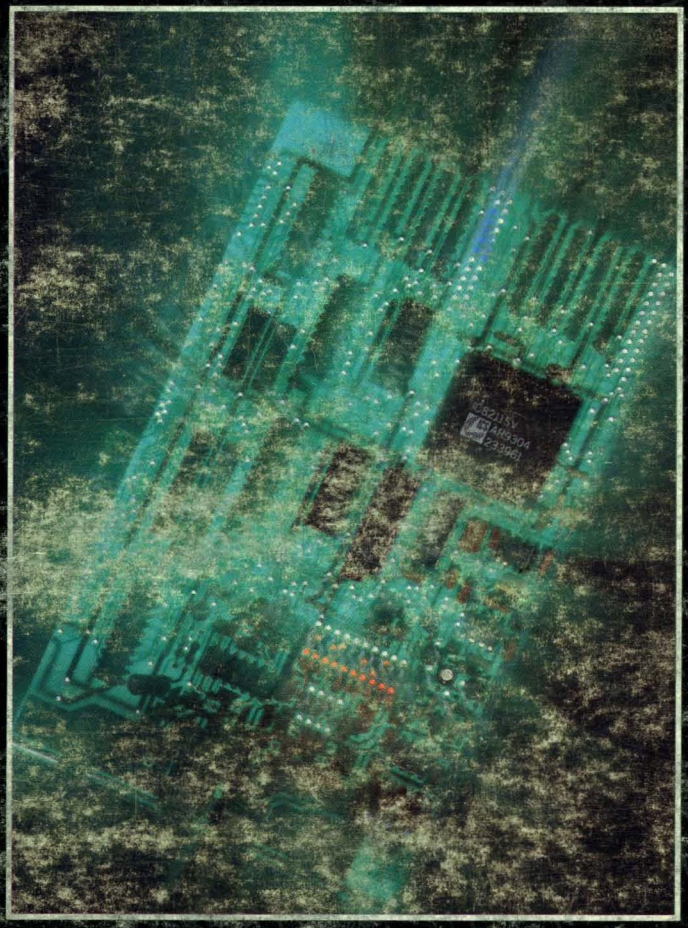
INTEGRATED CIRCUIT SYSTEMS, INC.



DATA BOOK
1994

ICS Product Data Book

ICS reserves the right to make changes in the device data identified in this publication without further notice. ICS advises its customers to obtain the latest version of all device data to verify that any information being relied upon by the customer is current and accurate.

ICS does not assume any liability arising out of or associated with the application or use of any product or integrated circuit or component described herein. ICS does not convey any license under its patent rights or the patent rights of others described herein. In the absence of a written or prior stated agreement to the contrary, the terms and conditions stated on the back of the ICS order acknowledgment obtain.

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ICS products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any nuclear facility application, or for any other application in which the failure of the ICS product(s) could create a situation where personal injury or death may occur. ICS will not knowingly sell its products for use in such applications, and the buyer shall indemnify and hold harmless ICS and its officers, employees, subsidiaries, affiliates, representatives and distributors against all claims, costs, damages, expenses, tort and attorney fees arising out of directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ICS was negligent regarding the design or manufacture of the part.

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Introduction

Integrated Circuit Systems, Inc. designs, develops and markets standard and application specific integrated circuits utilizing mixed analog/digital technology. Founded in 1976 to provide custom IC designs and product sourcing services to OEMs, ICS created its own sophisticated design tools, analog and digital cell libraries and quality assurance testing methods. In 1988, these unique tools and mixed signal design capabilities enabled ICS to create the first commercially viable video timing generator using advanced frequency synthesis technology. The ICS1394 pioneered the transition from multiple crystal oscillators to a single IC and emerged as the industry standard for producing the high frequency video dot timing function in IBM-compatible personal computers.

Integrated Circuit Systems merged with Avasem Corporation in November, 1992. Avasem was founded in 1980 to provide custom MOS integrated circuits and became a market leader in Phase Locked Loop (PLL) as well as mixed analog/digital integrated circuits. As individual companies, ICS and Avasem competed for market share in frequency timing generators. Today, as one company, ICS dominates the frequency synthesis market for CPU motherboards, workstations and PC graphics.

ICS has extended its knowledge of frequency timing into new products for PC multimedia sound and video. These include products that synchronize PC video images with live or recorded television video, and products that create real, digitized sound. To expand the capabilities of its PC sound/video design expertise, ICS formed the Multimedia Components Division in July, 1993 and merged with Turtle Beach Systems, Inc., a provider of PC-based hardware and software products for professional-quality sound generation and editing in multimedia applications.

Additionally, ICS is meeting the increasing demand for controlled, rapid NiCd or NiMH battery recharging for laptop and notebook computers with a family of power management integrated circuits.

ICS controls every phase of manufacturing and quality assurance at both locations. Our unique partnerships with international experts in wafer fabrication and assembly provide our customers with the highest quality and performance in each integrated circuit chip. We routinely produce both application specific integrated circuits (ASICs) and customized versions of our standard masks.

We are confident that ICS can provide you with the optimum IC solutions, outstanding customer service and dedication to quality to suit your needs.

Integrated Circuit Systems . . . Where the Digital World Meets the Real World.

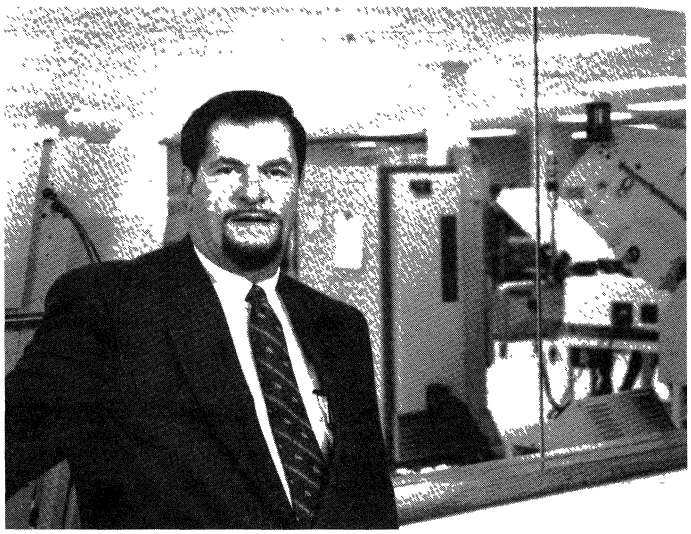
ICS: Committed to Quality and Reliability

At Integrated Circuit Systems, our goal is to produce and deliver products of exceptional quality and reliability. To achieve that goal, we dedicate our efforts to meeting your technical expectations, your delivery deadlines and your competitive pricing needs. We set our standards high. We take our commitment to you very seriously. At ICS we consistently strive:

- to maintain our world-class quality performance in the integrated circuit industry for both products and services;
- to establish a culture that focuses on continuous improvement and accepts the challenge for instituting ever higher levels of quality and reliability;
- to continue an effective total quality process that provides customers with products and services that meet or exceed:
  - specification requirements
  - performance requirements
  - quality expectations
  - support needs before and after delivery;
- to delegate the responsibility for quality to all ICS employees, with the emphasis on preventive actions.

In addition, we expect the same kind of quality and reliability from the wafer foundries and assembly sources we select. We constantly monitor their performance to ensure continued conformance to our standards.

ICS' ongoing commitment to quality and reliability is a company-wide policy that originates with management. It starts with your first phone call to ICS and is pursued through the design, production and delivery of your product.



Founder and Chairman, Edward Arnold, in front of ICS Production Facility.

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GENDAC is a trademark of Integrated Circuit Systems, Inc

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Pentium is a trademark of Intel Corporation.

ICS Product Selection Guide

Multimedia Products

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Video Graphics	GSP500	VGA/NTSC Genlock.	68 Pin PLCC	9
	GSP500 Application Notes			99
	GSP600	VGA/PAL Genlock.	68 Pin PLCC	23
	GSP600 Application Notes			131
	ICS1522	See High-Performance section.		541
Sound/Video Synchronization	ICS2008	SMPTE-MIDI Peripheral	44 Pin PLCC	61
	ICS2008A	Improved SMPTE-MIDI Peripheral		79
Sound	ICS2001	Sound Output Circuit, Parallel Port.	16 Pin DIP, SOIC	37
	ICS2002	Business Audio Codec	44 Pin PLCC	43
	ICS2101	5 Channel Digitally Controlled Audio Mixer.	28 Pin DIP, SOIC	81
	ICS2102	Sound Blaster™ Compatible Mixer.	28 Pin SOIC	89
	ICS2115	WaveFront Synthesizer	84 Pin PLCC	93
	CHIP SET ICS2116	WaveFront Interface	100 Pin QFP	94
	ICS2122	2-Megabyte Gen-Midi Sound ROM	44 Pin SSOP	95
	ICS2124-001, ICS2124-002	4-Megabyte General Midi Sound ROM Set	44 Pin SSOP	95

Sound Blaster is a trademark of Creative Technologies, Inc.

Video Timing Generator Products

PRODUCT APPLICATION	ICS DEVICE TYPE	FEATURES	MAX FREQUENCY	CLOCK OUTPUTS	PACKAGE TYPES	PAGE
P.C. Clock Generators	ICS1394	External Loop Filter. For New Designs Use ICS1494.	85 MHz	1 TTL	20 Pin DIP, SOIC	153
	ICS1494	Buffered Xtal Out, Lock Detect Output.	135 MHz	1 TTL	20 Pin DIP, SOIC	155
	ICS2494/ ICS2494A	Dual Video Memory Clock Generator with 16 Preprogrammed Video and 4 Preprogrammed Memory Frequencies.	135 MHz	2 TTL	20 Pin DIP, SOIC	161
	ICS2495	Small Footprint, Narrow Body SO Package.	135 MHz	2 TTL	16 Pin DIP, SOIC	167
	ICS2496	Low Voltage, 3/5 Volt Operation for Laptop/Notebook Applications. Power-down Mode.	85/135 MHz	2 TTL	16 Pin DIP, SOIC	173
	ICS2595	Programmable Dual ICS2494 Pin Compatible.	135 MHz	2 TTL	20 Pin DIP, SOIC	179
	ICS82C404	Dual Programmable Graphics Clock Generator. ICD82C404 Compatible.	120 MHz	2 TTL	16 Pin DIP, SOIC	189
	ICS9161	Dual Programmable Graphics Clock Generator. ICD2061 Compatible.	135 MHz	3 TTL	16 Pin DIP, SOIC	223
	AV9194	Dual Video Memory Clock Generator with 16 Preprogrammed Video and 4 Preprogrammed Memory Frequencies.	135 MHz	2 TTL	20 Pin DIP, SOIC	237
Western Digital Compatible Clock Generators	ICS90C61A	Drop-in upgrade for the WD90C61. Integral Loop Filters.	80 MHz	2 TTL	20 Pin DIP, SOIC PLCC	193
	ICS90C64A	WD90C31 VGA Controller Compatible. Enhanced Version. Integral Loop Filter. (Replaces ICS90C63, ICS90C64.)	135 MHz	2 TTL	20 Pin DIP, SOIC PLCC	203
	ICS90C65	Low Voltage, 3/5 Volt. Powerdown Mode. WD90C26 VGA Controller Compatible.	135 MHz	2 TTL	20 Pin DIP, SOIC PLCC	213

GENDAC™ Products

PRODUCT APPLICATION	ICS DEVICE TYPE	FEATURES	PACKAGE TYPES	PAGE
Personal Computer and Engineering Work Station Computer Graphics	ICS5300	Integrated Dual Clock. 8-bit Generic.	44 Pin PLCC	275
	ICS5301	Integrated Dual Clock. 8-bit Tseng Compatible.	44 Pin PLCC	303
	ICS5340	Integrated Dual Clock. 16-bit Generic.	68 Pin PLCC	331
	ICS5341	Integrated Dual Clock. 16-bit Tseng Compatible.	68 Pin PLCC	363

GENDAC is a trademark of Integrated Circuit Systems, Inc.

Motherboard Timing Generator Products

PRODUCT APPLICATION	ICS DEVICE TYPE	FEATURES	NUMBER OF OUTPUTS	NUMBER OF PLL s	PACKAGE TYPES	PAGE
Motherboard	ICS2407 ICS2409 ICS2439	IMI407, IMI409 and IMI439 Compatible.	6 9 9	2 2 2	18 Pin DIP, SOIC 24 Pin DIP, SSOP 24 Pin DIP, SSOP	369
	ICS2492	Buffered XTAL Out. Tristate PLL Outputs.	3	2	20 Pin DIP, SOIC	375
	ICS2494-244 ICS2494A-317	Buffered XTAL Out. Note: See Video Dot Clock Section for Data.	3	2	20 Pin DIP, SOIC	161
	ICS2694	9 Fixed, CPU-CPU/2 Selectable Provides CPU, Co-Processor, Hard and Floppy Disk, Kbd, Ser. Port, Bus Clk Function.	11	2	24 Pin DIP, SOIC	381
	AV9107	CPU Clock Generator.	2	1	8 or 14 Pin DIP, SOIC	387
	ICS9108	3 Volt CPU Clock Generator.	2	1	8 or 14 Pin DIP, SOIC	395
	AV9128/9	Motherboard Frequency Generator Outputs KBD Clock, System Clock, I/O Clock, Comm. Clock and CPU Clock.	8/11	4	16 or 20 Pin DIP, SOIC	403
	ICS9131	32 kHz Input Generates CPU Clocks.	3	2	16 Pin SOIC, PDIP	417
	ICS9132	32 kHz Input Generates all Motherboard Clocks.	6	4	20 Pin DIP, SOIC	425
	ICS9133	32 kHz Input Generates CPU Clock and System Clock and Two Fixed Clocks.	6	3	20 Pin SOIC, PDIP	435
	AV9140	R4000 Processor Series Master Clock Generator.	1	1	8 Pin DIP, SOIC	441
	AV9154	Low Cost 16 Pin Clock Generator. Generates CPU Clock, Keyboard Clock, System Clock and I/O Clock.	7	2	16 Pin DIP, SOIC	445
	AV9155	Motherboard Clock Generator. Produces CPU Clock, Keyboard Clock, System Clock and I/O Clock.	8	2	20 Pin DIP, SOIC	461
	ICS9158	Clock Generator with Integrated Buffers.	11	2	24 Pin SOIC	473
Laptop/Notebook	ICS2496-456	3V Operation, Buffered XTAL Out. Note: See Video Dot Clock Section for Data.	3	2	20 Pin DIP, SOIC	173
	AV9154-06/60	Clock Generator Designed Specifically for Use with OPTI Chipset.	4	2	16 Pin DIP, SOIC	455

Special Purpose ICs (Disk Drive, Low Skew (Pentium™)

PRODUCT APPLICATION	ICS DEVICE TYPE	FEATURES	NUMBER OF OUTPUTS	NUMBER OF PLL s	PACKAGE TYPES	PAGE
Motherboard	ICS1694A	Single Crystal Generates Three Low-Jitter Clocks.	3	1	8 Pin DIP, SOIC	481
	AV9110	User-Programmable "On-the-Fly"; Low-Jitter makes it Ideal for Disk Drive or Video Applications.	1	1	14 Pin DIP, SOIC	485
	ICS9123	High Resolution Clock Generator; One Channel has Accuracy to within 50 PPM making it Ideal for Modem, Ethernet and AD1848 Applications.	6	3	16 or 20 Pin DIP, SOIC	495
	AV9170	Clock Synchronizer and Multiplier.	2	1	8 Pin DIP, SOIC	497
	AV9172	Low Skew Output Buffer. Low Skew and Jitter make it Ideal for Pentium Applications.	6	1	16 Pin DIP, SOIC	511
	AV9173	Lost Cost Video Genlock PLL.	2	1	8 Pin DIP, SOIC	519
	ICS9175	Low Skew Output Buffer Crystal Generates Six Low Skew, Low-Jitter Clocks.	6	1	16 Pin DIP, SOIC	523
	ICS9176	Input Clock Generates IO Low Skew, Low-Jitter Outputs. Ideal for Pentium or PLI Applications.	11	1	28 Pin PLCC	529

Pentium is a trademark of Intel Corporation.

High-Performance Video Timing Generator Products

PRODUCT APPLICATION	ICS DEVICE TYPE	FEATURES	MAX FREQUENCY	CLOCK OUTPUTS	PACKAGE TYPES	PAGE
Workstation Clock Generators	ICS1522	User-Programmable Frequencies; 'Line Lock' Capability.	230 MHz	Diff ECL	24 Pin SOIC	541
	ICS1561	÷ 2, 4, 8 TTL Out. Integral Loop Filter. NOT RECOMMENDED FOR NEW DESIGN	180 MHz	Diff ECL	20 Pin DIP, SOIC	549
	ICS1561A	÷ 2,4,8 TTL Out. Integral Loop Filter. Replaces ICS1561.	180 MHz	Diff ECL	20 Pin DIP, SOIC	551
	ICS1562	User-Programmable Frequencies. RAMDAC™ Reset Logic (Brooktree Compatible).	230 MHz [320+MHz] [Special Pin]	Diff ECL	16 Pin Narrow SOIC	557
	ICS1567	32 Frequency ROM-based RAMDAC Reset Logic (Brooktree Compatible).	180 MHz	Diff ECL	20 Pin DIP, SOIC	575
	ICS1572	User-Programmable Frequencies. RAMDAC Reset Logic (Brooktree Compatible).	180 MHz	Diff ECL	20 Pin SOIC	585
	ICS2572	User-Programmable Dual PLL 16V + 4M Locations.	185 MHz	Diff ECL	20 Pin DIP, SOIC	603

Notes:
1. All products have internal loop filters except as noted.
2. All products operate at 5 volts typ. except as noted.

RAMDAC is a trademark of Brooktree Corporation.

Power Management Products

PRODUCT APPLICATIONS	ICS DEVICE TYPE	FEATURES	MINIMUM CHARGE RATE	PACKAGE TYPES	PAGE
NiCd Battery Charge Processor	ICS1700	NOT RECOMMENDED FOR NEW DESIGN	4C	16 Pin DIP 20 Pin SOIC	615
	ICS1700A	QuickSaver™ Controller for Fast Charge and Conditioning of NiCd Batteries.	4C	16 Pin DIP 20 Pin SOIC	617
NiCd Battery Charge Processor **NiMH Battery Charge Processor**	ICS1702	QuickSaverII Controller for Fast Charge and Conditioning of NiCd and NiMH Batteries.	4C IC	16 Pin DIP 20 Pin SOIC	633
Battery Charging and Capacity Measurement IC	ICS1705	SmartBat™ In-the-Pack Data Acquisition and Storage IC for Charge Control and Capacity Measurement.	N/A	8 Pin SOIC	653
Notebook PCs and PDAs Power Switching	AV9304/9504	Quad High-Side Switches 300mΩ R_{DS} On Slow Turn-on for Glitch-Free Operation.	N/A	16 Pin SOIC 16 Pin DIP	655
	AV9312/9512	Dual High-Side Switches 200mΩ R_{DS} On Slow Turn-on for Glitch-Free Operation.	N/A	14 Pin SOIC 14 Pin DIP	659

Note: C = Ampere/hour capacity of battery.

QuickSaver is a trademark of Integrated Circuit Systems, Inc.
SmartBat is a trademark of Integrated Circuit Systems, Inc.

Communications Products

PRODUCT APPLICATION	ICS DEVICE TYPE	COMMENTS	PACKAGE TYPES	PAGE
Caller I.D.	ICS1660	FSK Signal Interface Device.	18 Pin DIP 20 Pin SOIC	687

ICS

Multimedia

Products

At ICS, the digital world meets the real world with multimedia products for adding audio and motion video to computer and consumer electronics products. We combine our experience in phase-locked-loop, digital signal processing, and mixed-signal design to product multimedia ICs for OEMs around the world. Our solutions in audio and video are matched to OEM requirements for cost-effective products.

In video, ICS offers the GSP and 2008 product lines. The GSP family offers Genlocking to enable full-motion, computer-generated text and graphics to be overlayed on any standard video signal, such as TV, camcorder, VCR, or video disc. It also supports easy recording of the enhanced video image onto videotape. The 2008 production line implements VITC and LTC read and write of the standard SMPTE Time Code data, synchronized with MTC (midi time code) output.

In audio, ICS offers Wavedec™ and WaveFront.™ Wavedec, our digital audio codec for computer and consumer electronics products, records and plays 16 bit compatible files for applications running in MS DOS or MS Windows platforms. WaveFront, our wavetable synthesizer, creates the audio subsystem required for producing the full General MIDI patch set on next-generation, 16 bit sound cards and consumer electronics products.

Most importantly, we understand the systems-integration challenges of adding multimedia capabilities to your products. Our applications engineering team includes engineers responsible for the Multisound product from our Turtle Beach Systems division and for the Sensation™ multimedia computer from Tandy. ICS views our multimedia IC business as a systems business and we can assist you with your systems-integrations needs. We look forward to partnering with you and making you and your new products succeed in the marketplace.

Wavedec and WaveFront are trademarks of Integrated Circuit Systems, Inc

ICS Multimedia Product Selection Guide

Product Applications	ICS Device Type	Features	Package Types	Page
Video Graphics	GSP500	NTSC Genlock.	68 Pin PLCC	9
	GSP600	PAL Genlock.	68 Pin PLCC	23
Sound/Video Synchronization	ICS2008	SMPTE-MIDI Peripheral.	44 Pin PLCC	61
	ICS2008A	Improved SMPTE-MIDI Peripheral.		79
Sound	ICS2001	Sound Output Circuit, Parallel Port.	16 Pin DIP, SOIC	37
	ICS2002	Business Audio Codec.	44 Pin PLCC	43
	ICS2101	5 Channel Digitally Controlled Audio Mixer.	28 Pin DIP, SOIC	81
	ICS2102	Sound Blaster Compatible Mixer.	28 Pin SOIC	89
	ICS2115	Wavetable Synthesis.	84 Pin PLCC	93
	CHIP SET ICS2116	Wavetable Interface.	100 Pin QFP	94
	ICS2122	2-Megabyte Gen-Midi Sound ROM.	44 Pin SSOP	95
	ICS2124-001, ICS2124-002	4-Megabyte General Midi Sound ROM Set.	44 Pin SSOP	95

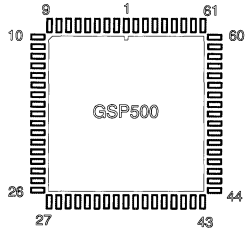
ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development Characteristic data and other specifications are subject to change without notice.

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development Characteristic data and other specifications are design goals. ICS reserves the right to change or discontinue these products without notice.

VGA/NTSC Video Genlock Processor with Overlay

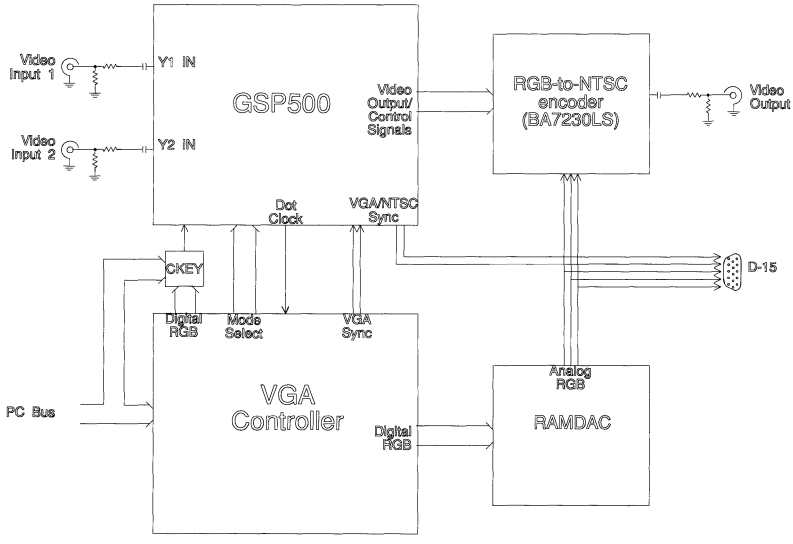
Overview

The **GSP500** allows the text and graphic images of VGA and Super VGA controllers to be displayed on standard NTSC televisions or recorded on a VCR. Additionally, the **GSP500** accepts external video input from a camcorder or a VCR and will synchronize (genlock) the VGA or Super VGA controller to the external video. The **GSP500** also allows VGA and video images to be overlaid on the same television screen. The **GSP500** meets or exceeds all RS-170A broadcast standards for timing accuracy and allows the VGA controller to maintain true NTSC compatibility at all times. The **GSP500** is compatible with virtually all VGA controllers. Tseng Labs, Oak Technology, Trident Microsystems, S3, and NCR already have full BIOS support available for the **GSP500**.

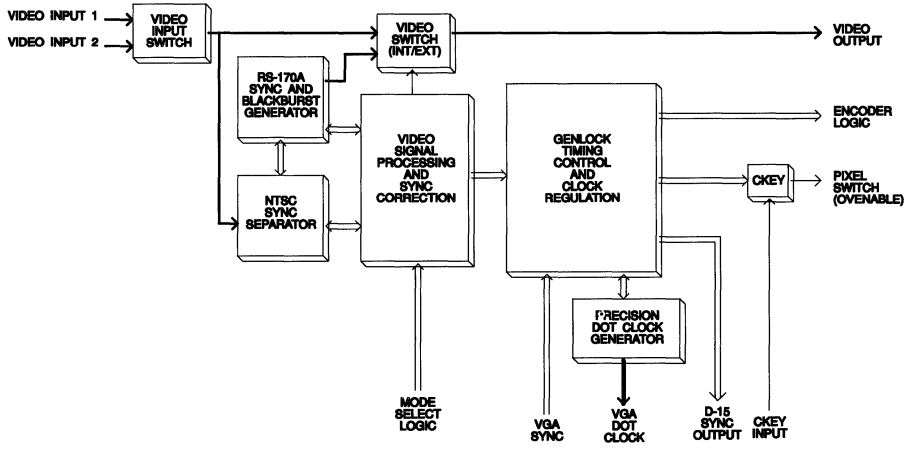


Features

- Direct input of NTSC or S-Video (S-VHS and Hi-8 video).
- On board NTSC/S-Video sync and black burst generation for local video operation. Video chroma burst separate with 3.579545 MHz and 14.31818 MHz phase locked outputs.
- Meets or exceeds alltiming specifications for studio and broadcast television.
- High efficiency NTSC/S-Video conversion that maintains VGA performance.
- Dynamic overscan and underscan adjustment of NTSC/S-Video modes under BIOS and/or software control.
- Software selection between all VGA and NTSC/S-Video modes.
- NTSC/S-Video conversion support for all VGA and Extended VGA modes with 480 or fewer lines.
- Built-in dot clock circuitry to eliminate crystal oscillators for VGA, plus extended VGA operation up to 135 Mhz.
- Low power consumption, ideal for laptop computers.



Internal Block Diagram



Theory of Operation

The **GSP500** can be thought of as an extremely sophisticated dot clock generator. In its simplest form, the **GSP500** will generate all of the dot clock frequencies necessary to drive VGA and Super VGA controllers. The different frequencies are selected with the **MODE SELECT LOGIC** from the VGA chip. Selection is similar to selecting frequencies on any of the ICS dot clock generators (i.e., ICS1394, ICS1494, ICS1561, ICS2494, etc.). Additionally, there are four reserved frequency addresses. These are labeled GL (genlock), OV (overlay), VO (video only), and GO (graphics only). Choosing any of these addresses will switch the **GSP500** from VGA mode to NTSC mode. Under NTSC mode, the **GSP500** accepts vertical and horizontal **VGA SYNC** from the VGA controller and uses the sync to generate and adjust the **VGA DOT CLOCK**. The **GSP500** will automatically vary the frequency of the dot clock in order to synchronize the VGA sync signals with an NTSC reference signal. This reference signal can be derived from a video device (such as a camcorder) connected to **VIDEO INPUT 1** or **VIDEO INPUT 2**. The **GSP500** provides an RGB-to-NTSC encoder with the **VIDEO OUTPUT** signal which is either **VIDEO INPUT 1**, **VIDEO INPUT 2**, or an internally generated black burst signal. All of the necessary **ENCODER LOGIC** signals to properly drive the encoder are provided by the **GSP500**. During NTSC modes the **GSP500** also creates the **D-15 SYNC OUTPUT** for the monitor connection to allow for TV projection output of the VGA images. The **PIXEL SWITCH** information derived from external **CKEY INPUT** tells the encoder whether to display the VGA image or external video for each pixel. Assuming the images are genlocked, this creates the overlay effect.

Block definition

Video Input Switch

The Video Input Switch selects whether the **GSP500** uses VIDEO INPUT 1 or VIDEO INPUT 2 as the external video source. It is controlled by an external pin of the **GSP500**.

NTSC Sync Separator

The **GSP500** contains a high quality sync separator to allow direct input of NTSC, S-VHS, or HI-8 video signals from camcorders, VCRs, and other video products. The **GSP500** utilizes a differential video input circuitry for maximum noise immunity. It also employs digital noise filtering and enhanced digital signal tracking technology to ensure maximum compatibility with consumer, industrial, and broadcast video signals. Although low cost video sync separator products are commonly available, they are primarily designed for television and video monitor use. The simple diode clamping circuit used in these devices does not have the accuracy or noise immunity required for genlocking.

RS-170A Sync and Black Burst Generator

RS170A Sync Generator

The studio quality built-in video sync generator allows the **GSP500** to operate without an external video input and still maintain broadcast video timing. This assures NTSC compatibility at all times. When external video is present, the sync generator works in conjunction with the sync separator to isolate sync from noisy video signals.

Black Burst Generation

Most RGB-to-NTSC encoders synchronize a crystal oscillator to the chroma burst signal of the external video signal. This provides the color reference portion of the video signal. If an external video signal is not available, the crystal oscillator will free run, creating screen artifacts such as 45 degree moving lines in constant color portions of the screen. To eliminate this problem, the **GSP500** generates a black burst video signal. Black burst video is an analog signal containing both sync and a correctly phased chroma burst signal. This ensures proper color reference generation at all times. The **GSP500** provides black burst output to the encoder when external video is either missing or not selected (non-genlock mode).

INT/EXT Video Switch

The Internal/External Video Switch determines whether the encoder uses external video or the black burst signal. If external video is chosen, the **GSP500** will simply pass the external video signal through to the encoder, unaffected. Black burst is used when external video is not present. The switch is controlled by the Video Signal Processing and Sync Correction circuitry.

Video Signal Processing and Correction

Video Signal Processing

The Video Signal Processing circuitry of the **GSP500** measures the incoming video signal for basic timing accuracy and signal noise. It contains intelligent circuitry to remove extraneous portions of the video signal that would normally be incorrectly categorized as sync. This is extremely important when using a VCR as a video input. If there is an interruption of the external video signal, this circuit will automatically switch inputs from the external video signal to the internal sync generator. When the external video signal resumes, the circuit will automatically switch back to the external video. The Video Signal Processing accepts the MODE SELECT LOGIC from the VGA chip. This logic chooses either VGA or NTSC operation and selects whether genlock to external video is to be enabled.

Sync Correction

The Sync Correction circuitry looks for missing sync pulses, block sync, single field video, and phase shift errors caused by the head switching zone of a VCR. It assures proper genlock during all of these problems common in consumer video products.

Genlock Timing Control and Clock Regulation

The **GSP500** looks at the input sync from the VGA controller and determines how to alter the dot clock to create RS-170A timing. Both the frequency and the method can change with different VGA modes. The **GSP500** enables virtually any VGA controller capable of interlacing to create RS-170A timing. The **GSP500**'s unique architecture provides ultra-high efficiency and flexibility and allows the frequency of the dot clock to be controlled totally under BIOS or software control. Screen attributes such as horizontal width and position can be individually programmed for each mode while maintaining genlock integrity. This circuit will modify the timing of virtually any mode, with 480 or fewer lines, to meet RS-170A NTSC specifications. The **GSP500** genlock timing control and clock regulation design is awaiting patent approval.

Precision Dot Clock Generator

The **GSP500** uses the same state-of-the-art dot clock technology that has made ICS the premier supplier of VGA dot clock generators. ICS offers the highest accuracy and lowest jitter products available.

CKEY

The ckey (or color-key) circuitry creates the pixel switch for the encoder. This signal determines whether the VGA image or external video is displayed for each pixel. Ckey is modified by the **GSP500** to ensure that the pixel switch signal is delayed (to make up for delays in the RAMDAC) and that it has proper levels during sync and blanking. If the VGA and external signals are genlocked, this pixel switch will create an overlay effect.

PIN NUMBER	NAME	DESCRIPTION
1	VLE	VERTICAL LOCK ENABLE. HIGH for VGA controllers. LOW disables vertical lock feature, may be useful for Non-VGA Operation.
2	ODD/EVEN	ODD/EVEN FIELD IDENTIFICATION. HIGH indicates odd numbered field, LOW indicates even numbered field.
3	BP	BACK PORCH PULSE. Negative polarity TTL level signal used by some RGB-to-NTSC encoders.
4	DATAIN	Data input for inserting SMPTE time code in video signal.
5	CB	COMPOSITE BLANKING OUTPUT. Indicates non-screen data portions of NTSC signal.
6	CS	COMPOSITE SYNC. NTSC Composite sync output for RGB-to-NTSC encoders. Gated off during VGA modes.
7	CKEY	COLOR KEY. Resultant input from the 8-bit compare of digital RGB (P0-P7) and a software selectable byte. This color key determines which pixels display VGA and which display external video in overlay mode. See Hardware Interface Manual for more details.
8	TEST	For ICS use only.
9	VSYNCOUT	VERTICAL SYNC OUTPUT. Vsync output for DB-15 connector.
10	DATAFRAME	TTL level framing signal active during lines 10-20. For use in time code applications.
11	OVENABLE	OVERLAY ENABLE. Fast pixel rate switch. HIGH displays NTSC output, LOW display RGB output. Used for overlay encoders. See Application Notes for wiring details.
12	I/ES	INT./EXT. SYNC. Determines sync selection in OVENABLE signal. Tie LOW normally.
13	LOC/REM	LOCAL/REMOTE. A LOW output state signifies REMOTE status indicating that external video is present and a genlock mode has been selected. If external video goes away or a non-genlock mode is selected, LOCAL/REMOTE will go HIGH.
14	BRSTACT	For ICS use only.
15	$\overline{\text{FRTSTOUT}}$	For ICS use only, wire to pin 37.
16	HS	HORIZONTAL SYNC. For some RGB-to-NTSC encoders. Gated off during VGA modes.
17	$\overline{\text{HRSTOUT}}$	For ICS use only.
18	HSYNCOUT	HORIZONTAL SYNC OUTPUT. Hsync output for DB-15 connector.
19	VSS	Digital ground. We strongly recommend the use of a multilayer board and a ground plane.
20	VDD	5 Volt digital power. We strongly recommend the use of a multilayer board and a power plane.
21	VDD	5 Volt digital power. We strongly recommend the use of a multilayer board and a power plane.
22	VSS	Digital ground. We strongly recommend the use of a multilayer board and a ground plane.
23	FS5	Frequency Select 5. Selects between multiple VGA Dot Clock frequencies, Genlock modes and NTSC frequencies. See Dot Clock Generation and NTSC Mode Selection sections for a more detailed description. Also see Application Notes for wiring diagrams and BIOS Interface Manual for details.

PIN NUMBER	NAME	DESCRIPTION
24	FS4	Frequency Select 4. Selects between VGA Dot Clock frequencies and NTSC modes.
25	FS3	Frequency Select 3. Selects between VGA Dot Clock frequencies and NTSC modes.
26	FS2	Frequency Select 2. Selection between VGA Dot Clock frequencies and NTSC modes.
27	FS1	Frequency Select 1. Selects betweenVGA Dot Clock frequencies and NTSC modes.
28	FS0	Frequency Select 0. Selects between VGA Dot Clock frequencies and NTSC modes.
29	EXTSYNC	For ICS use only.
30	VCR1	HIGH permits using VCRs as an input.
31	CLAMPLEV	Clamping level adjustment for video input. See Application Notes for more details.
32	Y2	NTSC video input number 2. Note: This is also the Y (luminance) input for S-Video systems.
33	Y1	NTSC video input number 1. Note: This is also the Y (luminance) input for S-Video systems.
34	C2	C (Chrominance) input number 2 for S-Video systems.
35	C1	C (Chrominance) input number 1 for S-Video systems.
36	3.58SC	3.579545 MHz SUBCARRIER OUTPUT. Phase-locked to the chroma burst signal to allow encoders to maintain proper SCH phasing.
37	$\overline{\text{FRSTIN}}$	For ICS use only, wire to pin 15.
38	AVDD	5 Volt analog power. We strongly recommend the use of a multilayer board and a power plane.
39	GFF	Inverts field 1 and field 2 of VGA sync. Normally tied HIGH.
40	VCOLF	VCO LOOP FILTER CIRCUIT. External RC circuit used in VCO circuitry. See Application Notes for component values.
41	SYNCTHRS	Sync threshold adjustment for video input. See Application Notes.
42	VGAO/E	VGA ODD/EVEN FIELD IDENTIFICATION. HIGH indicates odd numbered field, LOW indicates even numbered field.
43	$\overline{\text{COUT}}$	C (Chrominance) OUTPUT. C output for S-Video systems.
44	$\overline{\text{RST}}$	Chip reset pulse. This to be tied high through a resistor. Do not tie to the computer reset line.
45	YOUT	Y (Luminance) OUTPUT. NTSC video output when the NTSC/SVID input is in the HIGH state. Y output for S-Video systems when the NTSC/SVID input is in the LOW state.
46	$\overline{\text{HALIGNOUT}}$	For ICS use only, wire to pin 62.
47	SYSLF	SYSTEM CLOCK LOOP FILTER CIRCUIT. External RC circuit used in the chroma burst phase locking circuit. See Application Notes for component values.
48	XTALI	14.31818 MHz crystal circuit. See Application Notes for parts specifications and wiring diagrams.
49	XTALO	14.31818 MHz crystal circuit. See Application Notes for parts specifications and wiring diagrams.

PIN NUMBER	NAME	DESCRIPTION
50	AVSS	Analog ground. We strongly recommend the use of a multilayer board and a ground plane.
51	VID1/2	Input selector. High for Y1/C1, Low for Y2/C2.
52	VCOOUT	For ICS use only, do not wire.
53	FILTSEL	For ICS use only, wire to pin 57.
54	DOTCLOCK	Clock signal input for VGA chip.
55	$\overline{\text{VFF}}$	Inverts field 1 and field 2 of NTSC sync. Normally tied HIGH.
56	$\overline{\text{VCR2}}$	LOW modifies sync characteristics to permit operation with VCR input.
57	VGA/NTSC	Mode identification output signal. HIGH indicates a VGA mode, LOW indicates an NTSC mode.
58	$\overline{\text{BG}}$	BURST GATE PULSE. Negative polarity TTL level signal used by RGB-to-NTSC encoders.
59	LOC/REM IN	For ICS use only, wire to pin 13.
60	VGAHSYNC	VGA HORIZONTAL SYNC. HSYNC signal from VGA chip. See BIOS Interface Manual for programming details.
61	VGAVSYNC	VGA VERTICAL SYNC. VSYNC signal from VGA chip. See BIOS Interface Manual for programming details.
62	$\overline{\text{HALIGNIN}}$	For ICS use only, wire to pin 46.
63	NTSC/SVID	NTSC/S-VIDEO. Selects between NTSC and S-Video output. HIGH= NTSC; Low= S-Video.
64	VS	VERTICAL SYNC. NTSC Vsync output for RGB-to-NTSC encoders. Gated off during VGA modes.
65	4XSC	4 TIMES SUBCARRIER OUTPUT. 14.31818 MHz signal phase-locked to the chroma burst signal.
66	PCLK	PCLK from VGA chip.
67	DATAOUT	TTL level output. This reads data during lines 10-20 and outputs it as a digital signal. For use in time code applications.
68	SCH	SCH PULSE. Positive polarity TTL level signal to distinguish between fields 1 and 3 or 2 and 4. Not necessary for most encoders.

BIOS Programming Example

BIOS support is currently available from Tseng Labs, Oak Technology, Trident Microsystems, S3, and NCR. Other VGA manufacturers have support programs underway. If you use one of these VGA controllers that have completed BIOS support, you can ignore this section. The following information may be helpful to VGA manufacturers and software developers. These tables represent register settings one particular VGA controller. Others are listed in the BIOS Interface Manual. This particular controller does not interlace text modes and uses an 8 x 8 font for modes 0, 1, 2 , 3, and 7. The horizontal registers are adjusted to produce underscan for text modes and overscan for graphics modes.

Horizontal CRTC Registers

CRTC INDEX	CRTC REGISTER	Modes: 00, 01, 04, 05, 0D	Modes: 02, 03, 06, 07, 0E, 0F, 10	Modes: 11, 12, 13
00	HT	35	6B	66
01	HDE	27	4F	4F
02	SHB	2A	53	52
03	EHB	96	8B	87
04	SHR	30	5B	58
05	EHR	92	83	80

Vertical CRTC Registers

CRTC INDEX	CRTC REGISTER	200 Line Modes: (Non-Interlaced) 00, 01, 02, 03, 07, 04, 05, 06, 0D, 0E, 13	350 Line Modes: (Interlaced) 0F, 10	480 Line Modes: (Interlaced) 12, 13
06	VT	05	05	05
07	OVERFLOW	11	11	11
10	VRS	E0	D3	F4
11	VRE	84	87	88
12	VDE	C7	AE	EF
15	SVB	DC	CF	F0
16	EVB	F2	E5	06

Note: The MSB of the MSL register (INDEX 09) must be turned OFF in 200 line NTSC modes. When using an 8 x 8 font for text (modes 00, 01, 02, 03, 07) the 4 LSB of this register will change from F to 7.

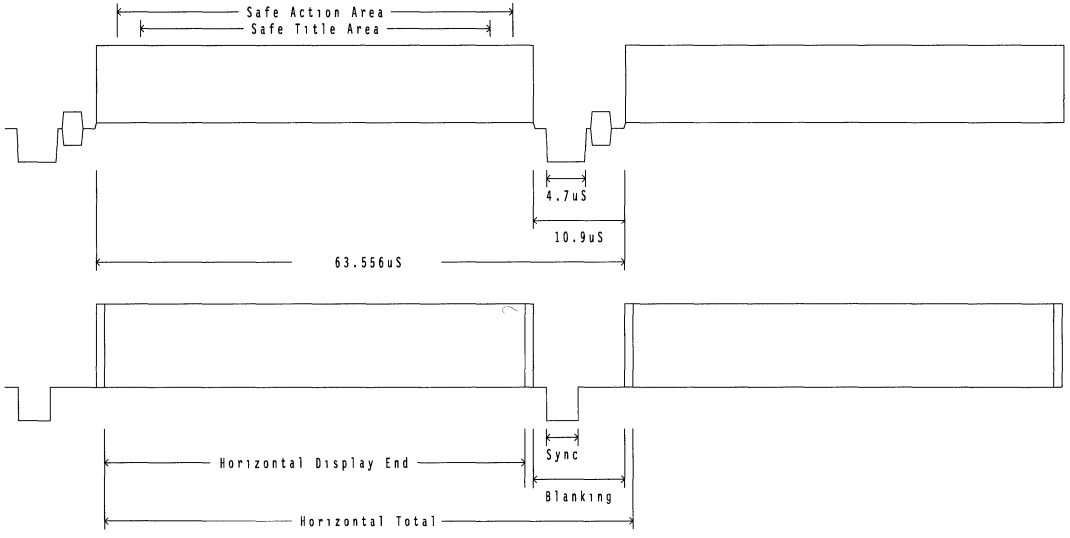
Miscellaneous Output Register

NTSC mode	Color Modes: 00, 01, 02, 03, 04, 05, 06, 0D, 0E, 10, 11, 12, 13	Monochrome Modes: 07, 0F
Genlock (GL)	23	22
Overlay (OV)	27	26
Video Only (VO)	2B	2A
Graphics Only (GO)	2F	2E

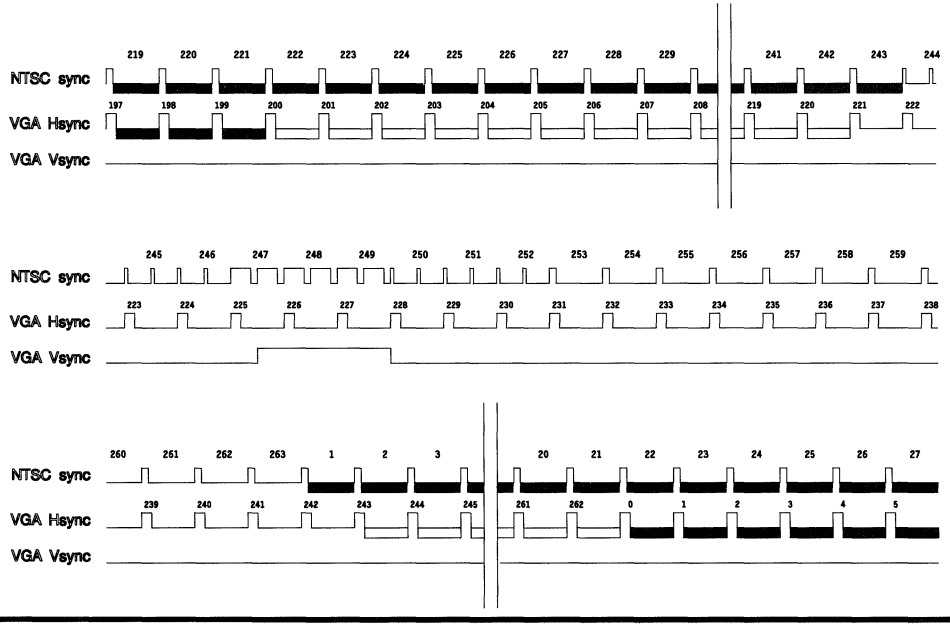
Extended Registers

Turn OFF all DOTCLOCK/2 bits.

NTSC vs. VGA Horizontal Timing



NTSC vs. VGA Vertical Timing (200 line mode)



Electrical Specifications

Operating temperature range 0 °C to 70 °C

Electrical Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
A_{VDD}	Analog Supply	4.5	5.0	5.5	Volts
D_{VDD}	Digital Supply	4.5	5.0	5.5	Volts
I_{DD} (VGA)	Operating Current - VGA Mode		35		mA
I_{DD} (NTSC)	Operating Current - NTSC Mode		50		mA

Input Signals

SIGNAL TITLE	PIN #	TYPICAL VALUE	OPERATING CONDITIONS
Y1	33	1 V_{P-P}	75 Ohm load
C1	35	1V_{P-P}	75 Ohm load
Y2	32	1V_{P-P}	75 Ohm load
C2	34	1V_{P-P}	75 Ohm load
VID1/2	51	TTL/CMOS	High = Y1,C1; Low = Y2,C2
NTSC/SVID	63	TTL/CMOS	High = NTSC; Low = S-Video
VGAVSYNC	61	TTL/CMOS	Positive polarity
VGAHSYNC	60	TTL/CMOS	Positive polarity
FS0-5	28-23	TTL/CMOS	Address/mode select
CKEY	7	TTL/CMOS	High = RGB; Low = NTSC
PCLK	66	TTL/CMOS	Pixel (DAC) Clock from VGA
I/ES	12	TTL/CMOS	High = Internal sync Low = External sync
DATAIN	4	TTL/CMOS	Active during DATAFRAME
CLAMPLEV	31	1-1.5 V	
SYNCTHRS	41	CLAMPLEV + 0.1 V	
VLE	1	TTL/CMOS	Tie to V_{DD} through resistor
RST/	44	TTL/CMOS	Tie to V_{DD} through resistor

Output Signals

SIGNAL TITLE	PIN#	TYPICAL VALUE	OPERATING CONDITIONS
VSYNCOUT	9	TTL	Positive polarity during NTSC modes
HSYNCOUT	18	TTL	Composite sync during NTSC modes
VS	64	$1V_{P-P}$	Positive polarity
HS	16	$1V_{P-P}$	Positive polarity
CS	6	$1V_{P-P}$	Positive polarity
DOTCLOCK	54	TTL	
YOUT	45	$1V_{P-P}$	75 Ohm load
COUT	43	$1V_{P-P}$	75 Ohm load
3.58SC	36	TTL	3.579545 MHz
4XSC	65	TTL	14.31818 MHz
LOC/REM	13	TTL	High = local; Low = remote
OVENABLE	11	TTL	High = NTSC; Low = RGB
VGA/NTSC	57	TTL	High = VGA; Low = NTSC
CB	25	TTL	Positive polarity
ODD/EVEN	2	TTL	High = odd field; Low = even field
VGAO/E	42	TTL	High = VGA odd field Low = VGA even field
BG/	58	TTL	Negative polarity
FP/	3	TTL	Negative polarity
SCH	68	TTL	Positive polarity
DATAFRAME	10	TTL	Lines 10-20
DATAOUT	67	TTL	Active during DATAFRAME

Dot Clock Selection

The following charts represent two of the many dot clock frequency selection tables supported by **GSP500**. See the BIOS manual or contact ICS applications engineering for additional information.

FREQUENCY (MHz)	FS5	FS4,FS3,FS2	FS1	FS0
50.350	0	1	0	0
56.644	0	1	0	1
65.028	0	1	1	0
72.000	0	1	1	1
75.000	1	0	0	0
80.000	1	0	0	1
89.800	1	0	1	0
110.000	1	0	1	1
Gen**L**ock	1	1	0	0
OVerlay	1	1	0	1
Video **O**nly	1	1	1	0
Graphics **O**nly	1	1	1	1

FREQUENCY (MHz)	FS5,FS3	FS4, FS2	FS1	FS0
25.175	0	1	0	0
28.322	0	1	0	1
40.000	0	1	1	0
44.900	0	1	1	1
Gen**L**ock	1	1	0	0
OVerlay	1	1	0	1
Video **O**nly	1	1	1	0
Graphics **O**nly	1	1	1	1

GSP500 Frequently Asked Technical Questions.

1. What will the GSP500 do for me?

The GSP500 adjusts the timing of a VGA controller to conform to RS-170A NTSC (television) specifications. The GSP500 accepts direct video input from video cameras, videodisc players or other video sources and will synchronize (genlock) a VGA controller to either the external video input or an internal NTSC sync generator. The GSP500 also contains a dot clock generator to eliminate the need for crystal oscillators or other dot clock generators.

2. How does the GSP500 differ from other genlock devices?

Other genlock devices, such as the Motorola MC1378, are very effective at genlocking two NTSC signals together and are generally used in consumer electronics products such as video window-in-a-window devices. The GSP500 is specifically designed to genlock a computer graphics controller to NTSC video and overcomes all of the incompatibilities between VGA and NTSC. Additionally, the GSP500 contains an NTSC sync generator and maintains chrominance phase lock in local modes. This allows the GSP500 to maintain RS-170A NTSC timing without an external video input. Furthermore, the sync separator circuit of the GSP500 is designed to satisfy the low jitter tolerances demanded by discriminating VGA customers.

3. Isn't genlock simply a phased-lock loop?

Phase locking two similar signals is fairly straightforward as long as phase jitter is not critical. As an example, ICS is one of the few companies able to successfully build phase-locked loop dot clock generators with low enough phase jitter for computer graphics display. Additionally, the differences between VGA and NTSC signals further complicate the genlock procedure. The GSP500 has patents applied for for the most advanced computer video genlock methods in the industry. These methods assure you of the highest possible quality product.

4. Most Genlock and Overlay products have a lot of discrete components with trimmer capacitors and potentiometers. All these adjustments can become very expensive in a mass production environment. How much external circuitry does the GSP500 require?

Although the GSP500 can be run with no trimmer capacitors or potentiometers, one trimmer capacitor should be used to meet the NTSC frequency tolerance of the chroma burst. This is a free running frequency and is very simple (and fast) to adjust. Additionally, the GSP500 uses high speed digital circuitry to eliminate virtually all discrete components. Only a few external components are needed for full operation.

5. Do I need an RGB-to-NTSC encoder with the GSP500?

Yes, an external RGB-to-NTSC encoder is needed. The encoder must be matched to the target audience. The GSP500 can be used under broadcast television scrutiny and most broadcast video equipment perform the encoding entirely with discrete components. As this may prove too costly and/or may use too much board space, the GSP500 contains all of the necessary signals to drive virtually any encoder. The GSP500's generous supply of timing signals will also drive external circuitry to turn off the encoder for laptop applications.

6. Why do I need the GSP500. Can't I program a VGA controller for NTSC sync and just drive an RGB-to-NTSC encoder?

NTSC sync contains equalizing pulses, blanking signals and pulse widths that are impossible to create under normal VGA control. Although marginal display quality is achievable on a television without adhering to the RS-170A standard, compatibility with other NTSC equipment is compromised. As an example, depending on which edge of horizontal sync the monitor triggers on will determine how far an incorrect width horizontal sync pulse will skew the screen. Additionally, it becomes virtually impossible to assure proper chroma burst (SCH) phasing. The GSP500 sync generator meets or exceeds all NTSC RS-170A broadcast standards for timing accuracy assuring you of maximum compatibility and ultimate quality.

7. National sells a sync separator for less than $2 while the Brooktree part costs over $50. What is the difference and how does the sync separator in the GSP500 compare?

The sync separation circuitry in the National part is a simple diode clamp. Although this may be adequate for driving a picture tube, the lack of noise and jitter immunity make it unsuitable for genlock applications. Additionally, the analog vertical sync detection circuit of these type of devices will not accurately track a VCR signal. The Brooktree device represents a mixed-mode approach to sync separation. By utilizing a fast analog circuitry coupled with high speed digital logic, noise and jitter immunity can be optimized. The GSP500 also uses a mixed mode approach specifically optimized for genlock operation yet the incorporation of a sync generator allows signal analysis not possible with other devices.

8. Is the GSP500 compatible with any VGA controller?

VGA controllers need to have two features to work with the GSP500. First, they need to be able to interlace - if your controller can display 1024 x 768 resolution, then it can probably interlace (the additional 256K memory is not necessary). Second, the controller must have at least three clock select lines for external dot clock generator support. Virtually all current VGA controllers have this feature. Check with your VGA controller manufacturer or ICS if you are unsure.

9. How do I turn the NTSC on and off and control it?

The GSP500 uses the three clock select lines to support 4 VGA clocks and 4 NTSC modes. The VGA clocks are available in 7 different patterns (i.e. 25.175, 28.322, 40.000, 65.000 is one pattern). The 4 NTSC modes are Genlock, Overlay, Graphics Only, and Video Only. The selection between any NTSC mode or between NTSC and VGA is done entirely under BIOS or software control.

10. Why did you incorporate a dot clock generator in the GSP500?

The GSP500 works by modifying the dot clock input for the VGA controller. It essentially is a dot clock generator designed for NTSC genlock. The dot clock generator is not so much of an extra feature as it is a subset of the genlock design. Consequently, this unity design assures you of a reliable glitch-free solution.

11. When the GSP500 displays an Overlay, how do I determine which part of the screen displays graphics and which is VGA?

The GSP500 uses a technique called Color-Key to determine where to display the external video. This Color-Key color is based on the VGA color number. Therefore, no colors are actually lost. As an example, the background color is always Color 0. When Color-Keying on Color 0, the screen will appear to have a background of the external video. The actual color that the VGA assigns to Color 0 does not matter. Any of the 256 color numbers can be assigned to be a Color-Key. Although the GSP500 modifies the Color-Key input, the Color-Key selection is done by an external 8 bit digital compare.

12. Why is the Color-Key selection external to the GSP500?

Color-Key selection is done with an 8 bit compare of the digital RGB signals with a preassigned byte. The digital RGB data comes from the VGA controller and the preassigned byte normally comes from the IBM bus via a port selection. The output of this comparison is fed into the CKEY (Color-Key) input of the GSP500. Although this Color-Key method will satisfy 95% of all customers, the external design allows other schemes with multiple or different comparison options. Additionally, since all of these signals are already available inside the VGA controller, many manufacturers have announced plans to incorporate the Color-Key function inside the VGA controller.

13. What about PAL and/or SECAM compatibility?

ICS is presently working on a PAL version of the GSP500. In its current implementation, it will be pin compatible with the GSP500 but require different values for the discrete components and will also need a different crystal oscillator. Although a SECAM version is technically possible, due to the uncertain market potential product development is not currently underway.

14. Can I look forward to a combination PAL and NTSC product?

Unfortunately, the amount of circuitry common to both a PAL and an NTSC version is minimal. Separate versions are currently the lowest cost solution. Although the crystal frequency, some discrete components and the Bios would have to change, the same board layout could support both standards by simply changing the parts list.

15. Does the GSP500 accept multiple video inputs? What about an S-Video input?

The GSP500 has two independent video inputs. Either input can be used or they can both be disabled. Either input can be wired to accept either S-Video or NTSC. Selection between the two inputs is performed under hardware control.

16. Why doesn't the GSP500 incorporate audio?

The NTSC and S-Video baseband signals do not have a provision for audio. This means that the video and audio signals are completely separate signals at all times. ICS offers audio products for the multimedia market that can be incorporated into the design but allows the designer maximum flexibility by keeping them separate products.

17. Can I use the GSP500 with an RF modulator?

Yes, but the quality of the image may suffer. When NTSC is modulated up to RF frequencies, audio is modulated onto a 4.5 MHz carrier and the video is limited to a maximum frequency of 4.2 MHz. Although 4.2 MHz may be sufficient for moving images it can be limiting for high resolution computer graphics. This problem is magnified because the majority of RF modulators are very low quality devices. Additionally, even if a high quality RF modulation is obtained, the signal may still be degraded by the RF demodulator inside the television set. ICS does recognize the these limitations may be outweighed by the user-friendliness and compatibility of the RF standard. High quality RF modulators are available and the GSP500 does have the necessary signals for support but these issues should be carefully weighed before implementation.

18. Can the GSP500 display NTSC video on my VGA screen?

No, in order to display NTSC video at 31.5 KHz, it is necessary to convert NTSC into component form, digitize it in real time, and store at least one frame of video. Although technology exists to accomplish this, the price-to-performance ratio of these products is too high for mass market acceptance at this time.

19. Is there any question that I forgot to ask?

Yes, when I use a graphics program, I find the borders very distracting yet I need the borders in text modes to insure that I can read the DOS prompt. Can the GSP500 help me with this problem? The GSP500 has the ability to adjust the width of the screen totally under Bios control. This means that you can have limited overscan in mode 13, minor underscan in mode 3 and generous overscan in mode 12. Software drivers can even be written to dynamically change the screen width with the cursor keys.

20. Does this mean I can change the height of the screen also?

NTSC has a fixed number of lines. In order to change the vertical size, the screen data must be compressed or expanded into fewer or greater lines. This can be accomplished in a text mode by changing the font size or in a graphics mode with linear interpolation. The GSP500 always maintains an exact one-to- one correlation between the NTSC and VGA line position and therefore does not support vertical sizing.

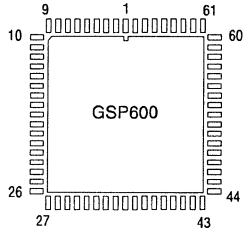
21. Where do I get a development kit for the GSP500?

Call ICS at (800) 220-3366 for more information. We will put you in touch with a local rep. who will be more than happy to supply you with a full GSP500 development kit. The ICS full service support organization is always ready to help you with the latest in Multimedia solutions.

VGA/PAL Video Genlock Processor with Overlay

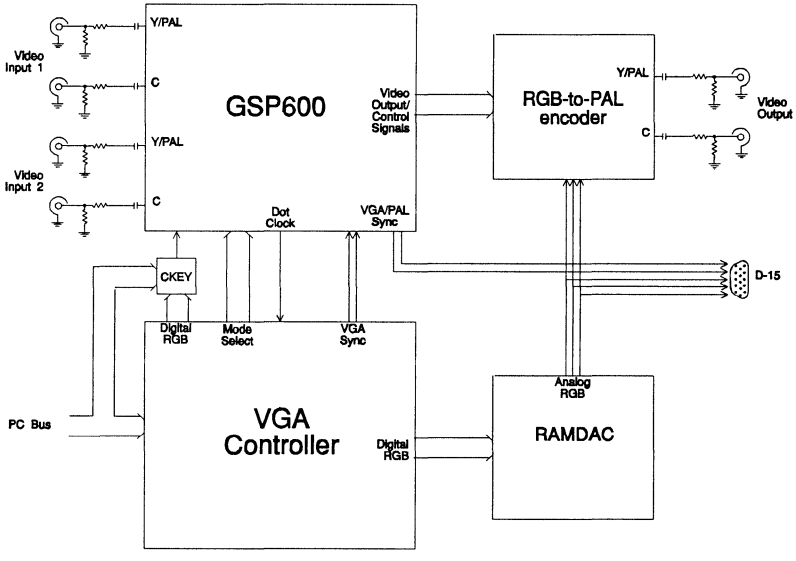
Overview

The **GSP600** allows the text and graphic images of VGA and Super VGA controllers to be displayed on standard PAL televisions or recorded on a VCR. Additionally, the **GSP600** accepts external video input from a camcorder or a VCR and will synchronize (genlock) the VGA or Super VGA controller to the external video. The **GSP600** also allows VGA and video images to be overlaid on the same television screen. The **GSP600** meets or exceeds all PAL broadcast standards for timing accuracy and allows the VGA controller to maintain true PAL compatibility at all times. The **GSP600** is compatible with virtually all VGA controllers. Tseng Labs, Oak Technology, Trident Microsystems, S3, and NCR have BIOS support available for the GSP family of products.

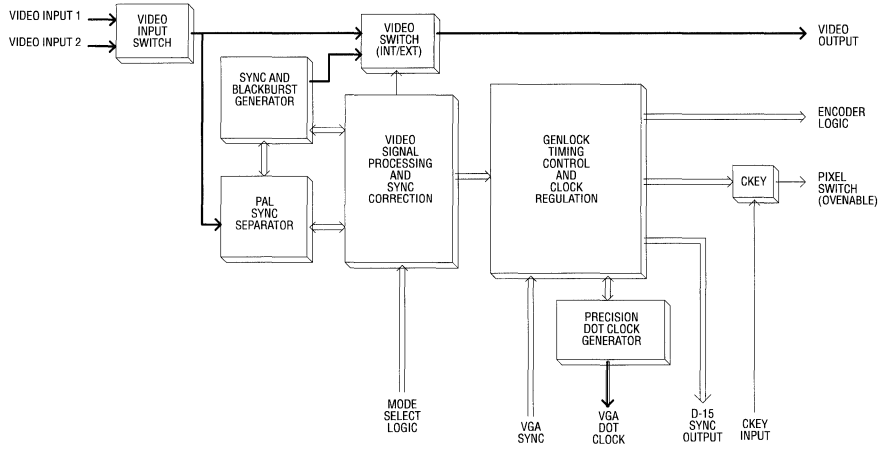


Features

- Direct input of PAL or S-Video (S-VHS and Hi-8 video).
- On board PAL/S-Video sync and black burst generation for local video operation. Video chroma burst separate with 4.433618 MHz and 17.734475 MHz phase locked outputs.
- Meets or exceeds all timing specifications for studio and broadcast television.
- High efficiency PAL/S-Video conversion that maintains VGA performance.
- Dynamic overscan and underscan adjustment of PAL/S-Video modes under BIOS and/or software control.
- Software selection between all VGA and PAL/S-Video modes.
- PAL/S-Video conversion support for all VGA and Extended VGA modes with 600 or fewer lines.
- Built-in dot clock circuitry to eliminate crystal oscillators for VGA, plus extended VGA operation up to 135 Mhz.
- Low power consumption, ideal for laptop computers.



Internal Block Diagram



Theory of Operation

The **GSP600** can be thought of as an extremely sophisticated dot clock generator. In its simplest form, the **GSP600** will generate all of the dot clock frequencies necessary to drive VGA and Super VGA controllers. The different frequencies are selected with the **MODE SELECT LOGIC** from the VGA chip. Selection is similar to selecting frequencies on any of the ICS dot clock generators (i.e., ICS1394, ICS1494, ICS1561, ICS2494, etc.). Additionally, there are four reserved frequency addresses. These are labeled GL (genlock), OV (overlay), VO (video only), and GO (graphics only). Choosing any of these addresses will switch the **GSP600** from VGA mode to PAL mode. Under PAL mode, the **GSP600** accepts vertical and horizontal **VGA SYNC** from the VGA controller and uses the sync to generate and adjust the **VGA DOT CLOCK**. The **GSP600** will automatically vary the frequency of the dot clock in order to synchronize the VGA sync signals with a PAL reference signal. This reference signal can be derived from a video device (such as a camcorder) connected to **VIDEO INPUT 1** or **VIDEO INPUT 2**. The **GSP600** provides an RGB-to-PAL encoder with the **VIDEO OUTPUT** signal which is either **VIDEO INPUT 1**, **VIDEO INPUT 2**, or an internally generated black burst signal. All of the necessary **ENCODER LOGIC** signals to properly drive the encoder are provided by the **GSP600**. During PAL modes the **GSP600** also creates the **D-15 SYNC OUTPUT** for the monitor connection to allow for TV projection output of the VGA images. The **PIXEL SWITCH** information derived from external **CKEY INPUT** tells the encoder whether to display the VGA image or external video for each pixel. Assuming the images are genlocked, this creates the overlay effect.

Block definition

Video Input Switch

The Video Input Switch selects whether the **GSP600** uses VIDEO INPUT 1 or VIDEO INPUT 2 as the external video source. It is controlled by an external pin of the **GSP600**.

PAL Sync Separator

The **GSP600** contains a high quality sync separator to allow direct input of PAL, S-VHS, or HI-8 video signals from camcorders, VCRs, and other video products. The **GSP600** utilizes a differential video input circuitry for maximum noise immunity. It also employs digital noise filtering and enhanced digital signal tracking technology to ensure maximum compatibility with consumer, industrial, and broadcast video signals. Although low cost video sync separator products are commonly available, they are primarily designed for television and video monitor use. The simple diode clamping circuit used in these devices does not have the accuracy or noise immunity required for genlocking.

PAL Sync and Black Burst Generator

PAL Sync Generator

The studio quality built-in video sync generator allows the **GSP600** to operate without an external video input and still maintain broadcast video timing. This assures PAL compatibility at all times. When external video is present, the sync generator works in conjunction with the sync separator to isolate sync from noisy video signals.

Black Burst Generation

Most RGB-to-PAL encoders synchronize a crystal oscillator to the chroma burst signal of the external video signal. This provides the color reference portion of the video signal. If an external video signal is not available, the crystal oscillator will free run, creating screen artifacts such as 45 degree moving lines in constant color portions of the screen. To eliminate this problem, the **GSP600** generates a black burst video signal. Black burst video is an analog signal containing both sync and a correctly phased chroma burst signal. This ensures proper color reference generation at all times. The **GSP600** provides black burst output to the encoder when external video is either missing or not selected (non-genlock mode).

INT/EXT Video Switch

The Internal/External Video Switch determines whether the encoder uses external video or the black burst signal. If external video is chosen, the **GSP600** will simply pass the external video signal through to the encoder, unaffected. Black burst is used when external video is not present. The switch is controlled by the Video Signal Processing and Sync Correction circuitry.

Video Signal Processing and Correction

Video Signal Processing

The Video Signal Processing circuitry of the **GSP600** measures the incoming video signal for basic timing accuracy and signal noise. It contains intelligent circuitry to remove extraneous portions of the video signal that would normally be incorrectly categorized as sync. This is extremely important when using a VCR as a video input. If there is an interruption of the external video signal, this circuit will automatically switch inputs from the external video signal to the internal sync generator. When the external video signal resumes, the circuit will automatically switch back to the external video. The Video Signal Processing accepts the MODE SELECT LOGIC from the VGA chip. This logic chooses either VGA or PAL operation and selects whether genlock to external video is to be enabled.

Sync Correction

The Sync Correction circuitry looks for missing sync pulses, block sync, single field video, and phase shift errors caused by the head switching zone of a VCR. It assures proper genlock during all of these problems common in consumer video products.

Genlock Timing Control and Clock Regulation

The **GSP600** looks at the input sync from the VGA controller and determines how to alter the dot clock to create PAL timing. Both the frequency and the method can change with different VGA modes. The **GSP600** enables virtually any VGA controller capable of interlacing to create PAL timing. The **GSP600**'s unique architecture provides ultra-high efficiency and flexibility and allows the frequency of the dot clock to be controlled totally under BIOS or software control. Screen attributes such as horizontal width and position can be individually programmed for each mode while maintaining genlock integrity. This circuit will modify the timing of virtually any mode, with 600 or fewer lines, to meet PAL specifications. The **GSP600** genlock timing control and clock regulation design is awaiting patent approval.

Precision Dot Clock Generator

The **GSP600** uses the same state-of-the-art dot clock technology that has made ICS the premier supplier of VGA dot clock generators. ICS offers the highest accuracy and lowest jitter products available.

CKEY

The ckey (or color-key) circuitry creates the pixel switch for the encoder. This signal determines whether the VGA image or external video is displayed for each pixel. Ckey is modified by the **GSP600** to ensure that the pixel switch signal is delayed (to make up for delays in the RAMDAC) and that it has proper levels during sync and blanking. If the VGA and external signals are genlocked, this pixel switch will create an overlay effect.

PIN NUMBER	NAME	DESCRIPTION
1	VLE	VERTICAL LOCK ENABLE. HIGH for VGA controllers. LOW disables vertical lock feature, may be useful for Non-VGA Operation.
2	ODD/EVEN	ODD/EVEN FIELD IDENTIFICATION. HIGH indicates odd numbered field, LOW indicates even numbered field.
3	BP	BACK PORCH PULSE. Negative polarity TTL level signal used by some RGB-to-PAL encoders.
4	DATAIN	Data input for inserting SMPTE time code in video signal.
5	CB	COMPOSITE BLANKING OUTPUT. Indicates non-screen data portions of PAL signal.
6	CS	COMPOSITE SYNC. PAL composite sync output for RGB-to-PAL encoders. Gated off during VGA modes.
7	CKEY	COLOR KEY. Resultant input from the 8-bit compare of digital RGB (P0-P7) and a software selectable byte. This color key determines which pixels display VGA and which display external video in overlay mode. See Hardware Interface Manual for more details.
8	TEST	For ICS use only.
9	VSYNCOUT	VERTICAL SYNC OUTPUT. Vsync output for DB-15 connector.
10	DATAFRAME	TTL level framing signal active during lines 10-20. For use in time code applications.
11	OVENABLE	OVERLAY ENABLE. Fast pixel rate switch. HIGH displays PAL output, LOW display RGB output. Used for overlay encoders. See Application Notes for wiring details.
12	I/ES	INT./EXT. SYNC. Determines sync selection in OVENABLE signal. Tie LOW normally.
13	LOC/REM	LOCAL/REMOTE. A LOW output state signifies REMOTE status indicating that external video is present and a genlock mode has been selected. If external video goes away or a non-genlock mode is selected, LOCAL/REMOTE will go HIGH.
14	BRSTACT	For ICS use only.
15	$\overline{\text{FRTSTOUT}}$	For ICS use only.
16	HS	HORIZONTAL SYNC. For some RGB-to-PAL encoders. Gated off during VGA modes.
17	$\overline{\text{HRSTOUT}}$	For ICS use only.
18	HSYNCOUT	HORIZONTAL SYNC OUTPUT. Hsync output for DB-15 connector.
19	VSS	Digital ground. We strongly recommend the use of a multilayer board and a ground plane.
20	VDD	5 Volt digital power. We strongly recommend the use of a multilayer board and a power plane.
21	VDD	5 Volt digital power. We strongly recommend the use of a multilayer board and a power plane.
22	VSS	Digital ground. We strongly recommend the use of a multilayer board and a ground plane.
23	FS5	Frequency Select 5. Selects between multiple VGA Dot Clock frequencies, Genlock modes and PAL frequencies. See Dot Clock Generation and PAL Mode Selection sections for a more detailed description. Also see Application Notes for wiring diagrams and BIOS Interface Manual for details.

PIN NUMBER	NAME	DESCRIPTION
24	FS4	Frequency Select 4. Selects between VGA Dot Clock frequencies and PAL modes.
25	FS3	Frequency Select 3. Selects between VGA Dot Clock frequencies and PAL modes.
26	FS2	Frequency Select 2. Selection between VGA Dot Clock frequencies and PAL modes.
27	FS1	Frequency Select 1. Selects betweenVGA Dot Clock frequencies and PAL modes.
28	FS0	Frequency Select 0. Selects between VGA Dot Clock frequencies and PAL modes.
29	EXTSYNC	For ICS use only.
30	VCR1	HIGH permits using VCRs as an input.
31	CLAMPLEV	Clamping level adjustment for video input. See Application Notes for more details.
32	Y2	PAL video input number 2. Note: This is also the Y (luminance) input for S-Video systems.
33	Y1	PAL video input number 1. Note: This is also the Y (luminance) input for S-Video systems.
34	C2	C (Chrominance) input number 2 for S-Video systems.
35	C1	C (Chrominance) input number 1 for S-Video systems.
36	4.43SC	4.433618 MHz SUBCARRIER OUTPUT. Phase-locked to the chroma burst signal to allow encoders to maintain proper SCH phasing.
37	$\overline{\text{FRSTIN}}$	For ICS use only.
38	AVDD	5 Volt analog power. We strongly recommend the use of a multilayer board and a power plane.
39	GFF	Inverts field 1 and field 2 of VGA sync. Normally tied HIGH.
40	VCOLF	VCO LOOP FILTER CIRCUIT. External RC circuit used in VCO circuitry. See Application Notes for component values.
41	SYNCTHRS	Sync threshold adjustment for video input. See Application Notes.
42	VGAO/E	VGA ODD/EVEN FIELD IDENTIFICATION. HIGH indicates odd numbered field, LOW indicates even numbered field.
43	$\overline{\text{COUT}}$	C (Chrominance) OUTPUT. C output for S-Video systems.
44	$\overline{\text{RST}}$	Chip reset pulse. This to be tied high through a resistor. Do not tie to the computer reset line.
45	YOUT	Y (Luminance) OUTPUT. PAL video output when the PAL/SVID input is in the HIGH state. Y output for S-Video systems when the PAL/SVID input is in the LOW state.
46	$\overline{\text{HALIGNOUT}}$	For ICS use only, wire to pin 62.
47	SYSLF	SYSTEM CLOCK LOOP FILTER CIRCUIT. External RC circuit used in the chroma burst phase locking circuit. See Application Notes for component values.
48	XTALI	17.734475 MHz crystal circuit. See Application Notes for parts specifications and wiring diagrams.
49	XTALO	17.734475 MHz crystal circuit. See Application Notes for parts specifications and wiring diagrams.

PIN NUMBER	NAME	DESCRIPTION
50	AVSS	Analog ground. We strongly recommend the use of a multilayer board and a ground plane.
51	VID1/2	Input selector. High for Y1/C1, Low for Y2/C2.
52	VCOOUT	For ICS use only, do not wire.
53	FILTSEL	For ICS use only, wire to pin 57.
54	DOTCLOCK	Clock signal input for VGA chip.
55	$\overline{\text{VFF}}$	Inverts field 1 and field 2 of PAL sync. Normally tied HIGH.
56	$\overline{\text{VCR2}}$	LOW modifies sync characteristics to permit operation with VCR input.
57	VGA/PAL	Mode identification output signal. HIGH indicates a VGA mode, LOW indicates a PAL mode.
58	$\overline{\text{BG}}$	BURST GATE PULSE. Negative polarity TTL level signal used by RGB-to-PAL encoders.
59	LOC/REM IN	For ICS use only, wire to pin 13.
60	VGAHSYNC	VGA HORIZONTAL SYNC. HSYNC signal from VGA chip. See BIOS Interface Manual for programming details.
61	VGAVSYNC	VGA VERTICAL SYNC. VSYNC signal from VGA chip. See BIOS Interface Manual for programming details.
62	$\overline{\text{HALIGNIN}}$	For ICS use only, wire to pin 46.
63	PAL/SVID	PAL/S-VIDEO. Selects between PAL and S-Video output. HIGH= PAL; Low= S-Video.
64	VS	VERTICAL SYNC. PAL Vsync output for RGB-to-PAL encoders. Gated off during VGA modes.
65	4XSC	4 TIMES SUBCARRIER OUTPUT. 17.734475 MHz signal phase-locked to the chroma burst signal.
66	PCLK	PCLK from VGA chip.
67	DATAOUT	TTL level output. This reads data during lines 10-20 and outputs it as a digital signal. For use in time code applications.
68	SCH	SCH PULSE. Positive polarity TTL level signal to distinguish between fields 1 and 3 or 2 and 4. Not necessary for most encoders.

BIOS Programming Example

BIOS support is currently available from Tseng Labs, Oak Technology, Trident Microsystems, S3, and NCR. Other VGA manufacturers have support programs underway. If you use one of these VGA controllers that have completed BIOS support, you can ignore this section. The following information may be helpful to VGA manufacturers and software developers. These tables represent register settings one particular VGA controller. Others are listed in the BIOS Interface Manual. This particular controller does not interlace text modes and uses an 8 x 8 font for modes 0, 1, 2 , 3, and 7. The horizontal registers are adjusted to produce underscan for text modes and overscan for graphics modes.

Horizontal CRTC Registers

CRTC INDEX	CRTC REGISTER	Modes: 00, 01, 04, 05, 0D	Modes: 02, 03, 06, 07, 0E, 0F, 10	Modes: 11, 12, 13
00	HT	35	6B	66
01	HDE	27	4F	4F
02	SHB	2A	53	52
03	EHB	96	8B	87
04	SHR	30	5B	58
05	EHR	92	83	80

Vertical CRTC Registers

CRTC INDEX	CRTC REGISTER	200 Line Modes: (Non-Interlaced) 00, 01, 02, 03, 07, 04, 05, 06, 0D, 0E, 13	350 Line Modes: (Interlaced) 0F, 10	480 Line Modes: (Interlaced) 12, 13
06	VT	05	05	05
07	OVERFLOW	11	11	11
10	VRS	E0	D3	F4
11	VRE	84	87	88
12	VDE	C7	AE	EF
15	SVB	DC	CF	F0
16	EVB	F2	E5	06

Note: The MSB of the MSL register (INDEX 09) must be turned OFF in 200 line NTSC modes. When using an 8 x 8 font for text (modes 00, 01, 02, 03, 07) the 4 LSB of this register will change from F to 7.

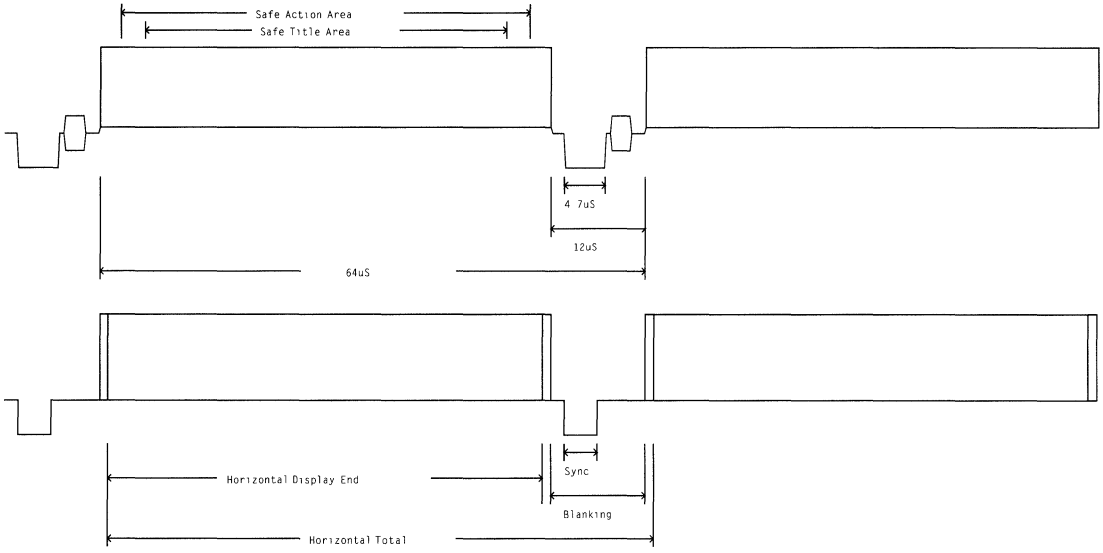
Miscellaneous Output Register

NTSC mode	Color Modes: 00, 01, 02, 03, 04, 05, 06, 0D, 0E, 10, 11, 12, 13	Monochrome Modes: 07, 0F
Genlock (GL)	23	22
Overlay (OV)	27	26
Video Only (VO)	2B	2A
Graphics Only (GO)	2F	2E

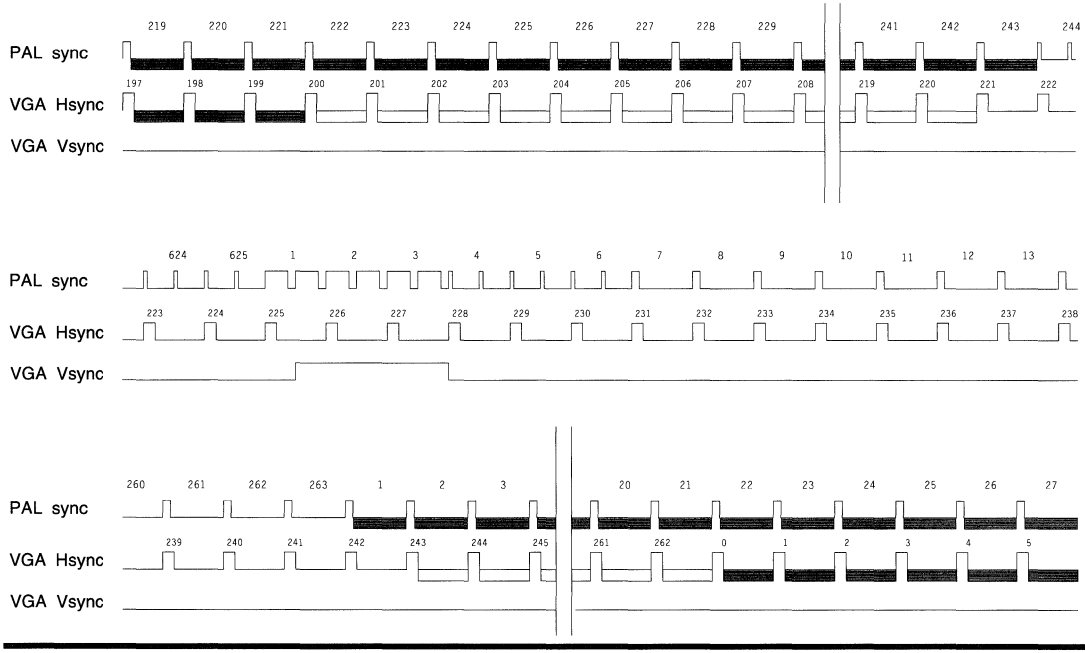
Extended Registers

Turn OFF all DOTCLOCK/2 bits.

PAL vs. VGA Horizontal Timing



PAL vs. VGA vertical timing (200 line mode)



Electrical Specifications

Operating temperature range 0 °C to 70 °C

Electrical Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
A_{VDD}	Analog Supply	4.5	5.0	5.5	Volts
D_{VDD}	Digital Supply	4.5	5.0	5.5	Volts
I_{DD} (VGA)	Operating Current - VGA Mode		35		mA
I_{DD} (PAL)	Operating Current - PAL Mode		50		mA

Input Signals

SIGNAL TITLE	PIN #	TYPICAL VALUE	OPERATING CONDITIONS
Y1	33	1 V_{P-P}	75 Ohm load
C1	35	1V_{P-P}	75 Ohm load
Y2	32	1V_{P-P}	75 Ohm load
C2	34	1V_{P-P}	75 Ohm load
VID1/2	51	TTL/CMOS	High = Y1,C1; Low = Y2,C2
PAL/SVID	63	TTL/CMOS	High = PAL; Low = S-Video
VGAVSYNC	61	TTL/CMOS	Positive polarity
VGAHSYNC	60	TTL/CMOS	Positive polarity
FS0-5	28-23	TTL/CMOS	Address/mode select
CKEY	7	TTL/CMOS	High = RGB; Low = PAL
PCLK	66	TTL/CMOS	Pixel (DAC) Clock from VGA
I/ES	12	TTL/CMOS	High = Internal sync Low = External sync
DATAIN	4	TTL/CMOS	Active during DATAFRAME
CLAMPLEV	31	1-1.5 V	
SYNCTHRS	41	CLAMPLEV + 0.1 V	
VLE	1	TTL/CMOS	Tie to V_{DD} through resistor
RST/	44	TTL/CMOS	Tie to V_{DD} through resistor

Output Signals

SIGNAL TITLE	PIN#	TYPICAL VALUE	OPERATING CONDITIONS
VSYNCOUT	9	TTL	Positive polarity during PAL modes
HSYNCOUT	18	TTL	Composite sync during PAL modes
VS	64	$1V_{P-P}$	Positive polarity
HS	16	$1V_{P-P}$	Positive polarity
CS	6	$1V_{P-P}$	Positive polarity
DOTCLOCK	54	TTL	
YOUT	45	$1V_{P-P}$	75 Ohm load
COUT	43	$1V_{P-P}$	75 Ohm load
4.43SC	36	TTL	4.433618 MHz
4XSC	65	TTL	17.734475 MHz
LOC/REM	13	TTL	High = local; Low = remote
OVENABLE	11	TTL	High = PAL; Low = RGB
VGA/PAL	57	TTL	High = VGA; Low = PAL
CB	25	TTL	Positive polarity
ODD/EVEN	2	TTL	High = odd field; Low = even field
VGAO/E	42	TTL	High = VGA odd field Low = VGA even field
BG/	58	TTL	Negative polarity
FP/	3	TTL	Negative polarity
SCH	68	TTL	Positive polarity
DATAFRAME	10	TTL	Lines 10-20
DATAOUT	67	TTL	Active during DATAFRAME

Dot Clock Selection

The following charts represent two of the many dot clock frequency selection tables supported by **GSP600**. See the BIOS manual or contact ICS applications engineering for additional information.

FREQUENCY (MHz)	FS5	FS4,FS3,FS2	FS1	FS0
50.350	0	1	0	0
56.644	0	1	0	1
65.028	0	1	1	0
72.000	0	1	1	1
75.000	1	0	0	0
80.000	1	0	0	1
89.800	1	0	1	0
110.000	1	0	1	1
Gen**L**ock	1	1	0	0
OV**e**rlay	1	1	0	1
Video **O**nly	1	1	1	0
Graphics **O**nly	1	1	1	1

FREQUENCY (MHz)	FS5,FS3	FS4, FS2	FS1	FS0
25.175	0	1	0	0
28.322	0	1	0	1
40.000	0	1	1	0
44.900	0	1	1	1
Gen**L**ock	1	1	0	0
OV**e**rlay	1	1	0	1
Video **O**nly	1	1	1	0
Graphics **O**nly	1	1	1	1

GSP600 Frequently Asked Technical Questions.

1. What will the GSP600 do for me?

The GSP600 adjusts the timing of a VGA controller to conform to PAL (television) specifications. The GSP600 accepts direct video input from video cameras, videodisc players or other video sources and will synchronize (genlock) a VGA controller to either the external video input or an internal PAL sync generator. The GSP600 also contains a dot clock generator to eliminate the need for crystal oscillators or other dot clock generators.

2. How does the GSP600 differ from other genlock devices?

Other genlock devices, such as the Motorola MC1378, are very effective at genlocking two PAL signals together and are generally used in consumer electronics products such as video window-in-a-window devices. The GSP600 is specifically designed to genlock a computer graphics controller to PAL video and overcomes all of the incompatibilities between VGA and PAL. Additionally, the GSP600 contains an PAL sync generator and maintains chrominance phase lock in local modes. This allows the GSP600 to maintain PAL timing without an external video input. Furthermore, the sync separator circuit of the GSP600 is designed to satisfy the low jitter tolerances demanded by discriminating VGA customers.

3. Isn't genlock simply a phased-lock loop?

Phase locking two similar signals is fairly straightforward as long as phase jitter is not critical. As an example, ICS is one of the few companies able to successfully build phase-locked loop dot clock generators with low enough phase jitter for computer graphics display. Additionally, the differences between VGA and PAL signals further complicate the genlock procedure. The GSP600 has patents applied for for the most advanced computer video genlock methods in the industry. These methods assure you of the highest possible quality product.

4. Most Genlock and Overlay products have a lot of discrete components with trimmer capacitors and potentiometers. All these adjustments can become very expensive in a mass production environment. How much external circuitry does the GSP600 require?

Although the GSP600 can be run with no trimmer capacitors or potentiometers, one trimmer capacitor should be used to meet the PAL frequency tolerance of the chroma burst. This is a free running frequency and is very simple (and fast) to adjust. Additionally, the GSP600 uses high speed digital circuitry to eliminate virtually all discrete components. Only a few external components are needed for full operation.

5. Do I need an RGB-to-PAL encoder with the GSP600?

Yes, an external RGB-to-PAL encoder is needed. The encoder must be matched to the target audience. The GSP600 can be used under broadcast television scrutiny and most broadcast video equipment perform the encoding entirely with discrete components. As this may prove too costly and/or may use too much board space, the GSP600 contains all of the necessary signals to drive virtually any encoder. The GSP600's generous supply of timing signals will also drive external circuitry to turn off the encoder for laptop applications.

6. Why do I need the GSP600. Can't I program a VGA controller for PAL sync and just drive an RGB-to-PAL encoder?

PAL sync contains equalizing pulses, blanking signals and pulse widths that are impossible to create under normal VGA control. Although marginal display quality is achievable on a television without adhering to the PAL standard, compatibility with other PAL equipment is compromised. As an example, depending on which edge of horizontal sync the monitor triggers on will determine how far an incorrect width horizontal sync pulse will skew the screen. Additionally, it becomes virtually impossible to assure proper chroma burst (SCH) phasing. The GSP600 sync generator meets or exceeds all PAL broadcast standards for timing accuracy assuring you of maximum compatibility and ultimate quality.

7. National sells a sync separator for less than $2 while the Brooktree part costs over $50. What is the difference and how does the sync separator in the GSP600 compare?

The sync separation circuitry in the National part is a simple diode clamp. Although this may be adequate for driving a picture tube, the lack of noise and jitter immunity make it unsuitable for genlock applications. Additionally, the analog vertical sync detection circuit of these type of devices will not accurately track a VCR signal. The Brooktree device represents a mixed-mode approach to sync separation. By utilizing a fast analog circuitry coupled with high speed digital logic, noise and jitter immunity can be optimized. The GSP600 also uses a mixed mode approach specifically optimized for genlock operation yet the incorporation of a sync generator allows signal analysis not possible with other devices.

8. Is the GSP600 compatible with any VGA controller?

VGA controllers need to have two features to work with the GSP600. First, they need to be able to interlace - if your controller can display 1024 x 768 resolution, then it can probably interlace (the additional 256K memory is not necessary). Second, the controller must have at least three clock select lines for external dot clock generator support. Virtually all current VGA controllers have this feature. Check with your VGA controller manufacturer or ICS if you are unsure.

9. How do I turn the PAL on and off and control it?

The GSP600 uses the three clock select lines to support 4 VGA clocks and 4 PAL modes. The VGA clocks are available in 7 different patterns (i.e. 25.175, 28.322, 40.000, 65.000 is one pattern). The 4 PAL modes are Genlock, Overlay, Graphics Only, and Video Only. The selection between any PAL mode or between PAL and VGA is done entirely under BIOS or software control.

10. Why did you incorporate a dot clock generator in the GSP600?

The GSP600 works by modifying the dot clock input for the VGA controller. It essentially is a dot clock generator designed for PAL genlock. The dot clock generator is not so much of an extra feature as it is a subset of the genlock design. Consequently, this unity design assures you of a reliable glitch-free solution.

11. When the GSP600 displays an Overlay, how do I determine which part of the screen displays graphics and which is VGA?

The GSP600 uses a technique called Color-Key to determine where to display the external video. This Color-Key color is based on the VGA color number. Therefore, no colors are actually lost. As an example, the background color is always Color 0. When Color-Keying on Color 0, the screen will appear to have a background of the external video. The actual color that the VGA assigns to Color 0 does not matter. Any of the 256 color numbers can be assigned to be a Color-Key. Although the GSP600 modifies the Color-Key input, the Color-Key selection is done by an external 8 bit digital compare.

12. Why is the Color-Key selection external to the GSP600?

Color-Key selection is done with an 8 bit compare of the digital RGB signals with a preassigned byte. The digital RGB data comes from the VGA controller and the preassigned byte normally comes from the IBM bus via a port selection. The output of this comparison is fed into the CKEY (Color-Key) input of the GSP600. Although this Color-Key method will satisfy 95% of all customers, the external design allows other schemes with multiple or different comparison options. Additionally, since all of these signals are already available inside the VGA controller, many manufacturers have announced plans to incorporate the Color-Key function inside the VGA controller.

13. What about NTSC and/or SECAM compatibility?

ICS has an NTSC version of the GSP600 (the GSP500). In its current implementation, it is pin compatible with the GSP600 but require different values for the discrete components and will also need a different crystal oscillator. Although a SECAM version is technically possible, due to the uncertain market potential product development is not currently underway.

14. Can I look forward to a combination PAL and NTSC product?

Unfortunately, the amount of circuitry common to both a PAL and an NTSC version is minimal. Separate versions are currently the lowest cost solution. Although the crystal frequency, some discrete components and the Bios would have to change, the same board layout could support both standards by simply changing the parts list.

15. Does the GSP600 accept multiple video inputs? What about an S-Video input?

The GSP600 has two independent video inputs. Either input can be used or they can both be disabled. Either input can be wired to accept either S-Video or PAL. Selection between the two inputs is performed under hardware control.

16. Why doesn't the GSP600 incorporate audio?

The PAL and S-Video baseband signals do not have a provision for audio. This means that the video and audio signals are completely separate signals at all times. ICS offers audio products for the multimedia market that can be incorporated into the design but allows the designer maximum flexibility by keeping them separate products.

17. Can I use the GSP600 with an RF modulator?

Yes, but the quality of the image may suffer. When PAL is modulated up to RF frequencies, audio is modulated onto a 4.5 MHz carrier and the video is limited to a maximum frequency of 4.2 MHz. Although 4.2 MHz may be sufficient for moving images it can be limiting for high resolution computer graphics. This problem is magnified because the majority of RF modulators are very low quality devices. Additionally, even if a high quality RF modulation is obtained, the signal may still be degraded by the RF demodulator inside the television set. ICS does recognize that these limitations may be outweighed by the user-friendliness and compatibility of the RF standard. High quality RF modulators are available and the GSP600 does have the necessary signals for support but these issues should be carefully weighed before implementation.

18. Can the GSP600 display PAL video on my VGA screen?

No, in order to display PAL video at 31.25 KHz, it is necessary to convert PAL into component form, digitize it in real time, and store at least one frame of video. Although technology exists to accomplish this, the price-to-performance ratio of these products is too high for mass market acceptance at this time.

19. Is there any question that I forgot to ask?

Yes, when I use a graphics program, I find the borders very distracting yet I need the borders in text modes to insure that I can read the DOS prompt. Can the GSP600 help me with this problem? The GSP600 has the ability to adjust the width of the screen totally under Bios control. This means that you can have limited overscan in mode 13, minor underscan in mode 3 and generous overscan in mode 12. Software drivers can even be written to dynamically change the screen width with the cursor keys.

20. Does this mean I can change the height of the screen also?

PAL has a fixed number of lines. In order to change the vertical size, the screen data must be compressed or expanded into fewer or greater lines. This can be accomplished in a text mode by changing the font size or in a graphics mode with linear interpolation. The GSP600 always maintains an exact one-to- one correlation between the PAL and VGA line position and therefore does not support vertical sizing.

21. Where do I get a development kit for the GSP600?

Call ICS at (800) 220-3366 for more information. We will put you in touch with a local rep. who will be more than happy to supply you with a full GSP600 development kit. The ICS full service support organization is always ready to help you with the latest in Multimedia solutions.

Sound Output Circuit

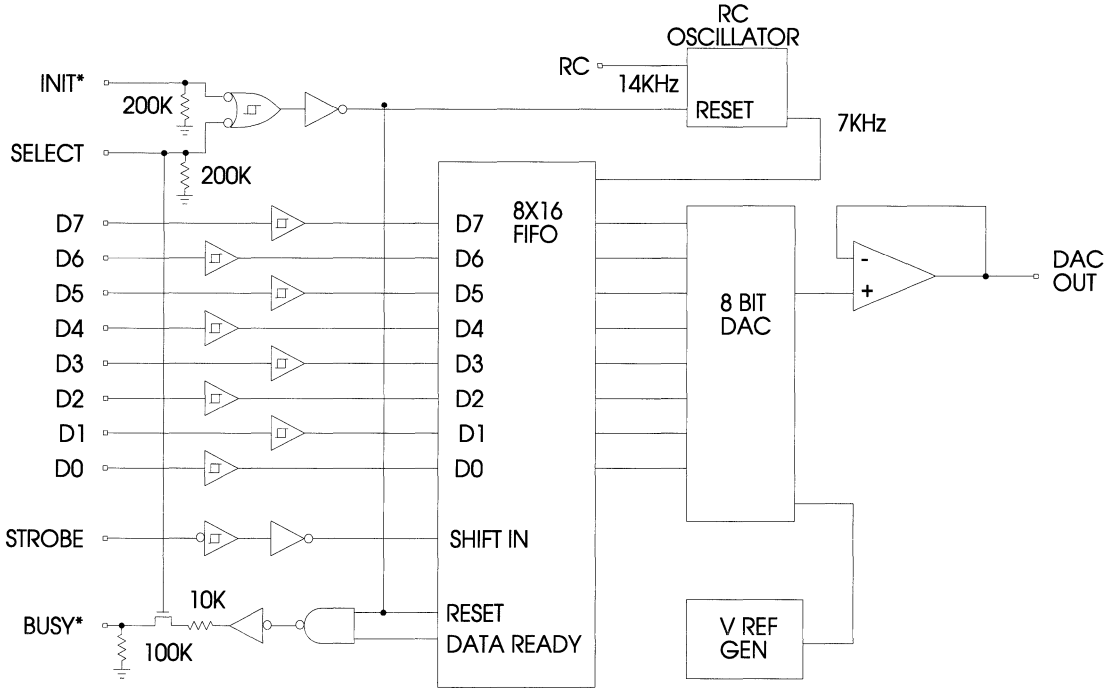
General Description

The **ICS2001** is a CMOS integrated circuit containing an 8-bit digital to analog converter fed by a 16-byte FIFO memory array. This device is intended to form the nucleus of a low-cost audio-output subsystem for personal computers, workstations, games, and talking books. The **ICS2001** is the core of the Disney Sound Source.™

Features

- 8-bit D/A converter
- 16-byte FIFO
- 5V and 9V operation
- TTL-level inputs with hysteresis
- RC clock oscillator
- Software drivers for DOS and Windows

Block Diagram

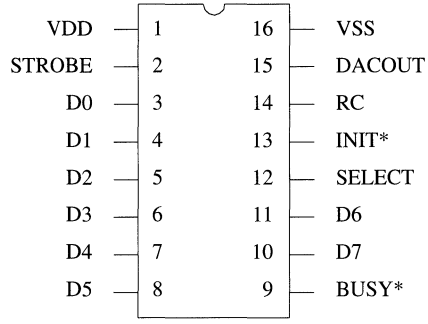


Ordering Information

ICS2001M (SO Package)
ICS2001N (DIP Package)

*Sound Source is a trademark of Walt Disney Computer Software Incorporated

Pin Configuration



Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VDD	Power	Positive power supply
2	STROBE	Input	Data strobe
3	D0	Input	Data input
4	D1	Input	Data input
5	D2	Input	Data input
6	D3	Input	Data input
7	D4	Input	Data input
8	D5	Input	Data input
9	BUSY*	Output	Busy (Active Low)
10	D7	Input	Data input
11	D6	Input	Data input
12	SELECT	Input	
13	INIT*	Input	Initialization (Active Low)
14	RC	Oscillator	One-pin oscillator
15	DACOUT	Output	Converter output
16	VSS	Power	Negative power supply/ground

Absolute Maximum Ratings

Storage temperature ..... -65 °C to 150 °C
Voltage on any pin with respect to ground..... -0.5V to V_{DD}+0.5V
Maximum V_{DD} 10.6V

Standard Test Conditions

Operating Temperature Range ..... 0 °C to 70 °C
Power Supply Voltage ..... 4.5 to 10.0V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

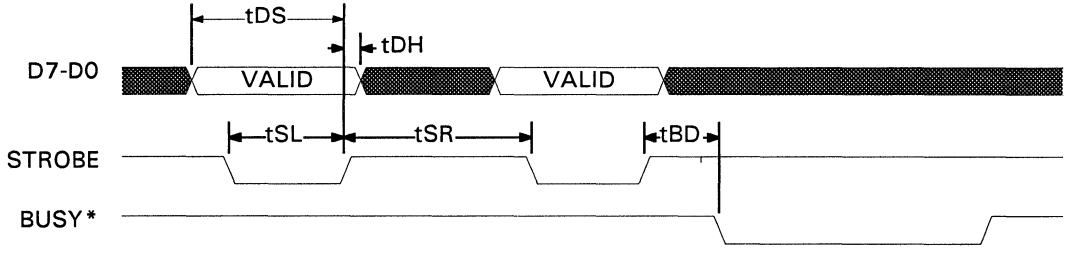
DC Characteristics

PARAMETER	SYMBOL	NOTES	MIN	TYP	MAX	UNITS
Logical 1 Input Voltage	V_{IH}		2.0		V_{DD}	V
Logical 0 Input Voltage	V_{IL}		0		0.8	V
Input Leakage Current	I_I	Any input	-1.0		1.0	uA
Input Hysteresis		Any input	20	50		mV
Pull down resistors		INIT*, SELECT	100	200	300	K ohm
Pull down resistor		BUSY*	50	100	200	K ohm
Supply Current	I_{DD}				5.0	mA
DAC output voltage	V_{DACOUT}	Data=$00 Data=$FF		V_{DD}/6 V_{DD}/2		V
DAC Differential Linearity			-1		+1	LSB
DAC Output Current	I_{DACOUT}	V_{DD}=4.5	200	500		uA
DAC Output Current	I_{DACOUT}	V_{DD}=9		1		mA
DAC Capacitive Load	C_L				20	pF
Output Current High	I_{OH}	V_{DD}=4.5V V_{OH}=2.0V	200	400		µA
Output Current Low	I_{OL}	V_{DD}=4.5V V_{OL}=.8V	200	400		µA

AC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Frequency	F_{OSC}	R=160K; C=1000pF	12.6	14.0	15.4	kHz
Data Setup	T_{DS}		0			ns
Data Hold	T_{DH}		100			ns
STROBE Width Low	T_{SL}		50			ns
STROBE Recovery High	T_{SR}		50			ns
BUSY* Delay	T_{BD}	C_L=50pF			750	ns

Timing Diagram



Function Description

The overall operational status of the **ICS2001** is controlled by the INIT* and SELECT inputs. If either INIT* or SELECT is low, the chip is held in the "reset" condition: The BUSY* output is asserted, the STROBE input is ignored, and DAC OUT is forced to VDD/6 (minimum value). When INIT* *and* SELECT become high, the device enters the "run" condition, and BUSY* goes high indicating the FIFO is "ready for data."

Binary data is fed to the **ICS2001** via the D0-D7 pins and latched into the FIFO buffer by the rising edge of STROBE. Input data flow is controlled by the BUSY* output. Data in the FIFO is shifted out to the D/A converter at a rate established by the RC oscillator, typically 7 kHz. A data value of $00 will generate nominal output of VDD/6 volts, while a value of $FF will result in an output of VDD/2 volts.

The following steps represent a typical sound-playback sequence: SELECT is asserted causing BUSY* to go high indicating buffer ready for data. Data applied to pins D0-D7 are latched into the FIFO on the rising edge of STROBE. Additional bytes of data may be strobed in as long as BUSY* remains high. Thus, BUSY* is used to control the flow of data into the FIFO. SELECT is de-asserted after the last data byte has been written and sufficient time allowed for it to be reproduced.

Note that the first data byte strobed in under a "ready," *i.e.* BUSY*=1, status will ripple through to the D/A converter and its analog value appears on DAC OUT asynchronously. Subsequent bytes will be output at the data rate established by the RC clock as long as there is data in the FIFO. Therefore, it is recommended that sound samples be padded with a $00 leading byte to avoid time distortion between the first and second sample. Similar glitches may occur in the middle of sound sequences if the FIFO is allowed to empty.

Also note, that if the device is enabled (INIT* *and* SELECT=1) while the STROBE input is high, the current value of the data bus will be shifted into the FIFO. Therefore, during initialization for operation with STROBE pulsing low (statically high), valid data (usually $00) should be placed on the data inputs before the reset condition is removed.

In a typical application, the **ICS2001** shares a standard personal computer (Centronics) printer port with the system printer, and is powered by the same 9V source that supplies the external low-pass filter and speaker driver that comprise the balance of the sound subsystem. In the interest of simplicity and minimal cost, this power source is usually a battery.

In order to minimize unwanted current flow through the inputs of the **ICS2001** when the battery is disconnected or dead, all chip inputs should be connected to the printer port via series resistors with a nominal value of 10K ohms, and the power connection to the VDD pin should include a blocking diode. The BUSY* output, which normally drives an external NPN transistor, is provided with an internal 100K pull-down resistor to keep the transistor turned off when the **ICS2001** is not powered up.

The oscillator frequency is set by an external resistor and capacitor. The design center values are 160K ohms (from the RC pin to VDD) and 1000pF (from the RC pin to VSS). This results in a nominal clock frequency of 14 kHz plus or minus 5 percent. This signal is internally divided by two to yield an output sampling frequency of 7 kHz.

Integrated Circuit Systems, Inc.

Wavedec™ Digital Audio Codec

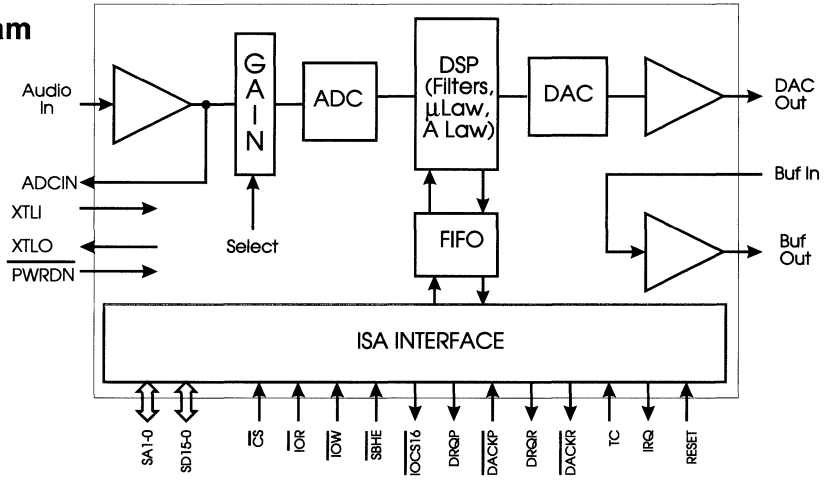
Features:

- Digital audio 8/16 bit record/playback
- Fully programmable sample rates including industry standards:
  - 44.1 kHz
  - 22.050 kHz
  - 11.025 kHz
  - 8.00 kHz
  - 5.513 kHz
- DAC output oversampled to simplify external filtering.
- Four data formats:
  - 16 bit linear
  - 8 bit linear
  - 8 bit u-law
  - 8 bit a-law
- 16 step analog output level control, -1.5dB/step
- 8 bit log scale digital volume control
- Oversampling ADC with input filter.
- Programmable IIR filters for input antialiasing and output reconstruction.
- ISA bus interface
- 8/16 bit DMA and I/O transfer modes
- Input/output FIFO buffer
- Power down mode
- 44 pin PLCC package

Description

The **ICS2002** is a mixed-signal integrated circuit providing a low-cost recording and playback solution for multimedia audio applications. These applications include document annotation, voice mail, interactive games, multimedia sound record/playback, and Windows™ sound production. The **ICS2002** supports the record and playback of 16-bit audio data, and provides a 8/16-bit parallel interface to the industry standard PC bus.

Block Diagram



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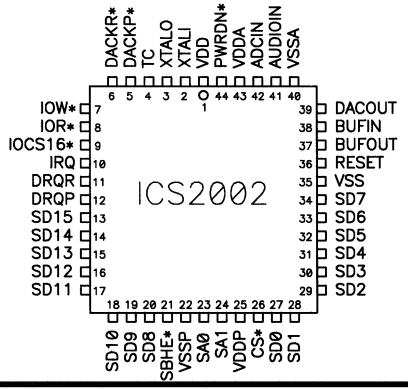
Pin Descriptions

PIN	TYPE	DESCRIPTION
SD15 - SD0	I/O	Data bus
SA1 - SA0	I	Address
CS*	I	Chip select (active low)
IOW*	I	Write strobe (active low)
IOR*	I	Read strobe (active low)
SBHE*	I	System High Byte Enable (active low)
IOCS16*	OC	Indicates that the access register can support 16 bit transfer.
DRQP	O	DMA Request (play channel)
DRQR	O	DMA Request (record channel)
DACKP*	I	DMA Acknowledge (play channel)
DACKR*	I	DMA Acknowledge (record channel)
TC	I	DMA terminal count
IRQ	O	Interrupt request (active high, open drain)
RESET	I	Reset (active high)
XTLI	I	Crystal oscillator
XTLO	O	Crystal oscillator
PWRDN*	I	Power down (active low)
AUDIOIN	AI	Audio buffer input
ADCIN	AO	Audio buffer output/input to ADC
DACOUT	AO	DAC audio output
BUFIN	AI	Uncommitted audio buffer input
BUFOUT	AO	Uncommited audio buffer output
VDD	P	Digital + 5V supply
VDDA	P	Analog + 5V supply
VDDP	P	Digital + 5V supply
VSS	P	Digital GND
VSSA	P	Analog GND
VSSP	P	Digital GND

Package Pinout

44 Pin PLCC



Ordering Information

ICS2002V

ICS devices in PLCC packages carry a "V" designation.

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to 7.0V
Logic Inputs..... -0.5V to V_{DD} + 0.5V
Ambient Operating Temperature..... 0° C to 70° C
Storage Temperature ..... -65° C to 150° C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

V_{DD} = 5.0V ± 10%; GND = 0V; T_A = 0° C to + 70° C

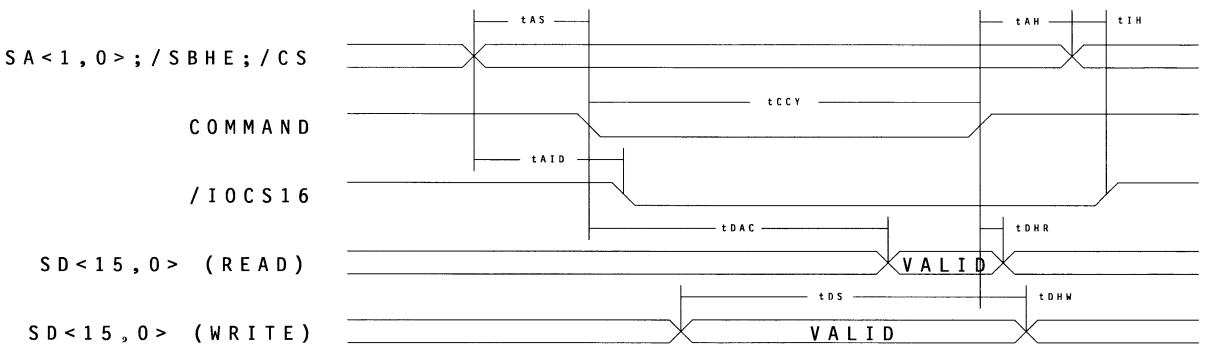
DC/STATIC					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Digital Inputs					
Input Low Voltage	V_{IL}	-0.3		0.8	V
Input High Voltage	V_{IH}	2.0		V_{DD} + 0.3	V
Input Leakage Current	I_{LI}			1	µA
Input Capacitance	C_{IN}			7	pF
Digital Outputs					
Output Low Voltage (I_{OL} = 4.0mA)	V_{OL}			0.4	V
Output High Voltage (I_{OH} = 0.4mA)	V_{OH}	2.4			V
Tri-State Current	I_{OZ}			10	µA
Output Capacitance				10	pF
Bi-directional Capacitance				10	pF
Analog Inputs					
Audio Input Voltage			0.7		Vrms
Audio Input Impedance		500K			ohm
Buffer Input Impedance		500K			ohm
Audio Outputs					
Audio Output Voltage			0.7		Vrms
DACOUT, BUFOUT Output Impedance				1K	ohm
Digital Supply Current	I_{CC1}			1	mA
Analog Supply Current	I_{DD2}			35	mA
Power Down Mode				1	mA
Play Only Mode				15	mA
Record Mode				30	mA

Electrical Characteristics

V_{DD} = 5.0V ± 10%; GND = 0V; T_A = 0°C to + 70°C

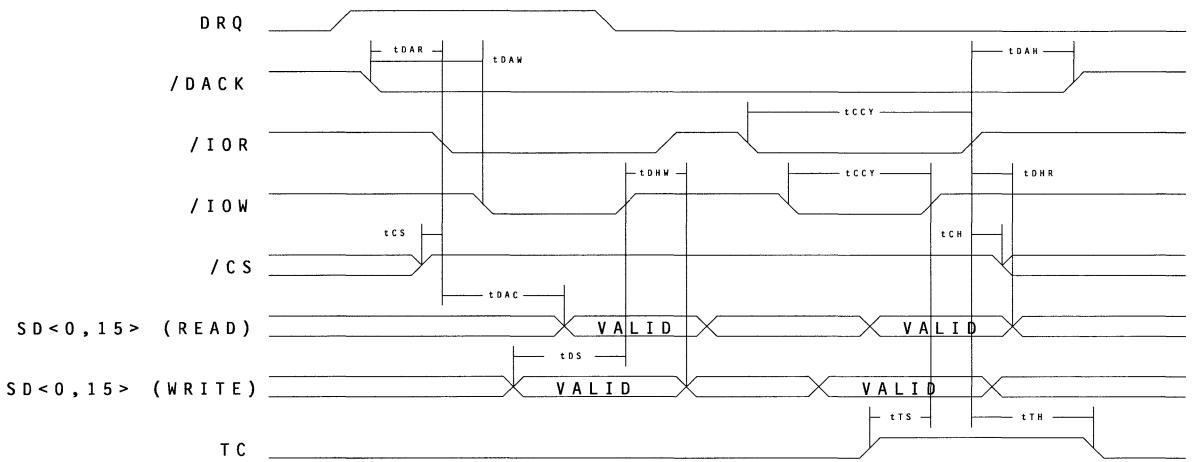
AC/DYNAMIC					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Address setup to command	t_{AS}	10			ns
Address hold from command	t_{AH}	10			ns
Command cycle time	t_{CCY}	100			ns
Address valid to /IOCS16 delay	t_{AID}			50	ns
IOCS16 hold from address invalid	t_{IH}	0			ns
Data valid to /IOW	t_{DS}	50			ns
/IOR active to valid data	t_{DAC}			60	ns
Data hold after /IOR	t_{DHR}	0			ns
Data hold after /IOW	t_{DHW}	10			ns
/DACK setup to /IOR	t_{DAR}	30			ns
/DACK setup to /IOW	t_{DAW}	50			ns
/DACK hold from command	t_{DAH}	50			ns
/CS setup to command	t_{CS}	10			ns
/CS hold from command	t_{CH}	10			ns
TC setup to command inactive	t_{TS}	25			ns
TC hold from command	t_{TH}	0			ns

Timing Diagrams



I/O Cycle Timing

Timing Diagrams



DMA Cycle Timing

Digital Audio Playback:

To play digital audio files, the chip is programmed for the desired sample rate, data type, DMA channel width, and output volume.

For DMA mode playback, DRQ generation is programmable for servicing the FIFO at several levels. This allows optimal performance with a variety of hosts. When TC is received, the chip will optionally generate an interrupt to the host to indicate the need to service the DMA controller.

For I/O Mode playback, data is written to the FIFO until it is full. This is determined by polling the "DIR" bit of the status register. Once the FIFO is full, an interrupt will be generated optionally at one of several selectable points: 1/4, 1/2, or 3/4 full. The host can then burst a predetermined amount of data to the FIFO and wait for the next interrupt.

Digital Audio Recording:
Audio recording operates in a DMA or I/O mode similarly to audio playback with the audio input programmable as a line or microphone level input. Simultaneous record and playback is supported and permits the recorded file to be synchronized to an existing file. The new and existing file can then be mixed digitally for high quality results.

Data Processing:
To simplify the external circuitry associated with the analog input and output signals of the chip, input and output sample rates are oversampled. This allows simple RC filters to be used.

For playback, the output data is oversampled, interpolated, filtered and scaled. Since the DSP is fully programmable, various sample rates and filter shapes can be implemented. The processed data is then output to the DAC. The DAC output passes through an analog volume control (4 bits, 1.5dB steps) before being passed to the analog filter stage.

For recording, the input data is first filtered, removing most of the frequency content above the Nyquist frequency. The resulting data stream is then undersampled to the desired sample rate and fed into the FIFO for transfer to the host.

Power Management:
The POWERDN* input can be programmed to act as an immediate hardware power control, or as an interrupt source for a software driven power management routine. The software driven option allows the driver to cleanly shut down to chip, thus preventing unwanted noise. When active, the power down function disables all analog components including the oscillator, and causes the chip to enter a low power mode.

Miscellaneous Functions:
The chip has a full complement of status and control functions. All significant functions are capable of generating interrupts and/or being polled.

The DMA can be run in single or demand mode (for bursts of data in programmed sizes).

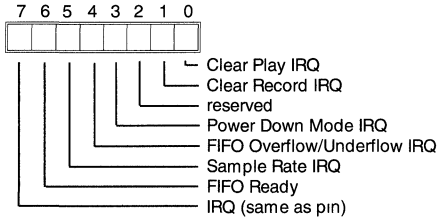
The FIFO has programmable interrupt and DMA request capacities, and also indicates when overflow or underflow conditions occur.

The processor interface is designed for simple connection to the ISA bus. For best noise performance, isolating the data lines from the ISA bus is recommended. In general, feed through of digital noise is reduced by minimizing the load which the digital outputs are driving.

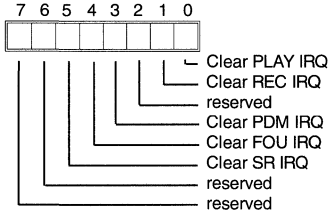
Direct Register Descriptions

The base address is determined externally by an address decoder which selects the chip via the CS* input.

Status (Base + 0 read)



IRQ Reset (Base + 0 write)



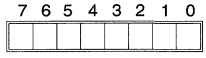
This register provides the driver software easy access to the interrupt source when read. Note that bit 7 indicates the state of the IRQ pin, and hence will be zero when the MIE bit is zero (see "Interrupt Enable" register).

A write to the register is performed to clear interrupts. Writing a one to a given bit will cause the associated interrupt to be cleared. To release the clear interrupt bit and allow further interrupts to occur, a zero must be written back to the bit of interest (some bits have alternate methods of clearing described later). This feature ensures that if the interrupt condition still exists, an edge will be generated on the IRQ pin, thus ensuring recognition on platforms that are edge sensitive. This also allows for a return from interrupt instruction to be executed on the platform while the IRQ line is inactive.

Bit 6 is a special case. There is no IRQ associated with this bit. It is located here for use in Sound Source Emulation Mode, and represents the BUSY status of a Sound Source. When the STATUS is read and tested with 40h, a zero result indicates that the play FIFO is full.

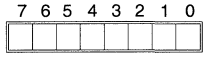
Note that this register can only be read in STAND ALONE mode. Hence, indirect access to this register has been provided at RA= 83h for use in COMPANION mode.

Register Address (RA) (Base + 1)



This register is the indirect pointer to direct data transfers to and from the data registers. It is a read/write register. Note that this register can only be read if the chip is in STAND ALONE mode.

Data Low Byte/Word (DLW)



Data High Byte (DH) (Base + 3)

These two addresses are used to accomplish all internal register reading and writing. Most internal registers are 8-bit or less. These are accessed by first writing the appropriate value to the DW, then writing (reading) the data byte to (from) DLW.

I/O Mode FIFO data (RA= 0Bh), Algorithm RAM, and Coefficient RAM are always treated as 16-bit entities, and can be transferred in two ways:

- a single operation to/from DLW with SBHE* = 0
- two successive operations, low byte to/from DLW with SBHE* = 1, then high byte to/from DH.

Indirect Register Map

Indirect Address	Register
4E	Companion Select Register (write only)
80	Chip Control
81	Interrupt Enables
82	reserved
83	Interrupt status
84	Sample Rate Low 8 bits
85	Sample Rate High 4 bits
86	Sample Rate Control/Status
87	reserved
88	Play DMA Control
89	Play DMA Burst Count
8A	Play DMA Mode
8B	DMA IO Mode Data Port
8C	FIFO Enable/Status
8D	FIFO IRQ Mode
8E	reserved
8F	reserved
90	Power Enable/Status
91	Power Mode
92	reserved
93	reserved
94	DSP Control/Status
95	DSP RAM Address Latch
96	Code RAM Data Port (8/16 bit)
97	Data RAM Data Port (8/16 bit)
98	Record DMA Control
99	Record DMA Burst Count
9A	Record DMA Mode
9B	reserved

Indirect Address	Register
9C	Record FIFO Enable/Status
9D	Record FIFO IRQ Mode
9E	reserved
9F	reserved
A0	Digital Master Volume
A1	DAC Deglitcher Control
A2	reserved
A3	reserved
A4	ADC Control
A5	Analog Volume/Mute
A6	ADC Timing Control
A7	reserved

Indirect Register Definitions

All writable bits/registers are also readable. In addition, there are some read only bits/registers, which are noted where appropriate.

Reserved bits should be written to zero, and read back zeroes. Reserved registers should not be written or read.

Except where noted, registers should be accessed as 8 bit registers via address BASE+ 2.

General Purpose Registers

IR4E Register Access Mode Select

This register must be written to 01h for any other indirect (or direct) accesses to occur, except for RA writes, which always occur based on chip select. This indirect address allows multiple companion chips to share resources in a system (such as bus buffers, address decodes, interrupts, and DMA channels).

This register is cleared only by hardware reset, and in unaffected by MCR (see below).

IR80 Chip Control

Bits 7:3 - reserved

Bit 2 - Sound Source Emulation Mode (SSMODE)
This bit sets the chip to operate in Sound Source Emulation mode. In Sound Source Emulation Mode, the two address pins (SA1, SA0) are mapped to match the PC parallel port as used by the Sound Source as follows:

Chip Address	Sound Source	IC2002
0	Data	DH
1	Status	Status
2	Control	DL
3	unused	RA

To use this mode, the chip must be configured before the Sound Source compatible application is run (I/O Mode DMA, DSP loaded and running, SR running, etc.) Then, the IC2002 is put in SSMODE and RA (now at address 3) is written to 8Bh. In the PC, the BIOS pointer to the parallel port is changed to the base address of the IC2002 chip, and the application can then be started.

This bit is reset by MCR. Hence, it must be set after MCR is set, on a second write to this register.

Bit 1 - Chip STAND ALONE Mode
This bit sets the chip to operate in STAND ALONE mode. In STAND ALONE mode, the STATUS and RA registers are accessible at BASE+ 0 and BASE+ 1. This mode should be used to speed register access when the IC2002 is being used by itself, without other ICS chips sharing resources (such as address decodes, interrupts, DMA channels, bus buffers, etc.).

When bit 1 is zero, the IC2002 will operate in COMPANION mode. In this mode, the STATUS register is mapped only to indirect address 83h. This is done to avoid conflict with other ICS chips that will provide STATUS and RA read back at the first two base addresses.

In addition, STAND ALONE mode configures the DRQP, DRQR, and IRQ pins to operate as outputs, with both one and zero levels being actively driven. When in COMPANION mode, these pins have a strong source for the high state and a weak sink for the low state to allow wire-and connections to other ICS chips.

This bit is reset by hardware reset only, not by MCR.

Bit 0 - Master Chip Reset (MCR)
0 - Hold chip in reset
1 - Remove reset
This bit is cleared to zero by a hardware reset. Thus, any functions reset by MCR are also reset by the RESET pin.

IR81 Interrupt Enables

Bit 7 - Master Interrupt Enable (MIE)
In the zero state, this bit prevents the IRQ pin from going active (high) regardless of the state of any of the individual interrupt sources. It is cleared to zero by MCR. A zero in this bit does not prevent an individual interrupt source from being active in the STATUS register. This allows interrupts to be masked while allowing their status to be polled.

Bit 6 - reserved

Bit 5 - Sample Rate Interrupt Enable (SRIE)

Bit 4 - FIFO Overflow/Underflow Interrupt Enable (FOUIE)

Bit 3 - Power-down Mode Change Interrupt Enable (PMCIE)

Bit 2 - reserved

Bit 1 - Record FIFO Interrupt Enable (RFIE)

Bit 0 - Play FIFO Interrupt Enable (PFIE)
Each of these bits individually enables, one, or disables, zero, their respective interrupt sources from being active in the STATUS register. In addition, there will be no IRQ generated if MIE is one when an individual enable bit is zero. The state of this bit does not affect the source of these interrupts in any way, and they may be polled for activity in the appropriate register for each interrupt type. These bits are all cleared to zero by MCR.

IR83 Status

This register is the same as the direct access status register, except that it can be read in COMPANION mode.

Sample Rate Generator Registers

IR84 Sample Rate Low 8 bits (SRL)

Bits 7:0 - Sample Rate Bits 7:0

IR85 Sample Rate High 4 bits (SRH)

Bits 3:0 - Sample Rate Bits 11:8
Together, these two registers define the record and playback sample rate. Based on the crystal frequency FXtal, and a 12 bit value SR (the concatenation of the two registers), the sample rate will be:

Sample Rate = FXtal * SR / 524288

These registers are not initialized by any of the reset mechanisms. Note that the Sample Rate Counter should always be stopped via SRCS bit 0 when these two registers are changed.

IR86 Sample Rate Control/Status (SRCS)

Bits 7:2 - reserved

Bit 1 - Sample Rate Interrupt (SRIRQ) - Read Only
This is set by the hardware whenever the sample rate counter overflows, indicating that a new sample is being input or generated. This bit is cleared by any of the following actions:

- Master Chip Reset
- Sample Rate Run = 0 (SRR bit 0)
- a write to STATUS with bit 5 = 1
- any write to SRCS

Bit 0 - Sample Rate Run (SRR)
This bit resets the Sample Rate Counter, the SRIRQ bit, and shuts down the sampling and playback processes when written to a zero. When written to a one, the sample rate generator runs at the programmed rate. SRR is internally synchronized to the master clock to provide clean starts and stops of the counter. MCR clears this bit.

Play DMA Control and Status Registers

IR88 Play DMA Control (DMACTL)

Bits 7 - reserved

Bit 6 - TC Reset Mask
When set to 1, this bit masks the 'DMA Run' bit reset upon receipt of TC, terminal count, signal from the ISA bus. When reset to 0, the 'DMA Run' bit will be reset upon receipt of TC.

Bits 5:1 - reserved

Bit 0 - DMA Run
This bit enables the DMA hardware to begin transferring data when set to one. It is cleared by either MCR or receipt of a TC when 'TC Reset Mask' is a zero (see the DMAMODE register for details).

IR89 Play DMA Burst Count (DMABC)

Bits 7:6 - reserved

Bits 5:0 - DMA Burst Count
This value determines the number of DMA transfers that take place for each DMA request issued to the host. The actual number of transfers will be DMABC+ 1. Thus, for single transfer mode, program this register to zero. The burst counter is automatically preset to the burst count whenever the DACKP* input is high. Thus, there is no need to reprogram the count value after TC, since the next transfer will use the full programmed count value. This register has no affect on I/O Mode data transfers, since its only influence is over the DRQP output. This register is not initialized by any means other than a direct write, and hence must be written to before DMA is enabled.

IR8A Play DMA Mode (DMAMODE)

All bits in this register are cleared by MCR.

Bits 7:6 - reserved

Bit 5 - Terminal Count Interrupt (TCIRQ) - (read only)
This bit indicates that a Terminal Count has been received on the last DMA operation. If the PFIE and PLAYIRQ bits have been programmed to a one, an interrupt will be generated at the end of the last DMA operation. This bit is cleared by MCR or a write to STATUS with bit 0 = one. The reset state is then removed by either writing the STATUS bit 0 to zero.

Bit 4 - I/O Mode Transfer (IOXFER)
When this bit is a one, the DMA hardware (DRQP and TCIRQ) is disabled. Data transfers take place via IR8Bh, and are required to be treated as 16 bit transfers. Thus, data should be written to DLW (with SBHE* = low, 16 bit data) or to DLW (with SBHE* = high, 8 bit data low byte) followed by DH (8 bit data, high byte). It is also the programmers responsibility to ensure that DMAMODE bit 2 (DMA16) is set to a one for all I/O mode transfers.

Bit 3 - Unsigned Data (USIGN)
When set to a one, this bit expects to receive (and will generate) unsigned data. The native data format is Signed Binary Twos Complement. This bit will invert the most significant bit of each data byte (or word, depending on the state of DATATYPE). Note that this bit should be zero when the DATATYPE indicates u-law or A- law data formats.

Bit 2 - 16 Bit Data (DMA16)
When set to a one, this bit causes the hardware to expect data to be sent in 16 bit words. When low, the hardware expects 8 bit bytes. This bit must be set to one when performing I/O mode transfers, as all I/O transfers are treated as 16 bit values.

Bit 1:0 - Data Type (DATATYPE)
These bits direct the hardware how to interpret the outgoing data. This is independent of the DMA or I/O data width. It effects how data is signed and how data is packed to and unpacked from the Play FIFO. The DATATYPE field selects the format of data for playback.

Value	Data Type
00	8 bit linear
01	16 bit linear
10	8 bit μ256 Law
11	8 bit A-Law

IR8B DMA I/O Mode Data Port (DMADATA) (8/16 bit)

This register address is used to trap I/O mode data to and from the FIFOs. It is only used in I/O mode. See the description of the IOXFER bits for more details.

When DMA16 is one, this register MUST be accessed as a sixteen bit value. Note that this can be done from either an eight or sixteen bit ISA slot, since the chip used SBHE* to determine the proper byte swapping.

FIFO Control/Status Registers

IR8C FIFO Enable/Status (FES)

Bit 0 - FIFO Enable (FE)
This bit holds the FIFO in a reset state when low, and enables the FIFO to operate when high. This bit is reset by MCR. This bit, when low, also resets all FIFO related conditions (see the following bits) and prevents DMA start requests from being issued. It does not reset the FIFO IRQ Mode register.

Bit 1 - FIFO Overflow (read only)
This bit is set when a FIFO shift in command is generated (by either DMA, I/O, or the DSP) with the FIFO full, and indicates an error condition. This bit will cause the FOUIRQ bit to go active, generating an IRQ if enabled. This bit is reset by writing to STATUS with bit 4 = 1, and re-enabled by writing to STATUS with bit 4 = 0. FE low also resets this bit.

Bit 2 - FIFO Underflow (read only)
This bit is set when a FIFO shift out command is generated (by either DMA, I/O, or the DSP) with the FIFO empty, and indicates an error condition. This bit will cause the FOUIRQ bit to go active, generating an IRQ if enabled. This bit is reset by writing to STATUS with bit 4 = 1, and re-enabled by writing to STATUS with bit 4 = 0. FE low also resets this bit.

Bit 3 - FIFO 25% Full (read only)
This bit goes high after 4 words (or 8 bytes) have been loaded into the FIFO, and low again when 13 words (or 26 bytes) may be loaded into the FIFO. There is no interrupt associated with this bit directly.

Bit 4 - FIFO 50% Full (read only)
This bit goes high after 8 words (or 16 bytes) have been loaded into the FIFO, and low again when 9 words (or 18 bytes) may be loaded into the FIFO. There is no interrupt associated with this bit directly.

Bit 5 - FIFO 75% Full (read only)
This bit goes high after 12 words (or 24 bytes) have been loaded into the FIFO, and low again when 5 words (or 10 bytes) may be loaded into the FIFO. There is no interrupt associated with this bit directly.

Bit 6 - FIFO DIR (read only)
This bit goes high when a single word (or two bytes) may be written to the FIFO. There is no interrupt associated with this bit directly. Note that this bit resets to a one because when the FIFO is reset it is forced to be empty, and hence is ready to accept data.

Bit 7 - FIFO DOR (read only)
This bit goes high when a single word (or two bytes) may be read from the FIFO. There is no interrupt associated with this bit directly.

IR8D FIFO IRQ Mode

This register must never be written to when the FIFO is enabled. Invalid interrupts and DMA requests could be generated as a result.

Bits 7:4 - reserved

Bit 3 - FIFO IRQ Enable (FIE)
This bit enables the various FIFO capacity thresholds to generate interrupts (as PLAYIRQ) when one. When zero, this bit prevents FIFO capacity IRQ generation when operating in DMA mode, which only needs TCIRQ.

Bits 2:0 - FIFO Ready IRQ Mode Selection
This field defines FIFO utilization for both DMA and I/O mode data transfers. In I/O mode, it is used to generate interrupts (FRDYIRQ) when the FIFO capacity reaches a predefined point. For DMA transfers, it signals the DMA logic to request a transfer at those same predefined points. By programming the DMA Burst Count appropriately, the FIFO may be easily kept near the desired capacity.

The following table describes the selections available:

Bits 2:0	IRQ/DRQ Source	Notes
000	DIR	Ready to take 1 word from HOST
001	EMPTY 75%	Ready to take 13 words from HOST
010	EMPTY 50%	Ready to take 9 words from HOST
011	EMPTY 25%	Ready to take 5 words from HOST
100	DOR	Ready to provide 1 word to DSP
101	FULL 25%	Ready to provide 4 words to DSP
110	FULL 50%	Ready to provide 8 words to DSP
111	FULL 75%	Ready to provide 12 words to DSP

Note that for byte transfers (DMA16= 0), the numbers listed above should be doubled.

This must be programmed before the FIFO is enabled. It may be changed while the FIFO is enabled, if necessary. This register is cleared by MCR, but not by FE low.

IR8E reserved

IR8F Play FIFO Output Data Read Back (8/16 bit)

This register is provided for test use only, although it may find system level use as a diagnostic tool.

Power Control and Status

IR90 Power Enable/Status (PEST)

Bit 7 - PWRIRQ (read only)
This bit is a one when either edge has occurred on the PWRDN* pin, and the edge enable in the Power Mode register is set. If bit 3 of the MIE is one, this will also generate an external interrupt. In any case, this bit is also visible as STATUS register bit 3. PWRIRQ is reset by disabling both edge enable bits or resetting the edge interrupts (see below).

Bits 6:5 - reserved

Bit 4 - ADCPWR Disable
This bit controls the power state of the ADC analog circuitry. When 0, ADC analog power is controlled by the SOFTPWR bit the same as the DAC analog power is. When this bit is set to a 1, the ADC analog power is turned off independent of the state of SOFTPWR.

This feature is included for advanced power management routines, as chip power dissipation can be reduced by almost half by turning ADC power off when not in use. Note, however, that several milliseconds of settling time is required after power is turned on before the ADC functions properly.

Bit 3 - PWRDN* Pin Value (read only)
This bit indicates the state of the PWRDN* pin.

Bit 2 - FALLIRQ (read only)
This bit is set when the PWRDN* pin makes a transition from high to low. If PWRMODE bit 2 (FALLIE) is one, this will cause PWRIRQ to go high as well. This bit is reset by one of the following:

- MCR
- any write to PEST
- a write to STATUS with bit 3 set to one. This will hold the bit reset until released by a write to STATUS with bit 3 cleared to zero.

Note that FALLIE does not mask this bit, allowing polling to be performed.

Bit 1 - RISEIRQ (read only)
This bit is set when the PWRDN* pin makes a transition from low to high. If PWRMODE bit 1 (RISEIE) is one, this will cause PWRIRQ to go high as well. This bit is reset by one of the following:

- MCR
- any write to PEST
- a write to STATUS with bit 3 set to one. This will hold the bit reset until released by a write to STATUS with bit 3 cleared to zero.

Note that RISEIE does not mask this bit, allowing polling to be performed.

Bit 0 - Soft Power (SOFTPWR)
The function of this bit depends on the status of the "SWMODE" bit (bit 0 of PWRMODE). When SWMODE is zero, writes to this bit have no affect. Reads will return the state of the PWRDN* pin, which is also the state of the on chip PWRON control signal. When SWMODE is a one, a write of one to this bit turns on power to the chip analog circuitry, while a zero clears this bit and puts the chip in a low power mode. Reads will return the last value written.

IR91 Power Mode (PWRMODE)

All bits in this register are cleared by MCR.

Bits 7:3 - reserved

Bit 2 - Fall IRQ Enable (FALLIE)
When set to one, this bit allows a falling edge on PWRDN* to cause PWRIRQ to go high. It does not mask PEST bit 2.

Bit 1 - Rise IRQ Enable (RISEIE)
When set to one, this bit allows a rising edge on PWRDN* to cause PWRIRQ to go high. It does not mask PEST bit 1.

Bit 0 - Software Mode (SWMODE)
When cleared to zero, this bit causes the chip to operate in a "hardware driven" mode; that is, the PWRDN* pin directly controls the chip analog power (for low power consumption). In this mode, a low on PWRDN* puts the chip in low power mode, while a high enables normal operation. When set to a one, this bit causes the chip to operate in a "software driven" mode. In this mode, changes on the PWRDN* pin only generate interrupts. The hardware low power mode is then controlled (via software) by SOFTPWR (bit 0 of PEST). This function allows "clean" software controlled turn on and off of the analog circuitry power.

IR92 reserved

IR93 reserved

IR94 DSP Control/Status (DSPCS)

Bits 7:4 - Index Counter Value (Read Only)
This value indicates the current contents of the DSP address Index Counter, and is provided as a code debug aid for use in Step Mode. In normal operation it should be ignored. It is reset to zero when the DSP is not running, and increments by one at the completion of each "pass" of the DSP engine.

Bit 3 - DSP Sequence Complete (Read only)
This bit is set each time the DSP completes its sequence and restarts. It is reset to zero when the DSPRUN bit is zero or after a read of this register.

Bit 2 - DSP Output Saturation Detect
This bit is set to one whenever the DSP output value written to any output destination (DATA RAM, DAC, or Record FIFO) exceeds a sixteen bit signed range. In these cases, the DSP output saturates to $7FFF or $8000 (for positive or negative values) rather than overflowing. It is reset to zero when the DSPRUN bit is zero or after a read of this register.

Bit 1 - DSP Step Mode
This bit is intended as a DSP code debug aid only. When set to a one, this bit halts the DSP microcode sequencer at the end of each "pass" of code. This enables the host to read the DATA RAM contents to check the results of the previous calculations. Note that writes to the Record FIFO and DAC will be captured by the DATA RAM "under" them to aid with debug efforts. For normal operation, this bit **MUST** be set to a zero.

Bit 0 - DSP Run
When written to one, this bit starts the DSP engine running. A zero stops and resets the DSP engine execution. This bit is reset by MCR.

Before running the DSP, the Code and Data RAMs must be loaded. To do this, perform the following:

1) write 95h (DSPRA) to the desired address
2) write 96h (Code Ram data) or 97h (Data RAM data) to the desired 16 bit value.
3) repeat 1 and 2 for all RAM locations of both RAMs.
4) when done, write any data to DSPRA to reset the load logic.

ICS will provide algorithm and constants data supporting filtering functions for various sample rates.

Note that when the DSP is running, it is forbidden to read or write either the Code or Data RAMs (except when halted in STEP mode, see above). Also, after writing to the Code or Data RAMs to load them, and before starting the DSP, you must reset the RAM load hardware by writing to the DSPRA register (the value written is ignored).

IR95 DSP RAM Address Latch (DSPRA) (write only)

Bit 7 - Read
When one, this bit indicates that the next DSP RAM operation is a read. Zero indicates a write operation.

Bits 5:0 - DSP RAM Address
These bits are the address for the next DSP RAM data transfer. Note that the Code RAM address can be $00 through $3f, and the Data RAM address can be $00 through $1F.

IR96 Code RAM Data Port (8/16 bit)

Bits B:0 - Code RAM Data
This 8/16 bit port is data to be read from/written to the DSP Code RAM. The data is the low 12 bits of the word.

IR97 Data RAM Data Port (8/16 bit)

Bits F:0 - Data RAM Data
This 8/16 bit port is the data to be read from/written to the DSP Data RAM. The data is a full 16 bit word.

Record DMA Control and Status Registers

IR98 Record DMA Control (DMACTL)

Bits 7 - reserved

Bit 6 - TC Reset Mask
When set to 1, this bit masks the 'DMA Run' bit reset upon receipt of TC, terminal count, signal from the ISA bus. When reset to 0, the 'DMA Run' bit will be reset upon receipt of TC.

Bits 5:1 - reserved

Bit 0 - DMA Run
This bit enables the DMA hardware to begin transferring data when set to one. It is cleared by either MCR or receipt of a TC when 'TC Reset Mask' is a zero (see the DMAMODE register for details).

IR99 Record DMA Burst Count (RDMABC)

Bits 7:6 - reserved

Bits 5:0 - Record DMA Burst Count
This value determines the number of DMA transfers that take place for each DMA request issued to the host. The actual number of transfers will be RDMABC + 1. Thus, for single transfer mode, program this register to zero. The burst counter is automatically preset to the burst count whenever the DACKR* input is high. Thus, there is no need to reprogram the count value after TC, since the next transfer will use the full programmed count value. This register has no affect on I/O Mode data transfers, since its only influence is over the DRQR output. This register is not initialized by any means other than a direct write, and hence must be written to before DMA is enabled.

IR9A Record DMA Mode (RDMAMODE)

All bits in this register are cleared by MCR.

Bits 7:6 - reserved

Bit 5 - Terminal Count Interrupt (RTCIRQ) (read only)
This bit indicates that a Terminal Count has been received on the last DMA operation. If the RECIE bit has been programmed to a one, an interrupt will be generated at the end of the last DMA operation. This bit is cleared by MCR or a write to STATUS with bit 1 = 1. The reset state is then removed by either writing the STATUS bit 0 to 0, or by the next DMA operation. Hence, there is no need to "remove" this reset as there is for other IRQ reset operations.

Bit 4 - Record I/O Mode Transfer (RIOXFER)
When this bit is a one, the DMA hardware (DRQR and RTCIRQ) is disabled. Data transfers take place via RA $8B (NOT $9B), and are required to be treated as 16 bit transfers. Thus, data should be read from DLW (with SBHE* = 0, 16 bit data) or from DLW (with SBHE* = 1, 8 bit data low byte) followed by DH (8 bit data, high byte). It is also the programmers responsibility to ensure that RDMAMODE bit 1 (RDMA16) is set to a one for all I/O mode transfers.

Bit 3 - Unsigned Data (RUSIGN)
When set to a one, the record FIFO will generate unsigned data. The native data format is Signed Binary Twos Complement. This bit will invert the most significant bit of each data byte (or word, depending on the state of RDATATYPE).

Bit 2 - 16 Bit DMA (RDMA16)
When set to a one, this bit causes the hardware to expect data to be sent in 16 bit words. When low, the hardware expects 8 bit bytes. This bit must be set to one when performing I/O mode transfers, as all I/O transfers are treated as 16 bit entities.

Bits 1:0 - Record Data Type (RDATATYPE)
These bits direct the hardware how to interpret the incoming data. Note that this is independent of the DMA or I/O data width. It effects how data is "signed" and how data is packed to/unpacked from the Record FIFO.

Value	Data Type
00	8 bit linear
01	16 bit linear
10	reserved
11	reserved

IR9B reserved

Record FIFO Control/Status Registers

IR9C Record FIFO Enable/Status (RFES)

Bit 0 - Record FIFO Enable (RFE)
This bit holds the record FIFO in a reset state when low, and enables the FIFO to operate when high. This bit is reset by MCR. This bit, when low, also resets all FIFO related conditions (see the following bits) and prevents DMA start requests from being issued. It does not reset the Record FIFO IRQ Mode register.

Bit 1 - FIFO Overflow (read only)
This bit is set when a FIFO shift in command is generated (by either DMA, I/O, or the DSP) with the FIFO full, and indicates an error condition. This bit will cause the FOUIRQ bit to go active, generating an IRQ if enabled. This bit is reset by writing to STATUS with bit 4 = 1, and re-enabled by writing to STATUS with bit 4 = 0. FE low also resets this bit.

Bit 2 - FIFO Underflow (read only)
This bit is set when a FIFO shift out command is generated (by either DMA, I/O, or the DSP) with the FIFO empty, and indicates an error condition. This bit will cause the FOUIRQ bit to go active, generating an IRQ if enabled. This bit is reset by writing to STATUS with bit 4 = 1, and re-enabled by writing to STATUS with bit 4 = 0. FE low also resets this bit.

Bit 3 - FIFO 25% Full (read only)
This bit goes high after 4 words (or 8 bytes) have been loaded into the FIFO, and low again when 5 words (or 10 bytes) may be loaded into the FIFO. There is no interrupt associated with this bit directly.

Bit 4 - FIFO 50% Full (read only)
This bit goes high after 8 words (or 16 bytes) have been loaded into the FIFO, and low again when 9 words (or 18 bytes) may be loaded into the FIFO. There is no interrupt associated with this bit directly.

Bit 5 - FIFO 75% Full (read only)
This bit goes high after 12 words (or 24 bytes) have been loaded into the FIFO, and low again when 13 words (or 26 bytes) may be loaded into the FIFO. There is no interrupt associated with this bit directly.

Bit 6 - FIFO DIR (read only)
This bit goes high when a single word (or two bytes) may be written to the FIFO. There is no interrupt associated with this bit directly. Note that this bit resets to a one because when the FIFO is reset it is forced to be "empty", and hence is ready to accept data.

Bit 7 - FIFO DOR (read only)
This bit goes high when a single word (or two bytes) may be read from the FIFO. There is no interrupt associated with this bit directly.

IR9D Record FIFO IRQ Mode

Bits 7:4 - reserved

Bit 3 - FIFO IRQ Enable (RFIE)
This bit enables the various FIFO capacity thresholds to generate interrupts (as RECIRQ) when one. When zero, this bit prevents FIFO capacity IRQ generation when operating in DMA mode, which only needs RTCIRQ.

Bits 2:0 - FIFO Ready IRQ Mode Selection
This register defines FIFO utilization for both DMA and I/O mode data transfers. In I/O mode, it is used to generate interrupts (RECIRQ) when the FIFO capacity reaches a predefined point. For DMA transfers, it signals the DMA logic to request a transfer at those same predefined points. By programming the Record DMA Burst Count appropriately, the FIFO may be easily kept near the desired capacity.

The following table describes the selections available:

Bits 2:0	Source	Notes
000	DIR	Ready to take 1 word from DSP
001	EMPTY 75%	Ready to take 13 words from DSP
010	EMPTY 50%	Ready to take 9 words from DSP
011	EMPTY 25%	Ready to take 5 words from DSP
100	DOR	Ready to provide 1 word to HOST
101	FULL 25%	Ready to provide 4 words to HOST
110	FULL 50%	Ready to provide 8 words to HOST
111	FULL 75%	Ready to provide 12 words

Note that for byte transfers (RDMA16= 0), the numbers listed above should be doubled.

This must be programmed before the FIFO is enabled. It may be changed while the FIFO is enabled if necessary. This register is cleared by MCR, but not by RFE low.

IR9E reserved

IR9F reserved

Miscellaneous Registers

IRA0 Digital Master Volume

Bits 7:0 - Volume
This value is used to scale all values that are output from the DSP to the DAC. It may be written while the DSP is running.

The value written is interpreted as to give a log scale output response of 0.1875dB per step. The value for nominal (0dB attenuation) is E0h. A value of FFh gives 5.8125dB of gain. Note that any value above E0h may result in digital saturation of the internal 16 bit data value.

IRA1 DAC Deglitcher Control

Bits 7:3 - Volume bits 7:3 (read only)

Bit 2 - DAC Enable Bit (read only, for test)

Bits 1:0 - DAC Deglitch Width

Code	Notes
00	Deglitcher disabled
01	Minimum deglitch width
10	Nominal deglitch width
11	Maximum deglitch width

This value is determined by the clock rate at which the chip is run. ICS will provide the proper value for an application. This register is also used for test purposes.

This register is not initialized in any way and should be programmed before muting is removed.

IRA2 reserved

IRA3 reserved

ADC and Analog Control Registers

IRA4 ADC Control

Bits 7:3 - reserved

Bit 2 - ADC Test Mode
This bit is for factory testing use only, and must always be programmed to zero by an application. It is reset to zero by a zero in ADCRUN, and hence takes two writes of $05 to this register to activate for safety.

Bit 1 - reserved

Bit 0 - ADC Run
When written to a one, this bit enables the ADC hardware to run. Note that the ADC Timing Control register should be programmed appropriately first. Also note that the DSP must be running (and programmed properly) for the conversion results to be retrieved. The Sample Rate Generator determines the rate at which the conversion data is loaded into the Record FIFO.

This bit is cleared to zero by MCR.

Note that this bit, when 0, shuts down the successive approximation logic, the dynamic comparators and various logic functions. When the ADC is not being used, disabling it via this bit reduces background noise in the playback section and power consumption, and thus is recommended.

IRA5 Analog Volume/Mute

Bits 7:5 - reserved

Bits 4:1 - Analog Volume
These bits set the analog output level, in 1.5dB steps. All bits one gives 0dB attenuation of the DAC output signal, and all bits zero gives full attenuation. These bits are unaffected by any reset mechanism.

Bit 0 - Audio Enable
This bit disconnects the audio output of the output buffer amp and sets the BUFOUT pin to the nominal bias voltage when cleared to zero. When set to one, it passes the output of the output buffer amp to the BUFOUT pin.

The main function of this bit is to prevent sudden DC offset changes on the BUFOUT pin when entering and leaving power-down mode. By proper software procedure, noiseless transitions can be made.

This bit is cleared to zero by MCR.

IRA6 ADC Timing Control

This register is used to control the ADC internal operation timing.

Bits 7:4 - Comparator Timing Control
These bits control the time of comparator input switching. Bits 7:5 are the count, and bit 4 is 0 for half cycle and 1 full cycle delays.

Bits 3:1 - Cycle Timing Control
These bits control the number of clocks used for each step of the successive approximation process. For the full 64 step DSP cycle, the value of these bits should be 7. For a 40 step cycle, the value should be 4.

Bit 0 - reserved

IRA7 reserved

SMPTE Time Code Receiver/Generator

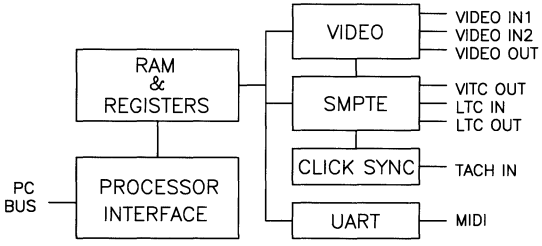
General Description

The **ICS2008**, SMPTE Time Code Receiver/Generator chip, is a VLSI device designed in a low power CMOS process. This device provides the timing coordination for Multimedia sight and sound events. Although it is aimed at a PC Multimedia environment, the **ICS2008** is easily integrated into products requiring SMPTE time code generation and/or reception in LTC (Longitudinal Time Code) and/or VITC (Vertical Interval Time Code) formats and MTC (MIDI Time Code) translation.

Taking its input from composite video, S-Video, or an audio track, the **ICS2008** can read SMPTE time code in VITC and LTC formats. Time code output formats are LTC and VITC. All are available simultaneously. A UART is provided for the user to support MTC or tape transport control.

The processor interface is compatible with the IBM PC and ISA bus compatible computers and is easily interfaced to other processors.

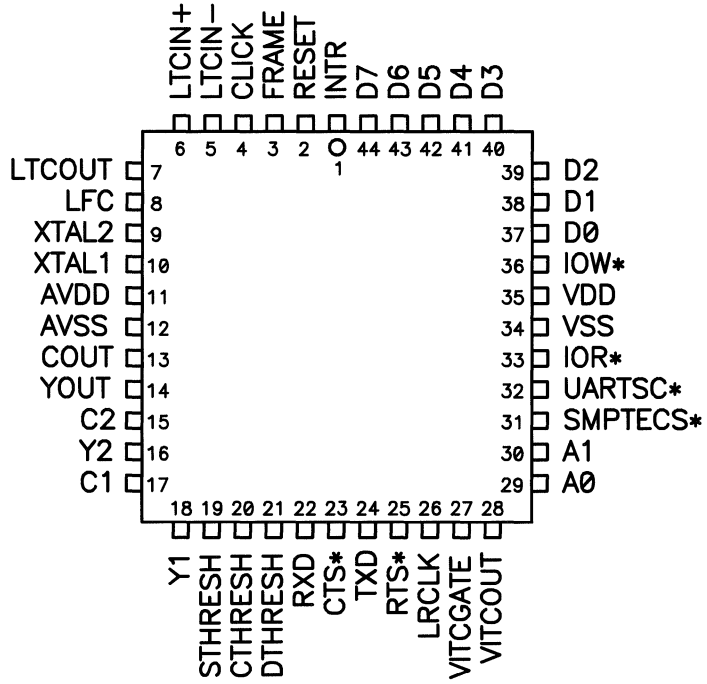
Block Diagram



Features

- Internal and external sync sources
  - Genlock to video or house sync inputs
  - internally generated timing from oscillator input
  - external click input
- LTC and VITC Generators
  - Real Time SMPTE Rates
    - 30 Hz (B&W, some audio)
    - 29.97 Hz (NTSC)
    - 25 Hz (PAL)
    - 24 Hz (film)
  - Time Code Modes
    - Drop Frame
    - Color Frame
  - VITC can be inserted on two lines from 10-40 (SMPTE specifies lines 10-20)
  - Update all data (time code, user data, and flag bits) on a frame-by-frame basis. This allows for "Jam Sync," "freewheeling," error bypass/correction, plus-one-frame, and other intelligent generator functions.
- LTC Receiver
  - Meets SMPTE and EBU LTC specifications including drop frame, color frame, time data, user data and status bits.
  - Synchronize bit rates from $1/30^{th}$ nominal to 80X nominal playback speed.
- VITC reader
  - Reads code from any or all selected scan lines.
  - Meets SMPTE VITC specifications including drop frame, color frame, time data, user data and status bits
- Time Code Burn-in Window selectable to overlay video with programmable screen position

Package Pinout



Ordering Information:

All ICS devices in PLCC packages carry a "V" designation.

Example: ICS2008V

Pin Description

PIN	TYPE	DESCRIPTION
Y1, Y2	AI	Video inputs from camera or other NTSC source. NOTE: This is also the Y (Luma) input for S-VHS and HI-8 systems.
C1, C	AI	C (Chroma) inputs for S-VHS and HI-8 systems. In NTSC systems, this pin should be tied to its respective Y input.
DTHRESH	AI	Data Threshold bypass input.
STHRESH	AI	SYNC Threshold bypass input.
CTHRESH	AI	Clamp Threshold bypass input.
YOUT	AO	NTSC video output. This is also the Y (Luma) output in S-Video mode.
COUT	AO	C (Chroma) output for S-VHS and HI-8 systems.
FRAME	AI	Color Frame A/B input. This input is self biased. (See Applications section.)
CLICK	AI	LTC SYNC input. This input is self biased. (See Applications section.)
LTCIN+	AI	SMPTE LTC input+ . This input is self biased. (See Applications section.)
LTCIN-	AI	SMPTE LTC input-. This input is self biased. (See Applications section.)
LTCOUT	AO	SMPTE LTC output.
LRCLK	O	SMPTE LTC receive clock output.
VITC	O	SMPTE VITC output to video mixer circuit.
VITCGATE	O	VITC gate indicates VITC code is being output for video overlay.
TxD	O	UART Transmit Data.
RxD	I	UART Receive Data.
CTS*	I	Clear to Send.
RTS*	O	Ready to Send.
XTAL1	I	14.318 MHz crystal input. This pin may be driven directly from a TTL 14.318 MHz source.
XTAL2	O	14.318 MHz crystal scillator output.
LFC	AI	External RC circuit.
A1-A0	I	Address bus
IOR*	I	Read Enable (active low)
IOW*	I	Write Enable (active low)
SMPTEC*	I	SMPTE port chip select (active low)
UARTCS*	I	UART chip select (active low)
RESET	I	Master reset (active high)
D7-D0	I/O	Bi-directional data bus
INTR	O	Interrupt Request (active high)
AVDD	P	Analog V_{DD}
AGND	P	Analog Ground
VDD	P	Digital V_{DD}
GND	P	Digital Ground

A - Analog I - Input
P - Power O - Output

Functional Description

The following is a functional description of the hardware registers in the **ICS2008** chip. It also describes how those registers can be utilized by the software to facilitate specific application services.

Hardware Environments

The **ICS2008** operates as a peripheral to a processor such as a PC or a single chip microprocessor. Many of the real time requirements are satisfied by double buffering both incoming and outgoing time codes.

LTC Input

LTCIN is a differential analog input feeding a comparator with hysteresis. It requires capacitive coupling to the LTC source. The output of the comparator goes to the LTC receiver, which is capable of receiving LTC in a forward or backward direction at a rate from $1/30^{th}$ to 80x nominal frame rates. The incoming LTC data is sampled with a phase-locked clock and loaded into the receive buffer following the receipt of a valid LTC SYNC pattern. When a complete frame has been received, an interrupt is generated.

LTC Output

The LTC output can be analog or digital. When set up as an analog output, it can drive a high impedance load.

The LTC generator outputs a LTC frame at the selected frame rate, such as 24Hz, 25Hz, 29.97Hz or 30Hz, and starts the frame based on a start time generated by the selected LTC SYNC source.

Video Inputs

There are two sets of video inputs. In a composite NTSC or PAL system, the Y input is the only one used. It is capacitively coupled to the source. In S-Video systems, capacitively couple Y and C to their respective sources. Proper termination of the source should be observed. One of the two video sources is selected by the VIDSEL bit in the SMPTE control registers as the video SYNC source. Internal timers are synchronized with the incoming video to extract timing information used to receive and generate VITC.

The VITC receiver samples the incoming video looking for a valid VITC code on selected scan lines. When a valid code is received it is written to a VITC receive buffer. More than one line can contain VITC code, and the codes can be different. For this reason, VITC codes from selected lines of a frame are written to separate VITC buffers.

Video Output

The video output combines the selected video input with the outputs from the VITC generator and the character generator. It can be a composite or an S-Video output as selected by the SVID bit in the SMPTE control registers.

VITC code is generated from data in the VITC generator buffer and output during the selected line time(s). The CRC and synchronizing bits are automatically generated by the VITC generator, but all of the data fields are sent directly from the buffer with no modification.

A character generator is provided to insert the time code in a burn-in window which overlays the incoming video. The vertical and horizontal position of the burn-in window is programmable.

MIDI Port

A UART is provided for a MIDI port. It can function as a MIDI IN and a MIDI OUT. It can generate an interrupt on receiver full and/or transmitter empty to the processor via the INTR pin. CTS and RTS modem controls are provided so that it can be used as a generic serial control port.

SMPTE SYNC Sources

A time code generator must have a SYNC input from a stable source in order to position the LTC code properly on a audio track of video tape or film. Three SYNC sources, video, click input, and free running, are available. In the case of a video tape, LTC code must start within plus or minus one line of the beginning of line 5. This requires "Genlocking" to the incoming video. The video timing section locks to the video's horizontal and vertical SYNC signal and generates a SMPTE SYNC. If some external SYNC source is available it can be input on the CLICK input. Otherwise, a free running SMPTE SYNC is generated from the oscillator at the selected frame rate.

Video Timing Generator

The video timing generator is "Genlocked" to the video input's SYNC separator. It extracts NTSC or PAL timing information from the video input and generates line and pixel rate timing for the VITC receiver, VITC generator, LTC generator and character generator. If no video input is present, it generates free running timing.

Overlay Character Generator

It is sometimes desireable to display the time code on a video display along with the picture. A character generator is provided for that purpose. The time code display, or burn-in window, can be positioned anywhere on the screen.

INTR Output

The INTR output pin is the interrupt source from **ICS2008** to the processor. Each interrupt source has its own interrupt enable and interrupt status.

Processor Interface

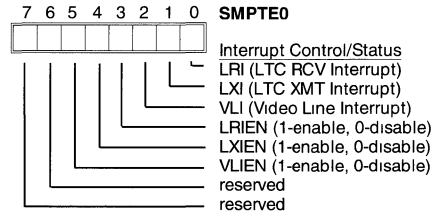
The **ICS2008** supports standard microprocessor interfaces and busses, such as the PC bus, to allow access of six control/status and data registers. These six registers are organized into two groups, one set of four for SMPTE control and the other set of two for direct UART port control. Each set of registers is selected with its own chip select, SMPTECS* and UARTCS*.

SMPTE Registers

The SMPTE register set allows access to 59 available registers. The first two are direct access registers addressed at locations 0 and 1. The remaining 64 registers are accessed by writing an indirect register address into location 2 and reading from or writing to location 3. If the AUTOINC bit in SMPTE2 is set to 1, the indirect register address is automatically incremented after an access to location 3. This eases the task of reading or writing sequential indirect locations.

SMPTECS*	A1	A0	REGISTER
0	0	0	SMPTE0 Interrupt Control/Status
0	0	1	SMPTE1 SMPTE Status
0	1	0	SMPTE2 Indirect Register Address
0	1	1	SMPTE3 Indirect Register Data

The SMPTE0 Register contains the SMPTE interrupt controls and status and the VITC read status. The three interrupt bits, LRI, LXI, VLI and TMI reflect the status of the potential interrupt sources to the processor. When a bit is set to one and the corresponding enable bit, LRIEN, LXIEN or VLIEN, is also set, the INTR output will be activated. Interrupts are cleared by reading SMPTE0. Bits 6 and 7 indicate a VITC read error. Further clarification of the error can be accomplished by reading the VITC Read Line registers, IR30 and IR31.

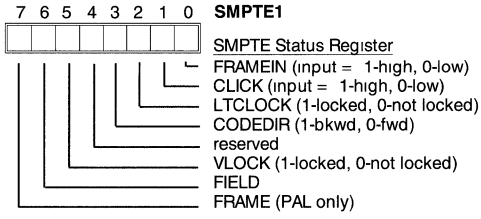


LRI - This bit indicates that a LTC receive interrupt has occurred. In order for an actual processor interrupt to occur, the LRIEN bit must also be set. An LRI interrupt occurs upon reception of the last byte of LTC receive data which was preceded by a valid LTC SYNC pattern. That is after the 64th LTC receive bit time in the forward direction. At normal frame rates, if the LTC transmitter is synchronized with the LTC receiver, there is about 3 milliseconds after this interrupt before the LTC transmit data for the next output frame is transferred to the output buffer.

LXI - This bit indicates that a LTC transmit interrupt has occurred. When this bit is set, and the corresponding LXIEN bit has been set, the INTR output will be activated. The LTC transmit interrupt is activated after the transfer of LTC transmit data to the output buffer. This occurs after LTXEN is set to one and after the 72nd LTC transmits bit time of the current frame, "N." Data loaded after this interrupt will appear in output frame "N+ 2" since the transmitter is double buffered.

VLI - This is a status bit that indicates that the video line selected via the Video Interrupt Line Register, VR9, has passed. When the VLIEN bit is also set, the processor will be interrupted. This interrupt can be used by the processor to determine when to sample the VITC time code when time locked to a video source. It will also be used to facilitate detection of LTC time code dropout and off speed LTC code, e.g. shuttling operations.

The SMPTE Status Register is a read only register which contains video and LTC status.



FRAMEIN - This bit indicates the state of the FRAME input pin. It is used as an alternate source for B/A frame status. This is useful when the quality of the video signal is not good enough to extract the B/A frame status.

CLICK - This bit indicates the state of the CLICK input pin. It can be used as a synchronization source for the LTC transmitter.

LTCLOCK - When a valid forward or backward LTC sync pattern is detected, this bit is set to one. It is reset to zero when an expected LTC sync pattern is missed or an invalid LTC bit is detected.

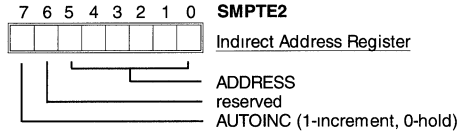
CODEDIR - The code direction bit works in conjunction with the LTCLOCK bit. When the LTCLOCK bit is set to one, the CODEDIR bit is valid. Otherwise, it is not. See the table below.

LTCLOCK	CODEDIR	LTC RECEIVER STATUS
0	X	Looking for SYNC pattern
1	0	receiving LTC (FORWARD)
1	1	receiving LTC (BACKWARD)

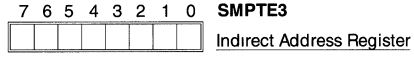
VLOCK - This is a hardware driven bit which indicates that genlock has been achieved with the selected video SYNC source.

FRAME & FIELD - The hardware SYNC separator detects the field and frame from the selected video input. The even/odd fields are identified by a 1/0 in bit 6. Bit 7, FRAME, is valid for PAL video after line 6. Bit 6, FIELD, is valid after line 5 in NTSC mode or line 2 in PAL mode.

The SMPTE2 register is the register which points to the 57 indirect registers. When reading or writing an indirect register, the value in the ADDRESS pointer, SMPTE2 bits 5 to 0, is the address of the register accessed through SMPTE3. If the AUTOINC bit is set to one, at the end of an access cycle to SMPTE3, ADDRESS will automatically increment. Otherwise, ADDRESS holds its value.



SMPTE3 is the data register through which all of the indirect registers are accessed. The address for a given register must first be set in SMPTE2 before accessing that register.



Indirect Registers

The following describes the functions controlled by the indirect registers. A map of the indirect registers follows this section.

LTC Read Registers **IR0-IR7** (read-only)
These read only registers contain the LTC data as received. Both forward and backward frames are stored with LTC bit 0 in the LSB of IR0 and LTC bit 63 in the MSB of IR7.

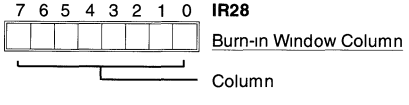
LTC Write Registers **IR8-IRf**
These registers contain the data to be sent by the LTC transmitter. The LSB of IR8 is sent as LTC bit 0, and the MSB of IRf is sent as LTC bit 63. The data is transmitted as it is stored in IR8-IRf.

VITC Read 1 Registers **IR10-IR17** (read-only)
These read only registers contain the VITC data as received from the video line selected in IR30. The frame is stored with VITC bit 2 in the LSB of IR10 and VITC bit 80 in the MSB of IR17. Note that a binary 10 sync pattern precedes every eight data bits of the VITC frame. The 10 sync pattern is not stored. The CRC is checked by the VITC receiver, and the result is reported in IR30.

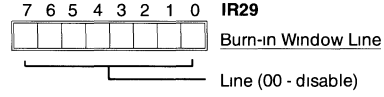
VITC Read 2 Registers **IR18-IR1f** (read-only)
As with the VITC Read 1 registers, these read only registers contain the VITC data as received from the video line selected in IR31. The frame is stored with VITC bit 2 in the LSB of IR18 and VITC bit 80 in the MSB of IR1f. The result of the CRC check is reported in IR31.

VITC Write Registers **IR20-IR27**
These registers contain the data to be output by the VITC generator. The VITC frame is output with the LSB if IR20 in VITC bit 2 and the MSB of IR27 in VITC bit 80. Note that the binary 10 sync pattern which precedes every eight data bits of the VITC frame is automatically generated by the VITC generator. The CRC is also automatically generated by the VITC generator.

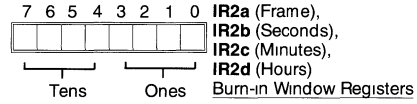
The next two registers control the position of the SMPTE video display, burn-in, window within the video raster. The window size is about one third the width of the screen and 32 lines high. IR28 selects the video column in which the burn-in window starts.



IR29 selects the video line which starts the SMPTE video display window in the video output. When this register is set to 0, there will be no Burn-In Window displayed in the video output.

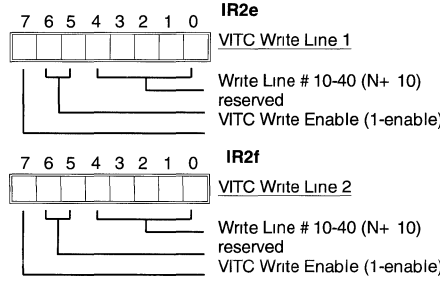


These registers contain the character codes used for the SMPTE time code in the burn-in window which overlays the source in the video output. An internal character generator converts the BCD nibbles to display characters.



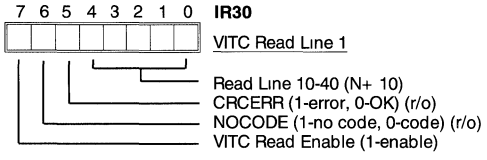
CODE	CHARACTER	CODE	CHARACTER
0	0	8	8
1	1	9	9
2	2	A	Do Not Use
3	3	B	?
4	4	C	_
5	5	D	□
6	6	E	■
7	7	F	Blank

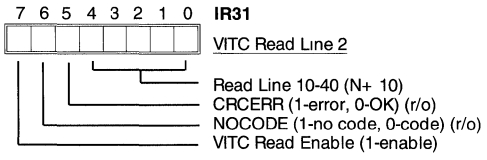
VITC code is normally output on two separate video lines in each field for redundancy. These two registers allow the individual line selection and output enables for the two VITC lines.



Write Line - Selects the video line on which the VITC code will be output. The video line on which the code is output will be the number in this register plus 10; e.g. writing a 1 to this register will cause the code to be output on line 11.

VITC Write Enable - Enables the output of VITC code on the specified line.



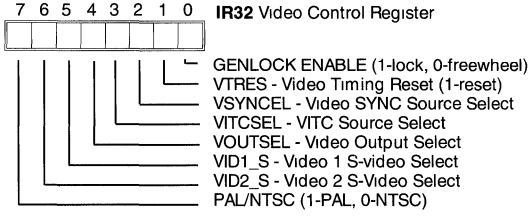


As with the VITC Write Line Register, these registers allow control of the individual redundant VITC read lines. The processor can also reprogram these dynamically to allow for scanning of VITC code when the source lines are unknown.

Read Line - Selects the line from which VITC code is to be read within each field. It works identically to the Write Line in that the video line selected is the number in this register plus 10.

CRCERR - This bit is reset to zero when a valid VITC code has been received. It is valid from the end of the selected video line until the end of the selected line in the next field.

NOCODE - This bit is set when a framing error occurs in the VITC code, i.e. not all the bits of the code were received by the time the end of the video line occurred. Both CRCOK and NOCODE must be zero to qualify a VITC code.



GENLOCK ENABLE - When set, this bit enables the genlock circuits to sync to the selected video input signal. When reset to 0, the video sync will "freewheel," generating video timing from the internal oscillator. The freewheel mode would be selected when striping LTC to allow synchronization with a MIDI sequencer or other strictly timed audio source.

VTRES - When set, this bit clears the video timing counters to dot zero of line 1 of field 1. This is useful when the video is free running, not genlocked and LTC sync needs to be synchronized to an event such as the CLICK input.

VSYNCSEL - When set to 1, this bit selects the video input source from Video 2 (Y2) to be the SYNC source for the internal video timing. Otherwise, when reset to 0, Video 1 (Y1) is selected.

VITCSEL - When set to 1, this bit selects the video input source from Video 2 (Y2) to be the VITC time code source for the VITC receiver. Otherwise, when reset to 0, Video 1 (Y1) is selected.

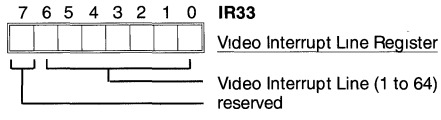
VOUTSEL - When set to 1, this bit selects the video input source from Video 2 (Y2, C2) to be output on the video outputs (YOUT, COUT). When reset to 0 Video 1 (Y1, C1) are selected.

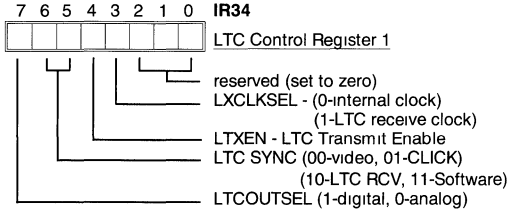
VID1_S - When set to 1, this bit causes the Video 1 source to be treated as S-Video. Otherwise, when cleared to 0, the Video 1 source is treated as composite video.

VID2_S - When set to 1, this bit causes the video 2 source to be treated as S-Video. Otherwise, when cleared to 0, the Video 2 source is treated as composite video.

PAL/NTSC - When set to 1, this bit causes the video to be synchronized with PAL timing. Otherwise, when cleared to 0, video is synchronized with NTSC timing.

Video Interrupt Line - This register selects the video line after which the Video Line Interrupt will occur. The actual video line number is the number in the register plus one.

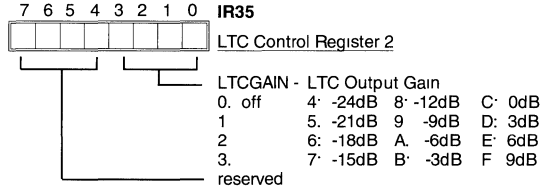




LXCLKSEL - This bit controls the source for the LTC transmit clock divider input. A 0 selects the internal 14.318MHz clock and a 1 selects the LTC receive clock. When the LTC receive clock is selected as the source to the LTC transmit clock divider, the clock rate is first doubled before being input to the divider so that loading a divider value of 001 will result in the LTC transmit clock running at the exact same rate as the LTC receive clock.

LTXEN - This bit, when set to 1, enables output of LTC code on the LTCOUT output pin. LTXEN is synchronized with the selected LTC SYNC source to ensure that only complete LTC frames are transmitted. The data to be sent by the LTC transmitter should be loaded into the associated RAM buffer before the LTCEN bit is set.

LTC SYNC - These bits select the LTC transmit sync source. Values 00, 01, 10 and 11 select start of video line 5, rising edge of CLICK, LTC receive sync pattern detect and write to IR3f respectively as the sync event. Care should be taken to disable LTXEN before changing the LTC SYNC select. Otherwise, an erroneous sync may be generated.

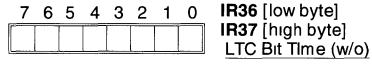


LTCOUTSEL - This bit, when set to 1, causes the LTCOUT pin to be a digital output. When cleared to 0, the LTCOUT pin is an analog output with gain control.

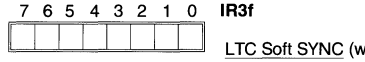
LTCGAIN - This bit sets the signal gain on the LTC audio output. The output gain is selectable in 3dB increments from -24dB to + 9dB referenced to 0VU = -10dbV. When this register is set to 0, there is no LTC audio output.

These next two write only registers control the LTC transmit bit rate. The transmit clock generator is a 12-bit divider. The upper four bits of IR37 are not used. Each bit requires two clocks. Therefore, the LTC transmit bit rate is the input clock divided by the divider value + 1, then divided by two. Since there are 80 bit times for each LTC frame, the LTC frame rate is the bit rate divided by 80.

LTC Tx Clock = Clock/(Divider Value + 1)
LTC Bit Rate = LTC Tx Clock/2
LTC Frame Rate = LTC Bit Rate/80



IR3f is not a register at all. It is simply an address which, when written and the LTC SYNC select is set for Soft SYNC, generates LTC SYNC for the LTC transmitter.



Indirect Register Map

		7	6	5	4	3	2	1	0
LTC	00	BINARY GROUP 1				FRAME UNITS			
Read	01	BINARY GROUP 2				COLR FRAME	DROP FRAME	FRAMES TENS	
	02	BINARY GROUP 3				SECONDS UNITS			
	03	BINARY GROUP 4				PHASE CORR	SECONDS TENS		
	04	BINARY GROUP 5				MINUTES UNITS			
	05	BINARY GROUP 6				BG FLAG 55	MINUTES TENS		
	06	BINARY GROUP 7				HOURS UNITS			
	07	BINARY GROUP 8				BG FLAG 75	UNASSIGNED	HOURS TENS	
LTC	08								
Write	...	SAME BIT DEFINITION AS LTC READ BUFFER							
	OF								
VITC	10	BINARY GROUP 1				FRAME UNITS			
READ1	11	BINARY GROUP 2				COLR FRAME	DROP FRAME	FRAMES TENS	
	12	BINARY GROUP 3				SECONDS UNITS			
	13	BINARY GROUP 4				FIELD MARK	SECONDS TENS		
	14	BINARY GROUP 5				MINUTES UNITS			
	15	BINARY GROUP 6				BG FLAG 55	MINUTES TENS		
	16	BINARY GROUP 7				HOURS UNITS			
	17	BINARY GROUP 8				BG FLAG 75	UNASSIGNED	HOURS TENS	
VITC	18								
Read2	...	SAME BIT DEFINITION AS VITC READ1 BUFFER							
	1F								
VITC	20								
Write	...	SAME BIT DEFINITION AS VITC READ1 BUFFER							
	27								
Regs	28	BURN-IN WINDOW COLUMN							
	29	BURN-IN WINDOW LINE							
	2A	FRAMES							
	2B	SECONDS							
	2C	MINUTES							
	2D	HOURS							
	2E	VITC1WE	0	0	----------	VITC WRITE LINE 1			----------
	2F	VITC2WE	0	0	----------	VITC WRITE LINE 2			----------
	30	VITC1RE	NOCODE1	CRCERR1	----------	VITC WRITE LINE 1			----------
	31	VITC2RE	NOCODE2	CRCERR2	----------	VITC READ LINE 2			----------
	32	PAL	VID2_S	VID1_S	VOUTSEL	VITCSEL	VSYNCSEL	VTRES	GEN_EN
	33	0	0	VIDEO LINE INTERRUPT (LINE#)					
	34	LTCOUTSEL	LTCSYNCSEL		LTXEN	LXCLKSEL	0	0	0
	35	0	0	0		LTC GAIN			
	36	FRAME RATE (low byte, write only)							
	37	0	0	0	0	FRAME RATE (high byte, write only)			
	38	reserved							
	39	reserved							
	3A	reserved							
	3B	reserved							
	3C	reserved							
	3D	reserved							
	3E	reserved							
	3F	SOFT LTC SYNC (write only, no data)							

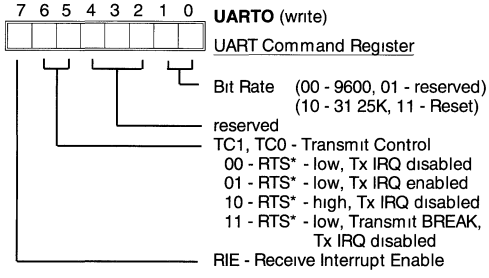
UART Registers

The UART emulates a 6850. Since the UART is tailored to MIDI applications, some of the generic 6850 functions have been omitted. The registers described below reflect that.

The two UART registers, Command/Status and Data, are accessible to the processor as shown in the following map.

UARTCS*	A1	A0	REGISTER
0	X	0	UART Command/Status Register
0	X	1	UART Data Register

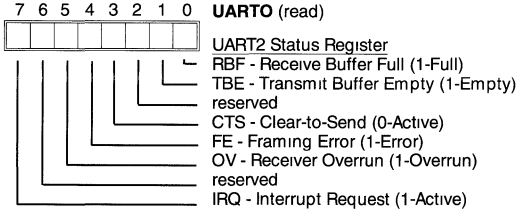
UART Command/Status Register



Bit Rate - This field selects the bit rate for data transmit and receive. After a master reset, its value is 11. One of the three bit rates must be selected in order to start the UART's operation. Writing a 11 will reset the UART.

TC1,TC0 - Bits 6 and 5, Transmit Control, provide control for transmit interrupt (when TBE is true), RTS control, and transmit BREAK level.

RIE - Bit 7, Receive interrupt enable, when set to one, enables the UART to interrupt the processor when the receive buffer is full or a receive overrun has occurred.



RBF - Bit 0, Receive Buffer Full, is set to 1 when read data is available in the UART data register. It is cleared to 0 when the UART data register is read.

TBE - Bit 1, Transmit Buffer Empty, is cleared to 0 when data is written to the UART data register. It is set to 1 when the UART transfers that data to its output shift register.

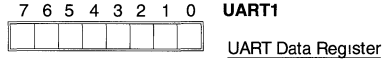
CTS - Bit 3, Clear-to-Send, is an active low status bit indicating the state of the CTS* input pin. A 0 in this bit position indicates that the modem or receiving device is ready to receive characters. A 1 indicates not ready. When CTS is inactive, 1, TBE is held at 0, the not-empty state.

FE - Bit 4, Framing Error, when set to 1, indicates that the receive character was improperly framed by the start and stop bits. It is detected by the absence of the first stop bit. This indicator is valid as long as the character data is valid.

OV - Bit 5, Receiver Overrun, is an error flag indicating that one or more characters in the data stream has been lost. It is set to 1 when a new character overwrites an old character which has not been read. The overrun error is cleared to 0 when a character is read from the UART data register.

IRQ - Bit 7, Interrupt Request, is a status bit which reflects the state of the interrupt request from the UART to the processor. When IRQ is 1, an interrupt is pending. Otherwise, no interrupt is pending.

The UART data register is actually two registers, a transmit buffer and a receive buffer. Writing to the data register causes the transmit buffer to be written. Reading from the data register causes the receive buffer to be read.



Absolute Maximum Ratings

Operating Temperature ..... 0 °C to + 70 °C
Storage Temperature ..... -65 °C to + 150 °C
Voltage on any pin to GND ..... -0.5V to V_{DD} + 0.5V
Voltage on V_{DD} to GND ..... -0.5V to + 7.0V
Power Dissipation ..... 1.0 watt

Note: Stress above that listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Operating the device at these levels is not recommended, and specifications are not implied.

DC Characteristics T_A= 0 °C to + 70 °C; V_{DD} = 5V± 10%; GND = 0V

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Digital Inputs					
Input Low Voltage	V_{IL}	-0.5		0.8	V
Input High Voltage	V_{IH}	2.0		V_{DD}+ 0.5	V
Input Leakage Current	I_{LI}			10	uA
Input Capacitance	C_{IN}			7	pF
Digital Outputs					
Output Low Voltage (I_{OL} = 4.0mA)	V_{OL}			0.4	V
Output High Voltage (I_{OH} = 0.4mA)	V_{OH}	2.4			V
Tri-State Current	I_{OZ}			10	uA
Output Capacitance				10	pF
Bi-Directional Capacitance				10	pF
Analog Inputs					
Video Input Voltage (Y1, Y2, C1, C2)			1.0		V_{p-p}
LTC Differential Input Voltage		0.1			V_{p-p}
LTCIN+ , LTCIN-, CLICK, FRAME input voltage		-0.3		V_{DD}+ 0.3	V
CLICK and FRAME bias voltage			V_{DD}/3		V
Analog Outputs					
Video output Voltage (YOUT, COUT)			1.0		V_{p-p}
LTC Output Voltage (Volume set at max.; I_{out} = 35mA)			2.0		V_{p-p}
LTC Output Voltage Amplitude Control Step			3		dB
LTC Output Voltage Amplitude Range			33		dB
Analog V_{DD} Supply Current	I_{DD1}			50	mA
Digital V_{DD} Supply Current	I_{DD2}			5	mA

AC Characteristics T_A= 0 °C to + 70 °C; V_{DD} = 5V± 10%; GND = 0V

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Address setup to IOR* or IOW* command	t_{ACS}	20			ns
Address hold from IOR* or IOW* command	t_{AH}	10			ns
Read pulse width	t_{RD}	50			ns
Access time	t_{ACC}			150	ns
Output enable access time	t_{OE}			50	ns
Data hold from IOR* high	t_{RDH}	10			ns
Read command inactive time	t_{RHRL}	210			ns
Write pulse width	t_{WR}	50			ns
Write data setup to IOW* high	t_{WDS}	20			ns
Write data hold from IOW* high	t_{WDH}	10			ns
Write command inactive time	t_{WHWL}	210			ns
CS* inactive time (Note 1)	t_{CHCL}	20			ns
UART Port Bit Rate (Command Register [1:0]= 00)			9.6		kHz
(Command Register [1:0]= 01)			31.3		kHz
(Command Register [1:0]= 10)			reserved		kHz

Note 1: This timing parameter must be met for proper operation of indirect register access using auto-increment.

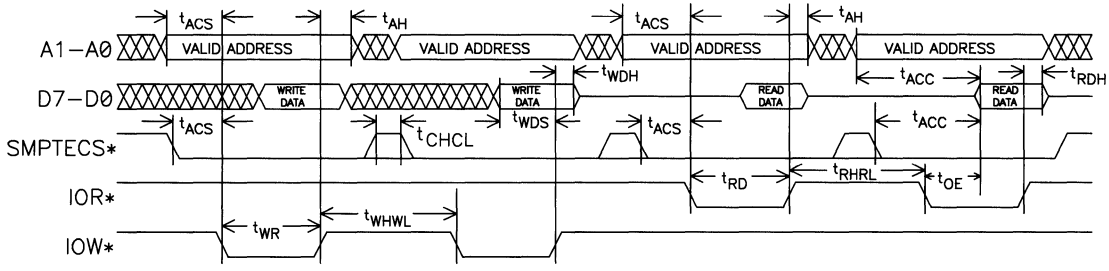


Figure 3 - Host Processor Bus Timing

Applications

Crystal Oscillator

This oscillator will operate properly with either a serial or parallel resonant crystal. If frequency accuracy is critical, a parallel resonant crystal is recommended. In this case the load capacitance is the series equivalent of the two capacitors connected from the crystal to ground.

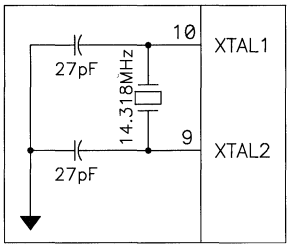


Figure 4 - Crystal Oscillator

Typical capacitance values of 27pF will produce a loading capacitance of about 15pF (with stray capacitance figured in).

Threshold Bypass Inputs

These inputs are used to set the clamping, SYNC extraction and data extraction threshold voltages. The values shown in Figure 5 are selected for a nominal RS-170 signal of 1Vp-p.

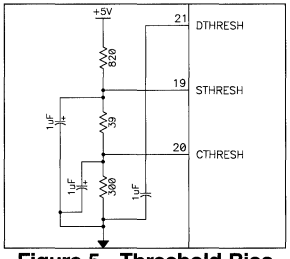


Figure 5 - Threshold Bias

If there are problems locking the **ICS2008** to incoming video, check the video on Y1 or Y2 with respect to CTHRESH and STHRESH.

CTHRESH is the threshold to which the input video sync tips are clamped. The CTHRESH level is nominally 1.3V. With the incoming video riding on this 1.3V DC level, the internal SYNC separator sizes the video at 20 IRE up from the SYNC tips. This level, STHRESH, is nominally 1.44V. The SYNC separator ignores short pulses which fall below the STHRESH level such as these that come from the chroma component of the video.

Care should be taken to keep lead to these pins short and clear of any digital signal traces.

Video Inputs

Y1, Y2, C1 and C2 pins must be capacitively coupled to the terminated video source(s). These inputs are clamped to the CTHRESH level. A typicalcoupling capacitance is .1uF.

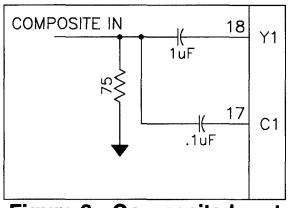


Figure 6 - Composite Input

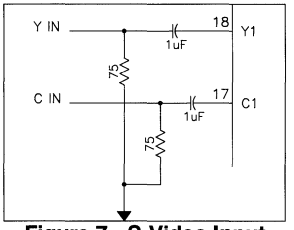


Figure 7 - S-Video Input

Video Outputs

YOUT and COUT are outputs of analog multiplexers which select the video source from Y1, C1 or Y2, C2. These outputs are not buffered. This minimizes signal distortion. It is, therefore, important to keep the capacitive and resistive load on the YOUT and COUT pins to a minimum. A video output buffer is shown in Figure 8. The plus input of the opamp should be high impedance, and its output should be able to drive a 75 ohm load with an appropriate video bandwidth. In general, composite NTSC and S-video signals have a bandwidth of 4.2MHz. A minimum output buffer bandwidth of 10MHz is recommended. Care should be taken in board layout to minimize stray capacitance on the YOUT and COUT pins. Otherwise, there could be high frequency rolloff. This could result in a loss of chrominance amplitude.

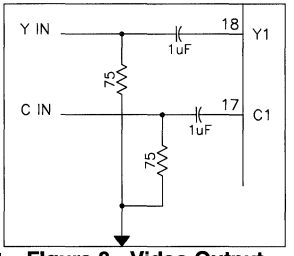


Figure 8 - Video Output

Self Biased Inputs

The CLICK and FRAME inputs are biased to 1/2 VDD and connected to plus inputs of two comparators. The minus inputs are internally biased to 1/2 VDD. When CLICK or FRAME sources are analog, they should be capacitively coupled to the input pin. However, if the sources are digital, they may be tied to the pins directly. It is important to make sure that the digital levels into these pins swing above and below the 1/2 VDD threshold of the comparators. This is not a problem with digital CMOS sources, but it could be with TTL sources.

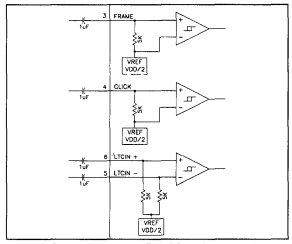


Figure 9 - Self Biased Inputs

LTCIN+ and LTCIN- are comparator inputs for the LTC input. This differential input is provided to maximize noise immunity. If the LTC source is single ended, the LTCIN- should be capacitively coupled to the ground reference of that source. If the LTC source is digital, set the LTCIN- to the desired threshold, and connect the digital source to LTCIN+ .

LFC Pin

This pin should be tied to V_{DD}.

Programming

The **ICS2008** is a SMPTE time code input/output device with a UART which can be used as a MIDI UART or transport control UART. All of the time critical functions to read and generate time code are performed by the chip's hardware, but all of the intelligence for processing time codes and generating the time code values are performed via an external processor. This makes the **ICS2008** flexible enough for a broad range of applications without making the processing requirements on the host system too great.

In the case of the LTC receiver, LTC data is received into a temporary buffer and transferred into the LTC read register (IR0 to IR7) when the last bit of LTC data has been received. It should be noted that the data is transferred before the SYNC pattern has been received. Once the data is in the LTC receive buffer, the LRI bit is set to one in the SMPTE0 register. If the LRIEN bit (SMPTE0) is set to a one, an interrupt will be generated. The interrupt is cleared when the SMPTE0 register is read. The data in the LTC receive buffer remains valid until the next LTC frame has been completely received.

The LTC generator transfers data from the LTC Write registers (IR8 to IRf) to the output buffer when the LTC generator is enabled; LTCEN is set to one. Data transfers for subsequent LTC frames occur eight bit times before the end of the LTC frame being output. Remember that a LTC frame ends with a 16 bit SYNC pattern. The LXI interrupt bit in SMPTE0 is set to one when LTC Write register data is transferred to the output buffer.

The UART has a four deep FIFO for its receive buffer. This allows for relaxed interrupt latency requirements. In the case of MIDI bit rates, the receiver will not overflow even if the interrupt response delay is 1msec.

Indirect Register Access

Indirect registers are accessed via the SMPTE2 (address) and SMPTE3 (data) registers. To read an indirect register, the program must first write its address to SMPTE2. Then the data is read from SMPTE3. Writing to an indirect register is similar. First, the address is written to SMPTE2. Then the data is written to SMPTE3.

In order to minimize the number of accesses required to read or write a block of registers, an auto-increment function is provided. If the MSB of SMPTE2 is written to a one with the address, the address is incremented after each read or write access to SMPTE3. For example, if one wants to read the LTC Read registers, IR0 to IR7, SMPTE2 is written to a 80h. Then SMPTE3 is read eight times. The first byte read is from IR0 followed by IR1, etc. The auto increment feature will not operate properly if CS* is not returned to the inactive state between accesses. See the AC timing section.

Interrupt Processing

Interrupts can be generated from four sources, LTC receiver, LTC generator, video line count and UART. The interrupt status of the first three interrupts, LRI, LXI, and VLI are in the SMPTE0 register. After this register is read, all three interrupts are cleared. It is, therefore, necessary to save the state of the interrupt status and process all active interrupts.

The UART interrupt status is in the UART0 register. The receive interrupt is cleared by reading the receive data register, UART1. The transmit interrupt is cleared by writing data to the transmit data register, UART1.

Reading LTC

LTC input data in available in the LTC Read registers after the last LTC data bit has been received. It is not necessary to wait for the LTC SYNC pattern to be complete. When LTC read data is available the LRI bit in SMPTE0 is set to one. If LRIEN is set to one, an interrupt is generated. LRI and the interrupt are cleared by reading SMPTE0. Data will remain valid until the last LTC data bit of the next frame has been received.

Generating LTC

A typical program for generating LTC output would first setup the LTC control registers and the LTC bit time registers. Then time code data would be written to the LTC Write register. Once this setup is done the LTC output would be enabled by setting LTCEN to a one. LTC output starts when a LTC SYNC is received. The LTC SYNC source is selected as part of the setup. While the LTC generator is waiting for SYNC, the data in the LTC Write register is transferred to the output buffer. When the transfer is complete the LXI status but is set to a one. The data for the next LTC output frame can then be loaded. The LXI status bit will be set to a one after the data transfer at the end of the first LTC output frame. At this point the LTC Write register is ready to receive data for the third LTC output frame.

The SMPTE1 register contains two status bits which indicate whether LTC data is being received and if so which direction. LTCLOCK is set to one when the LTC receiver has received a valid LTC SYNC pattern and data is still coming in. CODEDIR indicates the direction of the LTC SYNC pattern. This is useful to tell whether a tape with LTC is shuttling forwards or backwards.

Reading VITC

To read VITC code one must first setup IR30 thru IR33. The VITC Read Line registers, IR30 and IR31, select the video line from which VITC code is to be read. The MSB is the enable for VITC reading. The Read Line field, bits 4 to 0, should be programmed with the desired line number minus ten. So, if line 15 is desired, a 5 should be programmed in the Read Line field. IR32 selects the source and type of video. The GENLOCK ENABLE bit must be set to a one, and the VTRES bit must be set to a zero. The Video Interrupt Line register, IR33 should be set to a line after all VITC read and write lines. This allows all of the VITC receive and generate operations to be complete before processing VITC.

The VLOCK bit in the SMPTE1 register indicates whether the **ICS2008** is genlocked to the selected video source. Without the VLOCK status set to one, no VITC read will occur.

With VLOCK set to one and the control registers properly initialized VITC data is received a byte at a time from the video signal and written to the VITC Read registers. At the end of the VITC data frame the CRC byte is checked, and the result reported in bit 5 of IR30 and IR31. In addition to the CRC check, if a full VITC data frame is not received, the NOCODE bit, bit 6, is set to a one.

Generating VITC

Like reading VITC, IR2e, IR2f, IR32 and IR33 must be setup in order to generate VITC. The VITC Write Line registers, IR2e and IR2f, select the video line to which VITC code is to be written. The MSB is the enable for VITC generation. The Write Line field, bits 4 to 0, should be programmed with the desired line number minus ten. So, if line 12 is desired, a 2 should be programmed in the Write Line field. IR32 selects the source and type of video. The GENLOCK ENABLE bit must be set to a one, and the VTRES bit must be set to a zero. The Video Interrupt Line register, IR33 should be set to a line after all VITC read and write lines. This allows all of the VITC receive and generate operations to be complete before processing VITC.

With the VITC generator setup properly, when the selected video line starts, the VITC data in the VITC Write buffer, IR20 to IR27, is output. The video line interrupt, VLI in SMPTE0, is provided to allow ample processing time for VITC generation.

Burn-in Window

The burn-in window can be placed anywhere on the video display. The position of the upper left corner of the window is selected by the values written in IR28 and IR29. IR28 controls the horizontal position. Values from 00h to 71h put the corner in the first half of a video line (starting from the falling edge of HSYNC). Values from 80h to f1h put the corner in the second half of a video line. Any other values will not display the window. Care should be taken not to choose values which put the window in any part of the blanking area. IR29 controls the vertical position. The value written here is the video line number divided by 2.

IR2a to IR2d, are the registers which control the characters displayed in the burn-in window.

SMPTE Time Code Receiver/Generator

General Description

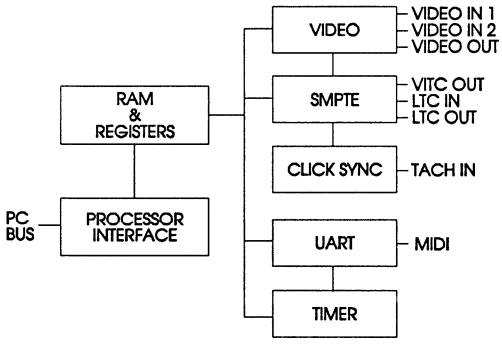
The **ICS2008A**, SMPTE Time Code Receiver/Generator chip, is a VLSI device designed in a low power CMOS process. This device provides the timing coordination for Multimedia sight and sound events. Although it is aimed at a PC Multimedia environment, the **ICS2008A** is easily integrated into products requiring SMPTE time code generation and/or reception in LTC (Longitudinal Time Code) and/or VITC (Vertical Interval Time Code) formats and MTC (MIDI Time Code) translation.

Taking its input from composite video, S-Video, or an audio track, the **ICS2008A** can read SMPTE time code in VITC and LTC formats. Time code output formats are LTC and VITC. All are available simultaneously. A UART is provided for the user to support MTC or tape transport control.

The processor interface is compatible with the IBM PC and ISA bus compatible computers and is easily interfaced to other processors.

The **ICS2008A** is an improved version of the **ICS2008**, with additional features and capabilities.

Block Diagram



Features

- Internal and external sync sources
  - Genlock to video or house sync inputs
  - Internally generated timing from oscillator input
  - External click input
- LTC and VITC Generators
  - Real Time SMPTE Rates: 30Hz, 29.97Hz, 25Hz, 24Hz
  - Time Code Modes: Drop Frame and Color Frame
  - VITC can be inserted on two lines from 10-40 (SMPTE specifies lines 10-20)
  - "Jam Sync," "freewheeling," error bypass/correction, and plus-one-frame capability
- LTC Receiver
  - Meets SMPTE and EBU LTC specifications
  - Synchronize bit rates from 1/30th nominal to 80X nominal playback speed
- VITC reader
  - Reads code from any or all selected scan lines
  - Meets SMPTE VITC specifications

New, Improved Features

- Time Code Burn-in Window selectable to overlay video with programmable screen position, size and black/white polarity
- Internal Timer, allows 1/4 Frame MIDI Time Code Messages
- LTC edge rate control, conforms to EBU Tr and Tf specification
- Improved video timing lock during VCR pause and shuttle modes
- VITC search mode, will search through VBI lines until VITC is found
- New UART frequency of 38.4 Kbaud for tape transport control
- Improved video output performance

Digitally Controlled Audio Mixer

Description

The **ICS2101** is a CMOS monolithic integrated circuit that fills the need for a digitally-controlled multi-channel line-level stereo audio mixer. The ten input channels may be treated as separate mono inputs, as stereo pairs or as a combination of mono and stereo inputs. High-performance attenuators provide accurate gain control with a minimum of noise. Stereo balance and mono panning functions are supported. The primary application for this part is in audio cards for multi-media personal computers.

Features

- 5 Stereo Input Pairs
- 1 Stereo Output Pair
- Logarithmic Attenuation: 7-Bit Resolution -- 0.5 dB per step
- Separate Attenuation and Balance Control for each Input Pair
- Mono Input Mode with Panning
- Master Attenuation and Balance Control for Output
- Low Noise, Low Distortion

Architecture

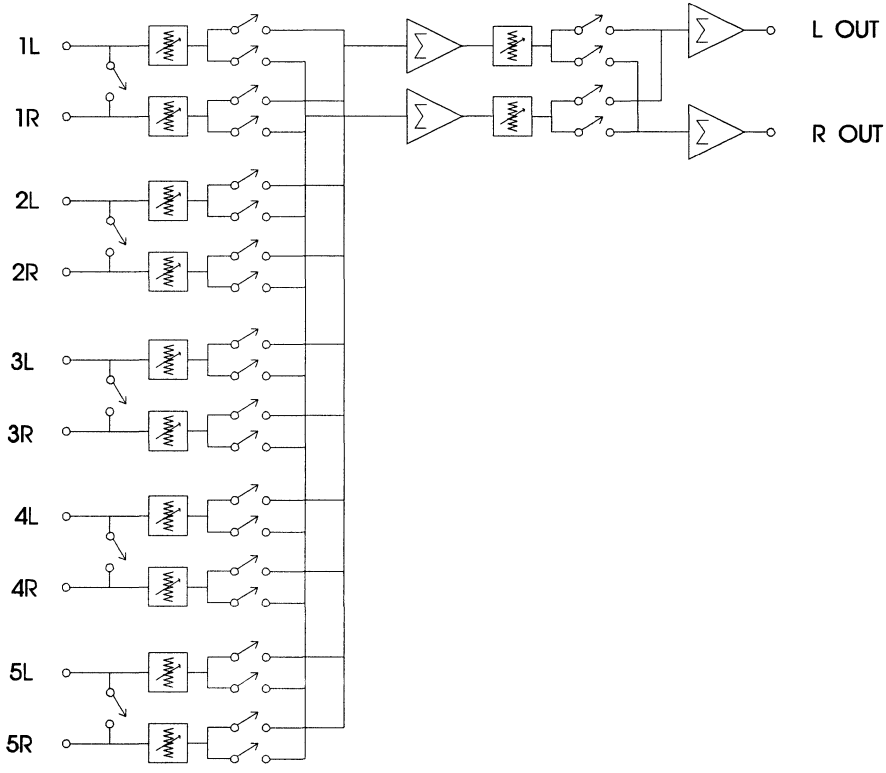


Figure 1 - Basic Block Diagram

The audio inputs are logically grouped into five stereo pairs. Each input passes through a digitally controlled attenuator and a buffer amplifier. The output of the buffer may be connected to either or both of the stereo summing buses. On-chip logic manages the two attenuators to achieve both level and balance control.

The outputs of the sum amps are applied to the master attenuation/balance controls and then to the buffer amps to deliver the signals to the outside world.

Absolute Maximum Ratings

Storage Temperature	-65 °C to 150 °C
Voltage on any pin with respect to ground	-0.3V to V_{DD}+ 0.3V
Maximum V_{DD}	7V
Power Dissipation	1W

Standard Test Conditions

Operating Temperature Range	0 °C to 70 °C
Power Supply Voltage	4.75 to 5.25 Volts

DC Characteristics

V_{DD} = 5V ± 5%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IH}	Logical 1 Input Voltage	2.4		V_{DDD}	V	
V_{IL}	Logical 0 Input Voltage	0		0.8	V	
I_{IL}	Input Leakage Current	-1		1	uA	0 < V_{IN} < V_{DDD}
I_{OH}	Output Source Current	-100			mA	V_{OUT} = V_{REF} + IV Master alternators off
I_{OL}	Output Sink Current			100	mA	V_{OUT} = V_{REF} - IV Master alternators off
V_{REF}	Internal Reference V		.44 V_{DD}		V	
I_{ADD}	Analog Suppiy Current		7	10	mA	
I_{DDD}	Digital Supply Current		10	100	µA	

AC Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
	ANALOG					
V_{AI}	Analog Input Voltage			3	Vpp	AC coupled
A_F	Analog Frequency Range	20		20,000	Hz	
R_{IN}	Attenuator Input Resistance	20	32		K ohm	Gain = 0dB
T_{HD}	Total Harmonic Distortion		0.2		%	2Vp-p, 1 KHz, Gain = 0dB
S_{NR}	Signal to Noise Ratio		86		dB	Gain = 0dB BW = 20 to 20 KHz
R_{MONO}	Mono Switch Resistance	100	200	400	ohms	
N_{CR}	Crosstalk - L/R Channel		78		db	1 KHz, 2 VPP Gain = 0db
ΔG	Analog Output Step		0.5		dB	Atten. value 127 through 16
	DIGITAL					
T_{RESET}	Reset Pulse Width	200			ns	
T_{IOWL}	IOW Pulse Width Low	80			ns	
T_{IOWH}	IOW Pulse Width High	120			ns	
T_{CSS}	Chip Select Setup Time	25			ns	
T_{CSH}	Chip Select Hold Time	25			ns	
T_{DS}	Data Setup Time	25			ns	
T_{DH}	Data Hold Time	25			ns	

Timing Waveforms

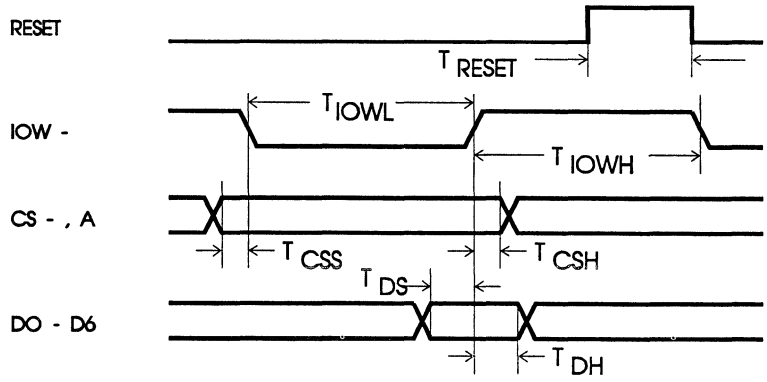


Figure 2 - Timing Diagram

Pin Descriptions

PIN NUMBER	PIN SYMBOL
1	1L
2	1R
3	CS-
4	V_{DDD}
5	IOW-
6	D0
7	D1
8	D2
9	D3
10	D4
11	D5
12	D6
13	V_{SSD}
14	A

PIN NUMBER	PIN SYMBOL
15	RESET
16	5L
17	5R
18	V_{DDA}
19	4L
20	4R
21	R OUT
22	L OUT
23	VREF
24	V_{SSA}
25	3L
26	3R
27	2L
28	2R

Reset: Active high. All control, pan, and attenuation registers are set to zeros.

Chip Select (CS-): Active low input. Chip select must be low at the trailing edge of the -IOW pulse to select the device.

Input Output Write (IOW-): Active low input. When the chip is enabled, it latches data from the bus on the rising edge of IOW.

Address/Data (A): Input. When this input is high, the address register is selected; when low, the data register associated with the contents of the address register is selected.

Data bus (D0 - D6): Active high input.

Audio Inputs (1L-5L, 1R-5R): Audio connections to the input attenuators. These inputs are internally referenced to VREF and are normally fed via an external coupling capacitor.

Audio Outputs (L OUT, R OUT): Line level audio outputs.

Reference Voltage (VREF): Internally generated reference voltage of approximately 0.44 V_{DDA}. A 1000pf capacitor should be connected between this pin and V_{SSA}.

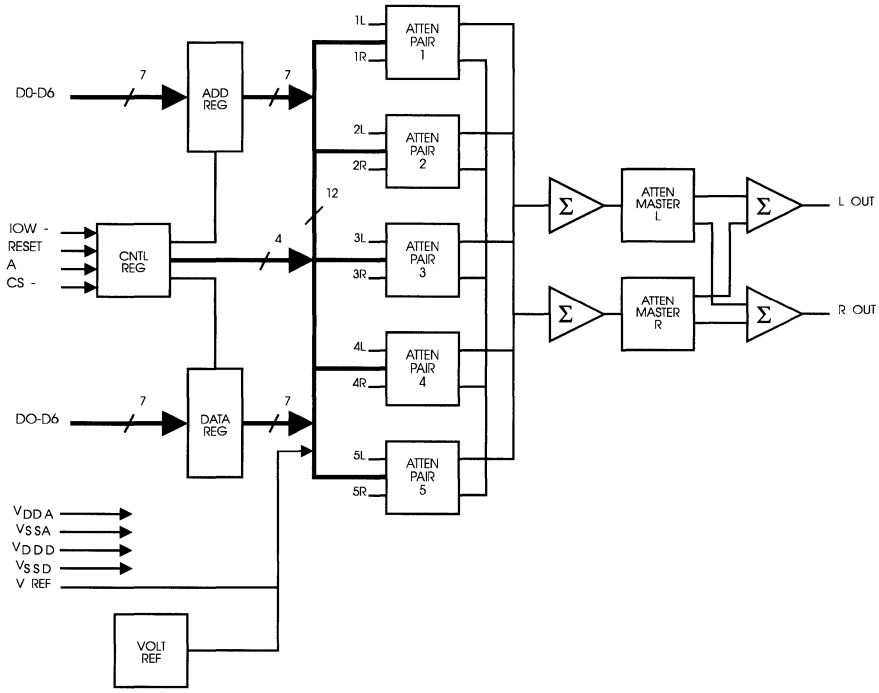


Figure 3 - Block Diagram

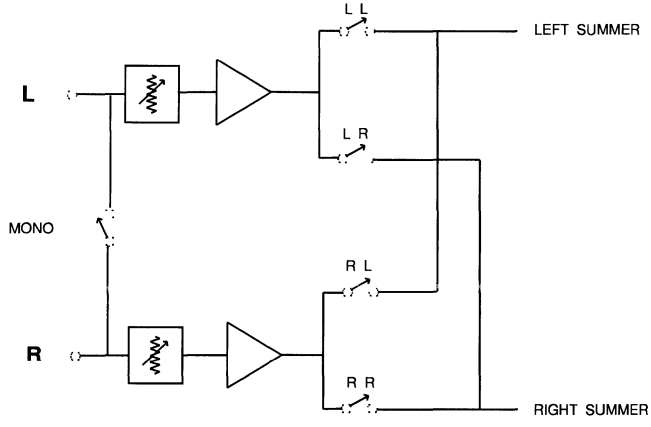


Figure 4 - Attenuator Pair Detail

Attenuation Control

Each attenuator is controlled by a 7-bit value written into its control register. Values of 127 through 16 increase the attenuation in one-half dB steps. Values of 15 through 0 cause the attenuation to approach infinity in increasingly coarser steps. This ensures that the channel is completely off when the control is at minimum value.

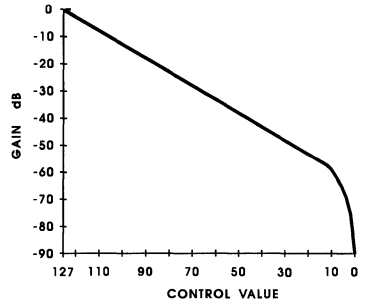


Figure 5 - Attenuation vs. Control Value

Registers and Modes of Operation

Address Register
The address register is used to point to the internal registers per the table listed at right:

Control Registers / Modes of Operation
Each attenuator pair may be operated in one of three modes and is controlled by five registers:

Left Control and Left Attenuation Register

Right Control and Right Attenuation Register (Normal Mode only)

Pan-Balance Position Register (Pan/Balance Mode only)

Address Register BITS: XX543210	
BITS 5, 4, 3	0, 0, 0 = Pair 1 0, 0, 1 = Pair 2 0, 1, 0 = Pair 3 0, 1, 1 = Pair 4 1, 0, 0 = Pair 5 1, 0, 1 = Master
BITS 2, 1, 0	0, 0, 0 = Control Left 0, 0, 1 = Control Right 0, 1, 0 = Attenuator Left 0, 1, 1 = Attenuator Right 1, 0, X = Pan

Normal Mode
In the normal mode, both the left and right control and attenuation registers are active, and the L and R inputs to an attenuator pair may be separately controlled. The mono switch is always open.

L CONTROL REG 3210	SWITCH LL	SWITCH LR
0000	off	off
0001	on	off
0010	off	on
0011	on	on

R CONTROL REG 3210	SWITCH RL	SWITCH RR
0000	off	off
0001	on	off
0010	off	on
0011	on	on

Stereo Mode

In the stereo mode the left control register controls the mode of the attenuator pair, and values written to the left attenuation register are sent to both the left and right channels. The gain of both channels is always equal. However, right control and attenuation registers are not inactive in this mode. Therefore, the host software must be careful not to write to the right control and attenuation registers while in the stereo mode. The master attenuator pair does not have a mono switch.

L CONTROL REG 3210	SWITCH LL	SWITCH LR	SWITCH RL	SWITCH RR	MONO SWITCH	OPERATION
0100	on	off	off	on	off	Stereo - Normal
0101	off	on	on	off	off	Stereo - Reversed Channels
0110	on	off	off	on	on	Mono
0111	off	on	on	off	on	Mono (Reserved)

Balance/Pan Mode

In the balance/pan mode, the left control register controls the mode of the attenuator pair, and the left attenuation register controls the overall gain of both channels. The balance/pan register controls the differential gain of the two attenuators, thereby regulating the balance of stereo signals and the panoramic position of mono signals in the stereo output of the mixer. The right control and attenuation registers are not inactive in this mode. Therefore, the host software must be careful not to write to the right control and attenuation registers while in the balance/pan mode. The pan mode does not apply to the master attenuator pair, as it does not have a mono switch.

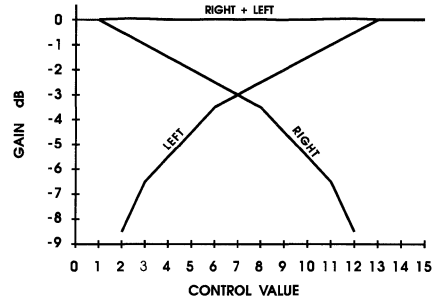


Figure 6

L CONTROL REG 3210	SWITCH LL	SWITCH LR	SWITCH RL	SWITCH RR	MONO SWITCH	OPERATION
1000	on	off	off	on	off	Balance - Normal
1001	off	on	on	off	off	Balance - Reversed Channels
1010	on	off	off	on	on	Pan - Normal
1011	off	on	on	off	on	Pan - Reversed

Programming Considerations

From the host processor perspective, the mixer chip consists of two write-only registers: the address register and the data register. The host first writes a value to the address register, which selects the appropriate data register for subsequent data-write operations. If a series of values are to be written to a single register, as when gradually fading one attenuator, the address register need only be written with the appropriate value once at the beginning of the operation.

In the pan/balance mode, two separate attenuator registers are being internally managed to control an attenuator pair. The attenuation value directed to the left attenuation register gets modified by the contents of the pan/balance register, and the appropriate values are written into both the left and right attenuation registers. Note that when a channel's pan/balance register is modified, it has no effect on the attenuator settings until a subsequent value is written to the left attenuation register.

Package Information

The **ICS2101** is available in 28-pin DIP and SO packages.

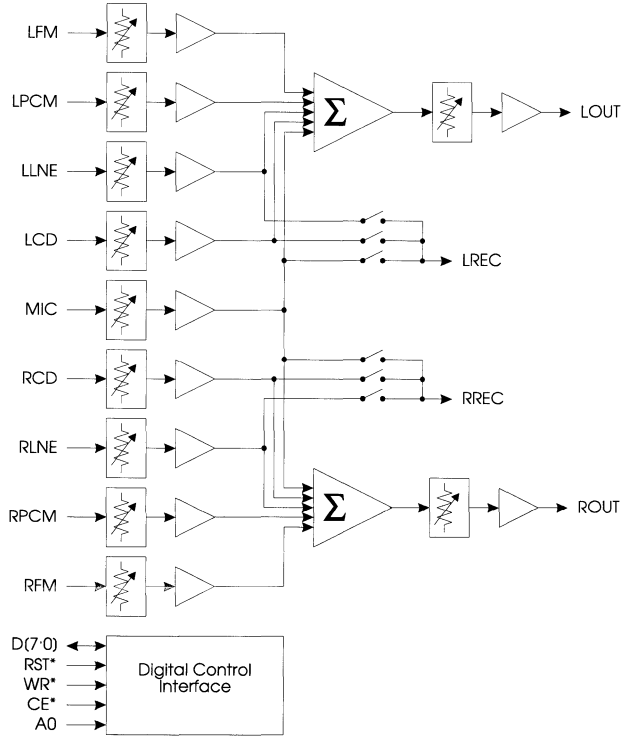
Sound Blaster™ Compatible Mixer

General Description

The **ICS2102** is a CMOS integrated circuit that provides mixing of 4 stereo and 1 monaural audio signals as well as master volume control. These functions are digitally controlled through Sound Blaster compatible mixer registers, an 8 bit parallel interface. The monaural microphone input has 4 levels of attenuation. The remaining 8 input channels have 8 levels of attenuation. The four stereo channels and one monaural channel are summed to form a composite signal before global volume controls are added. The master volume may be programmed with one of 8 levels of attenuation. This component performs all the necessary audio mixing for a product that is compatible with Sound Blaster Pro.™

Features

- 4 channel stereo and 1 monaural mixing
- 8 levels of independent channel input attenuation control, except microphone (4 levels)
- 8 level master volume control
- Separate digital and analog supplies
- 5V CMOS process
- 28 pin SOIC package



Sound Blaster and Sound Blaster Pro are trademarks of Creative Technologies, Inc

WaveFront™:General MIDI Wavetable Synthesis System

General Description

The WaveFront chip set provides professional quality music through wavetable synthesis. This form of synthesis achieves its startling realism by playing back short digital recordings of real instruments. With WaveFront, a simple design can sound like a full range of musical instruments at a cost that rivals artificial sounding FM synthesis.

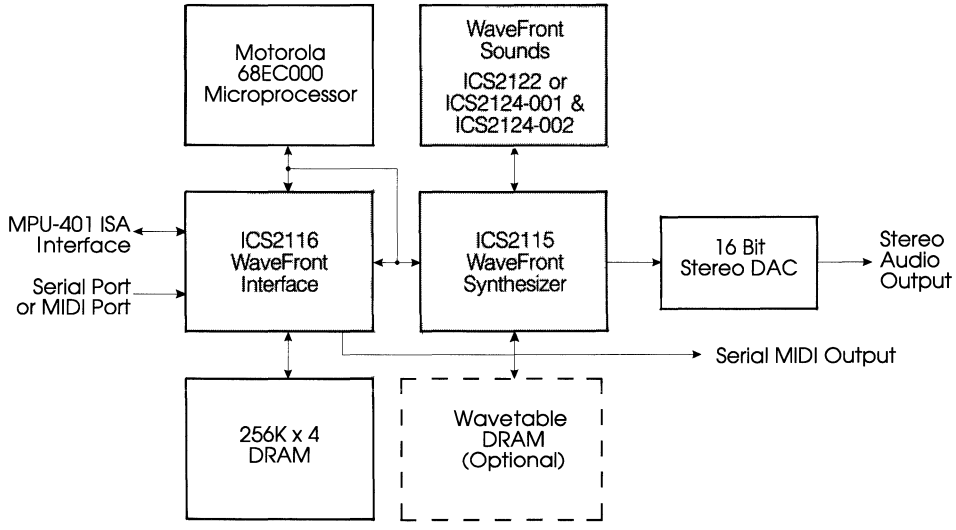
The primary component is the WaveFront Synthesizer, **ICS2115**, which has the ability to play 32 voices simultaneously. As a source for sound data, ICS offers WaveFront Sounds: **ICS2122**, **ICS2124-001** and **ICS2124-002**. These ROMs contain all the instruments in the extended version of the General MIDI specification (a standard developed by the IMA, International MIDI Association).

The WaveFront Interface, **ICS2116**, handles most of the support functions that a synthesizer requires. It allows WaveFront to communicate through a serial, parallel or port as well as the MPU-401 standard for the ISA bus. The **ICS2116** permits the WaveFront chip set to be a highly integrated system at a surprisingly low cost.

Features

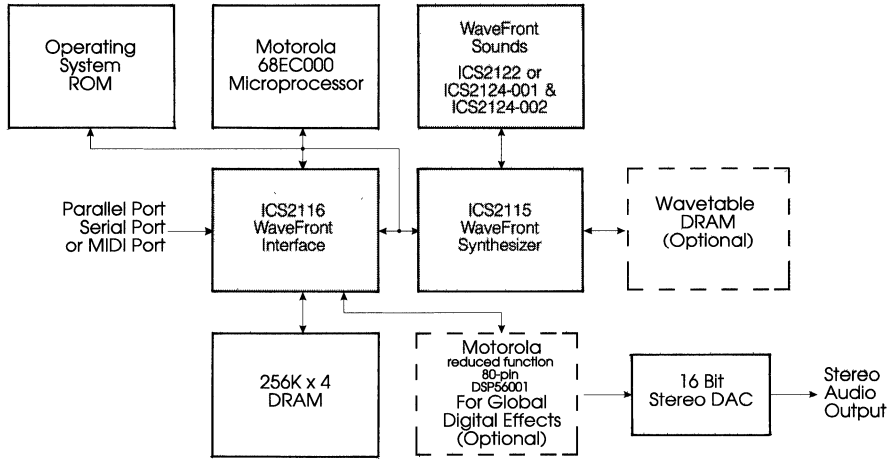
- Complete system for wavetable synthesis of General MIDI sounds
- Minimum of external components due to highly integrated design
- 24 voice polyphony using an output sample rate of 44.1kHz, or 32 voices at 33 kHz
- Serial and parallel port input provides interface with self contained unit
- MPU-401 emulation, for compatibility with thousands of DOS programs and the generic MPU-401 driver supplied with Microsoft Windows 3.1
- Two MIDI inputs and one output
- Well suited for both a ISA peripheral and a free standing unit
- No burden on host CPU for synthesis functions
- Option for 2MB or 4MB patch set
- Optional Wavetable DRAM for user samples
- Optional digital effects with free-standing unit

Block Diagram: WaveFront as an ISA Peripheral



WaveFront is a trademark of Integrated Circuit Systems, Inc.

Block Diagram: WaveFront as a Free-Standing Unit



Components for WaveFront Development

- WaveFront Operating System in two forms:
  - A binary file for an EPROM (for a free-standing unit)
  - A DOS executable that configures the system and downloads the code (for an ISA peripheral)
- Circuit Schematics of both the ISA peripheral and the free-standing design (OrCAD format)
- Gerber files of the two designs
- WaveFront Demo Board
  - ISA version
  - Free-standing version

Ordering Information

To construct one system using WaveFront, the following ICS parts are required:

- ICS2115 WaveFront Synthesizer (84-pin PLCC or 80-pin PQFP package)
- ICS2116 WaveFront Interface (100-pin PQFP package)
- WaveFront Sounds. Pick one of these three options:
  - ICS2122 for a 2MB patch set (44-pin SO package)
  - ICS2124-001 and ICS2124-002 for a 4MB patch set (each is a 44-pin SO package)
  - Obtain the mask file(s) for either the 2MB or 4MB patch sets and fabricate the masked ROMs.
- ICS2495-337 WaveFront Clock (This can be replaced by two crystal oscillators if desired)
  - ICS2495A-337 (20-pin DIP package)
  - ICS2495K-337 (20-pin SO package)

WaveFront™ Synthesizer

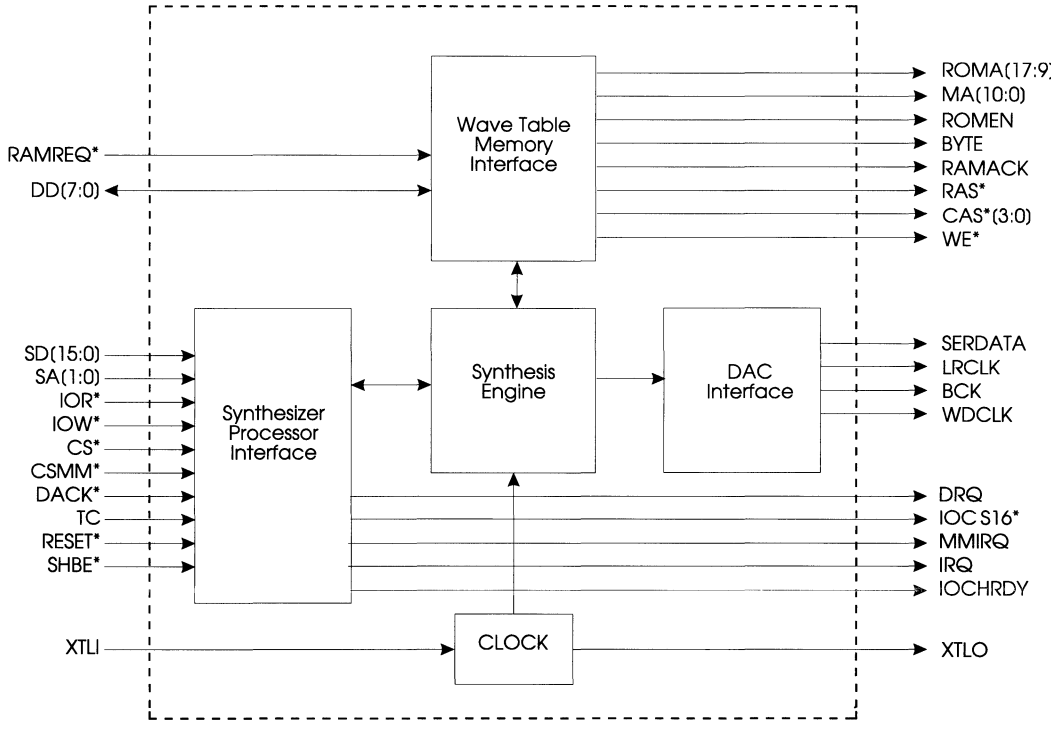
General Description

The WaveFront Synthesizer, **ICS2115**, is an audio synthesis chip which utilizes wavetable lookup to produce 16-bit, CD quality sound. The internal memory management unit allows both ROM, for standard samples, and low cost DRAM, for soft loadable samples, to be connected directly to the **ICS2115**. The WaveFront Synthesizer presents the audio output in 16-bit linear form for conversion by a low cost CD-type DAC.

Features

- Capable of addressing up to 32MB of wavetable ROM and up to 16MB of wavetable DRAM
- Variable Polyphony Rates: 24 voices at 44.1KHz through 32 voices at 33 kHz
- Uses 16 bit linear, 8 bit linear, and 8 bit u-Law wavetable data.
- Serial output for a CD player-type DAC

Block Diagram



WaveFront Interface

General Description

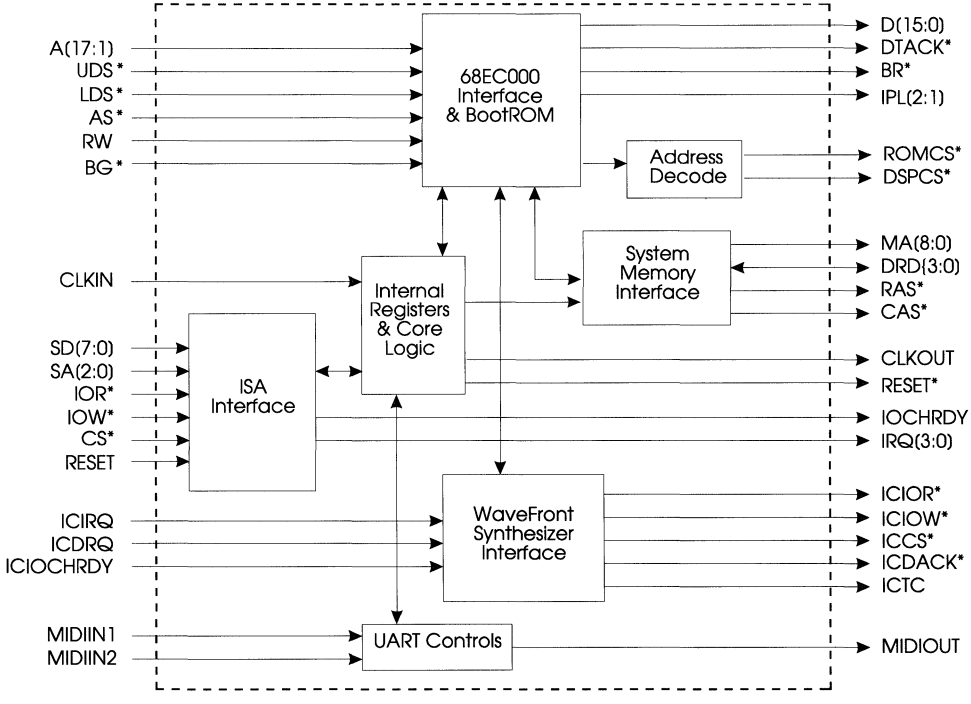
The WaveFront Interface is essential for a highly integrated design using the WaveFront Synthesizer. It incorporates an inexpensive Motorola 68EC000 microprocessor into the system. It also provides system RAM, address decoding, and data buffering to and from the input source. The input source can be a serial stream (including MIDI), a parallel port, or a set of registers on the ISA bus emulating MPU-401 or 6850 UART standards.

For systems not using the ISA bus, the WaveFront Interface can convert the serial output of the synthesizer into a form that a reduced-function Motorola 56001 DSP can read. This allows for global digital effects (such as reverb and chorus) to enhance the audio signal.

Features

- Provides the majority of system "glue" logic, for high integration and low cost.
- Uses a single inexpensive 256K x 4 DRAM as system memory
- Contains small code ROM, which eliminates the code ROM in an ISA design
- Soft select of 4 different IRQs on the ISA bus

Block Diagram



WaveFront Sounds

Description

The WaveFront Sounds, **ICS2122** and **ICS2124-001/-002**, are the sound material that comprises the wavetable for the WaveFront Synthesizer. Each part, a 2M x 8 masked ROM, contains all the information (digital recordings, loop points, volume contours, etc.) necessary to produce all the sounds in the General MIDI specification. For a 2MB sound set use the **ICS2122**, for a 4MB set use both the **ICS2124-001** and **ICS2124-002**.

Features

- 16 bit linear wavetable (**ICS2124-001/-002**) or compressed wave table (**ICS2122**) of General MIDI sounds
- Contains 128 instruments and 69 drum sounds

Instrument List

Acoustic Grand Piano
Bright Acoustic Piano
Electric Grand Piano
Honky-Tonk Piano
Electric Piano 1
Electric Piano 2
Harpsichord
Clavi
Celesta
Glockenspiel
Music Box
Vibraphone
Marimba
Xylophone
Tubular Bells
Dulcimer
Drawbar Organ
Percussive Organ
Rock Organ
Church Organ
Reed Organ
Accordian
Harmonica
Tango Accordian
Acoustic Guitar (nylon)
Acoustic Guitar (steel)
Electric Guitar (jazz)
Electric Guitar (clean)
Electric Guitar (muted)
Overdriven Guitar
Distortion Guitar
Guitar Harmonics
Acoustic Bass
Electric Bass (finger)
Electric Bass (pick)
Fretless Bass
Slap Bass 1
Slap Bass 2
Synth Bass 1
Synth Bass 2
Violin
Viola
Cello
Contrabass
Tremolo Strings
Pizzicato Strings
Orchestral Harp
Timpani
String Ensemble 1
String Ensemble 2
SynthStrings 1
SynthStrings 2
Choir Aahs
Voice Oohs
Synth Voice
Orchestra Hit
Trumpet
Trombone
Tuba
Muted Trumpet
French Horn
Brass Section
SynthBrass 1
SynthBrass 2
Soprano Sax
Alto Sax
Tenor Sax
Baritone Sax
Oboe
English Horn
Bassoon
Clarinet
Piccolo
Flute
Recorder
Pan Flute
Blown Bottle
Shakuhachi
Whistle
Ocarina
Lead 1 (square)
Lead 2 (sawtooth)
Lead 3 (calliope)
Lead 4 (chiff)
Lead 5 (charang)
Lead 6 (voice)
Lead 7 (fifths)
Lead 8 (bass + lead)
Pad 1 (new age)
Pad 2 (warm)
Pad 3 (polysynth)
Pad 4 (choir)
Pad 5 (bowed)
Pad 6 (metallic)
Pad 7 (halo)
Pad 8 (sweep)
FX 1 (rain)
FX 2 (soundtrack)
FX 3 (crystal)
FX 4 (atmosphere)
FX 5 (brightness)
FX 6 (goblins)
FX 7 (echoes)
FX 8 (sci-fi)
Sitar
Banjo
Shamisen
Koto
Kalimba
Bag Pipe
Fiddle
Shanai
Tinkle Bell
Agogo
Steel Drums
Wood Block
Taiko Drum
Melodic Tom
Synth Drum
Reverse Cymbal
Guitar Fret Noise
Breath Noise
Seashore
Bird Tweet
Telephone Ring
Helicopter
Applause
Gunshot
69 drum sounds

WaveFront Operating System Software

Description

The WaveFront Operating System software realizes the complete potential of the hardware. It manages a complex voice architecture where each voice has two envelopes with 6 segments, two LFOs and a modulation matrix. As shown in the chart below, the operating system responds to a comprehensive set of real time MIDI messages.

Features

- Full-featured implementation of a wavetable synthesizer
- Meets the synthesizer requirements of the MPC specification
- Selectable polyphony: 24 voices at 44.1kHz through 32 voices at 33 kHz

MIDI Implementation Chart

FUNCTION		TRANSMITTED	RECOGNIZED	REMARKS
Basic	Default	X	1 - 16	
Channel	Change	X	1 - 16	
	Default	X	Mode 3	Omni Off, Poly
Mode	Messages	X	Mode 3, 4 (m= 1)	*(see Notes)
	Altered	* * * * * * * * *		
Note		X	0 - 127	
Number	Sound Range	* * * * * * * * *	0 - 127	
Velocity	Note On	X	O	
	Note Off	X	X	
After	Key's	X	X	
Touch	Ch's	X	O	
Pitch Bend		X	O	Resolution: All 14 bits
	1	X	O	Modulation Wheel
	2	X	O	Breath Controller
	4	X	O	Foot Controller
Control	7	X	O	Volume
Change	10	X	O	Pan
	11	X	O	Expression Controller
	64	X	O	Sustain Pedal
	100, 101	X	O	RPN LSB, MSB
	120	X	O	All Sounds Off
	121	X	O	Reset All Controllers
Program		X	O	
Change		* * * * * * * * *	0 - 127	
System Exclusive		O	O	Dump & Receive Program Data
System	Song Pos	X	X	
Common	Song Sel	X	X	
	Tune	X	X	
System		X	X	
Real Time		X	X	
	Local ON/OFF	X	X	
Aux	All Notes Off	X	O (123 - 127)	
Messages	Active Sensing	X	O	
	Reset	X	X	

O: Yes X. No

NOTES: * Mode 4 (Omni Off, Mono) is recognized as m = 1 regardless of the value of m.

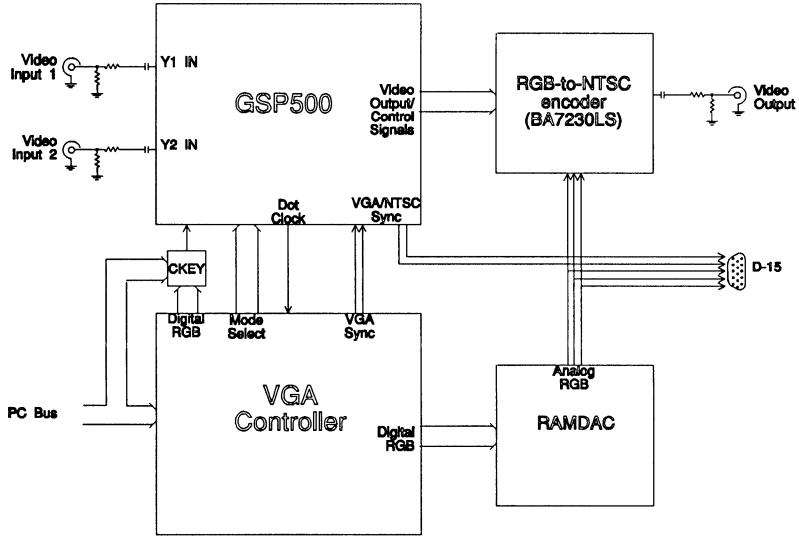
A

ICS

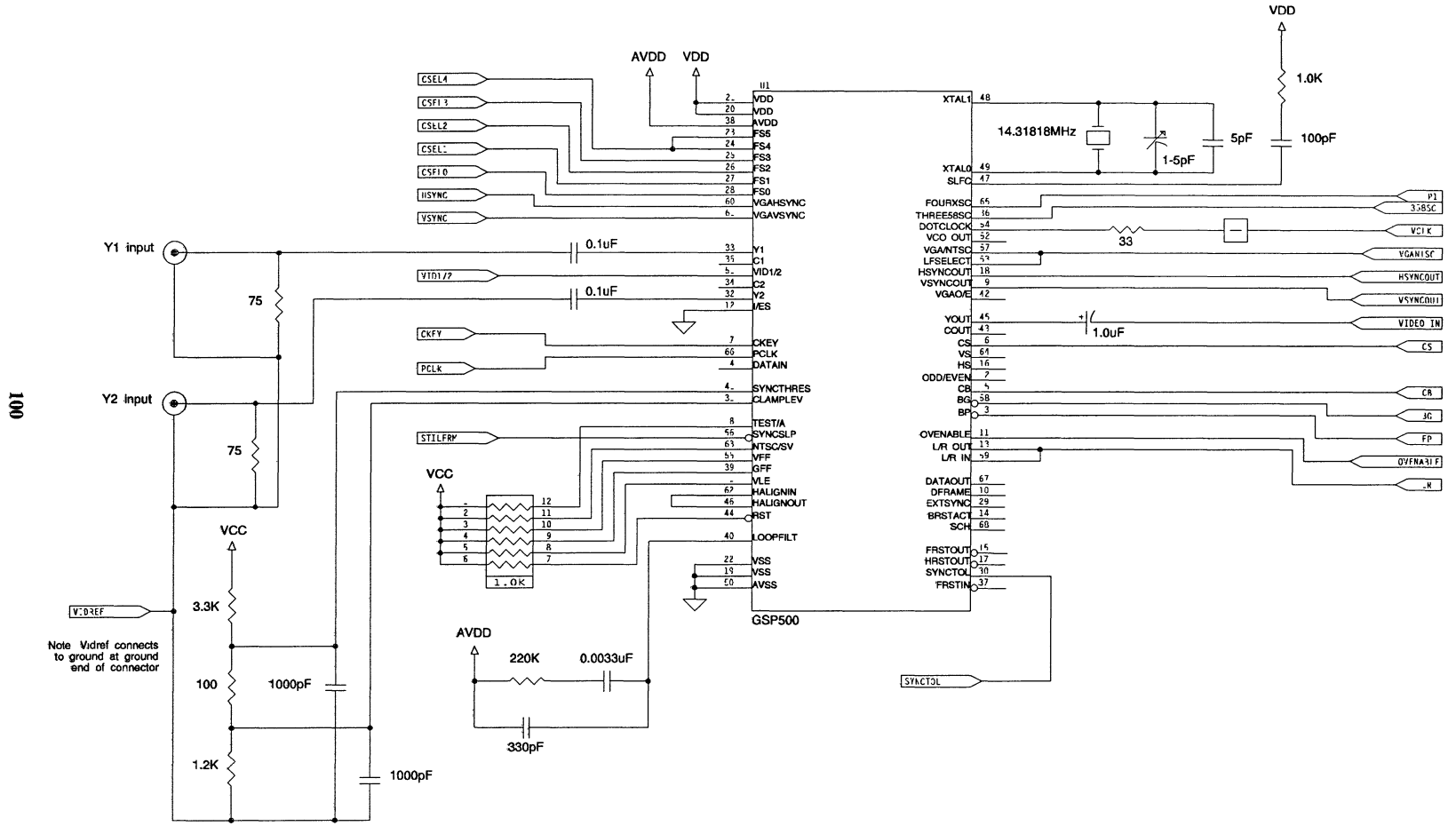
Multimedia Applications

Using the GSP500 with a Rohm BA7230LS Encoder

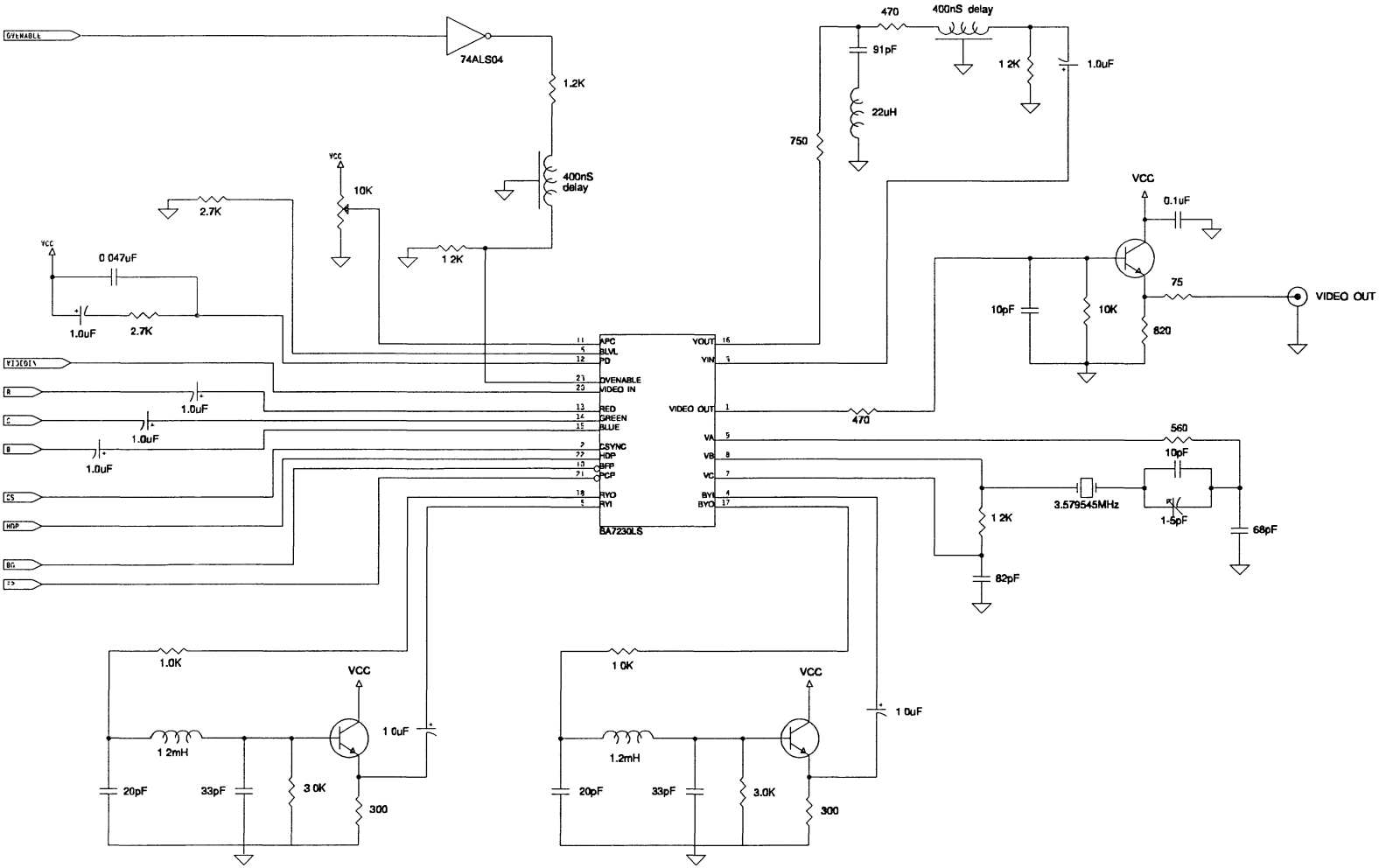
Contents



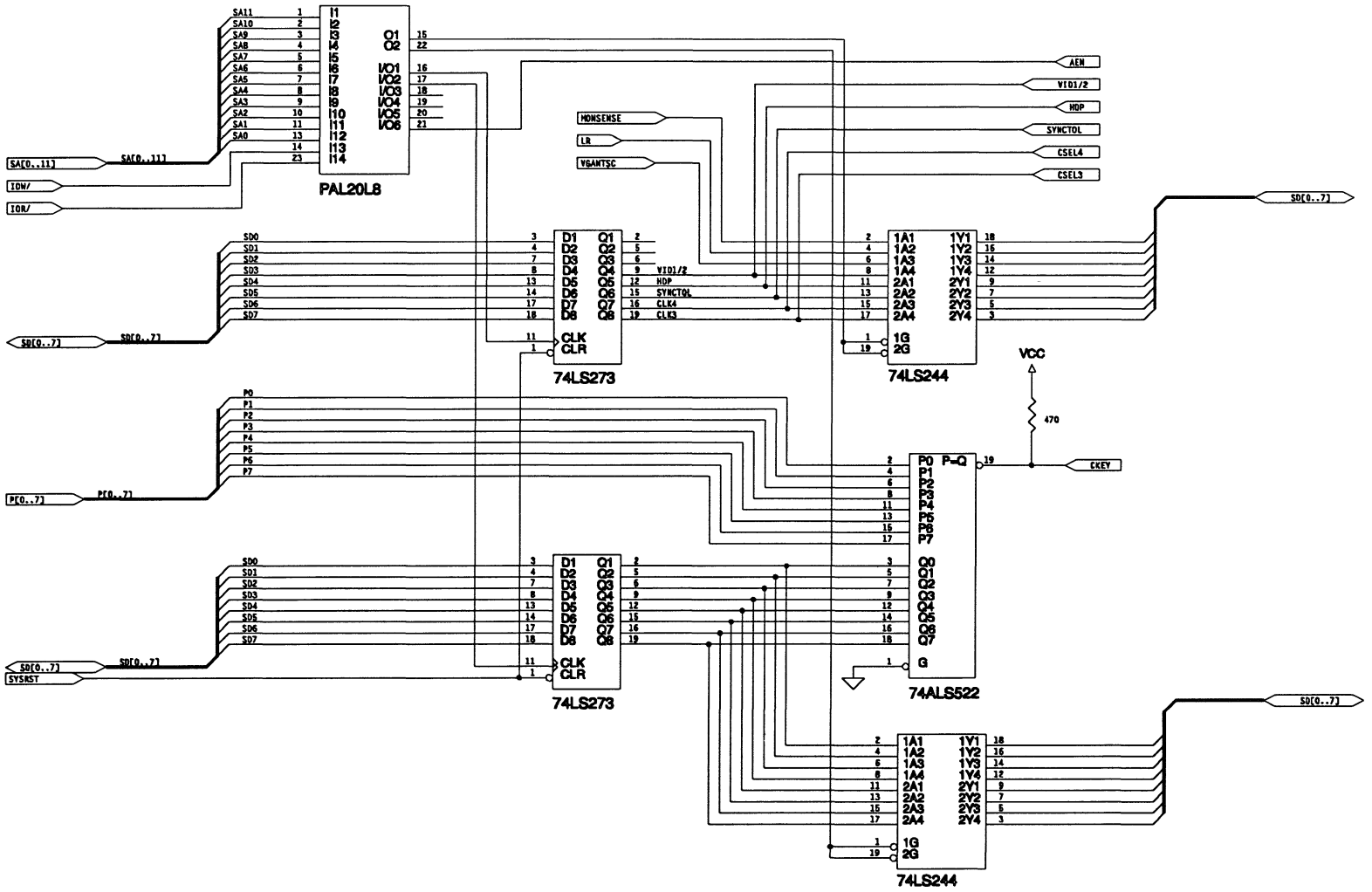
GSP500 Schematic, page 1 of 3: GSP500 Wiring



GSP500 Schematic, page 2 of 3: BA7230LS Wiring



GSP500 Schematic, page 3 of 3: Port Selection Wiring



PAL Equations - Expanded Product terms

HOLD1 = SA11
SA10
!SA9
!SA8
SA7
SA6
SA5

HOLD2 = SA4
SA3
!SA2

R306 = AEN & HOLD1 & HOLD2 & IOR & !IOW & !SA0 & SA1

R307 = AEN & HOLD1 & HOLD2 & IOR & !IOW & SA0 & SA1

W306 = AEN & HOLD1 & HOLD2 & !IOR & IOW & !SA0 & SA1

W307 = AEN & HOLD1 & HOLD2 & !IOR & IOW & SA0 & SA1

AEN.oe = 0

HOLD1.oe = 1

HOLD2.oe = 1

R306.oe = 1

R307.oe = 1

W306.oe = 1

W307.oe = 1

PAL Equations - Symbol Table

Pin Polarity	Variable Name	Ext	Pin	Type	Pterms used	Max Pterms	Min Level
!	AEN		21	V	—	—	—
	HOLD1		18	V	7	7	1
	HOLD2		19	V	3	7	1
!	IOR		23	V	—	—	—
!	IOW		14	V	—	—	—
!	R306		22	V	1	7	1
!	R307		15	V	1	7	1
	SA0		13	V	—	—	—
	SA1		11	V	—	—	—
	SA2		10	V	—	—	—
	SA3		9	V	—	—	—
	SA4		8	V	—	—	—
	SA5		7	V	—	—	—
	SA6		6	V	—	—	—
	SA7		5	V	—	—	—
	SA8		4	V	—	—	—
	SA9		3	V	—	—	—
	SA10		2	V	—	—	—
	SA11		1	V	—	—	—
!	W306		17	V	1	7	1
!	W307		16	V	1	7	1
	AEN	oe	21	D	1	1	0
	HOLD1	oe	18	D	1	1	0
	HOLD2	oe	19	D	1	1	0
	R306	oe	22	D	1	1	0
	R307	oe	15	D	1	1	0
	W306	oe	17	D	1	1	0
	W307	oe	16	D	1	1	0

LEGEND F: field
N: node
V: variable
D: default variable
I: intermediate variable
X: extended variable
M: extended node
T: function
U: undefined

Critical Layout Areas

A) **GSP500 VCXO input (pins 48 and 49 of GSP500)**
Keep etches as short as possible. Keep all etches, especially high speed digital, away from circuit area.

B) **GSP500 VCXO loop filter (pin 47 of GSP500)**
Try to keep components near GSP500. Keep all etches, especially high speed digital, away from circuit area.

C) **VCLK dotclock connection (pin 54 of GSP500)**
Keep etch as short as possible. Keep all etches, especially high speed digital, away from connection.

D) **GSP500 VCO loop filter (pin 40 of GSP500)**
Try to keep components near GSP500. Keep all etches, especially high speed digital, away from circuit area.

E) **GSP500 Video input ground connection**
Connect one of the video input jack pins to the ground plane. Connect all VIDREF connections to this point with at least a 20 mil etch. Keep 75 Ohm resistors close to the connectors.

F) **GSP500 Video inputs (pins 32 and 33 of GSP500)**
Try to guard band video inputs to GSP500. Signal etches should be at least 20 mil thick.

G) **Encoder VCXO loop filter (pin 12 of BA7230LS)**
Try to keep components near encoder. Keep all etches, especially high speed digital, away from circuit area.

H) **Luminance delay (pins 16 and 3 of BA7230LS)**
Keep etches as short as possible. Keep all etches, especially high speed digital, away from circuit area.

I) **Encoder VCXO crystal (pins 7 and 8 of BA7230LS)**
Keep etches as short as possible. Keep all etches, especially high speed digital, away from circuit area.

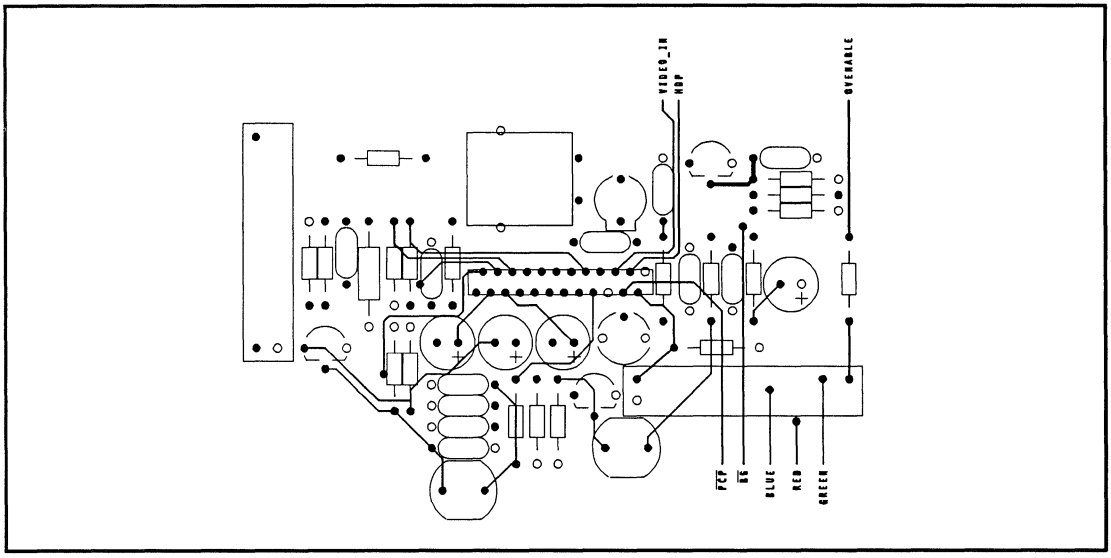
J) **Power supply and loop filter pull-up voltage for GSP500 and encoder (pins 20, 21, 38, 40, and 47 of GSP500, pins 12 and 24 of BA7230LS)**
Regulate all power supply and loop filter voltages.

GSP500 Pin Names

1	VLE	23	FS0	45	YOUT
2	ODD/EVEN	24	FS1	46	HALIGNOUT/
3	FP/	25	FS2	47	SYSLF
4	DATAIN	26	FS3	48	XTALI
5	CB	27	FS4	49	XTALO
6	CS	28	FS5	50	AVSS
7	CKEY	29	EXTSYNC	51	VID1/2
8	TEST	30	SYNCTOL	52	VCOOUT
9	VSYNCOUT	31	CLAMPLEV	53	FILTSEL
10	DATAFRAME	32	Y2	54	DOTCLOCK
11	OVENABLE	33	Y1	55	VFF
12	I/ES	34	C2	56	STILLFRAME
13	L/R OUT	35	C1	57	VGA/NTSC
14	BRSTACT	36	3.58SC	58	BG/
15	FRTSTOUT/	37	FRSTIN	59	L/R IN
16	HS	38	AVDD	60	VGAHSYNC
17	HRSTOUT/	39	GFF	61	VGAVSYNC
18	HSYNCOUT	40	VCOLF	62	HALIGNIN/
19	VSS	41	SYNCTHRS	63	NTSC/SVID
20	VDD	42	VGAO/E	64	VS
21	VDD	43	COUT	65	4XSC
22	VSS	44	RST/	66	PCLK

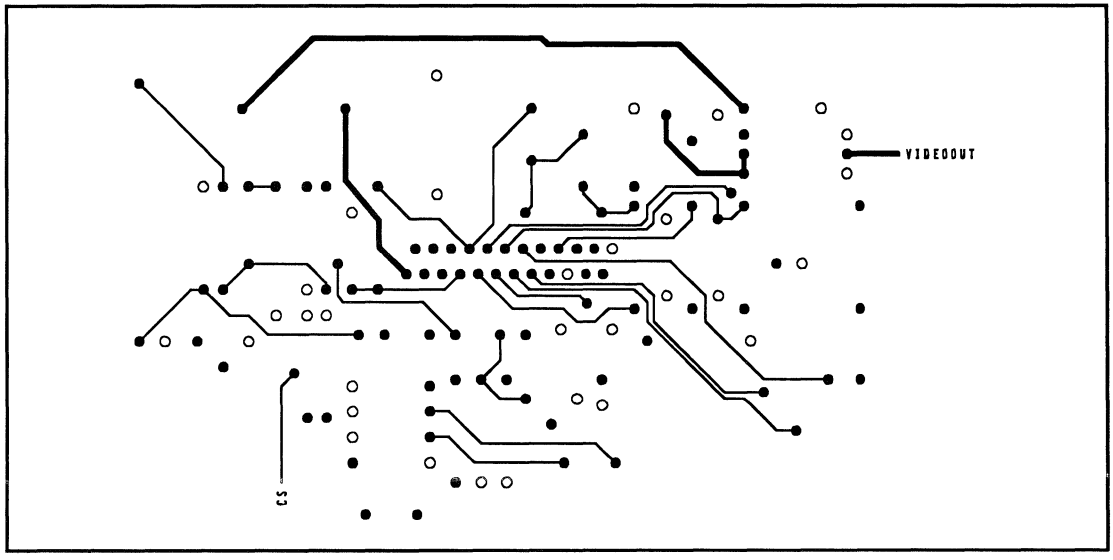
BA7230LS Pin Names

1	VIDEO OUT	13	RED
2	SYNC IN	14	GREEN
3	Y IN	15	BLUE
4	B-Y IN	16	Y OUT
5	R-Y IN	17	B-Y OUT
6	BURST LEVEL ADJ.	18	R-Y OUT
7	VC	19	GND
8	VB	20	VIDEO IN
9	VA	21	PCP IN (FP/)
10	BPF IN (BG/)	22	HDP IN
11	APC PHASE ADJ.	23	YS IN (OVENABLE/)
12	PD	24	VCC



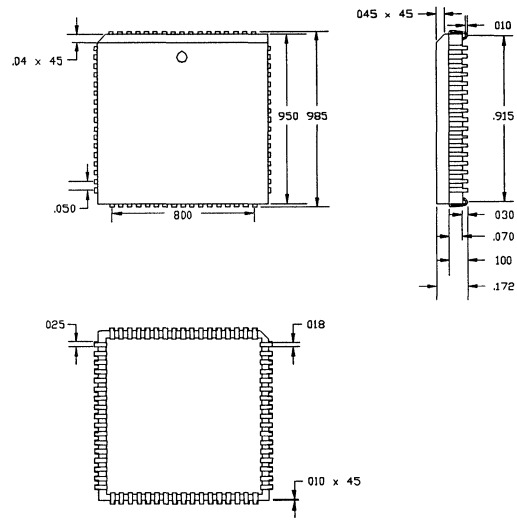
BA7230LS Test Layout

Component Side



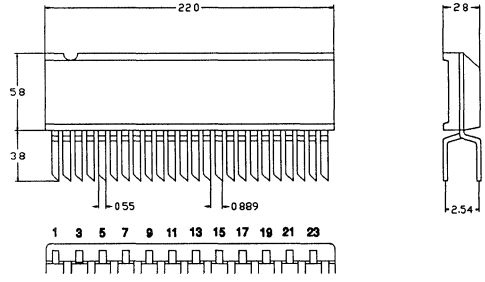
BA7230LS Test Layout

Solder Side



GSP500 Physical Specifications

(All dimensions are in inches)



BA7230LS Physical Specifications

(All dimensions are in millimeters)

Adjustment Features

GSP500

Set the **GSP500** for non-NTSC operation(any VGA mode). Adjust the variable capacitor (between pins 48 and 49 of the **GSP500**) until pin 65 of the **GSP500** reads 14.31818 MHz. If you are unable to adjust it far enough, you may have to increase or decrease the size of the capacitor parallel to the variable capacitor.

BA7230LS

Step 1
Adjust the variable resistor (pin 11 of the BA7230LS) until pin 11 reads 3.9 volts DC.

Step 2
Place GSP500 in genlock mode. Attach a vectorscope to the video output connector. Create a colorbar pattern on the computer screen (available from ICS). Adjust the variable capacitor until the vectorscope displays the proper phase.

Sources for Specialized Components

Encoders:

BA7230LS
ROHM Corporation
USA Headquarters
8 Watney
Irvine CA 92718
(714)855-2131 FAX:(714)855-1669

Delay Lines:

H321LNP-1436PBAB (400nsec)
TOKO America, Inc.
Corporate Headquarters
1250 Feehanville Drive
Mount Prospect, IL 60056
(708)297-0070 FAX:(708)699-7864

Inductors:

RC-875/122J-50 (1.2mH)
Sumida Electric Co., Ltd.
USA Head Office
637 East Golf Road
Suite 209
Arlington Heights, IL 60005
(708)956-0666 FAX:(708)956-0702

B230-52 (22uH)
J.W. Miller
306 E. Alondra Blvd.
Gardena, CA 90247-1059
(213)515-1720 FAX:(213)515-1962

Crystals:

143-20 (14.31818 MHz), 036S (3.579545 MHz)
Fox Electronics
5570 Enterprise Parkway
Fort Myers, FL 33905
(813)693-0099 FAX:(813)693-1554

Phono Connectors:

901
Keystone Manufacturers
31-07 20th Road
Astoria, NY 11105-2017
(718)956-8900 FAX:(718)956-9040

Variable Capacitors:

GKG7R011 (2-5pf)
Sprague/Goodman
134 Fulton Ave.
Garden City Pk, NY 11040
(516)746-1385 FAX:(516)746-1396

Potentiometers:

3321 + R (10K)
Murata-Erie
2200 Lake Park
Smyrna, GA 30080
(404)436-1300 FAX:(404)436-3030

EVM-SOGA01B14 (10K)
Panasonic
Box 511
Secaucus, NJ 07096
(201)348-5266 FAX:(201)392-4782

Distributors:

Digi-Key
701 Brook Ave South
Thief River Falls, MN 56701
(800)344-4539

Theory of Operation for a GSP500 Circuit Operating the VGA display at 2xNTSC Frequency

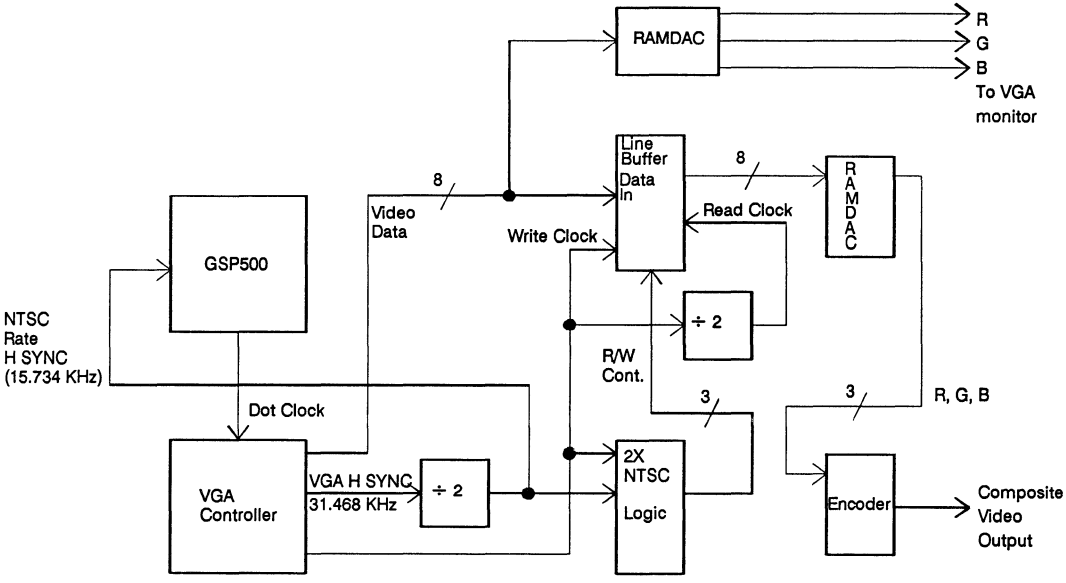
Introduction

In its minimal configuration the GSP500 with a VGA controller chip puts out both RGB to a VGA monitor and composite video in the NTSC format. However, due to the fact that NTSC video is interlaced, the minimal configuration requires that the VGA controller be programmed for interlaced operation; this allows the same RAMDAC to be used for both the VGA and the NTSC outputs (of course the NTSC output also must be encoded). Unfortunately, the VGA picture is somewhat degraded by interlacing - and even worse, some VGA monitors won't lock up to the interlaced signal. If this situation is not acceptable, a solution is available that only requires a few additional parts at minimal cost.

The solution is to run the VGA circuitry at exactly twice the NTSC rate and in a non-interlaced mode. This preserves the full quality of the VGA display while the VGA is still being gen-locked to an external NTSC signal. Of course, now that the VGA RAMDAC is running at a higher speed, another RAMDAC will be required which runs at the NTSC rate. Also, some means will be required to accept the fast data rate VGA output and put out the slower rate NTSC data. Under these circumstances, the VGA circuitry will be producing twice as much data as can be displayed in NTSC and therefore some of it will have to be discarded. All of the VGA lines are used in the NTSC frame, but each line is only used for every other NTSC field. In other words all the odd numbered VGA lines may be output to NTSC field 1 and all the even numbered VGA lines may be output to NTSC field 2 while both odd and even numbered lines are put out to the VGA display in every vertical period. The VGA frame rate is then the same as the NTSC field rate; the NTSC field simply has half as many horizontal lines.

Block Diagram

Application Circuit



One possible implementation of this idea is shown in the accompanying schematic. Only the additional circuitry required for the 2 x NTSC enhancement is shown. Following is a detailed description of the operation of the circuit; please refer to the schematic as you read it.

U5B divides the frequency of the VGA HSync signal VHS by two, producing a 50% duty cycle square wave with a frequency of 15.734 kHz. This signal essentially becomes the Write Enable signal at U4 pin 22 and is also sent to the GSP500 pin 60 as the Horizontal Sync signal. Note that the addition of a divide by 2 in the overall loop which the GSP500 controls forces the VGA chip to clock at twice the rate that it otherwise would, producing a VGA HSync frequency of 31.468 kHz.

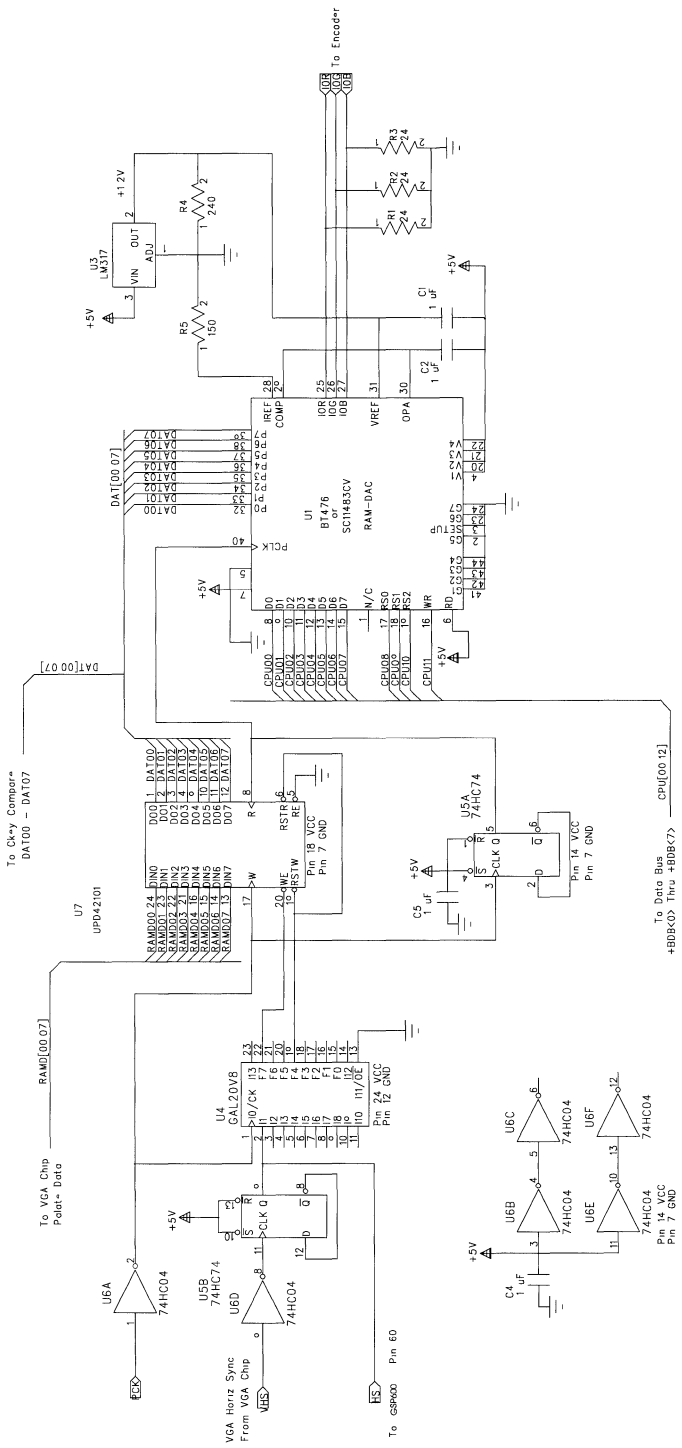
U7 is a line buffer memory which can hold up to 910 pixels with a width of 8 bits; it has individual write and read clocks with associated address pointers. Programmable logic device U4 provides a write enable and pointer reset signals to the line memory. Note that the write clock to U7 (pin 17) is the same rate as the VGA pixel clock; therefore every VGA pixel will be written in to the memory when write enable (pin 20) is active (low). The write enable is only active for every other line, however, since it is frequency divided by 2 from the VGA HSync as previously noted. This essentially discards half the VGA lines each NTSC field, by virtue of the fact that they are not written into memory. The time to write a complete line into memory is 1 VGA line time or 31.778µs. The read clock for U7 is simply the write clock frequency divided by 2 by U5A. Thus to read all the pixels out of the memory will require twice as long as to write them, or 63.557µs. This is the length of an NTSC line. Therefore, over the span of 2 VGA lines, 1 VGA line is written and 1 NTSC line is read, although the writing takes place at twice the NTSC rate.

Data read out from U7 at NTSC rate is fed to RAMDAC U1, which has its control lines paralleled across the main VGA RAMDAC, except that the active low read enable (pin 6) is permanently disabled by tying it to +5V. In this way anything written to the VGA RAMDAC (such as changes to the palette) will also be written to U1, but any reads will not cause a conflict with the main VGA RAMDAC. The analog RGB outputs of U1 are sent to the NTSC encoder to produce a composite video output. U3 provides a reference for the RAMDAC. Instead of a reference for each RAMDAC, it may be possible to use 1 voltage reference for both RAMDACs in the system if they can be configured to use a voltage reference as shown in the schematic.

Further Enhancement

Although the VGA at 2xNTSC enhancement is better than the minimal GSP500 configuration, it is still less than ideal with respect to the NTSC picture quality. It is probably intuitively obvious to most people that throwing away half the VGA data will result in a loss of picture quality on the NTSC output. The practically observed result of this is what is generally known as "flicker", and it should be noted that this problem plagues all scan converters and VGA-to-NTSC boards. It is worst when there is a lot of detail along the vertical axis of the VGA image. The most annoying example is probably a thin, bright white horizontal line made up of a single line on the VGA display. For an example case, imagine that line 100 of the VGA display contains the white line and the rest of the display is black. Then the white line would appear somewhere around line 50 of field 2 in the NTSC output, but not at all on field 1. The result will be a flashing of the line with a period of 33.33 ms (due to 30Hz frame rate). This is visually very noticeable and irritating. Because of this, many scan converters and VGA-to-NTSC boards have a "flicker filter." Interestingly, most flicker filters can be turned off, indicating that they are less than desirable in some situations.

A discussion of flicker filtering and how to implement it with the GSP500 will be the subject of another application note.


To Encoder
+12V
U3
LM317
VIN
OUT
ADJ
R4
240
R5
150
+5V
C1
1 uF
C2
1 uF
R3
24
R2
24
R1
24
U1
BT476
SC11483CV
RAM-DAC
IRF
COMP
IOR
IOG
IOB
VREF
OPA
DAT[00 07]
PCLK
N/C
RS0
RS1
RS2
WR
RD
CPU00
CPU01
CPU02
CPU03
CPU04
CPU05
CPU06
CPU07
CPU08
CPU09
CPU10
CPU11
To Ck+y Compar+
DAT00 - DAT07
U7
UPD42101
RAM[00 07]
RSTR
RSTW
WE
Pin 18 VCC
Pin 7 GND
U5A
74HC74
CPU[00 12]
To Data Bus
+BDB<0> Thru +BDB<7>
C5
1 uF
U4
GAL20V8
I0/CK
I11/OE
Pin 24 VCC
Pin 12 GND
To VGA Chip
Palet+ Data
U6A
74HC04
U5B
74HC74
U6D
74HC04
PCK
VHS
VGA Horiz Sync
From VGA Chip
HS
Pin 60
To GSP400
U6C
74HC04
U6F
74HC04
U6B
74HC04
U6E
74HC04
Pin 14 VCC
Pin 7 GND
C4
1 uF

CRTC Registers

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	HT	35	35	6B	6B	35	35	62	6C	35	62	62	62	62	62	62	62
01	HDE	27	27	4F	4F	27	27	4F	4F	27	4F	4F	4F	4F	4F	04	4F
02	SHB	2A	28	57	57	2A	2A	50	54	2A	50	50	50	50	50	50	50
03	EHB	95	96	8B	8B	96	96	85	8B	96	85	85	85	84	84	85	84
04	SHR	2E	2E	5D	5D	2F	2F	58	5D	2F	58	58	58	54	57	58	57
05	EHR	A0	A0	8C	8C	80	80	9B	83	80	9B	9B	9B	82	82	9B	82
06	VT	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B
07	OVERFLOW	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E
08	PRS	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
09	MSL	4F	4F	4F	4F	C1	C1	C1	4F	C0	C0	40	40	40	40	C0	40

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
0A	CS	0D	0D	0D	0D	00	00	00	0D	00	00	00	00	00	00	00	00
0B	CE	0E	0E	0E	0E	00	00	00	0E	00	00	00	00	00	00	00	00
0C	SAH	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0D	SAL	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0E	CLH	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0F	CLL	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
10	VRS	BE	BE	BE	BE	C5	C5	C5	BE	C5	C5	A7	A7	F4	F4	C5	EF
11	VRE	22	22	22	22	88	88	88	82	88	88	8B	8B	87	87	88	87
12	VDE	8F	8F	8F	8F	8F	8F	8F	8F	8F	8F	5D	5D	DF	DF	8F	DF
13	OFFSET	14	14	28	28	14	14	28	28	14	28	28	28	28	28	28	50
14	UNDERLINE	1F	1F	1F	1F	00	00	00	1F	00	00	0F	0F	00	00	40	60
15	SVB	B8	B8	B8	B8	C2	C2	C2	B8	C2	C2	9F	9F	E0	E0	C2	E0
16	EVB	E3	E3	E3	E3	05	05	05	E3	05	05	CA	CA	0C	0C	05	0C
17	MC	A3	A3	A3	A3	A2	A2	C2	A3	E3	E3	E3	E3	E3	E3	A3	AB
18	LC	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
*	INTERLACE																

* = Interlace Bit must be turned off for all modes

General Register

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	MISC OUT	#	#	#	#	#	#	#	@	#	#	@	#	#	#	#	#

#
23 = GenLock (GL)
27 = OVerlay (OV)
2B = Video Only (VO)
2F = Graphics Only (GO)

@
22 = GenLock (GL)
26 = OVerlay (OV)
2A = Video Only (VO)
2E = Graphics Only (GO)

Sequence Registers

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	CLK MODE	09	09	01	01	09	09	01	00	09	01	01	01	01	01	01	01

** = 640 x 480 x 256 colors

Source Code for PLD U4 (GAL20V8) in CUPL™ Language

```
Name        2ntsc;
Partno      XXXXX;
Date        12/07/92  02:12pm;
Revision    02;
Designer    Todd K. Moyer;
Company     Integrated Circuit Systems;
Assembly    XXXXX;
Location    XXXXX;

/*************************************************************************/
/*                                                                       */
/* VGA @ 2xNTSC rate controller                                          */
/*                                                                       */
/*                                                                       */
/*************************************************************************/
/*                                                                       */
/* Allowable Target Device Types:  g20v8
/*                                                                       */
/*************************************************************************/

/** Inputs **/

Pin 1          =   clock        ;     /* VGA p-clock                     */
Pin 2          =   h_sync_NTSC ;      /*                                 */

Pin 12         =   GND          ;
Pin 13         =   !OE          ;
Pin 24         =   VCC          ;

/** Outputs **/

Pin [15..18]   =   [HSN_S0..3];       /* used by state machine           */
Pin 19         =   !line_start;       /* pointer reset line mem, act lo  */
Pin 20         =   !write_enable_B;   /* not used by 2xNTSC              */
Pin 21         =   !write_enable_A;   /* not used by 2xNTSC              */
Pin 22         =   !write_enable;     /*                                 */

/** Declarations and Intermediate Variable Definitions **/

Field     State_HSync          = [HSN_S0..3];

/** Logic Equations **/
```

```
/** State machine definition **/

Sequence State_HSync
{
        present 0
•••••                   if h_sync_NTSC next 1
                                out line_start out line_startAB
                                out write_enable out write_enable_A;
                        if !h_sync_NTSC next 0
                                out write_enable;
        present 1
                        if h_sync_NTSC next 2
                                out line_start out line_startAB
                                out write_enable out write_enable_A;
                        if !h_sync_NTSC next 0;
        present 2
                        if h_sync_NTSC next 3
                                out line_start out line_startAB
                                out write_enable out write_enable_A;
                        if !h_synch_NTSC next 0;
        present 3
                        if !h_sync_NTSC next 4;
                                /* out write_enable; */
                        if h_sync_NTSC next 3
                                out write_enable_A;
        present 4
                        if !h_sync_NTSC next A;
                        if h_sync_NTSC next 3;
        present A
                        if !h_sync_NTSC next 5;
                        if h_sync_NTSC next 3;
        present 5
                        if h_sync_NTSC next 6
                                out line_start out line_startAB
                                out write_enable out write_enable_B;
                        if !h_sync_NTSC next 5
                                out write_enable;
        present 6
                        if h_sync_NTSC next 7
                                out line_start out line_startAB
                                out write_enable out write_enable_B;
                        if !h_sync_NTSC next 5;
        present 7
                        if h_sync_NTSC next 8
                                out line_start out line_startAB
                                out write_enable out write_enable_B;
                        if !h_sync_NTSC next 5;
        present 8
                        if !h_sync_NTSC next 9;
                                /* out write_enable; */
                        if h_sync_NTSC next 8
                        out write_enable_B;
```

```
        present 9
                        if !h_sync_NTSC next B;
                        if h_sync_NTSC next 8;
        present B
                        if !h_sync_NTSC next 0;
                        if h_sync_NTSC next 8;

        present C
                        next 0;
        present D
                        next 0;
        present E
                        next 0;
        present F
                        next 0;
}
```

Bill of Materials for 2xNTSC

Item	Qty	Part Name	Description	Manufacturer
1	1	74HC04	HEX INVERTER	Motorola
2	1	74HC74	DUAL D FLIP FLOP	Motorola
3	1	SC11483CV	RAM-DAC	Sierra
4	1	GAL20V8	PLD	Lattice
5	1	LM317	Adjustable Regulator	National
6	1	UPD42101	910x8 FIFO	NEC
7	7	CAP	.1µF Cap	
8	1	R1/4W	240 ohm	
9	1	R1/4W	150 ohm	
10	3	R1/4W	24 ohm	

Flicker Reduction Circuit for use with the GSP500

Introduction

Although a minimal configuration GSP500 VGA/NTSC system uses all of the lines of the graphics image to generate the NTSC picture, the resulting NTSC display is not (and cannot be) as good as the original VGA display. Despite the fact that all the lines are used, on the standard non-interlaced VGA display *every* line is used for *every* vertical period of about 16.7 ms, while it takes twice as long to put out all the lines to the NTSC picture (33.33 ms). This is accomplished in practice by one of two ways: 1) interlacing the VGA (slowing it down to NTSC rates), or 2) using odd numbered lines for odd NTSC fields and even numbered lines for even fields, essentially discarding half the lines that are output from the VGA (see the Application Note, AN502: *Theory of Operation for a GSP500 Circuit Operating the VGA Display at 2 x NTSC Frequency*). It is probably intuitively obvious that either slowing the VGA down or throwing away half the VGA data will result in the NTSC output looking less pleasing than the standard VGA display. The practically observed result of this is what is generally known as "flicker", and it should be noted that this problem plagues all scan converters and VGA-to-NTSC boards; it is a fundamental limitation of the NTSC standard. It is worst when there is a lot of detail along the vertical axis of the VGA image. The most annoying example is a thin, bright white horizontal line made up of a single line on the VGA display. For an example case, imagine that line 100 of the VGA display contains the white line and the rest of the display is black. Then the white line would appear somewhere around line 50 of field 2 in the NTSC output, but not at all on field 1. The result will be a flashing of the line with a period of 33.33 ms (reciprocal of the 30 Hz frame rate). This is very noticeable and quite irritating to the eye.

Knowing that displaying a VGA image on an NTSC monitor is at best a compromise, we would at least like to achieve the best possible performance from the conversion. Because of this, most scan converters and VGA-to-NTSC boards have a "flicker filter". It is enlightening to note that most flicker filters can be turned off, indicating that they are less than desirable in some situations. In fact they reduce the spatial "bandwidth" in the vertical direction, or in other words reduce the vertical resolution. A particularly simple and effective flicker reduction scheme (which can be implemented in software) is to repeat every other VGA line in both fields of the NTSC signal. This method, however, requires that half the VGA lines never get to the NTSC display; in other words the vertical resolution is cut in half.

A single horizontal line in the VGA image has only a 50/50 chance of being displayed in NTSC, depending on which line number it appears on. Obviously, this method leaves a lot to be desired, since some details in the VGA image can be completely absent from the NTSC signal; most people would judge it unacceptable.

You can get a feel for how a better typical flicker filter works by thinking about the example above of a single white horizontal line on scan line 50 of field 2. Imagine "spreading" the line so that some of it spills into the scan lines adjacent to the original line. In an interlaced system such as NTSC this means reducing the brightness of line 50 of field 2 (thereby making it gray), and putting some darker shade of gray into lines 50 and 51 of field 1, which are above and below line 50 of field 2, respectively, once the complete frame has been scanned. If done properly, in the right proportions, and viewed from a sufficient distance, the new wide line looks to be of the same brightness as the original single white line. This can significantly reduce the flicker, since there is no longer the situation of black on field 1 and white on field 2 rapidly alternating. However, as you can imagine, any rapid vertical transitions would also become smeared or blurred with such a scheme. The typical complaint is that when trying to display text on an NTSC display, a flicker filter will make the text less readable (if it remains readable at all). This type of flicker reduction works best if only the luminance portion of the signal is filtered, since the mixing of several VGA lines to make one NTSC line can significantly change the saturation and hue of the color displayed, seriously altering the picture when compared with the VGA display. It is primarily changes in luminance level that cause flicker, so that leaving the chrominance portion of the signal unchanged does not seriously degrade the flicker reduction that is achieved, while it does tend to preserve the look of the image.

To boil all this down, there is a trade-off between flicker reduction and vertical resolution, and it bears repeating that it is a practical impossibility to make an NTSC image look just as good as a high resolution VGA image. To try and work around this trade-off, some sophisticated flicker filters are "adaptive", which essentially means that they will dynamically turn themselves on when especially needed to reduce flicker and off when the loss of vertical resolution is especially detrimental. Predictably, this approach is rather expensive and takes up a lot of circuit board space, at least until the time when this function is incorporated into a monolithic integrated circuit. At any rate, a flicker filter of the more basic variety is presented here for use with GSP500 applications.

Application Circuit

In the accompanying schematic and block diagram an implementation of a simple luminance-only flicker filter which works with the **GSP500** in a VGA-to-NTSC system is shown. The schematic details only the portion of the system specific to the flicker filter function, since the VGA portion will vary depending on the VGA chip used. Please refer to the schematic when reading the following detailed circuit description.

U8B divides the frequency of the **VGA_HSYNC** signal **VHS** by two, producing a 50% duty cycle square wave with a frequency of 15.734 kHz. This signal essentially becomes the Write Enable signal at U5 pin 22 and is also sent to the GSP500 pin 60 as the Horizontal Sync signal **NTSC_RATE_HS**. Note that the addition of a divide by 2 in the overall loop which the GSP500 controls forces the VGA chip to clock at twice the rate that it otherwise would, producing a VGA HSync frequency of 31.468 kHz.

U2 is a line buffer memory which can hold up to 910 pixels with a width of 8 bits; it has individual write and read clocks with associated address pointers. Programmable logic device **U5** provides a write enable and pointer reset signals to the line memory. Note that the write clock to U2 (pin 17) is the same rate as the VGA pixel clock; therefore every VGA pixel will be written in to the memory when write enable (pin 20) is active (low). The write enable is only active for every other line, however, since it is frequency divided by 2 from the VGA HSync as previously noted. This essentially discards half the VGA lines each NTSC field, by virtue of the fact that they are not written into memory. The time to write a complete line into memory is 1 VGA line time or **31.778**µs. The read clock for U2 is simply the write clock frequency divided by 2 by U8A. Thus, to read all the pixels out of the memory will require twice as long as to write them, or **63.557**µs. This is the length of an NTSC line. Therefore, over the span of 2 VGA lines, 1 VGA line is written and 1 NTSC line is read, although the writing takes place at twice the rate.

Data read out from U2 at NTSC rate is fed to RAMDAC U9, which has its control lines paralleled across the main VGA RAMDAC, except that the active low read enable (pin 6) is permanently disabled by tying it to + 5V. In this way anything written to the VGA RAMDAC (such as changes to the palette) will also be written to U9, but any reads will not cause a conflict with the main VGA RAMDAC. The analog RGB outputs of U9 are sent to the NTSC encoder to produce the chrominance component of the composite video output. U6 provides the required voltage reference to U9. Also, the RGB outputs from U9 are combined by resistor matrix in the right proportions to create a luminance signal which can be summed with the adjacent lines' luminance signals, thereby spatially lowpass filtering the luminance signal in the vertical dimension.

Up to this point the circuitry described is basically the same as is required to make the VGA run at 2 x NTSC rates (see the Application Note AN502: *Theory of Operation for a GSP500 Circuit Operating the VGA Display at 2 x NTSC Frequency*). Note that there are an additional 2 line buffers (U3 and U4), 2 RAMDACs (U10 and U1), and 2 current references (U7A, Q1, and Q2). The additional 2 line buffers store the VGA lines before and after the current line being output via U2 and U9. The RGB current outputs from the RAMDACs U10 and U1 are connected together, summing the two sets of RGB currents together. The combined RGB signals from U10 and U1 are then matrixed together in the proper proportions to produce an adjacent-lines luminance signal. This signal amplitude is independent of the main luminance signal so that the ratio of adjacent line to main line luminance can be set to any desired value, primarily by adjusting R1, which controls the reference currents into U10 and U1.

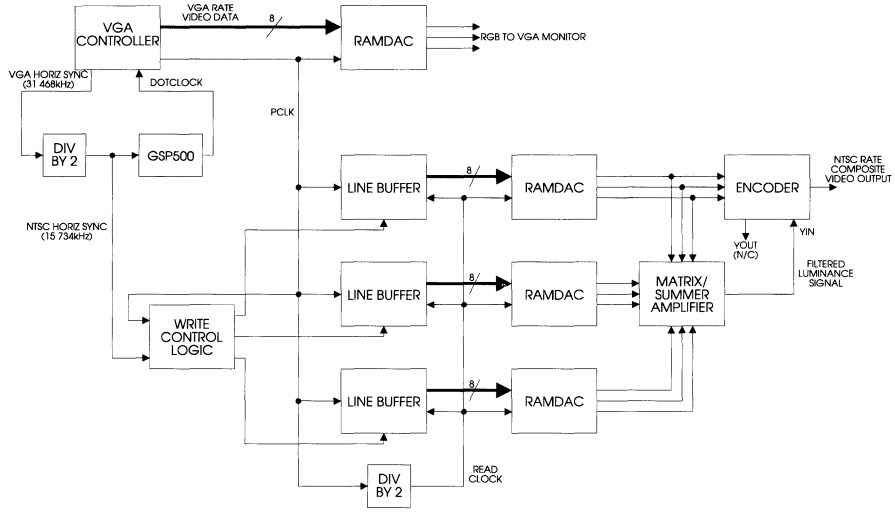


Figure 1

The two luminance signals are connected together, summing them at the input to amplifier U11. U11 then makes up for the resistive losses in the RGB matrices and drives the luminance delay line, whose output is the luminance component of the encoded composite signal. Most encoders have a luminance output and input which allows for an external delay line; not using the output provided while driving the input with an alternate luminance signal of the right amplitude, delay, and polarity allows convenient summing with the chrominance signal generated by the encoder to create the composite video signal.

Programmable logic chip U5 controls the writing of VGA lines into the line buffers such that U2 receives every other line, U3 receives every fourth line, and U4 receives every fourth line, as shown by the timing diagram in Figure 2. Note that only one line buffer is write enabled at a time and every line is written to a line buffer. With this scheme U2 always contains the main VGA line which is going out to the NTSC encoder, while U3 and U4 contain the lines adjacent to the main line. The CUPL™ language source code for PLD U5 is included later in this note.

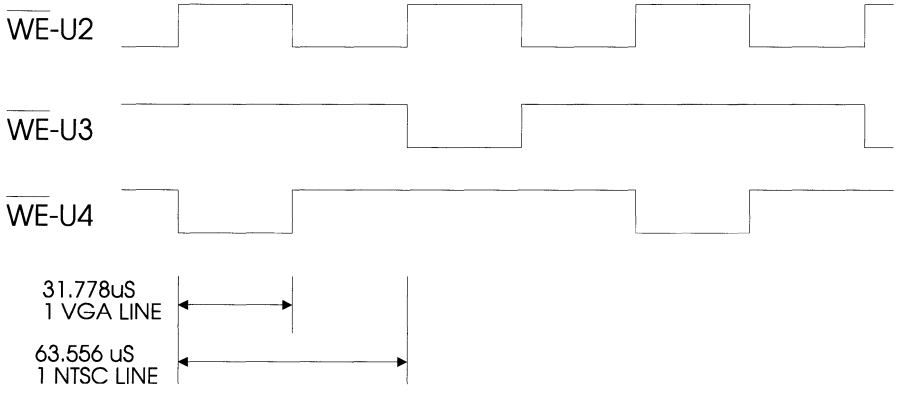


Figure 2

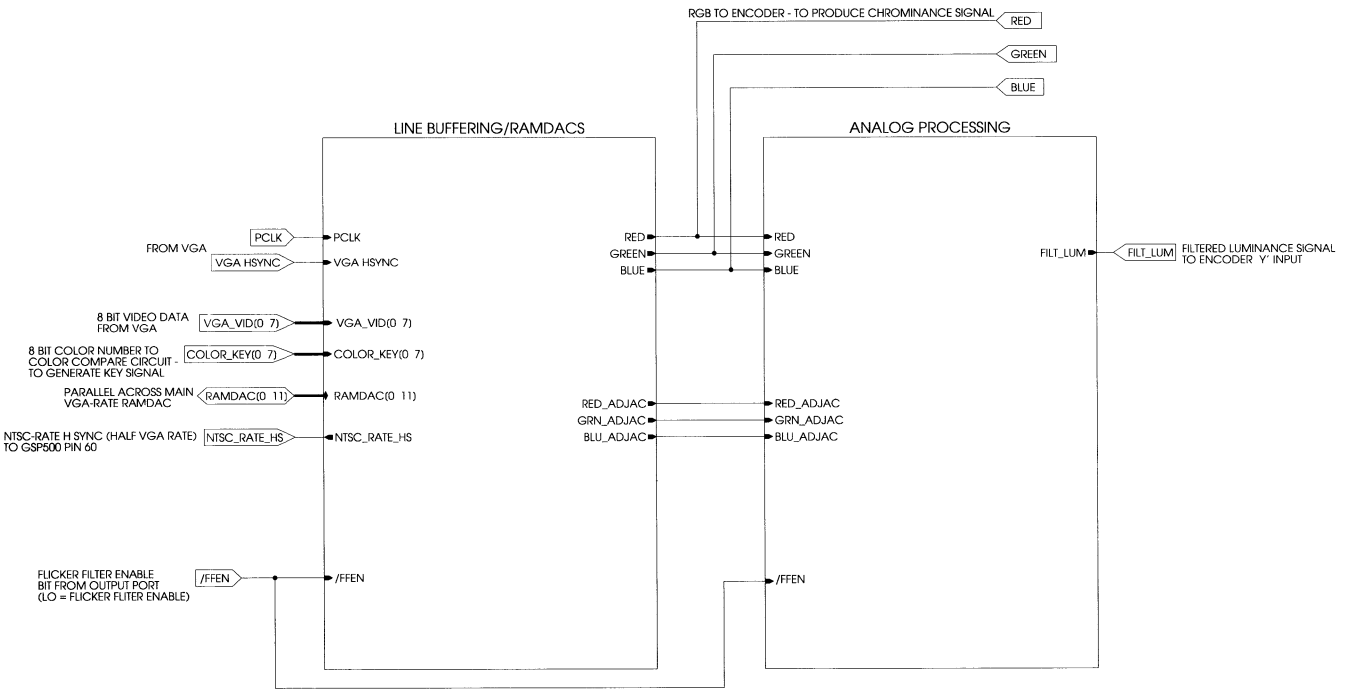
All of the line buffers are continuously read enabled, such that the RGB signal output to the encoder is a combination of the main line and the 2 adjacent line signals. U7A, Q1, and Q2 make up a dual matched current reference for RAMDACs U10 and U1. The amplitude of the adjacent line video signals summed in with the main line is adjustable with R1; the optimum value could be determined so that R1 could be replaced with a fixed divider to save the cost of the trimmer. The amplitude of the main line video signal is controllable by the value of R6 if it is necessary to adjust the proportion of the main line signal that gets summed into the final output. The relative weight of the 2 adjacent line signals in the output is the same due to the matching of the current references into U10 and U1; this should be best for most applications since it is symmetrical about the main line.

The luminance amplitude is controllable by varying the gain of U11 (set by the value of R22); this should normally be set so that luminance levels on any given line are somewhat lower than they would be without filtering. An optional feature shown in the schematic is the ability to switch off the flicker filtering with an I/O bit. Switches Q3 and Q4 turn on when the filter is disabled. In this state Q3 cuts the reference current into U10 and U1, thereby turning off the adjacent line luminance; while Q4 boosts the gain of U11 (by an amount set by R23) to what it should normally be without flicker reduction.

Since when a large area of high luminance level occurs, the video output could exceed the maximum allowed voltage, Q5 and Q6 are used as a positive luminance peak clipper. R27 can be set so that the peak luminance level at the final video output is 714 mV.

BIOS

The video BIOS for the circuit presented here will have to be modified from the typical GSP500 VGA/NTSC system; therefore, register setups for various video modes are given in several tables later in this note.



Flicker Filter Circuit for GSP500

Figure 3 - Flicker Filter Top Level Schematic

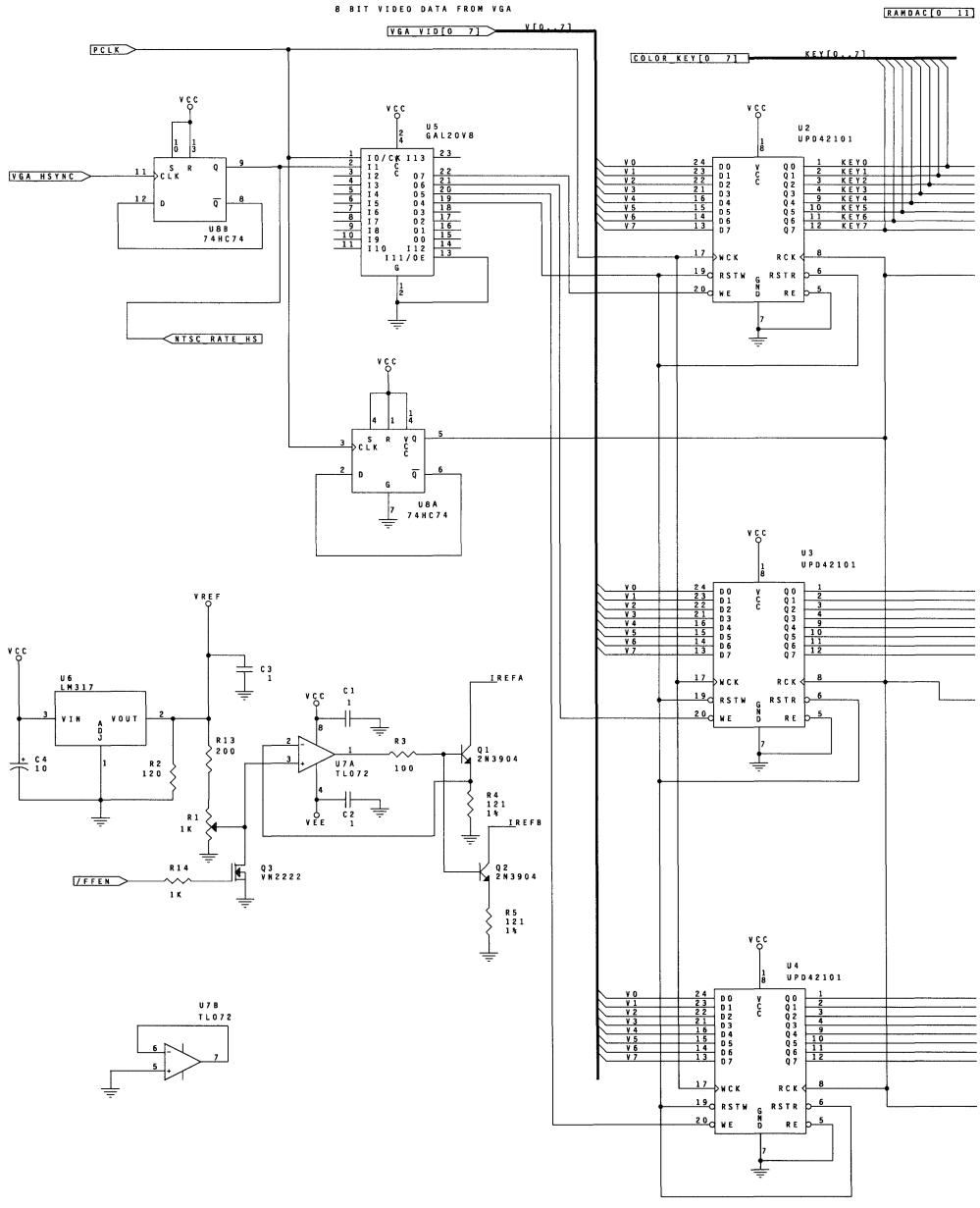
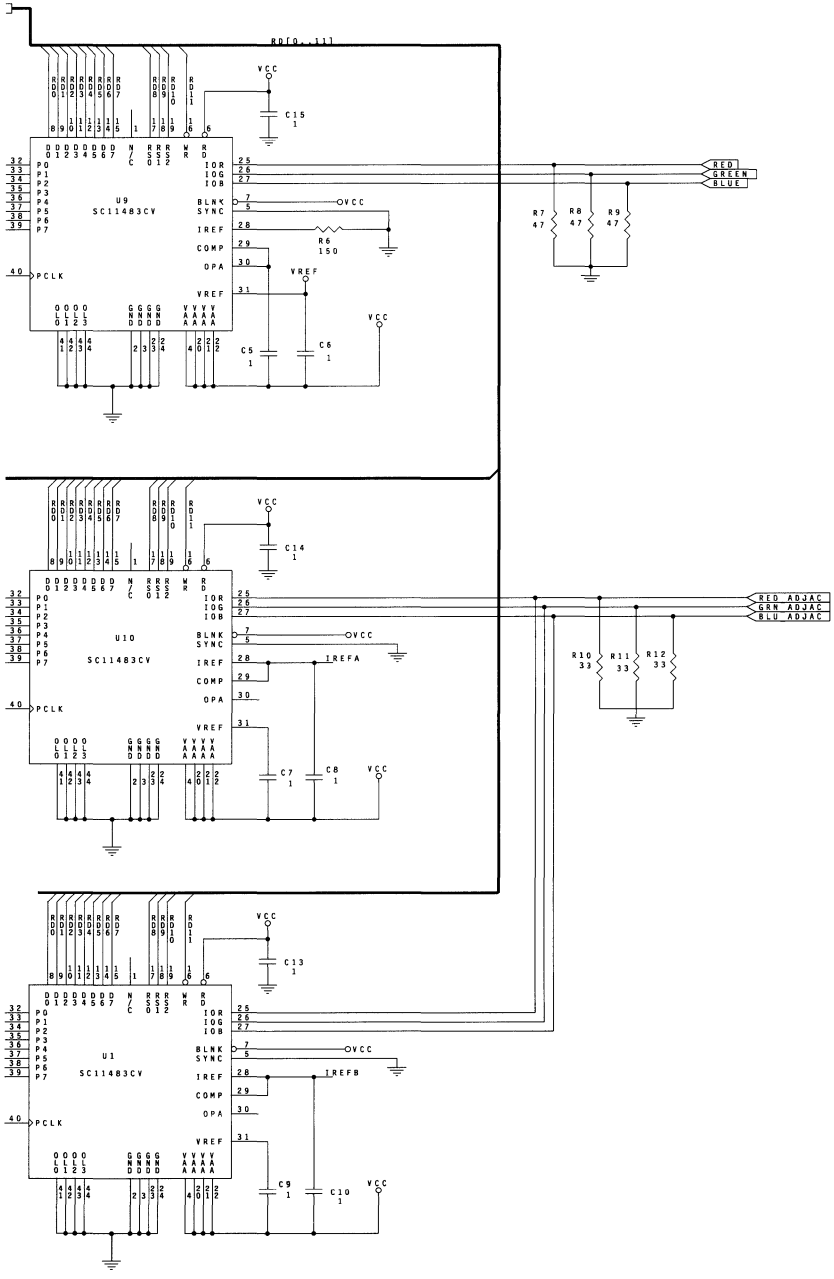

8 BIT VIDEO DATA FROM VGA
VGA VID[0 7]
V[0..7]
RAMDAC[0 11]
PCLK
COLOR KEY[0 7]
KEY[0..7]
VGA HSYNC
NTSC RATE HS
U5
GAL20V8
U2
UPD42101
U3
UPD42101
U4
UPD42101
U8B
74HC74
U8A
74HC74
U6
LM317
U7A
TL072
U7B
TL072
Q1
2N3904
Q2
2N3904
Q3
VN2222
/FFEN
IREFA
IREFB
VREF
R1
1K
R2
120
R3
100
R4
121
1%
R5
121
1%
R13
200
R14
1K
C1
C2
C3
C4
10
VCC
VEE
WCK
RCK
RSTW
RSTR
WE
RE

Figure 4 -



Flicker Filter Line Buffering/Ramdacs

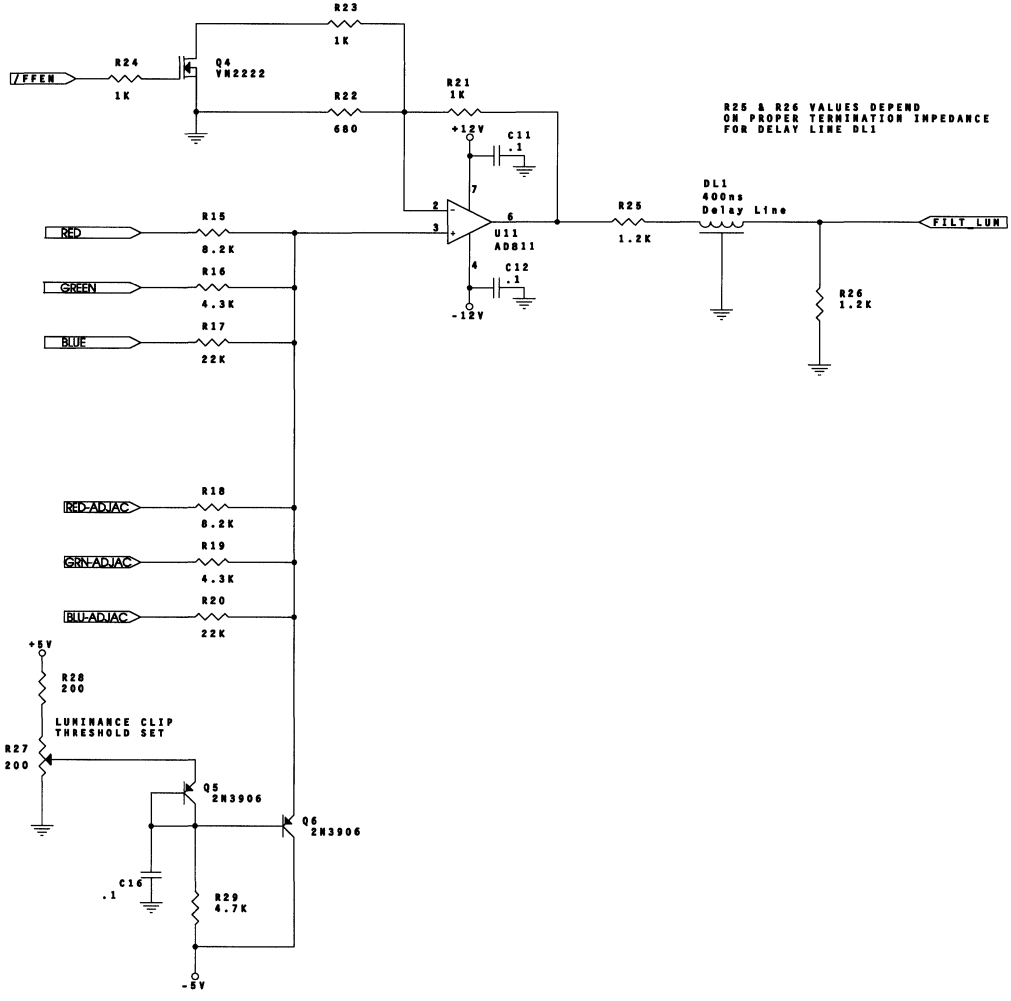


Figure 5 - Flicker Filter Analog Processing

CRTC Registers

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	HT	35	35	6B	6B	35	35	62	6C	35	62	62	62	62	62	62	62
01	HDE	27	27	4F	4F	27	27	4F	4F	27	4F	4F	4F	4F	4F	04	4F
02	SHB	2A	28	57	57	2A	2A	50	54	2A	50	50	50	50	50	50	50
03	EHB	95	96	8B	8B	96	96	85	8B	96	85	85	85	84	84	85	84
04	SHR	2E	2E	5D	5D	2F	2F	58	5D	2F	58	58	58	54	57	58	57
05	EHR	A0	A0	8C	8C	80	80	9B	83	80	9B	9B	9B	82	82	9B	82
06	VT	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B
07	OVERFLOW	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E
08	PRS	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
09	MSL	4F	4F	4F	4F	C1	C1	C1	4F	C0	C0	40	40	40	40	C0	40

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
0A	CS	0D	0D	0D	0D	00	00	00	0D	00	00	00	00	00	00	00	00
0B	CE	0E	0E	0E	0E	00	00	00	0E	00	00	00	00	00	00	00	00
0C	SAH	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0D	SAL	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0E	CLH	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0F	CLL	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
10	VRS	BE	BE	BE	BE	C5	C5	C5	BE	C5	C5	A7	A7	F4	F4	C5	EF
11	VRE	22	22	22	22	88	88	88	82	88	88	8B	8B	87	87	88	87
12	VDE	8F	8F	8F	8F	8F	8F	8F	8F	8F	8F	5D	5D	DF	DF	8F	DF
13	OFFSET	14	14	28	28	14	14	28	28	14	28	28	28	28	28	28	50
14	UNDERLINE	1F	1F	1F	1F	00	00	00	1F	00	00	0F	0F	00	00	40	60
15	SVB	B8	B8	B8	B8	C2	C2	C2	B8	C2	C2	9F	9F	E0	E0	C2	E0
16	EVB	E3	E3	E3	E3	05	05	05	E3	05	05	CA	CA	0C	0C	05	0C
17	MC	A3	A3	A3	A3	A2	A2	C2	A3	E3	E3	E3	E3	E3	E3	A3	AB
18	LC	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
*	INTERLACE																

* = Interlace Bit must be turned off for all modes

General Register

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	MISC OUT	#	#	#	#	#	#	#	@	#	#	@	#	#	#	#	#

#	@
23 = GenLock (GL)	22 = GenLock (GL)
27 = OVerlay (OV)	26 = OVerlay (OV)
2B = Video Only (VO)	2A = Video Only (VO)
2F = Graphics Only (GO)	2E = Graphics Only (GO)

Sequence Registers

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	CLK MODE	09	09	01	01	09	09	01	00	09	01	01	01	01	01	01	01

** = 640 x 480 x 256 colors

Source Code for PLD U5 (GAL20V8) in CUPL™ Language

```
Name        ff;
Partno      ff01;
Date        1/20/93;
Revision    01;
Designer    Todd K. Moyer;
Company     Integrated Circuit Systems;
Assembly    Flicker Filter;
Location    U5;

/*************************************************************************/
/*                                                                       */
/* VGA @ 2xNTSC rate controller with basic line flicker filtering        */
/*                                                                       */
/*                                                                       */
/*************************************************************************/
/*                                                                       */
/* Allowable Target Device Types:  g20v8                                 */
/*                                                                       */
/*************************************************************************/

/** Inputs **/

Pin 1          =   clock       ;    /* VGA PCLK signal                   */
Pin 2          =   h_sync_NTSC ;    /*                                   */
Pin 12         =   GND         ;
Pin 13         =   !OE         ;
Pin 24         =   VCC         ;

/** Outputs **/

Pin [15..18]   =   [HSN_S0..3];     /* used by state machine             */
Pin 19         =   !line_start;     /* pointer reset line mem, act lo    */

Pin 20         =   !write_enable_B; /*                                   */
Pin 21         =   !write_enable_A; /*                                   */
Pin 22         =   !write_enable;   /*                                   */

/** Declarations and Intermediate Variable Definitions **/

Field    State_HSync        =  [HSN_S0..3];

/** Logic Equations **/
```

```
/** State machine definition **/

Sequence State_HSync
{
        present 0
                if h_sync_NTSC next 1
                        out line_start out line_startAB
                        out write_enable out write_enable_A;
                if !h_sync_NTSC next 0
                        out write_enable;
        present 1
                if h_sync_NTSC next 2
                        out line_start out line_startAB
                        out write_enable out write_enable_A;
                if !h_sync_NTSC next 0;
        present 2
                if h_sync_NTSC next 3
                        out line_start out line_startAB
                        out write_enable out write_enable_A;
                if !h_synch_NTSC next 0;
        present 3
                if !h_sync_NTSC next 4;
                        /* out write_enable; */
                if h_sync_NTSC next 3
                        out write_enable_A;
        present 4
                if !h_sync_NTSC next A;
                if h_sync_NTSC next 3;
        present A
                if !h_sync_NTSC next 5;
                if h_sync_NTSC next 3;
        present 5
                if h_sync_NTSC next 6
                        out line_start out line_startAB
                        out write_enable out write_enable_B;
                if !h_sync_NTSC next 5
                        out write_enable;
        present 6
                if h_sync_NTSC next 7
                        out line_start out line_startAB
                        out write_enable out write_enable_B;
                if !h_sync_NTSC next 5;
        present 7
                if h_sync_NTSC next 8
                        out line_start out line_startAB
                        out write_enable out write_enable_B;
                if !h_sync_NTSC next 5;
        present 8
                if !h_sync_NTSC next 9;
                        /* out write_enable; */
                if h_sync_NTSC next 8
                out write_enable_B;
```

```
        present 9
                        if !h_sync_NTSC next B;
                        if h_sync_NTSC next 8;
        present B
                        if !h_sync_NTSC next 0;
                        if h_sync_NTSC next 8;

        present C
                        next 0;
        present D
                        next 0;
        present E
                        next 0;
        present F
                        next 0;
}
```

Bill of Materials

Item	Qty	Reference	Part
1	15	C1, C2, C3, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16	.1µF
2	1	C4	10µF
3	1	DL1	400 ns
4	2	Q1, Q2	2N3904
5	2	Q3, Q4	VN2222
6	2	Q5, Q6	2N3906
7	5	R1, R14, R21, R23, R24	1K
8	1	R2	120
9	1	R3	100
10	2	R4, R5	121
11	1	R6	150
12	3	R7, R8, R9	47
13	3	R10, R11, R12	33
14	3	R13, R27, R28	200

Item	Qty	Reference	Part
15	2	R15, R18	8.2K
16	2	R16, R19	4.3K
17	2	R17, R20	22K
18	1	R22	680
19	2	R25, R26	1.2K
20	1	R29	4.7K
21	3	U1, U9, U10	SC11483CV
22	3	U2, U3, U4	UPD42101
23	1	U5	GAL20V8
24	1	U6	LM317
25	1	U7	TL072
26	1	U8	74HC74
27	1	U11	AD811

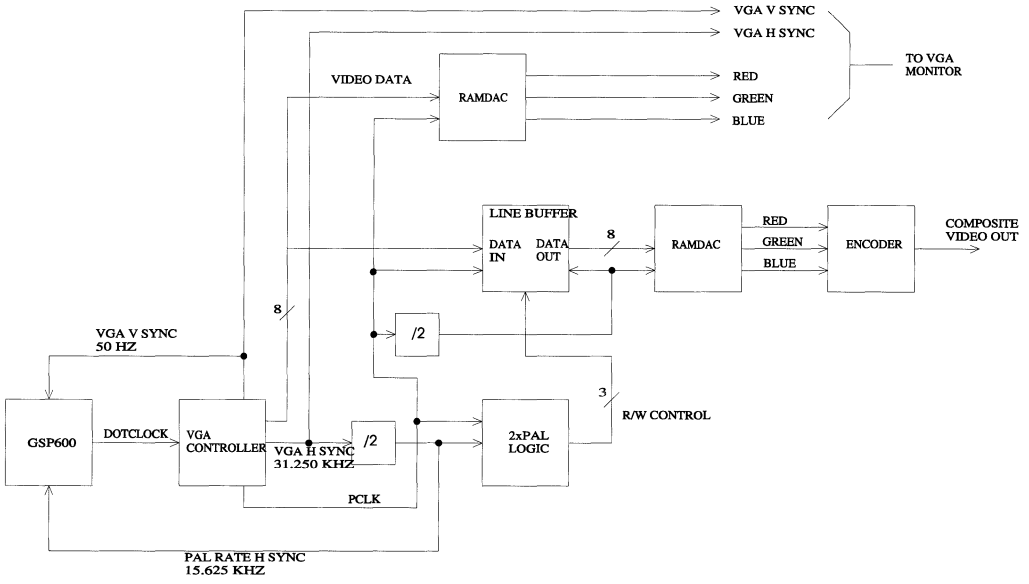
Theory of Operation for a GSP600 Circuit Operating the VGA Display at 2xPAL Frequency

Introduction

In its minimal configuration the **GSP600** with a VGA controller chip puts out both RGB to a VGA monitor and composite video in the PAL format. However, due to the fact that PAL video is interlaced, the minimal configuration requires that the VGA controller be programmed for interlaced operation; this allows the same RAMDAC™ to be used for both the VGA and the PAL outputs (of course the PAL output also must be encoded). Unfortunately, the VGA picture is somewhat degraded by interlacing - and even worse, some VGA monitors won't lock up to the interlaced signal. If this situation is not acceptable, a solution is available that only requires a few additional parts at minimal cost.

The solution is to run the VGA circuitry at exactly twice the PAL rate and in a non-interlaced mode. This preserves the full quality of the VGA display while the VGA is still being gen-locked to an external PAL signal. Of course, now that the VGA RAMDAC is running at a higher speed, another RAMDAC will be required which runs at the PAL rate. Also, some means will be required to accept the fast data rate VGA output and put out the slower rate PAL data. Under these circumstances, the VGA circuitry will be producing twice as much data as can be displayed in PAL and therefore some of it will have to be discarded. All of the VGA lines are used in the PAL frame, but each line is only used for every other PAL field. In other words all the odd numbered VGA lines may be output to PAL field 1 and all the even numbered VGA lines may be output to PAL field 2 while both odd and even numbered lines are put out to the VGA display in every vertical period. The VGA frame rate is then the same as the PAL field rate; the PAL field simply has half as many horizontal lines.

Block Diagram



RAMDAC is a trademark of Brooktree Corporation

Application Circuit

One possible implementation of this idea is shown in the accompanying schematic. Only the additional circuitry required for the 2xPAL enhancement is shown. Following is a detailed description of the operation of the circuit; please refer to the schematic as you read it.

U5B divides the frequency of the VGA HSync signal VHS by two, producing a 50% duty cycle square wave with a frequency of 15.625 kHz. This signal essentially becomes the Write Enable signal at U4 pin 22 and is also sent to the **GSP600** pin 60 as the Horizontal Sync signal. Note that the addition of a divide by 2 in the overall loop which the **GSP600** controls forces the VGA chip to clock at twice the rate that it otherwise would, producing a VGA HSync frequency of 31.650 kHz.

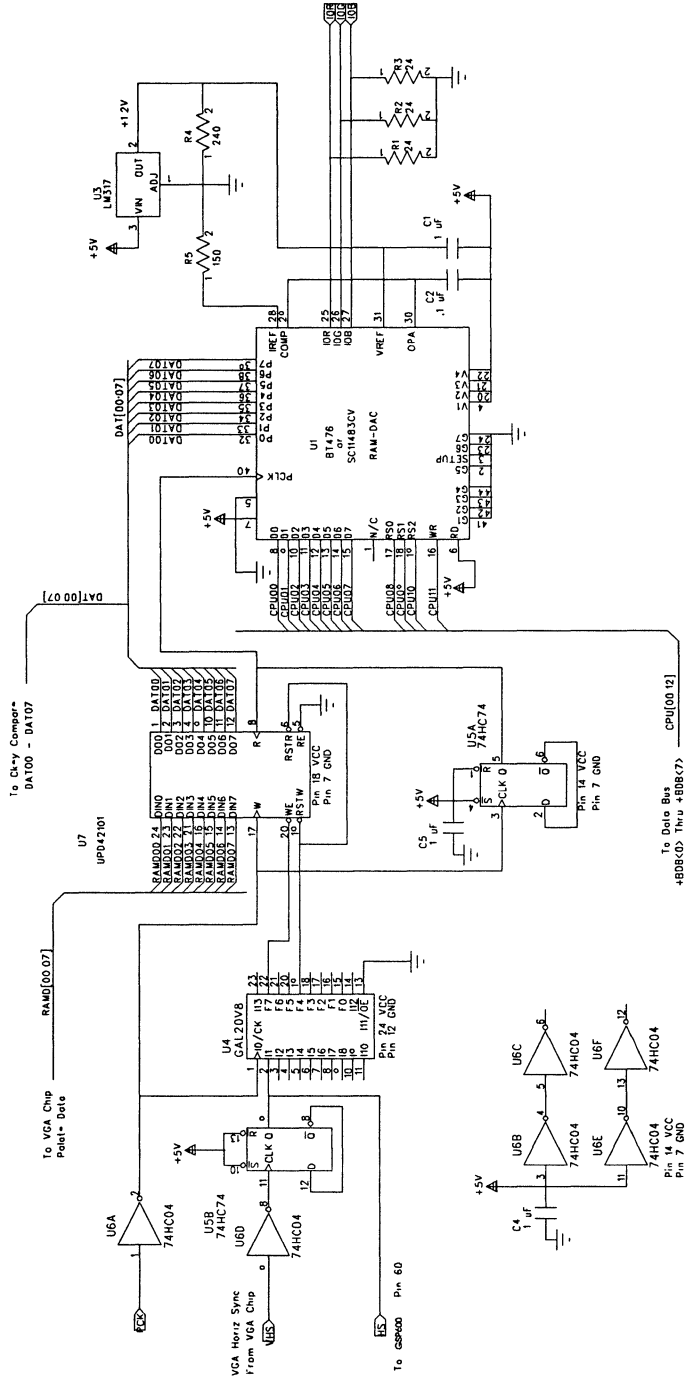
U7 is a line buffer memory which can hold up to 910 pixels with a width of 8 bits; it has individual write and read clocks with associated address pointers. Programmable logic device U4 provides a write enable and pointer reset signals to the line memory. Note that the write clock to U7 (pin 17) is the same rate as the VGA pixel clock; therefore every VGA pixel will be written in to the memory when write enable (pin 20) is active (low). The write enable is only active for every other line, however, since it is frequency divided by 2 from the VGA HSync as previously noted. This essentially discards half the VGA lines each PAL field, by virtue of the fact that they are not written into memory. The time to write a complete line into memory is 1 VGA line time or 32.0µs. The read clock for U7 is simply the write clock frequency divided by 2 by U5A. Thus to read all the pixels out of the memory will require twice as long as to write them, or 64.0µs. This is the length of a PAL line. Therefore, over the span of 2 VGA lines, 1 VGA line is written and 1 PAL line is read, although the writing takes place at twice the PAL rate.

Data read out from U7 at PAL rate is fed to RAMDAC U1, which has its control lines paralleled across the main VGA RAMDAC, except that the active low read enable (pin 6) is permanently disabled by tying it to + 5V. In this way anything written to the VGA RAMDAC (such as changes to the palette) will also be written to U1, but any reads will not cause a conflict with the main VGA RAMDAC. The analog RGB outputs of U1 are sent to the PAL encoder to produce a composite video output. U3 provides a reference for the RAMDAC. Instead of a reference for each RAMDAC, it may be possible to use 1 voltage reference for both RAMDACs in the system if they can be configured to use a voltage reference as shown in the schematic.

Further Enhancement

Although the VGA at 2xPAL enhancement is better than the minimal **GSP600** configuration, it is still less than ideal with respect to the PAL picture quality. It is probably intuitively obvious to most people that throwing away half the VGA data will result in a loss of picture quality on the PAL output. The practically observed result of this is what is generally known as "flicker", and it should be noted that this problem plagues all scan converters and VGA-to-PAL boards. It is worst when there is a lot of detail along the vertical axis of the VGA image. The most annoying example is probably a thin, bright white horizontal line made up of a single line on the VGA display. For an example case, imagine that line 100 of the VGA display contains the white line and the rest of the display is black. Then the white line would appear somewhere around line 50 of field 2 in the PAL output, but not at all on field 1. The result will be a flashing of the line with a period of 40.0 ms (due to 25Hz frame rate). This is visually very noticeable and irritating. Because of this, many scan converters and VGA-to-PAL boards have a "flicker filter." Interestingly, most flicker filters can be turned off, indicating that they are less than desirable in some situations.

A discussion of flicker filtering and how to implement it with the **GSP600** is the subject of Application Note AN603.


To Encoder
+12V
U3
LM317
VIN
OUT
ADJ
R4
240
R5
150
+5V
R3
R2
R1
C1
1 uF
C2
.1 uF
U1
BT476
or
SC11483CV
RAM-DAC
IREF
COMP
IOR
IOG
IOB
VREF
OPA
PCLK
M/C
PS0
PS1
PS2
WR
RD
DAT[00:07]
To Ck+y Compar+
DAT00 - DAT07
U7
UPD42101
DIN0
DIN1
DIN2
DIN3
DIN4
DIN5
DIN6
DIN7
DOUT
RSTRE
RSTIW
WE
Pin 18 VCC
Pin 7 GND
U5A
74HC74
CLK 0
Pin 14 VCC
Pin 7 GND
To Data Bus
+BDB<0> Thru +BDB<7>
CPU[00:12]
RAM0[00:07]
To VGA Chip
Polat+ Data
U4
CAL20V8
I0/CK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11/OE
F7
F6
F5
F4
F3
F2
F1
F0
I12
Pin 24 VCC
Pin 12 GND
U6A
74HC04
U5B
74HC74
U6D
74HC04
U6C
U6B
U6F
U6E
C4
1 uF
C5
1 uF
VGA Horiz Sync
From VGA Chip
To GSP400 Pin 60

CRTC Registers

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	HT	35	35	6B	6B	35	35	62	6C	35	62	62	62	62	62	62	62
01	HDE	27	27	4F	4F	27	27	4F	4F	27	4F	4F	4F	4F	4F	04	4F
02	SHB	2A	28	57	57	2A	2A	50	54	2A	50	50	50	50	50	50	50
03	EHB	95	96	8B	8B	96	96	85	8B	96	85	85	85	84	84	85	84
04	SHR	2E	2E	5D	5D	2F	2F	58	5D	2F	58	58	58	54	57	58	57
05	EHR	A0	A0	8C	8C	80	80	9B	83	80	9B	9B	9B	82	82	9B	82
06	VT	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B
07	OVERFLOW	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E
08	PRS	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
09	MSL	4F	4F	4F	4F	C1	C1	C1	4F	C0	C0	40	40	40	40	C0	40

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
0A	CS	0D	0D	0D	0D	00	00	00	0D	00	00	00	00	00	00	00	00
0B	CE	0E	0E	0E	0E	00	00	00	0E	00	00	00	00	00	00	00	00
0C	SAH	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0D	SAL	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0E	CLH	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0F	CLL	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
10	VRS	BE	BE	BE	BE	C5	C5	C5	BE	C5	C5	A7	A7	F4	F4	C5	EF
11	VRE	22	22	22	22	88	88	88	82	88	88	8B	8B	87	87	88	87
12	VDE	8F	8F	8F	8F	8F	8F	8F	8F	8F	8F	5D	5D	DF	DF	8F	DF
13	OFFSET	14	14	28	28	14	14	28	28	14	28	28	28	28	28	28	50
14	UNDERLINE	1F	1F	1F	1F	00	00	00	1F	00	00	0F	0F	00	00	40	60
15	SVB	B8	B8	B8	B8	C2	C2	C2	B8	C2	C2	9F	9F	E0	E0	C2	E0
16	EVB	E3	E3	E3	E3	05	05	05	E3	05	05	CA	CA	0C	0C	05	0C
17	MC	A3	A3	A3	A3	A2	A2	C2	A3	E3	E3	E3	E3	E3	E3	A3	AB
18	LC	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
*	INTERLACE																

* = Interlace Bit must be turned off for all modes

General Register

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	MISC OUT	#	#	#	#	#	#	#	@	#	#	@	#	#	#	#	#

#	@
23 = GenLock (GL)	22 = GenLock (GL)
27 = OVerlay (OV)	26 = OVerlay (OV)
2B = Video Only (VO)	2A = Video Only (VO)
2F = Graphics Only (GO)	2E = Graphics Only (GO)

Sequence Registers

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	CLK MODE	09	09	01	01	09	09	01	00	09	01	01	01	01	01	01	01

** = 640 x 480 x 256 colors

Source Code for PLD U4 (GAL20V8) in CUPL™ Language

```
Name        2PAL;
Partno      XXXXX;
Date        12/07/92  02:12pm;
Revision    02;
Designer    Todd K. Moyer;
Company     Integrated Circuit Systems;
Assembly    XXXXX;
Location    XXXXX;

/*************************************************************************/
/*                                                                       */
/* VGA @ 2xPAL rate controller          */
/*                                                                       */
/*                                                                       */
/*************************************************************************/
/*                                                                       */
/* Allowable Target Device Types:  g20v8                                 */
/*                                                                       */
/*************************************************************************/

/** Inputs **/

Pin 1          =   clock       ;     /* VGA p-clock                      */
Pin 2          =   h_sync_PAL  ;     /*                                  */

Pin 12         =   GND         ;
Pin 13         =   !OE         ;
Pin 24         =   VCC         ;

/** Outputs **/

Pin [15..18]   =   [HSN_S0..3];      /* used by state machine            */
Pin 19         =   !line_start;      /* pointer reset line mem, act lo   */
Pin 20         =   !write_enable_B;  /* not used by 2xPAL                */
Pin 21         =   !write_enable_A;  /* not used by 2xPAL                */
Pin 22         =   !write_enable;    /*                                  */

/** Declarations and Intermediate Variable Definitions **/

Field    State_HSync        =  [HSN_S0..3];

/** Logic Equations **/
```

```
/** State machine definition **/

Sequence State_HSync
{
        present 0
                if h_sync_PAL next 1
                        out line_start out line_startAB
                        out write_enable out write_enable_A;
                if !h_sync_PAL next 0
                        out write_enable;
        present 1
                if h_sync_PAL next 2
                        out line_start out line_startAB
                        out write_enable out write_enable_A;
                if !h_sync_PAL next 0;
        present 2
                if h_sync_PAL next 3
                        out line_start out line_startAB
                        out write_enable out write_enable_A;
                if !h_synch_PAL next 0;
        present 3
                if !h_sync_PAL next 4;
                        /* out write_enable; */
                if h_sync_PAL next 3
                        out write_enable_A;
        present 4
                if !h_sync_PAL next A;
                if h_sync_PAL next 3;
        present A
                if !h_sync_PAL next 5;
                if h_sync_PAL next 3;
        present 5
                if h_sync_PAL next 6
                        out line_start out line_startAB
                        out write_enable out write_enable_B;
                if !h_sync_PAL next 5
                        out write_enable;
        present 6
                if h_sync_PAL next 7
                        out line_start out line_startAB
                        out write_enable out write_enable_B;
                if !h_sync_PAL next 5;
        present 7
                if h_sync_PAL next 8
                        out line_start out line_startAB
                        out write_enable out write_enable_B;
                if !h_sync_PAL next 5;
        present 8
                if !h_sync_PAL next 9;
                        /* out write_enable; */
                if h_sync_PAL next 8
                out write_enable_B;
```

```
        present 9
                        if !h_sync_PAL next B;
                        if h_sync_PAL next 8;
        present B
                        if !h_sync_PAL next 0;
                        if h_sync_PAL next 8;

        present C
                        next 0;
        present D
                        next 0;
        present E
                        next 0;
        present F
                        next 0;
}
```

Bill of Materials

Item	Qty	Part Name	Description	Manufacturer
1	1	74HC04	HEX INVERTER	Motorola
2	1	74HC74	DUAL D FLIP FLOP	Motorola
3	1	SC11483CV	RAM-DAC	Sierra
4	1	GAL20V8	PLD	Lattice
5	1	LM317	Adjustable Regulator	National
6	1	UPD42101	910x8 FIFO	NEC
7	7	CAP	.1µF Cap	
8	1	R 1/4W	240 ohm	
9	1	R 1/4W	150 ohm	
10	3	R 1/4W	24 ohm	

Flicker Reduction Circuit for use with the GSP600

Introduction

Although a minimal configuration **GSP600** VGA/PAL system uses all of the lines of the graphics image to generate the PAL picture, the resulting PAL display is not (and cannot be) as good as the original VGA display. Despite the fact that all the lines are used, on the standard non-interlaced VGA display *every* line is used for *every* vertical period of about 20.0 ms, while it takes twice as long to put out all the lines to the PAL picture (40 ms). This is accomplished in practice by one of two ways: 1) interlacing the VGA (slowing it down to PAL rates), or 2) using odd numbered lines for odd PAL fields and even numbered lines for even fields, essentially discarding half the lines that are output from the VGA (see the Application Note AN602, *Theory of Operation for a GSP600 Circuit Operating the VGA Display at 2 x PAL Frequency*). It is probably intuitively obvious that either slowing the VGA down or throwing away half the VGA data will result in the PAL output looking less pleasing than the standard VGA display. The practically observed result of this is what is generally known as "flicker", and it should be noted that this problem plagues all scan converters and VGA-to-PAL boards; it is a fundamental limitation of the PAL standard. It is worst when there is a lot of detail along the vertical axis of the VGA image. The most annoying example is a thin, bright white horizontal line made up of a single line on the VGA display. For an example case, imagine that line 100 of the VGA display contains the white line and the rest of the display is black. Then the white line would appear somewhere around line 50 of field 2 in the PAL output, but not at all on field 1. The result will be a flashing of the line with a period of 40.0 ms (reciprocal of the 25 Hz frame rate). This is very noticeable and quite irritating to the eye.

Knowing that displaying a VGA image on an PAL monitor is at best a compromise, we would at least like to achieve the best possible performance from the conversion. Because of this, most scan converters and VGA-to-PAL boards have a "flicker filter." It is enlightening to note that most flicker filters can be turned off, indicating that they are less than desirable in some situations. In fact they reduce the spatial "bandwidth" in the vertical direction, or in other words reduce the vertical resolution. A particularly simple and effective flicker reduction scheme (which can be implemented in software) is to repeat every other VGA line in both fields of the PAL signal. This method, however, requires that half the VGA lines never get to the PAL display; in other words, the vertical resolution is cut in half.

A single horizontal line in the VGA image has only a 50/50 chance of being displayed in PAL, depending on which line number it appears on. Obviously, this method leaves a lot to be desired, since some details in the VGA image can be completely absent from the PAL signal; most people would judge it unacceptable.

You can get a feel for how a better typical flicker filter works by thinking about the example above of a single white horizontal line on scan line 50 of field 2. Imagine "spreading" the line so that some of it spills into the scan lines adjacent to the original line. In an interlaced system such as PAL this means reducing the brightness of line 50 of field 2 (thereby making it gray), and putting some darker shade of gray into lines 50 and 51 of field 1, which are above and below line 50 of field 2, respectively, once the complete frame has been scanned. If done properly, in the right proportions, and viewed from a sufficient distance, the new wide line looks to be of the same brightness as the original single white line. This can significantly reduce the flicker, since there is no longer the situation of black on field 1 and white on field 2 rapidly alternating. However, as you can imagine, any rapid vertical transitions would also become smeared or blurred with such a scheme. The typical complaint is that when trying to display text on an PAL display, a flicker filter will make the text less readable (if it remains readable at all). This type of flicker reduction works best if only the luminance portion of the signal is filtered, since the mixing of several VGA lines to make one PAL line can significantly change the saturation and hue of the color displayed, seriously altering the picture when compared with the VGA display. It is primarily changes in luminance level that cause flicker, so that leaving the chrominance portion of the signal unchanged does not seriously degrade the flicker reduction that is achieved, while it does tend to preserve the look of the image.

To boil all this down, there is a trade-off between flicker reduction and vertical resolution, and it bears repeating that it is a practical impossibility to make an PAL image look just as good as a high resolution VGA image. To try and work around this trade-off, some sophisticated flicker filters are "adaptive", which essentially means that they will dynamically turn themselves on when especially needed to reduce flicker and off when the loss of vertical resolution is especially detrimental. Predictably, this approach is rather expensive and takes up a lot of circuit board space, at least until the time when this function is incorporated into a monolithic integrated circuit. At any rate, a flicker filter of the more basic variety is presented here for use with **GSP600** applications.

Application Circuit

In the accompanying schematic and block diagram an implementation of a simple luminance-only flicker filter which works with the **GSP600** in a VGA-to-PAL system is shown. The schematic details only the portion of the system specific to the flicker filter function, since the VGA portion will vary depending on the VGA chip used. Please refer to the schematic when reading the following detailed circuit description.

U8B divides the frequency of the **VGA_HSYNC** signal **VHS** by two, producing a 50% duty cycle square wave with a frequency of 15.625 kHz. This signal essentially becomes the Write Enable signal at U5 pin 22 and is also sent to the **GSP600** pin 60 as the Horizontal Sync signal **PAL_RATE_HS**. Note that the addition of a divide by 2 in the overall loop which the GSP600 controls forces the VGA chip to clock at twice the rate that it otherwise would, producing a VGA HSync frequency of 31.25 kHz.

U2 is a line buffer memory which can hold up to 910 pixels with a width of 8 bits; it has individual write and read clocks with associated address pointers. Programmable logic device **U5** provides a write enable and pointer reset signals to the line memory. Note that the write clock to U2 (pin 17) is the same rate as the VGA pixel clock; therefore, every VGA pixel will be written in to the memory when write enable (pin 20) is active (low). The write enable is only active for every other line, however, since it is frequency divided by 2 from the VGA HSync as previously noted. This essentially discards half the VGA lines each PAL field, by virtue of the fact that they are not written into memory. The time to write a complete line into memory is 1 VGA line time or **32.0** µs. The read clock for U2 is simply the write clock frequency divided by 2 by U8A. Thus, to read all the pixels out of the memory will require twice as long as to write them, or **64.** µs. This is the length of a PAL line. Therefore, over the span of 2 VGA lines, 1 VGA line is written and 1 PAL line is read, although the writing takes place at twice the rate.

Data read out from U2 at PAL rate is fed to RAMDAC U9, which has its control lines paralleled across the main VGA RAMDAC, except that the active low read enable (pin 6) is permanently disabled by tying it to + 5V. In this way anything written to the VGA RAMDAC (such as changes to the palette) will also be written to U9, but any reads will not cause a conflict with the main VGA RAMDAC. The analog RGB outputs of U9 are sent to the PAL encoder to produce the chrominance component of the composite video output. U6 provides the required voltage reference to U9. Also, the RGB outputs from U9 are combined by resistor matrix in the right proportions to create a luminance signal which can be summed with the adjacent lines' luminance signals, thereby spatially lowpass filtering the luminance signal in the vertical dimension.

Up to this point the circuitry described is basically the same as is required to make the VGA run at 2 x PAL rates (see the Application Note AN602, *Theory of Operation for a GSP600 Circuit Operating the VGA Display at 2 x PAL Frequency*). Note that there are an additional 2 line buffers (U3 and U4), 2 RAMDACs (U10 and U1), and 2 current references (U7A, Q1, and Q2). The additional 2 line buffers store the VGA lines before and after the current line being output via U2 and U9. The RGB current outputs from the RAMDACs U10 and U1 are connected together, summing the two sets of RGB currents together. The combined RGB signals from U10 and U1 are then matrixed together in the proper proportions to produce an adjacent-lines luminance signal. This signal amplitude is independent of the main luminance signal so that the ratio of adjacent line to main line luminance can be set to any desired value, primarily by adjusting R1, which controls the reference currents into U10 and U1.

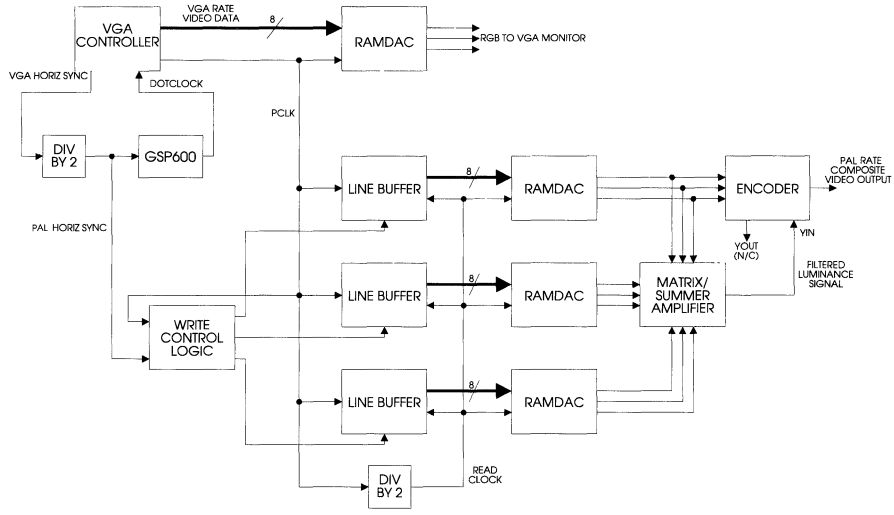


Figure 1

The two luminance signals are connected together, summing them at the input to amplifier U11. U11 then makes up for the resistive losses in the RGB matrices and drives the luminance delay line, whose output is the luminance component of the encoded composite signal. Most encoders have a luminance output and input which allows for an external delay line; not using the output provided while driving the input with an alternate luminance signal of the right amplitude, delay, and polarity allows convenient summing with the chrominance signal generated by the encoder to create the composite video signal.

Programmable logic chip U5 controls the writing of VGA lines into the line buffers such that U2 receives every other line, U3 receives every fourth line, and U4 receives every fourth line, as shown by the timing diagram in Figure 2. Note that only one line buffer is write enabled at a time and every line is written to a line buffer. With this scheme U2 always contains the main VGA line which is going out to the PAL encoder, while U3 and U4 contain the lines adjacent to the main line. The CUPL™ language source code for PLD U5 is included later in this note.

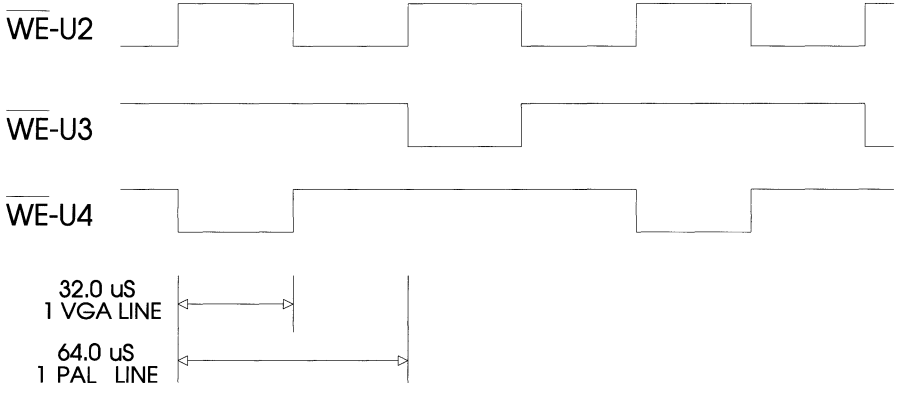


Figure 2

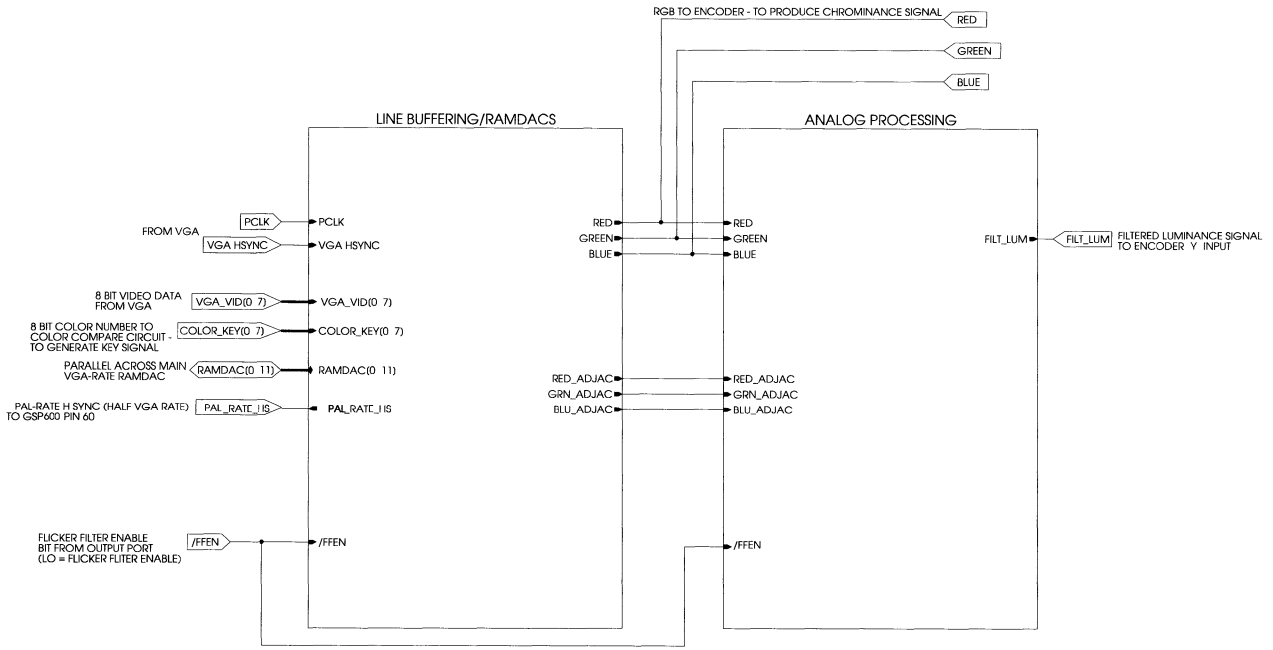
All of the line buffers are continuously read enabled, such that the RGB signal output to the encoder is a combination of the main line and the 2 adjacent line signals. U7A, Q1, and Q2 make up a dual matched current reference for RAMDACs U10 and U1. The amplitude of the adjacent line video signals summed in with the main line is adjustable with R1; the optimum value could be determined so that R1 could be replaced with a fixed divider to save the cost of the trimmer. The amplitude of the main line video signal is controllable by the value of R6 if it is necessary to adjust the proportion of the main line signal that gets summed into the final output. The relative weight of the 2 adjacent line signals in the output is the same due to the matching of the current references into U10 and U1; this should be best for most applications since it is symmetrical about the main line.

The luminance amplitude is controllable by varying the gain of U11 (set by the value of R22); this should normally be set so that luminance levels on any given line are somewhat lower than they would be without filtering. An optional feature shown in the schematic is the ability to switch off the flicker filtering with an I/O bit. Switches Q3 and Q4 turn on when the filter is disabled. In this state Q3 cuts the reference current into U10 and U1, thereby turning off the adjacent line luminance; while Q4 boosts the gain of U11 (by an amount set by R23) to what it should normally be without flicker reduction.

Since when a large area of high luminance level occurs, the video output could exceed the maximum allowed voltage, Q5 and Q6 are used as a positive luminance peak clipper. R27 can be set so that the peak luminance level at the final video output is 714 mV.

BIOS

The video BIOS for the circuit presented here will have to be modified from the typical **GSP600** VGA/PAL system; therefore, register setups for various video modes are given in several tables later in this note.



Flicker Filter Circuit for GSP 600

Figure 3 - Flicker Filter Top Level Schematic

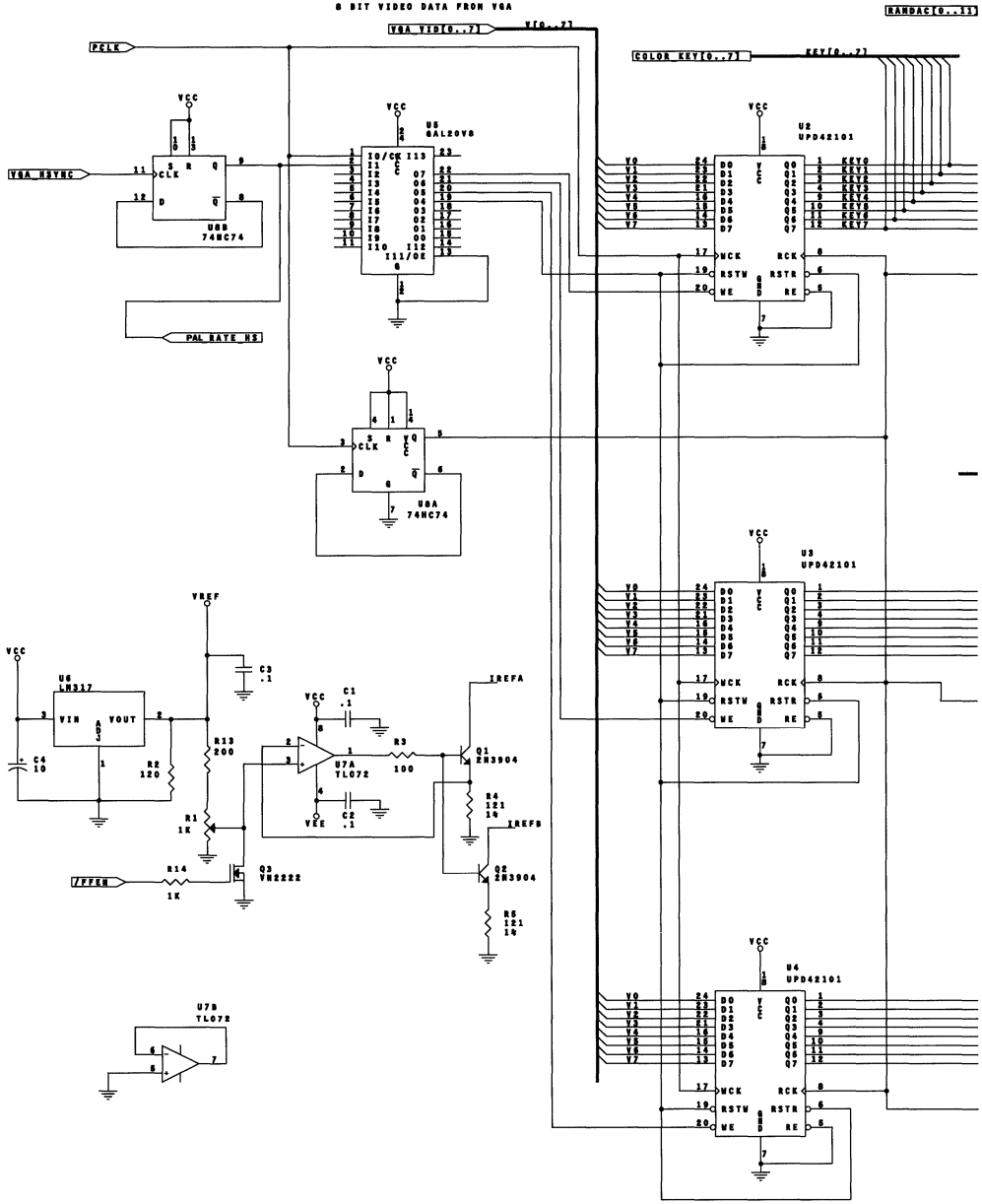
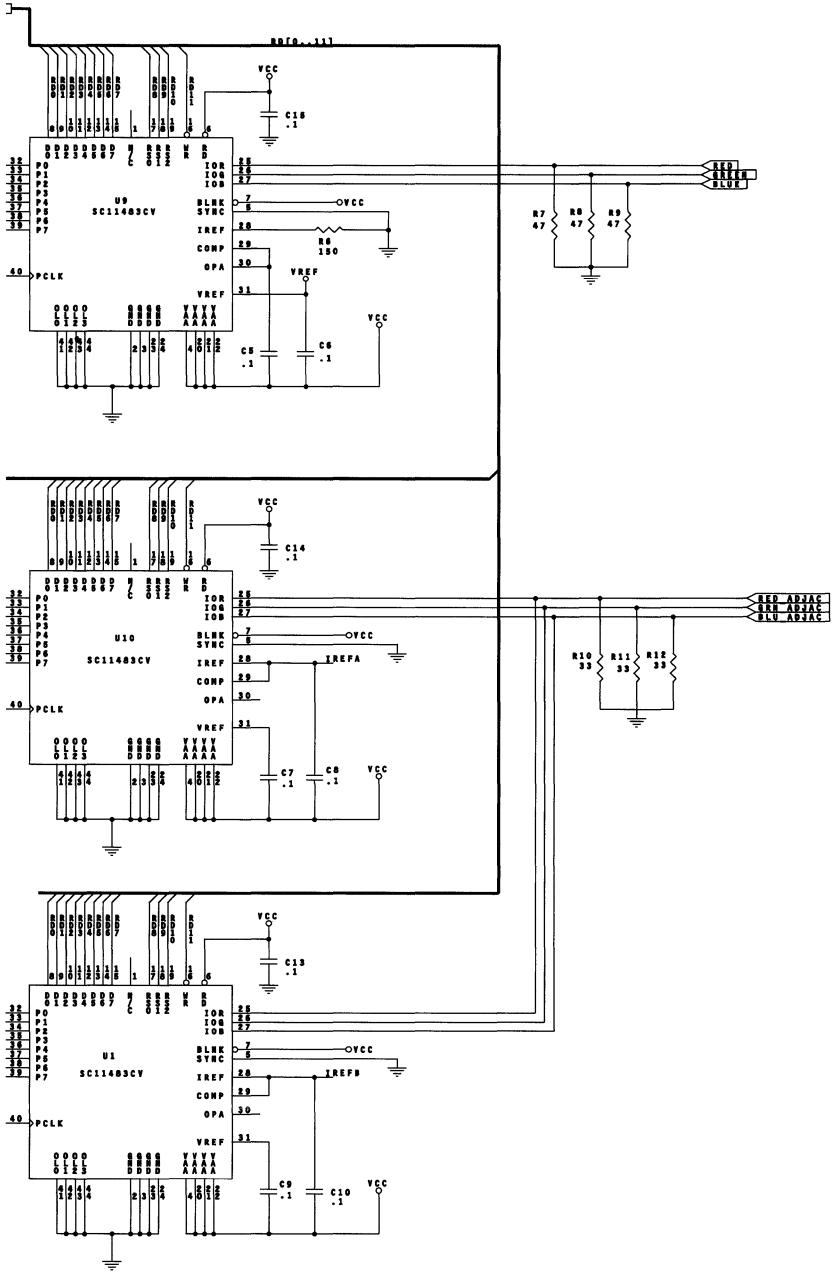

8 BIT VIDEO DATA FROM VGA
VGA_VID[0..7]
V[0..7]
RAMDAC[0..11]
COLOR_KEY[0..7]
KEY[0..7]
PCLK
VGA_HSYNC
PAL_RATE_HS
U8A 74HC74
U8B 74HC74
U5 GAL20V8
U2 UPD42101
U3 UPD42101
U4 UPD42101
VREF
U6 LM317
VIN
VOUT
C3 .1
C4 10
R2 120
R13 200
R1 1K
C1 .1
C2 .1
U7A TL072
R3 100
IREFA
IREFB
Q1 2N3904
Q2 2N3904
R4 121 1%
R5 121 1%
/FFEN
R14 1K
Q3 VN2222
U7B TL072
VCC
VEE

Figure 4 -



Flicker Filter Line Buffering/Ramdacs

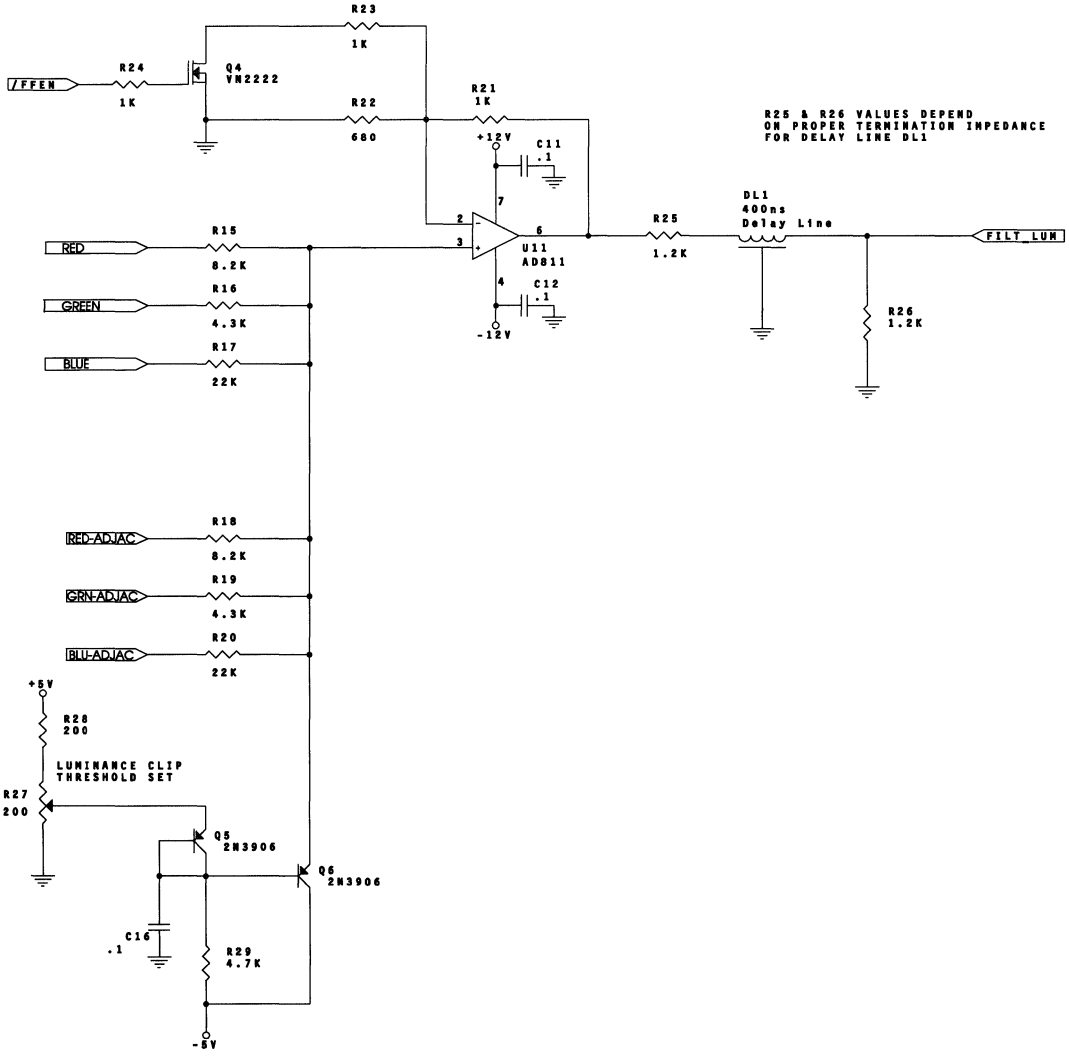


Figure 5 - Flicker Filter Analog Processing

CRTC Registers

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	HT	35	35	6B	6B	35	35	62	6C	35	62	62	62	62	62	62	62
01	HDE	27	27	4F	4F	27	27	4F	4F	27	4F	4F	4F	4F	4F	04	4F
02	SHB	2A	28	57	57	2A	2A	50	54	2A	50	50	50	50	50	50	50
03	EHB	95	96	8B	8B	96	96	85	8B	96	85	85	85	84	84	85	84
04	SHR	2E	2E	5D	5D	2F	2F	58	5D	2F	58	58	58	54	57	58	57
05	EHR	A0	A0	8C	8C	80	80	9B	83	80	9B	9B	9B	82	82	9B	82
06	VT	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B	0B
07	OVERFLOW	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E	3E
08	PRS	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
09	MSL	4F	4F	4F	4F	C1	C1	C1	4F	C0	C0	40	40	40	40	C0	40

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
0A	CS	0D	0D	0D	0D	00	00	00	0D	00	00	00	00	00	00	00	00
0B	CE	0E	0E	0E	0E	00	00	00	0E	00	00	00	00	00	00	00	00
0C	SAH	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0D	SAL	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0E	CLH	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0F	CLL	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
10	VRS	BE	BE	BE	BE	C5	C5	C5	BE	C5	C5	A7	A7	F4	F4	C5	EF
11	VRE	22	22	22	22	88	88	88	82	88	88	8B	8B	87	87	88	87
12	VDE	8F	8F	8F	8F	8F	8F	8F	8F	8F	8F	5D	5D	DF	DF	8F	DF
13	OFFSET	14	14	28	28	14	14	28	28	14	28	28	28	28	28	28	50
14	UNDERLINE	1F	1F	1F	1F	00	00	00	1F	00	00	0F	0F	00	00	40	60
15	SVB	B8	B8	B8	B8	C2	C2	C2	B8	C2	C2	9F	9F	E0	E0	C2	E0
16	EVB	E3	E3	E3	E3	05	05	05	E3	05	05	CA	CA	0C	0C	05	0C
17	MC	A3	A3	A3	A3	A2	A2	C2	A3	E3	E3	E3	E3	E3	E3	A3	AB
18	LC	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
*	INTERLACE																

* = Interlace Bit must be turned off for all modes

General Register

INDEX	REGISTER	VIDEO MODES															
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	MISC OUT	#	#	#	#	#	#	#	@	#	#	@	#	#	#	#	#

#	@
23 = GenLock (GL)	22 = GenLock (GL)
27 = OVerlay (OV)	26 = OVerlay (OV)
2B = Video Only (VO)	2A = Video Only (VO)
2F = Graphics Only (GO)	2E = Graphics Only (GO)

Sequence Registers

INDEX	REGISTER	VIDEO MODES														
		00	01	02	03	04	05	06	07	0D	0E	0F	10	11	12	13	**
00	CLK MODE	09	09	01	01	09	09	01	00	09	01	01	01	01	01	01	01

** = 640 x 480 x 256 colors

Source Code for PLD U5 (GAL20V8) in CUPL™ Language

```
Name        ff;
Partno      ff01;
Date        1/20/93;
Revision    01;
Designer    Todd K. Moyer;
Company     Integrated Circuit Systems;
Assembly    Flicker Filter;
Location    U5;

/*************************************************************************/
/*                                                                       */
/* VGA @ 2xPAL rate controller with basic line flicker filtering         */
/*                                                                       */
/*                                                                       */
/*************************************************************************/
/*                                                                       */
/* Allowable Target Device Types:  g20v8                                 */
/*                                                                       */
/*************************************************************************/

/** Inputs **/

Pin 1       =   clock       ;   /* VGA PCLK signal                      */
Pin 2       =   h_sync_PAL  ;   /*                                      */
Pin 12      =   GND         ;
Pin 13      =   !OE         ;
Pin 24      =   VCC         ;

/** Outputs **/

Pin [15..18]    =   [HSN_S0..3];    /* used by state machine            */
Pin 19          =   !line_start;    /* pointer reset line mem, act lo   */

Pin 20      =   !write_enable_B;    /*                                  */
Pin 21      =   !write_enable_A;    /*                                  */
Pin 22      =   !write_enable;      /*                                  */

/** Declarations and Intermediate Variable Definitions **/

Field   State_HSync     =   [HSN_S0..3];

/** Logic Equations **/
```

```
/** State machine definition **/

Sequence State_HSync
{
        present 0
                if h_sync_PAL next 1
                        out line_start out line_startAB
                        out write_enable out write_enable_A;
                if !h_sync_PAL next 0
                        out write_enable;
        present 1
                if h_sync_PAL next 2
                        out line_start out line_startAB
                        out write_enable out write_enable_A;
                if !h_sync_PAL next 0;
        present 2
                if h_sync_PAL next 3
                        out line_start out line_startAB
                        out write_enable out write_enable_A;
                if !h_synch_PAL next 0;
        present 3
                if !h_sync_PAL next 4;
                        /* out write_enable; */
                if h_sync_PAL next 3
                        out write_enable_A;
        present 4
                if !h_sync_PAL next A;
                if h_sync_PAL next 3;
        present A
                if !h_sync_PAL next 5;
                if h_sync_PAL next 3;
        present 5
                if h_sync_PAL next 6
                        out line_start out line_startAB
                        out write_enable out write_enable_B;
                if !h_sync_PAL next 5
                        out write_enable;
        present 6
                if h_sync_PAL next 7
                        out line_start out line_startAB
                        out write_enable out write_enable_B;
                if !h_sync_PAL next 5;
        present 7
                if h_sync_PAL next 8
                        out line_start out line_startAB
                        out write_enable out write_enable_B;
                if !h_sync_PAL next 5;
        present 8
                if !h_sync_PAL next 9;
                        /* out write_enable; */
                if h_sync_PAL next 8
                out write_enable_B;
```

```
        present 9
                    if !h_sync_PAL next B;
                    if h_sync_PAL next 8;
        present B
                    if !h_sync_PAL next 0;
                    if h_sync_PAL next 8;

        present C
                    next 0;
        present D
                    next 0;
        present E
                    next 0;
        present F
                    next 0;
}
```

Bill of Materials

Item	Qty	Reference	Part
1	15	C1, C2, C3, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16	.1µF
2	1	C4	10µF
3	1	DL1	400 ns
4	2	Q1, Q2	2N3904
5	2	Q3, Q4	VN2222
6	2	Q5, Q6	2N3906
7	5	R1, R14, R21, R23, R24	1K
8	1	R2	120
9	1	R3	100
10	2	R4, R5	121
11	1	R6	150
12	3	R7, R8, R9	47
13	3	R10, R11, R12	33
14	3	R13, R27, R28	200

Item	Qty	Reference	Part
15	2	R15, R18	8.2K
16	2	R16, R19	4.3K
17	2	R17, R20	22K
18	1	R22	680
19	2	R25, R26	1.2K
20	1	R29	4.7K
21	3	U1, U9, U10	SC11483CV
22	3	U2, U3, U4	UPD42101
23	1	U5	GAL20V8
24	1	U6	LM317
25	1	U7	TL072
26	1	U8	74HC74
27	1	U11	AD811

ICS

Video Timing Generator

Products

As the recognized world leader in frequency synthesis technology, ICS continues to build on its solid foundation, bringing the most requested features to market.

In particular, ICS has expanded video clock product offerings to provide a truly complete selection unequaled in performance, breadth and value. These new products are available now.

New products in this edition offer advanced features like full user-programmability to offer you the maximum in design flexibility.

As a market-oriented company, ICS welcomes inquiries concerning our new product areas or other frequency synthesis applications.

ICS Video Timing Generator Selection Guide

Product Application	ICS Device Type	Features	Max Frequency	Clock Outputs	Package Types	Page
P.C. Clocks	ICS1394	External Loop Filter. For New Designs. Use ICS1494A.	85 MHz	1 TTL	20 Pin DIP, SOIC	153
	ICS1494A	Buffered Xtal Out, Lock Detect Output.	135 MHz	1 TTL	20 Pin DIP, SOIC	155
	ICS2494/94A	Buffered Xtal Out, Lock DetectOutput.	135 MHz	2 TTL	20 Pin DIP, SOIC	161
	ICS2495	Small Footprint, Narrow Body SOIC Package.	135 MHz	2 TTL	16 Pin DIP, SOIC	167
	ICS2496	Low Voltage, 3/5 Volt Operation for Laptop/Notebook Applications. Powerdown Mode.	85/135 MHz	2 TTL	16 Pin DIP, SOIC	173
	ICS2595	Programmable Dual ICS2494 Pin Compatible.	135 MHz	2 TTL	20 Pin DIP, SOIC	179
	ICS82C404	Dual Programmable Graphics Clock Generator. ICS82C404 Compatible.	120 MHz	2 TTL	16 Pin DIP, SOIC	189
	ICS9161	Dual Programmable Graphics Clock Generator. ICD2061 Compatible	135 MHz	3 TTL	16 Pin DIP, SOIC	223
	AV9194	Dual Video memory Clock Generator with 16 Preprogrammed Video and 4 Preprogrammed Memory Frequencies.	135 MHz	2 TTL	20 Pin DIP, SOIC	237
Western Digital Compatible Clock Generators	ICS90C61A	Drop-in upgrade for the WD90C61. Integral Loop Filters.	80 MHz	2 TTL	20 Pin DIP, SOIC, PLCC	193
	ICS90C64A	WD90C31 VGA Controller Compatible. Enhanced Version. Integral Loop Filter. (Replaces ICS90C63, ICS90C64.)	80 MHz	2 TTL	20 Pin DIP, SOIC, PLCC	203
	ICS90C65	Low Voltage, 3/5 Volt. Powerdown Mode. WD 90C26 VGA Controller Compatible.	80 MHz	2 TTL	20 Pin DIP, SOIC, PLCC	213

Notes:
1. All products have internal loop filters except as noted.
2. All products operate at 5 volts typ. except as noted.

ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development Characteristic data and other specifications are design goals. ICS reserves the right to change or discontinue these products without notice

Video Dot Clock Generator

Features

- Low cost - eliminates need for multiple crystal clock oscillators in video display subsystems
- Strobed /transparent frequency select options
- Mask-programmable frequencies
- Glitch-free frequency transitions
- Compatible with Industry STD VGA Controllers
- Provision for two external frequency inputs
- Low power CMOS device technology
- Small footprint - 20 pin DIP or SO

Applications

- 85 MHz Guaranteed Performance
- EGA - VGA - Super VGA XGA video adapters
- High resolution MAC II displays
- Workstations
- LCD and other flat panel display systems
- 8514A - TMS 34010 - TMS 34020
- Motherboard - PS2 display systems

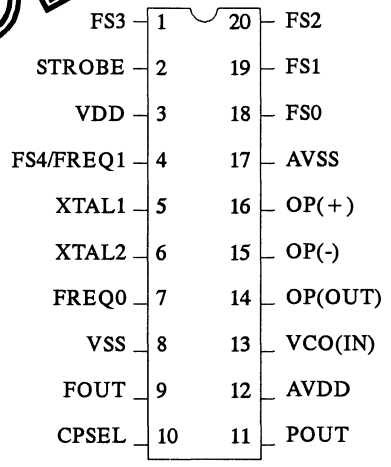
NOT RECOMMENDED FOR NEW DESIGN

Introduction

The **ICS1394 Dot Clock Generator** is an integrated circuit capable of generating up to 32 video dot clock frequencies for use with high performance video display systems. Utilizing CMOS technology to implement all linear, digital and memory functions, the **ICS1394** provides a low power, small footprint, low cost solution to the generation of video dot clocks. Outputs are compatible with **CGA, VGA, EGA, MCGA, XGA, MDA,** as well as the higher frequencies needed for advanced applications in desktop publishing and workstation graphics. Provision is made via a single level custom mask to implement customer specific frequency sets. Phase locked loop circuitry permits rapid glitch-free transitions between clock frequencies.

Principal applications for these products include generating dot clock frequencies for EGA, VGA, Super VGA, and XGA graphics products in the IBM-compatible world, as well as for high resolution MAC II and workstations. Applications utilizing 8514A and TMS 34010 and TMS 34020 benefit as well, with significant performance improvements and cost reductions in all of these applications.

Pin Configuration



Ordering Information

ICS1394NXXX (DIP Package)
ICS1394MXXX (SO Package)
(XXX = Pattern number)

Enhanced Video Dot Clock Generator

Features

- Low cost - eliminates need for multiple crystal clock oscillators in video display subsystems
- Mask-programmable frequencies
- Pre-programmed versions for Industry Standard VGA chips
- Glitch-free frequency transitions
- Provision for external frequency input
- Excellent power supply rejection

Applications

- Higher Frequency applications
- EGA - VGA - Super VGA-XGA video adapters
- High resolution MAC II displays
- Workstations
- LCD and other flat panel display systems
- 8514A - TMS 34010 - TMS 34020

Description

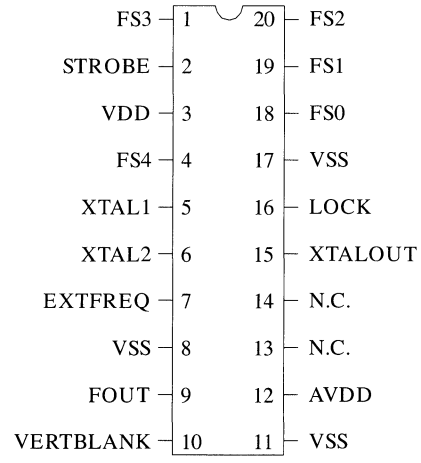
The **ICS1494** Dot Clock Generator is an integrated circuit capable of generating up to 32 video dot clock frequencies for use with high performance video display systems. Utilizing CMOS technology to implement all linear, digital and memory functions, the **ICS1494** provides a low power, small footprint, low cost solution to the generation of video dot clocks. Outputs are compatible with **VGA, EGA, XGA, MCGA, CGA, MDA,** as well as the higher frequencies needed for advanced applications in desktop publishing and workstation graphics. Provision is made via a single-level custom mask to implement customer-specific frequency sets. Phase-locked loop circuitry permits rapid glitch-free transitions between clock frequencies.

In addition to providing 32 clock rates, the **ICS1494** has provisions to multiplex an externally-generated signal source into the **FOUT** signal path. The **ICS1494** can also be programmed to select the crystal oscillator signal as the **FOUT** output. Internal phase-locked frequencies continue to remain locked at their preset values when these modes are selected. This feature permits instantaneous transition from an external frequency to an internally-generated frequency. Printed circuit board testing is simplified by the use of these modes, as an external clock generated by the ATE tester can be fed through, permitting synchronous testing of the entire graphics system.

Features

- 135 MHz Guaranteed Performance
- Fast acquisition of selected frequencies
- Internal loop filter eliminates noise pickup
- Advanced PLL for low phase-jitter
- Improved loop stability over entire frequency range
- Frequency change synchronized to vertical retrace
- Frequency change-detection circuitry enhances new frequency acquisition
- Lock Detect Output
- Buffered XTAL Out

Pin Configuration



Notes:

1. In applications where the external frequency input is not specified, EXTFREQ must be tied to VDD.
2. ICS1494M(SO) pinout is identical to ICS1494N(DIP).

Ordering Information

ICS1494NXXX (DIP Package)
ICS1494MXXX (SO Package)
(XXX = Pattern number)

Circuit and Application Options

The **ICS1494** will typically derive its frequency reference from a series-resonant crystal connected between pins 5 and 6. Where a high quality reference signal is available, such as in an application where the graphics subsystem is resident on the motherboard, this reference may directly replace the crystal. This signal should be coupled to pin 1. If the reference signal amplitude is less than 3.5 volts, a .047 microfarad capacitor should be used to couple the reference signal into XTAL1. Pin 6 must be left open.

The **ICS1494** is capable of multiplexing an externally generated frequency source of **FOUT** via a mask option, in addition to its internally generated clock.

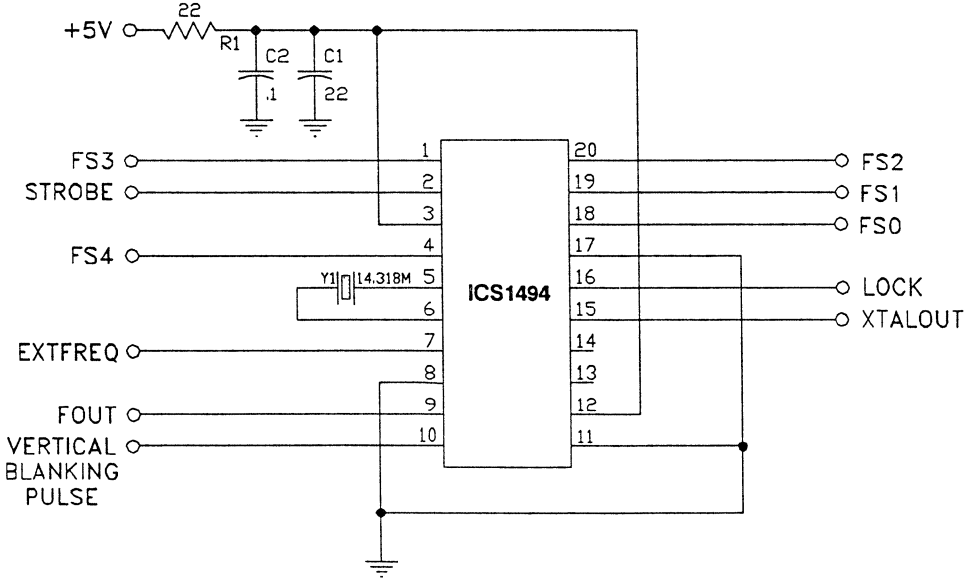
This is input via **EXTFREQ (7)**. When an external source is selected the PLL remains locked to the value specified in the selected address. This provision facilitates the ability to rapidly change frequencies. When this option is not specified in the ROM pattern, pin 7 is internally tied to V_{DD} and should be connected to V_{DD} on the PCB.

Power Supply Conditioning

The **ICS1494** is a member of the second generation of dot clock products. By incorporating the loop filter on chip and upgrading the VCO, the ease of application has been substantially improved over earlier products. If a stable and noise-free power supply is available, no external components are required. However, in most applications it is judicious to decouple the power supply as shown in Figures 1 or 2. Figure 1 is the normal configuration for 5 Volt only applications. Which of the two provides superior performance depends on the noise content of the power supplies. In general, the configuration of Figure 1 is satisfactory. Figure 2 is the more conventional if a 12 Volt analog supply is available, although the improved performance comes at a cost of an extra component. The cost of the discretes used in Figure 2 is less than the cost of Figure 1's discrete components.

The number and differentiation of the analog and digital supply pins are intended for maximum performance products. In most applications, all V_{DD}s may be tied together. The function of the multiple pins is to allow the user to realize the maximum performance from the silicon with a minimum degradation due to the package and PCB. At the frequencies of interest, the effects of the inductance of the bond wires and package lead frame are non-trivial. By using the multiple pins, ICS minimized the effect of packaging and minimized the interaction of the digital and analog supply currents.

Figure 1

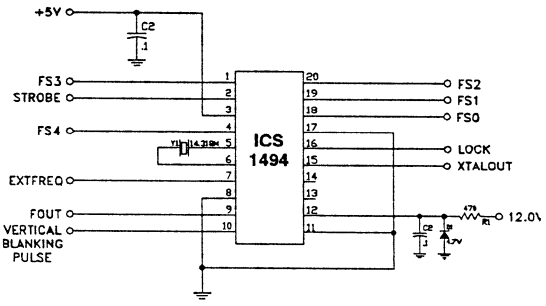


Applications

Layout Considerations

Utilizing the **ICS1494** in video graphics adapter cards or on PS2 motherboards is simple but does require precautions in board layout if satisfactory jitter-free performance is to be realized. Care should be exercised in ensuring that components not related to the **ICS1494** do not share its ground. In applications utilizing a multi-layer board, V_{SS} should be directly connected to the ground plane. Multiple pins are utilized for all analog and digital Vss and Vdd connections to permit extended frequency **VCLK** operation to 135 MHz. However, in all cases, all V_{SS} and V_{DD} pins should be connected.

Figure 2



Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate series-resonant crystal should be connected between **XTAL1 (5)** and **XTAL2 (6)**. In IBM-compatible applications this will typically be a 14.31818 MHz crystal, but fundamental mode crystals between 10MHz and 25MHz have been tested . Maintain short lead lengths between the crystal and the **ICS1494**. In some applications, it may be desirable to utilize the bus clock. If the signal amplitude is equal to or greater than 3.5 volts, it may be connected directly to **XTAL1 (5)**. If the signal amplitude is less than 3.5 volts, connect the clock through a .047 microfarad capacitor to **XTAL1 (5)**, and keep the lead length of the capacitor to **XTAL1 (5)** to a minimum to reduce noise susceptibility. This input is internally biased at $V_{DD}/2$. Since TTL compatible clocks typically exhibit a V_{OH} of 3.5V, capacitively coupling the input restores noise immunity. The **ICS1494** is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of this signal is typically outside of the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. **XTAL2 (6)** must be left open in this configuration.

LOCK

LOCK(16) is an output signal which may be monitored to indicate when the **ICS1494** has achieved phase lock after a change in frequency has been selected. In systems where it is used, it is tied to an interrupt input to the microprocessor. When high, it indicates phase lock has been achieved.

Buffered XTALOUT

In motherboard applications, it may be desirable to have the **ICS1494** provide the bus clock for the rest of the system. This eliminates the need for an additional 14.31818 MHz crystal oscillator in the system, saving money as well as board space. To do this, the **XTALOUT (15)** output should be buffered with a CMOS driver.

Output Circuit Considerations

As the dot clock is usually the highest frequency present in a video graphics system, consideration should be given to EMI. To minimize problems with meeting FCC EMI requirements, the trace which connects **FOUT(9)** and other components in the system should be kept as short as possible. The **ICS1494** outputs have been designed to minimize overshoot. In addition it may be helpful to place a ferrite bead in this signal path to limit the propagation of high order harmonics of this signal. A suitable device would be a Ferroxcube 56-590-65/4B or equivalent. This device should be placed physically close to the **ICS1494**. A 33 to 47 Ohm series resistor, sometimes called source termination, in this path may be necessary to reduce ringing and reflection of the signal and may reduce phase-jitter as well as EMI.

External Frequency Sources

EXTFREQ (7), on versions so equipped by the programming, is an input to a digital multiplexer. When this input is enabled, signals driving the input will appear at **FOUT(9)** instead of the PLL output. Internally, the PLL will remain in lock at the frequency selected by the ROM code. **If this option is not specified, pin (7) is connected to VDD internally, and MUST be connected to VDD or left open, not grounded!**

Digital Inputs

FS0 (18), FS1 (19), FS2 (20),FS3(1), and **FS4 (4)**, are the TTL compatible frequency select inputs for the binary code corresponding to the frequency desired. **STROBE (2),** when high, allows new data into the frequency select latches; and when low, prevents address changes per Figure 3. The internal power-on-clear signal will force an initial frequency code corresponding to an all zeros input state. **VERTBLANK (10)**, when low, inhibits the transfer of new frequency select information. Enabling this pin during the vertical blanking interval causes the change in frequency to happen at this time and prevents any visible glitch when a new frequency is selected. If this feature is not required, this pin may be left open.

Absolute Maximum Ratings

Supply Voltage ..... V_{DD} ..... -0.5V to + 7V
Input Voltage ..... V_{IN} ..... -0.5V to V_{DD}+ 0.5V
Output Voltage ..... V_{OUT} ..... -0.5V to V_{DD}+ 0.5V
Clamp Diode Current ..... V_{IK} & I_{OK} ..... + /-30mA
Output Current per Pin ..... I_{OUT} ..... + /-50mA
Operating Temperature ..... T_o ..... 0 °C to 70 °C
Storage Temperature ..... T_S ..... -85 °C to + 150 °C
Power Dissipation ..... P_D 500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to > = V_{SS} and < = V_{DD}.

DC Characteristics (0 °C to 70 °C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{dd}	Operating Voltage Range	4.0	5.5	V	
V_{il}	Input Low Voltage	V_{ss}	0.8	V	V_{dd} = 5V
V_{ih}	Input High Voltage	2.0	V_{dd}	V	V_{dd} = 5V
I_{lh}	Input Leakage Current	-	10	uA	V_{in} = V_{cc}
V_{ol}	Output Low Voltage	-	0.4	V	I_{ol} = 4.0 mA
V_{oh}	Output High Voltage	2.4	-	V	I_{oh} = 4.0 mA
I_{dda}	Analog Supply Current	-	5	mA	V_{dd} = 5.0V, FOUT = 25 MHz
I_{dda}	Analog Supply Current	-	7	mA	V_{dd} = 5.0V, FOUT = 110 MHz
I_{ddd}	Digital Supply Current	-	12	mA	V_{dd} = 5.0V, FOUT = 25 MHz
I_{ddd}	Digital Supply Current	-	25	mA	V_{dd} = 5.0V, FOUT = 110 MHz
R_{up} *	Internal Pullup Resistors	50	200	K Ohm	V_{dd} = 5V, V_{in} = 0V
C_{in}	Input Pin Capacitance	-	8	pF	F_c = 1 MHz
C_{out}	Output Pin Capacitance	-	12	pF	F_c = 1 MHz

* The following inputs have pull-ups: FS0-4, STROBE, EXTFREQ, VERTBLANK.

AC Timing Characteristics

The following notes apply to all parameters presented in this section:

1. Xtal Frequency = 14.31818 MHz
2. All units are in nanoseconds (ns).
3. Rise and fall time is between 0.8 and 2.0 VDC.
4. Output pin loading = 15pF
5. Duty cycle is measured at 1.4V.
6. Supply Voltage Range = 4.75 to 5.25 Volts
7. Temperature Range = 0 °C to 70 °C

SYMBOL	PARAMETER	MIN	MAX	NOTES
	STROBE TIMING			
Tpw	Strobe Pulse Width	20	-	
Tsu	Setup Time Data to Strobe	10	-	
Thd	Hold Time Data to Strobe	10	-	
	FOUT TIMING			
Tr	Rise Time	-	3	
Tf	Fall Time	-	3	
-	Frequency Error		0.5	%
-	Maximum Frequency		135	MHz
-	Propagation Delay for Pass Through Frequency	-	15	ns
	Duty Cycle	40%	60%	110 MHz or less

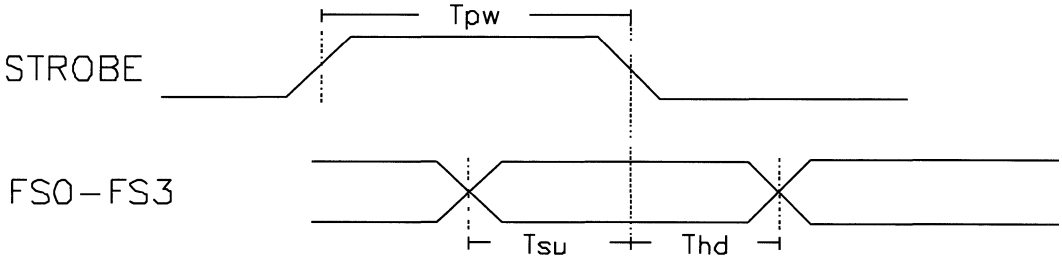


Figure 3

Dual Video/Memory Clock Generator

Features

- World standard ICS2494A has been reconfigured to allow 8 memory frequencies.
- Mask-programmable frequencies
- Pre-programmed versions for Industry Standard VGA chips
- Glitch-free frequency transitions
- Provision for external frequency input
- Internal clock remains locked when the external frequency input is selected
- Low power CMOS device technology
- Small footprint - 20 pin DIP or SO

New Features

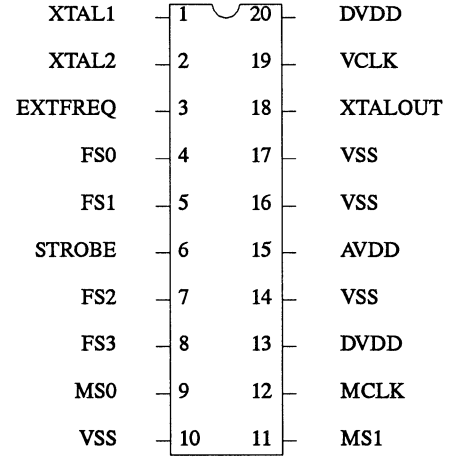
- Buffered Xtal Out
- Integral loop filter components
- Fast acquisition of selected frequencies, strobed or non-strobed
- Guaranteed performance up to 135 MHz
- Excellent power supply rejection
- Advanced PLL for low phase-jitter
- Frequency change detection circuitry which enhances new frequency acquisition and eliminates problems caused by programs that rewrite frequency information.
- Improved pinout - easier board layout.

Applications

- VGA-Super VGA-XGA video adapters
- Workstations
- 8514A-TMS34010-TMS34020
- Motherboard

Description

The Dot Clock Generator is an integrated circuit dual phase-locked loop frequency synthesizer capable of generating sixteen video dot clock frequencies and eight memory clock frequencies for use with high performance video display systems. Utilizing CMOS technology to implement all linear, digital and memory functions, the **ICS2494/94A** provides a low-power, small-footprint, low-cost solution to the generation of video dot clocks. Outputs are compatible with XGA, VGA, EGA, MCGA, CGA, MDA, as well as the higher frequencies needed for advanced applications in desktop publishing and workstation graphics. Provision is made via a single-level custom mask to implement customer-specific frequency sets. Phase-locked loop circuitry permits rapid glitch-free transitions between clock frequencies.



Notes:

1. In applications where the external frequency input is not specified, EXTFREQ must be tied to V_{SS}.
2. ICS2494/94AM(SO) pinout is identical to ICS2494/94AN(DIP).

Ordering Information

ICS2494NXXX, ICS2494ANXXX (DIP Package)
ICS2494MXXX, ICS2494AMXXX (SO Package)
(XXX = Pattern number)

Circuit and Application Options

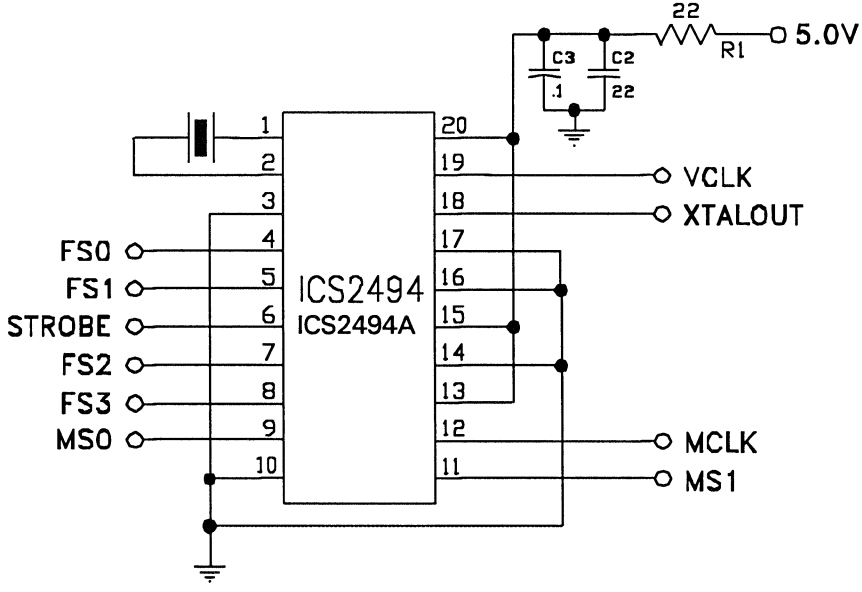
The **ICS2494/94A** will typically derive its frequency reference from a series-resonant crystal connected between pins 1 and 2. Where a high quality reference signal is available, such as in an application where the graphics subsystem is resident on the motherboard, this reference may directly replace the crystal. This signal should be coupled to pin 1. If the reference signal amplitude is less than 3.5 volts, a .047 microfarad capacitor should be used to couple the reference signal into **XTAL1**. Pin 2 must be left open.

Power Supply Conditioning

The **ICS2494/94A** is a member of the second generation of dot clock products. By incorporating the loop filter on chip and upgrading the VCO, the ease of application has been substantially improved over earlier products. If a stable and noise-free power supply is available, no external components are required. However, in most applications it is judicious to decouple the power supply as shown in Figures 1 or 2. Figure 1 is the normal configuration for 5 volt only applications. Which of the two provides superior performance depends on the noise content of the power supplies. In general, the configuration of Figure 1 is satisfactory. Figure 2 is the more conventional if a 12 volt analog supply is available, although the improved performance comes at a cost of an extra component. The cost of the discretes used in Figure 2, however, are less than the cost of Figure 1's discrete components.

The number and differentiation of the analog and digital supply pins are intended for maximum performance products. In most applications, all VDDs may be tied together. The function of the multiple pins is to allow the user to realize the maximum performance from the silicon with a minimum degradation due to the package and PCB. At the frequencies of interest, the effects of the inductance of the bond wires and package lead frame are non-trivial. By using the multiple pins, ICS minimized the effect of packaging and minimized the interaction of the digital and analog supply currents.

Figure 1

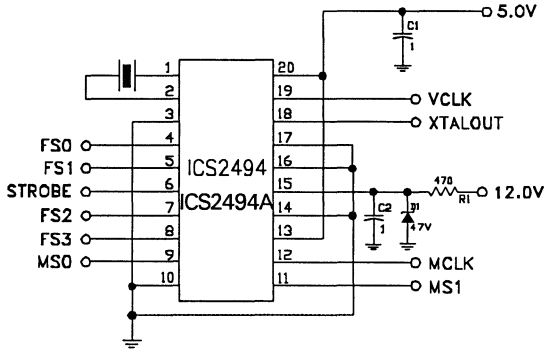


Applications

Layout Considerations

Utilizing the **ICS2494/94A** in video graphics adapter cards or on PS2 motherboards is simple but does require precautions in board layout if satisfactory jitter-free performance is to be realized. Care should be exercised in ensuring that components not related to the **ICS2494/94A** do not share its ground. In applications utilizing a multi-layer board, VSS should be directly connected to the ground plane. Multiple pins are utilized for all analog and digital VSS and VDD connections to permit extended frequency VCLK operation to 135 MHz. However, in all cases, all VSS and VDD pins should be connected.

Figure 2



Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate series-resonant crystal should be connected between **XTAL1 (1)** and **XTAL2 (2)**. In IBM-compatible applications this will typically be a 14.31818 MHz crystal, but fundamental mode crystals between 10 MHz and 25 MHz have been tested. Maintain short lead lengths between the crystal and the **ICS2494/94A**. In some applications, it may be desirable to utilize the bus clock. If the signal amplitude is equal to or greater than 3.5 volts, it may be connected directly to **XTAL1 (1)**. If the signal amplitude is less than 3.5 volts, connect the clock through a .047 microfarad capacitor to **XTAL1 (1)**, and keep the lead length of the capacitor to **XTAL1 (1)** to a minimum to reduce noise susceptibility. This input is internally biased at VDD/2. Since TTL compatible clocks typically exhibit a VOH of 3.5V, capacitively coupling the input restores noise immunity.

The **ICS2494/94A** is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of this signal is typically outside of the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. **XTAL2 (2)** must be left open in this configuration.

Buffered XTALOUT

In motherboard applications it may be desirable to have the **ICS2494/94A** provide the bus clock for the rest of the system. This eliminates the need for an additional 14.31818 MHz crystal oscillator in the system, saving money as well as board space. To do this, the **XTALOUT (18)** output should be buffered with a CMOS driver.

Output Circuit Considerations

As the dot clock is usually the highest frequency present in a video graphics system, consideration should be given to EMI. To minimize problems with meeting FCC EMI requirements, the trace which connects **VCLK (19) or MCLK (12)** and other components in the system should be kept as short as possible. The **ICS2494/94A** outputs have been designed to minimize overshoot. In addition it may be helpful to place a ferrite bead in these signal paths to limit the propagation of high order harmonics of this signal. A suitable device would be a Ferroxcube 56-590-65/4B or equivalent. This device should be placed physically close to the **ICS2494/94A**. A 33 to 47 Ohm series resistor, sometimes called source termination, in this path may be necessary to reduce ringing and reflection of the signal and may reduce phase-jitter as well as EMI.

Digital Inputs

FS0 (4), FS1 (5), FS2 (7), and **FS3 (8)** are the TTL compatible frequency select inputs for the binary code corresponding to the frequency desired. **STROBE (6)**, when high, allows new data into the frequency select latches; and when low, prevents address changes per Figure 3. The internal power-on-clear signal will force an initial frequency code corresponding to an all zeros input state. **MS0 (9), MS1 (11)** and **MS2 (3)** are the corresponding memory select inputs and are not strobed.

Absolute Maximum Ratings

Supply Voltage	V_{DD}	-0.5V to +7V
Input Voltage	V_{IN}	-0.5V to V_{DD}+0.5V
Output Voltage	V_{OUT}	-0.5V to VDD+0.5V
Clamp Diode Current	V_{IK} & I_{OK}	+/ -30mA
Output Current per Pin	I_{OUT}	+/ -50mA
Operating Temperature	T_o	0 °C to 70 °C
Storage Temperature	T_S	-85 °C to +150 °C
Power Dissipation	P_D	500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to >= V_{SS} and <= V_{DD}.

DC Characteristics (0 °C to 70 °C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{DD}	Operating Voltage Range	4.0	5.5	V	
V_{IL}	Input Low Voltage	V_{ss}	0.8	V	V_{dd} = 5V
V_{IH}	Input High Voltage	2.0	V_{dd}	V	V_{dd} = 5V
I_{IH}	Input Leakage Current	-	10	uA	V_{in} = V_{cc}
V_{OL}	Output Low Voltage	-	0.4	V	I_{ol} = 4.0 mA
V_{OH}	Output High Voltage	2.4	-	V	I_{oh} = 4.0 mA
I_{DD}	Supply Current	-	35	mA	V_{dd} = 5V, VCLK = 80 MHz
R_{UP} *	Internal Pullup Resistors	50	200	K Ohm	V_{dd} = 5V, V_{in} = 0V
C_{in}	Input Pin Capacitance	-	8	pF	F_c = 1 MHz
C_{out}	Output Pin Capacitance	-	12	pF	F_c = 1 MHz

* The following inputs have pullups: FS0-3, MS0-1, STROBE.

Frequency Pattern Availability

ICS offers the largest variety of standard frequency patterns in the industry, supporting all popular VGA controller devices. The attached listing provides the selection as of this publication date. Contact your local ICS sales office for latest frequency pattern availability.

AC Timing Characteristics

The following notes apply to all parameters presented in this section:

1. Xtal Frequency = 14.31818 MHz
2. $T_C = 1/F_C$
3. All units are in nanoseconds (ns).
4. Rise and fall time is between 0.8 and 2.0 VDC.
5. Output pin loading = 25pF
6. Duty cycle is measured at 1.4V.
7. Supply Voltage Range = 4.0 to 5.5 Volts
8. Temperature Range = 0 °C to 70 °C

SYMBOL	PARAMETER	MIN	MAX	NOTES
	STROBE TIMING			
Tpw	Strobe Pulse Width	20	-	
Tsu	Setup Time Data to Strobe	10	-	
Thd	Hold Time Data to Strobe	10	-	
	MCLK AND VCLK TIMINGS			
Tr	Rise Time	-	3	Duty Cycle 40% min. to
Tf	Fall Time	-	3	60% max.
-	Frequency Error		0.5	%
-	Maximum Frequency		135	MHz
-	Propagation Delay for Pass Through Frequency	-	15	ns

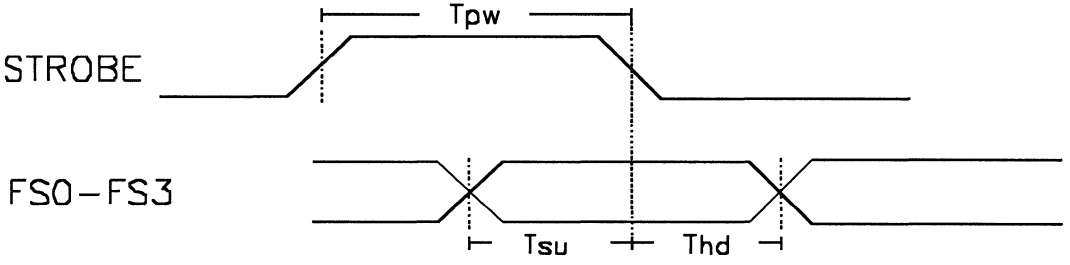


Figure 3

Dual Video/Memory Clock Generator

Features

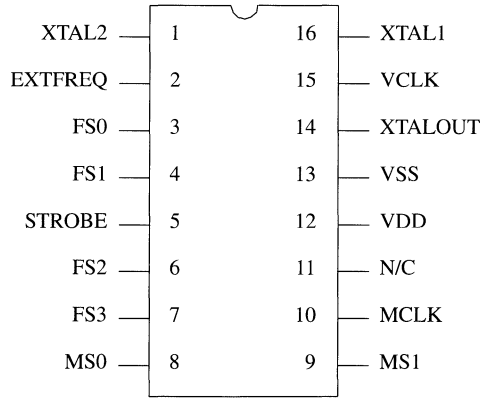
- Low cost - eliminates need for multiple crystal clock oscillators in video display subsystems
- Mask-programmable frequencies
- Pre-programmed versions for Industry Standard VGA chips
- Glitch-free frequency transitions
- Internal clock remains locked when the external frequency input is selected
- Low power CMOS device technology
- Small footprint - 16 pin DIP or SO
- Buffered Xtal Out
- Integral Loop Filter components
- Fast acquisition of selected frequencies, strobed or non-strobed
- Guaranteed performance up to 135 MHz
- Excellent power supply rejection
- Advanced PLL for low phase-jitter
- Frequency change detection circuitry enhances new frequency acquisition and eliminates problems caused by programs that rewrite frequency information

Description

The **ICS2495** Clock Generator is an integrated circuit dual phase-locked loop frequency synthesizer capable of generating 16 video frequencies and 4 memory clock frequencies for use with high performance video display systems. Utilizing CMOS technology to implement all linear, digital and memory functions, the **ICS2495** provides a low-power, small-footprint, low-cost solution to the generation of video dot clocks. Outputs are compatible with **XGA**, **VGA**, **EGA**, **MCGA**, **CGA**, **MDA**, as well as the higher frequencies needed for advanced applications in desktop publishing and workstation graphics. Provision is made via a single level custom mask to implement customer specific frequency sets. Phase-locked loop circuitry permits rapid glitch-free transitions between clock frequencies.

In addition to providing 16 clock rates, the **ICS2495** has provisions to multiplex an externally-generated signal source into the VCLK signal path. Internal phase-locked frequencies continue to remain locked at their preset values when this mode is selected. This feature permits instantaneous transition from an external frequency to an internally-generated frequency. Printed circuit board testing is simplified by the use of these modes as an external clock generated by the ATE tester can be fed through, permitting synchronous testing of the entire system.

Pin Configuration



Notes:
1 ICS2495M(SO) pinout is identical to ICS2495N(DIP).

Ordering Information

ICS2495N-XXX (DIP Package)
ICS2495M-XXX (SO Package)
(XXX = Pattern number)

Reference Oscillator & Crystal Selection

In cases where the on-chip crystal oscillator is used to generate the reference frequency, the accuracy of the crystal oscillation frequency will have a very small effect on output accuracy.

The external crystal and the on-chip circuit implement a Pierce oscillator. In a Pierce oscillator, the crystal is operated in its parallel-resonant (also called anti-resonant mode). This means that its actual frequency of oscillation depends on the effective capacitance that appears across the terminals of the quartz crystal. Use of a crystal that is characterized for use in a series-resonant circuit is fine, although the actual oscillation frequency will be slightly higher than the value stamped on the crystal can (typically 0.025%-0.05% or so). Normally, this error is not significant in video graphics applications, which is why the **ICS2495** will typically derive its frequency reference from a series resonant crystal connected between pins 1 and 16.

As the entire operation of the phase-locked loop depends on having a stable reference frequency, the crystal should be mounted as close as possible to the package. Avoid routing digital signals or the **ICS2495** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

Power Supply Conditioning

The **ICS2495** is a member of the second generation of dot clock products. By incorporating the loop filter on chip and upgrading the VCO, the ease of application has been substantially improved over earlier products. If a stable and noise-free power supply is available, no external components are required. However, in most applications it is judicious to decouple the power supply as shown in Figure 1.

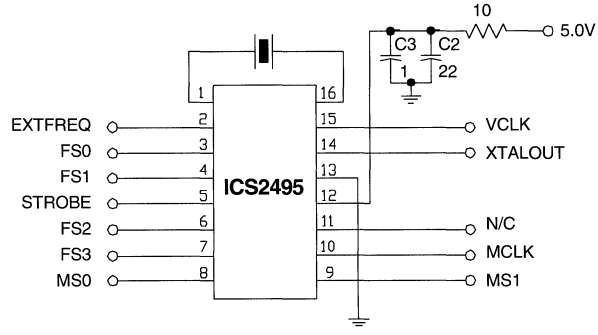
Layout Considerations

Utilizing the **ICS2495** in video graphics adapter cards or on PS2 motherboards is simple, but does require precautions in board layout if satisfactory jitter-free performance is to be realized. Care should be exercised to ensure that components not related to the **ICS2495** do not share its ground. In applications utilizing a multi-layer board, V_{SS} should be directly connected to the ground plane.

Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate crystal should be connected between **XTAL1 (16)** and **XTAL2 (1)**. In IBM compatible applications this will typically be a 14.31818 MHz crystal, but fundamental mode crystals between 10MHz and 25MHz have been tested. Maintain short lead lengths between the crystal and the **ICS2495**. In some applications, it may be desirable to utilize the bus clock. If the signal amplitude is equal to or greater than 3.5 volts, it may be connected directly to **XTAL1 (16)**. If the signal amplitude is less than 3.5 volts, connect the clock through a .047 microfarad capacitor to **XTAL1 (16)**, and keep the lead length of the capacitor to **XTAL1 (16)** to a minimum to reduce noise susceptibility. This input is internally biased at $V_{DD}/2$. Since TTL compatible clocks typically guarantee a V_{OH} of only 2.8V, capacitively coupling the input restores noise immunity. The **ICS2495** is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of this signal is typically outside of the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. **XTAL2 (1)** must be left open in this configuration.

Buffered XTALOUT



NOTES: FS3-FS0, MS1-MS0, EXTFREQ, and STROBE inputs are all equipped with pullups and need not be tied high.
Mount decoupling capacitors as close as possible to the device and connect device ground to the ground plane where available.
Mount crystal and its circuit traces away from switching digital lines and the VCLK, MCLK and XTALOUT lines.

Figure 1

In motherboard applications it may be desirable to have the **ICS2495** provide the bus clock for the rest of the system. This eliminates the need for an additional 14.31818 MHz crystal oscillator in the system, saving money as well as board space. Depending on the load, it may be judicious to buffer XTALOUT when using it to provide the system clock.

Output Circuit Considerations

As the dot clock is usually the highest frequency present in a video graphics system, consideration should be given to EMI. To minimize problems with meeting FCC EMI requirements, the trace which connects **VCLK** or **MCLK** and other components in the system should be kept as short as possible. The **ICS2495** outputs have been designed to minimize overshoot. In addition, it may be helpful to place a ferrite bead in these signal paths to limit the propagation of high-order harmonics of this signal. A suitable device would be a Ferroxcube 56-590-65/4B or equivalent. This device should be placed physically close to the **ICS2495**. A 33 to 47 Ohm series resistor, sometimes called source termination, in this path may be necessary to reduce ringing and reflection of the signal and may thereby reduce phase jitter as well as EMI.

External Frequency Sources

EXTFREQ on versions so equipped by the programming, is an input to a digital multiplexer. When this input is enabled by the FS0-3 selection, the signal driving pin 2 will appear at **VCLK (15)** instead of the PLL output. Internally, the PLL will remain in lock at the frequency selected by the ROM code.

The programming option also exists to output the crystal oscillator output on VCLK. In the case where XTAL1 is being driven by an external oscillator, then this frequency would appear on VCLK if so programmed.

Digital Inputs

FS0 (3), **FS1 (4)**, **FS2 (6)**, and **FS3 (7)**, are the TTL compatible frequency select inputs for the binary code corresponding to the frequency desired. **STROBE (5)** when high, allows new data into the frequency select latches; and when low, prevents address changes per Figure 2. The internal power-on-clear signal will force an initial frequency code corresponding to an all zeros input state. **MS0 (8)** and **MS1 (9)** are the corresponding memory select inputs and are not strobed.

Pin Descriptions

The following table provides the pin description for the 16-pin **ICS2495** packages.

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
1	XTAL2	OUT	Crystal interface
2	EXTFREQ	IN	External clock input (if so programmed)
3	FS0	IN	Control input for VCLK selection
4	FS1	IN	Control input for VCLK selection
5	STROBE	IN	Strobe for latching FS (0-3) (*High enable*)
6	FS2	IN	Control input for VCLK selection
7	FS3	IN	Control input for VCLK selection
8	MS0	IN	Select input for MCLK selection
9	MS1	IN	Select input for MCLK selection
10	MCLK	OUT	Memory Clock Output
11	N/C	-	Not Connected
12	VDD	-	Power
13	VSS	-	Ground
14	XTALOUT	OUT	Buffered Crystal Output
15	VCLK	OUT	Video Clock Output
16	XTAL1	IN	Reference input clock from system

Absolute Maximum Ratings

Ambient Temperature under bias	0 °C to 70 °C
Storage temperature	-40 °C to 125 °C
Voltage on all inputs and outputs with respect to V_{SS}	0.3 to 7 Volts

Note: Stresses above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (OV Ground). Positive current flows into the referenced pin.

Operating Temperature range	0 °C to 70 °C
Power supply voltage	4.75 to 5.25 Volts

DC Characteristics at 5 Volts V_{DD}

SYMBOL	PARAMETER		MIN	MAX	UNITS	CONDITIONS
V_{DD}	Operating Voltage Range		4.75	5.25	V	
V_{IL}	Input Low Voltage		V_{SS}	0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage		2.0	V_{DD}	V	V_{DD} = 5V
I_{IH}	Input Leakage Current		-	10	µA	$V_{in} = V_{CC}$
V_{OL}	Output Low Voltage:	VCLK, MCLK	-	0.4	V	I_{OL} = 8.0 mA
		XTALOUT	-	0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage:	VCLK, MCLK	2.4	-	V	I_{OH} = 8.0 mA
		XTALOUT	2.4	-	V	I_{OH} = 4.0 mA
I_{DD}	Supply Current		-	30	mA	VDD = 5V
R_{UP}	Internal Pullup Resistors		50	-	K ohms	V_{IN} = 0.0V
C_{in}	Input Pin Capacitance		-	8	pF	F_C = 1 MHz
C_{out}	Output Pin Capacitance		-	12	pF	F_C = 1 MHz

AC Timing Characteristics

The following notes apply to all of the parameters presented in this section.

1. REFCLK = 14.318 MHz
2. $T_C = 1/F_C$
3. All units are in nanoseconds (ns).
4. Maximum jitter within a range of 30 µs after triggering on a 400 MHz scope.
5. Rise and fall time between 0.8 and 2.0 VDC unless otherwise stated.
6. Output pin loading = 15pF.
7. Duty cycle measured at 1.4 volts.

SYMBOL	PARAMETER	MIN	MAX	NOTES
	STROBE TIMING			
Tpw	Strobe Pulse Width	20	-	
Tsu	Setup Time Data to Strobe	10	-	
Thd	Hold Time Data to Strobe	10	-	
	MCLK and VCLK TIMINGS			
Tr	Rise Time	-	2	Duty Cycle 40% min. to
Tf	Fall Time	-	2	60% max.
-	Frequency Error		0.5	%
-	Maximum Frequency		135	MHz
-	Propagation Delay for Pass Through Frequency	-	20	ns
-	Output Enable to Tri-State (into and out of) time		15	ns

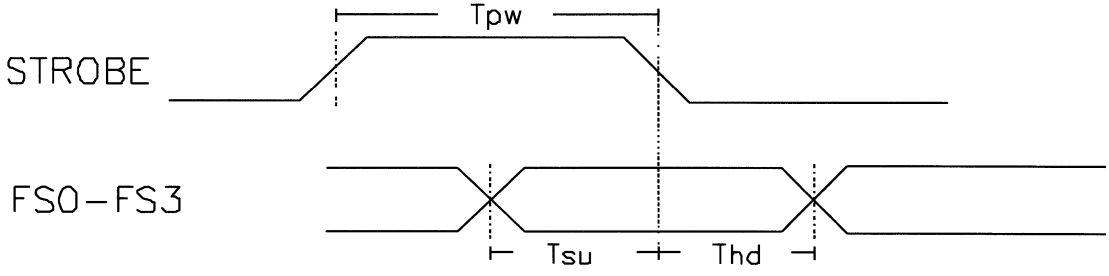


Figure 2

Integrated Circuit Systems, Inc.

Dual Voltage Video/Memory Clock Generator

Features

- Specified for dual voltage operation (V_{DD} = 3.3V or 5V) but operates continuously from 3.0V to 5.25V
- Powerdown input for extended battery life in portable applications
- Guaranteed performance up to 110 MHz (at 3.3V) or 135 MHz (at 5V)
- Advanced PLL for low phase-jitter
- Low power CMOS device technology
- Excellent power supply rejection
- Integral Loop Filter components
- Mask-programmable frequencies
- Small footprint - 16 pin DIP or SO
- Generates 16 video clock frequencies derived from a 14.318 MHz system clock reference frequency
- Provision for external frequency input
- Video clock is selectable among the 16 internally generated clocks, one external clock, or the buffered crystal oscillator
- Internal clock remains locked when the external frequency input is selected
- On-chip generation of four memory clock frequencies
- Patented technique eliminates cross-interference between video and memory clocks
- Fast acquisition of selected frequencies, strobed or non-strobed

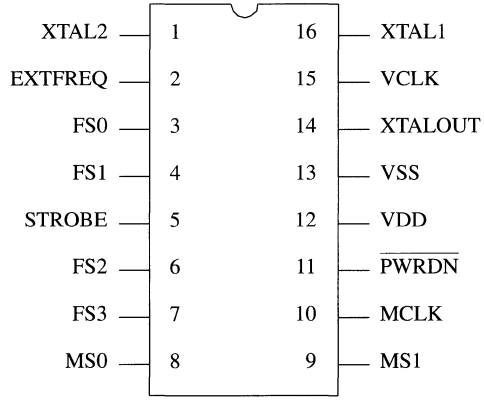
Description

The **ICS2496** has been specifically designed to serve the portable PC market with operation at either 3.3V or 5V with a comprehensive power-saving shut down mode.

The **ICS2496** Clock Generator is a dual phase-locked loop frequency synthesizer capable of generating 16 video frequencies and four memory clock frequencies for use with high performance video display systems. Utilizing CMOS technology to implement all linear, digital and memory functions, the **ICS2496** provides a low power, small footprint, low cost solution to the generation of video dot clocks. Provision is made via a single level custom mask to implement customer specific frequency sets. Phase-locked loop circuitry permits rapid glitch-free transitions between clock frequencies.

In addition to providing 16 clock rates, the **ICS2496** has provisions to multiplex an externally-generated signal source into the **VCLK** signal path. Internal phase-locked frequencies continue to remain locked at their preset values when this mode is selected. This feature permits instantaneous transition from an external frequency to an internally-generated frequency. Printed circuit board testing is simplified by the use of these modes, as an external clock generated by the ATE tester can be fed through, permitting synchronous testing of the entire system.

Pin Configuration



Notes:
1. ICS2496M(SO) pinout is identical to ICS2496N(DIP).

Ordering Information

ICS2496N-XXX (DIP Package)
ICS2496M-XXX (SO Package)
(XXX = Pattern number)

Circuit Function and Application

"Powerdown"

The **ICS2496** has been optimized for use in battery operated portables. It can be placed in a powerdown mode which drops its supply current requirement below 1 microamp. When placed in this mode, the digital inputs FS0-3, STROBE, MS0-1, and EXTFREQ may be either high or low or floating without causing an increase in the **ICS2496** sup-ply current.

The PWRDN pin must be low (It has an internal pull-down.) in order to place the device in its low power state. The output pins (VCLK and MCLK) are driven high and XTALOUT is driven low by the **ICS2496** when it is in its low power state.

If a crystal is being used, nothing needs to be done to achieve low power. If XTAL1 is being driven by an external source, it may be driven low or high without a power penalty. If XTAL1 is at an intermediate voltage (V_{SS} +0.5V < V_{IN} < V_{DD} -0.5), there will be a small increase in supply current. If XTAL1 is driven at 14.318 MHz while the chip is in powerdown, the **ICS2496** supply current will increase to approximately 1.2 mA.

The STROBE (pin 5) may be used to guard against inadvertent frequency changes during powerdown/power-up sequences. By holding the STROBE low during powerdown and power-up sequences, the **ICS2496** will retain the most recent video frequency selection.

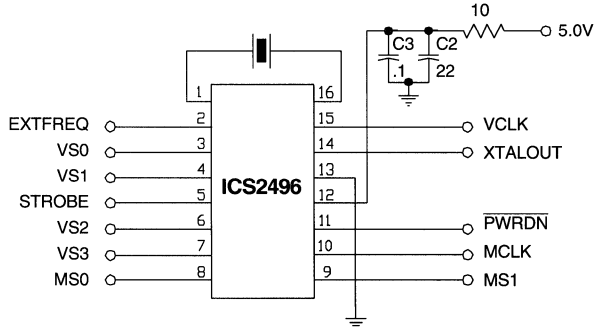
Reference Oscillator and Crystal Selection

In cases where the on-chip crystal oscillator is used to generate the reference frequency, the accuracy of the crystal oscillation frequency will have a very small effect on output accuracy.

The external crystal and the on-chip circuit implement a Pierce oscillator. In a Pierce oscillator, the crystal is operated in its parallel-resonant (also called anti-resonant) mode. This means that its actual frequency of oscillation depends on the effective capacitance that appears across the terminals of the quartz crystal. Use of a crystal that is characterized for use in a series-resonant circuit is fine, although the actual oscillation frequency will be slightly higher than the value stamped on the crystal can (typically 0.025%-0.05% or so). Normally, this error is not significant in video graphics applications, which is why the **ICS2496** will typically derive its frequency reference from a series-resonant crystal connected between pins 1 and 16.

As the entire operation of the phase-locked loop depends on having a stable reference frequency, the crystal should be mounted as close as possible to the package. Avoid routing digital signals or the **ICS2496** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

The **ICS2496** is a member of the second generation of dot clock products. By incorporating the loop filter on chip and upgrading the VCO, the ease of application has been substantially improved over earlier products. If a stable and noise-free power supply is available, no external components are required. However, in most applications it is judicious to decouple the power supply as shown in Figure 1.



NOTES: FS3-FS0, MS1-MS0, EXTFREQ, and STROBE inputs are all equipped with pull-ups and need not be tied high.
PWRDN input has an internal pulldown and must be driven or tied high for full device function.
Mount decoupling capacitors as close as possible to the device and connect device ground to the ground plane where available
Mount crystal and its circuit traces away from switching digital lines and the VCLK, MCLK, and XTALOUT lines.

Figure 1

Layout Considerations

Utilizing the **ICS2496** in video graphics adapter cards or on PS2 motherboards is simple, but does require precautions in board layout if satisfactory jitter-free performance is to be realized. Care should be exercised in ensuring that components not related to the **ICS2496** do not share its ground. In applications utilizing a multi-layer board, V_{SS} should be connected directly to the ground plane.

Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate crystal should be connected between **XTAL1 (16)** and **XTAL2 (1)**. In IBM-compatible applications this will typically be a 14.31818 MHz crystal, but fundamental mode crystals between 10MHz and 25MHz have been tested. Maintain short lead lengths between the crystal and the **ICS2496**. In some applications, it may be desirable to utilize the bus clock. If the signal amplitude is equal to or greater than 3.5 volts, it may be connected directly to **XTAL1 (16)**. If the signal amplitude is less than 3.5 volts, connect the clock through a .047 microfarad capacitor to **XTAL1 (16)**, and keep the lead length of the capacitor to **XTAL1 (16)** to a minimum to reduce noise susceptibility. This input is internally biased at V_{DD}/ 2. Since TTL compatible clocks typically guarantee a V_{OH} of only 2.8V, capacitively coupling the input restores noise immunity. The **ICS2496** is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of this signal is typically outside of the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. **XTAL2 (1)** must be left open in this configuration.

Buffered XTALOUT

In motherboard applications it may be desirable to have the **ICS2496** provide the bus clock for the rest of the system. This eliminates the need for an additional 14.31818 MHz crystal oscillator in the system, saving money as well as board space. Depending on the load, it may be judicious to buffer XTALOUT when using it to provide the system clock.

Output Circuit Considerations

As the dot clock is usually the highest frequency present in a video graphics system, consideration should be given to EMI. To minimize problems with meeting FCC EMI requirements, the trace which connects **VCLK** or **MCLK** and other components in the system should be kept as short as possible. The **ICS2496** outputs have been designed to minimize overshoot. In addition, it may be helpful to place a ferrite bead in these signal paths to limit the propagation of high order harmonics of this signal. A suitable device would be a Ferroxcube 56-590-65/4B or equivalent. This device should be placed physically close to the **ICS2496**. A 33 to 47 Ohm series resistor, sometimes called source termination, in this path may be necessary to reduce ringing and reflection of the signal and may thereby reduce phase-jitter as well as EMI.

External Frequency Sources

EXTFREQ on versions so equipped by the programming, is an input to a digital multiplexer. When this input is enabled by the FS0-3 selection, the signal driving pin 2 will appear at **VCLK (15)** instead of the PLL output. Internally, the PLL will remain in lock at the frequency selected by the ROM code.

The programming option also exists to output the crystal oscillator output on VCLK. In the case where XTAL1 is being driven by an external oscillator, then this frequency would appear on VCLK if so programmed.

Digital Inputs

FS0 (3), **FS1 (4)**, **FS2 (6)**, and **FS3 (7)**, are the TTL compatible frequency select inputs for the binary code corresponding to the frequency desired. **STROBE (5)**, when high, allows new data into the frequency select latches; and when low, prevents address changes per Figure 2. The internal power-on-clear signal will force an initial frequency code corresponding to an all-zeros input state. **MS0 (8)** and **MS1 (9)** are the corresponding memory select inputs and are not strobed.

Pin Descriptions

The following table provides the pin description for the 16-pin **ICS2496** packages:

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
1	XTAL2	OUT	Crystal interface
2	EXTFREQ	IN	External clock input (if so programmed)
3	FS0	IN	Control input for VCLK selection
4	FS1	IN	Control input for VCLK selection
5	STROBE	IN	Strobe for latching FS (0-3) (*High enable*)
6	FS2	IN	Control input for VCLK selection
7	FS3	IN	Control input for VCLK selection
8	MS0	IN	Select input for MCLK selection
9	MS1	IN	Select input for MCLK selection
10	MCLK	OUT	Memory Clock Output
11	$\overline{\text{PWRDN}}$	IN	Powerdown Control (low for powerdown)
12	VDD	-	Power
13	VSS	-	Ground
14	XTALOUT	OUT	Buffered Crystal Output
15	VCLK	OUT	Video Clock Output
16	XTAL1	IN	Reference input clock from system

Absolute Maximum Ratings

Ambient Temperature under bias	0 °C to 70 °C
Storage temperature	-40 °C to 125 °C
Voltage on all inputs and outputs with respect to VSS	0.3 to 7 Volts

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin.

Operating Temperature range	0 °C to 70 °C
Power supply voltage	3.0 to 5.25 Volts

DC Characteristics at 5 Volts V_{DD}

SYMBOL	PARAMETER		MIN	MAX	UNITS	CONDITIONS
V_{DD}	Operating Voltage Range		4.75	5.25	V	
V_{IL}	Input Low Voltage		V_{SS}	0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage		2.0	V_{DD}	V	V_{DD} = 5V
I_{IH}	Input Leakage Current		-	10	µA	$V_{in} = V_{CC}$
V_{OL}	Output Low Voltage:	VCLK, MCLK	-	0.4	V	I_{OL} = 8.0 mA
		XTALOUT	-	0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage:	VCLK, MCLK	2.4	-	V	I_{OH} = 8.0 mA
		XTALOUT	2.4	-	V	I_{OH} = 4.0 mA
I_{DD}	Supply Current		-	30	mA	VDD = 5V
R_{UP}	Internal Pullup Resistors		50	-	K ohms	V_{IN} = 0.0V
C_{in}	Input Pin Capacitance		-	8	pF	F_C = 1 MHz
C_{out}	Output Pin Capacitance		-	12	pF	F_C = 1 MHz
I_{PN}	Powerdown Supply Current		-	1.0	µA	V_{DD}=3.3V
R_{DN}	Internal Pulldown Equivalent		20	-	K ohms	$V_{IN}=V_{DD}$=5V

DC Characteristics at 3.3 Volts V_{DD}

SYMBOL	PARAMETER		MIN	MAX	UNITS	CONDITIONS
V_{DD}	Operating Voltage Range		3.0	3.6	V	
V_{IL}	Input Low Voltage		V_{SS}	0.8	V	V_{DD} = 3.3V
V_{IH}	Input High Voltage		2.0	V_{DD}	V	V_{DD} = 3.3V
I_{IH}	Input Leakage Current		-	10	µA	$V_{in} = V_{DD}$
V_{OL}	Output Low Voltage:	VCLK, MCLK	-	0.4	V	I_{OL} = 3.0 mA
		XTALOUT	-	0.4	V	I_{OL} = 1.5 mA
V_{OH}	Output High Voltage:	VCLK, MCLK	2.4	-	V	I_{OH} = 3.0 mA
		XTALOUT	2.4	-	V	I_{OL} = 1.5 mA
I_{DD}	Supply Current		-	20	mA	V_{DD} = 3.3V
R_{UP}	Internal Pullup Resistors		100	-	K ohms	V_{IN} = 0.0V
C_{in}	Input Pin Capacitance		-	8	pF	F_C = 1 MHz
C_{out}	Output Pin Capacitance		-	12	pF	F_C = 1 MHz
I_{PN}	Powerdown Supply Current		-	1.0	µA	V_{DD} =3.3V
R_{DN}	Internal Pulldown Equivalent		50	-	K ohms	$V_{IN} = V_{DD}$ =3.3V

AC Timing Characteristics

The following notes apply to all of the parameters presented in this section:

1. REFCLK = 14.318 MHz
2. $T_C = 1/F_C$
3. All units are in nanoseconds (ns).
4. Maximum jitter is within a range of 30 µs after triggering on a 400 MHz scope.
5. Rise and fall time is between 0.8 and 2.0 VDC unless otherwise stated.
6. Output pin loading = 15pF
7. Duty cycle is measured at $V_{DD}/2$ unless otherwise stated.

SYMBOL	PARAMETER	MIN	MAX	NOTES
	STROBE TIMING			
Tpw	Strobe Pulse Width	10	-	
Tsu	Setup Time Data to Strobe	10	-	
Thd	Hold Time Data to Strobe	2	-	
	MCLK and VCLK TIMINGS @ **5.0V**			
Tr	Rise Time	-	2	Duty Cycle 40% min. to
Tf	Fall Time	-	2	60% max.
-	Frequency Error		0.5	%
-	Maximum Frequency		135	MHz
-	Propagation Delay for Pass Through Frequency	-	20	ns
-	Output Enable to Tri-State (into and out of) time		15	ns
	MCLK and VCLK TIMINGS @ **3.3V**			
Tr	Rise Time	-	3	Duty Cycle 40% min. to
Tf	Fall Time	-	3	60% max.
-	Frequency Error		.5	%
-	Maximum Frequency		110	MHz
-	Propagation Delay for Pass Through Frequency	-	30	ns
-	Output Enable to Tri-State (into and out of) time		20	ns

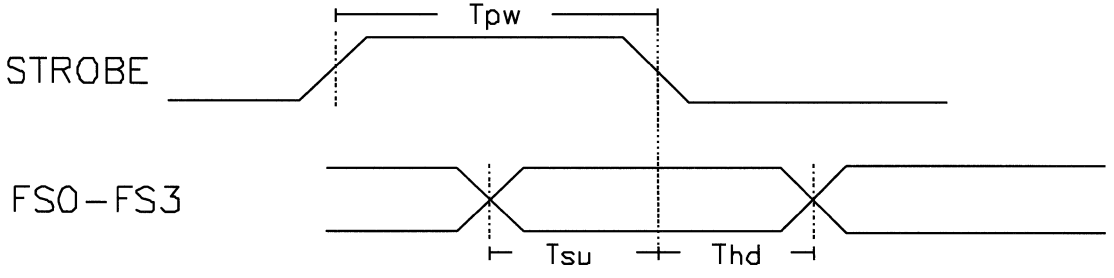


Figure 2

User-Programmable Dual High-Performance Clock Generator

Description

The **ICS2595** is a dual-PLL (phase-locked loop) clock generator specifically designed for high-resolution, high-refresh rate, video applications. The video PLL generates any of 16 pre-programmed frequencies through selection of the address lines **FS0-FS3**. Similarly, the auxiliary PLL can generate any one of four pre-programmed frequencies via the **MS0 & MS1** lines.

A unique feature of the **ICS2595** is the ability to redefine frequency selections in both the VCLK and MCLK synthesizers after power-up. This permits complete set-up of the frequency table upon system initialization.

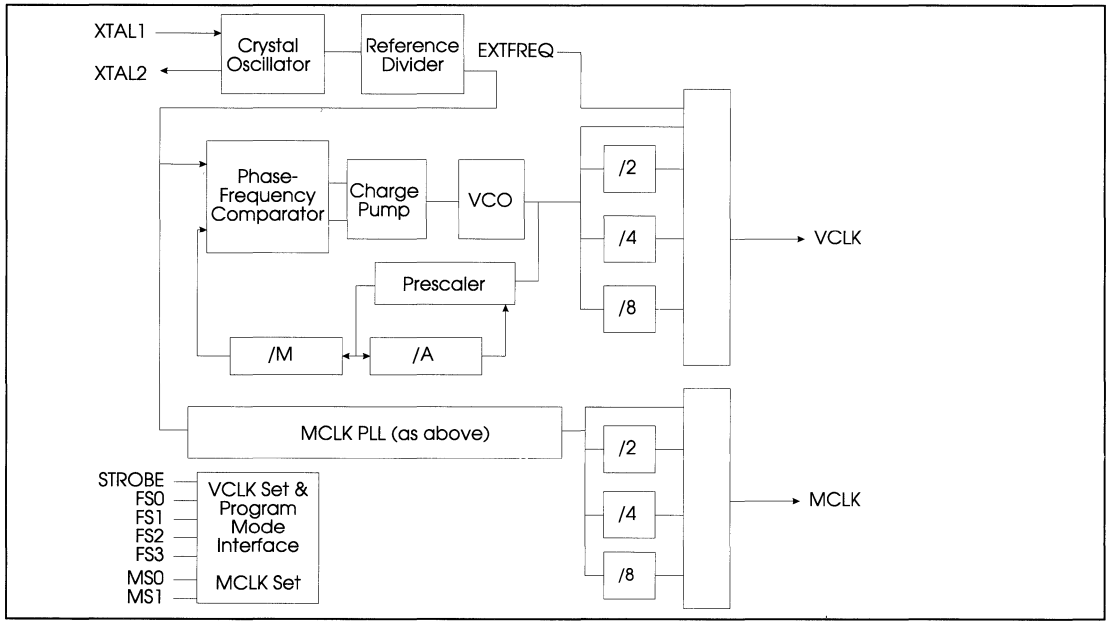
Features

- Advanced ICS monolithic phase-locked loop technology for extremely low jitter
- Supports high-resolution graphics - **VCLK** output to 145 MHz
- Completely integrated - requires only external crystal (or reference frequency and decoupling)
- Powerdown modes support portable computing
- Sixteen selectable **VCLK** frequencies (all user re-programmable)
- Four selectable **MCLK** frequencies (all user re-programmable)

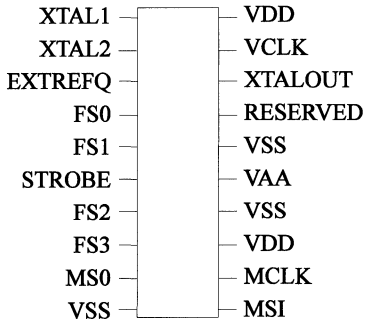
Applications

- PC Graphics
- VGA/Super VGA/XGA Applications.

Block Diagram



Pin Configuration



Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	XTAL1	A	Quartz crystal connection 1/Reference Frequency Input.
2	XTAL2	A	Quartz crystal connection 2.
3	EXTFREQ	I	External Frequency Input
4	FS0	I	VCLK PLL Frequency Select LSB.
5	FS1	I	VCLK PLL Frequency Select Bit.
7	FS2	I	VCLK PLL Frequency Select Bit.
8	FS3	I	VCLK PLL Frequency Select MSB.
6	STROBE	I	Control for Latch of VCLK Select Bits (FS0-FS3).
9	MS0	I	MCLK PLL Frequency Select LSB.
11	MS1	I	MCLK PLL Frequency Select MSB.
19	VCLK	O	VCLK Frequency Output
18	XTALOUT	O	Buffered Referenced Clock Output
12	MCLK	O	MCLK Frequency Output
17	RESERVED	-	Must Be Connected to VSS.
10, 14, 16	VSS	P	Device Ground. All pins must be connected.
13, 20	VDD	P	Output Stage Vdd. All pins must be connected.
15	VAA	P	Synthesizer Vdd.

Digital Inputs

The **FS0-FS3** pins and the **STROBE** pin are used to select the desired operating frequency of the **VCLK** output from the 16 pre-programmed/user-programmed selections in the **ICS2595**. These pins are also used to load new frequency data into the registers.

The standard interface for the **ICS2595** matches the interface of the industry standard ICS2494. That is, the FS0-FS3 inputs access the device internals transparently when the STROBE pin is high.

Optional configurations of the **STROBE** input include: positive-edge triggered, negative-edge triggered, and low-level transparent (see Ordering Information).

VCLK Output Frequency Selection

To change the **VCLK** output frequency, simply write the appropriate data to the **ICS2595 FS** inputs. Do not perform any further writes to the device for at least 50 milliseconds (assumes a 14.318 MHz reference). The synthesizer will output the new frequency programmed into that location after a brief delay (see time-out specifications).

Upon device power-up, the selected frequency will be the frequency pre-programmed into address 0 until a device write is performed.

MCLK Output Frequency Selection

The MS0-MS1 pins are used to directly select the desired operating frequency of the MCLK output from the four pre-programmed/user-programmed selections in the **ICS2595**. These inputs are not latched, nor are they involved with memory programming operations.

Programming Mode Selection

A programming sequence is defined as a period of at least 50 milliseconds (assumes 14.318 MHz reference) of no data writes to the **ICS2595** (to clear the shift register) followed by a series of data writes (as shown here):

FS0	FS1	FS2	FS3
X	X	**START** bit (must be "0")	0
X	X	"	1
X	X	**R/W*** control	0
X	X	"	1
X	X	**LO** (location LSB)	0
X	X	"	1
X	X	**L1**	0
X	X	"	1
X	X	**L2**	0
X	X	"	1
X	X	**L3**	0
X	X	"	1
X	X	**L4** (location MSB)	0
X	X	"	1
X	X	**N0** (feedback LSB)	0
X	X	"	1
X	X	**N1**	0
X	X	"	1
X	X	**N2**	0
X	X	"	1
X	X	**N3**	0
X	X	"	1
X	X	**N4**	0
X	X	"	1
X	X	**N5**	0
X	X	"	1
X	X	**N6**	0
X	X	"	1
X	X	**N7** (feedback MSB)	0
X	X	"	1
X	X	**EXTFREQ** bit (selected if "1")	0
X	X	"	1
X	X	**D0** (post-divider LSB)	0
X	X	"	1
X	X	**D1** (post-divider MSB)	0
X	X	"	1
X	X	**STOP1** bit (must be "1")	0
X	X	"	1
X	X	**STOP2** bit (must be "1")	0
X	X	"	1

Observe that the internal shift register is "clocked" by a transition of **FS3** data from "0" to "1". If an extended sequence of register loading is to be performed (such as a power-on initialization sequence), note that it is not necessary to implement the 50 millisecond delay between them. Simply repeat the sequence above as many times as desired. Writes to the FS port will not be treated as frequency select data until up to 50 milliseconds have transpired since the last write. Note that FS0 and FS1 inputs are "don't care."

Data Description

Location Bits (L0-L4)

The first five bits after the start bit control the frequency location to be re-programmed according to this table. The rightmost bit (the LSB) of the five shown in each selection of the table is the first one sent.

Table 1 - Location Bit Programming

L[4-0]	LOCATION
00000	VCLK Address 0
00001	VCLK Address 1
00010	VCLK Address 2
00011	VCLK Address 3
00100	VCLK Address 4
00101	VCLK Address 5
00110	VCLK Address 6
00111	VCLK Address 7
01000	VCLK Address 8
01001	VCLK Address 9
01010	VCLK Address 10
01011	VCLK Address 11
01100	VCLK Address 12
01101	VCLK Address 13
01110	VCLK Address 14
01111	VCLK Address 15
10000	MCLK Address 0
10001	MCLK Address 1
10010	MCLK Address 2
10011	MCLK Address 3

Feedback Set Bits (N0-N7)

These bits control the feedback divider setting for the location specified. The modulus of the feedback divider will be equal to the value of these bits + 257. The least significant bit (N0) is sent first.

Post-Divider Set Bits (D0-D1)

These bits control the post-divider setting for the location specified according to this table. The least significant bit (D0) is sent first.

Table 2 - Post-Divider Programming

D[1-0]	POST-DIVIDER
00	8
01	4
10	2
11	1

Read/Write* Control Bit

When set to a "0", the **ICS2595** shift register will transfer its contents to the selected memory register at the completion of the programming sequence outlined above.

When this bit is a "1", the selected memory location will be transferred to the shift register to permit a subsequent readback of data. No modification of device memory will be performed.

To readback any location of memory, perform a "dummy" write of data (complete with start and stop bits) to that location but set the **R/W*** control bit (make it "1"). At the end of the sequence (i.e. after the stop bits have been "clocked"), "clocking" of the FS3 input 11 more times will output the data bits only in the same sequence as above on the FS0 pin.

EXTFREQ Input

The **EXTFREQ** input allows an externally generated frequency to be routed to the VCLK or MCLK output pins under device programming control. If the EXTFREQ bit is set (logic "1") at the selected address location, the frequency applied to the **EXTFREQ** input will be routed to the output instead of the frequency generated by the **VCLK** (or MCLK) PLL.

When setting the EXTFREQ bit to a "1", be sure that the D0 and D1 bits are not both set to "1" also, unless it is intended that the phase-locked loop be shutdown as well.

Power Conservation

The **ICS2595** supports power conservation by permitting either or both of the phase-locked loops to be disabled. This can be done by programming a particular address to have EXTFREQ, D0, & D1 bits set to a logic "1". Any frequency applied to the EXTFREQ pin will still be passed through the output multiplexer and appear at the respective output.
The crystal oscillator is not affected by this powerdown function and will continue to operate normally.

Frequency Synthesizer Description

Refer to Figure 1 for a block diagram of the **ICS2595**.

The **ICS2595** generates its output frequencies using phase-locked loop techniques. The phase-locked loop (or PLL) is a closed-loop feedback system that drives the output frequency to be ratiometrically related to the reference frequency provided to the PLL. The phase-frequency detector shown in the block diagram drives the VCO to a frequency that will cause the two inputs to the phase-frequency detector to be matched in frequency and phase. This occurs when:

$$F_{VCO}=F_{XTALI}* \frac{N}{R}$$

where N is the effective modulus of the feedback divider chain and R is the modulus of the reference divider chain.

The feedback divider on the **ICS2595** may be set to any integer value from 257 to 512. This is done by the setting of the **N0-N7** bits. The standard reference divider on the **ICS2595** is fixed to a value of 43 (this may be set to a different value via ROM programming; contact factory). The **ICS2595** is equipped with a post-divider and multiplexer that allows the output frequency range to be scaled down from that of the VCO by a factor of 2, 4, or 8.

Therefore, the VCO frequency range will be from 5.976 to 11.906 (257/43 to 512/43) of the reference frequency. The output frequency range will be from 0.747 to 11.906 times the reference frequency. Worst case accuracy for any desired frequency within that range will be 0.2%.

If a 14.31818 MHz reference is used, the output frequency range would be from 10.697 MHz to 170.486 MHz (but the upper end is first limited to 145 MHz by the **ICS2595** output driver).

Programming Example

Suppose that we want differential CLK output to be 45.723 MHz. We will assume the reference frequency to be 14.31818 MHz.

The VCO frequency range will be 85.565 MHz to 170.486 MHz (5.976 * 14.31818 to 11.906 * 14.31818). We will need to set the post-divider to two to get an output of 45.723 MHz.

The VCO will then need to be programmed to two times 45.723 MHz, or 91.446 MHz. To calculate the required feedback divider modulus we divide the VCO frequency by the reference frequency and multiply by the reference divider:

$$\frac{91.446}{14.31818} *43=274.62$$

which we round off to 275. The exact output frequency will be:

$$\frac{275}{43} *14.31818* \frac{1}{2} =45.784 \text{ MHz}$$

The value of the **N** programming bits may be calculated by subtracting 257 from the desired feedback divider modulus. Thus, the **N** value will be set to 18 (275-257) or 00010010_2. The **D** bit programming is 10_2 (from Table 2).

Reference Oscillator & Crystal Selection

The **ICS2595** has on-board circuitry to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in parallel-resonant (also called anti-resonant mode). See the AC Characteristics for the effective capacitive loading to specify when ordering crystals.

Crystals characterized for their series-resonant frequency may also be used with the **ICS2595**. Be aware that the oscillation frequency in circuit will be slightly higher than the frequency that is stamped on the can (typically 0.025-0.05%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the **ICS2595** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

External Reference Sources

An external frequency source may be used as the reference for the VCLK and MCLK PLLs. To implement this, simply connect the reference frequency source to the XTAL1 pin of the **ICS2595**. For best results, insure that the clock edges are as clean and fast as possible and that the input voltage thresholds are not violated.

Power Supply

The **ICS2595** has three VSS pins to reduce the effects of package inductance. All pins are connected to the same potential on the die (the ground bus). ALL of these pins should connect to the ground plane of the video board as close to the package as is possible.

The **ICS2595** has two **VDD** pins which supply of +5 volt power to the output stages. These pins should be connected to the power plane (or bus) using standard high-frequency decoupling practice. That is, use low-capacitors should have low series inductance and be mounted close to the **ICS2595**.

The VAA pin is the power supply for the synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin (as shown in the recommended application circuitry). This will allow the PLL to "track" through power supply fluctuations without visible effects.

Absolute Maximum Ratings

Supply voltage ..... -.5V to +7V
Logic inputs ..... .5V to VDD +.5V
Ambient operating temp ..... 0 to 70°C
Storage temperature ..... -85 to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

DC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TTL-Compatible Inputs						
(VS0-3, MS0-1, STROBE):						
Input High Voltage	V_{ih}		2.0		VDD=0.5	V
Input Low Voltage	V_{il}		VSS-0.5		0.8	V
Input High Current	I_{ih}				10	uA
Input Low Current	I_{il}				200	uA
Input Capacitance	C_{in}				8	pF
XTAL1:						
Input High Voltage	Vxh		VDD*0.75		VDD+0.5	V
Input Low Voltage	Vxl		VSS-0.5		VDD*0.25	V
VCLK, MCLK Outputs:						
Output High Voltage	Voh		2.4			V
@Ioh=0.4mA						
Output Low Voltage	Vol				0.4	V
@Iol=8.0mA						

AC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Phase-Locked Loop:						
VCLK, MCLK VCO Frequency	Fvco		60		185	MHz
PLL Acquire Time	T_{lock}			500		uSec
Crystal Oscillator						
Crystal Frequency Range	F_{xtal}		5		25	MHz
Parallel Loading Capacitance				20		pF
XTAL1 Minimum High Time	Txhi		8			nSec
XTAL1 Minimum low Time	Txlo		8			nSec
Power Supplies:						
VDD Supply Current	idd				35	mA
VAA Supply Current	Iaa				10	mA
Digital Outputs:						
VCLK, MCLK, XTALOUT Rise Time @Cload=20pf	Tr				2	nSec
VCLK, MCLK, STALOUT Fall Time @Cload=20pf	Tf				2	nSec

Ordering Information

ICS2595N-SXX (0.300" DIP Package)
ICS2595M-SXX (0.300" SOIC Package)

where:
"s" denotes strobe option: A - positive level transparent (i.e., 2494 interface compatible)
B - negative level transparent
C - positive edge triggered
D - negative edge triggered

"xx" denotes default frequencies:

PATTERN	ICS2595-01			
Reference Divider	43			
VCLK ADDR	FbkDiv/PostDiv - F_{VCLK}(MHz)			
0	300/1- 99.89			
1	378/1 - 125.87			
2	277/1 - 92.24			
3	432/4 - 35.96			
4	302/2 - 50.28			
5	340/2 - 56.61			
6	EXTFREQ-			
7	270/2 - 44.95			
8	405/1 - 134.86			
9	384/4 - 31.97			
A	330/1 - 109.88			
B	481/2 - 80.08			
C	479/4 - 39.87			
D	270/2 - 44.95			
E	450/2 - 74.92			
F	390/2 - 64.93			
MCLK ADDR	FbkDiv/PostDiv - F_{MCLK}			
0	481/4 - 40.04			
1	270/2 - 44.95			
2	396/4 - 32.97			
3	300/2 - 49.95			

Integrated Circuit Systems, Inc.

ICS82C404

Advance Information

Dual Programmable Graphics Frequency Generator

B

Features

- **Pin for pin and function compatible with ICD's version of the 82C404**
- **Dual programmable graphics clock generator**
- **Memory and video clocks are individually programmable on-the-fly**
- **Ideal for designs where multiple or varying frequencies are required**
- **Increased frequency resolution from optional pre-divide by 2 on the M counter**
- **Output enable feature available for tri-stating outputs**
- **Independent clock outputs range from 390 kHz to 120 MHz**
- **Operation up to 140 MHz available**
- **Power-down capabilities**
- **Low power, high speed 0.8 μ CMOS technology**
- **Glitch-free transitions**
- **Available in 16 pin PDIP or SOIC package**

General Description

The ICS82C404 is a fully programmable graphics clock generator. It can generate user specified clock frequencies using an externally generated input reference or a single crystal. The output frequency is programmed by entering a 24 bit digital word through the serial port.

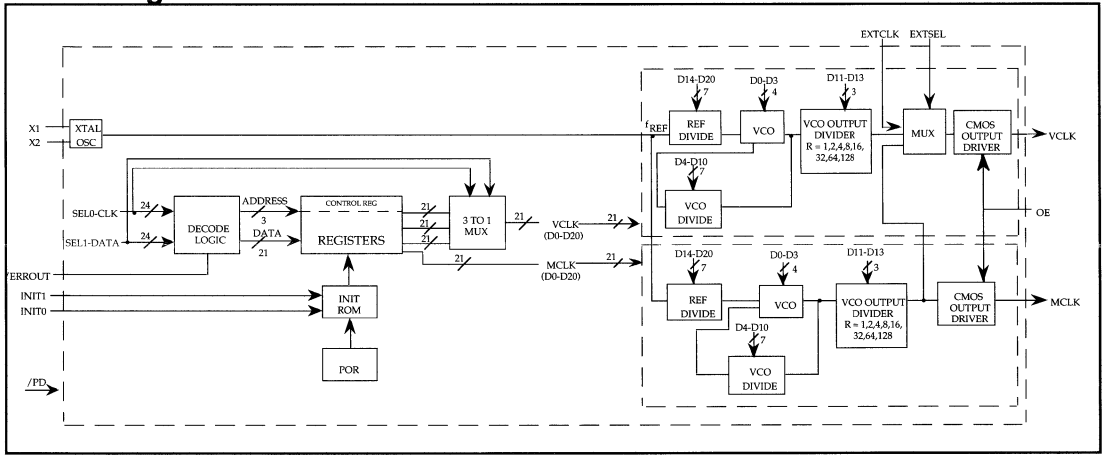
Two fully user-programmable phase-locked loops are offered in a single package. One PLL is designed to drive the memory clock, while the second drives the video clock. The outputs may be changed on-the-fly to any desired frequency between 390 kHz and 120 MHz. The ICS82C404 is ideally suited for any design where multiple or varying frequencies are required.

This part is ideal for graphics applications. It generates low jitter, high speed pixel clocks. It can be used to replace multiple, expensive high speed crystal oscillators. The flexibility of the device allows it to generate non-standard graphics clocks.

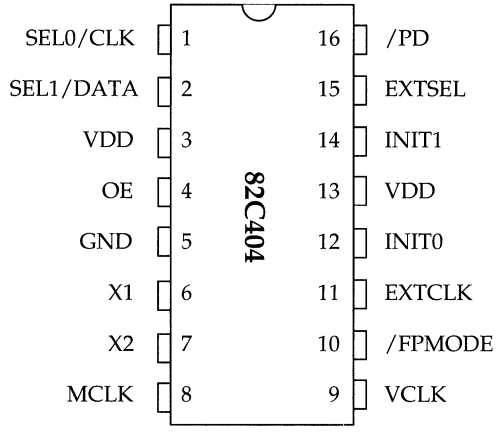
The ICS82C404 is much like the ICS9161 clock chip. For all pertinent timing diagrams, default registers, power management and programming information, see the ICS9161 data sheet. The only difference between the two devices is the pinout description and configuration – as described in the following two pages.

The leader in the area of multiple output clocks on a single chip, ICS has been shipping graphics frequency generators since October, 1990, and is constantly improving the phase locked loop. The ICS82C404 incorporates a patented fourth generation PLL that offers the best jitter performance available.

Block Diagram



Pin Configuration



Pin Description

Pin Name	Pin #	Description
SEL0-CLK	1	Clock input in serial programming mode Clock select pin in operating mode
SEL1-DATA	2	Data input in serial programming mode Clock select pin in operating mode
AVDD	3	Power
OE	4	Tri-states outputs when low
GND	5	Ground
X1	6	Crystal input
X2	7	Crystal output
MCLK	8	Memory clock output
VCLK	9	Video clock output
/FPMODE	10	Clock select input used to force REG2 programmed frequency
EXTCLK	11	External clock input
INIT0	12	Selects initial power-up conditions, LSB
VDD	13	Power
INIT1	14	Selects initial power-up conditions, MSB
EXTSEL	15	Selects external clock input (EXTCLK) as VCLK output
/PD	16	Power-down pin, active low

Register Definitions

The register file consists of the following six registers:

Register Addressing

Address	Register	Definition
000	REG0	Video Clock Register 1
001	REG1	Video Clock Register 2
010	REG2	Video Clock Register 3
011	MREG	Memory Register
100	PWRDWN	Divisor for Power-down mode
110	CNTL REG	Control Register

The ICS82C404 places the three video clock registers and the memory clock register in a known state upon power-up. The registers are initialized based on the state of the INIT1 and INIT0 pins at application of power to the device. The INIT pins must ramp up with VDD if a logical 1 on either pin is required. These input pins are internally pulled down and will default to a logical 0 if left unconnected.

The registers are initialized as follows:

Register Initialization

INIT1	INIT0	MREG	REG0	REG1	REG2
0	0	32.500	25.175	28.322	28.322
0	1	40.000	25.175	28.322	28.322
1	0	50.350	40.000	28.322	28.322
1	1	56.644	40.000	50.350	50.350

Register Selection

When the ICS82C404 is operating, the video clock output is controlled with a combination of the SEL0, SEL1, /PD, and OE pins. The video clock is also multiplexed to an external clock (EXTCLK) which can be selected with the EXTSEL pin. The VCLK Selection Table shows how VCLK is selected.

VCLK Selection

OE	/PD	EXTSEL	/FPMODE	SEL1	SEL0	VCLK
0	x	x	x	x	x	Tri-State
1	0	x	x	x	x	Forced High
1	1	x	1	0	0	REG0
1	1	x	1	0	1	REG1
1	1	0	1	1	0	EXTCLK
1	1	1	1	1	x	REG2
1	1	x	1	1	1	REG2
1	1	x	0	x	x	REG2

As seen in the table above, OE acts to tri-state the output. The /PD pin forces the VCLK signal high while powering down the part. The EXTCLK pin will only be multiplexed in when EXTSEL and SEL0 are logic 0 and SEL1 is a logic 1.

The memory clock outputs are controlled by /PD and OE as follows:

MCLK Selection

OE	/PD	MCLK
0	x	Tri-State
1	1	MREG
1	0	PWRDWN

The Clock Select pins SEL0 and SEL1 have two purposes. In serial programming mode, these pins act as the clock and data pins. New data bits come in on SEL1 and these bits are clocked in by a signal on SEL0. While these pins are acquiring new information, the VCLK signal remains unchanged. When SEL0 and SEL1 are acting as register selects, a timeout interval is required to determine whether the user is selecting a new register or wants to program the part. During this initial timeout, the VCLK signal remains at its previous frequency. At the end of this timeout interval, a new register is selected. A second timeout interval is required to allow the VCO to settle to its new value. During this period of time, typically 5 msec, the input reference signal is multiplexed to the VCLK signal.

When MCLK or the active VCLK register is being reprogrammed, then the reference signal is multiplexed glitch-free to the output during the first timeout interval. A second timeout interval is also required to allow the VCO to settle. During this period, the reference signal is multiplexed to the appropriate output signal.

Dual Video/Memory Clock Generator

Introduction

The Integrated Circuit Systems **ICS90C61A** is a dual clock generator for VGA applications. It simultaneously generates two clocks. One clock is for the video memory, and the other is the video dot clock.

This data sheet supplies sales order information, a functional overview, signal pin details, a block diagram, AC/DC characteristics, timing diagrams, and package mechanical information.

Description

The Integrated Circuit Systems Video Graphics Array Clock Generator (**ICS90C61A**) is capable of producing different output frequencies under firmware control. The video output frequency is derived from a 14.318 MHz system clock available in IBM PC/XT/AT and Personal System/2 computers. It is designed to work with Western Digital Imaging Video Graphics Array and 8514/A devices to optimize video subsystem performance.

The video dot clock output may be one of seven internally-generated frequencies or two external inputs. The selection of the video dot clock frequency is done through four inputs.

- SEL0
- SEL1
- VGATTL
- FCLKSEL

SEL0 and SEL1 are latched by the SELEN signal. VGATTL and FCLKSEL are used as direct inputs to the VCLK selection. Table 1-1 is the truth table for VCLK selection.

The input and truth table have been designed to allow a direct connection to one of the many Western Digital Imaging VGA controllers or 8514/A chip sets.

The MCLK output is one of four internally-generated frequencies as shown in Table 1-2. The various VCLK and MCLK frequencies are derived from the 14.318 MHz Input frequency.

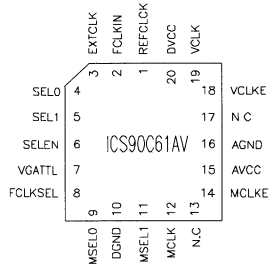
The VCLKE and MCLKE input can tristate the VCLK and MCLK outputs to facilitate board level testing.

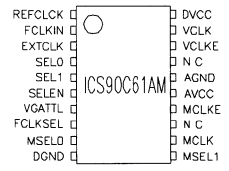
The **ICS90C61A** is capable of extended frequency output up to 80 MHz in custom applications. See page 5 for details.

Features

- Dual Clock generator for the IBM-compatible Western Digital Imaging Video Graphics Array (VGA) LSI devices, and 8514/A chip sets
- Integral loop filter components
- Generates seven video clock frequencies derived from a 14.318 MHz system clock reference frequency
- Video clock which is selectable among the seven internally generated clocks and two external clocks
- On-chip generation of four memory clock frequencies
- CMOS technology
- Available in 20-pin PLCC, SO, and DIP packages
- Extended frequency capabilities to 80 MHz in custom frequency patterns

Pin Configuration





Note ICS90C61AN (DIP) pinout is identical to ICS90C61AM (SO) pinout

Ordering Information

ICS90C61AV-PRx (PLCC Package)
ICS90C61AM-PRx (SO Package)
ICS90C61AN-PRx (DIP Package)
(PRx = Pattern Number)
Note: Unless a specific pattern is ordered, PR2 will be shipped

ICS90C61A VGA Interface

The **ICS90C61A** has two system interfaces: System Bus and VGA Controller, and six user-programmable inputs. Figure 2-1 shows how the Integrated Circuit Systems VGA Clock **ICS90C61A** is connected to a VGA controller. Western Digital Imaging VGA controllers normally have a status bit that indicates to the VGA controller that it is working with a clock chip. When working with a clock chip the VGA controller changes two of its clock inputs, VCLK1 and VCLK2, to outputs. These outputs are used to select the required video frequency.

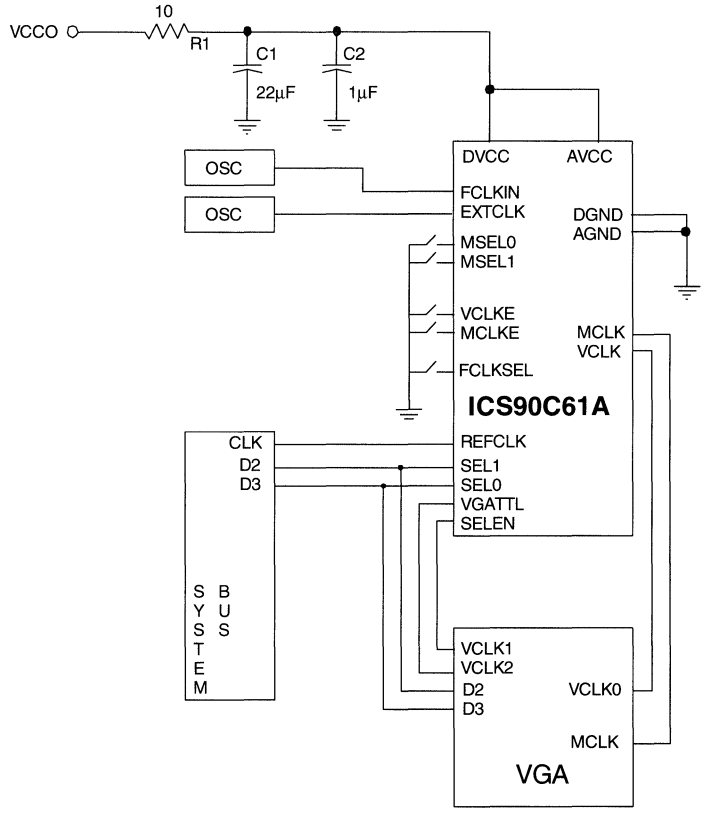


Figure 2-1 ICS 90C61A INTERFACE

Note:
C_2 should be placed as close as possible to the **ICS90C61A** AVCC pin.

System Bus Inputs

The system bus inputs are:

- REFCLK
- SEL0
- SEL1

The **ICS90C61A** uses the system bus 14.318 MHz clock as a reference to generate all its frequencies for both video and memory clocks. Data lines D2 and D3 are commonly used as inputs to VSEL0 and VSEL1 for video frequency selection.

Inputs from VGA Controller

The VGA controller input to the **ICS90C61A** is:

- SELEN

The **ICS90C61A** is programmed to generate different video clock frequencies using the inputs of SEL0, SEL1, VGATTL, and FCLKSEL. The signals VGATTL and FCLKSEL may be supplied by the VGA controller as is the case in Western Digital Imaging VGA controllers. The inputs SEL0-1 are latched with the signal SELEN. The SELEN input should be an active low pulse. This active low pulse is generated in Western Digital Imaging VGA controllers during I/O writes to internal register 3C2h.

Note: Only SEL0 and SEL1 are latched with signal SELEN.

Outputs to VGA Controller

The outputs from the **ICS90C61A** to the VGA controller are:

- MCLK
- VCLK

MCLK and VCLK are the two clock outputs to the VGA controller.

Analog Filters

The analog filters are integral to the **ICS90C61A** device. No external components are required. This feature reduces PC board space requirements and component costs. Phase jitter is reduced as externally-generated noise cannot easily influence the phase-locked loop filter.

User-Definable Inputs

The user-definable inputs are:

- EXTCLK
- FCLKIN
- VLCKE, MCLKE
- MSELO-1
- VGATTL, FCLKSEL

EXTCLK and FCLKIN are additional inputs that may be internally routed to the VCLK output. The additional inputs are useful for supporting modes that require frequencies not provided by the **ICS90C61A**.

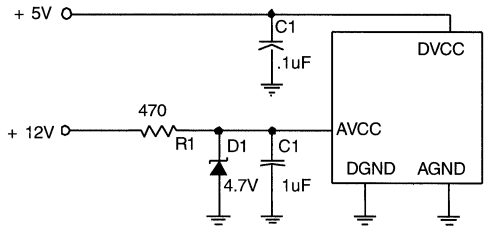
VCLKE and MCLKE are the output enable signals for VCLK and MCLK.When low, the respective output is tri-stated.

MSEL0-1 are the memory clock (MCLK) select lines. Table 1-2 shows how MCLK frequencies are selected. All signals in this group have internal pull-up resistors.

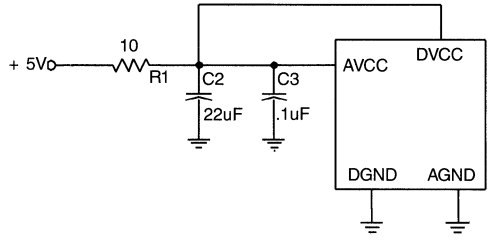
VGATTL and FCLKSEL are video clock (VCLK) select lines that can select additional VCLK frequencies. See Table 1-1.

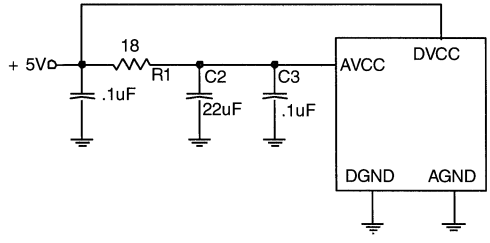
Power Considerations

The **ICS90C61A** product requires an AV_{CC} supply free of fast rise time transients. This requirement may be met in several ways and is highly dependent on the characteristics of the host system. A VGA adapter card is unique in that it must function in an unknown environment. + 5 Volt power quality is dependent not only on the quality of the power supply resident in the host system, but also on the other cards plugged into the host's backplane. Power supply noise ranges from fair to terrible. As the VGA adapter manufacturer has no control over this, he must assume the worst. The best solution is to create a clean + 5 Volts by deriving it from the + 12 Volt supply by using a zener diode and dropping resister. A 470 Ohm resistor and 4.7 Volt Zener diode are the least costly way to accomplish this. A .047 to .1 microfarad bypass capacitor tied from AV_{CC} to AGND insures good high-frequency decoupling of this point.



Laptop and notebook computers have entirely different problems with power. Typically they have no + 12 Volt supply; however, they are much quieter electrically. Because the designer has complete control of the system architecture, he can place sensitive components and systems such as the RAMDAC and Dual Video/Memory Clock away from DRAM and other noise-generating components. Most systems provide power that is clean enough to allow for jitter-free Dual Video/Memory Clock performance if the + 5 Volt supply is decoupled with a resistor and 22 microfarad Tantalum capacitor. Digital inputs that are desired to be held at static logical high level should not be tied to + 5 Volts as this will result in excessive current drain through the ESD protection diode. The internal pullup resistors will adequately keep these inputs high.





ICS90C61A Standard Patterns

FCLKSEL	VGATTL	SEL0	SEL1	VCLK FREQUENCY (MHz)
				ICS90C61A-PR2**
1	0	0	0	REFCLK
1	0	0	1	16.108
1	0	1	0	32.216
1	0	1	1	44.744
1	1	0	0	25.057
1	1	0	1	28.089
1	1	1	0	EXTCLK*
1	1	1	1	36.242
0	X	X	X	FCLKIN*

MSEL1	MSEL0	MCLK FREQUENCIES (MHz)
		ICS90C61A-PR2**
0	0	41.612
0	1	37.585
1	0	36.242
1	1	44.744

*Note: FCLKIN and EXTCLK may be programmed to output custom frequencies up to 80 MHz in applications which require this capability. Custom frequencies in these addresses require a significant volume committment and/or one-time mask charge. Contact ICS Sales for details.

**Note: If no "dash number" is specified, then the "– PR2" will be supplied since this version is completely compatible with the original WD90C61 frequency set.

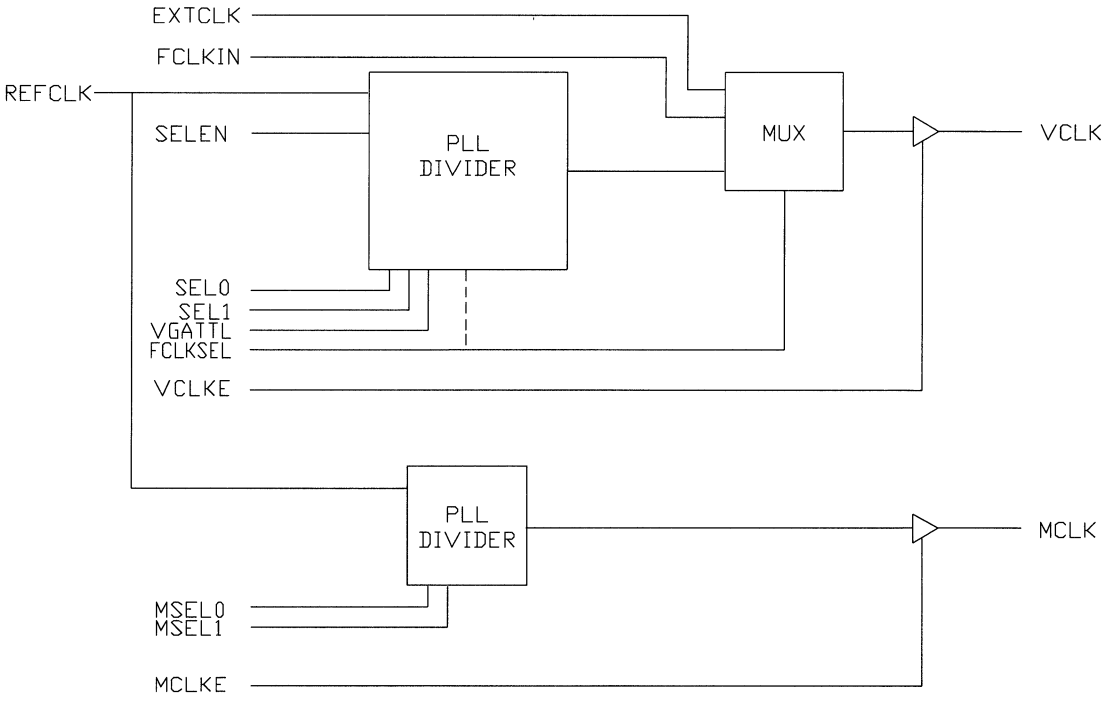


Figure 2-2 ICS90C61A FUNCTIONAL BLOCK DIAGRAM

Pin Descriptions

The following table provides the pin descriptions for the 20-pin **ICS90C61A** packages:

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
1	REFCLK	IN	Reference input clock from system
2	FCLKIN	IN	Feature clock input pin
3	EXTCLK	IN	External clock input for an additional frequency
4	SEL0	IN	Control input for VCLK selection
5	SEL1	IN	Control input for VCLK selection
6	SELEN	IN	Strobe for latching VSEL(0,1) *(Low enable)*
7	VGATTL	IN	Control input for VCLK selection
8	FCLKSEL	IN	Control input for FCLK selection
9	MSEL0	IN	Select input for MCLK selection
10	DGND	-	Ground for Digital Circuit
11	MSEL1	IN	Select input for MCLK selection
12	MCLK	OUT	Memory Clock Output
13	N.C.	-	No Connection
14	MCLKE	IN	Enable input for MCLK output *(high enables output)*
15	AVCC	-	Power supply for analog circuit
16	AGND	-	Ground for analog circuit
17	N.C.	-	No Connection
18	VCLKE	IN	Enable input for VCLK output *(high enables output)*
19	VCLK	OUT	Video Clock Output
20	DVCC	-	Power supply for Digital Circuit

NOTE:

CLK1, EXTCLK, FCLKIN, SEL0, SEL1,VGATTL, FCLKSEL, SELEN, MSEL0, MSEL1, VCLKE, and MCLKE - input pins have internal pullup resistors.

Absolute Maximum Ratings

Ambient temperature under bias	0 °C to 70 °C
Storage temperature	-40 °C to 125 °C
Voltage on all inputs and outputs with respect to V_{SS}	0.5 to 7 Volts

Note: Stresses above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (OV Ground). Positive current flows into the referenced pin.

Operating temperature range	0 °C to 70 °C
Power supply voltage	4.75 to 5.25 Volts

DC Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS	PINS
V_{IL}	Input Low Voltage	V_{SS}	0.8	V	V_{CC} = 5V	SEL0-1, SELEN, VGATTL, MSEL0-1, FCLKSEL, VCLKE, MCLKE, EXTCLK
V_{IH}	Input High Voltage	2.0	V_{CC}	V	V_{CC} = 5V	SEL0-1, SELEN, VGATTL, MSEL0-1, FCLKSEL, VCLKE, MCLKE, EXTCLK
V_{IL}	Input Low Voltage	V_{SS}	1.5	V	V_{CC} = 5V	FCLKIN
V_{IH}	Input High Voltage	V_{CC} -1.5	V_{CC}	V	V_{CC} = 5V	FCLKIN
I_{IH}	Input Leakage Current	-	20	µA	V_{in} = V_{CC}	
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 6.0 mA	
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = 4.0 mA	
I_{CCD}	Digital Supply Current	-	35	mA	V_{CC} = 5V, C_L = 15pF	
I_{CCA}	Analog Supply Current	-	10	mA	V_{CC} = 5V	
R_{UP}	Internal Pullup Resistors	25	-	K ohms	V_{CC} = 5V	
C_{in}	Input Pin Capacitance	-	8	pF	F_C = 1 MHz	
C_{out}	Output Pin Capacitance	-	12	pF	F_C = 1 MHz	

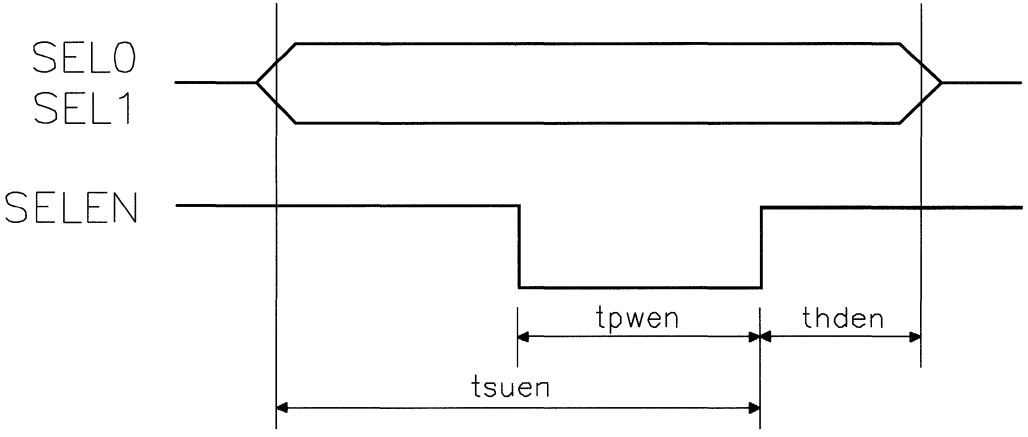
AC Timing Characteristics

The following notes apply to all of the parameters presented in this section.

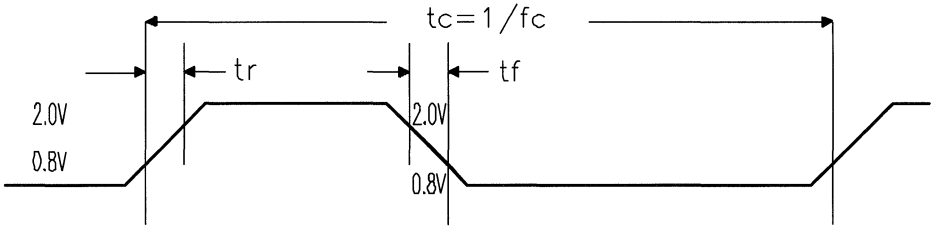
1. REFCLK = 14.318 MHz
2. T_C = 1/F_C
3. All units are in nanoseconds (ns).
4. Maximum jitter is within a range of 30 μ s after triggering on a 400 MHz scope.
5. Rise and fall time between 0.8 and 2.0 VDC.
6. Output pin loading = 15pF
7. Duty cycle is measured at 1.4V

SYMBOL	PARAMETER	MIN	MAX	NOTES
	SELEN TIMING			
T_{pwen}	Enable Pulse Width	20	-	
T_{suen}	Setup Time Data to Enable	20	-	
T_{hden}	Hold Time Data to Enable	10	-	
	REFERENCE INPUT CLOCK			
Tr	Rise Time	-	10	Phase-Jitter 1 ns max.
Tf	Fall Time	-	10	Duty Cycle 42.5% min. to 57.5% max.
	MCLK and VCLK TIMINGS			
Tr	Rise Time	-	3	Phase-Jitter 3 ns max.
Tf	Fall Time	-	3	Duty Cycle 40% min. to 60% max.
-	Frequency Error		1.0	%
-	Maximum Frequency		80	MHz
-	Propagation Delay for Pass Through Frequency	-	20	ns
-	Output Enable to Tri-State (into and out of) time		15	ns

ENABLE TIMING



CLOCK WAVEFORM



Dual Video/Memory Clock Generator

Introduction

The Integrated Circuit Systems **ICS90C64A** is a dual clock generator for VGA applications. It simultaneously generates two clocks. One clock is for the video memory, and the other is the video dot clock.

This data sheet supplies sales order information, a functional overview, signal pin details, a block diagram, AC/DC characteristics, timing diagrams, and package mechanical information.

Description

The Integrated Circuit Systems Video Graphics Array Clock Generator (**ICS90C64A**) is capable of producing different output frequencies under firmware control. The video output frequency is derived from a 14.318 MHz system clock available in IBM PC/XT/AT and Personal System/2 computers. It is designed to work with Western Digital Imaging Video Graphics Array and 8514/A devices to optimize video subsystem performance.

The video dot clock output may be one of fifteen internally-generated frequencies or one external input. The selection of the video dot clock frequency is done through four inputs.

- VSEL0
- VSEL1
- VSEL2
- VSEL3

VSEL0 and VSEL1 are latched by the SELEN signal. VSEL2 and VSEL3 are used as direct inputs to the VCLK selection. Table 1-1 is the truth table for VCLK selection.

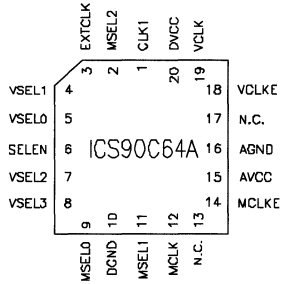
The input and truth table have been designed to allow a direct connection to one of the many Western Digital Imaging VGA controllers or 8514/A chip sets.

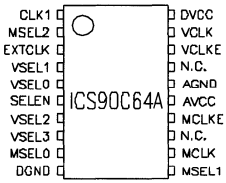
The MCLK output is one of eight internally-generated frequencies as shown in Table 1-2. The various VCLK and MCLK frequencies are derived from the 14.318 MHz Input frequency.

The VCLKE and MCLKE input can tristate the VCLK and MCLK outputs to facilitate board level testing.

Features

- Improved compatibility with Western Digital Controllers
- 100% backward compatible with ICS90C63 and ICS90C64
- Dual Clock generator for the IBM compatible Western Digital Imaging Video Graphics Array (VGA) LSI devices, and 8514/A chip sets
- Integral loop filter components. Reduce cost and phase-jitter
- Generates 15 video clock frequencies (including 25.175 and 28.322 MHz) derived from a 14.318 MHz system clock reference frequency
- On-chip generation of eight memory clock frequencies.
- Video clock is selectable among the fifteen internally generated clocks and one external clock
- CMOS technology
- Available in 20-pin PLCC, SO, and DIP packages





Note: ICS90C64AN (DIP) pinout is identical to ICS90C64AM (SO) pinout.

Ordering Information

ICS90C64AV-XXX (PLCC Package)
ICS90C64AM-XXX (SO Package)
ICS90C64AN-XX (DIP Package)
XXX = (Pattern number)

ICS90C64A VGA Interface

The **ICS90C64A** has two system interfaces: System Bus and VGA Controller, as well as analog filters and seven user programmable inputs. Figure 2-1 shows how the Integrated Circuit Systems VGA Clock **ICS90C64A** is connected to a VGA controller. Western Digital Imaging VGA controllers normally have a status bit that indicates to the VGA controller that it is working with a clock chip. When working with a clock chip the VGA controller changes two of its clock inputs, VCLK1 and VCLK2, to outputs. These outputs are used to select the required video frequency.

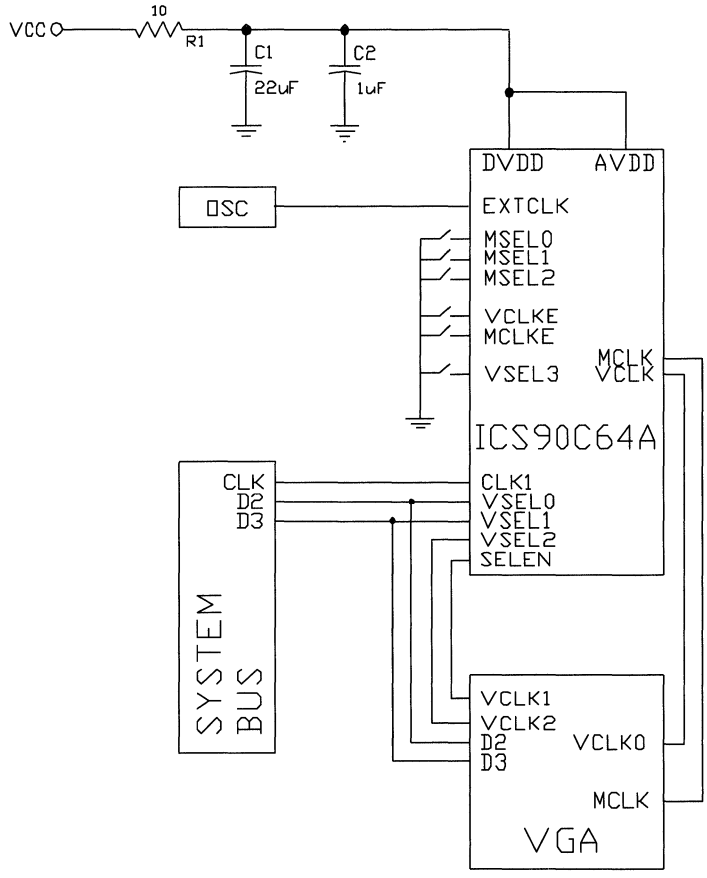


FIGURE 2-1 ICS90C64A INTERFACE

Note:

C_2 should be placed as close as possible to the ICS90C64A AVDD pin.

System Bus Inputs

The system bus inputs are:

- CLK1
- VSEL0
- VSEL1

The **ICS90C64A** uses the system bus 14.318 MHz clock as a reference to generate all its frequencies for both video and memory clocks. Data lines D2 and D3 are commonly used as inputs to VSEL0 and VSEL1 for video frequency selection.

Inputs from VGA Controller

The VGA controller input to the **ICS90C64A** is:

- SELEN

The **ICS90C64A** is programmed to generate different video clock frequencies using the inputs of VSEL0, VSEL1, VSEL2, and VSEL3. The signals VSEL2 and VSEL3 may be supplied by the VGA controller as is the case in Western Digital Imaging VGA controllers. The inputs VSEL0-1 are latched with the signal SELEN. The SELEN input should be an active low pulse. This active low pulse is generated in Western Digital Imaging VGA controllers during I/O writes to internal register 3C2h.

Note: Only VSEL0 and VSEL1 are latched with signal SELEN.

Outputs to VGA Controller

The outputs from the **ICS90C64A** to the VGA controller are:

- MCLK
- VCLK

MCLK and VCLK are the two clock outputs to the VGA controller.

Analog Filters

The analog filters are integral to the **ICS90C64A** device. No external components are required. This feature reduces PC board space requirements and component costs. Phase-jitter is reduced as externally-generated noise cannot easily influence the phase-locked loop filter.

User-Definable Inputs

The user-definable inputs are:

- EXTCLK
- VLCKE, MCLKE
- MSELO-2
- VSEL2, VSEL3

EXTCLK is an additional input that may be internally routed to the VCLK output. This additional input is useful for supporting modes that require frequencies not provided by the **ICS90C64A**.

VCLKE and MCLKE are the output enable signals for VCLK and MCLK. When low, the respective output is tri-stated.

MSEL0-2 are the memory clock (MCLK) select lines. Table 1-2 shows how MCLK frequencies are selected. All signals in this group have internal pull-up resistors.

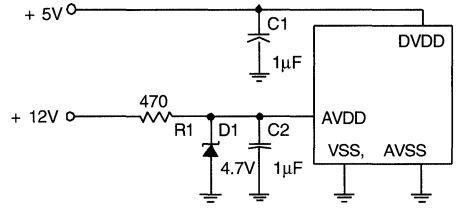
VSEL2 and VSEL3 are video clock (VCLK) select lines that can select additional VCLK frequencies. See Table 1-1.

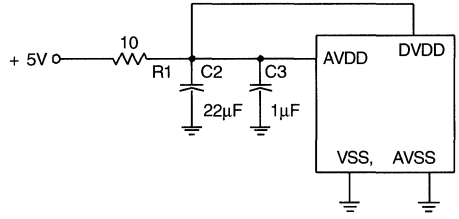
VSEL2 and VSEL3 have internal pullups.

Power Considerations

The **ICS90C64A** product requires an AV_{DD} supply free of fast rise time transients. This requirement may be met in several ways and is highly dependent on the characteristics of the host system. A VGA adapter card is unique in that it must function in an unknown environment. + 5 Volt power quality is dependent not only on the quality of the power supply resident in the host system, but also on the other cards plugged into the host's backplane. Power supply noise ranges from fair to terrible. As the VGA adapter manufacturer has no control over this, he must assume the worst. The best solution is to create a clean + 5 Volts by deriving it from the + 12 Volt supply by using a zener diode and dropping resistor. A 470 Ohm resistor and 5.1 Volt Zener diode are the least costly way to accomplish this. A .047 to .1 microfarad bypass capacitor tied from AV_{DD} to AVss insures good high-frequency decoupling of this point.

Laptop and notebook computers have entirely different problems with power. Typically they have no + 12 Volt supply; however, they are much quieter electrically. Because the designer has complete control of the system architecture, he can place sensitive components and systems such as the RAMDAC and Dual Video/Memory Clock away from DRAM and other noise-generating components. Most systems provide power that is clean enough to allow for jitter-free Dual Video/Memory Clock performance if the + 5 Volt supply is decoupled with a resistor and 22 microfarad Tantalum capacitor. Digital inputs that are desired to be held at a static logical high level should not be tied to + 5 Volts as this will result in excessive current drain through the ESD protection diode. The internal pullup resistors will adequately keep these inputs high.





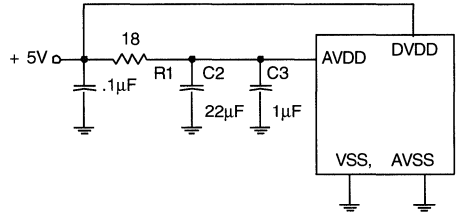


Table 1-1 VCLK SELECTION

3	2	1	0	VCLK Frequency (MHz)			
				ICS90C64A	ICS90C64A-903	ICS90C64A-907	ICS90C64A-909
0	0	0	0	30.0	30.0	30.250	30.0
0	0	0	1	77.25	77.25	77.25	77.25
0	0	1	0	EXTCLK	EXTCLK	EXTCLK	EXTCLK
0	0	1	1	80.0	80.0	80.0	80.0
0	1	0	0	31.5	31.5	31.5	31.5
0	1	0	1	36.0	36.0	35.5	36.0
0	1	1	0	75.0	7.50	75.0	75.0
0	1	1	1	50.0	50.0	72.0	50.0
1	0	0	0	40.0	40.0	40.0	40.0
1	0	0	1	50.0	50.0	50.0	50.0
1	0	1	0	32.0	32.0	32.0	32.0
1	0	1	1	44.9	44.9	44.9	44.9
1	1	0	0	25.175	25.175	25.175	25.175
1	1	0	1	28.322	28.322	28.322	28.322
1	1	1	0	65.0	65.0	65.0	65.0
1	1	1	1	36.0	36.0	36.0	36.0

Table 1-2 MCLK SELECTION

2	1	0	MCLK Frequencies (MHz)			
			ICS90C64A	ICS90C64A-903	ICS90C64A-907	ICS90C64A-909
0	0	0	33.0	33.0	65.0	75.0
0	0	1	49.218	49.218	49.218	40.0
0	1	0	60.0	60.0	60.0	45.0
0	1	1	30.5	30.5	62.5	50.0
1	0	0	41.612	41.612	41.612	55.0
1	0	1	37.5	37.5	37.5	60.0
1	1	0	36.0	36.0	55.0	65.0
1	1	1	44.296	44.296	44.296	70.0

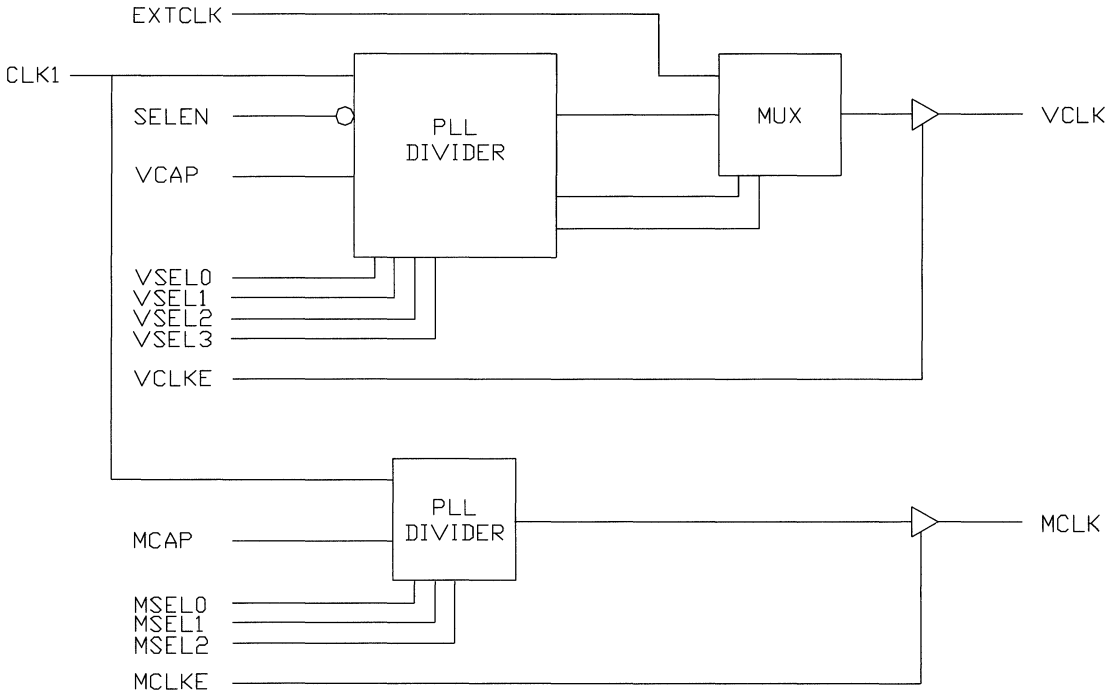


FIGURE 2-2 ICS90C64A FUNCTIONAL BLOCK DIAGRAM

Pin Descriptions

The following table provides the pin descriptions for the 20-pin **ICS90C64A** packages.

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
1	CLK1	IN	Reference input clock from system
2	MSEL2	IN	Select input for MCLK selection
3	EXTCLK	IN	External clock input for an additional frequency
4	VSEL1	IN	Control input for VCLK selection
5	VSEL0	IN	Control input for VCLK selection
6	SELEN	IN	Strobe for latching VSEL(0,1) *(Low enable)*
7	VSEL2	IN	Control input for VCLK selection
8	VSEL3	IN	Control input for VCLK selection
9	MSEL0	IN	Select input for MCLK selection
10	DGND	-	Ground for Digital Circuit
11	MSEL1	IN	Select input for MCLK selection
12	MCLK	OUT	Memory Clock Output
13	N.C.	-	No connection
14	MCLKE	IN	Enable input for MCLK output *(high enables output)*
15	AVDD	-	Power supply for analog circuit
16	AGND	-	Ground for analog circuit
17	N.C.	-	No connection
18	VCLKE	IN	Enable input for VCLK output *(high enables output)*
19	VCLK	OUT	Video Clock Output
20	DVDD	-	Power supply for Digital Circuit

Note:
CLK1, EXTCLK,VSEL0, VSEL1,VSEL2, VSEL3, SELEN, MSEL0, MSEL1, MSEL2, VCLKE, and MCLKE - input pins have internal pullup resistors.

Absolute Maximum Ratings

Ambient Temperature under bias	0 °C to 70 °C
Storage temperature	-40 °C to 125 °C
Voltage on all inputs and outputs with respect to V_{SS}	0.5 to 7 Volts

Note: Stresses above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (OV Ground). Positive current flows into the referenced pin.

Operating Temperature range	0 °C to 70 °C
Power supply voltage	4.75 to 5.25 Volts

DC Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage	V_{SS}		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{DD}	V	
I_{IH}	Input Leakage Current	-		10	µ A	V_{in} = V_{DD}
V_{OL}	Output Low Voltage	-		0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output High Voltage	V_{DD}-.4		-		I_{OH} = 4.0mA
V_{OH}	Output High Voltage	2.4		-	V	I_{OH} = 8.0 mA
I_{CC}	Supply Current	-	20	28	mA	No load VCLK = 28 MHz MCLK = 40 MHz
I_{CC}	Supply Current	-	27	35	mA	No load VCLK = 80 MHz MCLK = 40 MHz
R_{UP}	Internal Pullup Resistors	50		-	K ohms	V_{DD} = 5V
C_{in}	Input Pin Capacitance	-		8	pF	F_C = 1 MHz
C_{out}	Output Pin Capacitance	-		12	pF	F_C = 1 MHz

AC Timing Characteristics

The following notes apply to all of the parameters presented in this section:

1. REFCLK = 14.318 MHz
2. T_C = 1/F_C
3. All units are in nanoseconds (ns), unless labeled otherwise.
4. Output pin loading = 15pF

SYMBOL	PARAMETER	MIN	TYP	MAX	NOTES
	SELEN TIMING				
T_{pwen}	Enable Pulse Width	20			
T_{suen}	Setup Time Data to Enable	20			
T_{hden}	Hold Time Data to Enable	10			
	Reference Input Clock				
Tr	Rise Time			10	Phase-Jitter 1 ns max.
Tf	Fall Time			10	Duty Cycle 42.5% min. to 57.5% max.
	MCLK and VCLK TIMINGS				
Tr	Rise Time		.9	1.5	.8V-2.0V*
Tf	Fall Time		.9	1.5	2.0V-.8V
Tr	Rise Time		1.2	2.0	.3 V_{DD}-.7 V_{DD}
Tf	Fall Time		1.2	2.0	.7 V_{DD}-.3 V_{DD}
T_{high}	Duty Cycle	50%		60%	1.4V Switch Point
T_{high}	Duty Cycle	45%		55%	V_{DD}/2 Switch Point
	Frequency Error			0.5	%
	Maximum Frequency			135	MHz
	Propagation Delay for Pass Through Frequency			20	ns
	Output Enable to Tri-State (into and out of) time			15	ns

* WD90C11 Video Controller is designed with TTL level input thresholds on the inputs driven by the ICS90C64A VCLK and MCLK outputs. The later controllers (WD90C20, WD90C22, WD90C26, WD90C30, and WD90C31) are designed with input switch points of VCC/2 (CMOS)

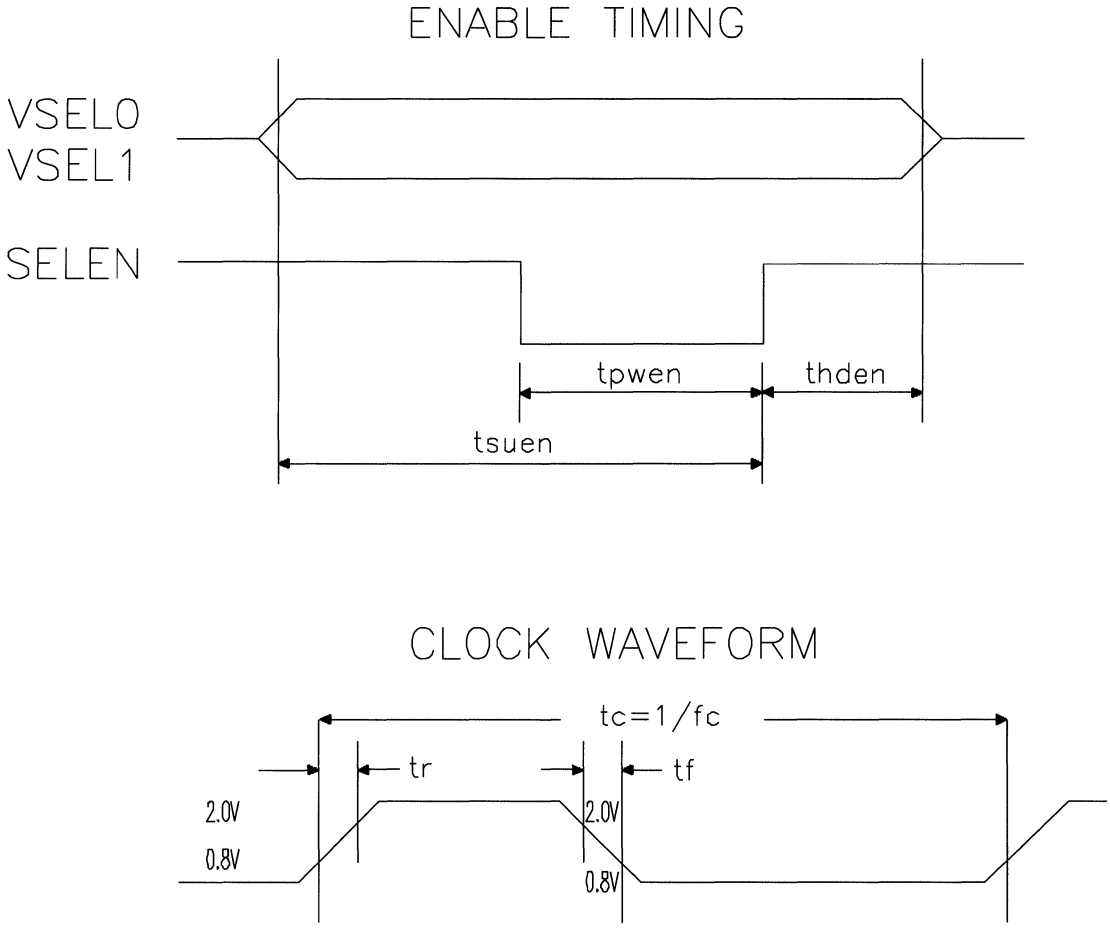


FIGURE 5-1 ICS90C64A TIMING

Dual Voltage Video/Memory Clock Generator

Introduction

The Integrated Circuit Systems **ICS90C65** is a dual clock generator for VGA applications. It simultaneously generates two clocks. One clock is for the video memory, and the other is the video dot clock.

The **ICS90C65** has been specifically designed to serve the portable PC market with operation at either 3.3V or 5V with a comprehensive power-saving shut-down mode.

This data sheet supplies sales order information, a functional overview, signal pin details, a block diagram, AC/DC characteristics, timing diagrams, and package mechanical information.

Description

The Integrated Circuit Systems Video Graphics Array Clock Generator (**ICS90C65**) is capable of producing different output frequencies under firmware control. The video output frequency is derived from a 14.318 MHz system clock available in IBM PC/XT/AT and Personal System/2 computers. It is designed to work with Western Digital Imaging Video Graphics Array and 8514/A devices to optimize video subsystem performance.

The video dot clock output may be one of 15 internally-generated frequencies or one external input. The selection of the video dot clock frequency is done through four inputs.

- VSEL0
- VSEL1
- VSEL2
- VSEL3

VSEL0 and VSEL1 are latched by the SELEN signal. VSEL2 and VSEL3 are used as direct inputs to the VCLK selection. Table 1-1 is the truth table for VCLK selection.

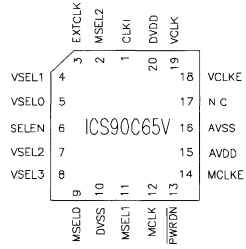
The input and truth table have been designed to allow a direct connection to one of the many Western Digital Imaging VGA controllers or 8514/A chip sets.

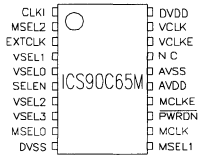
The MCLK output is one of eight internally-generated frequencies as shown in Table 1-2. The various VCLK and MCLK frequencies are derived from the 14.318 MHz Input frequency.

The VCLKE and MCLKE input can tristate the VCLK and MCLK outputs to facilitate board level testing.

Features

- Specified for dual voltage operation (V_{DD}= 3.3V or 5V), but operates continuously from 3.0V to 5.25V
- Designed to be powered down for extended battery life
- Backward compatibility to the ICS90C64 and ICS90C63
- Dual Clock generator for the IBM-compatible Western Digital Imaging Video Graphics Array (VGA) LSI devices, and 8514/A chip sets
- Integral loop filter components, reduce cost and phase jitter
- Generates fifteen video clock frequencies (including 25.175 and 28.322 MHz) derived from a 14.318 MHz system clock reference frequency
- On-chip generation of eight memory clock frequencies
- Video clock is selectable among the 15 internally generated clocks and one external clock
- CMOS technology
- Available in 20-pin PLCC, SO and DIP packages





Note: ICS90C65N (DIP) pinout is identical to ICS90C65M (SO) pinout.

Ordering Information

ICS90C65V-XXX (PLCC Package)
ICS90C65M-XXX (SO Package)
ICS90C65N-XXX (DIP Package)
(XXX = Pattern number)

ICS90C65 VGA Interface

The **ICS90C65** has two system interfaces: System Bus and VGA Controller, as well as other programmable inputs. Figure 1 shows how the Integrated Circuit Systems' VGA Clock **ICS90C65** is connected to a VGA controller. Western Digital Imaging VGA controllers normally have a status bit that indicates to the VGA controller that it is working with a clock chip. When working with a clock chip the VGA controller changes two of its clock inputs to outputs. They are theVCLK1/VCSLD/VCSEL and VCLK2/VCSEL/ VCSELH outputs and they are used to select the required video frequency.

When the powerdown capabilities are used, the control signal for PWRDN is normally held in one of a group of latches. If the powerdown function is not to be used, PWRDN must be tied to V_{DD}, otherwise the internal pull down will place the chip in the powerdown mode.

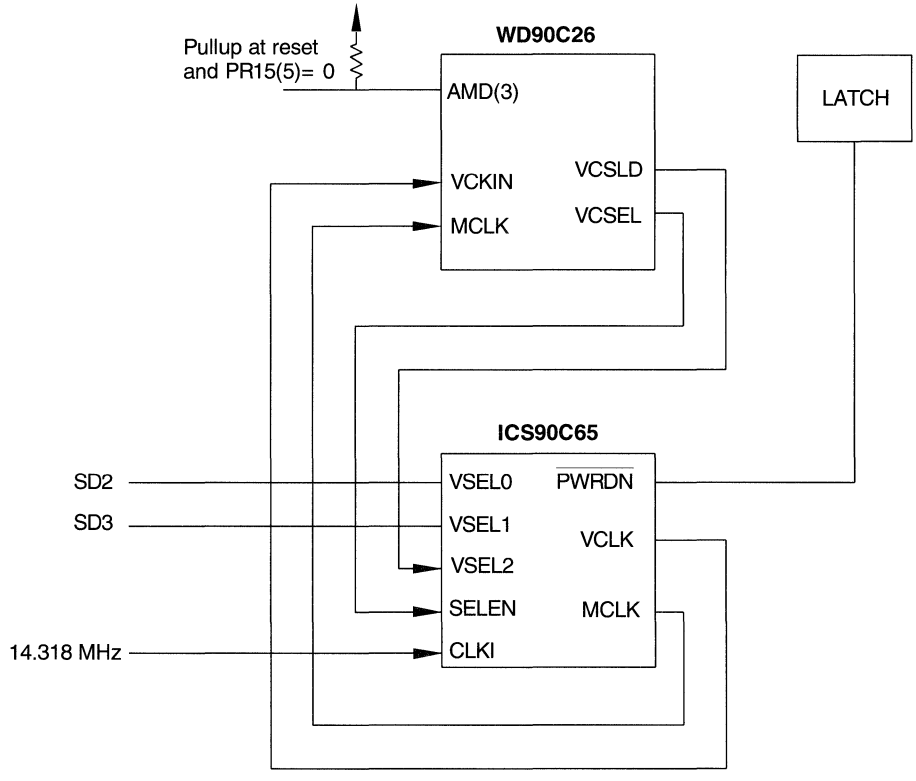


Figure 1

System Bus Inputs

The system bus inputs are:

- CLKI
- VSEL0
- VSEL1

The **ICS90C65** uses the system bus 14.318 MHz clock as a reference to generate all its frequencies for both video and memory clocks. Data lines D2 and D3 are commonly used as inputs to VSEL0 and VSEL1 for video frequency selection.

Inputs from VGA Controller

The VGA controller input to the **ICS90C65** is:

- SELEN

The **ICS90C65** is programmed to generate different video clock frequencies using the inputs of VSEL0, VSEL1, VSEL2, and VSEL3. The signals VSEL2 and VSEL3 may be supplied by the VGA controller as is the case in Western Digital Imaging VGA controllers. The inputs VSEL0-1 are latched with the signal SELEN. The SELEN input should be an active low pulse. This active low pulse is generated in Western Digital Imaging VGA controllers during I/O writes to internal register 3C2h.

Note: Only VSEL0 and VSEL1 are latched with signal SELEN.

Outputs to VGA Controller

The outputs from the **ICS90C65** to the VGA controller are:

- MCLK
- VCLK

MCLK and VCLK are the two clock outputs to the VGA controller.

Analog Filters

The analog filters are integral to the **ICS90C65** device. No external components are required. This feature reduces PC board space requirements and component costs. Phase-jitter is reduced as externally-generated noise cannot easily influence the phase-locked loop filter.

User-Definable Inputs

The user definable inputs are:

- EXTCLK
- VLCKE, MCLKE
- MSELO-2
- VSEL2, VSEL3
- $\overline{\text{PWRDN}}$

EXTCLK is an additional input that may be internally routed to the VCLK output. This additional input is useful for supporting modes that require frequencies not provided by the **ICS90C65** or for use during board test.

VCLKE and MCLKE are the output enable signals for VCLK and MCLK. When low the respective output is tri-stated.

MSEL0-2 are the memory clock (MCLK) select lines. Table 1-2 shows how MCLK frequencies are selected. All signals in this group have internal pull-up resistors.

VSEL2 and VSEL3 are video clock (VCLK) select lines that can select additional VCLK frequencies. See Table 1-1.

VSEL2 and VSEL3 have internal pullups.

$\overline{\text{PWRDN}}$ can place the **ICS90C65** in a powerdown mode which drops its supply current requirement below 1 microamp. When placed in this mode, the digital inputs may be either high or low or floating without causing an increase in the **ICS90C65** supply current.

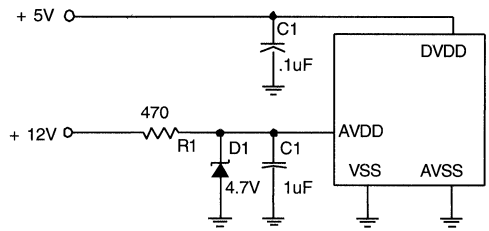
The $\overline{\text{PWRDN}}$ pin must be low (It has an internal pulldown.) in order to place the device in its low power state. The output pins (VCLK and MCLK) are driven high by the **ICS90C65** when it is in its low power state.

If CLKI is being driven by an external source, it may be driven low or high without a power penalty. If CLKI is at an intermediate voltage (V_{SS}+ 0.5 < V_{IN} < V_{DD}-0.5), there will be a small increase in supply current. If CLKI is driven at 14.318 MHz while the chip is in powerdown, the **ICS90C65** supply current will increase to approximately 1.2 mA.

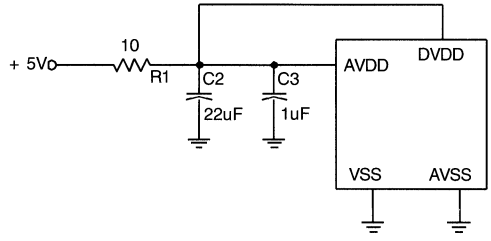
The SELEN (pin 6) may be used to guard against inadvertent frequency changes during powerdown/powerup sequences. By holding the SELEN low during powerdown and powerup sequences, the **ICS90C65** will retain the most recent video frequency selection.

Power Considerations

The **ICS90C65** product requires an AV_{DD} supply free of fast rise time transients. This requirement may be met in several ways and is highly dependent on the characteristics of the host system. A VGA adapter card is unique in that it must function in an unknown environment. + 5 Volt power quality is dependent not only on the quality of the power supply resident in the host system, but also on the other cards plugged into the host's backplane. Power supply noise ranges from fair to terrible. As the VGA adapter manufacturer has no control over this, he must assume the worst. The best solution is to create a clean + 5 Volts by deriving it from the + 12 Volt supply by using a zener diode and dropping resistor. A 470 Ohm resistor and 5.1 Volt Zener diode are the least costly way to accomplish this. A .047 to .1 microfarad bypass capacitor tied from AV_{DD} to A_{VSS} insures good high- frequency decoupling of this point.



Laptop and notebook computers have entirely different problems with power. Typically they have no + 12 Volt supply; however, they are much quieter electrically. Because the designer has complete control of the system architecture, he can place sensitive components and systems such as the RAMDAC and Dual Video/Memory Clock away from DRAM and other noise-generating components. Most systems provide power that is clean enough to allow for jitter-free Dual Video/Memory Clock performance if the + 5 Volt supply is decoupled with a resistor and 22 microfarad Tantalum capacitor. Digital inputs that are desired to be held at a static logical high level should not be tied to + 5 Volts as this may result in excessive current drain through the ESD protection diode. The internal pullup resistors will adequately keep these inputs high.



Pin Descriptions

The following table provides the pin descriptions for the 20-pin **ICS90C65** packages.

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
1	CLKI	IN	Reference input clock from system
2	MSEL2	IN	Select input for MCLK selection
3	EXTCLK	IN	External clock input for an additional frequency
4	VSEL1	IN	Control input for VCLK selection
5	VSEL0	IN	Control input for VCLK selection
6	SELEN	IN	Strobe for latching VSEL(0,1) *(Low enable)*
7	VSEL2	IN	Control input for VCLK selection
8	VSEL3	IN	Control input for VCLK selection
9	MSEL0	IN	Select input for MCLK selection
10	DVSS	-	Ground for Digital Circuit
11	MSEL1	IN	Select input for MCLK selection
12	MCLK	OUT	Memory Clock Output
13	$\overline{\text{PWRDN}}$	IN	Power Down Control
14	MCLKE	IN	Enable input for MCLK output *(high enables output)*
15	AVDD	-	Power supply for analog circuit
16	AVSS	-	Ground for analog circuit
17	N.C.	-	No connection
18	VCLKE	IN	Enable input for VCLK output *(high enables output)*
19	VCLK	OUT	Video Clock Output
20	DVDD	-	Power supply for Digital Circuit

Note:
CLKI, EXTCLK,VSEL0, VSEL1,VSEL2, VSEL3, SELEN, MSEL0, MSEL1, MSEL2, VCLKE, and MCLKE - input pins have internal pullup resistors. $\overline{\text{PWRDN}}$ has an internal pulldown resistor.

Absolute Maximum Ratings

Ambient Temperature under bias	0 °C to 70 °C
Storage temperature	-40 °C to 125 °C
Voltage on all inputs and outputs with respect to V_{SS}	0.3 to 7 Volts

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (OV Ground). Positive current flows into the referenced pin.

Operating Temperature range	0 °C to 70 °C
Power supply voltage	3.0 to 5.25 Volts

AC Timing Characteristics

The following notes apply to all of the parameters presented in this section:

1. REFCLK = 14.318 MHz
2. T_C = $1/F_C$
3. All units are in nanoseconds (ns).
4. Maximum jitter is within a range of 30 µs after triggering on a 400 MHz scope.
5. Rise and fall time is between 0.8 and 2.0 VDC unless otherwise stated.
6. Output pin loading = 15pF
7. Duty cycle is measured at $V_{DD}/2$ unless otherwise stated.

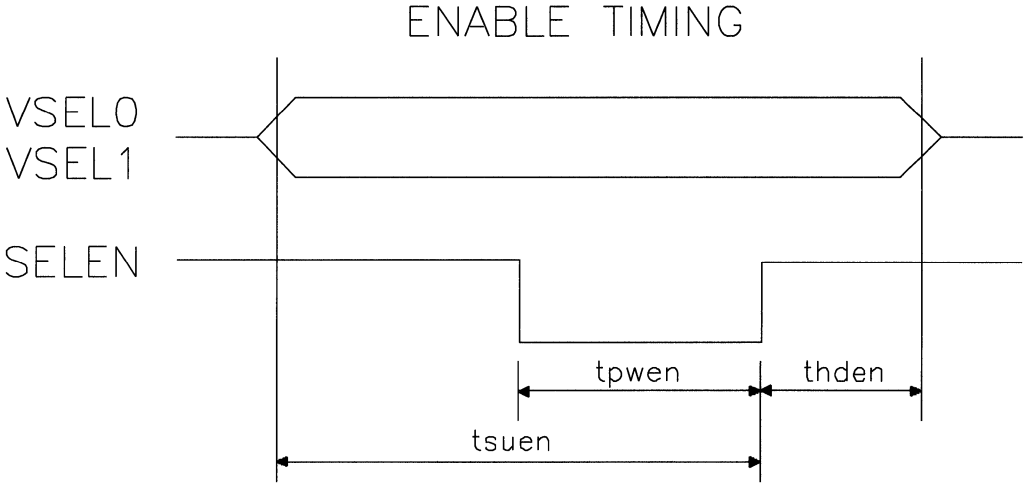
SYMBOL	PARAMETER	MIN	MAX	NOTES
	STROBE TIMING			
Tpw	Strobe Pulse Width	20	-	
Tsu	Setup Time Data to Strobe	20	-	
Thd	Hold Time Data to Strobe	10	-	
	MCLK and VCLK TIMINGS @ **5.0V**			
Tr	Rise Time	-	2	Duty Cycle 40% min. to
Tf	Fall Time	-	2	60% max.
-	Frequency Error		0.5	%
-	Maximum Frequency		135	MHz
-	Propagation Delay for Pass Through Frequency	-	20	ns
-	Output Enable to Tristate (into and out of) time		15	ns
	MCLK and VCLK TIMINGS @ **3.3V**			
Tr	Rise Time	-	3	Duty Cycle 40% min. to
Tf	Fall Time	-	3	60% max.
-	Frequency Error		.5	%
-	Maximum Frequency		110	MHz
-	Propagation Delay for Pass Through Frequency	-	30	ns
-	Output Enable to Tri-State (into and out of) time		20	ns

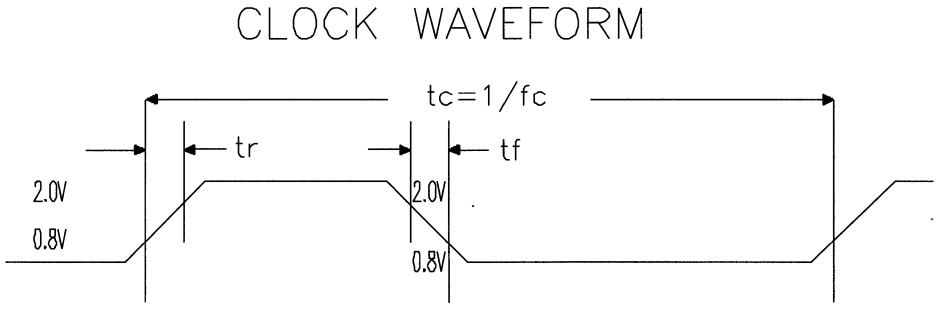
DC Characteristics at 5 Volts V_{DD}

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{DD}	Operating Voltage Range	4.75	5.25	V	
V_{IL}	Input Low Voltage	V_{SS}	0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0	V_{DD}	V	V_{DD} = 5V
I_{IH}	Input Leakage Current	-	10	µA	V_{IN} = V_{CC}
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = 8.0 mA
I_{DD}	Supply Current	-	30	mA	VDD = 5V
R_{UP}	Internal Pullup Resistors	50	-	K ohms	V_{IN} = 0.0V
C_{in}	Input Pin Capacitance	-	8	pF	F_C = 1 MHz
C_{out}	Output Pin Capacitance	-	12	pF	F_C = 1 MHz
I_{PN}	Powerdown Supply Current	-	1.0	µA	V_{DD}= 3.3V
R_{DN}	Internal Pulldown Equivalent	20	-	K ohms	V_{IN}= V_{DD}= 5V

DC Characteristics at 3.3 Volts V_{DD}

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{DD}	Operating Voltage Range	3.0	3.6	V	
V_{IL}	Input Low Voltage	V_{SS}	0.8	V	V_{DD} = 3.3V
V_{IH}	Input High Voltage	2.0	V_{DD}	V	V_{DD} = 3.3V
I_{IH}	Input Leakage Current	-	10	µA	V_{in} = V_{DD}
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 3.0 mA
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = 3.0 mA
I_{DD}	Supply Current	-	20	mA	V_{DD} = 3.3V
R_{UP}	Internal Pullup Resistors	100	-	K ohms	V_{IN} = 0.0V
C_{in}	Input Pin Capacitance	-	8	pF	F_C = 1 MHz
C_{out}	Output Pin Capacitance	-	12	pF	F_C = 1 MHz
I_{PN}	Powerdown Supply Current	-	1.0	µA	V_{DD} = 3.3V
R_{DN}	Internal Pulldown Equivalent	50	-	K ohms	V_{IN} = V_{DD} = 3.3V





ICS90C65 TIMING

Table 1-1 VCLK SELECTION

VSEL				
				VCLK FREQUENCY (MHz)
3	2	1	0	Pattern 951
0	0	0	0	30.0
0	0	0	1	77.25
0	0	1	0	EXTCLK
0	0	1	1	80.0
0	1	0	0	31.5
0	1	0	1	36.0
0	1	1	0	75.0
0	1	1	1	50.0
1	0	0	0	40.0
1	0	0	1	50.0
1	0	1	0	32.0
1	0	1	1	44.9
1	1	0	0	25.175
1	1	0	1	28.322
1	1	1	0	65.0
1	1	1	1	36.0

Table 1-2 MCLK SELECTION

MSEL			
			MCLK FREQUENCIES (MHz)
2	1	0	Pattern 951
0	0	0	33.0
0	0	1	49.218
0	1	0	60.0
0	1	1	30.5
1	0	0	41.612
1	0	1	37.5
1	1	0	36.0
1	1	1	44.296

Integrated Circuit Systems, Inc.

ICS9161

Preliminary Information

Dual Programmable Graphics Frequency Generator

B

Features

- **Pin for pin and function compatible with ICD2061A**
- **Dual programmable graphics clock generator**
- **Memory and video clocks are individually programmable on-the-fly**
- **Ideal for designs where multiple or varying frequencies are required**
- **Increased frequency resolution from optional pre-divide by 2 on the M counter**
- **Output enable feature available for tri-stating outputs**
- **Independent clock outputs range from 390 kHz to 120 MHz**
- **Operation up to 140 MHz available**
- **Power-down capabilities**
- **Low power, high speed 0.8 µ CMOS technology**
- **Glitch-free transitions**
- **Available in 16 pin SOIC or PDIP package**

General Description

The ICS9161 is a fully programmable graphics clock generator. It can generate user specified clock frequencies using an externally generated input reference or a single crystal. The output frequency is programmed by entering a 24 bit digital word through the serial port.

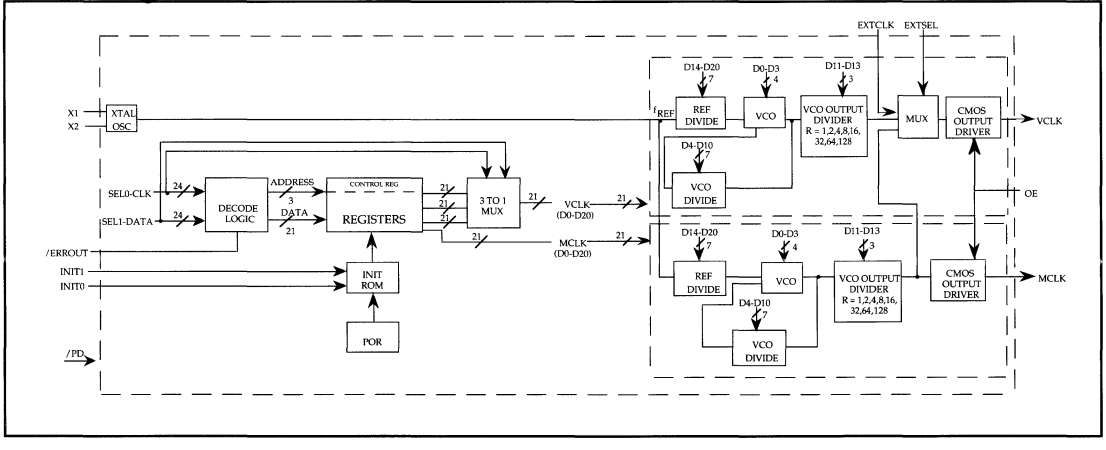
Two fully user-programmable phase-locked loops are offered in a single package. One PLL is designed to drive the memory clock, while the second drives the video clock. The outputs may be changed on-the-fly to any desired frequency between 390 kHz and 120 MHz. The ICS9161 is ideally suited for any design where multiple or varying frequencies are required.

This part is ideal for graphics applications. It generates low jitter, high speed pixel clocks. It can be used to replace multiple, expensive high speed crystal oscillators. The flexibility of the device allows it to generate non-standard graphics clocks.

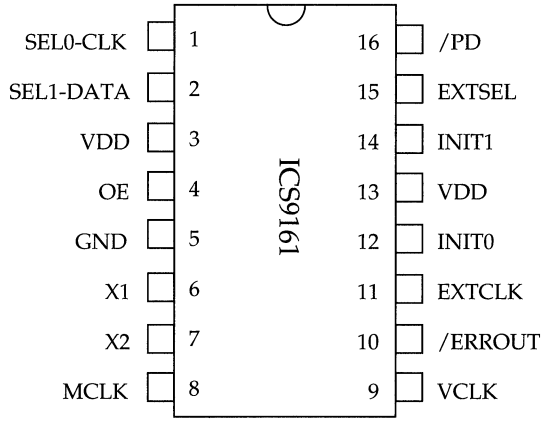
The ICS9161 is also ideal in disk drives. It can generate zone clocks for constant density recording schemes. The low profile, 16 pin SOIC or PDIP package and low jitter outputs are especially attractive in board space critical disk drives.

The leader in the area of multiple output clocks on a single chip, ICS has been shipping graphics frequency generators since October, 1990, and is constantly improving the phase locked loop. The ICS9161 incorporates a patented fourth generation PLL that offers the best jitter performance available.

Block Diagram



Pin Configuration



Pin Description

Pin Name	Pin #	Description
SEL0-CLK	1	Clock input in serial programming mode Clock select pin in operating mode
SEL1-DATA	2	Data input in serial programming mode Clock select pin in operating mode
AVDD	3	Power
OE	4	Tri-states outputs when low
GND	5	Ground
X1	6	Crystal input
X2	7	Crystal output
MCLK	8	Memory clock output
VCLK	9	Video clock output
/ERROUT	10	Output low signals an error in the serially programmed word
EXTCLK	11	External clock input
INIT0	12	Selects initial power-up conditions, LSB
VDD	13	Power
INIT1	14	Selects initial power-up conditions, MSB
EXTSEL	15	Selects external clock input (EXTCLK) as VCLK output
/PD	16	Power-down pin, active low

Register Definitions

The register file consists of the following six registers:

Register Addressing

Address	Register	Definition
000	REG0	Video Clock Register 1
001	REG1	Video Clock Register 2
010	REG2	Video Clock Register 3
011	MREG	Memory Register
100	PWRDWN	Divisor for Power-down mode
110	CNTL REG	Control Register

The ICS9161 places the three video clock registers and the memory clock register in a known state upon power-up. The registers are initialized based on the state of the INIT1 and INIT0 pins at application of power to the device. The INIT pins must ramp up with VDD if a logical 1 on either pin is required. These input pins are internally pulled down and will default to a logical 0 if left unconnected.

The registers are initialized as follows:

Register Initialization

INIT1	INIT0	MREG	REG0	REG1	REG2
0	0	32.500	25.175	28.322	28.322
0	1	40.000	25.175	28.322	28.322
1	0	50.350	40.000	28.322	28.322
1	1	56.644	40.000	50.350	50.350

Register Selection

When the ICS9161 is operating, the video clock output is controlled with a combination of the SEL0, SEL1, /PD, and OE pins. The video clock is also multiplexed to an external clock (EXTCLK) which can be selected with the EXTSEL pin. The VCLK Selection Table shows how VCLK is selected.

VCLK Selection

OE	/PD	EXTSEL	SEL1	SEL0	VCLK
0	x	x	x	x	Tri-State
1	0	x	x	x	Forced High
1	1	x	0	0	REG0
1	1	x	0	1	REG1
1	1	0	1	0	EXTCLK
1	1	1	1	x	REG2
1	1	x	1	1	REG2

As seen in the table above, OE acts to tri-state the output. The /PD pin forces the VCLK signal high while powering down the part. The EXTCLK pin will only be multiplexed in when EXTSEL and SEL0 are logic 0 and SEL1 is a logic 1.

The memory clock outputs are controlled by /PD and OE as follows:

MCLK Selection

OE	/PD	MCLK
0	x	Tri-State
1	1	MREG
1	0	PWRDWN

The Clock Select pins SEL0 and SEL1 have two purposes. In serial programming mode, these pins act as the clock and data pins. New data bits come in on SEL1 and these bits are clocked in by a signal on SEL0. While these pins are acquiring new information, the VCLK signal remains unchanged. When SEL0 and SEL1 are acting as register selects, a timeout interval is required to determine whether the user is selecting a new register or wants to program the part. During this initial timeout, the VCLK signal remains at its previous frequency. At the end of this timeout interval, a new register is selected. A second timeout interval is required to allow the VCO to settle to its new value. During this period of time, typically 5 msec, the input reference signal is multiplexed to the VCLK signal.

When MCLK or the active VCLK register is being reprogrammed, then the reference signal is multiplexed glitch-free to the output during the first timeout interval. A second timeout interval is also required to allow the VCO to settle. During this period, the reference signal is multiplexed to the appropriate output signal.

Control Register Definitions

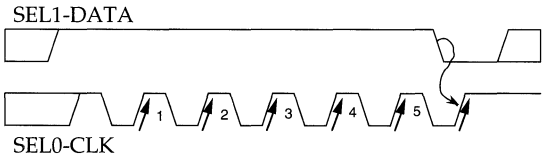
The control register allows the user to adjust various internal options. The register is defined as follows:

Bit	Bit Name	Default Value	Description
9	C5	0	This bit determines which power-down mode the /PD pin will implement. Power-down mode 1, C5 = 0, forces the MCLK signal to be a function of the power-down register. Power-down mode 2, C5 = 1, turns off the crystal and disables all outputs.
8	C4	0	This bit determines which clock is multiplexed to VCLK during frequency changes. C4 = 0 multiplexes the reference frequency to the VCLK output. C4 = 1 multiplexes MCLK to the VCLK output for applications where the graphics controller cannot run as slow as f_{REF}.
7	C3	0	This bit determines the length of the timeout interval. The timeout interval is derived from the MCLK VCO. If this VCO is programmed to certain extremes, the timeout interval maybe too short. C3 = 0, normal timeout. C3 = 1, doubled timeout interval.
6	C2	0	Reserved, must be set to 0.
5	C1	1	This bit adjusts the duty cycle. C1 = 0 causes a 1ns decrease in output high time. C1 = 1 causes no adjustment. If the load capacitance is high, the adjustment can bring the duty cycle closer to 50%.
4	C0	0	Reserved, must be set to 0.
3	NS2	0	Acts on register 2. NS2 = 0 prescales the N counter by 2. NS2 = 1 prescales the P counter value to 4.
2	NS1	0	Acts on register 1. NS1 = 0 prescales the N counter by 2. NS1 = 1 prescales the P counter value to 4.
1	NS0	0	Acts on register 0. NS0 = 0 prescales the P counter by 2. NS0 = 1 prescales the P counter value to 4.

Serial Programming Architecture

The pins SEL0 and SEL1 perform the dual functions of selecting registers and serial programming. In serial programming mode, SEL0 acts as a clock pin while SEL1 acts as the data pin. The ICS9161-01 may not be serially programmed when in power-down mode.

In order to program a particular register, an unlocking sequence must occur. The unlocking sequence is detailed in the following timing diagram:



The unlock sequence consists of at least 5 low-to-high transitions of CLK while data is high, followed immediately by a single low-to-high transition while data is low. Following this unlock sequence, data can be loaded into the serial data register.

Following any transition of CLK or DATA, the watchdog timer is reset and begins counting. The watchdog timer ensures that successive rising edges of CLK and DATA do not violate the timeout specification of 2ms. If a timeout occurs, the lock mechanism is reset and the data in the serial data register is ignored.
Since the VCLK registers are selected by the SEL0 and SEL1 pins, and since any change in their state may affect the output frequency, new data input on the selection bits is only permitted to pass through the decode logic after the watchdog timer has timed out. This delay of SEL0 or SEL1 data permits a serial program cycle to occur without affecting the current register selection.

Serial Data Register

The serial data is clocked into the serial data register in the order described in figure 1 below (Serial Data Timing).

The serial data is sent as follows: An individual data bit is sampled on the rising edge of CLK. The complement of the data bit must be sampled on the previous falling edge of CLK. The setup and hold time requirements must be met on both CLK edges. For specifics on timing, see the timing diagrams on pages 10, 11, and 12.

The bits are shifted in this order: a start bit, 21 data bits, 3 address bits (which designate the desired register), and a stop bit. A total of 24 bits must always be loaded into the serial data register or an error is issued. Following the entry of the last data bit, a stop bit or load command is issued by bringing DATA high and toggling CLK high-to-low and low-to-high. The unlocking mechanism then resets itself following the load. Only after a timeout period are the SEL0 and SEL1 pins allowed to return to a register selection function.

The serial data register is exactly 24 bits long, enough to

		Data Bits																				Address Bits			
		LBS																			MBS	LBS		MBS	
	START	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20	A0	A1	A2	STOP
BIT#		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	BIT#
VCO Prog-Word		M'0	M'1	M'2	M'3	M'4	M'5	M'6	R0	R1	R2	N'0	N'1	N'2	N'3	N'4	N'5	N'6	I0	I1	12	13	A0	A1	0	VCO Prog-Word
CNTL Reg		0	0	0	0	0	0	0	0	0	0	0	0	PS0	PS1	PS2	C0	C1	C2	C3	C4	C5	0	1	1	CNTL Reg
PWRDWN Reg		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P0	P1	P2	P3	0	0	1	PWRDWN Reg

Figure 1 - Serial Data Timing

accept the data being sent. The stop bit acts as a load command that passes the contents of the Serial Data Register into the register indicated by the three address bits. If a stop bit is not received after the serial register is full, and more data is sent, all data in the register is ignored and an error issued. If correct data is received, then the unlocking mechanism rearms, all data in the serial data register is ignored, and an error is issued.

/ERROUT Operation

Any error in programming the ICS9161 is signaled by /ERROUT. When the pin goes low, an error has been detected. It stays low until the next unlock sequence. The signal is invoked for any of the following errors: incorrect start bit, incorrect data encoding, incorrect length of data word, and incorrect stop bit.

Programming the ICS9161

The ICS9161 has a wide operating range, but it is recommended that it is operated within the following limits:

$1\ MHz < F_{REF} < 60\ MHz$	F_{REF} = Input Reference Frequency
$200\ KHz < F_{REF/M} < 5\ MHz$	M = Reference divide 3 to 129
$50\ MHz < F_{VCO} < 120\ MHz$	F_{VCO} = VCO output frequency
$F_{CLK} \leq 120\ MHz$	F_{CLK} = output frequency

The frequency of the programmable oscillator F_{VCO} is determined by the following fields:

Field	# of Bits
Index (I)	4
N counter value (N')	7
Mux (R)	3
M counter value (M')	7

Where the least significant bit is the last bit of M and the most significant bit is the first bit of I.

The equations used to determined the oscillator frequency are:

$$N = N' + 3 \qquad M = M' + 2$$

$$F_{VCO} = \text{Prescale} \cdot N/M \cdot F_{CLK}$$

where $3 \leq M \leq 129$ and $4 \leq N \leq 130$

and prescale = 2 or 4, as set in the control register

The value of F_{VCO} must remain between 50 MHz and 120 MHz. As a result, for output frequencies below 50MHz, F_{VCO} must be brought into range. To achieve this, an output divisor is selected by setting the values of the Mux Field (R) as follows:

Output Divisor

R	Divisor
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

Unlike the ICD2061A, the ICS9161's VCO does not require tuning to place it in certain ranges. The ICS9161's VCO will operate from 50 MHz to 120 MHz without adjusting the VCO gain. However, to maintain compatability, the I bits are programmed as in the ICD2061A.

These bits are dummy bits except for the following two cases:

Index Field (I)

I	VCLK F_{VCO}	MCLK F_{VCO}
1110	Turn off VCLK	50-120 MHz
1111	Mux MCLK to VLCK	50-120 MHz

When the index field is set to 1111, VCLK is turned off and both channels run from the same MCLK VCO. This is done in an effort to reduce jitter, which may increase when VCOs run at 2^n multiples of one another. If the two outputs must be multiples of one another, it is best to mux MCLK over to the output of the VCLK VCO, and to

power-down the VCLK VCO. The multiplexed frequency will be divided down by the correct divisor (M) and output on VCLK.

Power Management Issues

Power-down mode 1

The ICS9161 contains a mechanism to reduce the quiescent power when stand-by operation is desired. Power-down mode 1 is invoked by pulling /PD low and having the proper CNTL register bit set to zero. In this mode, VCOs are shut down, the VCLK output is forced high, and the MCLK output is set to a user-defined low frequency value to refresh dynamic RAM.

The power-down MCLK value is determined by the following equation:

$MCLK_{PD} = F_{REF}$ / (PWRDWN register divisor value)

The power-down register divisor is determined according to the 4-bit word programmed into the PWRDWN register (see table below).

Power-down mode 2

When there is no need for any output during power-down, an alternate mode is available which will completely shut down all outputs and the reference oscillator, but still preserves all register contents. Power-down mode 2 is invoked by first programming the power-down bit in the CNTL register and then pulling the /PD pin low.

The /PD pin

The /PD pin has a standard internal pull-up resistor during normal operation. When the chip goes into power-down mode 1 or 2, the normal pull-up resistor is dynamically switched to a weak pull-up, which reduces power consumption. If the /PD pin is allowed to float after it has been pulled down, the weak pull-up will bring the signal high and allow the device to resume operation.

Power Down Register Table

PWRDWN bits P3	P2	P1	P0	PWRDWN Register Value	Power-down Divisor	$MCLK_{PD}$ (f_{REF}=14.31818)
0	0	0	0	0	n/a	n/a
0	0	0	1	1	32	447.4 KHz
0	0	1	0	2	30	477.3 KHz
0	0	1	1	3	28	511.4 KHz
0	1	0	0	4	26	550.7 KHz
0	1	0	1	5	24	596.6 KHz
0	1	1	0	6	22	650.8 KHz
0	1	1	1	7	20	715.9 KHz
1	0	0	0	8 (default)	18	795.5 KHz
1	0	0	1	9	16	894.9 KHz
1	0	1	0	A	14	1.02 MHz
1	0	1	1	B	12	1.19 MHz
1	1	0	0	C	10	1.43 MHz
1	1	0	1	D	8	1.79 MHz
1	1	1	0	E	6	2.39 MHz
1	1	1	1	F	4	3.58 MHz

Absolute Maximum Ratings

VDD referenced to GND..... 7V
Operating temperature under bias..... 0°C to +70°C
Storage temperature..... -40°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation..... 0.5 Watts

Note. Stresses above those listed under Absolute Maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

Electrical Characteristics

(VDD = +5V ± 5%, 0°C ≤ $T_{AMBIENT}$ ≤ +70°C unless otherwise stated)

Device Specifications

Maximum Ratings

Name	Description	Min	Max	Units
VDD	Supply voltage relative to GND	-0.5	7.0	Volts
V_{IN}	Input voltage with respect to GND	-0.5	VDD + 0.5	Volts
T_{OPER}	Operating temperature	0	+70	°C
T_{STOR}	Storage temperature	-65	+150	°C
T_{SOL}	Max soldering temperature (10 sec)		+260	°C
T_J	Junction temperature		+125	°C
P_{DISS}	Package power dissipation		350	mWatts

DC Characteristics

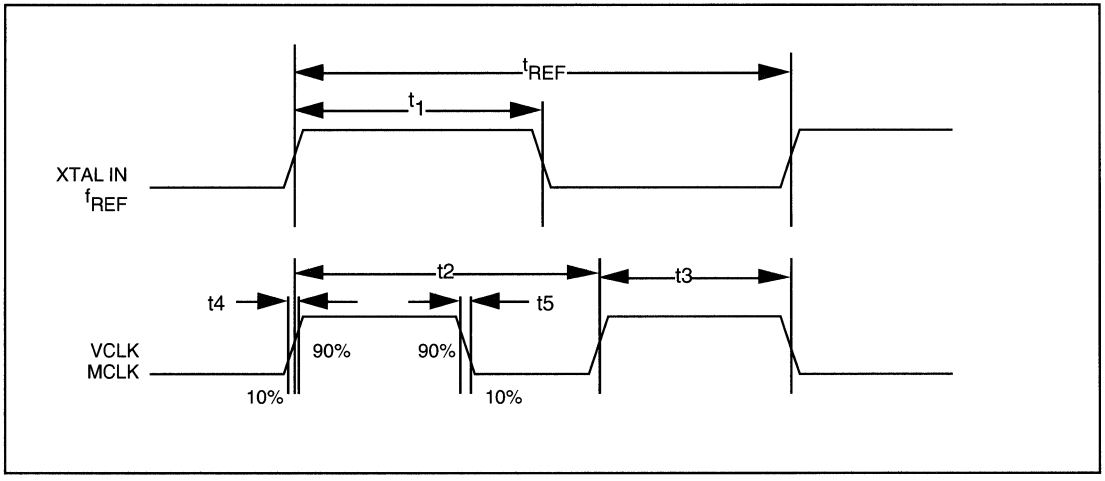
Name	Description	Min	Typ	Max	Units	Conditions
V_{IH}	High level input voltage	2.0			V	
V_{IL}	Low level input voltage			0.8	V	
V_{OH}	High level CMOS ouput voltage	3.84			V	I_{OH} = -4 ma
V_{OL}	Low level output voltage			0.4	V	I_{OL} = 4 ma
I_{IH}	Input high current			100	µa	V_{IH} = 5.25 V
I_{IL}	Input low current			-250	µa	V_{IL} = 0V
I_{OZ}	Output leakage current			10	µa	(tri-state)
I_{DD}	Power supply current	15		65	ma	
I_{DD-TYP}	Power supply current (typical)		35		ma	@60 MHz
I_{ADD}	Analog power supply current			10	ma	
I_{PD1}	Power-down current (Mode 1)		6	7.5	ma	
I_{PD2}	Power-down current (Mode 2)		25	50	µa	
C_{IN}	Input capacitance			10	pf	

AC Characteristics

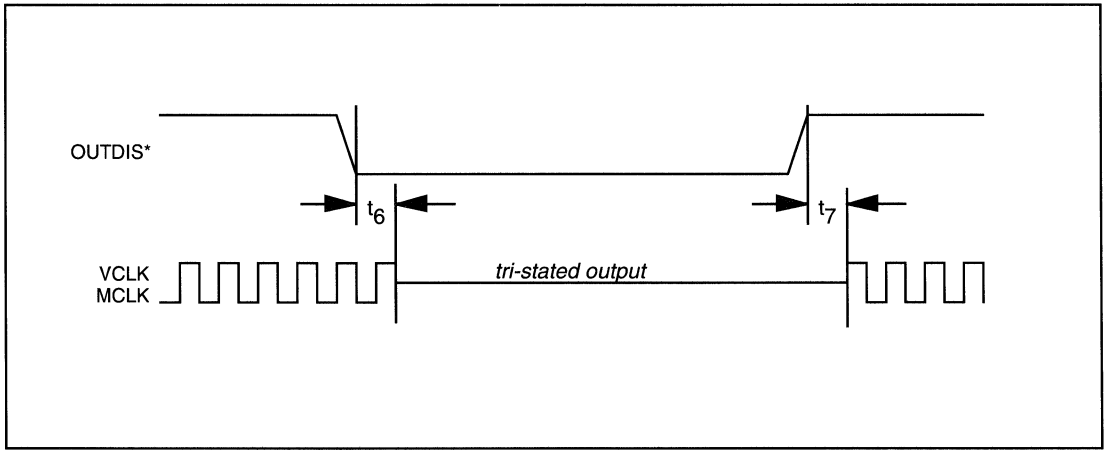
Symbol	Name	Description	Min	Typ	Max	Units
f_{REF}	Reference frequency	Reference oscillator value (note 1)	1	14.31818	60	Mhz
t_{REF}	Reference period	$1/f_{REF}$	16.6		1000	ns
t_1	Input duty cycle	Duty cycle for the input oscillator defined as t_1/t_{REF}	25%		75%	
t_2	Output clock periods	Output oscillator values	8.33 (120 MHz)		2564 (390 MHz)	ns
t_3	Output duty cycle	Duty cycle for the output oscillators (note 2)	45%		55%	
t_4	Rise times	Rise time for the ouput oscillators into a 25 pf load			3	ns
t_5	Fall times	Fall time for the output oscillator into a 25 pf load			3	ns
t_{freq1}	freq1 output	Old frequency output				
t_{freq2}	freq2 ouput	New frequency output				
t_A	f_{REF} mux time	Time clock output remains high while output muxes to reference frequency	$^{05}t_{REF}$		$^{1.5}t_{REF}$	ns
$t_{timeout}$	Timeout internal	Interval for serial programming and for VCO changes to settle (note 3)	2	5	10	ns
t_B	t_{freq2} muxtime	Time clock ouput remains high while output muxes to new frequency value	$^{05}t_{REF}$	$^{15}t_{REF}$		ns
t_6	Tri-state	Time for the ouput oscillators to go into tri-state mode after OUTDIS - signal assertion	0		12	ns
t_7	CLK valid	Time for the output oscillators to recover from tri-state mode after OUTDIS -signal goes high	0		12	ns
t_8	Power-Down	Time for power-down mode of operation to take effect			12	ns
t_9	Power-Up	Time for recovery from power-down mode of operation			12	ns
t_{10}	MCLKOUT high	Time for MCLK to go high after PWRDWN is asserted high	0		t_{PWRDWN}	ns
t_{11}	MCLKOUT delay	Delay of MCLK prior to f_{MCLK} signal at output	$^{05}t_{MCLK}$		$^{15}t_{MCLK}$	ns
t_{serclk}		Clock period of serial clock	$2 \cdot t_{REF}$		2	msec
t_{SU}		Setup time	20			ns
t_{HD}		Hold time	10			ns
t_{ldcmd}		Load command	0		t_1+30	ns

NOTES

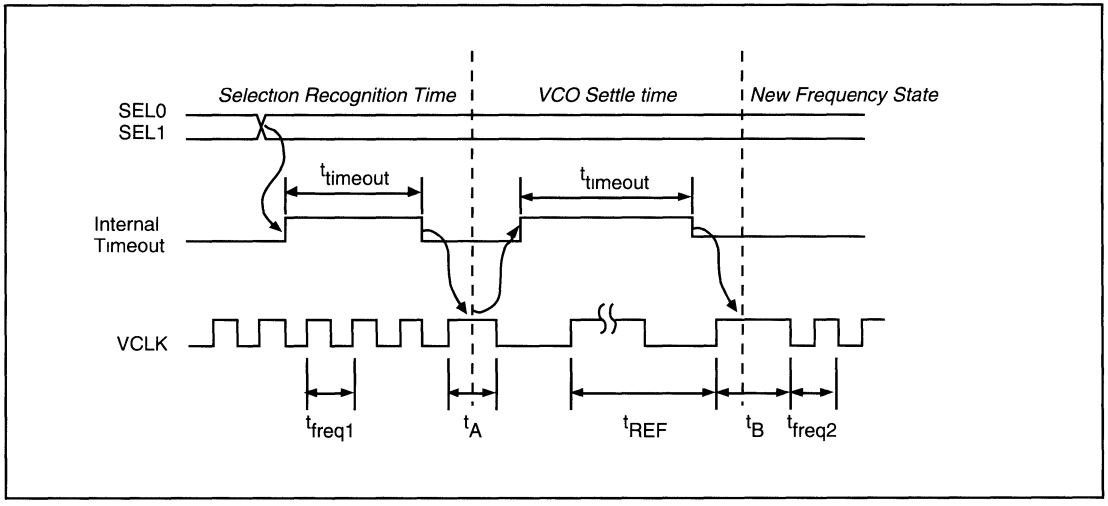
1. For reference frequencies other than 14.81818 MHz, the pre-loaded ROM frequencies will shift proportionally.
2. Duty cycle is measured at CMOS threshold levels. At 5 volts, V_{TH} = 2.5 volts).
3. If the interval is too short, see the timeout interval section in the control register definition.



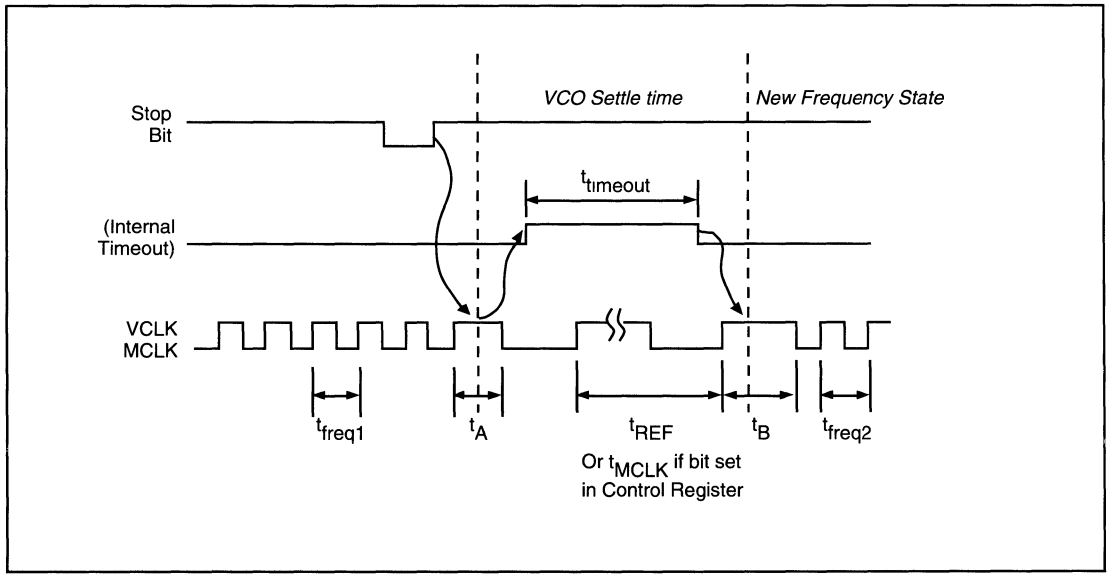
Rise and Fall Times



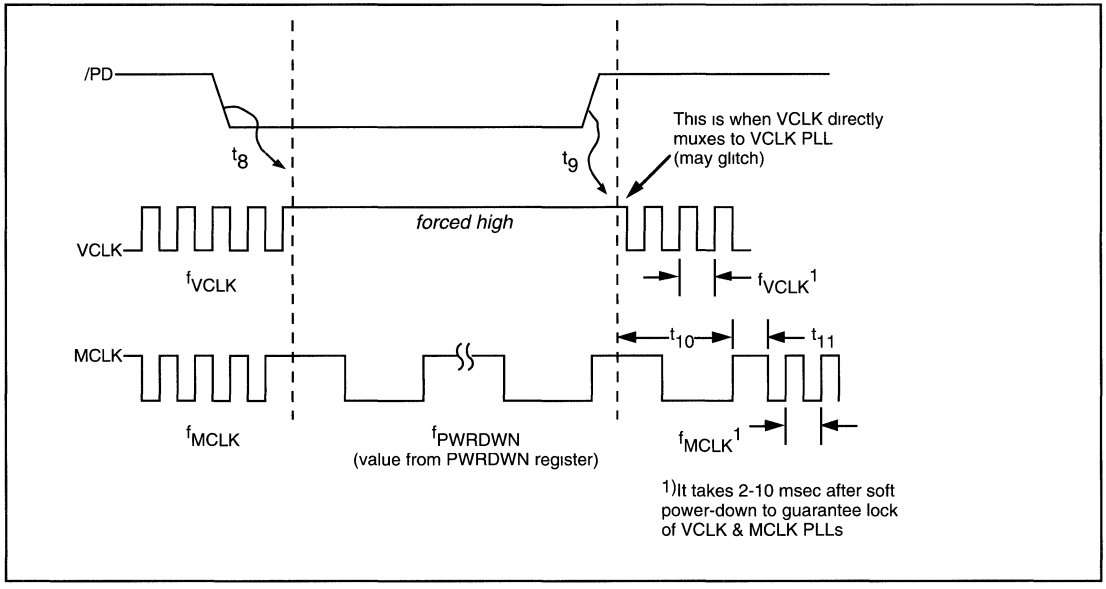
Tri-Stated Timing



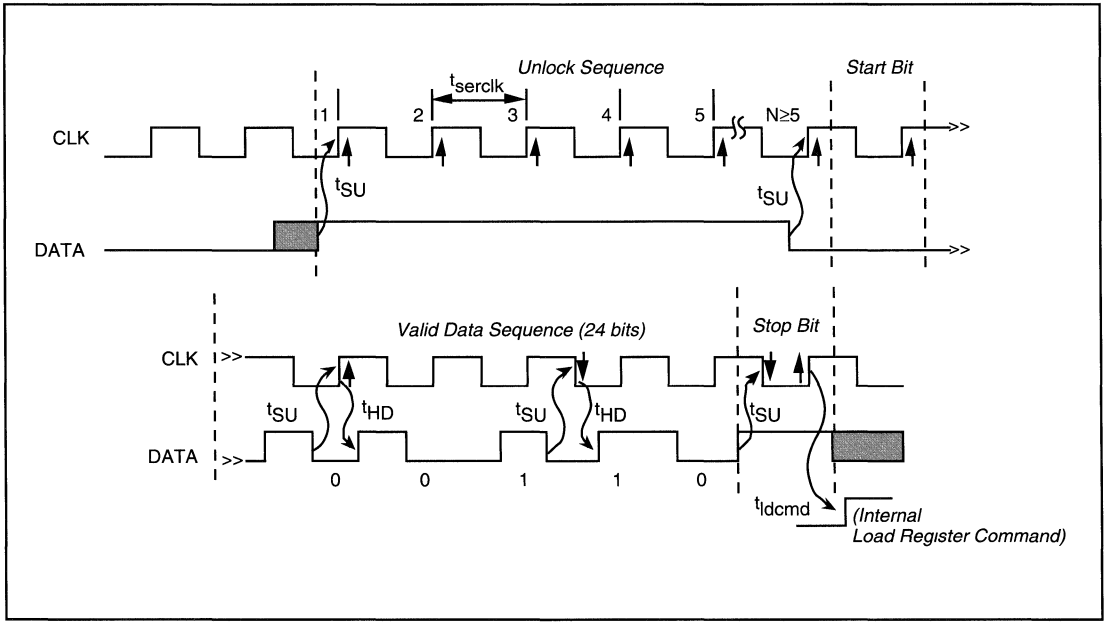
Selection Timing



MCLK & Active VCLK Register Programming Timing



Soft Power-Down Timing (Mode 2)



Serial Programming Timing

Ordering Information

Part Number	Temperature Range	Package Type
ICS9161-xxCW16	0°C to +70°C	16 lead Plastic SOIC
ICS9161-xxCN16	0°C to +70°C	16 lead Plastic DIP

Dual Frequency Generator

Features

- **Two independent clock outputs available**
- **On chip Phase Locked Loops with VCO and integrated loop filters for low jitter clock outputs**
- **Mask option for 16 + 4 frequencies, or 8 + 8**
- **Frequencies up to 130 MHz on each output clock generated internally**
- **Low power CMOS technology**
- **20 pin PDIP or SOIC package**
- **Minimum number of external components**
- **Tristate outputs**
- **Pin compatible with ICS2494 and ICS90C64**
- **Crystal oscillator circuitry with output clock**
- **16 pin narrow SOIC (150 mil) or PDIP package option available**

Applications

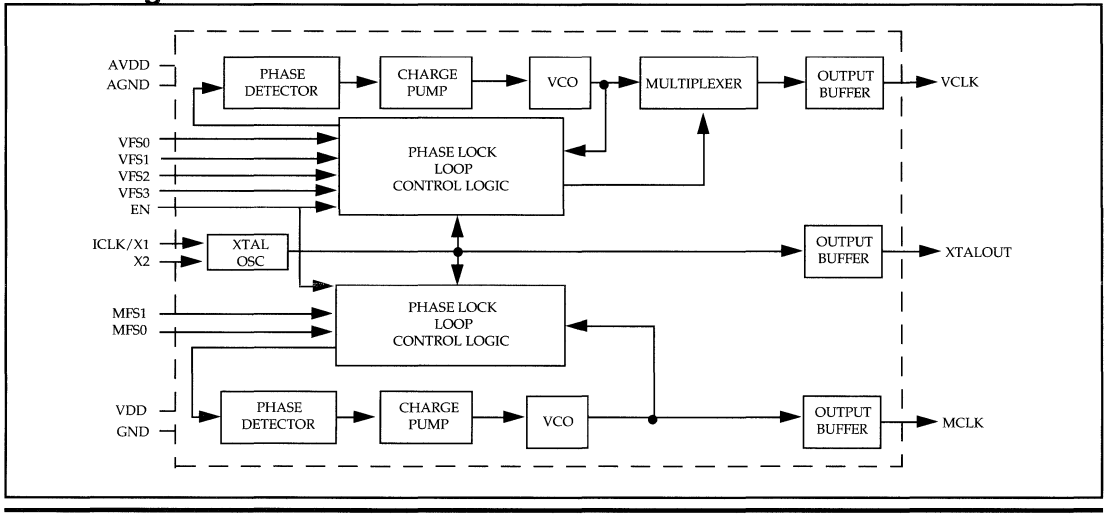
Graphics: Many video graphics systems now utilize multiple clock oscillators to provide all of the frequencies required for different monitors and modes of resolution. In addition, many graphics processors require one separate fixed frequency for the memory or system clock. By providing two independent output clocks, the AV9194 saves power, board space, and cost in eliminating these oscillators.

General Description

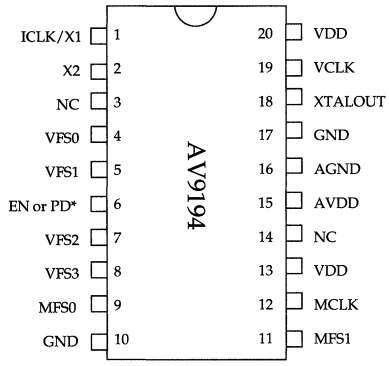
The AV9194 is a dual output frequency generator that is ideal for graphics applications. The device can replace many crystal oscillators by containing all of the required output frequencies on-chip. The AV9194 can use either a crystal or TTL level clock for its input reference frequency. On notebooks and other motherboards, the 14.318MHz input can be generated by the AV9128/9 or the AV9152/3/5. Utilizing ICS' proprietary analog CMOS Phase Locked Loop (PLL) technology, this reference frequency is used to generate two independently controlled output clocks, VCLK and MCLK. Up to 20 output frequencies, ranging from 5 to 130 MHz, can be mask programmed into the device at the time of manufacture. The six Frequency Select pins are used to choose one of 16 (or 8) masked output frequencies on the video clock, VCLK, and one of 4 (or 8) frequencies on the second clock, designated MCLK. This second clock can be used as a memory clock to time DRAMs and VRAMs, as another video (or pixel) clock, or as a system clock required by graphics processors like the 8514A and 34010/20. Standard versions of the AV9194 are available.

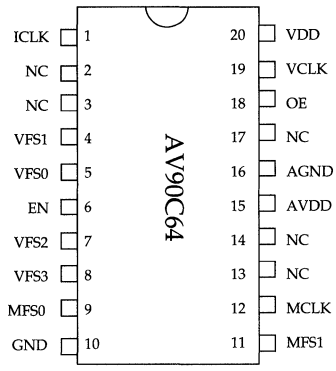
The AV9194 is one of the latest in ICS's frequency generator family. ICS has devices that are designed for many computer and computer peripheral applications, all manufactured in analog CMOS technology.

Block Diagram



Pin Configurations





Pin Description for AV9194 / AV90C64

Pin Name	Pin # AV9194	Pin # AV90C64	Pin type	Description
ICLK/X1	1	1	Input	INPUT CLOCK. TTL clock signal or crystal input
X2	2	-	Output	CRYSTAL OUT. Connect when using crystal or ceramic resonator
NC	3	3	-	NOT CONNECTED. No internal connection
VFS0	4	5	Input	VIDEO FREQUENCY SELECT 0 (LSB)
VFS1	5	4	Input	VIDEO FREQUENCY SELECT 1
EN	6	-	Input	ENABLE. Transparent high. A low latches the frequency select data
EN	-	6	Input	ENABLE. Latches VFS0-VFS3 and MFS0, MFS1 upon rising edge
PD*	6	-	Input	POWER DOWN. Turns off V+MCLK when low (AV9194-46 only)
VFS2	7	7	Input	VIDEO FREQUENCY SELECT 2
VFS3	8	8	Input	VIDEO FREQUENCY SELECT 3 (MSB)
MFS0	9	9	Input	MEMORY FREQUENCY SELECT 0 (LSB)
GND	10	10	-	DIGITAL GROUND
MFS1	11	11	Input	MEMORY FREQUENCY SELECT 1 (MSB)
MCLK	12	12	Output	MEMORY CLOCK output
VDD	13	-	-	Digital power supply. Connect to +5V DC supply
NC	14	14	-	NOT CONNECTED. No internal connection
AVDD	15	15	-	Analog power supply. Connect to +5V DC supply
AGND	16	16	-	ANALOG GROUND
GND	17	-	-	DIGITAL GROUND
XTALOUT	18	-	Intput	CRYSTAL CLOCK OUTPUT
OE	-	18	Input	OUTPUT ENABLE. Tristates VCLK when low
VCLK	19	19	Output	VIDEO CLOCK output to drive pixel clock
VDD	20	20	-	Digital power supply. Connect to +5V DC supply

ABSOLUTE MAXIMUM RATINGS

AVDD, VDD referenced to GND..... 7V
Operating temperature under bias.....0°C to +70°C
Storage temperature..... -40°C to +125°C
Voltage on I/O pins referenced to GND.....GND - 0.5V to VDD +0.5V

Power dissipation..... 0.5 Watts
ESD rating as per MIL-STD-883D, Method 3015, any pin.....1800V

Note: Stresses above those listed under Absolute Maximum ratings may cause permanent damage to the device This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect devices reliability.

Electrical Characteristics

(V_{DD} = +5V± 10%, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage	-		0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0		-	V	V_{DD} = 5V
$I_{IL(1)}$	Input Low Current	-5		-50	µA	V_{IN} = 0V
I_{IH}	Input High Current	-		5	µA	V_{IN} = VDD
V_{OL}	Output Low Voltage	-		0.4	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	VDD-.4V	-	-	V	I_{OH} = -1mA,VDD = 5.0V
V_{OH}	Output High Voltage	VDD-.8V	-	-	V	I_{OH} = -4mA,VDD = 5.0V
V_{OH}	Output High Voltage	2.4		-	V	I_{OH} = -8mA
I_{DD}	Supply Current		20		mA	No load. 28 and 40MHz
I_{DDSB}	Supply Current, Power Down (AV9194-46 Only)		30	50	µA	No load. 28 and 40MHz
$R_{UP(1)}$	Internal Pullup Resistors		500		KΩ	
F_d	Output Frequency Change over Supply and Temperature			0.005	%	With respect to typical frequency
C_I	Input Capacitance			8	pF	F_C = 1 MHz

NOTES: (1) Input pins VFS0-VFS3, MFS0, MFS1, EN, OE and PD* have internal pull-up resistors.
(2) Pins X1 and X2 have on-chip capacitors of 20pF to GND and are tied together by a 1MΩ on-chip resistor.

AC Characteristics						
t_{CLKR}	Input Clock Rise Time			20	ns	
t_{CLKF}	Input Clock Fall Time			20	ns	
t_w	Enable pulse width	20		-	ns	
t_{su}	Setup time data to enable	20		-	ns	
t_{hd}	Hold time data to enable	10		-	ns	
t_r	Rise time, 0.8 to 2.0 Volts	-	1	2	ns	25 pf load
t_r	Rise time, 20% to 80%	-	2	4	ns	25 pf load
t_f	Fall time, 2.0 to 0.8 Volts	-	1	2	ns	25 pf load
t_f	Fall time, 80% to 20%	-	2	4	ns	25 pf load
d_t	Duty cycle, MCLK andVCLK		48/52	40/60	%	25 pf load
f_{in}	Input frequency, ICLK	5	14.318	20	MHz	
t_{jls}	Jitter, 1 sigma		±75		ps	
t_{jab}	Jitter, absolute		±325	±500	ps	
fmax	Maximum Output Frequency			130	MHz	

AV9194 and AV90C64 Standard Versions

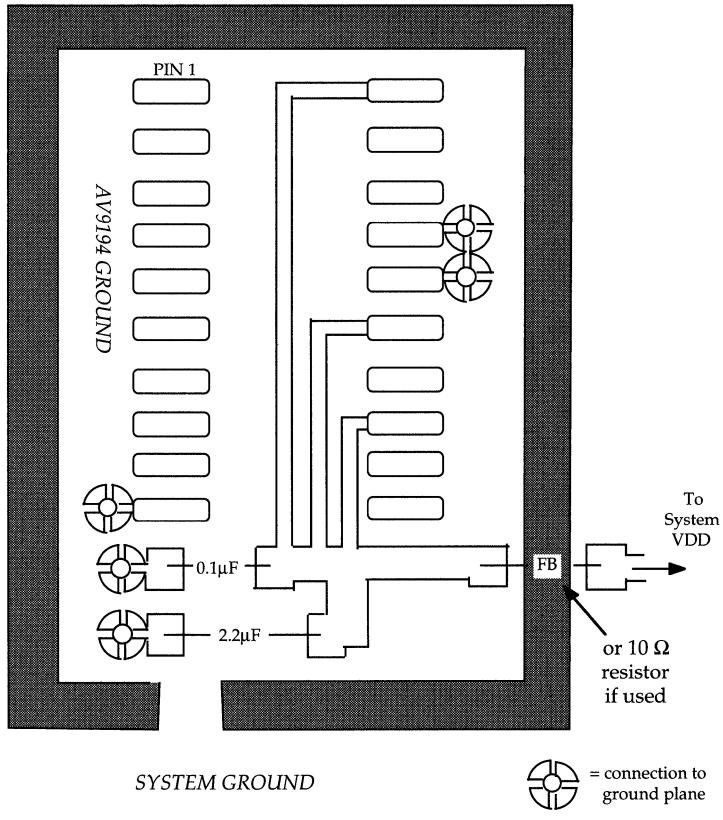
Mask Number	AV9194-04	AV9194-07	AV9194-11	AV9194-12	AV9194-36	AV9194-37
VGA Controllers	Tseng Labs ET4000	S3 86C801,805,928	S3 86C801,805,928	S3 86C911,924	Cirrus Logic	Tseng Labs ET4000
VCLK ADDRESS	VCLK OUTPUT (MHz)					
0	25.175	25.175	25.175	25.175	XTAL	50.350
1	28.322	28.322	28.322	28.322	65.028	56.644
2	32.514	40.0	40.0	40.0	EXTFREQ	65.00
3	36.00	0.00	0.00	0.00	36.00	72.00
4	40.00	50.00	50.00	50.00	25.175	80.00
5	44.90	77.00	77.00	77.00	28.322	89.80
6	50.35	36.00	36.00	36.00	24.00	63.00
7	65.00	44.90	44.90	44.90	40.00	75.00
8	50.35	130.00	130.00	130.00	44.90	25.175
9	56.664	120.00	120.00	120.00	50.35	28.322
A	65.028	80.00	80.00	80.00	16.257	31.50
B	72.00	31.50	31.50	31.50	32.514	36.00
C	80.00	110.00	110.00	110.00	56.644	40.00
D	89.80	65.00	65.00	65.00	20.00	44.90
E	75.00	75.00	75.00	75.00	41.539	50.00
F	108.00	94.50	94.50	72.00	80.00	65.00
MCLK ADDRESS	MCLK OUTPUT (MHz)					
0	41.00	45.00	32.90	40.00	55.00	55.00
1	46.00	38.00	35.60	41.612	60.00	75.00
2	50.00	52.00	43.90	44.744	70.00	70.00
3	56.00	50.00	49.10	50.00	65.00	80.00

AV9194 and AV90C64 Standard Versions (continued)

Mask Number	AV9194-42	AV9194-44	AV9194-46	AV9194-56	AV9194-60	AV90C64
VGA Controllers	WD WD90C30	CPU Applications	NCR 77C22E	S3 86C911, 86C924	Weitek 5X86	WD (All)
VCLK ADDRESS	VCLK OUTPUT (MHz)					
0	30.00	20.00	25.175	25.175	50.35	30.00
1	77.250	24.00	28.322	28.322	56.644	77.25
2	EXTFREQ	32.00	36.00	40.0	33.25	0.00
3	80.00	40.00	65.00	0.00	52.00	80.00
4	31.50	50.00	44.90	50.00	80.00	31.50
5	36.00	66.667	50.00	77.00	63.00	36.00
6	75.00	80.00	80.00	36.00	0.00	75.00
7	50.00	100.00	75.00	44.90	75.00	50.00
8	40.00	54.00	56.644	130.00	25.175	40.00
9	50.00	70.00	63.00	120.00	28.322	50.00
A	32.00	90.00	72.00	80.00	31.50	32.00
B	44.90	110.00	130.00	31.50	36.00	44.90
C	25.175	25.00	90.00	110.00	40.00	25.175
D	28.322	33.333	100.00	65.00	44.90	28.322
E	65.00	40.00	110.00	75.00	50.00	65.00
F	36.00	50.00	120.00	72.00	65.00	36.00
MCLK ADDRESS	MCLK OUTPUT (MHz)					
0	36.00	16.00	50.00	55.00	40.00	41.61
1	44.347	24.00	60.00	75.00	33.333	37.50
2	37.50	50.00	65.00	70.00	45.00	49.22
3	44.773	66.667	75.00	80.00	50.00	44.30

Avasem is continually developing new standard versions of the AV9194.
Consult your local sales representative for the latest Avasem products.

AV9194 BOARD LAYOUT

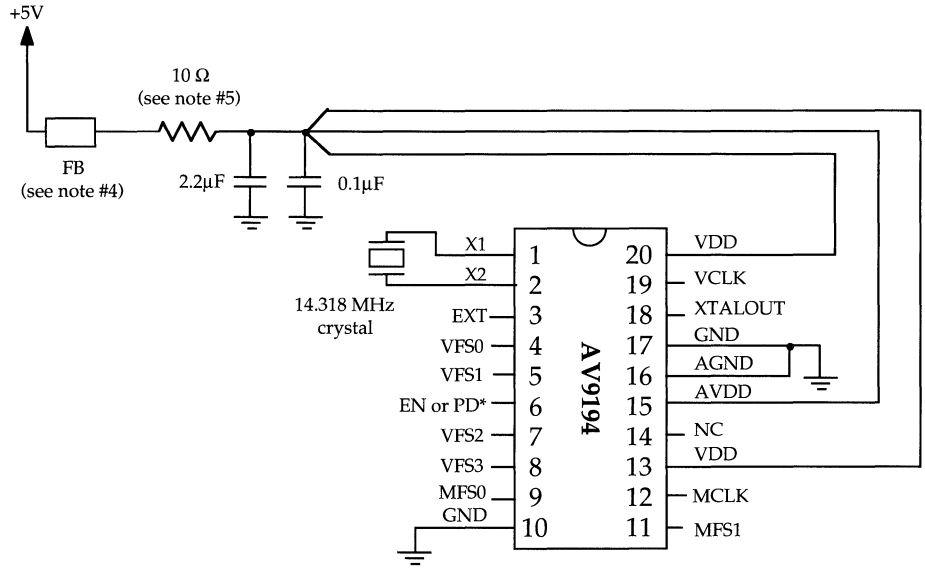


This is the recommended layout for the AV9194. Shown are the power connections and the ground plane.

The most important feature is the isolated ground plane, connected at one point near the 2.2µF and 0.1 µF decoupling caps. The ferrite bead is optional, but will help with EMI radiation from the power supply trace. In applications with an excessively noisy power supply, a 10 Ω resistor in the power supply line (between the decoupling caps and the ferrite bead, if used) is recommended to reduce induced clock jitter. The traces to distribute power should be as wide as possible.

If a crystal or crystal oscillator is used, it should be surrounded by the isolated ground plane. Clock output traces should be kept narrow, and distance over isolated ground plane should be kept to a minimum to reduce coupling.

AV9194
Recommended External Circuit



Notes:

1. Avasem recommends the use of an isolated ground plane for the AV9194. All grounds shown on this drawing should be connected to this ground plane. This ground plane should be connected to the system ground plane at a single point. Please refer to AV9194 Board Layout diagram.

2. A single power supply connection for all VDD lines at the decoupling capacitors is recommended to reduce interaction of analog and digital circuits. The decoupling capacitors should be located as close to the VDD pins as possible.

4. The ferrite bead does not enhance the performance of the AV9194, but will reduce EMI radiation from the VDD line.

5. The 10 Ω resistor is optional for noisy power supply applications. It is used to reduce clock jitter which may be induced by excessive power supply noise.

Ordering Information

Part Number	Temperature Range	Package Type
AV9194-xxCN20	0°C to +70°C	20 lead Plastic DIP
AV9194-xxCW20	0°C to +70°C	20 lead Plastic SOIC
AV90C64N	0°C to +70°C	20 lead Plastic DIP
AV90C64M	0°C to +70°C	20 lead Plastic SOIC

Note: The dash number following AV9194, (denoted by xx above) must be included when ordering product since it specifies the mask options being ordered. Please request an AV9194 customer order form when ordering custom masks.

ICS

Video Timing Generator Applications

Integrated Circuit Systems, Inc.

Application Note

Designing with ICS Video Dot Clock Generators

The ICS family of dot clock generators is a simple to use, cost-effective solution to the generation of dot clock frequencies required by VGA and other graphics subsystems. Application of these parts is fairly straightforward; however, certain precautions should be taken to insure a low phase jitter implementation when laying out circuit boards. The ICS dot clock products are high-speed high-performance mixed analog/digital IC products. As such they are capable of generating very fast risetime signals (< 1.5 nanoseconds). Although ICS dot clock generators have digital inputs and outputs, they are **precision analog ICs**. They are dependent internally on stable, noise-free analog signals in the microvolt region for jitter-free operation.

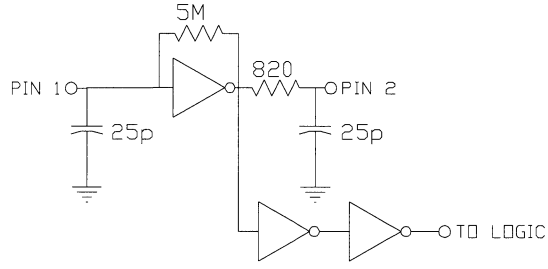
Grounding

The most common reason for poor performance of graphics subsystems products is inadequate grounding. To achieve maximum performance, a ground plane layer will be required for the area on which the dot clock generator is placed. Typical graphics cards already have this layer as many other parts of the subsystem such as the DRAM and Ramdac require this as well. To prevent ground loops and circulating currents associated with other parts of the subsystem from generating differential voltages across the circuitry used with the dot clock, a cut should be made in the groundplane layer surrounding the dot clock circuitry so that it connects with the main part of the groundplane at one point. Preferably this will lead to a low noise area close to the card edge connector. This insures that signals related to logic, DRAM memory, and other circuitry will not be superimposed on VCO control inputs.

The Two-Layer VGA Board

Recently, competitive pressure in the VGA adapter market has resulted in a high level of interest in designing a two-layer VGA PC board. With some compromise in jitter performance, a successful two layer design may be achieved. **The success of a two layer design is totally dependent on board layout**. Video RAM represents a highly capacitive load to the VGA controller. Read/write operations result in high currents in the order of amperes on the VGA board. If these current pulses interact with the dot clock generator via common ground paths, etc. the result will be highly unsatisfactory. If the ground paths to the VGA controller are not robust, the relative ground bounce of the VGA controller, dot clock generator, and Ramdac will create visually apparent problems. Component placement must be carefully thought out with respect to ground currents if a two layer design is to be successful. We strongly suggest that you contact ICS applications engineering and submit a copy of your layout and PCB artwork to us before you purchase boards.

Internal Crystal Oscillator



Crystal Oscillator & Crystal Selection

Most of the ICS family of dot clock generators have circuitry onboard to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in anti- (also called parallel-) resonant mode. See the AC Characteristics in the appropriate data sheet for the effective capacitive loading to specify when ordering crystals.

So called series-resonant crystals may also be used with the ICS dot clock generators. Be aware that the oscillation frequency will be slightly higher than the frequency that is stamped on the can (typically 0.005-0.01%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. As it is necessary for this circuitry to be biased into the linear region to implement the oscillator function these pins are susceptible to noise pickup. Avoid routing digital signals or the dot clock generator outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

Reference Frequency

Alternatively, the bus clock signal at 14.31818 may be used. If this is done, an on-board buffer should be used to clean up this signal, and prevent problems with noise, ringing, and overshoot. If a bipolar buffer is used, the signal should be capacitively coupled to XTAL1 as the internal oscillator is internally biased to a $V_{DD}/2$ threshold. A .047 or .1 microfarad capacitor is recommended for this application. HCMOS buffers may be directly connected to XTAL1 through a 33 ohm series resistor. XTAL2 must be left unconnected if an external clock is used.

Bypassing

High frequency bypassing of the ICS dot clock generator is mandatory for proper operation. Short, low inductance connections are important between the analog and digital V_{DD} pins to the bypass capacitors and from the capacitor to ground. When selecting capacitors to bypass this or any other high-frequency device, the frequency of most concern is not the operating frequency of the device, but the frequency equivalent to 1/risetime, in this case 500 MHz. Multiple bypass capacitors are preferable, with a small ceramic disk placed as close as possible to the supply pin. The capacitor, its leads, and the interconnect leads form a series resonant circuit. This circuit should be resonant at a frequency well above the frequency of interest (500 MHz). Therefore capacitor values of .047 microfarad or less will provide more effective bypassing, forcing the bypassing to operate on the capacitive side of resonance. A larger (1 microfarad or greater) tantalum bypass should parallel this to reject lower frequency noise.

"Microphonics"

ICS applications engineering occasionally receives complaints about graphics subsystems being "microphonic." It is claimed that our parts are subject to output jitter if they are tapped on or vibrated. These problems invariably show up on surface-mount board designs. When investigated, the problem always turns out to be ceramic capacitors.

Small surface-mount ceramic capacitors are made with barium titanate dielectric material. Barium titanate is also used to make microphones, ultrasonic transducers etc., as it is one of the most efficient piezoelectric material. Soldering these capacitors to a G10 glass epoxy PC board results in the capacitor being placed in mechanical compression, as the glass/epoxy material has a much higher coefficient of thermal expansion than does the barium titanate, a ceramic. When the PCB cools after a soldering operation the capacitor is partially compressed and rigidly atached to the board. Any vibration transmitted to the board results in flexure of the capacitor which outputs a resultant voltage. Although the same materials are used to make leaded components, the wire leads decouple the mechanical stress and vibration from the capacitor, and no problem results.

This phenomenon caused difficulties with graphics subsystems that used our first generation devices such as the ICS1394, ICS1560, and ICS90C63 which had external-loop filter components. The advent of second generation dot clock devices with integral loop filters has all but eliminated this problem if double bypassing is used. The larger tantalum capacitor is non-microphonic even in surface mount, and readily absorbs mechanically generated voltage spikes from the smaller (but more effective at high frequencies) ceramic capacitor.

Soldering Considerations

A problem that ICS applications engineering is beginning to see quite often is related to the new water-based fluxes. Until quite recently most fluxes used for PC board assembly were of the activated rosin type. Wave soldering machines sprayed flux directly on the solder side of the PCB, then the board traveled through the solder wave. Boards were then run through a vapor degreaser where trichlorethelyne (TCE) or Freon were used to remove residual flux. Environmental considerations have all but eliminated the use of these substances for flux removal.

Rosin based fluxes are very stable non-conductive materials at room temperatures and cause few problems even when poorly cleaned. Water-based fluxes are hygroscopic, that is they absorb water from the water vapor present in air. As they are ionic compounds, they can cause a resistive film to be left on boards that have been improperly cleaned. In addition, the incresased usage of surface mount technology has resulted in components being much closer to the PC board surface, making it harder to adequately remove flux from under these components. The smaller lead spacing and higher density of these boards results in shorter leakage paths, and a higher probability of leakage related problems. The problem typically manifests itself as a crystal oscillator startup problem. A customer will call ICS and say that one of our dot clock generator products refused to start. Replacing the device fixed the problem. As they have experienced the problem several times they are requesting ICS Quality Assurance to run a failure analysis. When we retest their parts all appear to work normally.

When the customer replaced the part he inadvertently fixed the problem. Board repair is invariably done with a soldering iron and rosin core solder. Most often an aerosol can of flux remover is used to clean up after a repair. Heating the solder pads to remove and replace the suspected device will drive any moisture from the PC board. The rosin flux has substances to entrap or neutralize ionic contaminants and, even if not properly cleaned, leaves a waterproof coating. With the offending conductive residue removed, the crystal oscillator circuitry is now capable of biasing itself back into the linear region and will be able to start.

This source of problems could also cause jitter related problems in first generation devices with external loop filter components, as this circuitry exhibits very high impedances. Straight digital circuitry is relatively immune to these problems; however, it may be causing similar problems with Ramdac circuitry.

Make sure your PC board assembly operation is regularly tested for ionic contamination and you will never see this problem.

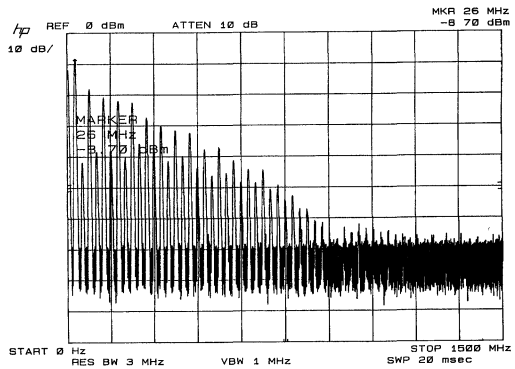
Output Considerations

The output circuitry of the ICS family of dot clock generator products exhibits a characteristic impedance of approximately 33 ohms. A series resistor of 33 ohms and an inexpensive ferrite bead in series with the output will greatly reduce the radiated harmonics of the output signal without otherwise impairing performance. This may be helpful in meeting FCC requirements. The ICS dot clock generator has consistently produced less interference than fixed frequency crystal oscillators in this respect, as it is only producing one frequency at a time and has nicely controlled rise and fall times. See the comparative spectral plots of the ICS dot clock generators and crystal oscillators and note the relatively rapid rate that high frequency harmonics fall off for the dot clock generator. **In no case should a capacitor be connected from the output signal to ground.** At the frequency equivalent to the risetime (500MHz) even a 6 picofarad oscilloscope probe is equivalent to a 50 ohm reactance. The current, to charge and discharge this capacitor, has to be provided from V_{DD} and ground. This capacitive loading defeats the purpose of our carefully controlled bypassing circuitry, and is not required for meeting FCC interference requirements, if the series resistor and ferrite bead are used.

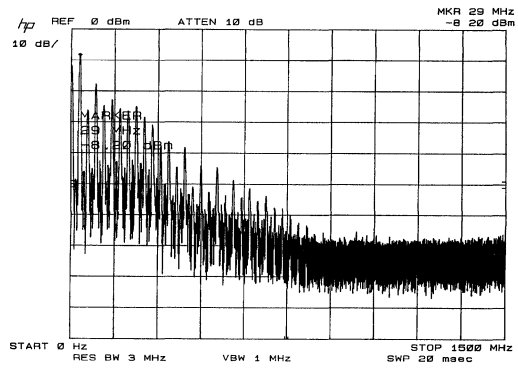
Power Supply Considerations

ICS dot clock generators function as phase-locked loops. A stable reference frequency is generated by the crystal oscillator. This frequency is divided down by a variable modulus frequency divider and fed to the reference input of the phase comparator. The feedback input of this phase comparator is fed by a second variable modulus frequency divider; however, this divider chain is driven by a voltage-controlled oscillator (VCO). The output of the phase comparator is a tristate signal which produces a pulse which has a width proportional to the phase difference between the reference and feedback inputs. The polarity of these error pulses is dependent on whether the feedback input leads or lags the reference input. These correction pulses are integrated in the loop filter and are applied to the VCO input in such a polarity as to minimize the phase error. In a perfect system this loop would settle with no remaining phase error and remain there until a new frequency was required and different modulo divisors were selected. In practice, the loop can correct for external disturbances as long as these disturbances occur more slowly than the loop natural frequency. Changes in power supply voltage affect the gain of the VCO, and the phase comparator. If they happen slowly enough, the loop compensates and no error is introduced. Step changes cannot be compensated for and must be eliminated.

XTAL OSC



ICS Dot Clock Generator



Output Spectrum

When a higher voltage supply is available, the simplest approach is to regulate the analog supply voltage and eliminate the disturbance. In desktop PCs the + 12 volt supply can be used either with a three terminal regulator or a zener diode and dropping resistor.

Laptop and notebook computers pose a more difficult problem in that a higher voltage supply is not usually available. The laptop/notebook electrical environment is more benign than the desktop computer environment, as there is no provision for using add-on boards that may inject unknown quantities of noise into the system. ICS dot clock generators are not particularly critical as to absolute supply voltage level, only to step disturbances. A series resistor and bypass tantalum electrolytic capacitor can be used to limit the rate of change in supply voltage to a rate that can be handled by the phase-locked loop. Two configurations are shown. Figure B is probably better where the VGA controller presents steady-state frequency-select information to the dot clock generator. In applications where the VGA controller presents frequency-select information on a bus and strobes the dot clock generator when frequency-select data is valid. Figure C is probably more appropriate because the bus signals may overshoot and inject noise through the input protection diodes.

Summary

ICS dot clock generators have revolutionized the personal computer and workstation graphics function.The capability to generate virtually any desired frequency at less cost than a single crystal oscilator has expanded the versatility of today's graphics systems for the PC beyond where high end workstation performance was a few years ago. Size, PC board real estate, and power requirements have shrunk to the point where today's laptop and notebook computers have graphics performance nearly as good as desktop machines. Systems design of a high-performance graphics system has been simplified so that with a few design precautions outlined above high-performance graphics can be implemented in any system.

Typical Power Supply Configurations

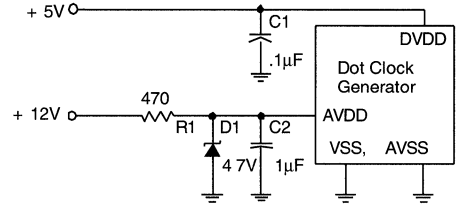


FIGURE A
OPTIMUM DESKTOP POWER CIRCUITRY

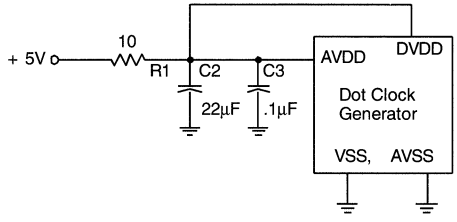


FIGURE B
LAPTOP/NOTEBOOK COMPUTER POWER CIRCUITS

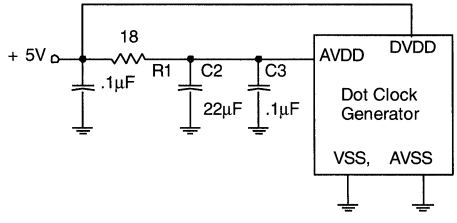
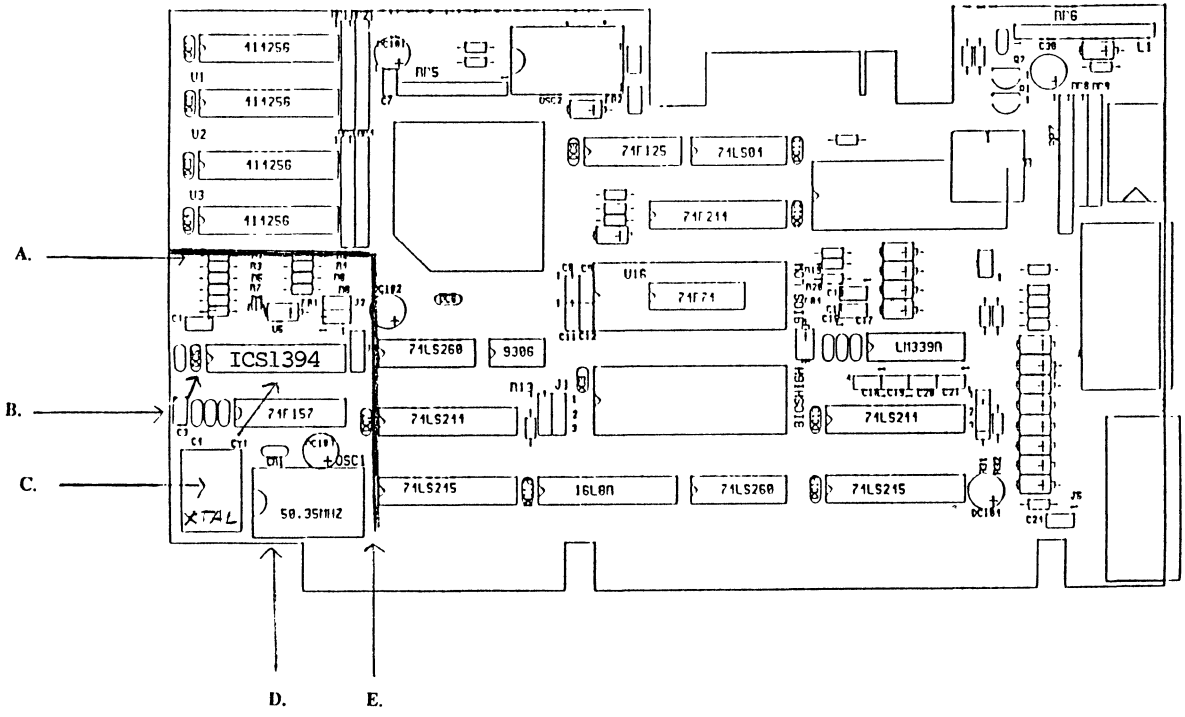


FIGURE C
LAPTOP/NOTEBOOK COMPUTER POWER CIRCUITS

Common VGA Board Layout Mistakes



Suggestions for a better layout:

A. Keep loop filter components (where required) close to dot clock generator and away from high speed DRAM circuitry.

B. Keep by-pass capacitor close to AV_{DD} pin.

C. Move XTAL close to pins XTAL1 and XTAL2. Keep fast logic signals away from this area.

D. Move oscillator can up between RAM and dot clock passive components.

E. Break ground plane level to create unipotential ground connection for dot clock circuitry.

Understanding ICS Data Sheet Jitter Specifications

Introduction

ICS clock generator devices utilize frequency synthesis based on phase locked loop (PLL) technology. Unless carefully designed, PLL-based clock generators are subject to excessive period variation, or "jitter." This applications brief will help in the understanding of ICS jitter specifications.

In most processor and time keeping applications, an excess of clock jitter does not affect operation. However, in other applications such as video, data acquisition or data recovery, clock jitter characteristics can be an important system design consideration. ICS is the most experienced manufacturer of video and processor clock devices and has perfected PLL based clock design. ICS produces clock devices exhibiting the lowest jitter and the least susceptibility to power supply noise.

Understanding ICS Jitter Specifications

Many of the ICS clock generator data sheets list output clock jitter specifications in the AC Characteristics section. ICS defines clock jitter as the difference in time of any given clock period as compared to the mean clock period, which is defined as 1/frequency. This can be expressed as time (psec) or as a percentage of the clock period.

Jitter, Absolute is the maximum deviation that would be expected (plus or minus) from a mean clock period.

Jitter, 1 Sigma is similar to an *average* deviation that would be expected (plus or minus) from a mean clock period. This specification assumes that, statistically, a sample of clock cycle periods follow a normal probability function, which indeed it typically does. *Jitter, 1 Sigma* is the jitter value at one standard deviation (one sigma) of the jitter measurement population. This specification is useful in graphics applications.

How ICS Clock Jitter is Measured

ICS characterizes output clock jitter using a Stanford Research SR620 Time Interval Analyzer. This instrument is set up to take 2,000 clock period samples over a several second period, therefore, random noncontiguous clock periods are sampled. The measure data provided by the instrument is the *typical* value listed in the data sheet (the SR620 provides both *1 Sigma* and *Absolute* measurements). The *maximum* value listed is the worst case measurement expected over the output frequency range, changes in operating conditions such as supply voltage and temperature, and changes in the semiconductor process.

Clock Output Frequency Accuracy and Input Reference Topics

This application note addresses output frequency accuracy of ICS Clock Synthesizers. Output frequency accuracy is determined both by the programmable step size of the PLL and input reference frequency accuracy. Input reference circuits are also discussed, with emphasis on using a discrete quartz crystal device.

Determining Your Frequency Accuracy Needs

ICS clock synthesizer devices are used in a diversity of applications all of which have different clock accuracy requirements. For example, in VGA graphics applications, the pixel clock frequency can easily tolerate an inaccuracy of 0.5% (5,000 ppm or part-per-million) or more since CRT timing is uncritical. This is also true for the CPU and other system clocks in mother board applications, as long as maximum clock rates are not taken to literally. There are, however, mother board applications that must have greater accuracy. Floppy disk drive control chips typically require a 24 MHz reference clock that is accurate to 0.1% (1,000 ppm). Modem and SCSI chips typically specify 0.002-0.005% (20-50 ppm) accuracy. Clocks used on the motherboard for time keeping purposes will create a 1 minute-per-month inaccuracy for every 0.0023% (23 ppm) deviation from ideal frequency. Musical instrument synthesis demands highly accurate clocks since even a small error can produce audible beating with another instrument.

With improved clock frequency accuracy comes increased component cost and design complexity. System clock accuracy requirements should therefore be approached realistically.

Clock Synthesizer Multiplication Ratio Granularity

ICS frequency generator ICs use the common PLL (Phase-Locked-Loop) technique for clock generation. Figure 1 shows a simplified block diagram of a PLL based clock generator which is applicable to all ICS clock generators. This approach to clock generation uses an input reference frequency that is multiplied by an integer ratio to obtain the desired output frequency. Once the PLL is "in lock" (typically several milli-seconds after power up), the output frequency of the chip is related to the reference frequency *exactly* by this programmed multiplication ratio.

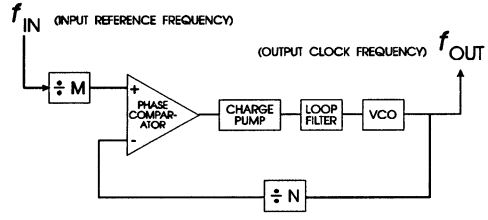


Figure 1
Simplified Diagram of PLL-Based Clock Generator Circuit

Referring to the PLL circuit in Figure 1,

$$f_{OUT} = f_{IN} \frac{N}{M}.$$

N and *M* are limited to a range of integer values that are predetermined in the clock synthesizer design. Considering this limitation of discrete values, with a given f_{IN}, f_{OUT} can only be increased or decreased in finite step sizes.

Thus, a desired output frequency (the target frequency) may not be hit exactly with a given reference frequency. The size of the minimum frequency steps will be determined by the devices *N* and *M* range. As an example, in the AV9107, *N* can be assigned integer values from 2 to 128 and *M* from 2 to 32. Using a 14.31818 MHz reference, if an output frequency of 50 MHz is desired, the closest output frequencies achievable are 49.88 MHz (N/M = 108/31) or 50.11 MHz (N/M = 7/2). In general, the AV9107 will have an approximate frequency error of 0.25% due to the programming granularity.

Some of the ICS clock synthesizer data sheets list both *target* and *actual* frequencies of the device. The *target frequency* is the typical value required for the intended application. For example, for processor clock devices, target frequencies are typically round numbers such as 20, 25, 33.3 or 50 MHz relating to the rated CPU speed. However, because the typical processor clock IC uses a 14.31818 MHz reference frequency, these exact target frequencies cannot be obtained within practical limits of *N* and *M* values. (The reference frequency of 14.31818 MHz is chosen because it is a common system clock frequency and quartz crystals at this frequency are readily available.) Furthermore, there is no reason for a processor clock to be extremely accurate (although it should be stable with little jitter and maintain a good duty cycle).

The *actual frequency* listed in the data sheet represents the output frequency of the device as determined by multiplying the *ideal* reference frequency of the device (exactly 14.31818 MHz) by the preprogrammed PLL ratio. Again, the PLL ratio is programmed to obtain an *actual frequency* as close to the *target frequency* as possible, within the limitation of the device's *N* and *M* integer ranges.

INPUT REFERENCE CLOCKS

Again by nature of the PLL technique, there will be a direct correlation between the accuracy of the input reference frequency and that of the output frequency. A +0.1 % error in the reference frequency will result in a +0.1 % error in the output frequency (deviation from *actual frequency* where applicable).

When choosing a reference frequency generator, precision is associated with cost. The most accurate and costly reference is a crystal oscillator module. The more common and less expensive approach is to use a discrete external quartz device (most ICS clock chips have built in crystal oscillator circuitry).

Any stable and continuous clock signal (within the specified frequency range) can be used as a reference clock for ICS clock chips. Special circuit considerations are advised when a clock signal, such a system clock or crystal oscillator module output, is used to drive an ICS clock generator that contains an integrated crystal oscillator circuit. Please refer to the device data sheet or contact ICS Applications Engineering.

Use of the Crystal Oscillator Module

A crystal oscillator module is a hybrid device that contains a quartz crystal, an oscillator circuit and an output buffer for the clock output. Since the internal circuit is trimmed during manufacturing, very good frequency accuracy and stability are achieved. These devices commonly yield accuracy's of +\- 20 ppm and exhibit excellent stability over time, temperature, and power supply voltage. The device requires a power supply and typically outputs a CMOS TTL-compatible output clock signal.

Use of the Discrete Quartz Crystal Device

Most ICS frequency generators contain an integral crystal oscillator circuit. With such devices, an external quartz crystal is connected between two specified device pins. This forms a complete parallel-resonant crystal oscillator circuit (also known as a Pierce oscillator). In most cases

the only external component required is the quartz crystal, since the required load capacitors and feedback resistor are integrated onto the chip as well. The complete oscillator circuit is shown in Figure 2. With careful design, accuracy to within +/- 100 ppm can be achieved.

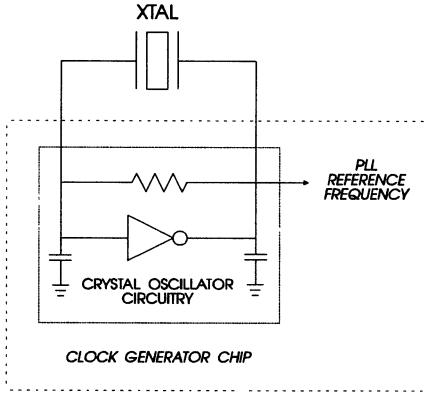


Figure 2
ICS Clock Generator
Crystal Oscillator Circuit

Quartz crystal devices can be specified by the crystal manufacturer for either series or parallel resonant operation. All ICS clock generator devices use parallel resonant operation, sometime referred to as "parallel mode". Parallel resonant crystals specify a load capacitance value which must be observed to ensure an accurate oscillation frequency.

Table 1 lists the load capacitance applied to the external crystal by various ICS clock generators. This is the total measured load capacitance which accounts for stray capacitance in the device package and printed circuit traces (short lead length used).

The load capacitance on the crystal can be increased by applying external load capacitors as shown in Figure 3. This is useful when the crystal's specified load capacitance is above that provided the provided by the clock generator. This is also used when no internal load capacitors are provided (refer to device data sheet).

ICS DEVICE	LOAD CAPACITANCE TO CRYSTAL
AV9107	12 pf
AV9110	12 pf
AV9128	12 pf
AV9129	12 pf
AV9154	12 pf
AV9155	12 pf
ICS1494	15 pf
ICS1562	11 pf
ICS1567	15 pf
ICS1694	15 pf
ICS2407	15 pf
ICS2409	15 pf
ICS2439	15 pf
ICS2494	15 pf
ICS2595	15 pf
ICS2655	15 pf
ICS5300	12 pf
ICS9132	7.5 pf

Table 1
ICS Clock Generator
Capacitive Load to Crystal

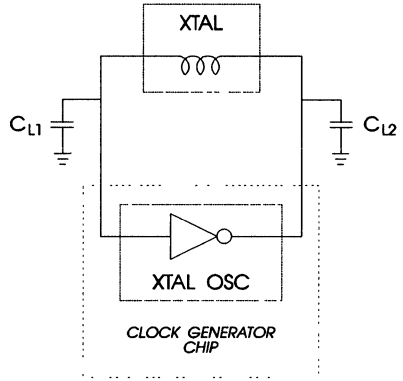


Figure 3
Connection of External Load Capacitors to Clock Generator Chip

The load presented to the crystal in Figure 3 is

$$C_L = \frac{C_{L1} \cdot C_{L2}}{C_{L1} + C_{L2}}.$$

C_{L1} and C_{L2} should be equivalent values.

Calculating Crystal Oscillation Frequency Accuracy

When a quartz crystal is operated in a series resonant oscillator, the crystal oscillates at it's series resonant frequency determined by L_M and C_M (the crystal's motional inductance and capacitance) as shown in Figure 4.

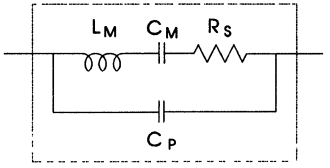


Figure 4
Electrical Model of Quartz Crystal

In a parallel resonant crystal oscillator circuit, such as used in ICS clock synthesizer devices, an LC tank circuit is created as illustrated in Figure 5. C_{EFF} is the lump capacitance consisting of C_M, C_P, and external C_L:

$$C_{EFF} = \frac{(C_L + C_P) \bullet C_M}{(C_L + C_P) + C_M}$$

The resonant frequency can then be calculated as:

$$f_{RESONANCE} = \frac{1}{2p\sqrt{L_M C_{EFF}}}.$$

The resistance R_S in the crystal has no effect on resonance frequency. However, the active circuitry of the oscillator, represented by the inverter in Figure 5, must have enough "negative resistance" to overcome the loss imposed by R_S. This allows the LS tank voltage amplitude to increase and maintain a full oscillation voltage swing. Most crystal manufactures recommend a negative resistance magnitude of at least five times the R_S (or ESR) value to ensure oscillator start up; ICS crystal oscillator circuits have a negative resistance magnitude above 250 ohms.

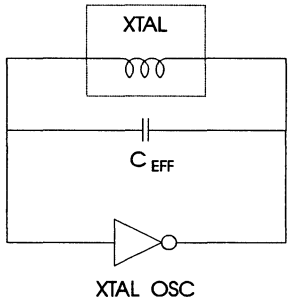


Figure 5
Electrical Model of Parallel Resonant Quartz Crystal Oscillator Circuit

The parallel resonant frequency of the crystal oscillator is higher than the series resonant frequency of the crystal. The fractional frequency "pulling" or the fractional amount that the parallel resonant frequency will be above the series resonate frequency can be calculated as

$$P = \frac{C_M}{2 \cdot C_L}.$$

If we know f_S, the series resonant frequency of the crystal, we can then calculate f_P, the parallel resonant frequency as

$$f_P = (1 + P) f_S.$$

Let's take the example of a series 14.31818 MHz crystal used with the AV9155. A typical value of C_M is 20×10^{-15} farad (the crystal manufacturer can give you this information). From Table 1, we find that C_L presented by the AV9155 is 12 pf. In this case, P is calculated to be 0.0008333 and f_P is calculated to be 14.33011 MHz which is 833 ppm (parts per million) above the series resonant frequency.

We can also use the above equations to determine oscillation error caused by total C_L error. In the example of using the AV9155 where typical circuit C_L is 12 pf, if we assume that total C_L variation can be +/- 3 pf, then oscillation frequency error will be from -166.7 ppm to +277.8 ppm. Even if assuming that external circuit capacitance can be controlled, just considering the variation of the AV9155's internal load capacitors, which vary -/- 10% or +/- 1 pf, would account for a oscillation frequency error of -166 ppm to +75 ppm. Remember that oscillator error due to C_L deviation is in addition to other errors such as the rated crystal frequency tolerance and the effects of crystal temperature and aging (consult the crystal's data sheet).

Crystal Power Dissipation

Crystal manufactures typically specify a suggested crystal power dissipation range. This is the range within which the crystal's temperature will not rise to the point of causing excessive oscillation frequency drift. Maximum crystal power dissipation is also typically listed. Well above the suggested dissipation range, this is the limit above which crystal damage can occur (it will stop working), over a period of time.

Most through-hole mount crystals specify a suggested power dissipation of about 1 mW, well suited for ICS clock generators. This is also true for the standard larger-sized surface mount crystals.

Problems can arise with some smaller types of surface mount crystals. A typical 14.318 MHz surface mount crystal used with an ICS clock generator will dissipate about 200 to 500 micro watts, depending on which clock generator is used. Maximum crystal power ratings of only 100 micro watts or lower are not uncommon, however most crystal manufactures will admit that this figure can be exceeded by 5-10 times. For maximum power dissipation it is best to consult directly with the crystal manufacturer.

Calculating Crystal Power Dissipation

Power dissipation within the quartz crystal is caused by oscillation current flowing through the crystal's effective series resistance, shown as R_S in Figure 4. This is commonly listed as 'ESR' (Effective Series Resistance) in the crystal data sheet. Power dissipation can be calculated as

$$P_D = I_{LC}^2 R_S,$$

where I_{LC} is the oscillation current in the LC tank circuit shown in Figure 5. It is difficult to measure I_{LC} during oscillation, therefore we measure differential voltage across the crystal and make the following substitution:

$$P_{DISS} = \left(\frac{V_{XTAL}}{|Z_{XTAL}|}\right)^2 R_S$$

Where V_{XTAL} is the RMS voltage across the crystal. Z_{XTAL} consists of both the reactance of the inductor shown in Figure 5 and resistance R_S not shown. However, at oscillation the inductive reactive is much larger than R_S and so the contribution of R_S to Z_{XTAL} can be ignored. Therefore we can make the approximation that

$$|Z_{XTAL}| \cong \omega L_M.$$

Substituting in the earlier equation we get

$$P_D \cong \left(\frac{V_{XTAL}}{\omega L_M}\right)^2 R_S.$$

By definition of a resonant circuit, the reactance's of the crystal's inductance and the external load capacitance are equal. This can be stated as

$$\omega L_M = \frac{1}{\omega C_L}.$$

Again through substitution we now get

$$P_D \cong (V_{XTAL} \bullet \omega C_L)^2 R_S$$

or

$$P_D \cong \left(\frac{\sqrt{2}}{2} V_{PK} \bullet 2\pi f C_L\right)^2 R_S,$$

where f is the frequency of oscillation and V_{PK} is the peak voltage across the crystal. Our final simplified equation is now

$$P_D \cong (1.414 \bullet V_{PK} \bullet \pi f C_L)^2 R_S.$$

Using the final equation it is easy to calculate approximate power dissipation with readily obtainable values. V_{PK} can be measured with a high speed differential oscilloscope (low capacitance probes must be used), or the curves of Figures 6 or 7 can be used for the following list of devices: AV9107, AV9110, AV9128, AV9129, AV9154, AV9155.

As an example, lets say that we are operating an AV9155 with a VDD of 5 volts using a 14.318 MHz crystal with an R_S (or ESR) rating of 35 ohms. From Table 1 we find that C_L = 12 pf and from Figure 6 we find that V_{PK} = 2.5 volts. Substituting values in the final equation above we determine that crystal power dissipation is approximately 127 micro-watts.

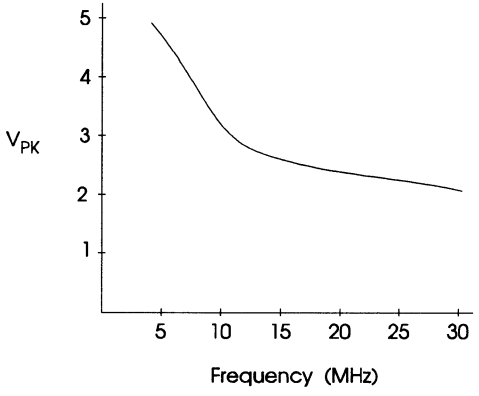


Figure 6
Peak Voltage Across Crystal
With VDD = 5.0 Volts

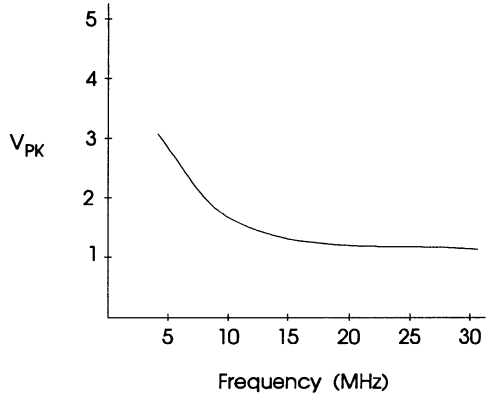


Figure 7
Peak Voltage Across Crystal
With VDD = 3.0 Volts

ICS

Video Timing Generator Product

Standard Frequency Patterns

ICS1494 Pattern Request Form

ICS produces a selection of standard pattern **ICS1494**'s pre-programmed for compatibility with many popular VGA chipsets. Custom patterns are also available, although a significant volume commitment and/or one-time mask charge will apply. Contact ICS sales for details.

ICS Part Number	ICS1494-523	ICS 1494-527	ICS1494-530	ICS1494-535	ICS 1494-539	ICS1494-540	ICS1494 543	ICS1494 544
Compatible VGA Chipsets	Tseng Labs ET4000	Cirrus Logic GD5320 GD6410	NCR 77C22E	ATI	Tseng Labs ET4000 (2X Freq)	Radius	Supermac	Seiko-Epson
Video Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	25 175	XTAL	XTAL	42.950	25 175	57 283	14 318	28 636
1	28 322	16 257	16 257	48.770	28 332	12.273	EXT	42 105
2	32.514	EXTFREQ	EXTFREQ	92 400	32.514	14 500	12 273	47 846
3	36 000	32.514	32 514	36 000	36 000	15 667	15 667	78 431
4	40 000	25 175	25 175	50 350	40 000	112 000	17 734	XTAL
5	44 900	28 322	28 322	56.644	44 900	126 000	25 175	21 053
6	65 000	24 000	24 000	EXT	50 350	30.240	30.240	50.350
7	84.000	40.000	40 000	44.900	65 000	91 200	13.500	25 175
8	25 175	XTAL	25.175	30 240	33 400	120 000	14.750	EXT
9	28 322	16.257	28 322	32.000	37.575	48.000	14 187	3.000
A	40.000	EXTFREQ	36.000	110 000	31 480	50 675	55.000	6.000
B	44.900	36 000	65.000	80.000	41 750	55.300	57.283	8.000
C	32 514	25.175	44.900	39 910	55 110	64.000	64.000	10 000
D	28 322	28.332	50 000	44 900	74 160	68.750	80 000	12 000
E	36.000	24 000	56 000	75.000	77 250	88 500	100.000	16 000
F	65.000	40.000	75.000	65 000	80 000	51.270	130.480	20 000
10	25 175	XTAL	25 175	42.950	50.350	100.000	28.322	25.000
11	28 322	65 028	28 322	48.770	56 664	95.200	36.000	30.000
12	32.514	EXTFREQ	40 000	92.400	65.028	55 000	40 000	32 000
13	36 000	36 000	65 000	36 000	72 000	60.000	40.900	33 000
14	40 000	25 175	44.900	50.350	80 000	63.000	44.900	40.000
15	44 900	28.332	50 000	56.644	89 800	99.522	50.000	44.000
16	56.000	24 000	56 000	EXT	75 000	130 000	62 000	46.000
17	65 000	40.000	75.000	44 900	108.000	80.000	65.000	50 000
18	25.175	44 900	25 175	30 240	70 000	25.175	75 000	60.000
19	28 322	50 344	28 322	32 000	75 000	28 322	89.211	66.000
1A	32.514	16.257	EXTFREQ	110 000	85.000	48 000	99 522	70 000
1B	40 000	32.514	EXTFREQ	80 000	90 000	76 800	103.140	80 000
1C	44.900	56 644	60 000	39.910	95.000	38 400	107 350	90 000
1D	60 000	20 000	80.000	44 900	110.000	43.200	111 518	100.000
1E	80.000	50 000	EXTFREQ	75.000	115.000	61 440	113.484	110.000
1F	84 000	80.000	EXTFREQ	65 000	120.000	EXT	122 320	120.000

Standard frequency patterns are available and are included as an example.
Standard frequencies shown have been specified by and are supported by the respective VGA manufacturer.
All standard patterns shown above use 14.31818 MHz as the input reference frequency.
If the internal frequency to which the ICS1494 remains locked when EXTFREQ is selected is critical, it should be specified.
Order info: ICS1494M-XXX or ICS1494N-XXX (M= SO pkg., N= DIP pkg., XXX = Pattern number)

ICS2494 Standard Patterns

ICS produces a selection of standard pattern **ICS2494**'s pre-programmed for compatibility with many popular VGA chipsets. Custom patterns are also available, although a significant volume commitment and/or one-time mash charge will apply. Contact ICS sales for details.

ICS Part Number	ICS2494-236 ICS2494A-310*[1]	ICS 9294-237 ICS2494A-304*[2]	ICS2494-240	ICS2494-244 ICS2494A 317*[3]	ICS2494-245/307	ICS2494-247	ICS2494-253	ICS2494-256
Compatible VGA Chipsets	Cirrus Logic GD6410	Tseng Labs ET4000 ET400-W32 Acer M3125	Texas. Instr TMS34010 TMS34020	Motherboard Applications (CPU Clocks)		Cirrus Logic GD5320	NCR 77C22E	S3 86C911 86C924
Video Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	XTAL	50.350	25.175	20 000	50.350	XTAL	25.175	25.175
1	65.028	56.644	28.332	24.000	56 644	16.257	28.322	28.322
2	EXTFREQ	65 000	28.636	32.000	65 000	EXTFREQ	40.000	40.000
3	36.000	72 000	36.000	40.000	72 000	32.514	65 000	EXTFREQ
4	25.175	80 000	40.000	50.000	80.000	25.175	44 900	50.000
5	28.322	89.800	42.954	66.667	89.800	28 322	50.000	77.000
6	24.000	63 000	44.900	80.000	63.000	24.000	130.000	36.000
7	40.000	75.000	57 272	100.000	75.000	40.000	75.000	44.889
8	44.900	25 175	60.000	54.000	25.175	XTAL	25 175	130.000
9	50 350	28.322	63 960	70.000	28.322	16.257	28.322	120.000
A	16.257	31 500	75.000	90.000	31.500	EXTFREQ	EXTFREQ	80.000
B	32.514	36.000	80.000	110.000	36.000	36.000	EXTFREQ	31.500
C	56.644	40.000	85 000	25.000	40.000	25.175	60.000	110.000
D	20.000	44.900	99.000	33.333	44.900	28.322	80 000	65.000
E	41.539	50.000	102 000	40.000	50.000	24 000	EXTFREQ	75.000
F	80.000	65.000	108.000	50.000	77.500	40.000	EXTFREQ	72.000
Memory Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	32.900	40.000	64 000	16.000	40.000	31 000	50.000	55.000
1	35.600	41.612	40 000	24.000	41.612	36.400	60.000	75.000
2	43.900	44.744	48.000	50.000	44.744	43.900	65.000	70.000
3	49.100	50.000	60.000	66 667	50.000	49.100	75.000	80 000

*1 ICS2494A-310 directly replaces ICS2494-236.
*2 ICS2494A-304 directly replaces ICS2494-237.
*3 ICS2494A-317 directly replaces ICS2494-244.
*4 ICS2494A-318 directly replaces ICS2494-266.
Standard frequencies shown have been specified by and are supported by the respective VGA manufacturer.
All standard patterns shown above use 14.31818 MHz as the input reference frequency.
Order info: ICS2494M-XXX or ICS2494N-XXX (M= SO pkg., N= DIP pkg., XXX= Pattern number)
ICS2494AM-XXX or ICS2494AN-XXX (M= SO pkg., N= DIP pkg., XXX= Pattern number)

ICS Part Number	ICS2494-260	ICS2494-263	ICS2494 266 ICS2494-318*4	ICS2494-271/321	ICS2494-273	ICS2494-275	ICS2494-277	ICS2494-280	ICS2494-281
Compatible VGA Chipsets	Weitek W5086 W5186	NCR 77C22E	Cirrus Logic GD5410		Headland HT216 HT216-32	S3 86C801 86C805 86C928	NCR 77C22E+	S3 86C801 86C805	Tseng
Video Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	50.350	25.175	30.250	25.175	25 175	25 175	25 175	25.175	50 350
1	56.644	28.322	65 000	28 322	28 322	28.322	28.322	28.322	56.644
2	33.250	36.000	85 000	EXT	40.000	40.000	36.000	40.000	65.000
3	52.000	65.000	36 000	44 900	32.500	EXTFREQ	65.000	EXT	72.000
4	80.000	44.900	25.175	41.539	50 350	50.000	44.900	50.000	80.000
5	63.000	50.000	283.322	78.000	65.000	77 000	50.000	77 000	89.800
6	EXTFREQ	80.000	34.000	79.200	38 000	36.000	80.000	36 000	63.000
7	75 000	75 000	40 000	80.000	44.900	44.889	75.000	44.889	75.000
8	25.175	25.175	44.900	31.469	31.500	130 000	56.644	130.000	83 078
9	28.322	28.322	50.350	35.402	36.000	120 000	63 000	120.000	93.463
A	31.500	EXTFREQ	31 500	EXTFREQ	80.000	80.000	72.000	80.000	100.000
B	36.000	EXTFREQ	32.500	56.125	63.000	31 500	130.000	31.500	104.000
C	40.000	60 000	63.000	51.924	50.000	110.000	90.000	110.000	108.000
D	44.900	80.000	72.000	91.000	100.00	65.000	100.000	65.000	120 000
E	50.000	EXTFREQ	75.000	87 406	76.000	75.000	110.000	75.000	130.000
F	65.000	EXTFREQ	80.000	36.000	110.000	94.500	120.000	94.500	134.700
Memory Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	40.000	50.000	36.000	51.924	70.000	45 000	50.000	55 000	50.000
1	33 333	40.000	44 000	41 539	63.830	38.000	60.000	60.000	55.000
2	45.000	65.000	49.000	44 900	60.000	52 000	65.000	70 000	60.000
3	50.000	75 000	40 000	56 125	81.000	50.000	75.000	65.000	65.000

*1 ICS2494A-310 directly replaces ICS2494-236.
*2 ICS2494A-304 directly replaces ICS2494-237.
*3 ICS2494A-317 directly replaces ICS2494-244.
*4 ICS2494A-318 directly replaces ICS2494-266.
Standard frequencies shown have been specified by and are supported by the respective VGA manufacturer.
All standard patterns shown above use 14.31818 MHz as the input reference frequency.
Order info: ICS2494M-XXX or ICS2494N-XXX (M= SO pkg., N= DIP pkg., XXX= Pattern number)
ICS2494AM-XXX or ICS2494AN-XXX (M= SO pkg., N= DIP pkg., XXX= Pattern number)

ICS Part Number	ICS2494A-305	ICS2494-306	ICS2494-314	ICS2494A-319	ICS2494A-320	ICS2494A-322	ICS2494A-324
Compatible VGA Chipsets	S3 86C924	Cirrus Logic GD6410 GD6412	Texas Instruments		AdvanceLogic ALG2101 ALG2201		Tseng Labs ET4000 ET4000 W32
Video Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	25.175	XTAL	12.273	25.175	50.350	20.000	50.000
1	28.322	65.000	13.500	28.322	56.644	20.480	56.644
2	40.000	EXTFREQ	14.750	40.000	89.800	24.576	65.000
3	EXTFREQ	36.000	25.175	72.000	72 000	24.704	72.000
4	50.000	25.175	28 322	50.000	75 000	25.216	80 000
5	77.000	28 322	36.000	77.500	65.000	25.248	89.800
6	36.000	24.000	40.000	36.000	63.000	25.600	63.000
7	44.889	40 000	44 900	44.900	80.000	26.000	75.000
8	130.000	44.900	50.000	63.000	57.272	28.800	83.078
9	120.000	50 350	64.000	100.000	85.000	29.491	93 463
A	80.000	16.257	75.000	80.000	94.000	30.720	100.000
B	31.500	32.514	80.000	31.500	96.000	32.768	104.000
C	110.000	56.644	100.000	110.000	100.000	33.6000	108.000
D	65.000	20.000	108.000	65.000	108.000	44.736	120.000
E	75.000	41.539	120.000	75.000	110.000	9.600	130.000
F	94.500	80.000	135.000	94.500	77.000	20.500	134.700
Memory Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	55.000	32.900	32.000	48.000	76 000	15.360	50.000
1	75.000	35.600	40.000	52.500	80.000	13.947	56.000
2	70.000	43.900	48.000	55 000	85.000	13.947	60.000
3	80.000	39.900	60.000	50.000	90.000	24.000	65.000

*1 ICS2494A-310 directly replaces ICS2494-236.
*2 ICS2494A-304 directly replaces ICS2494-237.
*3 ICS2494A-317 directly replaces ICS2494-244.
*4 ICS2494A-318 directly replaces ICS2494-266.
Standard frequencies shown have been specified by and are supported by the respective VGA manufacturer.
All standard patterns shown above use 14.31818 MHz as the input reference frequency.
Order info: ICS2494M-XXX or ICS2494N-XXX (M= SO pkg., N= DIP pkg., XXX= Pattern number)
ICS2494AM-XXX or ICS2494AN-XXX (M= SO pkg., N= DIP pkg., XXX= Pattern number)

ICS Part Number	ICS2494-325	ICS2494-326	ICS2494-330	ICS2494-334	ICS2494-	ICS2494	ICS2494-
Compatible VGA Chipsets	Maxtek						
Video Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	25.175	66.000	18.432	25.175			
1	28.322	62.000	31.470	28.322			
2	31.500	61.236	50.000	31.500			
3	36.000	61.000	EXTFREQ	36.000			
4	40.000	60.500	48.000	40.000			
5	44.900	60.000	54.000	44.900			
6	50.350	59.300	59.200	50.000			
7	65.000	59.000	75.500	65.000			
8	56.644	58.968	96.000	75.000			
9	72.00	57.200	108.778	77.500			
A	75.000	56.200	73.410	80.000			
B	77.000	55.500	50.490	90.000			
C	80.000	40.000	110.439	100.000			
D	94.500	38.200	100.000	110.000			
E	120.000	32.500	125.000	126.000			
F	108.000	30.500	135.000	135.000			
Memory Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	45.000	48.000	47.720	60.000			
1	50.000	50.000	45.000	50.000			
2	65.000	40.000	40.000	55.000			
3	70.000	60.000	50.000	50.000			

*1 ICS2494A-310 directly replaces ICS2494-236.
*2 ICS2494A-304 directly replaces ICS2494-237.
*3 ICS2494A-317 directly replaces ICS2494-244.
*4 ICS2494A-318 directly replaces ICS2494-266.
Standard frequencies shown have been specified by and are supported by the respective VGA manufacturer.
All standard patterns shown above use 14.31818 MHz as the input reference frequency.
Order info: ICS2494M-XXX or ICS2494N-XXX (M= SO pkg., N= DIP pkg., XXX= Pattern number)
ICS2494AM-XXX or ICS2494AN-XXX (M= SO pkg., N= DIP pkg., XXX= Pattern number)

ICS2492 Pattern Request Form

In addition to the pattern below, custom patterns are also available, although a significant volume commitment and/or one-time mask charge will apply. Contact ICS sales for details.

ICS Part Number	ICS2492-453		ICS2492-Custom Pattern # 1
Address FS3-0 (Hex)	Frequency (MHz)	Application	Frequency (MHz)
0	20	286-10	
1	24	-12	
2	32	386-16	
3	40	-20	
4	50	-25	
5	66.6	-33	
6	80	-40	
7	100	-50	
8	54	TURBO-27	
9	70	-35	
0	90	-45	
B	110	-55	
C	25	486-25	
D	33.3	-33	
E	40	-40	
F	50	-50	
Address MS0 (Hex)	Frequency (MHz)	Application	Frequency (MHz)
0	16	AT-BUS	
1	24	FDC	

Custom pattern # 1 reference frequency = _____

The standard frequency shown has been specified by and is supported by the respective VGA manufacturer.
The standard pattern shown above uses _____ MHz as the input reference frequency.
Order info: ICS2492M-XXX or ICS2492N-XXX (M= SO pkg., N= DIP pkg., XXX= Pattern number)

ICS2495 Pattern Request Form

Custom patterns are also available, although a significant volume commitment and/or one-time mask charge will apply. Contact ICS sales for details.

ICS Part Number	ICS2495-	ICS2495-
Compatible VGA Chipsets	Custom Pattern # 1	Custom Pattern # 2
Video Clock Address(HEX)	Frequency (MHz)	Frequency (MHz)
0		
1		
2		
3		
4		
5		
6		
7		
8		
9		
A		
B		
C		
D		
E		
F		
Memory Clock Address(HEX)	Frequency (MHz)	Frequency (MHz)
0		
1		
2		
3		

Custom pattern # 1 reference frequency = _____
Custom pattern # 2 reference frequency = _____
Standard frequencies shown have been specified by and are supported by the respective VGA manufacturer.
All standard patterns shown above use 14.31818 MHz as the input reference frequency.
If the internal frequency to which the ICS2495 remains locked to is critical when EXTFREQ is selected, it should be specified.
Order info: ICS2495M-XXX or ICS2495N-XXX (M= SO pkg., N= DIP pkg., XXX= Pattern number)

ICS2496 Pattern Request Form

ICS produces a selection of standard pattern **ICS2496**'s pre-programmed for compatibility with many popular VGA chipsets. Custom patterns are also available although a significant volume commitment and/or one-time mask charge will apply. Contact ICS Sales for details.

ICS Part Number	ICS2496-452	ICS2496-454	ICS2496-456
Compatible VGA Chipsets	Cirrus Logic GD6410	Cirrus Logic GD6412	Motherboard Applications (CPU Clocks)
Video Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	XTAL	XTAL	20.000
1	65.000	65.000	24.000
2	EXTFREQ	EXTFREQ	32.000
3	36.000	36.000	40.000
4	25.175	25.175	50.000
5	28.322	28.322	66.667
6	24.000	24.000	80.000
7	40.000	40.000	100.000
8	44.900	44.900	54.000
9	50.350	50.350	70.000
A	16.257	16.257	90.000
B	32.514	32.514	110.000
C	56.644	56.444	25.000
D	20.000	20.000	33.333
E	41.539	41.539	40.000
F	80.000	80.000	50.000
Memory Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	32.900	32.900	16.000
1	35.600	35.600	24.000
2	43.900	43.900	50.000
3	49.100	39.900	66.667

Standard frequencies shown have been specified by and are supported by the respective VGA manufacturer.

All standard patterns shown above use 14.31818 MHz as the input reference frequency.

Order info: ICS2496M-XXX or ICS2496N-XXX
(M=SO package, N=DIP package,
XXX=Pattern number).

ICS

GENDAC™

Products

ICS GENDACs provide highly integrated mixed-signal solutions for advanced VGA controllers. These products have been designed utilizing ICS's proven technology for exceptionally low-jitter video clock synthesizers and high-accuracy video DACs. The definitions for these products were written with the close cooperation of VGA controller manufacturers to ensure our customers maximum design flexibility. Our 16-bit pixel path devices are leading edge components for video systems and establish the industry standard with 70 hertz refresh requirements at resolutions of 1280 x 1024 pixels.

ICS GENDAC Products Selection Guide

Product Applications	ICS Device Type	Features	Package Types	Page
Personal Computer and Engineering Work Station Computer Graphics	ICS5300	8-bit Pixel Port, Triple 8-bit Video DACs, Operation to 135 MHz. 7 Selectable P-Clock Frequencies (5 Programmable).	44 Pin PLCC	275
	ICS5301	Tseng Compatibility, 8-bit Pixel Port, Triple 8-bit Video DACs, Operation to 135MHz. 7 Selectable P-Clock Frequencies (5 Programmable).	44 Pin PLCC	303
	ICS5340	16-bit Pixel Port, Triple 8-bit Video DACs, Operation to 135 MHz. 2:1 Pixel Multiplexing. 7 Selectable P-Clock Frequencies (5 Programmable). 2 Selectable and Programmable M-Clock Frequencies.	68 Pin PLCC	331
	ICS5341	Tseng Compatibility, 16-bit Pixel Port, Triple 8-bit Video DACs, Operation to 135MHz. 2:1 Pixel Multiplexing. 7 Selectable P-Clock Frequencies (5 Programmable). 2 Selectable and Programmable M-Clock Frequencies.	68 Pin PLCC	363

ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development Characteristic data and other specifications are subject to change without notice.

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development Characteristic data and other specifications are design goals ICS reserves the right to change or discontinue these products without notice.

Integrated Circuit Systems, Inc.

ICS5300 GENDAC

8-bit Integrated Clock-LUT-DAC

General Description

The ICS5300 GENDAC is a combination of dual programmable clock generators, a 256 x 18-bit RAM, and a triple 8-bit video DAC. The GENDAC supports 8-bit pseudo color applications, as well as 15-bit, 16-bit and 24-bit True Color bypass for high speed, direct access to the DACs.

The RAM makes it possible to display 256 colors selected from a possible 262,144 colors. The dual clock generators use Phase Locked Loop (PLL) technology to provide programmable frequencies for use in the graphics subsystem. The video clock contains 8 frequencies, 6 of which are programmable by the user. The memory clock has one programmable frequency location.

The three 8-bit DACs on the ICS5300 are capable of driving singly or doubly-terminated 75Ω loads to nominal 0 - 0.7 volts at pixel rates up to 135 MHz. Differential and integral linearity errors are less than 1 LSB over full temperature and V_{DD} ranges. Monotonicity is guaranteed by design. On-chip pixel mask register allows displayed colors to be changed in a single write cycle rather than by modifying the color palette.

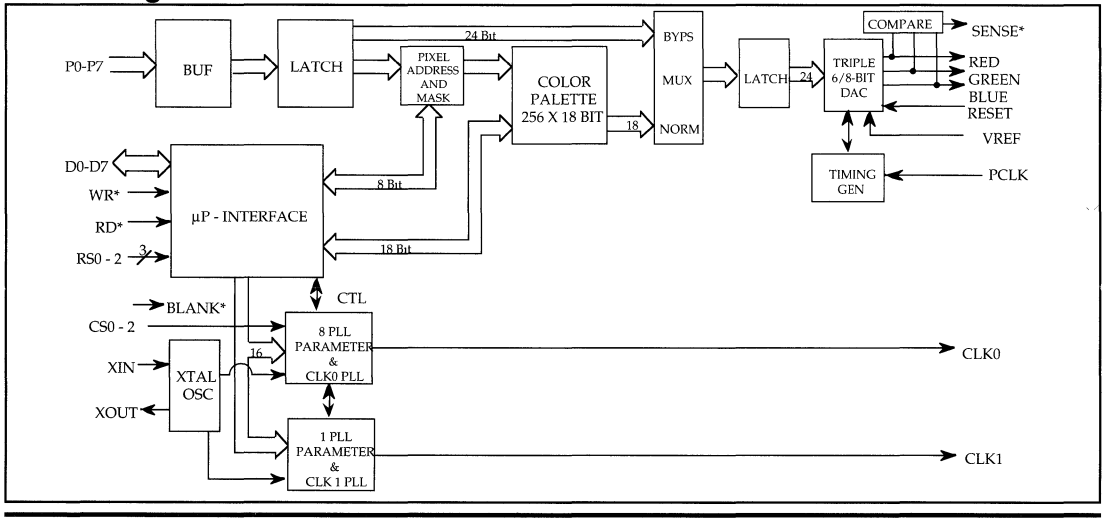
ICS is the world leader in all aspects of frequency (clock) generation for graphics, using patented techniques to produce low jitter video timing.

Features

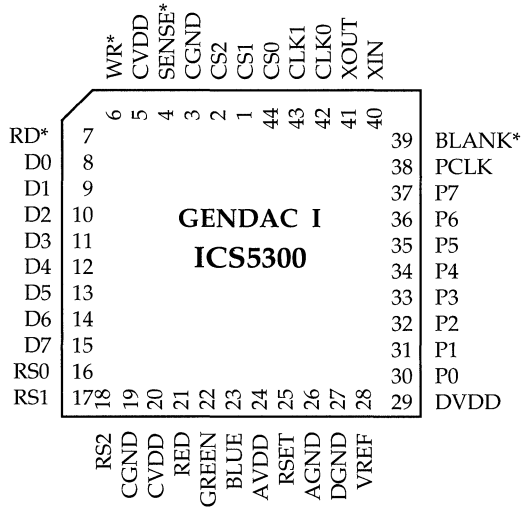
- **Triple video DAC, dual clock generator, and a color palette**
- **24, 16, 15, or 8-bit pseudo color pixel mode supports True Color, Hi-Color, and VGA modes**
- **High speed 256 x 18 color palette (135 MHz) with bypass mode and 8-bit DACs**
- **Two fixed, six programmable video (pixel) clock frequencies (CLK0)**
- **One programmable memory (controller) clock frequency (CLK1)**
- **DAC power down in blanking mode**
- **Low power operation**
- **Anti-sparkle circuitry**
- **On-chip loop filters reduce external components**
- **Standard CPU interface**
- **Single external crystal (typically 14.318 MHz)**
- **Monitor Sense**
- **Internal voltage reference**
- **135 MHz (-3), 110 MHz (-2) & 80 MHz (-1) versions**
- **Very low clock jitter**

C

Block Diagram



Pin Configuration



Pin Description (68 pin PLCC)

Symbol	Pin #	Type	Description
CS1	1	Input	Clock select 1. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output.
CS2	2	Input	Clock select 2. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output.
CGND	3	-	Ground for clock circuits. Connect to ground.
SENSE*	4	Output	Monitor Sense, active low. This pin is low when any of the red, green, or blue outputs have exceeded 335mV. The chip has on-board comparators and an internal 335mV voltage reference. This is used to detect monitor type.
CVDD	5	-	Clock Power Supply. Connect to DVDD
WR*	6	Input	RAM/PLL Write Enable, active low. This signal controls the timing of the write operation on the microprocessor interface inputs, D0-D7.
RD*	7	Input	RAM/PLL Read Enable, active low. This is the READ bus control signal. When active, any information present on the internal data bus is available on the Data I/O lines, D0-D7.
D0 - D7	8 - 15	I/O	System data bus I/O. These bidirectional Data I/O lines are used by the host microprocessor to write (using active low WR*) information into, and read (using active low RD*) information from the six internal registers (Pixel Address, Color Value, Pixel Mask, PLL Address, PLL Parameter, and Command). During the write cycle, the rising edge of WR* latches the data into the selected register (set by the status of the three RS pins). The rising edge of RD* determines the end of the read cycle. When RD* is a logical high, the Data I/O lines no longer contain information from the selected register and will go into a tri-state mode.

Pin Description (continued)

Symbol	Pin #	Type	Description
RS0 RS1 RS2	16 17 18	Input Input Input	Register Address Select 0. These inputs control the selection of one of the six internal registers. They are sampled on the falling edge of the active enable signal (RD* or WR*).
CGND	19	-	Ground for clock circuits. Connect to ground
CVDD	20	-	Clock Power Supply. Connect to AVDD
RED GREEN BLUE	21 22 23	Output Output Output	Color Signals. These three signals are the DACs' analog outputs. Each DAC is composed of several current sources. The outputs of each of the sources are added together according to the applied binary value. These outputs are typically used to drive a CRT monitor.
AVDD	24	-	Analog power supply. Connect to AVDD
RSET	25	Input	Resistor Set. This pin is used to set the current level in the analog outputs. It is usually connected through a 140Ω, 1% resistor to ground.
AGND	26	-	Analog Ground. Connect to ground
DGND	27	-	Digital Ground. Connect to ground
VREF DVDD	28 29	Input -	Internal Reference Voltage. Normally connects to a 0.1µF cap to ground. To use an external Vref, connect a 1.235V reference to this pin. Digital power supply.
P0 - P7	30 - 37	Input	Pixel Address Lines. This byte-wide information is latched by the rising edge of PCLK when using the Color Palette, and is masked by the Pixel Mask register. These values are used to specify the RAM word address in the default mode (accessing RAM). In the Hi-Color XGA, and True Color modes, they represent color data for the DACs. These inputs should be grounded if they are not used.
PCLK	38	Input	Pixel Clock. The rising edge of PCLK controls the latching of the Pixel Address Anding inputs. This clock also controls the progress of these values through the three-stage pipeline of the Color Palette RAM, DAC, and outputs.
BLANK*	39	Input	Composite BLANK* Signal, active low. When BLANK* is asserted, the outputs of the DACs are zero and the screen becomes black. The DACs are automatically powered down to save current during blanking. The color palette may still be updated through D0-D7 during blanking.
XIN	40	Input	Crystal input. A 14.318 MHz crystal should be connected to this pin.
XOUT	41	Output	Crystal output. A 14.318 MHz crystal should be connected to this pin.
CLK0	42	Output	Video clock output. Provides a CMOS level pixel or dot clock frequency to the graphics controller. The output frequency is determined by the values of the PLL registers.
CLK1	43	Output	Memory clock output. Used to time the video memory.
CS0	44	Input	Clock select 0. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output.

Internal Registers

RS2	RS1	RS0	Register Name	Description (all registers can be written to and read from)
0	0	0	Pixel Address WRITE	There is a single Pixel Address register within the GENDAC. This register can be accessed through either register address 0,0,0 or register address 0,1,1. A read from address 0,0,0 is identical to a read from address 0,1,1. Writing a value to address 0,0,0 performs the following operations: a) Specifies an address within the color palette RAM. b) Initializes the Color Value register. Writing a value to address 0,1,1 performs the following operations: a) Specifies an address within the color palette RAM. b) Loads the Color Value register with the contents of the location in the addressed RAM palette and then increments the Pixel Address register. Writing to this 8-bit register is performed prior to writing one or more color values to the color palette RAM.
0	1	1	Pixel Address READ	Writing to this 8-bit register is performed prior to reading one or more color values from the color palette RAM.
0	0	1	Color Value	The 18-bit Color Value register acts as a buffer between the microprocessor interface and the color palette. Using a three bytes transfer sequence allows a value to be read from or written to this register. When a byte is read, the color value is contained in the least significant 6 bits , D0-D5 (the most significant 2 bits are set to zero). When writing a byte, the same 6 bits are used. When reading or writing, data is transferred in the same order - the red byte first, then green, then blue. Each transfer between the Color Value register and the color palette replaces the normal pixel mapping operations of the GENDAC for a single pixel. After writing three definitions to this register, its contents are written to the location in the color palette RAM specified by the Pixel Address register, and the Pixel Address register increments. After reading three definitions from this register, the contents of the location in the color palette RAM specified by the Pixel Address registers are copied into the Color Value register, and the Pixel Address register increments.
0	1	0	Pixel Mask	The 8-bit Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs (P0-P7). A one in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered, while a zero sets that bit to zero. The Pixel Mask register does not affect the Pixel Address generated by the microprocessor interface when the palette RAM is being accessed.

Internal Registers (continued)

RS2	RS1	RS0	Register Name	Description (all registers can be written to and read from)
1	0	0	PLL Address WRITE	Writing to this 8-bit register is performed prior to writing one or more PLL programming values to the PLL Parameter register.
1	1	1	PLL Address READ	Writing to this 8-bit register is performed prior to reading one or more PLL programming values from the PLL Parameter register.
1	1	0	Command	This8-bit register selects the color mode, for instance 8-bit Pseudo Color, Hi-Color , True Color, or XGA, and DAC power down. The registers are reset to pseudo color mode on power up.
1	0	1	PLL Parameter	There are sixteen parameter registers as indexed by PLL Address Write/ Readregisters. Parameter registers 00-0D and 0F are two bytes long and 0E is one byte long. This register set contains one control register. The bits of this register include clock select and enable functions, the rest contain PLL frequency parameters. After writing the start index address in the PLL address register, these registers can be accessed in successive two (or one) bytes. The address register auto increments after one or two bytes to access the entire register set.

Absolute Maximum Ratings

Power Supply Voltage ..... 7 V
Voltage on any other pin ..... GND – 0.5V to V_{DD} + 0.5V
Temperature under bias ..... – 40° C to 85° C
Storage Temperature ..... – 65° C to 150° C
DC Digital Output Current ..... 25 mA
Analog Output Current ..... 45 mA
Reference Current ..... –15 mA
Power Dissipation ..... 1.0 W

Note Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
DC CHARACTERISTICS (note: J)					
V_{DD}	Positive supply voltage		4.75	5.25	V
V_{IH}	Input logic "1" voltage		2.0	V_{DD} + 0.5	V
V_{IL}	Input logic "0" voltage		– 0.5	0.8	V
I_{REF}	Reference current		–7.0	–10	mA
V_{REF}	Reference voltage		1.10	1.35	V
I_{IN}	Digital input current	V_{DD} = max, GND ≤ V_{IN} ≤ V_{DD}		± 10	µA
I_{OZ}	Off-state digital output current	V_{DD} = max, GND ≤ V_{IN} ≤ V_{DD}		± 50	µA
I_{DD}	Average power supply current	I_O = max, Digital outputs unloaded		250	mA
I_{DACOFF}	DACs in power down mode	No palette access		50	mA
V_{OH}	Output logic "1"	I_O = –3.2mA, note K	2.4		V
V_{OL}	Output logic "0"	I_O = -3.2mA, note K		0.4	V
$ICLK_r$	Input Clock Rise Time	TTL levels		15	ns
$ICLK_f$	Input Clock Fall Time	TTL levels		15	ns
F_D	Frequency Change of CLK0 and CLK1 over supply and temperature	With respect to typical frequency		0.05	%

Electrical Characteristics (continued)

Symbol	Parameter	Conditions	Min	Max	Units
DAC CHARACTERISTICS (note: J)					
V_O (max)	Maximum output voltage	$I_O \leq 10$ mA		1.5	V
I_O (max)	Maximum output current	$V_O \leq 1V$		21	mA
	Full scale error	note A, B		± 5	%
	DAC to DAC correlation	note B		±2	%
	Integral Linearity, 6-bit	note B		±0.5	LSB
	Integral Linearity, 8-bit	note B		±1	LSB
	Full scale settling time*, 6-bit	note C		28	ns
	Full scale settling time*, 8-bit	note C		20	ns
	Rise time (10% to 90%)*	note C		6	ns
	Glitch energy*	note C		200	pVsec

* Characterized values only

Symbol	Parameter	Conditions	Min	Max	Units
PLL AC CHARACTERISTICS					
f_0	Clock 0 operating range		25	135	MHz
f_1	Clock 1 operating range		25	135	MHz
t_r	Output clocks rise time	25 pf load, TTL levels		1.5	ns
t_r	Output clocks fall time	25 pf load, TTL levels		1.5	ns
d_t	Duty Cycle		40/60	60/40	%
j_{1s}	Jitter, one sigma			130 ps	ps
j_{abs}	Jitter, absolute		-300 ps	300 ps	ps
f_{ref}	Input reference frequency	Typically 14.318 MHz	5	25	MHz

AC Electrical Characteristics (note: J)

Symbol	Parameter	Condition	80 MHz		110 MHz		135 MHz		Units
			Min	Max	Min	Max	Min	Max	
t_{CHCH}	PCLK period		12.5		9.09		7.4		ns
Δt_{CHCH}	PCLK jitter	note D		±2.5		+2.5			%
t_{CLCH}	PCLK width low		5		3.6		3		ns
t_{CHCL}	PCLK width high		5		3.6		3		ns
t_{PVCH}	Pixel word setup time	note E	3		3		2		ns
t_{CHPX}	Pixel word hold time	note E	3		2		1		ns
t_{BVCH}	BLANK* setup time	note E	3		3		2		ns
t_{CHBX}	BLANK* hold time	note E	3		2		1		ns
t_{CHAV}	PCLK to valid DAC output	note F		20		20		20	ns
Δt_{CHAV}	Differential output delay	note G		2		2		2	ns
t_{WLWH}	WR* pulse width low		50		50		50		ns
t_{RLRH}	RD* pulse width low		50		50		50		ns
t_{SVWL}	Register select setup time	Write cycle	10		10		10		ns
t_{SVRL}	Register select setup time	Read cycle	10		10		10		ns
t_{WLSX}	Register select hold time	Write cycle	10		10		10		ns
t_{RLSX}	Register select hold time	Read cycle	10		10		10		ns
t_{DVWH}	WR* data setup time		10		10		10		ns
t_{WHDX}	WR* data hold time		10		10		10		ns
t_{RLQX}	Output turn-on delay		5		5		5		ns
t_{RLQV}	RD* enable access time			40		40		40	ns
t_{RHQX}	Output hold time		5		5		5		ns
t_{RHQZ}	Output turn-off delay	note H		20		20		20	ns
t_{WHWL1}	Successive write interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{WHRL1}	WR* followed by read interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{RHRL1}	Successive read interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{RHWL1}	RD* followed by write interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{WHWL2}	WR* after color write	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{WHRL2}	RD* after color write	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{RHRL2}	RD* after color read	note I	8 (t_{CHCH})		8 (t_{CHCH})		8 (t_{CHCH})		cycle
t_{RHWL2}	WR* after color read	note I	8 (t_{CHCH})		8 (t_{CHCH})		8 (t_{CHCH})		cycle
t_{WHRL3}	RD* after read address write	note I	8 (t_{CHCH})		8 (t_{CHCH})		8 (t_{CHCH})		cycle
t_{SOD}	SENSE* output delay			1		1	1		µs

NOTES

A Full scale error is derived from design equation
{[(F S I_{OUT}) R_L – 2 1 (I_{REF}) R_L]/[2 1(I_{REF})R_L]} 100%

$V_{BLACK\ LEVEL}$=0V F.S I_{OUT} = Actual full scale measured output

B R= 37 5Ω, I_{REF} = – 8 88mA

C Z_l = 37 5Ω + 30 pF, I_{REF} = – 8.88mA

D This parameter is the allowed Pixel Clock frequency variation It does not permit the Pixel Clock period to vary outside the minimum values for Pixel Clock (t_{CHCH}) period

E It is required that the color palette's pixel address be a valid logic level with the appropriate setup and hold times at each rising edge of P_{CLK} (this requirement includes the blanking period)

F The output delay is measured from the 50% point of the rising edge of CLOCK to the valid analog output A valid analog output is defined when the analog signal is halfway between its successive values.

G. This applies to different analog outputs on the same device

H Measured at ± 200 mV from steady state output voltage

I This parameter allows synchronization between operations on the microprocessor interface and the pixel stream being processed by the color palette

J. The following specifications apply for V_{DD} = +5V± 0 5V, GND=0 Operating Temperature = 0°C to 70°C

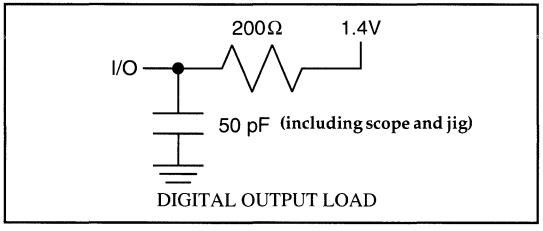
K. Except for SENSE pin.

AC Test Conditions

Input pulse levels.....V_{DD} to 3V
Input rise and fall times (10% to 90%).....3ns
Digital input timing reference level.....1.5V
Digital output timing reference level.....0.8V and 2.4V

Capacitance

C_I Digital input.....7pF
C_O Digital output.....7pF
C_{OA} Analog output.....10pF



DIGITAL OUTPUT LOAD

General Operation

The ICS5300 GENDAC is intended for use as the analog output stage of raster scan video systems. It contains a high-speed Random Access Memory of 256 x 18-bit words, three 6/8-bit high-speed DACs, a microprocessor/graphic controller interface, a pixel word mask, on-chip comparators, and two user programmable frequency generators.

An externally generated BLANK* signal can be applied to pin 39 of the ICS5300. This signal acts on all three of the analog outputs. The BLANK* signal is delayed internally so that it appears with the correct relationship to the pixel bit stream at the analog outputs.

A pixel word mask is included to allow the incoming pixel address to be masked. This permits rapid changes to the effective contents of the color palette RAM to facilitate such operations as animation and flashing objects. Operations on the contents of the mask register can also be totally asynchronous to the pixel stream.

The ICS5300 also includes dual PLL frequency generators providing a video clock (CLK0) and a memory clock (CLK1), both generated from a single 14.318 MHz crystal. There are eight selectable CLK0 frequencies of which six are programmable, and a single programmable CLK1 frequency. Default values (Table 1 and Table 2) are loaded into the appropriate registers on power up.

Video Path

The GENDAC supports four different video modes and is determined by bits 5-7 of the command register. The default mode is the 6-bit Pseudo Color mode. The other modes are the bypass 15-bit, 16-bit and 24 bit True Color.

Pseudo color

In this mode, Pixel Address and BLANK* inputs are sampled on the rising edge of the clock (PCLK) and any change appears at the analog outputs after three succeeding rising edges of the clock. The DAC outputs depends on the data in the color palette RAM.

Bypass Modes

The GENDAC supports three different bypass modes; 15-bit (5,5,5) mode, 16-bit (5,6,5) mode and the 24-bit True Color 8-bit DAC mode. In these modes, the pixel address pins P0-P7 represent the Color Data that is applied directly to the DAC. The internal RAM is bypassed. In the 15/16-bit mode two consecutive bytes contain the 15/16 bits of color data. Two consecutive rising edges of the PCLK latch the data on the P0-P7 pins into registers and the byte framing is internally synchronized with the rising edge of BLANK*. The internal pipe line delay from the "first byte" to the DAC is four PCLK rising edges. In the 24-bit True Color mode, three bytes contains the 24-bit color data. Three consecutive rising edges of the PCLK latch the data. The framing is the same as the 15/16-bit mode. The internal pipe line delay from the "first byte" to the DAC is five PCLK rising edges.

DAC Outputs

The outputs of the DACs are designed to be capable of producing 0.7 volt peak white amplitude with an I_{REF} of 8.88 mA when driving a doubly terminated 75Ω load. This corresponds to an effective DAC output load ($R_{EFFECTIVE}$) of 37.5Ω.

The formula for calculating I_{REF} with various peak white voltage/output loading combinations is given below:

$$I_{REF} = \frac{V_{PEAK\ WHITE}}{2.1 \times R_{EFFECTIVE}}$$

Note that for all values of I_{REF} and output loading:

$$V_{BLACK\ LEVEL} = 0$$

The reference current I_{REF} is determined by the reference voltage V_{REF} and the value of the resistor connected to R_{SET} pin. V_{REF} can be the internal band gap reference voltage or can be overridden by an external voltage. In both cases $I_{REF} = V_{REF}/R_{SET}$.

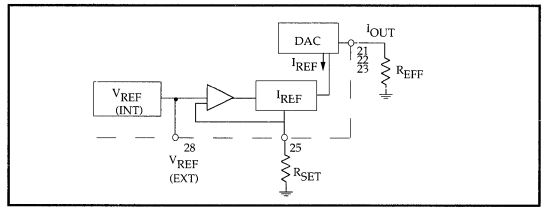


Figure 4 - DAC Set up

The BLANK* input to the GENDAC acts on all three of the DAC outputs. When the BLANK* input is low, the DACs are powered down.

The connection between the DAC outputs of the ICS5300 and the RGB inputs of the monitor should be regarded as a transmission line. Impedance changes along the transmission line will result in the reflection of part of the video signal back along the transmission line. These reflections may result in a degradation of the picture displayed by the monitor.

RF techniques should be observed to ensure good fidelity. The PCB trace connecting the GENDAC to the off-board connector should be sized to form a transmission line of the correct impedance. Correctly matched RF connectors should be used for connection from the PCB to the coaxial cable leading to the monitor and from the cable to the monitor.

There are two recommended methods of DAC termination: double termination and buffered signal. Each is described below with its relative merits:

Double Termination (Figure 1)
For this termination scheme, a load resistor is placed at both the DAC output and the monitor input. The resistor values should be equal to the characteristic impedance of the line. Double termination of the DAC output allows both ends of the transmission line between the DAC outputs and the monitor inputs to be correctly matched. The result should be an ideal reflection free system. This arrangement is relatively tolerant to variations in transmission line impedance (e.g. a mismatched connector) since no reflections occur from either end of the line.

A doubly terminated DAC output will rise faster than any singly terminated output because the rise time of the DAC outputs is dependent on the RC time constant of the load.

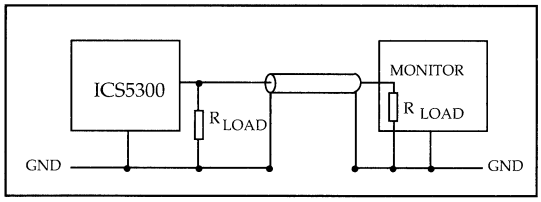


Figure 1 - Double Termination

Buffered Signal (Figure 2)
If the GENDAC drives large capacitive loads (for instance long cable runs), it may be necessary to buffer the DAC outputs. The buffer will have a relatively high input impedance. The connection between the DAC outputs and the buffer inputs should also be considered as a transmission line. The buffer output will have a relatively low impedance. It should be matched to the transmission line between it and the monitor with a series terminating resistor. The transmission line should be terminated at the monitor.

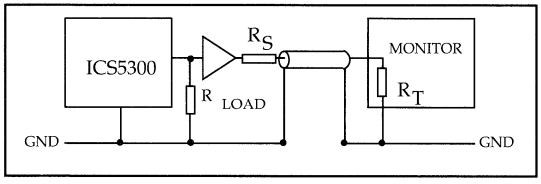


Figure 2 - Buffered Signal

SENSE Output

The GENDAC contains three comparators, one each for the DAC output (R, G and B) lines. The reference voltage to the comparators is proportional to the V_{REF} (internal or external) and is typically 0.33 for V_{REF} =1.23 Volts. When the voltage on any of these pins go higher than the reference voltage to the comparators, the SENSE* pin is driven low. This signal is used to detect the type of (or lack of) monitor connected to the system.

PLL Clock

The ICS5300 has dual PLL frequency generators for generating the video clock (CLK0) and memory clock (CLK1) needed for graphics subsystems. Both these clocks are generated from a single 14.318 MHz crystal or can be driven by an external clock source. The chip includes the capacitors for the crystal and all the components needed for the PLL loop filters, minimizing board component count.

There are eight possible video clock, CLK0, frequencies (f0-f7) which can be selected by the external pins CS0-CS2. Pins are software selectable by setting a bit in the PLL control register. Two of these frequencies (f0-f1) are fixed and the other six (f2-f7) can be programmed for any frequency by writing appropriate parameter values to the PLL parameter registers. The default frequencies on power up are commonly used video frequencies (table 1). At power up, the frequencies can be selected by pins CS0-CS2. There is only a single programmable memory clock frequency (CLK1). On power up this frequency defaults to the frequency given in table 2. The memory clock transition between frequencies is smooth and glitch free if the transition is kept between the limits 45-65 MHz.

fn	(MHz)	VLCK Comments
f0	25.175	VGA0 (VGA Color monitor) (fixed)
f1	28.322	VGA1 (VGA Monochrome monitor) (fixed)
f2	31.500	VESA 640 x 480 @72 Hz (programmable)
f3	36.00	VESA 800 x 600 @56 Hz (programmable)
f4	40.00	VESA 800 x 600 @60 Hz (programmable)
f5	44.889	1024 x 768 @43 Hz Interlaced (programmable)
f6	65.00	1024 x 768 @ 60 Hz, 640 x 480 Hi-Color @ 72 Hz (programmable)
f7	75.00	VESA 1024 x 768 @ 70 Hz, True Color 640 x 480 (programmable)

Table 1 - Video clock (CLK0) default frequency register (with a 14.318 MHz input)

fn	MHz	Comments
fA	45.00 MHz	Memory and GUI subsystem clock

Table 2 - Memory Clock (CLK1) default frequency register

Microprocessor Interface

Below are listed the six microprocessor interface registers within the ICS5300, and the register addresses through which they can be accessed.

RS2	RS1	RS0	Register Name
0	0	0	Pixel Address (write mode)
0	1	1	Pixel Address (read mode)
0	0	1	Color Value
0	1	0	Pixel Mask
1	0	0	PLL Address (write mode)
1	0	1	PLL Parameter
1	1	0	Command
1	1	1	PLL Address (read mode)
0/HF	1	0	Command Register accessed by (hidden) flag after special sequence of events

Table 3 - Microprocessor Interface Registers

Asynchronous Access to Microprocessor Interface
Accesses to all registers may occur without reference to the high speed timing of the pixel bit stream being processed by the GENDAC. Data transfers between the color palette RAM and the Color Value register, as well as modifications to the Pixel Mask register, are synchronized to the Pixel Clock by internal logic. This is done in the period between microprocessor interface accesses. Thus, various minimum periods are specified between microprocessor interface accesses to allow the appropriate transfers or modifications to take place. Access to PLL address, PLL parameter and to the command register are asynchronous to the pixel clock.

The contents of the palette RAM can be accessed via the Color Value register and the Pixel Address registers.

Writing to the color palette RAM
To set a new color definition, a value specifying a location in the color palette RAM is first written to the Write mode Pixel Address register. The values for the red, green and blue intensities are then written in succession to the Color Value register. After the blue data is written to the Color Value register, the new color definition is transferred to the RAM, and the Pixel Address register is automatically incremented.

Writing new color definitions to a set of consecutive locations in the RAM is made easy by this auto-incrementing feature. First, the start address of the set of locations is written to the write mode Pixel Address register, followed by the color definition of that location. Since the address is incremented after each color definition is written, the color definition for the next location can be written immediately. Thus, the color definitions for consecutive locations can be written sequentially to the Color Value register without re-writing to the Pixel Address register each time.

Reading from the RAM
To read a color definition, a value specifying the location in the palette RAM to be read is written to the read mode Pixel Address register. After this value has been written, the contents of the location specified are copied to the Color Value register, and the Pixel Address register automatically increments.

The red, green and blue intensity values can be read by a sequence of three reads from the Color Value register. After the blue value has been read, the location in the RAM currently specified by the Pixel Address register is copied to the Color Value register and the Pixel Address again automatically increments. A set of color values in consecutive locations can be read simply by writing the start address of the set to the read mode Pixel Address register and then sequentially reading the color values for each location in the set. Whenever the Pixel Address register is updated, any unfinished color definition read or write is aborted and a new one may begin.

The Pixel Mask Register
The pixel address used to access the RAM through the pixel interface is the result of the bitwise ANDing of the

incoming pixel address and of the contents of the Pixel Mask register. This pixel masking process can be used to alter the displayed colors without altering the video memory or the RAM contents. By partitioning the color definitions by one or more bits in the pixel address, such effects as rapid animation, overlays, and flashing objects can be produced.

The Pixel Mask register is independent of the Pixel Address and Color Value registers.

The Command Register
The Command register is used to select the various GENDAC color modes and to set the power down mode. On power up this register defaults to an 6-bit Pseudo Color mode. This register can be accessed by control pins RS2-RS0, or by a special sequence of events for graphics subsystems that do not have the control signal RS2. For graphic systems that do not have RS2, this pin is tied low and an internal flag (HF; Hidden Flag) is set when the pixel mask register is read four times consecutively. Once the flag is set, the following Read or Write to the pixel mask register is directed to the command register. The flag is reset for Read or Write to any register other than the pixel mask register. The sequence has to be repeated for any subsequent access to the command register.

The PLL Parameter Register
The CLK0 and CLK1 of the ICS5300 can be programmed for different frequencies by writing different values to the PLL parameter register bank. There are eight registers in the parameter register; seven are two bytes long and one (0E) is one byte long.

Writing to the PLL parameter register
To write the PLL parameter data, the corresponding address location is first written to the PLL address register. For software compatibility with other chips, two address registers are defined; the Write mode PLL address register and the Read mode PLL address register. They are actually a single Read/Write register in the ICS5300. The next PLL parameter write will be directed to the first byte of the address location specified by the PLL address register. The next Write to the parameter register will automatically be to the second byte of this register. At the end of the second Write the address is automatically incremented. For the one byte "0E" register the address location is incremented after the first byte Write. If this frequency is selected while programming, the output frequency will change at the end of the second Write.

Reading the PLL parameter register
To read one of the registers of the PLL parameter register the address value corresponding to the location is first written to the PLL address register. The next PLL parameter read will be directed to the first byte of the address location pointed by this index register. A next Read of the parameter register will automatically be the second byte of this register. At the end of the second Read, the address location is automatically incremented. The address register (0E) is incremented after the first byte Read.

C

Power Down Mode

When bit 0 in the Command register is high (set to 1) , the GENDAC enters the DAC power down mode. The DACs are turned off, and the data is retained in the RAM. It is possible to access the RAM, in which case the current will temporarily increase. While the RAM is being accessed, the current consumption will be proportional to the speed of the clock. There is no effect on either clock generator while in this mode.

Power Supply

As a high speed CMOS device, the ICS5300 may draw large transient currents from the power supply, it is necessary to adopt high frequency board layout and power distribution techniques to ensure proper operation of the GENDAC. Please refer to the suggested layout on page 29.

To supply the transient currents required by the ICS5300, the impedance in the decoupling path should be kept to a minimum between the power supply pins V_{DD} and GND. It is recommended that the decoupling capacitance between V_{DD} and GND should be a 0.1µF high frequency capacitor, in parallel with a large tantalum capacitor with

a value between 22µF and 47µF. A ferrite bead may be added in series with the positive supply to form a low pass filter and further improve the power supply local to the GENDAC. It will also reduce EMI.

The combination of series impedance in the ground supply to the GENDAC, and transients in the current drawn by the device will appear as differences in the GND voltages to the GENDAC and to the digital devices driving it. To minimize this differential ground noise, the impedance in the ground supply between the GENDAC and the digital devices driving it should be minimized.

Digital Output Information

The PCB trace lines between the outputs of the TTL devices driving the GENDAC and the input to the GENDAC behave like low impedance transmission lines driven from a low impedance transmission source and terminated with a high impedance. In accordance with transmission line principles, signal transitions will be reflected from the high impedance input to the device. Similarly, signal transitions will be inverted and reflected from the low impedance TTL output. Line termination is recommended to reduce or eliminate the ringing, particularly the undershoot caused by reflections. The termination may either be series or parallel.

Series termination is the recommended technique to use. It has the advantages of drawing no DC current and of using fewer components. Series termination is accomplished by placing a resistor in series with the signal at the output of the TTL driver. This matches the TTL output impedance to that of the transmission line and ensures that any signal incident on the TTL output is not reflected.

To minimize reflections, some experimentation will have to be done to find the proper value to use for the series termination. Generally, a value around 100Ω will be required. Since each design will result in a different signal impedance, a resistor of a predetermined value may not properly match the signal path impedance. Therefore, the proper value of resistance should be found empirically.

Functional Description

This section describes the register address and bit definition for RAMDAC and the Frequency Synthesizer sections.

Color Palette

Command Register

(RS0-RS2 = 011)
(RS0-RS1 = 01 with hidden flag)

By setting bits in the command register the ICS5300 can be programmed for different color modes and can be powered down for low power operation.

7 6 5	4 3 2 1	0
Color Mode 2 1 0	Reserved Should all =0	Snooze

Table 3 - Command Registers

Bit 7-5 **Color Mode Select**
These three bits select the Color Mode of RAMDAC operation as shown in the following table 4 (default is 0 at power up):

Bit 4 - 1 **(Reserved)**

Bit 0 **Power Down Mode of RAMDAC**
When this bit is set to 0 (default is 0), the device operates normally. If this bit is set to 1, the power and clock to the Color Palette RAM and DACs are turned off. The data in the Color Palette RAM are still preserved. The CPU can access without loss of data by internal automatic clock start/stop control. The DAC outputs become the same as BLANK* (sync) level output during power down mode. This bit does not effect the PLL clock synthesizer function.

Color Modes

The four selectable color modes are described here.

Mode 0: 8-bit Pseudo Color (one clock per pixel). This mode is the 8-bit per pixel Pseudo Color mode. In this mode. inputs P0-P7 are the pixel address for the color palette RAM and are latched on the rising edge of every PCLK. This is the default mode on power up and it is selected by setting bits CR7-CR5 to 000 . There are three clock cycles pipe line delays from input to DAC output.

8-bit Pseudo Color mode

DATA BYTE							
7	6	5	4	3	2	1	0
PIXEL ACCESS							
7	6	5	4	3	2	1	0

CM2 (CR7)	CM1 (CR6)	CM0 (CR5)	Color Mode	Clock Cycles/ Pixel Bits
0	0	0	6-Bit Pseudo Color with Palette (Default)	1
0	0	1	15-Bit Direct Color with Bypass (Hi-Color)	2
0	1	0	24-Bit True Color with Bypass (True Color)	3
0	1	1	16-Bit Direct Color with Bypass (XGA)	2
1	0	0	15-Bit Direct Color with Bypass (Hi-Color)	2
1	0	1	15-Bit Direct Color with Bypass (Hi-Color)	2
1	1	0	16-Bit Direct Color with Bypass (XGA)	2
1	1	1	24-Bit True Color with Bypass (True Color)	3

Table 4 - Color Mode Select

Mode 1: (15-bit per color bypassHi-Color mode).
This mode is the 15-bit per pixel bypass mode. In this mode, inputs P0-P7 are the color DATA and are input directly to the DAC, bypassing the color palette. The two bytes of data is latched in two successive PCLK rising edges. ICS5300 supports only the two clock mode and does not support the mode where the data are latched on the rising and the falling edges. For compatibility, the 15/16 one clock modes are selected as two clock modes in this chip. The low-byte, high byte synchronization is internally done by the rising edge of BLANK*. Each color is 5-bit wide and is packed into two bytes as shown below. The mode is selected by setting bits CR7-CR5 to 001, 100 or 101.

15-Bit Color Mode

3LSB = set to zero

SECOND BYTE								FIRST BYTE							
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
X	7	6	5	4	3	7	6	5	4	3	7	6	5	4	3
	RED				GREEN						BLUE				

Mode 2: (16-bit per pixel bypass XGA mode).
This mode is the 16-bit per pixel bypass mode and the P0-P7 inputs to go to the DAC directly, bypassing the color palette. The 2 bytes data is latched on two successive rising edges and the low-byte, high-byte synchronization is internally done by the rising edge of BLANK*. In this mode, blue and red colors are 6 bits wide and green is 5 bits wide. The 2 bytes of data is packed as shown below. The mode is selected by setting bits CR7-CR5 to 011 or 110.

16-Bit color mode

2LSB = set to zero (green)
3LSB = set to zero (blue, red)

SECOND BYTE								FIRST BYTE							
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
7	6	5	4	3	7	6	5	4	3	2	7	6	5	4	3
RED					GREEN						BLUE				

Mode 3: (24-bit per pixel True Color Mode).
This mode is the 24-bit per pixel bypass mode. The three bytes of data are latched on three successive PCLK edges and the first byte is synchronized by the rising edge of BLANK*. In this mode, each of the colors are 8-bit wide and the DAC is an 8-bit wide DAC. The first byte is blue followed by green and red. This mode can be selected by setting bits CR7-CR5 to 010 or 111. The DAC outputs changes every three cycles and the pipeline delay from the first byte to output is five cycles.

24-bit color mode

THIRD BYTE								SECOND BYTE								FIRST BYTE							
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
RED								GREEN								BLUE							

Frequency Generators

The ICS5300 clock synthesizer can be reprogrammed through the microprocessor interface for any set of frequencies. This is done by writing appropriate values to the PLL Parameter Register Bank (table 5).

PLL Address Registers

The address of the parameter register is written to the PLL address registers before accessing the parameter register. This register is accessed by register select pins RS2-RS0 = 100 or 111.

7	6	5	4	3	2	1	0
PLL REGISTER ADDRESS							
7	6	5	4	3	2	1	0

PLL Parameter Register

There are sixteen registers in the PLL parameter register (table 5). Registers 00 to 07 are for the CLK0 selectable frequency list, Register 0A for CLK1 programmable frequency and register 0E is the PLL CLK0 control register.

Index	R/W	Register	
00	R/-	CLK0 f0 PLL Parameters	(2 bytes)
01	R/-	CLK0 f1 PLL Parameters	(2 bytes)
02	R/W	CLK0 f2 PLL Parameters	(2 bytes)
03	R/W	CLK0 f3 PLL Parameters	(2 bytes)
04	R/W	CLK0 f4 PLL Parameters	(2 bytes)
05	R/W	CLK0 f5 PLL Parameters	(2 bytes)
06	R/W	CLK0 f6 PLL Parameters	(2 bytes)
07	R/W	CLK0 f7 PLL Parameters	(2 bytes)
08	R/-	(Reserved) = 0	(2 bytes)
09	R/-	(Reserved) = 0	(2 bytes)
0A	R/W	CLK1fA PLL	(2 bytes)
0B	R/-	(Reserved) = 0	(2 bytes)
0C	R/-	(Reserved) = 0	(2 bytes)
0D	R/-	(Reserved) = 0	(2 bytes)
0E	R/W	PLL Control Register	(1-byte)
0F	R/-	(Reserved) = 0	(2-byte)

Table 5 - PLL Parameter Registers

PLL Control Register

Bits in this register determine internal or external CLK0 select.

7	6	5	4	3	2	1	0
(RV)	(RV)	ENBL	(RV)	(RV)	INTERNAL SELECT		
=0	=0	INCS	=0	=0	X	X	X

Bit 7 - 6 Reserved.

Bit 5 Enable Internal Clock Select (INCS) for CLK0. When this bit is set to 1, the CLK0 output frequency is selected by bit 2 - 0 in this register. External pins CS0 - CS2 are ignored.

Bit 4 - 3 (Reserved).

Bit 2 - 0 Internal Clock Select for CLK0 (INCS). These three bits selects the CLK0 output frequency if bit 5 of this register is on. They are interpreted as an octal number, n, that selects fn. Default selects f0.

PLL Data Registers

The CLK0 and CLK1 input frequency is determined by the parameter values in this register. These are two bytes registers; the first byte is the M-byte and the second is the N-byte.

M-Byte PLL Parameter Input
The M-byte has a 7-bit value (1-127) which is the feedback divider of the PLL.

7	6	5	4	3	2	1	0
Reserved	M-Divider Value						
=0	X	X	X	X	X	X	X

N-Byte PLL Parameter Input
The N-byte has two values. N1 sets a 5-bit value (1-31) for the input pre scalar and N2 is a 2-bit code for selecting 1, 2, 4, or 8 post divide clock output.

7	6	5	4	3	2	1	0
Reserved	N2-Code		N1-Divider Value				
=0	X	X	X	X	X	X	X

N2 Post Divide Code

N2 code	Divider
00	1
01	2
10	4
11	8

The block diagram of the PLL clock synthesizer is given in following figure 3.

Based on the M and N values, the output frequency of the clocks is given by the following equation:

$$F_{out} = \frac{(M+2) \times F_{ref}}{(N1+2) \times 2^{N2}}$$

M and N values should be programmed such that the frequency of the VC0 is within the optimum range for duty cycle, jitter and glitch free transition. Optimum duty cycle is achieved by programming N2 for values greater than one. See the following page for programming example.

Programming Example

Suppose an output frequency of 25.175 MHz is desired. The reference crystal is 14.318 MHz. The VCO should be targeted to run in the 100 to 180 MHz range, so choosing a post divide of 4 gives a VCO frequency of :

4 X 25.175=101.021 MHz

From the table on page 17, we find N2 = 2
Substituting F_{ref} = 14.318 and 2^{N2} = 4 into the equation on page 17:

$$\left(\frac{25.175}{14.318}\right) \cdot 4 = \frac{(M+2)}{(N1+2)}$$

by trial and error:

$$\left(\frac{25.175}{14.318}\right) \cdot 4 \approx \frac{127}{18}$$

so M + 2 = 127 M = 125
N1 + 2 = 18 N1 = 16

so the registers are:

M = 125d = 1 1 1 1 1 0 1 b
N = 0 & N2 code & N1 = 0 & 1 0 & 1 0 0 0 0
N = 0 1 0 1 0 0 0 0 b

Additional Information on Programming the Frequency Generator section of the GENDAC

When programming the GENDAC PLL parameter registers, there are many possible combinations of parameters which will give the correct output frequency. Some combinations are better than others, however. Here is a method to determine how the registers need to be set:

The key guidelines come from the operation of the phase locked loop, which has the following restrictions:

1. 2 MHz < f_{REF} < 32 MHz
   This refers to the input reference frequency. Most users simply connect a 14.318 MHz crystal to the crystal inputs, so this is not a problem.

2. $$600 \text{ kHz} < \frac{f_{REF}}{(N1+2)} \leq 8 \text{ MHz}$$
   This is the frequency input to the phase detector.

3. $$60 \text{ MHz} \leq \frac{(M+2)}{(N1+2)} f_{REF} \leq 270 \text{ MHz}$$

   This is the VCO frequency. In general, the VCO should run as fast as possible, because it has lower jitter at higher frequencies. Also, running the VCO at multiples of the desired frequency allows the use of output divides, which tends to improve the duty cycle.

4. f_{CLK0} and $f_{CLK1} \leq 135$ MHz
   This is the output frequency.

These rules lead to the following procedure for determining the PLL parameters, assuming rules 1 and 4 are satisfied.

A. Determine the value of N2 (either 1, 2, 4 or 8) by selecting the highest value of N2, which satisfies the condition
   $N2 * f_{CLK} \leq 270$ MHz

B. Calculate $$\frac{(M2+)}{(N1+2)} = \frac{2^{N2} f_{out}}{fref}$$

C. Now (M+2) and (N1+2) must be found by trial and error. With a 14.318 MHz reference frequency, there will generally be a small output frequency error due to the resolution limit of (M+2) and (N1+2). For a given frequency tolerance, several different (M+2) and (N1+2) combinations can usually be found. Usually, a few minutes trying out numbers with a calculator will produce a workable combination. Multiplying possible values of (N1+2) by the desiredratio will indicate approximately the value of M. This method is shown in the example below. A program could be written to try all possible combinations of (M+2) and (N1+2) (3937 possible combinations), discard those outside error band, and select from those remaining by giving preference to ratios which use lower values of (M+2). Lower values of (M+2) and (N1+2) provide better noise rejection in the phase locked loop.

Example: Suppose we are using a 14.318 MHz reference crystal and wish to output a frequency of 66 MHz with an error of no greater than 0.5%. What are the values of the PLL data registers?

A. 66*8 = 528 > 250 VCO speed too high
66*4 = 264 > 250 VCO speed too high
66*2 = 132 < 250 VCO speed OK, N2 = 2, N2 code = 01 from table on page 17 of the data sheet.

B. 132/14.31818 = 9.219
This is the desired frequency multiplication ratio.

C. Setting (N1+2) = 3, 4,...12, 13 and performing some simple calculations yields the following table: (Note that N1 cannot be 0)

(N1+2)	(N1+2)*9.219	rounded (=M+2)	Actual Ratio	Percent Error
3	27.657	28	9.33	-1.23
4	36.876	37	9.25	-0.34
5	46.095	46	9.20	0.21
6	55.314	55	9.17	0.57
7	64.533	65	9.29	-0.72
8	73.752	74	9.25	-0.34
9	82.971	83	9.22	-0.03
10	92.19	92	9.20	0.21
11	101.409	101	9.18	0.40
12	110.628	111	9.25	-0.34
13	119.847	120	9.23	-0.13

The ratio 83/9 is closest. Thus (N2+2) = 9; N2=7. (M+2) = 83; M = 81. The M-byte PLL parameter word is simply 81 in binary, plus bit 7 (which must be set to 0), or 01010001. The N-byte PLL parameter word is N2 code (01) concatenated with 5 bits of N2 in binary (00111), or 00100111. Once again, bit 7 must be zero.

We have chosen the combination with the least frequency error, but several other combinations are within the 0.5% tolerance. Because the lowest value of (M+2) offers the best damping, the 37/4 combination will have the best power supply rejection. This results in lower jitter due to external noise.

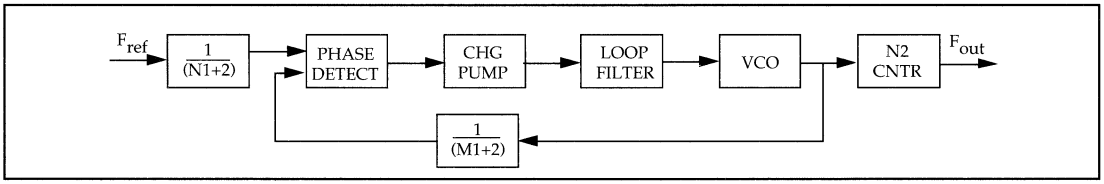
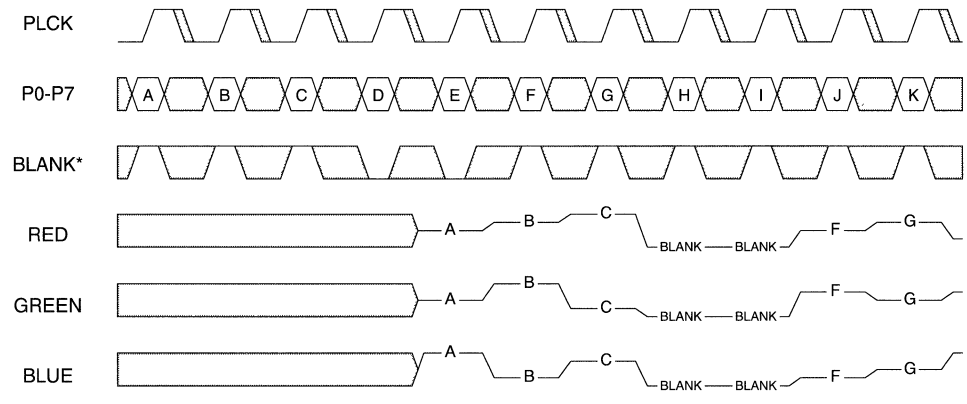


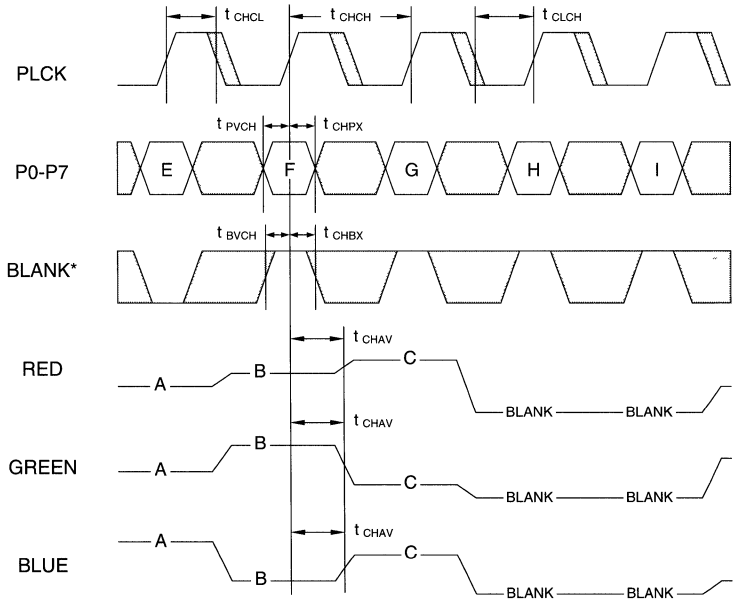
Figure 3 - PLL Clock Synthesizer Block Diagram

External Select			(Internal Select PLL Control Register)			
CS2	CS1	CS0	BIT 2	BIT 1	BIT 0	CLK 0 Frequency
0	0	0	0	0	0	f0
0	0	1	0	0	1	f1
0	1	0	0	1	0	f2
0	1	1	0	1	1	f3
1	0	0	1	0	0	f4
1	0	1	1	0	1	f5
1	1	0	1	1	0	f6
1	1	1	1	1	1	f7

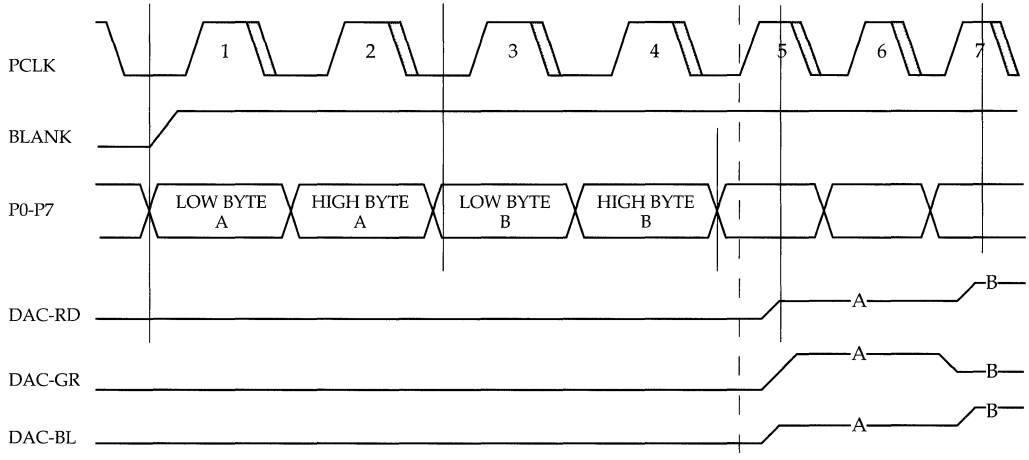
Video Clock Selection Table



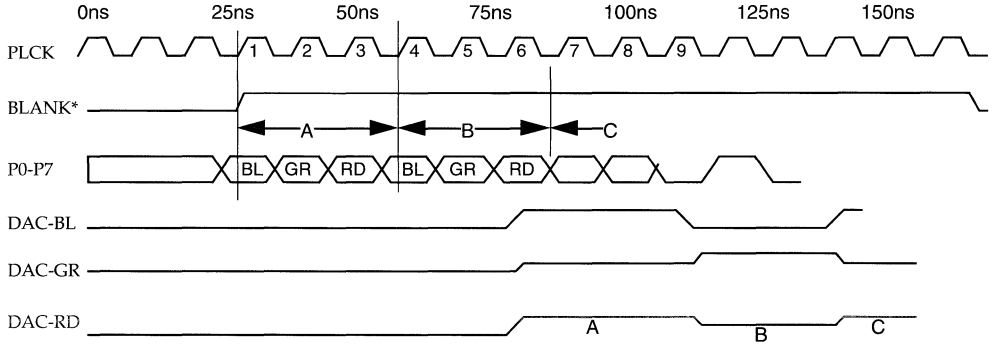
System Timing - Pseudo Color, Mode 0



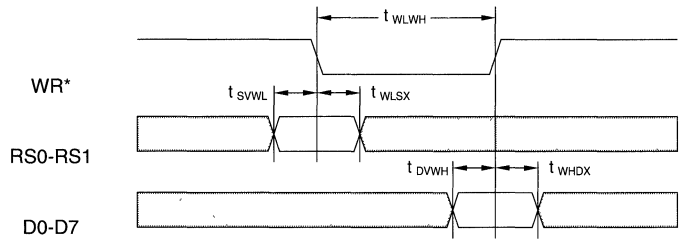
Detailed Timing Specifications - Pseudo Color, Mode 0



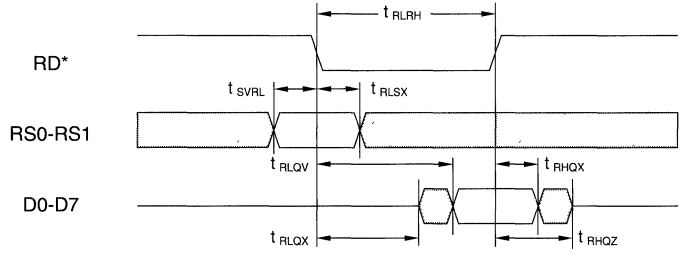
System Timing Bypass - 15 (5/5/5) and 16 (5/6/5) Modes 1, 2



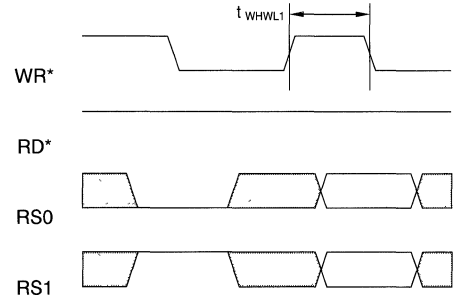
System Timing Bypass True Color 24 (8,8,8) Mode 3



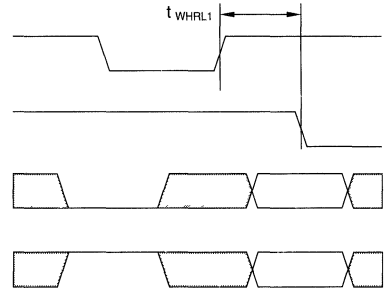
Basic Write Cycle Timing



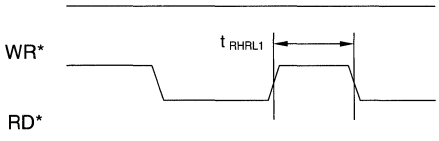
Basic Read Cycle Timing



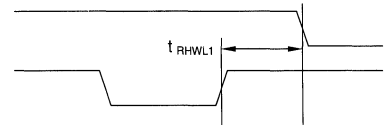
Write to Pixel Mask Register Followed by Write



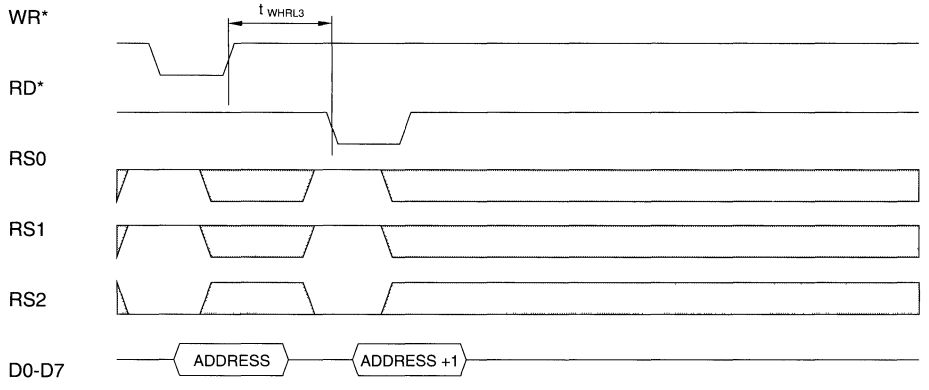
Write to Pixel Mask Register Followed by Read



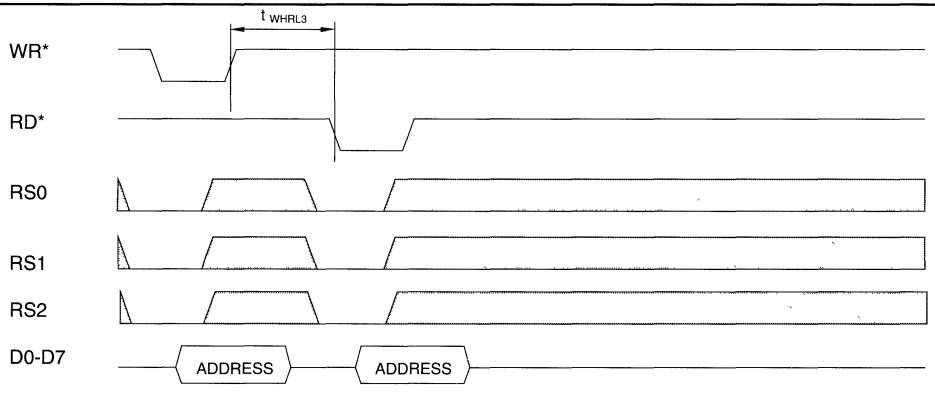
Read from Pixel or Pixel Address Register (Read or Write) followed by Read



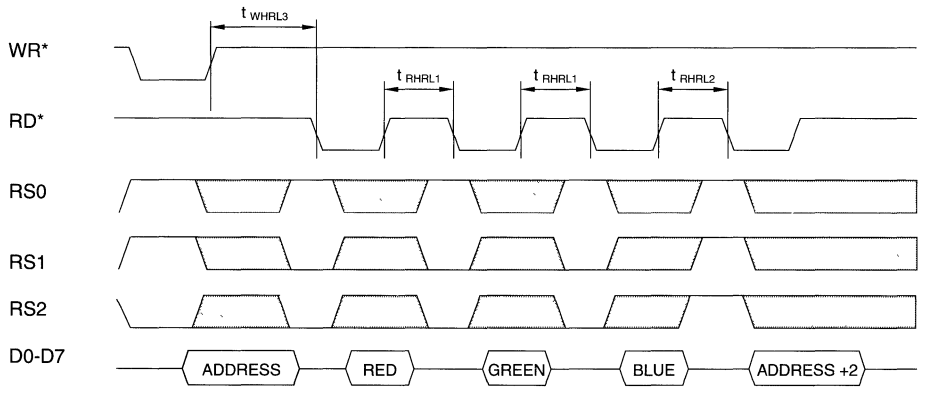
Read from Pixel or Pixel Address Register (Read or Write) followed by Write



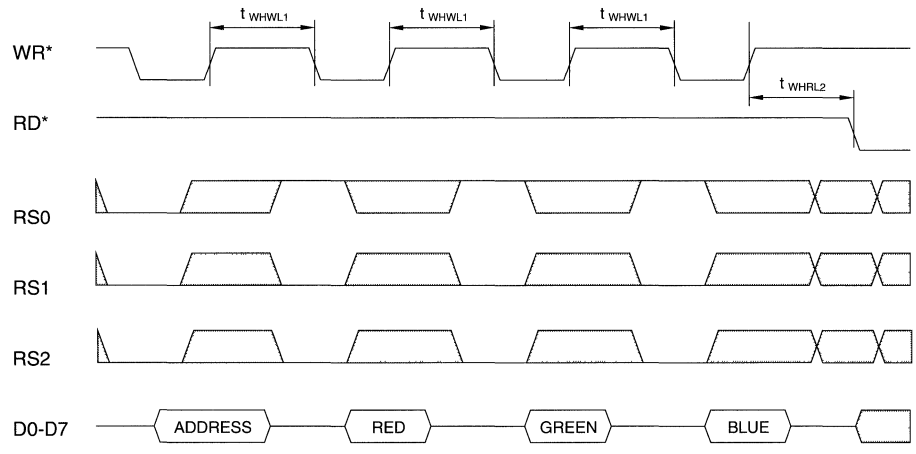
Write and Read Back Pixel Address Register (Read Mode)



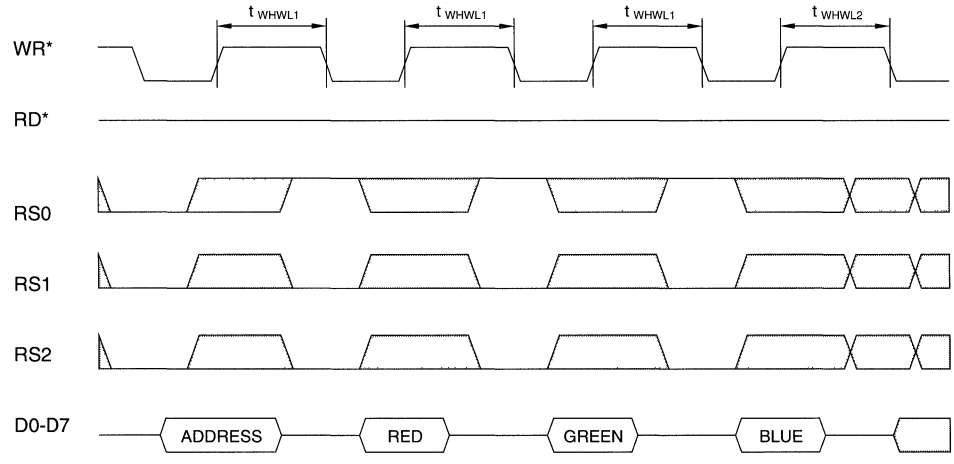
Write and Read Back Pixel Address Register (Write Mode)



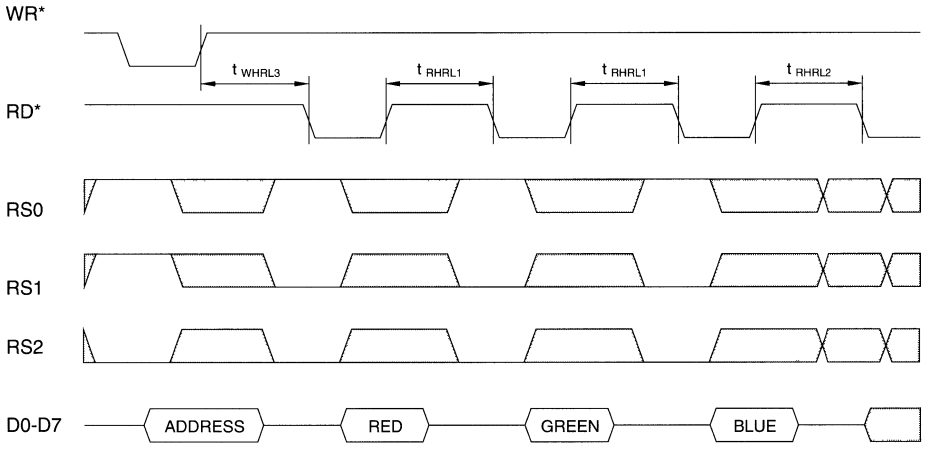
Read Color Value then Pixel Address Register (Read Mode)



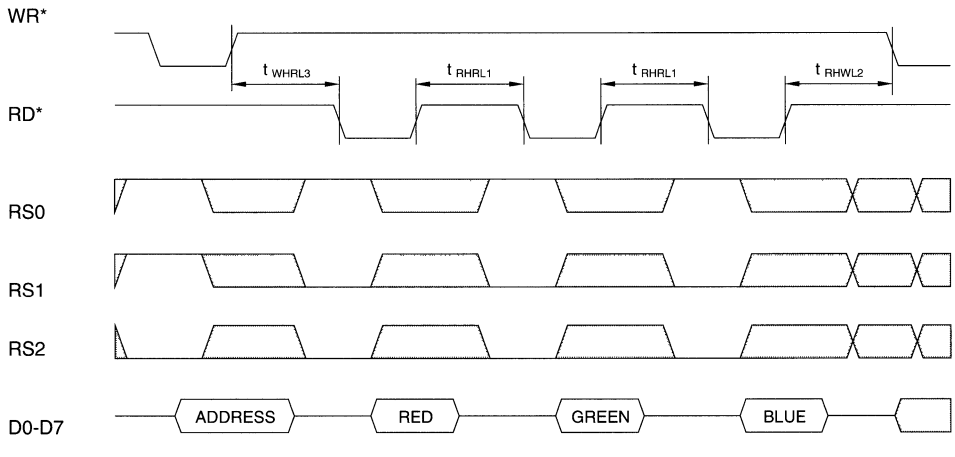
Color Value Write followed by any Read



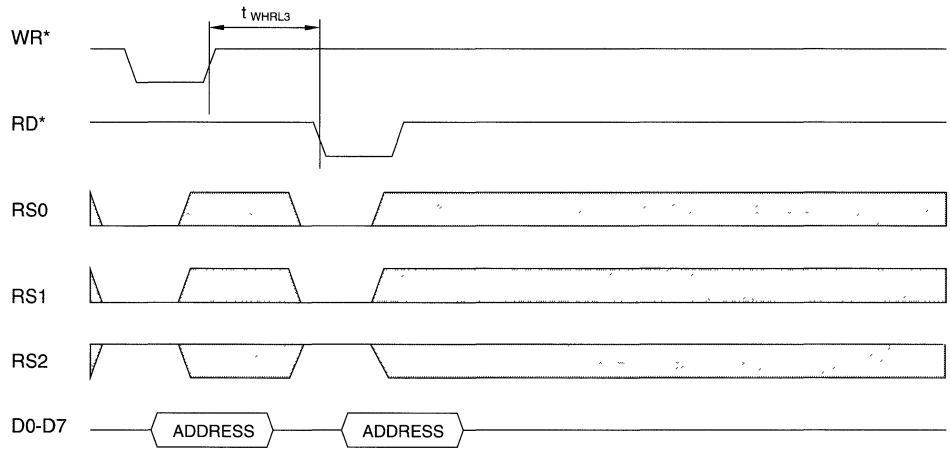
Color Value Write followed by any Write



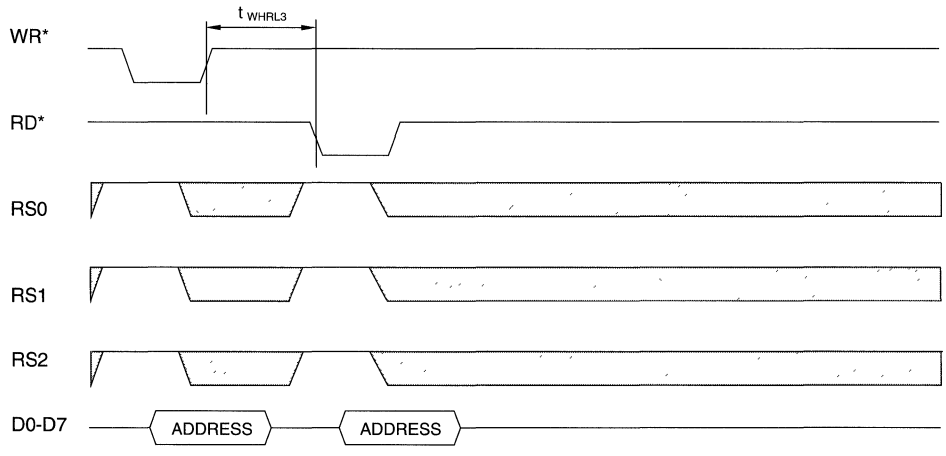
Color Value Read followed by any Read



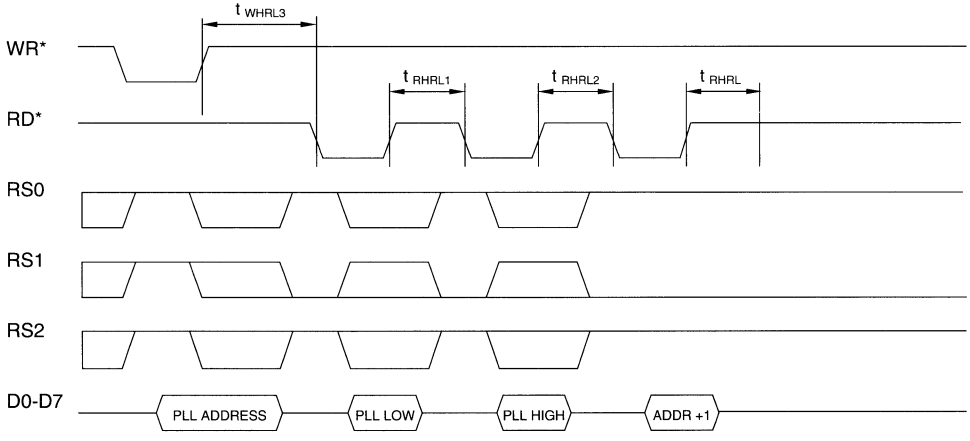
Color Value Read followed by any Write



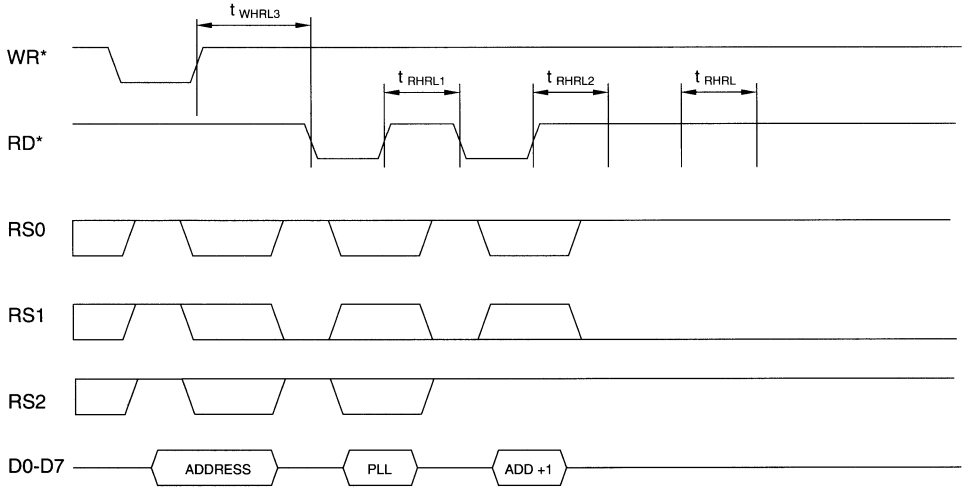
Write and Read back PLL Address Register (Write Mode)



Write and Read back PLL Address Register (Read Mode)

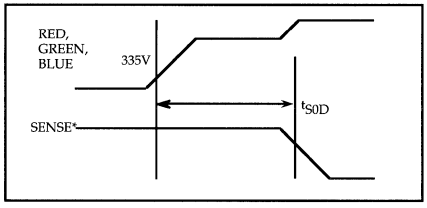


Read Two bytes PLL Register then PLL Address Register



Read One Byte PLL Register then PLL Address Register

Monitor SENSE Signal

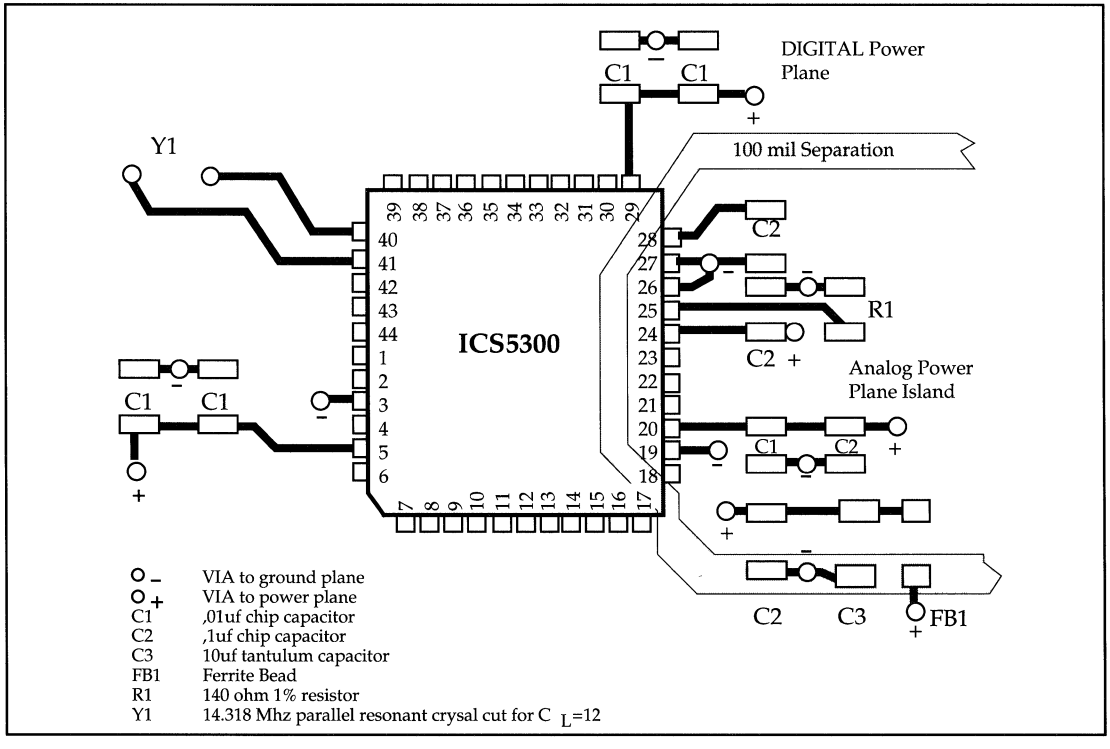


The high performance of which the ICS5300 GENDAC is capable is dependent on careful PC board layout. The use of a four layer board (internal power and ground planes, signals on the two surface layers) is recommended. The layout below shows a suggested configuration.

The ground plane is continuous, but the power plane is separated into analog and digital sections as shown. Power is supplied to the analog power plane through the ferrite bead, and bypassed at the power entry point by C3, a 10 µF tantalum capacitor. These high current connections should have multiple vias to the ground and power planes, if possible. Power connections should be connected to the analog or digital power plane, as shown in the diagram. Power pins 5 and 29 should be connected to digital power, power pins 20 and 24 to analog power. Decoupling capacitors (indicated by C1) should be placed as close to the GENDAC as possible.

The analog and digital I/O lines are not shown. Analog signals (DAC outputs, Vref, Rset) should only be routed above the analog power plane. Digital signals should only be routed above the digital power plane.

Recommended Layout



O –	VIA to ground plane
O +	VIA to power plane
C1	,01uf chip capacitor
C2	,1uf chip capacitor
C3	10uf tantulum capacitor
FB1	Ferrite Bead
R1	140 ohm 1% resistor
Y1	14.318 Mhz parallel resonant crysal cut for C_L=12

Integrated Circuit Systems, Inc.

ICS5301 GENDAC

8-Bit Integrated Clock-LUT-DAC

General Description

The ICS5301 GENDAC is a combination of dual programmable clock generators, a 256 x 18-bit RAM, and a triple 8-bit video DAC. The GENDAC supports 8-bit pseudo color applications, as well as 15-bit, 16-bit and 24-bit True Color bypass for high speed, direct access to the DACs.

The RAM makes it possible to display 256 colors selected from a possible 262,144 colors. The dual clock generators use Phase Locked Loop (PLL) technology to provide programmable frequencies for use in the graphics subsystem. The video clock contains 8 frequencies, 6 of which are programmable by the user. The memory clock has one programmable frequency location.

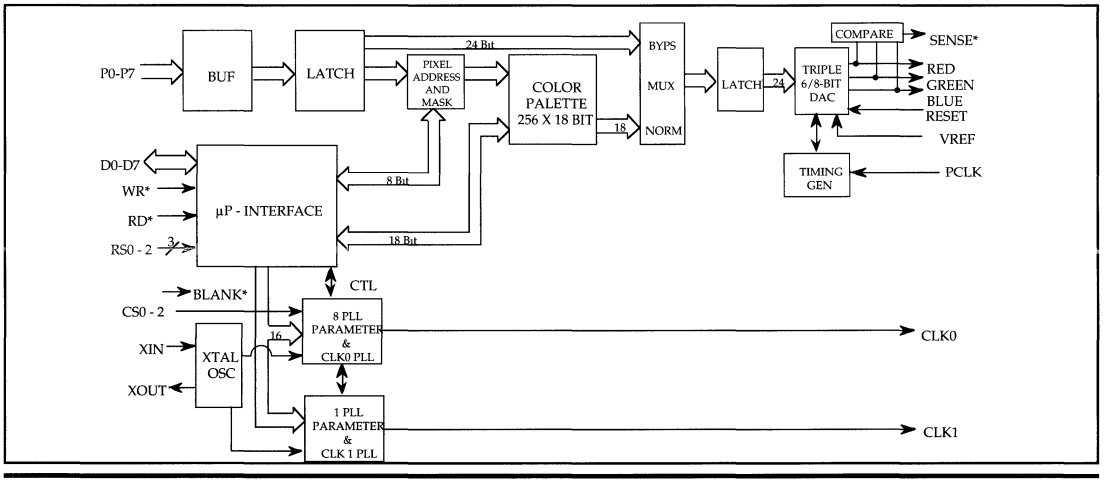
The three 8-bit DACs on the ICS5301 are capable of driving singly or doubly-terminated 75Ω loads to nominal 0 - 0.7 volts at pixel rates up to 135 MHz. Differential and integral linearity errors are less than 1 LSB over full temperature and V_{DD} ranges. Monotonicity is guaranteed by design. On-chip pixel mask register allows displayed colors to be changed in a single write cycle rather than by modifying the color palette.

ICS is the world leader in all aspects of frequency (clock) generation for graphics, using patented techniques to produce low jitter video timing.

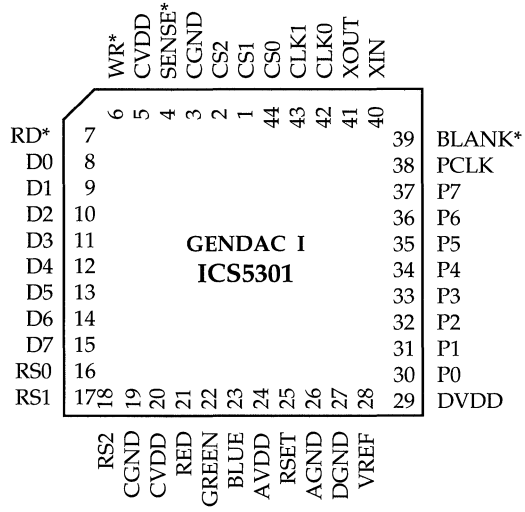
Features

- **Designed for compatibility with Tseng Labs VGA controllers**
- **Triple video DAC, dual clock generator, and a color palette**
- **24, 16, 15, or 8-bit pseudo color pixel mode supports True Color, Hi-Color, and VGA modes**
- **High speed 256 x 18 color palette (135 MHz) with bypass mode and 8-bit DACs**
- **Two fixed, six programmable video (pixel) clock frequencies (CLK0)**
- **One programmable memory (controller) clock frequency (CLK1)**
- **DAC power down in blanking mode**
- **Low power operation**
- **Anti-sparkle circuitry**
- **On-chip loop filters reduce external components**
- **Standard CPU interface**
- **Single external crystal (typically 14.318 MHz)**
- **Monitor Sense**
- **Internal voltage reference**
- **135 MHz (-3), 110 MHz (-2) & 80 MHz (-1) versions**
- **Very low clock jitter**

Block Diagram



Pin Configuration



Pin Description (68 pin PLCC)

Symbol	Pin #	Type	Description
CS1	1	Input	Clock select 1. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output.
CS2	2	Input	Clock select 2. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output.
CGND	3	-	Ground for clock circuits. Connect to ground.
SENSE*	4	Output	Monitor Sense, active low. This pin is low when any of the red, green, or blue outputs have exceeded 335mV. The chip has on-board comparators and an internal 335mV voltage reference. This is used to detect monitor type.
CVDD	5	-	Clock Power Supply. Connect to DVDD
WR*	6	Input	RAM/PLL Write Enable, active low. This signal controls the timing of the write operation on the microprocessor interface inputs, D0-D7.
RD*	7	Input	RAM/PLL Read Enable, active low. This is the READ bus control signal. When active, any information present on the internal data bus is available on the Data I/O lines, D0-D7.
D0 - D7	8 - 15	I/O	System data bus I/O. These bidirectional Data I/O lines are used by the host microprocessor to write (using active low WR*) information into, and read (using active low RD*) information from the six internal registers (Pixel Address, Color Value, Pixel Mask, PLL Address, PLL Parameter, and Command). During the write cycle, the rising edge of WR* latches the data into the selected register (set by the status of the three RS pins). The rising edge of RD* determines the end of the read cycle. When RD* is a logical high, the Data I/O lines no longer contain information from the selected register and will go into a tri-state mode.

Pin Description (continued)

Symbol	Pin #	Type	Description
RS0 RS1 RS2	16 17 18	Input Input Input	Register Address Select 0. These inputs control the selection of one of the six internal registers. They are sampled on the falling edge of the active enable signal (RD* or WR*).
CGND	19	-	Ground for clock circuits. Connect to ground.
CVDD	20	-	Clock Power Supply. Connect to AVDD.
RED GREEN BLUE	21 22 23	Output Output Output	Color Signals. These three signals are the DACs' analog outputs. Each DAC is composed of several current sources. The outputs of each of the sources are added together according to the applied binary value. These outputs are typically used to drive a CRT monitor.
AVDD	24	-	Analog power supply. Connect to AVDD.
RSET	25	Input	Resistor Set. This pin is used to set the current level in the analog outputs. It is usually connected through a 140Ω, 1% resistor to ground.
AGND	26	-	Analog Ground. Connect to ground.
DGND	27	-	Digital Ground. Connect to ground.
VREF DVDD	28 29	Input -	Internal Reference Voltage. Normally connects to a 0.1µF cap to ground. To use an external Vref, connect a 1.235V reference to this pin. Digital power supply.
P0 - P7	30 - 37	Input	Pixel Address Lines. This byte-wide information is latched by the rising edge of PCLK when using the Color Palette, and is masked by the Pixel Mask register. These values are used to specify the RAM word address in the default mode (accessing RAM). In the Hi-Color XGA, and True Color modes, they represent color data for the DACs. These inputs should be grounded if they are not used.
PCLK	38	Input	Pixel Clock. The rising edge of PCLK controls the latching of the Pixel Address and BLANK* inputs. This clock also controls the progress of these values through the three-stage pipeline of the Color Palette RAM, DAC, and outputs.
BLANK*	39	Input	Composite BLANK* Signal, active low. When BLANK* is asserted, the outputs of the DACs are zero and the screen becomes black. The DACs are automatically powered down to save current during blanking. The color palette may still be updated through D0-D7 during blanking.
XIN	40	Input	Crystal input. A 14.318 MHz crystal should be connected to this pin.
XOUT	41	Output	Crystal output. A 14.318 MHz crystal should be connected to this pin.
CLK0	42	Output	Video clock output. Provides a CMOS level pixel or dot clock frequency to the graphics controller. The output frequency is determined by the values of the PLL registers.
CLK1	43	Output	Memory clock output. Used to time the video memory.
CS0	44	Input	Clock select 0. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output.

Internal Registers

RS2	RS1	RS0	Register Name	Description (all registers can be written to and read from)
				There is a single Pixel Address register within the GENDAC. This register can be accessed through either register address 0,0,0 or register address 0,1,1. A read from address 0,0,0 is identical to a read from address 0,1,1. Writing a value to address 0,0,0 performs the following operations: a) Specifies an address within the color palette RAM. b) Initializes the Color Value register. Writing a value to address 0,1,1 performs the following operations: a) Specifies an address within the color palette RAM. b) Loads the Color Value register with the contents of the location in the addressed RAM palette and then increments the Pixel Address register.
0	0	0	Pixel Address WRITE	Writing to this 8-bit register is performed prior to writing one or more color values to the color palette RAM.
0	1	1	Pixel Address READ	Writing to this 8-bit register is performed prior to reading one or more color values from the color palette RAM.
0	0	1	Color Value	The 18-bit Color Value register acts as a buffer between the microprocessor interface and the color palette. Using a three bytes transfer sequence allows a value to be read from or written to this register. When a byte is read, the color value is contained in the least significant 6 bits, D0-D5 (the most significant 2 bits are set to zero). When writing a byte, the same 6 bits are used. When reading or writing, data is transferred in the same order - the red byte first, then green, then blue. Each transfer between the Color Value register and the color palette replaces the normal pixel mapping operations of the GENDAC for a single pixel. After writing three definitions to this register, its contents are written to the location in the color palette RAM specified by the Pixel Address register, and the Pixel Address register increments. After reading three definitions from this register, the contents of the location in the color palette RAM specified by the Pixel Address registers are copied into the Color Value register, and the Pixel Address register increments.
0	1	0	Pixel Mask	The 8-bit Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs (P0-P7). A one in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered, while a zero sets that bit to zero. The Pixel Mask register does not affect the Pixel Address generated by the microprocessor interface when the palette RAM is being accessed.

Internal Registers (continued)

RS2	RS1	RS0	Register Name	Description (all registers can be written to and read from)
1	0	0	PLL Address WRITE	Writing to this 8-bit register is performed prior to writing one or more PLL programming values to the PLL Parameter register.
1	1	1	PLL Address READ	Writing to this 8-bit register is performed prior to reading one or more PLL programming values from the PLL Parameter register.
1	1	0	Command	This 8-bit register selects the color mode, for instance 8-bit Pseudo Color, Hi-Color, True Color, or XGA, and DAC power down. The registers are reset to pseudo color mode on power up.
1	0	1	PLL Parameter	There are sixteen parameter registers as indexed by PLL Address Write/ Readregisters. Parameter registers 00-0D and 0F are two bytes long and 0E is one byte long. This register set contains one control register. The bits of this register include clock select and enable functions, the rest contain PLL frequency parameters. After writing the start index address in the PLL address register, these registers can be accessed in successive two (or one) bytes. The address register auto increments after one or two bytes to access the entire register set.

Absolute Maximum Ratings

Power Supply Voltage ..... 7 V
Voltage on any other pin ..... GND – 0.5V to V_{DD} + 0.5V
Temperature under bias ..... – 40° C to 85° C
Storage Temperature ..... – 65° C to 150° C
DC Digital Output Current ..... 25 mA
Analog Output Current ..... 45 mA
Reference Current ..... –15 mA
Power Dissipation ..... 1.0 W

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
DC CHARACTERISTICS (note: J)					
V_{DD}	Positive supply voltage		4.75	5.25	V
V_{IH}	Input logic "1" voltage		2.0	V_{DD} + 0.5	V
V_{IL}	Input logic "0" voltage		– 0.5	0.8	V
I_{REF}	Reference current		–7.0	–10	mA
V_{REF}	Reference voltage		1.10	1.35	V
I_{IN}	Digital input current	V_{DD} = max, GND ≤ V_{IN} ≤ V_{DD}		± 10	µA
I_{OZ}	Off-state digital output current	V_{DD} = max, GND ≤ V_{IN} ≤ V_{DD}		± 50	µA
I_{DD}	Average power supply current	I_O = max, Digital outputs unloaded		250	mA
I_{DACOFF}	DACs in power down mode	No palette access		50	mA
V_{OH}	Output logic "1"	I_O = –3.2mA, note K	2.4		V
V_{OL}	Output logic "0"	I_O = -3.2mA, note K		0.4	V
$ICLK_r$	Input Clock Rise Time	TTL levels		15	ns
$ICLK_f$	Input Clock Fall Time	TTL levels		15	ns
F_D	Frequency Change of CLK0 and CLK1 over supply and temperature	With respect to typical frequency		0.05	%

Electrical Characteristics (continued)

Symbol	Parameter	Conditions	Min	Max	Units
DAC CHARACTERISTICS (note: J)					
V_O (max)	Maximum output voltage	$I_O \leq 10$ mA		1.5	V
I_O (max)	Maximum output current	$V_O \leq 1V$		21	mA
	Full scale error	note A, B		± 5	%
	DAC to DAC correlation	note B		±2	%
	Integral Linearity, 6-bit	note B		±0.5	LSB
	Integral Linearity, 8-bit	note B		±1	LSB
	Full scale settling time*, 6-bit	note C		28	ns
	Full scale settling time*, 8-bit	note C		20	ns
	Rise time (10% to 90%)*	note C		6	ns
	Glitch energy*	note C		200	pVsec

* Characterized values only

Symbol	Parameter	Conditions	Min	Max	Units
PLL AC CHARACTERISTICS					
f_0	Clock 0 operating range		25	135	MHz
f_1	Clock 1 operating range		25	135	MHz
t_r	Output clocks rise time	25 pf load, TTL levels		1.5	ns
t_r	Output clocks fall time	25 pf load, TTL levels		1.5	ns
d_t	Duty Cycle		40/60	60/40	%
j_{1s}	Jitter, one sigma			130 ps	ps
j_{abs}	Jitter, absolute		-300 ps	300 ps	ps
f_{ref}	Input reference frequency	Typically 14.318 MHz	5	25	MHz

AC Electrical Characteristics (note: J)

Symbol	Parameter	Condition	80 MHz		110 MHz		135 MHz		Units
			Min	Max	Min	Max	Min	Max	
t_{CHCH}	PCLK period		12.5		9.09		7.4		ns
Δt_{CHCH}	PCLK jitter	note D		±2.5		+2.5			%
t_{CLCH}	PCLK width low		5		3.6		3		ns
t_{CHCL}	PCLK width high		5		3.6		3		ns
t_{PVCH}	Pixel word setup time	note E	3		3		2		ns
t_{CHPX}	Pixel word hold time	note E	3		2		1		ns
t_{BVCH}	BLANK* setup time	note E	3		3		2		ns
t_{CHBX}	BLANK* hold time	note E	3		2		1		ns
t_{CHAV}	PCLK to valid DAC output	note F		20		20		20	ns
Δt_{CHAV}	Differential output delay	note G		2		2		2	ns
t_{WLWH}	WR* pulse width low		50		50		50		ns
t_{RLRH}	RD* pulse width low		50		50		50		ns
t_{SVWL}	Register select setup time	Write cycle	10		10		10		ns
t_{SVRL}	Register select setup time	Read cycle	10		10		10		ns
t_{WLSX}	Register select hold time	Write cycle	10		10		10		ns
t_{RLSX}	Register select hold time	Read cycle	10		10		10		ns
t_{DVWH}	WR* data setup time		10		10		10		ns
t_{WHDX}	WR* data hold time		10		10		10		ns
t_{RLQX}	Output turn-on delay		5		5		5		ns
t_{RLQV}	RD* enable access time			40		40		40	ns
t_{RHQX}	Output hold time		5		5		5		ns
t_{RHQZ}	Output turn-off delay	note H		20		20		20	ns
t_{WHWL1}	Successive write interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{WHRL1}	WR* followed by read interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{RHRL1}	Successive read interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{RHWL1}	RD* followed by write interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{WHWL2}	WR* after color write	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{WHRL2}	RD* after color write	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{RHRL2}	RD* after color read	note I	8 (t_{CHCH})		8 (t_{CHCH})		8 (t_{CHCH})		cycle
t_{RHWL2}	WR* after color read	note I	8 (t_{CHCH})		8 (t_{CHCH})		8 (t_{CHCH})		cycle
t_{WHRL3}	RD* after read address write	note I	8 (t_{CHCH})		8 (t_{CHCH})		8 (t_{CHCH})		cycle
t_{SOD}	SENSE* output delay			1		1	1		µs

NOTES:

A. Full scale error is derived from design equation
{[(F.S I_{OUT}) R_L – 2 1 (I_{REF}) R_L]/[2 1(I_{REF})R_L]} 100%

$V_{BLACK\ LEVEL}$=0V F.S I_{OUT} = Actual full scale measured output

B. R= 37.5Ω, I_{REF} = – 8 88mA

C. Z_I = 37.5Ω + 30 pF, I_{REF} = – 8.88mA

D. This parameter is the allowed Pixel Clock frequency variation It does not permit the Pixel Clock period to vary outside the minimum values for Pixel Clock (t_{CHCH}) period

E It is required that the color palette's pixel address be a valid logic level with the appropriate setup and hold times at each rising edge of P_{CLK} (this requirement includes the blanking period)

F The output delay is measured from the 50% point of the rising edge of CLOCK to the valid analog output A valid analog output is defined when the analog signal is halfway between its successive values.

G. This applies to different analog outputs on the same device.

H. Measured at ± 200 mV from steady state output voltage

I. This parameter allows synchronization between operations on the microprocessor interface and the pixel stream being processed by the color palette.

J. The following specifications apply for V_{DD} = +5V± 0.5V, GND=0 Operating Temperature = 0°C to 70°C.

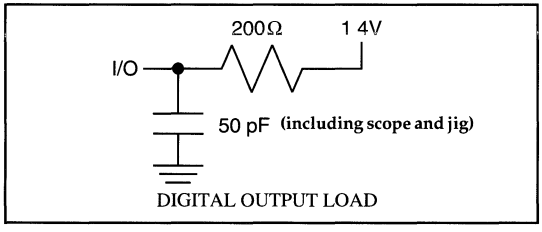
K. Except for SENSE pin

AC Test Conditions

Input pulse levels.....V_{DD} to 3V
Input rise and fall times (10% to 90%).....3ns
Digital input timing reference level.....1.5V
Digital output timing reference level.....0.8V and 2.4V

Capacitance

C_I Digital input.....7pF
C_O Digital output.....7pF
C_{OA} Analog output.....10pF



General Operation

The ICS5301 GENDAC is intended for use as the analog output stage of raster scan video systems. It contains a high-speed Random Access Memory of 256 x 18-bit words, three 6/8-bit high-speed DACs, a microprocessor/graphic controller interface, a pixel word mask, on-chip comparators, and two user programmable frequency generators.

C

An externally generated BLANK* signal can be applied to pin 39 of the ICS5301. This signal acts on all three of the analog outputs. The BLANK* signal is delayed internally so that it appears with the correct relationship to the pixel bit stream at the analog outputs.

A pixel word mask is included to allow the incoming pixel address to be masked. This permits rapid changes to the effective contents of the color palette RAM to facilitate such operations as animation and flashing objects. Operations on the contents of the mask register can also be totally asynchronous to the pixel stream.

The ICS5301 also includes dual PLL frequency generators providing a video clock (CLK0) and a memory clock (CLK1), both generated from a single 14.318 MHz crystal. There are eight selectable CLK0 frequencies of which six are programmable, and a single programmable CLK1 frequency. Default values (Table 1 and Table 2) are loaded into the appropriate registers on power up.

Video Path

The GENDAC supports four different video modes and is determined by bits 5-7 of the command register. The default mode is the 6-bit Pseudo Color mode. The other modes are the bypass 15-bit, 16-bit and 24 bit True Color.

Pseudo color

In this mode, Pixel Address and BLANK* inputs are sampled on the rising edge of the clock (PCLK) and any change appears at the analog outputs after three succeeding rising edges of the clock. The DAC outputs depends on the data in the color palette RAM.

Bypass Modes

The GENDAC supports three different bypass modes; 15-bit (5,5,5) mode, 16-bit (5,6,5) mode and the 24-bit True Color 8-bit DAC mode. In these modes, the pixel address pins P0-P7 represent the Color Data that is applied directly to the DAC. The internal RAM is bypassed. In the 15/16-bit mode two consecutive bytes contain the 15/16 bits of color data. Two consecutive rising edges of the PCLK latch the data on the P0-P7 pins into registers and the byte framing is internally synchronized with the rising edge of BLANK*. The internal pipe line delay from the "first byte" to the DAC is four PCLK rising edges. In the 24-bit True Color mode, three bytes contains the 24-bit color data. Three consecutive rising edges of the PCLK latch the data. The framing is the same as the 15/16-bit mode. The internal pipe line delay from the "first byte" to the DAC is five PCLK rising edges.

DAC Outputs

The outputs of the DACs are designed to be capable of producing 0.7 volt peak white amplitude with an I_{REF} of 8.88 mA when driving a doubly terminated 75Ω load. This corresponds to an effective DAC output load ($R_{EFFECTIVE}$) of 37.5Ω.

The formula for calculating I_{REF} with various peak white voltage/output loading combinations is given below:

$$I_{REF} = \frac{V_{PEAK\ WHITE}}{2.1 \times R_{EFFECTIVE}}$$

Note that for all values of I_{REF} and output loading:

$$V_{BLACK\ LEVEL} = 0$$

The reference current I_{REF} is determined by the reference voltage V_{REF} and the value of the resistor connected to R_{SET} pin. V_{REF} can be the internal band gap reference voltage or can be overridden by an external voltage. In both cases $I_{REF} = V_{REF}/R_{SET}$.

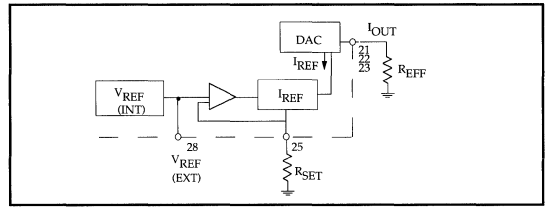


Figure 4 - DAC Set up

The BLANK* input to the GENDAC acts on all three of the DAC outputs. When the BLANK* input is low, the DACs are powered down.

The connection between the DAC outputs of the ICS5301 and the RGB inputs of the monitor should be regarded as a transmission line. Impedance changes along the transmission line will result in the reflection of part of the video signal back along the transmission line. These reflections may result in a degradation of the picture displayed by the monitor.

RF techniques should be observed to ensure good fidelity. The PCB trace connecting the GENDAC to the off-board connector should be sized to form a transmission line of the correct impedance. Correctly matched RF connectors should be used for connection from the PCB to the coaxial cable leading to the monitor and from the cable to the monitor.

There are two recommended methods of DAC termination: double termination and buffered signal. Each is described below with its relative merits:

Double Termination (Figure 1)
For this termination scheme, a load resistor is placed at both the DAC output and the monitor input. The resistor values should be equal to the characteristic impedance of the line. Double termination of the DAC output allows both ends of the transmission line between the DAC outputs and the monitor inputs to be correctly matched. The result should be an ideal reflection free system. This arrangement is relatively tolerant to variations in transmission line impedance (e.g. a mismatched connector) since no reflections occur from either end of the line.

A doubly terminated DAC output will rise faster than any singly terminated output because the rise time of the DAC outputs is dependent on the RC time constant of the load.

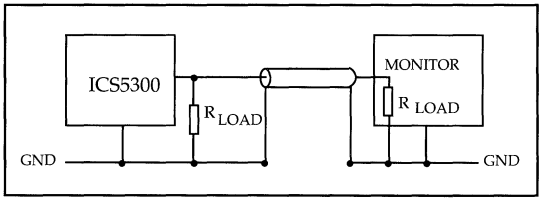


Figure 1 - Double Termination

Buffered Signal (Figure 2)
If the GENDAC drives large capacitive loads (for instance long cable runs), it may be necessary to buffer the DAC outputs. The buffer will have a relatively high input impedance. The connection between the DAC outputs and the buffer inputs should also be considered as a transmission line. The buffer output will have a relatively low impedance. It should be matched to the transmission line between it and the monitor with a series terminating resistor. The transmission line should be terminated at the monitor.

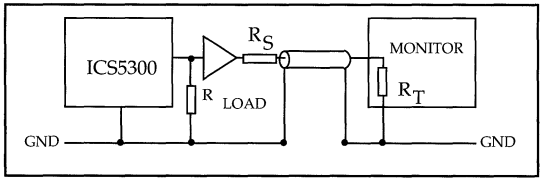


Figure 2 - Buffered Signal

SENSE Output

The GENDAC contains three comparators, one each for the DAC output (R, G and B) lines. The reference voltage to the comparators is proportional to the V_{REF} (internal or external) and is typically 0.33 for V_{REF} =1.23 Volts. When the voltage on any of these pins go higher than the reference voltage to the comparators, the SENSE* pin is driven low. This signal is used to detect the type of (or lack of) monitor connected to the system.

PLL Clock

The ICS5301 has dual PLL frequency generators for generating the video clock (CLK0) and memory clock (CLK1) needed for graphics subsystems. Both these clocks are generated from a single 14.318 MHz crystal or can be driven by an external clock source. The chip includes the capacitors for the crystal and all the components needed for the PLL loop filters, minimizing board component count.

There are eight possible video clock, CLK0, frequencies (f0-f7) which can be selected by the external pins CS0-CS2. Pins are software selectable by setting a bit in the PLL control register. Two of these frequencies (f0-f1) are fixed and the other six (f2-f7) can be programmed for any frequency by writing appropriate parameter values to the PLL parameter registers. The default frequencies on power up are commonly used video frequencies (table 1). At power up, the frequencies can be selected by pins CS0-CS2. There is only a single programmable memory clock frequency (CLK1). On power up this frequency defaults to the frequency given in table 2. The memory clock transition between frequencies is smooth and glitch free if the transition is kept between the limits 45-65 MHz.

fn	(MHz)	VLCK Comments
f0	50.350	VGA0 (VGA Color monitor) (fixed)
f1	56.644	VGA1 (VGA Monochrome monitor) (fixed)
f2	31.500	VESA 640 x 480 @72 Hz (programmable)
f3	36.00	VESA 800 x 600 @56 Hz (programmable)
f4	40.00	VESA 800 x 600 @60 Hz (programmable)
f5	44.889	1024 x 768 @43 Hz Interlaced (programmable)
f6	65.00	1024 x 768 @ 60 Hz, 640 x 480 Hi-Color @ 72 Hz (programmable)
f7	75.00	VESA 1024 x 768 @ 70 Hz, True Color 640 x 480 (programmable)

Table 1 - Video clock (CLK0) default frequency register (with a 14.318 MHz input)

MCLK (fA)	Comments
45.00 MHz	Memory and GUI subsystem clock Smooth transition between 45-65 MHz

Table 2 - Memory Clock (CLK1) Default Frequency Register

Microprocessor Interface

Below are listed the six microprocessor interface registers within the ICS5301, and the register addresses through which they can be accessed.

RS2	RS1	RS0	Register Name
0	0	0	Pixel Address (write mode)
0	1	1	Pixel Address (read mode)
0	0	1	Color Value
0	1	0	Pixel Mask
1	0	0	PLL Address (write mode)
1	0	1	PLL Parameter
1	1	0	Command
1	1	1	PLL Address (read mode)
0/HF	1	0	Command Register accessed by (hidden) flag after special sequence of events

Table 3 - Microprocessor Interface Registers

Asynchronous Access to Microprocessor Interface
Accesses to all registers may occur without reference to the high speed timing of the pixel bit stream being processed by the GENDAC. Data transfers between the color palette RAM and the Color Value register, as well as modifications to the Pixel Mask register, are synchronized to the Pixel Clock by internal logic. This is done in the period between microprocessor interface accesses. Thus, various minimum periods are specified between microprocessor interface accesses to allow the appropriate transfers or modifications to take place. Access to PLL address, PLL parameter and to the command register are asynchronous to the pixel clock.

The contents of the palette RAM can be accessed via the Color Value register and the Pixel Address registers.

Writing to the color palette RAM
To set a new color definition, a value specifying a location in the color palette RAM is first written to the Write mode Pixel Address register. The values for the red, green and blue intensities are then written in succession to the Color Value register. After the blue data is written to the Color Value register, the new color definition is transferred to the RAM, and the Pixel Address register is automatically incremented.

Writing new color definitions to a set of consecutive locations in the RAM is made easy by this auto-incrementing feature. First, the start address of the set of locations is written to the write mode Pixel Address register, followed by the color definition of that location. Since the address is incremented after each color definition is written, the color definition for the next location can be written immediately. Thus, the color definitions for consecutive locations can be written sequentially to the Color Value register without re-writing to the Pixel Address register each time.

Reading from the RAM
To read a color definition, a value specifying the location in the palette RAM to be read is written to the read mode Pixel Address register. After this value has been written, the contents of the location specified are copied to the Color Value register, and the Pixel Address register automatically increments.

The red, green and blue intensity values can be read by a sequence of three reads from the Color Value register. After the blue value has been read, the location in the RAM currently specified by the Pixel Address register is copied to the Color Value register and the Pixel Address again automatically increments. A set of color values in consecutive locations can be read simply by writing the start address of the set to the read mode Pixel Address register and then sequentially reading the color values for each location in the set. Whenever the Pixel Address register is updated, any unfinished color definition read or write is aborted and a new one may begin.

The Pixel Mask Register
The pixel address used to access the RAM through the pixel interface is the result of the bitwise ANDing of the

incoming pixel address and of the contents of the Pixel Mask register. This pixel masking process can be used to alter the displayed colors without altering the video memory or the RAM contents. By partitioning the color definitions by one or more bits in the pixel address, such effects as rapid animation, overlays, and flashing objects can be produced.

The Pixel Mask register is independent of the Pixel Address and Color Value registers.

The Command Register
The Command register is used to select the various GENDAC color modes and to set the power down mode. On power up this register defaults to an 6-bit Pseudo Color mode. This register can be accessed by control pins RS2-RS0, or by a special sequence of events for graphics subsystems that do not have the control signal RS2. For graphic systems that do not have RS2, this pin is tied low and an internal flag (HF; Hidden Flag) is set when the pixel mask register is read four times consecutively. Once the flag is set, the following Read or Write to the pixel mask register is directed to the command register. The flag is reset for Read or Write to any register other than the pixel mask register. The sequence has to be repeated for any subsequent access to the command register.

The PLL Parameter Register
The CLK0 and CLK1 of the ICS5301 can be programmed for different frequencies by writing different values to the PLL parameter register bank. There are eight registers in the parameter register; seven are two bytes long and one (0E) is one byte long.

Writing to the PLL parameter register
To write the PLL parameter data, the corresponding address location is first written to the PLL address register. For software compatibility with other chips, two address registers are defined; the Write mode PLL address register and the Read mode PLL address register. They are actually a single Read/Write register in the ICS5301. The next PLL parameter write will be directed to the first byte of the address location specified by the PLL address register. The next Write to the parameter register will automatically be to the second byte of this register. At the end of the second Write the address is automatically incremented. For the one byte "0E" register the address location is incremented after the first byte Write. If this frequency is selected while programming, the output frequency will change at the end of the second Write.

Reading the PLL parameter register
To read one of the registers of the PLL parameter register the address value corresponding to the location is first written to the PLL address register. The next PLL parameter read will be directed to the first byte of the address location pointed by this index register. A next Read of the parameter register will automatically be the second byte of this register. At the end of the second Read, the address location is automatically incremented. The address register (0E) is incremented after the first byte Read.

C

Power Down Mode

When bit 0 in the Command register is high (set to 1), the GENDAC enters the DAC power down mode. The DACs are turned off, and the data is retained in the RAM. It is possible to access the RAM, in which case the current will temporarily increase. While the RAM is being accessed, the current consumption will be proportional to the speed of the clock. There is no effect on either clock generator while in this mode.

Power Supply

As a high speed CMOS device, the ICS5301 may draw large transient currents from the power supply, it is necessary to adopt high frequency board layout and power distribution techniques to ensure proper operation of the GENDAC. Please refer to the suggested layout on page 29.

To supply the transient currents required by the ICS5301, the impedance in the decoupling path should be kept to a minimum between the power supply pins V_{DD} and GND. It is recommended that the decoupling capacitance between V_{DD} and GND should be a 0.1µF high frequency capacitor, in parallel with a large tantalum capacitor with

a value between 22μF and 47μF. A ferrite bead may be added in series with the positive supply to form a low pass filter and further improve the power supply local to the GENDAC. It will also reduce EMI.

The combination of series impedance in the ground supply to the GENDAC, and transients in the current drawn by the device will appear as differences in the GND voltages to the GENDAC and to the digital devices driving it. To minimize this differential ground noise, the impedance in the ground supply between the GENDAC and the digital devices driving it should be minimized.

Digital Output Information

The PCB trace lines between the outputs of the TTL devices driving the GENDAC and the input to the GENDAC behave like low impedance transmission lines driven from a low impedance transmission source and terminated with a high impedance. In accordance with transmission line principles, signal transitions will be reflected from the high impedance input to the device. Similarly, signal transitions will be inverted and reflected from the low impedance TTL output. Line termination is recommended to reduce or eliminate the ringing, particularly the undershoot caused by reflections. The termination may either be series or parallel.

Series termination is the recommended technique to use. It has the advantages of drawing no DC current and of using fewer components. Series termination is accomplished by placing a resistor in series with the signal at the output of the TTL driver. This matches the TTL output impedance to that of the transmission line and ensures that any signal incident on the TTL output is not reflected.

To minimize reflections, some experimentation will have to be done to find the proper value to use for the series termination. Generally, a value around 100Ω will be required. Since each design will result in a different signal impedance, a resistor of a predetermined value may not properly match the signal path impedance. Therefore, the proper value of resistance should be found empirically.

Functional Description

This section describes the register address and bit definition for RAMDAC and the Frequency Synthesizer sections.

Color Palette

Command Register

(RS0-RS2 = 011)
(RS0-RS1 = 01 with hidden flag)

By setting bits in the command register the ICS5301 can be programmed for different color modes and can be powered down for low power operation.

7 6 5	4 3 2 1	0
Color Mode 2 1 0	Reserved Should all =0	Snooze

Table 3 - Command Registers

Bit 7-5 Color Mode Select
These three bits select the Color Mode of RAMDAC operation as shown in the following table 4 (default is 0 at power up):

Bit 4 - 1 (Reserved)

Bit 0 Power Down Mode of RAMDAC
When this bit is set to 0 (default is 0), the device operates normally. If this bit is set to 1, the power and clock to the Color Palette RAM and DACs are turned off. The data in the Color Palette RAM are still preserved. The CPU can access without loss of data by internal automatic clock start/stop control. The DAC outputs become the same as BLANK* (sync) level output during power down mode. This bit does not effect the PLL clock synthesizer function.

Color Modes

The four selectable color modes are described here.

Mode 0: 8-bit Pseudo Color (one clock per pixel). This mode is the 8-bit per pixel Pseudo Color mode. In this mode. inputs P0-P7 are the pixel address for the color palette RAM and are latched on the rising edge of every PCLK. This is the default mode on power up and it is selected by setting bits CR7-CR5 to 000 . There are three clock cycles pipe line delays from input to DAC output.

8-bit Pseudo Color mode

DATA BYTE							
7	6	5	4	3	2	1	0
PIXEL ACCESS							
7	6	5	4	3	2	1	0

CM2 (CR7)	CM1 (CR6)	CM0 (CR5)	Color Mode	Clock Cycles/ Pixel Bits
0	0	0	6-Bit Pseudo Color with Palette (Default)	1
0	0	1	15-Bit Direct Color with Bypass (Hi-Color)	2
0	1	0	24-Bit True Color with Bypass (True Color)	3
0	1	1	16-Bit Direct Color with Bypass (XGA)	2
1	0	0	15-Bit Direct Color with Bypass (Hi-Color)	2
1	0	1	15-Bit Direct Color with Bypass (Hi-Color)	2
1	1	0	16-Bit Direct Color with Bypass (XGA)	2
1	1	1	24-Bit True Color with Bypass (True Color)	3

Table 4 - Color Mode Select

Mode 1: (15-bit per color bypassHi-Color mode).
This mode is the 15-bit per pixel bypass mode. In this mode, inputs P0-P7 are the color DATA and are input directly to the DAC, bypassing the color palette. The two bytes of data is latched in two successive PCLK rising edges. ICS5301 supports only the two clock mode and does not support the mode where the data are latched on the rising and the falling edges. For compatibility, the 15/16 one clock modes are selected as two clock modes in this chip. The low-byte, high byte synchronization is internally done by the rising edge of BLANK*. Each color is 5-bit wide and is packed into two bytes as shown below. The mode is selected by setting bits CR7-CR5 to 001, 100 or 101.

15-Bit Color Mode

3LSB = set to zero

SECOND BYTE								FIRST BYTE							
P7	P6	P5	P4	P3	P2	P1	P0	P7	P6	P5	P4	P3	P2	P1	P0
X	7	6	5	4	3	7	6	5	4	3	7	6	5	4	3
	RED				GREEN						BLUE				

Mode 2: (16-bit per pixel bypass XGA mode).
This mode is the 16-bit per pixel bypass mode and the P0-P7 inputs to go to the DAC directly, bypassing the color palette. The 2 bytes data is latched on two successive rising edges and the low-byte, high-byte synchronization is internally done by the rising edge of BLANK*. In this mode, blue and red colors are 6 bits wide and green is 5 bits wide. The 2 bytes of data is packed as shown below. The mode is selected by setting bits CR7-CR5 to 011 or 110.

16-Bit color mode

2LSB = set to zero (green)
3LSB = set to zero (blue, red)

SECOND BYTE								FIRST BYTE							
P7	P6	P5	P4	P3	P2	P1	P0	P7	P6	P5	P4	P3	P2	P1	P0
7	6	5	4	3	7	6	5	4	3	2	7	6	5	4	3
RED					GREEN						BLUE				

Mode 3: (24-bit per pixel True Color Mode).
This mode is the 24-bit per pixel bypass mode. The three bytes of data are latched on three successive PCLK edges and the first byte is synchronized by the rising edge of BLANK*. In this mode, each of the colors are 8-bit wide and the DAC is an 8-bit wide DAC. The first byte is blue followed by green and red. This mode can be selected by setting bits CR7-CR5 to 010 or 111. The DAC outputs changes every three cycles and the pipeline delay from the first byte to output is five cycles.

24-bit color mode

THIRD BYTE								SECOND BYTE								FIRST BYTE							
P7	P6	P5	P4	P3	P2	P1	P0	P7	P6	P5	P4	P3	P2	P1	P0	P7	P6	P5	P4	P3	P2	P1	P0
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
RED								GREEN								BLUE							

Frequency Generators

The ICS5301 clock synthesizer can be reprogrammed through the microprocessor interface for any set of frequencies. This is done by writing appropriate values to the PLL Parameter Register Bank (table 5).

PLL Address Registers

The address of the parameter register is written to the PLL address registers before accessing the parameter register. This register is accessed by register select pins RS2-RS0 = 100 or 111.

7	6	5	4	3	2	1	0
PLL REGISTER ADDRESS							
7	6	5	4	3	2	1	0

PLL Parameter Register

There are sixteen registers in the PLL parameter register (table 5). Registers 00 to 07 are for the CLK0 selectable frequency list, Register 0A for CLK1 programmable frequency and register 0E is the PLL CLK0 control register.

Index	R/W	Register	
00	R/-	CLK0 f0 PLL Parameters	(2 bytes)
01	R/-	CLK0 f1 PLL Parameters	(2 bytes)
02	R/W	CLK0 f2 PLL Parameters	(2 bytes)
03	R/W	CLK0 f3 PLL Parameters	(2 bytes)
04	R/W	CLK0 f4 PLL Parameters	(2 bytes)
05	R/W	CLK0 f5 PLL Parameters	(2 bytes)
06	R/W	CLK0 f6 PLL Parameters	(2 bytes)
07	R/W	CLK0 f7 PLL Parameters	(2 bytes)
08	R/-	(Reserved) = 0	(2 bytes)
09	R/-	(Reserved) = 0	(2 bytes)
0A	R/W	CLK1fA PLL	(2 bytes)
0B	R/-	(Reserved) = 0	(2 bytes)
0C	R/-	(Reserved) = 0	(2 bytes)
0D	R/-	(Reserved) = 0	(2 bytes)
0E	R/W	PLL Control Register	(1-byte)
0F	R/-	(Reserved) = 0	(2-byte)

Table 5 - PLL Parameter Registers

PLL Control Register

Bits in this register determine internal or external CLK0 select.

7	6	5	4	3	2	1	0
(RV) =0	(RV) =0	ENBL INCS	(RV) =0	(RV) =0	INTERNAL SELECT X	X	X

Bit 7 - 6 Reserved.

Bit 5 Enable Internal Clock Select (INCS) for CLK0. When this bit is set to 1, the CLK0 output frequency is selected by bit 2 - 0 in this register. External pins CS0 - CS2 are ignored.

Bit 4 - 3 (Reserved).

Bit 2 - 0 Internal Clock Select for CLK0 (INCS). These three bits selects the CLK0 output frequency if bit 5 of this register is on. They are interpreted as an octal number, n, that selects fn. Default selects f0.

PLL Data Registers

The CLK0 and CLK1 input frequency is determined by the parameter values in this register. These are two bytes registers; the first byte is the M-byte and the second is the N-byte.

M-Byte PLL Parameter Input
The M-byte has a 7-bit value (1-127) which is the feedback divider of the PLL.

7	6	5	4	3	2	1	0
Reserved =0	M-Divider Value X	X	X	X	X	X	X

N-Byte PLL Parameter Input
The N-byte has two values. N1 sets a 5-bit value (1-31) for the input pre scalar and N2 is a 2-bit code for selecting 1, 2, 4, or 8 post divide clock output.

7	6	5	4	3	2	1	0
Reserved =0	N2-Code X	X	N1-Divider Value X	X	X	X	X

N2 Post Divide Code

N2 code	Divider
00	1
01	2
10	4
11	8

The block diagram of the PLL clock synthesizer is given in following figure 3.

Based on the M and N values, the output frequency of the clocks is given by the following equation:

$$F_{out} = \frac{(M+2) \times F_{ref}}{(N1+2) \times 2^{N2}}$$

M and N values should be programmed such that the frequency of the VC0 is within the optimum range for duty cycle, jitter and glitch free transition. Optimum duty cycle is achieved by programming N2 for values greater than one. See the following page for programming example.

Programming Example

Suppose an output frequency of 25.175 MHz is desired. The reference crystal is 14.318 MHz. The VCO should be targeted to run in the 100 to 180 MHz range, so choosing a post divide of 4 gives a VCO frequency of :

4 X 25.175=101.021 MHz

From the table on page 17, we find N2 = 2
Substituting F_{rel} = 14.318 and 2^{N2} = 4 into the equation on page 17:

$$\left(\frac{25.175}{14.318}\right)\cdot 4 = \frac{(M+2)}{(N1+2)}$$

by trial and error:

$$\left(\frac{25.175}{14.318}\right)\cdot 4 \approx \frac{127}{18}$$

so M + 2 = 127 M = 125
N1 + 2 = 18 N1 = 16

so the registers are:

M = 125d = 1 1 1 1 1 0 1 b
N = 0 & N2 code & N1 = 0 & 1 0 & 1 0 0 0 0
N = 0 1 0 1 0 0 0 0 b

Additional Information on Programming the Frequency Generator section of the GENDAC

When programming the GENDAC PLL parameter registers, there are many possible combinations of parameters which will give the correct output frequency. Some combinations are better than others, however. Here is a method to determine how the registers need to be set:

The key guidelines come from the operation of the phase locked loop, which has the following restrictions:

1. 2 MHz < f_{REF} < 32 MHz
   This refers to the input reference frequency. Most users simply connect a 14.318 MHz crystal to the crystal inputs, so this is not a problem.

2. $600\text{ kHz} < \frac{f_{REF}}{(N1+2)} \leq 8\text{ MHz}$
   This is the frequency input to the phase detector.

3. $60\text{ MHz} \leq \frac{(M+2)}{(N1+2)} f_{REF} \leq 270\text{ MHz}$

   This is the VCO frequency. In general, the VCO should run as fast as possible, because it has lower jitter at higher frequencies. Also, running the VCO at multiples of the desired frequency allows the use of output divides, which tends to improve the duty cycle.

4. f_{CLK0} and $f_{CLK1} \leq 135$ MHz
   This is the output frequency.

These rules lead to the following procedure for determining the PLL parameters, assuming rules 1 and 4 are satisfied.

A. Determine the value of N2 (either 1, 2, 4 or 8) by selecting the highest value of N2, which satisfies the condition

$N2^* f_{CLK} \leq 270$ MHz

B. Calculate $\frac{(M2+)}{(N1+2)} = \frac{2^{N2} f_{out}}{fref}$

C. Now (M+2) and (N1+2) must be found by trial and error. With a 14.318 MHz reference frequency, there will generally be a small output frequency error due to the resolution limit of (M+2) and (N1+2). For a given frequency tolerance, several different (M+2) and (N1+2) combinations can usually be found. Usually, a few minutes trying out numbers with a calculator will produce a workable combination. Multiplying possible values of (N1+2) by the desiredratio will indicate approximately the value of M. This method is shown in the example below. A program could be written to try all possible combinations of (M+2) and (N1+2) (3937 possible combinations), discard those outside error band, and select from those remaining by giving preference to ratios which use lower values of (M+2). Lower values of (M+2) and (N1+2) provide better noise rejection in the phase locked loop.

Example: Suppose we are using a 14.318 MHz reference crystal and wish to output a frequency of 66 MHz with an error of no greater than 0.5%. What are the values of the PLL data registers?

A. 66*8 = 528 > 250 VCO speed too high
66*4 = 264 > 250 VCO speed too high
66*2 = 132 < 250 VCO speed OK, N2 = 2, N2 code = 01 from table on page 17 of the data sheet.

B. 132/14.31818 = 9.219
This is the desired frequency multiplication ratio.

C. Setting (N1+2) = 3, 4,...12, 13 and performing some simple calculations yields the following table: (Note that N1 cannot be 0)

(N1+2)	(N1+2)*9.219	rounded (=M+2)	Actual Ratio	Percent Error
3	27.657	28	9.33	-1.23
4	36.876	37	9.25	-0.34
5	46.095	46	9.20	0.21
6	55.314	55	9.17	0.57
7	64.533	65	9.29	-0.72
8	73.752	74	9.25	-0.34
9	82.971	83	9.22	-0.03
10	92.19	92	9.20	0.21
11	101.409	101	9.18	0.40
12	110.628	111	9.25	-0.34
13	119.847	120	9.23	-0.13

The ratio 83/9 is closest. Thus (N2+2) = 9; N2=7. (M+2) = 83; M = 81. The M-byte PLL parameter word is simply 81 in binary, plus bit 7 (which must be set to 0), or 01010001. The N-byte PLL parameter word is N2 code (01) concatenated with 5 bits of N2 in binary (00111), or 00100111. Once again, bit 7 must be zero.

We have chosen the combination with the least frequency error, but several other combinations are within the 0.5% tolerance. Because the lowest value of (M+2) offers the best damping, the 37/4 combination will have the best power supply rejection. This results in lower jitter due to external noise.

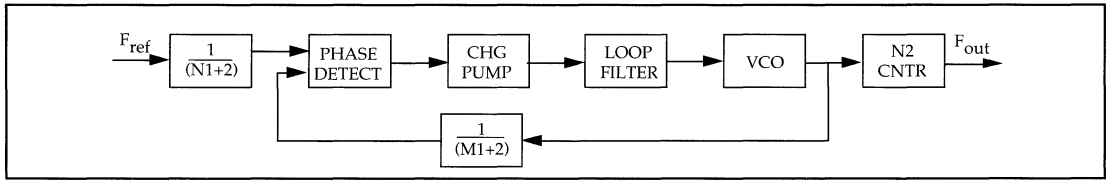
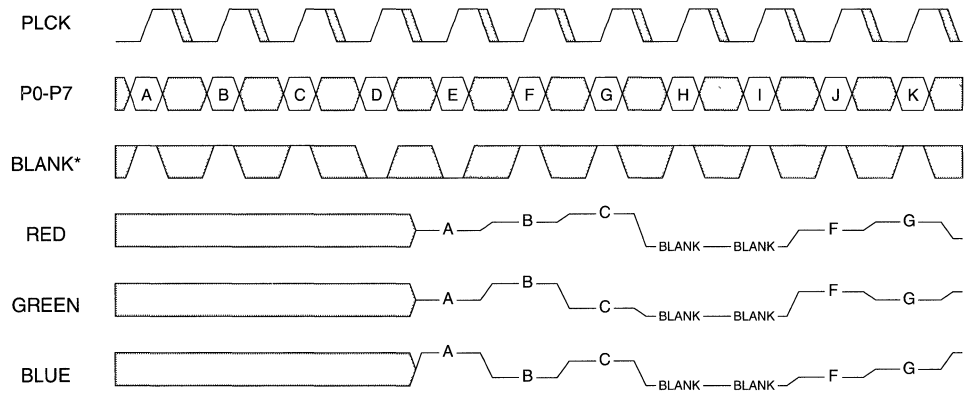


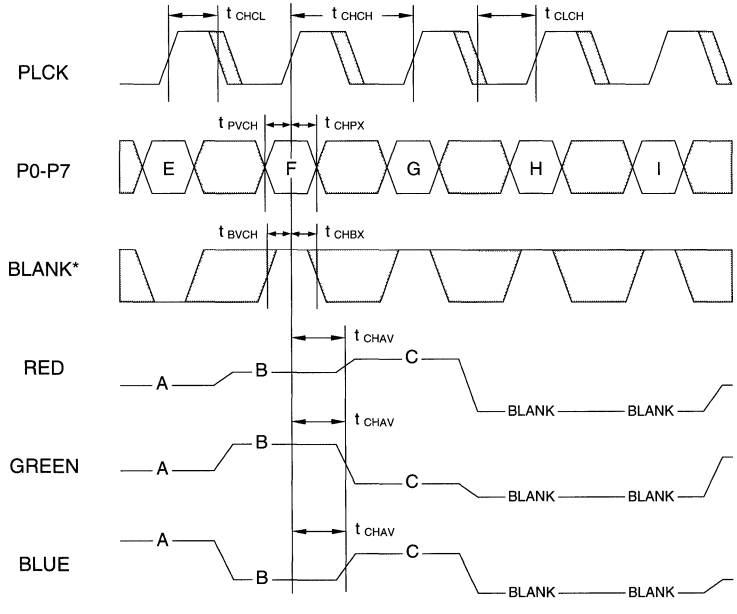
Figure 3 - PLL Clock Synthesizer Block Diagram

External Select			(Internal Select PLL Control Register)			
CS2	CS1	CS0	BIT 2	BIT 1	BIT 0	CLK 0 Frequency
0	0	0	0	0	0	f0
0	0	1	0	0	1	f1
0	1	0	0	1	0	f2
0	1	1	0	1	1	f3
1	0	0	1	0	0	f4
1	0	1	1	0	1	f5
1	1	0	1	1	0	f6
1	1	1	1	1	1	f7

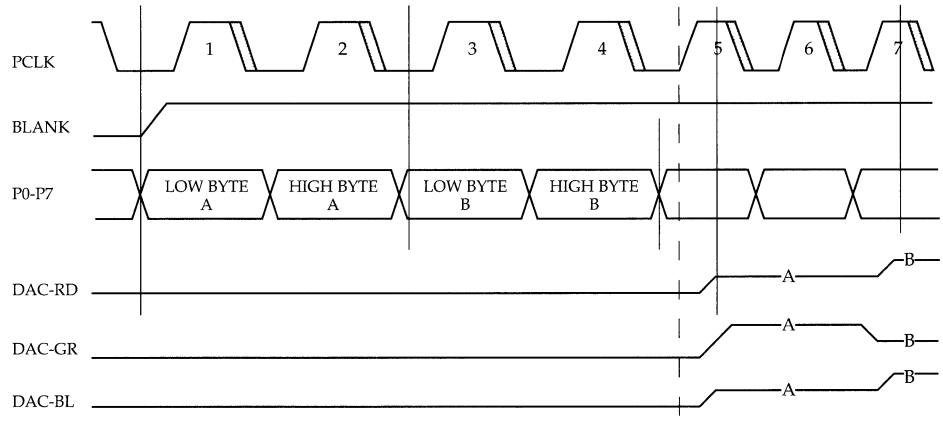
Video Clock Selection Table



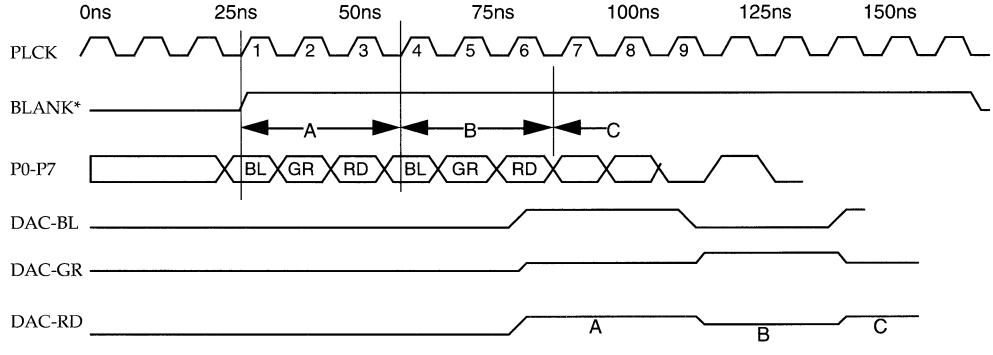
System Timing - Pseudo Color, Mode 0



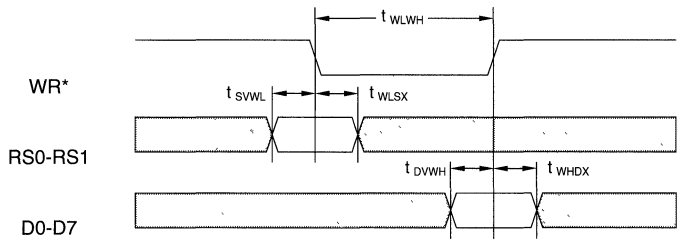
Detailed Timing Specifications - Pseudo Color, Mode 0



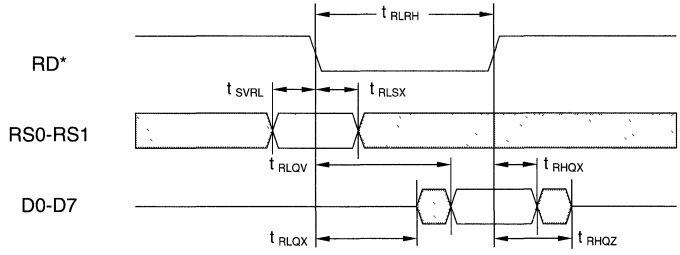
System Timing Bypass - 15 (5/5/5) and 16 (5/6/5) Modes 1, 2



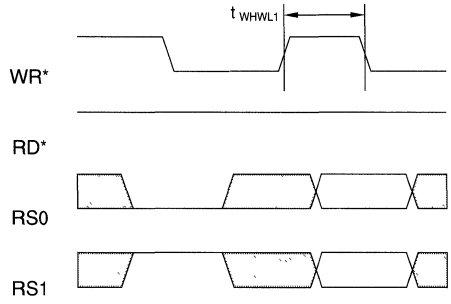
System Timing Bypass True Color 24 (8,8,8) Mode 3



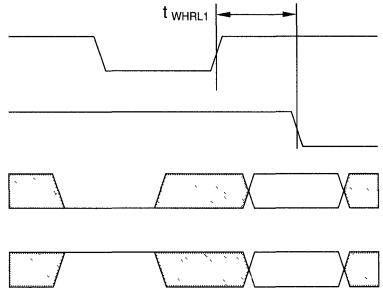
Basic Write Cycle Timing



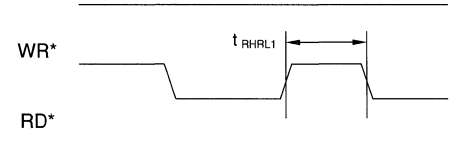
Basic Read Cycle Timing



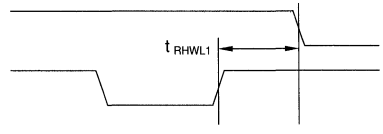
Write to Pixel Mask Register Followed by Write



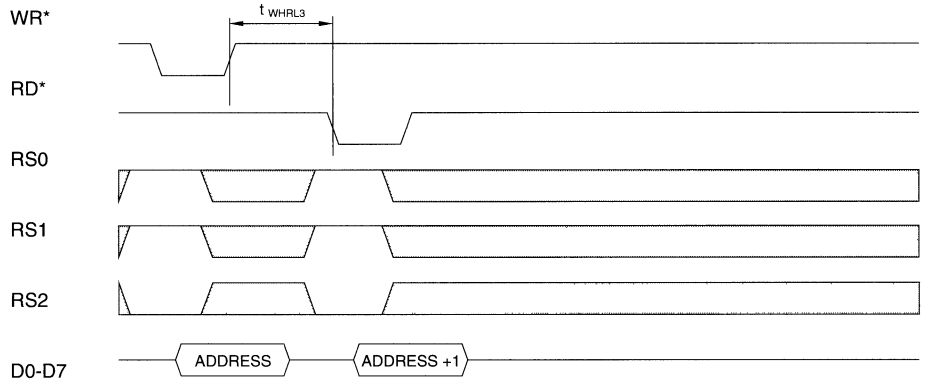
Write to Pixel Mask Register Followed by Read



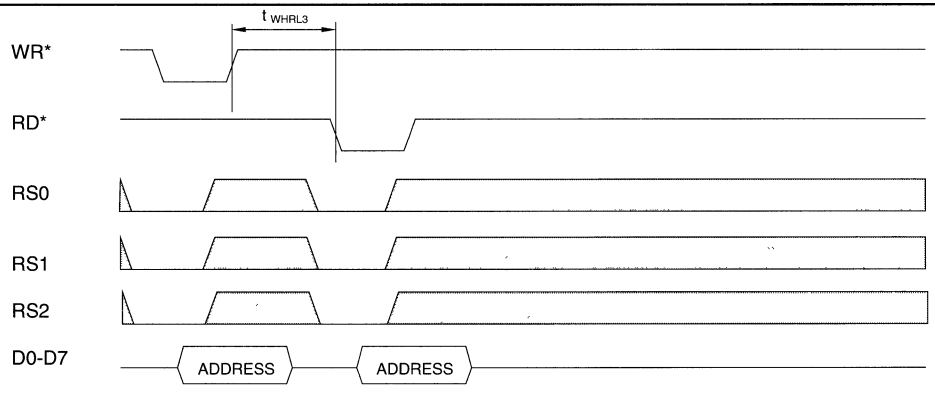
Read from Pixel or Pixel Address Register (Read or Write) followed by Read



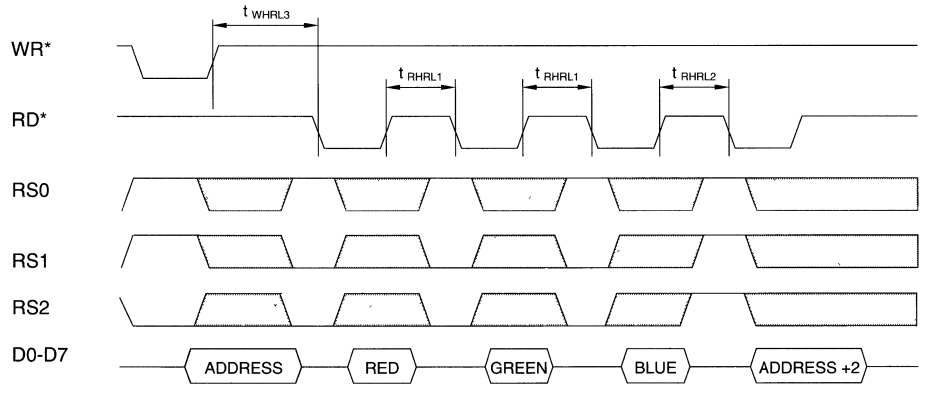
Read from Pixel or Pixel Address Register (Read or Write) followed by Write



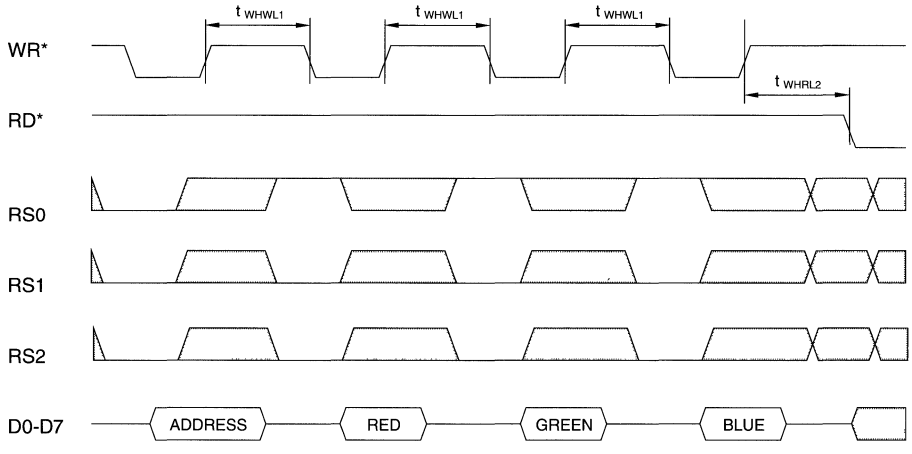
Write and Read Back Pixel Address Register (Read Mode)



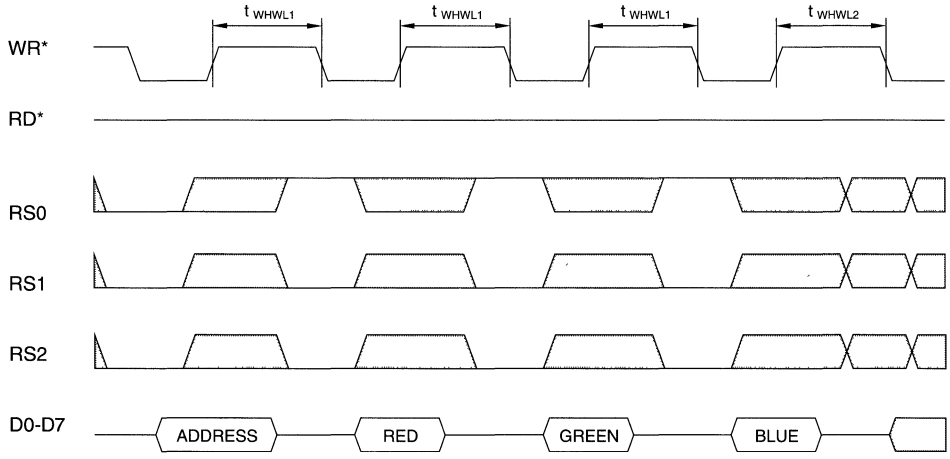
Write and Read Back Pixel Address Register (Write Mode)



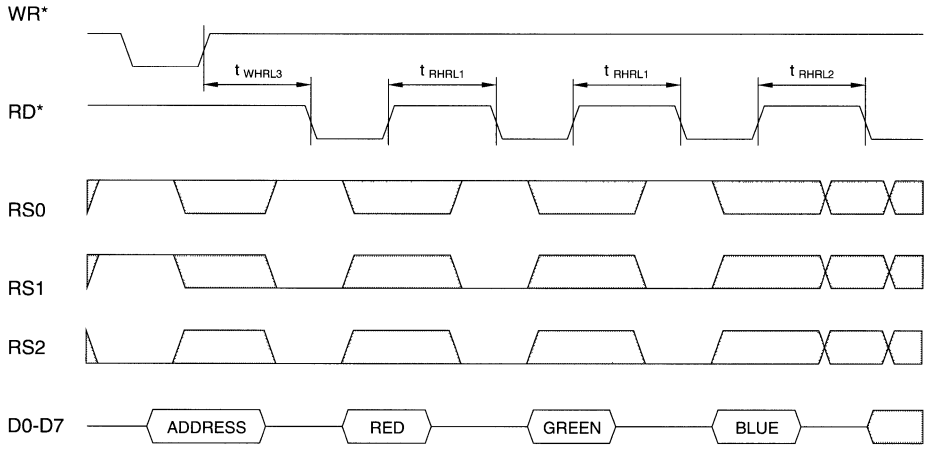
Read Color Value then Pixel Address Register (Read Mode)



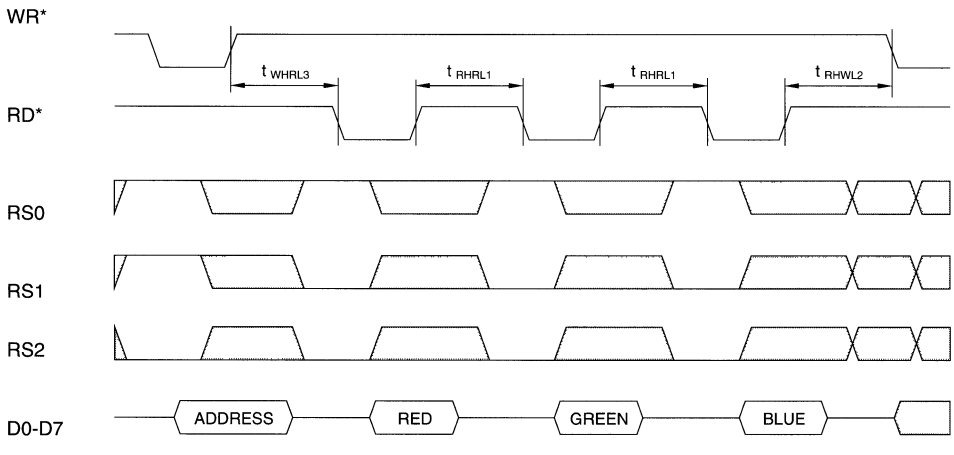
Color Value Write followed by any Read



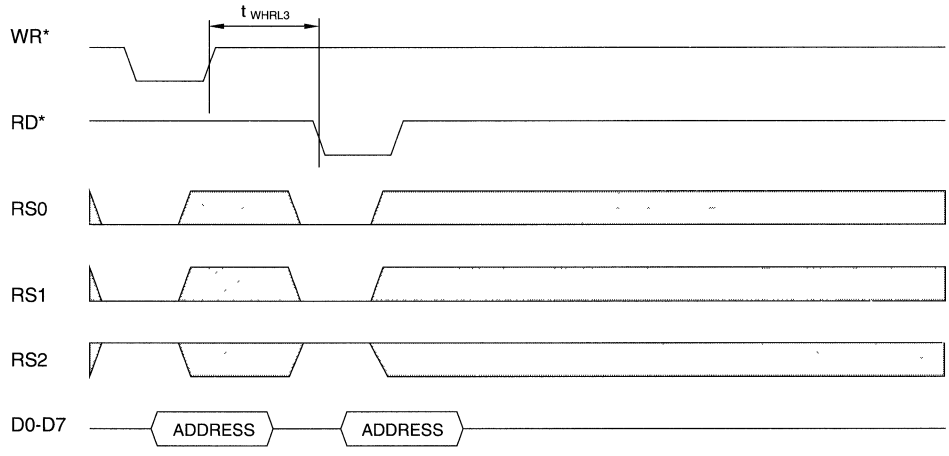
Color Value Write followed by any Write



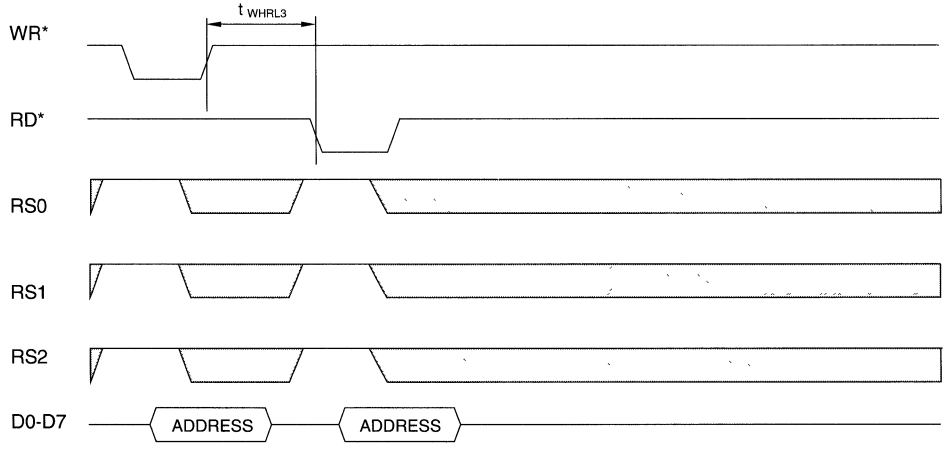
Color Value Read followed by any Read



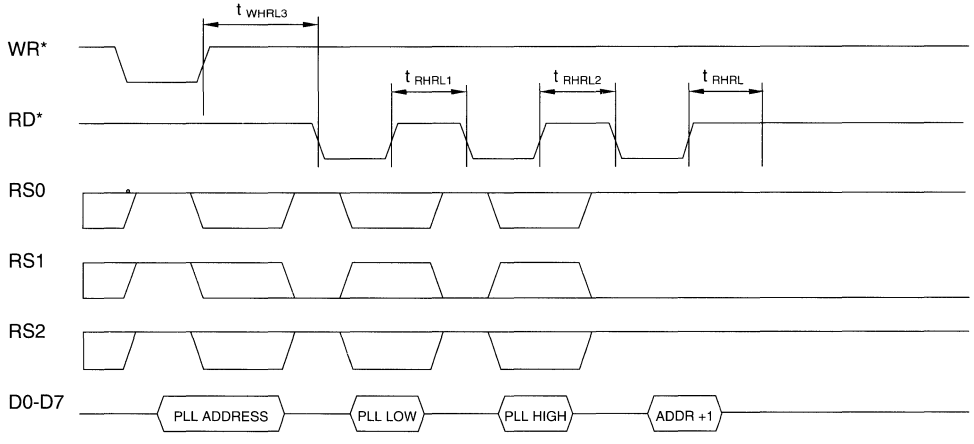
Color Value Read followed by any Write



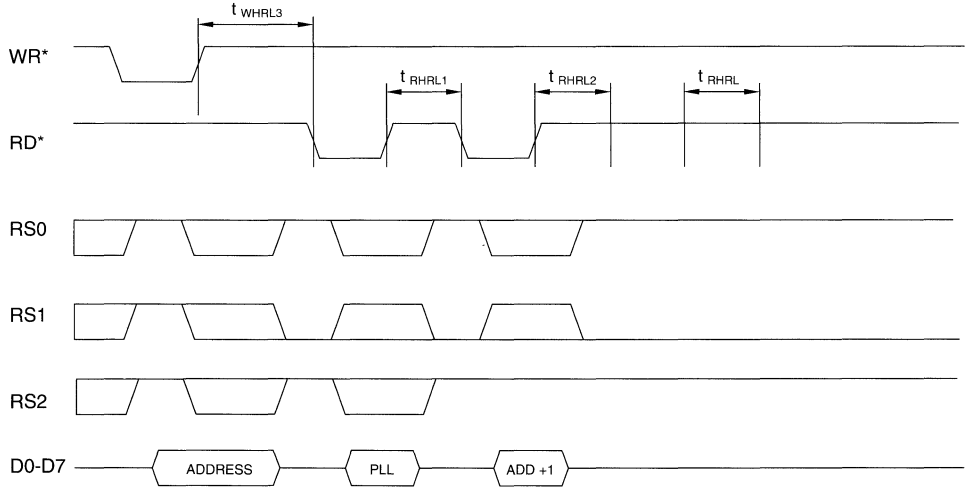
Write and Read back PLL Address Register (Write Mode)



Write and Read back PLL Address Register (Read Mode)

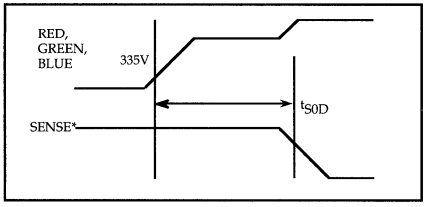


Read Two bytes PLL Register then PLL Address Register



Read One Byte PLL Register then PLL Address Register

Monitor SENSE Signal

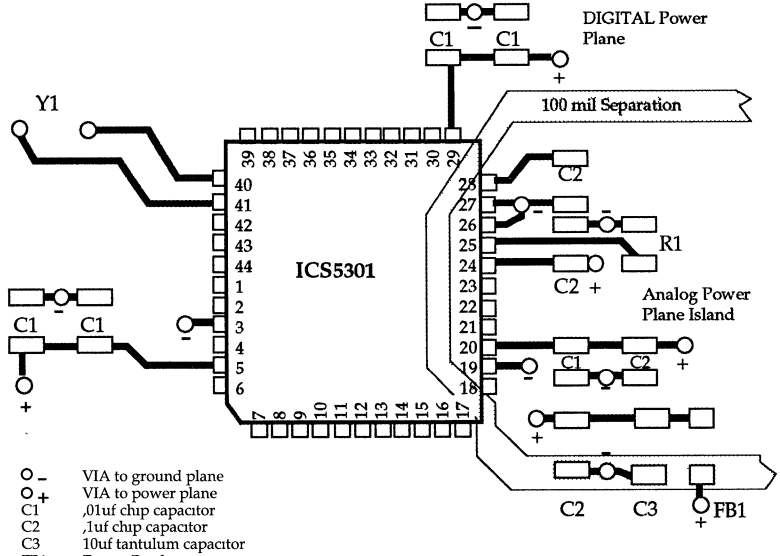


Recommended Layout

The high performance of which the ICS5301 GENDAC is capable is dependent on careful PC board layout. The use of a four layer board (internal power and ground planes, signals on the two surface layers) is recommended. The layout below shows a suggested configuration.

The ground plane is continuous, but the power plane is separated into analog and digital sections as shown. Power is supplied to the analog power plane through the ferrite bead, and bypassed at the power entry point by C3, a 10 µF tantalum capacitor. These high current connections should have multiple vias to the ground and power planes, if possible. Power connections should be connected to the analog or digital power plane, as shown in the diagram. Power pins 5 and 29 should be connected to digital power, power pins 20 and 24 to analog power. Decoupling capacitors (indicated by C1) should be placed as close to the GENDAC as possible.

The analog and digital I/O lines are not shown. Analog signals (DAC outputs, Vref, Rset) should only be routed above the analog power plane. Digital signals should only be routed above the digital power plane.



O –	VIA to ground plane
O +	VIA to power plane
C1	,01uf chip capacitor
C2	,1uf chip capacitor
C3	10uf tantulum capacitor
FB1	Ferrite Bead
R1	140 ohm 1% resistor
Y1	14.318 Mhz parallel resonant crysal cut for C_L=12

Integrated Circuit Systems, Inc.

ICS5340 GENDAC

16-Bit Integrated Clock-LUT-DAC

General Description

The ICS5340 GENDAC is a combination of dual programmable clock generators, a 256 x 18-bit RAM, and a triple 8-bit video DAC. The GENDAC supports 8-bit pseudo color applications, as well as 15-bit, 16-bit and 24-bit True Color bypass for high speed, direct access to the DACs.

The RAM makes it possible to display 256 colors selected from a possible 262,144 colors. The dual clock generators use Phase Locked Loop (PLL) technology to provide programmable frequencies for use in the graphics subsystem. The video clock contains 8 frequencies, 6 of which are programmable by the user. The memory clock has two programmable frequency locations.

The three 8-bit DACs on the ICS5340 are capable of driving singly or doubly-terminated 75Ω loads to nominal 0 - 0.7 volts at pixel rates up to 135 MHz. Differential and integral linearity errors are less than 1 LSB over full temperature and V_{DD} ranges. Monotonicity is guaranteed by design. On-chip pixel mask register allows displayed colors to be changed in a single write cycle rather than by modifying the color palette.

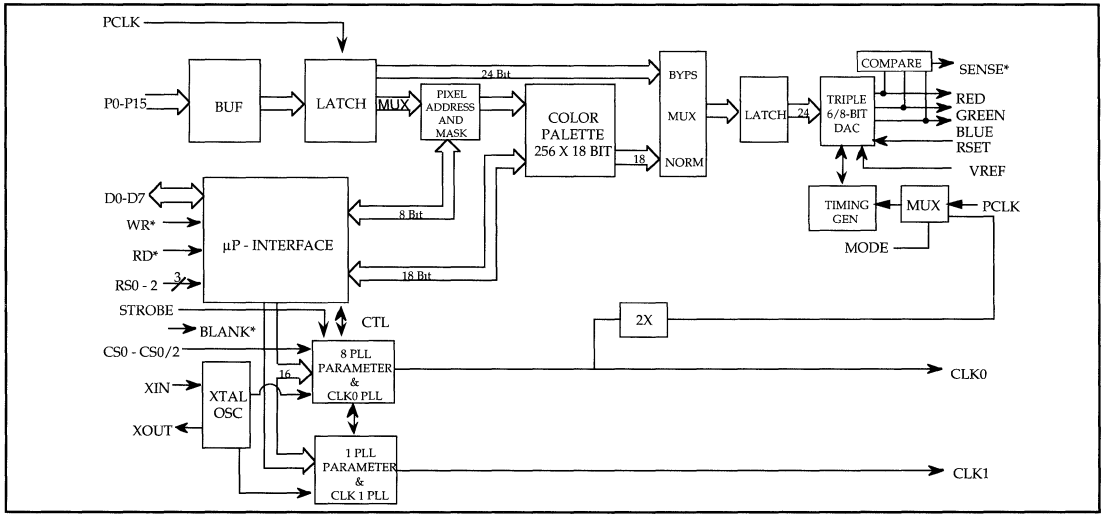
ICS is the world leader in all aspects of frequency (clock) generation for graphics, using patented techniques to produce low jitter video timing.

Features

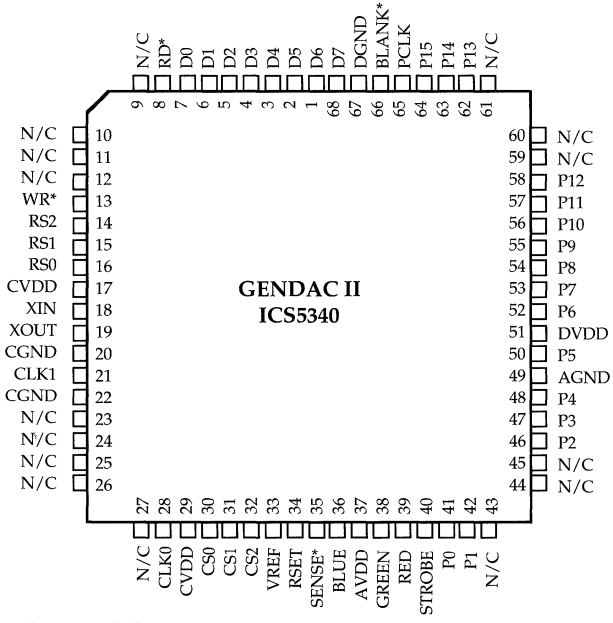
- **Triple video DAC, dual clock generator, and a color palette**
- **24, 16, 15, or 8-bit pseudo color pixel mode supports True Color, Hi-Color, and VGA modes**
- **High speed 256 x 18 color palette (135 MHz) with bypass mode and 8-bit DACs**
- **Two fixed, six programmable video (pixel) clock frequencies (CLK0)**
- **Two programmable memory (controller) clock frequency (CLK1)**
- **DAC power down in blanking mode**
- **Anti-sparkle circuitry**
- **On-chip loop filters reduce external components**
- **Standard CPU interface**
- **Single external crystal (typically 14.318 MHz)**
- **Monitor Sense**
- **Internal voltage reference**
- **135 MHz (-3), 110 MHz (-2) & 80 MHz (-1) versions**
- **Very low clock jitter**
- **Latched frequency control pin**

C

Block Diagram



Pin Configuration



Rev 1.0

Pin Description (68 pin PLCC)

Symbol	Pin #	Type	Description
D7 - D0	68, 1 - 7	I/O	System data bus I/O. These bidirectional Data I/O lines are used by the host microprocessor to write (using active low WR*) information into, and read (using active low RD*) information from the six internal registers (Pixel Address, Color Value, Pixel Mask, PLL Address, PLL Parameter, and Command). During the write cycle, the rising edge of WR* latches the data into the selected register (set by the status of the three RS pins). The rising edge of RD* determines the end of the read cycle. When RD* is a logical high, the Data I/O lines no longer contain information from the selected register and will go into a tri-state mode.
RD*	8	Input	RAM/PLL Read Enable, active low. This is the READ bus control signal. When active, any information present on the internal data bus is available on the Data I/O lines, D0-D7.
WR*	13	Input	RAM/PLL Write Enable, active low. This signal controls the timing of the write operation on the microprocessor interface inputs, D0-D7.
RS2 RS1 RS0	14 15 16	Input Input Input	Register Address Select 0. These inputs control the selection of one of the six internal registers. They are sampled on the falling edge of the active enable signal (RD* or WR*).
CVDD	17	-	Crystal oscillator and CLK0 power supply connect to AVDD.
XIN	18	Input	Crystal input. A 14.318 MHz crystal should be connected to this pin.
XOUT	19	Output	Crystal output. A 14.318 MHz crystal should be connected to this pin.
CGND	20	-	VSS for CLK0. Connect to ground.

Pin Description (continued)

Symbol	Pin #	Type	Description
CLK1	21	Output	Memory clock output. Used to time the video memory.
CGND	22	-	VSS for CLK1. Connect to ground.
CLK0	28	Output	Video clock output. Provides a CMOS level pixel or dot clock frequency to the graphics controller. The output frequency is determined by the values of the PLL registers.
CVDD	29	-	CLK1 Power Supply. Connect to AVDD.
CS0	30	Input	Clock select 0. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output. Latched by STB.
CS1	31	Input	Clock select 1. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output. Latched by STB.
CS2	32	Input	Clock select 2. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output. Latched by STB.
VREF	33	I/O	Internal Reference Voltage. Normally connects to a 0.1µ cap to ground. To use an external Vref, connect a 1.235V reference to this pin.
RSET	34	Input	Resistor Set. This pin is used to set the current level in the analog outputs. It is usually connected through a 140Ω, 1% resistor to ground.
SENSE*	35	Output	Monitor Sense, active low. This pin is low when any of the red, green, or blue outputs have exceeded 335mV. The chip has on-board comparators and an internal 335mV voltage reference. This is used to detect monitor type.
AVDD	37	-	DAC power supply. Connect to AVDD.
BLUE GREEN RED	36 38 39	Output Output Output	Color Signals. These three signals are the DACs' analog outputs. Each DAC is composed of several current sources. The outputs of each of the sources are added together according to the applied binary value. These outputs are typically used to drive a CRT monitor.
STROBE	40	Input	Latches the input clock select signals CS0 - CS2.
P0 - P15	41- 42 46-48, 50	Input	Pixel Address Lines. This byte-wide information is latched by the rising edge of PCLK when using the Color Palette, and is masked by the Pixel Mask register. These values are used to specify the RAM word address in the default mode (accessing RAM). In the Hi-Color XGA, and True Color modes, they represent color data for the DACs. These inputs should be grounded if they are not used.
AGND	49	-	DAC Ground. Connect to ground.
DVDD	51	-	Digital power supply.
PCLK	65 52-58, 62-64	Input	Pixel Clock. The rising edge of PCLK controls the latching of the Pixel Address and BLANK* inputs. This clock also controls the progress of these values through the three-stage pipeline of the Color Palette RAM, DAC, and outputs.
BLANK*	66	Input	Composite BLANK* Signal, active low. When BLANK* is asserted, the outputs of the DACs are zero and the screen becomes black. The DACs are automatically powered down to save current during blanking. The color palette may still be updated through D0-D7 during blanking.
DGND	67	-	Digital Ground. Connect to ground.

Internal Registers

RS2	RS1	RS0	Register Name	Description (all registers can be written to and read from)
0	0	0	Pixel Address WRITE	There is a single Pixel Address register within the GENDAC. This register can be accessed through either register address 0,0,0 or register address 0,1,1. A read from address 0,0,0 is identical to a read from address 0,1,1. Writing a value to address 0,0,0 performs the following operations: a) Specifies an address within the color palette RAM. b) Initializes the Color Value register. Writing a value to address 0,1,1 performs the following operations: a) Specifies an address within the color palette RAM. b) Loads the Color Value register with the contents of the location in the addressed RAM palette and then increments the Pixel Address register. Writing to this 8-bit register is performed prior to writing one or more color values to the color palette RAM.
0	1	1	Pixel Address READ	Writing to this 8-bit register is performed prior to reading one or more color values from the color palette RAM.
0	0	1	Color Value	The 18-bit Color Value register acts as a buffer between the microprocessor interface and the color palette. Using a three bytes transfer sequence allows a value to be read from or written to this register. When a byte is read, the color value is contained in the least significant 6 bits , D0-D5 (the most significant 2 bits are set to zero). When writing a byte, the same 6 bits are used. When reading or writing, data is transferred in the same order - the red byte first, then green, then blue. Each transfer between the Color Value register and the color palette replaces the normal pixel mapping operations of the GENDAC for a single pixel. After writing three definitions to this register, its contents are written to the location in the color palette RAM specified by the Pixel Address register, and the Pixel Address register increments. After reading three definitions from this register, the contents of the location in the color palette RAM specified by the Pixel Address registers are copied into the Color Value register, and the Pixel Address register increments.
0	1	0	Pixel Mask	The 8-bit Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs (P0-P7). A one in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered, while a zero sets that bit to zero. The Pixel Mask register does not affect the Pixel Address generated by the microprocessor interface when the palette RAM is being accessed.

Internal Registers (continued)

RS2	RS1	RS0	Register Name	Description (all registers can be written to and read from)
1	0	0	PLL Address WRITE	Writing to this 8-bit register is performed prior to writing one or more PLL programming values to the PLL Parameter register.
1	1	1	PLL Address READ	Writing to this 8-bit register is performed prior to reading one or more PLL programming values from the PLL Parameter register.
1	1	0	Command	This 8-bit register selects the color mode, for instance 8-bit Pseudo Color, Hi-Color , True Color, or XGA, and DAC power down. The registers are reset to pseudo color mode on power up.
1	0	1	PLL Parameter	There are sixteen parameter registers as indexed by PLL Address Write/ Read registers. Parameter registers 00-0D and 0F are two bytes long and 0E* is one byte long. This register set contains one control register. The bits of this register include clock select and enable functions, the rest contain PLL frequency parameters. After writing the start index address in the PLL address register, these registers can be accessed in successive two (or one) bytes. The address register auto increments after one or two bytes to access the entire register set.

Absolute Maximum Ratings

Power Supply Voltage ..... 7 V
Voltage on any other pin ..... GND – 0.5V to V_{DD} + 0.5V
Temperature under bias ..... – 40° C to 85° C
Storage Temperature ..... – 65° C to 150° C
DC Digital Output Current ..... 25 mA
Analog Output Current ..... 45 mA
Reference Current ..... –15 mA
Power Dissipation ..... 1.0 W

Note Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
DC CHARACTERISTICS (note: J)					
V_{DD}	Positive supply voltage		4.75	5.25	V
V_{IH}	Input logic "1" voltage		2.0	V_{DD} + 0.5	V
V_{IL}	Input logic "0" voltage		– 0.5	0.8	V
I_{REF}	Reference current		–7.0	–10	mA
V_{REF}	Reference voltage		1.10	1.35	V
I_{IN}	Digital input current	V_{DD} = max, GND ≤ V_{IN} ≤ V_{DD}		± 10	µA
I_{OZ}	Off-state digital output current	V_{DD} = max, GND ≤ V_{IN} ≤ V_{DD}		± 50	µA
I_{DD}	Average power supply current	I_O = max, Digital outputs unloaded		250	mA
I_{DACOFF}	DACs in power down mode	No palette access		50	mA
V_{OHS}	Sense logic "1"	I_O = .4mA	2.4		V
V_{OLS}	Sense logic "0"	I_O = .4mA		0.4	V
V_{OHC}	Clock logic "1"	I_O = TBD	2.4		V
V_{OLC}	Clock logic "0"	I_O = TBD		0.4	V
V_{OH}	logic "1"	I_O = -3.2mA, note K	2.4		V
V_{OL}	logic "0"	I_O = 3.2mA, note K		0.4	V
$ICLK_r$*	Input Clock Rise Time	TTL levels		15	ns
$ICLK_f$*	Input Clock Fall Time	TTL levels		15	ns
F_D	Frequency Change of CLK0 and CLK1 over supply and temperature	With respect to typical frequency		0.05	%

Electrical Characteristics (continued)

Symbol	Parameter	Conditions	Min	Max	Units
DAC CHARACTERISTICS (note: J)					
V_O (max)	Maximum output voltage	$I_O \leq 10$ mA		1.5	V
I_O (max)	Maximum output current	$V_O \leq 1V$		21	mA
	Full scale error	note A, B		± 5	%
	DAC to DAC correlation	note B		±2	%
	Integral Linearity, 6-bit	note B		±0.5	LSB
	Integral Linearity, 8-bit	note B		±1	LSB
	Full scale settling time*, 6-bit	note C		28	ns
	Full scale settling time*, 8-bit	note C		20	ns
	Rise time (10% to 90%)*	note C		6	ns
	Glitch energy*	note C		200	pVsec

* Characterized values only

Symbol	Parameter	Conditions	Min	Max	Units
PLL AC CHARACTERISTICS					
f_0	Clock 0 operating range*		25	135	MHz
f_1	Clock 1 operating range*		25	135	MHz
t_r	Output clocks rise time*	25 pf load, TTL levels		3	ns
t_r	Output clocks fall time*	25 pf load, TTL levels		3	ns
d_t	Duty Cycle*		40/60	60/40	%
j_{1s}	Jitter, one sigma*			130 ps	ps
j_{abs}	Jitter, absolute*		-300 ps	300 ps	ps
f_{ref}	Input reference frequency*	Typically 14.318 MHz	5	25	MHz

AC Electrical Characteristics (note: J)

Symbol	Parameter	Condition	80 MHz		110 MHz		135 MHz		Units
			Min	Max	Min	Max	Min	Max	
t_{CHCH}	PCLK period		12.5		9.09		7.4		ns
Δt_{CHCH}*	PCLK jitter	note D		±2.5		+2.5			%
t_{CLCH}	PCLK width low		5		3.6		3		ns
t_{CHCL}	PCLK width high		5		3.6		3		ns
t_{PVCH}	Pixel word setup time	note E	3		3		2		ns
t_{CHPX}	Pixel word hold time	note E	3		2		1		ns
t_{BVCH}	BLANK* setup time	note E	3		3		2		ns
t_{CHBX}	BLANK* hold time	note E	3		2		1		ns
t_{CHAV}*	PCLK to valid DAC output	note F		20		20		20	ns
Δt_{CHAV}	Differential output delay	note G		2		2		2	ns
t_{WLWH}	WR* pulse width low		50		50		50		ns
t_{RLRH}	RD* pulse width low		50		50		50		ns
t_{SVWL}	Register select setup time	Write cycle	10		10		10		ns
t_{SVRL}	Register select setup time	Read cycle	10		10		10		ns
t_{WLSX}	Register select hold time	Write cycle	10		10		10		ns
t_{RLSX}	Register select hold time	Read cycle	10		10		10		ns
t_{DVWH}	WR* data setup time		10		10		10		ns
t_{WHDX}	WR* data hold time		10		10		10		ns
t_{RLQX}	Output turn-on delay		5		5		5		ns
t_{RLQV}	RD* enable access time			40		40		40	ns
t_{RHQX}	Output hold time		5		5		5		ns
t_{RHQZ}	Output turn-off delay	note H		20		20		20	ns
t_{WHWL1}	Successive write interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{WHRL1}	WR* followed by read interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{RHRL1}	Successive read interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{RHWL1}	RD* followed by write interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{WHWL2}	WR* after color write	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{WHRL2}	RD* after color write	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{RHRL2}	RD* after color read	note I	8 (t_{CHCH})		8 (t_{CHCH})		8 (t_{CHCH})		cycle
t_{RHWL2}	WR* after color read	note I	8 (t_{CHCH})		8 (t_{CHCH})		8 (t_{CHCH})		cycle
t_{WHRL3}	RD* after read address write	note I	8 (t_{CHCH})		8 (t_{CHCH})		8 (t_{CHCH})		cycle
t_{SOD}	SENSE* output delay			1		1	1		µs

NOTES

A. Full scale error is derived from design equation
{[(F.S I_{OUT}) R_L – 2.1 (I_{REF}) R_L]/[2 1(I_{REF})R_L]} 100%

$V_{BLACK\ LEVEL}$=0V F.S I_{OUT} = Actual full scale measured output

B. R= 37.5Ω, I_{REF} = – 8.88mA

C Z_l = 37.5Ω + 30 pF, I_{REF} = – 8 88mA

D. This parameter is the allowed Pixel Clock frequency variation. It does not permit the Pixel Clock period to vary outside the minimum values for Pixel Clock (t_{CHCH}) period

E. It is required that the color palette's pixel address be a valid logic level with the appropriate setup and hold times at each rising edge of P_{CLK} (this requirement includes the blanking period).

F The output delay is measured from the 50% point of the rising edge of CLOCK to the valid analog output. A valid analog output is defined when the analog signal is halfway between its successive values.

G This applies to different analog outputs on the same device.

H. Measured at ± 200 mV from steady state output voltage

I. This parameter allows synchronization between operations on the microprocessor interface and the pixel stream being processed by the color palette.

J. The following specifications apply for V_{DD}= +5V± 0.5V, GND=0 Operating Temperature = 0°C to 70°C.

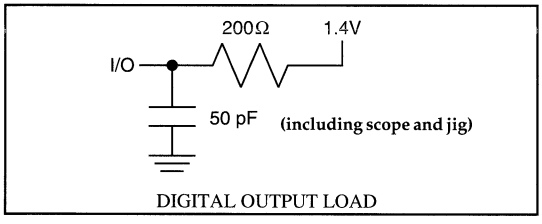
K. Except for SENSE pin.

AC Test Conditions

Input pulse levels.....V_{DD} to 3V
Input rise and fall times (10% to 90%).....3ns
Digital input timing reference level.....1.5V
Digital output timing reference level.....0.8V and 2.4V

Capacitance

C_I Digital input.....7pF
C_0 Digital output.....7pF
C_{0A} Analog output.....10pF



DIGITAL OUTPUT LOAD

General Operation

The ICS5340 GENDAC is intended for use as the analog output stage of raster scan video systems. It contains a high-speed Random Access Memory of 256 x 18-bit words, three 6/8-bit high-speed DACs, a microprocessor/graphic controller interface, a pixel word mask, on-chip comparators, and two user programmable frequency generators.

An externally generated BLANK* signal can be applied to pin 66 of the ICS5340. This signal acts on all three of the analog outputs. The BLANK* signal is delayed internally so that it appears with the correct relationship to the pixel bit stream at the analog outputs.

A pixel word mask is included to allow the incoming pixel address to be masked. This permits rapid changes to the effective contents of the color palette RAM to facilitate such operations as animation and flashing objects. Operations on the contents of the mask register can also be totally asynchronous to the pixel stream.

The ICS5340 also includes dual PLL frequency generators providing a video clock (CLK0) and a memory clock (CLK1), both generated from a single 14.318 MHz crystal. There are eight selectable CLK0 frequencies. Six are programmable, and two are fixed. There are two selectable and programmable CLK1 frequencies (fA, fB). Default values (Table 1 and Table 2) are loaded into the appropriate registers on power up.

Video Path

The GENDAC supports nine different video modes and is determined by bits 4-7 of the command register. The default mode is the 8-bit Pseudo Color mode. The other modes are the bypass 15-bit, 16-bit and 24 bit True Color modes in 8-bit and 16-bit interface, and the 16-bit Pseudo Color (2:1) mode with 2X Clock. . The 16-bit True Color has sparse and packed modes.

C

Pseudo Color

8-bit Interface
In this mode, Pixel Address, P0-P7 and BLANK* inputs are sampled on the rising edge of the clock (PCLK) and any change appears at the analog outputs after three succeeding rising edges of the PCLK. The DAC outputs depends on the data in the color palette RAM.

16-bit Interface
In this mode, Pixel Address, P0-P15 and BLANK* inputs are sampled on the rising edge of the clock (PCLK) and any change appears at the analog outputs after three succeeding rising edges of the 2 x ICLK. The DAC outputs depends on the data in the color palette RAM.

Bypass Mode

The GENDAC supports seven different bypass modes : three for byte transfers and four for word transfers. In these modes, the address pins P0-P15 represent Color Data that is applied directly to the DAC . The internal look-up table RAM is ignored. During byte transfers, the P8-P15 inputs are Don't Care. Data is always latched on the rising edge of PCLK. Byte or Word framing is internally synchronized with the rising edge of BLANK*.

Dac Outputs

The outputs of the DACs are designed to be capable of producing 0.7 volt peak white amplitude with an I_{REF} of 8.88 mA when driving a doubly terminated 75Ω load. This corresponds to an effective DAC output load ($R_{EFFECTIVE}$) of 37.5Ω. The formula for calculating I_{REF} with various peak white voltage/output loading combinations is given below:

$$I_{REF} = \frac{V_{PEAK\ WHITE}}{2.1 \times R_{EFFECTIVE}}$$

Note that for all values of I_{REF} and output loading:

$$V_{BLACK\ LEVEL} = 0$$

The reference current I_{REF} is determined by the reference voltage V_{REF} and the value of the resistor connected to R_{SET} pin. V_{REF} can be the internal band gap reference voltage or can be overridden by an external voltage. In both cases $I_{REF} = V_{REF}/R_{SET}$.

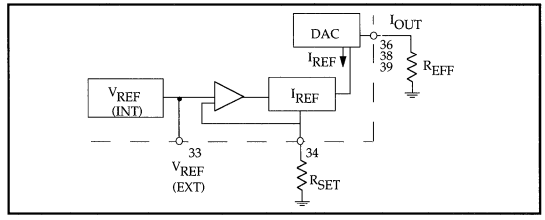


Figure 4 - DAC Set up

The BLANK* input to the GENDAC acts on all three of the DAC outputs. When the BLANK* input is low, the DACs are powered down.

The connection between the DAC outputs of the ICS5340 and the RGB inputs of the monitor should be regarded as a transmission line. Impedance changes along the transmission line will result in the reflection of part of the video signal back along the transmission line. These reflections may result in a degradation of the picture displayed by the monitor.

RF techniques should be observed to ensure good fidelity. The PCB trace connecting the GENDAC to the off-board connector should be sized to form a transmission line of the correct impedance. Correctly matched RF connectors should be used for connection from the PCB to the coaxial cable leading to the monitor and from the cable to the monitor.

There are two recommended methods of DAC termination: double termination and buffered signal. Each is described below with its relative merits:

Double Termination (Figure 1)
For this termination scheme, a load resistor is placed at both the DAC output and the monitor input. The resistor values should be equal to the characteristic impedance of the line. Double termination of the DAC output allows both ends of the transmission line between the DAC

outputs and the monitor inputs to be correctly matched. The result should be an ideal reflection free system. This arrangement is relatively tolerant to variations in transmission line impedance (e.g. a mismatched connector) since no reflections occur from either end of the line.

A doubly terminated DAC output will rise faster than any singly terminated output because the rise time of the DAC outputs is dependent on the RC time constant of the load.

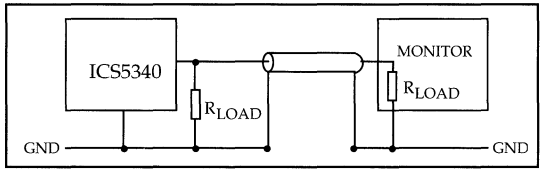


Figure 1 - Double Termination

Buffered Signal (Figure 2)
If the GENDAC drives large capacitive loads (for instance long cable runs), it may be necessary to buffer the DAC outputs. The buffer will have a relatively high input impedance. The connection between the DAC outputs and the buffer inputs should also be considered as a transmission line. The buffer output will have a relatively low impedance. It should be matched to the transmission line between it and the monitor with a series terminating resistor. The transmission line should be terminated at the monitor.

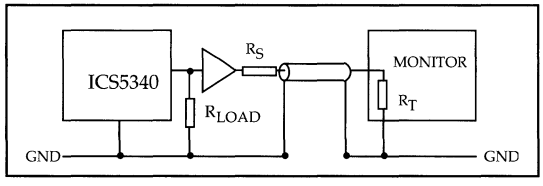


Figure 2 - Buffered Signal

SENSE Output

The GENDAC contains three comparators, one each for the DAC output (R, G and B) lines. The reference voltage to the comparators is proportional to the V_{REF} (internal or external) and is typically 0.33 for V_{REF} =1.23 Volts. When the voltage on any of these pins go higher than the reference voltage to the comparators, the SENSE* pin is driven low. This signal is used to detect the type of (or lack of) monitor connected to the system.

PLL Clock

The ICS5340 has dual PLL frequency generators for generating the video clock (CLK0) and memory clock (CLK1) needed for graphics subsystems. Both these clocks are generated from a single 14.318 MHz crystal or can be driven by an external clock source. The chip includes the capacitors for the crystal and all the components needed for the PLL loop filters, minimizing board component count.

There are eight possible video clock, CLK0, frequencies (f0-f7) which can be selected by the external pins CS0-CS2. Pins are software selectable by setting a bit in the PLL control register. Two of these frequencies (f0-f1) are fixed and the other six (f2-f7) can be programmed for any frequency by writing appropriate parameter values to the PLL parameter registers. The default frequencies on power up are commonly used video frequencies (table 1). At power up, the frequencies can be selected by pins CS0-CS2. There are two programmable memory clock frequencies (fA, fB). On power up this frequency defaults to the frequency given in table 2. The memory clock transition between frequencies is smooth and glitch free if the transition is kept between the limits 45-65 MHz.

fA	(MHz)	VLCK Comments
f0	25.175	VGA0 (VGA Graphics) (fixed)
f1	28.322	VGA1 (VGA Text) (fixed)
f2	31.500	VESA 640 x 480 @72 Hz (programmable)
f3	36.00	VESA 800 x 600 @56 Hz (programmable)
f4	40.00	VESA 800 x 600 @60 Hz (programmable)
f5	44.889	1024 x 768 @43 Hz Interlaced (programmable)
f6	65.00	1024 x 768 @ 60 Hz, 640 x 480 Hi-Color @ 72 Hz (programmable)
f7	75.00	VESA 1024 x 768 @ 70 Hz, True Color 640 x 480 (programmable)

Table 1 - Video clock (CLK0) default frequency register (with a 14.318 MHz input)

fn	MHz	Comments
fA	45.00 MHz	Memory and GUI subsystem clock
fB	55.00 MHz	Memory and GUI subsystem clock

Table 2 - Memory Clock (CLK1) default frequency register

Microprocessor Interface

Below are listed the six microprocessor interface registers within the ICS5340, and the register addresses through which they can be accessed.

RS2	RS1	RS0	Register Name
0	0	0	Pixel Address (write mode)
0	1	1	Pixel Address (read mode)
0	0	1	Color Value
0	1	0	Pixel Mask
1	0	0	PLL Address (write mode)
1	0	1	PLL Parameter
1	1	0	Command
1	1	1	PLL Address (read mode)
0/HF	1	0	Command Register accessed by (hidden) flag after special sequence of events

Table 3 - Microprocessor Interface Registers

Asynchronous Access to Microprocessor Interface
Accesses to all registers may occur without reference to the high speed timing of the pixel bit stream being processed by the GENDAC. Data transfers between the color palette RAM and the Color Value register, as well as modifications to the Pixel Mask register, are synchronized to the Pixel Clock by internal logic. This is done in the period between microprocessor interface accesses. Thus, various minimum periods are specified between microprocessor interface accesses to allow the appropriate transfers or modifications to take place. Access to PLL address, PLL parameter and to the command register are asynchronous to the pixel clock.

The contents of the palette RAM can be accessed via the Color Value register and the Pixel Address registers.

Writing to the color palette RAM

To set a new color definition, a value specifying a location in the color palette RAM is first written to the Write mode Pixel Address register. The values for the red, green and blue intensities are then written in succession to the Color Value register. After the blue data is written to the Color Value register, the new color definition is transferred to the RAM, and the Pixel Address register is automatically incremented.

Writing new color definitions to a set of consecutive locations in the RAM is made easy by this auto-incrementing feature. First, the start address of the set of locations is written to the write mode Pixel Address register, followed by the color definition of that location. Since the address is incremented after each color definition is written, the color definition for the next location can be written immediately. Thus, the color definitions for consecutive locations can be written sequentially to the Color Value register without re-writing to the Pixel Address register each time.

Reading from the RAM
To read a color definition, a value specifying the location in the palette RAM to be read is written to the read mode Pixel Address register. After this value has been written, the contents of the location specified are copied to the Color Value register, and the Pixel Address register automatically increments.

The red, green and blue intensity values can be read by a sequence of three reads from the Color Value register. After the blue value has been read, the location in the RAM currently specified by the Pixel Address register is copied to the Color Value register and the Pixel Address again automatically increments. A set of color values in consecutive locations can be read simply by writing the start address of the set to the read mode Pixel Address register and then sequentially reading the color values for each location in the set. Whenever the Pixel Address register is updated, any unfinished color definition read or write is aborted and a new one may begin.

The Pixel Mask Register
The pixel address used to access the RAM through the pixel interface is the result of the bitwise ANDing of the

incoming pixel address and of the contents of the Pixel Mask register. This pixel masking process can be used to alter the displayed colors without altering the video memory or the RAM contents. By partitioning the color definitions by one or more bits in the pixel address, such effects as rapid animation, overlays, and flashing objects can be produced.

The Pixel Mask register is independent of the Pixel Address and Color Value registers.

The Command Register
The Command register is used to select the various GENDAC color modes and to set the power down mode. On power up this register defaults to an 6-bit Pseudo Color mode. This register can be accessed by control pins RS2-RS0, or by a special sequence of events for graphics subsystems that do not have the control signal RS2. For graphic systems that do not have RS2, this pin is tied low and an internal flag (HF; Hidden Flag) is set when the pixel mask register is read four times consecutively. Once the flag is set, the following Read or Write to the pixel mask register is directed to the command register. The flag is reset for Read or Write to any register other than the pixel mask register. The sequence has to be repeated for any subsequent access to the command register.

The PLL Parameter Register
The CLK0 and CLK1 of the ICS5340 can be programmed for different frequencies by writing different values to the PLL parameter register bank. There are eight registers in the parameter register; seven are two bytes long and one (0E) is one byte long.

Writing to the PLL parameter register
To write the PLL parameter data, the corresponding address location is first written to the PLL address register. For software compatibility with other chips, two address registers are defined; the Write mode PLL address register and the Read mode PLL address register. They are actually a single Read/Write register in the ICS5340. The next PLL parameter write will be directed to the first byte of the address location specified by the PLL address register. The next Write to the parameter register will automatically be to the second byte of this register. At the end of the second Write the address is automatically incremented. For the one byte "0E" register the address location is incremented after the first byte Write. If this frequency is selected while programming, the output frequency will change at the end of the second Write.

Reading the PLL parameter register
To read one of the registers of the PLL parameter register the address value corresponding to the location is first written to the PLL address register. The next PLL parameter read will be directed to the first byte of the address location pointed by this index register. A next Read of the parameter register will automatically be the second byte of this register. At the end of the second Read, the address location is automatically incremented. The address register (0E) is incremented after the first byte Read.

C

Power Down Mode

When bit 0 in the Command register is high (set to 1), the GENDAC enters the DAC power down mode. The DACs are turned off, and the data is retained in the RAM. It is possible to access the RAM, in which case the current will temporarily increase. While the RAM is being accessed, the current consumption will be proportional to the speed of the clock. There is no effect on either clock generator while in this mode.

Power Supply

As a high speed CMOS device, the ICS5340 may draw large transient currents from the power supply, it is necessary to adopt high frequency board layout and power distribution techniques to ensure proper operation of the GENDAC. Please refer to the suggested layout on page 27.

To supply the transient currents required by the ICS5340, the impedance in the decoupling path should be kept to a minimum between the power supply pins V_{DD} and GND. It is recommended that the decoupling capacitance between V_{DD} and GND should be a 0.1µF high frequency capacitor, in parallel with a large tantalum capacitor with

a value between 22μF and 47μF. A ferrite bead may be added in series with the positive supply to form a low pass filter and further improve the power supply local to the GENDAC. It will also reduce EMI.

The combination of series impedance in the ground supply to the GENDAC, and transients in the current drawn by the device will appear as differences in the GND voltages to the GENDAC and to the digital devices driving it. To minimize this differential ground noise, the impedance in the ground supply between the GENDAC and the digital devices driving it should be minimized.

Digital Output Information

The PCB trace lines between the outputs of the TTL devices driving the GENDAC and the input to the GENDAC behave like low impedance transmission lines driven from a low impedance transmission source and terminated with a high impedance. In accordance with transmission line principles, signal transitions will be reflected from the high impedance input to the device. Similarly, signal transitions will be inverted and reflected from the low impedance TTL output. Line termination is recommended to reduce or eliminate the ringing, particularly the undershoot caused by reflections. The termination may either be series or parallel.

Series termination is the recommended technique to use. It has the advantages of drawing no DC current and of using fewer components. Series termination is accomplished by placing a resistor in series with the signal at the output of the TTL driver. This matches the TTL output impedance to that of the transmission line and ensures that any signal incident on the TTL output is not reflected.

To minimize reflections, some experimentation will have to be done to find the proper value to use for the series termination. Generally, a value around 100Ω will be required. Since each design will result in a different signal impedance, a resistor of a predetermined value may not properly match the signal path impedance. Therefore, the proper value of resistance should be found empirically.

Functional Description

This section describes the register address and bit definition for RAMDAC and the Frequency Synthesizer sections.

Color Palette Command Register

(RS0-RS2 = 011)
(RS0-RS1 = 01 with hidden flag)

By setting bits in the command register the ICS5340 can be programmed for different color modes and can be powered down for low power operation.

7 6 5	4	3 2 1	0
Color Mode 2 1 0	3	Reserved = 0	Snooze

Table 3 - Command Registers

Bit 7-4 **Color Mode Select**
These three bits select the Color Mode of RAMDAC operation as shown in the following table 4 (default is 0 at power up):

Bit 3 - 1 **(Reserved)**

Bit 0 **Power Down Mode of RAMDAC**
When this bit is set to 0 (default is 0), the device operates normally. If this bit is set to 1, the power and clock to the Color Palette RAM and DACs are turned off. The data in the Color Palette RAM are still preserved. The CPU can access without loss of data by internal automatic clock start/stop control. The DAC outputs become the same as BLANK* (sync) level output during power down mode. This bit does not effect the PLL clock synthesizer function.

8-BIT INTERFACE						
Mode Number	**CM3 (CR4)**	**CM2 (CR7)**	**CM1 (CR6)**	**CM0 (CR5)**	**Color Mode**	**Clock Cycles/ Pixel Bits**
0	0	0	0	0	8-Bit Pseudo Color with Palette (Default)	1
1	0	0	0	1	15-Bit Direct Color with Bypass (Hi-Color)	2
3	0	0	1	0	24-Bit True Color with Bypass (True Color)	3
2	0	0	1	1	16-Bit Direct Color with Bypass (XGA)	2
1	0	1	0	0	15-Bit Direct Color with Bypass (Hi-Color)	2
1	0	1	0	1	15-Bit Direct Color with Bypass (Hi-Color)	2
2	0	1	1	0	16-Bit Direct Color with Bypass (XGA)	2
3	0	1	1	1	24-Bit True Color with Bypass (True Color)	3
16-BIT INTERFACE						
Mode Number	**CM3 (CR4)**	**CM2 (CR7)**	**CM1 (CR6)**	**CM0 (CR5)**	**Color Mode**	**Clock Cycles/ Pixel Bits**
4	1	0	0	0	Muxed 16-Bit Pseudo Color with Palette	1/2
5	1	0	0	1	15-Bit Direct Color with Bypass (Hi-Color)	1
6	1	0	1	0	16-Bit Direct Color with Bypass (XGA)	1
7	1	0	1	1	24-Bit Direct Color with Bypass (True-Color)	2
8	1	1	0	0	24-Bit Packed Direct Color with Bypass (True-Color)	3/2
	1	1	0	1	Reserved	
	1	1	1	0	Reserved	
	1	1	1	1	Reserved	

Table 4 - Color Mode Select

Color Modes

The nine selectable color modes are described here. Modes 0 - 3 are 8-bit interfaces with P0-P7 bits, P8-P15 are Don't Care bits.

Mode 0: 8-bit Pseudo Color (one clock per pixel). This mode is the 8-bit per pixel Pseudo Color mode. In this mode, inputs P0-P7 are the pixel address for the color palette RAM and are latched on the rising edge of every PCLK. This is the default mode on power up and it is selected by setting bits CR7-CR4 to 0000 . There are three clock cycles pipe line delays from input to DAC output.

8-bit Pseudo Color Mode

PIXEL BYTE
P P P P P P P P
7 6 5 4 3 2 1 0
7 6 5 4 3 2 1 0
PIXEL ADDRESS

Mode 1: (15-bit per color bypassHi-Color mode).
This mode is the 15-bit per pixel bypass mode. In this mode, inputs P0-P7 are the color DATA and are input directly to the DAC, bypassing the color palette. The two bytes of data is latched in two successive PCLK rising edges. ICS5340 supports only the two clock mode and does not support the mode where the data are latched on the rising and the falling edges. For compatibility, the 15/16 one clock modes are selected as two clock modes in this chip. The low-byte, high byte synchronization is internally done by the rising edge of BLANK*. Each color is 5-bit wide and is packed into two bytes as shown below. This mode can be selected by setting bits CR7-CR4 to 0010, 1000 or 1010.

15-Bit Color Mode 1 Pixel Description

3LSB = set to zero

SECOND BYTE								FIRST BYTE							
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
X	7	6	5	4	3	7	6	5	4	3	7	6	5	4	3
	RED					GREEN					BLUE				

Mode 2: (16-bit per pixel bypass XGA mode).
This mode is the 16-bit per pixel bypass mode and the P0-P7 inputs to go to the DAC directly, bypassing the color palette. The 2 bytes data is latched on two successive rising edges and the low-byte, high-byte synchronization is internally done by the rising edge of BLANK*. In this mode, blue and red colors are 5 bits wide and green is 6 bits wide. The 2 bytes of data is packed as shown below. This mode can be selected by setting bits CR7-CR4 to 0110 or 1100.

16-Bit Color Mode 2 Pixel Description

2LSB = set to zero (green)
3LSB = set to zero (blue, red)

SECOND BYTE								FIRST BYTE							
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
7	6	5	4	3	7	6	5	4	3	2	7	6	5	4	3
RED					GREEN						BLUE				

Mode 3: (24-bit per pixel True Color Mode).
This mode is the 24-bit per pixel bypass mode. The three bytes of data are latched on three successive PCLK edges and the first byte is synchronized by the rising edge of BLANK*. In this mode, each of the colors are 8-bit wide and the DAC is an 8-bit wide DAC. The first byte is blue followed by green and red. This mode can be selected by setting bits CR7-CR4 to 0100 or 1110. The DAC outputs changes every three cycles and the pipeline delay from the first byte to output is five cycles.

24-bit Color Mode 3 Pixel Description

THIRD BYTE								SECOND BYTE								FIRST BYTE							
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
RED								GREEN								BLUE							

Modes 4 - 8 use the 16-bit pixel interface.

Mode 4: (8-bit Pseudo Color two pixels per clock) In this mode, inputs P0-P15 are latched on the rising edge of every PCLK. P0-7 and P8-P15 are used for successive addresses for the palette RAM using an internal clock that runs at twice the PCLK frequency. The DAC outputs change twice for every PCLK and the pipeline delay from the first word to output is one and a one half cycles. This mode can be selected by setting bits CR7-CR4 to 0001.

Multiplexed 8-bit Pseudo Color Word Mode 4 Pixel Description

PIXEL WORD	
P P P P P P P P P P P P P P P P	
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
7 6 5 4 3 2 1 0	7 6 5 4 3 2 2 0
2nd PIXEL ADDRESS	1st PIXEL ADDRESS

Mode 5: (16-bit pixel interface, 15-bit per color bypass Hi-Color Mode) In this mode inputs P0-P15 are the color Data and are input directly to the DAC, bypassing the color palette. The Data is latched by the rising edge of PCLK and is pipelined to the DAC. The pipeline delay from input to DAC output is 3 PCLK cycles. Each color is 5-bit wide as shown below. This mode is selected by setting bits CR7-CR4 to 0011.

15-Bit Color Word Mode 5 Pixel Description
3LSB = set to zero

P P P P P P P P P P P P P P P P			
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
X	7 6 5 4 3	7 6 5 4 3	7 6 5 4 3
	RED	GREEN	BLUE

Mode 6: (16-bit pixel interface, 16-bit per color bypass XGA mode) In this mode input P0-P15 are the color Data and are input directly to the DAC bypassing the color Palette. The Data is latched by the rising edge of PCLK and is pipelined to the DAC. The pipeline delay, from input to DAC output, is 3 PCLK cycles. In this mode Blue and Red colors are 5 bits wide, and Green is 6 bits wide. This mode is selected by selecting bits CR7-CR4 to 0101.

16-Bit Color Word Mode 6 Pixel Description
2LSB = set to zero (GREEN)
3LSB = set to zero (BLUE, RED)

P P P P P P P P P P P P P P P P		
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
7 6 5 4 3	7 6 5 4 3 2	7 6 5 4 3
RED	GREEN	BLUE

Mode 7: (16-bit pixel interface, 24-bit per color bypass TRUE color mode) In this mode inputs P0-P15 are the color Data and are input directly to the DAC bypassing the color Palette. Two words are latched on two successive rising edge of PCLK to form the 24-bit DAC input. The first word and the lower byte of the second word form the 24-bit pixel input to the DAC. The higher byte of the second word is ignored. The low and high word synchronization is internally done by the rising edge of the BLANK*. The pipeline delay from latching of first word to DAC output is 4 cycles and each pixel is 2 pixel clocks wide. In this mode, each of the colors are 8-bits wide and the DAC is 8-bit wide DAC. The first byte is Blue followed by Green and Red. This mode is selected by setting bits CR7-CR4 to 0111.

24-Bit Direct Color Word Mode 7 Pixel Description

FIRST WORD	
P P P P P P P P P P P P P P P P	
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
GREEN	BLUE

SECOND WORD	
P P P P P P P P P P P P P P P P	
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
	RED

Mode 8: (16-bit pixel interface packed 24-bit per color bypass TRUE color mode) In this mode inputs P0-P15 are the color Data and are input directly to the DAC bypassing the color Palette. Three words are latched on three successive rising edge of PCLK to form two successive 24-bit DAC inputs. The 16-bit first word and the lower byte of the second word from the first 24-bit pixel input and the second byte of the second word with the 16 bits of the third word from the second 24-bit pixel input. This cycle repeats every 3 cycles. The three word synchronization is internally done by the rising edge of BLANK*. The pipeline delay from latching of first word to DAC output is 3 ½ cycles and each of the colors are 8-bits wide and DAC is 8-bit wide DAC. The first byte is Blue followed by Green and Red. Repeats. This mode is selected by setting bits CR7-CR4 to 1001.

Packed 24-bit Word Mode 8 Pixel Description
1st DAC Cycle

SECOND WORD								FIRST WORD															
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
RED								GREEN								BLUE							

2nd DAC Cycle

THIRD WORD																SECOND WORD							
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
RED								GREEN								BLUE							

Frequency Generators

The ICS5340 clock synthesizer can be reprogrammed through the microprocessor interface for any set of frequencies. This is done by writing appropriate values to the PLL Parameter Register Bank (table 5).

PLL Address Registers

The address of the parameter register is written to the PLL address registers before accessing the parameter register. This register is accessed by register select pins RS2-RS0 = 100 or 111.

7	6	5	4	3	2	1	0
PLL REGISTER ADDRESS							
7	6	5	4	3	2	1	0

PLL Parameters Registers

There are sixteen registers in the PLL parameter register (table 5). Registers 00 to 07 are for the CLK0 selectable frequency list, Register 0A for CLK1 programmable frequency and register 0E is the PLL CLK0 control register.

Index	R/W	Register	
00	R/-	CLK0 f0 PLL Parameters	(2 bytes)
01	R/-	CLK0 f1 PLL Parameters	(2 bytes)
02	R/W	CLK0 f2 PLL Parameters	(2 bytes)
03	R/W	CLK0 f3 PLL Parameters	(2 bytes)
04	R/W	CLK0 f4 PLL Parameters	(2 bytes)
05	R/W	CLK0 f5 PLL Parameters	(2 bytes)
06	R/W	CLK0 f6 PLL Parameters	(2 bytes)
07	R/W	CLK0 f7 PLL Parameters	(2 bytes)
08	R/-	(Reserved) = 0	(2 bytes)
09	R/-	(Reserved) = 0	(2 bytes)
0A	R/W	CLK1 fA PLL	(2 bytes)
0B	R/W	CLK1 fB PLL	(2 bytes)
0C	R/-	(Reserved) = 0	(2 bytes)
0D	R/-	(Reserved) = 0	(2 bytes)
0E	R/W	PLL Control Register	(1-byte)
0F	R/-	(Reserved) = 0	(2-byte)

Table 5 - PLL Parameter Registers

PLL CONTROL REGISTER

Bits in this register determine internal or external CLK0 select.

7	6	5	4	3	2	1	0
(RV) =0	(RV) =0	ENBL INCS	CLK1 SEL	(RV) =0	INTERNAL SELECT		
					X	X	X

Bit 7,6, 3 Reserved.

Bit 5 Enable Internal Clock Select (INCS) for CLK0. When this bit is set to 1, the CLK0 output frequency is selected by bit 2 - 0 in this register. External pins CS0 - CS2 are ignored.

Bit 4 Clk1 Select
When this bit is set to 0, fA is selected. When it is set to 1, fB is selected. Default is 0, fA selected, at power up.

Bit 2 - 0 Internal Clock Select for CLK0 (INCS).
These three bits selects the CLK0 output frequency if bit 5 of this register is on. They are interpreted as an octal number, n, that selects fn. Default selects f0.

PLL Data Registers

The CLK0 and CLK1 input frequency is determined by the parameter values in this register. These are two bytes registers; the first byte is the M-byte and the second is the N-byte.

M-Byte PLL Parameter Input
The M-byte has a 7-bit value (1-127) which is the feedback divider of the PLL.

7	6	5	4	3	2	1	0
Reserved	M-Divider Value						
=0	X	X	X	X	X	X	X

N-Byte PLL Parameter Input
The N-byte has two values. N1 sets a 5-bit value (1-31) for the input pre scalar and N2 is a 2-bit code for selecting 1, 2, 4, or 8 post divide clock output.

7	6	5	4	3	2	1	0
Reserved	N2-Code		N1-Divider Value				
=0	X	X	X	X	X	X	X

N2 Post Divide Code

If mode 4 is set in the command register, CR7-CR4 equal 0001, N2 code must be 10.

N2 code	Divider
00	1
01	2
10	4
11	8

The block diagram of the PLL clock synthesizer is shown in figure 3.

Based on the M and N values, the output frequency of the clocks is given by the following equation:

$$F_{out} = \frac{(M+2) \times F_{ref}}{(N1+2) \times 2^{N2}}$$

M and N values should be programmed such that the frequency of the VC0 is within the optimum range for duty cycle, jitter and glitch free transition. Optimum duty cycle is achieved by programming N2 for values greater than one. See the next section for programming example.

Programming Example

Suppose an output frequency of 25.175 MHz is desired. The reference crystal is 14.318 MHz. The VCO should be targeted to run in the 100 to 180 MHz range, so choosing a post divide of 4 gives a VCO frequency of :

4 X 25.175=101.021 MHz

From the table in the previous section, we find N2 = 2
Substituting $F_{REF} = 14.318$ and $2^{N2} = 4$ into the equation on page 17:

$$\left(\frac{25.175}{14.318}\right) 4 = \frac{(M+2)}{(N1+2)}$$

by trial and error:

$$\left(\frac{25.175}{14.318}\right) \cdot 4 \approx \frac{127}{18}$$

so $M + 2 = 127$ $\quad M = 125$
$N1 + 2 = 18$ $\quad N1 = 16$

so the registers are:

M = 125d = 1 1 1 1 1 1 0 1 b
N = 0 & N2 code & N1 = 0 & 1 0 & 1 0 0 0 0
N = 0 1 0 1 0 0 0 0 b

Additional Information on Programming the Frequency Generator section of the GENDAC

When programming the GENDAC PLL parameter registers, there are many possible combinations of parameters which will give the correct output frequency. Some combinations are better than others, however. Here is a method to determine how the registers need to be set:

The key guidelines come from the operation of the phase locked loop, which has the following restrictions:

1. $2\ MHz < f_{REF} < 32\ MHz$

   This refers to the input reference frequency. Most users simply connect a 14.318 MHz crystal to the crystal inputs, so this is not a problem.

2. $600\ kHz < \frac{f_{REF}}{(N1+2)} \leq 8\ MHz$

   This is the frequency input to the phase detector.

3. $60\ MHz \leq \frac{(M+2)}{(N1+2)} f_{ref} \leq 270\ MHz$

   This is the VCO frequency. In general, the VCO should run as fast as possible, because it has lower jitter at higher frequencies. Also, running the VCO at multiples of the desired frequency allows the use of output divides, which tends to improve the duty cycle.

4. f_{CLK0} and $f_{CLK1} \leq 135\ MHz$

   This is the output frequency.

These rules lead to the following procedure for determining the PLL parameters, assuming rules 1 and 4 are satisfied.

A. Determine the value of N2 (either 1, 2, 4 or 8) by selecting the highest value of N2, which satisfies the condition $N2 * f_{CLK} \leq 270\ MHz$

B. Calculate $\frac{(M+2)}{(N1+2)} = \frac{2^{N2} f_{out}}{fref}$

C. Now (M+2) and (N1+2) must be found by trial and error. With a 14.318 MHz reference frequency, there will generally be a small output frequency error due to the resolution limit of (M+2) and (N1+2). For a given frequency tolerance, several different (M+2) and (N1+2) combinations can usually be found. Usually, a few minutes trying out numbers with a calculator will produce a workable combination. Multiplying possible values of (N1+2) by the desired ratio will indicate approximately the value of M. This method is shown in the example below. A program could be written to try all possible combinations of (M+2) and (N1+2) (3937 possible combinations), discard those outside error band, and select from those remaining by giving preference to ratios which use lower values of (M+2). Lower values of (M+2) and (N1+2) provide better noise rejection in the phase locked loop.

Example: Suppose we are using a 14.318 MHz reference crystal and wish to output a frequency of 66 MHz with an error of no greater than 0.5%. What are the values of the PLL data registers?

A. 66*8 = 528 > 250 VCO speed too high
66*4 = 264 > 250 VCO speed too high
66*2 = 132 < 250 VCO speed OK, N2 = 2, N2 code = 01 from table on page 17 of the data sheet.

B. 132/14.31818 = 9.219
This is the desired frequency multiplication ratio.

C. Setting (N1+2) = 3,4,...12, 13 and performing some simple calculations yields the following table: (Note that N1 cannot be 0).

(N1+2)	(N1+2)*9.219	rounded (=M+2)	Actual Ratio	Percent Error
3	27.657	28	9.33	-1.23
4	36.876	37	9.25	-0.34
5	46.095	46	9.20	0.21
6	55.314	55	9.17	0.57
7	64.533	65	9.29	-0.72
8	73.752	74	9.25	-0.34
9	82.971	83	9.22	-0.03
10	92.19	92	9.20	0.21
11	101.409	101	9.18	0.40
12	110.628	111	9.25	-0.34
13	119.847	120	9.23	-0.13

The ratio 83/9 is closest. Thus (N2+2) = 9; N2=7. (M+2) = 83; M = 81. The M-byte PLL parameter word is simply 81 in binary, plus bit 7 (which must be set to 0), or 01010001. The N-byte PLL parameter word is N2 code (01) concatenated with 5 bits of N2 in binary (00111), or 00100111. Once again, bit 7 must be zero.

We have chosen the combination with the least frequency error, but several other combinations are within the 0.5% tolerance. Because the lowest value of (M+2) offers the best damping, the 37/4 combination will have the best power supply rejection. This results in lower jitter due to external noise.

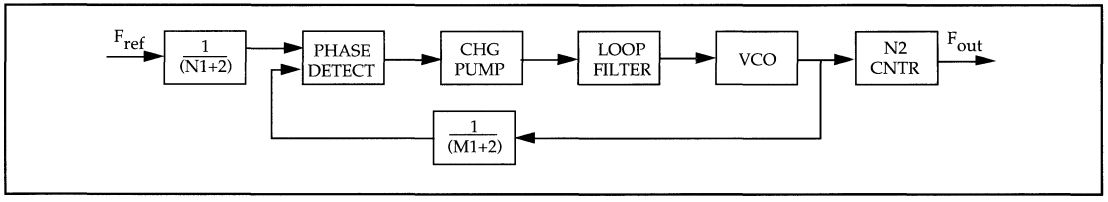
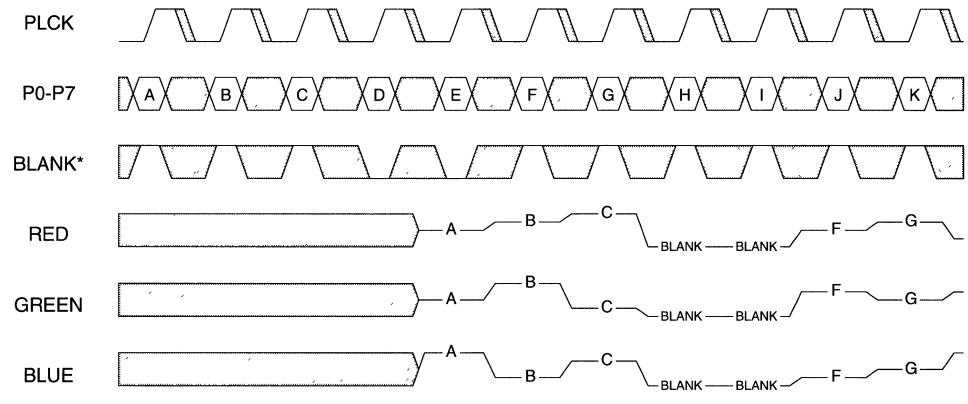


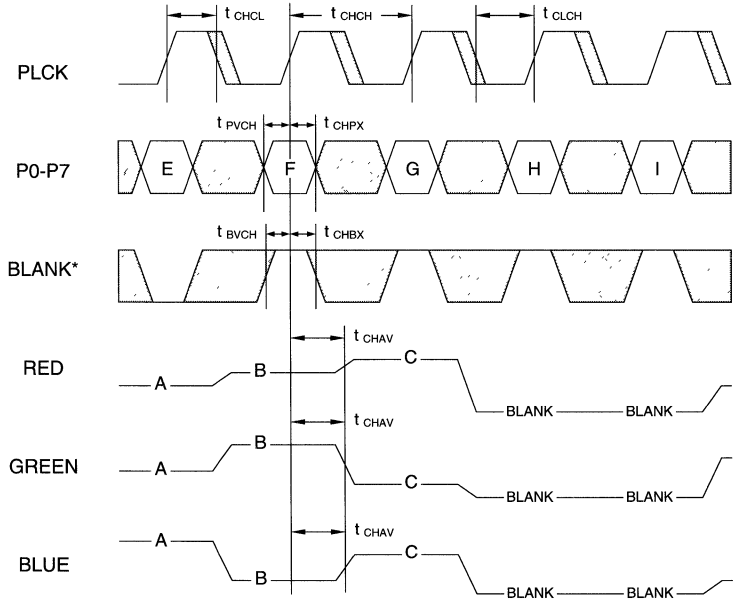
Figure 3 - PLL Clock Synthesizer Block Diagram

External Select			(Internal Select PLL Control Register)			
CS2	CS1	CS0	BIT 2	BIT 1	BIT 0	CLK 0 Frequency
0	0	0	0	0	0	f0
0	0	1	0	0	1	f1
0	1	0	0	1	0	f2
0	1	1	0	1	1	f3
1	0	0	1	0	0	f4
1	0	1	1	0	1	f5
1	1	0	1	1	0	f6
1	1	1	1	1	1	f7

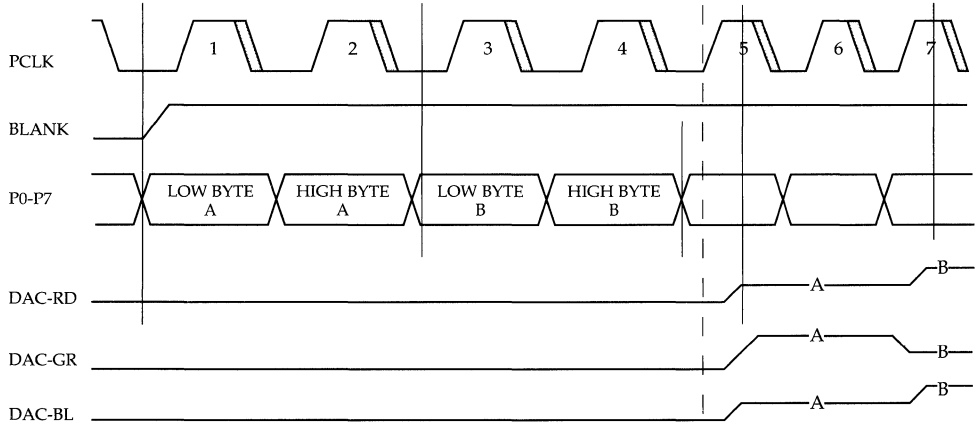
Video Clock Selection Table



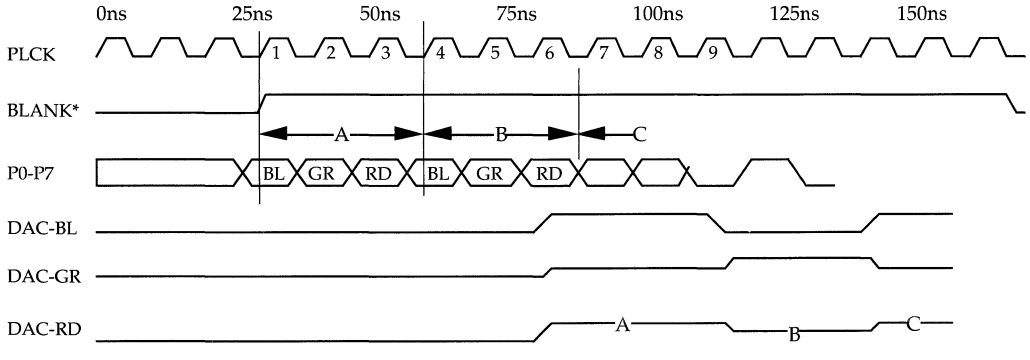
System Timing - Pseudo Color, Mode 0



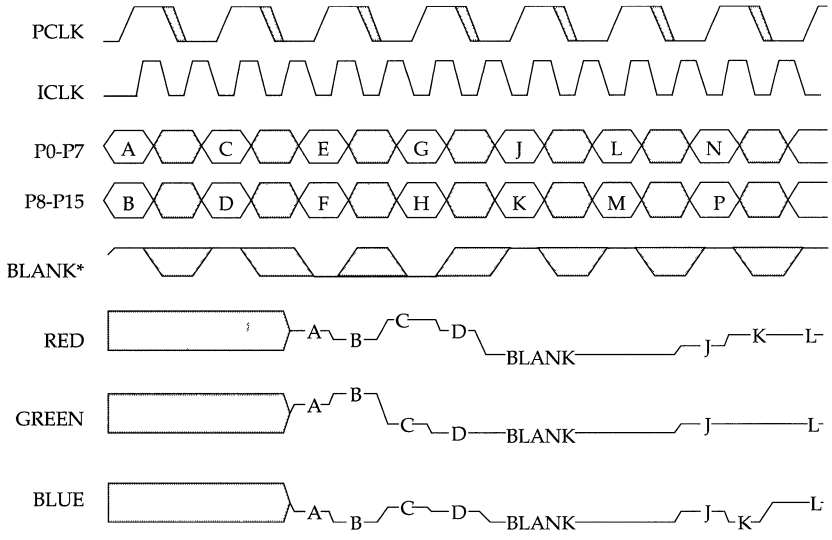
Detailed Timing Specifications - Pseudo Color, Mode 0



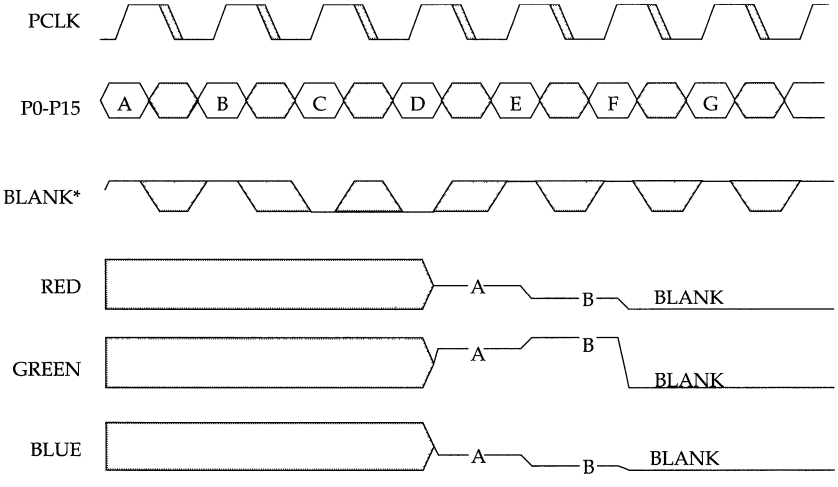
System Timing Bypass - 15 (5/5/5) and 16 (5/6/5) Modes 1, 2



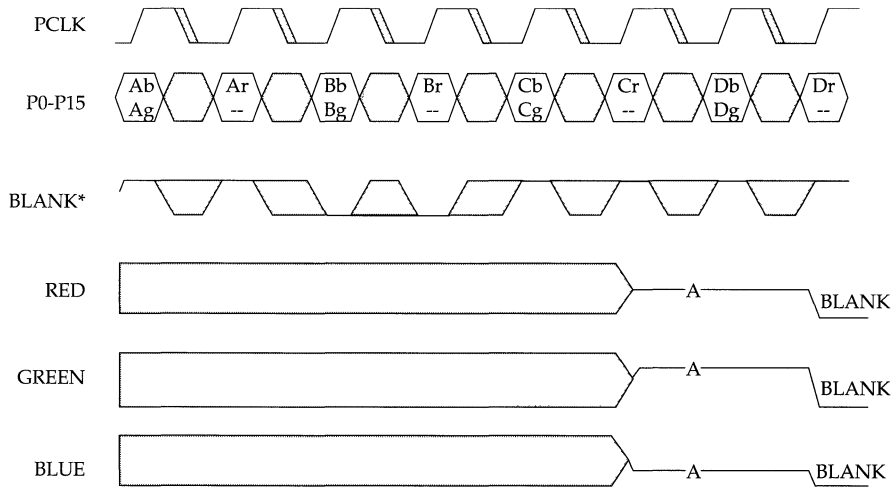
System Timing Bypass True Color 24 (8,8,8) Mode 3



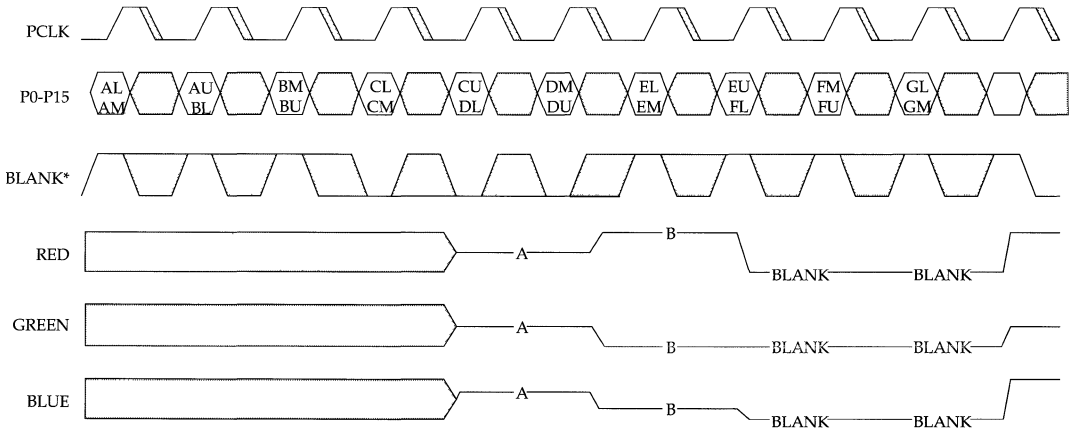
System Timing - Multiplexed 8-bit Pseudo Color, Mode 4



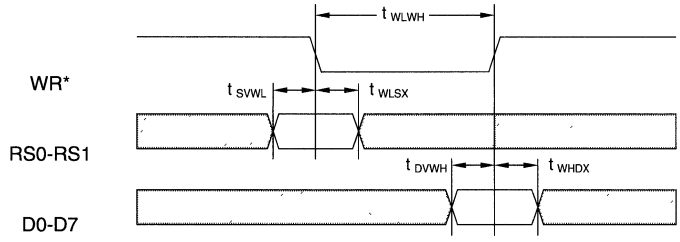
System Timing - 16-bit Color, Mode 5 (5,5,5) and 6 (5,6,5)



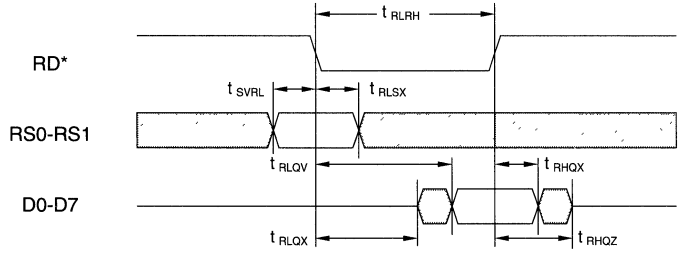
System Timing - 16-bit Direct True Color, Mode 7



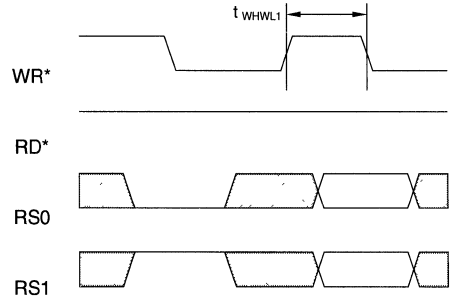
System Timing - 24-bit Packed Color, Mode 8



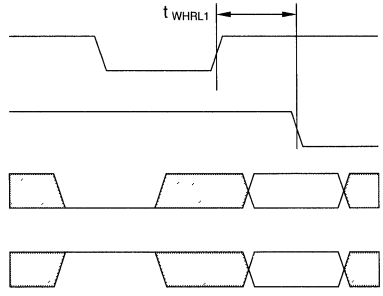
Basic Write Cycle Timing



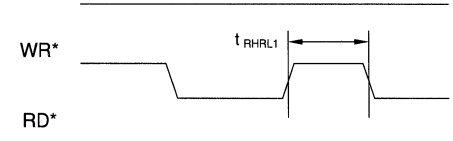
Basic Read Cycle Timing



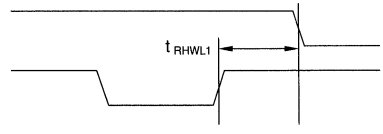
Write to Pixel Mask Register Followed by Write



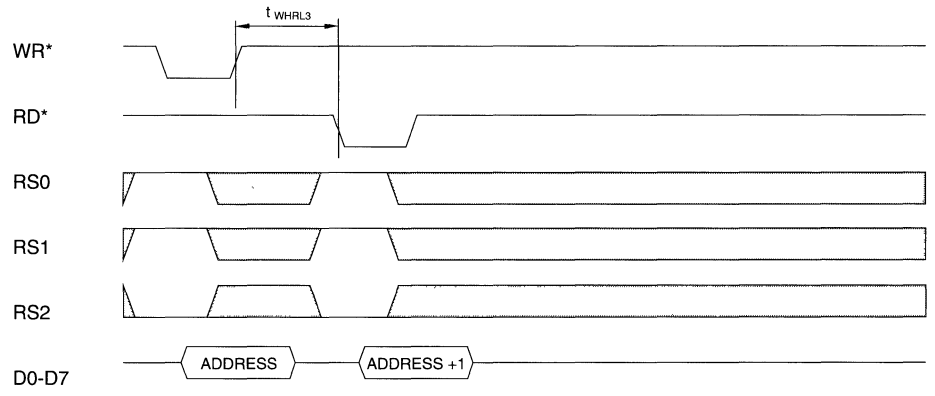
Write to Pixel Mask Register Followed by Read



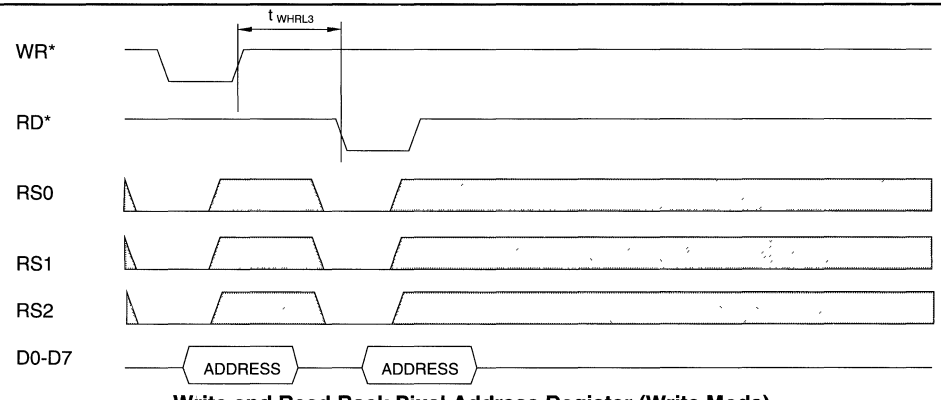
Read from Pixel or Pixel Address Register (Read or Write) followed by Read



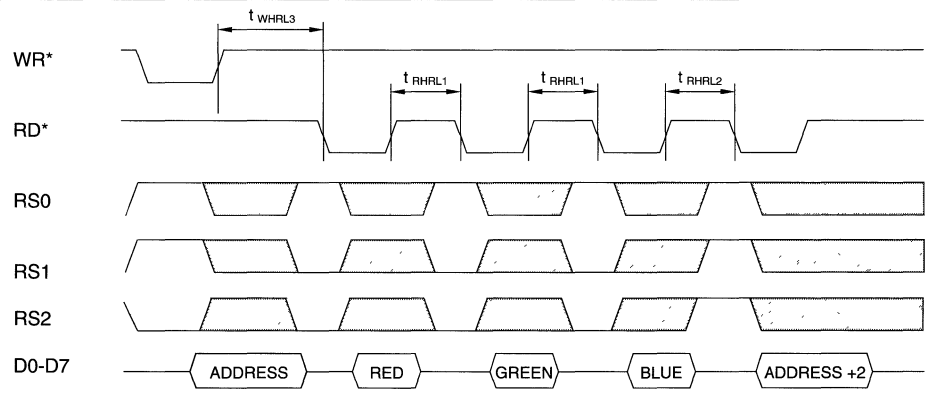
Read from Pixel or Pixel Address Register (Read or Write) followed by Write



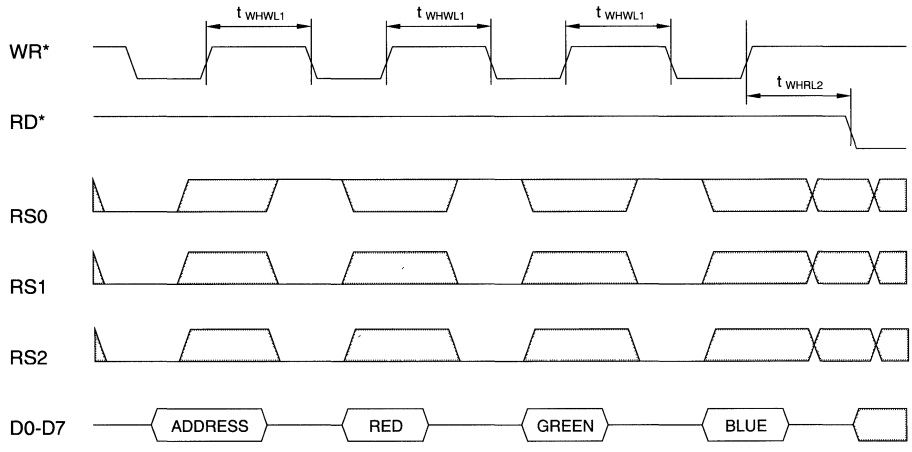
Write and Read Back Pixel Address Register (Read Mode)



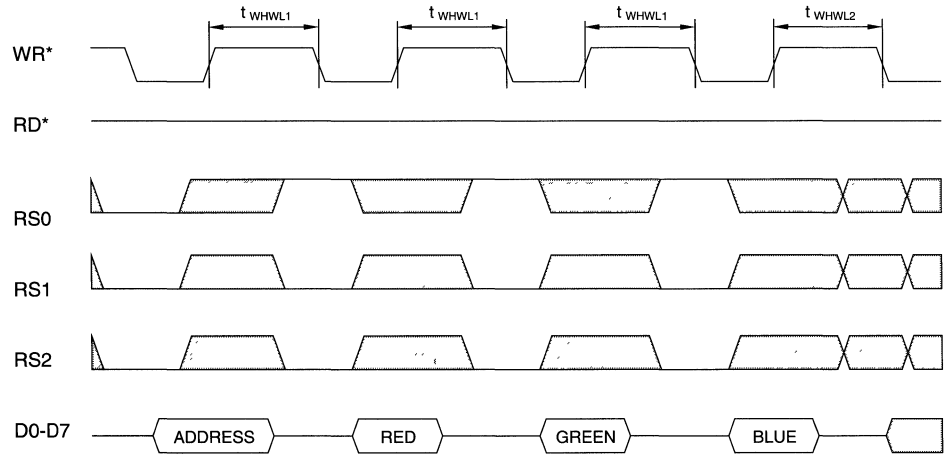
Write and Read Back Pixel Address Register (Write Mode)



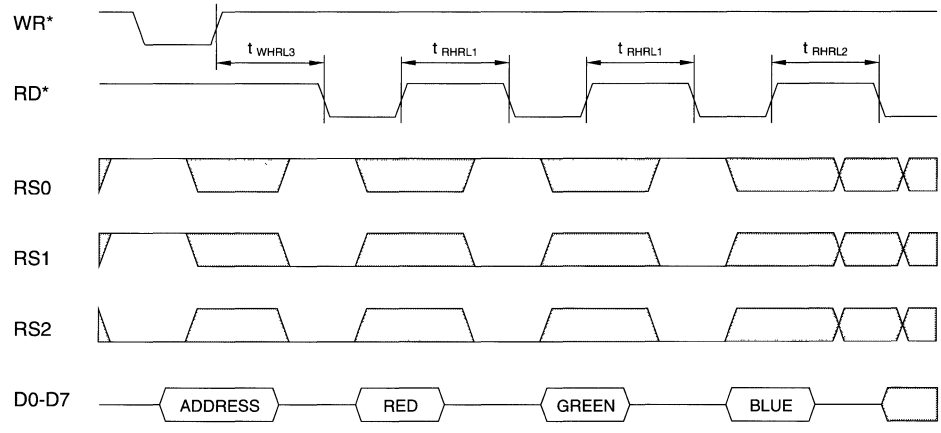
Read Color Value then Pixel Address Register (Read Mode)



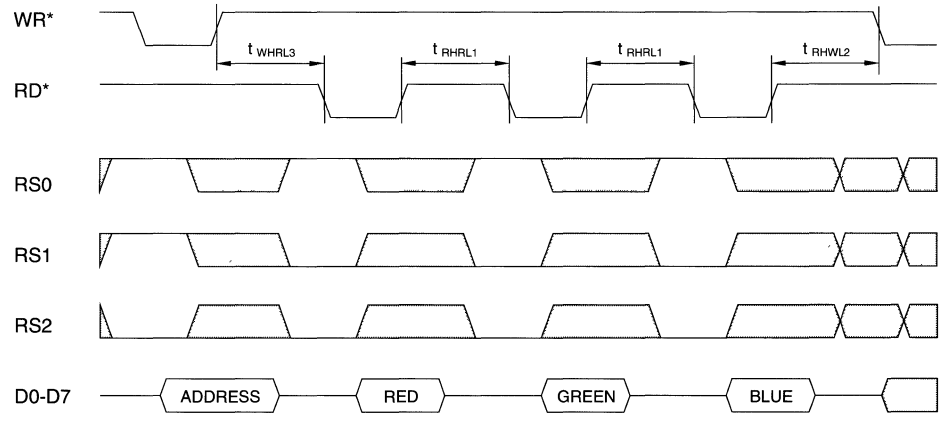
Color Value Write followed by any Read



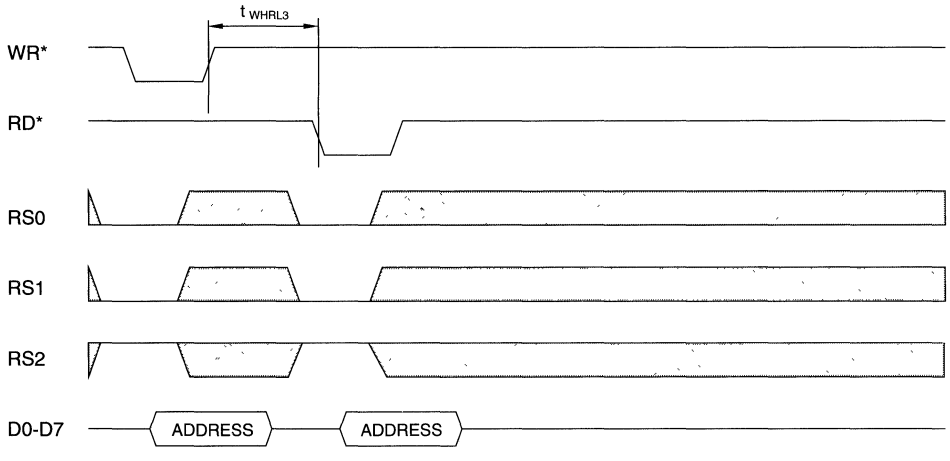
Color Value Write followed by any Write



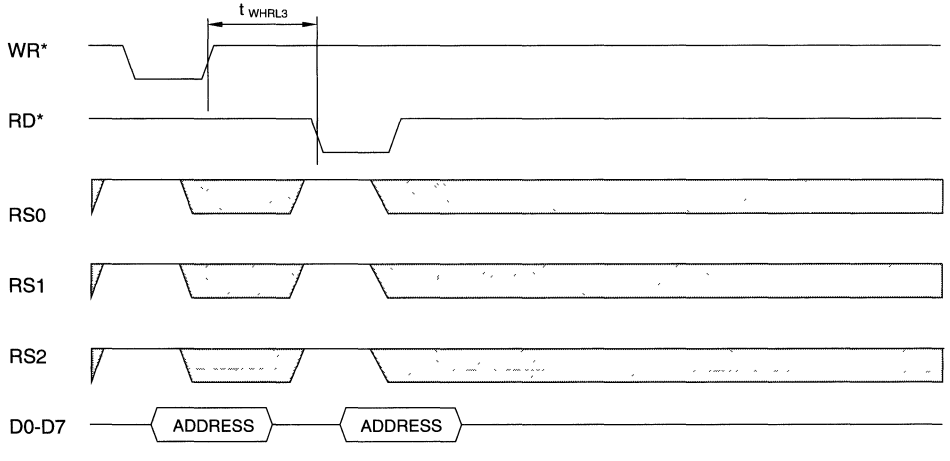
Color Value Read followed by any Read



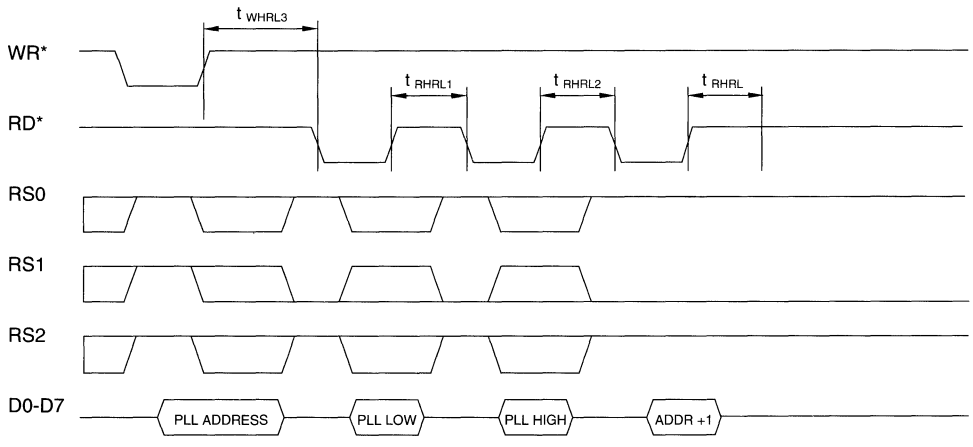
Color Value Read followed by any Write



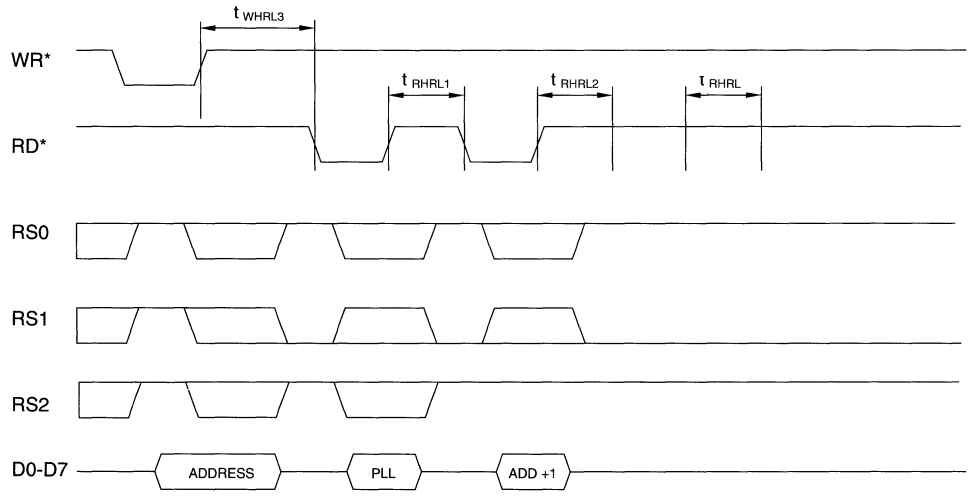
Write and Read back PLL Address Register (Write Mode)



Write and Read back PLL Address Register (Read Mode)

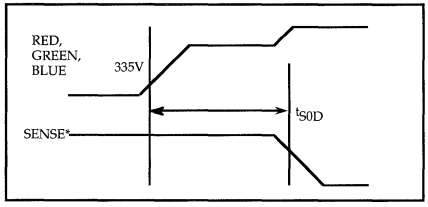


Read Two bytes PLL Register then PLL Address Register



Read One Byte PLL Register then PLL Address Register

Monitor SENSE Signal

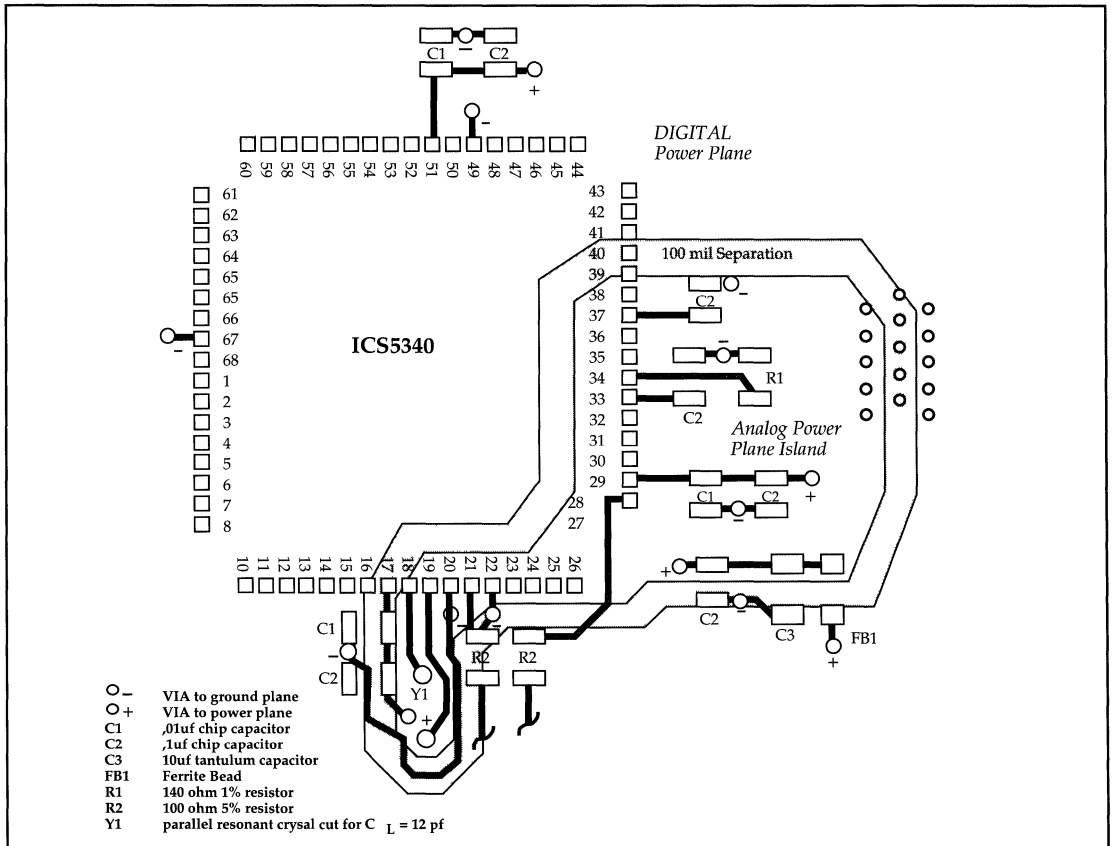


The high performance of which the ICS5340 GENDAC is capable is dependent on careful PC board layout. The use of a four layer board (internal power and ground planes, signals on the two surface layers) is recommended. The layout below shows a suggested configuration.

The ground plane is continuous, but the power plane is separated into analog and digital sections as shown. Power is supplied to the analog power plane through the ferrite bead, and bypassed at the power entry point by C3, a 10 µF tantalum capacitor. These high current connections should have multiple vias to the ground and power planes, if possible Power connections should be connected to the analog or digital power plane, as shown in the diagram Power pins 5 and 29 should be connected to digital power, power pins 20 and 24 to analog power. Decoupling capacitors (indicated by C1 and C2) should be placed as close to the GENDAC as possible.

The analog and digital I/O lines are not shown. Analog signals (DAC outputs, Vref, Rset) should only be routed above the analog power plane Digital signals should only be routed above the digital power plane.

Recommended Layout



Integrated Circuit Systems, Inc.

ICS5341 GENDAC

Advance Information

16-Bit Integrated Clock-LUT-DAC

General Description

The ICS5341 GENDAC is a combination of dual programmable clock generators, a 256 x 18-bit RAM, and a triple 8-bit video DAC. The GENDAC supports 8-bit pseudo color applications, as well as 15-bit, 16-bit and 24-bit True Color bypass for high speed, direct access to the DACs.

The RAM makes it possible to display 256 colors selected from a possible 262,144 colors. The dual clock generators use Phase Locked Loop (PLL) technology to provide programmable frequencies for use in the graphics subsystem. The video clock contains 8 frequencies, 6 of which are programmable by the user. The memory clock has two programmable frequency locations.

The three 8-bit DACs on the ICS5341 are capable of driving singly or doubly-terminated 75Ω loads to nominal 0 - 0.7 volts at pixel rates up to 135 MHz. Differential and integral linearity errors are less than 1 LSB over full temperature and V_{DD} ranges. Monotonicity is guaranteed by design. On-chip pixel mask register allows displayed colors to be changed in a single write cycle rather than by modifying the color palette.

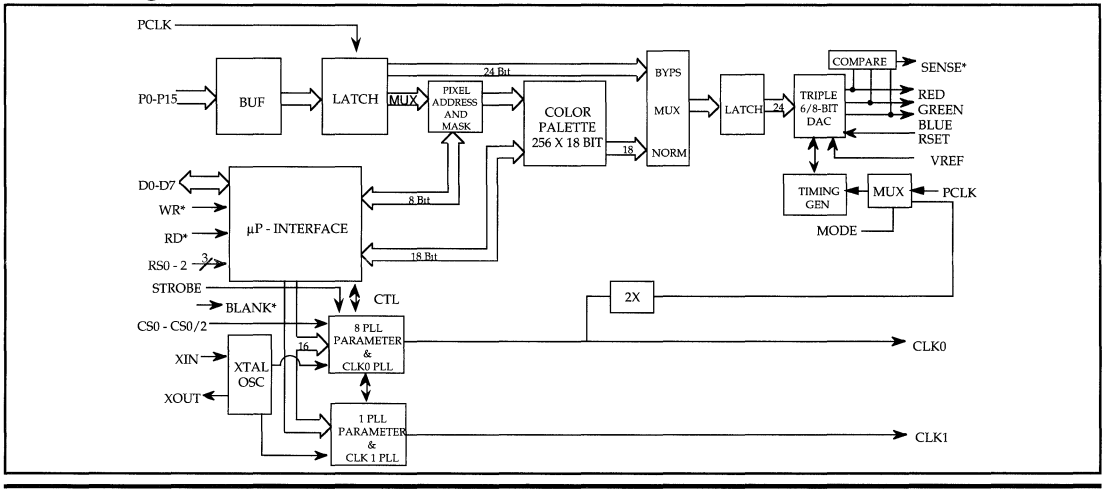
ICS is the world leader in all aspects of frequency (clock) generation for graphics, using patented techniques to produce low jitter video timing.

Features

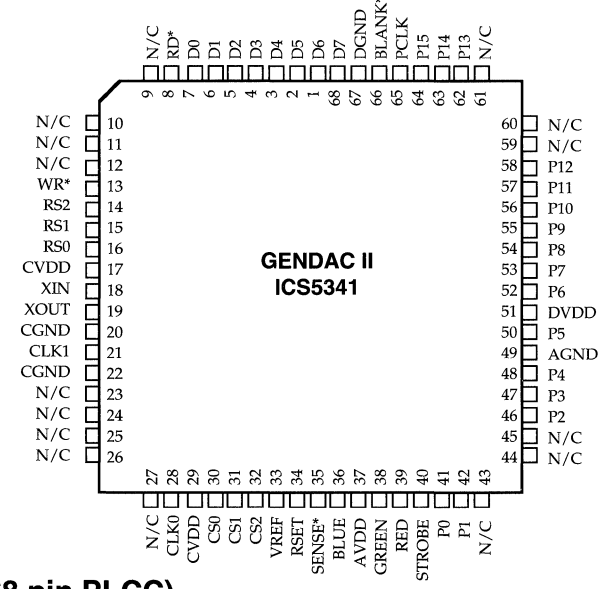
- **Designed for compatibility with Tseng Labs VGA controllers**
- **Triple video DAC, dual clock generator, and a color palette**
- **24, 16, 15, or 8-bit pseudo color pixel mode supports True Color, Hi-Color, and VGA modes**
- **High speed 256 x 18 color palette (135 MHz) with bypass mode and 8-bit DACs**
- **Two fixed, six programmable video (pixel) clock frequencies (CLK0)**
- **Two programmable memory (controller) clock frequency (CLK1)**
- **DAC power down in blanking mode**
- **Anti-sparkle circuitry**
- **On-chip loop filters reduce external components**
- **Standard CPU interface**
- **Single external crystal (typically 14.318 MHz)**
- **Monitor Sense**
- **Internal voltage reference**
- **135 MHz (-3), 110 MHz (-2) & 80 MHz (-1) versions**
- **Very low clock jitter**
- **Latched frequency control pin**

C

Block Diagram



Pin Configuration



Rev 1.0

Pin Description (68 pin PLCC)

Symbol	Pin #	Type	Description
D7 - D0	68, 1 - 7	I/O	System data bus I/O. These bidirectional Data I/O lines are used by the host microprocessor to write (using active low WR*) information into, and read (using active low RD*) information from the six internal registers (Pixel Address, Color Value, Pixel Mask, PLL Address, PLL Parameter, and Command). During the write cycle, the rising edge of WR* latches the data into the selected register (set by the status of the three RS pins). The rising edge of RD* determines the end of the read cycle. When RD* is a logical high, the Data I/O lines no longer contain information from the selected register and will go into a tri-state mode.
RD*	8	Input	RAM/PLL Read Enable, active low. This is the READ bus control signal. When active, any information present on the internal data bus is available on the Data I/O lines, D0-D7.
WR*	13	Input	RAM/PLL Write Enable, active low. This signal controls the timing of the write operation on the microprocessor interface inputs, D0-D7.
RS2 RS1 RS0	14 15 16	Input Input Input	Register Address Select 0. These inputs control the selection of one of the six internal registers. They are sampled on the falling edge of the active enable signal (RD* or WR*).
CVDD	17	-	Crystal oscillator and CLK0 power supply connect to AVDD.
XIN	18	Input	Crystal input. A 14.318 MHz crystal should be connected to this pin.
XOUT	19	Output	Crystal output. A 14.318 MHz crystal should be connected to this pin.
CGND	20	-	VSS for CLK0. Connect to ground.

Pin Description (continued)

Symbol	Pin #	Type	Description
CLK1	21	Output	Memory clock output. Used to time the video memory.
CGND	22	-	VSS for CLK1. Connect to ground.
CLK0	28	Output	Video clock output. Provides a CMOS level pixel or dot clock frequency to the graphics controller. The output frequency is determined by the values of the PLL registers.
CVDD	29	-	CLK1 Power Supply. Connect to AVDD.
CS0	30	Input	Clock select 0. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output. Latched by STB.
CS1	31	Input	Clock select 1. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output. Latched by STB.
CS2	32	Input	Clock select 2. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output. Latched by STB.
VREF	33	I/O	Internal Reference Voltage. Normally connects to a 0.1µ cap to ground. To use an external Vref, connect a 1.235V reference to this pin.
RSET	34	Input	Resistor Set. This pin is used to set the current level in the analog outputs. It is usually connected through a 140Ω, 1% resistor to ground.
SENSE*	35	Output	Monitor Sense, active low. This pin is low when any of the red, green, or blue outputs have exceeded 335mV. The chip has on-board comparators and an internal 335mV voltage reference. This is used to detect monitor type.
AVDD	37	-	DAC power supply. Connect to AVDD.
BLUE GREEN RED	36 38 39	Output Output Output	Color Signals. These three signals are the DACs' analog outputs. Each DAC is composed of several current sources. The outputs of each of the sources are added together according to the applied binary value. These outputs are typically used to drive a CRT monitor.
STROBE	40	Input	Latches the input clock select signals CS0 - CS2.
P0 - P15	41- 42 46-48, 50	Input	Pixel Address Lines. This byte-wide information is latched by the rising edge of PCLK when using the Color Palette, and is masked by the Pixel Mask register. These values are used to specify the RAM word address in the default mode (accessing RAM). In the Hi-Color XGA, and True Color modes, they represent color data for the DACs. These inputs should be grounded if they are not used.
AGND	49	-	DAC Ground. Connect to ground.
DVDD	51	-	Digital power supply.
PCLK	65 52-58, 62-64	Input	Pixel Clock. The rising edge of PCLK controls the latching of the Pixel Address and BLANK* inputs. This clock also controls the progress of these values through the three-stage pipeline of the Color Palette RAM, DAC, and outputs.
BLANK*	66	Input	Composite BLANK* Signal, active low. When BLANK* is asserted, the outputs of the DACs are zero and the screen becomes black. The DACs are automatically powered down to save current during blanking. The color palette may still be updated through D0-D7 during blanking.
DGND	67	-	Digital Ground. Connect to ground.

C

ICS

Motherboard Timing Generator

Products

D

In this latest issue of the data book, ICS continues to lead the market by offering the industry's widest selection of advanced motherboard and CPU clock generators found anywhere. New products include designs to address a wide variety of uses, including disk drive, modem, and Pentium™ CPU clocking applications. This is all in addition to the widest choice of advanced desktop and laptop motherboard and CPU systems clock generators in the industry.

As a market oriented company, ICS designs products with and for you, our customers, and we welcome inquiries concerning new product ideas for any of the above applications.

ICS Timing Generator Selection Guide

Motherboard Clock Products

Product Application	ICS Device Type	Features	Number of Outputs	Number of PLL's	Package Types	Page
Motherboard	ICS2407 ICS2409 ICS2439	IMI407, IMI409 and IMI439 Compatible.	6 9 9	2 2 2	18 Pin DIP, SOIC 24 Pin DIP, SSOP 24 Pin DIP, SSOP	369
	ICS2492	Buffered XTAL Out. Tristate PLL Outputs.	3	2	20 Pin DIP, SOIC	375
	ICS2494-244 ICS2494A-317	Buffered XTAL Out. Note: See Video Dot Clock Section for Data.	3	2	20 Pin DIP, SOIC	161
	ICS2694	9 Fixed, CPU-CPU/2 Selectable Provides CPU, Co-Processor, Hard and Floppy Disk, Kbd, Ser. Port, Bus Clk. Function.	11	2	24 Pin DIP, SOIC	381
	AV9107	CPU Clock Generator.	2	1	8 or 14 Pin DIP, SOIC	387
	ICS9108	3 Volt CPU Clock Generator.	2	1	8 or 14 Pin DIP, SOIC	395
	AV9128/9	Motherboard Frequency Generator Outputs Kbd Clock, Systems Clock, I/O Clock, Comm. Clock and CPU Clock.	8/11	4	16 or 20 Pin DIP, SOIC	403
	ICS9131	32 kHz Input Generates CPU Clocks.	3	2	16 Pin DIP, PDIP	417
	ICS9132	32 kHz Input Generates all Motherboard Clocks.	6	4	20 Pin DIP, SOIC	425
	ICS9133	32 kHz Input Generates CPU Clock and System Clock and Two Fixed Clocks.	6	3	20 Pin SOIC, PDIP	435
	AV9140	R4000 Processor Series Master Clock Generator.	1	1	8 Pin DIP, SOIC	441
	AV9154	Low Cost 16 Pin Clock Generator. Generates CPU Clock, Keyboard Clock, System Clock and I/O Clock.	7	2	16 Pin DIP, SOIC	445
	AV9155	Motherboard Clock Generator. Produces CPU Clock, Keyboard Clock, System Clock and I/O Clock	8	2	20 Pin DIP, SOIC	461
	ICS9158	Clock Generator with Integrated Buffers.	11	2	24 Pin SOIC	473
Laptop/ Notebook	ICS2496-456	3Volt Operation, Buffered XTAL Out. Note: See Video Dot Clock Section for Data.	3	2	20 Pin DIP, SOIC	173
	AV9154-06/60	Clock Generator Designed Specifically for use with OPTI Chipset.	4	2	16 Pin DIP, SOIC	455

ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. ICS reserves the right to change or discontinue these products without notice.

Integrated
Circuit
Systems, Inc.

ICS2407
ICS2409
ICS2439
Product Preview

Dual-PLL Motherboard Frequency Generator

Description

This ICS family of motherboard frequency generators all stem from the same basic design. They are dual-PLL (phase-locked loop) clock generators specifically designed for motherboard applications. Metal layer and assembly options are used to generate the three separate device types in order to optimize the functionality for specific applications. All frequencies are synthesized from a single reference clock which may be generated by the on-chip crystal oscillator or an external reference clock.

The CPU clock PLL is ROM-programmed to generate any of seven customer specified frequencies through selection of the address lines **SCLK0-SCLK2**. *In the **ICS2409** and **ICS2439** versions the **SCLK3** input selects those frequencies directly or divided by two for the **CPUX2** output.* The **CPUX2** output is then divided by two to generate the **CPUCLK** output. A power-down mode may be selected with the **SCLK** inputs to reduce standby current consumption to a few microamperes.

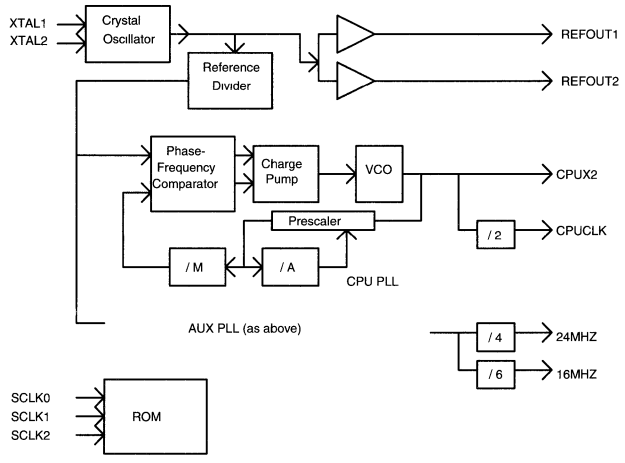
The auxiliary (AUX) PLL generates the fixed frequencies shown in Table 1 for other system uses. A buffered reference frequency output is available on the **REFOUT** pin. Two non-dedicated buffers are provided on the **ICS2439** and **ICS2409** for additional drive capability without adding external buffers and their board space.

Features

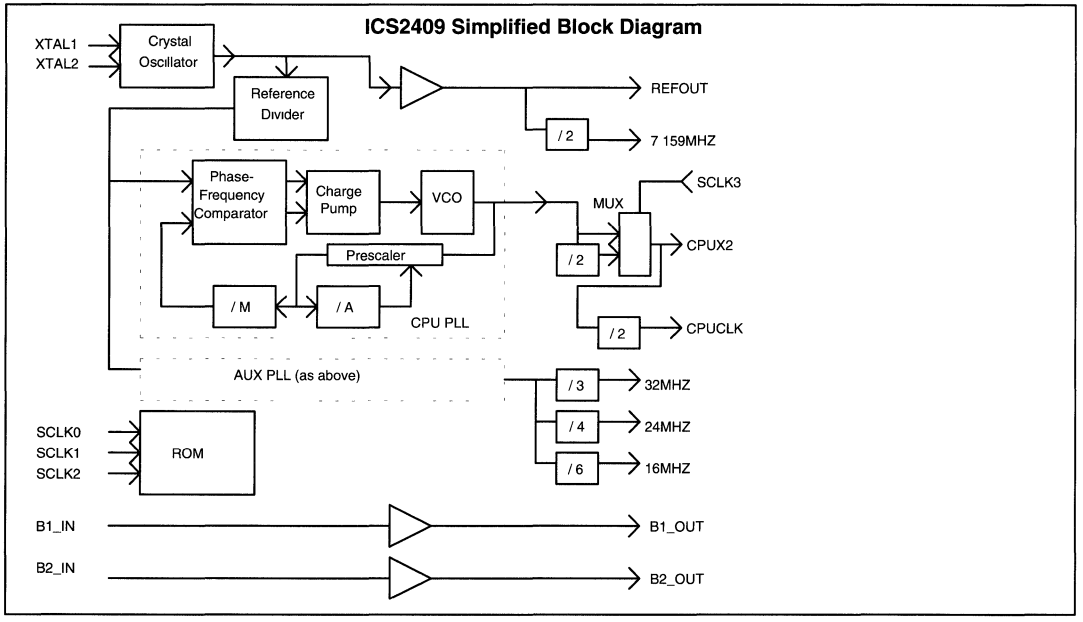
- Supports 286, 386, & 486 desktop and notebook motherboard designs
- Advanced ICS monolithic phase-locked loop technology for low short-term and "cumulative" jitter
- Completely integrated - no external loop filter capacitors required
- Dual-modulus prescaler permits high-speed operation with no sacrifice in accuracy
- Power-down mode for low standby power consumption
- Low-skew between **CPUX2** and **CPUCLK** outputs (< 1 nsec)
- 3-volt supply capability to 85 MHz (**CPUX2** output)
- Output enable (**OE~**) pin for tri-state of device outputs
- **ICS2409** and **ICS2439** offer 24-pin PDIP (0.3") and 24-pin SSOP (5.3mm) package options
- **ICS2407** offers 18-pin PDIP (0.3") and 18-pin SOIC (0.3") package options

D

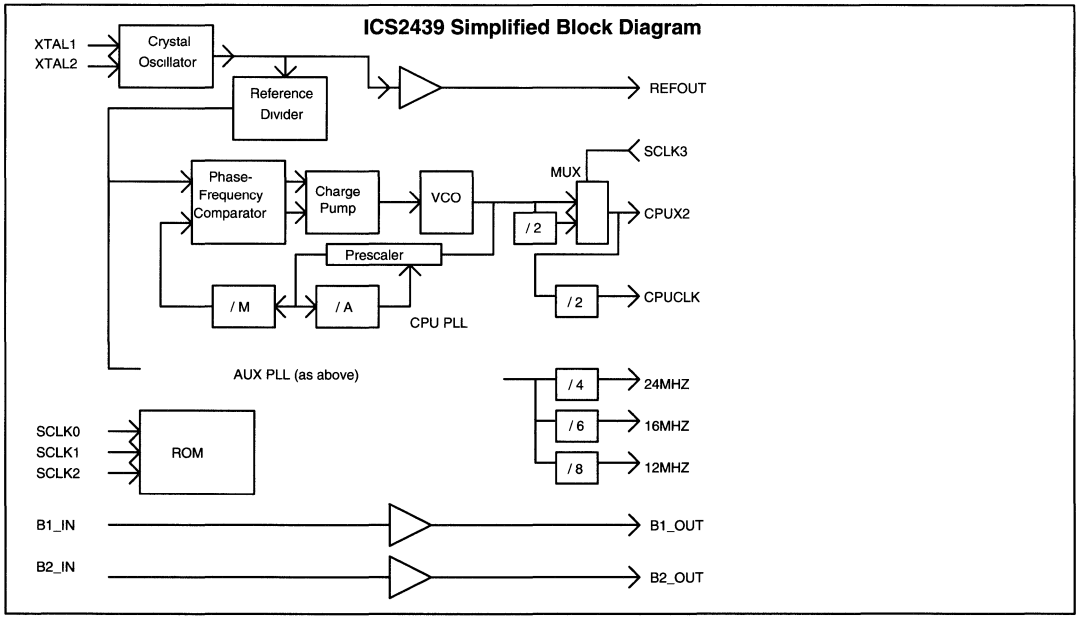
ICS2407 Simplified Block Diagram



ICS2409 Simplified Block Diagram



ICS2439 Simplified Block Diagram



Circuit Function and Application

Fixed Frequencies

The ICS motherboard family supplies "fixed" frequencies normally used to provide several system functions:

- 32 MHz - ISA Bus Clock
- 24 MHz - Floppy Drives
- 16 MHz - AT Bus Clock Output
- 12 MHz - Keyboard Clock
- 7.149 MHz - Keyboard Clock

Selectable CPU Clock Frequencies

The **ICS2407**, **ICS2409** and **ICS2439** are designed to generate CPU clock options ranging from 24MHz, to 88MHz. For added flexibility, the **ICS2409** and **ICS2439** allow the user to select each of these frequencies divided by 2.

Buffered Output Pins

In addition, the **ICS2409** and **ICS2439** provide 2 non-dedicated buffers for additional flexibility. This allows for extra drive capability without sacrificing the extra board space required for external buffers.

Buffered XTALOUT

In motherboard applications it may be desirable to have the **ICS2439** provide the bus clock for the rest of the system. This eliminates the need for an additional 14.31818 MHz crystal oscillator on the system, saving money as well as board space. Depending on the load, it may be judicious to buffer REFOUT when using it to provide the system clock. On the **ICS2407**, there are two identical outputs, REFOUT1 and REFOUT2.

Power-Down Mode

All three devices have been optimized for use in battery operated portables. It can be placed in a powerdown mode which drops its supply current requirement below 1µA (typical).

Pin Description

Input Pins

Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate crystal should be connected between XTAL1 (1) and XTAL2 (2). In IBM compatible applications this will typically be a 14.31818 MHz crystal.

Digital Inputs

SCLK0, SCLK1, SCLK2 and SCLK3 *(**ICS2409**, **ICS2439** only)* are the TTL compatible frequency select inputs for the binary code corresponding to the desired frequency. All select pins have internal pull-up devices built in *(See Table 2 for a complete list of available frequencies)*.

*Buffer Inputs (**ICS2409** & **ICS2439**)*

B1_IN and B2_IN (3, 7) provide additional buffering needed on a typical board design without the added cost of external components.

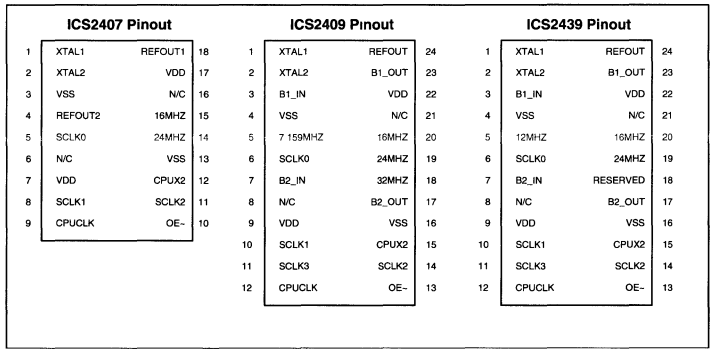
Output Enable

An output enable pin OE~ allows the user to tri-state the device outputs. When this pin is high, all outputs are in tri-state mode. When low, all outputs are enabled. This pin has an internal pull-down to enable all outputs when the pin is N/C.

Ordering Information

ICSXXXXM (SO Package)
ICSXXXXN (DIP Package)
ICSXXXXF (SSOP Package)

(XXX = Pattern number)



Absolute Maximum Ratings

Supply Voltage ..... V_{DD} ..... -0.5V to + 7V
Input Voltage ..... V_{IN} ..... -0.5V to V_{DD} + 0.5V
Output Voltage ..... V_{OUT} ..... -0.5V to V_{DD} + 0.5V
Clamp Diode Current ..... V_{IK} & I_{OK} ..... ± 30mA
Output Current per Pin ..... I_{OUT} ..... ± 50mA
Operating Temperature ..... T_O ..... 0°C to 70°
Storage temperature ..... T_S ..... -85°C to 150°
Power Dissipation ..... P_D 500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than themaximum rated voltages. For proper operation it is recommended that Vin and Vout be constrained to > = V_{SS} and < = V_{DD}.

DC Characteristics at 5 Volts V_{DD}

(0°C to + 70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Operating Voltage Range	V_{DD}		4.5	5.5	V
Input Low Voltage	V_{IL}	V_{DD}= 5V	V_{SS}	0.8	V
Input High Voltage	V_{IH}	V_{DD}= 5V	2.0	V_{DD}	V
Input Leakage Current	I_{IH}	V_{IN}= V_{DD}	-	10	µA
Output Low Voltage	V_{OL}	I_{OL}= 1.20mA	-	0.4	V
Output High Voltage	V_{OH}	I_{OH}= 1.20mA	2.4	0	V
Supply Current	I_{DD}	VCLK= 40MHz	-	40	mA
Supply Current	I_{DD}	VCLK= 88MHz	-	50	mA
Internal Pullup Current	R_{UP}	V_{IN}= 0.0V	30	100	µA
Internal Pulldown Current	R_{DOWN}	V_{IN}= 0.0V	30	100	µA
Input Pin Capacitance	C_{IN}	F_C= 1MHz	-	8	pF
Output Pin Capacitance	C_{OUT}	F_C= 1MHz	-	12	pF
Powerdown Supply Currrent	I_{PN}	V_{DD}= 3.3V	-	1	µA

DC Characteristics at 3.3 Volts V_{DD}

(0°C to + 70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Operating Voltage Range	V_{DD}		3.0	3.6	V
Input Low Voltage	V_{IL}	V_{DD}= 3.3V	V_{SS}	0.8	V
Input High Voltage	V_{IH}	V_{DD}= 3.3V	2.0	V_{DD}	V
Input Leakage Current	I_{IH}	V_{IN}= V_{DD}	-	10	µA
Output Low Voltage	V_{OL}	I_{OL}= 8.0mA	-	0.4	V
Output High Voltage	V_{OH}	I_{OH}= 8.0mA	2.4	0	V
Supply Current	I_{DD}	CPUX2= 40MHz	-	35	mA
Supply Current	I_{DD}	CPUX2= 88MHz	-	25	mA
Internal Pullup Current	R_{UP}	V_{IN}= 0.0V	20	70	µA
Internal Pulldown Current	R_{DOWN}	V_{IN}= 0.0V	20	70	µA
Input Pin Capacitance	C_{IN}	F_C= 1MHz	-	8	pF
Output Pin Capacitance	C_{OUT}	F_C= 1MHz	-	12	pF
Powerdown Supply Currrent	I_{PN}	V_{DD}= 3.3V	-	1	µA

D

AC Timing Characteristics

The following notes apply to all of the parameters presented in this section.
1. REFCLK = 14.31818 MHz
2. $t_c = 1/f_c$
3. All units are in nanoseconds (ns)
4. Rise and fall time between .8 and 2.0 VDX unless otherwise stated.
5. Output pin loading = 15pF
6. Duty cycle measured at $V_{DD}/2$ unless otherwise stated

SYMBOL	PARAMETER	MIN	MAX	NOTES
	OUTPUT TIMING @5v			
Tr	Rise Time	-	2	
Tf	Fall Time	-	2	
-	Frequency Error	-	0.5	%
Tak	Clock Skew (CPUCLK & CPUX2)	-	1.0	nSec
-	Duty Cycle	45	55	%
-	Output Enable to Tri-State (into and out of) time	-	15	nSec
	OUTPUT TIMING @3.3v			
Tr	Rise Time	-	3	
Tf	Fall Time	-	3	
-	Frequency Error	-	0.5	%
Tak	Clock Skew (CPUCLK & CPUX2)	-	1.5	nSec
-	Duty Cycle	45	55	%
-	Output Enable to Tri-State (into and out of) time	-	20	nSec

Table 1: Fixed Output Frequencies

ICS2439	ICS2409	ICS2407
24 MHz	32 MHz	24 MHz
16 MHz	24 MHz	16 MHz
12 MHz	16 MHz	
	7.159 MHz	

Table 2: CPU Clock Frequency Selection

SCLK3	SCLK2	SCLK1	SCLK0	ICS2439 Pattern 001	ICS2409 Pattern 001	ICS2407 Pattern 407
0	0	0	0	12 MHz	12 MHz	12 MHz
0	0	0	1	16	16	16
0	0	1	0	20	20	20
0	0	1	1	25	25	25
0	1	0	0	33.33	33.33	33.33
0	1	0	1	40	40	40
0	1	1	0	30	44	44
0	1	1	1	PowerDown	PowerDown	PowerDown
1	0	0	0	24	24	
1	0	0	1	32	32	
1	0	1	0	40	40	
1	0	1	1	50	50	
1	1	0	0	66.66	66.66	
1	1	0	1	80	80	
1	1	1	0	60	88	
1	1	1	1	TEST	TEST	

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development Characteristic data and other specifications are design goals ICS reserves the right to change or discontinue these products without notice

CPU Clock Generator

Features

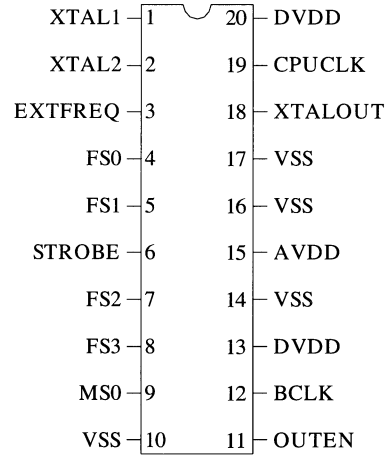
- Low cost - eliminates need for multiple crystal clock oscillators in motherboard applications
- Mask-programmable frequencies
- Pre-programmed versions for a selection of CPU clocks
- Glitch-free frequency transitions
- Provision for external frequency input
- Internal clock remains locked when the external frequency input is selected
- Low power CMOS device technology
- Small footprint - 20 pin DIP or SO
- Buffered Xtal Out
- Integral Loop Filter components
- Fast acquisition of selected frequencies, strobed or non-strobed
- Guaranteed performance up to 135 MHz
- Excellent power supply rejection
- Advanced PLL for low phase-jitter
- Output Enable function for tristate control of the two clock outputs.

Description

The **ICS2492** CPU Clock Generator is an integrated circuit dual phase locked loop frequency synthesizer capable of generating 16 CPU frequencies and two other clock frequencies for use with high performance personal computer motherboards. Utilizing CMOS technology to implement all linear, digital and memory functions, the **ICS2492** provides a low-power, small footprint, low-cost solution to the generation of CPU clocks. Provision is made via a single level custom mask to implement customer-specific frequency sets. Phase-locked loop circuitry permits rapid glitch-free transitions between clock frequencies.

The **ICS2492** is fully pin and function compatible with ICS' industry-standard ICS2494 dual clock generator except that an output enable function has been added to pin 11. A pre-programmed version with a full selection of CPU clocks is available as part number **ICS2492-453**. The frequencies in this pattern are essentially identical to those in the ICS2494-244 standard pattern.

Pin Configuration



Notes:

1. In applications where the external frequency input is not specified, EXTFREQ must be tied to V_{SS}.
2. ICS2492M(SO) pinout is identical to ICS2492N(DIP).

Circuit and Application Options

The **ICS2492** will typically derive its frequency reference from a series-resonant crystal connected between pins 1 and 2. Where a high quality reference signal is available, such as in an application where the graphics subsystem is resident on the motherboard, this reference may directly replace the crystal. This signal should be coupled to pin 1. If the reference signal amplitude is less than 3.5 volts, a .047 microfarad capacitor should be used to couple the reference signal into **XTAL1**. Pin 2 must be left open.

The **ICS2492** is capable of multiplexing an externally generated frequency source of **VCLK** via a mask option, in addition to its internally-generated clock.

This is input via **EXTFREQ (3)**. When an external source is selected, the PLL remains locked to the value specified in the selected address. This provision facilitates the ability to rapidly change frequencies. When this option is not specified in the ROM pattern, pin 3 is internally tied to V_{SS} and should be connected to V_{SS} on the PCB.

Power Supply Conditioning

The **ICS2492** is a member of the second generation of dot clock products. By incorporating the loop filter on chip and upgrading the VCO, the ease of application has been substantially improved over earlier products. If a stable and noise-free power supply is available, no external components are required. However, in most applications it is judicious to decouple the power supply as shown in Figures 1 or 2. Figure 1 is the normal configuration for 5 Volt only applications. Which of the two provides superior performance depends on the noise content of the power supplies. In general, the configuration of Figure 1 is satisfactory. Figure 2 is the more conventional if a 12 Volt analog supply is available, although the improved performance comes at a cost of an extra component; however, the cost of the discretes used in Figure 2 is less than the cost of Figure 1's discrete components.

The number and differentiation of the analog and digital supply pins are intended for maximum performance products. In most applications, all V_{DDS} may be tied together. The function of the multiple pins is to allow the user to realize the maximum performance from the silicon with a minimum degradation due to the package and PCB. At the frequencies of interest, the effects of the inductance of the bond wires and package lead frame are non-trivial. By using the multiple pins, ICS has minimized the effect of packaging and has minimized the interaction of the digital and analog supply currents.

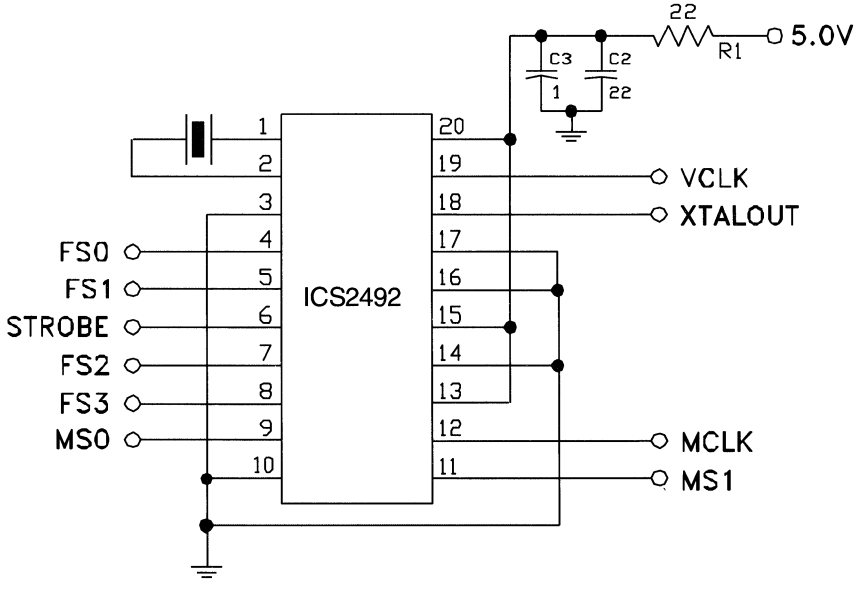


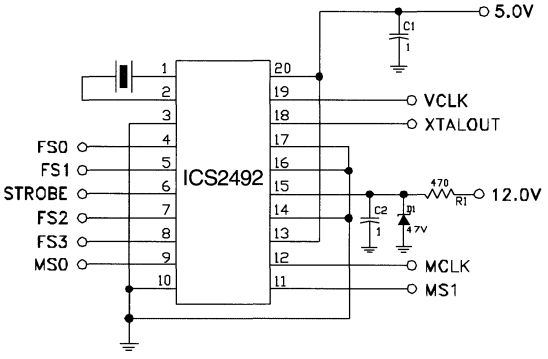
Figure 1

Applications

Layout Considerations

Utilizing the **ICS2492** in video graphics adapter cards or on PS2 motherboards is simple, but does require precautions in board layout if satisfactory jitter-free performance is to be realized. Care should be exercised in ensuring that components not related to the **ICS2492** do not share its ground. In applications utilizing a multi-layer board, V_{SS} should be directly connected to the ground plane. Multiple pins are utilized for all analog and digital Vss and Vdd connections to permit extended frequency **VCLK** operation to 135 MHz. However, in all cases, all V_{SS} and V_{DD} pins should be connected.

Figure 2



Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate series-resonant crystal should be connected between **XTAL1 (1)** and **XTAL2 (2)**. In IBM-compatible applications this will typically be a 14.31818 MHz crystal, but fundamental mode crystals between 10MHz and 25MHz have been tested. Maintain short lead lengths between the crystal and the **ICS2492**. In some applications, it may be desirable to utilize the bus clock. If the signal amplitude is equal to or greater than 3.5 volts, it may be connected directly to **XTAL1 (1)**. If the signal amplitude is less than 3.5 volts, connect the clock through a .047 microfarad capacitor to **XTAL1 (1)**, and keep the lead length of the capacitor to **XTAL1 (1)** to a minimum to reduce noise susceptibility. This input is internally biased at $V_{DD}/2$. Since TTL compatible clocks typically exhibit a V_{OH} of 3.5V, capacitively coupling the input restores noise immunity. The **ICS2492** is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of this signal is typically outside of the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. **XTAL2 (2)** must be left open in this configuration.

Buffered XTALOUT

In motherboard applications it may be desirable to have the **ICS2492** provide the bus clock for the rest of the system. This eliminates the need for an additional 14.31818 MHz crystal oscillator in the system, saving money as well as board space. To do this, the **XTALOUT (18)** output should be buffered with a CMOS driver.

Output Circuit Considerations

As the dot clock is usually the highest frequency present in a video graphics system, consideration should be given to EMI. To minimize problems with meeting FCC EMI requirements, the trace which connects **VCLK (19) or MCLK (12)** and other components in the system should be kept as short as possible. The **ICS2492** outputs have been designed to minimize overshoot. In addition, it may be helpful to place a ferrite bead in these signal paths to limit the propagation of high order harmonics of this signal. A suitable device would be a Ferroxcube 56-590-65/4B or equivalent. This device should be placed physically close to the **ICS2492**. A 33 to 47 Ohm series resistor, sometimes called source termination, in this path may be necessary to reduce ringing and reflection of the signal and may reduce phase-jitter as well as EMI.

External Frequency Sources

EXTFREQ (3) on versions so equipped by the programming, is an input to a digital multiplexer. When this input is enabled, signals driving the input will appear at **VCLK (19)** instead of the PLL output. Internally, the PLL will remain in lock at the frequency selected by the ROM code.

Digital Inputs

FS0 (4), FS1 (5), FS2 (7), and **FS3 (8)**, are the TTL compatible frequency select inputs for the binary code corresponding to the frequency desired. **STROBE (6),** when high, allows new data into the frequency select latches; and when low, prevents address changes per Figure 3. The internal power-on-clear signal will force an initial frequency code corresponding to an all-zeros input state. **MS0 (9)** and **MS1 (11)** are the corresponding memory select inputs and are not strobed.

Absolute Maximum Ratings

Supply Voltage . . . . . V_{DD} . . . . . -0.5V to + 7V
Input Voltage . . . . . V_{IN} . . . . . -0.5V to V_{DD}+ 0.5V
Output Voltage . . . . . V_{OUT} . . . . . -0.5V to VDD+ 0.5V
Clamp Diode Current . . . . V_{IK} & I_{OK} . . . . . + / -30mA
Output Current per Pin . . . I_{OUT} . . . . . + / -50mA
Operating Temperature . . . T_o . . . . . 0 °C to 70 °C
Storage Temperature . . . . . T_S . . . . . -85 °C to + 150 °C
Power Dissipation . . . . . P_D 500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to > = V_{SS} and < = V_{DD}

DC Characteristics (0 °C to 70 °C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{DD}	Operating Voltage Range	4.0	5.5	V	
V_{IL}	Input Low Voltage	V_{SS}	0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0	V_{DD}	V	V_{DD} = 5V
I_{IH}	Input Leakage Current	-	10	uA	V_{IN} = V_{cc}
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = 4.0 mA
I_{DD}	Supply Current	-	27	mA	V_{DD} = 5V, VCLK = 80 MHz
R_{UP} *	Internal Pullup Resistors	50	200	K Ohm	V_{dd} = 5V, V_{in} = 0V
C_{in}	Input Pin Capacitance	-	8	pF	F_c = 1 MHz
C_{out}	Output Pin Capacitance	-	12	pF	F_c = 1 MHz

* The following inputs have pullups: FS0-3, MS0-1, STROBE.

AC Timing Characteristics

The following notes apply to all parameters presented in this section:

1. Xtal Frequency = 14.31818 MHz
2. $T_C = 1/F_C$
3. All units are in nanoseconds (ns).
4. Rise and fall time is between 0.8 and 2.0 VDC.
5. Output pin loading = 25pF
6. Duty cycle is measured at 1.4V.
7. Supply Voltage Range = 4.0 to 5.5 Volts
8. Temperature Range = 0 °C to 70 °C

SYMBOL	PARAMETER	MIN	MAX	NOTES
	STROBE TIMING			
Tpw	Strobe Pulse Width	20	-	
Tsu	Setup Time Data to Strobe	10	-	
Thd	Hold Time Data to Strobe	10	-	
	MCLK AND VCLK TIMINGS			
Tr	Rise Time	-	3	Duty Cycle 40% min. to
Tf	Fall Time	-	3	60% max.
-	Frequency Error		0.5	%
-	Maximum Frequency		135	MHz
-	Propagation Delay for Pass Through Frequency	-	15	ns

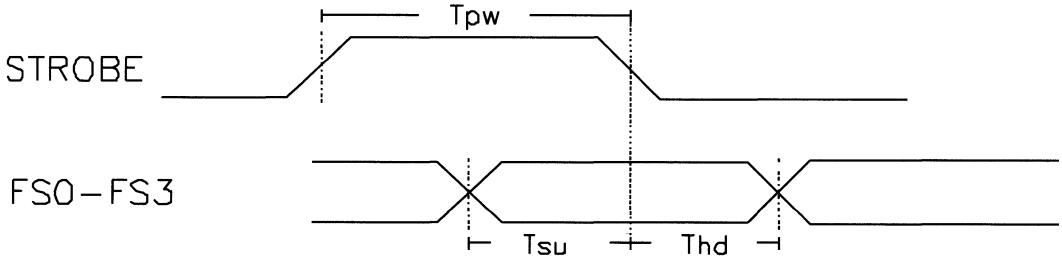


Figure 3

Motherboard Clock Generator

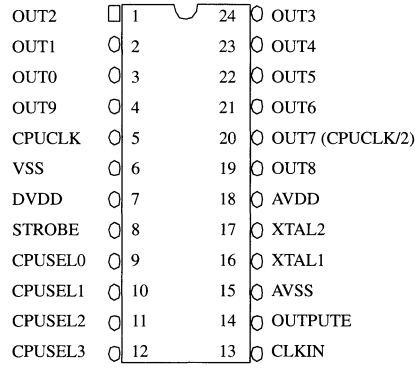
Features

- Low cost - eliminates multiple oscillators and Count Down Logic
- Primary VCO has 16 Mask Programmable frequencies (normally CPU clock)
- Secondary VCO has 1 Mask Programmable frequency (usually 96 MHz)
- Pre-programmed Versions for typical PC applications
- 10 Outputs in addition to the Primary CPU clock
- Capability to reconfigure counter stages to change the frequencies of the outputs via mask options
- Advanced PLL design
- On chip PLL filters
- Very Flexible Architecture

Applications

- CPU clock and Co-processor clock
- Hard Disk and Floppy Disk clock
- Keyboard clock
- Serial Port clock
- Bus clock
- System counting or timing functions

Pin Configuration



Description

The **ICS2694** Motherboard Clock Generator is an in-tegrated circuit using PLL and VCO technology to generate virtually all the clock signals required in a PC. The use of the device can be generalized to satisfy the timing needs of most digital systems by reprogramming the VCO or reconfiguring the counter stages which derive the output frequencies from the VCO's.

The primary VCO is customarily used to generate the CPU clock and is so labeled on the **ICS2694**. Pre-programmed frequency sets are listed on page 6. These choices were made to match the major microprocessor families. CPUSEL (0-3) allow the user to select the appropriate frequency for the application.

Due to the filter in the phase-locked loop, the CPUCLK will move in a linear fashion from one frequency to a newly-selected frequency without glitches. If a fixed CPUCLK value is desired, CPUSEL (0-3) may be hard wired to the desired address with STROBE tied high. (It has a pullup.) For board test and debug, pulling OUTPUTE to Ground will tristate all the outputs.

Ordering Information

ICS2694N-XXX (DIP Package)
ICS2694M-XXX (SO Package)
(XXX - Pattern number)

Pin Description

PIN NUMBER	NAME	DESCRIPTION
1	OUT2	4mA Output
2	OUT1	4mA Output
3	OUT0	4mA Output
4	OUT9	4mA Output
5	CPUCLK	4mA Output driven by Voltage Controlled Oscillator 1 (VC01). VC01 is controlled by a 16 word ROM.
6	VSS	Ground for digital portion of chip
7	DVDD	Plus supply for digital portion of chip
8	STROBE	Input control for transparent latches associated with CPU (0-3) which select one of 16 values for CPUCLK. Holding STROBE high causes the latches to be transparent.
9	CPUSEL0	LSB CPUCLK address bit
10	CPUSEL1	CPUCLK address bit
11	CPUSEL2	CPUCLK address bit
12	CPUSEL3	MSB CPUCLK address bit
13	CLKIN	An alternative input for the reference clock. The crystal oscillator output and CLKIN are gated together to generate the reference clock for the VCO's. If CLKIN is used, XTAL1 should be held high and XTAL2 left open. If the internal oscillator is used, hold CLKIN high.
14	OUTPUTE	Pulling this line low tristates all outputs.
15	AVSS	Ground for analog portion of chip
16	XTAL1	Input of internal crystal oscillator stage
17	XTAL2	Output of internal crystal oscillator stage. This pin should have nothing connected to it but one of the quartz crystal terminals.
18	AVDD	Positive supply for analog portion of chip.
19	OUT8	4mA Output
20	OUT7	4mA Output (Usually assigned as CPUCLK/2 for co-processor use)
21	OUT6	4mA Output
22	OUT5	4mA Output
23	OUT4	4mA Output
24	OUT3	4mA Output

Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate series-resonant crystal should be connected between XTAL1 (1) and XTAL2 (2). In IBM-compatible applications, this will typically be a 14.31818 MHz crystal, but fundamental mode crystals between 10 MHz and 25 MHz have been tested. Maintain short lead lengths between the crystal and the **ICS2694**. In order to optimize the quality of the quartz crystal oscillator, the input switching threshold of XTAL1 is VDD/2 rather than the conventional 1.4 V of TTL. Therefore, XTAL1 may not respond properly to a legal TTL signal since TTL is not required to exceed VDD/2. Therefore, another clock input CLKIN (pin 13) has been added to the chip which is sized to have an input switching point of 1.4 V. Inside the chip, these two inputs are ANDED. Therefore, when using the XTAL1 and XTAL2, CLKIN should be held high. (It has a pullup.) When using CLKIN, XTAL1 should be held high. (It does not have a pullup because a pullup would interfere with the oscillator bias.)

It is anticipated that some applications will use both clock inputs, properly gated, for either board test or unique system functions. By generating all the system clocks from one reference input, the phase and delay relationships between the various outputs will remain relatively fixed, thereby eliminating problems arising from totally unsynchronized clocks interacting in a system.

Power Supply Conditioning

The **ICS2694** is a member of the second generation of dot clock products. By incorporating the loop filter on chip and upgrading the VCO, the ease of application has been substantially improved over earlier products. If a stable and noise-free power supply is available, no external components are required. However, in some applications it may be judicious to decouple the power supply as shown in Figures 1 or 2. Figure 1 is the normal configuration for 5 Volt only applications. Which of the two provides superior performance depends on the noise content of the power supplies. In general, the configuration of Figure 1 is satisfactory. Figure 2 is the more conventional if a 12 Volt analog supply is available, although the improved performance comes at a cost of an extra component; however, the cost of the discretes used in Figure 2 are less than the cost of Figure 1's discrete components.

Since the **ICS2694** outputs a large number of high-frequency clocks, conservative design practices are recommended. Care should be exercised in the board layout of supply and ground traces, and adequate power supply decoupling capacitors consistent with the application should be used.

D

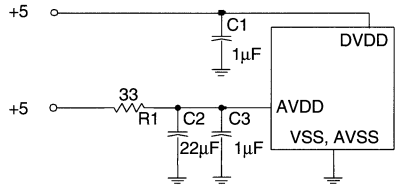


Figure 1

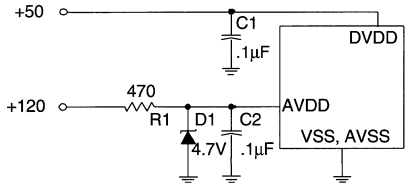


Figure 2

Absolute Maximum Ratings

Supply Voltage	V_{DD}	-0.5V to +7V
Input Voltage	V_{IN}	-0.5V to VDD +0.5V
Output Voltage	VOUT	-0.5V to VDD +0.5V
Clamp Diode Current	V_{IK} & I_{OK}	+/-30mA
Output Current per Pin	I_{OUT}	+/-50mA
Operating Temperature	T_O	0 °C to + 150 °C
Storage Temperature	T_S	-85 °C to + 150 °C
Power Dissipation	P_D	500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation, it is recommended that V_{IN} and V_{OUT} be constrained to > = V_{SS} and < = V_{DD}.

DC Characteristics (0 °C to 70 °C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{DD}	Operating Voltage Range	4.0	5.5	V	
V_{IL}	Input Low Voltage	V_{SS}	0.8	V	$V_{DD = 5V}$
V_{IH}	Input High Voltage	2.0	V_{DD}	V	V_{DD} = 5V
I_{IH}	Input Leakage Current	-	10	*u*A	$V_{IN} = V_{cc}$
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = 4.0 mA
I_{DD}	Supply Current	-	55	mA	V_{DD} = 5V, CPUCLK = 80 MHz
R_{UP} *	Internal Pullup Resistors	50	-	K Ohm	V_{DD} = 5V, V_{in} = 0V
C_{in}	Input Pin Capacitance	-	8	pF	F_c = 1 MHz
C_{out}	Output Pin Capacitance	-	12	pF	F_c = 1 MHz

* The following inputs have pullups: OUTPUTE, STROBE, CPUSEL (0-3), CLKIN.

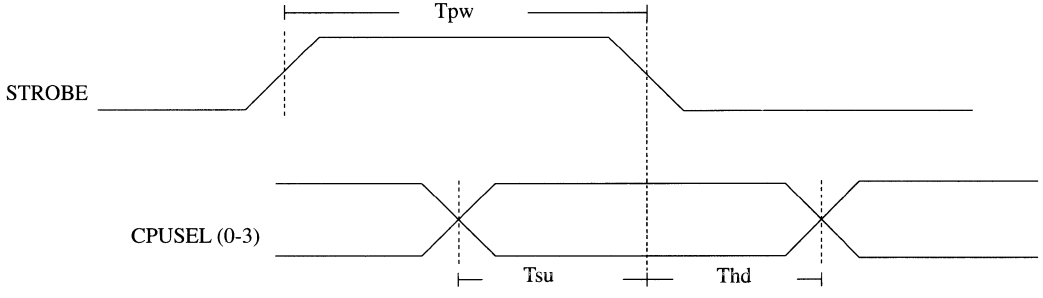
AC Timing Characteristics

The following notes apply to all parameters presented in this section:

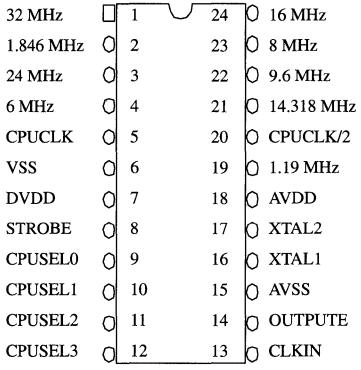
1. Xtal Frequency = 14.31818 MHz
2. All units are in nanoseconds (ns).
3. Rise and fall time is between 0.8 and 2.0 VDC.
4. Output pin loading = 15pF
5. Duty cycle is measured at 1.4V.
6. Supply Voltage Range = 4.5 to 5.5 Volts
7. Temperature Range = 0 °C to 70 °C

SYMBOL	PARAMETER	MIN	MAX	NOTES
	STROBE TIMING			
Tpw	Strobe Pulse Width	20	-	
Tsu	Setup Time Data to Strobe	10	-	
Thd	Hold Time Data to Strobe	10	-	
	FOUT TIMING			
Tr	Rise Time	-	3	Duty Cycle 40% min. to 60% max.
Tf	Fall Time	-	3	at 80 MHz
-	Frequency Error		0.5	%
-	Maximum Frequency		135	MHz

Note:
Pattern -004 has rising edges of CPUCLK and CPUCLK/2 matched to ± 2 ns.



ICS2694 Standard Patterns



ICS2694-004

CPUSEL0-3 (Hex)	CPUCLK OUTPUT (Pin 5) (MHz)
0	2
1	10
2	20
3	24
4	25
5	32
6	33.33
7	40
8	48
9	50
10	54
11	66.67
12	68
13	80
14	100
15	16

Note:
Pattern -004 has rising edges of CPUCLK and CPUCLK/2 matched to ± 2 ns.

Another alternative for CPU CLOCK generation is the ICS2494-244 if the additional functions of the **ICS2694** are not needed in the application.

ICS Part Number	ICS2494-244
Address FS3-0 (Hex)	Frequency (MHz)
0	20
1	24
2	32
3	40
4	50
5	66.6
6	80
7	100
8	54
9	70
0	90
B	110
C	25
D	33.3
E	40
F	50
Address MS1-0 (Hex)	Frequency (MHz)
0	16
1	24
2	50
3	66.6

Integrated Circuit Systems, Inc.

CPU Frequency Generator

Features

- **Patented on-chip Phase Locked Loop with VCO for clock generation**
- **Provides reference clock and synthesized clock**
- **Generates frequencies from 2 to 120 MHz**
- **2 to 32 MHz input reference frequency**
- **On chip loop filter**
- **Up to 16 frequencies stored internally**
- **Low power CMOS technology**
- **Single +3.3 or +5 volt power supply**
- **Runs up to 50 MHz at 3.3V**
- **8 pin DIP or SOIC package or 14 pin DIP or SOIC package**

General Description

The AV9107 offers a tiny footprint solution for generating two simultaneous clocks. One clock, the REFCLK, is a fixed output frequency which is the same as the input reference crystal (or clock). The other clock, CLK1, can vary between 2 and 120 MHz, with up to 16 selectable preprogrammed frequencies stored in internal ROM.

The device has advanced features which include on-chip loop filters, tri-state outputs, and power down capability. A minimum of external components - two decoupling capacitors and an optional ferrite bead - are all that are required for jitter free operation. Standard versions for computer motherboard applications are the AV9107-03, AV9107-04, AV9107-05 and AV9107-10. Custom masked versions, with customized frequencies and features, are available in 6-8 weeks for a small NRE.

Applications

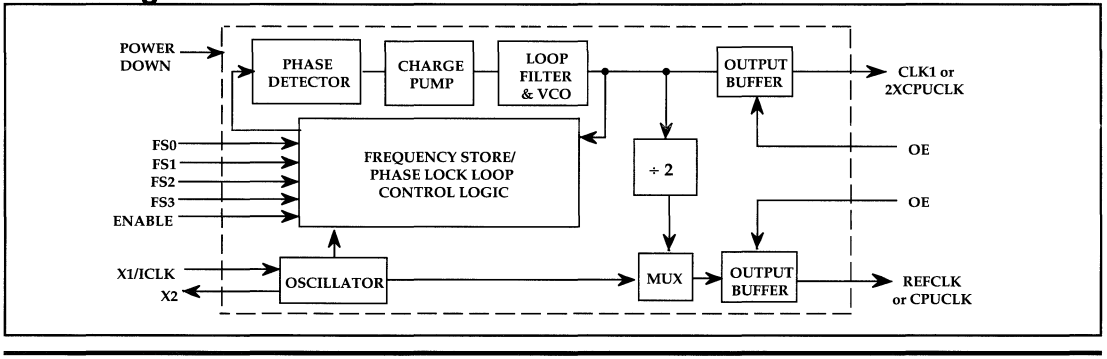
Graphics: The AV9107 is the easiest to use, lowest cost, and smallest footprint frequency generator for graphics applications. It can generate up to 16 different frequencies, including all frequencies necessary for VGA standards. It should be used in place of the AV9105/6 when the reference clock is also needed.

Computer: The AV9107 is the ideal solution for replacing high speed oscillators and for reducing clock speeds to save power in computers. The device provides smooth, glitch-free frequency transitions so that the CPU can continue to operate during slow down or speed up. The rate of frequency change makes the AV9107 compatible with all 386DX, 386SX, 486DX, 486DX2, and 486SX devices. Standard versions include the AV9107-03, -04, -05 and -10.

Disk Drives: Smaller than a single crystal or an oscillator, the tiny SOIC package can be used for any general purpose frequency generation in disk drives. The most popular application is for Constant Density Recording, where its low jitter output clock provides the necessary frequencies for reading and recording. Another popular application is for slowing the disk drive CPU to save power.

High Speed Systems: The AV9107 can be used as a proximity oscillator - using a low frequency (down to 2 MHz) input to generate a high frequency clock (up to 120 MHz) near the device requiring the high frequency. This avoids the need to route high speed traces over a long distance.

Block Diagram



Decoding Table for AV9107-05, 14.318 input

FS1	FS0	CLK1
0	0	40 MHz
0	1	50 MHz
1	0	66.6 MHz
1	1	80 MHz

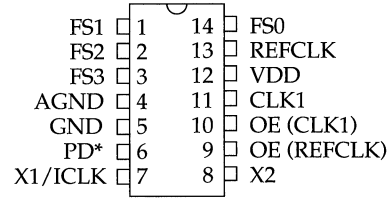
Decoding Table for AV9107-10, 14.318 input

FS1	FS0	CLK1
0	0	25 MHz
0	1	33.3 MHz
1	0	40 MHz
1	1	50 MHz

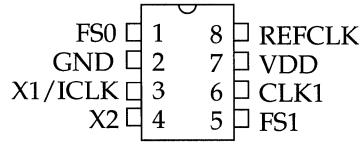
Decoding Table for AV9107-03, 14.318 input

FS3	FS2	FS1	FS0	CLK1
0	0	0	0	16 MHz
0	0	0	1	40 MHz
0	0	1	0	50 MHz
0	0	1	1	80 MHz
0	1	0	0	66.66 MHz
0	1	0	1	100 MHz
0	1	1	0	8 MHz
0	1	1	1	4 MHz
1	0	0	0	8 MHz
1	0	0	1	20 MHz
1	0	1	0	25 MHz
1	0	1	1	40 MHz
1	1	0	0	33.33 MHz
1	1	0	1	50 MHz
1	1	1	0	4 MHz
1	1	1	1	2 MHz

Pin Configurations



AV9107-03



AV9107-05/-10

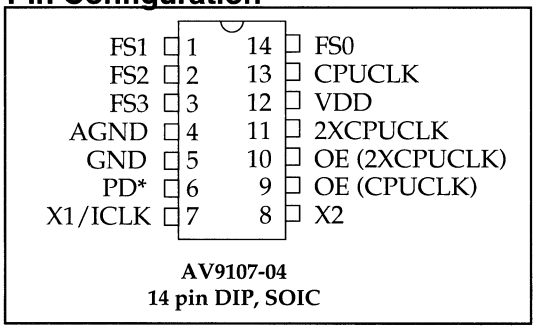
Pin Description for AV9107-03, AV9107-05 and AV9107-10

Pin Name	Pin #		Pin Type	Description
	-05/-10	-03		
FS0	1	14	Input	FREQUENCY SELECT 0 for CLK1 (-03 has pull-up)
FS1	5	1	Input	FREQUENCY SELECT 1 for CLK1 (-03 has pull-up)
FS2		2	Input	FREQUENCY SELECT 2 for CLK1 (-03 has pull-up)
FS3		3	Input	FREQUENCY SELECT 3 for CLK1 (-03 has pull-up)
AGND		4	-	Analog GROUND
GND	2	5	-	Digital GROUND
PD*		6	Input	POWER DOWN. Shuts off chip when low. Internal pull-up
X1/ICLK	3	7	Input	CRYSTAL INPUT or INPUT CLOCK frequency. Typically 14.318MHz system clock
X2	4	8	Output	CRYSTAL OUTPUT (No Connect when clock used)
OE(REFCLK)		9	Input	OUTPUT ENABLE. Tri-states REFCLK when low. Pull-up
OE(CLK1)		10	Input	OUTPUT ENABLE. Tri-states CLK1 when low. Pull-up
CLK1	6	11	Output	CLOCK1 Output (see decoding tables)
VDD	7	12	-	Digital power supply (+5V DC)
REFCLK	8	13	Output	REFERENCE CLOCK output. Produces a buffered version of the input clock or crystal frequency (typically 14.318 MHz)

The AV9107-04

The AV9107-04 provides a 2X output and a 1X output, which are skew controlled to within 1ns on the rising edges. For the frequencies listed in the decoding tables, the part assumes a 14.318 MHz input. The device is also useful for providing integer multiples or divides based on inputs in the range of 2 to 32 MHz.

Pin Configuration



AV9107-04
14 pin DIP, SOIC

Decoding Table for AV9107-04 (using a 14.318 MHz input)

FS3	FS2	FS1	FS0	2XCPUCLK	CPUCLK
0	0	0	0	80 MHz	40 MHz
0	0	0	1	66.66 MHz	33.33 MHz
0	0	1	0	50 MHz	25 MHz
0	0	1	1	40 MHz	20 MHz
0	1	0	0	100 MHz	50 MHz
0	1	0	1	33.33 MHz	16.67 MHz
0	1	1	0	32 MHz	16 MHz
0	1	1	1	25 MHz	12.5 MHz
1	0	0	0	64 MHz	32 MHz
1	0	0	1	2X INPUT	INPUT
1	0	1	0	3X INPUT	1.5X INPUT
1	0	1	1	8X INPUT	4X INPUT
1	1	0	0	.5X INPUT	.25X INPUT
1	1	0	1	.25X INPUT	.125X INPUT
1	1	1	0	120 MHz	60 MHz
1	1	1	1	130 MHz	65 MHz

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Pin Description for AV9107-04

Pin Name	Pin #	Pin Type	Description
FS1	1	Input	FREQUENCY SELECT 1 (see decoding table). Pull-up
FS2	2	Input	FREQUENCY SELECT 2 (see decoding table). Pull-up
FS3	3	Input	FREQUENCY SELECT 3 (see decoding table). Pull-up
AGND	4	-	Analog GROUND
GND	5	-	Digital GROUND
PD*	6	Input	POWER DOWN. Shuts off entire chip when low. Pull-up
X1/ICLK	7	Input	CRYSTAL INPUT or INPUT CLOCK frequency. Typically 14.318MHz system clock
X2	8	Output	CRYSTAL OUTPUT (No Connect when clock used)
OE(CPUCLK)	9	Input	OUTPUT ENABLE. Tri-states CPUCLK when low. Pull-up
OE(2XCPUCLK)	10	Input	OUTPUT ENABLE. Tri-states 2XCPUCLK when low. Pull-up
2XCPUCLK	11	Output	2X CPU CLOCK Output (see decoding table, note † below)
VDD	12	-	Digital power supply (+5V DC)
CPUCLK	13	Output	CPU CLOCK Output (see decoding table, note † below)
FS0	14	Input	FREQUENCY SELECT 0 (see decoding table). Pull-up

†The CPUCLK and 2XCPUCLK outputs are skew controlled to within 1.0 ns max

Frequency Accuracy and Calculation

The accuracy of the frequencies produced by the AV9107 depends on the input frequency and the desired actual output frequency. The formula for calculating the exact output frequency is as follows:

$$\text{Output Frequency} = \text{Input Frequency} \times \frac{A}{B}$$

where A = 2, 3, 4...128, and
B = 2, 3, 4...32.

For example, to calculate the actual output frequency for a video monitor expecting a 44.900 MHz clock and using a 14.318 MHz input clock, the closest A/B ratio is 69/22, which gives an output of 44.906 MHz (within 0.02% of the target frequency). Generally, the AV9107 can produce frequencies within 0.1% of the desired output.

Allowable Input and Output Frequencies

The input frequency should be between 2 and 32 MHz and the A/B ratio should not exceed 24. The output should fall in the range of 2-120 MHz.

Output Enable

The Output Enable feature tri-states the specified output clock pins. This places the selected output pins in a high impedance state to allow for system level diagnostic testing.

Power Down

If equipped, the power down pin shuts off the specified PLL or entire chip to save current. A few milliseconds are required to reach full functioning speed from a power down state.

Frequency Transitions

A key AV9107 feature is the ability to provide glitch-free frequency transitions across its output frequency range. The AV9107-03 provides smooth transitions between any of the two groups of eight frequencies (when FS3=0 or FS3=1), so that the device will switch glitch-free between 4 - 100 MHz and 2 - 50 MHz.

ABSOLUTE MAXIMUM RATINGS

AVDD, VDD referenced to GND..... 7V
Operating temperature under bias..... 0°C to +70°C
Storage temperature..... -65°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation..... 0.5 Watts

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device This is a stress rating only, and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect the reliability of the device.

ELECTRICAL CHARACTERISTICS AT 5V

(Operating V_{DD} = +4.5V to +5.5V, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC CHARACTERISTICS						
V_{IL}	Input Low Voltage	-	-	0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0	-	-	V	V_{DD} = 5V
I_{IL}	Input Low Current	-	-	-5	µA	V_{IN} = 0V
I_{IH}	Input High Current	-	-	5	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage	-	-	0.4	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	2.4	-	-	V	I_{OH} = -4mA
I_{DD}	Supply Current	-	10	20	mA	Note 1
F_d	Output Frequency Change over Supply and Temperature	-	0.002	0.05	%	With respect to typical frequency
C_I	Input Capacitance			10	pF	Except X1, X2
C_L	Load Capacitance		20		pF	Pins X1, X2
$I_{DDSTDBY}$	Standby Supply Current		25		µA	Note 2
AC CHARACTERISTICS						
t_w	Enable pulse width	20	-	-	ns	
t_{su}	Setup time data to enable	20	-	-	ns	
f_o	Output Frequency	2		120	MHz	
f_i	Input Frequency	2	14.318	32	MHz	
$ICLK_r$	Input Clock Rise time	-	-	20	ns	
$ICLK_f$	Input Clock Fall time	-	-	20	ns	
t_{hd}	Hold time data to enable	10	-	-	ns	
t_r	Output Rise time, 0.8 to 2.0V	-	1	2	ns	25 pf load
t_r	Rise time, 20% to 80% V_{DD}	-	2	4	ns	25 pf load
t_f	Output Fall time, 2.0 to 0.8V	-	1	2	ns	25 pf load
t_f	Fall time, 80% to 20% V_{DD}	-	-	4	ns	25 pf load
d_t	Duty cycle	40	50/50	60	%	15 pf load
T_{jls}	Jitter, 1 sigma		±0.5	±2	%	All frequencies
T_{jabs}	Jitter, absolute		±3	±5	%	All frequencies
t_{ft}	Frequency Transition time			20	ms	From 50 to 4 MHz
t_{pu}	Power up time		15	30	ms	From off to 100MHz
T_{sk}	Clock skew between CPUCLK and 2XCPUCLK outputs		±0.5	±1.0	ns	AV9107-04

Note 1: AV9107-03 with no load, with 14.318 MHz crystal input, and CLK1 running at 40 MHz. Power supply current varies with frequency. Consult Avasem for actual current at different frequencies.
Note 2: AV9107-03 with the power down pin low (active).
Note 3: To guarantee operation at 100 MHz or above, please indicate the highest speed used when ordering. For example, if 120 MHz would be used on the AV9107-04CS14, order it as AV9107-04CS14-120.

Electrical Characteristics at 3.3V

(Operating V_{DD} = +3.0V to +3.7V, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC CHARACTERISTICS						
V_{IL}	Input Low Voltage	-	-	$0.15V_{DD}$	V	
V_{IH}	Input High Voltage	$0.7V_{DD}$	-	-	V	
I_{IL}	Input Low Current	-	-	-5	µA	V_{IN} = 0V
I_{IH}	Input High Current	-	-	5	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage	-	-	0.1	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	V_{DD}-.1V	-	-	V	I_{OH} = -4mA
I_{DD}	Supply Current	-	8	15	mA	Note 1
F_d	Output Frequency Change over Supply and Temperature	-	0.002	0.01	%	With respect to typical frequency
C_I	Input Capacitance			10	pF	Except X1, X2
C_L	Load Capacitance		20		pF	Pins X1, X2
$I_{DDSTDBY}$	Supply Current, Standby		15		µA	When powered down
AC CHARACTERISTICS						
t_w	Enable pulse width	20	-	-	ns	
t_{su}	Setup time data to enable	20	-	-	ns	
$ICLK_r$	Input Clock Rise time	-	-	20	ns	
$ICLK_f$	Input Clock Fall time	-	-	20	ns	
t_{hd}	Hold time data to enable	10	-	-	ns	
t_r	Rise time	-	-	4	ns	15 pf load
t_f	Fall time	-	-	4	ns	15 pf load
d_t	Duty cycle	40	50/50	60	%	15 pf load
T^{jt}	Jitter, 1 sigma		±0.5	±2	%	All frequencies
T^{jts}_{jabs}	Jitter, absolute		±3	±5	%	All frequencies
t_{ft}	Frequency Transition time			20	ms	From 2 to 25 MHz
t_{pu}	Power up time		15		ms	From off to 66.66 MHz
f_o	Output Frequency	2		80	MHz	
f_i	Input Frequency	2	14.318	32	MHz	

Note 1: AV9107-03 with no load, with 14.318 MHz crystal input, and CLK1 running at 40 MHz. Power supply current varies with frequency. Consult ICS for actual current at different frequencies.
Note 2: To guarantee 3V operation, please specify the AV9107-xxCxxx-3V when ordering.

Actual Frequencies

Decoding Table for AV9107-05, 14.318 input

FS1	FS0	CLK1
0	0	40.01 MHz
0	1	50.11 MHz
1	0	66.61 MHz
1	1	80.01 MHz

Decoding Table for AV9107-03, 14.318 input

FS3	FS2	FS1	FS0	CLK1
0	0	0	0	16.00 MHz
0	0	0	1	39.99 MHz
0	0	1	0	50.11 MHz
0	0	1	1	80.01 MHz
0	1	0	0	66.58 MHz
0	1	0	1	100.23 MHz
0	1	1	0	8.02 MHz
0	1	1	1	4.01 MHz
1	0	0	0	8.02 MHz
1	0	0	1	20.00 MHz
1	0	1	0	25.06 MHz
1	0	1	1	40.01 MHz
1	1	0	0	33.29 MHz
1	1	0	1	50.11 MHz
1	1	1	0	4.01 MHz
1	1	1	1	2.05 MHz

Decoding Table for AV9107-10, 14.318 input

FS1	FS0	CLK1
0	0	25.057 MHz
0	1	33.289 MHz
1	0	40.006 MHz
1	1	50.113 MHz

Decoding Table for AV9107-04, 14.318 input

FS3	FS2	FS1	FS0	2XCPUCLK	CPUCLK
0	0	0	0	80.02 MHz	40.01 MHz
0	0	0	1	66.62 MHz	33.31 MHz
0	0	1	0	50.11 MHz	25.06 MHz
0	0	1	1	40.01 MHz	20.00 MHz
0	1	0	0	100.23 MHz	50.11 MHz
0	1	0	1	33.31 MHz	16.66 MHz
0	1	1	0	32.01 MHz	16.00 MHz
0	1	1	1	25.06 MHz	12.47 MHz
1	0	0	0	64.02 MHz	32.01 MHz
1	0	0	1	2X INPUT	1X INPUT
1	0	1	0	3X INPUT	1.5X INPUT
1	0	1	1	8X INPUT	4X INPUT
1	1	0	0	.5X INPUT	.25X INPUT
1	1	0	1	.25X INPUT	.125X INPUT
1	1	1	0	120.00 MHz	60.00 MHz
1	1	1	1	129.96 MHz	64.98 MHz

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Ordering Information

Part Number	Temperature Range	Package Type
AV9107-xxCN8	0°C to +70°C	8 lead Plastic DIP (300 mils)
AV9107-xxCS8	0°C to +70°C	8 lead SOIC (150 mils)
AV9107-xxCN14	0°C to +70°C	14 lead Plastic DIP (300 mils)
AV9107-xxCS14	0°C to +70°C	14 lead SOIC (150 mils)

Integrated Circuit Systems, Inc.

ICS9108

Advance Information

CPU Frequency Generator

Features

- 3V version of popular ICS9107
- Runs up to 66 MHz at 3.3V
- 50/50 typical duty cycle
- ±250 psec absolute jitter
- Generates frequencies from 2 to 140 MHz
- 2 to 32 MHz input reference frequency
- Up to 16 frequencies stored internally
- Patented on-chip Phase Locked Loop with VCO for clock generation
- Provides reference clock and synthesized clock
- On chip loop filter
- Low power 0.8 µ CMOS technology
- 8 pin or 14 pin DIP or SOIC package

General Description

The ICS9108 offers a tiny footprint solution for generating two simultaneous clocks. One clock, the REFCLK, is a fixed output frequency which is the same as the input reference crystal (or clock). The other clock, CLK1, can vary between 2 and 140 MHz, with up to 16 selectable preprogrammed frequencies stored in internal ROM.

The ICS9108 is ideal for use in a 3.3V system. It can generate a 66.66 MHz clock at 3.3V. In addition, the ICS9108 provides a symmetrical wave form with a worst case duty cycle of 45/55. The ICS9108-04 has very tight edge control between the CPU clock and 2XCPU clock outputs, with a worst case skew of 250 psec.

The device has advanced features which include on-chip loop filters, tri-state outputs, and power down capability. A minimum of external components - two decoupling capacitors and an optional ferrite bead - are all that are required for jitter free operation. Standard versions for computer motherboard applications are the ICS9108-03, ICS9108-04, ICS9108-05, and the ICS9108-10. Custom masked versions, with customized frequencies and features, are available in 6-8 weeks for a small NRE fee.

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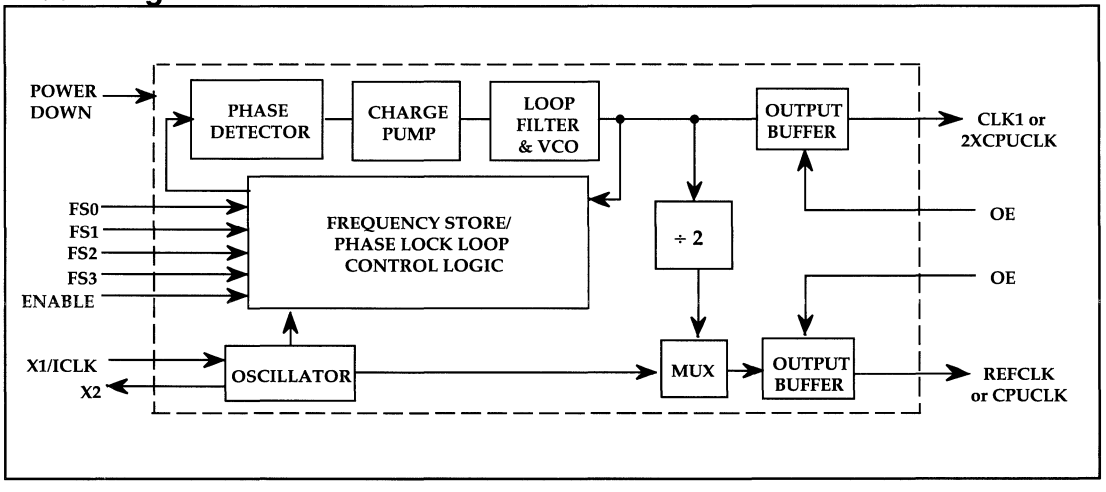
Block Diagram



Decoding Table for ICS9108-05, 14.318 input

FS1	FS0	CLK1
0	0	40 MHz
0	1	50 MHz
1	0	66.6 MHz
1	1	80 MHz

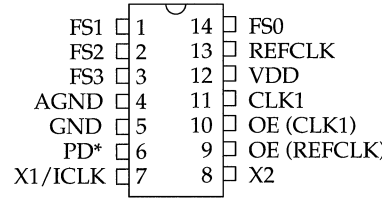
Decoding Table for ICS9108-10, 14.318 input

FS1	FS0	CLK1
0	0	25 MHz
0	1	33.3 MHz
1	0	40 MHz
1	1	50 MHz

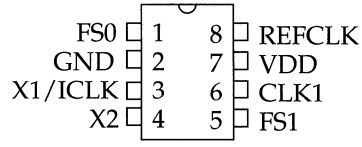
Decoding Table for ICS9108-03, 14.318 input

FS3	FS2	FS1	FS0	CLK1
0	0	0	0	16 MHz
0	0	0	1	40 MHz
0	0	1	0	50 MHz
0	0	1	1	80 MHz
0	1	0	0	66.66 MHz
0	1	0	1	100 MHz
0	1	1	0	8 MHz
0	1	1	1	4 MHz
1	0	0	0	8 MHz
1	0	0	1	20 MHz
1	0	1	0	25 MHz
1	0	1	1	40 MHz
1	1	0	0	33.33 MHz
1	1	0	1	50 MHz
1	1	1	0	4 MHz
1	1	1	1	2 MHz

Pin Configurations



ICS9108-03



ICS9108-05/-10

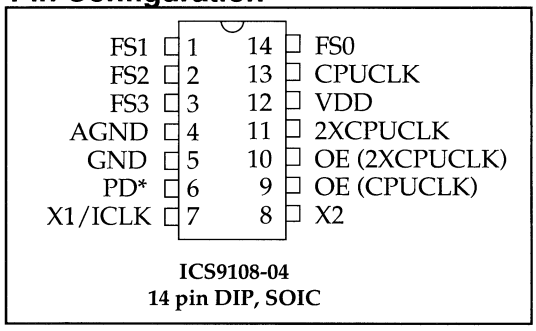
Pin Description for ICS9108-03, ICS9108-05 and ICS9108-10

Pin Name	Pin #		Pin Type	Description
FS0	1	14	Input	FREQUENCY SELECT 0 for CLK1 (-03 has pull-up)
FS1	5	1	Input	FREQUENCY SELECT 1 for CLK1 (-03 has pull-up)
FS2		2	Input	FREQUENCY SELECT 2 for CLK1 (-03 has pull-up)
FS3		3	Input	FREQUENCY SELECT 3 for CLK1 (-03 has pull-up)
AGND		4	-	Analog GROUND
GND	2	5	-	Digital GROUND
PD*		6	Input	POWER DOWN. Shuts off chip when low. Internal pull-up
X1/ICLK	3	7	Input	CRYSTAL INPUT or INPUT CLOCK frequency. Typically 14.318MHz system clock
X2	4	8	Output	CRYSTAL OUTPUT (No Connect when clock used)
OE(REFCLK)		9	Input	OUTPUT ENABLE. Tri-states REFCLK when low. Pull-up
OE(CLK1)		10	Input	OUTPUT ENABLE. Tri-states CLK1 when low. Pull-up
CLK1	6	11	Output	CLOCK1 Output (see decoding tables)
VDD	7	12	-	Digital power supply (+3V DC)
REFCLK	8	13	Output	REFERENCE CLOCK output. Produces a buffered version of the input clock or crystal frequency (typically 14.318 MHz)

The ICS9108-04

The ICS9108-04 provides a 2X output and a 1X output, which are skew controlled to within 1ns on the rising edges. For the frequencies listed in the decoding tables, the part assumes a 14.318 MHz input. The device is also useful for providing integer multiples or divides based on inputs in the range of 2 to 32 MHz.

Pin Configuration



ICS9108-04
14 pin DIP, SOIC

Decoding Table for ICS9108-04 (using a 14.318 MHz input)

FS3	FS2	FS1	FS0	2XCPUCLK	CPUCLK
0	0	0	0	80 MHz	40 MHz
0	0	0	1	66.66 MHz	33.33 MHz
0	0	1	0	50 MHz	25 MHz
0	0	1	1	40 MHz	20 MHz
0	1	0	0	100 MHz	50 MHz
0	1	0	1	33.33 MHz	16.67 MHz
0	1	1	0	32 MHz	16 MHz
0	1	1	1	25 MHz	12.5 MHz
1	0	0	0	64 MHz	32 MHz
1	0	0	1	2X INPUT	INPUT
1	0	1	0	3X INPUT	1.5X INPUT
1	0	1	1	8X INPUT	4X INPUT
1	1	0	0	.5X INPUT	.25X INPUT
1	1	0	1	.25X INPUT	.125X INPUT
1	1	1	0	120 MHz	60 MHz
1	1	1	1	130 MHz	65 MHz

D

Pin Description for ICS9108-04

Pin Name	Pin #	Pin Type	Description
FS1	1	Input	FREQUENCY SELECT 1 (see decoding table). Pull-up
FS2	2	Input	FREQUENCY SELECT 2 (see decoding table). Pull-up
FS3	3	Input	FREQUENCY SELECT 3 (see decoding table). Pull-up
AGND	4	-	Analog GROUND
GND	5	-	Digital GROUND
PD*	6	Input	POWER DOWN. Shuts off entire chip when low. Pull-up
X1/ICLK	7	Input	CRYSTAL INPUT or INPUT CLOCK frequency. Typically 14.318MHz system clock
X2	8	Output	CRYSTAL OUTPUT (No Connect when clock used)
OE(CPUCLK)	9	Input	OUTPUT ENABLE. Tri-states CPUCLK when low. Pull-up
OE(2XCPUCLK)	10	Input	OUTPUT ENABLE. Tri-states 2XCPUCLK when low. Pull-up
2XCPUCLK	11	Output	2X CPU CLOCK Output (see decoding table, note † below)
VDD	12	-	Digital power supply (+3V DC)
CPUCLK	13	Output	CPU CLOCK Output (see decoding table, note † below)
FS0	14	Input	FREQUENCY SELECT 0 (see decoding table). Pull-up

†The CPUCLK and 2XCPUCLK outputs are skew controlled to within 1.0 ns max

Frequency Accuracy and Calculation

The accuracy of the frequencies produced by the ICS9108 depends on the input frequency and the desired actual output frequency. The formula for calculating the exact output frequency is as follows:

$$\text{Output Frequency} = \text{Input Frequency} \times \frac{A}{B}$$

where A = 2, 3, 4...128, and
B = 2, 3, 4...32.

For example, to calculate the actual output frequency for a video monitor expecting a 44.900 MHz clock and using a 14.318 MHz input clock, the closest A/B ratio is 69/22, which gives an output of 44.906 MHz (within 0.02% of the target frequency). Generally, the ICS9108 can produce frequencies within 0.1% of the desired output.

Allowable Input and Output Frequencies

The input frequency should be between 2 and 32 MHz and the A/B ratio should not exceed 24. The output should fall in the range of 2-120 MHz.

Output Enable

The Output Enable feature tri-states the specified output clock pins. This places the selected output pins in a high impedance state to allow for system level diagnostic testing.

Power Down

If equipped, the power down pin shuts off the specified PLL or entire chip to save current. A few milliseconds are required to reach full functioning speed from a power down state.

Frequency Transitions

A key ICS9108 feature is the ability to provide glitch-free frequency transitions across its output frequency range. The ICS9108-03 provides smooth transitions between any of the two groups of eight frequencies (when FS3=0 or FS3=1), so that the device will switch glitch-free between 4 - 100 MHz and 2 - 50 MHz.

Absolute Maximum Ratings

AVDD, VDD referenced to GND..... 7V
Operating temperature under bias..... 0°C to +70°C
Storage temperature..... -65°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation..... 0.5 Watts

Note. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect the reliability of the device

Electrical Characteristics at 5V

(Operating V_{DD} = +4.5V to +5.5V, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage	-	-	0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0	-	-	V	V_{DD} = 5V
I_{IL}	Input Low Current	-	-	-5	µA	V_{IN} = 0V
I_{IH}	Input High Current	-	-	5	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage	-	-	0.4	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	2.4	-	-	V	I_{OH} = -4mA
I_{DD}	Supply Current	-	15	20	mA	Note 1
F_d	Output Frequency Change over Supply and Temperature	-	0.002	0.05	%	With respect to typical frequency
C_i	Input Capacitance			10	pF	Except X1, X2
C_L	Load Capacitance		20		pF	Pins X1, X2
$I_{DDSTDBY}$	Standby Supply Current		10		µA	Note 2
AC Characteristics						
t_w	Enable pulse width	20	-	-	ns	
t_{su}	Setup time data to enable	20	-	-	ns	
f_o	Output Frequency	2		120	MHz	
f_i	Input Frequency	2	14.318	32	MHz	
$ICLK_r$	Input Clock Rise time	-	-	20	ns	
$ICLK_f$	Input Clock Fall time	-	-	20	ns	
t_{hd}	Hold time data to enable	10	-	-	ns	
t_r	Output Rise time, 0.8 to 2.0V	-	1	2	ns	25 pf load
t_r	Rise time, 20% to 80% V_{DD}	-	2	4	ns	25 pf load
t_f	Output Fall time, 2.0 to 0.8V	-	1	2	ns	25 pf load
t_f	Fall time, 80% to 20% V_{DD}	-	-	4	ns	25 pf load
d_t	Duty cycle (Up to 66.6 MHz)	45	50	55	%	15 pf load
d_t	Duty cycle (All other frequencies)	40	48/52	60	%	15 pf load
T_{jls}	Jitter, 1 sigma		90	150	ps	16 - 100 MHz
T_{jns}	Jitter, 1 sigma		150	300	ps	8 - 14.318 MHz
T_{jns}	Jitter, 1 sigma			1.5	ns	Below 8 MHz
T_{jabs}	Jitter, absolute		±150	±250	ps	16 - 100 MHz
T_{jabs}	Jitter, absolute		±500	±800	ps	8 - 14.318 MHz
T_{jabs}	Jitter, absolute			±3.5	ns	Below 8 MHz
t_{ft}	Frequency Transition time			20	ms	From 50 to 4 MHz
t_{pu}	Power up time		15	30	ms	From off to 100MHz
T_{sk}	Clock skew between CPUCLK and 2XCPUCLK outputs			±250	ps	AV9107-04

Note 1: AV9108-03 with no load, with 14.318 MHz crystal input, and CLK1 running at 40 MHz. Power supply current varies with frequency. Consult Avasem for actual current at different frequencies.
Note 2: AV9108-03 with the power down pin low (active).
Note 3: To guarantee operation at 100 MHz or above, please indicate the highest speed used when ordering. For example, if 120 MHz would be used on the AV9107-04CS14, order it as AV9108-04CS14-120.

Electrical Characteristics at 3.3V

(Operating V_{DD} = +3.0V to +3.7V, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage	-	-	$0.15V_{DD}$	V	
V_{IH}	Input High Voltage	$0.7V_{DD}$	-	-	V	
I_{IL}	Input Low Current	-	-	-5	µA	V_{IN} = 0V
I_{IH}	Input High Current	-	-	5	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage	-	-	0.1	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	V_{DD}-.1V	-	-	V	I_{OH} = -4mA
I_{DD}	Supply Current	-	10	15	mA	Note 1
F_d	Output Frequency Change over Supply and Temperature	-	0.002	0.01	%	With respect to typical frequency
C_t	Input Capacitance			10	pF	Except X1, X2
C_L	Load Capacitance		20		pF	Pins X1, X2
$I_{DDSTDBY}$	Supply Current, Standby		10		µA	When powered down
AC Characteristics						
t_w	Enable pulse width	20	-	-	ns	
t_{su}	Setup time data to enable	20	-	-	ns	
$ICLK_r$	Input Clock Rise time	-	-	20	ns	
$ICLK_f$	Input Clock Fall time	-	-	20	ns	
t_{hd}	Hold time data to enable	10	-	-	ns	
t_r	Rise time	-	-	4	ns	15 pf load
t_f	Fall time	-	-	4	ns	15 pf load
d_t	Duty cycle	40	48/52	60	%	15 pf load
T^{jt}	Jitter, 1 sigma		90	150	ps	16 - 100 MHz
T^{jts}	Jitter, 1 sigma		150	300	ps	8 - 14.318 MHz
T^{jts}	Jitter, 1 sigma			1.5	ns	Below 8 MHz
T^{jabs}	Jitter, absolute		±150	±250	ps	16 - 100 MHz
T^{jabs}	Jitter, absolute		±500	±800	ps	8 - 14.318 MHz
T^{jabs}	Jitter, absolute			±3.5	ns	Below 8 MHz
t_{ft}	Frequency Transition time			20	ms	From 2 to 25 MHz
t_{pu}	Power up time		15		ms	From off to 66.66 MHz
f_o	Output Frequency	2		67	MHz	AV9107-03, FS3 = 0
f_i	Input Frequency	2	14.318	32	MHz	

Note 1: AV9108-03 with no load, with 14.318 MHz crystal input, and CLK1 running at 40 MHz. Power supply current varies with frequency. Consult ICS for actual current at different frequencies.
Note 2: To guarantee 3V operation, please specify the AV9108-xxCxxx-3V when ordering.

Actual Frequencies

Decoding Table for ICS9108-05, 14.318 input

FS1	FS0	CLK1
0	0	40.01 MHz
0	1	50.11 MHz
1	0	66.61 MHz
1	1	80.01 MHz

Decoding Table for ICS9108-03, 14.318 input

FS3	FS2	FS1	FS0	CLK1
0	0	0	0	16.00 MHz
0	0	0	1	39.99 MHz
0	0	1	0	50.11 MHz
0	0	1	1	80.01 MHz
0	1	0	0	66.58 MHz
0	1	0	1	100.23 MHz
0	1	1	0	8.02 MHz
0	1	1	1	4.01 MHz
1	0	0	0	8.02 MHz
1	0	0	1	20.00 MHz
1	0	1	0	25.06 MHz
1	0	1	1	40.01 MHz
1	1	0	0	33.29 MHz
1	1	0	1	50.11 MHz
1	1	1	0	4.01 MHz
1	1	1	1	2.05 MHz

Decoding Table for ICS9108-04, 14.318 input

FS3	FS2	FS1	FS0	2XCPUCLK	CPUCLK
0	0	0	0	80.02 MHz	40.01 MHz
0	0	0	1	66.62 MHz	33.31 MHz
0	0	1	0	50.11 MHz	25.06 MHz
0	0	1	1	40.01 MHz	20.00 MHz
0	1	0	0	100.23 MHz	50.11 MHz
0	1	0	1	33.31 MHz	16.66 MHz
0	1	1	0	32.01 MHz	16.00 MHz
0	1	1	1	25.06 MHz	12.47 MHz
1	0	0	0	64.02 MHz	32.01 MHz
1	0	0	1	2X INPUT	1X INPUT
1	0	1	0	3X INPUT	1.5X INPUT
1	0	1	1	8X INPUT	4X INPUT
1	1	0	0	.5X INPUT	.25X INPUT
1	1	0	1	.25X INPUT	.125X INPUT
1	1	1	0	120.00 MHz	60.00 MHz
1	1	1	1	129.96 MHz	64.98 MHz

Decoding Table for AV9108-10, 14.318 input

FS1	FS0	CLK1
0	0	25.057 MHz
0	1	33.289 MHz
1	0	40.006 MHz
1	1	50.113 MHz

D

Ordering Information

Part Number	Temperature Range	Package Type
ICS9108-xxCN8	0°C to +70°C	8 lead Plastic DIP (300 mils)
ICS9108-xxCS8	0°C to +70°C	8 lead SOIC (150 mils)
ICS9108-xxCN14	0°C to +70°C	14 lead Plastic DIP (300 mils)
ICS9108-xxCS14	0°C to +70°C	14 lead SOIC (150 mils)

Note: The dash number following ICS9108 (denoted by xx above) must be included when ordering product since it specifies the frequency decoding table being ordered. Decoding options can be created by a simple metal mask change. Please use the ICS9108 order form when ordering custom masks.

Integrated Circuit Systems, Inc.

AV9128/9

Motherboard Frequency Generator

Features

- AV9129 - 28 pin direct replacement for AV9127
- AV9128 - 20 pin version for space-critical applications
- Four independent clock generators
- Skew controlled outputs on AV9129
- Smooth frequency transitions
- Power down options
- Tri-state outputs
- Up to 11 output clocks
- On-chip loop filter components
- Can generate clocks up to 100 MHz
- 14.318 MHz oscillator circuitry
- 28 pin PDIP or SOIC package - AV9129
- 20 pin PDIP or SOIC package - AV9128

Applications

Desktop Computers/Workstations: The AV9128/9 can provide all of the necessary clocks for the motherboard, replacing crystals and oscillators, and can be a single chip solution for all different speeds and types of processors used. The AV9129 has up to five synchronized outputs that are skew controlled to within 1ns (typical) for the processor clock (Clock#2), making it ideal for high speed 386, 486 and RISC systems. The AV9129-06 and AV9129-23 are standard parts available to all customers.

Laptop/Notebook Computers: The AV9128/9 is the ideal solution for generating clocks in portables. The user can save power by running the processor clock at lower frequencies, depending on the task being performed. The AV9128/9 further reduces the current consumption by having the ability to completely shut down the individual clocks when not in use. Standard parts with power down for portable computers include the AV9129-08, AV9128-22, and AV9128-24.

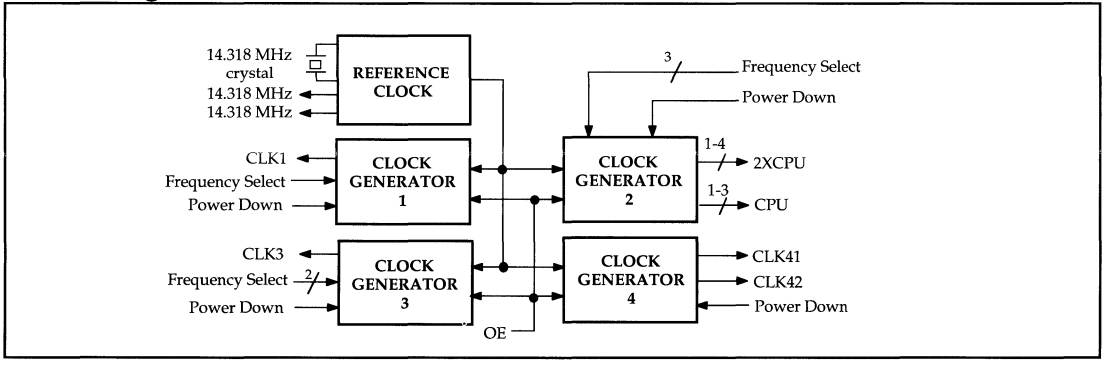
General Description

The AV9128/9 is designed to generate clocks for all 8088, 286, 386, 486, and RISC based motherboards, including laptops and notebook computers. The only external components required are an input crystal and decoupling capacitors. High performance applications may also require high speed clock termination components. The chip includes four independent clock generators plus the reference crystal oscillator clock to produce all necessary frequencies, including master clock, CPU clock, twice CPU clock frequency, keyboard clock, floppy disk controller clock, serial communications clock and bus clocks. Different frequencies from Clocks #1, #2 and #3 can be selected using the frequency select pins.

The frequencies and power down options in the AV9128/9 are mask programmable. Customer specific masks can be made and prototypes delivered within 6-8 weeks from receipt of order. ICS also offers standard versions such as those described in this data sheet.

The chip has multiple output buffers on key clocks to allow for improved EMI performance by isolating clocks going to different parts of the board, and thereby reducing the possibility of reflections. The chip provides slower clock edges compared to oscillators, further helping EMI.

Block Diagram

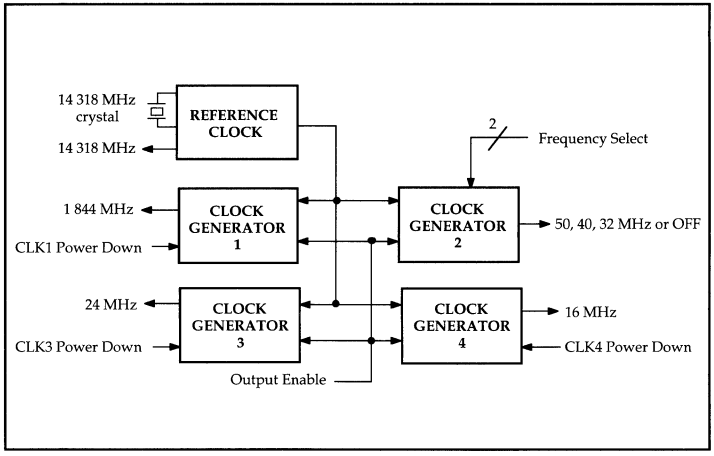


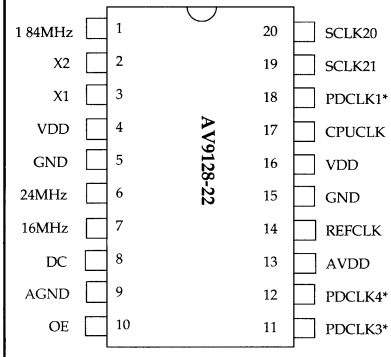
Pin Description for AV9128-22 (when using a 14.318MHz reference)

Pin Name	Pin #	Pin type	Description
CLK1	1	Output	CLOCK1. (1.84 MHz)
X2	2	Output	CRYSTAL connection for 14.318 MHz crystal
X1 / ICLK	3	Input	CRYSTAL connection for 14.318 MHz crystal or CLOCK INPUT
VDD	4	-	POWER SUPPLY (+5V)
GND	5	-	GROUND
CLK3	6	Output	CLOCK3 output (24 MHz)
CLK4	7	Output	CLOCK4 output (16 MHz)
DC	8	-	Don't Connect this pin
AGND	9	-	ANALOG GROUND
OE	10	Input	OUTPUT ENABLE. A low level tri-states all outputs. Note 1
PDCLK3*	11	Input	POWER DOWN. Powers down CLOCK3 when low
PDCLK4*	12	Input	POWER DOWN. Powers down CLOCK4 when low
AVDD	13	-	ANALOG POWER SUPPLY (+5V)
REFCLK	14	Output	REFERENCE CLOCK. Produces a 14.318 MHz clock
GND	15	-	GROUND
VDD	16	-	POWER SUPPLY (+5V)
CPUCLK	17	Output	CPU CLOCK. (see table)
PDCLK1*	18	Input	POWER DOWN. Powers down CLOCK1 when low
SCLK21	19	Input	CLOCK2 frequency SELECT 1
SCLK20	20	Input	CLOCK2 frequency SELECT 0

Note 1: Has internal pull-up resistor on this pin

Block Diagram for AV9128-22





D

Decoding Tables for AV9128-22
(using 14.318 MHz input. Actual frequencies shown, in MHz)

CLOCK#1

CLK1 (Pin 1)
1.844

CLOCK#3

CLK3 (Pin 6)
23.71

CLOCK#2

SCLK21 (Pin 19)	SCLK20 (Pin 20)	CPUCLK (Pin 17)
0	0	OFF
0	1	32.21
1	0	40.00
1	1	50.11

CLOCK#4

CLK4 (Pin 7)
16.00

REFERENCE CLOCK

REFCLK (Pin 14)
14.318

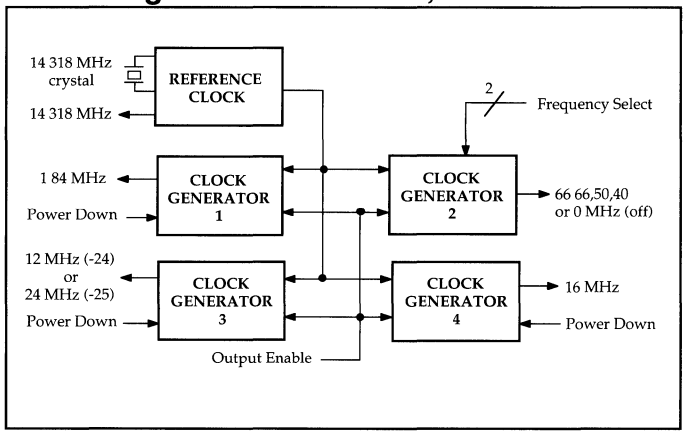
When all 4 clocks are powered down, the 14.318 MHz reference clock automatically powers down.

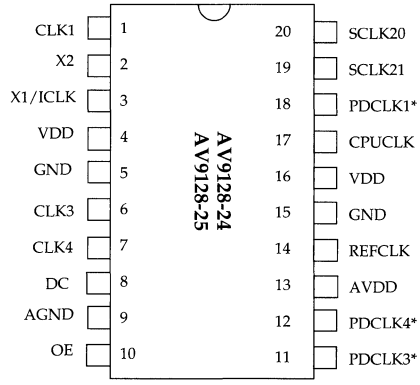
Pin Description for AV9128-24 and -25 (when using a 14.318MHz reference)

Pin Name	Pin #	Pin type	Description
CLK1	1	Output	CLOCK1 (1.84 MHz)
X2	2	Output	CRYSTAL connection for 14.318 MHz crystal. NC for clock input
X1/ICLK	3	Input	CRYSTAL connection or INPUT CLOCK
VDD	4	-	POWER SUPPLY (+5V)
GND	5	-	GROUND
CLK3	6	Output	CLOCK3 (12 MHz on AV9128-24, 24 MHz on AV9128-25)
CLK4	7	Output	CLOCK4 output (16 MHz)
DC	8	-	Don't Connect this pin
AGND	9	-	ANALOG GROUND
OE	10	Input	OUTPUT ENABLE. A low level tri-states all outputs. Note 1
PDCLK3*	11	Input	POWER DOWN. Powers down CLOCK3 when low
PDCLK4*	12	Input	POWER DOWN. Powers down CLOCK4 when low
AVDD	13	-	ANALOG POWER SUPPLY (+5V)
REFCLK	14	Output	REFERENCE CLOCK. Produces a 14.318 MHz clock.
GND	15	-	GROUND
VDD	16	-	POWER SUPPLY (+5V)
CPUCLK	17	Output	CPU CLOCK2 output (see table on following page)
PDCLK1*	18	Input	POWER DOWN. Powers down CLOCK1 when low
SCLK21	19	Input	CLOCK2 frequency SELECT 1
SCLK20	20	Input	CLOCK2 frequency SELECT 0

Note 1: Has internal pull-up resistor

Block Diagram for AV9128-24, AV9128-25





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Decoding Tables for AV9128-24, AV9128-25 (using 14.318 MHz input. Actual frequencies shown, in MHz)

CLOCK#1

CLK1 (Pin 1)
1.844

CLOCK#3

CLK3 (Pin 6)
11.86 or 23.71

CLOCK#2

SCLK21 (Pin 19)	SCLK20 (Pin 20)	CPUCLK (Pin 17)
0	0	OFF
0	1	40.00
1	0	50.11
1	1	66.58

CLOCK#4

CLK4 (Pin 7)
16.00

REFERENCE CLOCK

REFCLK (Pin 14)
14.318

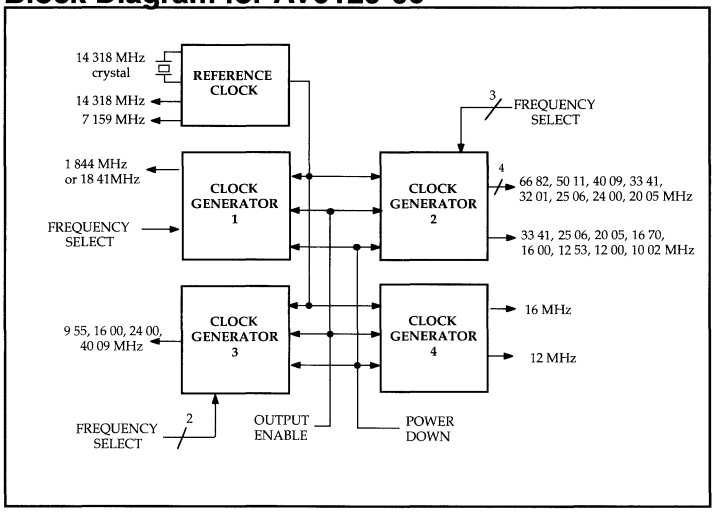
When all 4 clocks are powered down, the 14.318 MHz reference clock automatically powers down.

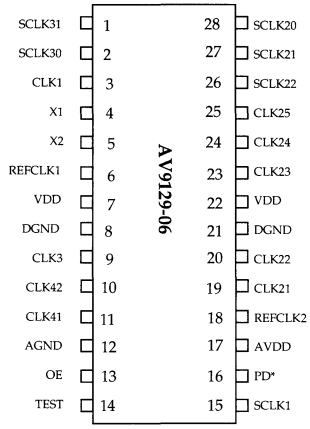
Pin Description for AV9129-06 (when using a 14.318MHz reference)

Pin Name	Pin #	Pin type	Description
SCLK31	1	Input	CLOCK3 frequency SELECT 1
SCLK30	2	Input	CLOCK3 frequency SELECT 0
CLK1	3	Output	CLOCK1 output
X1	4	Input	CRYSTAL connection for 14.318 MHz crystal, or input clock
X2	5	Output	CRYSTAL connection for 14.318 MHz crystal
REFCLK1	6	Output	REFERENCE CLOCK output #1. Produces 14.318 MHz clock
VDD	7	-	DIGITAL POWER SUPPLY (+5V)
DGND	8	-	DIGITAL GROUND
CLK3	9	Output	CLOCK3 output
CLK42	10	Output	CLOCK4 output #2
CLK41	11	Output	CLOCK4 output #1
AGND	12	-	ANALOG GROUND
OE	13	Input	OUTPUT ENABLE. A low tri-states the output clocks. Note 1
TEST	14	-	TEST. Connect to VDD or can be left floating. Note 1
SCLK1	15	Input	CLOCK1 frequency SELECT. Note 1
PD*	16	Input	POWER DOWN. A low shuts down all 4 clock generators. Note 1
AVDD	17	-	ANALOG POWER SUPPLY (+5V DC)
REFCLK2	18	Output	REFERENCE CLOCK output #2. Produces 7.159 MHz clock
CLK21	19	Output	CLOCK2 output #1
CLK22	20	Output	CLOCK2 output #2
DGND	21	-	DIGITAL GROUND
VDD	22	-	DIGITAL POWER SUPPLY (+5V)
CLK23	23	Output	CLOCK2 output #3
CLK24	24	Output	CLOCK2 output #4
CLK25	25	Output	CLOCK2 output #5
SCLK22	26	Input	CLOCK2 frequency SELECT 2
SCLK21	27	Input	CLOCK2 frequency SELECT 1
SCLK20	28	Input	CLOCK2 frequency SELECT 0

Note 1: These pins have internal pull-up resistors to maintain complete functionality when used in an AV9127 socket

Block Diagram for AV9129-06





D

Decoding Tables for AV9129-06
(using 14.318 MHz input. Actual frequencies shown, in MHz)

CLOCK#1

SCLK1 (Pin 15)	CLK1 (Pin 3)
0	18.44
1	1.844

CLOCK#2

SCLK22 (Pin 26)	SCLK21 (Pin 27)	SCLK20 (Pin 28)	CLK22-5 (Pins 20,23-25)	CLK21 (Pin 19)
0	0	0	66.63	33.32
0	0	1	50.11	25.06
0	1	0	40.09	20.05
0	1	1	33.32	16.66
1	0	0	31.98	15.99
1	0	1	25.06	12.53
1	1	0	23.98	11.99
1	1	1	20.05	10.02

CLOCK#3

SCLK31 (Pin #1)	SCLK30 (Pin #2)	CLK3 (Pin #9)
0	0	9.62
0	1	15.97
1	0	23.86
1	1	39.86

CLOCK#4

CLK41 (Pin 11)	CLK42 (Pin 10)
16.00	12.00

REFERENCE CLOCK

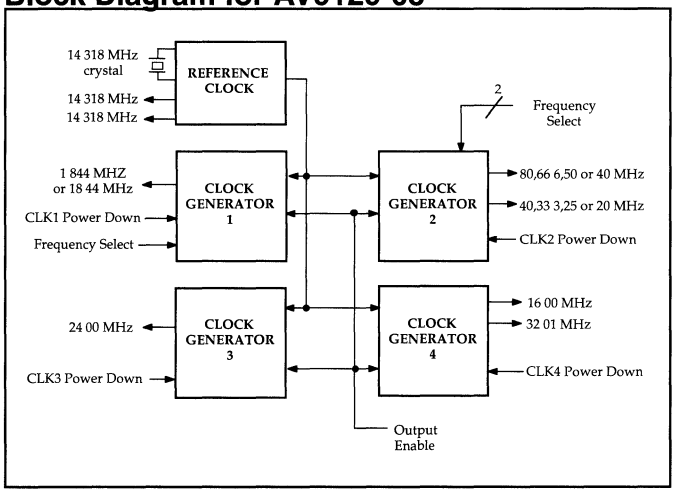
REFCLK1 (Pin 6)	REFCLK2 (Pin 18)
14.32	7.16

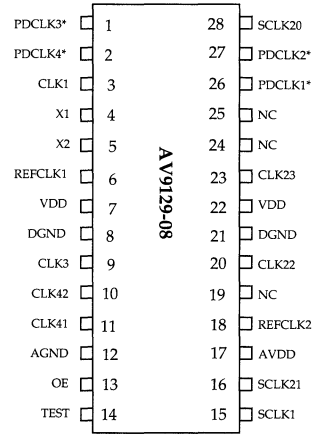
Pin Description for AV9129-08 (when using a 14.318MHz reference)

Pin Name	Pin #	Pin type	Description
PDCLK3*	1	Input	POWER DOWN CLOCK#3. Shuts off CLK3 when low
PDCLK4*	2	Input	POWER DOWN CLOCK#4. Shuts off CLK4 when low
CLK1	3	Output	CLOCK1 output
X1	4	Input	CRYSTAL connection for 14.318 MHz crystal, or input clock
X2	5	Output	CRYSTAL connection for 14.318 MHz crystal
REFCLK1	6	Output	REFERENCE CLOCK output #1. Produces 14.318 MHz clock
VDD	7	-	DIGITAL POWER SUPPLY (+5V)
DGND	8	-	DIGITAL GROUND
CLK3	9	Output	CLOCK3 output
CLK42	10	Output	CLOCK4 output #2
CLK41	11	Output	CLOCK4 output #1
AGND	12	-	ANALOG GROUND
OE	13	Input	OUTPUT ENABLE. A low tri-states the output clocks. Note 1
TEST	14	-	TEST. Connect to VDD or can be left floating. Note 1
SCLK1	15	Input	CLOCK1 frequency SELECT. Note 1
SCLK21	16	Input	CLOCK2 frequency SELECT 1. Note 1
AVDD	17	-	ANALOG POWER SUPPLY (+5V DC)
REFCLK2	18	Output	REFERENCE CLOCK output #2. Produces 14.318 MHz clock
NC	19	-	NO CONNECT
CLK22	20	Output	CLOCK2 output #2
DGND	21	-	DIGITAL GROUND
VDD	22	-	DIGITAL POWER SUPPLY (+5V)
CLK23	23	Output	CLOCK2 output #3
NC	24	-	NO CONNECT
NC	25	-	NO CONNECT
PDCLK1*	26	Input	POWER DOWN CLOCK#1. Shuts off CLK1 when low
PDCLK2*	27	Input	POWER DOWN CLOCK#2. Shuts off CLK2 when low
SCLK20	28	Input	CLOCK2 frequency SELECT 0

Note 1: These pins have internal pull-up resistors to maintain complete functionality when used in an AV9127 socket

Block Diagram for AV9129-08





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Decoding Tables for AV9129-08
(Using 14.318 MHz input. All frequencies in MHz)

REFCLK

PDCLK (1-4)*	REFCLK OUTPUT	REFCLK1 (Pin 6)	REFCLK2 (Pin 18)
0	OFF	LOW	LOW
1	ON	14.318	14.318

CLOCK#4

PDCLK4* (Pin 2)	CLK4 OUTPUTS	CLK41 (Pin 11)	CLK42 (Pin 10)
0	OFF	LOW	LOW
1	ON	32.00	16.00

CLOCK#1

PDCLK1* (Pin 26)	SCLK1 (Pin 15)	CLK1 OUTPUT	CLK1 (Pin 3)
0	X	OFF	LOW
1	0	ON	18.44
1	1	ON	1.844

CLOCK#3

PDCLK3* (Pin 1)	CLK3 OUTPUT	CLK3 (Pin 9)
0	OFF	LOW
1	ON	24.08

CLOCK#2

PDCLK2* (Pin 27)	SCLK21 (Pin 16)	SCLK20 (Pin 28)	CLK22, 23 (Pin 20,23)	CLK23 (Pin 23)	CLK 22 (Pin 20)
0	X	X	OFF	LOW	LOW
1	0	0	ON	80.05	40.03
1	0	1	ON	66.63	33.32
1	1	0	ON	50.11	25.06
1	1	1	ON	40.00	20.00

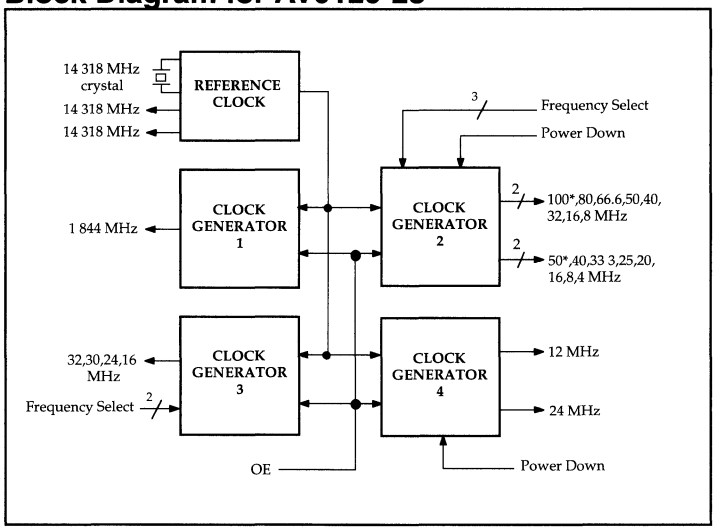
When PDCLK1*, PDCLK2*, PDCLK3*, and PDCLK4* all power down, the REFCLK automatically powers down.

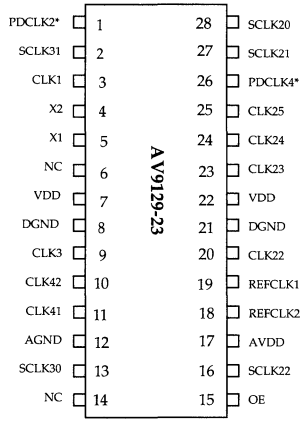
Pin Description for AV9129-23 (when using a 14.318MHz reference)

Pin Name	Pin #	Pin type	Description
PDCLK2*	1	Input	POWER DOWN. Powers down CLOCK2 when low. Note 1
SCLK31	2	Input	CLOCK3 frequency SELECT1. Note 1
CLK1	3	Output	CLOCK1 output (1.844 MHz)
X2	4	Output	CRYSTAL connection for 14.318 MHz crystal
X1	5	Input	CRYSTAL connection for 14.318 MHz crystal, or input clock
NC	6	-	NO CONNECT
VDD	7	-	DIGITAL POWER SUPPLY (+5V)
DGND	8	-	DIGITAL GROUND
CLK3	9	Output	CLOCK3 output
CLK42	10	Output	CLOCK4 output #2 (23.71 MHz)
CLK41	11	Output	CLOCK4 output #1 (11.86 MHz)
AGND	12	-	ANALOG GROUND
SCLK30	13	Input	CLOCK3 frequency SELECT0. Note 1
NC	14	-	TEST. Connect to VDD or can be left floating
OE	15	Input	OUTPUT ENABLE. All outputs are tri-stated when low. Note 1
SCLK22	16	Input	CLOCK2 frequency SELECT 2
AVDD	17	-	ANALOG POWER SUPPLY (+5V DC)
REFCLK2	18	Output	REFERENCE CLOCK output #2. Produces 14.318 MHz clock
REFCLK1	19	Output	REFERENCE CLOCK output #1. Produces 14.318 MHz clock
CLK22	20	Output	CLOCK2 output #2
DGND	21	-	DIGITAL GROUND
VDD	22	-	DIGITAL POWER SUPPLY (+5V)
CLK23	23	Output	CLOCK2 output #3
CLK24	24	Output	CLOCK2 output #4
CLK25	25	Output	CLOCK2 output #5
PDCLK4*	26	Input	POWER DOWN. Power down CLOCK4 when low. Note 1
SCLK21	27	Input	CLOCK2 frequency SELECT 1
SCLK20	28	Input	CLOCK2 frequency SELECT 0

Note 1: Has internal pull-up resistor on this pin

Block Diagram for AV9129-23





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Decoding Tables for AV9129-23
(using 14.318 MHz input. Actual frequencies shown, in MHz)

CLOCK#1

CLK1 (Pin 3)
1.844

CLOCK#2

SCLK22 (Pin 16)	SCLK21 (Pin 27)	SCLK20 (Pin 28)	CLK22,23 (Pins 20,23)	CLK24,25 (Pins 24,25)
0	0	0	7.50	3.75
0	0	1	15.51	7.75
0	1	0	32.22	16.11
0	1	1	40.09	20.04
1	0	0	50.11	25.05
1	0	1	66.54	33.27
1	1	0	80.18	40.09
1	1	1	100.23*	50.11*

CLOCK#3

SCLK31 (Pin 2)	SCLK30 (Pin 13)	CLK3 (Pin 9)
0	0	24.00
0	1	30.07
1	0	32.00
1	1	16.00

CLOCK#4

CLK41 (Pin 11)	CLK42 (Pin 10)
11.86	23.71

REFERENCE CLOCK

REFCLK1 (Pin 19)	REFCLK2 (Pin 18)
14.32	14.32

* The 1,1,1 selection does not guarantee a 100 MHz and 50 MHz output clock with the standard AV9129-23. If either of these clocks is desired, order the device as an AV9129-23Cx 28-100. The 100 MHz operation will be specially screened.

Absolute Maximum Ratings

AVDD, VDD referenced to GND..... 7V
Operating temperature under bias..... 0°C to +70°C
Storage temperature..... -40°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation..... 0.5 Watts

Note: Stresses above those listed under Absolute Maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect devices reliability

Electrical Characteristics

(V_{DD} = +5V± 10%, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage	-	-	0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0	-	-	V	V_{DD} = 5V
I_{IL}	Input Low Current	-	-	-5*	µA	V_{IN} = 0V
I_{IH}	Input High Current	-	-	5	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage	-	-	0.4	V	I_{OL} = 4mA
V_{OH}	Output High Voltage	V_{DD}-.4V	-	-	V	I_{OH} = -1mA,V_{DD}=5.0V
V_{OH}	Output High Voltage	V_{DD}-.8V	-	-	V	I_{OH} = -4mA,V_{DD}=5.0V
V_{OH}	Output High Voltage	2.4	-	-	V	1I_{OH} = -8mA
I_{CC}	Supply Current	-	45		mA	No load, AV9129-06
F_D	Output Frequency Change over Supply and Temperature	-	0.005	0.05	%	With respect to typical frequency
I_{SC}	Short circuit current	25	40		mA	Each output clock
I_{CC}	Supply Current		30		mA	No load, AV9129-08
$I_{CCSTDBY}$	Standby Supply Current		50		µA	All Clocks off
R_{PU}	Pull-up resistor value		680		kΩ	Pins 13-16 AV9129
AC Characteristics						
t_{ICr}	Input Clock Rise Time	-	-	20	ns	
t_{ICf}	Input Clock Fall Time	-	-	20	ns	
t_r	Output Rise time, 0.8 to 2.0V	-	1	2	ns	25 pf load
t_r	Rise time, 20% to 80% V_{DD}	-	2	4	ns	25 pf load
t_f	Output Fall time, 2.0 to 0.8V	-	1	2	ns	25 pf load
t_f	Fall time, 80% to 20% V_{DD}	-	2	4	ns	25 pf load
d_t	Duty cycle	43/57	48/52	57/43	%	25 pf load
d_t	Duty cycle, reference clocks	40/60	43/57	60/40	%	25 pf load
t_{jls}	Jitter, one sigma		1	3	%	As compared with
t_{jab}	Jitter, absolute		2	5	%	clock period
f_i	Input Frequency	5	14.318	32	MHz	
T_{sk}	Clock skew between any Clock #2 outputs		1	1.5	ns	
t_{pu}	Power up time		5		ms	From off to 80 MHz

* Crystal input pin will be higher, typically -10µA

Notes:
1. All clocks on AV9129-06 running at highest possible frequencies. Power supply current can change substantially with different mask configurations (see Application Note AAN02).

Ordering Information

Part Number	Temperature Range	Package Type
AV9128-xxCN20	0℃ to +70℃	20 lead Plastic DIP
AV9128-xxCW20	0℃ to +70℃	20 lead SOIC
AV9129-xxCN28	0℃ to +70℃	28 lead Plastic DIP (300 mils)
AV9129-xxCW28	0°C to +70°C	28 lead SOIC

Note: The dash number following AV9128/9, (denoted by xx above) must be included when ordering product, since it specifies the options being ordered. For 100 Mhz devices, add -100 MHz to part number.

32 kHz Motherboard Frequency Generator

General Description

The **ICS9131** offers a tiny footprint solution for generating a selectable CPU clock from a 32.768 kHz crystal. The device allows a variety of microprocessors to be clocked by changing the state of address lines FS0, FS1, and FS2. The **ICS9131** is the ideal solution for repacing high speed oscillators and for reducing clock speeds to save power in computers. The device provides smooth, glitch-free frequency transitions so that the CPU can continue to operate during slow down or speed up. The rate of frequency change makes the **ICS9161** compatible with all 386DX, 386SX, 486DX, 486DXZ, 486SX and Pentium™ microprocessors.

The **ICS9131** is driven from a single 32.768 kHz crystal. The only external components required are the crystal, crystal components, and decoupling capacitors. The device generates the 14.318 MHz system clock, eliminating the need for a 14.318 MHz crystal. High- Performance applications may require high speed clock termination components.

VDD32 Supply

The **ICS9131** has a separate power supply for the 32.768 kHz oscillator circuitry. This allows the 32 kHz clock to run from a battery or other souce while the main power to the chip is disconnected. The VDD32 supply is guaranteed to operate down to + 2.0V, with the clock consuming less than 10µA at + 3.3V with the main VDD at 0V.

The frequencies and power down options in the **ICS9131** are mask programmable. Customer specific masks can be made and prototypes delivered within 6-8 weeks from receipt of order. ICS also offers standard versions, such as those described in this data sheet.

Features

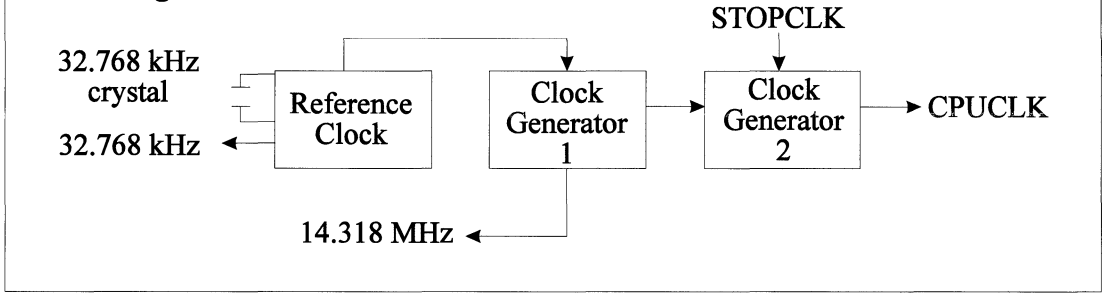
- Single 32.768 kHz crystal generates system clock and selectable CPU clock
- Generates CPU clocks from 8 MHz to 100 MHz.
- Operates from 3.3V or 5.0V supply
- Operates up to 66 MHz at 3.3V
- Separate VDD for 32 kHz clock enables it to run from battery
- STOPCLK feature allows for a smooth turn-on and turn-off of the CPU clock to static processors
- Output enable tristates outputs
- 16-pin PDIP or SOIC package

D

Applications

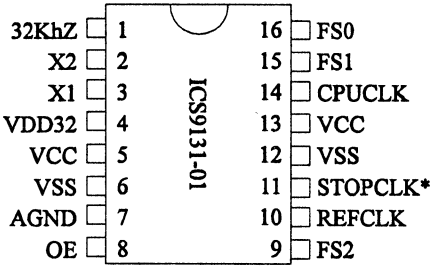
Notebook/Palmtop Computers: The **ICS9131** works with + 3V and + 5V and a single 32.768 kHz crystal, making it the ideal solution for generating clocks in portables with minimum board space. The user can save power by using this single part instead of oscillators or other frequency generators. The **ICS9131** further reduces the current consumption by having the ability to completely shut-down the individual clocks when not in used, while still maintaining the separately powered 32.768 kHz clock.

Block Diagram



Pentium is a trademark of Intel

Pin Configuration



Ordering Information
ICS9131-01CN (DIP)
ICS9131-01CM (SOIC)

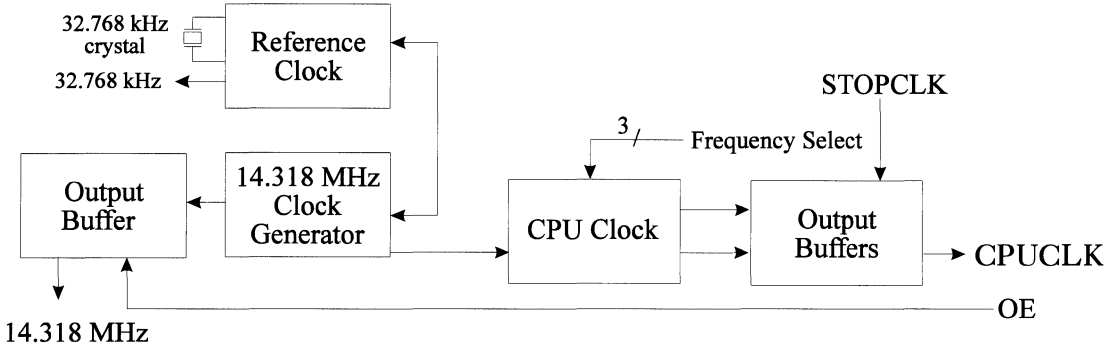
Decoding Table for CPU Clock

FS2	FS1	FS0	CPUCLK	ACTUALS
0	0	0	16	16.004
0	0	1	25	25.059
0	1	0	33.3	33.412
0	1	1	40	40.095
1	0	0	50	50.119
1	0	1	60	60.142
1	1	0	66.6	66.484
1	1	1	80	80.190

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	32 kHz	OUTPUT	32.768 kHz output
2	X2	OUTPUT	Connect 32 kHz crystal
3	X1	INPUT	Connect 32 kHz crystal
4	VDD32		Power Supply for 32 kHz oscillator
5	VCC		Power Supply (+ 3.3V - 5.0V)
6	VSS		Ground
7	AGND		Analog Ground
8	OE	INPUT	OE tristates outputs when low
9	FS2	INPUT	CPU clock frequency select 2
10	REFCLK	OUTPUT	14.318 MHz output
11	STOPCLK*	INPUT	Stops CPU Clock when low
12	VSS		Ground
13	VCC		Power supply (+ 3.3V-5.0V)
14	CPUCLK	OUTPUT	CPU Clock output (see Decoding table)
15	FS1	INPUT	CPU clock frequency select 1
16	FS0	INPUT	CPU clock frequency select 0

Block Diagram for ICS9133-01



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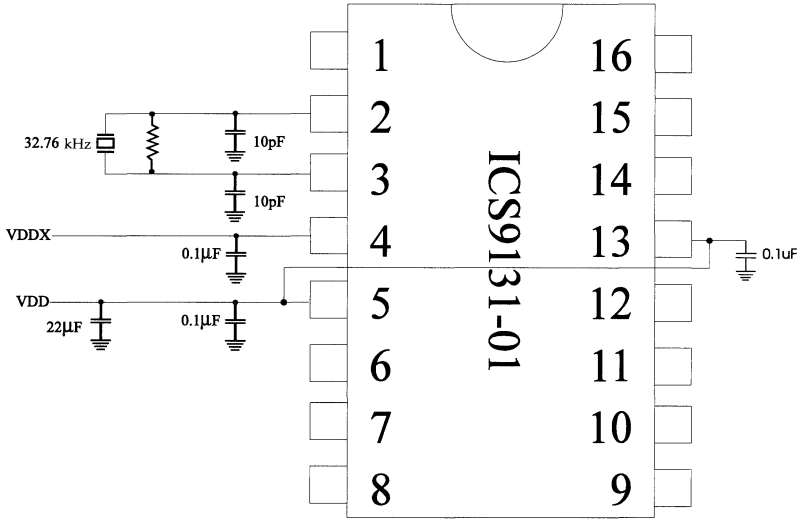
Recommended External Circuit



Notes:
1) The external components shown should be placed as close to the device as possible.
2) Pins 5 and 13 should be connected together externally. One decoupling capacitor may suffice for both pins.
3) May be part of system decoupling.
4) A 10Ω 3µF low pass filter maybe required.

Absolute Maximum Ratings

VDD referenced to GND 7V
Operating temperature under bias ..... 0°C to + 70°C
Storage temperature ..... -40°C to + 150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD+ 0.5V
Power dissipation..... 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

V_{DD} = + 3.0 to 3.7V, T_A= 0°C to 70°C unless otherwise stated)

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	V_{DD}= 3.3V	-	-	0.2V_{DD}	V
Input High Voltage	V_{IH}	V_{DD}= 3.3V	0.7V_{DD}	-	-	V
Input Low Current	I_{IL}	V_{IN}= 0V	-	-	-2*	µA
Input High Current	I_{IH}	V_{IN}= V_{DD}	-	-	2*	µA
Output Low Voltage	V_{OL}	I_{OL}= 4mA	-	-	0.1	V
Output High Voltage	V_{OH}	I_{OH}= -1mA, V_{DD}= 3.3V	V_{DD}-.1V	-	-	V
Output High Voltage	V_{OH}	I_{OH}= -4mA, V_{DD}= 3.3V	-	-	-	V
Output High Voltage	V_{OH}	I_{OH}= -8mA	2.4	-	-	V
Output Frequency Change over Supply and Temperature	F_D	With respect to typical frequency	-	.005	0.05	%
Short circuit current	I_{SC}	Each output clock		15		mA
Supply Current	I_{CC}	No load, 40 MHz		10		mA
Pull-up resistor value	R_{PU}			620		kΩ

Electrical Characteristics

V_{DD} = + 3.0 to 3.7V, T_A= 0°C to 70°C unless otherwise stated)

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Clock Rise Time	t_{ICr}		-	-	5	µs
Input Clock Fall Time	t_{ICf}			-	5	µs
Output Rise time, 0.8 to 2.0V	t_r	15 pf load	-	1.5	2	ns
Rise time, 20% to 80% V_{DD}	t_r	15 pf load	-	2.5	4	ns
Output Fall time, 2.0 to 0.8V	t_f	15 pf load	-	1.5	2	ns
Fall time, 80% to 20% V_{DD}	t_f	15 pf load	-	2.5	4	ns
Duty cycle	d_t	15 pf load	43/57	48/52	57/43	%
Duty cycle, reference clocks	d_t	15 pf load (Note 1)	40/60	43/57	60/40	%
Jitter, one sigman	t_{jis}	As compared with clock period	-	1	3	%
Jitter, absolute	t_{jab}			2	5	%
Input Frequency	f_i		25	32.768	40	kHz
Clock skew between any Clock # 2 outputs	T_{ak}			100	500	ps
Power up time	t_{pu}	From off to 40 MHz		10		ms

Note 1: 32 kHz output duty cycle is dependent on crystal used.

D

Electrical Characteristics

V_{DD} = + 5V± 10%, T_A= 0°C to 70°C unless otherwise stated)

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	V_{DD}= 3.3V	-	-	0.2V_{DD}	V
Input High Voltage	V_{IH}	V_{DD}= 3.3V	0.7V_{DD}	-	-	V
Input Low Current	I_{IL}	V_{IN}= 0V	-	-	-2*	µA
Input High Current	I_{IH}	V_{IN}= V_{DD}	-	-	2*	µA
Output Low Voltage	V_{OL}	I_{OL}= 4mA	-	-	0.1	V
Output High Voltage	V_{OH}	I_{OH}= -1mA, V_{DD}= 3.3V	V_{DD}-.1V	-	-	V
Output High Voltage	V_{OH}	I_{OH}= -4mA, V_{DD}= 3.3V	-	-	-	V
Output High Voltage	V_{OH}	I_{OH}= -8mA	2.4	-	-	V
Output Frequency Change over Supply and Temperature	F_D	With respect to typical frequency	-	.005	0.05	%
Short circuit current	I_{SC}	Each output clock		33		mA
Supply Current	I_{CC}	No load, 40 MHz		17		mA
Pull-up resistor value	R_{PU}			380		kΩ

Electrical Characteristics

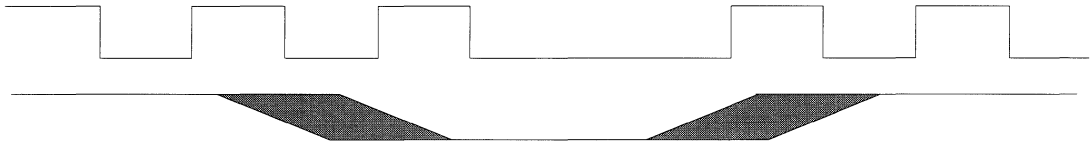
V_{DD} = + 5Væ10%, T_A= 0°C to 70°C unless otherwise stated)

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Clock Rise Time	t_{ICr}		-	-	5	µs
Input Clock Fall Time	t_{ICf}			-	5	µs
Output Rise time, 0.8 to 2.0V	t_r	15 pf load	-	1	1.5	ns
Rise time, 20% to 80% V_{DD}	t_r	15 pf load	-	2	3	ns
Output Fall time, 2.0 to 0.8V	t_f	15 pf load	-	1	1.5	ns
Fall time, 80% to 20% V_{DD}	t_f	15 pf load	-	2	3	ns
Duty cycle	d_t	15 pf load	43/57	48/52	57/43	%
Duty cycle, reference clocks	d_t	15 pf load (Note 1)	40/60	43/57	60/40	%
Jitter, one sigman	t_{jis}	As compared with clock period	-	1	3	%
Jitter, absolute	t_{jab}			2	5	%
Input Frequency	f_i		25	32.768	40	kHz
Clock skew between any Clock # 2 outputs	T_{ak}			100	500	ps
Power up time	t_{pu}	From off to 80 MHz		10		ms

Note 1: 32 kHz output duty cycle is dependent on crystal used.

Stop Clock Feature

The **ICS9131** incorporates a unique stop clock feature compatible with static logic processors. When the stop clock pin goes low, the CPUCLK will go low after the next occuring falling edge. When STOPCLK again goes high, CPUCLK resumes on the next rising edge of the internal clock. This feature enables fast, glitch-free starts and stops of the CPUCLK and is useful in Energy Star motherboard applications.



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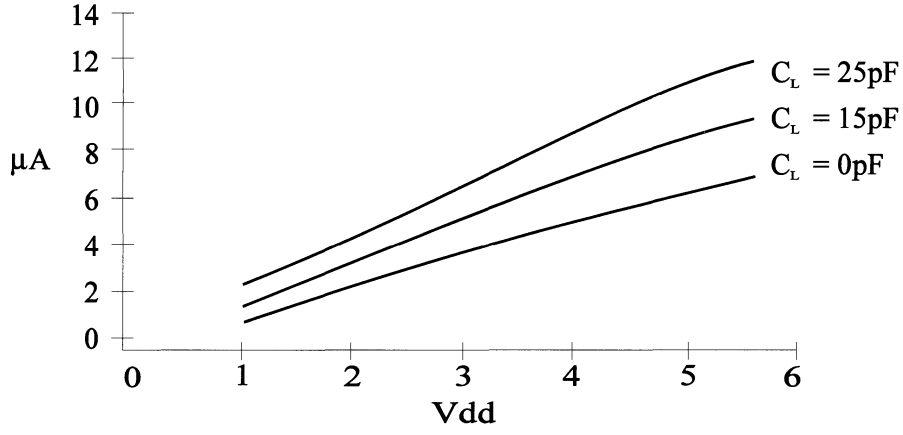
32 kHz Supply Current



ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development Characteristic data and other specifications are subject to change without notice

Integrated Circuit Systems, Inc.

ICS9132

Advance Information

32 kHz Motherboard Frequency Generator

Features

- **Single 32.768 kHz crystal generates all PC motherboard clocks**
- **Four independent clock generators**
- **Generate CPU clock from 12.5 to 100 MHz**
- **Up to 6 output clocks**
- **Each clock can be individually powered down**
- **Separate VDD for 32 kHz clock**
- **Output enable tri-states outputs**
- **On-chip loop filter components**
- **Operates from +3.3V or 5.0V supply**
- **Skew controlled 2x and 1x CPU clocks**
- **20 pin PDIP or SOIC package**

General Description

The ICS9132 is designed to generate clocks for all 286, 386, 486, Pentium and RISC based motherboards, including laptops and notebook computers. The only external components required are a 32.768 kHz crystal, crystal components, and decoupling capacitors. The device generates the 14.318 MHz system clock, eliminating the need for a 14.318 MHz crystal. High performance applications may require high speed clock termination components. The chip includes four independent clock generators plus the 32.768 kHz reference clock to produce all necessary frequencies, including real time clock/DRAM refresh, master clock, CPU clock, twice CPU clock frequency, keyboard clock, floppy disk controller clock, serial communications clock and bus clocks. Different frequencies from clocks #2, #3, and #4 can be selected using the frequency select pins, however clock #1 will be at 14.318 MHz for all standard versions.

Applications

Notebook/Palmtop Computers: The ICS9132-01 works with +3V and +5V and a single 32.768 kHz crystal, making it the ideal solution for generating clocks in portables with minimum board space. The user can save power by using this single part instead of oscillators or other frequency generators. The ICS9132 further reduces the current consumption by having the ability to completely shut down the individual clocks when not in use, while still maintaining the separately powered 32.768 kHz clock.

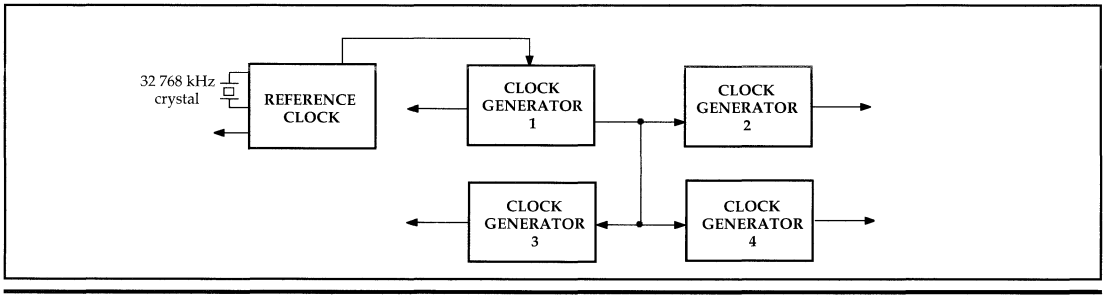
Desktop Computers: The ICS9132-03 works at 5V while saving the cost and space of oscillators. Using a single 32.768 kHz crystal, the ICS9132-03 generates all CPU and peripheral clocks found on a motherboard.

VDD32 SUPPLY

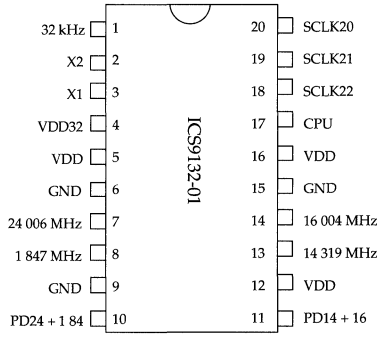
The ICS9132 has a separate power supply for the 32.768 kHz oscillator circuitry. This allows the 32 kHz clock to run from a battery or other source while the main power to the chip is disconnected. The VDD32 supply is guaranteed to operate down to +2.0V, with the clock consuming less than 10µA at +3.3V with the main VDD at 0V.

Part	Description
ICS9132-01	Notebook version
ICS9132-03	Desktop version
ICS9132-16	Pentium version with SCUZZY clock
ICS9132-18	Pentium version

Block Diagram



Pin Configuration



ICS9132-01 Decoding Table for CPU CLOCK

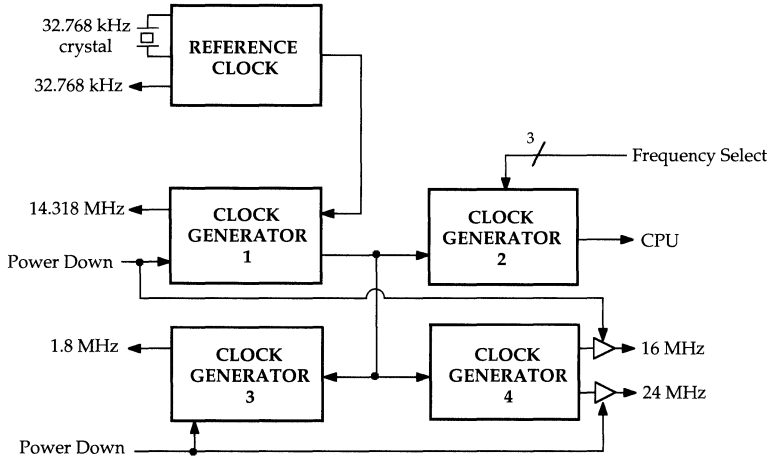
SCLK22 Pin 18	SCLK21 Pin 19	SCLK20 Pin 20	CPU (MHz) Pin 17
0	0	0	OFF
0	0	1	4.010 MHz
0	1	0	25.059
0	1	1	33.258
1	0	0	40.095
1	0	1	50.119
1	1	0	66.641*
1	1	1	80.060*

* Only at 5V supply voltage

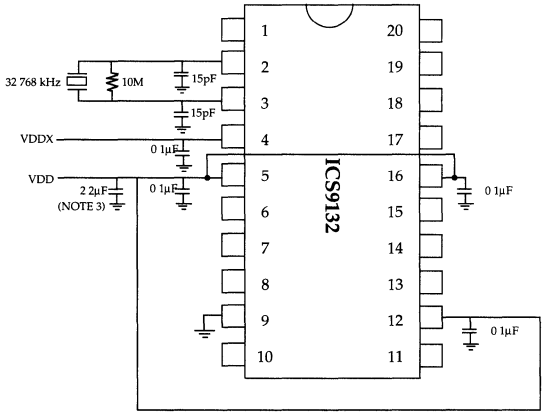
Pin Description for ICS9132-01

Pin Name	Pin #	Pin type	Description
32kHz	1	Output	32.768 kHz output
X2	2	Output	Connect 32 kHz crystal
X1	3	Input	Connect 32 kHz crystal
VDD32	4	-	Power supply for 32 kHz oscillator only
VDD	5	-	Power supply (+3.3 - +5.0V)
GND	6	-	GROUND
24.006 MHz	7	Output	24.006 MHz clock output
1.847 MHz	8	Output	1.847 MHz clock output
GND	9	-	GROUND
PD24.006 & 1.847 MHz	10	Input	POWER DOWN. Shuts off 24.006 & 1.847 MHz clocks when low
PD14 & 16 MHz	11	Input	POWER DOWN. Shuts off 14.319 & 16.004 MHz clocks when low
VDD	12	-	Power Supply (+3.3 to +5.0V)
14.319 MHz	13	Output	14.319 MHz clock output
16.004 MHz	14	Output	16.004 MHz clock output
GND	15	-	GROUND
VDD	16	-	Power Supply (+3.3 to +5.0V)
CPU	17	Output	CPU clock output (see decoding table)
SCLK22	18	Input	CPU clock frequency SELECT 2
SCLK21	19	Input	CPU clock frequency SELECT 1
SCLK20	20	Input	CPU clock frequency SELECT 0

Block Diagram for ICS9132-01

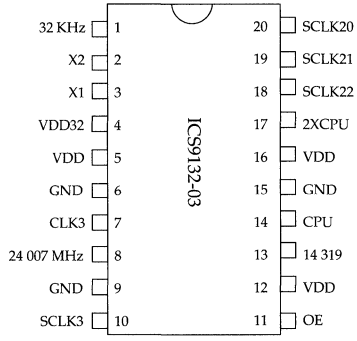


Recommended External Circuit



NOTES:
(1) The external components shown should be placed as close to the device as possible.
(2) Pins 5 and 16 should be connected together externally.
One decoupling capacitor may suffice for both pins.
(3) May be part of system decoupling.

Pin Configuration



ICS9132-03 Decoding Tables

CPU CLOCK

SCLK22 Pin 18	SCLK21 Pin 19	SCLK20 Pin 20	2x CPU (MHz) Pin 17	CPU (MHz) Pin 14
0	0	0	100.226	50.113
0	0	1	32.005	16.003
0	1	0	25.059	12.530
0	1	1	33.293	16.647
1	0	0	40.006	20.003
1	0	1	50.119	25.059
1	1	0	66.586	33.293
1	1	1	80.012*	40.006

KBD CLOCK

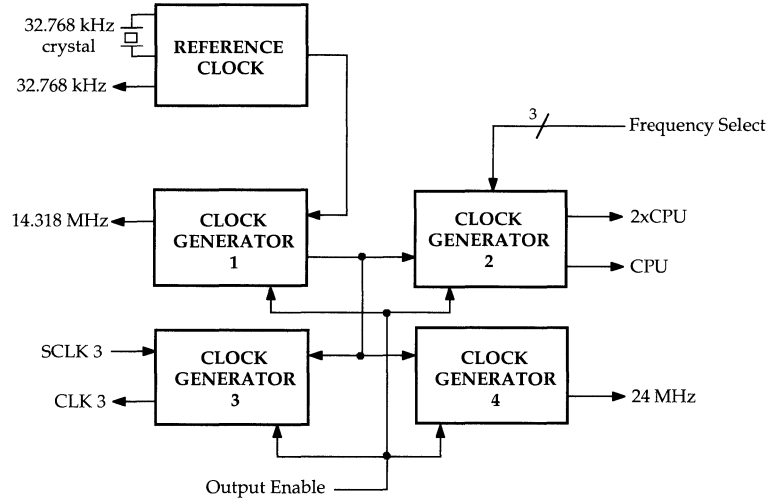
SCLK3	CLK3
0	8.002
1	12.082

* Only at 5V supply voltage

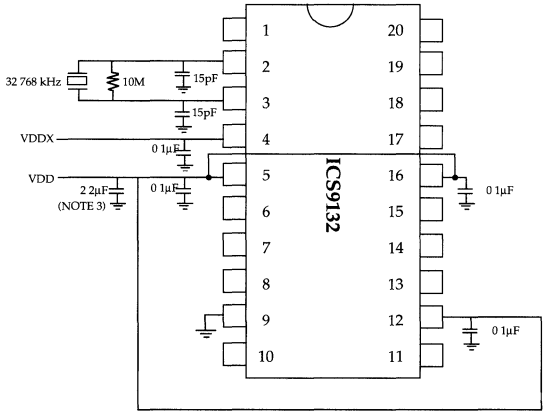
Pin Description for ICS9132-03 (5V operation. 3V available upon request)

Pin Name	Pin #	Pin type	Description
32kHz	1	Output	32.768 kHz output
X2	2	Output	Connect 32 kHz crystal
X1	3	Input	Connect 32 kHz crystal
VDD32	4	-	Power supply for 32 kHz oscillator only
VDD	5	-	Power supply (+5.0V)
GND	6	-	GROUND
CLK3	7	Output	Keyboard CLOCK 3 8 or 12 MHz output
24.007 MHz	8	Output	24.007 MHz clock output
GND	9	-	GROUND
SCLK3	10	Input	Keyboard CLOCK 3 Frequency Select. Pull-up resistor connected
OE	11	Input	OUTPUT ENABLE. A low tri-states clock outputs. Pull-up resistor connected
VDD	12	-	Power Supply (+5.0V)
14.319MHz	13	Output	14.319 MHz clock output
CPU	14	Output	CPU clock output (see decoding table)
GND	15	-	GROUND
VDD	16	-	Power Supply (+5.0V)
2xCPU	17	Output	Double frequency CPU clock output
SCLK22	18	Input	CPU clock frequency SELECT 2. Pull-up resistor connected
SCLK21	19	Input	CPU clock frequency SELECT 1. Pull-up resistor connected
SCLK20	20	Input	CPU clock frequency SELECT 0. Pull-up resistor connected

Block Diagram for ICS9132-03

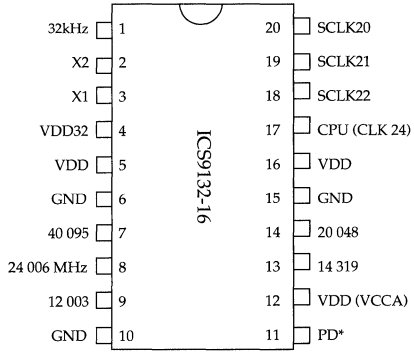


Recommended External Circuit



NOTES:
(1) The external components shown should be placed as close to the device as possible.
(2) Pins 5 and 16 should be connected together externally.
One decoupling capacitor may suffice for both pins.
(3) May be part of system decoupling.

Pin Configuration



ICS9132-16 Decoding Tables

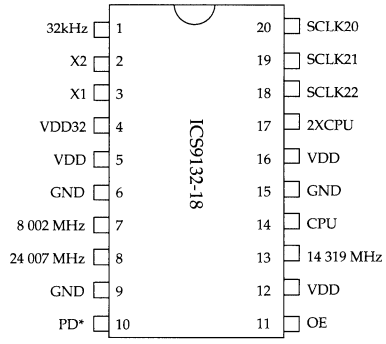
CPU CLOCK

SCLK22 Pin 18	SCLK21 Pin 19	SCLK20 Pin 20	CPU (MHz) Pin 17	
0	0	0	OFF	
0	0	1	8.055	smooth transitions
0	1	0	9.980	
0	1	1	11.858	
1	0	0	OFF	
1	0	1	50.119	smooth transitions
1	1	0	60.006	
1	1	1	66.617	

Pin Description for ICS9132-16 (5V operation. 3V available upon request)

Pin Name	Pin #	Pin type	Description
32kHz	1	Output	32.768 kHz output
X2	2	Output	Connect 32 kHz crystal
X1	3	Input	Connect 32 kHz crystal
VDD32	4	-	Power supply for 32 kHz oscillator only
VDD	5	-	Power supply (+5.0V)
GND	6	-	GROUND
40.095 MHz	7	Output	40.095 MHz SCUZZY clock output
24.006 MHz	8	Output	24.007 MHz clock output
12.003 MHz	9	Output	12.003 MHz keyboard clock output
GND	10	-	GROUND
PD*	11	Input	POWER DOWN. Forces all outputs low except 32 kHz
VDD	12	-	Power Supply (+5.0V)
14.319 MHz	13	Output	14.319 MHz clock output
20.048 MHz	14	Output	20.048 MHz clock output
GND	15	-	GROUND
VDD	16	-	Power Supply (+5.0V)
CPU	17	Output	CPU clock output (see decoding table)
SCLK22	18	Input	CPU clock frequency SELECT 2. Pull-up resistor connected
SCLK21	19	Input	CPU clock frequency SELECT 1. Pull-up resistor connected
SCLK20	20	Input	CPU clock frequency SELECT 0. Pull-up resistor connected

Pin Configuration



ICS9132-18 Decoding Tables

CPU CLOCK

SCLK22 Pin 18	SCLK21 Pin 19	SCLK20 Pin 20	2x CPU (MHz) Pin 17	CPU (MHz) Pin 14
0	0	0	59.999	29.999
0	0	1	16.002	8.001
0	1	0	25.056	12.528
0	1	1	33.255	16.627
1	0	0	39.992	19.996
1	0	1	49.896	24.948
1	1	0	66.610	33.305
1	1	1	80.012	40.006

D

Pin Description for ICS9132-18 (5V operation. 3V available upon request)

Pin Name	Pin #	Pin type	Description
32kHz	1	Output	32.768 kHz output
X2	2	Output	Connect 32 kHz crystal
X1	3	Input	Connect 32 kHz crystal
VDD32	4	-	Power supply for 32 kHz oscillator only
VDD	5	-	Power supply (+5.0V)
GND	6	-	GROUND
8.002 MHz	7	Output	8.002 MHz keyboard clock output
24.007 MHz	8	Output	24.007 MHz clock output
GND	9	-	GROUND
PD*	10	Input	POWER DOWN. All outputs go low except 32 kHz
OE	11	Input	OUTPUT ENABLE. A low tri-states clock outputs. Pull-up resistor connected
VDD	12	-	Power Supply (+5.0V)
14.319 MHz	13	Output	14.319 MHz clock output
CPU	14	Output	CPU clock output (see decoding table)
GND	15	-	GROUND
VDD	16	-	Power Supply (+5.0V)
2xCPU	17	Output	Double frequency CPU clock output
SCLK22	18	Input	CPU clock frequency SELECT 2. Pull-up resistor connected
SCLK21	19	Input	CPU clock frequency SELECT 1. Pull-up resistor connected
SCLK20	20	Input	CPU clock frequency SELECT 0. Pull-up resistor connected

Absolute Maximum Ratings

VDD referenced to GND..... 7V
Operating temperature under bias..... 0°C to +70°C
Storage temperature..... -40°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation..... 0.5 Watts

Note: Stresses above those listed under Absolute Maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect devices reliability.

Electrical Characteristics

(V_{DD} = +3.0 to 3.7V, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage	-	-	$0.2V_{DD}$	V	V_{DD} = 3.3V
V_{IH}	Input High Voltage	$0.7V_{DD}$	-	-	V	V_{DD} = 3.3V
I_{IL}	Input Low Current	-	-	-2*	µA	V_{IN} = 0V
I_{IH}	Input High Current	-	-	2*	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage	-	-	0.1	V	I_{OL} = 4mA
V_{OH}	Output High Voltage	V_{DD}-.1V	-	-	V	I_{OH} = -1mA,V_{DD}=3.3V
V_{OH}	Output High Voltage	-	-	-	V	I_{OH} = -4mA,V_{DD}=3.3V
V_{OH}	Output High Voltage	2.4	-	-	V	I_{OH} = -8mA
F_D	Output Frequency Change over Supply and Temperature	-	.005	0.05	%	With respect to typical frequency
I_{SC}	Short circuit current		15		mA	Each output clock
I_{CC}	Supply Current		10		mA	No load, 40 MHz
R_{PU}	Pull-up resistor value		620		kΩ	
AC Characteristics						
t_{ICr}	Input Clock Rise Time	-	-	5	µs	
t_{ICf}	Input Clock Fall Time	-	-	5	µs	
t_r	Output Rise time, 0.8 to 2.0V	-	1.5	2	ns	15 pf load
t_r	Rise time, 20% to 80% V_{DD}	-	2.5	4	ns	15 pf load
t_f	Output Fall time, 2.0 to 0.8V	-	1.5	2	ns	15 pf load
t_f	Fall time, 80% to 20% V_{DD}	-	2.5	4	ns	15 pf load
d_t	Duty cycle	43/57	48/52	57/43	%	15 pf load
d_t	Duty cycle, reference clocks	40/60	43/57	60/40	%	15 pf load (Note 1)
t_{jls}	Jitter, one sigma		1	3	%	As compared with
t_{jab}	Jitter, absolute		2	5	%	clock period
f_i	Input Frequency	25	32.768	40	kHz	
T_{sk}	Clock skew between any Clock #2 outputs		100	500	ps	
t_{pu}	Power up time		10		ms	From off to 40 MHz

Note 1: 32 kHz output duty cycle is dependent on crystal used.

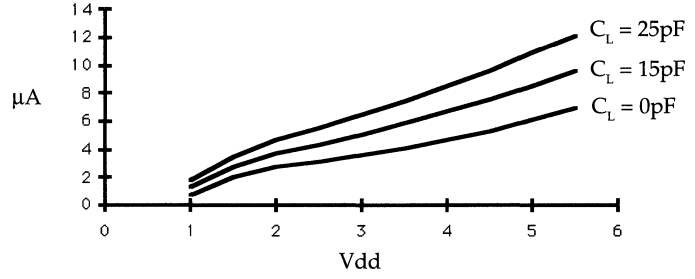
Electrical Characterisitics

(V_{DD} = +5V± 10%, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage	-	-	$0.2V_{DD}$	V	V_{DD} = 3.3V
V_{IH}	Input High Voltage	$0.7V_{DD}$	-	-	V	V_{DD} = 3.3V
I_{IL}	Input Low Current	-	-	-2*	µA	V_{IN} = 0V
I_{IH}	Input High Current	-	-	2*	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage	-	-	0.1	V	I_{OL} = 4mA
V_{OH}	Output High Voltage	V_{DD}-.1V	-	-	V	I_{OH} = -1mA,V_{DD}=3.3V
V_{OH}	Output High Voltage	-	-	-	V	I_{OH} = -4mA,V_{DD}=3.3V
V_{OH}	Output High Voltage	2.4	-	-	V	I_{OH} = -8mA
F_D	Output Frequency Change over Supply and Temperature	-	.005	0.05	%	With respect to typical frequency
I_{SC}	Short circuit current		33		mA	Each output clock
I_{CC}	Supply Current		17		mA	No load, 40 MHz
R_{PU}	Pull-up resistor value		380		kΩ	
AC Characteristics						
t_{ICr}	Input Clock Rise Time	-	-	5	µs	
t_{ICf}	Input Clock Fall Time	-	-	5	µs	
t_r	Output Rise time, 0.8 to 2.0V	-	1	1.5	ns	25 pf load
t_r	Rise time, 20% to 80% V_{DD}	-	2	3	ns	25 pf load
t_f	Output Fall time, 2.0 to 0.8V	-	1	1.5	ns	25 pf load
t_f	Fall time, 80% to 20% V_{DD}	-	2	3	ns	25 pf load
d_t	Duty cycle	43/57	48/52	57/43	%	25 pf load
d_t	Duty cycle, reference clocks	40/60	43/57	60/40	%	25 pf load (Note 1)
t_{jls}	Jitter, one sigma		1	3	%	As compared with
t_{jab}	Jitter, absolute		2	5	%	clock period
f_1	Input Frequency	25	32.768	40	kHz	
T_{sk}	Clock skew between any Clock #2 outputs		100	500	ps	
t_{pu}	Power up time		5		ms	From off to 80 MHz

Note 1: 32 kHz output duty cycle is dependent on crystal used.

32 kHz Supply Current



Ordering Information

Part Number	Temperature Range	Package Type
ICS9132-xxCN20	0°C to +70°C	20 lead Plastic DIP
ICS9132-xxCW20	0°C to +70°C	20 lead SOIC

-xx	Application	Features
-01	Notebook	Contains power down
-03	Desktop	Tri-state outsputs, 2xCPU

32 kHz Motherboard Frequency Generator

Features

- **Single 32.768 kHz crystal generates all PC motherboard clocks**
- **Cost-reduced version of popular ICS9132**
- **3 independent clock generators**
- **Generates CPU clocks from 12.5 to 100 MHz**
- **Up to 7 output clocks**
- **Separate VDD for 32 kHz clock**
- **Output enable tri-states outputs**
- **Power down options available**
- **Operates from 3.3V or 5.0V supply**
- **Operates up to 66 MHz at 3.3V**
- **Skew controlled 2x and 1x CPU clocks**
- **20 pin PDIP or SOIC package**

General Description

The ICS9133 is designed to generate clocks for all 286, 386, 486, Pentium and RISC based motherboards, including laptops and notebook computers. The only external components required are a 32.768 kHz crystal, crystal components, and decoupling capacitors. The device generates the 14.318 MHz system clock, eliminating the need for a 14.318 MHz crystal. High performance applications may require high speed clock termination components. The chip includes three independent clock generators plus the 32.768 kHz reference clock to produce all necessary frequencies, including real time clock/DRAM refresh, master clock, CPU clock, twice CPU clock frequency, keyboard clock, floppy disk controller clock, serial communications clock and bus clocks. Different frequencies from clocks #2 and #3 can be selected using the frequency select pins, but clock #1 will be at 14.318 MHz for all standard versions.

VDD32 Supply

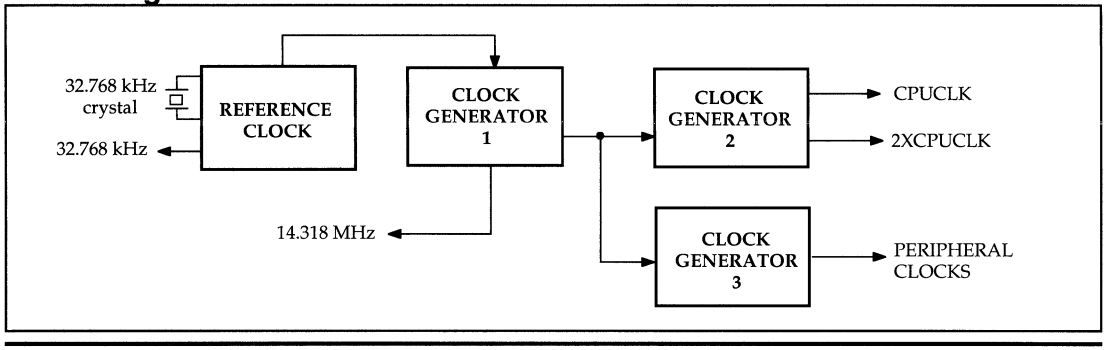
The ICS9133 has a separate power supply for the 32.768 kHz oscillator circuitry. This allows the 32 kHz clock to run from a battery or other source while the main power to the chip is disconnected. The VDD32 supply is guaranteed to operate down to +2.0V, with the clock consuming less than 10µA at +3.3V with the main VDD at 0V.

The frequencies and power down options in the ICS9133 are mask programmable. Customer specific masks can be made and prototypes delivered within 6 - 8 weeks from receipt of order. Integrated Circuit Systems also offers standard versions, such as that described in this data sheet.

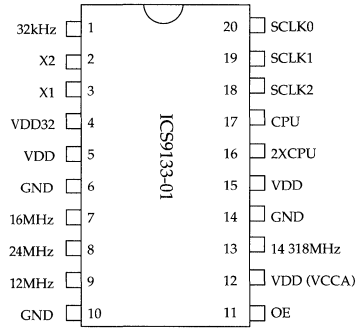
Applications

Notebook / Palmtop Computers: The ICS9133 works with +3V and +5V and a single 32.768 kHz crystal, making it the ideal solution for generating clocks in portables with minimum board space. The user can save power by using this single part instead of oscillators or other frequency generators. The ICS9133 further reduces the current consumption by having the ability to completely shut down the individual clocks when not in use, while still maintaining the separately powered 32.768 kHz clock.

Block Diagram



Pin Configuration



Decoding Table for CPU Clock

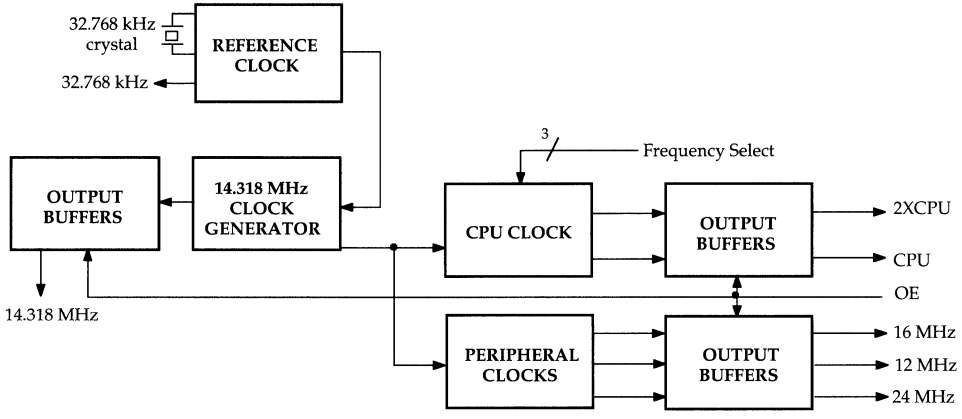
SCLK22	SCLK21	SCLK20	2XCPU	CPU
0	0	0	8	4
0	0	1	16	8
0	1	0	32	16
0	1	1	40	20
1	0	0	50	25
1	0	1	66.6	33.3
1	1	0	80*	40*
1	1	1	100*	50*

* Only at 5V supply voltage

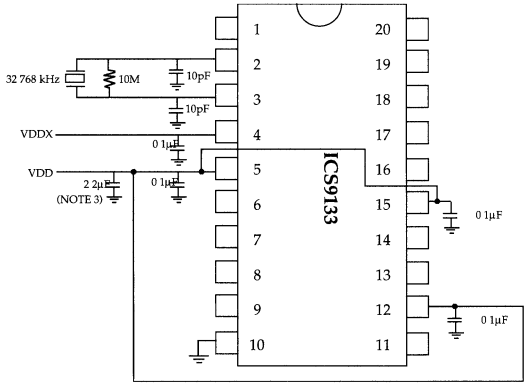
Pin Description for ICS9133

Pin Name	Pin #	Pin type	Description
32kHz	1	Output	32.768 kHz output
X2	2	Output	Connect 32 kHz crystal
X1	3	Input	Connect 32 kHz crystal
VDD32	4	-	Power supply for 32 kHz oscillator only
VDD	5	-	Power supply (+3.3 - +5.0V)
GND	6	-	GROUND
16MHz	7	Output	16 MHz clock output
24MHz	8	Output	24 MHz clock output
12MHz	9	Output	12 MHz clock output
GND	10	-	GROUND
OE	11	Input	OE tristate outputs when low
VDD	12	-	Power Supply (+3.3 to +5.0V)
14.318MHz	13	Output	14.318 MHz clock output
GND	14	-	GROUND
VDD	15	-	Power Supply (+3.3 to +5.0V)
2XCPU	16	Output	2XCPU clock output (see decoding table)
CPU	17	Output	CPU clock output (see decoding table)
SCLK2	18	Input	CPU clock frequency SELECT 2
SCLK1	19	Input	CPU clock frequency SELECT 1
SCLK0	20	Input	CPU clock frequency SELECT 0

Block Diagram for ICS9133-01



Recommended External Circuit



NOTES:
(1) The external components shown should be placed as close to the device as possible.
(2) Pins 5 and 15 should be connected together externally.
One decoupling capacitor may suffice for both pins.
(3) May be part of system decoupling.

ABSOLUTE MAXIMUM RATINGS

VDD referenced to GND..... 7V
Operating temperature under bias..... 0°C to +70°C
Storage temperature..... -40°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation..... 0.5 Watts

Note. Stresses above those listed under Absolute Maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect devices reliability.

Electrical Characteristics

(V_{DD} = +3.0 to 3.7V, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage	-	-	$0.2V_{DD}$	V	V_{DD} = 3.3V
V_{IH}	Input High Voltage	$0.7V_{DD}$	-	-	V	V_{DD} = 3.3V
I_{IL}	Input Low Current	-	-	-2*	µA	V_{IN} = 0V
I_{IH}	Input High Current	-	-	2*	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage	-	-	0.1	V	I_{OL} = 4mA
V_{OH}	Output High Voltage	V_{DD}-.1V	-	-	V	I_{OH} = -1mA,V_{DD}=3.3V
V_{OH}	Output High Voltage	-	-	-	V	I_{OH} = -4mA,V_{DD}=3.3V
V_{OH}	Output High Voltage	2.4	-	-	V	1 I_{OH} = -8mA
F_D	Output Frequency Change over Supply and Temperature	-	.005	0.05	%	With respect to typical frequency
I_{SC}	Short circuit current		15		mA	Each output clock
I_{CC}	Supply Current		10		mA	No load, 40 MHz
R_{PU}	Pull-up resistor value		620		kΩ	
AC Characteristics						
t_{ICr}	Input Clock Rise Time	-	-	5	µs	
t_{ICf}	Input Clock Fall Time	-	-	5	µs	
t_r	Output Rise time, 0.8 to 2.0V	-	1.5	2	ns	15 pf load
t_r	Rise time, 20% to 80% V_{DD}	-	2.5	4	ns	15 pf load
t_f	Output Fall time, 2.0 to 0.8V	-	1.5	2	ns	15 pf load
t_f	Fall time, 80% to 20% V_{DD}	-	2.5	4	ns	15 pf load
d_t	Duty cycle	43/57	48/52	57/43	%	15 pf load
d_t	Duty cycle, reference clocks	40/60	43/57	60/40	%	15 pf load (Note 1)
t_{jls}	Jitter, one sigma		1	3	%	As compared with clock period
t_{jab}	Jitter, absolute		2	5	%	
f_i	Input Frequency	25	32.768	40	kHz	
T_{sk}	Clock skew between any Clock #2 outputs		100	500	ps	
t_{pu}	Power up time		10		ms	From off to 40 MHz

Note 1: 32 kHz output duty cycle is dependent on crystal used.

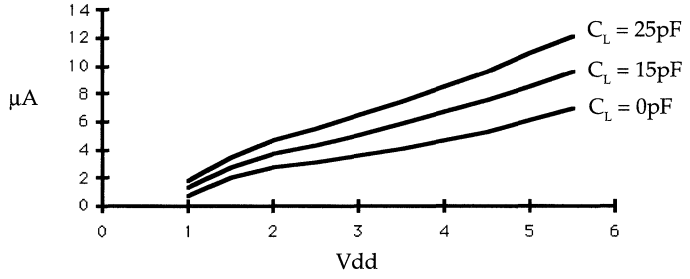
Electrical Characteristics

(V_{DD} = +5V± 10%, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage	-	-	$0.2V_{DD}$	V	V_{DD} = 3.3V
V_{IH}	Input High Voltage	$0.7V_{DD}$	-	-	V	V_{DD} = 3.3V
I_{IL}	Input Low Current	-	-	-2*	µA	V_{IN} = 0V
I_{IH}	Input High Current	-	-	2*	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage	-	-	0.1	V	I_{OL} = 4mA
V_{OH}	Output High Voltage	V_{DD}-.1V	-	-	V	I_{OH} = -1mA,V_{DD}=3.3V
V_{OH}	Output High Voltage	-	-	-	V	I_{OH} = -4mA,V_{DD}=3.3V
V_{OH}	Output High Voltage	2.4	-	-	V	I_{OH} = -8mA
F_D	Output Frequency Change over Supply and Temperature	-	.005	0.05	%	[1]With respect to typical frequency
I_{SC}	Short circuit current		33		mA	Each output clock
I_{CC}	Supply Current		17		mA	No load, 40 MHz
R_{PU}	Pull-up resistor value		380		kΩ	
AC Characteristics						
t_{ICr}	Input Clock Rise Time	-	-	5	µs	
t_{ICf}	Input Clock Fall Time	-	-	5	µs	
t_r	Output Rise time, 0.8 to 2.0V	-	1	1.5	ns	15 pf load
t_r	Rise time, 20% to 80% V_{DD}	-	2	3	ns	15 pf load
t_f	Output Fall time, 2.0 to 0.8V	-	1	1.5	ns	15 pf load
t_f	Fall time, 80% to 20% V_{DD}	-	2	3	ns	15 pf load
d_t	Duty cycle	43/57	48/52	57/43	%	15 pf load
d_t	Duty cycle, reference clocks	40/60	43/57	60/40	%	15 pf load (Note 1)
t_{jls}	Jitter, one sigma		1	3	%	As compared with
t_{jab}	Jitter, absolute		2	5	%	clock period
f_i	Input Frequency	25	32.768	40	kHz	
T_{sk}	Clock skew between any Clock #2 outputs		100	500	ps	
t_{pu}	Power up time		10		ms	From off to 80 MHz

Note 1: 32 kHz output duty cycle is dependent on crystal used.

32 kHz Supply Current



Ordering Information

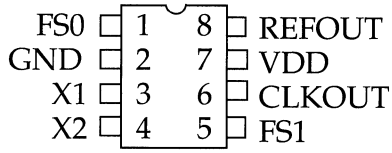
Part Number	Temperature Range	Package Type
ICS9133-01CN20	0°C to +70°C	20 lead Plastic DIP
ICS9133-01CW20	0°C to +70°C	20 lead SOIC

R4000 Frequency Generator

Features

- Ideally suited for R4000 family clock source
- Meets high and low time specifications
- Uses inexpensive 14.318 MHz reference crystal
- Selectable 50, 75 or 100 MHz output frequency
- Patented on-chip Phase Locked Loop with VCO for clock generation
- Power down frequency selection
- 8 pin DIP or SOIC package
- Low power CMOS technology
- +5 volt power supply

Pin Configuration



AV9140-01
8 pin DIP, SOIC

D

General Description

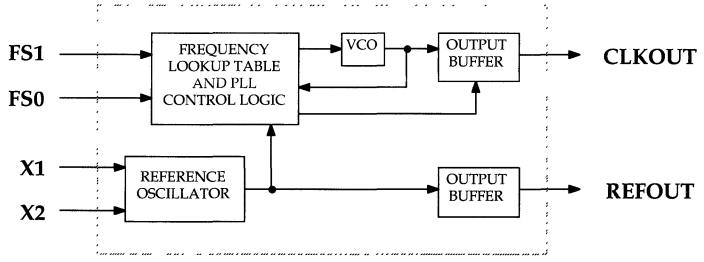
The AV9140 offers a small and inexpensive solution for generating an R4000 processor series master clock. It generates a selectable output frequency of 50, 75 or 100 MHz and generates an output waveform compatible with R4000 series master clock specifications. Output frequency is derived from a 14.318 MHz reference input clock using PLL techniques. The 14.318 reference clock can be either a discrete quartz crystal or a TTL clock signal.

The device includes an on-chip loop filter for the PLL circuit. Required external components include two decoupling capacitors and an optional ferrite bead for power supply conditioning, and two external load capacitors when a crystal reference is used. Custom masked versions, with customized frequencies and features, are available in 6-8 weeks for a small NRE.

Decoding Table for AV9140-01

Input Selection		Output Frequency	
FS1	FS0	Desired CLKOUT Frequency (MHz)	Actual CLKOUT Frequency (MHz)
0	0	OFF	OFF
0	1	50	50.113
1	0	75	74.959
1	1	100	100.227

Block Diagram



Pin Description

Pin Name	Pin #	Pin Type	Description
FS0	1	Input	FREQUENCY SELECT for CLKOUT
GND	2	-	GROUND
X1	3	Input	CRYSTAL INPUT or INPUT CLOCK frequency. Typically 14.318MHz system clock
X2	4	Output	CRYSTAL OUTPUT
FS1	5	Input	FREQUENCY SELECT for CLKOUT
CLKOUT	6	Output	CLOCK OUTPUT
VDD	7	-	Power Supply (+5V DC)
REFOUT	8	Output	REFERENCE CLOCK 14.318 MHz OUTPUT

Input Reference

The reference frequency of 14.31818 MHz was chosen since this is a common system frequency. Quartz crystals cut to this frequency are readily available and inexpensve. When using the AV9140 with a quartz crystal, the crystal is connected between pins X1 and X2. Appropriate load capacitors are also connected from X1 to ground and from X2 to ground, depending on crystal requirements. The AV9140 has an input capacitance of approximately 2.5 pF to ground at both X1 and X2. Refer to the quartz crystal data sheet for total load capacitance requirements.

When driving the AV9140 with an external clock, X1 is used as the clock input and pin X2 is left unconnected.

Power Down

When "OFF" is selected by FS2 and FS3, the chip goes into a power down mode.

Frequency Accuracy

The AV9140 uses PLL (Phase-Lock-Loop) circuitry to establish the output frequency which is based on a fixed ratio of the input frequency. The actual frequencies shown in the AV9140-01 decoding table are for when 14.31818 MHz is used as a reference frequency. Any percent error of this reference frequency will result in the same percent error in the output frequency.

Absolute Maximum Ratings

AVDD, VDD referenced to GND..... 7V
Operating temperature under bias..... 0°C to +70°C
Storage temperature..... -65°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation..... 0.5 Watts

Note. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect the reliability of the device.

Electric Characteristics

(Operating V_{DD} = +4.5V to +5.5V, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage	-	-	0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0	-	-	V	V_{DD} = 5V
I_{IL}	Input Low Current	-5	-	5	µA	V_{IN} = 0V
I_{IH}	Input High Current	-5	-	5	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage	-	-	.2 VDD	V	
V_{OH}	Output High Voltage	.8 VDD	-	-	V	
I_{DD}	Supply Current	-	10	20	mA	Note 1
I_{DD}	Supply Current	-	15	30	mA	Note 2
C_I	Input Capacitance	-	-	10	pF	Except X1
$I_{DDSTDBY}$	Standby Supply Current	-	25	-	µA	"OFF" selected
AC Characteristics						
t_w	Enable pulse width	20	-	-	ns	
t_{su}	Setup time data to enable	20	-	-	ns	
f_o	Output Frequency	8		100	MHz	
f_i	Input Frequency	2	14.318	30	MHz	
$ICLK_r$	Input Clock Rise time	-	-	20	ns	(Recommended)
$ICLK_f$	Input Clock Fall time	-	-	20	ns	(Recommended)
t_{hd}	Hold time data to enable	10	-	-	ns	
t_r	Output Rise time, 0.8 to 2.0V	-	1	2	ns	15 pf load
t_r	Rise time, 20% to 80% V_{DD}	-	1.5	3	ns	15 pf load
t_f	Output Fall time, 2.0 to 0.8V	-	1	2	ns	15 pf load
t_f	Fall time, 80% to 20% V_{DD}	-	1.5	3	ns	15 pf load
d_t	Output Duty cycle	40	48/52	60	%	15 pf load, Note 3
t_{ol}	Output Low time @ 75 MHz	3	-	-	ns	15 pf load
t_{oh}	Output High time @ 75 MHz	3	-	-	ns	15 pf load
T_{jns}	Jitter, 1 sigma	-	60	150	ns	All frequencies
T_{jabs}	Jitter, absolute	-	±250	±450	ns	All frequencies
t_{ft}	Frequency Transition time	-	-	20	ms	From 50 to 100 MHz
t_{pu}	Power up time	-	15	30	ms	From off to 100MHz

Notes
1. AV9140 with no load, with 14.318 MHz crystal input, and CLK1 running at 75 MHz. Power supply current varies with frequency. Consult Avasem for actual current at different frequencies.
2. AV9140 with 15 pF load on CLKOUT and REFOUT, CLKOUT = 100 MHz.
3. Output Duty Cycle measures using threshold voltage of 1.4 volts.

Ordering Information

Part Number	Part Marking	Temperature Range	Package Type
AV9140-01CN8	AV9140-01	0°C to +70°C	8 lead Plastic DIP (300 mils)
AV9140-01CS8	AV40-1	0°C to +70°C	8 lead SOIC (150 mils)
AV9140-01CS8T&R	AV40-1	-----	8 SOIC Tape and Reel (1000/reel)

Integrated Circuit Systems,Inc.

AV9154

Low Cost 16 Pin Frequency Generator

Features

- Compatible with 286, 386, and 486 CPUs
- Generates up to 6 output clocks for CPU plus peripherals
- Up to 100 MHz
- All loop filter components internal
- Skew controlled 2X and 1X CPU clocks
- 3V and 5V versions
- 16 pin PDIP or 150 mil wide SOIC
- Power down options

Applications

Computer Motherboards: The AV9154 replaces crystals and oscillators, saving board space, component cost, part count, and inventory costs. It produces a switchable CPU clock, and up to four fixed clocks to drive floppy disk, communications, super I/O, bus, and/or keyboard devices. The small package and 3V operation is perfect for handheld computers.

Disk Drives: The low profile, narrow SOIC package makes this a popular device for replacing expensive surface mount oscillators in space-critical disk drives.

General Description

The AV9154 is a low cost frequency generator designed for general purpose PC and disk drive applications. Its CPU clocks provide all necessary frequencies for 286, 386 and 486 systems, including support for the latest speeds of processors. The standard devices use a 14.318 MHz crystal to generate the CPU and peripheral clocks for integrated desktop and notebook motherboards.

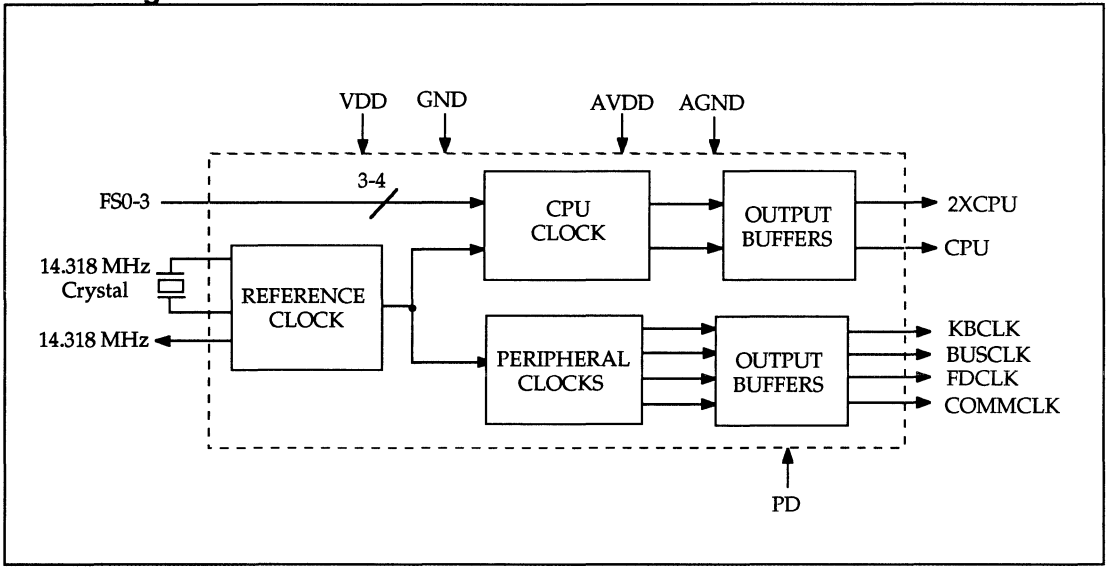
The CPU clock offers the unique feature of smooth, glitch-free transitions from one frequency to the next, making this the ideal device to use whenever slowing the CPU speed. The AV9154 makes a gradual transition between frequencies, so that it obeys the Intel cycle to cycle timing specification for 486 systems.

The simultaneous 2X and 1X CPU clocks offer controlled skew to within 1.0ns (max) of each other.

ICS has been shipping Motherboard Frequency Generators since April 1990, and is the leader in the area of multiple output clocks on a single chip. The AV9154 uses the same technology as ICS's highly successful AV9107 and AV9155 products. ICS offers a broad family of frequency generators for motherboards, graphics and other applications, including cost effective versions with only one or two output clocks. Consult ICS for all of your clock generation needs.

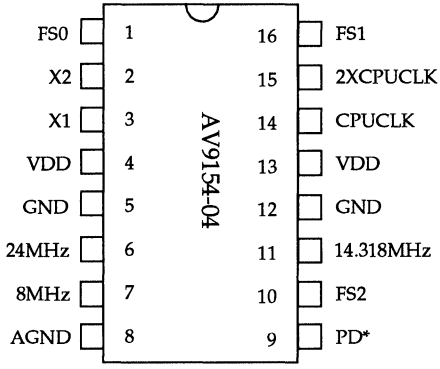
D

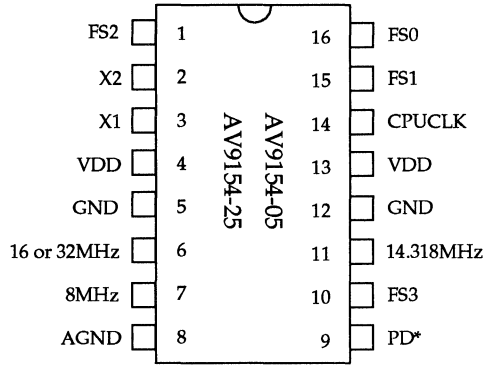
Block Diagram for AV9154

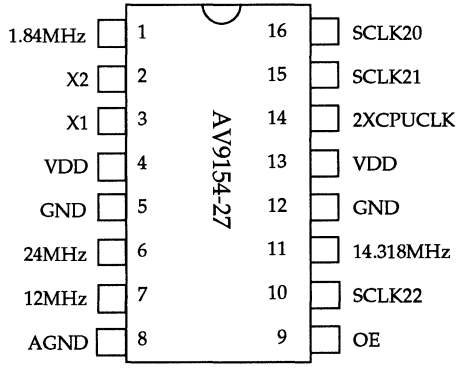


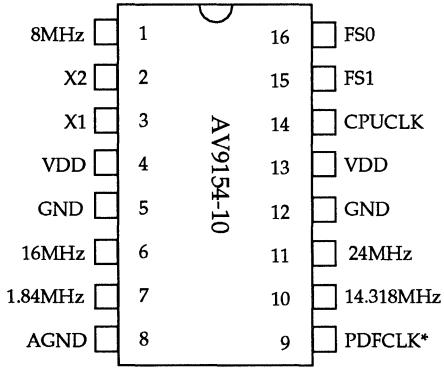
Pentium™ is a trademark of Intel Corporation

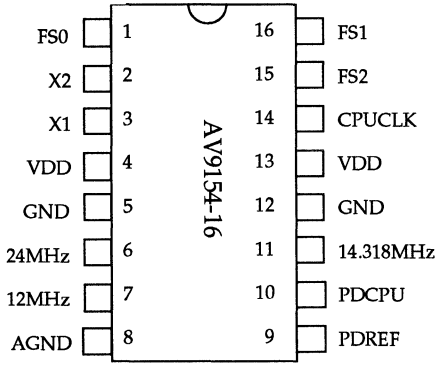
Pin Configurations











* Active low

Pin Description for AV9154-04, -05, -10, -16, -25, -27

Pin Name	Pin Type	Description	Pin # -04	-05	-10	-16	-25	-27
VDD	P	Digital Power (+3.3V or +5V)	4	4	4	4	4	4
VDD	P	Digital Power (+3.3V or +5V)	13	13	13	13	13	13
GND	P	Digital GROUND	5	5	5	5	5	5
GND	P	Digital GROUND	12	12	12	12	12	12
AGND	P	ANALOG GROUND	8	8	8	8	8	8
FS0	I	FREQUENCY SELECT 0 for CPUCLK	1	16	16	1	16	16
FS1	I	FREQUENCY SELECT 1 for CPUCLK	16	15	15	16	15	15
FS2	I	FREQUENCY SELECT 2 for CPUCLK	10	1	-	15	1	10
FS3	I	FREQUENCY SELECT 3 for CPUCLK	-	10	-	-	10	-
PDREF	I	POWER DOWN REFERENCE Clock (14.318 MHz) (Active High)	-	-	-	9	-	-
PDCPU	I	POWER DOWN CPU Clock (Active High)	-	-	-	10	-	-
PD*	I	POWER DOWN All (Active Low)	9	9	-	-	9	-
PDFCLK*	I	POWER DOWN FIXED CLOCK (1.84, 8, 16, 24)	-	-	9	-	-	-
X1	I	CRYSTAL IN	3	3	3	3	3	3
X2	O	CRYSTAL OUT	2	2	2	2	2	2
32MHz	O	32 MHz clock output	-	-	-	-	6	-
24MHz	O	24 MHz clock output	6	-	11	6	-	6
16MHz	O	16 MHz clock output	-	6	6	-	-	-
12MHz	O	12 MHz clock output	-	-	-	7	-	7
8MHz	O	8 MHz clock output	7	7	1	-	7	-
1.84MHz	O	1.84 MHz clock output	-	-	7	-	-	1
14.318MHz	O	14.318 MHz reference clock output	11	11	10	11	11	11
CPUCLK	O	CPU CLOCK output determined by status of FS0 - FS3	14	14	14	14	14	-
2XCPUCLK	O	2X CPU CLOCK output	15	-	-	-	-	14

*Active Low

D

Clock Tables in MHz
(All parts shown will operate at 3V)

FS(3:0)	-04		-05	-10	-16	-25	-27
	2XCPU	CPU	CPUCLK	CPUCLK	CPUCLK	CPUCLK	CPUCLK
0	100*	50*	2	PDCPU	16	2	75
1	80*	40*	8	40	20	8	32
2	66.6*	33.3*	16	50	25	16	60
3	50	25	20	66.6*	33.3	20	40
4	40	20	25	-	40	25	50
5	32	16	33.3*	-	50	33.3*	66.66
6	24	12	40*	-	66.6*	40*	80
7	16	8	50*	-	80*	50*	52
8	-	-	4	-	-	4	-
9	-	-	16	-	-	16	-
A	-	-	32	-	-	32	-
B	-	-	40	-	-	40	-
C	-	-	50	-	-	50	-
D	-	-	66.6*	-	-	66.6*	-
E	-	-	80*	-	-	80*	-
F	-	-	100*	-	-	100*	-
Floppy	24		-	24	24	-	24
Bus	-		16	16	-	32	-
Kybd	8		8	8	12	8	12
Comm	-		-	1.84	-	-	1.84
Refclk	14.318		14.318	14.318	14.318	14.318	14.318
3V	up to 50 MHz		up to 50 MHz	up to 50 MHz	up to 50 MHz	up to 50 MHz	up to 50 MHz

Smooth Transitions

Smooth Transitions

* These selections will only operate at 5V

Actual Output Frequencies
(using 14.318 MHz input. All frequencies in MHz)

FS(3:0)	-04		-05	-10	-16	-25	-27
	2XCPU	CPU	CPUCLK	CPUCLK	CPUCLK	CPUCLK	2XCPUCLK
0	100.23*	50.11*	2.15	PDCPU	16.11	2.15	75.17
1	80.18*	40.09*	8.18	40.09	20.05	8.18	31.94
2	66.48*	33.24*	16.11	50.11	25.06	16.11	60.136
3	50.11	25.06	20.05	66.48*	33.41	20.05	40.09
4	40.09	20.05	25.06	-	40.09	25.06	50.11
5	32.22	16.11	33.24*	-	50.11	33.24*	66.48
6	24.23	12.12	40.09*	-	66.48*	40.09*	80.18
7	15.75	7.88	50.11*	-	80.18*	50.11*	51.90
8	-	-	4.30	-	-	4.30	-
9	-	-	16.11	-	-	16.11	-
A	-	-	32.22	-	-	32.22	-
B	-	-	40.09	-	-	40.09	-
C	-	-	50.11	-	-	50.11	-
D	-	-	66.48*	-	-	66.48*	-
E	-	-	80.18*	-	-	80.18*	-
F	-	-	100.23*	-	-	100.23*	-
Floppy	24.00		-	24.00	24.00	-	24
Bus	-		16.00	16.00	-	32.01	-
Kybd	8.00		8.00	8.00	12.00	8.00	12
Comm	-		-	1.846	-	-	1.846
Refclk	14.318		14.318	14.318	14.318	14.318	14.318

Smooth Transitions

Smooth Transitions

D

* These selections will only operate at 5V

Absolute Maximum Ratings

VDD referenced to GND..... 7V
Operating temperature under bias..... 0°C to +70°C
Storage temperature..... -40°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation..... 0.5 Watts

Note: Stresses above those listed under Absolute Maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect devices reliability.

Electrical Characterisitcs at 5V

(V_{DD} = +5V± 10%, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage			0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0			V	V_{DD} = 5V
I_{IL}	Input Low Current			-5	µA	V_{IN} = 0V
I_{IH}	Input High Current			5	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4mA
V_{OH}	Output High Voltage	V_{DD}-.4V			V	I_{OH} = -1mA,V_{DD}=5.0V
V_{OH}	Output High Voltage	V_{DD}-.8V			V	I_{OH} = -4mA,V_{DD}=5.0V
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -8mA
I_{DD}	Supply Current		25	40	mA	[1]No load
F_D	Output Frequency Change over Supply and Temperature		0.002	0.01	%	With respect to typical frequency
I_{SC}	Short circuit current	25	40		mA	Each output clock
C_i	Input Capacitance			10	pF	Except X1, X2
C_L	Load Capacitance		20		pF	Pins X1, X2
I_{DDSTBY}	Supply Current, power down		30		µA	
AC Characteristics						
t_{ICr}	Input Clock Rise Time			20	ns	
t_{ICf}	Input Clock Fall Time			20	ns	
t_r	Output Rise time, 0.8 to 2.0V	-	1	2	ns	15 pf load
t_r	Rise time, 20% to 80% V_{DD}	-	2	4	ns	15 pf load
t_f	Output Fall time, 2.0 to 0.8V	-	1	2	ns	15 pf load
t_f	Fall time, 80% to 20% V_{DD}	-	2	4	ns	15 pf load
d_t	Duty cycle	40/60	48/52	60/40	%	15 pf load
d_t	Duty cycle, reference clocks	40/60	43/57	60/40	%	15 pf load
t_{jls}	Jitter, one sigma		0.8	2.5	%	As compared with
t_{jab}	Jitter, absolute		2	5	%	clock period
t_{jab}	Jitter, absolute			700	ps	16-100 MHz clocks
f_i	Input Frequency		14.318		MHz	
T_{sk}	Clock skew between CPU and 2XCPU outputs		0.5	1.0	ns	AV9154-04
t_{ft}	Frequency Transition time		15	20	ms	From 8 to 100 MHz

Notes:

1. All clocks on AV9154-05 running at highest possible frequencies. Power supply current can change substantially with different mask configurations. Consult ICS.

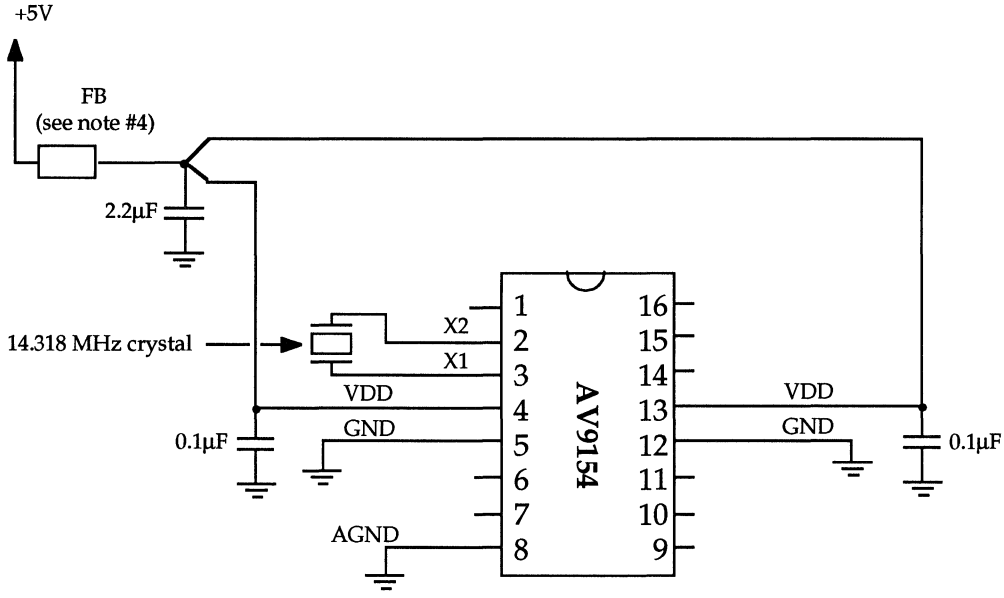
Electrical Characteristics at 3.3V

(Operating V_{DD} = +2.7V to +3.7V, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage	-	-	$0.15V_{DD}$	V	
V_{IH}	Input High Voltage	$0.7V_{DD}$	-	-	V	
I_{IL}	Input Low Current	-5	-	5	µA	V_{IN} = 0V
I_{IH}	Input High Current	-5	-	5	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage	-	-	0.1	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	V_{DD}-.1V	-	-	V	I_{OH} = -4mA
I_{DD}	Supply Current	-	15		mA	Note 1
F_d	Output Frequency Change over Supply and Temperature	-	0.002	0.01	%	With respect to typical frequency
C_i	Input Capacitance			10	pF	Except X1, X2
C_L	Load Capacitance		20		pF	Pins X1, X2
$I_{DDSTDBY}$	Supply Current, Standby		15		µA	When powered down
I_{SC}	Short Circuit Current		30		mA	
AC Characteristics						
t_w	Enable pulse width	20	-	-	ns	
t_{su}	Setup time data to enable	20	-	-	ns	
$ICLK_r$	Input Clock Rise time	-	-	20	ns	
$ICLK_f$	Input Clock Fall time	-	-	20	ns	
t_{hd}	Hold time data to enable	10	-	-	ns	
t_r	Rise time	-	-	4	ns	15 pf load
t_f	Fall time	-	-	4	ns	15 pf load
d_t	Duty cycle	40	48/52	60	%	15 pf load
T_{jis}	Jitter, 1 sigma		±0.5	±2	%	All frequencies
T_{jabs}	Jitter, absolute		±3	±5	%	All frequencies
t_{ft}	Frequency Transition time			20	ms	From 2 to 25 MHz
t_{pu}	Power up time		15		ms	From off to 50 MHz
f_o	Output Frequency	2		50	MHz	
f_i	Input Frequency	2	14.318	32	MHz	

Note 1: AV9154 with no load, with 14.318 MHz crystal input, and CLK1 running at 40 MHz. Power supply current varies with frequency. Consult ICS for actual current at different frequencies.

AV9154
Recommended External Circuit



Notes:

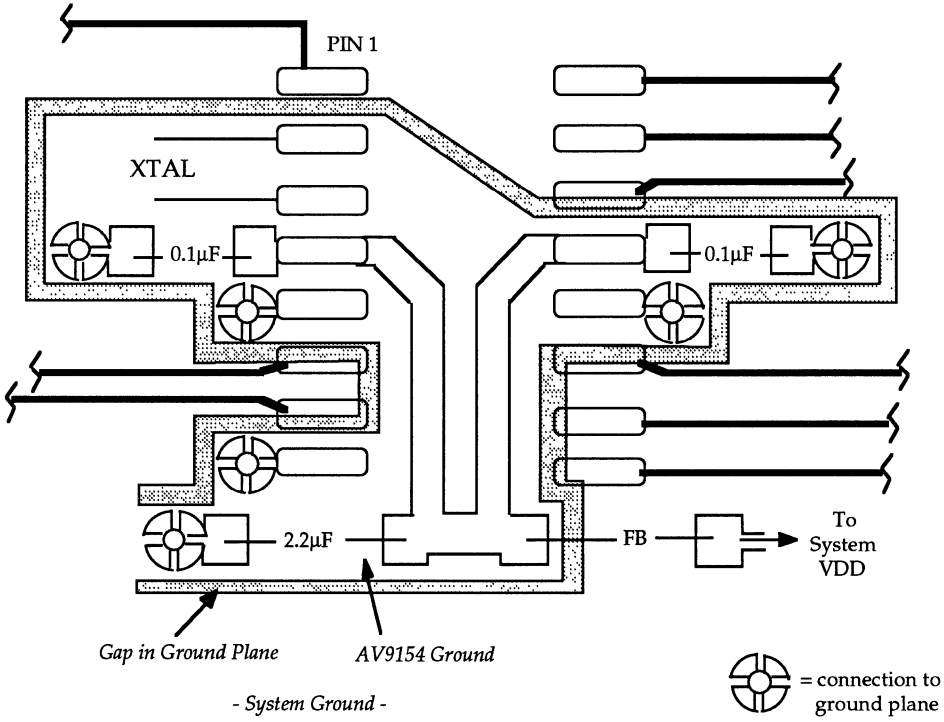
1. Avasem recommends the use of an isolated ground plane for the AV9154.
All grounds shown on this drawing should be connected to this ground plane.
This ground plane should be connected to the system ground plane at a single point.
Please refer to AV9154 Board Layout diagram.

2. A single power supply connection for all VDD lines at the 2.2 µF decoupling capacitor is recommended to reduce interaction of analog and digital circuits. The 0.1 µF decoupling capacitors should be located as close to each VDD pin as possible.

3. A 33 Ω series termination resistor should be used on any clock output which drives more than one load or drives a long trace (more than about 2 inches), especially when using high frequencies (>50 MHz). This termination resistor is put in series with the clock output line close to the clock output. It helps improve jitter perfomance and reduce EMI by damping standing waves caused by impedance mismatches in the output clock circuit trace.

4. The ferrite bead does not enhance the performance of the AV9154, but will reduce EMI radiation from the VDD line.

AV9154 Recommended Board Layout



This is the recommended layout for the AV9154 to maximize clock performance. Shown are the power and ground connections, the ground plane, and the input/output traces.

Use of the isolated ground plane and power connection, as shown, will prevent stray high frequency ground and system noise from propagating through the device. When compared to using the system ground and power planes, this technique will minimize output clock jitter. The isolated ground plane should be connected to the system ground plane at one point, near the 2.2µF decoupling cap. For lowest jitter performance, this isolated ground plane should be kept away from clock output pins and traces. Keeping the isolated ground plane area as small as possible will minimize EMI radiation. Use a sufficient gap between the isolated ground plane and system ground plane to prevent AC coupling. The ferrite bead in the VDD line optional, but will help reduce EMI.

The traces to distribute the output clocks should be over a system ground or power supply plane. The trace width should be about two times the thickness of the PC board between the trace and the underlying plane. These guidelines help minimize clock jitter and EMI radiation. The traces to distribute power should be as wide as possible.

Ordering Information

Part Number	Temperature Range	Package Type
AV9154-xxCN16	0°C to +70°C	16 lead Plastic DIP
AV9154-xxCS16	0°C to +70°C	16 lead 150 mil wide SOIC

Note: The dash number following AV9154, (denoted by xx above) must be included when ordering product, since it specifies the options being ordered.

Part Marking

ICS
AV9154-xxCx16
Date code/Lot code

OPTi Notebook Frequency Generator

Features

- **Compatible with 286, 386, and 486 CPUs**
- **Up to 66.6 MHz (-60) or 80 MHz (-06) CPU clocks**
- **All loop filter components internal**
- **3V and 5V operation**
- **16 pin 150 mil wide SOIC**
- **Power down control of CPU clock**

Applications

Computer Motherboards: The AV9154 replaces crystals and oscillators, saving board space, component cost, part count, and inventory costs. It produces a switchable CPU clock, and up to four fixed clocks to drive floppy disk, communications, super I/O, bus, and/or keyboard devices. The small package and 3V operation is perfect for handheld computers.

General Description

The AV9154 is a low cost frequency generator designed for general purpose PC and disk drive applications. Its CPU clocks provide all necessary frequencies for 286, 386 and 486 systems, including support for the latest speeds of processors. The standard devices use a 14.318 MHz crystal to generate the CPU and peripheral clocks for integrated desktop and notebook motherboards.

The AV9154-06 and AV9154-60 are specifically designed for use with OPTi core logic chip sets. The only noticeable difference between the two parts is in their CPU clock selection tables as shown on page 3.

The AV9154-06 and AV9154-60 can operate at 5.0V±10% or 3.3V±10%, but the CPU frequencies are limited (see the asterisks on the selection tables on page 3) during 3.3V operation. The parts have two power down pins. One shuts off the CPU clock to a low state when the power down pin is taken high, and the other turns off the 14.318 MHz output in the same manner.

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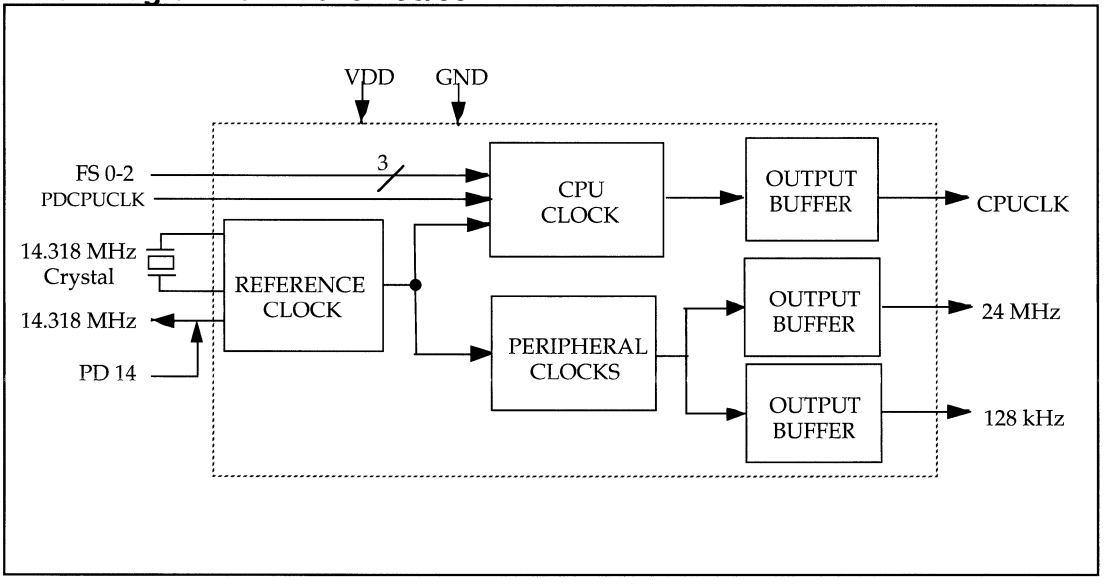
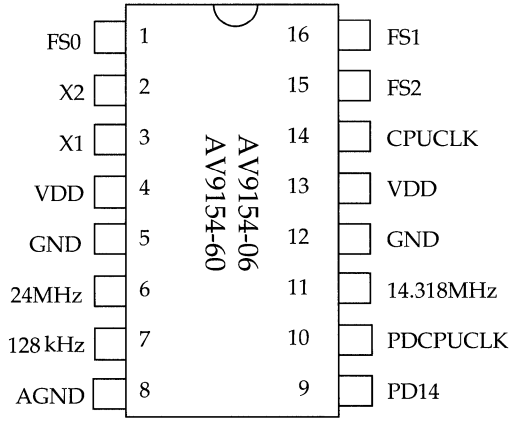
Block Diagram for AV9154-06/60



Pin Configurations



Pin Description for AV9154-06/60

PIN NAME	PIN #	PIN TYPE	DESCRIPTION
FS0	1	I	FREQUENCY SELECT 0 for CPUCLK
X2	2	O	Crystal out. Connect a 14.318 MHz crystal to this pin
X1	3	I	Crystal in. Connect a 14.318 MHz crystal to this pin
VDD	4	P	Digital Power (+3.3V or +5V)
GND	5	P	Digital GROUND
24MHz	6	O	24 MHz clock output
128 kHz	7	O	128 kHz clock output
AGND	8	P	ANALOG GROUND
PD14	9	I	POWER DOWN 14.318 MHz output (Active High)
PDCPUCLK	10	I	POWER DOWN CPU CLOCK (Active High)
14.318MHz	11	O	14.318 MHz reference clock output
GND	12	P	Digital GROUND
VDD	13	P	Digital Power (+3.3V or +5V)
CPUCLK	14	O	CPU CLOCK output determined by status of FS0 - FS2
FS2	15	I	FREQUENCY SELECT 2 for CPUCLK
FS1	16	I	FREQUENCY SELECT 1 for CPUCLK

Clock Tables for AV9154-06/60 (in MHz)

FS(2:0)	-06 CPUCLK	-60 CPUCLK
0	16	8
1	20	16
2	25	20
3	33.33	25
4	40	33.33
5	50	40*
6	66.66	50*
7	80*	66.66*

D

Actual Output Frequencies (in MHz)

FS(2:0)	-06 CPUCLK	-60 CPUCLK
0	16.11	8.182
1	20.05	16.11
2	25.06	20.05
3	33.24	25.06
4	40.09	33.24
5	50.11	40.09*
6	66.48	50.11*
7	80.18*	66.48*

* These selections will only operate at 5V

Absolute Maximum Ratings

VDD referenced to GND..... 7V
Operating temperature under bias..... 0°C to +70°C
Storage temperature..... -40°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation..... 0.5 Watts

Note. Stresses above those listed under Absolute Maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect devices reliability.

Electrical Characterisitcs at 5V

(V_{DD} = +5V± 10%, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage			0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0			V	V_{DD} = 5V
I_{IL}	Input Low Current			-5	µA	V_{IN} = 0V
I_{IH}	Input High Current			5	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4mA
V_{OH}	Output High Voltage	V_{DD}-.4V			V	I_{OH} = -1mA
V_{OH}	Output High Voltage	V_{DD}-.8V			V	I_{OH} = -4mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -8mA
I_{DD}	Supply Current		25	40	mA	[1]No load
F_D	Output Frequency Change over Supply and Temperature		0.002	0.01	%	With respect to typical frequency
I_{SC}	Short circuit current	25	40		mA	Each output clock
C_I	Input Capacitance			10	pF	Except X1, X2
C_L	Load Capacitance		20		pF	Pins X1, X2
I_{DDSTBY}	Supply Current, lowest		20		mA	When powered down
AC Characteristics						
t_{ICr}	Input Clock Rise Time			20	ns	
t_{ICf}	Input Clock Fall Time			20	ns	
t_r	Output Rise time, 0.8 to 2.0V	-	1	2	ns	15 pf load
t_r	Rise time, 20% to 80% V_{DD}	-	2	4	ns	15 pf load
t_f	Output Fall time, 2.0 to 0.8V	-	1	2	ns	15 pf load
t_f	Fall time, 80% to 20% V_{DD}	-	2	4	ns	15 pf load
d_t	Duty cycle	40/60	48/52	60/40	%	15 pf load
d_t	Duty cycle, reference clock	40/60	43/57	60/40	%	15 pf load
d_t	Duty cycle, CPU clock -06	40/60	42/58	60/40	%	15 pf load
T_{jls}	Jitter, one sigma		±0.8	±2.5	%	As compared with clock period
T_{jab}	Jitter, absolute		±2	±5	%	
T_{jab}	Jitter, absolute			700	ps	16-80 MHz clocks
f_i	Input Frequency		14.318		MHz	
t_{ft}	Frequency Transition time		15	20	ms	From 16 to 80 MHz
t_{pu}	Power up time		15		ms	From off to 50 MHz

Note 1. All clocks on AV9154-06 or -60 running at highest possible frequencies

Electrical Characteristics at 3.3V

(Operating V_{DD} = +3.0V to +3.7V, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage	-	-	$0.15V_{DD}$	V	
V_{IH}	Input High Voltage	$0.7V_{DD}$	-	-	V	
I_{IL}	Input Low Current	-5	-	5	µA	V_{IN} = 0V
I_{IH}	Input High Current	-5	-	5	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage	-	-	0.1	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	V_{DD}-.1V	-	-	V	I_{OH} = -4mA
I_{DD}	Supply Current	-	15		mA	Note 1
F_d	Output Frequency Change over Supply and Temperature	-	0.002	0.01	%	With respect to typical frequency
C_i	Input Capacitance			10	pF	Except X1, X2
C_L	Load Capacitance		20		pF	Pins X1, X2
I_{DDL}	Supply Current, Lowest		14		mA	When powered down
I_{SC}	Short Circuit Current		30		mA	
AC Characteristics						
t_{ICr}	Input Clock Rise Time			20	ns	
t_{ICf}	Input Clock Fall Time			20	ns	
t_r	Rise time	-	-	4	ns	15 pf load
t_f	Fall time	-	-	4	ns	15 pf load
d_t	Duty cycle, fixed clocks	40/60	48/52	60/40	%	15 pf load
d_t	Duty cycle, CPU clock -06	40/60	42/58	60/40	%	15 pf load
d_t	Duty cycle, reference clock	40/60	43/57	60/40	%	15 pf load
T_{Jls}	Jitter, 1 sigma		±0.5	±2	%	All frequencies
T_{Jabs}	Jitter, absolute		±3	±5	%	All frequencies
t_{ft}	Frequency Transition time			20	ms	From 8 to 33 MHz
t_{pu}	Power up time		15		ms	From off to 50 MHz
f_o	Output Frequency	2		33	MHz	Will operate up to 50MHz for -06 version
f_i	Input Frequency		14.318		MHz	

Note 1: AV9154 with no load, with 14.318 MHz crystal input, and CPUCLK running at 33 MHz. Power supply current varies with frequency. Consult ICS for actual current at different frequencies

Ordering Information

Part Number	Temperature Range	Package Type
AV9154-xxCS16	0°C to +70°C	16 lead 150 mil wide SOIC

Note: The dash number following AV9154, (denoted by xx above) must be included when ordering product, since it specifies the options being ordered.

Low Cost 20 Pin Frequency Generator

Features

- Compatible with 286, 386, and 486 CPUs
- Supports Turbo modes
- Generates communications clock, keyboard clock, floppy disk clock, system reference clock, bus clock and CPU clock
- Output Enable tri-states outputs
- Up to 100 MHz
- 20 pin DIP or SOIC
- All loop filter components internal
- Skew controlled 2X and 1X CPU clocks
- Power Down option

General Description

The AV9155 is a low cost frequency generator designed specifically for desktop and notebook PC applications. Its CPU clocks provide all necessary CPU frequencies for 286, 386 and 486 systems, including support for the latest speeds of processors. The device uses a 14.318 MHz crystal to generate the CPU and all peripheral clocks for integrated desktop motherboards.

The dual 14.318 MHz clock outputs allows one output for the system and one to be the input to an ICS Graphics Frequency Generator such as the AV9194.

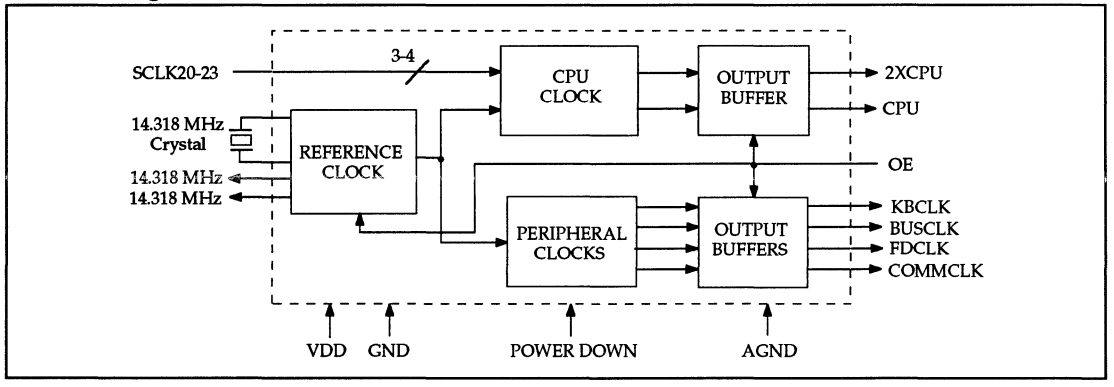
The CPU clock offers the unique feature of smooth, glitch-free transitions from one frequency to the next, making this the ideal device to use whenever slowing the CPU speed. The AV9155 makes a gradual transition between frequencies, so that it obeys the Intel cycle to cycle timing specification for 486 systems. The simultaneous 2X and 1X CPU clocks offer controlled skew to within 1.5ns (max) of each other.

ICS offers several versions of the AV9155. The different devices are shown below:

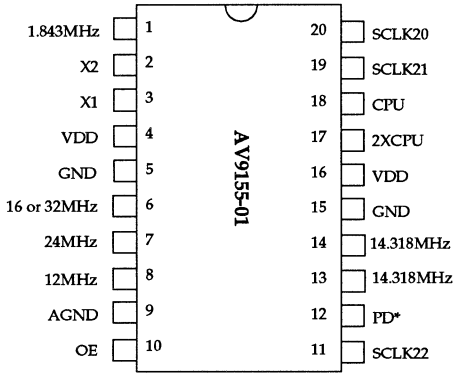
Part	Description
AV9155-01	Motherboard clock generator with 16 MHz BUS CLK
AV9155-02	Motherboard clock generator with 32 MHz BUS CLK
AV9155-03	Special frequencies for both 386 and 486 CPUs
AV9155-23	Includes Pentium™ frequencies
AV9155-36	Features a special 40MHz SCUZZY clock

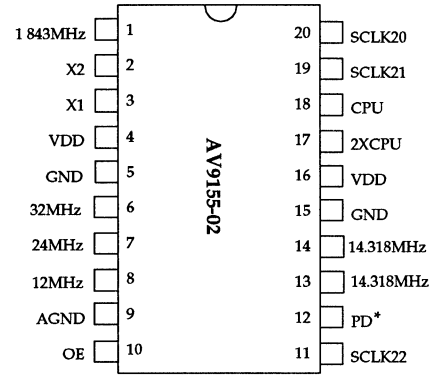
ICS has been shipping Motherboard Frequency Generators since April 1990, and is the leader in the area of multiple output clocks on a single chip. The AV9155 is a third generation device, and uses ICS's patented analog CMOS Phase Locked Loop technology for low phase jitter. ICS offers a broad family of frequency generators for motherboards, graphics and other applications, including cost effective versions with only one or two output clocks. Consult ICS for all of your clock generation needs.

Block Diagram for AV9155



Pin Configuration





Pin Description for AV9155-01, -02

Pin Name	Pin #	Pin type	Description
1.843MHz	1	Output	1.84 MHz clock output
X2	2	Output	CRYSTAL connection
X1	3	Input	CRYSTAL connection
VDD	4	-	DIGITAL POWER SUPPLY (+5V)
GND	5	-	Digital GROUND
16MHz/32MHz	6	Output	16 MHz (AV9155-01) or 32MHz (AV9155-02) clock output
24MHz	7	Output	24 MHz floppy disk/combination I/O clock output
12MHz	8	Output	12 MHz keyboard clock output
AGND	9	-	ANALOG GROUND (original version)
OE	10	Input	OUTPUT ENABLE. Tri-states all outputs when low
SCLK22	11	Input	CPU CLOCK frequency SELECT #2
AVDD	12	-	ANALOG POWER SUPPLY (+5V)
PD*	12	Input	POWER DOWN. Shuts off entire chip when low (U version)
14.318MHz	13	Output	14.318 MHz reference clock output
14.318MHz	14	Output	14.318 MHz reference clock output
GND	15	-	Digital GROUND
VDD	16	-	DIGITAL POWER SUPPLY (+5V)
2XCPU	17	Output	2X CPU clock output
CPU	18	Output	1X CPU clock output
SCLK21	19	Input	CPU CLOCK frequency SELECT #1
SCLK20	20	Input	CPU CLOCK frequency SELECT #0

Decoding and Clock Tables AV9155-01 (using 14.318 MHz input. All frequencies in MHz)

CLOCK#2 CPU and 2XCPU

SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin 17)	CPU (Pin 18)
0	0	0	8	4
0	0	1	16	8
0	1	0	32	16
0	1	1	40	20
1	0	0	50	25
1	0	1	66.66	33.33
1	1	0	80	40
1	1	1	100	50

PERIPHERAL CLOCKS

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.843	16	24	12

REFERENCE CLOCKS

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318

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Decoding and Clock Tables AV9155-02 (using 14.318 MHz input. All frequencies in MHz)

CLOCK#2 CPU and 2XCPU

SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin 17)	CPU (Pin 18)
0	0	0	8	4
0	0	1	16	8
0	1	0	32	16
0	1	1	40	20
1	0	0	50	25
1	0	1	66.66	33.33
1	1	0	80	40
1	1	1	100	50

PERIPHERAL CLOCKS

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.843	32	24	12

REFERENCE CLOCKS

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318

The "U" Version

ICS is producing enhanced versions of the AV9155-01 and AV9155-02 that are exactly compatible with the original versions. These "U" versions offer improved performance and the addition of a power down pin that turns off the entire chip.

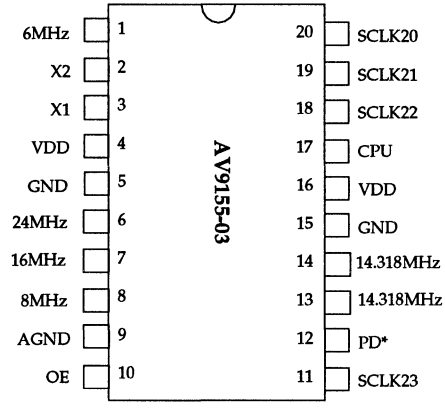
Frequency Transitions

A key feature of the AV9155 is its ability to provide smooth, glitch-free frequency transitions on the CPU and 2XCPU clocks when the frequency select pins are changed. These frequency transitions do not violate the Intel 486 specification of less than 0.1% frequency change per clock period.

Using an Input Clock as Reference

The AV9155 is designed to accept a 14.318 MHz crystal as the input reference. With some external changes, it is possible to use a crystal oscillator or clock input. Please see application note AAN04 for details on driving the AV9155 with a clock.

Pin Configurations



Pin Description for AV9155-03

Pin Name	Pin #	Pin type	Description
6MHz	1	Output	6 MHz clock output (-03) or 1.843 MHz (-23) clock output
X2	2	Output	CRYSTAL connection
X1	3	Input	CRYSTAL connection
VDD	4	-	DIGITAL POWER SUPPLY (+5V)
GND	5	-	Digital GROUND
24MHz	6	Output	24 MHz (-03) floppy disk or 16 MHz (-23) bus clock out
16MHz	7	Output	16 MHz (-03) bus clock output or 24 MHz (-23) floppy disk
8MHz	8	Output	8 MHz (-03) or 12 MHz (-23) keyboard clock output
AGND	9	-	ANALOG GROUND
OE	10	Input	OUTPUT ENABLE. Tri-states all outputs when low
SCLK23	11	Input	CPU CLOCK frequency
PD*	12	Input	POWER DOWN. Turns off entire chip when low
14.318MHz	13	Output	14.318 MHz reference clock output
14.318MHz	14	Output	14.318 MHz reference clock output
GND	15	-	Digital GROUND
VDD	16	-	DIGITAL POWER SUPPLY (+5V)
CPU	17	Output	CPU clock output / 2XCPU clock output
SCLK22	18	Input	CPU CLOCK frequency SELECT #2 (-03) / CPU clock output (-23)
SCLK21	19	Input	CPU CLOCK frequency SELECT #1
SCLK20	20	Input	CPU CLOCK frequency SELECT #0

Decoding and Clock Tables for AV9155-03
(using 14.318 MHz input. All frequencies in MHz)

CLOCK #2 CPU

SCLK23 (Pin 11)	SCLK22 (Pin 18)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	CPU (Pin 17)	
0	0	0	0	16	
0	0	0	1	40	
0	0	1	0	50	
0	0	1	1	80	
0	1	0	0	66.66	386
0	1	0	1	100	
0	1	1	0	8	
0	1	1	1	4	
1	0	0	0	8	
1	0	0	1	20	
1	0	1	0	25	
1	0	1	1	40	
1	1	0	0	33.3	486
1	1	0	1	50	
1	1	1	0	4	
1	1	1	1	2	

Smooth, glitch-free frequency transitions are guaranteed if the state of SCLK23 (pin 11) is not changed (smooth transitions are guaranteed in either the top or bottom half of the frequency decode table).

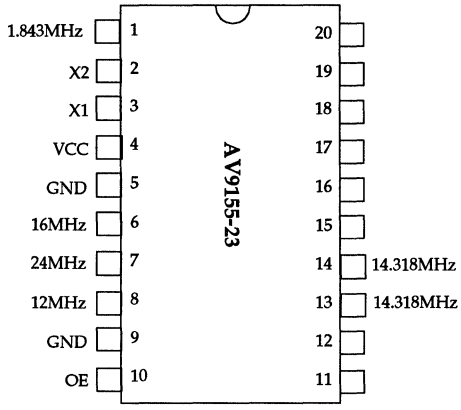
PERIPHERAL CLOCKS

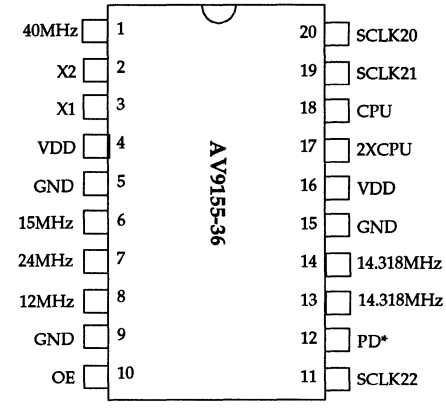
COMMCLK (Pin 1)	BUSCLK (Pin 7)	FDCLK (Pin 6)	KBCLK (Pin 8)
6 MHz	16 MHz	24 MHz	8 MHz

REFERENCE CLOCKS

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318

Pin Configuration





Pin Configuration for AV9155-23, -36

Pin Name	Pin #	Pin type	Description
1.843/40MHz	1	Output	1.843 MHz/40 MHz clock output
X2	2	Output	CRYSTAL connection
X1	3	Input	CRYSTAL connection
VDD	4	-	DIGITAL POWER SUPPLY (+5V)
GND	5	-	Digital GROUND
16MHz/15MHz	6	Output	16 MHz /15 MHz clock output
24MHz	7	Output	24 MHz floppy disk/combination I/O clock output
12MHz	8	Output	12 MHz keyboard clock output
AGND	9	-	ANALOG GROUND (original version)
OE	10	Input	OUTPUT ENABLE. Tri-states all outputs when low
SCLK22	11	Input	CPU CLOCK frequency SELECT #2
AVDD	12	-	ANALOG POWER SUPPLY (+5V)
PD*	12	Input	POWER DOWN. Shuts off entire chip when low (U version)
14.318MHz	13	Output	14.318 MHz reference clock output
14.318MHz	14	Output	14.318 MHz reference clock output
GND	15	-	Digital GROUND
VDD	16	-	DIGITAL POWER SUPPLY (+5V)
2XCPU	17	Output	2X CPU clock output
CPU	18	Output	1X CPU clock output
SCLK21	19	Input	CPU CLOCK frequency SELECT #1
SCLK20	20	Input	CPU CLOCK frequency SELECT #0

Decoding and ClockTables (using 14.318 MHz input. All frequencies in MHz)

AV9155-23

CLOCK#2 CPU and 2XCPU

SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin 17)	CPU (Pin 18)
0	0	0	75	37.5
0	0	1	32	16
0	1	0	60	30
0	1	1	40	20
1	0	0	50	25
1	0	1	66.66	33.33
1	1	0	80	40
1	1	1	52	26

PERIPHERAL CLOCKS

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.843	16	24	12

REFERENCE CLOCKS

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318

AV9155-36

CLOCK#2 CPU and 2XCPU

SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin 17)	CPU (Pin 18)
0	0	0	8	4
0	0	1	16	8
0	1	0	60	30
0	1	1	40	20
1	0	0	50	25
1	0	1	66.66	33.33
1	1	0	80	40
1	1	1	100	50

PERIPHERAL CLOCKS

SCUZZYCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
40	15	24	12

REFERENCE CLOCKS

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318

Absolute Maximum Ratings

AVDD, VDD referenced to GND..... 7V
Operating temperature under bias..... 0°C to +70°C
Storage temperature..... -40°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation..... 0.5 Watts

Note: Stresses above those listed under Absolute Maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect devices reliability.

Electrical Characteristics

(V_{DD} = +5V± 10%, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage			0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0			V	V_{DD} = 5V
I_{IL}	Input Low Current			-5	µA	V_{IN} = 0V
I_{IH}	Input High Current			5	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4mA
V_{OH}	Output High Voltage	V_{DD}-.4V			V	I_{OH} = -1mA,V_{DD}=5.0V
V_{OH}	Output High Voltage	V_{DD}-.8V			V	I_{OH} = -4mA,V_{DD}=5.0V
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -8mA
I_{CC}	Supply Current		40		mA	[1]No load
I_{CDSTBY}	Supply Current, Power Down		35	70	µA	No load
F_D	Output Frequency Change over Supply and Temperature		0.002	0.01	%	With respect to typical frequency
I_{SC}	Short circuit current	25	40		mA	Each output clock
R_{PU}	Pull-up resistor value		680		kΩ	Pin 10 (and 12,U only)
C_i	Input Capacitance			10	pF	Except X1, X2
C_L	Load Capacitance		20		pF	Pins X1, X2
AC Characteristics						
t_r	Output Rise time, 0.8 to 2.0V	-	1	2	ns	25 pf load
t_r	Rise time, 20% to 80% V_{DD}	-	2	4	ns	25 pf load
t_f	Output Fall time, 2.0 to 0.8V	-	1	2	ns	25 pf load
t_f	Fall time, 80% to 20% V_{DD}	-	2	4	ns	25 pf load
d_t	Duty cycle	40/60	48/52	60/40	%	25 pf load
d_t	Duty cycle, reference clocks	40/60	43/57	60/40	%	25 pf load
t_{jls}	Jitter, one sigma		0.8	2.5	%	As compared with
t_{jab}	Jitter, absolute		2	5	%	clock period
t_{jab}	Jitter, absolute			700	ps	16-100 MHz clocks
f_i	Input Frequency		14.318		MHz	
T_{sk}	Clock skew between CPU and 2XCPU outputs		1	1.5	ns	(1.0ns max on U parts)
t_{ft}	Frequency Transition time		15	20	ms	From 8 to 100MHz

Notes:
1. All clocks on AV9155-01 running at highest possible frequencies. Power supply current can change substantially with different mask configurations. Consult ICS.

Actual Output Frequencies
(using 14.318 MHz input. All frequencies in MHz)

AV9155-01 and AV9155-02

CPU CLOCK

SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin 17)	CPU (Pin 18)
0	0	0	7.50	3.75
0	0	1	15.51	7.76
0	1	0	32.22	16.11
0	1	1	40.09	20.05
1	0	0	50.11	25.06
1	0	1	66.82	33.41
1	1	0	80.18	40.09
1	1	1	100.23	50.11

PERIPHERAL CLOCKS

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.846	32.01 or 16.00	24. 00	12.00

AV9155-03

CLOCK #2 CPU

SCLK23 (Pin 11)	SCLK22 (Pin 18)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	CPU (Pin 17)
0	0	0	0	15.51
0	0	0	1	40.09
0	0	1	0	50.11
0	0	1	1	80.18
0	1	0	0	66.82
0	1	0	1	100.23
0	1	1	0	7.58
0	1	1	1	4.30
1	0	0	0	7.76
1	0	0	1	20.05
1	0	1	0	25.06
1	0	1	1	40.09
1	1	0	0	33.41
1	1	0	1	50.11
1	1	1	0	3.79
1	1	1	1	2.15

PERIPHERAL CLOCKS

COMMCLK (Pin 1)	BUSCLK (Pin 7)	FDCLK (Pin 6)	KBCLK (Pin 8)
6.00	16.00	24.00	8.00

AV9155-23

CPU CLOCK

SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin 17)	CPU (Pin 18)
0	0	0	75.170	37.585
0	0	1	31.940	15.970
0	1	0	60.136	30.068
0	1	1	40.090	20.045
1	0	0	50.113	25.057
1	0	1	66.476	33.238
1	1	0	80.181	40.091
1	1	1	51.903	25.952

PERIPHERAL CLOCKS

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.843	16.00	24. 00	12.00

AV9155-36

CPU CLOCK

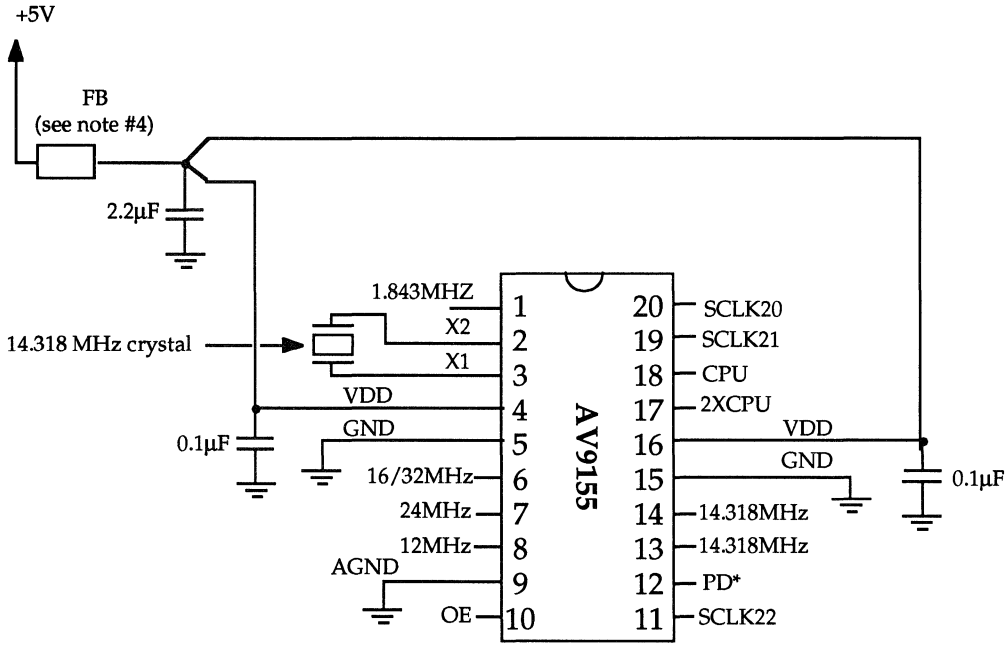
SCLK22 (Pin 11)	SCLK21 (Pin 19)	SCLK20 (Pin 20)	2XCPU (Pin 17)	CPU (Pin 18)
0	0	0	8.054	4.027
0	0	1	16.002	8.001
0	1	0	59.875	29.936
0	1	1	39.886	19.943
1	0	0	50.113	25.057
1	0	1	66.476	33.238
1	1	0	80.181	40.091
1	1	1	100.226	50.113

PERIPHERAL CLOCKS

SCUZZYCLK (Pin 1)	BUSCLK (Pin 7)	FDCLK (Pin 6)	KBCLK (Pin 8)
40.00	15.00	24.00	12.00

D

AV9155
Recommended External Circuit



Notes:

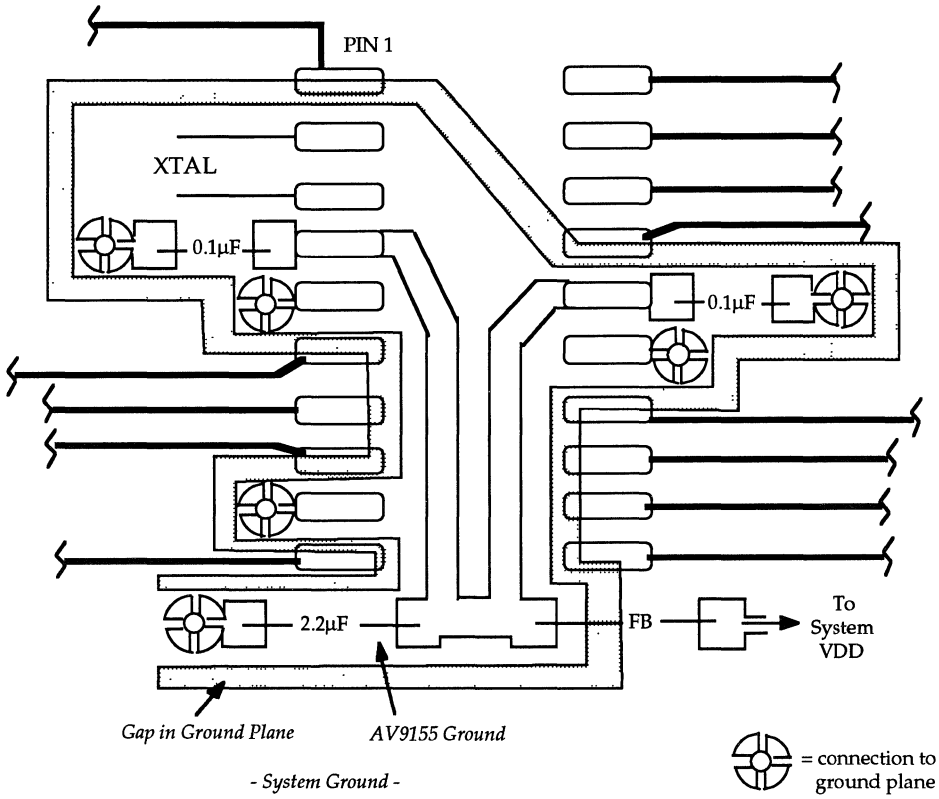
1. ICS recommends the use of an isolated ground plane for the AV9155.
All grounds shown on this drawing should be connected to this ground plane.
This ground plane should be connected to the system ground plane at a single point.
Please refer to AV9155 Board Layout diagram.

2. A single power supply connection for all VDD lines at the 2.2 µF decoupling capacitor is recommended to reduce interaction of analog and digital circuits. The 0.1 µF decoupling capacitors should be located as close to each VDD pin as possible.

3. A 33 Ω series termination resistor should be used on any clock output which drives more than one load or drives a long trace (more than about 2 inches), especially when using high frequencies (>50 MHz). This termination resistor is put in series with the clock output line close to the clock output. It helps improve jitter perfomance and reduce EMI by damping standing waves caused by impedance mismatches in the output clock circuit trace.

4. The ferrite bead does not enhance the performance of the AV9155, but will reduce EMI radiation from the VDD line.

AV9155 Recommended Board Layout



This is the recommended layout for the AV9155 to maximize clock performance. Shown are the power and ground connections, the ground plane, and the input/output traces.

Use of the isolated ground plane and power connection, as shown, will prevent stray high frequency ground and system noise from propagating through the device. When compared to using the system ground and power planes, this technique will minimize output clock jitter. The isolated ground plane should be connected to the system ground plane at one point, near the 2.2µF decoupling cap. For lowest jitter performance, this isolated ground plane should be kept away from clock output pins and traces. Keeping the isolated ground plane area as small as possible will minimize EMI radiation. Use a sufficient gap between the isolated ground plane and system ground plane to prevent AC coupling. The ferrite bead in the VDD line optional, but will help reduce EMI.

The traces to distribute the output clocks should be over a system ground or power supply plane. The trace width should be about two times the thickness of the PC board between the trace and the underlying plane. These guidelines help minimize clock jitter and EMI radiation. The traces to distribute power should be as wide as possible.

Ordering Information

Part Number	Temperature Range	Package Type
AV9155-xxCN20	0°C to +70°C	20 lead Plastic DIP
AV9155-xxCW20	0°C to +70°C	20 lead Plastic SOIC

Notes:
The dash number following AV9155, (denoted by xx above) must be included when ordering product, since it specifies the version being ordered. Tape and reel packaging should be ordered with the suffix T&R. For instance, if the -01 in SOIC and tape and reel is required, order the part as AV9155-01CW20T&R. All versions currently shipping are U versions, as of September 1992.

Part Marking

Original version (-01 and -02):

ICS
AV9155-xxCx20
Date code/Lot code

U version (-01 and -02):

ICS
AV9155-xxCx20
U Date code/Lot code

Integrated Circuit Systems, Inc.

ICS9158

Advance Information

Integrated Buffer and Motherboard Frequency Generator

Features

- Eight skew free, high drive CPU clock outputs
- Up to 100 MHz output at 5V, 66 MHz at 3.3V
- ± 250psec skew between CPU outputs
- Outputs can drive up to 30pF load
- 25mA output drivers
- Typical 50/50 duty cycle
- Compatible with 486 and Pentium CPUs
- Glitch-free start and stop clock feature
- Optional power-down mode supports Energy Star ("green") PCs
- On chip loop filter components
- Low power, high speed 0.8 µ CMOS technology
- 24 pin PDIP or SOIC package

General Description

The ICS9158 is a low cost frequency generator designed specifically for desktop and notebook PC applications. Eight high drive, skew controlled copies of the CPU clock are available, eliminating the need for an external buffer.

Each high drive (25 mA) output is capable of driving a 30pF load and has a typical duty cycle of 50/50. The CPU clock ouputs are skew controlled to within ±250psec.

The CPU clocks provide all necessary frequencies for 286, 386, 486, and Pentium systems, including support for the latest speeds of processors.

The CPU clock offers the unique feature of smooth, glitch-free transitions from one frequency to the next, making this the ideal device to use whenever slowing the CPU speed. The ICS9158 makes a gradual transition between frequencies, so that it meets the Intel cycle to cycle timing specification for 486 systems.

ICS has been shipping Motherboard Frequency Generators since April 1990, and is the leader in the area of multiple output clocks on a single chip. The ICS9158 is a third generation device, and uses ICS' patented analog CMOS Phase Locked Loop technology for low phase jitter. ICS offers a broad family of frequency generators for motherboards, graphics and other applications, including cost effective versions with only one or two output clocks. Consult ICS for all of your clock generation needs.

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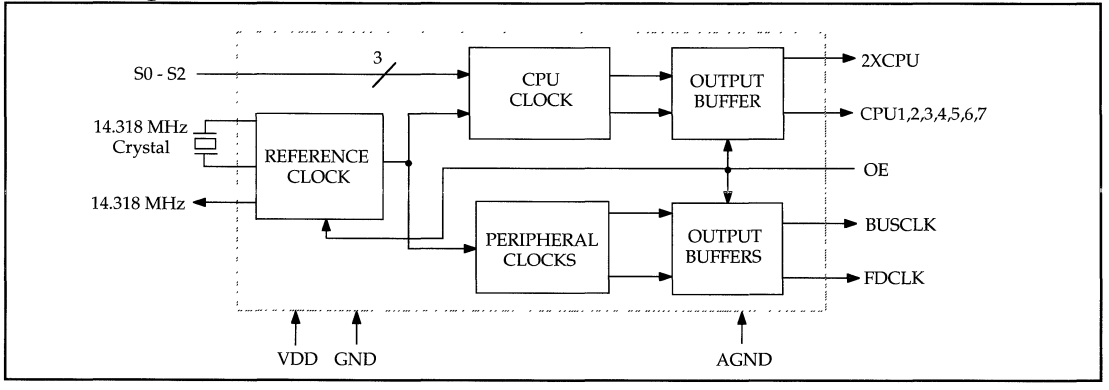
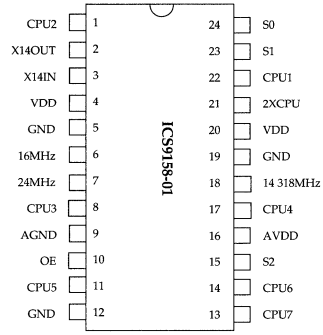
Clock Table (in MHz)

Clock	AV9158-01
BUSCLK	16
FDCLK	24
14.318	14.318
CPUCLK	4,8,30,20,25,33.3,40, or 50
2XCPUCLK	8,16,60,40,50,66.6,80, or 100

Block Diagram



Pin Configuration



ICS9158-01 Pin Description

Pin Name	Pin #	Pin Type	Description
CPU2	1	Output	CPU clock output
X14OUT	2	-	Crystal connection
X14IN	3	-	Crystal connection
VDD	4	-	Digital POWER SUPPLY (+5V)
GND	5	-	Digital GROUND
16MHz	6	Output	16 MHz clock output
24MHz	7	Output	24 MHz floppy disk/combination I/O clock output
CPU3	8	Output	CPU clock output
AGND	9	-	ANALOG GROUND
OE	10	Input	OUTPUT ENABLE. Tri-states all outputs when low
CPU5	11	Output	CPU clock output
GND	12	-	Digital GROUND
CPU7	13	Output	CPU clock output
CPU6	14	Output	CPU clock output
S2	15	Input	CPU clock frequency select 2
AVDD	16	-	ANALOG power supply (+5V)
CPU4	17	Output	CPU clock output
14.318MHz	18	Output	14.318 MHz clock output
GND	19	-	Digital GROUND
VDD	20	-	Digital POWER SUPPLY (+5V)
2XCPU	21	Output	2X CPU clock output
CPU1	22	Output	CPU clock output
S1	23	Input	CPU clock frequency select #1
S0	24	Input	CPU clock frequency select #0

Absolute Maximum Ratings

AVDD, VDD referenced to GND..... 7V
Operating temperature under bias..... 0°C to +70°C
Storage temperature..... -40°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation..... 0.5 Watts

Note: Stresses above those listed under Absolute Maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect devices reliability.

Electrical Characteristics

(V_{DD} = +5V± 10%, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage			0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0			V	V_{DD} = 5V
I_{IL}	Input Low Current			- 40	µA	V_{IN} = 0V
I_{IH}	Input High Current			+40	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4mA
V_{OH}	Output High Voltage	V_{DD}-.4V			V	I_{OH} = -1mA,V_{DD}=5.0V
V_{OH}	Output High Voltage	V_{DD}-.8V			V	I_{OH} = -4mA,V_{DD}=5.0V
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -8mA
I_{CC}	Supply Current		70		mA	[1]No load
F_D	Output Frequency Change over Supply and Temperature		0.002	0.01	%	With respect to typical frequency
I_{SC}	Short circuit current	25	56		mA	Each output clock
R_{PU}	Pull-up resistor value		680		kΩ	Input pin
C_I	Input Capacitance			8	pF	Except X1, X2
C_L	Load Capacitance		30		pF	Pins X1, X2
AC Characteristics						
t_r	Output Rise time, 0.8 to 2.0V	-	1	2	ns	30 pf load
t_r	Rise time, 20% to 80% V_{DD}	-	2.5	3	ns	30 pf load
t_f	Output Fall time, 2.0 to 0.8V	-	0.5	1	ns	30 pf load
t_f	Fall time, 80% to 20% V_{DD}	-	1.5	2	ns	30 pf load
d_t	Duty cycle	40/60	48/52	60/40	%	30 pf load
d_t	Duty cycle, reference clocks	40/60	43/57	60/40	%	30 pf load
t_{jls}	Jitter, one sigma		0.5	2.0	%	As compared with
t_{jab}	Jitter, absolute		2	5	%	clock period
t_{jab}	Jitter, absolute			500	ps	16-100 MHz clocks
f_I	Input Frequency		14.318		MHz	
T_{sk}	Clock skew between CPU and 2XCPU outputs		100	250	ps	
t_{ft}	Frequency Transition time		13	20	ms	From 3.79 to 50.1 MHz

Notes:
1. All clocks on ICS9158 running at highest possible frequencies. Power supply current can change substantially with different mask configurations. Consult ICS.

ICS9158-01 CPU Clock Decoding Table (using 14.318 MHz input. All frequencies in MHz)

CLOCK#2 CPU and 2XCPU

S2 (Pin 15)	S1 (Pin 23)	S0 (Pin 24)	2XCPU (Pin 21)	CPU
0	0	0	7.580	3.790
0	0	1	15.511	7.756
0	1	0	59.875	29.938
0	1	1	40.090	20.045
1	0	0	50.113	25.057
1	0	1	66.476	33.238
1	1	0	79.772	39.886
1	1	1	100.226	50.113

PERIPHERAL CLOCKS

BUSCLK (Pin 6)	FDCLK (Pin 7)
16.002	24.003

REFERENCE CLOCK

REFCLK1 (Pin 18)
14.318

Frequency Transitions

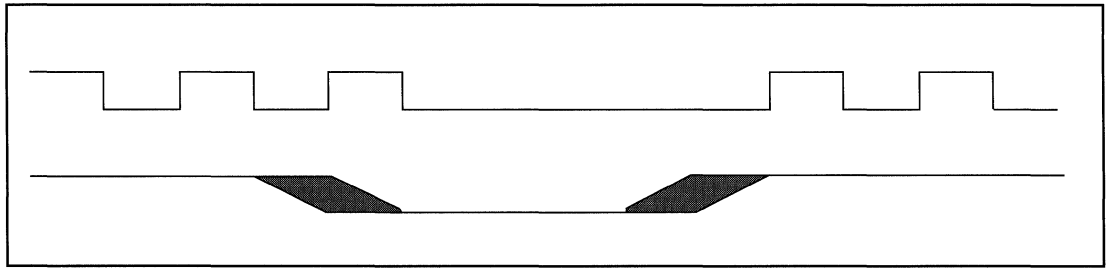
A key feature of the ICS9158 is its ability to provide smooth, glitch-free frequency transitions on the CPU and 2XCPU clocks when the frequency select pins are changed. The frequency transition rate does not violate the Intel 486 specification of less than 0.1% frequency change per clock period.

Using an Input Clock as a Reference

The ICS9158 is designed to accept a 14.318 MHz crystal as the input reference. With some external changes, it is possible to use a crystal oscillator or other clock sources. Please see application note AAN04 for details on driving the ICS9158 with a clock.

Stop Clock Feature

The ICS9158 incorporates a unique stop clock feature compatible with static logic processors. When the stop clock pin goes low, the CPUCLK will go low after the next occuring falling edge. When STOPCLK again goes high, CPUCLK resumes on the next rising edge of the internal clock. This feature enables fast, glitch-free starts and stops of the CPUCLK and is useful in Energy Star motherboard applications.



Ordering Information

Part Number	Temperature Range	Package Type
ICS9158-xxCN24	0°C to +70°C	24 lead Plastic DIP
ICS9158-xxCW24	0°C to +70°C	24 lead Plastic SOIC

ICS

Special Purpose IC

Products

D

Special Purpose IC Products Guide

Product Applications	ICS Device Type	Features	Package Types	Page
Motherboard	ICS1694A	Single Crystal Generates Three Low-Jitter Clocks.	8 Pin DIP, SOIC	481
	AV9110	User-Programmable "On-the-Fly"; Low-Jitter makes it Ideal for Disk Drive or Video Applications.	14 Pin DIP, SOIC	485
	ICS9123	High Resolution Clock Generator; One Channel has Accuracy to within 50 PPM and making it Ideal for Modem, Ethernet and AD1848 Applications.	16 or 20 Pin DIP, SOIC	495
	AV9170	Clock Synchronizer and Multiplier.	8 Pin DIP, SOIC	497
	AV9172	Low Skew Output Buffer. Low Skew and Jitter make it Ideal for Pentium™ Applications.	16 Pin DIP, SOIC	511
	AV9173	Low Cost Video Genlock PLL.	8 Pin DIP, SOIC	519
	ICS9175	Low Skew Output Buffer Crystal Generates Six Low Skew, Low-Jitter Clocks.	16 Pin DIP, SOIC	523
	ICS9176	Input Clock Generates IO Low Skew, Low-Jitter Outputs. Ideal for Pentium or PLI Applications.	28 Pin PLCC	535

ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. ICS reserves the right to change or discontinue these products without notice.

Integrated Circuit Systems, Inc.

ICS1694A

Product Preview

Mini-Motherboard Clock Generator

Features

- Low Cost Motherboard Clock Generator
- Small Footprint, space-saving package
- Very Flexible Architecture
- Advanced PLL design
- Upgraded the ICS1694 to include Output Enable and higher frequency capabilities
- Many standard patterns available

Applications

- Any design requiring clocking signals or count down chains derived from a clock signal
- Memory refresh
- Keyboard
- Serial port
- Floppy Disk
- Hard Disk
- CPU
- Coprocessor

D

Description

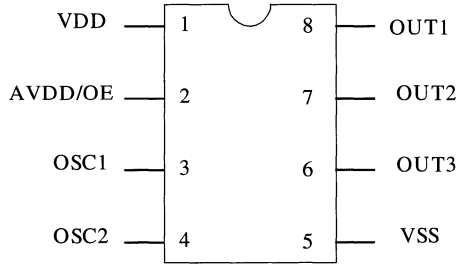
The **ICS1694A** Mini-Motherboard Clock Generator has been developed to give designers a unique, efficient (cost, size, and power) means of generating the various clocks required in a digital system. The initial patterns being offered as standards are summarized in Table 1.

The low cost and small size of the **ICS1694A** allow the designer to use multiple devices (different patterns) in a system in order to generate the clock signals physically close to the requirement, instead of having long PCB board traces transmitting (and radiating) the signals.

The **ICS1694A** contains all the passive components required for a crystal oscillator or it may be driven by a clock signal. In some applications, one of the outputs of one **ICS1694A** will be used as the clock input of a second or third **ICS1694A**, thus requiring only one quartz crystal for the system and, in the process, synchronizing all the clock signals to the crystal oscillator.

The **ICS1694A** contains a single PLL. Therefore all output frequencies, other than the buffered crystal oscillator, must be the result of an integer division of the PLL frequency. For instance, if the PLL operates at 120 MHz, the outputs could be a selection of three of any of the following: 120 MHz, 60 MHz, 40 MHz, 30 MHz, 24 MHz, 20 MHz, 15 MHz, 12 MHz, 10 MHz, 8 MHz, 6 MHz, etc. More detail concerning the options is given in the section titled PATTERNS.

Pin Configuration



Ordering Information
ICS1694AN-XXX (DIP Package)
ICS1694AM-XXX (SO Package)
(XXX= Pattern Number)

Options

Pin 2 may be bonded to serve as either AVDD (analog positive supply) or OE (output enable). The outputs (OUT1, OUT2, and OUT3) will be enabled when OE is held high. OE has internal pull-up so it may be allowed to float.

If particularly stable outputs are required, the option with pin 2 bonded as AVDD is recommended. AVDD should be driven by the system's analog supply, if available. In some applications where only a digital supply is available, AVDD can be driven from the digital VDD supply through a simple RC decoupling circuit. The voltage drop across the series resistor should be held to less than 250 mv. It is difficult to generalize across all applications, but in the majority of cases the performance of the **ICS1694A** is completely satisfactory when used with power supplied only to pin 1 and pin 2 bonded as Output Enable.

Patterns

A number of standard patterns will be offered which will satisfy most of the typical requirements of the PC market. New patterns are continuously being added as new applications surface. ICS welcomes suggestions for new patterns and will also fabricate custom patterns as described in the following paragraph.

The **ICS1694A** contains one PLL-VCO which is mask programmable to any frequency up to 180 MHz. The chip contains a number of counter stages which can be used to count the VCO frequency down to the desired output frequencies. The output frequencies are derived by dividing the VCO frequency by an integer.This is a limitation on the frequencies which can be generated in the same chip since each frequency must be derived from the same VCO frequency.

For instance, pattern 010 programs the VCO to 120 MHz. Then a divide by 3 yields 40 MHz; a divide by 4 yields 30 MHz; and a divide by 5 yields 24 MHz. Obviously, some of the divide chains can and are combined. An output may also be the crystal oscillator frequency or that frequency divided by an integer.

It should also be considered that the input does not have to be 14.318 MHz, but can be any fundamental mode crystal up to 25 MHz. Table 1 lists the frequencies available from the various patterns. For any of these patterns, the crystal frequency (and thus the PLL-VCO frequency) may be changed and the output frequencies will be scaled accordingly. For instance, if the crystal frequency used is one half of that listed in Table 1, the actual output frequencies will be one half those listed in the table. Also options are available which will work with an overtone crystal.

Absolute Maximum Ratings

Supply Voltage	V_{DD}	-0.5V to + 7V
Input Voltage	V_{IN}	-0.5V to V_{DD}+ 0.5V
Output Voltage	V_{OUT}	-0.5V to V_{DD}+ 0.5V
Clamp Diode Current	V_{IK} & I_{OK}	+ /-30mA
Output Current per Pin	I_{OUT}	+ /-50mA
Operating Temperature	T_o	0 °C to 70 °C
Storage Temperature	T_S	-85 °C to + 150 °C
Power Dissipation	P_D	300mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to > = V_{SS} and < = V_{DD}.

DC Characteristics (0°C to 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
		5.0V± 5% OPERATION			
V_{DD}	Operating Voltage Range	4.75	5.25	V	
V_{IL}	Input Low Voltage	V_{ss}	0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0	V_{DD}	V	V_{DD} = 5V
I_{LH}	Input Leakage Current	--	10	µA	V_{IN} = V_{cc}
V_{OL}	Output Low Voltage	--	0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4	--	V	I_{OH} = 4.0 mA
I_{DD}	Digital Supply Current	--	30	mA	V_{DD} = 5V, VCO = 120 MHz
I_{AA}	Analog Supply Current		8	mA	V_{DD} = 5V, VCO = 120 MHz
C_{in}	Input Pin Capacitance	--	8	pF	F_c = 1 MHz
C_{out}	Output Pin Capacitance	--	12	pF	F_c = 1 MHz
		3.3V± 10% OPERATION			
I_{DD}	Digital Supply Current	-	20	mA	V_{DD} = 3.3V, VCO = 120 MHz
I_{AA}	Analog Supply Current	-	6	mA	V_{DD} = 3.3V, VCO = 120 MHz

If the OE option is used, IDD will be the sum of both the digital and analog supply currents.

D

AC Timing Characteristics

The following notes apply to all of the parameters presented in this section:

1. Xtal Frequency = 14.318 MHz, unless otherwise noted.
2. All units are in nanoseconds (ns).
3. Rise and fall time is between 0.8 and 2.0 VDC at 5.0V.
4. Output pin loading = 15pF
5. Duty cycle is measured at 1.4V at 5.0V.
6. Temperature Range = 0 °C to 70 °C

5.0V± 5% OPERATION

SYMBOL	PARAMETER	MIN	MAX	NOTES
	MCLK AND VCLK TIMING			
Tr	Rise Time	--	2	
Tf	Fall Time	--	2	
Dc	Duty Cycle	45	55	%
Fm	Maximum Frequency		180	MHz

3.0V± 10% OPERATION

SYMBOL	PARAMETER	MIN	MAX	NOTES
	MCLK AND VCLK TIMING			
Tr	Rise Time	--	3	
Tf	Fall Time	--	3	
Dc	Duty Cycle	45	55	%
Fm	Maximum Frequency		120	MHz

Standard Frequency Patterns (MHz)

Table 1

PINS	FUNCTION	PATTERNS							
		010	011	012	013	014	015	016	017
8	OUT1	24	25	12	6	24	24	XTAL	XTAL
7	OUT2	40	40	40	60	40	XTAL	16	12
6	OUT3	30	30	30	20	20	40	24	24
5	VSS								
4	XTAL2	25	25	25	25	14.318	14.318	14.318	14.318
3	XTAL1								
2	AVDD/OE								
1	VDD								

PINS	FUNCTION	PATTERNS							
8	OUT1								
7	OUT2								
6	OUT3								
5	VSS								
4	XTAL2								
3	XTAL1								
2	AVDD/OE								
1	VDD								

Serially Programmable Frequency Generator

Features

- Complete user programmability of output frequency through serial input data port
- On chip Phase Locked Loop for clock generation
- Generates accurate frequencies up to 130 MHz
- Tri-state CMOS outputs
- 5 volt power supply
- Low power CMOS technology
- 14 pin DIP or 150 mil SOIC
- Very low jitter
- Wide operating range VCO.

Applications

Graphics: The AV9110 generates low jitter, high speed pixel (or dot) clocks. It can be used to replace multiple expensive high speed crystal oscillators. The flexibility of this device allows it to generate non-standard graphics clocks, allowing the user to program frequencies on-the-fly.

Disk Drives: The AV9110 generates zone clocks for constant density recording schemes. The low profile, narrow 14 pin SOIC package, and low jitter outputs are especially attractive in board-space critical disk drives.

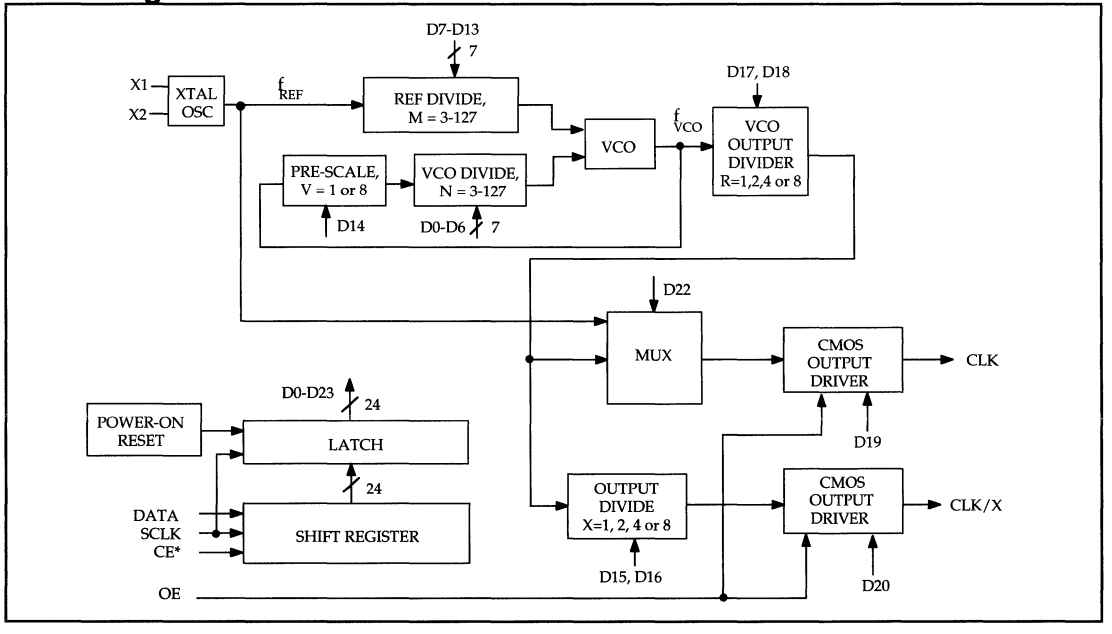
General Description

The AV9110 generates user specified clock frequencies using an externally generated input reference, such as a 14.318 MHz or 10.00 MHz crystal connected between pins 1 and 2. Alternately, a TTL input reference clock signal can be used. The output frequency is determined by a 24 bit digital word entered through the serial port. The serial port enables the user to change the output frequency on-the-fly.

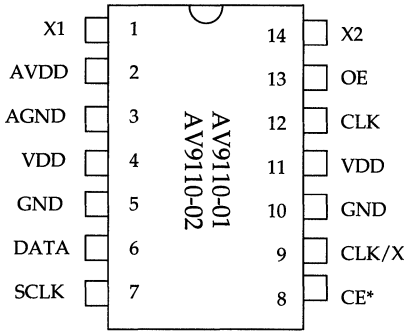
The clock outputs utilize CMOS level output buffers that operate up to 130 MHz.

D

Block Diagram



Pin Configuration



14 pin DIP, SOIC

Clock Reference Implementations: AV9110-01 vs. AV9110-02

The AV9110 requires a stable reference clock (5 to 32 MHz) to generate a stable, low-jitter output clock. The AV9110-01 is optimized to use an external quartz crystal as a frequency reference, without the need of additional external components. The AV9110-02 is optimized to accept an TTL clock reference. Either device can be used with an external crystal or accept a TTL clock reference, although extra components may be required. The various combinations implied are summarized in Figure 2 (see page 7) .

Pin Description

Pin Name	Pin #	Pin type	Description
X1	1	Input	Crystal input or TTL reference clock
AVDD	2	Power	ANALOG power supply. Connect to +5 V
AGND	3	Power	ANALOG GROUND
VDD	4	Power	Digital power supply. Connect to +5 V
GND	5	Power	Digital GROUND
DATA	6	Input	Serial DATA pin
SCLK	7	Input	SERIAL CLOCK. Clocks shift register
CE*	8	Input	CHIP ENABLE. Active low, controls data transfer
CLK/X	9	Input	CMOS CLOCK divided by X output
GND	10	Power	Digital GROUND
VDD	11	Power	Digital power supply. Connect to +5 V
CLK	12	Output	CMOS CLOCK output
OE	13	Input	OUTPUT ENABLE. Tri-states both outputs when low
X2	14	Input	Crystal input or TTL reference clock

Absolute Maximum Ratings

AVDD, VDD referenced to GND..... 7V
Operating temperature under bias..... 0°C to +70°C
Storage temperature..... -65°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation..... 0.8 Watts

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect the reliability of the device.

Electrical Characteristics

(V_{DD} = +5V± 10%, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage	-	-	0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0	-	-	V	V_{DD} = 5V
I_{IL}	Input Low Current	-	-	-5	µA	V_{IN} = 0V
I_{IH}	Input High Current	-	-	5	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage	-	-	0.4	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	2.4	-	-	V	I_{OH} = 8mA
$ICLK_r$	Input Clock Rise Time	-	-	20	nS	
$ICLK_f$	Input Clock Fall Time	-	-	20	nS	
I_{DD}	Supply Current	-	25		mA	No load
AC Characteristics						
f_o	Output frequency range	0.78	-	130	MHz	
t_r	Rise time, 20-80%	-	-	3	ns	25 pf load
t_f	Fall time, 80-20%	-	-	3	ns	25 pf load
d_t	Duty cycle	40		60	%	25 pf load
	Jitter, 1 sigma		±40	-	ps	
	Jitter, absolute		±125	-	ps	
f_{REF}	Input reference freq.; AV9110-01	5	14.318	32	MHz	Crystal input
f_{REF}	Input reference freq.; AV9110-02	0.6	14.318	32	MHz	TTL input
f_{DATA}	Input DATA or SCLK frequency			32	MHz	

D

Serial Programming

The AV9110 is programmed to generate clock frequencies by entering data through the shift register. Figure 1 displays the proper timing sequence. On the negative going edge of CE*, the shift register is enabled and the data at the DATA pin is loaded into the shift register on the rising edge of the SCLK. Bit D0 is loaded first, followed by D1, D2, etc. This data consists of the 24 bits shown in the Shift Register Bit Assignment in Table 1, and therefore takes 24 clock cycles to load. An internal counter then disables the input and transfers the data to internal latches on the rising edge of the 24th cycle of the SCLK. Any data entered after the 24th cycle is ignored until CE* is taken high and then low to start a new word. CE* must remain low for a minimum of 24 SCLK clock cycles. If CE* is taken high before 24 clock cycles have elapsed, the data is ignore (no frequency change occurs) and the counter is reset. Tables 1 and 2 display the bit location for generating the output clock frequency and the output divider circuitry, respectively.

Shift Register Bit Assignment

Bit	Assignment	Equation Variable	Default -01	Default -02	Bit
0	VCO frequency divider (LSB)	N Integer	1	1	0
1	"		1	1	1
2	"		1	1	2
3	"		1	1	3
4	"		1	1	4
5	"		1	1	5
6	VCO frequency divider (MSB)		1	1	6
7	Reference frequency divider (LSB)	M Integer	0	0	7
8	"		1	1	8
9	"		0	0	9
10	"		0	0	10
11	"		1	1	11
12	"		0	0	12
13	Reference frequency divider (MSB)		0	0	13
14	VCO pre-scale divide (0=divide by 1, 1=divide by 8)	V	0	0	14
15	CLK/X output divide COD0 (see table 2)	X	0	1	15
16	CLK/X output divide COD1 (see table 2)		1	0	16
17	VCO output divide VOD0 (see table 2)	R	0	0	17
18	VCO output divide VOD1 (see table 2)		1	1	18
19	Output enable CLK (0=tri-state)		1	1	19
20	Output enable CLK/X (0=tri-state)		1	1	20
21	Reserved. Should be programmed low (0)		1	1	21
22	Reference clock select on CLK (1 = reference frequency)		0	0	22
23	Reserved. Should be programmed high (1)		1	1	23

Table 1

Output Divider Truth Tables

COD1	COD0	CLK/X Output divide (X)
0	0	1
0	1	2
1	0	4
1	1	8

Table 2

VOD1	VOD0	VCO Output divide (R)
0	0	1
0	1	2
1	0	4
1	1	8

Table 3

Programming the PLL

The AV9110 has a wide operating range but it is recommended that it is operated within the following limits:

$2\ MHz < f_{REF} < 32\ MHz$	f_{REF}= Input reference frequency
$200\ KHz < \frac{f_{REF}}{M} < 5\ MHz$	M = Reference divide, 3 to 127
$50\ MHz < f_{VCO} < 250\ MHz$	f_{VCO} = VCO output frequency
$f_{CLK} \leq 130\ MHz$	f_{CLK} = CLK or CLK/X output frequency

The AV9110 is a classical PLL circuit and the VCO output frequency is given by:

$$f_{VCO} = \frac{N \bullet V \bullet f_{REF}}{M}$$

where N = VCO divide, 3 to 127
M = Reference divide, 3 to 127
V = Pre-scale, 1 or 8

The 2 output drivers then give the following frequencies:

$$f_{CLK} = \frac{f_{VCO}}{R} = \frac{N \bullet V \bullet f_{REF}}{M \bullet R} \text{ or } f_{REF} \text{ (output muxable by bit 17)}$$

$$f_{CLK/X} = \frac{f_{VCO}}{R \bullet X} = \frac{f_{VCLK}}{X}$$ Where R, X = output dividers, 1, 2, 4 or 8

Notes:
1. Output frequency accuracy will depend solely on input reference frequency accuracy.
2. For output frequencies below 125 MHz, it is recommended that the VCO output divide, R, should be 2 or greater. This will give improved duty cycle.
3. The minimum output frequency step size is approximately 0.2% due to the divider range provided.

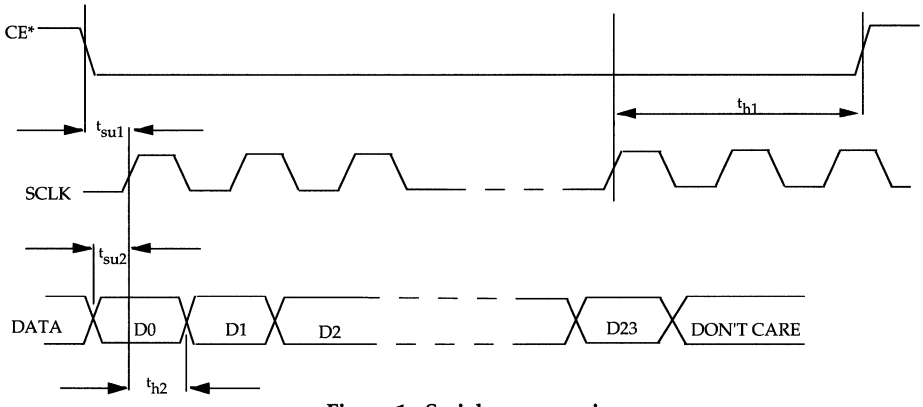


Figure 1 - Serial programming

AC Timing

Parameter	Minimum time (ns)
t_{su1}	10
t_{su2}	10
t_{h1}	10
t_{h2}	10

Frequency Acquisition Time

Frequency acquisition (or "lock") time is the time that it takes to change from one frequency to another, and is a function of the difference between the old and new frequencies. The AV9110 can typically lock to within 1% of a new frequency in less than 200µs. This is also true with power-on.

Power-On Reset

Upon power-up the internal latches are pre-set to provide the following output clock frequencies (14.318 MHz reference assumed):

Device	CLK output	CLK/X output
AV9110-01	25.175 MHz	6.29 MHz
AV9110-02	25.175 MHz	12.59 MHz

These preset default frequencies can be changed with a custom metal mask, as can other attributes.

Jitter

For high performance applications, the AV9110 offers extremely low jitter and excellent power supply rejection. The one sigma jitter distribution is typically less than 40 ps and the maximum jitter is typically less than ±125 ps. For optimum performance, the device should be decoupled with both a 2.2µF and a 0.1µF capacitor. Refer to Recommended Board Layout diagram on page 8.

Output Enable

The AV9110 outputs can be disabled with either the OE pin or through serial port programming. Setting the OE pin low tristates CLK and CLK/X. Alternatively, setting bits D19 and D20 low in the serial word will tri-state the two outputs. Both the OE pin and D19 or D20 must be high to enable an output.

Frequency Transition Glitches

The AV9110 starts changing frequency on the rising edge of the 24th serial clock. If the programming of any output divider is changed, the output clock may glitch before locking to the new output frequency. However, if the output dividers are unchanged, the VCO will change to the new frequency in less than 200 µsec with no output glitches (no partial clock cycles).

AV9110 Quartz Crystal Selection

When an external quartz crystal will be used as a frequency reference for the AV9110, attention needs to be given to crystal selection if accurate reference frequency and output frequency is desired. The AV9110 uses a Pierce oscillator design which operates the quartz crystal in parallel-resonant mode. It requires a quartz crystal cut for parallel-resonant operation to ensure an accurate frequency of oscillation (a less expensive series-resonant crystal can be used with the device but it will oscillate approximately 0.1% too fast). The AV9110-01 has internal crystal load capacitors which result in a total crystal load capacitance of approximately 12 pf ± 10%. The AV9110-02 does not have internal load capacitors, but contributes about 3 pf load capacitance to the crystal.

Following is a list of recommended crystal devices for the AV9110. They have been tested by the crystal manufacturer to operate suitably with the AV91xx-series crystal oscillator design, having load capacitance characteristics that are compatible with the AV9110-01.

Toyocom

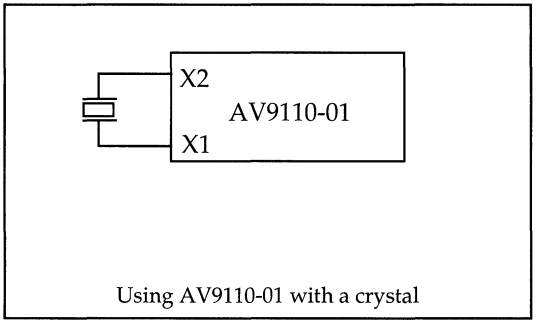
Part Number	
TN4-30374	14.318 MHz surface mount crystal
TN4-80375	20 MHz surface mount crystal
TN4-30376	14.318 MHz through-hole crystal
TN4-30377	20 MHz through-hole crystal

Epson

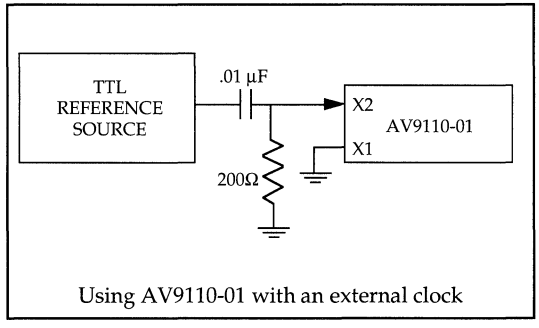
Part Number	
MA-505 or MA-506	Surface mount crystal
CA-301	Through-hole crystal

D

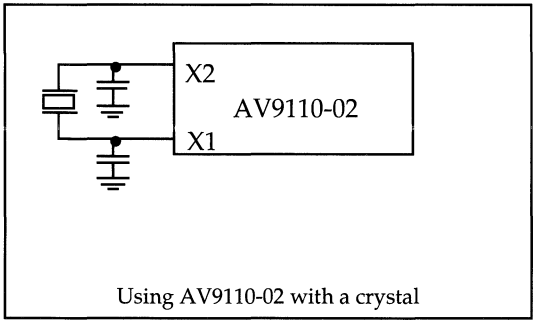
Figure 2
Clock Reference Combinations



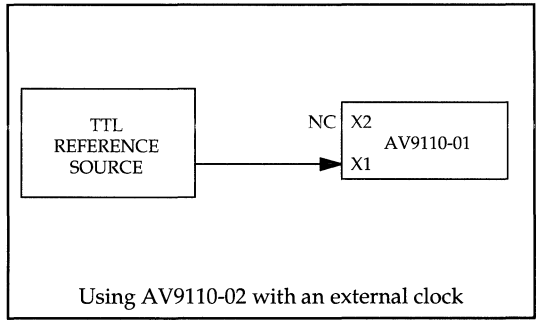
Using AV9110-01 with a crystal



Using AV9110-01 with an external clock

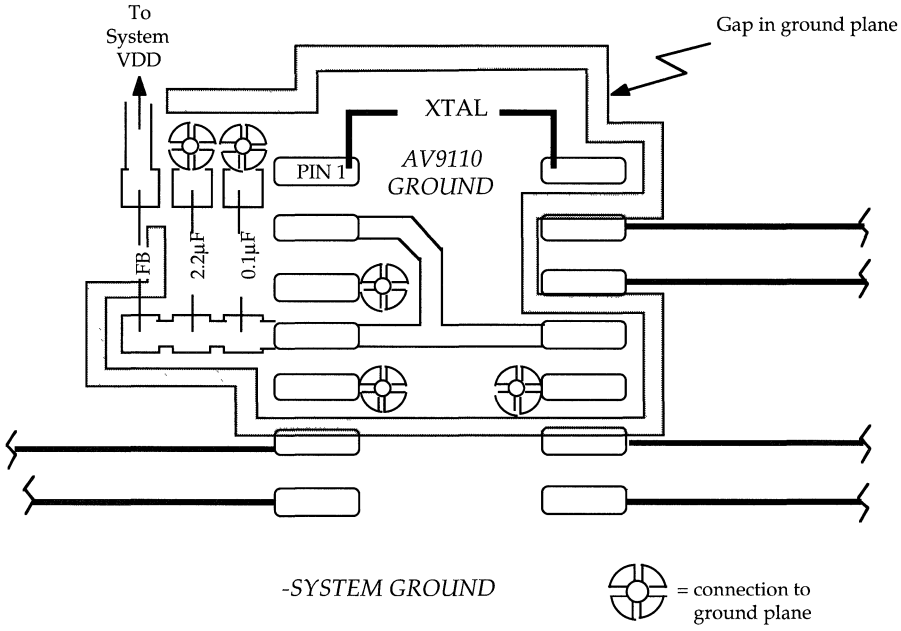


Using AV9110-02 with a crystal



Using AV9110-02 with an external clock

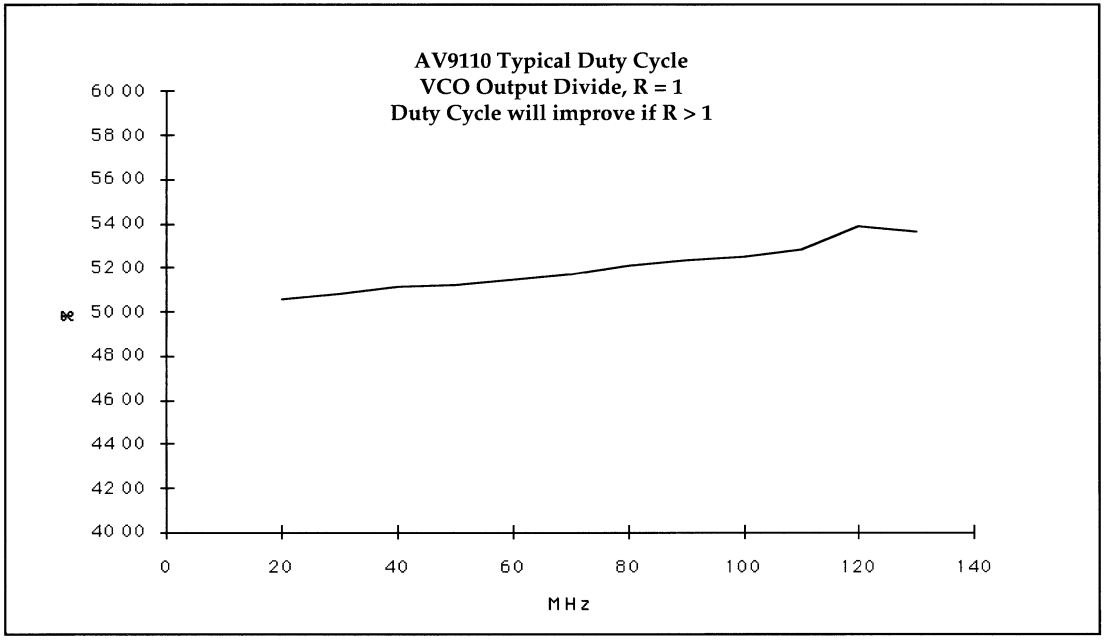
AV9110
Recommended Board Layout

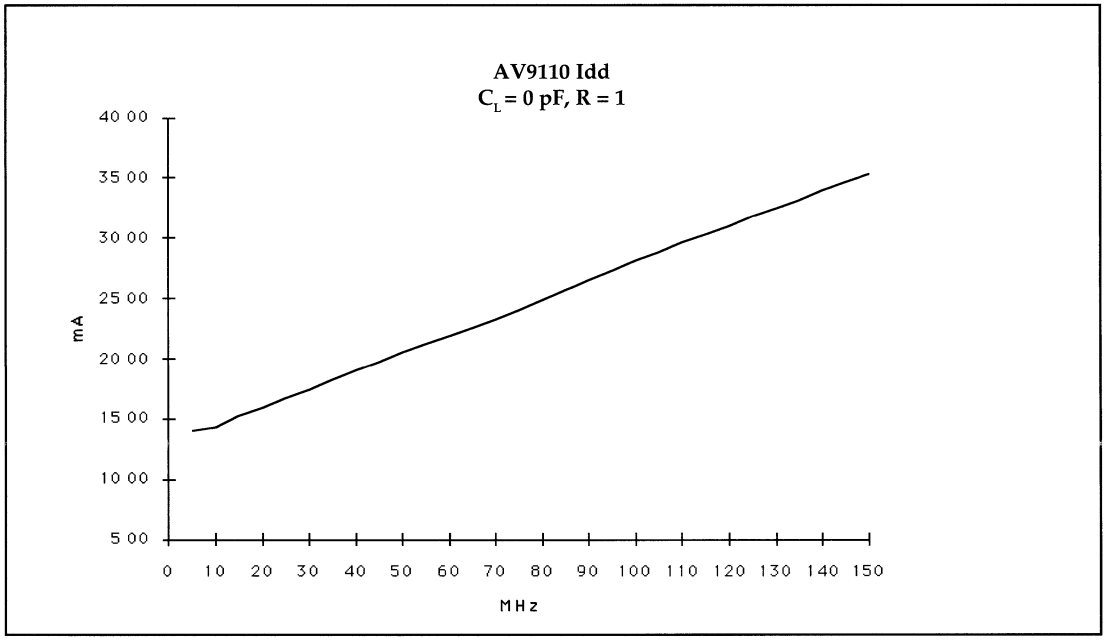


This is the recommended layout for the AV9110 to maximize clock performance. Shown are the power and ground connections, the ground plane, and the input/output traces.

Use of the isolated ground plane and power connection, as shown, will prevent stray high frequency ground and system noise from coupling to the AV9110. As when compared to using the system ground and power planes, this technique will lessen output clock jitter. The isolated ground plane should be connected to the system ground plane at one point, near the 2.2µF decoupling cap. For lowest jitter performance, this isolated ground plane should be kept away from clock output pins and traces. Keeping the isolated ground plane area as small as possible will minimize EMI radiation. Use a sufficient gap between the isolated ground plane and system ground plane to prevent AC coupling. The ferrite bead in the VDD line is optional, but will help reduce EMI.

The traces to distribute the output clocks should be over an unbroken system ground or power supply plane. The trace width should be about two times the thickness of the PC board between the trace and the underlying plane. These guidelines help minimize clock jitter and EMI radiation. The traces to distribute power should be as wide as possible.


AV9110 Typical Duty Cycle
VCO Output Divide, R = 1
Duty Cycle will improve if R > 1
60 00
58 00
56 00
54 00
52 00
50 00
48 00
46 00
44 00
42 00
40 00
%
0
20
40
60
80
100
120
140
MHz


AV9110 Idd
C_L = 0 pF, R = 1
40 00
35 00
30 00
25 00
20 00
15 00
10 00
5 00
mA
0
10
20
30
40
50
60
70
80
90
100
110
120
130
140
150
MHz

Ordering Information

Part Number	Temperature Range	Package Type
AV9110-01CN14	0°C to +70°C	14 lead Plastic DIP
AV9110-01CS14	0°C to +70°C	14 lead SOIC 150 mil wide
AV9110-02CN14	0°C to +70°C	14 lead Plastic DIP
AV9110-02CS14	0°C to +70°C	14 lead SOIC 150 mil wide

Integrated Circuit Systems, Inc.

ICS9123

Advance Information

High Resolution Frequency Generator

Features

- Cost effective solution for MODEM, ETHERNET and AD1848 applications
- Three independent PLL's
- Four clock frequencies generated from one crystal
- One high resolution PLL provides ± 50 PPM accuracy
- Eight ROM based frequency selections for the high resolution PLL1
- Four ROM based frequency selections each for PLL2 and PLL3
- 3V or 5V power supply
- On chip loop filter components
- Low power CMOS technology
- 20 or 16 pin PDIP or SOIC package

General Description

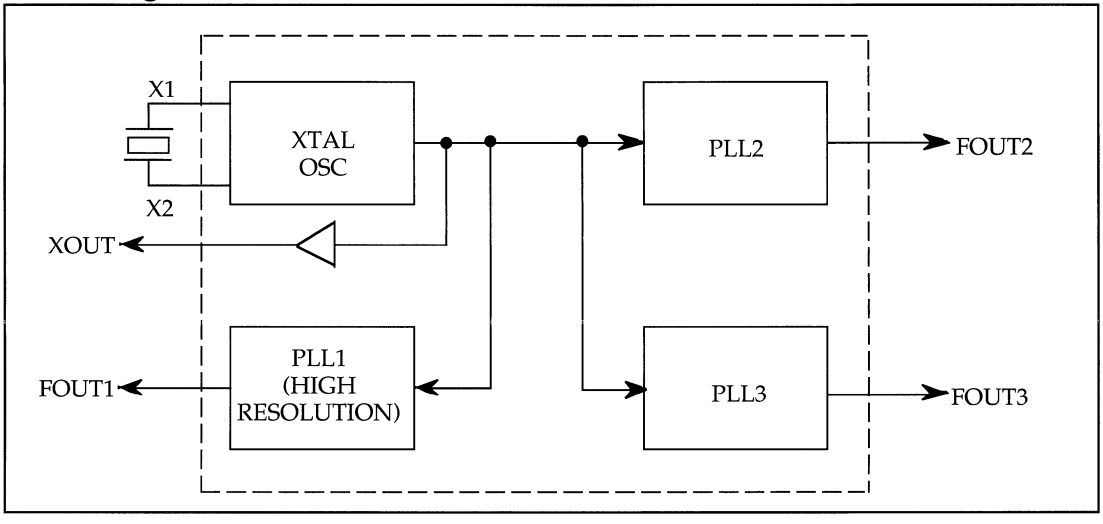
The ICS9123 is a multiple output frequency generator ultilizing PLL (Phase Lock Loop) frequency synthesis. It contains three PLL frequency synthesizers and an internal crystal oscillator reference circuit. Thus, with only an external crystal and the necessary power supply decoupling capacitors, four different output clock frequencies can be provided.

PLL1 of the device has the ability to provide high output frequency resolution (±50 ppm). This makes it suitable for providing clocks for system functions such as modems, ethernet, and sound synthesis. PLL2 and PLL3 provide output clocks for other system applications such as microprocessors and DSP chips. For example, in modem applications, the ICS9123 generates the high resolution clock generator for the A/D converter and two lower resolution clocks for the microprocessor and DSP.

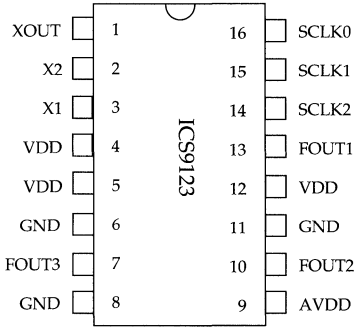
Each of the PLL clock generators has a ROM based frequency selection table which is addressed through device input pins. PLL1 has eight frequency select locations; PLL2 and PLL3 each has four. The ROM based tables are preprogrammed. However, they can be customized for the user specific applications.

D

Block Diagram



Pin Configuration



Decoding Table for Clock Frequency (Using 14.31818 MHz Input Frequency)

SCLK2 2	SCLK21	SCLK20	FOUT1* (MHZ)	FOUT2 (MHZ)	FOUT3 (MHZ)
					29.5
0	0	0	8.06400	19.7	8.06
0	0	1	19.66080	29.5	19.7
0	1	0	29.49120	8.06	16.5
0	1	1	11.05920	14.6	29.5
1	0	0	13.82400	19.7	8.06
1	0	1	3.68640	29.5	19.7
1	1	0	14.74560	8.06	16.5
1	1	1	16.00031	14.6	

* FOUT1 frequencies shown are accurate to within 2 PPM

Pin Description

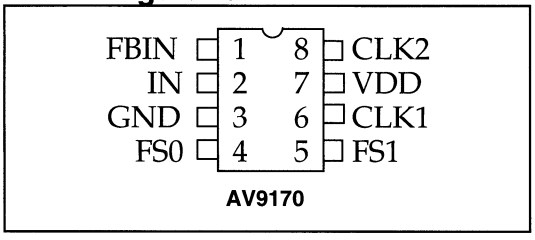
Pin Name	Pin #	Pin type	Description
XOUT	1	Output	Crystal buffered output
X2	2	Output	Connect crystal
X1	3	Input	Connect crystal
VDD	4	-	3V or 5V power supply
VDD	5	-	3V or 5V power supply
GND	6	-	GROUND
FOUT3	7	Output	Output frequency of one of 3 PLL's
GND	8	-	GROUND
VDD	9	-	3V or 5V power supply
FOUT2	10	Output	Output frequency of one of 3 PLL's
GND	11	-	GROUND
VDD	12	-	3V or 5V power supply
FOUT1	13	Output	Output frequency of the high resolution PLL
SCLK2	14	Input	CPU clock frequency SELECT 2
SCLK1	15	Input	CPU clock frequency SELECT 1
SCLK20	16	Input	CPU clock frequency SELECT 0

Clock Synchronizer and Multiplier

Features

- On chip Phase Locked Loop for clock synchronization
- Synchronizes frequencies up to 100 MHz (output)
- ±1ns skew (max) between input and output clocks
- Can recover poor duty cycle clocks
- CLK1 and CLK2 skew controlled to within ±1ns
- 5 volt only power supply
- Low power CMOS technology
- Small 8 pin DIP or SOIC package
- On chip loop filter
- AV9170-01, -04 for output clocks 20-100 MHz
- AV9170-02, -05 for output clocks 5-25 MHz

Pin Configuration



Description

The AV9170 generates an output clock which is synchronized to a given continuous input clock with zero delay (±1ns). Using ICS' proprietary phase locked loop (PLL) analog CMOS technology, the AV9170 is useful for regenerating clocks in high speed systems where skew is a major concern. By the use of the two select pins, multiples or divisions of the input clock can be generated with zero delay (see Tables 2 and 3). The standard versions produce two outputs, where CLK2 is always a divide by two version of CLK1.

The AV9170 is also useful to recover poor duty cycle clocks. A 50 MHz signal with a 20/80% duty cycle, for example, can be regenerated to the 48/52% typical of the part.

The AV9170 allows the user to control the PLL feedback, making it possible, with an additional 74F240 octal buffer (or other such device that offers controlled skew outputs), to synchronize up to 8 output clocks with zero delay compared to the input (see Figure 1).

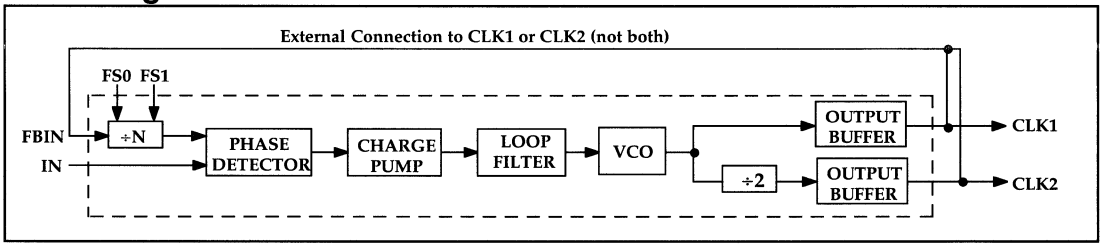
Application notes for the AV9170 are available. Please consult ICS.

D

Pin Description

Pin Name	Pin #	Type	Description
FBIN	1	Input	FEEDBACK INPUT
IN	2	Input	INPUT for reference clock
GND	3	-	GROUND
FS0	4	Input	FREQUENCY SELECT 0
FS1	5	Input	FREQUENCY SELECT 1
CLK1	6	Output	CLOCK output 1 (See Tables 1, 2, 3, 6, 7 for values)
VDD	7	-	Power Supply (+5V)
CLK2	8	Output	CLOCK output 2 (See Tables 1, 2, 3, 6, 7 for values)

Block Diagram



Using the AV9170

The AV9170 has the following characteristics:

1. Rising edges at IN and FBIN are lined up. Falling edges are not synchronized.

2. The relationship between the frequencies at FBIN and IN is shown in Table 1.

TABLE 1

FS1	FS0	f_{FBIN} (-01, -02)	f_{FBIN} (-04, -05)
0	0	$2 \cdot f_{IN}$	$3 \cdot f_{IN}$
0	1	$4 \cdot f_{IN}$	$5 \cdot f_{IN}$
1	0	f_{IN}	$6 \cdot f_{IN}$
1	1	$8 \cdot f_{IN}$	$10 \cdot f_{IN}$

3. The frequency of CLK2 is half the CLK1 frequency.

4. The CLK1 frequency ranges are:

AV9170-01, -04 $\quad 20 < f_{CLK1} < 100MHz$

AV9170-02, -05 $\quad 5 < f_{CLK1} < 25\ MHz$

The AV9170 will only operate correctly within these frequency ranges.

Eliminate High Speed Clock Routing Problems

The AV9170 makes it possible to route lower speed clocks over long distances on the PC board, and to place an AV9170 next to the device requiring a higher speed clock. The multiplied output can then be used to produce a phase locked, higher speed output clock.

Compensate for Propagation Delays

Including an AV9170 in a timing loop allows the use of PALs, gate arrays, etc., with loose timing specifications. The AV9170 compensates for the delay through the PAL and synchronizes the output to the input reference clock.

Operating Frequency Range

The AV9170 is offered in versions optimized for operation in two frequency ranges. The -01 and -04 cover high frequencies, 20 to 100 MHz. The -02 and -05 operate from 5 to 25 MHz. The AV9170 can be supplied with custom multiplication factors and operating ranges. Consult ICS for details.

Application of AV9170 for Multiple Outputs

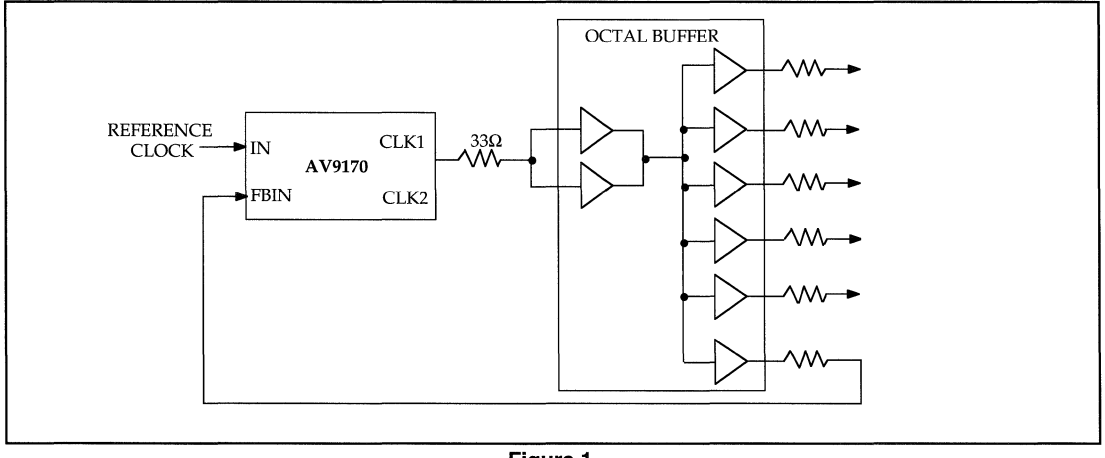


Figure 1

Using CLK2 Feedback

Connecting CLK2 to FBIN as shown in Figure 2 will cause all of the rising edges to be aligned (Fig. 4).

Using CLK1 Feedback

With CLK1 connected to FBIN as shown in Figure 3, the input and CLK1 output will be aligned on the rising edge, but CLK2 can be either rising or falling (Fig. 5). Consult ICS if the CLK1 frequency is desired to be higher than 100 MHz.

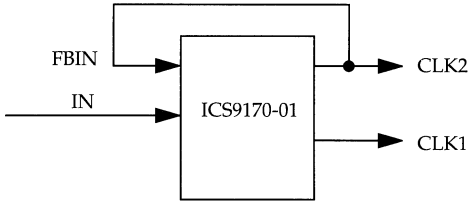


Figure 2
For CLK2 frequencies 10 - 50 MHz (-01)
For CLK2 frequencies 2.5 - 12.5 MHz (-02)

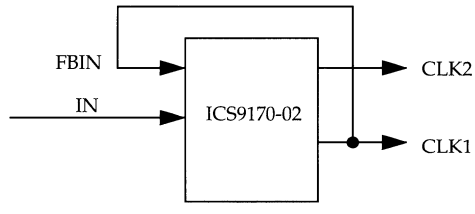


Figure 3
For CLK1 frequencies 20 - 100 MHz (-01)
For CLK1 frequencies 5 - 25 MHz (-02)

FS1	FS0	CLK1	CLK2
0	0	INx4	INx2
0	1	INx8	INx4
1	0	INx2	IN
1	1	INx16	INx8

Table 2
Decoding Table for AV9170-01, 2 with CLK2 Feedback

FS1	FS0	CLK1	CLK2
0	0	INx2	IN
0	1	INx4	INx2
1	0	IN	IN÷2
1	1	INx8	INx4

Table 3
Decoding Table for AV9170-01, 2 with CLK1 Feedback

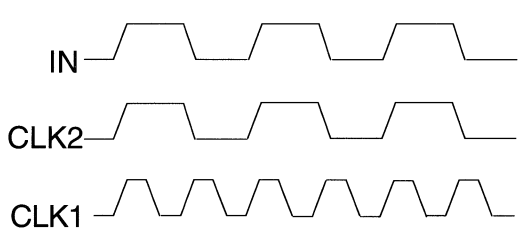


Figure 4
Input and Output Clock Waveforms with CLK2 Connected to FBIN

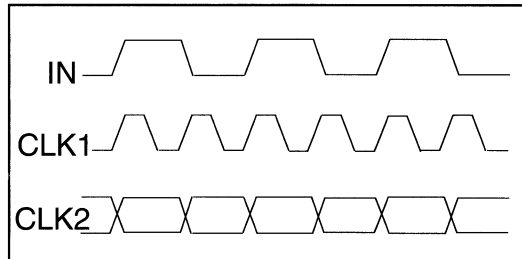


Figure 5
Input and Output Clock Waveforms with CLK1 Connected to FBIN

Using CLK2 Feedback

Connecting CLK2 to FBIN as shown in Figure 2 will cause all of the rising edges to be aligned (Fig. 4).

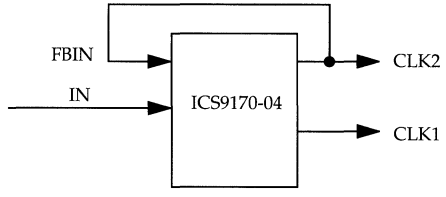


Figure 6
For CLK2 frequencies 10 - 50 MHz (-04)
For CLK2 frequencies 2.5 - 12.5 MHz (-05)

FS1	FS0	CLK1	CLK2
0	0	INx6	INx3
0	1	INx10	INx5
1	0	INx12	INx6
1	1	INx20	INx10

Table 6
Decoding Table for AV9170-04, 5 with CLK2 Feedback

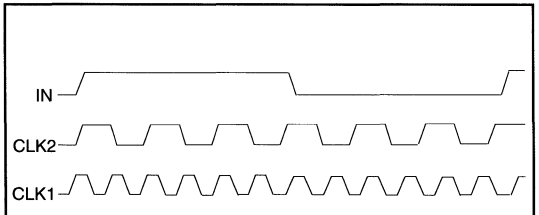


Figure 8
Input and Output Clock Waveforms with CLK2 Connected to FBIN

Using CLK1 Feedback

With CLK1 connected to FBIN as shown in Figure 3, the input and CLK1 output will be aligned on the rising edge, but CLK2 can be either rising or falling (Fig. 5). Consult ICS if the CLK1 frequency is desired to be higher than 100 MHz.

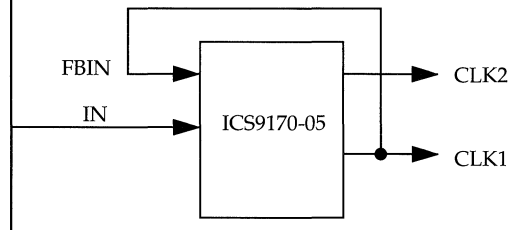


Figure 7
For CLK1 frequencies 20 - 100 MHz (-04)
For CLK1 frequencies 5 - 25 MHz (-05)

FS1	FS0	CLK1	CLK2
0	0	INx3	INx1.5
0	1	INx5	INx2.5
1	0	INx6	INx3
1	1	INx10	INx5

Table 7
Decoding Table for AV9170-04, 5 with CLK1 Feedback

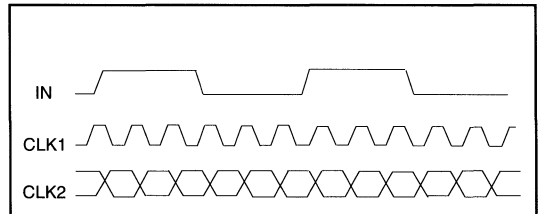


Figure 9
Input and Output Clock Waveforms with CLK1 Connected to FBIN

Absolute Maximum Ratings

VDD referenced to GND..... 7V
Operating temperature under bias..... 0°C to +70°C
Storage temperature..... -65°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation..... 0.5 Watts

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device This is a stress rating only, and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum conditions for extended periods may affect the reliability of the device.

Electrical Characteristics

(V_{DD}= +5V± 5%, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage	-	-	0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0	-	-	V	V_{DD} = 5V
I_{IL}	Input Low Current	-5	-	5	µA	V_{IN} = 0V
I_{IH}	Input High Current	-5	-	5	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage	-	-	0.4	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	V_{DD}-.4V	-	-	V	I_{OH} = -1mA,V_{DD}=5.0V
V_{OH}	Output High Voltage	V_{DD}-.8V	-	-	V	I_{OH} = -4mA,V_{DD}=5.0V
V_{OH}	Output High Voltage	2.4	-	-	V	I_{OH} = -8mA
I_{DD}	Supply Current	-	20	50	mA	Unloaded, 100MHz
AC Characteristics						
$ICLK_r$	Input Clock Rise Time	-	-	10	ns	
$ICLK_f$	Input Clock Fall Time	-	-	10	ns	
t_r	Output Rise time, 0.8 to 2.0V	-	1	2	ns	15 pf load
t_r	Rise time, 20% to 80% V_{DD}	-	2	4	ns	15 pf load
t_f	Output Fall time, 2.0 to 0.8V	-	1	2	ns	15 pf load
t_f	Fall time, 80% to 20% V_{DD}	-	2	4	ns	15 pf load
d_t	Output Duty cycle, AV9170-01	40	48/52	60	%	15 pf load. Note 2, 3
d_t	Output Duty cycle, AV9170-02	45	49/51	55	%	15 pf load. Note 2, 3
T_{1s}	Jitter, 1 sigma	-500	±120	300	ps	
T^{abs}	Jitter, absolute	-2%	±250	500	ps	For CLK1 > 10 MHz
T^{abs}	Jitter, absolute			2	%	For CLK1 < 10 MHz
f_i	Input Frequency	1		67	MHz	Note 1
f_o	Output Frequency CLK1	20		100	MHz	AV9170-01, -04
f_o	Output Frequency CLK1	5		25	MHz	AV9170-02, -05
t_{skew1}	FBIN to IN skew	-1	0.4	1	ns	Note 2, 4. Input rise time <5ns
t_{skew1}	FBIN to IN skew	-2	0.6	2	ns	Note 2, 4. Input rise time <10ns
t_{skew2}	CLK1 to CLK2 skew	-1	0.4	1	ns	Note 2, 4

NOTES:
1. It may be possible to operate the AV9170 outside of these ranges. Consult ICS for your specific application.
2. All a.c. specifications are measured with a 50Ω transmission line, load terminated with 50Ω to 1.4V.
3. Duty cycle measured at 1.4V.
4. Skew measured at 1.4V on rising edges.

Ordering Information

Part Number	Part Marking	Temperature Range	Package Type
AV9170-xxCC8	AV9170-xx	0°C to +70°C	8 lead CERDIP
AV9170-xxCN8	AV9170-xx	0°C to +70°C	8 lead Plastic DIP (300 mils)
AV9170-xxCS8	ICS70-x	0°C to +70°C	8 lead SOIC (150 mils)

For the SOIC package, the AV9170-01 is marked ICS70-1, and the AV9170-02 is marked ICS70-2.

Clock Synchronizer and Multiplier

1. Overview

This AV9170 Application Note provides theory of operation, application examples, and design hints for the device. It is intended to provide the reader a broader understanding of the device beyond the scope of the AV9170 data sheet.

2. Theory of Operation

To gain maximum benefit from the AV9170, it is first important to understand how the AV9170 works.

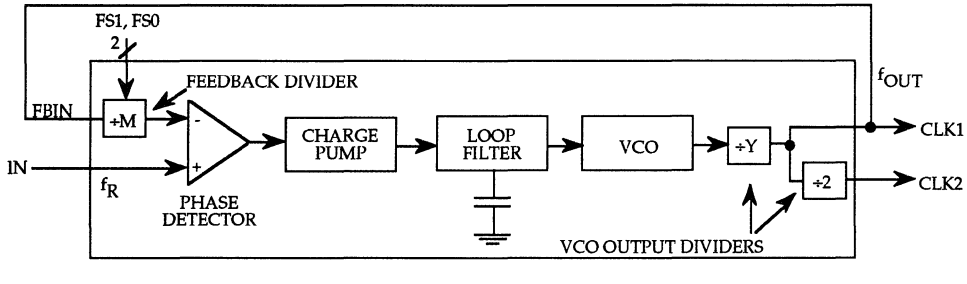
The AV9170 is a basic PLL (Phase-Locked-Loop) analog building block that is optimized for system clock applications. A complete block diagram of the AV9170-01/02 is shown in Figure 1. Unlike a simple clock buffer, the AV9170 contains an internal analog oscillator which generates a clock signal. This clock is kept in phase-lock with an input reference clock by the PLL.

2.1 Principles of Phase Lock Operation

Figure 1 displays a block diagram of a typical phase locked loop system. The elements of the system are a phase detector, charge pump, loop filter, Voltage Controlled Oscillator (VCO), and divider block.

The VCO is an oscillator whose output clock frequency is proportional to its input voltage. During normal operation, this input voltage to this oscillator is forced to a given value to produce the desired output frequency. The phase detector has two input clocks, one that is the input reference frequency (f_R), and a second that is a scaled version of the output; f_{OUT}/M (M is an integer value). The output of the phase detector is a low frequency signal that is proportional to the phase difference between the rising edges of these two input signals. The phase detector then controls the charge pump. The loop filter converts the output of the charge pump to a voltage and eliminates any high frequency components. The loop filter voltage is the VCO input voltage, completing the loop. The phase locked loop system causes the frequencies f_R and f_{OUT}/M to be equal. If, for example, f_{OUT}/M drifts to a higher frequency, an error signal is generated by the phase detector to reduce the input voltage to the VCO, causing the output frequency to be forced back to the desired value. Because of this feedback mechanism, a stable output frequency can be synthesized that is proportional to a reference frequency. The relationship between f_{OUT} and f_R can be summarized by the following equation:

$$f_{OUT} = (M)(f_R)$$



FS1	FS0	+M
0	0	2
0	1	4
1	0	1
1	1	8

DEVICE	+Y
AV9170-01	1
AV9170-02	4

Figure 1
AV9170 Complete Block Diagram

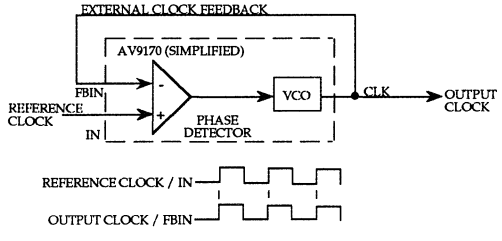


Figure 2
Phase Locked Loop Principle of AV9170

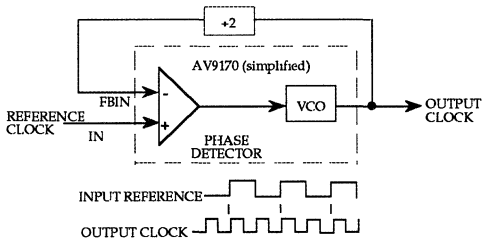


Figure 3
Example of Clock Multiplication by PLL

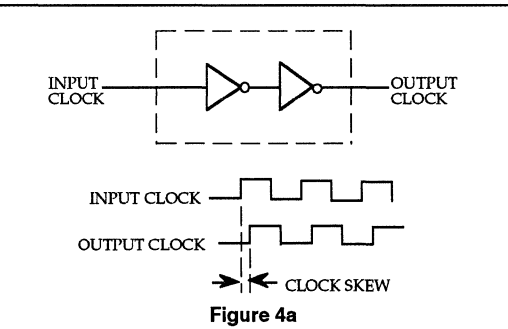


Figure 4a
Example of Delay in Clock Line

Figure 2 shows a simplified block diagram of the AV9170 and the relationship between the input and output clock when the loop is stable and no feedback division is used. The rising edges of "IN" and "FBIN" will occur within 1 nsec of each other. Figure 3 illustrates the resulting clock multiplication when a feedback divider (internal or external) is used.

2.2 AV9170 VCO Parameters

The AV9170's internal clock oscillator is a VCO that runs optimally over the range of 20-100 MHz. This operation range will provide duty cycle and jitter performance which is guaranteed in the AV9170 data sheet. In Figure 1 it can be seen that the VCO output can pass through one or two dividers, depending on which output is used. By using these dividers, this 20-100 MHz VCO frequency range can be translated to lower clock output frequencies. For example, the AV9170-02 can provide final clock output range as low as 1.25-6.25 MHz at CLK2 (the VCO frequency divided by 16).

Actual minimum speed of the AV9170 VCO operation is about 4 MHz. For example, when no reference clock is present at pin IN, the VCO will slow down to this minimum speed but will not stop.

The AV9170 loop filter adds the low-pass loop compensation necessary for loop stability. The AV9170-01 and AV9170-02 are compensated such that the VCO can make full range frequency changes and settle within approximately 200 µsec.

3. AV9170 Applications

3.1 Compensating for Circuit Delay in the Clock Path

Figure 4A illustrates an important problem associated with the distribution of high-speed clocks. Any time the clock signal passes through circuitry (gates, gate arrays, PALs, buffers, etc.) it acquires a time delay. Uncontrolled delays cause the set-up and hold times of various integrated circuits to be violated. Also, race conditions between two signals can be generated when the proper timing sequence is corrupted.

By virtue of the external clock feedback path, the AV9170 can be used to overcome such circuit delay so that the input and output clocks are in phase with no skew. This is illustrated by Figure 4B. In this circuit, the AV9170 is actually producing a clock output that is skewed *ahead* of the input reference clock to compensate for the circuit delay. The circuit delay represented in Figure 4b must be constant and continuous for the VCO/PLL to remain in lock. The circuit delay can be of any magnitude (even many clock cycles) and also inverted, but these parameters must remain constant.

Figure 4C shows an example of the AV9170 used to compensate for clock delay caused by a particular digital IC. In this example, the IC causes clock delay and also internally divides the clock by two. The divide-by-two in the digital IC is compensated for by the feedback loop such that the frequencies at IN and FBIN are identical as selected by FS0 and FS1.

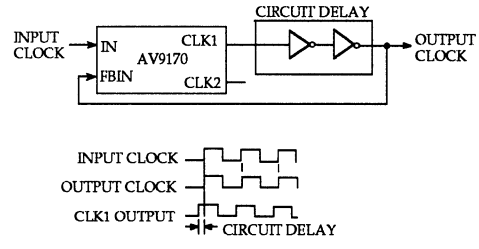


Figure 4b
Overcoming Circuit Delay with the AV9170

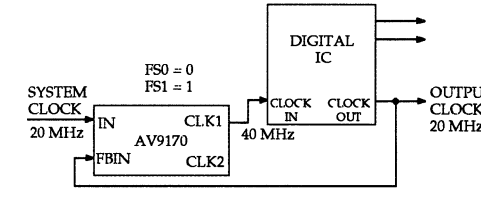


Figure 4c
Example of Restoring Clock Skew with the AV9170

3.2 Clock Buffering Using the AV9170

Alone, the AV9170 is designed to drive loads of up to 25 pf. Additional buffering can be accomplished with the simple circuit of Figure 5 (using either an inverting or non-inverting logic buffer). Because of transmission line effects involved when using high speed clocks (standing waves, etc.), it is a good idea to drive only one or two loads per clock driver. It is therefor best to use multiple output buffers when driving multiple loads.

Figure 6 shows a multiple output clock buffer implementation using the AV9170 and an octal buffer IC, such as the 74F240 family. The buffers are cascaded to avoid exceeding the output load capacitance limit of the AV9170 or the buffer circuits. Since the buffers are all integrated on a single monolithic device, clock delay is typically well matched. Thus, one buffer output can be used for the clock feedback, and then all the outputs are de-skewed to the reference clock. To ensure good phase matching between outputs, it is important that the outputs are similarly loaded (with about the same load capacitance). Optimum results are achieved when the buffer used for clock feedback is used for no other purpose. Otherwise, additional noise and/or standing waves caused by multiple loading could impose unwanted clock jitter or poor skew control characteristics.

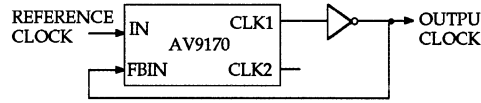


Figure 5
Simple Clock Buffer

3.3 Additional Output Clock Frequency Multiplication

Figure 7 illustrates the use of an external divider circuit in the AV9170 feedback path. By compounding the total divide ratio in the clock feedback path, this can be used to further multiply the VCO or output frequency. This is because the feedback loop maintains the frequency relationship between f_{IN} and f_{FBIN} as described in the data sheet. Input to output skew integrity is not maintained by this circuit, however, due to logic delay in the feedback path. Also keep in mind that VCO frequency must be kept within 20-100 MHz for stable operation. IN and FBIN signal frequencies should be kept within 0.5-67 MHz.

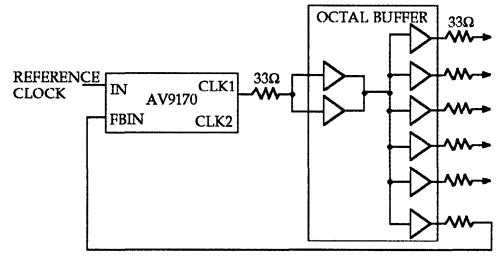


Figure 6
Zero Skew Multiple Output Clock Buffer

3.4 Restoring Clock Duty Cycle

The AV9170 output clocks, generated by the internal VCO, maintains excellent duty cycle characteristics. Output duty cycle from CLK1 and CLK2 is typically close to 50/50% (logic high time / logic low time), but will be within 40/60-60/40%, as specified in the AV9170 data sheet. But because the AV9170 only responds to rising clock edges at pin IN and FBIN, the device is less sensitive to input duty cycle than most logic chips. Thus, the AV9170 can be used in applications where duty cycle needs to be restored, as illustrated in Figure 8.

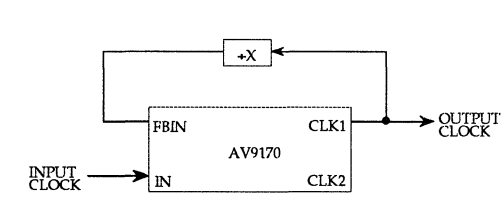


Figure 7
Additional Clock Output Frequency Multiplication by Factor "X"

Many digital ICs have a specified duty cycle limit on the clock input. Some clock sources, even some crystal oscillators, produce poor duty cycles or output waveforms which can violate these input clock specifications. Such waveforms are acceptable, however, for driving the AV9170. This is where using the AV9170 as a clock buffer can be useful. Duty cycle and clean clock edges are particularly important for those devices that utilize both the rising and falling edge of the input clock.

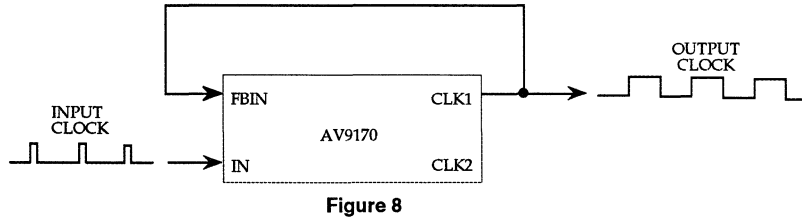


Figure 8
Restoring Clock Duty Cycle

3.5 Reducing Clock Distribution Frequency

One of the difficulties with high frequency system clocks is distribution. For example, clocks above 50 MHz or so can be difficult to pass through an edge connector bandwidth limitations. A long, high frequency clock trace can also produce undesirable EMI. One way around these problems is to use a lower clock frequency for distribution and then multiply up the frequency at the destination with the AV9170.

Figure 9 illustrates such an application. Here, an AV9155 is used to provide a 2X local CPU clock. The otherwise unused AV9155 1X output clock is used for remote distribution across a board connector. An AV9170 is then used to create the de-skewed 2X clock at the destination.

4. Practical Design Considerations

4.1 Circuit Skew Rates

For good output skew control, it is important that the circuitry driving IN and FBIN have similar rise times. Fast rise times are safest to avoid false triggering by noise (a fast rise time essentially functions as a low pass filter). Input threshold voltage of IN and FBIN is typically 1.4 volts (halfway between the Vil and Vih specifications). The outputs CLK1 and CLK2 have a typical rise time of 2 nsec.

4.2 Input Reference Clock Requirements

Since the AV9170 operation depends on a stable VCO/PLL condition, it can only operate with continuous frequency clock signals. It cannot be applied to non-continuous digital signals. The device will track a changing clock frequency (the VCO can change over its entire range in about 100 µsec) but may require about 200 µsec to fully lock in, depending on rate of change. In most applications, a few missing clock pulses will not greatly upset the stability of the output clock but may cause cycle slip. These input requirements are true for both the IN and FBIN inputs.

4.3 Circuit and Layout Considerations

When using the AV9170 in a digital system clock application, an inherently sensitive analog IC is placed in an environment with digital noise. Noise is easily coupled into the device via ground and VDD connections and through input and output pins. The AV9170 is designed to have excellent power supply rejection, but care must

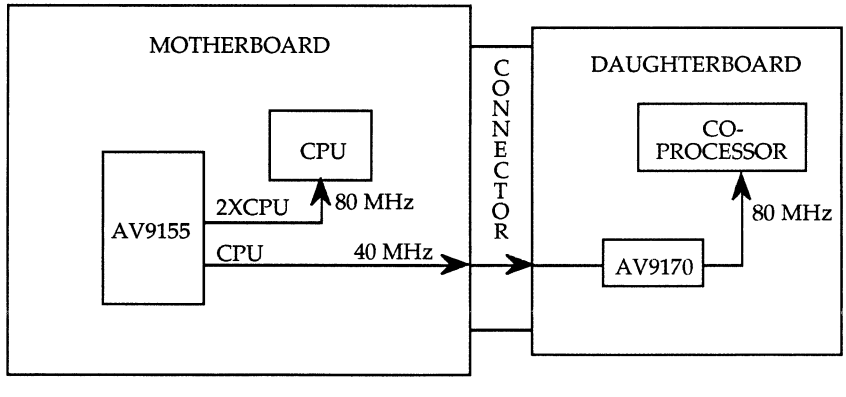


Figure 9
Lower Speed Clock Distribution

be used in circuit design and layout to minimize noise coupling. Using the guidelines given below will help ensure stable, low-jitter clock performance.

For EMI sensitive applications, clock signals are one of the biggest causes for FCC rejection. This is due to their continuous, single-frequency character that is easily picked up in the narrow band emitted frequency test. Following the circuit and layout guidelines below will help reduce EMI.

Figure 10 provides the AV9170 recommended external circuit, not including any additional feedback circuitry. A single power supply connection should be used to all device pins. The 0.1 µF decoupling capacitor should be located as close to the VDD pin as possible. Above 50 MHz output frequencies, it may be helpful to replace the 0.1 µF capacitor with a lower value, such as 0.01 µF, to better decouple higher frequencies. The ferrite bead shown in the VDD line does not enhance the AV9170 performance, but it will reduce EMI radiation from the VDD line caused by AV9170 dynamic loading. External feedback circuitry should have its own power supply connection and decoupling capacitors.

Except for very short clock output lines going to only one load, it is good practice to use a 33 ohm series termination resistor on the output clock line, as shown in Figure 10. It should be placed close to the AV9170 output. This will help reduce EMI and apparent clock jitter by damping standing waves caused by wave reflection at the end of the signal trace (which acts as a transmission line).

The recommended AV9170 PC board layout is shown in Figure 11. The optional 33 ohm output termination resistors or ferrite bead are not shown.

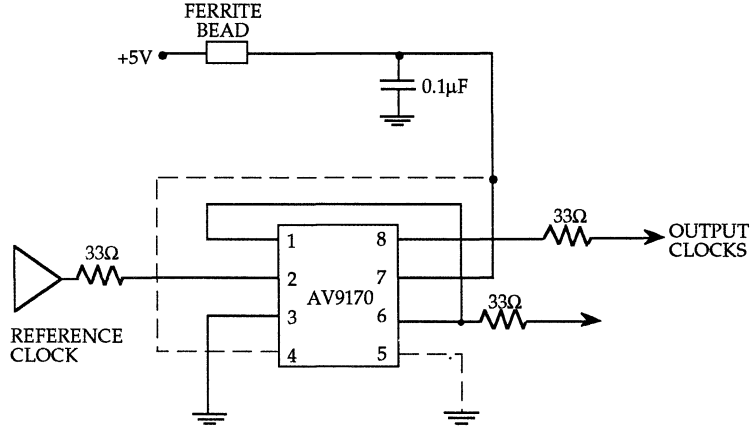


Figure 10
AV9170 Recommended Circuit Configuration
(arbitrary configuration of CLK1 feedback and pin 4, 5 logic states)

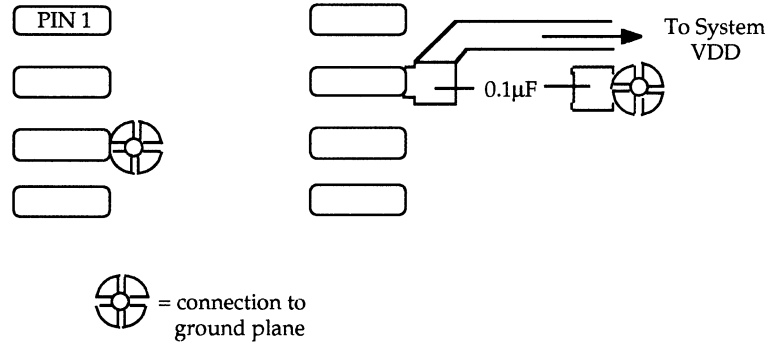


Figure 11
AV9170 Board Layout

D

5.0 Summary

The AV9170 is extremely flexible and provides utility in a wide range of system clock and other applications, not limited to those discussed in this application note. A related product is the AV9173, which is designed for video genlock (clock recovery) applications. Please refer to the AV9173 data sheet. The AV9170 may have applications in similar circuits as well. If this application note does not answer all of your AV9170 questions, please call ICS's applications department.

be used in circuit design and layout to minimize noise coupling. Using the guidelines given below will help ensure stable, low-jitter clock performance.

For EMI sensitive applications, clock signals are one of the biggest causes for FCC rejection. This is due to their continuous, single-frequency character that is easily picked up in the narrow band emitted frequency test. Following the circuit and layout guidelines below will help reduce EMI.

Figure 10 provides the AV9170 recommended external circuit, not including any additional feedback circuitry. A single power supply connection should be used to all device pins. The 0.1 µF decoupling capacitor should be located as close to the VDD pin as possible. Above 50 MHz output frequencies, it may be helpful to replace the 0.1 µF capacitor with a lower value, such as 0.01 µF, to better decouple higher frequencies. The ferrite bead shown in the VDD line does not enhance the AV9170 performance, but it will reduce EMI radiation from the VDD line caused by AV9170 dynamic loading. External feedback circuitry should have its own power supply connection and decoupling capacitors.

Except for very short clock output lines going to only one load, it is good practice to use a 33 ohm series termination resistor on the output clock line, as shown in Figure 10. It should be placed close to the AV9170 output. This will help reduce EMI and apparent clock jitter by damping standing waves caused by wave reflection at the end of the signal trace (which acts as a transmission line).

The recommended AV9170 PC board layout is shown in Figure 11. The optional 33 ohm output termination resistors or ferrite bead are not shown.

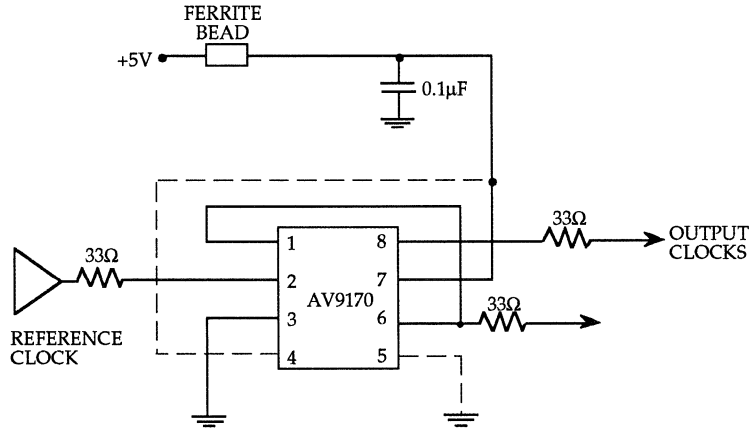


Figure 10
AV9170 Recommended Circuit Configuration
(arbitrary configuration of CLK1 feedback and pin 4, 5 logic states)

Low Skew Output Buffer

Features

- AV9172-01 is pin compatible with Gazelle GA1210E
- ±250ps skew (max) between outputs
- ±500ps skew (max) between input & outputs
- Input frequency range from 25 MHz to 50 MHz
- Output frequency range from 25 MHz to 100 MHz
- Special mode for two-phase clock generation
- Inputs and outputs are fully TTL compatible
- CMOS process results in low power supply current
- High drive, 25mA outputs
- Low cost
- 16 pin SOIC (300 mil) or 16 pin PDIP package

General Description

The AV9172 is designed to generate low skew clocks for clock distribution in high performance PCs and workstations. It uses phase-locked loop technology to align the phase and frequency of the output clocks with an input reference clock. Because the input to output skew is guaranteed to ±500ps, the part acts as a "zero delay" buffer.

The AV9172 has six configurable outputs. The AV9172-01 version has one output that runs at the same phase and frequency as the reference clock. A second output runs at the same frequency as the reference, but can either be in phase or 180° out of phase from the input clock. Two outputs are provided that are at twice the reference frequency and in phase with the reference clock. The final outputs can be programmed to be replicas of the 2x clocks or non-overlapping two phase clocks at twice the reference frequency. The AV9172-01 operates with input clocks from 25 MHz to 50 MHz while producing outputs from 25 MHz to 100 MHz.

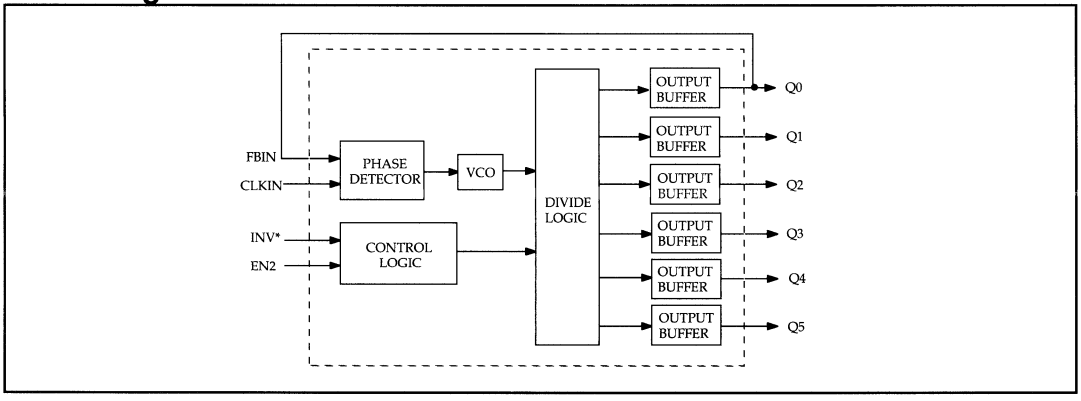
The use of a phase-locked loop (PLL) allows the output clocks to run at multiples of the input clock. This permits routing of a lower speed clock and local generation of a required high speed clock. Synchronization of the phase relationship between the input clock and the output clocks is accomplished when one output clock is connected to the input pin FBIN. The PLL circuitry matches rising edges of the input clock and output clocks.

The AV9172 is fabricated using CMOS technology which results in much lower power consumption and cost compared with the gallium arsenide based GA1210E. The typical operating current for the AV9172 is 50mA versus 120mA for the GA1210E.

ICS offers several versions of the AV9155. The different devices are shown below:

Part	Description
AV9172-01	Second source of GA1210
AV9172-03	Clock doubler and buffer
AV9172-07	Clock buffer

Block Diagram

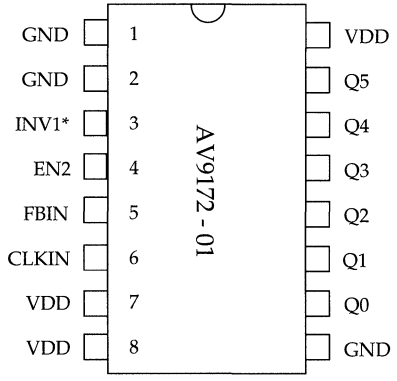


Configuration Table for 9172-01

EN2	INV1*	Q0	Q1	Q2	Q3	Q4	Q5
0	0	1X	1X*	2X	2X	2X	2X
0	1	1X	1X	2X	2X	2X	2X
1	0	1X	1X*	2X	2X	Ø1	Ø2
1	1	1X	1X	2X	2X	Ø1	Ø2

NOTES:
1. 1X designates that the output is a replica of CLKIN
2. 2X designates that the output is twice the frequency of CLKIN, and in phase
3. 1X* means that the output is at the same frequency and180° out of phase (inverted) from CLKIN
4. Ø1 will produce a 1/4 duty cycle clock of CLKIN
5. Ø2 will produce a 1/4 duty cycle clock delayed 180° from CLKIN

Pin Configuration

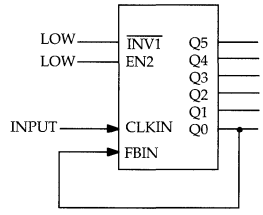


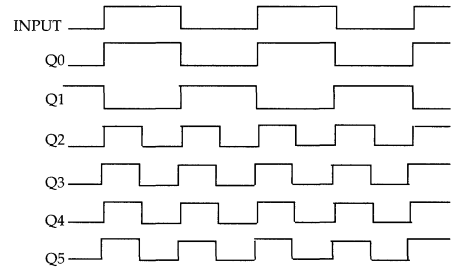
Pin Description for AV9172-01

PIN NAME	PIN #	PIN TYPE	DESCRIPTION
GND	1	-	GROUND
GND	2	-	GROUND
INV1*	3	Input	INV1* Inverts Q1 when low
EN	4	Input	EN converts Q4 and Q5 to phase clocks when high
FBIN	5	Input	FEEDBACK INPUT from output Q0
CLKIN	6	Input	INPUT for reference clock
VDD	7	-	Power supply (+5V)
VDD	8	-	Power supply (+5V)
GND	9	-	GROUND
Q0	10	Output	Q0 phase and frequency same as input (1X). Feed back to pin 5
Q1	11	Output	Q1 is a 1x clock in phase or 180° out of phase with input
Q2	12	Output	Q2 twice the frequency of Q0 (2x)
Q3	13	Output	Q3 twice the frequency of Q0 (2x)
Q4	14	Output	Q4 iseither a 2X clock or a two phase clock - see config. table
Q5	15	Output	Q5 is either a 2X clock or a two phase clock - see config. table
VDD	16	-	Power supply (+5V)

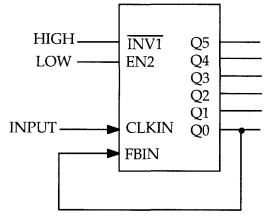
Timing Diagrams for 9172-01

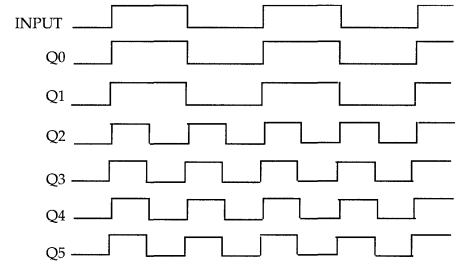
EN2 = 0 $\overline{\text{INV1}}$ = 0
FBIN = Q0



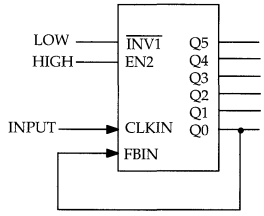


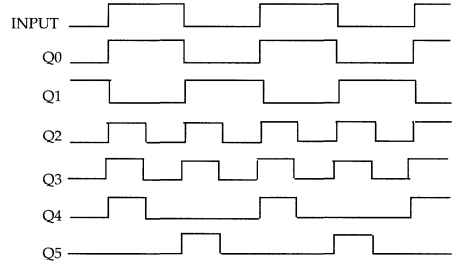
EN2 = 0 $\overline{\text{INV1}}$ = 1
FBIN = Q0



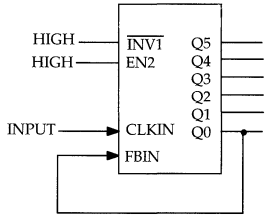


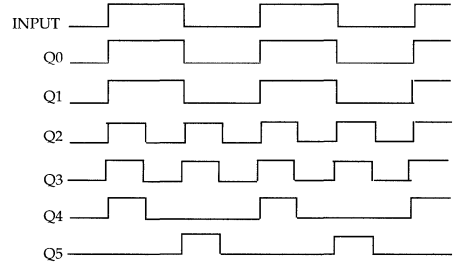
EN2 = 1 $\overline{\text{INV1}}$ = 0
FBIN = Q0





EN2 = 1 $\overline{\text{INV1}}$ = 1
FBIN = Q0



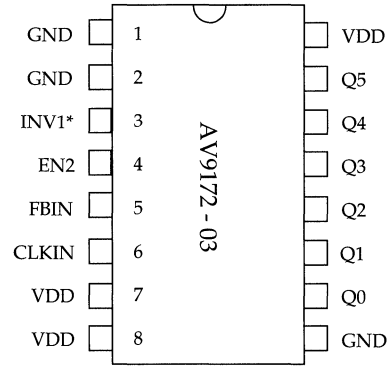


D

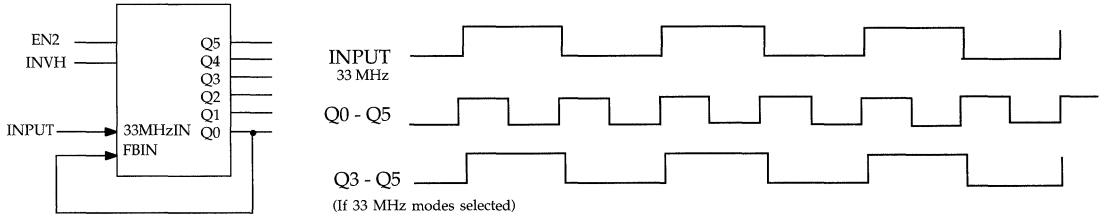
Configuration Table for AV9172-03 (33 MHz Input)

EN2	INV1*	Q0	Q1	Q2	Q3	Q4	Q5
0	0	66	66	66	66	66	66
1	0	66	66	66	66	66	33
0	1	66	66	66	33	33	66
1	1	66	66	66	33	33	33

Pin Configuration



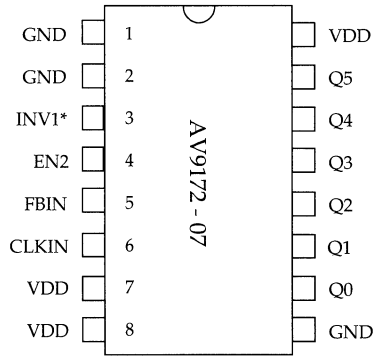
Timing Diagram for AV9172-03



Configuration Table for 9172-07 (66 MHz Input)

EN2	INV1*	Q0	Q1	Q2	Q3	Q4	Q5
0	0	66	66	66	66	66	66
1	0	66	66	66	66	66	33
0	1	66	66	66	33	33	66
1	1	66	66	66	33	33	33

Pin Configuration



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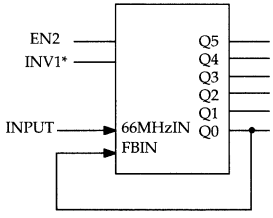
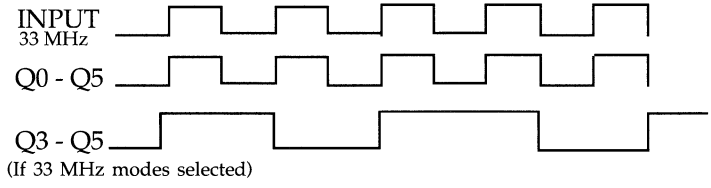
Timing Diagrams for AV9172-07





Absolute Maximum Ratings

VDD referenced to GND..... 7V
Operating temperature under bias..... 0°C to +70°C
Storage temperature..... -65°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation..... 0.5 Watts

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect the reliability of the device.

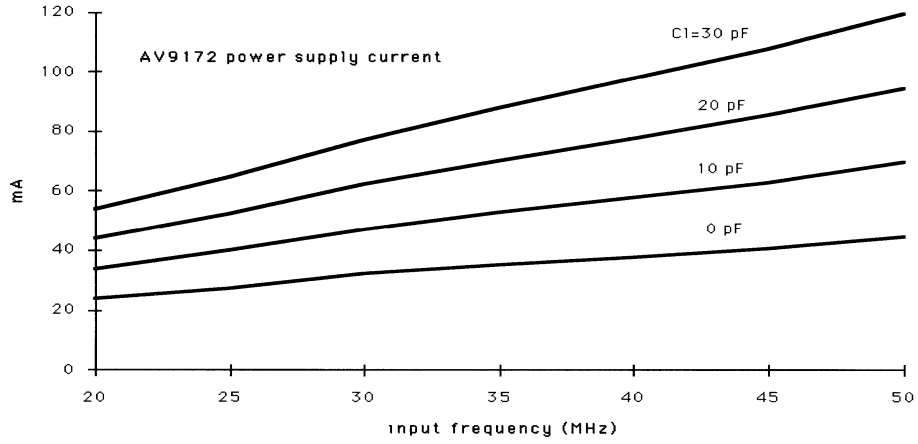
Electrical Characteristics

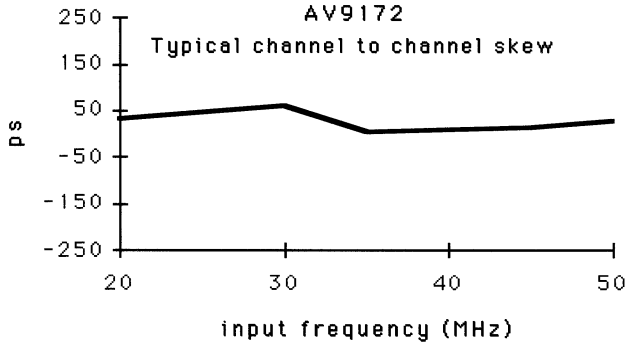
(V_{DD}= +5V± 5%, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage	-	-	0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0	-	-	V	V_{DD} = 5V
I_{IL}	Input Low Current	-5	-	5	µA	V_{IN} = 0V
I_{IH}	Input High Current	-5	-	5	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage	-	0.5	0.8	V	I_{OL} = 25mA
V_{OH}	Output High Voltage	2.4	-	-	V	I_{OH} = -25mA
I_{DD}	Supply Current	-	35	60	mA	Unloaded, 50MHz
AC Characteristics						
$ICLK_r$	Input Clock Rise Time	-	-	10	ns	
$ICLK_f$	Input Clock Fall Time	-	-	10	ns	
t_r	Output Rise time, 0.8 to 2.0V	-	0.7	1	ns	15 pf load
t_r	Rise time, 20% to 80% V_{DD}	-	1.2	2	ns	15 pf load
t_f	Output Fall time, 2.0 to 0.8V	-	0.7	1	ns	15 pf load
t_f	Fall time, 80% to 20% V_{DD}	-	1.2	2	ns	15 pf load
d_t	Output Duty cycle	45	49/51	55	%	15 pf load
T_{1s}	Jitter, 1 sigma		60		ps	
T_{abs}	Jitter, absolute		±200		ps	
f_i	Input Frequency	25		50	MHz	Note 1
f_o	Output Frequency	25		100	MHz	
t_{skew1}	FBIN to IN skew	-500	-300	500	ps	Note 2, 4. Input rise time <3ns
t_{skew1}	FBIN to IN skew	1000	-500	1000	ps	Note 2, 4. Input rise time <10ns
t_{skew2}	Skew between any 2 outputs at same frequency	-250	±50	250	ps	Note 2, 4
	Skew between any 2 outputs at different frequencies			500	ps	Note 2, 4

NOTES:
1. It may be possible to operate the AV9172 outside of these ranges. Consult ICS for your specific application.
2. All skew specifications are measured with a 50Ω transmission line, load terminated with 50Ω to 1.4V.
3. Duty cycle measured at 1.4V.
4. Skew measured at 1.4V on rising edges. Loading must be equal on outputs.

Typical Performance Characteristics





Ordering Information

Part Number	Part Marking	Temperature Range	Package Type
AV9172-xxCN16		0° C to +70° C	16 lead PDIP
AV9172-xxCS16		0°C to +70° C	16 lead SOIC (300 mils)

Integrated Circuit Systems, Inc.

Video Genlock PLL

Features

- Phase-detector/VCO circuit block
- Ideal for genlock system
- Reference clock range 15 kHz to 1 MHz
- Output clock range 1.25 to 50 MHz
- On chip loop filter
- Single 5 volt power supply
- Low power CMOS technology
- Small 8 pin DIP or SOIC package

General Description

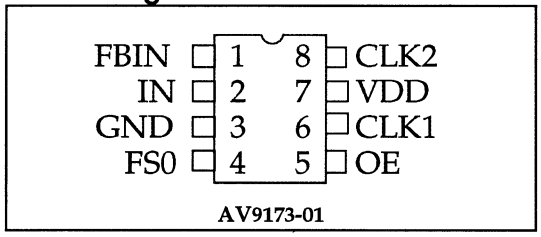
The AV9173 provides the analog circuit blocks required for implementing a video genlock dot (pixel) clock generator. It contains a phase detector, charge pump, loop filter, and voltage-controlled oscillator (VCO). By grouping these critical analog blocks into one IC and utilizing external digital functions, performance and design flexibility are optimized as are development time and system cost.

When used with an external clock divider, the AV9173 forms a Phase Locked Loop configured as a frequency synthesizer. The AV9173 is designed to accept video horizontal synchronization (h-sync) pulses and produce a video dot clock. A separated, negative-going sync input reference pulse is required at pin 2 (IN). The use of unstable video sources, such as a VCR output, is not recommended.

The AV9173 is also suited for other clock recovery applications in such areas as data communications.

D

Pin Configuration

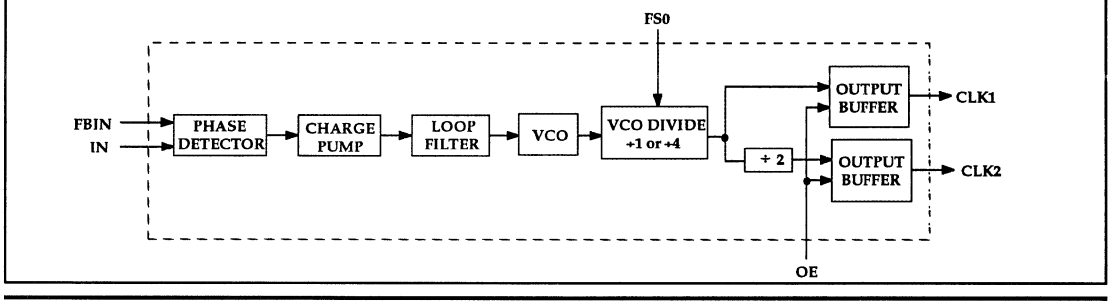


AV9173-01

Pin Description

Pin Name	Pin #	Type	Description
FBIN	1	Input	FEEDBACK INPUT
IN	2	Input	INPUT for reference sync pulse
GND	3	-	GROUND
FS0	4	Input	FREQUENCY SELECT 0 input
OE	5	Input	OUTPUT ENABLE
CLK1	6	Output	CLOCK output 1
VDD	7	-	Power supply (+5V)
CLK2	8	Output	CLOCK output 2

Block Diagram



Using the AV9173

Most video sources, such as video cameras, are asynchronous, free-running devices. To digitize video or synchronize one video source to another free-running reference video source, a video "genlock" (generator lock) circuit is required. The AV9173 integrates the analog blocks which make the task much easier.

In the complete video genlock circuit, the primary function of the AV9173 is to provide the analog circuitry required to generate the video dot clock within a PLL. This application is illustrated in Figure 1. The input reference signal for this circuit is the horizontal synchronization (h-sync) signal. If a composite video reference source is being used, the h-sync pulses must be separated from the composite signal. A video sync separator circuit, such as the National Semiconductor LM1881, can be used for this purpose.

The clock feedback divider shown in Figure 1 is a digital divider used within the PLL to multiply the reference frequency. Its divide ratio establishes how many video dot clock cycles occur per h-sync pulse. For example, if 880 pixel clocks are desired per h-sync pulse then the divider ratio is set to 880. Hence, together the h-sync frequency and external divider ratio establish the dot clock frequency:

$$f_{OUT} = f_{IN} \cdot N \qquad \text{where N is external divide ratio}$$

Both AV9173 input pins IN and FBIN respond only to negative-going clock edges of the input signal. The h-sync signal must be constant frequency and stable (low clock jitter) for creation of a stable output clock.

The output hook-up of the AV9173 is dictated by the desired dot clock frequency. The primary consideration is the internal VCO which operates over a frequency range of 10 MHz to 50 MHz. Because of the selectable VCO output divider and the additional divider on output CLK2, four distinct output frequency ranges can be achieved. The following table lists these ranges and the corresponding device configuration.

FS0 State	Output Used	Frequency Range
0	CLK1	10 - 50 MHz
0	CLK2	5 - 25 MHz
1	CLK1	2.5 - 12.5 MHz
1	CLK2	1.25 - 6.25 MHz

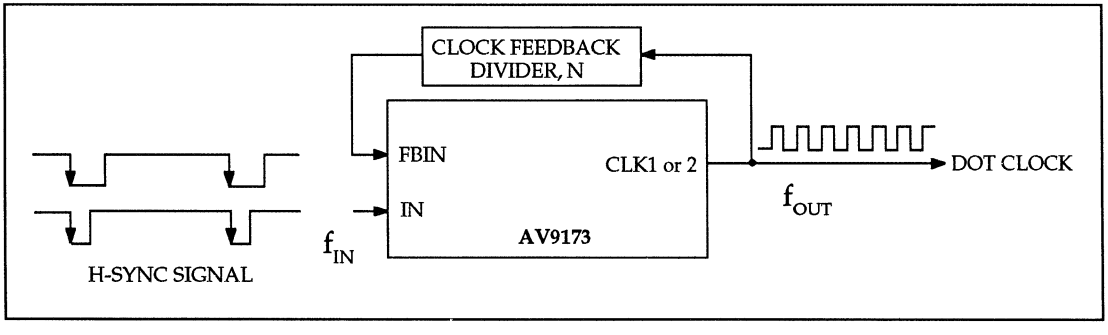
Note that both outputs, CLK1 and CLK2, are available during operation even though only one is fed back via the external clock divider.

Pin 5, OE, tri-states both CLK1 and CLK2 upon logic low input. This feature can be used to revert dot clock control to the system clock when not in genlock mode (hence, when in genlock mode the system dot clock must be tri-stated).

When unused, inputs FS0 and OE must be tied to either GND (logic low) or VDD (logic high).

For further discussion of VCO/PLL operation as it applies to the AV9173, please refer to the AV9170 application note. The AV9170 is a similar device with fixed feedback dividers for skew control applications.

Figure 1: Typical Application of AV9173 in a Video Genlock System



Absolute Maximum Ratings

VDD referenced to GND..... 7V
Operating temperature under bias..... 0°C to +70°C
Storage temperature..... -65°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation..... 0.5 Watts

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect the reliability of the device.

Electrical Characteristics

(V_{DD}= +5V± 5%, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage	-	-	0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0	-	-	V	V_{DD} = 5V
I_{IL}	Input Low Current	-5	-	-	µA	V_{IN} = 0V
I_{IH}	Input High Current	-5	-	5	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage	-	-	0.4	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	V_{DD}-.4V	-	-	V	I_{OH} = -1mA,V_{DD}=5.0V
V_{OH}	Output High Voltage	V_{DD}-.8V	-	-	V	I_{OH} = -4mA,V_{DD}=5.0V
V_{OH}	Output High Voltage	2.4	-	-	V	I_{OH} = -8mA
I_{DD}	Supply Current	-	20	50	mA	Unloaded, 50MHz
AC Characteristics						
$ICLK_r$	Input Clock Rise Time	-	-	10	ns	Note 1
$ICLK_f$	Input Clock Fall Time	-	-	10	ns	Note 1
t_r	Output Rise time, 0.8 to 2.0V	-	1	2	ns	15 pf load
t_r	Rise time, 20% to 80% V_{DD}	-	2	4	ns	15 pf load
t_f	Output Fall time, 2.0 to 0.8V	-	1	2	ns	15 pf load
t_f	Fall time, 80% to 20% V_{DD}	-	2	4	ns	15 pf load
d_t	Output Duty cycle	40	48/52	60	%	15 pf load. Note 2
T_{1s}	Cycle-to-cycle jitter, 1 sigma		120	300	ps	
T_{abs}	Cycle-to-cycle jitter, absolute	-500	±250	500	ps	
TL_{abs}	Line-to-line jitter, absolute		±4		ns	Note 3
f_{in}	Input Frequency, IN or FBIN	25		1000	kHz	Note 1
f_{VCO}	VCO clock speed	10		50	MHz	Note 1

NOTES:
1. It may be possible to operate the AV9173 outside of these ranges. Consult ICS for your specific application.
2. Duty cycle measured at 1.4V.
3. Input Reference Frequency = 15 kHz, Output Frequency = 25 MHz. Jitter measured between adjacent vertical pixels.

Ordering Information

Part Number	Part Marking	Temperature Range	Package Type
AV9173-01CC8	AV9173-01	0°C to +70°C	8 lead CERDIP
AV9173-01CN8	AV9173-01	0°C to +70°C	8 lead Plastic DIP (300 mils)
AV9173-01CS8	AV73-1	0°C to +70°C	8 lead SOIC (150 mils)

For the SOIC package, the AV9173-01 is marked AV73-1.

Integrated Circuit Systems, Inc.

ICS9175

Low Skew Output Buffer

Features

- Generates low skew clocks for Pentium™ microprocessor
- One 14.318 MHz crystal produces six output clocks
- 52 MHz, 60 MHz, and 66 MHz versions available
- ± 250 ps skew (max) between outputs
- 16 pin SOIC (300 mil) or 16 pin PDIP package
- Inputs and outputs are fully TTL compatible
- CMOS process results in low power supply current
- High drive, 25 mA outputs
- Low cost

General Description

The ICS9175 is designed to generate low skew clocks for clock distribution in high performance PCs and workstations. Using a 14.318 MHz crystal and phase-locked loop technology, six output clocks are produced at a master frequency or one half of the master frequency. The rising edges of the output clocks are guaranteed to be within 250 psec of one another.

There are three versions of the AV9175, each designed to support a different Pentium CPU frequency.

Part Number	CPU Frequency
ICS9175-04	66.6
ICS9175-05	60
ICS9175-06	52

The ICS9175 is ideal for generating multiple, high drive CPU clocks for Pentium applications. It meets the typical system specification for maximum skew between outputs (250 ps) and clock stability (± 250 ps).

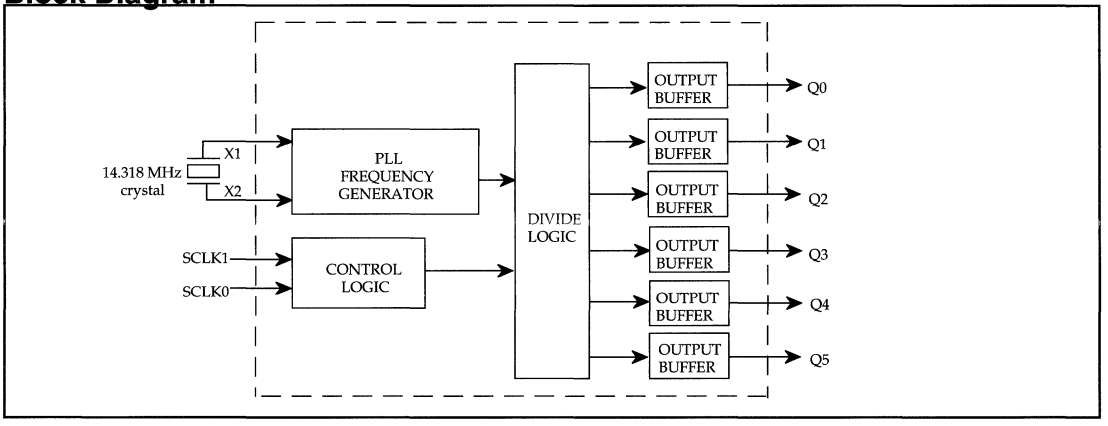
The use of a phase-locked loop allows the output clocks to run at multiples of the input crystal. The patented VCO design is capable of achieving internal frequencies of greater than 150 MHz operation. In the design of the ICS9175, the PLL is programmed to produce internal clocks at twice the desired frequency. The output is divided in half at the output to produce symmetric waveforms. Typical duty cycle is 50% ± 1%.

The ICS9175 is capable of producing half speed CPU clocks. Up to three of the six outputs can be configured as half speed CPU clocks. The skew matched circuitry matches rising edges of all CPU clocks and half speed clocks, guaranteeing low skew between outputs.

The ICS9175 is fabricated using CMOS technology which results in much lower power consumption and cost compared with similar devices based on Gallium arsenide or BiCMOS technology. The typical operating current for the ICS9175 is 50 mA.

The frequencies in the ICS9175 are mask programmable. Customer specific masks can be made and prototypes delivered within 6-8 weeks from receipt of order. ICS also offers standard versions such as those offered in this data sheet.

Block Diagram



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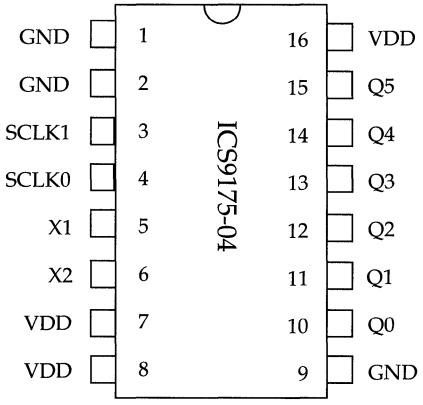
Pin Configuration



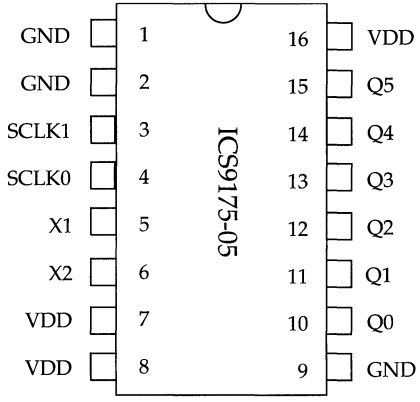
Configuration Table - ICS9175-04 (All units in MHz)

SCLK1	SCLK0	Q0	Q1	Q2	Q3	Q4	Q5
0	0	66	66	66	66	66	66
0	1	66	66	66	66	66	33
1	0	66	66	66	33	33	66
1	1	66	66	66	33	33	33

Pin Description for ICS9175-04

PIN NAME	PIN #	PIN TYPE	DESCRIPTION
GND	1	-	GROUND
GND	2	-	GROUND
SCLK1	3	Input	SCLK1 selects number of 1/2 speed clocks
SCLK0	4	Input	SCLK0 selects number of 1/2 speed clocks
X1	5	Input	X1 crystal output
X2	6	Input	X2 crystal output
VDD	7	-	Power supply (+5V)
VDD	8	-	Power supply (+5V)
GND	9	-	GROUND
Q0	10	Output	Q0 is a 66 MHz clock
Q1	11	Output	Q1 is a 66 MHz clock
Q2	12	Output	Q2 is a 66 MHz clock
Q3	13	Output	Q3 can be 66 MHz or 33 MHz clock
Q4	14	Output	Q4 can be 66 MHz or 33 MHz clock
Q5	15	Output	Q5 can be 66 MHz or 33 MHz clock
VDD	16	-	Power supply (+5V)

Pin Configuration



Configuration Table - ICS9175-05 (All units in MHz)

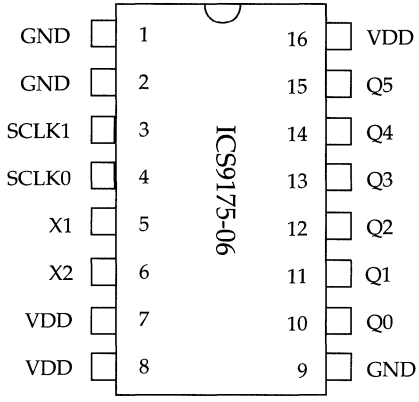
SCLK1	SCLK0	Q0	Q1	Q2	Q3	Q4	Q5
0	0	60	60	60	60	60	60
0	1	60	60	60	60	60	30
1	0	60	60	60	30	30	60
1	1	60	60	60	30	30	30

D

Pin Description for ICS9175-05

PIN NAME	PIN #	PIN TYPE	DESCRIPTION
GND	1	-	GROUND
GND	2	-	GROUND
SCLK1	3	Input	SCLK1 selects number of 1/2 speed clocks
SCLK0	4	Input	SCLK0 selects number of 1/2 speed clocks
X1	5	Input	X1 crystal output
X2	6	Input	X2 crystal output
VDD	7	-	Power supply (+5V)
VDD	8	-	Power supply (+5V)
GND	9	-	GROUND
Q0	10	Output	Q0 is a 60 MHz clock
Q1	11	Output	Q1 is a 60 MHz clock
Q2	12	Output	Q2 is a 60 MHz clock
Q3	13	Output	Q3 can be 60 MHz or 30 MHz clock
Q4	14	Output	Q4 can be 60 MHz or 30 MHz clock
Q5	15	Output	Q5 can be 60 MHz or 30 MHz clock
VDD	16	-	Power supply (+5V)

Pin Configuration



Configuration Table - ICS9175-06 (All units in MHz)

SCLK1	SCLK0	Q0	Q1	Q2	Q3	Q4	Q5
0	0	52	52	52	52	52	52
0	1	52	52	52	52	52	26
1	0	52	52	52	26	26	52
1	1	52	52	52	26	26	26

Pin Description for ICS9175-06

PIN NAME	PIN #	PIN TYPE	DESCRIPTION
GND	1	-	GROUND
GND	2	-	GROUND
SCLK1	3	Input	SCLK1 selects number of 1/2 speed clocks
SCLK0	4	Input	SCLK0 selects number of 1/2 speed clocks
X1	5	Input	X1 crystal output
X2	6	Input	X2 crystal output
VDD	7	-	Power supply (+5V)
VDD	8	-	Power supply (+5V)
GND	9	-	GROUND
Q0	10	Output	Q0 is a 52 MHz clock
Q1	11	Output	Q1 is a 52 MHz clock
Q2	12	Output	Q2 is a 52 MHz clock
Q3	13	Output	Q3 can be 52 MHz or 26 MHz clock
Q4	14	Output	Q4 can be 52 MHz or 26 MHz clock
Q5	15	Output	Q5 can be 52 MHz or 26 MHz clock
VDD	16	-	Power supply (+5V)

Absolute Maximum Ratings

VDD referenced to GND..... 7V
Operating temperature under bias..... 0°C to +70°C
Storage temperature..... -65°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation..... 0.5 Watts

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect the reliability of the device

Electrical Characteristics

(V_{DD}= +5V± 5%, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage	-	-	0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0	-	-	V	V_{DD} = 5V
I_{IL}	Input Low Current	-5	-	5	µA	V_{IN} = 0V
I_{IH}	Input High Current	-5	-	5	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage	-	0.5	0.8	V	I_{OL} = 25mA
V_{OH}	Output High Voltage	2.4	-	-	V	I_{OH} = -25mA
I_{DD}	Supply Current	-	35	60	mA	Unloaded, SCLK = 00
AC Characteristics						
t_r	Output Rise time, 0.8 to 2.0V	-	0.7	1	ns	15 pf load
t_r	Rise time, 20% to 80% V_{DD}	-	1.2	2	ns	15 pf load
t_f	Output Fall time, 2.0 to 0.8V	-	0.7	1	ns	15 pf load
t_f	Fall time, 80% to 20% V_{DD}	-	1.2	2	ns	15 pf load
d_t	Output Duty cycle	45	49/51	55	%	15 pf load
T_{1s}	Jitter, 1 sigma		60		ps	
T_{abs}	Jitter, absolute		± 200		ps	
f_i	Input Frequency		14.318		MHz	Note 1
f_o	Output Frequency			100	MHz	
t_{skew2}	Skew between any 2 outputs at same frequency	-250	± 50	250	ps	Note 2, 4
	Skew between any 2 outputs at different frequencies			500	ps	Note 2, 4

NOTES:
1. It may be possible to operate the ICS9175 outside of these ranges. Consult ICS for your specific application.
2. All skew specifications are measured with a 50Ω transmission line, load terminated with 50Ω to 1.4V.
3. Duty cycle measured at 1.4V.
4. Skew measured at 1.4V on rising edges. Loading must be equal on outputs.

Ordering Information

Part Number	Temperature Range	Package Type
ICS9175-xxCN16	0° C to +70° C	16 lead PDIP
ICS9175-xxCS16	0°C to +70° C	16 lead SOIC (300 mils)

Low Skew Output Buffer

Features

- **ICS9176-01 is pin compatible with Triquint GA1086**
- **±500 ps skew (max) between input and outputs**
- **±250 ps skew (max) between outputs**
- **10 symmetric, TTL-compatible outputs**
- **28 pin J-lead surface mount package**
- **High drive, 40 mA outputs**
- **Power down option**
- **Output frequency range 16 MHz to 130 MHz**
- **Input frequency range 6 MHz to 80 MHz**
- **Ideal for PCI bus applications**

General Description

The ICS9176 is designed specifically to support the tight timing requirements of high-performance microprocessors and chip sets. Because the jitter of the device is limited to ±250 psec, the ICS9176 is ideal for clocking Pentium™ systems. The 10 high drive (40 mA), low-skew (± 250 psec) outputs make the ICS9176 a perfect fit for PCI clocking requirements.

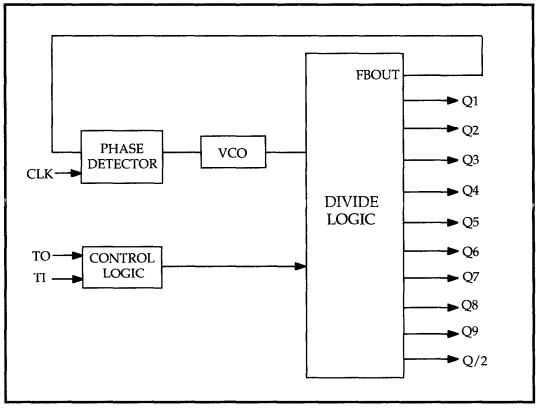
The ICS9176 has 10 outputs synchronized in phase and frequency to an input clock. The internal phase locked loop (PLL) acts either as a 1X clock multiplier or a 1/2X clock multiplier depending on the state of the input control pins T0 and T1. With metal mask options, any type of ratio between the input clock and output clock can be achieved, including 2X.

The PLL maintains the phase and frequency relationship between the input clock and the outputs by externally feeding back FBOUT to FBIN. Any change in the input will be tracked by all 10 outputs. However, the change at the outputs will happen smoothly so no glitches will be present on any driven input. The PLL circuitry matches rising edges of the input clock and the output clock. Since the input to FBIN skew is guaranteed to ±500 psec, the part acts as a "zero delay" buffer.

The ICS9176 has a total of eleven outputs. Of these, FBOUT is dedicated as the feedback into the PLL and another, Q/2, has an output frequency half that of the remaining nine. These nine outputs can either be running at the same speed as the input, or at half the frequency of the input. The maximum rise and fall time of an output is 14 ns and each is TTL-compatible with a 40 mA symmetric drive.

The ICS9176 is fabricated using CMOS technology which results in much lower power consumption and cost compared with the gallium arsenide based 1086E. The typical operating current for the ICS9176 is 60mA versus 115mA for the GA1086E.

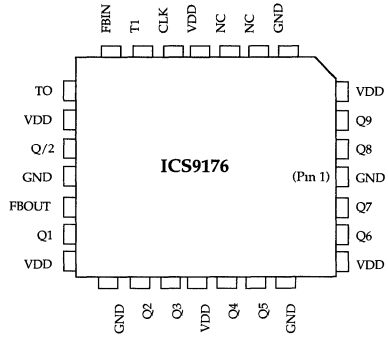
Block Diagram



Selection Table

T_1	T_0	Description
0	0	Power Down
0	1	Test Mode (PLL Off CLK = outputs)
1	0	Normal (PLL On)
1	1	Divide by 2 Mode

Pin Configuration



Pin Description

Pin Name	Pin #	Pin type	Description
GND	1	-	GROUND
Q8	2	Output	Output clock 8
Q9	3	Output	Output clock 9
VDD	4	-	Power supply (+5V)
GND	5	-	GROUND
NC	6	-	No connect
NC	7	-	No connect
VDD	8	-	Power supply (+5V)
CLK	9	Input	Input for reference clock
T1	10	Input	T1 selects normal operation, powerdown, or test mode
FBIN	11	Input	FEEDBACK INPUT from output FBOUT
T0	12	Input	T0 selects normal operation, powerdown, or test mode
VDD	13	-	Power Supply (+5V)
Q/2	14	Output	Half-clock output
GND	15	-	GROUND
FBOUT	16	Output	FEEDBACK OUTPUT to Input FBIN
Q1	17	Output	Output clock 1
VDD	18	-	Power Supply (+5V)
GND	19	-	GROUND
Q2	20	Output	Output clock 2
Q3	21	Output	Output clock 3
VDD	22	-	Power supply (±5V)
Q4	23	Output	Output clock 4
Q5	24	Output	Output clock 5
GND	25	-	GROUND
VDD	26	-	Power Supply (±5V)
Q6	27	Output	Output clock 6
Q7	28	Output	Output clock 7

Applications

FBOUT is normally connected to FBIN to facilitate input to output skew control. However, there is no requirement that the external feedback connection be a direct hardwire from an output pin to the FBIN pin. As long as the signal at FBIN is derived directly from the FBOUT pin and maintains its frequency, additional delays can be accommodated. The clock phase of the outputs (rising edge) will be adjusted so that the phase of FBIN and the input clock will be the same. See Figure 1 for an example.

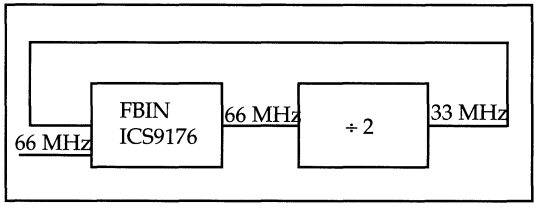


Figure 1

In Figure 1, the propagation delay through the divide by 2 circuit is eliminated. The internal phase-locked loop will adjust the output clock on the ICS9176 to ensure zero phase delay between the FBIN and CLK signals, as a result, the rising edge at the output of the divide by two circuit will be aligned with the rising edge of the 66 MHz input clock. This type of configuration can be used to eliminate propagation delay as long as the signal at FBIN is continuous and is not gated or conditional.

The ICS9176 is also ideal for clocking multi-processor systems. The 10 outputs can be used to synchronize the operation of CPU cache and memory banks operating at different speeds. Figure 2 depicts a 2-CPU system in which processors and associated peripherals are operating at 66 MHz. Each of the nine outputs operating at 66 MHz are fully utilized to drive the appropriate CPU, cache and memory control logic. The 33 MHz output is used to synchronize the operation of the slower memory bank to the restart of the system.

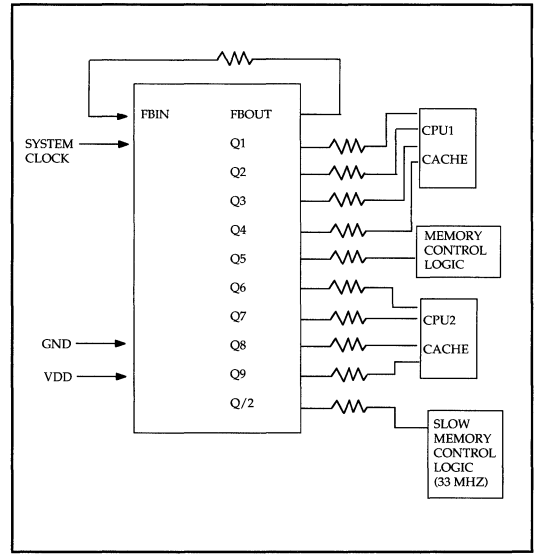
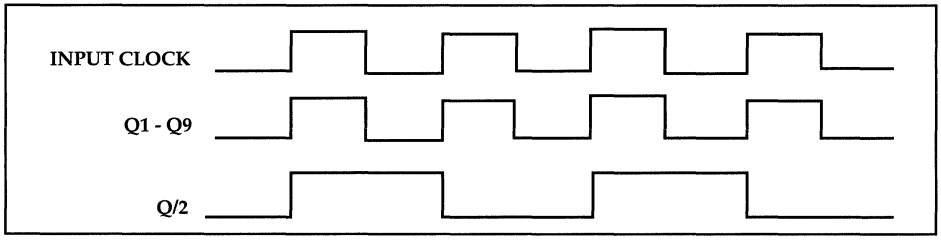


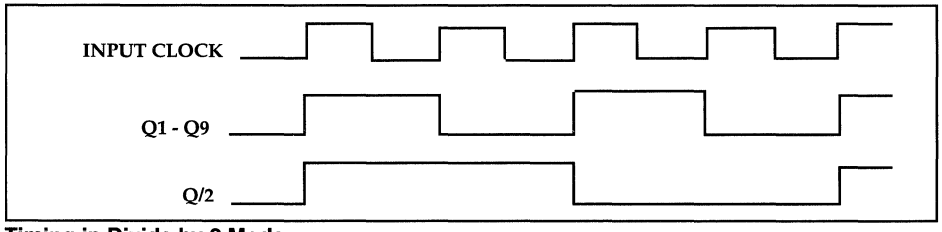
Figure 2

D

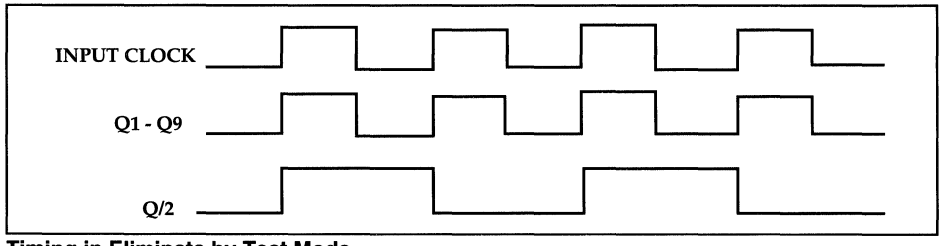
Timing Diagrams



Timing in Divide by 1 Mode

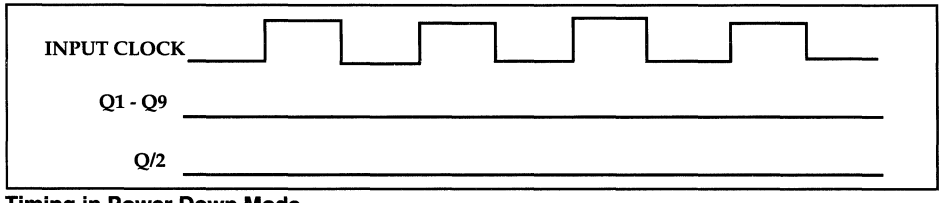


Timing in Divide by 2 Mode



Timing in Eliminate by Test Mode

Note: In test mode, the VCOs are bypassed. The test clock input is simply buffered, then output. The part is transparent. Damage to the device may occur if an output is shorted or forced to ground or VDD.



Timing in Power Down Mode

Absolute Maximum Rating

VDD referenced to GND..... 7V
Operating temperature under bias..... 0°C to +70°C
Storage temperature..... -65°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation..... 0.5 Watts

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect the reliability of the device.

Electrical Characteristics

(V_{DD}= +5V± 5%, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage	-	-	0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0	-	-	V	V_{DD} = 5V
I_{IL}	Input Low Current	-5	-	5	µA	V_{IN} = 0V
I_{IH}	Input High Current	-5	-	5	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage	-	0.5	0.8	V	I_{OL} = 25mA
V_{OH}	Output High Voltage	2.4	-	-	V	I_{OH} = -25mA
I_{DD}	Supply Current	-	55	110	mA	Unloaded, 66.66MHz
AC Characteristics						
$ICLK_r$	Input Clock Rise Time	-	-	10	ns	
$ICLK_f$	Input Clock Fall Time	-	-	10	ns	
t_r	Output Rise time, 0.8 to 2.0V	-	0.7	1	ns	15 pf load
t_r	Rise time, 20% to 80% V_{DD}	-	1.2	2	ns	15 pf load
t_f	Output Fall time, 2.0 to 0.8V	-	0.7	1	ns	15 pf load
t_f	Fall time, 80% to 20% V_{DD}	-	1.2	2	ns	15 pf load
d_t	Output Duty cycle	45	49/51	55	%	15 pf load
T_{1s}	Jitter, 1 sigma		60		ps	
T_{abs}	Jitter, absolute	-300	±200	300	ps	
f_i	Input Frequency	25		50	MHz	Note 1
f_o	Output Frequency	16		130	MHz	
t_{skew1}	FBIN to IN skew	-500	-300	500	ps	Note 2, 4. Input rise time <3ns
t_{skew2}	Skew between any 2 outputs at same frequency	-250	±50	250	ps	Note 2, 4
	Skew between any 2 outputs at different frequencies			500	ps	Note 2, 4

NOTES:
1. It may be possible to operate the ICS9176 outside of these ranges. Consult ICS for your specific application.
2. All skew specifications are measured with a 50Ω transmission line, load terminated with 50Ω to 1.4V.
3. Duty cycle measured at 1.4V.
4. Skew measured at 1.4V on rising edges. Loading must be equal on outputs.

Ordering Information

Part Number	Part Marking	Temperature Range	Package Type
AV9176-xx		0° C to +70° C	28 lead PLCC

ICS

Special Purpose IC Applications

Clocking Intel Pentium Based Systems

The Intel Pentium processor brings new levels of performance to PC based desktop systems. Unfortunately for the system designer, it also places higher demands on the system clocking. Jitter, high and low time, and skew are carefully specified. Oscillators may be expensive or difficult to obtain for the frequencies needed. Clock skew can be difficult to control.

ICS offers a number of solutions for the Pentium system designer, from our workhorse AV9155, proven in millions of 386 and 486 systems, to the AV9175, with its 6 skew controlled outputs. The AV9172 and AV9176 are pin and function compatible CMOS alternatives to GA1210 and GA1086 GaAs PLL clock drivers.

For low cost systems, where only the processor is clocked, the simplest solution is to use the AV9155-23, shown in Figure 1. This clock generator features fixed outputs of 1.84, 16, 24, 12, and two 14.318 MHz. The CPU output can be selected with the three address pins to one of eight frequencies, including 66.66, 60, and 52 MHz. A CPU/2 output is also provided, which is skew matched to typically 200 ps.

The AV9154-27 shown in Figure 2 offers the most commonly used system clocks of 1.84, 24, 12 and 14.318 MHz, as well as a single CPU output which can be set to one of eight frequencies. The 16 pin package uses very little board space.

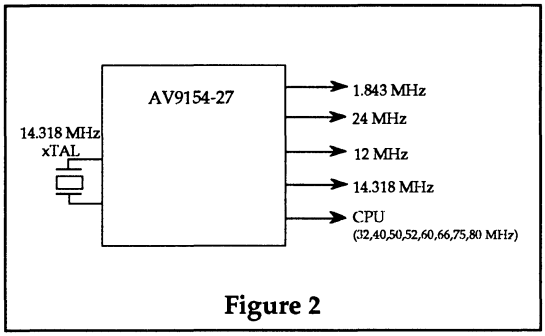


Figure 2

D

High performance systems have more demanding clock requirements. The processor, cache controller, local bus accelerators, and PCI-EISA bridge require low skew, low jitter clocks. The AV9172 is a phase-locked loop buffer with 6 outputs - four at the CPU frequency and two at 1/2 CPU frequency. Two of the CPU outputs can be configured as non-overlapping clocks. The AV9172 has guaranteed skew of 250 ps between outputs running at the same frequency (50 ps typical) and 500 ps between 1x and 1/2x outputs. A typical configuration is shown in Figure 3. The output frequency is exactly 1x or 2x the input frequency with ±500 ps skew between input and output.

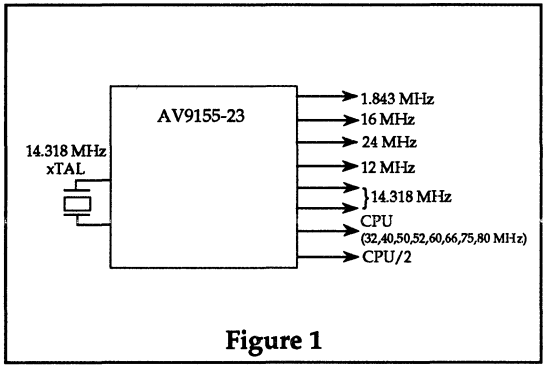


Figure 1

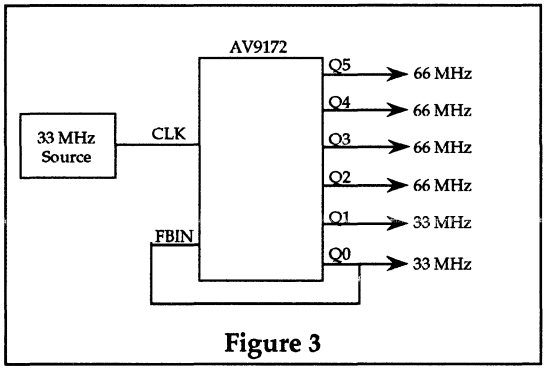


Figure 3

Pentium™ is a trademark of Intel Corporation

An ideal source for the 1/2x clock required by the AV9172 is the AV9155-23 mentioned earlier. This gives the system designer all the fixed clocks that he requires, as well as low jitter, skew matched copies of the CPU and 1/2 CPU clocks (Figure 4). The AV9172 is a direct replacement for the Gazelle GA1210, but fabricated in a high speed CMOS process rather than expensive gallium arsenide.

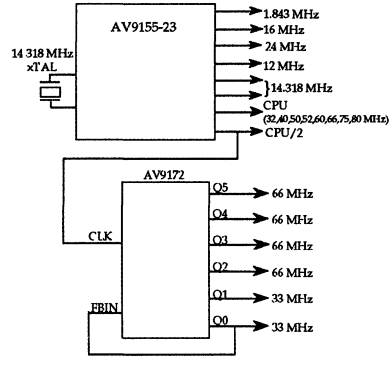


Figure 4

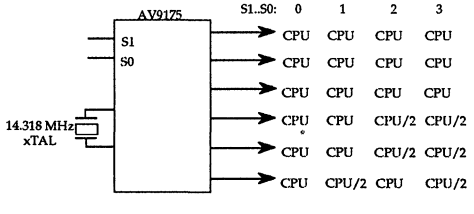


Figure 5

The AV9175 is a single frequency clock generator which synthesizes standard Pentium system frequencies from a low cost 14.318 MHz crystal. Using the select pins, the designer can allocate the six outputs to be either 1x or 1/2x outputs as shown in Figure 5. The AV9175 may also be driven directly from the 14.318 MHz output of the AV9155-23 as shown in Figure 6. This gives the system designer all required fixed clocks, six skew matched CPU clocks plus another CPU and 1/2 CPU output, which can be independently varied in frequency.

The AV9176 is a direct replacement for the Gazelle GA1086, which features ten skew matched outputs. Additional information will be forthcoming.

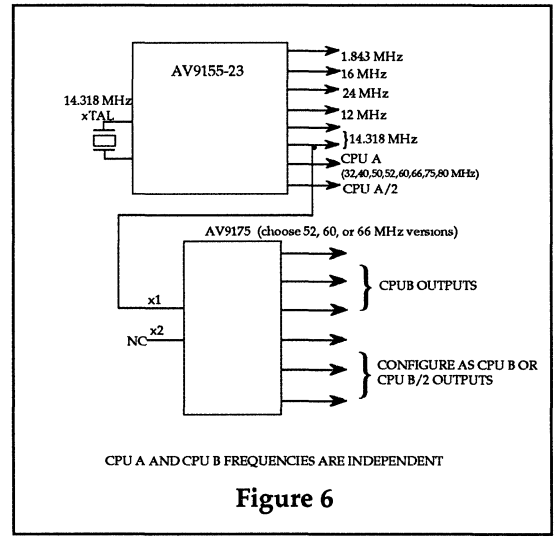


Figure 6

ICS

High-Performance

Products

ICS continues to set new standards for High-Performance Frequency Synthesis, and this latest product offering represents the highest frequency performance and widest choice of products in the industry. ICS puts its unique mixed signal CMOS technology to work, offering high frequency video and CPU timing solutions and features previously unavailable in the market. For example, the ICS1562 video graphics clock is being utilized successfully in customer CPU and video applications to over 400 MHz.

New products in this issue of the ICS data book include a 180 MHz version of the very popular ICS1562, (ICS1572), a 'line lock' clock for synchronizing with low frequency references (ICS1522), and a dual PLL clock with both video and memory outputs. These new products also offer the advantages available across the ICS High Performance line - features such as user programmability, extremely low jitter, and multiple outputs.

ICS High-Performance Products are designed with and for you, our customers. Our customer dialog is continuous, and we welcome the opportunity to discuss how we can put our High-Performance to work for you.

ICS High-Performance Product Selection Guide

Product Applications	ICS Device Type	Features	Package Types	Page
Workstation Clock Generators	ICS1522	User-Programmable Frequencies, 'Line Lock' Capability	24 Pin SOIC	541
	ICS1561	÷ 2, 4, 8 TTL Out. Integral Loop Filter. NOT RECOMMENDED FOR NEW DESIGN	20 Pin DIP, SOIC	549
	ICS1561A	÷ 2, 4, 8 TTL Out. Integral Loop Filter. Replaces ICS1561.	20 Pin DIP, SOIC	551
	ICS1562	User-Programmable Frequencies. RAMDAC™ Reset Logic (Brooktree compatible).	16 Pin Narrow SOIC	557
	ICS1567	32 Frequency ROM-based RAMDAC Reset Logic (Brooktree compatible).	20 Pin DIP, SOIC	575
	ICS1572	User-Programmable Frequencies. RAMDAC Reset Logic (Brooktree compatible).	20 Pin SOIC	585
	ICS2572	User-Programmable Dual PLL. 16V+ 4M Locations.	20 Pin DIP, SOIC	603

Notes:
1. All products have internal loop filters except as noted.
2. All products operate at 5V typ. except as noted.

ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. ICS reserves the right to change or discontinue these products without notice.

User-Programmable Video Clock Generator/ Line-Locked Clock Regenerator

Description

The **ICS1522** is a very high performance monolithic phase-locked loop (PLL) frequency synthesizer. Utilizing ICS' advanced CMOS mixed-mode technology, the **ICS1522** provides a low-cost solution for high-end video clock generation where synchronization to an external video source is required.

The **ICS1522** has differential video clock outputs (**CLK+** and **CLK-**) that are compatible with industry standard video DAC.

Operating frequencies are fully programmable with direct control provided for reference divider, pre-scaler, feedback divider and post-scaler.

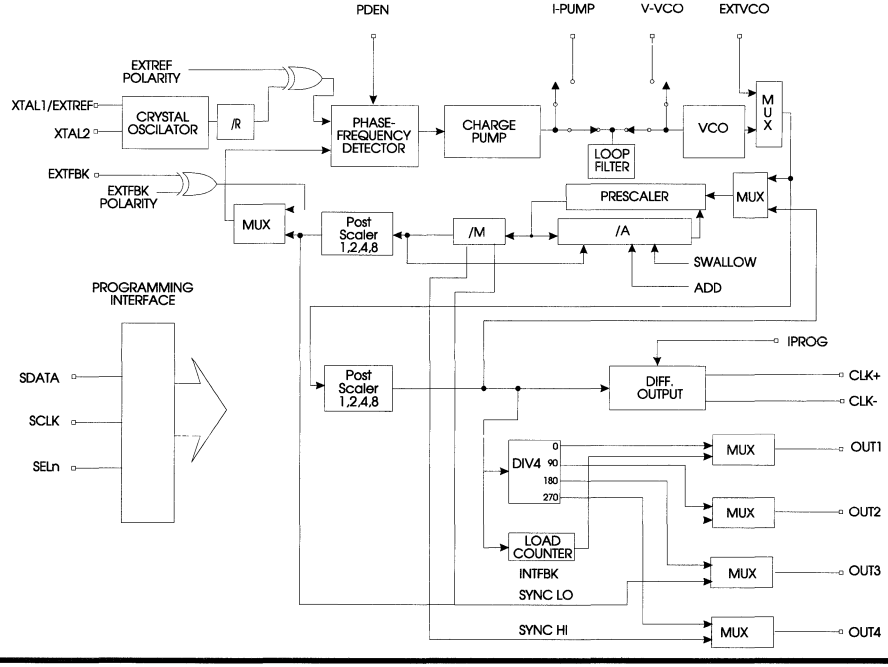
Features

- Serial programming: Input and reference divisors, VCO gain, phase comparator gain, delay, and test modes
- Supports high-resolution graphics - Differential CLK outputs to 230 MHz
- Eliminates need for multiple ECL output voltage controlled crystal oscillators and external components
- Fully-programmable synthesizer capability - not just a clock multiplier
- Line-locked clock generation capability; 15 - 100 kHz
- External feedback loop capability allows graphics system to be used as the feedback divisor
- Small footprint 24-pin SOIC
- Phase adjustment permits precise clocking in video recovery application

Applications

- LCD Projector Systems
- Multimedia video line locking
- Genlock applications

Block Diagram



E

Overview

The **ICS1522** is ideally suited to provide the graphics system clock signals required by high-performance video DACs. Fully programmable feedback and reference divider capability allow virtually any frequency to be generated, not just simple multiples of the reference frequency. The **ICS1522** uses the latest generation of frequency synthesis techniques developed by ICS and is completely suitable for the most demanding video applications.

PLL Synthesizer Description - Ratiometric Mode

The **ICS1522** generates its output frequencies using phase-locked loop techniques. The phase-locked loop (or PLL) is a closed-loop feedback system that drives the output frequency to be ratiometrically related to the reference frequency provided to the PLL (see Figure 1). The reference frequency is generated by an on-chip crystal oscillator or the reference frequency may be applied to the **ICS1522** from an external frequency source, typically horizontal sync from another display system.

The phase-frequency detector shown in the block diagram drives the voltage-controlled oscillator, or VCO, to a frequency that will cause the two inputs to the phase-frequency detector to be matched in frequency and phase. This occurs when:

$$F(VCO) := \frac{F(XTAL1) \cdot \text{Feedback Divider}}{\text{Reference Divider}}$$

This expression is exact; that is, the accuracy of the output frequency depends solely on the reference frequency provided to the part (assuming correctly programmed dividers).

The VCO gain is programmable, which permits the **ICS1522** to be optimized for best performance at all operating frequencies.

The feedback divider may be programmed for any modulus from 1 to 2048 in steps of one followed by a divide by 1, 2, 4 or 8 feedback post-scaler.

The reference divider may be programmed for any modulus from 1 to 1024 in steps of one.

Function	Address 101 Data Bits 6, 7
Feedback ÷ 1	11
Feedback ÷ 2	01
Feedback ÷ 4	10
Feedback ÷ 8	00

Output Post-Scaler

A programmable post-scaler may be inserted between the VCO and the CLK+ and CLK- outputs of the **ICS1522**. This is useful in generating of lower frequencies, as the VCO has been optimized for high-frequency operation.

The post-scaler allows the selection of:

Function	Address 101 Data Bits 4, 5
VCO frequency	11
VCO frequency ÷ 2	01
VCO frequency ÷ 4	10
VCO frequency ÷ 8	00

Load Clock Divider

The **ICS1522** has an additional programmable divider (referred to in Figure 1 as the load counter) that is used to generate the LOAD clock frequency for the video DAC. The modulus of this divider may be set to 3, 4, 5, 6, 8, or 10 under register control. The design of this divider permits the output duty factor to be 50/50, even when odd modulus is selected. The input frequency to this divider is the output of the output post-scaler described above.

Address 110		Data Bits 0, 1, 2	
L(2)	L(1)	L(0)	Divide Ratio
0	0	0	3
0	0	1	4
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	8
1	1	0	8
1	1	1	10

Digital Inputs - ICS1522

The programming of the **ICS1522** is performed serially by using the **SDATA**, **SCLK**, and **SELn** pins to load the 7, 11 bit internal memory locations.

Single bit changes are accomplished by addressing the appropriate memory location and writing only 11 bits of data, not by writing all 77 data bits.

For proper programming of the **ICS1522**, it is important that all transitions of the **SELn** input occur during the same state of the **SCLK** input.

SDATA is shifted into a 15 bit serial register on the rising edge of **SCLK** while **SELn** is low. The first bit loaded is R/Wn followed by a 3 bit address and 11 bit data (both address & data are LSB first). When a rising edge of **SCLK** occurs while **SELn** is high (**SDATA** ignored), the contents of the serial register are loaded into the addressed 11 bit memory location if R/Wn is low. If R/Wn is high upon the above condition, the data from the addressed memory location is loaded into the serial shift register and **SDATA** is set as an output. The R/Wn bit, 3 bit address, and 11 bit data will be serially shifted out of the **ICS1522** on the **SDATA** pin on the rising edge of **SCLK** while **SELn** is low.

An additional control pin on the **ICS1522**, **PDEN** can be used to disable the phase-frequency detector in line-locked applications. When disabled, the phase detector will ignore any inputs and allow the VCO to coast. This feature is useful in systems using composite sync.

Output Description

The differential output drivers, **CLK+** and **CLK-**, are current-mode and are designed to drive resistive terminations in a complementary fashion. The outputs are current-sinking only, with the amount of sink current programmable via the **IPRG** pin. The sink current, which is steered to either **CLK+** or **CLK-**, is four times the current supplied to the **IPRG** pin. For most applications, a resistor from VDDO to IPRG will set the current to the necessary precision.

Reference Oscillator and Crystal Selection

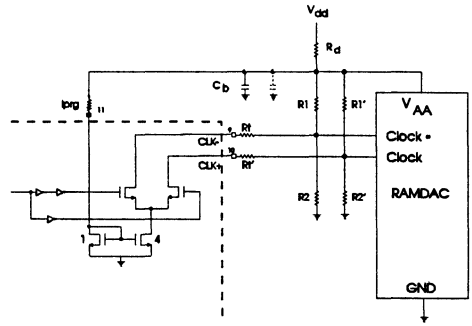
The **ICS1522** has circuitry on-board to implement a Pierce oscillator with the addition of a quartz crystal and two external loading capacitors. Pierce oscillators operate the crystal in anti- (also called parallel-) resonant mode.

Series-resonant crystals may also be used with the **ICS1522**. Be aware that the oscillation frequency will be slightly higher than the frequency that is stamped on the can (typically 0.025-0.05%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the **ICS1522** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

If an external reference frequency source is to be used with the **ICS1522**, it is important that it be jitter-free. The rising and falling edges of that signal should be fast and free of noise for best results.

The loop phase is locked to the rising edges of the XTAL1/EXTREF input signal, if REF_POL is set to logic 0.



Typical Output Circuitry Configuration

Line-Locked Operation

Some video applications require a clock to be generated that is a multiple of horizontal sync. The **ICS1522** supports this mode of operation. The reference divider should be set to divide by one and the desired polarity (rising or falling) of lock edge should be selected. By using the phase detector hardware disable mode (PDEN), the PLL can be made to free-rum at the beginning of the vertical interval of the external video, and can be reactivated at its completion.

External Feedback Operation

The **ICS1522** option also supports the inclusion of an external counter as the feedback divider of the PLL. This mode is useful in graphic systems that must be "genlocked" to external video sources.

When the FBK_SEL bit is set to logic 0, the phase-frequency detector will use the **EXTFBK** pin as its feedback input. The loop phase will be locked to the rising edges of the signal applied to the EXTFBK input if FBK_POL is set to logic 0.

Power-On Initialization

The **ICS1522** has an internal power-on reset circuit that sets the multiplexer to pass the reference frequency to the **CLK+** and **CLK-** outputs.

These functions should allow initialization of most graphics systems that cannot immediately provide for register programming upon system power-up.

Because the power-on reset circuit is on the VDD supply, and because that supply is filtered, care must be taken to allow the reset to de-assert before programming. A safe guideline is to allow 20 microseconds after the VDD supply reaches four volts.

Board Test Support

It is often desirable to statically control the levels of the output pins for circuit board test. The **ICS1522** supports this through a register programmable mode, AUXEN. When this mode is set, AUXCLK will directly control the logic levels of the CLK+ and CLK- pins while OMUX1, OMUX2, OMUX3, and OMUX4 will control OUT1, OUT2, OUT3 and OUT4, respectively.

Power Supplies and Decoupling

The **ICS1522** has two **VSS** pins to reduce the effects of package inductance. Both pins are connected to the same potential on the die (the ground bus). BOTH of these pins should connect to the ground plane of the video board as close to the package as is possible.

The **ICS1522** has a **VDDO** pin which is the supply of + 5 volt power to all output drivers. This pin should be connected to the power plane (or bus) using standard high-frequency decoupling practice. That is, capacitors should have low series inductance and be mounted close to the **ICS1522.**

The **VDD** pin is the power supply pin for the PLL synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin (as shown in the recommended application circuitry). This will allow the PLL to "track" through power supply fluctuations without visible effects.

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	IPUMP	OUT	Charge Pump Output (External loop filter applications
2	SDATA	IN/OUT	Serial Data Input/Output
3	SCLK	IN	Serial Clock Input
4	SELn	IN	Serial Port Enable
5	AVDD	PWR	Analog + 5 Volt Supply
6	XTAL1/EXTREF	IN	External Reference Input / Xtal Oscillator Input
7	XTAL2	OUT	Xtal Oscillator Output
8	Reserved	NC	Reserved for future application
9	VSS	PWR	Ground
10	VSS	PWR	Ground
11	OUT4	OUT	Output 4
12	OUT3	OUT	Output 3
13	VDD	PWR	Digital + 5 Volt Supply
14	OUT2	OUT	Output 2
15	OUT1	OUT	Output 1
16	VSS	PWR	Ground
17	IPRG	IN	Output Driver Current Programming Input
18	CLK-	OUT	Differential CLK- Output
19	CLK+	OUT	Differential CLK+ Output
20	VDDO	PWR	Output Driver + 5 Volt Supply
21	PDEN	IN	Phase Detector Enable
22	EXTFBK	IN	External Feedback Input
23	EXTVCO	IN	External VCO Input
24	VVCO	IN	VCO Control Voltage Input (External loop filter applications)

Absolute Maximum Ratings

V_{DD}, V_{DDO} (measured to V_{SS}) 7.0V
Digital Inputs ..... V_{SS} -0.5 to V_{DD} to 0.5V
Digital Outputs ..... V_{SS} -0.5 to V_{DDO} to + 0.5V
Ambient operating temp ..... -55 to 125 °C
Storage temperature ..... -65 to 150 °C
Junction temperature ..... 175° C
Soldering temperature ..... 260° C

Recommended Operating Conditions

V_{DD}, V_{DDO} (measured to V_{SS}) ..... 4.75 to 5.25V
Operating Temperature (Ambient) ..... 0 to 70° C

DC Characteristics

TTL-Compatible Inputs

(PDEN, EXTFBK, SDATA, SCLK, SELn)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	V_{ih}		2.0	V_{DD} + 0.5	V
Input Low Voltage	V_{il}		V_{SS} - 0.5	0.8	V
Input Hysteresis			.20	.60	V
Input High Current	I_{ih}	V_{ih} = V_{DD}	-	10	uA
Input Low Current	I_{il}	V_{il} = 0.0	-	200	uA
Input Capacitance	C_{in}		-	8	pF

XTAL1/EXTREF Input and EXTVCO

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	Vxh		3.75	V_{DD} + 0.5	V
Input Low Voltage	Vxl		V_{SS} - 0.5	1.25	

CLK+ , CLK- Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Differential Output Voltage			0.6	-	V

OUT1, OUT2, OUT3, OUT4 Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output High Voltage (Ioh= 4.0mA)			2.4	-	V
Output Low Voltage (Iol= 8.0mA)			-	0.4	V

AC Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
F_{vco}	VCO Frequency	14		230	MHz
F_{xtal}	Crystal Frequency	5		20	MHz
Cpar	Crystal Oscillator Loading Capacitance		20		pF
F_{HSYNC}	Horizontal Sync Rate	15		100	kHz
T_{xhi}	XTAL1 High Time (when driven externally)	8			ns
T_{xlo}	XTAL1 Low Time (when driven externally)	8			ns
T_{JIT}	Phase Jitter (see Note 1)			1	ns
T_{lock}	PLL Acquire Time (to within 1%)			500	µs
I_{dd}	V_{DD} Supply Current		15		mA
I_{ddo}	VDDO Supply Current (excluding CLK+ /– termination)		20		mA
	ANALOG INPUTS				
T_{FPH}	Fine Phase Adjustment Range	0		10	ns
V_{FPH}	Control Voltage for FPHADJ	0		5	VDC
	FPHADJ Input Bias Current			20	nA
	Capacitance of FPHADJ Input			100	pF
	Bandwidth of FPHADJ Input (3dB)	0.5		1.5	kHz
	DIGITAL INPUT				
	SELn, SDATA Setup Time	10			ns
	SELn, SDATA Hold Time	10			ns
	SCLK Pulse Width (T_{hi} or T_{lo})	20			ns
	SCLK Frequency			20	MHz
	Phase-frequency detector enable time			50	ns
	Phase-frequency detector disable time			50	ns
	DIGITAL OUTPUTS				
T_{SKEW}	Time Skew between CLK+ , CLK–			500	pS
F_{CLK}	CLK+ and CLK– Clock Rate			230	MHz
	GAINS				
VCO	VCO Gain, VCO(0:2)	15		100	MHz/V
PFD	Phase Detector Gain, PFD (0:2)	.05		12	µA/rad

Note 1: T_{JIT} is the total uncertainty of the phase measured at the start of a video line on a 350 MHz oscilloscope under these conditions: HSYNC pin driven with crystal oscillator at 48.363 kHz; F_{VCO} = 65.000 MHz; M = 0 (divide by 1 on the output; and N = 1343 (1344 clocks per line).

Note 2: TDRIFT is the difference between the average phase at the start of the line and the average phase at the end of the line as measured under the same conditions as in Note 1.

Memory Definition

ICS1522 memory is loaded serially with the least significant bit clocked into the device first. After the R/Wn bit, the next three bits of the programming word (15 bits) hold the memory location to be loaded. The least significant 11 bits are the data to be loaded.

Memory Address	Data Bits	Default Values (Hex)	Name	Description
000	0-10	04F	F(0:10)	Feedback Divider Modulus (Modulus = Value + 1)
001	0-7	03	LO(0:7)	M Counter Lo Sync State
001	8-10	0		Don't Care
010	0-7	06	HI(0:7)	M Counter Hi Sync State
010	8-10	0		Don't Care
011	0-9	013	R(0:9)	Reference Divider Modulus (Modulus = Value + 1)
011	10	0	REF_POL	External Reference Polarity (1 = Invert)
100	0-2	4	VCO(0:2)	VCO Gain (See Table)
100	3-5	3	PFD(0:2)	Phase Detector Gain (See Table)
100	6	1	PDEN	Phase Detector Enable (1 = Enable)
100	7	1	INT_FLT	Internal Loop Filter (1 = Internal)
100	8	1	INT_VCO	Internal VCO (1 = Internal)
100	9	0	CLK_SEL	Internal feedback input clock select (0 = VCO Output)
100	10	0	Reserved	Reserved - Set to Zero
101	0	1	FBK_SEL	Feedback Select (1 = Internal)
101	1	0	FBK_POL	External Feedback Polarity (1 = Invert)
101	2	0	ADD	Addition of 1 VCO Cycle (0 to 1 = Add)
101	3	0	SWLW	Removal of 1 VCO Cycle (0 to 1 = Swallow)
101	4-5	0	PDA(0:1)	Output Post-Scaler
101	6-7	3	PDB(0:1)	Feedback Post-Scaler
101	8-10	0		Don't Care
110	0-2	7	L(0:2)	Load Counter
110	3	0	OMUX1	OUT1 Select (0 = Load Cntr, 1 = Div By 4 0Deg)
110	4	0	OMUX2	OUT2 Select (0 = Int Fbk, 1 = Div By 4 90Deg)
110	5	0	OMUX3	OUT3 Select (0 = Sync Lo, 1 = Div By 4 180Deg)
110	6	1	OMUX4	OUT4 Select (0 = Sync Hi, 1 = Div By 4 270Deg)
110	7	0	DACRST	Output Reset (CLK+ = 1, CLK- = 0)
110	8	0	AUXEN	Output Test Mode (1 = Test, See Board Test Support)
110	9	0	AUXCLK	Output Clock When in Test Mode
110	10	0		Don't Care

Pixel-by-Pixel Adjustment of Genlocking Phase

To understand the operation of the pixel-by-pixel phase adjustment feature, imagine that the modulus of the on-chip divider (that is, N1 X N2) is equivalent to the graphics system overall divide. Also, imagine that the overflow of the internal N2 divider occurs at the same time as the overflow of the graphics system line counter. We would be able to switch carefully between both dividers with no effect on the loop. Let us assume that we are now using the internal divider.

Now, imagine that the programmed value of the N1 divider (really a pre-scaler) is increased by one for a single pass-through that pre-scaler (think of this as "swallowing" a feedback pulse). We will lose exactly one CLK period of phase in the feedback path. The VCO will speed up momentarily to compensate for that, and re-lock the loop.

In doing so, the graphics system will receive exactly one extra CLK cycle, advancing the phase of the graphics system HSYNC by one CLK period relative to the reference HSYNC. In a similar fashion, we can decrease the programmed value of the prescaler ("adding" a pulse) to retard the phase of the graphics system.

Initial synchronization can be performed (to within + /- CLK) by a scheme where the internal counters are held in reset until an HSYNC pulse is returned from the graphics system.

Ordering Information

All ICS devices in SOIC packages carry an "M" designation.

Example: ICS1522M

Integrated Circuit Systems, Inc.

ICS1561

Differential Output Video Dot Clock Generator

Features

- High frequency operation for extended video modes - up to 180 MHz
- Compatible with Brooktree high performance RAM-DACs™
- Low Cost - Eliminates need for multiple ECL crystal clock oscillators in video display subsystems
- Strobed /Transparent frequency select options
- Mask-programmable frequencies
- Fast acquisition of selected frequencies, strobed or non-strobed
- Advanced PLL for low phase-jitter
- Dynamic control of VCO sensitivity providing optimized loop gain over entire frequency range
- Small footprint - 20 pin DIP or SO

Applications

- Workstations
- High resolution MACII displays
- EGA - VGA - Super VGA video adapters
- 8514A - TMS 34010 - TMS 34020

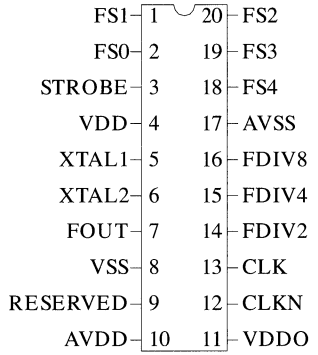
NOT RECOMMENDED FOR NEW DESIGN

E

Description

The **ICS1561** Dot Clock Generator is an integrated circuit capable of generating up to 32 video dot clock frequencies for use with high performance video display systems. Utilizing CMOS technology to implement all linear, digital and memory functions, the **ICS1561** provides a low power, small footprint, low cost solution to the generation of video dot clocks. Output frequencies are compatible with **VGA, EGA, MCGA, CGA, MDA** as well as the higher frequencies needed for advanced applications in desktop publishing and workstation graphics. Provision is made via a single level custom mask to implement customer specific frequency sets. Phase-locked loop circuitry permits rapid glitch-free transitions between clock frequencies. The **ICS1561** provides positive ECL outputs compatible with RAMDAC™ clock and clock* inputs. TTL compatible clocks at 1, 1/2, 1/4, and 1/8 the primary clock frequency facilitate the interfacing of video DRAM to the system.

Pin Configuration



Top View

Ordering Information

ICS1561NXXX (DIP Package)
ICS1561MXXX (SO Package)
(XXX = Pattern number)

Differential Output Video Dot Clock Generator

Description

The **ICS1561A** is a very high performance monolithic PLL frequency synthesizer. Utilizing ICS' advanced CMOS mixed mode technology, the **ICS1561A** provides a low cost solution for high-end video clock generation.

The **ICS1561A** has differential video clock outputs (CLK and CLK*) that are compatible with industry standard video DACs & RAMDACs™. Additional clock outputs, FDIV2, FDIV4 and FDIV8, provide frequencies which are 1/2, 1/4 and 1/8 the main clock frequency.

Operating frequencies are selectable from a preprogrammed (customer defined) table. An on-chip crystal oscillator for generating the reference frequency is provided on the **ICS1561A**.

Features

- High Frequency operation for extended video modes - up to 230 MHz
- Compatible with Brooktree high performance RAMDACs
- Low Cost - Eliminates need for multiple ECL crystal clock oscillators in video display subsystems
- Advanced PLL for low phase-jitter
- Dynamic control of VCO sensitivity provides optimized loop gain over entire frequency range
- Strobed/Transparent frequency select options
- Small footprint - 20 pin DIP or SO packages available
- Fully backward compatible to ICS1561

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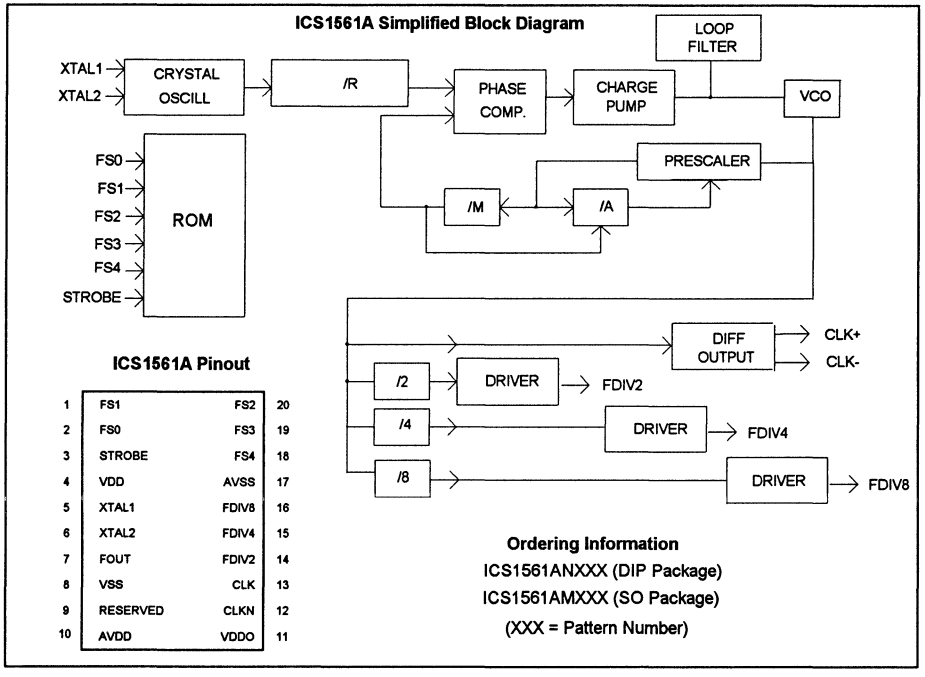
Block Diagram



RAMDAC is a trademark of Brooktree Corporation

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	FS1		Frequency select input, TTL compatible
2	FS0		Frequency select input, TTL compatible (LSB)
3	STROBE		Negative edge clock for select inputs, TTL compatible
4	VDD		5V power pin
5	XTAL1		Crystal interface/Ext. oscillator input
6	XTAL2		Crystal interface
7	FOUT		Clock output, TTL compatible
8	VSS		Digital ground
9	Phase out		Phase comparator output
10	AVDD		Analog VDD input
11	VDDO		Output stage VDD supply pin
12	CLOCKN		Complementary clock output, positive ECL
13	CLOCK		Clock output, positive ECL
14	FDIV2		Clock/2 output, TTL compatible
15	FDIV4		Clock/4 output, TTL compatible
16	FDIV8		Clock/8 output, TTL compatible
17	AVSS		Analog ground
18	FS4		Frequency select input, TTL compatible
19	FS3		Frequency select input, TTL compatible
20	FS2		Frequency select input, TTL compatible

Absolute Maximum Ratings

Supply voltage	V_{DD}	-0.5V to + 7V
Ambient operating temp	T_O	0°C to 70°C
Storage temperature	T_S	-85°C to + 150°C
Input Voltage	V_{IN}	-0.5V to VDD+ 0.5V
Output Voltage	V_{OUT}	-0.5V to VDD+ 0.5V
Clamp Diode Current	V_{IK} & I_{OK}	± 30mA
Output Current per Pin	I_{OUT}	± 50mA
Power Dissipation	P_D	500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation, it is recommended that Vin and Vout be constrained to > = V_{SS} and < = V_{DD}.

DC Characteristics

(Power Supply Voltage 4.75-5.25 Volts)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	V_{DD}= 5V	V_{SS}		0.8	V
Input High Voltage	V_{IH}	V_{DD}= 5V	2.0		V_{DD}	V
Input Leakage Current	I_{IH}	V_{IN}= VDD	-		10	µA
Output Low Voltage	V_{OL}	I_{OL}= 8.0mA	-		0.4	V
Output High Voltage	V_{OH}	I_{OH}= 4.0mA	2.4		-	V
Supply Current	I_{DD}	V_{DD}= 5V	-		30	mA
Internal Pull-up Current	R_{UP}	V_{DD}= 5V	25		100	µA
Input Pin Capacitance	C_{IN}	F_C= 1MHz	-		8	pF
Output Pin Capacitance	C_{OUT}	F_C= 1MHz	-		12	pF

E

Circuit Description

Overview

The **ICS1561A** is designed to provide the graphics system clock signals required by industry standard RAMDACs. One of 32 pre-programmed (user definable) frequencies may be selected under digital control. Fully programmable feedback and reference divider capability allow virtually any frequency to be generated, not just simple multiples of the reference frequency. The **ICS1561A** uses the latest generation of frequency synthesis techniques developed by ICS and is completely suitable for the most demanding video applications.

Digital Inputs

The FS0-FS4 pins and the STROBE pin are used to select the desired operating frequency from the 32 pre-programmed frequencies in the ROM table of the **ICS1561A**. The FS0-FS4 and STROBE pins are each equipped with a pull-up and will be at a logic HIGH level when not connected.

Transparent Mode - When the STROBE pin is held HIGH, the FS0 through FS4 inputs are transparent; that is, they directly access the ROM table. The synthesizer will output the frequency programmed into the location addressed by the FS0-FS4 pins.

Latched Mode - When the STROBE pin is held LOW, the FS0-FS4 pins are ignored. The synthesizer will output the frequency corresponding to the state of the FS0-FS4 pins when the STROBE pin was last HIGH. In the event that the **ICS1561A** is powered up with the STROBE pin held LOW, the synthesizer will output the frequency programmed into address 0 (i.e., the one selected with FS0 through FS4 at a logic LOW level).

Divided Dot clock Outputs

The **ICS1561A** has additional outputs which provide a /2, /4 and /8 of the main frequency.

Output Stage Description

The CLK and CLK* outputs are each connected to the drains of P-Channel MOSFET devices. The source of each of these devices is connected to VDDO. Typical on resistance of each device is 15 Ohms. These outputs will drive the clock and clock* of a RAMDAC device when a resistive network is utilized.

The divided outputs are high current CMOS type drives.

Frequency Synthesizer Description

The reference frequency is generated by an on-chip crystal oscillator, or the reference frequency may be applied to the **ICS1561A** from an external frequency source.

The **ICS1561A** generates its output frequencies using phase-locked loop techniques. The phase-locked loop (or PLL) is a closed loop feedback system that drives the output frequency to be ratiometrically related to the reference frequency provided to the PLL. The phase-frequency detector shown in the block diagram drives the VCO to a frequency that will cause the two inputs to the phase frequency detector to be matched in frequency and phase. This occurs when:

$$F_{(VCO)} = \frac{F(XTAL1) * \text{Feedback Divider}}{\text{Reference Divider}}$$

This expression is exact; that is, the accuracy of the output frequency depends solely on the reference frequency provided to the part (assuming correctly programmed dividers). The divider programming is one of the functions performed by the ROM lookup table in the **ICS1561A**. The VCO gain is also ROM programmable which permits the **ICS1561A** to be optimized for best performance at each frequency in the table.

The feedback divider makes use of a dual modulus prescaler technique that allows construction of a programmable counter to operate at high speeds while still allowing the feedback divider to be programmed in steps of 1. This is an improvement over conventional fixed prescaler architectures that typically impose a factor-of-four penalty (or larger) in this respect.

A post divider may be inserted between the VCO and the CLK and CLK* outputs of the **ICS1561A**. This is useful in generation of lower frequencies, as the VCO has been optimized for high frequency operation. Different post divider settings may be used for each frequency in the table.

Application Information

Power Supplies

The **ICS1561A** has a VDDO pin which is the supply of + 5 volt power to all output stages. This pin should be connected to the power plane (or bus) using standard high frequency decoupling practice. This decoupling consists of a low series inductance bypass capacitor, using the shortest leads possible, mounted close to the **ICS1561A**.

The AVDD pin is the power supply for the synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin (as shown in the recommended application circuitry). This will allow the PLL to "track" through power supply fluctuations without visible effects.

Crystal Oscillator and Crystal Selection

The **ICS1561A** has circuitry onboard to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in anti (also called parallel) resonant mode. See the AC Characteristics for the effective capacitive loading to specify when ordering crystals.

So-called series resonant crystals may also be used with the **ICS1561A**. Be aware that the oscillation frequency will be slightly higher than the frequency that is stamped on the can (typically 0.0050.01%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the **ICS1561A** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

Bus Clock Interface

In some applications, it may be desirable to utilize the bus clock. To do this, connect the clock through a .047uF capacitor to XTAL1 (5) and keep the lead length of the capacitor to XTAL1 (5) to a minimum to reduce noise susceptibility. This input is internally biased at VDD/2. Since TTL compatible clocks typically exhibit a VOH of 3.5V, capacitively coupling the input restores noise immunity. The **ICS1561A** is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of the bus clock is typically outside the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. XTAL2 (6) must be left open in this configuration.

ICS1561A Interface

The **ICS1561A** should be located as close as possible to the video DAC or RAMDAC. The differential output CLOCK drivers are current sourcing only and are designed to drive resistive terminations in a complementary fashion. CLK and CLK* connections should follow good ECL interconnection practice. Terminating resistors should be as close as possible to the RAMDAC.

ICS1561A Standard Patterns

ICS produces standard frequency patterns for the **ICS1561A**. These patterns include the majority of frequencies most customers require. Custom patterns are also available, although a significant volume commitment and/or one-time mask charge will apply. Contact ICS sales for details.

ICS Part Number	ICS1561 -706	ICS1561- 707	ICS1561- Custom Pattern 1	ICS1561- Custom Pattern 2
Video Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	12.273	25.175		
1	14.500	28.322		
2	15.667	32.500		
3	25.175	36.000		
4	28.000	37.500		
5	30.240	40.000		
6	31.500	44.900		
7	38.400	57.000		
8	43.200	64.000		
9	50.400	65.000		
A	50.675	72.000		
B	51.270	74.160		
C	55.000	76.000		
D	57.283	80.000		
E	63.000	84.000		
F	64.000	98.000		
10	68.750	100.000		
11	75.000	107.000		
12	88.500	108.000		
13	99.422	110.000		
14	99.522	112.000		
15	100.000	130.000		
16	112.000	135.000		
17	126.000	140.000		
18	140.000	160.000		
19	160.000	170.000		
1A	180.000	180.000		
1B	200.000	200.000		
1C	217.000	126.500		
1D	60.000	128.000		
1E	250.000	132.000		
1F	7.875	136.710		
Reference Frequency	14.31818 MHz	14.31818 MHz	MHz	MHz

Note: All frequencies above 180MHz in the standard patterns shown above are experimental and are not guaranteed.

Order info: ICS1561M-XXX or ICS1561N-XXX (M = SO pkg., N = DIP pkg., XXX = Pattern number)

User Programmable Differential Output Graphics Clock Generator

Description

The **ICS1562** is a very high performance monolithic phase-locked loop (PLL) frequency synthesizer. Utilizing ICS' advanced CMOS mixed-mode technology, the **ICS1562** provides a low cost solution for high-end video clock generation.

The **ICS1562** has differential video clock outputs (CLK+ and CLK-) that are compatible with industry standard video DAC. Another clock output, LOAD, is provided whose frequency is derived from the main clock by a programmable divider. An additional clock output is available, LD/N2, which is derived from the LOAD frequency and whose modulus may also be programmed.

Operating frequencies are fully programmable with direct control provided for reference divider, pre-scaler, feedback divider and post-scaler.

Reset of the pipeline delay on Brooktree RAMDACs™ may be performed under register control. Outputs may also be set to desired states to facilitate circuit board testing.

Features

- Two programming options:
  ICS1562-001 (Parallel Programming)
  ICS1562-201 (Serial Programming)
- Supports high-resolution graphics - CLK output to 230MHz
- Eliminates need for multiple ECL output crystal oscillators
- Fully programmable synthesizer capability - not just a clock multiplier
- Circuitry included for reset of Brooktree RAMDAC™ pipeline delay
- VRAM shift clock generation capability (-201 option only)
- Line-locked clock generation capability
- External feedback loop capability (-201 option only)
- Compact - 16-pin 0.150" skinny SOIC package

E

Simplified Block Diagram - ICS1562

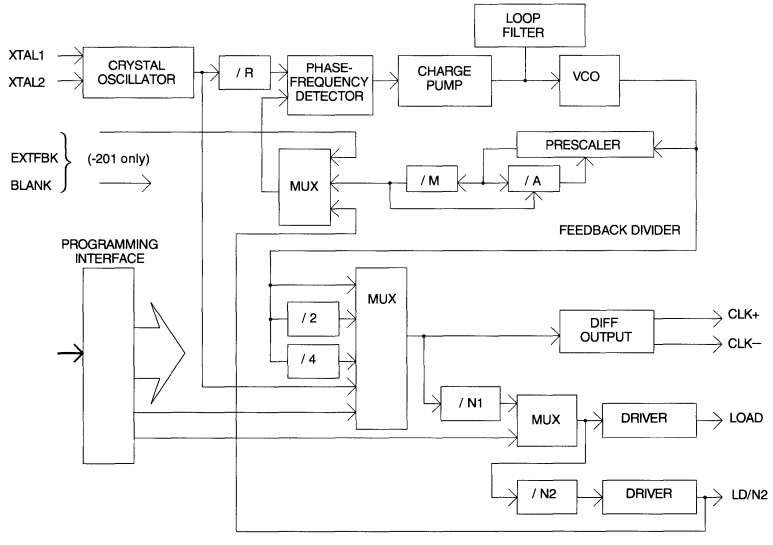


Figure 1

ICS1562 - 001 Pinout

1	AD0	AD1	16
2	XTAL1	AD2	15
3	XTAL2	AD3	14
4	STROBE	VDD	13
5	VSS	VDDO	12
6	VSS	IPRG	11
7	LOAD	CLK+	10
8	LD/N2	CLK–	9

ICS1562 - 201 Pinout

1	EXTFBK	DATA	16
2	XTAL1	$\overline{\text{HOLD}}$	15
3	XTAL2	BLANK	14
4	DATCLK	VDD	13
5	VSS	VDDO	12
6	VSS	IPRG	11
7	LOAD	CLK+	10
8	LD/N2	CLK–	9

Ordering Information
ICS1562M-XXX
(16 pin SOIC package)
(XXX= Pattern number)

Overview

The **ICS1562** is ideally suited to provide the graphics system clock signals required by high-performance video DACs. Fully programmable feedback and reference divider capability allow virtually any frequency to be generated, not just simple multiples of the reference frequency. The **ICS1562** uses the latest generation of frequency synthesis techniques developed by ICS and is completely suitable for the most demanding video applications.

PLL Synthesizer Description - Ratiometric Mode

The **ICS1562** generates its output frequencies using phase-locked loop techniques. The phase-locked loop (or PLL) is a closed-loop feedback system that drives the output frequency to be ratiometrically related to the reference frequency provided to the PLL (see Figure 1). The reference frequency is generated by an on-chip crystal oscillator or the reference frequency may be applied to the **ICS1562** from an external frequency source.

The phase-frequency detector shown in the block diagram drives the voltage-controlled oscillator, or VCO, to a frequency that will cause the two inputs to the phase-frequency detector to be matched in frequency and phase. This occurs when:

$$F(VCO) := \frac{F(XTAL1) \cdot \text{Feedback Divider}}{\text{Reference Divider}}$$

This expression is exact; that is, the accuracy of the output frequency depends solely on the reference frequency provided to the part (assuming correctly programmed dividers).

The VCO gain is programmable, which permits the **ICS1562** to be optimized for best performance at all operating frequencies.

The reference divider may be programmed for any modulus from 1 to 128 in steps of one.

The feedback divider may be programmed for any modulus from 37 through 448 in steps of one. Any even modulus from 448 through 896 can also be achieved by setting the "double" bit which doubles the feedback divider modulus. The feedback divider makes use of a dual-modulus prescaler technique that allows the programmable counters to operate at low speed without sacrificing resolution. This is an improvement over conventional fixed prescaler architectures that typically impose a factor-of-four penalty (or larger) in this respect.

Table 1 permits the derivator of "A" & "M" converter programming directly from desired modulus.

PLL Post-Scaler

A programmable post-scaler may be inserted between the VCO and the CLK+ and CLK- outputs of the **ICS1562**. This is useful in generating of lower frequencies, as the VCO has been optimized for high-frequency operation.

The post-scaler allows the selection of:

- VCO frequency
- VCO frequency divided by 2
- VCO frequency divided by 4
- Internal register bit (AUXCLK) value

Load Clock Divider

The **ICS1562** has an additional programmable divider (referred to in Figure 1 as the N1 divider) that is used to generate the LOAD clock frequency for the video DAC. The modulus of this divider may be set to 3, 4, 5, 6, 8, or 10 under register control. The design of this divider permits the output duty factor to be 50/50, even when an odd modulus is selected. The input frequency to this divider is the output of the PLL post-scaler described above.

Digital Inputs - ICS1562-001 Option

The AD0-AD3 pins and the STROBE pin are used to load all control registers of the **ICS1562** (-001 option). The AD0-AD3 and STROBE pins are each equipped with a pull-up and will be at a logic HIGH level when not connected. They may be driven with standard TTL or CMOS logic families.

The address of the register to be loaded is latched from the AD0-AD3 pins by a negative edge on the STROBE pin. The data for that register is latched from the AD0-AD3 pins by a positive edge on the STROBE pin. See Figure 2 for a timing diagram. After power-up, the **ICS1562-001** requires 32 register writes for new programming to become effective. Since only 13 registers are used at present, the programming system can perform 19 "dummy" writes to address 13 or 14 to complete the sequence.

This allows the synthesizer to be completely programmed for the desired frequency before it is made active. Once the part has been "unlocked" by the 32 writes, programming becomes effective immediately.

ALL registers identified in the data sheet (0-9, 11, 12 & 15) MUST be written upon initial programming. The programming registers are not initialized upon power-up, but the latched outputs of those registers are. The latch is made transparent after 32 register writes. If any register has not been written, the state upon power-up (random) will become effective. Registers 13 & 14 physically do not exist. Register 10 does exist, but is reserved for future expansion. To insure compatibility with possible future modifications to the database, ICS recommends that all three unused locations be written with zero.

ICS1562-001 Register Loading

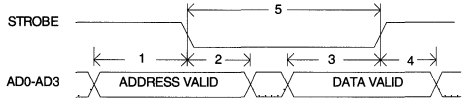


Figure 2

Digital Inputs - ICS1562-201 Option

The programming of the **ICS1562-201** is performed serially by using the DATCLK, DATA, and HOLD~ pins to load an internal shift register.

DATA is shifted into the register on the rising edge of DATCLK. The logic value on the HOLD~ pin is latched at the same time. When HOLD~ is low, the shift register may be loaded without disturbing the operation of the **ICS1562**. When high, the shift register outputs are transferred to the control registers, and the new programming information becomes active. Ordinarily, a high level should be placed on the HOLD~ pin when the last data bit is presented. See Figure 3 for the programming sequence.

ICS1562-201 Register Loading

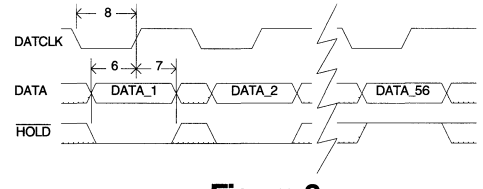


Figure 3

An additional control pin on the **ICS1562-201**, BLANK can perform either of two functions. It may be used to disable the phase-frequency detector in line-locked applications. Alternatively, the BLANK pin may be used as a synchronous enable for VRAM shift clock generation. See sections on Line-Locked Operations and VRAM shift clock generation for details.

Output Description

The differential output drivers, CLK+ and CLK, are current-mode and are designed to drive resistive terminations in a complementary fashion. The outputs are current-sinking only, with the amount of sink current programmable via the IPRG pin. The sink current, which is steered to either CLK+ or CLK-, is four times the current supplied to the **IPRG** pin. For most applications, a resistor from VDDO to IPRG will set the current to the necessary precision.

The LOAD output is a high-current CMOS type drive whose frequency is controlled by a programmable divider that may be selected for a modulus of 3, 4, 5, 6, 8, or 10. It may also be suppressed under register control.

The LD/N2 output is high-current CMOS type drive whose frequency is derived from the LOAD output. The programmable modulus may range from 1 to 512 in steps of one.

Pipeline Delay Reset Function

The **ICS1562** implements the clocking sequence required to reset the pipeline delay on Brooktree RAMDACs™. This sequence can be generated by setting the appropriate register bit (DACRST) to a logic 1 and then resetting to logic 0.

When changing frequencies, it is advisable to allow 500 microseconds after the new frequency is selected to activate the reset function. The output frequency of the synthesizer should be stable enough at that point for the video DAC to correctly execute its reset sequence. See Figure 4 for a diagram of the pipeline delay reset sequence.

Pipeline Delay Reset Timing

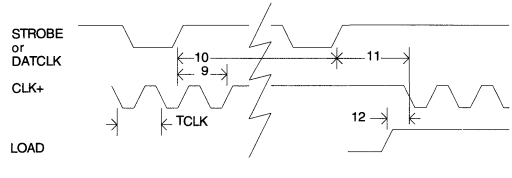


Figure 4

Reference Oscillator and Crystal Selection

The **ICS1562** has circuitry on-board to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in anti- (also called parallel-) resonant mode. See the AC Characteristics for the effective capacitive loading to specify when ordering crystals.

Series-resonant crystals may also be used with the **ICS1562**. Be aware that the oscillation frequency will be slightly higher than the frequency that is stamped on the can (typically 0.025-0.05%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the **ICS1562** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

If an external reference frequency source is to be used with the **ICS1562**, it is important that it be jitter-free. The rising and falling edges of that signal should be fast and free of noise for best results.

The loop phase is locked to the falling edges of the XTAL1 input signals.

Line-Locked Operation

The **ICS1562** supports line-locked clock applications by allowing the LOAD (N1) and N2 divider chains to act as the feedback divider for the PLL.

The N1 and N2 divider chains allow a much larger modulus to be achieved than the PLL's own feedback divider. Additionally, the output of the N2 counter is accessible off-chip for performing horizontal reset of the graphics system, where necessary. This mode is set under register control (ALTLOOP bit). The reference divider (R counter) will ordinarily be set to divide by 1 in this mode, and the HSYNC signal of the external video will be supplied to the XTAL1 input. The output frequency of the synthesizer will then be:

$$F_{(CLK)} := F\ (XTAL1) \cdot N1 \cdot N2.$$

By using the phase-detector hardware disable mode, the PLL can be made to free-run at the beginning of the vertical interval of the external video, and can be reactivated at its completion.

ICS1562-001 The **ICS1562-001** supports phase detector disable via a special control mode. When the PDRSTEN (phase detector reset enable) bit is set and the last address latched is 15 (0Fh), a high level on AD3 will disable PLL locking.

ICS1562-201 The **ICS1562-201** supports phase detector disable via the BLANK pin. When the PDRSTEN bit is set, a high level on the BLANK input will disable PLL locking.

External Feedback Operation

The **ICS1562-201** option also supports the inclusion of an external counter as the feedback divider of the PLL. This mode is useful in graphic systems that must be "genlocked" to external video sources.

When the EXTFBEN bit is set to logic 1, the phase-frequency detector will use the EXTFBK pin as its feedback input. The loop phase will be locked to the rising edges of the signal applied to the EXTFBK input.

VRAM Shift Clock Generation

The **ICS1562-201** option supports VRAM shift clock generation and interruption. By programming the N2 counter to divide by 1, the LD/N2 output becomes a duplicate of the LOAD output. When the SCEN bit is set, the LD/N2 output may be synchronously started and stopped via the blank pin. When BLANK is high, the LD/N2 will be free-running and in phase with LOAD. When BLANK is taken low, the LD/N2 output is stopped at a low level. See Figure 5 for a diagram of the sequence. Note that this use of the **BLANK** pin precludes its use for phase comparator disable (see Line-Locked Operation).

VRAM Shift Clock Control

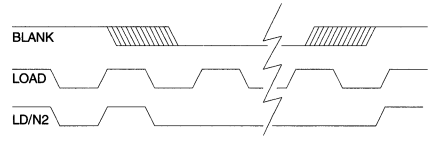


Figure 5

Power-On Initialization

The **ICS1562** has an internal power-on reset circuit that performs the following functions:

1) Sets the multiplexer to pass the reference frequency to the CLK+ and CLK- outputs.

2) Selects the modulus of the N1 divider (for the LOAD clock) to be four.

These functions should allow initialization of most graphics systems that cannot immediately provide for register programming upon system power-up.

Because the power-on reset circuit is on the VDD supply, and because that supply is filtered, care must be taken to allow the reset to de-assert before programming. A safe guideline is to allow 20 microseconds after the VDD supply reaches 4 volts.

Programming Notes

- VCO Frequency Range: Use the post-divider to keep the VCO frequency as high as possible within its operating range.
- Divider Range: For best results in normal situations (i.e, pixel clock generation for hi-res displays), keep the reference divider modulus as short as possible (for a frequency at the output of the reference divider in the few hundred kHz to several MHz range). If you need to go to a lower phase comparator reference frequency (usually required for increased frequency accuracy), that is acceptable, but jitter performance will suffer somewhat.
- VCO Gain Programming: Use the minimum gain which can reliably achieve the VCO frequency desired, as shown here:

VCO GAIN	MAX FREQUENCY
4	120 MHz
5	200 MHz
6	230 MHz
7	*

*SPECIAL APPLICATION. Contact factory for custom product above 230 MHz.

- Phase Detector Gain: For most graphics applications and divider ranges, set P[1,0] = 10 and set P[2] = 1. Under some circumstances, setting the P[2] bit "on" can reduce jitter. During 1562 operation at exact multiples of the crystal frequency, P[2] bit = 0 may provide the best jitter performance.

Board Test Support

It is often desirable to statically control the levels of the output pins for circuit board test. The **ICS1562** supports this through a register programmable mode, AUXEN. When this mode is set, two register bits directly control the logic levels of the CLK+ /CLK- pins and the LOAD pin. This mode is activated when the S[0] and S[1] bits are both set to logic 1. See Register Mapping for details.

Power Supplies and Decoupling

The **ICS1562** has two VSS pins to reduce the effects of package inductance. Both pins are connected to the same potential on the die (the ground bus). BOTH of these pins should connect to the ground plane of the video board as close to the package as is possible.

The **ICS1562** has a VDDO pin which is the supply of + 5 volt power to all output drivers. This pin should be connected to the power plane (or bus) using standard high-frequency decoupling practice. That is, capacitors should have low series inductance and be mounted close to the **ICS1562**.

The VDD pin is the power supply pin for the PLL synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin (as shown in the recommended application circuitry). This will allow the PLL to "track" through power supply fluctuations without visible effects. See Figure 6 for typical external circuitry.

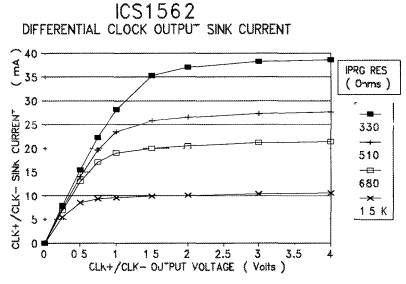
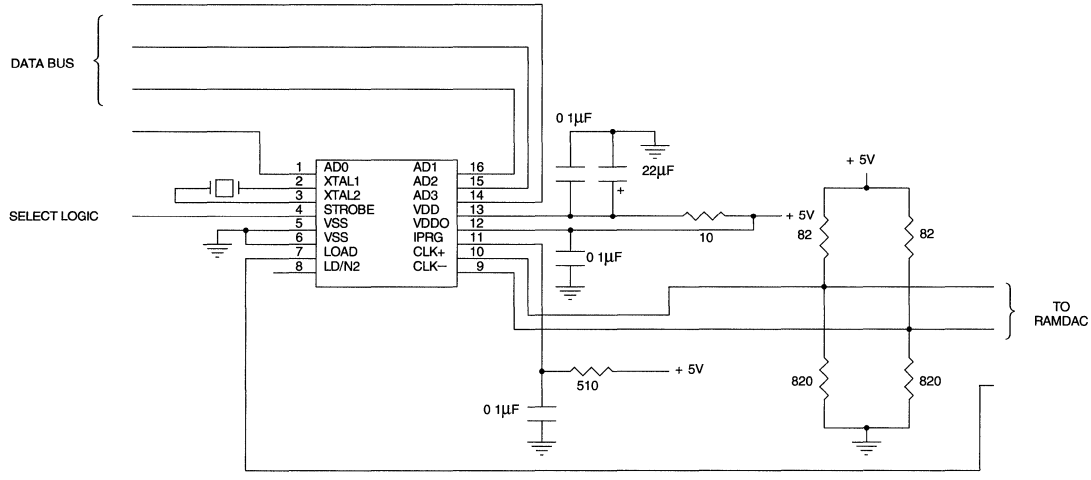


Figure 6

a)

ICS1562-001 Typical Interface



b)

ICS1562-201 Typical Interface

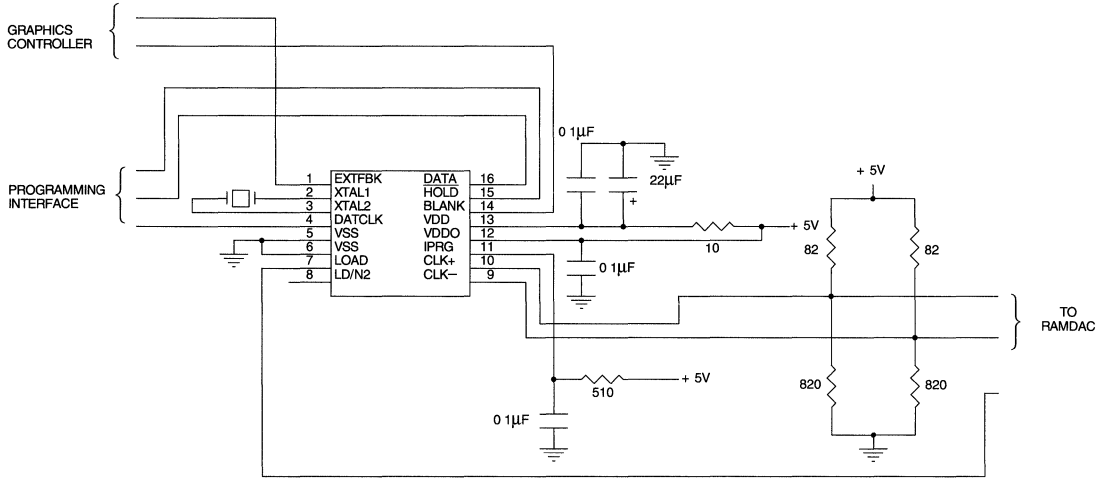


Figure 7

Register Mapping - ICS1562-001 (Parallel Programming Option)

NOTE: IT IS NOT NECESSARY TO UNDERSTAND THE FUNCTION OF THESE BITS TO USE THE ICS1562. PC SOFTWARE IS AVAILABLE FROM ICS TO AUTOMATICALLY GENERATE ALL REGISTER VALUES BASED ON REQUIREMENTS. CONTACT FACTORY FOR DETAILS.

REG#	BIT(S)	BIT REF.	DESCRIPTION
0	0-3	R[0]..R[3]	Reference divider modulus control bits
1	0-2	R[4]..R[6]	Modulus = value + 1
2	0-3	A[0]..A[3]	Controls A counter. When set to zero, modulus= 7. Otherwise, modulus= 7 for "value" underflows of the prescaler, and modulus= 6 thereafter until M counter underflows.
3	0-3	M[0]..M[3]	M counter control bits
4	0-1	M[4]..M[5]	Modulus = value + 1
4	3	DBLFREQ	Doubles modulus of dual-modulus prescaler (from 6/7 to 12/14).
5	0-2	N1[0]..N1[2]	Sets N1 modulus according to this table. These bits are set to implement a divide-by-four on power-up.

N1[2]	N1[1]	N1[0]	RATIO
0	0	0	3
0	0	1	4
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	8
1	1	0	8
1	1	1	10

6	0-3	N2[0]..N2[3]	Sets the modulus of the N2 divider.
7	0-2	N2[4]..N2[7]	The input of the N2 divider is the output of the N1 divider in all clock modes except AUXEN.
8	3	N2[8]	
8	0-2	V[0]..V[1]	Sets the gain of the VCO.

V[2]	V[1]	V[0]	VCO GAIN (MHz/VOLT)
1	0	0	30
1	0	1	45
1	1	0	60
1	1	1	80

REG#	BIT(S)	BIT REF.	DESCRIPTION
9	0-1	P[0]..P[1]	Sets the gain of the phase detector according to this table.

P[1]	P[0]	GAIN (uA/radian)
0	0	0.05
0	1	0.15
1	0	0.5
1	1	1.5

9	3	[P2]	Phase detector tuning bit. Normally should be set to one.
11	0-1	S[0]..S[1]	PLL post-scaler/test mode select bits

S[1]	S[0]	DESCRIPTION
0	0	Post-scaler= 1. F(CLK)= F(PLL). The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
0	1	Post-scaler= 2. F(CLK)= F(PLL)/2. The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
1	0	Post-scaler= 4. F(CLK)= F(PLL)/4. The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
1	1	AUXEN CLOCK MODE. The AUXCLK bit drives the differential outputs CLK+ and CLK- and the AUXN1 bit drives the LOAD output which, in turn, drives the N2 divider.

11	2	AUX_CLK	When in the AUXEN clock mode, this bit controls the differential outputs.
11	3	AUX_N1	When in the AUXEN clock mode, this bit controls the LOAD output (and consequently the N2 output according to its programming).
12	0	RESERVED	Must be set to zero.
12	1	JAMPLL	Tristates phase detector outputs; resets phase detector logic, and resets R, A, M, and N2 counters.
12	2	DACRST	Set to zero for normal operation. When set to one, the CLK+ output is kept high and the CLK- output is kept low. (All other device functions are unaffected.) When returned to zero, the CLK+ and CLK- outputs will resume toggling on a rising edge of the LD output (+ /- 1 CLK period). To initiate a RAMDAC™ reset sequence, simply write a one to this register bit followed by a zero.
12	3	SELXTAL	When set to logic 1, passes the reference frequency to the post-scaler.
15	0	ALTLOOP	Controls substitution of N1 and N2 dividers into feedback loop of PLL. When this bit is a logic 1, the N1 and N2 dividers are used.
15	3	PDRSTEN	Phase-detector reset enable control bit. When this bit is set, the AD3 pin becomes a transparent reset input to the phase detector. See LINE-LOCKED CLOCK GENERATION section for more details on the operation of this function.

Register Mapping - ICS1562-201 (Serial Programming Option)

NOTE: IT IS NOT NECESSARY TO UNDERSTAND THE FUNCTION OF THESE BITS TO USE THE ICS1562 PC SOFTWARE IS AVAILABLE FROM ICS TO AUTOMATICALLY GENERATE ALL REGISTER VALUES BASED ON REQUIREMENTS CONTACT FACTORY FOR DETAILS

BIT(S)	BIT REF.	DESCRIPTION
1-3	N1[0]..N1[2]	Sets N1 modulus according to this table. These bits are set to implement a divide-by-four on power-up.

N1[2]	N1[1]	N1[0]	RATIO
0	0	0	3
0	0	1	4
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	8
1	1	0	8
1	1	1	10

4	RESERVED	Set to zero.
5	RESERVED	MUST be set to zero. If this bit is ever programmed for a logic one, device operation will cease and further serial data load into the registers will be inhibited until a power-off/power-on sequence.
6	JAMPLL	Tristates phase detector outputs, resets phase detector logic, and resets R, A, M, and N2 counters.
7	DACRST	Set to zero for normal operations. When set to one, the CLK+ output is kept high and the CLK- output is kept low. (All other device functions are unaffected.) When returned to zero, the CLK+ and CLK- outputs will resume toggling on a rising edge of the LD output (+ /– 1 CLK period). To initiate a RAMDAC™ reset sequence, simply write a one to this register bit followed by a zero.
8	SELXTAL	When set to logic 1, passes the reference frequency to the post-scaler.
9	ALTLOOP	Controls substitution of N1 and N2 dividers into feedback loop of PLL. When this bit is a logic 1, the N1 and N2 dividers are used.
10	SCEN	VRAM shift clock enable bit. When logic 1, the BLANK pin can be used to disable the LD/N2 output.
11	EXTFBKEN	External PLL feedback select. When logic 1, the EXTFBK pin is used for the phase-frequency detector feedback input.
12	PDRSTEN	Phase detector reset enable control bit. When this bit is set, a high level on the BLANK input will disable PLL locking. See LINE-LOCKED CLOCK GENERATION section for more details on the operation of this function.

BIT(S)	BIT REF.	DESCRIPTION
13-14	S[0]..S[1]	PLL post-scaler/test mode select bits.

S[1]	S[0]	DESCRIPTION
0	0	Post-scaler= 1. F(CLK)= F(PLL). The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
0	1	Post-scaler= 2. F(CLK)= F(PLL)/2. The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
1	0	Post-scaler= 4. F(CLK)= F(PLL)/4. The output of the N1 divder drives the LOAD output which, in turn, drives the N2 divider.
1	1	AUXEN CLOCK MODE. The AUXCLK bit drives the differential outputs CLK+ and CLK- and the AUXN1 bit drives the LOAD output which, in turn, drives the N2 divider.

15	AUX_CLK	When in the AUXEN clock mode, this bit controls the differential outputs.
16	AUX_N1	When in the AUXEN clock mode, this bit controls the N1 output (and consequently the N2 output according to its programming).
17-24 28	N2[0]..N2[7] N2[8]	Sets the modulus of the N2 divider. The input of the N2 divider is the output of the N1 divider in all clock modes except AUXEN.
25-27	V[0]..V[2]	Sets the gain of VCO.

V[2]	V[1]	V[0]	VCO GAIN (MHz/VOLT)
1	0	0	30
1	0	1	45
1	1	0	60
1	1	1	80

29-30	P[0]..P[1]	Sets the gain of the phase detector according to this table.

P[1]	P[0]	GAIN (uA/radian)
0	0	0.05
0	1	0.15
1	0	0.5
1	1	1.5

31	RESERVED	Set to zero.
32	P[2]	Phase detector tuning bit. Should normally be set to one.

BIT(S)	BIT REF.	DESCRIPTION
33-38	M[0]..M[5]	M counter control bits Modulus = value + 1
39	RESERVED	Set to zero.
40	DBLFREQ	Doubles modulus of dual-modulus prescaler (from 6/7 to 12/14).
41-44	A[0]..A[3]	Controls A counter. When set to zero, modulus= 7. Otherwise, modulus= 7 for "value" underflows of the prescaler, and modulus= 6 thereafter until M counter underflows.
45-48	RESERVED	Set to zero.
49-55	R[0]..R[6]	Reference divider modulus control bits Modulus = value + 1
56	RESERVED	Set to zero.

Table 1 - "A" & "M" Divider Programming
Feedback Divider Modulus Table

A[2]..A[0]- M[5]..M[0]	001	010	011	100	101	110	111	000
000000								7
000001	13							14
000010	19	20						21
000011	25	26	27					28
000100	31	32	33	34				35
000101	37	38	39	40	41			42
000110	43	44	45	46	47	48		49
000111	49	50	51	52	53	54	55	56
001000	55	56	57	58	59	60	61	63
001001	61	62	63	64	65	66	67	70
001010	67	68	69	70	71	72	73	77
001011	73	74	75	76	77	78	79	84
001100	79	80	81	82	83	84	85	91
001101	85	86	87	88	89	90	91	98
001110	91	92	93	94	95	96	97	105
001111	97	98	99	100	101	102	103	112
010000	103	104	105	106	107	108	109	119
010001	109	110	111	112	113	114	115	126
010010	115	116	117	118	119	120	121	133
010011	121	122	123	124	125	126	127	140
010100	127	128	129	130	131	132	133	147
010101	133	134	135	136	137	138	139	154
010110	139	140	141	142	143	144	145	161
010111	145	146	147	148	149	150	151	168
011000	151	152	153	154	155	156	157	175
011001	157	158	159	160	161	162	163	182
011010	163	164	165	166	167	168	169	189
011011	169	170	171	172	173	174	175	196
011100	175	176	177	178	179	180	181	203
011101	181	182	183	184	185	186	187	210
011110	187	188	189	190	191	192	193	217
011111	193	194	195	196	197	198	199	224

A[2]..A[0]- M[5]..M[0]	001	010	011	100	101	110	111	000
100000	199	200	201	202	203	204	205	231
100001	205	206	207	208	209	210	211	238
100010	211	212	213	214	215	216	217	245
100011	217	218	219	220	221	222	223	252
100100	223	224	225	226	227	228	229	259
100101	229	230	231	232	233	234	235	266
100110	235	236	237	238	239	240	241	273
100111	241	242	243	244	245	246	247	280
101000	247	248	249	250	251	252	253	287
101001	253	254	255	256	257	258	259	294
101010	259	260	261	262	263	264	265	301
101011	265	266	267	268	269	270	271	308
101100	271	272	273	274	275	276	277	315
101101	277	278	279	280	281	282	283	322
101110	283	284	285	286	287	288	289	329
101111	289	290	291	292	293	294	295	336
110000	295	296	297	298	299	300	301	343
110001	301	302	303	304	305	306	307	350
110010	307	308	309	310	311	312	313	357
110011	313	314	315	316	317	318	319	364
110100	319	320	321	322	323	324	325	371
110101	325	326	327	328	329	330	331	378
110110	331	332	333	334	335	336	337	385
110111	337	338	339	340	341	342	343	392
111000	343	344	345	346	347	348	349	399
111001	349	350	351	352	353	354	355	406
111010	355	356	357	358	359	360	361	413
111011	361	362	363	364	365	366	367	420
111100	367	368	369	370	371	372	373	427
111101	373	374	375	376	377	378	379	434
111110	379	380	381	382	383	384	385	441
111111	385	386	387	388	389	390	391	448

Notes:

To use this table, find the desired modulus in the table. Follow the column up to find the A divider programming values. Follow the row to the left to find the M divider programming. Some feedback divisors can be achieved with two or three combinations of divider settings. Any are acceptable for use.

The formula for the effective feedback modulus is: $N = [(M + 1) \cdot 6] + A$

except when A= 0, then: $N = (M + 1) \cdot 7$

Under all circumstances: $A \leq M$

Pin Descriptions - ICS1562-001

PIN#	NAME	DESCRIPTION
10	CLK+	Clock out (non-inverted)
9	CLK–	Clock out (inverted)
7	LOAD	Load output. This output is normally at the CLK frequency divided by N1.
2	XTAL1	Quartz crystal connection 1/external reference frequency input
3	XTAL2	Quartz crystal connection 2
1	AD0	Address/Data Bit 0 (LSB)
16	AD1	Address/Data Bit 1
15	AD2	Address/Data Bit 2
14	AD3	Address/Data Bit 3 (MSB)
8	LD/N2	Divided LOAD output. See text.
4	STROBE	Control for address/data latch
13	VDD	PLL system power (+ 5V. See application diagram.)
12	VDDO	Output stage power (+ 5V)
11	IPRG	Output stage current set
5,6	VSS	Device ground. Both pins must be connected to the same ground potential.

E

Pin Descriptions - ICS1562-002

PIN#	NAME	DESCRIPTION
10	CLK+	Clock out (non-inverted)
9	CLK–	Clock out (inverted)
7	LOAD	Load output. This output is normally at the CLK frequency divided by N1.
2	XTAL1	Quartz crystal connection 1/external reference frequency input
3	XTAL2	Quartz crystal connection 2
4	DATCLK	Data Clock (Input)
16	DATA	Serial Register Data (Input)
15	HOLD~	$\overline{\text{HOLD}}$ (Input)
14	BLANK	Blanking (Input). See Text.
8	LD/N2	Divided LOAD output/shift clock. See text.
1	EXTFBK	External feedback connection for PLL (input). See text.
13	VDD	PLL system power (+ 5V. See application diagram.)
12	VDDO	Output stage power (+ 5V)
11	IPRG	Output stage current set
5,6	VSS	Device ground. Both pins must be connected.

Absolute Maximum Ratings

VDD, VDDO (measured to V_{SS}) ..... 7.0 V
Digital Inputs ..... V_{SS}-0.5 to V_{DD} + 0.5 V
Digital Outputs ..... V_{SS}-0.5 to V_{DDO} + + 0.5 V
Ambient Operating Temperature ..... -55 to 125 °C
Storage Temperature ..... -65 to 150 °C
Junction Temperature ..... 175 °C
Soldering Temperature ..... 260 °C

Recommended Operating Conditions

VDD, VDDO (measured to V_{SS}) ..... 4.75 to 5.25 V

Operating Temperature (Ambient) ..... 0 to 70 °C

DC Characteristics

TTL-Compatible Inputs
001 Option - (AD0-AD3, STROBE),
201 Option - (DATCLK, DATA, HOLD, BLANK, EXTFBK)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	V_{ih}		2.0	V_{DD}+ 0.5	V
Input Low Voltage	V_{il}		V_{SS}-0.5	0.8	V
Input High Current	I_{ih}	V_{ih}= VDD	-	10	uA
Input Low Current	I_{il}	V_{il}= 0.0	-	200	uA
Input Capacitance	C_{in}		-	8	pF

XTAL1 Input

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	V_{xh}		3.75	V_{DD}+ 0.5	V
Input Low Voltage	V_{xl}		V_{SS}-0.5	1.25	

CLK+ , CLK- Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Differential Output Voltage			0.6	-	V

LOAD, LD/N2 Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output High Voltage (Ioh = 4.0mA)			2.4	-	V
Output Low Voltage (Iol = 8.0mA)			-	0.4	V

AC Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
F_{vco}	VCO Frequency (see Note 1)	20		230	MHz
F_{xtal}	Crystal Frequency	5		20	MHz
Cpar	Crystal Oscillator Loading Capacitance		20		pF
F_{load}	LOAD Frequency			80	MHz
T_{xhi}	XTAL1 High Time (when driven externally)	8			ns
T_{xlo}	XTAL1 Low Time (when driven externally)	8			ns
T_{lock}	PLL Acquire Time (to within 1%)		500		µs
I_{dd}	VDD Supply Current		15	t.b.d.	mA
I_{ddo}	VDDO Supply Current (excluding CLK+ /– termination)		20	t.b.d.	mA
	DIGITAL INPUTS - ICS1562-001				
1	Address Setup Time	10			ns
2	Address Hold Time	10			ns
3	Data Setup Time	10			ns
4	Data Hold Time	10			ns
5	STROBE Pulse Width (T_{hi} or T_{lo})	20			ns
	DIGITAL INPUTS - ICS1562-201				
6	DATA/HOLD~ Setup Time	10			ns
7	DATA/HOLD~ Hold Time	10			ns
8	DATCLK Pulse Width (T_{hi} or T_{lo})	20			ns
	PIPELINE DELAY RESET				
9	Reset Activation Time			2*Tclk	ns
10	Reset Duration	4*Tload			ns
11	Restart Delay			2*Tload	ns
12	Restart Matching	-1*Tclk		+ 1.5*Tclk	ns
	DIGITAL OUTPUTS				
13	CLK+ /CLK– Clock Rate			230	MHz
14	LOAD To LD/N2 Skew (Shift Clock Mode)	-2	0	+ 2	ns

Note 1: Use of the post-divider is required for frequencies lower than 20MHz on CLK+ & CLK- outputs. Use of the post-divider is recommended for output frequencies lower than 65MHz.

Note 2: Using load circuit of Figure 6. Duty cycle measured at zero crossings of difference voltage between CLK+ and CLK-.

Note 3: Cumulative jitter is defined as the maximum error (in the domain) if any CLK edge, at any point in time, compared with the equivalent edge generated by an ideal frequency source.
ICS laboratory testing indicates that the typical value shown above can be treated as a maximum jitter specification in virtually all applications. Jitter performance can depend somewhat on circuit board layout, decoupling, and register programming.

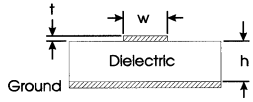
E

Output Circuit Considerations for the ICS1562

Output Circuitry

The dot clock signals CLK and CLK- are typically the highest frequency signals present in the workstation. To minimize problems with EMI, crosstalk, and capacitive loading extra care should be taken in laying out this area of the PC board. The **ICS1562** is packaged in a 0.2"-wide 16-pin SOIC package. This permits the clock generator, crystal, and related components to be laid out in an area the size of a postage stamp. The **ICS1562** should be placed as close as possible to the RAMDAC. The CLK and CLK- pins are running at VHF frequencies; one should minimize the length of PCB trace connecting them to the RAMDAC so that they don't become radiators of RF energy.

At the frequencies that the **ICS1562** is capable of, PC board traces may be long enough to be a significant portion of a wavelength of that frequency. PC traces for CLK and CLK- should be treated as transmission lines, not just interconnecting wires. These lines can take two forms: microstrip and stripline. A microstrip line is shown below:



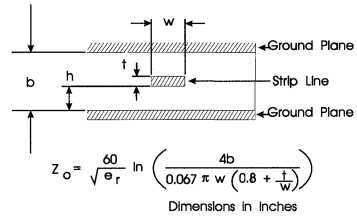
$$Z_o = \frac{87}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98h}{0.8w+t}\right)$$

Dimensions in inches

Microstrip Line

Essentially, the microstrip is a copper trace on a PCB over a ground plane. Typically, the dielectric is G10 glass epoxy. It differs from a standard PCB trace in that its width is calculated to have a characteristic impedance. To calculate the characteristic impedance of a microstrip line one must know the width and thickness of the trace, and the thickness and dielectric constant of the dielectric. For G10 glass epoxy, the dielectric constant (e_r) is about 5. Propagation delay is strictly a function of dielectric constant. For G10 propagation, delay is calculated to be 1.77 ns/ft.

Stripline is the other form a PCB transmission line can take. A buried trace between ground planes (or between a power plane and a ground plane) is common in multi-layer boards. Attempting to create a workstation design without the use of multi-layer boards would be adventurous to say the least, the issue would more likely be whether to place the interconnect on the surface or between layers. The between layer approach would work better from an EMI standpoint, but would be more difficult to lay out. A stripline is shown below:



$$Z_o = \frac{60}{\sqrt{e_r}} \ln\left(\frac{4b}{0.067\,\pi\, w\left(0.8 + \frac{t}{w}\right)}\right)$$

Dimensions in inches

Stripline

Using 1oz. copper (0.0015" thick) and 0.040"thickness G10, a 0.010" trace will exhibit a characteristic impedance of 75Ω in a stripline configuration.

Typically, RAMDACS require a V_{ih} of V_{AA}-1.0 Volts as a guaranteed logical "1" and a V_{il} of V_{AA}-1.6 as a guaranteed logical "0". Worst case input capacitance is 10 pF.

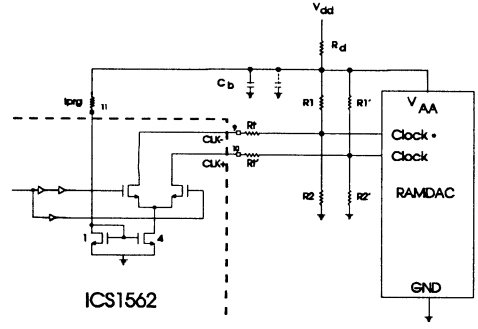
Output circuitry for the **ICS1562** is shown in the following diagram. It consists of a 4/1 current mirror, and two open drain output FETs along with inverting buffers to alternately enable each current-sinking driver. Both CLK and CLK- outputs are connected to the respective CLOCK and CLOCK* inputs of the RAMDAC with transmission lines and terminated in their equivalent impedances by the Thevenin equivalent impedances of R1 and R2 or R1' and R2'.

The **ICS1562** is incapable of sourcing current, so V_{th} must be set by the ratios of these resistors for each of these lines. R1 and R2 are electrically in parallel from an AC standpoint because V_{dd} is bypassed to ground through bypass-capacitor network C_b. If we picked a target impedance of 75Ω for our transmission line impedance, a value of 91Ω for R1 and R1' and a value of 430Ω for R2 and R2' would yield a Thevinin equivalent characteristic impedance of 75.1W and a Vih value of VAA-.873 Volts, a margin of 0.127Volts. This may be adequate; however, at higher frequencies one must contend with the 10 pF input capacitance of the RAMDAC. Values of 82Ω for R1 and R1' and 820Ω for R2 and R2' would give us a characteristic impedance of 74.5Ω and a V_{th} value of V_{AA}-.45. With a .55 Volt margin on V_{th}, this voltage level might be safer.

To set a value for V_{il}, we must determine a value for I_{prg} that will cause the output FET's to sink an appropriate current. We desire V_{il} to be V_{AA}-1.6 or greater. V_{AA}-2 would seem to be a safe value. Setting up a sink current of 25 milliamperes would guarantee this through our 82Ω pull-up resistors. As this is controlled by a 4/1 current mirror, 7 mA into I_{prg} should set this current properly. A 510Ω resistor from V_{dd} to I_{prg} should work fine.

Resistors Rt and Rt' are shown as series terminating resistors at the ICS1562 end of the transmission lines. These are not required for operation, but may be useful for meeting EMI requirements. Their intent is to interact with the input capacitance of the RAMDAC and the distributed capacitance of the transmission line to soften up rise and fall times and consequently cut some of the high-order harmonic content that is more likely to radiate RF energy. In actual usage they would most likely be 10 to 20Ω resistors or possibly ferrite beads.

C_b is shown as multiple capacitors. Typically, a 22 µF tantalum should be used with separate .1 µF and 220pF capacitors placed as close to the pins as possible. This provides low series inductance capacitors right at the source of high frequency energy. R_d is used to isolate the circuitry from external sources of noise. Five to ten ohms should be adequate.



ICS1562 Output Circuitry

Great care must be used when evaluating high frequency circuits to achieve meaningful results. The 10 pF input capacitance and long ground lead of an ordinary scope probe will make any measurements made with it meaningless. A low capacitance FET probe with a ground connection directly connected to the shield at the tip will be required. A 1GHz bandwidth scope will be barely adequate, try to find a faster unit.

E

Differential Output Video Dot Clock Generator

Features

- High frequency operation for extended video modes - up to 180 MHz
- Compatible with Brooktree high performance RAMDACs™
  a) Differential output clocks with ECL logic levels
  b) Programmable divider modulus for load clock
  c) Circuitry included for automatic reset of Brooktree RAMDAC™ pipeline delay
- Low cost - eliminates need for multiple ECL crystal clock oscillators in video display systems
- Strobed/Transparent frequency select options
- 32-user selected mask-programmable frequencies
- Fast acquisition of selected frequencies, strobed or non-strobed
- Advanced PLL for low phase-jitter
- Dynamic control of VCO sensitivity providing optimized loop gain over entire frequency range
- Small footprint - 16 pin wide body (300 mil) SOIC

Applications

- Workstations
- High-resolution PC and MAC displays
- 8514A - TMS340X0 systems
- EGA - VGA - Super VGA video
- Telecom reference clock generation - suitable for Sonet, ATM and other data rates up to 155.52 Mb.

E

Description

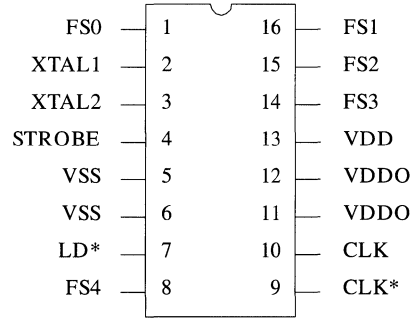
The **ICS1567** is a very high performance monolithic PLL frequency synthesizer. Utilizing ICS' advanced CMOS mixed-mode technology, the **ICS1567** provides a low cost solution for high-end video clock generation, and for telecom system clock generation.

The **ICS1567** has differential video clock outputs (CLK and CLK*) that are compatible with industry standard video DACs & RAMDACs. An additional clock output, LD*, is provided, whose frequency is divided down from the main clock by a programmable divider.

Operating frequencies are selectable from a pre-programmed (customer-defined) table. An on-chip crystal oscillator for generating the reference frequency is provided on the **ICS1567**.

Programming of the **ICS1567** is accomplished via frequency select pins on the package. The **ICS1567** has five lines plus a STROBE pin which permits selection of 32 frequencies. Reset of the pipeline delay on Brooktree RAMDACs is automatically performed on a rising edge of the STROBE line.

Pin Configuration



Ordering Information
ICS1567MXXX (16 pin SOIC Package)
(XXX= Pattern number)

Block Diagram

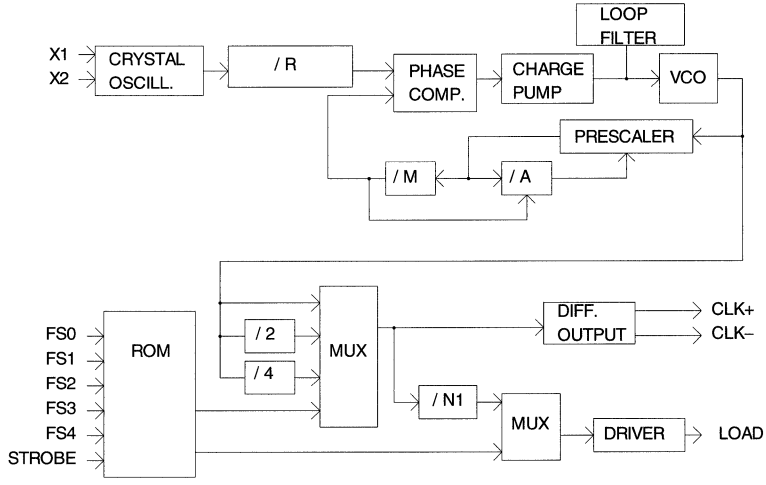


Figure 1

System Schematic

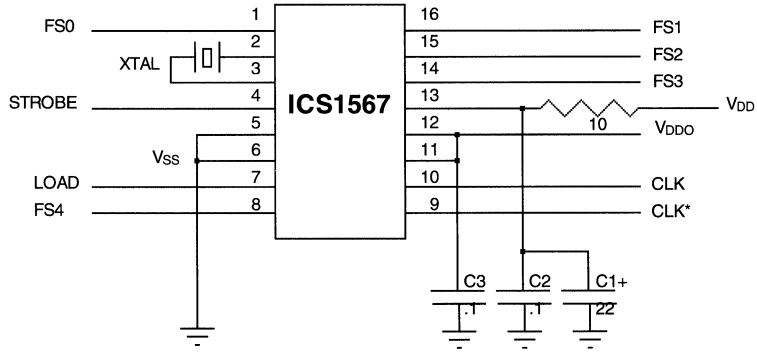
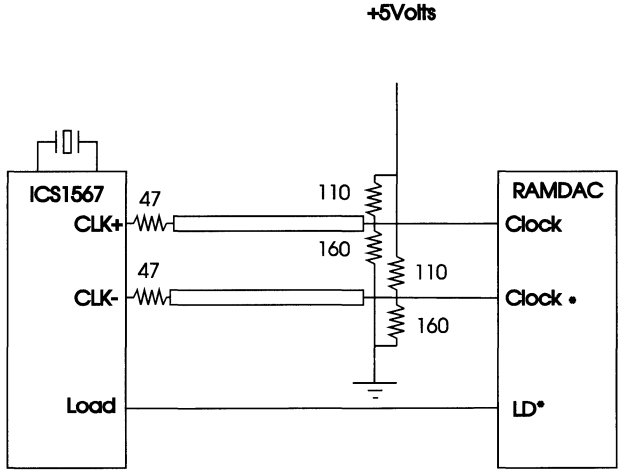


Figure 2

Typical Output Configuration



Notes:
CLK & CLK* outputs are pseudo-ECL. Logic low level is set by the ratio of the resistors stacked across the power supply V_{LO} = (V supply • 160)/(110 + 160) in the example shown above.
The above values are a good starting point for RAMDAC™ or clock generator interface.

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Figure 3

Pin Description

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
1	• FS0	IN	Frequency Select LSB
2	XTAL1	IN	Crystal Interface/External Oscillator Input
3	XTAL2	OUT	Crystal Interface
4	• STROBE	IN	Control For Frequency Select Latch, also performs automatic RAMDAC reset
5	VSS	--	Device Ground (Both pins must be connected.)
6	VSS	--	Device Ground (Both pins must be connected.)
7	LD*	OUT	Load Output. This output is at CLK frequency divided by N1.
8	• FS4	IN	Frequency Select MSB
9	CLK*	OUT	Clock Output Inverted
10	CLK	OUT	Clock Output Non-Inverted
11	VDDO	--	Output Stage Power (Both pins must be connected)
12	VDDO	--	Output Stage Power (Both pins must be connected)
13	VDD	--	PLL System Power
14	• FS3	IN	Frequency Select
15	• FS2	IN	Frequency Select
16	• FS1	IN	Frequency Select

• = inputs with internal pull-up resistor

Circuit Description

Overview

The **ICS1567** is designed to provide the graphics system clock signals required by industry standard RAMDACs. One of 32 pre-programmed (user-definable) frequencies may be selected under digital control. Fully programmable feedback and reference divider capability allow virtually any frequency to be generated, not just simple multiples of the reference frequency. The **ICS1567** uses the latest generation of frequency synthesis techniques developed by ICS and is completely suitable for the most demanding video applications.

Digital Inputs

The FS0-FS4 pins and the STROBE pin are used to select the desired operating frequency from the 32 pre-programmed frequencies in the ROM table of the **ICS1567**. The STROBE pin also controls activation of the pipeline delay RESET function included in the **ICS1567** (see PIPELINE DELAY RESET section for details). The FS0-FS4 and STROBE pins are each equipped with a pull-up and will be at a logic HIGH level when not connected.

Transparent Mode - When the STROBE pin is held HIGH, the FS0 through FS4 inputs are transparent; that is, they directly access the ROM table. The synthesizer will output the frequency programmed into the location addressed by the FS0-FS4 pins.

Latched Mode - When the STROBE pin is held LOW, the FS0-FS4 pins are ignored. The synthesizer will output the frequency corresponding to the state of the FS0-FS4 pins when the STROBE pin was last HIGH. In the event that the **ICS1567** is powered-up with the STROBE pin held LOW, the synthesizer will output the frequency programmed into address 0 (i.e., the one selected with FS0 through FS4 at a logic LOW level).

Frequency Synthesizer Description

Refer to Figure 1 for a block diagram of the **ICS1567**. The reference frequency is generated by an on-chip crystal oscillator, or the reference frequency may be applied to the **ICS1567** from an external frequency source.

The **ICS1567** generates its output frequencies using phase-locked loop techniques. The phase-locked loop (or PLL) is a closed-loop feedback system that drives the output frequency to be ratiometrically related to the reference frequency provided to the PLL. The phase-frequency detector shown in the block diagram drives the VCO to a frequency that will cause the two inputs to the phase-frequency detector to be matched in frequency and phase. This occurs when:

$$F(vco) = \frac{F(XTAL1) \bullet \text{Feedback Divider}}{\text{Reference Divider}}$$

This expression is exact; that is, the accuracy of the output frequency depends solely on the reference frequency provided to the part (assuming correctly-programmed dividers). The divider programming is one of the functions performed by the ROM look-up table in the **ICS1567**. The VCO gain is also ROM programmable which permits the **ICS1567** to be optimized for best performance at each frequency in the table.

The feedback divider makes use of a dual-modulus prescaler technique that allows construction of a programmable counter to operate at high speeds while still allowing the feedback divider to be programmed in steps of 1. This is an improvement over conventional fixed prescaler architectures that typically impose a factor-of-four penalty (or larger) in this respect.

A post-divider may be inserted between the VCO and the CLK and CLK* outputs of the **ICS1567**. This is useful in generation of lower frequencies, as the VCO has been optimized for high-frequency operation. Different post-divider settings may be used for each frequency in the table.

Load Clock Divider

The **ICS1567** has an additional programmable divider that is used to generate the LOAD frequency. The modulus of this divider may be set to 3, 4, 5, 6, 8, or 10. The design of this divider permits the output duty factor to be 50/50, even when an odd modulus is selected.

The selection of the modulus is done by the ROM look-up table. A different modulus may, therefore, be selected for each frequency address.

Pipeline Delay Reset Function

The **ICS1567** implements the clocking sequence required to reset the pipeline delay on Brooktree RAMDACs. This sequence is automatically generated by the **ICS1567** upon any rising edge of the STROBE line.

When the frequency select inputs (FS0-FS4) are used in a transparent mode, simply lower and raise the STROBE line to activate the function. When the frequency select inputs are latched, simply load the same frequency into the **ICS1567** twice.

When changing frequencies, it is advisable to allow 500uSec after the new frequency is selected to activate the reset function. The output frequency of the synthesizer should be stable enough at that point for the RAMDAC to correctly execute its reset sequence.

See Figure 4 for a diagram of the clock sequencing.

Output Stage Description

The CLK and CLK* outputs are each connected to the drains of P-Channel MOSFET devices. The source of each of these devices is connected to VDDO. Typical on resistance of each device is 15 Ohms. These outputs will drive the clock and clock* of a RAMDAC device when a resistive network equivalent to Figure 3 is utilized.

The LD* output is a high-current CMOS type drive whose frequency is controlled by a programmable divider that may be selected for a modulus of 3, 4, 5, 6, 8, or 10. Under control of the ROM, this output may also be suppressed (logic low level) at any frequency select address, if desired.

Application Information

Power Supplies

The **ICS1567** has two VSS pins to reduce the effects of package inductance. Both pins are connected to the same potential on the die (the ground bus). BOTH of these pins should connect to the ground plane of the video board as close to the package as is possible.

The **ICS1567** has two VDDO pins which are the supply of + 5 volt power to all output stages. Again, both VDDO pins connect to the same point on the die. BOTH of these pins should be connected to the power plane (or bus) using standard high-frequency decoupling practice. This decoupling consists of a low series inductance bypass capacitor, using the shortest leads possible, mounted close to the **ICS1567**.

The VDD pin is the power supply for the synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin (as shown in the recommended application circuitry). This will allow the PLL to "track" through power supply fluctuations without visible effects.

Crystal Oscillator and Crystal Selection

The **ICS1567** has circuitry on-board to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in anti- (also called parallel-) resonant mode. See the AC Characteristics for the effective capacitive loading to specify when ordering crystals.

So-called series-resonant crystals may also be used with the **ICS1567**. Be aware that the oscillation frequency will be slightly higher than the frequency that is stamped on the can (typically 0.005-0.01%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the **ICS1567** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

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Application Notes *(continued)*

Bus Clock Interface

In some applications, it may be desirable to utilize the bus clock. To do this, connect the clock through a .047uF capacitor to XTAL1 (2) and keep the lead length of the capacitor to XTAL1 (2) to a minimum to reduce noise susceptibility. This input is internally biased at VDD/2. Since TTL compatible clocks typically exhibit a VOH of 3.5V, capacitively coupling the input restores noise immunity. The **ICS1567** is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of the bus clock is typically outside the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. XTAL2 (3) must be left open in this configuration.

ICS1567 Interface

The **ICS1567** should be located as close as possible to the video DAC or RAMDAC. Figure 3 illustrates interfacing the **ICS1567** to a RAMDAC. The differential output CLOCK drivers are current sourcing only and are designed to drive resistive terminations in a complementary fashion. CLK and CLK* connections should follow good ECL interconnection practice. Terminating resistors should be as close as possible to the RAMDAC.

Absolute Maximum Ratings

Ambient Temeperature under bias....	T_O	0°C to 70°C
Supply Voltage	V_{DD}	-0.5V to + 7V
Input Voltage.....	V_{IN}	-0.5V to V_{DD} + 0.5V
Output Voltage	V_{OUT}	-0.5V to V_{DD} + 0.5V
Clamp Diode Current.....	V_{IK} & I_{OK}	+ /-30mA
Output Current per Pin	I_{OUT}	+ /-50mA
Storage Temperature	T_S	-85°C to + 150°C
Power Dissipation.....	P_D	500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation, it is recommended that V_{IN} and V_{OUT} be constrained to > = V_{SS} and < = V_{DD}.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to VSS (OV Ground). Positive current flows into the referenced pin.

Operating Temperature range	0°C to 70°C
Power supply voltage	4.75 to 5.25 Volts

DC Characteristics

PARAMETER	SYMBOL	MIN	MAX	UNITS	CONDITIONS
Input High Voltage	V_{IH}	2.0	V_{DD} + 0.5	V	
Input Low Voltage	V_{IL}	V_{SS} -0.5	0.8	V	
Input High Current	I_{IH}		10	uA	V_{IN} = V_{DD}
Input Low Current	I_{IL}		-200	uA	V_{IN} = V_{SS}
LOAD OUTPUT					
Output High Voltage	V_{OH}	2.4		V	I_{OH} = -4.0 mA
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 6.0 mA
CLOCK OUTPUTS					
Differential Output Voltage (CLK-CLK*)	V_{OD}	1.2		V	See Figure 4
XTAL1 INPUT					
Input High Voltage	V_{XH}	3.75	V_{DD} + 0.5	V	
Input Low Voltage	V_{XL}	VSS -0.5	1.25	V	
Operating Current	I_{DD}		50	mA	Outputs Unloaded
Input Pin Capacitance	C_{IN}		8	pF	F_C = 1 MHz
Output Pin Capacitance	C_{OUT}		12	pF	F_C = 1 MHz

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AC Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK and CLK* TIMING						
Duty Cycle	T_{HIGH}	40		60	%	3, 4, 9
Frequency Error				0.5	%	
Rise Time	T_r			2	ns	5, 9
Fall Time	T_f			2	ns	5, 9
VCO Frequency	F_{VCO}	20		180	MHz	1
PLL Acquire Time	T_{LOCK}		500		uS	
LD* TIMING						
Duty Cycle	T_{HIGH}	40		60	%	6
Load Frequency	F_{LOAD}			60	MHz	
Rise Time	T_r			2	ns	7, 8
Fall Time	T_f			2	ns	7, 8
REFERENCE INPUT CLOCK						
Crystal Frequency	F_{XTAL}	5		20	MHz	
Crystal Oscillator Loading Capacitance	C_{PAR}		20		pF	
XTAL1 High Time	T_{XHI}	8			ns	2
XTAL1 Low Time	T_{XLO}	8			ns	2
Rise Time	T_r			10	ns	2, 7
Fall Time	T_f			10	ns	2, 7
DIGITAL INPUTS						
Frequency Select Setup Time	1	10			ns	10
Frequency Select Hold Time	2	10			ns	10
Strobe Pulse Width	3	20			ns	10
PIPELINE DELAY RESET						
Reset Activation	4			$2*T_{CLK}$	ns	10
Reset Duration	5	$4*T_{CLK}$			ns	10
Restart Delay	6	$-1*T_{CLK}$		$+ 1.5*T_{CLK}$	ns	10

Notes:

1. Use of the post-divider is required for frequencies lower than 20 MHz on CLK and CLK* outputs. Use of the post-divider is recommended for output frequencies lower than 65 MHz.
2. Values for XTAL1 driven by an external clock
3. Duty Cycle for Differential Output (CLK- CLK*)
4. Duty cycle measured at VOD/2 for Differential CLK Output
5. Rise and fall time between 20% and 80% of VOD
6. Duty cycle measured at 1.4v for TTL I/O
7. Rise and fall time between 0.8 and 2.0 VDC for TTL I/O
8. Output pin loading = 15 pf
9. See Figure 3.
10. See Figure 4.

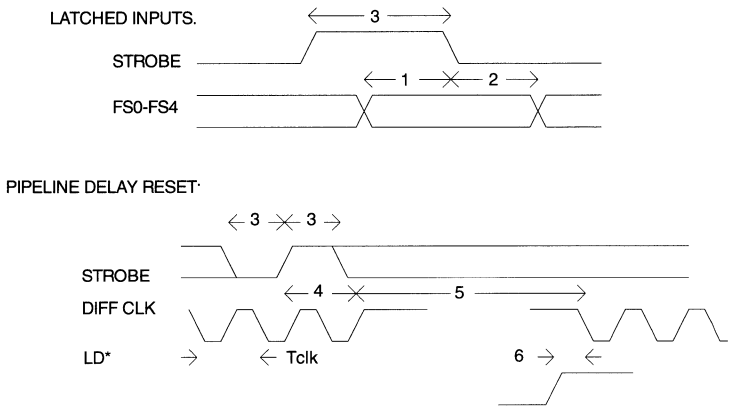
LATCHED INPUTS.
3
STROBE
1
2
FS0-FS4
PIPELINE DELAY RESET·
3
3
STROBE
4
5
DIFF CLK
LD*
Tclk
6

Figure 4

ICS1567 Pattern Request Form

Custom patterns are also available, although a significant volume commitment and/or one-time mask charge will apply. Contact ICS Sales for details.

ICS Part Number	ICS1567-742	ICS1567-Custom Pattern # 1
Video Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)
0	112.000	
1	148.000	
2	OFF	
3	135.000	
4	31.500	
5	105.500	
6	78.000	
7	86.000	
8	108.000	
9	120.000	
10	128.000	
11	93.000	
12	112.000	
13	148.000	
14	135.000	
15	89.210	
16	105.500	
17	112.000	
18	25.000	
19	45.000	
20	64.000	
21	75.000	
22	78.000	
23	86.000	
24	103.000	
25	108.000	
26	120.000	
27	127.000	
28	128.000	
29	135.000	
30	112.000	
31	148.000	

Custom pattern # 1 reference frequency = _____

Standard parttern shown above uses 16.000 MHz as the input reference frequency.
Order info: ICS1567M-XXX or ICS1567N-XXX (M= SO pkg., N= DIP pkg., XXX= Pattern number)

Integrated Circuit Systems, Inc.

User Programmable Differential Output Graphics Clock Generator

Description

The **ICS1572** is a high performance monolithic phase-locked loop (PLL) frequency synthesizer. Utilizing ICS' advanced CMOS mixed-mode technology, the **ICS1572** provides a low cost solution for high-end video clock generation in workstations and high-end PC applications.

The **ICS1572** has differential video clock outputs (CLK+ and CLK-) that are compatible with industry standard video DACs. Another clock output, LOAD, is provided whose frequency is derived from the main clock by a programmable divider. An additional clock output is available, LD/N2, which is derived from the LOAD frequency and whose modulus may also be programmed.

Operating frequencies are fully programmable with direct control provided for reference divider, pre-scaler, feedback divider and post-scaler.

Reset of the pipeline delay on Brooktree RAMDACs™ may be performed under register control. Outputs may also be set to desired states to facilitate circuit board testing.

Features

- Supports high-resolution graphics - CLK output to 180 MHz
- Eliminates need for multiple ECL output crystal oscillators
- Fully programmable synthesizer capability - not just a clock multiplier
- Available in 20-pin 300 mil wide body SOIC package
- Available in both parallel (101) and serial (301) programming versions
- Circuit included for reset of Brooktree RAMDAC pipeline delay

Applications

- Workstations
- AutoCad Accelerators
- High-end PC graphics systems

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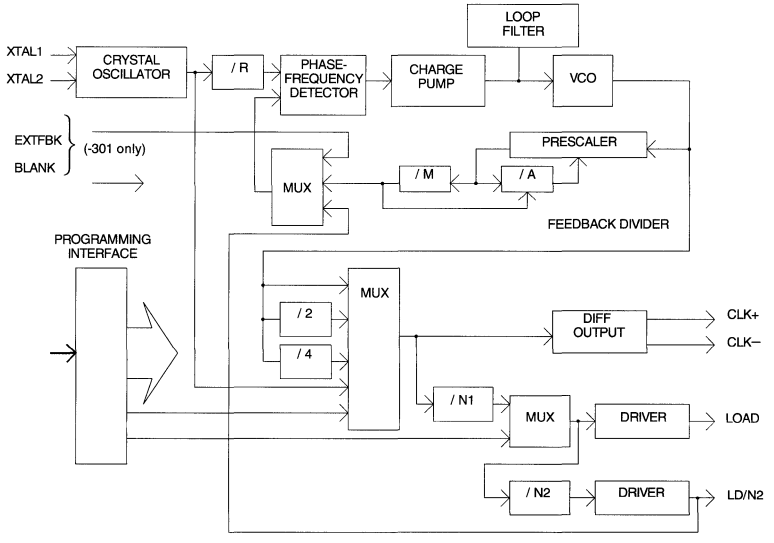


ICS1572-101 Pinout

1	N C	N C	20
2	AD0	AD1	19
3	XTAL1	AD2	18
4	XTAL2	AD3	17
5	STROBE	VDD	16
6	VSS	VDDO	15
7	VSS	IPRG	14
8	LOAD	CLK+	13
9	LD/N2	CLK–	12
10	N C	N C	11

ICS1572-301 Pinout

1	N C	N C	20
2	EXTFBK	DATA	19
3	XTAL1	$\overline{\text{HOLD}}$	18
4	XTAL2	BLANK	17
5	DATCLK	VDD	16
6	VSS	VDDO	15
7	VSS	IPRG	14
8	LOAD	CLK+	13
9	LD/N2	CLK–	12
10	N C	N C	11

Figure 1

RAMDAC is a trademark of Brooktree Corporation

Overview

The **ICS1572** is ideally suited to provide the graphics system clock signals required by high-performance video DACs. Fully programmable feedback and reference divider capability allow virtually any frequency to be generated, not just simple multiples of the reference frequency. The **ICS1572** uses the latest generation of frequency synthesis techniques developed by ICS and is completely suitable for the most demanding video applications.

PLL Synthesizer Description - Ratiometric Mode

The **ICS1572** generates its output frequencies using phase-locked loop techniques. The phase-locked loop (or PLL) is a closed-loop feedback system that drives the output frequency to be ratiometrically related to the reference frequency provided to the PLL (see Figure 1). The reference frequency is generated by an on-chip crystal oscillator or the reference frequency may be applied to the **ICS1572** from an external frequency source.

The phase-frequency detector shown in the block diagram drives the voltage-controlled oscillator, or VCO, to a frequency that will cause the two inputs to the phase-frequency detector to be matched in frequency and phase. This occurs when:

$$F(VCO) := \frac{F(XTAL1) \cdot \text{Feedback Divider}}{\text{Reference Divider}}$$

This expression is exact; that is, the accuracy of the output frequency depends solely on the reference frequency provided to the part (assuming correctly programmed dividers).

The VCO gain is programmable, which permits the **ICS1572** to be optimized for best performance at all operating frequencies.

The reference divider may be programmed for any modulus from 1 to 128 in steps of one.

The feedback divider may be programmed for any modulus from 37 through 391 in steps of one. Any even modulus from 392 through 782 can also be achieved by setting the "double" bit which doubles the feedback divider modulus. The feedback divider makes use of a dual-modulus prescaler technique that allows the programmable counters to operate at low speed without sacrificing resolution. This is an improvement over conventional fixed prescaler architectures that typically impose a factor-of-four penalty (or larger) in this respect.

Table 1 permits the derivation of "A" & "M" counter programming directly from desired modulus.

PLL Post-Scaler

A programmable post-scaler may be inserted between the VCO and the CLK+ and CLK- outputs of the **ICS1572**. This is useful in generating of lower frequencies, as the VCO has been optimized for high-frequency operation.

The post-scaler allows the selection of:

- VCO frequency
- VCO frequency divided by 2
- VCO frequency divided by 4
- Internal register bit (AUXCLK) value

Load Clock Divider

The ICS1572 has an additional programmable divider (referred to in Figure 1 as the N1 divider) that is used to generate the LOAD clock frequency for the video DAC. The modulus of this divider may be set to 3, 4, 5, 6, 8, or 10 under register control. The design of this divider permits the output duty factor to be 50/50, even when an odd modulus is selected. The input frequency to this divider is the output of the PLL post-scaler described above.

Digital Inputs - ICS1572-101 Option

The AD0-AD3 pins and the STROBE pin are used to load all control registers of the **ICS1572** (-101 option). The AD0-AD3 and STROBE pins are each equipped with a pull-up and will be at a logic HIGH level when not connected. They may be driven with standard TTL or CMOS logic families.

The address of the register to be loaded is latched from the AD0-AD3 pins by a negative edge on the STROBE pin. The data for that register is latched from the AD0-AD3 pins by a positive edge on the STROBE pin. See Figure 2 for a timing diagram. After power-up, the **ICS1572-101** requires 32 register writes for new programming to become effective. Since only 13 registers are used at present, the programming system can perform 19 "dummy" writes to address 13 or 14 to complete the sequence.

This allows the synthesizer to be completely programmed for the desired frequency before it is made active. Once the part has been "unlocked" by the 32 writes, programming becomes effective immediately.

ALL registers identified in the data sheet (0-9, 11, 12 & 15) MUST be written upon initial programming. The programming registers are not initialized upon power-up, but the latched outputs of those registers are. The latch is made transparent after 32 register writes. If any register has not been written, the state upon power-up (random) will become effective. Registers 13 & 14 physically do not exist. Register 10 does exist, but is reserved for future expansion. To insure compatibility with possible future modifications to the database, ICS recommends that all three unused locations be written with zero.

ICS1572-101 Register Loading

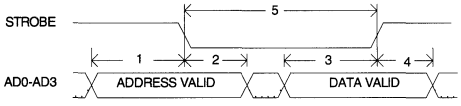


Figure 2

Digital Inputs - ICS1572-301 Option

The programming of the **ICS1572-301** is performed serially by using the DATCLK, DATA, and HOLD~ pins to load an internal shift register.

DATA is shifted into the register on the rising edge of DATCLK. The logic value on the HOLD~ pin is latched at the same time. When HOLD~ is low, the shift register may be loaded without disturbing the operation of the **ICS1572**. When high, the shift register outputs are transferred to the control registers, and the new programming information becomes active. Ordinarily, a high level should be placed on the HOLD~ pin when the last data bit is presented. See Figure 3 for the programming sequence.

ICS1572-301 Register Loading

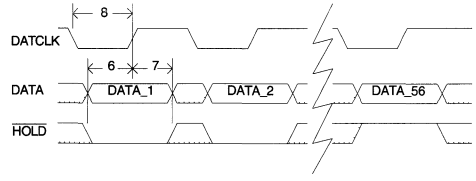


Figure 3

An additional control pin on the **ICS1572-301**, BLANK can perform either of two functions. It may be used to disable the phase-frequency detector in line-locked applications. Alternatively, the BLANK pin maybe used as a synchronous enable for VRAM shift clock generation. See sections on Line-Locked Operations and VRAM shift clock generation for details.

Output Description

The differential output drivers, CLK+ and CLK, are current-mode and are designed to drive resistive terminations in a complementary fashion. The outputs are current-sinking only, with the amount of sink current programmable via the IPRG pin. The sink current, which is steered to either CLK+ or CLK-, is approximately four times the current supplied to the **IPRG** pin. For most applications, a resistor from VDDO to IPRG will set the current to the necessary precision. See Figure 6 for output characteristics.

The LOAD output is a high-current CMOS type drive whose frequency is controlled by a programmable divider that may be selected for a modulus of 3, 4, 5, 6, 8, or 10. It may also be suppressed under register control.

The LD/N2 output is high-current CMOS type drive whose frequency is derived from the LOAD output. The programmable modulus may range from 1 to 512 in steps of one.

Pipeline Delay Reset Function

The **ICS1572** implements the clocking sequence required to reset the pipeline delay on Brooktree RAMDACs. This sequence can be generated by setting the appropriate register bit (DACRST) to a logic 1 and then resetting to logic 0.

When changing frequencies, it is advisable to allow 500 microseconds after the new frequency is selected to activate the reset function. The output frequency of the synthesizer should be stable enough at that point for the video DAC to correctly execute its reset sequence. See Figure 4 for a diagram of the pipeline delay reset sequence.

Pipeline Delay Reset Timing

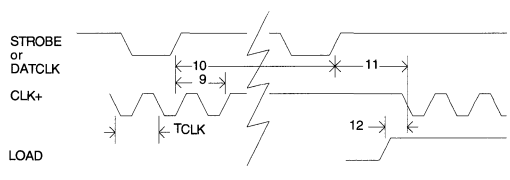


Figure 4

Reference Oscillator and Crystal Selection

The **ICS1572** has circuitry on-board to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in anti- (also called parallel-) resonant mode. See the AC Characteristics for the effective capacitive loading to specify when ordering crystals.

Series-resonant crystals may also be used with the **ICS1572**. Be aware that the oscillation frequency will be slightly higher than the frequency that is stamped on the can (typically 0.025-0.05%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the **ICS1572** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

If an external reference frequency source is to be used with the **ICS1572**, it is important that it be jitter-free. The rising and falling edges of that signal should be fast and free of noise for best results.

The loop phase is locked to the falling edges of the XTAL1 input signals.

Line-Locked Operation

The **ICS1572** supports line-locked clock applications by allowing the LOAD (N1) and N2 divider chains to act as the feedback divider for the PLL.

The N1 and N2 divider chains allow a much larger modulus to be achieved than the PLL's own feedback divider. Additionally, the output of the N2 counter is accessible off-chip for performing horizontal reset of the graphics system, where necessary. This mode is set under register control (ALTLOOP bit). The reference divider (R counter) is set to divide by 1 in this mode, and the HSYNC signal of the external video will be supplied to the XTAL1 input. The output frequency of the synthesizer will then be:

$$F_{(CLK)} := F\ (XTAL1) \cdot N1 \cdot N2.$$

By using the phase-detector hardware disable mode, the PLL can be made to free-run at the beginning of the vertical interval of the external video, and can be reactivated at its completion.

ICS1572-101 The **ICS1572-101** supports phase detector disable via a special control mode. When the PDRSTEN (phase detector reset enable) bit is set, a high level on AD3 will disable PLL locking.

ICS1572-301 The **ICS1572-301** supports phase detector disable via the BLANK pin. When the PDRSTEN bit is set, a high level on the BLANK input will disable PLL locking.

External Feedback Operation

The **ICS1572-301** option also supports the inclusion of an external counter as the feedback divider of the PLL. This mode is useful in graphic systems that must be "genlocked" to external video sources.

When the EXTFBEN bit is set to logic 1, the phase-frequency detector will use the EXTFBK pin as its feedback input. The loop phase will be locked to the rising edges of the signal applied to the EXTFBK input.

VRAM Shift Clock Generation

The **ICS1572-301** option supports VRAM shift clock generation and interruption. By programming the N2 counter to divide by 1, the LD/N2 output becomes a duplicate of the LOAD output. When the SCEN bit is set, the LD/N2 output may be synchronously started and stopped via the blank pin. When BLANK is high, the LD/N2 will be free-running and in phase with LOAD. When BLANK is taken low, the LD/N2 output is stopped at a low level. See Figure 5 for a diagram of the sequence. Note that this use of the **BLANK** pin precludes its use for phase comparator disable (see Line-Locked Operation).

VRAM Shift Clock Control

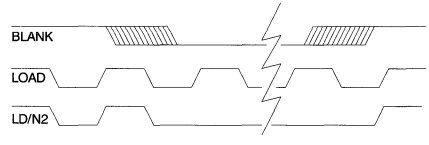


Figure 5

Power-On Initialization

The **ICS1572** has an internal power-on reset circuit that performs the following functions:

1) Sets the multiplexer to pass the reference frequency to the CLK+ and CLK- outputs.

2) Selects the modulus of the N1 divider (for the LOAD clock) to be four.

These functions should allow initialization of most graphics systems that cannot immediately provide for register programming upon system power-up.

Because the power-on reset circuit is on the VDD supply, and because that supply is filtered, care must be taken to allow the reset to de-assert before programming. A safe guideline is to allow 20 microseconds after the VDD supply reaches 4 volts.

Programming Notes

- VCO Frequency Range: Use the post-divider to keep the VCO frequency as high as possible within its operating range.
- Divider Range: For best results in normal situations (i.e., pixel clock generation for hi-res displays), keep the reference divider modulus as short as possible (for a frequency at the output of the reference divider in the few hundred kHz to several MHz range). If you need to go to a lower phase comparator reference frequency (usually required for increased frequency accuracy), that is acceptable, but jitter performance will suffer somewhat.
- VCO Gain Programming: Use the minimum gain which can reliably achieve the VCO frequency desired, as shown here:

VCO GAIN	MAX FREQUENCY
4	120 MHz
5	200 MHz
6	230 MHz
7	*

* SPECIAL APPLICATION Contact factory for custom product above 230 MHz.

- Phase Detector Gain: For most graphics applications and divider ranges, set P[1,0] = 10 and set P[2] = 1. Under some circumstances, setting the P[2] bit "on" can reduce jitter. During 1572 operation at exact multiples of the crystal frequency, P[2] bit = 0 may provide the best jitter performance.

Board Test Support

It is often desirable to statically control the levels of the output pins for circuit board test. The **ICS1572** supports this through a register programmable mode, AUXEN. When this mode is set, two register bits directly control the logic levels of the CLK+ /CLK- pins and the LOAD pin. This mode is activated when the S[0] and S[1] bits are both set to logic 1. See Register Mapping for details.

Power Supplies and Decoupling

The **ICS1572** has two VSS pins to reduce the effects of package inductance. Both pins are connected to the same potential on the die (the ground bus). BOTH of these pins should connect to the ground plane of the video board as close to the package as is possible.

The **ICS1572** has a VDDO pin which is the supply of + 5 volt power to all output drivers. This pin should be connected to the power plane (or bus) using standard high-frequency decoupling practice. That is, capacitors should have low series inductance and be mounted close to the **ICS1572**.

The VDD pin is the power supply pin for the PLL synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin (as shown in the recommended application circuitry). This will allow the PLL to "track" through power supply fluctuations without visible effects. See Figure 7 for typical external circuitry.

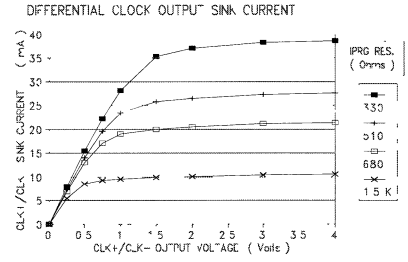


Figure 6

ICS1572 Typical Interface

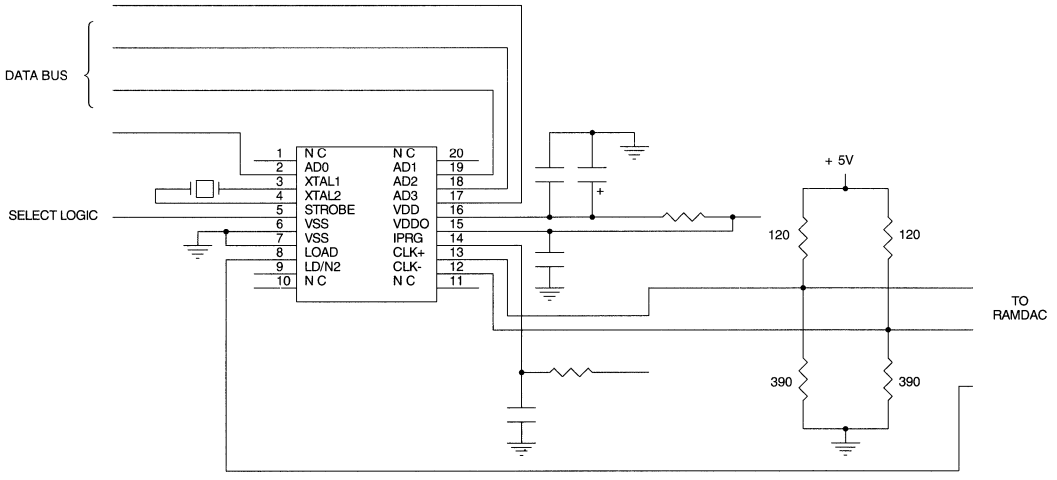


Figure 3

Register Mapping - ICS1572-101 (Parallel Programming Option)

NOTE: IT IS NOT NECESSARY TO UNDERSTAND THE FUNCTION OF THESE BITS TO USE THE ICS1572 PC SOFTWARE IS AVAILABLE FROM ICS TO AUTOMATICALLY GENERATE ALL REGISTER VALUES BASED ON REQUIREMENTS CONTACT FACTORY FOR DETAILS

REG#	BIT(S)	BIT REF.	DESCRIPTION
0	0-3	R[0]..R[3]	Reference divider modulus control bits
1	0-2	R[4]..R[6]	Modulus = value + 1
2	0-3	A[0]..A[3]	Controls A counter. When set to zero, modulus= 7. Otherwise, modulus= 7 for "value" underflows of the prescaler, and modulus= 6 thereafter until M counter underflows.
3	0-3	M[0]..M[3]	M counter control bits
4	0-1	M[4]..M[5]	Modulus = value + 1
4	3	DBLFREQ	Doubles modulus of dual-modulus prescaler (from 6/7 to 12/14).
5	0-2	N1[0]..N1[2]	Sets N1 modulus according to this table. These bits are set to implement a divide-by-four on power-up.

N1[2]	N1[1]	N1[0]	RATIO
0	0	0	3
0	0	1	4
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	8
1	1	0	8
1	1	1	10

6	0-3	N2[0]..N2[3]	Sets the modulus of the N2 divider. Modulus = value + 1
7	0-3	N2[4]..N2[7]	The input of the N2 divider is the output of the N1 divider in all clock modes except AUXEN.
8	3	N2[8]	
8	0-2	V[0]..V[1]	Sets the gain of the VCO.

V[2]	V[1]	V[0]	VCO GAIN (MHz/VOLT)
1	0	0	30
1	0	1	45
1	1	0	60
1	1	1	80

REG#	BIT(S)	BIT REF.	DESCRIPTION
9	0-1	P[0]..P[1]	Sets the gain of the phase detector according to this table.

P[1]	P[0]	GAIN (uA/radian)
0	0	0.05
0	1	0.15
1	0	0.5
1	1	1.5

9	3	[P2]	Phase detector tuning bit. Normally should be set to one.
11	0-1	S[0]..S[1]	PLL post-scaler/test mode select bits

S[1]	S[0]	DESCRIPTION
0	0	Post-scaler= 1. F(CLK)= F(PLL). The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
0	1	Post-scaler= 2. F(CLK)= F(PLL)/2. The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
1	0	Post-scaler= 4. F(CLK)= F(PLL)/4. The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
1	1	AUXEN CLOCK MODE. The AUXCLK bit drives the differential outputs CLK+ and CLK- and the AUXN1 bit drives the LOAD output which, in turn, drives the N2 divider.

11	2	AUX_CLK	When in the AUXEN clock mode, this bit controls the differential outputs.
11	3	AUX_N1	When in the AUXEN clock mode, this bit controls the LOAD output (and consequently the N2 output according to its programming).
12	0	RESERVED	Must be set to zero.
12	1	JAMPLL	Tristates phase detector outputs; resets phase detector logic, and resets R, A, M, and N2 counters.
12	2	DACRST	Set to zero for normal operation. When set to one, the CLK+ output is kept high and the CLK- output is kept low. (All other device functions are unaffected.) When returned to zero, the CLK+ and CLK- outputs will resume toggling on a rising edge of the LD output (+ /- 1 CLK period). To initiate a RAMDAC™ reset sequence, simply write a one to this register bit followed by a zero.
12	3	SELXTAL	When set to logic 1, passes the reference frequency to the post-scaler.
15	0	ALTLOOP	Controls substitution of N1 and N2 dividers into feedback loop of PLL. When this bit is a logic 1, the N1 and N2 dividers are used.
15	3	PDRSTEN	Phase-detector reset enable control bit. When this bit is set, the AD3 pin becomes a transparent reset input to the phase detector. See LINE-LOCKED CLOCK GENERATION section for more details on the operation of this function.

Register Mapping - ICS1572-301 (Serial Programming Option)

NOTE IT IS NOT NECESSARY TO UNDERSTAND THE FUNCTION OF THESE BITS TO USE THE ICS1572. PC SOFTWARE IS AVAILABLE FROM ICS TO AUTOMATICALLY GENERATE ALL REGISTER VALUES BASED ON REQUIREMENTS. CONTACT FACTORY FOR DETAILS

BIT(S)	BIT REF.	DESCRIPTION
1-3	N1[0]..N1[2]	Sets N1 modulus according to this table. These bits are set to implement a divide-by-four on power-up.

N1[2]	N1[1]	N1[0]	RATIO
0	0	0	3
0	0	1	4
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	8
1	1	0	8
1	1	1	10

4	RESERVED	Set to zero.
5	RESERVED	MUST be set to zero. If this bit is ever programmed for a logic one, device operation will cease and further serial data load into the registers will be inhibited until a power-off/power-on sequence.
6	JAMPLL	Tristates phase detector outputs, resets phase detector logic, and resets R, A, M, and N2 counters.
7	DACRST	Set to zero for normal operations. When set to one, the CLK+ output is kept high and the CLK- output is kept low. (All other device functions are unaffected.) When returned to zero, the CLK+ and CLK- outputs will resume toggling on a rising edge of the LD output (+ /– 1 CLK period). To initiate a RAMDAC™ reset sequence, simply write a one to this register bit followed by a zero.
8	SELXTAL	When set to logic 1, passes the reference frequency to the post-scaler.
9	ALTLOOP	Controls substitution of N1 and N2 dividers into feedback loop of PLL. When this bit is a logic 1, the N1 and N2 dividers are used.
10	SCEN	VRAM shift clock enable bit. When logic 1, the BLANK pin can be used to disable the LD/N2 output.
11	EXTFBKEN	External PLL feedback select. When logic 1, the EXTFBK pin is used for the phase-frequency detector feedback input.
12	PDRSTEN	Phase detector reset enable control bit. When this bit is set, a high level on the BLANK input will disable PLL locking. See LINE-LOCKED CLOCK GENERATION section for more details on the operation of this function.

BIT(S)	BIT REF.	DESCRIPTION
13-14	S[0]..S[1]	PLL post-scaler/test mode select bits.

S[1]	S[0]	DESCRIPTION
0	0	Post-scaler= 1. F(CLK)= F(PLL). The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
0	1	Post-scaler= 2. F(CLK)= F(PLL)/2. The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
1	0	Post-scaler= 4. F(CLK)= F(PLL)/4. The output of the N1 divider drives the LOAD output which, in turn, drives the N2 divider.
1	1	AUXEN CLOCK MODE. The AUXCLK bit drives the differential outputs CLK+ and CLK- and the AUXN1 bit drives the LOAD output which, in turn, drives the N2 divider.

15	AUX_CLK	When in the AUXEN clock mode, this bit controls the differential outputs.
16	AUX_N1	When in the AUXEN clock mode, this bit controls the N1 output (and consequently the N2 output according to its programming).
17-24 28	N2[0]..N2[7] N2[8]	Sets the modulus of the N2 divider. The input of the N2 divider is the output of the N1 divider in all clock modes except AUXEN.
25-27	V[0]..V[2]	Sets the gain of VCO.

V[2]	V[1]	V[0]	VCO GAIN (MHz/VOLT)
1	0	0	30
1	0	1	45
1	1	0	60
1	1	1	80

29-30 P[0]..P[1] Sets the gain of the phase detector according to this table.

P[1]	P[0]	GAIN (uA/radian)
0	0	0.05
0	1	0.15
1	0	0.5
1	1	1.5

31	RESERVED	Set to zero.
32	P[2]	Phase detector tuning bit. Should normally be set to one.

BIT(S)	BIT REF.	DESCRIPTION
33-38	M[0]..M[5]	M counter control bits Modulus = value + 1
39	RESERVED	Set to zero.
40	DBLFREQ	Doubles modulus of dual-modulus prescaler (from 6/7 to 12/14).
41-44	A[0]..A[3]	Controls A counter. When set to zero, modulus= 7. Otherwise, modulus= 7 for "value" underflows of the prescaler, and modulus= 6 thereafter until M counter underflows.
45-48	RESERVED	Set to zero.
49-55	R[0]..R[6]	Reference divider modulus control bits Modulus = value + 1
56	RESERVED	Set to zero.

Table 1 - "A" & "M" Divider Programming
Feedback Divider Modulus Table

A[2]..A[0]- M[5]..M[0]	001	010	011	100	101	110	111	000
000000								7
000001	13							14
000010	19	20						21
000011	25	26	27					28
000100	31	32	33	34				35
000101	37	38	39	40	41			42
000110	43	44	45	46	47	48		49
000111	49	50	51	52	53	54	55	56
001000	55	56	57	58	59	60	61	63
001001	61	62	63	64	65	66	67	70
001010	67	68	69	70	71	72	73	77
001011	73	74	75	76	77	78	79	84
001100	79	80	81	82	83	84	85	91
001101	85	86	87	88	89	90	91	98
001110	91	92	93	94	95	96	97	105
001111	97	98	99	100	101	102	103	112
010000	103	104	105	106	107	108	109	119
010001	109	110	111	112	113	114	115	126
010010	115	116	117	118	119	120	121	133
010011	121	122	123	124	125	126	127	140
010100	127	128	129	130	131	132	133	147
010101	133	134	135	136	137	138	139	154
010110	139	140	141	142	143	144	145	161
010111	145	146	147	148	149	150	151	168
011000	151	152	153	154	155	156	157	175
011001	157	158	159	160	161	162	163	182
011010	163	164	165	166	167	168	169	189
011011	169	170	171	172	173	174	175	196
011100	175	176	177	178	179	180	181	203
011101	181	182	183	184	185	186	187	210
011110	187	188	189	190	191	192	193	217
011111	193	194	195	196	197	198	199	224

A[2]..A[0]- M[5]..M[0]	001	010	011	100	101	110	111	000
100000	199	200	201	202	203	204	205	231
100001	205	206	207	208	209	210	211	238
100010	211	212	213	214	215	216	217	245
100011	217	218	219	220	221	222	223	252
100100	223	224	225	226	227	228	229	259
100101	229	230	231	232	233	234	235	266
100110	235	236	237	238	239	240	241	273
100111	241	242	243	244	245	246	247	280
101000	247	248	249	250	251	252	253	287
101001	253	254	255	256	257	258	259	294
101010	259	260	261	262	263	264	265	301
101011	265	266	267	268	269	270	271	308
101100	271	272	273	274	275	276	277	315
101101	277	278	279	280	281	282	283	322
101110	283	284	285	286	287	288	289	329
101111	289	290	291	292	293	294	295	336
110000	295	296	297	298	299	300	301	343
110001	301	302	303	304	305	306	307	350
110010	307	308	309	310	311	312	313	357
110011	313	314	315	316	317	318	319	364
110100	319	320	321	322	323	324	325	371
110101	325	326	327	328	329	330	331	378
110110	331	332	333	334	335	336	337	385
110111	337	338	339	340	341	342	343	392
111000	343	344	345	346	347	348	349	399
111001	349	350	351	352	353	354	355	406
111010	355	356	357	358	359	360	361	413
111011	361	362	363	364	365	366	367	420
111100	367	368	369	370	371	372	373	427
111101	373	374	375	376	377	378	379	434
111110	379	380	381	382	383	384	385	441
111111	385	386	387	388	389	390	391	448

Notes:

To use this table, find the desired modulus in the table. Follow the column up to find the A divider programming values. Follow the row to the left to find the M divider programming. Some feedback divisors can be achieved with two or three combinations of divider settings. Any are acceptable for use.

The formula for the effective feedback modulus is: $N = [(M + 1) \cdot 6] + A$

except when A= 0, then: $N = (M + 1) \cdot 7$

Under all circumstances: $A \leq M$

Pin Descriptions - ICS1572-101

PIN#	NAME	DESCRIPTION
13	CLK+	Clock out (non-inverted)
12	CLK–	Clock out (inverted)
8	LOAD	Load output. This output is normally at the CLK frequency divided by N1.
3	XTAL1	Quartz crystal connection 1/external reference frequency input
4	XTAL2	Quartz crystal connection 2
2	AD0	Address/Data Bit 0 (LSB)
19	AD1	Address/Data Bit 1
18	AD2	Address/Data Bit 2
17	AD3	Address/Data Bit 3 (MSB)
9	LD/N2	Divided LOAD output. See text.
5	STROBE	Control for address/data latch
16	VDD	PLL system power (+ 5V. See application diagram.)
15	VDDO	Output stage power (+ 5V)
14	IPRG	Output stage current set
6,7	VSS	Device ground. Both pins must be connected to the same ground potential.
1,10,11,20	NC	Not connected

Pin Descriptions - ICS1572-301

PIN#	NAME	DESCRIPTION
13	CLK+	Clock out (non-inverted)
12	CLK–	Clock out (inverted)
8	LOAD	Load output. This output is normally at the CLK frequency divided by N1.
3	XTAL1	Quartz crystal connection 1/external reference frequency input
4	XTAL2	Quartz crystal connection 2
5	DATCLK	Data Clock (Input)
19	DATA	Serial Register Data (Input)
18	HOLD~	$\overline{\text{HOLD}}$ (Input)
17	BLANK	Blanking (Input). See Text.
9	LD/N2	Divided LOAD output/shift clock. See text.
2	EXTFBK	External feedback connection for PLL (input). See text.
16	VDD	PLL system power (+ 5V. See application diagram.)
15	VDDO	Output stage power (+ 5V)
14	IPRG	Output stage current set
6,7	VSS	Device ground. Both pins must be connected.
1,10,11,20	NC	Not connected

Absolute Maximum Ratings

VDD, VDDO (measured to VSS)..... 7.0V
Digital Inputs..... V_{SS}-0.5 to V_{DD} + 0.5V
Digital Outputs..... V_{SS}-0.5 to V_{DDO} + 0.5V
Ambient Operating Temperature..... -55 to 125 °C
Storage Temperature..... -65 to 150 °C
Junction Temperature..... 175 °C
Soldering Temperature..... 260 °C

Recommended Operating Conditions

VDD, VDDO (measured to VSS)..... 4.75 to 5.25V

Operating Temperature (Ambient)..... 0 to 70 °C

DC Characteristics

TTL-Compatible Inputs
101 Option - (AD0-AD3, STROBE),
301 Option - (DATCLK, DATA, HOLD, BLANK, EXTFBK)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	V_{ih}		2.0	V_{DD}+ 0.5	V
Input Low Voltage	V_{il}		V_{SS}-0.5	0.8	V
Input High Current	I_{ih}	V_{ih} = VDD	-	10	uA
Input Low Current	I_{il}	V_{il} = 0.0	-	150	uA
Input Capacitance	C_{in}		-	8	pF

XTAL1 Input

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	V_{xh}		3.75	V_{DD}+ 0.5	V
Input Low Voltage	V_{xl}		V_{SS}-0.5	1.25	

CLK+ , CLK- Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Differential Output Voltage			0.6	-	V

LOAD, LD/N2 Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output High Voltage (Ioh= 4.0mA)			2.4	-	V
Output Low Voltage (Iol= 8.0mA)			-	0.4	V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
F_{vco}	VCO Frequency (see Note 1)	20		160	MHz
F_{xtal}	Crystal Frequency	5		20	MHz
C_{par}	Crystal Oscillator Loading Capacitance		20		pF
F_{load}	LOAD Frequency			80	MHz
T_{xhi}	XTAL1 High Time (when driven externally)	8			ns
T_{xlo}	XTAL1 Low TIme (when driven externally)	8			ns
T_{high}	Differential Clock Output Duty Cycle (see Note 2)	45		55	%
J_{clk}	Differential Clock Output Cumulative Jitter (see Note 3)		< 0.06		pixel
T_{lock}	PLL Acquire Time (to within 1%)		500		µs
I_{dd}	VDD Supply Current		15	t.b.d.	mA
I_{ddo}	VDDO Supply Current (excluding CLK+ /- termination)		20	t.b.d.	mA
	DIGITAL INPUTS - ICS1572-101				
1	Address Setup Time	10			ns
2	Address Hold Time	10			ns
3	Data Setup Time	10			ns
4	Data Hold Time	10			ns
5	STROBE Pulse Width (T_{hi} or T_{lo})	20			ns
	DIGITAL OUTPUTS - ICS1572-301				
6	DATA/HOLD~ Setup Time	10			ns
7	DATA/HOLD~ Hold Time	10			ns
8	DATCLK Pulse Width (T_{hi} or T_{lo})	20			ns
	PIPELINE DELAY RESET				
9	Reset Activation Time			2*Tclk	ns
10	Reset Duration	4*Tload			ns
11	Restart Delay			2*Tload	ns
12	Restart Matching	-!*Tclk		+ 1.5*Tclk	ns
	DIGITAL OUTPUTS				
13	CLK+ /CLK- Clock Rate			180	MHz
14	LOAD To LD/N2 Skew (Shift Clock Mode)	-2	0	+ 2	ns

Note 1: Use of the post-divider is required for frequencies lower than 20 MHz on CLK+ & CLK- outputs. Use of the post-divider is recommended for output frequencies lower than 65 MHz.

Note 2: Using load circuit of Figure 6. Duty cycle measured at zero crossings of difference voltage between CLK+ and CLK-.

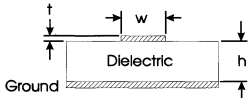
Note 3: Cumulative jitter is defined as the maximum error (in the time domain) of any CLK edge, at any point in time, compared with the equivalent edge generated by an ideal frequency source.
ICS laboratory testing indicates that the typical value shown above can be treated as a maximum jitter specification in virtually all applications. Jitter performance can depend somewhat on circuit board layout, decoupling, and register programming.

Output Circuit Considerations for the ICS1572

Output Circuitry

The dot clock signals CLK and CLK- are typically the highest frequency signals present in the workstation. To minimize problems with EMI, crosstalk, and capacitive loading extra care should be taken in laying out this area of the PC board. The **ICS1572** is packaged in a 0.3"-wide 20-pin SOIC package. This permits the clock generator, crystal, and related components to be laid out in an area the size of a postage stamp. The **ICS1572** should be placed as close as possible to the RAMDAC. The CLK and CLK- pins are running at VHF frequencies; one should minimize the length of PCB trace connecting them to the RAMDAC so that they don't become radiators of RF energy.

At the frequencies that the **ICS1572** is capable of, PC board traces may be long enough to be a significant portion of a wavelength of that frequency. PC traces for CLK and CLK- should be treated as transmission lines, not just interconnecting wires. These lines can take two forms: microstrip and stripline. A microstrip line is shown below:



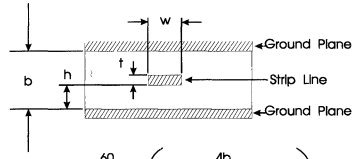
$$Z_o = \frac{87}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98h}{0.8w+t}\right)$$

Dimensions in Inches

Microstrip Line

Essentially, the microstrip is a copper trace on a PCB over a ground plane. Typically, the dielectric is G10 glass epoxy. It differs from a standard PCB trace in that its width is calculated to have a characteristic impedance. To calculate the characteristic impedance of a microstrip line one must know the width and thickness of the trace, and the thickness and dielectric constant of the dielectric. For G10 glass epoxy, the dielectric constant (e_r) is about 5. Propagation delay is strictly a function of dielectric constant. For G10 propagation, delay is calculated to be 1.77 ns/ft.

Stripline is the other form a PCB transmission line can take. A buried trace between ground planes (or between a power plane and a ground plane) is common in multi-layer boards. Attempting to create a workstation design without the use of multi-layer boards would be adventurous to say the least, the issue would more likely be whether to place the interconnect on the surface or between layers. The between layer approach would work better from an EMI standpoint, but would be more difficult to lay out. A stripline is shown below:



$$Z_o = \frac{60}{\sqrt{e_r}} \ln\left(\frac{4b}{0.067\,\pi\, w\left(0.8 + \frac{t}{w}\right)}\right)$$

Dimensions in Inches

Stripline

Using 1oz. copper (0.0015" thick) and 0.040"thickness G10, a 0.010" trace will exhibit a characteristic impedance of 75Ω in a stripline configuration.

Typically, RAMDACS require a V_{ih} of V_{AA}-1.0 Volts as a guaranteed logical "1" and a V_{il} of V_{AA}-1.6 as a guaranteed logical "0". Worst case input capacitance is 10 pF.

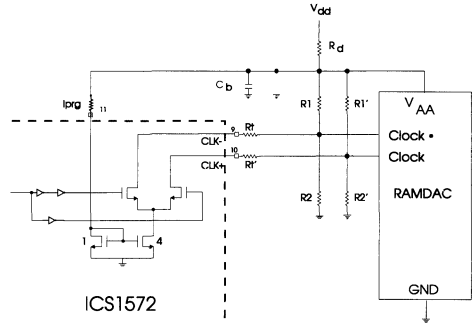
Output circuitry for the **ICS1572** is shown in the following diagram. It consists of a 4/1 current mirror, and two open drain output FETs along with inverting buffers to alternately enable each current-sinking driver. Both CLK and CLK- outputs are connected to the respective CLOCK and CLOCK* inputs of the RAMDAC with transmission lines and terminated in their equivalent impedances by the Thevenin equivalent impedances of R1 and R2 or R1' and R2'.

The **ICS1572** is incapable of sourcing current, so V_{ih} must be set by the ratios of these resistors for each of these lines. R1 and R2 are electrically in parallel from an AC standpoint because V_{dd} is bypassed to ground through bypass-capacitor network C_b. If we picked a target impedance of 75Ω for our transmission line impedance, a value of 91Ω for R1 and R1' and a value of 430Ω for R2 and R2' would yield a Thevinin equivalent characteristic impedance of 75.1W and a Vih value of VAA-.873 Volts, a margin of 0.127Volts. This may be adequate; however, at higher frequencies one must contend with the 10 pF input capacitance of the RAMDAC. Values of 82Ω for R1 and R1' and 820Ω for R2 and R2' would give us a characteristic impedance of 74.5Ω and a V_{ih} value of V_{AA}-.45. With a .55 Volt margin on V_{ih}, this voltage level might be safer.

To set a value for V_{il}, we must determine a value for I_{prg} that will cause the output FET's to sink an appropriate current. We desire V_{il} to be V_{AA}-1.6 or greater. V_{AA}-2 would seem to be a safe value. Setting up a sink current of 25 milliamperes would guarantee this through our 82Ω pull-up resistors. As this is controlled by a 4/1 current mirror, 7 mA into I_{prg} should set this current properly. A 510Ω resistor from V_{dd} to I_{prg} should work fine.

Resistors Rt and Rt' are shown as series terminating resistors at the **ICS1572** end of the transmission lines. These are not required for operation, but may be useful for meeting EMI requirements. Their intent is to interact with the input capacitance of the RAMDAC and the distributed capacitance of the transmission line to soften up rise and fall times and consequently cut some of the high-order harmonic content that is more likely to radiate RF energy. In actual usage they would most likely be 10 to 20Ω resistors or possibly ferrite beads.

C_b is shown as multiple capacitors. Typically, a 22 µF tantalum should be used with separate .1 µF and 220pF capacitors placed as close to the pins as possible. This provides low series inductance capacitors right at the source of high frequency energy. R_d is used to isolate the circuitry from external sources of noise. Five to ten ohms should be adequate.



ICS1572 Output Circuitry

Great care must be used when evaluating high frequency circuits to achieve meaningful results. The 10 pF input capacitance and long ground lead of an ordinary scope probe will make any measurements made with it meaningless. A low capacitance FET probe with a ground connection directly connected to the shield at the tip will be required. A 1GHz bandwidth scope will be barely adequate, try to find a faster unit.

E

User-Programmable Dual High-Performance Clock Generator

Description

The **ICS2572** is a dual-PLL (phase-locked loop) clock generator with differential video outputs specifically designed for high-resolution, high-refresh rate, video applications. The video PLL generates any of 16 pre-programmed frequencies through selection of the address lines **FS0-FS3.** Similarly, the auxiliary PLL can generate any one of four pre-programmed frequencies via the **MS0** & **MS1** lines.

A unique feature of the **ICS2572** is the ability to redefine frequency selections after power-up. This permits complete set-up of the frequency table upon system initialization.

Features

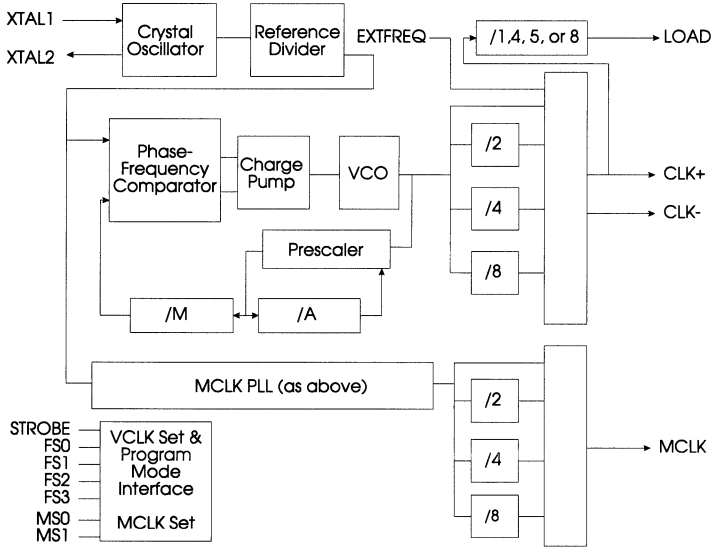
- Advanced ICS monolithic phase-locked loop technology
- Supports high-resolution graphics - differential **CLK** output to 185 MHz
- Divided dotclock output (**LOAD**) available
- Simplified device programming
- Sixteen selectable **VCLK** frequencies (all user re-programmable)
- Four selectable **MCLK** frequencies (all user re-programmable)
- Windows NT compatible

Applications

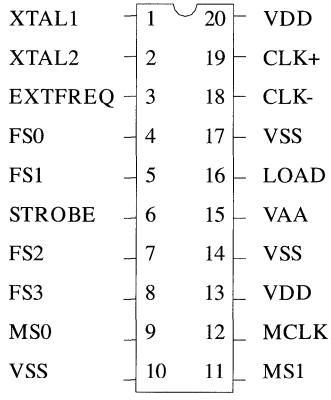
- High end PC/low end workstation graphics designs requiring differential output
- X Terminal graphics

E

Block Diagram



Pin Configuration



Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	XTAL1	A	Quartz crystal connection 1/Reference Frequency Input.
2	XTAL2	A	Quartz crystal connection 2.
3	EXTFREQ	I	External Frequency Input
4	FS0	I	VCLK PLL Frequency Select LSB.
5	FS1	I	VCLK PLL Frequency Select Bit.
7	FS2	I	VCLK PLL Frequency Select Bit.
8	FS3	I	VCLK PLL Frequency Select MSB.
6	STROBE	I	Control for Latch of VCLK Select Bits (FS0-FS3).
9	MS0	I	MCLK PLL Frequency Select LSB.
11	MS1	I	MCLK PLL Frequency Select MSB.
19	CLK+	O	Pixel Clock Output (not-inverted)
18	CLK-	O	Pixel Clock Output (inverted)
16	LOAD	O	Divided Dotclock (/4, 5, or 8)
12	MCLK	O	MCLK Frequency Output
17	RESERVED	-	Must Be Connected to VSS.
10, 14	VSS	P	Device Ground. All pins must be connected.
13, 20	VDD	P	Output Stage Vdd. All pins must be connected.
15	VAA	P	Synthesizer Vdd.

Digital Inputs

The **FS0-FS3** pins and the **STROBE** pin are used to select the desired operating frequency of the **VCLK** output from the 16 pre-programmed / user-programmed selections in the **ICS2572**. These pins are also used to load new frequency data into the registers.

Available configurations for the **STROBE** input include: positive-edge triggered, negative-edge triggered, high-level transparent, and low-level transparent (see Ordering Information).

VCLK Output Frequency Selection

To change the **VCLK** output frequency, simply write the appropriate data to the **ICS2572 FS** inputs. Do not perform any further writes to the device for 50 milliseconds (assumes a 14.318 MHz reference). The synthesizer will output the new frequency programmed into that location after a brief delay (see timeout specifications).

MCLK Output Frequency Selection

The **MS0-MS1** pins are used to directly select the desired operating frequency of the **MCLK** output from the four pre-programmed/user-programmed selections in the **ICS2572.** These inputs are not latched, nor are they involved with memory programming operations.

Programming Mode Selection

A programming sequence is defined as a period of at least 50 milliseconds of no data writes to the **ICS2572** (to clear the shift register) followed by a series of data writes (as shown here):

FS0	FS1	FS2	FS3
X	X	**START** bit (must be "0")	0
X	X	"	1
X	X	**R/W*** control	0
X	X	"	1
X	X	**L0** (location LSB)	0
X	X	"	1
X	X	**L1**	0
X	X	"	1
X	X	**L2**	0
X	X	"	1
X	X	**L3**	0
X	X	"	1
X	X	**L4** (location MSB)	0
X	X	"	1
X	X	**N0** (feedback LSB)	0
X	X	"	1
X	X	**N1**	0
X	X	"	1
X	X	**N2**	0
X	X	"	1
X	X	**N3**	0
X	X	"	1
X	X	**N4**	0
X	X	"	1
X	X	**N5**	0
X	X	"	1
X	X	**N6**	0
X	X	"	1
X	X	**N7** (feedback MSB)	0
X	X	"	1
X	X	**EXTFREQ** bit (selected if "1")	0
X	X	"	1
X	X	**D0** (post-divider LSB)	0
X	X	"	1
X	X	**D1** (post-divider MSB)	0
X	X	"	1
X	X	**STOP1** bit (must be "1"	0
X	X	"	1
X	X	**STOP2** bit (must be "1")	0
X	X	"	1

Observe that the internal shift register is "clocked" by a transition of **FS3** data from "0" to "1". If an extended sequence of register loading is to be performed (such as a power-on initialization sequence), note that it is not necessary to implement the 50 millisecond delay between them. Simply repeat the sequence above as many times as desired. Writes to the **FS** port will not be treated as frequency select data until up to 50 milliseconds have transpired since the last write. Note that **FS0** and **FS1** inputs are "don't care."

Data Description

Location Bits (L0-L4)

The first five bits after the start bit control the frequency location to be re-programmed according to this table. The rightmost bit (the LSB) of the five shown in each selection of the table is the first one sent.

Table 1 - Location Bit Programming

L[4-0]	LOCATION
01100	VCLK Address 12
01101	VCLK Address 13
01110	VCLK Address 14
01111	VCLK Address 15
10010	MCLK Address 2
10011	MCLK Address 3

Feedback Set Bits (N0-N7)

These bits control the feedback divider setting for the location specified. The modulus of the feedback divider will be equal to the value of these bits + 257. The least significant bit (N0) is sent first.

Post-Divider Set Bits (D0-D1)

These bits control the post-divider setting for the location specified according to this table. The least significant bit (D0) is sent first.

Table 2 - Post-Divider Programming

D[1-0]	POST-DIVIDER
00	9
01	4
10	2
11	1

Read/Write* Control Bit

When set to a "0", the **ICS2572** shift register will transfer its contents to the selected memory register at the completion of the programming sequence outlined above.

When this bit is a "1", the selected memory location will be transferred to the shift register to permit a subsequent readback of data. No modification of device memory will be performed.

To readback any location of memory, perform a "dummy" write of data (complete with start and stop bits) to that location but set the **R/W*** control bit (make it "1"). At the end of the sequence (i.e. after the stop bits have been "clocked"), "clocking" of the **FS3** input 11 more times will output the data bits only in the same sequence as above on the FS0 pin.

EXTFREQ Input

The **EXTFREQ** input allows an externally generated frequency to be routed to the **VCLK** output pin under device programming control. If the EXTFREQ bit is set (logic "1") at the selected address location (VCLK addresses only), the frequency applied to the EXTFREQ input will be routed to the **VCLK** output.

Frequency Synthesizer Description

Refer to Figure 1 for a block diagram of the **ICS2572**.

The **ICS2572** generates its output frequencies using phase-locked loop techniques. The phase-locked loop (or PLL) is a closed-loop feedback system that drives the output frequency to be ratiometrically related to the reference frequency provided to the PLL. The phase-frequency detector shown in the block diagram drives the VCO to a frequency that will cause the two inputs to the phase-frequency detector to be matched in frequency and phase. This occurs when:

$$F_{VCO} = F_{XTALI} * \frac{N}{2}$$

where N is the effective modulus of the feedback divider chain and R is the modulus of the reference divider chain.

The feedback divider on the **ICS2572** may be set to any integer value from 257 to 512. This is done by the setting of the **N0-N7** bits. The standard reference divider on the **ICS2572** is fixed to a value of 43 (this may be set to a different value via ROM programming; contact factory). The **ICS2572** is equipped with a post-divider and multiplexer that allows the output frequency range to be scaled down from that of the VCO by a factor of 2, 4, or 8.

Therefore, the VCO frequency range will be from 5.976 to 11.906 (257/43 to 512/43) of the reference frequency. The output frequency range will be from 0.747 to 11.906 times the reference frequency. Worst case accuracy for any desired frequency within that range will be 0.2%.

If a 14.31818 MHz reference is used, the output frequency range would be from 10.697 MHz to 170.486 MHz.

Programming Example

Suppose that we want differential **CLK** output to be 45.723 MHz. We will assume the reference frequency to be 14.31818 MHz.

The VCO frequency range will be 85.565 MHz to 170.486 MHz (5.976 * 14.31818 to 11.906 * 14.31818). We will need to set the post-divider to two to get an output of 45.723 MHz.

The VCO will then need to be programmed to two times 45.723 MHz, or 91.446 MHz. To calculate the required feedback divider modulus we divide the VCO frequency by the reference frequency and multiply by the reference divider:

$$\frac{91.446}{14.31818} * 43 = 274.62$$

which we round off to 275. The exact output frequency will be:

$$\frac{275}{43} * 14.31818 * \frac{1}{2} = 45.784\ \text{MHz}$$

The value of the **N** programming bits may be calculated by subtracting 257 from the desired feedback divider modulus. Thus, the **N** value will be set to 18 (275-257) or 00010010_2. The **D** bit programming is 10_2 (from Table 2).

LOAD Frequency Selection

The LOAD (or divided dotclock) output frequency will be the CLK+ /CLK- frequency divided by 1, 4, 5, or 8. The choice of modulus is a factory option, and is specified along with the ROM frequencies in the VCLK and MCLK tables by way of the two-digit suffix of the part number.

Reference Oscillator & Crystal Selection

The **ICS2572** has on-board circuitry to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in parallel-resonant (also called anti-resonant mode. See the AC Characteristics for the effective capacitive loading to specify when ordering crystals.

Crystals characterized for their series-resonant frequency may also be used with the **ICS2572**. Be aware that the oscillation frequency in circuit will be slightly higher than the frequency that is stamped on the can (typically 0.025-0.05%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the **ICS2572** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

External Reference Sources

An external frequency source may be used as the reference for the VCLK and MCLK PLLs. To implement this, simply connect the reference frequency source to the XTAL1 pin of the **ICS2572**. For best results, insure that the clock edges are as clean and fast as possible and that the input voltage thresholds are not violated.

Power Supply

The **ICS2572** has two **VSS** pins to reduce the effects of package inductance. Both pins are connected to the same potential on the die (the ground bus). BOTH of these pins should connect to the ground plane of the video board as close to the package as is possible.

The **ICS2572** has a **VDD** pin which is the supply of + 5 volt power to all output stages. This pin should be connected to the power plane (or bus) using standard high-frequency decoupling practice. That is, use low-capacitors should have low series inductance and be mounted close to the **ICS2572**.

The **VAA** pin is the power supply for the synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin (as shown in the recommended application circuitry). This will allow the PLL to "track" through power supply fluctuations without visible effects.

Absolute Maximum Ratings

Supply voltage ..... -.5V to + 7V
Logic inputs ..... -.5V to V_{DD} + .5V
Ambient operating temp ..... 0 to 70°C
Storage temperature ..... -85 to + 150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

DC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TTL-Compatible Inputs						
(FS0-3, MS0-1, STROBE):						
Input High Voltage	V_{ih}		2.0		VDD+ 0.5	V
Input Low Voltage	V_{il}		VSS-0.5		0.8	V
Input High Current	I_{ih}				10	uA
Input Low Current	I_{il}				200	uA
Input Capacitance	C_{in}				8	pF
XTAL1:						
Input High Voltage	Vxh		VDD*0.75		VDD+ 0.5	V
Input Low Voltage	Vxl		VSS-0.5		VDD*0.25	V
CLK+ /CLK- Output Sink Current	Isink					mA
High Voltage (Other Outputs)	Voh		4			V
@Ioh= 0.4mA						
Low Voltage (Other Outputs)	Vol				0.4	V
@Iol= 8.0mA						

E

AC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Phase-Locked Loop:						
VCLK, MCLK VCO Frequency	Fvco		100		235	MHz
PLL Acquire Time	Tlock			500		uSec
Crystal Oscillator						
Crystal Frequency Range	Fxtal		5		25	MHz
Parallel Loading Capacitance				20		pF
XTAL1 Minimum High Time	Txhi		8			nSec
XTAL1 Minimum Low Time	Txlo		8			nSec
Power Supplies:						
VDD Supply Current	idd				35	mA
VAA Supply Current	Iaa				10	mA
Digital Outputs:						
CLK+ /CLK- Recommended Termination			50		2	ohms
Other Outputs Rise Time @ Cload= 20pf	Tf				2	nSec
Other Outputs Fall Time @ Cload= 20pf	Tf					nSec

Ordering Information:

ICS2572N-SXX (0.300" DIP Package)
ICS2572M-SXX (0.300" SOIC Package)

where:
"s" denotes strobe option: A - positive level transparent (i.e., 2494 interface compatible)
"xx" denotes default frequencies: B - negative level transparent
C - positive edge triggered
D - negative edge triggered

PATTERN	ICS2572-01			
Reference Divider	43			
VCLK ADDR	FbkDiv/PostDiv - F_{VCLK}(MHz)			
0	300/1- 99.89			
1	378/1 - 125.87			
2	277/1 - 92.24			
3	432/4 - 35.96			
4	302/2 - 50.28			
5	340/2 - 56.61			
6	EXTFREQ-			
7	270/2 - 44.95			
8	405/1 - 134.86			
9	384/4 - 31.97			
A	330/1 - 109.88			
B	481/2 - 80.08			
C	479/4 - 39.87			
D	270/2 - 44.95			
E	450/2 - 74.92			
F	390/2 - 64.93			
MCLK ADDR	FbkDiv/PostDiv - F_{MCLK}			
0	481/4 - 40.04			
1	270/2 - 44.95			
2	396/4 - 32.97			
3	300/2 - 49.95			

ICS

Power Management

Products

In 1991 ICS introduced first silicon on its QuickSaver™ Controller using voltage inflection termination and ReFLEX® charging to fast charge Nickel Cadmium batteries. Today ICS unveils the next generation - QuickSaver™II Controller - for fast and quick charging of Nickel Cadmium and Nickel Hydride batteries.

The QuickSaver™II Controller family uses more sophisticated mixed-signal building blocks to bring cost-effectively the real value of inflection voltage termination and reverse pulse conditioning charge to your designs.

ICS has also introduced a line of load management switches. These switches provide glitch-free handling of the power management shut-down function in the PC environment.

ReFLEX is a registered trademark of Christie Electric Corporation.

ICS Power Management Products

Selection Guide

Product Application	ICS Device Type	Features	Maximum Charge Rate	Package Types	Page
Ni-Cd Battery Charge Processor	ICS1700 NOT RECOMMENDED FOR NEW DESIGN	Integrated Battery Charge Maintenance Controller.	4C	16 Pin DIP 20 Pin SOIC	615
	ICS1700A	Integrated Battery Charge Maintenance Controller.	4C	16 Pin DIP 20 Pin SOIC	617
Ni-Cd Battery Charge Processor NiMH Battery Charge Processor	ICS1702	Enhanced Feature Integrated Battery Charge-Maintenance Control.	4C	16 Pin DIP 20 Pin SOIC	633
Battery Charging and Capacity Measurement IC	ICS1705	SmartBat™ In-the-Pack Data Acquisition and Storage IC for Charge Control and Capacity Measurement.	N/A	8 Pin SOIC	653
Notebook PCs and PDAs Power Switching	AV9304/9504	Quad High-Side Switches 300mΩ R_{DS} On Slow Turn-on for glitch-free Operation.	N/A	16 Pin DIP 16 Pin SOIC	655
	AV9312/9512	Dual High-Side Switches 200mΩ R_{DS} On Slow Turn-on for glitch-free Operation.	N/A	16 Pin DIP 16 Pin SOIC	659

Note: C=Ampere/hour capacity of battery.

SmartBat is a trademark of Integrated Circuit Systems, Inc.

Integrated Circuit Systems, Inc. (ICS) shall be held harmless for any misapplication of this device such as: exceeding the rated specifications of the battery manufacturer; charging batteries other than nickel-cadmium and/or nickel metal hydride type; personal or product damage caused by the charging device, circuit, or system itself; unsafe use, application, and/or manufacture of a charging system using this device.

ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. ICS reserves the right to change or discontinue these products without notice.

Integrated Circuit Systems, Inc.

ICS1700

Data Sheet

QuickSaver™ Controller For Nickel-Cadmium Batteries

NOT RECOMMENDED FOR NEW DESIGN

Features

- A ReFLEX® charging system (1)
- Capable of full charge in 20 minutes*
- Pulsed maintenance mode charge - keeps batteries primed at peak capacity
- Employs sophisticated multiple charge termination methods - as recommended by battery producers
- Reduces internal cell heating
- Reduces internal cell pressure
- LED drivers for charge status, over temperature and some fault conditions
- Multiple charge rate capability
- Microprocessor-based with internal ROM
- Internal safety timer protects against damaging over overcharge

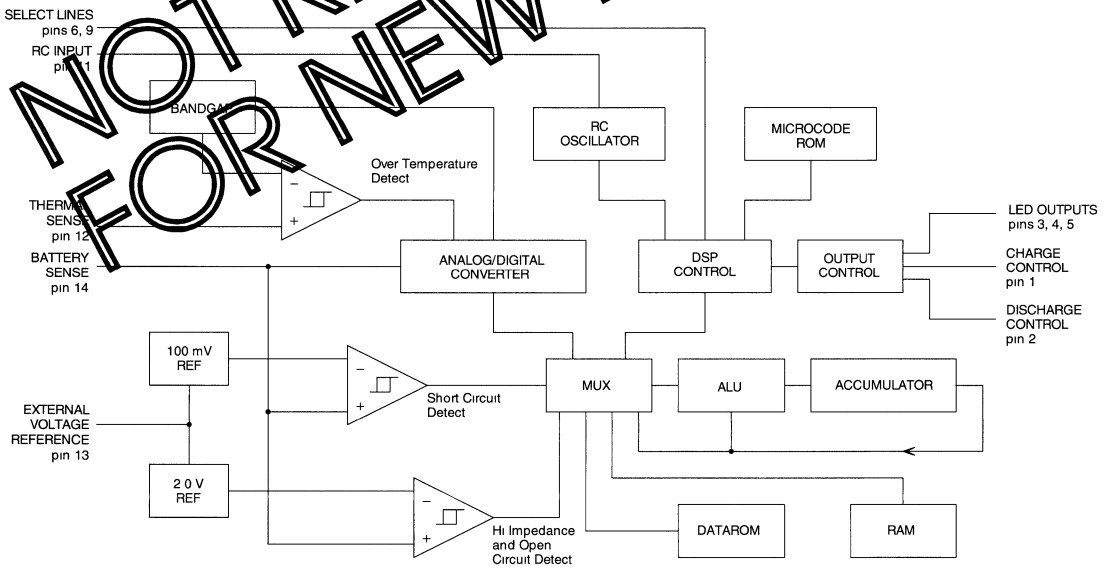
Applications

- AC or DC powered NiCd Battery Chargers
- Notebook and laptop personal computers
- Portable communications equipment
- Portable video and audio equipment
- Portable point-of-sale equipment
- Portable power tools

Description

The ICS1700 QuickSaver™ Controller is an LSI device using CMOS technology specifically designed for the intelligent charging of nickel-cadmium batteries. This device uses the patented ReFLEX® principle of charging and time-derivative charge termination (1). The combination of these two methods can allow the safe charging of nickel-cadmium batteries in as little as 20 minutes.*

Block Diagram



Pin numbers shown are for DIP package

* A 20 minute charge assumes a charging rate of 4C. NOT ALL BATTERIES ARE CAPABLE OF ACCEPTING A 4C CHARGE RATE.
(1) ReFLEX® is the registered trademark of Christie Electric Corporation.

REV2/25/93

F

Integrated Circuit Systems, Inc.

ICS1700A

Advance Information

QuickSaverII™ Controller for Nickel-Cadmium Batteries

General Description

The **ICS1700A** QuickSaverII device is a CMOS monolithic integrated circuit that supervises and controls the charge and charge termination of rechargeable Nickel-cadmium batteries. The **ICS1700A** is a pin-for-pin, functionally compatible replacement device for the original QuickSaver controller ICS1700. The **ICS1700A** employs voltage termination of the fast charge cycle and reverse pulse charging for battery conditioning in all charge stages.

Applications

- AC or DC powered NiCd Battery Chargers
- Notebook and laptop personal computers
- Portable communications equipment
- Portable video and audio equipment
- Portable point-of-sale equipment
- Portable power tools

Features

- A QSII™ charging system
- Capable of full charge in 15 minutes[1]
- Pulse maintenance mode charge - keeps batteries primed at peak capacity
- Accepts a thermal switch or thermistor input
- Four stage charge
  Soft start
  Fast
  Topping
  Maintenance
- Polling mode auto-reset
- Employs several charge termination methods - as recommended by battery producers
- Reduces internal cell heating
- Reduces internal cell pressure
- LED drivers for charge status, over temperature and some fault conditions
- Multiple charge rate capability
- Microprocessor-based with internal ROM
- Internal safety timer protects against damaging over overcharge

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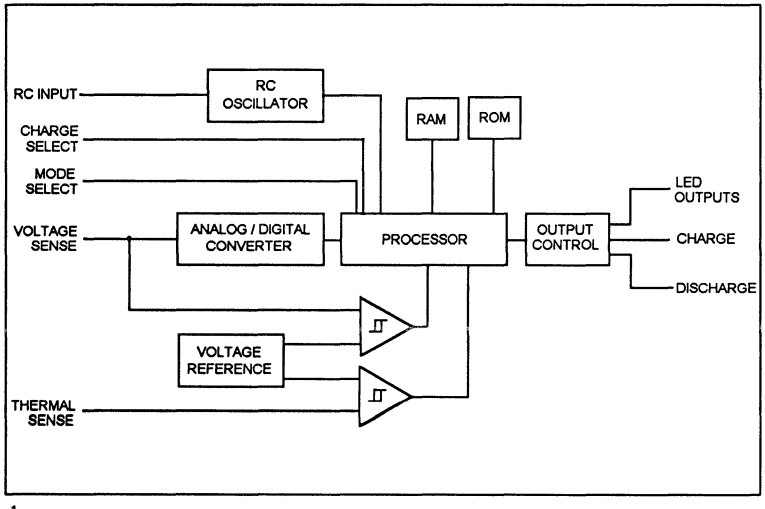
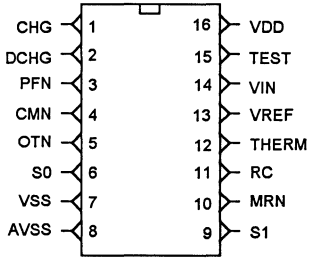
Block Diagram



Pin Configuration



Ordering Information
ICS1700AN
(DIP 16 Pin Package)
ICS1700AM
(SOIC 20 Pin Package)

[1] ICS makes no claim about the capability of any battery to accept a fast charge. ICS strongly recommends that the battery manufacturer be consulted before fast charging.

Table 1: Pin Definitions

PIN NUMBER (DIP)	PIN NUMBER (SO)	PIN NAME	TYPE	DEFINITION
1	1	CHG	OUT	Active high TTL compatible signal turns on external current source providing current to charge battery.
2	2	DCHG	OUT	Active high TTL compatible signal turns on external current sink.
3	3	PFN	OUT	Auto polling and fault indicator. An active low turns on an external indicator to show the device is either polling for a battery or has detected a fault condition.
4	5	CMN	OUT	Charge Mode. An active low turns on external LED, indicating the state of the charge cycle. Continuous low indicates charge in progress, while an alternating low/high indicates maintenance mode.
5	7	OTN	OUT	Over temperature indicator. An active low turns on an external indicator to show the temperature of the battery is too hot to charge.
6	8	S0	IN	Select **0**. Used with S1 signal to program the device for the desired charge rate.
7	9	V_{SS}	PWR	Logic ground.
8	10	LV_{SS}	PWR	Ground pin for output indicator (LED) drivers.
9	11	S1	IN	Select **1**. Used with the S0 signal to program the device for the desired charge rate.
10	12	MRN	IN	Master **RESET** signal initiates the charge sequence.
11	13	RC	IN	Resistor/Capacitor pin sets the frequency of the internal clock.
12	14	THERM	IN	Thermistor or thermal switch input. An internal resistor string establishes the voltage thresholds for hot or cold temperature sensing.
13	16	V_{REF}		No connect.
14	18	VIN	IN	Battery voltage normalized to one cell with external resistor divider.
15	19	TEST	IN	Active high on this pin activates factory test mode. Tie to V_{SS}.
16	20	V_{DD}	PWR	+5 volt supply.

Pins 4, 6, 15, and 17 are "No Connects" in the SO package.

Pin Descriptions

The **ICS1700A** requires some external components to control the clock rate, sense temperature and provide an indicator display. The chip must be interfaced to an external power source that will provide the constant current required to charge a battery pack as well as a circuit that will sink a negative current discharge pulse.

The **ICS1700A** does not control the amount of current flowing into the battery in any way other than turning it on and off. The required current for the selected charge rate must be provided by the user's power source. The external charging circuitry must provide a constant current at the selected charge rate. For example, to charge a 1.2 ampere hour battery at a 30 minute (2C) rate, requires approximately 2.4 amperes of current.

Output Logic Signals: CHG, DCHG Pins

The CHG and DCHG signals are active high, TTL compatible signals. In addition to being TTL compatible, the CMOS outputs are capable of sourcing current which adds flexibility when interfacing to other circuitry. A logic high on the CHG signal indicates that the constant current supply should be activated. A logic high on the DCHG signal indicates that the discharger should be activated.

Care must be taken to control wiring resistance, and the load resistor must be capable of handling this short-duration high-amplitude pulse. If the deep discharge-to-charge mode is selected, the power dissipation of the load resistor must be properly selected to accept the extended length of the discharge pulse.

Indicators: CMN, PFN, OTN Pins

Indicators can be connected to the device to display the charge mode and any fault conditions. The device has four outputs for driving external indicators. These pins are active low. The four indicator outputs have open drains and are designed to be used with LEDs. Each output can sink over 20 mA which requires the use of an external current limiting resistor. The four indicator signals denote fast charge mode, maintenance mode, polling detect mode and out of temperature range condition.

The charge mode (CMN) indicator is activated continuously during the soft start and pulsed fast charge modes. When the controller enters the dual phase maintenance mode, the signal is turned off.

The polling detect (PFN) indicator is on when the **ICS1700A** polls for a battery or a battery fault occurs. The indicator is a warning that charge pulses are appearing at the charging system terminals at regular intervals. When a battery is found, the indicator is deactivated.

The over temperature (OTN) indicator is active whenever the voltage at the temperature sense input falls into a range that indicates to the **ICS1700A** that the attached battery may be too hot to charge. The OTN indicator is also activated with the MMN indicator if the battery is initialized in the cold temperature charge region. The OTN indicator will also activate if the battery becomes cold while a charge is in progress.

Charge Rate Selection: S0, S1 Pins

The S0 and S1 signals must be programmed by the user to inform the **ICS1700A** of the desired charge rate. Since the signals have an internal 100KΩ pull-up, no connection to VDD is required to program a high level. When a low level is desired, the pin should be grounded. A high impedance condition may be accomplished through a resistor divider. The voltage ranges for logic low, high impedance and logic high are detailed in Table 7 Logic Signals. To program the S0 and S1 signals, refer to the Charge Rate List in Table 2.

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Table 2: Charge Rate List

SO	S1	Charge Rate	Charge Time	Topping Charge Pulse Period[2]	Maintenance Charge Pulse Period[2]	Timer
L	L	4C	15 min (1/4 hr)	40 sec	160 sec	18.75 min
L	H	2C	30 min (1/2 hr)	20 sec	80 sec	37.08 min
H	L	1C	60 min (1 hr)	10 sec	40 sec	72.50 min
H	H	C/2	120 min (2 hr)	5 sec	20 sec	141.60 min

[2]Period means the time between pulses.

Master Reset: MRN Pin

The MRN pin is provided to re-program the chip for a new mode or charging sequence. An internal debounce circuit protects against spikes on the line lasting less than 100 ms. This pin has an internal pull-up of 100KΩ. A logic low on the MRN pin must be present for more than 300 ms for a reset to occur. A master reset is required to clear an over temperature condition, clear the device self test or to change charge rates or modes.

Clock Input: RC Pin

The RC pin is used to set the frequency on the internal clock. A 16 KΩ resistor is connected between this pin and VDD. A 100 pF capacitor is connected between this pin and ground. The frequency of the internal clock is 1 MHz.

Temperature Sensing: THERM Pin

The THERM pin requires some thought if a thermistor is going to be used for hot and cold temperature termination. The input impedance of the THERM pin is about 1ΩM typically. The example below works for a 10K @ 25°C thermistor such as the Semitec USA (Ishizuka Electronics Corp.) part # AT103-2. The **ICS1700A** has a 100KΩ pull-up internal to the pin.

For NiCd and NiMH cells, charging should be prevented below 10°C and above 45°C. At 10°C, the resistance of the specified thermistor is nominally 17.96 KΩ. At 45°C, the resistance drops to 4749 Ω. The **ICS1700A** has a voltage threshold for the low temperature (10°C) at 2.4 V, and a voltage threshold for the high temperature (45°C) at 0.98 V All voltages are referred to V_{DD} = 5 V. Using a resistor divider with 10 KΩ for the thermistor and a 24 KΩ fixed resistance, the divider looks like Figure 1 at 25°C:

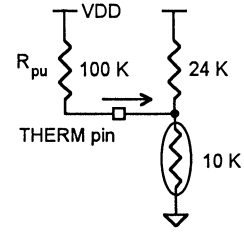

Figure 1: Voltage divider at THERM pin

The voltage at the THERM pin should be about 1.67V at 25°C. Table 4 contains the voltage thresholds and the corresponding temperatures. A short circuit thermal switch threshold of about 0.15V at the THERM pin is available when either an open circuit thermal switch or no temperature sense device is used. If a voltage is below the short circuit thermal switch threshold, the **ICS1700A** assumes the thermal switch is closed to ground and the part is allowed to operate. When the thermal switch opens at high temperature, the pull-up raises the voltage above the high temperature voltage threshold, and the part shuts down. **If no temperature sense device is used, the THERM pin must be grounded.** The short circuit voltage corresponds to a thermistor temperature of about 150°C.

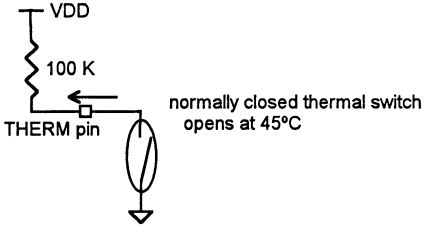

Figure 2: Thermal switch to connection to ground at the THERM pin

Table 4: Temperature Threshold List

Parameter	Voltage	Thermistor Temperature
Open Circuit Thermal Switch Voltage	4.2	-25 °C
Cold Temperature Thermistor Voltage	2.4	10 °C
Hot Temperature Thermistor Voltage	0.98	45 °C
Short Circuit Thermal Switch Voltage	0.150	150 °C

Voltage Input: VIN Pin

The normalized battery voltage is connected to the voltage input (VIN) pin. The input impedance of the VIN pin is about 1 MΩ typically. The battery voltage must be normalized through a resistor divider network to one cell. For example, if the battery consists of six cells in a series, the voltage at the VIN pin must be equal to the total battery voltage divided by six. This can be accomplished with two external resistors. To determine the correct resistor values, count the number of cells to be charged in series. Then choose either R_1 or R_2 and solve for the other resistor using:

$$R1 = R2 \times (\#\ \text{of cells} - 1) \quad \text{or} \quad R2 = R1 / (\#\ \text{of cells} - 1)$$

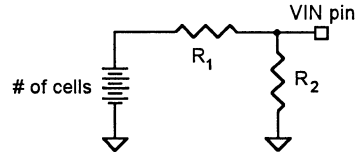

Figure 3: Resistor divider network at the VIN pin

Power: VDD Pin

The device power supply is connected to the VDD pin. The voltage should be + 5 VDC and may be supplied to the part through a regulator which can handle periodic current demands. See Table 6, *DC Characteristics* for more information.

Grounding: VSS, AVSS Pins

There are two ground pins. One pin is used to return the current that the indicator drivers must sink and to handle the internal digital logic. This pin is labeled VSS and should have a direct connection to a solid ground point to avoid inducing ground bounce in the AVSS ground. The AVSS ground connects to the internal analog circuitry. The AVSS pin should also have a direct connection to a solid ground point. Care must be taken to maintain the same potential at both the VSS and AVSS ground point connections.

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Data Tables

Table 5: Absolute Maximum Ratings

Supply Voltage	6.5	V
Logic Input Levels	-0.5 to V_{DD} + 0.5	V
Ambient Operating Temperature	0 to 70	°C
Storage Temperature	-55 to 150	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at the Absolute Maximum Ratings or other conditions not consistent with the characteristics shown in this document is not recommended. Exposure to absolute maximum rating condition for extended periods may affect product reliability.

Table 6: DC Characteristics

V_{DD} = 5.0V; T_{amb} = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Supply Current, Static	I_{DDs}			5		mA
Supply Current, Dynamic	I_{DDd}			10		mA
Upper A/D Converter Range		V_{BG} = 1.23V		2.46		V
Lower A/D Converter Range				0		V
A/D Resolution		8192 clocks (13 bits)		300		µV
High level Source Current, Pull-up	I_{PU}	V_{GS} = 5V		50		µA
Low Level Sink Current, Pull-down	I_{PD}	V_{GS} = 5V		50		µA
High level Source Current, Charge/Discharge Pins	I_{HCD}	V_{GS} = 5V, V_T = 0.95V		43.3		mA
Low Level Sink Current, Charge/Discharge Pins	I_{LCD}	V_{GS} = 5V, V_T = 0.7V		91.0		mA
Low Level Sink Current, Indicator Pins	I_{LL}	V_{GS} = 5V, V_T = 0.7V		122		mA
Input Impedance, VIN pin	Z_{VIN}			1.0		MΩ

Table 7: Logic Signals

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
High Level Input Voltage	V_{IH}		3.5			V
Low Level Input Voltage	V_{IL}		0.8	0.84	0.89	V
High Level Output Voltage	V_{OH}	I_{OH} = 2.0 mA V_{DD} = MIN	2.4			V
Low Level Output Voltage	V_{OL}	I_{OL} = 2.0 mA V_{DD} = MIN			0.4	V
Low Level Output Voltage, Indicator Pins	V_{LL}	I_{OL} = 10 mA	0.102	0.109	0.115	V

Table 8: Timing Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Clock Frequency	f_{CLK}	R = 16KW, C = 100pF		1.0		MHz
Reset/Thermal Switch Debounce		f_{CLK} = 1.0 MHz		300		ms
Charge Pulse Width	t_{CPW}	f_{CLK} = 1.0 MHz		1048		ms
Discharge Pulse Width	t_{DPW}	f_{CLK} = 1.0 MHK		5		ms
Settling Time		f_{CLK} = 1.0 MHz		4		ms
ADC Acquisition Time	t_{ADC}	f_{CLK} = 1.0 MHz		16.38		ms
Cycle Time	t_{cycle}	f_{CLK} = 1.0 MHz		1077		ms
Capacitor Discharge Pulse Width	t_{CDW}	f_{CLK} = 1.0 MHz		5		ms
Capacitor Discharge Pulse Period	t_{CD}	f_{CLK} = 1.0 MHz		100		ms
Polling Detect Pulse Width	t_{PDW}	f_{CLK} = 1.0 MHz		100		ms
Polling Detect Pulse Period	t_{PD}	f_{CLK} = 1.0 MHz		524		ms
Topping Charge Length	t_{TC}	f_{CLK} = 1.0 MHz		2.096		hrs
Maintenance Mode Sample Delay		f_{CLK} = 1.0 MHz		4.19		s
Maintenance Mode Voltage Sample Period		f_{CLK} = 1.0 MHz		4.19		s

Table 9: Voltage Thresholds

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Maintenance Mode Removal Voltage Drop	V_{rem}			0.2		V
Temperature Voltage Difference		THERM		15.9		mV
Thermal Switch Open Circuit		THERM		4.2		V
Thermal Switch Short Circuit		THERM		0.15		V
Cold Thermistor				2.4		V
Hot Thermistor				0.98		V
Capacitor Discharge Short Circuit	V_{SC}			0.2		V

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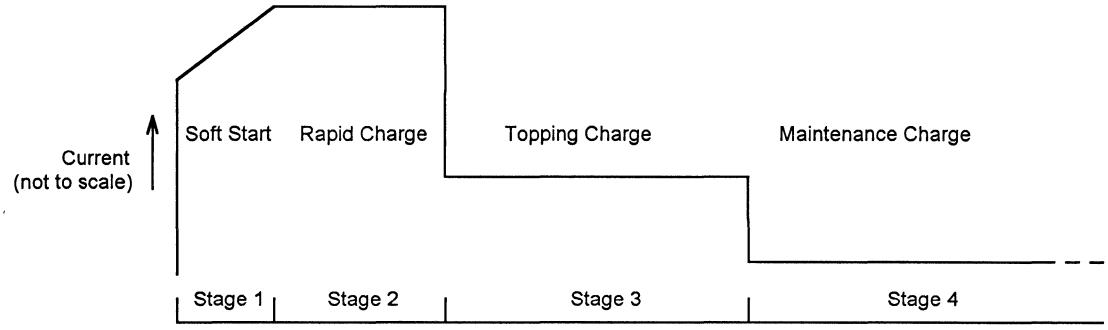

Figure 4: Graphical representation of current levels during the four charging stages

Operation

Charging Stages

The charging sequence consists of four stages. The application of current can be shown graphically in Figure 4. Soft start charge gradually increases current levels up to the user specified fast charge levels during the first few minutes of charge.

The soft start is followed by a high current charge that includes a deep, reverse polarity pulse of short duration, which continues until termination. After termination, a two hour C/10 topping charge followed by a C/40 maintenance charge is applied. Each of these four stages is described next in more detail.

Soft Start Charge

Rechargeable cells can exhibit a high impedance condition while accepting the initial charging current. This high impedance condition can cause a false voltage inflection point at the beginning of the charge cycle which may be misinterpreted as a fully charged battery by the voltage inflection termination method. In the first stage, the soft start routine is intended to ease batteries into a fast charge mode by gradually increasing the current to the fast charge rate. The gradual increase in current alleviates the false inflection point, improves charge efficiency and improves battery life.

Fast Charge

In the second stage, the **ICS1700A** employs a method of applying the charge current in a series of charge and discharge pulses that is intended to increase the charging efficiency. The technique consists of a positive current charging pulse followed by a high current, short duration discharge pulse. The cycle, shown with charge, discharge, rest and data acquisition periods in Figure 5, repeats until the batteries are fully charged.

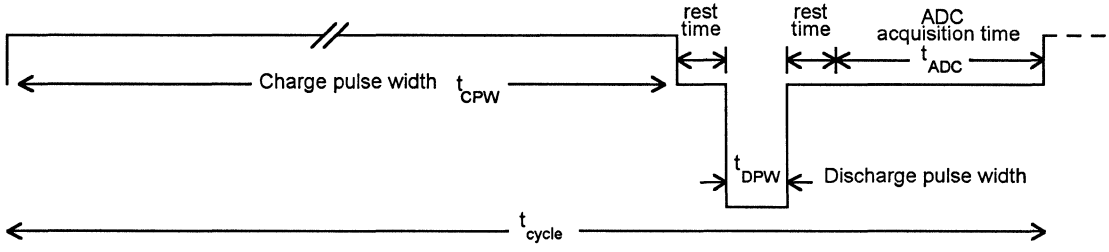

Figure 5: Charge cycle showing charge and discharge current pulses

The amplitude of the charging pulse is determined by the current capability of the power supply, the desired charge rate, the cell capacity and the ability of that cell to accept the charge current. The **ICS1700A** can control nine user-selectable fast charge rates from 15 minutes (4C) to four hours (C/4). Charge pulses occur approximately every second. The charge indicator CMN is the only indicator active during this charge mode. Additional information on charge rates is discussed under the heading, *Charge Rate Selection*.

The discharge current pulse should have an amplitude set to a minimum of -2.5 times the amplitude of the charging current. For example, if the charge current at 4C is 4 amps, then the discharge current should be -10 amps. The energy removed during the discharge pulse is a fixed ratio to the positive charge rate. The cell capacity determines the absolute value of the discharge pulse.

A data acquisition window immediately follows a brief settling time after the discharge pulse. No charge is applied during the settling time or during the acquisition window to allow the cell chemistry to recover. Since no current is flowing, the measured cell voltage is not obscured by any internal or external IR drops or distortions caused by excess plate surface charge. The **ICS1700A** makes one continuous reading of the no-load battery voltage during the entire acquisition window. The voltage that is measured during this window contains less noise and is a more accurate representation of the true state of charge of the battery. Specific timing information is given in Table 8, *Timing Characteristics*.

Topping Charge

A cell that is quickly charged suffers a loss of charge efficiency depending on the ability of the cell to accept charge at high current rates. The third stage is a topping charge designed to ease the cells into a slight overcharge. This ensures a 100% charge to the batteries. Current is applied at a rate low enough to prevent overcharge damage but high enough to ensure a full charge.

When the **ICS1700A** completes the fast charge mode, a timed C/10 charging current is applied for 2 hours (t_{TC}). This charging current consists of the same reverse pulse current technique used during the fast charge mode, however the duty cycle of the pulse sequence has been extended as shown in Figure 6 below. Extending the delay time between charge pulses allows the same charging current used to fast charge the cells so that no changes to the constant current source are necessary. For example, the same charge pulse that occurs every second at a 2C fast charge rate will occur every 20 seconds for a topping charge rate of C/10. The pulse periods for the topping charge at different charge rates is discussed under the heading, *Charge Rate Selection*. The maintenance mode indicator is the only indicator active during this mode.

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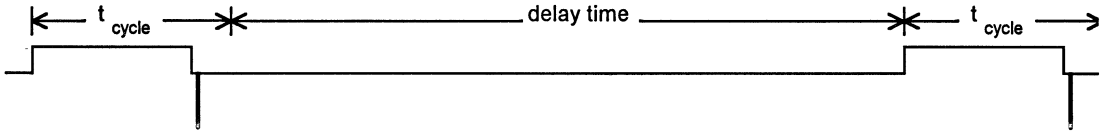

Figure 6: Representative timing diagram for topping and maintenance charges

Maintenance Charge

The maintenance charge is intended to offset the natural self-discharge of NiCd batteries by keeping the cells primed at peak charge. When the topping charge mode is completed, the **ICS1700A** begins the fourth charge stage by extending the duty cycle of the applied current pulses again. The current pulses are decreased to a C/40 rate which will last for as long as a battery voltage is present at the voltage input (VIN) pin, or, if the ten hour timer mode is enabled, until the timer stops the controller. The maintenance mode indicator MMN is the only indicator active during this mode.

Charge Termination Methods

Several charge termination schemes, including voltage inflection (*dV/dt*), negative voltage slope (*-dV/dt*), maximum voltage (V_{max}), maximum temperature (T_{max}) and two overall charge timers are available for use during fast charge. The voltage inflection and negative voltage slope methods may be used with or without the temperature slope and the maximum temperature method. Maximum temperature, maximum voltage and the fast charge timer are always enabled as backup methods. If voltage termination is used, an initial voltage slope check is performed to detect fully charged cells.

Voltage Inflection Termination (dV/dt)

The most distinctive point on the voltage curve of a charging battery in response to a constant current is the peak in the voltage curve that occurs as the cell transitions from charge to overcharge. The voltage peak is characterized by a relatively shallow voltage slope that becomes sharply steeper, flattens out and drops sharply negative. By mathematically calculating the first derivative (*dV/dt*) of the voltage, a second curve can be generated showing the change in voltage with respect to time, as shown in Figure 7.

The slope changes its profile sharply in response to small perturbations in the cell voltage. The slope will reach a maximum just before the actual peak in the cell voltage, as shown in the figure. By calculating a relation between the minimum slope and an empirically derived threshold, the **ICS1700A** can predict the moment of full charge and accurately terminate the applied current before the battery begins to overcharge.

Negative Voltage Slope Termination (-dV/dt)

Cells that are charged at low charge rates, or those cells which are not thoroughly conditioned, or are possessing an unusual cell construction may not have a normal voltage profile. The **ICS1700A** also uses an alternate method of charge termination based on a slight decrease in the voltage slope to stop charge to cells whose voltage profile is very shallow. The negative slope method looks for a flattening of the voltage slope which may indicate a shallow peak in the voltage profile, and enters the maintenance mode if the slope is less than zero for three successive samples. The zero slope point occurs slightly beyond the peak voltage and is shown on the voltage curve graph.

Maximum Voltage Termination (V_{max})

Through the use of an internal bandgap reference set at 1.23VDC, the ICS1700A uses two comparators in front of the analog-to-digital converter to determine the presence of a battery. Provided that the system designer has maintained a 2.0V/cell terminal voltage, the chip will terminate the charge when it detects an open circuit voltage above 2.0V/cell. (*Maximum voltage should not be used as the only charge termination method, especially when fast charging any battery!*)

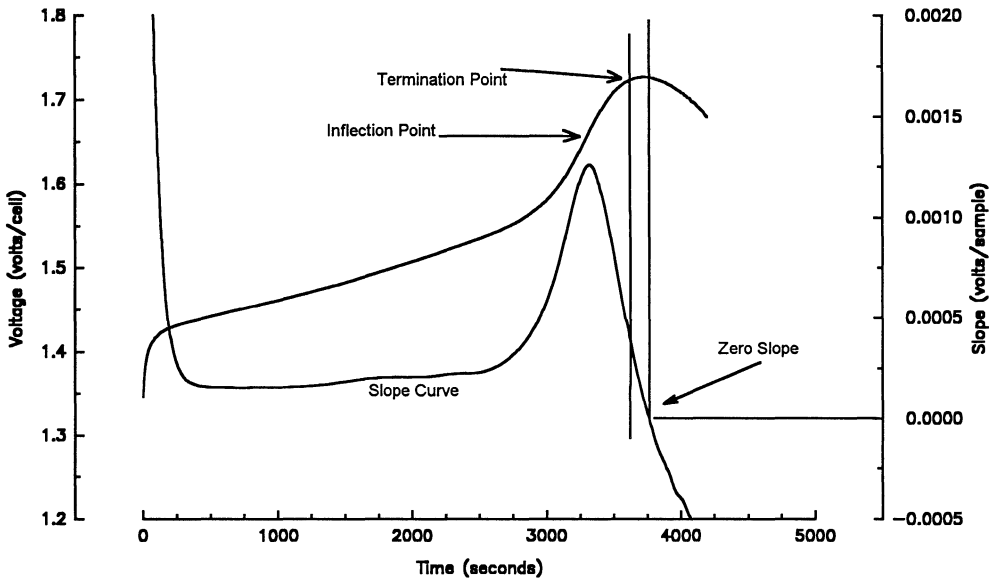

Figure 7: Voltage and slope curves vs. charge time

Maximum Temperature Termination (T_{max})
Maximum temperature can be sensed using either a thermistor or a thermal switch. The maximum temperature termination can also be bypassed if desired, although it is strongly recommended that some form of temperature termination be used. The hardware used to sense maximum temperature levels is always enabled, and can only be disabled by shorting the temperature sense pin (THERM) to ground. Maximum temperature termination cannot be disabled if temperature slope termination is used.

If a thermistor is used, the **ICS1700A** has two voltage thresholds which sense whether the battery is too hot or too cold to charge. The thresholds are designed for a typical 10 KΩ @ 25°C NTC thermistor. These voltage levels are sensed across the thermistor. As temperature increases, the voltage across the thermistor will drop. At a temperature of 45°C, the **ICS1700A** assumes the battery has gotten hot and charge is terminated. Refer to Table 4 for voltage indications at several temperatures.

If a thermal switch is used, a 45°C open circuit switch is recommended. If the switch is closed to ground (signifying the battery is less than 45°C), the chip will operate since the voltage at the THERM pin will be at ground. If the switch opens at 45°C, an internal pull-up will engage and the **ICS1700A** will fault to over temperature since the voltage will be at V_{DD}.

If a battery is determined to be hot, either through an open thermal switch or a thermistor threshold, the over temperature (OTN) indicator will turn on. The device must be reset once the over temperature condition has cleared to start the charge sequence. The appropriate indicators for the particular charge mode will light when the temperature is normal and charging can begin.

The section Mode Selection, *Cold Temperature Charging* has information on the cold temperature region. See the section under *Temperature Sensing* for more information regarding the use of a thermistor or a thermal switch at the temperature sense pin. Table 4 in that section lists voltages and corresponding temperatures.

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Fast Charge Timer Termination[3]

The **ICS1700A** also uses a timer to shut off the fast charge if the device goes beyond a safe charging time limit. These times are programmed into the chip, and are listed below in Table 10. If the device is used at a charge rate other than the ones allowed, care must be taken to avoid premature termination due to the timer cutoff. This *deadman* timer cannot be disabled.

Initial Slope Check

The initial slope check is a test to detect fully charged batteries before a long term high current charge is applied. After that period of time, the initial slope value is calculated and is tested for a negative value. If the initial slope is negative, the voltage must be decreasing over the sampling period and the battery is assumed to be fully charged. The **ICS1700A** will then enter the maintenance mode. If the slope is positive, the **ICS1700A** stores the slope and continues charging.

This check is always active when voltage slope termination is enabled.

Table 10: Fast Charge Timer List

Charge Time (minutes)	Charge Rate	Timer Cutoff (minutes)
15	4C	18.75
30	2C	37.08
45	1.3C	55.00
60	1C	72.50
90	C/1.5	107.5
120	C/2	141.6
150	C/2.5	209.89
180	C/3	241.90
240	C/4	273.14

Battery Detection and Removal

Polling Detect

The polling/fault detect (PFN) indicator is on when the **ICS1700A** is polling for a battery or has shut down due to a fault condition. When polling, the indicator is a warning that the charger is still active and that charge pulses are occuring at the charging system terminals consistent with the user selected charge rate. The **ICS1700A** enters this mode by applying a charge pulse for a 100 ms (τpd) period. During the pulse, the **ICS1700A** monitors the voltage of the input pin to determine the voltage relative to the open circuit voltage at the terminals. If a battery is present, its voltage will be below the open circuit voltage while charge is applied, and a normal charging sequence will begin. If a battery is not present, the voltage will be at or above the open circuit voltage reference and the part will eventually shut off.

The 100 ms pulse will recur over a 524 ms (τpd) period incorporating 20 individual pulse samples (approximately 10 seconds). After this period, the part will shut down and must be reset through the master reset (MRN) pin. The fault indication will occur if a battery is present and a fault occurs. In that case, the **ICS1700A** will stop the charging sequence upon detection of the fault.

Out of Temperature Range

The out of temperature range (OTN) indicator is active whenever the voltage at the temperature sense input falls into the range that indicates to the **ICS1700A** that the attached battery may be too hot to charge. The OTN indicator is active also if the battery is cold during the initialization of charge or becomes cold while charging is in progress. This condition, while indicated, does not terminate the charge sequence and is not a fault condition, per se.

[3] When the fast charge timer shuts off the fast charge operation, the ICS1700A will go into maintenance mode charge and the maintenance mode indicator will be on at this time.

Application Information

FEATURE	BENEFIT TO USER
Inflection Termination	**Reduces internal heat and pressure, and extends the batteries "working" life.**
Reverse Pulse	**Eliminates the need to discharge before charge; available in all charge modes.**
Auto Polling	**Automatic search for battery presence at the terminals.**
Temperature Input	**Thermistor or thermal switch high temperature shut down.**
Four Stage Charge	**Soft start and topping modes in addition to fast and maintenance mode charge.**
Safety Timers	**A failsafe deadman timer.**

The **ICS1700A** is a pin-for-pin compatible version of the original QuickSaver™ ICS1700. In this version, ICS has modified the internal device building blocks to be more robust. The **ICS1700A** features a 13 bit *delta-sigma* analog-to-digital converter, (the same converter designed into the **ICS1700A**), and a wider data path to improve the data acquisition aspects of the device.

The **ICS1700A** includes three new features not found on the ICS1700.

1) Battery temperature sensing for over temperature charge termination through a thermistor or a thermal switch. The present device only accepts a thermal switch input.

2) Four stage charging that prevents early charge termination when the battery is completely discharged. A two-hour C/10 topping mode to ease the battery into 100% full charge.

3) Auto polling at the battery terminals applies a charge pulse then monitors the voltage input and compares this to the open circuit voltage to determine if the battery is present. If the battery has been temporarily removed and is re-inserted or contact with the battery is broken momentarily, the charging sequence will re-start automatically.

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Application Information

Figure 8 shows a typical application using the **ICS1700A**. R1 and R2 are selected to scale the battery voltage to 1 cell. The following table shows some typical values. Additional information is available under Pin Descriptions-*Voltage Input: VIN Pin.*

CELLS	R1	R2
1	Short	Open
2	2K	2K
3	2K	1K
4	3K	1K
5	12K	3K
6	10K	2K
7	12K	2K
8	9.1K	1.3K

It is very important that care be taken to minimize noise coupling and ground bounce. In addition, wiring resistance and connectors can add significant amounts of resistance to the charge and discharge circuits. Be sure to connect the ground side of the discharge transistor to the negative lead of the battery as close to the battery as possible. This will reduce ground bounce and coupled noise.

When designing a printed circuit board, make sure ground and power traces are heavy and bypass capacitors are used close to the chip. Use a separate ground system for the discharge current to prevent high circulating currents from disturbing normal operation.

A constant current source should be used to provide charging current to the battery. Resistors may be used if the current does not vary more than 20%.

Additional application information will be provided in the final version of the data sheet, and as part of a series of regular technical updates.

Notes: 1) Value of resistor determined by discharge current and capacity of battery pack.

2) Device must be logic level compatible.

3) Negative battery terminal and DC return should be connected at one point.

4) A thermal switch or thermistor can be used with the ICS1700A. Refer to the application note for the equivalent circuit diagram when using a thermistor.

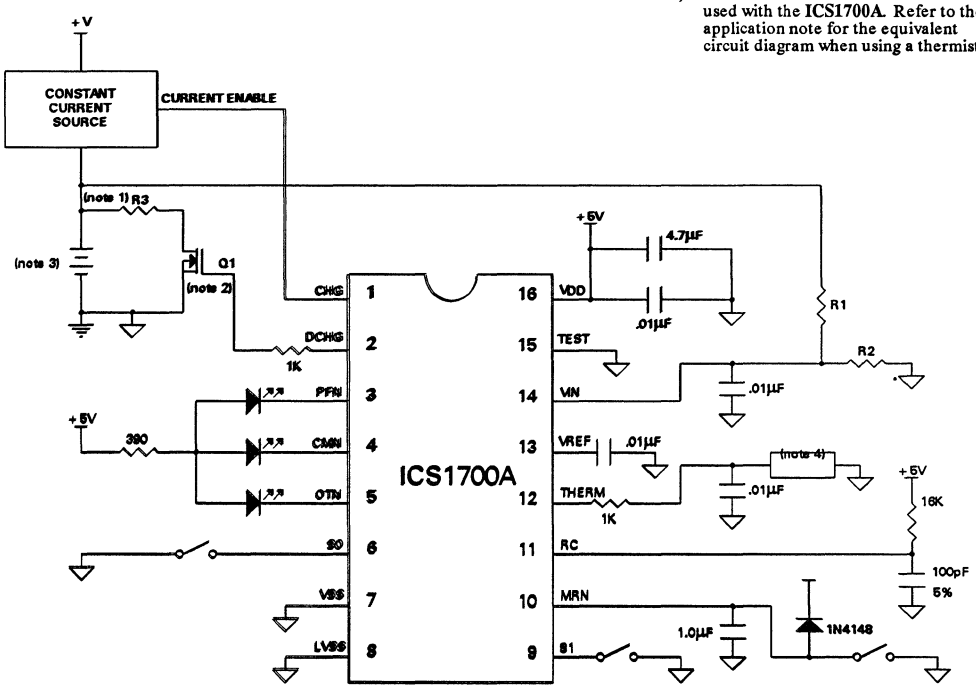

Figure 8: Functional Diagram

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Integrated Circuit Systems, Inc.

ICS1702

Advance Information

QuickSaverII™ Controller for Fast Charge and Conditioning of NiCd and NiMH Batteries

General Description

The **ICS1702** QuickSaver II device is a CMOS monolithic integrated circuit that supervises and controls the charge and charge termination of rechargeable Nickel-Cadmium, and Nickel-Metal Hydride batteries. The **ICS1702** employs voltage and temperature termination methods and pulse charging for battery conditioning.

Applications

- AC or DC powered NiCd and/or NiMH battery chargers
- Cellular telephone
- Portable PC
- Remote data acquisition
- Two-way radio
- Portable video equipment
- Portable power tools
- Portable audio equipment

Features

- Patent pending QS II charge algorithm
- Voltage inflection termination
- Temperature slope termination
- Reverse pulse conditioning
  in charge mode
  in maintenance mode
  in condition mode
- Four stage charge
  Soft start
  Fast
  Topping
  Maintenance
- Fast charging
  15 minutes for NiCd[1]
  1 hour for NiMH[1]
- 7 charge terminations
- 9 programmable charge rates
- Cold battery condition charge
- Hot battery charge fault
- Polling mode Auto-Reset
- System test through QS II controller
- Full condition cycle to 0.8V/cell
- Adjustable open circuit reference

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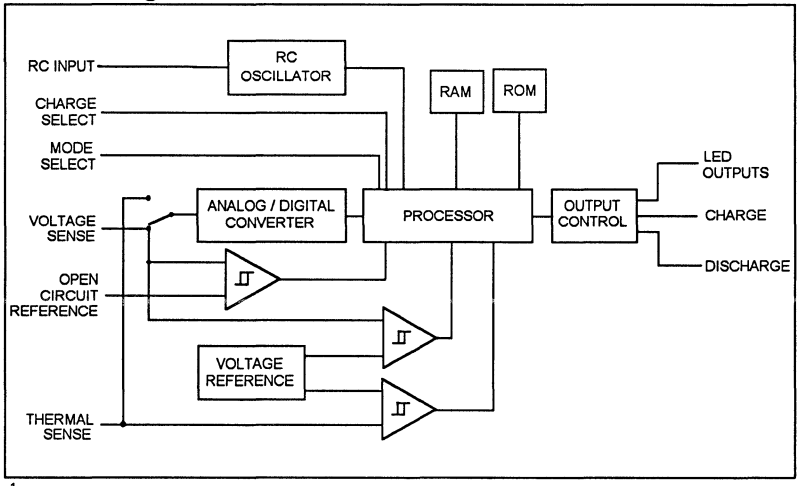
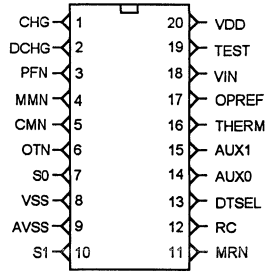
Block Diagram



Pin Configuration



Ordering Information
ICS1702N (20 Pin DIP Package)
ICS1702M (20 Pin SOIC Package)
Temp. Range = 0°C to + 70°C

[1] ICS makes no claim about the capability of any battery (NiCd or NiMH) to accept a fast charge. ICS strongly recommends that the battery manufacturer be consulted before fast charging.

Table 1: Pin Definitions

PIN NUMBER	PIN NAME	TYPE	DEFINITION
1	CHG	OUT	Active high TTL compatible signal available to turn on an external current source to provide current to charge the battery.
2	DCHG	OUT	Active high TTL compatible signal available to turn on a discharge circuit.
3	PFN	OUT	Polling detect indicator. An active low turns on an external indicator to show the device is in the polling detect mode and is polling for the presence of the battery.
4	MMN	OUT	Maintenance mode indicator. An active low turns on an external indicator showing the battery is in either a topping charge mode, maintenance mode or a condition mode. This signal is also applied with the over temperature indicator when the battery is in a cold charge mode.
5	CMN	OUT	Charge mode indicator. An active low turns on an external indicator, indicating the device is in either a soft start or a fast charge mode.
6	OTN	OUT	Out of temperature range indicator. An active low turns on an external indicator showing the battery to be out of the normal fast charge temperature range.
7	S0	IN	Tristate input used with the S1 pin to program the device for the desired charge rate.
8	VSS	PWR	Logic and display indicator ground.
9	AVSS	PWR	Analog ground.
10	S1	IN	Tristate input used with the S0 pin to program the device for the desired charge rate.
11	MRN	IN	Master reset signal. A low to high transition initiates a device reset.
12	RC	IN	A resistor and capacitor sets the frequency of the internal clock.
13	DTSEL	IN	Selects temperature slope and/or voltage slope termination.
14	AUX0	IN	Tristate input used with the AUX1 pin to program the device for a special charge mode or a device self-test mode.
15	AUX1	IN	Tristate input used with the AUX0 pin to program the device for a special charge mode or a device self-test mode.
16	THERM	IN	Thermistor or thermal switch input. An internal resistor string establishes voltage thresholds for hot or cold temperature sensing.
17	OPREF	IN	Open circuit reference. A resistor divider on this pin sets the open circuit voltage reference used to detect the presence of the battery.
18	VIN	IN	Battery terminal voltage normalized to one cell with a resistor divider.
19	TEST	n/c	No Connect (Engineering test mode input).
20	VDD	PWR	Device supply = +5.0 VDC ± 0.5 Vdc.

Pin Descriptions

The **ICS1702** requires some external components to control the clock rate, sense temperature and provide an indicator display. The chip must be interfaced to an external power source that will provide the constant current required to charge a battery pack as well as a circuit that will sink a negative current discharge pulse.

The **ICS1702** does not control the amount of current flowing into the battery in any way other than turning it on and off. The required current for the selected charge rate must be provided by the user's power source. The external charging circuitry must provide a constant current at the selected charge rate. For example, to charge a 1.2 ampere hour battery at a 30 minute (2C) rate, requires approximately 2.4 amperes of current.

Output Logic Signals: CHG, DCHG Pins

The CHG and DCHG signals are active high, TTL compatible signals. In addition to being TTL compatible, the CMOS outputs are capable of sourcing current which adds flexibility when interfacing to other circuitry. A logic high on the CHG signal indicates that the constant current supply should be activated. A logic high on the DCHG signal indicates that the discharger should be activated.

Care must be taken to control wiring resistance, and the load resistor must be capable of handling this short-duration high-amplitude pulse. If the deep discharge-to-charge mode is selected, the power dissipation of the load resistor must be properly selected to accept the extended length of the discharge pulse.

Indicators: CMN, MMN, PFN, OTN Pins

Indicators can be connected to the device to display the charge mode and any fault conditions. The device has four outputs for driving external indicators. These pins are active low. The four indicator outputs have open drains and are designed to be used with LEDs. Each output can sink over 20 mA which requires the use of an external current limiting resistor. The four indicator signals denote fast charge mode, maintenance mode, polling detect mode and out of temperature range condition.

The charge mode (CMN) indicator is activated continuously during the soft start and pulsed fast charge modes. When the controller enters the dual phase maintenance mode, the signal is turned off.

The maintenance mode (MMN) indicator is on when the **ICS1702** is in either the topping charge, maintenance charge, direct maintenance mode, or the condition mode. The MMN indicator is also lit in conjunction with the OTN indicator when cold temperature charging is in progress. The maintenance mode indicator pulses at a 524 ms rate when the **ICS1702** is controlling the discharge portion of the discharge-to-charge mode.

The polling detect (PFN) indicator is on when the **ICS1702** polls for a battery. The indicator is a warning that charge pulses are appearing at the charging system terminals at regular intervals. When a battery is found, the indicator is deactivated.

The over temperature (OTN) indicator is active whenever the voltage at the temperature sense input falls into a range that indicates to the **ICS1702** that the attached battery may be too hot to charge. The OTN indicator is also activated with the MMN indicator if the battery is initialized in the cold temperature charge region. The OTN indicator will also activate if the battery becomes cold while a charge is in progress.

Charge Rate Selection: S0, S1 Pins

The S0 and S1 signals must be programmed by the user to inform the **ICS1702** of the desired charge rate. Since the signals have an internal 100KΩ pull-up, no connection to V_{DD} is required to program a high level. When a low level is desired, the pin should be grounded. A high impedance condition may be accomplished through a resistor divider. The voltage ranges for logic low, high impedance and logic high are detailed in Table 8 *Logic Signals*. To program the S0 and S1 signals, refer to the *Charge Rate List* in Table 2.

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Table 2: Charge Rate List

SO	S1	Charge Rate	Charge Time	Topping Charge Pulse Period[2]	Maintenance Charge Pulse Period[2]	Timer
L	L	4C	15 min (1/4 hr)	40 sec	160 sec	18.75 min
L	H	2C	30 min (1/2 hr)	20 sec	80 sec	37.08 min
L	Z	1.3C	45 min (3/4 hr)	13 sec	53 sec	55.00 min
H	L	1C	60 min (1 hr)	10 sec	40 sec	72.50 min
H	Z	C/1.5	90 Min (1 1/2 hr)	7 sec	27 sec	107.50 min
H	H	C/2	120 min (2 hr)	5 sec	20 sec	141.60 min
Z	L	C/2.5	150 min (2 1/2 hr)	4 sec	16 sec	209.87 min
Z	Z	C/3	180 min (3 hr)	3 sec	13 sec	241.90 min
Z	H	C/4	240 (4 hr)	2 sec	10 sec	273.13 min

Mode Selection: AUX0, AUX1 Pins

The AUX0 and AUX1 signals must be programmed by the user to inform the **ICS1702** of the desired mode. Since the signals have an internal pull-up of 100KΩ no connection to V_{DD} is required to program a high level. When a low level is desired, the pin should be grounded.

High impedance may be accomplished through a resistor divider. The voltage ranges for logic low, high impedance and logic high are detailed in Table 8, *Logic Signals*. To program the AUX0 and AUX1 signals, refer to the Mode Select List in Table 3.

Table 3: Mode Select List

AUX0	AUX1	Mode Selected	Mode Operation
L	L	Direct Maintenance	Indefinite C/40 maintenance mode
L	Z	Data Output	Outputs data in a serial self-clocking format[3]
L	H	Device Self-Test	Device self-test for embedded applications
Z	Z	Ten Hour Timer	Limits total charge including the maintenance charge to 10 hours
H	L	Deep Discharge to Charge	1C battery discharge followed by full charge
H	Z	Condition	Timed C/10 topping charge followed by C/40 maintenance charge
H	H	Fast Charge	Normal operation

[2] Period means the time between pulses
[3] Data output help disks will be available from the factory in 1stQtr 1994

Master Reset: MRN Pin

The MRN pin is provided to re-program the chip for a new mode or charging sequence. An internal debounce circuit protects against spikes on the line lasting less than 100 ms. This pin has an internal pull-up of 100KΩ. A logic low on the MRN pin must be present for more than 131 ms for a reset to occur. A master reset is required to clear an over temperature condition, clear the device self test or to change charge rates or modes.

Clock Input: RC Pin

The RC pin is used to set the frequency on the internal clock. A 16 KΩ resistor is connected between this pin and VDD. A 100 pF capacitor is connected between this pin and ground. The frequency of the internal clock is 1 MHz.

Temperature Sensing: THERM Pin

The THERM pin requires some thought if a thermistor is going to be used for hot and cold temperature termination. The input impedance of the THERM pin is about 1ΩM typically. The example below works for a 10K @ 25°C thermistor such as the Semitec USA (Ishizuka Electronics Corp.) part # AT103-2. The **ICS1702** has a 100KΩ pull-up internal to the pin.

For NiCd and NiMH cells, charging should be prevented below 10°C and above 45°C. At 10°C, the resistance of the specified thermistor is nominally 17.96 KΩ. At 45°C, the resistance drops to 4749 Ω. The **ICS1702** has a voltage threshold for the low temperature (10°C) at 2.4 V, and a voltage threshold for the high temperature (45°C) at 0.98 V All voltages are referred to V_{DD} = 5 V. Using a resistor divider with 10 KΩ for the thermistor and a 24 KΩ fixed resistance, the divider looks like Figure 1 at 25°C:

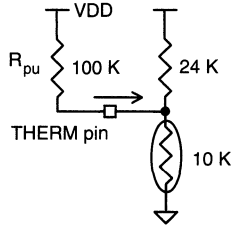

Figure 1: Voltage divider at THERM pin

The voltage at the THERM pin should be about 1.67V at 25°C. Table 4 contains the voltage thresholds and the corresponding temperatures. A short circuit thermal switch threshold of about 0.15V at the THERM pin is available when either an open circuit thermal switch or no temperature sense device is used. If a voltage is below the short circuit thermal switch threshold, the **ICS1702** assumes the thermal switch is closed to ground and the part is allowed to operate. When the thermal switch opens at high temperature, the pull-up raises the voltage above the high temperature voltage threshold, and the part shuts down. **If no temperature sense device is used, the THERM pin must be grounded**. The short circuit voltage corresponds to a thermistor temperature of about 150°C.

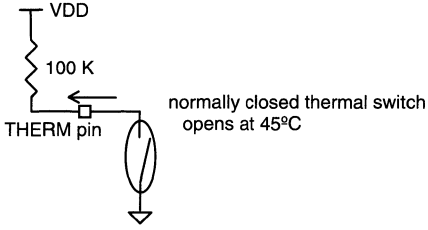

Figure 2: Thermal switch to connection to ground at the THERM pin

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Table 4: Temperature Threshold List

Parameter	Voltage	Thermistor Temperature
Open Circuit Thermal Switch Voltage	4.2	-25 °C
Cold Temperature Thermistor Voltage	2.4	10 °C
Hot Temperature Thermistor Voltage	0.98	45 °C
Short Circuit Thermal Switch Voltage	0.150	150 °C

Termination Select: DTSEL Pin

The **ICS1702** has the capability to support either temperature termination, voltage termination or both methods simultaneously. A pull-down at the DTSEL pad enables voltage termination only and is the default condition. Tying the pin to V_{DD} enables both temperature (*dT/dt*) and voltage (*dVdt*) termination methods. Temperature slope termination as the only method is enabled by tying the DTSEL pin to the CMN indicator. A transition of the CMN indicator and the DTSEL pin tied to CMN will set the temperature slope termination method *only* in the **ICS1702**. See Table 5 for the DTSEL logic conditions.

Table 5: Termination Select List

Tie DTSEL Pin to . .	Condition	Result
No Connect (pull-down at pad)	Low (default)	Voltage slope termination only (*dV/dt, -dV/dt*)
dV/dt, -dVdt)VDD	High	Voltage and temperature termination (*dV/dt, -dV/dt, dT/dt*)
CMN	High to Low	Temperature slope termination only (*dT/dt*)
Note: Maximum temperature, maximum voltage (open circuit detection) and fast charge timer termination methods are always enabled. Refer to specific sections for information on disabling the max temperature and max voltage methods.		

Open Circuit Reference: OPREF Pin

The open circuit reference (OPREF) pin requires a voltage divider to establish the open circuit voltage reference. To be effective, the open circuit reference should be 200 to 300 mV higher than the maximum expected charging voltage. The maximum voltage that can be read by the analog to digital converter at the voltage input pin is about 2.4V, so the open circuit reference voltage should be set below that point. The maximum voltage allowed at the OPREF pin is V_{DD}.

Voltage Input: VIN Pin

The normalized battery voltage is connected to the voltage input (VIN) pin. The input impedance of the VIN pin is about 1 MΩ typically. The battery voltage must be normalized through a resistor divider network to one cell. For example, if the battery consists of six cells in a series, the voltage at the VIN pin must be equal to the total battery voltage divided by six. This can be accomplished with two external resistors. To determine the correct resistor values, count the number of cells to be charged in series. Then choose either R_1 or R_2 and solve for the other resistor using:

$R1 = R2 \times (\#\ \text{of cells} - 1)$ or $R2 = R1 / (\#\ \text{of cells} - 1)$

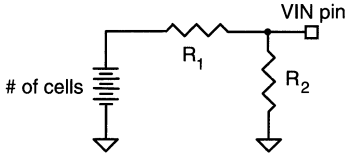

Figure 3: Resistor divider network at the VIN pin

Power: VDD Pin

The device power supply is connected to the VDD pin. The voltage should be + 5 VDC and may be supplied to the part through a regulator which can handle periodic current demands. See Table 7, *DC Characteristics* for more information.

Grounding: VSS, AVSS Pins

There are two ground pins. One pin is used to return the current that the indicator drivers must sink and to handle the internal digital logic. This pin is labeled VSS and should have a direct connection to a solid ground point to avoid inducing ground bounce in the AVSS ground. The AVSS ground connects to the internal analog circuitry. The AVSS pin should also have a direct connection to a solid ground point. Care must be taken to maintain the same potential at both the VSS and AVSS ground point connections.

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Data Tables

Table 6: Absolute Maximum Ratings

Supply Voltage	6.5	V
Logic Input Levels	-0.5 to V_{DD} + 0.5	V
Ambient Operating Temperature	0 to 70	℃
Storage Temperature	-55 to 150	℃

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at the Absolute Maximum Ratings or other conditions not consistent with the characteristics shown in this document is not recommended. Exposure to absolute maximum rating condition for extended periods may affect product reliability.

Table 7: DC Characteristics

V_{DD}= 5.0V; T_{amb}= 25℃

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Supply Current, Static	I_{DDs}			5		mA
Supply Current, Dynamic	I_{DDd}			10		mA
Upper A/D Converter Range		V_{BG}= 1.23V		2.46		V
Lower A/D Converter Range				0		V
A/D Resolution		8192 clocks (13 bits)		300		µV
High level Source Current, Pull-up	I_{PU}	V_{GS}= 5V		50		µA
Low Level Sink Current, Pull-down	I_{PD}	V_{GS}= 5V		50		µA
High level Source Current, Charge/Discharge Pins	I_{HCD}	V_{GS}= 5V, V_T= 0.95V		43.3		mA
Low Level Sink Current, Charge/Discharge Pins	I_{LCD}	V_{GS}= 5V, V_T= 0.7V		91.0		mA
Low Level Sink Current, Indicator Pins	I_{LL}	V_{GS}= 5V, V_T= 0.7V		122		mA
Input Impedance, VIN pin	Z_{VIN}			1.0		MΩ

Table 8: Logic Signals

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
High Lev el Input Voltage	V_{IH}		3.5			V
Low Level Input Voltage	V_{IL}		0.8	0.84	0.89	V
High Level Output Voltage	V_{OH}	I_{OH}= 2.0 mA V_{DD}= MIN	2.4			V
Low Level Output Voltage	V_{OL}	I_{OL}= 2.0 mA V_{DD}= MIN			0.4	V
Low Level Output Voltage, Indicator Pins	V_{LL}	I_{OL}= 10 mA	0.102	0.109	0.115	V
Low Level Tristate Input Voltage	V_{ZL}	S0, S1, AUX0, AUX1	0	0.4	0.82	V
High Impedance Level Tristate Input Voltage	V_{ZZ}	S0, S1, AUX0, AUX1	0.82	2.5	4.1	V
High Level Tristate Input Voltage	V_{ZH}	S0, S1, AUX0, AUX1	4.1	5	5	V

Table 9: Timing Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Clock Frequency	f_{CLK}	R= 16KW, C= 100pF		1.0		MHz
Reset/Thermal Switch Debounce		f_{CLK}= 1.0 MHz		131		ms
Charge Pulse Width	t_{CPW}	f_{CLK}= 1.0 MHz		1048		ms
Discharge Pulse Width	t_{DPW}	f_{CLK}= 1.0 MHK		5		ms
Settling Time		f_{CLK}= 1.0 MHz		4		ms
ADC Acquisition Time	t_{ADC}	f_{CLK}= 1.0 MHz		16.38		ms
Cycle Time	t_{cycle}	f_{CLK}= 1.0 MHz		1077		ms
Capacitor Discharge Pulse Width	t_{CDW}	f_{CLK}= 1.0 MHz		5		ms
Capacitor Discharge Pulse Period	t_{CD}	f_{CLK}= 1.0 MHz		100		ms
Polling Detect Pulse Width	t_{PDW}	f_{CLK}= 1.0 MHz		100		ms
Polling Detect Pulse Period	t_{PD}	f_{CLK}= 1.0 MHz		524		ms
Topping Charge Length	t_{TC}	f_{CLK}= 1.0 MHz		2.096		hrs
Maintenance Mode Sample Delay		f_{CLK}= 1.0 MHz		4.19		s
Maintenance Mode Voltage Sample Period		f_{CLK}= 1.0 MHz		4.19		s
Temperature Sample Period		f_{CLK}= 1.0 MHz		33.54		ms
Deep Discharge MMN Indicator Blink Rate		f_{CLK}= 1.0 MHz		524		ms
Deep Discharge Pulse Width	t_{DDC}	f_{CLK}= 1.0 MHz		250		ms

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Table 10: Voltage Thresholds

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Deep Discharge Termination	V_{DDC}			0.8		V
Maintenance Mode Removal Voltage Drop	V_{rem}			0.2		V
Temperature Voltage Difference				15.9		mV
Thermal Switch Open Circuit				4.2		V
Thermal Switch Short Circuit				0.15		V
Cold Thermistor				2.4		V
Hot Thermistor				0.98		V
Capacitor Discharge Short Circuit	V_{SC}			0.2		V

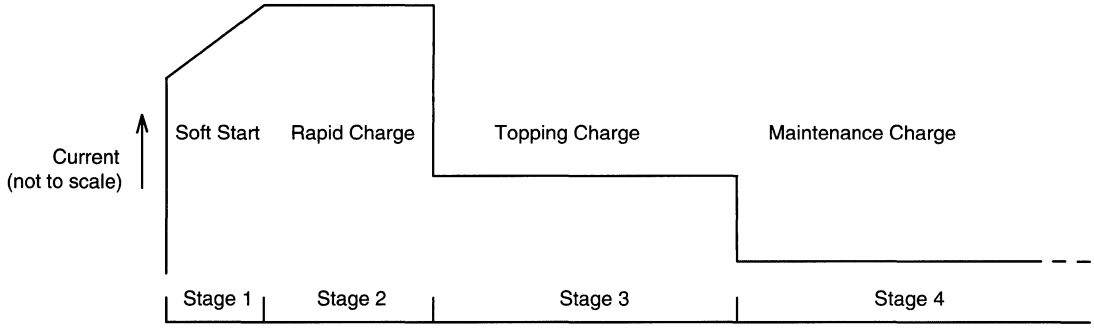

Figure 4: Graphical representation of current levels during the four charging stages

Operation

Charging Stages

The charging sequence consists of four stages. The application of current can be shown graphically in Figure 4. Soft start charge gradually increases current levels up to the user specified fast charge levels during the first few minutes of charge.

The soft start is followed by a high current charge that includes a deep, reverse polarity pulse of short duration, which continues until termination. After termination, a two hour C/10 topping charge followed by a C/40 maintenance charge is applied. Each of these four stages is described next in more detail.

Soft Start Charge

Rechargeable cells can exhibit a high impedance condition while accepting the initial charging current. This high impedance condition can cause a false voltage inflection point at the beginning of the charge cycle which may be misinterpreted as a fully charged battery by the voltage inflection termination method. In the first stage, the soft start routine is intended to ease batteries into a fast charge mode by gradually increasing the current to the fast charge rate. The gradual increase in current alleviates the false inflection point, improves charge efficiency and improves battery life.

Fast Charge

In the second stage, the **ICS1702** employs a method of applying the charge current in a series of charge and discharge pulses that is intended to increase the charging efficiency. The technique consists of a positive current charging pulse followed by a high current, short duration discharge pulse. The cycle, shown with charge, discharge, rest and data acquisition periods in Figure 5, repeats until the batteries are fully charged.

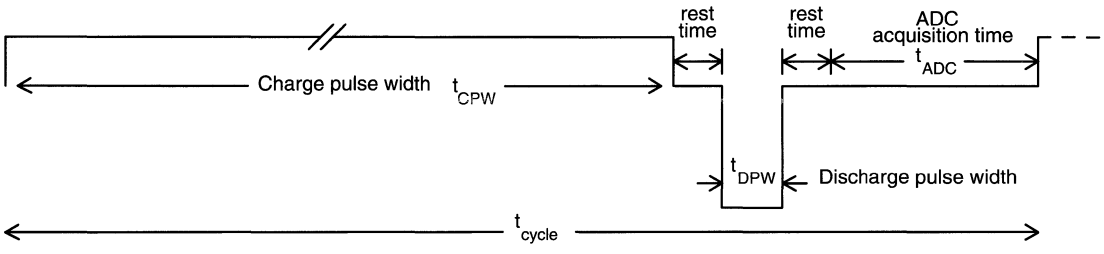

Figure 5: Charge cycle showing charge and discharge current pulses

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The amplitude of the charging pulse is determined by the current capability of the power supply, the desired charge rate, the cell capacity and the ability of that cell to accept the charge current. The **ICS1702** can control nine user-selectable fast charge rates from 15 minutes (4C) to four hours (C/4). Charge pulses occur approximately every second. The charge indicator CMN is the only indicator active during this charge mode. Additional information on charge rates is discussed under the heading, *Charge Rate Selection*.

The discharge current pulse should have an amplitude set to a minimum of -2.5 times the amplitude of the charging current. For example, if the charge current at 4C is 4 amps, then the discharge current should be -10 amps. The energy removed during the discharge pulse is a fixed ratio to the positive charge rate. The cell capacity determines the absolute value of the discharge pulse.

A data acquisition window immediately follows a brief settling time after the discharge pulse. No charge is applied during the settling time or during the acquisition window to allow the cell chemistry to recover. Since no current is flowing, the measured cell voltage is not obscured by any internal or external IR drops or distortions caused by excess plate surface charge. The **ICS1702** makes one continuous reading of the no-load battery voltage during the entire acquisition window. The voltage that is measured during this window contains less noise and is a more accurate representation of the true state of charge of the battery. Specific timing information is given in Table 9, *Timing Characteristics*.

Topping Charge

A cell that is quickly charged suffers a loss of charge efficiency depending on the ability of the cell to accept charge at high current rates. The third stage is a topping charge designed to ease the cells into a slight overcharge. This ensures a 100% charge to the batteries. Current is applied at a rate low enough to prevent overcharge damage but high enough to ensure a full charge.

When the **ICS1702** completes the fast charge mode, a timed C/10 charging current is applied for 2 hours (t_{TC}). This charging current consists of the same reverse pulse current technique used during the fast charge mode, however the duty cycle of the pulse sequence has been extended as shown in Figure 6 below. Extending the delay time between charge pulses allows the same charging current used to fast charge the cells so that no changes to the constant current source are necessary. For example, the same charge pulse that occurs every second at a 2C fast charge rate will occur every 20 seconds for a topping charge rate of C/10. The pulse periods for the topping charge at different charge rates is discussed under the heading, *Charge Rate Selection*. The maintenance mode indicator is the only indicator active during this mode.

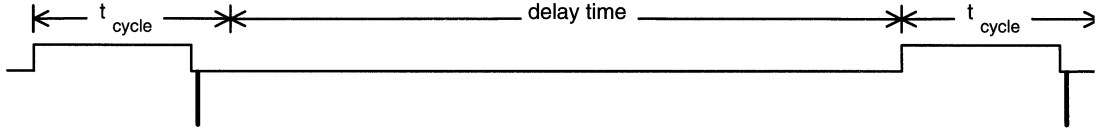

Figure 6: Representative timing diagram for topping and maintenance charges

Maintenance Charge

The maintenance charge is intended to offset the natural self-discharge of NiCd or NiMH batteries by keeping the cells primed at peak charge. When the topping charge mode is completed, the **ICS1702** begins the fourth charge stage by extending the duty cycle of the applied current pulses again. The current pulses are decreased to a C/40 rate which will last for as long as a battery voltage is present at the voltage input (VIN) pin, or, if the ten hour timer mode is enabled, until the timer stops the controller. The maintenance mode indicator MMN is the only indicator active during this mode.

Charge Termination Methods

Seven charge termination schemes, including voltage inflection (*dV/dt*), negative voltage slope (*-dV/dt*), maximum voltage (V_{max}), temperature slope (*dT/dt*), maximum temperature (T_{max}) and two overall charge timers are available for use during fast charge. The voltage inflection and negative voltage slope methods may be used with or without the temperature slope and the maximum temperature method. Maximum temperature, maximum voltage and the fast charge timer are always enabled as backup methods. If voltage termination is used, an initial voltage slope check is performed to detect fully charged cells.

Voltage Inflection Termination (dV/dt)

The most distinctive point on the voltage curve of a charging battery in response to a constant current is the peak in the voltage curve that occurs as the cell transitions from charge to overcharge. The voltage peak is characterized by a relatively shallow voltage slope that becomes sharply steeper, flattens out and drops sharply negative. By mathematically calculating the first derivative (*dV/dt*) of the voltage, a second curve can be generated showing the change in voltage with respect to time as shown in Figure 8.

The slope changes its profile sharply in response to small perturbations in the cell voltage. The slope will reach a maximum just before the actual peak in the cell voltage, as shown in the figure. By calculating a relation between the minimum slope and an empirically derived threshold, the **ICS1702** can predict the moment of full charge and accurately terminate the applied current before the battery begins to overcharge.

Negative Voltage Slope Termination (-dV/dt)

Cells that are charged at low charge rates, or those cells which are not thoroughly conditioned, or are possessing an unusual cell construction may not have a normal voltage profile. The **ICS1702** also uses an alternate method of charge termination based on a slight decrease in the voltage slope to stop charge to cells whose voltage profile is very shallow. The negative slope method looks for a flattening of the voltage slope which may indicate a shallow peak in the voltage profile, and enters the maintenance mode if the slope is less than zero for three successive samples. The zero slope point occurs slightly beyond the peak voltage and is shown on the voltage curve graph.

Maximum Voltage Termination (V_{max})

By placing a voltage level at the open circuit reference (OPREF) pin, the ***ICS1702*** establishes an open circuit, or maximum voltage threshold. If the normalized battery voltage reaches the threshold, the charge terminates to the polling detect mode until voltage levels fall below the threshold. This mode can be disabled by tying the pin to V_{DD}. *This method is not recommended as the only charge termination method because the **ICS1702** will attempt to recharge the battery if the voltage levels fall below the threshold at the OPREF pin. The maximum voltage threshold is primarily intended to detect the removal or insertion of the battery.*

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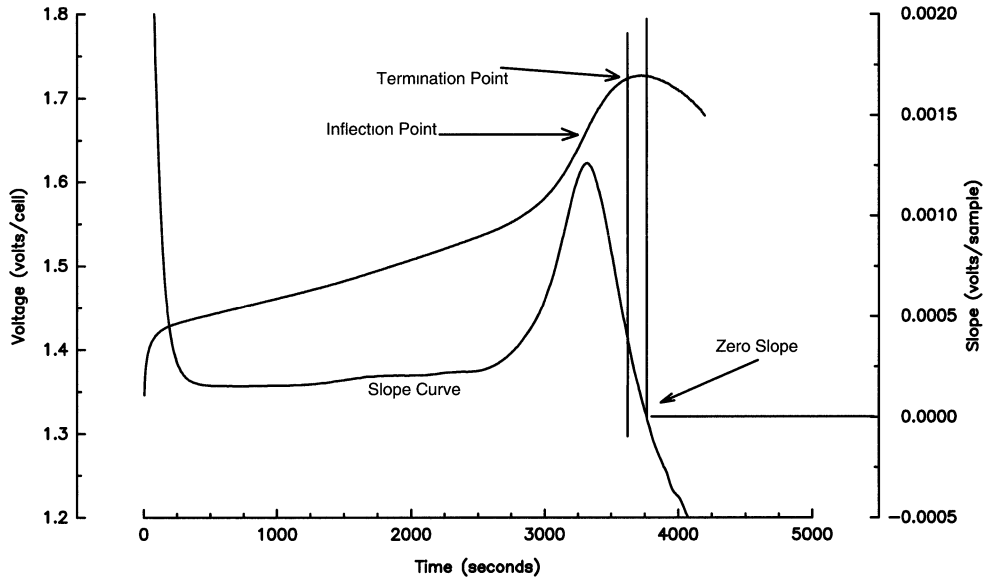

Figure 7: Voltage and slope curves vs. charge time

Temperature Slope Termination (dT/dt)

Temperature slope termination is based on the premise that a battery which is approaching full charge will experience a high rate of heating due to the internal chemical reaction. NiCd batteries differ from NiMH batteries in that the chemical reaction that occurs during charge is endothermic (the reaction absorbs heat) and is exothermic for NiMH batteries (the reaction produces heat). However, both types will produce measurable heat as the overcharge region is approached.

The **ICS1702** can be configured to terminate the fast charge with or without voltage based termination methods via temperature slope termination. See Operation, *Termination Selection* for information on setting the termination select (DTSEL) pin to enable termination on voltage slope, temperature slope or both.

A thermistor must be used for temperature slope termination, and a 10 KΩ @ 25°C type is recommended. Maximum temperature is always enabled, so voltage levels must fall into the proper voltage zones (see the *Maximum Temperature Termination* section). The **ICS1702** samples the voltage dropped across the thermistor every 32 seconds, and will terminate if the voltage difference at the pin is greater than 16 mV between one sample and the next. This corresponds to an increase in cell temperature of approximately 0.7°C/min. See Operation Information, *Temperature Sensing* for information on using a thermistor at the temperature sense (THERM) pin.

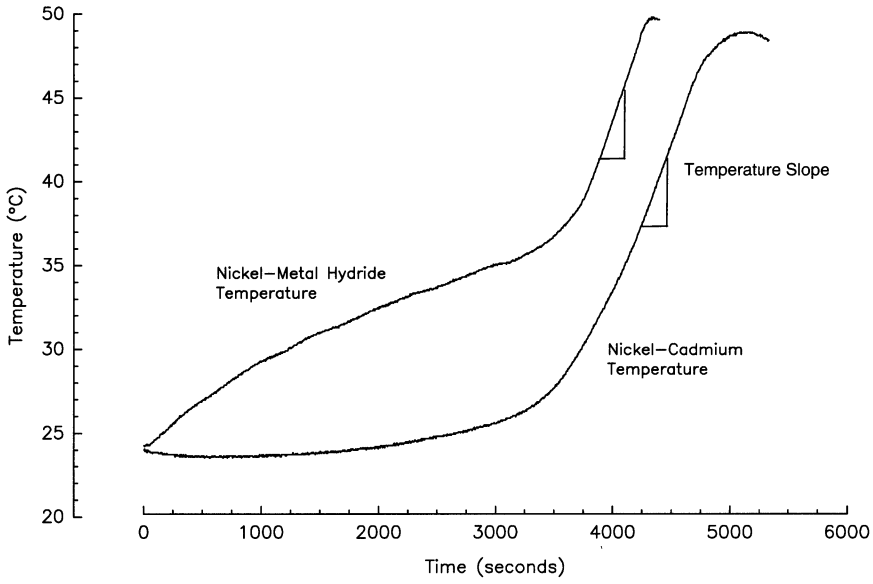

Figure 8: Temperature curves for NiCd and NiMH batteries

Maximum Temperature Termination (T_{max})
Maximum temperature can be sensed using either a thermistor or a thermal switch. The maximum temperature termination can also be bypassed if desired, although it is strongly recommended that some form of temperature termination be used. The hardware used to sense maximum temperature levels is always enabled, and can only be disabled by shorting the temperature sense pin (THERM) to ground. Maximum temperature termination cannot be disabled if temperature slope termination is used.

If a thermistor is used, the **ICS1702** has two voltage thresholds which sense whether the battery is too hot or too cold to charge. The thresholds are designed for a typical 10 KΩ @ 25°C NTC thermistor. These voltage levels are sensed across the thermistor. As temperature increases, the voltage across the thermistor will drop. At a temperature of 45°C, the **ICS1702** assumes the battery has gotten hot and charge is terminated. Refer to Table 4 for voltage indications at several temperatures.

If a thermal switch is used, a 45°C open circuit switch is recommended. If the switch is closed to ground (signifying the battery is less than 45°C), the chip will operate since the voltage at the THERM pin will be at ground. If the switch opens at 45°C, an internal pull-up will engage and the **ICS1702** will fault to over temperature since the voltage will be at V_{DD}.

If a battery is determined to be hot, either through an open thermal switch or a thermistor threshold, the over temperature (OTN) indicator will turn on. The device must be reset once the over temperature condition has cleared to start the charge sequence. The appropriate indicators for the particular charge mode will light when the temperature is normal and charging can begin.

The section Mode Selection, *Cold Temperature Charging* has information on the cold temperature region. See the section under *Temperature Sensing* for more information regarding the use of a thermistor or a thermal switch at the temperature sense pin. Table 4 in that section lists voltages and corresponding temperatures.

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Ten Hour Timer Termination[3]

Placing the AUX0 and AUX1 pins in a high impedance state enables an overall ten hour timer. The timer limits the total charge, including the maintenance charge, to approximately ten hours. The actual time will vary depending on the charge rate selected and on the termination method. This mode is useful in avoiding an indefinite maintenance charge applied to the battery. The maximum time for the maintenance mode beyond the charge time is given in Table 11.

Table 11: Ten Hour Timer List

Charge Time (hours)	Charge Rate	Maximum Timer Cutoff After Charge Termination (hours)
0.25	4C	9.70
0.5	2C	9.38
0.75	1.3C	9.08
1	1C	8.79
1.5	C/1.5	8.20
2	C/2	7.64
2.5	C/2.5	6.50
3	C/3	5.97
4	C/4	5.45

Fast Charge Timer Termination[4]

The **ICS1702** also uses a timer to shut off the fast charge if the device goes beyond a safe charging time limit. These times are programmed into the chip, and are listed below in Table 12. If the device is used at a charge rate other than the ones allowed, care must be taken to avoid premature termination due to the timer cutoff. This *deadman* timer cannot be disabled.

Initial Slope Check

The initial slope check is a test to detect fully charged batteries before a long term high current charge is applied. After that period of time, the initial slope value is calculated and is tested for a negative value. If the initial slope is negative, the voltage must be decreasing over the sampling period and the battery is assumed to be fully charged. The **ICS1702** will then enter the maintenance mode. If the slope is positive, the **ICS1702** stores the slope and continues charging.

This check is always active when voltage slope termination is enabled. If temperature slope termination is used without voltage termination, this check is not performed.

Table 12: Fast Charge Timer List

Charge Time (minutes)	Charge Rate	Timer Cutoff (minutes)
15	4C	18.75
30	2C	37.08
45	1.3C	55.00
60	1C	72.50
90	C/1.5	107.5
120	C/2	141.6
150	C/2.5	209.89
180	C/3	241.90
240	C/4	273.14

[3] When the ten-hour timer shuts off, the ICS1702 MUST be reset before a charge can begin again No indicator will be on after this timer shuts off

[4] When the fast charge timer shuts off the fast charge operation, the ICS1702 will go into maintenance mode charge and the maintenance mode indicator will be on at this time

Battery Detection and Removal

The following sequences describe how the **ICS1702** attempts to determine the presence of a battery before and during charge. An open circuit voltage threshold (V_{OC}) should be established at the OPREF pin at a level which can only occur when current is applied to open terminals. If the voltage at the terminals exceeds the threshold while a charging current is applied, the **ICS1702** assumes the battery is missing and enters the polling detect mode. More information on the open circuit threshold is provided below and in the section, *Open Circuit Reference.*

Capacitor Discharge Detect

After a master reset has occurred, the **ICS1702** uses six 5ms discharge pulses spaced 100ms apart to remove any excess charge from any output filter capacitors at the charging system terminals. When the discharge pulse sequence is complete, the **ICS1702** will expect to see more than 0.2V (V_{SC}) at the voltage input pin if a battery is present. If the voltage at the pin is less than V_{SC}, the device assumes no battery is present, and the polling detect mode is initiated. No indicator is active during the discharge pulses.

Polling Detect

The **ICS1702** enters this mode by applying a charge pulse for a 100ms duration. During the pulse, the **ICS1702** monitors the voltage input pin to determine if a voltage above V_{OC} is at the terminals. If the battery is present, the battery voltage will be below the voltage set at the open circuit reference pin while charge is applied. If a battery is not present, the voltage will be above the open circuit voltage reference.

The charge pulses will recur at 524ms intervals for an indefinite period of time. Caution must be used since there is always the possibility of a potential present at the charging system terminals. The polling detect indicator (PFN) is the only indicator active as long as the **ICS1702** is in the polling detect mode. Once a battery is detected, the **ICS1702** will enter the soft start mode. The **ICS1702** will automatically re-enter the polling detect sequence if the battery is removed during charge or during the dual stage maintenance mode.

Charge Mode Removal

During the application of soft start charge pulses and fast charge pulses, the voltage at the voltage input pin is compared to the voltage at the open circuit reference pin. If the voltage is greater than the open circuit reference during the application of the current pulse, then the battery is assumed to have been removed and the **ICS1702** enters the polling detect mode. If the voltage is below the reference level, the charging mode continues. Voltage comparisons are made once every second.

Maintenance Mode Removal

When in the topping charge or maintenance charge modes, a charge pulse may not occur for several seconds. During the period between charge pulses, the **ICS1702** records the voltages at the battery terminals. After the most recent charge pulse, the **ICS1702** waits 4 seconds to allow the battery voltage to settle. If the voltage at the VIN pin drops more than 0.2V (V_{rem}) during any subsequent 4 second period when no current is applied, the device assumes the battery has been removed and the **ICS1702** enters the polling detect mode. Note: If the charge pulse period is less than 8 seconds (for either the topping charge or maintenance charge, as listed in Table 2) then the **ICS1702** relies on the same method as described in the *Charge Mode Removal* section.

Mode Selection

The **ICS1702** allows six special methods of operation to help customize the charging system for certain applications. The tristate AUX0 and AUX1 pins are used to select the operating mode the **ICS1702**. An internal pull-up at the AUX0 and AUX1 pins default the **ICS1702** into normal fast charge operation. For specialized applications, the **ICS1702** can enter five other modes. Once a mode has been selected, no other mode can be used unless the part is re-programmed and reset.

Deep Discharge to Charge Mode

Batteries with an unknown amount of energy remaining can be cycled through a complete discharge before a fast charge is initiated. This mode drains the battery down to 0.8V (V_{DDC}) as read at the voltage input pin under load and enters the fast charge mode programmed by the charge rate select pins. The load is supplied by pulsing the discharge pin at a 250ms rate. Assuming that the discharge pin is calibrated at a -2.5C current amplitude for the desired battery capacity, the discharge rate will be approximately 1C.

The deep discharge to charge mode can be entered by setting the AUX0 to a high logic level and AUX1 to a low logic level. Set the S0 and S1 line for the desired charge rate. Once the device is reset the discharge mode will occur first, to be followed by the selected fast charge mode. During the discharge period of this mode, the maintenance mode indicator MMN will alternate on and off at a 524ms rate.

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Direct Maintenance Mode

The **ICS1702** can be brought directly into the C/40 maintenance mode for cells that require a maintenance charge only. The direct maintenance mode is activated by setting the AUX0 and AUX1 pins both to a low logic state and resetting the device. The S0 and S1 pins must also be set for charge current capability of the constant current supply. The maintenance charge is applied until the battery is removed from the voltage input pin, upon which the device will enter a polling detect mode. The maintenance mode indicator MMN will be active during the application of the maintenance charge.

Conditioning Mode

The **ICS1702** can enter a conditioning mode which applies a C/10 charge for a timed 10 hour charge, followed by an indefinite C/40 maintenance mode until the batteries are removed. This mode may be used for brand new batteries which need to be conditioned at a low charge rate, or for cells whose general condition is unknown.

The conditioning mode can be entered by setting the AUX0 and AUX1 pins to a high logic and high impedance state, respectively. The S0 and S1 pins must also be set for the charge current capability of the constant current supply. The **ICS1702** will enter the mode upon a master reset. The maintenance mode indicator (MMN) will be active during the 10 hour conditioning charge and the maintenance charge which will follow. The device enters a polling detect mode if the battery is removed from the voltage input pin.

Device Self-Test Mode

The self-test mode is intended for use in applications where the functionality of the **ICS1702** is to be tested in a circuit. The self-test sequence consists of the one second testing of the CMN, MMN and PFN indicator pins as well as the CHG and DCHG lines. The over temperature indicator is not tested. The mode is entered by placing the AUX0 and AUX1 lines in a low and high logic state, respectively. The **ICS1702** shuts the internal oscillator down after the test sequence is finished and a master reset must be performed to reactivate the device.

Ten Hour Mode

Placing the AUX0 and AUX1 pins in a high impedance state enables an overall ten hour timer. This timer limits the total charge, including the maintenance charge, to approximately ten hours. This mode is useful for users who wish to avoid an indefinite maintenance charge applied to their cells and serves as a final safety check. Additional information is given under Charge Termination Methods, *Ten Hour Timer Termination*.

Cold Temperature Charging

Cold temperature charging is activated if a voltage at the temperature sense (THERM) pin is in the cold temperature voltage range, as shown in Table 4. The voltage is generated by a thermistor where a change in resistance causes a voltage divider to maintain a voltage in a specific range. The **ICS1702** only checks for a cold battery before the fast charge cycle is to begin. If a battery becomes cold while a normal charge is in progress, the OTN indicator will become active, however fast charging will continue.

If a cold battery is determined to be present before charging begins, the **ICS1702** begins a two hour C/10 topping charge (the pulsed duty cycle is based on the selected charge rate). The thermistor voltage at the temperature sense pin is checked every second to see if the battery has warmed into the fast charge region. If so, the **ICS1702** stops the topping charge and begins a fast charge at a rate selected by the S0 and S1 lines. If a cold battery is not present, the normal charge as determined by the S0 and S1 lines will begin.

The maintenance mode and over temperature indicators will be active (low), indicating that a low current charge is being applied to a battery that is outside the specified temperature range for fast charging.

Applications Information

Figure 9 shows a typical application using the **ICS1702**. R1 and R2 are selected to scale the battery voltage to 1 cell. The following table shows some typical values. Additional information is available under Pin Descriptions-*Voltage Input: VIN Pin.*

CELLS	R1	R2
1	Short	Open
2	2K	2K
3	2K	1K
4	3K	1K
5	12K	3K
6	10K	2K
7	12K	2K
8	9.1K	1.3K

R3 and R4 are used to set the open circuit reference voltage. The function of this pin is discussed under Pin Descriptions *Open Circuit Reference: OPREF Pin.*

It is very important that care be taken to minimize noise coupling and ground bounce. In addition , wiring resistance and connectors can add significant amounts of resistance to the charge and discharge circuits. Be sure to connect the ground side of the discharge transistor to the negative lead of the battery *as close to the battery as possible.* This will reduce ground bounce and coupled noise.

When designing a printed circuit board, make sure ground and power traces are heavy and bypass capacitors are used close to the chip. Use a separate ground system for the discharge current to prevent high circulating currents from disturbing normal operation.

A constant current source should be used to provide charging current to the battery. Resistors may be used if the current does not vary more than 20%.

Additional application information will be provided in the final version of the data sheet, and as part of a series of regular technical updates.

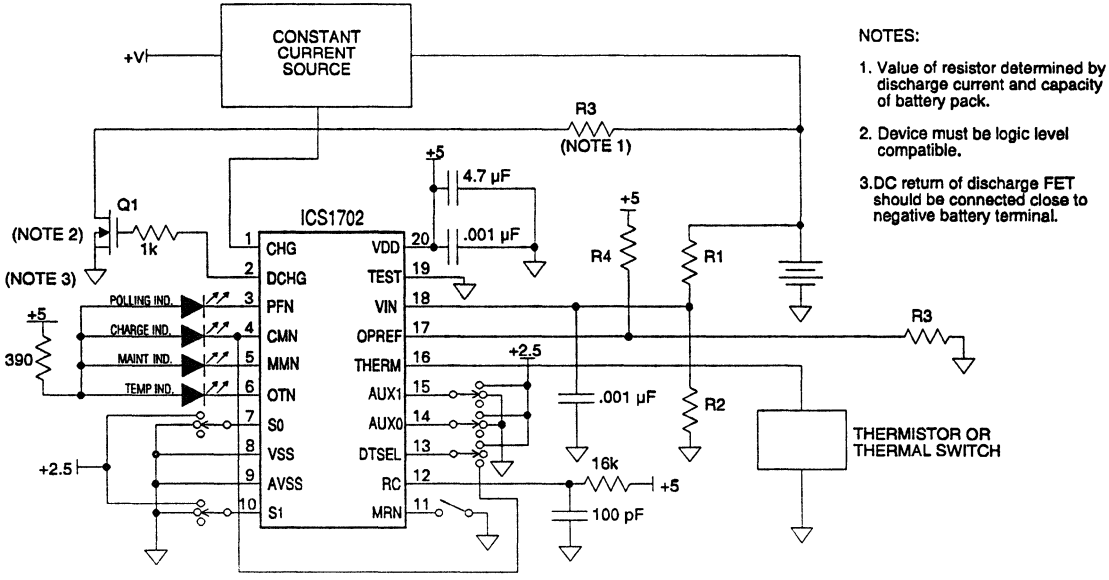


Figure 9: Functional Diagram

Battery Charging and Capacity Measurement IC

General Description

The **ICS1705** is a CMOS IC which resides in the battery pack and operates in conjunction with a host processor or controller. The host processor and the **ICS1705** are configured as Master/Slave. The **ICS1705** provides *pack specific* battery information, and contains all the analog circuitry necessary for accurate capacity, self-discharge and voltage measurement.

The **ICS1705** measures and stores battery voltage and monitors temperature through a sensor, providing all analog data to allow the host processor to control the charging. The **ICS1705** also outputs one of 8 factory-programmable battery identification numbers, and accumulates temperature dependent self-discharge information. To minimize interconnect, the **ICS1705** supports a single wire bi-directional asynchronous serial link to the host processor for data read/write, voltage and temperature monitoring and is compatible with most microcontroller asynchronous serial I/O ports.

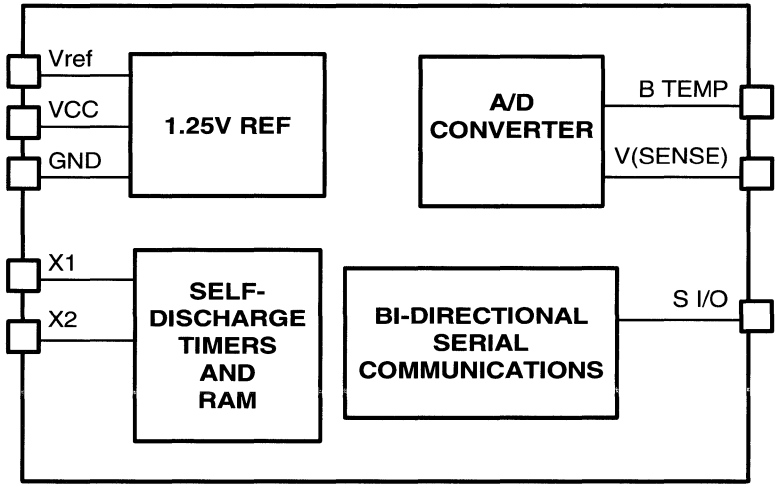
Features

- Complete "in the pack" capacity and charge measurement system
- Delta/sigma A/D for measurement of:
  Battery voltage
  Ambient and battery temperatures
- Temperature dependent self-discharge monitor
- Single wire asynch serial interface to host µC
- 20µA (max) standby current
- Eight bytes of RAM for capacity and history storage
- Wide supply voltage operating range

Applications

- Mobile communications
- Consumer video
- Notebook and laptop computers
- Personal digital assistants
- Portable instruments

Block Diagram



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Quad Power Management Switches

General Description

The AV9304/AV9504 Power Management Integrated Switch (PMIS) is designed for 3 and 5 Volt systems that need to switch steady state currents of up to 500mA. The PMIS is a self contained part requiring no external components. The AV9304 and AV9504 contain four power switches, in either the 16 pin PDIP or the 300 mil wide 16 pin SOIC package.

The N-Channel FET switches have a typical 0.3Ω on- resistance, with a maximum of 0.4Ω. For switching currents larger than 500mA, these transistors can be paralleled together. The +2.7V to +3.7V input supply range, the low quiescent current and the automatic power down features make the AV9304 ideal for battery-powered switching and control applications, such as notebook computers, portable medical analyzers and test equipment.

The "soft turn-on" feature of the 9304/9504 ensures that there will be no spikes on the switched power supply when the power turns on to the load.

The 9304 operates with a supply voltage of 2.7 to 3.6V while the 9504 operates with a supply voltage of 4.5 to 5.5V. Either part can switch loads from 2.7V to 5.5V.

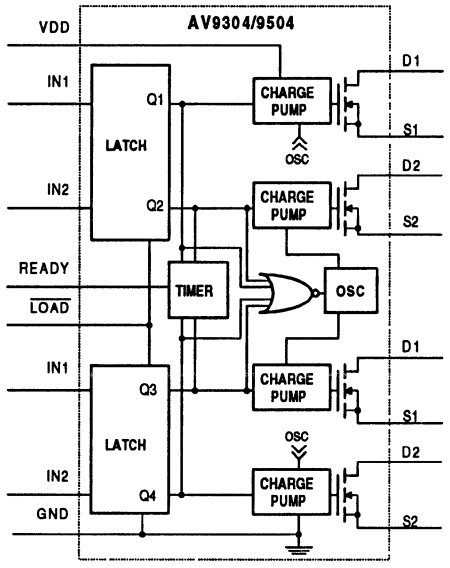
Features

- AV9304: 3.0 or 3.3V operating supply voltage
- AV9504: 5V operating supply voltage
- Switches loads from 2.7V to 5.5V
- 0.3Ω typical, 0.4Ω max switch resistance
- Steady state current of 500mA per switch
- Automatic Power Down
- 1 msec FET soft turn on
- No external components required
- Output Ready signal

Applications

- Notebook PC Power Switching
- PCMCIA VCC Switching
- PDA's
- Palmtop Computers
- Hand-Held Medical Instruments

Block Diagram



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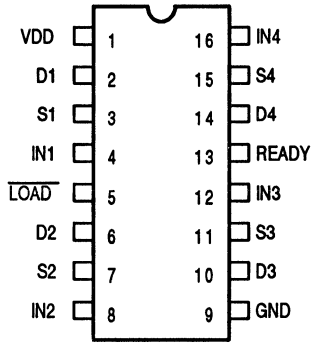
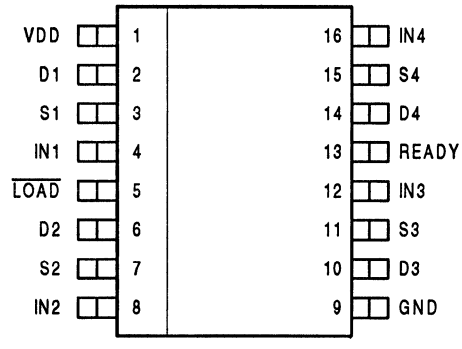
Pin Configuration



16-Pin DIP (N16)



16-Pin SOIC (M16W)

Pin Descriptions

PIN #	PIN NAME	TYPE	DESCRIPTION
1	VDD	—	Positive supply voltage for the IC
2	D1	Out	FET 1 Drain
3	S1	Out	FET 1 Source
4	IN1	In	Logic input to FET 1 driver
5	$\overline{\text{LOAD}}$	In	Transparent low latch. A logic "0" on this pin allows data to flow from IN to the FET driver. A logic "1" latches the outputs in their present state.
6	D2	Out	FET 2 Drain
7	S2	Out	FET 2 Source
8	IN2	In	Logic input to FET 2 driver
9	GND	—	Ground
10	D3	Out	FET 3 Drain
11	S3	Out	FET 3 Source
12	IN3	In	Logic input to FET 3 driver
13	READY	Out	Pulse indicating last input to change has its FET stable and fully turned on
14	D4	Out	FET 4 Drain
15	S4	Out	FET 4 Source
16	IN4	In	Logic input to FET 4 driver

Ordering Information:

Part Number	Temperature Range	Package Type
AV9304CN16	0°C to 70°C	16-lead plastic DIP (P16)
AV9304CW16	0°C to 70°C	16-lead Plastic SOIC (M16W)
AV9504CN16	0°C to 70°C	16-lead plastic DIP (P16)
AV9504CW16	0°C to 70°C	16-lead Plastic SOIC (M16W)

Absolute Maximum Ratings

VDD referenced to GND 7V
Storage temperature ..... -40°C to +125°C
Voltage on I/O pins ..... -.05V to VDD +0.5V
Power dissipation ..... 0.5 Watts

Operating Conditions

Drain Voltage:
AV9304 ..... 2.7V to 5.5V
AV9504 ..... 2.7V to 5.5V
Operating temperature under bias ..... 0°C to +70°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

AV9304 (Operating V_{DD}=+2.7 to +3.7V, T_A=0°C to 70°C unless otherwise stated)
AV9504 (Operating V_{DD}=+4.5 to +5.5V, T_A=0°C to 70°C unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Characteristics						
Chip supply	V_{DD}	AV9304	2.7	3.3	3.7	V
Chip supply	V_{DD}	AV9504	4.5	5	5.5	V
Switch Drain Voltage	V_{DF}(1)		2.7		5.5	V
Switch Source Voltage	V_{SF}		V_{DF} -0.2		V_{DF}	V
Input Low Voltage	V_{IL}		V_{SS}		0.2V_{DD}	V
Input High Voltage	V_{IH}		0.7 V_{DD}		V_{DD}	V
Switch Current	I_{DF}		0		500	mA
Supply Current	I_{DD2}(2)	All switches active		100	200	µA
Standby Current	I_{DDSB}	All switches off		2	4	µA
Input Low Current	I_{IL}	V_{IN} = 0V		-	-2	µA
Input High Current	I_{IH}	V_{IN} = V_{DD}		-	2	µA
Switch on Resistance	R_{ON}	All conditions		.3	.4	Ω
Switch on Resistance	R_{ON}	25°C,V_{DF}=3.3V		.25		Ω
AC Characteristics						
$\overline{LOAD}$ Pulse Width	t_W		50		-	ns
IN_X to LOAD Inactive Setup Time	t_{SU}		20		-	ns
LOAD inactive to IN_X Hold Time	t_{HD}		10			ns
Delay to Ready	t_D				6	ms

Note 1: In addition to the power dissipated by the oscillator and 4 charge pumps, the drop across the switches also contributes to the on chip power. This power per switches is given by: $I_{DF}(V_{DF}-V_{SF})$. The total on-chip power should be held below 0.5W.

Note 2: The current consumed by the IC is proportional to the number of switches on. If only 1 FET is on, I_{DD} will be 1/4 of specified value.

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Device Description

Each of the channels consists of a transparent latch, charge pump, and N-Channel FET. Logic inputs to the drivers are latched when $\overline{LOAD}$ goes high. The logic high signal from the latch activates the charge pump and, a few milliseconds later, the FET is fully turned on. On chip circuitry controls the FET turn on, which typically takes 1ms (fig 2.), to avoid the power supply current spikes (fig. 1) which would occur if the switch turned on fast into a fully discharged load capacitance. The chip has a common oscillator that drives the 4 charge pumps and runs at approximately 500KHz.

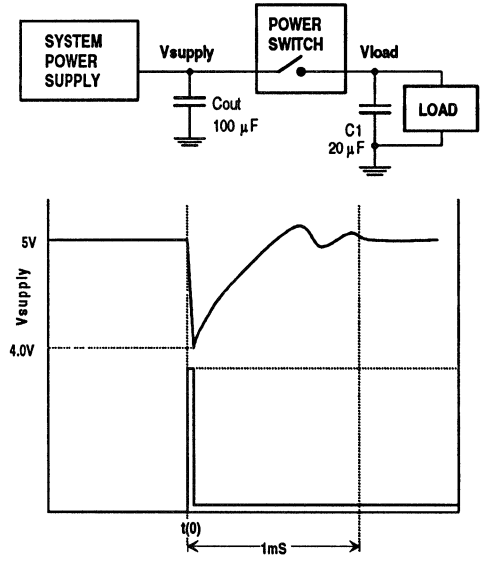

Figure 1. Power Supply glitch caused by fast T_{ON}

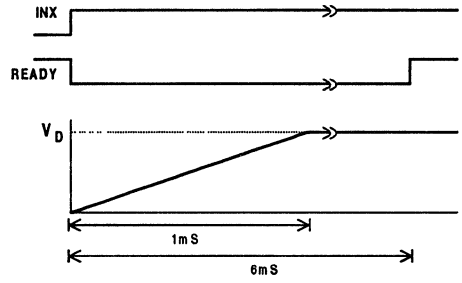

Figure 2. ICS9304/9504 controlled output rise-time and READY signal timing

An edge detector monitors the 4 latch outputs and activates the timer when any output goes high . The Ready signal, which comes from the timer, goes low immediately and then goes high again typically in 6ms, thus generating a negative going pulse (see Figure 1). Ready returns to the high state when output FET is stable and fully turned on.

The automatic power down feature works by monitoring the latch outputs. When all the latch outputs are at a logical zero, the output of the NOR gate is high and asserts the power down to the oscillator.

The AV9304/9504 FETs do not contain source to drain diodes, so when the part is used for switching inductive loads an external diode should be connected across the FET.

Dual Power Management Switches

General Description

The AV9312/9512 Power Management Integrated Switches are designed for 3 and 5 Volt systems that need to switch steady state currents of up to 500mA. These are self contained parts requiring no external components. The AV9312 and AV9512 contain two power switches, and are available in either 14 pin PDIP or 150 mil wide 14 pin SOIC package.

The N-Channel FET switches have a typical 0.2Ω on- resistance, with a maximum of 0.3Ω. For switching currents larger than 500mA, these transistors can be paralleled together. The +2.7V to +3.7V input supply range, the low quiescent current and the automatic power down features make the AV9312 ideal for battery-powered switching and control applications, such as notebook computers, portable medical analyzers and test equipment.

The "soft turn-on" feature of the 9312/9512 ensures that there will be no spikes on the switched power supply when the power turns on to the load.

The 9312 operates with a supply voltage of 2.7 to 3.6V while the 9512 operates with a supply voltage of 4.5 to 5.5V. Either part can switch loads from 2.7V to 5.5V.

Features

- AV9312: 3.0 or 3.3V operating supply voltage
- AV9512: 5V operating supply voltage
- Switches loads from 2.7V to 5.5V
- 0.2Ω typical, 0.3Ω max switch resistance
- Steady state current of 500mA per switch
- Automatic Power Down
- 1 msec FET soft turn on
- No external components required

Applications

- Notebook PC Power Switching
- PCMCIA VCC Switching
- PDA's
- Palmtop Computers
- Hand-Held Medical Instruments

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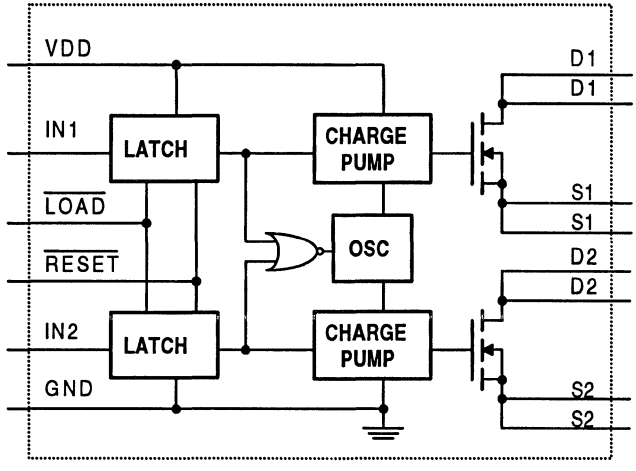
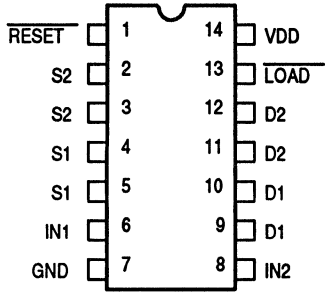
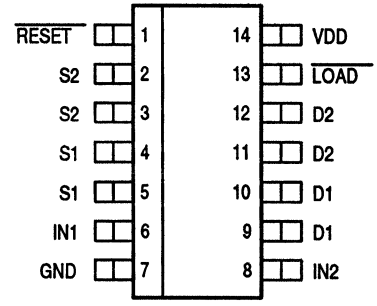
Block Diagram



Pin Configuration



14-Pin DIP (N14)



14-Pin SOIC (M14)

Pin Descriptions

PIN #	PIN NAME	TYPE	DESCRIPTION
1	$\overline{\text{RESET}}$	In	Resets input latches and turns all FET switches off when low
2	S2	Out	FET 2 Source, Must be externally connected to Pin 3
3	S2	Out	FET 2 Source, Must be externally connected to Pin 2
4	S1	Out	FET 1 Source, Must be externally connected to Pin 5
5	S1	Out	FET 1 Source, Must be externally connected to Pin 4
6	IN1	In	Logic input to FET 1 driver
7	GND	—	Ground
8	IN2	In	Logic input to FET 2 driver
9	D1	Out	FET 1 Source, Must be externally connected to Pin 10
10	D1	Out	FET 1 Source, Must be externally connected to Pin 9
11	D2	Out	FET 2 Source, Must be externally connected to Pin 12
12	D2	Out	FET 2 Source, Must be externally connected to Pin 11
13	$\overline{\text{LOAD}}$	In	Transparent low latch. A logic "0" on this pin allows data to flow from IN to the FET driver. A logic "1" latches the outputs in their present state.
14	VDD	—	Power Supply for the chip: 2.7 to 3.6V for AV9312 and 4.5 to 5.5V for AV9512

Ordering Information:

Part Number	Temperature Range	Package Type
AV9312CN14	0°C to 70°C	14-lead Plastic DIP (N14)
AV9512CN14	0°C to 70°C	14-lead Plastic DIP (N14)
AV9312CS14	0°C to 70°C	14-lead Plastic SOIC (M14)
AV9512CS14	0°C to 70°C	14-lead Plastic SOIC (M14)

Absolute Maximum Ratings

VDD referenced to GND 7V
Storage temperature ..... –40°C to +125°C
Voltage on I/O pins ..... –.05V to VDD +0.5V
Power dissipation ..... 0.5 Watts

Operating Conditions

Drain Voltage:
AV9312 ..... 2.7V to 5.5V
AV9512 ..... 2.7V to 5.5V
Operating temperature under bias ..... 0°C to +70°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

AV9312 (Operating V_{DD}=+2.7 to +3.7V, T_A=0°C to 70°C unless otherwise stated)
AV9512 (Operating V_{DD}=+4.5 to +5.5 V, T_A=0°C to 70°C unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Characteristics						
Chip supply	V_{DD}	AV9312	2.7	3.3	3.7	V
Chip supply	V_{DD}	AV9512	4.5	5	5.5	V
Switch Drain Voltage	V_{DF}(1)		2.7		5.5	V
Switch Source Voltage	V_{SF}		V_{DF} –0.2		V_{DF}	V
Input Low Voltage	V_{IL}		V_{SS}		0.2V_{DD}	V
Input High Voltage	V_{IH}		0.7 V_{DD}		V_{DD}	V
Switch Current	I_{DF}		0		500	mA
Supply Current	I_{DD2}(2)	All switches active		100	200	µA
Standby Current	I_{DDSB}	All switches off		2	4	µA
Input Low Current	I_{IL}	V_{IN} = 0V		-	-2	µA
Input High Current	I_{IH}	V_{IN} = V_{DD}		-	2	µA
Switch on Resistance	R_{ON}	All conditions		.2	.3	Ω
Switch on Resistance	R_{ON}	25°C,V_{DF}=3.3V		.15		Ω
AC Characteristics						
$\overline{\text{LOAD}}$ Pulse Width	t_W		50		-	ns
IN_X to LOAD Inactive Setup Time	t_{SU}		20		-	ns
LOAD inactive to IN_X Hold Time	t_{HD}		10			ns

Note 1: In addition to the power dissipated by the oscillator and 2 charge pumps, the drop across the switches also contributes to the on chip power. This power per switches is given by: $I_{DF}(V_{DF}–V_{SF})$. The total on-chip power should be held below 0.5W.

Note 2: The current consumed by the IC is proportional to the number of switches on. If only 1 FET is on, I_{DD} will be 1/2 of specified value.

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Device Description

Each switch channel consists of a transparent latch, charge pump, and N-Channel FET. Logic inputs to the drivers are latched when $\overline{LOAD}$ goes high. The logic high signal from the latch activates the charge pump and, a few milliseconds later, the FET is fully turned on. On chip circuitry controls the FET turn on, which typically takes 1ms (fig 2.), to avoid the power supply current spikes (fig. 1) which would occur if the switch turned on fast into a fully discharged load capacitance. The chip has a common oscillator that drives the 2 charge pumps and runs at approximately 500KHz.

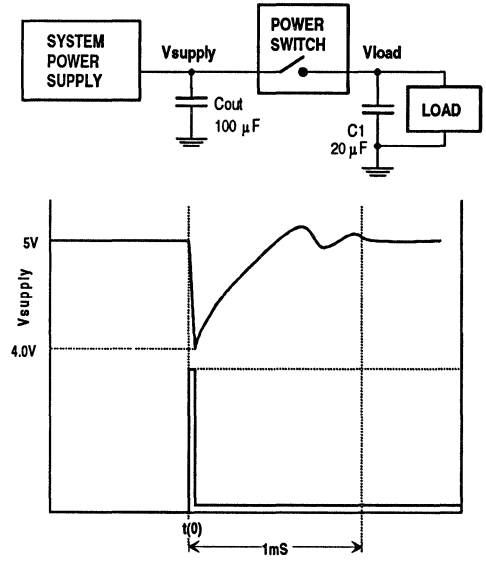

Figure 1. Power Supply glitch caused by fast T_{ON}

The automatic power down feature works by monitoring the latch outputs. When all the latch outputs are at a logical zero, the output of the NOR gate is high and powers down the oscillator to conserve power.

The AV9312/9512 FETs do not contain source to drain diodes. If the part is used for switching inductive loads, an external diode should be connected across the FET.

The source pins and drain pins should be connected together externally for each output switch to obtain minimum switch on resistance. So, D1 (pin#9) should be connected to D1 (pin #10) and likewise with D2, S1, and S2.

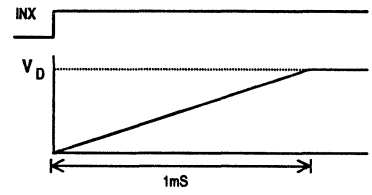

Figure 2. ICS9312/9512 controlled output rise-time

To insure the FET switches are off, the $\overline{RESET}$ pin should be pulsed low.

An edge detector monitors the 4 latch outputs and activates the timer when any output goes high . The Ready signal, which comes from the timer, goes low immediately and then goes high again typically in 6ms, thus generating a negative going pulse (see Figure 1). Ready returns to the high state when output FET is stable and fully turned on.

The automatic power down feature works by monitoring the latch outputs. When all the latch outputs are at a logical zero, the output of the NOR gate is high and asserts the power down to the oscillator.

The AV9312/9512 FETs do not contain source to drain diodes, so when the part is used for switching inductive loads an external diode should be connected across the FET.

ICS

Power Management

Applications

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QuickSaver™ Controller For Nickel-Cadmium Batteries

Development of Nickel-Cadmium Batteries

Alkaline nickel plate technology began with the 1899 invention of a vented nickel-cadmium battery by Waldmar Jungner. Around the same time, Thomas Edison experimented with a rechargeable nickel-iron battery for use in electric automobiles. Unfortunately, the materials for these alkaline storage batteries were expensive in comparison with other types of batteries, so their practical use was severely limited.

Since then, several major refinements to Jungner's nickel-cadmium battery have dramatically enhanced the characteristics of nickel-cadmium technology. An improvement in 1932 was a method to place the active materials inside a porous nickel plate electrode, which was then packed inside a metal tube container. By 1947, research had begun on the development of a sealed nickel-cadmium battery that recombined the internal gases caused by the chemical reactions instead of venting them. The successful resolution of that problem has led to a wide range of possible uses for nickel-cadmium batteries.

The advantages of sealed nickel-cadmium batteries include excellent efficiency, long discharge life, high-cycle lifetimes and high-energy density in a small, lightweight, compact design. Nickel-cadmium batteries are cost-effective, require no maintenance and are very rugged. These attributes continue to make these batteries a popular choice for industrial and consumer applications.

Battery Parameters

Batteries are defined as consisting of one or more cells, usually connected in series for higher output voltages. Cells are the individual building blocks, containing a positive cadmium plate, a negative nickel plate, an insulating separator and an alkaline electrolyte.

Cell capacity is specified as the rate of current a cell can supply over time under discharge, usually measured in units of ampere-hours. The quantity of reactive materials inside a cell determines the charge a cell can contain; therefore, the bigger the cell, the more capacity it has.

The parameter for describing current flow is known as the **C** rate. The **C** rate is defined as the current flow rate that is equal to the rated battery capacity. For example, applying a 2 ampere charge to a 1 ampere-hour battery is a 2**C** charge rate. The same 2 ampere charge to a 500 mAh cell is a 4**C** rate. The **C** rate scales with the battery capacity.

The voltage that a nickel-cadmium cell can supply is typically around 1.3 volts under no-load conditions. The internal electrochemical reactions determine the no-load voltage (V_O) of the cell. The voltage changes slightly with ambient temperature, age, and condition of the cell. V_O also varies as a function of the amount of capacity already removed from the cell.

The effective internal impedance (Z_I) is determined by two factors: the resistance of the internal plates in the cell and the degree of difficulty of the ionic flow through the separator and electrolyte. The resistance of the plates is constant; however, the impedance due to the ionic flow varies dramatically during the application of charge to a cell.

Cell Electrochemistry

When a cell is charged or discharged, the nickel and cadmium plates undergo an oxidation-reduction (redox) reaction. This means oxygen, in an ionized form, is transferred between the positive and negative plates.

The redox reaction between the plates occurs without changing the physical condition of the plates. The reaction is entirely self-contained and completely reversible, since the charge or discharge process consumes none of the active materials on the plates. While under charge, the positive plate reduces from cadmium hydroxide to cadmium by releasing oxygen into the electrolyte and by accepting electrons from the charging circuitry:

$$Cd(OH)_2 + 2e^- \underset{\text{Discharge}}{\overset{\text{Charge}}{\rightleftharpoons}} Cd + 2OH^-$$

Equation 1: Reduction Reaction

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QuickSaver is a trademark of Integrated Circuit Systems, Inc

The nickel hydroxide in the negative plate accepts oxygen from the electrolyte to create nickel oxyhydroxide:

$$2Ni(OH)_2 + 2OH^- \underset{\text{Discharge}}{\overset{\text{Charge}}{\rightleftharpoons}} 2NiOOH + 2H_2O + 2e^-$$

Equation 2: Oxidation Reaction

The alkaline electrolyte in the cell does not undergo a chemical change. Its purpose is only to transfer hydroxide ions from one set of plates to the other. The overall reaction of the cell in the electrolyte is:

$$2Ni(OH)_2 + Cd(OH)_2 \underset{\text{Discharge}}{\overset{\text{Charge}}{\rightleftharpoons}} Cd + 2H_2O + 2NiOOH$$

Equation 3: Net Reaction

The oxygen gases that are generated and recombined at the positive and negative plates are exothermic reactions. This means that heat is created during the reaction. The exothermic heating is a potential problem when charging nickel-cadmium batteries.

Cell Charge Curve

Nickel-cadmium cells have a typical voltage vs. time charging curve, as shown in Figure 1:

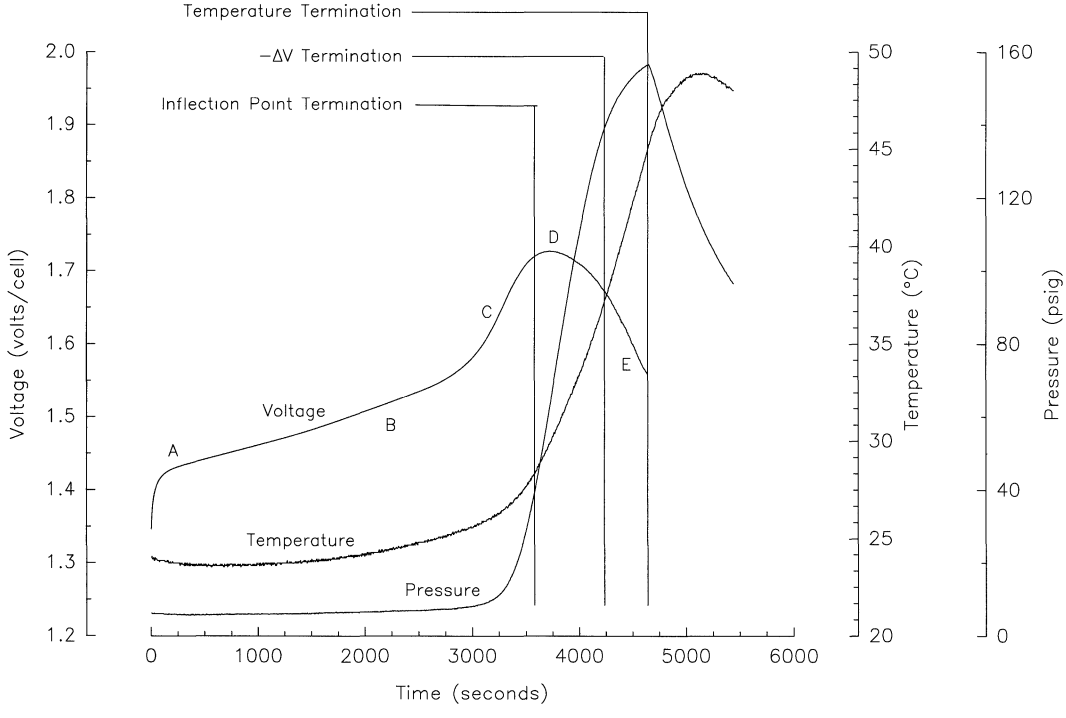

Figure 1: Voltage, Temperature and Pressure Curves

The application of a steady charging current to a discharged battery causes an immediate jump in the cell voltage, due to the cell's internal impedance (point A). The cell voltage continues to rise at a much slower rate as the battery begins to accept a charge. In this region (point B) the oxygen gas generated by the electrochemical reaction is being recombined at the same rate, so the internal cell temperature and pressure remain low.

Oxygen and hydrogen are the two gases generally present during cell charging. Oxygen, which is present in much greater amounts than hydrogen, causes pressure build-up when more oxygen is created than can be absorbed. A nominal pressure during charge of about 1 lb./sq.in. will increase rapidly during overcharge to 100 lb./sq.in. or higher, depending on the charge rate.

At some time during the charge, the cell voltage begins to rise much more sharply (point C). This change in slope is caused by an increase in the internal impedance and signals that the battery is nearing its capacity to accept charge. The increase in impedance is due to fewer and fewer sites remaining on the positive electrode that can generate oxygen.

Overcharge

Eventually the continued application of current is no longer converted to stored energy in the cell. Instead, the oxygen overpotential at the positive plates is surpassed. Oxygen gas is produced due to the electrolysis of the electrolyte, and not by the reduction of cadmium hydroxide to cadmium. The electrolyte, composed of potassium hydroxide and water, changes hydroxide ions into oxygen, water and free electrons.

$$4OH^- \longrightarrow O_2 + 2H_2O + 4e^-$$

Equation 4: Anion Oxidation Reaction

The oxygen produced by electrolysis is quickly recombined in the electrolyte at the negative plates. However, a marked increase in cell temperature and pressure follows as the current input shifts from raising the cell's state of charge to generating oxygen gas.

The switch from generating oxygen at the plates to generating oxygen in the electrolyte also causes a sharp drop in the cell's impedance, since it is easier to strip oxygen from the abundant hydroxide ions than from the scarcer cadmium hydroxide. This drop in impedance causes a corresponding drop in voltage, creating a peak in the cell voltage curve (point D).

Generating and recombining oxygen in the electrolyte are exothermic reactions. Overcharging a battery (point E) continues to generate oxygen gas, building temperatures and pressures. Forcing a battery to vent causes a loss of electrolyte, reducing battery capacity and damaging the cell. If the gas cannot vent quickly enough, the battery can explode.

Charging Concerns

Pressure

The gas buildup in nickel-cadmium cells is a problem when contemplating methods to charge batteries. Gas bubbles accumulate on the surface of plates, reducing the plate surface area and increasing impedance. Overcharging produces gas which, if not recombined quickly enough, can cause damaging pressures to build up inside a cell. Excess pressure causes a sealed cell to vent, resulting in a loss of electrolyte. As electrolyte escapes through repeated venting, the capacity decreases and impedance increases as it becomes tougher to transfer ions between plates.

Temperature

Exothermic heating contributes to shortened battery life by increasing the possibility of venting, the principle source of low battery life. Nickel-cadmium batteries also have a negative temperature coefficient, meaning an increase in the ambient temperature by a hot cell reduces the no-load voltage of the surrounding cells.

Memory Effect

Under normal use (i.e., complete cell discharge) the crystal size on the cell plates remains small. If the nickel oxyhydroxide is not completely converted back into nickel hydroxide during a partial battery discharge, the nickel oxyhydroxide crystals will clump together, forming larger crystal structures. This crystal size change is the cause of the memory effect in nickel-cadmium batteries.

Cell Shorting

Using low rate constant-current trickle charges, crystalline fingers, or dendrites, can propagate through the plate separators and across the cell plates. In severe circumstances, these crystal dendrites can partially or completely short-circuit a cell internally.

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Conventional Chargers

The majority of chargers try to avoid the problems associated with overcharging by applying a low current charge. Nickel-cadmium cells have a natural charge decay rate of about **C**/30 to **C**/50 if left undisturbed. A nickel-cadmium cell can accept a low rate current of **C**/10 or less for extended periods (18 to 22 hours) without excessive gassing or heating. A low rate constant-current charger can apply a low trickle charge current for as long as the battery remains connected to the charger. As the cell slowly charges, it can radiate heat to lower temperature surrounding areas.

The problem with trickle chargers is that they are fairly slow. For example, the capacity of the cell determines exactly how slow: a one ampere/hour cell on a **C**/10 charge takes 10 hours or more. Continued recharging with slow rate currents also causes dendrite formations to occur. Most trickle chargers even apply a charge without any feedback control to monitor temperature or voltage in case of an emergency shutdown.

Voltage Termination

Chargers employing a feedback control mechanism are much safer to operate. Some feedback systems monitor the battery voltage, some watch the cell temperature, and others are timer controlled.

The most distinctive parameter to monitor is the peak in the cell voltage that occurs as the cell transitions from charge to overcharge. Many chargers look for a negative change in voltage ($-\Delta V$) and terminate charge at that point. Others look for a certain voltage threshold and stop charging at that point.

Problems occur if batteries are composed of unmatched cells since each cell has its own characteristics. The voltage monitoring methods are inappropriate for unmatched cells, since the voltages of different cells in a battery pack are often inconsistent with each other. Battery voltages can vary 5% with a 25 °C variation in ambient temperature, and the internal imbalances, impedances and levels of precharge will vary from cell to cell.

Temperature Termination

Another way to recognize full charge involves sensing cell temperature. Batteries typically reach about 45 °C to 50 °C at peak charge. Another method is to monitor the temperature gradient between the inside and outside of a battery pack and terminate at some predetermined threshold.

In either case, though, the battery will be undercharged at high ambient temperatures or damaged at low temperatures due to the negative temperature coefficient of nickel-cadmium cells. Variations in unmatched cell charge acceptance cannot be monitored with any accuracy since there is no way to tell if a particular cell out of several cells has reached its full charge. Also, the battery pack manufacturer must place the thermal sensors in the appropriate position inside the pack.

The goal of the **ICS1700A** QuickSaverII Controller is to quickly and safely charge a nickel-cadmium cell without stressing the cell. Solving some of the problems associated with rapidly charging a nickel-cadmium cell requires a controlled application of the charging current to the cell, as well as a careful monitoring of the cell's condition. These two requirements are met by using a pulsed current to charge the cell and a mathematically-derived first derivative of the battery voltage to watch the cell's state of charge.

The QuickSaverII Charge Method

The **ICS1700A** QuickSaverII Controller employs a unique method of charging batteries that solves some of the problems raised previously. This method, patent pending, consists of a positive current charging pulse followed by a high-current, short duration discharge pulse. The cycle, shown in Figure 2, is repeated until the batteries are charged.

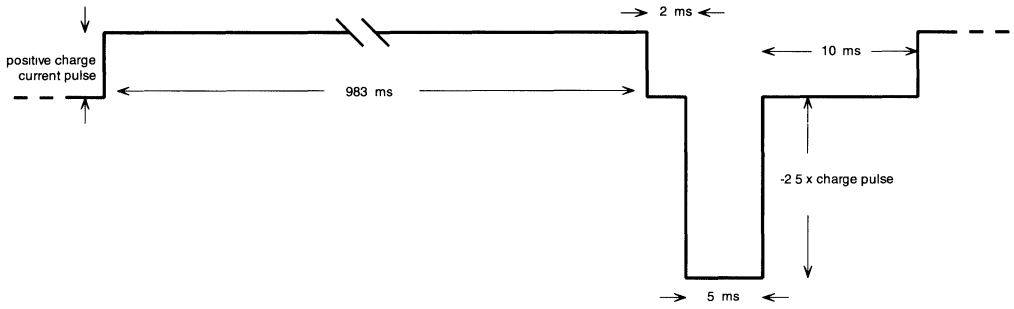

Figure 2: Reverse Pulse Charge Profile

The amplitude of the positive charging pulse is determined by the current capability of the power supply, the desired charge rate and the cell capacity. The **ICS1700A** is capable of controlling four user-selectable rapid charge rates of 4**C**, 2**C**, 1**C** and 0.5**C**, where **C** is the rated battery capacity in ampere-hours. These charge rates roughly translate into 20 minute, 45 minute, 1.5 hour and 3 hour charge times.

The discharge pulse has an amplitude set at -2.5 times the charging current. Thus the negative charge energy also varies as a function of cell capacity but remains a fixed ratio to the positive charge rate.

"Burping" the Battery

The primary purpose of the discharge pulse is to prevent the accumulation of gas bubbles on the cell plates. These gas bubbles are created under charge by the normal recombination of nickel hydroxide into nickel oxyhydroxide and cadmium hydroxide into cadmium.

The generated oxygen gas accumulates as bubbles across the cell plates, reducing the effective surface area and raising the internal cell impedance. Since the plate area is diminished, the time needed to completely charge the batteries increases.

The discharge pulse acts to "burp" a battery by stripping the bubbles away from the plates and assisting in the recombination of oxygen at the negative plates. This depolarizing process helps reduce the cell's internal pressure, temperature and impedance, turning the majority of the applied charge into stored energy instead of gas and heat.

The charge/discharge pulse cycle helps to restore the crystal structure of the cell plates by breaking down crystal formations, eliminating "memory" problems. The process also helps restore the crystal structure of the cadmium anodes. Reducing the effect of crystal size problems enhances the charging efficiency, allowing quicker charges at higher currents.

Trough Voltage Sensing

A 10 millisecond delay immediately follows the discharge pulse. No charge is applied during this delay, allowing the cell chemistry to recover. The **ICS1700A** reads the no-load battery voltage during this "quiet" window. The no-load voltage that is measured here contains less noise and is a more accurate representation of a battery's true charge state. Since no charging current is flowing, the measured cell voltage is not obscured by any internal or external IR drops or distortions caused by excess plate surface charge.

Maintenance Mode

Once the QuickSaverII Controller has determined that the cells under charge have reached a full charge state, it drops into a maintenance mode. The purpose of this mode is to keep the nickel-cadmium batteries primed at peak charge for later use. Since the charge on a nickel-cadmium battery naturally decays over time at a varying rate of **C**/30 to **C**/50, the maintenance mode provides a **C**/30 charge for as long as the cells are connected in the charger, and the charger is "ON."

The applied C/30 charge consists of the same charge/discharge pulse used in QSII fast charging, except the duty factor of the pulse sequence has been extended. For example, the same charge/discharge pulse that happens every second at a 2**C** charge rate would now occur every 60 seconds for a maintenance rate of **C**/30.

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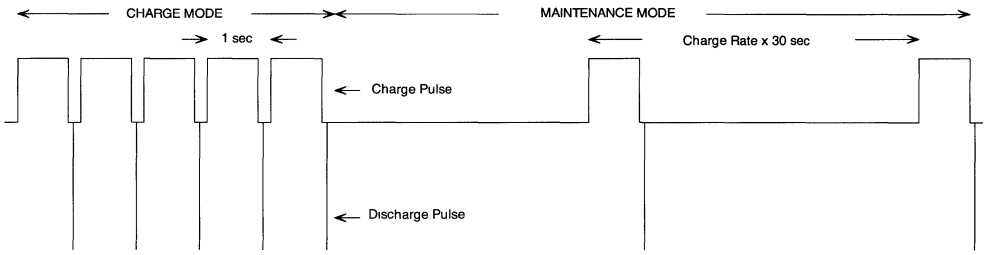

Figure 3: Charge and Maintenance Profile

The charge/discharge pulses in the maintenance mode prevent dendrite formations from propagating across the plates and separators, and helps maintain the crystal structure of the cell plates.

Slope Termination

By far the most distinctive point to look for is the peak in the cell voltage curve, indicating the transition from charge to overcharge. The voltage peak is characterized by a steep positive slope that flattens out, then turns sharply negative. By taking the first derivative (*dv/dt*) of the cell voltage, a second curve can be drawn showing the change in voltage with respect to time.

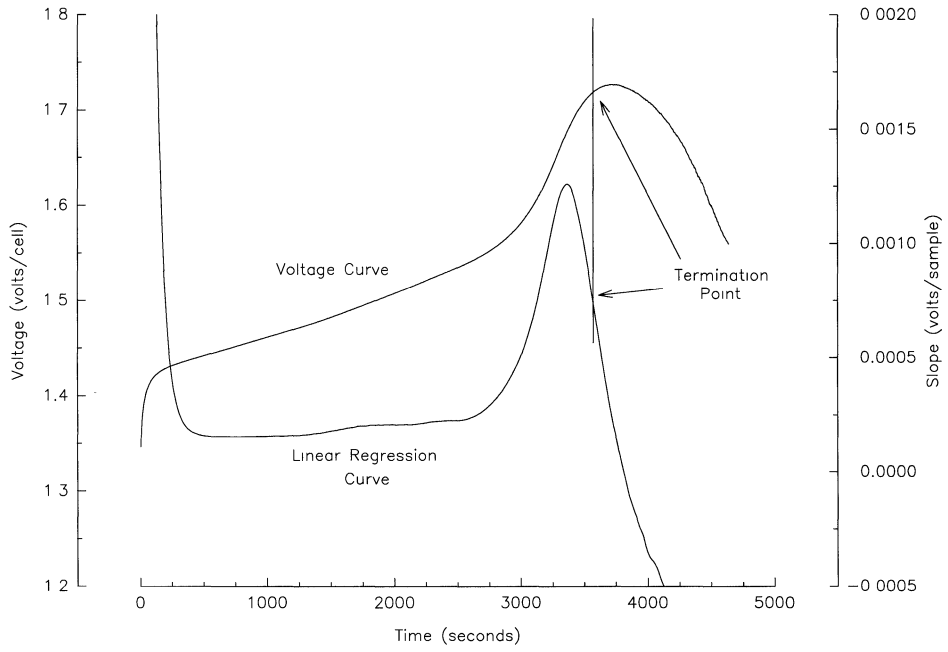

Figure 4: Voltage and Slope Curves with Termination Point

The first derivative will change its slope sharply in response to small perturbations in the cell voltage curve. This sensitivity to the cell voltage helps monitor changes in the voltages of individual cells. The first derivative, shown in Figure 4, will peak just before the actual peak in the cell voltage. The QuickSaverII controller can then accurately terminate charge before the battery begins overcharging.

To enhance the shape of the first derivative, a linear regression algorithm can find the best fit curve for any set of data points. The **ICS1700A** uses a linear regression formula to best fit the slope m in the equation for a line $y = mx + b$:

$$m = \frac{s\Sigma xy - \Sigma x \Sigma y}{s\Sigma x^2 - (\Sigma x)^2}$$

Equation 5: Linear Regression Formula

where s is the number of samples used in calculating the slope m, and x and y represent axis coordinates.

Chip Operation

The core of the **ICS1700A** is essentially a specialized reduced instruction set (RISC) microprocessor, optimized for efficient numerical calculations since the mathematics needed to derive the linear regression slope and to determine the correct termination point are fairly complex.

The controller uses a 10 bit successive approximation analog to digital converter (ADC) to change the measured analog voltages to digital voltage numbers. These voltage numbers are then averaged with successive numbers to create an average voltage number. The averaging process limits the effect of voltage jumps caused by battery and ADC noise. The number of successive voltage numbers used in the average depends on the charge rate.

An infinite impulse response (IIR) filter weights the averaged voltage number to filter out any large aberrations in the cell voltage curve. The filtered average is stored in a 12 sample first-in first-out (FIFO) queue. The twelve point FIFO holds the voltage numbers used to generate the slope.

QuickSaverII Termination Methods

The **ICS1700A** uses eight different techniques to determine when to end the charge, employing voltage monitoring, temperature sensing and timer cutoff methods.

1) The primary method monitors the linear regression slope of the battery voltage as outlined on Page 9. The charge is terminated and a maintenance mode begins when the slope reaches a derived cutoff threshold, shown on Figure 4. The derived threshold is continuously calculated from the start of the charge routine.

   Several requirements must be met, however, before the cutoff threshold can be correctly computed to avoid premature termination caused by anomalies in the different cells. Due to the sensitivity of the linear regression slope to the voltage curve, small variations in the voltage curve can cause large swings in the linear regression slope. This sensitivity to the battery voltage is especially useful in monitoring unmatched cells with different charge peaks.

2) Several unmatched cells may cause a battery charge curve to never reach a voltage peak. This condition occurs if some cells reach their individual peaks while others are still charging. A second method of charge termination watches for a few successive calculations of a negative linear regression slope which would indicate a diminishing voltage curve. The **ICS1700A** then discontinues charging and places these cells on maintenance.

3) If a charge is applied to a fully charged battery, the cell voltage will rise very rapidly since any applied energy becomes plate surface charge only and does not add any appreciable energy to the stored charge in the battery. The **ICS1700A** detects this rapid increase in voltage and quickly shuts off the charge routine to avoid overcharging. The cells are then placed on maintenance charge.

4) Overcharged batteries which have a charge immediately re-applied to them will show a sharp drop in cell voltage as a result of the change in the cell impedance. The voltage drop triggers a sharp decrease in the linear regression slope and will cause the **ICS1700A** to quickly drop into a low current maintenance mode.

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5) After several months of disuse some nickel-cadmium cells may exhibit a high impedance condition. This high impedance condition may not be noticeable until the battery is under full charge. Continued charging of these cells will create high temperatures and pressures in a battery that may have been weakened previously. The **ICS1700A** watches for these high impedance batteries and terminates the charge if the no-load voltage runs too high. It is recommended that these cells be replaced. The **ICS1700A** must be reset before charging another battery.

6) A battery sometimes contains cells that may be shorted internally due to dendrite growth or damaged separators. The **ICS1700A** attempts to detect these batteries before a long term high current charge is applied. A normal battery will jump to about 1.3 volts in response to an applied current. A shorted battery will remain below a preset threshold, indicating previously damaged cells. These cells should be replaced. The controller must be reset before another battery can be charged.

7) Failsafe termination utilizes the "deadman" timer which terminates charge after a preset amount of time in the unlikely event that the cell voltage curve never reaches a peak voltage nor descends in slope. The timer will time out after a certain period based on the selected charge rate. The charger must be reset before charging can continue.

8) The final method utilizes an end-user supplied thermal switch which will open circuit if the battery becomes too warm. Shutoff temperatures for nickel-cadmium batteries are about 45 °C to 50 °C to avoid unnecessary venting. It is strongly recommended that a thermal switch be used when charging nickel-cadmium batteries at high rates.

   Short circuit or open circuit charger contacts are detected before a full charge is applied to avoid harming the charging circuitry. A high current pulse is applied to the contacts with the resulting voltage compared to preset thresholds. If the voltage never rises, or rises too high, a contact fault is presumed. The **ICS1700A** assumes that a battery has been misplaced against the contacts, and will reattempt to start a charge. At the end of this period the controller will quit trying and will have to be reset for further use.

Interfacing to External Circuitry

The **ICS1700A** requires some external components to control the clock rate and provide an indicator display (see Figure 5). The chip must be interfaced to an external power source that will provide the constant current required to charge a battery pack as well as a circuit that will sink a negative current discharge pulse.

The **ICS1700A** does not control the amount of current flowing into the battery in any way other than turning it on and off. **THE REQUIRED CURRENT FOR THE SELECTED CHARGE RATE MUST BE PROVIDED BY THE USER'S POWER SOURCE.** The external charging circuitry must provide a constant current at the charge rate that was previously selected. For example, to charge a 1.2 ampere hour battery at a 2C rate, 2.4 amperes of current would be needed.

The Charge and Discharge signals are active high, TTL compatible signals. In addition to being TTL compatible, the CMOS outputs are capable of sourcing current which can add flexibility when interfacing to other circuitry. A "high" on the "Charge" signal indicates that the constant current supply should be activated. A "high" on the "Discharge" signal indicates that the discharger should be activated.

Care must be taken to control wiring resistance, and the load resistor must be capable of handling this short-duration high-amplitude pulse.

LED indicators can be connected to the device to display the charge mode and any fault conditions. The device has three outputs for driving external indicators. The three indicator outputs have open drains and are designed to be used with LED indicators. Each output can sink over 20 mA which requires the use of an external current limiting resistor. The three indicator signals denote battery fault, charge mode and over temperature.

The battery fault indicator is activated whenever a battery with low charge slope or a high impedance is detected. Either one of these faults indicates a defective battery. The low charge slope failure indicates that the battery is not accepting charge normally. It is detected by a very slow rise in battery voltage during the first twenty seconds of charge. The high impedance failure is detected by very high charging voltage during the first twenty seconds of charge.

The battery fault indicator is also activated when a poor contact between the charger and the battery is detected. It may also activate if the charge terminals are short circuited or if a battery pack has several shorted cells. In the event that a contact fault is detected, the controller will retest twice per second for a good contact for a total of 10 seconds. If the contact fault is not cleared during the initial ten seconds of

charging, the controller will enter a quit mode and can only be restarted by momentarily opening the over temperature switch or by momentarily grounding the reset pin.

The charge mode indicator is activated continuously during charging. When the controller enters maintenance mode, the signal is pulsed on and off at a one half second rate.

The over temperature indicator is activated whenever the over temperature switch opens. This indicates that excessively high temperatures have occurred in the battery pack. The over temperature signal also issues a reset command to the microprocessor. If a fault condition occurs, it can be cleared by opening the over temperature line connected to the temperature switch contained within the battery pack.

The TS input connects to one side of the temperature sensor (thermal) switch. The other side of this switch connects to ground. The thermal switch should have a cutoff of 45 °C. The TS input has an internal pull-up resistor insuring a high logic level when the switch is open. The controller will not attempt to start a charge sequence unless this signal is low.

The S0 and S1 signals must be programmed by the user to inform the **ICS1700A** of the desired charge rate. Since the signals have an internal pull-up, no connection to V_{DD} is required to program a high level. When a low level is desired, the pin should be grounded. To program the S0 and S1 signals, refer to the table shown below (Table 1).

Table 1

S0	S1	RATE	TIMER	MAINT PULSE PERIOD
L	L	4C	18.75 min	160 sec
L	H	2C	37.08 min	80 sec
H	L	1C	72.3 min	40 sec
H	H	0.5C	141.6 min	20 sec

The normalized battery voltage is connected to the VIN pin. The battery voltage must be normalized to one cell. For example, if the battery consists of six cells in series, the VIN voltage must be equal to the battery voltage divided by six. This can be accomplished with two external resistors. The input impedance of the VIN pin is quite high, about 1 MΩ typically.

The RC pin is used to set the frequency of the internal clock. A 16KΩ resistor is connected between this pin and V_{DD}, and a 100pF capacitor is connected between this pin and ground. The frequency of the internal clock is 1 MHz.

The reset pin is provided to restart the charge sequence. An external 1 µf capacitor should be connected to this pin and ground to provide a power-on master clear signal. In addition, a diode should be connected from this pin to the + 5V supply to discharge the capacitor in the event of a momentary power interruption. This pin has a Schmidt trigger input which protects against slowly rising voltages. A reset is required to clear a battery fault or contact fault condition or to exit the maintenance mode.

An external reference voltage is not required for the ICS1700A. An internal bandgap voltage reference (1.25V, nominally) is provided for battery and contact fault detection. **If a more precise reference is required, an external voltage reference can be used on pin 13 and this reference will override the internal bandgap reference**.

There are two ground pins. One pin is used exclusively to return the current that the LED drivers must sink. The pin is labeled LVSS and should have a direct connection to a ground point to avoid inducing ground bounce in the VSS ground. The ground for the rest of the circuitry is labeled VSS. Both ground points must have the same potential.

The "ICS1700A QuickSaverII Controller Evaluation Board Application Note" contains some additional, valuable information regarding interfacing with external components.

References

1) Sealed Type Nickel-Cadmium Batteries Engineering Handbook. Sanyo Corp., 1990.

2) Sealed Rechargeable Batteries Application Manual. Gates Energy Products, 1989.

3) Nickel Cadmium Technical Manual. Panasonic Industrial Co., 1989.

4) Benjamin, Fred. The Reflex Principle of Charging Nickel-Cadmium and Other Batteries. Gardena: Christie Electric Corp., May 22, 1972, pp 3-11.

5) Benjamin, Fred, et al. 6-in-1 Battery Sleuth - CASP with Reflex 2000 - The Ultimate Answer to Battery Problems. Gardena: Christie Electric Corp.

6) Benjamin, Fred. "System for 20-Min Recharging of Sealed Nickel-Cadmium Batteries." SMPTE Journal, 86 (April 1977) pp. 204-209.

7) Bailer, John, et al. Chemistry. 2nd ed. Orlando: Academic Press, 1984.

Notes: 1) Value of resistor determined by discharge current and capacity of battery pack.

2) Device must be logic level compatible.

3) Negative battery terminal and DC return should be connected at one point.

4) A thermal switch or thermistor can be used with the **ICS1700A**. Refer to the application note for the equivalent circuit diagram when using a thermistor.

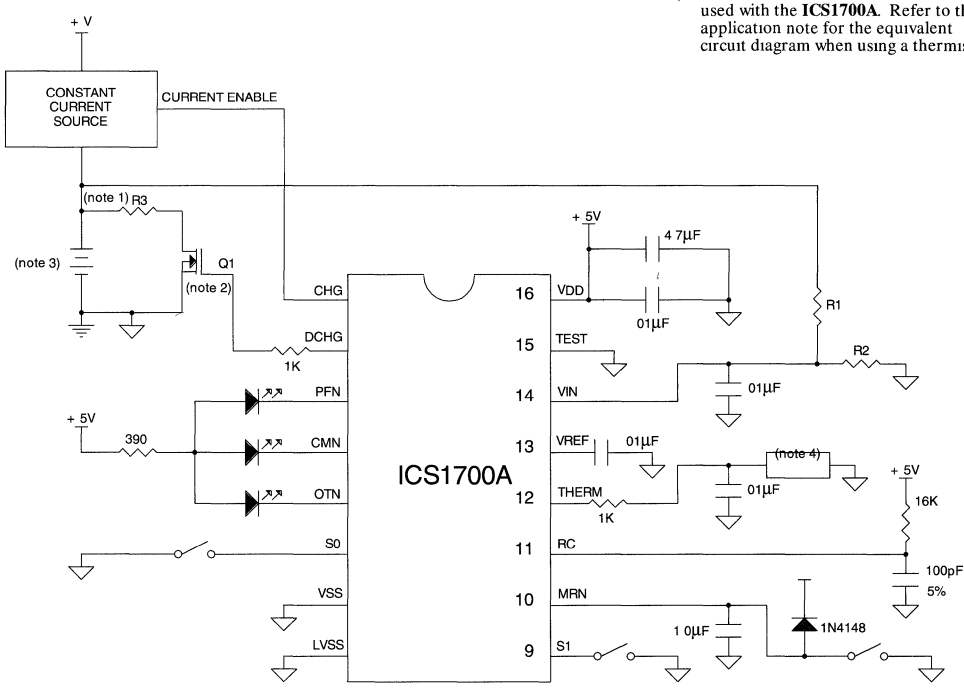
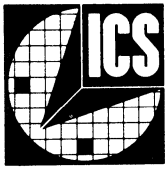


Figure 5: Functional Diagram



Integrated Circuit Systems, Inc.

REVERSE PULSE CHARGING - AN OVERVIEW OF CURRENT RESEARCH PROGRAMS

by
Tom Gosse'

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ABSTRACT

Recent research into the cycle life of rechargeable consumer cell NiCd batteries has produced interesting results. While the evolution of battery technology has accounted for increases in the total number of charge/discharge cycles, more dramatic results appear to be available with improvements in battery charging methodology. A study that compared inflection voltage termination in combination with reverse polarity charging pulses to negative delta voltage in combination with a constant current charge, provides preliminary data that suggests a 2X improvement in 'working' cycles.

INTRODUCTION

The market for mobile products powered by rechargeable consumer cell technology is growing at a significantly greater rate than the rest of the technology products market. At the same time formerly third order problems such as untethered operating time, battery reliability, consumer safety, and environmental correctness are fast becoming second and first order concerns of the product manager. Product designers are turning to intelligent power control to answer some of these questions. Smart micro controllers with consumer safety features built-in, offer a facile approach to fast charge, but the issues of overall run time and battery reliability must be examined in greater depth.

Integrated Circuit Systems (ICS) performed fast charge and discharge cycle testing from August of 1992 to March of 1993 using fast charge NiCd consumer cells. The testing compared two different charge methods. The results of this testing encouraged ICS to commission a study by THE STATE UNIVERSITY OF NEW JERSEY RUTGERS entitled "Reverse Pulse Method of Charging Alkaline Batteries". The discussion that follows covers background, philosophy, and method for both the ICS test and RUTGERS study.

Definition of Terms

In order to minimize confusion a brief definition of terms is necessary. Gates Energy Products defines various types of charging as a function of the C rate[1] . This is "the rate in amperes or milliamperes numerically equal to the capacity rating of the cell given in ampere-hours or milliampere-hours."[2] The simplest type of charger trickles current into the battery at a small fraction of the C rate, (e.g. C/20 full recharge in 36-48 hours). More complex chargers allow current to virtually pour into the battery at some multiple of C, (e.g. 4C full recharge in 15-20 minutes).

Table 1 below defines three methods of charging batteries. Recharge time is only an estimate based on battery temperatures <25°C and reasonable conversion efficiency from the constant current source. Fast charge will be the focus of this presentation.

METHOD OF CHARGING	"C" RATE	RECHARGE TIME (HOURS)
STANDARD	C/20 - C/10	36 - 16
QUICK	C/5 - C/2	7 - 2
FAST	1C - 4C	1 - .3

Table 1 - Methods of Charge

Fast Charge

The life cycle testing performed at ICS was conducted at a 4C charge rate and a 1C discharge rate with a cool down period between discharge and charge. The average temperature of the batteries at the start of each charge cycle was observed automatically by the system. The charge cycle could not start until the battery pack measured 25°C ±0.25°. The charge period was approximately 17 minutes for the inflection voltage with pulses and approximately 22 minutes for the -delta voltage, constant current method. Discharge was performed into a known load and was approximately 1 hour each time.

Fast Charge Techniques

Fast charge techniques are comprised of two main elements: terminating the charge and delivering the energy. A brief look at these elements and comparison of their features will facilitate the discussion.

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[1]Gates Energy Products APPLICATION MANUAL for SEALED RECHARGEABLE BATTERIES; Section 3.2; pp53-80.
[2]op cit p53.

Termination

When fast charging sealed consumer cell batteries two internal characteristics provide the necessary information for charge termination - battery voltage and temperature. The absolute value of both of these variables change when the battery is under charge. Cell voltage and temperature can be measured externally to provide termination data. A summary of several termination approaches for voltage and temperature is germane to this primer. Figure 1 compares voltage and temperature termination to internal cell temperature and pressure when fast charging. (Notice the rapid rise in the temperature and pressure component after the voltage infection point.)**

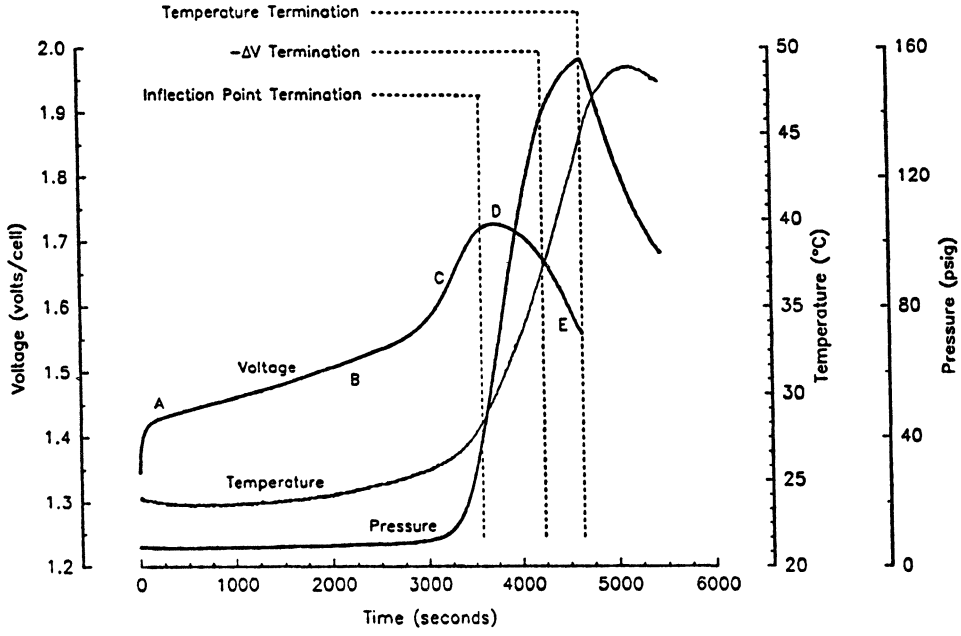

Figure 1
A comparison of various termination methods at 1C

** Data for Figure 1 has been accumulated over the past 2 years by testing a large variety of rapid and standard charge batteries from a number of manufacturers. The pressure and temperature data is actual and was acquired using pressure transducers inserted in the battery and temperature sensors in the pack.

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A comparison study of voltage based termination methods includes *dV/dt*, *-dV*, and V_{max} so that a conclusive analysis can be performed. *dV/dt* type charge termination is a relatively complex mathematical calculation of the first derivative of voltage through the use of a linear regression formula[3]. This terminates the charge at the voltage inflection when the cell has reached ~98% of full charge voltage. This point of inflection is prior to a transition into cell overcharge.

-dV and V_{max} are far simpler termination methods using either a comparison to cell voltage at the start of charge or a maximum voltage threshold referenced to an external open circuit voltage level.

Figure 2 below highlights the voltage inflection and the negative voltage and maximum voltage points can be seen as well. In the study performed by ICS discussed in this paper we compared only *dV/dt* and *-dV*. The amount of negativity was set at -7 millivolts per cell.

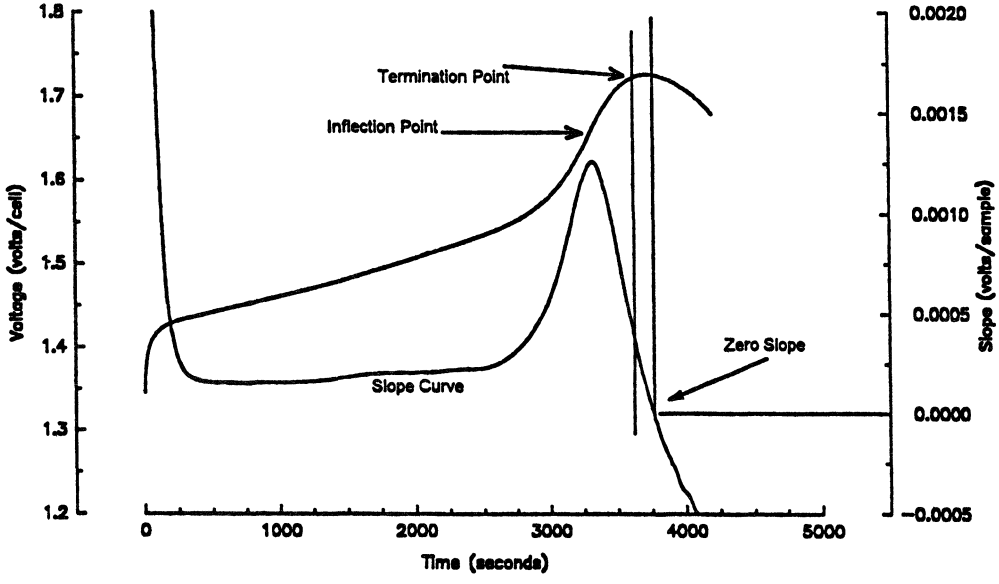

Figure 2.
A comparison of voltage termination methods.

[3] To enhance the shape of the first derivative, a linear regression algorithm can find the best fit curve for any set of data points. ICS uses $y = mx + b$: $m = s\Sigma xy - \Sigma x\Sigma y / s\Sigma x^2 - (\Sigma x)^2$, where s is the number of samples used in calculating the slope m, and x and y represent axis coordinates.

Termination of charge using the temperature method is predicated upon the internal heat generated by the cell as it approaches full charge. This method requires monitoring of both the cell temperature and compensating for ambient temperature differences. Similarly to voltage, several varieties of temperature methods can be employed to terminate a fast charge, *dT/dt*, *dT*, and T_{max}.

In a small measure *dT/dt* can be likened to *dV/dt* because of the requirement for constant sampling of the temperature so that a representative curve can be obtained. It is quite different though when comparing the volatility of the two variables. The cell temperature will generally rise more rapidly than ambient as it approaches the charge/overcharge transition point. However fast charging hot or cold batteries (as defined by the manufacturer's specifications) can be quite a nasty experience and some method of understanding the batteries pre-charge temperature should be included in any temperature based scheme.

dT which terminates the charge upon detection of a crossover temperature point when compared to a 'dummy' thermal mass in the battery and T_{max} which essentially shuts off the charge after the battery reaches a fixed temperature can definitely be affected by the hot/cold battery problem. Figure 3 below shows some typical temperature slopes for NiCd and NiMH battery types.

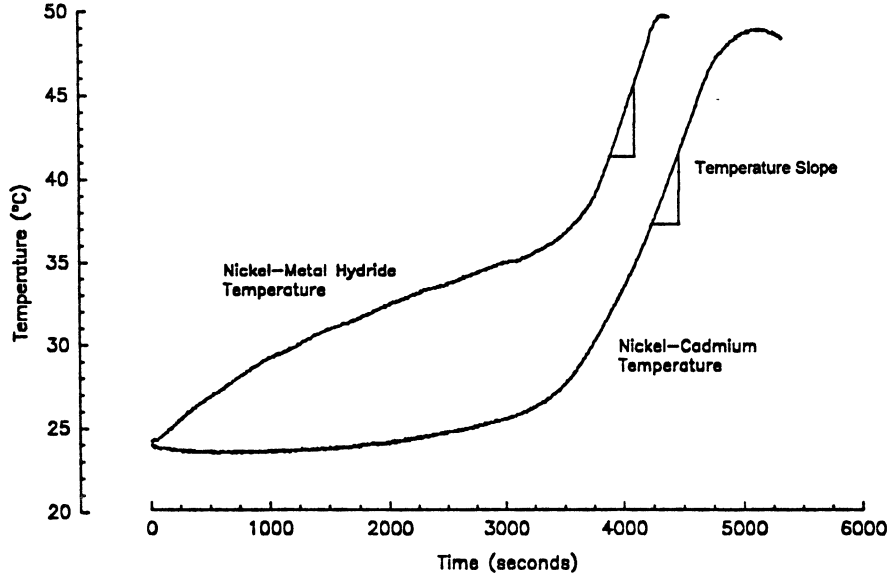

Figure 3.
dT/dt curves for NiCd and NiMH batteries.

Charge Current

Another component of fast charging sealed consumer cell NiCd batteries is to provide a current source. In the first tests that ICS performed we compared *constant current* with *reverse polarity pulsing current*. There is also *positive pulsing current* that can be used to charge batteries. In Figure 4 the various components of each of these three applications of current are presented.

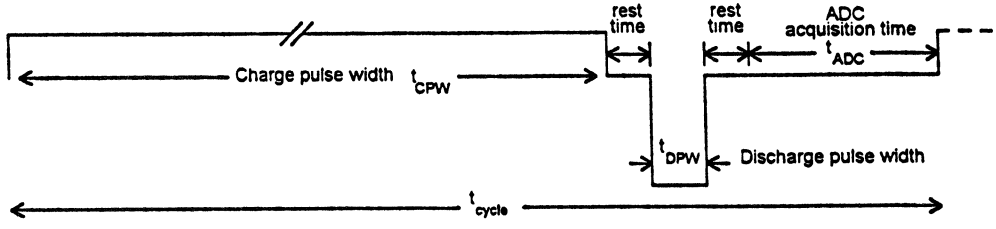

Figure 4.
The application of current during charge.

A *constant current* charge consists of a continuous application of current to the negative electrode. *Reverse polarity pulsing current* consists of a forward bias and reverse bias current pulse. While *positive pulsing current* is the application of forward bias current in an on/off pattern.

ICS uses a specific *reverse polarity pulsing current* pattern that is represented from start to finish in the one(1) second segment shown in Figure 4. This pattern is based primarily on the Christie Electric reFLEX® principle put forth by Fred Benjamin in a paper entitled "THE reFLEX PRINCIPLE OF CHARGING NICKEL-CADMIUM AND OTHER BATTERIES"[4] circa 1976. (ICS is the exclusive licensee of Christie patent 4,746,852 for incorporation into integrated circuit devices.) The pulse pattern is composed of three main elements: a forward bias current, a high current reverse bias discharge, and a rest period. This pattern is repeated throughout the charging sequence, with battery voltage measurements taken once every second, within the rest period.

The discharge pulse is set at -2.5X the charge rate, e.g. a charge rate of 1C (1 hour) for a 1.2 ampere-hour battery would be discharged at -3A, so that the desired effect of the pulse can be assured every time. Regularity is an important feature of this method and allows for consistent voltage readings and good charge efficiency. The -2.5X discharge is

[4] Excerpts from "THE reFLEX PRINCIPLE OF CHARGING NICKEL-CADMIUM AND OTHER BATTERIES" F. Benjamin; pp.3-11, along with notes from the ICS data sheet for the ICS1700 QuickSaver™ CONTROLLER for NiCd Batteries.

intended to momentarily reverse the gas bubbling effect of the charge process, incrementally reducing internal heating and associated pressure effects. It is also believed to promote charge efficiency by way of temporarily reducing the surface resistance to charge of the positive nickel plate.[5]

Simple *pulse current* charging does not have the same effect on the battery because the stress relief in the opposing direction is not present. In many instances in the past, on/off pulses were misconstrued to mean the same thing as reverse polarity pulsing, but there are significant differences that can actually be felt when charging the battery at high rates 15-30 minutes or less.[6] In fact, the average temperature of cells charged with this method in ICS testing was less than 3°C above ambient compared to an average of 3X that for cells charged with constant current.

Research Program

In 1991 ICS executed a license agreement with Christie Electric Company of Gardena California that permitted ICS to incorporate the principle features of the Christie CASP apparatus into a single mixed signal integrated circuit. Upon completion of the development of this IC, and a test configuration that would provide substantive battery charging data, ICS began to accumulate data on batteries at various high rate charges. The initial data was taken over a relatively short number of consecutive cycles to understand the actual temperature changes, final capacity at termination, and operational mysteries of the Christie machine interpreted into an algorithm.

Subsequent testing saw the incorporation of the internal pressure measurement. This measurement became available when it was discovered that there was a small gap at the bottom of most sealed cells that could be tapped and a pressure transducer inserted and soldered into place. A GPIB data acquisition system that had heretofore been used only for temperature and voltage information was formatted to accept and plot pressure data as well. A summary of this data is shown in Figure 1.

Preliminary Life Cycle Testing

Further expansion of the GPIB system led to the development of a 'life cycle test plan'. This plan took twelve new, rapid charge batteries, purchased through a battery distributor, and subjected them consecutive charge and discharge cycles until they fell below 50% of their specified minimum capacity. The batteries were made into two 6 cell battery packs, with all cells connected in series. A thermal switch was inserted into each pack for safety and a thermistor was also inserted to record pack temperature during charge and discharge. Each pack was cycled ten times at a C/10 rate for cell conditioning.

[5] F. Benjamin, op cit, p. 5.
[6] F. Benjamin, op cit, pp. 5-6, and excerpts from ICS lab notes on battery charge testing at high rates.

The charge rate was 4C and charge time averaged 17 minutes for the reverse polarity pulse charge and 23 minutes for the constant current charge. The discharge rate into a known load was 1C, based on the manufacturer's specification. There was a cool down period of 15 minutes provided for each pack between charge and discharge such that neither pack started the charge cycle at a temperature higher than ambient. Testing began in August of 1992 and concluded in March of 1993.

Results

The results of this testing was that a significant improvement in the number of charge and discharge cycles could be seen in one method over another. This was an important first step because most of the published information from the battery manufacturers indicated the opposite. In fact, most of the manufacturers purported to get 500 cycles using conventional trickle charging. The results of the graph on the next page show that fast charging gives you a higher target to shoot at and that critical components of the charging methodology may improve that target as well.

Rutgers Plan

In order to further exercise this theory of charging techniques ICS has contracted Rutgers University in New Jersey to perform more extensive testing on larger numbers of cells. Their test proposal will include all of the elements discussed above along with a destructive physical analysis of the cells at 10, 100, and 500 cycles. The purpose of this analysis is to examine the actual effect of the charge and discharge process on the electrodes, separators, and internal physics of the battery. Since this paper is being written in August, some of the early results of this testing will be available at the PCIM conference in October.

The goal of the test plan is to develop an *inside the cell* picture of the stress induced by charging and discharging a battery. A detailed examination of both the nickel and cadmium electrodes will be performed through a testing lab associated with Rutgers in an attempt to determine if the constant application of current is detrimental to the electrodes and separator and conversely if the application of current and a reverse pulse provides a positive effect to electrodes and separator.

Simplifying Dual Voltage PCMCIA Power Switching

Most new notebook PC designs incorporate support for two PCMCIA interface cards. The PCMCIA spec (release 2.01) supports both 5V and 3.3V cards.

After card insertion is detected, the VCC pins (pins 51 and 17) go from their initial state of no power to 5V. The card is then interrogated to determine whether the card's operation should be at 5V or 3.3V by reading the card's identification ROM tuples.

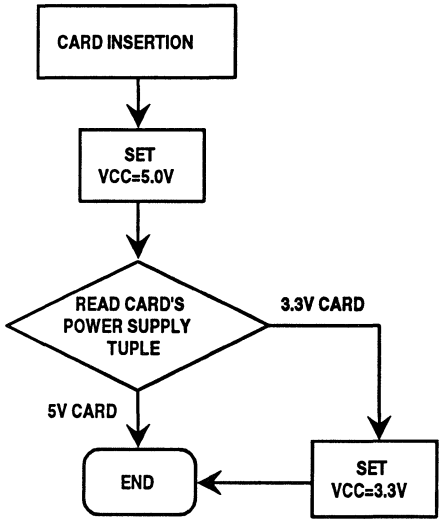

Figure 1. PCMCIA Power-up Sequence

If a 3.3V supply requirement is read from the card, the system is required to drop the card's power supply from 5V to 3.3V. This requires power switching on the VCC line.

Therefore, two power switches are required per socket, one switch for 5V and one for 3.3V as shown in figure 2.

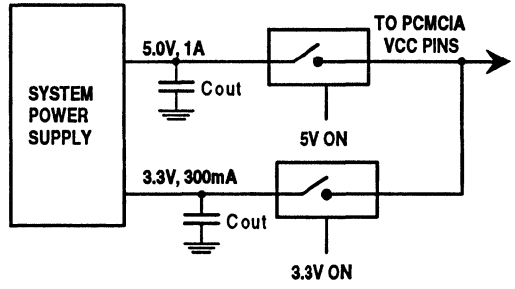

Figure 2. PCMCIA VCC Switching

The 5V line may be called upon to supply significant (>1A peak) power to run disk drives, LAN cards etc. 3.3V power requirements are typically much lower, (300mA max.) since the overwhelming majority of 3.3V only cards anticipated are semiconductor memory cards.

In figure 3, discrete P-Channel power MOSFETs are chosen for the 5V switching, since they provide low R_{DSON} with 5V enhancement. The AV9312 or AV9512 offer a compact and economical solution for switching the 3.3V, with both channels being handled in a single SOIC package with no external components. In addition, the AV9312 and 9512 have 1mS rise time, ensuring no glitching to the system supply when the switch closes. The 5V MOSFET switches are slowed down with external R and C to avoid high switching currents when charging the external card's capacitance.

The AV9512 is designed to work with VCC at 5V and works with CMOS input logic levels. If the PCMCIA controller runs from a 3.3V supply, the AV9312 would be used and level translation will be required for PMOS switches Q1 and Q2 (fig 4).

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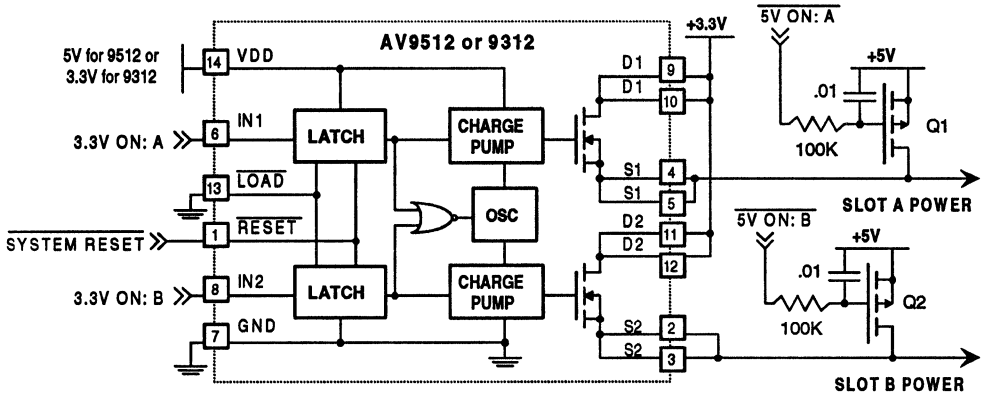


Figure 3. Complete Schematic for Dual Slot 5.0V or 3.3V PCMCIA V_{CC} support

Figure 4 shows translation from 3.3V signals to the 5V switches with slow rise time, assuming the command signal is active low. If load capacitance is small, rise time control may not be necessary and D1, R2, and C1 can be eliminated. Q1 and R1 can be replaced by a non-inverting 3.3V to 5V buffer if available.

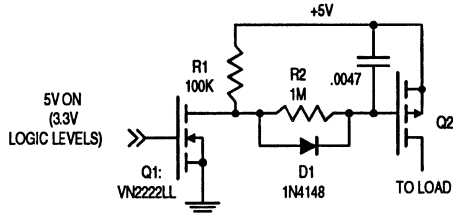


Figure 4. 3.3V Logic Level to PMOS Drive with Rise-Time Control

A simpler solution to the 3.3V translation problem uses a single 9304 for each PCMCIA card slot (Fig. 5). Three Channels of the switch are paralleled for the 5V switching to increase current handling capability to 1.5A and reduce R_{DSON} to below 100mΩ

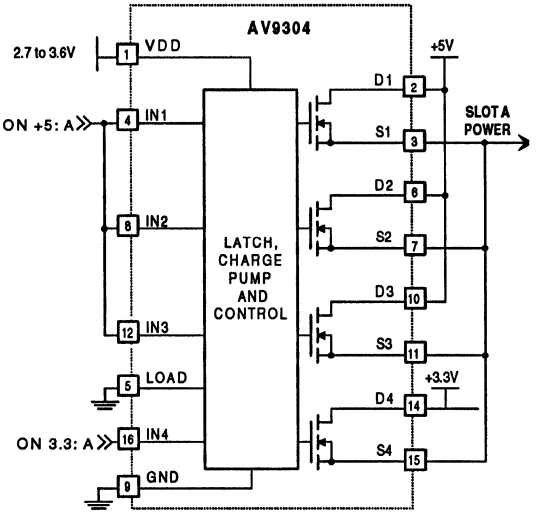


Figure 5. 3.3V Logic Level input PCMCIA Power Switching - Minimal Component Usage

In all of these circuits, the control logic should *never* command both the 5V and 3.3V switches to be on simultaneously. A simultaneous "on" command would cause substantial current to flow from the 5V to the 3.3V power supplies and damage the power devices.

ICS

Communications

Products

In addition to the Caller ID product offering in this issue, ICS is applying its unique High Performance mixed signal CMOS technology to a new market - Communications. Applying our extensive Frequency Synthesis capability to communications systems clock and timing applications will allow ICS to offer this market a new level of system performance. These advanced products are in process now, with data sheets available in the near future. Contact ICS for further information.

ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. ICS reserves the right to change or discontinue these products without notice.

Integrated Circuit Systems, Inc.

ICS1660

Incoming Call Line Identification (ICLID) Receiver with Ring Detection

Description

The **ICS1660** "ICLID" circuit is a monolithic CMOS VLSI device that decodes and detects the Frequency Shift Keying (FSK) signals used in caller identification telephone service. The **ICS1660**, when used in conjunction with some external components, amplifies, filters and demodulates the FSK data transmitted from the central office to the telephone subscriber.

The **ICS1660** detects the first power ring signal and demodulates the 1200 baud FSK data transmitted during the silent interval between the first and second power ring. The FSK data is transmitted from the central office switch to the subscriber line as part of the CLASS service of Calling Number Delivery (CND). This data is then demodulated, amplified and filtered by the **ICS1660** and digitally transmitted to the host controller/processor.

The **ICS1660** is designed to be powered by any off-the-shelf 9.0 volt battery. The on-chip 5.0 voltage regulator powers the host microprocessor and any external circuitry supported by the **ICS1660**. This portion of the circuit can be overridden by connecting the V_{IN} pin (18) to the V_{DD} pin (1) for a common power supply. A low battery detection circuit is also provided on-chip and signals the microprocessor on the FSK/BAT pin (17) when the PWR pin (16) input is pulled low.

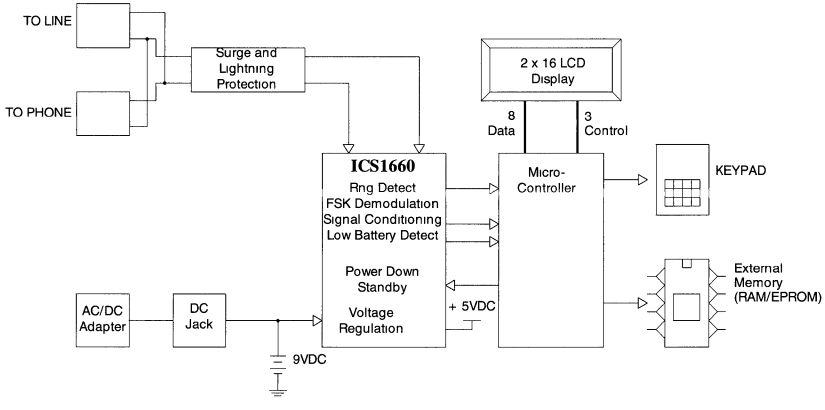
Features

- Ring Detection
- Low Battery Detection
- Internal 5V Regulator - can externally source 25mA
- FSK Demodulation
- Powerdown in Standby Mode
- Direct Interface to Host Microprocessor or Microcomputer

Applications

- Telephones
- Facsimile Machines
- Modems
- Telephone Interface Equipment
- Stand-alone ICLID products

ICLID Block Diagram



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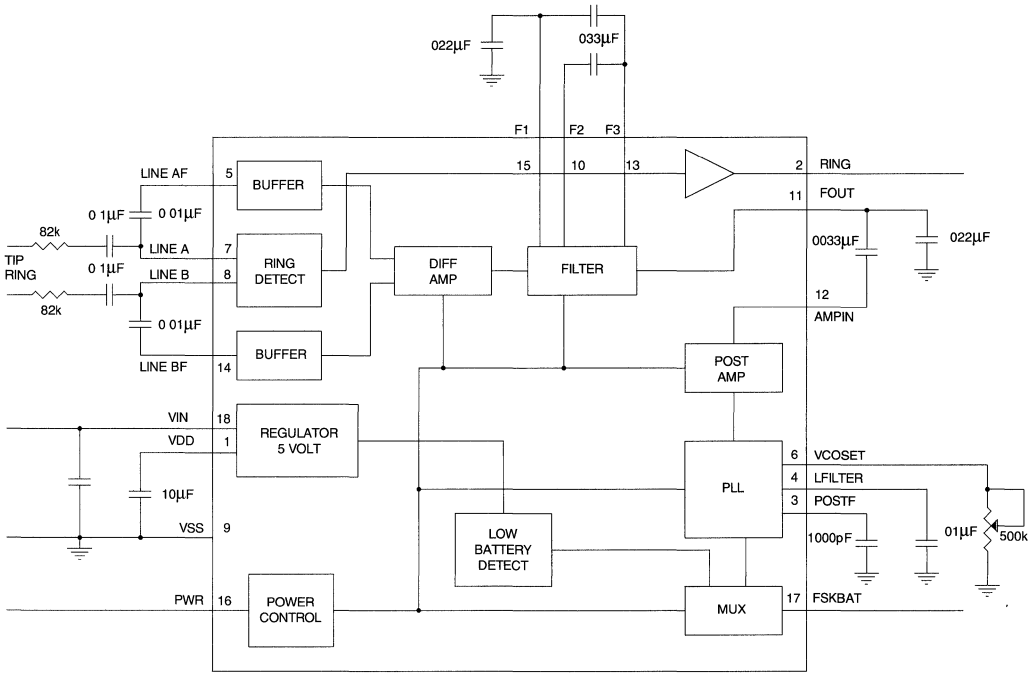
Block Diagram



Function Description

Power Supply

The **ICS1660** is designed to be powered by a standard 9.0 volt battery. The chip contains a voltage regulator that powers external circuitry and provides the supply voltage for all digital I/O on the circuit. This allows easy interface between the **ICS1660** and other standard logic working at 5.0V. This regulator has short circuit protection and requires an external filter/compensation capacitor with a minimum value of 10uf.

In the event that an external regulated 5.0V supply is available, the V_{IN} and V_{DD} pins can be shorted to permit the entire system to work from a common supply.

A low battery detection circuit is provided. This circuit is designed for a typical trip point of 6.0V with hysteresis of about 200mV above the trip point. This signal is low active and is multiplexed to the FSKBAT output pin when the PWR input is low.

In an effort to keep power dissipation to a minimum and extend battery life, most of the analog circuits are turned off when the circuit is at rest waiting for a ring detect, (PWR pin low). During this time only the regulator, low battery detect, reference generator, and ring detect circuits are active. When the PWR pin is high, all circuits are active.

Ring Detect

As shown in the attached block diagram, the LINEA and LINEB inputs should be connected to the telephone line through external 82KΩ resistors and 0.1uf capacitors. This provides DC isolation and sets up a voltage divider with internal resistors that will detect 35.0V RMS typically. This voltage is applied across the LINEA and LINEB inputs. The design value of the internal resistors is 8.1KΩ ± 20% with relative accuracy of 2%. The RING output is high active.

Differential Front End

As shown in the attached block diagram, the LINEA and LINEB inputs go into a differential amplifier which in turn drives a filter. All resistors are internal to the chip while capacitors are connected as shown in the block diagram. After filtering, the signal is AC coupled into a high gain amplifier that converts the signal to digital. This digital signal in turn acts as the reference frequency for the phase comparator section of the phase locked loop.

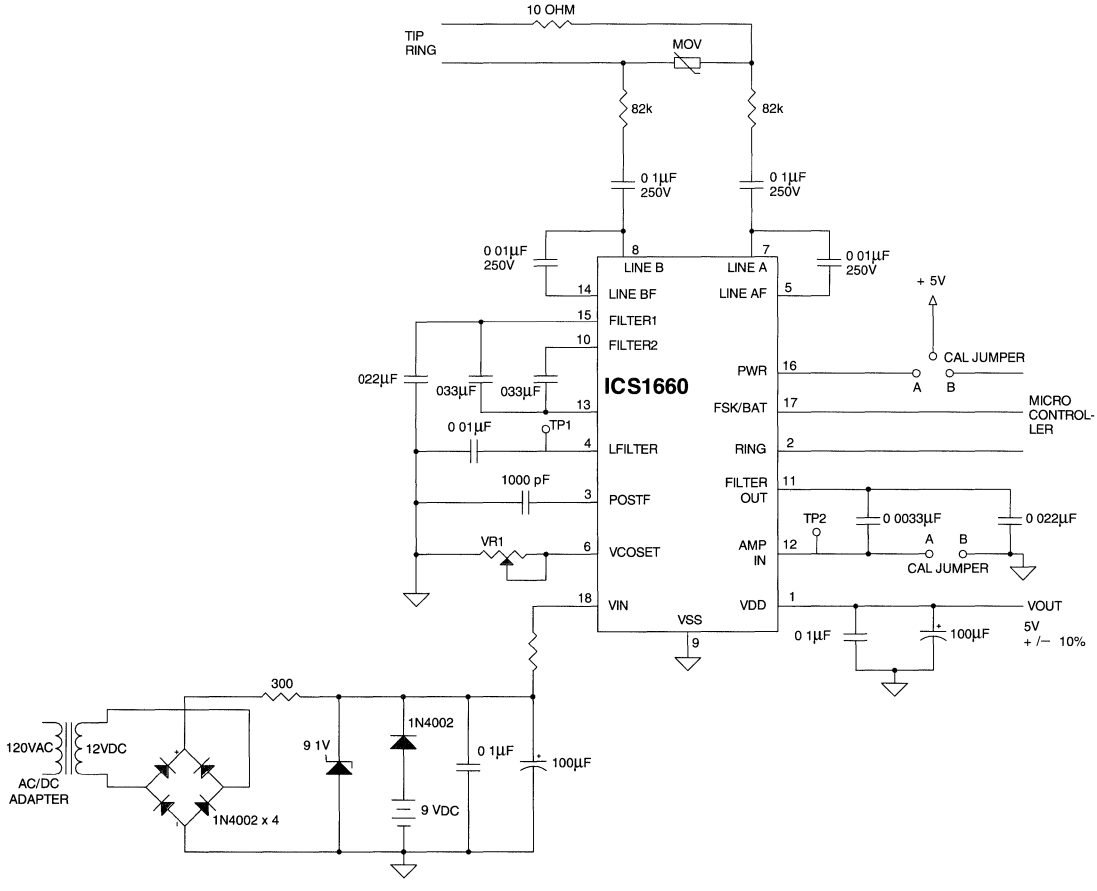
FSK Demodulation

After the signal from the telephone line has been filtered, amplified and converted to digital, it acts as an input to a phase locked loop. This PLL does FSK demodulation. The summing amplifier shown in the block diagram provides a signal to the VCO that should be about 0.5V for MARK frequency (1200 HZ), and 2.0V for SPACE frequency (2200 HZ).

As shown in the block diagram, the LFILTER (loop filter) output has a post filter attached to it. This POSTF signal is sent to a comparator. The other side of the comparator is set to approximately 2.5V. This comparator has a small amount (200 mV) of hysteresis and its output is the demodulated FSK data. The FSK output is high for MARK frequency and low for SPACE frequency. FSK data is multiplexed out of the FSKBAT pin when the PWR input is high.

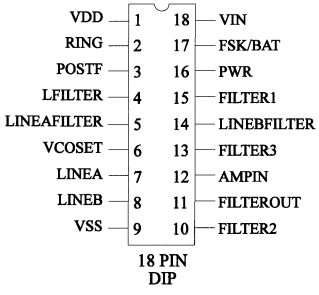
The VCO frequency is set with one external resistor with a value in the range of 300K for a center frequency of 1700 HZ. The lock range will be 660 HZ to 2630 HZ typical. The center frequency reproducibility will be ± 15%. The center frequency can be adjusted in the system by connecting AMPIN to VSS, PWR to VDD, and adjusting the external resistor for 1700 HZ. This frequency can be observed at the LFILTER output or the FSK/BAT output.

Typical Application

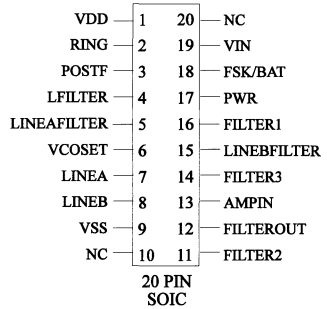


Pin Descriptions

PIN NUMBER DIP	PIN NUMBER SO	NAME	DESCRIPTION
1	1	VDD	Supply voltage pin to external circuits. Output of 5.0 volt regulator.
2	2	RING	Ring detect output signal to the host microprocessor.
3	3	POSTF	Post loop filter signal used by demodulator.
4	4	LFILTER	Loop filter for PLL.
5	5	LINEAFILTER	Filter input from line "A."
6	6	VCOSET	Center frequency adjustment pin.
7	7	LINEA	"Tip" input from telephone line.
8	8	LINEB	"Ring" input from telephone line.
9	9	VSS	Ground.
10	11	FILTER2	Active filter pin.
11	12	FILTEROUT	Active filter pin.
12	13	AMPIN	Input from active filter.
13	14	FILTER3	Active filter pin.
14	15	LINEBFILTER	Filter input from line "B."
15	16	FILTER1	Active filter pin.
16	17	PWR	Logic input signal to switch from low current standby mode.
17	18	FSK/BAT	Multiplexed output signal controlled by PWR pin. In standby mode, this is a low battery (active low) signal. During FSK demodulation, this is the data line to the µP (mark = high).
18	19	VIN	Input power supply pin.
10	20	NC on SOIC	



18 PIN DIP



20 PIN SOIC

Ordering Information
ICS1660N (DIP Package)
ICS1660M (SOIC Package)

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Input/Output Specifications

Digital

RING and FSKBAT outputs are standard CMOS outputs with voltage swings between V_{SS} and V_{DD}.

PWR is a logic input. A level converter circuit is on chip to allow the logic signal that swing between V_{SS} and V_{DD} to be internally converted to signals that swing between V_{SS} and V_{IN}. It should be noted that to minimize power consumption caused by through current in logic gates, the PWR input should always swing to within 100 mV of V_{SS} or V_{DD}. The PWR input signal is low when the **ICS1660** is in lower power mode waiting for an incoming call.

The LFILTER output is a standard CMOS output powered from VDD. This output has an internal resistor with a typical value of 30KΩ. This is used in conjunction with the external capacitor shown in the block diagram to form the loop filter for the PLL.

Analog

The value of the ring detect is as previously discussed 35.0V RMS typical. The actual value is set by the choice of the external resistors that are connected to the LINEA and LINEB inputs. The matching of these resistors to the internal 8.1KΩ resistors is also a factor. The signal level at the chip that will cause a ring is the bandgap voltage, (1.25V) or below.

The chip is designed for an input signal level of -12.5dbm to -28.5dbm into 900 ohms. This translates to a signal that is between 100 mV and 636 mV peak to peak.

The filter section should be connected as shown in the block diagram. Using the external capacitors as shown, and assuming nominal values on the internal resistors, the corner frequencies are 900HZ and 3860HZ.

An external resistor with a value of approximately 330KΩ is connected between the LFILTER and POSTF pads. This resistor along with the external capacitor shown in the block diagram form the post filter. This post filter is used in conjunction with the comparator to do the FSK demodulation.

Absolute Maximum Ratings*

(Voltages referenced to V_{SS})

Supply Voltage	V_{IN}	-0.5V to + 10V
Voltage at any Input		-0.5V to V_{DD} + 0.5V
Operation Temperature Range		-55 °C to + 125 °C
Storage Temperature Range		-50 °C to 150 °C

* Absolute maximum ratings are those values beyond which the safety of this device cannot be guaranteed. These values are NOT RECOMMENDED operating conditions.

DC Characteristics

V_{IN} = 4.5V - 10.0V; T_A = 0 °C - 70 °C, Recommended Operating Range

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
I_{IN}	Standby Current	-	20	30	uA	PWR LOW, V_{IN} = 9.0V, I_{DD}= 2µA
I_{IN}	Active Current	-	-	10	mA	PWR HIGH, V_{IN}= 9.0V VCOSET= 300K
V_{DD}	Regulator Output Voltage	4.5	5.0	5.5	Volts	
I_{DD}	Regulator Output Current	2.0		25.0	mA	Output Current
V_{IN}	Regulator Dropout		0.5	1.0	Volts	
	Low Battery Detect		6.0		Volts	
	Low Battery Detect Hysteresis		200		mV	Low Battery Detect - Hysteresis
OUTPUT CURRENT SINK/SOURCE						
I_{OUT}	Ring Source Current	-500	-	-	uA	$VOUT_H$ = V_{DD} - 0.5V
I_{OUT}	FSKBAT and Ring Sink Current	-	-	500	uA	$VOUT_L$ = V_{SS} + 0.4V

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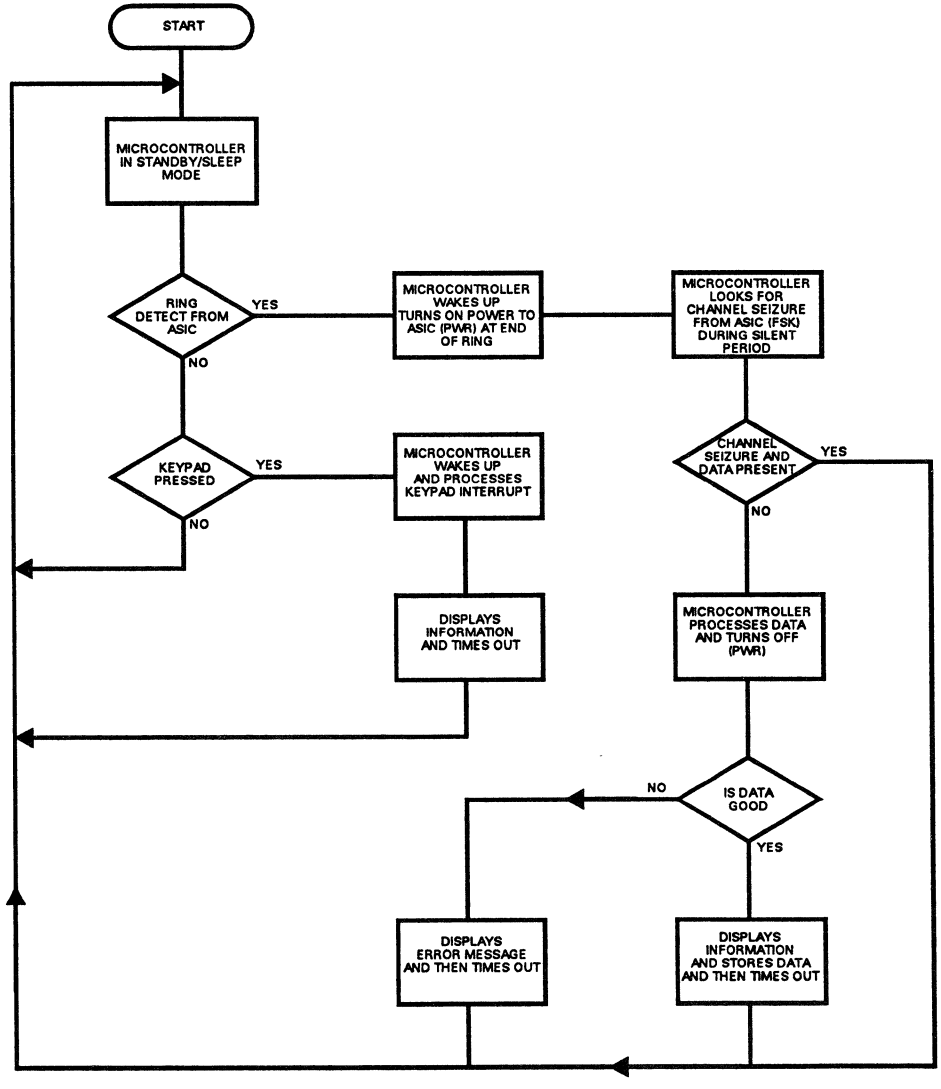
ICLID Process Flowchart

(for Microprocessor and ASIC (ICS1660) Interface)



ICS1660 ICLID Demonstration Board

Overview

The **DB1660** ICLID demonstration board is intended to be used to demonstrate the function of the **ICS1660** Incoming Call Line Identification Receiver IC. It provides a full-function incoming call display unit to verify the proper function of the **ICS1660** ICLID device.

NOTE: The only device that Integrated Circuit Systems Inc. is able to supply is the ICS1660. The other semiconductor devices and the display used on this board are proprietary designs and are not available from ICS.

Operation

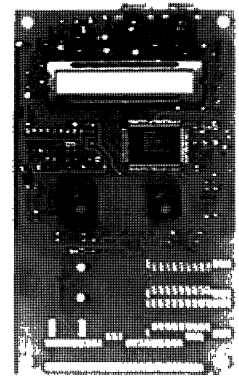
To use the **ICS1660** ICLID demo board, install a 9 volt alkaline battery in the battery clip on the board, and attach the battery connector. Facing the connector end of the board with the board "battery side up", the RJ11 connector on the right should be connected to a standard modular phone jack. The connector at the center of the board may be connected to the telephone instrument removed from the modular connector. Turn the board over so that the display is facing up and the two push buttons are toward you. Assuming that caller ID is available in your area, when your telephone begins ringing, the display will show the telephone number of your caller. After 20 seconds the display will return to its normal (blank) mode and the number will be stored in memory as the most recent call. When someone calls you from an area where the telephone company is not offering caller ID service or an area that is not yet providing caller ID information via the long distance network, the display will say "OUT-OF-AREA." In some areas, the calling party may be able to block their number from appearing on your call display. In this case, the display will say "PRIVATE." If the **DB1660** receives garbled data, a "?" will appear in every digit location that has unrecognized numbers. If all digits are garbled, the display will read "ERROR" but will not be stored in memory. In some areas, the local phone company will send a long-distance indicator which will show as an "L" on the display either with or without the incoming number.

Pushbutton Functions

Two pushbuttons exist on the **DB1660** board. The button to the left when facing the board, display up and buttons toward you is the **TIME** button. The button to your right is the **REVIEW** button. When the **REVIEW** button is pressed the phone number of the most recent call will be displayed. Each additional time the **REVIEW** button is pressed (within 20 seconds) the next most recent call is displayed. When the last call stored in memory has been reviewed, the next press of the **REVIEW** button will display "END."

Features

- Fully functional system permits verification of results obtained in a product application.
- Displays ICLID function without extensive design effort.



If **REVIEW** is pressed again within 20 seconds, it will bring you back to the start of the memory list and the most recent call will be displayed. If more than 20 seconds have elapsed before the **REVIEW** button is pressed, the display will blank and the next time **REVIEW** is pressed the most recent call will be displayed.

The time and date of an incoming call can be viewed by first pressing the **REVIEW** button until the selected number is displayed, and then pressing the **TIME** button. If the **TIME** button is pressed again within 20 seconds, the telephone number will again be displayed. This allows the **TIME** button to be used as a toggle between the telephone number and the date/time of the particular call.

NOTE: The **REVIEW** and **TIME** buttons are not operative during the interval when a new incoming phone number is being received.

When the ten call memory of the **DB1660** is full, the oldest call will automatically be erased to make room for the next call that comes in. To manually remove all calls, press the **TIME** button while the **REVIEW** button is pressed. This will also cause all the segments of the LCD display to be visible for as long as both of these buttons are pressed.

G

ICS

ASIC Capabilities

H

Mixed Analog/Digital Technology

ICS's capability in mixed analog/digital (mixed mode) technology is a direct outgrowth of 16 years experience providing turn-key designs. We have found that few mixed-mode applications lend themselves to a high level of integration with standard cells only. Customization is critical to bridge the gap between standard cells and the application.

ICS's confidence and success in mixed-mode design is due to our custom cell approach and our focus on understanding the systems in which the IC must perform. We firmly believe the development of any mixed-signal IC can be completed quickly and accurately by our team of skilled, experienced analog designers.

At ICS we use a custom cell based design methodology for our analog designs. We have developed the tools and expertise that allow us to customize analog cells reliably and inexpensively. This approach combines the ease of design and low risk of standard cells with the flexibility of full custom.

Of course, developing a functioning analog circuit is not as easy as connecting a few cells. An analog designer must view the circuit function as a whole to ensure correct and accurate performance. Below is a representative list of analog functions which we have designed and produced.

Power Conversion/Regulation
Bandgap Voltage Reference
Linear Voltage Regulator
Charge-Pump Voltage Booster
Charge-Pump Voltage Inverter
Microprocessor Reset/Clock Supervisor
Low Battery Detect
Power Switching Circuits

Control/Actuator Drive
Stepper Motor Driver
Air-Core Meter Movement Driver
Pulse-Width Modulated Motor Driver
Solenoid Driver
SCR/Triac Drive/Phase Control
X-Y Sensor Grid Drive
4-20mA 2-Wire Current Loop
LVDT Demodulator/Driver

Miscellaneous
LED/LCD Display Drive
Crystal & Ceramic Resonator Oscillators
Timers/Oscillators
Precision Matched Current Sources
High-Frequency VCO/PLL (230MHz)

Op-Amps
Low-Quiescent Current (uA)
Wide Input/Output Common Mode
High Speed (6MHz)
High Output Current

A/D Converters
Successive Approximation
Dual-Slope
Sample/Track & Hold
V/F Converters

D/A Converters
R-2R
Weighted

Signal Conditioning
Active Filters
Balanced Synchronous Demodulator
Digital Sine Wave Synthesis
Fixed & Variable Gain AC Amplification

ASICS At ICS

ICS has been a leader in providing state-of-the-art mixed signal and complex digital ASIC designs since 1976. The company was founded by assembling an unequaled engineering and design team to supply the electronics industry with the best in technical solutions and customer service in the ASIC marketplace. ICS has developed over 400 circuits since its beginning, and its success in standard products can be attributed to the same attention to detail applied to ASIC contract designs. ASIC projects are an important part of our business, and we can provide our customers with the best, most cost-effective solution to their ASIC needs.

ICS has focused its resources on providing the very best technical design expertise in both analog and digital technology. The cornerstone of this expertise is a custom/cell based approach where ICS assumes responsibility for the design, simulation, layout and verification of each circuit. We use standard cell libraries together with custom cells/functions where needed, a fully integrated CAD system, and proven CMOS processes. In addition, we develop the test hardware and programs necessary for each device we design. Our goal is to supply a high quality product. We remain committed to every product through on-time delivery, inventory management and ongoing product engineering.

Our business philosophy is to form a partnership with any customer whose business and technical requirements fit our guidelines and capabilities. We provide our ASIC customers with product management, development and production sourcing capabilities, by acting as an extension of your own engineering force. Through this partnership we are able to provide the most cost-effective solution to meet your requirements. We have developed unique relationships with software design companies, silicon foundries, photomask houses, and assembly operations, both domestic and international. These relationships provide ICS with the flexibility to select from many particular methodologies, processes or techniques. Our high volume of standard product business insures competitive pricing and service that's second to none.

- **A Technical Engineering Focus** - - The ICS engineering design team assigned to your ASIC product is involved from concept through characterization. Test development is considered part of this design task, thereby assuring that all critical parameters are adequately tested. Our engineers develop a full understanding of the engineering application for each ASIC device which allows ICS to critically evaluate the planned approach.

- **Design Flexibility** - - ICS advanced design technology makes changes and modifications affordable and fast at any stage of design or production. Simple modifications can often be corrected in one or two mask levels, saving time and money when changes are needed.

- **Process Flexibility** - - To bring the very best technology to your application, our suppliers include many of the leading semiconductor foundries and packaging houses. This allows for multi-sourcing, various packaging alternatives, and optimal utilization of semiconductor process technology. The large volume of standard product business we do with our suppliers assures us of competitive pricing. This permits ICS to extend large-volume pricing advantages to our ASIC customers.

- **Complete Production Support** - - ICS's approach is to outsource mask tooling, wafer fab and assembly while maintaining in-house control over production control, testing, QC and product engineering.

ICS Application Specific Standard Product

ICS has the capability to customize any of the standard products we offer to better suit the needs of its customers. Customized Standard Products permit an OEM customer to optimize his system design and minimize the amount of "glue" logic (or "glue linear") required to implement his end product. This can result in significant size, power, and cost savings in most OEM products.

Customization of ICS standard products can entail various degrees of complexity. A simple example might be to change the sense of logic levels input or output from a standard product. Frequency Timing Generator products often require specific output frequencies, power down capabilities, or control capabilities not available from our standard product listings. A more complex example would be the addition of latches to input or output signals. Perhaps the addition of a microphone preamplifier to one of the inputs of the ICS2101 audio mixer IC would simplify your design, packaging, and manufacturing task.

Obviously the investment in many of these alterations can be substantial in tooling and inventory costs. Therefore the projected volume must justify the investment. In some cases ICS may be willing to share the cost if other markets can be found for the new product.

The growth of laptop and notebook personal computers in the marketplace has placed a severe demand on manufacturers in the area of packaging, power consumption, performance and cost. ASIC devices may be the only practical way to satisfy these needs.

The standard for computers since the first integrated circuits made their appearance in the marketplace has been 5 volt logic levels. Power consumption, size (due to the size of battery packs), and performance requirements are rapidly moving this standard towards 3 volt logic levels. ICS ASIC capabilities permit many standard products to be redesigned to work at 3 volt levels.

Since ICS standard products are a logical outgrowth of our ASIC experience they utilize the same wafer fabs, semiconductor processes, standard cell libraries and building blocks used in our ASIC designs. This allows ICS to use most of our standard products as super cells in ASIC designs. The inclusion of standard product designs in your large-scale ASIC design permits fully characterized building blocks to be incorporated into your ASIC with minimum risk when compared to designed-from-scratch implementations of a complex function. Design cost, risk, and time-to-market are also improved as we do not have to reinvent the wheel each time the function is needed.

Foundry Selection

The chart below shows the qualified CMOS processes used by ICS for ASIC and standard products. This chart is constantly changing, as ICS is always negotiating for the latest proven manufacturing technology. This allows us to offer the most competitive costs to our ASIC customers, while at the same time providing qualified, proven manufacturing processes. Please contact your ICS representative for the latest list of available processes applicable to your particular need.

ICS Technologies **Principal Features**

SEMICONDUCTOR TECHNOLOGY	SPEED	DENSITY	LSI CELLS	MULTI SOURCE	STD CELLS	GATE ARRAY	VOLTS	ANALOG CELLS	FULL CUSTOM
CMOS 3μ Single Metal	Medium 25 MHz	Medium	Some	YES	YES	NO	3-10	YES	YES
CMOS 3μ Double Poly	Medium	Medium	NO	YES	YES	NO	10	Switched Cap.	YES
CMOS 1.5μ Double Metal	High	OK Gates	Some	YES	YES	NO	5	YES	YES
CMOS Metal Gate	Low 10 MHz	Low	NO	YES	YES	NO	5-18	YES	YES
CMOS High Voltage	Low 10 MHz	Low	NO	NO	YES	NO	30	YES	YES
CMOS 1.0μ	High	High	Many	YES	YES	NO	5	YES	YES
CMOS 8μ	High	Very High	Many	NO	YES	NO	5	YES	YES
CMOS .6μ	High	Very High	Many	NO	YES	NO	5	YES	YES

ICS

Quality and Reliability Information

H

ICS: Reliability Through Design

Right from the start, we concentrate on the ultimate quality of the product. ICS product reliability is designed in to meet the necessary controls that are imposed during production and testing. All ICS designs utilize a variety of "design-process-rule checks" to insure that product performance is consistent with our quality and reliability goals. Design simulations and wafer data base file verifications play a prominent role throughout the prototype and are production stages of the design to eliminate test correlation problems after the design is completed.

In a continuing effort to improve reliability as new devices are being developed, we review the data acquired from previous device designs to determine if any changes are necessary to improve performance and/or enhance the new device's operation. We evaluate all aspects of packaging technology, including leadframe vs. die-size compatibility, packaging materials and methods. ICS develops test programs to isolate problems during wafer probe and final testing to assure the quality of our products.

An extremely important phase of the product development cycle is the characterization of devices to insure their functional performance and establish margins of performance relative to device specifications. Samples of prototype units are initially measured to ascertain their performance characteristics and to verify that the transition from design and simulation to production processes has not had any deleterious effects.

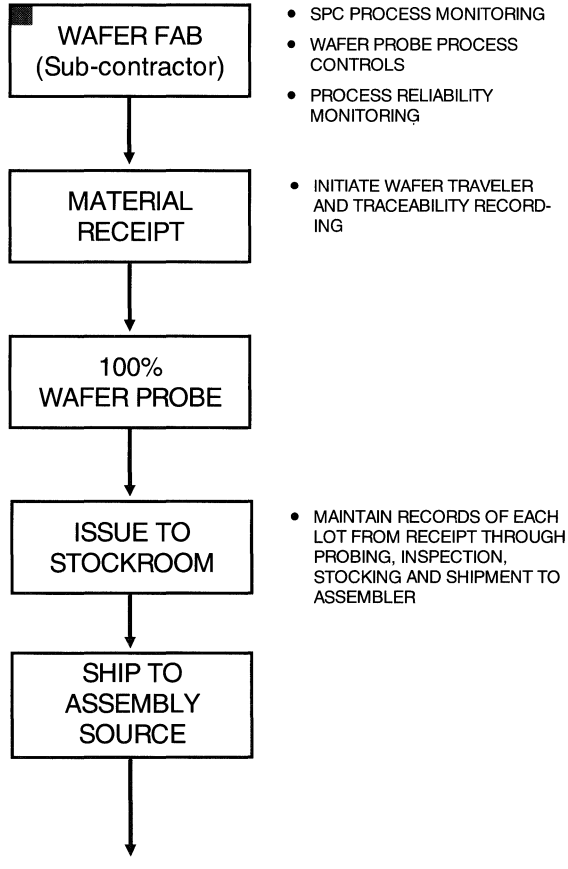
Production Flow

The production flow for ICS products is shown in the adjacent diagram, which provides some detail of the basic controls that are exercised through the various process stages. The processes of Wafer Fabrication, Assembly and Taping and Reeling are performed by outside facilities, with a process control- and electrical-data review for each lot of material before being routed for processing by these subcontractors. Wafer and package testing are performed at ICS.

A set of electrical characteristics data is provided for each wafer lot ICS receives. Every lot gets a parametric evaluation to determine the uniformity of the process and to serve as a quality control gate for wafer acceptance from manufacturing. SPC controls are maintained through the use of the accumulated profile parameters to serve as a source of electrical data feedback in support of process control and improvement programs. This data is also monitored by ICS to assess wafer fab performance and establish acceptance criteria for wafer fab lots. Environmental test monitoring including, HTOL, Temperature Cycling, Autoclave and Temperature/Humidity tests are performed to monitor the reliability of wafers produced.

The introduction of wafers into ICS from the wafer fab source initiates the traceability recording that tracks every part shipped from ICS. Wafer lot numbers assigned at the wafer fab source are recorded and are tracked through all stages of test, assembly, taping and ultimate shipment. At the ICS facility, all wafers are probed on a 100% basis before being shipped for assembly.

GENERAL PROCESS FLOW

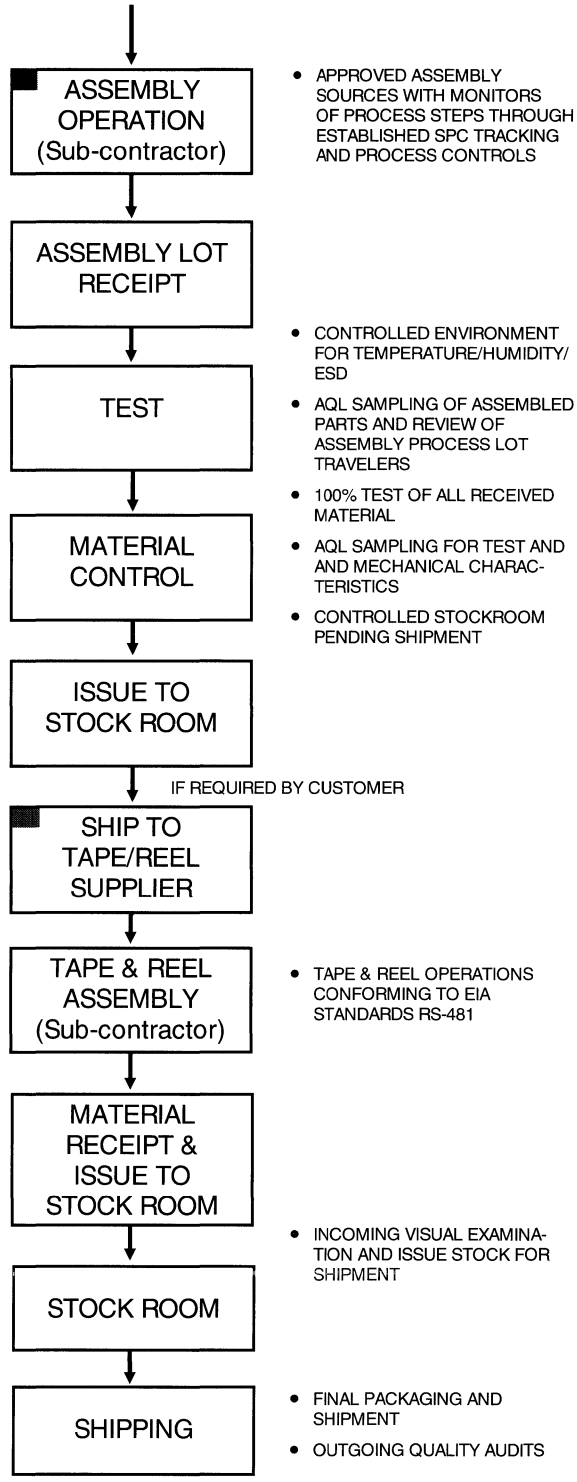


GENERAL PROCESS FLOW (continued)

Assembly suppliers are responsible to ICS for the processing of probed wafers into finished package configurations in accordance with ICS-supplied assembly specifications and bonding diagrams. Each assembly lot is supplied with a process traveler, which delineates the results of each process step and process monitor inspection. SPC data is maintained and reviewed on a periodic basis to assess such characteristics as: die shear, bond pull, solderability, marking permanence and process control elements pertinent to the assembly operations.

Processing at ICS includes incoming inspection examination of finished packages. Then we initiate test travelers to record test and inspection results and to allow for control of material into the stockroom. All parts are tested on a 100% basis in established test programs, and are checked on an AQL sampling basis for electrical and mechanical characteristics before acceptance to stock.

If customer requirements call for parts to be on tape & reel, the parts are packaged to ICS control specs for the implementation of this operation. The basic spec for this operation is per EIA Standard RS-481.



H

Traceability

At ICS, traceability of products is a critical attribute of the entire production process. Tracking is initiated at the wafer fabrication process and is maintained through all successive processing steps through final shipment. Records of traceability are retained to allow for tracking of product delivered to a specific customer so that its source may be determined if the need arises. Records are also available for communicating with suppliers the identification and isolation of any problems.

Electrostatic Protection

The phenomenon of ESD (Electrostatic Discharge) can be a source of damage to sensitive semiconductor devices. In order to address this potential for damage a dual approach is initiated. It is first addressed in the design stage where the design guidelines provide for electrostatic protection of the input/output stages of the device. ESD susceptibility of each device is verified to ensure the design is robust enough to be handled in the customers' environment using normal handling precautions. A minimum level of 2kV is the standard for design; however, product currently under test is equal to or exceeds 4kV susceptibility levels. Tests are performed in accordance with MIL STD 883 method 3015.7.

Second, we protect against damage throughout the inspection, test and subsequent handling of parts. All personnel are aware of the effects of ESD and are trained in proper handling techniques. Work stations are ESD controlled with ground straps, ESD dissipative table tops and floor mats and air ionizers. Work in process is transported in conductive tubs and discharged before handling on the dissipative work tables. Parts are shipped in ESD protective tubes or reels which are further protected by electrostatic protective bags.

Product Qualification and Monitoring

The Quality Assurance Department is responsible for the qualification and monitoring of all devices manufactured by ICS. This activity is designed to evaluate all wafer processes and package configurations and to maintain a proactive corrective program to prevent the shipment of unreliable product.

In the qualification process, we apply the following tests and stresses:

High Temperature Operating Life

High temperature operating life (HTOL or HTOB) testing is performed to accelerate failure mechanisms which are thermally activated through the application of extreme temperatures and the use of biased operating conditions. The temperature and voltage conditions used in the stress will vary with the product being tested. However, the typical stress ambient is 125 °C with the bias applied equal to or greater than the data sheet nominal value. All devices used in the HTOL test are sampled directly after final electrical test with no prior burn-in or other prescreening unless called out in the normal production flow. Testing can either be performed with dynamic signals applied to the device or in static bias configuration for a typical test duration of 1000 hours.

Temperature Humidity Bias

Temperature humidity bias (THB) is an environmental test performed at a temperature of 85 °C and a relative humidity of 85%. The test is designed to measure the moisture resistance of plastic encapsulated circuits. A nominal static bias is applied to the device to create the electrolytic cells necessary to accelerate corrosion of the metalization. Most groups are tested to 1000 hours.

Autoclave

Autoclave is an environmental test which measures device resistance to moisture penetration and the resultant effects of galvanic corrosion. Autoclave is a highly accelerated and destructive test. Conditions employed during the test include 121 °C, 100% relative humidity, and 15 psig. Corrosion of the die is the expected failure mechanism. Groups of parts are normally tested for a 96 hour duration.

High Temperature Storage

High temperature storage is performed to measure the stability of semiconductor devices during storage at elevated temperatures with no electrical stress applied. The devices are typically exposed to an ambient of 150 °C. An acceleration of charge loss from the storage cell or threshold changes are the expected results. All groups are typically tested to 1000 hours.

Temperature Cycle

Temperature cycle testing accelerates the effects of thermal expansion mismatch among the different components within a specific die and packaging system. This test is typically performed per MIL STD 883 or MIL STD 750 with the minimum and maximum temperatures being -65 °C and + 150 °C. During temperature cycle testing, devices are inserted into a cycling system and held at the cold dwell temperature for at least ten minutes. Following this cold dwell, the devices are heated to the hot dwell where they remain for another ten minute minimum time period. The system employs a circulating air environment to assure rapid stabilization at the specified temperature. The dwell at each extreme, plus the two transition times of five minutes each (one up to the hot dwell temperature, another down to the cold dwell temperature), constitute one cycle. Test duration for this test will vary with the device and packaging system employed. A typical test consists of 300 cycles, however some tests are extended to look for longer term effects.

Thermal Shock

The objective of thermal shock testing is the same as that for temperature cycle testing - to emphasize differences in expansion coefficients for components of the packaging system. However, thermal shock provides the additional stress of sudden temperature change. This sudden change is due to the shorter transfer time, 10 seconds maximum, and the increased thermal conductivity of a liquid ambient. This test is typically performed per MIL STD 883 or MIL STD 750 with minimum and maximum temperatures being -65 °C to + 150 °C. Devices are placed in a fluorocarbon bath and cooled to minimum specified temperature. After being held in the cold chamber for five minutes minimum, the devices are transferred to an adjacent chamber filled with fluorocarbon at the maximum specified temperature for an equivalent time. Two five-minute dwells plus two ten-second transitions constitute one cycle.

Reliability Data Analysis

Reliability is the probability that a semiconductor device will perform its specified function in a given environment for a specified period of time. The most frequently used reliability measure is the device failure rate. The failure rate is obtained by dividing the number of failures observed by the product of the number of total device on test and the test time interval. This is normally expressed in failures per billion device hours (FITS), which is a point estimate because it is obtained from observations on a portion, or sample, of the population of devices.

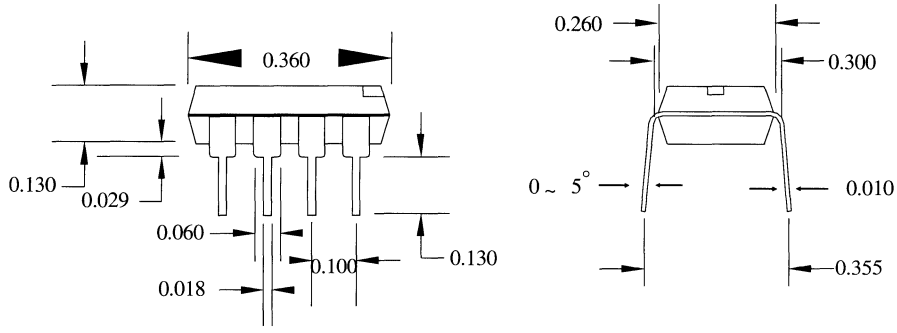
To project the failure rate of devices being tested to a total population, chi-square distribution statistics are applied at established confidence intervals. These are nominally calculated at 60% and 90% confidence levels to express a level of confidence that the sample failure rate approximates that of the entire population. In addition, since the failure rate of semiconductor devices is inherently low, the application of acceleration factors is applied to the data. Commonly used Arrhenius equations are applied which provide relationships between test stress levels and normal use operation. In applying this assessment tool an activation energy (Ea) of 0.7 Ea is normally used to determine the Acceleration factor. This Ea level is chosen in lieu of establishing individual Ea values for each of the failure mechanisms applicable to the technology and circuit under evaluation, particularly since the failure mechanism database is so limited.

To determine the failure rate of ICS products, the HTOL data for individual as well as families of devices is utilized. HTOL testing provides an adequate thermal stress with the devices being biased at greater than nominal value and operated in a dynamic mode in this environment. Utilization of these techniques will provide a realistic, conservative estimation of the product failure rate.

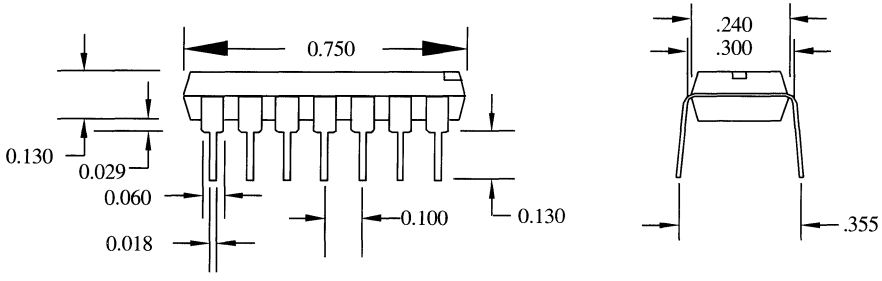
ICS

Standard

Package Dimensions

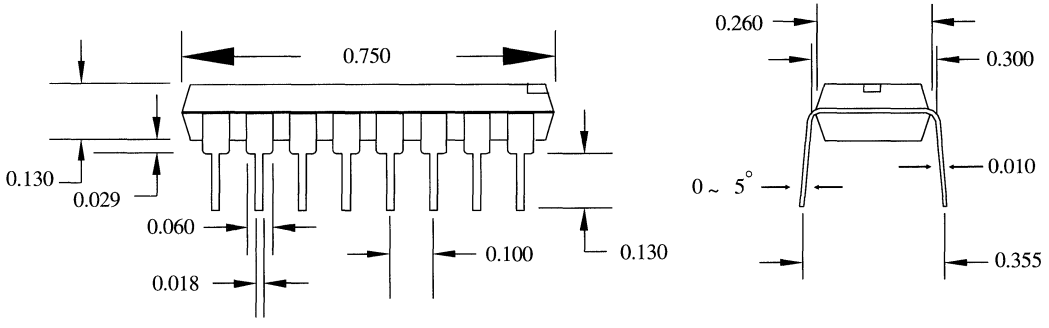


8 Pin DIP Package

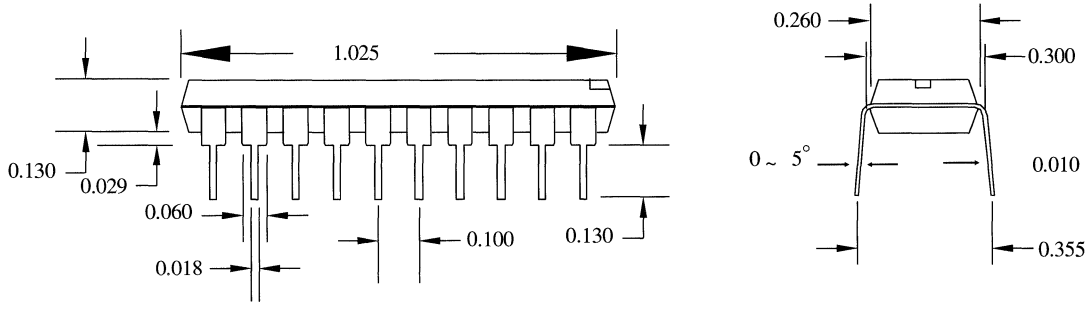


14 Pin DIP Package

See individual data sheets for more specific ordering information.

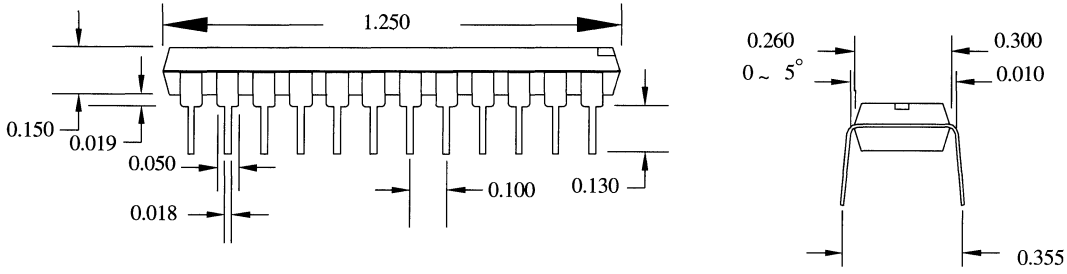


16 Pin DIP Package

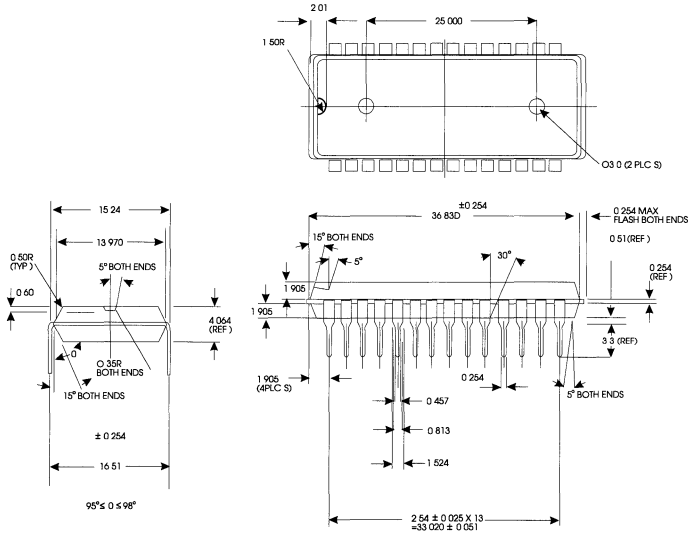


20 Pin DIP Package

See individual data sheets for more specific ordering information.



24 Pin DIP Package

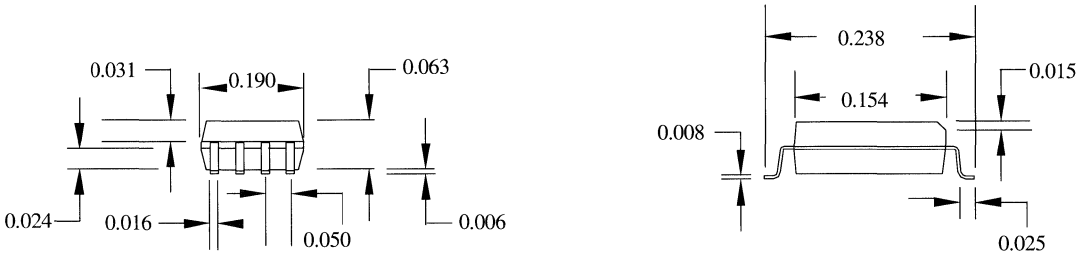


28 Pin DIP Package

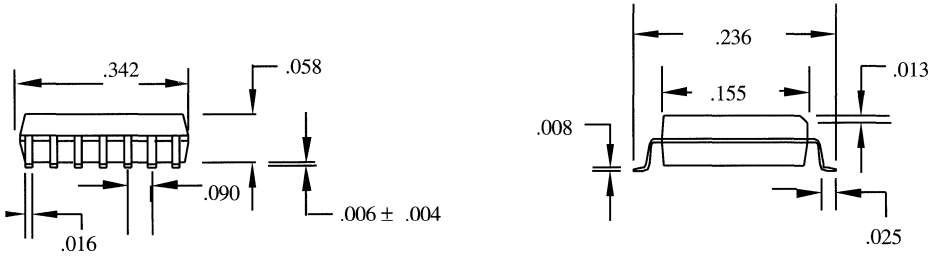
I

See individual data sheets for more specific ordering information.

SOIC Packages



8 Pin SOIC Package



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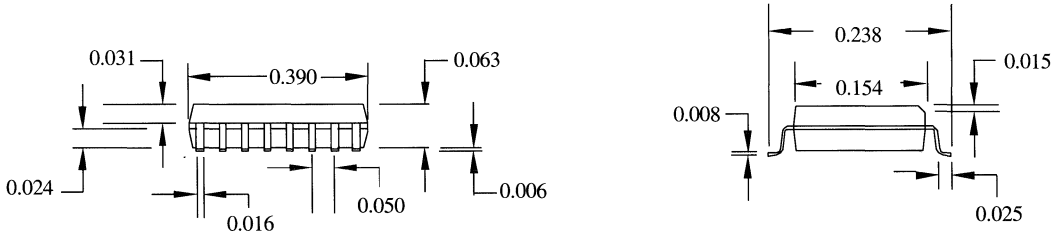
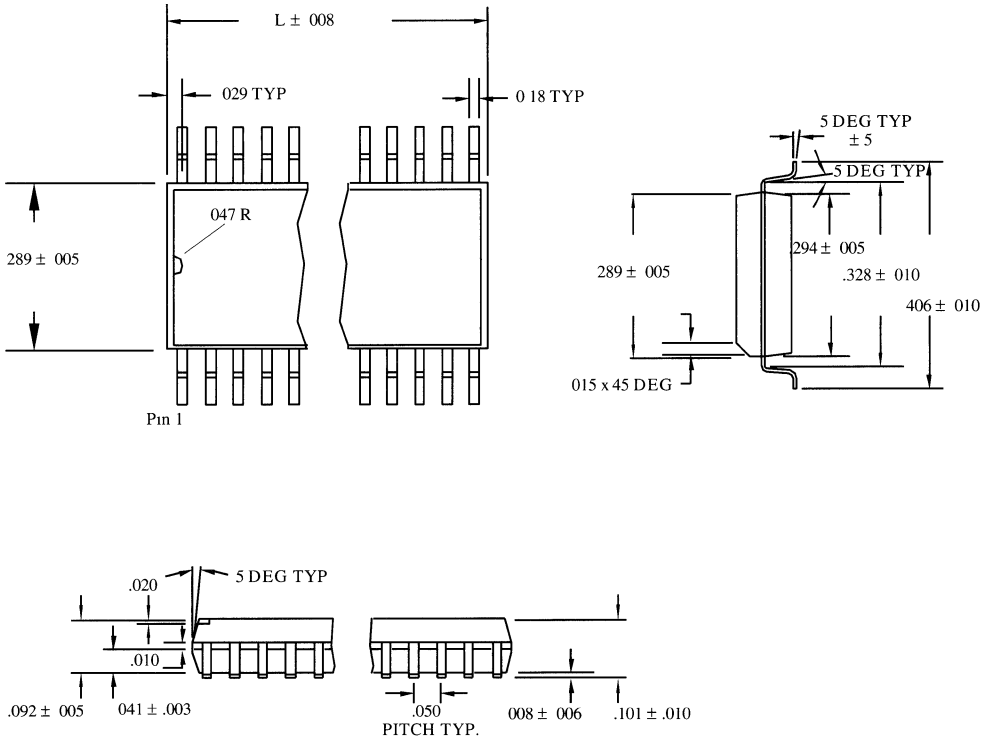


16 Pin SOIC Package

See individual data sheets for more specific ordering information.

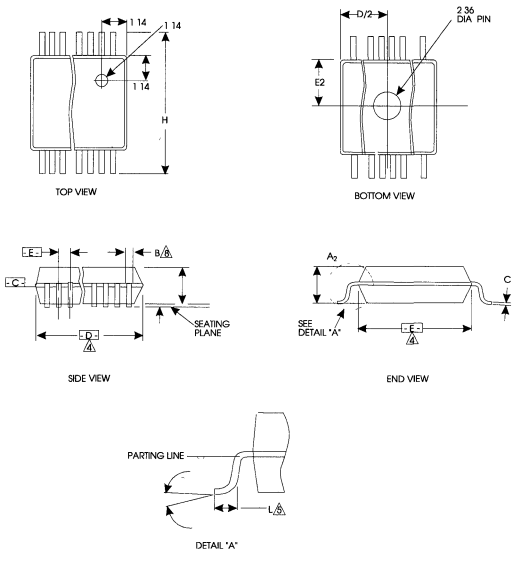


SOIC Packages (wide body)

LEAD COUNT	14L	16L	18L	20L	24L	28L	32L
DIMENSION L	.354	.404	.454	.504	.604	.704	.704

See individual data sheets for more specific ordering information.

SSOP Packages

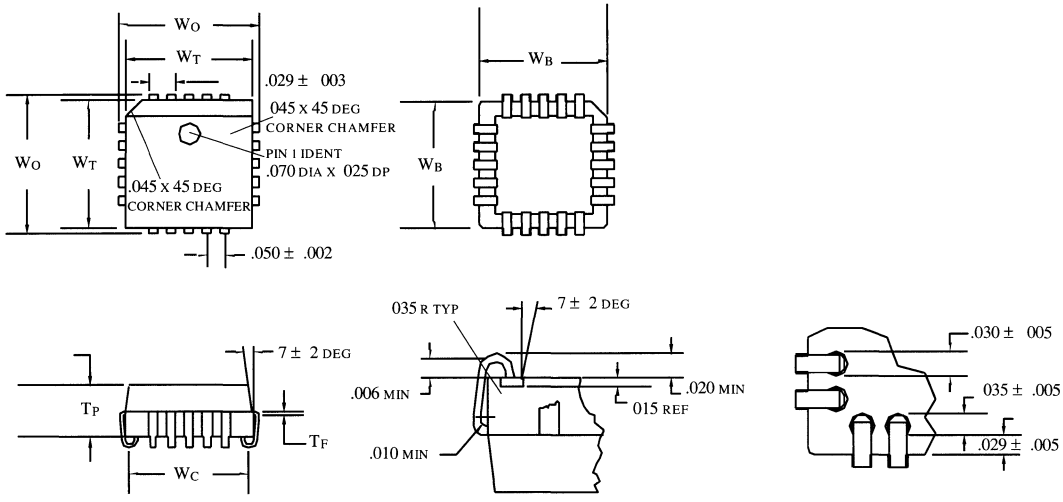


SSOP Package

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	4			6
					VARIATIONS	D			N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	0.68	.073	0.78		AA	.239	.244	.249	14
A1	.002	.005	.008		AB	.239	.244	.249	16
A2	.066	.068	.070		AC	.278	.284	.289	20
B	.010	.012	.015		AD	.318	.323	.328	24
C	.005	.006	.008		AE	.397	.402	.407	28
D	See Variations			4	AF	.397	.402	.407	30
E	.205	.209	.212	4					
e									
H	.301	.307	.311						
L	.022	.030	.037	5					
N	See Variations			6					
∝	0É	4É	8É						

This table in inches.

See individual data sheets for more specific ordering information.



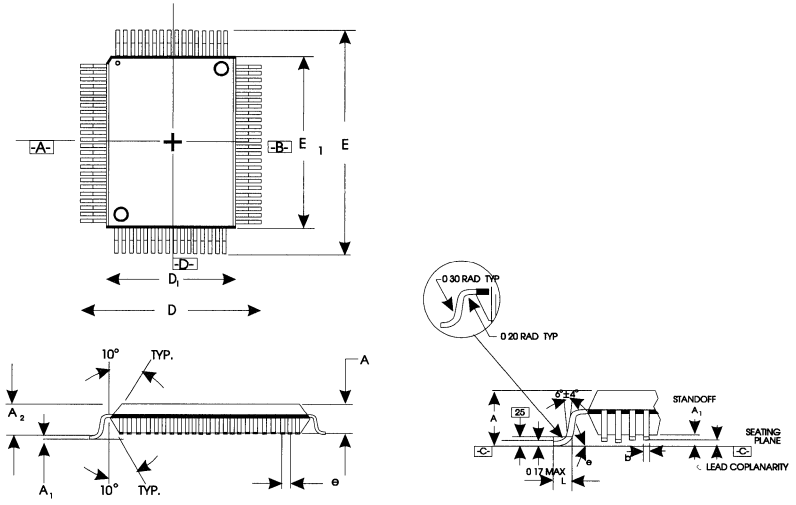
PLCC Package

LEAD COUNT	FRAME THICKNESS T_F + /-.0003	PKG. THICKNESS T_P + /-.004	PKG. WIDTH TOP W_T + /-.004	PKG. WIDTH BOTTOM W_B + /-.066	OVERALL PKG. WIDTH W_O + /-.005	CONTACT WIDTH W_O + .010/-.030
20L	0.010	0.152	0.350	0.323	0.390	0.320
28L	0.010	0.152	0.450	0.423	0.490	0.420
44L	0.010	0.152	0.650	0.623	0.690	0.620
52L	0.010	0.152	0.750	0.723	0.790	0.720
68L	0.008	0.150	0.950	0.923	0.990	0.920
84L	0.008	0.150	1.160	1.123	1.190	1.120

I

See individual data sheets for more specific ordering information.

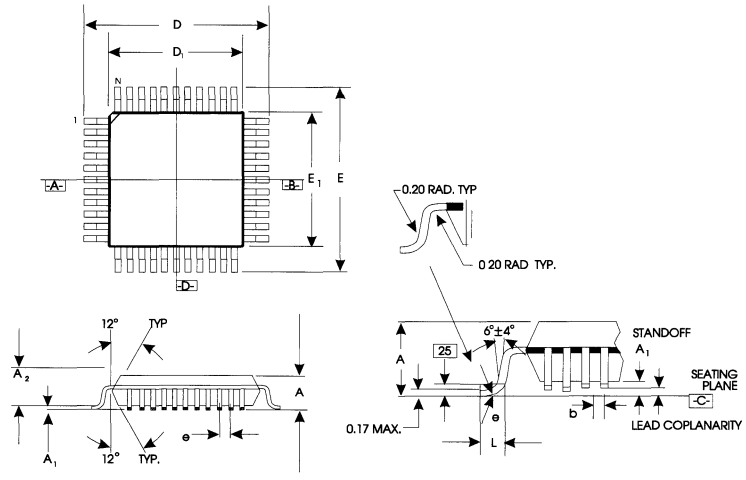
QFP Packages



QFP Package

LEAD COUNT		64L	80L	100L	64L	80L	100L
BODY THICKNESS		2.00			270		
FOOTPRINT (BODY+)		3.20					
DIMENSIONS	TOLERANCE						
A	MAX.	2.45			3.40		
A_1		0.25 MAX.			0.25 MIN.		
A_2	± 0.10	2.00			2.70		
D	± 0.25	17.20					
D_1	± 0.10	14.00					
E	± 0.25	23.20					
E_1	± 0.10	20.00					
L	± 0.15/0.10	0.88					
e	BASIC	1.00	0.80	0.65	1.00	0.80	0.65
b	+ 0.05	0.35		0.30	0.35		0.30
ccc	MAX.	0.10					
ddd		0.20 NOM.		0.12 NOM	0.20 NOM		0.12 NOM.
0		0° - 7°					

See individual data sheets for more specific ordering information.



TQFP Package

LEAD COUNT		32L	
BODY THICKNESS		1.00	1.40
FOOTPRINT (BODY+)		2.00	
DIMENSIONS	TOLERANCE		
A	MAX.	1.20	1.60
A_1		0.05 MIN./0.10 MAX.	
A_2	± 0.5	1.00	1.40
D	± 0.25	9.00	
D_1	± 0.10	7.00	
E	± 0.25	9.00	
E_1	± 0.10	7.00	
L	± 0.15/-0.10	0.60	
e	BASIC	0.80	0.50
b	+ 0.05	0.35	0.22
ccc	MAX.	0.10	0.08
ddd		0.20 MAX.	0.08 MAX.

See individual data sheets for more specific ordering information.

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and

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