Computer Systems Department

OUTPUT SYSTEM

C697-416L-ST

24 April 1967

Keesler Technical Training Center
Keesler Air Force Base, Mississippi

Computer Systems Department
KTTC, Mississippi

Student Text
ABR30533-1
24 April 1967

OUTPUT SYSTEM

This Student Text provides student study material in support of Course ABR30533-1.

CONTENTS

CHAPTER 1. INTRODUCTION TO OUTPUTS

1. Function of Output System in AN/FSQ-7 Combat Direction Central

The Output System in the AN/FSQ-7 Combat Direction Central transfers output messages from the Central to adjacent Centrals and remote sites through telephone facilities. (See Figure 1-1.) After forming an output message, the Central Computer System stores it on the output buffer (OB) fields of the LOG drum in the Drum System for eventual transfer to the Output System. The Output System accepts the output message from the OB fields and transfers the message to telephone facilities for transmission to its intended destination(s). The path followed by the output message from the Central Computer System to the telephone facilities is shown in Figure 1-2. The general manner in which the Output System accepts output messages from the OB fields and transfers them to telephone facilities is discussed below. Because the Output System is logically divided into two elements, the output control element and the output storage element, as shown in Figure 1-3, the following general description of the operations performed by the Output System is treated by referring to these two elements.

2. Output Control Element

The output control element primarily controls the flow of output message words from the OB fields of the LOG drum to the output storage element. Another function of the output control element is to make available to the Central Computer System specific data which is used by the Air Defense program as an aid in controlling the transmission time of output messages. The output control element also provides visual indications of alarm conditions that might occur in the Output System and, in addition, contains Output System test equipment which can be used both as an aid in detecting the sources of trouble within the Output System and as an aid in checking certain elements of the Input System.

3. Output Storage Element

The output storage element temporarily stores the words of an Output message and then, at the completion of read-in (when the complete message is present in the output storage element) transfers the message serially to telephone terminal equipment. This element contains three storage sections; each accommodates a different class of output messages. Output messages are grouped into three classes: ground-to-air time division (G/A-TD), ground-to-ground (G/G), and teletype (TTY). The storage sections are labeled accordingly, the G/G storage section, the G/A-TD storage section, and the TTY storage section. These storage sections receive and store output messages and then transfer them serially to the telephone terminal equipment. However, the transfer rate employed by the storage sections differs and depends upon the class of output message handled. Output messages in the G/G and G/A-TD classes are sent over telephone data channels to sites equipped with automatic input equipment. Sites not equipped with automatic input devices are supplied with teletypewriter receivers. Output messages destined for such sites are in the TTY message class and are transferred by the TTY storage section to telephone equipment at the standard TTY rate of 60 words per minute (wpm).

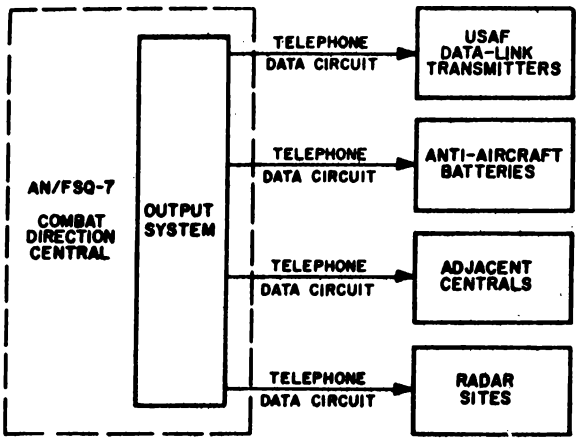


Figure 1-1. Remote Sites, Block Diagram

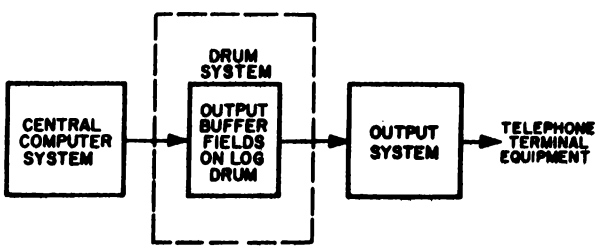


Figure 1-2. Output Message Flow, Block Diagram

Output Messages

1. General

An output message is a communication sent from an AN/FSQ-7 Combat Direction Central to adjacent Centrals or remote units. The Central Computer System performs various operations, controlled by the air defense situation data supplied to the Central Computer System by radar sites adjacent Centrals, and by personnel (manually) through the Input System. If the results of these operations are to be transmitted to remote units, such results are formed into output messages. As previously indicated, an output message falls into one of three classes: G/G, G/A-TD, and TTY. The data used to form each message class and the purpose or purposes of each class are described below.

Ground-to-air TD messages are composed of data which will help manned fighter aircraft intercept assigned enemy targets. The G/A-TD messages are transmitted

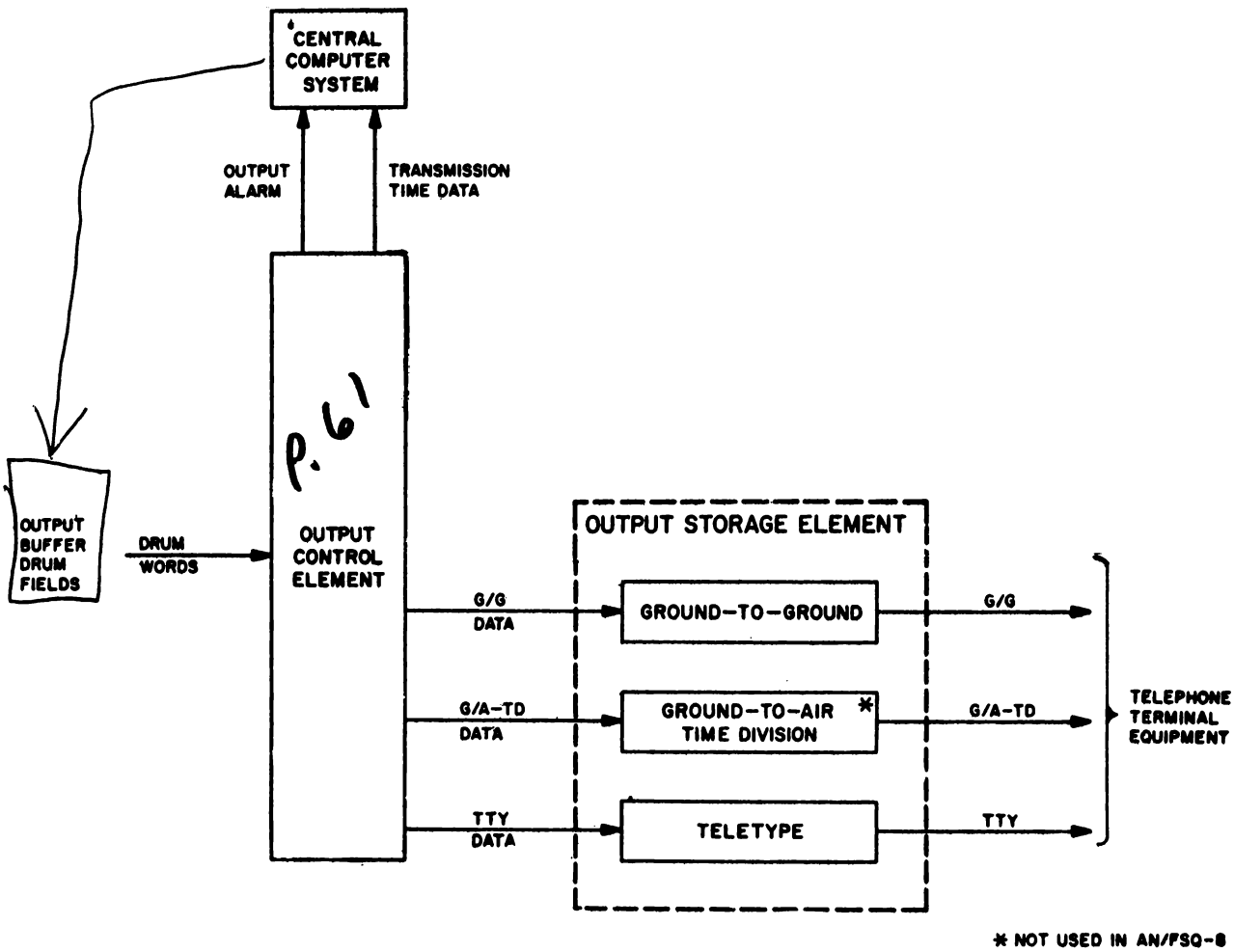


Figure 1-3. Output System, Block Diagram

from the Central to the remote G/A-TD data-link transmitters which provide the radio link with the aircraft.

A G/G message is composed of either crosstelling (XTL) data, forwardtelling data, height-finder request, or a missile control message. Ground-to-ground XTL messages are transmitted to adjacent AN/FSQ-7 Combat Direction Centrals, and G/G forwardtelling messages are sent to an AN/FSQ-8 Combat Control Central. Crosstelling information is data that aids the receiving Central in performing its assigned function. Forwardtelling data is a report on the over-all situation in the area of the sending Central. Another type of G/G message is composed of a height-finder request which is sent to height-finding equipment at a radar site.

A height-finder request message is employed whenever the altitude of a specific target is required. The remaining type of G/G message is used for in-flight control of unmanned interceptors (missile).

Teletype messages are formed of either information intended for higher headquarters, information for non-automatic adjacent sectors (sectors not equipped with AN/FSQ-7 Combat Direction Centrals), or early warning information intended for anti-aircraft batteries. Forward-telling information sent to higher headquarters is a summary tabulation of the up-to-the-minute air defense situation. The TTY messages sent to non-automatic adjacent sectors contain information similar to the data in G/G messages. Teletype messages sent to the anti-aircraft batteries are composed of early warning radar data.

2. Timing of Output Message Transmissions

The time for the transmission of each output message is selected in the Central Computer System, and certain Output System Circuits ensure that the message is transmitted at the selected time. The reasons for this control and the means by which it is accomplished are described in the following text.

Output messages must be transmitted in correct sequence within each of the three classes: G/G, G/A-TD, and TTY. In addition, certain types of messages in each class must be transmitted at the proper times.

3. Message Formation. (Refer to Table 1-1.)

a. General

An output message as formed by the Central Computer System is composed of several words; the exact number of words used to form each message varies with the class of the message. A G/G message contains five words; a G/A-TD message, four words; and a TTY message, an indefinite number of words. Each drum word is composed of 32 bits and is divided into halves, the left half-word and the right half-word. The right half-word contains output data to be transmitted, and the left half-word is made up of address data and a burst number. After formation, and prior to storing the word on the OB fields for eventual transfer to the Output System, a parity bit is added, increasing the total number of bits to 33.

b. Left Half-Word

The left half-word of each word contains a 3-bit section address (L5-L2), a 5-bit register address (L3-L7) and a burst number which may contain as many as eight bits (L8-L15). This data is used to inform the Output System of the output storage section that is to transmit the right half-word, the storage register in the selected output storage section where the right half-word is to be stored, and the burst period during which the right half-word is to be accepted from the OB fields and transmitted by the selected storage section. The combination of the section address and register address determines the group of remote sites to which the right half-word is transmitted. In

Illegal OSA 0, 4, 6, 7

OSA 000 illegal - word thrown away

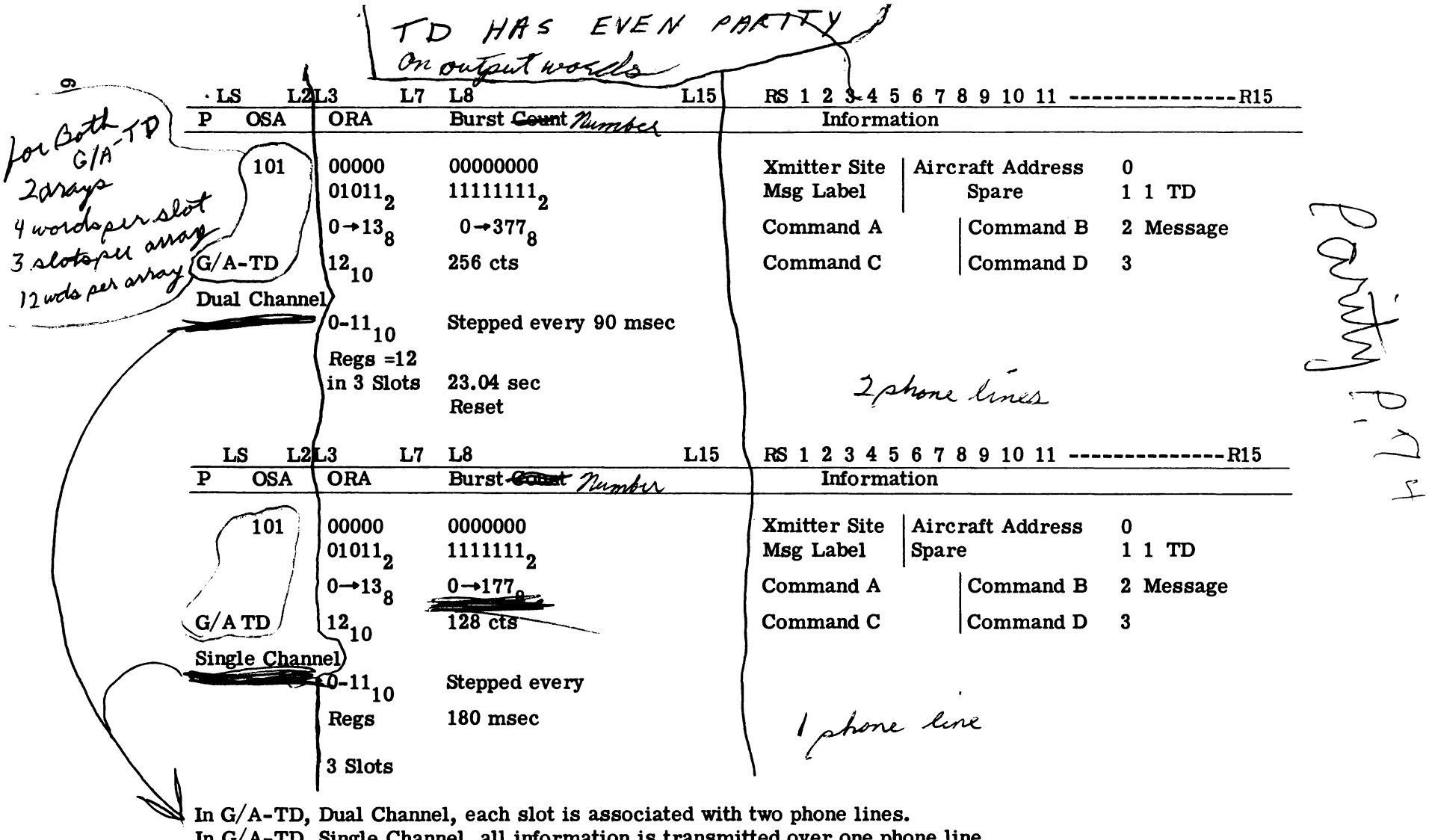
LS L2	L3 L7	L8 L15	RS 1 2 3 4 5 6 7 8 9 10 11 R15
P OSA	ORA	Burst ~~Count~~ Number	Information
odd parity on output word			
010	00000	00000000	XTELL to an AN/FSQ-7
DUPLEX OUTPUTS	11000_2	11111111_2	Forward Tell to an AN/FSQ-8
SECTOR ADDRESS	0 30_8	0 377_8	Height Finder Request (typical format)
G/G	25_{10} max	256_{10} cts	Old Height Reg # Radar Site Adr (Word #0)
	$0 \rightarrow 24_{10}$	$0 \rightarrow 255$	00 Y Coordinates---- 0000 #1
	Regs		00 X Coordinates---- 0000 #2
		Ctr stepped	00 Spare Special Request 0000 #3
2 arrays	5 Slots per array	every 92/1300 sec	00 000000000000000000000000 0000 #4
5 slots per array	output reg address	Approx 70.7 msec	Missile Control & Missile Master (Nike)
5 words per slot msg		Reset every 18 sec	5 phone lines
odd parity on output word	P OSA	ORA	Burst ~~Count~~ Number	Information
011		00000	00000000	1 Command / Command / Command
TTY		11000_2	00011111_2	A
		$0 \rightarrow 30_8$	$0 \rightarrow 37_8$	L
1 array		25_{10}	32_{10} cts	W
1 word per slot		0 24_{10}	Ctr stepped	A
25 slots (10)		Regs	every 45/91 sec	Y
			Approx 1/2 sec	S
		25_{10} Slots		25 phone lines
	31 or more octal ent is illegal		Reset Approx every 16 secs	25th phone line is site self-monitor

Each slot is associated with an individual phone line.

Parity p. 74

OUTPUT DRUM WORD LAYOUTS

Table 1-1



OUTPUT SYSTEM DRUM WORD LAYOUTS

Table 1-2

order to understand how the section and register addresses are used to accomplish this, a short discussion pertaining to the logical composition of the storage device employed in the output storage sections and to the telephone facility connections is required.

The output storage sections employ ferrite core arrays as storage devices. An array is composed of 26 core registers, each of which has the capacity to store a right half-word. An array within an output storage section is logically divided into slots, each formed by the number of registers required to accommodate the right half-words of one output message. Therefore, a slot can store one output message. Since the number of words forming an output message varies according to the output message class, the number of registers forming a slot differs in each output storage section. A G/G slot is composed of five registers; a G/A-TD slot, of four registers; and a TTY slot, of only one register. The TTY slot requires only one register because only one word of a teletype message is transmitted during a teletype burst period.

During the formation of an output message, the remote site intended to receive this message is known as a result of the Central Computer System operations performed on air defense situation data. A binary code for a storage section is selected and assigned as a section address. This section address is assigned to each left half-word of the output message. The section address is a general address because it merely specifies the output storage section that is to transmit the message. In order to complete the addressing of the output message, the words of the message must be addressed to those registers composing the slot in the selected output storage section array that supplies the telephone circuit connected to the intended destination of the message. Therefore, successive words in the output message are sequentially assigned the register addresses of the registers in the slot concerned.

The remaining portion of a left half-word is the burst number. The burst number that is assigned to a message indicates the burst period during which the words of the message are to be accepted by the Output System from the OB fields and then transmitted. The same burst number is assigned to each left half-word of the message (or messages, if there is more than one in a burst).

c. Right Half-Word

The right half-word of each output message word is formed by the Central Computer System, using only a part of the data composing a complete output message. The remaining output message data is used to form the right halves of the other words in the message.

A G/G message contains five right-half drum words (a total of 80 bits employed by the Central to carry either XTL information to an adjacent Central, forward-telling data to an AN/FSQ-8 Combat Control Central, or a height-finder request to a radar site. The data used to form a G/G XTL or forwardtelling message can be varied by the air defense program in the Central Computer System. Therefore, the amount of XTL or forwardtelling data used to form each right half-word of a G/G message is not fixed.

Each right half-word of a typical XTL or forwardtelling message is formed by the Central Computer System. The last (third) type of G/G message is employed to carry height-finder requests to radar sites.

A G/A-TD message is composed of four right half-words that are separated into groups of two right half-words and transmitted over separate telephone channels to manned interceptors via data-link transmitters. Two data phone lines are used to transmit the G/A-TD message to the manned interceptor. One data phone line handles information relating to site address, aircraft address, and the message label, whereas the command data associated with the G/A-TD message is transmitted over the other data phone line.

One G/A-TD message contains four commands. The G/A-TD messages are sent from the Central via data-link transmitters that are located within a given area, with each transmitter operating on the same assignedfrequency. Selection of a particular data-link transmitter is established by the site address portion of the G/A-TD message. If a G/A-TD message is addressed to a particular aircraft in a group of aircraft, only that aircraft will take action on the transmitted message.

A TTY message is employed by the Central to carry information to remote sites not equipped with automatic input devices through telephone TTY circuits. Each right half-word of a TTY message contains the binary equivalent of three TTY code symbols. A TTY code symbol represents either a letter, a figure, or a TTY operation. Table 1-3 shows the TTY letter, figure, or operation associated with a 5-bit binary code symbol. As shown in Table 1-3, a binary code may represent either a letter or a figure. Because of this, a code symbol representing either of the TTY operations, entitled letters or figures, must be transmitted prior to the group of letter or figure codes. The three 5-bit code symbols employed to form a right half-word of a TTY message depend upon the data to be transmitted. The 15 bits of the three 5-bit code symbols occupy bit positions R1 through R15 of a TTY right drum word. Bit RS is always a 1.

d. Parity Bit

A parity bit is added to the drum word to cause the sum of the 1's in a word to be odd if odd parity is desired and to be even if even parity is desired.

A parity check for the correctness of the drum word is accomplished by counting the number of 1 bits of the drum word which are stored in the OB register and affecting odd parity.

In the Central Computer System, after the left and right halves of a word are formed, a count is made of the 1 bits in the word. When an odd total is discovered, a 0 parity bit is assigned; however, should an even total result, a 1 parity bit is added. In both cases, the total number of 1 bits in the word plus the parity bit is odd. Therefore, the number of 1 bits in a word, together with its parity bit, when placed on the OB fields, should always be odd. The 32-bit word plus the parity bit is referred to as a 33-bit drum word. When the Output System reads a drum word from the OB fields, it performs a parity count to determine whether or not the word is acceptable. The word is accepted if it has odd parity and rejected if it has even parity.

LETTERS	FIGURES	CODE SIGNALS
A	-	00111
B	?	01100
C	:	10001
D	$	01101
E	3	01111
F	!	01001
G	&	10100
H	#	11010
I	8	10011
J	'	00101
K	(	00001
L	)	10110
M	.	11000
N	,	11001
O	9	11100
P	0	10010
Q	1	00010
R	4	10101
S	Bell	01011
T	5	11110
U	7	00011
V	;	10000
W	2	00110
X	/	01000
Y	6	01010
Z	"	01110
Space		11011
Carriage Return		11101
Line Feed		10111
Figures		00100
Letters		00000
Blank		11111

Table 1-3. Teletype Code Characters

Drum Storage

1. General

> Note: For a detailed discussion of the LOG Drum and the three OB fields refer to the Job Proficiency Guide of the C.C. Drum System.

There are three OB fields on the LOG drum in the Drum System upon which drum words are stored by the Central Computer System for eventual transfer to the Output System. These OB fields are used consecutively and therefore may be thought of as one triple-size drum field. One restriction upon this concept is the fact that a continued reading from, and writing onto, these fields is interrupted because a delay of 120 usec is introduced when switching from one field to the next. These OB fields are divided into 6,144 registers (2,048 per field); however, only 2,036 registers per field are used to store drum words because 120 usec are required at the beginning of each field to allow for switching fields. Thus, 12 drum registers per field have no usable information in them (dead registers); consequently, only 2,036 drum-word registers are used. The drum rotation is such that successive registers are spaced 10 usec apart.

The drum words of an output message are written onto the OB fields at the maximum rate of 50,000 drum words per second. They remain on the OB fields until the arrival of the burst period, during which the output message is intended for transmittal by the Output System. At the start of this burst period, the drum words of the output message are accepted by the Output System from the OB fields at the maximum rate of 100,000 drum words per second, but not for the same section.

In addition to transferring drum words stored on the OB fields to the Output System, the Drum System supplies the Output System with OD LOG drum timing pulses. The Output System utilizes these timing pulses to synchronize its operations with those of the Drum System.

2. OB Fields Writing

The drum words of an output message are written on either all odd or all even drum-word registers of the OB fields, as specified by the Central Computer System. Since there is a 10-usec interval between successive registers, the minimum interval between the writing of successive drum words of an output message on the OB fields is 20 usec; i.e., writing cannot occur at a rate greater than 50,000 drum words per second. The drum words of the same output message are intended for a specific storage section of the Output System, which receives them at the same rate at which they are written onto the OB fields. The maximum rate at which information can be placed in a ferrite core array employed by an output storage section is 50,000 pulses per second (pps). Thus, limiting the writing of successive drum words onto only odd or even drum registers ensures that the rate at which the drum words of a message are transferred to a particular core array never exceeds 50,000 drum words per second.

Successive drum words of one message are not necessarily written onto these drum fields in successive odd or even registers. Instead, each drum word is written onto the first odd or even drum-word register that is available to the drum word.

A drum-word register is considered to be available if its contents have been accepted by the Output System; it is considered unavailable when it stores a drum word that has not yet been accepted by the Output System. Thus, when a drum word is accepted by the Output System, the status of its associated drum-word register is changed to indicate an available register. In like manner, the status of a register is changed to unavailable when a drum word is written onto the register. No separate erasing procedure is performed when a drum word is accepted by the Output System because the action of writing a new drum word onto an available register effectively erases the old drum word as part of the write-in process.

Frequently, each successive drum word must wait for a register to become available; consequently, successive drum words are often placed on the OB fields several drum-word registers apart. Therefore, the interval between the writing of successive drum words of the same message may be greater than 20 usec (but the interval is always a multiple of 20 usec).

3. OB Fields Reading

The contents of the drum-word registers on the OB fields are read consecutively and transferred to the Output System. Since there is a 10-usec interval between drum-word registers, the drum words cannot be read at a rate greater than 100,000 drum words per second. Each drum word received by the Output System is examined and either accepted, rejected for being in error, or rejected for arriving too soon. The statuses of the registers associated with the drum words that are either accepted or rejected for being in error are changed to available. The drum words that are rejected for arriving too soon remain on the OB fields. These rejected drum words contain good information and will be accepted at a later time. Consequently, the statuses of the registers containing the rejected drum words remain unchanged to prevent the writing of new drum words over still useful information.

4. Log Drum OD Timing Pulses

The LOG drum OD timing pulses are used to synchronize the transfer operations of the Drum System with the processing operations of the Output System. There are four OD timing pulses, designated OD 1, OD 2, OD 3, and OD 4. These pulses occur in sequence from OD 1 through OD 4 with a spacing of 2.5 usec between successive pulses. Therefore, an OD cycle, which is the interval between an OD 1 pulse and a following OD 1 pulse, is 10 usec. The OD pulses are generated continuously, with every OD 4 pulse followed 2.5 usec later by an OD 1 pulse.

Ferrite Core Storage

Note: Refer to Figure 1-4.

1. The ferrite core array is a coincident-current storage device, similar in some respects to the core memory of the Central Computer System. This array consists of 572 ferrite cores arranged to form 22 columns and 26 rows. As shown in Figure 1-4, the two axes are termed the message axis and the address axis, and each row is known as an addresss register.

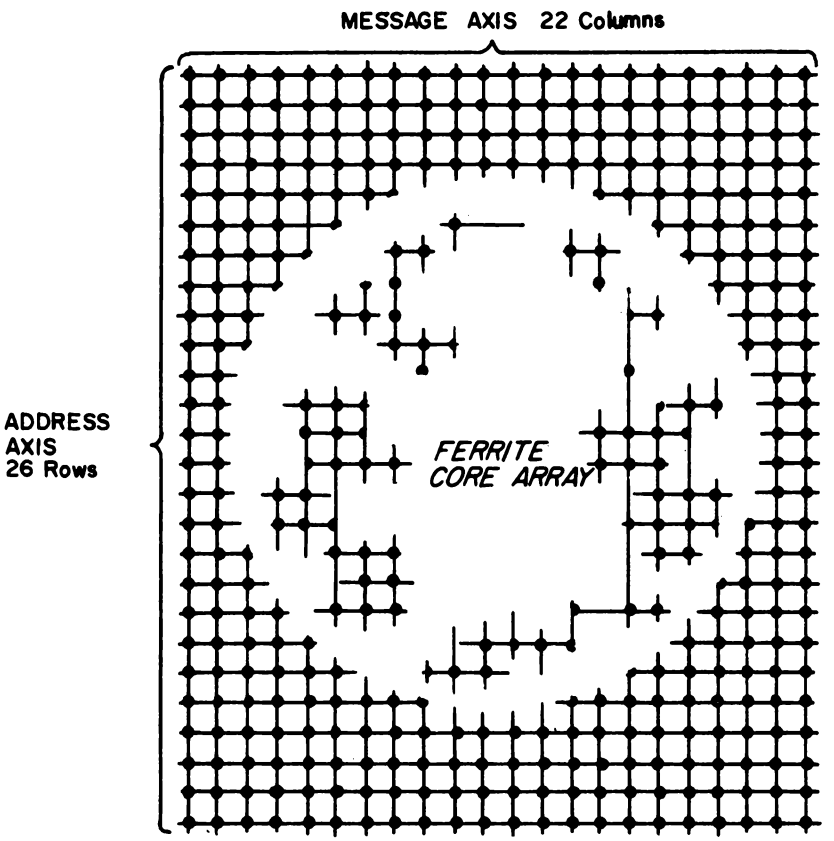


Figure 1-4

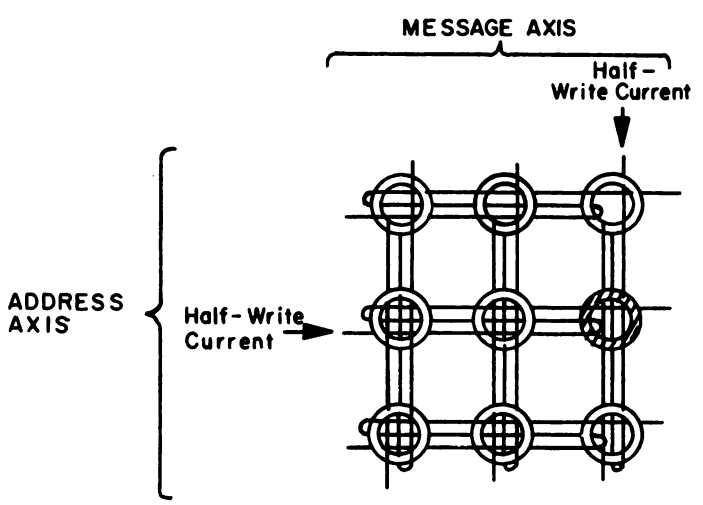


Figure 1-5

The ferrite core is a device with square loop hysteresis characteristics, capable of two saturated states. These two states represent binary digits 0 and 1. Read-in of information switches one or more cores in the array from the 0 state to the 1 state and allows other cores to remain in the 0 state. Readout of information sequentially senses the state of all cores in the array and switches the cores previously set to the 1 state back to the 0 state.

During read-in of information, a particular core in the array is set to the 1 state upon receipt of two half-write currents: one from the address axis and one from the message axis. Each column and each row is provided with a 2-turn read-in winding which carries the half-write current. Figure 1-5 shows a simplified version of an array and the method by which a particular core is selected for read-in of information. The coincidence of two half-write currents applied to a particular core results in the full-write current necessary to switch the core from the saturated 0 state to the saturated 1 state. Note: Refer to Figure 1-5.

Readout of information from an array necessitates two windings for each column and each row in addition to the read-in windings previously mentioned. (See Figure 1-6.) These windings are termed the readout winding and the sense winding. Readout differs from read-in in that it is not produced by two coincident currents; instead, a single readout current flows through the 2-turn readout winding of all ferrite cores of a column. Sequentially, one column after another is read out in this manner. This process is illustrated in Figure 1-7.

When the readout current pulse is applied to a given column, all cores in that column that were previously switched to a 1 state are switched back to the 0 state. The sense winding is a single-turn winding which connects all the cores in a given row. The effect of pulsing the readout winding is to induce a voltage in the sense winding. The induced voltage is of either of two configurations, depending upon whether the core was already in a 0 state or whether the core switched from the 1 state to the 0 state. Refer to Figure 1-7.

In accomplishing the read-in and readout processes in accordance with requirements imposed on the Output Storage System, various special circuits are employed. These circuits are explained in detail in Chapter 3. The paragraphs which follow explain the over-all relationships of these circuits with each other and with the ferrite core array.

2. Array Read-In

Note: Refer to Figure 1-8.

The ferrite cores of each column and each row of an array receive half-write current from a tape core device known as a core current driver (CCD). (See Figure 1-8.) The CCD is switched from either of two saturated states, 0 and 1. A core is said to be set when it is switched to the 1 state and reset when it is switched to the 0 state. A separate CCD is coupled to each row and each column of the array. When a CCD is switched from the 0 to the 1 state, the associated ferrite cores remain unaffected. However, when the CCD is switched from the 1 state back to the 0 state, a half-write current is transferred to all the ferrite cores in the associated row or column.

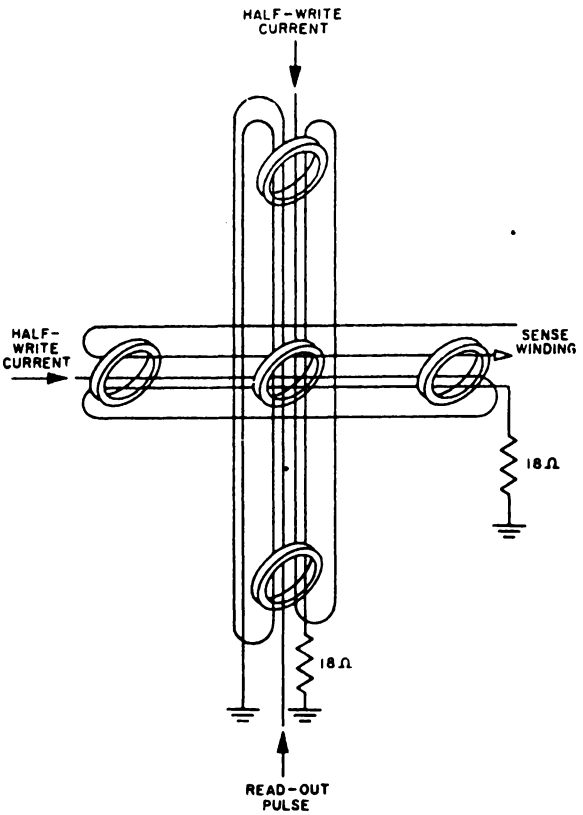


Figure 1-6. Core Windings, Simplified Diagram

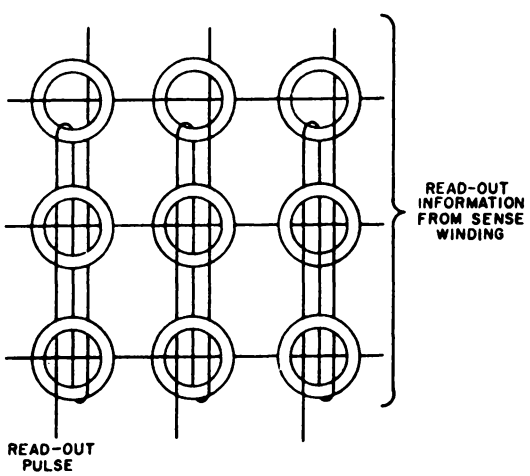


Figure 1-7. Readout by Columns, Simplified Diagram

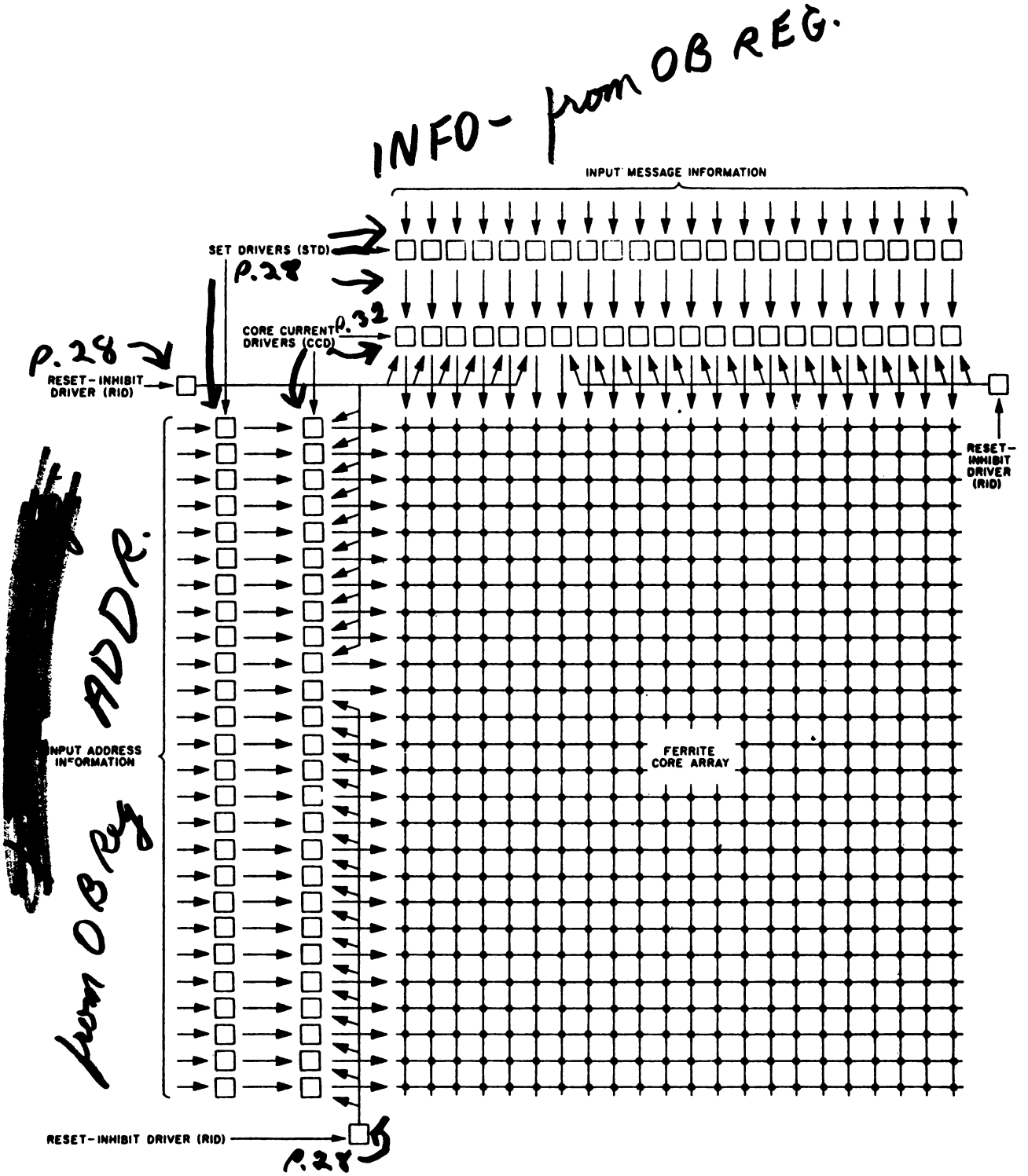


Figure 1-8. Ferrite Core Array with Associated Special Circuit Used for Read-In, Block Diagram

The CCD is set to the 1 state by a circuit known as the set driver (STD). Particular STD's are selected along the address and message axes. Pulsing the selected STD's sets the associated CCD's to the 1 state. The CCD's must now be reset in order to transfer half-write currents into the array.

Associated with each ferrite core array are three identical circuits called reset-inhibit drivers (RID). Each RID is used to reset 16 CCD's, the three RID's simultaneously switching all 48 CCD's. When the RID's are pulsed, all previously set CCD's are reset to the 0 state, causing the read-in of half-write currents into the ferrite cores.

The RID's also perform another function. Information is simultaneously transmitted to all arrays used in the Output System. However, information at a given time is intended for storage in only one array. To prevent entry of information into certain arrays, the RID's associated with these arrays are pulsed in such a way as to reset all associated CCD's. This inhibiting pulse, delivered at the same time the STD's are pulsed, cancels the effect of the set pulse delivered to the CCD's. For that array intended for storing information, the RID does not inhibit the effect of the STD on the CCD.

To summarize the read-in operation: the RID's are used to select the array intended for storing information by inhibiting the setting of CCD's in all other arrays. The selected STD's are pulsed, setting their associated CCD's along the address and message axes of the selected array. Then the RID delivers a reset pulse to the CCD, resetting previously set 1's to 0's. Resetting of the CCD's results in half-write currents being transferred to the associated ferrite cores in the row or column. Upon receipt of two coincident half-write currents, a ferrite core is switched from the 0 state to the 1 state. At the completion of the read-in operation, each selected address register of the array contains word information.

3. Array Readout

The current necessary to read out the ferrite cores in the array is produced by a thyratron core driver (TCD), a circuit which delivers a current output only when triggered. (See Figure 1-9.) One such driving circuit is associated with each column of the array.

Upon receipt of a pulse from a given TCD, all ferrite cores in the corresponding column which were previously switched to the 1 state are switched back to the 0 state.

Triggering of the TCD's is controlled by core shift (CS) units, each unit controlling a separate driver. Each CS contains a tape core which may be saturated in either of two states. This group of CS's is known as the readout shift register.

In order to trigger the TCD's sequentially, one at a time, the CS's of the register must be sequentially switched, one at a time. This process is as follows: The core prime (CP), a driver circuit, pulses the first CS of the register, switching this core from the 0 to the 1 state. Then, all CS's are pulsed simultaneously by the core shift driver (CSD). This latter pulse switches the first core back to 0. The switching causes two things: It switches the second CS from 0 to 1, and it triggers the corresponding TCD which reads out the associated column (switches the ferrite cores to 0). The

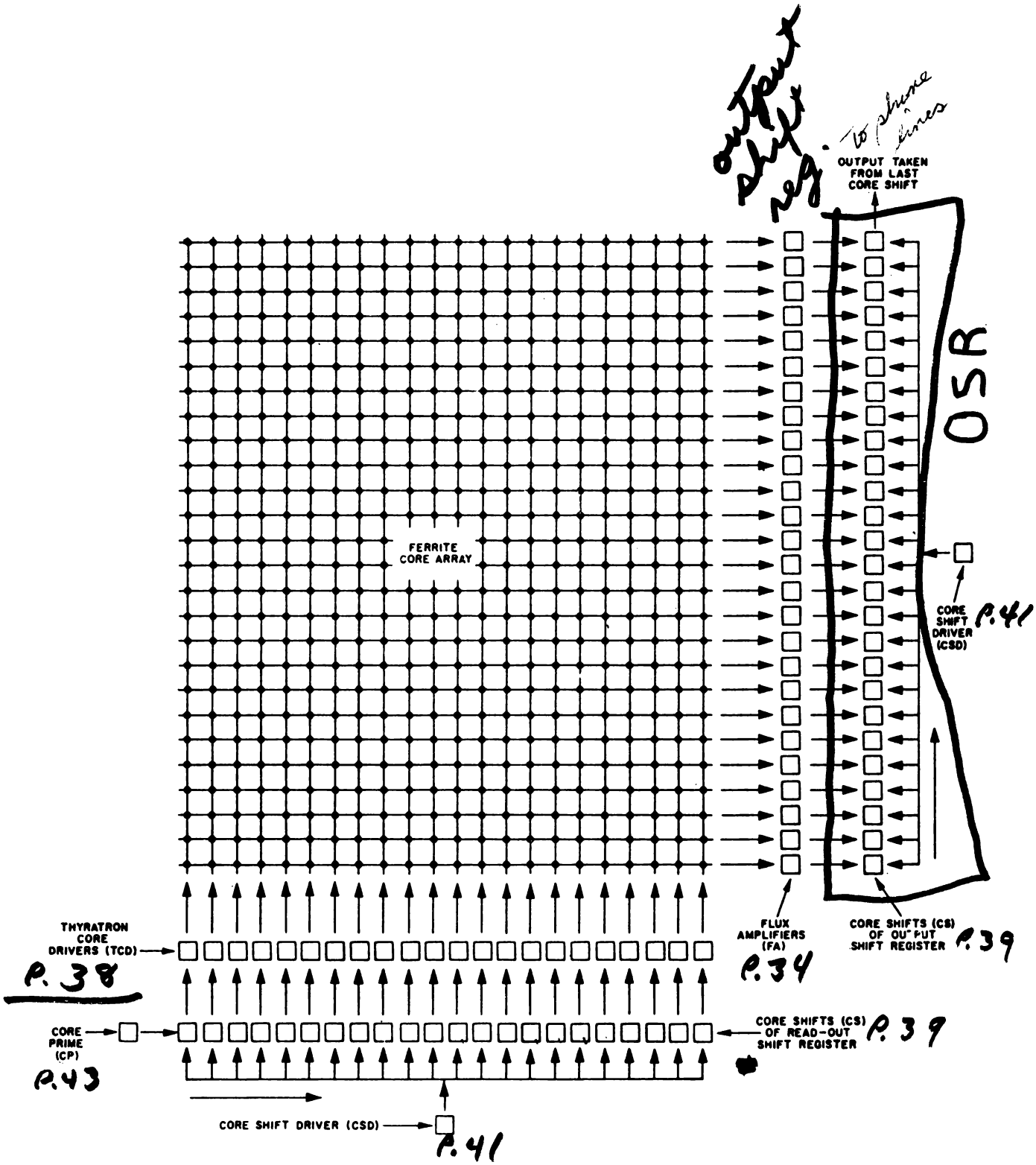


Figure 1-9. Ferrite Core Array with Associated Special Circuits Used for Readout, Block Diagram

CSD is then pulsed again, which switches the second CS back to 0 and the third CS to 1. Switching of the second CS to 0 fires the second TCD, which reads out the second column. This action continues until all columns have been read out. Thus, it might be said that readout information is serially entered into the readout shift register and that message information is taken from the column by parallel readout.

As each column of the array is pulsed, a voltage is induced into the sense winding of each row. Each sense winding drives a flux amplifier (FA). The FA either rejects the sense winding signal if the corresponding ferrite core contained a 0 or accepts it if the core contained a 1. Each FA drives a separate CS of the output shift register (OSR). Ferrite cores that contained 1's cause associated CS's to be switched to the 1 state; ferrite cores that contained 0's allow associated CS's to remain in the 0 state.

Since the information contained in all the ferrite cores of a column is entered simultaneously into the OSR, the register is said to receive this information by parallel entry.

Once the information contained in a column is transferred to the OSR, the CSD associated with the register is then pulsed repeatedly. With each pulse, information contained in each CS is transferred to its succeeding CS. Output from the register is taken from the last CS. The CSD is pulsed until all information is serially read out of the register.

To summarize the readout operation: the first CS in the readout register is switched to the 1 state by a core prime. This is necessary to initiate the serial switching which takes place in the register. As the CSD pulses the readout shift register, the first CS is reset to 0, the second CS is set to 1, and the first TCD is triggered to reset all ferrite cores in the first column to 0. Information contained in the first column is transferred through the flux amplifiers to the OSR. The associated CSD is pulsed repeatedly until all information is serially readout of the register, output information being taken from the last CS in the register.

After the first column has been read out, the CSD associated with the readout shift register is pulsed again. This initiates readout of the second column. This action continues until all columns in the array have been readout. Thus, the word information contained in each row of the array is serially readout column by column. The array is now ready for read-in again.

Special Circuits Used in the Output System

1. Tuning Fork Oscillator

a. Definition and Description

A tuning fork oscillator (TFO) is a non-logic circuit which generates continuous sine waves.

Table 1-4 lists the three models of the TFO's utilized in AN/FSQ-7 and -8 equipments. Each circuit is listed by logic symbol showing the characteristics which

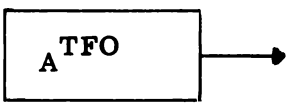
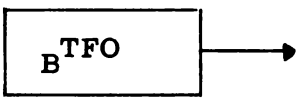
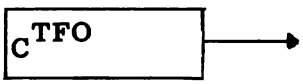
MODEL	LOGIC BLOCK SYMBOL	CHARACTERISTICS
A		Generates sine wave at a frequency of either 512 or 364 cps, depending on application. Amplitude: 45v peak-to-peak.
B		Generates continuous sine wave of 1,300 cps with normal amplitude of 7 to 8v peak-to-peak.
C		Generates sine wave at a frequency of 1,300 cps or 1,600 cps, depending on tuning fork used. Amplitude: 11v peak-to-peak.

Table 1-4. Tuning Fork Oscillators

REFERENCE SYMBOL	FUNCTION
R1	V1 grid return
R2	Plate load resistor for V1
R3	V2 plate load resistor
R4	V2 cathode resistor
R5	Part of feedback network (with C2)
C1	Bypass capacitor
C2	Part of feedback network (with R5)

Table 1-5. Tuning Fork Oscillator, Model B
Function of Detail Parts

distinguish one model from the other. Since all three models operate identically, only model B is discussed in detail.

b. Principles of Operation

The model $_{B}$TFO, shown in schematic form in Figure 1-10, will be discussed as a typical TFO circuit in the following discussion. Table 1-5 lists associated detail parts and their functions.

The $_{B}$TFO produces a continuous 1300 cps sine wave whose period is extremely stable and accurate. The output from the tuning fork is a 0.5v peak-to-peak sine wave which is applied to the grid of V2. This signal is amplified and fed to V1. The output signal from V1 is a positive 3v feedback of proper phase and magnitude to maintain oscillation of the tuning fork.

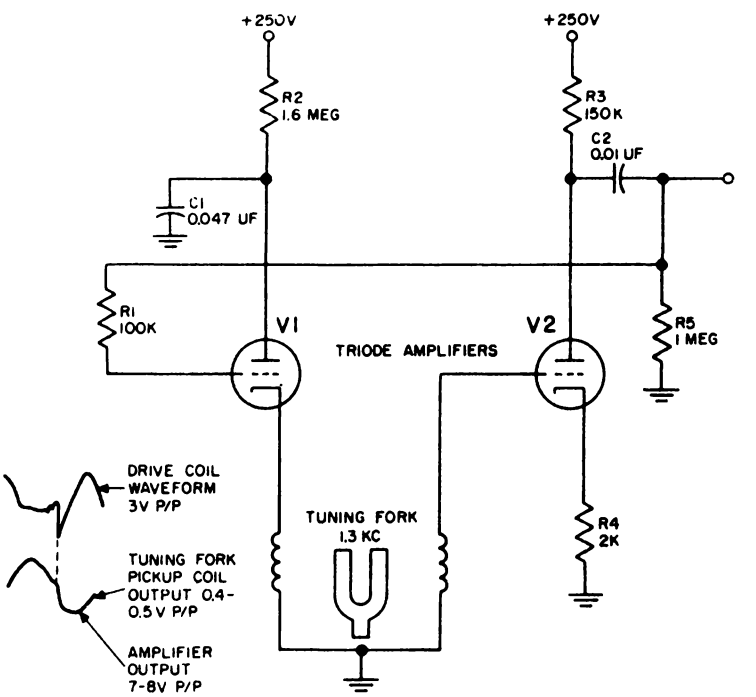


Figure 1-10. Tuning Fork Oscillator
Model B, Schematic Diagram

2. Schmitt Trigger, Model A

a. Definition and Description

The model A Schmitt trigger (AST) is a non-logic circuit which produces a constant amplitude bilevel output and is capable of voltage level discrimination and reasonably fast switching. The logic block symbol for the Schmitt trigger is shown.

b. Principles of Operation

The AST is shown schematically in Figure 1-11. Table 1-6 lists associated detail parts and their functions. In its quiescent condition, the grid of V1A is considerably negative with respect to its cathode. With the application of a rising positive level on the grid of V1A, this tube starts conducting. As conduction increases in V1A, the current through R3 causes a decrease in voltage at the plate of this tube and a consequent proportional drop at the grid of V1B because of the action of voltage divider R5 and R7. As the grid voltage of V1B is lowered, this tube heads toward cutoff. Since there is less conduction through the cathode resistors, the cathode goes more negative, increasing the positive-going difference between the grid and cathode of V1A and thereby driving the tube further into conduction. This action continues in the direction of conduction in V1A and cutoff in V1B until V1A saturates. Any further positive movement of the left grid results only in an increase in grid current. As the voltage level on the left grid is now lowered, a point in reached at which the feedback divider moves the right grid to a point where some conduction starts, raising the cathode slightly. Since the left grid is held by the input voltage and the cathode is now moving positive-wise, V1A tends toward cutoff, further raising its plate and the grid of V1B. The circuit has now switched back to the original state.

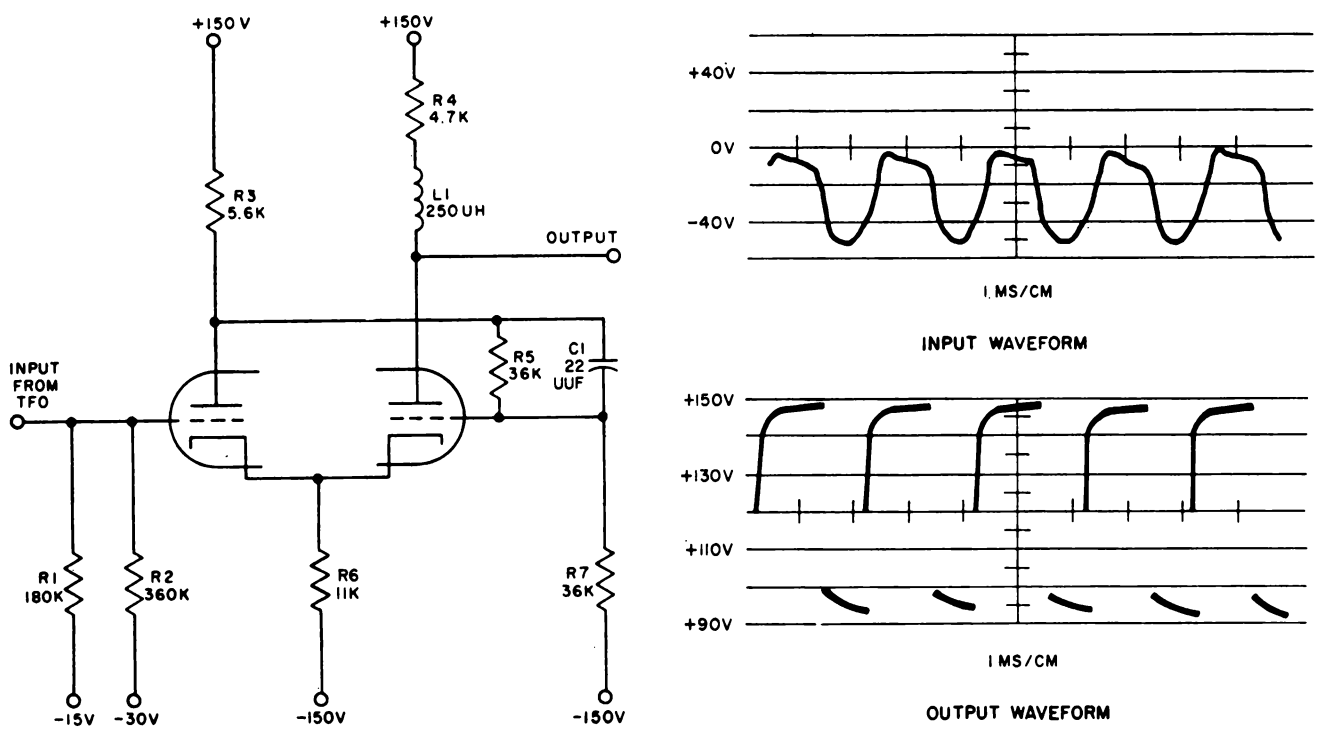


Figure 1-11. Schmitt Trigger, Model A, Schematic Diagram

The input voltage level needed to cause conduction to switch from right to left is somewhat higher than that needed to cause the reverse action. This is due to the difference in the plate load resistors in the two halves of the circuit and produces a hysteresis effect with more inheritability than that found in a symmetrical circuit.

REFERENCE SYMBOL	FUNCTION
R1, R2	Grid bias resistors for V1A
R3	Plate load V1A
R4	Part of V1B plate load (with L1)
R5	Voltage divider (with R7)
R6	Cathode resistor common to V1A and V1B
R7	Voltage divider (with R5)
C1	Part of RC circuit which serves to increase a-c loop gain (with R5)
L1	Choke in plate load of V1B serves to provide peaking action

Table 1-6. Schmitt Trigger, Model A, Function of Detail Parts

3. Constant Voltage Amplifier

a. Definition and Description

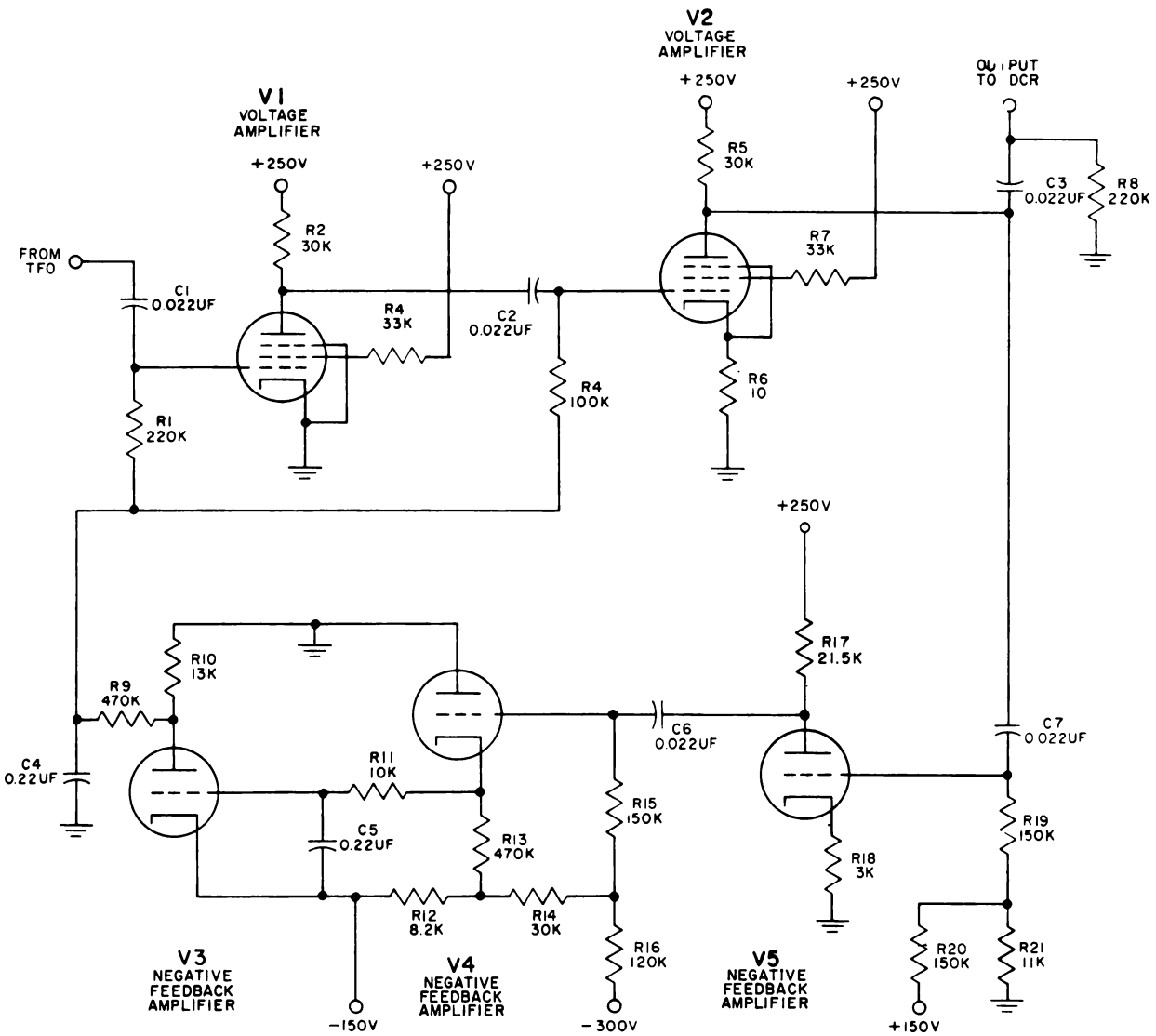
The constant voltage amplifier (CVA) is an amplifier circuit which provides a constant voltage output. The logic block symbol for the CVA is shown in Figure 1-12.

b. Principles of Operation

Figure 1-13 is the schematic diagram of the CVA. Table 1-7 lists the associated detail parts and their functions. The circuit consists of two pentode tubes, V1 and V2, comprising a 2-stage voltage amplifier. The input signal, a 1,300-cycle 7-8v peak-to-peak sine wave, is applied to the control grid of V1. This signal is amplified and applied to the grid of V2 through C2. The output of V2 is a constant 12v peak-to-peak sine wave.

The triode tubes, V3, V4, and V5, comprise a negative feedback network which applies d-c bias to the control grids of V1 and V2. This bias is proportioned to the input voltage. Consequently, automatic regulation for producing a constant 12v peak-to-peak output is achieved for inputs from 2 to 12 peak-to-peak.

Figure 1-12. Constant Voltage Amplifier, Logic Block Symbol



NOTES:

1. SERVICE VOLTAGES ARE DECOUPLED IN THE PLUGGABLE UNIT.
2. PARASITIC SUPPRESSORS HAVE BEEN OMITTED.

Figure 1-13. Constant Voltage Amplifier, Schematic Diagram

The feedback voltage is taken from the output of V2 and coupled through C7 to the grid of V5. Tube V5 amplifies the feedback voltage to 60v peak-to-peak. This 60v signal is applied to the grid of V4 which is operated near cutoff. The output of V4 taken from across C5 is a d-c level which varies in accordance with amplitude variations of the 1,300-cycle, input signal.

This d-c signal is amplified by V3 with capacitor C4 filtering out any remaining 1,300-cycle component present in the signal. The d-c signal is then used to bias voltage amplifiers V1 and V2. Negative bias is increased when the output from V2 tends to exceed 12v; it is decreased when the output tends to become less than 12v.

REFERENCE SYMBOL	FUNCTION
R1	Grid return for V1
R2	Plate load for V1
R3	Screen-dropping resistor for V1
R4	Grid return for V2
R5	Plate load for V2
R6	Provides degeneration for improved regulation
R7	Screen-dropping resistor for V2
R8	Output load resistor
R9, R10	Provides bias for V1 and V2, with R10 as V3 plate load
R11	Part of V4 cathode load (with C5 and R13)
R12	Forms part of voltage divider network (with R14 and R16)
R13	Cathode load for V7 (with C5 and R11)
R14	Part of voltage divider (with R12 and R16)
R15	Grid-dropping resistor V4
R16	Part of voltage divider network (with R12 and R14)
R17	Plate load resistor for V5
R18	Cathode bias for V5
R19	Grid-dropping resistor V5
R20, R21	Voltage divider network
C1-C3	Coupling capacitors
C4	Bypass capacitor
C5	Part of V4 cathode load (with R11 and R13)
C6, C7	Coupling capacitors

Table 1-7. Constant Voltage Amplifier, Function of Detail Parts

4. All-Channel Driver

a. Definition and Description

The all-channel driver (ACD) is a non-logic circuit which produces a sine wave output. The logic block symbol for the ACD is shown in Figure 1-14. In the Output System, the ACD supplies a sine wave output which drives a matching amplifier circuit and a logic driver for each of the channels supplying data to the telephone equipment.

b. Principles of Operation

Figure 1-15 is the schematic diagram for the ACD. The circuit consists of two model D cathode followers of standard design. For details of operation, refer to the cathode follower write-up in the basic circuits manual.

5. Data Conversion Receivers, Models A, C

a. Definition and Description

The data conversion receivers (DCR) are logic circuits which convert sinusoidal input signals into signals suitable for processing within the Input and Output Systems. The principles of operation are similar; for this reason, only the model $_{A}$DCR is described in detail. Model C is shown schematically, accompanied by tables listing the detail parts and their functions.

b. Principles of Operation

Refer to Figure 1-16.

Figure 1-16 is the schematic diagram for the $_{A}$DCR. The $_{A}$DCR employs three double triodes to convert a 2v sine wave into a narrow, negative 50v pulse. Transformer T1 amplifies the input signal by 5 and is connected to produce an in-phase signal across R1. Capacitor C1 and resistor R2 form the first phase shifting network. The network at the grid of V1 leads the T1 output signal by 48 degrees (see waveform 3, Figure 1-16). The unbypassed cathode resistor R4 of V1 minimizes distortion by providing degenerative feedback. Plate load resistor R3 is shunted by C2 to bypass high-frequency noise generated in the telephone lines feeding the $_{A}$DCR. The input to V1 is amplified by 3 and coupled to V2 by the second phase shifting circuits consisting of C3 and R5. The signal at the grid of V2 leads the V1 plate signal by 48 degrees. Cathode resistor R7 of V2 being larger than R4 introduces a larger feedback signal and reduces the gain of V2 to 2.6. The negative bias of -15v on the cathode enables V2 to function as a class A amplifier. The 85v output signal of V2 is coupled to V3 by C5.

Tube V3 is a diode-connected triode. The clipping circuit connected to the cathode of V3 provides a square wave input to V4 and operates as follows. The voltage at the junction of R10 and R11 is -7v. At the junctions of R14 and R15, the voltage is +5v. The difference in potential at these points produces a current through R9, CR2, and R12. The resultant voltage at the anode of CR2 is approximately 0v. During the

Figure 1-14. All-Channel Driver, Logic Block Symbol

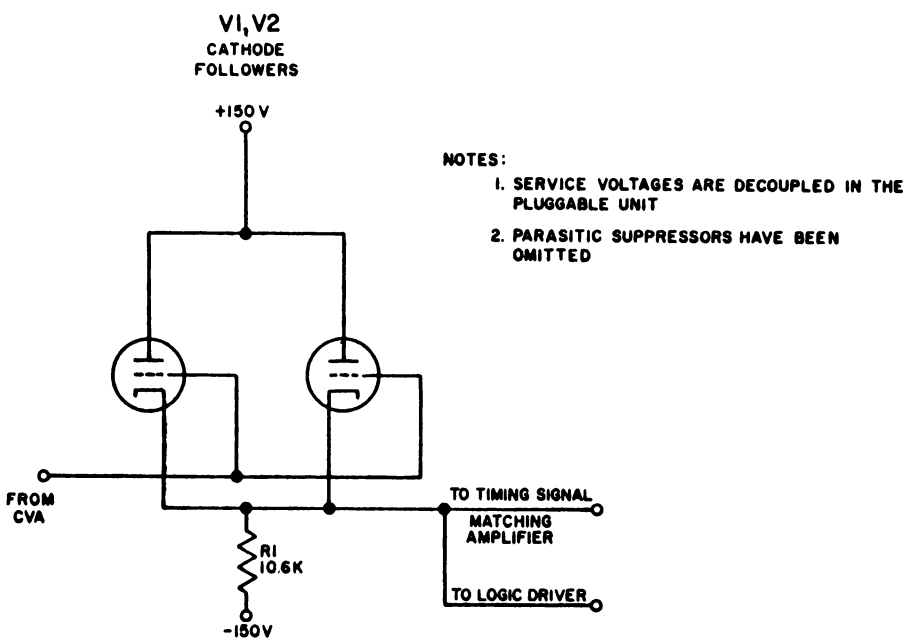
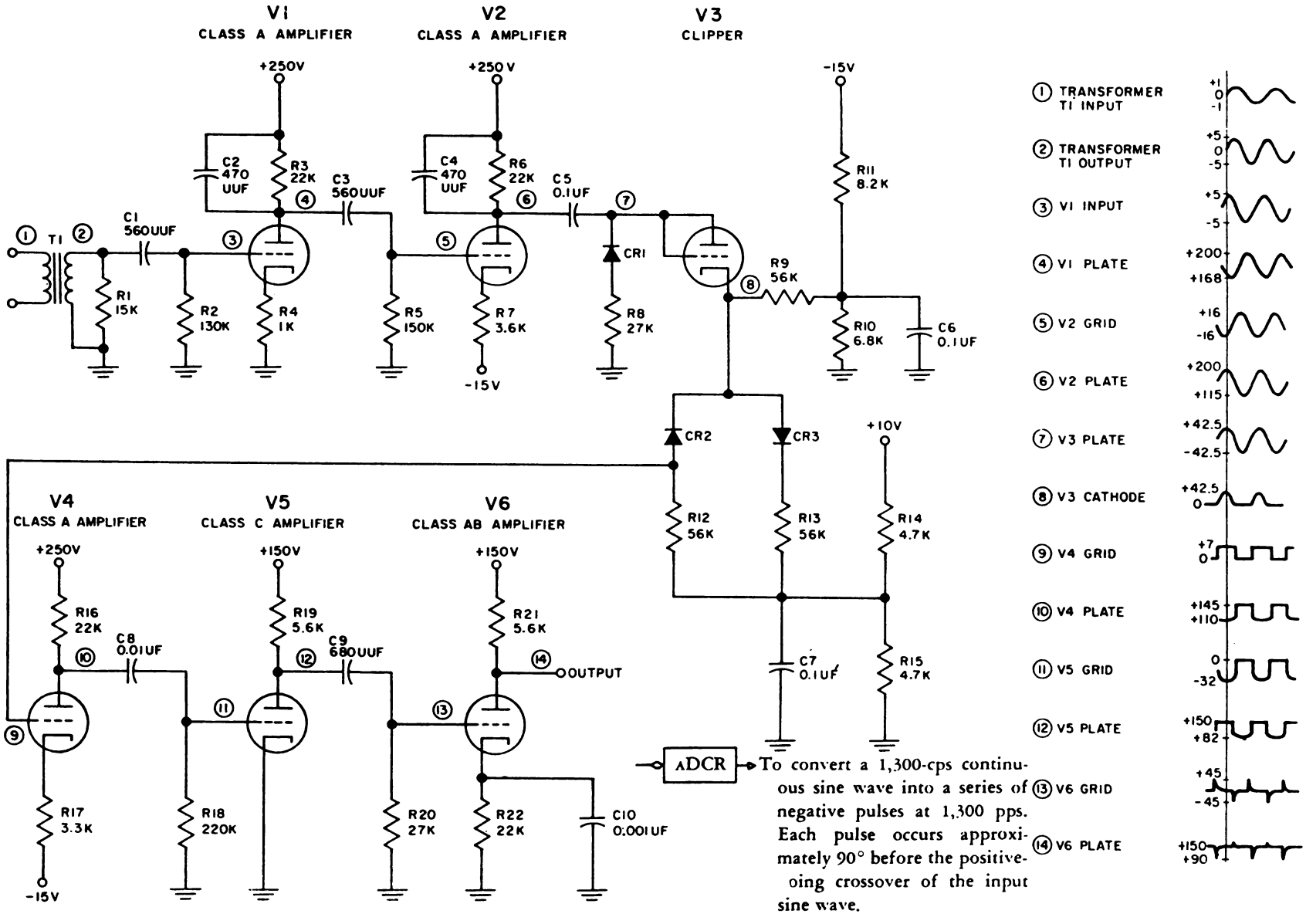


Figure 1-15. All-Channel Driver, Schematic Diagram

negative half cycles of signals developed by V2, clipper V3 is cut off and 0v present at the anode of CR3 is applied to V4. Clipper V3 conducts during the positive half cycle of signals developed by V2. The cathode of V3 follows the plate (see waveform 8, Figure 1-16). A 40v forward bias causes CR3 to conduct, dropping 35v across CR3 and R13. Voltage divider action of the back resistance of CR2 and R12 set the anode of CR2 at +7v. Thus, the grid of V4 is fed by a square wave varying between 0 and +7v at 1,300 cps (see waveform 9, Figure 1-16).

Because of the unbypassed cathode resistor, amplifier V4 conducts throughout the entire input cycle. With the application of the 0 to +7v input signal on the grid, the resultant output is a square wave of 35v peak-to-peak (waveform 10, Figure 1-16) which is coupled by capacitor C8 to the grid of V5.

Tube V5, a class C amplifier, amplifies the square wave output of V4, resulting in a square wave at the plate of V5 (+82v to +150v) which is then differentiated by the network consisting of capacitor C9 and resistor R20. The result is a series of



To convert a 1,300-cps continuous sine wave into a series of negative pulses at 1,300 pps. Each pulse occurs approximately 90° before the positive-going crossover of the input sine wave.

Figure 1-16. Data Conversion Receiver, Model A, Schematic Diagram

negative and positive pulses appearing at the grid of V6. The amplitude of the spikes is 45v (waveform 13, Figure 1-16).

Tube V6 is the final stage of the $_{A}$DCR. This tube operates as a class AB amplifier. The positive and negative spikes from V5 are applied to the grid of V6. The tube conducts during the positive spikes and is cut off during the greater portion of the negative spikes. The resultant output of V6 consists of sharp negative-going pulses with an amplitude of 60v and small positive pulses from slightly under +150v. These small positive pulses result from the fact that the tube is self-biased and these pulses have no deleterious effect on the circuit.

An analysis similar to the one presented above can be applied to the Model C, DCR. Figure 1-17 is the schematic diagram for the model. Table 1-8 lists the associated detail parts and their functions.

6. Set Driver

a. Definition and Description

The set driver (STD) is a non-logic circuit which is used to produce a current pulse to switch tape cores. The logic block symbol for the STD is shown in Figure 1-18.

b. Principles of Operation

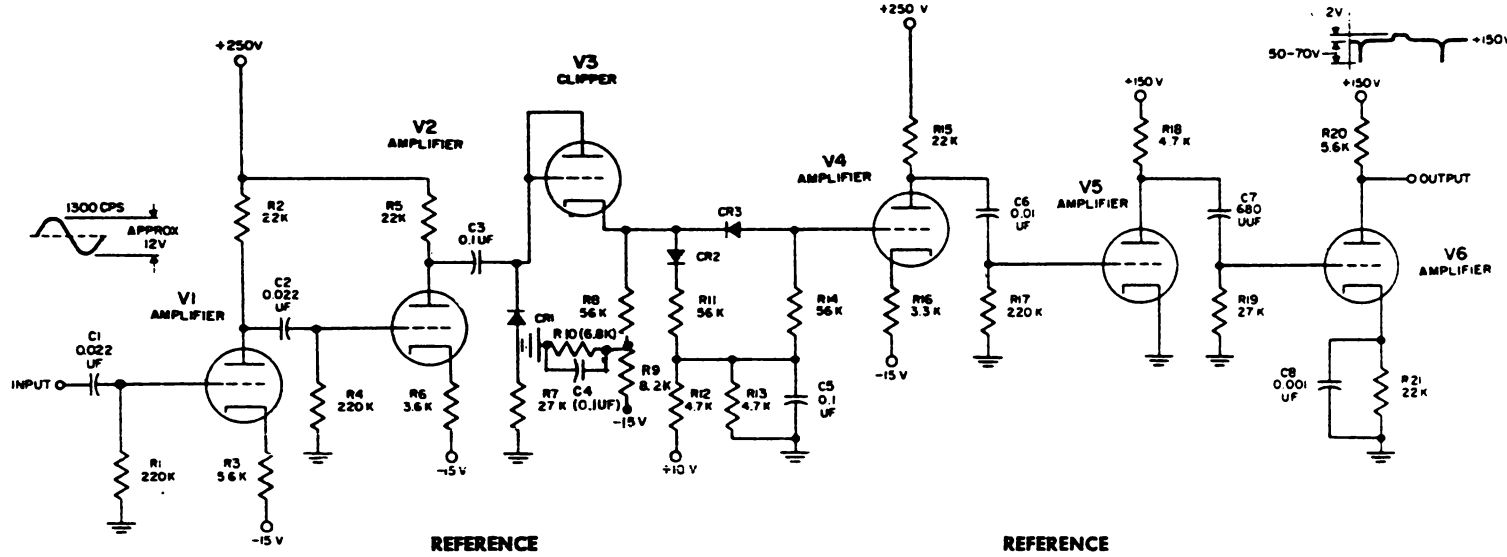
The STD shown schematically in Figure 1-18 consists of a single pentode tube. Input signals are applied to the suppressor and control grids. Inputs to the suppressor grid are from two sources: (1) the suppressor grid of an STD used for the address axis receives its input from the register address decoder, to determine in which row in the core array the information will be written. (2) The suppressor grid of an STD used for the message axis receives its input from the right drum word register which contains the intelligence (message column) to be written in the particular row of the core array. Input to the control grid is from the read-in control circuit.

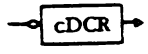
The plate voltage of the STD pentode is obtained from the +250v service voltage supply, and the screen grid voltage from the +90v marginal checking voltage supply. A nominal current of 28 ma flows through the CCD set windings connected in the plate circuit. The tube is maintained at cutoff by the -30v level of a flip-flop circuit that supplies the control grid and by the absence of a positive level on the suppressor grid. The register address decoder or the right drum word register selects a specific row or column and its associated circuitry places a +10v level on the suppressor grid of the selected STD. This signal level (conditioning) is maintained throughout the complete read-in operation (approximately 6 usec). If the address and parity information is correct and the word is correctly timed, the read-in control circuit, through a flip-flop circuit, places a +10v pulse on the control grid of the selected STD.

7. Reset-Inhibit Driver

a. Definition and Description

Figure 1-17. Data Conversion Receiver, Model C (Zero Detector), Schematic Diagram





To produce a series of negative pulses each coincident with the positive-going zero crossover of the 1,300- or 1,600-cps input sine wave.

REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
R1	V1 grid return	R20	V6 plate load resistor
R2	V1 plate load resistor	R21	V6 cathode resistor
R3	V1 cathode resistor	CR1, CR2, CR3	Part of clipping and clamping network (with R7-R14)
R4	Part of RC coupling network (with C2) and V2 grid return	C1	Coupling capacitor
R5	V2 plate load resistor	C2	Part of RC coupling network (with R4)
R6	V2 cathode resistor	C3	Coupling capacitor
R7-R14	Part of clipping and clamping network (with CR1, CR2, and CR3)	C4	Bypass capacitor
R15	V4 plate load resistor	C5	Bypass capacitor
R16	V4 cathode resistor	C6	Part of RC coupling network (with R17)
R17	Part of RC coupling network (with C6) and V5 grid return	C7	Part of RC coupling network (with R19)
R18	V5 plate load resistor	C8	Bypass capacitor
R19	Part of RC coupling network (with C7) and V6 grid return		

Table 1-8

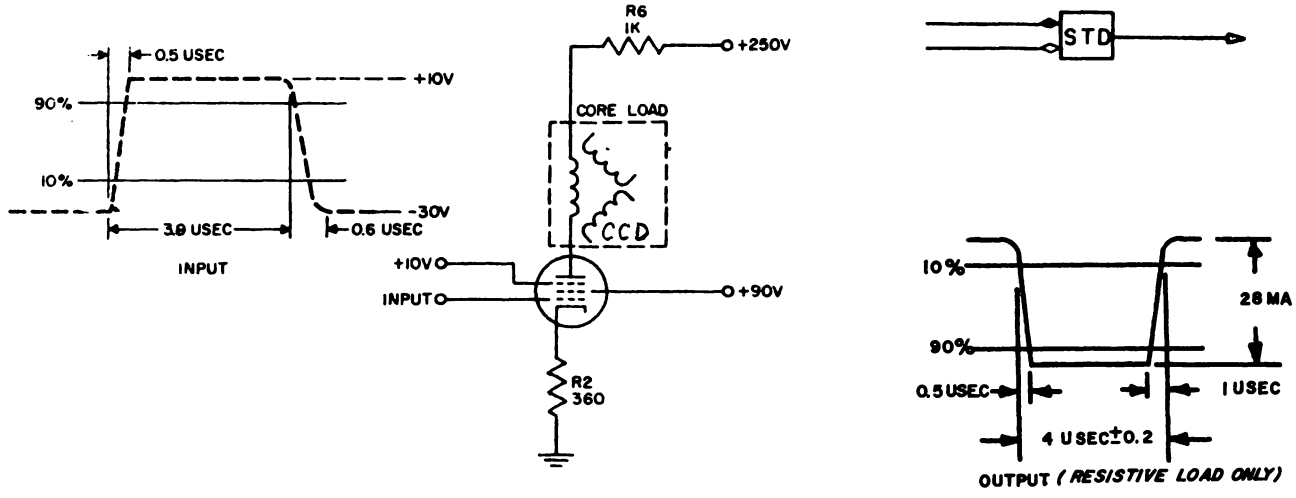

0.5 USEC
+10V
90%
10%
-30V
3.9 USEC
0.6 USEC
INPUT
R6
1K
+250V
CORE LOAD
CCD
+10V
INPUT
+90V
R2
360
STD
10%
28 MA
90%
0.5 USEC
1 USEC
4 USEC±0.2
OUTPUT (RESISTIVE LOAD ONLY)

Figure 1-18

REFERENCE SYMBOL	FUNCTION	REFERENCE SYMBOL	FUNCTION
R1	V1 control grid resistor	R10	Part of plate load for V2 (with L1)
R2, R3, R4	Feedback voltage divider network (with R6)	R11	Load resistance for feedback voltages
R5	V1 plate load resistor	L1	Part of V2 plate load (with R10)
R6	Part of voltage divider feedback network (with R2, R3 and R4)	C1	Input coupling capacitor
R7	V2 control grid resistor	C2	Output coupling capacitor
R8, R9	Voltage divider which provides V2 cathode with —90V bias	C3	Forms part of degenerative feedback circuit which couples plate of V2 to cathode of V1
		C4	Bypass capacitor

Table 1-9. Reset-Inhibit Driver, Function of Detail Parts

Figure 1-19. Reset-Inhibit Driver, Logic Block Symbol

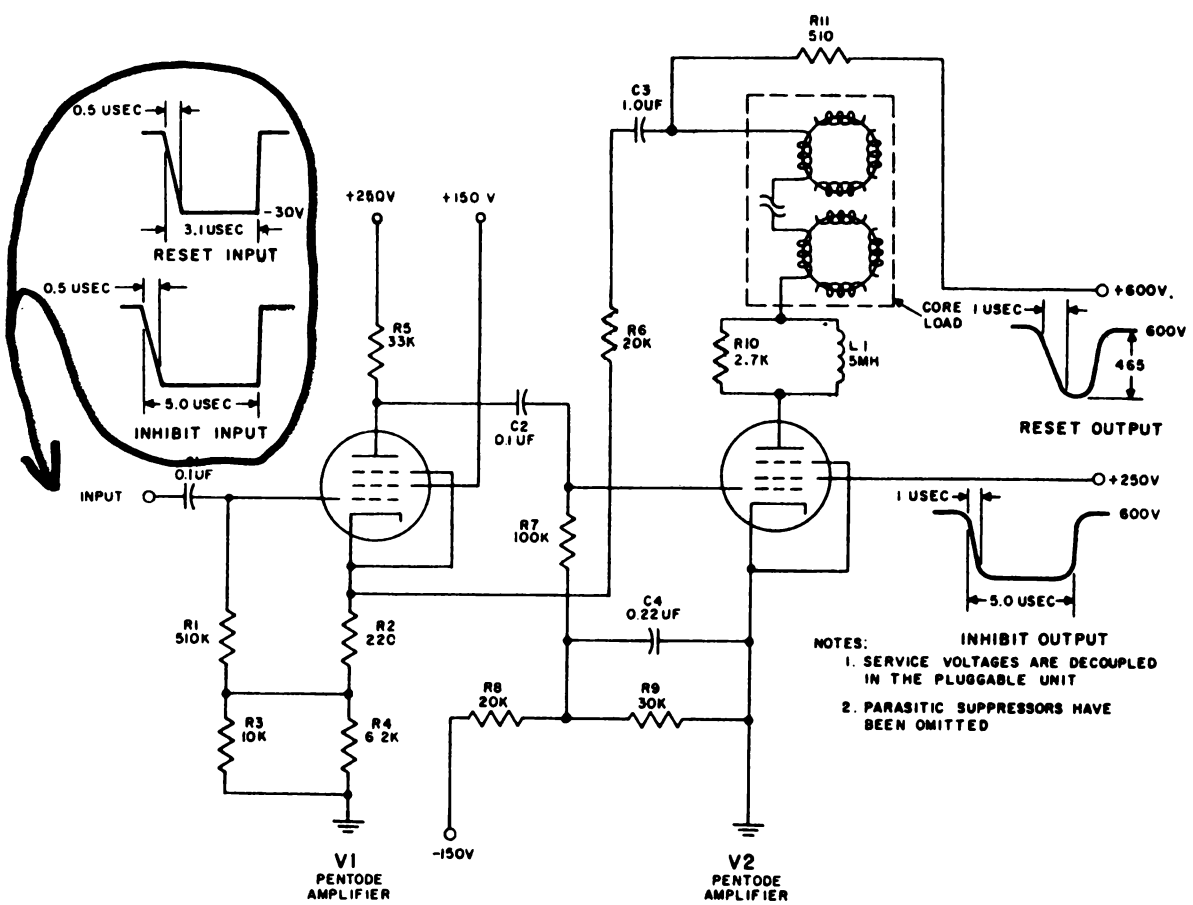


Figure 1-20. Reset-Inhibit Driver, Schematic Diagram

The reset-inhibit driver (RID) is a non-logic circuit which either prevents the read-in of information into an array or furnishes a pulse which produces the read-in of information. The logic block symbol for the RID is shown in Figure 1-19.

Refer to Figure 1-19, Figure 1-20, and Table 1-9.

b. Principles of Operation

Figure 1-20 is the schematic diagram of the RID. Table 1-9 lists associated detail parts and their functions. The circuit is a 2-stage feedback amplifier. The second stage supplies a nominal current of 185 ma to reset or inhibit core current drivers.

The first stage input is a negative pulse of 30v amplitude and having a nominal width of 3.1 or 5.0 usec, depending upon whether the reset or inhibit function is being performed. This pulse is amplified in both stages and delivers current to a load consisting of the reset-inhibit windings of 16 CCD's in series and a load resistance of 510 ohms. The current rise time through the load is approximately 1 usec, thus providing a proper output current pulse from the CCD's during reset time. C3 and R6 form the degenerative feedback circuit coupling the plate of the second stage to the cathode of the first stage; thus, the amplifier functions as a constant current source. The output voltage is obtained from the plate side of the 510-ohm resistor to ground.

The input pulse to the first stage varies from 0 to -30v. When the input drops to the maximum level, the first tube, which has been conducting, is cut off.

The plate voltage, because of no voltage drop across the 33k plate load resistor, rises toward the +250v supply. This rise in plate voltage is coupled through a 0.1-uf capacitor to bring the control grid of the second tube above cutoff, where it has been biased at -90v by the action of the voltage divider across the -150v supply. The positive-going grid voltage results in a flow of plate current through the core load of this stage. The plate voltage drops from the +600v supply output to +135v for a change of 465v.

When the input to the first stage rises to 0v after 3.1 or 5.0 usec, depending upon whether the reset or inhibit function was complete, plate current flows, producing a drop in plate voltage. The second tube is cut off again by this action and its plate voltage rises to the supply output of +600v.

8. Core Current Driver

a. Definition and Description

The core current driver (CCD) is a non-logic circuit which supplies the half-write current to ferrite cores in the ferrite core array of the Output System. The logic block symbol for the CCD is shown in Figure 1-21.

b. Principles of Operation

Figure 1-22 is the schematic diagram for the CCD. Each CCD consists of a metallic tape core upon which are wound three separate windings, a set winding, a

Figure 1-21. Core Current Driver, Logic Block Symbol

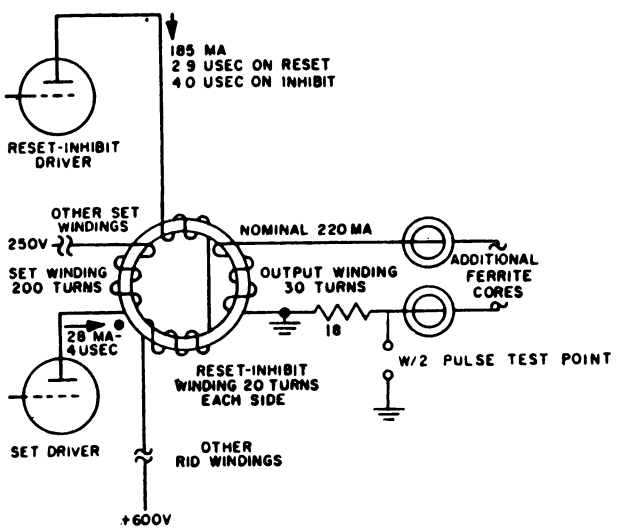


Figure 1-22. Core Current Driver, Schematic Diagram

reset-inhibit winding, and an output winding. The set winding consists of 200 turns and represents the output of the set driver circuit. The reset-inhibit winding consists of 40 turns and represents the output of the reset-inhibit driver. The output winding, which consists of 30 turns, switches the associated ferrite cores in the array by driving a 2-turn winding on these associated cores. Operation of the CCD involves switching the tape core from its reset saturated state to a set saturated state and then back to its original state.

Switching the CCD is influenced by two circuits: the set driver and the reset-inhibit driver. The set windings of the CCD's are connected in series and represent the output load of the set driver circuit. The reset-inhibit windings of the CCD's are connected in series and represent the output load of the reset-inhibit circuit. The output winding of each of the CCD's is series-connected with a 2-turn winding on the ferrite cores in a particular address row or message column of the array.

A CCD is set when its associated set driver is pulsed after the latter has been conditioned by message or address information. The output current of the set driver required to switch from reset to set is nominally 28 ma. Switching from the reset state to the set state produces a pulse in the output winding of the CCD. Since during normal operation the output resulting from a set pulse to the CCD occurs only after the ferrite cores have been read out (driven to a 0 state), this output has a negligible effect on the ferrite cores. The set information is retained in the CCD until the reset-inhibit driver is pulsed. The reset-inhibit pulse resets the CCD, resulting in the CCD's output winding delivering a half-write current to all the ferrite cores in its associated row or column of the array.

For the situation where no information is set into a CCD by its associated set driver, but the reset-inhibit driver passes a current through the core winding, an output current is produced which has a negligible effect on the ferrite core array.

The full-write current necessary to set a ferrite core occurs with the coincidence current produced by two CCD outputs, one driving the address axis and the other driving the message axis.

9. Flux Amplifier

a. Definition and Description

The flux amplifier (FA) is a non-logic circuit which is used to sense output signals, to discriminate between these signals as to amplitude, and to amplify them. The logic block symbol for the FA is shown in Figure 1-23. Note: Refer to Figures 1-23, 1-24, and Table 1-10.

b. Principles of Operation

Figure 1-24 is the schematic diagram of the FA. Table 1-10 lists the associated detail parts and their functions. The circuit utilizes a twin-triode tube, one-half of which amplifies the approximately half-sine-wave output of a row of a ferrite core array; the other half drives the input winding of the associated core shift in the output shift registers.

The input signal is received from the sense winding of the associated row of ferrite cores. This negative pulse core output of approximately 0.35v is stepped up in transformer T1 to approximately 5.0v. A network, consisting of crystal diodes CR1 and CR2 with resistor R2, is used in the control grid circuit of the first stage to prevent unwanted triggering of the circuit by noise or other extraneous pulses. A gating voltage, clamped at standard levels, is supplied to the input transformer's secondary to condition the network and thereby reject spurious signals.

When the gate voltage is normally at its upper level of +10v, the cathode of CR1 is also at this voltage. The -30v supply places the anode of this diode at -30v because CR2 is conducting toward the +150v mc voltage supply through R2. The 40v (+10v level and -30v supply) is across the high back resistance of nonconducting CR1.

REFERENCE SYMBOL	FUNCTION
R1	Load for T1
R2	Forms part of biasing network in grid circuit of first stage (with CR1 and CR2)
R3	Cathode bias resistor for V1A
R4	Forms part of network which is used to increase duration of pulse developed across diode load L2 (with C2 and CR5)
R5	Cathode bias resistor for V1B
R6	V1B plate load resistor
C1	Coupling capacitor
C2	Forms part of network used to increase duration of load pulse (with R4 and CR5)
C3	Cathode bias bypass capacitor
CR1, CR2	Part of biasing network in grid circuit of V1A (with R2)
CR3	Damps out ringing effects between stages
CR4	Forms part of amplitude-disciminating network (with L1 and L2)
CR5	Forms part of network used to increase duration of load pulse (with R4 and C2)
L1, L2	Forms part of amplitude-discriminating network (with CR4)
L3	Plate load for V1A
T1	Step-up input transformer

Table 1-10. Flux Amplifier, Function of Detail Parts

Figure 1-23. Flux Amplifier, Logic Block Symbol

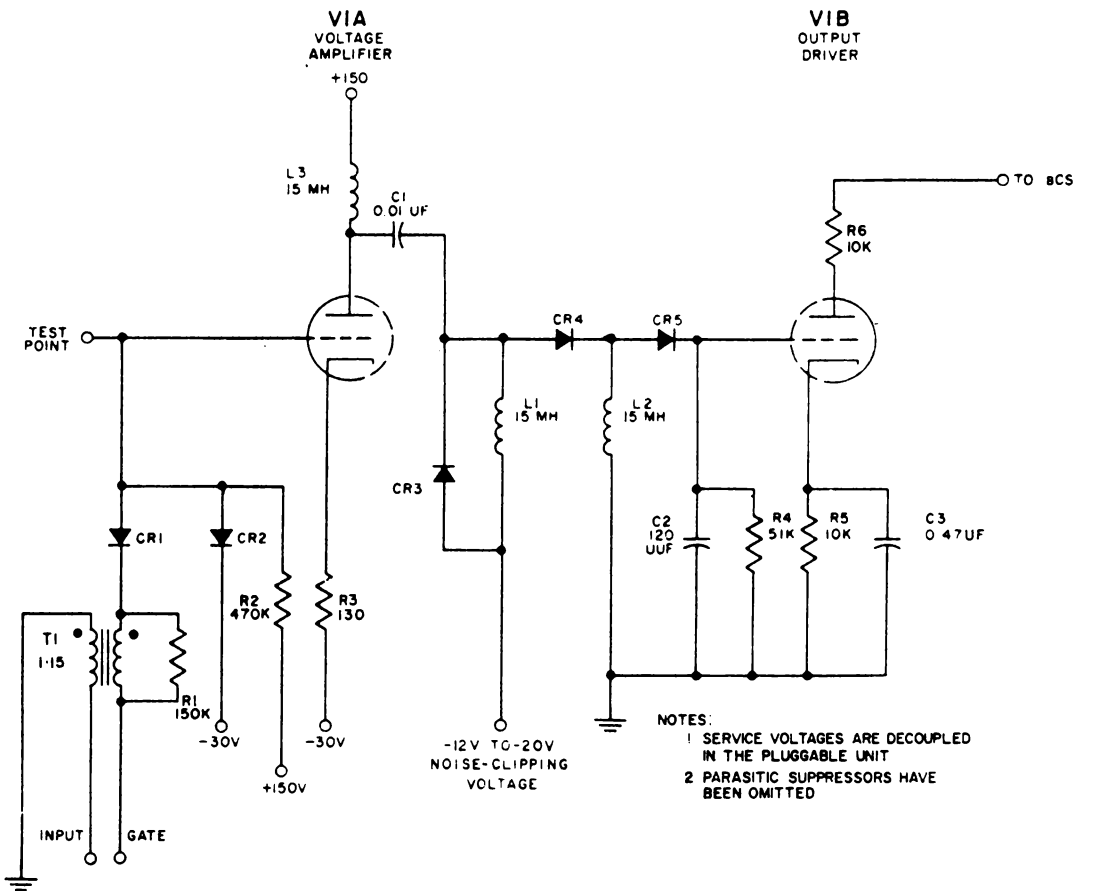


Figure 1-24. Flux Amplifier, Schematic Diagram

This places the control grid at a potential of -30v. The cathode is returned to a -30v supply, but, due to the voltage drop across cathode bias resistor R3, the cathode is less negative than the -30v. This grid-to-cathode voltage biases the tube to the point which allows plate current to flow. Noise or extraneous positive pulses during this time make the cathode of CR1 more positive, preventing the pulse from affecting the control grid of the tube. The pulse voltage is dropped across the high resistance of the nonconducting diode. An unwanted negative pulse during the +10v time of the gate must exceed -40v to cause the diode to conduct. This possibility is remote.

The gate is supplied from the same source that indicates the readout from the ferrite core array. When the array is ready to be read out, the gate drops to -30v, applying the voltage to the cathode of CR1. The anode remains at -30v which results in no potential difference across the diode, and the grid-to-cathode voltage remains unchanged.

The gate duration is 2.5 usec; during this time, a pulse is obtained from the ferrite core array (if a "1" was entered in a core). This negative pulse, between 0.3 and

REFERENCE SYMBOL	FUNCTION
R1	Forms part of input pulse-shaping network (with C2).
R2	Forms part of voltage divider network (with R4)
R3	Grid current-limiting resistor
R4	Part of voltage divider (with R2)
R5	Serves as high resistance source which produces voltage drop necessary to cut off V1.
R6	Screen grid return
C1	Input coupling capacitor
C2	Forms part of input pulse-shaping network (with R1)
C3	Provides output current when discharged
L1	Limits surge voltages when V1 fires or deionizes.

Table 1-11. Thyratron Core Driver, Model A, Function of Detailed Parts

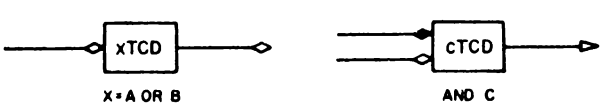


Figure 1-25. Thyratron Core Drivers, Models A, B, and C, Logic Block Symbols

0.5v, after being stepped up through the input transformer, is a negative pulse of approximately 5.0v peak and of 0.25 to 0.45 usec duration. Voltages less negative than -30v cannot cause conduction of CR1; but larger negative voltages such as those obtained during the time of the input from the array, make the cathode of diode CR1 more negative than the anode, causing conduction. This current flowing through resistor R2 and the back resistance of diode CR2 produces a voltage drop which makes the grid negative. The

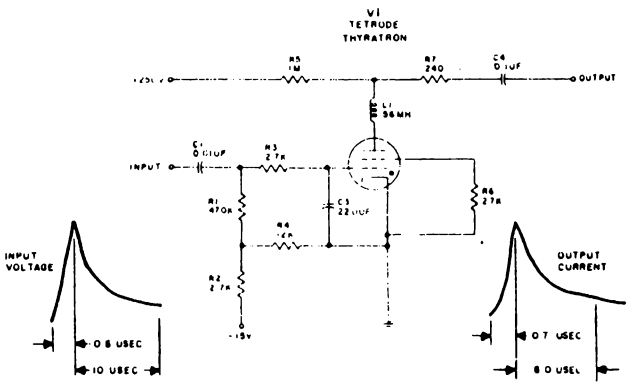


Figure 1-26. Thyrarron Core Driver, Model A, Schematic Diagram

change of plate current produces a large positive increase in plate voltage across inductive load L3.

The signal coupling to the next stage is provided by C1. Diode CR4 is biased negatively on its anode side by the clipping voltage applied through L1, setting a clipping level of -12v to -20v. The pulse from the first stage must exceed the clipping voltage to overcome this bias and cause a transfer of signal to the second stage. This transfer takes place only for a 1 which exceeds +20v; but a 0 input or noise pulses are not large enough to overcome the bias.

The duration of the pulse developed across diode load L2 must be increased to provide a pulse width of 6 usec for writing into the tape core load of the second amplifier stage. This is accomplished in the following manner. Capacitor C2 charges from ground toward the voltage source which is the pulse across L2. When the pulse level falls, the capacitor discharges through R4. The time constant of C2 and R4 is 6 usec. The highest positive value reached by the pulse is 4.0v and, 6 usec (one time constant) later, the pulse amplifier is approximately 2.5v. In discharging to this value in 6 usec, the voltage at 3 usec is still sufficient to produce the required tube current through the tape core load of the tube. The tube is initially biased near cutoff. Upon application of the lengthened pulse, plate current rises. When the input pulse reaches the required voltage, the plate current is sufficient to write a 1 into the core load. The input pulse amplitude remains great enough to maintain the plate current at a value sufficient to prime its core load.

10. Thyratron Core Drivers

a. Definition and Description

A thyratron core driver (TCD) is a logic circuit which produces a peaked current waveform utilized to drive out the contents of a core register. There are three

models of the TCD utilized in AN/FSQ-7 and -8 equipments. The basic difference between models A and B is in the number of cores driven by each. Model C is essentially the same as A and B, except that it is gated.

Model C is used when two ferrite core arrays are required. The gated TCD permits one array to be read out while the other array is prevented from delivering information in cases where the input voltage controlling both readouts comes from a single source.

Since all models of the TCD operate basically the same, only the $_{A}$TCD is discussed in detail. Figure 1-25 contains the logic block symbols of the three TCD's.

b. Principles of Operation

Figure 1-26 is the schematic diagram for the $_{A}$TCD. Table 1-11 lists associated detail parts and their functions. The circuit consists of a tetrode thyratron and its associated circuits.

The grid of the thyratron is biased at approximately -12v established by voltage divider R2 and R4 between -15v and ground. This bias is sufficient to cut off the tube. The input signal, which is 40v to 60v positive, overcomes this bias, triggering the tube. Since the internal resistance of an ionized thyratron is negligible, plate voltage drops from +250v to almost zero. Capacitor C3, originally charged to the +250v supply, now discharges through the driver load consisting of 33 core windings, setting all cores to the 0 state and producing a sense output from those cores that were in the 1 state. The low plate voltage now present at the thyratron is insufficient to maintain current flow through the tube and, as a result, the thyratron deionizes and returns to cutoff. Capacitor C3 again begins to charge through R5 toward the +250v supply, terminating the current flow through the core drive windings.

11. Core Shifts

a. Definition and Description

A core shift (CS) is a logic circuit which possesses two stable states of magnetization and is used as a storage device.

There are 15 models of CS's utilized in AN/FSQ-7 and -8 equipments. The most significant differences between each model are in the number of windings used and the number of turns in each winding. The basic CS contains three windings: an add-in (or read-in) winding, a readout winding, and a drive winding. All other CS's contain a fourth winding, the reset winding. In addition, several models contain a fifth winding, either inhibit or feedback, depending on its application in a circuit. Basically, the principles of operation for all CS's are identical. For this reason, only the basic CS is described in detail below. Figure 1-27 shows the logic block symbol of a basic CS.

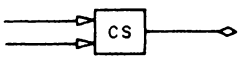


Figure 1-27. Basic Core Shift, Logic Block Symbol

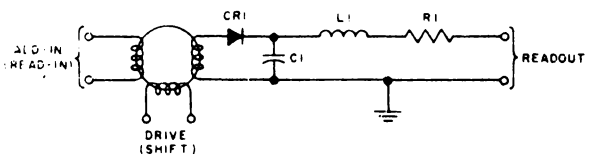


Figure 1-28. Basic Core Shift, Schematic Diagram

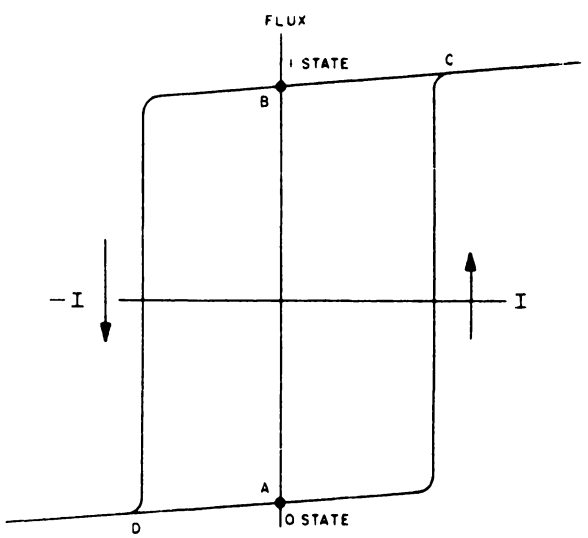


Figure 1-29. Typical Magnetic Tape Core Hysteresis Loop

b. Principles of Operation

Figure 1-28 is the schematic diagram of the basic CS. The core shift consists of three windings: an add-in (or read-in) winding, a readout winding, a drive winding, and associated components.

The magnetization state (1 or 0) of the core is varied by the application of current pulses applied to its add-in and drive windings. The magnetizing process follows the hysteresis loop illustrated in Figure 1-29. Assume (Figure 1-29) that the core is initially at flux point A (0 state). The application of a positive current pulse to the add-in winding changes the flux state of the core to the point represented by C. When the current returns to 0, the flux value decreases to the point represented by B (1 state). A negative-current pulse applied to the drive winding will then change the flux state of the core to the point represented by D. When this current returns to 0, the flux value returns to point A and the core is once again at the 0 state. The flux value remains at point A until the application of a second positive pulse.

The application of a pulse to the drive winding will always cause the core to store a 0 regardless of its previous state. If the core had been storing a 1, applying a pulse to the drive winding causes a reversal in the direction of core magnetization. As a result, the core is cleared and returns to the 0 state. If the core had been storing a 0, the application of a pulse to the drive winding has no effect on the magnetization and the induced output voltage is negligible.

The readout circuit of a CS makes possible the transfer of a 1 from one core to another. This transfer function is utilized in CS registers. As described previously, when a CS is magnetized in the 1 state, the application of a negative-current pulse to the drive winding causes a reversal in the magnetization of the core. This induces a voltage across the readout winding which charges capacitor C1 (Figure 1-28) through diode CR1. Diode CR1 prevents the capacitor from discharging through its charging path. Inductor L1, because of its high impedance, prevents the initial surge of the C1 charging current from flowing through the parallel path which includes the read-in winding of the next CS and resistor R1. The value of R1 determines the discharge time of C1. This resistance is sufficiently high to enable C1 to retain a considerable charge after the decay of the drive pulse. At the end of the drive pulse, C1 discharges completely through L1, R1, and the read-in winding of the next core. The discharge current writes a 1 into this core. This transfer of a 1 occurs whenever a drive pulse is applied to the drive windings of a core storing a 1. Thus, a stored 1 can be shifted through a register by applying as many drive (shift) pulses as there are CS's in the register.

12. Core Shift Drivers

a. Definition and Description

A core shift driver (CSD) is a non-logic circuit which provides the current necessary to transfer information serially through a register. Table 1-12 lists the seven models of CSD's utilized in AN/FSQ-7 and -8 equipments. Each model is listed by its logic block symbol showing the characteristics which distinguish one model from the other.

b. Principles of Operation, Model C

The $_{C}$CSD is a typical CSD circuit and is used as an example of CSD circuits in general in the following discussion.

The $_{C}$CSD, shown in schematic form in Figure 1-30, consists of a pentode amplifier and associated components. The plate load of the stage consists mainly of the series-connected CS drive windings or the add-in windings. In its quiescent state, the voltage at the grid of V1 is -30v which is the effective bias on the tube, and the cathode is at ground potential. The input signal to the stage, which is developed across grid return resistor R1, is a pulse +10v in amplitude and approximately 3.5 usec (bias-width) in duration. As this input voltage rises to +10v, the bias on the tube is overcome, and the stage conducts. When the stage conducts, plate current flows through the core load in the shift register. When the stage is being employed to amplify drive pulses, the plate current magnetizes the cores in a direction opposite that caused by setting a 1 into the cores. When the stage is being employed to amplify add-in pulses, the plate current magnetizes the cores in such a direction as to set the cores to 1.

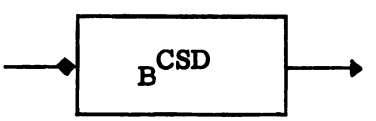
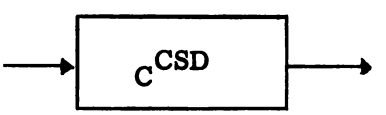
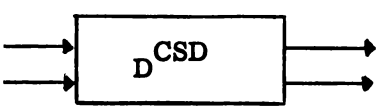
MODEL	LOGIC BLOCK SYMBOL	CHARACTERISTICS
A	$_{A}$CSD*	Provides current to drive eight cores in the shift register of the manual data input unit.
B		Provides current to read out tape cores in 3-output shift register of output storage section.
C		Provides read current for the core shift register.
D		Provides add-in current in tape-core counter.
E	$_{E}$CSD*	Provides shift current in tape core counter.
F	$_{F}$CSD	Provides shift current in the parallel read-out and identification register.
G	$_{G}$CSD	Provides current to reset cores in azimuth counter.

Table 1-12. Core Shift Driver, Model-Distinguishing Characteristics

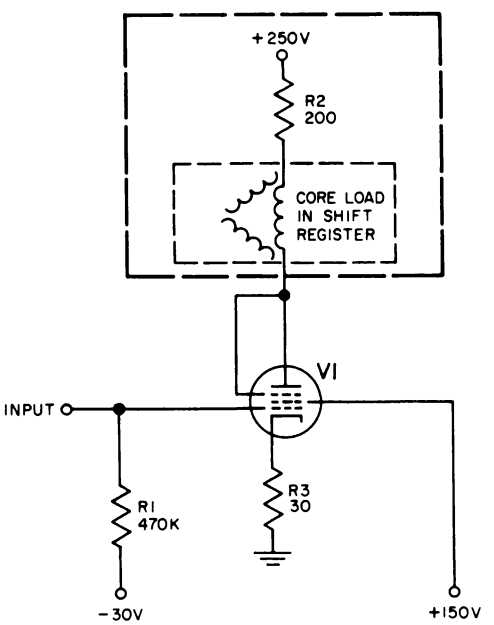
*Logic block symbols for these models identical with that for model $_{C}$CSD.

13. Core Prime, Models A, B, C, and D

a. Definition and Description

A core prime (CP) is a non-logic power-amplifying circuit which provides a high-current output pulse utilized to set a core shift to the "1" state.

Table 1-13 lists the four models of CP's utilized in AN/FSQ-7 and -8 equipments. Each circuit is listed by logical symbol showing the characteristics which distinguish one model from the other.



NOTES:

1. SERVICE VOLTAGES ARE DECOUPLED IN THE PLUGGABLE UNIT
2. PARASITIC SUPPRESSORS HAVE BEEN OMITTED

Figure 1-30. Core Shift Driver, Model C, Schematic Diagram

b. Principles of Operation

Refer to Figure 1-31 and Table 1-14.

The electronic operation of the models is identical; therefore, only the model A is described in detail. The schematic diagram for the $_{A}$CP is shown in Figure 1-31. Table 1-14 lists the associated detail parts and their functions. The circuit consists of a cathode follower and associated components.

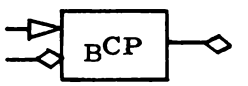
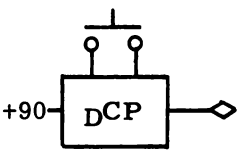
MODEL	LOGIC BLOCK SYMBOL	CHARACTERISTICS
A		Drives a model A, B, or C core shift with standard level input pulse.
B		Drives a model C core shift with either a standard pulse input or with a 1 output from a core bit.
C		Drives one or two model C core shifts connected in parallel upon application of an input pulse that consists of a 1 output from a core bit.
D		Drives a model C core shift with an output current which is generated within the circuit by the discharge of a capacitor through a choke, resistor, and core input winding in series. The depression of a pushbutton permits this to occur.

Table 1-13. Core Prime Model - Distinguishing Characteristics

REFERENCE SYMBOL	FUNCTION
R1	Plate current-limiting resistor
R2	Grid-limiting resistor
R3	Grid return resistor
R4, R5	Form voltage divider which determines grid bias
R6	Prevents CP from conducting due to transformer action when the core shift driver is pulsed
C1	Input coupling capacitor
C2	Places junction of voltage divider R4 and R5 at a-c ground potential
CR1	Crystal diode which serves to prevent d-c restoration action at input

Table 1-14. Core Prime, Model A, Function of Detail Parts

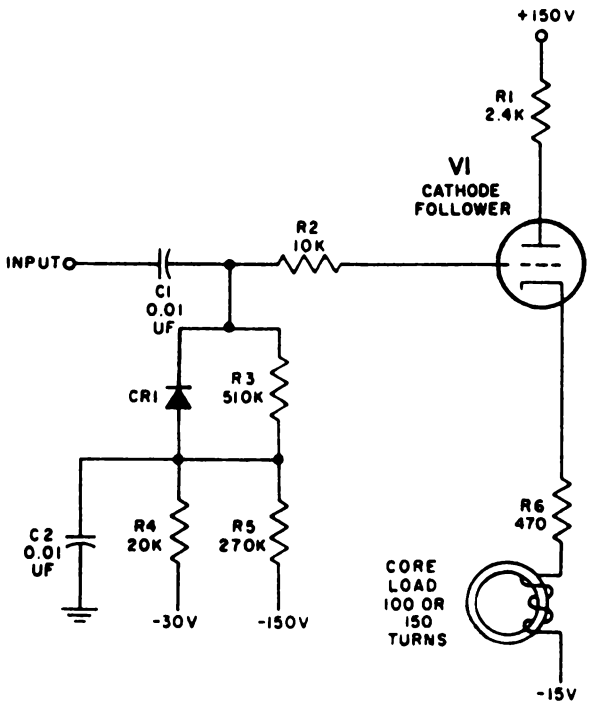


Figure 1-31. Core Prime, Model A, Schematic Diagram

With no input signal, a negative voltage of approximately 22v (grid to cathode) maintains the tube at cutoff. This voltage is obtained by connecting the grid circuit to a voltage divider which is connected to the -30 and -150v supplies and by connecting the cathode circuit to the -15v supply. The voltage divider is placed at a-c ground potential by a capacitor which is located at the junction of the two resistors comprising the divider.

When a -30v level is applied to the input of the CP, the tube remains at cutoff; when the pulse level rises to +10v, plate current flows. The plate current, returning to the cathode through the input or prime winding of the core load, switches the core to the 1 state. When the input pulse level reaches +10v, the grid becomes positive, causing grid current to flow, causing the coupling capacitor in the input circuit to charge. This tends to build up the bias, producing a d-c restoration action. However, this condition is prevented by the action of crystal diode CR1 in discharging the coupling capacitor rapidly.

14. Matching Amplifier, Model A

a. Definition and Description

The model A matching amplifier ($_{A}$MA) is a non-logic circuit which performs the function of impedance matching. There are two types of MA's. Type 1 is used to match

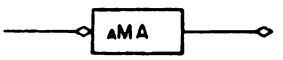


Figure 1-32. Matching Amplifier, Model A, Logic Block Symbol

REFERENCE SYMBOL	FUNCTION
R1	Grid return for V1
R2	Bias resistor to assure linear operation of V1
C1	Coupling capacitor for type 1 input
C2	Bypass capacitor for R2
T1	Stepdown transformer serving as cathode follower load

Table 1-15. Matching Amplifier, Model A, Function of Detail Parts

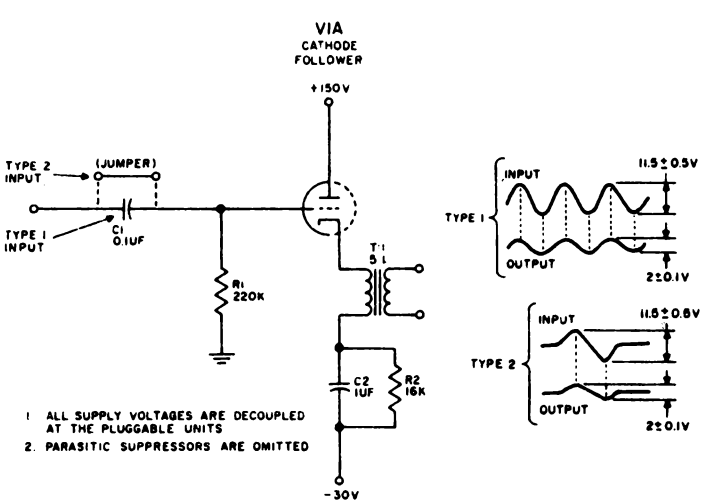


Figure 1-33. Matching Amplifier, Model A, Schematic Diagram

the impedance of the all-channel driver to a 600-ohm line, and type 2 matches the logic gate circuits to a 600-ohm line. Both MA circuits are identical except that type 1 uses a coupling capacitor in its input, and, in type 2, the capacitor is replaced by a jumper. The logic block symbol for the MA is shown in Figure 1-32.

b. Principles of Operation

Figure 1-33 is the schematic diagram for the matching amplifier. Table 1-15 lists associated detail parts and their functions. The $_{A}$MA is a cathode follower type circuit which has a 5:1 stepdown transformer in the cathode circuit. As in all cathode follower circuits, there is no phase shift between the input and output signal. A sinusoidal current through the tube, caused by a sinusoidal voltage input, produces a sinusoidal voltage at the output terminals of transformer T1. The output of this circuit for an input signal of 11.5v (peak-to-peak) is approximately 2v.

The input signal to the $_{A}$MA, type 1, is a 1,300 cps sine wave, 11.5 $\pm$ 0.5v peak to-peak and the output, when terminated with 600 ohms, is a continuous 1,300 sine wave, 2v peak-to-peak. Type 2 has input and output signals of the same frequency and magnitude but instead of being continuous they are gated.

15. Logic Driver, Model A

a. Definition and Description

The model A logic driver (ALD) is a non-logic circuit which produces a continuous sine wave at ground potential. The logic block symbol for the ALD is shown in Figure 1-34.

In output system logic, the ALD is used in the model A data conversion transmitter to drive two 2-way AND circuits.

b. Principles of Operation

Figure 1-35 is the schematic diagram for the ALD. Table 1-16 lists the associated detail parts and their functions. The circuit consists of an ac-coupled cathode follower with an inductive cathode load. The input signal is a continuous sine wave of 1,300 cycles with a peak-to-peak amplitude of approximately 11.5v. The cathode load consists of a 2.5-henry choke whose impedance is more a function of frequency than of d-c current. The choke is connected to the voltage divider consisting of R3 and R4; this connection is made to compensate for the d-c voltage drop across the choke. The values of R3 and R4 are chosen to provide approximately a ground level for the output signal which is identical with the input except that its amplitude is 11.4v.

Figure 1-34. Logic Driver, Model A,
Logic Block Symbol

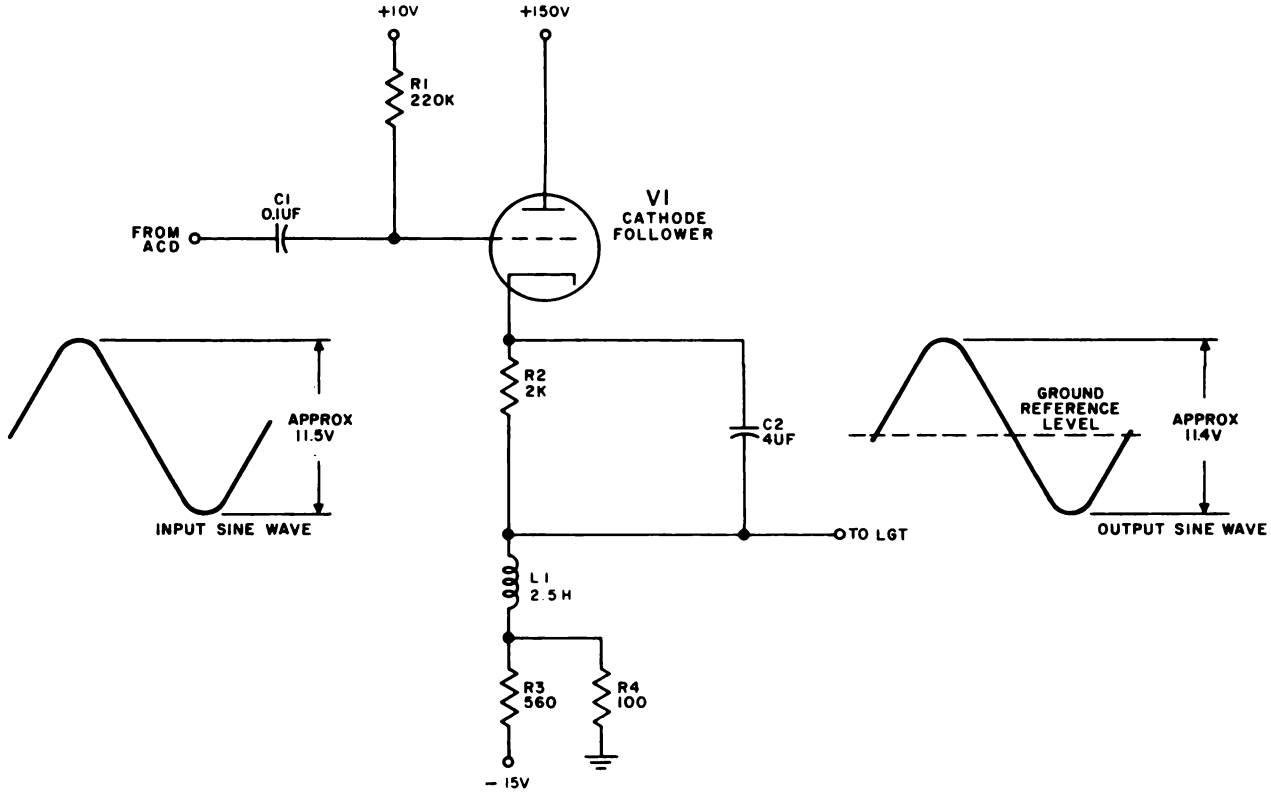


Figure 1-35. Logic Driver, Model A, Schematic Diagram

REFERENCE SYMBOL	FUNCTION
R1	Grid return for V1
R2	Cathode resistor
R3, R4	Voltage divider which compensates for d-c voltage drop across L1
C1	Coupling capacitor
C2	Capacitor bank (four 1-uuf capacitors in parallel) serving as part of cathode load (with L1)
L1	Choke, serving as part of cathode load (with C2)

Table 1-16. Logic Driver, Model A, Function of Detail Parts

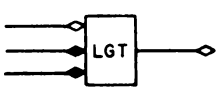


Figure 1-36. Logic Gate, Logic Block Symbol

16. Logic Gate

a. Definition and Description

The logic gate circuit (LGT) is a logic circuit which produces either a 1,300 cycle sine wave or a ground level, depending on its input conditions. The logic block symbol for the LGT is shown in Figure 1-36.

b. Principles of Operation

Figure 1-37 is the schematic diagram for the LGT. Table 1-17 lists the associated detail parts and their functions. The inputs to the LGT are taken from a flip-flop which is controlled by data pulses from the output storage section and timing pulses from the output control element. A 1,300 cycle sine wave timing signal is also supplied from the logic driver. Standard AND and OR circuits are used for logical gating. The logic driver supplies current to the AND circuit when the other AND input is up at +10v. The output from the AND circuit is -30v when the input from the flip-flop is -30v and an 11.8v peak-to-peak sine wave when the input from the flip-flop is at +10v.

To remove the sine wave representing sync or data information from the 30v pedestal, the AND circuit output is fed to its associated OR circuit which also receives

REFERENCE SYMBOL	FUNCTION
R1, R2	Form split cathode load for cathode follower
R3	Load resistor for AND circuit
R4	Load resistor for OR circuit
C1	Compensating capacitor
CR1, CR2	Standard AND circuit
CR3, CR4	Clamps OR circuit input at —30V
CR5, CR6	Standard OR circuit

Table 1-17. Logic Gate, Function of Detail Parts

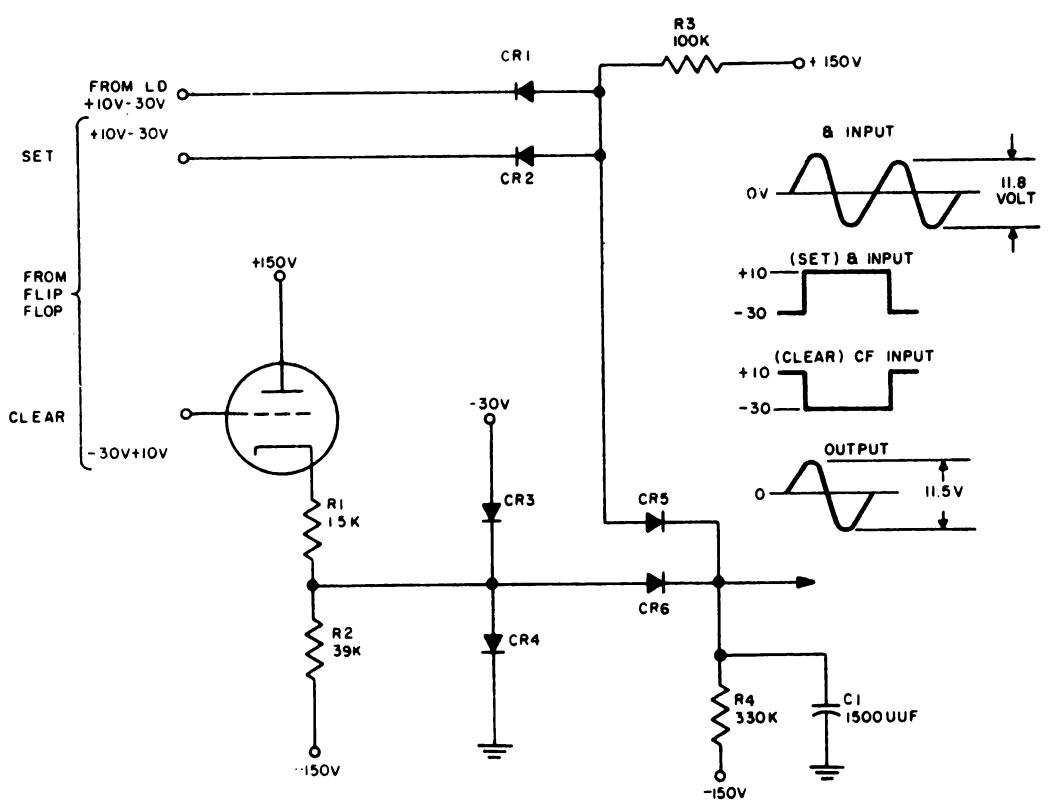


Figure 1-37. Logic Gate, Schematic Diagram

a ground or -30v level input from the OR driver cathode follower uses a split cathode load resistance in its cathode in order to obtain an output of either ground or -30v. When the output of the AND circuit is at -30v, the cathode follower output is at ground potential. Consequently, the OR circuit output is at ground when no data or sync signals are present. When data or sync signals are present, the OR circuit output consists of 12v peak-to-peak gated sine waves at ground reference level.

Output System, Block Diagram Analysis

1. General

The Output System transmits each output message from the Central to the intended destination of the message. The transmission is done in serial form during the proper burst period and at the correct rate of transmission over either a telephone data channel or a telephone teletype channel. The Output System is composed of two elements, the output control (unit 42) and the output storage (unit 33). These elements perform the Output System functions. A separate discussion of each element follows related to the Output System block diagram (Figure 1-38).

2. Output Control Element, Block Analysis

Although the output control element has several functions, it primarily controls the flow of right half-words from the OB fields to the output storage element. Secondly, the output control element makes available to the Central Computer System the contents of the G/G, G/A-TD, and TTY burst counters. Specifically, there are three burst time counters. Each section has its own burst time counter. This information aids the Central Computer System in assigning the proper burst number to future bursts. The output control element also provides visual indications of any alarm conditions that might occur in the Output System. Furthermore, this element contains test equipment which can detect the sources of trouble within the Output System and can also be used to aid in checking certain elements of the Input System.

The output control element receives 33-bit drum words successively from the OB fields at the maximum rate of 100,000 drum words per second. As each drum word appears, the section and register addresses are decoded and a parity count is made of the bits of the drum word. The parity count is initiated by an OB-loading pulse that is received from the Drum System simultaneously with each drum word. Coincidental with the decoding of the section and register addresses and the parity check, the burst number is compared to the contents of the G/G, G/A-TD, and TTY burst counters. Each burst counter is associated with an Output System storage section. If the burst number of the drum word is equal to the contents of any one burst counter, the output control element generates either a G/G-compare, G/A-TD-compare or TTY-compare level. The specific level generated depends upon the burst counter whose contents match the burst number.

A compare level generated in the output control element will start the transfer of the right-half drum word from the output control element to the output storage element if the following conditions are met:

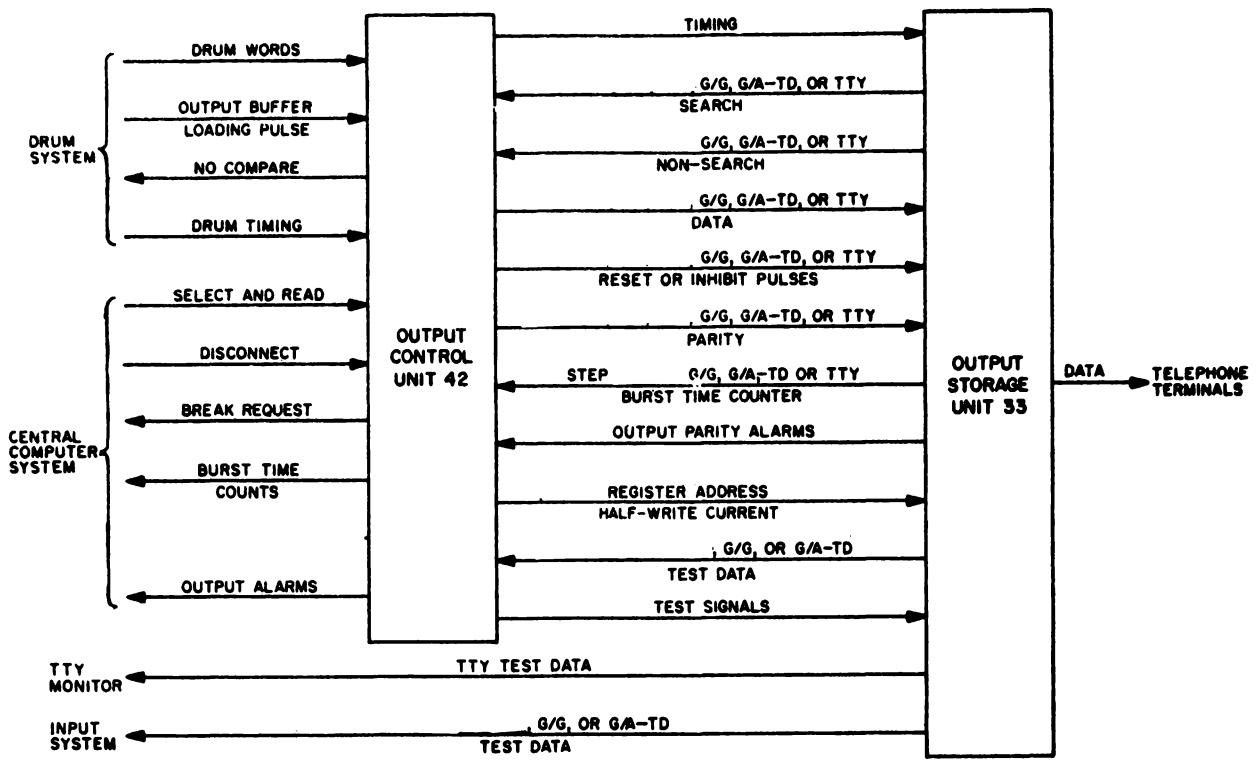


Figure 1-38. Output System (3.0), Simplified System Diagram

a. The correct storage section must have been selected; this is indicated by the section address (e.g., the G/A-TD storage section). Refer to Figure 1-39.

b. The compare level must be received from the burst counter associated with the selected storage section. (If the G/A-TD storage section is selected, it is required that the G/A-TD-compare level be received.)

c. The parity count result must be odd.

d. Receipt of the drum word from the OB fields must occur during search time for the selected storage section. (If the G/A-TD storage section is selected, receipt of the drum word must occur during the G/A-TD search time.)

The last condition is controlled by the output storage element which applies three levels to the output control element; each level indicates search time for a different storage section. These levels are labeled search G/G, search-G/A-TD, and search-TTY, respectively. If the search level is up for a particular storage section, and the other listed conditions are also met, a correct compare level causes the transfer of the 16 bits of the right-half drum word to the selected storage section as half-write message pulses. A half-word-address pulse, which results from decoding the register address,

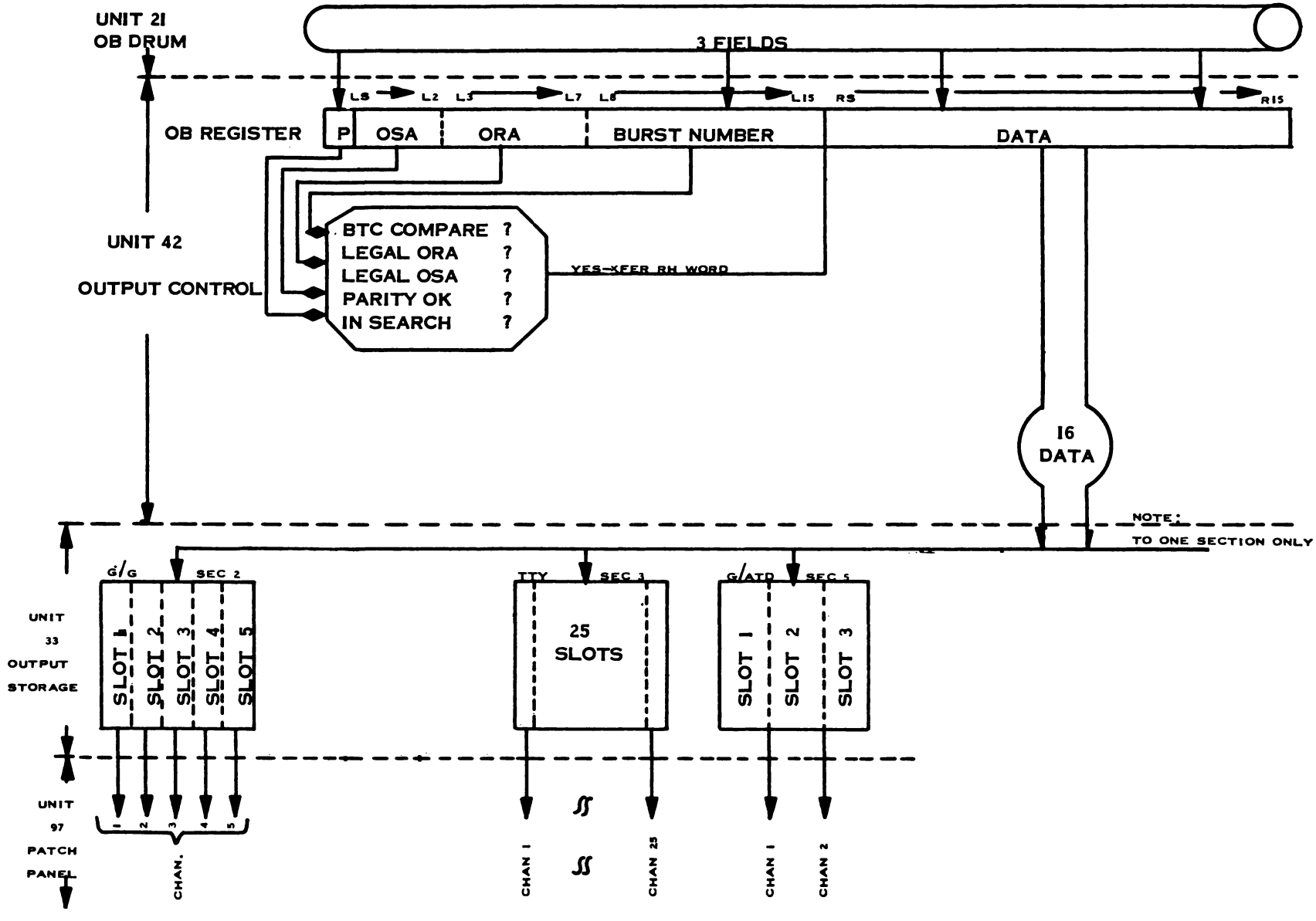

UNIT 21
OB DRUM
3 FIELDS
L8
L2
L3
L7
L6
L15
R8
R15
OB REGISTER
P
OSA
ORA
BURST NUMBER
DATA
UNIT 42
OUTPUT CONTROL
BTC COMPARE ?
LEGAL ORA ?
LEGAL OSA ?
PARITY OK ?
IN SEARCH ?
YES-XFER RH WORD
16
DATA
NOTE:
TO ONE SECTION ONLY
G/G
SEC 2
TTY
SEC 3
G/ATD
SEC 5
UNIT
33
OUTPUT
STORAGE
SLOT 1
SLOT 2
SLOT 3
SLOT 4
SLOT 5
25
SLOTS
SLOT 1
SLOT 2
SLOT 3
UNIT
97
PATCH
PANEL
1
2
3
4
5
CHAN.
CHAN 1
CHAN 25
CHAN 1
CHAN 2

Figure 1-39

is transferred in parallel with the 16 bits of the output word when the compare level is up.

When the burst number of a drum word does not compare to the contents of any of the burst counters, it is an indication that this drum word is not to be accepted at this time. Consequently, the drum word is rejected and a no-compare pulse is generated by the output control element. The no-compare pulse is sent to the Drum System, where it causes the status of the drum-word register upon which the rejected drum word is stored to remain unchanged. If the Drum System does not receive a no-compare pulse from the output control element during the 10-usec interval between drum words, it is an indication that the drum word is accepted, and the status of the drum-word register storing the accepted drum word is changed to indicate that the register is now available.

During the parity count of the drum word by the output control element, a parity bit is added to ensure that the right-half drum word contains an even number of 1 bits. This parity bit causes the total number of 1's in the 16-bit right-half drum word plus this parity bit to be even.

This parity bit is transferred to the output storage element in parallel with the right-half drum word as a G/G, or TTY parity bit, depending upon the section address in the drum word. However, in the case of the G/A-TD section, a parity bit is added to ensure that the right-half drum word contains an odd number of 1 bits. This is a prime requisite for the G/A-TD section. The G/A-TD word transfer operation is the same as that mentioned for the other sections.

The G/G, and G/A-TD data, after being processed, is transferred from the output storage element to telephone terminal equipment via relays in the output storage element. These relays do not interfere with the flow of G/G, and G/A-TD data to the telephone terminal equipment in a normal operation. During test operations, however, the flow of data is rerouted by these relays. If the Output System is under test (unit test), only one section at a time is rerouted. Therefore, test data, after being processed by the output storage element, is matched to original test data that was manually loaded into the output control element. In this manner, the accuracy of the data, after passing through the Output System, is checked. If a computer test is being made to check the flow of information, the route of the output data received from the output storage element is changed by the output test equipment. In this case, the output data is sent from the output storage element to the Input System. At the termination of the computer test, the test data is examined by the Central Computer System for errors.

The three burst counters (G/G, G/A-TD, and TTY) are contained in the output control element; their contents are always present there. Upon receipt of a select-and-read pulse from the Central Computer System, a burst-time count transfer operation (burst-count read cycle) is initiated, during which the contents of the burst counters are sequentially transferred to the Central Computer System with a 10-usec interval between burst time counts. Simultaneous with the transfer of each burst time count, a break-request pulse is sent to the Central Computer System, initiating the input-output (IO) break during which the burst time count enters the Central Computer System. When the Central Computer System has read any or all of the burst time counters as desired, it generates a disconnect pulse that is sent to the output control element. This pulse terminates the burst-time-count transfer operation.

If an alarm condition is detected during the processing of output data by the output storage element, an alarm pulse is generated by the pertinent storage section and sent to the output control element as either a G/G, G/A-TD or TTY alarm pulse. In the output control element, if an error is discovered in the drum word that is being examined, or if one of the three alarm pulses from the output storage element is received, an Output System alarm level is produced. This alarm level is sent to the maintenance console of the Central Computer System, causing the illumination of a visual alarm.

The output control element contains the complete test equipment for the Output System. This test equipment allows the Output System to be tested separately from the Central Computer during a unit loop test function. Various test operations are visually indicated on neons and lamps of the alarm portion of the Output System.

The output control element receives LOG-OD timing pulses from the Drum System; these are employed to synchronize the operations of the Drum and Output Systems. These OD timing pulses are distributed by the output control element to the various sections of the Output System. The output control element also generates and sends to the output storage element the timing pulses that are used in transferring the output data from the output storage element to the transmission equipment.

3. Output Storage Element, Block Analysis

Refer to Figure 1-40.

The purpose of each of the storage sections in the output storage element is to receive, temporarily store, and transfer messages in the proper form and at a rate comparable with the transmission facilities.

The burst number of each drum word read from the OB fields is received in the output control element and is compared to the contents of the three burst counters. If the burst number matches the contents of a burst counter, that burst counter produces a G/G-compare, TTY-compare level, or G/A-TD-compare level which is sent to the output control element.

The contents of the burst counters in the output control element are labeled G/G burst time count, G/A-TD burst time count, and TTY burst time count. In this manner, the contents of these counters are always present in the output control element and made available to the Central Computer System through a programmed IO select-and-read pulse.

Each storage section in the output storage element has its own timing circuits which enable it to record the start and end-of-search time for each burst period. Each storage section sends a search level to the output control element. When this level is up, it indicates search time for the pertinent storage section.

These levels are labeled search-G/G, search G/A-TD, and search-TTY.

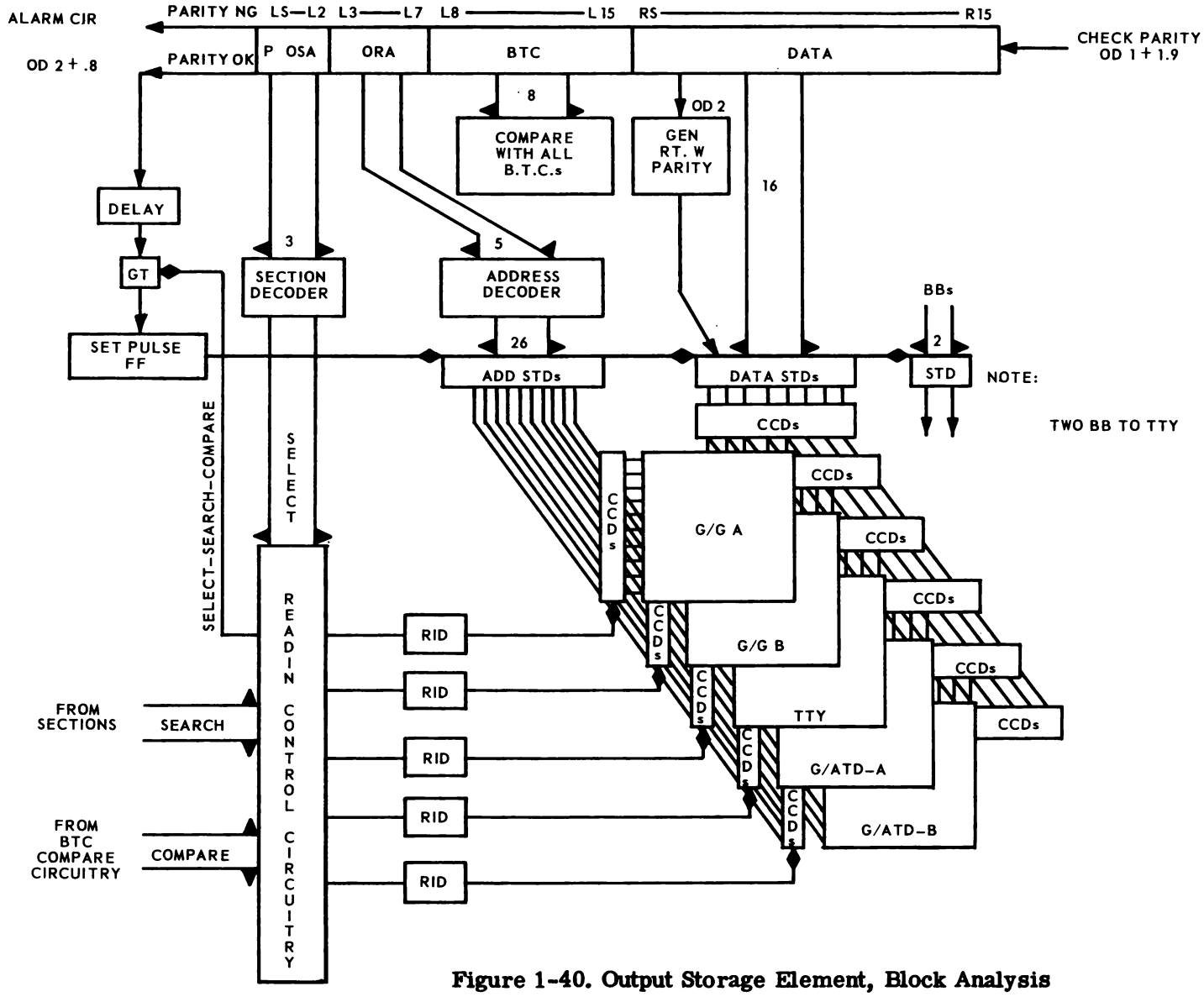


Figure 1-40. Output Storage Element, Block Analysis

During search time of each burst period, a storage section can receive the right-half drum words of the burst that is to be transmitted during the remaining portion of the burst period (referred to as the readout interval). The drum words of a particular burst are stored by the Central Computer System on the OB fields at a maximum rate of 50,000 words per second. Because of this, an output storage section receives drum words during search time at the maximum rate of 50,000 words per second. This rate corresponds to the switching rate of the ferrite cores that are employed in the core array storage devices.

The 16 bits of each right-half drum word accepted by the Output System are sent from the output control element to the correct storage section in the output storage element as specified by the section address in the left-half drum word, as half-write-message pulses. In addition, a half-write-address pulse that is indicative of the register address is also received by the pertinent storage section in parallel with the half-write-message pulses. This half-write address pulse causes the half-write-message pulses to be written into the correct register of the core array in the selected storage section.

A parity bit is also received in parallel with the half-write-address pulses and the half-write-message pulses and is written into the selected register together with the half-write-message pulses of the right-half drum word.

The contents of a register are labeled as an output word. When this word is transferred from the output storage element, the parity bit provides a means of checking it for accuracy. At the completion of search time for a storage section, the burst stored in the core array of the storage section is transferred from the storage section to transmission facilities.

Because of the type of transmission equipment employed, the form of each message in a burst must be modified before it can be transmitted. The G/G and G/A-TD messages are modified by their respective conversion circuits and then transmitted to their destinations over telephone data channels in serial form. The TTY messages are also transmitted in serial form. However, the TTY storage section simulates several TTY transmitters and sends a TTY message at the rate of 60 words per minute to a telephone TTY channel. For these reasons, the forms of the output messages are modified to a serial form and transferred to the proper transmission facilities at the proper rate. The TTY messages, likewise are transferred over telephone data channels to their destinations.

A parity check is performed when a message is transferred from a storage section. If a parity error is detected, an alarm pulse is generated by the storage section. This alarm pulse is sent as a G/G-alarm, G/A-TD alarm, or TTY-alarm pulse to the output control element. This element produces an output-alarm level that is sent to the maintenance console, causing the illumination of a neon alarm indicator. When the output control element is used to test equipment, there is an interchange of numerous pulses and levels between the test equipment and the output storage element during either a computer or unit test.

Drum timing pulses which are used to synchronize the operations of the output storage element with the operations of the Drum System are received by the output

storage element from the output control element. In addition, the timing pulses required to transfer the output messages from the output storage element at the proper rates are also received by the output storage element from the output control element.

SUMMARY QUESTIONS

1. Name the two elements that make up the Output System.

2. List 4 functions of the Output Control Element.

3. List the 6 storage sections in the Output Storage Element.

4. How many OB fields are there in a duplex system?

5. Can OB be read normally from the OD side, when being written on by the CD circuitry?

6. When a full OB register is found on the OD side, what will be written in the CD status channel? Explain.

7. Fill in the blank portions of the following program so that 100 words will be written on even registers of OB from core memory locations 5100 through 5177.

LDC	A
SDR(B)	C
WRT	D

8. Which one of the following OB status combinations is not possible:

A.	CD-1, OD-1
B.	CD-1, OD-0
C.	CD-0, OD-1
D.	CD-0, OD-0
E.	None of the above.

9. What is the duration of the "shift pulses" as used in conjunction with tape cores?

10. List two advantages of tape cores as storage devices with comparison to flip-flops.

11. Which bits of the drum word contain the burst count?

12. Which bits of the drum word indicate the section address?

13. How many slots are there in the G/A-TD storage section?

14. How many words per G/G Slot?

15. How many commands per TTY word?

16. At what OB time do we read information off the OB drum?

17. What addresses are illegal for all output sections?

18. How many words make up a G/G message?

19. Drum words are read by the output buffer register at a _____ kilocycle rate.

20. To "readout" a ferrite core in the Output System, the core is switched to a _____.

21. What parity is assigned for each word stored?

a. G/A-TD, Single Channel
b. G/G
c. TTY
d. G/A-TD, Dual Channel

22. What is the time from OD4-13 to OD2-13?

23. What is the time from OD2-91 to OD2-91?

24. There are a total of _____ burst time counters located in the output _____ element.

25. Search Time is the interval of time that information can be written into the storage section. (T/F)

26. A parity check is made when the information is transferred out of the storage section. (T/F)

CHAPTER 2: OUTPUT CONTROL ELEMENT, DETAILED ANALYSIS

1. General

The primary purpose of the output control element is to control the flow of intelligence from the output buffer (OB) fields of the drum to the output storage element and then to the transmission facilities. In addition, the output control element, upon request, sends burst count information (essential for the computer program) to the Central Computer System and performs specific tests on the Output System. The tests include both system and programmed computer tests. The output control element also provides visual indications of any Output System alarm conditions.

Several terms, used frequently in the output control element, are explained as follows:

a. Drum Word. This is a 33-bit word entered into the output control element from the OB drum fields of the Drum System. It contains the intelligence destined for transmission, the data which identifies the storage location, and the transmission sequence of the word.

b. Output Word. This is the intelligence portion of the drum word (right half) and is the portion sent to the output storage element from the output control element.

c. Burst. A burst is the group of words consisting of the messages which are simultaneously transferred from a storage section to the associated telephone lines during the complete emptying of the storage section.

d. Burst Period. The burst period is the interval between the entrance of successive bursts into the Output System. The burst period consists of search time and readout time. Search time (read-in-time) is the time required to read the burst from the OB drum field into one of the output storage sections. Readout (nonsearch) time is the time required to empty the burst out of the output storage section and into the telephone lines, plus any pauses or delays. The bursts are counted in each output storage section so that information is always available as to which burst period is in progress.

e. Burst Number. The burst number is part of the 33-bit drum word and designates the particular burst period during which the word is to be entered into the output storage section.

f. Elapsed Time. The elapsed time is the time that has elapsed since the start of a burst period.

2. Element Diagram Analysis

The output control element is divided into four major sections as shown in Figure 2-1. They are the output buffer, output computer, output alarm, and output test equipment sections. Note: Refer to Figure 2-1.

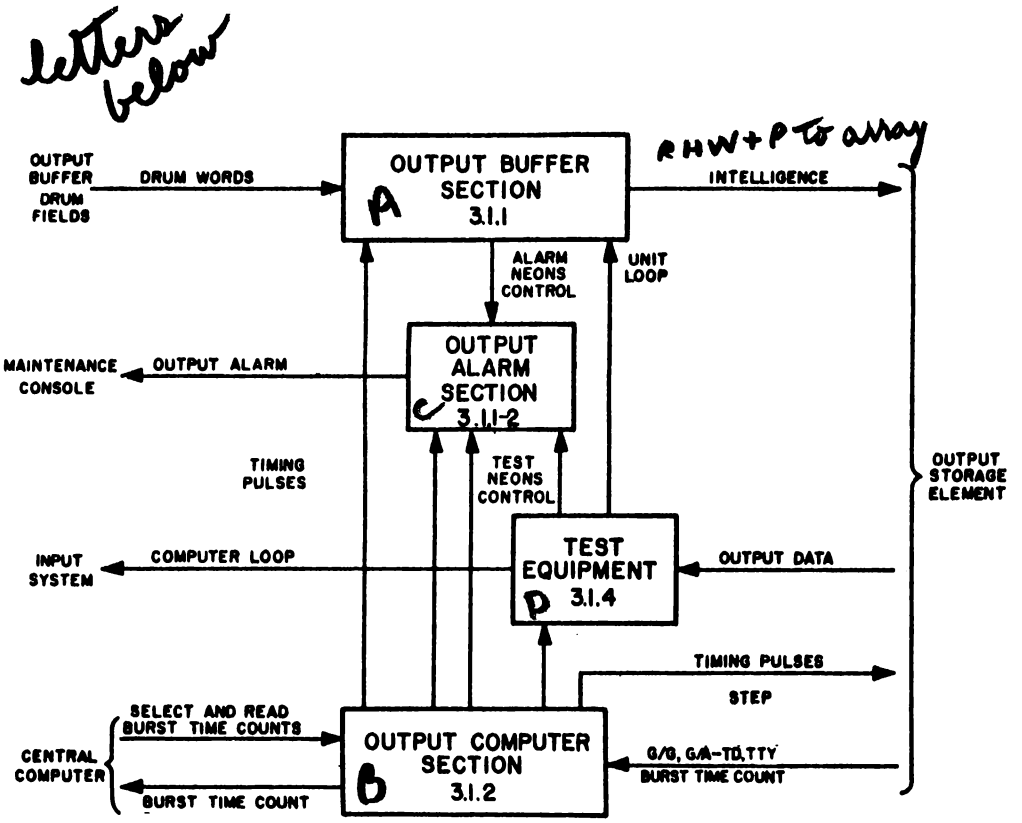


Figure 2-1. Output Control Element, Block Diagram

a. The OB drum section receives a drum word from the LOG drum OB fields in parallel form, tests the parity of the word, examines its addresses and burst number, and checks the validity of the word. On the basis of the word addresses, this section determines to which storage section and core array register within this storage section the right-half drum word (intelligence portion of the word) should be sent. It also generates an output parity bit for the right-half drum word. If the right-half drum word is valid, it is sent to the selected section and register in the output storage element.

b. The output computer section transfers the burst counts of the G/G, G/A-TD, and TTY burst counters to the Central Computer System at the latter's request. Upon receipt of a select-and-read pulse, the output computer section releases this information to the Central Computer System. The Central Computer System utilizes the information to assign the proper burst numbers to future output messages. In addition to this function, the output computer section generates some, and distributes all, timing pulses used for controlling operations in the Output System.

c. The output alarm section stores information regarding the status of several alarms and displays the status of these alarms by neon indicators. It also displays the drum word bits and certain test operations on neon indicators and indicator lamps. These indicators are located on the maintenance consoles and output unit test panels.

d. The output test section, which is an integral part of the output control element, is used to perform programmed computer and unit tests within the Combat Direction Central.

Two types of loop tests are provided for the Output System: the unit loop test and the computer loop test. Each test involves the feedback of test information to its origin for the purpose of checking whether this information was correctly transmitted. The Output System test equipment effects the modification of information paths to form the test information on path required for the test undertaken; i.e., unit test or computer test.

A description of the logical operations performed by the four sections comprising the output control element is included in the following text. The block schematic diagrams used have been simplified by the exclusion of nonlogical circuits such as cathode followers and amplifiers. For the complete circuitry of a logical circuit, refer to the Engineering Data Book. The logical reference number of each of these drawings has been included in the caption of each of the corresponding simplified diagrams in this manual.

Detailed Analysis of the Output Buffer Section

1. Operations Performed

The output buffer section of the output control element performs the following basic related operations:

a. Enters the complete drum word from the OB fields of the LOG drum into the OB register flip-flops.

b. Checks the parity of the drum word in the OB register flip-flops.

c. Decodes the output section and register address in the output word.

d. Checks the legality (correctness) of the output section and register addresses.

e. Generates a parity bit for the output word if needed.

f. Controls the read-in of the output word into the proper section and register address in the output storage element.

These basic operations are discussed in relation to the over-all action performed by the output buffer section in processing and accepting or rejecting the word.

Note: Refer to Figure 2-2 and Figure 2-3.

2. Drum Word Entry

a. Flip-Flop Register

Each drum word is temporarily stored in a flip-flop register which is divided into the right-half drum word, burst number, register address, section address, and parity registers. The drum word consists of 33 binary digits grouped as shown in Figure 2-3. The right drum word, consisting of bits R5 to R15, inclusive, represents the intelligence intended for transmission as the output word. The left drum word (bits

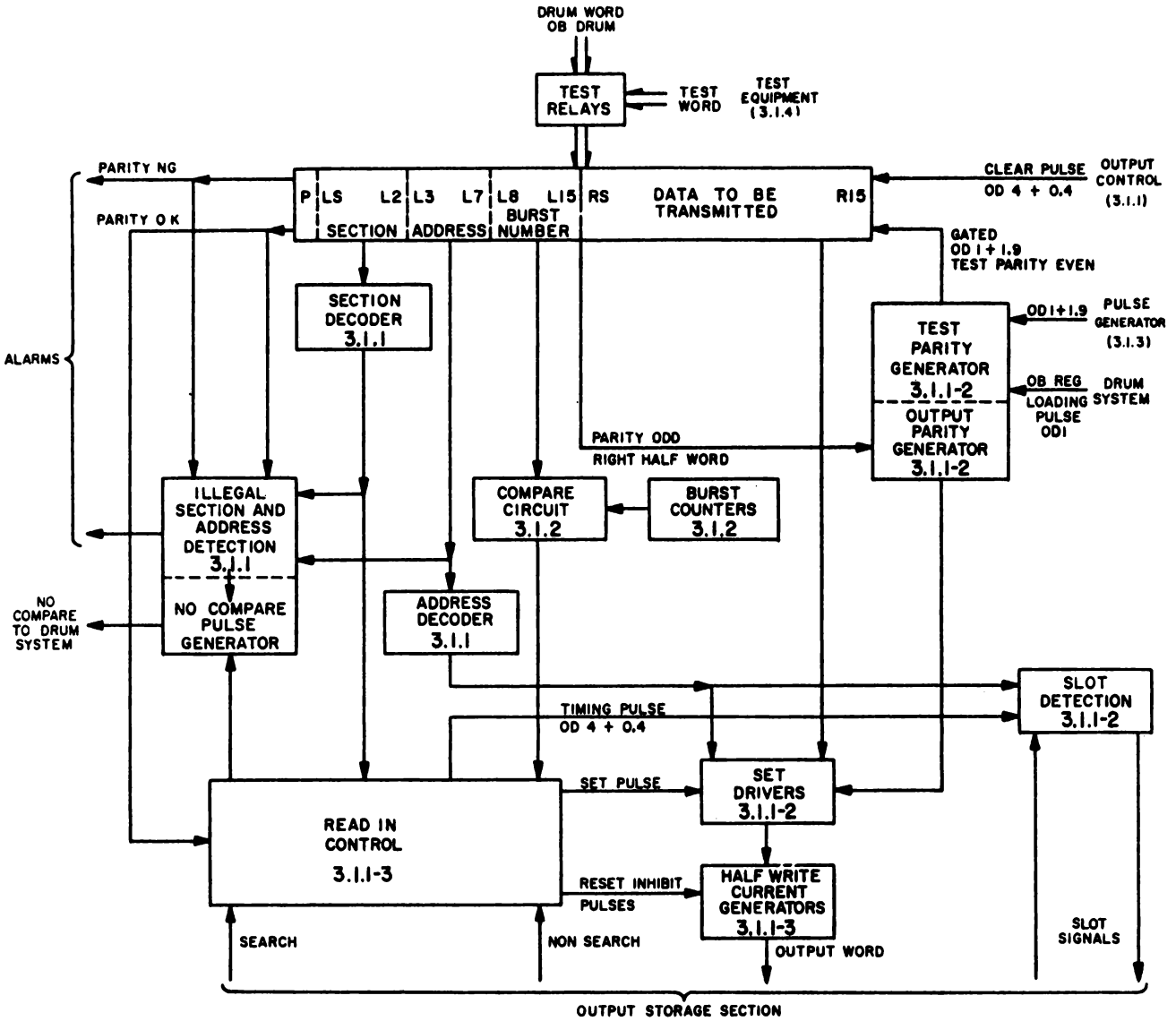


Figure 2-2. Output Buffer Section (3.1.1), Block Diagram

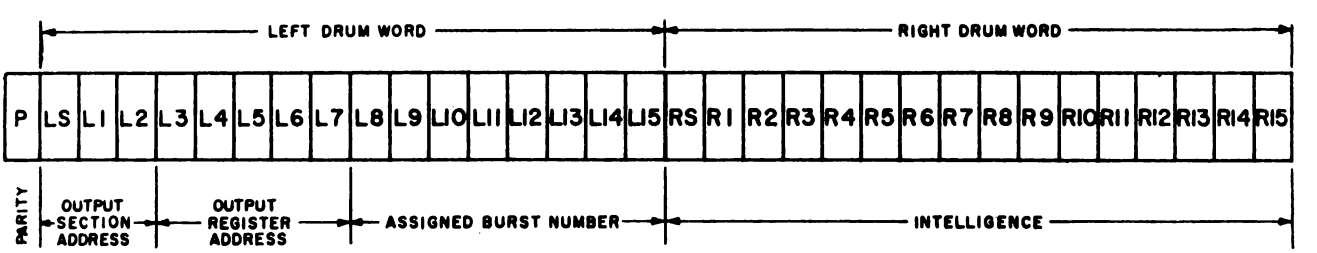


Figure 2-3. Drum Word Structure

LS to L15, inclusive) consists of the output section address, the output register address, and the burst number. The addresses denote the output storage section and register to which a right-half drum word is assigned; the burst number determines the time and sequence of transmission of the associated right-half drum word. The remaining drum word is a parity bit.

b. Right-Half Drum Word Register

The right-half drum word register consists of 16 flip-flops, as shown in Figure 2-4. A right-half drum word is applied to the register flip-flops in the form of parallel standard pulses from the OB fields. A 1 bit is represented by the presence of a pulse and a 0 bit by the absence of a pulse. The right-half drum word register is cleared prior to the receipt of each drum word; thus, when a right half-word is applied, it is reproduced at the flip-flop outputs as d-c levels. The flip-flops are cleared approximately 7.9 usec after receipt of a right-half drum word in preparation for the next word. The time interval between the registering and the clearing of the drum word is chosen to be approximately 7.9 usec because approximately 10 usec are required for each drum register of the OB field to pass the drum read head. Hence, since a new drum word may be passed from the OB field to the Output System flip-flop register every 10 usec (time OD1), the flip-flop register must be cleared after a time interval of slightly less than 10 usec.

During the time that the right-half drum word is in its register, its bits are applied to the STD's of the read-in circuit, the parity gates, and the output test equipment section (Figure 2-2). The STD's initiate preparations for the transfer of a word into one of the storage sections, should it be accepted. The parity gates, which are in the same location as the right-half word register, permit a sampling of the right-half drum word when checking the parity of the complete drum word. The gates utilize both the 0 and 1 flip-flop outputs. The STD's require only the 1 outputs to perform their functions.

c. Burst Number Register

The burst number register temporarily stores bits L8 to L15 of the drum word. The assigned burst number can have a maximum of eight binary digits, and therefore 256 possible variations. The number of possible variations (different possible burst numbers) must be large enough to ensure that all bursts within a program frame can be assigned a different burst number.

The burst number register, shown in Figure 2-5, contains eight flip-flops designated L8 to L15. Bits L8 and L15 are inserted in the register at the same time that the other bits of the drum word are placed in their respective registers. As in the case of the right-half drum word register, the burst number flip-flops are cleared approximately 7.9 usec later. During this interval, both the 1 and 0 outputs are made available to the parity gates, which are in the same location as the burst number register, and to the burst counter compare circuits. This permits the parity check and burst number comparison operations to be conducted. The burst number comparison operation consists of comparing the burst number of the drum word with the contents of the burst time counter in the output control element. Therefore, the contents of the counter indicate the burst number of the drum word which should be stored next. If the drum

word which has been entered does not have the right burst number, but if all other information in the word is found to be correct, the word is rejected from the Output System but is not erased from the OB field of the drum. It is therefore available to be reentered at the correct time. A no-compare pulse is generated to accomplish this operation.

d. Section Address Register

Binary digits LS to L2 of the drum word constitute a binary coded message that designates the section address. This address denotes the specific output storage section in which the associated right-half drum word is to be stored. At present, there are only three output storage sections (G/G, G/A-TD, and TTY). Since three binary digits can make up eight possible combinations, there are eight possible addresses. It follows that since only three addresses are assigned, an error exists if one of the other five addresses is called for by the coded message. The illegal section address detection circuit determines whether the section address is in error.

A simplified logic diagram of the section address register is shown in Figure 2-6. The outputs of these three flip-flops are routed to the parity gates which are in the same location as the register, and also to the section address decoder. The latter decodes the information contained in bits LS through L2 to produce a signal level on one of the three section address lines. This action produces control which directs the right-half drum word to the assigned storage section. The illegal section detection circuit produces an illegal-section-address pulse if the decoded section address indicates one of the five unassigned section addresses. This pulse is used in the alarm circuit. Also, an illegal section level is generated which is used in the no-compare pulse generator circuit to cause a drum word which has an illegal section address, and is therefore rejected from the Output System, to be erased from the drum.

As in the case of the other flip-flop registers, the clear pulse is applied to the section address register approximately 7.9 usec after entrance of the bits. This clears the register.

e. "Register Address" Register

Binary digits (bits) L3 to L7 of the drum word constitute a binary coded message which designates the register address. This address denotes the specific register within a storage section in which the associated right-half drum word is to be stored. At present the G/G and TTY storage sections use 25 storage registers; and the G/A-TD storage section, 12 registers. A 5-bit code is used which furnishes 32 distinct addresses. Therefore, there are seven unassigned register addresses each for G/G and TTY, and 20 unassigned for G/A-TD. It follows that if the 5-bit register address designates an unassigned storage address for the storage section designated by bits LS to L2, the register address is in error (illegal). This error is detected by the illegal register address detection circuit. This circuit produces an illegal register-address pulse if the register address is illegal. This pulse is used in the output alarm circuit and is also used in the same manner as the illegal-section-address pulse. The illegal register address detection circuit uses only the signal levels from the 1 side of the flip-flops.

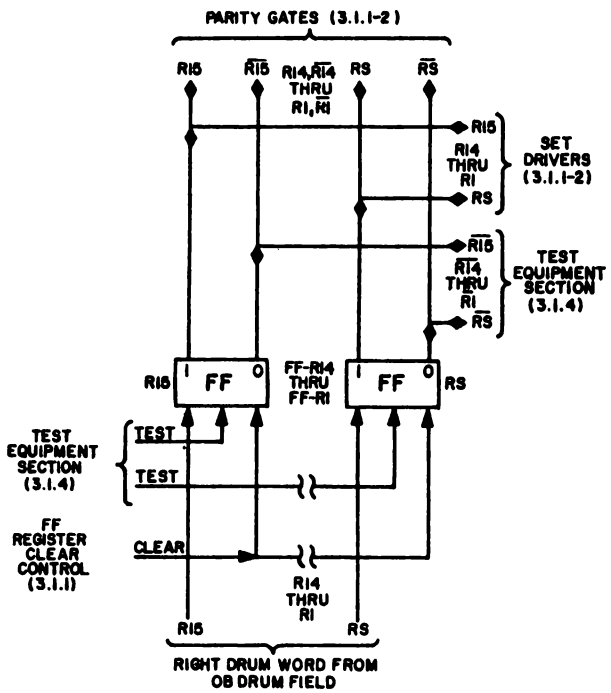


Figure 2-4. Right Drum Word Register (3.1.1-2), Simplified Logic Diagram

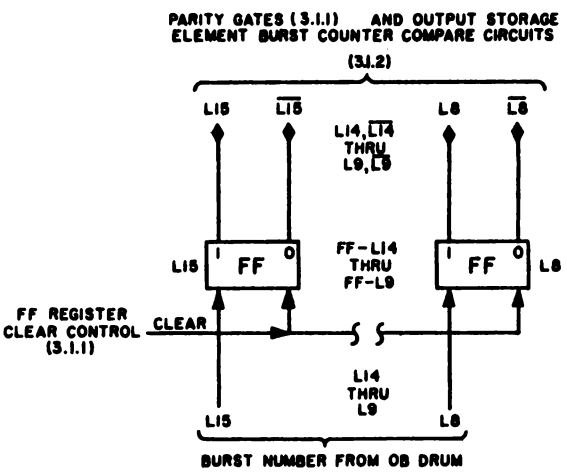


Figure 2-5. Burst Number Register (3.1.1), Simplified Logic Diagram

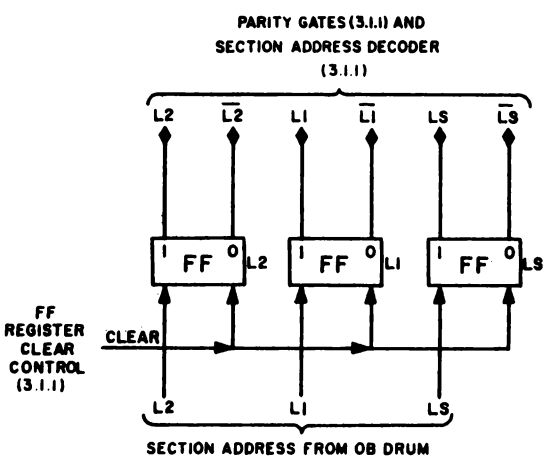


Figure 2-6. Section Address Register (3.1.1), Simplified Logic Diagram

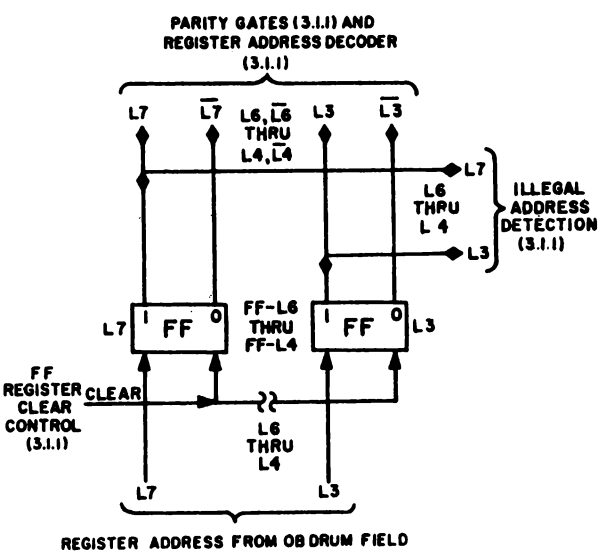


Figure 2-7. Register Address Register (3.1.1), Simplified Logic Diagram

A simplified logic diagram of the address register is shown in Figure 2-7. The outputs of these five flip-flops are routed to the address decoder, to the illegal address detector, and to the parity gates. The parity gates are in the same location as the address registers. The registers address decoder decodes the message contained in bits L3 to L7 to produce a signal level on one of the register address lines; there is one line for each register address. This signal level is passed to the STD's (Figure 2-2) and produces control which directs the right-half drum word to the assigned register in the assigned storage section.

As in the case of the other registers, the clear pulse clears the flip-flops approximately 7.9 usec after the bits are entered.

f. Parity Register

The 33rd binary digit, designated P, is inserted in the drum word at the Central Computer System for parity checking purposes. The parity bit is therefore transmitted from the parity register to the parity gates to be counted with the other drum word bits. The parity register is merely a one flip-flop circuit (Figure 2-8). The parity register and gates are in the same location. For a detailed discussion of the parity checking operation, refer to paragraph 4, page 70.

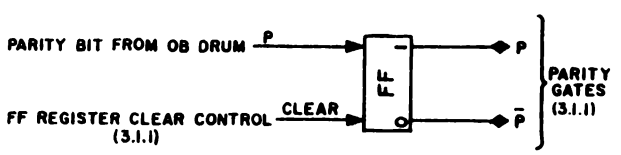


Figure 2-8. Parity Register (3.1.1), Simplified Logic Diagram

g. Flip-Flop Register Clearing

The temporary storage period of the OB register is controlled by the flip-flop clear (reset) pulse. This pulse is generated by the drivers section of the parity register and drivers circuit. The controlling factors for the application of the clear pulse are shown in Figure 2-9. The clear pulse is a gated OD 4 + 0.4 usec timing pulse that is sent out on separate lines to clear various flip-flops and flip-flop registers as indicated in the figure.

Since the OB register receives the drum word at OD 1 time, the normal storage time of the OB register can be established at 7.9 usec (OD 1 to OD 4 + 0.4). Referring to Figure 2-9, it can be seen that the application of the clear pulse is dependent upon GT 1 and GT 2 being conditioned. The conditioning level that is applied to GT 1 is a not-error level (+10v) which is always present at this gate in normal operation. However, this level is brought down when an error in a word transfer operation occurs during a computer loop test operation. Gate tube 2 is normally conditioned by a +10v level which is applied through the normally closed contact points of de-energized relay K2.

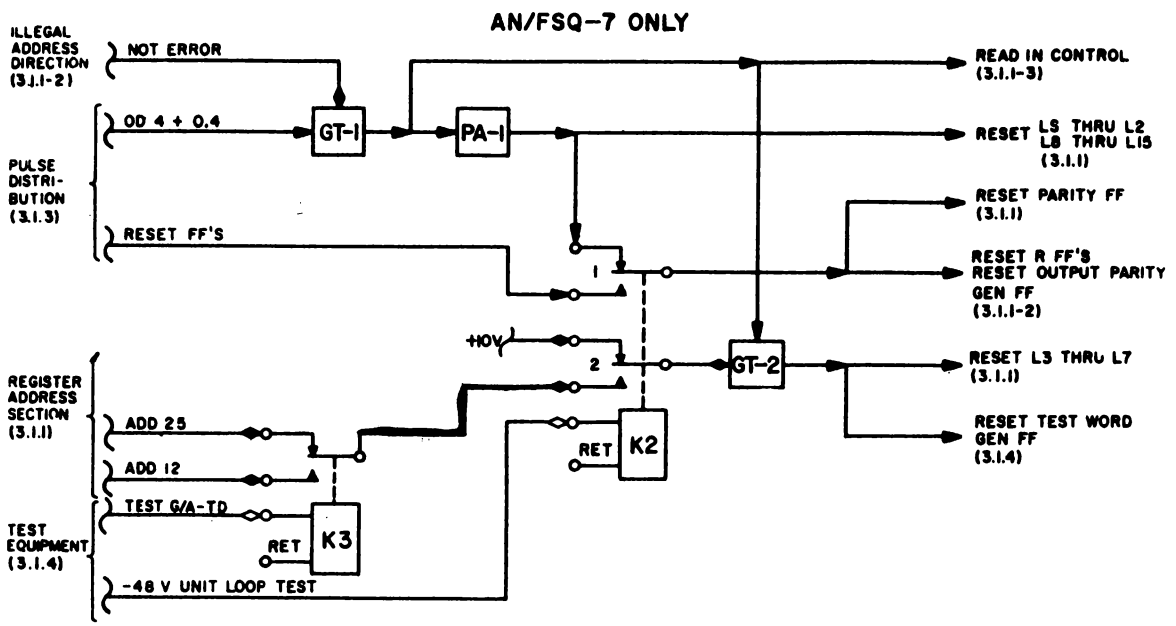


Figure 2-9. Flip-Flop Register Clear Control (3.1.1), Simplified Logic Diagram

PARITY	SECTION ADDRESS	REGISTER ADDRESS	BTC	IN SEARCH	WORD DISPOSITION	BITS PUT IN STATUS CHANNEL
OK	OK	OK	OK	Yes	Accepted	0
OK	OK	OK	OK	No	Lost	0
Bad	OK	OK	OK	Yes	Lost	0
Bad	OK	OK	OK	No	Lost	0
OK	Illegal	OK	OK	Yes	Lost	0
OK	Illegal	OK	OK	No	Lost	0
OK	OK	Illegal	OK	Yes	Lost	0
OK	OK	Illegal	OK	No	Lost	0
OK	OK	OK	Bad	Yes	Saved	1
OK	OK	OK	Bad	No	Saved	1

Table 2-1. Conditions for Acceptance or Rejection of a Drum Word

This relay is energized only during a unit loop test. Therefore, during normal operation, all of the OB register flip-flops will be cleared 7.9 usec after receipt of a drum word.

When the Output System is placed in the unit loop test, K2 will be energized, preventing the right OB register flip-flops from being cleared except by manual operation. During a unit loop test, the right half-word is processed through a particular storage section, through the test circuitry, and then returned to complement the right OB register flip-flops. Each flip-flop containing a 1 will be complemented to its 0 side. Thus, by preventing the normal clearing of the right OB register flip-flops and by using neons, a visual indication of how correctly the test word was processed can be obtained.

Whenever K2 is energized, the conditioning level that is applied to GT 2 is dependent upon the output levels generated in the address decoder. In a unit loop test operation, the address portion of the OB register (L3-L7) is stepped once for each test word that is read into the storage array until all of the legal register addresses are made to contain the test word. When this occurs, and depending upon the section that is under test, an add-12 (G/A-TD) or add-25 (G/G and TTY), level will be applied to condition GT 2. Conditioned GT 2 will then pass an OD 4 + 0.4 pulse to end the test word read-in operation.

To summarize, the registers are always cleared 7.9 usec after a word is entered into the registers during normal operations. Only during test operations is it possible for the drum word to remain in the registers longer than this period.

The OD 4 + 0.4 reset pulse shown in Figure 2-9 is gated in the read-in control circuit when a word is missed. It then becomes a nonsearch signal to the output alarm section and the Central Computer. The OD 4 + 0.4 pulse is used since it occurs at a time sufficiently later than the time of entrance of the word (OD 1) to permit complete examination of the word.

3. Checking Drum Word for Acceptance

a. Acceptance Requirements

In order for the right-half drum word to be read out of the output control element into the output storage element, the complete drum word must meet all of the following requirements:

(1) Correct parity

(2) Correct section and register address

(3) Correct timing (section must be in search)

(4) Favorable comparison between the burst number and the contents of the burst counter

If a drum word has either incorrect parity, an illegal section address or register address, or incorrect timing it is not accepted by the Output System and is

erased from the OB field. If all conditions for acceptance are correct except the burst number, the word is rejected temporarily by the Output System. This word is preserved for use at a later time because its correct parity and correct address have caused the generation of a no-compare pulse. If the burst number does not compare with the contents of the burst counter, and the particular burst period in progress is in the readout operation (nonsearch time), a no-compare pulse is still generated even though the timing is apparently wrong. This is so because, although readout is taking place, the lack of comparison indicates that the word is not assigned to this particular burst period. Therefore, the word has not been missed and is still good. It should therefore be stored until a later time, so a no-compare pulse is generated. On the other hand, if the burst number compares with the contents of the burst counter, and readout is taking place (incorrect timing), there has been a programming error, as previously described. The word cannot be entered into the Output System and must be erased from the OB field of the drum. A no-compare pulse is not generated.

When all four of the conditions listed above are satisfactorily met, the output word (right-half word) is transferred to the storage section and register indicated by the respective addresses.

b. Acceptance Checks Made in Output Buffer Section

A summary of the conditions for acceptance or rejection of a drum word by the Output System is found in Table 2-1.

The output drum section performs the checks to determine whether the parity is correct and whether the section and register addresses are legal. The burst number comparison is made in the output control element. The timing check is made in the output storage element. The results of all four checks are passed to the read-in control (Figure 2-2) of the output buffer section. This circuit then examines the results of the checks and proceeds to accomplish one of the following functions:

(1) Operates the set drivers (STD's) to read the right-half drum word into the output storage section if all checks are correct.

(2) Generates a no-compare pulse and rejects the drum word if only the burst number fails to check.

(3) Rejects the drum word and does not generate a no-compare pulse if the parity or either of the addresses is not correct.

4. Parity Checking

a. Type of Parity Check

One of the conditions imposed on a drum word before acceptance by the Output System is correct parity. An odd parity check is employed and each drum word received should have an odd number of 1's. The parity check functions in the following manner. The drum word (less the parity bit) is examined at the Central Computer System to determine whether the total number of 1's is odd or even. If the number of 1's is odd, a 0 parity bit is registered; the total number of 1's in the 33-bit drum word

thus remains odd. Should the total number of 1's be even (before insertion of the parity bit), a 1 parity is registered, and the 33-bit drum word now contains an odd number of 1's. Therefore, any drum word received by the Output System should contain an odd number of 1's.

The presence of an even number of 1's in the drum word indicates that a 1 was either lost or gained during the time of transit between the Central Computer System memory buffer register and the Output System. Should such a situation arise, steps are taken to prevent the further transmission of the incorrect word. Also, an alarm signal is generated. (Note that the parity check would not fail if the word were to gain or lose two 1's; the total number of 1's would then be odd and the word would appear to be correct. However, the probability of such an occurrence is slight, and the described parity check method is considered to be sufficiently accurate.)

A parity check is also performed on the transmitted output word at the equipment receiving the message. This requires the addition of a parity bit to the output word. The output word parity is not to be confused with the drum word parity described above. More detailed information concerning output word parity is given in paragraph d.

A discussion of the generation of the drum-word test-parity pulse, the method of determining the parity status of a drum word, and the generation of the output word parity is given below.

b. Drum Word Test Parity Generator

The parity check operation is initiated by applying a test-parity-even pulse to the right-half drum word register parity gates. This pulse is produced and controlled by the drum word test parity generator (Figures 2-2 and 2-10). The parity gates operated by all the flip-flop registers are connected serially, and the application of the test-parity pulse at the beginning of the series connection produces a check of whether the complete drum word, including the parity bit, has odd parity.

The test parity flip-flop is set by the flip-flop register-loading pulse at OD 1 time. This pulse is received by the output control element from the OB drum signal simultaneously with each drum word. The flip-flop output level, after passing through an AND circuit, conditions GT 2 which passes an OD 1 + 1.9 usec pulse as the test-parity-even pulse. A sampling of the parity gates then follows to determine drum word parity. At the completion of the parity check, a parity-OK or parity-NG pulse will be generated at approximately OD 2 + 0.8 usec to clear the flip-flop, deconditioning GT's 1 and 2. The timing is such that GT 1 will not be conditioned at OD 3 time if a parity check of the drum word has been completed. Should the test-parity pulse not be generated, or if it does not get through all of the parity gates, GT 1 will be conditioned to pass the OD 3 pulse which will cause the generation of a lost parity alarm.

In order for the conditioning level of the two gates to be up, coincidence is required between the flip-flop output and the single-shot multivibrator output. The single-shot multivibrator used here has a normally positive output. Thus, when it is pulsed by the restart signal from the test equipment, the single-shot multivibrator produces a negative output level of 100-ms duration before reverting to its normal

positive level. This inhibits the passage of test-parity pulses and causes the OB drum to be cleared.

During an Output System test operation, the flow of drum words from the OB fields to the output control element is temporarily halted by the inhibiting action of a stop pulse manually generated in the output test equipment section and sent to the read circuits of the OB fields. Therefore, during a test operation, output data which should be transmitted at the time the test operation is in progress accumulates on the OB fields. At the completion of a test operation, a restart pulse is manually generated in the output test section and sent to the OB field read circuits where it restarts the flow of drum words to the output control element. The restart pulse is also sent to the drum word test parity generator, shown in Figure 2-10, where it triggers the single-shot multivibrator. The drum words received by the output control element following a test operation are those that should have been transmitted during the test operation. Thus, these drum words contain old data and will be destroyed.

Destruction of these drum words is accomplished in the output control element by accepting all drum words from the OB fields and not transferring them to the output storage element during the 100 ms following the generation of the restart pulse. This is the purpose of the single-shot multivibrator in the drum word test parity generator. Since its output is produced by the restart pulse, the test parity signals are not generated during the 100 ms interval following receipt of the restart pulse. Because no parity check is performed on the drum words received during this time, the drum words are accepted by the output control element from the OB fields but are not transferred to the output storage element. Consequently, during the 100-ms interval, successive drum words are loaded into the flip-flop register and approximately 7.9 usec after each drum word is placed in the flip-flop register, the flip-flop register is cleared. Since these words are accepted from the OB fields, the status of the drum registers in which they were stored on the OB fields is changed to indicate that the registers contain old information. Thus, successive clearance of the flip-flop register destroys the drum words. Approximately 65 ms are required to read the three OB fields; therefore, at the completion of the 100 ms following a test operation, all old output data has been destroyed.

As shown in Figure 2-10, the flip-flop may also be set by a selected read-in-test-word pulse from the test equipment. This is also a test equipment function and is used to generate a test-parity signal while the equipment is under test, since information flow from the OB fields, including the OB-register-loading pulse, is cut off during test.

c. Drum Word Parity Gates

The drum word received from the OB drum is subjected to a parity test to determine whether it contains an odd or even number of 1's. It has been shown that a correct incoming word must be of odd parity. An even parity indicates the presence of an error. Both the 1 and 0 outputs of the register flip-flops serve as conditioning signals for the parity gates (Figure 2-11). A test parity pulse then successively samples the parity gates associated with the 33 drum word bits. The result is either a parity-OK signal, indicating odd parity, or a parity-NG signal, indicating even parity.

The test-parity pulse is simultaneously applied to GT's 1 and 2 (which are in the right-half drum word register at OD 1 + 1.9 usec). Assume that flip-flop R15

of the right drum word register is set in the 1 state. Gate 1 is conditioned to pass the test-parity pulse and passes a pulse which is then designated odd. Gate 2 does not pass the test-parity pulse because the conditioning of GT 1 resulted from the register R15 being in the 1 state. The portion of the drum word thus far scanned contains an odd number of 1's. Therefore, the output of GT 1 is designated as odd. Carrying this procedure to the following stage, the odd pulse then simultaneously samples GT's 4 and 5. Assume that level R14 is down (bit R14 of the drum is a 0); GT 5 as expected, passes an odd signal to the next stage.

Consider the case where bits R14 and R15 are 1's. The scanning of the two respective stages should then indicate an even parity. The odd pulse from GT 1 samples GT's 4 and 5, but only GT 4 is conditioned to pass the signal which is appropriately labeled "even."

The scanning continues in similar fashion through the remaining gates associated with all the drum word bits. The result, at the output of the parity gates, is either the parity-OK or the parity-NG pulse, indicating odd or even parity, respectively. The parity-OK pulse, if generated, goes to the read-in control of the read-in section (Figures 2-2 and 2-11). Briefly, a parity-OK pulse is necessary for the right half drum word to be transferred to the output storage section. The parity-NG pulse, if generated, goes to the output alarm section to set an alarm indicating an error in the parity of the input drum word.

Either the parity-OK or parity-NG pulse, depending upon which is generated, goes to the illegal address detection section. Briefly, the pulse that is present is used as a pulse source for the generation of the illegal-register-address pulse and the illegal section-address pulse, if either of the addresses is illegal. Also, the parity-OK pulse is used in the generation of the no-compare pulse. The no-compare pulse is generated when the burst number is wrong but the address, parity, and search timing are correct. The reason that parity-OK or -NG pulses are used in the illegal address detection circuits is to cause these checks to be made after the parity check but to be independent of the results. In addition, the parity-OK or parity-NG pulses are used to clear the test parity generator flip-flop for the reasons explained in paragraph b.

d. Output Word Parity Generator

Since the drum word does not remain intact beyond the output control element, the drum word parity bit cannot be used as the storage word parity bit. Therefore, a new parity bit is generated for each right-half drum word as it is read into the storage array and is transmitted with it on the telephone lines. This permits one parity check to be made as the message leaves the Output System and another at the receiving equipment. Thus, possible errors incurred during the processing of the word through the storage element or through the telephone equipment may be detected.

The following paragraph describes the operation of the output parity generator circuit for all sections except G/A-TD.

In normal operation, relay K1 is de-energized (Figure 2-12); also the flip-flop is cleard 7.9 usec after each word is read into the OB register. The parity checking pulse (OD 1 + 1.9) emanates from the last parity gate of the right half

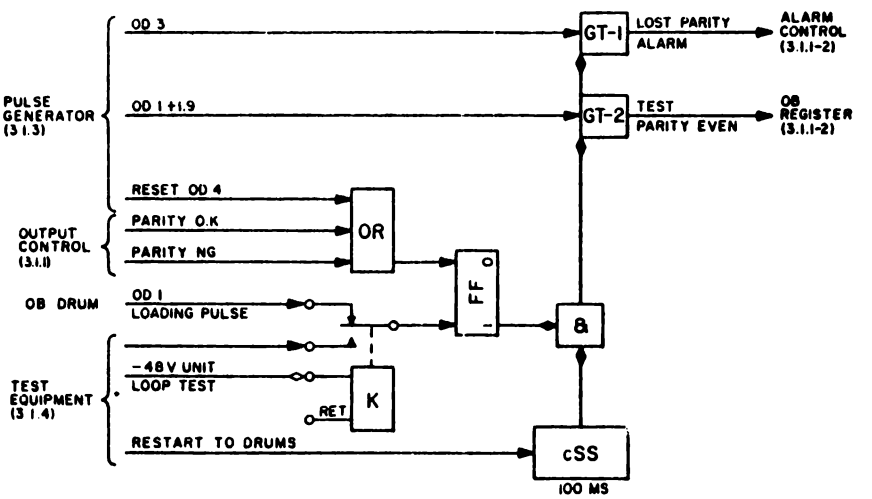


Figure 2-10. Drum Word Test Parity Generator (3.1.1-2), Simplified Logic Diagram

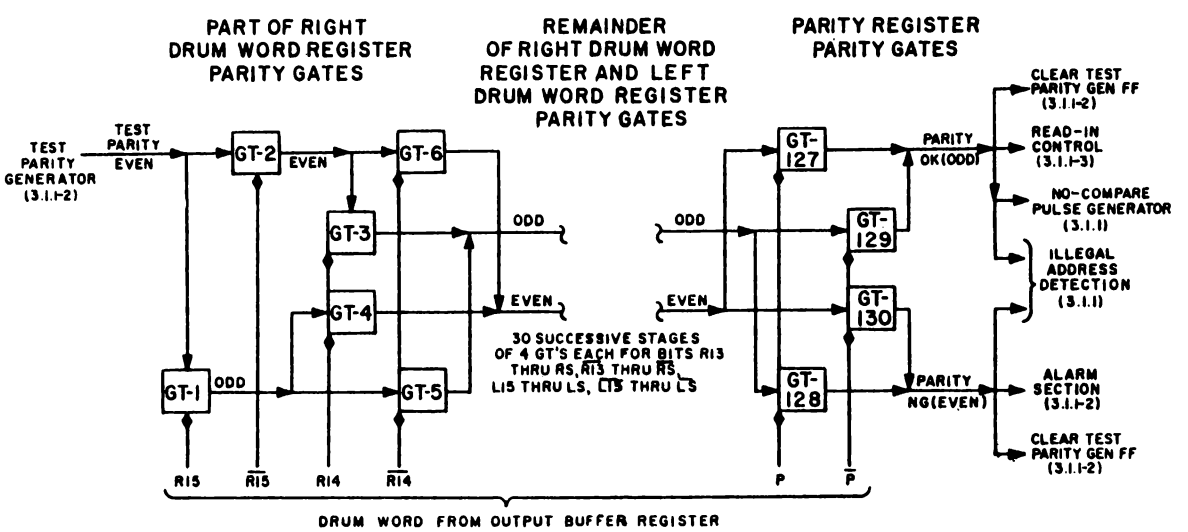


Figure 2-11. Drum Word Parity Gates (3.1.1, 3.1.1-2), Simplified Logic Diagram

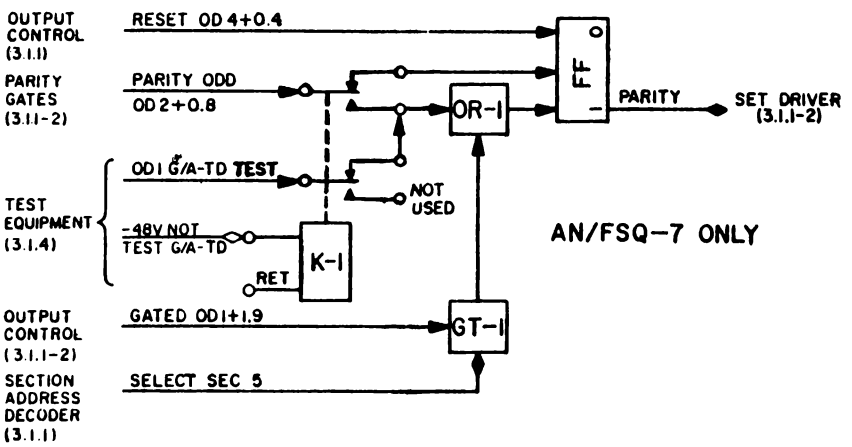


Figure 2-12. Output Parity Generator (3.1.1-2), Simplified Logic Diagram

drum word (RS) as either a parity-odd or parity-even pulse to strobe the gate. This pulse occurs at approximately OD 2 time. If parity of the right-half drum word is even, the flip-flop remains clear; thus, the storage parity bit will be a 0 maintaining an even number of 1 bits in the storage array. On the other hand, if the parity-checking pulse appears on the odd line, the flip-flop will be complemented to its set side. Then the parity bit added to the right-half word will be a 1, making the total number of 1 bits even. It can be seen that for all sections except G/A-TD, storage parity will be even.

The storage parity of a G/A-TD word is odd; therefore, additional circuitry is required to utilize the output parity generator flip-flop in a manner similar to that of the other sections. When a G/A-TD word is read into the OB register, a select-section-5 level will be generated to condition the gate. This gate will then pass the OD 1 + 1.9 parity-checking pulse which strobes it to set the flip-flop. Assuming that the right half-word has odd parity, a parity-odd pulse (OD 2) will be produced to complement the flip-flop to its clear side. Thus, odd parity of the right half-word is maintained. The relay will be energized only when unit loop testing any section other than G/A-TD. During unit loop test, the operation of the parity generator circuit is, by necessity, slightly different; however, even storage word parity for all sections other than G/A-TD (which has odd parity) will be maintained. Since the AN/FSQ-8 uses only a G/G and a TTY storage section, the operation of the output parity generator circuit differs somewhat from the previous description.

5. Decoding

a. Need for Decoding

Previously, it was mentioned that each right-half drum word has associated with it a storage section address and a storage register address. The addresses are in binary coded form and must be decoded before a word can be routed to its proper destination. Further, each word falls into a particular slot. A slot is a group of registers

within a storage array that feed one telephone channel. Therefore, the contents of a given slot are words of one message having a common destination. The method of slot detection and the coding of the section address and register address are explained below.

b. Section Address Decoder

The input signals to the section address decoder consist of the three address bits from the section address register flip-flops. There are eight possible variations of section decoder inputs in binary code whose equivalents correspond to decimal digits 0 through 7. Each of the eight combinations of three d-c levels is fed to a separate AND circuit. When all three inputs to one of the AND circuits are simultaneously positive, a select-section level is fed to the read-in control circuit. Select sections 2, 3, and 5 represent the G/G, TTY and G/A-TD sections, respectively. Numbers 0, 1, 4, 6, and 7 are presently unassigned since present plans call for only three output sections. Therefore, a binary code corresponding to these numbers (illegal sections) constitutes an error in the section address. If a select-section-0, 1, 4, 6, or a select-section-7 level is produced, it is sent to the illegal section circuit and thence to the alarm control circuit, whereupon an illegal section alarm is generated. The possible binary codes and their respective section assignments are shown in Table 2-2.

The AN/FSQ-8 section address decoder is basically the same as that described above except that only two section addresses, G/G and TTY (010, 011, respectively), are legal. Therefore, the other section address numbers 0, 1, and 4 through 7 will be decoded as illegal sections.

BINARY CODE (INPUT)			SELECT	SECTION ASSIGNMENT
LS	L1	L2	SECTION	(OUTPUT)
0	0	0	0	Illegal section
0	0	1	1	Illegal section
0	1	0	2	Ground-to-Ground
0	1	1	3	Teletype
1	0	0	4	Illegal section
1	0	1	5	Ground-to-air TD
1	1	0	6	Illegal section
1	1	1	7	Illegal section

Table 2-2. Section Address Assignment

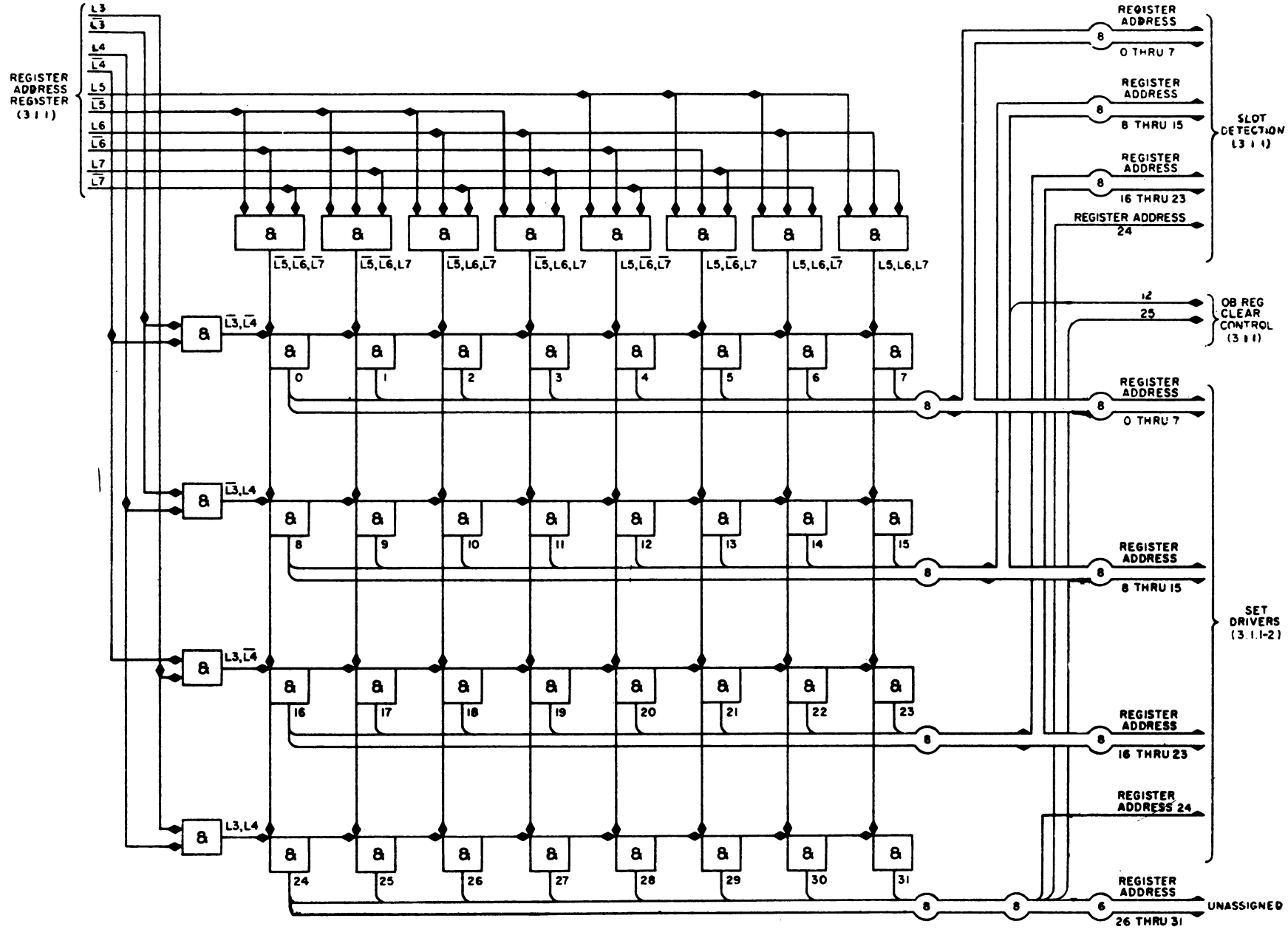


Figure 2-14. Register Address Decoder (3.1.1), Simplified Logic Diagram

c. Register Address Decoder

Each right-half word entering the Output System has as associated register address in binary code. The address consists of five bits with 32 possible combinations. A decoding operations is then necessary to produce one signal corresponding to each 5-bit address (Figure 2-14).

Bits L3 to L17 are applied to the decoder from the register address register flip-flops. Two of the five bits (L3 and L4) are fed in four combinations to four AND circuits. The remaining bits (L5, L6, and L7) form eight combinations, each of which is applied to an AND circuit. By further combining the L3 and L4 AND outputs with the L5, L6, and L7 AND outputs, output signals are produced on 32 possible lines, each line representing a different register address.

A +10v level is produced on the line which corresponds to the decoded address. This level is then sent to the STD's in preparation for reading the right half drum word into a storage section register address. Register addresses 0 through 24 are passed to the STD's whereas register addresses 25 through 31 are designated unassigned. The G/A-TD storage section uses register addresses 0 through 11; the G/G storage section, addresses 0 through 24; and the TTY storage section, register addresses 0 through 24. Note that register addresses 0 through 24 are sent to the slot detection network and that addresses 12 and 25 are sent to the OB register clear control circuit. The register assignments are given in Table 2-3.

d. Slot Detection, Circuit Description

Note: Refer to Figure 2-15.

As each right-half drum word is ready to be placed in a storage section register, the corresponding slot is noted in the slot detection circuit. The purpose of this circuit is to produce signals which are used in the G/G and G/A-TD output storage sections to determine how many registers in each slot are filled. The TTY output storage section does not require slot detection information since there is only one register per slot for this storage section.

It is necessary to produce a +10v slot level on the line associated with a particular slot whenever a G/G or G/A-TD word appears which has a register address corresponding to this slot. This is known as slot detection. The G/G slot levels are developed as the outputs of five 6-way OR circuits; each OR circuit produces an output for each register address introduced from the register address decoder. One G/G storage section has 25 registers divided into five slots. Consequently, only register addresses 0 through 24 are required to produce G/G slot signals 1 to 5. Hence, five + 10v slot levels are required for each G/G slot (one +10v level for each word read into a slot); in effect, this indicates that all five registers of a message slot are filled and can be transmitted. Therefore, if a G/G array were filled with information, 25 +10v levels would be generated, indicating that 25 registers are filled and ready for transmission.

The G/G slot levels are also produced by a d-c level from the completed message shift register. This signal, labeled clear-G/G-CMSR, is not associated with a specific right-half drum word. Rather, it is a timed level which arrives just before

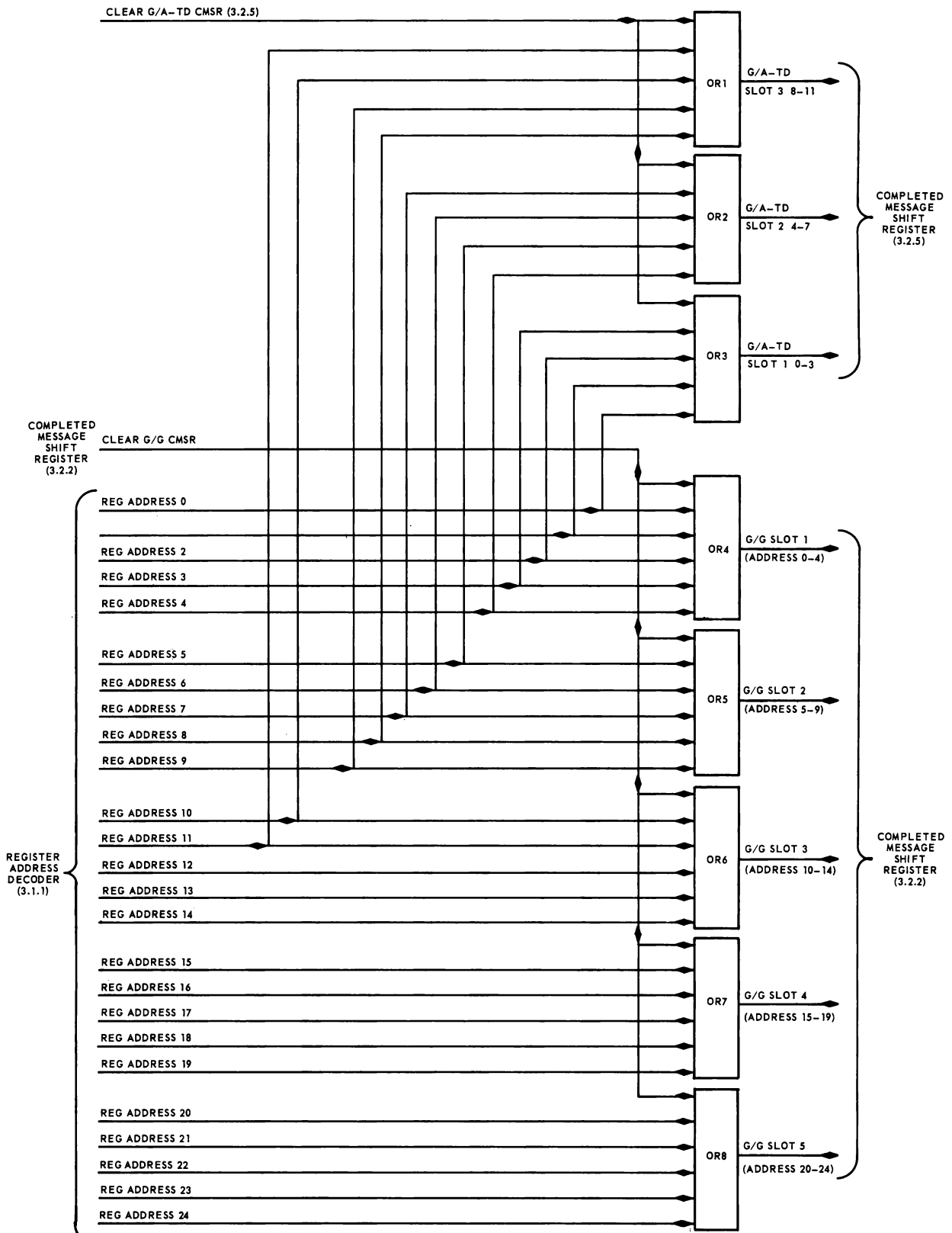


Figure 2-15. Slot Detection Circuit (3.1.1), Simplified Logic Diagram

CODED REGISTER ADDRESS (INPUT)					DECODED REGISTER ADDRESS (OUTPUT)
L3	L4	L5	L6	L7	
0	0	0	0	0	Register address 0
0	0	0	0	1	Register address 1
0	0	0	1	0	Register address 2
0	0	0	1	1	Register address 3
0	0	1	0	0	Register address 4
0	0	1	0	1	Register address 5
0	0	1	1	0	Register address 6
0	0	1	1	1	Register address 7
0	1	0	0	0	Register address 8
0	1	0	0	1	Register address 9
0	1	0	1	0	Register address 10
0	1	0	1	1	Register address 11
0	1	1	0	0	Register address 12
0	1	1	0	1	Register address 13
0	1	1	1	0	Register address 14
0	1	1	1	1	Register address 15
1	0	0	0	0	Register address 16
1	0	0	0	1	Register address 17
1	0	0	1	0	Register address 18
1	0	0	1	1	Register address 19
1	0	1	0	0	Register address 20
1	0	1	0	1	Register address 21
1	0	1	1	0	Register address 22
1	0	1	1	1	Register address 23
1	1	0	0	0	Register address 24
1	1	0	0	1	Register address 25
1	1	0	1	0	Register address 26
1	1	0	1	1	Register address 27

1	1	1	0	0	Register address 28
1	1	1	0	1	Register address 29
1	1	1	1	0	Register address 30
1	1	1	1	1	Register address 31

Table 2-3. Register Address Assignment

readout begins, to check the completeness of a G/G message, if any, in each message slot. If a G/G message slot is not filled by the time G/G readout is to take place, that message is considered to be incomplete and is not sent out on the telephone lines. The action of the G/G slot levels in the completed message shift register of the output storage section is to prevent a G/G message from being sent to the telephone lines if the clear-G/G-CMSR signal arrives at the slot detection OR circuits before all the registers in a slot have been filled.

Although the register addresses for all six storage sections enter the five OR or G/G circuits, the signals are rejected from the completed message shift register unless the shift pulse from the shift-completed message shift register pulse generator (Figure 2-15) is also sent to the completed message shift register. Since this pulse is sent only if the section address is G/G, if the burst number compares with the G/G burst counter, and if G/G search time is in progress, the completed message shift register responds to the slot signal only if a G/G word is to be entered.

The operation of the slot detection circuit for G/A-TD is the same as that described for the G/G storage section except that G/A-TD has only three slots. Also, a G/A-TD word whose register address is 0 through 3 produces a G/A-TD slot 1 pulse; register address 4 through 7, a G/A-TD slot 2 pulse; and register address 8 through 11, a G/A-TD slot 3 pulse.

6. Illegal Address Detection

a. Introduction

At present, not all of the possible storage section addresses and register addresses are assigned. A code representing one of the unassigned addresses is known as an illegal address and denotes an address error. The detection of illegal register and section addresses is discussed below.

b. Illegal Section Address Detection

Of the eight possible storage section addresses, only three (sections 2, 3, and 5) are presently used. Consequently, the presence of section address 0, 1, 4, 6, or 7 is indicative of a section address error. An error in a section address is detected by means of the illegal section address circuit (Figure 2-16). The detection is accom-

plished by passing either one of the illegal select-section levels through an OR circuit to condition a gate. The illegal-section pulse is produced when either the parity-NG or the parity-OK pulse samples the gate. In this manner, the illegal-section pulse is generated after the parity check is made and is independent of the parity check results. The illegal-section pulse is then sent to the alarm section; also, the no-compare pulse generator. A no-compare pulse cannot be generated if there is an illegal-section level (+10v) present.

c. Illegal Register Address Detection

Consider first an illegal register address associated with a TTY or G/G word, both of which have the same number of registers. Referring to Figure 2-17, note that a select-section level, designating that the G/G or the TTY section, as called for by the left-half drum word, is sent by the section decoder to the illegal register address detection circuit. The OR 1 circuit applies a level to the AND 1 circuit if either of these sections is designated by the left-half drum word.

Also applied to this AND circuit are bits L3 and L4 of the left drum word, and bit L5, L6, or L7 of the left drum word, via the OR 2 circuit. These bits make up the coded register address. Therefore, in order for AND 1 to pass a pulse, a select-section-2 or -3 pulse must be present (G/G or TTY); bits L3 and L4 must both be 1's; and one of the bits L5, L6, or L7 must be a 1. Checking the register address assignment table (Table 2-3), bits L3 and L4 are both 1's only for register addresses 25 through 31. However, only for register addresses 25 through 31 is there a 1 for L5, L6, or L7. Therefore, only for register addresses 25 through 31 does the AND circuit produce a +10v level. In brief, then, a +10v level is produced from the AND 1 circuit if the decoded section address portion of the drum word is G/G or TTY and the coded register address bits have 1's in such a position as to call for register address 25, 26, 27, 28, 29, 30, or 31. Since these register addresses are unassigned, and therefore are illegal, the level designates an illegal address.

The G/A-TD storage section uses register addresses 0 through 11. Referring to Figure 2-17, the AND 2 circuits will produce a +10v level only when the select-section-5 level is present and when register address bit L3 is a 1. Referring to Table 2-3, L3 will be a 1 for addresses 16 through 31, making these addresses illegal. The AND 3 circuit will pass a +10v level when the select-section-5 level is present and when register address bits L4 and L5 are 1's. These bits will both be 1's for addresses 12, 13, 14, and 15, thereby making them illegal. Therefore, a +10v illegal-address level will be produced by either AND 2 or AND 3 for addresses 12 through 31.

The three AND circuits feed an OR circuit. Therefore, if any of the AND 1, 2, or 3 circuits passes an illegal-register-address level, the OR circuit will pass this level. This conditions a gate which then passes an illegal-address pulse derived from either the parity-OK or parity-NG pulse. In this way, the illegal-register-address pulse is generated after the parity check is made and is independent of the parity check results. The illegal-address pulse goes to the output alarm section and the illegal-address level goes to the no-compare pulse generator. A no-compare pulse cannot be generated if there is an illegal-register-address +10v level.

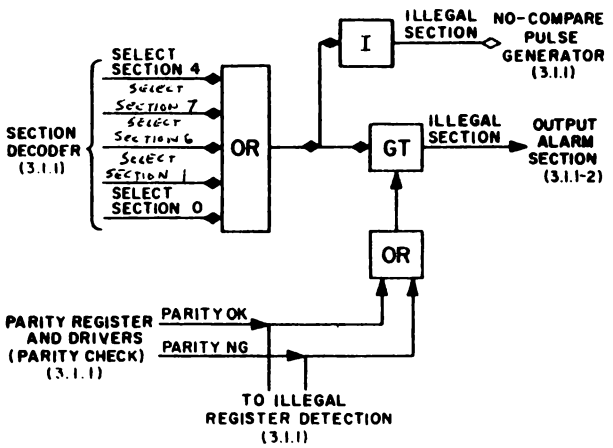


Figure 2-16. Illegal Section Address Detection (3.1.1), Simplified Logic Diagram

7. Storage Element

Note: Refer to Figure 2-18.

a. Review of Operations

The following briefly summarizes the action of the Output System to this point. The drum word received from the OB drum, after being placed in the flip-flop register, is examined to ascertain its parity, section address, register address, and storage array slot. Moreover, provision is made for detecting an illegal register or section address. In addition, the burst number is compared with the contents of the burst counter in the output control element. Favorable results of the above tests then form the basis for acceptance of a right-half drum word by the Output System.

The flow of a right-half word from the drum word register through the STD's and half-write current generator to a storage matrix is shown in Figure 2-18. The read-in control circuit acts as a valve which permits the passage of an acceptable right-half word and prevents entrance of a right-half drum word which does not conform to the established criteria.

The read-in operations associated with each drum word occur during a 5.4 usec interval from OD 2 to OD 4 +0.4 (OD 4 pulse delayed 0.4 usec). A drum word is received by the OB register from the OB fields at OD 1 time. Between this OD 1 time and the following OD 2 time, the operations mentioned in the preceding text occur. The right-half drum word, output storage parity bit, and register address pulses are present in the STD's by the OD 2 time. If the drum word is acceptable, this data will be transferred to the selected storage section through the half-write current generator. The acceptance of a drum word is determined by the read-in control circuit.

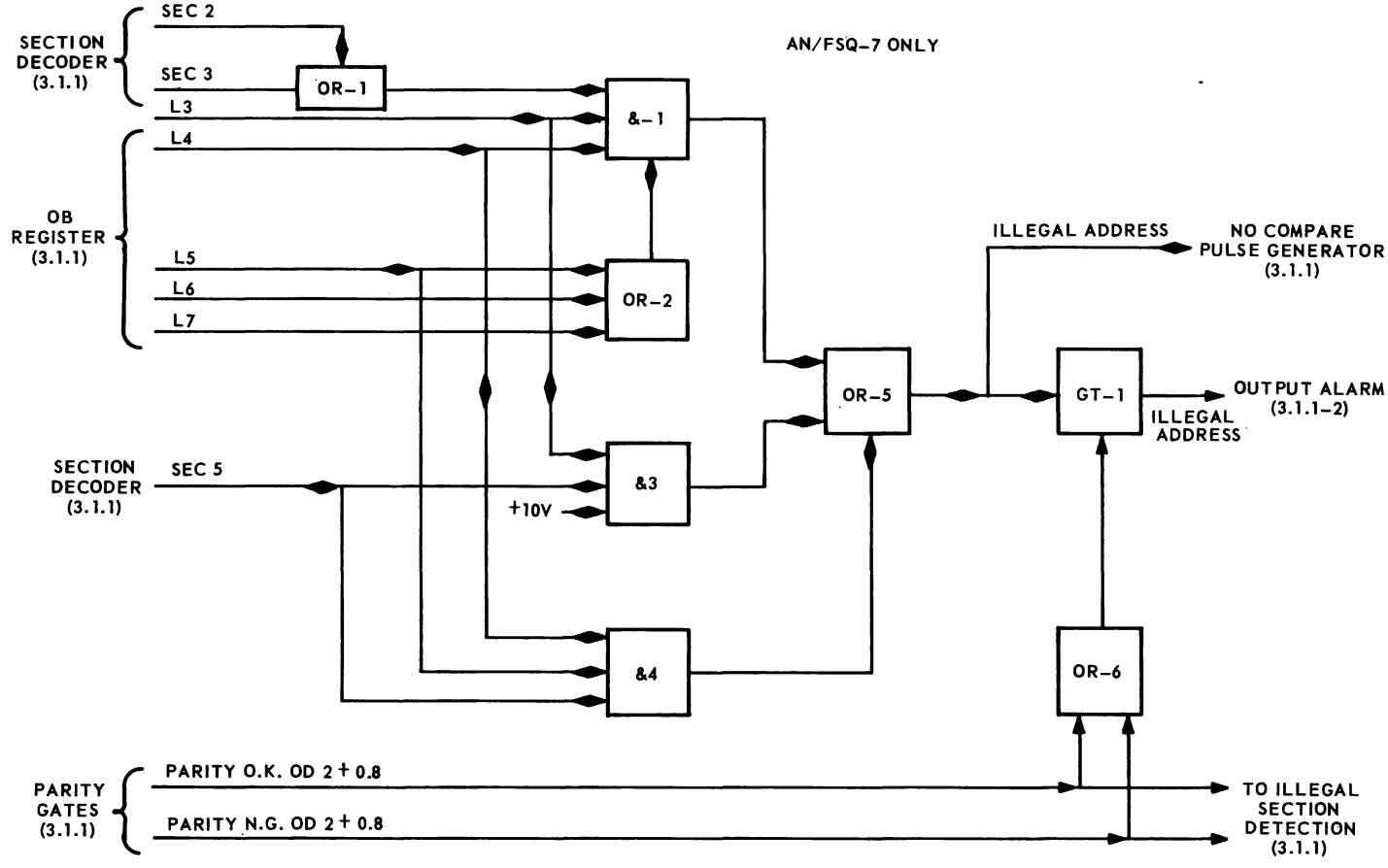


Figure 2-17. Illegal Register Address Detection (3.1.1), Simplified Logic Diagram

At the initiation of read-in operations, the read-in control circuit is supplied with the data required to determine whether the drum word is to be accepted and then transferred. This information is:

(1) The selected storage section.

(2) The result from each burst counter of the comparison between the burst number and the contents of the burst counter.

(3) The presence of search or nonsearch time in each storage section.

(4) The result of the parity count.

If a storage section is selected and the burst number matches the contents of the burst counter associated with the selected storage section, the right-half of the drum word is intended to be transmitted by the selected storage section during the current burst period. A storage section receives data during the first part of a burst period called search time. It transmits the data during the later portion of the burst period, called readout time, and receive data during readout. The read-in control circuit is informed of the portion of a burst period in progress in each of the three storage sections.

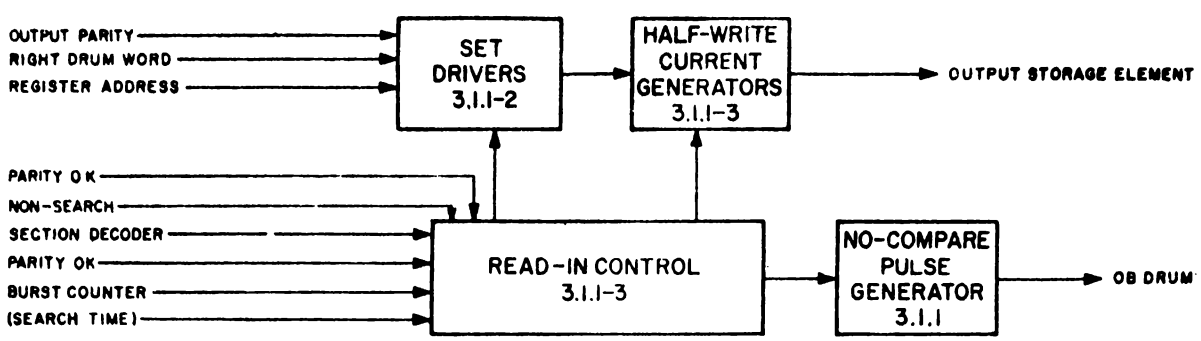


Figure 2-18. Read-In to Storage Element, Simplified Logic Diagram

If, at the initiation of the read-in operation, search time is in progress in the selected section, if the burst number is equal to the contents of the selected storage section burst counter, and if no parity or address errors are detected, the drum word is acceptable. With these favorable conditions present, the read-in control circuit causes the transfer of the data in the STD's to the selected storage section. However, if all conditions are the same except that readout is in progress, the drum word is missing from the burst being transmitted. This is referred to as a nonsearch alarm condition. When such a condition is detected, an alarm pulse is generated by the read-in control circuit and sent to the alarm section of the output control element. Also, the word is rejected and effectively erased from the OB field.

If there are no errors in the drum word, but the burst number does not compare, the drum word is assumed to have arrived too early and is not acceptable at this time. Under this condition, the read-in control circuit causes the no-compare pulse generator to produce a no-compare pulse. This pulse is sent to the OB fields and causes the register associated with the drum word to retain its status. Thus, although the drum word is rejected, it remains on the OB fields for acceptance during a future burst period.

Whenever a parity or address error is detected in a drum word, or a non-search condition exists, while at the same time the burst number compares, the generation of a no-compare pulse is suppressed. Thus, whenever an error is found, the status of the drum word register on the OB fields is changed (the word is erased). In addition, the read-in control circuit prevents the transfer of data to the storage element. This arrangement provides a means of eliminating incorrect or missed drum words from the OB fields and preventing their transmission.

The read-in control circuit produces the signals required to transfer the data from the STD's through the half-write current generator. The half-write current generator, in general terms, consists of several channels, any of which could be filled with the data from the STD's. At least one channel connects the half-write current generator with each storage section. Upon acceptance of the drum word, the read-in control circuit ensures that the data from the STD's is routed through the proper channel in the half-write current generator to the selected storage section.

At OD 2 time (start of read-in) three inhibit pulses are generated by the read-in control circuit and sent to the half-write current generator flip-flops. These inhibit pulses block the channels to the storage sections that are not selected. A set pulse is generated 1.2 usec after the inhibit pulses, producing a level which is sent to the STD's. The set level gates the data (right-half drum word, storage parity bit, and register-address levels) to the half-write current generator. As a result of the inhibit pulses, the data is placed only in the selected storage section channel (the one uninhibited channel). At the termination of read-in to the CCD's, a reset level is produced in the read-in control circuit at OD 4 + 0.4 time. This reset level is applied to the CCD's of the selected storage section and shifts the data to the selected address of the selected storage section.

b. Read-In Control

Note: For an over-all block diagram of read-in control circuits, refer to Figure 2-19.

The read-in control circuit gathers the data that is necessary for the acceptance of a drum word. On the basis of the collected information, the circuit responds either to accept or reject the word. If the word is acceptable, the read-in control circuit initiates steps which subsequently cause the word to be transferred into its storage section.

The read-in control circuit is divided into four parts. Those portions of the read-in control circuit that are associated with the G/G, G/A-TD, and TTY drum words form three of the four parts. The remaining part is that which is common to all three.

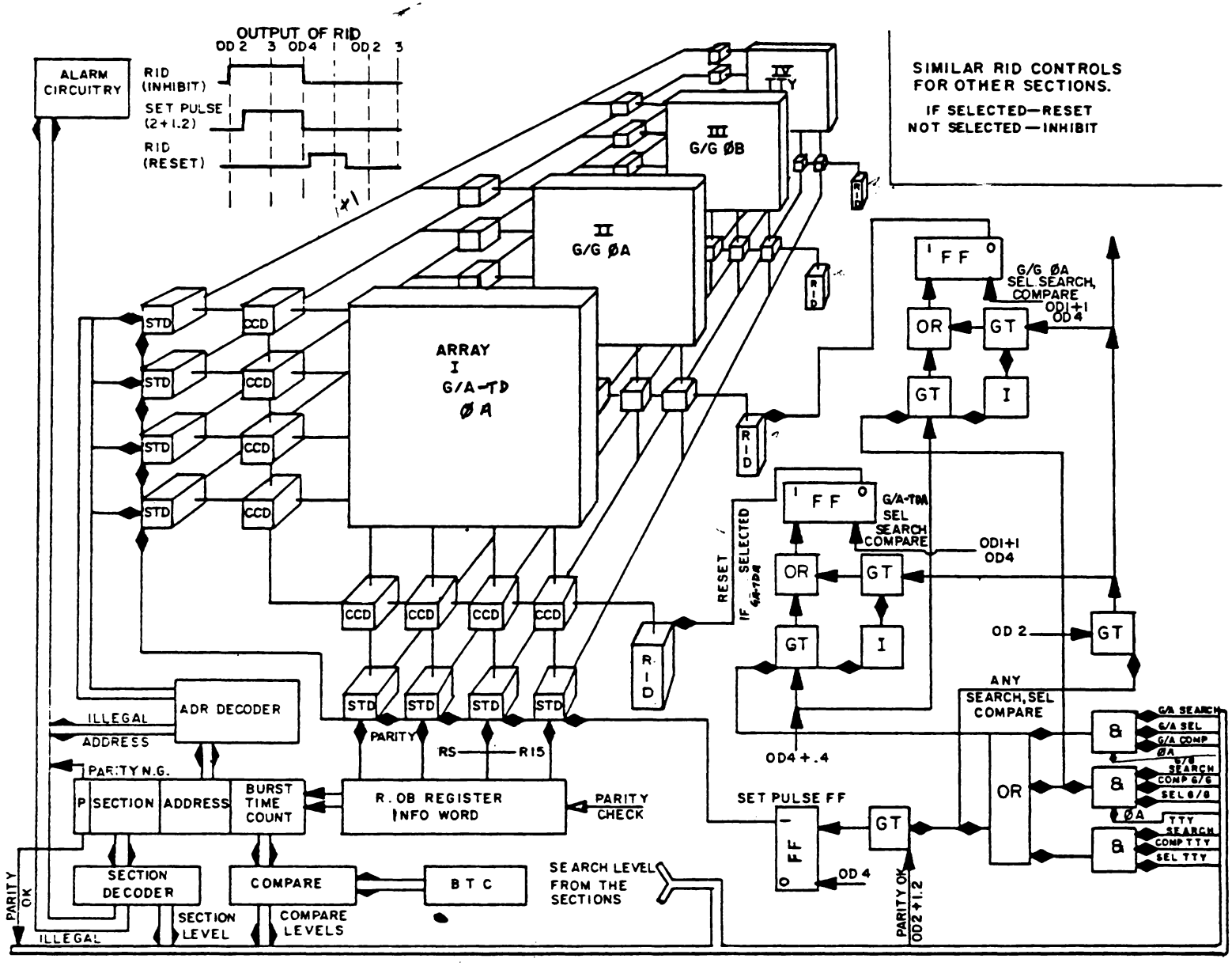

OUTPUT OF RID
OD 2 3 OD4 1 OD 2 3
ALARM CIRCUITRY
RID (INHIBIT)
SET PULSE (2+1.2)
RID (RESET)
SIMILAR RID CONTROLS FOR OTHER SECTIONS.
IF SELECTED—RESET
NOT SELECTED—INHIBIT
IV TTY
III G/G ØB
II G/G ØA
ARRAY I G/A-TD ØA
STD
CCD
R-I-D
F F
G/G ØA SEL SEARCH, COMPARE
OD1+1 OD4
OR
GT
I
G/A-TDA SEL SEARCH COMPARE
RESET IF G/A-TDA SELECTED
OD 2
ANY SEARCH, SEL COMPARE
G/A SEARCH
G/A SEL
G/A COMP
ØA
G/G SEARCH
COMP G/G
SEL G/G
TTY SEARCH
COMP TTY
SEL TTY
8
ADR DECODER
ILLEGAL ADDRESS
PARITY N.G.
PARITY
RS—R15
P SECTION
ADDRESS
BURST TIME COUNT
R.OB REGISTER INFO WORD
PARITY CHECK
OD4+.4
SET PULSE FF
OD 4
PARITY OK OD2+1.2
SECTION DECODER
COMPARE
B T C
SEARCH LEVEL FROM THE SECTIONS
PARITY OK
ILLEGAL
SECTION LEVEL
COMPARE LEVELS

Figure 2-19

The G/G, G/A-TD, TTY, and common parts of the read-in control circuit are discussed separately, followed by a summary of their combined operation.

The action of the G/G read-in control can best be understood by referring to the simplified logic diagram (Figure 2-18). The G/G read-in control operations are dependent upon six levels; search-G/G, compare G/G, select-section-2, not-search-G/G, and either shift-phase A or shift-phase B. The select-section-2 level is received from the address decoder, and when up, indicates that the drum word in the OB register is addressed to the G/G storage section. The search or not-search and the shift-phase A or B levels originate in the G/G storage sections. The G/G compare level, when up, informs the G/G read-in control that the burst numbers of the drum compare with the G/G burst counter. The two levels, search-G/G and not-search-G/G, are up alternately. A positive G/G search level denotes that search time for the G/G storage section during the current G/G burst period is in progress and data may be read into its select array (A or B). However, when the not-search level is up, it indicates that read-out time for the current G/G burst period is in progress and data cannot be read into either G/G storage array. As G/G has two arrays, one of which is being read into while the other is being read out of, the non-search level is up for a very limited time as compared to the search level. The two levels, shift-phase A and shift-phase B, also originate in the G/G storage section. These two levels are alternately up and indicate which array is to be read out of during the current burst period. Notice that the shift-phase A level is applied to the G/G-B read-in control circuit, and the shift-phase B level is applied to the G/G-A read-in control circuit. Thus, when the select-section-2, search-G/G, and compare-G/G levels are up coincident with the shift-phase B level, a reset G/G-A pulse is generated in preparation for reading into G/G matrix A. The polarity of these six levels establishes the basis for acceptance or rejection of data for the G/G storage section and governs the action of the G/G read-in control. Three groupings of the six levels are:

(1) Select-section-2, compare-G/G, search-G/G, and shift phase A or B levels are up.

(2) Either the select-section-2, compare G/G, or the search G/G level is down. Shift phase A or B will be up.

(3) Select-section-2, compare-G/G, not-search, and shift phase A or B levels are up.

Should the select-section-2, compare-G/G, and search G/G levels be up simultaneously, it is an indication that the word is acceptable to the G/G storage section. The array of actual read will be determined by the presence of either the shift phase A or shift phase B levels from the G/G storage sections. Only one of these levels may be present at a time. This word will be accepted provided the above conditions exist and there has been no illegal section, illegal address, and parity is OK. A select-search-compare-G/G level is produced to condition GT 3 which is used in conjunction with the CMSR circuitry in the G/G storage section. The select-search-compare G/G levels in conjunction with a shift-phase A or B level is applied to either GT 1 or GT 2, as determined by the shift-phase level present. Assuming the presence of the shift-phase A level, GT 1 and I 1 would be conditioned. At OD 2 time, GT 4 and GT 5, as well as similar GT's from all other sections, are strobed. As I 2 is not conditioned, it will

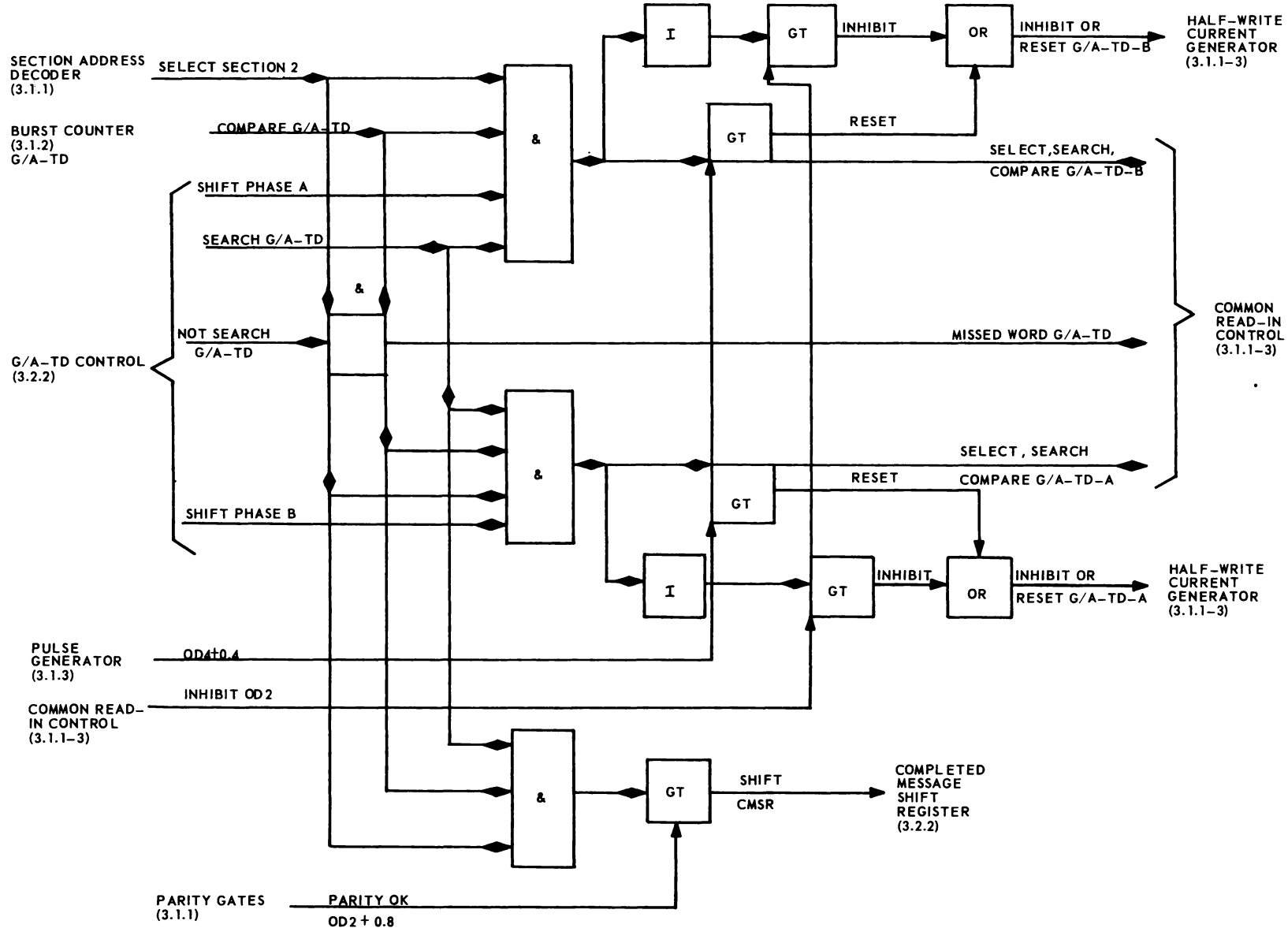


Figure 2-19A. G/A-TD Read-In Control (3.1.1), Simplified Logic Diagram

have an output of +10 volts to condition GT 4. Similar GT's in all non-select sections will also be conditioned by their inverters not being conditioned (selected). The OD 2 pulse will be passed by GT 4 (and other non-selected GT's) to set the current generator FF's of all non-selected arrays, thereby generating RID inhibit current to the CCD's of the non-selected arrays. The RID's for the selected array (G/G-A) will not be conditioned and therefore the G/G-A CCD's will not be inhibited. The Set-Pulse FF will be set at OD 2 + 1.2 usec. (Parity OK, OD 2 + 0.8 usec, Delayed .4 usec.) The set-pulse FF will condition the STD's. Upon being conditioned, the STD's attempt to write the output word (RHW + Parity) into all arrays. Only the selected array (G/G-A) may be written into, as all others are inhibited through the action of their RID's being turned on. If the select-section-2, compare-G/G, and not-search levels are up, a missed (non-search) condition exists. This signifies that the word in the OB register is missing from the G/G burst that is to be transmitted in the subsequent burst period.

The levels which originate in the G/G storage section are designated shift-phase A and shift-phase B. The nature of the two levels is such that they do not occur simultaneously; each level, when up, denotes that the contents of its associated array is being read out. Consequently, output words can be written into the other array. Thus, when the select-section-2, search-G/G, and compare-G/G levels are up coincident with the shift-phase B level, a reset-G/G-A pulse is generated in preparation for reading into G/G matrix A.

Another function of the read-in control circuit is the generation of shift pulses which are passed to the completed message shift register in the G/G output storage section. The completed message shift register and the shift pulse are used with the G/G slot level to count the number of words entered into the G/G storage array. The read-in control circuit is used to generate the required shift pulses. A combination of a parity-OK pulse, and compare, search, and select-section levels for a G/G word generates a completed-message-shift-register-shift pulse; that is, a shift pulse is produced once for each word entered into a G/G storage array. Hence, coincidence between a shift pulse and a slot level indicates that the slot level is for G/G rather than for the other sections.

Refer to Figures 2-21 and 2-22.

The common read-in control functions when a select-search-compare G/G-A, G/G-B, G/A-TD-A, G/A-TD-B, or TTY level is present (Figure 2-22). One of these levels passes a 5-way OR circuit and is applied to GT 1, GT 2, and the no-compare pulse generator.

Gates 1 and 2 will conduct when strobed. Gate 2 is strobed by an odd parity pulse at OD 2 + 1.2 time, producing a set pulse which is sent to the STD's. This set pulse causes the STD's to transfer the right half-word, its parity bit, and its register address to the half-write current generator. Similarly, GT 1 is sensed by an OD 2 pulse which is passed and sent to the G/G, G/A-TD, and TTY read-in sections as an inhibit (OD 2) pulse.

Missed-word levels from the three storage section read-in control circuits are sent to a 3-way OR circuit in the common read-in control. Any one of these levels will pass and be supplied as non-search levels to both GT 3 and the no-compare pulse

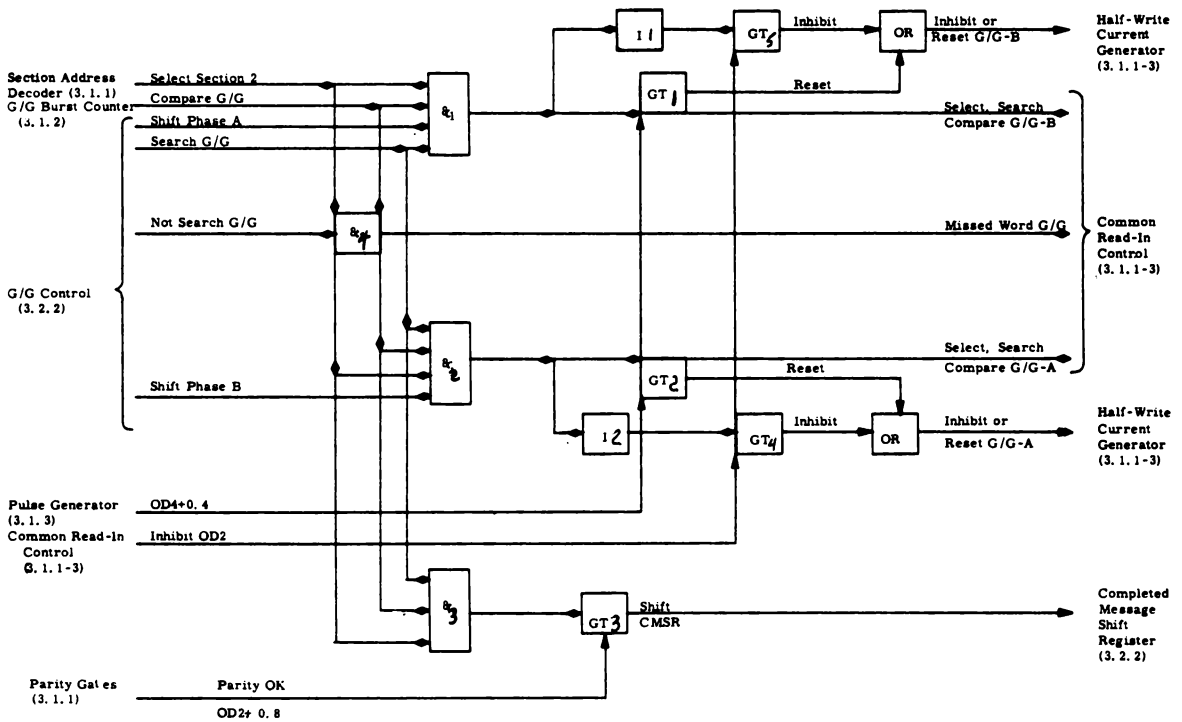


Figure 2-20. G/G Read-In Control (3.1.1-3)

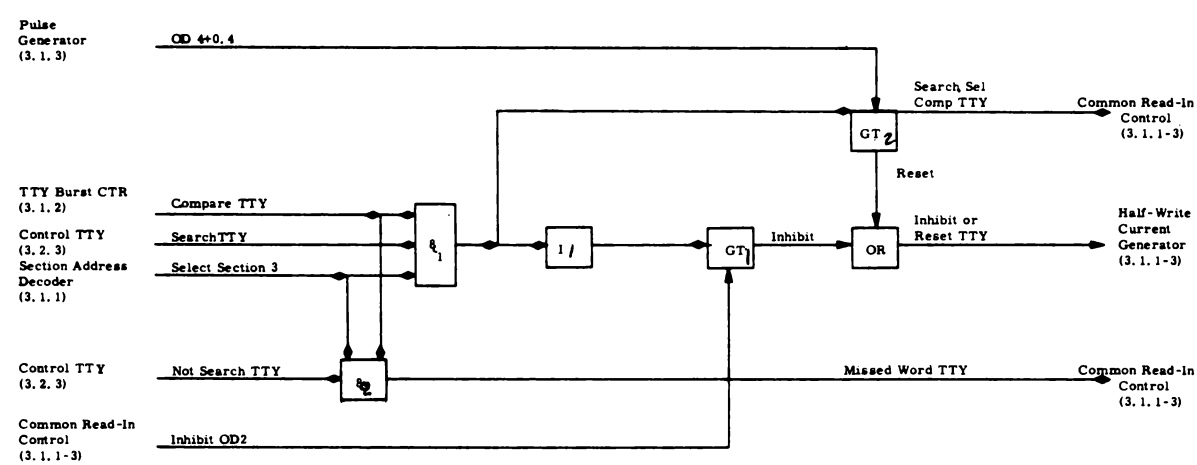


Figure 2-21. TTY Read-In Control (3.1.1-3)

generator. A positive nonsearch level indicates a missed word combination which means that the drum word in the OB register would be erased. This is accomplished by suppressing the no-compare pulse and not relaying the data to the storage element. The nonsearch level conditions GT 3 which is strobed by an OD 4 + 0.4 reset pulse from the OB register clear control. The output from GT 3 is a nonsearch pulse that is sent to the alarm control section where it causes a nonsearch alarm to be generated. The over-all action of the read-in control circuit can best be described by considering the case of a G/G word. Assume that the select-search- and compare-G/G levels are up; with this condition present, the other sections find the word unacceptable, and, consequently, their select-search-compare levels are down. However, the G/G read-in control finds the word acceptable. As a result of the positive select-search-compare-G/G level, an inhibit (OD 2) pulse is generated by the common read-in control. This pulse, under the existing conditions, prevents the output data from being transferred to the G/A-TD and TTY storage sections.

The next step of the common read-in control is to pass (1.2 usec later) a set pulse (OD 2 + 1.2) which will set the set-pulse flip-flop, causing a level of +10v to be generated for 3.8 usec (OD 2 + 1.2 to OD 4). The generated +10v level is applied to the STD's, causing the output data to be transferred from the STD's to the G/G CCD's. The timing is such that the transfer of data from the STD's to the CCD's of the other sections is inhibited by the 5 usecs inhibit level. A reset-G/G pulse is generated by the G/G read-in control 4.2 usec later (OD 4 + 0.4). The reset-G/G pulse causes the transfer of the data from the half-write current generators (CCD's) to the G/G storage array, terminating the read-in.

c. No-Compare Pulse Generator

When a word is accepted by the Output System, the drum register containing the word is used to store a succeeding word. This has the effect of erasing the first word. However, should the assigned burst number of a word not compare with the burst count at this time, it may be necessary to retain the word on the drum, thereby making it available to the Output System during the next drum cycle. In this manner, a word may be stored until the time it is scheduled to be transmitted; that is, when the assigned burst number does compare with the burst count. When all conditions (with the exception of compare) are favorable for the acceptance of a word, a no-compare pulse is generated and sent back to the drum section. This prevents the word from being erased from the OB drum.

A simplified logic diagram of the no-compare pulse generator is shown in Figure 2-23. The signals which affect the generation of the no-compare pulse are as follows:

(1) Nonsearch level when burst number compares (missed word).

(2) Illegal section.

(3) Illegal register.

(4) Search-select-compare.

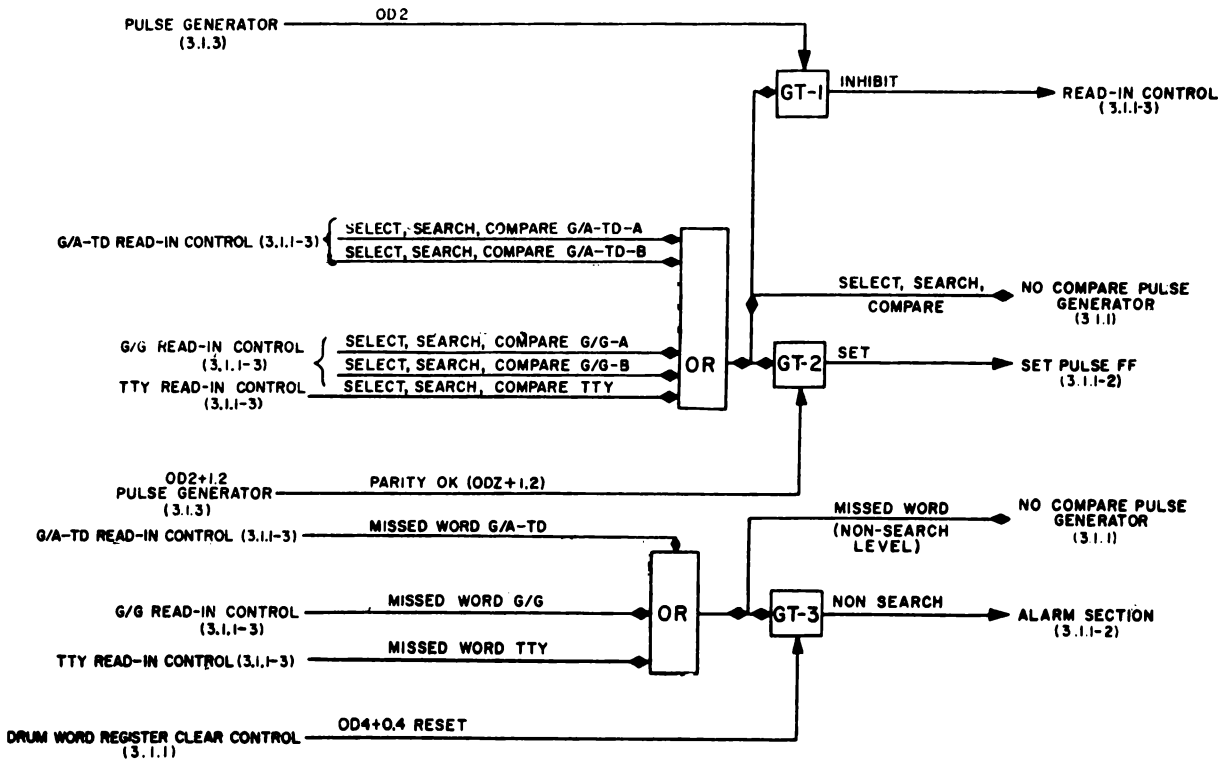


Figure 2-22. Read-In Control Common Equipment (3.1.1-3), Simplified Logic Diagram

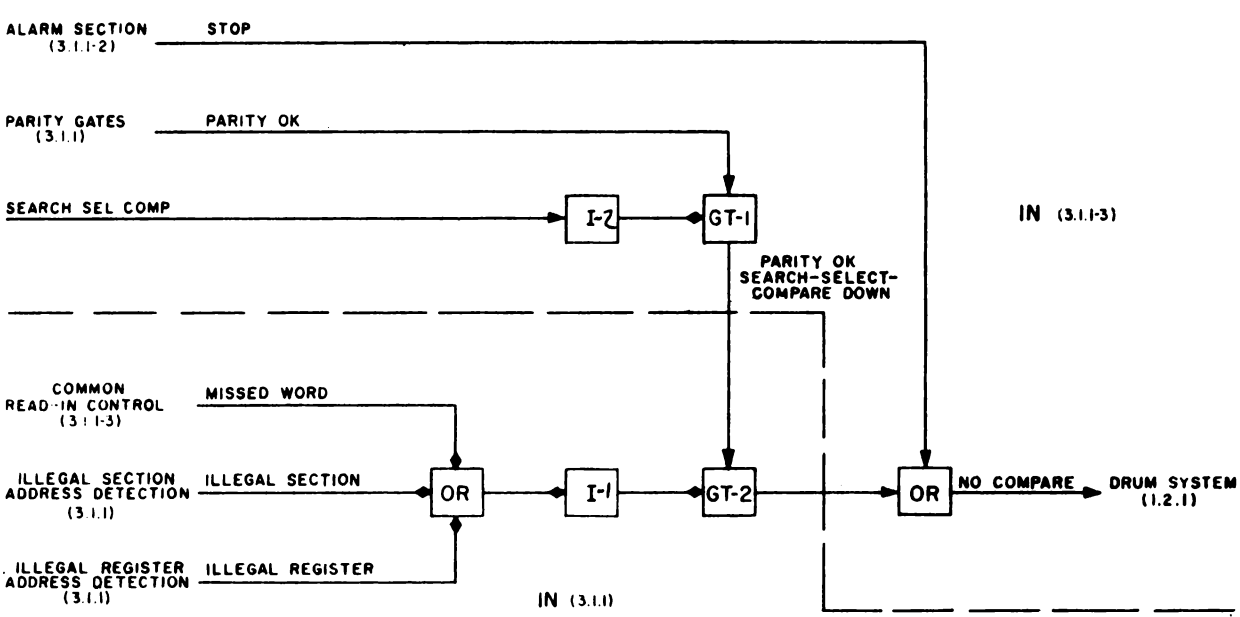


Figure 2-23. No-Compare Pulse Generator (3.1.1-3), Simplified Logic Diagram

(5) Parity-OK.

Since the above signals, with the exception of parity-OK, are applied to inverters, the no-compare pulse can be generated only when all these signals are coincidentally absent (assuming correct parity). The presence of any one of these signals automatically inhibits the production of a no-compare pulse.

Gate 2 passes a no-compare pulse only if the following conditions are present:

(1) Select-search-compare down (-30v).

(2) No missed word.

(3) Legal address.

(4) Legal section.

(5) Parity OK.

The select-search-compare level will be down without affecting one of the other listed conditions in only two situations; search and no-compare or nonsearch and no-compare. Either one of these situations will bring the select-search-compare level down, but a no-compare pulse will be generated only if the four remaining listed conditions are met. It should be noted that bringing the select-search-compare level down (-30v) in any other way will result in acquiring either a missed-word or an illegal-section level, either of which prevents the generation of a no-compare pulse. This is summarized in Table 2-4.

The previously mentioned signals are functions of four basic variable quantities, assuming that parity is OK; these are compare, select section, select register, and search time. In Table 2-4, the 0's indicate the absence and the 1's denote the presence of the quantity shown at the top of each column. The 16 possible combinations of the four basic signals are shown with the resultant effects of those signals used for no-compare pulse generation. It should be noted that the missed-word signal occurs when select section and compare occur during nonsearch time. The results show that no-compare is generated when the assigned burst number does not compare with the burst count, providing that the section and register addresses are legal and parity is OK (Table 2-1). The significance of these results may be summarized as follows:

(1) First, it is desired to retain a word on the OB drum when it appears before its predetermined time of transmission. This is accomplished by returning a no-compare pulse to the Drum System when the assigned burst number does not compare with the burst count.

(2) Second, it is not desired to retain a word associated with incorrect parity, illegal register or illegal section address. Consequently, a no-compare pulse is generated only when parity is correct and the section and register addresses are valid.

(A 0 INDICATES ABSENCE: A 1 INDICATES PRESENCE)

Compare	Section	Register	Search	Missed Word	Illegal Section	Illegal Register	Search Select Compare	No-Compare
0	0	0	0	0	1	1	0	0
0	0	0	1	0	1	1	0	0
0	0	1	0	0	1	0	0	0
0	0	1	1	0	1	0	0	0
0	1	0	0	0	0	1	0	0
0	1	0	1	0	0	1	0	0
0	1	1	0	0	0	0	0	1
0	1	1	1	0	0	0	0	1
1	0	0	0	0	1	1	0	0
1	0	0	1	0	1	1	0	0
1	0	1	0	0	1	0	0	0
1	0	1	1	0	1	0	0	0
1	1	0	0	1	0	1	0	0
1	1	0	1	0	0	1	1	0
1	1	1	0	1	0	0	0	0
1	1	1	1	0	0	0	1	0

Table 2-4. Tabular Summary, No-Compare Pulse Generator

(3) Third, the generation of a no-compare signal is not restricted to a word occurring during search time. Thus, a word that does not compare and occurs during nonsearch time (being favorable for acceptance in other respects) can be made available for transmission when it does compare (i.e., at a later time).

Referring again to the no-compare generator, it will be noted that aside from the above considerations the no-compare signal is also generated upon the appearance of a stop pulse from the alarm section. (See Figure 2-23.) The stop pulse is generated when either parity-NG, illegal-section, or illegal-register signals exist. This enables an incorrect word to be retained on the drum for further examination.

8. Set Drivers

A set driver (STD) is basically a coincidence type circuit which produces a current that is capable of changing the state of a core from 0 to 1. Functionally, the STD circuit, shown in Figure 2-24, delivers signals to the half-write current generator for each address, for busy bits, whenever a 1 appears in the right drum word and when an output parity bit is included. These outputs are produced only when these 1's appear at the same time as a set pulse from the read-in control circuit. (See Figure 2-22.) It will be recalled that the set signal is generated by a word accepted by one of the six storage sections. Therefore, the STD circuit serves as common equipment for all words accepted by the Output System. The actual selection of a storage section occurs in the half-write

current generator circuit. It should be noted that only those words which prove acceptable for transmission cause the STD's to send the appropriate signals to the half-write current generator.

There is provision in the STD's for generating two 1 bits, referred to as busy bits, whenever data is transferred from the STD's to the half-write current generator. The generation of these busy bits is made possible by the connection of two STD's to a + 10v source. Thus, whenever a set pulse is applied to the STD's, the two busy bits are produced and transferred, together with the other data, to the half-write current generator. These busy bits are required by the TTY storage section.

Provisions are made for register addresses 0 through 24, representing the maximum number of registers used in any one output storage section. However, for a given word, only one register address level is present. Thus, the information sent to the half-write current generator consists of signals denoting a register address, the right drum word, output parity, and busy bits. The manner in which this information is employed by the half-write current generator is discussed in the following paragraphs.

9. Half-Write Current Generator

The half-write current generator circuit produces currents which are capable of changing the state of ferrite cores from the signals delivered to it by the STD's and the read-in control circuit. These currents are utilized by a ferrite core storage matrix in the output storage section to cause storage of a word in the matrix.

a. Flip-Flops and Reset-Inhibitor Drivers

The current generator is discussed from the standpoint of the current generator flip-flops, shown in Figure 2-25, and the current generator matrix, shown in Figure 2-26. It is the function of the flip-flops to deliver the required inputs to the reset-inhibit drivers (RID) which, in turn, deliver currents required by the current generator matrix. Functionally, a RID is capable of producing a current which will either reset or inhibit a change of state in the cores when applied to tape core windings. The cores are wound in a manner which causes a reset signal to reset the cores to the 0 state or an inhibit signal to prevent a core from being changed from 0 to 1. It is important to note that a RID produces an output voltage only from a negative voltage input. Referring to Figure 2-25, initially, all the flip-flops which control the RID's have been cleared and the 0 sides are up. Under this condition, there is no current out of the RID's and the half-write current generator cores (Figure 2-26) which are connected to the RID's can then have 1's set into them by the STD's. However, when an inhibit pulse is sent to a flip-flop, the 0 side is brought down to -30v. The corresponding RID then passes either an inhibit signal or a reset signal to the related cores in the half-write current generator. These two signals are identical in magnitude but differ in timing and function. An inhibit pulse is sent at the beginning of a read-in operation and prevents a 1 from being set into a core by the STD. A reset pulse is sent after the information is set into the cores and drives the cores which have been set to 1 back to 0. This causes the 1's to be read out of the cores and into the appropriate ferrite cores in the appropriate output storage array.

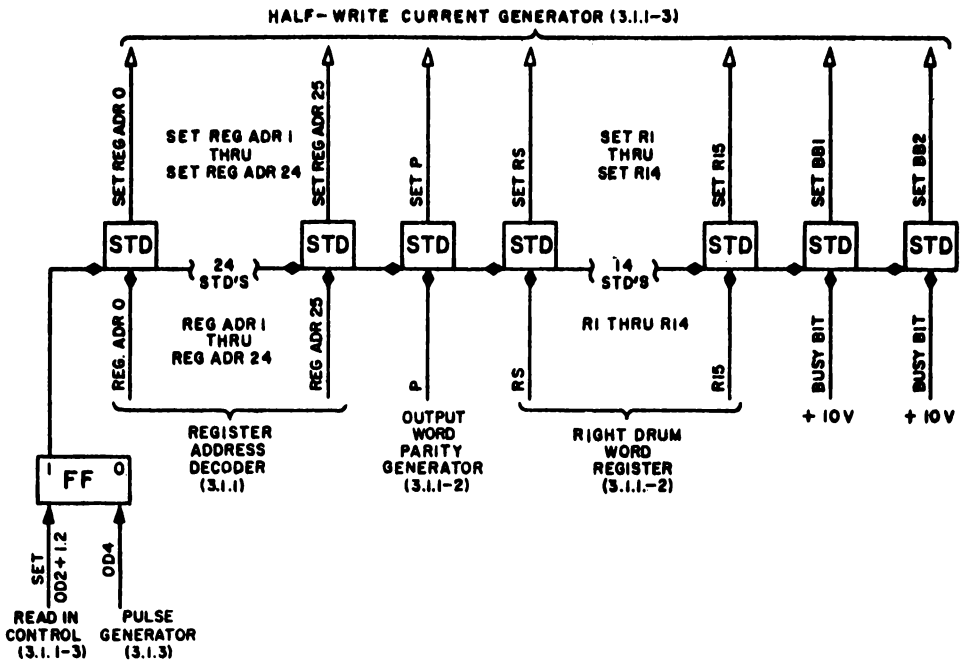


Figure 2-24. Set Drivers (3.1.1-2), Simplified Logic Diagram

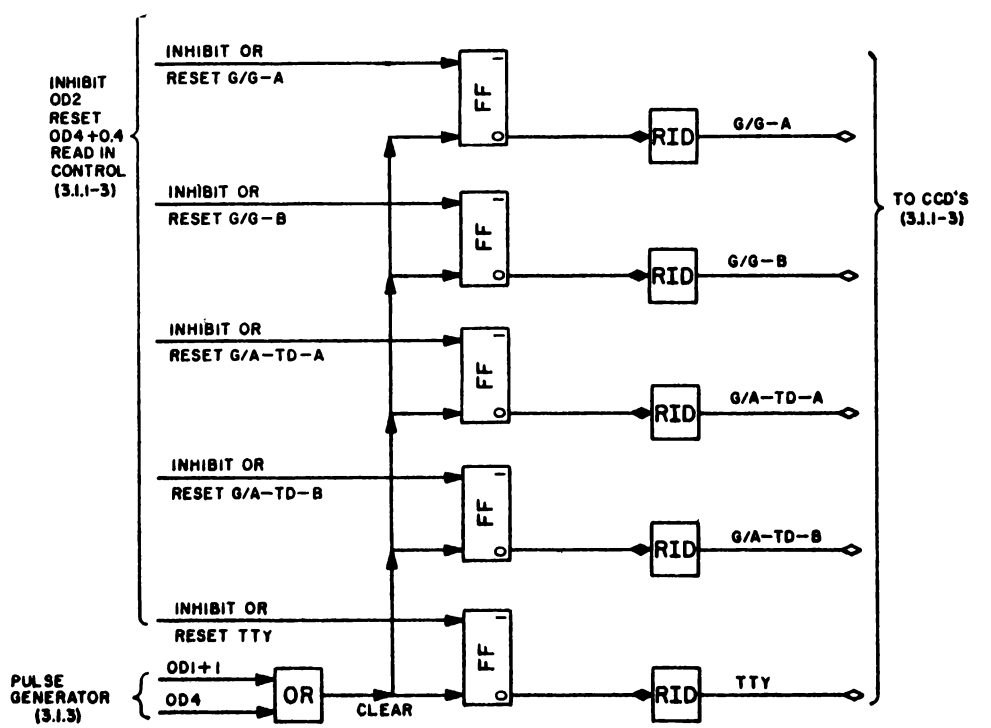


Figure 2-25. Half-Write Current Generator Flip-Flops (3.1.1-3)

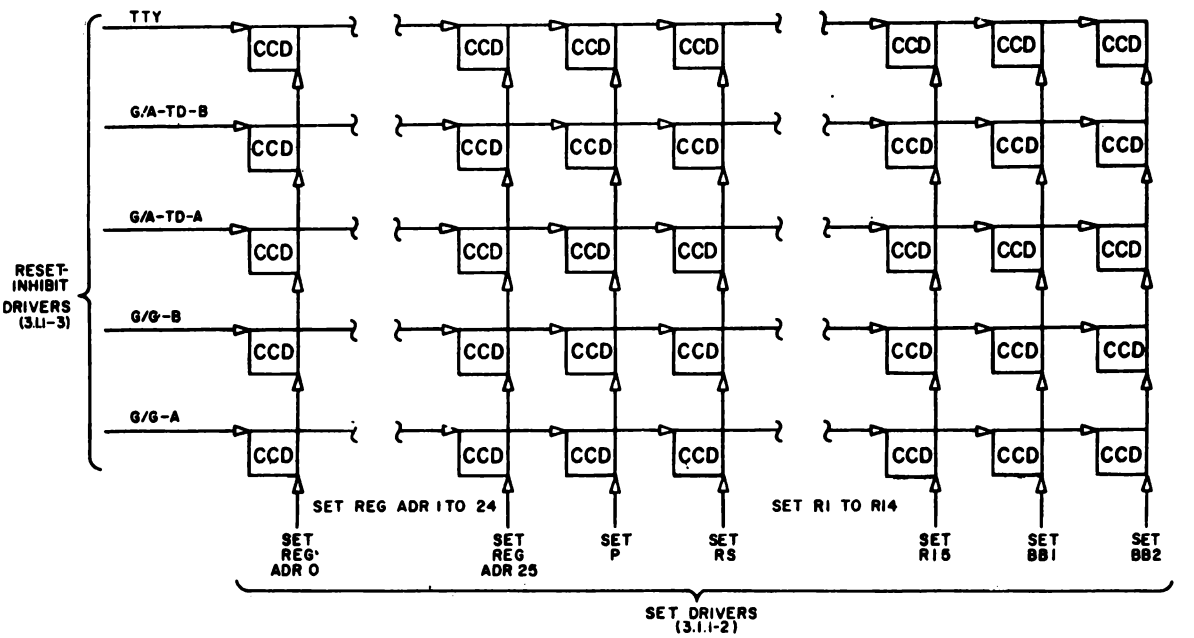


Figure 2-26. Half-Write Current Generator Matrix (3.1.1-3), Simplified Logic Diagram

b. Core Current Drivers

The half-write current generator matrix consists of 48 vertical columns and 12 horizontal rows of tape core current drivers (CCD). Each of the 576 CCD's is capable of delivering a current of half the amplitude required to cause a change of state in a corresponding ferrite core in the output storage element. At present, only five of the 12 rows are in use, one each for G/G-A, G/G-B, G/A-TD-A, G/A-TD-B, and TTY.

The lines which pulse the horizontal rows feed the signals in from the RID's. Similarly, the lines pulsing the vertical column bring the bits of the right drum word, the associated register address of that word, the output parity bit, and the busy bits from the STD's.

Initially, all the cores in the CCD's are in the 0 state. During the time that the vertical columns are pulsed, the horizontal row of cores corresponding to the section associated with the word being read into the CCD's is not pulsed. Those cores associated with sections not selected are pulsed by inhibit signals. In this manner, the cores corresponding to the selected section change state in accordance with the information being read in, whereas the other cores are prevented from changing state. That is, only in the selected section cores do 1 bits cause a change of state from 0 to 1; the 0 bits have no effect. Some time later, a reset signal is applied to all of the cores. This causes the cores containing the temporarily stored information to revert

to the 0 state and, in the process of changing state, the information is transferred out as half-write currents. For the sake of clarity, the lines leading to the output storage element from each CCD are not shown in Figure 2-26.

c. Timing Cycle

To illustrate how the half-write current generator functions, consider the case for a G/G-A word. The timing sequence for this condition is shown in Figure 2-27. The drum word, after being taken off the OB drum, is placed in the drum word register. The contents of the right drum word register are then made available to the STD's during the interval between OD 1 and OD 4 + 0.4. The STD's pass their information along to the CCD's of the half-write current generator OD 2 + 1.2 and OD 4. (See Figures 2-24 and 2-27.) (This assumes that all conditions are favorable for accepting the word.) Since the section selected is G/G-A, the read-in control circuit delivers inhibit signals to the half-write current generator flip-flops associated with the other seven arrays. Since an inhibit pulse is not delivered to the G/G-A flip-flop, the 0 side of this flip-flop is up. Therefore, there is no current from the RID associated with this flip-flop. On the other hand, the other RID's deliver inhibit currents to the CCD's associated with G/G-B, G/A-TD-A, G/ATD-B, and TTY, from OD 2 to OD 4, at which time the RID flip-flops are cleared. (See Figure 2-25.) Actually, only the RID's which were inhibited change back to the 0 side up, since the uninhibited RID (G/G-A, in this example) was not originally changed from this condition. The inhibit level is up for an interval that is concurrent with and slightly longer than the STD outputs representing the right drum word, the associated register address, and the busy bits. This assures complete inhibiting. Because of the inhibiting action, no information is placed in the CCD's corresponding to the sections not selected.

During the interval discussed above, the G/G-A CCD's are free to receive the right drum word, the corresponding register address, the output parity bit, and the busy bits. Referring again to the timing chart, it can be seen that the G/A-FD RID flip-flop output is up from OD 4 + 0.4 to OD 1 + 1 and represents a reset signal. (See Figures 2-18, 2-25, and 2-27.) No other information is being fed into the CCD's during this interval. The G/G-A reset signal clears the G/G-A CCD's to the 0 state, causing the temporarily stored data to be read into the G/G-A storage matrix in the output storage element. The CCD's are then all in the 0 state, prepared for the receipt of another word. It should be noted that the OD pulse times mentioned in this discussion are approximate, since considerations such as cable delays and rise and fall times of the circuits were not taken into account.

All the RID flip-flops are cleared at OD 1 + 1, as shown in Figure 2-25. This action sets the 0 side of the reset RID flip-flop up, the RID flip-flops which were inhibited having been cleared at OD 4.

Output Computer Section, Detailed Analysis

Over-all block diagram of the Output Computer section is Figure 2-28.

1. General

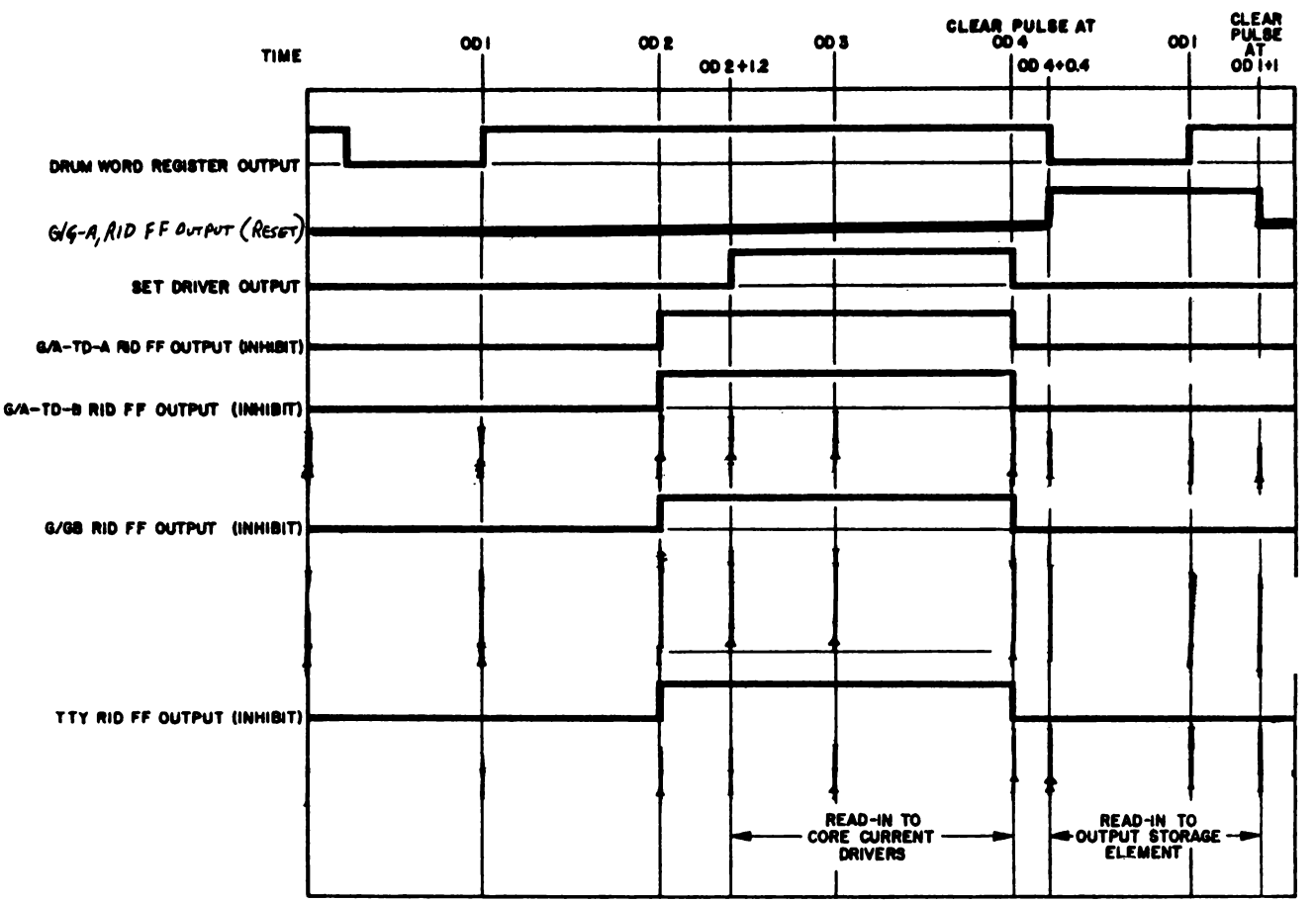


Figure 2-27. Half-Write Current Generator Timing for G/A-FD Word, Functional Representation

The Central Computer System must have access to the burst counts of current burst periods. The burst counts are contained in periodically stepped burst counters in the output control element and represent the burst numbers of current burst periods.

The transfer of the burst counts to the Central Computer System is accomplished in the output computer section of the output control element upon request by the Central Computer System. In addition, the output computer section generates various timing pulses used for controlling numerous operations throughout the Output System.

2. Burst-Count Selection and Transfer

Refer to Figures 2-29 and 2-30.

a. General

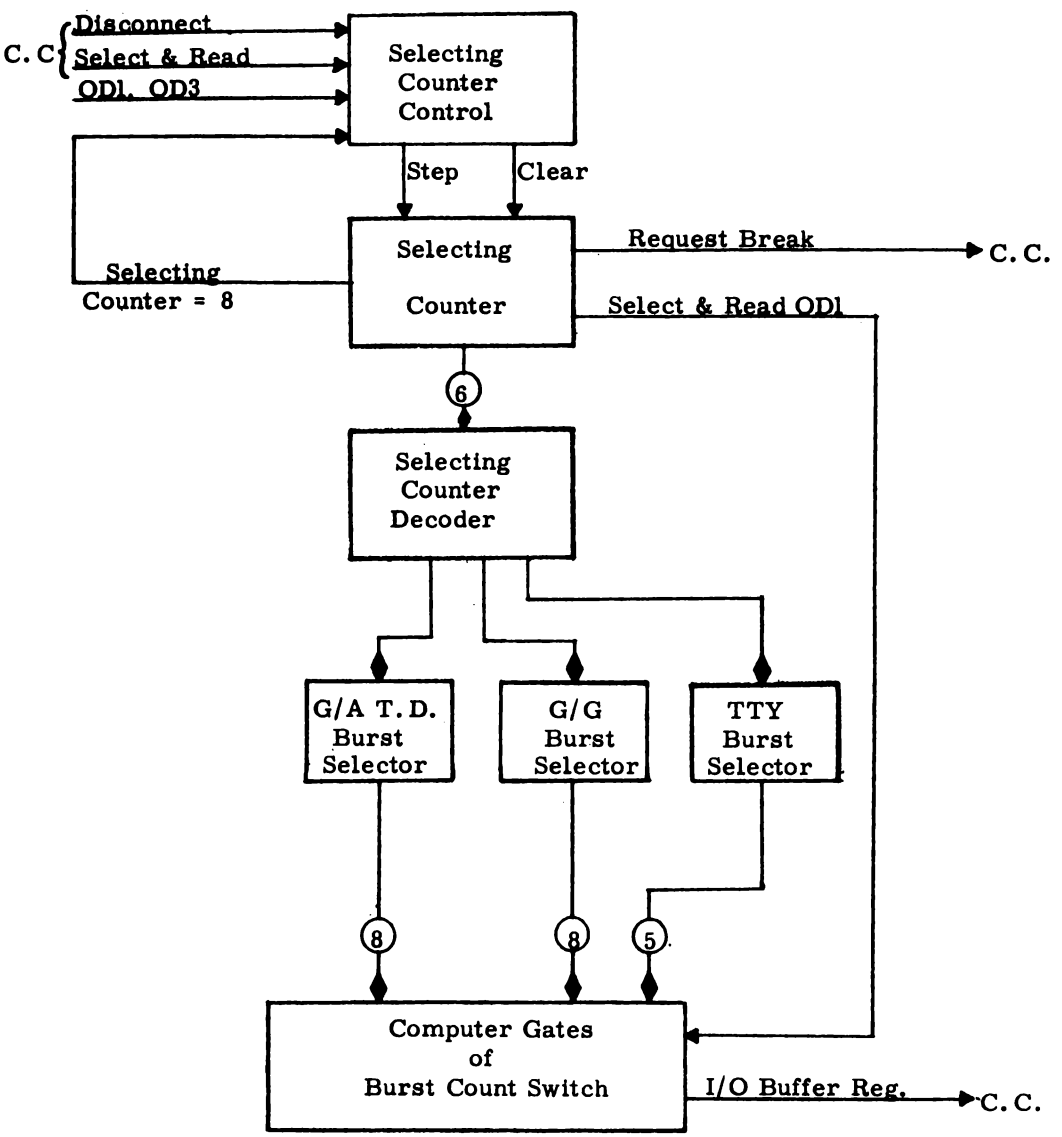


Figure 2-28. Output Computer Section (3.1.2) Block Diagram

The selection of burst counts and their transfer to the Central Computer System is the function of the output computer section. The contents of each of the three burst counters are made available to the Central Computer System through the sections of the burst-count selecting counter, the selecting counter decoder, and the burst-time count switch (See Figure 2-28.)

b. Burst-Count Selecting Counter

This circuit controls the read cycle of the burst-time count. During this cycle, the current contents of each burst counter are transferred to the Central Computer System. A burst-time count read cycle is initiated upon receipt of a select-and-read pulse from the Central Computer System. The burst-count selecting counter is then stepped at the rate of 100,000 pps (every 10 usec), causing successive 3-bit binary codes to be generated. Each code selects a different burst counter contents to the Central Computer System. After five codes have been produced, the contents of the three burst counters are in the Central Computer System (codes 000 and 011 are unassigned). The burst-time selecting counter then receives a disconnect pulse from the Central Computer System terminating the burst-time count read cycle.

The selecting counter control generates the stepping and clear pulses used by the selecting counter. A burst-time count read cycle is begun with the reception of a select-and-read pulse from the Central Computer System. As shown in Figure 2-30, the select-and-read pulse sets FF 1. This starts the following sequence of operations: the 1 side of FF 1 conditions GT 2, passing an OD 3, which sets FF 2; GT 4 is conditioned and passes the next OD 1 pulse; each successive OD 1 pulse is gated through GT 4 as long as FF 2 remains set; these OD 1 pulses are sent to the selecting counter as stepping pulses.

If (Figure 2-30) either a disconnect signal of selecting-counter-equals-eight pulse is applied to the OR circuit, FF 1 is cleared. Gate 1 is conditioned and the next OD 3 pulse is passed, clearing FF 2. The 0 side of FF 2 conditions GT 3 and the succeeding OD 1 pulse is gated through. All OD 1 pulses passed through GT 3 are sent to the selecting counter as clear pulses. The selecting counter generates the binary codes which select the burst counts to be transferred to the Central Computer System. This circuit is a scale-of-eight counter composed of three flip-flops. (See Figure 2-30.)

Refer to Figure 2-31.

As each burst-count read cycle begins, the counter is clear; i.e., the binary output is 000. The first stepping pulse applied to the counter produces an output binary code of 001. A second stepping pulse changes this to 010. The third stepping pulse causes the counter to generate a binary combination of 011. This counting process continues until the binary output is 111 or, in other words, the counter is equal to seven. The counter-equals-seven pulse is sent to the selecting counter control, thus causing the counter to be cleared. However, if a disconnect pulse is received by the selecting counter control prior to the action of the counter-equals-seven pulse, the counter is cleared at that time.

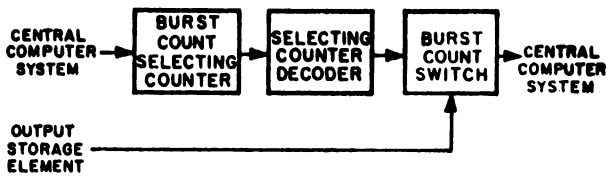


Figure 2-29. Burst Count Selection and Transfer, Block Diagram

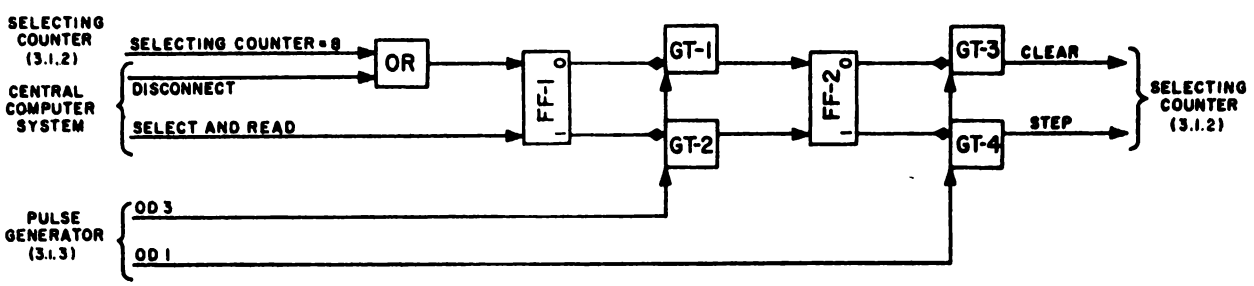


Figure 2-30. Selecting Counter Control (3.1.2), Simplified Diagram

Although the burst-count selecting counter is a scale-of-eight, its scale is controlled by the Central Computer System through the action of the disconnect pulse. The burst-count selecting counter is a scale-of-eight to produce a binary output for each of the eight possible storage sections. Since only three storage sections are employed, which utilize only three burst time counters, it would be a waste of time to allow the selecting counter to count its maximum limit. The Central Computer System is programmed for the number of burst-time counters that are employed in the Output System. The program determines the number of burst counts that can be received during a burst-time count read cycle. The Central Computer System then generates a disconnect pulse after receiving the number of burst-time counts desired, which may be one or more. For example, there are three storage sections in the output storage element. After five stepping pulses from the selecting counter control, the burst-count selecting counter is equal to five and the burst count from each of the three burst counters has been sent to the Central Computer System. The five stepping pulses have been sent to the Central Computer System as break-request pulses (Figure 2-31). These pulses prepare the Central Computer System for the reception of each burst count and they step a counter in the Central Computer System for each burst number transferred. When the counter in the Central Computer System counts the number of burst counts desired, it generates a disconnect pulse. The disconnect pulse causes the burst-count selecting counter to be cleared thus ending a burst-time counters read cycle. The select-and-

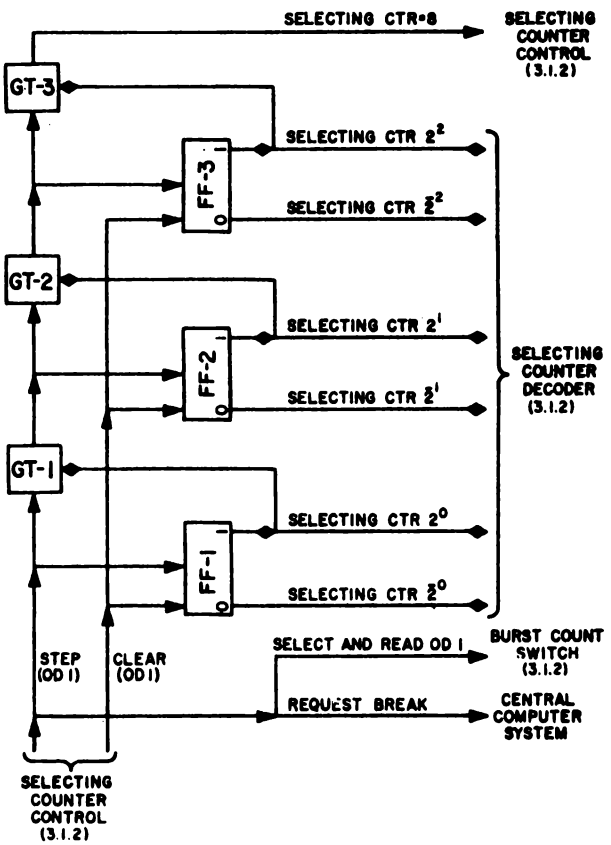


Figure 2-31. Selecting Counter (3.1.2), Simplified Logic Diagram

read OD 1 pulses (Figure 2-31) which are coincident in time with the stepping and break-request pulses, are fed to the burst-time count switch to cause the transfer of the burst-time and elapsed-time counts.

c. Selecting Counter Decoder

The selecting counter decoder receives the 3-bit binary combination from the burst-count selecting counter. For each binary code a signal to select a particular burst counter is produced and sent to the burst-time count switch.

As shown in Figure 2-32, the selecting counter decoder is composed of three 3-way AND circuits. The three inputs to each AND circuit constitute a different 3-bit binary code. Therefore, for each binary code received, an output level is produced by one of the three AND circuits. Only three levels are presently used. They are select-G/A-TD, select-G/G and select-TTY.

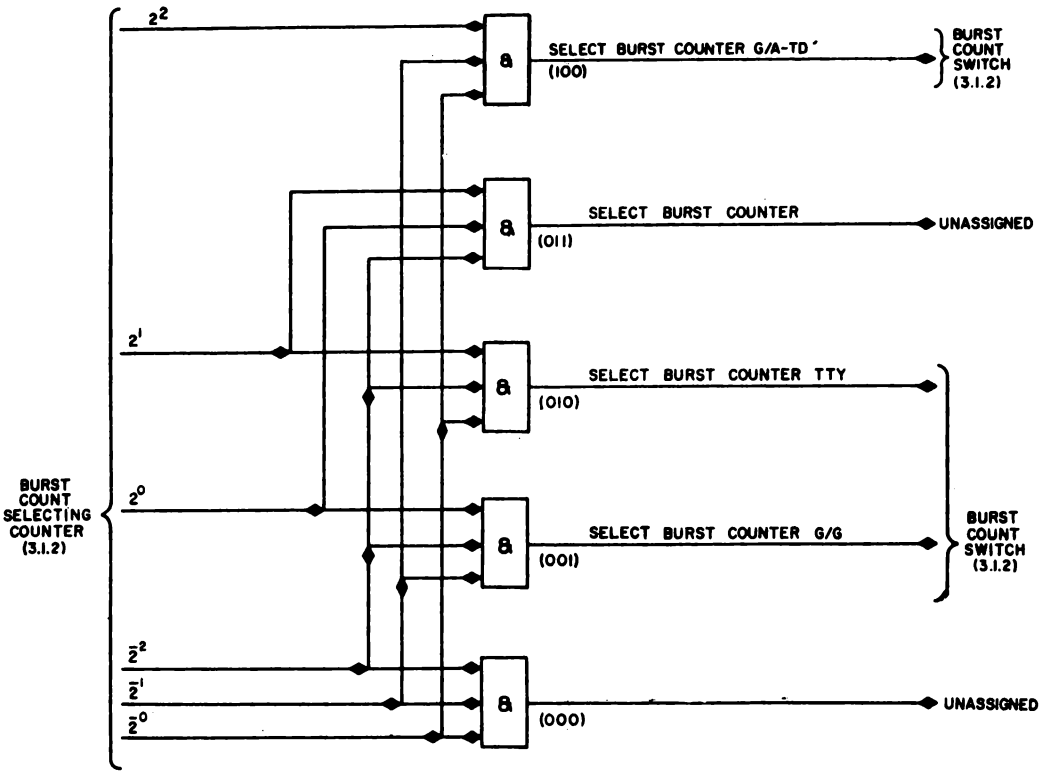


Figure 2-32. Selecting Counter Decoder (3.1.2), Simplified Logic Diagram

The first binary combination received by the decoder is 000 which is not used and will not condition any circuit. This is followed 10 usec later (time OD 1) by binary combination of 001 that causes a select-G/G-burst-counter level to be produced by AND circuit 2. The third binary code that is received during each burst-count read cycle is 010. At the time of reception of this binary code, AND circuit 3 generates a select-TTY-burst-counter level. The fourth binary code that is received during the burst-counter read cycle is 011. This causes AND circuit 4 to generate a level; however, this level has no application and is considered only for reasons of representing a count of the selecting counter. The final binary code that is received during each burst-count read cycle is 100. At the time of reception of this binary code, AND circuit 5 generates a select G/A-TD-burst-counter level.

d. Burst-Time Count Switch

The burst-time count switch contains the current count of each burst counter. It furnishes, through the burst-count readout process, the current contents of each burst counter to the Central Computer System. For purposes of discussion, the burst-count switch is divided into two parts, the burst selector and the computer gates. The burst selector is that part of the burst selector switch which is connected directly to

the burst counters. The burst selector is subdivided into three parts: the G/G burst selector, the G/A-TD burst selector, and the TTY burst selector. Each burst selector consists of a row of 2-way AND circuits. (See Figure 2-33.)

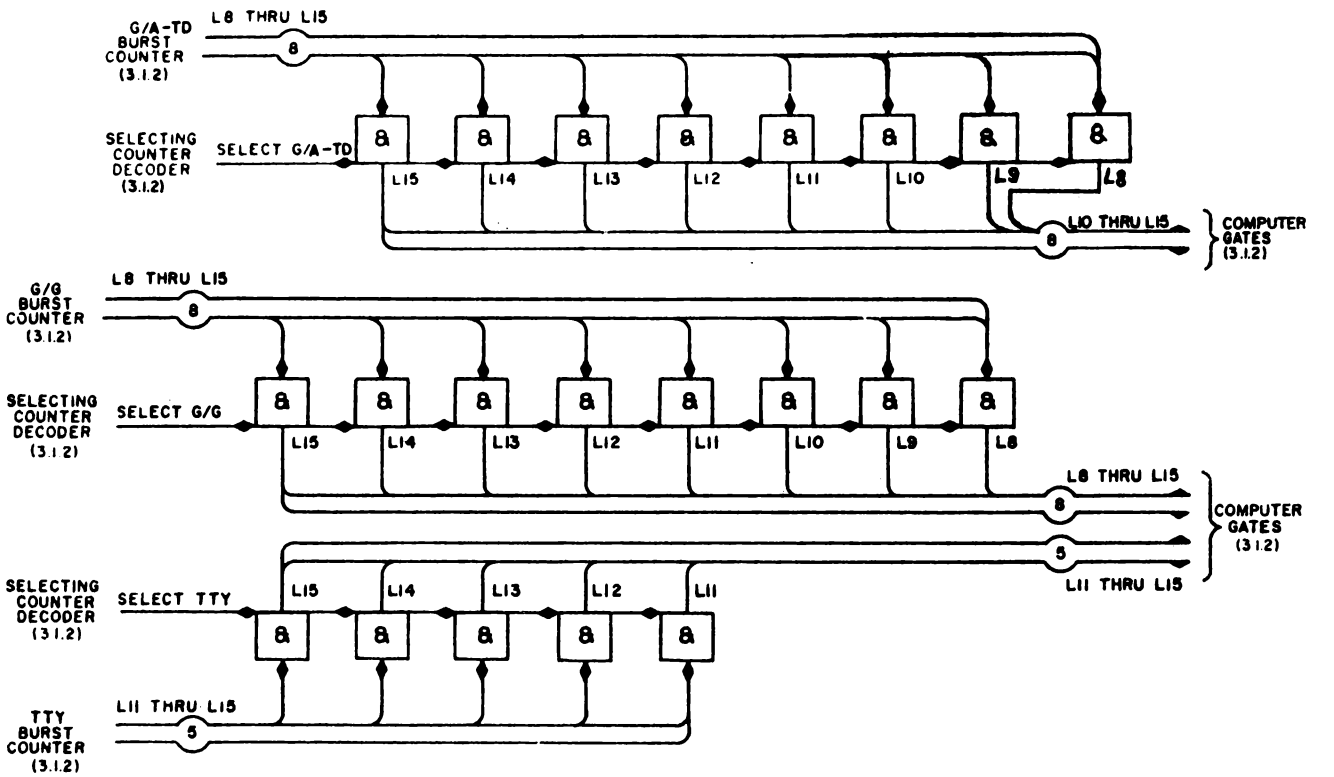


Figure 2-33. G/A-TD, G/G, and TTY Burst Selectors of the Burst-Time Count Switch

The first burst counter selected during a burst-count read cycle is the G/G-A burst counter. The contents of the G/G-A burst-counter level is applied to the AND circuits. The G/G-A burst count is then fed to the computer gate.

The TTY burst counter and the G/A-TD burst counters are selected after the G/G-A burst counter. Their burst counts are also sent to the computer gates as they are selected. The computer gates transfer the burst counts to the Central Computer System.

As shown in Figure 2-34, the bits fed from the burst selector are applied to a number of OR circuits. Each OR circuit is fed a corresponding bit from each burst counter. Since the burst counters are selected individually, only one of four lines applied to any OR circuit is up at any one time. The bits of the selected burst counter are passed through the OR circuits to condition their associated gates.

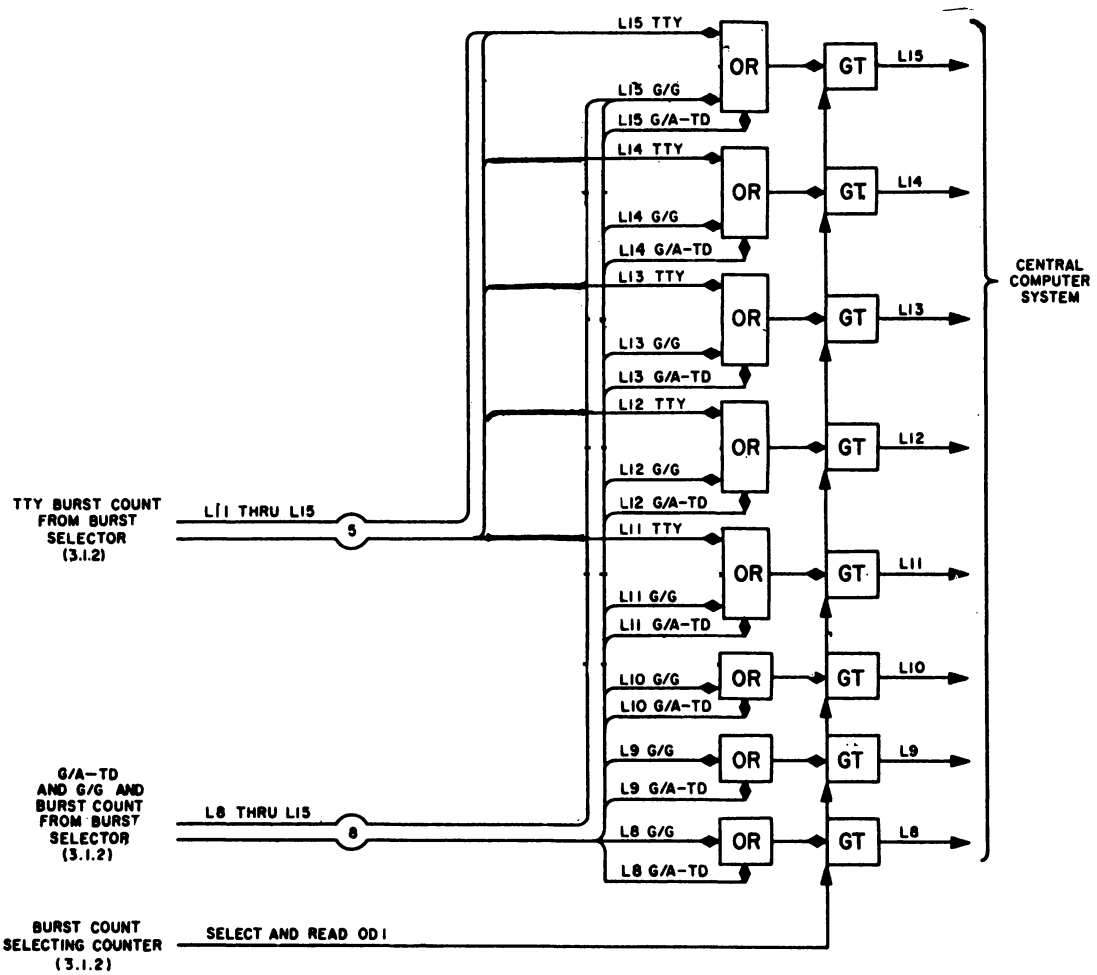


Figure 2-34. Computer Gates of the Burst-Time Count Switch (3.1.1-3), Simplified Logic Diagram

The pulse which gates the burst counts through to the Central Computer System is the select-and-read-OD 1 pulse. It is coincident with both the stepping pulse utilized by the burst-count selecting counter and the break-request pulse sent to the Central Computer System. Each time that this select-and-read-OD 1 pulse is generated, a different burst count is transferred to the Central Computer System.

To summarize the selection and transfer process, a complete burst-count read cycle is discussed below. During the discussion, refer to Figures 2-30 and 2-35.

Each burst-count read cycle is begun with the reception of a select-and-read pulse from the Central Computer System. However, prior to the reception of this pulse, the three units employed in the selection and transfer of the burst counts are in the following statuses:

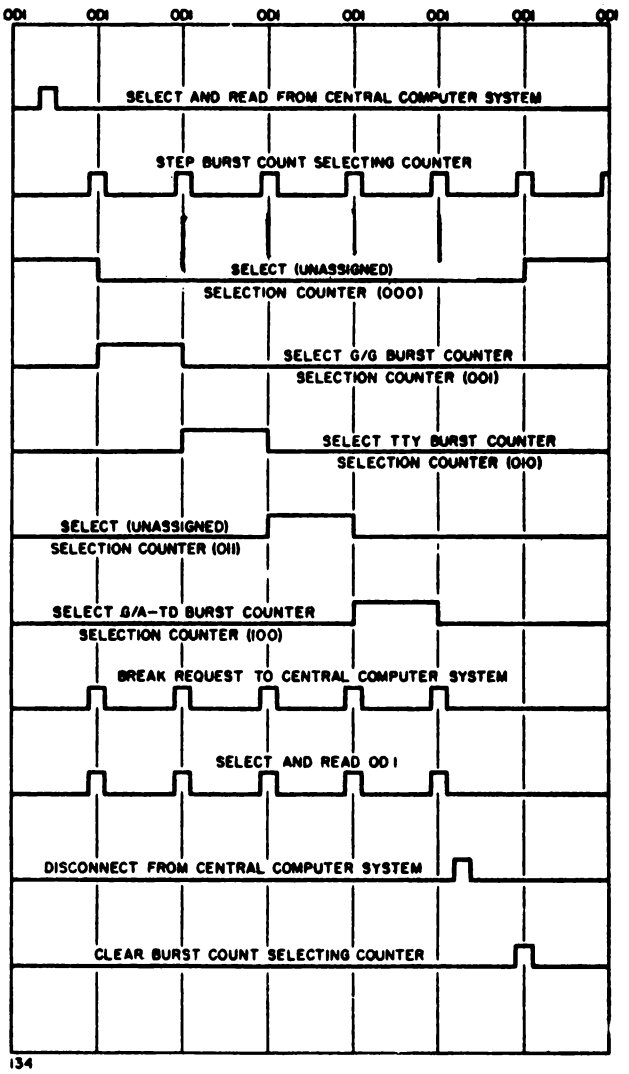


Figure 2-35. Burst Counter Read Cycle, Timing Chart
Functional Representation

(1) The burst-count selecting counter is clear; its binary output is 000.

(2) This binary code is unassigned.

When the burst-count selecting counter receives a select-and-read signal from the Central Computer System it feeds successive OD 1 pulses to the selecting counter as stepping pulses, to the Central Computer System as break-request signals, and to the computer gates as select-and-read-OD 1 signals.

The first OD 1 pulse initiates three operations which occur simultaneously. It steps the burst-count selecting counter, thus changing the binary output of the burst-count selecting counter to 001. Coincident with this, the Central Computer System receives a break-request pulse that prepares it for the reception of a burst count and also records the fact that one burst count is read. Simultaneously with these two operations, the first OD 1 pulse labeled select-and-read-OD 1, strobes the computer gates, as no BTC is conditioned, all zeros are transferred to the Central Computer System.

The binary code 001, which was produced as a result of the selecting counter being stepped by the first OD 1 pulse, then causes the select-G/G burst counter line to be up. This signal is applied to the G/G burst counter selector section, and the G/G burst count is fed to the computer gates.

The second OD 1 pulse, which occurs 10 usec after the first pulse, steps the selecting counter to 010, is sent to the Central Computer System as a break-request pulse, and gates the G/G burst count to the Central Computer System. The stepping of the selecting counter results in the selection of the TTY burst counter. When the third OD 1 pulse appears, it steps the selecting counter to 011, is sent to the Central Computer System as a break-request pulse, and transfers the TTY burst count to the Central Computer System.

The fourth OD 1 pulse, which occurs 10 usec after the third pulse, steps the selecting counter to 100 and is sent to the Central Computer System as a break-request pulse. However, no transfer of this particular count is made to the Central Computer because this count has no application.

The fifth OD 1 pulse occurs which steps the selecting counter to 101; it is sent to the Central Computer System as a break-request pulse and transfers the G/A-TD burst count to the Central Computer System.

3. Pulse Generator and Pulse Generator Conversion Unit

Refer to Figure 2-36.

a. General

The pulse generator and pulse generator conversion unit produce some and distribute all timing pulses used in the Output System (Figure 2-36). The pulse generator consists of several individual circuits which control and distribute all the pulses used in the Output System. It also contains the circuit which generates the 91-pps pulses. The pulse generator conversion unit is a circuit which generates 1,300-pps pulses. These pulses are fed to the pulse generator for distribution and control. Each of the circuits is described in the following paragraphs.

b. OD Pulse Distributor

Refer to Figure 2-37.

The OD pulse distribution circuit consists of four gates and four register drivers (Figure 2-37). Each gate is fed a different OD pulse from the Drum System. The OD pulses are a series of timing pulses generated within the Drum System.

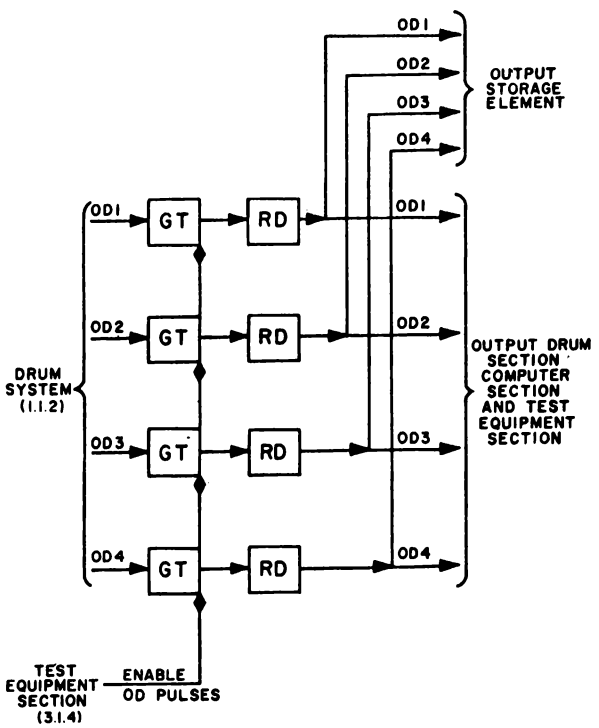


Figure 2-36. Pulse Generators (3.1.3), Block Diagram

The four gates of the OD distribution circuit are simultaneously conditioned by the enable-OD pulses d-c level. This level is produced in the test equipment section and remains up unless an error is detected during a test operation. The OD pulses are passed. through the gates and register drivers and then distributed to the output storage element, the output drum section, the output computer section, and the output test equipment section.

c. 91-PPS Generator

Refer to Figure 2-38.

The 91-pps generator contains a tuning fork oscillator, a Schmitt trigger, and a pulse generator (Figure 2-38). The 91-pps generator tuning for oscillator is tuned to 364 cps which is a multiple (4th Harmonic) of the desired frequency of 91 pps. The

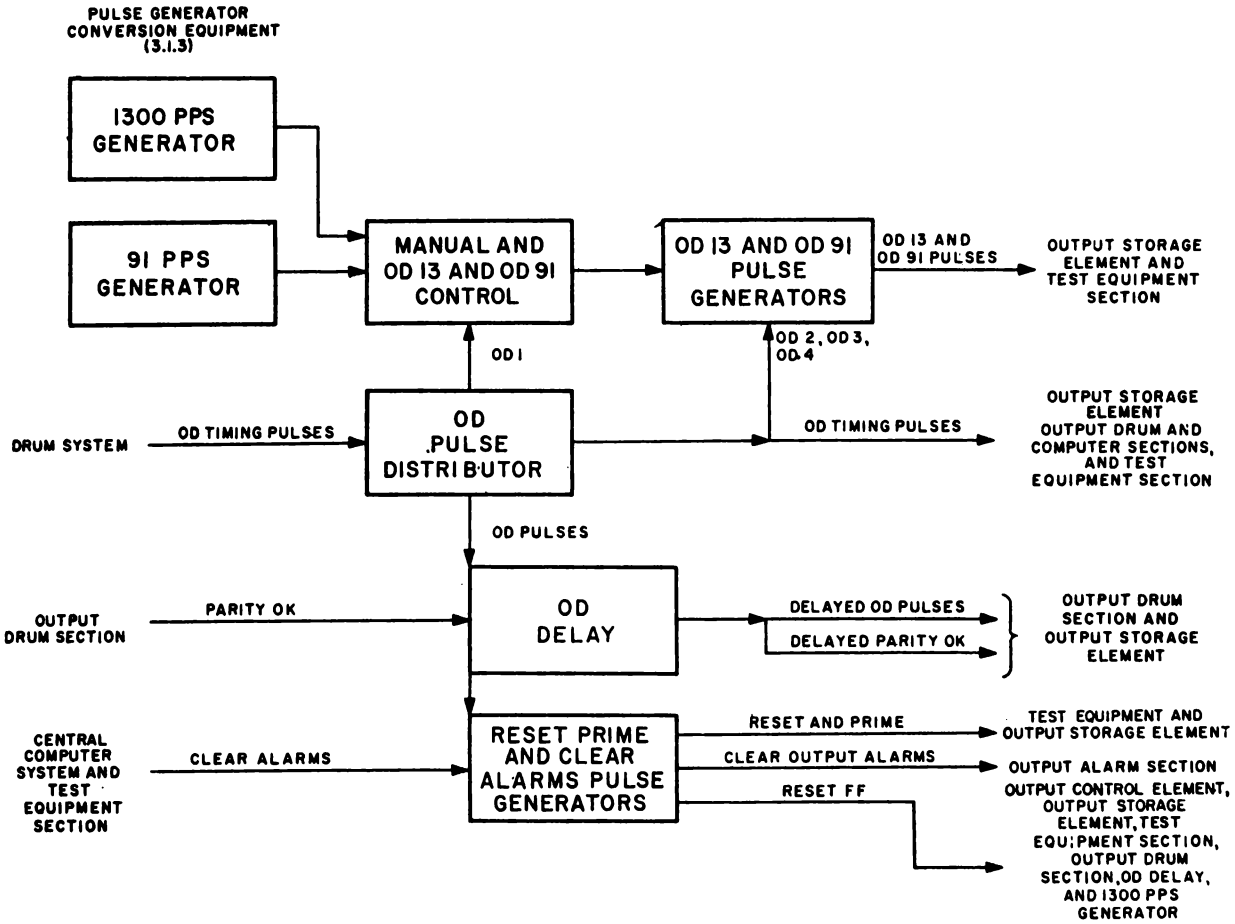


Figure 2-37. OD Pulse Distributor (3.1.3), Simplified Logic Diagram

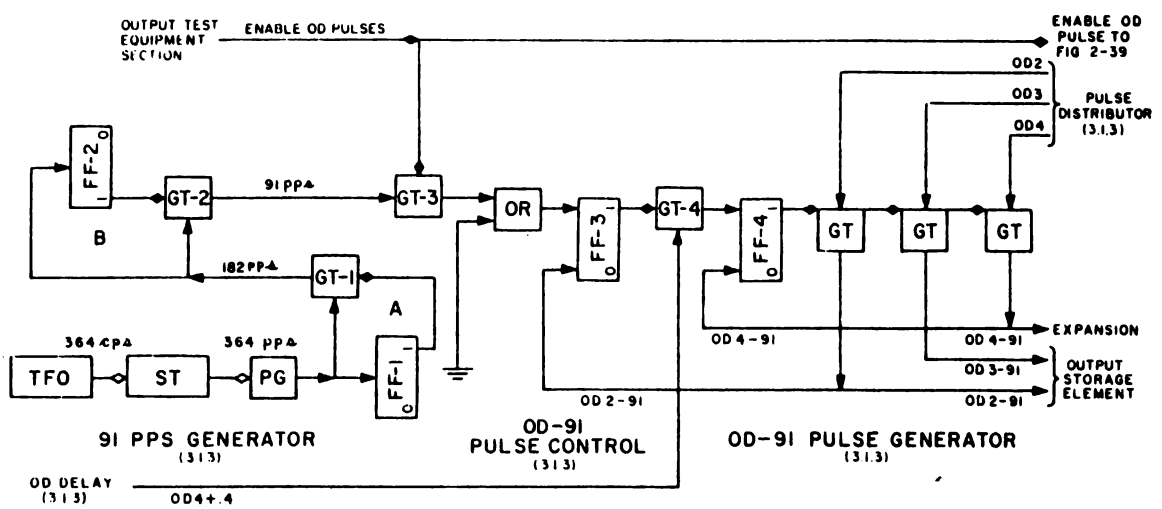


Figure 2-38. 91-PPS Generator, OD 91 Control, and OD 91 Pulse Generators (3.1.3), Simplified Logic Diagram

output of the oscillator is a sine wave which is fed to the Schmitt trigger. This circuit generates a trigger pulse for each cycle. These trigger pulses are fed to the pulse generator which generates pulses at the rate of 364 pps. Two divider circuits are then used to step down the tuning fork oscillator frequency. Each divider circuit is composed of a flip-flop and a gate. (See Figure 2-38.) Pulses occurring at the rate of 364 pps are applied to frequency divider A as complementing signals. This results in frequency divider A producing output pulses at the rate of 182 pps which are then applied to frequency divider B. The final result is the desired output of 91 pps which is sent to the OD 91 pulse control circuit. The detailed method by which the frequency is brought down to 91 pps is as follows: Assume that initially FF 1 and FF 2 are both cleared (the 0 side up). When the first 364 pps pulse arrives, it cannot pass GT 1, since this gate is not conditioned. However, this pulse will set FF 1, conditioning GT 1. When the second 364-pps pulse arrives, it passes through the now-conditioned GT 1. The pulse cannot pass through GT 2, since FF 2 is clear at this time, but it does set FF 2, conditioning GT 2. Also, this second pulse clears FF 1. The third 364-pps pulse cannot pass GT 1 since FF 1 was cleared by the second 364-pps pulse.

However, the third pulse again sets FF 1. During this time, FF 2 has remained with its 1 side up. Therefore, when the fourth 364-pps pulse is applied, both gates are conditioned because both flip-flops are set, so the pulse passes through both gates. At the same time, this fourth pulse resets both flip-flops to their clear sides which the original condition assumed. The action repeats continuously, one pulse passing GT 2 for every four pulses applied to GT 1. It follows that the 364-pps pulses are reduced to 91-pps (1/4 of 364) at the output of GT 2. The following chart summarizes the action.

364 PPS Pulse No.	GT 1	FF 1	GT 2	FF 2
Original State		0		0
1		1		0
2	Pulse	0		1
3		1		1
4	Pulse	0	Pulse	0

d. OD 91 Pulse Control Circuit

The OD 91 control circuit (Figure 2-38) controls the synchronizing of the 91-pps signals with OD timing pulses. The 91-pps signals, when synchronized with OD pulses, are referred to an OD 91 pulse. Means are provided to control the generation of the pulses in the OD 91 control circuit.

The 91-pps pulses are fed to GT 3 which is conditioned by a d-c level (enable-OD pulses) from the test equipment section. The enable-OD pulses level remains up during normal operating conditions and may be brought down only during unit loop test. During normal operation, the 91-pps pulses then pass through a series of logical circuits, are synchronized with OD 4 + 0.4 timing pulses, and produce output

pulses at GT 4 occurring at the rate of 91 pps (OD 4 + 0.4-91). That is, the output pulses are OD 4 + 0.4 pulses occurring at the rate of 91 pps. The logical circuit consists of FF 3 and GT 4. The 91-pps generator produces pulses at a rate of 91 pps. A pulse is applied to the 1 side of FF 3 which brings its 1 side up. This conditions GT 4 which passes an OD 4 + 0.4 pulse. However, before the next OD 4 + 0.4 pulse is applied to GT 4, the clear pulse at time OD 2-91 clears FF 3, deconditioning GT 4. An OD 4 + 0.4 pulse will not be passed through GT 4 until the next 91-pps pulse arrives to condition GT 4. Hence, it follows that GT 4 passes OD 4 + 0.4 pulses at the rate of 91 pps. These pulses are called OD 4 + 0.4 - 91 pulses.

e. OD 91 Pulse Generator

The TTY output storage element requires controlling pulses occurring at the rate of 91 pps. It is further required that these pulses be provided in three groups:

(1) 91 pps synchronized to occur at OD 2 time (OD 2-91).

(2) 91 pps synchronized to occur at OD 3 time (OD 3-91).

(3) 91 pps synchronized to occur at OD 4 time (OD 4-91).

The above pulses are synchronized in the OD 91 pulse generator (Figure 2-38).

Each OD 4 + 0.4-91 pulse is applied to the OD 91 pulse-stop flip-flop (FF 4), causing a level to be generated which conditions a series of gates. The result is the generation of the desired OD 2-91, OD 3-91, and OD 4-91 pulses. Every OD 2-91 pulse is sent back to the OD 91 pulse control circuit as a clear pulse, as described before. The OD 4-91 pulse clears the pulse-stop flip-flop so that only one series of OD pulses will pass through the gates for each start-OD 91 pulse applied to FF 3. Synchronized OD 2-91 and OD 3-91 pulses are fed to the output storage element.

f. 1,300-PPS Generator

The 1,300-pps generator makes up the pulse generator conversion unit and consists basically of a tuning fork oscillator, a zero detector, and a flip-flop. (See Figure 2-39. The tuning fork oscillator also feeds 1,300 cps to the output storage section which uses this signal as a continuous 1,300-cps timing signal.

The output of the tuning fork oscillator is a continuous 1,300-cps sine wave. This signal is fed to a data conversion receiver (DCR) which functions in this circuit as a zero detector. Under this condition, the zero detector provides a pulse every time the sine wave passes through zero degrees in a positive-going direction. Hence, it provides continuous pulses at 1,300 pps. These pulses are applied to the 1 side of the FF 1. The flip-flop converts the negative pulses from the zero detector to the standard positive level required to condition GT 1. Flip-flop 1 is reset by an OD 2-13 pulse from the OR circuit. The flip-flop can also be cleared by the reset flip-flops or start pulse at the OR circuit. This is done when power is first supplied to the system or when a test is started.

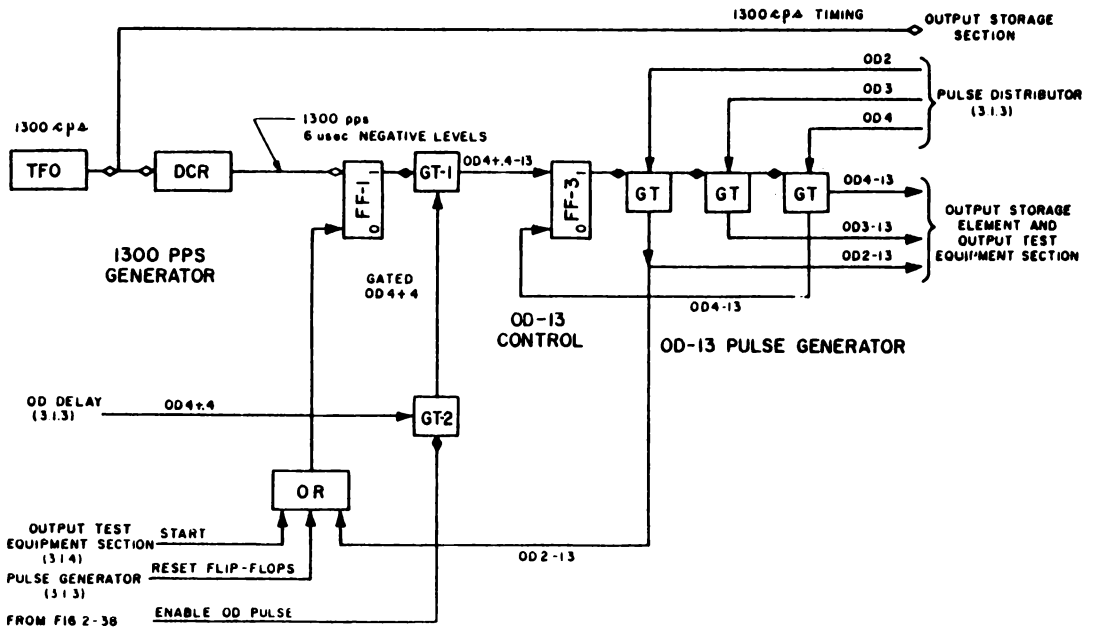


Figure 2-39. 1,300-PPS Generator, OD 13 Control, and OD 13 Pulse Generator (3.1.3), Simplified Logic Diagram

g. OD 13 Pulse Control Circuit

The OD 13 control circuit (Figure 2-39) functions similarly to the OD 91 control circuit described previously. The OD 13 control circuit controls the synchronizing of the 1,300-pps signals with OD timing pulses.

The 1,300-pps pulses cause GT 1 to be conditioned by FF 1 at a rate of 1,300 times per second. A gated OD 4 + 0.4 pulse is applied to this gate. The gated OD 4 + 0.4 pulse is present as long as GT 2 is conditioned by the enable-OD-pulses level, which is the case during all normal operations. The enable OD pulse may be brought down only during a unit loop test.

The OD 4 + 0.4 pulse is passed by GT 1 only when the gate is conditioned. Since the OD 2-13 clear pulse resets FF 1 after an OD 4 + 0.4 pulse is passed by GT 1, this gate does not pass another OD 4 + 0.4 pulse until FF 1 is again set by the 1,300-pps signal. Since this action takes place at a rate of 1,300 times per second, GT 1 passes OD 4 + 0.4 pulses at a rate of 1,300 pps. These pulses are called OD 4 + 0.4-13 pulses.

h. OD 13 Pulse Generator

By comparing Figures 2-38 and 2-39, it can be seen that the OD 13 pulse generator operates similarly to the OD 91 pulse generator.

i. OD Delay

In order to perform their functions in proper sequence, sections of the output control and output storage elements require pulses that occur between OD pulses. These delays are essential to the output control element where the delayed pulses initiate, in correct sequence, the parity count and certain read-in operations. A delayed pulse is also required for proper operation of the completed message shift register in the G/G and G/A-TD storage sections. These delayed pulses are produced by passing the OD pulses through delay circuits and their associated delay drivers (Figure 2-40). The delayed pulses are then distributed to the test parity generator, the half-write current generator, the read-in control, and the pulse generators, all of which are located in the output control element, and to the completed message shift register in the output storage element.

j. Reset Flip-Flop, Reset and Prime, and Clear Alarms Pulse Generators

Prior to and following each test operation, reset flip-flop and reset-and-prime pulses are applied to the output storage element, and to other circuits of the Output System. These pulses are produced as shown in Figure 2-41. The generation of these pulses is controlled by either of two pushbuttons, one located in the test equipment section and the other at the maintenance console of the Central Computer System. The reset flip-flop levels thus produced trigger the respective pulse generators which produce a reset flip-flop pulse. This pulse is sent to the output storage element, the output control element, the test equipment section, the write flip-flops, the set pulse flip-flop, the burst-time counter, and the 1,300-pps generator. It is also applied to a series of flip-flops and gates whose output is the reset-and-prime pulse which is sent to the output storage element and test equipment section.

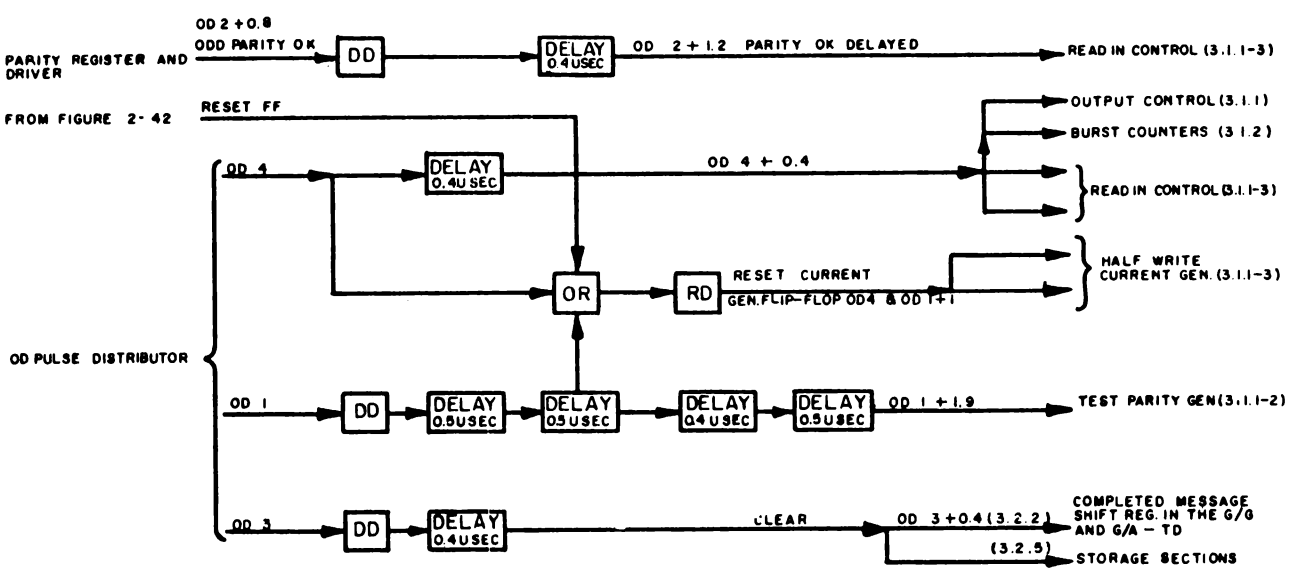


Figure 2-40. OD Delay (3.1.1), Simplified Logic Diagram

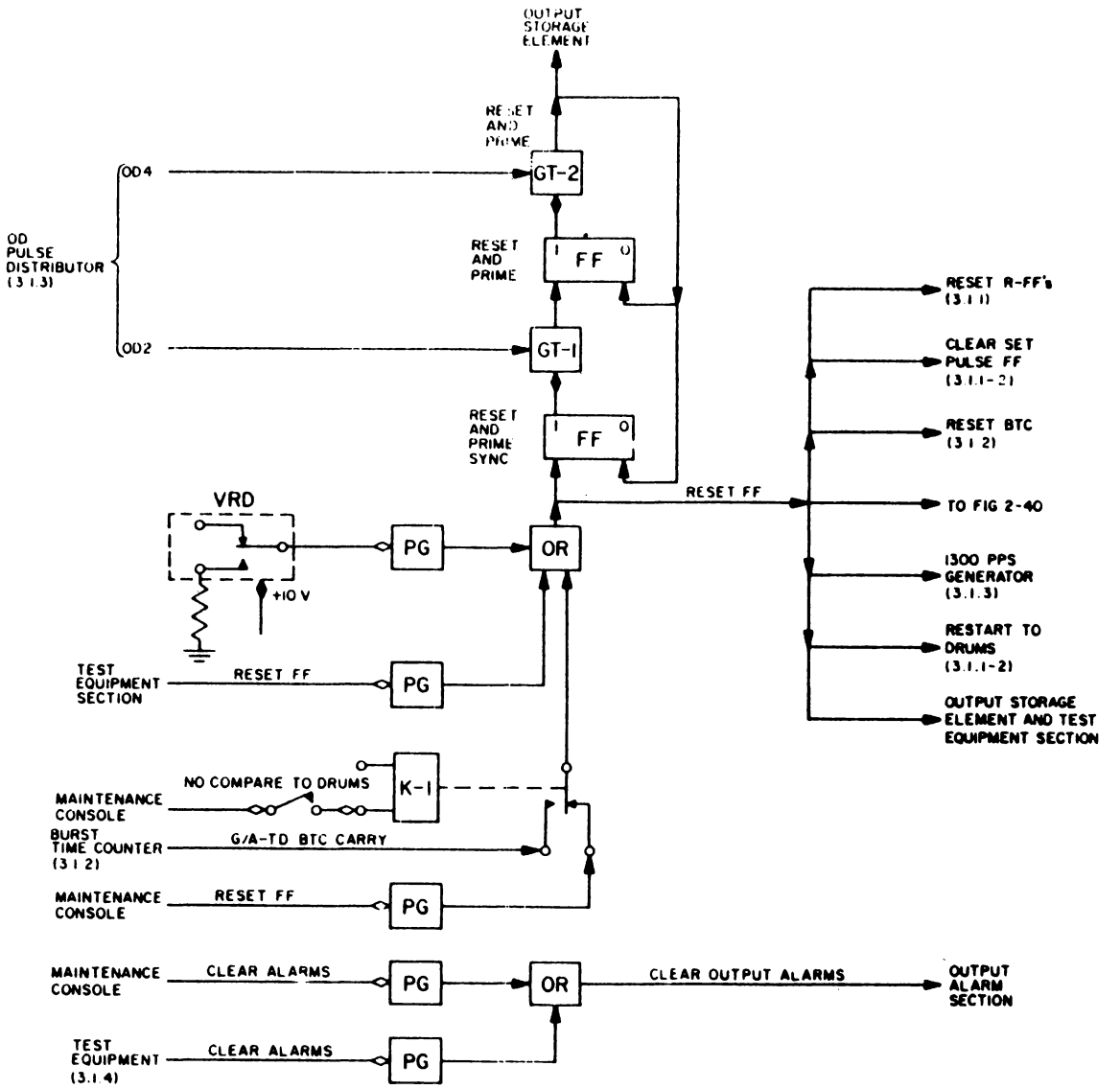


Figure 2-41. Reset Flip-Flop, Reset-and-Prime, and Clear-Alarms Pulse Generators (3.1.3), Simplified Logic Diagram

A reset flip-flop pulse is also produced by the vacuum tube relay driver (VRD) and its associated pulse generator. The VRD operates a relay which causes the pulse generator to produce a pulse when the power to the system is turned on. This ensures that the flip-flops are cleared at the start of operation. Provision is made at the maintenance console for clearing output alarm indications at the alarm display.

k. Reset Drum Status Bit Generator

The reset drum status bit generator circuit shown in Figure 2-42 is used during a test operation to restore drum status bits into the drum status channels of the three OB drum fields, thereby causing data information stored on the drums to be retained following a drum readout cycle. This function is particularly desirable for testing the Output System in that a program is stored and retained on the drums where it can be read out repeatedly, without the intervention of the Central Computer, to test individual storage sections of the Output System.

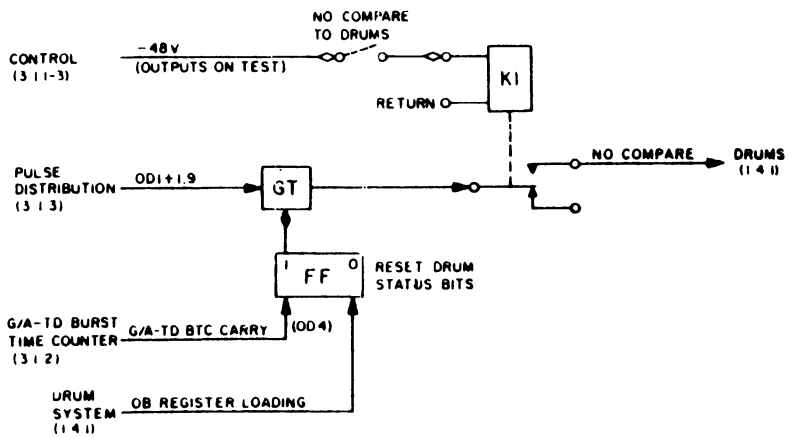


Figure 2-42. Reset-Drum Status Bits Generator, Simplified Logic Diagram

This test function is accomplished by activating the NO COMPARE TO DRUMS switch to energize relay K1 shown in Figure 2-42. Following a drum readout cycle of the three OB drum fields, and at the completion of the G/A-TD burst counter cycle, a burst time carry (BTC) pulse (OD 4) is generated to set the reset drum status bit flip-flop. This BTC pulse is generated at the completion of the G/A-TD burst time counter cycle or every 23 seconds (256 x 90 ms or 128 x 180 ms). Since the G/A-TD BTC cycle is longer than the BTC cycles of the other storage sections, a complete search of the drums occurs in the 23-seconds cycle. All words will have been read; therefore, all the drum status bits will be in the zero state.

The reset drum status bit flip-flop, when set by a BTC pulse, remains in this state for a period of 60 ms. In turn, a gating level is applied to GT 1 which is normally strobed by OD 1 + 1.9 pulses. The latter are passed by the conditioned gate for 60 ms and routed through the closed contact points of energized relay K1 as no-compare pulses to the Drum System. Sufficient time is provided, therefore, to allow the reset drum status bit generator, to write 1's in the status channels associated with the three drum fields of the OB drum (20 ms per field). This causes the drum test data to be retained on the drums in preparation for a subsequent drum readout cycle and without further intervention from the Central Computer.

In general, programs used for this particular test function are written so that a burst-time count equal to zero is never included in the program. Accordingly, the generation of a non-search alarm is prevented. In addition, prior to the test function and loading of a program on the drums, the OB drums should be erased and placed in a COMPUTER TEST mode. Following the loading of the program on the drums, the drums are placed in the OPERATE mode. This action prevents the drum status channels from being restored to the 1 state while a program is being loaded on the drums. If the program does not fill all available drum addresses, all zero words will be sent to the Output System. This will cause a drum parity alarm and an illegal section alarm which should be disregarded for the purpose of this type of test.

Output Alarm Section

1. Introduction

It is necessary to install certain alarms in the Output System to indicate to maintenance personnel the nature of errors which may develop within the system. It is the function of the output alarm section to store the status of the alarms and to display their status by means of neon indicators. The alarms which are provided are the nonsearch comparison, G/G, G/A-TD, TTY, parity-NG, illegal address, illegal section, and lost parity.

The output alarm system displays other conditions, as shown in Figure 2-43. The contents of the output drum section flip-flop register, some of the OD pulses, distributed by the output computer section, and the various test pulses are also displayed by neon indicators. Besides this, indicator lamps are included to display certain test operations.

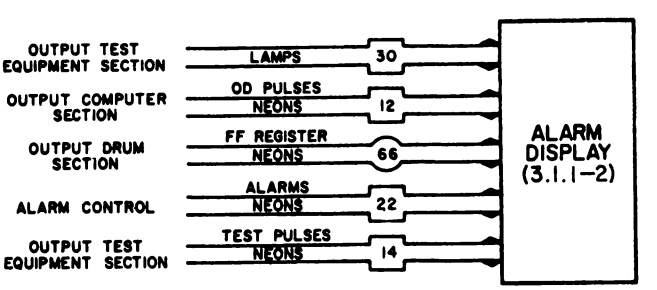


Figure 2-43. Output Alarm Section, Block Diagram

The nonsearch comparison alarm is generated when a word on the OB drum is read into the flip-flop register with the proper burst number for the section to which it is addressed; but the word arrives during the nonsearch period of the current burst. In this case, conditions are such that this word can never be accepted from the drum because the nonsearch period is the last part of any given burst period and the burst number changes before another search period can occur. Thus, the word will be lost (erased).

The G/A-TD, G/G, or TTY alarm is generated when its storage parity is bad. The parity NG alarm is generated when the parity of the word received in the OB register is bad. The illegal address or illegal section alarm occurs when the storage register address or the section address contained in the left half-word of the OB register has not been assigned to an actual section or register within the Output System. The lost parity alarm is generated when a parity check on the word in the OB register is not initiated or completed.

The output alarm section is broken down into two parts: the alarm control and the alarm display. (See Figure 2-44.)

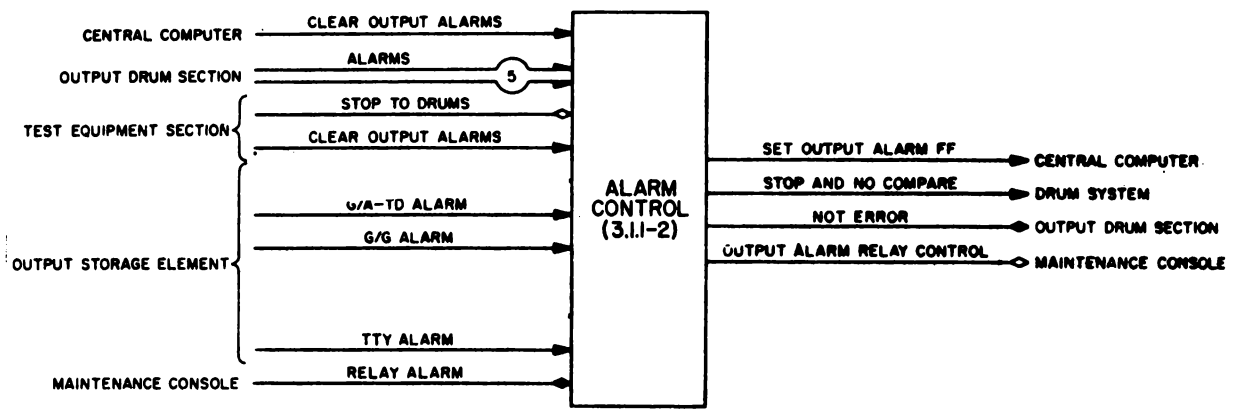


Figure 2-44. Alarm Control Block Diagram

2. Alarm Control

The statuses of the various alarms are stored within the alarm control. (See Figure 2-45.) One flip-flop is provided for each alarm. The 1-side indicator neon of each flip-flop is located in the alarm display unit.

The 1 outputs of all the alarm flip-flops are sent through an OR circuit to a VRD, the relay of which continually sends to the maintenance console in the Central Computer System indication of whether there is an output alarm. These two signals activate indicator lights on the maintenance console. The 0 sides of the illegal address, illegal section, parity NG, and lost parity alarm flip-flops are fed to an AND circuit.

The output of this AND circuit feeds one leg of a 2-way OR circuit. The other leg of the OR circuit is connected to either +10v or -30v, depending on the status of the STOP TO DRUMS relay. In normal operation, this relay will be de-energized, thus supplying +10v through its N/C contacts to the OR circuit. Therefore, the output of the OR circuit generates a NOT ERROR level; this is always +10v during normal operation. This level is used to condition a gate tube in the OB register reset control circuitry. When the gate tube is conditioned, the resetting of various flip-flops in the Output System, in addition to the OB register flip-flops, is affected in the normal manner. It is

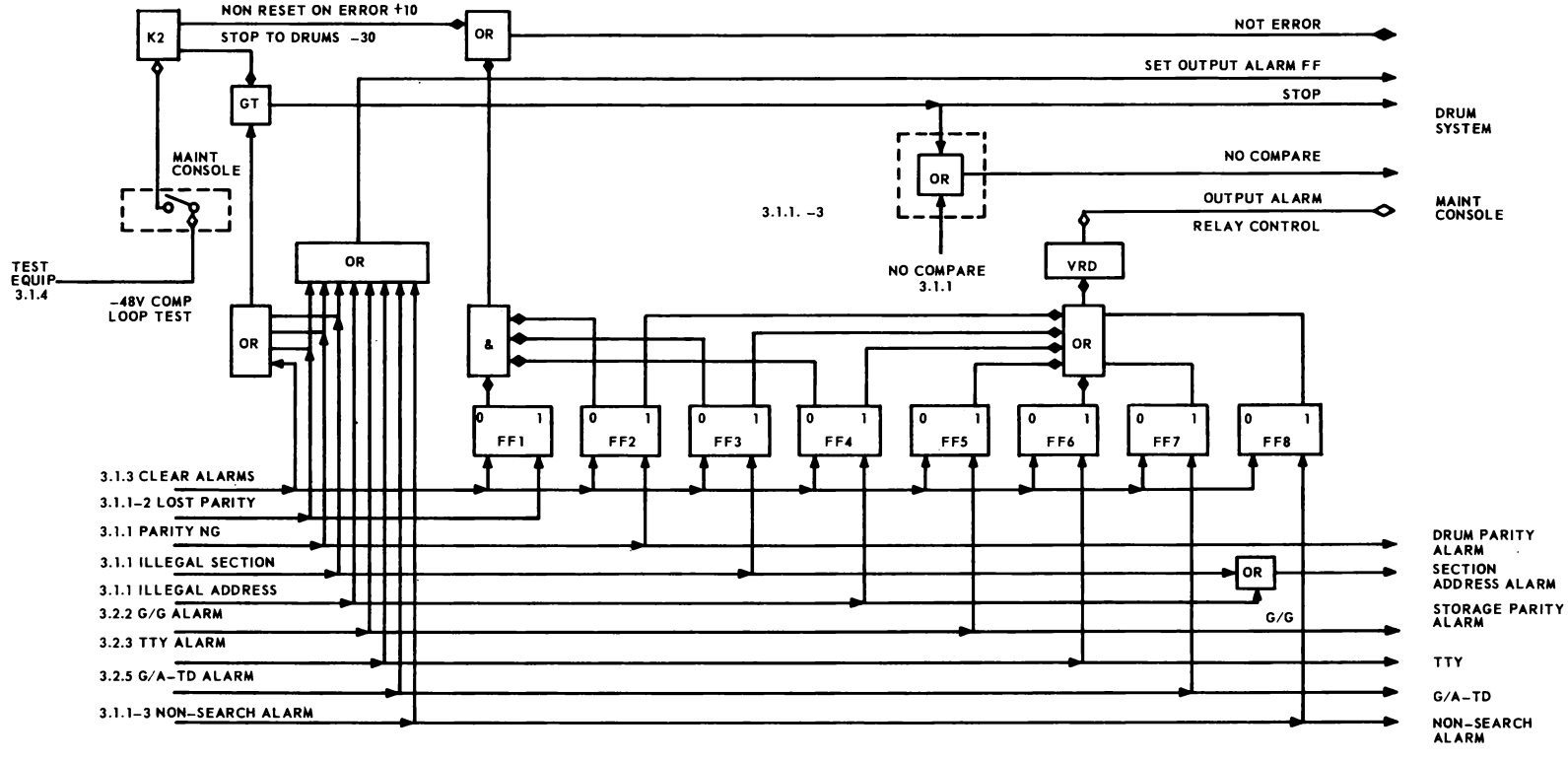


Figure 2-45. Output Alarm Control (3.1.1-2), Simplified Logic Diagram

sometimes desired, during computer loop test, to have the operation of the Output System halt, when an error is incurred, and to inhibit the resetting of the various flip-flops, particularly the OB register flip-flops. Thus, the word that caused the error is retained in the register for examination. This is accomplished by the STOP TO DRUMS switch on the duplex maintenance console which controls the STOP TO DRUMS relay mentioned previously. When the switch is activated, -48v is supplied from the test circuitry through the switch to energize the STOP TO DRUMS relay. With the relay energized, -30v is fed to one leg of the OR circuits which supply the NOT ERROR level. Therefore, the NOT ERROR level will now be dependent upon the status of the illegal address, illegal section, parity NG, and lost parity alarm flip-flops. If one of these flip-flops is set as a result of an error, no level (NOT ERROR) will be present at the gate, deconditioning the gate tube which passes the reset pulse. Therefore, the contents of the OB register may be examined to determine the cause of the error.

The parity-NG, illegal-address, illegal-section, and lost-parity pulses are also fed through an OR circuit to a gate. When this gate is conditioned by a stop-to drums signal from the test equipment section, a stop pulse is transmitted to the Drum System and to the read-in control unit. When an error occurs here, the stop pulse or a no-compare pulse passes through an OR circuit and goes to the Drum System. The puspose of the stop pulse during the test procedure is to inhibit the transfer of data from the OB drum to the Output System, to prevent the erroneous word in the drum register from being erased, and to hold the operation of the Output System so that the error can be examined.

The alarm pulses from the various sections also cause a set-output-alarm-synchronizing flip-flop signal to be sent to the Central Computer System. This flip-flop is used by the Central Computer System to sense an output alarm. The alarm pulses from the various sections also go to a group of OR circuits. An output parity alarm is generated if parity does not check out in any of the six output sections. A nonsearch alarm, drum parity alarm, or a section or register alarm is generated if any of these conditions do not check out. These alarms are used in the Central Computer System.

3. Alarm Display (Note: Refer to Figure 2-46)

The purpose of the alarm display is to indicate to maintenance personnel any malfunctioning of the Output System. The alarm displays (Figure 2-46) are on the indicator and test control panel located on the test door on the back of output control unit 42. Neon indicators on the panel indicate the statuses of the Output System alarms. Neon indicators are also provided for various registers within the Output System. Among the quantities represented in the alarm display are the contents of the drum word flip-flop register and certain of the timing pulses. Also represented in the alarm display of neons and lamps are various control functions used in testing the Output System.

Note in Figure 2-46 that there are two neon tubes associated with each display. Only the 1 neon is on the display panel and is read. If it is on, it indicates a 1 bit; if it is off, it indicates a 0 bit. The other neon is used to cut off the firing of the 1 neon when the 0 side of the flip-flop is up (+10v) since, at this time, the 1 side is down (-30v). In order to cut off the firing of the 1 neon when the 1 side is down (-30v), the 0 neon is included. This neon fires when the 1 side is down and effectively shorts out the voltage across the 1 neon. If the 0 neon were not included, a rather complex circuit

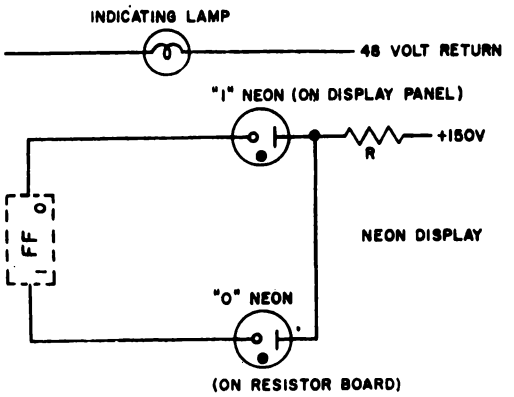


Figure 2-46. Alarm Display (3.1.1-2), Simplified Block Diagram

would be necessary to cut off the firing of the 1 neon when the 1 side of the flip-flop goes from up to down.

SUMMARY QUESTIONS

1. A group of words which are used to make up the output message is called a _____ .

2. Why is a Parity NG and a Parity OK pulse used to check for any errors?

3. Why is there an alarm for each section plus others?

4. The drum word stays in the OB Register for_____ approximately.

5. Under what circumstances is a no-compare pulse generated?

6. What is the purpose of the no-compare pulse?

7. There are_____illegal section addresses.

8. The illegal register addresses for the following sections are:

   a. G/G =

   b. TTY =

   c. G/A-TD =

9. Which Output Register Addresses are illegal for all sections?

10. What is the function of $_{C}$SS in P.U. 42 AY? (3.1.1-2) (2B)

11. All storage sections, except G/A-TD use _____ parity for the output word.

12. A nonsearch alarm for any section, i.e., G/A-TD, G/G, etc., indicates a good word was received during nonsearch time. T/F

13. The burst-count selecting counter is cleared by a _____ or a _____ pulse.

14. The burst time counts that are transferred to C.C. are transferred in what order?

15. How many BTC's are there?

16. What could cause the following alarms?

a. G/G

b. TTY

c. G/A-TD

The following questions will refer to the Output Logic.

17. Logic 3.1.1 (3B) open line at 42AVC1. What malfunction could occur?

18. Logic 3.1.1-2 (14A) open line at 42AXA3. What malfunction could occur?

19. Logic 3.1.1 (12D) if P.U. 42CR had an open line at pin J7. What malfunction would occur?

20. Logic 3.1.1-3 (18C) open at edge connector 42CD3g will result in what malfunction?

21. Logic 3.1.2 (16D) if 42DDC5 is open, what would result?

22. Refer to Logic 3.1.2 42DN A2 open. What will be the Burst counts transferred for G/A, G/G, and TTY. Assuming G/A BTC = 32_8, G/G BTC = 174_8, and TTY BTC = 6_8.

23. 42DFF2 is open on 3.1.2. The G/A-TD BTC = 70_8 G/G BTC = 141_8, and the TTY BTC = 27_8. If all three burst counts are read by the computer, what numbers will be transferred?

24. Given the following program, what addresses in core memory will contain the G/A-TD BTC, G/G BTC, and TTY BTC after halting?

a. SEL (21)--------

b. LDC 1006

c. RDS 5

d. LDC 1005

e. RDS 3

f. LDC 1004

g. RDS 1

h. HLT ----

CHAPTER 3. OUTPUT STORAGE ELEMENT, DETAILED ANALYSIS

1. General

Data processed by an AN/FSQ-7 Combat Direction Central is made available to associated components of the Air Defense Command sector through the Output System and commercial telephone line facilities. Information enters the Output System from the Drum System at a relatively high rate of speed. By temporarily storing this information, the output storage section of the output system slows down the rate of transmission to a frequency that is compatible with commercial telephone line equipment.

Output data is classified into three general categories: ground-to-air time division (G/A-TD), ground-to-ground (G/G), and teletype (TTY). G/A-TD data is utilized by airborne interceptors; G/G data is intended for adjacent centrals, higher headquarters, missile control, and height-finder radars. Among the possible uses for TTY data are crosstelling to nonmechanized adjacent sectors crosstelling to higher headquarters, and the feeding of early-warning data directly to antiaircraft gun batteries.

The output storage element is divided into three sections to accommodate the three general categories of output data now being used. (See Figure 3-1.) Provision is made, however, for possible future expansion of the output storage element to eight sections.

All information enters the output storage section through the output control element after being checked for accuracy and proper sequence. The output control element accepts words from the output buffer drum at 10-usec intervals; however, the words are distributed on the drum fields so that the smallest interval between successive words entering a storage section is 20 usec. This provides ample time for a storage section to store a word and prepare for the next incoming word.

Each storage section has its own timing and control circuits which enable it to accept words and transmit messages independently of the other sections. Synchronism with the Drum System and the output control element is achieved by using the OD drum timing pulses.

2. Bursts

Each storage section can store and then transmit more than one message simultaneously. The simultaneous transmission of all messages stored in a storage section is called a burst. The three storage sections differ in the number of messages that can be stored at one time. Therefore, the burst size of each of these sections differs. The size of each burst for each section is as follows:

Output Message	No. of Message	Output Words Per Message	Bits Per Output Word
G/A-TD	3	4	17
G/G	5	5	17
TTY	25	1	19

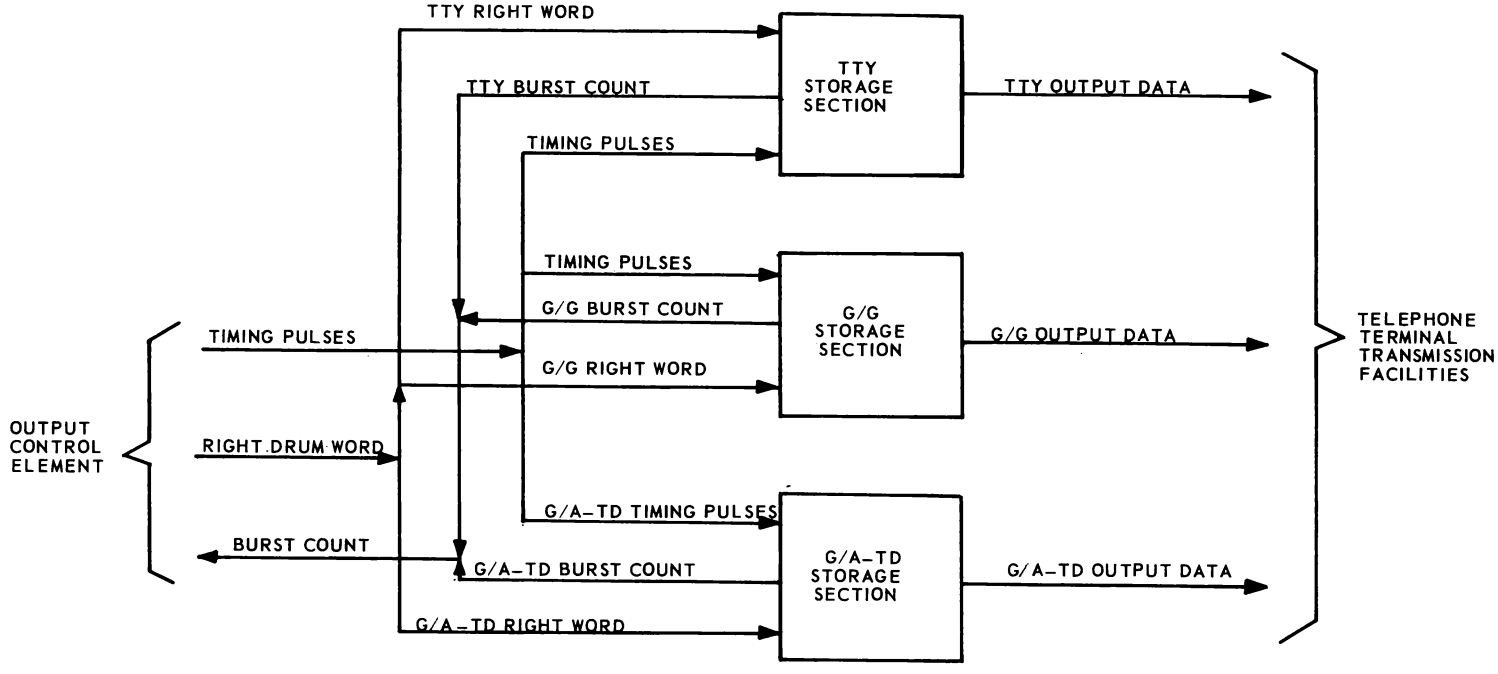


Figure 3-1. Output Storage Element, Block Diagram

An output word consists of a right half-word, a storage parity bit, and, in some cases, additional 1 bits called busy bits. Drum words containing the right half-words of messages to be transmitted during a burst are assigned the same burst number by the Central Computer System. This enables the Output System to identify the drum words for a particular burst and to ensure that only those words are accepted from the output buffer (OB) drum and subsequently transmitted during the associated burst period.

3. Burst Period

The interval during which an Output System storage section receives all messages of a specific burst and then transfers the burst to transmission equipment is a burst period. The burst periods of each of the three Output System storage sections are of different duration and occur successively. The length of each burst period is as follows:

Storage Section	Burst Period
G/A-TD (Dual Channel)	0.090 sec
G/A-TD (Single Channel)	0.180 sec
G/G	0.070 sec
TTY	0.495 sec

Each burst period is composed of search time and readout time. Search time is the only portion of a burst period during which the Output System storage section can receive the output words of a burst from the OB drum. Readout time is the interval during which the burst is transferred to transmission equipment. Since drum words containing the right half-words of a burst are written at random on the three OB fields, some drum words of a specific burst may be stored on each of these fields. To ensure that all drum words of the burst are read during search time, the minimum search interval is made equal to the amount of time required to read all three OB fields. This search interval is determined as follows: 6,108 drum word registers (2,036 per field) times 10 usec (interval between successive drum registers) plus 360 usec (120 usec per field for switching) equals 61.44 ms. Allowing for drum speed variations, search time for each burst period, except for G/A-TD, is set at approximately 65 ms. The search interval is approximately the same for two of the three storage sections. The search interval for G/A-TD is approximately 86.2 ms for dual channel operation and 176.15 for single channel operation.

G/G Storage Section (Figure 3-2)

1. General

The G/G output storage section assembles output words received in parallel form from the output control element into messages, and then transmits these messages serially over telephone data channels to specific destinations. These messages are transmitted at 1,300 pps. A simplified diagram of the G/G storage section is shown in Figure 3-3.

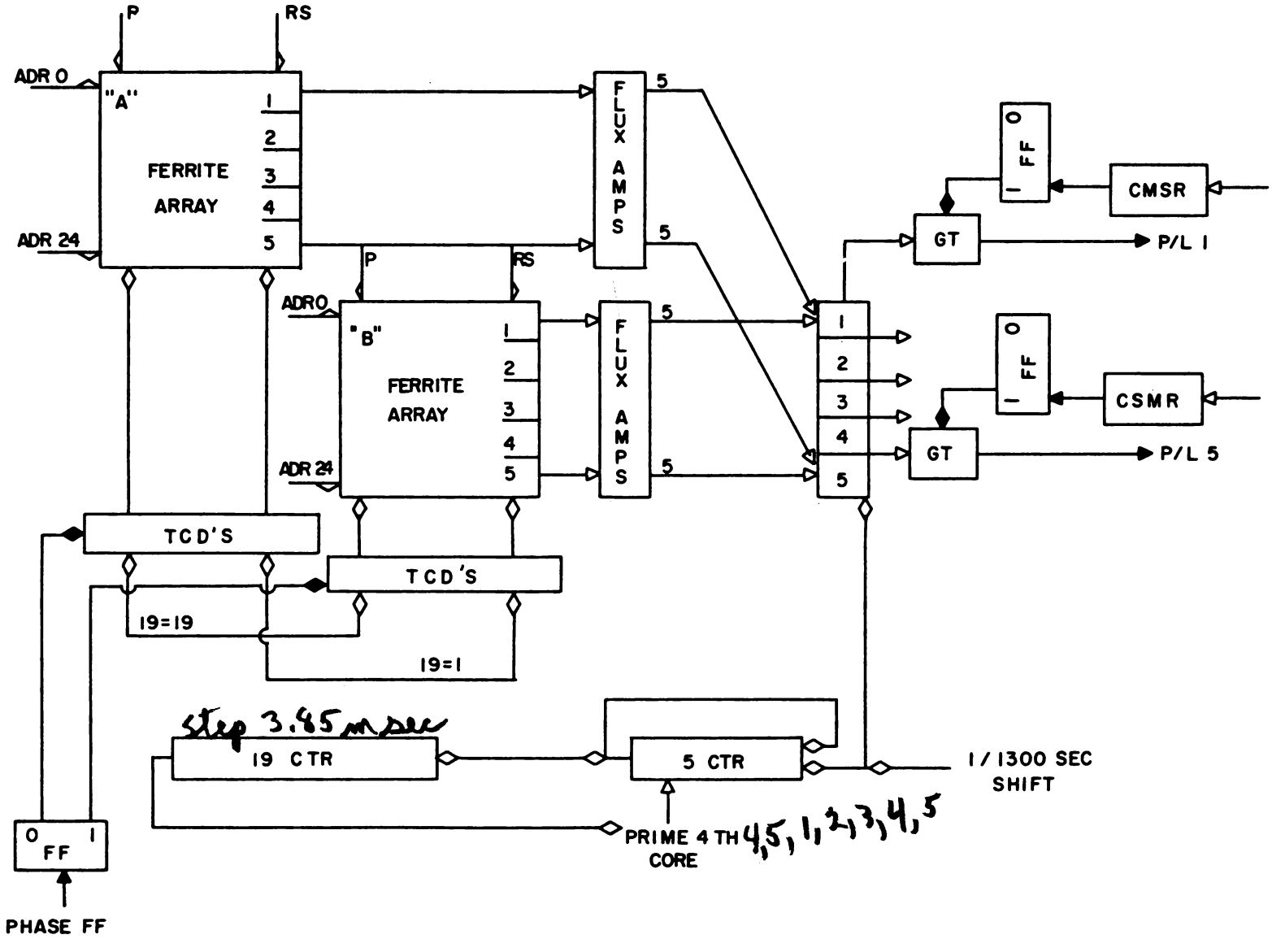


Figure 3-2. Block Diagram of G/G Storage

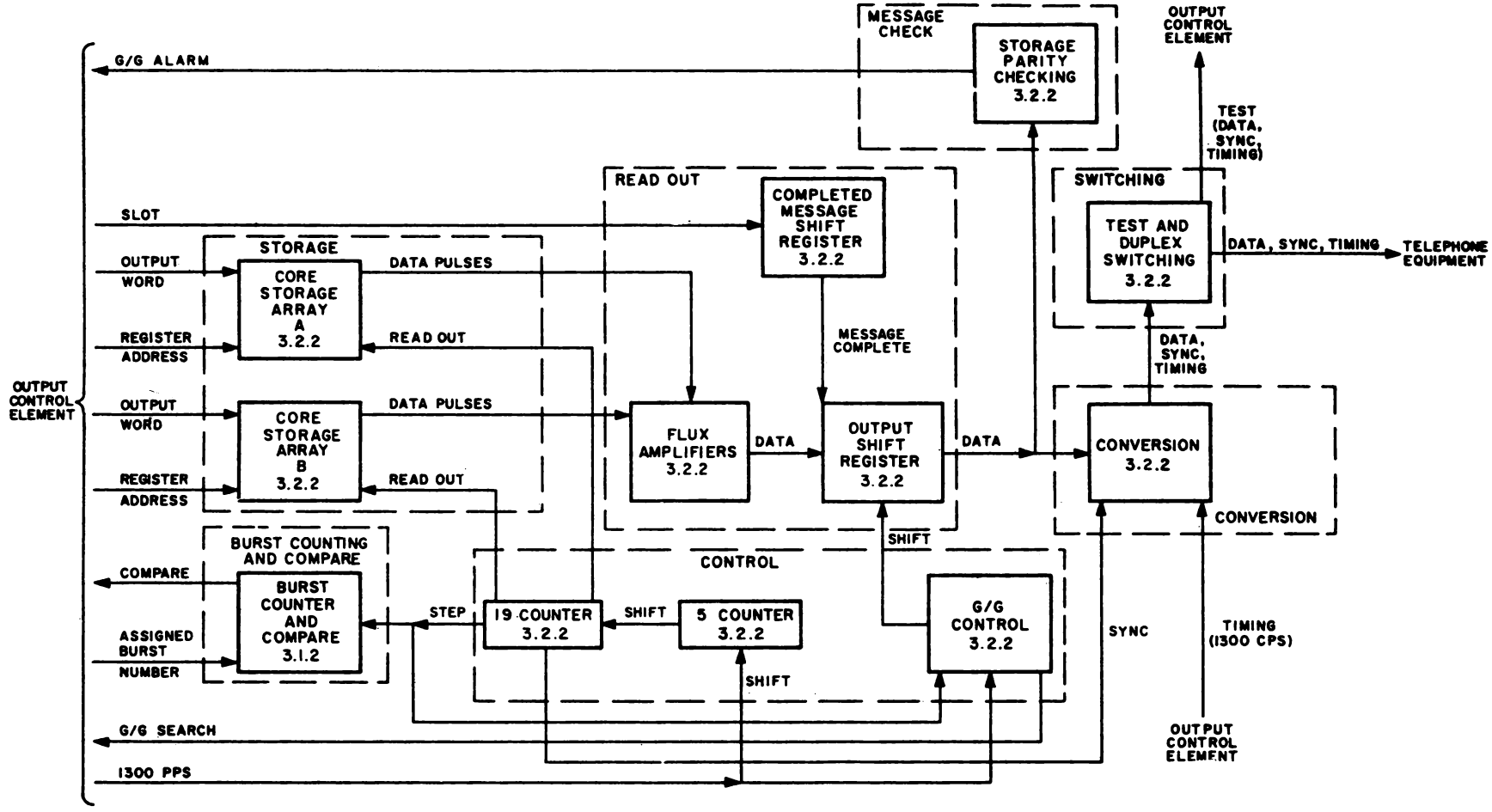


Figure 3-3. G/G Output Storage Section (3.2.2), Simplified Block Diagram

Five G/G messages may be transmitted simultaneously during each G/G burst period. Each message is composed of five output words and is transmitted over a separate telephone data channel to a specific destination. These messages are of the following types:

a. Forwardtelling messages to an AN/FSQ-8 Combat Control Central.

b. Crosstelling messages to an adjacent AN/FSQ-7 Combat Direction Central.

c. Height-finder request messages to height-finder radars at radar sites.

d. Messages to unmanned missiles through missile controls.

A parity check is performed on each output word by the site receiving the G/G message to determine whether the original contents of the output word have been altered by noise affecting the transmission channel. To ensure greater accuracy in the parity check, the output words in the G/G messages are transmitted in a serial interleaved form. The 17 bits of an output word are therefore spaced five bits apart on the telephone data channel. Refer to Figure 3-4.

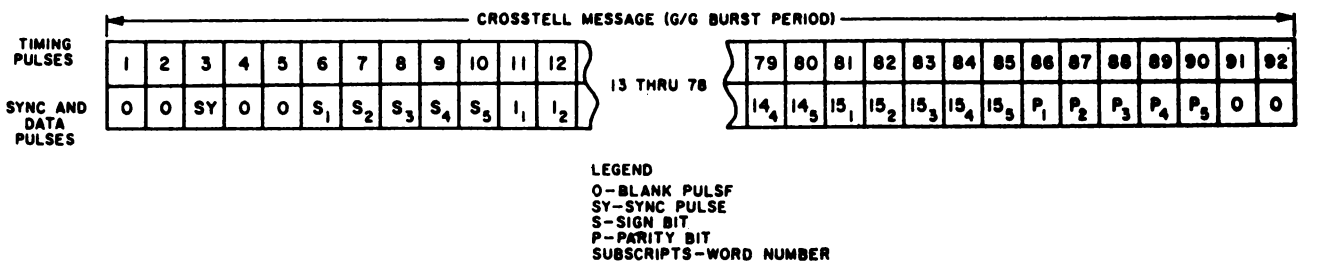


Figure 3-4. G/G Message, Serially Interleaved Form

With this manner of transmission, errors in up to five adjacent bits can be detected by the parity check. The fact that no two adjacent information bits are checked by the same parity check circuit ensures that double errors will be detected if they are in adjacent bits of the message.

The time required to read out all messages in a G/G core storage array is 70 ms. This is about equal to G/G search time which is 65 ms. To eliminate the waste of telephone line time which would result if the line were not used during search time, two core storage arrays are included in the G/G storage section. One array receives information while the contents of the second array are read out to telephone line channels. Twice as many G/G messages can therefore be sent. Since two storage arrays are employed and search time for one storage array occurs simultaneously with the readout of the other, a G/G burst period is set at 70 ms.

2. System Operation

A simplified diagram of the G/G storage section is shown in Figure 3-3. As depicted in this diagram, the G/G storage section is logically divided into the following areas:

a. Storage - the storage circuits store the five G/G messages prior to their being sent to the readout circuits.

b. Control - the control circuits initiate and control all operations of the G/G output storage section.

c. Readout - the readout circuits prepare the messages for transmission to the conversion circuits.

d. Burst counting and compare - the burst counting and compare circuits check the drum word in the output control element to ensure the correct sequence of message transmission.

e. Message check - the message check circuits check the transmitted message for errors.

f. Conversion - the conversion circuits modify the G/G messages to gated 1300 cycle sine waves for transmission over the telephone data channels.

g. Switching - the switching circuits are used to perform test functions. They are also used to switch output storage data from the telephone lines to the test equipment.

A description of the operation of the G/G storage section follows.

a. Counter Operation

The control circuits consist of the G/G control, the 5 counter, and the 19 counter. The two counters control the timing operations and operates as explained below.

The 5 counter is shifted at a 1,300-pps rate by pulses from the output control section. On every fifth shift, a 5-counter-equals-5 pulse is generated which is used to shift the 19 counter. The 19 counter repeats its counting cycle after it has been shifted 19 times. A complete G/G burst period takes place during this cycle, during which time one G/G core storage array is read into while the other is simultaneously read out.

A G/G operational cycle consisting of read-in and readout for one of the two core arrays is described in the following paragraphs. The G/G read-in interval and the readout interval for a single core array each takes place during successive burst periods. Two G/G burst periods are therefore required for the G/G storage section to complete a cycle of operations. In actual operation, the read-in and readout functions occur simultaneously; while one core array is being written into, the other array is simultaneously being readout.

b. Read-In

Each G/G burst period ends at the 1st shift of the 19 counter. At this time, the 5 counter and the 19 counter are cleared and primed. The 19-counter cycle starts with its next shift. At 19-counter-1 time, the G/G control sends a search level to the output control element and steps the BTC. This level signals the output control element that read-in can now take place. The core array which had been read out during the previous burst period is now written into. Each correct G/G output word (right half drum word bits RS through R15 plus an even parity bit) whose assigned burst number matches the contents of the G/G burst counter is written into; a pulse is sent to the completed message shift register by the control element. The completed message shift register counts the number of words loaded in each message slot in a core array. Read-in is completed before 19-counter-18 time. At this time, the G/G control generates a sync pulse, a not-search level, and a shift-phase level. The sync pulse is sent to the conversion equipment; the not-search level prevents the output control element from writing into any more core registers. The shift-phase level switches core arrays so that the array just read into will be read out during the next burst period.

c. Readout

Readout of the core array which has been written into starts at 19-counter-1 time. At this time, the 19 counter generates a clear-column-1 pulse. This pulse is sent to the core storage array where it serves to send all the information contained in the first column of cores through the FA's and into the OSR's. This information is now passed out of the OSR (as explained in the following paragraphs) only if the completed message shift register has counted five words written into that slot of the core array. This prevents transmission of the incomplete messages.

In the interval between 19-counter-1 time and 19-counter-2 time, the OSR's and the 5 counter are shifted five times. With each shift of the OSR, one bit of each of the five G/G messages is sent to the conversion circuits, to the storage parity checking circuit, and to the output control element. The output control element utilizes this information when test procedures are performed. At the storage parity checking circuit, the data is entered and later examined for errors. A G/G alarm is generated if an error is found. At the conversion circuits, the data is made compatible for transmission by the telephone data channels.

Simultaneously with the fifth shift of the 5 counter, the OSR is emptied. At this time, the 5 counter generates a 5-counter-equals-5 pulse. This pulse shifts the 19 counter, causing it to read out another column of the core storage array into the OSR. The information is then shifted out of the register in the same manner as the data from the first column. The process repeats itself until the entire message has been read out of the core array.

3. Storage

a. Core Storage Arrays

The output words comprising G/G messages are stored in rectangular ferrite core storage arrays. Each G/G output word, which is 17 bits in length, is stored in one

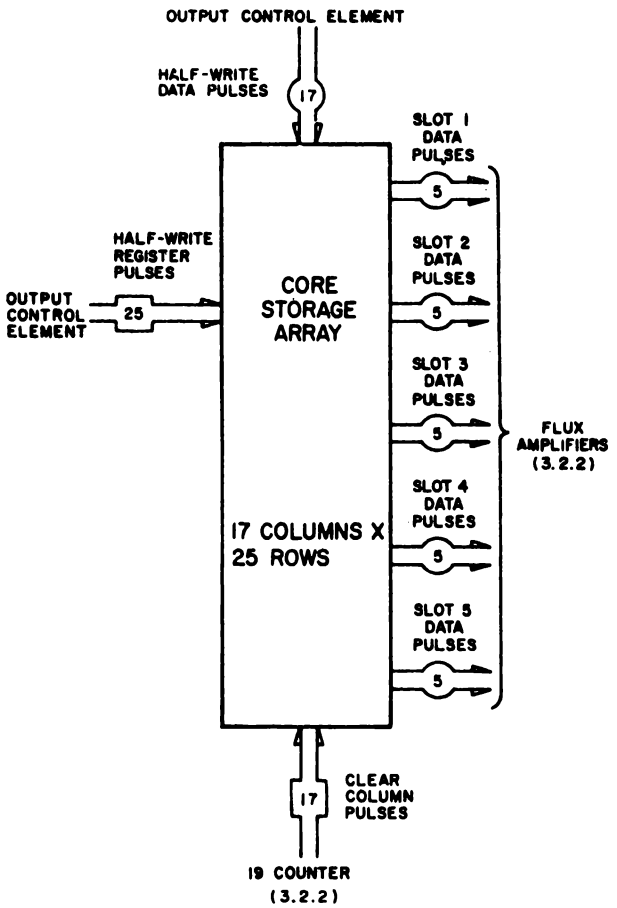


Figure 3-5. G/G Core Storage Array (3.2.2), Simplified Block Diagram

register or row of the array. The array has 17 columns and 25 rows, and can therefore store 25 output words. (See Figure 3-5.)

Two identical arrays are included to provide the most efficient use of telephone channels. Each array is written into row by row and read out column by column. Writing is done by coincident currents (See Figure 3-6.) As each word is transferred to the core storage array, a half-write current is applied to the register address winding of the row in which that word should be written. Simultaneously, right drum word half-write current pulses are applied to those column windings in which a 1 should be recorded. During readout each core in the column receives a full-read current, with each core output appearing on the corresponding row array; output winds in the two arrays are wired in parallel. (See Figure 3-7.) No interference between matrices results since only one array is read out at a time through use of gated TCD's.

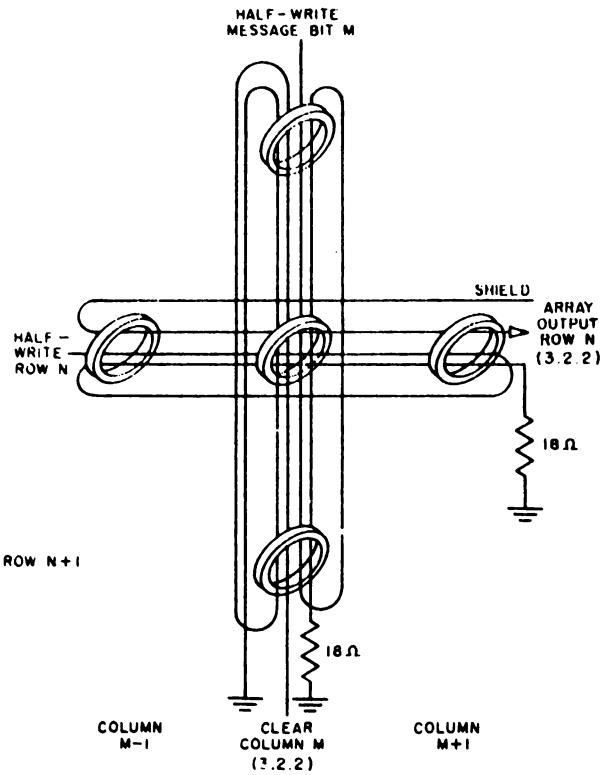


Figure 3-6. Portion of G/G Core Storage Array (3.2.2), Simplified Diagram

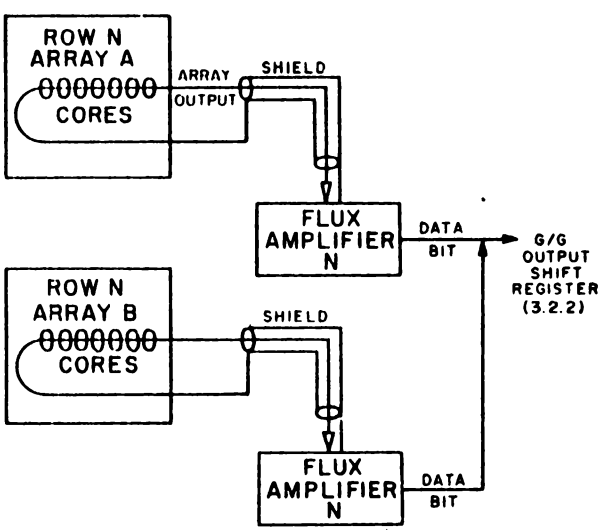


Figure 3-7. Output Wiring of G/G Core Arrays A and B, Simplified Diagram

b. Core Array Read-In

During each burst period, G/G message words are written into the core storage array which is not being read out. The right drum word with its even parity bit is applied by the output control element to the core storage array as half-write pulses on those drum word lines whose bits are 1's.

The row in the array on which the word is written is specified by the register address contained in the left drum word. Thus, message assembly is accomplished by the assigned burst number and the register address. Since the search period for the OB fields is approximately 65 ms, read-in to one array can be completed during the 70-ms readout time for the other array.

The selection of an array for read-in is accomplished by the output control element. The G/G control supplies that element with information on which array is being read out. The output control element, in turn, routes words for read-in into the other array.

4. Control

a. General

While many of the control functions of the G/G output storage section are managed by the output control element, certain functions unique to the section are managed by control circuits within the section. These control units include the 5 counter, the 19 counter, and the G/G control.

b. 5 counter

The 5 counter, shown in Figure 3-8, is a 5-core ring counter which is cleared, primed, and then continuously stepped at 1,300 pps. The outputs from this counter are used in performing test operations and controlling functions of the storage section. The operation of the 5 counter follows.

At the start of system operation or after a shutdown or test operation, the output control element sends an OD 4 reset and prime pulse to the 5 counter and the G/G control. This pulse and the following OD 3 pulse cause a 7.5 usec shift pulse to clear the 5 counter. The G/G control then primes the 5 counter by entering a 1 in its fourth core. Generated by the flip-flop for each combination of an OD 2-13 and OD 3 pulse applied to it, 5-counter shift pulses shift this 1 through the counter. As the 1 is shifted out of the fifth core, it is transferred to the first core. From this point until the end of the burst period, the 5 counter maintains a continuous serial count of each group of five shift pulses.

As the 1 is transferred from one core to another, a 5-counter-equals pulse is generated. The 5-counter-equals-1 through 5-counter-equals-5 pulses are sent to the test equipment section. The 5-counter-equals-5 pulse is also used to condition a gate which is pulsed by OD 3-13 timing pulses. At 5-counter-5 time, an OD 3-13 pulse is passed by the gate and sent to the G/G control (Figure 3-10) as a 5-counter-equals-5 pulse. This pulse is used to generate a 19-counter-shift pulse and a G/G sync pulse.

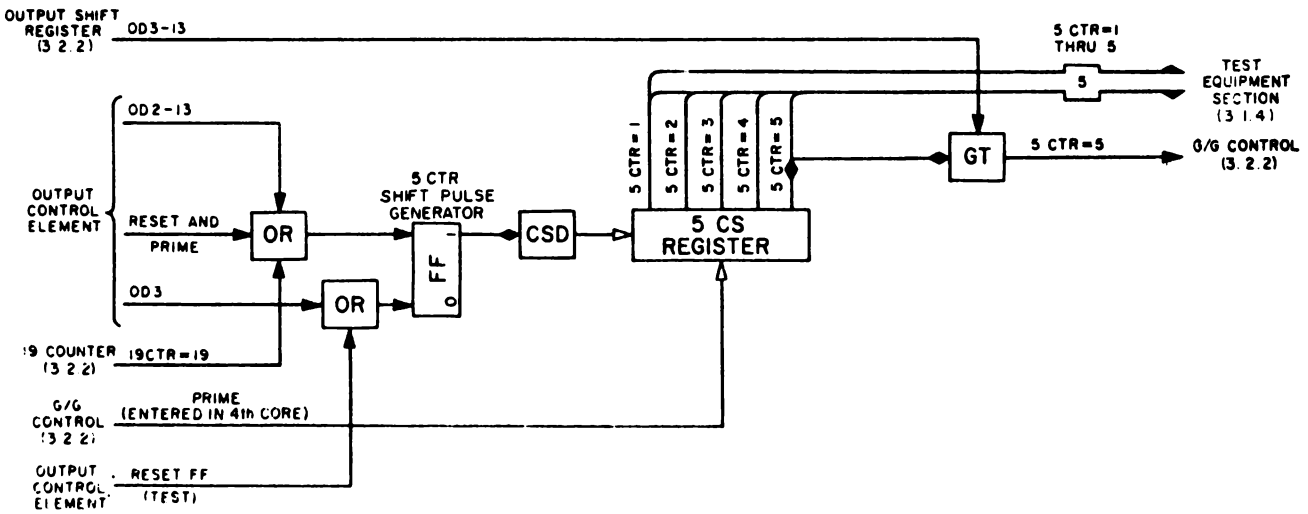


Figure 3-8. 5 Counter (3.2.2), Simplified Logic Diagram

The sync pulse is generated only at 19-counter-18 time. The 5 counter is continually shifted until the 19th shift of the 19 counter. At this time, which is the end of the burst period, the 5 counter is cleared by a 7.5-usec shift pulse developed by the combination of a 19-counter-equals-19, an OD 4-13 pulse, and the following OD 3 pulse. The 19 counter is simultaneously cleared by the G/G control, which then primes both counters. The 5 counter then resumes shifting to start the next burst period.

The 5 counter is always primed by entering a 1 in its fourth core. This is done to satisfy the requirement that 92 timing pulses (5-counter shift pulses) occur during a G/G burst period. By priming the 5 counter in this way, two 5-counter shifts are made to occur between 19-counter-19, which is the time of priming, and 19-counter-1, which is the start of readout and read-in. Since 90 5-counter-shift pulses occur between 19-counter-1 and 19-counter-19, the 92 required 5-counter shift pulses are obtained.

c. 19 Counter

The 19 counter (a 19-core shift register) sequences the readout of each column of the core storage array. Each time this counter is stepped, from 19-counter-1 through 19-counter-17, one column in the core storage array is read out. Figure 3-9 shows a simplified diagram of the 19 counter.

At the start of operation, the 19 counter is cleared and primed by the G/G control. The 19 counter is then shifted by the G/G control once for each 5-counter-equals-5 pulse. Each time the 19-counter is shifted, a 19-counter-equals pulse is generated. These pulses are generated in sequence from 1 through 19. The first 17 of these pulses are used to read out each column of the core array. Since only one register is conditioned

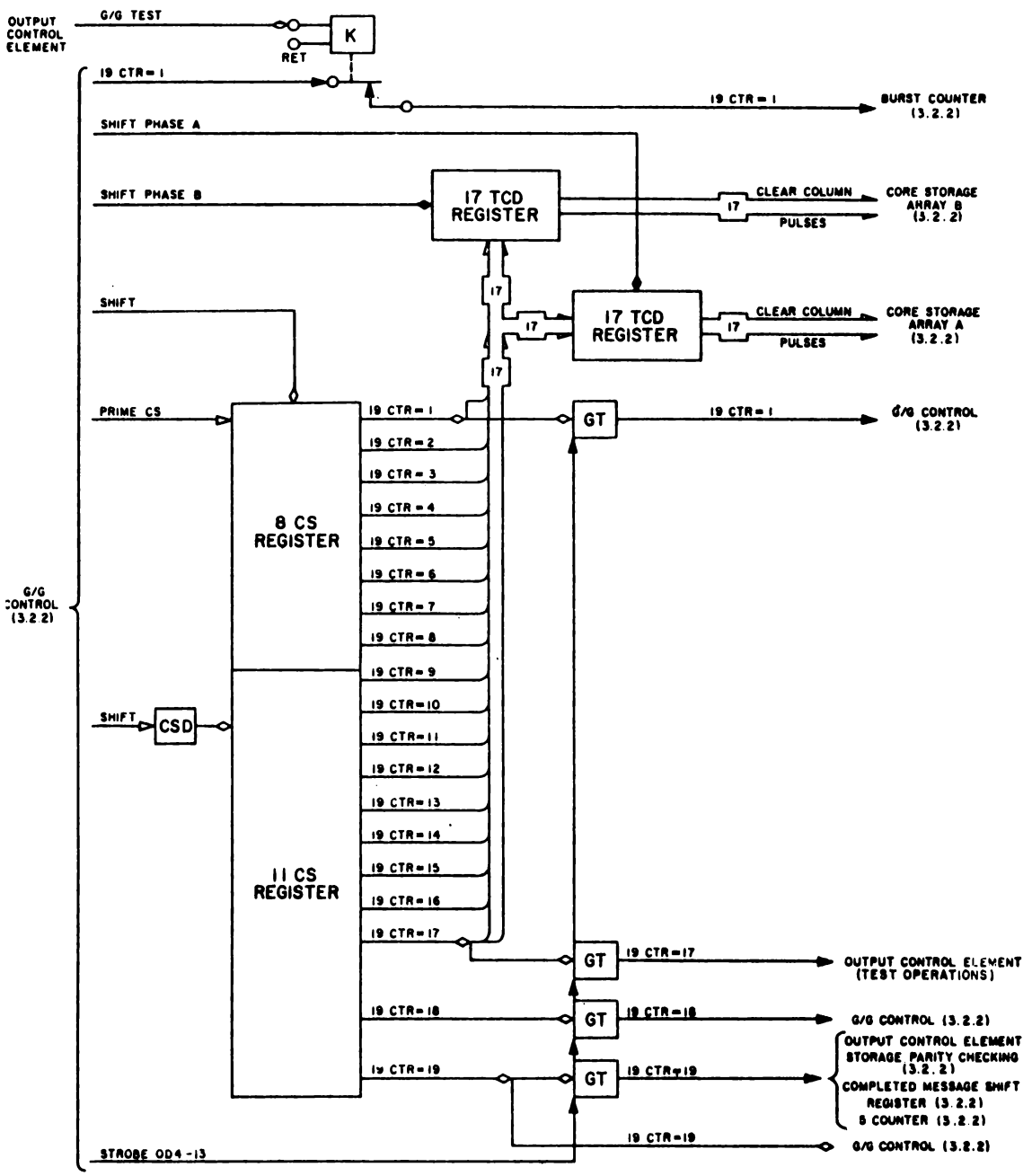


Figure 3-9. 19 Counter (3.2.2), Simplified Logic Diagram

at any one time, clear-column pulses are applied to only one core storage array at a time. The conditioning levels for the TCD registers, shift-phase-B, are supplied by the G/G control.

The 19-counter-equals-1, -17, -18, and -19 pulses are applied as conditioning levels to four gates in the 19 counter. An OD 4-13 pulse occurring at either 19-counter-1, -17, -18, or -19 time will be passed by the gate whose conditioning level is up as a result of the 19-counter-equals pulse.

An OD 4-13 pulse occurring at 19-counter-1 time is sent to the G/G control (Figure 3-10) as a 19-counter-equals-1 pulse, where it starts the shifting of the OSR and also initiates the search G/G level. In addition, the 19-counter-equals-1 pulse is sent from the G/G control, through relay contacts in the 19 counter, to the burst counter (Figure 3-16). During normal operation, the relay in the 19 counter is de-energized and the 19-counter-equals-1 pulse is used to step the burst counter.

During test operation, the relay is energized and the burst counter is prevented from being stepped.

An OD 4-13 pulse occurring at 19-counter-17 time is sent to the test equipment section when it is used in test operations.

An OD 4-13 pulse occurring at 19-counter-18 time is sent to the G/G control as a 19-counter-equals-18 pulse, where it performs the following functions.

(1) Ends shifting of the OSR

(2) Initiates the not-search level

(3) Functions in the generation of the G/G sync pulse

(4) Selects G/G-A or G/G-B arrays for readout

An OD 4-13 pulse occurring at 19-counter-18 time is also sent to the completed message shift register (Figure 3-14) as a 19-counter-equals-18 pulse, where it is used to reset the output flip-flops.

An OD 4-13 pulse occurring at 19-counter-19 time is sent to the following circuits as a 19-counter-equals-19 pulse:

(1) To the 5 counter (Figure 3-8) where it serves to clear the registers.

(2) To the storage parity checking circuit (Figure 3-5) where it is used in the storage parity check.

(3) To the completed message shift register (Figure 3-14) where it is used in the completed message check.

(4) To the test equipment section where it is used in test operations.

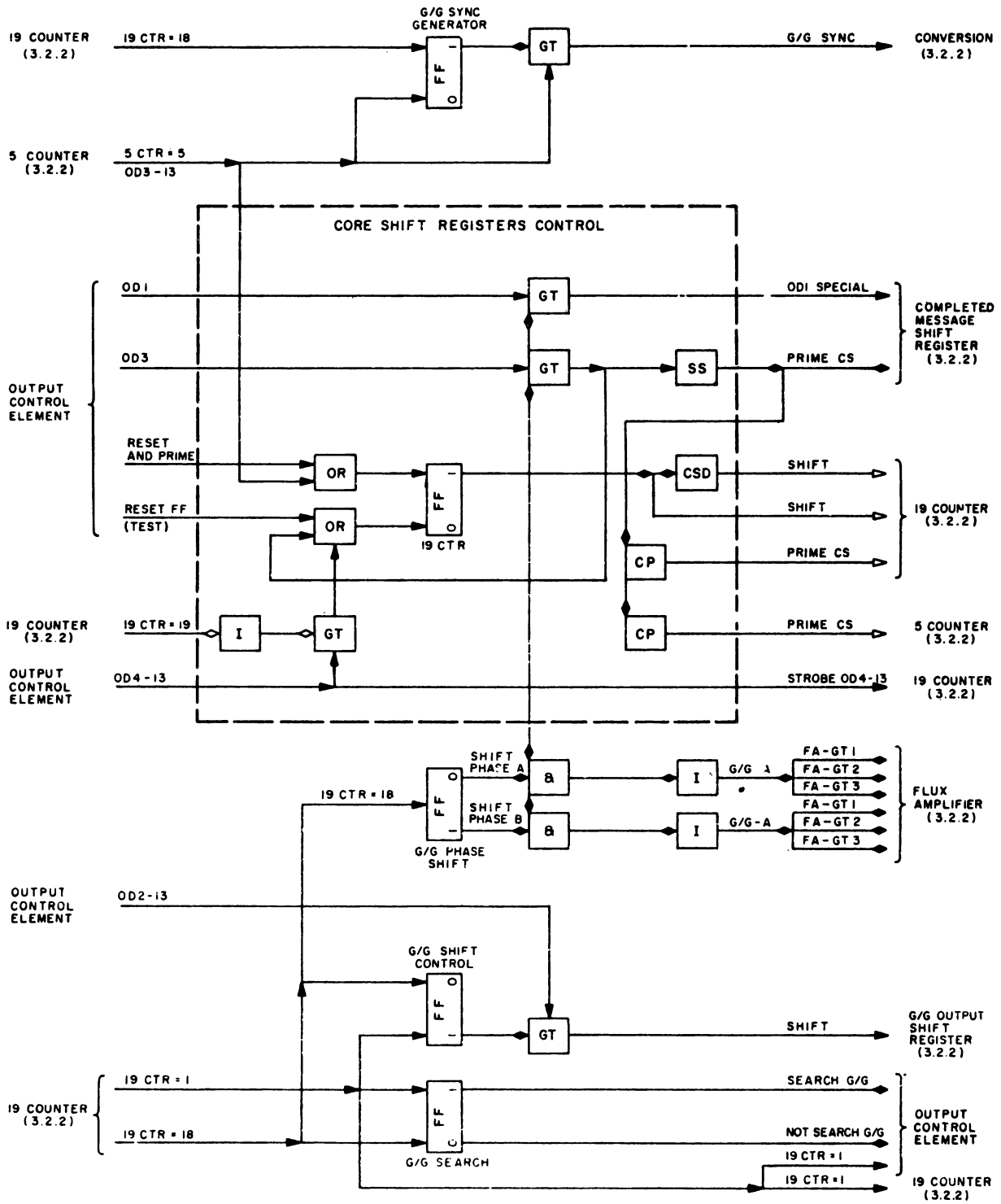


Figure 3-10. G/G Control (3.2.2), Simplified Logic Diagram

In addition to gating an OD 4-13 pulse as previously explained, the 19-counter-equals-19 pulse is applied to an inverter within the G/G control. This pulse serves to prime the 5 counter and the 19 counter as explained in detail later in this section.

d. G/G Control

The G/G control (Figure 3-10) handles the bulk of control functions in the G/G output storage section. This control supplies two sets of levels to the output control element: search G/G or not-search G/G levels, and shift-phase-A or shift-phase-B levels.

The G/G search and G/G not-search levels are developed by the 1 and 0 sides, respectively, of the G/G search flip-flop. This flip-flop is set by each 19-counter-equals-1 pulse. This raises the search G/G level which is sent to the output control element, informing it that the G/G storage section can receive data. The search G/G level remains up until the flip-flop is cleared by a 19-counter-equals-18 pulse. At this time the search G/G level is terminated and the not-search G/G level is raised. This level is sent to the output control element, halting the flow of data to the G/G storage section.

The shift-phase-A and shift-phase-B levels are developed by the 0 and 1 sides, respectively, of the G/G shift-phase flip-flop. This flip-flop is complemented by each 19-counter-equals-18 pulse. The two shift-phase levels therefore alternate between burst periods, each level being raised at the end of every other burst period. These levels are sent to the output control element where they cause data to be written into the core array not being read out at the time. These levels are also applied to the 19 counter, where they are used to condition the TCD registers.

Shift pulses for the OSR are supplied by the output control element as OD 2-13 pulses. These pulses are gated through the G/G control between 19-counter-equals-1 and 19-counter-equals-18 by the action of the G/G shift control flip-flop. The strobe pulse used to sense the counter-conditioned gates in the 19 counter also originates in the output control element as OD 4-13. Since it is used in the G/G control, the strobe pulse is routed through there before being applied to the 19 counter.

The sync pulse indicating the beginning of a burst period transmission is developed in the G/G control by the action of the G/G sync generator flip-flop. This flip-flop is set by a 19-counter-equals-18 pulse. The level developed by the 1 side of this flip-flop conditions a gate which is sensed by 5-counter-equals-5 OD 3-13 pulses and is applied to the conversion equipment as a G/G sync pulse. This 5-counter-equals-5 pulse also sets the 19-counter carry flip-flop.

The remaining portion of the G/G control (the portion labeled core shift registers control in Figure 3-10) supplies all clear, prime, and shift pulses for the 19 counter and the completed message shift register, the prime pulse for the 5 counter, and the gating levels which are applied to the FA's.

The major component of the CSR's control is the 19-counter shift flip-flop. At the start of operations, this flip-flop is set by a reset-and-prime pulse applied by

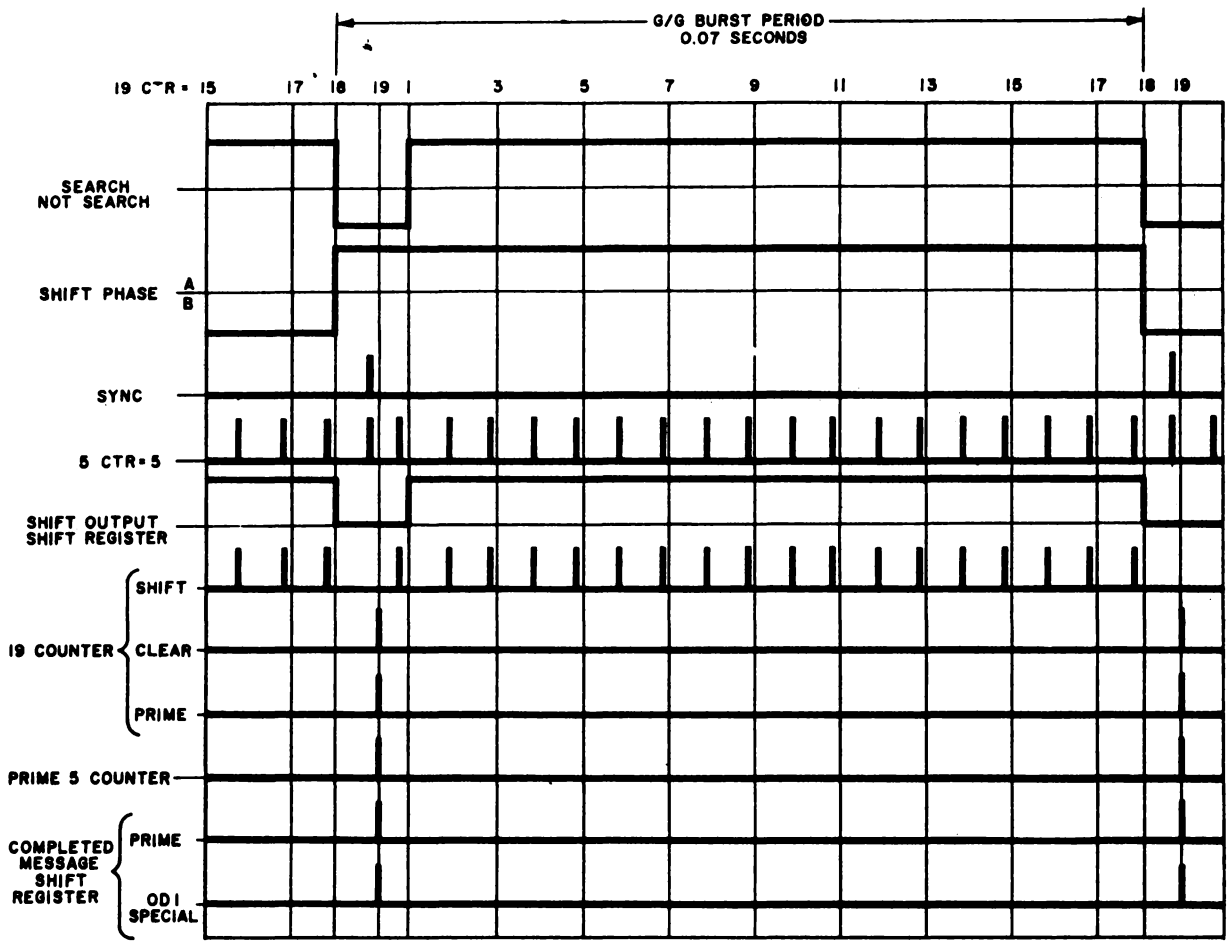


Figure 3-11. G/G Control Timing Chart

the output control element at OD 4 time. The level thus developed by the 1 side of the flip-flop is applied to the 19-counter CSD's and to a gate sensed by OD 3 pulses. The following OD 3 pulse is passed by this gate, clears the 19-counter shift flip-flop and develops a 7.5 usec level which is applied by the CSD's to the 19 counter, thus clearing its register.

The OD 3 pulse that clears the 19-counter shift flip-flop also triggers a single-shot multivibrator. This multivibrator generates a 25 usec signal which primes the 5 counter, the 19 counter, and the completed message shift register.

The 19-counter shift flip-flop is now set by the following 5-counter-equals-5 pulse received at OD 3-13 time. This flip-flop is cleared by the next OD 4-13 pulse when the gate through which the pulse is applied is conditioned by the 19-counter-not-19 level from the inverter. Thus, for all conditions of the 19 counter except 19-counter-

equals-19, the 19-counter shift flip-flop is set between 5-counter-equals-5 (OD 3-13) and 5-counter-equals-5 (OD 4-13) for 2.5 usec. The flip-flop output levels are sent as shift pulses to the 19 counter. In addition, these output levels are sent to strobe two 2-way AND circuits. The latter are associated with the respective output lines of the G/G shift-phase flip-flop. Hence, when an output level is generated by the 19-counter shift flip-flop and is present at either AND circuit in coincidence with a G/G shift-phase level (A or B), the conditioned AND circuit will pass a level to its respective inverter circuit. The level is thus inverted and sent as gating levels 1, 2, and 3 to the FA's. The flip-flop output also conditions two gates. However, the timing of the pulses which sense these two gates is such that the gates produce no output. The conditioning level will not be up fast enough for the gate sensed by OD 3 to pass that pulse, and the level will be down before the OD 1 pulse senses the other gate. Therefore, the only outputs of the CSR's control during 19-counter-not-19 time are the shift pulses for the 19 counter and the FA gating levels.

When the 19 counter reaches 19, the 19-counter flip-flop is set, as before, by a 5-counter-equals-5 pulse which occurs every fifth OD 3-13 pulse. However, at this point the OD 4-13 clear pulse is not passed by the gate, since the inverter deconditions the gate at 19-counter-equals-19. The flip-flop therefore remains set until the gate sensed by OD 3 passes that pulse to clear the flip-flop, an interval of 10 usec. This 10-usec pulse from the flip-flop acts as a clear pulse for the 19 counter and is applied on the shift line. The OD 3 pulse which clears the flip-flop also triggers a single-shot multivibrator to produce a prime pulse for the 5 counter, the 19 counter, and the completed message shift register. The other gate, sensed by OD 1, passes this pulse as OD 1-special to the completed message shift to sense the gates therein and set the completed message flip-flops. Thus, at 19-counter-equals-19, clear pulses are generated for the 19 counter, and prime pulses are generated for the 5 counter, 19 counter, and the completed message shift register. Figure 3-11 shows the timing of the various functions of G/G control.

5. G/G Readout

a. General

Readout of the G/G message is accomplished in three steps. Refer to Figure 3-3. Each message is read out of the core storage array, five bits at a time, through the FA's into the OSR. These five bits are shifted serially out of the OSR. Finally, if permitted by the completed message shift register, the data bits are presented to the conversion equipment. Although this and the following discussion treats only one message slot, the G/G output storage section contains five messages simultaneously. The accompanying illustrations show all five slots; the discussion of one channel applies equally to the other four.

b. Core Array Readout

Note: Refer to Figure 3-12.

Each message slot is read out of the core array by columns at the start of a burst period. The core array is comprised of 17 columns, pulsed serially by clear-column pulses that are applied by the TCD's located in the 19 counter. Each time that

a column is pulsed, the five bits stored in its cores, one bit from each of the five output words in the message slot, are shifted from the core array in parallel form to the FA's. The G/G core array readout is similar to the G/A-FD core array readout.

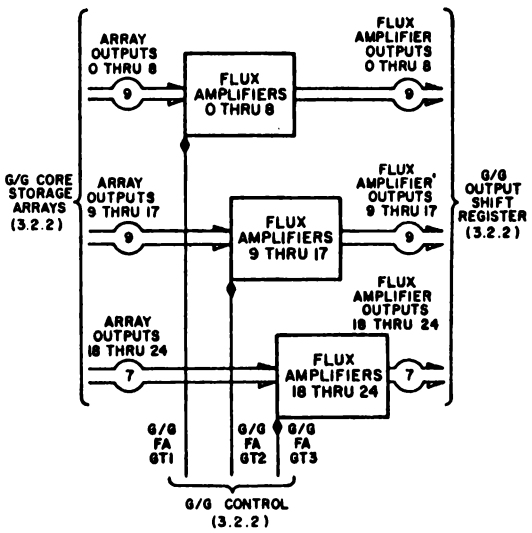


Figure 3-12. Flux Amplifiers (3.2.2), Simplified Block Diagram

Each of the five array output pulses from the G/G core storage array is applied to an FA. A 1 bit is represented by a pulse and a 0 bit by the absence of a pulse. Separate groups of the five FA's shown in Figure 3-12 are gated by gating levels 1, 2, and 3. These levels are 2.5-usec OD 3-13 and OD 4-13 negative pulses employed to prevent noise and spurious signals from passing through the FA's. They are produced in the G/G control simultaneously with each shift of the 19 counter that occurs during readout time. Since these 19-counter shifts generate clear-column pulses which read out columns of the core array, the core storage array outputs are applied to the FA's during the 2.5 usec that the FA's are gated and operative. The FA's after amplifying and stretching the array output pulses, send the pulses to the OSR as FA outputs. The outputs from the FA's are sent over 25 lines labeled FA output 0 through FA output 24, respectively.

c. Output Shift Register (OSR)

The OSR (Figure 3-13) receives five bits at a time from each of the five messages, and loads them into five 5-core shift registers. Shift pulses from the G/G control shift each register 1,300 times per second. Since the gate at the output of each 5-core shift register is sensed only when the data bits are placed in the shift register, no spurious output pulses are generated when the register is loaded. The shift signals from the flip-flop are 2.5 usec in duration.

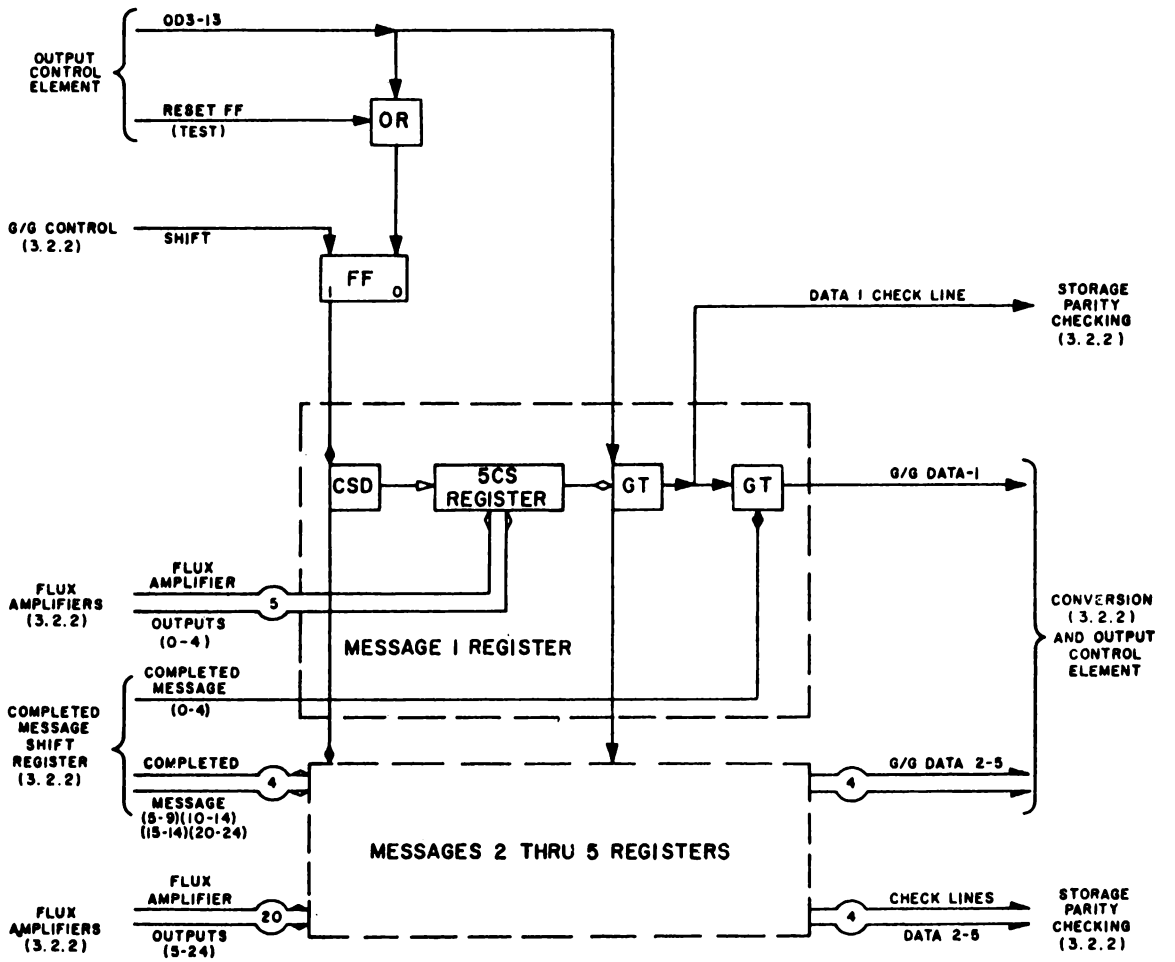


Figure 3-13. G/G Output Shift Register (3.2.2), Simplified Logic Diagram

The output of the first gate is applied to the storage parity check circuit and to a second gate. This gate is conditioned by a completed-message level from the completed message shift register. If the level is applied, the contents of the OSR are sent to the conversion equipment.

The next five 5-bit groups from the FA's must be loaded into the OSR within 4 ms after the first groups have been shifted out. This is done to maintain an even 1,300-pps output rate from the OSR.

d. Completed Message Shift Register

The completed message shift register (Figure 3-14) counts the number of output words written into each slot in the core storage array. If the full five words are written into a slot during a burst period, the message in that slot will be passed through

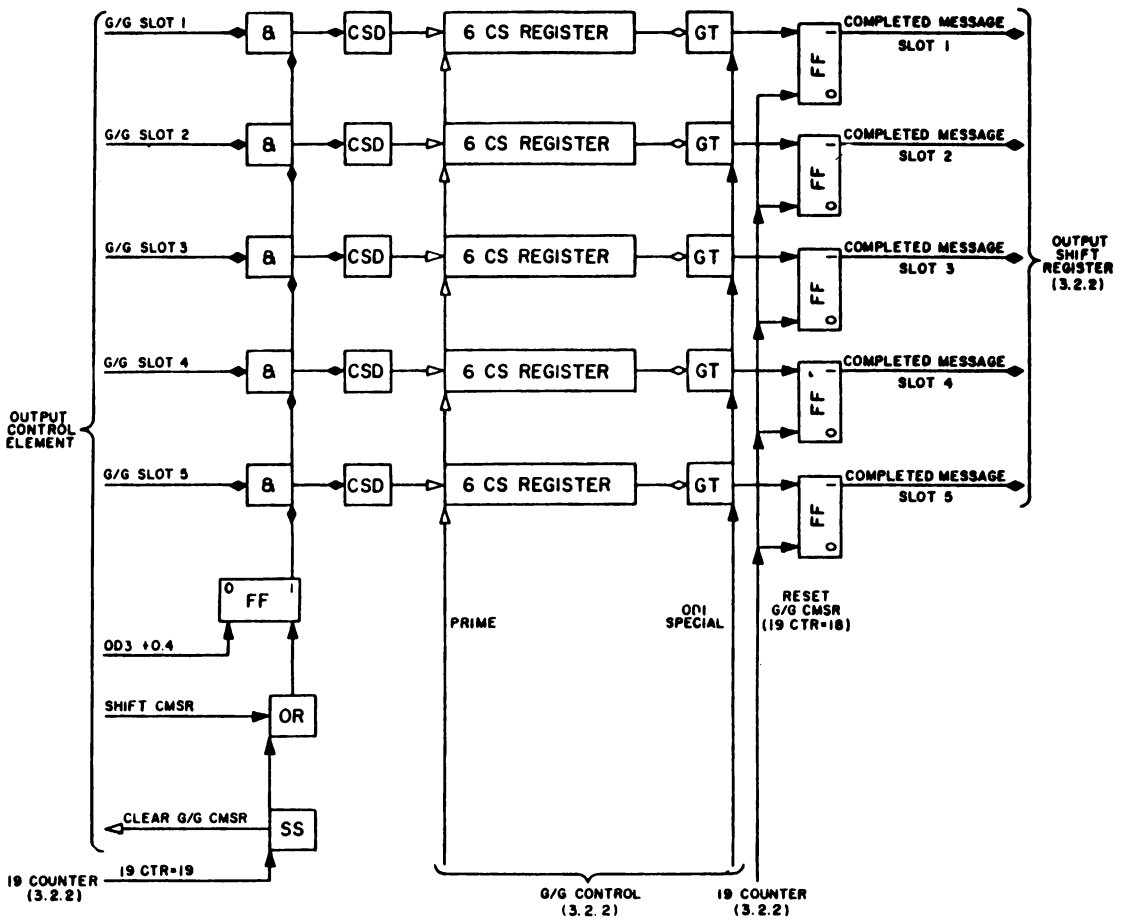


Figure 3-14. Completed Message Shift Register (3.2.2), Simplified Logic Diagram

the OSR to the conversion equipment. If not, the second gate in the OSR is not conditioned and no data from that message is presented for transmission.

At the beginning of a burst period, each OSR in the completed message shift register unit is primed by the G/G control which writes a 1 in the first core. As each word is written into the appropriate core storage array, a slot level is raised corresponding to the message slot in which the word is written and a shift-completed-message-shift-register pulse is supplied by the output control element. This pulse shifts ahead the 1 in the shift register corresponding to that slot. After five words have been written into a slot, the last core in that shift register will hold the 1.

As the read-in ends, the flip-flops which now hold the results of the complete message check on the message that was being simultaneously read out from the other

array are cleared by a 19-counter-equals-18 pulse. A 19-counter-equals-19 pulse from the 19 counter is now applied both to a single-shot multivibrator and to the shift-pulse generator flip-flop. The output of the single-shot multivibrator is sent to the output control element, which returns it to the completed message shift register as a conditioning level on all five AND circuits. Thus, the 19-counter-equals-19 pulse shifts all 5-core shift registers simultaneously. If the last core of a register holds a 1 when this last shift occurs, the gate at the output of the CSR is conditioned and then sensed by the special OD 1 pulse which occurs at this time. This sets the corresponding flip-flop, supplying the completed message level for that slot. If fewer or more than five words are written in a slot during a search period, the 1's placed in the first core of each CSR will not be in the last core of the register to set the flip-flops, and the completed message level will remain down.

6. Message Check

As G/G messages are transferred out of the output storage section for transmission, a parity check is taken on each message. The data check lines from the OSR, shown in Figure 3-13, are applied to the storage parity checking circuit (Figure 3-15). In that circuit, the number of 1's in each message is counted. The number should be even, counting the parity bit added to each right-half drum word by the output control element. If the parity count in any message is odd, the 1 side of that message channel flip-flop will be up, conditioning the gate through the OR. When the gate is sensed at 19-counter-equals-19, a G/G alarm is generated. This alarm is also used to clear the flip-flops.

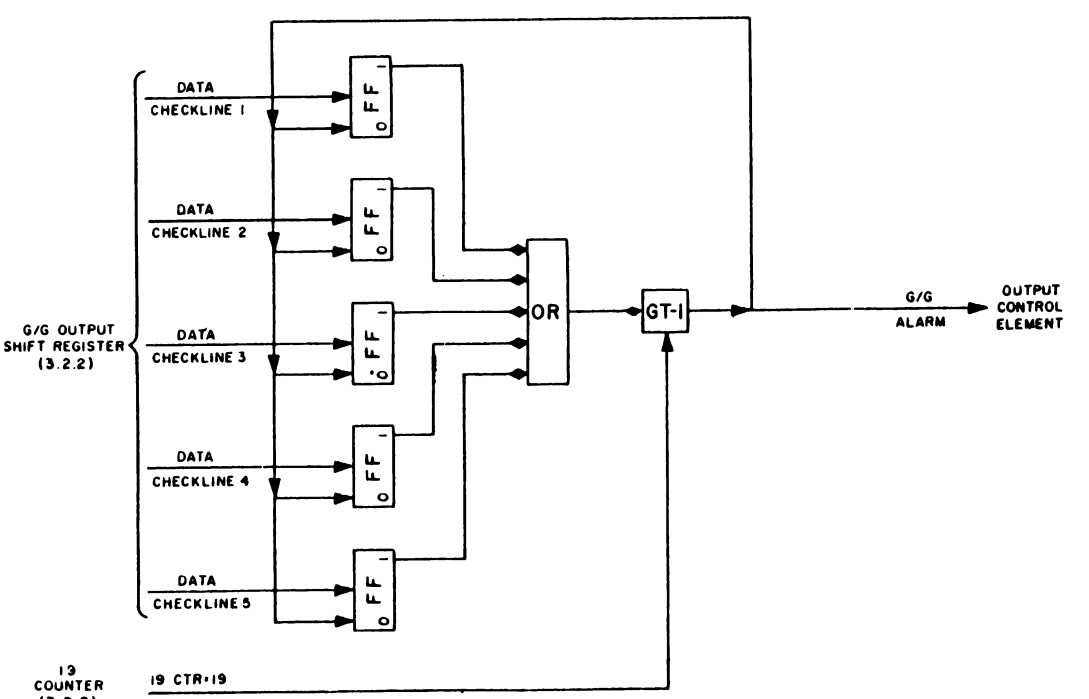


Figure 3-15. G/G Storage Parity Checking (3.2.2), Simplified Logic Diagram

7. Burst Sequence and Timing

a. Purpose

G/G messages are transmitted in 70-ms burst periods. Successive messages on a single channel may follow each other immediately if sufficient message words are delivered through the OB fields to the output storage section. Messages are addressed to specific receiving points and also sequenced for transmission. This sequencing is accomplished by assigning each message word a burst number and keeping a count of the number of the burst to be next transmitted. By comparing the assigned burst number of a message word to the burst count for the next burst period, and by writing into the core storage array during read-in only those message words which are scheduled for transmission within that burst period, the time sequence is established.

b. Burst Counter

The G/G burst counter (Figure 3-16) is a standard 8-bit flip-flop counter (scale of 256) which is stepped by 19-counter-equals-1 pulses at all times except during test operations. Two sets of outputs are taken from the counter, one set from the 0 sides of the flip-flops, designated the burst counter complement. The burst counter contents are supplied to the output control element and are also used in the comparison circuits. A reset flip-flops signal from the output control element is supplied after shutdown or test operations.

c. Burst Number Comparison

The burst counter is stepped at the start of a burst period by a 19-counter-equals-1 pulse. The number in the burst counter during each burst period corresponds to the number of the next burst period.

G/G message words are read from the OB fields by status identification, using the burst number as the identity code. As a word on the OB fields moves into reading position, bits L8 through L15 (which contain the assigned burst number) are read into a flip-flop register in the output control element. This register supplies to the G/G burst counter both the assigned burst number of the word and the complement of the assigned burst number. The assigned burst number of the word and the complement of the G/G burst counter contents are applied to an AND circuit, while the complement of the assigned burst number and G/G burst counter contents are applied to another AND circuit. If the assigned burst number matches the burst counter contents, the outputs of the AND's will be down. Since all the inputs to the OR circuit shown in Figure 3-16 are down, the output of the inverter (compare G/G) will be up. The word will therefore be accepted, and the output word will be written into the core storage array in the slot and register to which it was addressed by the left drum word.

If the assigned burst number of the words does not match the G/G burst counter contents, one or more AND outputs will be up, suppressing the compare-G/G level from the inverter. In this case, the drum word is not accepted and the search continues to the next word.

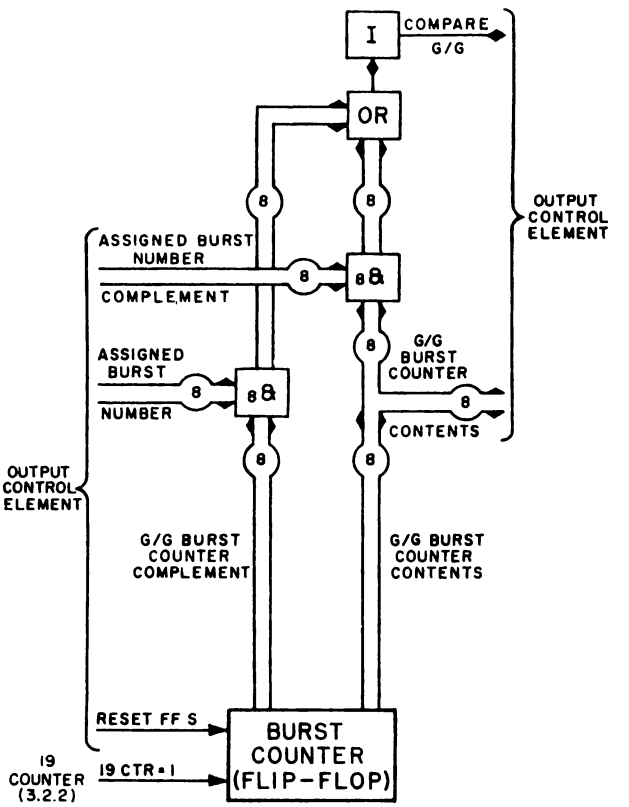


Figure 3-16. G/G Burst Counter (3.1.2), Simplified Block Diagram

8. Conversion

Information leaving the G/G output shift register is modified by the conversion circuits before being fed through the switching circuits to the telephone transmission equipment. Refer to Figure 3-17. The conversion circuits convert the G/G data and sync standard pulses to a series of synchronized, gated, 1,300-cps sine waves. The information is modified in this manner to make it comparable with telephone company equipment requirements.

The conversion circuits contain five identical channels, one for each of the G/G messages. These channels are identical in circuitry and operation to the G/A-FD conversion channels. Figure 3-17 shows one of the five identical G/G message conversion channels, the channel for G/G message 1. For each data or sync pulse received, the conversion channel will transmit slightly less than one cycle of the 1,300-cps timing signals to the telephone equipment over the data or sync lines. It is required that exactly two 0 bits occur on the data lines between the end of the output sync signal and the beginning of the first data bit. (See Figure 3-18.) This is accomplished by applying an OD

3-13 G/G sync pulse to the sync conversion channel simultaneously with the 19th shift of the 19 counter. Since two 5-counter shifts occur between 19-counter-19 and the start of readout which occurs at 19 counter-1 time the required sync pattern (. . .00S00) is obtained.

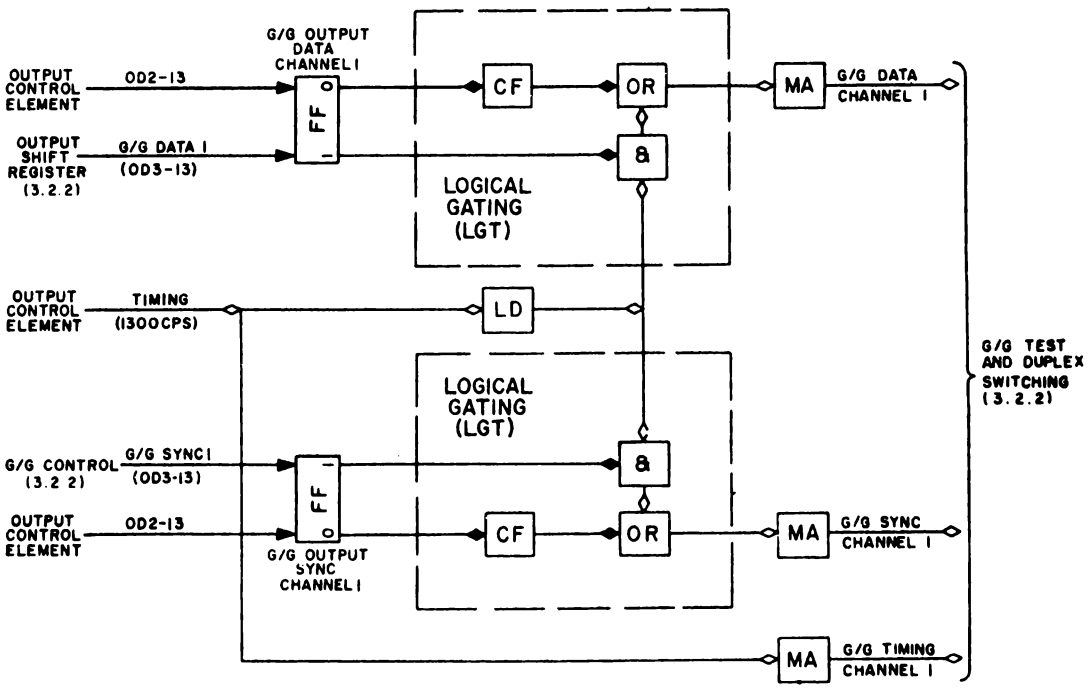


Figure 3-17. G/G Conversion, Message 1 (3.2.2), Simplified Logic Diagram

The data, sync, and timing inputs and outputs of one G/G message conversion channel for a typical G/G message are shown in Figure 3-19. The outputs of this message channel, together with the outputs of the other four identical message channels, are fed to the switching circuits and from there sent out to the telephone equipment.

9. Switching

The G/G test and duplex switch circuits control the G/G output of the Output System of each computer. The switching circuits contain relays which provide for the switching of each of the five G/G messages. However, the relay circuits for each message are identical. For this reason, Figure 3-19 shows a simplified diagram of the G/G test and duplex switching circuits for only one G/G message.

The relays provided by the G/G test and duplex switching circuits are controlled so that only the Output System of the active computer is presented to the telephone line terminal equipment. Relays are also provided to enable the Output System on standby status to be switched to the appropriate test busses through the pattern generator. These relays are operated during test operations only.

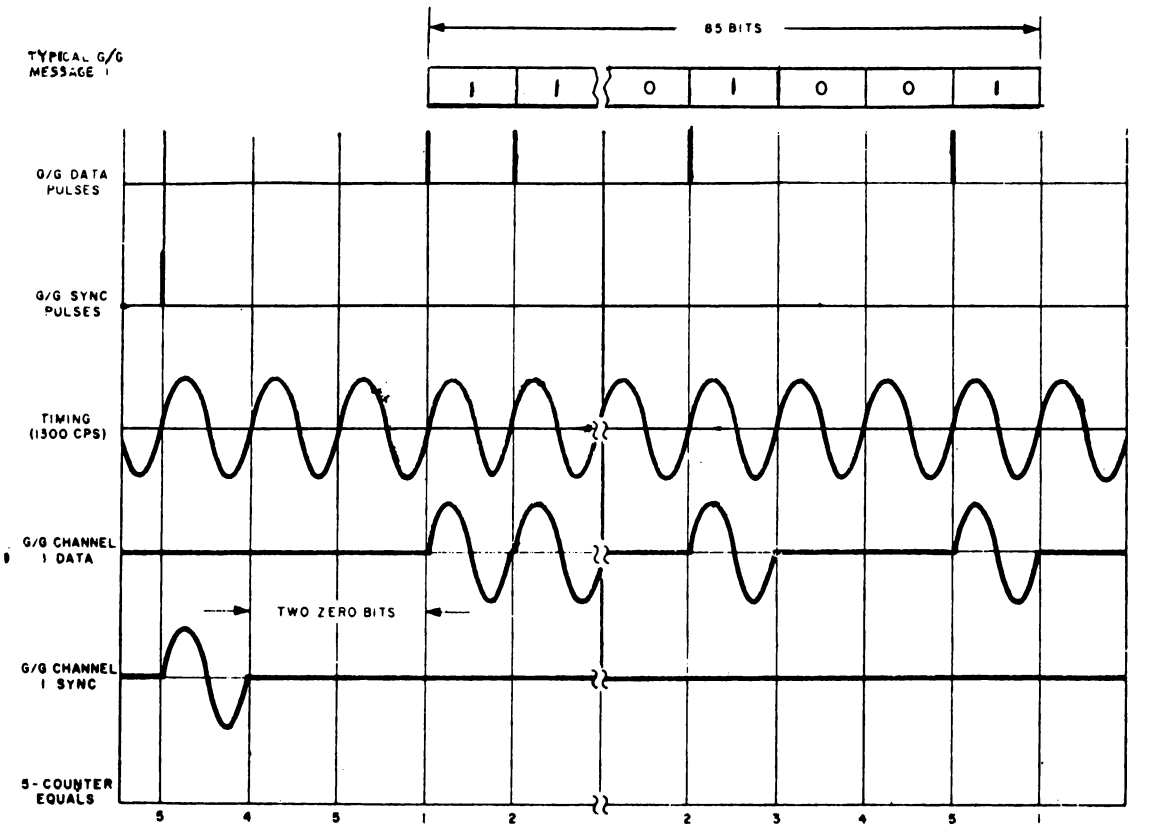


Figure 3-18. G/G Conversion, Input and Output Signals

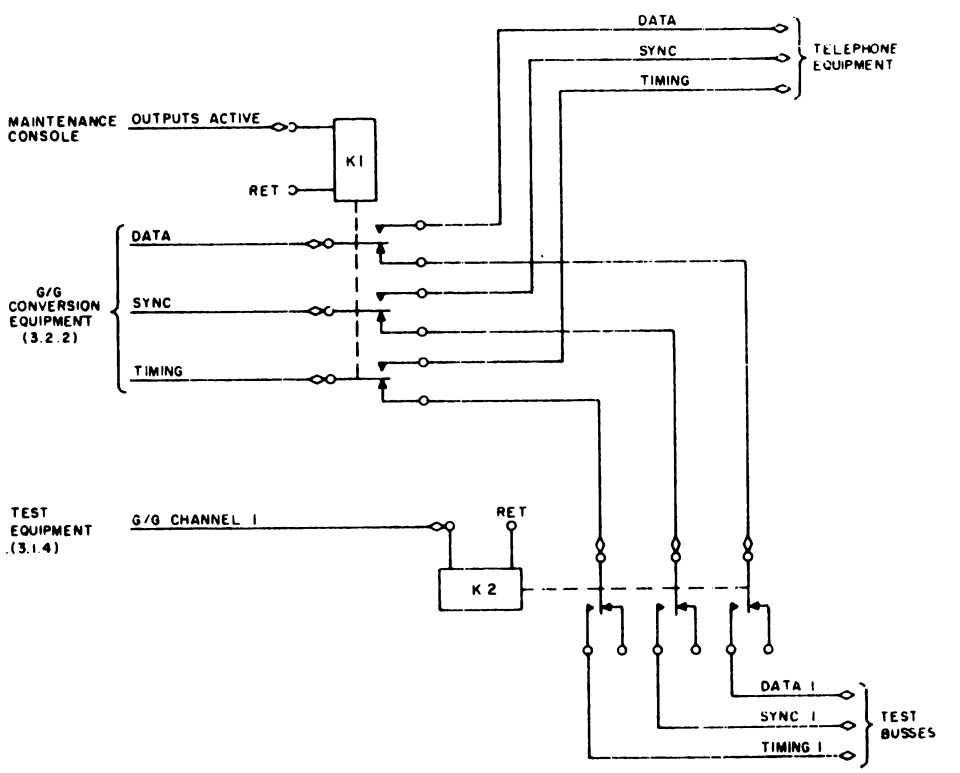


Figure 3-19. G/G Test and Duplex Switching, Message 1 (3.2.2), Simplified Diagram

SUMMARY QUESTIONS

1. G/G Readout Time is_____ mil-sec.

2. G/G storage consists of _____storage arrays.

3. Search Time for G/G begins with 19-counter-_____to 19-counter-_____.

4. Readout time for G/G begins with 19 counter-_____to 19-counter-_____.

5. G/G storage parity is_____.

6. A sync pulse is generated as a result of 5-counter-_____and 19-counter-_____.

7. The FA circuits are gated by a negative signal. (T/F)

8. What is the function of the CMSR's?

9. How long is the clear level to the 19 counter?

10. Messages are loaded into all slots but the data flip-flops for all channels are never set. This could be caused by:

   a. GT 5 in 33LN passing all pulses (10A)

   b. Pin E5 in 33LT open (12D)

   c. Pin B2 33LW open (10C)

   d. P.U. 33 LS removed

   e. GT 7 in 33 JG will not pass a pulse

11. How much time is there from the 19-counter-19 until R2 for Adr. 3 sets the data FF? (Express in ratio/1300)

12. If we have successive messages in Slot 1, how long is CM FF cleared in usecs? (In 33LL) (12C)

13. The data FF for channels 4 and 5 can never be set. Channels 1, 2 and 3 function normally. What could cause this?

   a. 33HW $_{B}$CSD 8, 9 will not conduct (10B)

   b. GT 1 33LP non-conductive (7C)

   c. GT 9 33JG non-conductive (11A)

   d. PA5 and PA6 in 33HY non-conductive (5D)

   e. 33HX G1 open (9C)

TTY Storage

1. The TTY storage section receives right half-words, their storage parity bits, and busy bits from the output control element. This data is stored temporarily and then transmitted over 25 TTY channels to standard teletypewriters. The teletypewriters are located at anti-aircraft operational centrals, air bases, higher headquarters, and non-automatic adjacent centrals. The TTY storage section, when transmitting TTY data simulates a transmitting teletypewriter. Thus, the TTY data is transmitted in a form compatible with receiving teletypewriters at the TTY channel termination points.

A standard TTY machine operates at a nominal speed of 60 wpm. This is a normal rate, since the number of words will vary, depending on the number of operations the machine must perform. The standard TTY performs 360 operations per minute. An operation, or character, is defined as one of 26 printing functions or one of six command functions, the whole termed TTY signals.

The TTY machine transmits 360 signals per minute. These signals are sent, one at a time, through a 4-terminal transmission channel, or loop. Figure 3-20 shows the composition of one TTY signal. Each signal consists of seven consecutive intervals. The first and the last of these seven intervals are, respectively, the start and the stop intervals; the remaining five intervals comprise a code identifying the character or command being sent. There are only two possible conditions of the teletype line; that is, mark or space (closed or open, respectively) and therefore the code is a binary code. The 5-bit binary TTY code can be enclosed into 32 possible combinations. Thus, 32 different TTY signals may be sent. The signals sent consist of 26 printing or typing functions and five machine command functions (See Table 1-3.) The usual command functions are blank, space, line feed, carriage return, letters or figures. The latter two command functions determine whether the typing functions following will be alphabetical letters or figures and symbols. The printing or typing functions may therefore represent the 26 letters of the alphabet, or 26 decimal numbers and symbols.

The TTY transmission line is normally kept closed; a pulse causes the line to open. Thus, the pulses are inverted with respect to the usual conception of a circuit.

The start pulse is always transmitted as a space, opening the TTY line and causing a rotary distributor in the TTY receiver to start rotating. As the arm of the distributor rotates, it crosses each of five contacts in succession, which correspond to the five information bits in the TTY character. Each bit, therefore, is read into the appropriate contact circuit in the receiver. When the stop interval arrives, the distributor arm is in the stop position and the closed or mark condition which occurs during the stop interval stops the distributor in the start position, ready for the next character. The five information bits that were received energize electromechanical circuits, causing the transmitted character to be typed, or the indicated command to be executed.

The TTY signals, as synthesized by the TTY storage section, are actually transmitted at a rate of 364 signals per minute, or one signal every 15/91 second, closely approximating the standard rate. The seven pulses constituting a signal are transmitted during this interval. The start bit and the five information bits are of equal

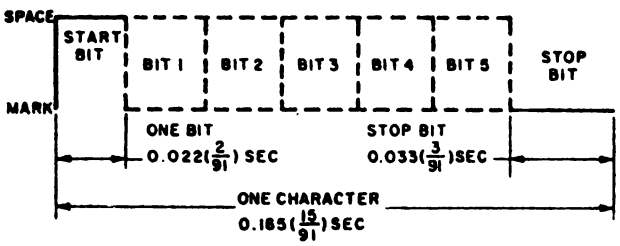


Figure 3-20. Composition of TTY Signals

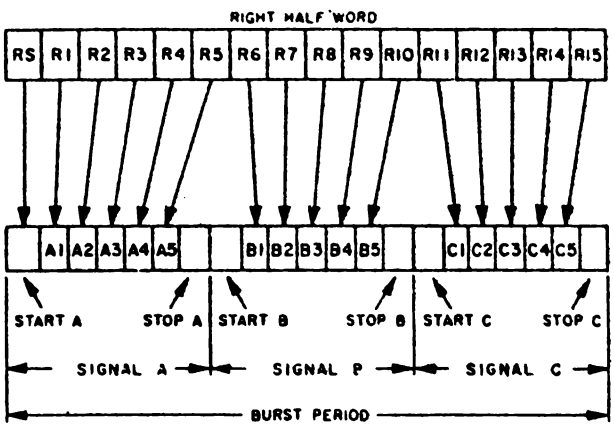


Figure 3-21. Composition of TTY Output Word

length, 2/91 second; the stop bit is 1-1/2 times as long, or 3/91 second. (See Figure 3-20.) Thus, each of the first six bits lasts approximately 22 ms and the stop bit is 33 ms long.

Twenty-five TTY output words may be transmitted simultaneously during a TTY burst period. Each output word is transmitted over a separate TTY channel to its specific destination. A TTY output word contains three TTY signals as shown in Figure 3-21. Since a complete TTY message is always longer than these three signals, it follows that several successive TTY burst periods will be required to transmit a single message on each TTY channel.

It should be noted that the RS bit of the right half-word is employed as the start bit of TTY signal A. The start bits for signals B and C are made up of BB2 and BB1, respectively. Since the start bits must be transmitted as spaces (open line), the RS, BB2, and BB1 are 1 bits.

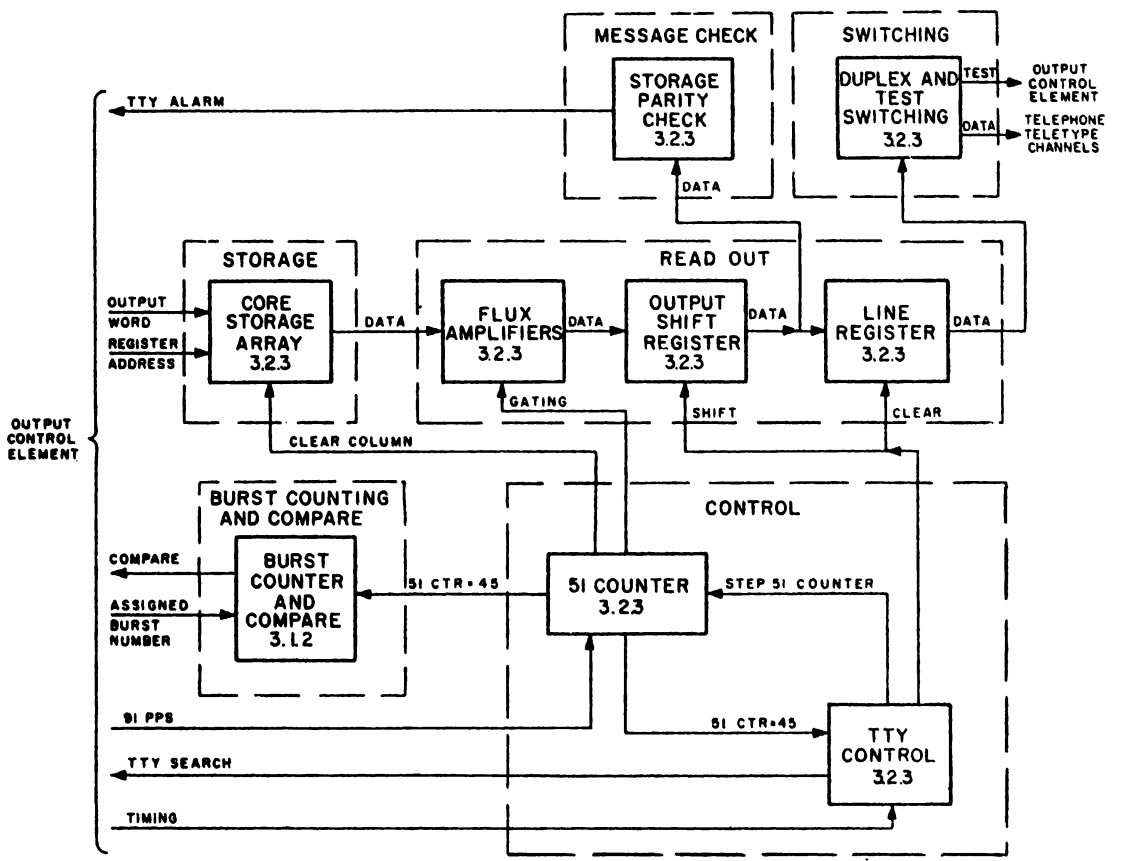


Figure 3-22. TTY Output Storage Section (3.2.3), Simplified Block Diagram

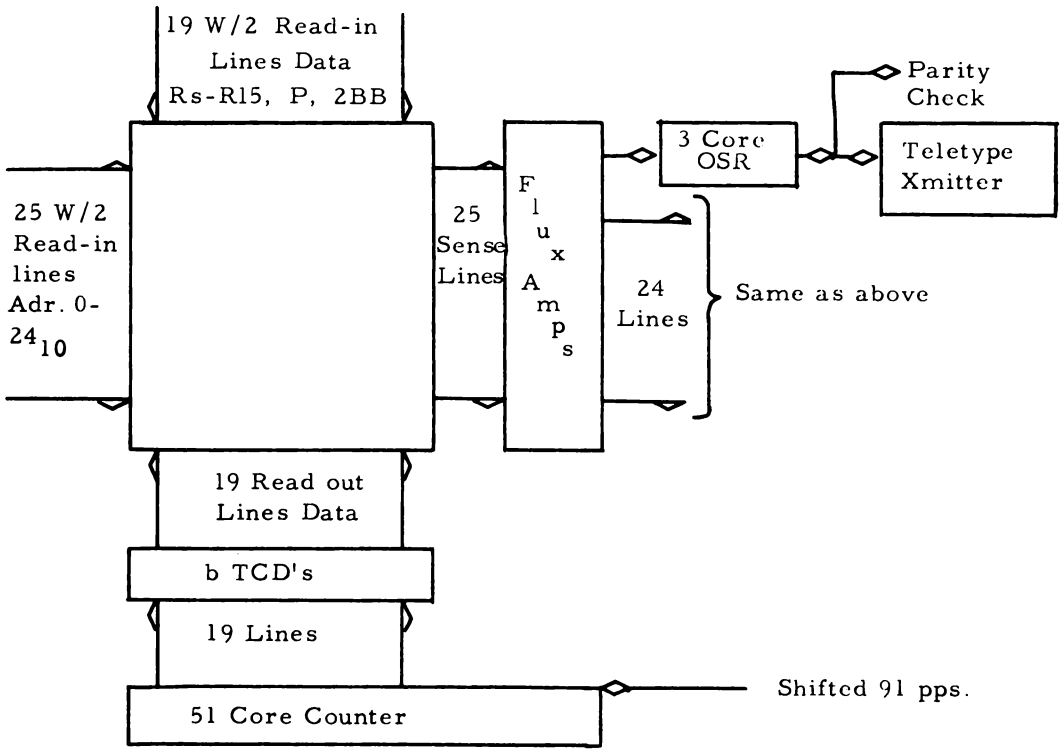
2. Operation (Figure 3-23)

A simplified diagram of the TTY storage section is shown in Figure 3-22. As is shown in this diagram, the TTY storage section is functionally divided into storage, control, readout, burst counting and compare, message-check, and switching circuits. These circuits perform functions similar to the corresponding circuits of the G/A-FD storage section.

Operation of the TTY storage section is similar to that of the G/A-FD storage section in that each TTY burst period is divided into search time and readout time. This division is accomplished by the action of the control circuits. These circuits, consisting of the TTY control and the 51 counter, also control the functions of the storage section during each separate interval. The 51 counter, in particular, controls the timing of these functions.

a. Counter Operation

In order for the 51 counter to perform the timing functions, the counter operates as follows:



Sequence of Read Out

P, RS — R15

Figure 3-23. TTY Storage, Block Diagram

The 51 counter is shifted continuously and repeats its counting cycle after it has been shifted 51 times from its start of operations. This counter is generally shifted at a 91-pps rate of timing pulses received from the output control element. During the interval between its second and eighth shifts after the start of each cycle, however, the 51 counter is shifted at high speed; that is, once every 20 usec, to eliminate the parity bit from the final teletype message. Each time this counter is shifted, a 51-counter-equals pulse is produced.

b. Search Time

Search time is the interval during which output words are accepted for storage by the storage section. The TTY search time starts at the time of the 45th shift of the 51 counter. At this time, the 51-counter-equals-45 pulse which is produced shifts the burst counter and also causes the TTY control to supply a search TTY level to the output control element. This search level indicates the TTY storage section is ready to receive output words for a new burst. During search time, each correct TTY output word on the OB drum which has a burst number that compares with the present contents of the TTY burst counter is entered in the TTY core storage array.

Search time continues until 51-counter-51 time, a total of six 51-counter shifts or 6/91 second (66ms). This is sufficient time for the OB fields to be searched.

The 51-counter-equals-51 pulse then causes the TTY control to raise the not-search-TTY level, thereby ending search time. The 51 counter now repeats its operational cycle, and with its next shift produces a 51-counter-equals-1 pulse. This pulse starts the interval of the burst period called readout time.

c. Readout Time

Readout time is the interval between 51-counter-1 time and 51-counter-45 time. During this interval, the output words previously assembled in the core storage array are read out into the OSR. The OSR then transfers these words, bit by bit, through the line register and onto the TTY channels. Readout takes place as explained in the following paragraphs.

The 51-counter-equals-1 pulse, produced when the 51 counter is first shifted at the beginning of its cycle, is sent to the core storage array where it serves to read out the information contained in one column of cores. This information consisting of 25 parity bits, is sent through the FA's and loaded into the 25 3-core shift registers which make up the OSR. Each bit is entered in the first core of each of these registers. The next shift of the 51 counter generates a 51-counter-equals-2 pulse. This pulse shifts the 25-shift registers, causing the bits entered in the first core of each register to be shifted to the second core. The 51 counter is now shifted six times at high speed. As a result, 51-counter-equals-3 through 51-counter-equals-8 pulses are generated by these shifts. These pulses alternately read out a column of cores into the OSR and then shift the register. During this high-speed shifting, the parity bits which were present in the OSR at the beginning of the high-speed shifts are shifted out of the OSR and into the line register. This shifting takes place at a speed too high for response of the line register relays, and the parity bits are effectively destroyed. The parity bits are not required because a teletypewriter has no means of checking parity.

At the end of the high-speed shifts, three columns of cores have been read out of the array and loaded into the three cores of the 25 shift registers. The start bit of the first TTY character of each output word is present in the last core of each of the 25 shift registers. The 51 counter is now shifted at a 91-pps rate and generates pulses which alternately read a column of cores into the OSR and then shifts this register. Each time the OSR is shifted, the bits present in its last cores are applied to the line register. The line register controls 25 relays that hold each of the TTY lines in an open or closed position, depending on whether the corresponding output word bit applied is a space (1) or a mark (0).

Readout continues as described above until 51-counter-45 time, at which time the core array is empty and search time begins. During each time, an interval of approximately 66 ms, readout from the core array is interrupted. This delay is eliminated from the message transmission by the action of the OSR. At the start of readout, the three cores of each shift register are loaded at high speed when the first three bits of each TTY output word. During search time, these bits continue to be applied to the line register and the TTY lines, thereby eliminating any transmission delay caused by array read-in.

During search time at 51-counter-50 time, the stop bit of the last character of the TTY output word is shifted into the line register. It stays there for the required

three timing pulses (3/91 second) until the next shift pulse, which occurs at 51-counter-2 time.

At 51-counter-51 time, the end of searchtime, the OSR is empty, but the core storage has been refilled. At 51-counter-1 time, the readout process repeats.

During readout the data is examined for errors in transmission. This check is performed by the storage parity checking circuit which receives TTY data as it is shifted out of the OSR. If an error is found, a TTY alarm is transferred to the alarm section in the output control element.

The operation of the TTY storage section is shown in chart form in Figure 3-24. This chart shows the column cleared by each 51-counter pulse, and also shows the position of each bit as it is shifted out of the core array and through the OSR and line register. The shift pulses for the OSR and line register are shown in this chart as shift time pulses.

3. Storage

a. General

The TTY storage section has provision for the storage of one 3-character TTY output word in each of 25 registers. Each register receives the information contained in one right half-word, and then supplies information to one TTY channel. The composition of a right half-word and the division of this word into three TTY characters is shown in Figure 3-21.

b. Core Storage Array

The TTY core storage is an array of ferrite cores and is similar in operation to that array described in the G/A-FD section. The array consists of 26 registers; 25 are used for storage and one is a spare.

Each register contains 22 cores. Of these, only cores 1 to 3 and cores 7 to 22 are used. The cores in the core storage are arranged in registers and columns of bits. (See Figure 3-25.)

c. Core Array Read-In

The read-in to the TTY core storage array (Figure 3-25) is similar to that of the G/A-FD core storage array. Each of the cores has two half-write windings. A half-write register winding and a half-write message winding. Current through either one of these windings does not produce enough flux to set the core, but current through both windings will set the core. The half-write register winding is in series with windings on each other core in the same register. The half-write message winding is in series with each core in the same column. To write into a core, then it is necessary to select both the column and the register.

In the read-in operation during a TTY search interval, as each right-half word addressed to the TTY storage section is received, a half-write current pulse passes

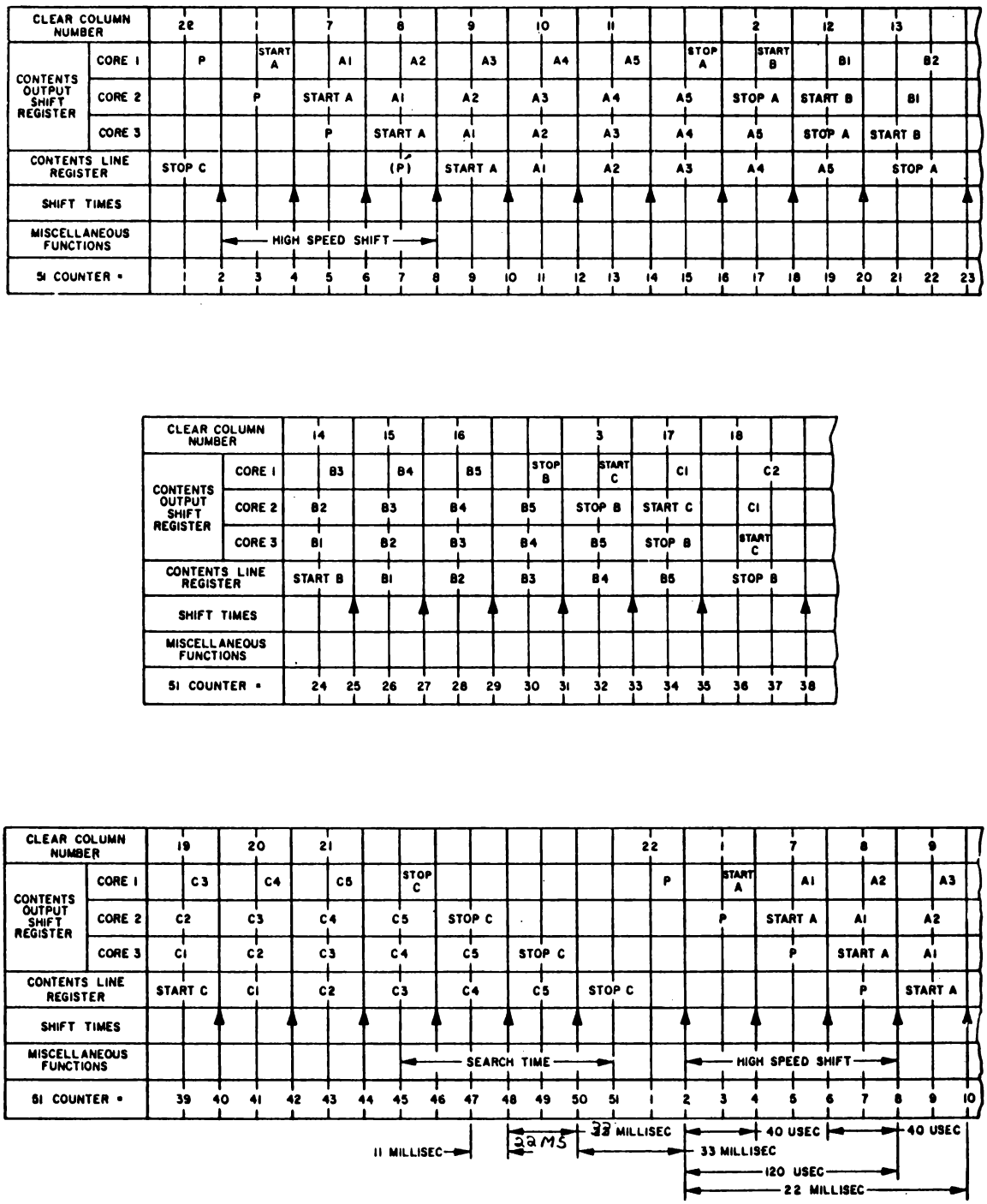


Figure 3-24. Timing of TTY Storage Section Operations

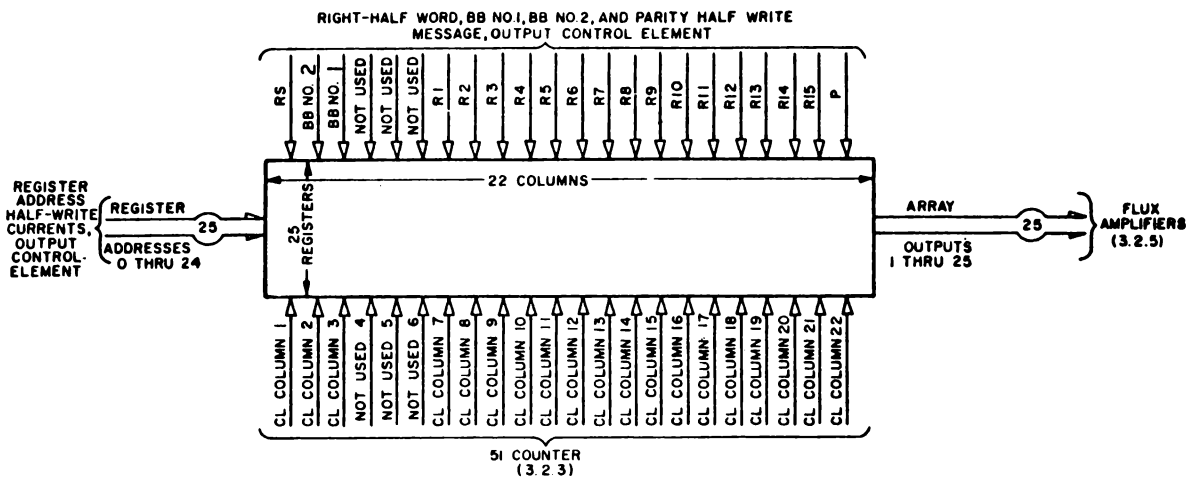


Figure 3-25. TTY Core Storage Array (3.2.3), Simplified Logic Diagram

through the half-write register windings in the register selected for read-in. At the same time, the contents of the right half-word, parity bit, and busy bits are applied to the half-write message windings in columns 1, 2, 3, and 7 through 22. Thus, data is written into the selected register. Columns 4, 5, and 6 are not used.

4. Control

a. General

The action of the TTY storage section is controlled by the 51 counter and the TTY control. These circuits generate and gate the timing signals necessary to accomplish the various operations of the TTY storage section. Note: Refer to Figure 3-26.

b. 51 Counter

The 51-counter, shown in Figure 3-26, is a tape core counter similar to the 25 counter in the G/A-FD storage section, but with 51 cores. At the beginning of each counting cycle, the counter is cleared. Immediately thereafter, a 1 is primed into the first core and then continuous stepping of the counter at a 91-pps rate begins. The outputs of the 51 counter are labeled with respect to the core from which they originated. Generally, the output of every other core in the 51 counter is used to shift the contents of successive columns from the core storage through the FA's in the OSR. The other alternative outputs of the 51 counter are used both to shift the OSR and to clear the line register. Table 3-1 shows the destination and function of each 51-counter output pulse.

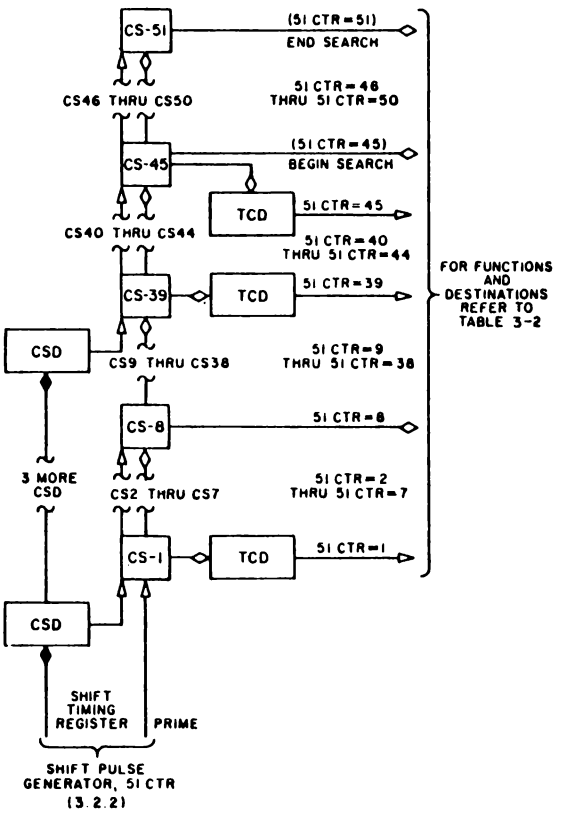


Figure 3-26. 51 Counter (3.2.3), Simplified Logic Diagram

It will be noticed from Table 3-1 that the 51-counter-equals-15, -30, and -45 pulses do not perform any control functions. These pulses are used to produce the stop bits, one of which is required to complete each TTY character. (See Figure 3-22.) Since the stop bits are all 0 bits, they are not stored in the array and therefore must be generated by the TTY storage section. Either a 51-counter-equals-15, -30, or -45 pulse is generated after six clear-column pulses have been produced. Clear-column pulses shift the first six bits of each TTY character from the core array. The 51-counter-equals-15, -30, and -45 pulses therefore occur at the time that the seventh bit should be shifted from the array and entered in the OSR. Since these pulses are not used to clear a column, the first cores of the OSR retain a 0 bit, and this bit always completes TTY character.

The shift time pulses listed in Table 3-1 go to the shift-pulse generator circuit of the 51 counter, where they are collected in an OR circuit and transferred to the TTY control (see Figure 3-27). The output pulses of the 51 counter are comparatively long sawtooth-shaped pulses. These pulses are not acceptable for certain applications in this form and are therefore gated (at OD 3 time) in the shift-pulse generator of the 51 counter to provide standard 0.1 usec pulses.

51 COUNTER	DESTINATION	FUNCTION
1	Teletype core storage	Clear column 22
2	Shift-pulse generator, 51 counter	Shift time
2	Shift-pulse generator, 51 counter	Start high-speed shift
3	Teletype core storage	Clear column 1
4	Shift-pulse generator, 51 counter	Shift time
5	Teletype core storage	Clear column 7
6	Shift-pulse generator, 51 counter	Shift time
7	Teletype core storage	Clear column 8
8	Shift-pulse generator, 51 counter	Shift time
8	Shift-pulse generator, 51 counter	Stop high-speed shift
9	Teletype core storage	Clear column 9
10	Shift-pulse generator, 51 counter	Shift time
11	Teletype core storage	Clear column 10
12	Shift-pulse generator, 51 counter	Shift time
13	Teletype core storage	Clear column 11
14	Shift-pulse generator, 51 counter	Shift time
15	Not used	Stop bit
16	Shift-pulse generator, 51 counter	Shift time
17	Teletype core storage	Clear column 2
18	Shift-pulse generator, 51 counter	Shift time
19	Teletype core storage	Clear column 12
20	Shift-pulse generator, 51 counter	Shift time
21	Teletype core storage	Clear column 13
22	Not used	
23	Shift-pulse generator, 51 counter	Shift time
24	Teletype core storage	Clear column 14
25	Shift-pulse generator, 51 counter	Shift time
26	Teletype core storage	Clear column 15
27	Shift-pulse generator, 51 counter	Shift time
28	Teletype core storage	Clear column 16
29	Shift-pulse generator, 51 counter	Shift time
30	Not used	Stop bit
31	Shift-pulse generator, 51 counter	Shift time

Table 3-1. Destination and Function of 51-Counter Pulses

51 COUNTER	DESTINATION	FUNCTION
31	Shift-pulse generator, 51 counter	Shift time
32	Teletype core storage	Clear column 3
33	Shift-pulse generator, 51 counter	Shift time
34	Teletype core storage	Clear column 17
35	Shift-pulse generator, 51 counter	Shift time
36	Teletype core storage	Clear column 18
37	Not used	
38	Shift-pulse generator, 51 counter	Shift time
39	Teletype core storage	Clear column 19
40	Shift-pulse generator, 51 counter	Shift time
41	Teletype core storage	Clear column 20
42	Shift-pulse generator, 51 counter	Shift time
43	Teletype core storage	Clear column 21
44	Shift-pulse generator, 51 counter	Shift time
45	Shift-pulse generator, 51 counter	Begin search
46	Shift-pulse generator, 51 counter	Shift time
47	Not used	
48	Shift-pulse generator, 51 counter	Shift time
49	Not used	
50	Shift-pulse generator, 51 counter	Shift time
51	Shift-pulse generator, 51 counter	End search
51	Shift-pulse generator, 51 counter	Prime 51 counter

Table 3-1. Destination and Function of 51-Counter Pulses (Cont'd)

The 51-counter shift pulses and the TTY-FA-GT pulses used to gate the FA's are 2.5 usec in length, occurring between OD 2 and OD 3. These pulses are generated by the flip-flop in the 51-counter shift-pulse generator (Figure 3-27). The flip-flop is normally set at OD 2-91 time and is cleared at the following OD 3 time, unless the 51-counter-equals-51 pulse causes the OD 3 pulse to be inhibited. In this case, the shift pulse lasts an extra OD cycle (10 usec), causing the 51 counter to be cleared and causing a 1 to be primed into the first core of the 51 counter.

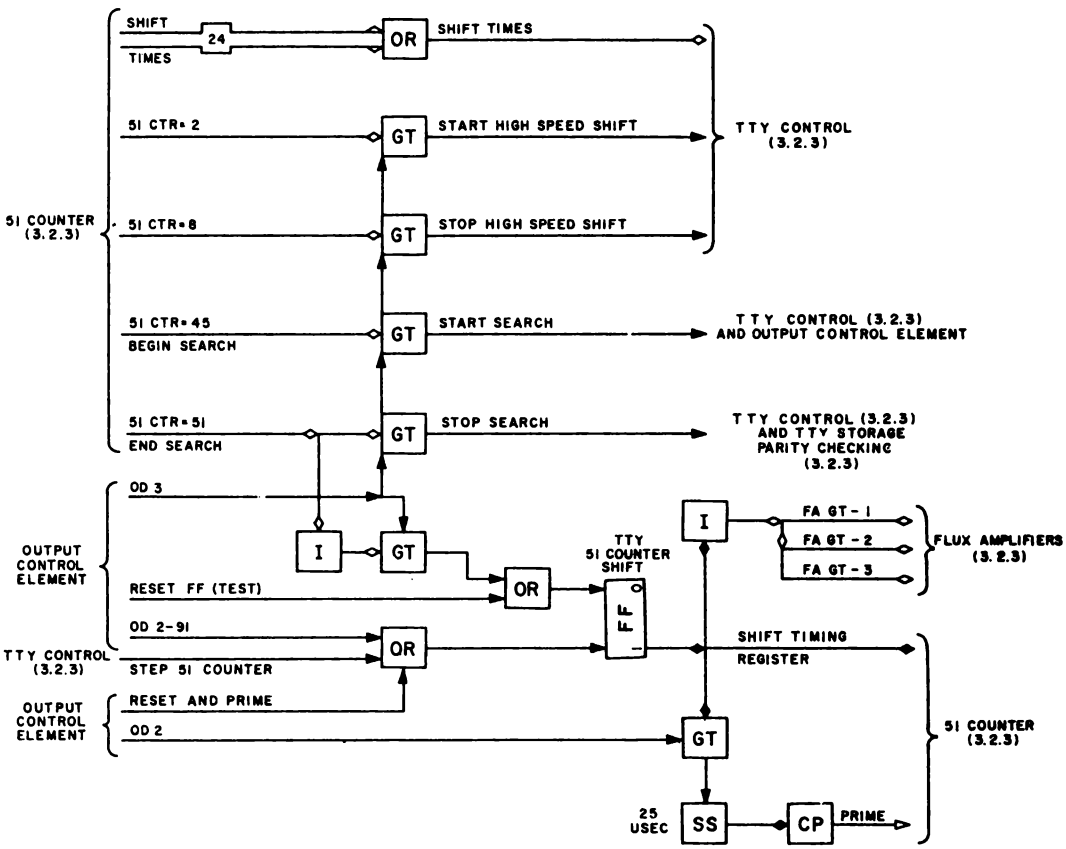


Figure 3-27. Shift-Pulse Generator, 51 Counter (3.2.3), Simplified Logic Diagram

c. Teletype Control (Refer to Figure 3-28)

The TTY control, shown in Figure 3-28, regulates the supply of shift pulses to the 51 counter and gates all shift pulses to the OSR and line register. Another function of the TTY control is sending search and not-search control levels to the read-in control of the output control element to coordinate the read-in cycle with the readout cycle.

The search TTY and not-search TTY levels are developed by the 1 and 0 sides, respectively, of the search flip-flop. This flip-flop is set by a 51-counter-equals-45 pulse, thereby developing the search TTY level, and reset by a 51-counter-equals-51 pulse, thereby developing the not-search TTY level. These levels start and terminate TTY search time. The TTY control sends OD 3-91 pulses to the OSR and line register as shift pulses only when the shift-time level is up. This level is raised at the 51-counter times specified in Table 3-1.

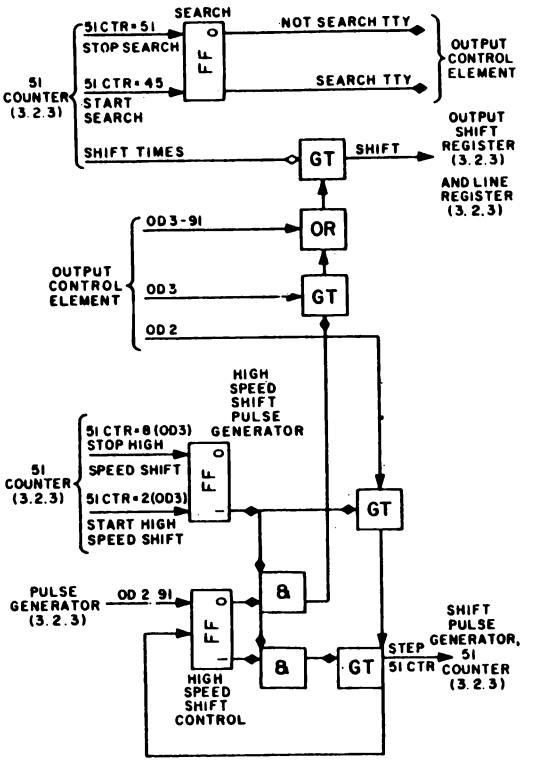


Figure 3-28. TTY Control (3.2.3), Simplified Logic Diagram

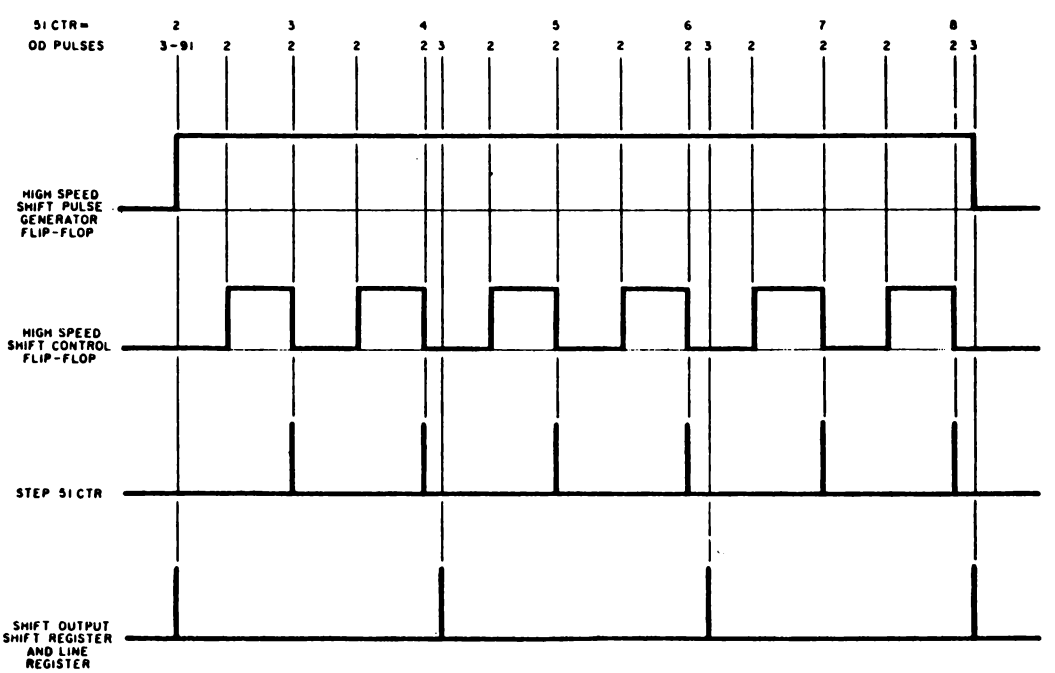


Figure 3-29, High-Speed Shift Timing

The TTY control also controls the high-speed shifting of the 51-counter, OSR and the line register. This is accomplished as explained below. (See Figure 3-29.)

The 51-counter-equals-2 (start high-speed shift) and the 51-counter-equals-8 (stop high-speed shift) gates pulses respectively set and clears the high-speed shift pulse generator flip-flop. When this flip-flop is set, OD 2 pulses are enabled to complement the high-speed shift control flip-flop. This latter flip-flop is always reset by an OD 2-91 pulse before the first complementing OD 2 pulse is applied. The first complementing pulse applied, therefore, sets the high-speed shift control flip-flop. The 1 side of this flip-flop conditions a gate which is pulsed by OD 2 pulses. The next OD 2 pulse is passed by this gate as a step-51-counter pulse, and this pulse shifts the 51 counter to 51-counter-equals-3. The same OD 2 pulse simultaneously resets the high-speed shift control flip-flop. The 0 side of this flip-flop now conditions a gate which is pulsed by OD 3 pulses, and the next OD 3 pulse is passed by this gate and applied to a gate which is conditioned by the shift times level. This level is up at the 51-counter times specified in Table 3-1. During the high-speed shifting, the shift times level is up at 51-counter-4, -6, and -8 time only. Since the 51 counter is now at 51-counter-equals-3, the OD 3 pulse is not passed.

The complementing of the high-speed shift control flip-flop, with the subsequent shifting of the 51 counter continues at a 50-kilocycle rate until 51-counter-8 time. During this time, an OD 3 pulse is sent as a shift pulse to the OSR and line register at the times when the high-speed shift control flip-flop is reset during 51-counter-4, -6, and -8 time. At these times the shift times level is up. At 51-counter-8 time, the high-speed shift-pulse generator is reset by the 51-counter-equals-8 pulse, and the high-speed shifting is thus terminated.

5. Teletype Readout

a. General

Readout of the TTY storage section must be performed to meet the standard TTY machine requirements. The readout operation is controlled by timing signals generated in the 51 counter and the TTY controls. Figure 3-30 shows the logical flow of data during readout. There are five identical readout channels, only one of which will be described in this discussion. Bits are read out from each array register serially, through FA's and into a 3-core OSR. From the OSR, the bits enter a line register (a flip-flop) which controls a relay that holds the line in an open or closed position depending upon whether the bit is a space (1) or a mark (0).

b. Core Array Readout

Each TTY output word is read out of the TTY core storage array by columns. There are 22 columns in the core array, of which 19 are active and 3 are spares. (See Figure 3-31.) The 19 active columns are pulsed by clear-column pulses, applied by the TCD's located in the 51-core shift register. Each time a column is pulsed, the bits stored in its cores are shifted from the core array in parallel to the FA's. The bits from each column are composed of one bit from each of the 25 output words that are stored in the array. Table 3-2 shows the assignment of bits by columns, the 51-counter

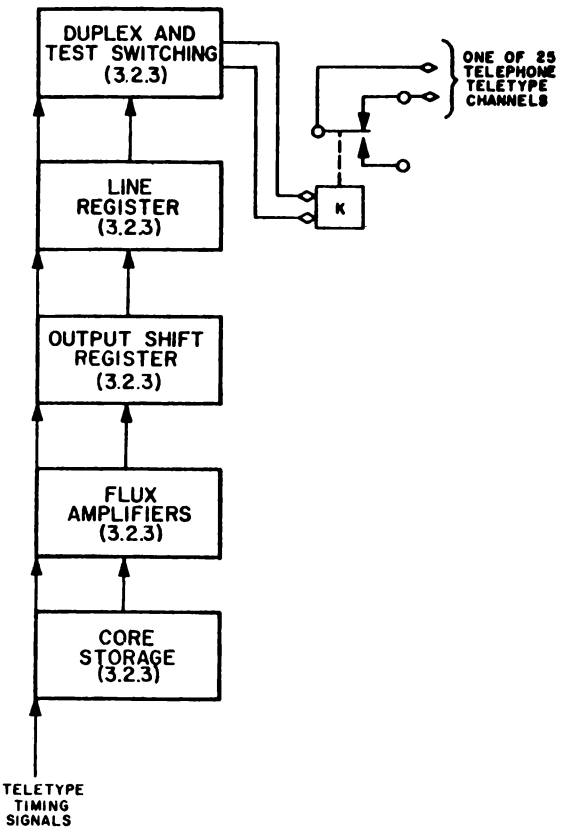


Figure 3-30. TTY Readout Flow of Data, Block Diagram

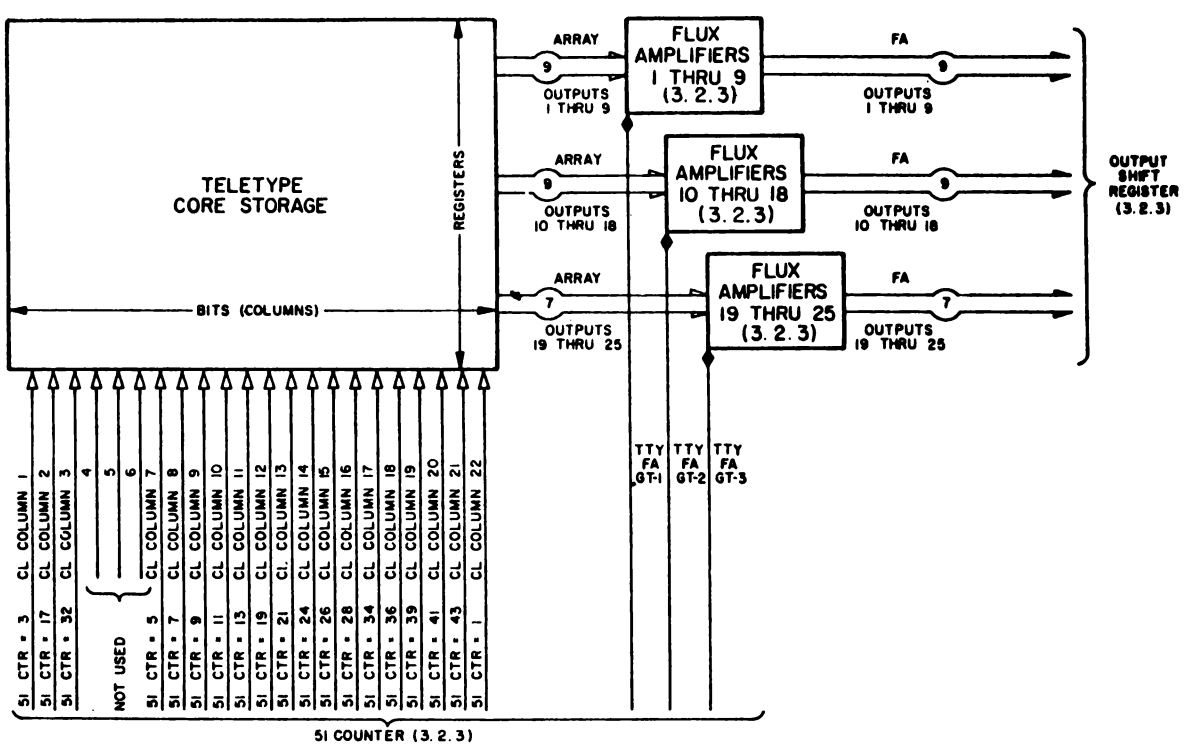


Figure 3-31. TTY Core Storage Readout, Simplified Block Diagram

BIT	CORE STORAGE COLUMN	READOUT AT 51 COUNTER	ORDER OF READOUT OF COLUMNS	RELETYPE BIT
RS	1	3	2nd	Start A
BB2	2	17	8th	Start B
BB1	3	32	14th	Start C
R1	7	5	3rd	A-1
R2	8	7	4th	A-2
R3	9	9	5th	A-3
R4	10	11	6th	A-4
R5	11	13	7th	A-5
R6	12	19	9th	B-1
R7	13	21	10th	B-2
R8	14	24	11th	B-3
R9	15	26	12th	B-4
R10	16	28	13th	B-5
R11	17	34	15th	C-1
R12	18	36	16th	C-2
R13	19	39	17th	C-3
R14	20	41	18th	C-4
R15	21	43	19th	C-5
P	22	1	1st	P

Table 3-2. Assignment of Bits in TTY Core Storage

pulse that clears each column, the order of readout, and the significance of each bit in the core storage.

c. Flux Amplifiers (FA's)

Each of the 25 array output pulses from the TTY core storage array is applied to an FA. A 1 bit is represented by a pulse and a 0 bit is indicated by the absence of a pulse. Separate groups of the 25 FA's are gated as shown in Figure 3-31 by gating levels 1, 2, and 3. These gating levels are 2.5 usec negative pulses employed to prevent noise and spurious signals from passing through the FA's. They are produced in the 51-counter shift-pulse generator simultaneously with each shift of the 51-counter. Since alternate 51 counter shifts generate clear-column pulses which read out columns of the core array, the array outputs are applied to the FA's during the 2.5 usec that the FA's are gated and operative. The FA's, after amplifying and stretching the array output pulses, send the pulses to the OSR as FA outputs. The outputs from the FA's are sent over 25 lines labeled FA output 1 through FA output 25, respectively.

d. Output Shift Register

The purpose of the OSR (Figure 3-32) is to provide a 3-shift-buffer so that there is no delay or pause on the TTY channel during TTY search time.

The OSR is made up of 25 3-core shift registers. One shift register is provided for each of the 25 TTY channels used. Each CSR is a tape core register identical to those used in the G/A-FD OSR. The information bits, as they are shifted out of the core storage array and amplified in the FA's, are read into the first core of each register. After receipt of each group of bits, and prior to receipt of the next group, the CSR's are shifted. In this manner, the bits from a register in the core array are shifted serially through each 3-core shift register to a line flip-flop in the line register.

Output shift register shift pulses are produced by the flip-flop shown in Figure 3-32. This flip-flop is set upon receipt of an OD 3 shift pulse from the TTY control. The level developed by the 1 side of this flip-flop is simultaneously applied to the shift registers as a shift signal and as a conditioning level to a gate. After 2.5 usec, an OD 4 pulse passes the gate and clears the flip-flop. Thus, the level applied to the registers and gate falls. In this manner, a 2.5 usec shift pulse is developed for each OD 3 shift pulse received from the TTY control. The OD 3 shift pulses are applied when a shift times level is developed at the times specified in Table 3-1.

Each bit shifted from the last core of a register is applied as a conditioning level to a gate. This gate is pulsed by each OD 4 pulse which clears the flip-flop. If the bit shifted out of the register is a 1, the gate is conditioned and the OD 4 clear pulse is sent to a line flip-flop in the line register. Note: Refer to Figure 3-33.

e. Line Register

Figure 3-33 shows the 25-line registers and their associated relay circuits. The line flip-flops are set by each 1 bit that is read out of the OSR, just after the shift. The flip-flops are then cleared by the shift pulse which shifts the next bit out of the OSR.

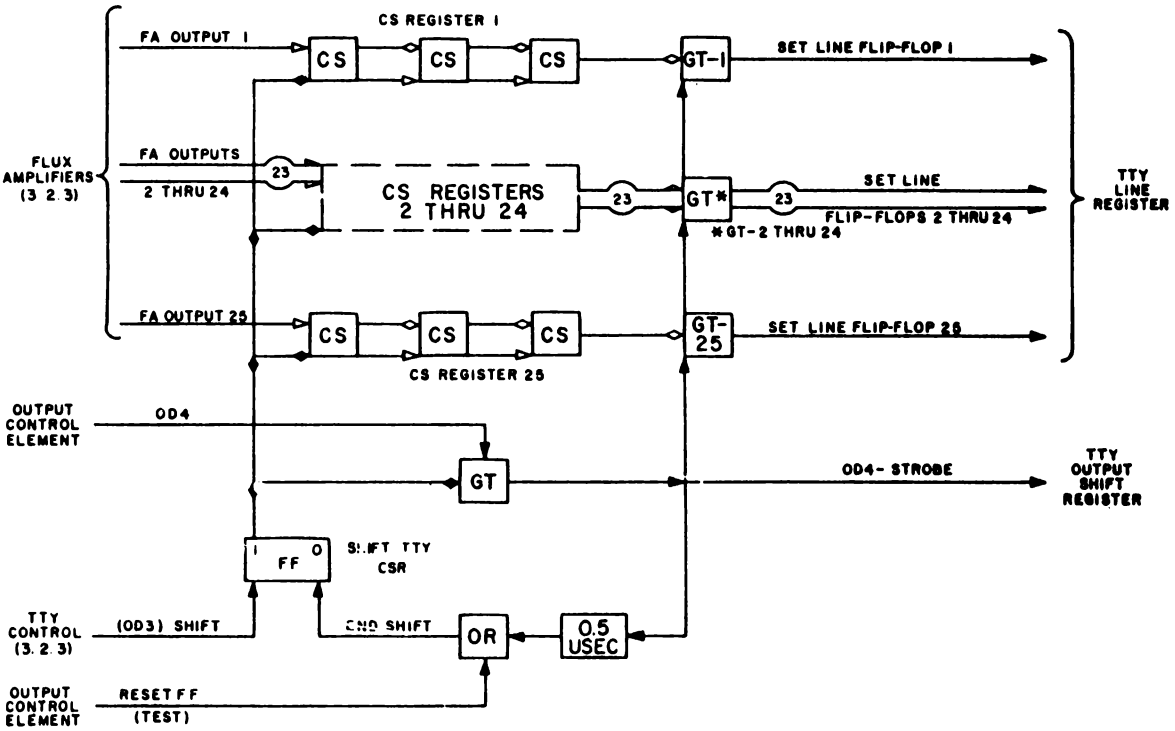


Figure 3-32. TTY Output Shift Register (3.2.3), Simplified Logic Diagram

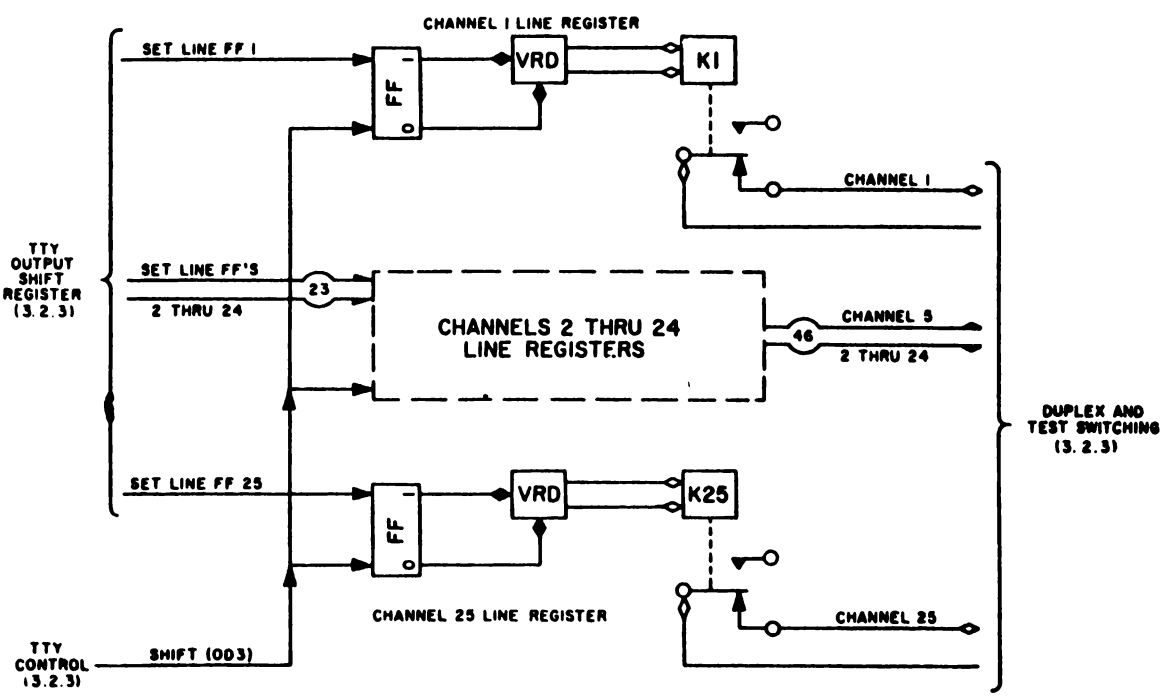


Figure 3-33. Line Register (3.2.3), Simplified Logic Diagram

The relay follows the action of the line register. When the flip-flop is in the 1 state, the relay opens the TTY channel. Thus, a 1 bit causes an open line or space. Note: Refer to Figure 3-34.

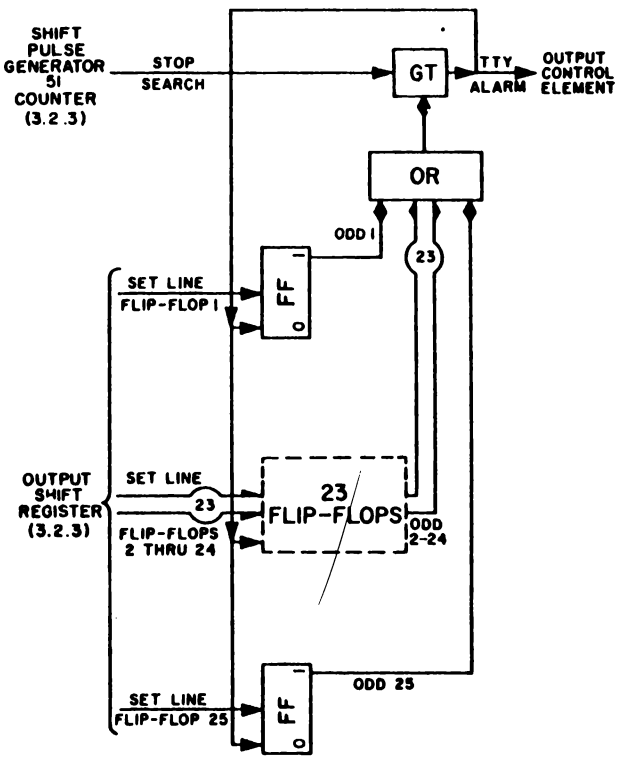


Figure 3-34. TTY Storage Parity Checking (3.2.3), Simplified Logic Diagram

6. Message Check

The function of the storage parity checking circuit, shown in Figure 3-34, is to transmit a TTY parity alarm signal to the alarm control in the case of a storage parity alarm. This circuit is similar to the G/A-FD storage parity checking circuit.

If any of the parity check flip-flops is set at 51-counter-51 time, the gate which is conditioned by the 1 side of these flip-flops will pass the stop-search pulse applied to it at this time. This pulse will clear the set flip-flops. Readout now starts, and as bits are shifted out of the OSR's and into the line flip-flops, they are also transmitted to the parity storage checking circuit where they complement the parity check flip-flops. Since the total number of 1's in the TTY message, including the parity bit, is even, all flip-flops should be in the 0 state at the following stop-search time. The 1 sides of the flip-flops are sampled, and if any flip-flops are found to be in the 1 state, the TTY

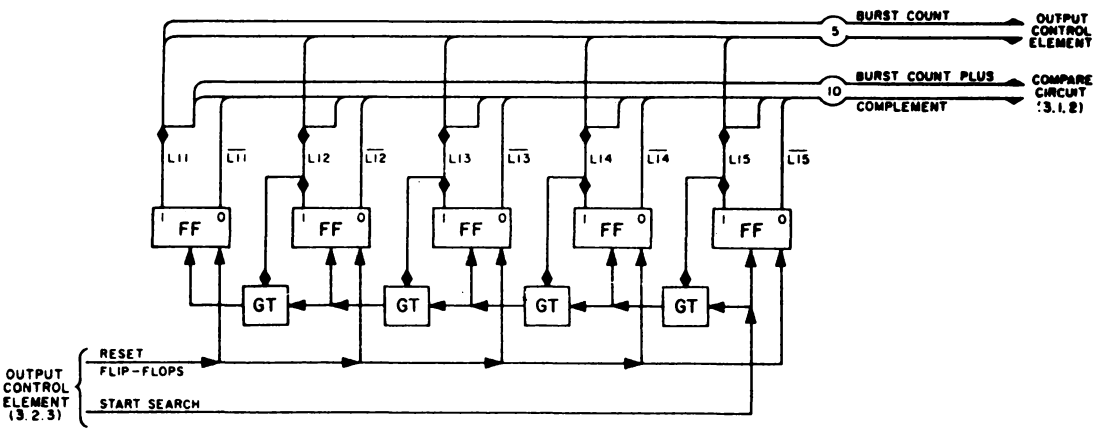


Figure 3-35. TTY Burst Counter (3.1.2), Simplified Logic Diagram

alarm is transmitted. This alarm also clears the set flip-flops in preparation for the next parity check.

7. Burst Sequence and Timing

The TTY burst count and comparison are accomplished within the TTY burst counter and compare circuits. The TTY burst sequence and timing are identical to the burst sequence and timing operation of the G/A storage section, except for the number of bits used. The TTY burst count and compare circuits use a 5-bit burst number; the TTY burst counter is composed of five flip-flops. This is a standard flip-flop counter, having a scale of 32. The burst counter is stepped at start search (51-counter-45 time). Figures 3-35 and 3-36 are simplified logical block diagrams of the TTY burst counter and the comparison circuits, respectively.

8. Switching

The TTY test and duplex switching circuits control the TTY output of the Output System of each computer. The switching circuits contain relays which provide for the switching of each of the 25 TTY messages. However, the relay circuits for each message are identical. For this reason, Figure 3-36A shows a simplified diagram of the TTY test and duplex switching circuits for only one TTY message.

The relays provided by the TTY test and duplex switching circuits are controlled so that only the Output System of the active computer is presented to the telephone line terminal equipment. Relays are also provided to enable the Output System on standby status to be switched to the TTY test busses. These relays are operated during test operations only.

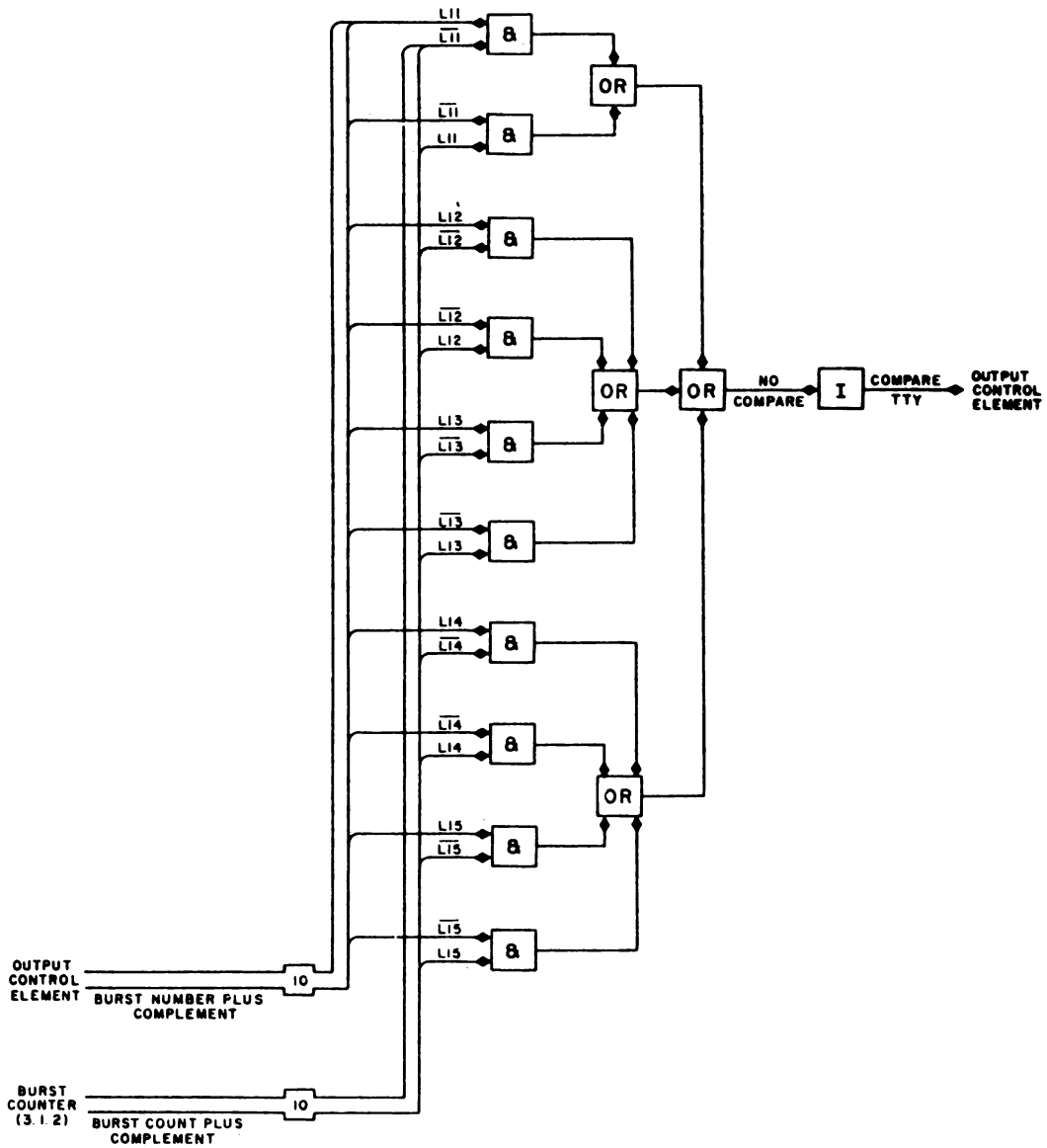


Figure 3-36. Comparison Circuit, Tletype Burst Counter (3.1.2), Simplified Logic Diagram

SUMMARY QUESTIONS

1. A TTY signal consists of seven consecutive intervals. The first interval is the _____ interval and the 7th interval is the _____ interval. The remaining five intervals comprise a code specifying a character or command.

2. There are two possible conditions of the TTY line, i.e., closed is a _____ and open is a _____.

3. Start bits must be transmitted as open line (1 bits). The three start bits in the TTY message word are _____, _____, and _____.

4. The search time interval for TTY is from 51-counter- _____ to 51-counter- _____.

5. Readout time is from 51-counter _____ to 51-counter- _____.

6. The parity bits of a TTY message word while in storage is destroyed by _____ _____.

7. The three stop bits are generated when 51-counter- _____, _____, and - _____.

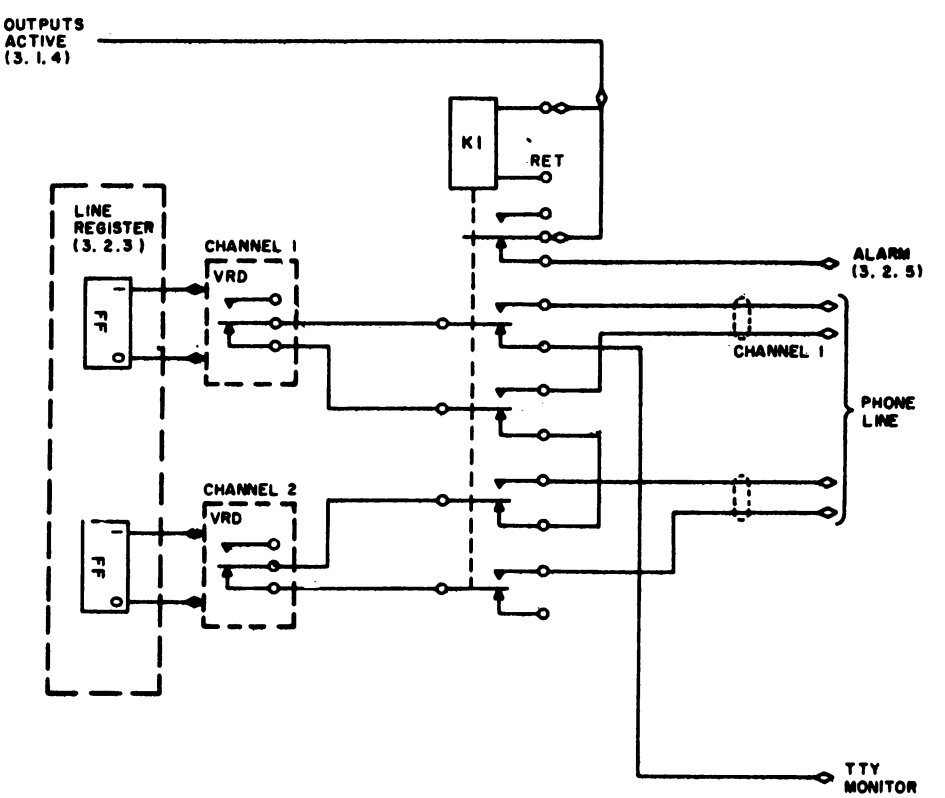


Figure 3-36A. TTY Duplex and Test Switching for Messages 1 and 2 (3.2.3), Simplified Logic Diagram

8. How many TTY characters per TTY word?

9. How many bits per TTY character?

10. How many Busy Bits are used with a TTY word?

11. Right sign must always be a "1." (T/F)

12. What is the maximum number of words that can be read into the TTY Ferrite Array in a Burst Period?

13. How many cores in the counter used to control TTY timing?

14. Each TTY character has its own start and stop bits. (T/F)

15. How many bits are loaded into the array with each TTY word?

16. What are the bits referred to in question No. 15?

17. What is the function of the TTY OSR?

18. How long is the 51-counter shift FF set during a normal reset operation?

19. When power is brought up, how long is the 51-counter shift FF set?

20. What is the name of the relay used with the line registers?

21. How long is a stop bit?

22. How long is the "P" bit in line FF's?

23. Parity is checked for Add "0" when the 51-counter-?

24. The Line Regs are loaded at what OD time?

25. The TTY OSR is always shifted at even counts of the 51-counter. (T/F)

26. The High Speed Shift Control FF in 33KJ (5B) must be cleared in order to shift the OSR. (T/F)

27. What addresses would be affected if 33GC H_8 were open? (3.2.2-8B)

28. How many outputs of the 51 counter are used for readout of the array?

29. 33 JT F3 open (3.2.3-5A) message would be transmitted correctly with an occasional TTY output alarm. (T/F) Use one word in.

30. If in putting outputs to active status one of the active relays fails to pick an output switching alarm is generated. (T/F)

31. TTY transmits three characters every 1/2 second. (T/F)

G/A-TD Storage Section, Dual Channel Operation

1. The G/A-TD output storage section assembles output words received in parallel form from the output control element into messages, and then transmits these messages serially over telephone data channels to control manned interceptors. These messages are transmitted at a 1,300-pps rate. A simplified diagram of the G/A-TD storage section is shown in Figures 3-37 and 3-38.

Three G/A-TD messages may be transmitted during a G/A-TD burst period. Each message is composed of four output words which are separated in groups of two words and transmitted over separate telephone channels to manned interceptors, via data-link transmitters. Each G/A-TD data link transmitter that is located within a given area operates on the same assigned frequency. Selection of a particular data-link transmitter is established by the site address portion of a G/A-TD message. If a G/A-TD message is addressed to a particular aircraft in a group of interceptors, only that aircraft will take action on the transmitted message.

A parity check is performed on each output word to determine whether the original contents of the output word have been altered. There are an odd number of 1 bits present in each G/A-TD word, as opposed to the even number of 1 bits required in all G/A-FD, BOMARC, G/G, and TTY words.

The time required to read out all three G/A-TD messages in a G/A-TD core storage array is 90 ms. This is about equal to G/A-TD search time which is 86.2 ms. To eliminate the waste of telephone line time which would result if the line were not used during search time, two core storage arrays are included in the G/A-TD storage section. One array receives information while the contents of the other array are read out to the telephone line channels. Since two storage arrays are employed and search time for one storage array occurs simultaneously with the readout of the other array, messages may be transmitted almost continuously.

2. System Operation

The G/A-TD storage section is logically divided into storage readout, control, message check, burst counting and compare, conversion and switching circuits, as shown in Figure 3-37. These circuits perform functions similar to the corresponding circuits of the G/G, and TTY storage sections. However, since the G/A-TD storage section and word makeup differs somewhat from the other storage section, a discussion of the G/A-TD circuits follows:

a. Counter Operation

The control circuits consist of the G/A-TD control, the 15 counter and the 17 counter. The two counters control the timing for the G/A-TD storage section. A brief discussion of these counters follows: The 17 counter is shifted at two rates, a 25-kc (40 usec) fast-shift rate and the normal 1,300-cps (770-usec) slow-shift rate. The 17 counter controls the shifting of the 15 counter. During one burst period, the 15 counter is shifted through a complete cycle of operation. A G/A-TD operational cycle consisting of read-in and readout of the two core storage arrays is described in subsequent paragraphs. The G/A-TD read-in interval and the readout interval for a single core array

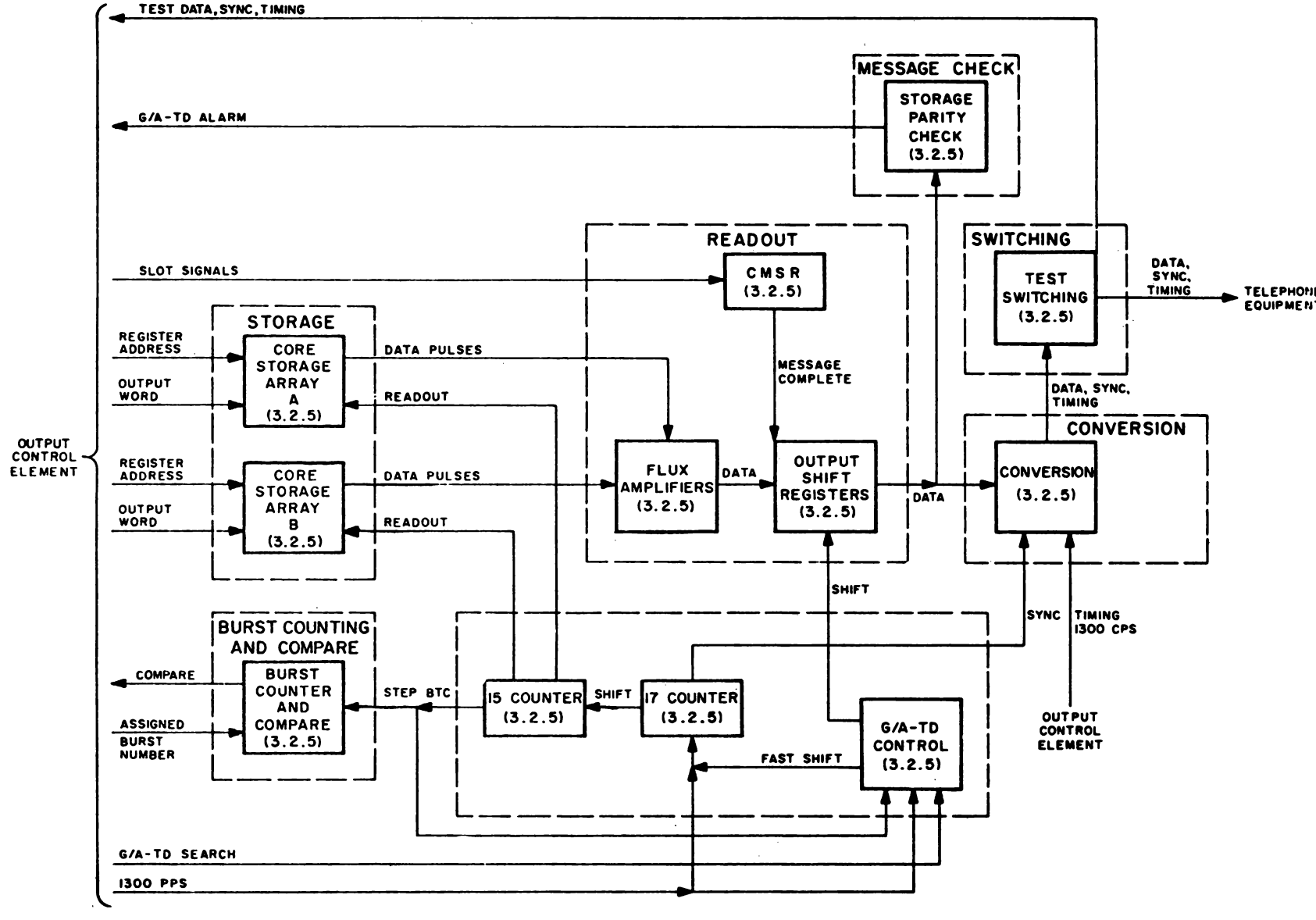


Figure 3-37. G/A-TD Output Storage Section, Simplified Block Diagram

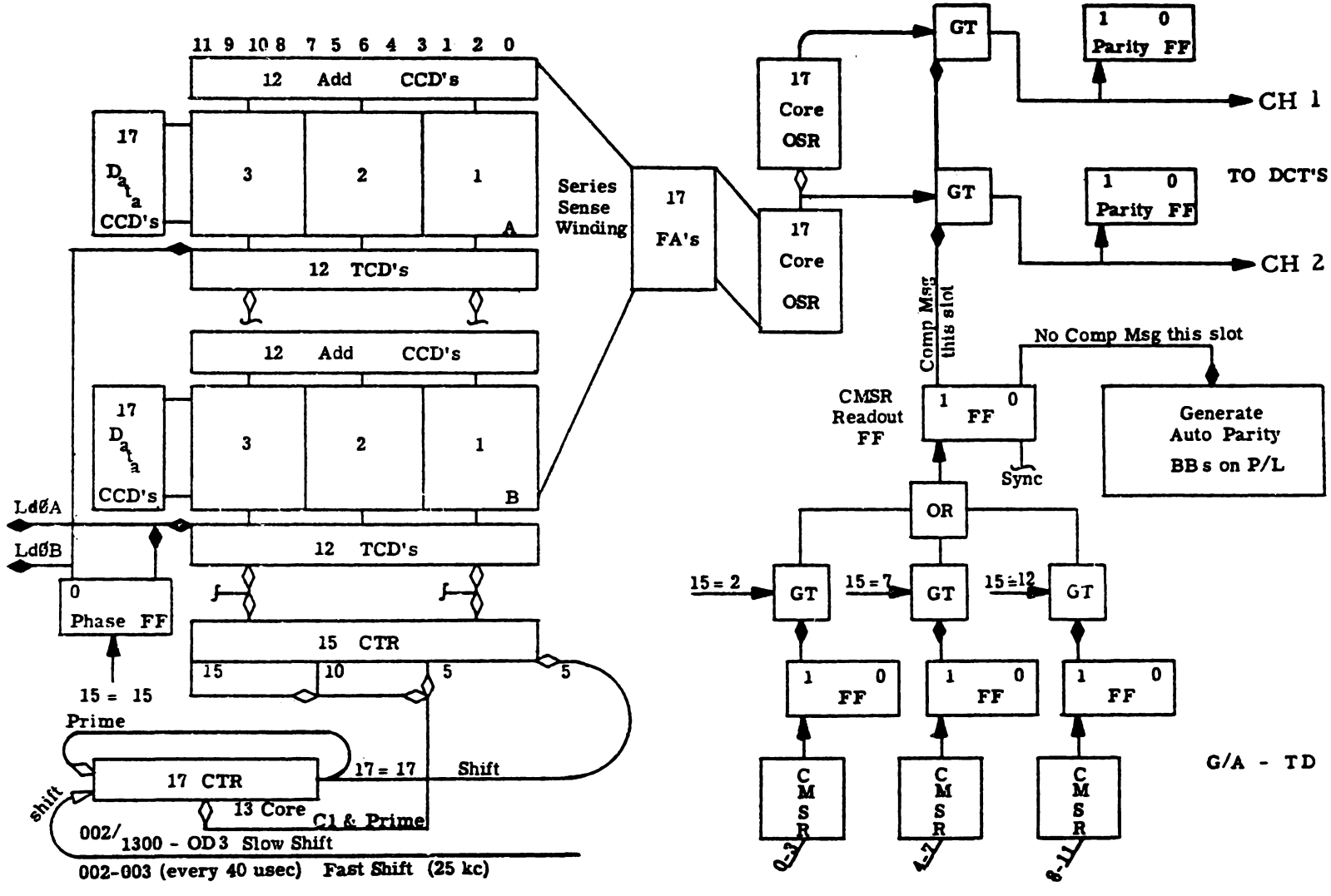


Figure 3-38. G/A-TD Block Diagram

take place during successive burst periods. Thus two G/A-TD burst periods are required for one G/A-TD core storage array to complete a cycle of operations. In actual operation, the read-in and readout functions occur simultaneously; as one core array is being written into, the other array is being simultaneously read out.

b. Read-In

The read-in operation of the G/A-TD storage section is similar to the read-in operation described for the G/G storage section except for the differences stated below.

In general, all counters are reset and primed in order to control the read-in of the G/A-TD word in the output section. The G/A-TD burst period begins at the first shift of the 15 counter. Search time for the storage section also begins at this time. The search level signals the G/A-TD output control element that read-in of the G/A-TD words can now take place. The G/A-TD output word to be read in is made up of bits RS through R15 plus an odd parity bit. It is to be noted that only in the G/A-TD section is an odd parity used. Like the G/G section, a pulse is sent to the CMSR to count the number of words loaded into each of the three message slots in a core storage array. One G/A-TD message slot contains four words.

The read-in of the G/A-TD words is completed before 15-counter-15 time. At 15-counter-15 time the G/A-TD control generates a not-search level and a shift-phase level. The not-search level prevents the output control element from writing into any more core registers. The shift-phase level switches core arrays so that the array just read into will be read out during the next burst period.

c. Readout

Readout of the core storage array that was written into the previous cycle starts at 15-counter-1 time. In the G/A-TD storage section, two OSR's are used. At 15-counter-1 time, a clear-column pulse is generated to read out the first column in one of the selected storage arrays. The column of bits in this array is read out and sensed by the FA's where they are amplified to prime the cores of the first OSR. In the interval between 15-counter-1 and 15-counter-2 time, the word is fast-shifted from OSR 1 to OSR 2.

At 15-counter-2 time, the second clear-column pulse is generated to read out the second column of bits from the array into OSR 1. There are now two G/A-TD words contained in the OSR's; that is, register address 0 is in OSR 2 and register address 2 is in OSR 1. The latter is then shifted out in serial fashion only if there is a complete G/A-TD message made up of four words in a slot. This prevents the transmission of an incomplete G/A-TD message.

In the interval between 15-counter-2 and 15-counter-3 time the words contained in OSR 1 and OSR 2 are shifted out serially under the control of the 17 counter to the conversion equipment, to the storage parity checking circuits, and to the test equipment section. In the storage parity checking circuits, the words are examined for proper parity (odd). If parity is even, a G/A-TD output alarm will be generated. Nevertheless, the G/A-TD word is allowed to go out over the phone lines regardless of output word parity.

In the conversion equipment, the information is made compatible with the phone line equipment. The test equipment circuits make use of the information received only if a unit-loop-test or computer-loop-test condition exists.

At 17-counter-17 time, the last bits of the G/A-TD words are read out of both OSR's; at the same time, a pulse is gated to the 15-counter shift flip-flop. The output of this flip-flop will generate the next clear-column pulse at 15-counter-3 time. This, in effect, transfers the third G/A-TD word (register address 1) to OSR 1, whereupon it will be fast-shifted under the control of the 17 counter to OSR 2. When the next clear-column pulse is generated at 15-counter-4 time, the fourth G/A-TD word (register address 3) is read out of the core storage array into OSR 1. The third and fourth G/A-TD words are read out of the OSR's under the control of the 17 counter; this, then, completes the readout operation cycle for one complete G/A-TD message slot.

3. Storage

a. Core Storage Arrays

The output words comprising the G/A-TD messages are stored in ferrite core arrays. Each G/A-TD output word is 17 data bits in length and is stored in one register column of the array. The array has 12 columns and 17 rows and can therefore store 12 output words. (See Figure 3-39.)

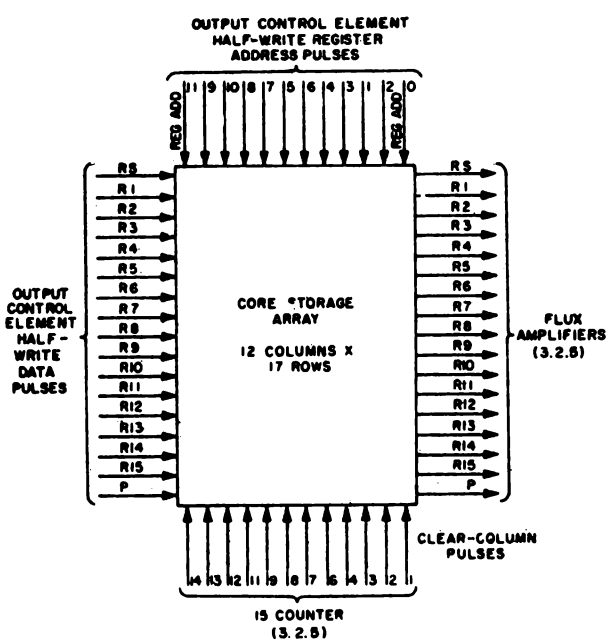


Figure 3-39. G/A-TD Core Storage Array, Simplified Logic Diagram

Two identical arrays are included to provide more efficient use of telephone channels. Each array is written into column by column and read out column by column; in this fashion, the G/A-TD storage array is read out word by word rather than bit by bit as in the TTY, and G/G storage section. As each word is transferred to the core storage array a half-write current is applied to the register address winding of the column in which that word should be written. Simultaneously, right drum word half-write current pulses are applied to those row windings in which a 1 should be recorded. During readout, a read current pulse is applied to a clear-column winding. Each core in the column receives a full read current, with each core output appearing on the array output winding for its row. Corresponding row array output windings in the two arrays are wired in series. (See Figure 3-38.) No interference between matrices results, since only one array is read out at a time through use of gated TCD's.

b. Core Array Read-In

Figure 3-38. During each burst period, G/A-TD message words are written into the core storage array which is not being read out. The right drum word with odd parity is applied by the output control element of the core storage array as half-write pulses on those drum word lines whose bits are 1's. The row in the array on which the word is written is specified by the register address contained in the left drum word. Thus, message assembly is accomplished by the assigned burst number and the register address. Since the search period for the OB fields is approximately 86.2 ms, read-in to one array can be completed during the 90-ms readout time for the other array.

The selection of an array for read-in is accomplished by the output control element. The G/A-TD control supplies that element with information on which array is being read out. The output control element, in turn, routes words for read-in into the other array.

4. Control

a. General

While many of the control functions of the G/A-TD output storage section are managed by the output control element, certain functions unique to the section are managed by control circuits within the section. The control circuits for G/A-TD are the 17 counter, the frequency divider, the fast-shift circuits, the 15 counter, and associated control circuits.

b. 17 Counter

The 17 counter, as shown in Figure 3-40, is a 17-core ring counter which is cleared, primed, and then continuously stepped at 1300-pps and also at a 25-kc rate (fast shift). The outputs of this counter are used to control certain functions in the G/A-TD storage section. The controlled functions are:

(1) Generation of the G/A-TD sync pattern.

(2) Stepping of the 15 counter.

(3) Fast and slow shifting of G/A-TD words into and out of the OSR's.

(4) Generation of parity bits to the phone line in the absence of a G/A-TD message or an incomplete message from the OB drum fields.

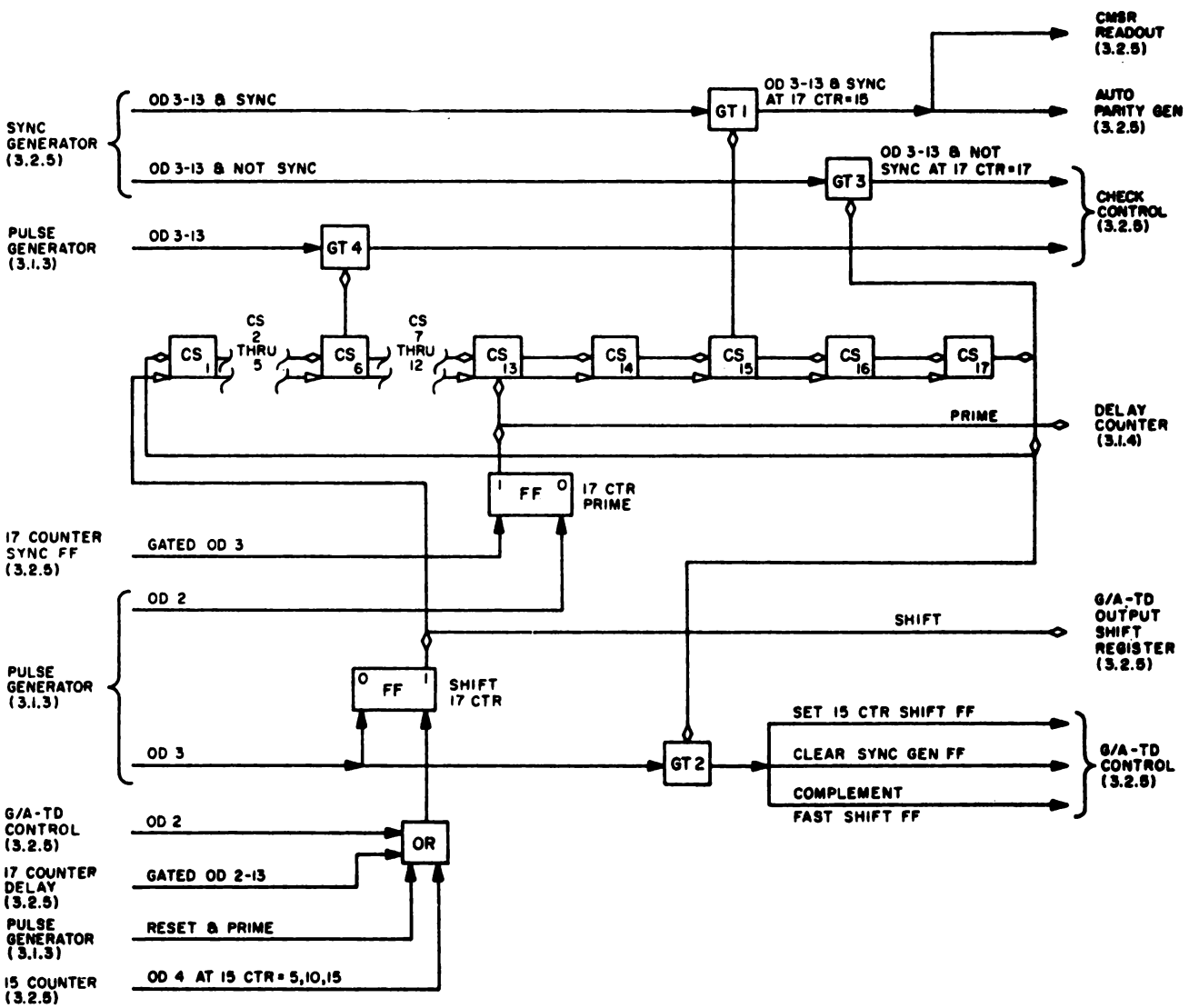


Figure 3-40. G/A-TD 17 Counter (3.2.5), Simplified Logic Diagram

At the start of system operation or after a shutdown or test operation, the output control element sends an OD 4 reset-and-prime pulse via OR 1 to the 17-counter shift flip-flop and the G/A-TD control. This OD 4 pulse, in conjunction with the following OD 3 pulse, allows the 17-counter shift flip-flop to produce a 7.5 usec reset level which

clears (resets) the 17 counter and both OSR's. This reset level (7.5 usec) is again generated whenever the 15 counter is stepped to 15-counter-5, -10, and -15. The latter reflects those times when a G/A-TD message (four words) has been read out of the OSR's to the phone lines. This same OD 3 pulse is gated to set the 17-counter prime flip-flop, which is normally cleared by the following OD 2 pulse. Setting of the 17-counter prime flip-flop generates a level to prime a 1 into the 13th core of the 17 counter (Figure 3-40). This priming allows for the generation of the G/A-TD sync pattern (00S00) that is required at the beginning of each G/A-TD message. The 1 bit is then shifted from the 13th core to the 14th core of the 17 counter; at the same time, both OSR's will also be shifted by 2.5 usec shift pulses which are generated from the 17 counter shift flip-flop. During a normal shift cycle, this flip-flop is set by gated OD 2-13 pulses and cleared by the following OD 3 pulses. However, since no information is present in either OSR, the first 0 bit of the G/A-TD sync pattern is now generated. When the 17 counter is shifted to 17-counter-14 time, another 0 is sent to the phone lines. At 17-counter-15 time, GT 1 is conditioned to pass an OD 3-13 and sync pulse to set both G/A-TD output sync flip-flops in the DCT's thus providing the synchronizing pulse of the sync pattern. In addition, the gated OD 3-13 and sync pulse clears the automatic parity bits generation flip-flop, thus preventing the generation of spurious 1 bits on the phone line. Successive stepping of the 17 counter to 17-counter-16 and -17 time generates the remaining 0 bits of the sync pattern.

After the 17 counter steps to 17-counter-17, it returns to prime a 1 bit in the first core of the 17 counter. Also at this time, GT 2 is conditioned to pass an OD 3 pulse to complement the fast shift flip-flop to the set side. Since the sync pattern has been generated, this same gated OD 3 pulse will clear the sync generation flip-flop and cause the 15-counter shift flip-flop to be set. This, in effect, causes the 1 bit located in a core of the 15 counter to be shifted to its succeeding core.

When the 17 counter is shifted to 17-counter-6 time, a level will be generated to condition GT 4. Conditioned GT 4 will pass an OD 3-13 pulse which is sent to the phone lines as an odd parity bit in lieu of G/A-TD words when the latter are absent from the phone lines.

c. Frequency Divider

The G/A-TD frequency divider circuit shown in Figure 3-41 is a 2-stage flip-flop counter which is used to fast-shift the 17 counter and both G/A-TD OSR's at a 25-kc rate.

As shown in Figure 3-40, OD 2 pulses are used to step the 17 counter. The operation of the counter is such that every fourth OD 2 pulse is gated to the fast-shift circuit. Hence, it can be seen from the figure that the frequency divider circuit supplies OD 2 pulses at a 40-usec rate (25 kc) to the fast-shift.

d. Fast-Shift Control

As previously mentioned in 2.c., readout of the G/A-TD word is accomplished by transferring a complete G/A-TD word out of the core storage array and into OSR 1. This G/A-TD word must then be shifted serially into OSR 2 before the following OD 3-13 time to prevent spurious data from appearing on the phone lines and

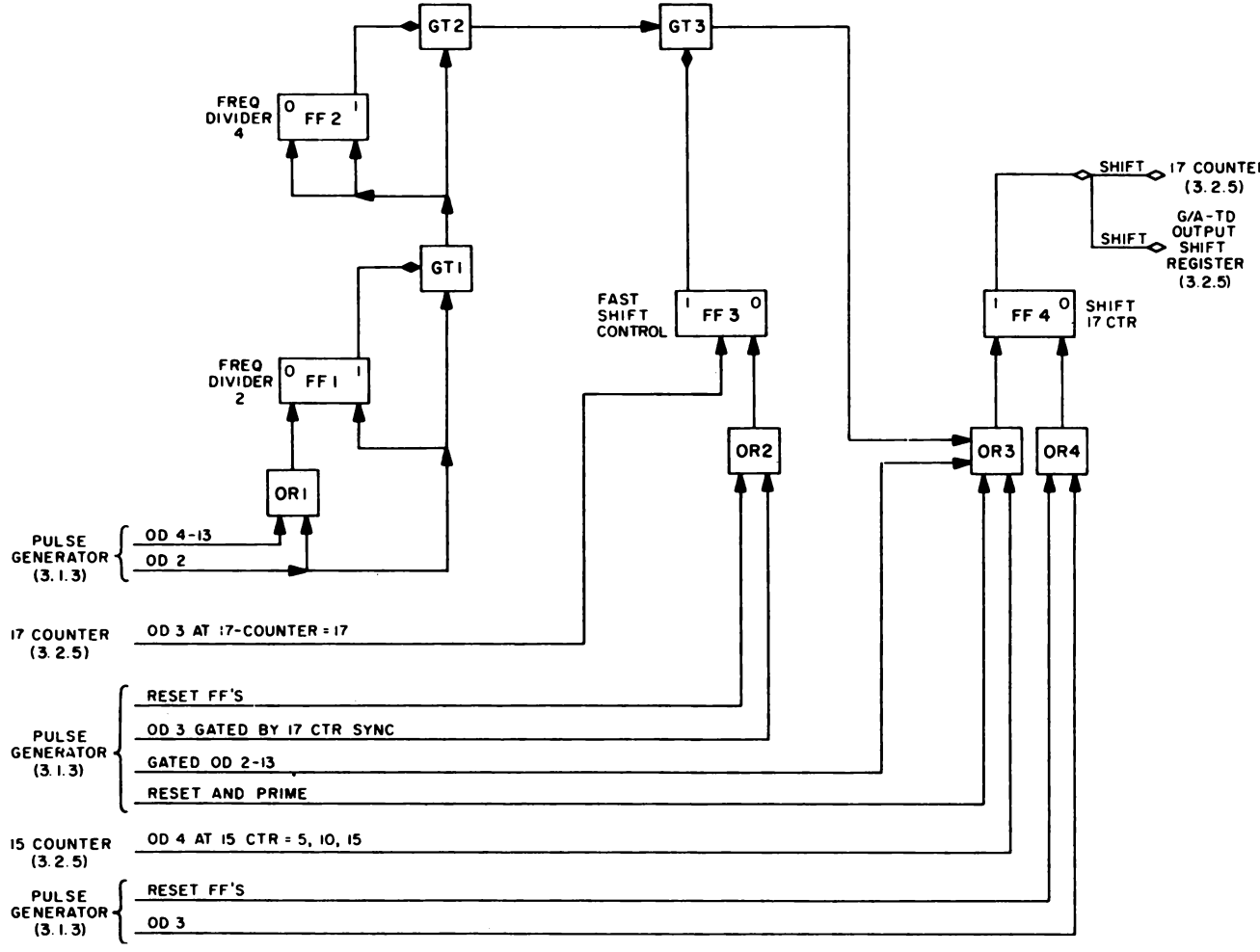


Figure 3-41. G/A-TD Frequency Divider, Fast-Shift Control, 17 Counter Shift Circuits Simplified Logic Diagram

to ensure that OSR 1 will be clear to receive the next incoming G/A-TD word from the core storage array. The fast-shift circuit (Figure 3-41) described below enables the above word transfer to be accomplished during the required time.

As shown in Figure 3-41, at 17-counter-17 time the sync pattern has been generated and the OD 3 pulse, which is now an OD 3-at-17 counter-17 pulse, is passed to complement the fast-shift flip-flop to the set side. The output of the set side of this flip-flop conditions GT 3, which is strobed by OD 2 pulses occurring at a 40-usec rate (25 kc) from the frequency divider.

These gated OD 2 pulses set the 17-counter shift flip-flop via OR 3. This flip-flop is cleared at the following OD 3 time; therefore, the 17 counter and both OSR's are fast-shifted through the complete 17 counter cycle. When the 17 counter is at 17-counter-17 time, an OD 3 pulse is passed to complement the fast-shift flip-flop to the clear side, thus ending the fast-shift operation. A timing chart is presented in Figure 3-43 to better illustrate the timing of the fast-shift control circuit.

e. 15 Counter

The 15 counter, as shown in Figure 3-42, is a 15-core shift register which is cleared, primed, and then shifted by an OD 3 pulse at 17-counter-17. The outputs of this counter are used for controlling certain functions in the G/A-TD storage section. These functions are:

(1) Initiating the start of the G/A-TD search period.

(2) Stepping the G/A-TD burst time counter.

(3) Controlling the readout of each column in two arrays.

(4) Initiating the generation of the sync pattern for each succeeding G/A-TD message by resetting and priming the 17 counter.

At the start of the operation, the 15 counter shift flip-flop is set by an OD 3 pulse at 17-counter-17 time. The 15-counter shift flip-flop is cleared by a following OD 4 pulse. Thus, the flip-flop generates a 2.5 usec shift pulse to shift the 1 bit from core 1 to core 2 of the 15 counter. When the bit is shifted from the first core to the second core in the counter, an output level is generated to condition GT 1 to pass an OD 4-13 pulse. This OD 4-13 pulse is used to set the search flip-flop and to step the G/A-TD burst time counter.

The output level generated by the first core of the 15 counter also causes the G/A-TD word contained in the first column of the selected array to be read out into OSR 1. In the interval between 15-counter-1 and 15-counter-2 times, the G/A-TD word now contained in OSR 1 is fast-shifted into OSR 2. At 15-counter-2 time, the second G/A-TD word is read out of the second column of the selected array into OSR 1. In the interval between 15-counter-2 and 15-counter-3 time, both G/A-TD words are shifted serially out of both OSR's at the same time to their respective phone lines. When the counter is shifted to 15-counter-3 and 15-counter-4, the remaining two G/A-TD

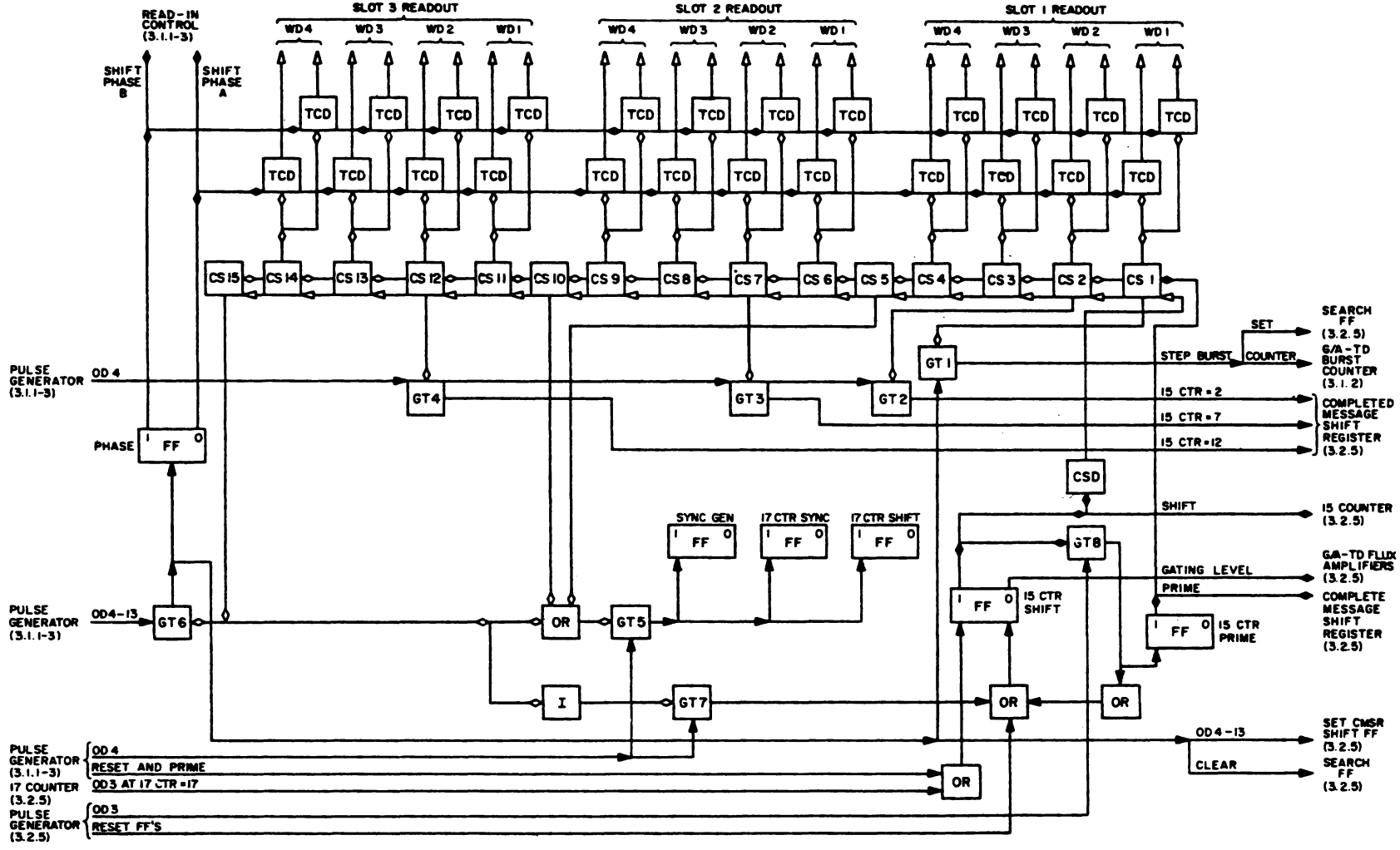


Figure 3-42. G/A-TD 15 Counter (3.2.5), Simplified Logic Diagram

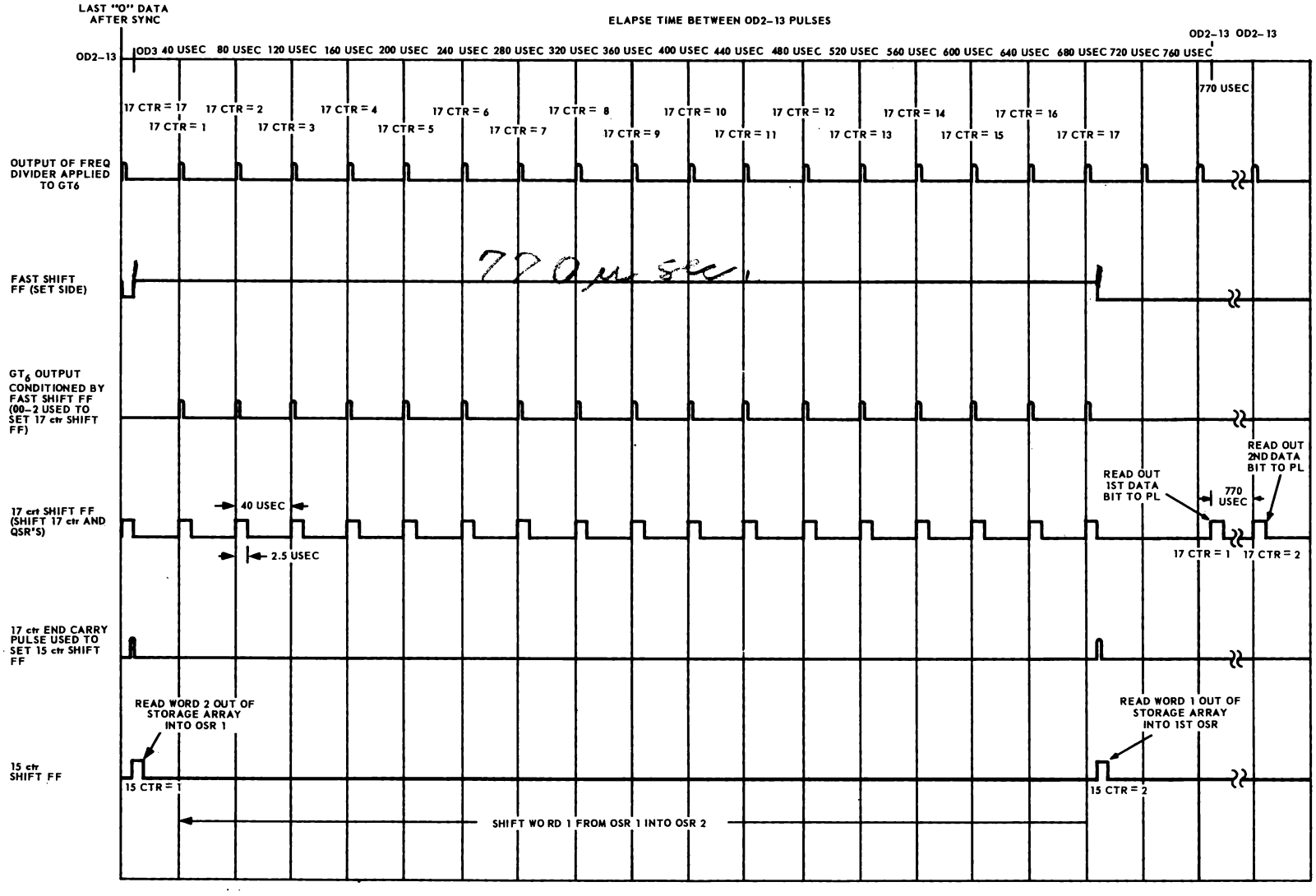


Figure 3-43. G/A-TD High-Speed Shift Timing Chart

words of slot 1 are read out of the selected array in the manner described for 15-counter-1 and 15-counter-2 times.

Readout of G/A-TD message slot 2 is performed in the same manner as that described for G/A-TD message slot 1. However, its readout time occurs from 15-counter-6 time through 15-counter-9 time.

Similarly G/A-TD message slot 3 is also read out in the manner described for G/A-TD message slots 1 and 2; however, its readout time is from 15-counter-11 time through 15-counter-14 time.

At 15-counter-2 time, an OD 4 pulse is passed through GT 2 to the G/A-TD CMSR circuitry. This OD 4 pulse at 15-counter-2 strobes the gate that is associated with the CMSR slot-1 flip-flop. If a complete message has been read into G/A-TD message slot 1, the gate will be conditioned to pass the OD 4 pulse at 15-counter-2 time to set the CMSR readout flip-flop. Setting this flip-flop permits the G/A-TD words of message slot 1 to be shifted out of OSR 1 and OSR 2 to the phone lines.

The operation described above is again repeated when the 15 counter is shifted to 15-counter-7 and 15-counter-12 time for the subsequent readout of G/A-TD message slots 2 and 3, respectively. The CMSR slot flip-flops (FF's 1, 2, and 3) are subsequently cleared whenever the 15 counter is stepped to 15-counter-12 time.

Whenever the 15 counter is shifted to 15-counter-5, -10, and -15, GT 5 passes an OD 4 pulse to set the sync generation flip-flop, the 17-counter shift flip-flop, and also the 17-counter sync flip-flop. Setting these flip-flops permits the generation of the G/A-TD sync pattern which must precede each G/A-TD message.

When the 15 counter has completed its operational cycles at 15-counter-15 time, GT 6 is conditioned to pass an OD 4-13 pulse. This pulse complements the phase flip-flops and clears the search flip-flops, thus ending the G/A-TD search period. In addition, this 15 counter-15 end-carry level is returned to the 15-counter shift circuitry, whereupon the 15 counter is reset in preparation for a new 15 counter cycle.

A timing chart is presented in Figure 3-43, to illustrate the over-all timing process of the G/A-TD storage section.

f. Associated Control Circuits

In addition to the G/A-TD counters that are used for timing and control purposes in the G/A-TD storage section, other control circuitry is required to control the various operations listed below:

(1) G/A-TD search and not-search (g)

(2) Array selection (h)

(3) 15-counter shift control (i)

(4) Automatic parity bit generation (j)

(5) 17-counter associated control circuits (k)

(6) Fast-shift control (l)

g. G/A-TD Search and Not-Search

During search time, the G/A-TD storage section accepts messages from the OB drum fields into its respective core storage arrays. The G/A-TD search and not-search circuit generates the required search and not-search levels needed to begin and end the G/A-TD read-in operation.

As shown in Figure 3-44, the required G/A-TD search level is generated when the search flip-flop is set, by an OD 4-13 pulse at 15-counter-1 time. This flip-flop is cleared by an OD 4-13 pulse at 15-counter-15 time. Therefore, search time for a G/A-TD read-in operation is approximately 86.2 ms. When the search flip-flop is cleared, it remains in this state for a period of 3.85 ms. The latter constitutes the not-search period; that is, when no messages will be accepted from the OB drum fields by the G/A-TD storage section.

h. Array Selection

The G/A-TD storage section utilizes two core storage arrays which are used to store incoming G/A-TD messages. Since two core storage arrays are used, read-in and readout of the G/A-TD messages can occur simultaneously. The circuit which is used to select and control the G/A-TD read-in and readout operations is the phase circuit.

As shown in Figure 3-45, selection of the particular G/A-TD core storage array to be read out is determined by the phase flip-flop. This flip-flop is complemented by an OD-4-13 pulse whenever the 15 counter is at 15-counter-15 time. Thus, the core storage array which was read into is now selected to be read out.

i. 15-Counter Shift Control

The 15-counter shift flip-flop (Figure 3-46) is used to control the shifting of the 15 counter with 2.5-usec shift pulses. Subsequent shifting of the 15 counter generates clear-column pulses to the core storage array columns to read out the G/A-TD words.

The 2.5-usec shift pulses are also used to gate the FA's associated with the core-storage-array data output lines. These FA's when gated transfer the G/A-TD data that is read out of the array into OSR 1. Other functions of the G/A-TD shift control circuit are (1) generating a reset level to the 15 counter, (2) checking the CMSR's for completed G/A-TD messages and (3) priming the G/A-TD CMSR's and the 15 counter.

As shown in Figure 3-46, the 15 counter shift flip-flop is set by an OD 3 pulse at 17-counter-17 time, and is cleared by the following OD 4 pulse for every

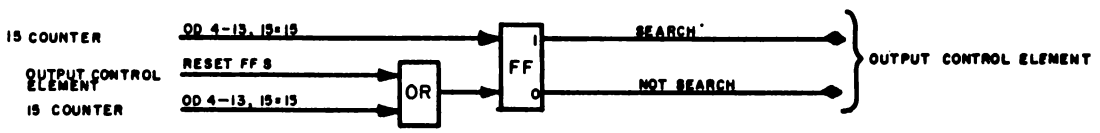


Figure 3-44. G/A-TD Search Flip-Flop

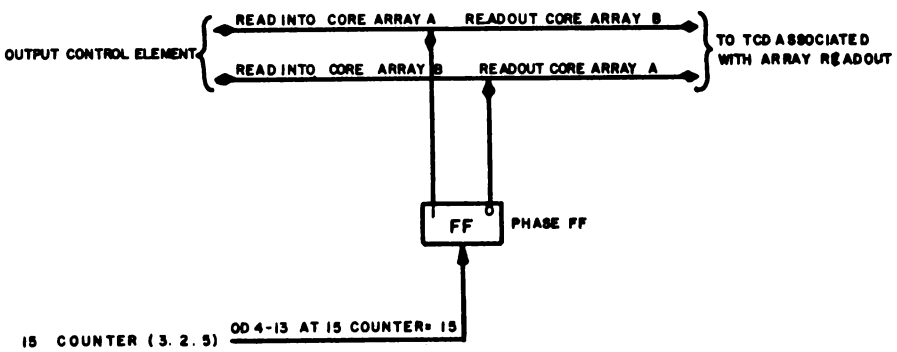


Figure 3-45. G/A-TD Array Selection (3.2.5), Simplified Logic Diagram

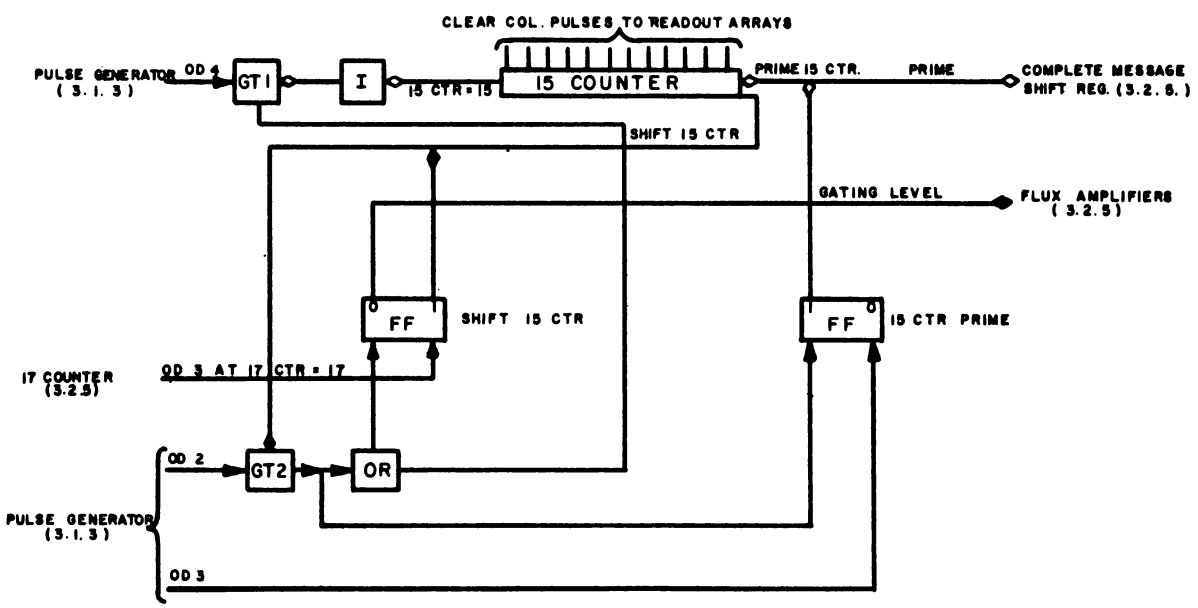


Figure 3-46. G/A-TD 15-Counter Control Circuits (3.2.5), Simplified Diagram

shift of the 15 counter except when the counter is at 15-counter-15 time. Hence, the 15 counter shift flip-flop generates shift pulses of 2.5-usec duration which are used to shift the 15 counter and to condition the FA's as described above.

When the 17 counter is at 17-counter-17 time an OD 3 pulse is passed to set the 15-counter shift flip-flop. This flip-flop, when set, will cause the 15 counter to be stepped by 2.5-usec shift pulses until the counter completes its operational cycle at 15-counter-15 time. At that time, a positive level is applied to the inverter. The output of this inverter deconditions GT 1, thus preventing the OD 4 pulses from clearing the 15-counter shift flip-flop.

The purpose of inhibiting the clearing of the 15-counter shift flip-flop at OD 4 time is to allow a 10-usec level to be generated so that the 15 counter may be reset. This reset level is obtained by conditioning GT 2 (the shift flip-flop is set) and strobing it with OD 3 pulses. The OD 3 pulse occurring after the inhibited OD 4 pulse (7.5 usec later) will be passed to clear the 15 counter shift flip-flop; at the same time, it will set the 15-counter prime flip-flop. The latter primes at 1 into the first core of each CMSR (there are three CMSR's) and also primes a 1 into the first core of the 15 counter in preparation for the start of a new 15-counter cycle. Refer to Figure 3-47 and Figure 3-48.

j. Automatic Parity Bit Generation

The auto parity generator (Figure 3-47) is used to automatically place parity bits on the G/A-TD data phone lines whenever a particular G/A-TD message slot has not been filled with the prescribed number of four words. In the absence of a complete G/A-TD message, therefore, the auto parity generator will generate four parity bits (one 1 bit per G/A-TD word) to maintain the odd parity bit status required of G/A-TD messages (Figure 3-48). This action also prevents the generation of the G/A-TD output parity alarm. However, it is to be noted that auto parity generation will occur only at those times when particular G/A-TD message slots do not contain the required number of words (four) for transmission on G/A-TD data phone lines. Detailed operation of the parity generator circuit follows.

During the first normal shift cycle of the 17 counter at 17-counter-15, an OD 3-13-and-sync pulse is generated to clear the auto parity generator flip-flop. This same pulse is also used to generate the sync bit of the sync pattern. The latter precedes all G/A-TD messages.

When a slot is not filled, an incompleted-message level (shown in Figure 3-47) is generated by the 0 side of the CMSR flip-flop. The generated incompleted-message level is used to condition GT 1. The sync generator flip-flop produces an OD 3-13-and-not-sync pulse at the completion of the second normal shift cycle of the 17 counter; that is, at 17-counter-17 time. Therefore, at the conclusion of this second normal shift cycle of the 17 counter, this pulse will be passed by conditioned GT 1 to strobe GT 2, and will be sent to the parity checking circuit and the data phone line conversion equipment associated with phone line 2. The auto parity bit generator flip-flop (cleared at 17-counter-15 time by an OD 3-13-and-sync pulse) conditions GT 2. Hence the OD 3-13-and-not-sync pulse which occurs at 17-counter-17 will thus be passed to the output converter and parity checking circuits associated with G/A-TD data phone

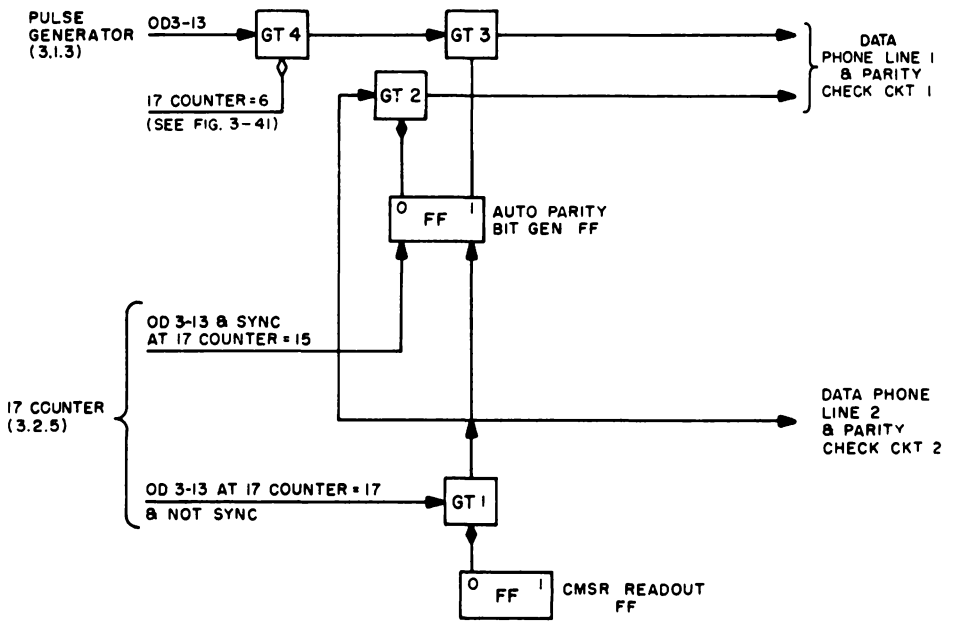


Figure 3-47. G/A-TD Auto Parity Bit Generator, Simplified Logic Diagram

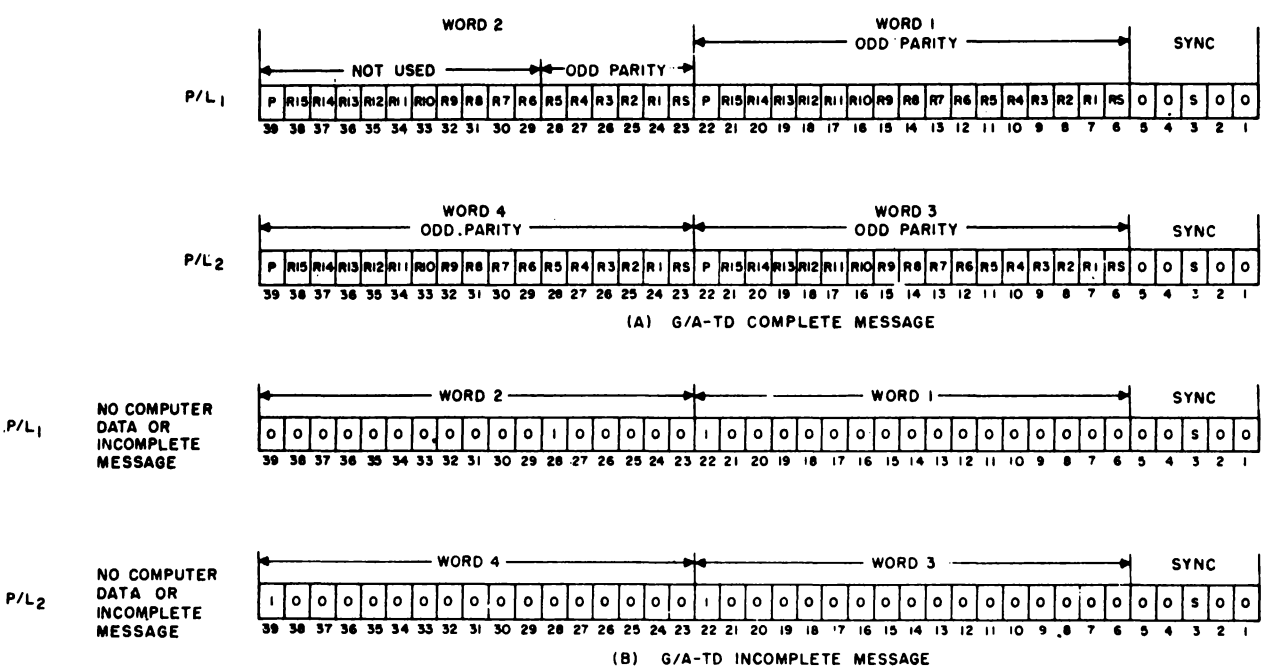


Figure 3-48. G/A-TD Word Message Layout

line 1. Thus, a parity bit is generated in lieu of the first G/A-TD word (word 1 or 3) that is absent from data phone lines 1 and 2. Referring to Figure 3-48B, it can be seen that the generated parity bits are inserted in bit position 22 for words 1 and 3.

The OD 3-13-and-not-sync pulse which occurs at 17-counter-17 time will also cause the auto parity bit generator flip-flop to be set. Setting this flip-flop conditions GT 3 so that, during the ensuing third normal shift cycle of the 17 counter, an OD 3-13 pulse, which is gated at 17-counter-6 time by GT 4, is passed to strobe GT 3. Conditioned GT 3 will therefore pass this OD 3-13 pulse which occurs at 17-counter-6 time to the output converter and parity checking circuits associated with G/A-TD in lieu of the second G/A-TD word (word 2) that is absent from data phone line 1. Referring to Figure 3-48B, the generated parity bit is inserted in bit position 28 of word 2.

At the conclusion of the third, normal, slow shift cycle of the 17 counter, another OD 3-13-and-not-sync pulse (at 17-counter-17) is passed through conditioned GT 1. From this gate, the pulse is then sent to the output converter and to the parity checking circuit associated with G/A-TD data phone line 2. Thus, a parity is generated in lieu of the second G/A-TD word (word 4) that is absent from data phone line 2. Referring to Figure 3-48B, the generated parity bit is inserted in bit position 39 of word 4.

During the fourth normal shift cycle of the 17 counter at 17-counter-15 time, the sync bit of the sync pattern is again generated. The generated sync pattern precedes the G/A-TD message contained in slot 2. At this time, the OD 3-13 and sync pulse gated by the sync generator flip-flop at 15-counter-5 time will clear the auto parity bit generator flip-flop. The auto parity bit generator circuit is therefore once again ready to detect the absence of any G/A-TD messages from any of the G/A-TD message slots. (Figure 3-49.)

k. Associated Control Circuits, 17 Counter

The control circuits associated with the 17 counter are the 17-counter sync flip-flop, the 17-counter prime flip-flop, and the fast-shift control circuits. As shown in Figure 3-49, the 17-counter-sync control circuit is used to set the 17-counter prime flip-flop, clear the fast-shift flip-flop, initiate the start-delay pulse to the delay counter, and, when used in conjunction with the 17-counter prime flip-flop, control the priming of both the delay counter and the 13th core of the 17 counter. The detailed operation of both the 17-counter sync flip-flop and 17-counter prime flip-flop follows.

When the 15 counter is shifted to the following 15-counter-5, -10, and -15 times, an OD 4 timing pulse is gated to set the 17-counter sync flip-flops via OR 1. Setting this flip-flop conditions GT 1, which is strobed by an OD 3 pulse. This OD 3 pulse is passed by conditioned GT 1 to set the 17-counter prime flip-flop and clear the fast-shift flip-flop; it is also sent to set the start delay flip-flop in the test equipment section and clear the 17-counter sync flip-flop via OR 2.

With the setting of the 17-counter prime flip-flop, a level is caused to be generated which is subsequently used to prime a 1 bit in the 13th core of the 17 counter, thus providing the start of the sync pattern generation cycle as well as priming a 1 bit in the first core of the delay counter in the test equipment section. The 17-counter

prime flip-flop is then cleared at the following OD 2 time, thus ending the functions of the control circuits associated with the 17 counter.

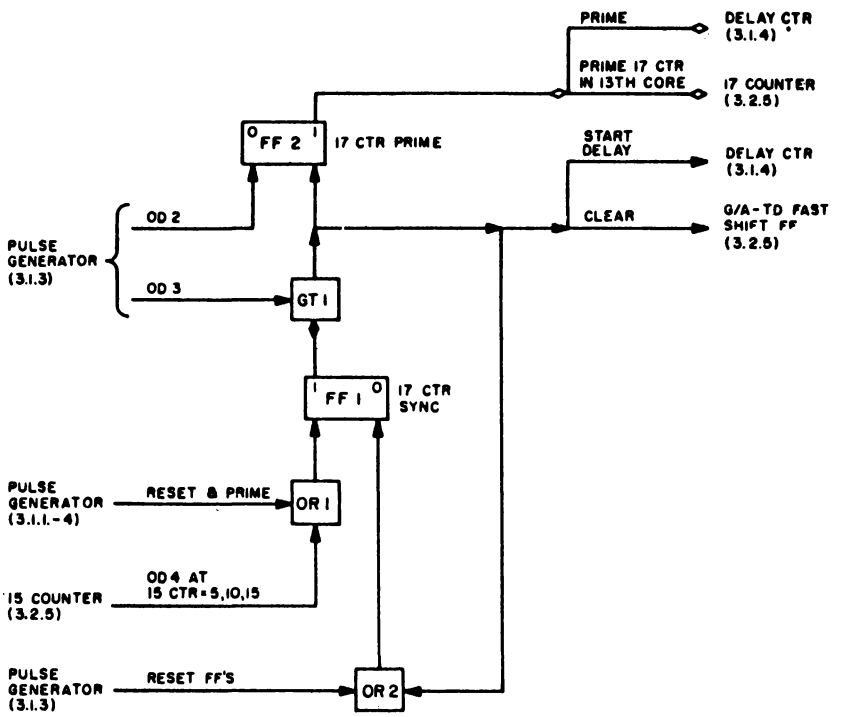


Figure 3-49. Associated Control Circuits, 17 Counter Simplified Logic Diagram

1. Fast-Shift Control Circuit

The fast-shift control circuit (Figure 3-41) is also used in association with the 17 counter; it is mentioned only briefly because its operation is described in detail in 4.d.

5. Readout

a. General

Readout of all G/A-TD messages is accomplished as follows:

(1) Read out G/A word 1 from selected array to OSR 1.

(2) Fast shift G/A-TD word 1 from OSR 1 to OSR 2.

(3) Read out G/A-TD word 2 from selected array to OSR 1.

(4) CMSR filled; read out complete G/A-TD message to G/A-TD core storage arrays.

b. Core Array Readout

Each G/A-TD message is read out of the G/A-TD core storage arrays one 17-bit column at a time, through FA's, into OSR 1. The message is subsequently fast-shifted into OSR 2. When both OSR's contain the two 17-bit columns representing two G/A-TD words, these words will be shifted serially out of their respective OSR's to their respective data conversion equipment under the control of the G/A-TD completed message shift register.

As mentioned previously, each G/A-TD message slot is read out of the core array by columns during the G/A-TD burst period. Each core array is comprised of 12 columns which are pulsed serially by clear-column pulses that are applied by the TCD's associated with the 15 counter. Each time a column is pulsed, the 17 bits (representing a complete G/A-TD word) stored in its cores are shifted in parallel form to the FA's.

Each of the 17 bit output pulses from the G/A-TD core storage array is applied to an FA. A 1 bit is represented by a pulse, and a 0 bit is represented by the absence of a pulse. Each FA, shown in Figure 3-50, is gated by a gating level emanating from the 0 side of the 15-counter shift flip-flop. These levels are 2.5-usec negative pulses (OD 3 at 17-counter-17 to OD 4) used to prevent noise and spurious signals from passing

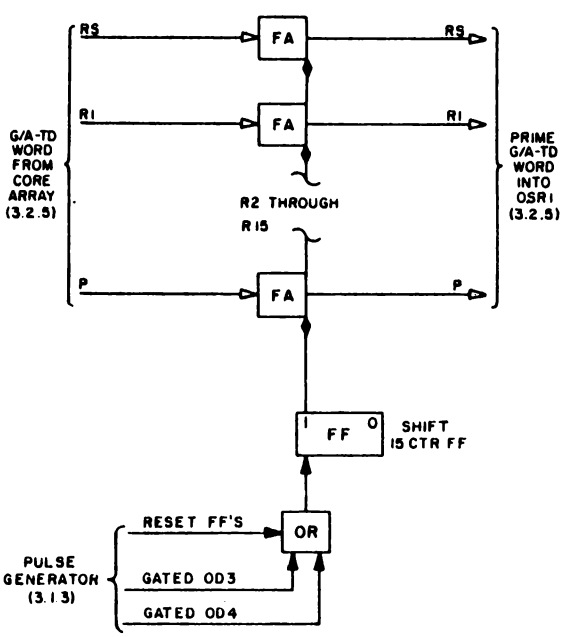


Figure 3-50. G/A-TD Flux Amplifiers (3.2.5), Amplified Logic Diagram

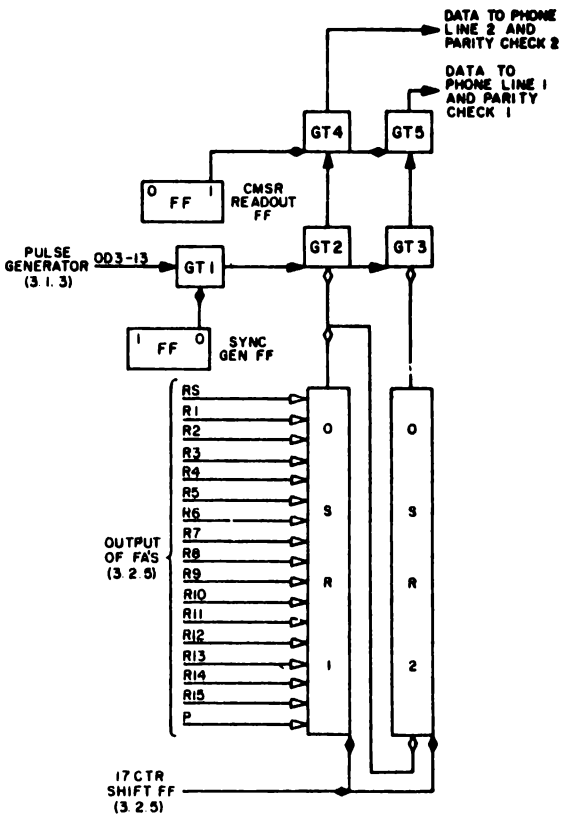


Figure 3-51. G/A-TD Output Shift Register, Simplified Logic Diagram

through the FA's. These pulses are produced in the G/A-TD control coincident with each shift of the 15 counter that occurs during readout time. (Refer to 4.f.) Since these 15-counter shifts generate clear-column pulses which read columns out of the core array, the core storage array outputs are applied to the FA's during the 2.5-usec period that the FA's are gated and made operative.

The FA's, after amplifying the array output pulses, send the pulses to both OSR's as FA outputs. The outputs from the FA's are sent over 17 lines labeled RS to R15, including P, respectively.

c. Output Shift Registers (OSR's)

The G/A-TD storage section utilizes two OSR's which store two G/A-TD words at one time (Figure 3-51). Each OSR is comprised of a 17-core shift register which is shifted at two specific rates. The first is called the normal shift rate which occurs at 1,300 pps and is used to shift the G/A-TD words out of the two OSR's onto the G/A-TD data phone lines and their respective parity checking circuits. The second

shift mode is called the fast shift and is used specifically to fast-shift the first and third words of a particular G/A-TD message from OSR 1 to OSR 2.

Figure 3-51 is a representative diagram of the G/A-TD OSR's and their associated circuitry. Both OSR's are shifted under the control of the 17-counter shift flip-flop. Readout of the G/A-TD words from the two OSR's to the data phone lines depends upon the CMSR flip-flop being set. The set condition of this flip-flop indicates that a complete message is contained in a particular G/A-TD slot, that this message is ready to be read out of the OSR's and that the sync generator flip-flop is clear. The latter flip-flop when cleared, indicates that the sync pattern required to precede all G/A-TD messages has been generated and that readout of the G/A-TD message can now be executed.

During normal operation, a G/A-TD word is read into OSR 1 from a selected core storage array under the control of the 15 counter. The G/A-TD word now stored in OSR 1 is fast-shifted into OSR 2 under the control of the 17-counter shift flip-flop.

Subsequently, a second G/A-TD word is read into OSR 1 from the selected core storage array, with the result that two G/A-TD words are then stored in the OSR's. When a shift level is generated by the 17-counter shift flip-flop, readout of the two G/A-TD words from the OSR's to the data phone lines will be effected in serial form at the normal shift rate of 1,300 pps.

For every 1 data bit that is read out of each OSR, the respective GT 2 and 3 associated with each OSR will be conditioned. Conditioned GT's 2 and 3 will then pass the gated OD 3-13 pulses passed by previously conditioned GT 1 (GT 1 is conditioned by the 0 side of the sync flip-flop) to strobe CMSR GT's 4 and 5. If the CMSR readout flip-flop has been set, GT's 4 and 5 will be conditioned to pass the 1 bits of each G/A-TD word on to data phone lines 1 and 2 and their respective parity checking circuits.

The above readout cycle is again repeated for readout of the third and fourth G/A-TD words. At the completion of the latter cycle, a complete G/A-TD message containing four words will have been read out to the data phone lines.

It is to be observed that, when the first and second G/A-TD words are read out of OSR 1 and OSR 2 to the data phone lines, the second G/A-TD word will, at the same time, be shifted into OSR 2. However, this second G/A-TD word is never read out of OSR 2 to the data phone lines because at the time when the third G/A-TD word is fast-shifted into OSR 2, the second G/A-TD word will also be fast-shifted out of OSR 2 to condition GT 3. Because no OD 3-13 pulses are present to strobe GT 3 during the fast-shift cycle, the second G/A-TD word data bits will not be passed by GT 3 and will therefore be destroyed.

The above condition will also prevail for the third and fourth G/A-TD words. In this case, however, the fourth G/A-TD word will not be fast-shifted as in the case of the second G/A-TD word, but instead it will be destroyed at the completion of the G/A-TD message read out by a reset level of 7.5 usec duration which is generated by the 17-counter shift flip-flop. The reset level generated by the 17-counter shift flip-flop clears both OSR 1 and OSR 2 as well as the 17 counter.

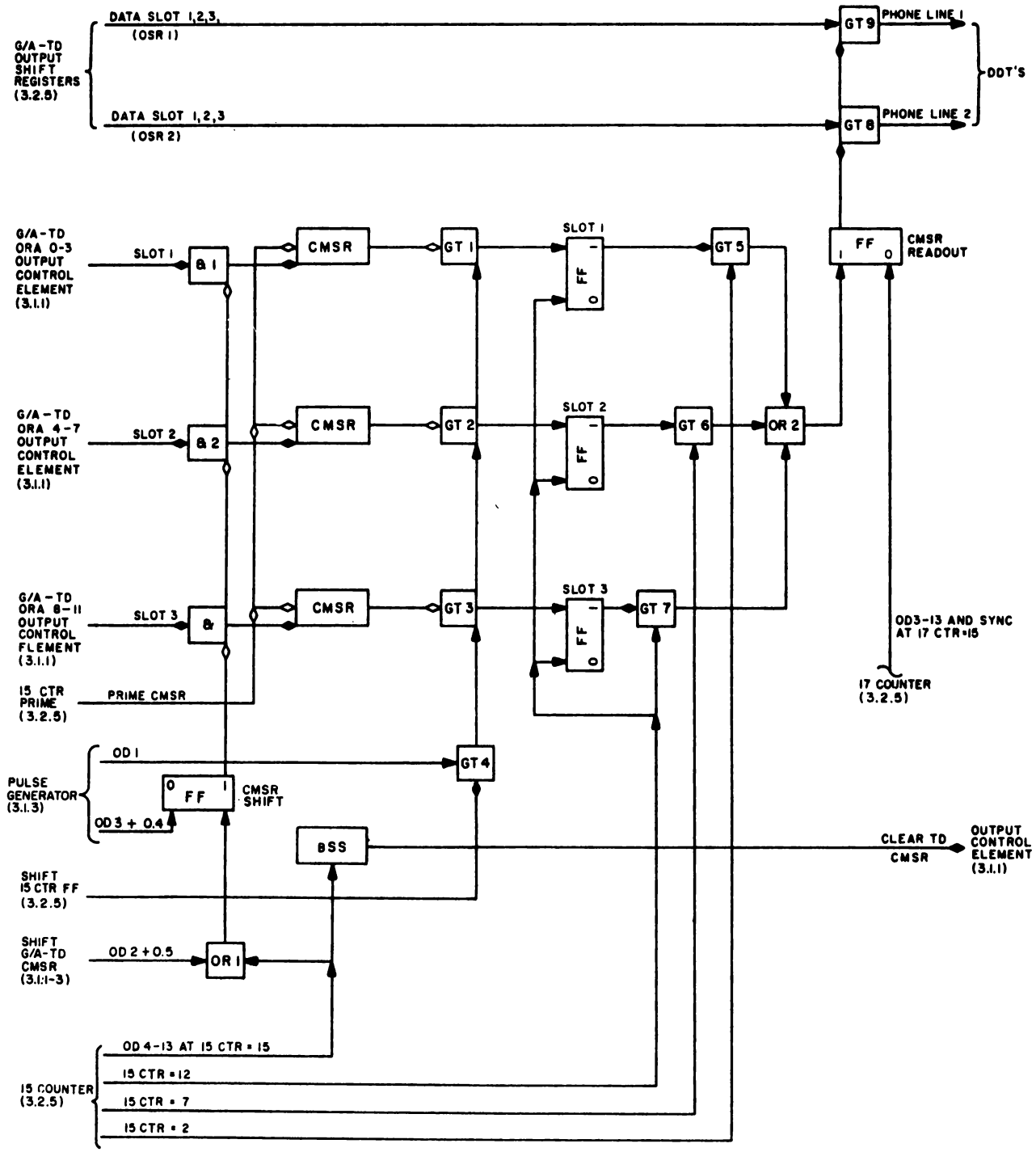


Figure 3-52. G/A-TD Completed Message Shift Register (3.2.5), Simplified Logic Diagram

d. Completed Message Shift Register

The G/A-TD completed message shift register (CMSR) (Figure 3-52) counts the number of G/A-TD output words written into each slot in the core storage array. If four G/A-TD words are written into a slot during a burst period, the completed message in that slot will be passed through the OSR's to the conversion equipment. If the message slots do not contain the required complement of four words per slot, no messages are read out and the auto parity generator will be caused to generate odd parity bits on the data phone lines.

As shown in Figure 3-52, three G/A-TD CMSR word counters are used, each capable of counting and recording the required four words needed to complete a G/A-TD message slot. Preparatory to the read-in and counting of the G/A-TD words during a burst period, the three G/A-TD CMSR slots are primed under the control of the 15-counter prime flip-flop. The latter flip-flop primes a 1 into the first core of each CMSR, and also primes a 1 into the first core of the 15 counter.

Assuming that the ORA's of the G/A-TD words to be read in are addresses 0 through 3 (message slot 1), a conditioning, slot-1, level will be applied to one of two input lines of the 2-way AND circuit (AND 1 of Figure 3-52). Coincident with this level, a CMSR shift pulse (parity O K O D 2 + 0.5) is supplied through OR 1 to set the CMSR shift flip-flop. Setting this flip-flop causes a +10v level (2.5 usec duration) to be applied to one input line of all three 2-way AND circuits associated with the G/A-TD CMSR's. The AND 1 circuit will be conditioned for a period of 2.5 usec to shift the 1 bit that has been primed into its associated CMSR. This 1 bit is shifted one core at a time for each G/A-TD word that is read into message slot 1 of the selected core storage array. Thus, the CMSR counts the G/A-TD words contained in message slot 1 as these words are being read into the selected core storage array.

When a complete message has been read into the selected core storage array, the 1 bit will be located in the last core of the CMSR for slot 1. This operation, in effect, completes the read-in operation of the G/A-TD message in slot 1 during a G/A-TD burst period. Similarly, the operation described above will also take place for message slots 2 and 3 when these are being read into the selected core storage array.

The read-in operation of the G/A-TD words into a selected core storage array is completed when the 15 counter is at 15-counter-15 time. At this time, the following operational steps take place:

(1) An OD 4-13 pulse is gated to complement the phase flip-flop (Figure 3-45) to select for readout the core storage array that has just been read into.

(2) This OD 4-13 pulse clears the search flip-flop (Figure 3-44) ending search time.

(3) This OD 4-13 pulse sets the CMSR shift flip-flop. The latter, when set, generates a level (+10v) that is applied to one input line of all three 2-way AND circuits associated with the CMSR's.

(4) The OD 4-13 pulse also causes a single-shot multivibrator to fire; thus, a 25-usec level (+10v) is applied to the remaining input lines of the three 2-way AND circuits and conditions these circuits.

The output of all three conditioned AND circuits is a reset level (7.9-usec duration) that is applied to reset each of the respective CMSR's. Resetting the CMSR's causes the 1 bits that are located in the last cores of each to be shifted out to condition the respective gates of each CMSR. All three gates (GT's 1, 2, and 3) are strobed by an OD 1 pulse that is passed through GT 4 only when the 15-counter shift flip-flop is set (for 10 usec) at 15-counter-15 time.

Since GT's 1, 2, and 3 are conditioned, the OD 1 pulse which strobes each individual gate is passed to set the CMSR slot flip-flops. These flip-flops, when set, generate a conditioning level to their associated gates (GT's 5, 6, and 7). Conditioning the individual gates indicates that the message slot associated with each has been filled.

During the following 15-counter cycle, at 15-counter-2 time, an OD 4 pulse is gated to strobe GT 5. If a complete G/A-TD message was read into slot 1, the OD 4 pulse is passed through the OR 2 circuit to set the CMSR readout flip-flop. This flip-flop is cleared during the generation of the G/A-TD sync pattern (00S00) by an OD 3-13-and-sync pulse which occurs at 17-counter-15. Setting the CMSR readout flip-flop causes a level to be generated to condition GT's 8 and 9, thus allowing for the subsequent readout of the complete G/A-TD message that was stored in slot 1 of the selected core storage array.

The readout operation for G/A-TD message slots 2 and 3 is the same as the operation described for message slot 1, with the exception that, for the readout of G/A-TD message slot 2, the gated OD 4 pulse is passed by GT 6 to set the CMSR readout flip-flop at 15-counter-7 time, and for the readout of G/A-TD message slot 3, the gated OD 4 pulse is passed by GT 7 to set the CMSR readout flip-flop at 15-counter-12 time, this same OD 4 pulse also clears CMSR FF's 1, 2, and 3.

Should a particular G/A-TD message slot not contain the required four words necessary for a complete message, the particular gate associated with the incompleted message slot will remain deconditioned; hence, its respective CMSR slot flip-flop will remain cleared. Therefore, at the 15-counter-equals time for that particular slot, no pulse will be gated to set the CMSR readout flip-flop, and no message readout can occur for that slot.

6. Parity Check

As the G/A-TD words are read out of the storage section to the data phone lines, a parity check of each word is performed. The parity of all G/A-TD words must be odd. However, if any G/A-TD words contain an even number of 1 bits, a G/A-TD output alarm is generated and the word containing the even number of 1 bits is nevertheless transmitted to the data phone lines.

Each G/A-TD word is simultaneously read out to the data phone line and the respective parity checking circuit. In the parity checking circuit (Figure 3-53), the G/A-TD word data intended for data phone line 1 is supplied through OR 2 to complement the

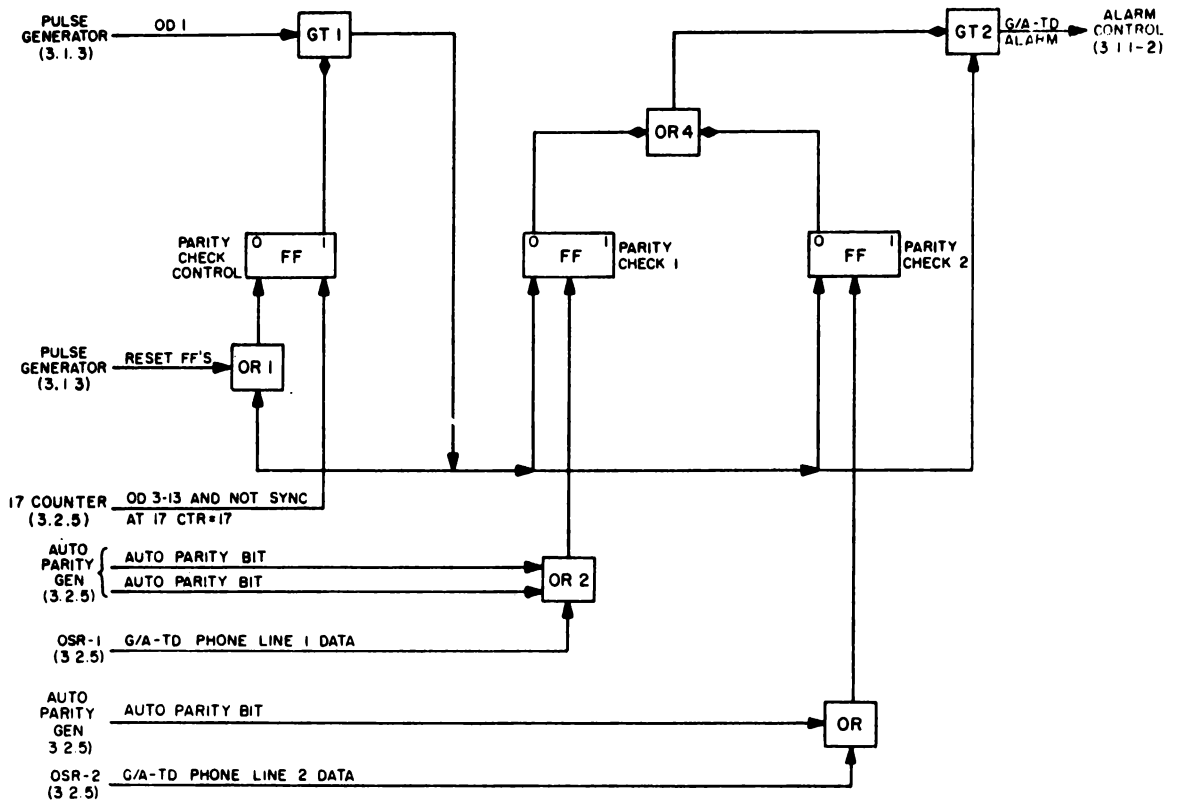


Figure 3-53. G/A-TD Parity Check Circuit (3.2.5), Simplified Logic Diagram

parity check 1 flip-flop. The G/A-TD word data intended for data phone line 2 is supplied through OR 3 to complement the parity check 2 flip-flop. Should the transmitted G/A-TD words on data phone lines 1 and 2 be of the correct parity (odd) no alarm will be generated. Conversely, if either of the two G/A-TD words has an incorrect parity (even) when transmitted over data phone lines 1 and 2, the parity checking flip-flop associated with the incorrect word will be clear at the end of the parity check operation.

If either of the parity check flip-flops is clear, a level is generated through OR 4 to condition GT 2. Conditioned GT 2 is strobed by and passes a gated OD 1 pulse is passed through GT 1 when the parity check control flip-flop is set. This flip-flop is set by an OD 3-13-not-sync pulse when the 17 counter is at 17-counter-17 time. This pulse appears in coincidence with the readout of the last data bit of every G/A-TD word that is transmitted over data phone lines 1 and 2. The parity check control flip-flop is cleared by the gated OD 1 pulse, 5 usec after it was set. Clearing this flip-flop ends the parity checking circuitry to check the parity of the succeeding G/A-TD words to be transmitted.

Figure 3-47. In the absence of a complete G/A-TD message, the auto parity generator (Figure 3-47) generates an odd parity bit in lieu of an absent G/A-TD word.

The data-1 bits generated by the parity generator are fed to OR 2 and OR 3 to complement the respective parity check flip-flops associated with each data phone line, thus ensuring that no G/A-TD alarm is generated.

7. Burst Sequence and Timing

a. General

The G/A-TD burst counter and compare circuit and the burst number of the assigned G/A-TD message are the basic means employed to control the order and time of transmission of messages. The assigned burst numbers of each drum word are compared to the current contents of the burst counters. If the assigned burst number is equal to the contents of the G/A-TD burst counter, and if all the other conditions are favorable, the word is accepted by the Output System.

To be sure that the message is transmitted in proper sequence and at the proper time, the Central Computer System assigns a burst number to each G/A-TD message to which the reading of the G/A-TD burst counter will be equal at the predicted transmission time. Each word of a burst is assigned the same burst number by the Central Computer System. To make it possible for the Central Computer System to determine this burst number, it is given access to the current readings of the G/A-TD burst counter through the output computer section of the output control element.

b. Burst Counter

The G/A-TD burst counter (Figure 3-54) is a standard 8-bit flip-flop counter having a scale of 256. This counter is stepped by each 15-counter-1 pulse which corresponds to the start of search time for each G/A-TD burst period. The 15 counter requires 90 ms to complete one cycle of operation.

The 8-bit burst count produced is fed to the computer section of the output control element and to the G/A-TD compare circuitry. The output levels from the 1 side of the flip-flops in the burst time counter are sent to the computer section, whereas both the 1 and 0 sides of these same flip-flops are sent to the computer circuit. A reset flip-flop signal from the output control element is supplied to reset the burst counter after shutdown or test operations.

c. Burst Number Comparison

The G/A-TD compare circuit (Figure 3-55) is used to determine which words in a given burst period are to be accepted from the OB fields. The burst number of each G/A-TD output word is fed into the G/A-TD compare circuit where it is then examined to ascertain whether it is equal to the contents of the G/A-TD burst time counter. If the G/A-TD compare circuit finds that the counts are equal, it generates a G/A-TD-compare signal. Conversely, if the burst counts are found to be unequal, a no-compare signal is generated.

The G/A-TD compare circuit comprises 16 2-way AND circuits, five 4-way OR circuits, and one inverter. Each AND circuit is fed a bit from the burst number supplied by the Central Computer and a bit from the G/A-TD burst counter. Although

these two bits are numerically equal, they represent opposite states; that is, while one bit represents a 1, the other represents its complement, which is 0. Under these conditions, an AND circuit produces a signal only when corresponding bits of the assigned burst number and the current count of the burst counter are unequal. When they are equal, all 16 2-way AND circuits produce a -30v output level. The AND circuits are connected to four OR circuits, which in turn are connected to a single OR circuit. Therefore, the -30v level emanating from the AND circuits is passed by the OR circuits and applied to the inverter. The output of the inverter is a +10v level which is then sent to the output control element as a G/A-TD no-compare level.

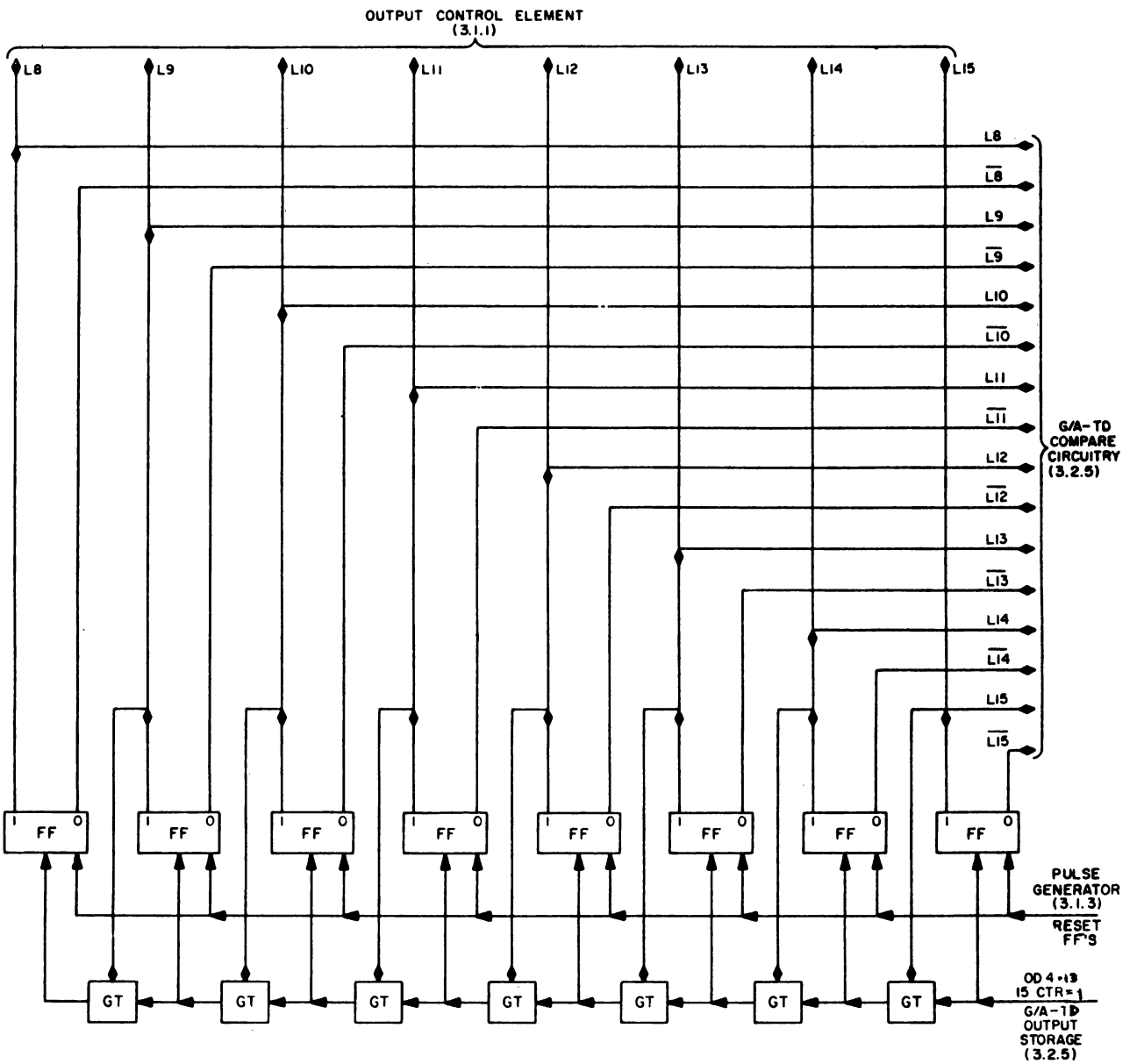


Figure 3-54. G/A-TD Burst Counter (3.1.2), Simplified Logic Diagram

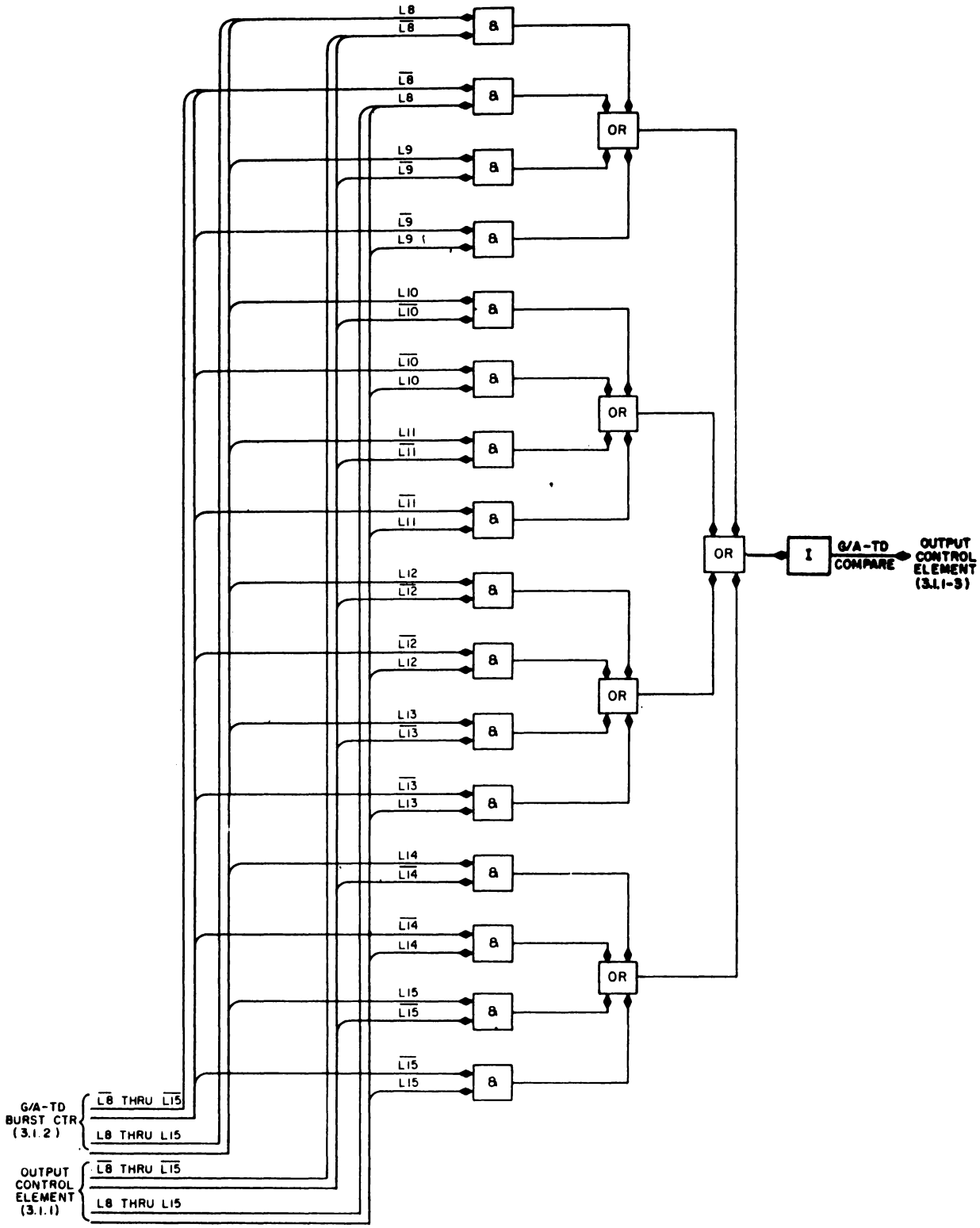


Figure 3-55. G/A-TD Compare (3.1.2), Simplified Logic Diagram

Should the assigned burst number and the burst time count be unequal, one or more of the AND circuits will produce a +10v level which is passed by the OR circuits (Figure 3-55) and applied to the inverter. The output of the inverter is a -30v level which is then sent to the output control element to indicate a no-compare situation.

8. Conversion

a. General

Information leaving the G/A-TD OSR's is sent to the conversion circuits prior to being fed through the switching circuits to the telephone transmission equipment. The conversion circuits convert the G/A-TD and sync information, which consists of standard 0.1-usec pulses, to a series of synchronized gates, 1,300-cps sine waves. The information is modified in this manner to make it compatible with telephone company equipment requirements.

b. Conversion Equipment

All of the conversion circuits are contained in the G/A-TD conversion equipment. This equipment is comprised of two identical channels, each capable of transmitting one G/A-TD word (half a message) at a time. Each channel contains a data conversion channel, an identical sync conversion channel, and a timing channel. The data and sync conversion channels perform the required conversion on their respective information inputs. The timing channel serves to match the timing signal, a 1,300-cps sine wave, to the telephone equipment, but does not modify its waveshape. The two channels are identical in operation. For this reason, the detailed operation of only one channel is presented in the following paragraphs.

c. Data Conversion Channel

Ground-to-air time division data is either a standard pulse occurring at OD 3-13 time to represent a 1 bit or the absence of this pulse at this time to represent a 0 bit. This data is applied to the G/A-TD output data channel 1 flip-flop. This flip-flop is set by G/A-TD data pulses and cleared by the following OD 2-13 timing pulses (Figure 3-56).

The G/A-TD output data channel 1 flip-flop supplies an input level to the 2-way AND circuit component of a logical gating (LGT) circuit. The LGT is comprised of this AND circuit plus a cathode follower and an OR circuit. The other input to the 2-way AND circuit is the 1,300 cps timing signal. The output of the AND circuit is either the timing signal or a -30v level, depending on whether the flip-flop is set or clear, respectively.

The flip-flop also supplies an input level to the OR driver cathode follower component of the LGT circuit. This cathode follower generates a clamped ground or a -30v output level, depending on whether the flip-flop is clear or set, respectively.

The AND circuit and cathode follower outputs constitute the inputs to the OR circuit component of the LGT circuit. The output of this OR circuit is either the 1,300 cps timing signal or a ground level, depending on whether the flip-flop is set or clear,

respectively. This output is sent to the telephone equipment via the MA circuit. When the flip-flop is set by receipt of a 1 bit (i.e., a standard pulse occurring at OD 3-13 time), the data conversion channel sends a 1,300 cps sine wave to the telephone equipment. This sine wave continues until the flip-flop is cleared by the following OD 2-13 pulse. Since the OD 3-13 pulses recur at a 1,300 cps rate and the OD 2-13 pulse precedes the next OD 3-13 pulse by 2.5 usec, the interval between an OD 3-13 data pulse and the following OD 2-13 clear pulse will be 2.5 usec less than the period of the 1,300 cps timing signal. Therefore, for each 1 bit received by the flip-flop, slightly less than one cycle of the 1,300 cps timing signal will be sent to the telephone equipment. When the flip-flop remains clear due to the absence of a 1 bit (i.e., the absence of a standard pulse), a ground level will be sent to the telephone equipment.

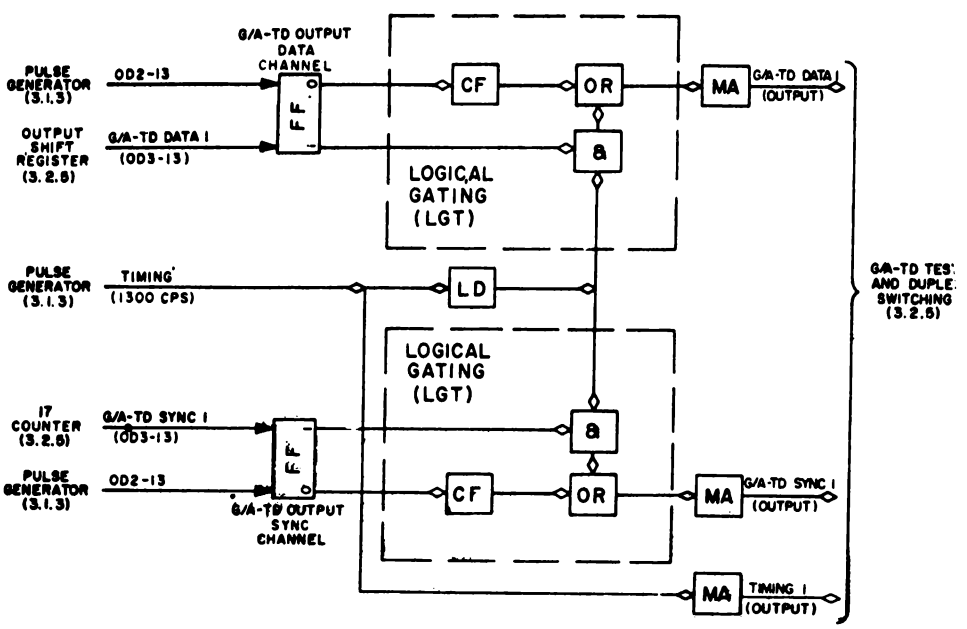


Figure 3-56. G/A-TD Conversion, Message 1 (3.2.5), Simplified Logic Diagram

d. Sync Conversion Channel

The sync conversion channel shown in Figure 3-56 operates in a manner identical with the data conversion channel just described. For each sync pulse received, the sync conversion channel transmits slightly less than one cycle of the 1,300 cps timing signal to the telephone equipment. The sync pulse is applied to the conversion equipment at such a time that exactly two 0 bits occur on the data lines between the end of the output sync signal and the time that the first data bit is transmitted over the data lines. (See Figure 3-57.)

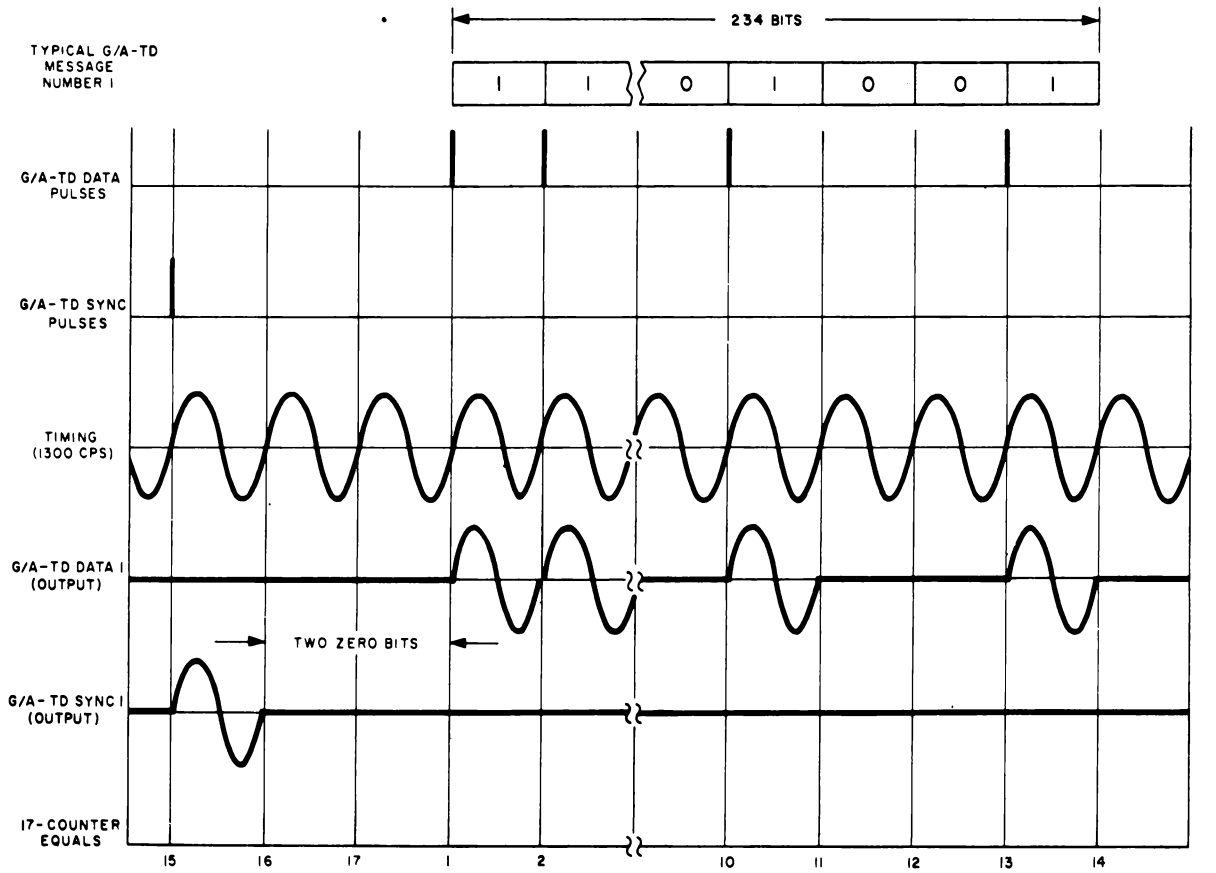


Figure 3-57. G/A-TD Conversion, Input and Output Signals

This timing, which is necessary for decoding in the airborne receiver, is obtained by having an OD 3-13 sync pulse occur at 17-counter-15 time just prior to the readout portion each burst period. The sync pulse, therefore, precedes the data pulses, which are read out starting with the second 17-counter-equals-1 pulse, by two 17-counter shifts. In this manner, two 0 bits (the absence of two data pulses on the data lines at OD 3-13 time) occur between the receipt of the sync pulse and the start of the data pulses (00S00).

The data, sync, and timing inputs and outputs of one channel of the G/A-TD conversion equipment for a typical G/A-TD message are shown in Figure 3-57. The outputs of this channel, together with the outputs of the second identical channel, are fed to the switching circuits and from there are sent out to the telephone equipment.

9. Switching

The G/A-TD test and duplex switching circuits control the output of the Output System of each computer. The switching circuits contain relays which provide for the

switching of each G/A-TD message. However, the relay circuits for each message are identical. For this reason, Figure 3-58 shows a simplified diagram of the G/A-TD test and duplex switching circuits for only one G/A message.

The relays provided by the G/A-TD test and duplex switching circuits are controlled so that only the Output System of the active computer is presented to the telephone line terminal equipment. Relays are also provided to enable the Output System on standby status to be switched to the LRI test busses through pattern generators. These relays are operated during test operations only.

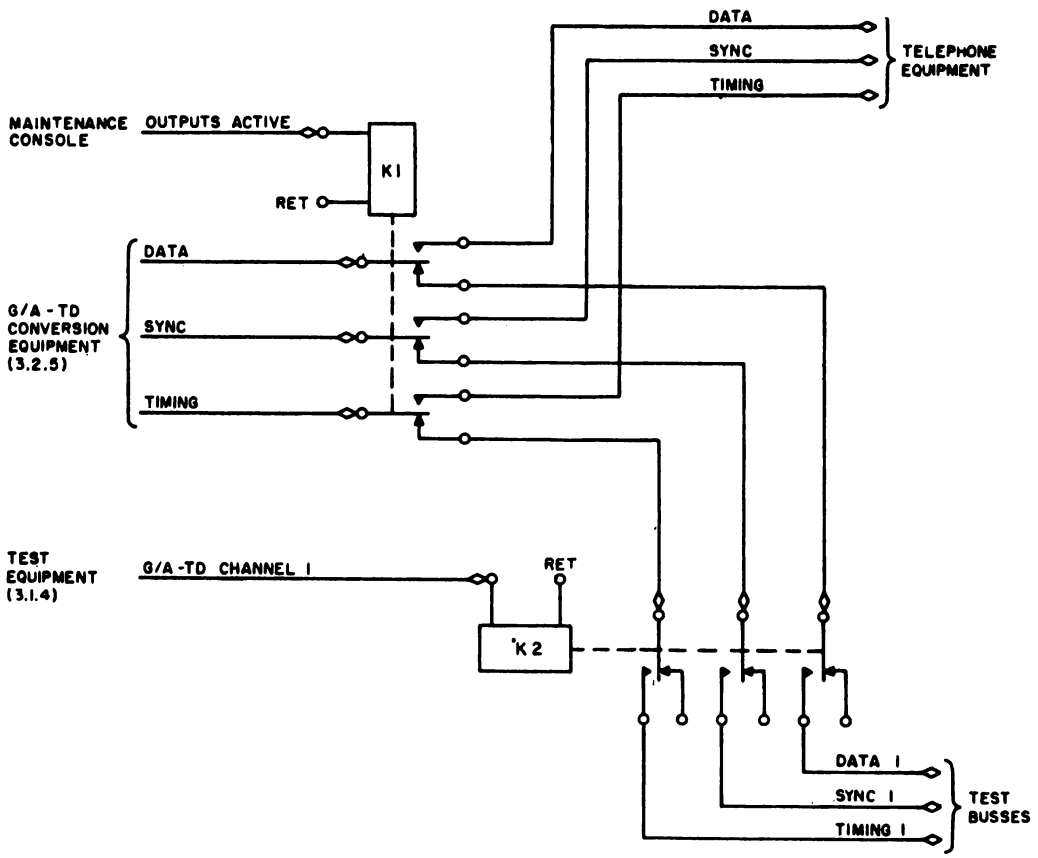


Figure 3-58. G/A-TD Test and Duplex Switching, Message 1 (3.2.5), Simplified Logic Diagram

SUMMARY QUESTIONS

1. G/A-TD output word has_____ parity.

2. The G/A-TD burst period is _____ millisecs.

3. For G/A-TD storage, _____arrays are used. Each array utilizes _____ registers. The registers are divided into_____slots with _____registers per slot.

4. G/A-TD read-in starts with 15-counter-_____ and is completed by 15-counter-_____.

5. In reading out G/A-TD, information is read out word by word.(T/F)

6. When no messages are being processed by G/A-TD, is an odd parity bit generated and sent over the phone lines?

7. In shifting the OSR's to send data onto the phone lines, G/A-TD words 2 and 4 will be shifted into OSR Register No. 2. (T/F)

8. G/A-TD messages sent over the phone lines are checked for parity. If even parity is detected, an alarm is generated and the message is destroyed. (T/F)

9. G/A-TD shares the 8 bit BTC FF's with G/A-FD (in the OB Reg). T/F)

10. The G/A-TD phone line message is preceded by sync followed by two zero bits. (T/F)

11. G/A-TD messages may be sent to GFI test busses provided the output system is in standby status.

12. How long is the Sync Gen FF set in usecs?

13. What is the time between 15=8 and 15=9?

14. At what time do we check parity in respect to the 15 counter?

15. How long is the clear pulse of the 17 counter?

16. 33 DJ J1 open (8A) 3.2.5

    a. CMSR slot 1 FF can never be set (10E).

    b. No slots can send information out of the phone line.

    c. The fast shift FF cannot be cleared.

    d. The CMSR readout FF in 9E can never be set.

    e. None of the above.

G/A-TD Storage Section, Single Channel Operation

1. The single channel mode of operation in the output's G/A-TD section, is a modification of the dual channel operation and incorporates much of the same circuitry. The major differences in the single channel operation are in the timing of the control functions and the manner in which the message is sent to the phone lines.

In the single channel operation, all data is sent out to phone line No. 1, via data conversion channel No. 2. As the entire message is sent out over one phone line, the time required per burst time count is necessarily increased by 100 percent. This is to allow the serial transfer of all words of each message out to a single phone line - phone line channel No. 1. The slowed-down operation is accomplished by changing the 15 counter to an 18/15 counter and disabling the fast-shift circuitry associated with the 17 counter.

2. System Operation

The G/A-TD storage section is logically divided into storage readout, control, message check, conversion, and switching. The sections perform functions similar to the corresponding circuits of the G/A-TD dual channel operation. However, since the G/A-TD single channel timing and message format differ somewhat from the G/A-TD dual channel operation, a discussion of the single channel operation follows.

a. Counter Operation

The control circuits consist of the 18/15 counter and 17 counter. The two counters control the operation and timing for the G/A-TD storage section. The 17 counter is stepped at a 1,300 cps (770 usec) rate. The 17 counter controls the stepping of the 18/15 counter.

During one burst period, the 18/15 counter is shifted through a complete cycle of operation. A G/A-TD operation cycle consisting of read-in and readout of the two core storage arrays is described in subsequent paragraphs. The G/A-TD read-in interval and readout interval for a single core array takes place during successive burst periods. Thus, two G/A-TD burst periods are required for one G/A-TD core storage array to complete a cycle of operation, consisting of read-in and readout. In actual operation, the read-in and readout functions occur simultaneously; as one core array is being written into, the other array is being simultaneously readout.

b. Read-In

The read-in operation for G/A-TD single channel is exactly the same as the read-in operation described for G/A-TD dual channel, except that the search period for G/A-TD single channel is somewhat longer than the search period for the dual channel operation.

In general, all counters are reset and primed in order to control the read-in of the G/A-TD words in the output section. The G/A-TD burst period begins with the first shift of the 18 counter. Search time for the storage section also begins at this time.

The read-in of the G/A-TD words is completed before 18/15 counter-18 time. At 18/15 counter-18 time the G/A-TD control generates a not-search level and a shift-phase level. The not-search level prevents the output control element from writing any more words in to the core registers. The shift-phase level switches core arrays so that the array just read into will be read out during the next burst period.

c. Readout

Readout of the core storage array that was written into during the previous burst period starts at 18/15 counter-1 time. In the G/A-TD single channel mode of operation, only one OSR (No. 1) is used. At 18/15 counter-1 time, a clear column pulse is generated to read out the first column of the selected array. The column of bits will make up one word which is readout and sensed by the FA's where they are amplified to prime the cores of the OSR. In the interval between 18/15 counter-1 time and 18/15 counter-2 time, this word is shifted out in serial fashion only if there is a complete G/A-TD message, made up of four words in the first slot of the array. This prevents the transmission of an incomplete G/A-TD message.

At 18/15 counter-2 time, the second column in the array is readout. This word is then shifted to the message check circuitry, test equipment, and to the conversion equipment for transmission over the phone lines.

As each word is shifted to the conversion equipment and hence to the phone lines, parity of each word is checked. In the parity check circuitry, each word is examined for proper parity (odd). If any word is found to have even parity, a G/A-TD output alarm will be generated. Nevertheless, the word is transmitted over the phone lines regardless of parity.

At 17 counter-17 time the last bit of the second word is readout of the OSR to the conversion equipment; at the same time a pulse is gated to shift the 18/15 counter. When 18/15 counter-3 time, no word is read out of the array. However, a "dummy sync" pattern is generated.

End carry from the 17 counter after the dummy sync will again shift the 18/15 counter to -4 time. 18/15 counter-4 time will readout the third word of the message. From 18/15 counter-4 time to 18/15 counter-5 time, this word is shifted from the OSR to the conversion equipment and message check circuitry. When the next clear column pulse is generated at 18/15 counter-5 time, the fourth word of the message is readout to the OSR. The OSR is then shifted out, under control of the 17 counter, to the conversion equipment and message check circuitry. Thus, the readout operation for the first message slot is completed.

3. Storage

a. Core Storage Arrays

The output words comprising the G/A-TD messages are stored in ferrite core arrays. Each G/A-TD output word is 17 data bits in length, and is stored in one register column of the array. The array has 12 columns and 17 rows and can therefore store 12 output words. (See Figure 3-60.)

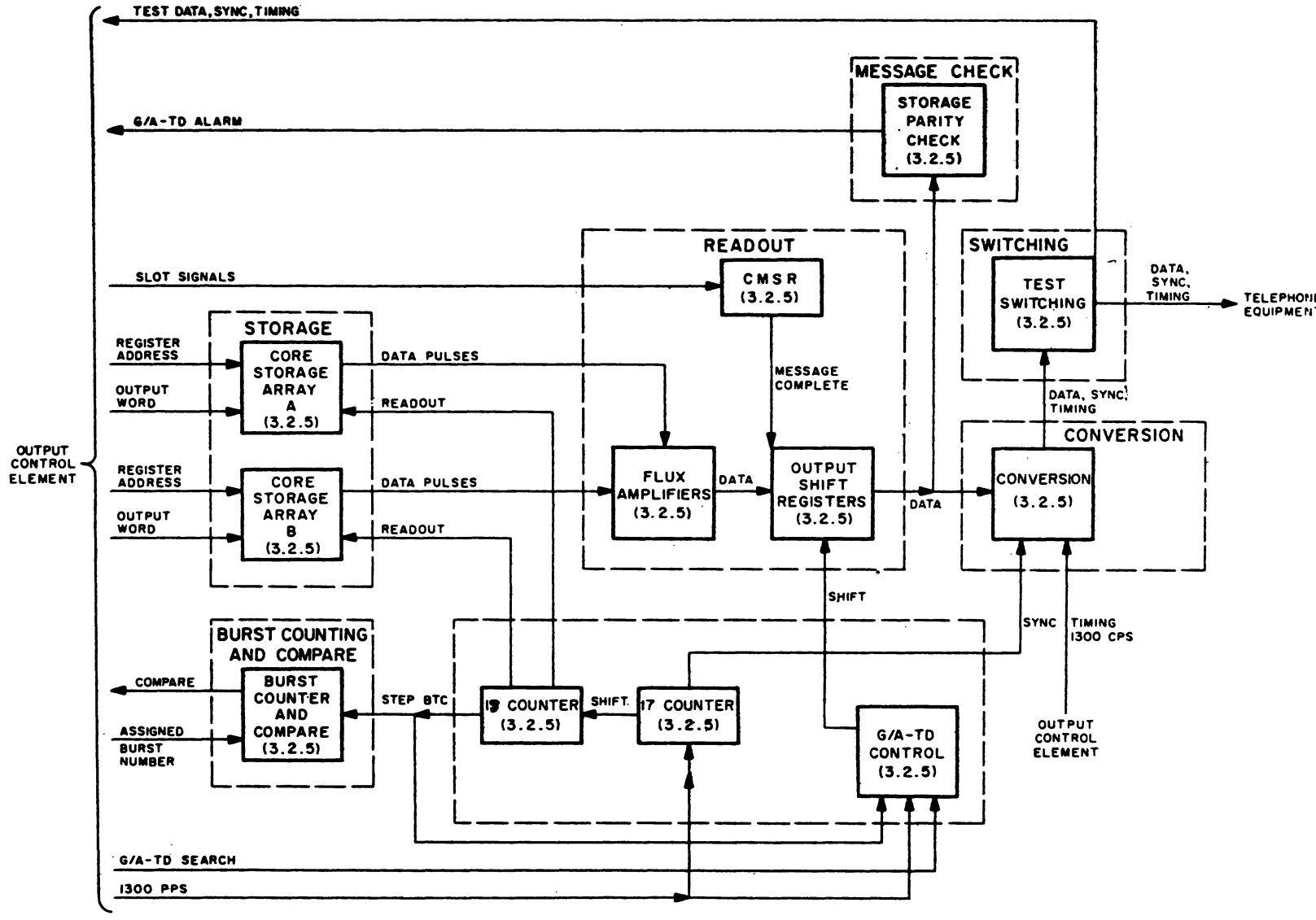


Figure 3-59. G/A-TD Output Storage Section, Simplified Block Diagram

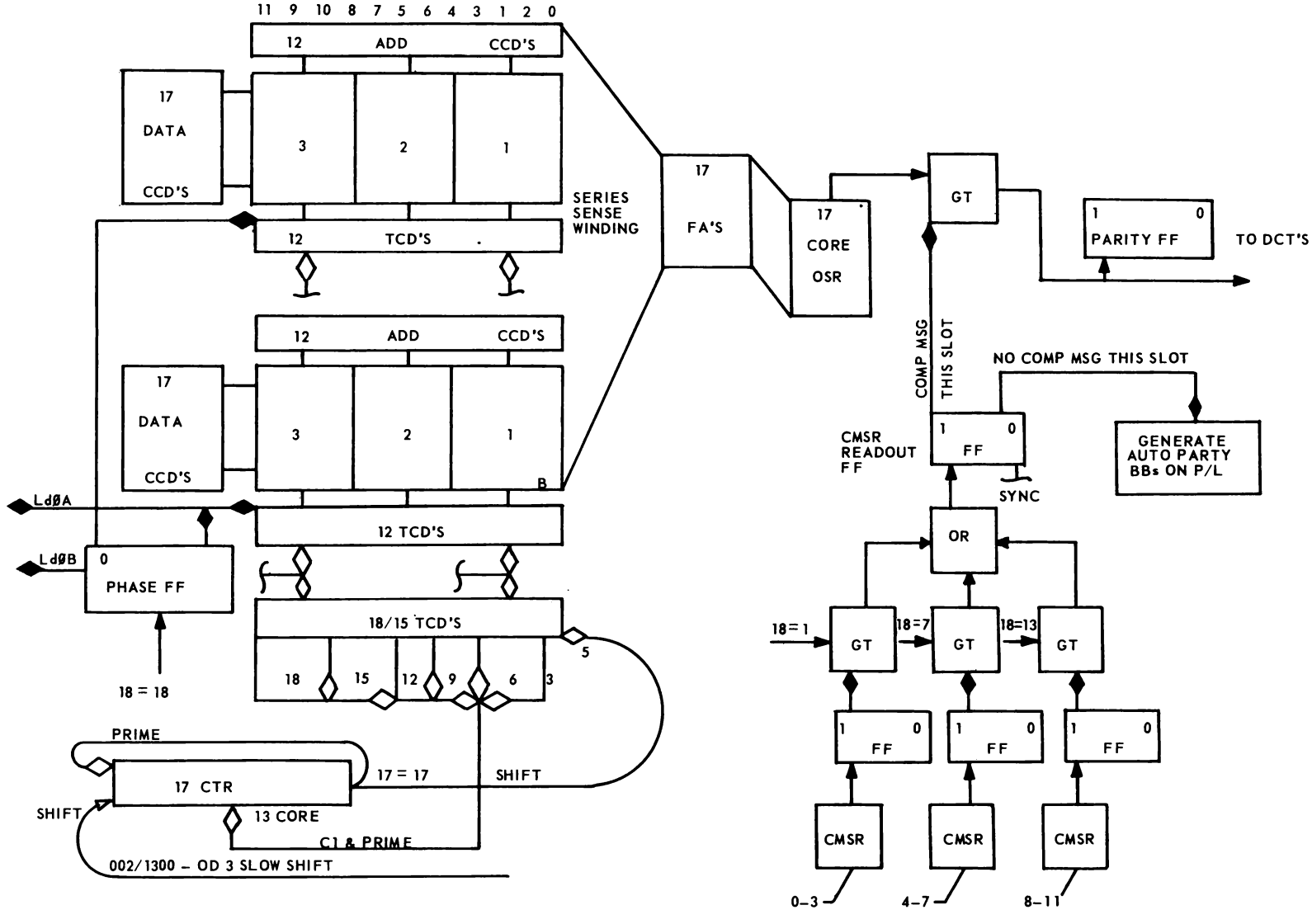


Figure 3-60. G/A-TD Single Channel Block Diagram

Two identical arrays are included to provide more efficient use of the telephone channel. Each array is written into column by column and read out column by column; in this fashion, the G/A-TD storage array is read out word by word rather than bit by bit as in the TTY, and G/G storage sections. As each word is transferred to the core storage array, a half-write current is applied to the register address winding of the column in which that word should be written. Simultaneously, right drum word half-write current pulses are applied to those row windings in which a "1" should be recorded. During readout, a read current pulse is applied to a clear-column winding. Each core in the column receives a full read current, with each core output appearing on the array output winding for its row. Corresponding row array output windings in the two arrays are wired in series. No interference between matrices results, since only one array is read out at a time through use of gated TCD's.

b. Core Array Read-In

During each burst period, G/A-TD message words are written into the core storage array which is not being read out. The right drum with odd parity is applied by the output control element to the core storage array as half-write pulses on those drum word lines whose bits are 1's. The row in the array on which the word is written is specified by the register address contained in the left drum word. Thus, message assembly is accomplished by the assigned burst number and the register address. Since the search period for the OB fields is approximately 176.2 ms, read-in to one array can be completed during the 180 ms readout time for the other array.

The selection of an array for read-in is accomplished by the output control element. The G/A-TD control supplies that element with information on which array is being read out. The output control element, in turn, routes words for read-in into the other array.

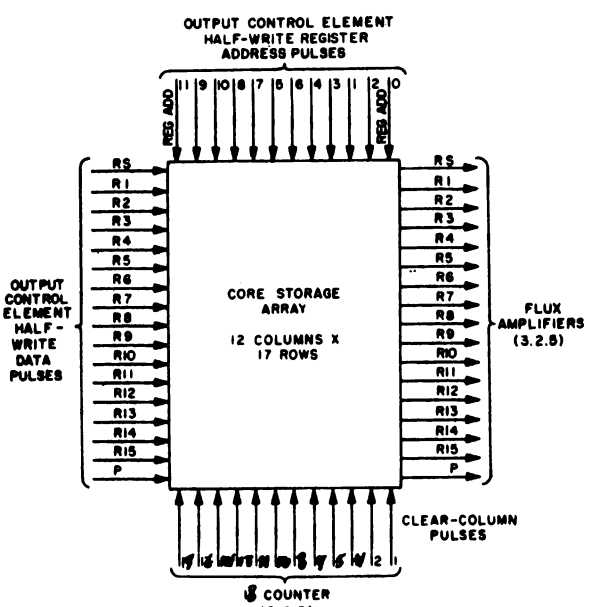


Figure 3-61. G/A-TD Core Storage Array, Simplified Logic Diagram

4. Control

a. General

While many of the control functions of the G/A-TD output storage section are managed by the output control element, certain functions unique to the section are managed by control circuits within the section. The control circuits for G/A-TD are the 17 counter, single channel sync control, the 18/15 counter, and associated control circuits.

b. 17 Counter

The 17 counter, as shown in Figure 3-62, is a 17 core ring counter which is cleared, primed, and then continuously stepped at 1,300 pps. The outputs of this counter are used to control certain functions in the G/A-TD storage section. The controlled functions are:

(1) Generation of the G/A-TD sync pattern.

(2) Stepping of the 18/15 counter.

(3) Slow shifting of G/A-TD words into and out of the OSR.

(4) Generation of parity bits to the phone line in the absence of a G/A-TD message or an incomplete message from the OB drum fields.

At the start of system operation or after a shut-down or test operation, the output control element sends an OD 4 reset-and-prime pulse via OR 1 to the 17-counter shift flip-flop and the G/A-TD control. This OD 4 pulse, in conjunction with the following OD 3 pulse, allows the 17-counter shift flip-flop to produce a 7.5 usec reset level which clears (resets) the 17 counter and the OSR. This reset level (7.5 usec) is again generated whenever the 18/15 counter is stepped to 18/15 counter -3, -6, -9, -12, -15, and -18. The latter reflects those times when a G/A-TD message (four words) has been read out of the OSR to the phone lines or when dummy sync is generated between the second and third word of each message. This same OD 3 pulse is gated to set the 17-counter prime flip-flop, which is normally cleared by a following OD 2 pulse. Setting of the 17-counter prime flip-flop generates a level to prime a "1" into the 13th core of the 17 counter (Figure 3-62). This priming allows for the generation of the G/A-TD sync pattern (00S00) that is required at the beginning of each G/A-TD message. This same sync pattern will also be generated between the second and third word of each message as a dummy sync, however the dummy sync bit will not reach the phone line, as the "single channel sync control" FF will not be set for the generation of dummy sync. The 1 bit is then shifted from the 13th core to the 14th core of the 17 counter; at the same time, the OSR will also be shifted by 2.5 usec shift pulse which is generated from the 17-counter shift flip-flop. During a normal shift cycle, this flip-flop is set by gated OD 2-13 pulses and cleared by the following OD 3 pulses. However, since no information is present in the OSR, the first 0 bit of the G/A-TD sync pattern is now generated. When the 17 counter is shifted to 17-counter-14 time, another 0 is sent to

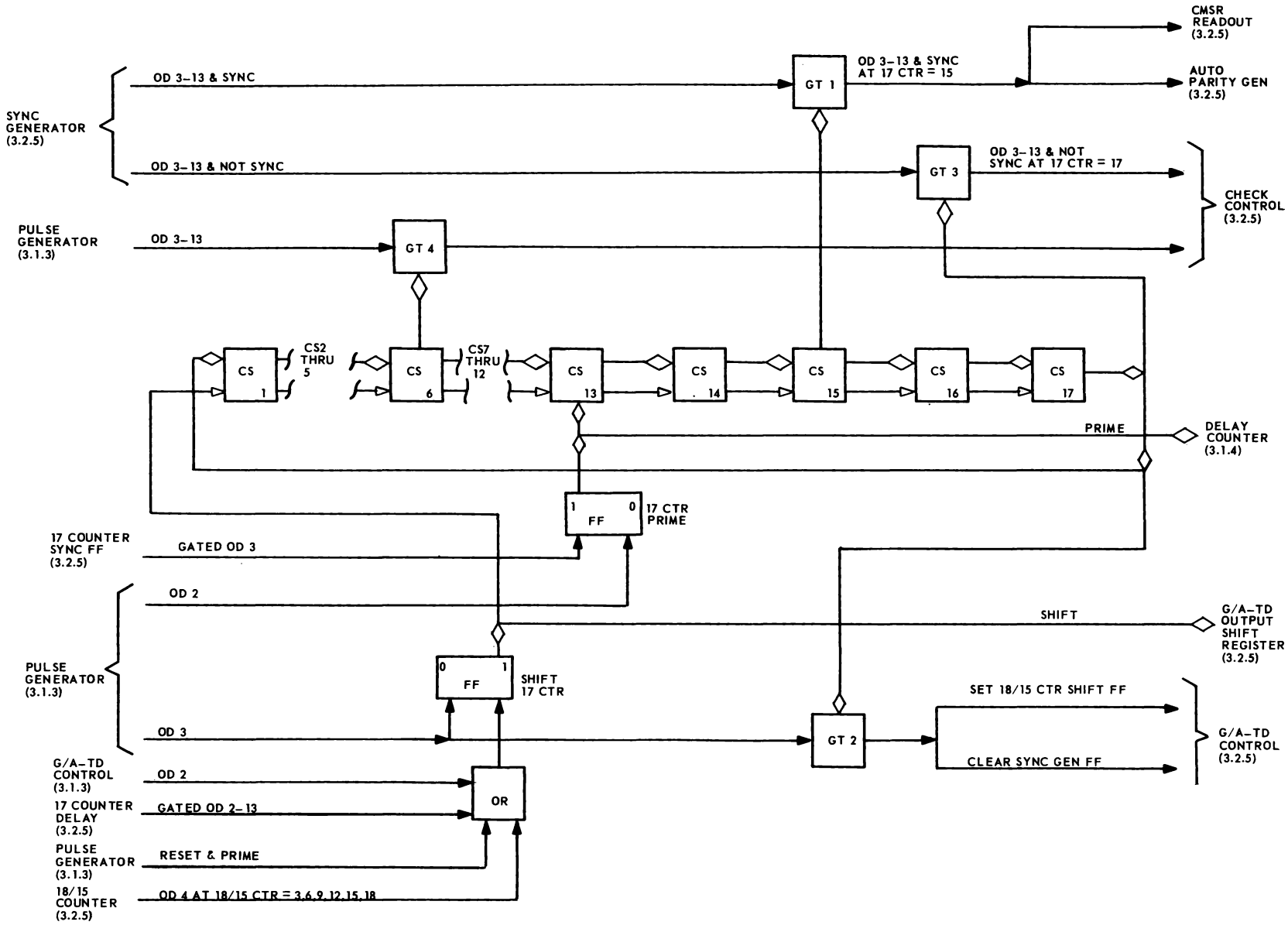


Figure 3-62. G/A-TD 17 Counter (3.2.5)

the phone lines. At 17-counter-15 time, GT 1 is conditioned to pass an OD 3-13 and if the "single channel sync control" FF is set, this sync pulse will set the G/A-TD output sync flip-flop in the DCT, thus providing the synchronizing pulse of the sync pattern. In addition, the gated OD 3-13 and sync pulse clears the automatic parity bits generation flip-flop, thus preventing the generation of spurious 1 bits on the phone line, and clears the CMSR readout FF. Successive stepping of the 17 counter to 17-counter-16 and -17 time generates the remaining 0 bits of the sync pattern.

After the 17 counter steps to 17-counter-17, it returns to prime a 1 bit in the first core of the 17 counter. Since the sync pattern has been generated, this same gated OD 3 pulse will clear the sync generation flip-flop and cause the 18/15 counter shift flip-flop to be set. This, in effect, causes the 1 bit located in a core of the 18/15 counter to be shifted to its succeeding core.

When the 17 counter is shifted to 17-counter-6 time, a level will be generated to condition GT 4. Conditioned GT 4 will pass an OD 3-13 pulse which is sent to the phone lines as an odd parity bit in lieu of G/A-TD words when the latter are absent from the phone lines.

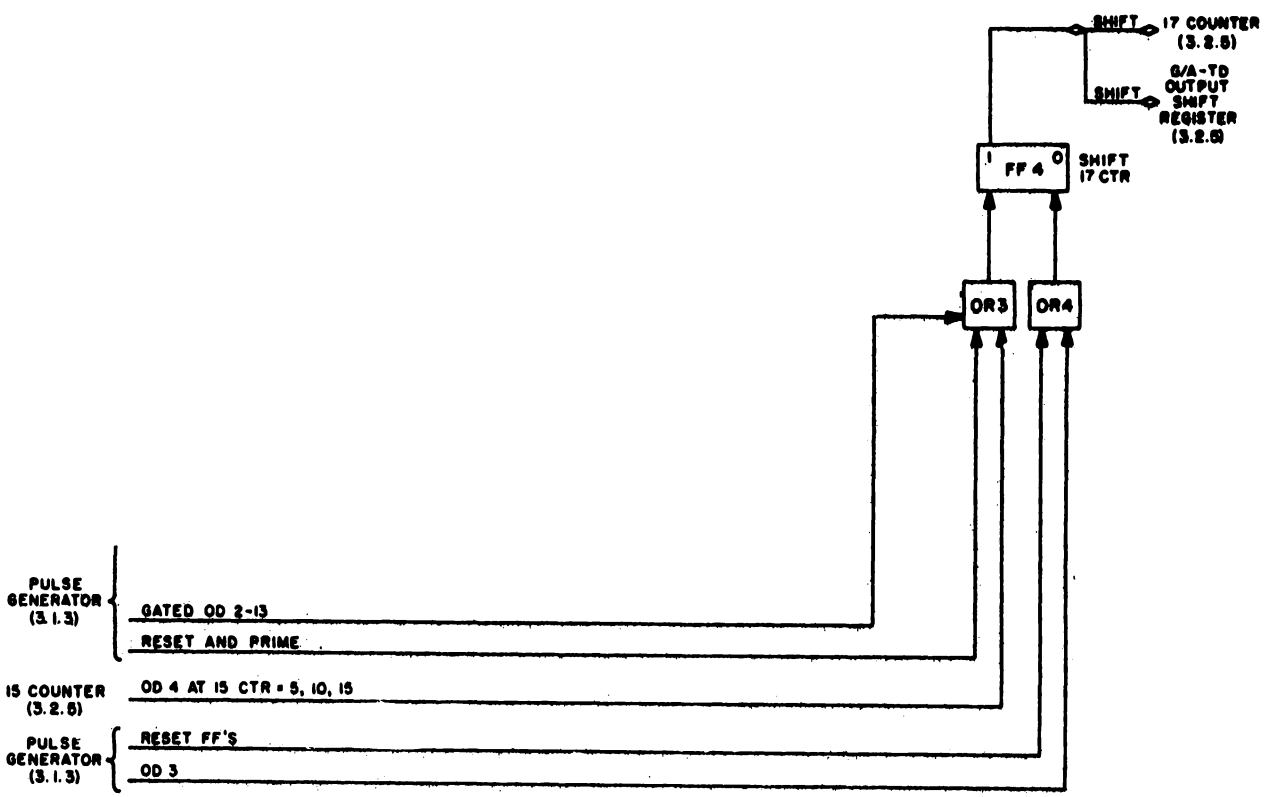


Figure 3-63. G/A-TD 17-Counter Shift Circuits, Simplified Logic Diagram

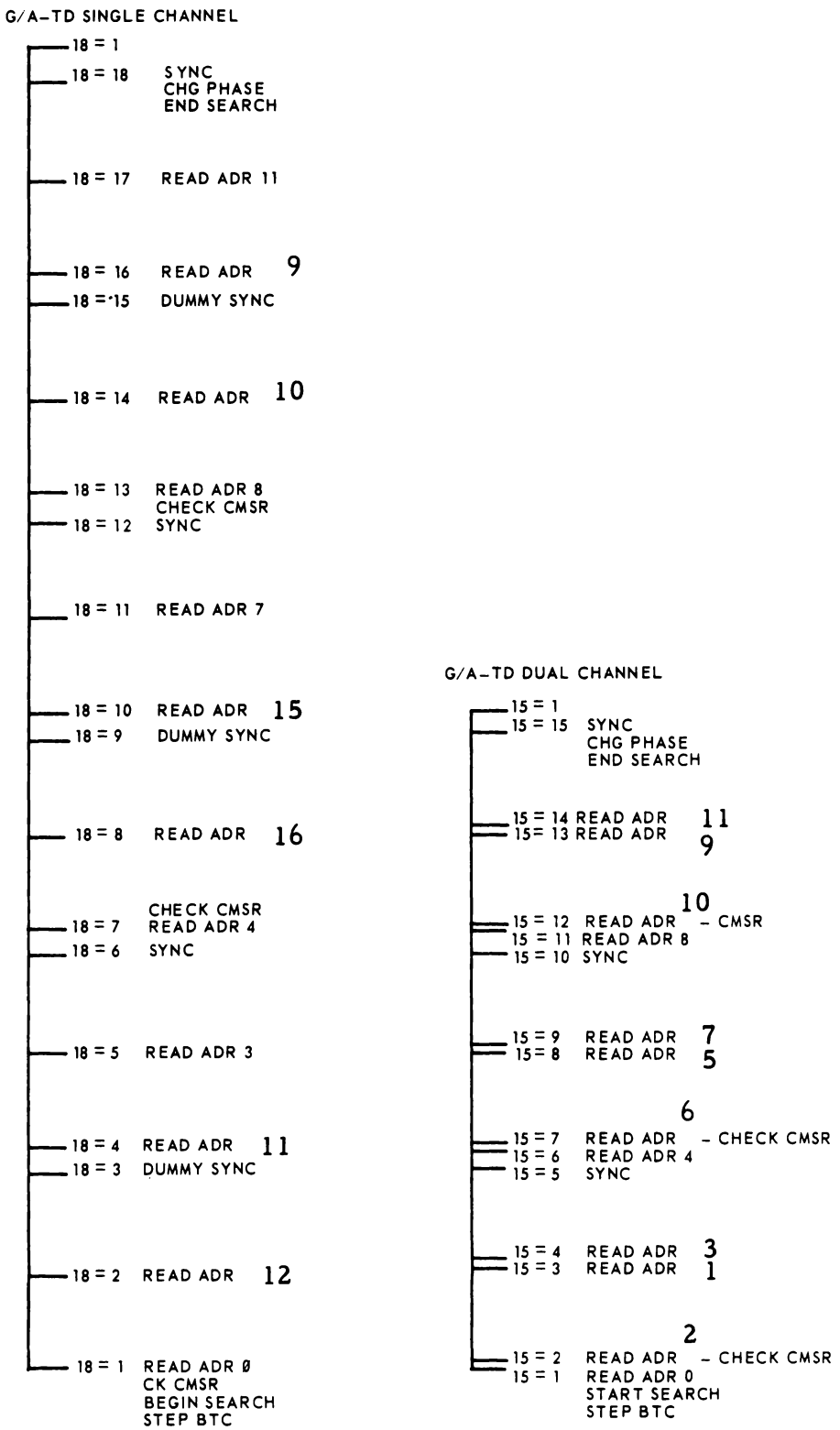


Figure 3-64. G/A-TD Single/Dual Channel Comparison

c. 18/15 Counter

The 18/15 counter is an 18-core shift register which is cleared, primed, and then shifted by an OD 3 pulse at 17-counter-17. The outputs of this counter are used for controlling certain functions in the G/A-TD storage section. These functions are:

(1) Initiating the start of the G/A-TD search period.

(2) Stepping the G/A-TD burst time counter.

(3) Controlling the readout of each column in two arrays.

(4) Initiating the generation of the sync pattern and dummy sync pattern for each succeeding G/A-TD message by resetting and priming the 17 counter.

(5) Changing arrays at the end of each cycle.

At the start of the operation, the 18/15 counter shift flip-flop is set by an OD 3 pulse at 17-counter-17 time. The 18/15 counter shift flip-flop is cleared by a following OD 4 pulse. Thus, the flip-flop generates a 2.5 usec shift pulse to shift the 1 bit from core 1 to core 2 of the 18/15 counter. When the bit is shifted from the first core to the second core in the counter, an output level is generated to condition GT 1 to pass an OD 4-13 pulse. This OD 4-13 pulse is used to set the search flip-flop and to step the G/A-TD burst time counter.

The output level generated by the first core of the 18/15 counter also causes the G/A-TD word contained in the first column of the selected array to be read out into OSR 1. In the interval between 18/15 counter and "1" and 18/15 counter-2 times, the G/A-TD word now contained in OSR 1 is shifted to the conversion equipment, message check circuitry, and test equipment. At 18/15 counter-2 time, the second G/A-TD word is read out of the second column of the selected array into OSR 1. In the interval between 18/15 counter-2 and 18/15 counter-3 time, this G/A-TD word is shifted serially out of the OSR to the phone line. When the counter is shifted to 18/15 counter-3, an output level is generated to condition GT 7 (33EJ), which passes an OD 4 to begin the dummy sync pattern.

At 18/15 counter-4 time the third word is readout of the array to the phone lines. The fourth word is read out of the array at 18/15 counter-5 time and shifted to the phone lines from 18/15-5 to 18/15-6 time.

Readout of G/A-TD message slot 2 is performed in the same manner as that described for G/A-TD message slot 1. However, its readout time occurs from 18/15 counter-7 time through 18/15 counter-12 time.

Similarly, G/A-TD message slot 3 is also read out in the manner described for G/A-TD message slots 1 and 2; however, its readout time is from 18/15 counter-13 time through 18/15 counter-18 time.

At 18/15 counter-1 time, an OD 4 pulse is passed through GT 4 (33GV) to the G/A-TD CMSR circuitry. This OD 4 pulse at 18/15 counter-1 time strobes the gate that is associated with CMSR slot-1 flip-flop. If a complete message has been read into G/A-TD message slot 1, the gate will be conditioned to pass the OD 4 pulse at 18/15 counter-1 time to set the CMSR readout flip-flop. Setting this flip-flop permits the G/A-TD words of message slot 1 to be shifted out of OSR 1 to the phone lines.

The operation described above is again repeated when the 18/15 counter is shifted to 18/15 counter-7 and 18/15 counter-13 time for the subsequent readout of G/A-TD message slots 2 and 3, respectively. The CMSR slot flip-flops (FF's 1, 7, and 8) are subsequently cleared whenever the 18/15 counter is stepped to 18/15 counter-13 time. A completed message check will have been made for each slot by this time.

Whenever the 18/15 counter is shifted to 18/15 counter-6, -12, and -18, GT 8 (33EH) passes an OD 4 pulse to set the sync generation flip-flop, Single Channel Sync Control, the 17-counter shift flip-flop, and also the 17-counter sync flip-flop. Setting these flip-flops permits the generation of the G/A-TD sync pattern which must precede each G/A-TD message. A pulse will also be generated at 18/15 counter-3, -9, and -15, for the generation of dummy sync, between the second and third word of each message. The Single Channel Sync Control FF is cleared for dummy sync generation. The CMSR readout FF is not cleared and the sync bit is not transmitted during dummy cycles.

When the 18/15 counter has completed its operational cycle at 18-counter-18 time, GT 1 (33EH) is conditioned to pass an OD 4-13 pulse. This pulse complements the phase flip-flops and clears the search flip-flop, thus ending the G/A-TD search period. In addition, this 18/15 counter end-carry level is returned to the 18/15 counter shift circuitry, whereupon the 18/15 counter is reset in preparation for a new 18/15 counter cycle.

d. Associated Control Circuits

In addition to the G/A-TD counters that are used for timing and control purposes in the G/A-TD storage section, other control circuitry is required to control the various operations listed below:

(1) G/A-TD search and not-search (g)

(2) Array selection (h)

(3) 18/15 counter shift control (i)

(4) Automatic parity bit generation (j)

(5) 17-counter associated control circuits (k)

e. G/A-TD Search and Not-Search

During search time, the G/A-TD storage section accepts messages from the OB drum fields into its respective core storage arrays. The G/A-TD search and

not-search circuit generates the required search and not-search levels needed to begin and end the G/A-TD read-in operation.

As shown in Figure 3-65, the required G/A-TD search level is generated when the search flip-flop is set, by an OD 4-13 pulse at 18/15 counter-1 time. This flip-flop is cleared by an OD 4-13 pulse at 18/15 counter-18 time. Therefore, search time for a G/A-TD read-in operation is approximately 176.2 ms. When the search flip-flop is cleared, it remains in this state for a period of 3.85 ms. The latter constitutes the not-search period; that is, when no messages will be accepted from the OB drum fields by the G/A-TD storage section.

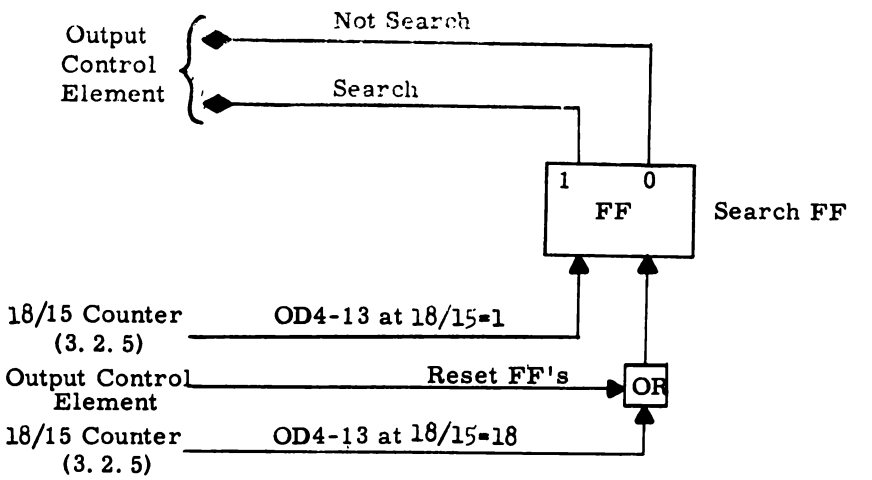


Figure 3-65. G/A-TD Search Flip-Flop, Simplified Logic Diagram

f. Array Selection

The G/A-TD storage section utilizes two core storage arrays which are used to store incoming G/A-TD messages. Since two core storage arrays are used, read-in and readout of the G/A-TD messages can occur simultaneously. The circuit which is used to select and control the G/A-TD read-in and readout operations is the phase circuit.

As shown in Figure 3-66, selection of the particular G/A-TD core storage array to be read out is determined by the phase flip-flop. This flip-flop is complemented by an OD 4-13 pulse whenever the 18/15 counter is at 18/15 counter-18 time. Thus, the core storage array which was read into is now selected to be read out.

g. 18/15 Counter Shift Control

The 18/15 counter shift flip-flop (Figure 3-67) is used to control the shifting of the 18/15 counter with 2.5-usec shift pulses. Subsequent shifting of the 18/15 counter generates clear-column pulses to the core storage array columns to read out the G/A-TD words.

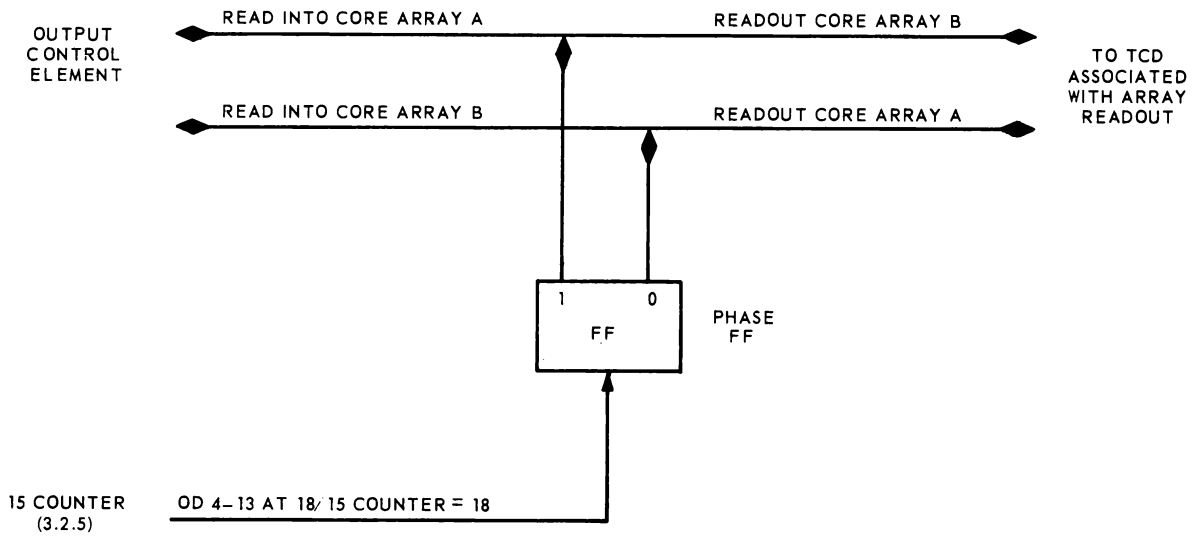


Figure 3-66. G/A-TD Array Selection (3.2.5), Simplified Logic Diagram

The 2.5-usec shift pulses are also used to gate the FA's associated with the core-storage-array data output lines. These FA's, when gated, transfer the G/A-TD data that is read out of the array into OSR 1. Other functions of the G/A-TD shift control circuit are (1) generating a reset level to the 18 counter, (2) checking the CMSR's for completed G/A-TD messages, and (3) priming the G/A-TD CMSR's and the 18/15 counter.

As shown in Figure 3-67, the 18/15 counter shift flip-flop is set by an OD 3 pulse at 17-counter-17 time, and is cleared by the following OD 4 pulse for every shift of the 18/15 counter except when the counter is at 18/15 counter-18 time. Hence, the 18/15 counter shift flip-flop generates shift pulses of 2.5-usec duration which are used to shift the 18/15 counter and to condition the FA's as described above.

When the 17 counter is at 17-counter-17 time, an OD 3 pulse is passed to set the 18/15 counter shift flip-flop. This flip-flop, when set, will cause the 18/15 counter to be stepped by 2.5-usec shift pulses until the counter completes its operational cycle at 18/15 counter-18 time. At that time, a positive level is applied to the inverter. The output of this inverter deconditions GT 1, thus preventing the OD 4 pulses from clearing the 18/15 counter shift flip-flop.

The purpose of inhibiting the clearing of the 18/15 counter shift flip-flop at OD 4 time is to allow a 10 usec level to be generated so that the 18/15 counter may be reset. This reset level is obtained by conditioning GT 2 (the shift flip-flop is set) and strobing it with OD 3 pulses. The OD 3 pulse occurring after the inhibited OD 4 pulse (7.5 usec later) will be passed to clear the 18/15 counter shift flip-flop; at the same time, it will set the 18/15 counter prime flip-flop. The latter primes a 1 into the first core of each CMSR (there are three CMSR's) and also primes a 1 into the first core of the 18/15 counter in preparation for the start of a new 18/15 counter cycle.

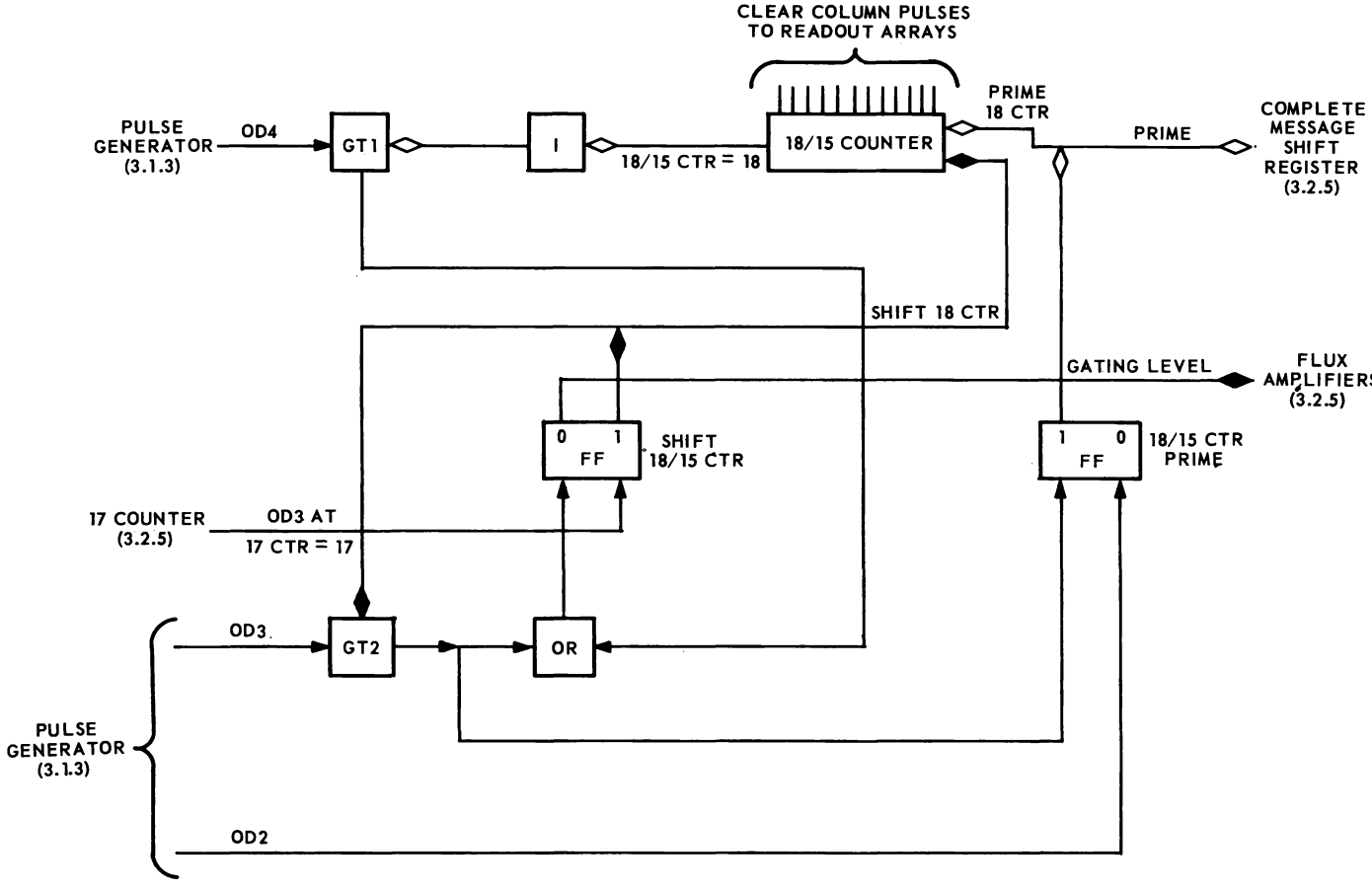


Figure 3-67. G/A-TD 18 Counter Control Circuits (3.2.5), Simplified Logic Diagram

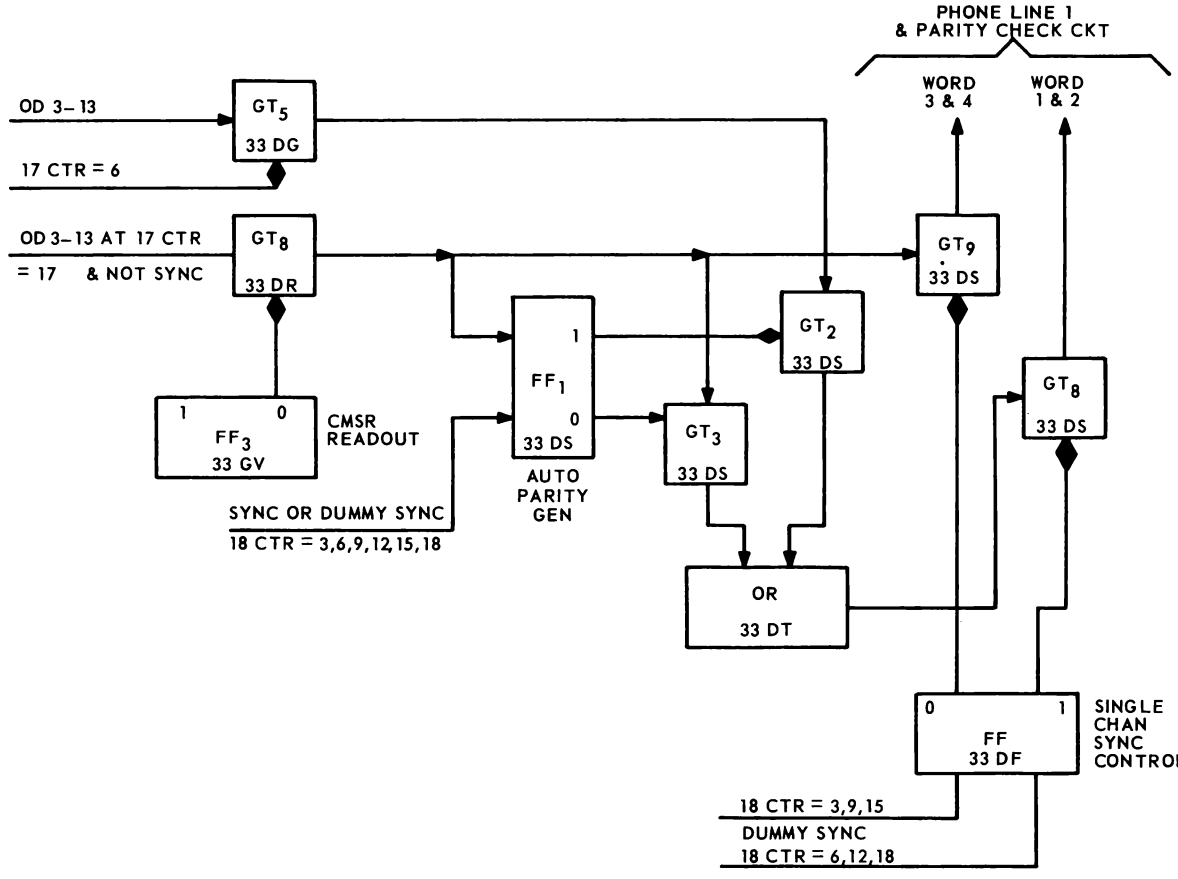


Figure 3-68. G/A-TD Single Channel Auto Parity Bit Generator

h. Automatic Parity Bit Generation

The auto parity generator (Figure 3-68) is used to automatically place parity bits on the G/A-TD data phone lines whenever a particular G/A-TD message slot has not been filled with the prescribed number of four words. In the absence of a complete G/A-TD message, therefore, the auto parity generator will generate four parity bits (one 1 bit per G/A-TD word) to maintain the odd parity bit status required of G/A-TD messages (Figure 3-69). This action also prevents the generation of the G/A-TD output parity alarm. However, it is to be noted that auto parity generation will occur only at those times when particular G/A-TD message slots do not contain the required number of words (four) for transmission on G/A-TD data phone lines. Detailed operation of the parity generator circuit follows.

Recall that the Single Channel Sync Control FF is set for the generation of each sync pattern (18-6, -12, -18) which precedes each message, and is cleared for the dummy sync which comes between the second and third word of every message. The sync pattern preceding each message also clears the Auto Parity Generator FF and the CMSR Readout FF.

During the first normal shift cycle of the 17 counter at 17-15, an OD 3-13-and-sync pulse is generated to clear the Auto Parity Generator and CMSR Readout FF. This same sync pulse is transmitted as the message sync over phone line 1. This sync pulse precedes all G/A-TD messages.

When a slot is not filled, an incomplete-message level (Figure 3-68) is generated off the 0 side of the CMSR Readout FF. The generated incomplete-message level is used to condition GT 8 (33DR).

The sync generator FF produces an OD 3-13-not-sync pulse at the completion of each normal shift cycle (except at the end of the sync cycle) of the 17 counter; that is, at 17-counter-17. Therefore, at the conclusion of each word readout cycle (17 counter cycle), this pulse will be passed by GT 8 (33DR) to strobe GT 3 (33DS) and GT 9 (33DS). This pulse will also set the auto parity generator FF. As the auto parity generator FF was initially in the cleared state, the first OD 3-13-not-sync will be passed by GT 3 (33DS). The OD 3-13-not-sync pulse applied to GT 9 (33DS) will not be passed due to the single channel sync control FF being set at this time. The OD 3-13-not-sync pulse which is passed by GT 3 (33DS), goes through the OR circuit and strobes GT 8 (33DS). As the single channel sync control FF is not set, this OD 3-13-not-sync, which occurred at 17-counter-17 time, will be passed through GT 8 (33DS) to the parity check circuitry and to the data conversion equipment.

The effect of this pulse will be to complement the parity check circuitry, preventing a G/A-TD alarm, and place a 1 bit in the last bit position (Figure 3-69) of the first word in the incomplete message. There will be only one bit transmitted for each word of an incomplete message.

The 17 counter, having completed one cycle, will reprime a 1 bit into its first core and begin a new cycle, for the second word of the message. At 17 counter-6 time, the 17 counter will condition GT 5 (33DG) which is strobed by OD 3-13 pulses. The OD 3-13 pulse occurring at 17 counter-6 time will be passed by GT 5 (33DG)

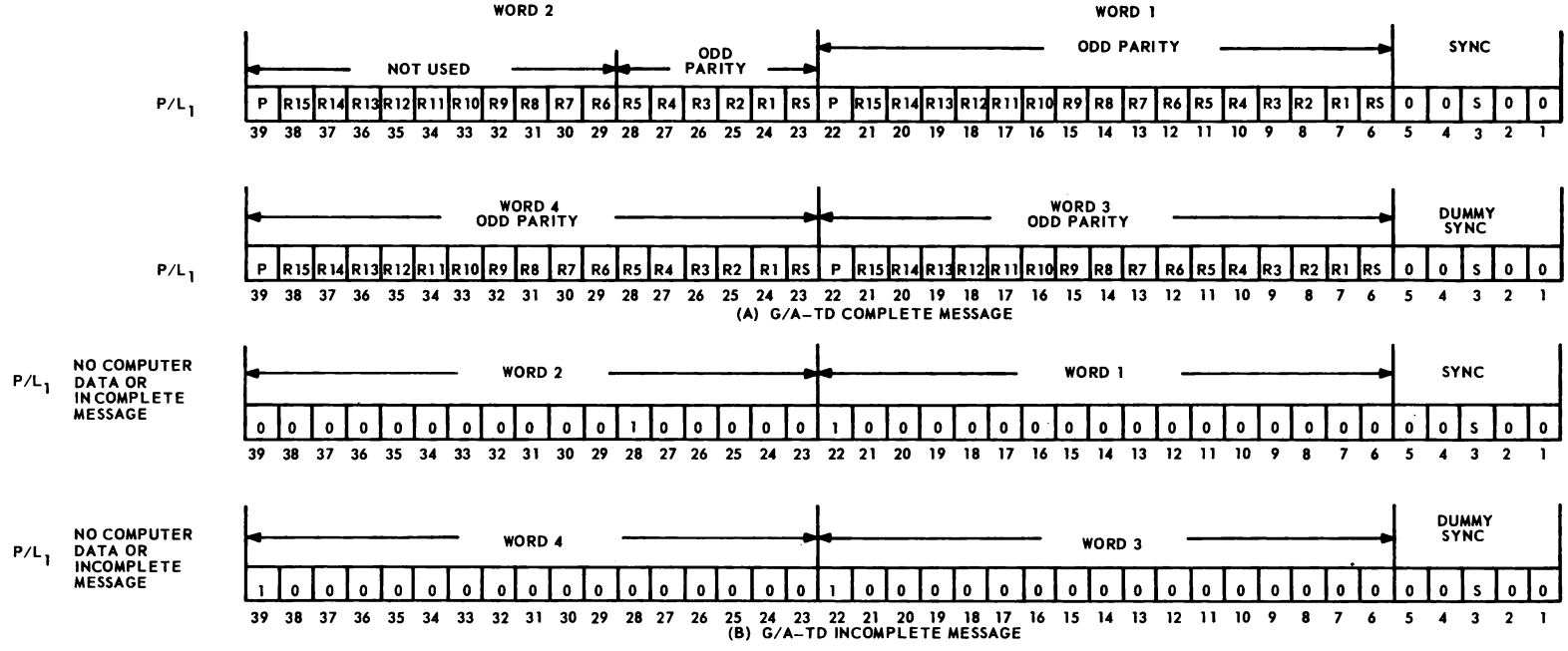


Figure 3-69. G/A-TD Word Message Layout

to strobe GT 2 (33DS), which is conditioned by the auto parity generator FF, through the OR circuit to GT 8 (33DS), and hence to the parity check and data conversion circuits. The 17 counter will continue to shift to 17-counter-17, which represents the end of the second word of the incomplete message. Notice, that for the second word of the message only the first six bits are used and that the auto parity BB was effectively placed on the phone line in the sixth bit position of word 2 of the message. The dummy sync pattern is generated after the second word of each message. The generation of the dummy sync (18 counter-3, -9, and -15) pattern will clear the auto parity generator FF and also clear the single channel sync control FF.

At the end of the dummy sync pattern the 17 counter completes a normal cycle equivalent to a word 3 cycle. With the 17-counter-17 OD 3-13-and-not-sync pulse GT 8 (33DR) is once again checked and found to be conditioned. Getting out of GT 8 (33DR), this OD 3-13-not-sync pulse will check two GT's, GT 3 (33DS), and GT 9 (33DS). Both GT's are conditioned, the GT 3 by the auto parity generator FF having been cleared by the dummy sync, and GT 9 by the 0 side of the single channel sync control which was also cleared by the dummy sync pattern. Notice that the pulse which is passed by GT 3 and strobes GT 8 (33DS), cannot be passed by GT 8 as the single channel sync control FF is now cleared. The OD 3-13-at-17 counter-17-and-not-sync pulse which initially strobed GT 9 (33DS), will be passed to the parity checking circuits and also to the data conversion equipment and hence to the phone line. Again the 17 counter will cycle, and a fourth 17 counter-17 OD 3-13-not-sync pulse will be generated. This fourth OD 3-13-not-sync pulse will strobe GT 8 (33DR) and get out to GT 3 and GT 9. The pulse is gated out of GT 9 to the parity check circuit and to the phone lines as an auto parity BB in the last bit position of word four. As this represents the last bit of the last word of the message, a sync pattern will now begin for the next message to be transmitted.

To reiterate, there are four words in a G/A-TD message. As the parity of these words (individually) is odd, all zeros cannot be transmitted over the phone line in lieu of a message. The auto parity generator circuit will provide a one bit in the last bit position of each word. As the second word of the message only uses six bits, the auto parity BB is placed in the sixth bit position of word two. The readout of the OSR is controlled by the 17 counter shift FF; therefore, the seventeenth shift of the 17 counter corresponds to shifting of the last bit of the OSR.

The first 17 counter-17 and OD 3-13-not-sync pulse of a message, checks a GT off the 0 side of the CMSR Readout FF. If this GT is conditioned (indicating an incomplete message/slot), the auto parity generator FF is set and the OD 3-13-not-sync pulse is gated to the parity check and data conversion circuits. During the second cycle of the 17 counter (word 2 cycle), at 17 counter-6, an OD 3-13 pulse is gated off the 1 side of the auto parity generator FF to the parity check and data conversion circuits. Notice that this effectively places the auto parity BB in the sixth bit position of word 2. Dummy sync is always generated after the second word cycle of all G/A-TD messages. The dummy sync will clear the single channel sync control FF and the auto parity generator FF. The next two cycles of the 17 counter (representing words 2 and 3), 17 counter-17, OD 3-13-not-sync pulse will be gated through the GT 8 (33DR), off the 0 side of the CMSR Readout FF, to a GT 9, conditioned by the single channel sync control FF being clear, to the auto parity BB for words two and three of the incomplete message.

As this represents the end of the incomplete message, sync will be generated for the next message to be transmitted.

i. Associated Control Circuits, 17 Counter

The control circuits associated with the 17 counter are the 17-counter sync flip-flop, and the 17-counter prime flip-flop. As shown in Figure 3-70, the 17-counter-sync control circuit is used to set the 17-counter prime flip-flop, initiate the start-delay pulse to the delay counter, and, when used in conjunction with the 17-counter prime flip-flop, control the priming of both the delay counter and the 13th core of the 17 counter. The detailed operation of both the 17-counter sync flip-flop and 17-counter prime flip-flop follows.

When the 18/15 counter is shifted to the following 18/18 counter-3, -6, -9, -12, -15, and -18 times, an OD 4 timing pulse is gated to set the 17-counter sync flip-flop via OR 1. Setting this flip-flop conditions GT 1, which is strobed by an OD 3 pulse. This OD 3 pulse is passed by conditioned GT 1 to set the 17-counter prime flip-flop; it is also sent to the start delay flip-flop in the test equipment section and to clear the 17-counter sync flip-flop via OR 2.

With the setting of the 17-counter prime flip-flop, a level is caused to be generated which is subsequently used to prime a 1 bit in the 13th core of the 17 counter, thus providing the start of the sync pattern generation cycle as well as priming a 1 bit in the first core of the delay counter in the test equipment section. The 17-counter prime flip-flop is then cleared at the following OD 2 time, thus ending the functions of the control circuits associated with the 17 counter.

5. Readout

a. General

Readout of all G/A-TD messages is accomplished as follows:

(1) Readout G/A-TD word 1 from selected array.

(2) CMSR filled; readout complete G/A-TD message to G/A-TD data phone lines. CMSR not filled; generate auto parity BB for each word.

(3) Readout G/A-TD word 2 from selected array.

(4) Generate dummy sync pattern.

(5) Readout G/A-TD word 3 from selected array.

(6) Readout G/A-TD word 4 from selected array.

(7) Generate sync pattern for next message.

The above steps represent the mode of readout operations required for all G/A-TD single channel messages. The following paragraphs contain discussions relating

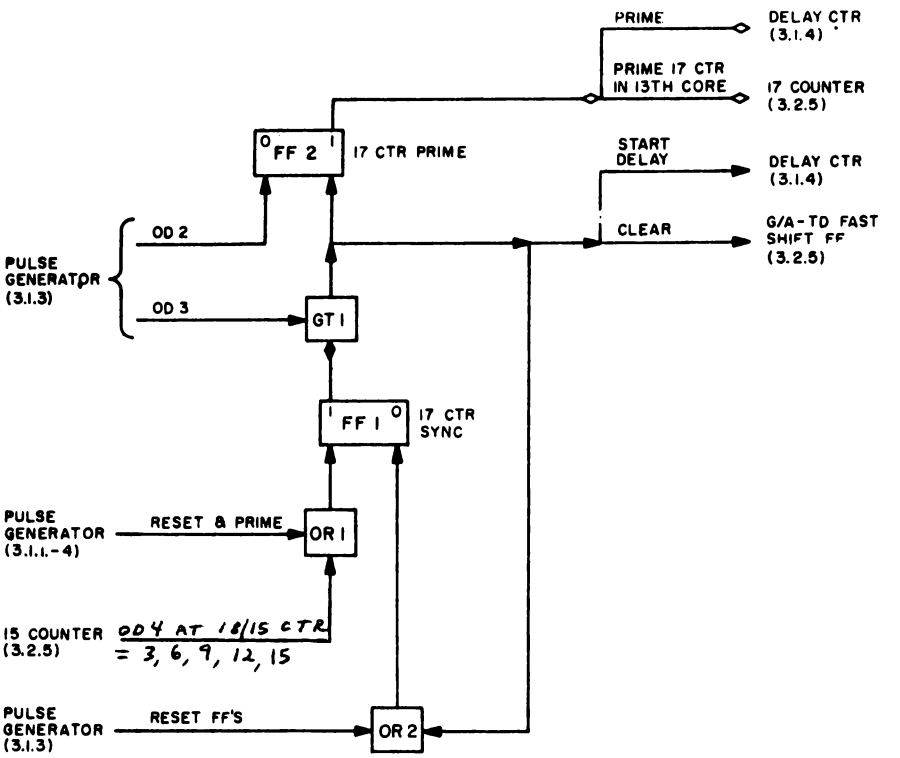


Figure 3-70. Associated Control Circuits, 17 Counter, Simplified Logic Diagram

to the readout operations required to readout one of the three G/A-TD message slots from the G/A-TD core storage arrays.

b. Core Array Readout

Each G/A-TD message is read out of the G/A-TD core storage arrays one 17-bit column at a time, through FA's into OSR 1. This word will be shifted serially out of the OSR to the data conversion equipment under the control of the G/A-TD completed message shift register.

As mentioned previously, each G/A-TD message slot is read out of the core array by columns during the G/A-TD burst period. Each core array is comprised of 12 columns which are pulsed serially by clear-column pulses that are applied by the TCD's associated with the 18/15 counter. Each time a column is pulsed, the 17 bits (representing a complete G/A-TD word) stored in its cores are shifted in parallel form to the FA's.

Each of the 17-bit output pulses from the G/A-TD core storage array is applied to an FA. A 1-bit is represented by a pulse, and a 0-bit is represented by the absence of a pulse. Each FA, shown in Figure 3-71, is gated by a gating level emanating

from the 0 sides of the 18/15 counter shift flip-flop. These levels are 2.5-usec negative pulses (OD 3 at 17-counter-17 to OD 4) used to prevent noise and spurious signals from passing through the FA's. These pulses are produced in the G/A-TD control coincident with each shift of the 18 counter that occurs during readout time. (Refer to 4.f.) Since these 18-counter shifts generate clear-column pulses which read columns of the core array, the core storage array outputs are applied to the FA's during the 2.5-usec period that the FA's are gated and made operative.

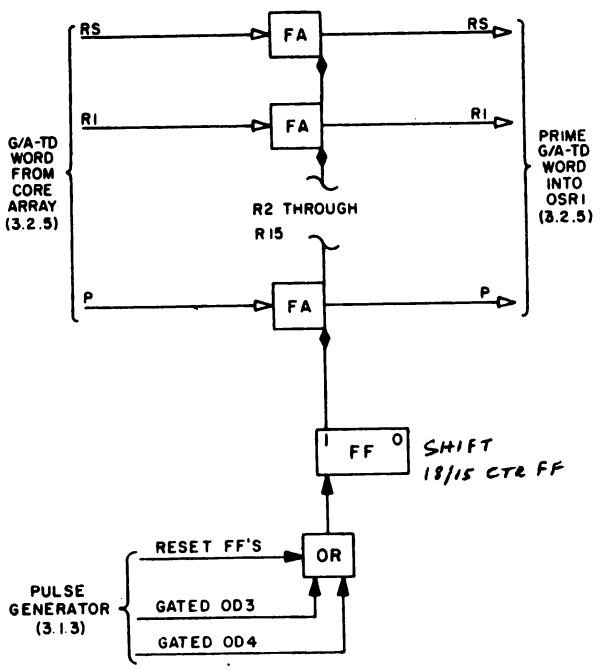


Figure 3-71. G/A-TD Flux Amplifiers (3.2.5), Simplified Logic Diagram

The FA's after amplifying the array output pulses, send the pulses to the OSR as FA outputs. The outputs from the FA's are sent over 17 lines labeled RS to R15 including P, respectively.

c. Output Shift Register (OSR)

The G/A-TD single channel storage section utilizes one OSR which stores one G/A-TD word at one time (Figure 3-72). This OSR is comprised of a 17-core shift register which is shifted at one specific rate. This is called the normal shift rate which occurs at 1,300 pps and is used to shift the G/A-TD words out of the OSR onto the G/A-TD data phone line and parity checking circuit.

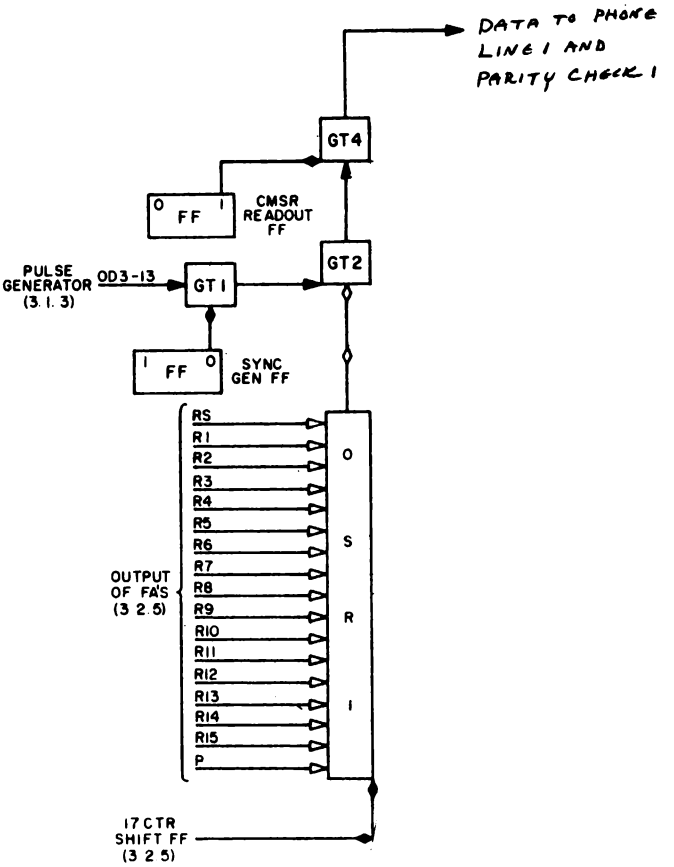


Figure 3-72. G/A-TD Output Shift Register, Simplified Logic Diagram

Figure 3-72 is a representative diagram of the G/A-TD OSR 1 and its associated circuitry. The OSR is shifted under the control of the 17-counter shift flip-flop. Readout of the G/A-TD words from OSR 1 to the data phone lines depends upon the CMSR flip-flop being set. The set condition of this flip-flop indicates that a complete message is contained in a particular G/A-TD slot, that this message is ready to be read out of the OSR and that the sync generator flip-flop is clear. The latter flip-flop, when cleared, indicates that the sync pattern required to precede all G/A-TD messages has been generated or that dummy sync is not being generated, and the readout of the G/A-TD message can now be executed.

During normal operation, a G/A-TD word is read into OSR 1 from the selected core storage array under control of the 18/15 counter. The G/A-TD word now stored in OSR 1 is readout to the data phone lines under control of the 17 counter shift FF. Readout of the G/A-TD word from the OSR to the data phone line will be effected in serial form at a shift rate of 1,300 pps.

For every 1 data bit that is read out of the OSR, the GT 6 (33DP 8B) associated with the OSR will be conditioned. Conditioned GT 6 will pass the gated OD 3-13

pulses passed by the previously conditioned GT 8 (33DP 8B), which is conditioned by the 0 side of the sync generator FF, to strobe the CMSR GT 7 (33DP 8E). If the CMSR readout FF has been set, GT 7 will be conditioned to pass the 1 bits of each G/A-TD word on to the data phone line and the parity check circuitry.

The above readout cycle is again repeated for the second word of the G/A-TD message. Upon completion of readout for the second G/A-TD message word, the dummy sync pattern is initiated. 18-counter-3, -9, -15 will generate what is known as a dummy sync pattern, between the second and third word of each G/A-TD message word. 18 counter-3, -9, and -15 condition a 270 OR circuit (33EJ 7A) which will in turn condition GT 7 (33EJ 6A) to pass an OD 4 pulse. This OD 4 will set the sync generator FF, clear the single channel sync control FF, set the 17 counter shift FF, and set the 17 counter sync FF. This will cause the 17 counter to be reset and primed to the 13th core. The 17 counter will be stepped to 17 counter-13, -14, and then -15. At 17 counter-15, an OD 3-13 pulse is passed by GT 8 (33EG 4C). This pulse will clear the auto parity BB FF, and strobe a GT 9, which is conditioned by the one side of the single channel sync control FF. As the single channel sync control FF is now clear, this pulse will not be passed, and therefore the G/A-TD output sync channel FF will not be set and CMSR readout FF will not be cleared in the dummy sync pattern as is normally done in sync generation. The remaining two shifts of the 17 counter provide the last two 0's of the dummy sync pattern. At 17 counter-17, GT's 6 and 7 (33EG 4C) will be conditioned and GT 6 will pass an OD 3 pulse which will clear the sync generator FF and set the 18 counter FF. The 18 counter shift FF being set with OD 3 and cleared by an OD 4 pulse, will shift the 18 counter to 18 counter-4, -10, or -16, causing the third word of the message to be read out of the selected array and into the OSR. This word will then be shifted to the data phone line, and the parity check circuitry. Upon completion of readout for this word the fourth word will then be readout of the selected array to the OSR and out to the data phone line 1. This concludes the readout of the message. At the end of each message, a sync pattern is generated for the next message.

It is observed that as data is shifted out of OSR 1 to the phone lines, this same data is also shifted into OSR 2. However, data from OSR 2 is not checked for parity nor is any of this data permitted to be transmitted to the phone line, because relays 33NEK1, and K2 are not picked in single channel operation (see logic 3.2.5 4E).

d. Completed Message Shift Register

The G/A-TD completed message shift register (CMSR) (Figure 3-73) counts the number of G/A-TD output words written into each slot in the core storage array. If four G/A-TD words were written into a slot during the previous burst period, the completed message in that slot will be passed through the OSR's to the conversion equipment. If the message slots do not contain the required complement of four words per slot, no messages are read out and the auto parity generator will be caused to generate odd parity bits on the data phone lines.

As shown in Figure 3-73, three G/A-TD CMSR word counters are used, each capable of counting and recording the required four words needed to complete a G/A-TD message slot. Preparatory to the read-in and counting of the G/A-TD words during a burst period, the three G/A-TD CMSR slots are primed under the control of the 18/15 counter prime flip-flop. The latter flip-flop primes a 1 into the first core

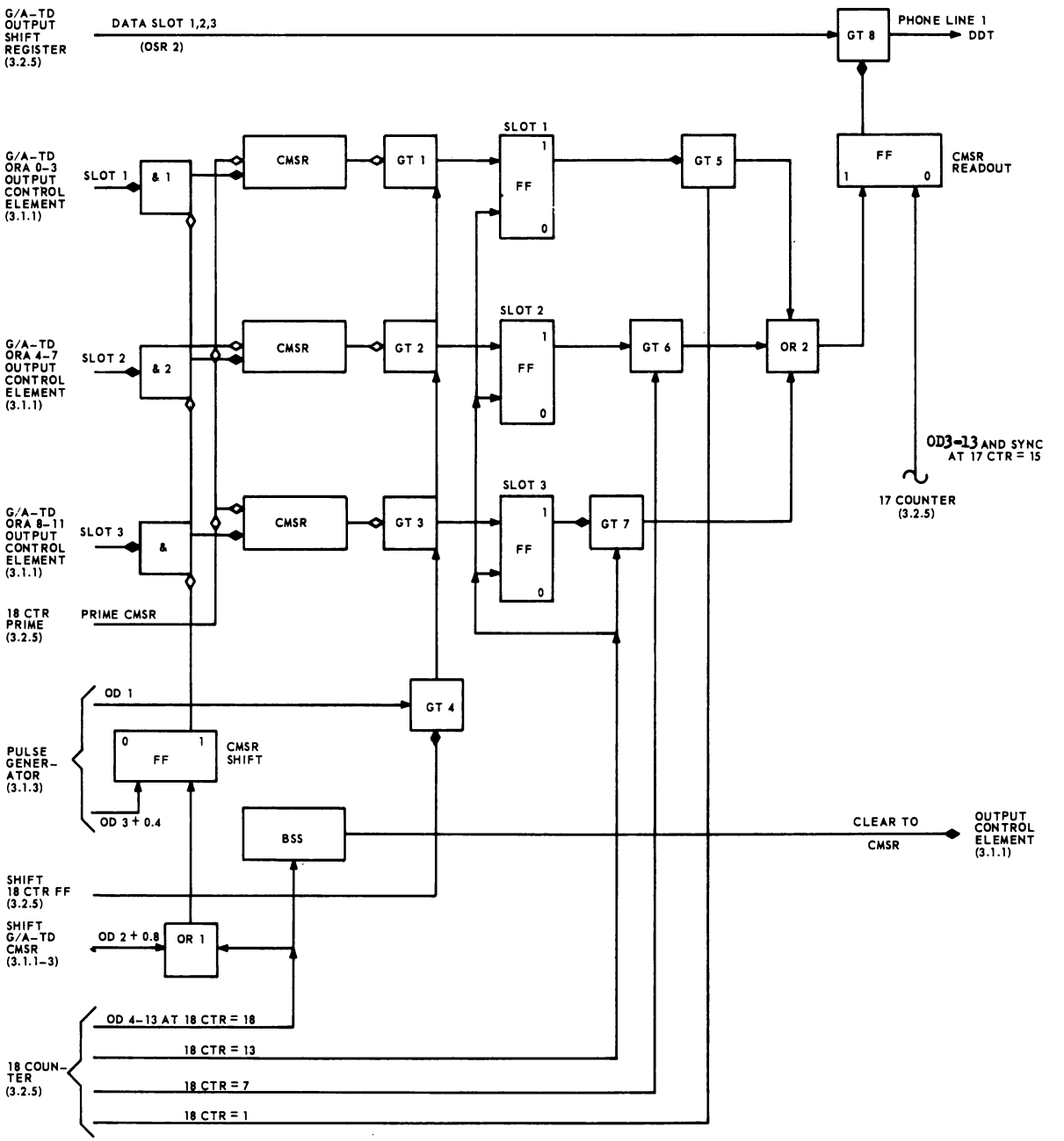


Figure 3-73. G/A-TD Completed Message Shift Register (3.2.5)

of each CMSR, and also primes a 1 into the first core of the 18/15 counter, prior to beginning each burst period.

Assuming that the ORA's of the G/A-TD words to be read in are addresses 0 through 3 (message slot 1), a conditioning, slot-1, level will be applied to one of two input lines of the 2-way AND circuit (AND 1 of Figure 3-73). Coincident with this level, a CMSR shift pulse (parity OK OD 2+0.5) is supplied through OR 1 to set the CMSR shift flip-flop. Setting this flip-flop causes a +10v level (2.5 usec duration) to be applied to one input line of all three 2-way AND circuits associated with the G/A-TD CMSR's. The AND 1 circuit will be conditioned for a period of 2.5 usec to shift the 1 bit that has been primed into its associated CMSR. This 1 bit is shifted one core at a time for each G/A-TD word that is read into message slot 1 of the selected core storage array. Thus, the CMSR counts the G/A-TD words contained in message slot 1 as these words are being read into the selected core storage array.

When a complete message has been read into the selected core storage array, the 1 bit will be located in the last core of the CMSR for slot 1. This operation, in effect, completes the read-in operation of the G/A-TD message in slot 1 during a G/A-TD burst period. Similarly, the operation described above will also take place for message slots 2 and 3 when these are being read into the selected core storage array.

The read-in operation of the G/A-TD words into a selected core storage array is completed when the 18 counter is at 18-counter-18 time. At this time, the following operational steps take place:

(1) An OD 4-13 pulse is gated to complement the phase flip-flop (Figure 3-66) to select for read-out the core storage array that has just been read into.

(2) This OD 4-13 pulse clears the search flip-flop (Figure 3-65) ending search time.

(3) This OD 4-13 pulse sets the CMSR shift flip-flop. The latter, when set, generates a level (+10v) that is applied to one input line of all three 2-way AND circuits associated with the CMSR's.

(4) The OD 4-13 pulse also causes a single-shot multivibrator to fire; thus, a 25-usec level (+10v) is applied to the remaining input lines of the three 2-way AND circuits and conditions these circuits.

The output of all three conditioned AND circuits is a reset level (7.9-usec duration) that is applied to reset each of the respective CMSR's. Resetting the CMSR's causes the 1 bits that are located in the last cores of each to be shifted out to condition the respective gate of each CMSR. All three gates (GT's 1, 2, and 3) are strobed by an OD 1 pulse that is passed through GT 4 only when the 18-counter shift flip-flop is set (for 10 usec) at 18-counter-18 time.

Since GT's 1, 2, and 3 are conditioned, the OD 1 pulse which strobes each individual gate is passed to set the CMSR slot flip-flops. These flip-flops, when set, generate a conditioning level to their associated gates (GT's 5, 6, and 7). Conditioning the individual gates indicates that the message slot associated with each has been filled.

During the following 18-counter cycle, at 18-counter-1 time, an OD 4 pulse is gated to strobe GT 5. If a complete G/A-TD message was read into slot 1, the OD 4 pulse is passed through the OR 2 circuit to set the CMSR readout flip-flop. This flip-flop is cleared during the generation of the G/A-TD sync pattern (00S00) by an OD 3-13-and-sync pulse which occurs at 17-counter-15, but not during the generation of the dummy sync pattern. Setting the CMSR readout flip-flop causes a level to be generated to condition GT 8, thus allowing for the subsequent readout of the complete G/A-TD message that was stored in slot 1 of the selected core storage array.

The readout operation for G/A-TD message slots 2 and 3 is the same as the operation described for message slot 1, with the exception that, for the readout of G/A-TD message slot 2, the gated OD 4 pulse is passed by GT 6 to set the CMSR readout flip-flop at 18/15 counter-7 time, and for the readout of G/A-TD message slot 3, the gated OD 4 pulse is passed by GT 7 to set the CMSR readout flip-flop at 18/15 counter-13 time. At 18/15 counter-13 time, this same OD 4 pulse also clears CMSR FF's 1, 2, and 3.

Should a particular G/A-TD message slot not contain the required four words necessary for a complete message, the particular gate associated with the incompleted message slot will remain deconditioned; hence, its respective CMSR slot flip-flop will remain cleared. Therefore, at the 18/15 counter-equals time for that particular slot, no pulse will be gated to set the CMSR readout flip-flop, and no message readout can occur for that slot.

6. Parity Check

As the G/A-TD words are read out of the storage section to the data phone lines, a parity check of each word is performed. The parity of all G/A-TD words must be odd. However, if any G/A-TD words contain an even number of 1 bits, a G/A-TD output alarm is generated and the word containing the even number of 1 bits is nevertheless transmitted to the data phone lines.

Each G/A-TD word is simultaneously read out to the data phone line and the parity checking circuit. In the parity checking circuit (Figure 3-74) the G/A-TD word data for data phone line 1 is supplied through OR 2 to complement the parity check 2 flip-flop. Should the transmitted G/A-TD word on data phone line 1 be of the correct parity (odd) no alarm will be generated. Conversely, if the G/A-TD word has an incorrect parity (even) when transmitted over data phone lines 1, the parity checking flip-flop associated with the incorrect word will be clear at the end of the parity check operation.

If either of the parity check flip-flops is clear, a level is generated through OR 4 to condition GT 2. Conditioned GT 2 is strobed by and passes a gated OD 1 pulse to initiate the G/A-TD output alarm. This OD 1 pulse is passed through GT 1 when the parity check control flip-flop is set. This flip-flop is set by an OD 3-13-not-sync pulse when the 17 counter is at 17-counter-17 time. This pulse appears in coincidence with the readout of the last data bit of every G/A-TD word that is transmitted over data phone line 1. The parity check control flip-flop is cleared by the gated OD 1 pulse, 5 usec after it was set. Clearing this flip-flop ends the parity checking operation for

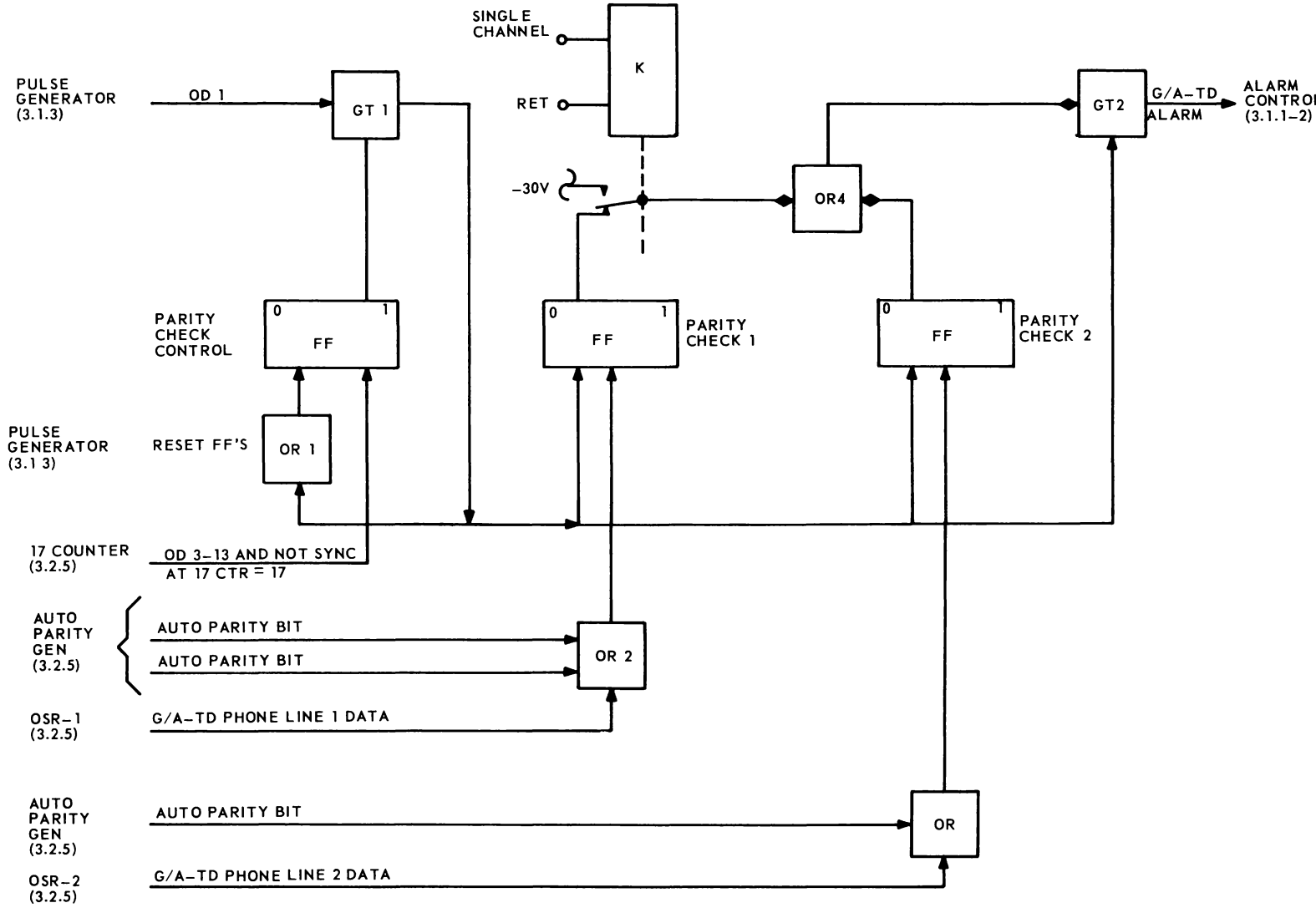


Figure 3-74. G/A-TD Parity Check Circuit (3.2.5), Simplified Logic Diagram

the transmitted G/A-TD word and, at the same time, readies the parity checking circuitry to check the parity of the next G/A-TD word to be transmitted.

In the absence of a complete G/A-TD message, the auto parity generator (Figure 3-68) generates an odd parity bit in lieu of an absent G/A-TD word. The data 1 bits generated by the parity generator are fed to OR 2 to complement the parity check flip-flop associated with the data phone line, thus ensuring that no G/A-TD alarm is generated.

7. Burst Sequence and Timing

a. General

The G/A-TD burst counter and compare circuit and the burst number of the assigned G/A-TD message are the basic means employed to control the order and time of transmission of messages.

The assigned burst numbers of each drum word are compared to the current contents of the burst counters. If the assigned burst number is equal to the contents of the G/A-TD burst counter, and if all the other conditions are favorable, the word is accepted by the Output System.

To be sure that the message is transmitted in proper sequence and at the proper time, the Central Computer System assigns a burst number to each G/A-TD message to which the reading of the G/A-TD burst counter will be equal at the predicted transmission time. Each word of a burst is assigned the same burst number by the Central Computer System. To make it possible for the Central Computer System to determine this burst number, it is given access to the current readings of the G/A-TD burst counter through the output computer section of the output control element.

b. Burst Counter

The G/A-TD burst counter (Figure 3-75) is a standard 7-bit flip-flop counter having a scale of 128, this is the same counter as used in dual channel; however, the most significant stage has been bypassed. This counter is stepped by each 18/15 counter-1 pulse which corresponds to the start of search time for each G/A-TD burst period. The 18/15 counter required 180 ms to complete one cycle of operation.

The 7-bit burst count produced is fed to the computer section of the output control element and to the G/A-TD compare circuitry. The output levels from the 1 side of the flip-flops in the burst time counter are sent to the computer section, whereas both the 1 and 0 sides of these same flip-flops are sent to the computer circuit. A reset-flip-flop signal from the output control element is supplied to reset the burst counter after shutdown or test operations.

c. Burst Number Comparison

The G/A-TD compare circuit (Figure 3-77) is used to determine which words in a given burst period are to be accepted from the OB fields. The burst number of each G/A-TD output word is fed into the G/A-TD compare circuit where it is then

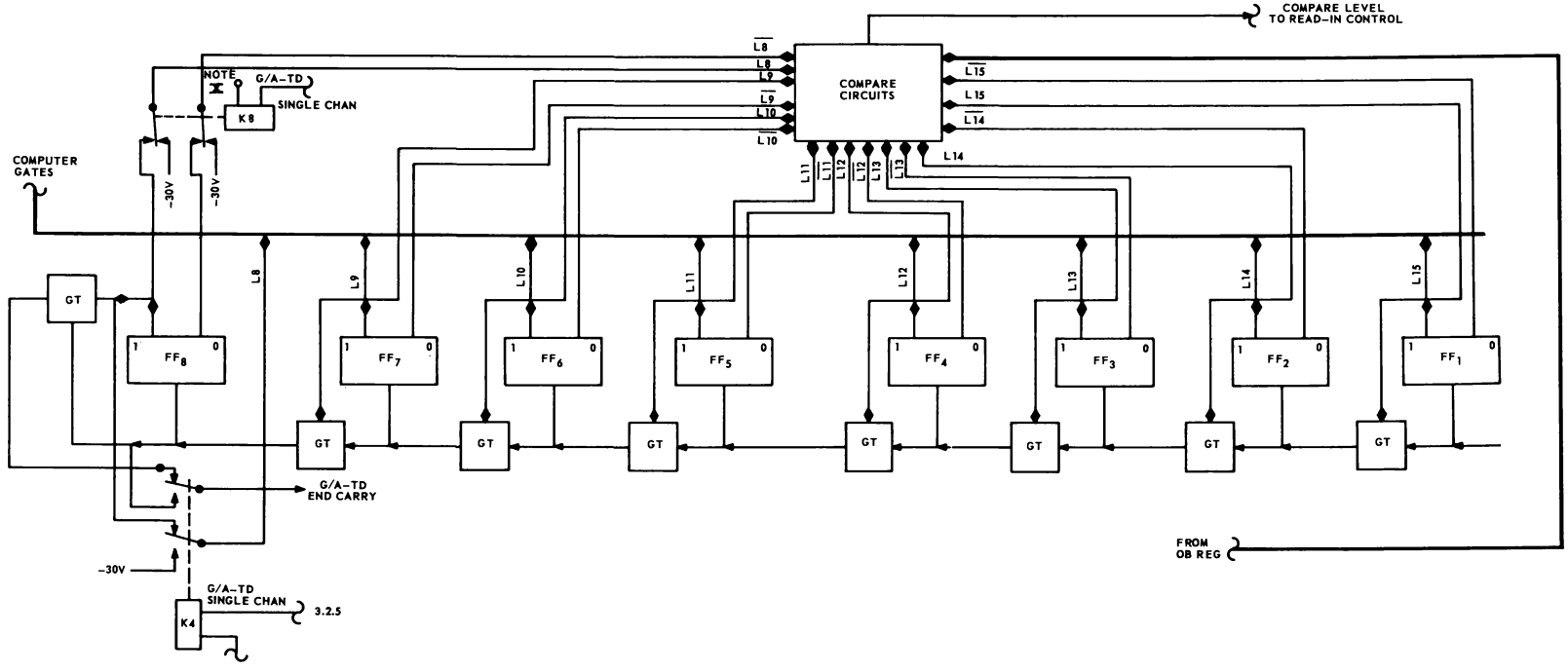


Figure 3-75. G/A-TD Burst Counter

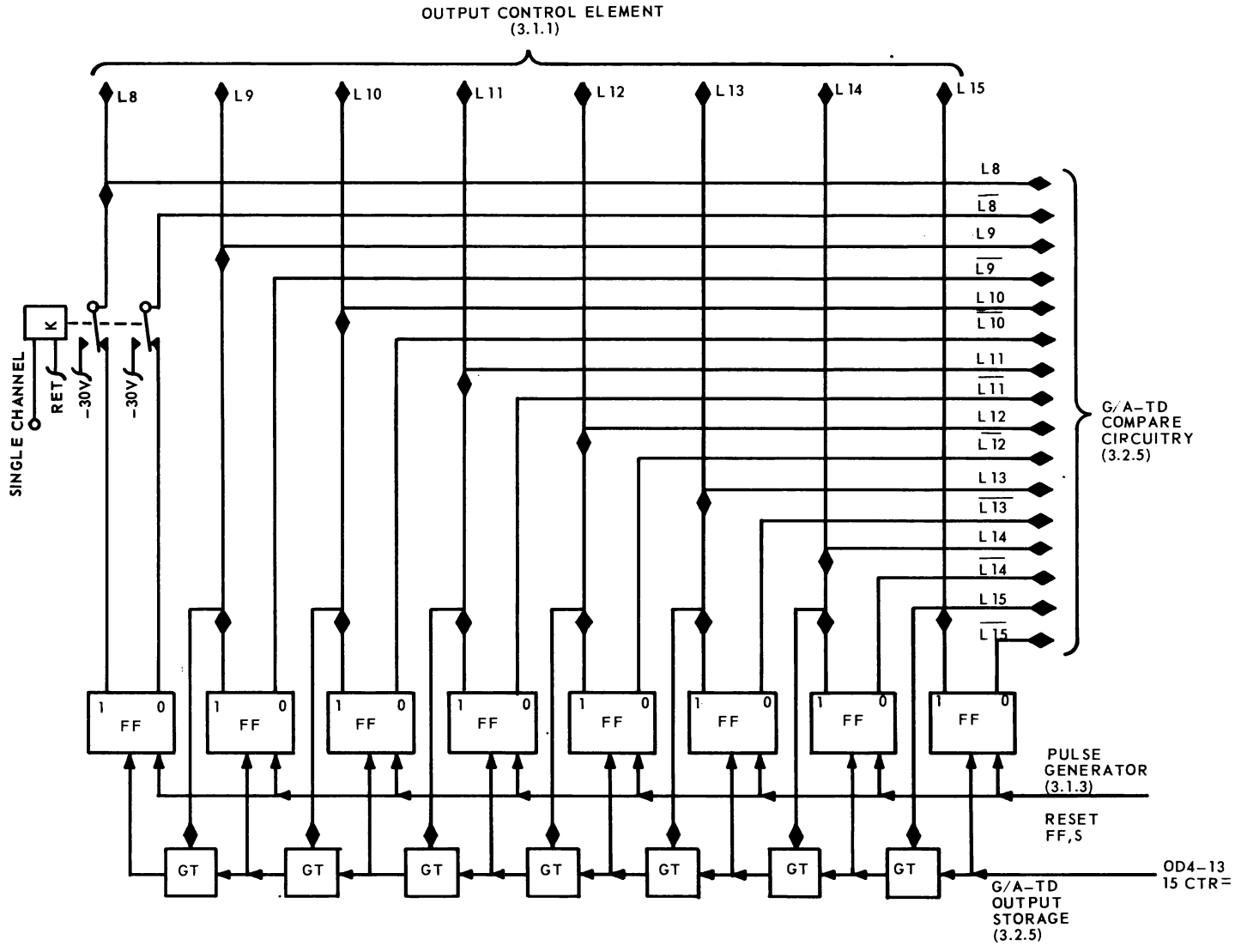


Figure 3-76. G/A-TD Burst Counter (3.1.2), Simplified Logic Diagram

examined to ascertain whether it is equal to the contents of the G/A-TD burst time counter. If the G/A-TD compare circuit finds that the counts are equal, it generates a G/A-TD compare signal. Conversely, if the burst counts are found to be unequal, a no-compare signal is generated.

The G/A-TD compare circuit comprises 16 2-way AND circuits, five 4-way OR circuits, and one inverter. Each AND circuit is fed a bit from the burst number supplied by the Central Computer and a bit from the G/A-TD counter. During single channel operation, the two AND circuits associated with L8, $\overline{L8}$ bit are tied to -30v and are not compared. Although these two bits are numerically equal, they represent opposite states; that is, while one bit represents its complement, which is 0. Under these conditions, an AND circuit produces a signal only when corresponding bits of the assigned burst number and the current count of the burst counter are unequal. When they are equal, all 14 2-way AND circuits used in single channel produce a -30v output level. The AND circuits are connected to four OR circuits, which in turn are connected to a single OR circuit. Therefore, the -30v level emanating from the AND circuits is passed by the OR circuits and applied to the inverter. The output of the inverter is a +10v level which is then sent to the output control element as a G/A-TD compare level.

Should the assigned burst number and the burst time count be unequal, one or more of the AND circuits will produce a +10v level which is passed by the OR circuits (Figure 3-77) and applied to the inverter. The output of the inverter is a -30v level which is then sent to the output control element as a G/A-TD no-compare level.

8. Conversion

a. General

Information leaving the G/A-TD OSR 1 is sent to the conversion circuits prior to being fed through the switching circuits to the telephone transmission equipment. The conversion circuits convert the G/A-TD data and sync information, which consists of standard 0.1-usec pulses, to a series of synchronized, gated, 1,300 cps sine waves. The information is modified in this manner to make it compatible with telephone company equipment requirements.

b. Conversion Equipment

All of the conversion circuits are contained in the G/A-TD conversion equipment. This equipment is comprised of two identical channels, each capable of transmitting G/A-TD data, however only data channel 2 and phone line No. 1 is used. Each channel contains a data conversion channel, an identical sync conversion channel, and a timing channel. The data and sync conversion channels perform the required conversion on their respective information inputs. The timing channel serves to match the timing signal, a 1,300 cps sine wave, to the telephone equipment, but does not modify its waveshape. The detailed operation data and sync channel 2 is presented in the following paragraphs.

c. Data Conversion Channel

Ground-to-air time division data is either a standard pulse occurring at OD 3-13 time to represent a 1 bit or the absence of this pulse at this time to represent

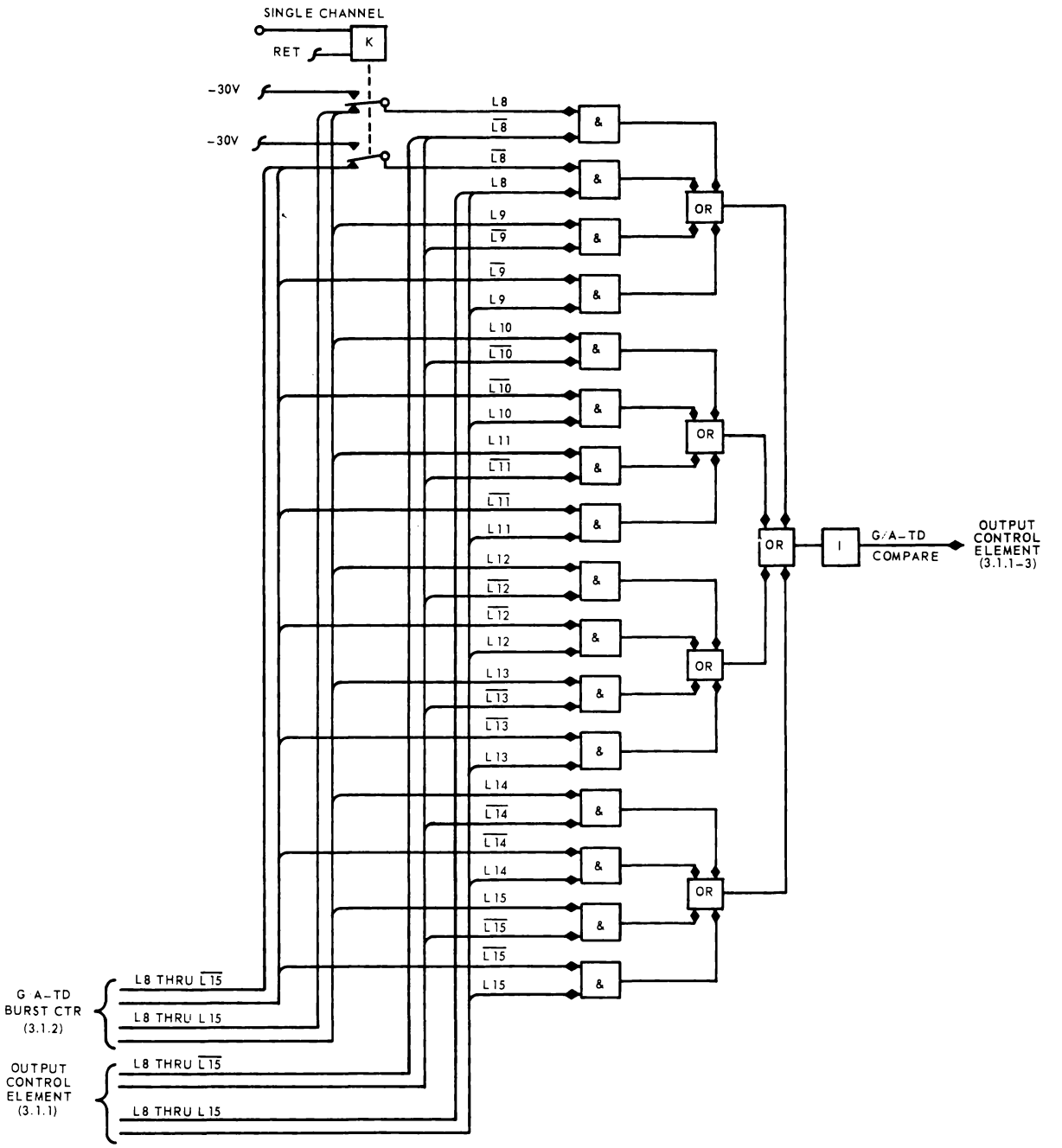


Figure 3-77. G/A-TD Compare (3.1.2), Simplified Logic Diagram

a 0 bit. This data is applied to the G/A-TD output data channel 2 flip-flop. This flip-flop is set by G/A-TD data pulses and cleared by the following OD 2-13 timing pulses (Figure 3-78).

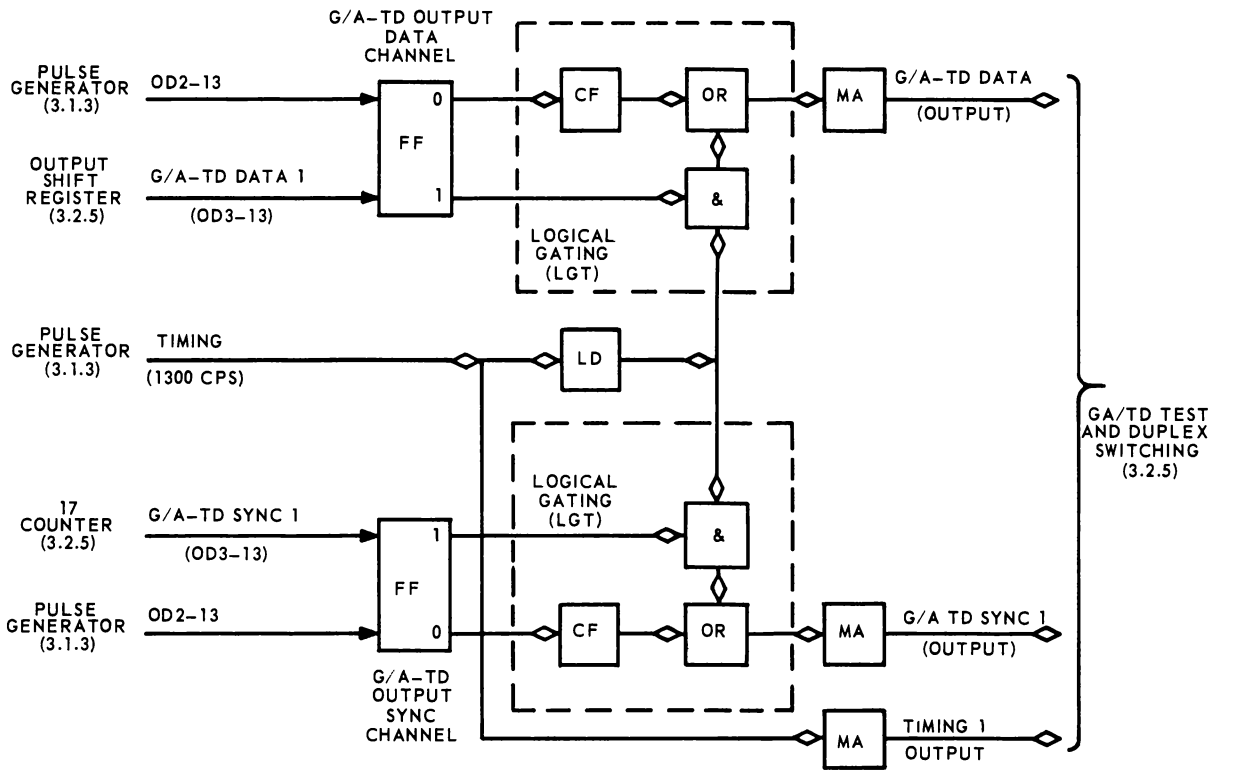


Figure 3-78. G/A-TD Conversion, Message 1 (3.2.5), Simplified Logic Diagram

The G/A-TD output data channel 2 flip-flop supplies an input level to the 2-way AND circuit component of a logical gating (LGT) circuit. The LGT is comprised of this AND circuit plus a cathode follower and an OR circuit. The other input to the 2-way AND circuit is the 1,300 cps timing signal. The output of the AND circuit is either the timing signal or a -30v level, depending on whether the flip-flop is set or clear, respectively.

The flip-flop also supplies an input level to the OR driver cathode follower component of the LGT circuit. This cathode follower generates a clamped ground or a -30v output level, depending on whether the flip-flop is clear or set, respectively.

The AND circuit and cathode follower outputs constitute the inputs to the OR circuit component of the LGT circuit. The output of this OR circuit is either the 1,300 cps timing signal or a ground level, depending on whether the flip-flop is set or clear, respectively. This output is sent to the telephone equipment via the MA circuit.

When the flip-flop is set by receipt of a 1 bit (i.e., a standard pulse occurring at OD 3-13 time), the data conversion channel sends a 1,300 cps sine wave to the telephone equipment. This sine wave continues until the flip-flop is cleared by the following OD 2-13 pulse. Since the OD 3-13 pulses recur at a 1,300 cps rate and the OD 2-13 pulse precedes the next OD 3-13 pulse by 2.5 usec, the interval between an OD 3-13 data pulse and the following OD 2-13 clear pulse will be 2.5 usec less than the period of the 1,300 cps timing signal. Therefore, for each 1 bit received by the flip-flop, slightly less than one cycle of the 1,300 cps timing signal will be sent to the telephone equipment. When the flip-flop remains clear due to the absence of a 1 bit (i.e., the absence of a standard pulse), a ground level will be sent to the telephone equipment.

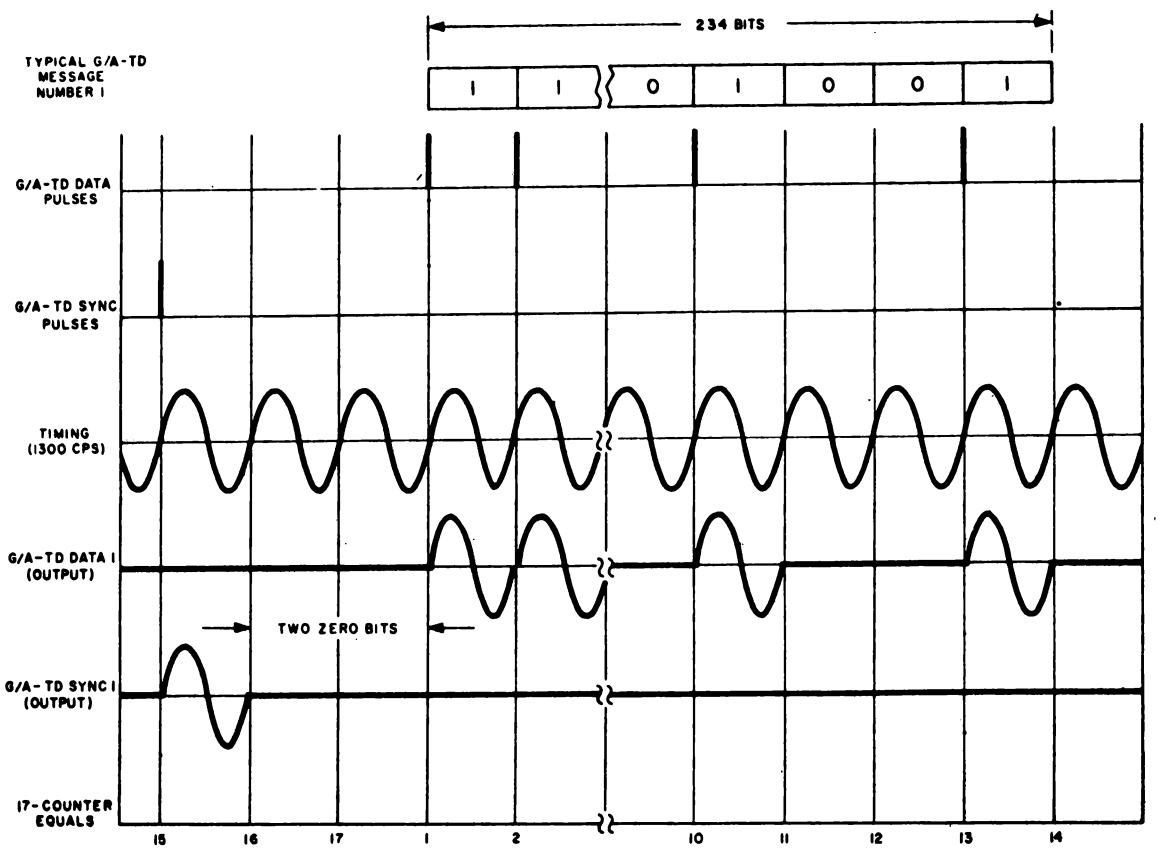


Figure 3-79. G/A-TD Conversion, Input and Output Signals

d. Sync Conversion Channel

The sync conversion channel shown in Figure 3-78 operates in a manner identical with the data conversion channel just described. For each sync pulse received, the sync conversion channel transmits slightly less than one cycle of the 1,300 cps timing signal to the telephone equipment. The sync pulse is applied to the conversion equipment at such a time that exactly two 0 bits occur on the data lines between the end of the output sync signal and the time that the first data bit is transmitted over the

data lines. (See Figure 3-79.) This timing which is necessary for decoding in the airborne receiver, is obtained by having an OD 3-13 sync pulse occur at 17-counter-15 time just prior to the readout portion each burst period. The sync pulse, therefore, precedes the data pulses, which are read out starting with the second 17-counter-equals-1 pulse, by two 17-counter shifts. In this manner, two 0 bits (the absence of two data pulses on the data lines at OD 3-13 time) occur between the receipt of the sync pulse and the start of the data pulses (00S00).

The data, sync, and timing inputs and outputs of channel 2 of the G/A-TD conversion equipment for a typical G/A-TD message are shown in Figure 3-79. The outputs of this channel are fed to the switching circuits and from there are sent out to the telephone equipment over phone line 1. No data is sent over phone line 2 in the single channel mode.

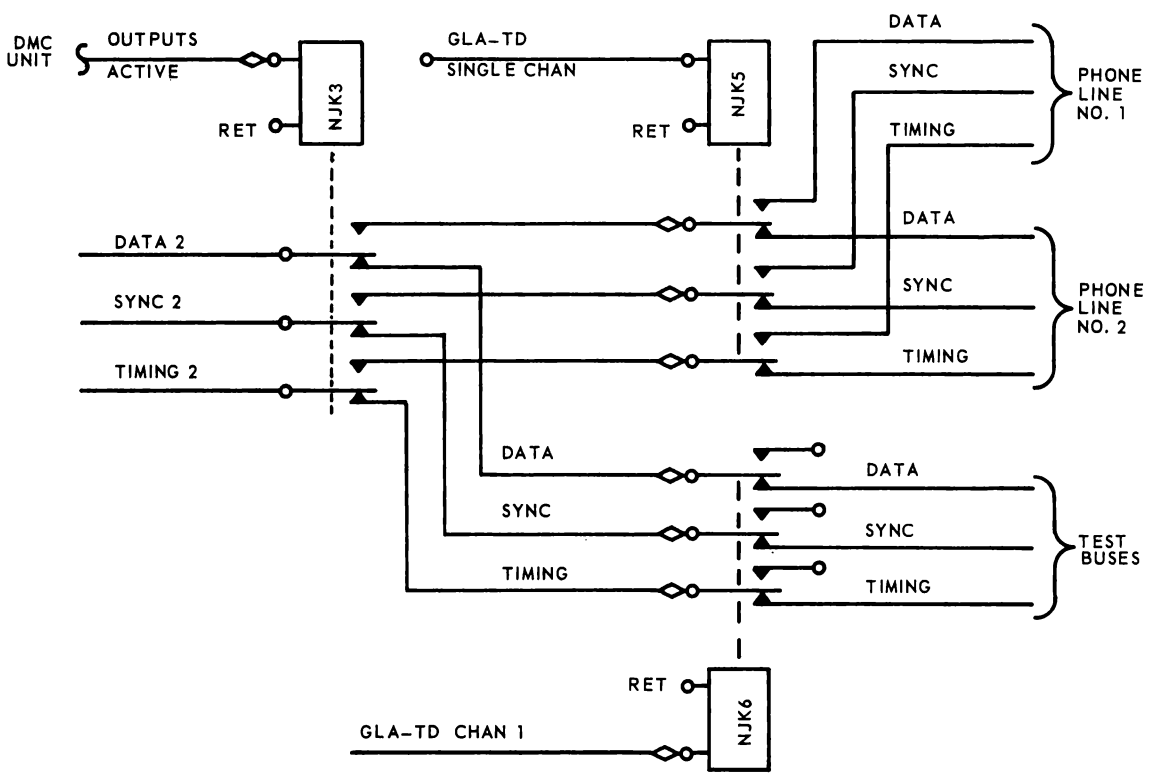


Figure 3-80. G/A-TD Test and Duplex Switching, Message 1 (3.2.5)

9. Switching

The G/A-TD test and duplex switching circuits control the output of the Output System of each computer. The switching circuits contain relays which provide for the switching of each G/A-TD message. However, the relay circuits for each message are identical. For this reason, Figure 3-80 shows a simplified diagram of the G/A-TD test and duplex switching circuits for only one G/A message.

The relays provided by the G/A-TD test and duplex switching circuits are controlled so that only the Output System of the active computer is presented to the telephone line terminal equipment. Relays are also provided to enable the Output System on standby status to be switched to the LRI test busses through pattern generators. These relays are operated during test operations only.

It is of particular importance to notice that information from OSR 1 is fed to the parity check 2 circuitry and G/A-TD Output Data Channel 2. However, when in the single channel mode of operation, relay 33NJK5 switches the information from phone line 2 to phone line 1. No data is sent out over phone line 2, nor are timing or sync transmitted over phone line 2 during single channel operation.

SUMMARY QUESTIONS

1. The G/A-TD, single channel, burst period is _____ milliseconds.

2. The G/A-TD, single channel, burst time counter is stepped at _____.

3. Not-search for G/A-TD, single channel, is from ____ to ____ and lasts for a total of _____ milliseconds.

4. How many auto parity BB will be transmitted per incompleted-message in G/A-TD, single channel?

5. The G/A-TD single channel BTC consists of _____ bits which are compared with the _____.

6. At what time do we check parity in respect to the 18 counter?

7. The single channel sync control FF is set for _____ milliseconds, _____ times in each burst period.

8. What is the time between 18/15-9 to 18/15-10?

9. What is the function of relay 33NJK5? (Logic 3.2.5 (3D))

10. Logic 3.2.5, 33EJG77 passes no pulses. How long are the effected G/A-TD single channel burst periods?

11. Logic 3.2.5, 33DS GT 2 is nonconductive. What would be the effect on an incomplete message?

12. Logic 3.2.5 33DPG8 is open. What alarms will be generated and what will be the general effect upon the message?

13. 33GW GT 4 Logic 3.2.5 is nonconductive. With twelve words read into the array, how many messages will be readout? Why?

CHAPTER 4. TEST EQUIPMENT SECTION

The output test equipment section is incorporated in the output control element of the Output System for the purpose of testing circuit functions and the logical operation of the Output System. The test equipment consists of switches, relays, and logical circuits. Also, certain of the neons and indicator lamps of the output alarm section operate with the output test equipment section. The various switches, neons, and lamps are located on the Output System test panel, which is mounted on the back of unit 42. (See Figure 4-1.)

Two basic types of tests are provided by the test equipment: the unit loop test and the computer loop test. Each loop test involves the feedback of test information to its origin, where a comparison is made to ascertain whether the test information was correctly transmitted. The unit loop test is performed manually by means of switches, whereas, the computer loop test is programmed and is therefore performed automatically. The unit loop test checks the operation of the various individual sections of the Output System while the system is isolated from the remainder of the Combat Direction Central.

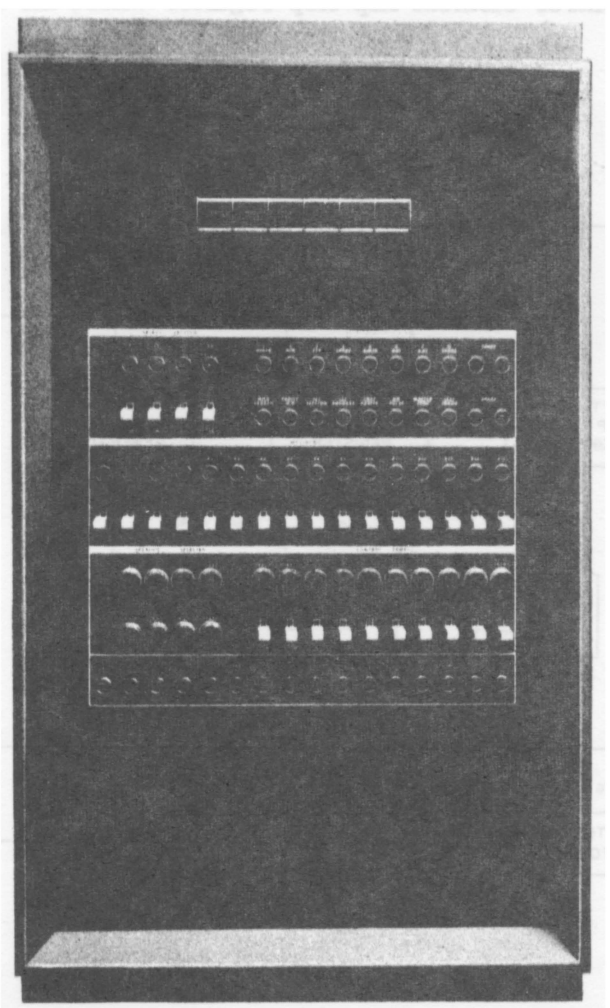


Figure 4-1. Test Control Panel, Unit 42

The computer loop test provides a means of checking the Output System in conjunction with a large portion of the Combat Direction Central.

Unit Loop Test (Figure 4-2)

1. General

In the unit loop test, the Output System is isolated from the Drum System, and a test word is then inserted manually by means of switches. The test word is processed in the normal manner by the output control element. If the conditions for its acceptance have been fulfilled (parity OK, burst number compares, no illegal addresses, and search time up), the word is transferred in the normal manner to the selected storage section in the output storage element. The word is then processed through this element. For the G/G, and G/A-TD storage sections, the output data (right drum word) is looped back into the output control element flip-flop register where the word was originally entered.

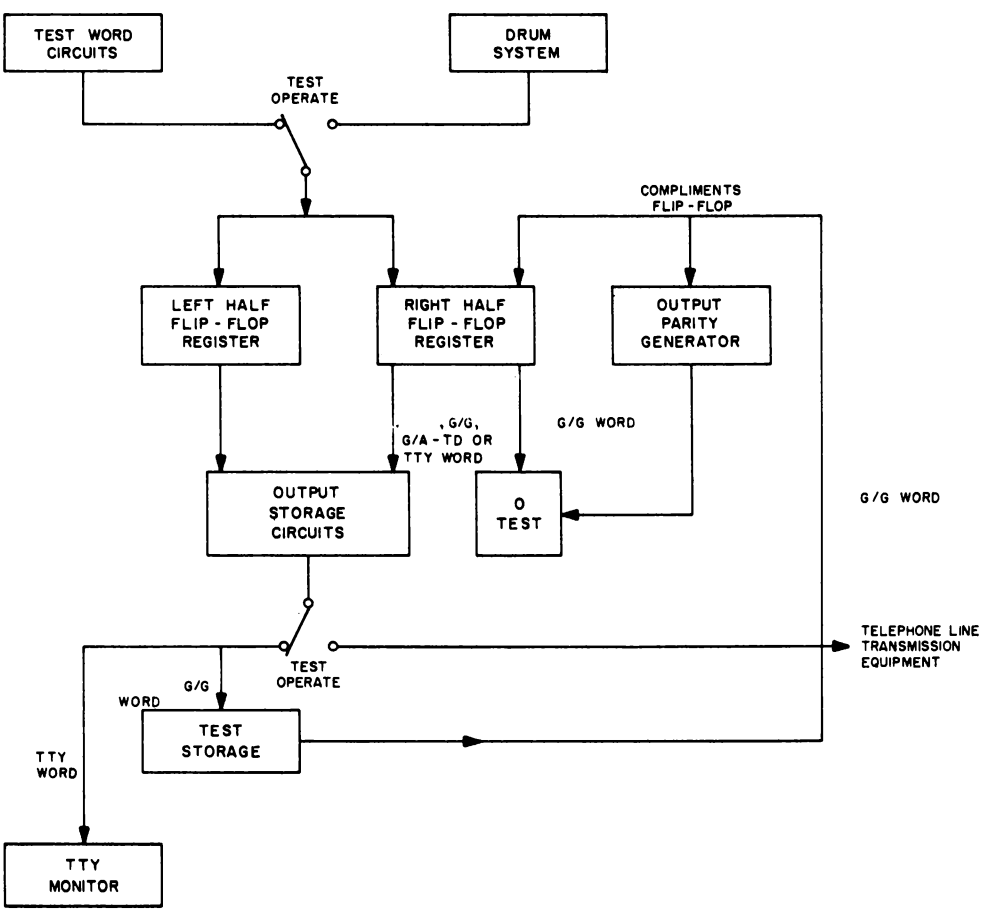


Figure 4-2. Unit Loop Test Data Flow, Block Diagram

If the transfer of the word was successful, the flip-flop register will be cleared. If the transfer was unsuccessful, one or more of the output flip-flop register neons will be illuminated. (See Figure 4-2.)

Besides this visual representation, the test equipment section indicates an error in one of several other ways described in 2.m.

For the TTY storage section, the output word is recorded on a TTY monitor. This data is then visually compared with the test contents of the flip-flop register to determine whether an error has occurred.

The unit loop test procedure may be divided into three basic circuit groupings: unit loop control, unit loop storage, and specific unit loop tests. The unit loop control circuits control the general flow of the test word through the output control element and output storage element and provide the processing operations for detecting an error. The unit loop storage circuits provide for the storage of the test word in the test equipment section. The unit loop test circuits control the specific test operations in each of the storage sections of the output storage element during testing operations.

2. Unit Loop Control, Error Detection

The general process of error detection involves the manual setting in of a test word in the flip-flop registers and the processing of this word to determine whether any errors occur. The test word is processed through the output control element in the normal manner and transferred to the output storage section. It is processed by the particular output storage section as described in 4. From there, a G/G, or G/A-TD word goes to the unit loop control circuits. A TTY word, on the other hand, is sent not to the unit loop control circuits but to a TTY monitor.

a. Unit Loop Test Switching

The operation of the Output System during testing is controlled by relays, which in turn are controlled by switches. These switches are located on the panel on the test door on the back of the output control unit.

Any kind of a test on the Output System disables it, thereby preventing the associated computer from being used to solve the Air Defense Problem. Therefore, an interlock (controlled at the maintenance console) is necessary to prevent inadvertently starting a test during the processing of an air defense problem. This interlock is accomplished by switching the relay voltage supply for the test equipment section at the maintenance console. Thus, the OPERATE-TEST switch on the maintenance console sends a computer test signal to the unit-loop-on-test circuit of the unit loop control. (See Figure 4-3.) This signal controls the relay voltage supply for the output test equipment section and is sent via the computer loop control circuits since a computer loop test takes precedence over a unit loop test. Hence, control over whether a unit loop test can take place depends upon whether a computer loop test is in progress.

A unit test pushbutton (S6, Figure 4-3) in the test equipment section causes a holding relay to close, which controls the output test relay voltage (the output-on-test

signal) to the test circuits. The end unit test pushbuttons (S1) breaks the voltage to the holding relay at the end of the test operation.

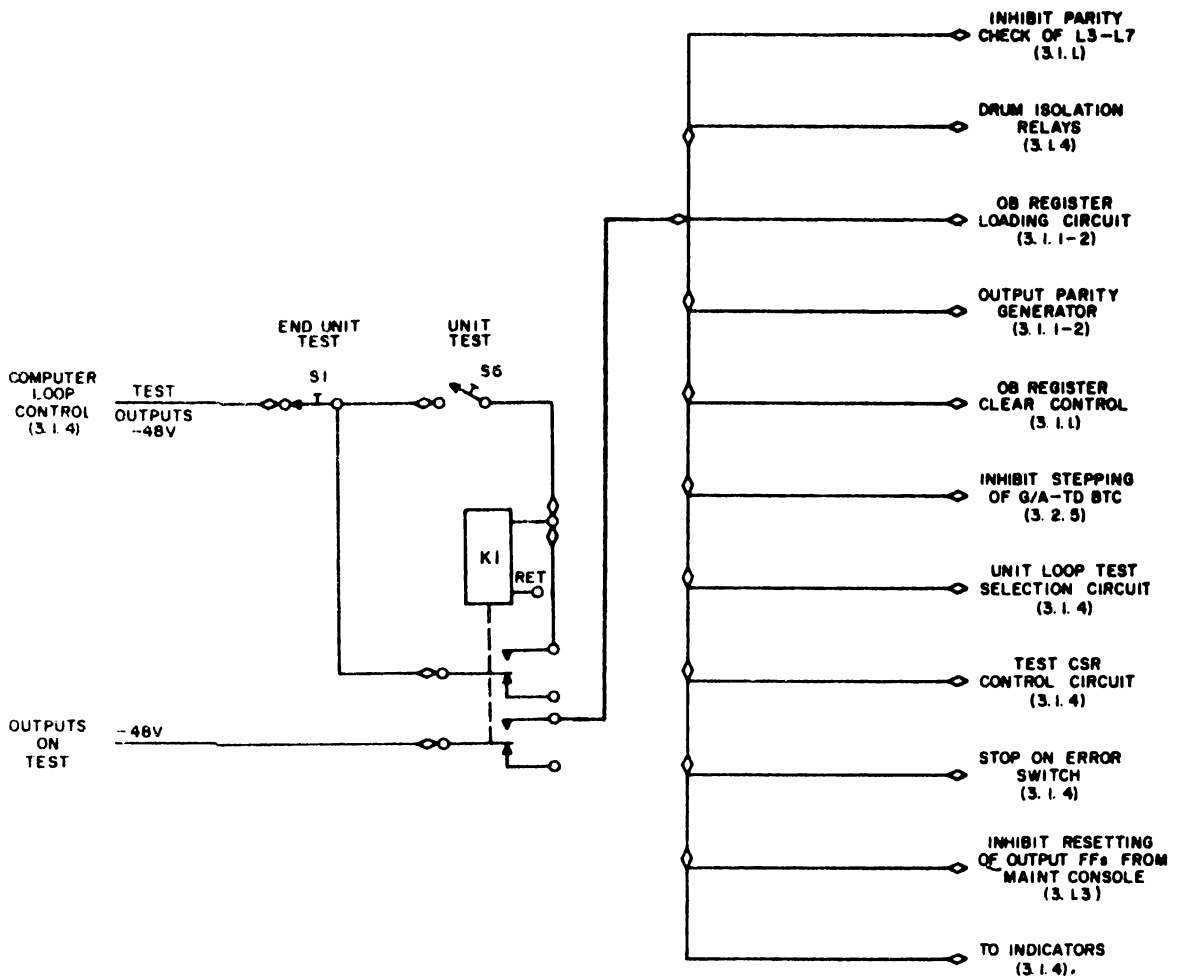


Figure 4-3. Unit-Loop-On-Test Control Circuit (3.1.4), Simplified Logic Diagram

b. Drum Isolation and Test, Bit Circuits

To set in a test word, the flip-flop register of the output control element must be isolated from the Drum System. After this is done, the test word can be set into the flip-flop register.

Eight relays, controlled by the -48v unit loop test relay voltage, are used to isolate the OB (output buffer) register from the Drum System. Five of these relays, as shown in Figure 4-4, isolate 20 of the 33 bit lines from the Drum System. The remaining 13 bit lines and the associated isolation relays are not shown because they have no corresponding bit switches. The reason for this is explained in the following paragraphs.

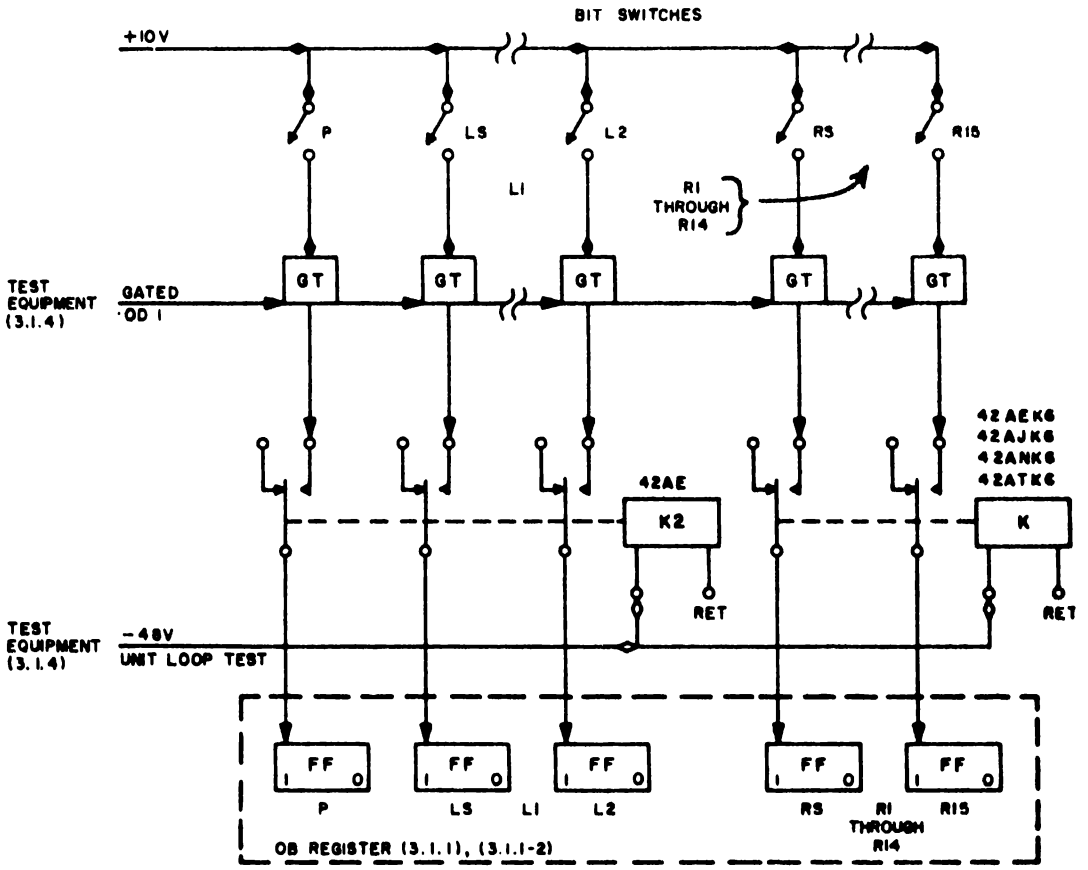


Figure 4-4. Drum Isolation and Test Bit Circuit (3.1.4), Simplified Logic Diagram

The test word generator of the output test equipment section provides a standard test word pulse equivalent to a 1 bit to each of 20 gates. Each gate is connected to a read-in test word switch corresponding to 20 of 33 bits which make up a word. The bit switches used in a unit loop test are the P bit, LS through L2, and Rs through R15.

When a switch is closed, a +10v level conditions the corresponding gate which passes the test-word pulse. This sets the corresponding flip-flop in the flip-flop register. It follows, of course, that read-in test switches which are not activated will have no effect on their respective flip-flops; thus the latter will remain cleared (0 side up).

When setting in a test word for G/G, or G/A-TD, the right drum word (bits RS through R15) may be set to any desired combination of 1's and 0's. For TTY, the restrictions explained in 4.d. must be considered.

The burst number, bits L8 through L15, must be all 0's since the stepping pulses to the burst counters in the output control element are inhibited. Since bits L8

through L15 must always be 0's, their corresponding bit switches have been removed from the unit test door. The desired register address in the array of the selected section, designated bits L3 through L7, does not require the use of bit switches during a unit loop test because the register address portion of the OB register is automatically stepped during loop testing.

However, some provision is made to step the register addresses manually. The desired section address, designated bits LS through L2, is set according to the section address code. Care must be taken not to set in an unassigned section. The parity bit, P, must reflect a manual parity count of the 19 other bits (L3 through L7 are not parity-checks during a unit loop test) so as to produce odd parity for all 20 bits.

c. Inhibit Resetting of Right Drum Word

Under normal operation, the parity drivers of the output control element clear the flip-flop register approximately 7.9 usec after the word is entered. During test operations, however, the right drum word should remain in the flip-flop register until it is complemented by the completely processed, looped-back word for G/G, and G/A-TD tests, or visually compared with the TTY monitor for TTY tests.

The clearing of right drum word registers is prevented whenever the Output System is placed in unit loop test.

As shown in Figure 4-3, the -48v relay voltage level is passed by unit test relay K1 to the relay in the parity register and drivers (Figure 2-8) which controls the application of the clear pulse. The opening of this latter relay prevents the clear pulse from being passed to the right drum word flip-flops. Since only the message portion of the drum word (right drum word) and the output parity bit arrive at the output of the output storage element, only this (the right) portion of the drum word and the output parity bit are looped back to the flip-flop register for comparison purposes.

Since the address portion of the left-half drum word (L3-L7) is automatically or manually stepped during read-in, the clear pulse to these flip-flops is delayed until all legal register addresses contain the test word (Figure 2-9).

d. Clearing Alarms and Resetting Flip-Flops

Before the test operation is begun, all alarms and flip-flops in the Output System should be cleared by depressing the CLEAR ALARMS and RESET FLIP-FLOPS switches (S5 and S4). This action grounds the pulse generators in the pulse distributor circuits of the output computer section. Clear pulses now pass to the appropriate circuits. (See Figure 2-41.)

e. Unit Loop Test Selection Circuit

Selection of the various sections for unit loop testing is accomplished by means of three relays, depicted in Figure 4-5. As shown in the figure, these relays are controlled by select section switches LS, L1, and L2, which are located on the unit test door.

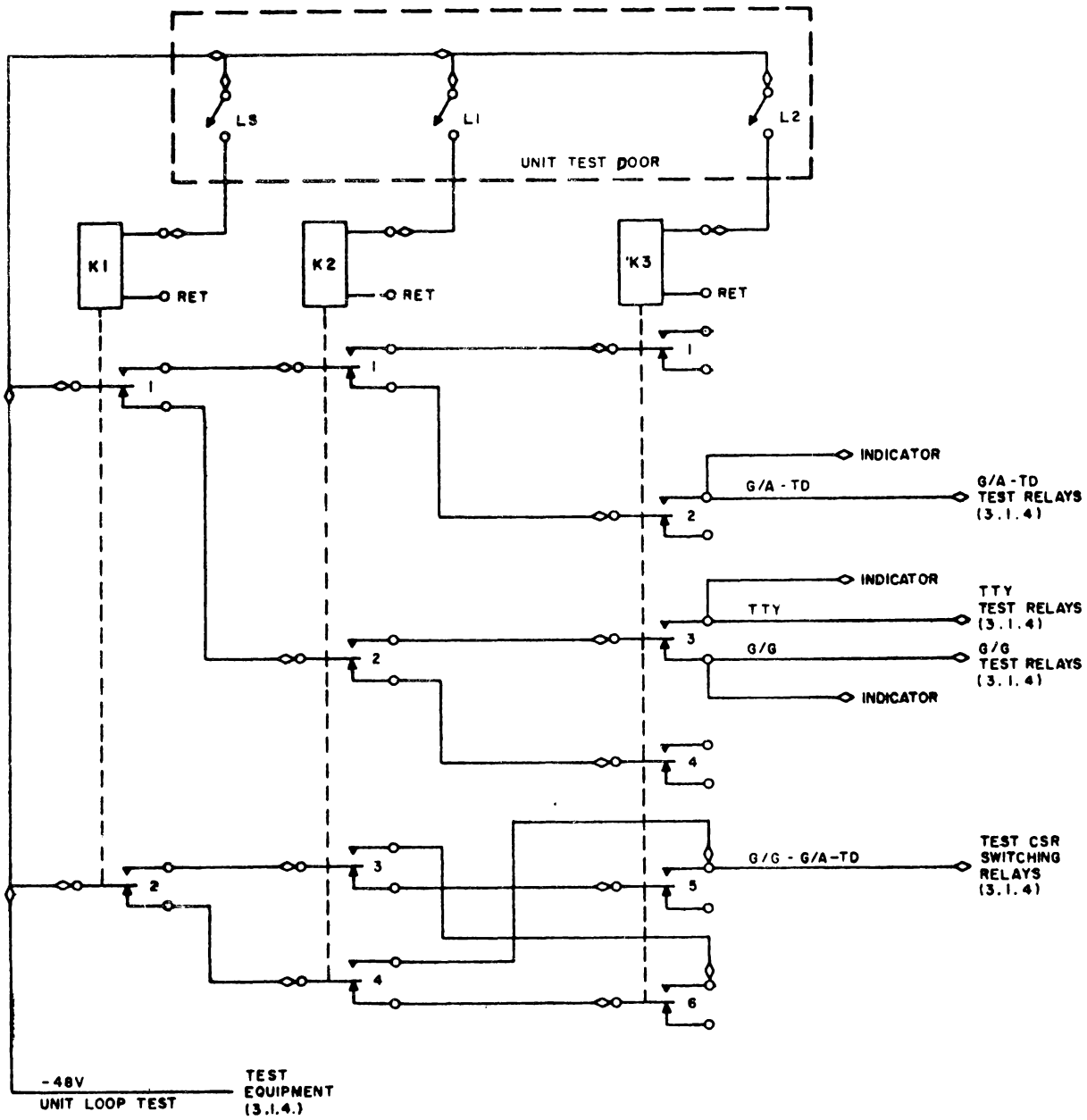


Figure 4-5. Unit Loop Test Selection Circuit (3.1.4)

When it is desired to select a particular section for unit loop test purposes (say, the G/G section, section 2), then select section switch L1 must be operated. In addition to inserting the section number (010) in the OB register, this switch, when operated to the closed position, allows -48v to be applied to K2, energizing it.

It can also be seen from the figure (Figure 4-5) that the -48v relay voltage is also routed through the normally closed contacts (K1-1NC, K1-2NC) of de-energized

relay K-1 and routed through the normally open contacts (K2-2NO, K2-4NO) to the normally closed contacts (K3-5NC, K3-3NC). The -48v relay voltage is applied to relay contacts (K3-3NC) to light an indicator lamp and energize all the G/G unit test relays. This -48v relay voltage is also routed through relay contacts (K3-5NC) to energize the test CSR switching relay. The visual indication provided by the indicator light serves to indicate which section is selected for unit loop test and also serves as an additional check on the operations of the associated relays.

During a unit loop test operation of the Output System, only one section will be processing test data information at one time; thus no interaction between relays is possible. The unit loop test switching procedure employed by the other sections of the Output System is identical with that described for the G/G storage section; therefore, their operations need not be presented here.

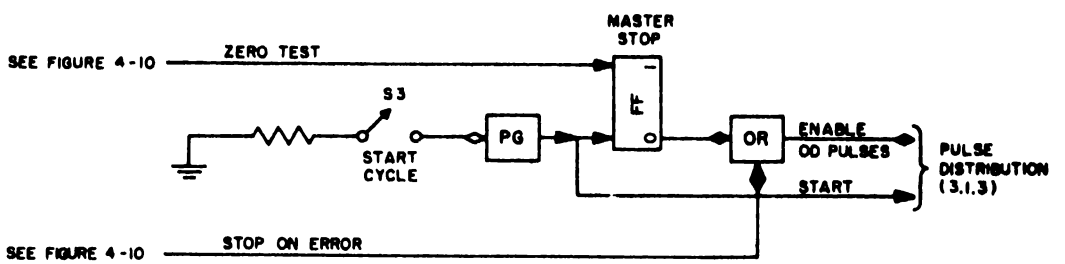


Figure 4-6. Test Start Control (3.1.4), Simplified Logic Diagram

f. Test Start Control (Figure 4-6)

Before a unit loop test is started, the previous basic switch settings must be made. Then the specific switch settings described in 4.a. must be made, depending upon the storage section (G/G, G/A-TD or TTY) selected. Also, the method of error detection is selected. If the STOP ON ERROR switch is engaged, the test should be started by depressing the START CYCLE pushbutton, S3. As shown in Figure 4-6, this action grounds the pulse generator, which produces a pulse to clear the master stop flip-flop. This latter flip-flop produces an enable OD level, which then causes the various OD pulses to be distributed by the output control section. This action sets the circuits into operation. Also, the start pulse is sent to the 1,300 pps generator to clear its flip-flop at the start of the test.

As described in 2.m., if the STOP ON ERROR switch is not engaged, the OR circuit following the master stop flip-flop usually FF clear has a +10v level on it from the clear side of the reset and prime FF. With the reset and prime, the enable-OD-signal level is always present and the Output System is continuously cycling. Under this condition, the test is always in progress, even while the test word is being entered. Therefore, the START CYCLE button has no significance.

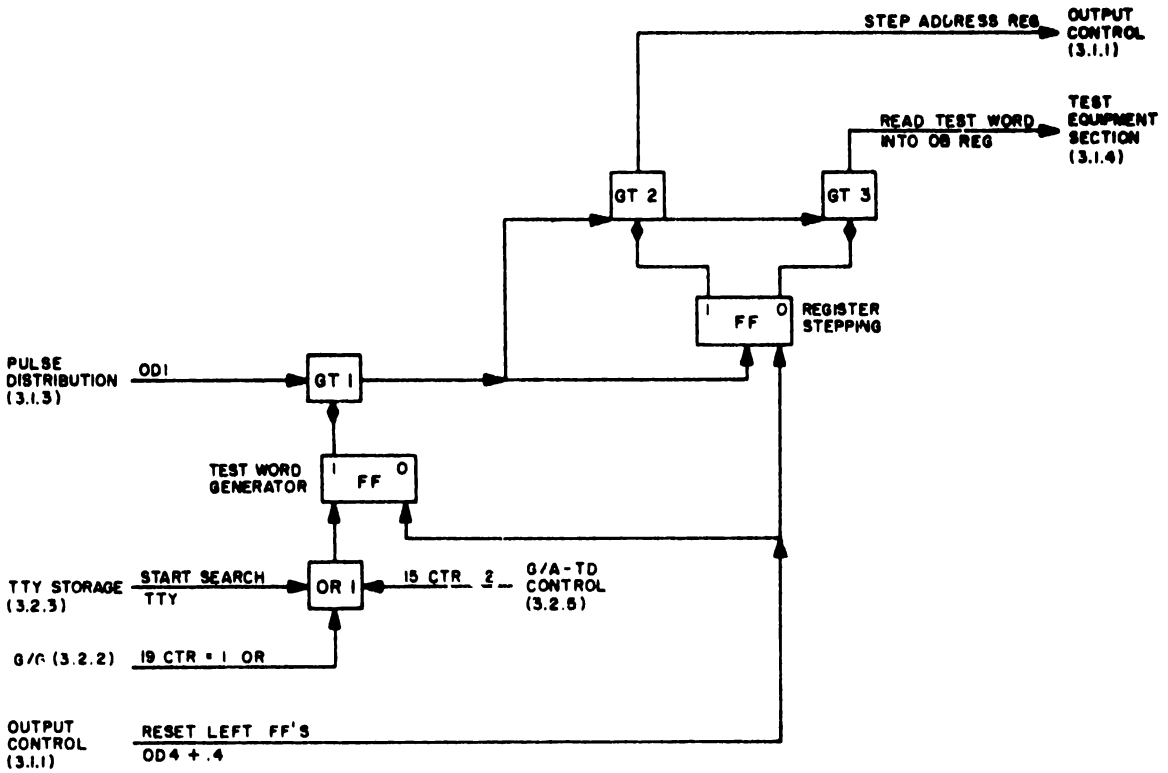


Figure 4-7. Test Word Generator and Address Register Stepping Simplified Logic Diagram

g. Test Word Read-In (Figure 4-7)

To unit-loop-test the individual storage sections in the Output System, a test word, as selected by the bit switches located on the unit test door, is read into each individual address of a selected storage section in sequential fashion until all legal addresses have been read into.

The read-in operation of the test word into a specific core storage array is accomplished by stepping the address register until the test word is contained in each address. The stepping of the address is accomplished under the control of the test word generator and address register stepping flip-flops, shown in Figure 4-7.

As shown in Figure 4-7, various pulses generated from any one of the individual storage sections are used to set the test word generator flip-flop, except TD. When set, the flip-flop will generate a level to condition GT 1, which is strobed by OD 1 pulses. During a unit loop test, the gated OD 1 pulses strobe GT's 2 and 3, in addition to complementing the register stepping flip-flop which controls both the stepping of the register addresses and the read-in operation of the test word into the OB register. Gates 2 and 3 are conditioned by the outputs of the register stepping flip-flop. Initially, this

flip-flop is clear and is complemented by a gated OD 1 pulse to its set side; GT 3 thus is conditioned to pass the OD 1 pulse.

The latter is sent as a read-test-word pulse to the OB register. The test word is now inserted into register address 0. Succeeding OD 1 pulses strobe conditioned GT 1. This gated OD 1 pulse strobes GT's 2 and 3 while at the same time complementing the register stepping flip-flop to its clear side. Gate 2 is now conditioned to pass the same OD 1 pulse which is now used to step the register address to address 1. This action is repeated until all addresses in a particular storage section are made to contain the test word. When this occurs, the register stepping flip-flop is set in a status conditioning GT 2 to pass the following gated OD 1 pulse, thus stepping the address register to an illegal address count. When this occurs, a reset flip-flop pulse (OD 4 +0.4) is gated from the output control element to clear both the test word generator and the register stepping flip-flops, thus ending the read-in operation of the test word information by address into the core storage array of the selected storage section under test.

h. Single-Address Stepping

Provisions are made to incorporate an additional refinement or feature should an error be detected while processing the test word through a selected storage section into an array. In the event that an error is detected, an alternate method of reading in the test word is performed; i.e., each register address is stepped, one at a time, when the SELECT ADDRESS pushbutton (S2) is depressed. Figure 4-8 depicts the single address stepping circuit used to perform this function.

As shown in Figure 4-8, selection of test word read-in in the single-address mode is accomplished by closing single-address switch S1, thus energizing K1 and K2. Following this, SELECT ADDRESS pushbutton is depressed, causing a pulse to be generated through the closed contact points of K1 as a stepping pulse to step the register address portion of the OB register. Each time the SELECT ADDRESS pushbutton is depressed, the register address will be stepped to its succeeding count. Energized K2 will allow gated OD 3 pulses to set the unit test control flip-flop. The function of the latter is described in the following paragraphs.

i. Transfer of Word from Output Storage Section to Test Circuits CSR

The test data bits that are contained in all register addresses of the selected storage array are read out of the array into the output shift registers (OSR's) by columns containing either all 0's or all 1 bits. This, in effect, represents well over 200 data bits that would have to be read into the test core shift register (CSR). The test CSR is capable of handling a maximum of 17 data bits; hence, it can be seen that some provision must be made to reflect the composite of all data bits stored in the selected core storage array into the test CSR. This is accomplished by reading out each column of an array, simultaneously checking the odd or even count of each column as it is read out, and inserting the resultant count of each column into the test CSR. This function is accomplished by using the existing parity checking circuit shown in Figure 4-9 to determine the total odd or even count of test data bits as they are read out of the OSR's.

The resultant condition of the parity check circuit that is obtained after a column of test data bits is shifted out of the OSR's is subsequently fed to control circuits,

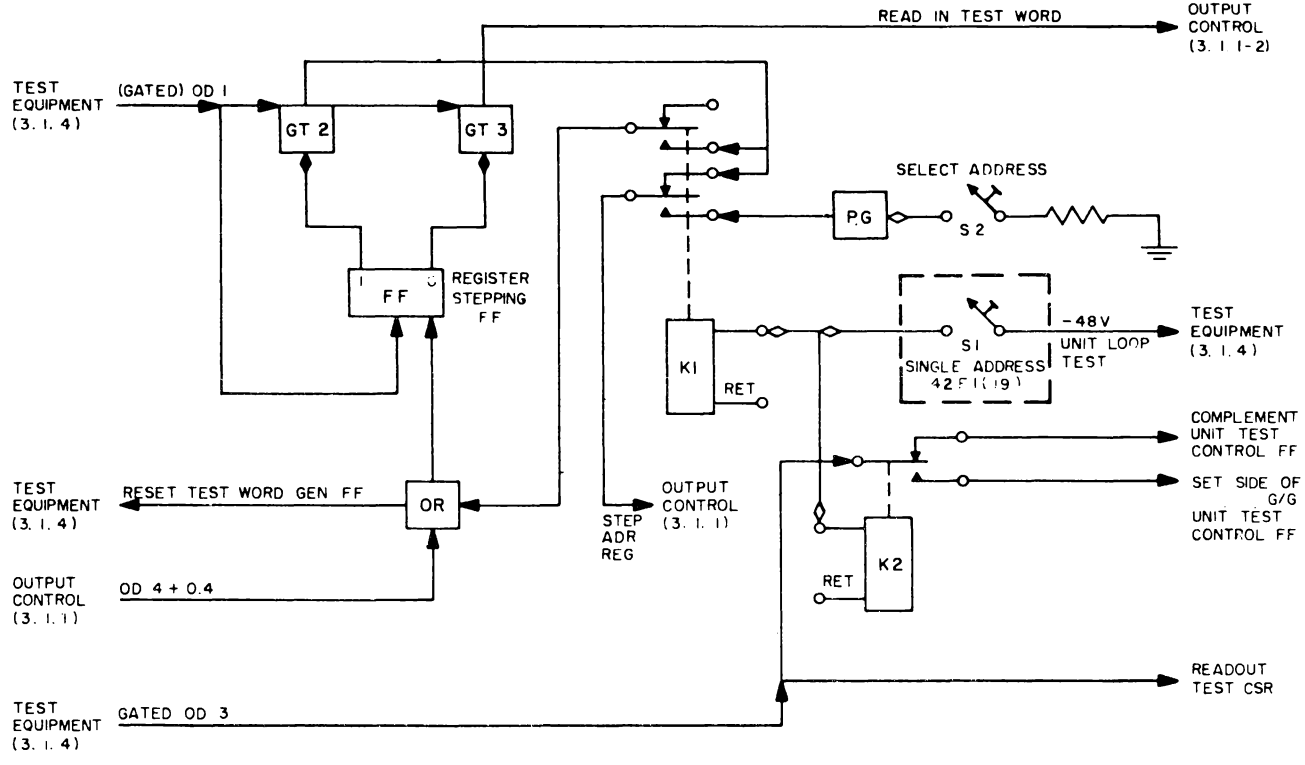


Figure 4-8. Single-Address Stepping Circuit (3.1.4), Simplified Logic Diagram

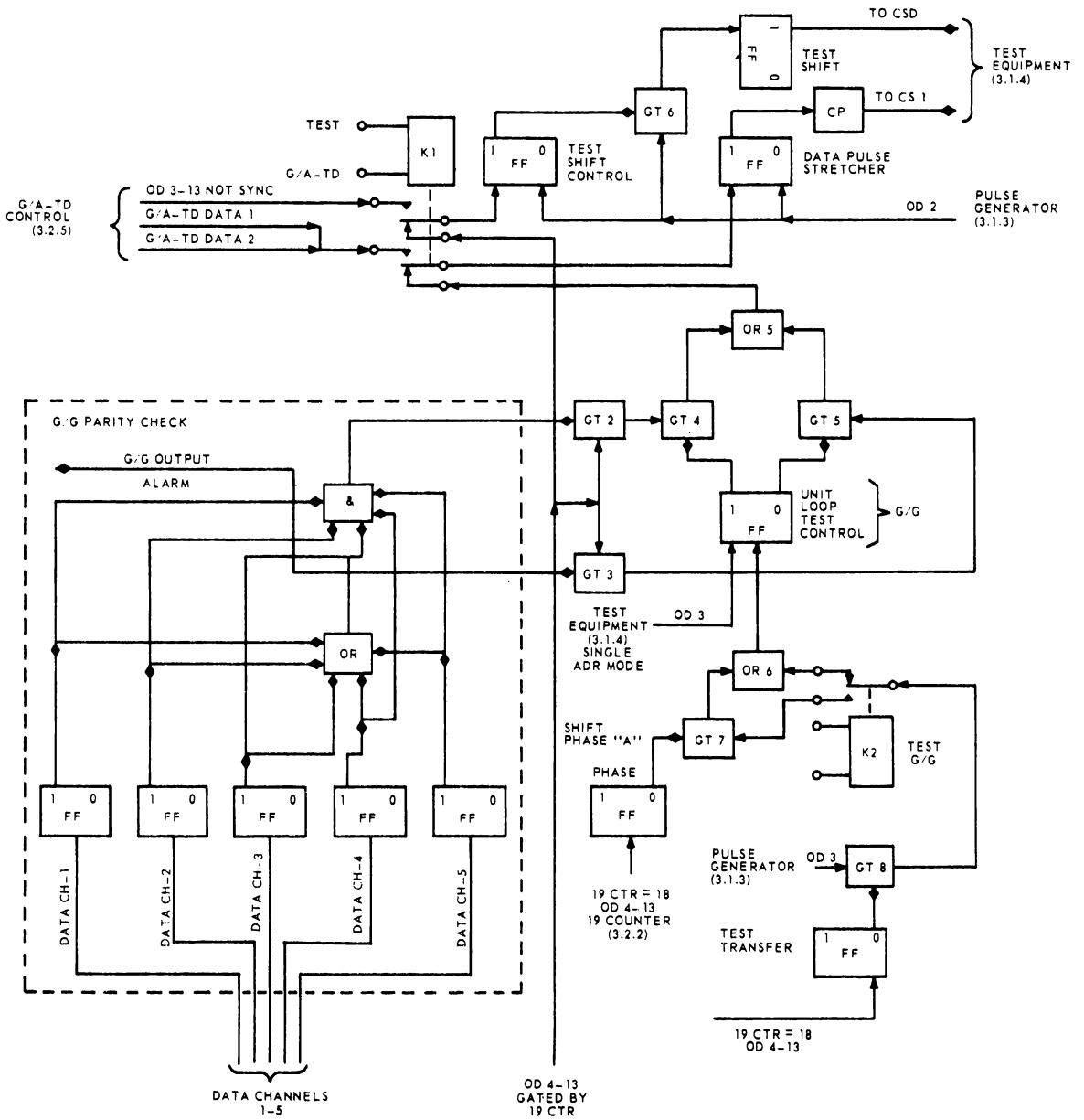


Figure 4-9. Test CSR Data-Bit Generator and Error Check Circuit (3.1.4) Simplified Logic Diagram

which determine whether a 1 bit is to be printed into the test CSR. The parity checking circuits and control circuitry are shown in Figure 4-9 and discussed in detail in the following paragraphs.

As seen from the figure, the test data read out of the OSR's is supplied to the complement lines of the parity checking flip-flops. Initially, these flip-flops are cleared and are complemented every time a 1 bit is read out of the OSR's. If the array column which was read out contained all 1 bits, then each parity checking flip-flop is complemented an odd number of times. For G/G, each parity checking flip-flop is complemented five times. Thus the parity checking flip-flops are in a set status at the end of readout of a single column of 1 bits from the OSR. However, in the case of G/A-TD, no output parity check is performed on the test word during a test transfer operation. The latter is discussed in detail in 2.1.

It must be noted from the figure that GT 1 will be conditionted to pass an output-parity-alarm pulse whether an error is present during the parity checking cycle or not and that, therefore, the alarm pulse is meaningless during this particular operation. If the parity count for a column of 1's as read out is odd, indicating no error, both the AND 1 and OR 2 circuits are conditioned, and their output levels are applied as conditioning levels to the OR 3 and OR 4 circuits, respectively. As a result, both GT's 2 and 3 are conditioned to pass OD 4-13 pulses, which strobe them. These pulses are generated at the completion of a column readout and are passed by GT's 2 and 3 to strobe GT's 4 and 5. The conditioning level for the latter gates is supplied by the G/G unit loop test control flip-flop. This flip-flop is complemented by gated OD 3 pulses at the end of an array "A" readout at 19-counter-19 time whenever the single address mode is not being used during a test. However, if the single-address mode is used for test, the OD 3 pulses are fed to the 1 side of the unit loop test control flip-flop via energized K2, shown in Figure 4-9.

When the single-address mode is not used during a unit loop test, the unit loop test control flip-flop is complemented, conditioning either GT 4 or GT 5. Hence, either gate can pass the gated OD 4-13 pulse, which strobes them. The data pulse stretcher flip-flop is then set via OR 5 and the normally closed contact points of K1. This relay (K1) is energized only when a unit loop test of the G/A-TD storage section is in progress.

When setting the data pulse stretcher flip-flop, a test data bit is primed into the test CSR as each individual array column is read out. As each test data bit is entered into the test CSR, it is shifted to succeeding cores until all bits have been entered into it. The individual bits are shifted under the control of the test shift control and test shift flip-flops.

At the end of an array column readout, an OD 4-13 pulse is generated and gated to strobe both GT's 2 and 3, in addition to setting the test shift control flip-flop via the normally closed contact points of K1. The latter, when set, generates a level to condition GT 6, which is normally strobed by an OD 2 pulse. Similarly, the OD 2 pulse is also used to clear both the data pulse stretcher and test shift control flip-flops. At this time, the OD 2 pulse will be passed by conditioned GT 6 to set the test shift flip-flop. Hence, each time that the latter flip-flop is set, shifting of the CSR will take place regardless of whether a bit has been primed into the test CSR.

To summarize the test word transfer operation during a unit loop test, a test word is read out of an array by columns and is parity-checked for an odd or even count. The resultant test data bit count is then primed into the test CSR under the control of the unit loop test control and data pulse stretcher flip-flops. Subsequently, the bit count is shifted to succeeding cores in the test CSR under the control of the test shift control and test shift flip-flops until all test data bits have been inserted into it. The test word data is then read out of the test CSR in parallel form to complement the right half-word of the OB register.

The aforementioned circuit analysis reflects normal test operation; however, this test cycle is repeated several times to determine whether the gain or loss of a bit has been incurred during a test word transfer. Detection of "grown" or "dropped" bits is discussed in the following paragraph.

j. Data Bit Generator Error Check

G/G storage sections should result, at the end of a parity check count, in having all five parity checking flip-flops come to rest on their 0 and 1 sides (both clear and both set). This then reflects a no-error operation.

However, some errors might be incurred during a test word transfer operation wherein some test data bits might be dropped (loss of a bit) or, on the other hand, grown (gain of a bit). The error detection circuit, shown in Figure 4-9, is used to detect errors that might be incurred during a test word transfer operation of the G/G storage section.

As stated in 2.i., the word transfer test cycle is repeated several times (a minimum of two test cycles) to allow for the detection of grown or dropped bits. That is to say, a complete array could conceivably contain a column of 0's and a column of 1's, a column of 0's and a column of 1's, etc.; hence, one complete test cycle is required to check the columns of 0's and another to check the columns of 1 bits.

Figure 4-9 depicts the error check circuit, which comprises the unit loop test control flip-flop and its associated gates, GT's 4 and 5. It can be seen from the figure that only GT 4 is strobed by OD 4-13 pulses when an error is present during a parity check test cycle. Also, GT 5 can be conditioned to pass OD 4-13 pulses only under the conditions that the unit loop control flip-flop is clear and that the OD 4-13 pulse is present at the gate. The latter condition can occur only if a parity check count, when performed on any one column of 1's is found to be correct.

It can be further stated that, when the unit loop control is at rest on its clear side for one array readout cycle, a dropped bit will be detected. Conversely, if the flip-flop is at rest on its set side for one array readout cycle, a growing bit will be detected. Assuming that a bit was dropped during a parity test cycle of a column of 1 bits and that the unit loop test control flip-flop is at rest on its clear side at this time, then GT 4 is strobed by a gated OD 4-13 pulse. Gate 4 would remain deconditioned and could not pass the pulse to set the data pulse stretcher flip-flop, and no bit is primed into the test CSR, indicating that a bit has been dropped.

On the other hand, had the unit loop control flip-flop been at rest on its set side at that time, then the dropped bit could not have been detected until the following test cycle because the test CSR would still be primed. Conversely, if a bit is grown during a parity check test cycle of a column of 0's, then GT 4 is strobed by a gated OD 4-13 pulse, assuming, however, that the unit loop test control flip-flop is at rest on its clear side at this time. Gate 4 remains deconditioned and cannot pass the pulse to set the data pulse stretcher flip-flop. No bit is primed into the test CSR, and the error remains undetected until the following test cycle.

In the ensuing test cycle, the unit loop control test flip-flop is complemented to its set side, GT 4 is conditioned, and, if the error is still present, the OD 4-13 pulse is passed by the conditioned gate to set the data pulse stretcher flip-flop, thus priming a bit into the test CSR indicating that a bit has been grown.

From the above explanation, it is evident that the sequence for determining whether a parity check for growing or dropping of bits is to be performed is largely dictated by the status of the loop test control flip-flop during any given test cycle. It is obvious that, when a column of 1 bits is being processed for test and no error is present in the column, that status of the unit loop control flip-flop, at any time, is relatively unimportant since both GT's 4 and 5 would be strobed by the OD 4-13 pulse and either could pass the pulse to set the data pulse stretcher flip-flop, inserting a bit into the test CSR.

k. Data Bit Generator Error Check (G/G)

Because the G/G storage section utilizes two core storage arrays (A and B), some additional refinements are used to select a particular array for test. Also, because both arrays are tested in sequential fashion, regardless of which array is first processed for test, the parity-checking sequence is reflected as the following (Figure 4-9):

(1) Array A is checked for dropped bits.

(2) Array B is checked for dropped bits.

(3) Array A is checked for grown bits.

(4) Array B is checked for grown bits.

Selection of a particular array for parity-checking purposes is dictated by the status of the flip-flop during a given cycle. This flip-flop is complemented by an OD 4-13 pulse at 19-counter-18 or at the end of a core array (A or B) readout. Complementing the flip-flop to its 0 side will select core array A to be processed for a parity check; likewise, complementing to its 1 side (set) selects core array B for test.

The parity-checking cycle for the G/G storage section begins at the end of a readout cycle at 19-counter-18 time, whereupon the test transfer flip-flop is set by an OD 4-13 pulse and the phase flip-flop is complemented to its clear side by this same pulse. Setting the latter flip-flop generates a shift phase A level to condition GT 7.

The test transfer flip-flop, having been set, generates a level to condition GT 8 to pass an OD 3 pulse. When a parity check test of the G/G storage section is effected, K2 will be energized to pass the OD 3 pulse via its closed contact points to strobe conditioned GT 7. The OD 3 pulse is then passed by conditioned GT 7 to complement the unit loop test control flip-flop via the OR 6 circuit.

Assuming that the latter flip-flop is complemented to its clear side at this time, it follows that core array A is now being parity-checked for dropping bits. At the conclusion of the array A parity check cycle, at 19-counter-18 time, the phase flip-flop is again complemented to its 1 side. However, GT 7 is now deconditioned, no pulse (OD 3) is passed to complement the unit loop test control flip-flop, and the flip-flop remains clear. As a result, core array B is now processed for a parity check of dropping bits, completing the first parity check cycle for both arrays A and B.

The above parity check test cycle is again repeated for detecting grown bits. When this occurs, the unit loop test control flip-flop will be complemented to its 1 side, whereupon it will remain in this state until both arrays have been parity-checked for grown bits.

l. G/A-TD Test Word Transfer

The test word transfer operation during a unit loop test of the G/A-TD storage section differs greatly from that described for the G/G storage sections. The difference lies in the fact that G/A-TD words, which are 17 data bits in length, are stored in the register address column of an array and, since the G/A-TD arrays are read out by addresses, one complete G/A-TD test word is transferred to the test CSR. Subsequently, a zero test of the G/A-TD test word is performed at the conclusion of the word transfer operation, eliminating the need for performing a parity or error check upon the test word.

As shown in Figure 4-9, the G/A-TD test information is sent over G/A-TD data channel lines to the data pulse stretcher flip-flop via energized K1. This relay is energized each time a unit loop test of the G/A-TD storage section is in progress. Each time the data pulse stretcher flip-flop is set, a 1 bit will be primed into the test CSR. Shifting of the primed bit in the test CSR is primarily a function of the test shift control and test shift flip-flops. This function is initiated by an OD 3-13-and-not-sync pulse, which is generated at the end of an array column readout.

In summary then, a G/A-TD test word is read out of an array by columns, with each column representing an address, and transferred via data channel lines to the data pulse stretcher flip-flop. The test data is then primed into the test CSR under the control of the data pulse stretcher flip-flop. Subsequently, the data bits are shifted to succeeding cores in the test CSR under the control of the test shift control and test shift flip-flops until all test data bits have been entered in it. The G/A-TD test word is now available for zero test purposes.

m. Error-Detection AND Circuit

When the complete test word has been read into the test CSR as described in 2.i., a test-transfer pulse initiates a synchronizing cycle which results in the sampling

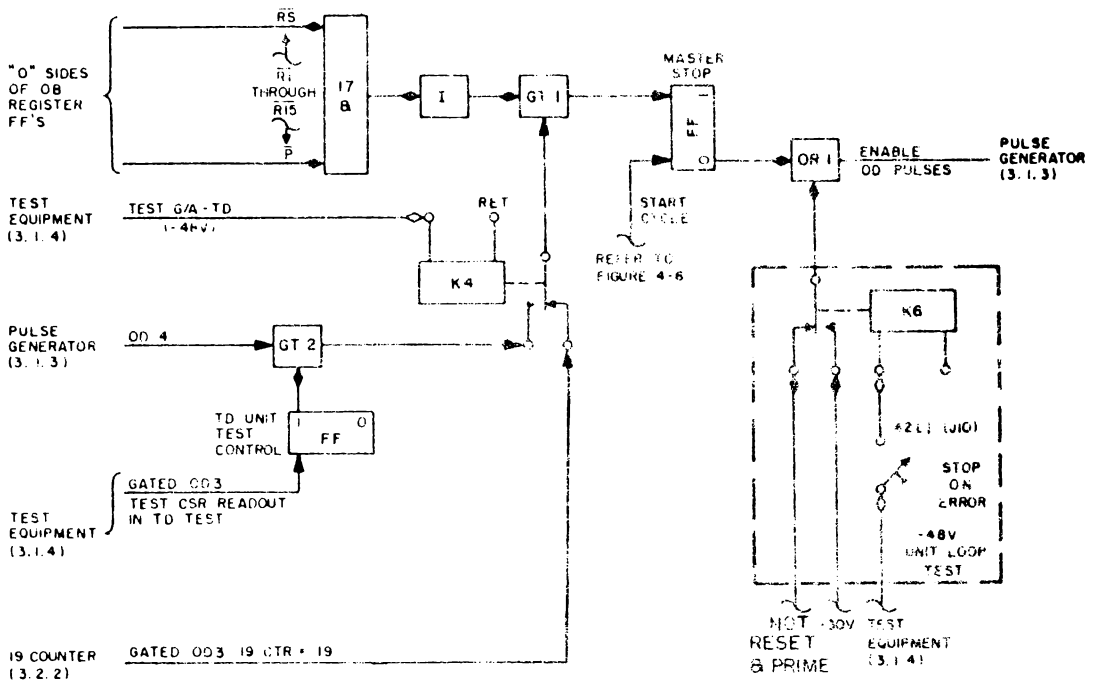


Figure 4-10. Zero Test and Master Stop Circuit (3.1.4), Simplified Logic Diagram

of each core in the register. Each core containing a 1 bit sends a complementing pulse back to a particular flip-flop in the flip-flop register of the output Drum System. This flip-flop would be the corresponding right test word flip-flop into which the bit was originally entered. If, in a particular right word flip-flop, the original bit entered was a 1 and the complementing bit is (correctly) also a 1, the flip-flop is complemented with the 0 side up.

If, in a particular right word flip-flop, the original bit was a 0 and the complementing bit is (correctly) a 0, the flip-flop will remain with its 0 side up. However, if the original bit is a 1 and the complementing bit is (incorrectly) a 0, or if the original bit is a 0 and the complementing bit is a 1, the flip-flop is complemented with the 1 side up.

As shown in Figure 4-10, the 0 side of the 16 right-word flip-flops of the flip-flop register and the 0 side of the output parity bit generator flip-flop are fed to the 17-way AND circuit. (See Figure 4-10.)

If none of these bits have been erroneously changed from 0 to 1 or from 1 to 0 during the processing through the Output System, the complementing of the flip-flops should reset the 0 sides of all the flip-flops. The 17-way AND circuit conducts. The inverter then prevents any further passage of the signal level. However, if one (or more) of the flip-flops is complemented with the 1 side up, which would happen if an error occurred in processing the test word, the AND circuit would not conduct. The inverter

then passes a level to the OR 1 circuit to condition GT 1. The select section bit switches (LS, L1, and L2) on the unit test door are operated to select a particular section (G/G, or G/A-TD), reflecting the section address of the test word. In any case, relay K2 shown in Figure 4-10 will be energized for G/A-TD and de-energized for G/G. For a G/G test word, K4 is in a de-energized state to pass a 19-counter-19 (OD 4-13) pulse; for a G/A-TD test word, K4 is energized to pass a gated OD 4 pulse. The individual pulses are then sent to strobe GT 1 as a zero test pulse for their respective storage sections. The pulses occur at the end of readout time in the respective sections and therefore arrive after the complete processing of the test word. If GT 1 is conditioned as a result of an error in the processing of the test word by the Output System, the gate passes the zero-test pulse. This sets the 1 side of the master stop flip-flop. Two actions can take place:

If the STOP ON ERROR switch (J10) has been operated to the closed position, the unit-loop-on-test voltage level is passed to energize K6, passing a -30v level to the OR 4 circuit. This results in the enable-OD-pulse-signal level's being produced only if the 0 side of the master stop flip-flop is up. Since an error causes the 1 side of this flip-flop to be up, the enable-OD level is cut off and the test stops.

If the STOP ON ERROR switch (J10) is not operated, a +10v level rather than a -30v level is applied to the OR 4 circuit. Therefore, except during a reset and prime operation, the enable-OD-pulse level remains up and the test operation cycles continuously without stopping. However, neons which are not shown in Figure 4-10 light if a flip-flop is not correctly complemented; these neons indicate the presence of an error.

3. Unit Loop Storage

The unit loop storage section is the test CSR previously described. It accumulates the processed test-word bits from the selected section and register of the output storage section. The bits are shifted into the test CSR, which is a series of 17 tape cores (core shifts) in serial form. At the end of the output storage section readout operation, the contents of the core shifts are read out in parallel form to complement the corresponding flip-flops in the right-half of the flip-flop register of the output control section, where the test word was originally entered.

Since the TTY word is not fed back to the flip-flop register for comparison with the original test word but is, instead, sent to a TTY monitor for a visual comparison, the unit loop storage discussion applies only to G/G and G/A-TD test words.

4. Parallel Readout Control

The parallel readout control circuit controls the parallel readout of the test word in the unit loop storage register (CSR). Selection of a particular storage section for unit loop test purpose is effected by closing select section switches LS, L1, and L2, located on the unit test door (Figure 4-1). Depending upon which section address is assigned to the test word, closing these switches singly or in combination will cause associated relays (K1, K4, or K5) to be energized during unit loop test.

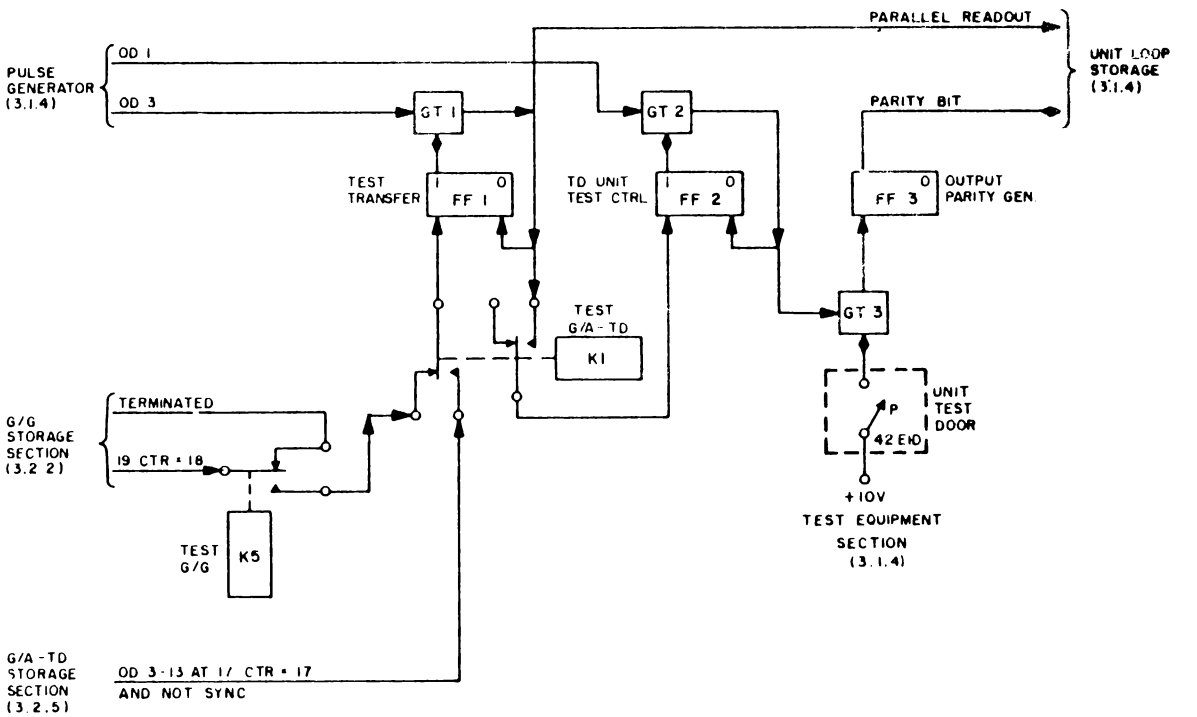


Figure 4-11. Parallel Readout Control Circuit (3.1.4), Simplified Logic Diagram

For a unit loop test of the G/G storage sections, a 19-counter-18 pulse is used to produce the readout pulse; for G/A-TD test an OD 3-13 at 17-counter-17 and not sync pulse is selected to produce the readout pulse. Each of these pulses occurs just before the last group of like-order bits is readout of their corresponding storage sections. Hence, these pulses occur just before the last bit is read into the first core shift in the test CSR.

As shown in Figure 4-11, when a unit loop test of the G/G storage section is being performed, K5 will be energized to pass a 19-counter-18 pulse. This pulse is then sent through the normally closed contacts of de-energized K1 to set the test transfer flip-flop. The latter flip-flop, when set, generates a level to condition GT 1 to pass an OD 3 pulse. This pulse is then sent as a readout pulse to strobe the parallel readout gates in the test core shift register circuit to effect the transfer of test information to the OB register for comparison purposes.

The parallel readout control operation for the G/A-TD storage section differs somewhat from that for the other storage sections because the G/A-TD right drum test word must reflect an odd-parity count as opposed to the even-parity count required for test words emanating from other storage sections. Therefore, to prohibit the G/A-TD test word from acquiring an even bit count (RS to R15) and thus producing an erroneous word indication, additional circuitry (shown in Figure 4-11) is introduced to provide and maintain the odd-parity status of the G/A-TD test word during the parallel readout operation to the OBR. The readout control operation and the generation of odd parity during a G/A-TD unit loop test are discussed in detail in the following paragraph.

At the end of a column readout of a G/A-TD core storage array, wherein a complete G/A-TD test word is transferred to the test CSR, a gated OD 3-13-at-17-counter-17-and-not-sync pulse is selected and passed via energized K1 to set the test transfer flip-flop (Figure 4-11). This relay is energized only when a unit loop test of the G/A-TD storage section is being performed. The test transfer flip-flop, when set, generates a level to condition GT 1, which is strobed by an OD 3 pulse. The conditioned gate thus passes the OD 3 pulse, which is then sent as a parallel readout pulse to strobe the parallel readout gates of the test CSR to effect the transfer of test information, to the OB register for comparison. In addition, the pulse clears the test transfer flip-flop. The OD 3 pulse is also sent to set the G/A-TD unit test control flip-flop via energized K1.

The latter flip-flop, having been set at OD 3 time, conditions GT 2, which is strobed by an OD 1 pulse. The OD 1 pulse is passed by the conditioned gate to clear the G/A-TD unit test control flip-flop, at the same time strobing GT 3. The latter gate is conditioned by a +10v level produced when parity switch P, which is located on the unit test door, is closed. Hence, to ensure the odd-parity status of G/A-TD test word, parity switch P is closed, conditioning GT 3, and the OD 1 pulse is passed to set the parity flip-flop in the OB register.

b. Core Register Circuit

The core register circuit, shown in Figure 4-12, is a tape-core register of 17 core shifts and is similar to the 19-counter in the G/G storage section. The processed test-word pulse from the storage register control circuit reads the extracted bits into the read-in winding of the first core of the register. This read-in occurs for 5.0 usec between OD 4 and OD 2 times. The shift pulse starts at OD 2 with the receipt of the start-shift signal from the storage register control circuit. The start-shift signal and the end-shift signal control the test shift flip-flop. This flip-flop supplies the shift pulse to the register. The shift pulse lasts 2.5 usec, from OD 2 to OD 3. At OD 3 time, following the shift pulse, the former content of each core appears at the output line to the gate circuit at the same time that the bit is being read into the next core. However, there is no transfer through these gates unless they are pulsed by the readout signal. After the last pulse, however, the register is full. The readout signal, which comes from the parallel readout control circuit at OD 3 time and coincides with the end shift signal, is applied to the parallel readout gates, causing the information to be transferred.

Thus, in the parallel readout operation, each bit is directed back to the individual flip-flop of the OB register from which the bit was originally generated.

4. Specific Unit Loop Tests

The preceding paragraphs described the general, common circuitry and processes used in performing a unit loop test involving any of the storage sections in the Output System. The paragraphs which follow describe the particular processes and circuitry which are unique for each particular storage section. As has been previously mentioned, the output control element functions in the normal manner regardless of the storage section selected.

a. Ground-to-Ground

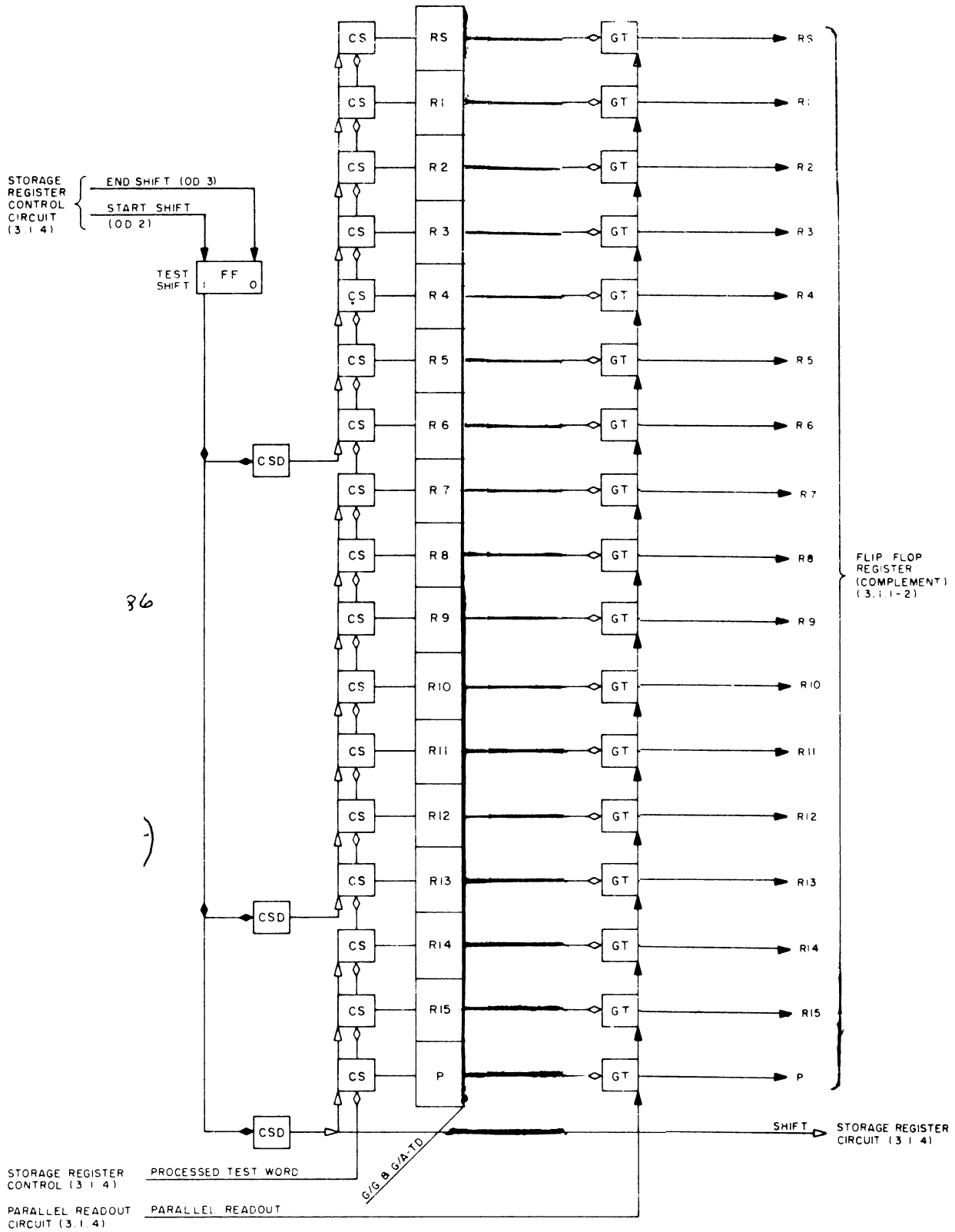


Figure 4-12. Core Register (3.1.4), Simplified Logic Diagram

The over-all operation of the G/G storage section during a unit loop test is essentially the same as during normal operation except for a few minor variations. In effect, unit loop testing of the G/G storage section is begun by activating the UNIT TEST pushbutton, causing the output test relay voltage to be applied to the test circuitry. Prior to setting up the test word, the OB register is isolated from the Drum System, the G/G burst counters are inhibited, and alarms are cleared. Inhibiting the reset of the right drum word flip-flops is automatically performed when in a unit loop test. The desired section address and the test word are selected manually by means of bit switches located on the unit test door. If it is desired, a STOP ON ERROR switch is engaged to detect errors and stop the test cycle.

The unit test operation commences when the START CYCLE pushbutton is activated. The manually selected test word is then automatically read into each individual address register of the G/G-FD core storage array until all legal register addresses have been read into. This automatic read-in of the test word into all register addresses may be substituted by an alternate method of read-in, whereby the test word is manually stepped into each address register.

Subsequent to the above read-in operation (automatic or manual), the test word stored in the array is read out in columnar fashion; that is, the resultant test data bit count of the column is read out and transferred via relays to the test CSR circuitry. During the transfer operation, an error check is performed on the test data bit count to determine whether bits have been grown or lost during the test word reading operation. In any circumstances, the test word is entered into the test CSR bit by bit under control of the unit loop test control circuitry.

The G/G storage section comprises two core storage arrays; hence, a unit loop test of this storage section necessitates that both arrays (A and B) be subjected to test. In addition, other circuitry peculiar to the G/G storage section (namely, the CMSR circuit and the switching circuit, which is used principally to switch test data information from one array to another) is also subjected to scrutiny during a unit loop test.

In the G/G unit loop test, a test word is automatically read into all the address registers of an array (say array A) during the search time period. The test word stored in array A is then read out during the first cycle of the 19-counter while, at the same time, the test word is being written into array B. At the completion of the array A readout cycle (19-counter-18 time), an OD 4-13 pulse is generated to complement the phase flip-flop to a 1. The latter, when set, produces a shift phase B level, thus selecting array B for readout of the G/G test word. Array B is read out during the second 19-counter cycle while, at the same time, the test word is being written into array A. At the end of the second 19-counter cycle at 19-counter-18 time, the phase flip-flop is complemented to 0 by an OD 4-13 pulse. In this state, the phase flip-flop generates a level selecting array A for readout of the test word.

It may be noted that, as one array is being read into, the other is being read out; hence, each array (A or B) is read out at every other cycle of the 19-counter.

The G/G test word may be automatically or manually stepped into all address registers of a selected array. If the automatic-address stepping mode is used during a unit loop test, then the CMSR flip-flop neons located on the duplex maintenance console

will be set, indicating that all legal address registers have been filled with the test word, that all message slots have been filled with the test word, and that readout of the test word is taking place. However, if the manual-address stepping mode is used during a unit loop test, the CMSR flip-flops will remain cleared because, in this mode, the G/G test word is entered into and is read out of each individual address register of a selected array one at a time; hence, the CMSR message slots are never filled with the test word and thus no completed message indications by the CMSR flip-flop are presented.

Following the readout of the G/G test word from core storage array A or B, the word is routed via relays to the test CSR circuitry. During transfer operations, an error check is performed on the test data bit count to determine whether bits have been grown or lost during the test word reading operations. In any circumstance, the test word is entered into the test CSR bit by bit under control of the unit loop test control circuitry. At the end of an array readout, a 19-counter-18 pulse is generated and sent to the test CSR, causing the test word in the core register to be readout, in parallel fashion. At this time, a zero test is performed on the G/G test word; that is, if the word in the OB register is not correctly complemented, an error has occurred and, with the STOP ON ERROR switch in an activated state, the test cycle will end. On the other hand, if the OB register has been correctly complemented, thus indicating no error, the test cycle will be repeated until the END UNIT TEST pushbutton is activated.

c. Ground-to-Air Time Division

Unit loop testing of the G/A-TD storage section is similar in many respects to the unit loop test operation described for the G/G storage section except for a few minor variations, some of which are mentioned herein.

Like the G/G storage section, the G/A-TD storage section comprises two core storage arrays, a CMSR circuit, and a decoding circuit which is used specifically to select either of the two arrays in this section. In addition, the G/A-TD test word may, like T/G test words, be automatically stepped into all address registers of an array or manually stepped into each, both operations having been explained in previous paragraphs. However, unlike the other storage sections, where a test word is contained in columns of like-order bits in their respective storage-section arrays (that is, one array column contains all RS bits, the second, all R1 bits . . .,etc.), the G/A-TD core arrays store a complete G/A-TD test word in each address column (there being 12) of their respective arrays. Furthermore, unlike the other storage section, readout of the G/A-TD test word from the individual arrays is performed by address, in parallel fashion to one or two OSR's, depending on the mode the G/A-TD is in.

This is in direct contrast to that method of readout employed by the other storage sections, where columns of like-order bits are read out in parallel fashion to one OSR.

In the G/A-TD unit loop test, a test word is automatically entered into each address column of a selected array (A or B) during the G/A-TD search time period. The test word now contained in all address columns of an array (say array A) is read out to the OSR's during the first cycle of the 15-counter while the test word is being read into array B. At the completion of the first 15-counter cycle (15-counter-15 time), an OD 4-13 pulse is generated to complement the phase flip-flop in the decoding circuit

to a 1. The latter, when set, generates a shift phase B level, thus selecting array B for readout of the test word during the second 15-counter cycle while the test word is being read into array A. Like the G/G storage section, as one array is being read into, the other is read out at every other cycle of the 15-counter.

As in normal operation, the G/A-TD dual channel test words, when read out of the selected array, are temporarily stored in the OSR(s), one word per OSR, whereupon they are simultaneously shifted out of the OSR(s) in serial fashion to separate test data lines and routed to the test circuitry. In the test circuit, the G/A-TD test words are processed in the same manner as described for unit loop testing the G/G storage section, except that different control pulses are used to synchronize the G/A-TD test word flow through the test circuitry during a unit loop test. First, synchronization is accomplished by using the OD 3-13-and-not-sync pulse to shift the G/A-TD test data bits into the test CSR until a complete test word has been read into the test CSR. Secondly, an OD 3-13-at-17-counter-17-and-not-sync pulse is used to initiate the transfer of the G/A-TD test word from the test CSR to complement the OB register (see Figure 4-11). Thirdly, a gated OD 4 pulse is used to zero-test the G/A-TD test word for any errors that may occur during unit loop tests (Figure 4-10).

It has been stated that the test data information is routed over two test data channel lines, channels 1 and 2. However, only one test data line is tested on one time. Therefore, selection of a particular test data channel line for test is largely dependent on the status of the TEST G/A-TD CHAN 2 switch. If the latter is activated, the test data contained in the test data channel 2 line will be processed for test. If the latter is left inactive, the test data contained in test data channel 1 line will be processed for test. G/A-TD, single channel, operation is very similar to dual channel except for a few variations. In the single channel mode, G/A-TD test words are readout of the array to OSR 1, one at a time. No test words are placed into OSR 2. All G/A-TD test words are individually shifted out of OSR 1 to the test CSR. The G/A-TD data channel select switch must remain in the Channel 1 (inactive) position, during unit loop of G/A-TD single channel operation.

d. Teletype Monitor Test

During testing, the TTY output storage section functions in much the same way as during normal operation except for a few minor variations in operations. As has been previously described, in the TTY test, the test word is not looped back to the test control circuits and to the 17-way AND circuit for zero test but is passed to a monitor where a visual comparison is made between the original test word and the processed test word. (Figure 4-13.)

When setting up the test word, the procedure followed is the same as that previously described for a G/G and G/A-TD word, except that, for a TTY test word, bit RS must always be a 1. The latter, preceding the test word, produces the start signal required to initiate the TTY monitor into operation. The remaining bits of the right drum word are selected to represent a particular TTY character.

The TTY storage section is selected for unit loop test purposes by means of selection bit switches located on the unit test door. When a computer under test is in a standby mode, its respective TTY channel relays are arranged in series, since

they are not energized. In normal operation (outputs active), however, the TTY channel relays are energized, and their respective contacts are made to operate independently of other relay contacts.

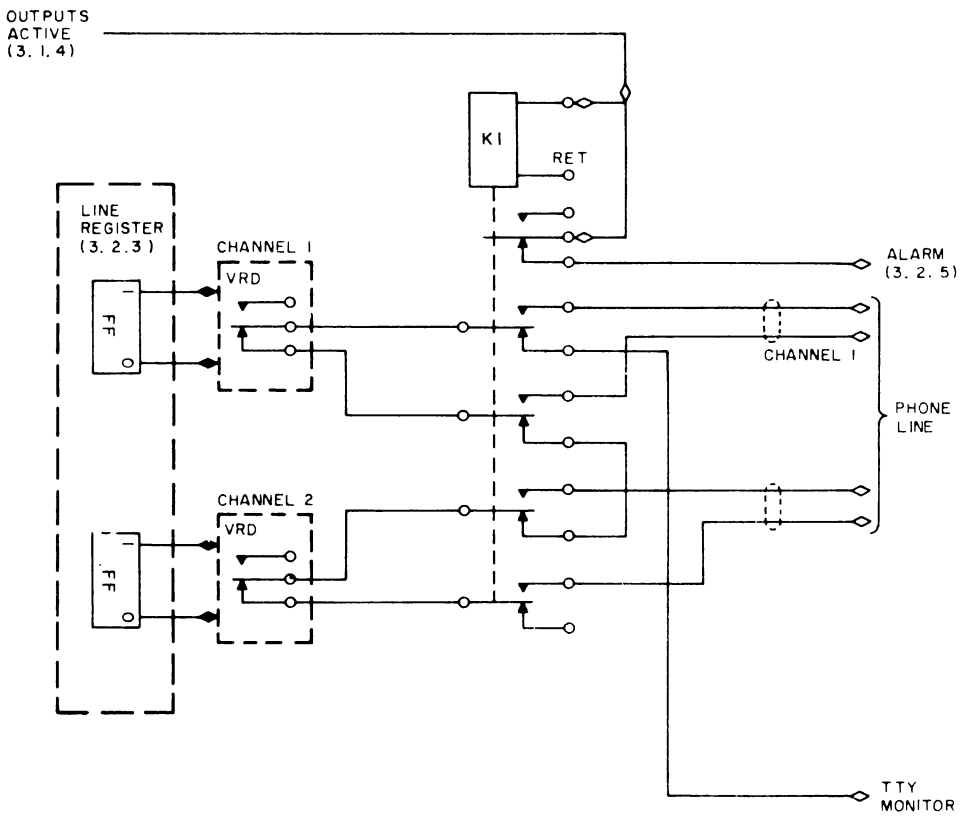


Figure 4-13. TTY Duplex and Test Switching for Messages 1 and 2 (3.2.3)

At the beginning of test, a start-search pulse is applied to the test word generator. This initiates the read-in of the test word into the OB register and the automatic address register stepping of the test word in all addresses of the TTY core array. In addition, the start-search pulse is transferred and routed to inhibit the TTY burst counters.

During test, the test word data bits are read out of the storage array to the OSR under control of the 51-counter. In the OSR, the test data bits or test words are stored temporarily and subsequently shifted out under the control of the 51-counter to complement the output parity counter flip-flops. These flip-flops are used to sample the test word for errors. At the same time, the test data bits are routed to the conversion circuit, where they are applied to the set lines of the conversion circuit flip-flops. The output levels generated from these flip-flops are supplied to energize relays (VRD's) associated with each of the conversion flip-flops. These relays control the transfer of test data bits to their respective TTY channel lines. Thus, when a conversion

flip-flop is complemented to the 1 side, its corresponding relay (VRD) will be energized to open the TTY channel line to produce a space signal (Figure 4-13). Conversely, when a flip-flop is caused to rest on its 0 side, its corresponding relay will close the TTY channel line, producing a mark signal. In this fashion, the binary-coded test word is made compatible with the input signal requirements (mark or space) required of the TTY monitor for proper operation.

As previously stated, when the automatic-address stepping mode is used during a TTY unit loop test operation, the TTY channel relay contacts are arranged in series order so that, whenever a channel relay is caused to open, all other channel relays will open. Similarly, when a channel relay is caused to be closed, all other channel relays will close. However, when the single-address stepping mode of operation is used, the individual channel relays are made to operate independently of each other.

Computer Loop Test

1. General

The computer loop test is a comprehensive check of the input and output circuits of the AN/FSQ-7 Combat Direction Central. It tests the operation of the Output System, Input System, Drum System, and various parts of the Central Computer System itself. During the test, the flow of information through the various elements of both the AN/FSQ-7 and AN/FSQ-8 Centrals closely approximates the information flow in the respective equipments when they are actually processing the air defense problem.

Basically, the test comprises two modes, each of which is separately tested. On one mode, the outputs of the G/A-TD storage section are looped through the output test section to the long-range radar input (LRI) element. In the other mode, the output of the G/G storage section is looped through the test equipment section to the cross-tell (XTL) input element. Figure 4-14 shows the two paths of information flow.

In both modes, the test information originates within the Central Computer System and is passed through the OB fields of the Drum System to the Output System. In the Output System, the test information passes through the G/A-TD storage section to the test equipment section, and on to the LRI element of the Input System; from there it passes through the LRI field of the Drum System and back into the Central Computer System for comparison with the original test information.

The other path is through the G/G storage and test equipment sections to the XTL element of the Input System, through the XTL field of the Drum System, and back to the Central Computer System.

a. Ground-to-Ground to XTL Loop

In the regular operation of AN/FSQ-7 Combat Direction Centrals, the output of the G/G storage section is transmitted over telephone line circuits to one of the adjacent AN/FSQ-7 Combat Direction Centrals. Information enters the adjacent equipment through the XTL input element, the manner in which the information is transmitted, therefore is compatible with the operation of the XTL input element.

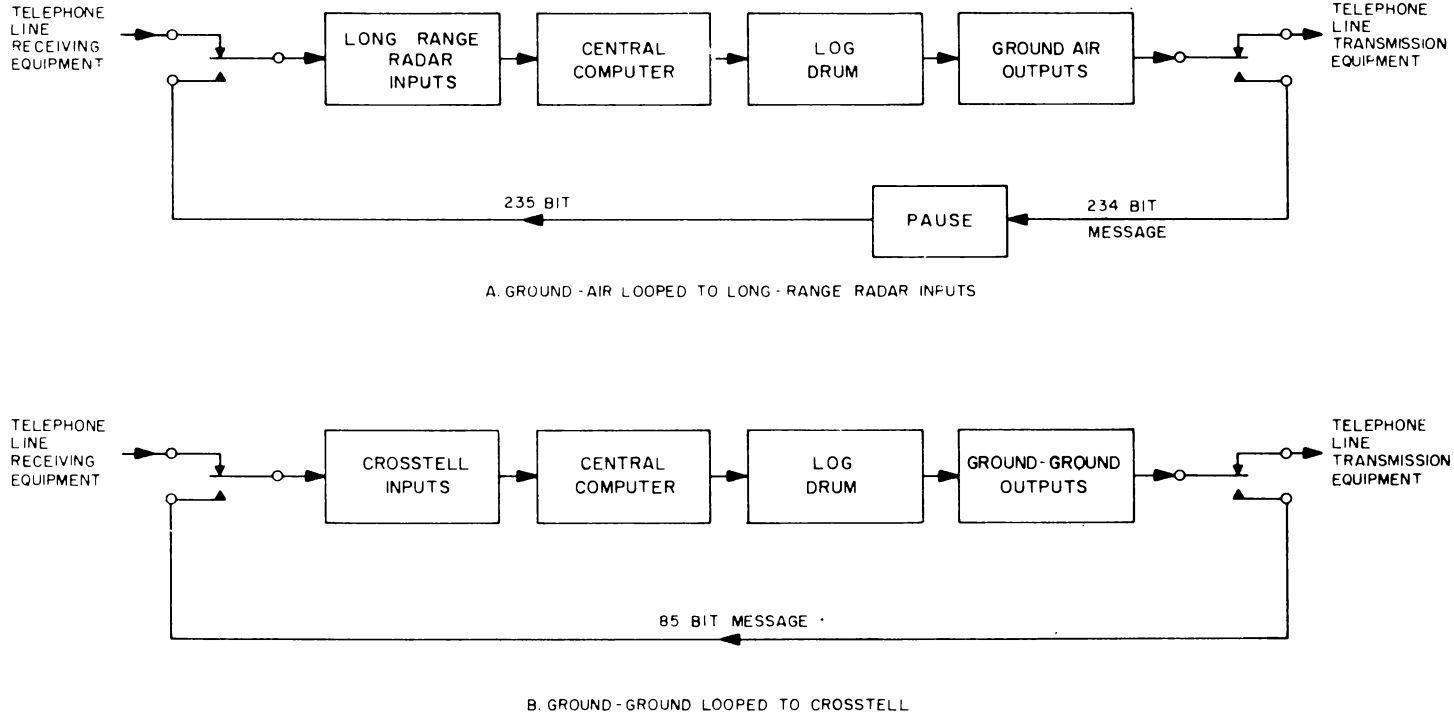


Figure 4-14. Computer Loop Test, Flow of Data, Simplified Block Diagram

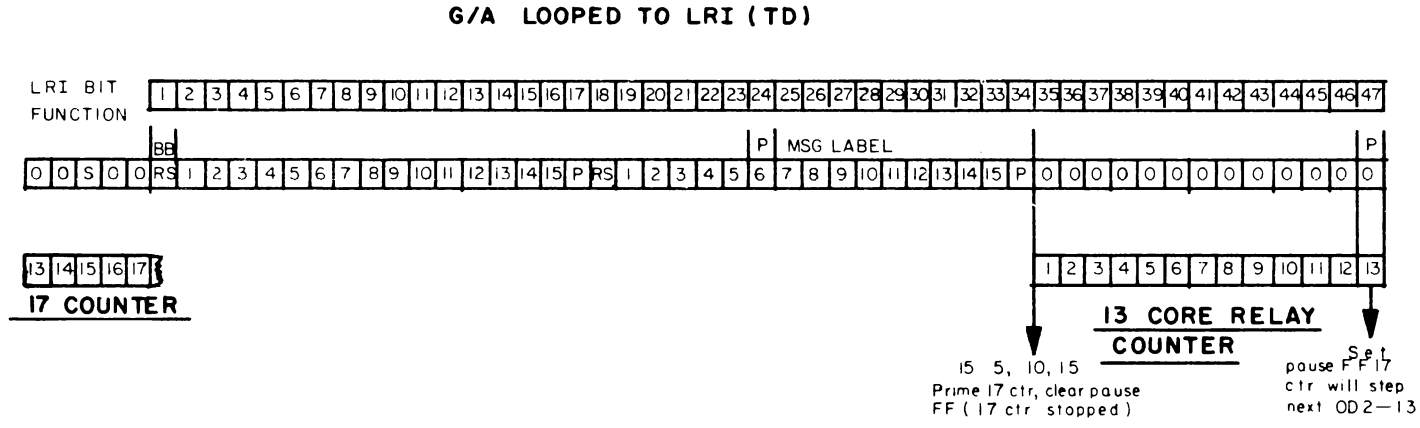


Figure 4-14A. Message Layout Computer Loops

There are five G/G output channels. Each of these channels is capable of being included in the computer loop test, one at a time. Further, there may be several XTL input channels in the XTL input element. Only one such input channel may be used at one time in the computer loop test. Therefore, to conduct the test, it is necessary to select one G/G output channel and one XTL input channel. The test information is programmed to pass through the Output System and must reflect the channel selection in the address part of the information. The output channels are selected and switched automatically within the computer loop control. Since the information is already compatible it is switched straight through the computer loop control without any modification. The test information is programmed within the Central Computer System.

b. In the normal operation of AN/FSQ-7 Combat Direction Centrals, the G/A-TD storage section outputs are forwarded to data link receivers via telephone transmission lines.

Data information from the storage section is routed over two output channels, and messages to each data-link receiver contain 234 data pulses.

The LRI element requires five 47-bit words each word preceded by a specific sync pattern (00S00). (See Figure 4-15.) Thus, the LRI element must be provided with a total of 235 bits of information plus the sync pattern. The 235 bits represent one bit more than the G/A-TD array can provide. Hence, an additional bit must be supplied which is always a 0. Paragraph 2a describes the circuitry involved in making a G/A-TD to LRI computer loop test or a G/G to XTL input loop test.

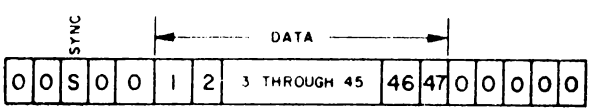


Figure 4-15. Long-Range Radar Input Message

c. TTY Monitor Test

A computer loop test may be performed on the TTY storage section. However, there is no provision for feeding information from the Output system back to the Central Computer. Therefore, a TTY monitor such as is used in the TTY unit loop test is used in the TTY computer loop test.

2. Computer Loop Control

a. G/A-TD to LRI Channel Selection

Channel selection of the various sections of the AN/FSQ-7 equipment during a computer loop test operation is effected by means of programming. Programs are

generally written to route test data information over individual channels of selected sections in concurrent fashion, incurring no delay between the selection of the individual channels.

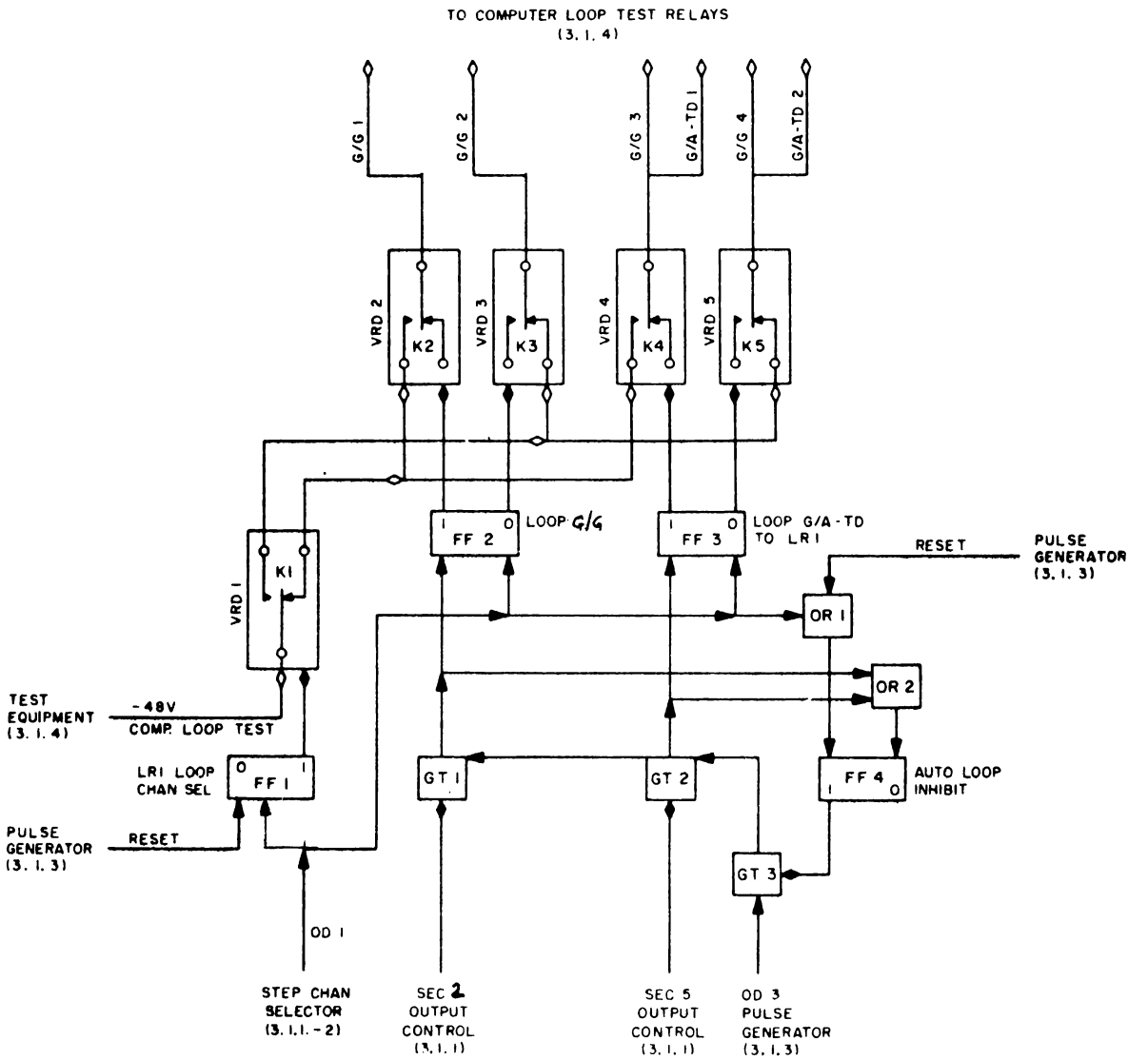


Figure 4-16. Computer Loop Test Channel Selection Circuit (3.1.4), Simplified Logic Diagram

The selection of section and channel is accomplished by means of the channel selection circuit shown in Figure 4-16. It can be seen from the figure that a BTC pulse occurring at OD 1 time is obtained by selecting the burst time counters and reading $10_{(8)}$ (octal) words. The select-selection levels are obtained from the section decoder circuit,

which determines which channels or sections will be selected to route the test data information. These levels are of 7.9-usec duration and occur each time a word is read into the OB register.

To computer-loop test G/A-TD channels 1 and 2 by means of programming, the following pre-operational test procedure must take place. The OUTPUTS TEST-OPERATE switch is operated to the TEST position. This applies -48v to the armature of K1 of circuit VRD 1. Next, the RESET flip-flops pushbutton is depressed. This action clears the LRI loop channel selection flip-flop (FF1), de-energizing K1 and thus allowing -48v to be applied to the normally closed (NC) contact points of K1. The program is written so as to cause the burst time count to be selected and read ($10_{(8)}$ times) twice, thus generating two step-channel (OD 1) pulses. This action is required to ensure that all the channel selection flip-flops are clear and that the auto loop inhibit flip-flop (FF 4) is set before a computer loop test of a particular section and its associated channels can take place.

With the generation of the first OD 1 pulse, FF 1 is complemented to its 1 side; the loop G/A-TD to LRI flip-flop (FF 3) is cleared, and FF 4 is set via the OR 1 circuit. In order that the conditions established in the preceding paragraph may be met, a second OD 1 pulse is programmed to complement FF 1 back to its clear side; FF 3 will remain cleared, and FF 4 will remain set, ending the pre-operational test procedure. A G/A-TD section and its associated channels can now be selected for computer loop test purposes.

When the first G/A-TD word is read into the OB register, a select-section-5 level is generated to condition GT 2. Flip-flop 4, having been set by an OD 1 pulse generates a level to condition GT 3. Both GT's 2 and 3 are now conditioned to pass an OD 3 pulse to set FF 3. The OD 3 pulse is also returned via OR 2 to clear FF 4, de-conditioning GT 3.

Flip-flop 3, having been set at OD 3 time, allows the -48v to be passed through the normally closed (NC) contact points of de-energized K1 of VRD 1 and to be subsequently fed to the normally open (NO) contact points of energized K4 in VRD 4. This relay voltage is then applied to energize the G/A-TD channel 1 computer loop test relay, enabling G/A-TD channel 1 test data to be looped to the LRI element, via the LRI test bus lines and the test pattern generator, to be returned to the Central Computer for comparison purposes.

If desired, the computer loop test program can be written to process the test information repeatedly over the same section and channel, another channel within that section, or proceed to select another section for test. On the other hand, if it is desired, say, to select channel 2 of the G/A-TD storage section, then the program is written so that once again the burst time counter is selected and then read. The BTC, having been read, generates at this time a step-channel selection (OD 1) pulse to complement FF 1 to its set side. The latter generates a level energizing K1 of VRD 1 and enabling -48v to be passed through its normally open (NO) contact points and applied to K5 or VRD 5.

This, in effect, removes the -48v relay voltage from VRD 2 and de-energizes the G/A-TD channel 1 computer loop test relay. In addition, the OD 1 pulse is applied to the 0 side of FF 2 and to the 1 side of FF 4. Flip-flop 3 will again be set upon receipt of the first Section 5 Drum word.

Flip-flop 3, being set, energizes K4 and de-energizes K3, thus the -48v is passed through the normally closed contacts of K5 to energize the G/A-TD channel 2 computer loop test relay. Hence, the drum test word data is routed over the G/A-TD channel 2 lines and looped to the LRI element, via the LRI test bus lines and the test pattern generator, and returned to the Central Computer for comparison purposes.

It should be noted from the figure that G/G Channels 3 and 4 are selected in coincidence with the selection of G/A-TD channels 1 and 2. However, this does not contribute any adverse effects on the G/A-TD channel selection operation since the G/G test data information is looped to the XTL element, whereas the G/A-TD is looped to the LRI element.

b. G/G to XTL Channel Selection

The procedure used for computer-loop testing the G/G storage section and its associated channels is the same as that described in the previous paragraph for the G/A-TD storage section. As shown in Figure 4-16, the VRD 4 circuit must be energized if it is desired to select a G/A-TD channel 1 or G/G channel 3 line for test. This circuit is energized only when a select section-5 level is present and when FF 3 is in set status. It is apparent, therefore, that, when selection of a G/G channel 3 line is required it is necessary that, initially, the first word received from the OB drum be made to contain a G/A-TD section number. In all other cases, select-section-2 level is required initially to effect selection of the remaining G/G channels.

Using this method of selection, it is possible to check the G/A-TD channel 1 line and then, without changing the status of the selection circuit, go on to check the G/G channel 3 line. The two checks may be performed alternately or simultaneously.

c. Stop to Drums

When the STOP TO DRUMS switch is activated, K2 is energized (Figure 4-17). This sends a -30v level as a non-reset-on-error signal and a +10v level as a stop-to-drum signal level to the alarm control section. The -30v non-reset-on-error signal causes the contents of the flip-flop register of the output drum section to be retained for inspection if a parity-NG, an illegal register, or section address alarm is produced (Figure 2-44). The stop-to-drums pulse is passed to Drum System if either of the previously mentioned errors occurs. It stops the Drum System and prevents the erasure of the test word so that the error can be examined.

d. Restart-to-Drums Circuit

When the OUTPUTS TEST-OPERATE switch is moved to the OPERATE position, the falling of the test-outputs signal generates a pulse in the restart to-drums circuit (Figure 4-18). This pulse sets the synchronizing restart-to-drums-sync flip-flop. The restart-to-drums flip-flop is set at the following OD 3 time; at

OD 1 time, the restart pulse is generated. The restart pulse is carried to the Drum System and to the parity generator of the output control element. This pulse is used in the Drum System to re-enable the transfer of the information from the OB drum to the Output System. In the output control element, the pulse causes a compare signal to be sent to the Drum System for 100 ms but prevents any words from being accepted during this interval. This prevents any stale information in the drums from being transferred and causes such information to be erased from all three OB drum fields. The outputs-active signal, which arrives when a system is changed from standby to active has the same effect as the test-out-signal.

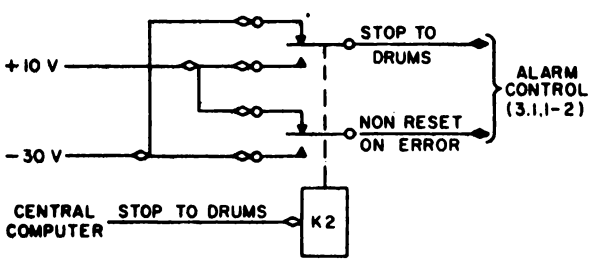


Figure 4-17. Stop-to-Drums Circuit (3.1.4), Simplified Logic Diagram

e. 13-Core Delay Counter

In general, a G/A-TD test message is composed of 39 timing pulses; 34 of these represent G/A-TD data, and the remainder constitute the sync pattern (00S00) which precedes each G/A-TD test message (2 words). Since each LRI message requires a total of 52 timing pulses, including the sync pattern, the transmitted G/A-TD test data must be modified. The latter, when modified is then compatible with the requirements of the LRI input element.

Modification of G/A-TD messages during a G/A-TD to LRI computer loop test is accomplished by the 13-core delay counter circuit (see Figure 4-19). During the delay initiated by the 13-core delay counter, the shifting of the 17 counter is inhibited by the 13-core delay counter, thus preventing the readout of any G/A-TD data and thereby allowing 13 timing pulses to be transmitted without any data being transmitted on the data lines. These 13 timing pulses when added to the 39 data pulses of the G/A-TD test message, make the message compatible with the LRI input equipment requirements of 52 timing bits per message. A detailed discussion of the operation of the 13-core delay circuit follows:

Assume that a G/A-TD test message consisting of four 17-data bit words has been read out of the OSR's (two words per channel) preceded by their sync pattern 00S00. At this time, the following conditions will be evident:

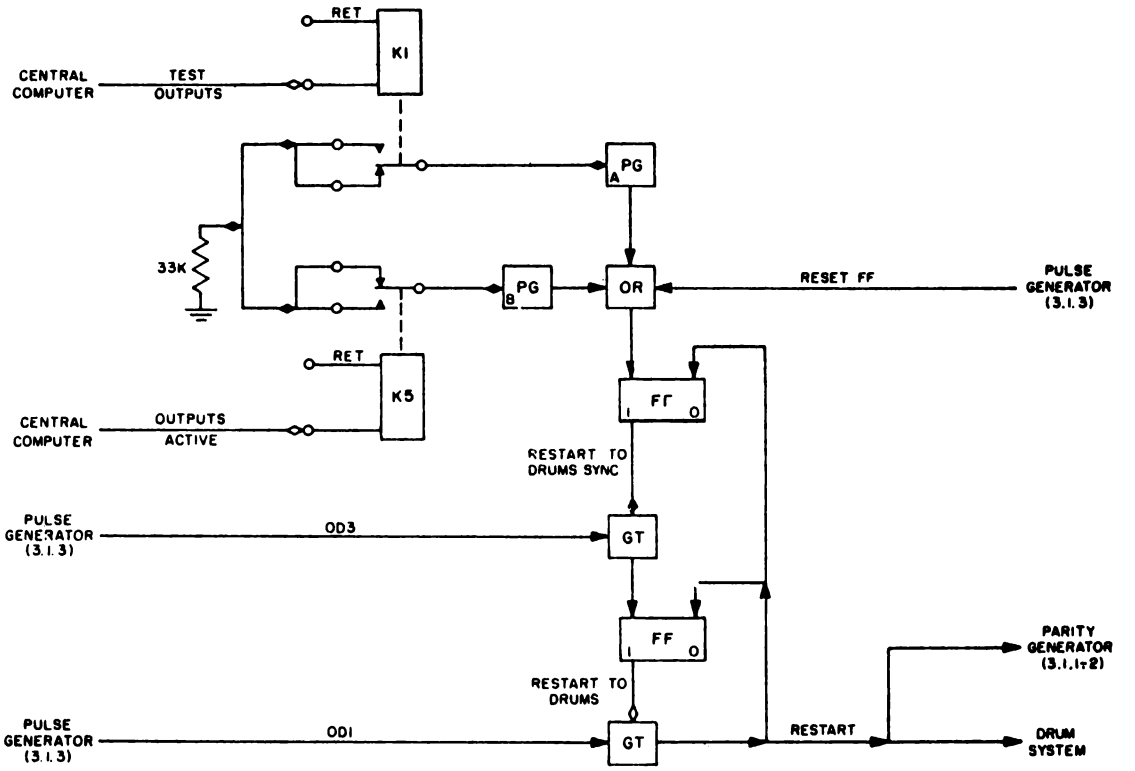


Figure 4-18. Restart-to-Drums Circuit (3.1.1-2), Simplified Logic Diagram

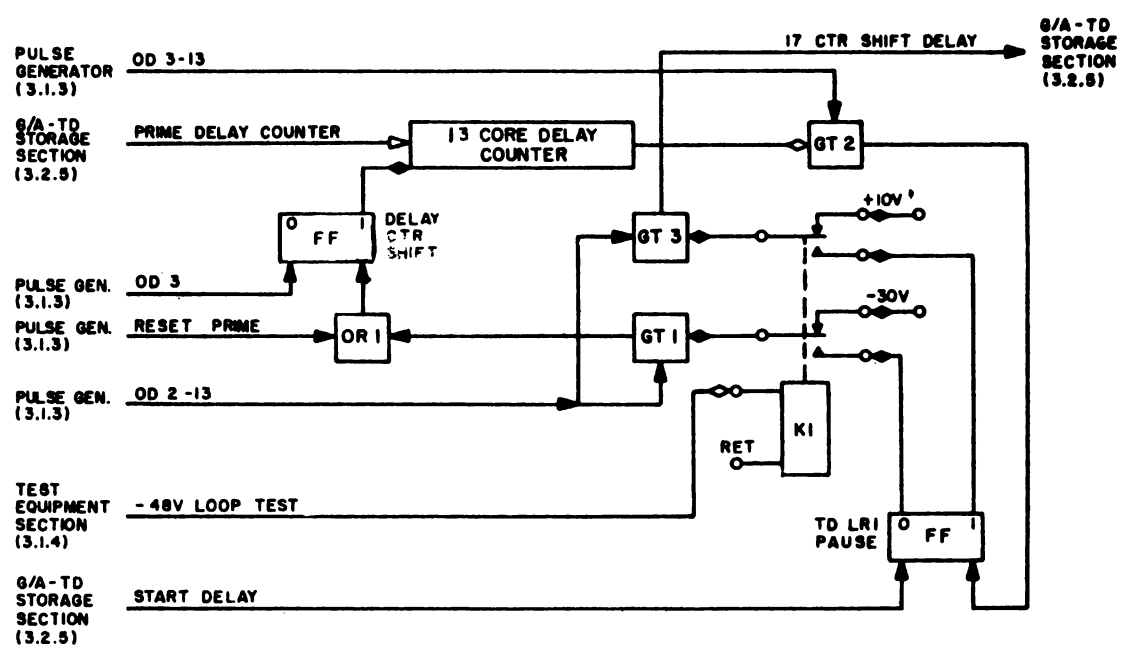


Figure 4-19. G/A-TD 13-Core Delay Counter (3.2.5), Simplified Logic Diagram

(1) The 17-counter fast-shift flip-flop is cleared.

(2) The 15-counter is shifted to 15-counter-5 time.

(3) The 17-counter is being reset and primed.

At 15-counter-5 time, an OD 4 pulse is gated to set the sync generator flip-flop, the 17-counter shift flip-flop, and the 17-counter sync flip-flop preparatory to the readout of G/A-TD message slot 2. With the setting of the 17-counter sync flip-flop, a level is generated to condition a gate which is strobed by an OD 3 pulse. The conditioned gate passes the OD 3 pulse, which in turn is used to perform the following:

(1) Set the 17-counter prime flip-flop.

(2) Clear the TD LRI pause flip-flop.

(3) Clear the 17-counter sync flip-flop.

The 17-counter prime flip-flop, when set by the gated OD 3 pulse, generates a level to prime the 13th core of the 17-counter (see Figure 3-49), readying the 17-counter for sync pattern generation. This level is also used to prime the first core of the 13-core delay counter, alerting this counter for the 13 timing pulse delay required to modify the G/A-TD test message.

The operations depicted above are applicable only during a G/A-TD computer loop test operation. When the OUTPUTS TEST-OPERATE switch is set to the OPERATE position, K1 (shown in Figure 4-19) will become energized. The same OD 3 pulse that sets the 17-counter prime flip-flop is also used to clear the TD LRI pause flip-flop. The TD LRI pause flip-flop, when cleared generates a level through the closed contact points of K1 to condition GT 1. At the same time, a -30v level emanating from the set side of the flip-flop is applied to decondition GT 3. Deconditioning GT 3 prevents the shifting of the 17-counter during the delay. Conditioned GT 1 will pass an OD 2-13 pulse to set the delay counter shift flip-flop via the OR 1 circuit. This flip-flop is cleared by OD 3 pulses; hence, this flip-flop generates 2.5 usec shift pulses, which are used to shift the 13-core delay counter.

Coincident with the shifting of the 1 bit in the 13-core delay counter by the delay counter shift flip-flop, a timing pulse is passed to the LRI element. Therefore, at the completion of the operational cycle for the 13-core delay counter, 13 timing pulses will have been passed to the LRI element. At the same time, GT 2 is conditioned to pass an OD 3-13 which is used to set the TD LRI pause flip-flop. When the latter is set, GT 1 is deconditioned, preventing the shifting of the 13 core delay counter. In addition, GT 3 is conditioned to pass OD 2-13 pulses, which are subsequently used to shift the 17-counter. Shifting the 17-counter initiates the generation of the sync pattern for the following test message.

It can be seen therefore, that each time a G/A-TD message comprising 39 data pulses is transmitted to the LRI input equipment a 13 timing pulse delay is executed by the 13-core delay counter circuit. As a result, the G/A-TD test message is modified to conform to the 52 timing pulses needed for an LRI message.

SUMMARY QUESTIONS

(True or False)

1. The G/A-TD output message is changed to 47 LRI input messages in computer loop test.

2. In G/A-TD, G/G and TTY unit loop test the zero test of the OBR can be used effectively to find errors in the right half word.

3. There are 25 TTY monitors, one for each channel, at each site.

4. If the Test-Operate switch on the maintenance console is in the operate position, the output system cannot be placed in unit loop test.

5. There are six alarm lights at the top of the test door.

6. The sync bit for message one is the normal sync bit that is generated in G/A-TD outputs.

7. G/A-TD and G/G can be placed in test at the same time, then the word will be read into both arrays.

8. While computer loop testing the G/A-TD outputs, the Xtell input channels are used.

9. The "Stop on Error" switch must be on in order to allow the "Master Stop" FF to stop operation.

CHAPTER 5. AN/FSQ-8 OUTPUT SYSTEM

1. General

This section of the lesson plan contains pertinent information relative to the function and operation of an AN/FSQ-8 Combat Control Central in the SAGE System. Since, in a functional (tactical) sense, a Combat Control Center occupies a higher station in the command echelon of the SAGE system than that held by a Combat Direction Center, it is axiomatic that the equipment utilization of a Control Central also differs from that of a Direction Central.

Basically, the equipment complex of an AN/FSQ-8 Combat Control Central is similar to that employed in an AN/FSQ-7 Combat Direction Central with a few exceptions. The main exception is that a Control Central has no facilities for communicating directly with manned or unmanned interceptors. Consequently, ground-to-air (G/A-TD) output facilities (required in a Direction Central) are not required in a Combat Control Central.

The facilities utilized in the Output system of a Control Central are the ground-to-ground G/G and the teletype (TTY) storage sections. The operation of these two storage sections, including the differences (circuit or operational) between them and their Combat Direction Central counterparts, is discussed in the ensuing paragraphs.

2. Output System in AN/FSQ-8 Combat Control Central

The computer that is utilized in a Combat Control Central is a modified version of the AN/FSQ-7 Computer shown in Figure 5-1. The Output System in an AN/FSQ-8 Central comprises the G/G and TTY storage sections. These storage sections operate in a manner similar to that described for their Direction Central counterparts, but for a few exceptions. Therefore, for purposes of brevity, it is necessary to discuss in this part of the Student Text only the circuit or operational differences between the AN/FSQ-7 and AN/FSQ-8 Output Systems.

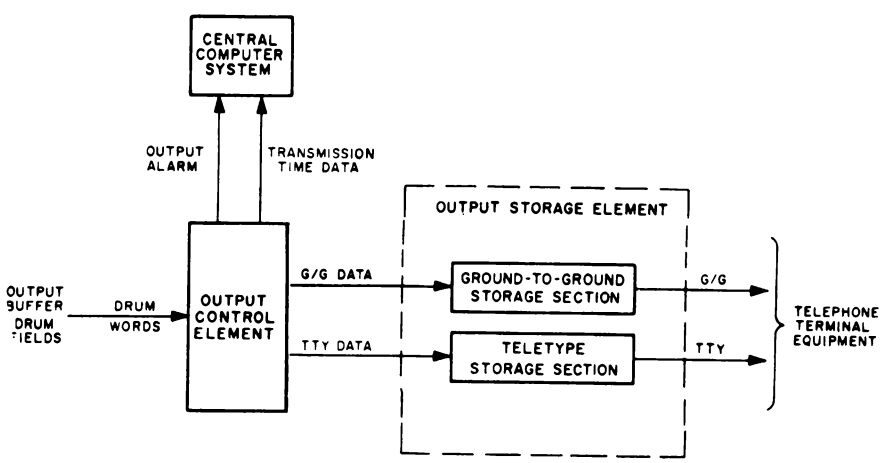


Figure 5-1. Output System, Block Diagram

Difference Data

1. Description

The difference data presented in this chapter has reference to the departures from the circuit and functional operation which normally complements an AN/FSQ-7 Combat Direction Central and is used exclusively in an AN/FSQ-8 Combat Control Central.

Except for the differences mentioned herein, the operation of the Output System in a Direction Central, as described in the preceding parts of this Student Text is also pertinent to the Output System in a Control Central. Hence, when applicable, all references relating to an AN/FSQ-8 Output System operation should be directed to that information contained in previous discussions in this Student Text which are concerned with the operation of the Output System in a Direction Central.

2. Circuit Differences, Output Control Element

The operation of the output control element, as discussed in this Student Text is also applicable to the AN/FSQ-8 output control element. However, all references to the G/A-TD mentioned in this part should be disregarded. Circuit differences evident in the discussion of the output control element (AN/FSQ-7) and common to the AN/FSQ-8 output control element are discussed in the following paragraphs.

a. Flip-Flop Register Clearing

The temporary storage period of the Flip-Flop register is controlled by the Flip-Flop-clear (reset) pulse generated in the driver section of the parity register and drivers. The controlling factors for the application of the clear pulse are shown in Figure 5-2. The clear pulse is a gated OD 4 timing pulse passed through a 0.4-usec delay circuit. The clear pulse is then applied through separate lines to the left drum and parity registers and the right drum word register. The clear time is thus established at OD 4 + 0.4 usec.

The drum word is received from the OB field at OD 1 time plus the delay introduced by the connecting cable. The cable delay depends on the length of cable used and may be as great as 0.5 usec.

Since OD 4 is 7.5 usec after OD 1 (2.5 x 3), OD 4 + 0.4 occurs approximately 8.0 usec after the time that the drum word is received. Hence, the flip-flop register is cleared approximately 8.0 usec after it is set by the drum word.

The application of the clear pulse is a function of the presence of the not-error-signal level at the gate. This pulse is always present during normal operations and is removed only for testing purposes.

The inhibit reset signal from the unit loop control circuit (a test function) energizes a relay, causing the normally closed contact to open. This action prevents the right drum word register from being clear but has no effect on the passage of the left-drum-word-register clear pulse.

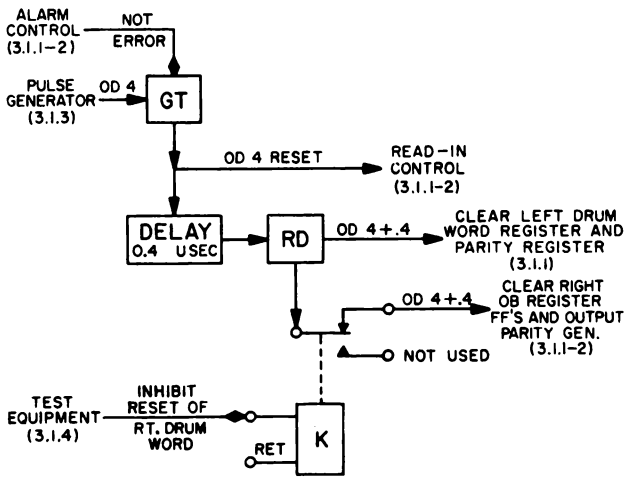


Figure 5-2. Flip-Flop Register Clear Control (3.1.1), Simplified Logic Diagram

To summarize, the registers are always cleared 8.0 usec after a word is entered into the registers during normal operations. Only during test operations is it possible for the drum word to remain in the registers longer than this period. Thus, during testing, a drum word may be retained for longer than the normal time interval when test operations require this condition.

The OD 4 reset pulse, shown in Figure 5-2, is gated into the read-in control circuit when a word is missed. It then becomes a nonsearch signal to the output alarm section and the Central Computer. The OD 4 pulse is used since it occurs at a time sufficiently later than the time of entrance of the word (OD 1) to permit complete examination of the word.

b. Output-Word Parity Generator

Since the drum word does not remain intact beyond the output control element, the drum-word parity cannot be used for further parity checking. Therefore, a new parity bit is generated, added to the right drum word, and transmitted with it to the telephone receiving terminals. This permits another parity check to be conducted at that point (i.e., at the terminals) for detection of possible telephone channel errors. Unlike drum-word parity, the output parity bit is even; that is, the total number of 1's in a correct output word, including the output parity bit, is even.

The parity gates used to test drum-word parity are also instrumental in generating the output parity bit. The output-word parity generator flip-flop, shown in Figure 5-3 is initially cleared by the flip-flop register clear control and is therefore set with the 0 side up before the new word is entered into the flip-flop register. The output word parity generator is then set with the 1 side up only if the new right drum

word produces the odd-parity pulse shown in Figure 5-3. This pulse comes from the odd line of the parity gates associated with the RS bit of the right drum word. Hence, the pulse comes only if there is an odd total of 1's in the right drum word. It follows that an output word parity bit is generated whenever the right drum word is of odd parity. The output word parity bit, when added to the output word through the STD's makes the total number of 1's even. If the right drum word has an even total of 1's, there is no pulse to the 1 side of the flip-flop. Hence, the flip-flop remains with the 0 side up and there is no parity bit added to the right drum word. Since in this case, the right drum word must have originally had an even total of 1's, it still has an even total of 1's.

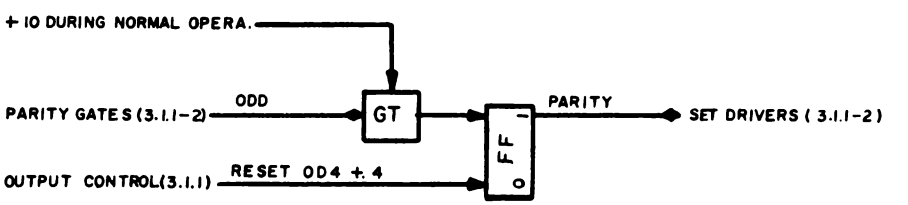


Figure 5-3. Output Parity Generator (3.1.1-2), Simplified Logic Diagram

3. Circuit Differences, Output Storage Element

The operation of the output storage, as discussed previously, of this proficiency guide is also applicable to the AN/FSQ-8 output storage element. However, all references to the G/A-TD mentioned in this part should be disregarded.

4. Circuit Differences, Test Equipment Section

The operation of the test equipment section in the AN/FSQ-8 output system differs greatly from that of its AN/FSQ-7 counterpart. This difference is attributable to the variance in circuit applicability or function and the test procedural methods used to perform test functions (unit loop or computer loop tests) on the AN/FSQ-8 output system. A discussion of the operation of the test equipment section in an AN/FSQ-8 output system is presented in the following paragraphs.

5. Introduction, Test Equipment Section

The output test equipment section is incorporated in the output control element of the Output System for the purpose of testing the circuit functioning and the logical operation of the Output System. The test equipment consists of switches, relays, and logic circuits. Also, certain of the neons and indicator lamps of the output alarm section operate with the output test equipment section. The various switches, neons, and lamps are located on the output system test panel, which is mounted on the back of unit 42. (See Figure 4-1.)

Two basic types of tests are provided by the test equipment: the unit loop test and the computer loop test. Each loop test involves the feedback of test information to its origin, where a comparison is made to ascertain whether the test information was correctly transmitted. The unit loop test is performed manually by means of switches, whereas the computer loop test is programmed and is therefore performed automatically. The unit loop test checks the operation of the various individual sections of the output system while the system is isolated from the remainder of the Combat Control Central. The computer loop test provides a means of checking the Output System in conjunction with a large portion of the Combat Control Central.

6. Unit Loop Test

a. General

In the unit loop test, the Output System is isolated from the Drum System, and a test word is then inserted manually by means of switches. The test word is processed in the normal manner by the output control element. If the conditions for its acceptance have been fulfilled (parity OK, burst number compares, no illegal addresses, and search time up), the word is transferred in the normal manner to the selected storage section in the output storage element. The word is then processed through this element. For the G/G storage section, the output data (right drum word) is looped back into the output control element flip-flop register, where the word was originally entered. If the transfer was unsuccessful, one or more of the output alarm section flip-flop register neons will be illuminated. (See Figure 5-5.) Besides this visual representation, the test equipment section indicates an error in one of several other ways. For the TTY storage section, the output word is recorded on a TTY monitor. This data is then visually compared with the test contents of the flip-flop register to determine whether an error has occurred.

The unit loop test procedure may be divided into three basic circuit groupings; unit loop control, unit control circuits control the general flow of the test word through the output control element and the output storage element and provide the processing operation for detecting an error. The unit loop storage circuits provide for the storage of the test word in the test equipment section. The unit loop test circuits control the specific test operations in the storage section of the output storage element during testing operations.

b. Unit Loop Control, Error Detection

The general process of error detection involves the manual setting in of a test word in the flip-flop register and the processing of this word to determine whether any errors occur. The test word is processed through the output control element in the normal manner and transferred to the output storage section. From there a G/G word goes to the unit loop control circuits. A TTY word, on the other hand, is sent not to the unit loop control circuits, but to a TTY monitor.

(1) Unit Loop Test Switching

The operation of the Output System during testing is controlled by relays, which are in turn controlled by switches. These switches are located on the panel on the test doors on the back of the output control unit.

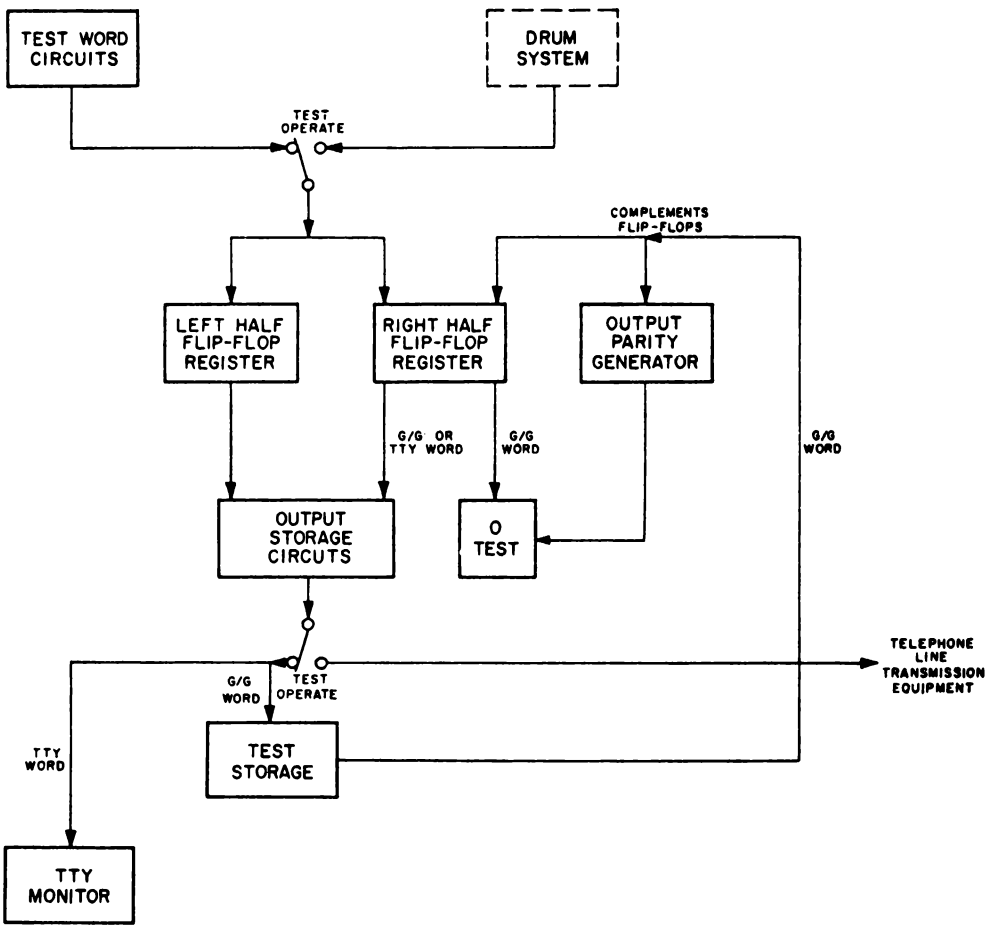


Figure 5-5. Unit Loop Test Data Flow, Block Diagram

Any kind of a test on the Output System disables it thereby disabling the operation of the entire Central. Therefore, an interlock (controlled at the maintenance console) is necessary to prevent inadvertently starting a test during the processing of an air defense problem. This interlock is accomplished by switching the relay voltage supply for the test equipment section at the maintenance console. Thus, the OPERATE-TEST switch on the maintenance console sends a computer-test signal to the unit-loop-on-test circuit of the unit loop control. (See Figure 5-6.) This signal controls the relay voltage supply for the output test equipment section and is sent via computer loop control circuits since a computer loop test takes precedence over a unit loop test. Hence, control over whether a unit loop test can take place depends upon whether a computer test is in progress.

A unit test pushbutton (S8, Figure 5-6) in the test equipment section causes a holding relay to close, which controls the output test relay voltage (the output on-test signal) of the test circuits. The end unit test pushbutton (S7) breaks the voltage to the holding relay at the end of the test operation.

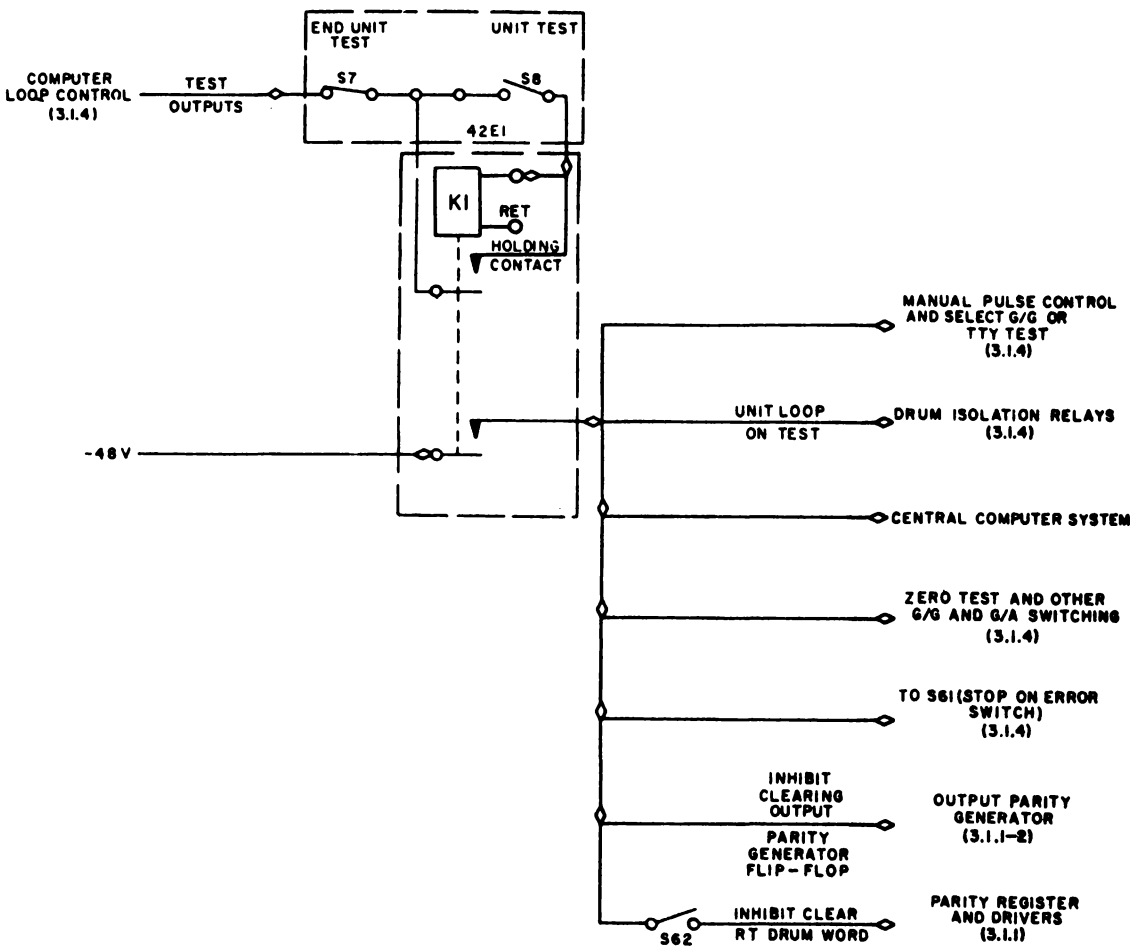


Figure 5-6. Unit-Loop-on-Test Test Circuit (3.1.4), Simplified Logic Diagram

(2) Drum Isolation and Test-Bit Circuits

To set in a test word, the flip-flop register of the output control element must be isolated from the Drum System. After this is done, the test word can be set into the flip-flop register.

As shown in Figure 5-7, the unit loop test circuit supplies the relay voltage to 33 relays, each of which opens one of the 33 bit lines from the Drum System.

The test word generator of the output test equipment provides a standard test-word pulse equivalent to a 1 bit to each of 33 gates. Each gate is connected to a read-in test-word switch corresponding to each of the 33 bits which make up a word. When a switch is closed, a +10v level conditions the corresponding gate which passes the test-word pulse. This sets the 1 side of the corresponding flip-flop in the flip-flop register up. Therefore, by closing the appropriate switches, 1's are read in to make up a

drum word. (It follows, of course, that the flip-flops associated with the read-in test-word switches left open are set with the 0 side up.)

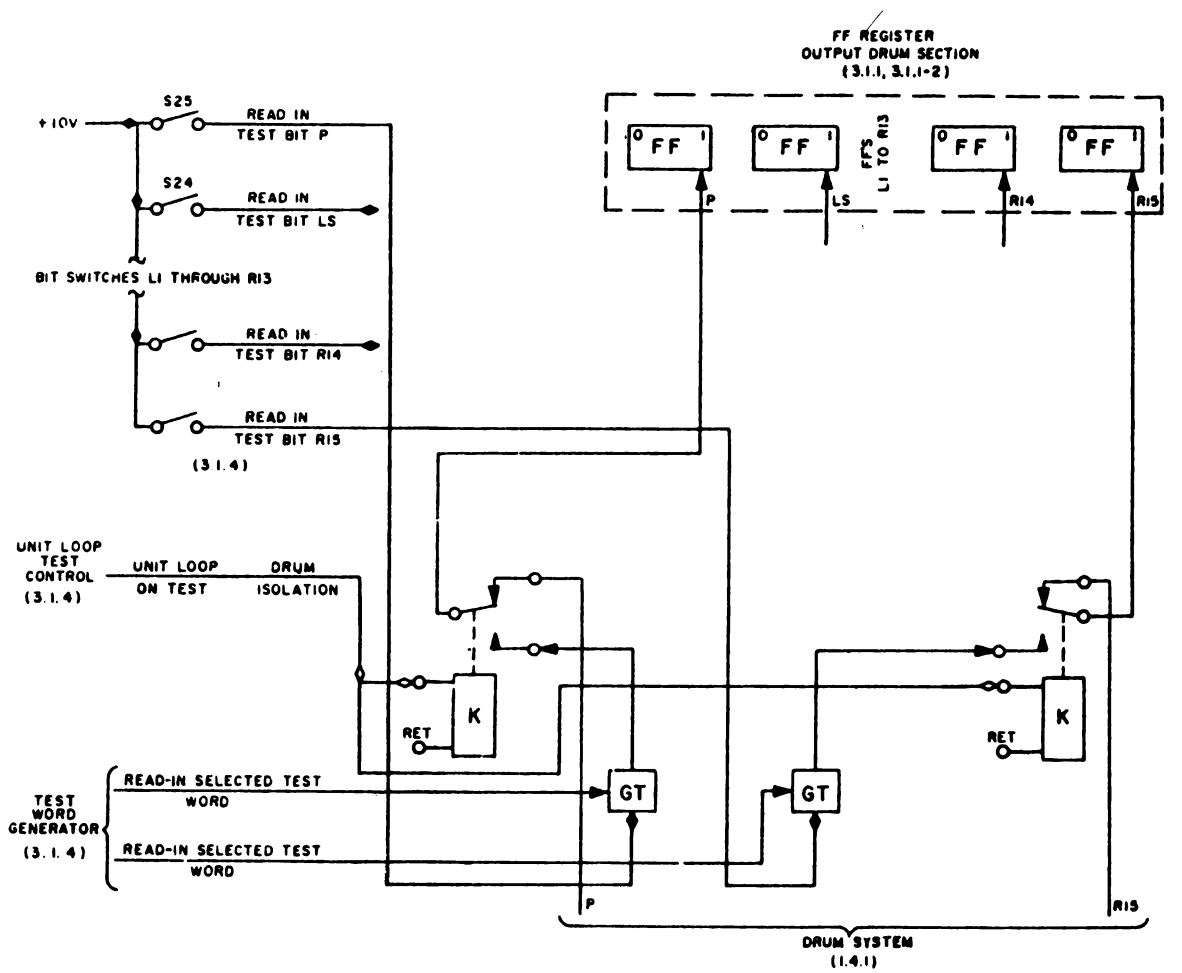


Figure 5-7. Drum Isolation and Test-Bit Circuit (3.1.4), Simplified Logic Diagram

When setting in a test word for G/G, the right drum word (bits RS through R15) may be set to any desired combination of 1's and 0's. For TTY, restrictions must be considered. The burst number, bits L8 through L15, must be all 0's since the burst counters in the output storage element are inhibited. The desired register address in the array of the selected section, designated by bits L3 through L7, is set according to the register address code; the desired section address, designated by bits LS through L2 is set according to the section address code. Care must be taken not to set in an unassigned section or register. The parity bit, P, must reflect a manual parity count of the 32 other bits so as to produce odd parity for all 33 bits.

(3) Inhibit Resetting of Right Drum Word

Under normal operation, the parity drivers of the output control element clear the flip-flop register 7.9 usec after the word is entered. However, during test operations, the right drum word should remain in the flip-flop register until it is complemented by the completely processed, looped-back word for G/G tests, or visually compared with the TTY monitor for TTY tests.

The clearing of right drum word registers is prevented by closing INHIBIT RESET RIGHT DRUM WORD switch S62. This transfers the -48v relay level passed by the unit test relay (K1, Figure 5-6) to the relay in the parity register and drivers (Figure 5-2) that controls the application of the clear pulse. The opening of this latter relay prevents the clear pulse from being passed to the right drum word flip-flops and also the output parity generator flip-flops (Figure 5-3). The clearing of the left drum word and input parity bit is not prevented since only the message portion of the drum word (right drum word) and the output bit arrive at the output of the output storage element. Therefore, only this (the right) portion of the drum word is looped back to the flip-flop register for comparison purposes.

(4) Clearing Alarms and Resetting Flip-Flops

Before the test operation is begun, all alarms and flip-flops in the Output System should be cleared by depressing the CLEAR ALARMS AND RESET FLIP-FLOPS switches (S5 and S6). This action grounds the pulse generators in the pulse distributor circuits of the output computer section. Clear pulses now pass to the appropriate circuit.

(5) Test Start Control

Before a unit loop test is started, the previous basic switch settings must be made. Then, specific switch settings must be made, depending upon the storage section (G/G or TTY) selected. Also, the method of error detection is selected. If the STOP ON ERROR switch is engaged, the test should be started by depressing START CYCLE pushbutton S2. As shown in Figure 5-8, this action grounds the pulse generator which produces a pulse to clear the single-cycle output flip-flop and the master flip-flop. This latter flip-flop produces an enable OD level, which then causes the various OD pulses to be distributed by the output computer section. This action sets the circuits into operation. Also, the start pulse is sent to the 1,300-pps generator to clear its flip-flops at the start of the test.

If the STOP ON ERROR switch is not engaged, the OR circuit following the master stop flip-flop has a +10v level on it at all times. In this case, the enable-OD-signal level is always present and the Output System is continuously cycling. Under this condition the test is always in progress, even while the test word is being entered. Therefore, the START CYCLE button has no significance.

(6) Transfer of Word from Output Storage Section to Test Circuit CSR.

After the test word that has been entered is processed in the normal manner by the output control element, it is passed to the selected output storage section. The G/G word is transferred from the output storage section back to the test equipment circuits after it leaves the output shift register (OSR) of the selected storage section.

A TTY word is not returned to the test equipment circuits, but is passed to a TTY monitor. Hence, the discussion that follows applies only to G/G words.

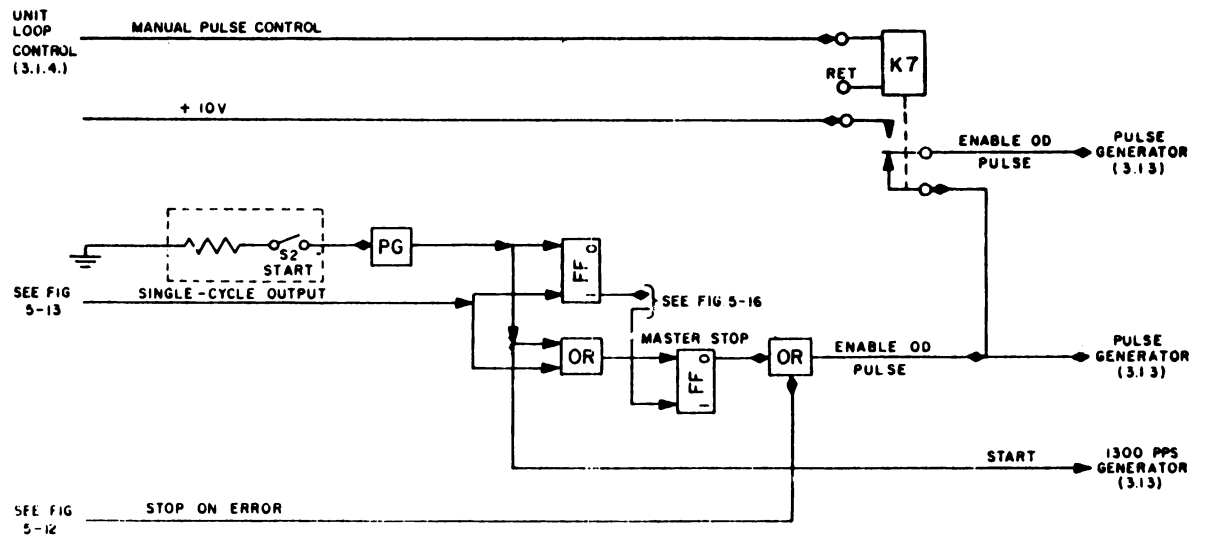


Figure 5-8. Test Start Control Circuit (3.1.4), Simplified Logic Diagram

Since only one word is read into the selected output storage section array, the bits are shifted serially out of the OSR at a comparatively slow rate. A data-sample level is produced each time a bit of G/G word is read out of the OSR. As shown in Figure 5-9, when a bit is read out of the OSR, the produced data sample level conditions GT's 1 and 2. The G/G test-data pulse is passed by the conditioned GT 1 and sets the test data pulse stretcher flip-flops. The test-data pulse is generated only when a 1 bit is read out of the OSR and arrives at time OD 3-13. Since the flip-flop is cleared at OD 1, the core prime receives a 5.0 usec pulse for each 1 bit in the test word. The core prime then primes the first core in the test core shift register (CSR) for each 1 bit in test word. At the same time that GT 1 is conditioned by the data-sample level, GT 2 is also conditioned by this level. (See Figure 5-9.) Gate 2 passes the OD 3-13 pulse as an enable-high-speed-shift pulse, which sets the 1 side of the test shift control flip-flop and also pulses the core shift driver (CSD). The CSD shifts to the second core the bit set into the first core by the core prime, and so on down the line. Hence, it can be seen that the test shift control flip-flop (and related logic) pulses the CSD of the CSR every 1/1,300 second, immediately after the core prime is either primed by a 1 bit in the test word or left unprimed by a 0 bit in the test word. This priming (or lack of priming), followed by a shift, continues until the complete test word is serially entered into the test.

(7) Data-Sample Level Generator

As part of the specific operations performed when making a G/G test, TEST switch S50 is set to the G/G position. Naturally, the switch position must agree

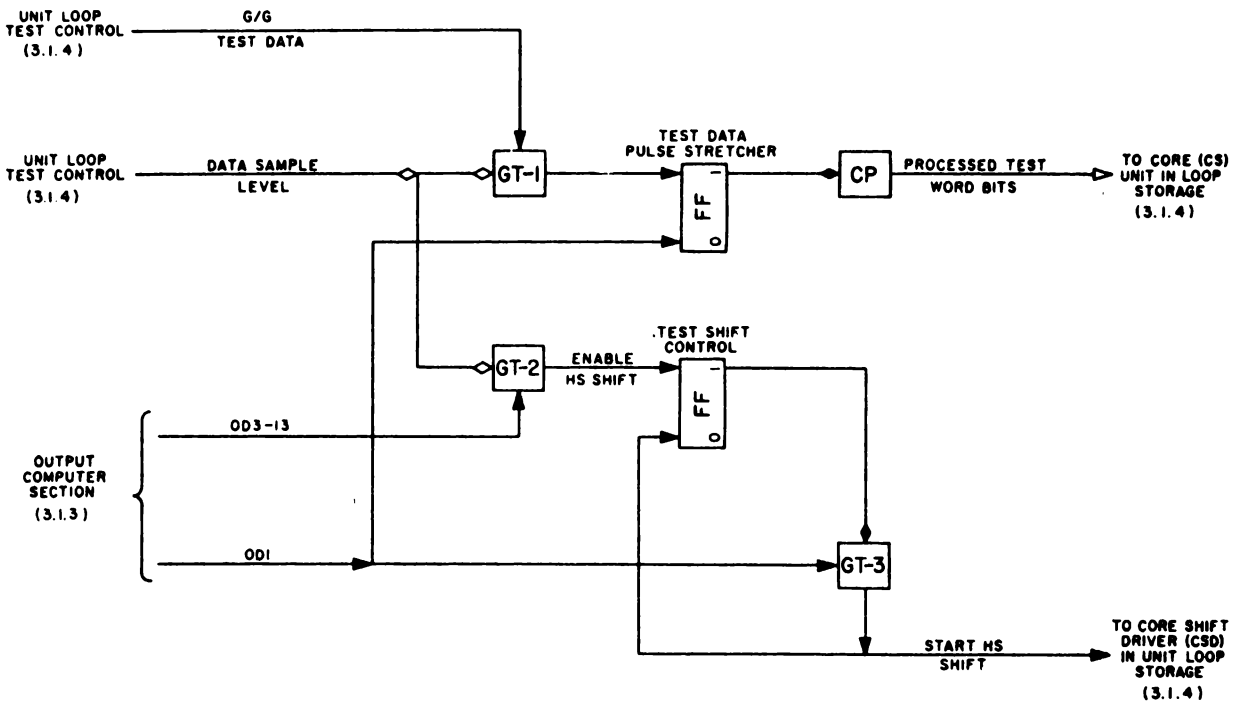


Figure 5-9. Test Core Shift Control Circuit (3.1.4), Simplified Logic Diagram

with the section address set into the test word. If G/G is selected, the G/G SELECT REGISTER 0-4 pushbutton (S44, Figure 5-10) is depressed the number of times necessary to cause stepper switch S1 to move to the position that corresponds to the register address set into the test word. The position of the stepper switch corresponds to the interleaving of the information in the output channels (slots). Hence, register addresses 0, 5, 10, 15, and 20 are read out of the OSR at the same time; register addresses 1, 6, 11, 16, and 21 are read out at the same time, etc. Therefore, the 25 register addresses in the G/G storage section are read out in groups of 5 by five different timing pulses, which occur at times 5-counter-equals-1 through 5-counter-equals-5. Hence, there must be five positions of the stepping switch corresponding to these five timing pulses. These positions are 5CSR 1 CORE through 5CSR 5 CORE. Indicator lamps reveal which position the switch is in. The stepping switch is set to the position that corresponds to the register address set in the test word.

On the 5 CSR line that corresponds to the register address in the test word, a level occurs at the same time that a bit is being read out of the OSR. By having relay K2 de-energized and the stepping switch in the correct position, the level is passed through K2 as the data-sample level.

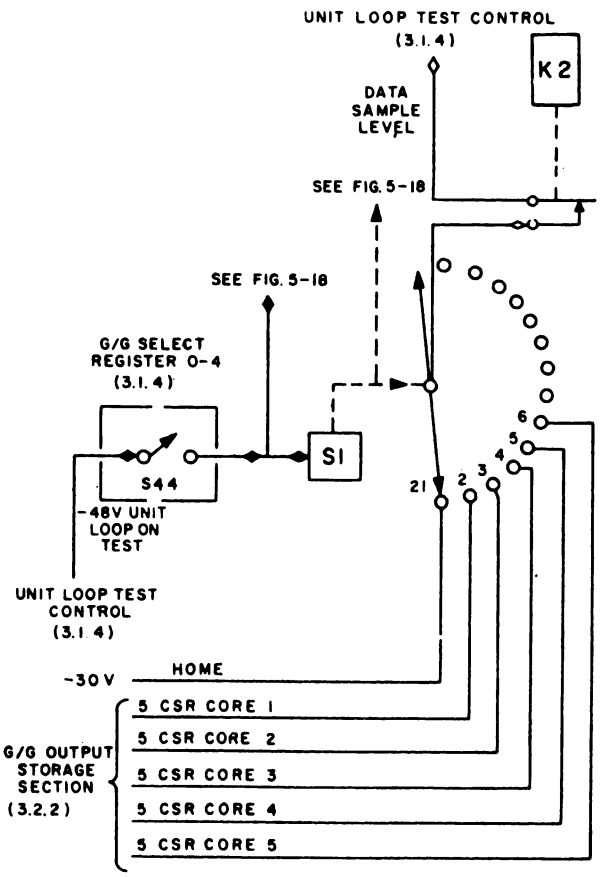


Figure 5-10. Data-Sample Level Generator (3.1.4), Simplified Logic Diagram

(8) Test-Data Pulse Generator

As shown in Figure 5-11, when the unit loop test is begun, the unit-loop-on-test signal level is sent to K1. The closing of this relay connects all G/G data lines 1 through 5 to a common output line. The data lines correspond to the channels (slots) in each storage section, and the register address of the G/G word corresponds to one of the data lines. A pulse is produced on the appropriate data line whenever a 1 bit in the test word is read out of the OSR. Hence, a pulse appears on the common G/G test data line for each 1 bit in the G/G test word, regardless of the register address of the word. The appropriate switch (S56 through S60) must be thrown that corresponds to the slot which includes the assigned register address.

(9) Error-Detection AND Circuit

When the complete test word has been read into the test CSR, a test-transfer pulse initiates a synchronizing cycle which results in the sampling of each core in the register. Each core containing a 1 bit sends a complementing pulse back to

a particular flip-flop in the flip-flop register of the output Drum System. This flip-flop would be the corresponding right test word flip-flop into which the bit was originally entered. If, in a particular right word flip-flop, the original bit entered was a 1 and the complementing bit is (correctly) also a 1, the flip-flop is complemented with the 0 side up. If, in a particular right word flip-flop the original bit entered was a 0 and the complementing bit is correctly a 0, the flip-flop has the 0 side up. However, if the original bit is a 1 and the complementing bit is (incorrectly) a 0, or if the original bit is a 0 and the complementing bit is a 1, the flip-flop is complemented with the 1 side up.

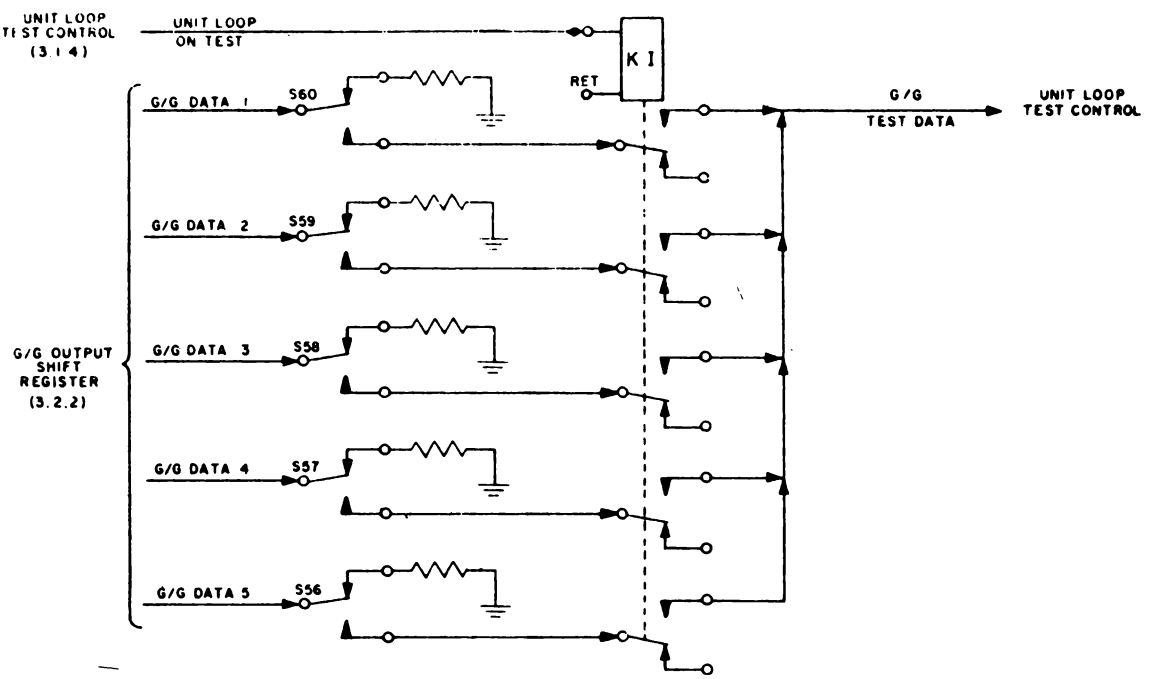


Figure 5-11. Test-Data Pulse Generator (3.1.4), Simplified Logic Diagram

As shown in Figure 5-12, the 0 side of the 16 right word flip-flops of the flip-flop register and the 0 side of the output parity bit generator flip-flops are fed to the 68-way AND circuit. If none of these bits has been erroneously changed from 0 to 1 or from 1 to 0 during the processing through the Output System, the complementing of the flip-flops should reset the 0 sides of all the flip-flops. The 68-way AND circuit conducts. The inverter then blocks any further passage of the signal level. However, if one (or more) of the flip-flops is complemented with the 1 side up, which would happen if an error occurred in the processing of the test word, the AND circuit would not conduct.

The inverter then passes a level to the OR circuit which conditions a gate. The "O" TEST switch (S49) has been thrown to the G/G position. This passes the unit-loop-on-test signal level to a relay (K4) in the unit loop storage section. This relay closes and passes a 19-counter-equals-19 pulse, for a G/G word, to the gate

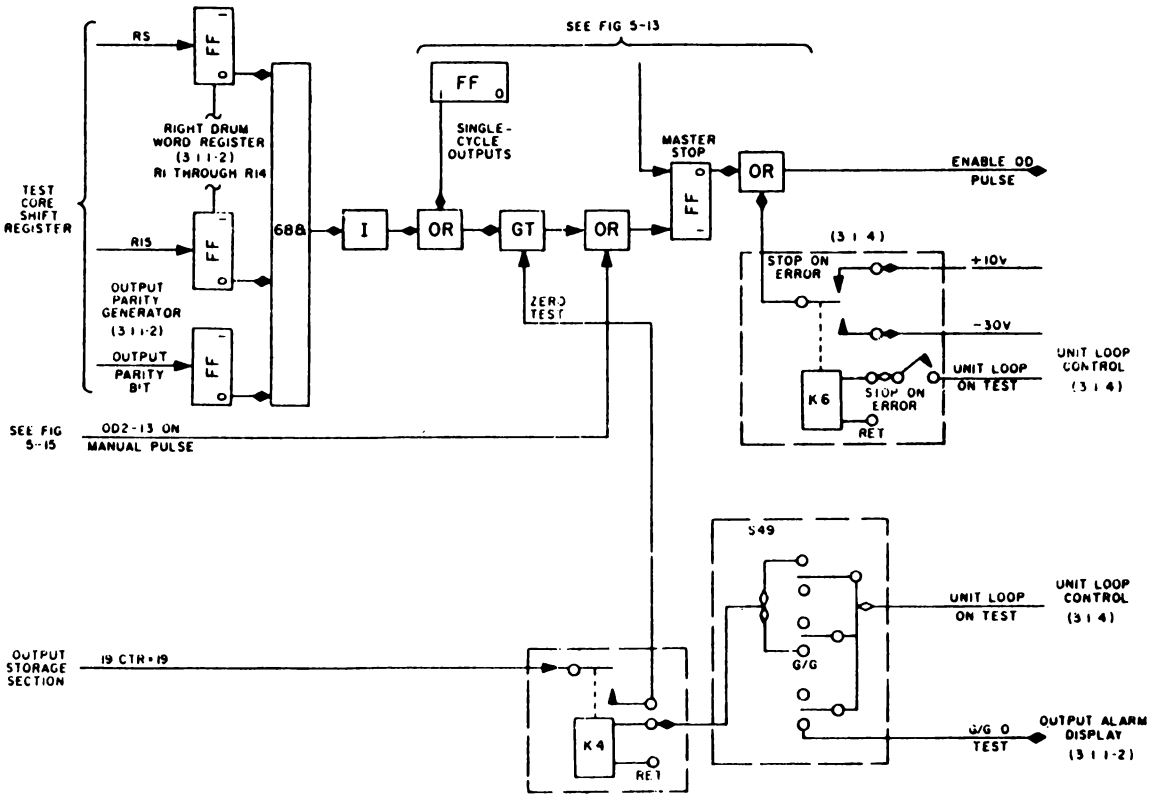


Figure 5-12. Error Detection Circuit and Master Stop (3.1.4), Simplified Logic Diagram

shown in Figure 5-12 as a zero-test pulse. These pulses occur at the end of readout time in the respective sections and therefore arrive after the complete processing of the test word. If the gate is conditioned as a result of an error in the processing of the test word by the Output System, the gate passes the zero-test pulse. This sets the 1 side of the master stop flip-flop. Two actions can take place. If the STOP ON ERROR switch (S61) has been thrown, the unit-loop-on-test signal level is passed to K6, passing a -30v level to the second OR circuit. As a result, the enable OD-pulse signal level is produced only if the 0 side of the master stop flip-flop is up. Since an error causes the 1 side of this flip-flop to be up, the enable OD level is cut off and the test stops. If the STOP ON ERROR switch is not thrown, the OR circuit receives a +10v level instead of the -30v level. Therefore, regardless of whether the 68 AND circuit detects an error, the enable-OD-pulse level remains up and the test operation cycles continuously without stopping. However, neons that are not shown in Figure 5-12 light if a flip-flop is not correctly complemented; these neons indicate the presence of an error.

(10) Optional Operation Control Circuits

The previous paragraphs described the cyclic mode of operation of the test circuits. It was noted that the test word cycles continuously and stops only if the

STOP ON ERROR switch is thrown and there is an error in the processing of the test word. There are two other possible modes of operation; the single-cycle mode and the manual-pulse mode. In the single-cycle mode, the test word makes one complete cycle through the system each time the SINGLE CYCLE OUTPUT button is depressed. In the manual-pulse mode, the test word completes one step in the loop cycle each time the MANUAL PULSE button is depressed. For either of these tests, the STOP ON ERROR switch must be engaged to provide a -30v level at the OR circuit following the master stop flip-flop. (See Figure 5-12.) If this is not done, the normally present +10v level in this OR circuit will at all times pass an enable OD pulse signal level. Under this condition, the single-cycle or manual-pulse test cannot be performed since the test word will just keep cycling continuously.

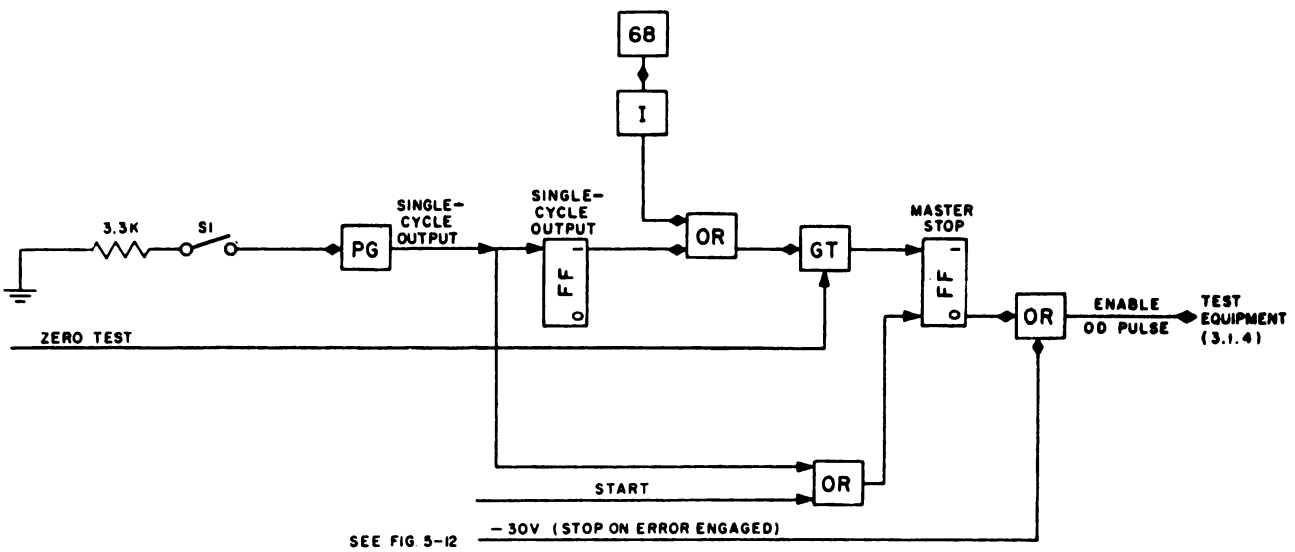


Figure 5-13. Single-Cycle Control Circuit (3.1.4), Simplified Logic Diagram

(11) Single-Cycle MODE

As shown in Figure 5-13, when the SINGLE CYCLE OUTPUT button is depressed, the single-cycle output pulse generator passes a pulse to the master stop flip-flop. This sets the 0 side of this flip-flop and produces an enable-OD-pulse signal level which causes the unit loop cycle to begin. The single-cycle output pulse also sets the 1 side of the single-cycle output flip-flop up. This conditions the zero test gate, which passes a pulse at 19-counter-equals-19 time, as previously described. This sets the master stop flip-flop, which cuts off the enable-OD-signal level. Hence, the Output System stops, and one complete cycle of the test word has been made.

To switch to a continuously cycling mode of operation, the START CYCLE pushbutton is depressed.

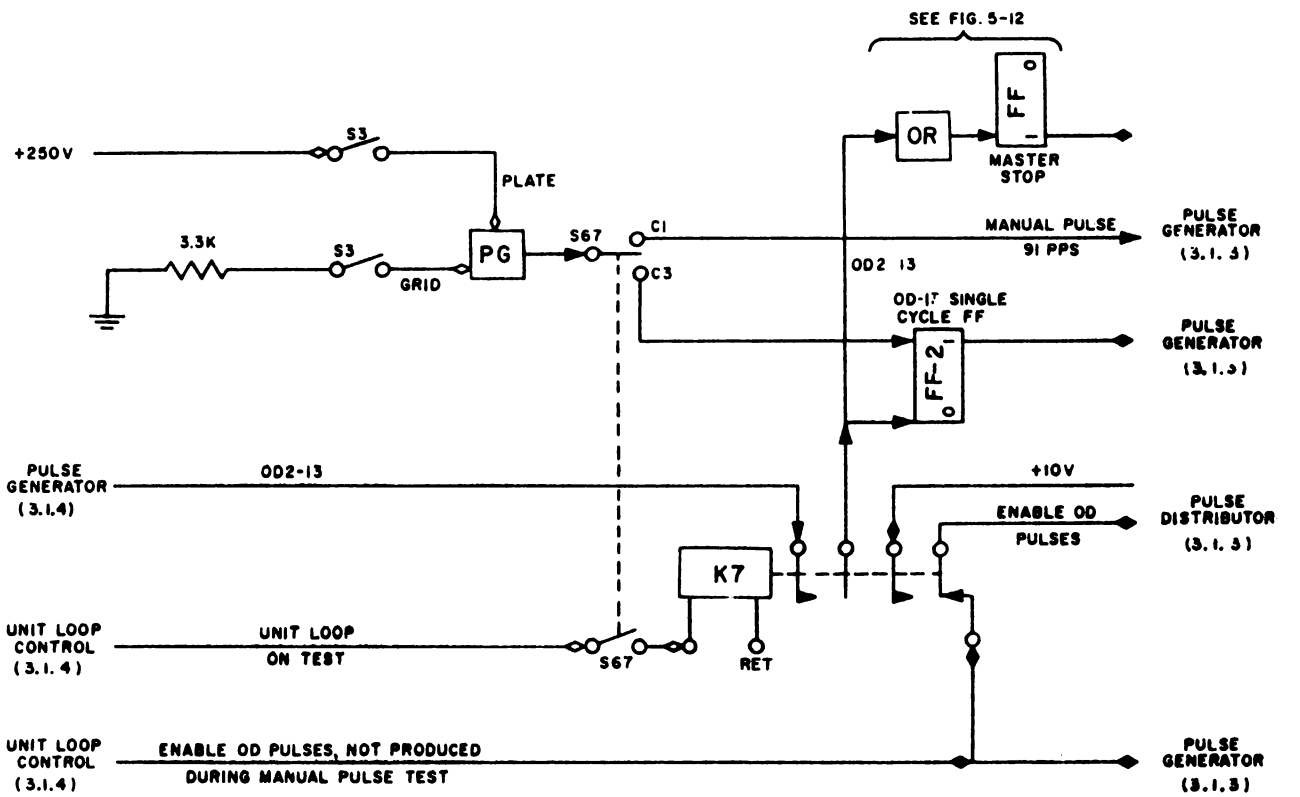


Figure 5-14. Manual Pulse Control Circuit (3.1.4), Simplified Logic Diagram

(12) Manual-Pulse Mode

The manual-pulse mode consists of two distinct phases; the manual-pulse 1,300-cps mode for G/G and the manual-pulse 91-cps mode for TTY. The two modes are very similar.

If the manual-pulse 1,300-cps mode is selected, the MANUAL PULSE CONTROL switch is moved to 1,300. As shown in Figure 5-14, this puts switch S67 in position C3 so that, when the pulse generator produces a pulse, it goes to the OD 13 single-cycle flip-flop of the OD 13 generator. In the other position of the switch, the pulse goes to the OD 91 pulse generator. For either position of S67, the unit-loop-on-test level is passed to K7 to close it. (See Figure 5-14.) An OD 2-13 pulse is transferred through K7 to the OD 13 single-cycle flip-flop. This pulse also goes to the 1 side of the master stop flip-flop to cut off the enable-OD-pulse signal level.

A +10v level is passed as the enable-OD pulse to the pulse distributor since the enable OD pulse is not produced. (Figure 5-8.) The manual pulse takes the place of the enable-OD pulse shown in Figures 5-8 and 5-12 (Figure 5-12). When the MANUAL PULSE pushbutton (S3) is depressed, the pulse generator produces a pulse which sets the OD 13 single-cycle flip-flop or OD 91 single-cycle flip-flop up.

The 1,300-cps oscillator turns on the OD 13 start flip-flop (FF 1, Figure 2-39) and one set of OD pulses (OD 2-13, OD 3-13, and OD 4-13) is generated (Figure 2-39). The OD 2-13 pulse resets the OD 13 single-cycle flip-flop, and no further pulses are passed. Hence, the MANUAL PULSE pushbutton allows OD 91 pulses for a TTY test or OD 13 pulses for a G/G test to be applied at a controlled rate. Thus, each step taken in the output storage element may be examined for sources of possible errors.

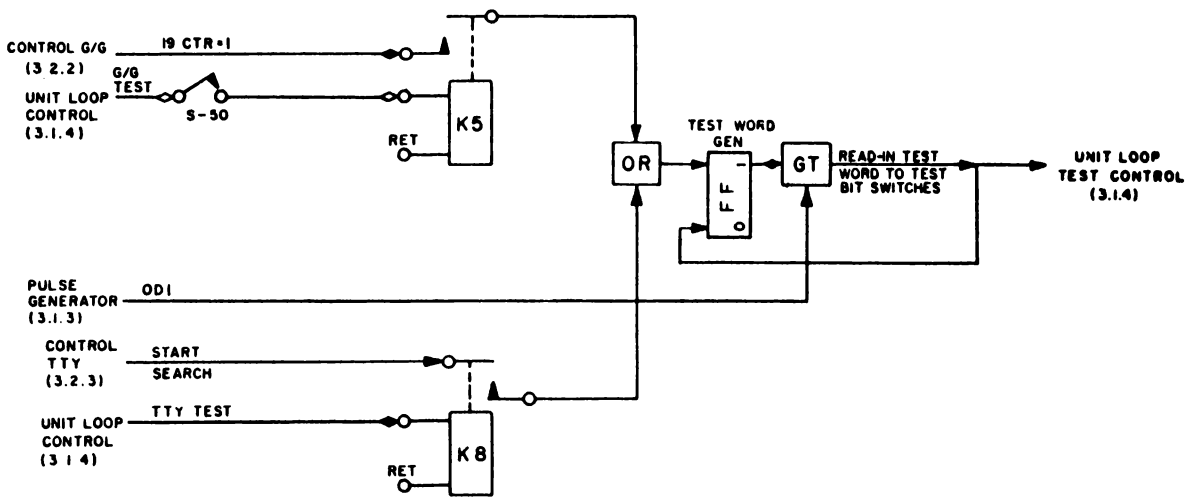


Figure 5-15. Test Word Generator (3.1.4), Simplified Logic Diagram

c. Unit Loop Control, Test Word Generator

The test-word generator (Figure 5-15) produces a pulse for each 1 bit selected for the test word. The test-word pulse is generated in the following manner: An OR circuit passes either a 19-counter-equals-1 or a start-search pulse to the test-word generator flip-flop, depending on whether a G/G or TTY test has been selected. The G/G pulses occur at the start of a readout cycle, and the TTY signal is the start-search signal which normally goes to the TTY burst counter. The test-word generator flip-flop conditions a gate which passes an OD 1 pulse as the pulse which produces 1 bits in the selected flip-flop registers of the output control element. Since during normal operations the drum word is entered at time OD 1, the timing of the test word is made to agree exactly with the timing of a normal drum word.

d. Unit Loop Storage

The unit loop storage section is the test CSR previously described. It accumulates the processed test-word bits from the selected section and register of the output storage section. The bits are shifted into the test CSR, which is a series of 17 tape cores (core shifts) in serial form. At the end of the output storage section readout operation, the contents of the core shifts are read out in parallel to complement the corresponding flip-flops in the right half of the flip-flop register of the output control section, where the test word was originally entered.

Since the TTY word is not fed back to the flip-flop register for comparison with the original test word but is, instead, sent to a TTY monitor for a visual comparison, the unit loop storage discussion applies only to a G/G test word.

(1) Parallel Readout Control

When the TEST switch (S50, Figure 5-15) is moved to G/G (the section address assigned to the test word), K5 (Figure 5-16) is energized. For a G/G test, a 19-counter-equals-17 pulse is selected. This pulse occurs just before the last group of like-order bits is read out of the corresponding storage section. (Figure 5-15.) Hence, the pulse occurs just before the last bit is read into the first core shifts.

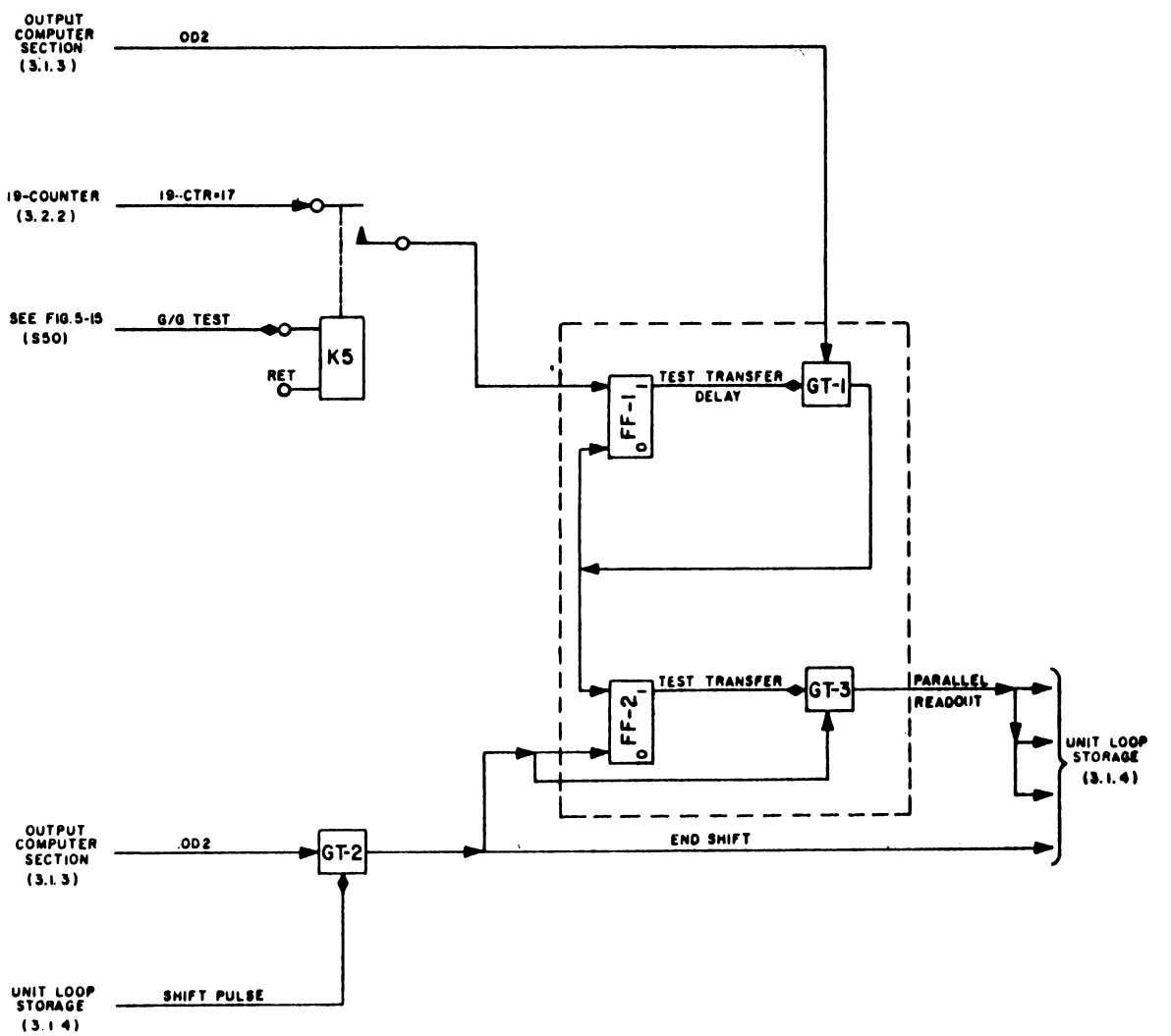


Figure 5-16. Parallel Readout Control Circuit (3.1.4), Simplified Logic Diagram

At the following OD 2 time, the second flip-flop in the parallel readout control circuit is set and remains set until the last bit is received from the output storage element. The last bit is read into the core register, and the high-speed shift takes place. As the shift pulse is ended, the end-shift signal is gated through the parallel readout control circuit to generate the readout pulse. This pulse is carried to the parallel readout gates in the core register circuit to effect the transfer of information to the flip-flop register for comparison.

(2) Core Register Circuit

The core register circuit, shown in Figure 5-17, is a tape-core register of 17 core shifts and is similar to the 19-counter in the G/G storage section. The processed test-word pulse from the storage register control circuit (Figure 5-9) reads the extracted bit into the read-in winding of the first core of the register. (See Figure 5-17.) This read-in occurs for 5.0 usec between OD 3 and OD 1 times. The shift pulse starts at OD 1 with the receipt of the start-high-speed-shift signal from the storage register control circuit. (Figure 5-8.) The start-high-speed-shift signal and the end-shift signal control the shift flip-flop. This flip-flop supplies the shift pulse to the register. The shift pulse lasts 2.5 usec from OD 1 to OD 2. At OD 2 time, following the shift pulse, the former content of each core appears at the output line to the gate circuit at the same time that the bit is being read into the next core. However, there is no transfer through these gates unless they are pulsed by the readout signal. After the last pulse, however, the register is full. The readout signal, which comes from the parallel readout control circuit at OD 2 time and coincides with the end shift signal, is applied to the parallel readout gates, causing the information to be transferred.

When the TEST switch (S50) in the test-word-generator circuit of the unit loop control is in the G/G position, the two relays in the core register circuit are energized, causing the data in bits R8 through R15 to be transferred in unmodified form. Thus, in the parallel readout operation, each bit is directed back to the individual flip-flop of the OB register from which the bit was originally generated.

e. Specific Unit Loop Tests

The preceding paragraphs described the general, common circuitry and processes used in making a unit loop test involving the G/G storage section. The paragraphs that follow describe the particular processes and circuitry unique to that particular storage section. As has been previously mentioned, the output control element functions in the normal manner regardless of the storage section selected.

(1) Ground-to-Ground

The over-all operation of the G/G storage section during a unit loop test is essentially the same as during normal operation, except for a number of minor variations. Since only one word is read into the storage array, there must be some means of synchronizing the operation of the test CSR with the readout of the output shift register of the G/G storage section. In addition, the G/G burst counter must be inhibited. Synchronization is accomplished by using the 19-counter-equals-17 pulse to initiate transfer on the information stored in the test CSR to complement the flip-flop register, using the 19-counter-equals-19 pulse as the zero test, and using the 19-counter-equals-1 pulse in the test word generator.

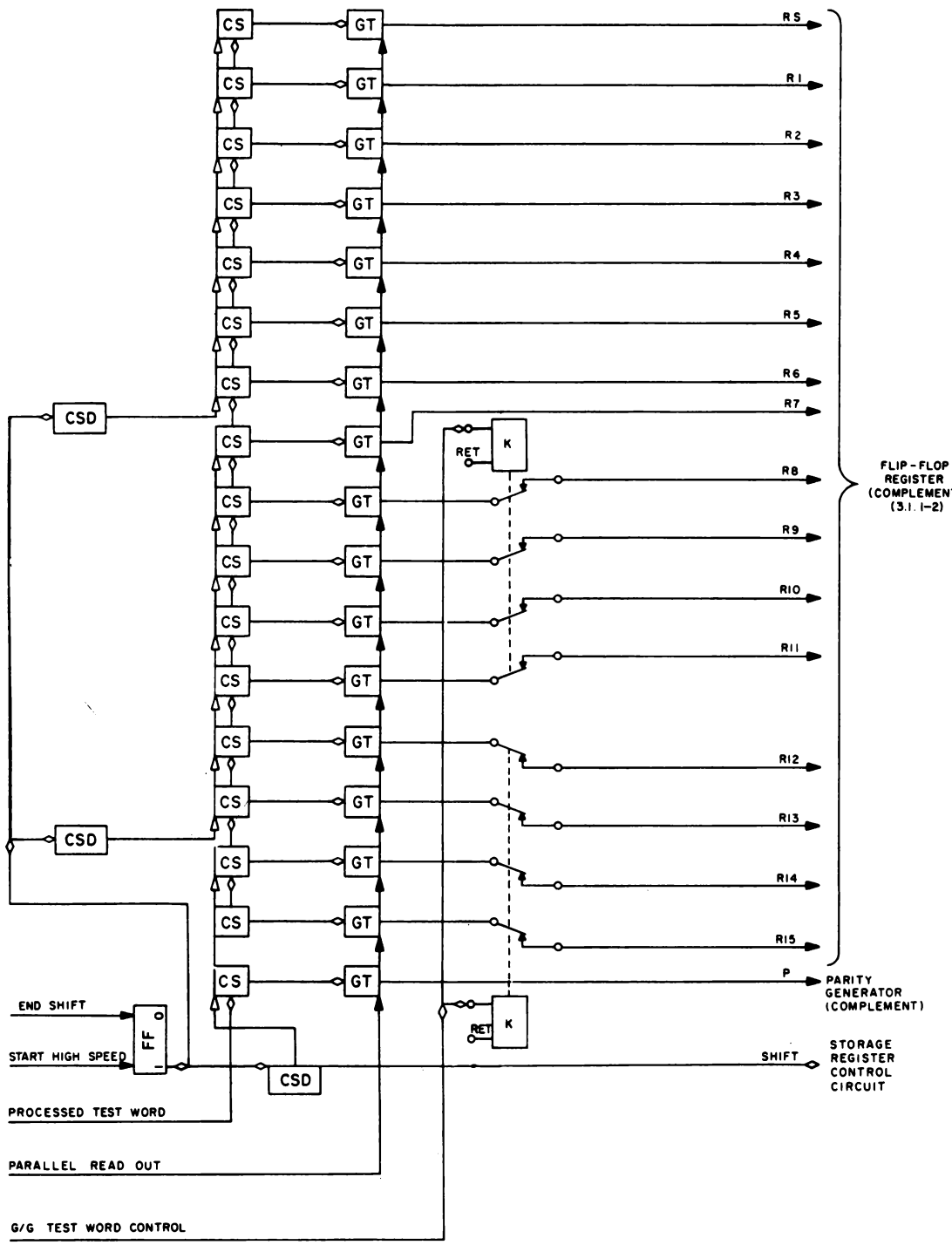


Figure 5-17. Core Register (3.1.4), Simplified Logic Diagram

For a G/G unit loop test, a test word is written into one register in one array during the first 19-counter cycle. During the second 19-counter cycle, the test word is read out of this array while it is being read into the other array. This results in an alternate read-in and readout operation as far as the arrays are concerned. It is possible to select one array and to operate it at twice its normal rate while the other array is idle; that is, a read-in and readout of the same array will occur during each 19-counter cycle.

Test switch S50 selects the storage section and the 19-counter pulses used for the G/G unit test. When the TEST switch (S50) is set to the G/G position, it passes the unit-loop-on-test signal level as an inhibit signal to the G/G burst counter. In addition, the unit-loop-on-test signal level is also sent to a relay in the completed message shift register (CMSR) of the G/G output storage section. This action permits readout after one word has been read into a slot, rather than after the normal number of five words. The output is now taken from the second core rather than from the sixth core of the CMSR.

The register address that corresponds to the address set into the test word is set into the data-sample level circuit by means of stepping switch S1, shown in Figure 5-10. Not all portions of this switch are shown in this figure, the remaining portions being shown in Figure 5-18. As shown in Figure 5-18, bank B of the switch operates indicator lamps to indicate the register address selected each time the stepping switch is depressed. Bank A of the switch is used to return the stepping switch to the HOME position. As seen from Figure 5-18, all the contacts of this bank of the switch are tied together except the HOME position. Hence, when G/G HOME pushbutton S43 is depressed, the unit-loop-on-test signal level is passed to the shorted contacts of bank A of the stepping switch. This causes the switch to step automatically to the HOME position, at which point the signal level is no longer connected. The HOME position is the neutral position of the switch.

(3) Teletype Monitor Test

During testing, the TTY output storage section functions essentially the same as during normal operations. As has been previously described, in the TTY test, the test word is not looped back to the test control circuits and the 17-way AND circuit for a zero test, but is passed to a monitor where a visual comparison is made between the original test word and the processed test word.

When setting up the test word, the procedure is the same as that previously described for the G/G word, except that, for the TTY word, bit RS must be a 1. This is necessary to provide the first busy bit. The remaining bits of the right drum word are selected to represent desired TTY characters.

A particular TTY slot must be selected by using the switches on the duplex maintenance console. Since in the TTY storage section there is one slot for each register address, the slot selected must agree with the register address set into the test word.

As shown in Figures 5-15 and 5-19, when a TTY storage section test is selected, TTY TEST switch S47 is lifted. This passes the unit-loop-on-test signal level

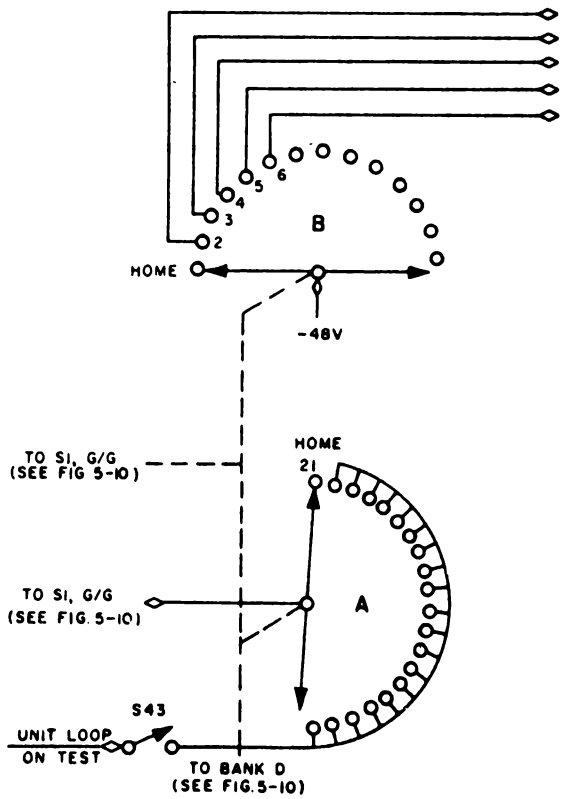


Figure 5-18. Stepping Switch Home Control (3.1.4), Simplified Logic Diagram

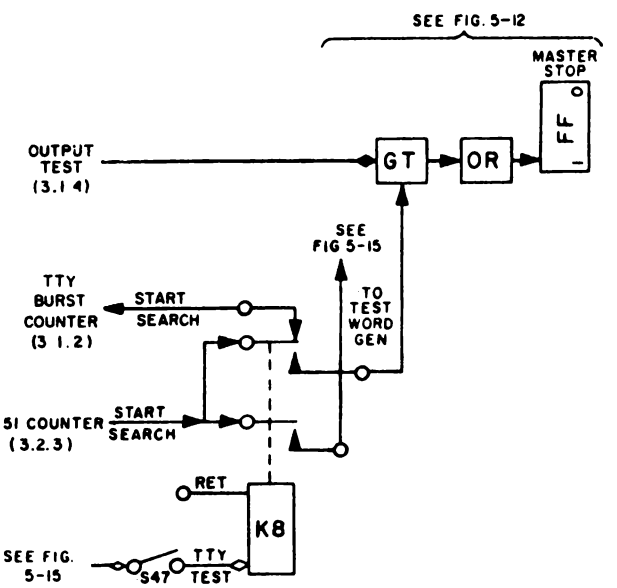


Figure 5-19. TTY Unit Loop Test Control Circuit (3.1.4), Simplified Logic Diagram

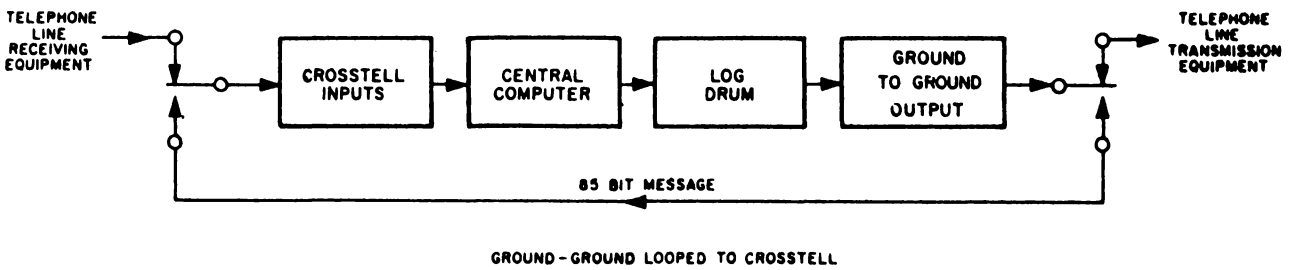


Figure 5-20. Computer Loop Test, Flow of Data, Block Diagram

to K8. As shown in Figure 5-15, the start-search pulse is applied to the test word generator. This action of transferring the route of the start-search pulse inhibits the TTY burst counter, as required. Also, as shown in Figure 5-19, the start-search pulse turns on the master stop flip-flop, which permits single cycling in the TTY test. If an error occurs within the TTY storage section, the TTY parity neon will be turned on.

7. Computer Loop Test

a. General

The computer loop test is a comprehensive check of the input and output circuits of AN/FSQ-8 Combat Control Centrals. It tests the operation of the Output System, Input System, Drum System, and various parts of the Central Computer System itself. During the test, the alignment of the flow of information through the various elements of AN/FSQ-8 Combat Control Central closely approximates the alignment of information flow in the equipment when it is actually processing the air defense problem.

Basically, the output of the G/G storage section is looped through the test equipment section to the crosstell (XTL) input element. Figure 5-20 shows the path of information flow.

The test information originates within the Central Computer System and is passed through the OB fields of the Drum System to the Output System. In the Output System, the test information passes through the G/G storage section and the test equipment section to the XTL element of the Input System, through the XTL field of the Drum System, and back into the Central Computer System for comparison with the original test information.

b. Ground-to-Ground to XTL Input Loop

In the regular operation of AN/FSQ-8 Combat Control Centrals, the output of the G/G storage section is transmitted over telephone to one of the adjacent AN/FSQ-8 Combat Control Centrals. Information enters the adjacent equipment through the XTL input element. The manner in which the information is transmitted, therefore, is compatible with the operation of the XTL input element.

There are five G/G output channels. Each of these channels is capable of being included in the computer loop test, one at a time. Further, there may be several XTL input channels in the XTL input element. Only one such input channel may be used at one time in the computer loop test.

Therefore, to conduct the test, it is necessary to select one G/G output channel and one XTL input channel. The test information is programmed to pass through the Output System and must reflect the channel selection in the address part of the information. The selection and switching of input and output channels is accomplished manually within the computer loop control. Since the information is already compatible, it is switched straight through the computer loop control without any modification. However, it is necessary to manually disconnect the output channel from the telephone line transmission equipment and the input channel from the telephone line receiving equipment. The test information is programmed within the Central Computer System.

c. Teletype Monitor Test

A computer loop test may be performed on the TTY storage section. However, there is no provision for feeding information from the Output System back to the Central Computer. Therefore, a TTY monitor such as is used in the TTY unit loop test is used in the TTY computer loop test.

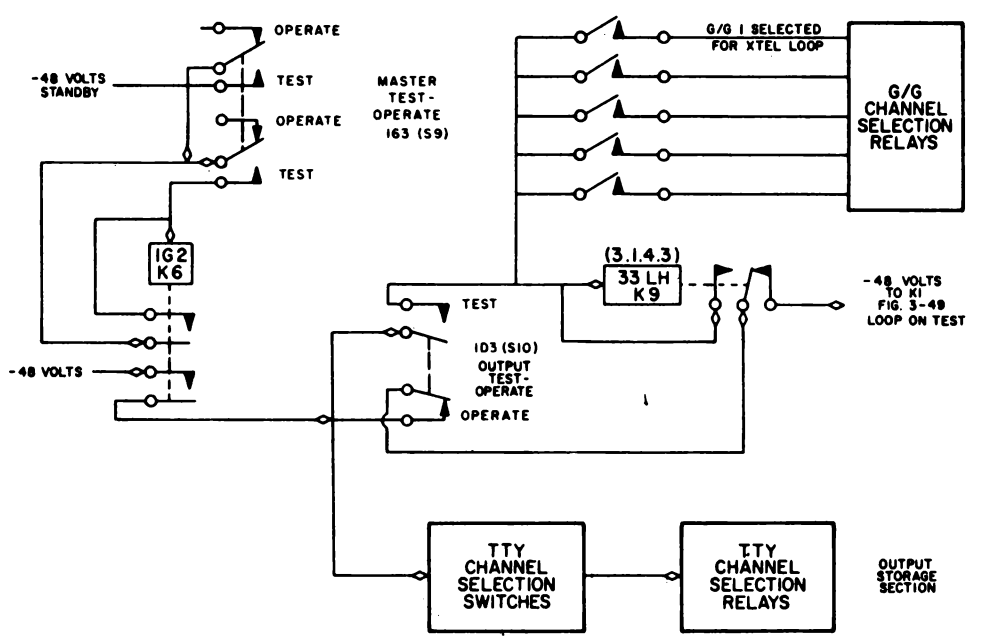


Figure 5-21. Computer Loop Test Relaying and Switching, Simplified Block Diagram

8. Computer Loop Control

a. General

The computer loop control provides some of the circuits for manually switching test information from the selected G/G output channel to the selected XTL input channel. Certain of the switches are included in the Central Computer System.

To place the Output System in a computer loop test, the Central Computer must be in the standby status. The MASTER TEST-OPERATE switch on the duplex maintenance console and the OUTPUTS TEST-OPERATE switch in the Central Computer must be moved to the TEST position. This action supplies relay voltage to the TTY channel selection switches and to relay K9LH, as shown in Figure 5-21. The energizing of K9 cuts off power from K1 (Figure 5-6), which cuts off any unit loop test in progress. Hence, the computer loop test always overrides a unit loop test which may be in progress. The energizing of K9 also provides voltage to the G/G to XTL CHANNEL SELECTION switch in the Central Computer. This allows the desired channel to be selected and connected to the test bus through the relays in the duplex and test switching of the output storage section.

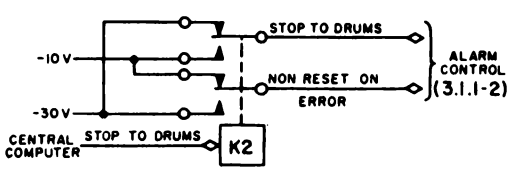


Figure 5-22. Stop-to-Drums Circuit (3.1.4), Simplified Logic Diagram

b. Stop to Drums

As shown in Figure 5-22, when the STOP TO DRUMS switch in the Combat Control Central is turned on, K2 is energized. This sends a -30v level as a nonreset-on-error signal and a +10v level as a stop-to-drum signal level to the alarm control section. As described previously, the -30v nonreset-on-error signal causes the contents of the flip-flop register of the output drum section to be retained for inspection if a parity-NG, an illegal register, or section address alarm is produced during a test. The stop-to-drums pulse is passed to the Drum System if either of the previously mentioned errors occurs. It stops the Drum System and prevents the erasure of the test word so that the error can be examined.

c. Restart to Drum Circuit

At the completion of a test operation, when the OUTPUTS TEST-OPERATE switch is moved to the OPERATE position, the falling of the test-outputs signal generates

a pulse in the restart-to-drums circuit. (See Figure 5-23.) The pulse thus generated sets the restart-to-drums-A flip-flop, which is a synchronizing flip-flop. The restart-to-drums-B flip-flop is set at the following OD 3 time; at OD 1 time, the restart pulse is generated.

The restart pulse is carried to the Drum System and to the parity generator of the output control element. This pulse is used in the Drum System to re-enable the transfer of the information from the OB drum to the Output System. In the output control element, the pulse causes a compare signal to be sent to the Drum System for 100 ms but prevents any words from being accepted during the 100-ms interval. This prevents any old information in the drums from being transferred and causes any such information to be erased from the drums. The 100-ms period is long enough to allow erasure of all three OB drum fields used. The outputs active signal, which arrives when a system is changed from standby to in-use, has the same effect as the test-out signal.

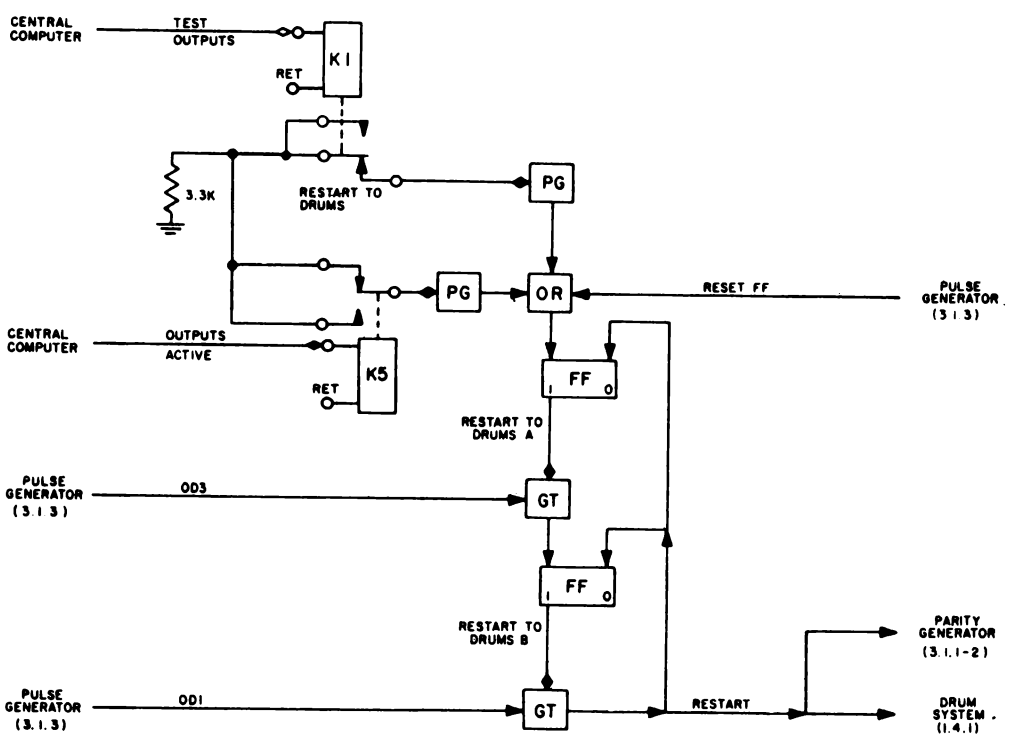


Figure 5-23. Restart-to-Drums Circuit (3.1.1-2), Simplified Logic Diagram