INSTRUCTION BULLETIN

UNCLASSIFIED

BULLETIN NO. 231

64^2 MEMORY MAINTENANCE

64^2 MEMORY PREVENTIVE MAINTENANCE PROCEDURES

July, 1958

MILITARY PRODUCTS DIVISION

INTERNATIONAL BUSINESS MACHINES CORPORATION

KINGSTON, NEW YORK

IBM KINGSTON TECHNICAL PUBLICATIONS

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FOREWORD

The information contained herein has never appeared in any previous publication. It represents the initial step of providing scheduled preventive maintenance checks for the 64^2 memory.

The preventive maintenance checks are functionally divided into two groups; those requiring scoping, and those not requiring scoping such as mechanical, resistance, and voltage checks. It is recommended that all checks be performed in accordance with the schedule provided in the text. This schedule reflects current concepts of equipment requirements and is subject to review based on field experience.

Valuable computer time will be saved if the reader familiarizes himself with the contents of this Instruction Bulletin before proceeding with the checks. It will be noted that where outside references are required the reader is directed, in the text, to the applicable Instruction Bulletin.

Comments on this Instruction Bulletin are solicited from the field. It is recognized that maintenance is a dynamic undertaking and that new and improved techniques and procedures are the inevitable result of on-the-job experience. Forward all correspondence to Field Technical Assistance, Department 912, Kingston, New York.

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PREVENTIVE MAINTENANCE

1. PREVENTIVE MAINTENANCE REQUIRING SCOPING

1.1 Philosophy

The value of maintenance programs cannot be overemphasized with regard to their utility in localizing system malfunctions. There is one area, namely memory, where the printouts of failures that occur with a memory maintenance program are not always diagnostic to the extent of isolating the trouble to certain specific pluggable units. In addition, it has been learned from experience that certain memory failures produce erratic symptoms and printouts that, even with experienced personnel, require a time-consuming analysis to localize and correct the malfunction.

It becomes apparent, therefore, that an additional maintenance aid would serve a very useful function in expediting memory failure analysis. Memory failures can be divided into the three most common types: control circuitry (clock, gate generators, etc.), addressing circuitry (MAR, DMD, MOA, MGG, and CMD), and digit or bit failures (DPD and SA circuitry). Although scheduled memory maintenance programs qualify as preventive maintenance tools, it is proposed that the memory programs be supplemented to include a periodic evaluation of waveforms observed at strategic test points in the memory control and addressing circuitry (fig. 1). The latter test points have been singled out because failures associated with them cause misleading symptoms that are difficult to analyze. The other memory malfunction category, that is, digit or bit failures (DPD and SA circuitry), have clearly definitized trouble symptoms that may be more easily corrected using conventional maintenance techniques.

1.1.1 Statistical Summary

It is significant to note that the circuitry to be monitored on a preventive maintenance basis constitutes only 34.7 percent of the total number of pluggable units used in units 7 and 9, and 10 and 12. The remainder, or 65.3 percent, of the pluggable units contain the sense amplifiers and digit plane drivers.

Note

The aforementioned preventive maintenance checks are intended solely for waveform analysis. They do not include any provision for periodic tuning of memory because field experience indicates this is unjustified. Memory tuning should be performed only when the results obtained during preventive maintenance confirm the need for it.

1.1.2 Memory Driver Panels

The memory driver panels, located in units 8 and 11, are not included in the preventive maintenance chart because they are to be tested independent of the computer on the memory driver panel tester located in the site maintenance and test area. A schedule for cycling the driver panels through the maintenance and test area is incorporated into the master preventive maintenance schedule described in paragraph 3.

1.2 Specific Advantages

The time required to perform the electrical preventive maintenance checks will be more than compensated for by the time saved in troubleshooting intermittent and other failures that are difficult to isolate. The benefits that will accrue from this procedure may be summed up as follows:

a. Intermittent failures, the most serious problem, may be caused by subtle circuit deficiencies that produce waveshape deteriorations too slight to be detected with applied margins; but under constant operation with noise buildup and other cumulative deleterious effects, the overall circuitry may deteriorate sufficiently to produce a bad word from memory. Preventive maintenance will closely monitor these basic waveshapes.

b. It will serve as a valuable troubleshooting guide; the most recent preventive maintenance data chart may be used as the criterion of equipment performance.

c. Circuit defects may be more closely evaluated with regard to the time interval between failures.

d. It provides a cross-reference to previous adjustments. This is useful since it will discourage the indiscriminate use of adjustments that may have the effect of masking the actual malfunction.

e. It will permit complete familiarization with the circuit test points and with the expected results.

1.3 Preventive Maintenance Chart Procedures

1.3.1 General

The subsequent paragraphs will analyze the equipment and procedures to be employed in compiling the data required for the preventive maintenance chart (fig. 1). It is recommended that two men be assigned to the task. This arrangement will ensure the high degree of accuracy required for observing all pertinent data.

1.3.2 Equipment Requirements

The following equipment is required:

a. Oscilloscope - Tektronix 545 (3080475)

b. Preamplifier - Tektronix 53/54K (3080476)

c. Probe - Tektronix 510 A (3033788)

d. Hood - Tektronix H510 (3033343)

e. Graticule - 3033583

f. Sync Test Lead - use one that is as short as possible to minimize noise pickup.

The oscilloscope, in conjunction with the accessories listed above, must be calibrated in accordance with the detailed procedures given in paragraphs 1, 2, and 3 of Instruction Bulletin 232.

1.3.3 Procedural Step Analysis

In order to establish proper references for future failure analysis, it is essential that the required preliminary data shown at the top of the preventive maintenance chart be recorded, at this time, in the spaces provided.

Note

The read, write, and inhibit current amplitudes will be measured during memory cycle timing and should be recorded at that time. If these currents, when measured, differ from those recorded in the core memory record data sheet or, if available, in the most recent preventive maintenance chart, any discrepancy must be evaluated to determine whether memory retuning is necessary.

To condition the equipment for waveform analysis, use program MEMORY PM 7, written specifically for this purpose. It must be used for the clock and memory cycle timing checks. If desired, DCS can be used for the other checks although program MEMORY PM 7 will give better results.

To load program MEMORY PM 7 proceed as follows:

1. For memory 1, set the core-memory-assignment switch to REVERSE; for memory 2 set the core-memory-assignment switch to NORMAL.

2. Set the test memory switch to ASSIGNED.

3. Depress the MASTER RESET pushbutton and then the LOAD FROM CARD READER pushbutton.

All measurements are to be made using the test point designated SYNC in the preventive maintenance chart as the triggering input to the oscilloscope. The oscilloscope preamp input is, in turn, to be connected to the other test points shown in the chart in order to display the individual pulse for analysis.

The sequential order of measurements to be performed consistent with a detailed analysis of each follows:

A. Checking the Clock.

This involves a check of the timing between the sync pulses shown in the chart and the other pulses generated in the timing and gating circuitry. Two checks are actually required: the timing, and an evaluation of the waveform. The timing must be recorded in microseconds; however, the pulse may be checked off as correct in the OK column if it meets the amplitude specifications for a standard pulse. If not, institute corrective action. The amplitude specifications apply to all pulses shown with the exception of the three start-memory pulses which are nonstandard types. It must be noted that the width of the standard pulse is not being checked. This has been omitted because the scope sweep setting would have to be changed to evaluate width properly, thereby introducing possible discrepancies between each measurement. With regard to timing, the reference to be used is the core memory record sheet or, if available, the most recent preventive maintenance chart. For an example of the core memory record sheets available at earlier and more recent sites, refer to figures 4 and 5 of Instruction Bulletin 232. To observe the clock pulses, proceed as follows:

1. Using the calibrated oscilloscope and probe, set the sweep to 0.5 usec/cm, the vertical to 1.0V/cm; and the sync control to EXTERNAL.

2. Connect the sync lead to the first sync test point shown (10AEA5) and the probe input to 10ADB1. Position the displayed pulse on the vertical line of the graticule at the extreme left side of the oscilloscope. All timings will be taken with respect to this setting unless otherwise noted.

3. Connect the probe to 10ACB2 and depress the L5 toggle switch of the A register to observe the start-memory pulse from the program counter. Record the results.

4. Release the L5 toggle switch and depress the L6 toggle switch of the A register to observe the start-memory pulse from the address register. Record the results.

5. Release the L6 toggle switch and depress the L7 toggle switch of the A register to observe the start-memory pulse from the IO address counter. Record the results.

6. Release the L7 toggle switch, depress the L6 toggle switch, and perform the remainder of the clock checks. Record the results.

Note

As shown in the preventive maintenance chart, the clear-write and clear-inhibit pulses are synchronized on set-write at 10BCC1. When changing sync to this point, do not readjust the triggering as this may cause an erroneous reading.

B. Checking the Gate Generators.

This involves a check of the six output signals available from the read, write, inhibit, and sample gate generators. The observed waveforms must fall within the specifications shown in the chart. Note that the upper waveform applies only to the X read, Y read, X write, and Y write gate generators; the lower waveform is used only for the inhibit left half-word and inhibit right half-word gate generators. If the observed waveforms conform to the specifications, indicate by checking the OK column. If a deviation exists, institute corrective action.

To observe the gate generator pulses, proceed as follows:

1. Using the calibrated oscilloscope and probe, set the sweep to 1 usec/cm, the vertical to 1.0V/cm, and the sync control to EXTERNAL.

2. The L1 toggle switch of the A register should be depressed for all checks. (All other toggle switches must be in their normal released position.)

3. Connect the oscilloscope sync and probe leads to the respective test points shown in the chart and record the results.

C. Checking the MAR $_{C}$PCF.

This involves a check of the output signals from each $_{C}$PCF in the memory address register. The observed waveforms must fall within the specifications noted on the chart. If they conform, indicate by checking the OK column. If a deviation exists, institute corrective action.

To observe the MAR $_{C}$PCF waveforms, proceed as follows:

1. Using the calibrated oscilloscope and probe, set the sweep to 1 usec/cm, the vertical to 1.0V/cm, and the sync control to EXTERNAL.

2. The L1 toggle switch of the A register should remain depressed for all checks.

3. Connect the oscilloscope sync and probe leads to the respective test points shown in the chart and record the results.

D. Checking the MGG's.

This involves a check of the output signals from each of the MGG's. The observed waveforms must fall within the specifications noted on the chart. If they conform, indicate by checking the OK column. If a deviation exists, institute corrective action.

To observe the MGG outputs, proceed as follows:

1. Using the calibrated oscilloscope and probe, set the sweep to 1 usec/cm, the vertical to 5V/cm, and the sync control to EXTERNAL.

2. The L1 toggle switch of the A register should remain depressed for all checks.

3. Connect the oscilloscope sync and probe leads to the respective test points shown in the chart. If there is any doubt that the observed waveshape may not be within specifications, use more scope vertical sensitivity (2V/cm) and remeasure. Record the results.

E. Check the Memory Cycle Timing.

This involves a check of the relationship between specific waveshapes. These are the memory buffer level vs. the inhibit gate and the inhibit overlap vs. the write current. The observed waveforms must fall within the specifications listed on the chart. If they conform, indicate by checking the OK column. If a deviation exists, institute corrective action.

Note

In addition to the specific checks listed, it is most convenient at this time to measure the inhibit, write, and read current amplitudes and to record their values in the spaces provided in the preliminary data section of the preventive maintenance chart.

To observe the timing relationships and the amplitudes of inhibit, write, and read currents, proceed as follows:

1. Using the calibrated oscilloscope and probe, and the maintenance console, set up the applicable controls as follows:

	Scope		Maintenance Console
	Sweep	Vert	A register switches
a. Mem. buffer level vs. inhibit gate	1 usec/cm	1.0V/cm	Depress L1
b. Inhibit overlap vs. write current and amplitude of inhibit current	1 usec/cm	0.05V/cm	Depress LS
c. Amplitude of read and write currents	1 usec/cm	0.05V/cm	Depress L1

2. Connect the oscilloscope sync and probe leads to the respective test points shown in the chart and record the results.

Note

The inhibit overlap must be observed across one of the inhibit winding terminating resistors. The write and read current must be observed across one of the drive line terminating resistors. For the location of both types of resistors, refer to figures 6 and 7 of Instruction Bulletin 232.

F. Checking the DPD Decoupling.

This involves a check of the noise present at the DPD decoupling circuitry. The noise measurement must include the peak-to-peak excursions. Record the measured values on a separate piece of paper, and then scope the peak-to-peak noise at the corresponding points on either module A or C. Compare the measurements; the noise measured at module B should be the same or less than that present at either module A or module C. If it is, indicate by checking the OK column. If it is greater, troubleshoot the decoupling circuitry in the Z module. To aid in troubleshooting this circuitry, refer to the subject matter on DPD Decoupling in Instruction Bulletin 230 for a complete circuit analysis.

To observe the noise, proceed as follows:

1. Using the calibrated oscilloscope and probe, set the sweep for a long time base (500 usec/cm), the vertical to 0.1V/cm, and the sync to INTERNAL.

2. Depress the L4 toggle switch of the A register. (All other toggle switches must be in their normal released position.)

3. Connect the oscilloscope probe to the test points shown in the chart, and then to the corresponding points on either modules A or C. Compare the values and record the results.

2. PREVENTIVE MAINTENANCE NOT REQUIRING SCOPING

2.1 Introduction

When an equipment malfunction exists, the ensuing troubleshooting procedure invariably concentrates on finding a defective pluggable unit or component part. Sometimes the malfunction is not caused by an electrically defective component, but instead to a poor solder or mechanical connection, or to other causes (not necessarily mechanical) that may easily be overlooked during routine troubleshooting tests. Since these conditions, if present, cause misleading symptoms, it is recommended that certain critical memory areas be checked on a preventive maintenance basis to ensure their reliability.

The subsequent paragraphs give detailed procedures for accurately checking fuses, checking the filament bias voltages, cleaning the blue ribbon connectors, visual inspection of the decoupling resistors in the memory array unit, checking the drive-line ground return, precision checking of the resistance of the inhibit and drive-line terminating resistors, and checking the tightness of the Z row barrier strip screws and other screw connections on the d-c distribution panel of the memory array unit.

2.2 Fuse Check

2.2.1 Purpose

A fuse is part of a continuous line which protects circuits feeding the line against abnormal current surges. Since it is an integral part of a line, it must not alter the line's resistance characteristic. If a fuse is poorly seated in its holder, it will result in a high

resistance connection that causes its associated line to reflect a higher than normal resistance, adversely affecting circuit operation. It is this type of potential fuse problem that is being monitored by the resistance check in the following preventive maintenance procedure. Sight or touch cannot be relied upon to provide this information

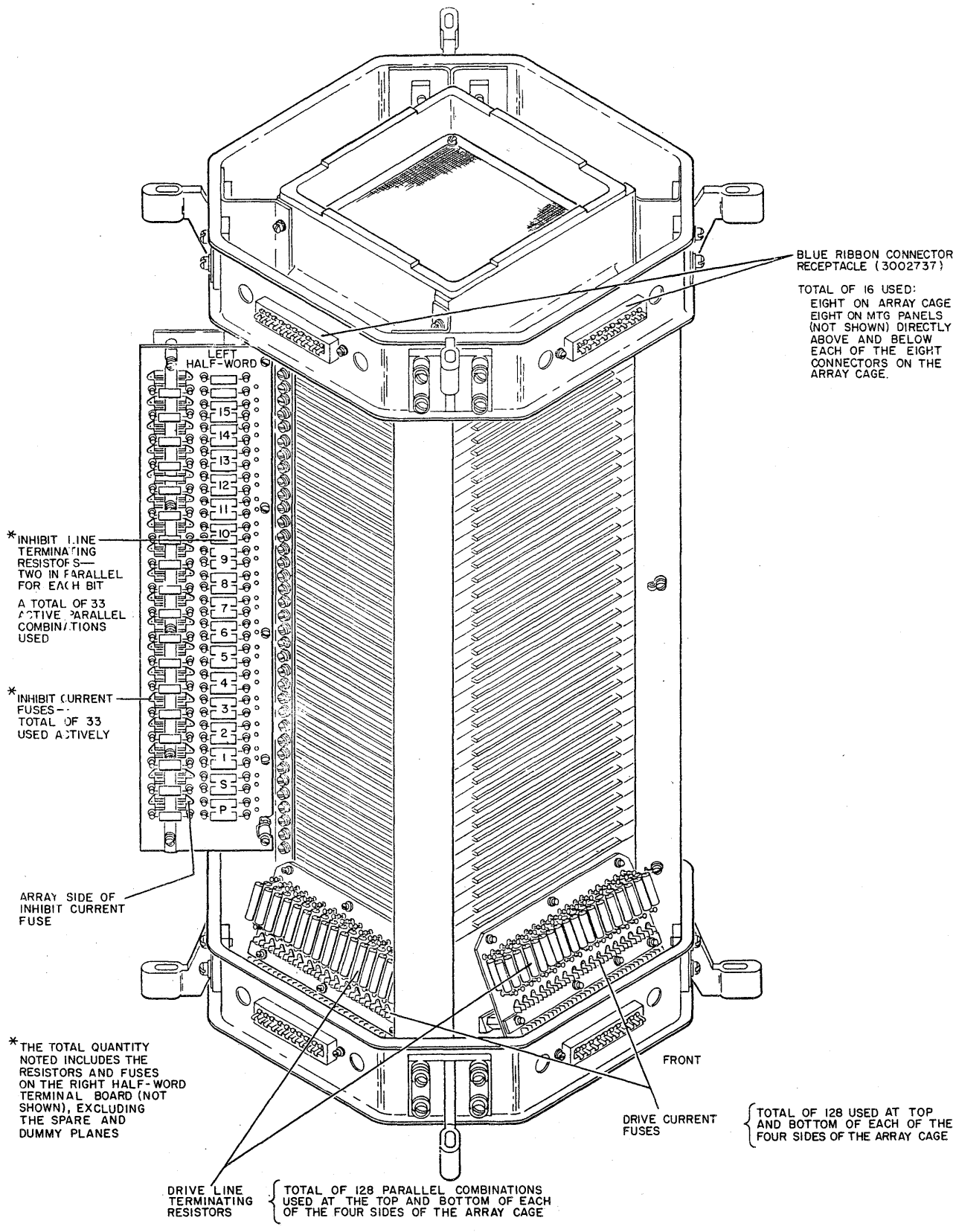


FIGURE 2. MEMORY ARRAY CAGE ASSEMBLY

2.3.2 Procedure

The equipment required consists of a Weston Analyzer (3033318). It is recommended that two men be used to perform these checks. This arrangement will expedite the checks and minimize the time the Central Computer will be inactivated.

WARNING

High voltages are present. Exercise safety precautions in making all voltage checks.

Proceed as follows:

1. Refer to table 1 for the pertinent test data required.

2. Select the analyzer scale that corresponds to the voltage range to be measured.

3. The voltage measurements are to be made with the analyzer connected between the indicated terminals and ground. Figure 3 identifies these terminals on both 6- and 9-tube module assemblies. For example, terminal 2X corresponds to the filament bus bar X (see exploded view) located in the column designated 2 on the module assembly.

4. Corrective action should be taken if the measured voltages differ appreciably from those given in the table. This will entail a visual and resistance check of the applicable filament bias resistor network located in the back-panel wiring of row A of the module under test. Corrective action must be undertaken only with power removed.

TABLE 1. FILAMENT BIAS VOLTAGES

Unit	Module	Voltage	Terminals
7-10	A (9-tube)	-70 -70 -70	2X, 2Y 3X, 3Y 4X, 4Y
	B (6-tube)	-70 -150	2X, 2Y 3X, 3Y
	C (9-tube)	-70 -70 +100	2X, 2Y 3X, 3Y 4X, 4Y
9-12	A (9-tube)	-70 -70 +100	2X, 2Y 3X, 3Y 4X, 4Y
	B (6-tube)	-70 -150	2X, 2Y 3X, 3Y
	C (9-tube)	-70 -70 -70	2X, 2Y 3X, 3Y 4X, 4Y

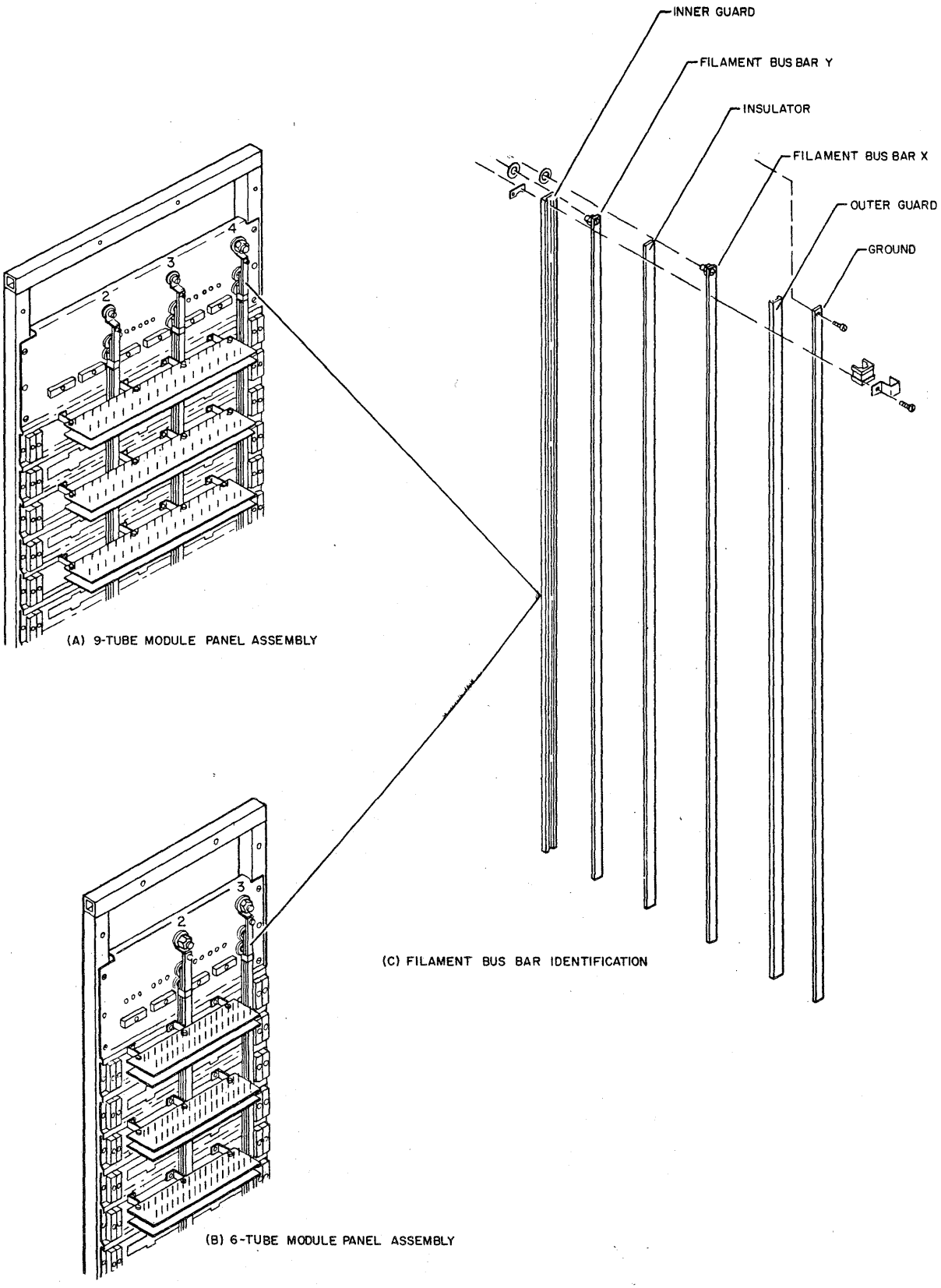


FIGURE 3. FILAMENT BIAS VOLTAGE TEST POINTS

2.4 Cleaning the Connector Receptacles (3002737)

2.4.1 Purpose

This receptacle (see fig. 2), commonly referred to as a blue ribbon connector, contains 32 metallic female contacts. To ensure positive contact with the corresponding male pins of the driver panel, both the male and female contacts must be clean and free from oxidation or other foreign matter.

2.4.2 Procedure

The equipment required consists of a supply of applicators with cotton tips or equivalent and Tecsolv 928 (3034686) cleaning solution. It is recommended that two men be used to clean the connector receptacles. This arrangement will expedite the process and minimize the time the Central Computer will be inactivated.

Proceed as follows:

1. Remove d-c and a-c power.
2. Remove any one of the driver panels.
3. Dip an applicator in the cleaning solution and swab each of the 32 position contacts on the two female connectors that are exposed with the removal of the driver panel. Repeat this procedure for the associated male pins on the driver panel.
4. Replace the driver panel.
5. Repeat the foregoing procedure on an individual basis for each of the remaining seven driver panels. Change the applicator as often as necessary to maintain a good cleaning surface.
6. When completed, a total of 16 female and 16 male connectors will have been cleaned, and all driver panels will be in place.
7. Restore a-c and d-c power.

2.5 Visual Inspection of Decoupling Resistors

2.5.1 Purpose

It is not always possible to detect a decoupling circuit component failure with maintenance programs. Since these conditions have been known to occur, producing the subtle type of circuit defect, the decoupling resistors on the memory array (units 8 and 11) should be visually inspected on a preventive maintenance basis to preclude the existence of such conditions.

2.5.2 Procedure

Inspect each of the decoupling resistors (see fig. 4) on the d-c distribution panel, located at the bottom rear of the memory array, for charring or other physical symptoms of failure. If present, institute action to determine the cause of failure and correct as necessary.

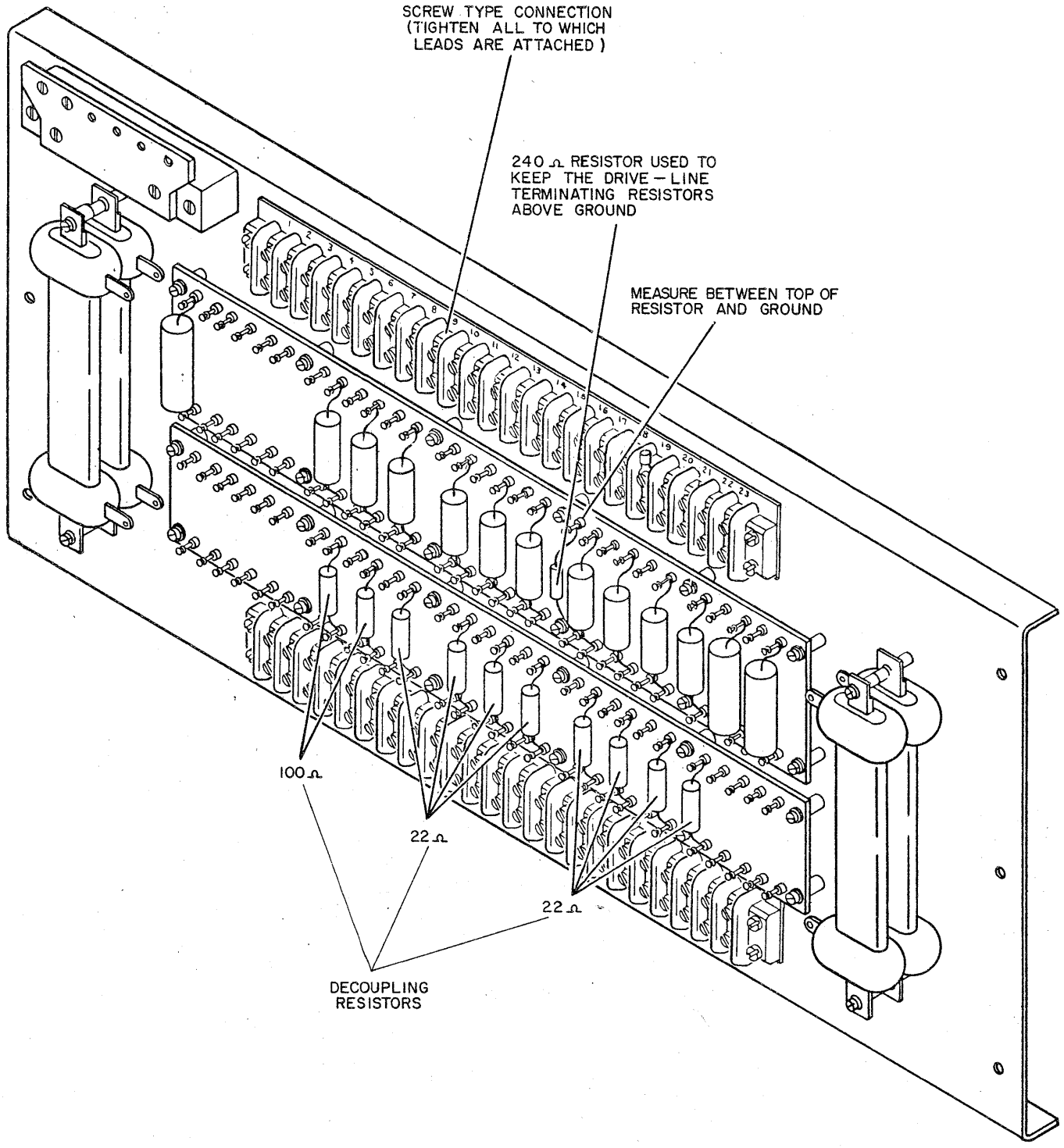


FIGURE 4. DC DISTRIBUTION PANEL ASSEMBLY

2.6 Drive-Line Ground Return Check

2.6.1 Purpose

The drive-line terminating resistors are not returned directly to ground. Instead, they are kept above ground (floating) by a single 240-ohm, 2W, 5% resistor on the d-c distribution panel located at the bottom rear of the memory array (unit 8 or 11) (fig. 4). Since maintenance programs do not readily detect the subtle type of marginal conditions associated with an improper ground return path, such as those due to a direct short to ground or a defective 240-ohm resistor, it is proposed that the ground return path be checked on a preventive maintenance basis. For a theoretical explanation of the floating ground system thus used, refer to Instruction Bulletin 230.

2.6.2 Procedure

The equipment required consists of a Weston Analyzer (3033318). Proceed as follows:

1. Remove a-c and d-c power.

2. Select the R x 10 scale and connect the analyzer between the top of the 240-ohm resistor (see fig. 4) and ground. This connection permits a check of the 240-ohm resistor as well as the ODD V circuit breaker (CB) (9Z3G16) that is in series with the resistor and ground. The measured value should approximate 370 ohms (combined values of resistor and CB).

3. Restore power.

2.7 Terminating Resistor Check

2.7.1 Purpose

The components to be checked in this category are the inhibit and drive current terminating resistors. Individually they are 10-ohm ±1% precision types that are paired in parallel to provide an effective load of 5-ohms ±1%. It is this effective load resistance which is to be measured on a preventive maintenance basis. The importance of monitoring this terminating load resistance cannot be overemphasized. The reason for this stems from the fact that the drive and inhibit currents are scoped for proper amplitude as a function of the voltage drop across the terminating load resistance. Reviewing, this is accomplished by calibrating the scope to the value of voltage drop that corresponds to 400 ma of current flowing through 5 ohms. According to Ohm's Law this is computed to be 2V. Hence, if the resistive load should change in value, the voltage drop will vary accordingly. If the inhibit or drive currents were to be observed under these conditions, it would appear that the currents had varied and required adjustment. Indiscriminate adjustment of the currents to compensate for the load resistance change will only result in deteriorating the actual current through the memory plane cores. The only practical solution, therefore, is identification and replacement of the defective component.

2.7.2 Procedure

The equipment required consists of a General Radio Bridge (3033319). Set it up for resistance measurements in accordance with the instructions contained in the operating manual for this equipment.

It is recommended that two men be used to perform these checks. This arrangement will expedite the checks and minimize the time the Central Computer will be inactivated.

Proceed as follows:

1. Remove the air and a-c and d-c power from the memory array.

2. Remove all driver panels. This is done to eliminate the shunting effects of the driver circuitry.

3. Remove all memory array window panels.

4. Place the bridge test leads, in turn, across each of the parallel resistor combinations constituting the individual inhibit and drive-line terminating resistors (fig. 2). Due to the small value of resistance being checked, each measurement must be made with the test leads connected in exactly the same manner to minimize the possibility of error.

5. Note the resistance; it must fall within the range of 4.9 to 5.1 ohms. This tolerance is slightly higher than 5 ohms ±1% because it takes into account the practical limitations of the scope reading when measuring current amplitude. Replace the paralleled 10-ohm resistors if these limits cannot be met.

6. Restore air and a-c and d-c power upon completion of all checks.

2.8 Screw Tightness Check

2.8.1 Purpose

A loose screw connection is a potential source of trouble. To avoid the possibility of such an occurrence, it is proposed that those screw connections in the memory units associated with d-c distribution be checked for tightness on a preventive maintenance basis.

2.8.2 Procedure

The equipment required consists of a screwdriver. It is recommended that two men be used to check the tightness of screws involved. This arrangement will expedite the process and minimize the time that the Central Computer will be inactivated.

Proceed as follows:

1. Remove d-c and a-c power.

2. Tighten all screws to which leads are attached on the d-c distribution panel assembly (fig. 4). This panel is accessible through the opening of the cable duct door at the bottom rear of the memory array (units 8 and 11).

3. Remove the covers from the Z rows of units 7 and 9 for memory 1 (10 and 12 for memory 2), and tighten all screws thereon to which leads are attached.

4. Replace the Z row covers.

5. Restore power.

3. PREVENTIVE MAINTENANCE SCHEDULE

3.1 Introduction

Preventive maintenance checks are composed of two basic groupings: those requiring scoping and those not requiring scoping. In the former category are all the checks included in the preventive maintenance chart (see fig. 1 and par. 1.3) and the cycling of memory driver panels in the maintenance and test area (refer to 1.1.2). In the latter category are all the mechanical, resistance, and voltage checks (refer to par. 2). Both groups, broken down into their constituent functional sections together with the time interval assigned to each, are itemized in the grouping column of the master schedule chart illustrated in figure 5, foldout.

3.2 Scheduled Checks

As shown in figure 5, the preventive maintenance checks requiring scoping are to be performed on a 3-month basis. Preventive maintenance not requiring scoping is segregated into 6- and 12-month periods; that is, the fuse check, filament bias voltage check, cleaning the connector receptacles and visual inspection of the decoupling resistors are to be done every 6 months, whereas the terminating resistor check and the screw tightness check are to be performed every 12 months.

The assigned schedules are based on current concepts of equipment requirements; however, they will be under constant review, and adjustments will be made, if warranted, based on field experience.

When each of the individual checks are completed, the Field Engineer should indicate this fact by placing the completion date and his initials in the spaces provided for the applicable memory unit under test (memory 1 or memory 2). The only exception pertains to the cycling of the driver panels because they involve both memory units. This has been done in order to limit the removal of only one of the original driver panels in each memory at a time. As noted (fig. 5), the recommended schedule sequence fulfills this requirement since it provides initially for the testing of the memory 1 and memory 2 spare driver panels. These, in turn, should then be used singly as replacements for the other driver panels when they are cycled through the maintenance and test area. The date to be recorded for the completion of these checks must correspond to the day the driver panels are reinserted in their respective memory units. The initials required are those of the Field Engineer who reinserts the driver panel in the memory array unit. This must be done only when it is confirmed that the driver panel has been duly tested in the maintenance and test area, though not necessarily by the Field Engineer making the entry.

PRELIMINARY DATA

DATE _____

RECORD THE FOLLOWING:

COMPUTER A ☐ B ☐ MEMORY I ☐ II ☐

OSCILLOSCOPE NO. _____

PRE-AMP NO. _____

MEMORY TUNE CHARACTERISTICS

READ CURRENT _____ MA
WRITE CURRENT _____ MA
INHIBIT CURRENT _____ MA
} THESE MEASUREMENTS ARE MADE DURING MEMORY CYCLE TIMING

RUN MCI MEM 01 AND RECORD MARGINS TO FAILURE ON THE FOLLOWING LINES:

-300 B1 (E1) + _____ − _____
-300 B2 (E2) + _____ − _____

ARE ALL PU'S IN UNITS 7, 8 AND 9; OR 10, 11 AND 12 IN THEIR ASSIGNED LOCATIONS ? YES ☐ NO ☐

IF ANSWER IS NO, IDENTIFY THE MISPLACED ITEMS

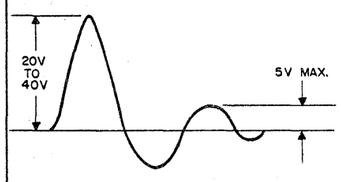
_____
_____
_____
_____

MEASURED DATA

CLOCK

PULSE	LOCATION	TIMING	OK
CLR MEM CTLS	10 AEA 5	SYNC	
START MEM	10 ACB 2		
PGR CTR		μsec } NOT STD PULSE	
ADR REG		μsec } NOT STD PULSE	
ADR CTR		μsec } NOT STD PULSE	
SET READ	10 ACA 2	μsec	
SAMPLE	10 ACJ 1	μsec	
CLR MEM CTLS	12 CDB 1	SYNC	
SAMPLE R.	12 CFF 7	μsec	
CLR MEM CTLS	10 AEA 5	SYNC	
SAMPLE L.	10 AEH 3	μsec	
CLR READ	10 ACE 5	μsec	
SET INHIBIT	10 BCE 5	μsec	
SET WRITE	10 BCC 1	μsec	
SET WRITE	10 BCC 1	SYNC	
CLR WRITE	10 BDB 4	μsec	
CLR INHIBIT	10 BDE 8	μsec	

STANDARD PULSE



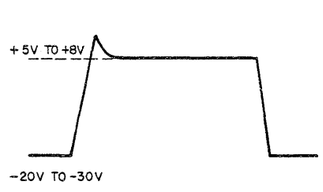
GATE GENERATORS

FUNCTION	LOCATION	OK
CLR MEM CTLS	10 AEA 5	SYNC
X READ	10 CLB 8	
X WRITE	10 CLH 4	
INHIBIT LHW	10 ADH 6	
CLR MEM CTLS	12 CDB 1	SYNC
Y READ	12 ALB 8	
Y WRITE	12 ALH 4	
INHIBIT RHW	12 CDH 6	

GATE GENERATOR WAVEFORMS

RISE TIME -0.5 USEC MAX.
FALL TIME -0.5 USEC MAX.

X-Y READ AND X-Y WRITE ONLY



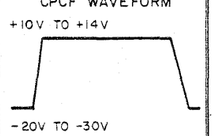
RISE TIME -0.3 USEC MAX.
FALL TIME -0.3 USEC MAX.

INHIBIT LHW-RHW ONLY

MAR cPCF

LOCATION	OK
12 CDB 1	SYNC
12 APF 5	
12 ARC 5	
12 ARG 1	
12 ASF 5	
12 ATF 5	
12 AUC 5	
12 AUG 1	
12 AVF 5	
12 AWF 5	
12 AXC 5	
12 AXG 1	
12 AYF 5	
10 AEA 5	SYNC
10 CPF 5	
10 CRC 5	
10 CRG 1	
10 CSF 5	
10 CTF 5	
10 CUC 5	
10 CUG 1	
10 CVF 5	
10 CWF 5	
10 CXC 5	
10 CXG 1	
10 CYF 5	

CPCF WAVEFORM

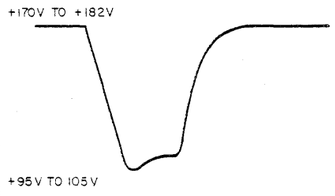


RISE TIME -0.5 USEC MAX.
FALL TIME -0.5 USEC MAX.

MGG OUTPUT

FUNCTION	LOCATION	OK
CLR MEM CTLS	10 AEA 5	SYNC
X READ ODD	10 CCF 5	
X WRITE ODD	10 CEF 5	
X READ EVEN	10 CGF 5	
X WRITE EVEN	10 CJF 5	
CLR MEM CTLS	12 CDB 1	SYNC
Y READ ODD	12 ACF 5	
Y WRITE ODD	12 AEF 5	
Y READ EVEN	12 AGF 5	
Y WRITE EVEN	12 AJF 5	

MGG WAVEFORM

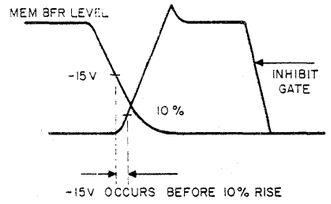


MEMORY CYCLE TIMING

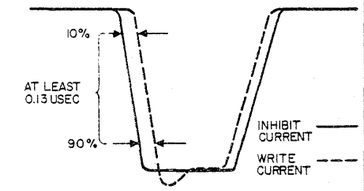
TIMING RELATIONSHIP	LOCATION	OK
CLR MEM CTLS	10 AEA 5	SYNC
*MEM BFR LEVEL VS	10 BFA 6	
INHIBIT GATE	10 BFA 7	
**INHIBIT OVERLAP VS	ANY INHIBIT LINE	
WRITE CURR	ANY Y LINE	

SPECIFICATIONS

* WHEN MEASURING AT THE INPUT TO THE DPD, THE MEMORY BUFFER LEVEL SHALL BE DOWN TO -15V BEFORE THE 10% RISE OF THE INHIBIT GATE GENERATOR



** THE INHIBIT CURRENT SHALL START AT LEAST 0.13 USEC BEFORE WRITE CURRENT AT ALL CORRESPONDING POINTS OF THE PULSE BETWEEN THE 10% AND 90% POINTS. THE END OF INHIBIT MUST OCCUR AT THE SAME TIME OR LATER THAN THE END OF WRITE, BUT NO LATER THAN 6.6 USEC FROM CLEAR-MEMORY-CONTROLS.



DPD DECOUPLING

VOLTAGE	LOCATION	OK
-150 V	10 BFD 1	
+150 V	10 BFE 3	
-150 V	12 BFD 1	
+150 V	12 BFE 3	

FIGURE 1. 64^2 CORE MEMORY PREVENTIVE MAINTENANCE CHART

GROUPING	3 MONTHS													3 MONTHS												3 MONTHS												3 MONTHS												
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52
PM REQUIRING SCOPING																																																			
3-MONTH SCHEDULE																																																		
USING PM CHART	MEM I											MEM II		MEM I											MEM II		MEM I										MEM II		MEM I											MEM II		
DATE																																																		
INITIAL																																																		
CYCLING OF DRIVER PANELS		MEM I SPARE	MEM II XA	MEM II XB	MEM II XC	MEM II XD		MEM II YA	MEM II YB	MEM II YC	MEM II YD				MEM II SPARE	MEM II XA	MEM II XB	MEM II XC	MEM II XD		MEM II YA	MEM II YB	MEM II YC	MEM II YD				MEM II SPARE	MEM II XA	MEM II XB	MEM II XC	MEM II XD		MEM II YA	MEM II YB	MEM II YC	MEM II YD				MEM II SPARE	MEM II XA	MEM II XB	MEM II XC	MEM II XD		MEM II YA	MEM II YB	MEM II YC	MEM II YD		
DATE																																																		
INITIAL																																																		
PM NOT REQUIRING SCOPING																																																		
6-MONTH SCHEDULE							MEM I													MEM II											MEM I																				
FUSE CHECK					DATE / INITIAL ___													DATE / INITIAL ___											DATE / INITIAL ___											DATE / INITIAL ___										
FILAMENT BIAS VOLTAGE CHECK					DATE / INITIAL ___													DATE / INITIAL ___											DATE / INITIAL ___											DATE / INITIAL ___										
CLEANING THE CONNECTOR RECEPTACLES					DATE / INITIAL ___													DATE / INITIAL ___											DATE / INITIAL ___											DATE / INITIAL ___										
VISUAL INSPECTION OF DECOUPLING RESISTORS					DATE / INITIAL ___													DATE / INITIAL ___											DATE / INITIAL ___											DATE / INITIAL ___										
DRIVE LINE GND RETURN CHECK					DATE / INITIAL ___													DATE / INITIAL ___											DATE / INITIAL ___											DATE / INITIAL ___										
12-MONTH SCHEDULE			MEM I																											MEM II																				
TERMINATING RESISTOR CHECK		DATE / INITIAL ___																									DATE / INITIAL ___																						
CHECK TIGHTNESS OF SCREWS		DATE / INITIAL ___																									DATE / INITIAL ___																						

FIGURE 5. RECOMMENDED MASTER SCHEDULE FOR PREVENTIVE MAINTENANCE (PM) OF MEMORY (ONE YEAR PERIOD)