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THEORY OF OPERATION

OF

INPUT SYSTEM

FOR

AN/FSQ-7

COMBAT DIRECTION CENTRAL

AND

AN/FSQ-8

COMBAT CONTROL CENTRAL

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PART 1
INTRODUCTION

CHAPTER 1
GENERAL

1.1 SCOPE OF MANUAL

This manual presents a theory of operation for the AN/FSQ-7 Combat Direction Central and the AN/FSQ-8 Combat Control Central. The AN/FSQ-7 Combat Direction Central is regarded as standard and is described in detail. The AN/FSQ-8 Combat Control Central is considered a variation of the AN/FSQ-7 equipment and, for purposes of explanation, is described in terms of its differences from the AN/FSQ-7 equipment.

The manual is divided into seven parts. Part 1, Introduction, discusses data processing systems in general and the AN/FSQ-7 Combat Direction Central as an example of such a system; the relationship of the Input System to other systems in the Central; and the origin and processing of input data and test and monitoring equipment used with the Input System. The part concludes with a general description of the simplex maintenance console: equipment which is not physically part of the Input System but is used mainly for the control of Input System equipment. Parts 2 through 6 of the manual are devoted to specific portions of the Input System. The long-range radar input (LRI), gap-filler input (GFI), and crosstell (XTL) elements are described in Parts 2, 4, and 5 respectively; Part 3 deals with the long-range radar input monitor (LRI monitor) whch is associated with the LRI element; and Part 6 describes the test pattern generator (TPG) which serves as test equipment for the LRI, GFI, and XTL elements. The AN/FSQ-8 Combat Control Central is the subject of Part 7 which describes the differences between this equipment and the AN/FSQ-7 Central.

The various installations of the AN/FSQ-7 or AN/FSQ-8 equipments often differ in certain details; for example, in the number of channels of XTL equipment employed (which determines the number of other Centrals which may be connected to the Central). Usually these differences are ignored, since they do not affect the principles of equipment operation and the equipment is discussed in terms of its maximum capabilities. Occasionally, however, differences between systems do affect the theory of operation, and these differences are discussed.

1.2 AN/FSQ-7 COMBAT DIRECTION CENTRAL

The AN/FSQ-7 Combat Direction Central is a data-processing system of the high-speed digital-computer type performing operations on data in binary form. It receives information of the air defense situation continuously, automatically, and in large volume, and must process this information without delay. These requirements call for an elaborate Input System, quite different from anything usually found in data-processing systems. Input Systems in general, and then the AN/FSQ-7 Input System, are discussed below.

1.3 INPUT SYSTEMS IN GENERAL

Consider first a simple data-processing system such as a desk calculator. This instrument is a slow-speed, mechanical, decimal, digital computer. It is capable of accurate and efficient computation, but a means must be provided for the operator to introduce into the machine the problem which he wishes solved. This means is the calculator keyboard. The operator expresses the problem by depressing keys which, in turn, operate the necessary mechanisms in the machine. The keyboard is the input "system" of the calculator.

More elaborate mechanical and electronic-mechanical data-processing systems can process a much greater volume of data in a given time than any desk computer. In fact, data cannot be inserted manually into such a machine fast enough to take advantage of its capabilities, and is therefore transferred to punched cards or punched tapes. This makes possible an accumulation of input data which the computer can then accept at a rate compatible with its data-processing capacity.

Computing machines operating by means of moving parts are inherently slow compared to modern electronic computers using pulsed electronic signals. Again, however, the Input System must be adequate to the potentialities of the computer. Modern computers, therefore, transfer data to magnetic tapes or drums or to magnetic core or flip-flop registers: temporary storage devices capable of releasing data to the computer at high-speed regardless of the speed at which the data was originally introduced.

In all of the systems considered above, data is, in a sense, prepackaged; i.e., offered in a form most suitable to the operation of the machine. Under these circumstances a comparatively simple Input System suffices. However, the AN/FSQ-7 Combat Direction Central is not an isolated machine; it is part of the SAGE Complex. This relationship imposes a special set of operational requirements on the Central and on its Input System, which must, specifically, be adequate to the following conditions:

a. Input data originates at distant points and is transmitted to the Combat Direction Central over phone lines. The data format and rate of transmission is established by phone-line characteristics, not by the characteristics of the computer.

b. Input data is of several types. Each type originates at many sources. The computer must be capable of processing data of all types and from all sources.

c. The types and densities of data traffic are determined by the tactical situation, not by computer requirements. The Input System must accept all data, make the necessary discernments as to its validity, process it, store it temporarily, transfer it according to certain priority specifications, etc. The result of these steps, the "product" of the Input System, is analogous to the prepackaged input to more conventional computers. The Input System might almost be thought of as a digital computer feeding another digital computer.

1.4 AN/FSQ-7 INPUT SYSTEM

1.4.1 General

The Input System of the AN/FSQ-7 Combat Direction Central (fig. 1–1) receives three types of data:

a. Long-range radar input (LRI): data from long-range radar (P) sites.

b. Gap-filler input (GFI): data from gap-filler sites, supplementing the long range radar sites.

c. Crosstell (XTL): data from other Combat Direction or Combat Control Centrals.

These three types of data are processed by the LRI, GFI, and XTL elements, respectively. In addition, the Input System includes a LRI monitor associated with the LRI element and a test pattern generator (TPG) used to test the three elements.

1.4.2 LRI Element

The LRI element may receive information over a maximum of 32 telephone channels. The information comes from radar P-sites (see Ch 2) and consists of binary-coded messages (see Ch 3), 52 bits in length. The input signal repetition rate is 1,300 cycles-per-second

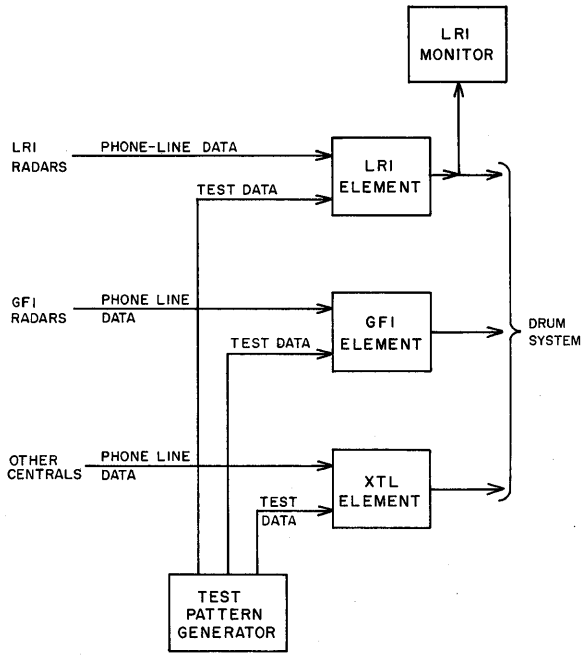


Figure 1–1. Input System Block Diagram and Signal Flow

(cps); thus, a single message takes a maximum of 52/1,300 seconds, or approximately 40 ms, to enter the LRI element.

The information contained in the LRI messages represents filtered-target data. In other words, in normal operation only data pertinent to the Air Defense Program is transmitted to the Input System. The data consists of targets detected by long-range radars, friendly targets detected and identified by identification-friend-or-foe (IFF) radar, and height information on selected targets as requested by the Combat Direction Central.

The LRI message is checked for accuracy, divided into two message words, then read out in parallel fashion to the Drum System. The LRI element adds a site identity code to the message, indicating the channel that processed the message, and clock time, indicating the relative time the message was sent from the LRI element to the Drum System.

The readout of the message words to the Drum System is governed by the receipt of a drum-demand pulse which indicates an empty slot in the LRI field on the LOG drum. The drum-demand pulse searches the individual input channels in order of priority, until a channel storing a message is found. The drum-demand pulse then initiates the transfer of the message to the Drum System. This readout takes 20 μsec. Since it takes 40 ms to load a message into an input channel, the LRI element is theoretically capable of transferring to the Drum System all messages received over all 32 channels, with very little delay.

1.4.3 GFI Element

The GFI element may receive information over a maximum of 16 telephone channels. The information received from a gap-filler radar site (see Ch 2) differs from LRI information in that it is not in the form of encoded messages suitable for transfer to the Drum System, and it includes data on all targets detected by the gap-filler radar. To allow transmission of this information over commercial telephone facilities, a system of slowed-down video (SDV) is used. The SDV divides the radar display into boxes and provides sufficiently accurate location of targets by defining the box within which the target is located. The information is received at a rate of 1,600 pulses-per-second (pps).

The GFI target data is viewed within the GFI element by mapper operators who screen out unwanted targets. This information is then processed by counter circuits, which reduce the data to binary form and make up a message of the type acceptable to the Drum System. Filtered-target information is then read out to the Drum System in a manner similar to that described in 1.4.2.

1.4.4 XTL Element

The XTL element may receive information over telephone lines from a maximum of 22 other Combat Direction Centrals. The reception and processing of the XTL message is similar to that described in 1.4.2 for LRI messages. The XTL message, however, is composed of 92 bits: five separate message words of 17 bits each, 6 blank timing pulses and 1 sync bit. The five incoming words are sent in serially interleaved form: the first bits of each word in sequence followed by the second bits of each word, and continuing in this manner. Since XTL messages are sent on a party line to a group of Direction Centrals, the XTL message contains an address code. The XTL element checks the address and accepts only messages that are addressed to the particular receiving Direction Central or to all Centrals. The XTL element then reconstructs the five original message words, adds site identity and clock time (as in the case of the LRI message) and reads out the message to the Drum System in response to a drum-demand pulse.

1.4.5 LRI Monitor

The LRI monitor is used to monitor data processed by the LRI element for transfer to the Drum System. The processed data is in the form of messages, each relating to a particular target. Messages selected for display appear as target indications in a plan-position indication (PPI) type of display at one or more of four display consoles. One console is camera-equipped to photograph such displays.

The LRI monitor permits examination of LRI data after processing by the LRI element but before processing by the Central Computer. It thus assists operating and maintenance personnel to evaluate LRI coverage and operation of the LRI element.

1.4.6 Test Pattern Generator

The TPG is used to test the operation of the LRI, XTL, and GFI elements during installation and subsequent maintenance. It consists of three sections, LRI, XTL, and GFI, each providing test signals, simulating phone-line inputs, to the indicated elements. Each section of the TPG may be operated under manual or computer control or by a combination of both.

CHAPTER 2
DATA SOURCES AND TRANSMISSION

2.1 LRI DATA

2.1.1 General

LRI data originates at radar P-sites. A fully equipped P-site contains a long-range search radar equipped with an MK X IFF radar beacon, two semi-automatic height-finder radars and various data-processing equipments. The number and location of P-sites depends on the size and shape of the subsector area; as many as 16 P-sites can send LRI data to a Combat Direction Control.

At each P-site, data is filtered by various devices to reduce noise, spurious targets, and jamming returns and thus furnish the computer with information of maximum usefulness. The filtered data is formed into binary messages, each relating to a particular target, and transmitted over a phone circuit to the Combat Direction Central. The processing of data at radar sites does not fall within the scope of this manual and is discussed only briefly below. Long-range search radar, MK X IFF, and height-finder radar data are considered in that order, followed by a discussion of the telephone transmission of LRI data.

2.1.2 Long-Range Search Radar Data

Long-range search radar data is upgraded at the radar site by these processes: moving target indicator (MTI), fine-grain data (FGD), and manual mapping.

The MTI apparatus endeavors to eliminate all radar returns except those produced by a moving object.

Fine-grain data apparatus uses the technique of beam-splitting to achieve a much higher degree of azimuth resolution when locating a target than is possible with conventional radar. (Beam-splitting notes the azimuths at which the first and last radar returns are received from a target during one sweep and then computes the average or middle azimuth. The disadvantage of beam-splitting – the time delay between initial detection of a target and the reporting of the averaged azimuth – is overcome by noting the duration of the delay in the LRI message). Fine-grain data apparatus also tends to reject noise by establishing minimal criteria for an acceptable target.

Finally, manual mapping is used to eliminate unwanted radar returns which have survived the other filtering techniques. In manual mapping, targets are presented on a display screen and an operator uses an opaquing fluid to blot out those targets or areas which are of no tactical significance. Un-opaqued target indications are picked up by a photoelectric device, and generate descriptive messages for transmission to the Combat Direction Central. These messages contain the following information:

a. Target range from the radar set
b. Target azimuth with respect to true north from the radar set
c. Time delay between initial detection of target and transmission of message
d. Run length, indication of size of target or existence of multiple targets at reported location
e. Message label which identifies the message source as search radar rather than IFF or height finder.

2.1.3 MK X IFF Radar Beacon Data

The MK X IFF radar beacon enables radar systems to distinguish between friendly and hostile aircraft. Friendly aircraft carry transponders (receiver-transmitters) which reply in a prescribed code when interrogated by a ground interrogator (transmitter-receiver). The response is usually displayed alongside the radar return, indicating to the operator that the target is friendly.

The MK X IFF radar beacon sends messages to the Direction Central which contain the following information in binary form:

a. Target range from the radar set
b. Target azimuth with respect to true north from the radar set
c. Time delay between initial detection of target and transmission of message, up to 16 seconds, with an accuracy of $\frac{1}{4}$ second
d. Security identification feature (SIF), if used
e. Message label which identifies message source as IFF rather than search radar or height finder.

In order to obtain a simultaneous report of the MK X IFF response with the radar report of the target, the MK X set and its associated radar are synchronized, when sweeping, in azimuth and range. This synchronization allows the MK X IFF to generate range and azimuth information on friendly targets by noting the radar azimuth when a response is received and the time between interrogation and response. The IFF range and azimuth data is in FGD form.

2.1.4 Height-Finder Radar Data

The height-finder radar equipment associated with a P-site supplies target-height data on specific targets to the Combat Direction Central in response to requests received from the Central. The height-finder radars are semiautomatic; that is, the radar antenna is automatically positioned to the azimuth of the target for which height information is requested. In addition, the range cursor on the range-height indicator is automatically positioned at target range. The last-measured or estimated height is also supplied to the height-finder operator to aid in identifying the target. New target height determined by the height finder is automatically encoded and sent to the Direction Central as part of the height-finder message. Replies to special requests in the height-request message are selected and added to the height-finder message by depressing one of a set of pushbuttons.

The complete height-finder message contains the following information in binary form:

a. New target height
b. Predominant formation of a multiple target
c. Separation between aircraft in a multiple target
d. Number of aircraft in a multiple target
e. Request number
f. Address identifying which of two height finders is replying
g. Special reply (if any)
h. Message label which identifies the message source as a height finder rather than search radar of IFF.

2.2 GFI DATA

2.2.1 General

Gap-filler radars are automatic radars used to fill gaps in long-range radar coverage which might allow low-flying targets to pass undetected. Processing of GFI data at the radar sites is different from that of LRI data because the GFI sites are designed to be unattended. The mapping function must therefore be performed within the AN/FSQ-7 Combat Direction Central (refer to Part 4). The data is transmitted to the Central in raw form. However, some degree of data-reduction is necessary to permit the radar-video information, which normally has a bandwidth of several megacycles, to be transmitted over commercial telephone facilities having an upper frequency limit of 2,000 cycles. The technique used is slowed-down video (SDV).

2.2.2 Slowed-Down Video

The SDV technique relies on the principles of quantizing and video integration. Quantizing in this case consists of dividing an undifferentiated area into quanta or boxes of fixed dimensions and definable location. Video integration integrates all targets within one of these boxes into one report. Thus the information transmitted to the Central must perform two functions:

a. Locate the box, or quanta, which is being reported on.
b. Report the presence or absence of any targets within the box.

GFI quantizing is illustrated in figure 1–2. The total area of coverage is divided into 256 azimuth sections. Each azimuth section is divided, nominally, into 64 range segments. A particular box is therefore located by establishing its azimuth with reference to north and establishing its range with reference to zero.

At the radar site all target returns within a box are reported as a single return (video integration). The presence of one target results in a report; the presence of additional targets is not indicated. In figure 1–2, for example, a target indication appears in the 38th range segment of the 15th azimuth section, but the number of targets represented by this indication cannot be known.

It can be seen, therefore, that quantizing results in a loss or coarsening of data. The degree of coarsening is determined by the size of the box, and this in turn depends on the characteristics of telephone transmission and of radar operation. The average rate of rotation of the GFI radar antenna is 6 rpm: equal to one revolution per 10 seconds. The equipment must be theoretically capable of reporting on every box in its coverage area during each revolution, or in present usage, of reporting on 16,384 boxes (256 azimuths x 64 range segments): equivalent to 1,638 boxes per second. Since the rotational rate of the radar antenna varies, the figure of 64 range segments per azimuth sector is not critical; and the number of boxes per sweep may be rounded to 1,600 per second. To provide target reports to this degree of fineness, a telephone transmission frequency of 1,600 cps, or one cycle per box, is required – well within the 2,000 cps upper frequency limit for telephone transmission.

2.3 XTL DATA

Crosstell messages originate in the Output System of another Combat Direction Central or of a Combat Control Central. A typical example of such a message would be track data on a target moving from one sector to an adjoining one. The message is sent to all Centrals associated with the originating Central but an address code included in the message makes it acceptable only to the Central for which it is intended, or, in the case of an all-parties message, to all Centrals.

2.4 TELEPHONE TRANSMISSION OF DATA

The three types of data described above are all sent to the Combat Direction Central over telephone lines. Transmission is described for each type below.

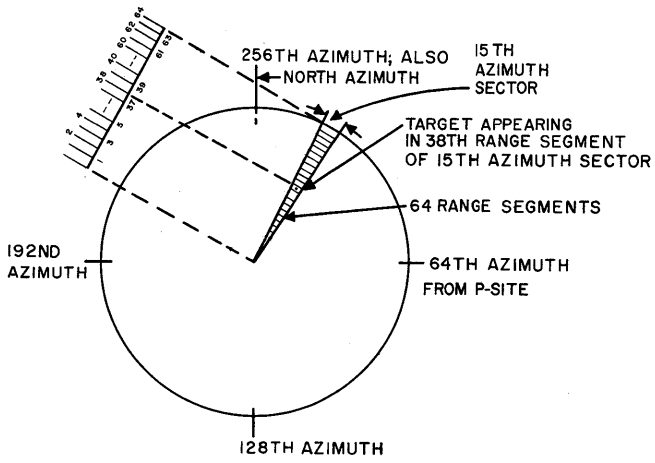


Figure 1–2. Quantizing of GFI Information

2.4.1 LRI Data

The pulses digitally expressing the LRI message (whether search, MK X IFF, or height-finder) are fed to a data conversion transmitter (DCT) at the radar site. This equipment converts the pulses to sine waves, adds a timing frequency, and feeds out on three lines (called timing, sync, and data) to a digital data transmitter (DDT), a part of the telephone transmitting apparatus. The timing signal is a continuous 1,300-cps sine wave; the sync and data signals are gated 1,300-cps sine waves in phase with the timing signals. Within the DDT, the three signals modulated a voice-frequency carrier. The frequency of the timing signal is halved (to 650 cps) before it modulates the carrier. The three signals are distinguished by their amplitudes.

The modulated-telephone-carrier signal is transmitted over commercial telephone lines to a digital data receiver (DDR) in the telephone terminal equipment at the receiving Central. Within the DDR, the carrier signal is demodulated. The three component signals are separated according to their relative amplitudes. The timing signal frequency is doubled to the original 1,300 cps. The three signals are then sent on separate lines to data conversion receivers (DCR's) in the LRI input channel equipment. The timing signal is again a continuous 1,300-cps sine wave; the sync and data signals are gated 1,300-cps sine waves in phase with the timing signal.

The complete telephone transmission facilities include duplicate parallel DDT's, DDR's, and telephone lines. The second set of telephone facilities is a restoration telephone line for use if the first telephone line develops trouble. Automatic switching facilities are included in the telephone terminal equipment. Both telephone circuits are monitored at the Combat Direction Central, and the one that provides the more satisfactory transmission is automatically selected as the active circuit. (Manual selection of the active circuit is also possible.)

2.4.2 GFI Data

Though GFI data is transmitted from the radar sites in quite a different form than LRI data, the transmission process is very similar to LRI data transmission. The minor differences are:

a. The basic timing frequency for GFI messages is 1,600 cps instead of 1,300 cps.

b. Because of the nature of the GFI message, the three types of signal are designated azimuth and north azimuth (sync), targets (data), and range (timing). The terms in parentheses are the analogous LRI signals.

c. Transmission is over a single circuit only. There are no restoration, automatic monitoring, or automatic switching circuits.

2.4.3 XTL Data

Crosstell data is transmitted by the same type of equipments and circuits and in the same manner as LRI data.

CHAPTER 3
DATA PROCESSING IN INPUT SYSTEM

3.1 GENERAL

LRI, GFI, and XTL data flows into LRI, GFI, and XTL elements respectively. There are basic similarities in the operation of all three elements (fig. 1–3); these will be considered first followed by a discussion of the particular elements.

Each element contains many channels. Each channel is associated with a specific data source: a radar site or another Central. Data comes into each channel on three lines from a digital data receiver (telephone equipment). The data is expressed by a configuration of individual sine waves or bits, in synchronism with a basic timing frequency.

Entering the element, data first passes through an input switching section. This section permits substitution, if desired, of test data (generated by the test

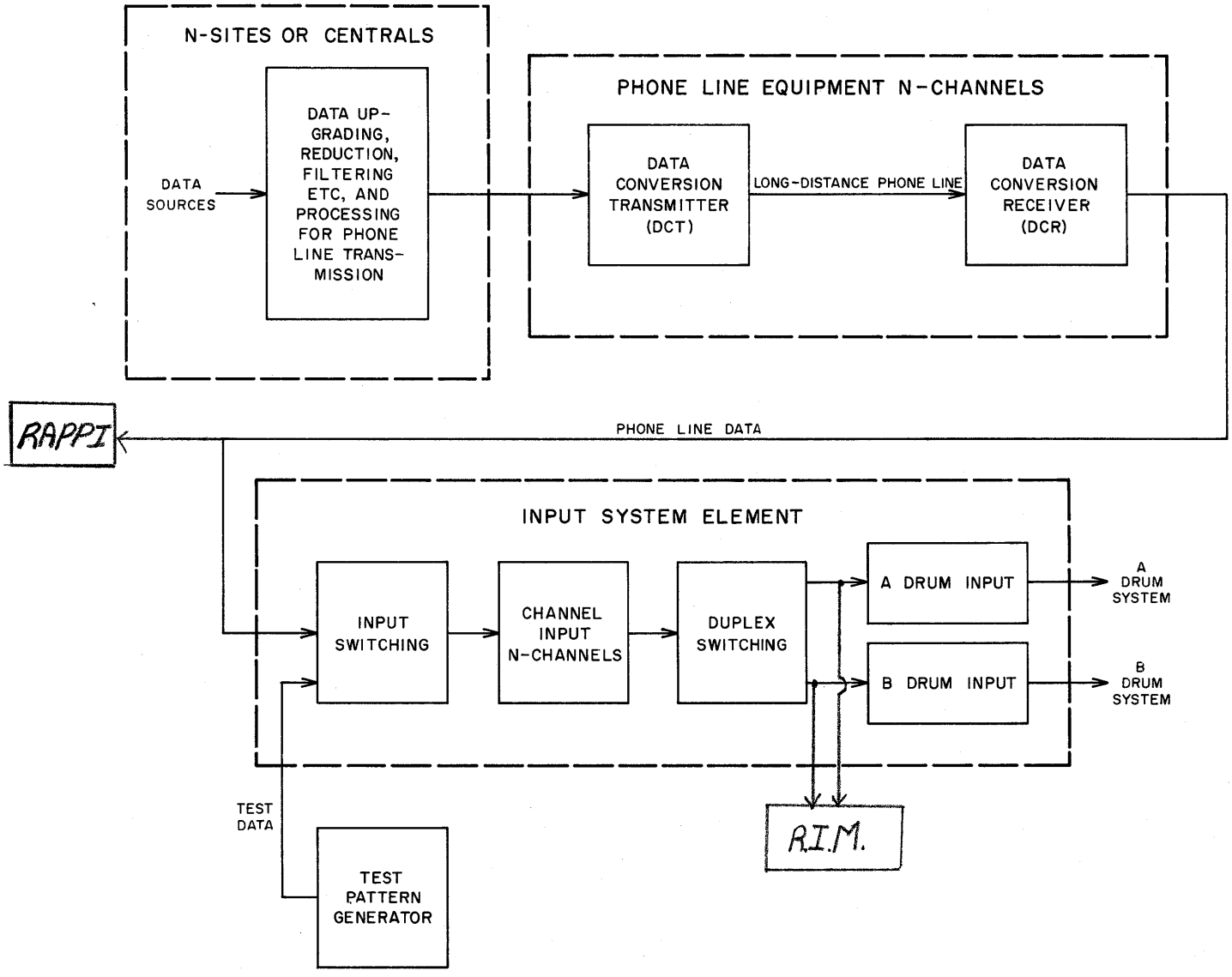


Figure 1–3. Typical Input System Element and Data Flow

pattern generator) for active, or phone line, data, and also permits the substitution of a spare channel for any other channel. Data is then transferred to the channel input section. The channel input section consists of many portions of identical circuitry, one for each channel. In each channel, the incoming data is processed: synchronized with drum timing, checked for parity in the case of LRI and XTL data, filtered in the case of GFI data, formed into drum words, and stored. A drum-demand pulse from the Drum System (signalizing empty storage space) senses each channel in order of pre-established priority for stored data and causes its parallel readout through duplex switching to the drum input section. The drum input section is common to all channels and is duplexed; duplex switching funnels data from channels in the active status to the active drum input section, and data from standby channels to the standby drum input section. The drum input section adds a site identity code to the message, identifying the origin of the data, and transfers the message without delay to the Drum System; in the LRI and XTL elements, the time of transfer relative to computer time and the parity of each drum word are also added to the message. Thus the data from channel after channel is processed cyclically in step with drum timing.

3.2 LRI DATA

The LRI element provides a maximum of 36 channels of which 4 are spare. Two channels are required to service the normally equipped P-site: one channel processes radar search and MX X IFF data, the other channel processes height-finder data. Thus, a maximum of 16 P-sites may be served.

All types of LRI data (par. 2.1) arrive at the LRI element in basically the same format, entering the element on three lines: timing, sync, and data. The timing frequency is 1,300 cps. The sync and data input together form a 52-bit message. A busy bit, always a 1, on the data line begins the message; 46 data bits (combinations of 1's and 0's) follow; the message concludes with a 0 0 sync bit 0 0 pattern.

In the channel input section the message is divided into two words, the parity of each is checked to assure accuracy of reception, and the two words are stored to await a drum-demand pulse. The drum-demand pulse initiates readout of the two words through duplex switching and the drum-input (common) section to a slot on the LRI drum field. As the message passes through the drum-input section, a 4-bit site identity code is added to the first word, identifying the channel which processed the message; a 5-bit clock time code is added to the second word, indicating the time, relative to computer time, that the message was transferred to the Drum System; and a parity bit is added to each drum word.

3.3 GFI DATA

The GFI element provides a maximum of 18 channels of which two are spare. Each operational channel serves one radar site.

Inputs to each channel, on three lines designated azimuth and north azimuth, range, and target, are described below:

a. Azimuth and north azimuth: A complete revolution (360 degrees) of a gap-filler radar is divided into 256 equal parts, called azimuth sectors. Each time the gap-filler radar completes an azimuth sector, a single cycle of a 1,600-cps sine wave appears on the azimuth and north-azimuth input line. When the gap-filler radar antenna passes through north, two successive cycles of a 1,600-cps sine wave appear on the azimuth and north-azimuth input line. The number of azimuth signals received after a north-azimuth signal therefore indicates the angle of rotation past north traversed by the radar antenna.

b. Range: The radar scan for each azimuth is divided into a maximum of 64 range boxes. The range input is a continuous 1,600-cps sine wave, with each cycle indicating a single range box. The number of range cycles after each azimuth signal therefore indicates the distance that has been scanned for the particular azimuth.

c. Target: A target signal consists of a single cycle of a 1,600-cps sine wave whenever a target return is received by the radar.

It may be seen from the above, that GFI inputs, unlike LRI inputs, do not compose a message giving a binary description of the target. Instead, information is in comparatively crude form and must be processed into such a message. First, unwanted target data must be eliminated, a step omitted at the gap-filler radar site for lack of manual filtering facilities. This step is performed at a mapper console, one of which is provided for each GFI channel. The azimuth signal drives the mapper in synchronism with the gap-filler radar antenna and the north-azimuth signal is used to check and, if necessary, correct this synchronism. The target signal develops target indications on the mapper scope in a PPI type of display. Thus each mapper provides a PPI survey of the area covered by a gap-filler radar site. At the mapper, an operator manually opaques all areas or targets of no operational interest. Unopaqued, or filtered, target indications are picked up by photoelectric devices. Meanwhile, the channel circuitry maintains a count of azimuths since the previous north-azimuth signal and a count of range signals since the previous azimuth signal. Each filtered target releases these counts in the form of a message giving range and

azimuth of the target in binary. The message is stored. A GFI drum-demand pulse senses each channel, in order of pre-established priority, for a stored message, and initiates readout of the message through duplex switching to the drum-input or common section. There, site identity is added and the message transferred, undelayed, in the form of one drum word to the Drum System.

3.4 XTL DATA

The XTL element provides a maximum of 24 channels, of which two are spare (in certain Combat Direction Centrals the maximum is 12 channels, one of which is spare). Inputs and data processing are similar to those of the LRI element. The input to each channel is on three lines, designated timing, sync, and data. The timing signal is a continuous 1,300-cps sine wave. Information is in binary message form, each message totaling 92 bits. A sync bit, a single cycle of the timing frequency, is transmitted at the beginning of the message, two 0's follow; then there are 85 data bits, in synchronism with the timing frequency, with each 1 bit represented by a single cycle of the timing frequency and each 0 bit by a missing cycle. Four 0's conclude the message.

The 85 data bits are regarded as divided into five message words of 17 bits each. The 17th bit is a parity bit; parity for each word is even. The five words are interleaved in the transmitted message. That is, the first bit of each of the five words are transmitted sequentially as bits 1, 2, 3, 4 and 5 of the message; the second bit of the five words follow as bits 6 through 10, etc. Within the channel, the five message words are sorted out into their original (pre-interleaved) form and the parity of each word is checked. The message address is in the fourth word. Since messages are sent on a party-line basis, the address is checked to ascertain whether the message is addressed to the receiving Central (or to all Centrals). If such is the case, and the parity of all words is correct, the message is stored in the form of three drum words. The XTL drum-demand pulse, sensing the channels for stored data, initiates readout of the message to the drum-input or common section. There, site-identity and time relative to computer time are added to the first drum word, parity bits are furnished for each drum word, and the complete message is transferred to the Drum System.

CHAPTER 4
MONITORING AND TEST EQUIPMENT

4.1 LONG-RANGE RADAR INPUT MONITOR C-2021/FSQ

LRI messages in transit to the Drum System (par. 3.2) are also made available to the LRI monitor. The LRI monitor provides the means for selecting LRI data for display. It thus enables operating personnel to make preliminary analyses of LRI coverage and data independently of the Central Computer, and it assists maintenance personnel to evaluate the operational efficiency of the Input System.

The LRI monitor consists of four display consoles, units 620, 621, 622, and 623, and the LRI monitor control unit, unit 93, which contains the circuits that serve all four consoles. LRI messages are selected for display by means of keyboard controls at the consoles or, in the case of units 620 and 621, at an auxiliary control console, unit 947. The following selection principle is employed. Each processed LRI message contains a message label indicating whether the message contains search, MK X IFF, or height-finder data, and a site identity code (added in the drum-input section) indicating the source of the data. An operator selects a message or messages for display by using the keyboard controls to specify the message label and site identity of interest to him. The target information in the selected messages is then presented, in PPI form, on the cathode-ray tube (CRT) of the display console at which, or for which, the display was requested. Unit 621 is camera-equipped to record the display at this console; the camera itself is controlled at unit 947.

Functionally, the LRI monitor consists of four sections: digital, analog, display, and switching. The digital section accepts the LRI message, determines whether it has been selected for display by comparing its message label and its identity with requests expressed at keyboard controls, and begins the processing of the target information in selected messages. The analog section transforms the digital target information into analog form. The display section presents the target information in a PPI display on one or more of the CRT screens. The switching section contains the circuitry used to express message selections to control the operations of the camera and to associate the consoles with either the active or the standby duplex machine.

4.2 TEST PATTERN GENERATOR TS-923/FSQ

4.2.1 General

Test Pattern Generator TS-923/FSQ is provided to generate test signals simulating the phone-line inputs to the Input System. The equipment is essentially three test pattern generators serving the LRI, XTL, and GFI elements. By means of a switch associated with a channel, signals from the appropriate TPG may be substituted for the phone-line inputs to the particular channel. Providing a known and controlled input to the various channels, the TPG offers the means of thoroughly checking the operation of an element during installation and subsequent to it.

4.2.2 Test Signals

4.2.2.1 LRI TPG Signals

The test signals generated by the LRI TPG go out on three lines: timing, sync, and data. The timing signal is a continuous 1,300-cps sine wave. The sync and data signals are individual sine waves generated in synchronism with the timing signal, together they form the message, the composition of which may be varied manually or by computer command.

4.2.2.2 XTL TPG Signals

The XTL TPG signals and messages are similar to those employed for the long-range radar input.

4.2.2.3 GFI TPG Signals

The test signals generated by the GFI TPG go out on three lines: range, azimuth and north azimuth, and target. The range signal is a continuous 1,600 cps sine wave. The azimuth and target signal are individual sine waves generated at regular intervals in synchronism with the range signals. Two azimuth signals at successive range cycles form the north-azimuth signal.

The GFI TPG is capable of advancing or delaying the north-azimuth signal by a varying number of azimuths (early north and late condition respectively), of causing azimuth signals to be omitted following the north-azimuth signal (missing azimuth condition), and of inserting extra or spurious signals after the north-azimuth signals.

Targets may be generated in various patterns. Certain patterns are called ring patterns because the targets appear as a ring on a PPI type of display (such

as a mapper console). Other patterns are called blanket-coverage since they place a target indication in all but a few of the hypothetical range boxes (par. 2.2.2) in the GFI type of display.

4.2.3 Physical Description

The TPG is housed on unit 92, with the exception of certain controls located in the TPG module of the simplex maintenance console. Unit 92 comprises four modules, one each for the LRI, XTL, and GFI TPG's, and a utility module. The TPG module of the simplex maintenance console contains three control panels, one each for the LRI, XTL, and GFI TPG's.

4.2.4 Modes of Operation

4.2.4.1 General

Incorporated in all three TPG's are controls for operating the TPG manually and circuitry which processes instructional pulses from the Central Computer in automatic or semi-automatic operation. The relative extent of manual, or computer control is determined by the mode or mode-type in which the TPG is operated. These modes and mode-types have been developed in response to maintenance needs. For example, manual control is frequently necessary for troubleshooting, while computer control is required for programmed maintenance. These modes and mode-types are described below.

4.2.4.2 LRI and XTL TPG's

The LRI and XTL TPG's may each be operated in mode I, mode II, or in feedback loop. In mode I the LRI and XTL TPG's are completely under manual control. Specifically, start-stop operation and composition of the message (pattern of data bits) are manually controlled. Mode II is differentiated into types 1 and 2. In type 1, the TPG is completely under computer control; each message is initiated and composed by computer commands. In type 2, messages are initiated by computer command but manually composed. Feedback loop is a special type of operation in which the TPG serves as a link to feed back messages from the Output System to the Input System for test purposes. The ground-to-air section of the Output System is linked to the LRI element through the LRI TPG; the ground-to-ground section to the XTL element through the XTL TPG.

4.2.4.3 GFI TPG

The GFI TPG may be operated in mode I or mode II. In mode I operation, the GFI TPG, like the LRI and XTL TPG's, is completely under manual control. Start-stop operation and the signal variations, target pattern, length of azimuth cycle (number of azimuth signals between north azimuths), early-north and late-north conditions, etc., are manually controlled. Mode II operation is subdivided into three types. In type 1, the GFI TPG is completely under computer control. In type 2 operation, the GFI TPG is manually controlled except for the length of the azimuth cycle which is set in type 1 operation and carried over into type 2. On computer command, type 2 operation will revert to type 1. In type 3 operation, the GFI TPG is under manual control in all respects, except one: upon computer demand it will revert to type 1 operation.

The various types of mode II operations have been developed to increase the flexibility of maintenance programming.

CHAPTER 5
SIMPLEX MAINTENANCE CONSOLE

5.1 METHOD OF PRESENTATION

Though the simplex maintenance console unit 47 (fig. 1–4) is not physically part of the Input System, it is largely used for control and monitoring of Input System equipment. A general description of this equipment is therefore included in this manual. For details of circuit operation refer to the portion of this manual, or of other manuals, describing the equipment to which the control or monitoring circuit is related. For example, the circuits of the simplex maintenance console involved in the control of the simplex power supplies are described in 3-82-0, *Theory of Operation of Power Supply System for AN/FSQ-7 Combat Direction Central and AN/FSQ-8 Combat Control Central.* The circuits permitting selection of phone-lines or test inputs to the LRI channels are discussed in Part 2 of this manual (in connection with input switching).

5.2 PURPOSE OF EQUIPMENT

The simplex maintenance console, unit 47, provides centralized facilities for controlling the operation of the simplex equipment in the Combat Direction Central. Specifically, it performs the following functions:

a. Controls the power cycling of the two simplex power supplies.

b. Supplies control facilities for marginal checking of simplex equipment.

c. Controls the operation of channel equipment of the Input System, providing the following types of control:

1. Connects the channel to the active or standby computer and simplex power supply.
2. Selects the source of the inputs (phone line or test) to the channel, as desired.

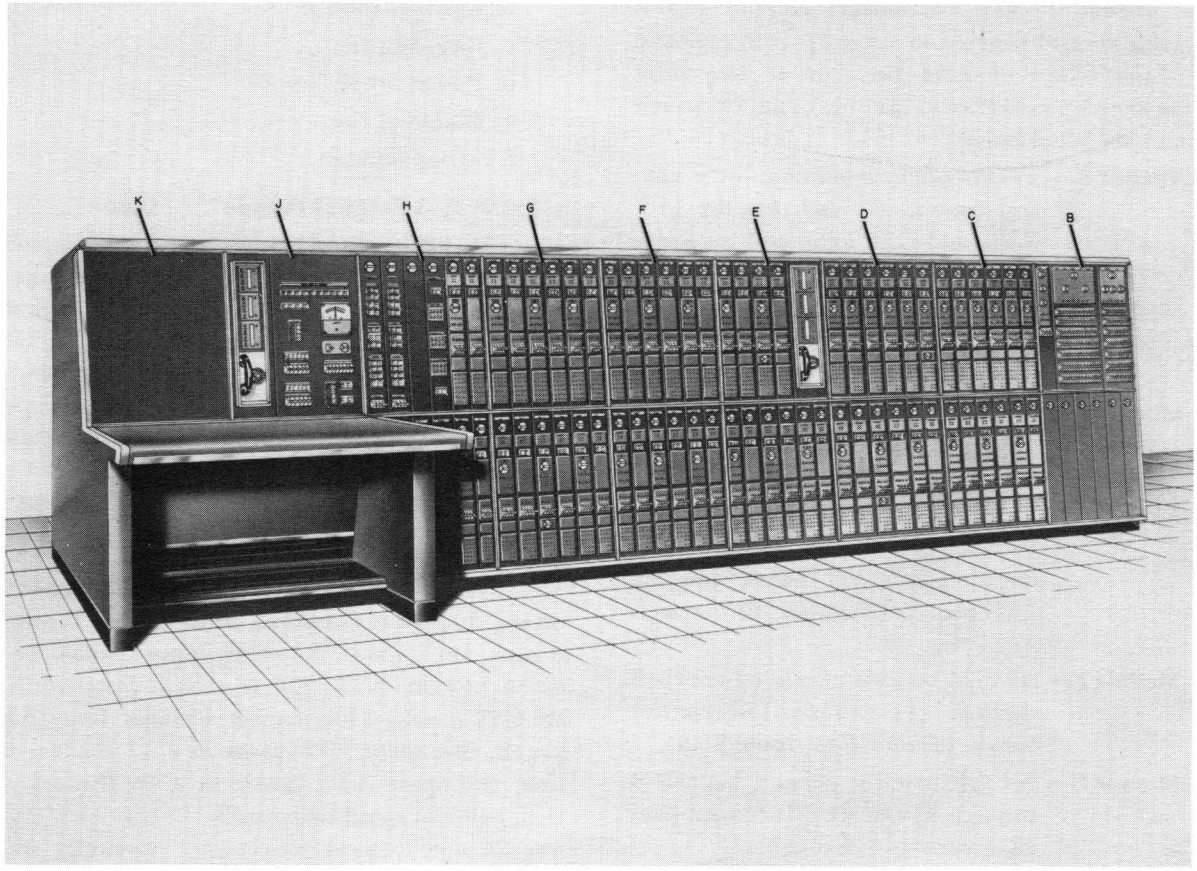


Figure 1–4. Simplex Maintenance Console (12 XTL-Channel Installation)

3. Provides various alarms and indicators to monitor the channel power supply connections, inputs, and signal processing.

d. Provides alarm indications and connection indications for computer entry punches (Display System).

e. Shares control of the TPG's with the control facilities on the TPG, unit 92.

f. Provides maintenance intercommunication facilities, and will eventually provide centralized scope-and-probe facilities.

5.3 PHYSICAL DESCRIPTION

5.3.1 Differences between Systems

The simplex maintenance console varies somewhat in different installations. In the present installations the simplex maintenance console consists of nine modules, but in the 24th installation and in all Combat Direction Centrals subsequent to that it is expanded to 10 modules to accommodate an increase from 12 to 24 in the maximum number of XTL channels. The present simplex maintenance console is described below; a description of the expanded equipment follows.

5.3.2 Present Systems

The present simplex maintenance console utilizes 72 pluggable control panels and 3 fixed panels, mounted in 9 modules. These modules (in right to left order facing the simplex maintenance console) and the panels they mount are listed below:

a. Module B — TPG module mounting three control panels, one each for the LRI, XTL, and GFI TPG, and six blank panels.

b. Module C — Six XTL control panels (for channels 7 through 12) and six LRI panels (channels 31 through 36).

c. Module D — Six XTL control panels (channels 1 through 6) and six LRI control panels (channels 25 through 30).

d. Module E — Four GFI control panels (channels 15 through 18), one telephone (intercommunication) panel, and six LRI panels (channels 19 through 24).

e. Module F — Six GFI control panels (channels 9 through 14) and six LRI control panels (channels 13 through 18).

f. Module G — Six GFI control panes (channels 3 through 8) and six LRI control panels (channels 7 through 12).

g. Module H — Two GFI control panels, one computer entry punch (CEP) panel, one blank panel, two power supply panels (channels 1 through 6).

h. Module J — One marginal check control panel.

i. Module K — Centralized scope and probe facilities (not available at present).

5.3.3 Future Systems

In the 24th installation and in subsequent Combat Direction Centrals, a 10th module, module A, is added to the right of module B. This module and module B are then used as follows.

a. Module A — Six XTL control panels (channels 19 through 24) in the upper section and the three TPG control panels in the lower section.

b. Module B — Six XTL control panels (channels 13 through 18) and six spare panels.

None of the other modules, C through K, are affected by this modification.

5.4 FUNCTIONAL DESCRIPTION

5.4.1 General

For purposes of discussion, the panels are grouped as follows:

a. TPG control

b. Channel control

c. CEP control

d. Power supply control

e. Marginal check control

f. Miscellaneous

5.4.2 TPG Control Panels

The TPG control panels are described and illustrated in Part 6 of this manual, which pertains to the TPG; refer also to 4.2 of this part for a brief description of this equipment. All three panels, LRI, GFI, and XTL, contain power switches and indicators, and a TEST switch, for selecting the TPG mode of operation. In addition, the LRI and XTL panels contain the BIT SELECTION switches which determine the composition of the test messages generated by these TPG's.

5.4.3 Channel Control Panels

Channel control panels compose the greatest part of the simplex maintenance console. One control panel is provided for each automatic input channel or a total of 36 LRI, 12 XTL, (24 in certain installations), and 18 GFI panels. This number includes four spare LRI panels, one spare XTL panel in a 12 channel installation, two spare XTL panels in a 24 channel installation, and two spare GFI panels.

Channel control panels vary physically and functionally, depending on which input element they are associated with, whether they serve odd-numbered or

even-numbered channels, and whether they are spare. However, there are certain basic similarities in these panels.

With the exceptions noted, the channel control panels are made up of six sections: panel connector, alarm, power, data circuit, channel selector, and neon. The channel connector section contains a 156-pin connector which makes all connections to the panel and mounts it. The alarm section provides visual and aural indication of an alarm condition (such as a parity error) in channel operation. The power section is found in all XTL panels, but only in the odd LRI and GFI panels where each power control section services odd and even channels. The power section contains the UNIT STATUS switch, which associates a channel (or pair of channels) with the active or standby computer, with the active or standby simplex power supply, and also related indicators. The data circuit section is used to select the source of the input (phone-line or test) to the channel and contains related indicators. The channel selector section is found only in spare channel panels and is used to select the panel or pair of panels for which the spare panel will be substituted. The neon section mounts neon indicators showing the condition of various key flip-flops in channel circuitry.

5.4.4 CEP Control Panel

The CEP control panel contains three sections, one for each CEP in Combat Direction Central AN/FSQ-7. Each section furnishes the following power indications for its CEP.

a. A-B SIGNAL CONTACTORS CLOSED: indicates the computer A or B, to which CEP is supplying data.
b. C-D POWER CONTACTORS CLOSED: indicates the simplex power supply, C or D, furnishing power to the CEP.
c. C-D CIRCUIT BREAKER ALARM: indicates an open circuit breaker in the simplex power-supply circuits furnishing power to the CEP.

The RESET AUDIBLE ALARM pushbutton is found in the lower part of the panel.

5.4.5 Power Control Panels

There are two power control panels, one for each simplex power supply. The panels provide the switches and related indicators and alarms for cycling up power to one or the other simplex power supply.

5.4.6 Marginal Check Panel

The marginal check panel is a fixed panel constituting the marginal check module. It contains all the controls and indicators necessary to control marginal checking of simplex equipment.

5.4.7 Miscellaneous Panels

Miscellaneous panels include the two phone stations used for maintenance intercommunication and blank panels to provide for expansion of facilities.

PART 2
LONG-RANGE RADAR INPUT ELEMENT

CHAPTER 1
INTRODUCTION

1.1 GENERAL

This part presents the theory of operation of the long-range radar input element (LRI). Because the LRI element is an intermediate processing link between a source of information and other systems of the equipment, some functions of other systems are discussed, but only to the extent necessary to describe the operation of the LRI element.

1.2 FUNCTION OF LONG-RANGE RADAR INPUT ELEMENT

The LRI element receives messages from up to 16 permanent long-range radar (P) sites, and processes the messages for subsequent presentation to the Central Computer System via the Drum System.

1.3 RELATIONSHIP OF LRI ELEMENT TO SOURCES OF INFORMATION

A block diagram illustrating the flow of LRI data from a P site to the LRI drum field is shown in figure 2–1. The data flow for all 16 P sites is identical to that illustrated for the single P site.

A radar P site contains three radar units, each originating different information:

a. A long-range search radar set producing target coordinate information in fine grain data (FGD) form.

b. Mark X identification friend or foe (IFF) radar with a selective identification feature.

c. A semiautomatic height-finder radar producing height-above-ground data for each target.

In normal operation, as shown in figure 2–1, each P-site sends data to two LRI channels. The two channels will be an odd and even pair such as channels 1-2, 3-4, 29-30, or 35-36. The data sent to one of the two channels will be search radar and Mark X information. All

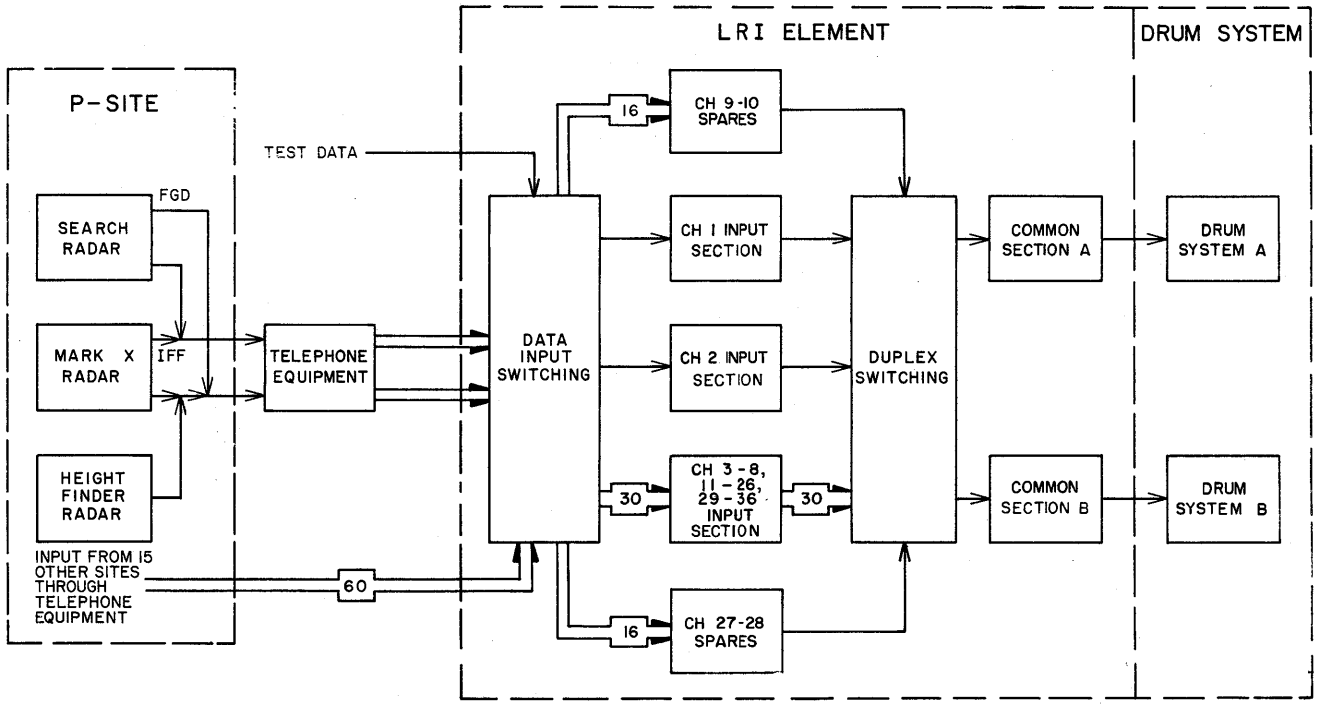


Figure 2–1. LRI Information Flow, Simplified Diagram

three types of messages are sent to the other channel. The output of the P-site intended for an odd channel is sent to two digital data transmitters (DDT's) and is then transmitted over separate phone lines to the Central. Therefore, an odd channel receives identical information over two input lines (designated circuit 1 and circuit 2). Similar circuitry exists for the even channel to receive information. If a P-site sends information to a Central for use only during the expanded mode of sector operation, only one phone line (circuit 1) will feed the odd channel and only one phone line circuit (circuit 1) will feed the even channel. The information flow through the LRI element to the Drum System is also shown in figure 2–1 and is discussed in 1.6.

1.4 PHYSICAL DESCRIPTION

The LRI element is contained in unit 41, shown in figure 2–2. This element contains 18 modules of simplex channel equipment and six modules that are evenly divided between two duplex common equipments. Three of these common equipment modules are associated with computer A and three with computer B.

Controls for the simplex channel equipment are located on the simplex maintenance console (unit 47). Indicators for the duplex equipment are located on the associated duplex maintenance console (unit 1A or 1B).

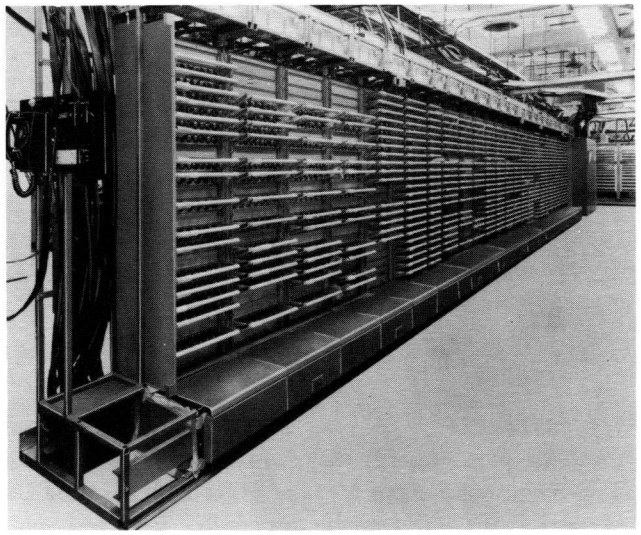
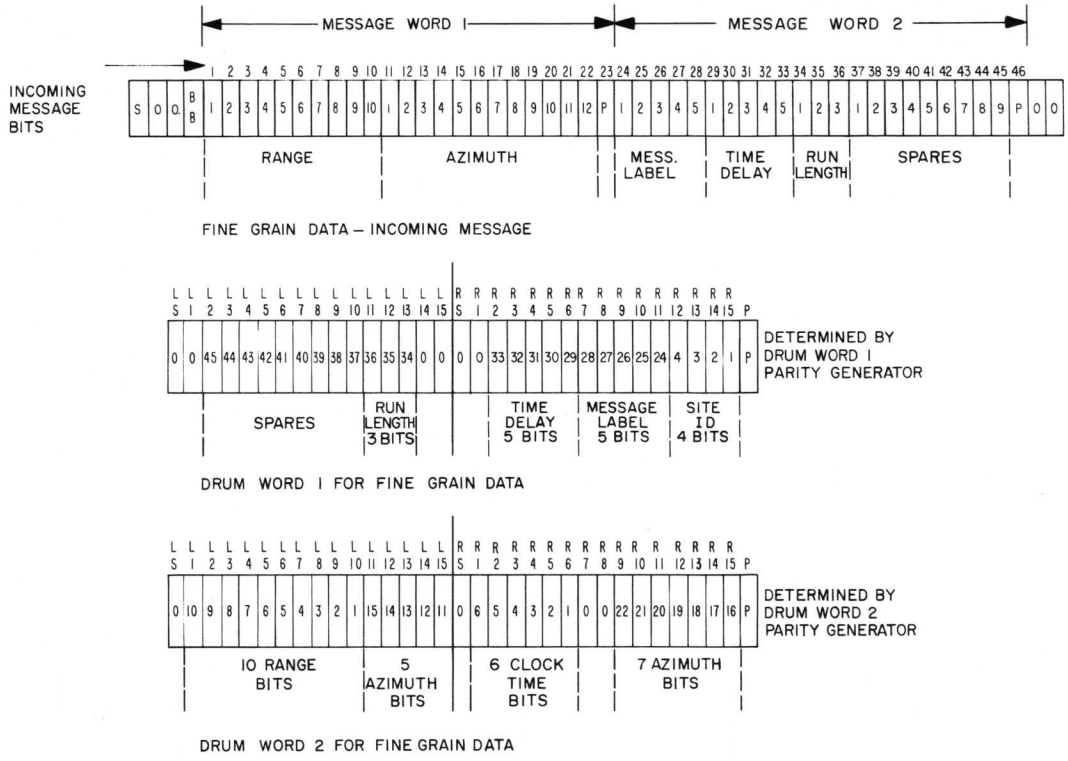


Figure 2–2. LRI Unit 41

1.5 MESSAGE AND DRUM WORD LAYOUT

The LRI element receives three types of messages from each P site. Each type of message contains data bits which are received by the LRI element in serial form. Each message consists of two message words. The order of reception, the data content of each message, and the drum words derived from each message are



NOTE: NUMBERS IN DRUM WORDS REFER TO INCOMING MESSAGE BIT NUMBER EXCEPT FOR SITE IDENTITY AND CLOCK TIME NUMBERS.

Figure 2–3. Message and Drum Word Layout, Fine Grain Data Message

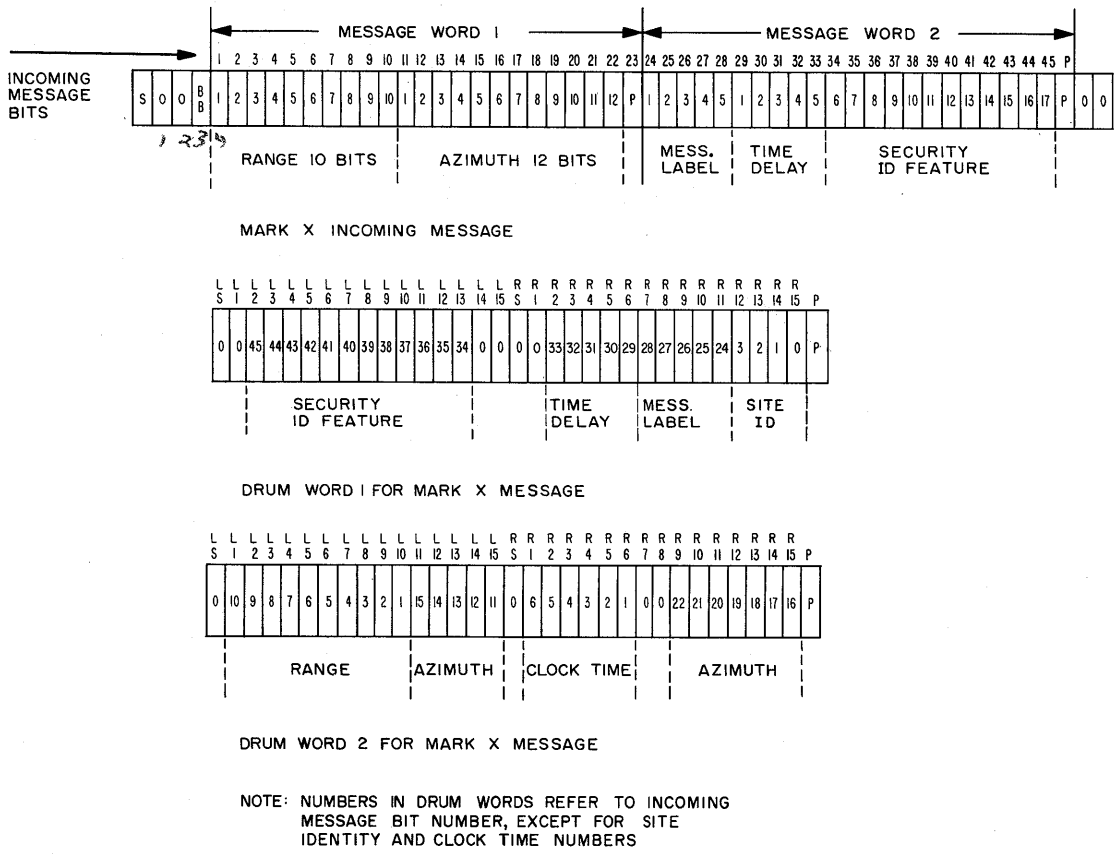


Figure 2–4. Message and Drum Word Layout, Mk X Message

shown in figures 2–3, 2–4, and 2–5. Each of the three types of messages starts with a sync bit, two 0 bits, and a busy bit (BB). The busy bit is always a 1 bit indicating the start of message data. Two message words follow the busy bit and a parity bit follows each message word. The message ends with two 0 bits. The site identity, clock time, and drum word parity (shown in the drum word layouts) are incorporated as the words are transferred to the Drum System.

1.5.1 Fine Grain Data Message

Each FGD message contains the following items of target information in binary form.

a. Range from the radar site.
b. Azimuth relative to true north, from radar set.
c. Time delay between initial detection of the target and transmission of the message (5 bits).
d. Run length indicative of the size of targets or existence of multiple targets at the reported location (3 bits).
e. Message label which identifies the type of message, whether FGD, IFF, or height finder.

1.5.2 MK X IFF Message

The MK X IFF message contains the following binary data:

a. Range from radar site (10 bits).
b. Azimuth from true north at radar site (12 bits).
c. Message label indicating type of message (FGD, IFF, or height finder) (5 bits).
d. Time delay between initial detection and transmission of the target (5 bits).
e. Security identification feature of target (12 bits).

1.5.3 Height-Finder Message

The height-finder message contains the following binary information:

a. Number of aircraft (3 bits)
b. Separation of aircraft (2 bits)
c. Formation of aircraft (2 bits)
d. Special reply (3 bits)
e. Request number (3 bits)
f. Address (1 bit)
g. Height (8 bits)
h. Message label (5 bits)

1.6 GENERAL FUNCTIONAL DESCRIPTION

The LRI element is shown in block diagram form in figure 2–6. The element consists of an input switching section, a 36 channel input section (only one is

shown), a duplex switching section and a duplex common section. These sections are discussed briefly below and in detail in separate chapters.

1.6.1 Input Switching

The input switching section contains the controls, indicators, relays, and associated circuitry necessary to perform the following functions.

a. Establish the status, active or standby, of each channel.

b. Apply incoming phone line data to active channels and test data to standby channels when desired.

c. Substitute a spare channel for a regular channel when desired.

d. Provide indications at the simplex maintenance console to monitor the above functions.

1.6.2 Channel Input Section

The channel input section serially receives the LRI message, performs certain operations on the message data (such as synchronization, separation of two message words, etc.), and stores the message. When a drum slot becomes available, the LRI message is transferred from the channel input section, through the associated common section, to the Drum System. The process of transferring messages out of the channel section is designated readout and is performed in a parallel manner, with message word 2 being read out first, followed by message word 1. Channel readout is performed one channel at a time with the order of readout determined by a priority sensing system of drum-demand pulses.

1.6.3 Duplex Switching Section

The duplex switching section transfers the output of the channel input section to the proper common section (A or B) depending on the status, active or standby, of the channel and of the A and B computers. Information from channels in the active status is transferred to the common equipment associated with the active computer. Information from channels in the standby status is transferred to the common equipment associated with the standby computer. In addition, certain pulses and levels are transmitted through duplex switching from common A and B to the appropriate channel input sections. Some signals (such as readout alarm) are transmitted in the opposite direction (i.e., from channel input to the common equipment).

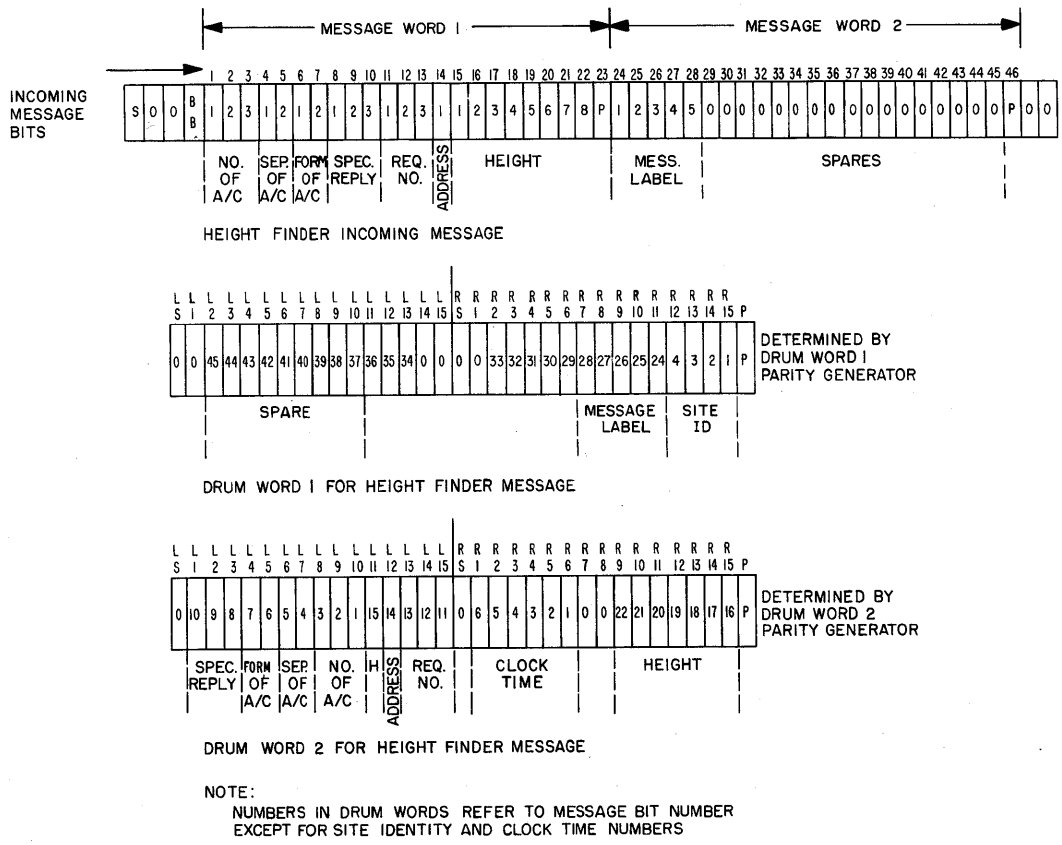


Figure 2–5. Message and Drum Word Layout, Height-Finder Message

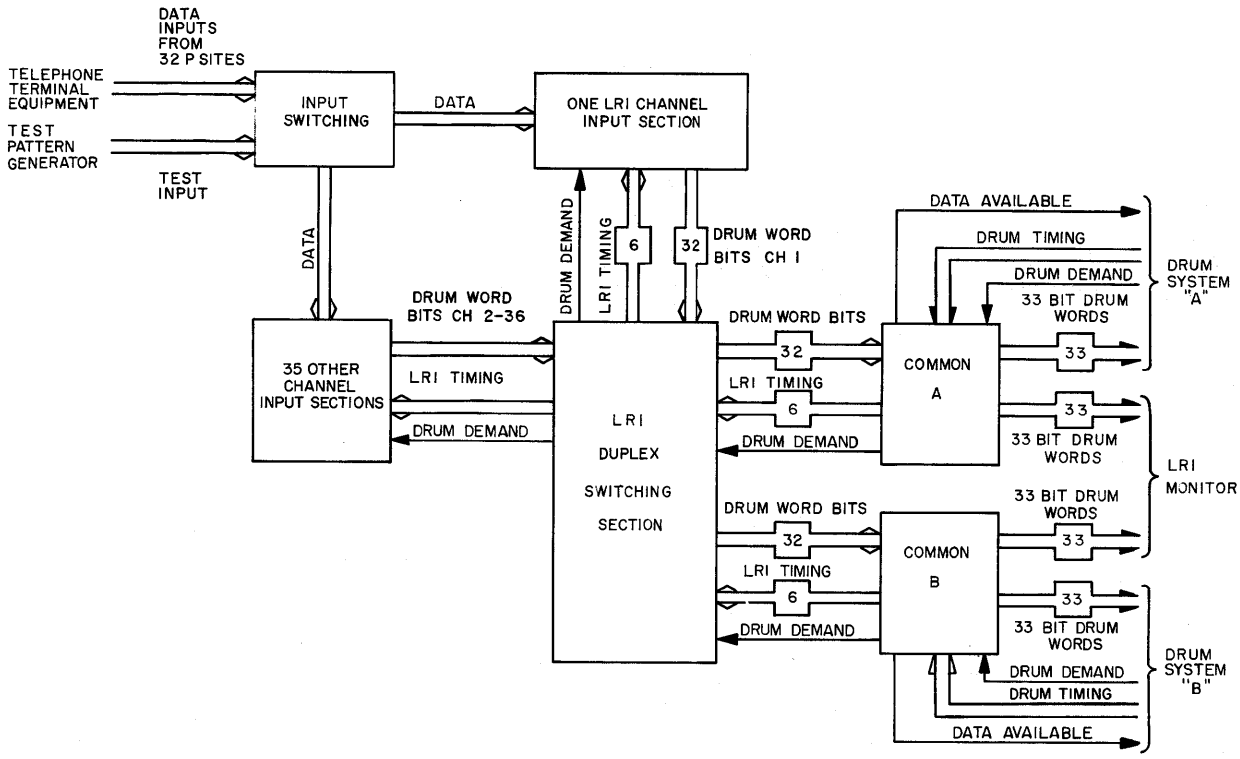


Figure 2–6. LRI Input Element, Block Diagram

1.6.4 Common Equipment

The active common equipment receives the message words read out of all active channels. The common section then adds information to both message words and transfers, one at a time, the two message words plus added information to the Drum System as two 33-bit drum words. The information added to the message is clock time, site identity, and drum-word parity bits. Site identity and a parity bit are added to the first drum word, and clock time and a parity bit are added to the second drum word. The purpose of this added information is discussed in Chapter 5.

The common equipment also receives drum timing (OD) pulses and generates a group of LR pulses, which are synchronized with the OD pulses, for use in the channel input sections. The LR pulses are generated to obtain pulses of 20-μsec intervals that are synchronized with OD pulses (OD pulses occur at 10-μsec intervals). The LR and OD pulses synchronize operations of the channel input section with the Drum System operation, so that the data can be sent to the drum at the proper time.

1.7 SIMPLEX MAINTENANCE CONSOLE LRI CONTROL PANELS

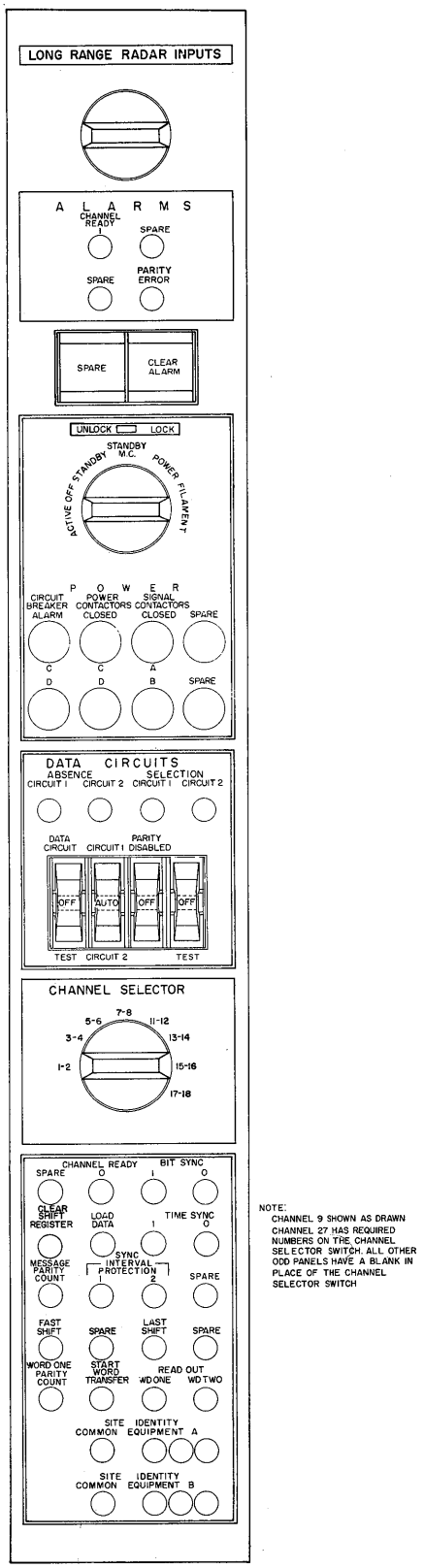
1.7.1 General

There are 36 LRI control panels located in the lower sections of modules C, D, E, F, G, and H of the simplex maintenance console (unit 47). The 18 odd panels (corresponding to channels 1, 3, 5, etc.) are made up of alarm, power, data circuit, and neon indicator sections. Two of the odd panels (9 and 27) are spare and contain a channel selector section in addition to sections common to all odd panels. The remaining panels (corresponding to channels 2, 4, 6, etc.) are made up of alarm, data circuit, and neon indicator sections. Panels 10 and 28 are spare and are paired with odd panels 9 and 27 for spare channel selection. Figure 2–7 shows the panel for spare channel 9 and figure 2–8 shows a panel for an even (or even-spare) channel.

1.7.2 Function of LRI Control Panel Switches

The unit status switch in the power control section of each odd panel (fig. 2–7) determines the status (active or standby) of that channel and of the even channel with which it is associated. With the switch set to ACTIVE, the two channels which it controls are connected to the active computer. Only telephone line data can be processed when the switch is in the ACTIVE position. With the switch set to STANDBY (or STANDBY MC), the channels are connected to the standby position, and either telephone line data or test data may be processed.

There are four switches in the data circuit section of the panel: data source switch, data circuit switch,



NOTE:
CHANNEL 9 SHOWN AS DRAWN
CHANNEL 27 HAS REQUIRED
NUMBERS ON THE CHANNEL
SELECTOR SWITCH. ALL OTHER
ODD PANELS HAVE A BLANK IN
PLACE OF THE CHANNEL
SELECTOR SWITCH

Figure 2–7. LRI Control Panel, Odd and Odd-Spares

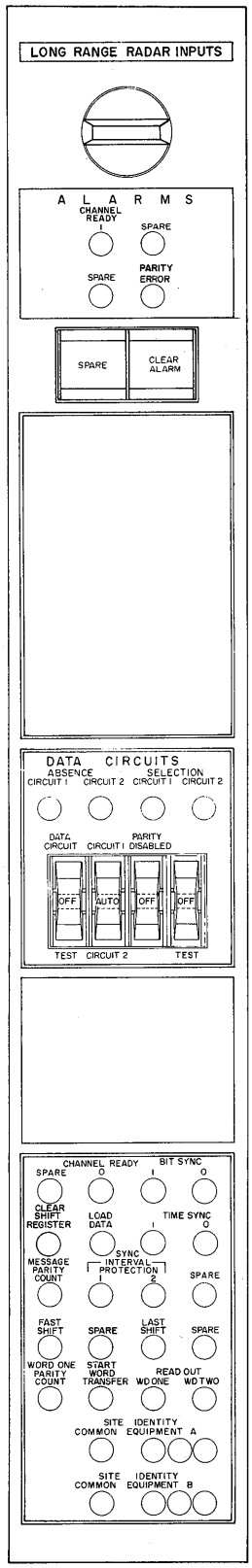


Figure 2–8. LRI Control Panel, Even and Even-Spares

PARITY DISABLED switch, and the TEST switch. In conjunction with the unit status switch (power section), the data source switch selects the source from which data is received. With the switch set to DATA CIRCUIT, the channel receives messages from P-sites over telephone line circuits. In the off position, the channel is inactive and data is not received. With the switch set to TEST, data is received from the test pattern generator to permit testing of channel operations in maintenance procedures. To prevent test data from entering the active computer, the test position of the switch functions only when the unit status switch (power control section) is set to STANDBY or STANDBY MC. The data circuit switch is used to select one of two telephone line circuits which feed data to the LRI channel. With the switch set to AUTO, telephone company equipment automatically selects the proper circuit. Either circuit may be manually selected by setting the switch to the CIRCUIT 1 or CIRCUIT 2 position. The PARITY DISABLED switch has two positions: off and PARITY DISABLED. In the off position, channel operation is normal (a message with incorrect parity is destroyed). In the PARITY-DISABLED position, test messages can be processed without regard to the parity of the message. The TEST switch, when set to the TEST position, checks the ability of a channel to prevent a readout if a malfunction causes the channel ready flip-flop to have an up-level output from both the 1 and 0 sides.

The CHANNEL SELECTOR switch, which appears on the panels corresponding to channel 9 and channel 27, electrically substitutes the spare channels for regular channels. Channels 9 and 10 can be substituted (as a 2-channel group) for channels 1 through 8 and channels 11 through 18. Channels 27 and 28 replace channels 19 through 26 and 29 through 36 when desired.

CHAPTER 2
INPUT SWITCHING

2.1 GENERAL

There is a maximum of 36 LRI channels at a Central, of which 32 are regular channels and four (9, 10, 27 and 28) are spares. Normally, two phone lines are provided for each channel in operation (refer to 1.3). Each phone line is connected to a Digital Data Receiver (DDR) and the outputs of each DDR are three lines designated timing, sync, and data. The group of three outputs from one DDR is designated circuit 1 and the group of outputs from the second DDR is designated circuit 2. Normally, the two circuits carry identical information. One circuit, selected by the data circuit switch (LRI control panel, simplex maintenance console), is connected to the channel. For example, when the data circuit switch for channel 1 is set to CIRCUIT 1, circuit 1 is connected to channel 1, and circuit 2 is connected to the spare channel. Setting the switch to CIRCUIT 2 connects circuit 2 to channel 1 and circuit 1 to the spare. When the switch is set to AUTO, telephone line equipment can cause the phone line feeding the active to be switched with the phone line feeding the spare channel. The switching takes place automatically if the active phone line develops trouble. Under normal operating conditions, circuit 1 feeds the active channel, and circuit 2 feeds the spare channel. If circuit 1 develops trouble, the phone line equipment automatically switches, causing circuit 2 to feed the active channel, and circuit 1, the spare channel. Circuit 2 will now continue to feed the active channel until a malfunction develops in circuit 2.

In addition to the telephone line circuits, a test circuit is available to each channel input section under control of input switching. The test circuit consists of three lines (timing, sync, and data) which are connected to the test pattern generator (TPG) through three test buses. When the source switch (LRI channel control panel, simplex maintenance console) is set to TEST, and the channel is in the standby status, the output of the LRI section of the TPG is applied to the channel input section. When the switch is in the DATA-CIRCUIT position, the telephone line input (either circuit 1 or circuit 2) is available to the channel input section.

The switching functions discussed above are performed by the input switching section, which also provides suitable monitoring at the channel control panels.

2.2 INPUT DATA SWITCHING

The data-input switching circuit selects either telephone line data or test signals from the LRI TPG as the inputs to be directed to each LRI channel. Figure 2–9 shows the relay switching circuits involved in selecting the input for channels 1 and 2. The relay switching circuits for any other pair of channels (except for spare channels) is the same as that shown for channels 1 and 2 on figure 2–9. For this reason, only channels 1 and 2 are discussed here.

When the channel 1 source switch (located on the simplex maintenance console) is set to the DATA CIRCUIT position, relay 41AT(K2) is energized and the telephone line inputs are connected to the data conversion receiver in channel 1. The telephone line inputs and test data inputs consist of data, sync, and timing lines but, for simplicity, shown on figure 2–9 as a single line.

When relay 41AT(K1) is energized, test data is connected to the data conversion receiver in channel 1. In order for this relay to be energized, two conditions must be met: (1) The unit status switch for channels 1 and 2 must be in the STANDBY or STANDBY MC position so that standby relay 41AR(K8) is energized. This relay controls the —48V return line for channel 1 test relay 41AT(K1) and channel 2 test relay 41AT(K4). (2) The source switch for channel 1 must be in the TEST position so that the control voltage will be applied to the channel 1 test relay.

The purpose of the standby relays is to prevent test signals from being sent to the active computer. The inputs for channel 2 are selected in the same manner as described above for channel 1.

2.3 SPARE-CHANNEL SWITCHING

2.3.1 General

Space-channel switching is the operation of electrically substituting a pair of spare channels (channels 9 and 10 or channels 27 and 28) for a pair of channels within a group. It is accomplished by setting the CHANNEL SELECTOR (fig. 2–10,A) switch (on the ODD spare channel control panels, simplex maintenance console) to the numbers of the channels to be replaced. Three functions are thereby performed.

a. The alternate telephone circuit for the replaced channel is connected to the spare channel.

b. The telephone-terminal-equipment indicators of the spare channel are substituted for these indicators on the replaced channel.

c. A write level generated in a spare channel is applied to the site can for the replaced channel. A write level causes readout of site identity by a site can to associate the source of a message with the message data. In spare-channel switching it is necessary to associate the site identity related with the replaced channel with message data processed by the spare channel.

In the discussion of *a* and *b* it is assumed that channels 9 and 10 are substituted for channels 1 and 2. Function *c* is discussed in Chapter 4.

2.3.2 Alternate Telephone-Line Switching

The alternate phone line circuit (circuit 1 or 2 whichever it is at any given moment) is connected to the contacts of alternate telephone line switching relays 41EH(K1) and 41EH(K2) (fig. 2–10,B). When the CHANNEL SELECTOR switch is set to position 1-2, these relays are energized, applying channel 1 telephone

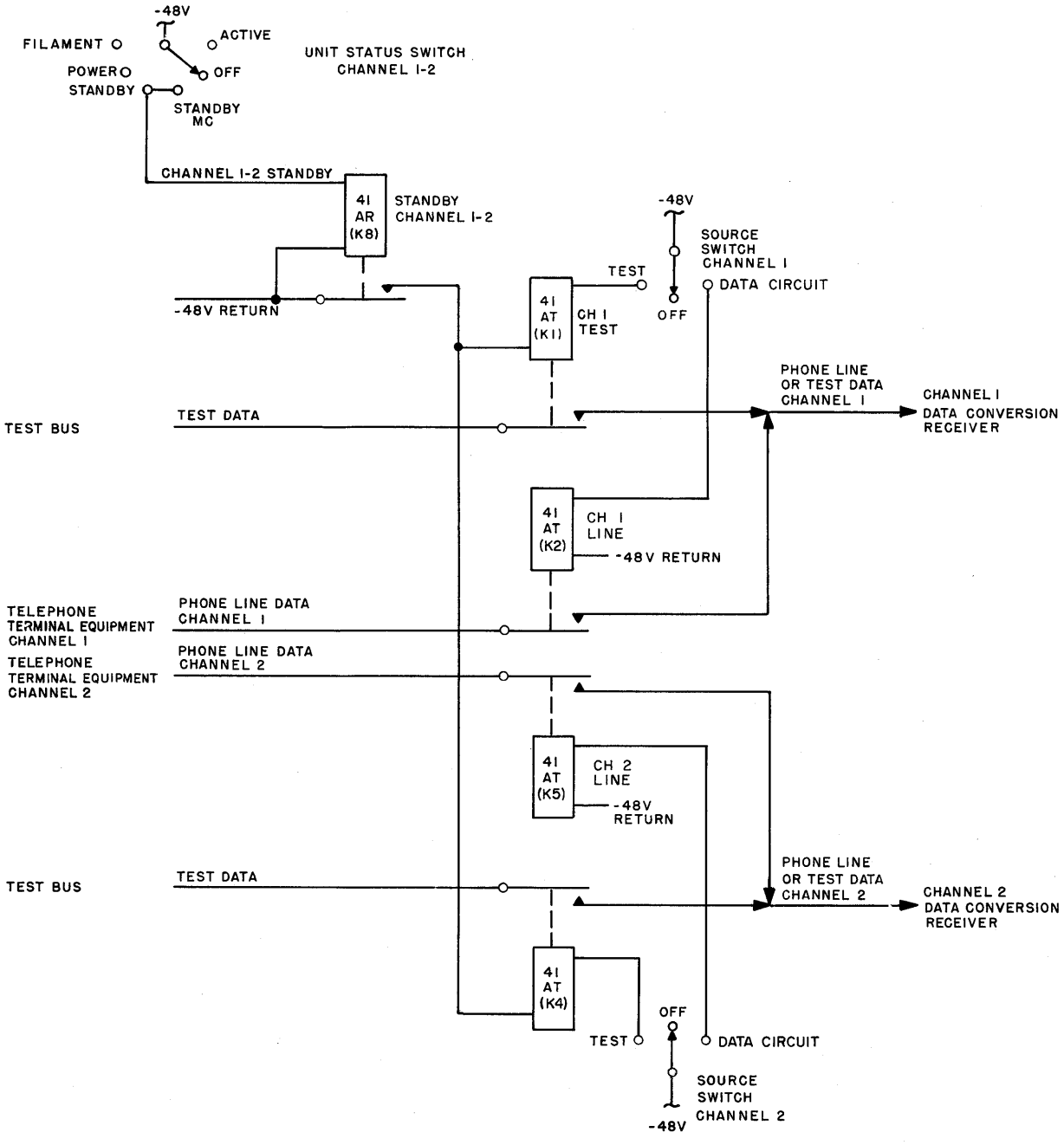
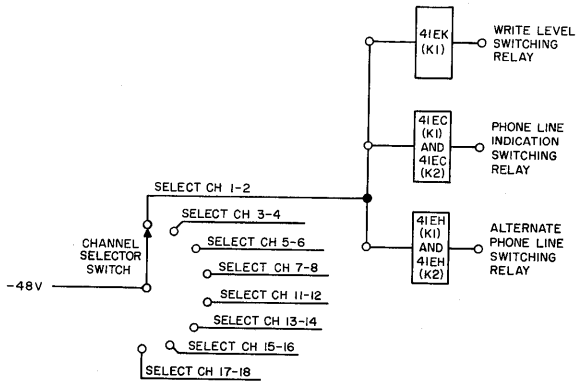
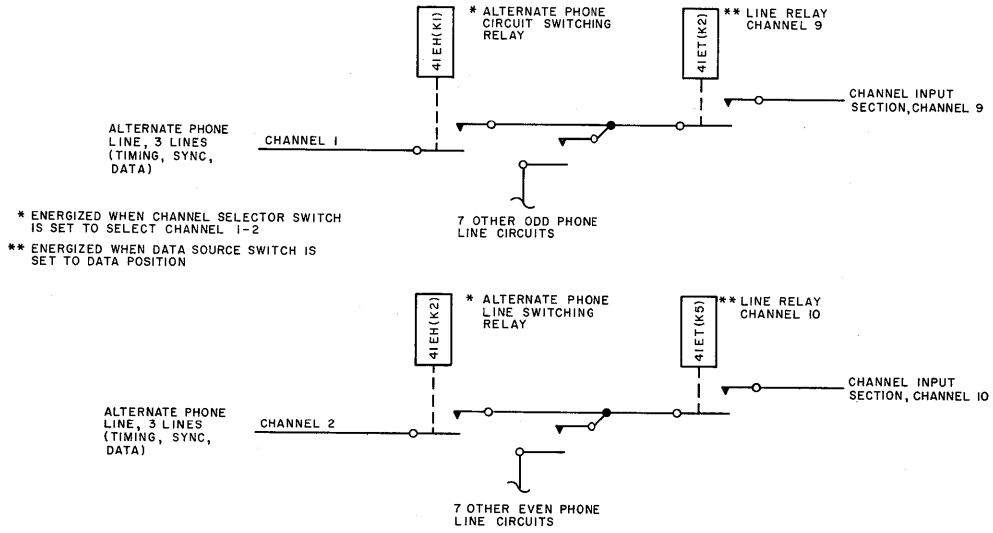


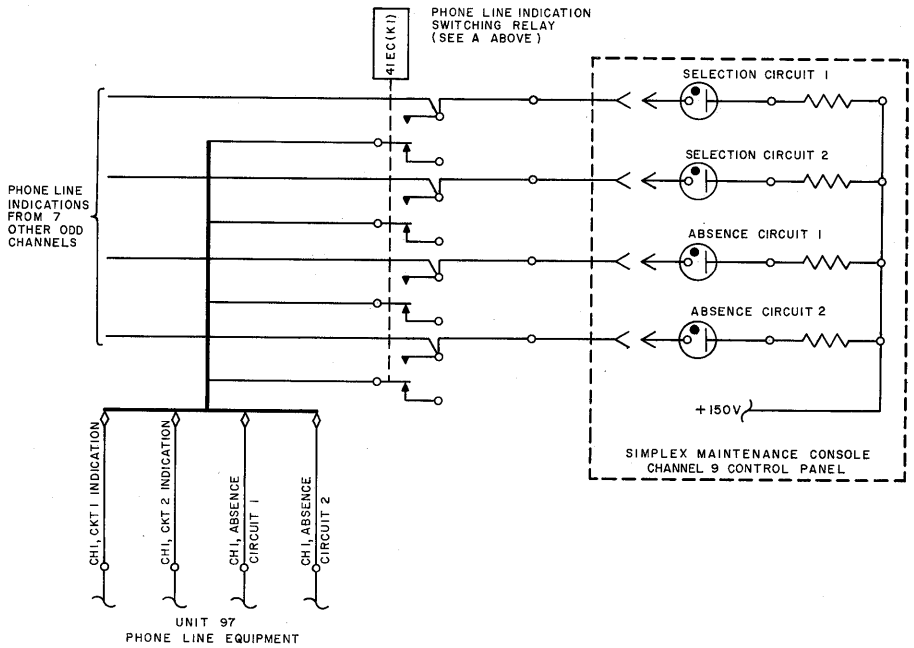
Figure 2–9. Input-Data Switching, Channels 1 and 2



A. OPERATION OF CHANNEL SELECTOR SWITCH



B. ALTERNATE PHONE LINE CIRCUIT SWITCHING



C. PHONE LINE INDICATION SWITCHING

Figure 2–10. Spare-Channel Switching

line data to the contacts of line relay 9 and channel 2 telephone line data to the contacts of line relay 10. If the source switch for channel 9 or 10 is set to DATA CIRCUIT, the line relay for that channel is energized, applying channel 1 telephone line data to channel 9 and channel 2 telephone line data to channel 10.

2.3.3 Switching of Basic Telephone Terminal Indications

Telephone line and terminal facilities are monitored to ensure proper operation of the Central. Each LRI control panel mounts indicators to show which telephone line circuit is connected to the channel input section (SELECTION, CIRCUIT 1, and CIRCUIT 2) and whether there has been a loss of data on a circuit (ABSENCE, CIRCUIT 1, and CIRCUIT 2). When a spare channel is substituted for another channel, the indicators on the spare channel are also substituted.

Placing the CHANNEL SELECTOR switch in position 1-2 causes relay 41EC(K1) to be energized. Four lines (fig. 2–10,C) from unit 97 (telephone terminal equipment) are thereby connected to the appropriate indicators on the spare channel control panel: channel 1 circuit 1 line to the SELECTION, CIRCUIT 1 light; channel 1 circuit 2 line to the SELECTION, CIRCUIT 2 light; channel 1 absence circuit 1 line to the ABSENCE CIRCUIT 1 light; and channel 1 absence circuit 2 line to the ABSENCE CIRCUIT 2 light. As shown in figure 2–10,C, the indicators on the channel 9 control panel are substituted for the odd channels in the channel 1 through channel 18 group. Similar circuitry exists for the even channels, with the indicators mounted on the simplex maintenance console channel 10 control panel. Indicators on channel control panels 27 and 28 are substituted for the odd and even channels respectively in spare channel operations involving channels 19 through 36.

CHAPTER 3
CHANNEL INPUT SECTION

3.1 INTRODUCTION

The function of the channel input section of the LRI element is to receive the LRI message (in serial form) from the telephone terminal equipment to separate the two words contained in the LRI message, to temporarily store the two words, and, when an empty drum slot is available, to transfer the two words (in parallel form, at relatively high speed) to the common equipment and then to the drum system. The channel input section also performs several operations on the message as it is processed. These operations include synchronizing the input data pulses with the operation of the Drum System, checking the parity of the incoming message to detect errors introduced in transmission, and destroying the message if the sync bit or busy bit is missing from the message.

A block diagram of a single LRI channel section is shown in figure 2–11. The diagram is simplified and shows only the data flow and the more important control signals. A detailed discussion for each of the blocks shown on figure 2–11 is included in the remainder of the chapter.

The data flow through the channel section begins with the application of the timing, sync, and data inputs that make up an LRI message to the data converter and synchronizer. The timing input is converted from a continuous 1,300-cps sine wave signal to a series of 10-μsec standard levels, one for each timing cycle. The sync input is converted from a single cycle of a 1,300-cycle sine wave to a standard pulse. The data input consists of a single cycle of a 1,300-cycle sine wave for each 1 bit and no input for each 0 bit. This data input is converted to a standard pulse for each 1 bit and no output for 0 bits. The pulses and levels produced by the data converter and synchronizer circuit are synchronized by pulses related to Drum System OD-timing pulses. These related pulses are designated LR pulses, have a 20-μsec pulse repetition time, and are synchronized by the OD pulses (which have a 10-μsec pulse repetition time). The LR pulses that are used in the channel sections are generated in the common equipment from OD pulses.

The data pulses and timing levels from the data converter and synchronizer circuit are applied to the primary core shift register control circuits. The primary core shift register is a 52-core shift register which stores the complete LRI message. The message is loaded into the primary register at the rate of 1,300 data bits per second (rate of reception of data bits from telephone terminal equipment). After a complete message has been inserted into the primary register, a fast shift level is applied which transfers the message serially from the primary register to the word 1 and word 2 core buffer registers at the rate of 50,000 shifts per second. The word 1 and word 2 core buffer registers are two 33-core-shift registers. The LRI message is divided into its two message words, with message word 1 stored in the word 1 buffer register and message word 2 stored in the word 2 buffer register. The parity bits for message words 1 and 2 are also stored in their respective registers. The complete LRI message is therefore stored in the word 1 and word 2 buffer registers to await transfer to the Drum System. When an empty drum slot is available, the two message words are read out, one word at a time, in parallel form to the common equipment. Message word 2 is read out first and passes through the common section, where additional data is added to make up the first word to the drum. Immediately after, the first message word is read out to the common section, where additional data is added to make up the second word to the drum.

The LRI message is converted and synchronized, divided into its two words, and read out to the common section by the data converter and synchronizer, primary core shift register, and word 1 and word 2 core buffer registers. The remaining circuits on figure 2–11 do not process data but are concerned with the control and checking operations of the channel.

The parity alarm circuit checks the parity of the incoming message words by making an odd-even count of the 1 data bits in each word. The busy bit detector checks for the presence of a busy bit. If the parity count is incorrect, a parity-error pulse is sent to the primary core shift register control circuits which will then destroy the message. The message is also destroyed if the sync bit or busy bit is missing from the message.

The fast-shift control circuit generates a fast-shift level when the complete LRI message has been received. The fast shift is turned off when the complete message has been transferred to the word 1 and word 2 core buffer registers.

The readout controls circuit receives a drum-demand (DD) pulse, and will generate the readout signals for the word 1 and word 2 core buffer registers when a message is contained in the core buffer registers.

The operations of the channel input section are synchronized by signals received from the drum input (common) section. These signals are derived from four standard pulses (OD 1, OD 2, OD 3, OD 4) originating in the Drum System. The OD pulses are standard pulses spaced 2.5 μsec apart. Recycling occurs without delay so that OD 1 occurs 2.5 μsec after OD 4. The OD pulse repetition rate of 10 μsec is too fast for the operation of some circuits in the channel input section; therefore the drum input section generates a group of pulses, with a 20-μsec repetition rate, for use in the channel input section. The following pulses and levels are furnished through switching to the drum input section:

a. OD 1+1
b. OD 4
c. LR 2
d. LR 4
e. LR 8
f. LR 1/2 (a level of 2.5 μsec duration)

The relationship of the LR and OD pulses and levels is shown in figure 2–12. The generation of the signals is more fully discussed in Chapter 5.

3.2 DATA CONVERTER AND SYNCHRONIZER

The data converter and synchronizer converts the timing sine wave inputs into timing-levels, and sync or data sine wave inputs into standard pulses, which are synchronized with LRI timing (LR) pulses for use within other circuits of the LRI channel input section. The data converter and synchronizer also provides a pulse to the primary shift register control to cause clear-

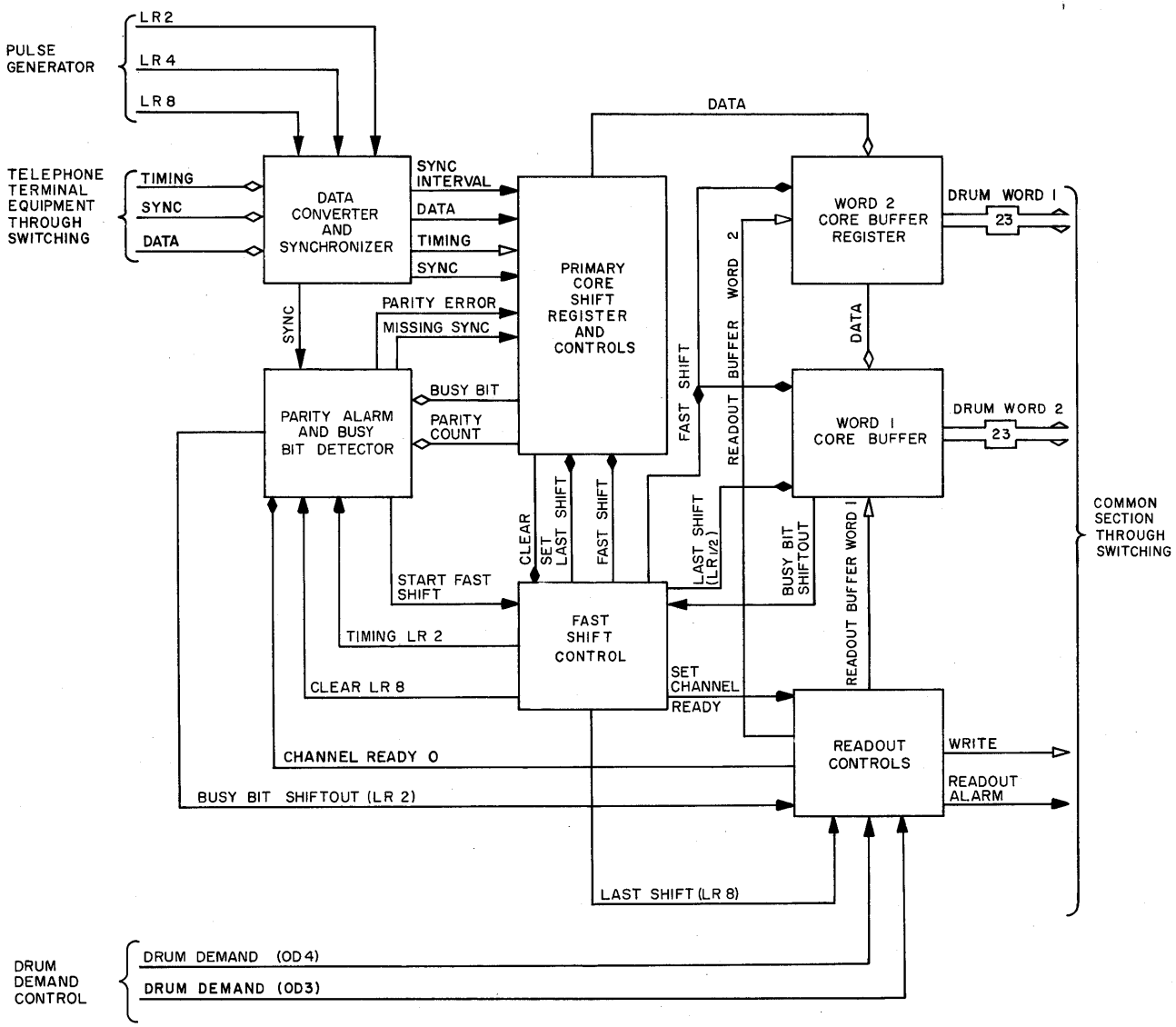


Figure 2–11. LRI Channel Equipment, Simplified Logic Diagram

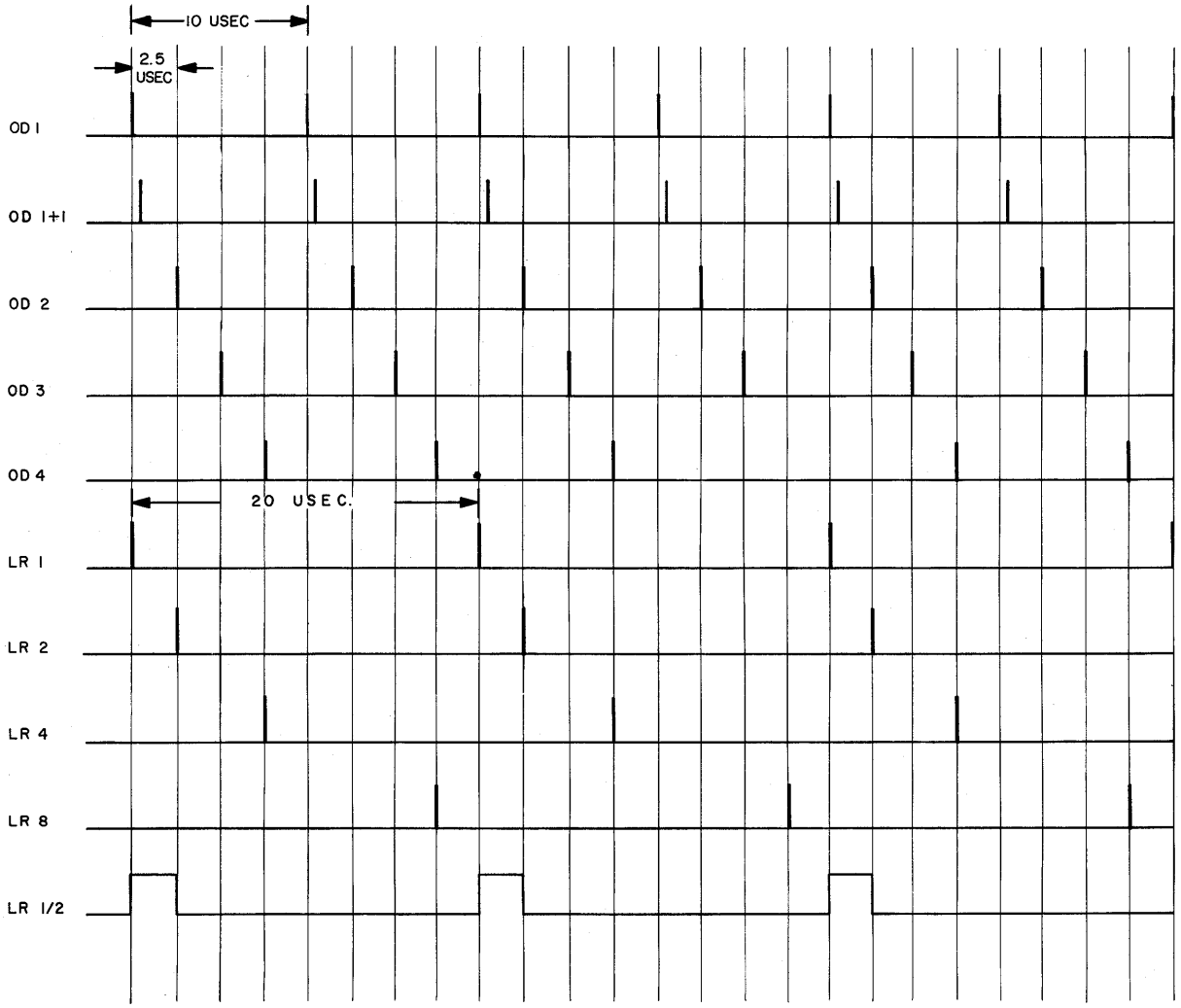


Figure 2–12. Relation of LR Pulses to OD Pulses, Timing Chart

ing of the primary shift register after a sync bit has been received by the data conversion receiver DCR 1.

The three classes of signals contained in an LRI message (timing, sync, and data) are sent from the telephone terminal equipment to the LRI element over separate lines. Relays in the input switching section permit the data converter and synchronizing circuit to accept messages from either the telephone line or the test bus. Each type of signal is applied to a data conversion receiver (DCR). See figure 2–13 and timing chart, figure 2–14. The timing is applied to the model A DCR which converts the 1,300-cycle sine wave to a nonstandard pulse. The sync and data signals go to model B DCR's whose outputs are standard levels (200 μsec duration) which occur whenever there is an input signal.

The timing pulse from the DCR sets FF 1 which conditions GT 1 and permits the succeeding LR 8 pulse to set FF 2. The 1 output from FF 2 conditions GT 2 and permits the succeeding LR 2 pulse to clear FF 1. The clearing of FF 1 deconditions GT 1 and prevents passage of LR 8 pulses until the next timing pulse is received. The clearing of FF 2 (by an LR 4 pulse) establishes the duration of the timing level (LR 8/4) at 10 μsec. The timing LR 8/4 level is fed to the primary shift register control to aid in the generation of shift levels for the primary shift register. The timing LR 8/4 level is also applied to GT 2 which passes one LR 2 pulse during each timing cycle. This timing LR 2 pulse is sent to the busy bit detector circuit. The timing LR 2 pulse applied to GT 3 generates a sync LR 2 pulse when a sync bit is received by DCR 1. For each data 1 bit received via DCR 2, GT 4 passes a data LR 2 pulse to the primary shift register control to cause a 1 data bit to be loaded into the primary shift register.

The sync LR 2 output of GT 3 is also applied to the set input of FF 2. Conditioned GT 5 passes the succeeding timing LR 2 pulse to clear FF 4, conditioning GT 6. The next timing LR 2 (and fast shift FF cleared)

pulse passes GT 6 and is sent to the primary shift register control to cause clearing of the cores of the primary shift register. The output of GT 6 also restores FF's 3 and 4 to their original states.

3.3 PRIMARY CORE SHIFT REGISTER AND CONTROLS

The primary core shift register control circuit serially receives the data of an LRI message from the data converter and synchronizer circuit at the rate of 1,300 bits per second. The data is loaded into the primary register. After the complete LRI message has been received and inserted into the primary register, the data is transferred to the word 1 and word 2 core buffer registers at the rate of 50,000 bits per second. The main purpose of the primary register is to permit a message to be received by the channel without disturbing the previous message stored in the word 1 and word 2 core buffer registers. This provides enough time for the message stored in the buffer registers to obtain access to an LRI field on the LOG drum. The time that a message can remain in the buffer registers without being disturbed by the next message is approximately equal to the time it takes to load the primary core shift register. The primary core shift register and control circuit is shown in figure 2–15.

The first data bit of an LRI message is always a 1 (busy bit); therefore, the first data LR 2 pulse generated from the busy bit clears FF 2. The flip-flop remains cleared until an LR 8 pulse is applied to the set input. Consequently, FF 2 is cleared for 15 μsec (LR 2 to following LR 8) each time a 1 data bit is received. The clear output of FF 2 primes (inserts a 1) the first core shift (CS 1) of the primary register. The next LR 8/4 timing level (occurring 1/1,300 second later) is applied through OR 3 to the AND circuit, and this then passes a single LR 1/2 pulse. The 2.5-μsec LR 1/2 level is applied through OR 2 to the CSD, which then shifts the

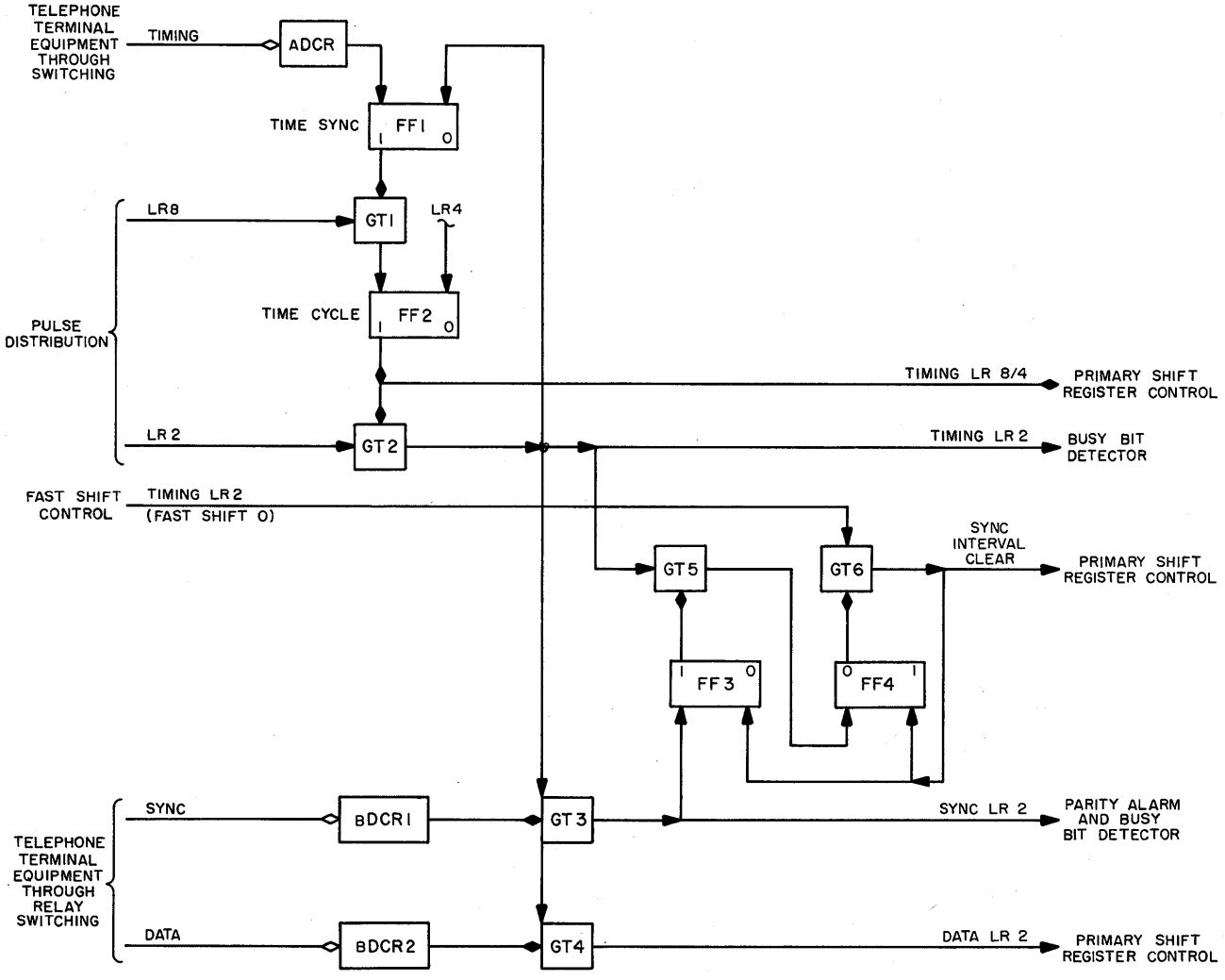


Figure 2–13. Data Converter and Synchronizer, Simplified Logic Diagram

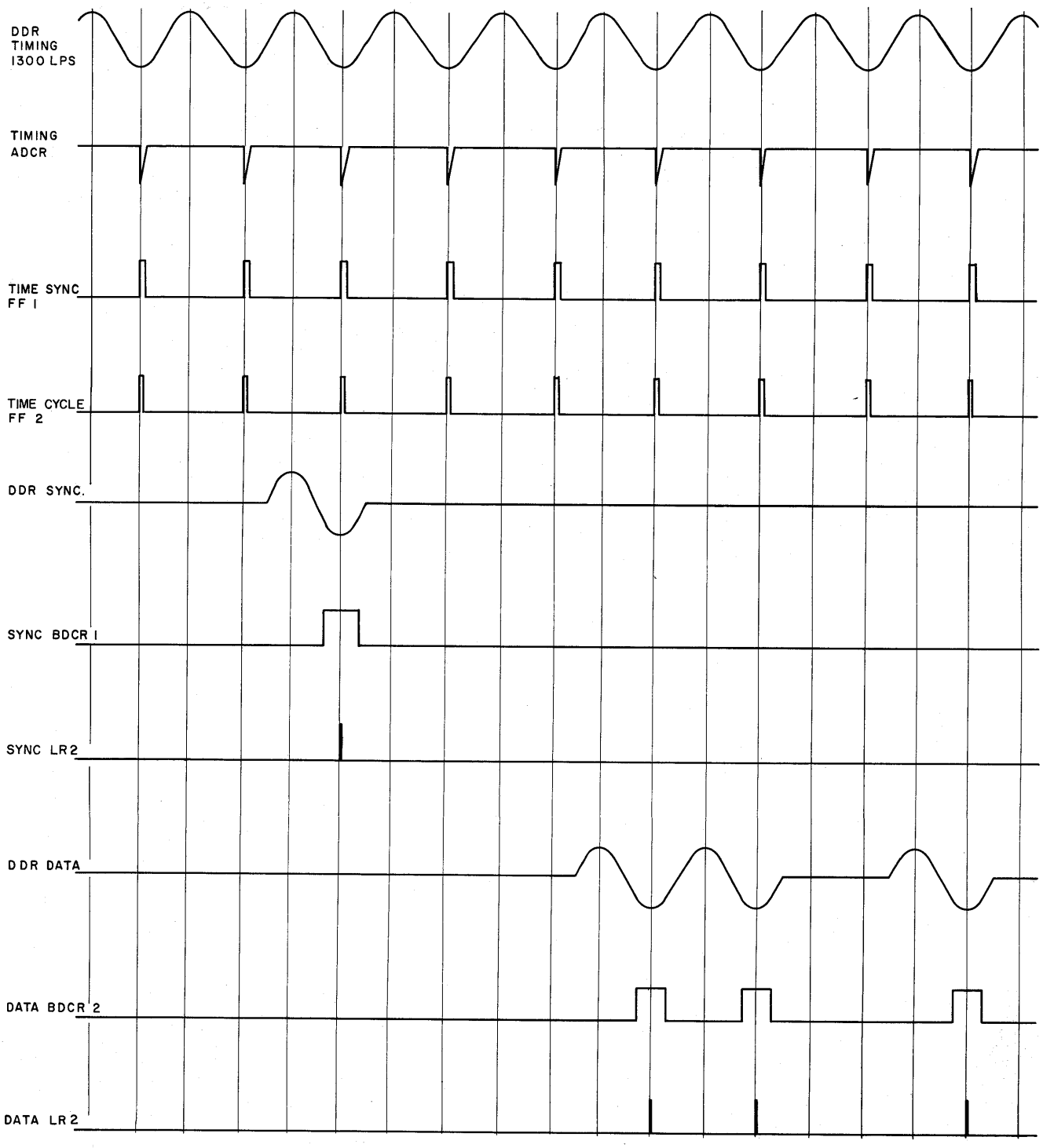


Figure 2–14. Data Converter and Synchronizer, Timing Chart

contents of each core of the primary register to the adjacent core. The next data bit is then inserted into CS 1 in the same manner as described above. When a data bit is a 0, CS 1 is not primed by the clear output of FF 2 because the data LR 2 pulse is not generated. The next shift level causes the 0 in CS 1 to be shifted to CS 2. Each shift level causes each bit to be shifted into the next core. Core shift 1 is always zero after each shift, permitting the next data bit to be inserted. The process continues in this manner until all the data bits are contained in the register. The shifting of the register is done at a 1,300 shifts-per-second rate since an LR 1/2 level is applied to the CSD only during a timing LR 8/4 level.

The 49th shift level occurs after 49 data bits have been inserted into the primary register. As the 49th shift level occurs, the busy bit is transferred from CS 49 to CS 50, and the transfer is also sensed on the output line connected to the output of CS 49. When the busy bit is transferred from CS 49 to CS 50, the output is a 1 which is sent to the parity alarm and busy bit detector circuit. A sync pulse received simultaneously with a busy bit output from CS 49 (while not in fast shift) is an indication that the primary register contains all the data bits of a message. The fast shift control circuit is signaled that a complete LRI message is stored in the primary register, and the fast shift level is generated. The fast shift level, applied through OR 3 to the AND circuit, permits LR 1/2 levels to shift the register. The LR 1/2 shift levels occur every 20 μsec (fast shift). Each data bit is transferred to the buffer storage on the output line of CS 52. The output of CS 50 is also sent to the parity alarm and busy bit detector circuit to aid in generating a signal, when the busy bit or sync bit is missing from the message.

The outputs of CS 2 and CS 25 are sent to the parity alarm and busy bit detector circuit where they are used to check the parity of the message words.

When the clear FF is set by any one of the four inputs, it will provide a +10V level to the CSD. The +10V level will cause the CSD to supply current to the reset or shift winding of the primary core shift register. The current will continue until FF 1 is cleared at LR 8. Therefore, the reset current will continue from LR 2 for the sync-interval-clear, parity-error, and missing-sync, until LR 8 (15 μsec in duration). For the set-last-

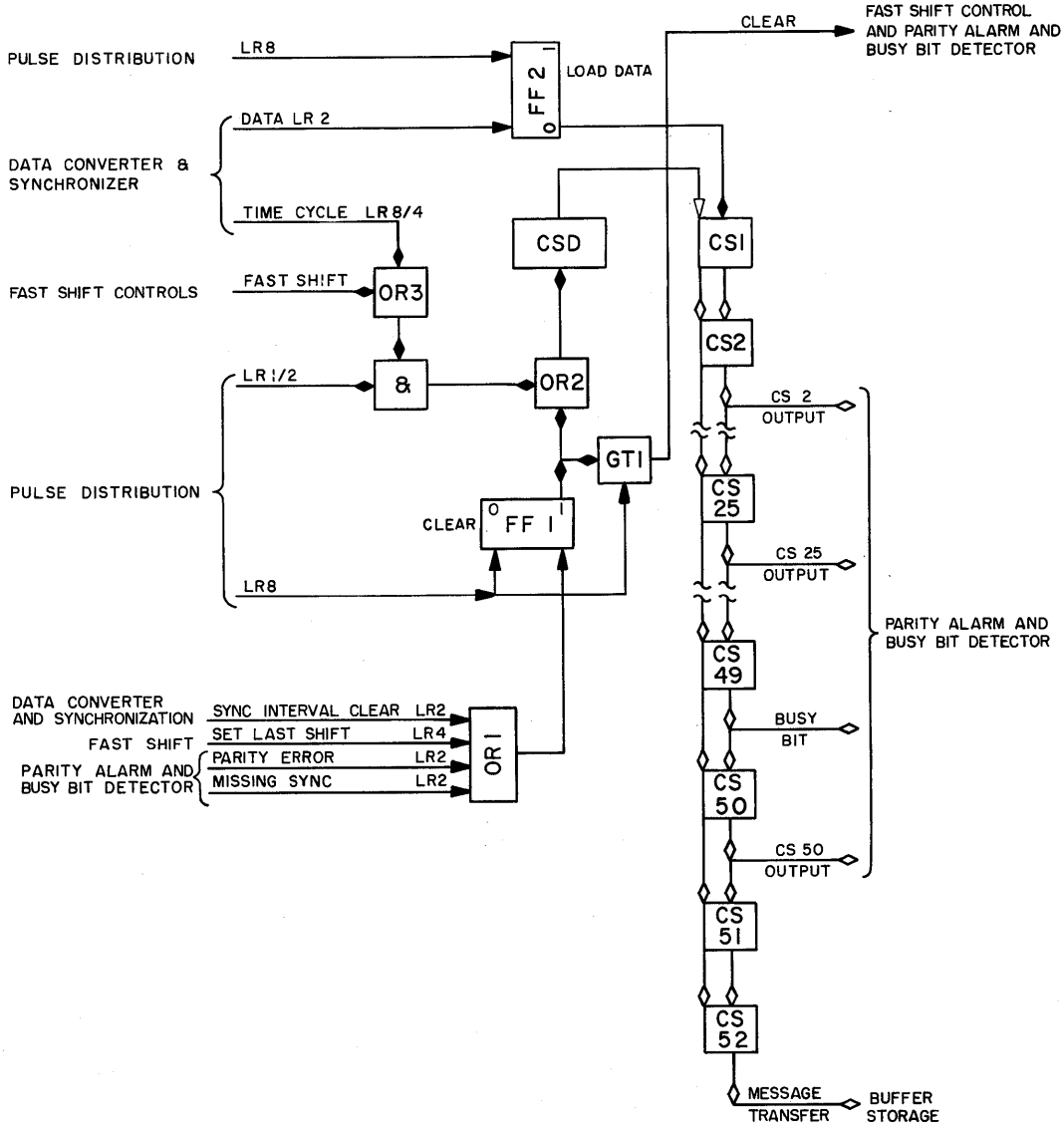


Figure 2–15. Primary Core Shift Register and Controls, Simplified Logic Diagram

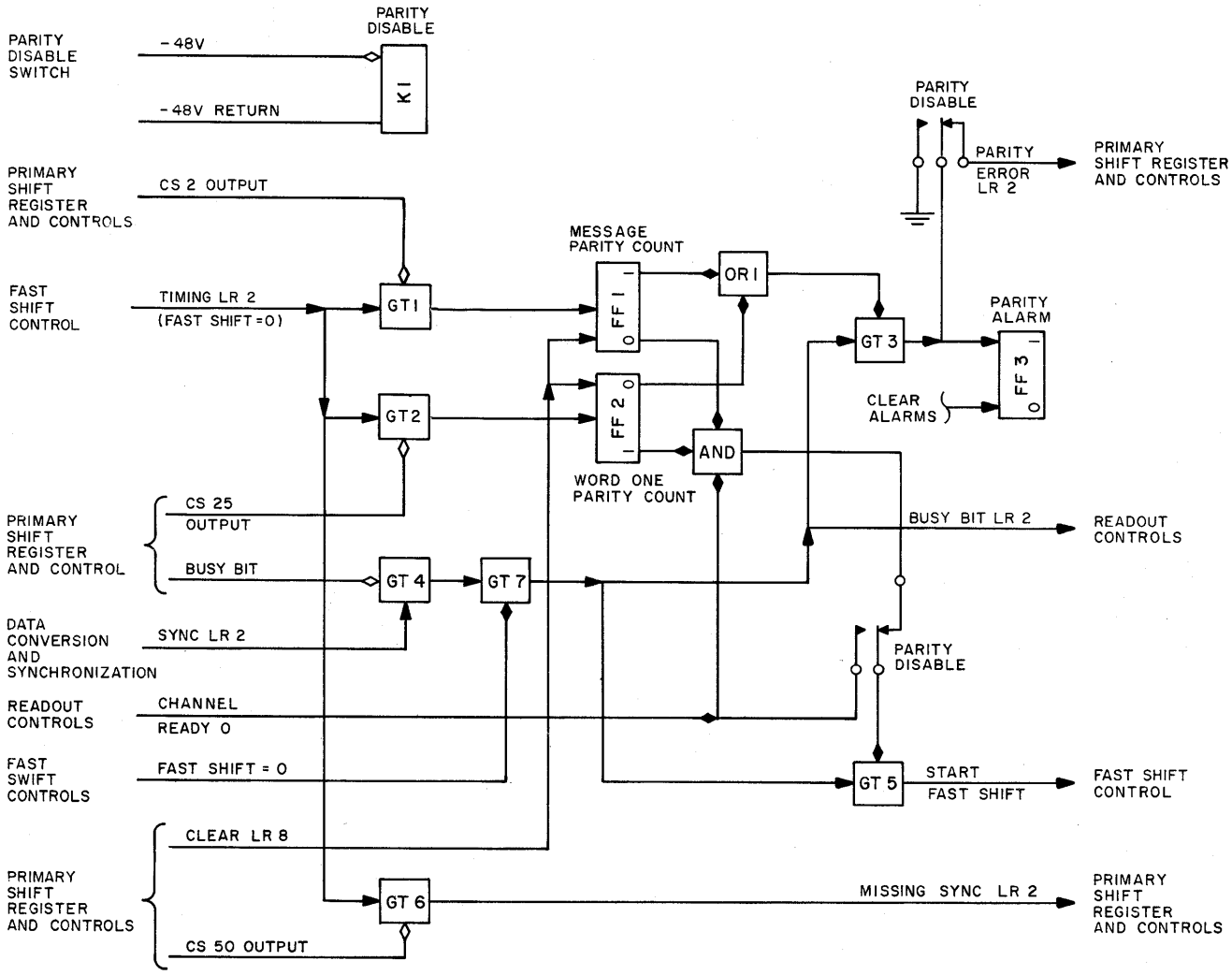


Figure 2–16. Parity Alarm and Busy Bit Detector, Simplified Logic Diagram

shift LR 4 input to the clear FF, the reset current will have a duration of 10 μsec. At LR 8 time, when FF 1 is clear, GT 1 (fig. 2–15) is strobed, and a pulse is generated to clear the parity FF's and to clear the fast-shift FF (discussed in 3.4 and 3.5, respectively).

3.4 PARITY ALARM AND BUSY BIT DETECTOR

The parity alarm and busy bit detector circuit performs the following functions.

a. Checks the parity of the incoming LRI message.

b. Checks for the presence of the busy bit and sync bit as the message is processed in the primary shift register.

c. Sends a start-fast-shift signal to the fast shift control circuit, if the message parity is correct and the sync bit is present when the busy bit reaches a predetermined point in the primary shift register (an indication of a good message).

d. Sends a parity-error pulse to the primary shift register and controls, and lights a parity error neon in the alarm section of the LRI control panel if a parity error occurs.

e. Sends a pulse to the readout control circuit to generate an alarm, if the buffer storage registers contain a message awaiting transfer to the Drum System.

The parity of the incoming message is checked by analyzing the number of data bits in the overall message word and the number of data bits in the first message word for an odd-even count. The busy bit is included in both counts. The parity check circuit, shown in figure 2–16, receives the CS 2 output of the primary shift register as the data bits are shifted from CS 2 to CS 3. If a 1 data bit is present, GT 1 passes the timing LR 2 pulse which is applied to the complement input of FF 1. If the message parity is correct, FF 1 is complemented

to the cleared side when all the data bits of the message (including the busy bit) have been received. Gate 2 receives the CS 25 output of the primary shift register, so that when the message is contained in the register, GT 2 has received a signal for every 1 data bit in the first word of the message (including the busy bit). Gate 2 is strobed by timing LR 2 pulses (if the fast shift FF in the fast shift controls is cleared), and the resulting pulses are applied to the complement input of word one parity FF 2.

Correct parity causes FF 2 to be complemented to the set condition when the complete message has been received by the primary shift register. If both parity counts are correct and the channel ready FF, in the readout control circuit, is cleared, the AND circuit conditions GT 5 to pass the LR 2 pulse received from GT 7. The pulse passed by GT 5 (start-fast-shift) is sent to the fast shift control circuit to initiate a fast shift of the message from the primary shift register into the buffer storage. If either the message parity count or the word one parity count is incorrect, GT 3 is conditioned and passes the output of GT 7 as a parity-error pulse. The parity-error pulse is sent to the primary shift register and controls to cause clearing of the message currently in the register. The parity-error pulse also sets the parity alarm FF which lights the parity error neon in the alarm section of the LRI control panel (simplex maintenance console). The PARITY DISABLED switch on the LRI control panel can be used to energize relay K1 (if the channel is in the standby status) to permit further message processing to take place. although the message may have incorrect parity.

The output of GT 7, sent to GT's 3 and 5 and to the readout control circuit, is an indication of a correct sync bit and busy bit but only when fast-shift $= 0$. Gate 6 receives the CS 50 output of the primary shift register. If GT 6 receives a 1 bit from CS 50 and the fast-shift FF (fast-shift control circuit) is cleared, GT 6 passes the missing sync LR 2 pulse which is sent to the primary shift register and controls in order to initiate a clear level for the cores of the primary shift register.

3.5 FAST-SHIFT CONTROLS

The fast-shift control circuit, shown in figure 2–17, performs the following functions:

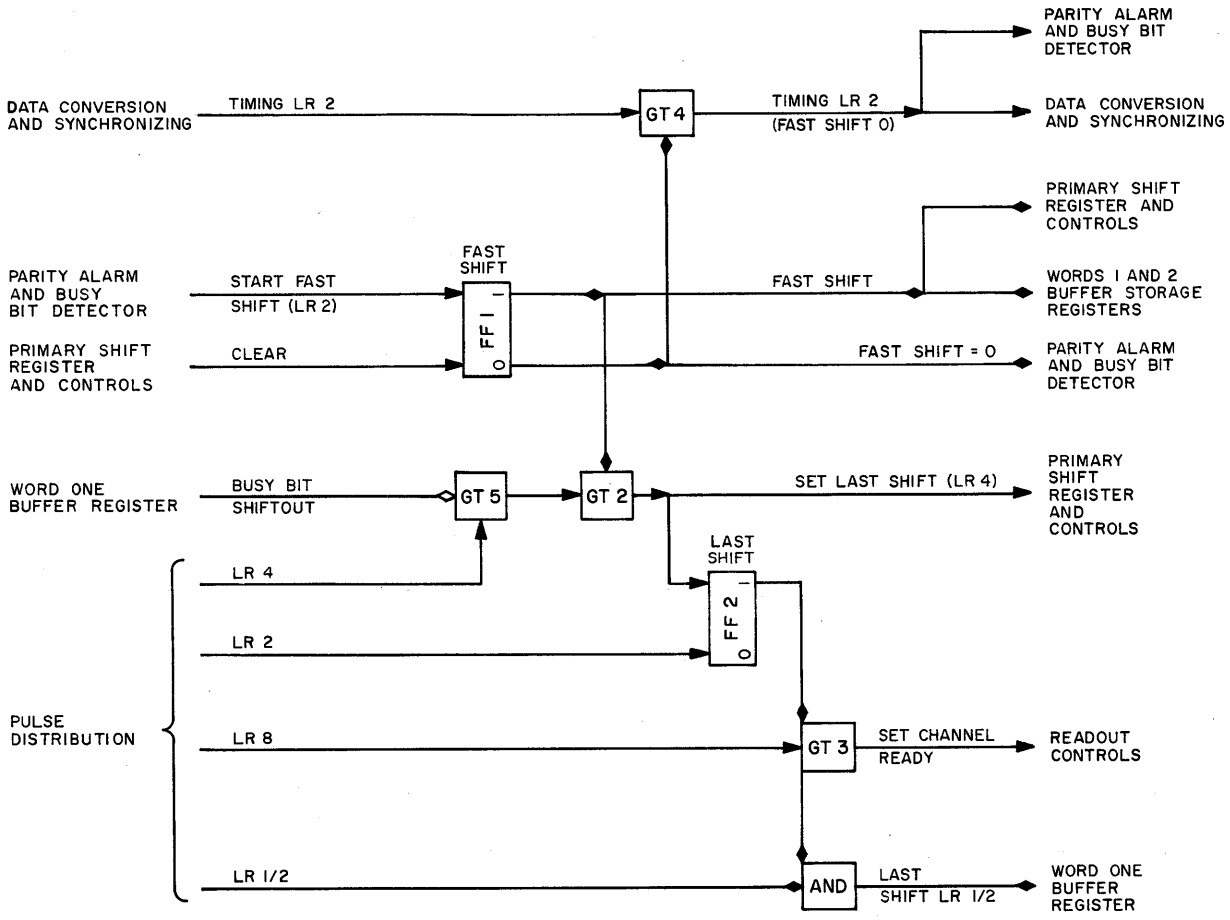


Figure 2–17. Fast-Shift Controls, Simplified Logic Diagram

a. Furnishes a fast-shift level which allows the fast shifting of the message from the primary shift register into the buffer storage.
b. Furnishes a last-shift LR 1/2 level to the word one buffer register.
c. Sends a pulse to set the channel ready FF in the readout control circuit.
d. Sends a set last-shift LR 4 pulse to the primary shift register and controls to initiate a clear level for the register.
e. Sends a fast-shift = 0 level to the parity alarm and busy-bit detector circuit to gate the busy-bit LR 2 pulse.
f. Sends a timing LR 2 (fast-shift = 0) to the parity alarm and busy-bit detector, and to the data conversion and synchronizing circuits as controlling signals in these circuits.

Flip-flop 1 is set by a start-fast-shift (LR 2) pulse from the parity alarm and busy-bit detector as an indication of the receipt of a good message. The set output of FF 1 is fed to the buffer storage and primary shift register and controls as a conditioning signal for the fast shift LR 1/2 levels. The set output of FF 1 also conditions GT 2 to pass the busy-bit-shiftout (LR 4) pulse from GT 5. The output of GT 2 (set-last-shift LR 4 pulse) initiates a clear level in the primary shift register and also sets the last-shift flip-flop (FF 2). The set output of FF 2 furnishes a conditioning level for GT 3 and the AND circuit. The set-channel-ready pulse sets the channel ready FF in the readout controls as an indication that the buffer register contains a message ready for transfer to the Drum System. The purpose of the last-shift LR 1/2 level from the AND circuit is discussed in 3.6. The timing LR 2 (fast-shift = 0) pulse from GT 4 permits missing sync detection and parity checking by the parity alarm and busy-bit detection circuit, as the primary shift register receives a message. The timing LR 2 (fast-shift = 0) pulse is also used in the data conversion and synchronization circuit to initiate a level to clear the cores of the primary shift register, two timing cycles after receipt of the sync bit. The clear LR 8 pulse from GT 1 resets the parity checking FF's.

3.6 WORD 1 AND WORD 2 CORE BUFFER REGISTERS

The word 1 and word 2 core buffer registers receive the message in serial form at fast-shift speed (50,000 shifts per second), store the message temporarily until a slot is available on the LRI field of the LOG drum, and read out the message in parallel form to the common equipment. The core buffer register circuit also generates the fast-shift LR 1/2 levels which shift the message into the core buffer as it is being shifted out of the primary shift register; the core buffer circuit also sends a busy-bit signal to the fast-shift controls to cause clearing of the primary shift register and termination of the fast shift. After the termination of the fast-shift, the circuit shifts word 1 buffer register an additional shift, so that readout of a bit in core 1 of word 2 buffer register will not cause an error in a position of word 1 which is transferred to the Drum System.

The word 1 and word 2 core buffer registers (fig. 2–18) are two identical core shift registers of 33 cores each. When an LRI message is read into the core buffer register, the data bits of the message are shifted out of the primary core shift register and are primed into core 33 of the word 2 core buffer register. The fast-shift level from the fast-shift controls is applied to the AND circuit which also receives LR 1/2 levels. The resulting fast-shift LR 1/2 levels are applied through OR 2 to the core shift drivers of the word 2 core buffer register and through OR 1 to the core shift drivers of the word 1 core buffer register. The first bit (busy bit) of the incoming LRI message is then shifted, one core per shift, from core 33 to core 1 of the word 2 core buffer register. The shiftout of core 1 of the word 2 core buffer register causes the busy bit to be primed into core 33 of the word 1 core buffer. The shifting of the word 1 core buffer progresses until the busy bit reaches core 10. On the shiftout of core 11 and into core 10, a busy-bit signal is sent to the fast-shift controls, initiating the end of fast shift, removing the fast-shift input to the AND circuit, and stopping the fast-shift LR 1/2 levels. This stops the shifting of both word 1 and word 2 core buffer registers. A last-shift level from the fast-shift controls, applied to OR 1, causes the word 1 core buffer to shift once more, moving the busy bit to core 9 which has no output connection to the drum. The data bits that follow the busy bit in the LRI message are shifted into the core buffers in the same manner as the busy bit, emptying the 33rd core of the word 1 core buffer register.

The last shift for the word 1 core buffer is necessary in order to prevent the last bit in buffer word 1 from being affected during the readout of buffer word 2. Since buffer word 2 is read out before buffer word 1, the output of core 1 in buffer register 2 would affect the bit contained in the 33rd core of buffer register 1, if there was not a last shift emptying the 33rd core.

The shifting process, just described, ends with the first half of the LRI message in cores 10 through 32 of the word 1 core buffer register, with the parity bit in core 32. The second half of the LRI message is in the word 2 core buffer register in cores 1 through 23. The buffer word 2 parity bit is in core 23.

The LRI message is read out of the core buffer registers in parallel form for each word. The word 2

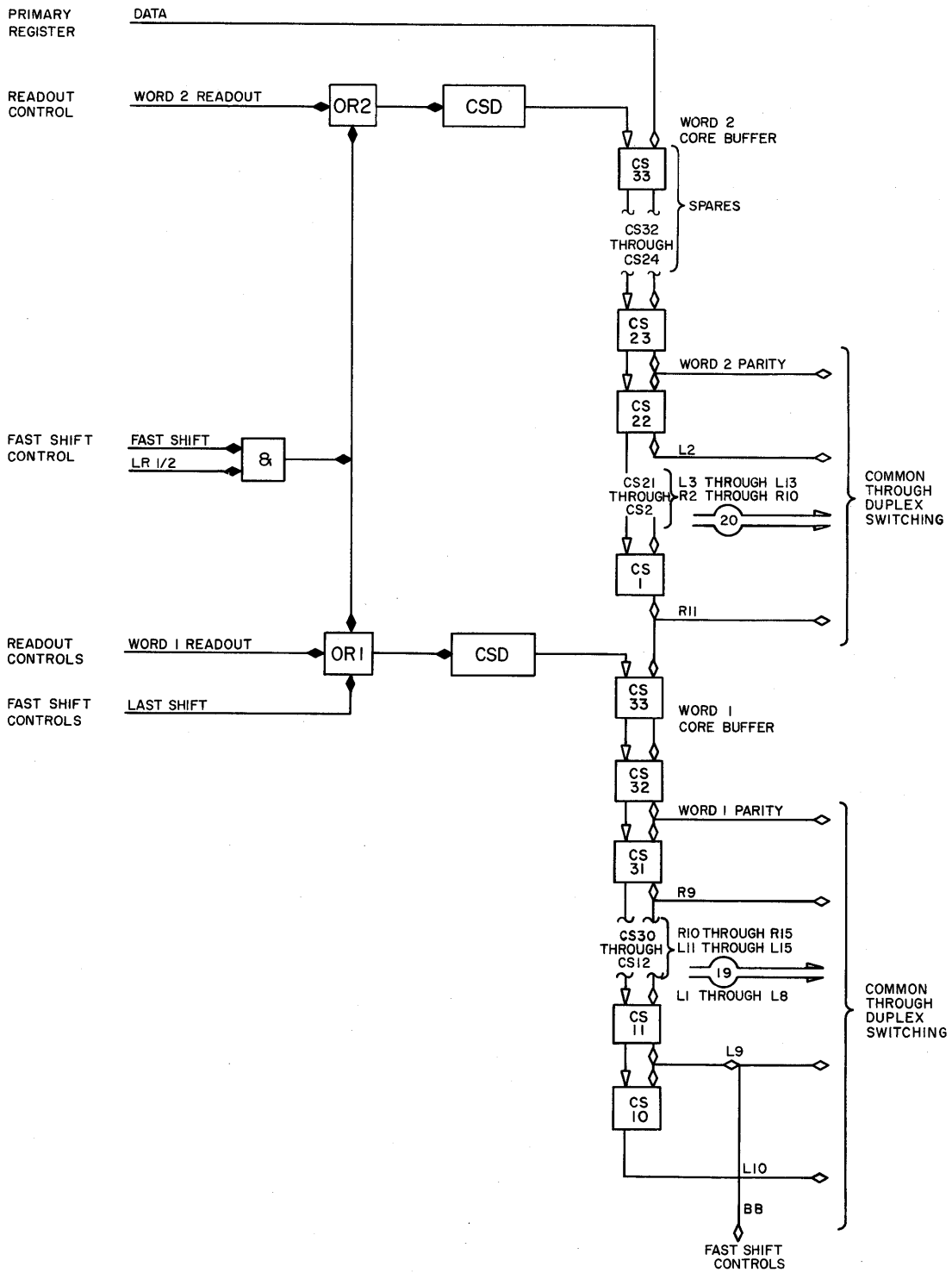


Figure 2–18. Word 1 and 2 Core Buffer Registers, Simplified Logic Diagram

buffer register is read out, first. A word-2-readout level from the readout controls is applied to OR 2. This 10-μsec level causes an output from each core in the word 2 buffer that contains a 1 bit. This output is sent to the LRI common equipment to condition gates that pass pulses to the drum. Following the readout of word 2, word 1 is read out, in a like manner, through the common section to the drum. All the data in word 1 and word 2 core buffer registers, except the parity bits and the busy bit, is sent directly to the drum. Additional information generated in the common equipment is, however, also read out to the drum so that the drum words contain more information than the core buffer words. The parity bits are also processed in the common equipment before transmittal to the drum fields so that the entire drum word will have the required odd parity. The busy bit, having served its purpose in initiating the end of fast shift, is not transmitted out of the core buffer register.

The parallel output wiring of the core buffers is so connected that the data in the drum words is rearranged differently from the order in the core buffer words.

3.7 READOUT CONTROL CIRCUIT

The readout control circuit (fig. 2–19) performs the following functions:

a. Generates the word 1 and word 2 readout levels which cause readout of the core buffer registers.

b. Generates a write level to read out site identity; the site identity becomes a part of drum word 1.

c. Generates a channel-ready-0 level to control generation of the start-fast-shift pulse.

d. Generates a readout-alarm pulse, if the primary shift register is about to transfer a message to the core buffer register and the core buffer register contains a message which has not been transferred to the Drum System.

e. Relays a DD pulse to the channel of next higher priority if the core buffer register does not contain a message ready for transfer.

f. Tests the ability of the circuit to inhibit readout if a malfunction causes the channel-ready FF to generate simultaneous up levels on both the cleared and set output lines.

Flip-flop 1 is set by the set-channel-ready pulse, indicating that a good message is stored in the core buffer register. The following DD (OD 3) pulse (indicating an available drum slot) from the Drum System is passed by GT 5 and the VRD to set FF 2, conditioning GT 1. The DD (OD 4) pulse, passed by conditioned GT 1, sets FF 3 which generates the word-2-readout level and the write level (13.5 μsec in duration). The write level is fed to the common equipment to generate data-available pulses and site identify. The word-2-readout level transfers the data bits in the word 2 core buffer register. The output of FF 3 also conditions GT 2 which passes the next OD 4 pulse to set FF 4. Flip-flop 3 is cleared by the succeeding OD 1+1 pulse via OR 1, and FF 4 is cleared by the succeeding OD 4, establishing the word-1-readout level (10 μsec in duration) to read out the word 1 core buffer register.

If the core buffer registers contain a message (FF 1 in set condition), and a busy-bit-shiftout (LR 2) pulse, indicating that a new message is about to be shifted into the core buffer register is received, GT 6 will send a readout-alarm pulse to the common equipment to initiate alarm indications. Receipt of a DD (OD 3) pulse, at a time when the core buffer registers do not have a message available for transfer (FF 1 cleared), permits GT 7 to pass the DD (OD 3) pulse to the channel of next higher priority. The channel-ready-0 level is sent to the parity alarm and busy-bit detection circuit as a control for the generation of the start fast-shift.

The circuit should inhibit the transfer of data to the Drum System, if both output lines of FF 1 should have a simultaneous up-level output. The up-level outputs will condition AND 1, transmitting a signal to the control input of the VRD. The normally closed contacts of the VRD will open, preventing the initiation of further readout levels by FF 2. A test circuit is provided to check the ability of the channel to inhibit readout under these conditions. With the TEST switch (LRI control panel, simplex maintenance console) in the TEST position, relay K1 is energized, applying +10V to both inputs to AND 1, which simulates the malfunction of FF 1, described above.

Flip-flop 3 can be cleared by a DD (OD 3) pulse applied via OR 1, to ensure that FF 3 is always cleared when a DD pulse requests information, thereby preventing the loss of incoming radar data.

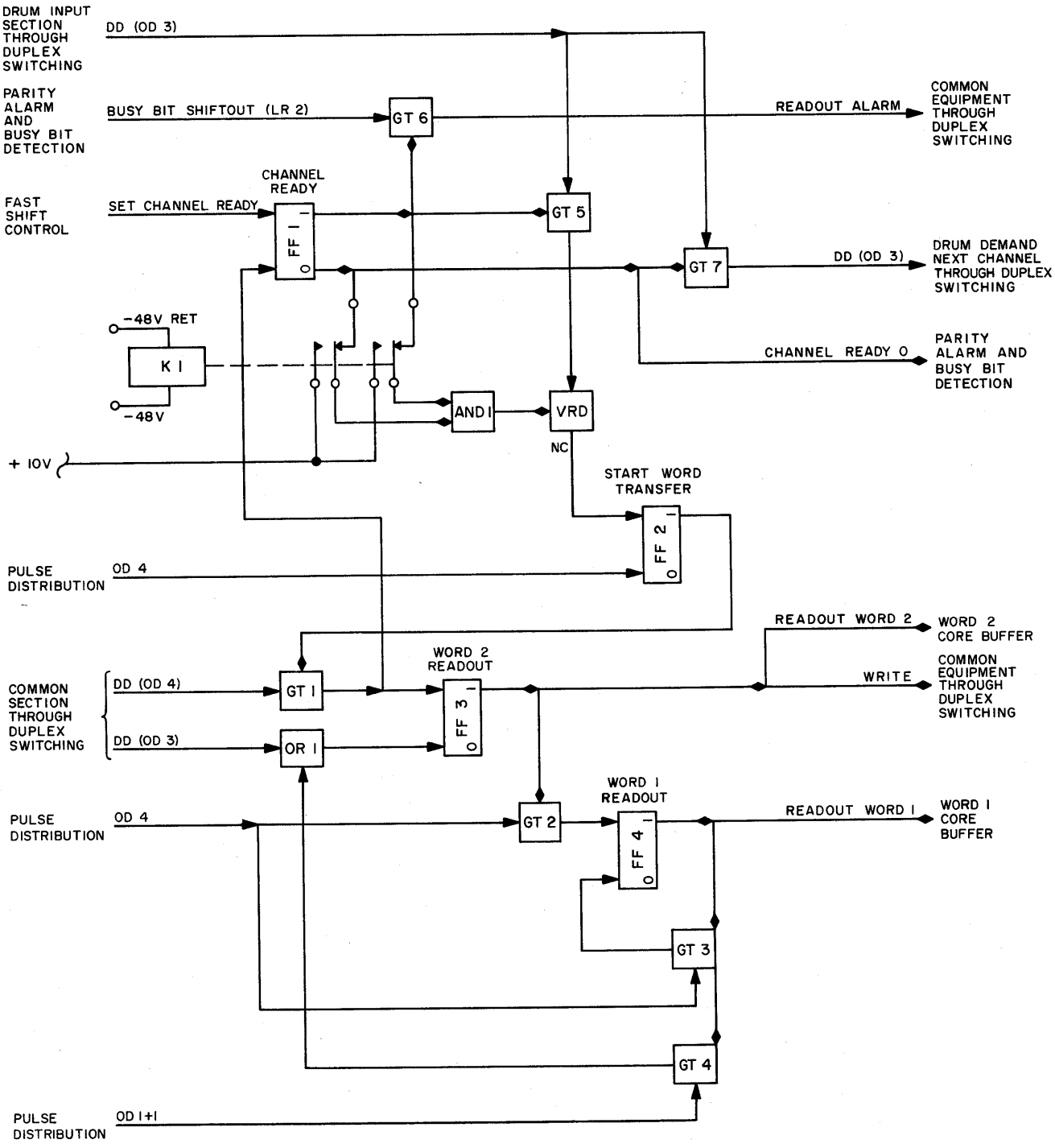


Figure 2–19. Readout Controls, Simplified Logic Diagram

CHAPTER 4
DUPLEX SWITCHING

4.1 GENERAL

Duplex switching relates simplex equipment to the proper A or B common equipment and, ultimately, to the proper A or B computer. Simplex equipment in the active status is associated with the duplex computer currently in the active status, and simplex equipment in the standby status is associated with the duplex computer in the standby status.

Duplex switching in the LRI element provides the necessary circuitry to accomplish the following functions:

a. Core data switching: Transfers the data from the core buffer registers of the 36 channel sections to the common A or common B section indicated by the status of the channel and the status of the A and B duplex computer.

b. Write level switching: Transfers the write level generated in a channel input section to the proper half (A or B) of the common equipment. In spare channel switching (refer to 2.3), the write level generated by the spare channel must be switched to the site can of the replaced channel. Accordingly, when a spare channel is substituted, write level switching involves both duplex and simplex switching.

c. Readout alarm switching: Directs the readout alarm pulse to the proper A or B common equipment.

d. Timing pulse and level switching: Transfers the OD pulses and the LR pulses and levels from the proper half of the common section to the channel input section to synchronize channel operations with the operation of the common section with which the channel is associated.

e. Drum demand switching: Transfers the DD pulses to the channel sections to initiate readout to the common equipment on a priority basis.

f. Site neon indication switching: Causes illumination of either the A or B site neons on the channel control panel (simplex maintenance console).

g. Status indication switching: Sends status indication of each channel to the MDI element of the proper computer.

4.2 DRIVING OF A AND B SIGNAL RELAYS

The operations listed above are accomplished by means of groups of relays, designated A signal relays and B signal relays. Only one group can be energized at any one time, depending on the status of the channel and the status of the A or B computer. The driving circuit for these relays is shown in figure 2–20. The —48V driving voltage is supplied by MCD unit 59A or 59B through individual cells of power distribution unit 55. This voltage is applied to the terminals of unit status switch sections G and H. Section G controls the energizing of the A signal relays; section H controls the energizing of the B signal relays.

Assume that the A machine has been designated active and the B machine standby by the duplex selection control at the duplex switching console. Relay-driving voltage is then applied to terminal 1 (ACTIVE) of section G and terminals 3 and 4 of section H (STANDBY, STANDBY MC, respectively, of the unit status switch of each channel). If this switch is placed in the ACTIVE position, driving voltage is applied to the A signal relays; if this switch is placed in the STANDBY or STANDBY MC position, driving voltage is applied to the B signal relays. Reversing the status of the A and B machine reverses the effect of the UNIT STATUS switch positions on the signal relays.

The signal control relays for channel 1 are listed, and their functions are indicated in table 2–1. Each contact group of a relay (if used) performs a specific function, and corresponding contact groups of paired A and B signal relays perform the same functions. Thus, when A signal relay 41AM(K1) is energized, contact group 2 causes transfer of the write level from channel 1 to the A drum input section; if the B signal relays are energized, contact group 2 of 41AM(K2) transfers the write level from channel 1 to the B drum input section.

When a group of signal relays for a channel are energized, one set of contacts from each relay (connected in a series array) completes a circuit to cause illumination of the related (A or B) SIGNAL CONTACTORS CLOSED lamp (power section, odd or odd-spare LRI control panel). Illumination of the SIGNAL CONTACTORS CLOSED lamp indicates which computer is receiving data from the pair of channels controlled by the power section of the control panel; it

also indicates that all relays in the group are energized.

The detailed operation of the signal relays for channel 1 is discussed by function below; different relays, tabulated in the Input System schematic manuals, are employed in other channels, but their operation is the same as that of corresponding relays in channel 1.

4.3 CORE-DATA SWITCHING

The action of the core-data switching circuit determines whether the output of each pair of channels is directed to common A or common B. The choice of common A or B is determined by manual switches located on the duplex switching and simplex maintenance consoles, as discussed in 4.2. The outputs from all active pairs of channels are directed to the common equipment that has been selected by the operator as active; the outputs from channels in the standby status are sent to the standby common equipment.

The switching circuit for a typical data bit (R4) is shown in figure 2–21. For channels 1-2, an OR circuit combines the word message signals from the core buffer registers. With both computer A and channels 1-2 active, channels 1 and 2 transfer data to common A through the normally open contacts of the A signal relay.

The bit signal lines from the A relays are then combined with four similar output lines from the other pairs of channels (3-4 through 9-10) in an OR circuit to form a single output line of channels 1-10 for R4 of words 1 and 2. The channels 1-10 output is combined in an OR circuit with a similar output from channels 11-18. The channels 11-18 output is combined with a similar channels 19-36 output to obtain a one-line channels 1-36 output for words 1 and 2. This is the output line from the common A section and is fed to the Drum System.

The core-data switching circuits for all other channel pairs are identical to the switching circuits for channels 1-2. When a pair of channels are transferring data to common B, the appropriate B signal relays are energized, connecting that channel to common B by circuits identical with those discussed above for common A.

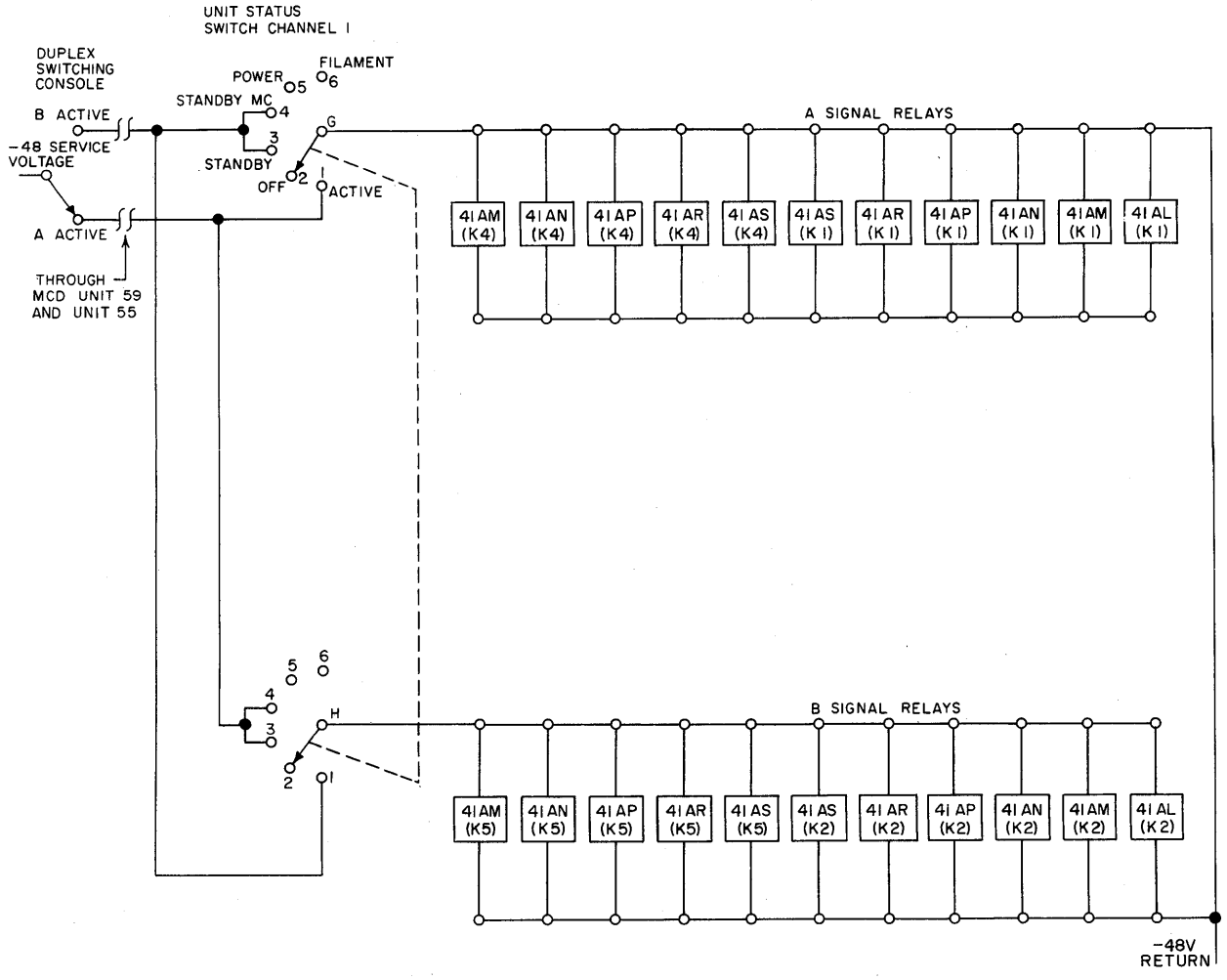


Figure 2–20. A and B Signal Relays Driving Circuit, Simplified Schematic Diagram

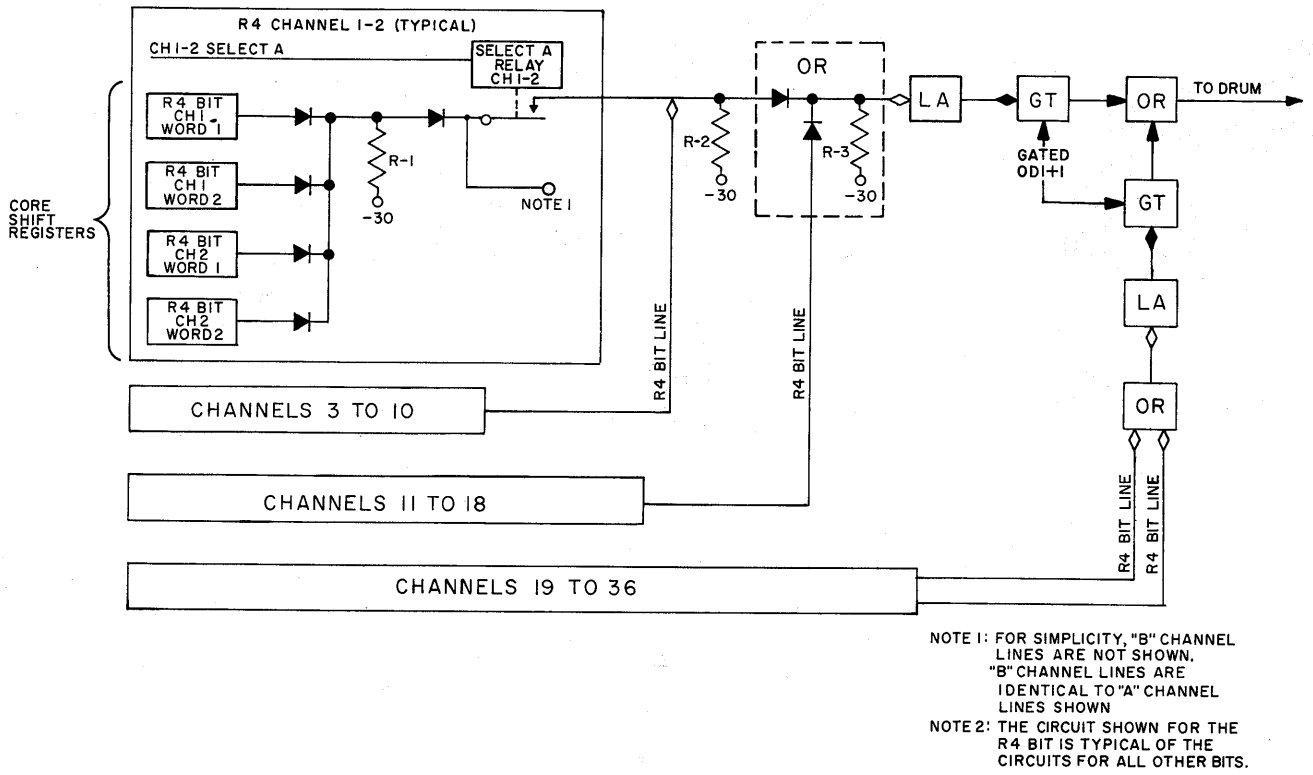


Figure 2–21. Core-Data Switching

TABLE 2–1. FUNCTION OF SIGNAL RELAY CONTACTS, CHANNEL 1

FUNCTION	A SIGNAL RELAY	B SIGNAL RELAY
CORE DATA TRANSFER		
L1	41AN(K4) 3	41AN(K5) 3
L2	41AN(K4) 4	41AN(K5) 4
L3	41AN(K4) 5	41AN(K5) 5
L4	41AN(K4) 6	41AN(K5) 6
L5	41AP(K4) 2	41AP(K5) 2
L6	41AP(K4) 3	41AP(K5) 3
L7	41AP(K4) 4	41AP(K5) 4
L8	41AS(K4) 2	41AS(K5) 2
L9	41AS(K4) 3	41AS(K5) 3
L10	41AS(K4) 4	41AS(K5) 4
L11	41AS(K4) 5	41AS(K5) 5
L12	41AR(K4) 5	41AR(K5) 5
L13	41AR(K4) 2	41AR(K5) 2
L14	41AR(K4) 3	41AR(K5) 3

TABLE 2–1. FUNCTION OF SIGNAL RELAY CONTACTS, CHANNEL 1 (cont'd)

FUNCTION	A SIGNAL RELAY	B SIGNAL RELAY
CORE DATA TRANSFER		
L15	41AR(K4) 4	41AR(K5) 4
R1	41AN(K1) 3	41AN(K2) 3
R2	41AN(K1) 4	41AN(K2) 4
R3	41AN(K1) 5	41AN(K2) 5
R4	41AN(K1) 6	41AN(K2) 6
R5	41AP(K1) 2	41AN(K2) 2
R6	41AP(K1) 3	41AP(K2) 3
R7	41AP(K1) 4	41AP(K2) 4
R8	41AS(K1) 2	41AS(K2) 2
R9	41AS(K1) 3	41AS(K2) 3
R10	41AS(K1) 4	41AS(K2) 4
R11	41AS(K1) 5	41AS(K2) 5
R12	41AS(K1) 6	41AS(K2) 6
R13	41AR(K1) 2	41AR(K2) 2
R14	41AR(K1) 3	41AR(K2) 3
R15	41AR(K1) 4	41AR(K2) 4
WORD 1 PARITY BIT	41AN(K1) 2	41AN(K2) 2
WORD 2 PARITY BIT	41AN(K4) 2	41AN(K5) 2
WRITE LEVEL	42AM(K1) 2	41AM(K2) 2
READOUT ALARM	41AM(K4) 2	41AM(K5) 2
DD OD 3 (INTO CHANNEL)	41AL(K1) 3	41AL(K2) 3
(OUT OF CHANNEL)	41AL(K1) 4	41AL(K2) 4
DD OD 4	41AM(K4) 6	41AM(K5) 6
OD AND LR TIMING OD 1 +1	41AR(K1) 6	41AR(K2) 6
OD 4	41AP(K4) 5	41AP(K5) 5
LR 2	41AP(K1) 5	41AP(K2) 5
LR 4	41AP(K1) 6	41AP(K2) 6
LR 8	41AR(K4) 6	41AR(K5) 6
LR ½	41AR(K1) 5	41AR(K2) 5
SITE IDENTITY	41AP(K4) 6	41AP(K5) 6
STATUS INDICATION	41AL(K1) 5	41AL(K2) 5

4.4 WRITE LEVEL SWITCHING

Write level switching connects a write level generated in the channel input section to the A or B site can in the drum input section. In spare channel operations, write level switching involves both simplex and duplex switching because the write level generated in a spare channel must be applied to the site can for the replaced channel.

The write level switching circuit for channels 1-2 is shown in figure 2–22. A write level, originating in channel 1, is transferred to either common A or common B through the 2 contact of either A signal relay K2, or B signal relay K1. The write level for channel 2 and other regular channels is transferred in a similar manner, depending on which signal relay (A or B) is energized. In spare channel operations, a channel 9 write level, generated in the drum input section, is transferred through the 2 contact of either the A or B signal relay for channel 9 and through the 1 or 2 contact of the select spare for channels 1-2 relay (K1). The output is on the channel 1 write line to common A or common B, as determined by the channel 9 signal relay. A similar circuit related to the channel 2 write level is shown for channel 10. Circuitry exists for other channel pairs with the select spare for channels 3-4, 5-6, etc., in place of relay K1.

4.5 READOUT ALARM SWITCHING

A readout alarm pulse is generated in the readout control circuit (3.7), indicating that the primary shift register has a message ready for fast-shifting into a core buffer register which already contains a message. The readout alarm pulses for each channel are transferred through switching to the proper A or B common section, causing the readout alarm FF to be set. For channel 1, the readout alarm pulse is transferred through signal relay A contact 41AM(K4) 2 or through B signal relay contact 41AM(K5) 2, as indicated in table 2–1.

4.6 TIMING PULSE AND LEVEL SWITCHING

The OD pulse and LRI pulse and level switching circuitry switches the timing pulses and levels generated or controlled by the A and B drum input section to the channels associated with the A and B computers, respectively. Refer to 3.1 for a list of these timing pulses and levels and to table 2–1 for the A and B signal relays involved in the transfer.

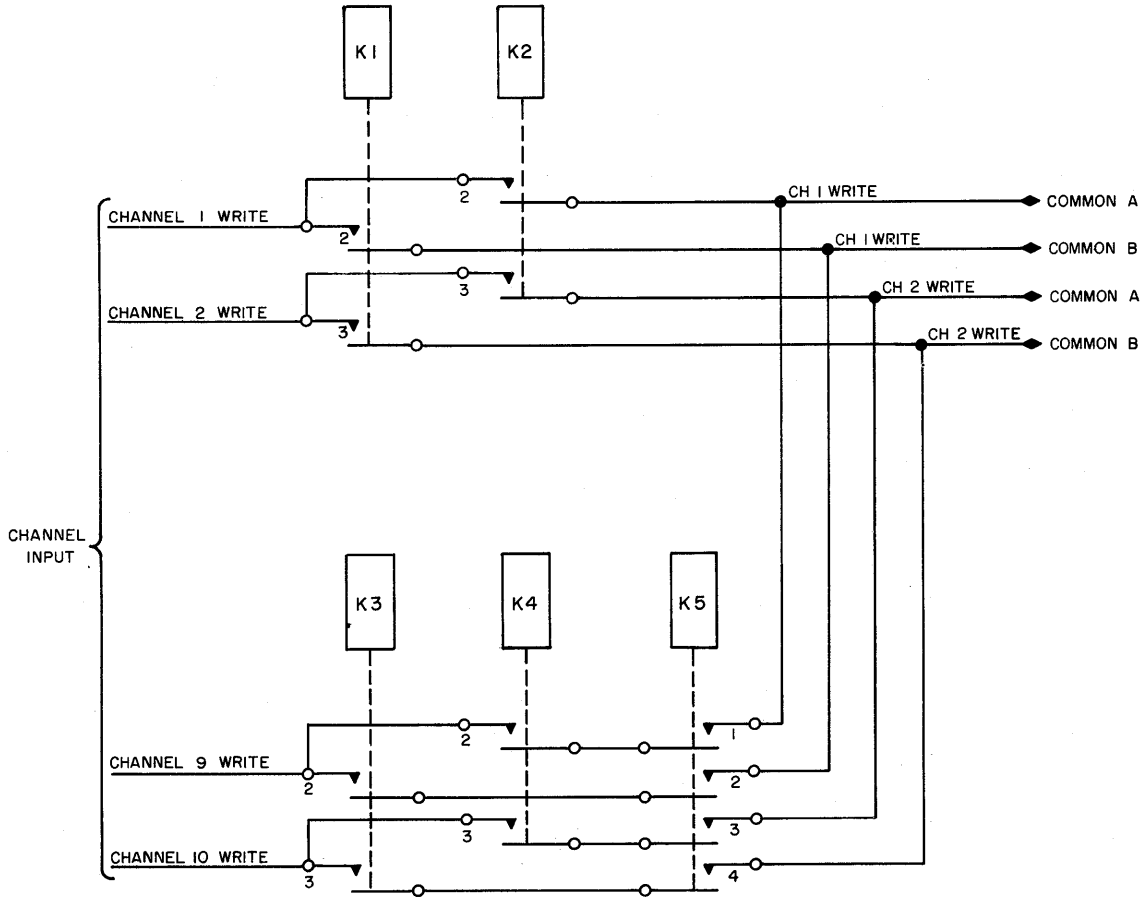


Figure 2–22. Write Level Switching, Simplified Diagram

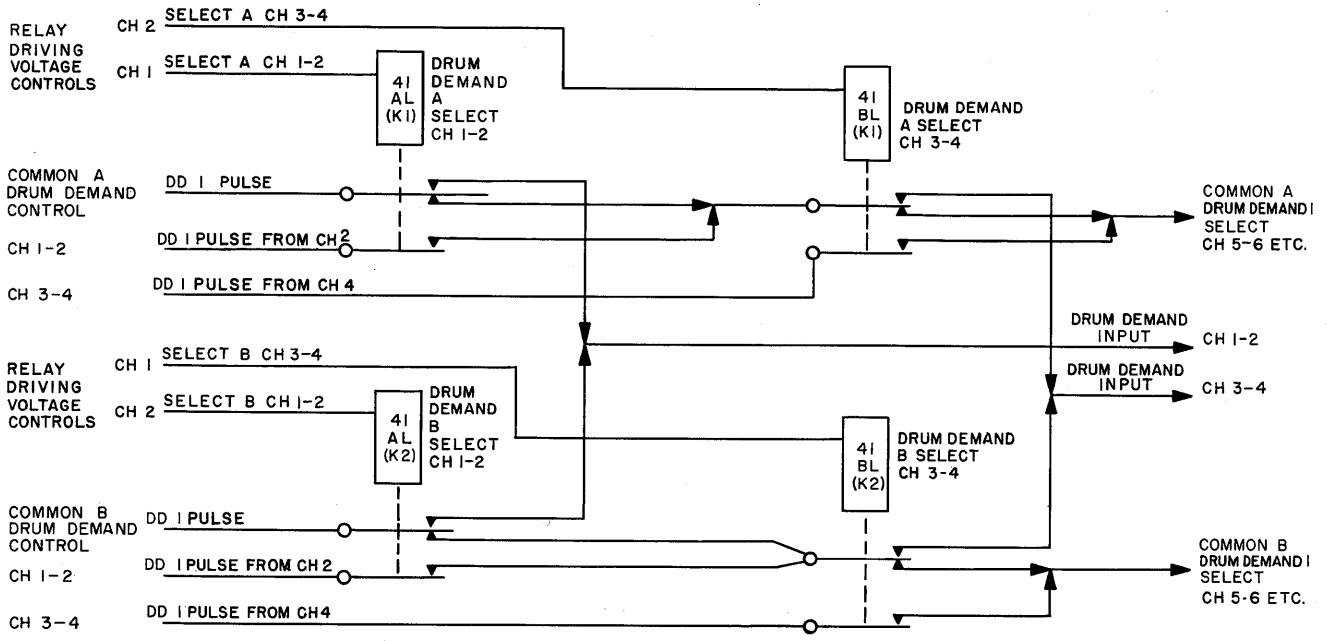


Figure 2–23. Drum-Demand Switching (chan. 1 and 2; chan. 3 and 4)

4.7 DRUM-DEMAND SWITCHING

The drum-demand circuit of Drum Systems A and B sends pulses to the channels connected to common A and B, respectively. The function of the drum-demand switching circuit is to send, in order of priority, the A DD pulses to the input channels connected to common A, and the B DD pulses to the input channels connected to the common B. The input channels connected to common A in the channels 1-18 chain receive the A DD 1 pulse from the drum-demand circuit, while the 19-36 channels chain receives the DD 2 pulse.

Drum-demand switching for channels 1, 2, 3, and 4 is shown in figure 2–23. The circuitry for energizing the relays is discussed in 4.2.

4.7.1 Drum-Demand Switching for Channels 1 and 2

The DD 1 pulse from the drum-demand control circuit in common A is sent to the readout control circuit of channel 1 when the select A channels 1-2 line is energized. The DD 1 pulse initiates readout of channel 1, or, if channel 1 has no message data stored, it passes the DD 1 pulse to the readout control circuit of channel 2. If channel 2 is not ready, the DD 1 pulse comes out of channel 2 and is passed to the A select relay contacts of channels 3-4.

When channels 1 and 2 are connected to common B, the DD 1 pulse passes directly from common A to the drum-demand A select relay of channels 3-4, completely bypassing channels 1 and 2.

4.7.2 Drum-Demand Switching for Channels 3 and 4

When a DD 1 pulse from the drum-demand switching circuit is applied to the A select relay for channels 3-4, it is sent to channel 3, if the channels 3-4 select A line is energized (or to channel 5 if the A select line is not energized). The DD 1 pulse passes through the readout control circuits of, first, channel 3, and then, channel 4. When channels 3 and 4 are not connected to common A, the DD 1 pulse from channel 2 passes directly to the drum-demand switching for channels 5-6, or to 7-8 if 5-6 are not activated, etc.

All channels which are connected to common B use and pass DD 1 pulse from the drum-demand switching circuit of common B in exactly the same manner described above for the channels connected to common A.

The drum-demand switching for all other pairs of channels (in the channels 1-18 group) is controlled in the same manner as described above. The last 18 channels (channels 19-36) receive the DD 2 pulse from the drum-demand switching circuit in the same manner as described for the DD 1 pulses entering the first 18 channels.

4.8 SITE NEON INDICATION SWITCHING

Each LRI control panel (simplex maintenance console) has two sets of site identity neon indicators, identifying the P-site from which the channel is receiving information. The A set of indicators is active when the

channel is in the same status as the A machine; the B set is active when the channel is in the same status as the B machine. Switching is accomplished through a contact on the A or B signal relays which connects the four neons (as a group) to a +150V source.

4.9 STATUS INDICATION SWITCHING

Status indication switching causes a +10V level to be applied to set a 1 in an assigned core in the direct entry section of the MDI element. Periodically, these cores (organized as a core matrix) are read out to the computer. Thus, each computer is informed of the associated LRI channels and of the status of each channel. The signal relay contacts, used in status indication switching for channel 1, are shown in table 2–1. Similar circuitry and contacts, for each of the other channels, associate the channels with either the A or B computer.

CHAPTER 5
COMMON EQUIPMENT

5.1 INTRODUCTION

The common equipment of the long-range radar input element serves as a common path for data flowing from the 36 LRI channel sections to the LRI drum fields. As the LRI message is transferred to the drum field, the message is re-formed into two drum words (see figs. 2–3, 2–4, and 2–5 for message-drum word relationship), and three pieces of information are added. The three pieces of information added are:

a. Site identity, which provides identification of the long-range radar site originating a message.
b. Clock time, which indicates the time a message is transmitted to the drum, relative to the real time clock of the Central Computer System.
c. Drum word parity, which is a bit for each drum word to establish odd drum word parity.

The common equipment is duplex. That is, the equipment is duplicated, with the two sections designated common A and common B, respectively. One of the common sections (A or B) will be active while the other is either in off or standby status. The active section receives data from active channels for processing. The standby section, however, can be switched to replace the active section. Since only one common section is active at any one time, the assumption is made for purposes of discussion in this chapter that common A is the active section.

In addition to adding site identity, clock time, and parity bits to each message, the common equipment performs the following functions:

a. Sends the drum words to the LRI monitor.
b. Sends DD pulses in priority sequence when an empty drum slot becomes available. The messages from channels 1-18 are sent to drum field 1, and the messages from channels 19-36 are sent to drum field 2.
c. Informs the Drum System and LRI monitor when a drum word is being transferred to them.
d. Synchronizes the transfer of data to the Drum System with Drum System timing pulses.
e. Generates a series of timing pulses, for use throughout the LRI element, that are synchronized with OD pulses from the Drum System.
f. Generates visual alarms displayed on the maintenance console when certain error-causing conditions arise.

Figure 2–24 is a simplified block diagram of the LRI common A, showing the data flow and some of the control signals. A block-by-block discussion, keyed to this diagram, follows:

The drum-demand control circuit receives DD pulses from drum field 1 and drum field 2. The drum demand control circuit sends a DD pulse to the readout control circuits of channels 1-18, in order of priority, when an empty slot on drum field 1 is available (indicated by the reception of a DD 1 pulse). The highest priority channel (lowest channel number in channels 1-18) having a message ready for transfer to the Drum System initiates readout. The DD 2 pulse causes readout of the highest-priority-ready channel in the 19-36 chain.

The drum-word readout control circuit receives the write levels from the 36 channel sections and transmits a data-available-drum-field-1 pulse to the Drum System when one of the 1-18 channels is prepared to read out or transmits a data-available-drum-field-2 pulse to the Drum System, if one of the 19-36 channels is prepared to read out. The drum-word readout control circuit also sends the data-available pulses to the monitor. In addition, two read-out pulses are generated which are synchronized with the drum word 1 and 2 readout, respectively.

The site identity generator receives the write levels from the 36 channels and generates a binary site number for the message. The site identity, therefore, is generated by determining the channel on which a message was received, since each channel receives messages from only one site.

The clock continuously generates a binary count of the number of quarter-seconds that have elapsed between 16-second pulses from the central computer clock. This relative time output is included in drum word 2 so that the central computer can calculate the time between the writing and the processing of a message.

The drum word 2 parity generator generates the parity bit for drum word 2 by using the parity of the first message word and the parity of clock time to determine the required parity bits to give odd parity to the second drum word.

The drum-word-1 parity generator determines the parity bit of the first drum word from the message-word-2 parity and the site identity parity.

The site gates convert the site identity generator output into standard pulses synchronized with the read-

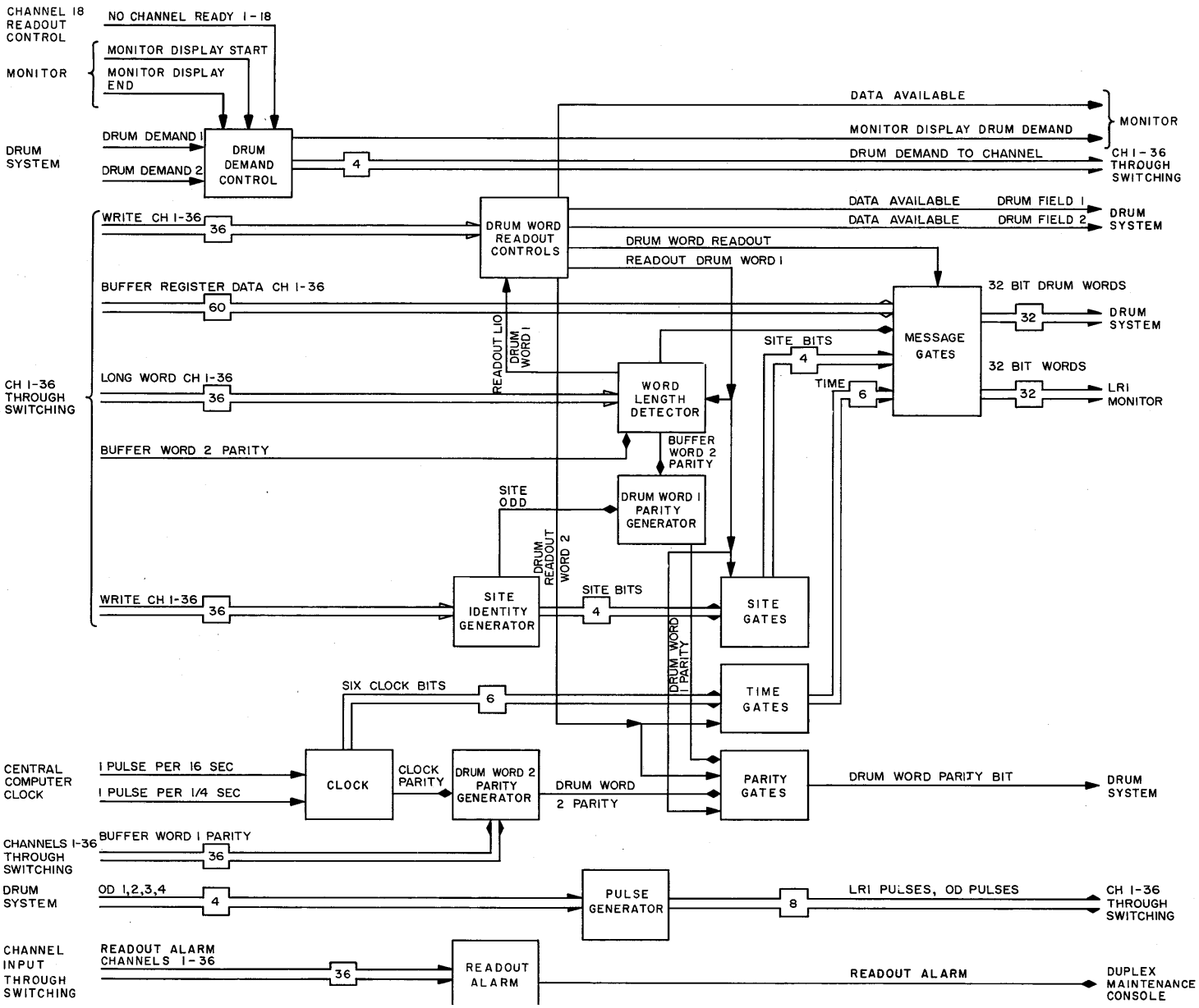


Figure 2–24. LRI Common A, Simplified Block Diagram

out of the remainder of drum word 1. The four site bits are then amplified in the message gate circuit and placed in the proper drum bit position.

The time gates convert the clock output into standard pulses synchronized with the readout of the remainder of drum word 2. The time bits are then inserted into their proper position in drum word 2 by the message gates circuit.

The parity gates receive the drum-word-1 and drum-word-2 parity bits from their respective generators, insert the parity bit of drum word 1 into the parity position when the first drum word is formed, and then insert the parity bit of drum word 2 into the second drum word parity position.

The message gates receive the output of the buffer registers from each channel. The buffer register containing message word 2 is read out first, and the bits are transferred to the proper positions in drum word 1. Ten μsec later, the word 1 buffer register transfers its contents (message word 1) to the drum as part of drum word 2. The site identity is also inserted into drum word 1, and the clock time is inserted in drum word 2.

5.2 PULSE GENERATOR

The pulse generator provides timing pulses which are synchronized with Drum System OD-timing pulses for use in the LRI element. Since the OD-timing pulses have a repetition frequency of 100,000 pps, they are not suitable for shifting the tape cores that have an optimum shifting rate of 50,000 cps. The pulse generator produces a group of LR pulses that have the necessary 50,000-pps repetition rate. The outputs of the generator are LR 2, LR 4, and LR 8 pulses and an LR 1/2 level, which are used in the channel input sections. The pulse generator also produces an OD-1-delayed (OD 1+1) 1-μsec pulse which is used to avoid close timing conditions in the channel input section.

Figure 2–25 is a simplified logic diagram, and figure 2–26 is a timing chart for the pulse generator. The Drum System generates four drum-timing pulses, designated OD 1, OD 2, OD 3, and OD 4. Each of the four pulses has a pulse repetition interval of 10 μsec; they are spaced at 2.5-μsec intervals, as shown on the timing chart. The OD 4 pulses are applied to the complement input of FF 1. Each OD 4 pulse changes the state of FF 1. Therefore, FF 1 is set by an OD 4 pulse and cleared by the following OD 4 pulse. The set out-

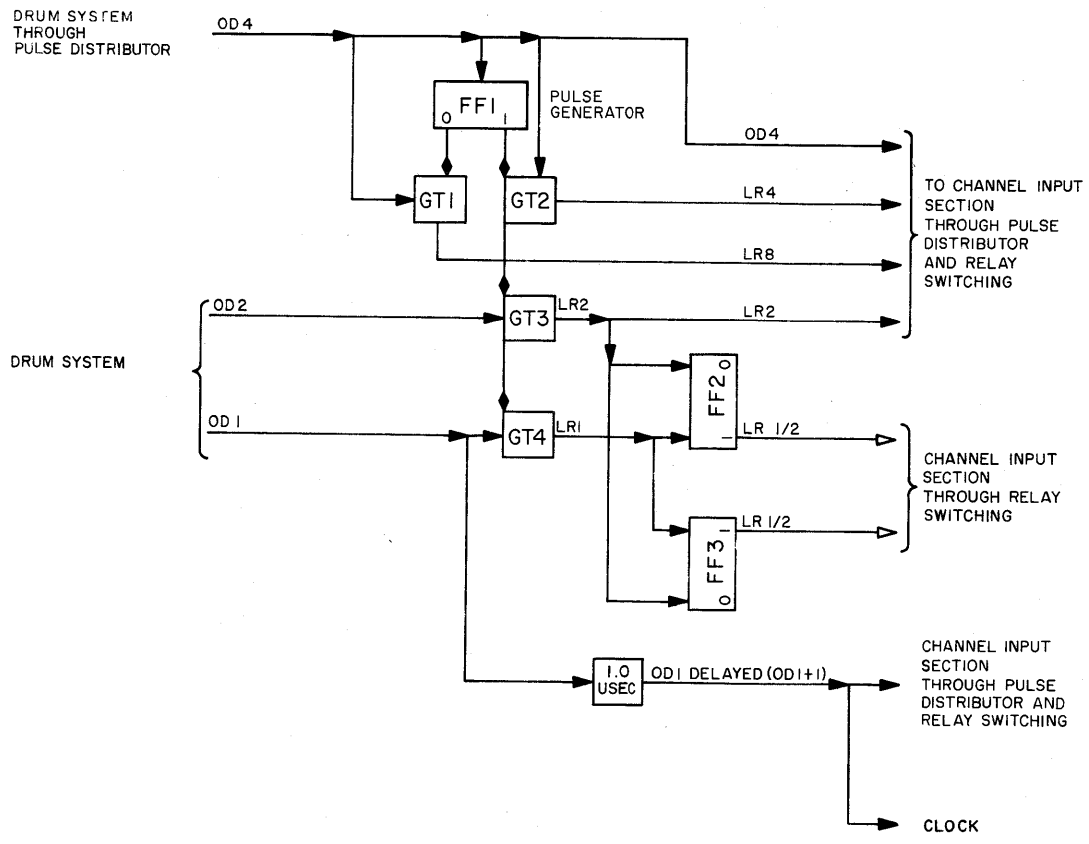


Figure 2–25. Pulse Generator, Simplified Logic Diagram

put of FF 1 conditions GT's 2, 3, and 4, while the clear output conditions GT 1.

Assuming the FF 1 is initially cleared, GT 1 is conditioned while GT's 2, 3, and 4 are deconditioned. The first OD 4 pulse is applied to GT 1, GT 2, and the complement input of FF 1. Because of the short time delay of FF 1, GT 1 remains conditioned long enough to pass the first OD 4 pulse before FF 1 is set. The OD 4 pulse passing through GT 1 is designated LR 8 and is followed in 2.5 μsec by an OD 1 pulse. This OD 1 pulse (LR 1) is passed by conditioned GT 4 and sets FF's 2 and 3. The OD 1 pulse is also applied to a 1-μsec delay circuit, and the delayed pulse output is sent to the channels and to the clock circuit. This OD-1-delayed pulse is designated OD 1+1. The following OD 2 pulse is applied to GT 3 (which is conditioned by the set output of FF 1) 2.5 μsec after this OD 1 pulse. The OD 2 pulse passed by GT 3 (designated LR 2) is sent to the channel equipment and also clears FF's 2 and 3. Flip-flops 2 and 3 are thereby set by the LR 1 pulse and cleared by the LR 2 pulse. The output of FF's 1 and 2 is a standard level, lasting 2.5 μsec, and is designated LR 1/2. The next OD 4 pulse appears 5 μsec after the preceding OD 2 pulse and passes through GT 2 before clearing FF 1. The output of GT 2 is designated LR 4. The OD 1 pulse following the second OD 4 pulse does not pass through GT 4 since FF 1 is now cleared, deconditioning GT's 2, 3, and 4. Gates 2, 3, and 4 remain deconditioned until the third OD 4 pulse sets FF 1. Consequently, the LR 1, 2, and 4 pulses are coincident with every even OD 1, 2, and 4 pulse, respectively. The LR 8 pulse is coincident with every odd OD 4 pulse. The LR pulses, therefore, have a repetition interval of 20 μsec (50,000-pps rate).

5.3 DRUM-DEMAND CONTROL

The LRI element supplies data to two drum fields of each computer. Drum field 1 of A or B receives

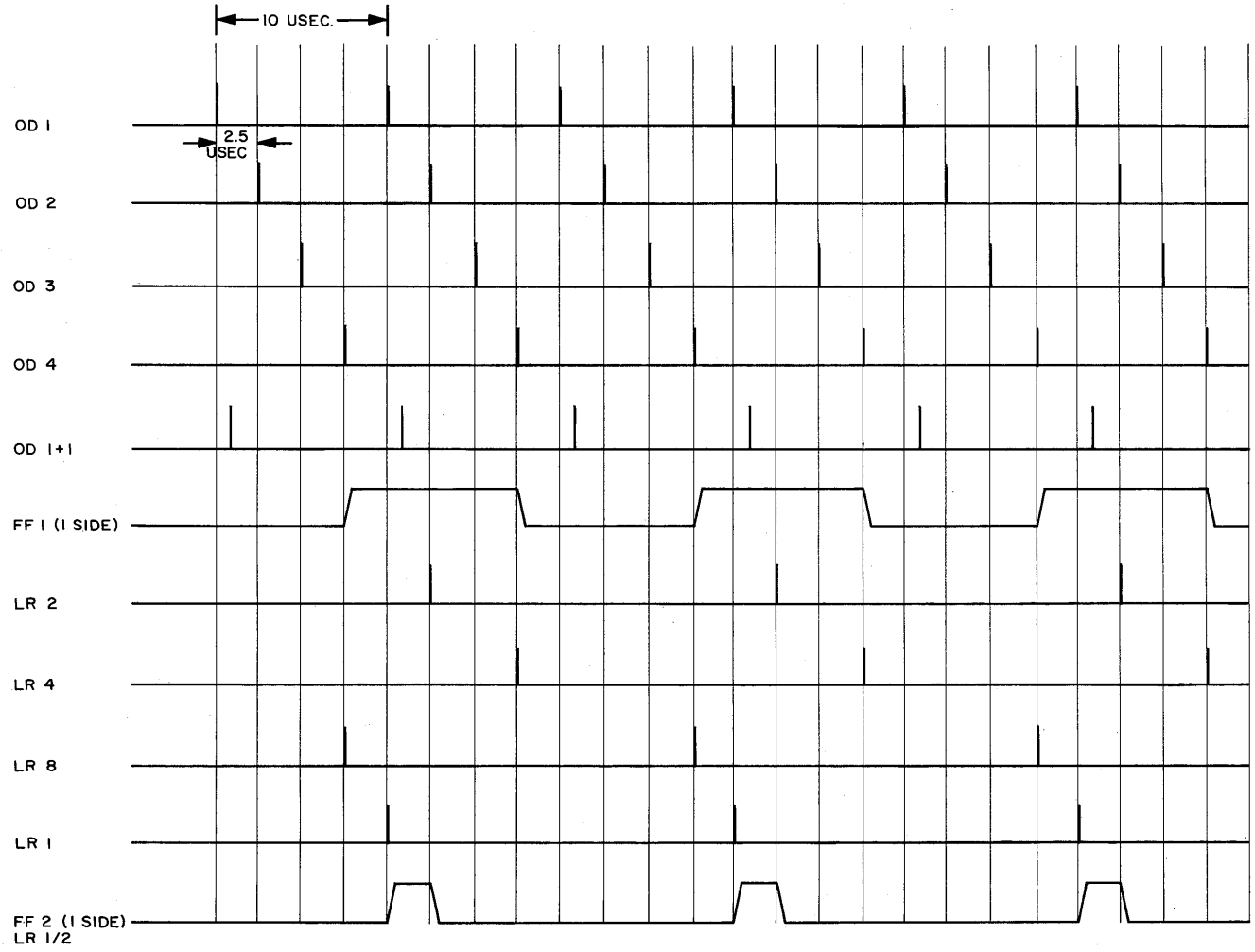


Figure 2–26. Pulse Generator, Timing Chart

information from channels 1-18 and drum field 2 of A or B receives data from channels 19-36. Two DD pulses from the A system are received by the drum-demand control circuit and are designated DD 1 (OD 3) and DD 2 (OD 3). The B drum-demand circuit receives B drum-demand pulses. The DD pulse is synchronized with an OD 3 drum-timing pulse. The appearance of the DD 1 (OD 3) pulse indicates an empty slot on drum field 1 which is therefore ready to receive data from a channel. The DD 2 (OD 3) pulse occurs when an empty position is available on drum field 2.

In the following discussion, the A computer will be considered active and the B computer standby. The A drum-demand control circuit sends the DD 1 (OD 3) pulse initially to the readout control circuit of channel 1, if active, or if not, to the next active channel and sends the DD 2 (OD 3) pulse initially to the readout control circuit of channel 19, if active. The DD 1 (OD 3) pulse initiates the readout of channel 1 if this channel is ready; that is, if channel 1 has a message stored in the word 1 and 2 buffer storage registers. If channel 1 does not contain a complete message, the DD 1 (OD 3) pulse is sent to the readout control circuit for channel 2, where it initiates readout if channel 2 is ready, or this pulse is passed on to the readout control circuit of channel 3 if it is active. In this manner, the DD 1 (OD 3) pulse from the active Drum System senses the condition of channels 1-18 and causes the readout of the lowest-number active channel that is ready. A single DD 1 pulse will cause only one of the 18 channels to read out since the DD 1 (OD 3) pulse indicates room on drum field 1 for only one message. This system is known as "readout by order of priority." For example, assuming that channels 1, 5, and 10 are ready and active, it is seen that the first A DD 1 (OD 3) pulse causes the contents of channel 1 to be transferred to the drum. The next DD 1 (OD 3) pulse (occurring when next drum slot is available) is passed through channels 1 (now empty) 2, 3, and 4, to channel 5 where it initiates readout. The third DD 1 (OD 3) pulses through channels 1-9 to cause readout of channel 10. In a similar manner, B DD pulses would be sent to the standby channels. The DD 2 (OD 3) pulse causes readout of active channels 19-36 and the B DD pulse causes readout of standby channels in the same manner. Although all channels are receiving data simultaneously and only one channel can read out data at a time, the speed of readout (20 μsec) is small enough, compared to the time necessary to receive a complete message approximately 40 ms, to permit all incoming messages to reach the drums.

Each DD 1 (OD 3) and DD 2 (OD 3) pulse is applied to its respective channel chain, except when the LRI monitor is displaying data. Operation of the LRI monitor, fully explained in Part 3, is briefly considered at this point to indicate its effect on the operation of the LRI element. The LRI monitor consists of a control unit and four display consoles at which LRI target data may be presented in PPI form. All LRI messages on their way to the Drum System are sent to the LRI monitor as well. Operators select target data for display at a console by specifying the site identity and the message label of the data of interest. The control unit compares these selection requests to the site identity and message label found in drum word 1. If a selection is accomplished, a display-started pulse is sent to the LRI element, inhibiting further readout during the display cycle, and target information in the second drum word is converted to a form suitable for presentation in a PPI display. The display requires 267.5 μsec from the time of the DD pulse which initiated the readout of the message. Ten μsec later, a display-ended pulse is returned to the LRI element confirming the fact that the display has ended, and the readout of LRI messages is resumed. The following example explains the need for preventing readout during display. Assume that one LRI monitor console requests the data received by channel 2 at the same time that another LRI monitor console requests data received by channel 3. Also assume that channels 2 and 3 contain complete messages at the same time. The first DD 1 (OD 3) pulse applied to channel 2 initiates readout. The data is transferred through the common section to the Drum System and to the monitor control. The monitor starts to arrange for the display on the LRI console that has requested the channel 2 data. The monitor takes 267.5 μsec to process and display the information. If, during this time, another DD 1 (OD 3) pulse should appear and cause readout of channel 3, the monitor console requesting channel 3 data could not display this information because the monitor control is still occupied with arranging for the display of the previous message. To prevent this loss of display, all DD pulses and, hence, all readouts are inhibited during the display time.

A simplified logic diagram of the drum-demand circuit is shown in figure 2–27. The discussion is divided into two parts: the generation of drum-demand pulses and the inhibiting of drum-demand pulses during LRI monitor display time.

5.3.1 Generation of Drum-Demand Pulses

The drum-demand control circuit receives DD pulses from drum fields 1 and 2. A DD 1 (OD 3) or a DD 2 (OD 3) pulse is received when an empty slot is available on drum field 1 or drum field 2, respectively, indicating that the drum field is ready to accept a message. Flip-flop 1 is set (unless a display is taking

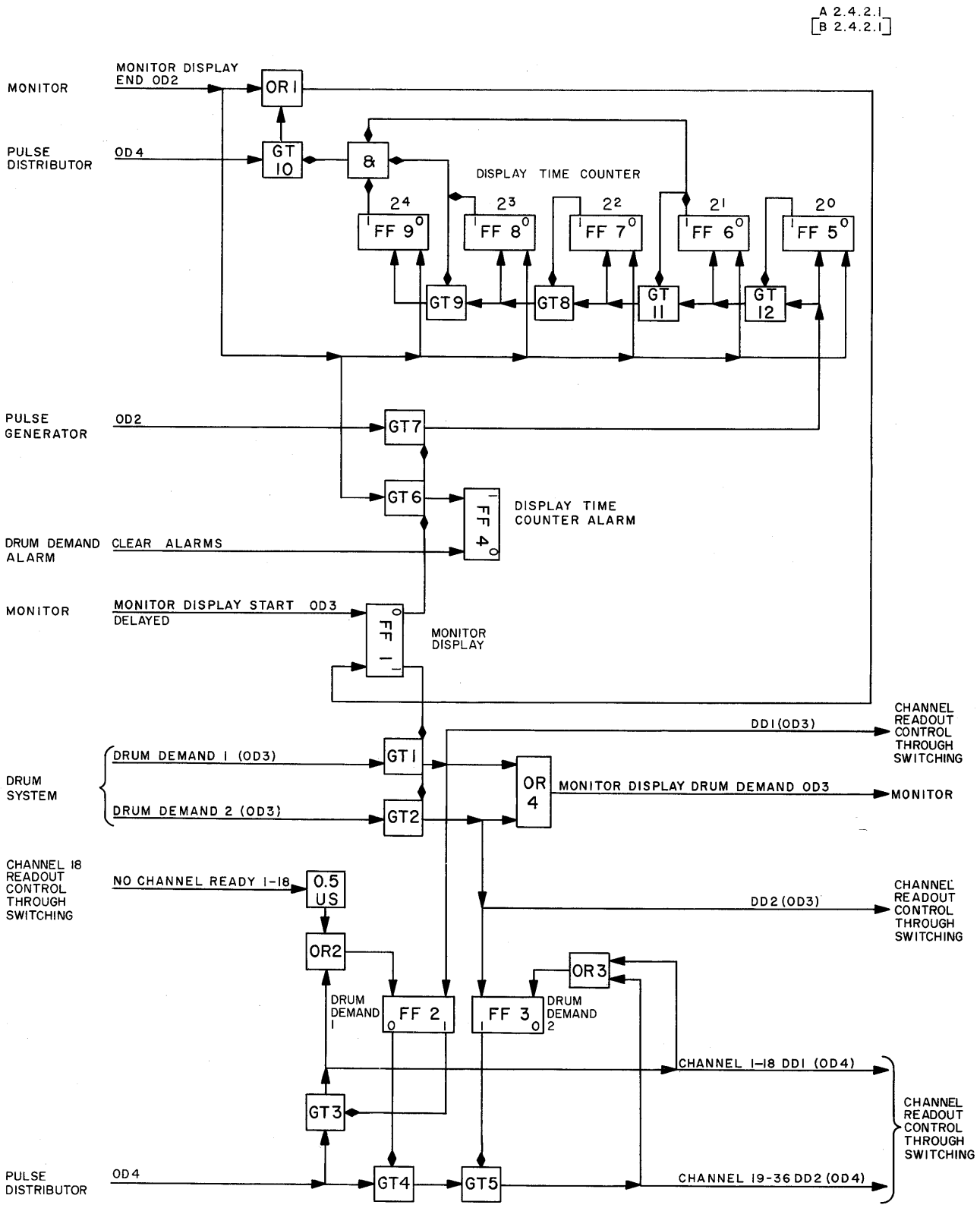


Figure 2–27. Drum-Demand Control, Simplified Logic Diagram

place). The set output of FF 1 conditions GT's 1 and 2, permitting the DD pulses to pass. There are three possible cases regarding the reception of DD pulses. They are:

Case 1 – DD 1 pulse received.

Case 2 – DD 2 pulse received.

Case 3 – DD 1 and 2 pulses received simultaneously.

5.3.1.1 Case 1: Drum-Demand 1 Pulse Received

The DD 1 pulse is received when an empty slot on drum field 1 is in position to receive data (fig. 2–28). Drum field 1 receives the data from channels 1-18. The DD 1 pulse passes through GT 1. This DD 1 (OD 3) pulse is sent to the readout control circuit of channel 1

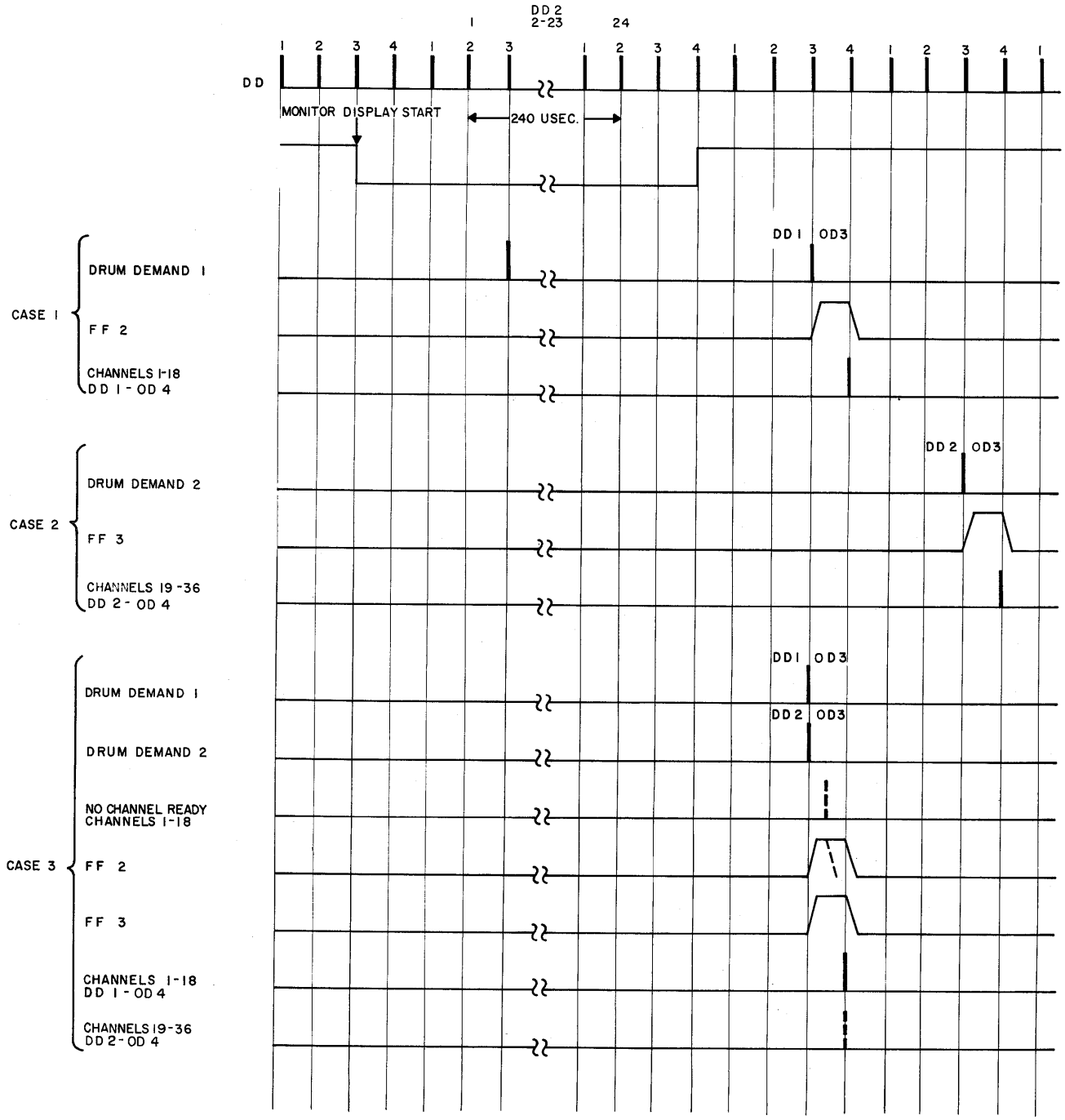


Figure 2–28. Drum-Demand Control, Timing Chart

where it will initiate readout (if a channel is ready), or else be passed to the next and following channel. The DD 1 (OD 3) pulse is passed through OR 4 to the LRI monitor (where it indicates the passage of a message to the Drum System). The pulse also sets FF 2. The set output of FF 2 conditions GT 3 which then passes the following OD 4 pulse. This channels 1-18 DD 1 (OD 4) pulse clears FF's 2 and 3 through OR's 2 and 3, respectively, and also is applied to the readout control circuits of channels 1-18. The lowest-numbered ready channel in channels 1-18 is then read out.

5.3.1.2 Case 2: Drum-Demand 2 Pulse Received

The DD 2 pulse is received when an empty slot on drum field 2 is in position to receive data from one of the last 18 channels (channels 19-36). The DD 2 pulse passes through GT 2 and is then designated DD 2 (OD 3). This DD 2 (OD 3) pulse is sent to the readout control circuit of channel 19 where it either initiates readout or is passed to channels 20, 21, etc. The DD 2 (OD 3) pulse passes through OR 4 to the LRI monitor and is also used to set FF 3. The set output of FF 3 conditions GT 5. Gate 4 is also conditioned by the clear output of FF 2 (normally cleared). The next OD 4 pulse passes through GT's 4 and 5 as a channels 19-36 DD 2 (OD 4) pulse that is applied to the readout control circuits of channels 19-36. The lowest-numbered ready channel will then read out after receiving the DD 2 (OD 3) and the channels 19-36 DD 2 (OD 4) pulse.

5.3.1.3 Case 3: Drum-Demand 1 and Drum-Demand 2 Pulses Received Simultaneously

Since channels 1-18 have higher priority than channels 19-36, the simultaneous arrival of DD 1 and DD 2 pulses causes readout of one of the channels 1-18. However, if none of the first 18 channels is ready, one of the channels 19-36 chain is permitted to read out.

The simultaneous arrival of DD 1 and DD 2 pulses causes the DD 1 (OD 3) and DD 2 (OD 3) pulses to be generated. Flip-flops 2 and 3 are both set. The following OD 4 pulse is passed by GT 3, as a DD 1 (OD 4) pulse which clears FF's 2 and 3 and is also sent to the readout control circuits of channels 1-18.

However, should none of the channels in the 1-18 chain be ready, the DD 1 (OD 3) pulse, coming out of channel 18, is delayed 5 μsec and clears FF 2 through OR 2. This is illustrated on the timing chart by the dotted no-channel-ready pulse, which causes FF 2 to be cleared (dotted fall line), permitting the channels 19-36 DD 2 (OD 4) pulse to appear (dotted pulse). The OD 4 is then passed through GT's 4 and 5 as a channels 19-36 DD 2 (OD 4) pulse. Therefore, when both DD 1 and DD 2 pulses appear simultaneously, the resulting pulses generated are the same as those produced for a DD 1 pulse (case 1), unless channels 1-18 are not ready, in which case, the results are the same as those for a DD 2 pulse received alone (case 2).

5.3.2 Inhibiting of Drum-Demand Pulses during LRI Monitor Display

The inhibition of DD pulses during LRI monitor display time, discussed in 5.3, follows the time sequence given below:

a. Time zero: DD pulse initiates the display cycle in the LRI monitor.
b. 10.0 μsec: Display-start pulse (OD 3), fed from the LRI monitor, clears FF 1, deconditioning GT's 1 and 2. Reception of DD 1 and 2 pulses is thereby prevented. Clear side of FF 1 conditions GT 7.
c. 17.5 μsec: OD 2 pulses begin to pass GT 7, stepping binary counter (FF 5 through FF 9 and GT's 8, 9, 11, and 12).
d. 267.5 μsec: OD 2 count reaches 26. FF's 6, 8, and 9 are set, satisfying AND, which conditions GT 10.
e. 272.5 μsec: OD 4 pulse passes GT 10 and OR 1, setting FF 1. The drum-demand circuit is thereby activated.
f. 277.5 μsec: Display-end pulse is fed from the LRI monitor, resetting counter.
g. 280 μsec: First DD pulse, after end of display, is passed.

In the event of a failure of the binary counter, the display-end pulse at 277.5 μsec passes through OR 1, setting FF 1, thus assuring the passage of DD pulses. The pulse also passes through GT 6, setting the display time counter alarm, FF 4. The alarm neon associated with FF 4, on the duplex maintenance console, lights, indicating faulty counter operation. When the circuit operates normally, GT 6 is deconditioned at 272.5 μsec by setting FF 1. Accordingly, the display-end pulse is not passed 5 μsec later.

If the LRI monitor does not provide a display-end pulse (because of circuit failure), the counter is not reset. The AND remains satisfied and GT 10 remains conditioned. FF 1 may be cleared by a display-start pulse, but it is set 2.5 μsec later by an OD 4 pulse passing through GT 10. Therefore, GT 7 is again deconditioned, preventing the counter from being stepped, and GT's 1 and 2 are conditioned, passing DD 1 and DD 2 pulses. Under these circumstances, the circuit has no effect on drum-demand pulses. Thus, it may be seen that the display-end pulse assures the resumption of DD pulses in case of counter failure, but the failure of the LRI monitor does not cause the inhibition of DD pulses.

5.4 SITE IDENTITY GENERATOR

The site identity generator provides a means of identifying the LRI radar site that has sent an LRI message. A binary site number is generated and added by the LRI element to the message being sent to the Drum System. The incoming message does not contain the identity of the site that transmitted the message; this shortens the message length and conserves transmission time.

Each radar site transmits LRI messages to the Central, using a separate telephone line to one of the input channels. A site identification number is assigned to each message, according to the channel on which it is received.

The write level (OD 4 to OD 1+1) from the readout control circuit of each channel is sent, through switching, to a separate site identity can in the common equipment. The write level is generated during readout of a message by the readout control circuit in the channel equipment. Figure 2-29 shows the site identity cans for channels 1 and 2 if the binary site numbers for channels 1 and 2 are assumed to be 1001 and 0010, respectively. Channel numbers are assigned as a function of site and priority. The channel 1 site can is wired so that the write signal from channel 1 produces 1's (+10V) on site bit lines 1 and 4. Site bit lines 2 and 3 are connected to −30V, indicating binary 0's on these lines. Since the site number for channel 1 has an even

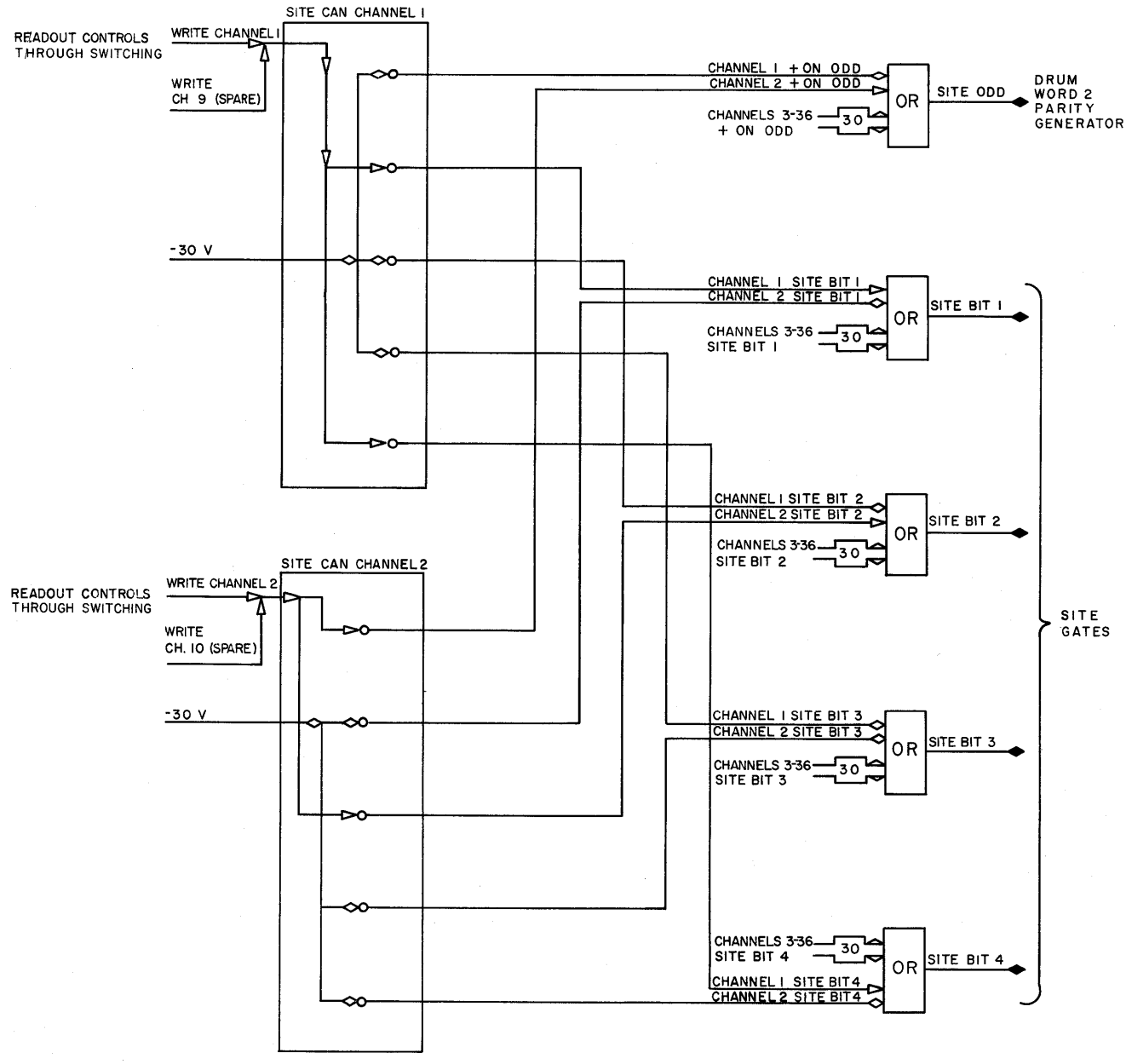


Figure 2—29. Site Identity Generator, Simplified Logic Diagram

parity (even number of 1's on 1001), the plus on-site-odd line is connected to —30V. The channel 2 site number is generated by wiring the channel 2 site can so that the write level from channel 2 produces a 1 on site bit line 2, and a —30V causes zeros on site bit lines 1, 3, and 4 (odd number of 1's in site identity). The plus-on-site odd is made +10V since it is connected to the write level for that channel.

The write level from a channel is generated when the channel is reading out the first drum word. Therefore, the binary site number of the channel is generated during the transfer of the first drum word, and is transferred to the site gates when the second message-word data is transferred to the message gates.

The outputs of these OR's are designated site bits 1, 2, 3, and 4 and site odd. When none of the channels is reading data (no write levels), the inputs to (and, consequently, the outputs of) these five OR circuits are 0 (—30V). However, when channel 1 generates a write signal, 1's are produced on the channel site bit 1 and site bit 4 lines. These 1 inputs to their respective OR circuits cause the site-bit-1 and site-bit-4 outputs to be 1's for the duration of the write level. The site-bit outputs of the OR's are sent to the site gates where each site-bit-1 will condition a gate and permit a standard pulse to pass to the Drum System. When channel 1 is reading out, a 1 is inserted in the first and fourth site identity bit positions on the drum while 0's are being written in the second and third positions. The site odd output is sent to the drum word parity generator where it is used to determine the parity bit of the drum word. During the readout of channel 1, the site odd output is a 0.

In a similar manner, the readout of any channel causes the site identity number of that channel to be transferred to the site gates and the parity of the site number to be indicated to the drum word 1 parity generator.

The telephone-line inputs to a channel may be connected to a spare channel in the event of failure of a regular channel. The write-level input to each site identity can is, therefore, from the regular channel or substituted channel. The correct site identity is generated for messages received on the spare channel. For example, when channel 1 equipment becomes inoperative, the telephone lines normally connected to channel 1 are switched to channel 9 (the spare channel for the odd channels from 1 through 17). The messages now received by channel 9 originate from the radar site normally connected to channel 1. Since the channel 1 site can is wired to produce the site identity number for this site, the write signal from channel 9 is now connected to the channel 1 site can. In this manner, the correct site identity is added to messages read out of channel 9.

5.5 CLOCK

The clock circuit records the relative time at which a message is transferred to the Drum System and inserts this information into the messages as part of drum word 2. The central computer uses this clock information to determine the interval between the time of transfer to the Drum System and the time of processing by the Central Computer. The relative time at which the message is transferred is indicated by six binary bits in the second drum word. The basic time interval is one quarter-second; therefore, the time cycle is 64 quarter-seconds (16 seconds).

The six binary bits are generated by the clock circuit from successive standard pulses occurring every quarter-second. A binary output is produced indicating the number of quarter-seconds that have elapsed. The clock resets itself to zero every 16 seconds, and counting is continuous. The clock circuit is synchronized by pulses from the Central Computer clock.

The clock circuit (fig. 2–30) is basically a 6-stage binary counter that provides a continuous indication of the total number of quarter-seconds that have elapsed. The counter is stepped every quarter-second by a drum pulse synchronized with a standard pulse from the central computer clock. The clock circuit also contains a parity generator which indicates the parity at any time of the clock output. A clock test circuit is included which tests the clock every 16 seconds and generates a clock alarm in the event of an incorrect reading. The logic discussion of the clock circuit is divided into four parts:

a. Clock stepping and synchronizing
b. Clock indication (6-stage binary counter)
c. Clock parity generator
d. Clock test

5.5.1 Clock Stepping and Synchronizing

The stepping and synchronizing section of the clock circuit consists of FF's 8, 9, and 10 and GT's 8, 9, and 10. Standard pulses from the central computer clock, occurring at a rate of 4 pps (quarter-second pulses), set FF 9. The set output of FF 9 conditions GT 9, permitting an OD 3 pulse to pass. The OD 3 pulse sets FF 10, conditioning GT 10. An OD 1+1 pulse is passed by GT 10. This OD 1+1 pulse clears FF's 9 and 10 and is used to step the clock. A single OD 1+1 pulse is passed for each quarter-second pulse applied to the circuit. Since the quarter-second pulses and OD pulses are not synchronized, the time delay between the arrival of the quarter-second clock pulse and the generation of the OD 1+1 stepping pulse varies from a minimum of 6 μsec (OD 3 to OD 1+1) to a maximum of 16 μsec (OD 3 and quarter-second

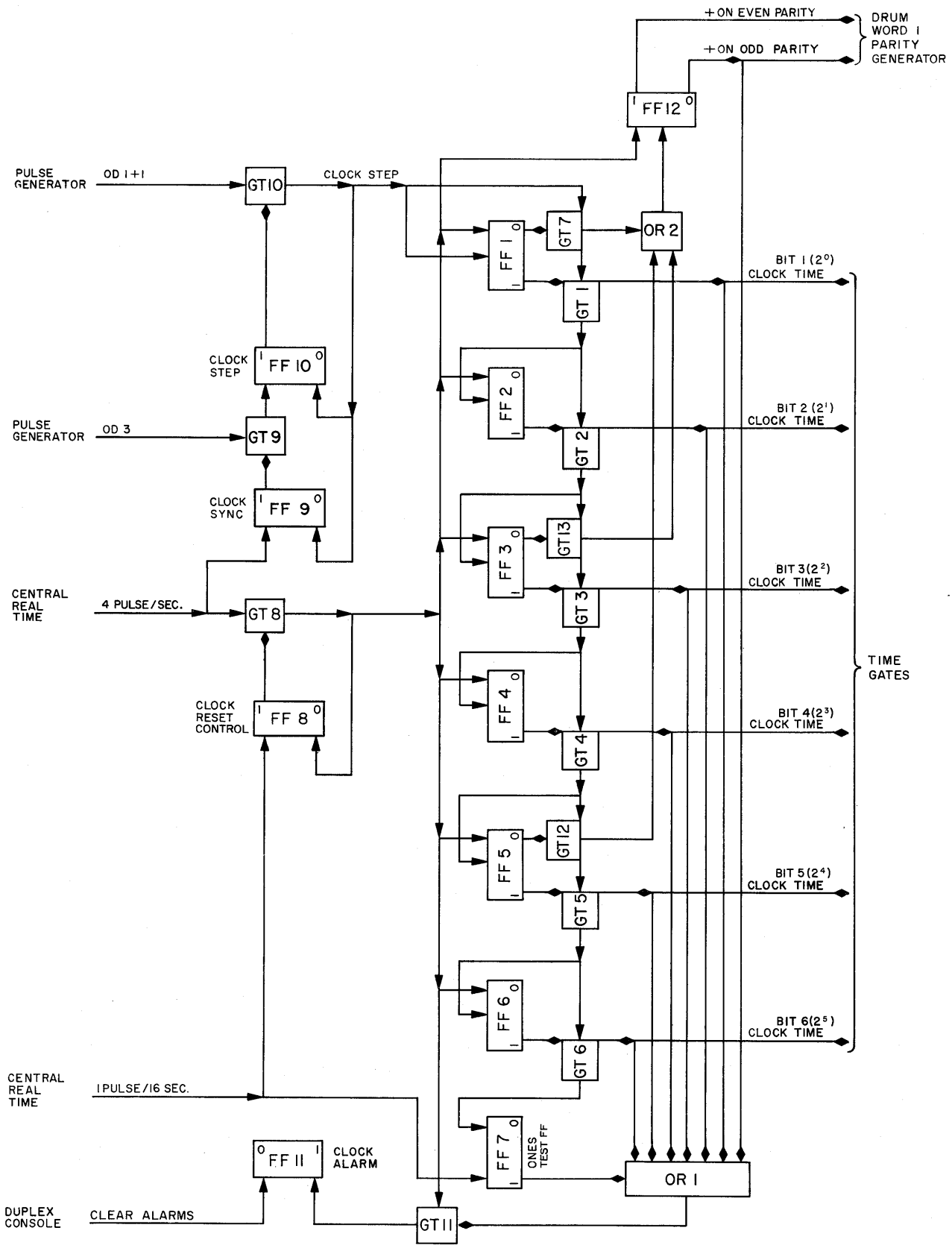


Figure 2–30. Clock, Simplified Logic Diagram

pulses occurring simultaneously). The clock is synchronized with the central computer clock by a synchronizing pulse which occurs every 16 seconds. This pulse sets FF 8; this conditions GT 8 which passes the following quarter-second pulse and clears the 6-stage binary counter. The next synchronizing 16-second standard pulse occurs after 63 quarter-second pulses have been received (coincident with the 64th quarter-second pulse). If the counter has operated correctly, the flip-flops will be cleared by the 64th quarter-second pulse, and the 16-second standard pulses serve only to check clock synchronism (an alarm is generated if the clock has not been reset). The timing chart (fig. 2–31) shows the timing relationship in the clockstepping and synchronizing section of the clock circuit. Because of the time delay of the stepping circuit, the reset pulse occurs between the 64th and 1st stepping pulses.

5.5.2 Clock Indication (6-Stage Binary Counter)

The 6-stage binary counter (FF's 1 through 6 and GT's 1 through 6), produces the six clock bits which are sent to the Drum System. The set output of each flip-flop is a single binary clock bit (with a binary value as shown in fig. 2–30), which indicates the

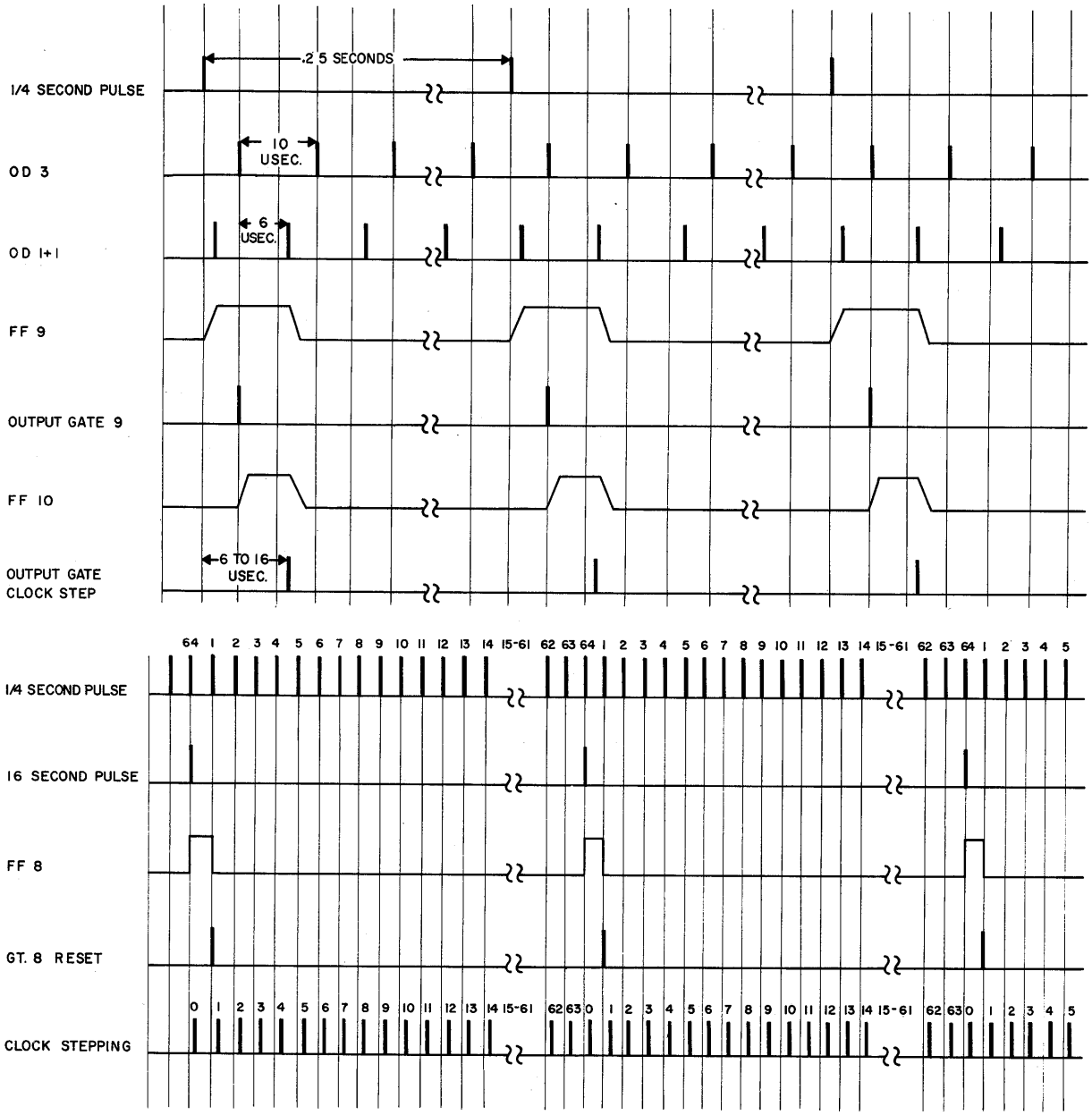


Figure 2–31. Clock-Stepping and Synchronizing, Timing Chart

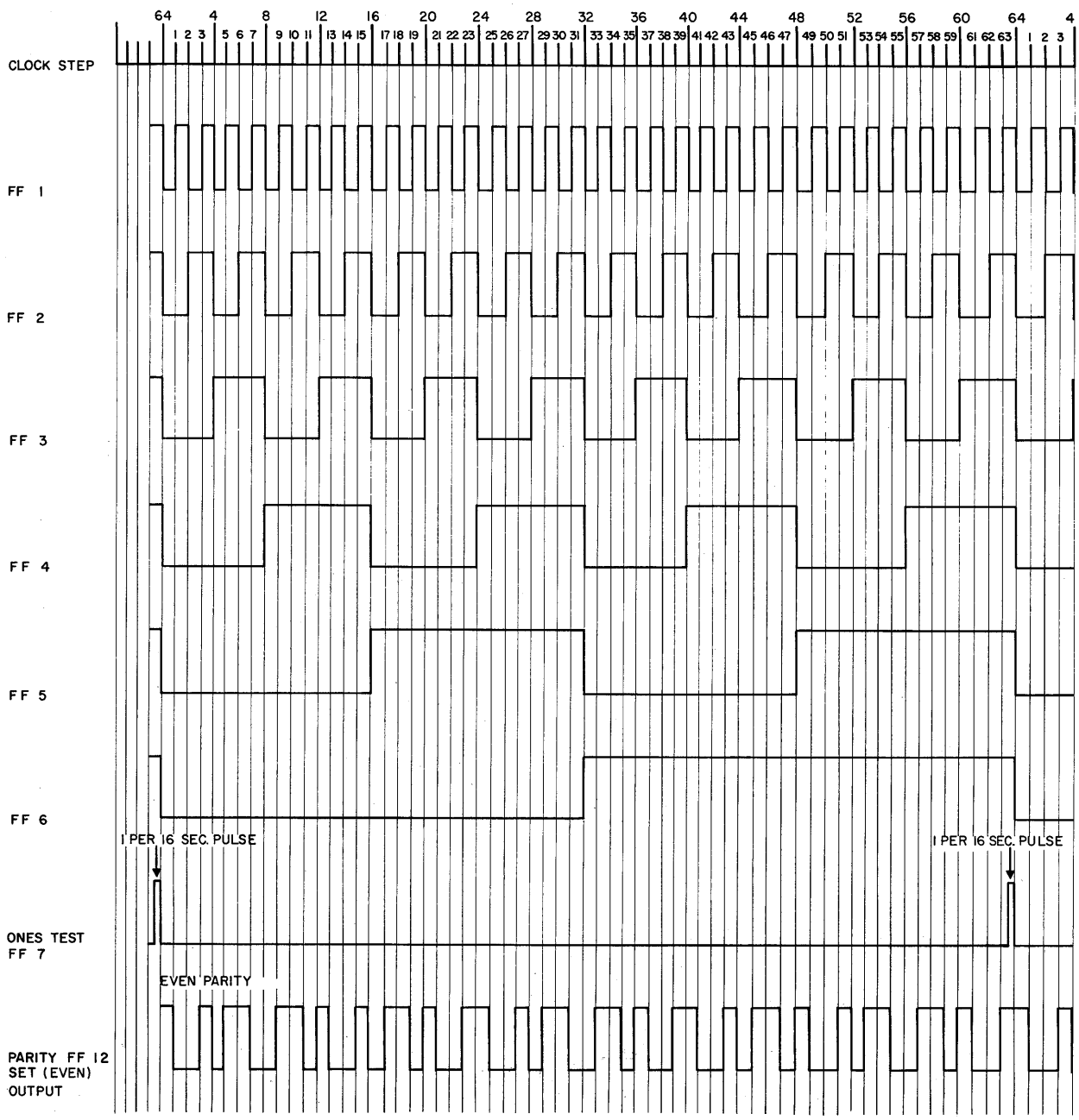


Figure 2–32. Clock Timing Chart, Binary Counter Output

number of quarter-second stepping pulses that have occurred since the last 16-second synchronizing pulse. The timing chart (fig. 2–32) shows the output of the six flip-flops for any number of clock steps. The clock bit outputs are considered to be 1's when the flip-flop is set and 0's when the flip-flop is cleared. The six clock bits are sent to the time gates for transfer to the Drum System.

5.5.3 Clock Parity Generator

The parity (odd or even number of 1 bits) in the clock at any time must be determined in order to generate (in conjunction with the parity of message word 1) the correct parity for drum word 2. The parity of the clock for each quarter-second is indicated on the timing chart (fig. 2–32).

The parity generator consists of FF 12, OR 2, and GT's 7, 13, and 12. Flip-flop 12 is set for an even clock parity and cleared for an odd clock parity. Gate 7 passes a standard pulse whenever the first bit of clock time changes from 0 to 1 (hence, whenever FF 1 is set). When FF 1 is in the cleared state (clock bit 1 is 0), GT 7 is conditioned by the 0 output. The clock-step

pulse is simultaneously applied to GT 7 and to the complement input of FF 1. Because of the time delay necessary to change the state of FF 1, the stepping pulse passes through GT 7 to OR 2, just before FF 1 is set. In the same manner, GT 13 passes a standard pulse to OR 2 each time FF 3 is set (bit 3 changing from 0 to 1). Gate 12 passes a standard pulse to OR 2 each time FF 5 is set (bit 5 changing from 0 to 1). The output of OR 2 is therefore a standard pulse appearing each time clock bit 1, 3, or 5 changes from 0 to 1. This output of OR 2 is applied to the complement input of parity check FF 12. The output of FF 12 then changes each time the 1, 3, or 5 clock bit changes from 0 to 1. Flip-flop 12 is set (even parity) at the start of a counting cycle. The first clock stepping pulse produces a 000001 binary output. Since the first binary bit has changed from 0 to 1, the parity FF 12 is changed to indicate an odd parity. The second stepping pulse changes the clock output to 000010. Since neither the 1, 3, or 5 clock bit has changed from 0 to 1, the parity flip-flop remains cleared, correctly indicating odd parity. Table 2–2 shows the binary output for each stepping pulse along with the parity of each number. Examination of this table will show that each time the parity is changed, either the 1, 3, or 5 clock bit will change from a 0 to a 1. After 64 quarter-second pulses have been counted, the parity should be even. In case of an incorrect count, the reset occurring once every 16 seconds will set FF 12 after the 64th quarter-second pulse, insuring the proper starting position for the parity generation. The two outputs of FF 12 (odd and even parity) are transferred to the drum word 2 parity generator where the clock parity and message word 1 parity are combined so that the correct drum word 2 parity bit is generated.

5.5.4 Clock Test

The clock is tested every 16 seconds to determine if a correct and complete count has been made. The LRI clock alarm neon (duplex maintenance console) is turned on if an error occurs in the clock count.

Assuming that the clock starts from a cleared condition (FF's 1 through 7 cleared), after 63 quarter-seconds, the six clock bits should all be 1's (FF's 1 through 6 set), and GT's 1 through 6 conditioned. The 16-second pulse which occurs simultaneously with the 64th quarter-second pulse then sets FF's 7 and 8. The 64th stepping pulse passes (6 to 16 μsec after the 64th quarter-second pulse) through GT's 1 through 6, clearing FF 7 and complementing FF's 1 through 6 to the clear side. Flip-flop is called the 1's test flip-flop since it is cleared only if clock bits 1 through 6 were 1's after the 63 count.

After the 64th stepping pulse has appeared, FF's 1 through 7 should be cleared and the parity FF 12 set (even parity for 000000). This zero condition is tested by applying the set (1) outputs of FF's 1 through 7 and the cleared (odd) output of FF 12, to OR 1. If any of these inputs to OR 1 contains a 1, then the output of OR 1 will condition GT 11. Flip-flop 8, which was set by the 16-second pulse, conditions GT 8, which permits the first quarter-second pulse to strobe GT 11, to clear FF's 1 through 6 and FF 8, and to set FF 12. When GT 11 is conditioned by a set output from FF's 1 through 7 or by an odd (cleared) output from FF 12, the first quarter-second pulse passes through GT 11 and sets the clock alarm FF 11 which lights a clock alarm neon on the duplex maintenance console. The first quarter-second pulse also acts as a reset signal for the clock and sets FF 12 to indicate an even initial parity. The clock is then stepped by the first clock-step pulse occurring at least 6 μsec after the first (reset) quarter-second pulse. When the clock has correctly counted 64 stepping pulses, FF's 1 through 7 will have cleared after 64 pulses, and the reset pulse occurring between the 64th and 1st stepping pulses will have no effect.

5.6 DRUM WORD READOUT CONTROLS

The drum-word readout controls circuit initiates the readout of messages to the drum by the generation of data-available and word-read out pulses. The circuit (fig. 2–33) receives the write (OD 4 to OD 1+1) levels from the readout control circuits in the 36 channels. A write level is generated by a channel during the readout of the message. Only one channel at a time is able to read out messages: therefore, only one of the 36 write levels is present at any one time. The write-level lines for channels 1-18 are combined into a single output (channels 1-18 write) by OR 1. This combined output produces a +10V write level when any one of the first 18 channels is read out. Similarly, the channels 19-36 write lines are combined into a single output (channels 19-36 write) by OR 2. The following pulses are generated by the circuit when one of the channels is read out (producing a write level):

a. Data-available-drum-field-1: Two successive OD 1+1 standard pulses are sent to the Drum System when a write level is produced by one of the first 18 channels. Since data from channels 1-18 is written on drum field 1, these pulses indicate to the Drum System that drum field 1 is to receive the data.

b. Data-available-drum-field-2: Two successive OD 1+1 standard pulses are sent to the Drum System, indicating that one of the last 18 channels (channels 19-36) is transferring data to drum field 2.

c. Data-available-monitor: Two successive OD 1+1 standard pulses indicate to the monitor that

TABLE 2–2. CLOCK-BINARY COUNTER OUTPUT AND PARITY

¼ SEC	CLOCK BIT NO. 2^5	2^4	2^3	2^2	2^1	2^0	PARITY
64	0	0	0	0	0	0	E
1	0	0	0	0	0	1	O
2	0	0	0	0	1	0	O
3	0	0	0	0	1	1	E
4	0	0	0	1	0	0	O
5	0	0	0	1	0	1	E
6	0	0	0	1	1	0	E
7	0	0	0	1	1	1	O
8	0	0	1	0	0	0	O
9	0	0	1	0	0	1	E
10	0	0	1	0	1	0	E
11	0	0	1	0	1	1	O
12	0	0	1	1	0	0	E
13	0	0	1	1	0	1	O
14	0	0	1	1	1	0	O
15	0	0	1	1	1	1	E
16	0	1	0	0	0	0	O
17	0	1	0	0	0	1	E
18	0	1	0	0	1	0	E
19	0	1	0	0	1	1	O
20	0	1	0	1	0	0	E
21	0	1	0	1	0	1	O
22	0	1	0	1	1	0	O
23	0	1	0	1	1	1	E
24	0	1	1	0	0	0	E
25	0	1	1	0	0	1	O
26	0	1	1	0	1	0	O
27	0	1	1	0	1	1	E
28	0	1	1	1	0	0	O
29	0	1	1	1	0	1	E
30	0	1	1	1	1	0	E
31	0	1	1	1	1	1	O
32	1	0	0	0	0	0	O

TABLE 2–2. CLOCK-BINARY COUNTER OUTPUT AND PARITY (cont'd)

¼ SEC	CLOCK BIT NO. 2^5	2^4	2^3	2^2	2^1	2^0	PARITY
33	1	0	0	0	0	1	E
34	1	0	0	0	1	0	E
35	1	0	0	0	1	1	O
36	1	0	0	1	0	0	E
37	1	0	0	1	0	1	O
38	1	0	0	1	1	0	O
39	1	0	0	1	1	1	E
40	1	0	1	0	0	0	E
41	1	0	1	0	0	1	O
42	1	0	1	0	1	0	O
43	1	0	1	0	1	1	E
44	1	0	1	1	0	0	O
45	1	0	1	1	0	1	E
46	1	0	1	1	1	0	E
47	1	0	1	1	1	1	O
48	1	1	0	0	0	0	E
49	1	1	0	0	0	1	O
50	1	1	0	0	1	0	O
51	1	1	0	0	1	1	E
52	1	1	0	1	0	0	O
53	1	1	0	1	0	1	E
54	1	1	0	1	1	0	E
55	1	1	0	1	1	1	O
56	1	1	1	0	0	0	O
57	1	1	1	0	0	1	E
58	1	1	1	0	1	0	E
59	1	1	1	0	1	1	O
60	1	1	1	1	0	0	E
61	1	1	1	1	0	1	O
62	1	1	1	1	1	0	O
63	1	1	1	1	1	1	E
64	0	0	0	0	0	0	E

Note: E = Even, O = Odd

data is being transferred from one of the 36 channels to the Drum System.

d. Drum-word-readout: Two successive OD 1+1 pulses are synchronized with the readout of word 2 and word 1 buffers. These pulses strobe the message readout gates that send data to the drums.

e. Readout-drum-word-1: A single OD 1+1 pulse occurs when the second buffer word is being read out of the word 2 buffer register of a channel. Since the second buffer word is read out before the first buffer word, the first drum word is formed by the second buffer word plus site identity. The readout-drum-word-1 pulse strobes the site gates, thereby inserting the site identity into the first drum word.

f. Readout-drum-word-2: An OD 1+1 pulse occurs when the first buffer word is being read out (second drum word being formed). This pulse strobes the time gates, inserting the clock output into drum word 2.

g. Readout-L10: Because of previous circuitry, the readout of bit L10 was treated in a separate manner. For convenience in revising the circuitry, the bit L10 readout is still treated as a special situation. However, as a practical consideration, the readout control circuit generates two OD 1+1 strobing pulses which are sent to the L10 message gates. The two L10 (OD 1+1) pulses are synchronized with the drum word readout pulses to the remaining message gates.

The timing chart (fig. 2–34) illustrates the timing relationships for the generation of the above pulses. The buffer-word-readout signals are included on the timing chart.

The write outputs from channels 1-18 and channels 19-36 are combined by OR 1 and OR 2, respectively. When one of the channels 1-18 is sending a message to the drum, the output of OR 1 is up for the duration of the write level. The channels 1-18 write level conditions GT 1, which passes two successive OD 1+1 pulses (from the pulse generator) while the write level is present. These two OD 1+1 pulses are synchronized with the two word-buffer readout signals in the channel, with the first OD 1+1 pulse occurring during the readout of the word 2 buffer register, and with the second OD 1+1 pulse occurring during the readout of the word 1 buffer register. Since the data from channels 1-18 is transferred to drum field 1, the two OD 1+1

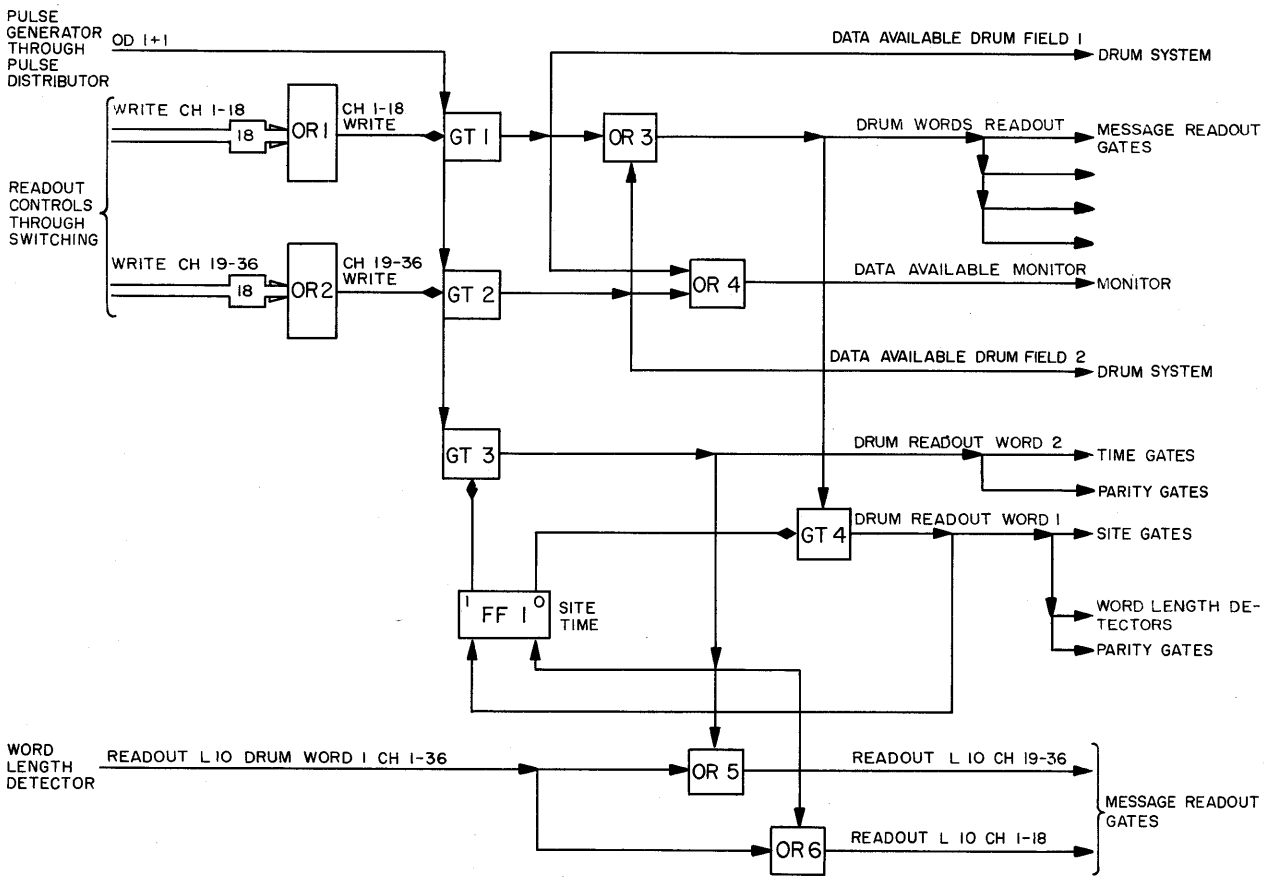


Figure 2–33. Drum Word Readout Controls, Simplified Logic Diagram

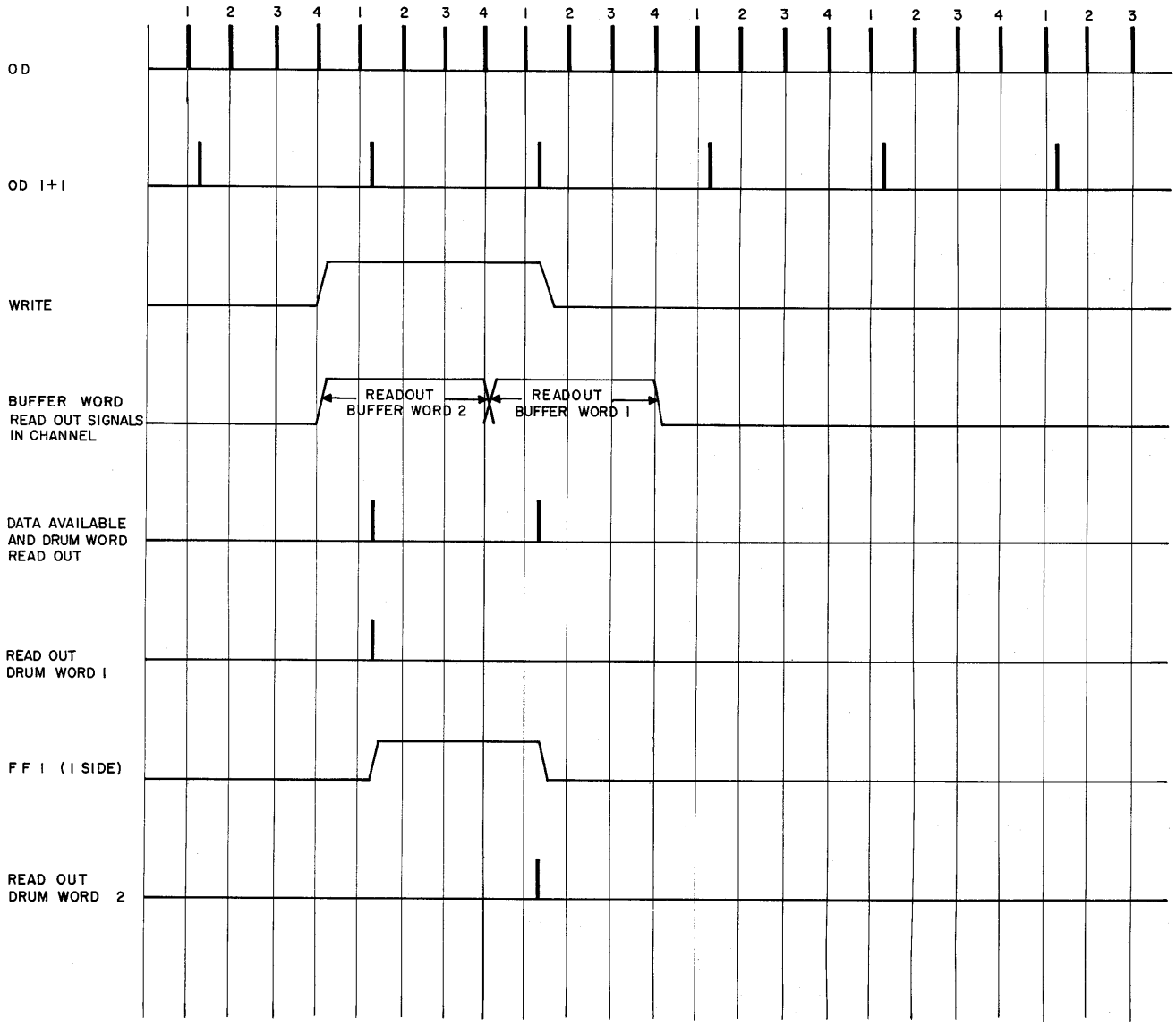


Figure 2–34. Drum Word Readout Controls, Timing Chart

pulses, passing through GT 1 when the channels 1-18 write level is applied, are sent to the Drum System as data-available-drum-field-1 pulses. These pulses indicate to the Drum System that data is being transferred to drum field 1. The two OD 1+1 pulses are also sent to the LRI monitor through OR 4 as data-available-monitor pulses which indicate to the monitor control circuit that an LRI message is being transferred to the drums. The message gates also receive the two OD 1+1 pulses through OR 3. The OD 1+1 pulses are used in the message gates circuit as strobing pulses for gates that are conditioned by the 1 bits of the message. Each gate in the message-gates circuit receives two message bits, one during word 2 buffer readout and the second during word 1 buffer readout. The first OD 1+1 strobing pulse is passed if the buffer word 2 message bit applied to a gate is a 1, and the second OD 1+1 pulse is passed if the buffer word 1 message bit is a 1.

Flip-flop 1 is initially cleared, thereby conditioning GT 4. The first OD 1+1 readout-drum-word-1 pulse is passed by GT 4. After passing through GT 4, the first OD 1+1 pulse sets FF 1, which deconditions GT 4 and conditions GT 3. Gate 3 then passes the second OD 1+1 pulse, which clears FF 1. The output of GT 4 is therefore the first OD 1+1 pulse and is designated the readout-drum-word-1 pulse since it occurs during the formation of the first drum word. Gate 3 passes the second OD 1+1 pulse and is designated the readout-drum-word-2 pulse since it occurs during the readout of the second drum word. The readout-drum-word-1 pulse occurs during the readout of the word 2 buffer and is the pulse that writes drum word 1. Since site

identity is added to buffer word 2 to form drum word 1, the readout-drum-word-1 pulse strobes the site gates, thereby permitting the site identity to be inserted into the first drum word. Similarly, the readout-drum-word-2 pulse strobes the time gates, permitting the clock time to be inserted into drum word 2 along with buffer word 1.

OR 5 and OR 6 are fed by a drum-readout-word-2 pulse and by a readout-L10-drum-word-1-channels-1-36 pulse. Consequently, both OR 5 and OR 6 have an OD 1+1 output during the readout of buffer word 1 and during the readout of buffer word 2. The outputs of OR 5 and OR 6 go to the L10 message readout gates for channels 19-36 and channels 1-18 respectively.

The same pulses generated for channels 1-18 are generated for channels 19-36, with the exception of the data-available-drum-field-1 pulse. The channels 19-36 write level conditions GT 2 which passes two OD 1+1 pulses to the Drum System as data-available-drum-field-2 pulses. These pulses indicate to the Drum System that the data being read out of a channel is intended for drum field 2. The remaining pulses are all generated exactly as they were for the channels 1-18-write level, with the data-available-drum-field-2 pulses replacing the data-available-drum-field-1 pulses when the channels-19-36-write level is present.

5.7 DRUM WORD 1 PARITY GENERATOR

The drum word 1 parity generator circuit generates the parity bit necessary to make an overall odd count of 1 bits (including the parity bit) in drum word 1. Drum word 1 is made up of message word 2, site identity, and the parity bit. If the combined number of 1 bits in message word 2 (buffer word 2) and in site identity is even, the parity bit is 1; if the combined number of 1 bits in buffer word 2 and in site identity is odd, the parity bit is 0. The number of 1 bits in site identity is indicated by the site-odd input from the site identity generator. This input is a 1 when the site identity data being sent to the drum contains an odd number of 1 bits, it is a 0 when the site identity contains an even number of 1 bits. The number of 1 data bits in message word 2 (buffer word 2) is indicated by the buffer word 2 parity input. The number of 1 bits in an LRI message is even, and the number of 1 bits in message word 1 is odd; therefore, the number of 1 bits in message word 2 is odd. Buffer word 2 must have either an odd number of 1 data bits and a 0 parity bit or an even number of 1 data bits and a 1 parity bit. The buffer-word-2-parity-input line indicates an even number of 1 data bits by a +10V level and an odd number of 1 data bits by a −30V level, during readout of buffer word 2. The drum word 1 parity generator circuit receives the site-odd input from the parity generator and the buffer word 2 parity from the word length detector. The combined parity is then established and the generated parity bit (1 or 0) is sent to the parity gates circuit.

The drum word 1 parity bit is a 1 when combined site identity and buffer word 2 count is even; the parity bit is a 0 when the combined count is odd. In this way, the parity of the complete drum word 1 (including the parity bit) is odd. Table 2–3 shows the possible combinations of site identity and buffer word data count, the combined data count, and the resulting drum word 1 parity bit generated.

The first condition shown in the table is buffer word 2 count odd and site identity count odd. If this situation exists, OR 1 will pass an up level from the site identity generator to condition one input to AND 1, as shown in figure 2–35. The −30V level buffer-word-2-parity input is inverted by I 2 to condition the other input to AND 1. The resulting up-level output of AND 1 is passed by OR 3 to the parity gates circuit to cause a 1 parity bit to be written on the drum. In the second condition shown (site even, buffer word 2 even), the 0 input from the site identity generator is inverted by I 1

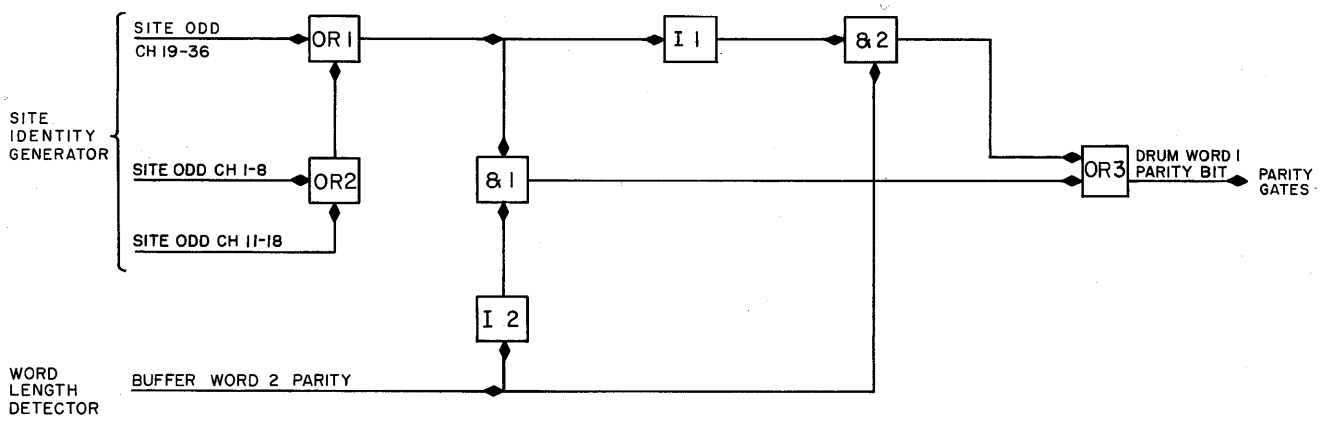


Figure 2–35. Drum Word 1 Parity Generator, Simplified Logic Diagram

to condition one input to AND 2, and the up level on the buffer word 2 parity input conditions the second input to AND 2. OR 3 passes the up-level output of AND 2 to cause a parity 1 bit to be sent to the drums by the parity gates circuit. The third and fourth conditions shown will cause a 0 parity bit to be generated since neither AND 1 nor AND 2 will be conditioned.

The parity bits produced in the drum word 1 parity generator are synchronized with the readout of the rest of the drum word. The output of OR 3 is a 0 when drum words are not being formed, since all inputs to the circuit are 0's and neither AND 1 nor AND 2 will have a +10V output.

TABLE 2–3. DRUM WORD 1 PARITY GENERATION

BUFFER WORD DATA COUNT	SITE IDENTITY DATA COUNT	COMBINED DATA COUNT	DRUM WORD 1 PARITY BIT
ODD	ODD	EVEN	1
EVEN	EVEN	EVEN	1
ODD	EVEN	ODD	0
EVEN	ODD	ODD	0

5.8 DRUM WORD 2 PARITY GENERATOR

The drum word 2 parity generator circuit (fig. 2–36) generates the parity bit for drum word 2. Drum word 2 is made up of message word 1, clock time, and the drum word 2 parity bit. The drum word 2 parity bit is added to give an overall odd count of 1 bits in the drum word. The parity bit is a 1 if the combined number of 1 bits in clock time and in message word 1 (buffer word 1) is even; the parity bit is a 0 if the combined number of 1 bits in clock time and in message word 1 is odd. In this way, the total number of 1 bits in a drum word is odd.

The drum word 2 parity generator receives indications of the number of 1 bits being transferred to the drum by the clock circuit and by buffer word 1. The odd-even count of 1 bits in clock time is indicated by a +10V level on one of the two parity inputs from the clock. The number of 1 bits in buffer word 1 is indicated on the buffer word 1 parity input lines. The correct word 1 parity, as checked by the parity checking circuit (3.4) is odd. However, this includes the busy bit which is not read out of the word 1 buffer. Therefore, if the number of 1 data bits to be transferred to the drums is even, the parity bit is 0; if the number of 1 data bits to be transferred by buffer word 1 is odd, the parity bit is a 1. This condition is reflected on the buffer word 1 parity line by a −30V level for an even number of 1 bits and a +10V level for an odd number of 1 data bits. Table 2–4 shows the possible combinations of odd and even 1 bits in clock time and in buffer word 1, the resulting odd-even count, and the parity bit generated for drum word 2.

With an even number of 1 bits in both clock time and buffer word 1, the combined number of 1 bits is even, and a 1 parity bit is generated. AND 2 is conditioned by a clock-+-on-even level from the clock circuit. The −30V level from OR 1 causes the inverter to condition the second input to AND 2. The resulting +10V level from AND 2 is sent via OR 2 to the parity gates circuit to generate a 1 as the drum word 2 parity bit. With an odd number of 1 data bits for transfer by both the clock and buffer word 1, the combined odd-even count is even, and a 1 bit is generated to form the parity bit. If this situation exists, AND 1 is conditioned by a +10V clock-+-on-odd level and by a +10V level applied through OR 1. The resulting +10V output of AND 1 is sent by OR 2 to the parity gate circuit. The combination of clock-odd and buffer-word-1-even, or clock-even and buffer-word-1-odd causes a 0 parity bit to be generated since neither AND 1 nor AND 2 will have a +10V output under these conditions.

TABLE 2–4. DRUM WORD 2 PARITY GENERATION

BUFFER WORD 1 DATA COUNT	CLOCK TIME DATA COUNT	COMBINED DATA COUNT	PARITY BIT GENERATED
EVEN	EVEN	EVEN	1
ODD	ODD	EVEN	1
EVEN	ODD	ODD	0
ODD	EVEN	ODD	0

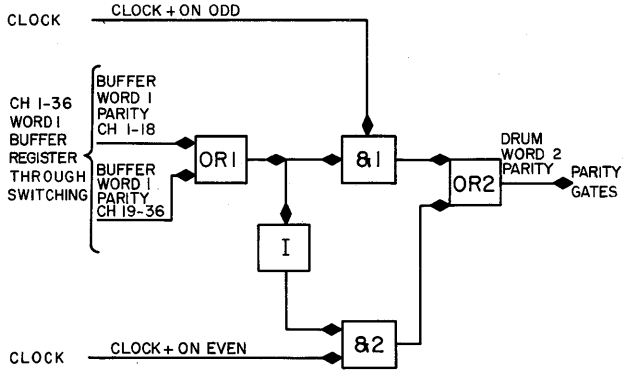


Figure 2–36. Drum Word 2 Parity Generator, Simplified Logic Diagram

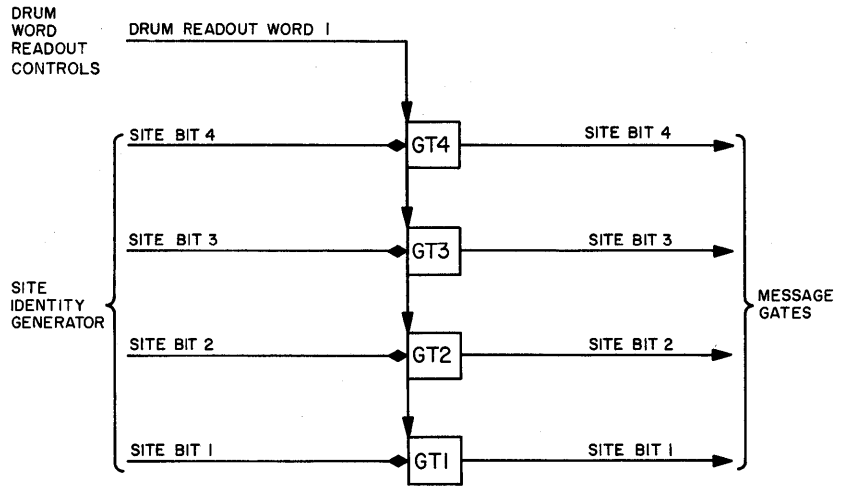


Figure 2–37. Site Gates, Simplified Logic Diagram

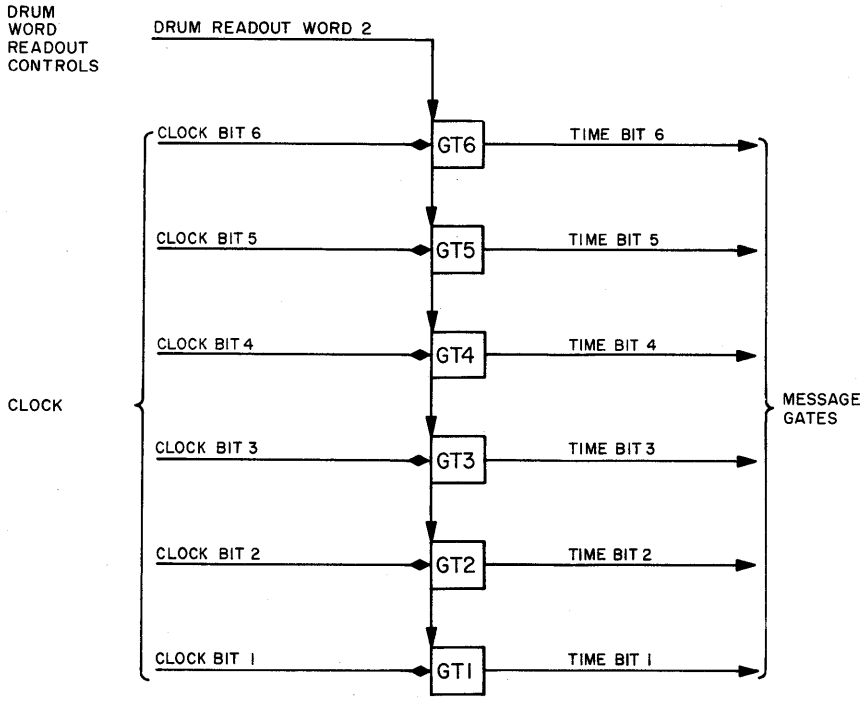


Figure 2–38. Time Gates, Simplified Logic Diagram

5.9 SITE GATES

The site gates circuit (fig. 2–37) converts the four site levels generated by the site identity generator into standard pulses which are synchronized with the read-out of the first drum word.

The four levels from the site identity generator are site bits 1, 2, 3, and 4 and are standard levels (+10V for 1 bits, −30V for 0 bits), indicating the binary site number. Site bit levels 1, 2, 3, and 4 are applied to GT's 1, 2, 3, and 4, respectively. The four gates are simultaneously strobed by the read-out-drum-word-1 pulse (OD 1+1), from the drum-word readout controls circuits. The output of each gate is therefore a single OD 1+1 pulse when the site level applied to the gate is a 1 (+10V). The 0 site levels applied to a gate de-condition the gate, and no output is produced. The outputs of the four gates form a binary site number with the 1 bits being a standard OD 1+1 pulse and the 0 bits being no output. These four outputs, designated site bits 1, 2, 3, and 4, are sent to the message gate where

the 1 bits (OD 1+1 pulse) are amplified and sent to the Drum System. The Drum System then writes a 1 into the proper drum position for each site bit. Since the OD 1+1 site bits are present only during readout of drum word 1, the site identity is written into the first drum word. The site identity occupies the R12 through R15 positions of drum word 1.

Zero bits for site identity (and all other data) are indicated by a lack of 1 bits. Therefore, it is necessary to insert only the 1 bits into the proper drum position to write the complete site identity number since the 0 bits of site identity are indicated by the absence of 1 bits.

5.10. TIME GATES

The time gates (fig. 2–38) convert the standard level outputs of the clock into standard pulses (OD 1+1), during readout of drum word 2.

The six clock outputs, designated clock bits 1 through 6, are applied to GT's 1 through 6, respectively. The six outputs of the clock circuit offer a binary representation of the number of quarter-seconds that have elapsed since the last clock synchronizing pulse from the Central Computer.

The six gates are either conditioned or not conditioned by the clock output; that is each clock bit that is a 1 conditions its gate while 0 clock outputs do not condition their gates. The six gates are strobed by the readout-drum-word-2 pulse (OD 1+1) when drum word 2 is formed. Each gate conditioned by a 1 clock bit passes the OD 1+1 pulse at this time. The six outputs of the circuit (designated time bits 1 through 6) during the formation of the second drum word make up the binary clock time at this instant. The 1 bits of clock time are indicated by the OD 1+1 pulse; the 0 bits are indicated by the absence of the OD 1+1 pulse. The outputs of the time gates are sent to the message gates circuit where the 1 bits are amplified and sent to the Drum System as time data to be included in drum word 2. The six time bits are inserted into the R1 through R6 positions of drum word 2.

The time gates have an output only when the second drum word is formed, since the gates are strobed by the drum-word-2-readout pulse. Clock time inserted into drum word 2 will be the binary count of the clock circuit when drum word 2 is formed.

5.11 PARITY GATES

The parity gates circuit (fig. 2–39) receives the parity bits for drum words 1 and 2 from the drum word 1 parity generator circuit and drum word 2 parity generator circuit, respectively. The parity bits received from the two circuits are standard levels. These two levels condition gates (for 1 parity bits) which are strobed by standard pulses synchronized with the formation of the individual drum words.

The parity bit of drum word 1, as determined by the drum word 1 parity generator, is applied to GT 1. Gate 1 is strobed by the drum-word-1-readout pulse from the drum-word readout controls circuit. When the drum word 1 parity output of the drum word 1 parity generator is up (+10V), the drum-word-1-readout pulse (an OD 1+1 pulse) is passed by GT 1, through the OR circuit, to a pulse amplifier (PA), causing a 1 to be inserted into the parity position of drum word 1. When the input to GT 1 is down, the OD 1+1 pulse is not passed, causing a 0 to be inserted into the parity position of drum word 1.

The drum word 2 parity bit is determined by the drum word 2 parity generator and is applied to GT 2. Gate 2 passes the drum-word-2-readout pulse if the gate is conditioned by the drum word 2 parity bit. The standard pulse is then passed through the OR and PA, causing a 1 to be inserted into the parity position of drum word 2.

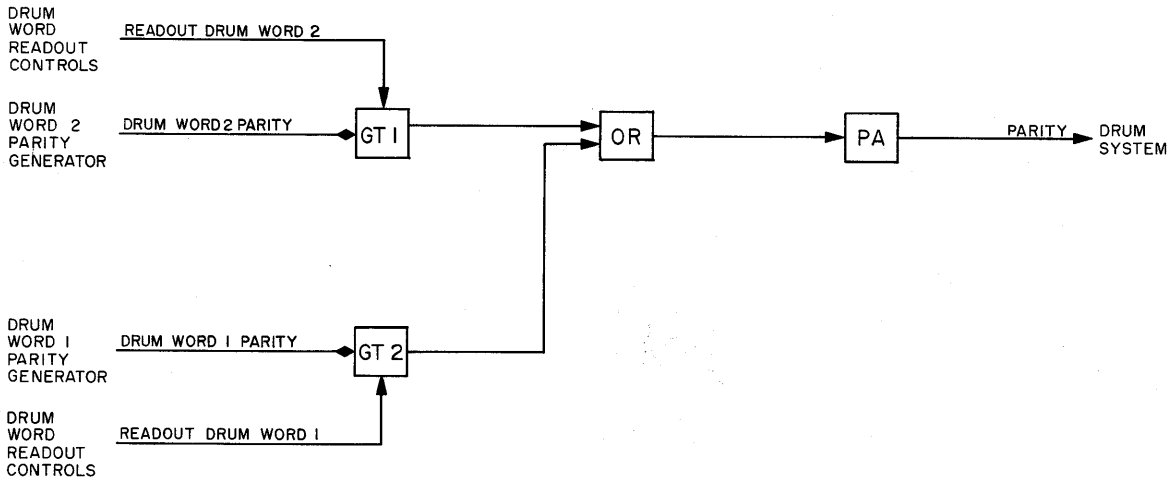


Figure 2–39. Parity Gates, Simplified Logic Diagram

5.12 MESSAGE READOUT GATES

The function of the message readout gates (fig. 2–40.) is to convert the output of the buffer registers into standard pulses for transfer to the Drum System and to the LRI monitor. The formation of the L1 output is shown in detail. The following discussion of the L1 bit is true for the remaining drum bits. The L1 inputs are L1 channels 1-10, 11-18, 19-28, and 29-36. Since only one channel can read out at a time, only one of these lines can present the L1 bits to the message gates circuit. Assume that channel 1 is read out. If the L1 output of buffer word 2 register is a 1, the L1 channel 1-10 input to OR 1 is a nonstandard core output.

This nonstandard output is applied to a level setter through OR 1 and is converted to a standard level (+10V) which conditions GT 1. The first drum-word-readout pulse then strobes GT 1 and is passed to OR 3 and OR 4. The output of OR 3 and OR 4 (a standard pulse) is then amplified by PA's 1 and 2. The output of PA 1 is a single standard pulse (indicating a 1 bit for L1); the pulse is sent to the monitor. The output of PA 2 (a standard pulse) causes a 1 to be written in the L1 position of drum word 1. Ten μsec later, the L1 output of the word 1 buffer register is applied to OR 1. If this input to OR 1 is a 1 bit, the second drum-word-readout pulse is passed as an L1 drum bit, causing a 1 to be inserted into L1 position in drum word 2. This pulse is also sent to the monitor. Figure 2–41 shows the timing relationship for the formation of a 1 bit. The readout of the bits from the buffer registers is accomplished during the application of the word readout levels to buffer register 2 and buffer register 1. The

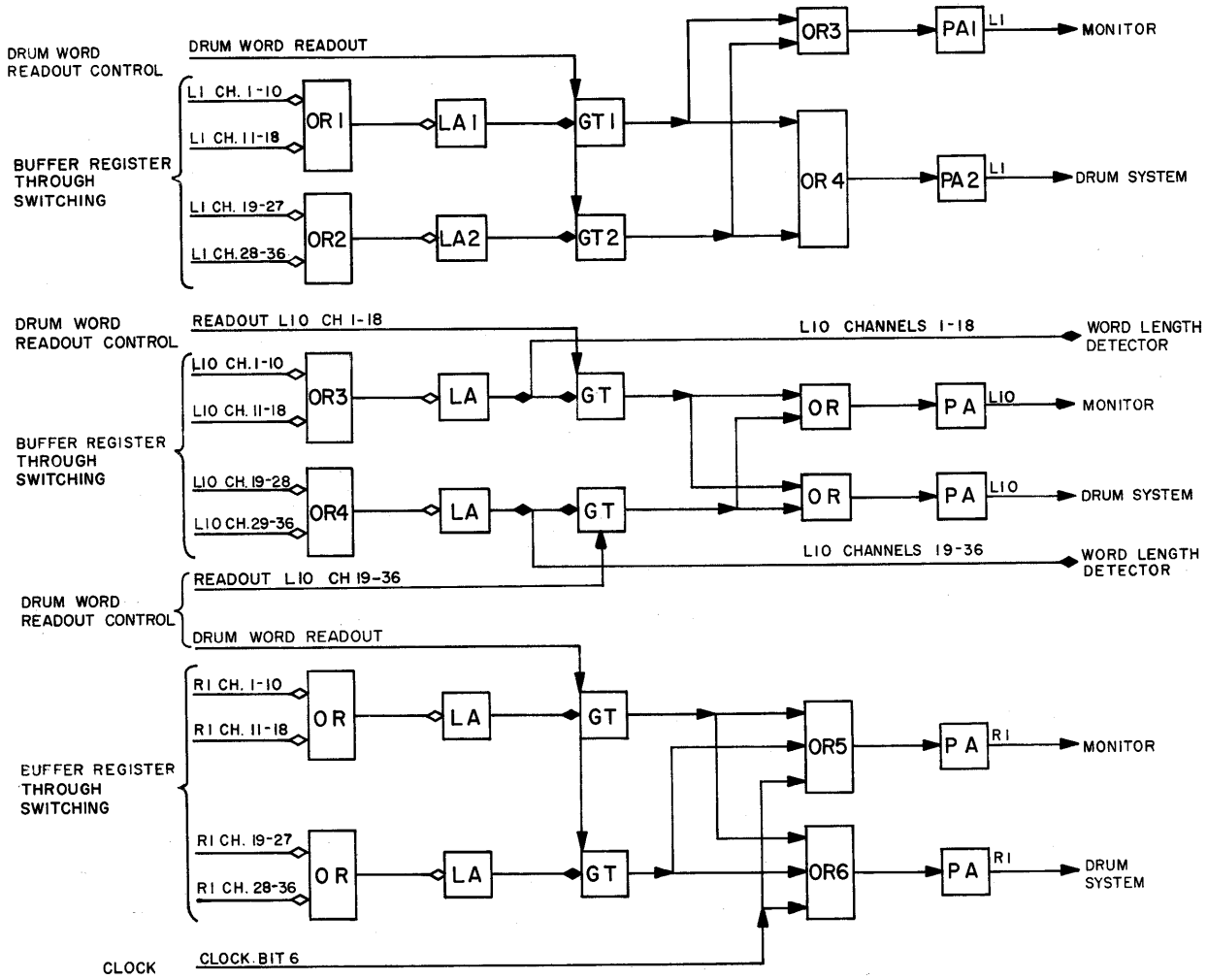


Figure 2–40. Message Gates, Simplified Logic Diagram

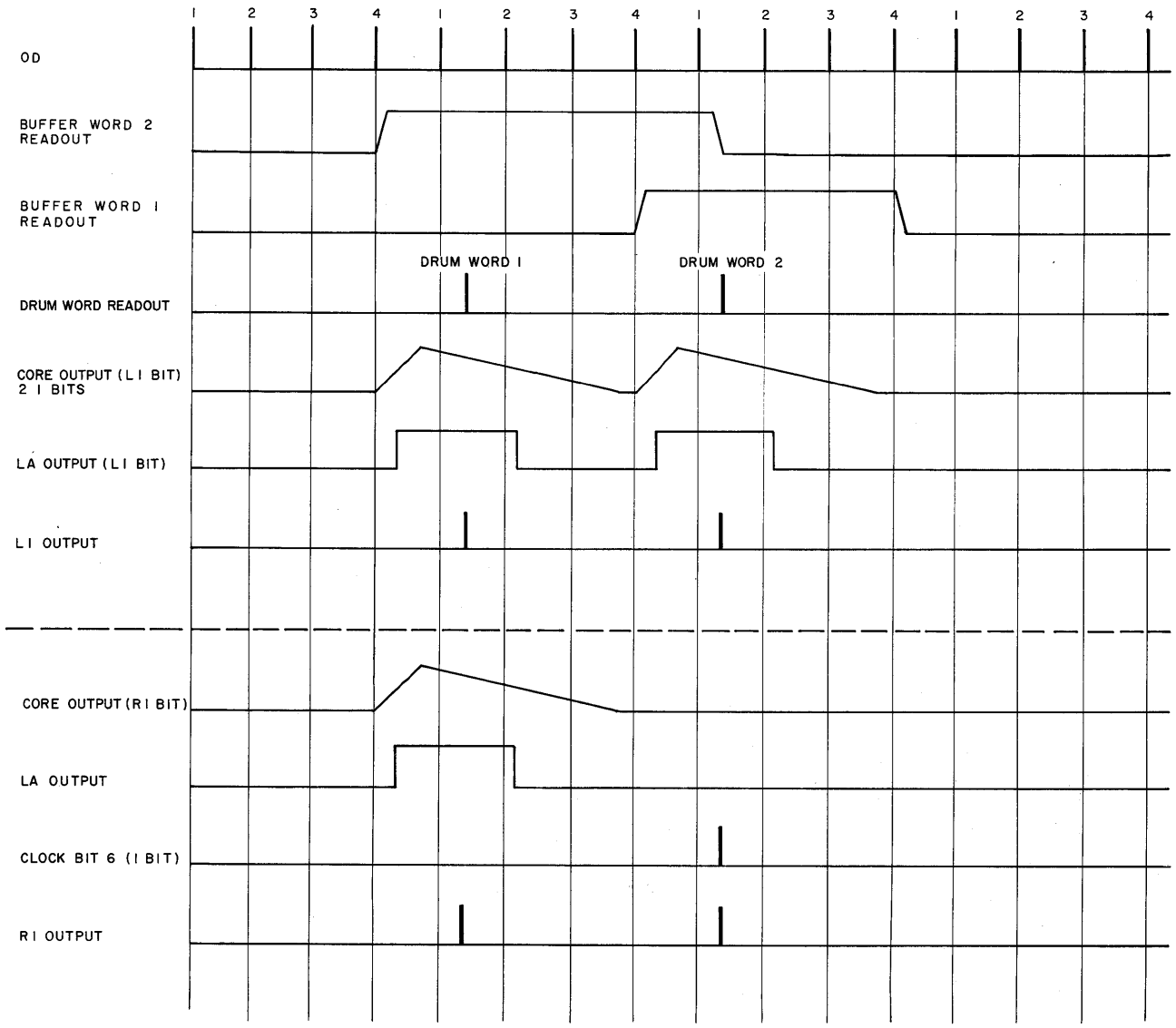


Figure 2–41. Message Gates, Timing Chart

drum word readout pulses strobe the gates and are passed as 1 bits when the related core in the buffer register has an up-level output.

The clock time and site identity data is presented to the drum by applying the output of the time and site gates to the PA (through OR circuits) for the drum bits that receive this data.

The insertion of clock bit 6 (highest order bit of clock time) into the R1 bit position is shown in detail on the logic diagram (fig. 2–40). When the first drum word is formed, the R1 output of buffer word 2 is sent to the Drum System and to the monitor in the same manner as described for the L1 bit. The R1 output of buffer word 2 will appear on one of the input lines (R1, channels 1-10, 11-18, 19-28, 29-36), permitting the first drum-word-readout pulse to pass to the drum and the monitor. During the readout of buffer word 1 (formation of drum word 2), the R1 inputs from the 36 channels are all 0's since there is no R1 output from the word 2 buffer. At OD 1+1 (drum-word-2-readout pulse), clock bit 6 is passed through OR 5 and OR 6 to the Drum System and the monitor. In the same manner, the remaining clock bits are inserted into the R2-R6 positions of the second drum word. The site identity bits from the site gates are similarly inserted into the R12-R15 positions of drum word 1. The site bits are presented as an OD 1+1 drum-word-1-readout pulse for 1 bits. The R12-R15 inputs from the channel during formation of drum word 1 are all 0.

Bit L10 is read out in a similar manner; however, the two gates associated with L10 are strobed on in-

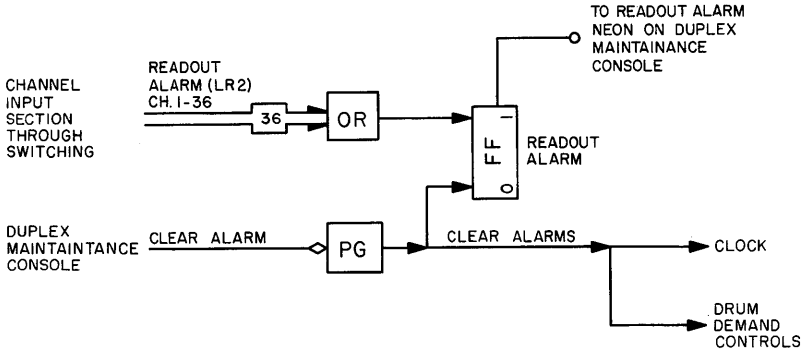


Figure 2–42. Readout Alarm, Simplified Logic Diagram

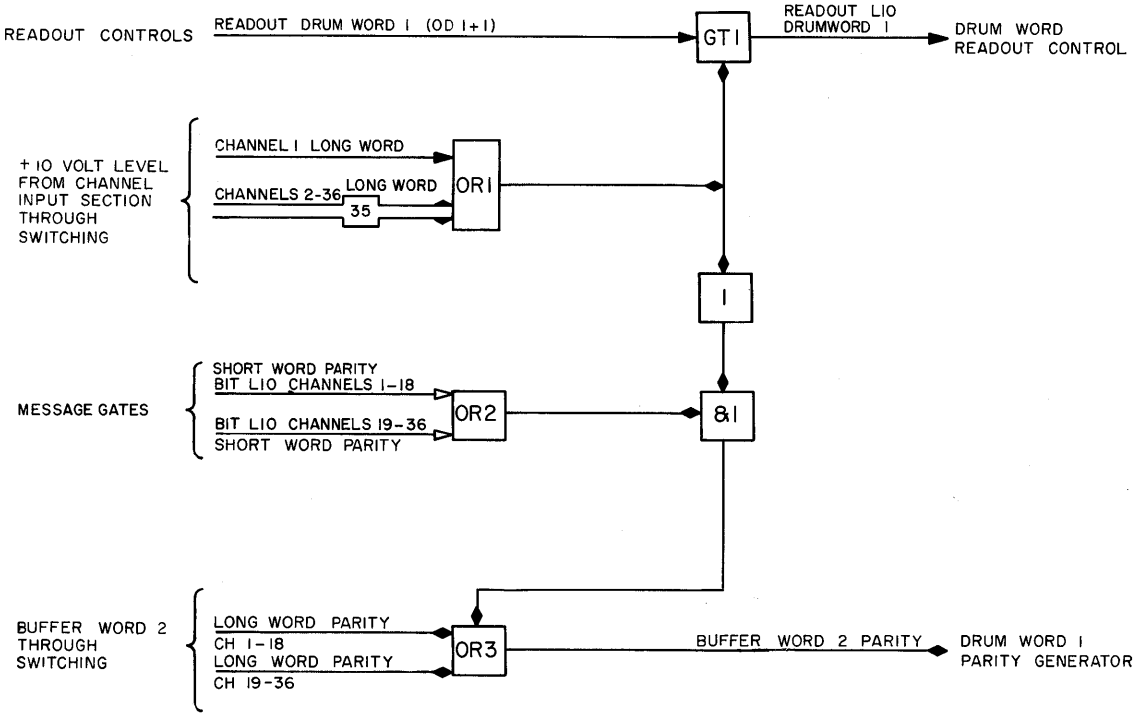


Figure 2–43. Word-Length Detector, Simplified Logic Diagram

dividual lines. Because of message format revision, the outputs of the L10 level setters which are sent to the word length detector do not have a function.

5.13 READOUT ALARM

The readout alarm circuit (fig. 2–42), generates a visual alarm on the duplex maintenance console when any of the LRI channel sections has generated a readout alarm pulse. The readout-alarm pulse indicates that an incoming message cannot be placed in the buffer registers because a previous message is still contained in the buffer registers awaiting transfer to the Drum System. The incoming message is then destroyed in the primary registers.

The readout alarm circuit receives the readout-alarm pulses from all 36 channel sections. These 36 outputs are combined into a single-channel 1-36 readout alarm input. The combined input is applied to the set input of the readout alarm flip-flop. When any of the 36 channels generates a readout-alarm pulse, the flip-flop is set, lighting a neon on the duplex maintenance console. The flip-flop remains set until a clear alarms level from the duplex maintenance console is applied to the pulse generator by depressing a CLEAR ALARMS switch. The pulse generator then produces a standard pulse which clears the flip-flop, turning off the neon. The clear-alarm pulses are also used to reset the clock alarm flip-flop in the clock circuit and the display counter alarm flip-flop in the drum demand control circuit.

5.14 WORD-LENGTH DETECTOR CIRCUIT

The word-length detector circuit (figure 2–43) was designed to detect a variable length in message word 2. However, a message word format change established a fixed word length for message word 2. The word length detector circuit now functions only to relay the buffer word 2 parity bit to the drum word 1 parity generator and to forward the readout-drum-word-1 (as the readout L10 drum word 1) pulse to the drum word readout control circuit.

A +10V level from the channel input section is passed by OR 1 to GT 1 and to the inverter. Consequently, the level input to GT 1 is a constant +10V and the input to AND 1 from the inverter is a constant −30V. Gate 1 passes a readout-drum-word-1 pulse (when received) as a readout-L10-drum-word-1 pulse to the drum word readout control circuit. AND 1 is constantly deconditioned by the inverter and does not pass any signals. OR 3 receives the parity bit (designated as the long-word-parity channels 1-18 and 19-36 level), and forwards the signal to the drum word 1 parity generator as the buffer word 2 parity bit. The drum word 1 parity generator utilizes the buffer word 2 parity bit to establish the overall parity bit for drum word 1.

PART 3

LONG-RANGE RADAR INPUT MONITOR C-2021/FSQ

CHAPTER 1

INTRODUCTION

1.1 SCOPE OF PART

This part contains the theory of operation of Long-Range Radar Input Monitor C-2021/FSQ (fig. 3–1), commonly called the LRI monitor. Chapter 1 presents general information on the equipment, such as physical and functional descriptions, system theory, etc. Also discussed in this chapter is the mathematical basis of the operation of the equipment. Subsequent chapters are devoted to a detailed theory of operation.

1.2 PURPOSE OF EQUIPMENT

The LRI monitor provides a visual means of checking the quality of LRI data after it has been processed by the Input System, but before it is made available to the Central Computer. It thus enables operational personnel to make preliminary analysis, independently of the Central Computer, of the air situation as seen by long-range radar. In addition, it permits maintenance personnel to evaluate the operational efficiency of the Input System, assisting in general localization of troubles. Specifically, the LRI monitor may be used to perform the following functions:

a. Assist in comparison of LRI data before and after processing by the computer.
b. Provide coverage of data source by showing raw data and display of clutter.
c. Check LRI channel equipment during initial installation, and subsequently.
d. Take photographic records of LRI data before it has been processed by the Central Computer.

To perform these functions, four display consoles are provided:

a. ASO unit 623, located in the air surveillance area and utilized by the air surveillance officer.
b. Unit 622, located in the maintenance area and utilized by maintenance personnel.
c. MSP unit 620, located in the mapper survey position and controlled by the mapper supervisor.
d. Camera unit 621, also controlled by the mapper supervisor and equipped with a camera to record the displays which he selects.

1.3 PHYSICAL DESCRIPTION

The LRI monitor consists of the four display consoles referred to, above, and unit 93, the LRI monitor control unit. Associated with the monitor for control purposes is the auxiliary control console unit 947 (part of the Display System). Information is selected for display by means of pushbutton keyboards at the consoles or at unit 947 and is then presented by the cathode-ray tube (CRT) in each console. Unit 93 contains the circuitry which serves all four consoles. The general features and controls of the consoles are described below, followed by a description of unit 93.

1.3.1 Display Consoles

1.3.1.1 General Features

Each display console contains a 16-inch CRT on which a plan-position indication (PPI) type of display is produced. Also found in all consoles are the following:

a. A UNIT STATUS switch which determines the power status of the console and which may be used to connect the console to either the active or standby duplex machine (1.4.4).
b. A high-voltage power supply which provides the necessary CRT high voltages.
c. Two pluggable interchangeable deflection amplifiers to position the display.

1.3.1.2 Units 622 and 623

The 622 and 623 display consoles are identical. At each, messages are selected for display by means of SITE and MESSAGE selection controls mounted in two 15-button interlocked-release pushbutton banks, one bank on each side of the CRT.

1.3.1.3 Unit 620

Unit 620 differs from units 622 and 623 in that the message selection controls for this console are remoted to auxiliary control console unit 947.

1.3.1.4 Unit 621

Unit 621 is camera-equipped; in other respects, it is similar to unit 620. Message selection controls and the basic camera controls and indicators are remoted to auxiliary control unit 947. The camera is mounted in such a way as to permit simultaneous photography of

Figure 3–1. LRI Monitor Equipment

the face of the CRT (with minimum distortion) and visual inspection of the display. Included in the camera field are indicators to identify the site identity, message label selection, and film exposure-time selections made at unit 947. These selections thus become part of the photographic record. The clock time of the display is also shown.

1.3.2 Unit 93

The LRI monitor control unit, unit 93 in systems 17 (DC-12) and beyond, differs somewhat from that in systems 1 through 16. In all systems, this unit is duplexed. In systems 1 through 16, each half of the unit consists of four modules, A, B, C, and Z. Modules A and B mount 13 types of pluggable units. These units contain the digital circuitry described generally in 1.6 and in detail in Chapter 2. Module C mounts six double-size pluggable units, six conventional single-size pluggable units, and one test panel. The pluggable units contain the analog circuitry described generally in 1.6 and in detail in Chapter 3. The Z module provides the usual power distribution and overload protection facilities. An interlock system in the C module prevents d-c power from being brought up to the unit 93 frame if a pluggable unit is removed from the frame or is improperly seated.

In systems 17 and beyond, each half of unit 93 consists of three modules, B, C, and Z. Digital circuitry is contained in one module, module B; otherwise, the units are the same. The reduction in the number of pluggable units devoted to digital circuitry is made possible by design refinements permitting the elimination of many power amplifiers, cathode followers, and similar nonlogic circuits.

1.4 SYSTEM THEORY OF OPERATION

1.4.1 Position of LRI Monitor in AN/FSQ-7 Combat Direction Central

The position of the LRI monitor in the Input System of AN/FSQ-7 Central is seen in figure 3–2. The monitor selects, for display, outputs of the LRI common equipment on the way to the Drum System. These outputs are described in 1.4.2. Operation of the LRI monitor is synchronized with that of the LRI element by means of OD, drum demand (DD), and other pulses fed to or from the LRI common equipment and the LRI monitor. These pulses are discussed in 1.4.3. The LRI common equipment is duplexed and the LRI monitor may be associated with the A or B equipment and thus with the active or standby machine. Duplexing is discussed in 1.4.4.

1.4.2 Composition of LRI Message

Digital messages containing target data and related information are serially transmitted over land lines from the radar sites to the LRI element. The LRI element processes these messages, adding clock time, site identity, and parity bits; it then transfers them in the form of two 33-bit words, in parallel readout, to the Drum System. These words are fed to the LRI monitor as well. As shown in figure 3–3, the first word includes five message label bits and four site identity bits. The message label indicates the type of message (fine-

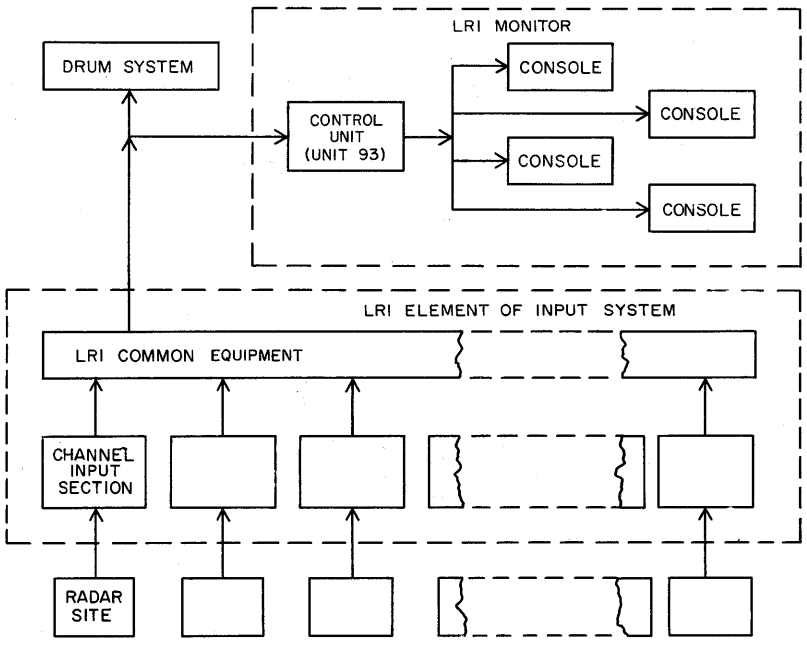


Figure 3–2. Position of LRI Monitor in Input System

grain data (FGD), Mark X IFF, or height-finder) being transmitted from the site. All message labels in use are binary representations of odd numbers (the least significant bit is a control bit and is always a "1"). By designating the site number in binary, the site identity bits identify the radar site at which the message originated. The second word provides the range and azimuth data which the target indication on the CRT will represent. Ten bits are available in this word to express range information, permitting a 1,024-unit scale. Twelve bits are available to express azimuth information, permitting a 4,096-unit scale. Messages are selected for displays on the basis of the site identity and message label data in the first word; then, the information in the second word is visually presented.

1.4.3 Synchronization with LRI Element

Operation of the LRI monitor is synchronized with the transmission of LRI data by means of pulses presented to the monitor by the LRI element. Certain of these pulses are generated in the Drum System and fed through the LRI common equipment. These include the OD pulses: four standard sync pulses generated 2.5 μsec apart in a continuously repeated sequence.

Specifically, the following synchronizing pulses are fed to the LRI monitor.

a. OD 2.
b. OD 3.
c. Drum demand (DD), furnished by the Drum System in synchronism with OD 3, indicates that a drum slot is available to accept a message.
d. Data available (DA), furnished by the LRI common equipment in synchronism with OD 1 delayed, indicates that a message word is being transferred.

When the LRI monitor has selected a message for display, it sends a display-started pulse back to the LRI common equipment, signifying that the message is to be displayed. The transfer of future LRI messages to the drums is blocked until the message display is completed. A display-ended pulse, returned to the LRI element after conclusion of a display, confirms the fact that display is completed.

1.4.4 Duplexing

In the LRI monitor, the control unit, unit 93, is duplexed; unit 93A is associated with the A computer; Unit 93B with the B computer. The four consoles are simplexed; each may be connected to either half of unit 93, and thus to either Direction Central computer, by means of the console UNIT STATUS switch. The ACTIVE position of the switch connects the console to the half of unit 93 associated with the active-designated computer; the STANDBY position of the switch connects the console to the half of unit 93 associated with the standby-designated computer. If the A and B computers change status, the consoles are automatically reconnected to the half of unit 93, active or standby, designated by the position of the console UNIT STATUS switch.

Duplex-simplex relationships in the LRI monitor and associated units are shown in figure 3–4. Lines are provided to each console to indicate the status of each duplex machine and of each simplex power supply. Personnel are thus aware of the operational position in the AN/FSQ-7 system of each monitor console.

1.5 MATHEMATICAL BASIS OF THEORY OF OPERATION

1.5.1 General

To prepare digital target data for display, the LRI monitor must, in effect, perform certain mathematical operations upon it. A prior understanding of these mathematical operations will make it easier to grasp the theory of operation of the equipment. Accordingly, the mathematical basis of data-processing in the LRI monitor is discussed in 1.5.2.

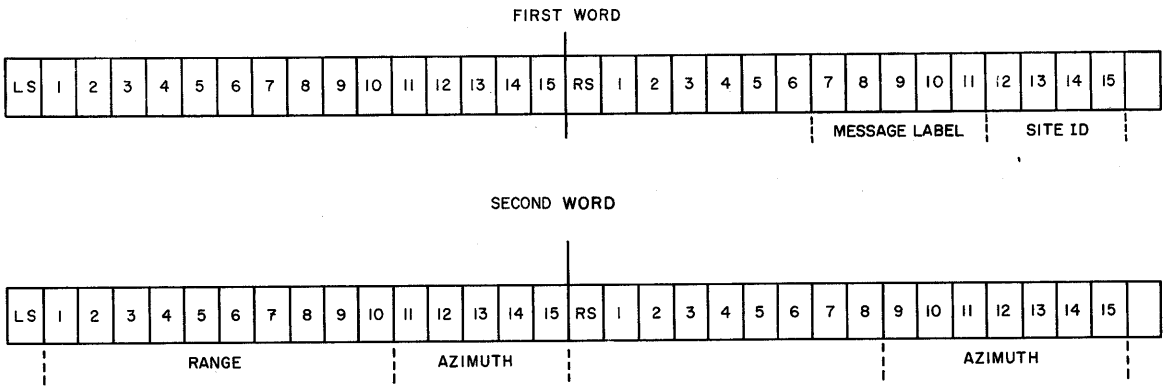


Figure 3–3. Composition of LRI Message to LRI Monitor

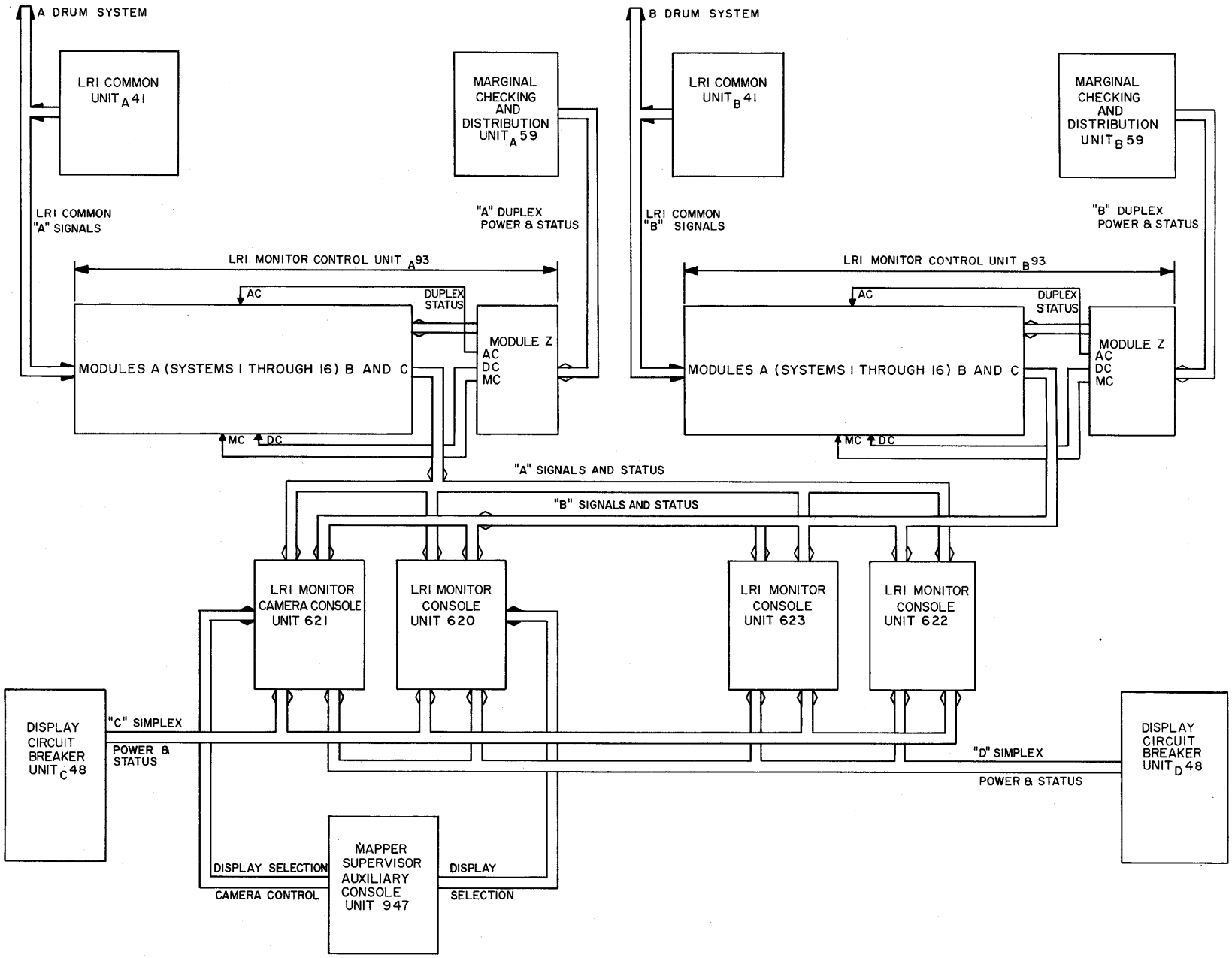


Figure 3—4. Relationship of LRI Monitor to Associated Equipment

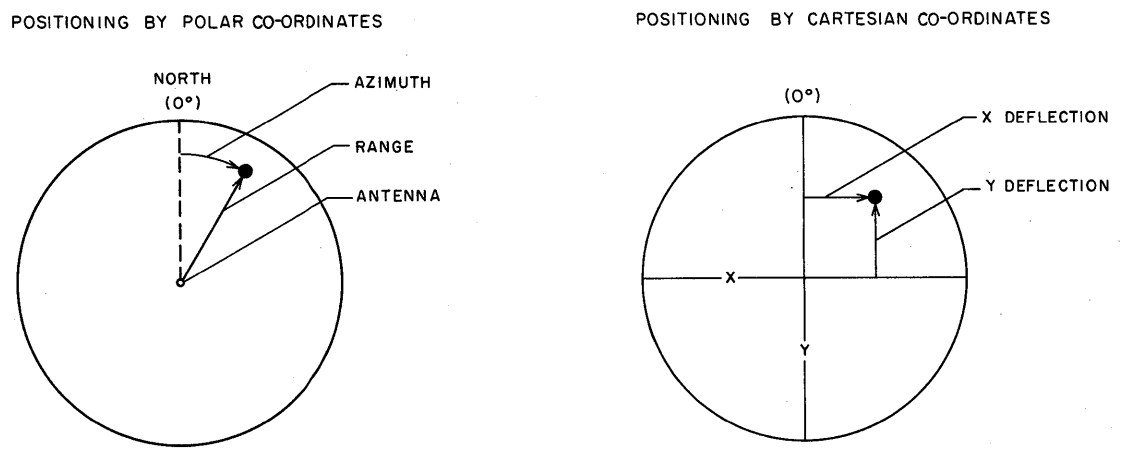


Figure 3–5. Target Positioning by Polar and Cartesian Co-ordinates

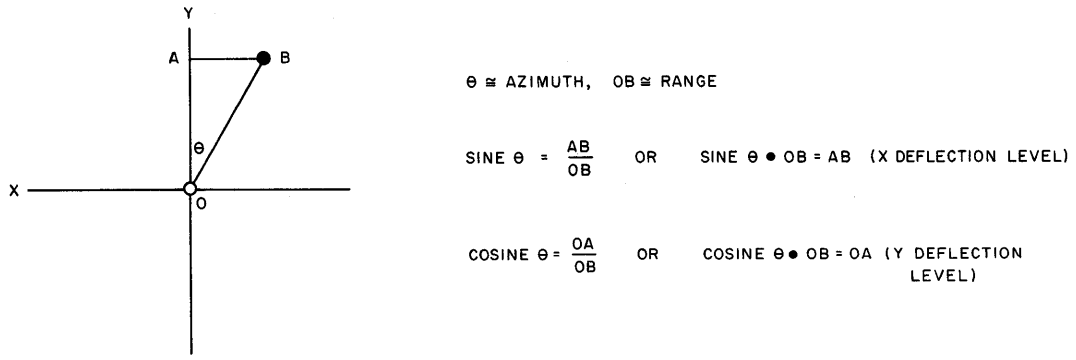


Figure 3–6. Mathematical Basis for Development of Deflection Levels

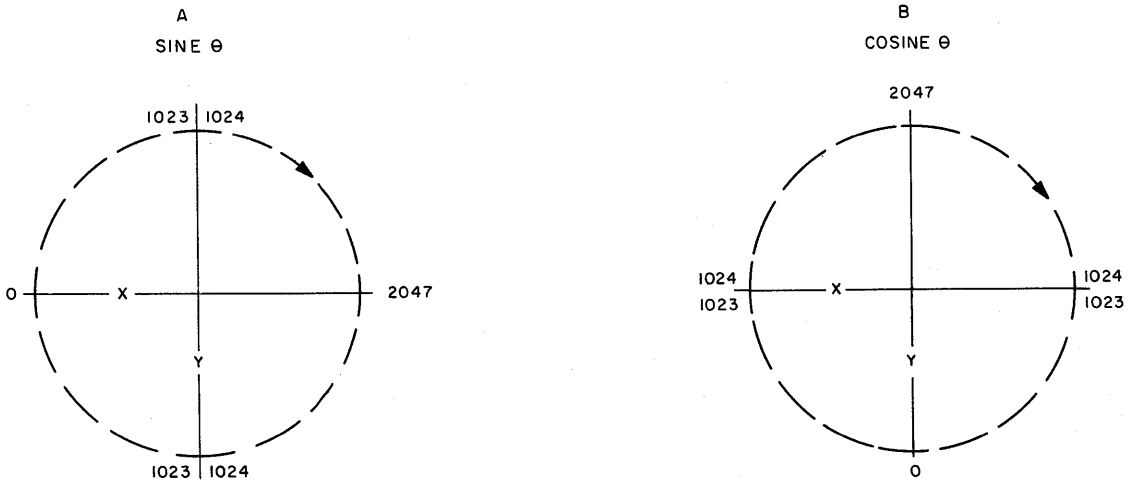


Figure 3–7. Digital Equivalents of Approximations of Sine θ and Cosine θ

1.5.2 Generation of PPI Display

A PPI display presents a map of the area being surveyed by a radar installation with the antenna occupying the center of the screen. Targets appear as points in the display geographically referenced to the antenna.

The position of an LRI target is described by digital information in the LRI message. This information is in polar co-ordinate form, specifying the azimuth and range of the target. However, the display circuitry of the LRI monitor positions a target by means of its cartesian co-ordinates; that is, with respect to the X and Y axis of the display screen. Figure 3–5 compares the two methods of target location. Accordingly, the LRI monitor must develop, from the original polar information, two voltage (actually current) levels representing the X-Y co-ordinates of the target to drive the horizontal (X) and vertical (Y) deflection coils of the CRT.

1.5.3 Determination of Deflection Values

One approach to this problem is suggested by figure 3–6. Here θ represents the known azimuth, and OB the known range; the problem is to find AB (X deflection) and OA (Y deflection).

By definition $\text{Sine } \theta = \frac{AB}{OB}$

Therefore, AB = (Sine θ) OB

Since OB is known, the problem may be solved by finding sine θ and multiplying it and OB.

Similarly, cosine $\theta = \frac{OA}{OB}$; or OA = (cosine θ) OB, and OA is found by deriving cosine θ and multiplying it and OB.

This approach, in an electronic form, is actually used in the LRI monitor. The sine value and the cosine value of the azimuth are electronically derived in a manner described below and multiplied with the range value to produce the X and Y deflection levels.

1.5.4 Sine and Cosine Approximation

The electronic derivations of azimuth sine and cosine values are very similar; the derivation of the sine value is discussed in detail below.

In the LRI message, azimuth is expressed on a linear 0-4095 binary scale, representing a clockwise progression from north-azimuth to 360 degrees. Thus, 1,024 represents 90 degrees and 3,072 represents 270 degrees. The sine value of the changing azimuth varies in a quite different way, however. As the azimuth progresses from 0 to 90 degrees, the sine value of the azimuth increases toward +1; then the value returns to 0 as the azimuth progresses toward 180 degrees; it continues toward −1 as the azimuth continues its progression toward 270 degrees; and it returns again to 0 as the azimuth reaches 360 (or 0) degrees. The pictorial representation of this variation in sine values is, of course, the classic sine wave, in which the positive-going zero-crossing represents 0 (or 360) degrees, the positive peak of the sine wave, 90 degrees, the negative-going zero-crossing, 180 degrees, and the negative peak 270 degrees. Thus, the problem is to be able to derive electronically a series of values which plot a sine wave from a series of values which lie on a straight line.

In the LRI monitor, the problem is solved in two stages. First, approximations of the sine and cosine values are electronically derived from the azimuth value. These approximations are expressed on a 0-2047 binary scale as shown in figure 3–7, A (sine value) and 3–7, B (cosine value) and summarized below.

SINE APPROXIMATION

AZIMUTH (degrees)	SINE VALUE	BINARY EQUIVALENT
0	0	1023
90	+1	2047
180	0	1023
270	−1	0

COSINE APPROXIMATION

AZIMUTH (degrees)	COSINE VALUE	BINARY EQUIVALENT
0	+1	2047
90	0	1023
180	−1	0
270	0	1023

If the binary equivalents for the sines or cosines of intermediate azimuths were plotted as well, the result would be triangularly shaped curves, crudely approximating a sine wave. The next stage in obtaining sine and cosine approximation is to convert these binary values to analog voltage levels and to process these levels in such a way that the voltages developed by a plot of the entire 0-360-degree range of azimuth inputs will closely resemble a sine wave.

1.5.5 Target Presentation

Assume now that a particular target described in the LRI message is to be presented. From the digital azimuth information in the message, two analog voltage levels are developed (as described above in 1.5.4), representing the sine and cosine respectively of the azimuth. From the digital range information in the message, an analog level is developed linearly expressing range from 0 miles (antenna). The levels are now processed accord-

ing to the mathematical philosophy discussed in 1.5.3. The sine voltage level is electronically multiplied with the range voltage level to yield a voltage level representing the X deflection of the target (AB in fig. 3–6). This level, applied through a deflection amplifier to the horizontal deflection coil of a CRT, properly positions the target indication with respect to the X axis. In the same way, the cosine voltage level is electronically multiplied with the range voltage level to produce a level representing the Y deflection of the target OA in figure 3–6, and this level is amplified to drive the vertical deflection coil of the CRT.

The circuits performing the operations described above are discussed next.

1.6 GENERAL FUNCTIONAL DESCRIPTION

1.6.1 LRI Monitor Sections

The function of the LRI monitor is to select, process, and display, in a PPI presentation, messages prepared by the LRI element for transfer to the drums. To perform these functions, the LRI monitor utilizes four functional sections: digital; analog; display; and switching. The sections are described briefly below (1.6.2 through 1.6.5) and in detail in Chapters 2 through 5. The relationship between the four sections is illustrated in figure 3–8.

1.6.2 Digital Section

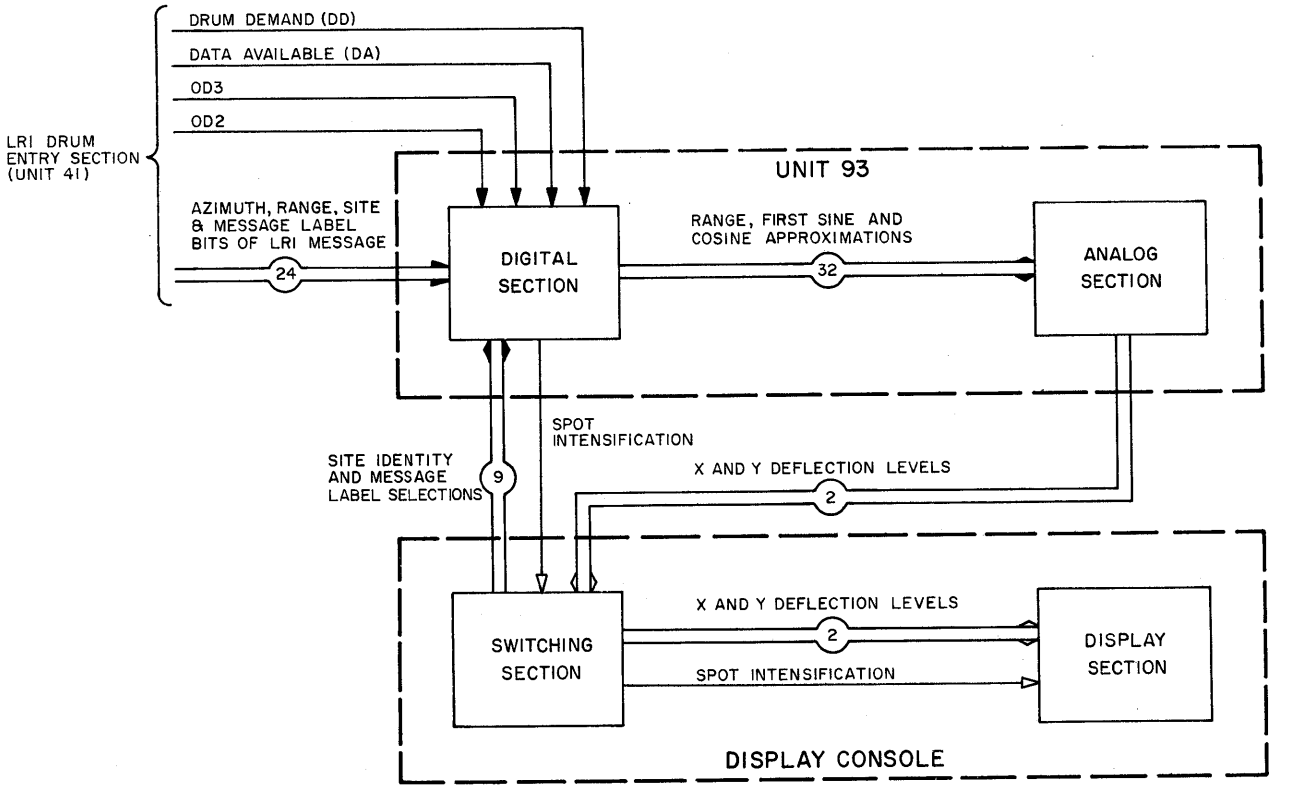
The digital selection performs the following functions:

a. Accepts the LRI message which has been prepared by the LRI element for transfer to the drums.

b. Determines whether the message has been selected for display at one or more of the four consoles.

c. When a message has been selected, transfers the target range and azimuth information in the message to the analog section after initial processing, for PPI presentation, of the azimuth information.

d. Causes inhibition of message-transfer from the LRI element to the drums, during the display of the message on a console.



NOTE:
ONLY ONE OF THE FOUR DISPLAY CONSOLES IS INDICATED. THE SAME SIGNALS ARE FURNISHED TO OR BY THE SWITCHING SECTION CIRCUITS FOR THE OTHER CONSOLES, EXCEPT FOR SPOT INTENSIFICATION; THIS GOES ONLY TO THE CONSOLE(S) WHICH HAVE SELECTED THE MESSAGE

Figure 3–8. LRI Monitor Functional Diagram

To perform these functions the digital section distinguishes the first and second word of the message, stores each word successively in flip-flop registers, and processes each word appropriately. The first word contains the site identity and message label information (1.4.2) which provides the basis for display-selection. Operating or maintenance personnel specify, by means of pushbutton control on the consoles or unit 947, the site identity and message label designations of the message they wish to have displayed. The digital section compares these requests with the site identity and message label information in the first word of the message, and, if a message has been selected for display, transfers the range and azimuth information in the second word to the analog section. Prior to the transfer, azimuth information is processed in the following manner.

First, the quadrant in which the azimuth is located is determined by sensing certain flip-flops in a register containing the azimuth information. Then, flip-flops expressing the azimuth are appropriately complemented to obtain, in digital form, the first approximation of the sine and cosine functions of the azimuth (1.5.4). The resulting digital values, together with the unprocessed range information, are applied to the analog section.

1.6.3 Analog Section

The analog section transforms digital range information and digital approximation of the azimuth sine and cosine into corresponding voltage levels. The sine and cosine voltage levels are further processed by shaping networks into almost pure sine and cosine functions of azimuth (1.5.4). The sine voltage level and range voltage level are then multiplied in an analog multiplier to provide the means (after amplification) for X-positioning of the CRT beam. The cosine and range voltage levels are similiarly multiplied to provide the means for Y-positioning of the beam (1.5.5).

1.6.4 Display Section

The voltage levels generated by the analog section are applied to the display section. This section contains the CRT tubes, one in each console, used to present LRI target information in PPI form. The translation of this target information into analog voltage levels has been explained above. These voltage (actually current) levels cause deflection yokes in all four consoles, if they are in the correct status (active or standby), to be energized, positioning the beam in accordance with the original target range and azimuth information. The beam is then unblanked at the consoles at which, or for which, the message display was requested, causing an appropriate target indication.

1.6.5 Switching Section

The switching section is distributed between the consoles and unit 947. It contains the controls, relays, and associated circuitry required to perform the following functions.

a. Determine the operational status (active, standby) of each console.
b. Specify the site identity and message label designations of messages to be displayed at the consoles.
c. Control the operation of the camera in unit 621.

CHAPTER 2
DIGITAL SECTION

2.1 OVERALL THEORY OF OPERATION

2.1.1 General

Inputs to the digital section of the LRI monitor consist of the LRI messages prepared by the LRI element for transfer to the drums, and system timing and synchronization pulses supplied by or through the LRI element. These inputs, described in Chapter 1, are transferred from the LRI element to the digital section over 24 lines, seven of them time-shared between the first and second words. Eight spare lines are also provided.

Processing of inputs within the digital section consists of three functions: message selection; target-data conversion; and synchronization and timing. These functions are discussed generally below; refer to figure 3–9 during the discussion. Then, the contribution of specific circuits to these functions is described in detail (2.2 through 2.4).

2.1.2 Message Selection

By means of pushbutton keyboards at the LRI monitor consoles, or at unit 947, personnel specify the site identity and message labels of the messages they wish to have displayed. The pushbutton-activated circuits supply sets of voltage levels to the site identity selector and message label selector circuits. There is one site identity selector, one single message label selector, and one multiple message label for each console.

The site identity bits in the first word of the message are accepted by the 4-FF site identity storage register which supplies a corresponding set of voltage levels to all the site identity selectors. Similarly, the five message label bits are accepted by the 5-FF message label storage register, which supplies a corresponding set of voltage levels to all the single-message label selectors and mutiple-message label selectors. In the selectors, comparisons are made between the levels supplied by the console keyboards circuitry and by the storage registers. If, on the basis of this comparison, a message is selected for display at one or more consoles, the display selection and timing circuit is activated. This circuit provides a display-started pulse to the LRI common equipment, receipt of which prevents further transfer of LRI messages to the Drum System. After a delay to allow the CRT deflection coils at all four consoles to be fully energized, the display selection and timing circuit sends a CRT intensification pulse to the display console or consoles for which the display was requested. Following the end of the intensification period, the display selection and timing circuit sends a display-ended pulse to the LRI common which confirms the fact that display has ended and prepares the monitor for the reception of the next pair of words.

2.1.3 Target Data Conversion

The 10 range bits of the second message word are accepted by the 10-FF range storage register which supplies corresponding voltage levels directly to the range decoder in the analog section. The 12 bits of azimuth information in the second word are fed to the 12-FF sine storage register, and the 11 least significant bits are fed to the 11-FF cosine storage register. The FF^{10} and FF^{11} in the sine storage register are sensed by the register corrector to determine the quadrant in which the target azimuth lies. On the basis of this quadrant determination, the register corrector complements selected flip-flops in the sine storage register and may complement the flip-flops in the cosine storage register to provide approximations in digital form of the sine and cosine functions of the azimuth. These approximations are fed as voltage levels to the sine and cosine binary decoders, respectively, in the analog section.

2.1.4 Synchronization and Timing

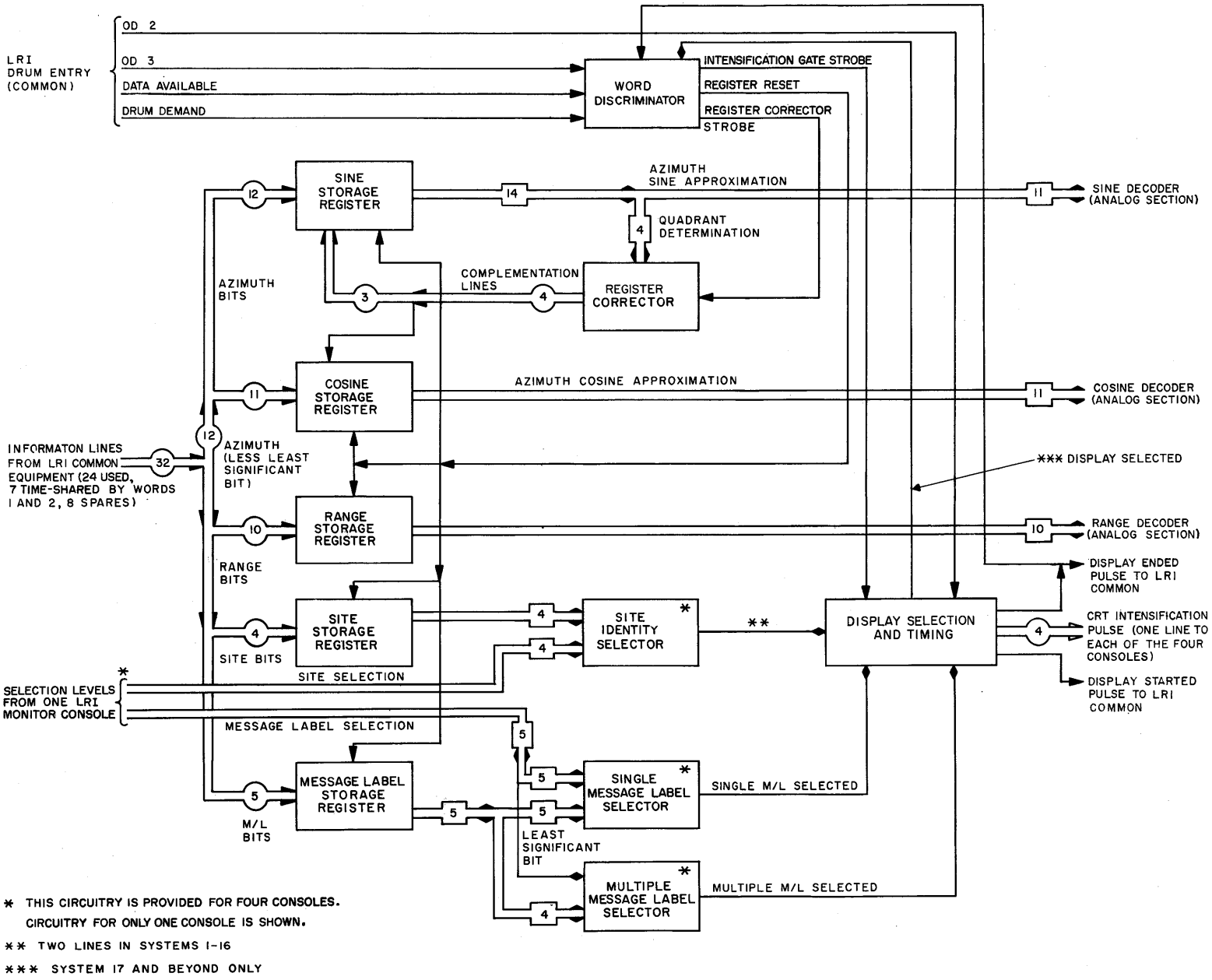
2.1.4.1 General

Synchronization between the LRI monitor and LRI element is performed mainly by the word discriminator. Receiving OD 3, drum-demand, and data-available pulses from the LRI element, the word discriminator distinguishes between the first and second word of the message and produces various strobing pulses which, with OD 2 pulses, regulate the timing cycle of the monitor when a message is displayed.

The timing cycle in systems 1 through 16 differs from the cycle in subsequent systems. The differences will be pointed out in this and other applicable portions of the chapter. The conditions in systems 17 (DC 13) and beyond will be regarded as standard; conditions in the earlier systems, as a variation.

2.1.4.2 Systems 17 and Beyond

The timing cycle (fig. 3–10), that is, the time required to display a single target, requires 280 μsec. The cycle is considered to begin with the arrival of a DD pulse at the word discriminator. This pulse resets all storage registers. At 6 μsec, the LRI element feeds a



* THIS CIRCUITRY IS PROVIDED FOR FOUR CONSOLES. CIRCUITRY FOR ONLY ONE CONSOLE IS SHOWN.

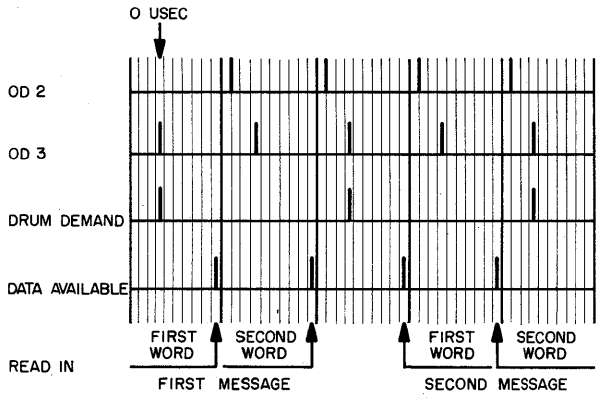
** TWO LINES IN SYSTEMS 1-16

*** SYSTEM 17 AND BEYOND ONLY

Figure 3–9.. LRI Monitor Digital Section, Overall Section Diagram

data-available (DA) pulse to the word discriminator; at the same time, the first word information is installed in the site identity and message label registers. In the next 4 μsec (until 10 μsec) the information in these registers is compared by the site identity and message label selectors with the message selections made at the consoles or unit 947, and a decision is made to display or ignore the information in the second word of the message. At 10 μsec, the word discriminator produces an intensification gate strobe. This pulse is fed to the display selection and timing circuit, activating that circuit if a message has been selected for display. The display selection and timing circuit returns a display-started pulse to the LRI common section, inhibiting further DD pulses and thus suspending transfer of LRI messages to the Drum System. The site identity and message label registers are also cleared at 10 μsec. At 16 μsec, the second word is stored in the range and azimuth storage registers; simultaneously, the register corrector determines the quadrant in which the target azimuth lies. At 20 μsec, the register corrector is activated by the register corrector strobe from the word discriminator, and, on the basis of the previous quadrant determination, the corrector complements selected flip-flops in the sine storage register, and may complement all the flip-flops in the cosine storage register. The approximations of the sine and cosine functions of the azimuth thus produced are immediately available to the analog section.

Meanwhile, at 17.5 μsec, if a message has been selected for display, an OD 2 pulse (regarded as OD 2 pulse No. 1) initiates a counting action in the display selection and timing circuit. At the 24th OD 2 pulse (247.5 μsec), this circuit feeds an intensification level to the console for which a message display was requested. The level is continued until the 26th OD 2 pulse (267.5 μsec). At the next OD 2 pulse (277.5 μsec), a display-ended pulses is fed from the display selection and timing circuit to LRI common, and to the word discriminator, which, in turn, produces a register-



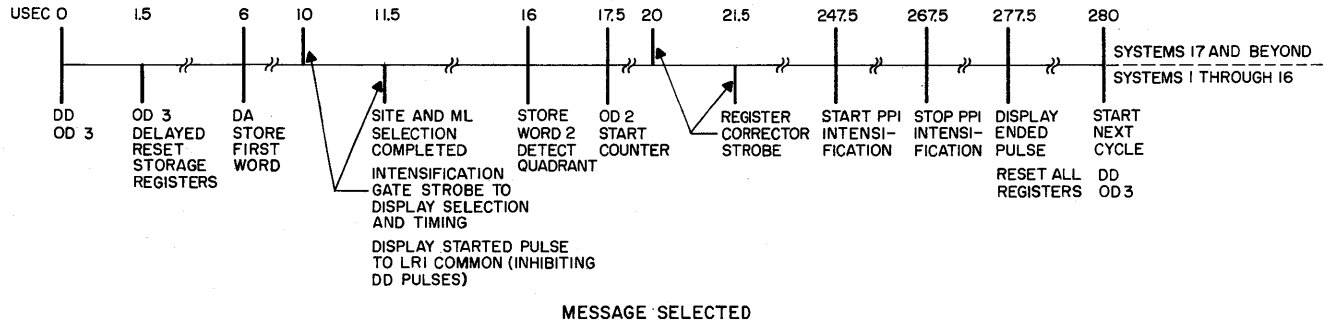


Figure 3—10. LRI Monitor, Overall Timing Charts

reset pulse, causing all storage registers to be reset in preparation for the start of the next cycle. That cycle begins with the next DD pulse at 280 μsec.

If a message selection is not made, drum-demand pulses are not inhibited at 10 μsec, and, at 20 μsec, all storage registers are cleared in preparation for receipt of the next word.

2.1.4.3 Systems 1 through 16

The timing cycle in systems 1 through 16 differs from that in systems 17 and beyond in the fact that an OD 3 delayed pulse (rather than OD 3 pulse) is used as a reference for the action of the word discriminator. Accordingly, registers are reset at 1.5 and 11.5 μsec (rather than 0 and 10); an intensification gate strobe is sent to the display selection and timing circuit and a display-started pulse to the LRI common section at 11.5 (rather than 10) μsec; the register corrector strobe is sent to the register corrector circuit and, when no selection is made, the registers are reset at 21.5 (rather than 20) μsec. In other essentials, the timing cycle is the same for all systems.

2.2 MESSAGE SELECTION CIRCUITS

2.2.1 Site Identity and Message Label Storage Registers

The site identity and the message label storage registers (fig. 3–11) are reset by the drum-demand

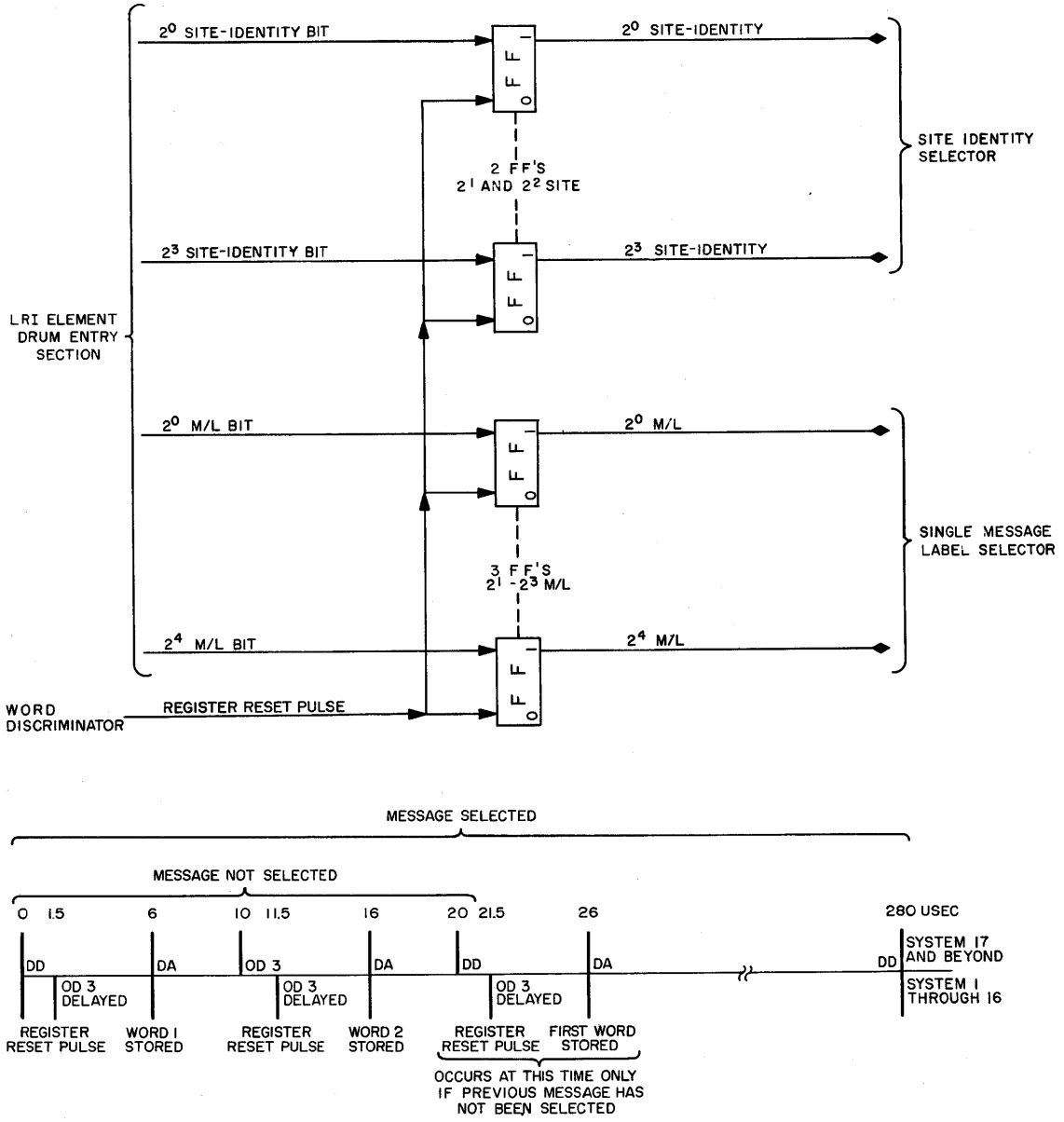


Figure 3–11. Site and Message Label Storage Register, Simplified Logic and Timing Diagrams

pulse at the beginning (0 time) of the timing cycle (1.5 μsec in systems 1–16). At 6 μsec the site identity bits, R12-R15 of the first word, are entered into the 4-FF site identity register and the message label bits, R7-R11 of the first word, are entered into the 5-FF message label register.

The set sides of the site identity flip-flops are connected to the site identity selector circuits. The set sides of all message label flip-flops are connected to the single message label selector circuit and the set side of 2^0, 2^2, 2^3, and 2^4 message label flip-flops are connected to the multiple message label selector circuits. At 10 μsec of the timing cycle, (11.5 μsec in systems 1 through 16), all registers are reset. In the interval between 6 and 10 (or 11.5) μsec, the selector circuits operate on the information supplied to them by their associated registers, to determine whether a message will be selected for display.

2.2.2 Site Identity Selector

2.2.2.1 General

There are four site identity selectors (fig. 3–12), one for each display console. Each selector compares the level applied to the site identity storage register with site identity selection levels supplied by a particular console (or keyboard on unit 947). The selection levels from the consoles are produced by pushbutton-activated circuits discussed in Chapter 5. Depressing a site-selection pushbutton generates a unique set of four levels or bits, as indicated in table 3–1. When these levels complement the levels supplied by the site storage register, the site identity selector indicates selection to the display selection and timing circuit. Circuit operation of the site identity selector is explained below. There are slight differences in the logic of this circuit (but not in the principle of operation) between systems 1 through 16 and succeeding systems. Circuit operation in systems 17 and beyond is regarded as standard and is discussed first. In all systems, the four selectors operate identically.

TABLE 3–1. SITE SELECTION

PUSHBUTTON DEPRESSED	CONSOLE OUTPUT BIT POSITION 4	3	2	1
0	1	1	1	1
1	1	1	1	0
2	1	1	0	1
3	1	1	0	0
4	1	0	1	1
5	1	0	1	0
6	1	0	0	1
7	1	0	0	0
8	0	1	1	1
9	0	1	1	0
10	0	1	0	1
11	0	1	0	0
12	0	0	1	1
13	0	0	1	0
14	0	0	0	1

Note: ONE = +10V level
ZERO = −30V level

TABLE 3–2. MESSAGE LABEL SELECTION

PUSHBUTTON DEPRESSED	CONSOLE OUTPUT BIT POSITIONS 5	4	3	2	1
0	0	0	0	0	1
1	0	1	0	0	0
2	0	1	0	1	0
3	0	0	1	0	0
4	0	0	1	1	0
5	0	0	0	0	0
6	0	0	0	1	0
7	1	0	0	0	0
8	1	1	0	0	0
9	1	0	1	0	0
10	0	1	1	0	0
11	1	0	0	1	0
12	1	1	0	1	0
13	1	0	1	1	0
14	1	1	1	1	0

Note: ONE = +10V level
ZERO = −30V level

2.2.2.2 Systems 17 and Beyond

Assume that (as shown in fig. 3–12) the levels from the site storage register are represented by the binary word 1010. To achieve selection, levels equivalent to 0101 must be supplied by the console. The following conditions are then found; a positive input is applied to OR 1 and OR 3 by the site storage register

and to OR 2 and OR 4 by the console keyboard. Consequently, four inputs to AND 5 are up. There is only one positive input to AND 1, AND 2, AND 3, and AND 4. Therefore, the outputs of those AND's are down and there is no output from OR 5; and consequently, there is an output from the INVERTER circuit. The output of the inverter supplies the fifth input required to produce an output from AND 5.

Inspection of the logic shows that if the inputs from the site storage register and the console are not complementary, there will be no output from the site identity selector circuit. That is, the output of OR 1, OR 2, OR 3, OR 4 will be down or the output of AND, AND 2, AND 3, or AND 4 will be up, or both conditions will prevail.

2.2.2.3 Systems 1 through 16

In systems 1 through 16 there are four inputs to AND 5; the output of the INVERTER goes instead directly to the display selection and timing circuit where an AND checks for coincidence of output from the INVERTER and AND 5.

2.2.3 Single-Message Label Selector

2.2.3.1 General

One single message label selector (fig. 3–13) is associated with each console. The logic of the circuit is very similar to that of the site identity selectors. The main difference is that five levels are applied to each selector circuit by the message label storage register and by the message label pushbutton circuit of the consoles. When the levels from these two sources complement each other, the outputs for OR 1 through OR 5 are up, supplying five of the six possible inputs to AND 6. The outputs of AND 1 through AND 5 are down. Therefore, there is no input to the INVERTER and its output is positive, supplying the sixth input required to bring up the output of AND 6; that is, selection is indicated.

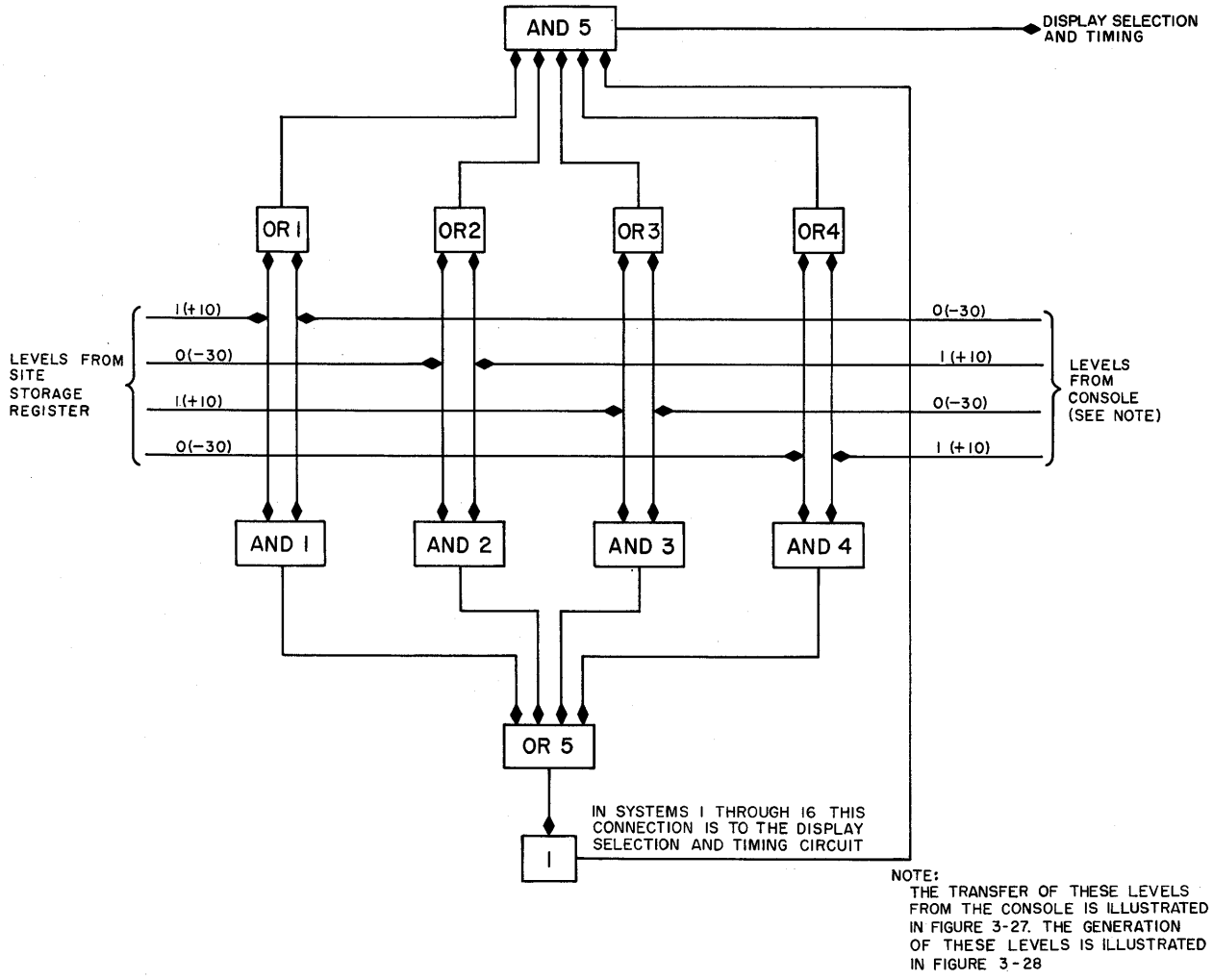


Figure 3–12. Site Identity Selector, Simplified Logic Diagram

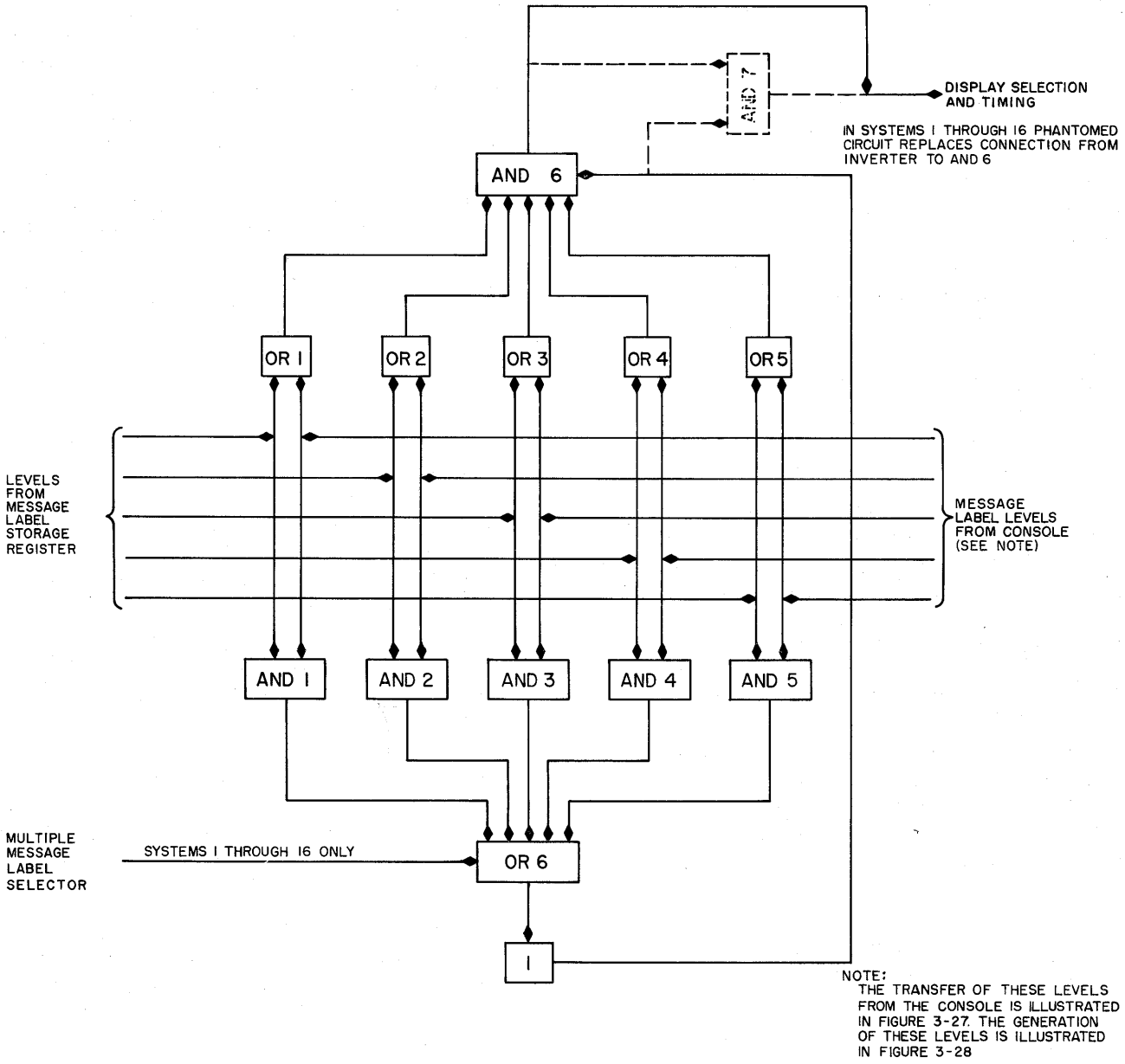


Figure 3–13. Single-Message Label Selector, Simplified Logic Diagram

2.2.3.2 Differences in Systems 1 through 16

In systems 1 through 16, the phantomed circuitry in figure 3–13 is provided, essentially dividing the function of AND 6 between AND 6 and AND 7; the principle of operation is unaffected. Also, an interlock from the multiple message label selector is provided to prevent simultaneous outputs from the single message label and multiple message label selectors associated with one console. Such a condition should not occur if the equipment is operating properly, and the interlock provision is omitted in systems subsequent to system 16.

2.2.4 Multiple-Message Label Selector

The multiple-message label selectors (fig. 3–14) enable the display of all messages from selected sites, except for messages with message labels 17 and 19 in binary (10001 and 10011). These messages label designate height-finder messages which the LRI monitor is not equipped to display. One multiple message label selector is associated with each console. All function identically. The logic operates as follows. An output from the multiple message label selector is available when the AND is up. To produce this condition, inputs to the AND must be supplied by:

a. The least significant bit message label selection line from the console.

b. The set side of FF 2^0 in the message label register.

c. The OR.

Input a is provided by depressing the 0 (multiple message label selection) pushbutton at the console. Levels representing 00001 are then supplied by the console, as indicated in table 3–2. Note that this is the only pushbutton selection which provides a "1" on the least significant bit line.

All message labels actually in use provide input b, since only odd number message labels are used and all odd numbers, in binary, have a 1 in the 2^0 position flip-flop.

All message labels except 10001 and 10011 (17 and 19 in binary) will provide input c; both of these numbers present two 0's directly to the OR and a 1 to the INVERTER, which thus presents a third 0 to the OR.

In other words, the multiple-message label selector provides an output for all message labels in actual use, except binary 17 and 19, when the multiple message label selection is specified at the console.

2.3 TARGET DATA CONVERSION

2.3.1 Sine Storage and Cosine Storage Registers

The sine storage register and the cosine storage register (fig. 3–15) are cleared at zero time by the DD pulse and at 10 (11.5 μsec in systems 1 through 16) by a reset pulse from the word discriminator. At 16 μsec in the timing cycle, the 12 bits of azimuth information L11 – L15 and R9 – R15 of word 2 in the LRI message, are read into the sine storage register and the eleven least significant bits (R9 is excluded) are entered into the cosine storage register.

The first approximation of azimuth sine and cosine function (1.5.4) is achieved by the action of the register corrector on the sine and cosine storage registers. FF 2^{10} and FF 2^{11} in the sine storage register supplies both clear and set output levels to the register corrector. Assume a message has been selected for display. At 20 μsec (21.5 μsec in systems 1 through 16) the register corrector circuit complements certain flip-flops of the sine storage register and all or none of the flip-flops of the cosine storage register, in accordance with the quadrant determination logic described in 2.3.2. The set output of the eleven least significant FF's in the sine storage register are available to the sine binary decoder (analog section). The set outputs of all the FF's in the cosine storage register are available to the cosine binary decoder.

Note

The sine storage register shares the four flip-flops of the site identity storage register and shares three of the flip-flops in the message label storage register. The seven input lines to these flip-flops are time-shared. This economy is made possible by the fact that first word data is cleared from the site identity and message label storage register at 10 (or 11.5) μsec of the timing cycle, allowing these facilities to be used at 16 μsec for processing second word data.

If a message has not been selected for display, no complementation takes place; instead, all registers are cleared at 20 μsec (21.5 μsec in systems 1 through 16) by a reset pulse from the word discriminator.

Note

Only 11 digits are needed to express the contents of the sine register after complementation because the highest possible number in the register is then 2047, binary.

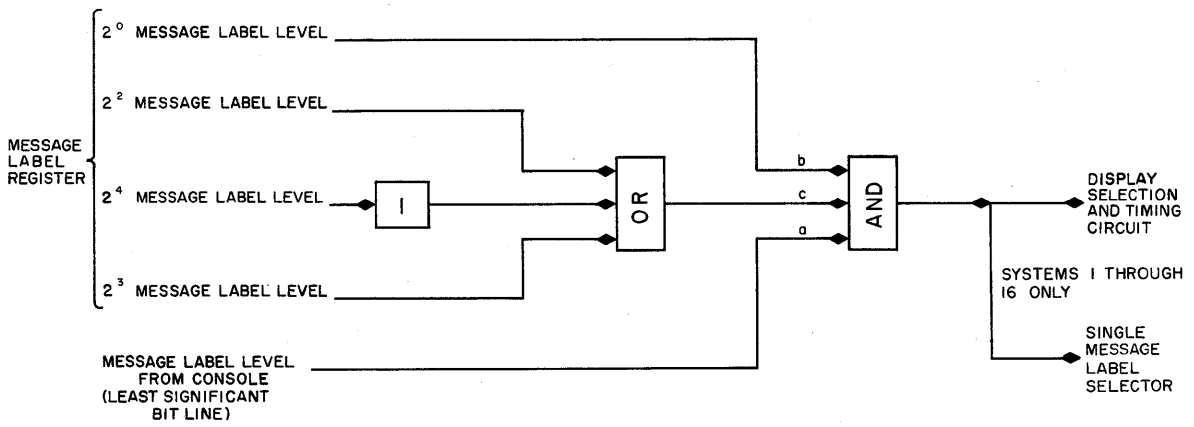


Figure 3–14. Multiple-Message Label Selector, Simplified Logic Diagram

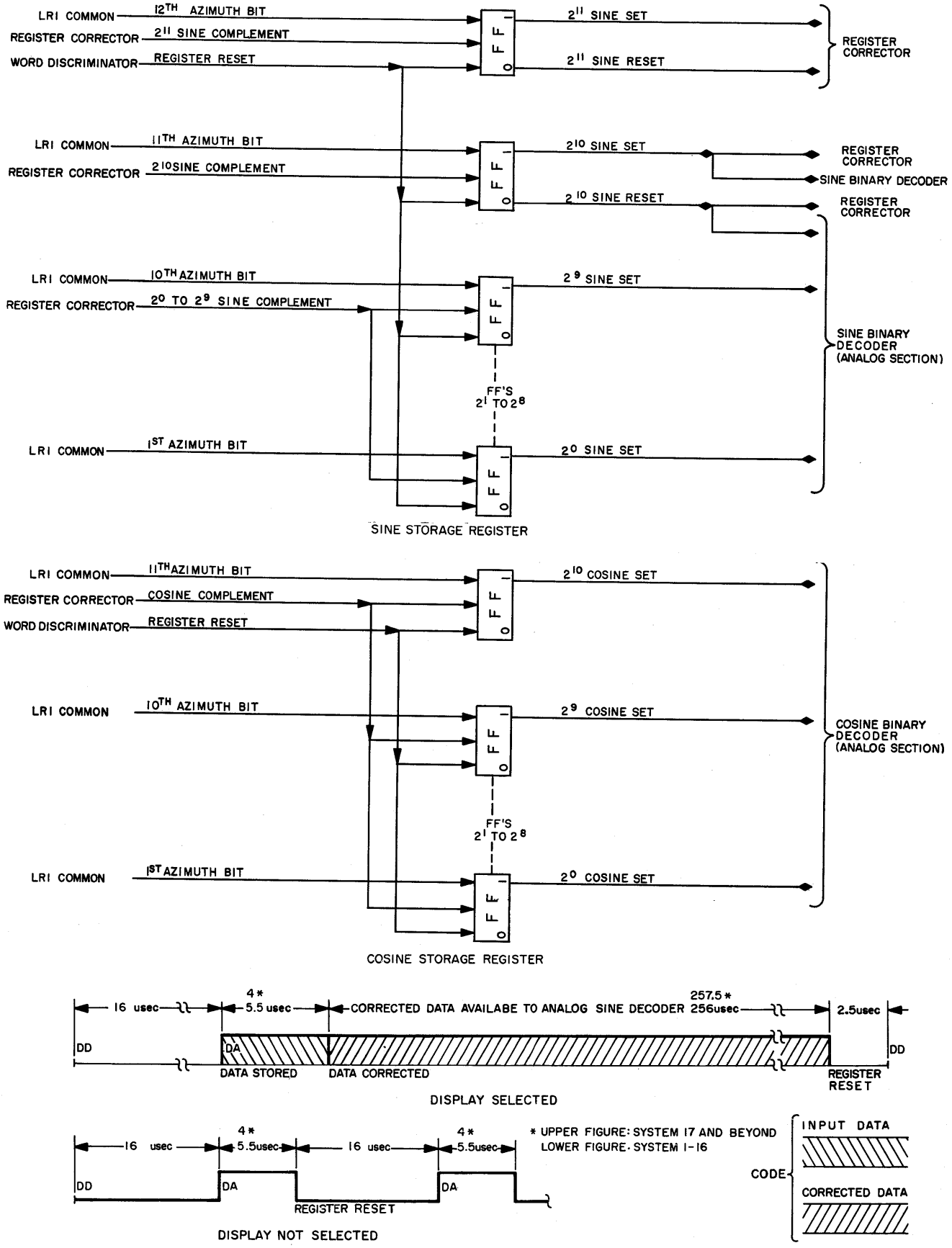
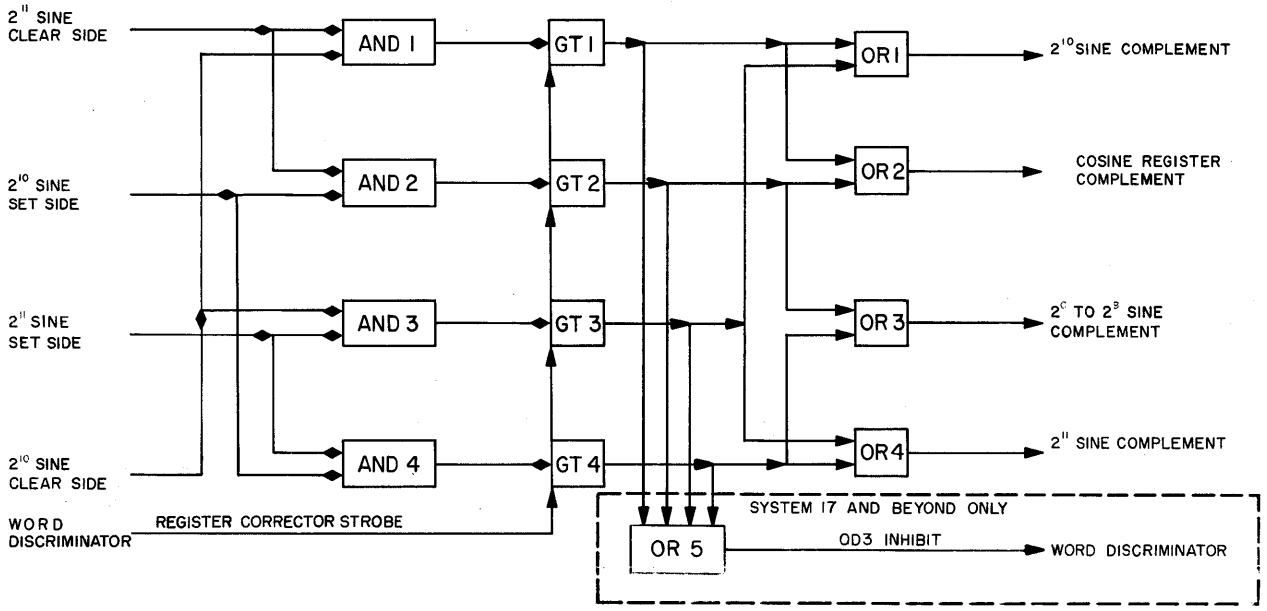
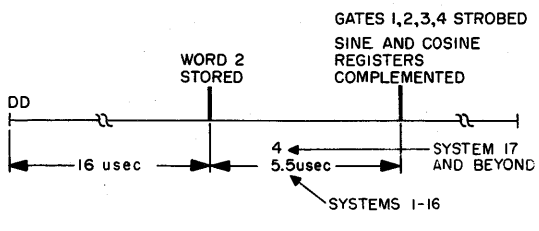


Figure 3–15. Sine and Cosine Storage Registers, Simplified Logic and Timing Diagrams

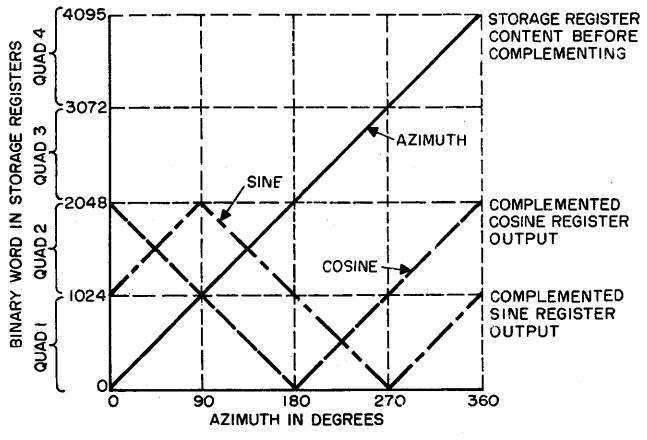
2.3.2 Register Corrector

Complementation of the sine and cosine storage registers to produce first sine and cosine approximations is accomplished as follows. The FF 2^{10} and FF 2^{11} in the sine storage register supply four levels, two from the set side of the flip-flops and two from the clear side, to AND's 1, 2, 3, and 4 in the register corrector (fig. 3–16). At 16 μsec of the timing cycle, azimuth information is installed in the sine storage register and these levels become significant. The combination of possible levels represent the four possible quadrants in which the target may appear. The first quadrant, 0 to 90 degrees, is represented by azimuth values between 0 and 1,023; therefore, FF 2^{10} and FF 2^{11} are clear, bringing up the output of AND 1. The second quadrant, 90 to 180 degrees, is represented by azimuth values between 1,024 and 2,047; therefore, FF 2^{10} is set, FF 2^{11} is clear, and the output of AND 2 is up. The third quadrant, 180 to 270 degrees, is represented by azimuth values between 2,048 and 3,071; therefore, FF 2^{10} is clear and FF 2^{11} is set, supplying the two necessary inputs to bring up AND 3. The fourth quadrant, 270 to 360 degrees, is represented by azimuth values between 3,072 and 4,095; therefore, FF 2^{10} and FF 2^{11} are set, and the AND 4 output is up. Only one AND can produce an output at any given time. The output from each AND goes to a gate having a corresponding designation (AND 1 to GT 1, etc). Four μsec after the AND output is brought up, the register corrector strobe from the word discriminator strobes all four gates. An out-





TIMING



EFFECTS OF SINE AND COSINE REGISTER COMPLEMENTING

Figure 3–16. Register Corrector, Logic and Timing Diagrams

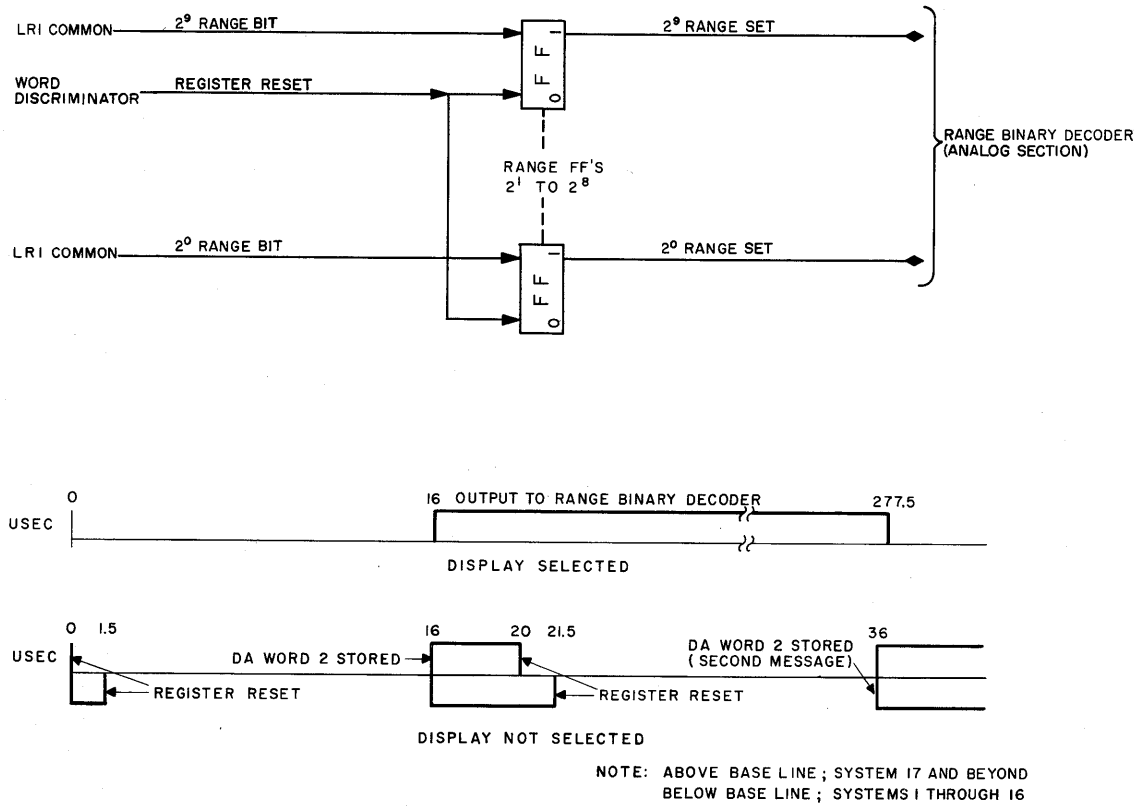


Figure 3–17. Range Storage Register, Simplified Logic and Timing Diagrams

put from GT 1 goes to OR 1 and OR 2, causing FF 2^{10} of the sine storage register and the entire cosine storage register to be complemented. An output from GT 2 goes to OR 2 and OR 3, causing FF 2^{0} through FF 2^{9} of the sine storage register and the entire cosine storage register to be complemented. An output from GT 3 goes to OR 1 and OR 4, causing FF 2^{10} and FF 2^{11} of the sine storage register to be complemented; none of the cosine storage register flip-flops is complemented. An output from GT 4 goes to OR 3 and OR 4 causing FF 2^{0} through FF 2^{9} and FF 2^{11} of the sine storage register to be complemented; none of the cosine storage register flip-flops is complemented.

Note

OR 5 and the OD 3 inhibit pulse are present only in systems 17 and beyond, and are unrelated to the function of the register corrector circuit. The OD 3 inhibit pulse is, in effect, the register corrector strobe (since the strobe always finds one of the gates conditioned); this inhibit pulse is routed through the register corrector rather than directly to its destination in the word discriminator, only because of certain circuit limitations not related to logic operation.

The effects of complementation upon the sine and cosine storage registers are illustrated in figure 3–16 and tabulated below. Note that the chart in figure 3–16 indicates the effects of complementation on the *entire range* of possible inputs to the sine and cosine storage registers (as if the registers were stepped like counters). Each input, of itself, produces a single output level.

QUADRANT	SINE STORAGE REG. 2^{11} BIT	SINE STORAGE REG. 2^{10} BIT	COMPLEMENT SINE REG	COMPLEMENT COSINE REG
1	0	0	2^{10}	ALL
2	0	1	2^{0}–2^{9}	ALL
3	1	0	2^{0}–2^{9}, 2^{11}	NONE
4	1	1	2^{10}, 2^{11}	NONE

2.3.3 Range Storage Register

The range storage register (fig. 3–17) is cleared by the DD pulse (1.5 μsec later in systems 1 through 16); it receives the range information portion of the LRI message, L1 – L10, of word 2, at 16 μsec. The outputs of the set side of the 10 flip-flops in this register are immediately available to the range binary decoder.

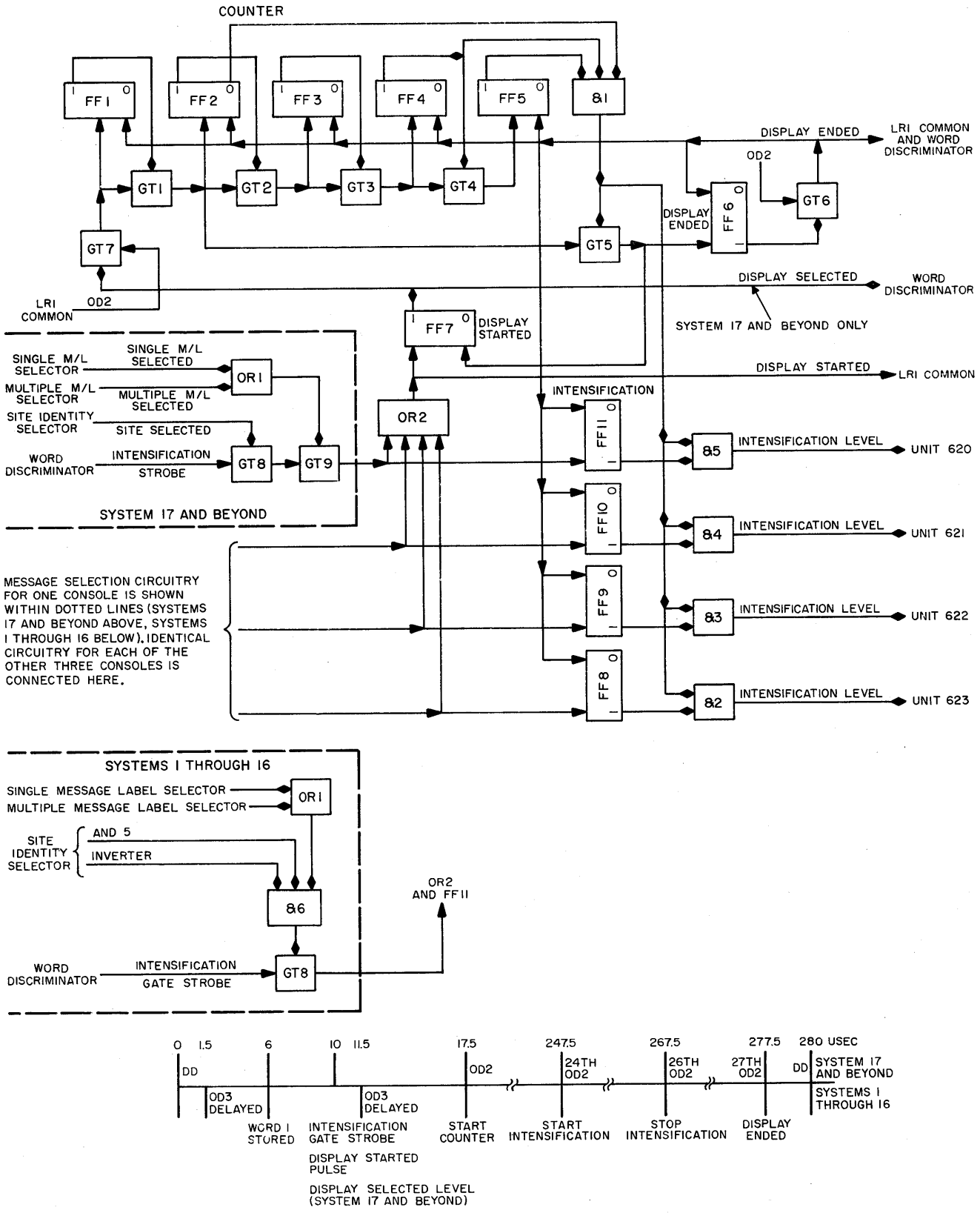


Figure 3–19. Display Selection and Timing, Simplified Logic and Timing Diagrams

2.4 SYNCHRONIZATION AND TIMING

As was pointed out in 2.1.4, synchronization and timing in systems 1 through 16 differs from that in subsequent systems. In the discussion, operation in systems 17 and beyond will be regarded as standard and operation in systems 1 through 16 as a variation.

2.4.1 Word Discriminator

The word discriminator (fig. 3–18, foldout) is the basic control circuit of the LRI monitor, synchronizing its action with the LRI element by triggering, strobing, and resetting other circuits in the equipment at the proper time. Logic operation is discussed below.

2.4.1.1 Systems 17 and Beyond

In systems 17 and beyond (fig. 3–18A) the drum demand pulse (0 time) clears FF 1 and FF 2. At six μsec, the data available pulse accompanying the read-in of drum word 1 complements FF 2 conditioning GT 3. At ten μsec, an OD 3 pulse passes GT 1 and GT 3 (GT 2 is deconditioned). The output of GT 3 is sent to the display selection and timing circuit. If a selection has been made, a display-selected level is returned to condition GT 2. (Concurrently, DD pulses are inhibited in the LRI element.) At 16 μsec, the data available pulse accompanying read-in of word 2 complement-clears FF 2, deconditioning GT 3. At 20 μsec, an OD 3 pulse passes GT 2 as a register corrector strobe. The register corrector circuit returns the pulse without delay as an inhibit OD 3 pulse which sets FF 1. Flip-flop 1 remains set during the remainder of the display cycle, blocking OD 3 pulse, and the circuit is therefore inactive until the next DD pulse initiates a new cycle.

If a selection is not made, GT 2 is not conditioned; the register corrector strobe is not developed; FF 1 is not set. The OD 3 pulse concurrent with the next DD pulse passes GT 1, but, with no effect, since GT 2 and GT 3 are deconditioned. The circuit is in the proper condition for the display cycle initiated by the DD pulse.

2.4.1.2 Systems 1 through 16

In systems 1 through 16 (fig. 3–18B), the DD pulse which is considered to start the timing cycle sets FF 1, conditioning GT 1. The OD 3 pulse, arriving simultaneously, is delayed 1.5 μsec, then strobes GT 1. The output of GT 1 passes through OR 1 to clear all registers in preparation for receipt of the first message word. It also sets FF 3, conditioning GT 4; the DA pulse sets FF 2 six μsec after the DD pulse, conditioning GT 2. The next OD 3 pulse, delayed 1.5 μsec, strobes GT 1 and GT 2 at 11.5 μsec. The output of GT 2 resets FF 2 in preparation for the next DA pulse, and strobes GT 3, which is not conditioned, and GT 4, which is. The output of GT 4 is fed to the display selection and timing circuit as the intensification gate strobe. It also clears FF 3, conditioning GT 3 and deconditioning GT 4; clears FF 1, deconditioning GT 1; and passes through OR 1 to clear the first word out of the registers. (Message selection takes place, if, at all, between 6 and 11.5 μsec; therefore, it is not necessary to store the first word after 11.5 μsec.) The next DA pulse, at 16 μsec, sets FF 2, conditioning GT 2. The third OD 3 delayed pulse strobes GT 1 and GT 2. If a message has been selected for display, DD pulses have been inhibited; therefore, GT 1 is not conditioned and there is no output from it. GT 2 is conditioned, however, and its output resets FF 2 and strobes GT 3 and GT 4. At this time, GT 3 is conditioned, but GT 4 is not. The output of GT 3 (at 21.5 μsec) is fed to the register corrector circuit as the register corrector strobe. Subsequent OD 3 pulses have no effect since both GT 1 and GT 2 remain deconditioned. The circuit is in a sense quiescent, until message display is completed; then a display-ended pulse at 277.5 μsec from the display selection and timing circuit passes through OR 1 to reset the register and a DD pulse arrives at 280 μsec to reset FF 1 and start a new cycle.

If a message is not selected for display, DD pulses are not inhibited; the second DD pulse at 20 μsec resets FF 1 and begins a new cycle.

2.4.2 Display Selection and Timing Circuit

2.4.2.1 General

The display selection and timing circuit (fig. 3–19) determines whether a selection has been made, and, if it has been made, performs the following functions:

a. Sends a display-started pulse to the LRI common, which causes inhibition of further DD pulses, and sends a display-selected level to the word discriminator.

b. Performs a counting action during which the analog current levels achieve stability in the CRT deflection coils.

c. At the end of the count, sends a 20-μsec intensification level to the console for which the display was requested; this level unblanks the CRT at that console, permitting a target indication.

d. Following a target presentation, sends a display-ended pulse to the LRI common, conforming the fact that display has ended, and to the word discriminator, causing the registers to be reset.

In systems 17 and beyond, the logic operates as follows:

OR 1, GT 8, and GT 9 determine whether message selection has been achieved for a particular console (designated unit 620 in fig. 3–19). If either the single message selector or the multiple message selector for that console provides an input to OR 1, GT 9 is condi-

tioned. If the corresponding site selector provides an output concurrently, GT 8 is conditioned. The intensification gate strobe from the word discriminator then passes GT 8 and GT 9 at 10 μsec, setting FF 11. (Had another console selected the message for display, the flip-flop associated with that console, whether FF 8, FF 9, or FF 10, would have been set). The output of GT 8 is also fed through OR 2 to the LRI common as the display-started pulse; in addition, it sets FF 7, conditioning GT 7 and providing a display-selected level to the word discriminator. The OD 2 pulse, at 17.5 μsec passes GT 7, initiating action of the conventional 5-bit counter, composed of FF 1 through FF 5 and GT 1 through GT 4. Succeeding OD 2 pulses step the counter. When the count reaches 24 (247.5 μsec), the output of AND 1 is up (FF 4 and FF 5 set, FF 2 clear), conditioning GT 5 and supplying an input to AND 2, AND 3, AND 4, and AND 5. Since FF 11 was set at 10 μsec, there is an output from AND 5 and an intensification level is supplied to, in this case, unit 620. (Had FF 8, FF 9, or FF 10 been set, the intensification level would have been sent to the associated console.) The 25th OD 2 pulse sets FF 1, conditioning GT 1. The 26 OD 2 pulse passes GT 1 and GT 5, setting FF 6 (the effect of which is described below) and resetting FF 7. The reset of FF 7 deconditions GT 7 and stops the action of the counter at 26. This count finds FF 2 set; therefore, AND 1 no longer provides an output discontinuing the intensification level at the console.

When set, FF 6 conditions GT 6. The 27th OD 2 pulse (at 277.5 μsec) strobes GT 6. The output of GT 6 is the display-ended pulse; it is sent to the LRI common, and to the word discriminator; it also resets the counter, flip-flops FF 6 and FF 8 through FF 11. The display cycle is concluded, beginning again with the next DD pulse (280 μsec).

2.4.2.2 Systems 1 through 16

In systems 1 through 16 the display selection portion of this circuit (within dotted lines in fig. 3–19) is somewhat different from that in subsequent systems. Its function, however, is the same: to determine whether a message has been selected for display at a particular console and, if it has, to start the timing action of his circuit.

In systems 1 through 16, AND 6 provides an output when the site identity selector (2.2.2.3) provides two inputs to it and there is an input from either the single-message selector (2.2.3.2) or the multiple-message selector (2.2.4); in other words, when a message has been selected for display. The output of AND 6 conditions GT 8 which is strobed at 11.5 μsec by the intensification gate strobe. From this point on, the action of the circuit is the same in all systems.

CHAPTER 3
ANALOG SECTION

3.1 GENERAL

The analog section decodes digital information from the sine, cosine, and range storage registers in the digital section (Ch 2) and converts it into two analog voltages which correspond to the X and Y co-ordinates of a target indication on a CRT screen. These voltages are supplied to the four display consoles in a form capable of driving the CRT deflection amplifiers. The corrected inputs from the digital section, representing each target, are sustained for 247.5 μsec to allow analog and display circuitry to achieve stability.

As shown in figure 3–20, analog circuitry is divided into five sections comprising 12 units: binary decoders (3 units); buffer amplifiers (3 units); sine and cosine approximators (2 units); multipliers (2 units); and distribution power amplifiers (2 units). All of these are special circuits, discussed on the logic level below. A test panel associated with the analog section is described in 3.8.

3.2 BINARY DECODERS

The three binary decoders (BD) convert digital input information to corresponding analog voltages. The inputs to the sine and cosine binary decoders represent approximations of the sine and cosine functions, respectively, of the azimuth and, in each case, are supplied in an 11-bit binary code. Information to the third decoder represents target range and is supplied in a 10-bit binary code. The output from each decoder is an

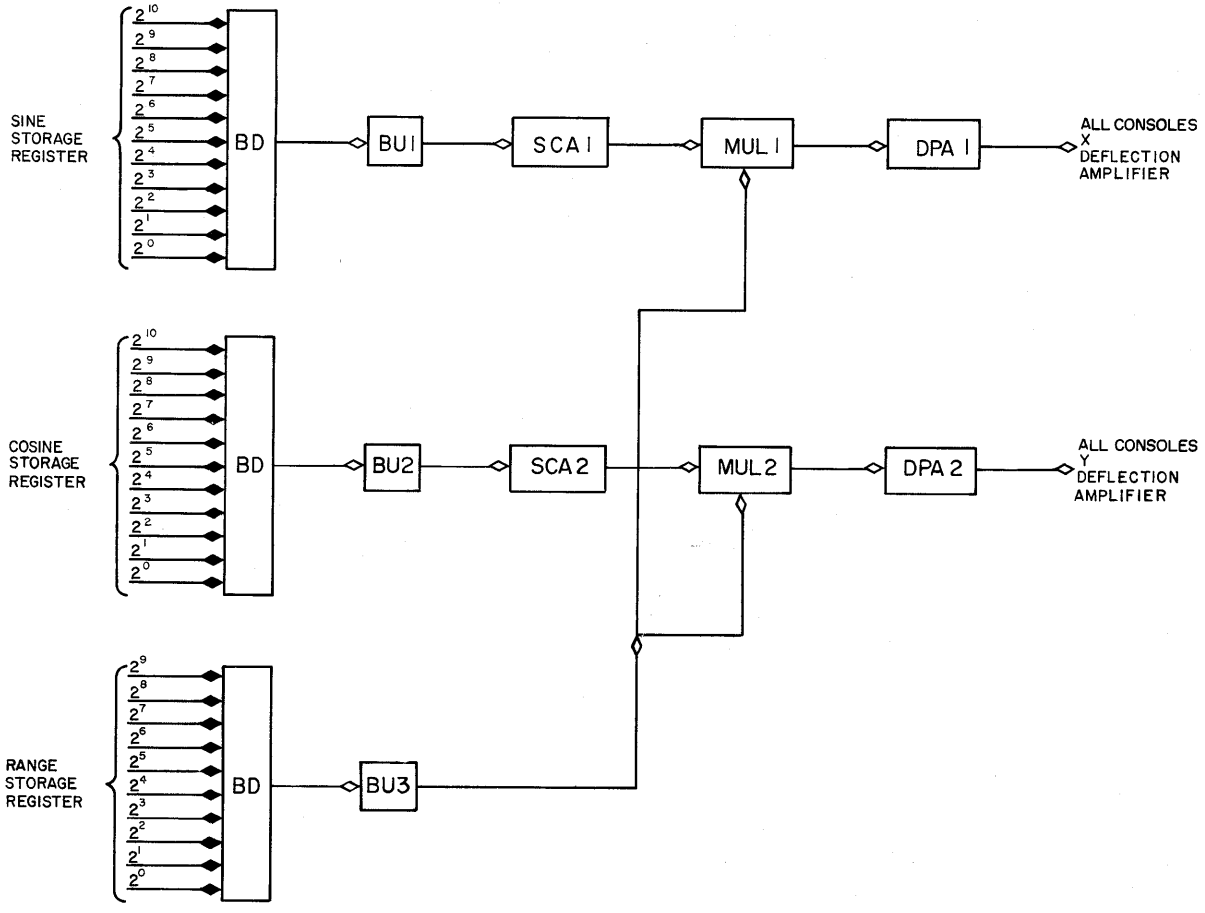


Figure 3–20. Simplified Logic Diagram of Analog Section

analog voltage between fixed limits, 100 and 150V, varying from those limits in proportion to the digital value of the inputs. Thus digital input 00000000000 $(0)_2$ produces an output of approximately 100V, and 11111111111 $(2047)_2$ produces an output of approximately 150V. Intermediate digital values are represented by corresponding intermediate voltages.

3.3 BUFFER AMPLIFIERS

The three buffer amplifiers (BU) are employed to couple the binary decoder outputs to their respective loads. These loads are the sine and cosine approximators for the sine and cosine binary decoders, and, the multipliers for the range binary decoder. The buffer amplifiers shift down the voltage level of the binary decoder output (100 to 150V), providing a zero voltage reference level for this signal and also furnishing a proper impedance match with the binary decoder loads.

3.4 SINE AND COSINE APPROXIMATORS

The sine and cosine approximators (SCA) are identical shaping networks which convert straight-line approximations of the azimuth sine and cosine functions to sinusoidal curves more closely representing these functions. These straightline approximations, in analog form, are supplied by the sine and cosine binary decoders (through the buffer amplifiers) and converted to sinusoidal curves by a proportionate decrease in gain as either limit of the input is approached.

Note

The terms "straight-line approximations" and "sinusoidal curves" describe the effects of the stage upon the entire range of inputs, not upon individual inputs. Each input, considered by itself, is a level. (Refer also to 2.3.2 of Ch 2.)

3.5 MULTIPLIERS

Each multiplier (MUL) receives the output from one of the sine-cosine approximators, and the output from the range buffer amplifier. The sine or cosine input to each unit is multiplied by the range input so that the output of the multipliers becomes R sine θ and R cosine θ, respectively, which correspond to the X and Y rectangular co-ordinates of the target. The mathematical basis of this process is discussed in 1.5.

3.6 DISTRIBUTION POWER AMPLIFIERS

Distribution power amplifiers (DPA) are special circuits which provide sufficient power to drive deflection amplifiers in each of the four display consoles. The amplifiers input impedance is high to match the multiplier outputs, and output impedance is low to match the capacitive loads presented by the connecting cables and CRT deflection amplifiers. The distribution power amplifiers are identical. In the four consoles, one drives all the horizontal deflection amplifiers and the other all the vertical deflection amplifiers.

3.7 POWER SUPPLIES

To provide the high degree of accuracy and stability required in analog circuitry, the analog section employs special regulated voltages in addition to the service voltages used throughout the Combat Direction Central. The voltage supplies and their function are shown in figure 3–21. All are special circuits.

3.8 ANALOG CALIBRATION

3.8.1 Alignment Panel

Alignment circuits and reference voltages are incorporated in the analog circuitry to assure required accuracy of target presentation. A test panel in module C mounts an array of pushbutton switches which are operated in combination to bring out critical points in the circuitry to test receptacles. The outputs of all the signals' stages are thus made easily measurable: binary decoders, buffer amplifiers, sine and cosine approximators, multipliers and distribution power amplifiers. In addition, provision is made to check the individual stages of the binary decoders, +16, −16, −150, and −250 regulated voltages, and the reference voltage utilized in the binary decoders. A toggle (NORMAL-REVERSE) switch permits the polarity of the voltage at the test points to be reversed.

The test panel is used as follows. In each of the four rows of pushbuttons, one pushbutton, called the ROW 1, ROW 2, ROW 3 or ROW 4 pushbutton makes the other pushbuttons in the row effective. For example, to bring the output of the cosine binary decoder to the test points, the ROW 2 pushbutton is depressed; then the COS BD OUT pushbutton in row 2 is depressed.

3.8.2 Multiplier Alignment

A multiplier alignment circuit is included in the analog section to provide test voltages for aligning the multipliers. The multiplier alignment unit generates a-c voltages which are used to drive the multipliers through their complete range of possible input signals. Operation is as follows. A three position switch is located on the front panel of the multiplier alignment pluggable unit. With this switch set to the OPERATE position, the multipliers operate normally; the multiplier alignment circuit is without effect. With the switch in the ALIGN RANGE position, the multiplier alignment circuit provides a 50-volt peak-to-peak a-c input to the range inputs of the multipliers and grounds the azimuth inputs. Adjustments are then made on the multipliers to provide a zero output (as nearly as possible) throughout the entire range of the a-c input. With the switch set to the ALIGN AZIMUTH position, the mul-

tiplier alignment circuit provides a 32-volt peak-to-peak a-c input to the azimuth input of the multipliers and grounds the range inputs. Again adjustments are made on the multipliers to provide a zero output (as near as possible) throughout the entire range of the AC input.

3.8.3 Other Alignment Circuits

Other controls used in alignment are located on the pluggable units containing the circuitry to be aligned. For example, in alignment of individual stages in the binary decoders, the DECODER STAGE ADJ switch on the binary decoder pluggable unit is operated to select the stage; then the appropriate switches in row 4 are operated to permit measurements, at the test points, of the alignment voltage for this stage. To understand the purpose of the controls on the pluggable units, consult the appropriate circuit description in the Special Circuits manual. A full description of alignment procedures is found in T. O. 31P2-2FSQ7-162, *Maintenance Techniques and Procedures of Input System for AN/FSQ-7 Combat Direction Central (Revised 1 April 1957).*

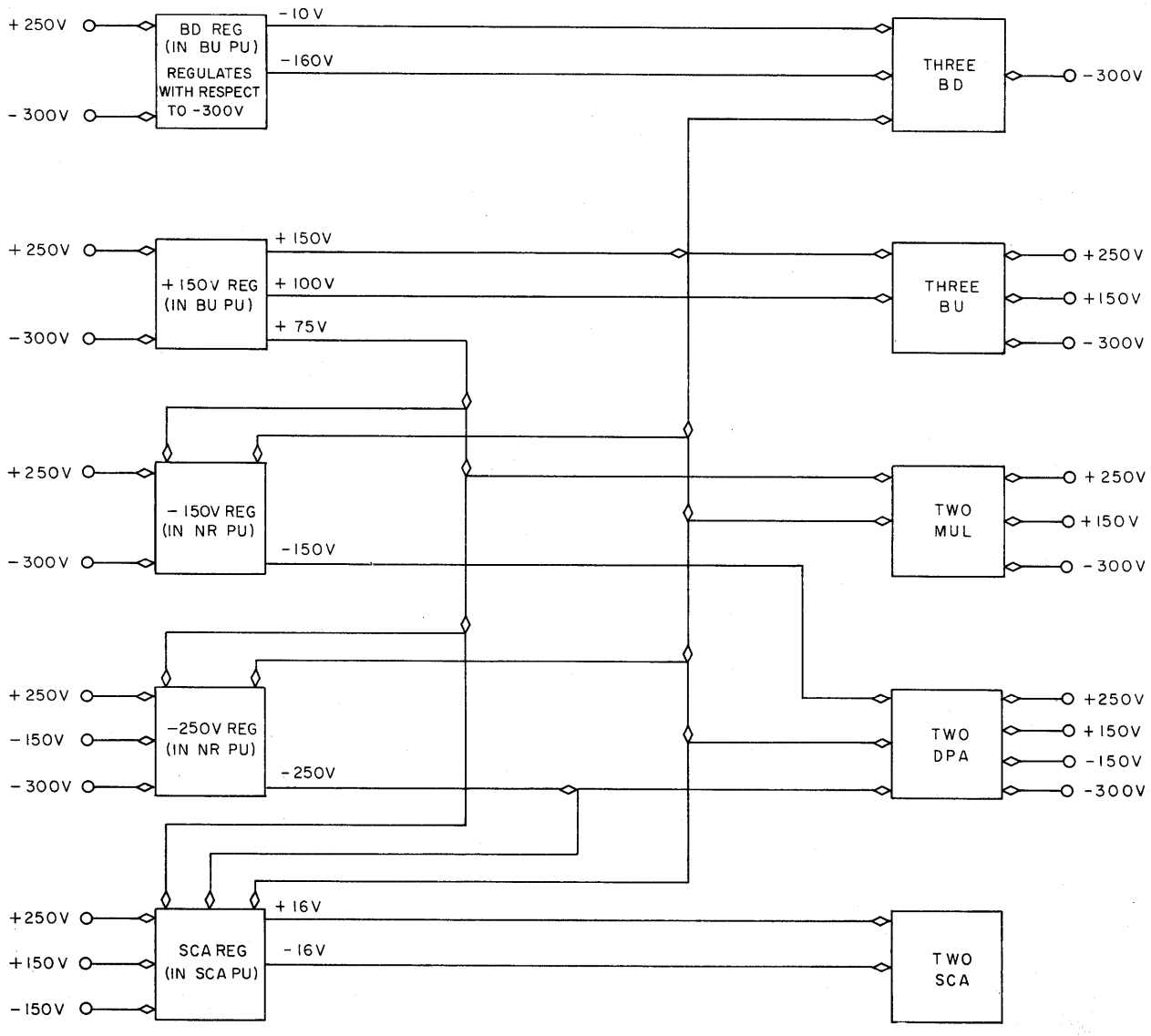


Figure 3–21. D-C Distribution and Voltage Regulation, Analog Section

CHAPTER 4
DISPLAY SECTION

4.1 OPERATION OF CRT SECTION

4.1.1 General

The CRT with its associated circuitry is block diagrammed in figure 3–22. This conventional arrangement requires a CRT for display, a yoke (not illustrated) for positioning the CRT electron beam, two deflection amplifiers to provide sufficient drive for the yoke, and a high-voltage power supply for operation of the CRT. The intensification pulse indicated occurs at 247.5 μsec in the display cycle. Applied to the control grid, it allows the intensity of the electron beam to increase, thus causing screen fluorescence.

The high-voltage power supply and deflection amplifiers are special circuits and this section is concerned only with their logical application.

4.1.2 Cathode-Ray Tube

The CRT used for display is a conventional magnetic-deflection-tube, employing a typical electron gun and a round 16-inch screen coated with a medium-persistence phosphor. When a target is to be displayed, the magnetic deflection fields are set by the yoke; then the electron beam is turned on for 20 μsec by a 40V intensification pulse.

4.1.3 Deflection Amplifiers

Current delivered by the distribution power amplifiers in the analog section is not sufficient to drive the CRT deflection coils, and, therefore, must be amplified. This is done in deflection amplifiers, two of which, a horizontal and a vertical deflection amplifier, are located in each of four LRI monitor consoles.

The deflection amplifiers are direct-coupled, negative-feedback interchangeable units, each supplying current to one axis of a yoke. Amplification is linear and output is in phase with input. Individual gain and centering controls and input and output test points for each amplifier are located on the calibration test panel (4.2) in each console.

All horizontal deflection amplifiers are connected in parallel and driven by the same distribution amplifier simultaneously. The vertical deflection amplifiers, also connected in parallel, are driven by the other distribution amplifier.

4.1.4 High-Voltage Power Supply

A high-voltage power supply is located in each LRI monitor console. It provides 2,500 and 7,500V for the accelerating anodes of the CRT and it is powered through the UNIT STATUS switch and relays located in the console. Major components of the high-voltage power supply are the transformer, selenium bridge rectifier, filtering circuit, and load resistors. A voltmeter is mounted on the front of the power supply unit for monitoring the output.

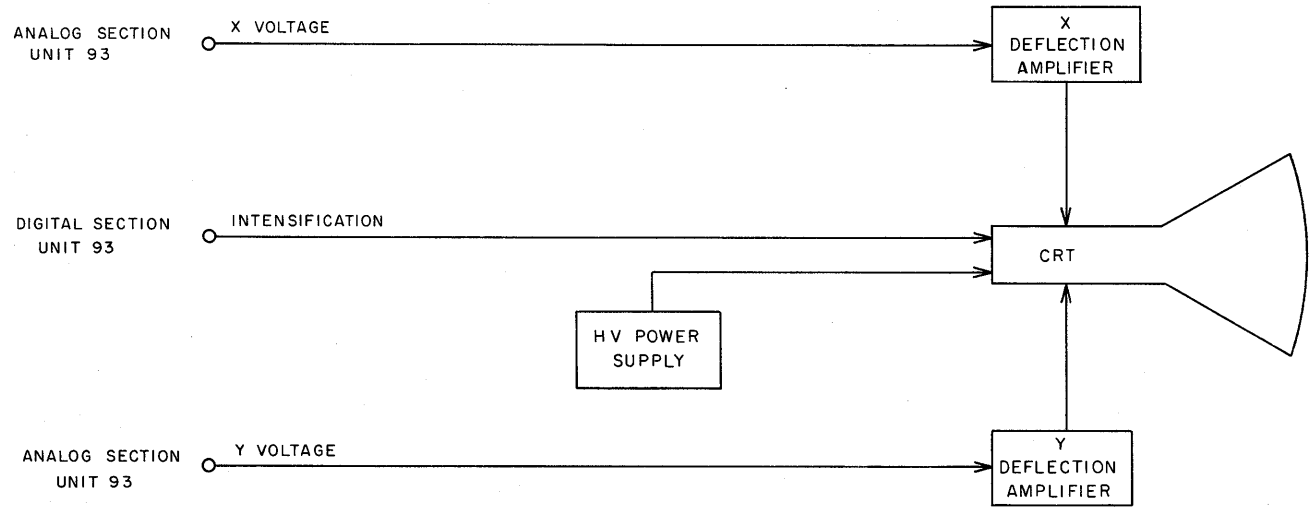


Figure 3–22. Block Diagram of CRT Circuitry

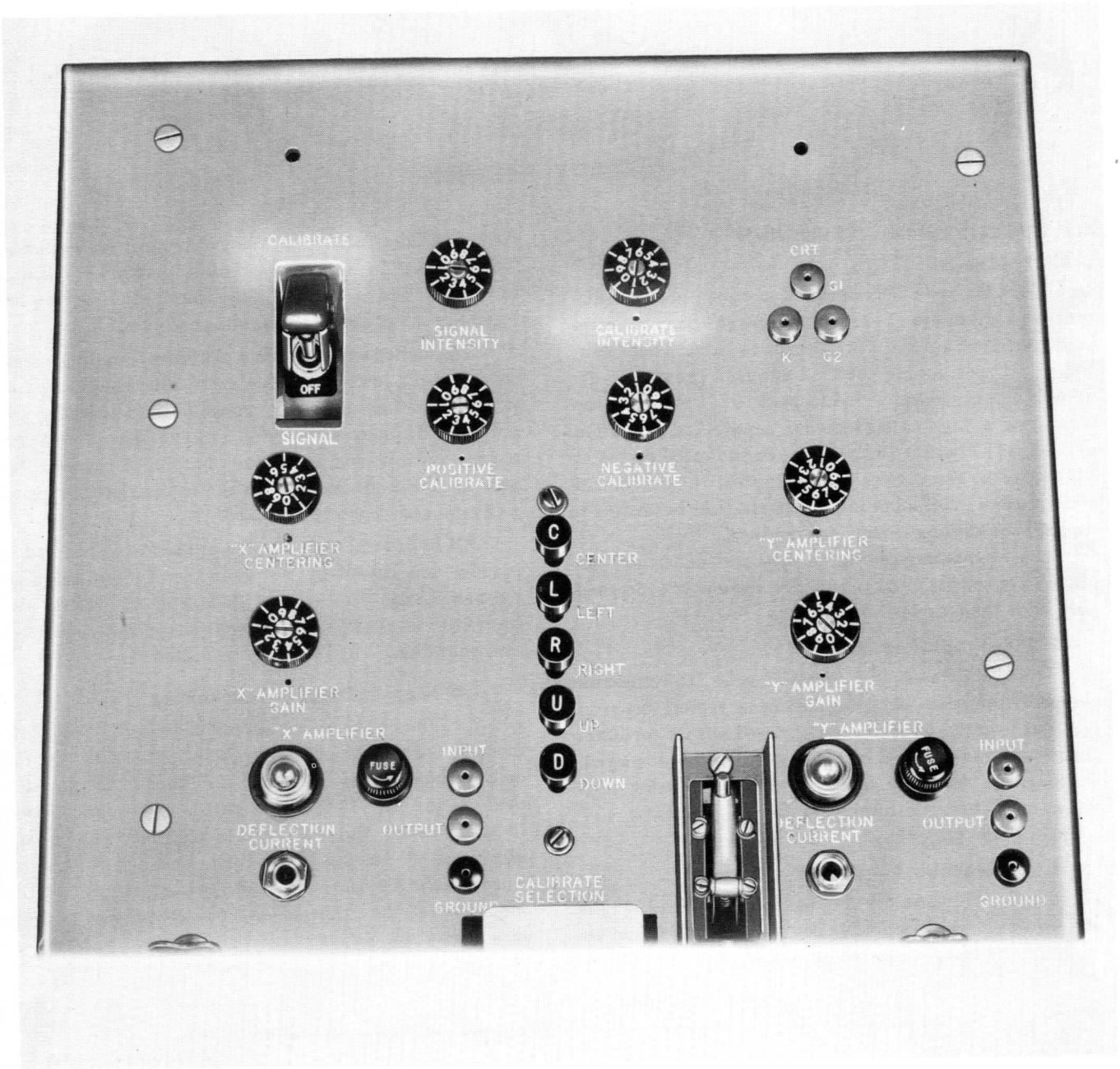


Figure 3–23. Display Console Calibration Test Panel

4.2 CALIBRATION

4.2.1 General

A test panel is incorporated in each console to permit calibration of the deflection amplifiers and adjustment of signal intensity. It is located beneath a hinged cover on top of the console. The test panel and calibration circuitry are shown, respectively, in figures 3–23 and 3–24.

4.2.2 Circuit Switching

When the CALIBRATE SIGNAL switch is in the OFF position, two sets of contacts on relay K23 connect the X and Y deflection levels to the corresponding deflection amplifiers, and one set of contacts on relay K24 connects the intensification level to the control grid through coupling capacitor C14. Another set of contacts on relay K24 connects a variable, negative-bias voltage from resistor network R40, R41, R42 to the control grid. This bias is controlled by the SIGNAL INTENSITY control and determines the intensity of the display.

When the CALIBRATE SIGNAL switch is in the ON position (calibrate mode of operation) relays K23 and K24 are energized and the CRT and deflection am-

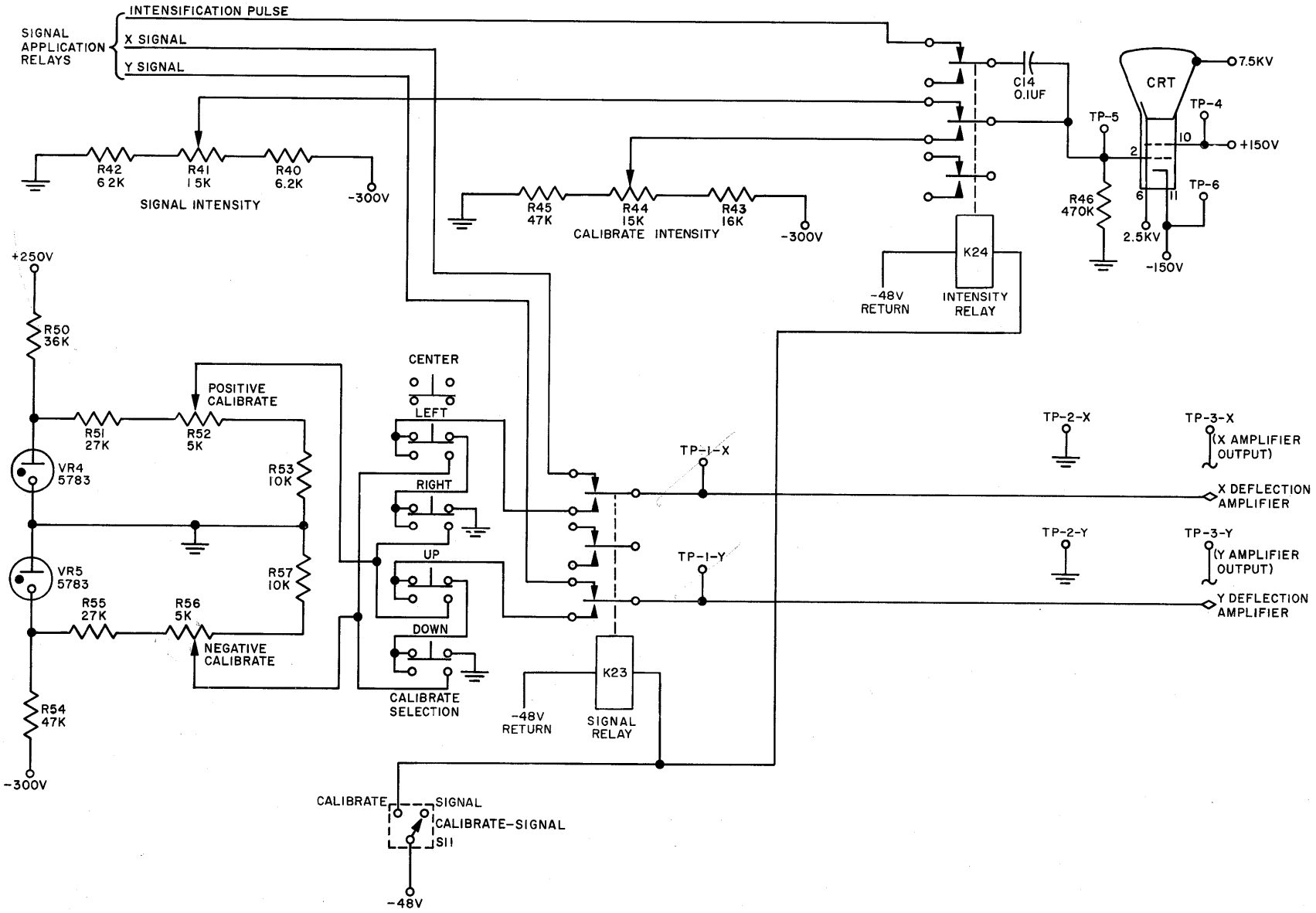


Figure 3–24. Calibration Test Panel, Circuit Diagram

plifier connections are switched from the input signals to internal calibration voltages. CRT control grid bias is then tapped from the voltage divider network R43, R44, R45 and adjusted by the CALIBRATE INTENSITY control.

Relay K23 connects the deflection amplifier inputs to the CALIBRATE SELECTION pushbutton switches labeled CENTER, LEFT, RIGHT, UP, and DOWN. These switches are interlocked so that depressing one pushbutton releases the other four. The CENTER button makes no connection, but, when depressed, it releases the other four switches so that the deflection amplifier inputs are connected to ground. The zero potential on the grounded inputs corresponds to the zero (center) position of the CRT display, and calibration for proper display is made by the X and Y amplifier controls labeled CENTERING. The two centering controls are located on the calibration test panel, but are electrically part of the respective deflection amplifier circuits.

Depressing the LEFT or DOWN pushbutton removes the respective amplifier input ground and connects the input to a negative calibration. This voltage causes the display to shift left or down as the case may be, and the deflection amplifiers may then be calibrated for a known spot displacement by adjusting the X and Y amplifier controls labeled GAIN. The same action takes place when the RIGHT or UP button is depressed except that the calibration voltage is positive and the display appears right or up. The calibration GAIN controls used for LEFT and DOWN are also used for right and up, and, like the centering controls, are electrically part of the respective deflection amplifier circuits.

4.2.3 Calibration Voltages

Voltages for calibrating the deflection amplifiers are taken from the voltage divider network shown on the left in figure 3–24. Plus 250V is supplied to the network through current limiting resistor R50, and the positive potential in the circuit is maintained by the voltage regulator tube VR4. Minus 300V is supplied through current limiting resistor R54, and the negative potential in that circuit is maintained by the voltage regulator tube VR5. The positive and negative voltages are developed across voltage dividers R51, R52, R53, and R55, R56, R57, respectively.

4.2.4 Calibration Test Points

Test points located on the calibration test panel are identified and explained in table 3–3. Use of these test points and the various adjustment controls are explained in the maintenance manual for the Input System, T.O. 31P2-2FSQ7-162.

TABLE 3–3. DISPLAY CONSOLE CALIBRATION TEST POINTS

CIRCUIT (fig. 3–24)	PANEL (fig. 3–23)	PURPOSE
TP1-X	INPUT	To check calibration voltages or signal input to the respective deflection amplifier
TP1-Y	INPUT	
TP2-X	GROUND	Ground connection for test lead
TP2-Y	GROUND	
TP3-X	OUTPUT	To check deflection amplifier output voltage
TP3-Y	OUTPUT	
TP4	G2	To check CRT focusing grid voltage
TP5	G1	To check CRT control grid voltage
TP6	K	To check CRT cathode voltage
(In the X and Y deflection amplifier circuits)	DEFLECTION CURRENT	To check current flowing in the X and Y deflection coils
	DEFLECTION CURRENT	

CHAPTER 5
SWITCHING SECTION

5.1 GENERAL

The switching section contains the controls, indicators, and circuitry required to control the operation of the LRI monitor. Specifically, it performs the following functions.

a. Determines which of the two simplex power supplies will supply power to each monitor console.
b. Determines which half of the duplexed LRI monitor control unit, 93A or 93B, will be connected to a particular console; that is, will feed intensification and deflection levels to the CRT, and receive site identity and message label levels from the console.
c. Provides controls (site identity and message label pushbuttons) and associated circuitry for message selection.
d. Controls operation of the camera, including start-stop, and film exposure-time selection. Indicates, within the camera field, site identity and message label selection and film exposure-time selections. Also provides indications of alarm conditions pertaining to camera operation.

Physically, the switching section is distributed among the four display consoles of the monitor and auxiliary control console unit 947. Functionally, it may be thought of as consisting of four subsections: unit status switching, signal application relay circuitry, site identity and message selection circuitry, and camera control circuitry. The relationship of these subsections to each other and to other portions of the LRI monitor is illustrated in figure 3–25, and described generally, for a typical console, below. Detailed circuit operation is described in 5.2 through 5.5.

A —48V service voltage is supplied to each console on four of eight lines selected by the position of the duplex power switch and simplex power switch at the duplex switching console. The UNIT STATUS switch at each of the LRI monitor consoles then applies this service voltage to filament and power contactors and to signal application relays appropriate to the UNIT STATUS switch position.

The signal application relay circuitry relates the console to the A or B section of unit 93, depending on which Direction Central computer has been designated active and depending on the position of the console UNIT STATUS switch. The console then feeds message selection voltage levels to the selected (93A or 93B) section, which, in turn, supplies CRT deflection levels and, when a message is selected for display, supplies an intensification level to the console.

The site identity and message label selection circuitry contains the pushbutton controls by which messages are selected for display at a particular console. Each site identity or message selection pushbutton activates none, one, or several relays supplying a unique combination of bits (10V and —30V levels) to the signal application relay circuitry, which, in turn, passes them on to the digital section of unit 93A or unit 93B. In camera console unit 621, the site identity and message label selection relays employ extra sets of contacts to light indicators in the camera field. These indicators identify the display in the photographic record by associating it with the pushbuttons that elicited the display.

Camera operation controls and indicators are found at unit 947. The associated relays and timing gear are located in unit 621. By means of these controls and associated circuitry, camera operation is initiated, the duration of film exposure is determined, the film is advanced, and visual and audible alarms are presented when the film is about to run out. Other indicators on unit 947 show when the shutter is open and whether the UNIT STATUS switch on unit 621 is in the ACTIVE or STANDBY position.

5.2 UNIT STATUS SWITCH

A UNIT STATUS switch (fig. 3–26) on each LRI monitor console permits the console operator to control the application of power to the console and relate the console, as desired, to the active or standby duplex machine and simplex power supply.

The UNIT STATUS switch uses six sections of a 4-wafer, ganged rotary switch. (Each wafer contains two switch sections.) As shown in figure 3–26, section A controls the application of voltage to the C filament contactor; section B controls the application of voltage to the D filament contactor; sections C and D control the application of the standby and active voltages to the the C and D power contactors. Sections E and F control the application of standby or active energizing voltages to the signal application control relays.

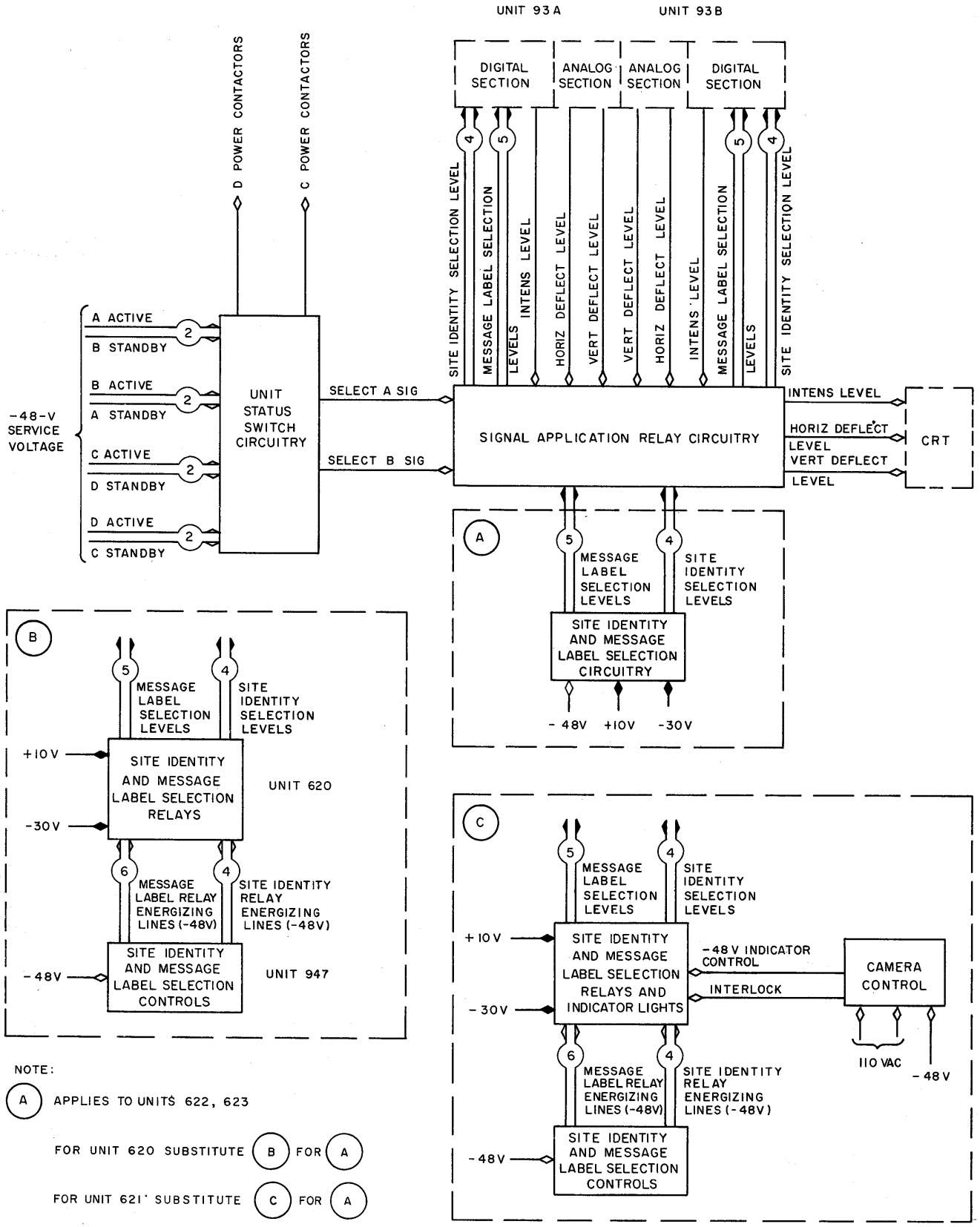


Figure 3–25. Section Diagram of Switching Section

The functions of the UNIT STATUS switch positions are as follows: in the FILAMENTS, POWER ON, and STANDBY positions, the UNIT STATUS switch causes the console to draw power from the standby designated simplex power supply; in the FILAMENT position, filament power alone is supplied; and in the POWER ON and STANDBY positions, all operating voltages are supplied. The STANDBY position, in addition, applies relay operating voltage from the standby-designated duplex machine to the signal application relays.

In the OFF position, no power or operating voltages of any kind are supplied in the console. In the ACTIVE position, operating power for the console is drawn from the active-designated simplex power supply; and the active-designated duplex machine furnishes the energizing voltages to the signal application relays.

Operation of the UNIT STATUS switch circuitry is described below. Assume the following switch positions at the duplex switching console:

SIMPLEX switch in C ACTIVE-D STANDBY position

DUPLEX switch in B ACTIVE-A STANDBY position

The C ACTIVE-D STANDBY position of the SIMPLEX switch (C simplex power supply designated active) causes —48V to be applied to the following terminals: 5 of section A; 1, 2, 3 of section B; 5 of section C; and 2, 3 of section D of the UNIT STATUS switch. Accordingly, the FILAMENT, POWER ON, or STANDBY positions of this switch cause the D filament contactor to be energized, and the POWER ON and STANDBY positions also cause the D power contactors to be energized. The OFF position is blank. The ACTIVE position causes the C filament and power contactors to be energized.

The B ACTIVE-A STANDBY position of the DUPLEX switch (B duplex machine designated active) causes application of —48V to terminal 3 of section E and to terminal 5 of section F of the UNIT STATUS switch. Accordingly, the STANDBY position of the UNIT STATUS switch applies relay-energizing voltage on the select A signal line, and the ACTIVE position applies relay-energizing voltage on the select B signal line.

The effects of other positions of the SIMPLEX and DUPLEX switches may be observed by referring to figure 3–26.

5.3 SIGNAL APPLICATION CONTROL RELAYS

The signal application control relays (fig. 3–27, foldout) connect the console to unit 93A or unit 93B, depending on the setting of the UNIT STATUS switch. Relays K1, K2, and K3 are A group relays, energized by the select A signal line and used to connect the console to unit 93A; K4, K5 and K6 are B group relays, energized by the select B signal line and used to connect the console to unit 93B. Of these relays, K3 or K6 feeds intensification and deflection levels from unit 93 to the console CRT, and K1 and K2, or K4 and K5 supply message selection levels from the message label and site identity selection relays to unit 93.

Assume that energizing voltage is applied on the select A signal line (A machine active and UNIT STATUS switch on ACTIVE position, or A machine standby and UNIT STATUS switch on STANDBY position). X-deflection, Y-deflection, and intensification levels from unit 93A are then supplied to the CRT by way of contacts 1a-1c, 3a-3c, and 5a-5c, respectively, of K3. Relay K1 feeds the five message label bits to unit 93A and relay K2 feeds the four site identity bits to unit 93A. When the B group relays are picked, corresponding connections are made by K4, K5, and K6 between unit 93B and the console.

5.4 SITE IDENTITY AND MESSAGE LABEL SELECTOR SWITCH AND RELAY CIRCUITRY

5.4.1 General

The site identity and message label selection switching circuitry (fig. 3–28, foldout) is used to express requests for message display. It consists of two 15-button interlock-release pushbutton switch assemblies for each console, one for site identity selection, and one for message label selection and associated relays. The pushbutton assemblies for units 622 and 623 are located on the consoles, and for units 620 and 621 on auxiliary control console unit 947. In all cases, however, the associated relays are found in the consoles. A pushbutton, when depressed, applies —48V to none, one, or several of these relays. The relays, in turn, supply a configuration of +10 and —30V levels, equivalent to 1 and 0 bits, respectively, to the signal application relays which pass the bits to the digital section of unit 93A or 93B for comparison with the message selection data in the LRI message.

In the camera console unit 621, additional circuitry, described in 5.4.4, is provided to light lamps in the camera field, indicating which site identity and message label selection have been made. An interlock circuit is also provided which makes message selection effective, only if it is performed before film exposure is started; this circuit is described in 5.4.5.

5.4.2 Message Label Switches and Relays

The circuitry consists of relays K20, K33 through K37, and MESSAGE switch S104. Relays K33 through K37 supply +10V levels (1 bits), when energized, and —30V levels (0 bits), when energized, to the signal application relays. Each pushbutton causes from none to three of relays K33 through K37 to be energized. For

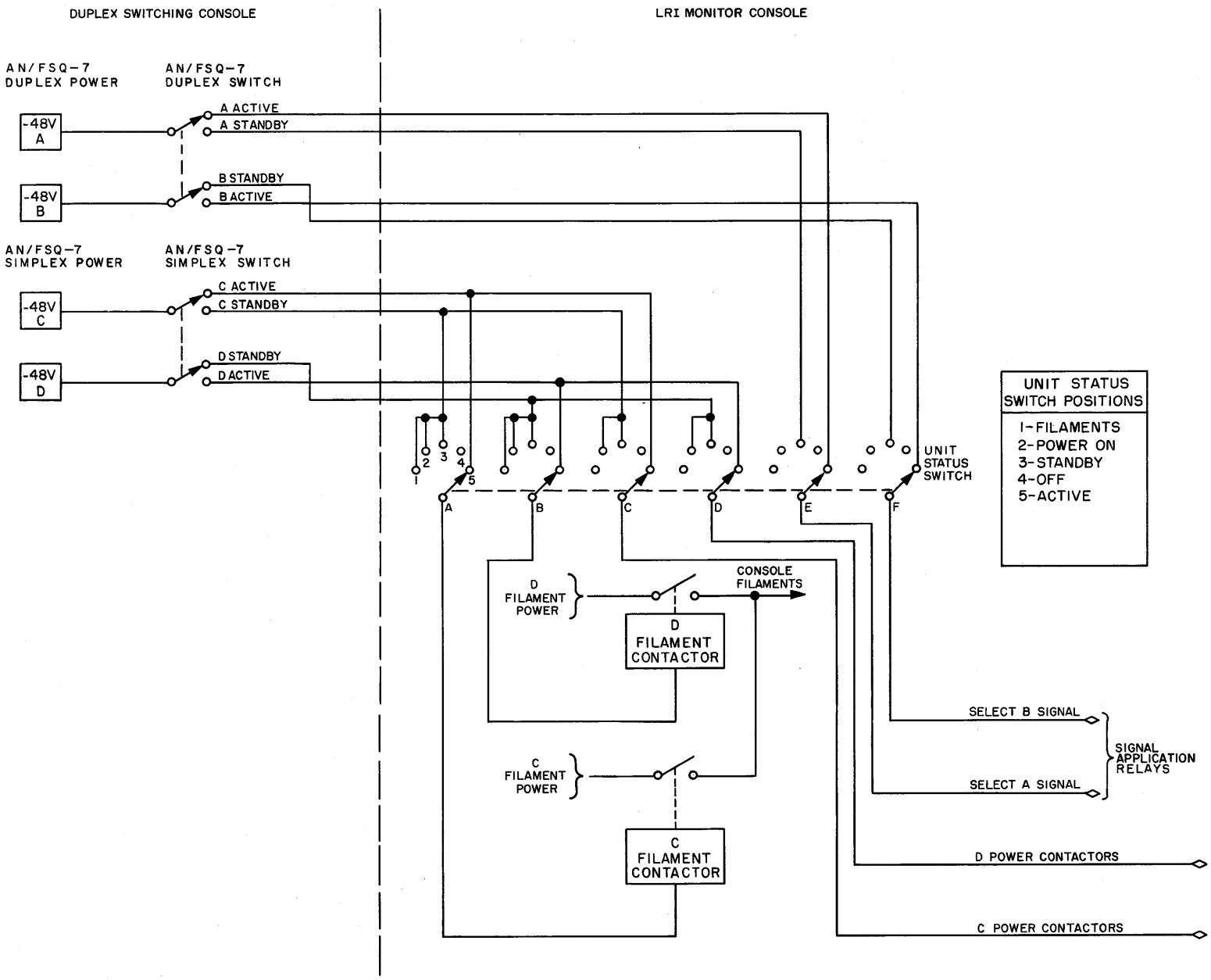


Figure 3–26. Unit Status Switching Diagram

example, pushbutton 1 applies —48V to K36, supplying a +10V level in the fourth M/L bit position. The output configuration of the circuitry is therefore 01000. Pushbutton 9 energizes K35 and K37. The output configuration is therefore 10100. Pushbutton 14 operates somewhat differently. When pressed it energizes relay K20. The contacts of K20 apply —48V to K34 through K37, producing output configuration 11110. When depressed, pushbutton 0, the multiple M/L pushbutton, causes K33 to be energized, supplying a 1 on the M/L bit 1 line through contact 1a of this relay. The output configuration is therefore 00001 (refer to 2.2.4). Table 3–2 lists the binary configurations produced by all pushbuttons.

Note

The order of significance of bit positions is from right to left, to correspond to the order of significance of the bits in the site and message label portions of the LRI message.

5.4.3 Site Identity Switches and Relays

The site identity switch circuitry consists of relays K38 through K41 and SITE switch 103. The relays supply + 10V (1 bits) in the unenergized condition and —30V (0 bits) in the energized condition to the signal application relay circuitry. All of the pushbuttons of S103 operate similarly. When depressed, each causes from none to three of relays K38 through K41 to be energized. For example, pushbutton 3 energizes relays K38 and K39. The output configuration is then equivalent to 1100. Note that this is the complement of 0011 (binary 3), which designates LRI site 3 in the LRI message. The output configurations produced by all pushbuttons are listed in table 3–1.

5.4.4 Site Selection and Message Label Indicators, Unit 621

In unit 621 (fig. 3–29, foldout), lamps are provided in the camera field to record the selections made by the MESSAGE and SITE switches S104 and S103. The switches and associated relays operate as in the other consoles, but additional sets of relay contacts and also additional relays (K21 in the message label circuitry and K22 in the site identity circuitry) are employed to light appropriate lamps, when the switch pushbuttons are depressed. Operation is as follows:

Assume message label pushbutton 9 is depressed. As described in 5.4.3, relays K35 and K37 are thereby energized. Relay K21, paralleled with K37, is also energized. Relays K20, K33, K34, and K36 are not energized. Accordingly, the —48V return circuit for indicator DS 25 is completed through contacts 2a-2c of K21, 4a-4b of K36, 3a-3c of K35, 2a-2b of K34 and 3a-3b of K33. Lamp DS-25 is the indicator for MESSAGE pushbutton 9.

Assume, next, that site selector button 3 has been depressed. As described in 5.4.3, relays K38 and K39 are thereby energized; K40, K41, and K22 are not energized. Accordingly, the —48V return circuit for indicator DS-4 is completed through 3a-3b of K41, 2a-2b of K40, and 2a-2c of K39 and K38. The —48V return circuits set up by other pushbutton selections can be similarly traced in figure 3–29.

Lighting voltage is made available to all lamps in the camera field when film exposure is initiated. Those lamps which are provided with a —48V return light. Approximately two seconds after film exposure begins, the —48V supply line to all indicator lamps is disconnected (to prevent overexposure). The timing-control of power for this purpose is performed in the camera control circuitry and is described in 5.5.

5.4.5 Film Exposure Interlock, Unit 621

An interlock circuit consisting of relays K46, K48, K49, K50, and K51 is provided in unit 621 to prevent a new message selection, made after film exposure has been initiated, from taking effect until exposure is completed. Relays K49 and K51 are normally energized through contacts 1-2 and 4-5, respectively, of unenergized K46. Relay K49 passes the message label levels from switch S104, and relay K51 passes the site selection levels from switch S103, to the message selection relays.

Initiation of film exposure causes relays K48 and K50 to energize. Relay K46 is then energized through contacts 5a-5c of K50 and the following actions take place. Relay-energizing voltage is applied through contacts 2-3 and 5-6 of K46 to the bussed "a" contacts of K48 and K50, respectively, and, because these relays are energized, it is applied to holding contacts of the message selection relays. Concurrently, —48V is disconnected (at K46) from K49 and K50. These relays deenergize, and the condition of S103 and S104 no longer affects the message-selection relays. However, —48V at the holding contacts of these relays keeps energized those message selection relays already energized. The overall effect, therefore, is to continue the conditions established by the message selection switches S103 and S104 but to inhibit the effect of any change in the setting of those switches during exposure. (Relay K46 is make-before-break to assure reliability in the action described above.)

As an example, depressing pushbutton 9 of S104 causes K35, K37, and K21 (paralleled with K37) to energize. When exposure is initiated, energizing voltage to these relays is discontinued. Concurrently, however, this voltage is applied through contacts 4a-4c of K48 to holding contact 4c of K35, and through 6a-6c of K48 to 5c of K21 which holds both K21 and K37. Thus, relays K35, K37 and K21 remain energized. Should the condition of S104 be changed during exposure, it will

have no effect since this switch is effectively disconnected at K49. When exposure ends, energizing voltage is no longer applied to K48, K50, and K46. Accordingly, relays K49 and K51 are energized and the settings of S104 and S103 again establish the condition of the message selection relays.

5.5 CAMERA CONTROL CIRCUIT

5.5.1 General

Camera-console unit 621 photographs the displays on the CRT, recording, at the same time, the site identity and message label selections associated with each display, film exposure time, and the clock time of the display, as shown on a 24-hour clock in the camera field (fig. 3–30, foldout).

Camera operation is controlled by means of pushbuttons, alarms and indicators at unit 947. The associated relays, timing gear, and other control devices are found in unit 621. Control functions include:

a. Film exposure control and exposure-time indicators.
b. Indicator disconnect circuit (disconnects all indicator lamps on the camera field after film has been exposed approximately 4 seconds).
c. Film advance after a film exposure is complete.
d. Alarm indications (when 4 feet of film are left).
e. Film interlock (prevents camera operation when there is no film in magazine).

5.5.2 Film Exposure Control

5.5.2.1 Controls and Indicators

The main film exposure controls and indicators are the following:

a. EXPOSURE SELECTION switch S105, an interlocked-release 5-pushbutton switch. The buttons are used to select film exposure times of 8, 10, 12, 14, and 16 seconds, respectively.
b. MULTIPLIER SELECTION switch S106, an interlocked-release 5-pushbutton bank switch. The buttons select a factor of 1, 2, 5, 10, or 20, respectively, by which the exposure-time selected by switch S105 is multiplied.
c. START switch S301, a momentary-contact switch which initiates film-exposure.
d. STOP switch S302, a momentary-contact switch which may be used to terminate exposure manually. Note that this switch is *normally closed.*
e. EXPOSURE ON indicator X6 indicates when camera shutter is open.
f. EXPOSURE and MULTIPLIER SELECTION lights. These lights in the camera field indicate which exposure selection and multiplier selection buttons have been pushed.

In addition, ACTIVE and STANDBY indicators (X9 and X8) indicate the status of the console as established by the UNIT STATUS switch; the FILM ALARM indicator X5 indicates when 4 feet, or less, of film remains in the magazine; the AUDIBLE ALARM I 101 is energized concurrently with the FILM ALARM indicator and manually cleared by the CLEAR AUDIBLE ALARM S303 pushbutton.

5.5.2.2 General Description of Circuit Operation

Depressing the START switch energizes shutter solenoid A1 and relay K101. The solenoid opens the shutter, starting film exposure. Relay K101 starts motor B101. By a self-latching action, K101 remains energized, continuing to apply power to B101 and keeping the shutter solenoid energized for a period determined by the setting of the exposure selection pushbutton S105 and the multiplier selection pushbutton S106. These switches set up a circuit which is completed at the desired time by the action of motor B101, cam-actuated switch S103, and stepping switch assemblies S101 and S102. The shaft of B101 revolves at a 30-rpm rate, cam-actuating S103, and, immediately afterwards, S104, once every revolution. The switches are closed for 1/4 second. The action of S104 may be ignored at this time. Each closing of S103 actuates S102, the exposure-selection stepping switch, causing S102A and S102B to step to the next position. When S102AB reaches a position selected by exposure selection switch S105, it steps very rapidly through the remaining positions and in so doing actuates the multiplier-selector stepping switch S101, causing S101A-B to step once. When S101, in turn, reaches a position designated by the multiplier selection switch S106, causes relay K101 to de-energize, stopping exposure. The opening of S104 on each revolution has no effect until K101 de-energizes; the next opening of S104 stops B101.

5.5.2.3 Detailed Description of Circuit Operation

The detailed description below assumes 12-second and X10 multiplier film-exposure selections; that is, pushbuttons 2 of S105 and 3 of S106 are depressed. Depressing START switch S301 applies —48V on the —48V hold line to shutter solenoid A1, opening the shutter; the same action applies —48V on the exposure-off line through normally closed STOP switch S302 to relay K101 (and also to contact 27 of S101A which may be ignored at this point). Energizing of K101 has the following effects.

a. Contacts 1a-1c of K101 produce a latching effect to keep K101 energized after the START switch is released. The latching circuit is: —48V line, contacts C-D (film interlock) of P14-J14,

contacts 1a-1c of K101, —48V hold line, normally closed S302, exposure-off line, Y terminal of K101. Relay-energizing voltage will remain on the —48V hold line until K101 is de-energized.

b. The voltage on the —48V hold line keeps the shutter solenoid energized.

c. The —48V hold line also branches to K102 and K103; these relays apply power to the exposure and multiplier selection indicators, as described in 5.5.4, when the —48V return is supplied through S101 B-26 or -1.

d. Motor B101 has stopped with cam-operated S104 open. Contacts 2a-2c of K101 complete the 110V a-c line to B101, starting the motor.

Each revolution of the motor actuates S103, completing the —48V return to stepping switch S102. (Z side of S102 contacts 2a-2c of energized K101, switch S103.) Since —48V is always applied (through the film interlock) to S102, this switch is energized, stepping S102 A and B once; that is, to position 1. Contacts c3c-c3a are mechanically closed and remain closed. Two seconds later, S103 is actuated again, causing S102A and B to step to position 2. When the switch has stepped to position 6, —48V return is connected through pushbutton 2 (12-second exposure) of S105 and contact 6 of S101A to the arm of S102A, and thus to the Z side of relay K104. The relay is energized and is then held by a latching circuit: Z terminal and contacts 1c-1a of K104 closed contacts c2c-c2a of S102, contacts 2a-2c of K104. Switch S103 opens when the cam rotates past it, but a —48V return is provided S102 through its interrupter contacts c1c-c1a. The interrupter operates in a manner similar to an electric bell clapper, rapidly making and breaking the —48V return circuit to the Z side of S102. As a result, stepping switch S102A and B steps very rapidly to its home (26) position. As the arm of S102B passes through position 10, it extends —48V return, permanently connected to contact 27 of S102B, to the Z terminal of S101. Switch S101 then steps once to position 1. When switch S102 reaches home, contacts c2c-c2a open mechanically; the latching circuit for K104 is opened, discontinuing the stepping action of S102. The action described above is now repeated; S103 closes at 2-second intervals, stepping S102 at the same rate, and when S102 has stepped a number of times determined by the setting of exposure selector switch S105 (6 steps in the example given), it steps rapidly to home, stepping S101 once. Contact 10 of S101A is connected to —48V return through pushbutton 3 (X10 multiplier) of S106. When S101A and B reach position 10, the —48V return is extended to the Y side of K101 shorting this relay. De-energizing of K101 has the following effects:

a. Voltage is removed from the —48V hold line; the shutter solenoid is thereby de-energized and the camera shutter closes, ending exposure.

b. Motor B101 stops with the stopping circuit operating as follows: the 110V connection to terminal E110 of B101 is made through two paths. One path through S104 opens once every revolution of the motor shaft: normally, with no effect, since power is available through the other path, contacts 3a-3c of K101. That path is opened, however, when K101 de-energizes. Consequently, the actuating of S104 immediately following de-energizing of K101 removes power from B101 which stops with S104 open.

c. Contacts 4a-4b of unenergized K101 maintain —48V return to S102 (through c2c and c2a of that switch) furnishing a reset circuit for that stepping switch, and contacts 5a-5b of K101 perform the same function for S101.

5.5.3 Stop Mechanisms

Film exposure may be manually terminated at any time by means of the STOP switch S302. Depressing this normally closed switch opens the latching circuit for K101. De-energizing of K101 has the effects listed a through c above.

A safety circuit is provided to limit the duration of exposure when no selection is expressed by S105 and S106. Depressing the START switch initiates the stepping of S102 at the usual 2-second intervals. When S102 reaches position 9, —48V return is extended from contact 27 of S102B through the arm of S102A to the Z side of K104, energizing this relay with the effects described in 5.5.2; that is, S102 steps rapidly to home and steps S101 once. When S101 has stepped to position 21, relay K101 is shorted, terminating exposure. Thus, the maximum length of exposure, when no exposure duration is otherwise expressed, is 378 seconds (9 x 2 x 21).

5.5.4 Selection Indicators and Indicator Disconnect Circuit

When exposure starts, relay-energizing voltage is applied on the —48V hold line to relays K102 and K103. The return connection for these relays is made through contacts 27-26 of S101B and 26-27 of S102B, and the relays are energized. Minus 48 volts is then connected through contacts 1a-1c of K102 to the bus for all the indicator lights in the camera field; the following lights illuminate:

DS 45 Message label: identifies message label indicators

DS 46 Clock: identifies clock

DS 47-48 Clock illumination lights: illuminates clock

DS 49 Site identity: identifies site identity lights

DS 41 Exposure: identifies exposure selection lights

DS 42 Second: identifies seconds-exposure selection lights

DS 43 and DS 44 Multiplier: Identifies exposure-multiplier selection lights

Power is made available to all other indicator lights, and those illuminate for which a —48V return has been provided. The contacts of K102, other than 1a-1c, and the contacts of K103 extend —48V return to the seconds-exposure and exposure-multiplier-selection lights selected by S105 and S106, respectively. Thus, in the example used in the present explanation, the lighting circuit for DS33 is completed through contacts 3a-3c of K103 and through the contacts of pushbutton 2 (12-second exposure) of S105; and the lighting circuit for DS 39 is completed through contacts 2a-2c of K102 and the contacts of pushbutton 3 (X10 multiplier) of S106. The establishment of —48V return circuits for appropriate message label and site identity selection lights has been described in 5.4.4.

Four seconds after exposure is initiated, S102 steps for the second time and the —48V return circuit to K102 and K103 is opened. The relays de-energize and lighting power is discontinued for the indicators in the camera field. The —48V return line to K102 and K103 remains disconnected during the entire exposure period since it runs through contact 26 of S101A and therefore opens as soon as S101 steps once. (But for this feature, the indicators would light for four seconds during each cycle of S102.)

5.5.5 Film-Advance Circuit

The film-advance motor advances the film one frame after exposure is concluded, in preparation for the next exposure. The motor is controlled, as follows. When shutter solenoid A1 is activated, 110V ac is applied through its c-a contacts to the set coil (K43A) of film-advance relay K43, closing this relay's contacts. When the solenoid is de-energized at the conclusion of the exposure, 110V ac is applied through solenoid contacts a-b and the now closed contacts of K43 to the film-advance motor, thereby advancing the film. The contacts of cam-actuated switch S7 close. The reset coil (K43B) of K43 is energized through contacts 1a-1c of S7, opening the contacts of K43. However, operating current continues to be applied to the film-advance motor through contacts 2a-2c of S7, until the cam releases the S7 contacts. By this time, the film has been advanced on frame.

The film may also be advanced manually by depressing the film advance pushbutton. This momentary action switch applies 110V ac to the film advance motor.

5.5.6 Film Alarm Circuit

When 4 feet of film remain, a roller riding on the reel of unexposed film comes close enough to the center of the reel to close the contacts of switch S6. The —48V circuit is thereby completed directly for FILM ALARM indicator X5 and is completed through the normally closed 3c-3b contacts of film alarm relay K105 for the audible alarm I101. To stop the audible alarm CLEAR AUDIBLE ALARM switch, S303 is pressed. Relay K105 is thereby energized, opening the audible alarm circuit (The FILM ALARM indicator circuit is unaffected.) Contacts 1a-1c provide a latching action for K303, keeping this relay energized after S303 is released. The relay is reset and the lamp is extinguished only by replacement of the film, which opens switch S6.

5.5.7 Miscellaneous Circuits

5.5.7.1 Film Interlock

The equipment is interlocked to prevent camera operation when no film remains on the magazine. The interlock connects contacts C-D of J14. When this connection is open, the —48V of service voltage is available only to the alarm circuits.

5.5.7.2 EXPOSURE ON Indicator

The —48V hold line branches to the EXPOSURE ON indicator, X6; thus this light is on during film exposure.

PART 4
GAP-FILLER INPUT ELEMENT

CHAPTER 1
INTRODUCTION

1.1 GENERAL

This part describes the theory of operation of the gap-filler input element (GFI). The discussion parallels the flow of data through the element, although the detailed description of the operation of the GFI mapper is presented in the final chapter (Ch 6) of this part.

1.2 FUNCTION OF THE GAP-FILLER INPUT ELEMENT

The primary functions of the GFI element are reception of information from GFI radar sites, conversion of the information into a binary form acceptable for use by the Central Computer, and transmission of the data to the LOG drum for eventual transfer to the Central Computer System. The operations of the GFI element and the transfer to the Drum System are synchronized with the timing of the LOG drum. The GFI mappers of the element provide the facility to filter out undesired targets to eliminate loading the Central Computer with unnecessary information.

1.3 RELATIONSHIP OF THE GFI ELEMENT TO INFORMATION SOURCES

The GFI radar sites are remote from the receiving Central and telephone-line facilities are used to transmit the modified radar data to the Central. The relationship of the GFI element to the originating and transmitting facilities is illustrated in figure 4–1. Information originating at the GFI radar site is processed by the coordinate data transmitter and is presented as slowed-down-video data to the digital data transmitter (DDT). The DDT adapts the information for telephone-line transmission to the digital data receivers (DDR's). The data conversion receivers (DCR's) of the GFI element convert the output of the DDR's into a pulse form acceptable for use by the GFI element.

Data is modified at the radar site to adapt the radar data for transmission by available narrow-band telephone-line facilities. The modification process is known as quantizing and the resulting data is called slowed-

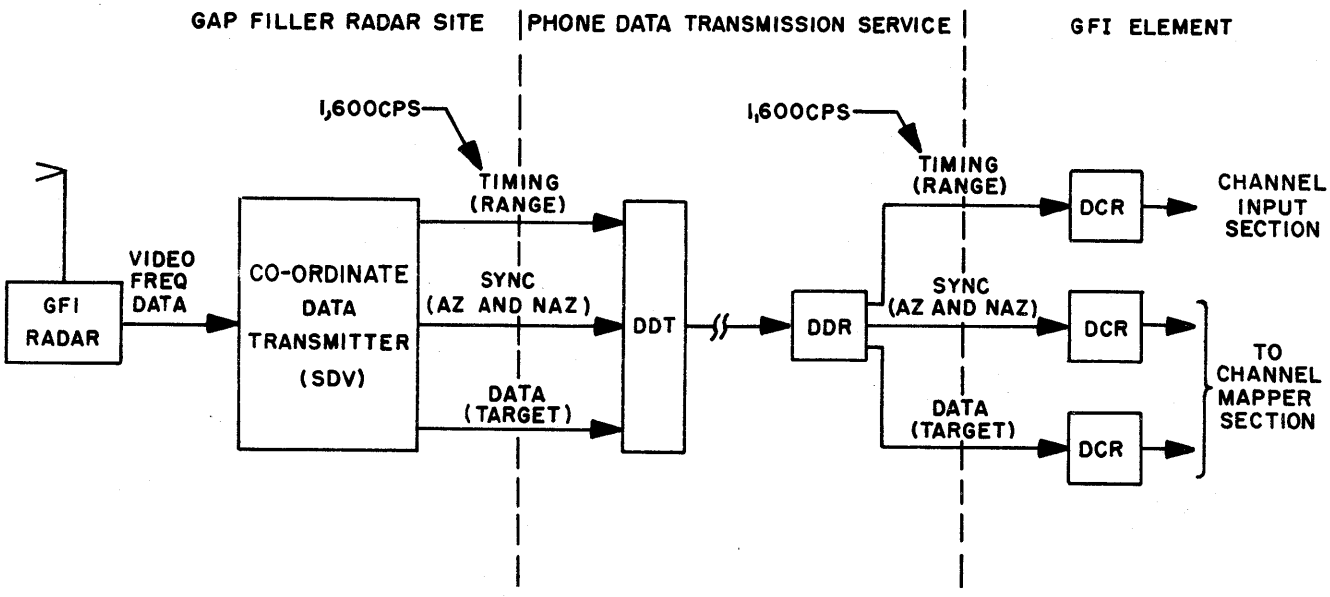


Figure 4–1. Transmission of GFI Information

down-video information. The slowed-down-video information is coarse-grained (less detailed than LRI information), since only one target indication is generated for a given area although multiple targets may exist. A target (or targets) is indicated as being present in an area, a number of azimuth sectors from north and a number of range increments from the radar site. For a detailed description of quantizing and slowed-down-video, refer to Part 1, Chapter 2, of this manual.

The input to the timing DCR consists of a continuous 1,600-cps signal with each cycle representing one range box. The input to the sync DCR consists of one cycle of a 1,600-cps signal denoting the beginning of an azimuth cycle. When the radar antenna passes north, two consecutive cycles of a 1,600-cps signal will appear on the sync line. A target will be indicated by one cycle of a 1,600-cps signal on the input line to the data DCR. The single cycles on the sync and data lines will be in synchronism with the timing cycles. The DCR's convert the 1,600-cps signal into signals usable by the input equipment.

1.4 PHYSICAL DESCRIPTION

The GFI element is made up of unit 34 and GFI mapper consoles, units 600 through 617. Unit 34 (fig. 4–2) contains the channel and common equipment. There may be a maximum of 18 mapper consoles (one of which is shown in fig. 4–3). Two of the channels and the associated mapper consoles are spares and may be substituted for other channels.

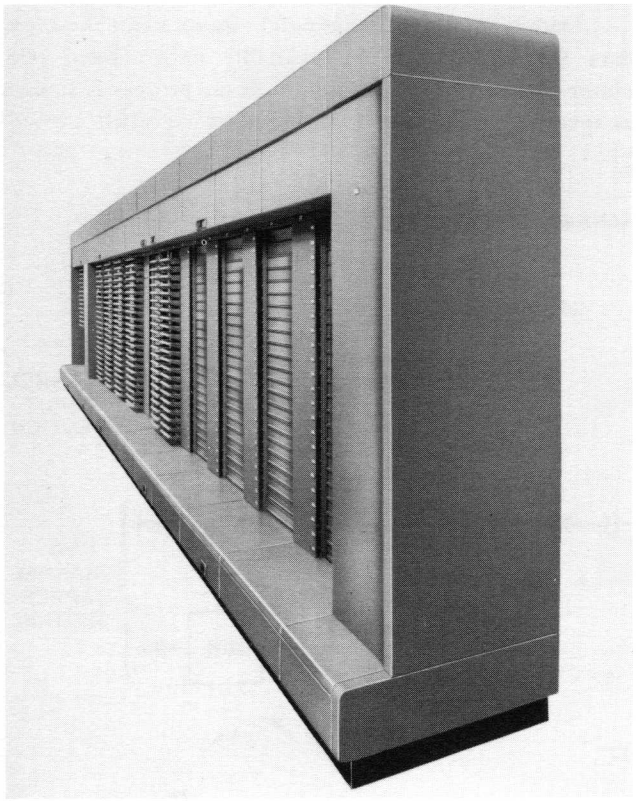


Figure 4–2. GFI Unit 34

Figure 4–3. GFI Mapper Console

1.5 DRUM WORD LAYOUT AND DRUM ENTRY

One of the functions of the GFI element is to compose the bits of the GFI message into a form acceptable to the GFI field of the LOG drum for use in the computer. A GFI drum word or register layout is depicted in figure 4–4. The customary 32 bits contained in the conventional drum word are not all used for a GFI message. In this case, only 26 of the 32 bits contain information. The range and azimuth information is contained in bits LS through L7 and RS through R7, respectively. In each case, the 8 bits allow 256 (2 to the 8th power) combinations of 1's and 0's. Bits L8, L9, L15, R8, R9, and R10 are not used in a GFI message. The relative time information, contained in bits L10 through L14, is inserted into each message by the Drum System (within the nearest $\frac{1}{4}$ second of its actual writing).

Bits R11 to R15 identify the source of the GFI message. An address number or code is written into each message by the common equipment in the GFI element to indicate at which GFI site the radar message originated.

The GFI field of the LOG drum is written-on by the status method. "Status method" means that the data

is written in the first available empty register on the GFI drum. An empty register generates a drum-demand pulse as it moves into writing position, and the message is then applied in parallel form to the drum for subsequent transfer to the computer.

1.6 GENERAL FUNCTIONAL DESCRIPTION

A diagram showing the flow of information through the GFI element is presented in figure 4–5. The dotted line through the diagram divides the channel equipment from the common equipment. The GFI element is made up of an input switching section, 18 mapper consoles, 18 channel input sections (only 1 mapper console and 1 channel input section are shown), a duplex switching section, and a duplexed common section. The various sections are discussed briefly below and in detail in the following chapters.

1.6.1 Input Switching Section

The data from each GFI site is applied to the corresponding channel equipment through the input switching section. The section also contains relays controlled by switches on the simplex maintenance console which will allow signals from the test pattern generator to be substituted for the telephone-line input for a test procedure.

The spare channels (2) can be substituted for any of the 16 channels by the use of relays in the spare channel switching section. The site identity relays also switch the site identity drive of the spare channel to provide the correct site identification data for the site using the spare channel.

1.6.2 Channel Equipment

Each of the 18 GFI channels (16 active and 2 spare) contains the three channel-equipment sections that are shown for one channel in figure 4–5. Data signals from the telephone terminal equipment or test signals from the test pattern generator (TPG) are applied to the channel through input switching. Timing (OD) pulses and drum-demand (DD) pulses are applied through duplex switching.

The 1,600-cps outputs from the telephone terminal equipment are converted into appropriate levels and pulses by the DCR circuit. The range, azimuth, and target signals are then processed by the mapper and counter sections to form a binary word acceptable to the GFI field of the LOG drum. Upon receipt of a filtered target pulse, the accumulated data is transferred to the tape core registers of the counter section. Receipt of a DD pulse from the Drum System causes readout of the tape core registers transmitting the target information to the LOG drum via the common sections. The site-identity-drive (write) signal is transferred through switching to the common section, causing the addition of site identity to the drum word. The data-available pulse originating in the counter section is sent through duplex switching and the common section to the Drum System to inform the LOG drum that a message is being transferred.

1.6.3 Duplex Switching Section

The duplex switching section receives the filtered target information in drum-word form from the channel equipments for application to the Drum System of computer A or computer B. This section receives the drum-timing signals from computers A and B and supplies them to the proper channel equipments to synchronize channel operation with that of the Drum System. The switches and circuits in the duplex switching section control the connection to the Drum Systems of the two computers, so that active channels are connected to the Drum System of the active computer and standby channels are connected to the Drum System of the standby computer.

1.6.4 Common Equipment

The common equipment switches and provides driving circuitry used in the GFI element, adds site identity information to the GFI message, and converts the GFI message into the standard-pulse form required by the Drum System. The common equipment circuitry is used by all channels of the GFI channel equipment section. The common equipment section is duplexed with common equipment A sending data to computer A and common equipment B sending data to computer B via the associated A or B drum field. Duplex switching controls the application of site-identity-drive, data-available pulses, and range and azimuth data from active channel equipments to the active common equipment (A or B) and connects these inputs from standby channels to the standby common equipment.

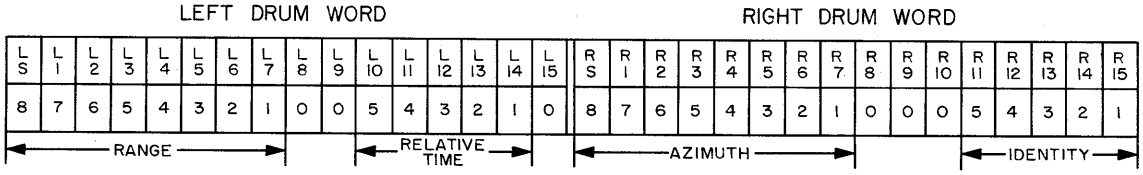


Figure 4–4. GFI Drum Word Layout

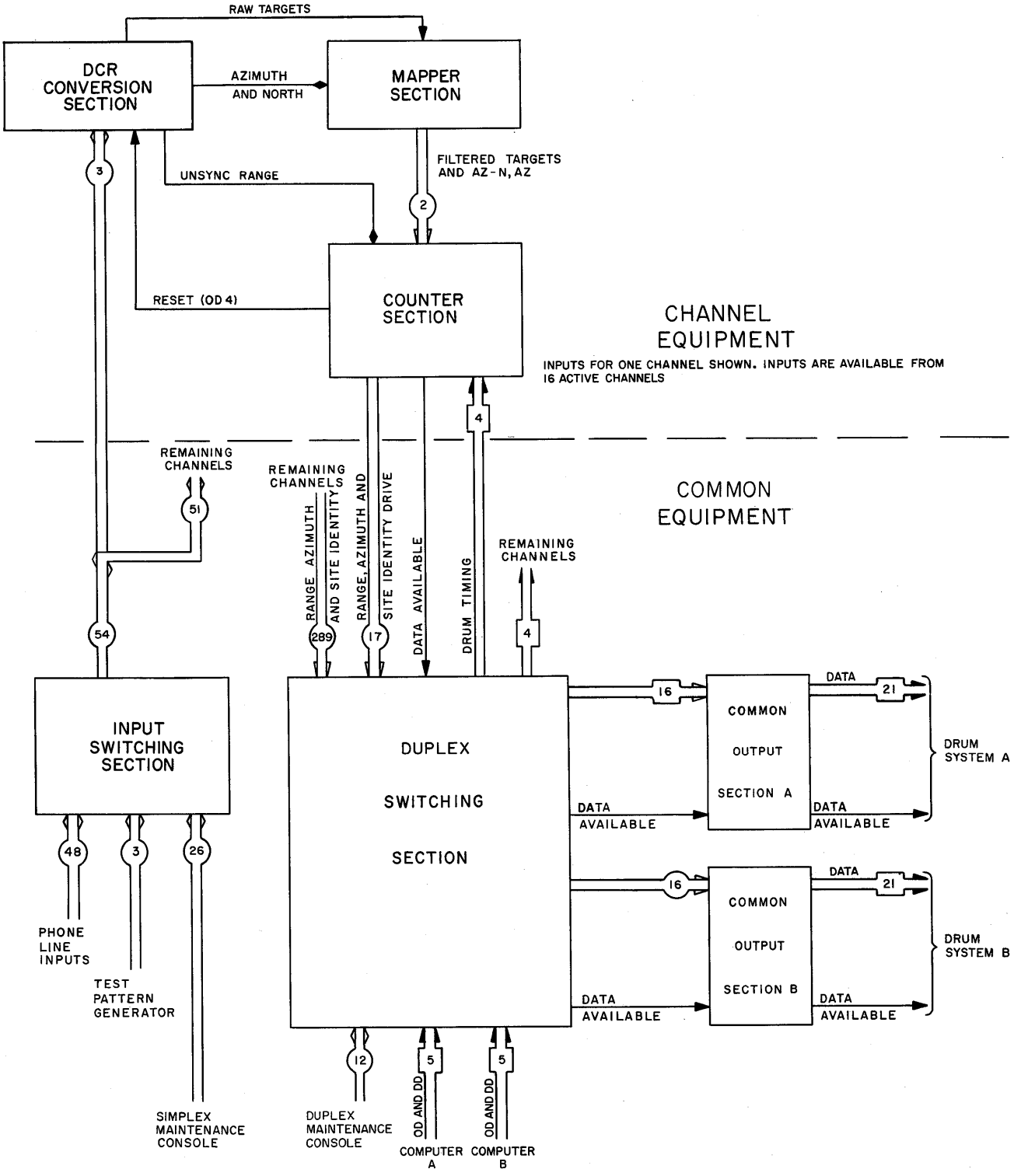


Figure 4–5. GFI Element, Simplified Block Diagram

1.6.5 GFI Mapper

The GFI mapper functions to filter out undesirable target information collected at the radar site. By means of a target selection method, the undesired target signals are suppressed, and only pertinent data is permitted to reach the Central Computer System.

The mapper console contains circuits, which synchronize the operation of the mapper with the operation of the GFI site radar. Visual and audible alarms inform the operator when this synchronism is lost and cathode-ray tubes (part of the mapper console) display the radar data. A mapping technique is used to remove target information caused by ground, sea, or cloud returns, stray noise, or deliberate jamming.

Synchronization of the cathode-ray tube (CRT) deflection yoke in the mapper console with respect to the radar antenna is necessary for accurate displays. To establish this synchronism, the azimuth pulses in the radar data are used to control the speed of a synchronous motor which drives the CRT yoke. To ensure proper orientation of the deflection yoke with respect to the radar scanning, a yoke-speed changing mechanism, consisting of a series of brakes and differential gears, produces a change in yoke speed without a corresponding change in the speed of the azimuth drive motor.

The audible-and-visible-alarm system signals the mapper console operator when the mapper is operating asynchronously. Synchronism may be lost because of the arrival of spurious azimuth pulses (the azimuth motor operating on a harmonic of the azimuth frequency), the absence of azimuth pulses, or azimuth jitter.

1.7 SIMPLEX MAINTENANCE CONSOLE GFI CONTROL PANELS

1.7.1 General

There are 18 GFI control panels (one per channel) location in the upper sections of modules E, F, G, and H of the simplex maintenance console. The odd and odd-spare panels (1, 3, 5, . . . 17) contain alarm, power control, data circuit, and neon indicator sections. The even and even-spare panels (2, 4, 6, . . . 18) are similar, except that the power-control section is not used. In addition, the odd-spare panel mounts a channel selector section which is used for spare channel selection. The three types of panels are illustrated in figure 4–6.

1.7.2 Function of GFI Control Panel Switches

The unit status switch, in the power control section of each odd panel, controls the status (ACTIVE, STANDBY, etc.) of the related channel and the status of the next higher even channel (unit status switch on the first panel controls the status of channels 1 and 2). With the switch set to ACTIVE, the two channels which it controls are connected to the active computer. Only telephone-line data can be processed with the switch set to the ACTIVE position. With the switch set to STANDBY (or STANDBY MC), the two channels are connected to the standby computer and either telephone-line or test data can be processed.

There are three switches in the data circuit section of the panel: the source switch, TEST switch, and the EXCESS TARGET INHIBIT switch. The source switch is used to select the origin of the data to be processed by the channel. With the switch set to DATA CIRCUIT, the channel receives information from GFI radar sites over telephone-line facilities. With the switch set to TEST, the channel receives data from the TPG, permitting controlled testing of the channel operations in maintenance procedures. To prevent test data from entering the active computer, interlock circuitry permits test data to be selected only when the channel is in the standby status.

The EXCESS TARGET switch, when set to INHIBIT, prevents the mapper from initiating an alarm, regardless of the number of alarm conditions which arise from excess targets. The TEST switch is used to test the ability of the channel to halt readout operations if the channel-ready flip-flop produces simultaneous up-levels on both output lines. The switch is normally in the off position.

The CHANNEL SELECTOR switch (odd-spare channel control panel) electrically substitutes spare channels 17 and 18 for any other 2-channel group. Channel 17 substitutes for the odd channel and channel 18 substitutes for the even channel.

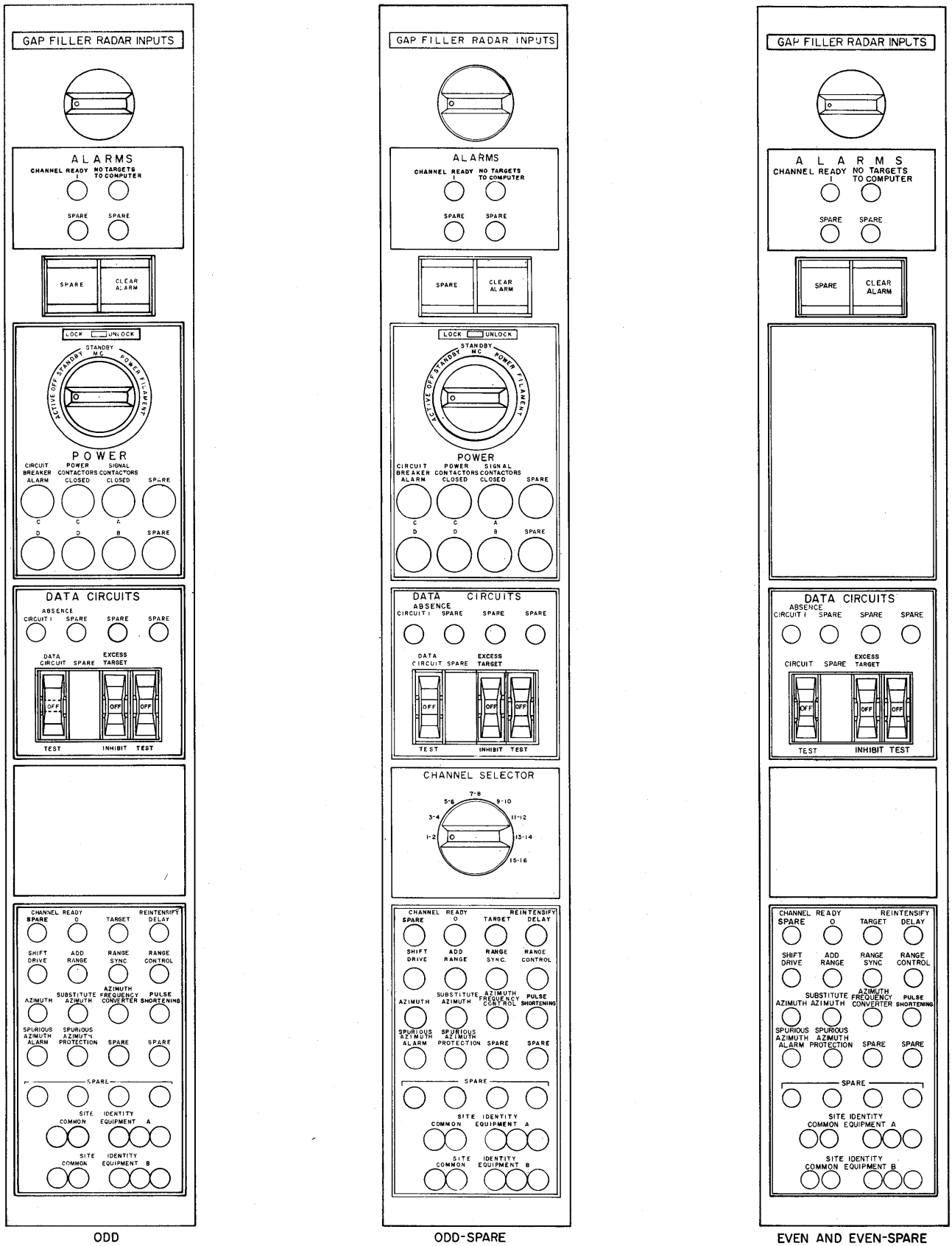


Figure 4–6. Gap-Filler Input Control Panels

CHAPTER 2
INPUT SWITCHING

2.1 GENERAL

The input switching section receives GFI radar data from telephone terminal equipment and test data from the GFI section of the TPG. The function of the input switching section is the selection of either the telephone-line data or test data for each channel. As a second function, the input switching section controls the substitution of the spare channels for the regular channels. The switches controlling the input switching circuitry are located on the GFI control panels of the simplex maintenance consoie.

2.1.1 Input Data Switching

The relationship of the unit status switch and the two associated source switches is shown in figure 4–7. In conjunction with the unit status switch, the source switch determines which type of data (test or phone line) will be applied to the two channel input sections. Placing the source switch for channel 1 in the DATA position causes relay 34AM(K2) to be energized, regardless of the position of the unit status switch. Phone-line data is thereby applied to the channel 1 DCR's. A similar circuit exists for channel 2 under control of relay 34AM(K5).

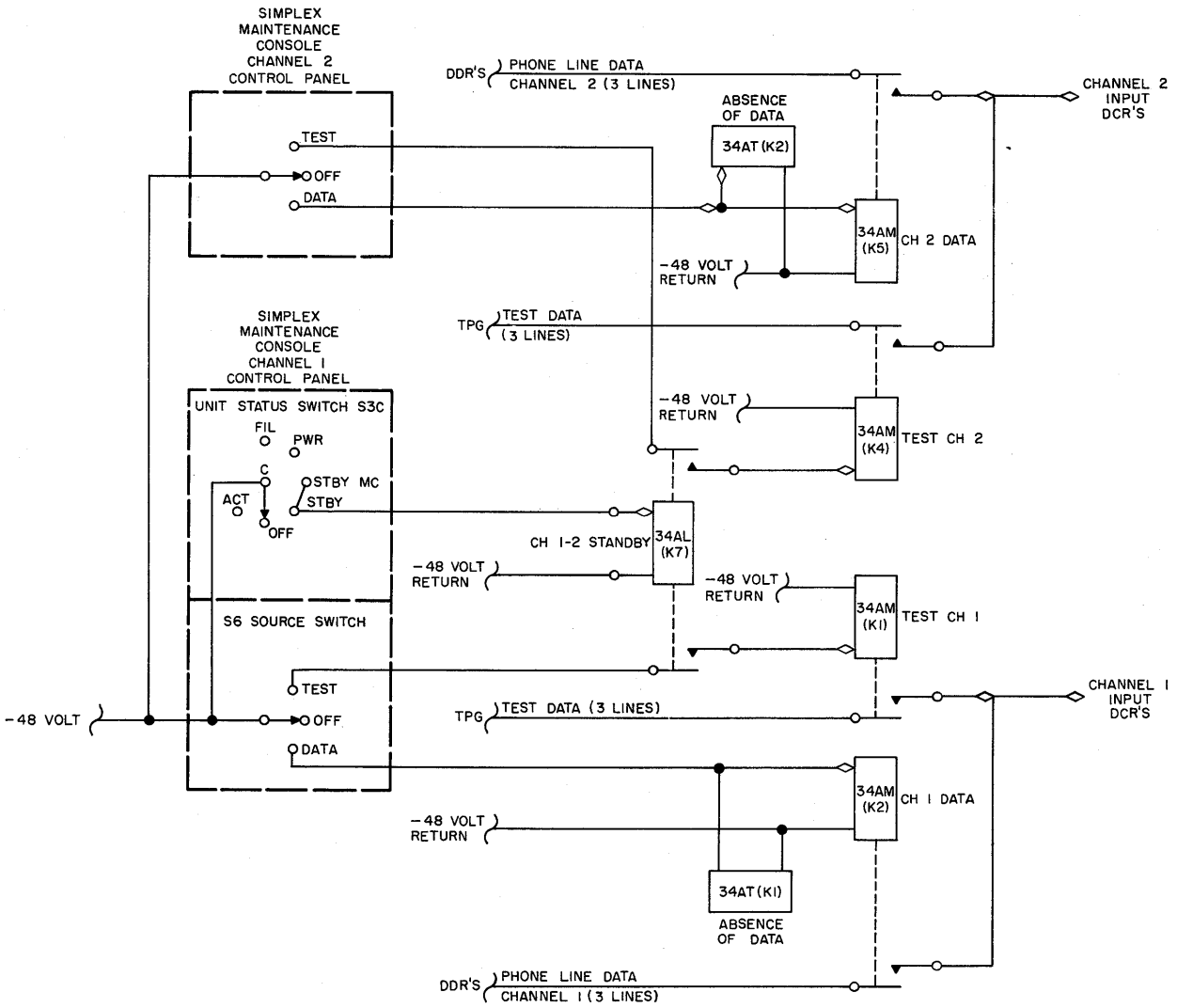
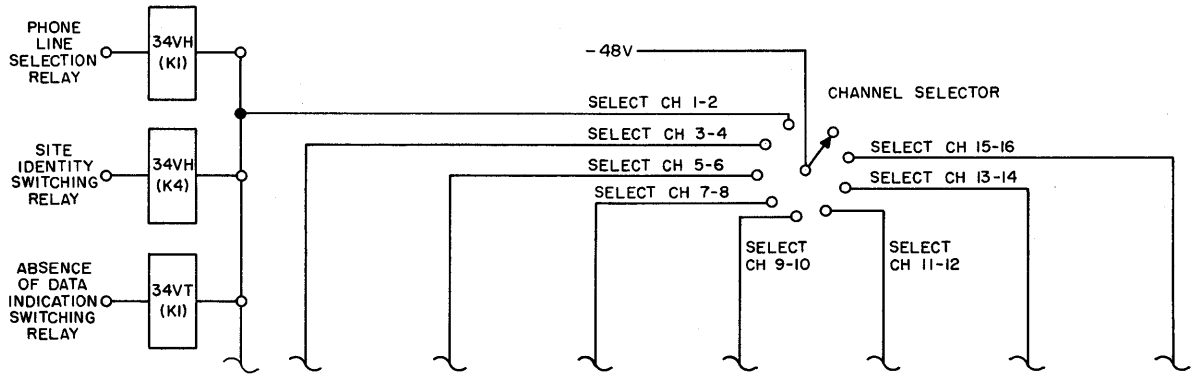
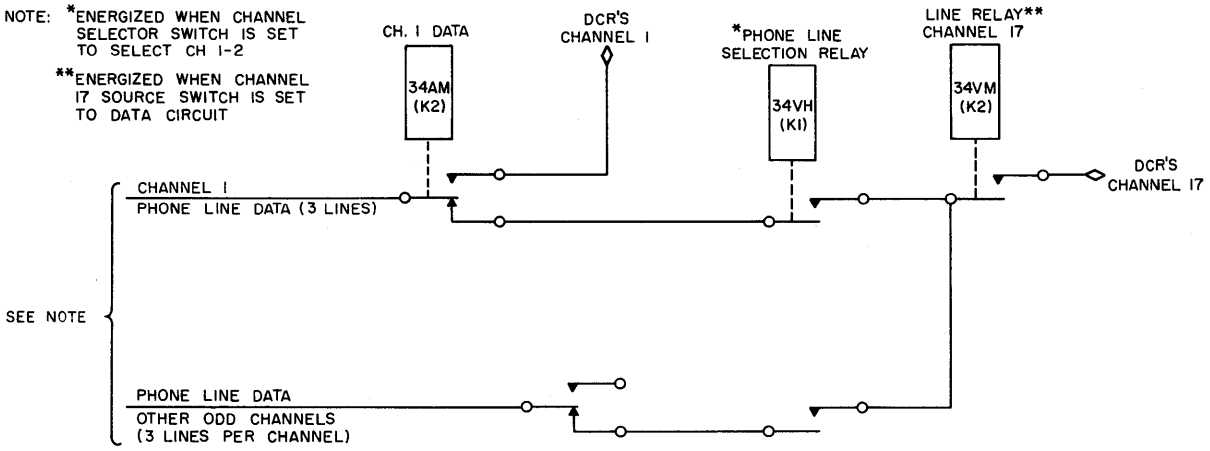


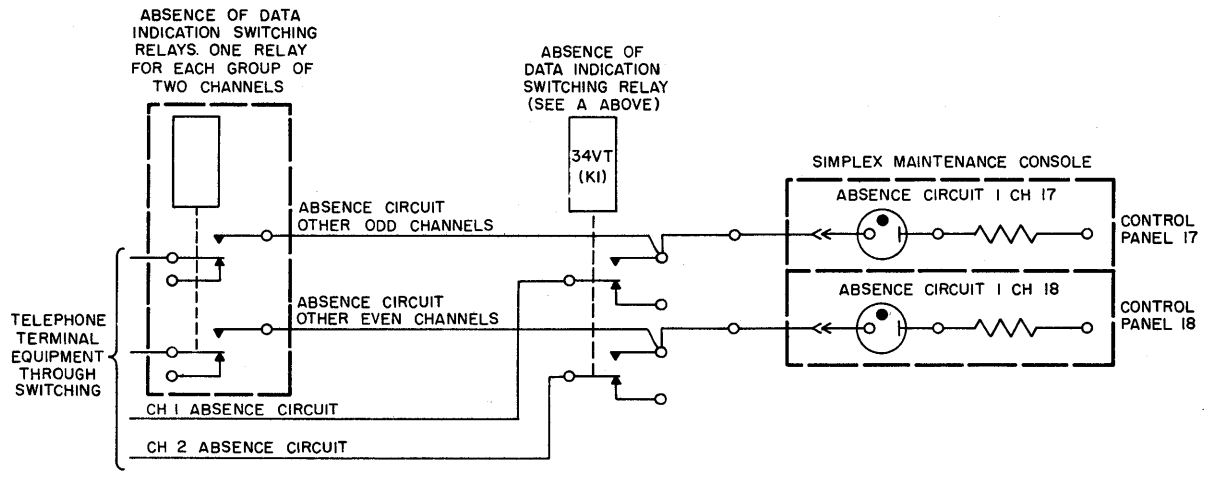
Figure 4–7. Input Data Switching, Simplified Logic Diagram



A. OPERATION OF CHANNEL SELECTOR SWITCH, SPARE CHANNEL



B. TELEPHONE LINE DATA SWITCHING, SPARE CHANNEL



C. PHONE LINE INDICATION SWITCHING

Figure 4–8. Spare Channel Switching

When the unit status switch is placed in the STANDBY, or STANDBY MC position, —48V is provided to energize relays 34AM(K1) and 34AM(K4). When the source switch for channel 1 is placed in the TEST position, relay 34AM(K1) is energized through the normally open contacts of relay 34AL(K7), applying test signals to channel 1 input section. The purpose of this interlock is to prevent test signals from being applied to an active channel and thus read into the Central Computer. Channel 2 test data is applied through the normally open contacts of relay 34AM(K4), which is also energized under control of relay 34AL (K7). The contacts of 34AT(K1) connect the absence-of-data neon (channel 1 control panel) to telephone terminal equipment. An absence of data on the telephone equipment is indicated when the neon is lit.

2.1.2 Spare Channel Switching

Spare channel switching is the operation of electrically substituting the two spare channels for two regular channels. It is accomplished by setting the CHANNEL SELECTOR switch (on the odd-spare control panel) to the numbers of the channel group to be replaced. Three functions are thereby performed:

a. Phone-line data of the replaced channels is directed to the spare channels.
b. The operations of the ABSENCE CIRCUIT neons on the replaced channels are replaced by the operation of the corresponding neons on the spare control panels.
c. The site identity driving signal generated in the spare channel is switched to drive the site cans of the replaced channel, to associate the data processed by the spare channel with the site normally related to the replaced channel.

Functions a and b are discussed below. Function c involving both spare channel switching and duplex switching is discussed in Chapter 4.

Assume that channels 1 and 2 have been selected for replacment by the spare channels by the CHANNEL SELECTOR switch (fig. 4–8). Relays 34VH(K1), 34VH(K4), and 34VT(K1) will be energized. Channel 1 telephone-line data is transmitted through the normally closed contacts of the channel 1 data relay and the normally open contacts of the telephone-line selection relay 34VH(K1). With the channel 17 line relay energized, the channel 1 telephone-line data is thereby applied to channel 17. Similar circuitry applies other odd channel telephone-line data to channel 17 and other even telephone-line data to channel 18 under control of the CHANNEL SELECTOR switch.

The ABSENCE CIRCUIT 1 neon (GFI channel control panels) is lit when telephone terminal equipment for that channel is not receiving data. When a spare channel is selected, the contacts of relay 34VT (K1) cause the ABSENCE CIRCUIT 1 neon on the spare panel to assume the function of the corresponding neon of the replaced channel.

CHAPTER 3
GFI CHANNEL INPUT

3.1 INTRODUCTION

Each GFI channel input section (fig. 4–9) receives telephone-line data from a radar site or test data from the TPG, eliminates undesired target returns, and converts the target information into a form acceptable to the Drum and Central Computer Systems. When the Drum System requests information, the target data is transferred to the GFI drum field. The operations of the channel and the transfer to the drum field are synchronized by drum-originated timing pulses.

The sinusoidal input data is converted into standard levels and Drum System synchronized pulses for use in

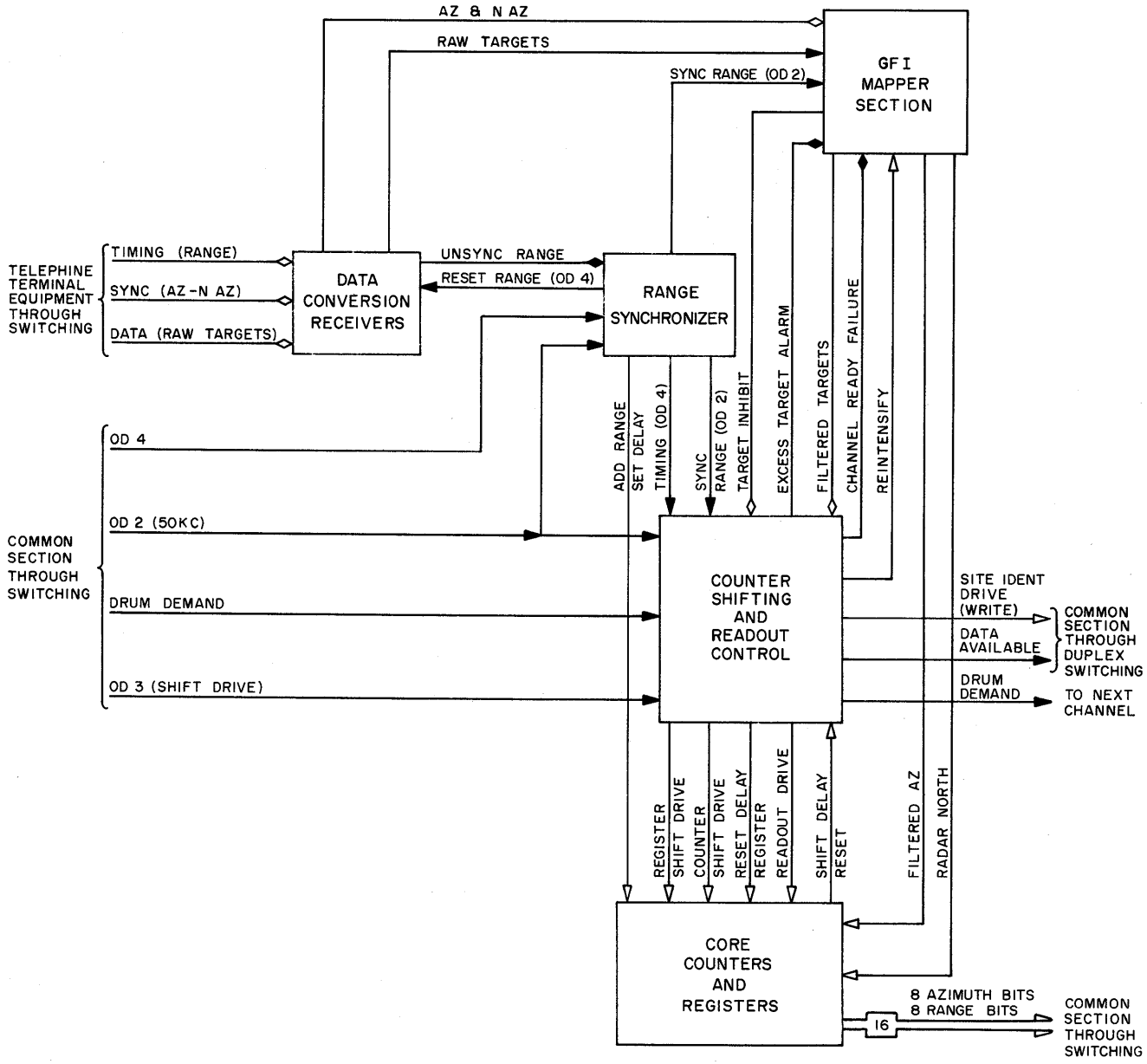


Figure 4–9. GFI Channel, Simplified Block Diagram

other circuits of the channel equipment. The range and azimuth pulses are used to accumulate a binary representation of the polar co-ordinates of a target. Upon receipt of a filtered-target pulse from the mapper, the accumulated information contained in the range and azimuth binary counters is transferred to the respective tape core registers. When a DD pulse is received (indicating an available slot on the GFI drum field), the contents of the registers are transferred to the GFI drum field.

Operations of the channel input section are synchronized by OD pulses originating in the Drum System, specifically for use by the GFI element. The OD drum timing pulses are a series of four standard pulses, OD 1, OD 2, OD 3, and OD 4, equally spaced at 2.5 μsec. Recycling takes place without delay, so that OD 1 occurs 2.5 μsec after OD 4. The OD pulse repetition rate is too fast for some circuits of the channel input section; consequently, the OD 2 pulse which is supplied has a repetition rate of 20 μsec. The following timing pulses are furnished by the related common section through duplex switching and are discussed in Chapter 5.

a. OD 2 (50 kc)
b. OD 3
c. OD 4

3.2 DATA CONVERSION RECEIVER CIRCUIT

The range, azimuth, and target sinusoidal inputs are sent to the GFI channel on separate lines. Each of the three inputs is applied to a DCR by the telephone-line input switching circuits. Figure 4–10 is a simplified logic diagram of the DCR circuit. Figure 4–11 is the timing chart.

The DCR circuit converts the sinusoidal range input into a non-standard pulse for each range cycle. The azimuth and north-azimuth inputs are converted into a standard level of 200-μsec duration for each azimuth cycle. The sinusoidal target inputs are converted into a standard pulse for each target input.

The range input, which is a continuous sine wave with a frequency of 1,600 cps, is applied to an ADCR. The ADCR produces a negative non-standard pulse for each negative peak of the sinusoidal range input. This negative pulse, having a pulse repetition rate of 1,600 pps, sets a flip-flop. The flip-flop is then cleared by an OD 4 reset pulse from the range synchronizer circuit. The short-duration set output of the flip-flop is a standard level, occurring once for each cycle of the range input. This unsynchronized range pulse is sent to the range synchronizer circuit.

The north-azimuth signals consists of two consecutive cycles of 1,600-cps sine waves; the azimuth signals consist of single cycles of 1,600-cps sine wave. These azimuth inputs are applied to a BDCR which produces a standard level output of fixed duration (200 μsec) for each negative peak of the sinusoidal input. The north-azimuth input generates two 200-μsec standard levels spaced 1/1,600 second apart. The azimuth output is sent to the azimuth and north protection circuit and to the start and alarm circuit in the mapper section.

The target signal consists of a single cycle of a 1,600-cps sine wave. This input is applied to a BDCR which produces a 200-μsec standard level for each negative peak of a target-input signal. The output of the BDCR conditions a gate to allow the passage of an OD 4 pulse from the range-synchronizing circuit. A single pulse is sent to the sweep and intensification circuit of the mapper for each target-input signal.

3.3 GFI MAPPER SECTION

The GFI mapper section provides a means of target selection which suppresses undesirable target information and thereby permits only pertinent data to reach the Central Computer. The mapper also furnishes correct azimuth and north-azimuth pulses to other circuits of the channel equipment. The GFI mapper is discussed in detail in Chapter 6 of this part. However, at this point, it is essential to understand the relationship of the mapper section to other channel equipment.

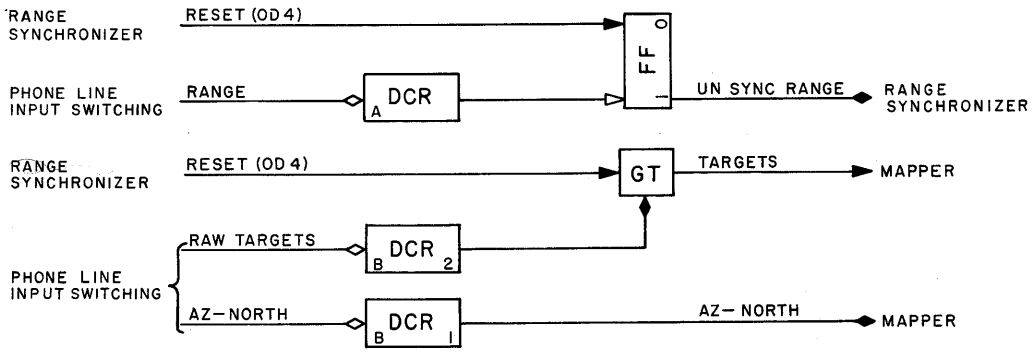


Figure 4–10. GFI Data Conversion Receiver Circuit, Simplified Logic Diagram

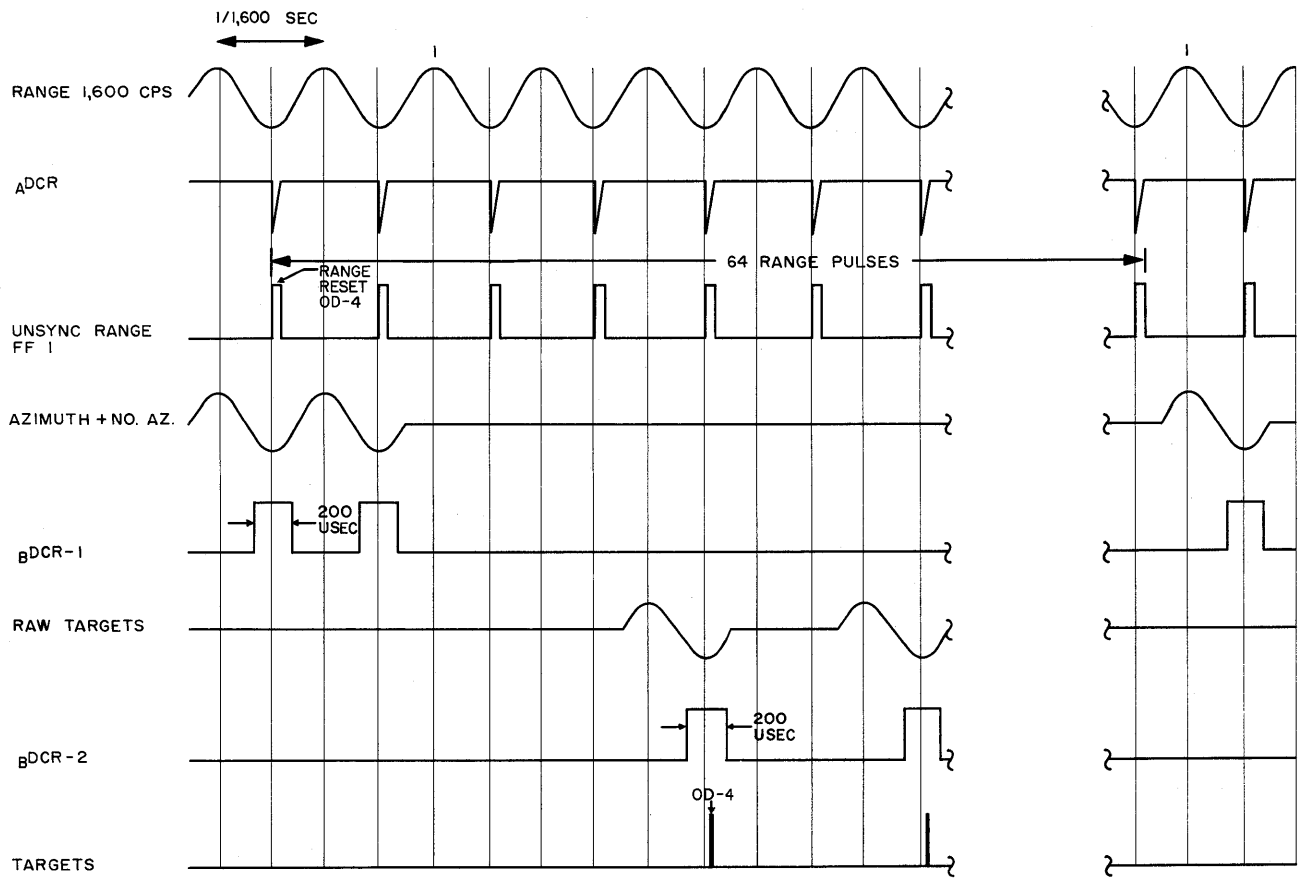


Figure 4–11. GFI Data Conversion Receiver, Timing Chart

The mapper section receives azimuth, north-azimuth, and raw target pulses from the data conversion receivers. Spurious azimuth pulses are inhibited by mapper circuitry from reaching the counter circuits. If the mapper determines that an azimuth pulse is missing, a substitute azimuth pulse is generated and forwarded to the counter circuits. A filtered north azimuth pulse is furnished to the counter circuit as an indication that the radar and mapper CRT have reached the north position. Some areas of the mapper CRT may be masked with a yellow fluid to suppress target indications caused by extraneous objects in the radar sweep. A raw target appearing on an unmasked area of the mapper CRT causes generation of a filtered target pulse which is sent to the counter shifting and readout control circuit to prepare the accumulated information for transfer to the Drum System.

3.4 GFI COUNTER SECTION

3.4.1 General

The function of the GFI counter section is the translation of range and azimuth pulses into a binary representation of the polar co-ordinates of targets. Upon receipt of a filtered target from the mapper section, the accumulated data contained in the range and azimuth counters is inserted in the tape core registers. A DD pulse (indicating an empty drum slot) then causes the contents of the registers to be transferred to the Drum System for eventual transfer to the Central Computer. The azimuth and range data is read out to the Drum System in parallel form.

3.4.2 Range Synchronizer

The range synchronizer circuit (fig. 4–12) receives the unsynchronized range levels from the DCR and generates range-output pulses which are synchronized with the Drum System timing pulses.

The unsynchronized range level from the timing DCR conditions GT's 1 and 4, and the following OD 2 (50 kc) passes GT 1 to set FF 1, conditioning gates 2 and 3. Five μsec after the OD 2 pulse, an OD 4 pulse passes conditioned GT's 3 and 4. This OD 4 (reset) pulse is sent to the DCR circuit where it performs two functions: it clears the timing flip-flop, thereby removing the unsync range level from the range synchronizer circuit; it supplies the second input to the target gate, furnishing a pulse to the mapper, if a target is present. A second OD 4 pulse is received before the next 50 kc

OD 2. This second OD 4 pulse will pass GT 3, but since GT 5 is still deconditioned and the conditioning level (unsync range) has been removed from GT 4, the circuit does not have an output at this time. Five μsec after the second OD 4 pulse, an OD 2 pulse will pass GT 2 and will set FF 2. The output of GT 2, sync range (OD 2), is also sent to the azimuth protection circuit and to the counter shifting and readout circuit. The next OD 4 is passed by GT's 3 and 5 to clear FF's 1 and 2. The output of GT 5 is also sent to the counter shifting and readout control to clear the channel ready flip-flop if a filtered target level is received from the mapper.

3.4.3 Counter Shifting and Readout Control

The counter-shifting and readout control circuit generates both the counter-shift-drive pulses necessary to the operation of the azimuth and range counters and generates the pulses that cause the range and azimuth counts, at the time of a filtered target, to be transferred to their respective registers. Finally, the counter-shifting and readout control circuit produces the readout pulse, which transfers the contents of the range and azimuth registers to the Drum System when an empty drum slot is available. Figure 4–13 is a simplified logic diagram of the counter-shifting and readout control circuit, and figure 4–14 shows the timing.

3.4.3.1 Generation of Counter-Shift-Drive Pulses

The range and azimuth core counters have the capacity to count the number of range and azimuth signals received. The range counter receives successive range indications from the range synchronizer (add range output), which change the count by one unit. The counting technique employed (explained in detail in 3-3-0, *Special Circuits for AN/FSQ-7 Combat Direction Central and AN/FSQ-8 Combat Control Central*) requires that the range counter be shifted nine times each time a single range bit is added to the count. The azimuth counter (identical with the range counter, except that it is primed by the azimuth output of the mapper section) also requires nine shifts for each addition of azimuth. The counter-shifting and readout circuit generates nine shift pulses after each sync-range pulse is received and applies these shift pulses to the range and azimuth counters. The range counter changes its count, therefore, each time the series of nine pulses is applied. The azimuth counter, however, does not receive an add-azimuth signal every time it is shifted nine times (since a single-azimuth signal appears once for every 64 range pulses). The application of the nine shift pulses, without an add-azimuth signal, does not change the binary indication in the azimuth counter.

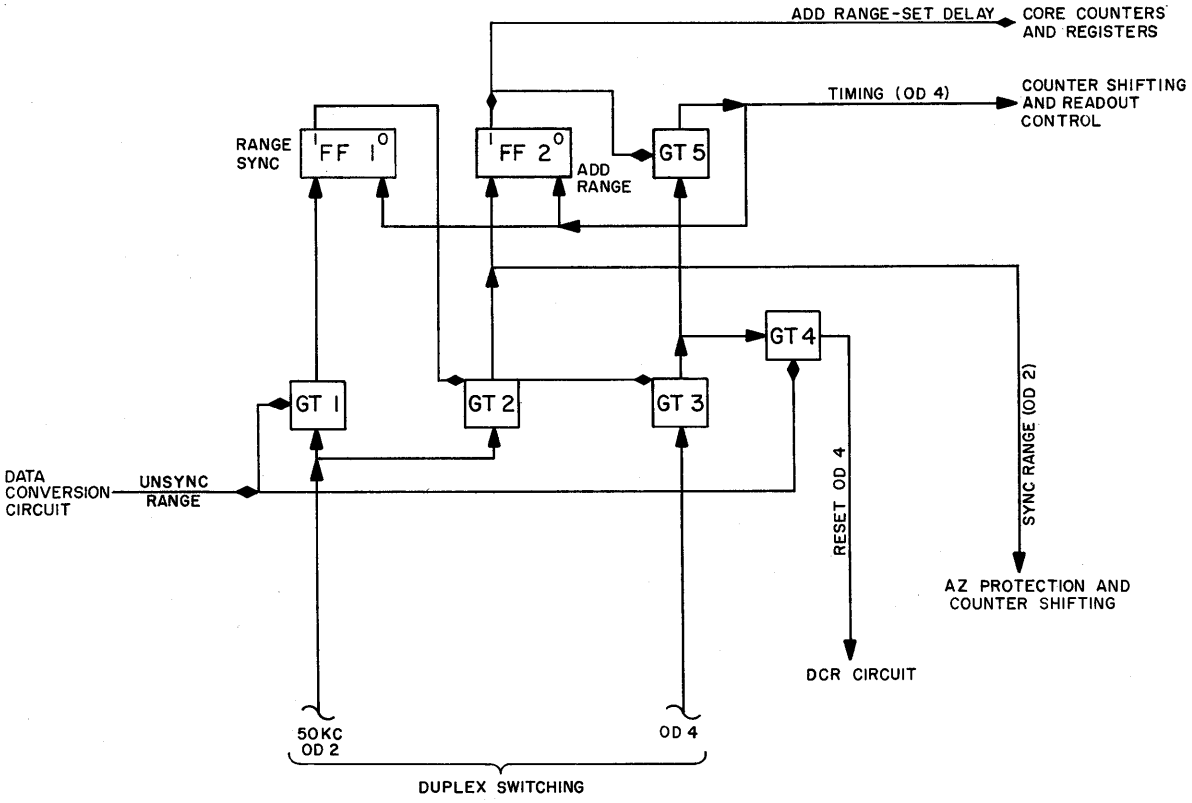


Figure 4–12. GFI Range Synchronizer, Simplified Logic Diagram

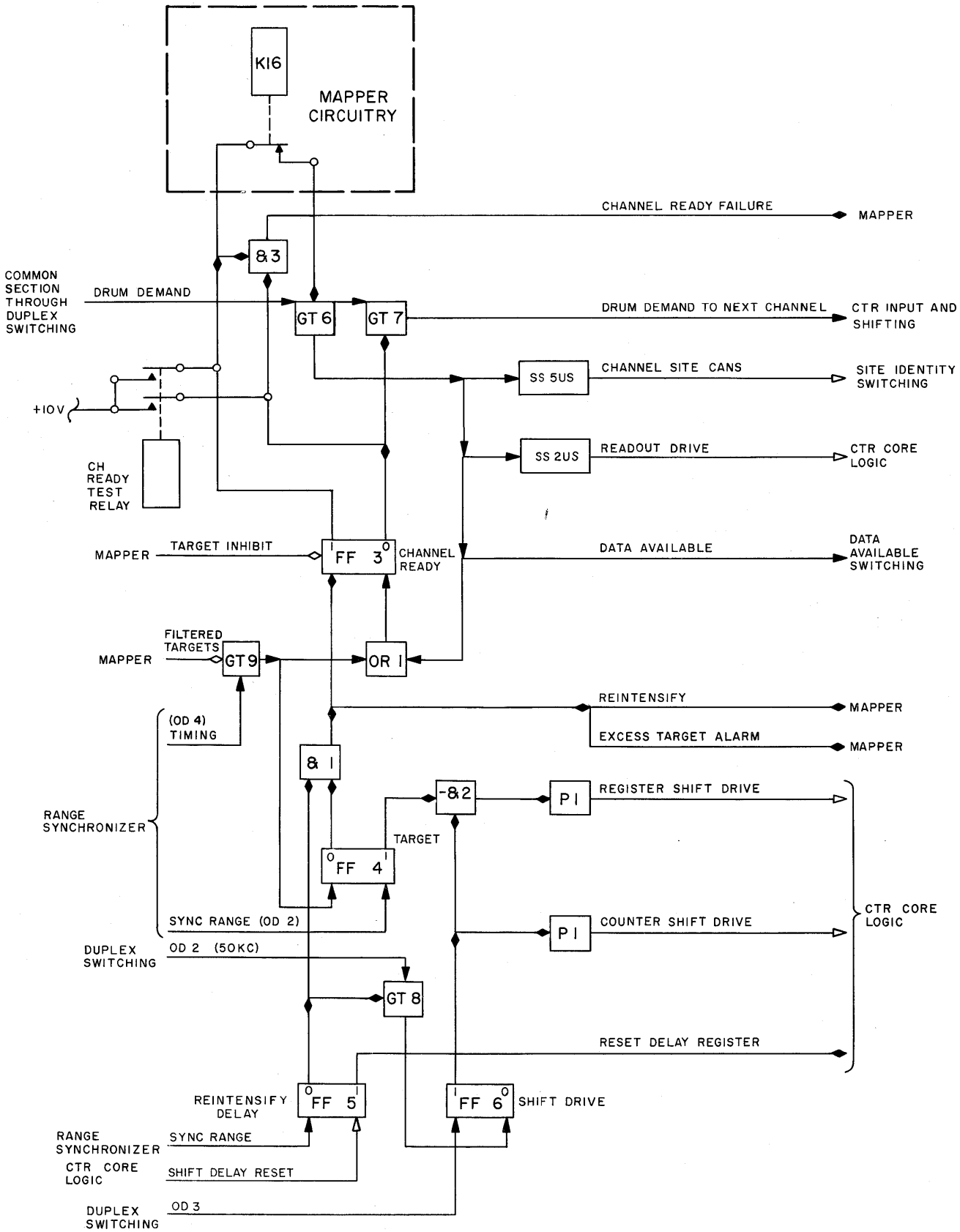


Figure 4–13. Counter-Shifting and Readout Control, Simplified Logic Diagram

The nine shift pulses, generated after each sync-range pulse is received, are also applied to a 9-core delay register which terminates the shift pulses after nine shifts have taken place. The delay register (described in 3.4.4) consists of nine core shifts. The add-range set-delay output of the range synchronizer inserts a 1 in the first core of the delay register when a range signal is received. Each shift pulse moves the 1 to its adjacent core. On the ninth shift, the 1 is transferred from the ninth core to the counter-shifting and readout circuit, where it terminates the generation of additional counter-shift pulses.

A sync-range (OD 2) pulse from the range synchronizer sets FF 4 and clears FF 5. Flip-flop 6 is now cleared by OD 2 (50-kc rate) pulses from GT 8 and is set 2.5 μsec later by continuous OD 3 pulses. The set output of FF 6 is down for 2.5 μsec (OD 2 to OD 3). The set output of FF 6 is applied to a power inverter (PI), which converts each of the 2.5-μsec negative pulses into a positive pulse. The output of the PI is the counter-shift-drive pulse; it is applied to the core shift drivers (CSD's) for the range counter, azimuth counter, and delay register. After nine of these counter-shift pulses, the delay register produces an output which sets FF 5. The clear output of FF 5 is now a 0, which deconditions GT 8, preventing additional OD 2 pulses from passing to FF 6 and thereby terminating the counter-shift-drive pulses.

The set output of FF 5 (caused by delay output) resets the cores in the delay register to 0.

The sync-range pulse (a single OD 2 pulse for each range signal input) is applied to the set input of FF 4. The set output level of FF 4 is applied to a negative AND circuit (—AND 2), which prevents a negative output. A negative AND circuit is the same as an OR circuit; it has a 0 output only when all inputs are 0.

3.4.3.2 Generation of Register-Shift-Drive Pulses

A filtered-target level from the mapper section conditions GT 9 when a filtered target appears. A timing OD 4 pulse passes through conditioned GT 9 to clear FF's 3 and 4. Flip-flops 3 and 4 are cleared 5 μsec after FF 5 but prior to the actual generation of the counter-shift-drive pulses by FF 6. Flip-flop 4, being cleared, has a 0 at its set output to —AND 2. The —AND 2 circuit also receives the set output of FF 6, which is a series of nine negative counter-shift-drive pulses. The two inputs to —AND 2 are —30V whenever a counter-shift-drive pulse is generated. The two —30V inputs produce a —30V output, which is applied to a PI causing a series of nine pulses which are sent to the counter-core logic as register-shift-drive pulses. The register-shift-drive pulses occur in synchronism with the counter-shift-drive pulses whenever a filtered target appears.

3.4.3.3 Generation of Readout Pulse

When a filtered-target level appears, an OD 4 pulse passes GT 9 and clears FF 4. Flip-flop 5 has been cleared by the previous sync-range (OD 2) pulse. The cleared outputs of FF's 4 and 5 are applied to AND 1. The up-level output of AND 1 is used to reintensify

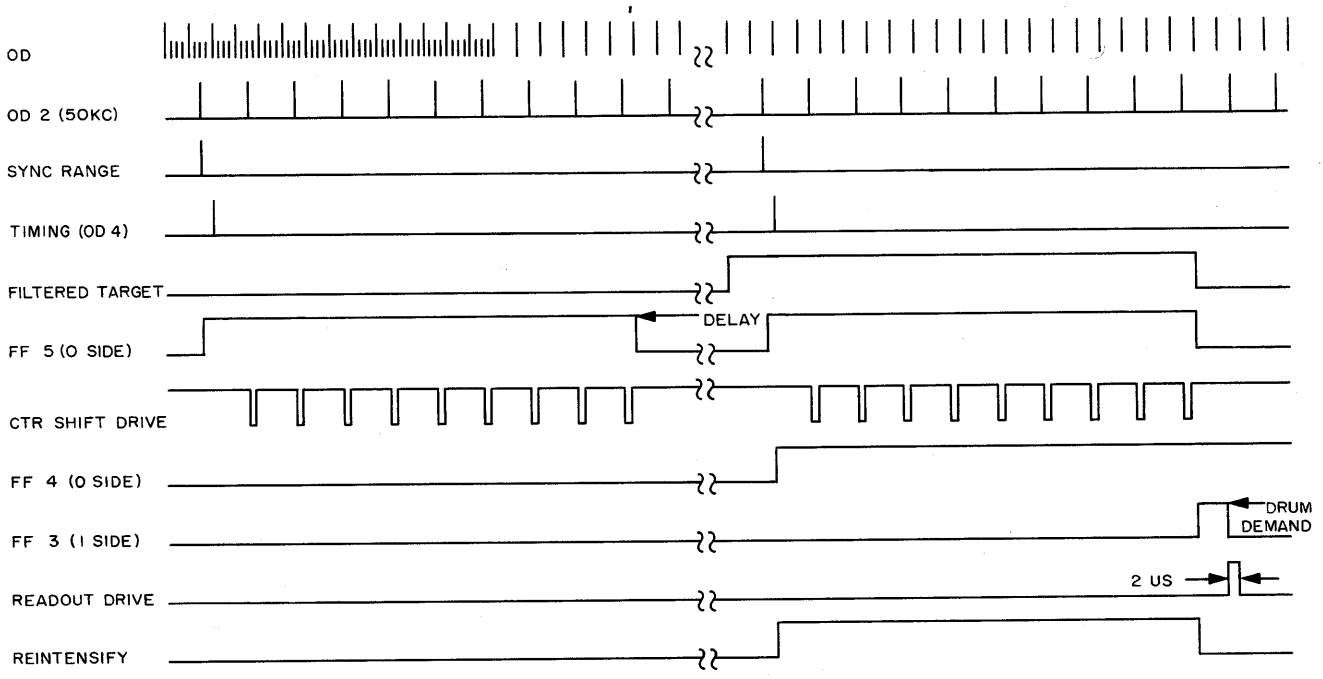


Figure 4—14. Counter-Shifting and Readout Control, Timing Chart

the target indication on the mapper console and is sent to the excess target alarm circuit in the mapper section. The reintensify signal is sent to the mapper, where it illuminates the target indicating that the target is being processed. The filtered-target level remains up for the duration of the reintensify signal. When the reset pulse is received (from the counter core logic), FF 5 is set, removing one of the +10V inputs to AND 1. The output of AND 1 changes from a +10V to a −30V, terminating the reintensify signal. The negative shift in the output of AND 1 also sets FF 3, conditioning GT 6. The next drum-demand (OD 1 + 0.5) pulse that is received passes GT 6 and clears FF 3. The output of GT 6 is sent to the common section as a data-available pulse and is also used to trigger two single-shot multivibrators (SS's). One SS generates a readout-drive (2-μsec duration) pulse, which causes readout of the binary count in the azimuth and range registers to the common section. The other SS produces a 5-μsec signal which is applied to the channel site cans in the common section.

When FF 3 is cleared, GT 7 is conditioned. The DD pulse is then transferred to the next channel, where it initiates readout if a message is ready or is transferred to the following channel, and so on. The first channel that is ready is read out, and the DD pulse is not transferred to any succeeding channels. In this manner, only one channel can be read out when a drum slot is available.

The target inhibit input to FF 3 is produced by the excess target alarm circuit in the mapper section. Whenever a filtered-target pulse appears, a level is sent to the excess target alarm circuit. The excess target alarm circuit is an analog counter that counts the number of target pulses that occur in a certain length of time. When the number of targets occurring threatens to overload the drum, the excess target alarm circuit activates relay K16 which removes the −300V cathode supply from FF 3. This causes FF 3 to remain in the cleared state, preventing readout, regardless of the filtered-target pulses. An excess target alarm is usually caused by the sudden appearance of nonstrategic target indications on the GFI mapper. The operator will map out this useless data and reset the alarm permitting normal operation.

Relay K16 can also be energized if a malfunction causes a simultaneous up-level output from both sides of FF 3. This type of malfunction causes AND 3 to send a channel-ready-failure level to the mapper section, energizing relay K16. Energizing relay K16 causes FF 3 to be cleared and further readout of the channel is prevented. For testing purposes, the channel-ready-test relay can be energized under control of the TEST switch (simplex maintenance console, GFI control panel), to simulate the malfunction of FF 3 by applying +10V to both legs of AND 3 through the normally open contacts of the relay.

3.4.4 Core Counters and Registers

The core counters and registers circuit employs magnetic core devices which function as counters and registers. Figure 4–15 is a simplified logic diagram of the counter core logic circuit.

The circuit consists of an azimuth and a range counter, associated registers, a delay register, and CSD's. The delay register is a 9-core shift register. The first core is set (a 1 inserted) by a range level from the range synchronizer (add-range set-delay output). The counter-shift-drive pulses, from the counter-shifting and readout circuit, are then applied at a 20-μsec repetition rate to the delay register CSD's. The first shift drive (output of CSD) transfers the 1 from the first CS to the second CS. Each succeeding shift drive moves the 1 to the adjacent CS. After nine shifts, the 1 is transferred out of the ninth core as a delay output. This delay output is sent to the counter-shifting and readout circuit, where it terminates the generation of shift-drive pulses and produces a reset-delay pulse which is sent to reset the delay register (make all cores 0). The delay register, therefore, permits nine shift-drive pulses to be generated for each range signal input.

The azimuth and range counters are physically identical; both have the capacity to count up to eight bits of binary data. They both are shifted by the same pulses (a series of nine shifts following each range pulse), and both read out their contents into identical registers when a filtered-target pulse appears. The range counter contains the number of range signals that have occurred in any one azimuth cycle. The azimuth counter contains the count of the azimuths from north azimuth. A filtered-target pulse causes the contents of these two counters to be inserted into their respective registers. The numbers stored in the registers, therefore, are the polar co-ordinates of a particular target. The indication in the azimuth register represents the number of azimuths past north azimuth, while the range register contains the range to the target. When an empty drum slot becomes available, the eight bits contained in each register are read out in parallel (all 16 bits at once) and transferred through the common section to the Drum System.

The two counters use the subtractive or count-down method of counting; that is, initially, the counter is reset to contain all 1's, and each pulse added to the counter is subtracted from the previous contents. The counter, therefore, is said to contain the 1's complement of the count (a 1 representing a binary 0 and a 0 representing a binary 1). These complements of the count are read into the registers when a target appears.

However, the readout windings of the register cores are reversed, so that a 1 core output becomes a 0, and a 0 core output becomes a 1. The register outputs to the Drum System are therefore the true binary counts.

The azimuth counter is reset by the radar-north level from the mapper; it then counts each succeeding azimuth level. The range counter is reset by each azimuth level and then counts the succeeding range levels.

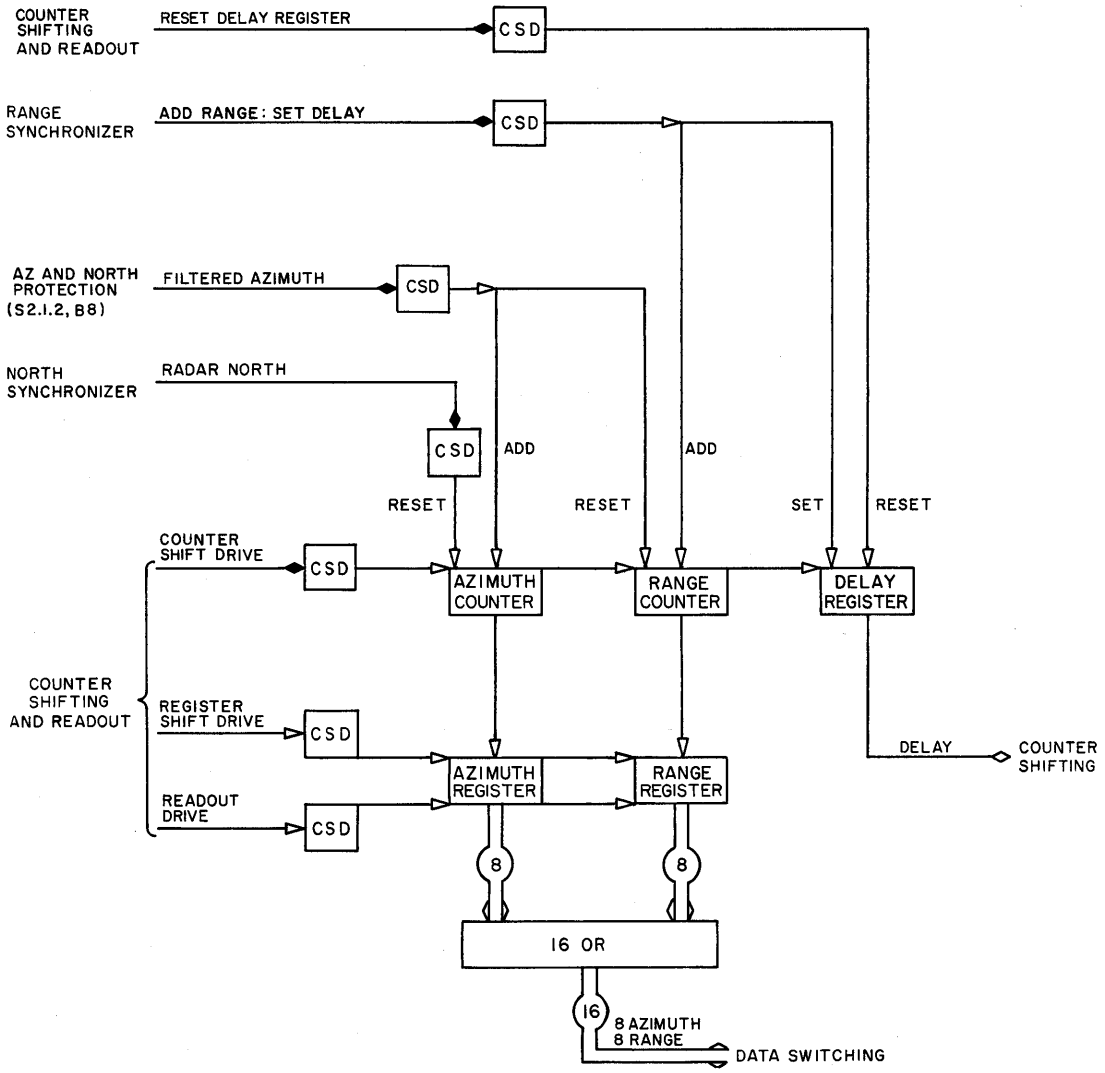


Figure 4–15. Core Counters and Registers, Simplified Logic Diagram

CHAPTER 4
DUPLEX SWITCHING

4.1 GENERAL

Duplex switching associates the operation of simplex equipment with the proper (A or B) duplex machine. Simplex equipment in the active status is associated with the duplex machine currently in the active status, and simplex equipment in the standby status is associated with the standby duplex machine.

In the GFI element, duplex switching provides the circuitry to accomplish the following functions:

a. Drum demand and data available switching; transfers DD pulses from the proper (A or B) Drum System to the channel input section of the various channels and transfers data-available pulses from the channel section to the proper Drum System.

b. Site identity switching; directs the site identity drive signal from the input section to the proper common section.

c. Site identity switching for spare channels; transfers the site identity drive signal generated in the spare channels to the site identity cans of the channels being replaced.

d. Data switching; directs data from active channels to the active common section and directs data from standby channels to the standby common section.

e. Common timing and pulse distribution; distributes OD timing pulses to the channel input sections.

f. Site neon switching; causes illumination of the proper set of site neon indicators on the channel control panel (simplex maintenance console).

g. Status indication switching; sends status indication to the proper half of the MDI element.

Duplex switching is accomplished through the A and B signal relays associated with each channel. The A or B relays are energized under control of the duplex selection switch on the duplex switching console and the unit status switch on the channel control panel (simplex maintenance console). One set of contacts on the A signal relays is series-connected with the A SIGNAL CONTACTORS CLOSED indicator on the channel control panel, so that failure of one relay to energize will cause the indicator to remain unlit. A similar arrangement is used for the B signal relays and the B SIGNAL CONTACTORS CLOSED indicator.

4.2 DRUM DEMAND AND DATA AVAILABLE SWITCHING

The drum-demand and data-available switching receives gated DD pulses from the common timing and pulse distribution circuits and circulates them, in the order of channel priority, through the counter-shifting and readout control circuits. The effect of these pulses is discussed in 3.4.3.3 (Generation of Readout Pulse). When filtered target data is available in a channel (and other conditions are satisfied), a data-available pulse is returned to drum-demand and data-available switching which sends it to a common output section (5.4). Under circumstances preventing the generation of a data-available pulse in a particular channel, the gated DD pulse is passed to the next channel, sensing again for filtered target data.

The circuit for four channels, designated channels 1, 2, 3, and 4, is shown in figure 4–16. Gates 6 and 7, shown in phantom for each channel, are the same as GT's 6 and 7 in figure 4–13. Channels are made active or standby in pairs. The relays accordingly operate in pairs. For example, when relay 34AN(K4) is energized, relay 34AN(K5) is not. Thus, channels 1 and 2 are sensed (for filtered target data) by the gated DD pulses derived from the A Drum System, and a data-available pulse, if produced by either channel, is fed to common output section A. When relay 34AN(K4) is not energized, relay 34AN(K5) is energized; gated DD pulses from the B Drum System sense channels 1 and 2; and a data-available pulse, if produced by either channel, is fed to common output section B. (Whether the K4 or K5 relay is energized is determined by duplex switching and by the position of the unit status switch for the pair of channels.)

Assume that the A machine is active and that channels 1 and 2 are in the active status; 3 and 4 are in the standby status. Relays 34AN(K4) and 34CN(K5) are then energized; 34AN(K5) and 34CN(K4) are unenergized. The gated DD pulse derived from the A Drum System strobes GT 6 and GT 7 of channel 1 through contacts 1a-1c of 34AN(K4). If GT 6 is conditioned (filtered target data available), a data-available pulse from GT 6 passes through contacts 4a-4c of 34AN(K4) to the common output section A. If GT 6 is not conditioned, GT 7 is conditioned (fig. 4–16), and the DD pulse senses channel 2. If GT 6 of that channel is conditioned, a data-available pulse passes through contacts

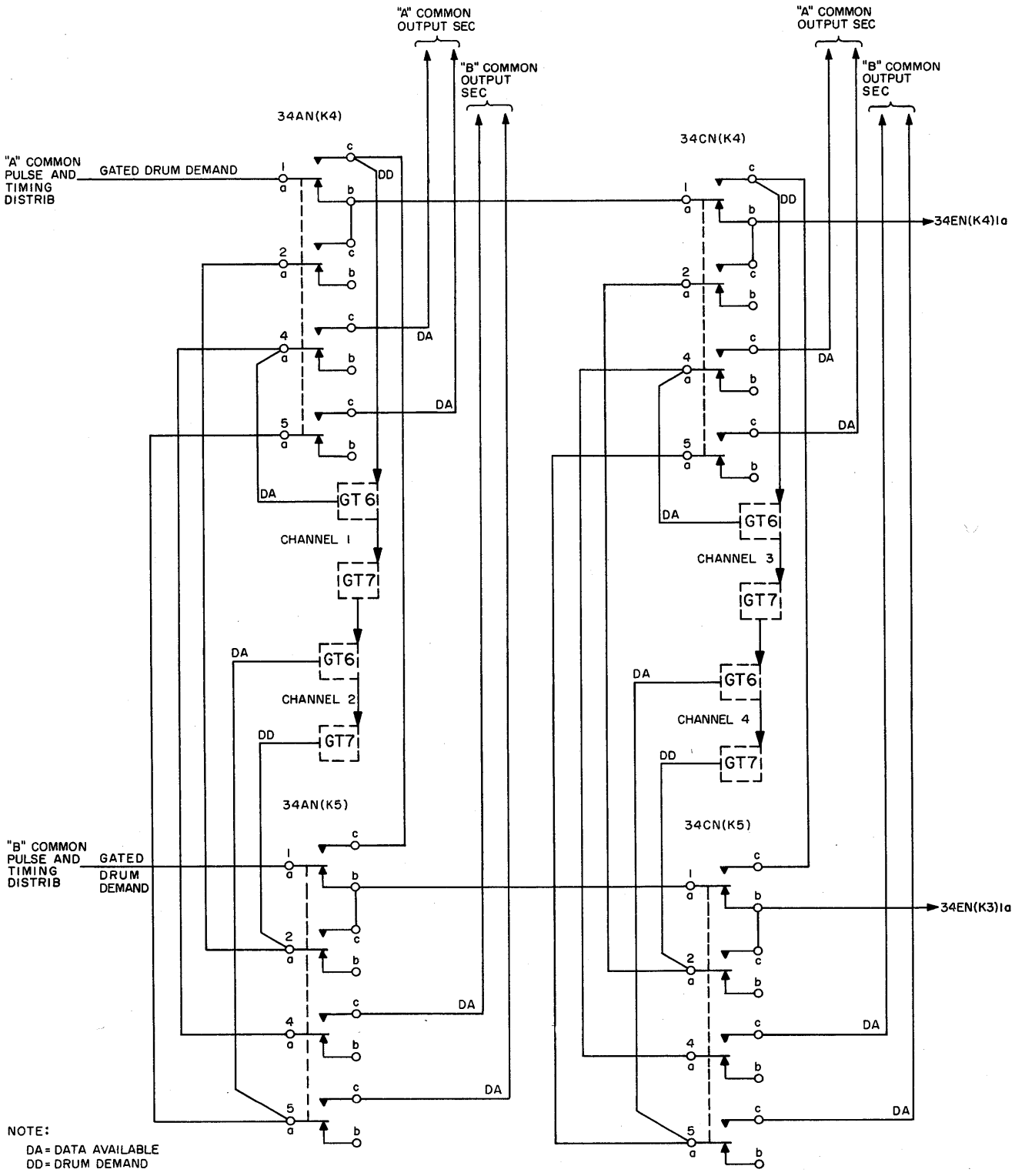


Figure 4–16. Drum Demand and Data Available Switching Circuit

5a-5c of 34AN(K4) to common output section A. If GT 6 is not conditioned, the DD pulse continues to circulate, passing through contacts 2a-2c-1b of 34AN(K4) to contact 1a of 34CN(K4). Since this relay is not energized, the DD pulse, derived from the A Drum System, passes on to the next pair of channels. Meanwhile, the gated DD pulse, derived from the B Drum System, can pass through contacts 1a-1b of unenergized 34AN(K5), through contacts 1a-1c of energized 34CN(K5), and through contact 1c of unenergized 34CN(K4) to sense channels 3 and 4. A data-available pulse produced by either of these channels will be connected by appropriate contacts in energized 34CN(K5) to common output section B.

4.3 SITE IDENTITY SWITCHING

The site identity switching directs the site identity drive signals from the active channels to the active common section and directs site identity drive signals from standby channels to the standby common section.

The site identity switching circuit consists of two relays for each pair of channels. The relays for channels 1 and 2 are shown in figure 4–17.

When common A is selected as the active common, and channels 1 and 2 are placed in the active status by the module A unit status switch, relay 34AS(K1) is energized, connecting the site identity drive of channels 1 and 2 to the site identity generator of common A (active) section. Placing channels 1 and 2 in standby status causes relay 34AS(K2) to be energized, connecting the two site identity drive signals to the site identity generator of common B (standby) section.

The selection of common B as active (hence common A as standby) causes relay 34AS(K2) to be energized when channels 1 and 2 are active, thereby sending the channel 1 and 2 site identity drive signals to the common B (active) section. Placing channels 1 and 2 in standby when common B is active causes relay 34AS (K1) to be energized, sending the signals to the common A (standby) section.

The energizing voltages for the two relays are controlled by the interaction of the DUPLEX SELECTION switch and the unit status switch (discussed in 4.5).

The write signals for the other pairs of channels are switched in exactly the same manner as described for channels 1 and 2. In general, the switching sends the site identity drive signals of standby channels to the standby common section and sends site identity drive signals from active channels to the active common section.

4.4 SITE IDENTITY SWITCHING FOR SPARES

The site identity switching for the spare channels circuit directs the write (site identity drive) outputs from the spare channels (channels 17 and 18) to be applied to the site identity cans of the channels being replaced by the spare channels.

Figure 4–18 shows the spare channel site identity switching circuit. The write signals from channels 17 and 18 are applied to the contacts of both switching re-

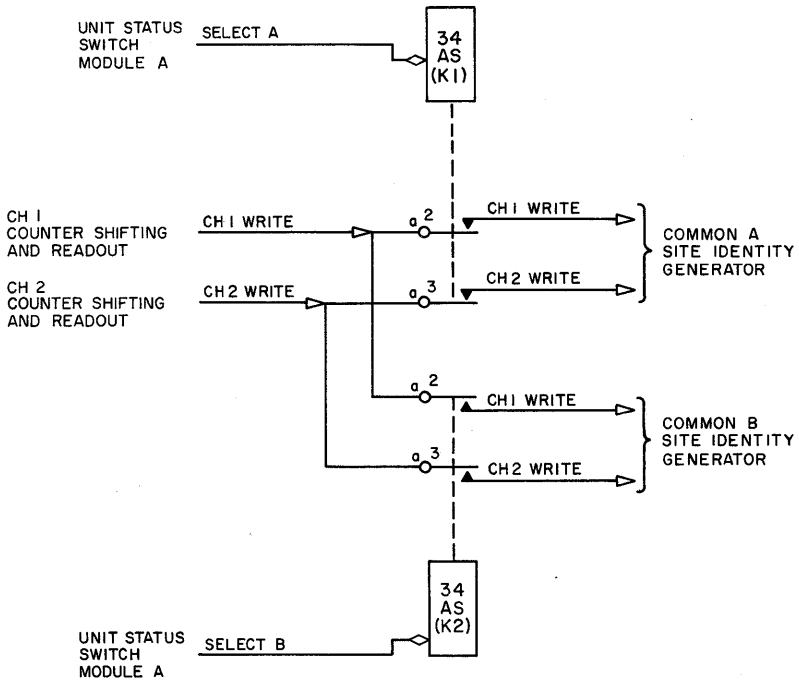


Figure 4–17. Site Identity Switching, Channels 1 and 2

lays 34VS(K1) and 34VS(K2). Relay 34VS(K1) is energized by the select A (—48V) line, while 34VS(K2) is activated by the select B (—48V) line. The select A line carries the —48V relay energizing voltage when duplex A is active and channels 17 and 18 are active, or when duplex B is active (duplex A, standby) and channels 17 and 18 are standby. Conversely, the select B line carries —48V when duplex B is active and channels 17 and 18 are active, or when duplex A is active (duplex B standby) and channels 17 and 18 are standby.

The write outputs of channels 17 and 18 are connected to site identity generator A when the select A relay 34VS(K1) is energized and to site identity generator B when the select B relay 34VS(K2) is energized. The write outputs from channels 17 and 18 are applied to the site cans for the channels substituted by the spares. When channels 1 and 2 are using the spares, the select channel 1 and 2 output of the spare CHANNEL SELECTOR switch on the simplex maintenance console energizes relay 34VT(K1), connecting the channel 17 and 18 write signals to site cans for channels 1 and 2, respectively. In the same manner, the other pairs of channels, when selected for substitution, will receive the channel 17 and 18 write signals.

4.5 DATA SWITCHING TO COMMON A OR COMMON B

The function of the data switching circuits is to present data from active channels to the active common section and data from standby channels to the standby common section. The common section is duplex, the sections being designated common A and common B. The DUPLEX SELECTION switch on the duplex switching console is used to select the common section that is to be active. When one of the common sections is active, the other section is standby.

Figure 4—19 is a simplified diagram of the data switching for channels 1 and 2 (module A). The circuit is simplified by showing a single-line representation for the 16 outputs from each channel.

With the DUPLEX SELECTION switch in the select A position, the —48V relay-driving voltage is then applied to the active contact (contact 1) of section G of the module A unit status switch. The standby positions (contacts 3 and 4) on section H of the module A unit

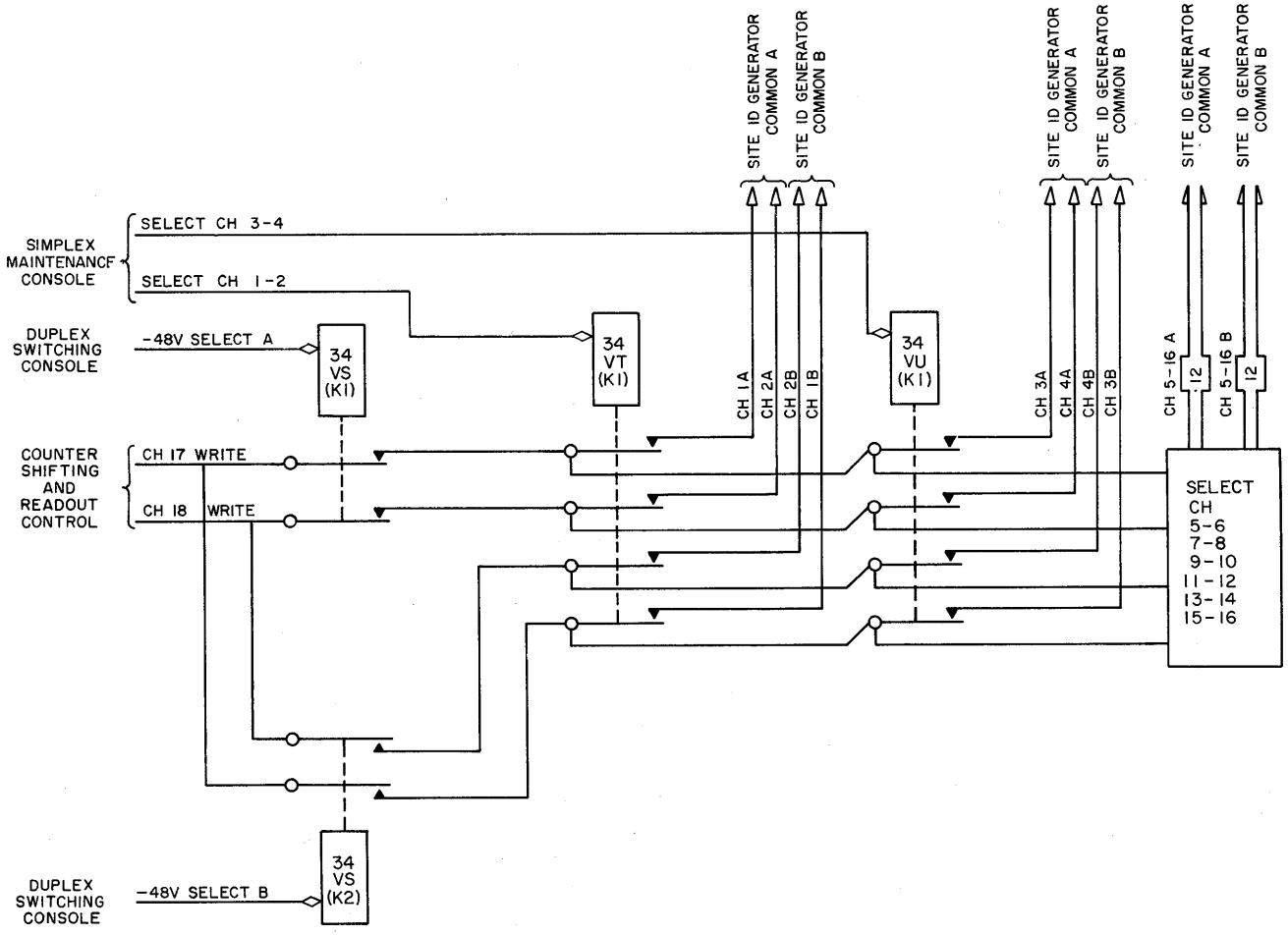


Figure 4—18. Site Identity Switching for Spare Channels

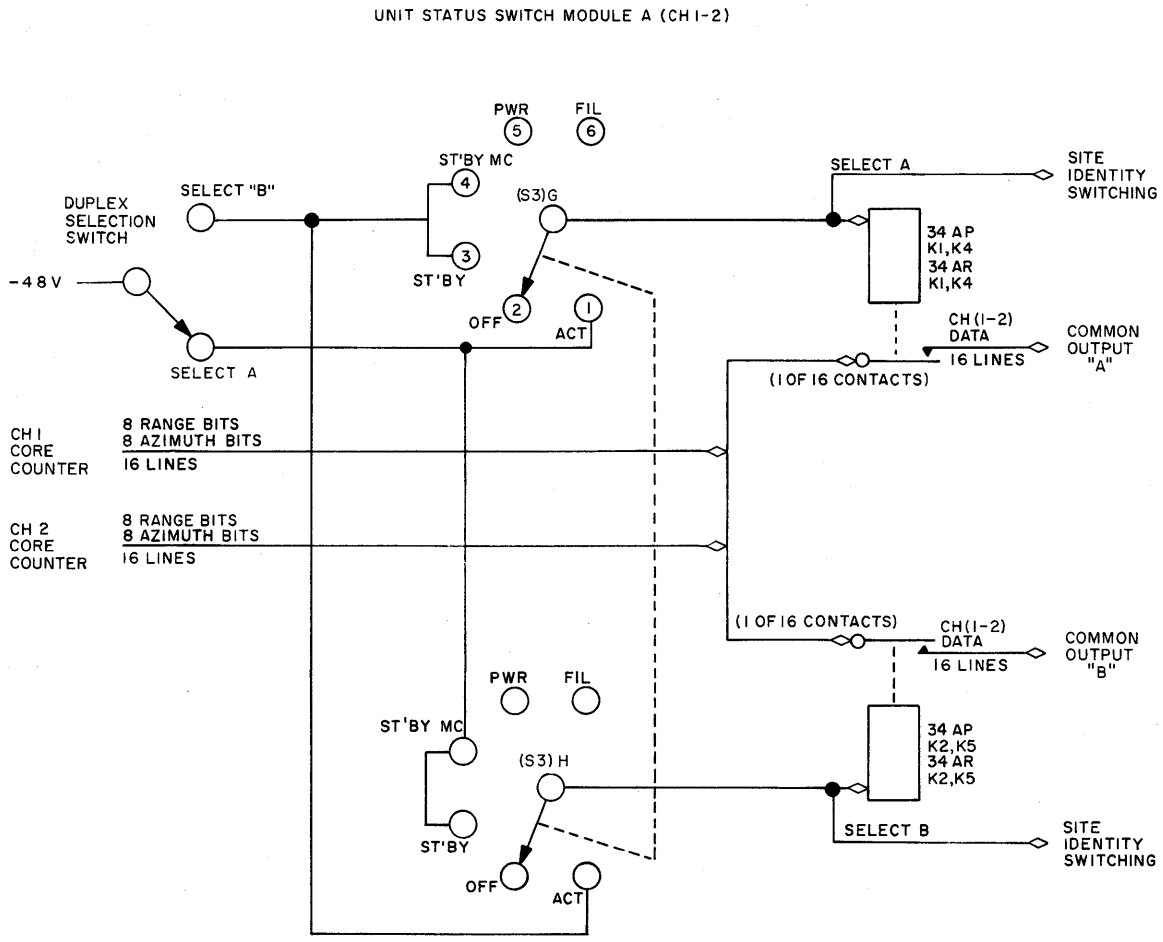


Figure 4–19. Data Switching

status switch also receive —48V. With module A (channels 1 and 2) in the active status (unit status switch set to contact 1), relays 34AP(K1), 34AP(K4), 34AR(K1), and 34AR(K4) are energized, connecting the 16 data outputs from channels 1 and 2 to common A, the active common section. With the unit status switch in the standby position, relays 34AP(K2), 34AP(K5), 34AR (K2) and 34AR(K5) are energized, connecting the 16 data outputs of channels 1 and 2 to the common B section which is in standby status.

When the DUPLEX SELECTION switch selects common B as the active section, the data outputs of channels 1 and 2 are sent to common B when the unit status switch for module A is active. Placing module A in the standby condition connects the data outputs of channels 1 and 2 to the standby common A.

The 16 outputs of all the active channels in the channel 1 through 8 group are combined and sent to the common output circuit. The 16 data bits of the active channels in the channel 9 through 18 group are also combined into 16 data inputs to the common output circuit.

4.6 TIMING PULSE SWITCHING

The timing pulses received from the Drum System are distributed, through switching, to channels which are in the same status as the common section. The OD 2 (50 kc), OD 3, and OD 4 pulses are transmitted from common A to channels in the same status as common A through the A signal relays; the pulses are transmitted from common B to channels in the same status as common B through the B signal relays. For channels 1 and 2, the pulses are distributed by contacts 1 through 5 of relay 34AN(K1); likewise, the pulses are distributed by contact 5 of 34AS(K1) for channels associated with common A and by contacts 1 through 5 of 34AN(K2) and contact 5 of 34AS(K2) for channels associated with common B. The relays are energized under control of the DUPLEX SELECTION switch (duplex switching console) and under control of the unit status switch (GFI channel control panel, simplex maintenance console).

4.7 SITE NEON SWITCHING

Each GFI channel control panel contains two sets of site identity indicators, indicating in a 5-bit binary

code the site which is transmitting information to the channel. The A set of indicators is active when the channel is in the same status as the A machine; the B set is illuminated when the channel is in the same status as the B machine.

4.8 STATUS INDICATION SWITCHING

When the signal relays of a channel are energized, +10V is transferred through relay switching to the related direct entry section of the MDI element, where it sets a 1 in an assigned core. Periodically, the cores (organized as a core matrix) are read out to the corresponding Central Computer. Energizing the A signal relays for channels 1 and 2 causes two cores to be set in the A MDI element through contact 2 and contact 3 of relay 34AS(K4). Contacts 2 and 3 of 34AS(K5) apply the +10V to the B MDI element, if the B signal relays for channels 1 and 2 are energized. Each computer is thus informed of the GFI channels associated with it.

CHAPTER 5
GFI COMMON SECTION

5.1 INTRODUCTION

The GFI common section receives filtered target co-ordinates from the counter sections of each of the 18 (16 plus 2 spare) channels and transfers these co-ordinates to the Drum System. The site identity number (in binary form) is sent to the Drum System along with the target data.

Figure 4–20 shows the common section in simplified form and also illustrates the relationship with duplex switching. The common section is duplicated for reliability and the two identical sections are designated common A and common B, respectively. In operation, one of these sections is active, while the other is standby. The active common section receives target data from active GFI channels; the standby common section receives target data or test data from channels in the standby status.

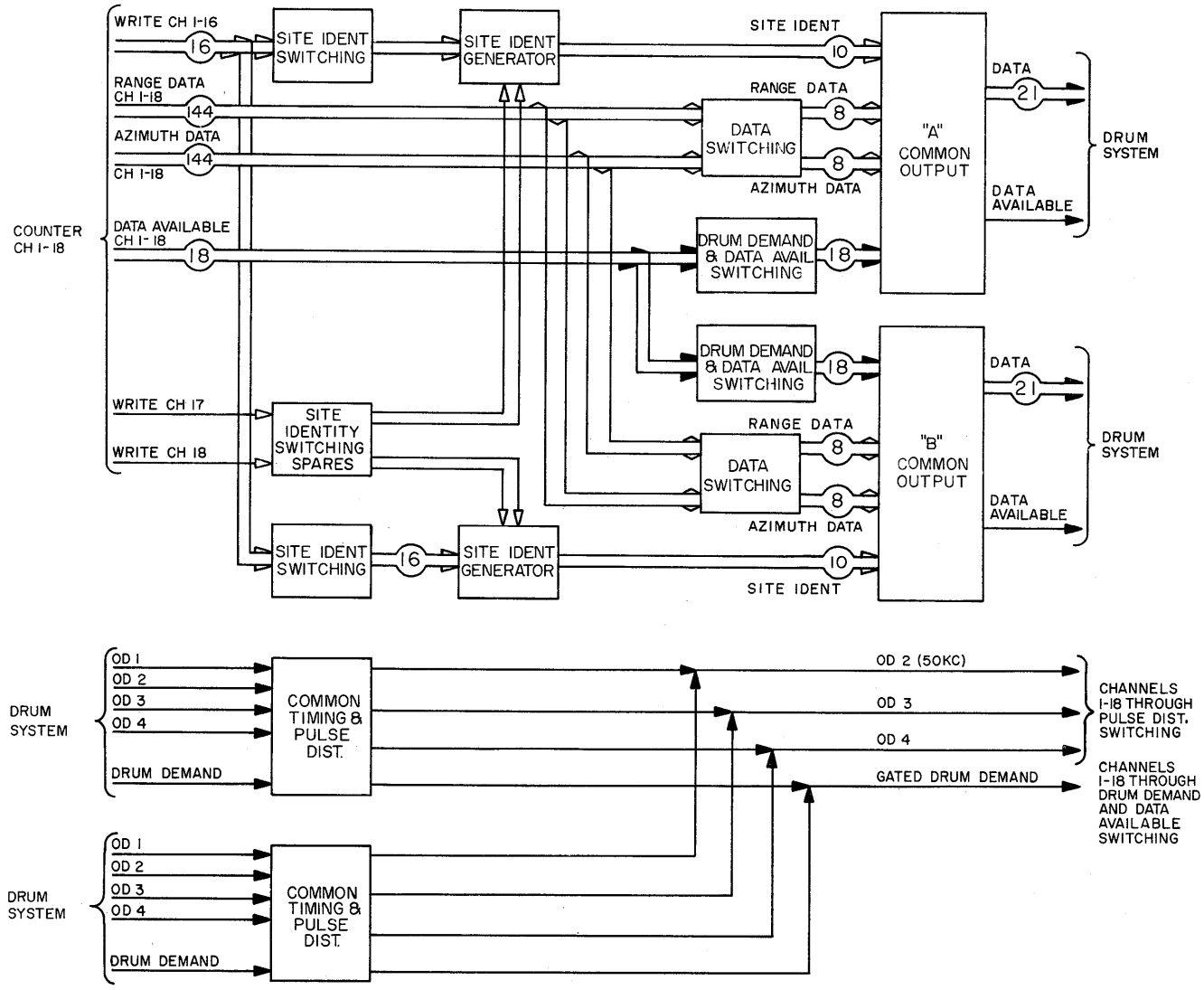


Figure 4–20. GFI Common Section, Simplified Block Diagram

The common section performs the following functions:

a. The common timing and pulse distribution circuit receives OD 1, OD 2, OD 3, OD 4, and DD pulses from the Drum System. It distributes OD 3, OD 4, and alternate OD 2 pulses to the channel circuitry; pulses from the active Drum System are distributed to the active channels, and pulses from the standby Drum System are distributed to the standby channels. It also supplies gated DD pulses to the drum-demand and data-available switching circuit. This circuit circulates each gated DD pulse through the channel counter sections until it finds a channel containing filtered target data. It then connects the data output from the counter section of that channel to the common output circuits. The counter sections of the active channels are linked to the active Drum System through the active common output circuit; the counter sections of the standby channels are linked to the standby Drum System through the standby common output circuit.

b. The active site identity generator receives the site identity drive signals from the active counters and generates a site identity binary number (five bits) for each site identity drive signal received. Since each GFI radar site sends its messages to a separate GFI counter section, the GFI radar site originating a target is identified by the counter section that has processed the target.

c. The active common output circuit receives target data bits from the active counter circuits through the data switching circuit, receives five site identity bits from the active site identity generator, and transmits a standard pulse to the active Drum System for each 1 bit of target data or site identity. The standby common output circuit performs the same function for the standby counter and site identity generator outputs.

5.2 COMMON TIMING AND PULSE DISTRIBUTION

The common timing and pulse distribution circuit processes and distributes pulses from the Drum System as follows: the OD 3 and OD 4 pulses are first current-amplified; the OD 3 pulses are then fed to the counter-shifting and readout control circuit as shift drive pulses, and to the azimuth protection circuit for use in the north-azimuth protection and separation circuit, and elsewhere. The OD 4 pulses are also fed to the azimuth protection circuit and to the range synchronizer.

Alternate OD 2 (50 kc) pulses are current-amplified and fed to the range synchronizer where, among other uses, they synchronize the unsynchronized range level from the data conversion circuit. The OD 2 frequency is halved by FF 1 and GT 1, shown in figure 4–21. Assume that FF 1 is set and that GT 1 is conditioned. The first OD 2 pulse passes GT 1 and resets FF 1. GT 1 is now deconditioned, blocking the second OD 2 pulse.

OD 3, OD 4, and OD 2 (50 kc) pulses are supplied by the A Drum System when channel relays in the 34-N(K1) and 34-S(K1) series are energized, and are supplied by the B Drum System when channel relays in the 34-N(K2) and 34-S(K2) series are energized.

Drum-demand pulses from the Drum System are gated to the counter-shifting and readout control circuit of the highest priority channel at OD 1 + 0.5 time. The gating circuit consists of FF 2, GT 2, and the 0.5-μsec delay block, shown in figure 4–21. FF 2 is set by the DD pulse, conditioning GT 2. The next OD 1 pulse, delayed 0.5 μsec, strobes GT 2. Two μsec later, FF 2 is cleared by an OD 2 pulse, deconditioning GT 2.

5.3 SITE IDENTITY GENERATOR

The site identity generator circuit provides a means of identifying the gap-filler radar that has sent particular target data. A binary number is generated and added to each set of target co-ordinates being sent to the Drum System.

Each channel receives target data from a separate gap-filler site. Therefore, a site identification number is assigned to each target according to the channel on which it is received.

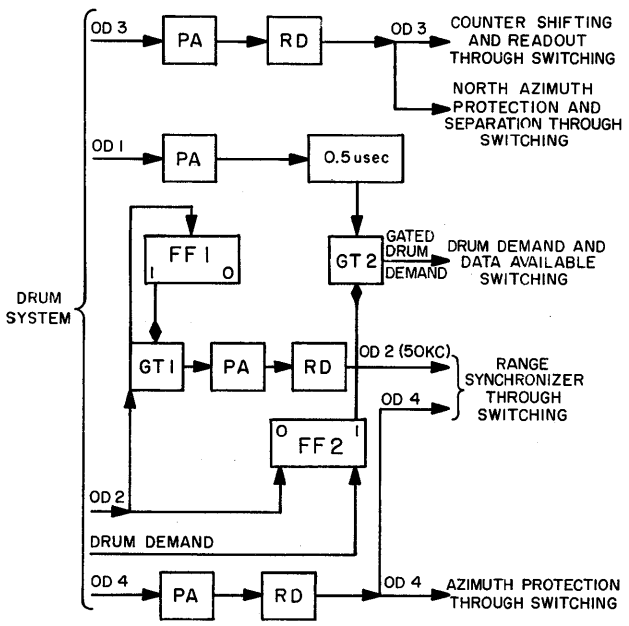


Figure 4–21. Common Timing and Pulse Distribution

5.3.1 Site Identity for Channels 1 through 16

As shown in figure 4—13, a channel which reads out data from its azimuth and range registers also sends a 5-μsec level to the site identity generator, a simplified block diagram of which is shown in figure 4—22. The site identity generator receives these 5-μsec levels from each channel and applies them to a separate site identity can.

Each site identity can is wired so that the application of the 5-μsec level produces a binary site identity number on the five output lines. Figure 4—22 shows the detailed wiring of the site identity cans for channels 1 and 2. The binary site identity is 11011 for channel 1 and 10101 for channel 2. The site identity can for channel 1 is wired so that the +10V level from channel 1 (which is up for 5 μsec) produces 1's (+10V) on site identity bit lines 1, 2, 4, and 5. The third site identity bit line is connected to —30V which indicates a binary 0. The +10V level from channel 2, when applied to the channel 2 site identity can, produces 1's (+10V) on the first, third, and fifth site identity bit lines. The second and fourth site identity bits are —30V (binary 0).

The generation of the site identity bits for the other channels is accomplished in the same manner as that described for channels 1 and 2, except that the wiring of each site identity can is arranged so that the output produced is the binary site identity number for the particular channel. The like-numbered site identity bit lines

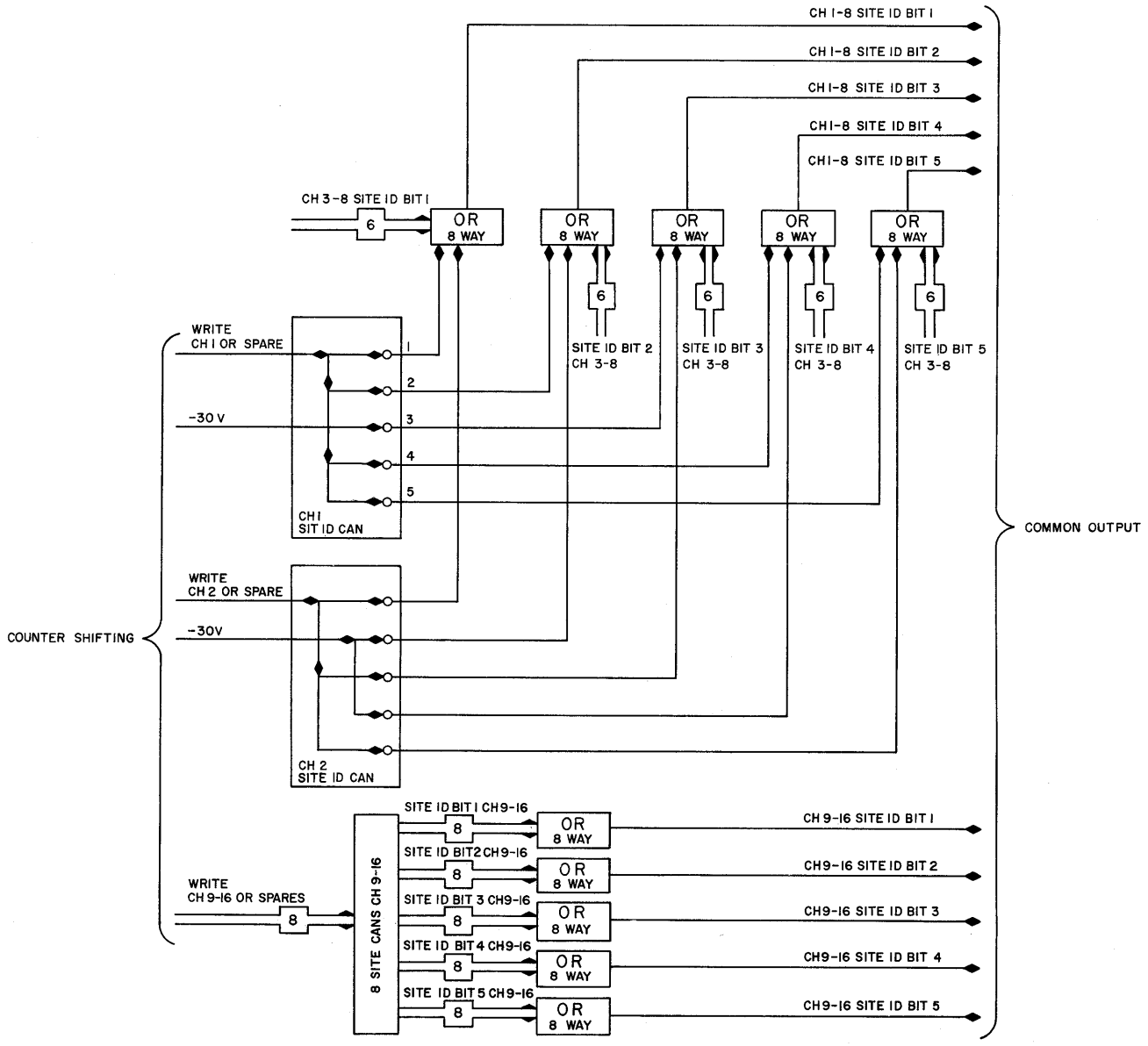


Figure 4—22. Site Identity Generator, Simplified Logic Diagram

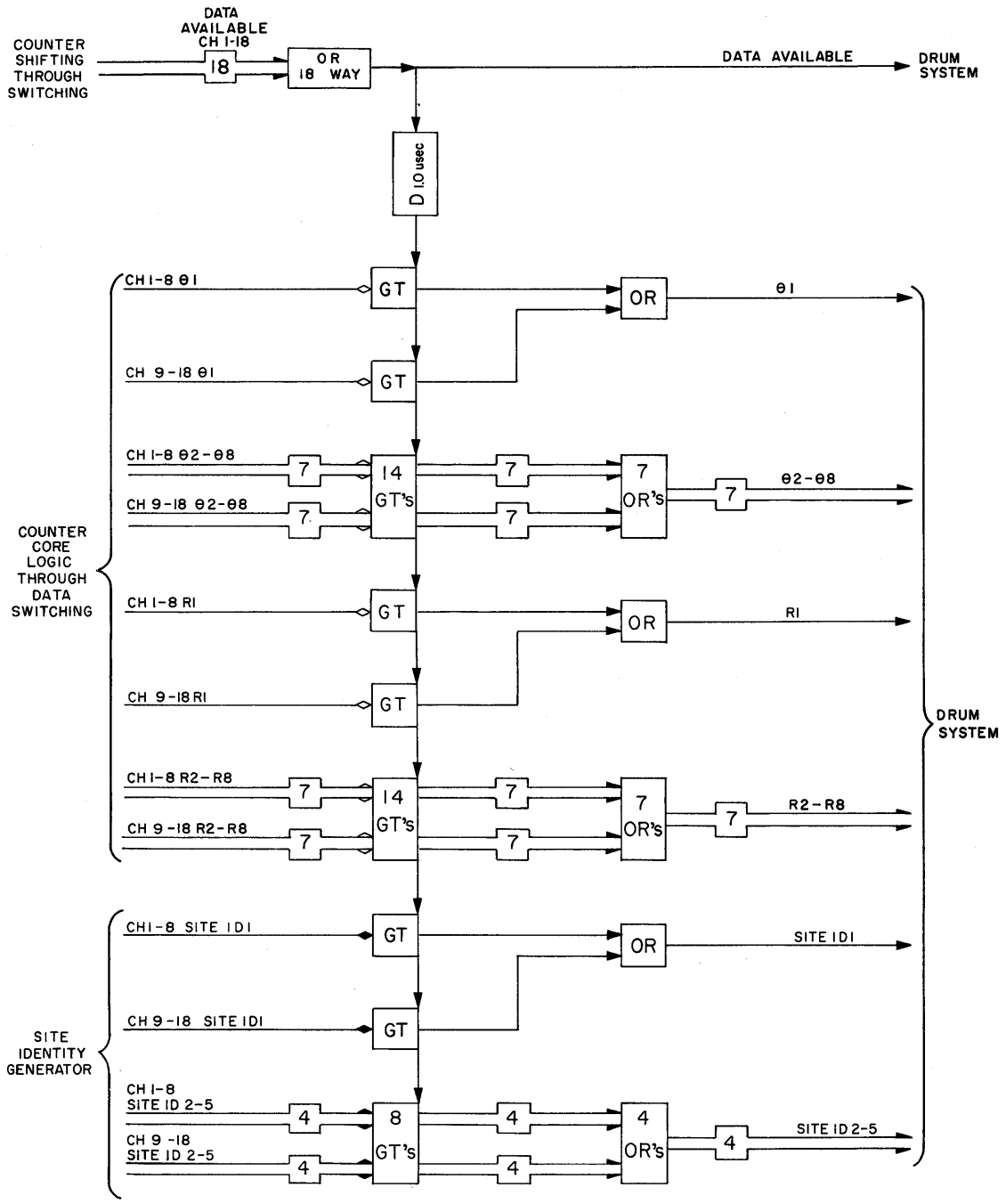


Figure 4–23. Common Output Circuit

from the site cans for channels 1 through 8 are combined by two 4-way OR's and a 2-way OR (shown as a single 8-way OR). The output of each of these 8-way OR circuits represents the site identity for the channel which is transferring data to the Drum System via the common section. For example, when none of the channels is transferring data, the inputs to the 8-way OR circuits are all 0's (—30V). Consequently, the outputs of the 8-way OR circuits are also 0's. Assuming that channel 1 begins to read out, a 5-μsec +10V output from an SS in the counter-shifting circuit of channel 1 is applied to the channel 1 site identity can. The channel 1 inputs to the 8-way OR circuits for site identity bits 1, 2, 4, and 5 are then +10V. The output of these 8-way OR circuits is a 1 (a single 1 input to an OR produces a 1 output). Therefore, channel 1 through 8 site identity bits 1, 2, 3, and 5 are 1's, while channel 1 through 8 site identity bit 3 is a 0 (the inputs to the 8-way OR cir-

cuit for bit 3 are all 0's). In the same manner, the channel 1 through 8 output for the five site identity bits will always be the site identity of the channel that is read out.

The outputs of the site identity cans for channels 9 through 16 are also combined by 8-way OR circuits and are designated channels 9 through 16 site identity bits 1, 2, 3, 4, and 5.

The channels 1 through 8 and 9 through 16 bits are sent to the common output circuit where they permit a standard pulse to be transferred to the Drum System for each 1 bit of site identity data. The site identity for each target is thereby indicated to the Central Computer along with the target co-ordinates (range and azimuth).

5.3.2 Site Identity for Spare Channels

Spare channels (17 and 18) may be substituted for regular channels (1 through 16) for operational or maintenance purposes. When the spare channels are substituted, the spare channels assume the processing functions of the replaced channels. However, the site identity of the gap-filler radar site associated with the regular channel must be retained. For instance, if channel 1 has been selected for replacement by spare channel 17, channel 17 processes the target data and transmits the information through the common section to the Drum System. The write level generated by channel 17 is applied to channel 1 site can via spare channel switching and duplex switching. Thus, when channel 17 is transmitting range and azimuth data to the Drum System, the site identity generator is sending the site identity of the GFI radar site (as indicated by channel 1 site can) associated with channel 1. Similar circuitry adds the site identity of other channels when these channels are replaced by the spares.

5.4 GFI COMMON OUTPUT

The GFI common output circuit (fig. 4–23) receives the 21 data bits (8 azimuth bits, 8 range bits, and 5 site identity bits) from the channel equipment and transfers a standard pulse to the Drum System for each 1 data bit. The relative-time bits which make up the remaining bits of the GFI drum word are inserted at the Drum System by the relative-time counter of the LOG drum.

When a channel that has a target position stored in its range and azimuth registers receives a DD pulse, the registers read out the 16 data bits (8 azimuth and 8 range bits). The core outputs of the registers are transferred to the data switching circuit which combines the identical bits from the channels into two outputs for each bit. The bits are designated $\theta 1$, $\theta 2$, $\theta 3$, etc., for the eight azimuth bits, and R1, R2, R3, R4, etc., for the eight range bits. The two outputs for each bit are designated CH 1-8, for the outputs from channels 1 through 8, and CH 9-18, for the outputs from channels 9 through 18. Combining 18 outputs for each bit into two outputs is made possible because only one channel can read out the data contained in its registers when a DD pulse is received. The sensing of one channel at a time, in order of priority, by the DD pulse accounts for the single-channel readout.

The common output circuit comprises 42 gates (two for each drum word bit). The gates are simultaneously strobed by a data-available pulse, delayed by the 1-μsec delay unit. The data-available pulse initiates the readout in the channel and is delayed in the common section so that it strobes the gates when the register core outputs are at the maximum value. Since a channel will produce a data-available pulse only during readout, the 18 data-available lines are combined by an OR circuit into a common data-available output. This output is sent to the Drum System and is also delayed and used as the strobing pulse for the gates.

An example of how a drum bit is generated follows. Assume that the first azimuth bit ($\theta 1$), contained in the azimuth register, is a 1. When the channel receives a DD pulse, a 2-μsec readout signal is generated and applied to the range and azimuth registers. The subsequent outputs of the register CS's are +10V pulses for each CS that contains a 1 bit, and no (0V) output from core shifts containing 0 bits. The $\theta 1$ bit, being a 1, causes either the channel 1 through 8 $\theta 1$ or channel 9 through 18 $\theta 1$ inputs (depending on which channel is reading out) to the common output circuit to be at +10V. The +10V conditions the gate, permitting the delayed data available pulse to pass through the gate and through an OR circuit to the Drum System. The standard pulse applied to the Drum System for a 1 data bit causes a 1 to be written into the $\theta 1$ drum bit position. If the $\theta 1$ 1 bit appeared on the channel 1 through 8 $\theta 1$ input (one of the first eight channels reading out), then the channel 9 through 18 $\theta 1$ input would be a 0 since none of the channels connected to that line would be reading out. When the $\theta 1$ bit being transferred is a 0 instead of a 1, both channels 1 through 8 and 9 through 18 inputs will be 0 and neither $\theta 1$ gate will be conditioned. The output to the Drum System will then be 0, which will cause a 0 to be written in the $\theta 1$ drum bit position.

All the other azimuth and range bits are written on the drum in exactly the same manner that has been described for the $\theta 1$ bit. The site identity drum bits are produced in the same manner except that the voltages that condition the gates are generated by the site identity generator. The site identity generator produces five bits whenever a channel is transferring data to the drums. The bits produced are determined by the channel that is transferring the data. The five bits are thus

an indication of the radar site that has sent the data. The site identity bits are inserted on the drum along with the target data. The Central Computer is then made aware of the location of a target by receiving the polar co-ordinates of the target with the site location as the origin.

CHAPTER 6
GFI MAPPER SECTION

6.1 INTRODUCTION

The Central Computer System would be overburdened if all the target signals that could conceivably appear were accepted and stored. Therefore, a mapper console (fig. 4–3) is employed as a means of target selection. A mapper technique is used to remove target signal indications caused by ground, sea, cloud returns, fixed objects, stray noise, or deliberate jamming.

A simplified block diagram of the mapper section is shown in figure 4–24. A polar co-ordinate presentation on the face of a CRT is provided to reproduce the target location in a given radar coverage area. Incoming target signals cause intensification of the CRT electron beam to produce a blue flash and a long-persistent yellow afterglow on its phosphorescent screen. A photomultiplier tube, made sensitive with a blue filter to blue light, detects this target indication and causes a filtered target pulse to be generated. The pulse is fed to the counter section to prepare any accumulated azimuth and range counts designating the target location for transfer to the Drum System and, hence, for transfer to the Central Computer System. The counter section returns a reintensify pulse to the sweep intensification and focus circuit and, hence, to the grid of the CRT.

To present an accurate plan position indicator (PPI) display, the position of the deflection yoke of the GFI mapper must be synchronized with that of the radar antenna which is the source of the information. To achieve the synchronization, two conditions must be met: the mapper deflection yoke must rotate at the same speed as the radar antenna; the mapper deflection yoke must be oriented with the radar antenna (i.e., the yoke must pass through north at the same time as the radar antenna). The mapper deflection yoke is made to rotate at the correct speed through the operation of the azimuth-synchronizing circuit and proper orientation is maintained through the operation of the north-synchronizing circuit. The azimuth and north protection circuit provides protection against loss of synchronization resulting from missing or spurious azimuth and north-azimuth pulses.

The azimuth synchronizer receives azimuth pulses from the azimuth and north protection circuit. These pulses are converted into a 2-phase voltage to drive the 2-phase, synchronous yoke motor. During start operation, the azimuth synchronizer receives a 60-cycle motor drive voltage from the start and alarm circuit rather than the azimuth pulses from the azimuth and north protection circuit.

The north synchronizer receives a north-azimuth pulse from the azimuth and north protection circuit and a yoke-north pulse from the yoke-north cam switch. Any difference in the arrival time of these two pulses causes a correction to be made by the brake system of the yoke gear train. A difference in the arrival time of the north-azimuth pulse and the yoke-north pulse can be caused by the presence of some spurious azimuth pulses during the previous revolution of the radar antenna, by the absence of some of the normal azimuth pulses, or by subharmonic operation.

An azimuth and north protection circuit is provided to maintain synchronization and a correct azimuth count. This circuit suppresses spurious pulses and generates substitute pulses for any that are missed. It receives azimuth and north-azimuth pulses and separates them into two signals, sending azimuth pulses to the azimuth synchronizer and counter sections and north pulses to the north synchronizer. This separation utilizes a north signal from the yoke-north cam switch as a gating signal. Normal azimuth pulses are also applied to a magnetic drum to be used to generate substitute azimuth pulses, when required. The magnetic drum returns a pulse to the azimuth and north protection circuit, after a time delay, if the succeeding pulse fails to appear from the az-north DCR. In the event of either a missing or a spurious azimuth pulse, a level shift is sent to the start and alarm circuit. The OD 3 and OD 4 pulses are used as standard timing pulses in the circuit.

The start and alarm circuit is provided to control the operation of the yoke motor during start operation, to inhibit the generation of alarm conditions during start operation, and to provide audible and visual signals for indicating an alarm condition if erroneous information persists. The input to the start and alarm circuit consists of azimuth and north-azimuth pulses from the az-north DCR during start operation and azimuth and target alarms during normal operation.

A logic circuit discussion of the mapper components follows.

6.2 AZIMUTH SYNCHRONIZER

6.2.1 General

The angular position of the target display on the CRT screen corresponds to the azimuth component of

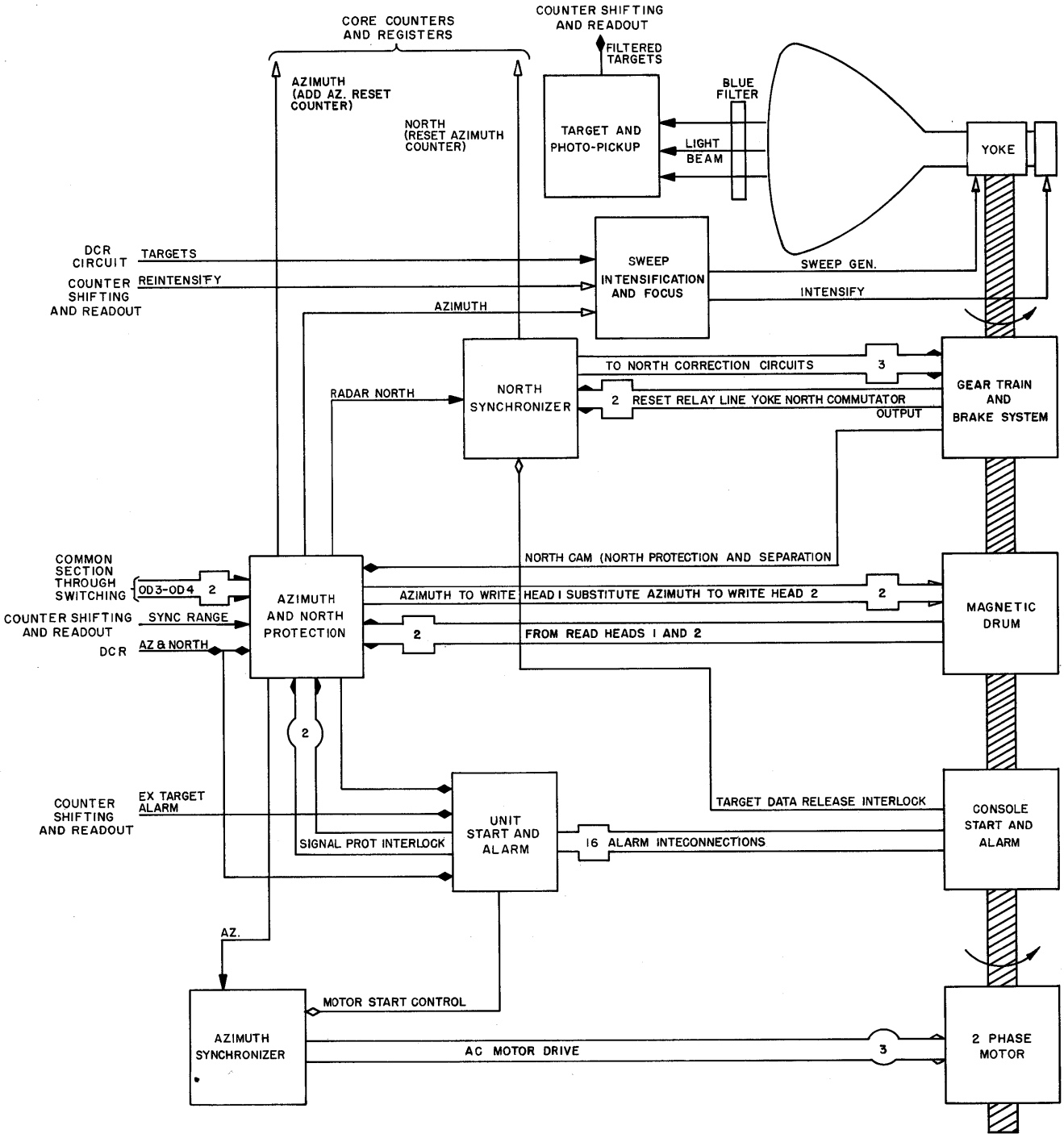


Figure 4–24. GFI Mapper, Simplified Block Diagram

target position with respect to the scanning radar. In order to obtain this correspondence, it is necessary to synchronize the angular position of the CRT deflection yoke with respect to the angular position of the associated radar antenna. This synchronization is developed through the interaction of the start and alarm circuits, the azimuth synchronizer circuit, and the north synchronizer circuit.

The rotation of a remotely located radar antenna generates azimuth pulses. These azimuth pulses are fed through a telephone-line data link and are converted into two voltages which drive the 2-phase synchronous motor in the GFI mapper. This motor is connected through a gear reduction train to the yoke of the GFI mapper CRT, so that the yoke rotation is a function of motor speed. The motor speed depends on the repeti-

tion rate of the azimuth pulses generated at the radar site; i.e., one revolution of the azimuth motor occurs for each azimuth pulse. The repetition rate is 256 pulses per antenna revolution, multiplied by the speed of the antenna. If the antenna speed is 6 rpm, for example, a total of 1,536 ppm is generated and, consequently, the motor speed is 1,536 rpm. Appropriate reduction gears drive the yoke at the same speed as the radar antenna.

The azimuth motor drive circuit must follow the radar antenna over the scan rate of 2 to 10 rpm, which corresponds to an azimuth frequency range of 8.5 to 42.5 cps.

6.2.2 Azimuth Synchronizer, Block Level Discussion

The input to the azimuth synchronizer is an OD 4 pulse following an azimuth pulse. This pulse is applied to the complement input of the flip-flop (as shown in fig. 4–25) at a frequency range of 8.5 to 42.5 cps, depending on the rotational speed of the radar antenna. The flip-flop square wave output changes from +10V to −30V and back to +10V for each pair of pulse inputs. Therefore, one output cycle is obtained for every two input pulses, or an output rate of one-half the input; i.e., 4.25 to 21.25 cps.

The output of the flip-flop is connected to the control grid of the Miller Integrator. Since the gain of the Miller Integrator is inversely proportional to the frequency of the input signal, provision must be made to maintain a constant amplitude output, regardless of the input frequency as determined by the speed of antenna rotation. This is accomplished by the automatic gain control (AGC) circuit which applies variable clamping levels to the Miller Integrator input.

The output from the Miller Integrator is a triangular wave of the same frequency as the square wave. This output is applied to a frequency doubler (FD), which doubles the frequency of the triangular wave. This frequency, then, is equal to that of the azimuth pulses.

The output from the frequency doubler is applied to the level amplifier (LEA). The output of the level amplifier is applied to the AGC circuit and the phase splitter of the motor drive section.

The output of the AGC circuit is converted, as a result of filter action, into a d-c potential. This voltage establishes the variable clamping levels mentioned previously.

The other level amplifier output is applied to the phase splitter through contacts 1 and 2 of relay K11. The phase-splitter outputs are two voltages, 90 degrees out of phase, which drive the 2-phase synchronous motor. The drive voltages are nearly constant in amplitude throughout the frequency range. Therefore, the motor speed is a function of the antenna-azimuth pulse rate, which, in turn, depends on the antenna speed. When appropriate reduction gears are used, the yoke of the mapper CRT will rotate at the same speed as the radar antenna. During start operation, contacts 2 and 3 of relay K11 apply 34 volts, 60 cycles, to the phase splitter.

6.3 NORTH SYNCHRONIZER

6.3.1 General

As noted in 6.2.1, the north synchronizer maintains the polar orientation of the deflection yoke with respect to the radar antenna by correcting any position errors which occur. The north synchronizer senses these errors as differences between the occurrence time of the north-azimuth pulse (which represents the radar antenna north position) and the north pulse developed in the console (which represents the deflection yoke north position).

The azimuth synchronizer circuit (described in 6.2) drives the motor which, in turn, rotates the yoke through a set of gears and differentials. When the synchronization is correct, a normal-speed brake engages a differential gear to keep the yoke turning at normal speed. If the yoke lags behind the radar, a double-speed brake engages a differential, resulting in the yoke turning at twice the normal speed. If the yoke reaches north in advance of the radar north, a stop brake locks the yoke in a stationary position until the north-azimuth pulse arrives; after this action, the normal-speed brake is again engaged. The action of the brakes is controlled by relays, which are energized or de-energized in accordance with the condition of relay driver circuits responding to the north pulses from the radar and the yoke. The correction starts not more than 10 degrees before the yoke reaches north and ends not more than

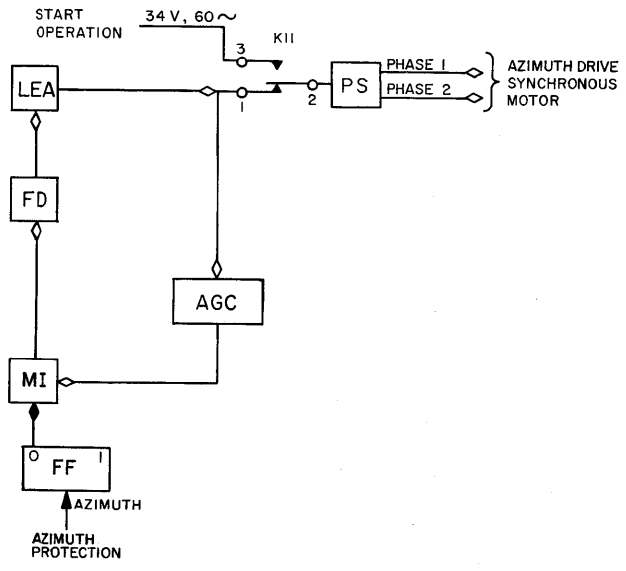


Figure 4–25. Azimuth Synchronizer, Simplified Logic Diagram

5 degrees after it passes north. The angular limits are maintained by the use of a cam rotating on the same shaft as the yoke. If an error is greater than these limits, the yoke remains in the north position until the following north-azimuth pulse is received.

The following discussion of the north synchronizing circuit operation is considered in terms of the three possible operating conditions:

a. Yoke passes through north after the occurrence of a north-azimuth pulse.
b. Yoke passes through north before the occurrence of a north-azimuth pulse.
c. Yoke-north synchronized with north-azimuth pulse.

6.3.2 Yoke Lags Radar Antenna

This condition indicates that the mapper CRT yoke is lagging behind the scanning radar antenna. In this case, the yoke speed is doubled until yoke-north is coincident with the north-azimuth pulse, at which time the speed is restored to its normal rate.

The north synchronizer is shown in simplified block diagram form in figure 4–26. Doubled speed of the yoke is accomplished as follows. The radar north signal from the azimuth and north protection circuit causes thyratron relay driver (RYD) 1 to fire, which energizes relays K2 and K3. Contacts 1 and 2 of K3 apply —150V to the coil of relay K4 to maintain energization of K4, when relay K1 is de-energized later in the opera-

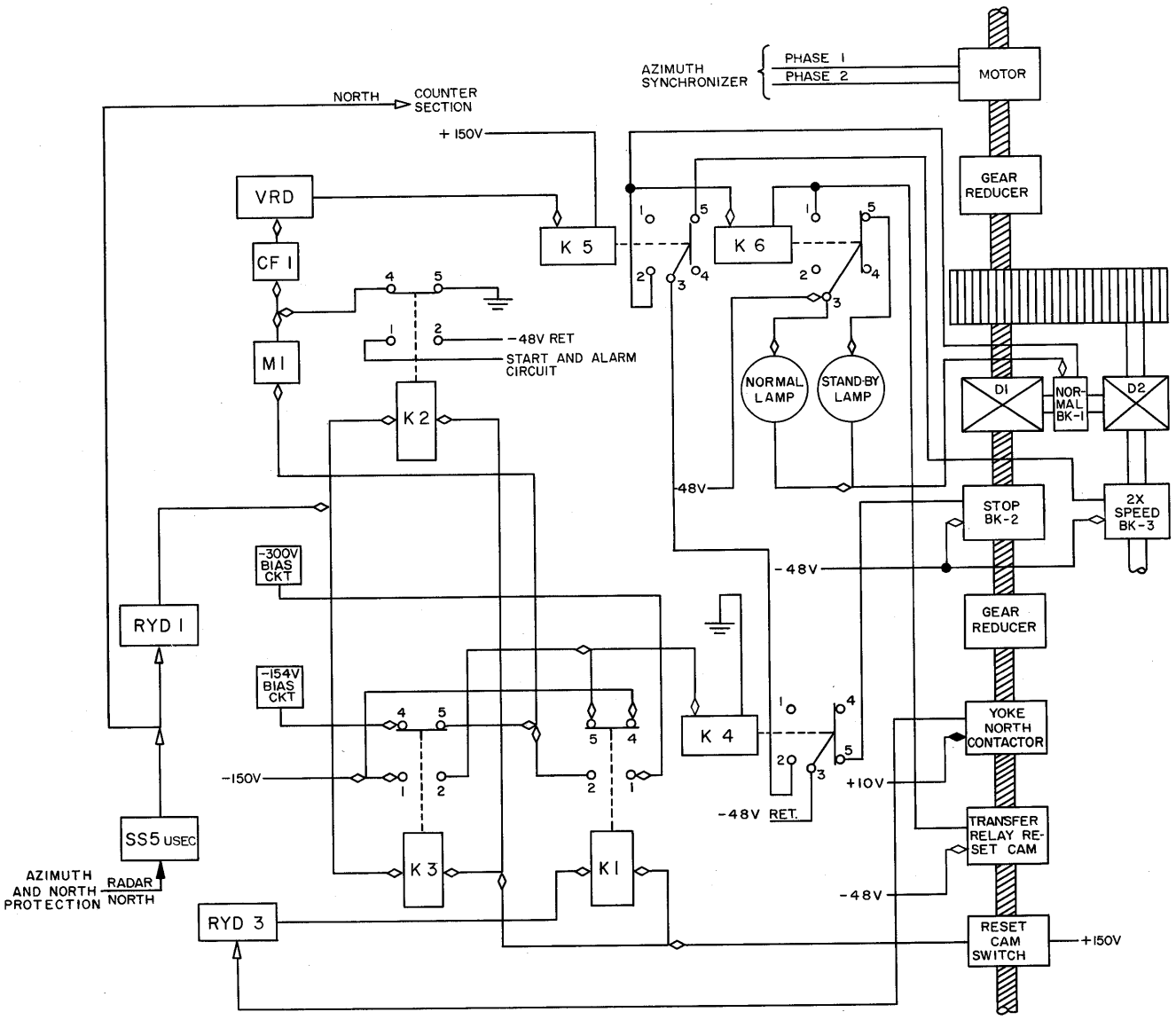


Figure 4–26. North Synchronizer, Simplified Block Diagram

tion. The opening of contacts 4 and 5 of relay K3 causes a positive step voltage (removal of —154V bias) to be applied to the Miller Integrator, which causes its output to fall. At the same time, the energizing of relay K2 removes a ground from the input to cathode follower (CF) 1. The effect of this ground is such that, when it is present, the output from the cathode follower is a d-c level slightly greater than the cut-off value of vacuum tube relay driver (VRD) 2, to which it is applied. The effect of the above action (the decrease in the output of the Miller Integrator and the removal of the ground from the input to CF 1) causes VRD 2 to cut off and de-energize relay K5. This action de-energizes normal-speed brake BK-1. A —48V d-c return path is completed to double-speed brake BK-3 through contact 2 of relay K4 and contact 5 of relay K5, thus energizing it. The yoke then rotates at twice its normal speed.

When the yoke passes through the north position, RYD 3 is fired by a signal from the yoke-north contactor, causing energization of relay K1 which applies a negative step voltage to the Miller Integrator. The output of the Miller Integrator increases and fires VRD 2, energizing relay K5. Energization of relay K5 energizes the normal speed brake and de-energizes the double-speed brake. The yoke proceeds at a speed of twice the normal rate during the interval between the radar-north pulse and the yoke-north pulse. Because of the action of the Miller Integrator, the double speed is maintained for an equivalent period of time after the yoke-north pulse appears. As a result, the yoke is returned to synchronism with the gap-filler radar, and the yoke resumes normal speed.

6.3.3 Yoke Leads Radar Antenna

A second condition of relative position exists when the yoke position is in advance of the radar antenna. The condition is corrected by stopping the yoke until the radar-north pulse is received. Figure 4–26 shows that the yoke-north pulse fires RYD 3. The output of this relay driver energizes relay K1, removing —150V from K4, and de-energizing it. This applies a —48V return to the stop brake (BK-2) through points 4 and 5 of relay K4, thus energizing the stop brake. Relay K4 also removes the —48V return from the normal speed brake (BK-1) at the same time. This condition of relay K4 causes the normal-speed brake to be de-energized and the stop brake to be energized.

The yoke then remains stationary until the radar-north pulse is received. In order to restore the yoke to synchronous operation with respect to radar north, radar-north pulses must cause stop brake BK-2 to be released and normal-speed brake BK-1 to be energized. The north radar pulse causes RYD 1 to fire and to energize relays K2 and K3. Relay K3 applies —150V dc to the coil of relay K4, energizing it. This action de-energizes the stop brake and energizes the normal-speed brake. The yoke now resumes its normal speed in synchronism with the scanning radar antenna.

6.3.4 Yoke and Radar Antenna Synchronized

When the yoke is in synchronism with the antenna, the north-synchronizing circuit receives two pulses simultaneously, one, the radar-north pulse and the other, the yoke-north pulse. The operation of the north synchronizer under this condition is such that neither the stop brake nor the double-speed brake becomes energized. When these two pulses arrive at the same time, RYD's 1 and 3 fire simultaneously (fig. 4–26). The resulting signals, occurring together, energize relays K1, K2, and K3. This condition of the relays keeps the Miller Integrator inoperative, thereby preventing relay K5 from being de-energized. At this time, these relays maintain the —150V dc energizing voltage for relay K4.

6.3.5 Operation of Relay K6

During normal operation (that is, when the normal-speed brake is energized), relay K6 is also energized. The —48V d-c level necessary to keep BK-1 energized is applied through the normal lamp which functions as a resistor. During unsynchronized operation, however, relay K6 is de-energized. The —48Vdc level is now provided with a parallel path to the magnet of BK-1. One branch of the parallel network is through the normal lamp; the other is through contacts 3 and 5 of relay K6 to the standby lamp. This, in effect, gives a lower resistance path to current flow and, as a result, the current applied to the magnet of BK-1 is increased. Because of the condition of relays K4 and K5, BK-1 is de-energized at this time. Therefore, the increased current acts to anticipate the return of BK-1 to normal operation because an initial surge of current will aid the normal brake to return the yoke to synchronism with the radar antenna.

6.3.6 Generation of Yoke-North Pulse

The yoke-north pulse is generated by a contactor whose rotor rotates at yoke speed. The rotor is zeroed with respect to the deflection yoke so that a rotor-mounted shorting pin connects two stationary contacts each time the yoke passes through the yoke-north position. The circuit completed through the contacts and the shorting pin applies a +10V pulse to the grid of RYD 3 of the north synchronizer circuit.

Relays K1, K2, and K3 of the north synchronizer circuit are de-energized throughout approximately 95.8 percent of each cycle so that spurious correction signals cannot develop. The conditioning voltage which allows the circuit to function through approximately 4.2 percent of each cycle is furnished through a reset switch actuated by a cam which, like the yoke-north contactor, is driven at the same speed as the deflection yoke. The

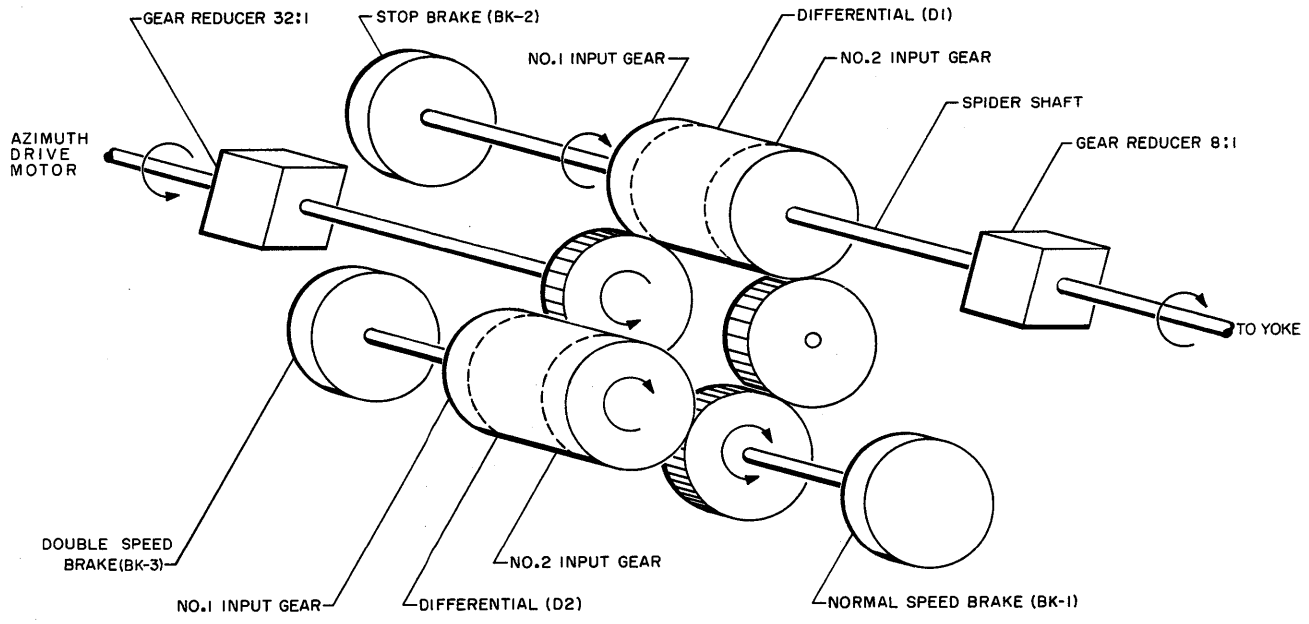


Figure 4–27. Yoke Drive Brake and Differential, Schematic Diagram

cam is aligned with respect to the yoke so that the circuit is made for a period from 10 degrees before yoke north to 5 degrees after yoke north.

6.3.7 Mechanical Operation of Gear Train

The stop and double-speed corrections which maintain the synchronization of the deflection yoke with respect to the antenna are introduced into the deflection yoke drive gear train by means of the system of differentials and brakes, shown in figure 4–27. Each of the two differentials has the property that the speed of its spider shaft is equal to one-half the algebraic sum of the speeds of its two input gears. The No. 1 input gears of both differentials are driven by a common gear which, in turn, is driven through reduction-gearing by the azimuth motor. The deflection yoke is driven through further reduction-gearing by the spider shaft of differential D1. When normal-speed brake BK-1 is energized, the No. 2 input gears of both differentials are stopped. Thus, both spider shafts turn at one-half the No. 1 input speed. Under this condition, the speed reduction from the azimuth motor to the deflection yoke is the normal 256 to 1.

In order to introduce a double-speed correction, BK-1 is released and double-speed brake BK-3 is energized. This stops the spider shaft of differential D2. Thus, the No. 2 input gear of differential D2 turns at -1 times the No. 1 input speed (because the algebraic sum of the speeds of the No. 1 and No. 2 input gears is always equal to the speed of the spider shaft, which, in this case, is zero). The No. 2 input gear of differential D2 drives No. 2 input gear of differential D1 through the two intermediate gears at a speed of $+1$ times the speed of No. 1 input gear of differential D1. Thus, the spider shaft of differential D1 turns at (No. 1 input speed + No. 2 input speed) $= \frac{1}{2}(1 + 1) = 1$. Under this condition, the speed reduction from the azimuth motor to the deflection yoke is only 128 to 1. (This means that the yoke turns at twice the normal speed.)

6.4 AZIMUTH SIGNAL PROTECTION

6.4.1 General

The arrival of a spurious azimuth pulse at the azimuth pulse input line of the counter section would introduce an error into the azimuth and range counts. A missing azimuth pulse would produce the same effect. The purpose of the azimuth protection circuit is to maintain valid azimuth and range counts by inhibiting the introduction of spurious pulses and by replacing missing pulses.

The probability of introduction of spurious pulses is minimized by disabling the azimuth pulse input gate for 88 percent of the azimuth cycle. Missing pulses are replaced by substitute pulses which are generated after each normal pulse occurrence time, but which are gated to the counter input line only when the normal pulse fails to appear.

The action of the protection circuit is as follows. Let the time interval between the normal occurrence time of the nth azimuth pulse and the normal occurrence time of the $(n + 1)$th azimuth pulse be defined as the nth azimuth cycle. Assume that the nth azimuth pulse occurs at its normal time. It is then passed to the counter section and, in addition, is placed in storage in the protection circuit. Two and one-half μsec after the nth occurrence time, the protection circuit disables its

input gate. Thus, spurious pulses are prevented from passing through the circuit.

After 88 percent of the nth azimuth cycle has elapsed, the stored nth pulse is used to condition the gate to pass the $(n + 1)$th azimuth pulse. After 12 percent of the $(n + 1)$th cycle has elapsed, the stored nth pulse is used again to generate a substitute pulse. If the $(n + 1)$th pulse has failed to appear at the normal time, this substitute pulse is gated to the counter section to maintain valid azimuth and range counts and is stored in the protection circuit, where it performs (during the next cycle) the protection functions just described. If the $(n + 1)$th pulse does appear at the normal time, the substitute pulse still appears but it is not gated through the protection circuit.

The action of the azimuth protection circuit requires the storage of the nth azimuth pulse throughout the nth cycle and through 12 percent of the $(n + 1)$th cycle. It requires that the nth pulse be read out of storage after 88 percent of the nth cycle has elapsed and, again, after 12 percent of the $(n + 1)$th cycle has elapsed. It also requires that a substitute pulse (written into storage 12 percent of a cycle later than the time for storing normal pulses) be read as though it were written at the time normal pulses are written. This is accomplished by displacement of the substitute pulse write head, as described in 6.4.2.

6.4.2 Magnetic Drum

The storage functions described above are performed by a magnetic drum in the GFI mapper console. The drum, which is equipped with two write heads, two read heads, and an erase head, is driven by the azimuth motor through reduction-gearing at a speed of 0.8 revolution per azimuth cycle. This rate of revolution permits an azimuth pulse to be stored on the drum throughout the necessary 12 percent of the following azimuth cycle without the bit passing under write head 1 (W1) a second time.

Refer to figure 4–28 for the following discussion. When an azimuth pulse is written onto the drum by write head 1, it must be read by read head 1 (R1) after 88 percent of its cycle. The drum rotates 0.8 of 360 degrees (288 degrees) between azimuth cycles. Therefore, read head 1 must be placed 0.88 of 288 degrees away from write head 1. This corresponds to a displacement of 253.4 degrees.

It is also necessary to read the azimuth pulse after 12 percent of the cycle in order to compensate for missing azimuth pulses. Twelve percent of an azimuth cycle corresponds to 34.6 degrees (0.12 of 288 degrees). Therefore, read head 2 must be advanced 34.6 degrees from the 288-degree position making a total displacement from write head 1 of 322.6 degrees. It has been stated that write head 2 must write a substitute pulse on the drum in the event of a missing azimuth. Write head 2 must be advanced from write head 1 by 12 percent on an azimuth cycle, so that the substitute pulse is located where the missing azimuth pulse would have been. This again corresponds to 34.6 degrees in displacement.

The function of the write and read heads can be summarized as follows. Write head 1 writes azimuth pulses on the drum at the normal time. Write head 2 writes substitute azimuth pulses on the drum after 12 percent of the azimuth cycle. Read head 1 reads an azimuth pulse after 88 percent of an azimuth cycle. Read head 2 reads an azimuth pulse after 112 percent of its azimuth cycle, as part of the procedure of compensating for missing pulses. After passing beneath read head 2, the stored signal passes under an erase head (E) and is thus removed from the drum.

Write heads 1 and 2 are driven by write head drivers (WHD's) which are thyratron tube circuits.

6.4.3 Protection Against Spurious Azimuth Pulses

Protection against spurious azimuth signals is necessary to minimize the effect of telephone-line noise in producing erroneous azimuth and range counts. The azimuth and north signals from the DCR are passed by OR 1 (fig. 4–29) to condition GT 1. A subsequent sync range (OD 2) pulse from the counter section is passed by GT 1 and applied to GT 2. The conditioning level for GT 2 is initially supplied through OR 2 by a d-c level originating in the start circuit. This d-c level is maintained during the starting process and permits passage of initial azimuth pulses. Flip-flop 3 is set to the 1 state by the output of GT 2 and is cleaned by the following OD 4 pulse from conditioned GT 3. Since the interval between OD 2 and OD 4 is 5 μsec,

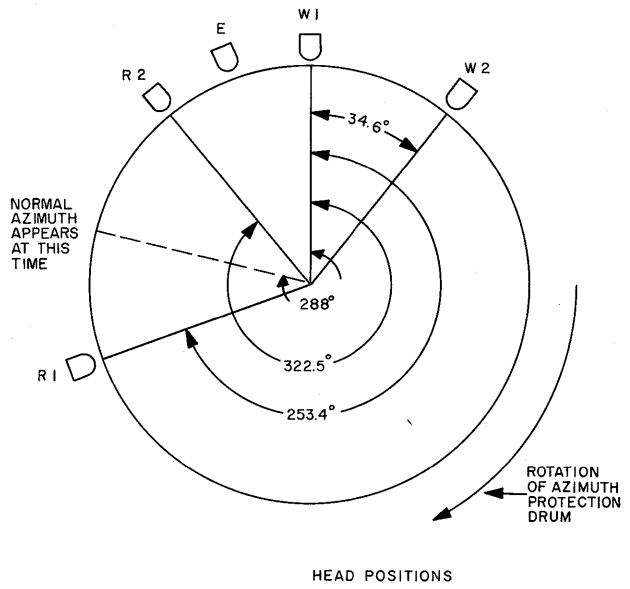


Figure 4–28. Relative Drum Head Positions

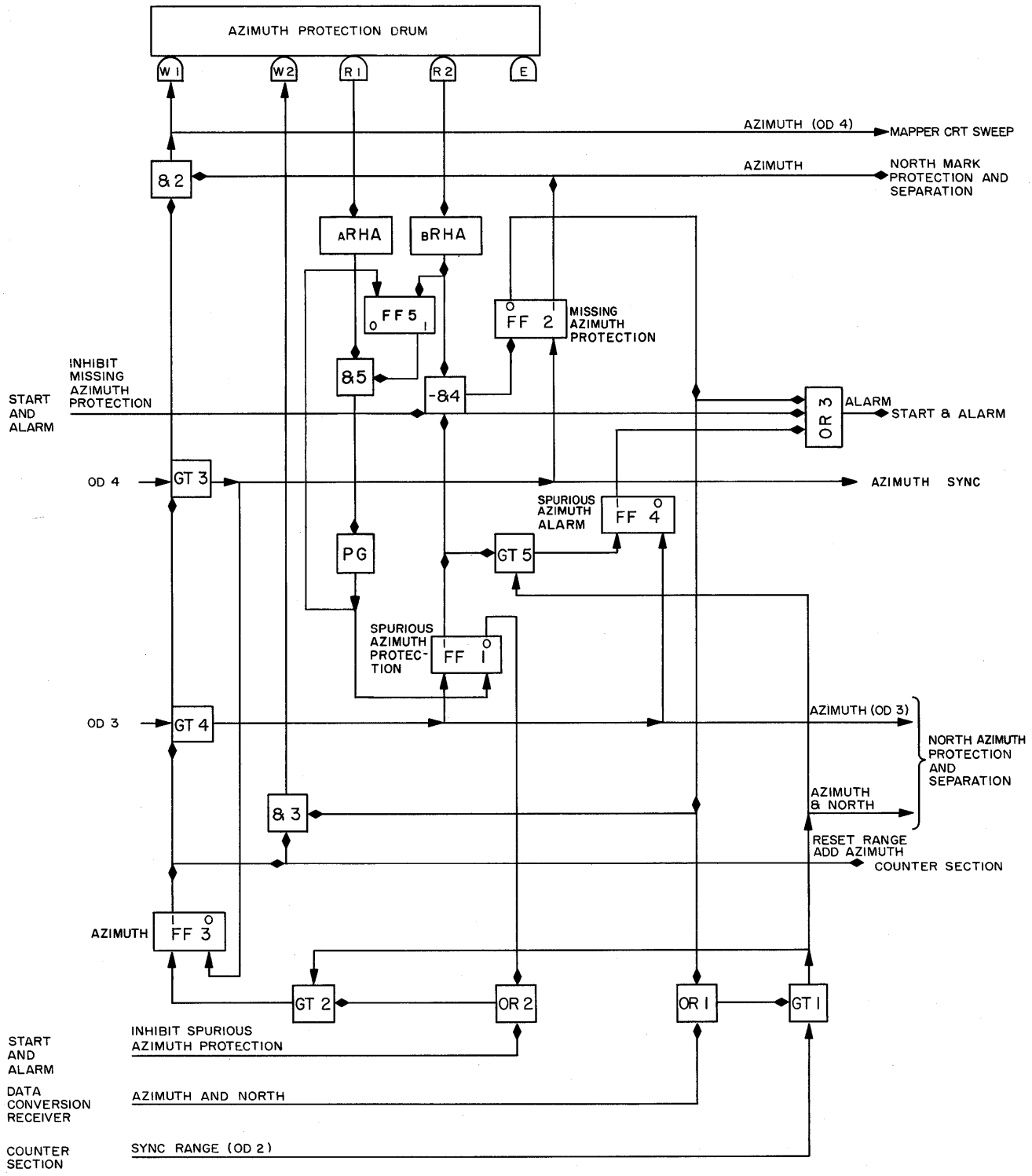


Figure 4–29. Azimuth Protection, Simplified Logic Diagram

the output of FF 3 is a 5-μsec level. This output is sent to the counter section as a reset-range-add-azimuth signal.

The 5-μsec pulses from FF 3 condition GT's 3 and 4. Gate 4 is sampled by the OD 3 pulse, and one of the uses of the resulting output is that of the azimuth pulse in the north separation circuit. Gate 3 is sampled by the OD 4 pulse, and one of the uses of the resulting output is as the azimuth pulse in the azimuth synchronizer circuit. From this point, the circuit is devoted to the suppression of spurious azimuth pulses and to the generation of substitute pulses for missed azimuth pulses. Protection against the appearance of spurious pulses is provided by applying a conditioning voltage to GT 2, which permits azimuth pulses to pass during a relatively short interval of the azimuth cycle. The conditioning voltage which allows the azimuth pulse to pass is caused indirectly by the azimuth pulse of the preceding cycle. This sequence requires a time delay or storage of a signal associated with the preceding cycle pulse. Flip-flop 3, in addition to supplying the reset range-add-azimuth pulse to the counter section, supplies azimuth data through AND 2 to the sweep intensification and focus circuit. This information from AND 2 is also written on the azimuth protection drum through write head 1. The position of read head 1 with respect to write head 1 is such that stored azimuth data is read after 88 percent of the azimuth cycle. The read information produces a positive level at the output of the aRHA which is passed by AND 5, causing the PG to generate a 0.1 μsec pulse, clearing FF 1 and FF 5. Thus, the 0 side of FF 1 conditions GT 2 (through OR 2) after 88 percent of the azimuth cycle.

The conditioning level at GT 2 is terminated when FF 1 is set by an OD 3 pulse from GT 4, after receipt of an azimuth pulse from the DCR. Azimuth pulses passing through GT 2 occur at OD 2 time, and the conditioning level is removed 2.5 μsec later, preventing any closely following azimuth pulses from passing. Because the conditioning level at GT 2 is established only during 12 percent of the azimuth cycle, the passage of spurious azimuth pulses is substantially reduced.

The presence of a spurious azimuth signal from the DCR will cause a signal to be sent to the alarm section of the start and alarm circuit. The spurious azimuth signal sets FF 4 through GT 5, and the resulting output of FF 4 is applied through OR 3 to the start and alarm circuit.

6.4.4 Protection Against Missed Azimuth Pulses

Because an incorrect range and azimuth count in the counter section would result, it is necessary to substitute a pulse when an azimuth signal is missing. A normal azimuth pulse is written on the drum by write head 1. If another azimuth signal has not been received after 112 percent of the azimuth cycle, the following sequence takes place. The position of read head 2 is such, that read head 2 reads the last received pulse after 112 percent of the azimuth cycle. The information read from the drum is applied to —AND 4 through bRHA. The —AND 4 circuit produces a negative output, only when all inputs are negative. The bRHA produces a negative signal, and FF 1, being clear, applies a negative level to —AND 4. The third output from the start circuit is normally an open circuit, except during the start cycle. The effect of this open circuit is the same as a negative input. Consequently, —AND 4 produces an output which is applied to FF 2. Note that every pulse written on the drum is read by read head 2, but the output is utilized only when a an azimuth pulse is missed. When azimuth pulses occur in normal sequence, —AND 4 does not produce a negative output because FF 1 maintains a positive potential on its input to —AND 4.

The negative output of —AND 4 clears FF 2 to the 0 side, conditioning AND 3, OR 1, OR 3. The output of OR 1 conditions GT 1 to pass the following sync range (OD 2) pulse, setting FF 3 through conditioned GT 2. Flip-flop 3 produces the reset-range-add-azimuth pulse which is sent to the counter section to maintain the proper count, although the normal azimuth signal was missing. The output of OR 3 is sent to the start and alarm circuit.

It is necessary for read head 1 to read a pulse from the drum at the proper time in order to maintain the accurate range and azimuth count. Consequently, when an azimuth signal is missing, a substitute pulse must be written on the drum to be read at the proper time by read head 1. AND 3 is conditioned by the cleared output of FF 2 and the set output of FF 3, during generation of the substitute azimuth signal. The output of AND 3 causes the substitute azimuth to be written on the drum by write head 2. This occurs at a time corresponding to 112 percent of the azimuth cycle following the last azimuth signal. The position of write head 2 is such, that the substitute pulse will be read by read head 1 at the same time that the missing pulse would have been read if it had been present.

6.4.5 North Azimuth Protection and Separation

The north azimuth consists of two successive azimuth pulses. The second of the two pulses must be separated and fed to the north synchronizer and counter circuits to perform its assigned functions. Figure 4–30 shows the portion of the protection circuit in which the separation is accomplished. A gated OD 3 timing pulse is passed through GT 1 by the conditioning signal supplied by FF 2 (fig. 4–29). The OD 3 pulse then triggers a single-shot multivibrator (fig. 4–30) to produce a d-c level which is applied to an AND circuit.

The other AND circuit input is received from the north protection and reset cam switch of the north-synchronizing circuit. The north protection and reset cam switch delivers a signal during a time interval representing 10 degrees of azimuth before yoke-north, and 5 degrees of azimuth after yoke north. The AND circuit output then conditions GT 2, which permits passage of only the second of the two azimuth pulses. The output pulse is sent to the north-synchronizing circuit.

6.5 CRT OPERATION

6.5.1 General

The GFI mapper console provides a PPI presentation of the position of targets scanned by an associated GFI radar antenna. The CRT display is developed in terms of polar co-ordinates. The angular component of CRT electron beam deflection is determined by the angular position of a yoke which is rotated about the neck of the CRT at a rate corresponding to the angular rate of the scanning radar antenna. The radial component of electron beam deflection is determined by the instantaneous value of the sweep signal applied to the rotating yoke. This sweep signal is generated by the mapper sweep generator which is fired by each azimuth pulse. If the CRT electron beam were continuously unblanked, it would sweep out 256 azimuth sectors for each complete revolution of the scanning radar antenna. However, the positive-intensity signal is applied to the control grid of the CRT only when the range and azimuth components of beam deflection correspond to the position of a target being scanned by the radar antenna.

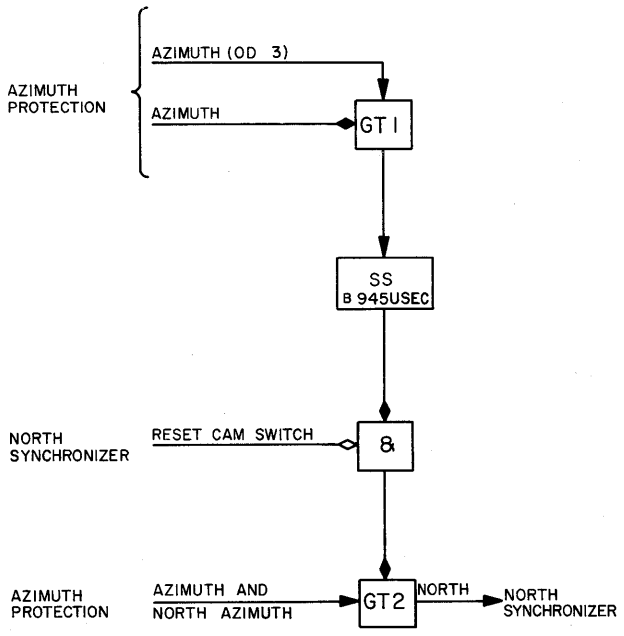


Figure 4–30. North Azimuth Protection and Separation, Simplified Logic Diagram

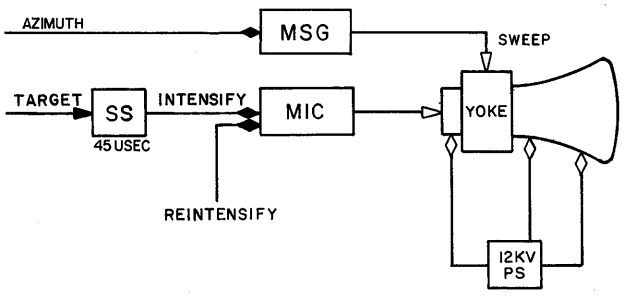


Figure 4–31. Sweep and Intensification Circuits, Simplified Logic Diagram

6.5.2 Radial Sweep

As noted above, each azimuth pulse drives the mapper sweep generator. The mapper sweep generator provides a sawtooth current wave output which drives the deflection coil, as shown in figure 4–31. A d-c clamp circuit is used to establish an initial zero deflection and to limit the length of the sweep.

6.5.3 Intensification

A system of double intensification is used to establish a higher level of brightness for selected targets, than for masked targets. Unsynchronized target pulses are lengthened by a 45-μsec single shot, as shown in figure 4–31. They are then applied to the mapper intensification circuit (MIC), where they are clipped to a preset level and applied to the control grid of the CRT. Those targets which are not masked by the application of mapping fluid to the mapping surface are sensed by the photo-pickup circuit, which applies them to the counter section. In response, the counter section returns a reintensify pulse to the mapper intensification circuit. This pulse is applied to the control grid of CRT through the second input to the mapper intensification circuit. However, the reintensify pulses are not clipped and, therefore, attain a greater positive magnitude, with the result that the unmasked target spots are brightened. Thus, the operator can determine from the brightness of the display which target pulses are actually reaching the counter section.

6.5.4 Focus

The voltage applied to the focus electrode of the CRT has a nominal value of 4 kv. The voltage is taken from the arm of a potentiometer in the power supply, thus providing a means of adjusting the focus of the CRT.

6.6. PHOTO PICKUP

The photo-pickup circuit senses unmasked target pulses appearing on the CRT screen and amplifies these pulses for use in the counter section. The circuit is shown in figure 4–32.

The light spots, representing targets, on the CRT-screen consist of two components: the blue fluorescence

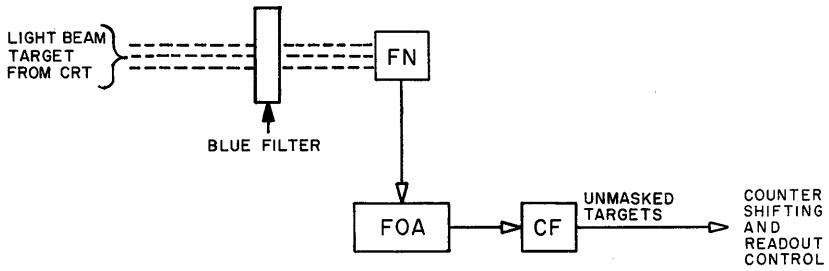


Figure 4–32. Photo Pickup, Simplified Logic Diagram

which appears while the screen is being excited by an electron beam, and the yellow phosphorescence which persists after the excitation has ceased. The photo-pickup circuit responds only to the blue fluorescence. Thus, targets can be masked by applying yellow mapping fluid to the region of the mapping surface where the targets appear. The mapping fluid blocks the blue fluorescence but passes the yellow phosphorescence so that the target remains visible to the operator.

In order to make the photo-pickup circuit respond to the blue fluorescence only, a photomultiplier tube (FN) which has its peak response in the blue region of the spectrum is used, and a blue filter is added to the viewing aperture through which the beam of light from the CRT reaches the photomultiplier tube.

The output of the photomultiplier tube is a negative pulse which feeds the photo-pickup amplifier (FOA). The amplifier amplifies and inverts this pulse to drive the cathode follower. The output from the cathode follower is a positive level corresponding to pickup of a target and is a negative (—30V) level when no target is being picked up. This output is applied to the counter section, causing the readout of azimuth and range pulses from the counters to the registers.

6.7 START AND ALARM LOGIC

Since many of the same relays function in connection with both start and alarm operations, the start and alarm circuits are shown together in figure 4–33. The functions of the individual relays are described as follows. Relay K11 connects the 34V, 60-cycle line to the azimuth motor for starting or it connects the azimuth synchronizer output to the azimuth motor for synchronous operation. Thermal time-delay relay K14, which with relay K17 controls the energization of relay K13, maintains energization of K13 for a fixed period of time after K11 is de-energized. This is for the purpose of disabling a portion of the alarm circuitry until the deflection yoke has had time to become synchronized with the scanning radar antenna. Relay K7 initiates an alarm operation in response to a certain number of either missing or spurious azimuth pulses or to the failure of the azimuth motor to come into synchronization with the radar antenna information. Relay K9 indicates an alarm operation under the control of circuitry in the Central Computer. Relay K16 initiates an alarm condition in response to an excess in the quantity of target information received from the radar site. Relay K8 functions to disable the audible alarm which is sounded as part of any alarm operation. Relay K8 is controlled by a pushbutton. Relays K10 and K12 function to prevent the readout of range and azimuth data to the Drum System when the deflection yoke is not in synchronization with the scanning radar antenna. These relays inhibit data during the period of a stop correction. On the other hand, after any alarm condition or after the power has been turned off, it is necessary to depress a pushbutton in order to resume the passage of target data to the counter section. The start and alarm operations are discussed in detail below in terms of figure 4–33.

6.7.1 Start Circuit

The start operation following a power-off condition is as follows. When the power is supplied to the console, it is applied to the coil of relay K15 through the normally closed contacts of the low-speed centrifugal switch. Relay K15 energizes, thus connecting the input of the alarm analog counter (BAC) to the azimuth and north line from the DCR and also connecting the output of the counter to the coil of relay K11. Azimuth and north-azimuth pulses appearing on the input line actuate the analog counter, causing the relay driver to conduct and thus energize relay K11. Contacts 4 and 5 of relay K11 complete a hold circuit through the normally closed contacts of the high-speed centrifugal switch to ground; contacts 2 and 3 connect the 34V, 60-cycle line to the azimuth synchronizer phase splitter in the motor drive circuit; contacts 7 and 8 connect +10V to the inhibit spurious azimuth protection line; contacts 9 and 10 (not shown) connect the —48V return line to the coil of relay K17.

The connection of the 34V, 60-cycle line to the phase splitter places a driving voltage of line frequency on the azimuth motor, and the motor starts. The +10V supplied to the inhibit spurious azimuth protection line

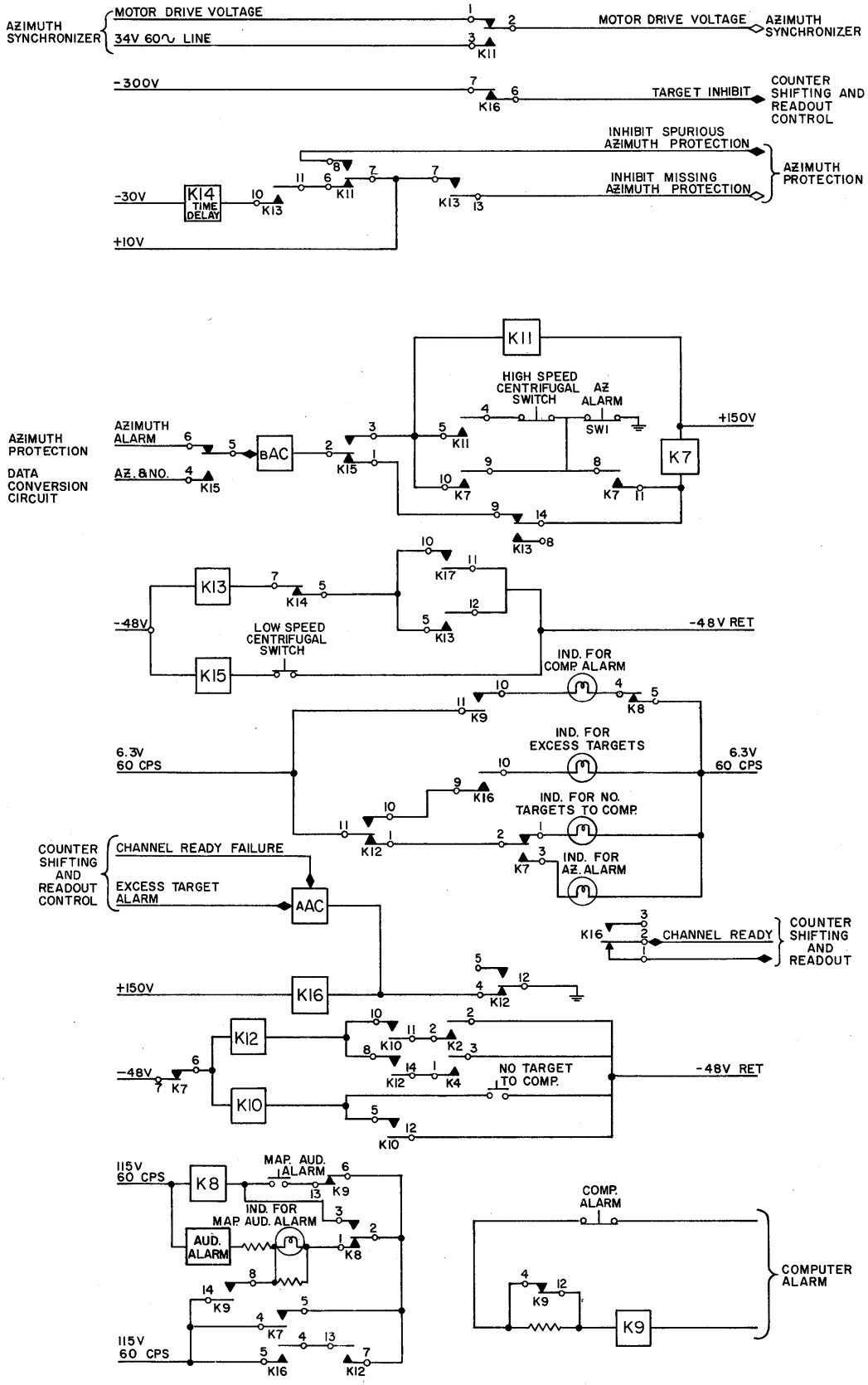


Figure 4–33. Start and Alarm Circuit, Simplified Logic Diagram

conditions GT 2 in the azimuth protection circuit (fig. 4–29), which passes the initial azimuth pulse necessary to write a bit on the drum; this will allow the azimuth protection circuit to function after normal speed is attained. At the same time, relay K13 is energized by the application of the —48V return line to its coil circuit.

Contacts 5 and 12 of relay K13 set up a hold circuit; contacts 9 and 14 open the coil circuit of alarm relay K7 so that an alarm will be initiated during the start operation; contacts 7 and 13 apply +10V to the inhibit-missing-azimuth-protection line. This inhibit voltage prevents the generation of a missing azimuth alarm pror to the synchronization of the azimuth signal with the incoming radar data.

When the azimuth motor reaches a speed of 512 rpm, the low-speed centrifugal switch opens, causing relay K15 to de-energize. Contacts 5 and 6 of relay K15 thus connect the analog counter to receive alarm information.

When the azimuth motor reaches a speed of 3,200 rpm, the high-speed centrifugal switch opens, breaking the hold circuit of relay K11. When K11 de-energizes, contacts 1 and 2 place the azimuth phase splitter in the motor drive section under the control of the Miller integrator of the azimuth synchronizer and initiate synchronized operation. Contacts 6 and 7 place +10V on the coil of thermal relay K14 through contacts 10 and 11 of K13. After providing sufficient delay to allow the deflection yoke to be brought into synchronization with the associated radar antenna, relay K14 energizes, opening the hold circuit for relay K13. Relay K13 then de-energizes, completing the start cycle. Relay K7 is now connected to the output of the analog counter through contacts 9 and 14 of K13 and contacts 1 and 2 of K15 so that it will be actuated by any alarm information generated by the counter.

Although the starting cycle is complete, target information is still prevented from entering the counter section for the following reason. When power was removed from the console, relays K10 and K12 were de-energized. The return of power to the console does not cause either relay to energize, since relay K12 is energized through normally open contacts 10 and 11 of relay K10, while relay K10 in turn is energized through the normally open contacts of the NO TARGET TO COMP pushbutton. Thus, relay K16 is energized by the ground applied to it through normally closed contacts 4 and 12 of relay K12. With relay K16 energized, the channel ready level and the —300V target inhibit level are not applied to the counter section. It is the absence of these levels which prevent the readout of target data from the counter section to the Drum System. If the NO TARGET TO COMP pushbutton is depressed, relay K10 will energize and establish a hold circuit through contacts 5 and 12. If deflection yoke-north is synchronized with radar north, contacts 1 and 2 of relay K2 provide a momentary —48V return to the coil of relay K12 through contacts 10 and 11 of energized relay 10. If the yoke is being driven at normal speed, relay K12 completes a hold circuit through contacts 1 and 3 of energized relay K4 in the north synchronizer circuit. Relay K16 will now de-energize, allowing the —300V inhibit level to be passed to the counter section through contacts 6 and 7 and the channel ready level to be passed by contacts 1 and 2, which, in turn, allows the readout of the azimuth and range registers.

The arrival of a yoke-north pulse before the arrival of a radar-north pulse will be sensed by the north synchronizer as an early yoke-north condition; response to this condition causes relay K4 to de-energize. This will stop the deflection yoke until it receives a radar-north pulse. It will also remove the hold voltage from relay K12. Thus, relay K12 will de-energize. Under this condition, however, relay K10 will remain energized. Upon the arrival of a radar-north pulse, the north synchronizer will energize relay K4 and, if the yoke is properly synchronized with respect to this new radar data, relay K12 will receive an energizing signal through contacts 10 and 11 of energized relay K10.

6.7.2 Alarm Circuit

The alarm circuit provides audible and visual alarm indications in response to azimuth, excess-target, or central-computer-alarm signals. A predetermined number of azimuth alarm inputs to the BAC causes it to give an output which energizes relay K7 through contacts 1 and 2 of relay K15 and contacts 9 and 14 of relay K13. Relay K7 connects 115V to the audible alarm through the normally closed contacts of relay K8 and, in addition, energizes relay K11, initiating the start cycle. With relay K7 energized, the start cycle is modified by the fact that the high-speed centrifugal switch is bypassed. Thus, as long as relay K7 is energized, the azimuth motor is driven by the 34V, 60-cycle line. When the alarm condition has been removed, relay K7 can be disabled by depressing the normally closed AZIMUTH ALARM INDICATOR glow button (switch 1). This breaks the hold circuit of relay K7 so that the start cycle can be completed and control of the azimuth motor returned to the azimuth synchronizer circuit. Note that, when relay K7 energizes, it opens the coil circuit of relays K10 and K12. Thus, a restart after an azimuth alarm condition necessitates depression of the NO TARGET TO COMP button to cause the resumption of target data flow to the Drum System. In this respect, it resembles a restart after a power-off condition.

The presence of excess target data at the input to the AAC actuates the counter, causing the relay driver to conduct and thus energizing relay K16. This places 6.3V across the EXCESS TARGETS lamp and 115V across the audible alarm. Relay K16 de-energizes when the alarm condition is removed.

When the Central Computer has found something radically wrong with the GFI data it is processing, an alarm signal is applied across the coil of relay K9. Relay K9 energizes, placing 6.3V across the INDICATOR FOR COMPUTER ALARM and 115V across the audible alarm. A normally closed pushbutton in the hold circuit of relay K9 allows K9 to be disabled locally.

When the audible alarm is sounded in response to either an azimuth or an excess target alarm input, it can be silenced by momentarily depressing the MAPPER AUDIBLE ALARM button. This completes the coil circuit of relay K8 which, in turn, picks up and breaks the circuit of the audible alarm. Notice that an alarm signal from the computer causes the 115V line to be applied to the audible alarm directly, so that a computer-actuated alarm cannot be silenced by depressing the MAPPER AUDIBLE ALARM button.

PART 5
CROSSTELL INPUT ELEMENT

CHAPTER 1
INTRODUCTION

1.1 GENERAL

This part describes the operation of the crosstell (XTL) element. The XTL element being an intermediate data-processing agent, signal and data flow relationships with other systems are described, but only to the extent required for use in the operation of the XTL element.

1.2 FUNCTION OF XTL INPUT ELEMENT

Crosstelling refers to the exchange of information between AN/FSQ-8 Combat Control Centrals and between AN/FSQ-7 Combat Direction Centrals. In this exchange of information, the XTL element functions as the information-processing element at the receiving Central. In the exchange of information between a Central and a higher echelon (forward-telling) or between a Central and a lower echelon (back-telling), the XTL input element functions in the same manner as in crosstelling. Accordingly, no distinction is made in this part of the manual between the three types of message transfer. Only crosstelling is discussed and, unless otherwise indicated, the discussion applies equally to forward-telling and back-telling.

In all cases, the function of the XTL elements is to receive, serially and at a relatively slow speed, information originating at other Centrals. The information is processed, temporarily stored, and, when a slot is available on the MIXD drum, transferred to the Drum System by the XTL element. The transfer to the Drum System is accomplished at relatively high speed in parallel form.

1.3 RELATIONSHIP OF XTL ELEMENT TO INFORMATION SOURCES

The flow of data between two Centrals is shown in figure 5–1. Transmission of information between Cen-

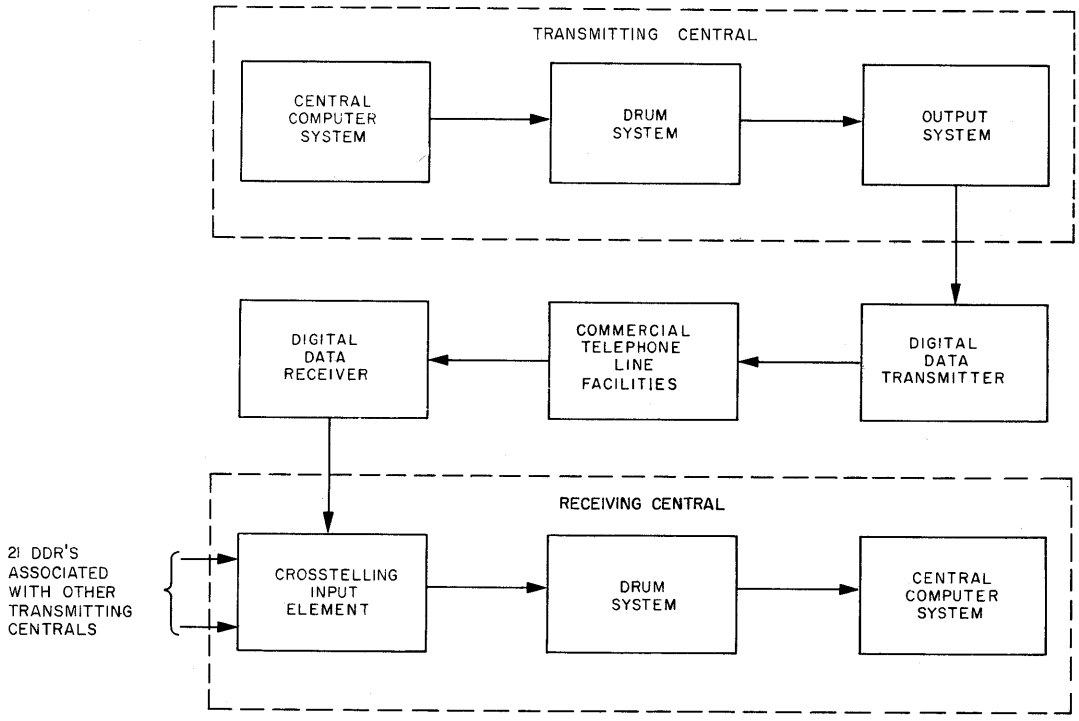


Figure 5–1. Crosstelling Between Centrals

trals is accomplished by commercial telephone facilities which include digital data transmitters (DDT's), commercial-type telephone lines, and digital data receivers (DDR's). The message is formulated in the Central Computer, Drum, and Output Systems of the transmitting Central and is sent to a DDT. The DDT converts the message into a form which permits transmission of the message over the commercial-type telephone lines. The DDR at the receiving Central forwards the message to the XTL element in a form which is adaptable for processing by the XTL element. The message is then processed by the XTL element and by the Drum and Central Computer Systems. One Central may transmit a message simultaneously to several other Centrals. Since a message may be intended for a specific Central, an address is incorporated in the message, denoting the intended receiver. A Central may receive information from up to a maximum of 22 other Centrals; some Centrals receive information from a maximum of 11 Centrals.

1.4 PHYSICAL DESCRIPTION

1.4.1 Twenty-Four-Channel Installations

The XTL element is contained in unit 32, 16 modules of which are shown in figure 5–2. Four of these modules are associated with the common equipment, two with common A and two with common B. Each of the remaining 12 modules contains circuitry for a particular channel, with module F containing the circuitry for spare channel 6. Up to a maximum of 12 additional modules may be included (or added), giving the element the capacity to process information from up to a maximum of 22 Centrals. The module corresponding to channel 13 contains the spare channel circuitry for the additional channels. The additional modules are located adjacent to the modules shown in figure 5–2.

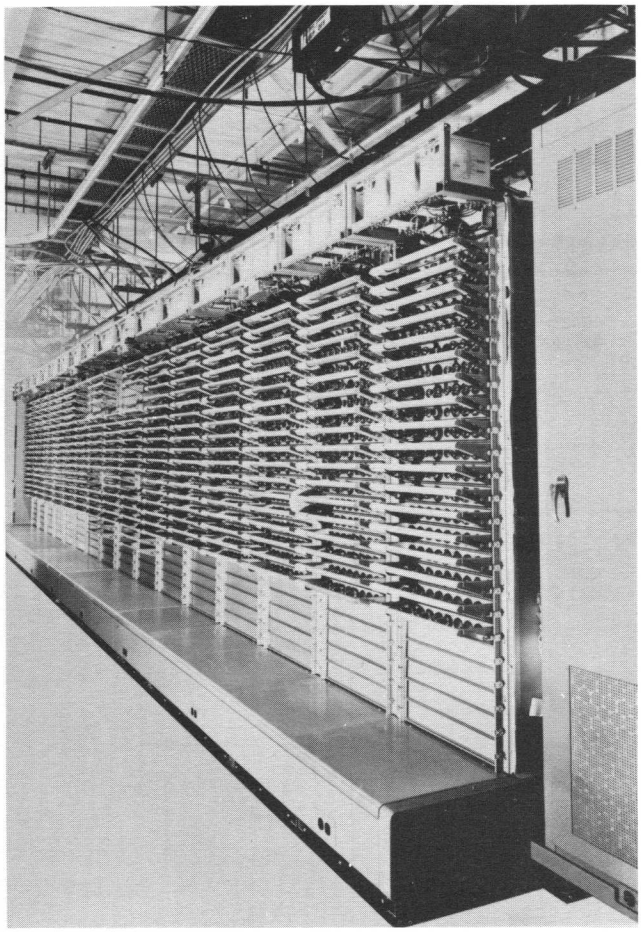


Figure 5–2. XTL Element, Unit 32

Controls and indicators for the simplex channel equipment are located on the simplex maintenance console, unit 47. Indicators for the duplex equipment are located on the associated duplex maintenance console, unit 1 A or 1 B.

1.4.2 Twelve-Channel Installation

When information is to be received from 11 or less other Centrals, the LRI circuitry is contained in the modules shown in figure 5–2.

1.5 MESSAGE LAYOUT

The XTL message consists of five 17-bit words, each word consisting of 16 information bits and a parity bit. Prior to transmission, in the Output System of the Central transmitting the message, the bits of each of the five words are serially interleaved, with the first bit of each word transmitted in succession, followed by the second bit of each word, etc. The interleaving process improves the efficiency of parity checking by reducing the probability of transmission errors in successive bits of a word and thereby reducing the probability of correct parity indication for a word with compensating errors.

The bits occur in synchronism with 1,300-pulse-per-second (pps) timing pulses. A total of 92 timing pulses are employed in a complete XTL message, thus establishing the message period at 92/1,300 of a second. The relationship of the timing pulses, interleaved message bits, and message words is shown in table 5–1. A sync bit, which is synchronized with the first timing pulse, precedes the data bits, which start with the fourth timing pulse.

The XTL element receives the XTL message, reconstructs the five message words, and adds additional data to form three 33-bit drum words shown in figure 5–3. The drum words are then written on the XTL field of the MIXD drum for subsequent transfer to the Central Computer System.

1.6 GENERAL FUNCTIONAL DESCRIPTION

1.6.1 Twenty-Four-Channel Installation

The XTL input element, shown in block diagram form in figure 5–4, consists of an input switching section, a 24-channel input section (only one channel sec-

tion is shown in fig. 5–4), a duplex switching section, and a duplex drum input (common) section. These sections are discussed briefly below and in detail in the following chapters.

1.6.1.1 Input Switching

The input switching section contains the controls, relays, indicators, and associated circuitry necessary to perform the following functions:

a. Establish the status (active or standby) of each channel

b. Apply incoming phone line data to active channels and test data to standby channels when desired

c. Substitute a spare channel for another channel within a group

d. Provide indications at the simplex maintenance console to monitor the above functions

1.6.1.2 Channel Input Section

The channel input section encompasses a portion of all 24 channels. Normally, the operation of only one channel at a time is discussed. The term, channel input section, is generally not used collectively; it refers to the channel input section portion of one channel.

The channel input section receives timing, sync, and data inputs constituting the XTL message (or analogous test signals from the test pattern generator) over three separate lines from its associated DDR and composes the message into five 17-bit words. It also receives an XTL drum-demand pulse from the Drum System informing the channel input section that a slot in the XTL drum field is prepared to accept the message. If a message has not been prepared by the channel, the drum-demand pulse is sent to the next channel. The process continues until a channel is found that contains a message or until all channels have been sampled. Transfer of the message to the drum input section then occurs. Accompanying the transfer are certain pulses and levels relating to the validity of the message. A good-message level indicates that the message was intended for the receiving Central (correct address) and that the message words all have correct (even) parity.

Three alarm pulses may be generated in the channel input section: the parity-alarm pulse, indicating incorrect message word parity; readout-alarm pulse, indicating that an overlap of messages in the channel input section has occurred, causing the first message to be destroyed; and a channel-ready-alarm pulse, indicating a malfunction of the channel-ready flip-flop and the possibility of transferring information from two channels at one time.

TABLE 5–1. INTERLEAVED XTL MESSAGE

TIMING PULSE	MESSAGE WORD	MESSAGE WORD BIT
1	—	Sync
2	—	—
3	—	—
4	1	1
5	2	1
6	3	1
7	4	1
8	5	1
9	1	2
10	2	2
11	3	2
12	4	2
13	5	2
14	1	3
15	2	3
16 through 80	—	—
81	3	16
82	4	16
83	5	16
84	1	17
85	2	17
86	3	17
87	4	17
88	5	17
89	—	—
90	—	—
91	—	—
92	—	—

1.6.1.3 Duplex Switching Section

The duplex switching section transfers the output of the channel input section to the drum input (common) section A or B, depending on the status, active or standby, of the channel and of the A and B machines. The output of a channel in the active status is transferred to the common section, A or B, associated with

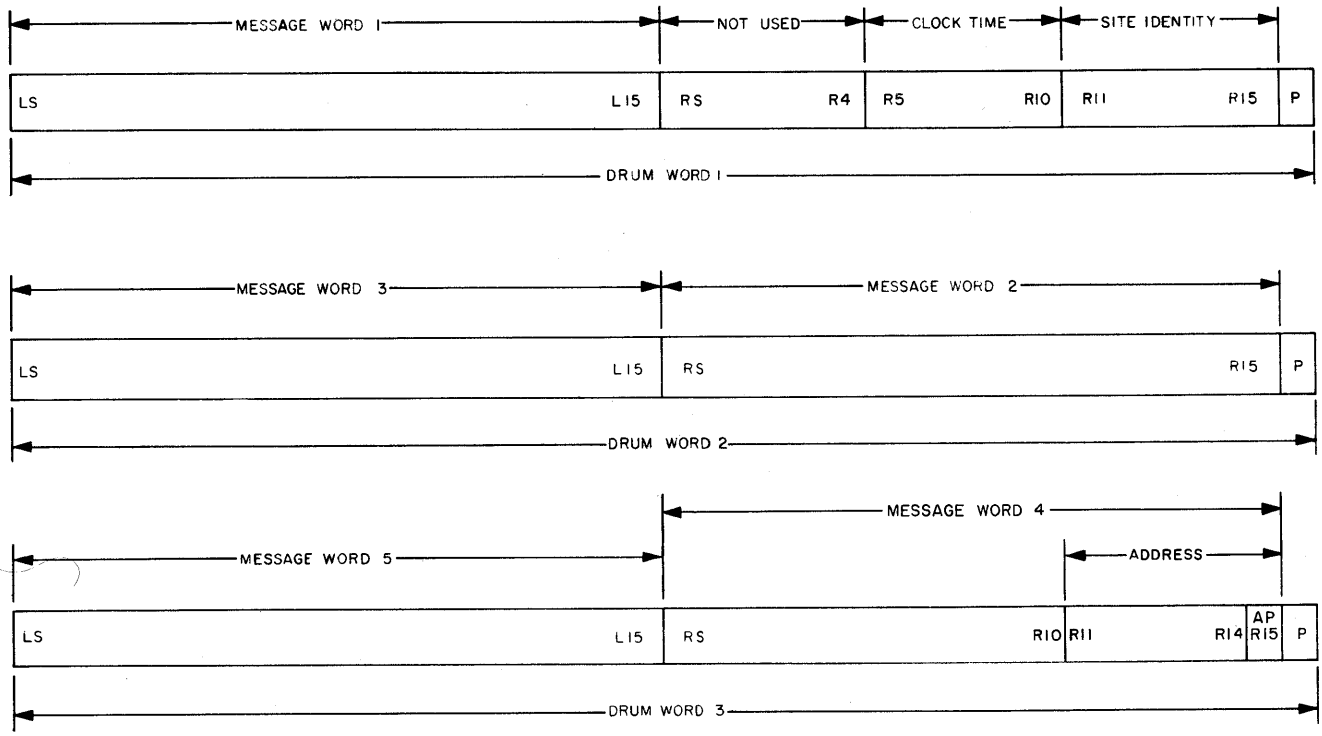


Figure 5–3. Crosstell Message in Drum System

the active machine. Certain timing pulses and levels are also transferred, through duplex switching from the A and B drum input section, to the appropriate channels; other pulses and levels, such as the good-message signal, are transferred in the reverse direction.

1.6.1.4 Drum Input (Common) Section

The drum input (common) section is utilized by all channels and is duplex (fig. 5–4). It receives, on a channel priority basis, the 5-word message, accompanying pulses and levels, and, if present, alarm indications developed in the channel input section. It also receives OD timing pulses from the Drum System and real-time pulses from the Central Computer real-time clock.

The drum input section adds identification of the site at which the message originated, Central Computer clock time, and drum-word parity to the message it receives from the channel input section, and transfers the message as three 33-bit words to the Drum System. It utilizes the OD timing pulses from the Drum System to synchronize XTL operations with those of other parts of the Central, generating from the OD pulses additional timing pulses and levels required by the channel input section. It also indicates alarm conditions, if present, at the duplex maintenance console.

1.6.2 Twelve-Channel Installation

A 12-channel installation is employed at a receiving Central when information is to be received from 11 or less other Centrals. The operation and circuitry is essentially the same as that for Centrals of larger XTL channel capacity. However, the channel input and switching circuitry of unused channels is omitted and the related simplex maintenance console channel control panels are not used. Spare channel 6 is provided regardless of the number of channels employed.

1.7 SIMPLEX MAINTENANCE CONSOLE XTL CONTROL PANELS

1.7.1 General

There are 24 XTL control panels located in the upper sections of modules A, B, C, and D of the simplex maintenance console (unit 47). Each panel is made up of alarm, power control, data circuit, and neon indicator sections as shown in figure 5–5. Two of the panels (corresponding to channels 6 and 13) are spares and contain a channel selector section in addition to sections common to all panels. Only the switches on the panels are discussed as related to input switching.

1.7.2 Function of XTL Control Panel Switches

The unit status switch in the power control section of each XTL control panel determines the status (active or standby) of the channel. With the switch set to ACTIVE, the related channel is connected to the active computer. Only phone line data can be processed when the switch is set to the ACTIVE position. In the STANDBY (or STANDBY MC) position, the channel is connected to the standby computer; in this position,

either phone line data or test data may be processed.

There are three switches, in the data circuit section of the panel, concerned with data flow: the data source switch, the data circuit switch, and the parity disable switch. In conjunction with the unit status switch, the data source switch selects the source from which data is to be received. With the switch set to DATA CIRCUIT, the channel receives data on phone line circuits from other Centrals. In the off position, the channel is inactive, and data is not received or processed. In the TEST position, data is received from the test pattern generator (TPG) to permit testing of channel operations in maintenance procedures. To prevent test data from entering the active computer, the test position of the switch functions only when the unit status switch (power control section) is set to the STANDBY or STANDBY MC position. The data circuit switch is used to select one of two phone line circuits which feed data to the XTL channel. With the switch set to AUTO, telephone company equipment automatically selects the proper circuit. Either circuit can be manually selected by setting the switch to the CIRCUIT 1 or CIRCUIT 2 position. The parity disable switch has two positions: off and PARITY DISABLED. In the off position, channel operation is normal – a message with incorrect parity is discarded. In the PARITY DISABLED position, test messages can be processed without regard to message parity.

The CHANNEL SELECTOR switch, which appears only on the panels corresponding to channel 6 and 13, is used to electrically substitute the spare channel for any of the channels within a group. Spare channel 6 can be substituted for channels 1 through 5 or 7 through 12. Channel 13 can be substituted for channels 14 through 24.

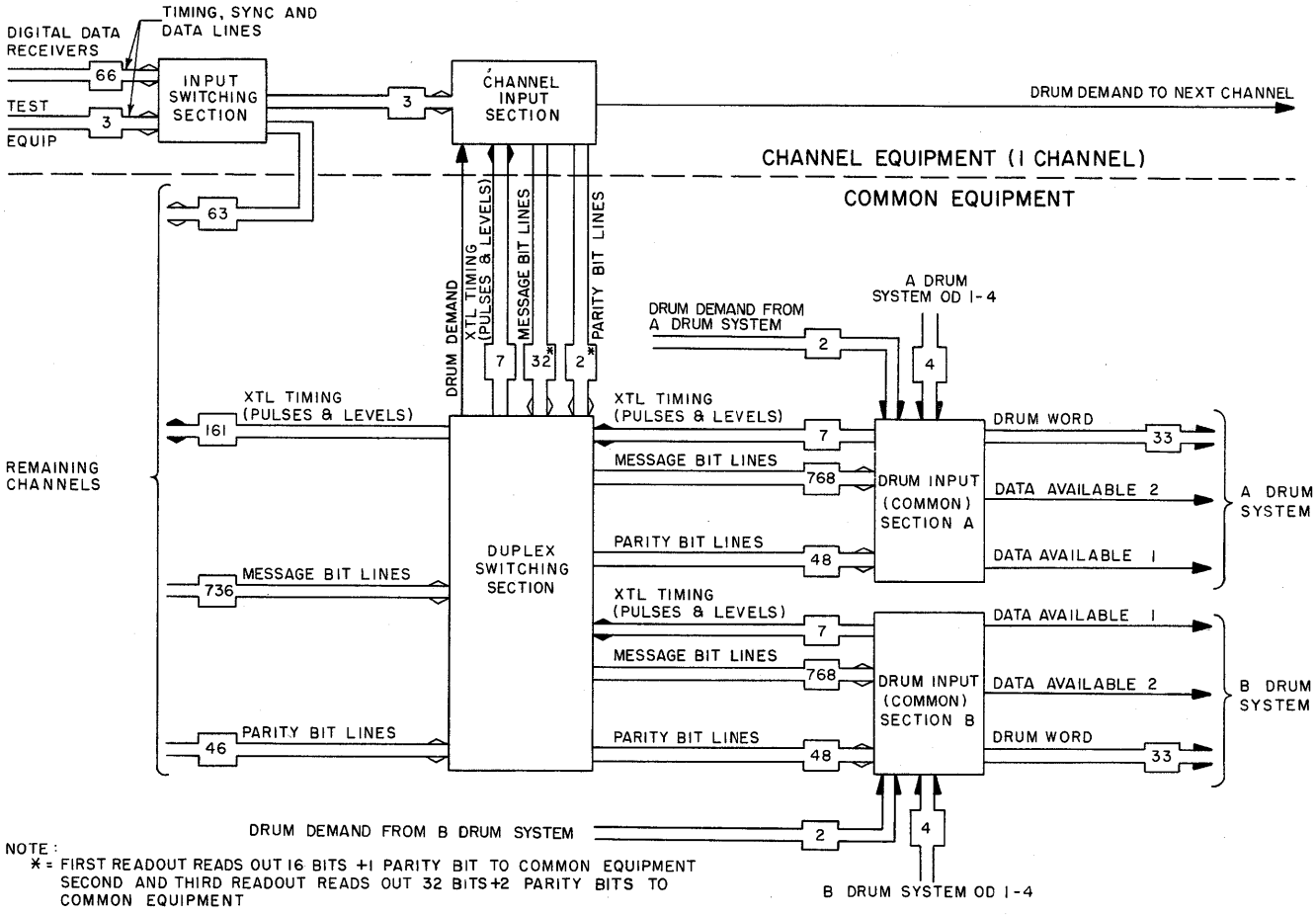
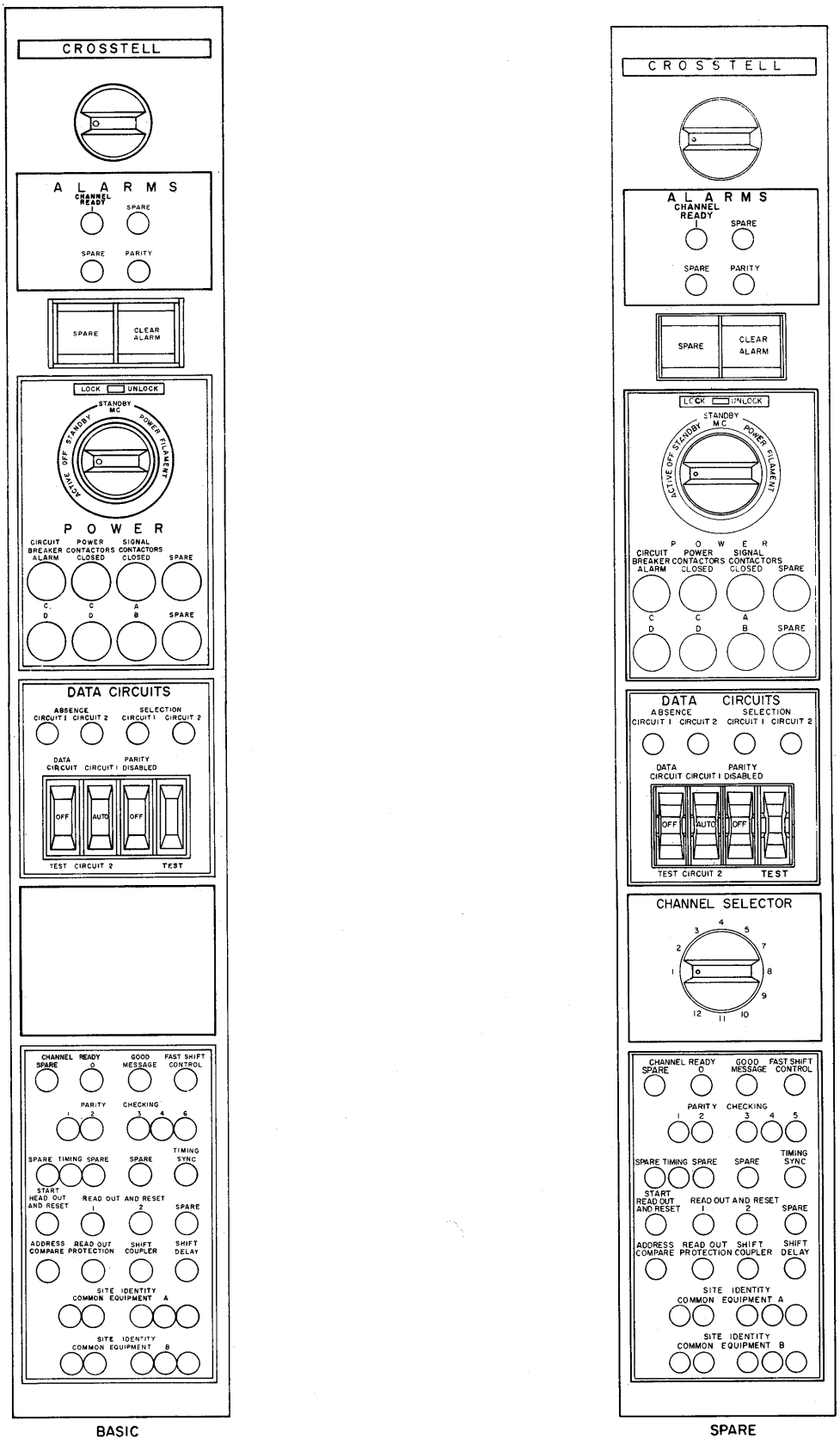


Figure 5–4. Crosstell Element, Block Diagram



BASIC SPARE

Figure 5–5. Crosstell Panels, Simplex Maintenance Console

CHAPTER 2
INPUT SWITCHING

2.1 GENERAL

A Central may contain a maximum of 24 XTL channels. However, it can receive information from a maximum of 22 other Centrals, since two of the channels are spares. A total of six telephone input lines are provided for each channel normally in use. These lines are divided into two circuit groups, designated circuit 1 and circuit 2, each group being made up of timing, sync, and data lines.

The XTL message for each channel is carried by both circuits. One circuit, selected by the data circuit switch on the XTL control panel, is connected to the channel input section; the alternate circuit is then available to the spare channel. For example, when the data circuit switch on the channel 1 control panel is set to CIRCUIT 1, circuit 1 is connected to channel 1 and circuit 2 is available for use by the spare channel. When the switch is in the AUTO position, phone line equipment not part of the (Central) determines whether circuit 1 or 2 will be made available to the channel input section.

Note

In a Combat Control Central at a combined site (Combat Control Central adjacent to a Combat Direction Central), only one phone line is provided for channel 5. Consequently, the data circuit switch is not employed.

In addition to the phone line circuits, a test circuit is available to each channel input section. The test circuit consists of three lines (timing, sync, and data) connected to the TPG through a test bus for each line. When the source switch on the XTL channel control panel is set to TEST (and the channel is in the standby status), the output of the TPG is applied to the channel input section. When the switch is in the DATA CIRCUIT position, phone line inputs are available (from either circuit 1 or 2) to the channel input section.

The switching functions discussed above are performed by the input switching section which also provides suitable monitoring indications at the channel control panels. The input switching section may be regarded as the connecting of two interrelated subsections: input data switching and spare channel switching. The input data switching circuit selects phone-line or test data as the input to the individual channels. The spare-channel switching circuits perform the various operations required to substitute a spare channel for one of the other 11 channels. In subsequent spare channel considerations, although only channel 6 is discussed as a spare for channels 1 through 5 and 7 through 12, the discussion applies equally for channel 13, as a spare for channels 14 through 24, except for references to specific contact designations, relays, terminals, etc.

2.2 INPUT DATA SWITCHING

The relationship of the unit status switch and source switch for channel 1 is shown in figure 5–6. The circuit applies to all other channels except channels 6 and 13, the spare channels.

Placing the source switch in the DATA position causes 32AF(K2) to be energized regardless of the position of the unit status switch. Phone line data is thereby applied to the channel input section. (The phone line data will be carried on circuit 1 or 2, depending on the position of the data circuit switch and associated phone line circuitry.)

When the unit status switch is placed in the STANDBY or STANDBY MC position, 32AG(K8) is energized, providing a —48V return for 32AF(K1). When the source switch is placed in the TEST position, 32AF(K1) is energized, applying test signals (from the XTL TPG) to the channel input section. The purpose of this interlock is to prevent test signals from being applied to an active channel and thus read into the Central Computer.

2.3 SPARE CHANNEL SWITCHING

2.3.1 General

Spare channel switching is the operation of electrically substituting a spare channel, channel 6 or channel 13, for one of the 11 other channels. It is accomplished by setting the CHANNEL SELECTOR switch (on the spare channel control panel, simplex maintenance console) to the number of the channel to be replaced. Three functions are thereby performed:

a. The alternate telephone circuit for the replaced channel is connected to the spare channel.

b. The telephone-terminal-equipment indicators of the spare channel are substituted for these indicators on the replaced channel.

c. A write level, generated in a spare channel, is applied to the site can of the replaced channel. (A write level causes readout of site identity by a site can to associate the source of a message with the message data. In spare channel operations, it is necessary to associate the site identity of the replaced channel with the information processed by the spare channel.)

In the discussion of *a* and *b*, it is assumed that spare channel 6 has been substituted for channel 1. Function c is discussed in Chapter 4.

2.3.2. Alternate Telephone Line Switching

Setting the CHANNEL SELECTOR switch (shown in fig. 5–7, A) to position 1, causes energization of relays 32FD(K1), 32FG(K1), and 32FP(K1). With the switch in this position, alternate telephone line data, whichever is selected at the moment, is applied to the contacts of relay 32FF(K2) through transferred contacts on 32FP(K1) as shown in figure 7, B. If the channel 6 source switch is in the DATA CIRCUIT position, 32FF(K2) is energized, and the alternate telephone data is applied to the channel 6 input section.

2.3.3 Switching of Basic Telephone-Terminal Indications

Telephone line and terminal facilities are not part of the AN/FSQ —7 or —8 but are monitored to ensure proper operation of the Central. Each XTL control panel mounts indicators to show which phone line circuit is connected to the channel input section (SELECTION, CIRCUIT 1, and CIRCUIT 2) and whether there has been a loss of data on a circuit (ABSENCE, CIRCUIT 1, and CIRCUIT 2). When the spare channel is substituted for another channel, the indicators on the spare channel are also substituted, as described below, for the indicators on the replaced channel.

Placing the CHANNEL SELECTOR switch in position 1 causes relay 32FG(K1) to be energized. Four lines from unit 97 (telephone terminal equipment) (shown in fig. 5–7,C) are thereby connected to appropriate indicators on the spare channel control panel: the channel 1, circuit 1 indication line to the SELECTION CIRCUIT 1 light; the channel 1, circuit 2 indication line to the SELECTION CIRCUIT 2 light; the channel 1, absence circuit 1 line to the ABSENCE CIRCUIT 1 light; and the channel 1, absence circuit 2 line to the ABSENCE CIRCUIT 2 light.

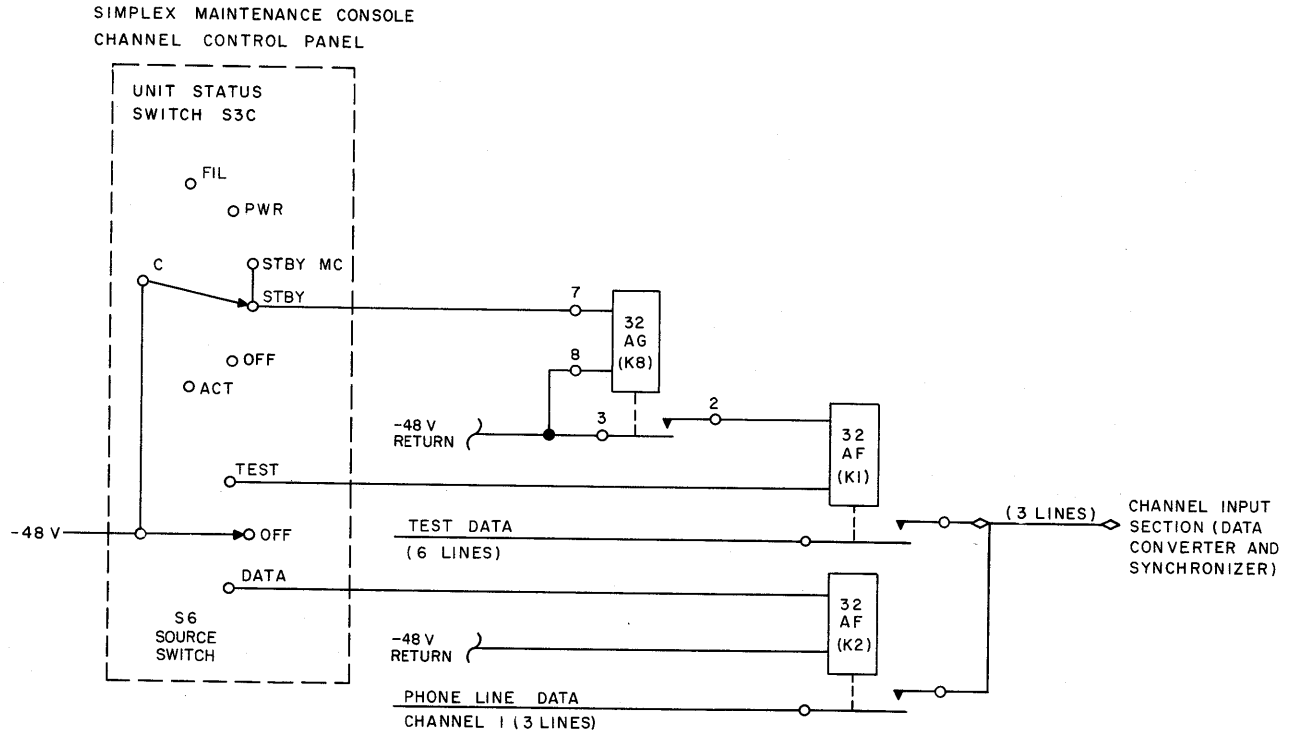
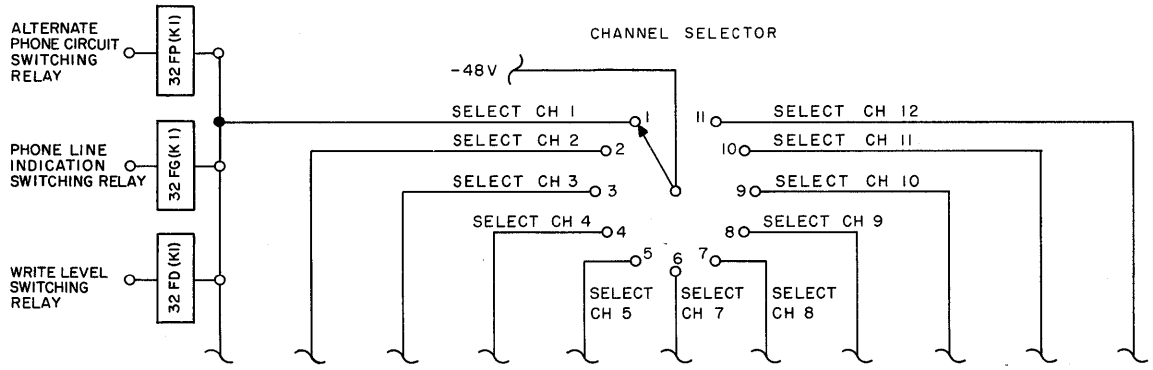
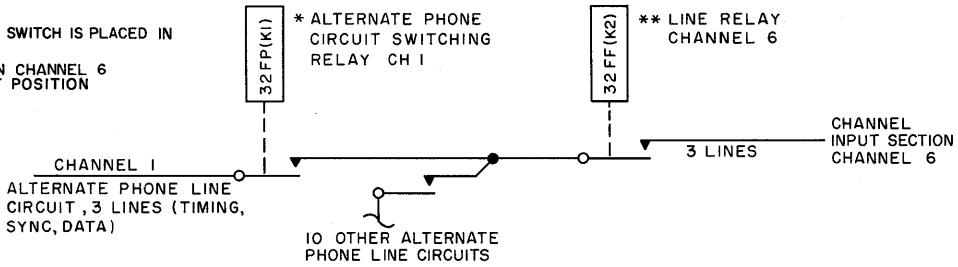


Figure 5–6. Input Data Switching

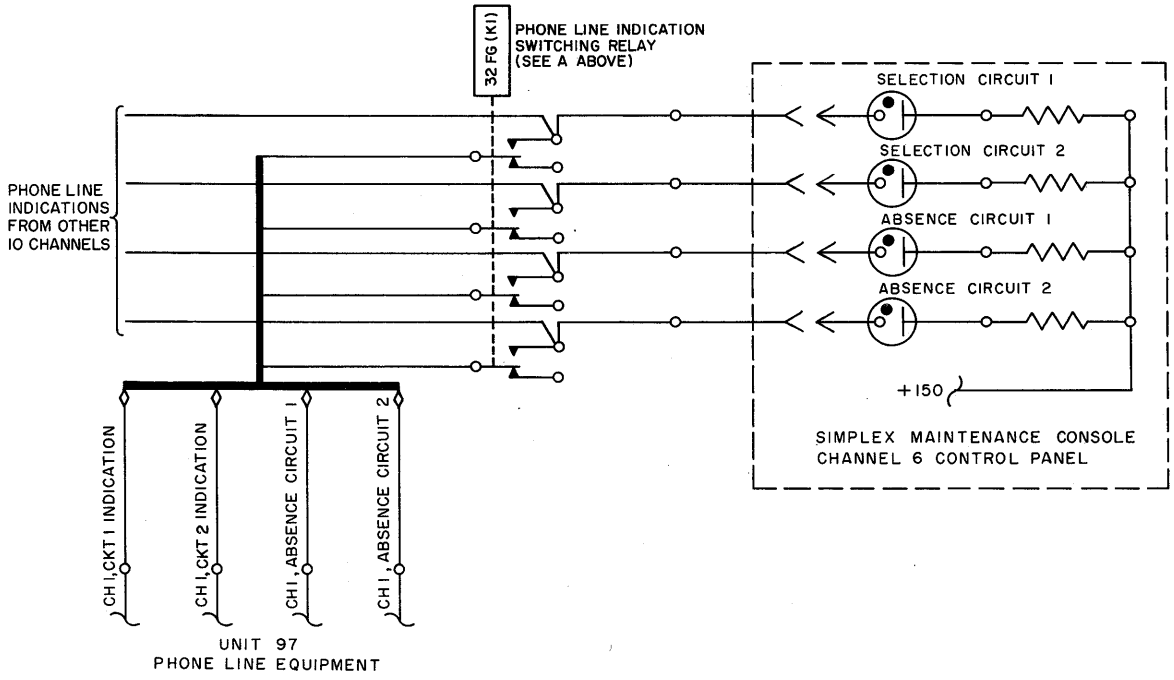


A. OPERATION OF CHANNEL SELECTOR SWITCH, SPARE CHANNEL

NOTE:
* ENERGIZED WHEN CHANNEL SELECTOR SWITCH IS PLACED IN POSITION 1 (SEE A ABOVE)
**ENERGIZED WHEN SOURCE SWITCH ON CHANNEL 6 (SPARE) IS PLACED IN DATA CIRCUIT POSITION



B. ALTERNATE PHONE LINE CIRCUIT SWITCHING



C. PHONE LINE INDICATION SWITCHING

Figure 5–7. Spare Channel Switching

CHAPTER 3
CROSSTELL CHANNEL INPUT SECTION

3.1 INTRODUCTION

The function of the channel input section in the XTL input element is to receive, in interleaved serial form, the XTL message from the DDR, to unscramble the received data, re-forming it into the five original message words, and to transfer these message words to the drum input (common) section. During these operations, the message is checked for the correct address (included as part of incoming message) and is also checked for parity (to detect any errors introduced during transmission).

The operation of the channel input section is synchronized by OD pulses and by pulses and levels developed from OD pulses, specifically for the use of the XTL element. The OD drum timing pulses are a series of four standard pulses, OD 1, OD 2, OD 3, and OD 4, equally spaced at 2.5 μsec. Recycling takes place without delay so that OD 1 occurs 2.5 μsec after OD 4. The OD pulse repetition rate of 10 μsec is too fast for some of the circuits in the channel input section. Therefore, the XTL common section develops, in synchronism with the OD pulses, a group of timing pulses having a repetition rate of 20 μsec; these pulses are designated XTL 1, XTL 3, XTL 6, etc. The common equipment also generates standard level outputs of a fixed duration; these outputs are designated XTL 2/3 and XTL 5/6. The XTL 2/3 level is a standard +10V level started by the XTL 2 pulse and terminating with the XTL 3 pulse. Similarly, the XTL 5/6 level is bounded by the XTL5 and 6 pulses. The generation of these pulses and levels is discussed in connection with the drum input section (Ch 5). The following pulses and levels are furnished by the drum input section to the channel input section through duplex switching (Ch 4):

a. OD 1 delayed (OD 1 + 1)
b. OD 4
c. XTL 1
d. XTL 3 delayed (XTL 3 +1)
e. XTL 6
f. XTL 2/3
g. XTL 5/6

Figure 5–8 shows the relationship between various XTL pulses and levels. A block diagram of the XTL channel input section is shown in figure 5–9. The

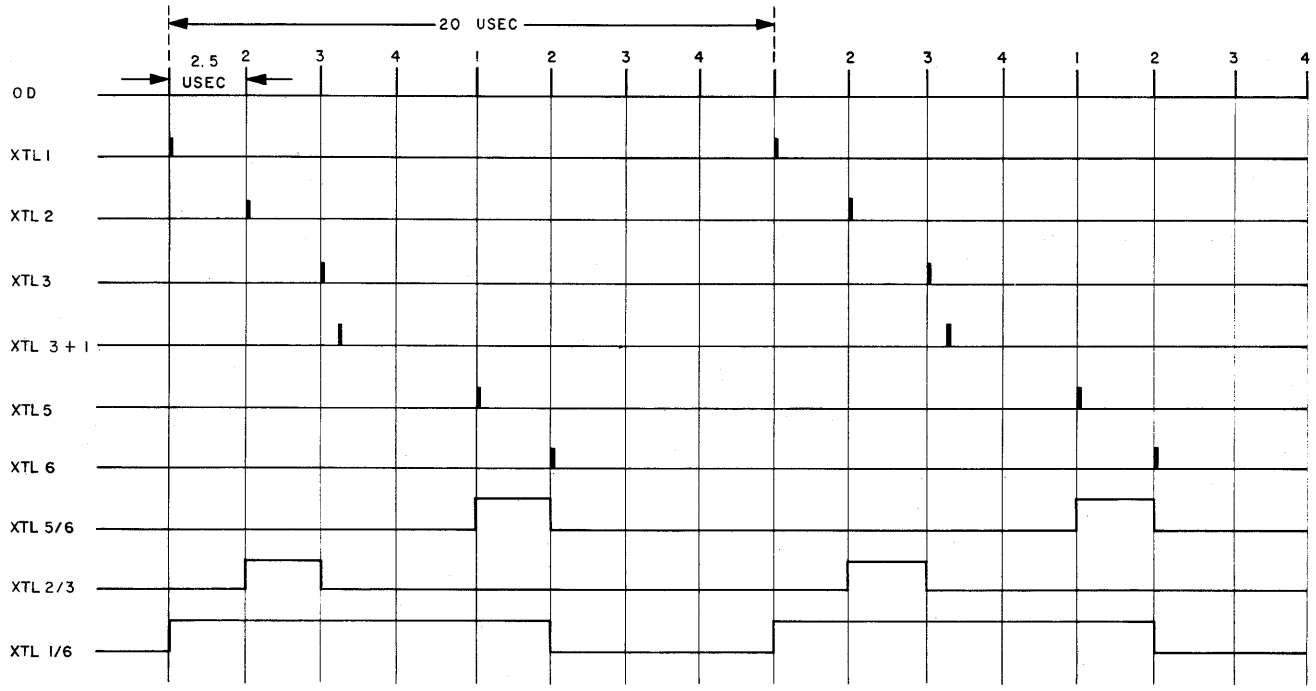


Figure 5–8. Crosstell Pulses ad Levels, Timing Chart

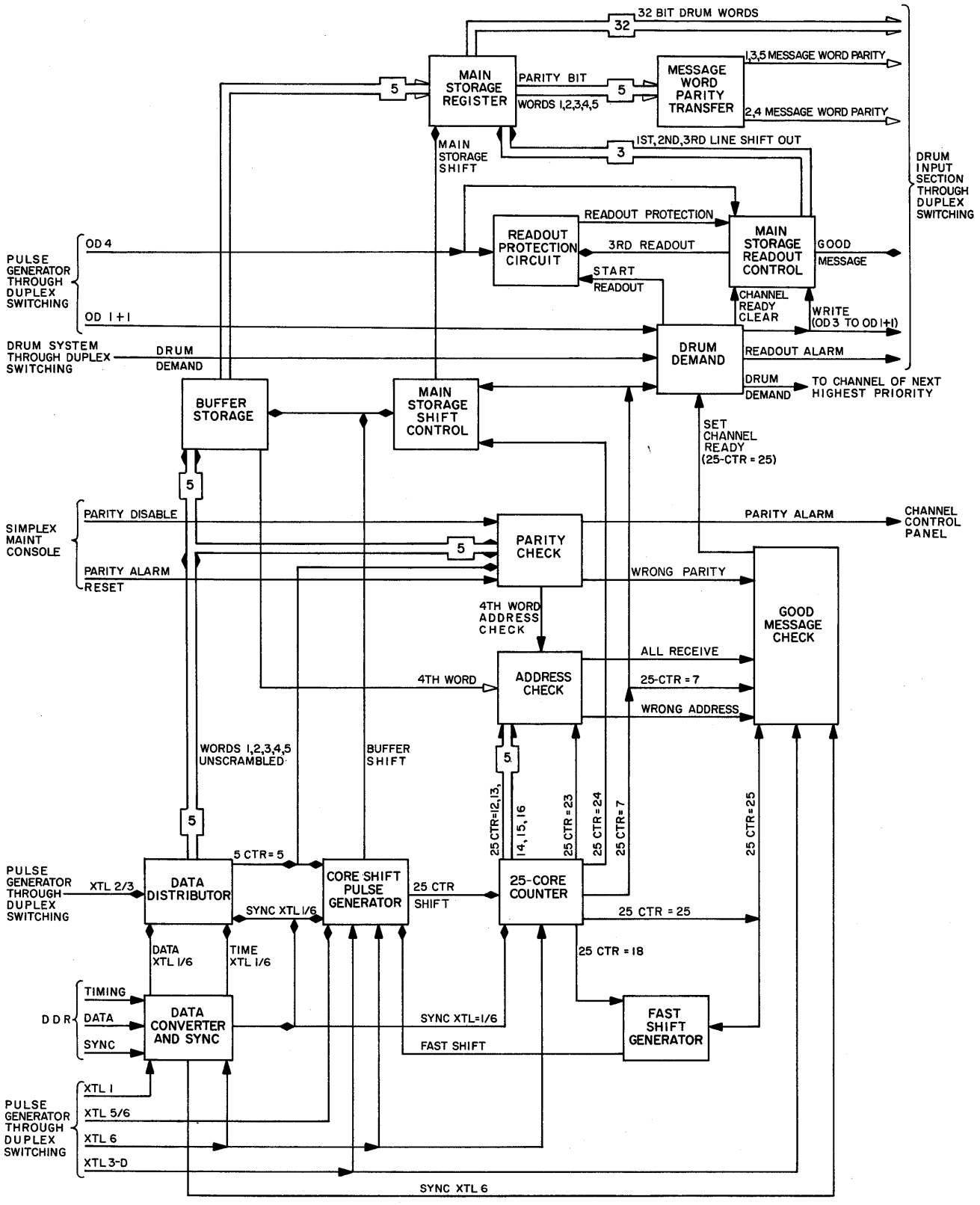


Figure 5–9. Crosstell Channel Input Section, Simplified Block Diagram

diagram shows the circuits employed in the channel along with the data flow and control layout of the channel as a whole.

The timing, sync, and data inputs that make up an XTL message are sent to the data converter and synchronizer circuit which converts these sinusoidal inputs into standard levels synchronized with OD and XTL timing pulses. The timing input is a continuous 1,300-cps sine wave signal and is converted into a single timing XTL 1/6 level for each cycle of the input sine wave. The sync input is a single cycle of a 1,300-cps sine wave signal which is converted into a single sync XTL 1/6 level. The data input is a single cycle of a 1,300-cps sine wave signal for each 1 data bit and no signal for each 0 data bit; it is converted into a single XTL 1/6 data level for each 1 data bit and no output for each 0 data bit. The three separate outputs (timing, sync, and data) are sent to the data distributor. The sync XTL 1/6 level is also sent to the 25-core counter to indicate the start of a message.

The five XTL message words are transmitted to the channel in interleaved form; the first data bit of each of the five words is received, followed by the second data bit of each word, etc. The successive data bits of the same word are five bits apart as the data bits are received. The data distributor circuit re-forms the five original XTL message words by producing five separate outputs, each of which is the data of a particular XTL message word. The five separate outputs of the data distributor are designated word 1 through word 5 data. They are inserted into separate buffer storage registers for each word and are also sent to the parity check circuit where the parity of each word is checked.

The buffer storage registers are five 7-core shift (CS) registers, with the output of each last core sent to the main storage registers. The latter are five 17-CS registers. Each main storage register is capable of storing a complete XTL message word (17 data bits); the entire XTL message is eventually stored here to await transfer to the Drum System. The reason for sending the unscrambled data bits to the buffer storage registers before transfer to the main storage registers is to enable the channel to receive and store the first 35 data bits (seven bits in each buffer storage register) of an incoming message before destroying the word of a previous message stored in the main storage registers. This time delay gives the Drum System ample time to locate an empty drum slot and to transfer the previous message from the main storage registers to the Drum System.

The rest of the circuits contained in the channel do not process data and are related only with the shifting, readout, and checking of the message. These circuits are described in detail in the logic discussions of each. The following is only a brief functional description.

The CS pulse generator produces a buffer-shift pulse after every five data bits (one from each message word) have been inserted into their proper buffer storage registers. The buffer-shift pulses are also used to shift the 25-core counter which keeps track of the position of the first group of data bits as they are transferred through the buffer and main storage registers. After seven buffer shifts, the first group of data bits is contained in the last core of each buffer storage register. The 25-counter then sends a 25-counter-equals-7 pulse to the main storage shift control circuit, causing the buffer-shift pulses to be simultaneously applied to the main storage registers. After the complete XTL message has been received by the channel and stored (seven bits of each word in the buffer storage registers and 10 bits of each word in the main storage registers), a 25, counter-equals-18 pulse is applied, through the fast-shift generator, to the CS pulse generator. The latter then produces buffer-shift pulses at a 20-μsec rate (fast shift), rapidly transferring the last seven bits of each word from the buffer storage registers to the main storage registers.

The parity check circuits receive the data bits of the five message words from the data distributor and check the parity of each message word. The address check circuit receives data from word 4 only. In the event of an incorrect parity count, the parity check circuit produces a wrong-parity signal. In the event of an incorrect address, the address check circuit generates a wrong-address signal. In the absence of a wrong-parity or a wrong-address signal, the good message check circuit produces a set-channel-ready (25-counter-equal-25) signal when a message has been received and stored in the main registers. The drum demand circuit is informed of the reception and storage of a message by the set-channel-ready pulse and the 25-counter-equals-25 pulse. The drum demand circuit then produces a write signal when an empty drum slot is available. The write signal is applied to the main storage readout control circuit which then produces three readout signals, causing the parallel readout of the message words from the main storage registers to the drum input section (common equipment).

3.2 DATA CONVERTER AND SYNCHRONIZER

The data converter and synchronizer converts timing, sync, and data sinusoidal inputs into standard levels of fixed duration synchronized with XTL timing pulses. The synchronized timing, sync, and data levels are used in other circuits of the XTL channel input section.

The timing, sync, and data (sinusoidal) inputs are sent to the XTL input channel on separate lines. Each of the three input signals is applied to a data conversion receiver (DCR). A simplified logic diagram of the circuit is shown in figure 5–10. Timing relationships in

the operation of the circuit are shown in figure 5–11. The timing input, a continuous 1,300-cps sine wave, is applied to a model ADCR, which produces a negative nonstandard pulse for each negative peak of the timing sinusoidal input. This negative pulse is used to set flip-flop (FF) 1. The 1 output level of FF 1 conditions gate tube (GT) 1, permitting an XTL 1 pulse to pass and set FF 2. The 1 output level of FF 2 conditions GT 3, allowing an XTL 6 pulse to pass. The XTL 6 clears FF's 1 and 2. Since FF 2 was set by an XTL 1 pulse and cleared by the following XTL 6 pulse, it produces a set output level for the time between XTL 1 and XTL 6, designated timing XTL 1/6, with a duration of 12.5 μsec. Timing XTL 1/6 levels are sent to the data distributor, to AND 1, AND 2, and GT 3.

The sync input consists of a single cycle of a 1,300-cps sine wave signal, indicating the start of a message, which is applied to BDCR 2. The DCR 2 produces a standard level output of 200-μsec duration for each negative peak of its input. The output of DCR 2 is applied to AND 2 and GT 2. AND 2 then passes the timing XTL 1/6 output of FF 2. The single timing XTL 1/6 level, passed through AND 2 when the sync level is present, is a sync XTL 1/6 level sent to the data distributor, to the CS pulse generator, and to the 25-core counter. Gate 2 is conditioned by the output of DCR 2 and can pass the XTL 6 pulse (that clears FF's 1 and 2) applied to it from GT 3. The output of GT 2 is a single XTL 6 pulse occurring when the sync input is presented to the channel. This sync XTL 6 pulse is sent to the parity check circuit.

The data input consists of a single cycle of a 1,300-cps sine wave signal for each 1 data bit and no signal for each 0 data bit. This input is applied to BDCR 1,

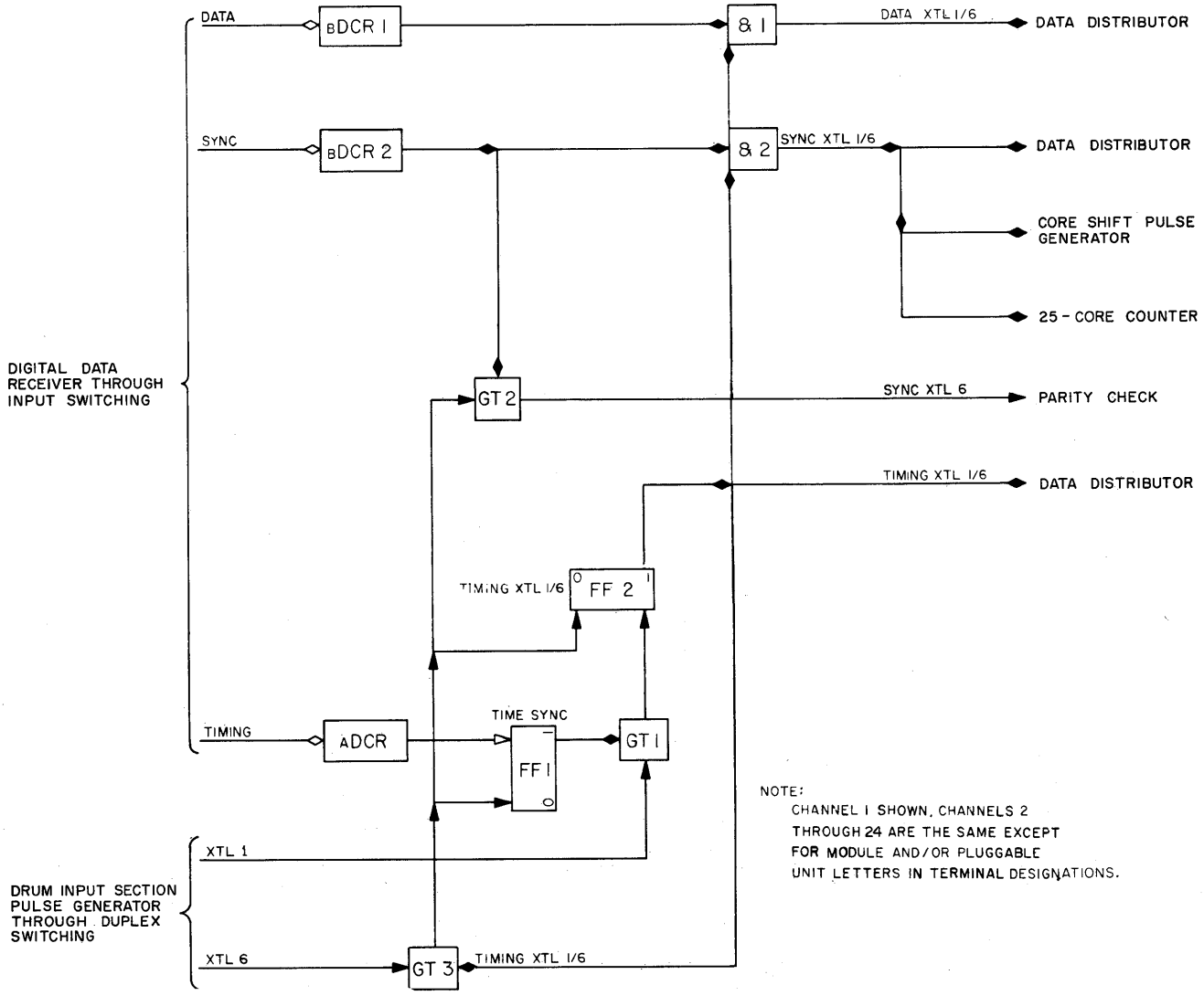


Figure 5–10. Data Converter and Synchronizer, Simplified Logic Diagram

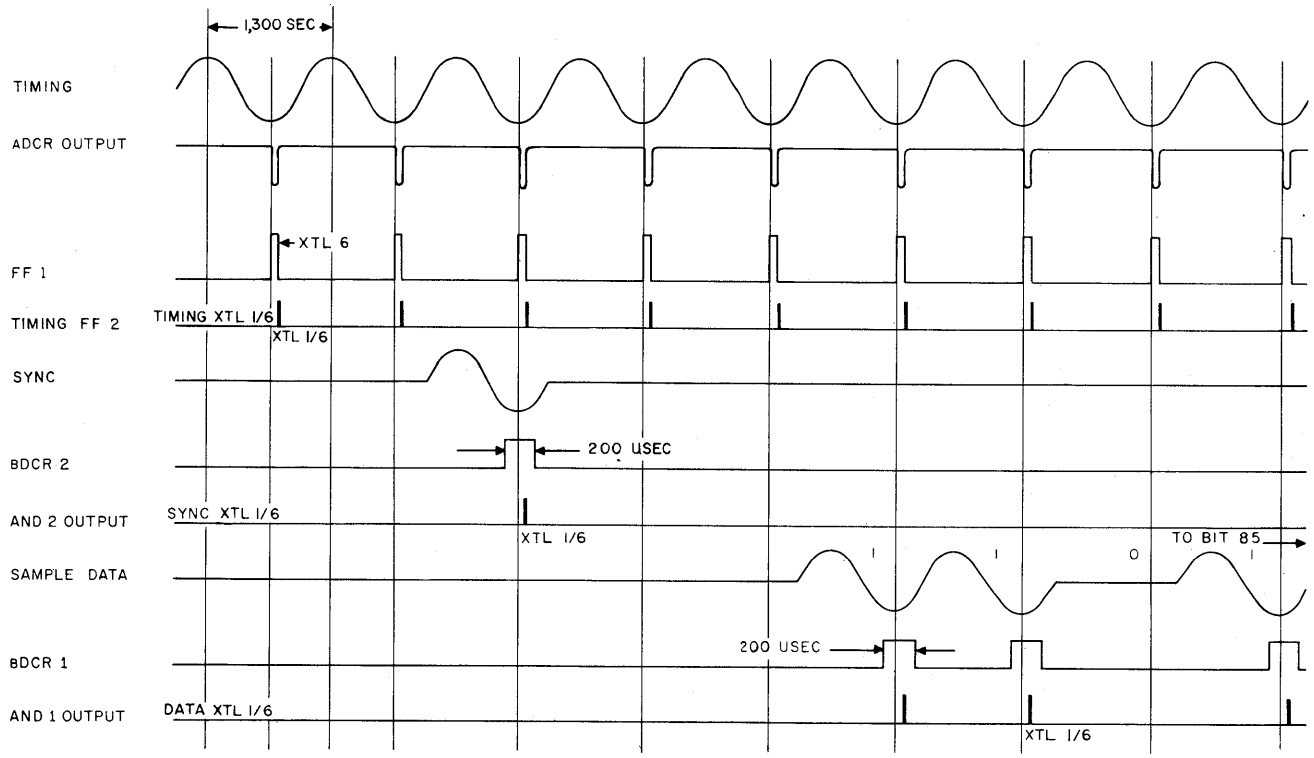


Figure 5–11. Data Converter and Synchronizer, Timing Chart

which produces a 200-μsec standard level output for each 1 data bit. The BDCR 1 output is applied to AND 1. AND 1 passes an XTL 1/6 level whenever a 1 data bit appears and has no output for 0 data bits. These data XTL 1/6 levels are sent to the data distributor.

3.3 DATA DISTRIBUTOR

The data distributor re-forms the five original XTL words from the 85 interleaved data bits of an incoming XTL message and sends the words to the five buffer storage registers, one word to each register. The five words are also sent to the parity check circuit where the parity of each word is checked.

The data distributor, shown in figure 5–12, receives data XTL 1/6 levels, timing XTL 1/6 levels, and a sync XTL 1/6 level from the data converter and synchronizer. The data bits (a single XTL 1/6 level for each 1 data bit and a 0 level for each 0 data bit) are applied simultaneously to AND circuits 1, 2, 3, 4, and 5. Each of the AND circuits also receives a single output signal from the 5-core ring counter. The 5-core ring counter outputs are 5-counter-equals-1, -2, -3, -4, and -5 and are applied to AND circuits 1, 2, 3, 4, and 5, respectively. The 5-counter is primed and shifted so that, when the first incoming data bit is present, only the 5-counter-equals-1 pulse appears. If the first data bit is a 1, AND 1 passes the 5-counter-equals-1 pulse. The 5-counter-equals-2 pulse appears when the second incoming data bit is applied and passes through AND 2 if the second data bit is a 1. In the same manner, AND 3 passes a 5-counter-equals-3 pulse if the third data bit is a 1; AND 4 passes a 5-counter-equals-4 pulse if the fourth data bit is a 1; and AND 5 passes a 5-counter-equals-5 pulse if the fifth data bit is a 1. The 5-counter then recycles, with AND 1 passing a 5-counter-equals-1 pulse if the sixth data bit is a 1, etc. Each AND circuit passes every fifth data bit if it is a 1 and produces no output for each 0 data bit, thereby accomplishing the unscrambling of the interleaved data and re-forming the original 5 words. Refer to table 5–2.

At the start of a message, a sync XTL 1/6 level is applied through an OR circuit to the core shift driver (CSD), producing a long-duration-shift signal (12.5 μsec) that clears the five core shifts to 0. The same sync XTL 1/6 level is also applied to the input winding of CS 4 through a delay network in the CS circuit. The delay circuit enables the sync XTL 1/6 level to prime the CS after the clearing shift XTL 1/6 signal has terminated. Thus, a single 1 is stored in CS 4, and the other core shifts store a 0 at the beginning of a message.

Timing XTL 1/6 levels are applied to AND 6 which then passes XTL 2/3 levels from the drum input section. AND 6 passes a single XTL 2/3 level whenever a timing XTL 1/6 level is present. This timing XTL 2/3 level is applied through the OR circuit to the CSD, producing

a shift pulse output (2.5 μsec) to the five CS's. The shift pulse transfers the contents of each CS to the adjacent CS. The first timing XTL 2/3 level transfers the 1 in CS 4 to CS 5. The second timing XTL 2/3 level transfers the 1 from CS 5 to CS 1. The next timing XTL 2/3 level, which occurs simultaneously with the first incoming data bit (sync is followed by two 0's before the first incoming data bit), moves the 1 from CS 1 to CS 2. The output line connected between CS 1 and CS 2 is activated by the transfer. This nonstandard output is applied to a level setter (LA) which produces a standard level output designated 5-counter-equals-1. The next timing pulse (which occurs simultaneously with data bit 2) transfers the 1 from CS 2 to CS 3, producing a 5-counter-equals-2 pulse. The 5-counter-equals-3, -4, and -5 pulses occur simultaneously with data bits 3, 4, and 5, respectively. Since the 5-CS register is connected as a ring (CS 5 drives CS 1), the 5-counter-equals-1 pulse occurs again when the sixth data bit is present, etc. (See fig. 5–13.) In this manner, the output of AND 1 is data bits 1, 6, 11, 16, 21, etc., which is the unscrambled word 1 data. The AND 2, 3, 4, and 5 outputs are unscrambled word 2, 3, 4, and 5 data, respectively.

The 5-counter-equals-5 pulse is also sent to the CS pulse generator circuit (discussed in 3.5) and to the parity check circuit (discussed in 3.10).

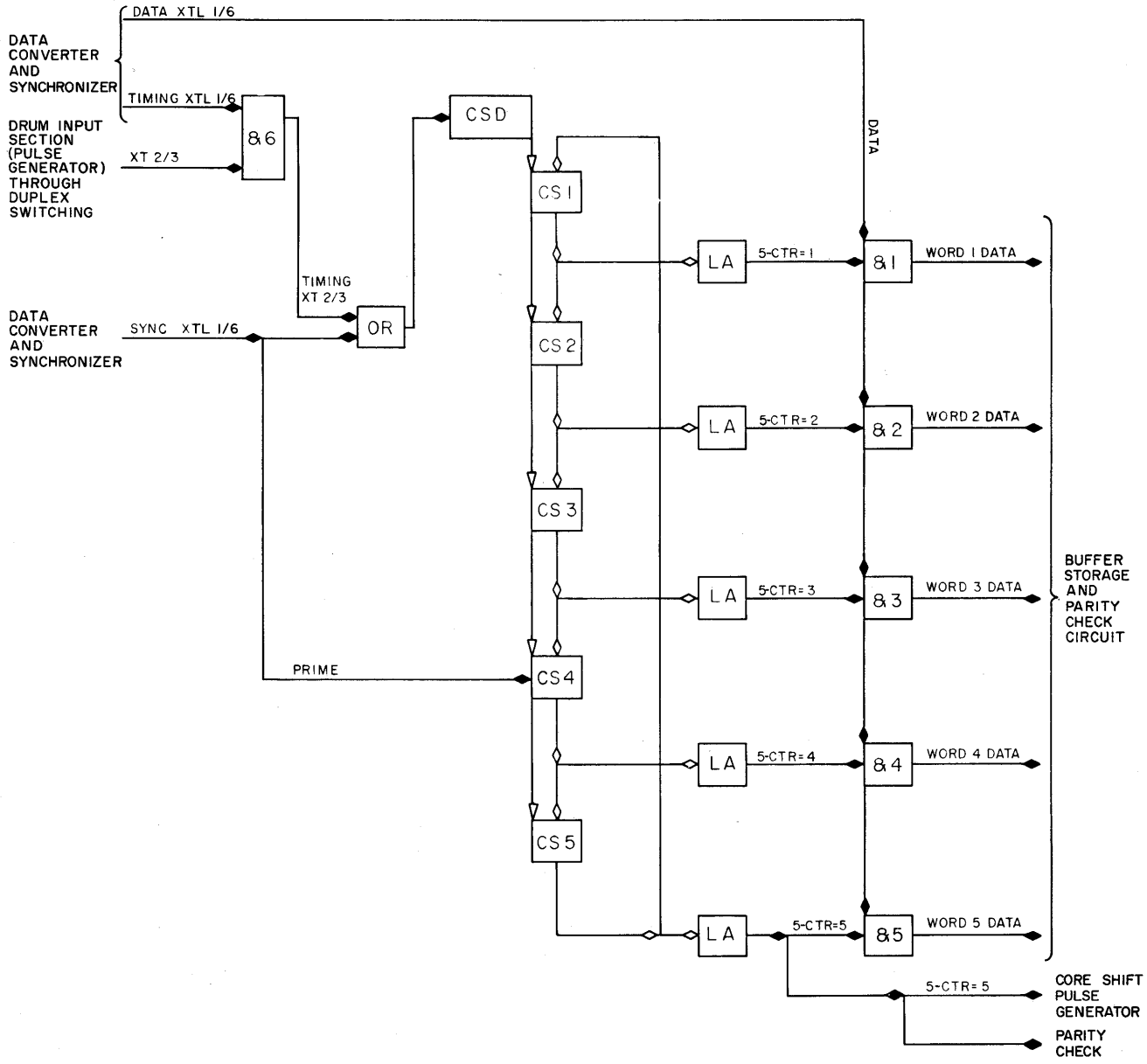


Figure 5–12. Data Distributor, Simplified Logic Diagram

3.4 BUFFER STORAGE REGISTERS

The five buffer storage registers are filled serially by the data bits of the five XTL words from the data distributor. Their function is to delay the transfer of data to the main storage register sufficiently to permit the drum to demand and to accept a previous message from the main storage registers. They achieve this delay by receiving and storing the first 35 bits of an incoming message. A time lapse of 35/1,300 second is thereby provided in which the drum section can locate an available drum slot and receive the previous message from the main storage circuit.

The buffer storage circuit, shown in figure 5–14, consists of five 7-CS registers. The first core of each of these buffer storage registers is primed by the word data bits from the data distributor. Buffer storage registers 1 through 5 receive the data of words 1 through 5, respectively. After the first group of five data bits has been inserted into the first core of each buffer storage register, a shift XTL 5/6 level from the CS pulse generator circuit is applied to the CSD of each buffer storage register. This shift level transfers the contents of each core to the adjacent core. The five data bits of the next group are then inserted into their respective buffer storage registers, and a second shift level is applied. The shift level is applied after the insertion of every five data bits, producing a shift rate of 5/1,300 second.

After the buffer storage registers have received the first 35 data bits, they are full (seven bits in each word register). At this time, the main storage shift control circuit permits the main storage registers to be shifted along with the buffer storage registers. The data bits of each word are then transferred from the last core of each buffer storage register to the first core of each main storage register. After an additional 50 data bits have been received, the entire message (85 data bits) will have been received and stored (seven bits in each buffer storage register and 10 bits in each main storage register). The CS pulse generator now produces shift levels at a fast-shift rate (50,000 pps), transferring the last seven bits of each word from the buffer storage registers to the main storage registers. The main storage registers then contain the complete message (17 bits per word). The fourth word buffer storage register output is also sent to the address check circuit, since address information is contained in a portion of the fourth XTL message word.

3.5 CORE SHIFT PULSE GENERATOR AND FAST-SHIFT GENERATOR

The CS pulse generator produces the pulses used to shift the buffer storage registers. The buffer-shift

TABLE 5–2. DATA DISTRIBUTOR, DATA BIT DISTRIBUTION – UNSCRAMBLING

	Sync																	
	0																	
Output of	0																	
AND 1	1	6	11	16	21	26	31	36	41	46	51	56	61	66	71	76	81	XTL word 1
	MB															MB	PAR	
AND 2	2	7	12	17	22	27	32	37	42	47	52	57	62	67	72	77	82	XTL word 2
	MB															MB	PAR	
AND 3	3	8	13	18	23	28	33	38	43	48	53	58	63	68	73	78	83	XTL word 3
	MB															MB	PAR	
AND 4	4	9	14	19	24	29	34	39	44	49	54	59	64	69	74	79	84	XTL word 4
	MB										AD	AD	AD	AD		AP	PAR	
AND 5	5	10	15	20	25	30	35	40	45	50	55	60	65	70	75	80	85	XTL word 5
	MB																PAR	
Word bits	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

MB = *Incoming message bit*
PAR = *Parity bit*
AD = *Address bit*
AP = *All-parties bit*

pulses are also applied to the main storage shift control circuit and to the 25-core counter.

The CS pulse generator, shown in figure 5-15, is supplied with the 5-counter-equals-5 level from the data distributor. This level appears after a data bit has been inserted in each of the five buffer registers. The latter must now be shifted so that the next data bit of each word may be inserted in its respective register. The CS pulse generator produces an XTL 5/6 buffer shift level after each 5-counter-equals-5 level has appeared. After 17 buffer-shift pulses have been generated, the complete XTL message will have been received and stored in the channel equipment (10 bits of each word in the main storage registers and seven bits of each word in the buffer-storage registers). The fast shift is then turned on, permitting a buffer-shift pulse to occur every 20 μsec. This transfers the seven bits in each buffer register to the associated main storage register at a rapid rate.

OR circuit 1 receives either the 5-counter-equals-5 level or the fast-shift level from FF 1. The 5-counter-equals-5 pulse, passing through OR 1, conditions GT 1. Gate 1 passes an XTL 3 + 1 pulse which sets FF 2. The set output of FF 2 is applied to AND 1 which then passes an XTL 5/6 level. The output of AND 1 is used to drive the CSD of each buffer register. Flip-flop 2 is cleared by an XTL 6 level, deconditioning AND 1 after it has passed the single XTL 5/6 shift level. The XTL 5/6 shift level is also sent to the main storage shift control circuit where it is used to shift the main storage registers at the appropriate time.

The fast shift (mentioned above) is controlled by FF 1 which, in turn, is controlled by the 25-core counter. The 25-counter counts the number of buffer-shift levels. The 18th buffer shift causes the 25-counter-equals-18 (XTL 6) pulse to appear, setting FF 1. The output of FF 1 (fast-shift signal) is applied through OR 1 and

Figure 5—13. Data Distributor, Timing Chart

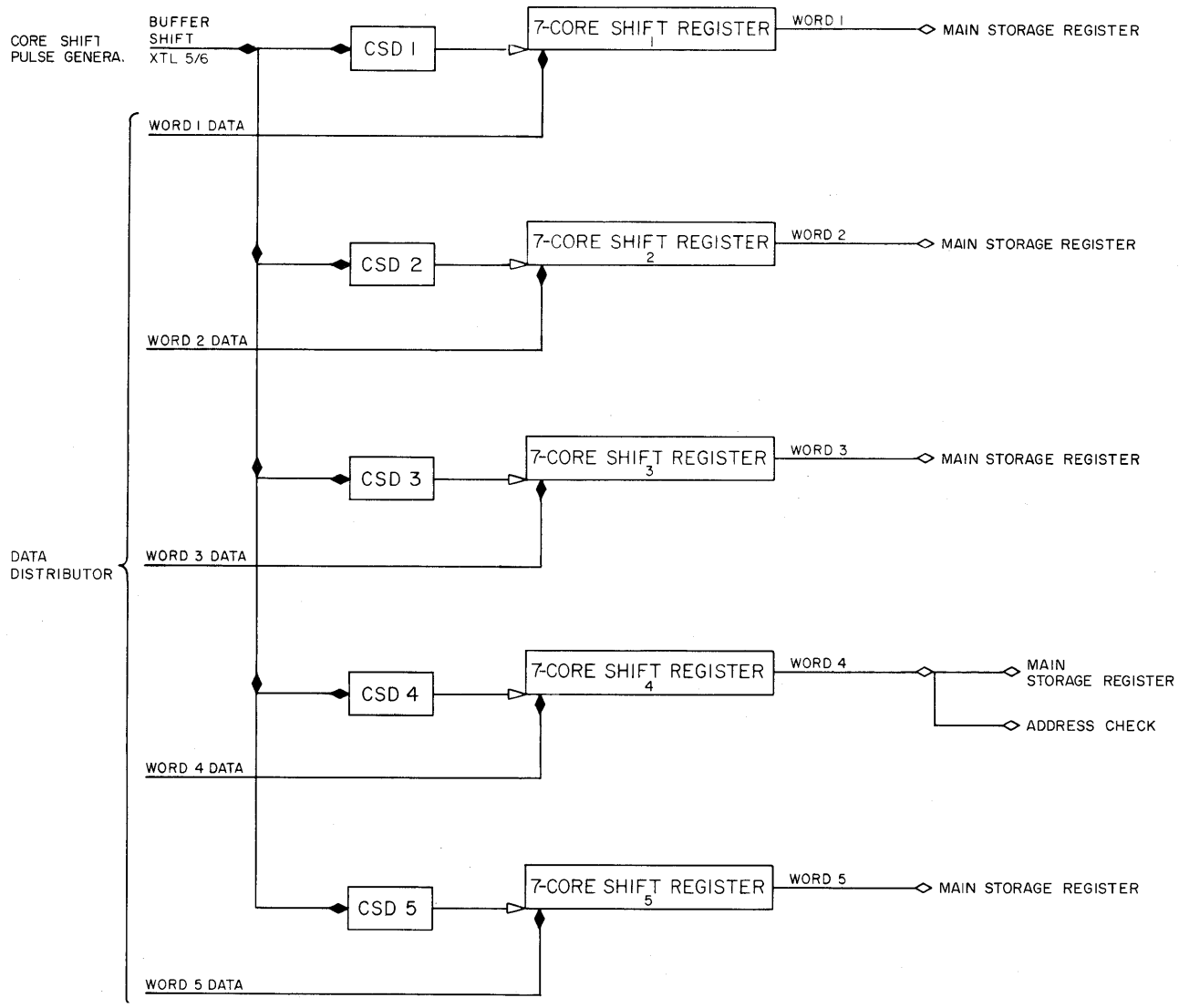


Figure 5–14. Buffer Storage Registers, Simplified Logic Diagram

conditions GT 1. Gate 1 passes each XTL 3 + 1 pulse that occurs while the fast shift is on. These XTL 3 + 1 pulses set FF 2. The set output of FF 2 is applied to AND 1 which then passes each XTL 5/6 level, producing a shift pulse every 20 μsec (the pulse repetition time of XTL 5/6 levels). These XTL 5/6 levels are used to shift the buffer storage registers, main storage registers, and 25-counter. After six shift levels at the fast-shift rate, the complete message is in the main storage registers, and the 25-counter-equals-24 pulse turns off the shift coupler FF. The 25-counter-equals-25 (XTL 6) pulse clears FF 1, turning the fast shift off. (See fig. 5–16.) The main storage registers now hold the complete XTL message (five words of 17 bits each) until it is transferred to the drum input section (common equipment).

3.6 THE 25-CORE COUNTER

The 25-core counter reflects the progress of the message through the buffer and main storage registers by counting the buffer-shift levels (applied by the CS pulse generator). At various counts, the 25-core counter supplies pulses which initiate and terminate the operation of other circuits.

The 25-core counter circuit, shown in figure 5–17, consists of a 25-CS register, 10 GT's and a CSD. At the start of a message, the CS pulse generator provides a pulse, derived from a sync XTL 1/6 level, on its 25-counter output line. This pulse is applied to a CSD, the output of which clears the cores in the 25-core register. The sync XTL 1/6 level, fed from the data converter and synchronizer, primes the first CS of the 25-counter. The 25-counter now counts buffer-shift levels. The first

buffer-shift level causes the 1 in the first CS of the 25-counter to be shifted to the second CS. After the first group of five data bits has been inserted into the buffer storage registers, the second buffer-shift level shifts the buffer storage registers and the 25-core counter, moving the 1 in CS 2 to CS 3. The process continues, with the single 1 in the 25-CS register moving one CS each time the buffer storage registers are shifted. In this manner, the position of the 1 in the 25-counter indicates the progress of the first group of data bits through the buffer and then through the main storage registers. When the first group of data bits is transferred to the seventh core of each buffer storage register, the 1 in the 25-core counter moves from CS 7 to CS 8, producing an output on the line connected between these two CS's. This output conditions a gate, permitting an XTL 6 pulse to pass as the 25-counter-equals-7 pulse. The 25-counter-equals-7 pulse (indicating that the first group of data bits is in the seventh core of the buffer storage registers) is sent to the main storage shift control circuit where it is used to initiate the generation of shift pulses to the main storage registers. (It is necessary to start shifting the main storage registers at 25-counter-equals-7 time since the next buffer-shift pulse will transfer the first group of data bits to the main storage register). The 25-counter-equals-7 pulse is also sent to the good message check circuit and to the drum demand circuit.

When the 25-counter-equals-12 line is pulsed, the first group of data bits has been shifted 12 times and the 12th data bit of each XTL word is now inserted into the buffer storage registers. The 25-counter-equals-12, -13, -14, -15, and -16 pulses are sent to the address check circuit because address data is contained in the 12th, 13th, 14th, 15th, and 16th bit of the fourth word. (Refer to 3.9 for the use of these 25-counter pulses.)

The 25-counter-equals-18 pulse appears after the 17th data bit of each word has been entered into the buffer storage registers. The complete XTL message has now been received (17 bits per word). The 25-counter-equals-18 pulse is sent to the fast-shift generator to initiate the fast-shift signal.

The 16th bit of the fourth word leaves the word 4 buffer storage register when the 25-counter-equals-23 pulse appears. Since the 16th bit of the fourth word is

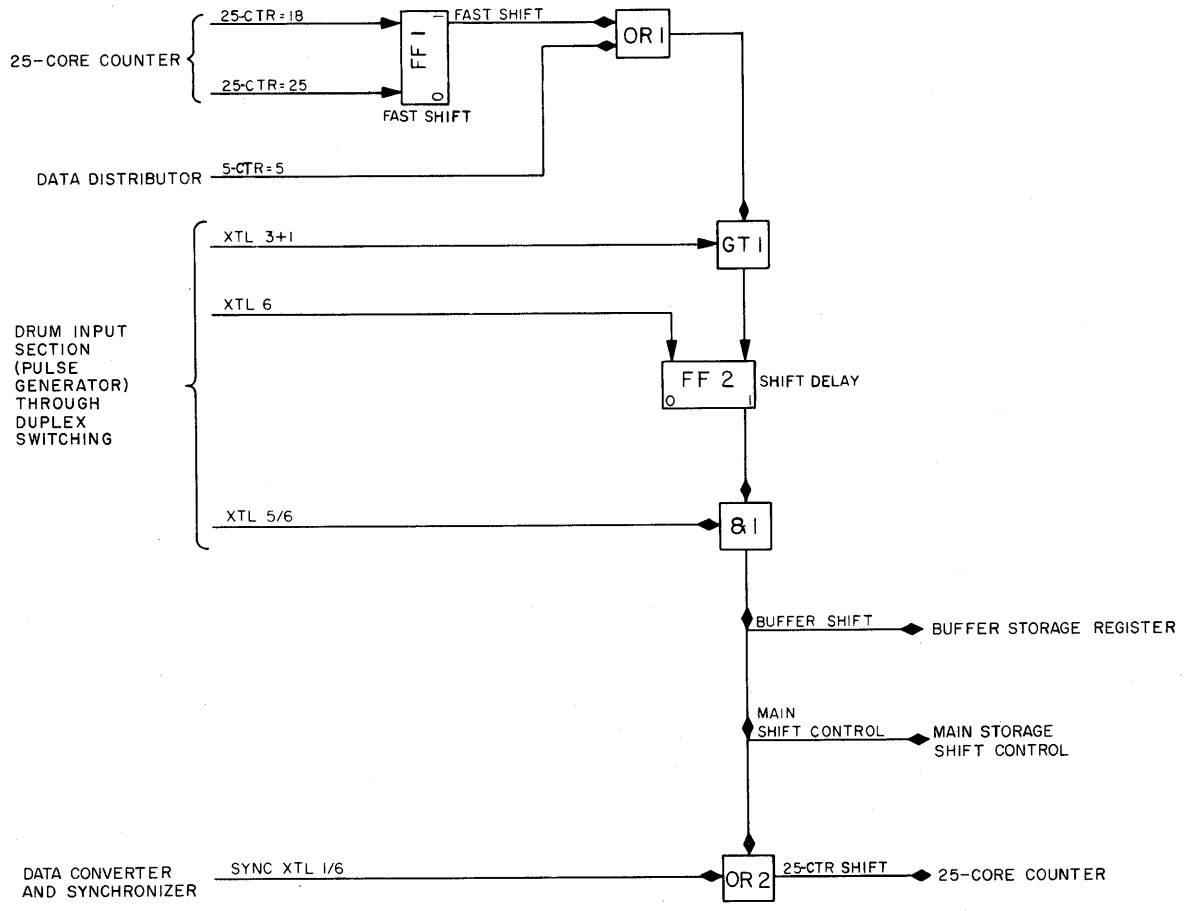


Figure 5—15. Core Shift Pulse Generator and Fast Shift Generator, Simplified Logic Diagram

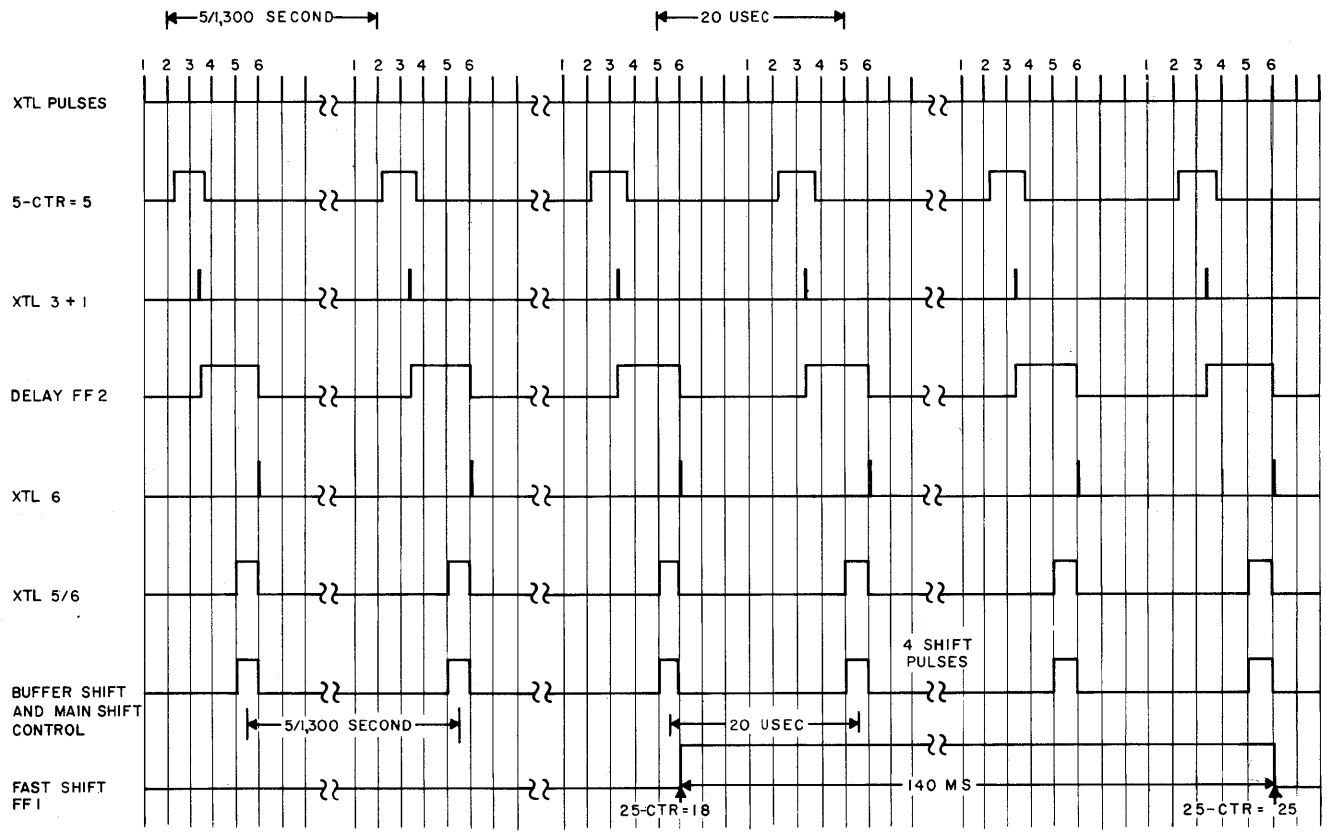


Figure 5–16. Core Shift Pulse Generator and Fast Shift Generator, Timing Chart

the all-parties bit, the 25-counter-equals-23 pulse is sent to the address check circuit where it permits the all-parties bit (when present) to pass.

The 25-counter-equals-24 pulse is sent to the good message check circuit, where it is passed if a parity error is present, and to the main storage shift control circuit, where it terminates the generation of main-storage-shift pulses. The 25-counter-equals-25 pulse is sent to the fast-shift generator to terminate the fast-shift signal and to the good message check circuit to provide a set-channel-ready pulse to the drum demand circuit when a good message has been stored in the main storage registers.

3.7 MAIN STORAGE

3.7.1 General

The main storage circuit serially receives the data bits of each of the five words constituting the XTL message, temporarily stores the words, and, when an XTL drum slot becomes available, transfers the words in the required order to the XTL drum input section.

The main storage circuit (fig. 5–18) consists of five 17-CS registers, each of which receives a word of the XTL message. A detailed diagram of the word 1 main storage register is shown in figure 5–19.

3.7.2 Word Storage

The data bits from the five buffer storage registers are each fed to the corresponding 17-CS main storage register. Like data bits for each word are received simultaneously by the main storage registers. For example, the first bit of words 1 through 5 is transferred into its respective main storage register at the same time. A shift pulse from the main storage shift is then applied through each OR circuit to each CS driver, shifting all five registers. The second bit of each word is then received by the five main storage registers. This process continues until the five registers are full, containing the entire XTL message. The shifting pulse from the main storage shift then stops.

The main storage shift does not occur at the same rate continuously. During the input of the first 11 bits of each word, the main-storage-shift pulse occurs every 5/1,300 second. After the 10th bit of each word is inserted in the main storage registers, the entire message of 17 bits per word is stored in the channel input; i.e., 10 bits of each word in the main storage registers and seven bits of each word in the buffer storage registers. At 5/1,300 second after this time, the main-storage-register and buffer-storage-register-shift pulses are applied every 20 μsec, and the six bits for each word that are stored in

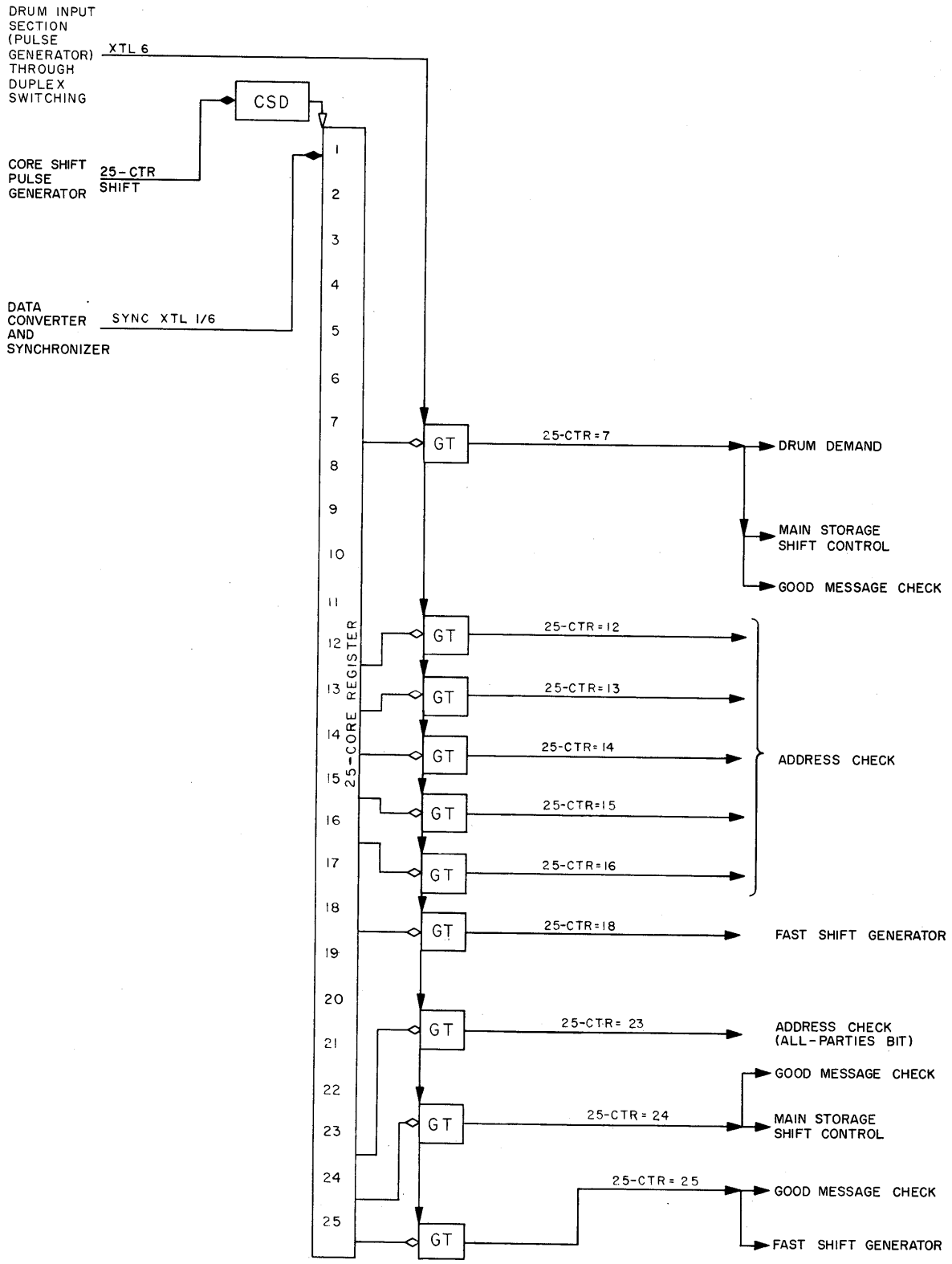


Figure 5–17. Twenty-Five Core Counter, Simplified Logic Diagram

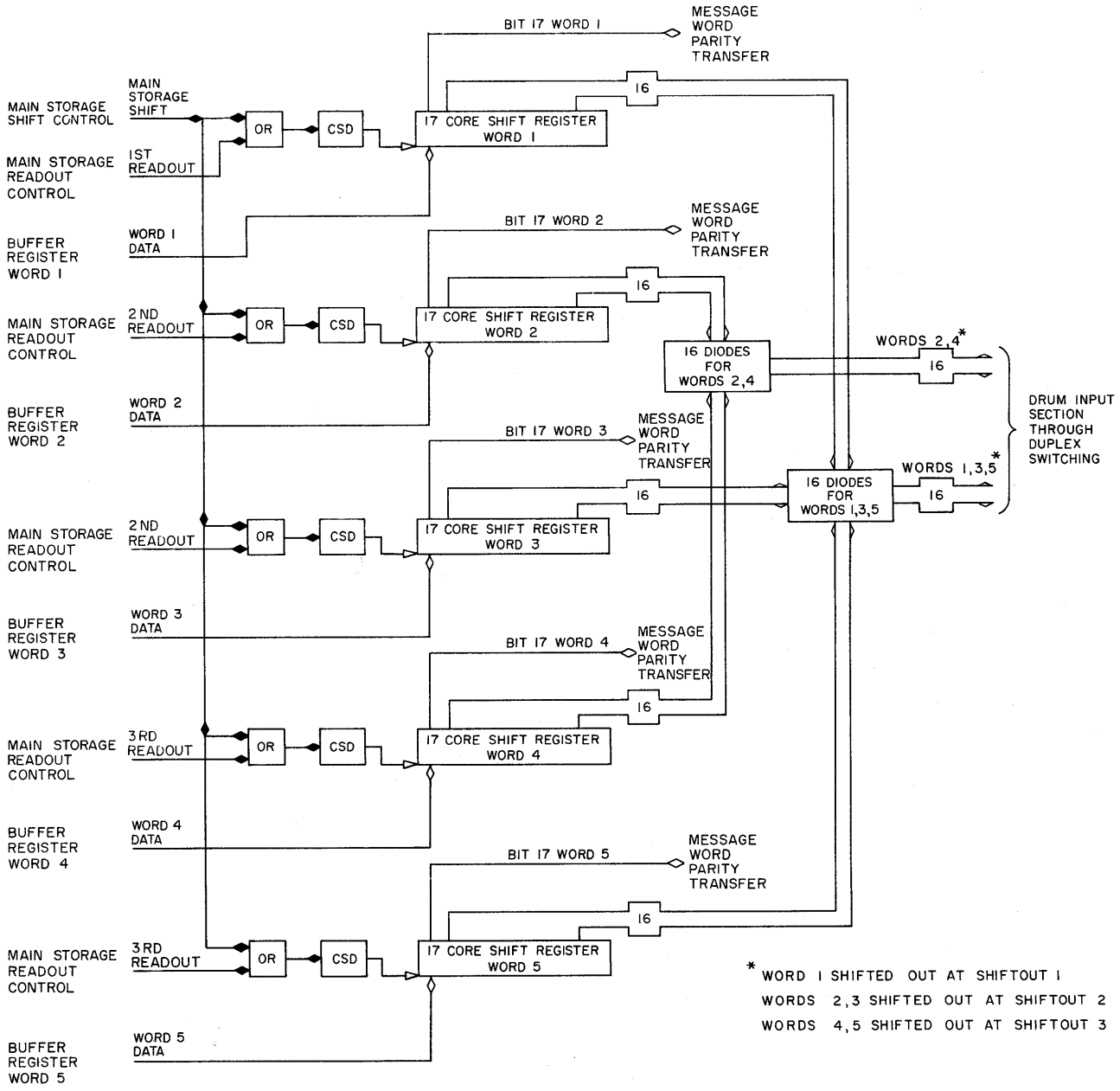


Figure 5–18. Main Storage Registers, Simplified Logic Diagram

the buffer enter the main storage at this rate (fast shift).

3.7.3 Word Readout

The 25-counter-equals-25 pulse now informs the drum demand circuit (through the good message circuit) that the entire XTL message is in the main storage circuit awaiting transfer to the drum field. The next drum-demand pulse, indicating an empty slot on the drum, initiates the readout process during which the five words in the main storage are transferred to the drum input section. This readout is controlled by the main storage readout control circuit which generates three readout levels. The first readout level is applied to the CSD for register 1 through an OR circuit. This shift level causes each core to shift and to produce an output on each of the 17 lines connected to the output of each of the 17 cores. Thus, the readout to the drum input is done in a parallel manner: all 16 data bits are transferred at once. The main storage registers containing words 2 and 3 transfer their data in the same manner when the second readout level is applied. The third readout level transfers words 4 and 5 to the drum input section. The parity bit, which is the 17th bit of each word, is sent to the message word parity transfer circuit.

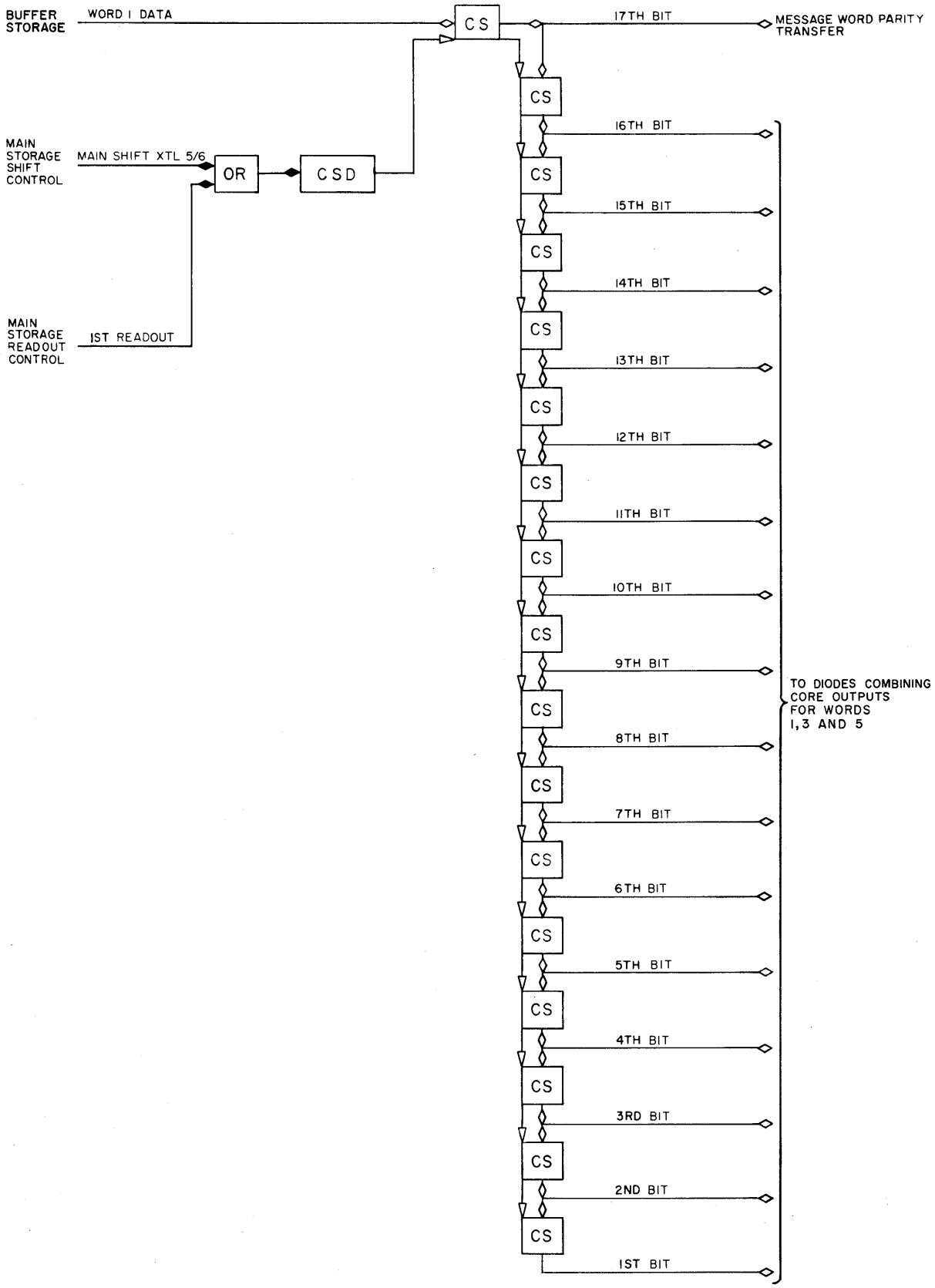


Figure 5–19. Main Storage Register Word, Simplified Logic Diagram

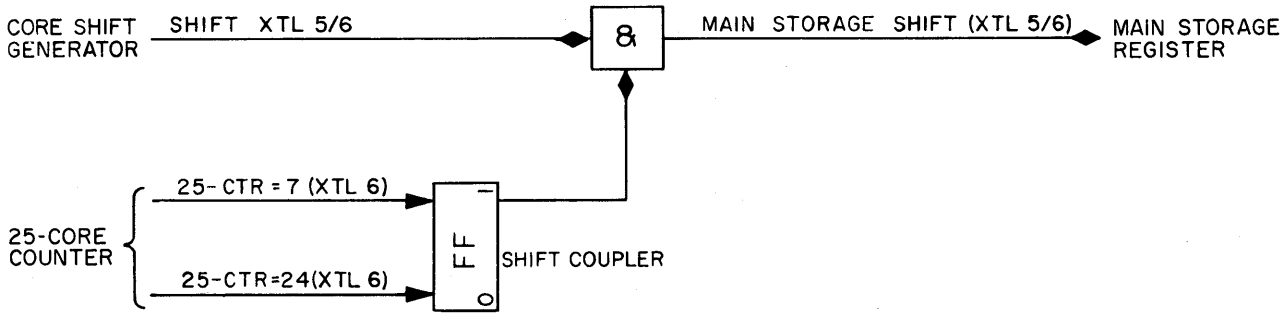


Figure 5—20. Main Storage Register Shift Control, Simplified Logic Diagram

3.7.4 Diode Isolating Circuits

The like data cores of words 1, 3, and 5 main storage registers (e.g., each LS core) and of words 2 and 4 main storage registers (e.g., each RS core) are connected through separate diodes to duplex switching. Since word 1, words 2-3, and words 4-5 are shifted out separately, only one bit can pass through a diode at each readout.

The purpose of the diodes is to function as an OR circuit and to isolate the main storage registers of one channel from those of another. A total of 32 diodes are provided which accommodate all core output lines except the word parity cores, L 16 of words 1, 3 and 5 main storage registers, and R 16 of words 2 and 4 main storage registers. The word parity cores are connected to a separate circuit, the parity transfer circuit described in 3.15.

3.8 MAIN STORAGE SHIFT CONTROL

The main storage shift control circuit (fig. 5—20) controls the flow of shift pulses to the main storage registers. The circuit contains a flip-flop set by the 25-counter-equals-7 pulse and cleared by the 25-counter-equals-24 pulse. The set output of the flip-flop conditions the AND circuit, allowing XTL 5/6 shift levels from the CS pulse generator to pass. The XTL 5/6 shift levels drive the CSD in the main storage registers circuit.

From the 25-counter-equals-1 time to 25-counter-equals-7 time, the buffer storage circuit receives the first 35 data bits of the XTL message. During this time, the main storage registers are not shifted. At 25-counter-equals-7 time, the first group of data bits is inserted into the last core of each buffer storage register and will be transferred to the main storage registers by the next shift level. Therefore, the shift levels are supplied to the CSD in the main storage registers after the 25-counter-equals-7 pulse has appeared. At 25-counter-equals-24 time, the complete message is stored in the main storage registers and further shifting would destroy the message. Therefore, the 25-counter-equals-24 pulse clears the flip-flop, preventing any additional shift XTL 5/6 levels from shifting the main storage registers.

3.9 ADDRESS CHECK

The address check (fig. 5—21) circuit serially receives the data bits of the fourth word (from the parity check circuit), checks the address contained in the word, and produces a wrong-address pulse if the pulse is incorrect. The address check circuit also produces an all-receive pulse if the all-parties bit (16th bit, word 4) is a 1. The operation of the address check circuit consists of checking the address bits to determine whether the message is to be accepted and further processed.

3.9.1 Address Checking

In address checking, jumpers are connected to conform with the address of the receiving Central. The 25-counter-equals-12 line is connected to OR 2 (through J1) if the first bit of the receiving Central address is a 1 or is connected to the clear input of the flip-flop if the first bit of the receiving Central address is 0. The 25-counter-equals-13 line is jumpered (J2) to OR 2 if the second bit of the receiving Central address is a 1; the 25-counter-equals-14 line is jumpered (J3) to OR 2 if the third bit is a 1; and the 25-counter-equals-15 line is jumpered (J4) to OR 2 if the fourth bit is a 1. In figure 5—21, the proper connections for an address of 1101 are shown; i.e., J1, J2, and J4 are connected to OR 2.

If a 25-counter-12, -13, -14, or -15 pulse (XTL 6) is passed by the jumper connector to OR 2, it sets FF 1 which conditions GT 1. When the incoming word 4 data contains the correct address, address compare FF 1 is cleared each time by XTL (3 + 1) pulses applied to the complement input, and GT 1 is deconditioned.

When the incoming word 4 data contains the wrong address, one of two conditions results either of which causes a wrong-address output pulse:

a. Flip-flop 1 is set by one or more 25-counter -12, -13, -14, or -15 pulses (XTL 6) applied to its set input through a jumper connector and OR 2. It is not cleared by a corresponding word 4 data-address pulse (XTL 3 + 1) to its complement input.

b. Flip-flop 1 is not set by a 25-counter -12, -13, -14, or -15 pulse (XTL 6) (jumper not connected) to OR 2. A word 4 data-address pulse (XTL 3 + 1), applied to the complement input, sets FF 1.

Assume that FF 1 has been set, as described in a or b, above; GT 1 will be conditioned by the set output level of FF 1. The following counter 25-13, -14, -15, or -16 pulse (XTL 6), applied to GT 1 through OR 1, results in a wrong-address pulse at the output of GT 1, which is sent to the good message check circuit.

The timing chart (fig. 5–22) shows the operation of the circuit for two incoming messages; one containing the correct address for the central, 1101; and the other containing an incorrect address, 1111. In the first case, each time FF 1 is set (at XTL 6) by a 25-counter pulse, it is complement-cleared (at XTL 3 + 1) by a fourth word data bit. Therefore, the next 25-counter pulse finds GT 1 deconditioned; no wrong-address output pulse is produced. In the second case, the 25-counter-equals-13 and -14 pulses find GT 1 deconditioned. However, the third incoming address bit sets FF 1, permitting the 25-counter-equals-15 pulse to pass GT 1 as a wrong-address pulse.

3.9.2 All-Receive

The all-receive portion of the circuit produces an all-receive pulse when an incoming message is intended for all Centrals receiving it. The circuit consists of a gate which is conditioned by the word 4 data output of the buffer register and strobed by the 25-counter-equals-23 pulse. When the 25-counter is shifting from 23 to 24, the 16th bit of each word is leaving the buffer register. If the 16th bit of word 4 (the all-parties bit) is a 1, all-receive GT 2 passes the 25-counter-equals-23 pulse (XTL 6). This all-receive pulse is sent to the good message check circuit, indicating that the message is intended for all receiving Centrals.

3.10 PARITY CHECK

The parity check circuit checks the parity of each of the five XTL words and sends a wrong-parity signal to the good message check circuit if any of the words has an odd parity. The parity of each word is checked by an odd-even count of data bits; if an odd count results for any word, a wrong-parity signal is generated.

The parity check circuit (fig. 5–23) receives the data bits from the five XTL words as they are inserted into the buffer storage registers. The data bits of each word are applied to a separate gate. The five gates are simultaneously strobed by XTL 3 + 1 pulses. The output of each gate (an XTL 3 + 1 pulse whenever a 1 data bit is present) is applied to the complement input of a flip-flop. The outputs of GT's 1 through 5 go to the complement inputs of FF's 1 through 5, respectively.

At the start of a message, the sync XTL 6 pulse from the data converter and synchronizer clears the five

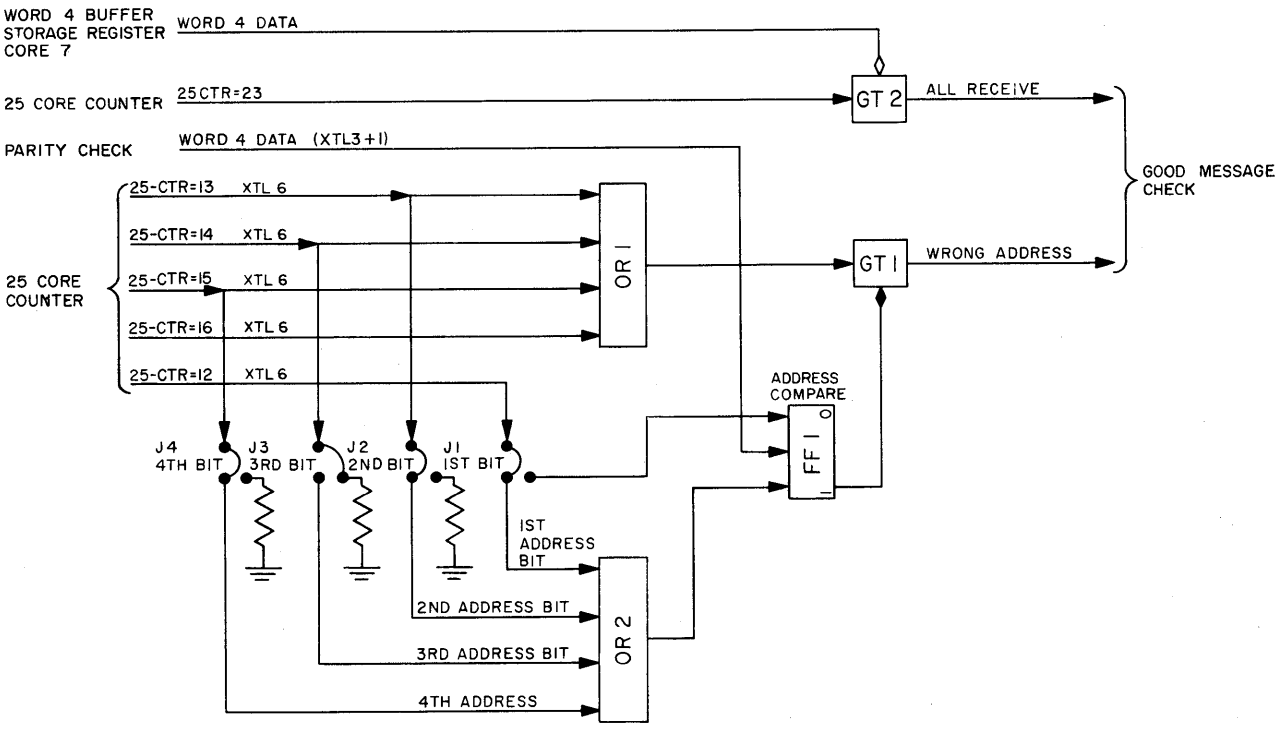


Figure 5–21. Address Check, Simplified Logic Diagram

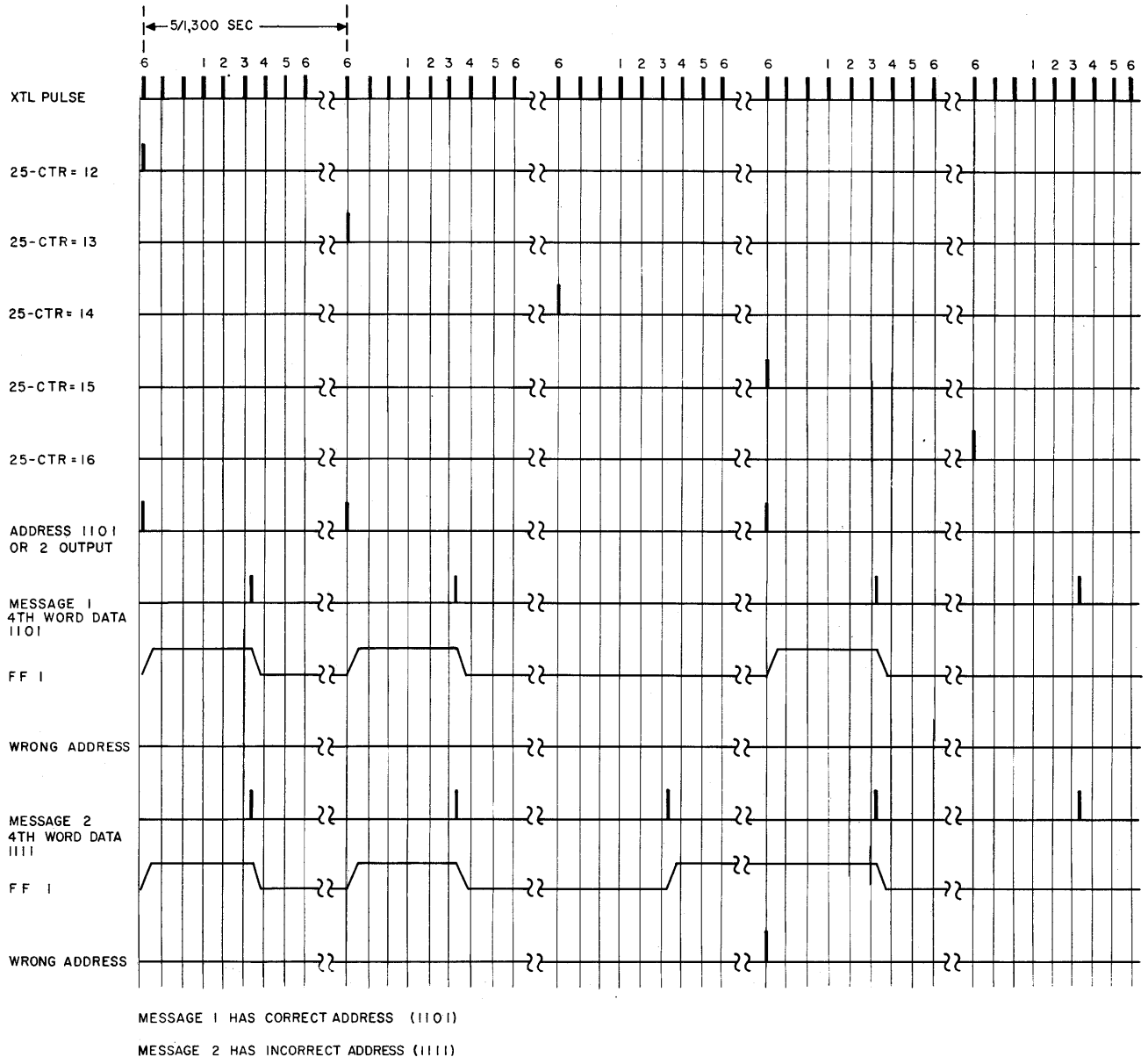


Figure 5—22. Address Check, Timing Chart

flip-flops. The first 1 data bit of the first word data allows an XTL 3 + 1 pulse to pass to the complement input of FF 1, setting it. The second 1 data bit of the first word allows an XTL 3 + 1 pulse to clear FF 1. After all the 1 bits in the first word data have been applied FF 1 is either cleared or set: an even number of 1's in the first word data leaves the flip-flop cleared; an odd number of 1's leaves it set. In the same manner, FF's 2 through 5 are cleared for an even number of 1's and set for an odd number of 1's in their respective words.

The set output of each of the five flip-flops is applied to OR 1. If any of the flip-flops has a set output after all the data bits have been applied (indicating an odd-parity count), the OR circuit sends a conditioning signal to GT 6. Gate 6 is strobed by the 25-counter-equals-24 pulse. Since all the data bits of the five words have been inserted into the buffer storage registers before the 25-counter-equals-24 time, the flip-flops have completed the parity count when the 25-counter-equals-24 pulse appears. If any of the flip-flops are set, an incorrect message has been received, and the 25-counter-equals-24 parity-error pulse passes to the good message check circuit. The parity-error pulse also sets parity error FF 6, causing an alarm indication on the channel control panel at the simplex maintenance console.

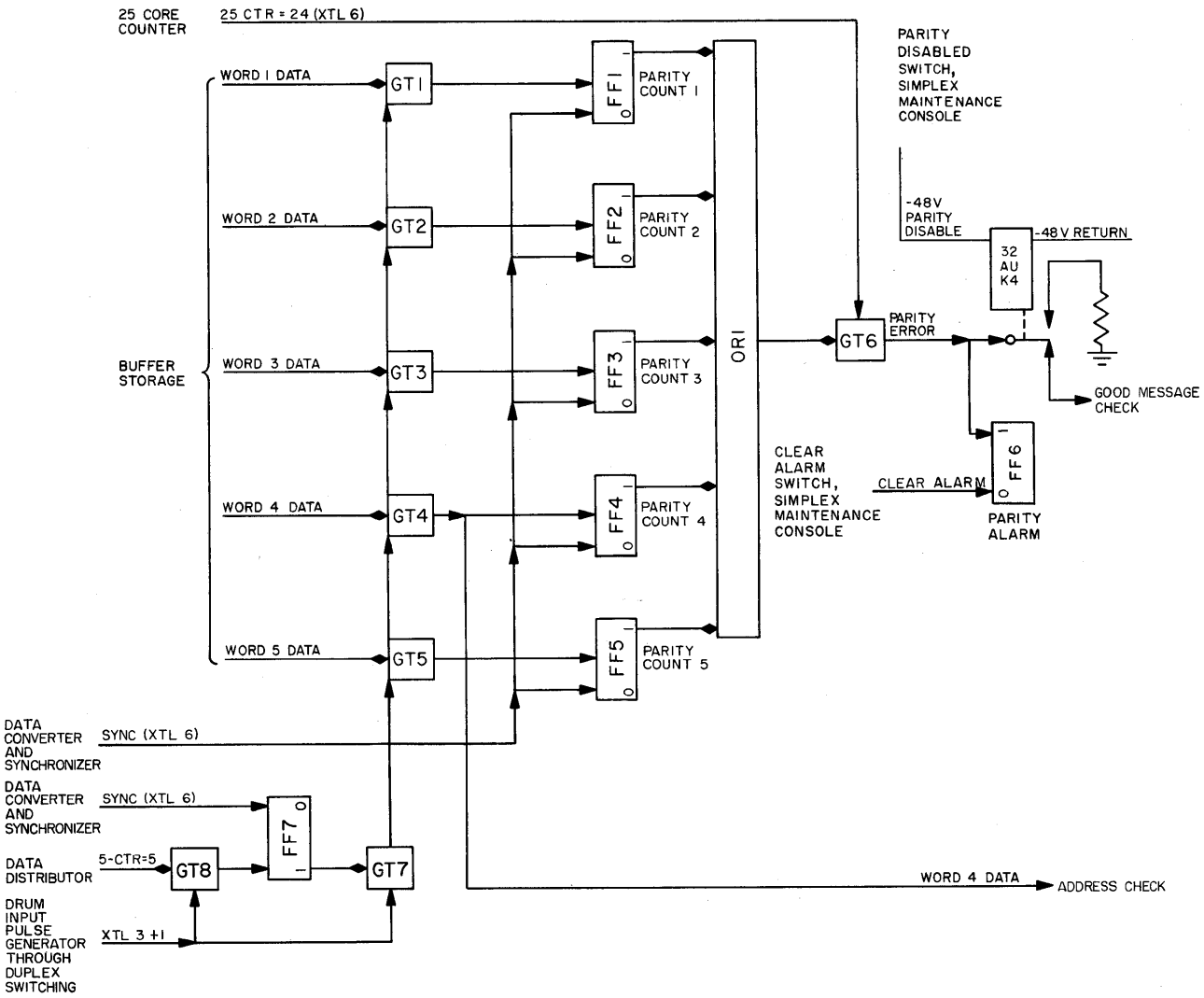


Figure 5–23. Parity Check, Simplified Logic Diagram

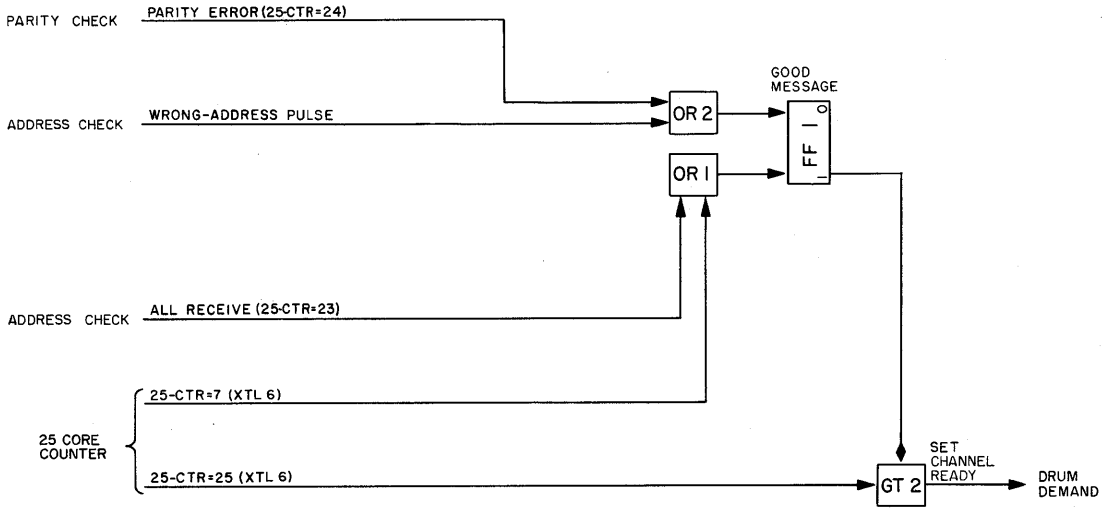


Figure 5–24. Good Message Check, Simplified Logic Diagram

Erroneous data bits which may occur during the second and third timing cycles are prevented from causing a false parity count. Flip-flop 7 is cleared by a sync XTL 6 and set at the following 5-counter-equals-5 time by an XTL 3 + 1 pulse applied via GT 8. Thus, GT 7 is deconditioned during the second and third timing cycles and GT's 1 through 5 are not strobed by the XTL 3 + 1 pulse.

The parity error circuit can be disabled during testing by activating relay 32AUK4, causing the parity-error signal to be bypassed to ground. This relay is activated by closing the PARITY DISABLED switch on the channel control panel, thus permitting wrong parity words to be read out to the drum input section. The PARITY ERROR neon continues to light when the parity is incorrect.

3.11 GOOD MESSAGE CHECK

The good message check circuit (fig. 5–24) provides a set-channel-ready pulse to the drum demand circuit when a good message has been received and inserted in the main storage registers. The conditions for a good message are:

a. The parity of each XTL word must be even.

b. The message address must correspond to the address of the Central receiving it or the message is intended for all Centrals.

A set-channel-ready level is produced by the set side of FF 1. This flip-flop is set by the 25-counter-equals-7 pulse (the message has just started to enter the main storage registers) and remains set unless cleared by an input through OR 2. This input may be a parity-error pulse from the parity check circuit at 25-counter-equals-24 pulse time or a wrong-address pulse from the address check circuit at 25-counter-equals-13, -14, -15, or -16 pulse time.

A wrong-address pulse (or pulses) will be produced when the incoming message is intended for all receiving Centrals; however, the all-receive pulse produced at 25-counter-equals-23 pulse time, by the address check circuit, sets FF 1 again.

Thus, when the parity of all incoming words is correct, and when the address is correct, FF 1 remains set (or, if cleared, is set again at 25-counter-equals-23 pulse time). The set side of FF 1 conditions GT 2, which then passes a 25 counter-equals-25 pulse as a set-channel-ready pulse to the drum demand circuit.

Figure 5–25 shows the timing relationships in the good message check circuit. The message illustrated in the timing chart is intended for all Centrals and has a parity error.

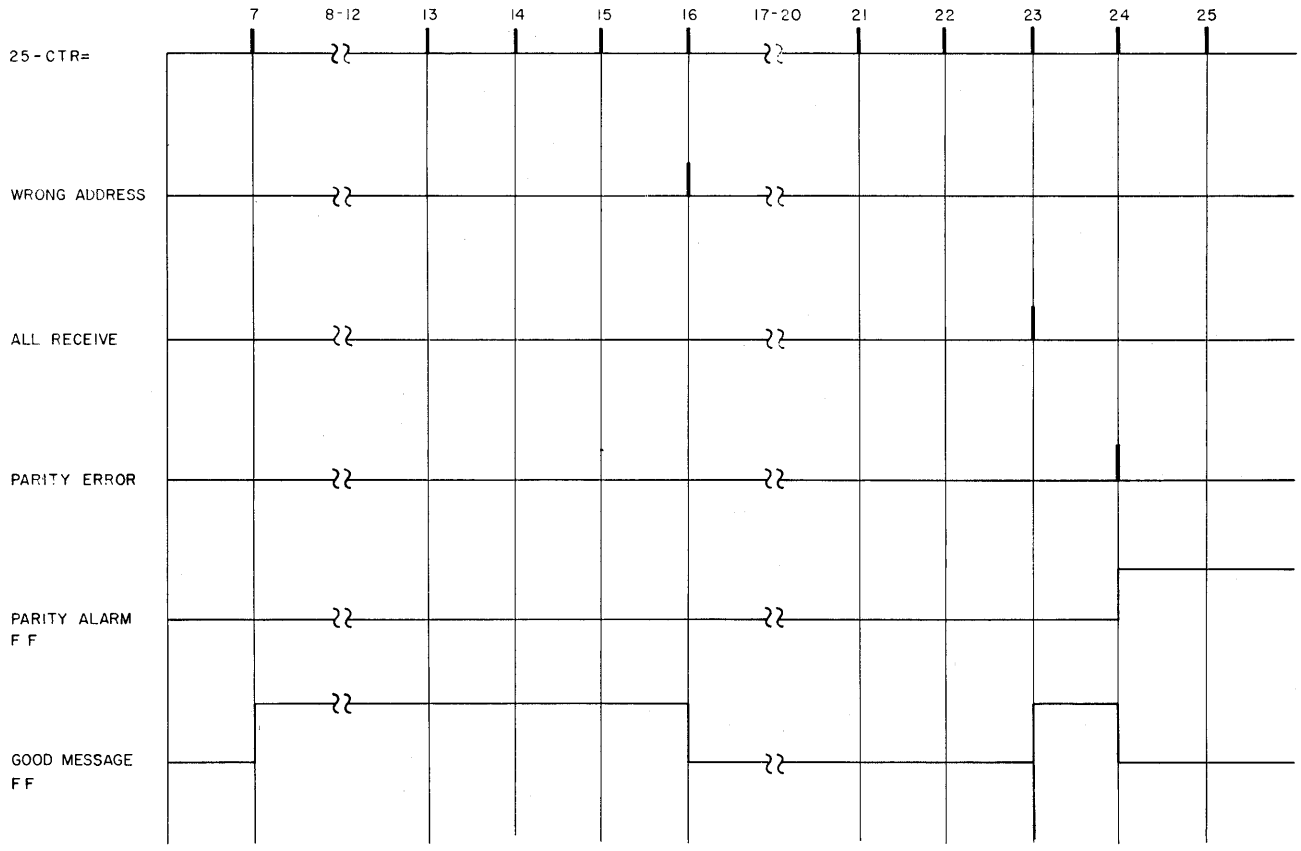


Figure 5–25. Good Message Check, Timing Chart

3.12 DRUM DEMAND

A drum-demand (DD) pulse (OD 3) is supplied to the channel input section through duplex switching when an empty XTL drum slot is available. The DD pulse is passed from one channel to another on a priority basis. If a good message (correct parity and address) is stored in the main storage registers, the DD pulse causes the drum demand circuit to produce a write signal. This signal is sent to the main storage readout control, where it initiates the readout process, and to the proper site identity generator (drum input section), where it causes the insertion of a site identity code into the first drum word.

If a good message is not stored in the main storage registers of a channel, the DD pulse is passed on to the channel of next highest priority. Thus, the DD pulse senses each channel in turn, causing the readout of one channel at a time in the order of priority.

In addition, the drum demand circuit generates an alarm pulse (readout alarm) whenever a new message is about to be loaded into the main storage circuit, if the main storage registers already contain a message awaiting transfer to the drum. This alarm is applied through the duplex switching section to the alarm circuit in the drum input section. The drum demand circuit also sends a start-readout pulse to the readout protection circuit.

When a good message (correct parity and correct address) has been stored in the main storage register, the good message check circuit passes a 25-counter-

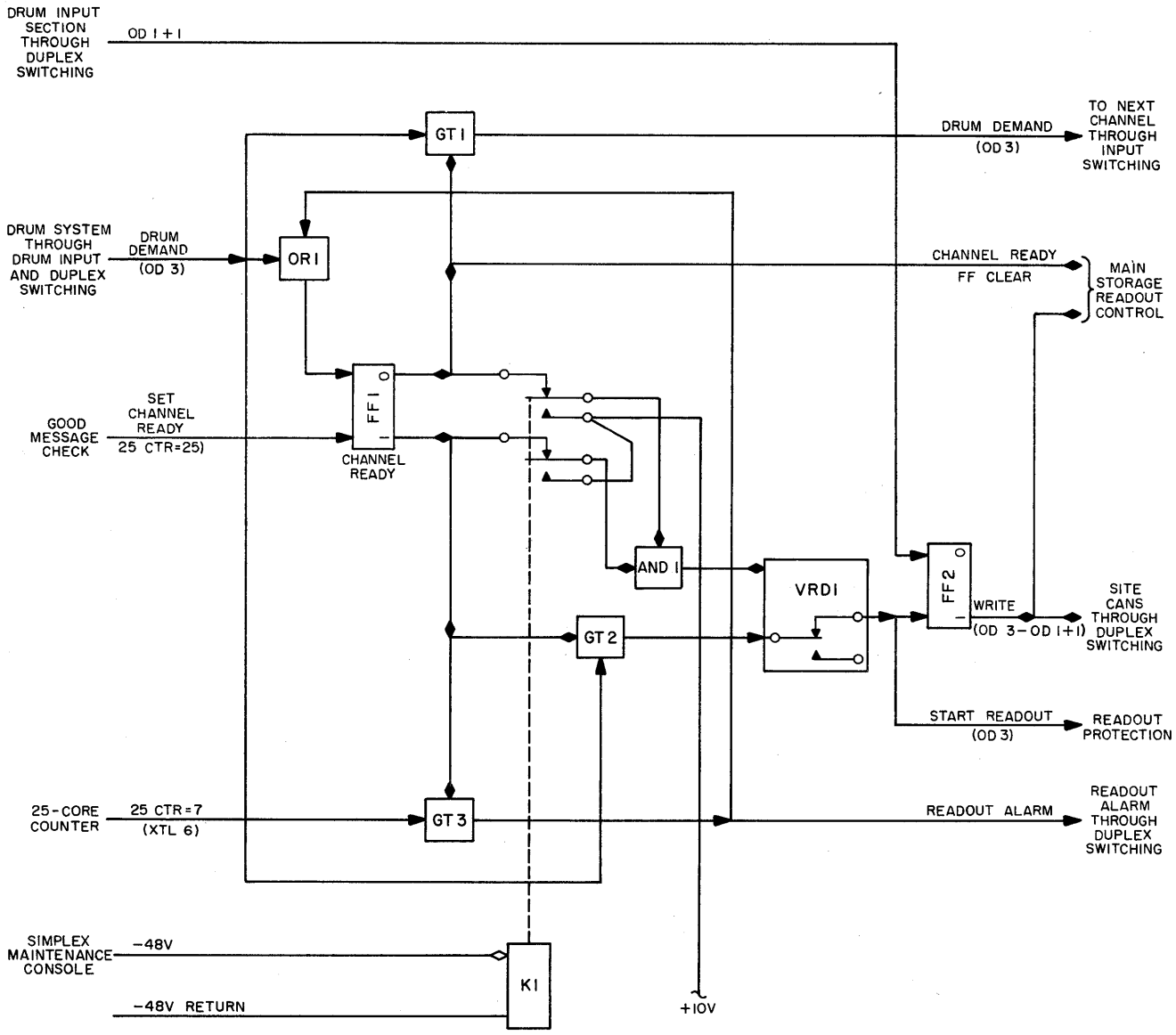


Figure 5–26. Drum Demand Circuit, Simplified Logic Diagram

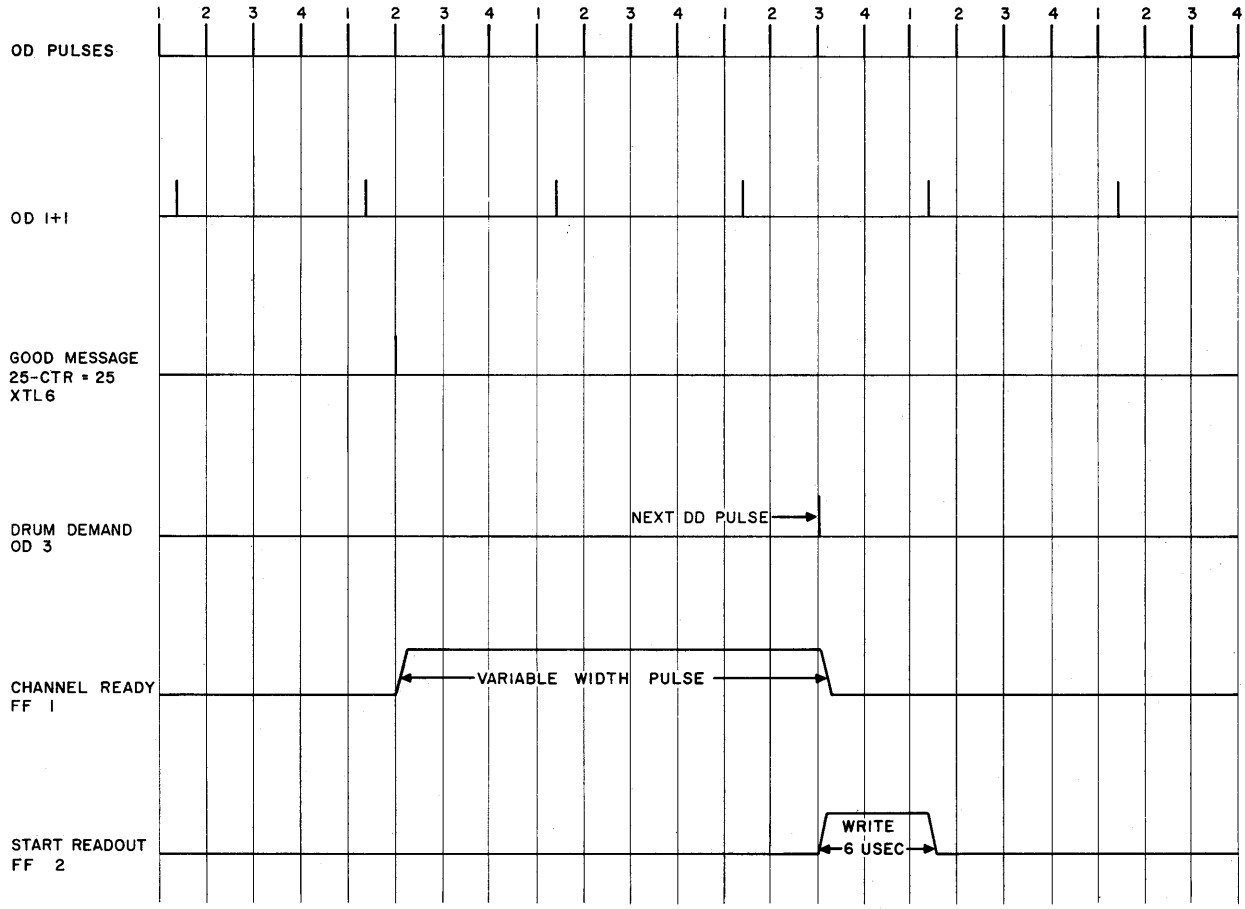


Figure 5–27. Drum Demand Circuit, Timing Chart

equals-25-good-message pulse to the drum demand circuit (fig. 5–26). The good-message pulse sets channel ready FF 1, conditioning GT's 2 and 3. The next DD pulse (OD 3) (indicating an open slot on the drum) is applied directly to GT 2 and is also used to clear channel ready FF 1, through OR 1. Because of the time delay of FF 1 (approximately 0.3 μsec), GT 2 remains conditioned long enough to pass the DD pulse. This pulse is used to set start-readout FF 2; it is also sent to the readout protection circuit. The set output of FF 2 is the write signal. Flip-flop 2 is cleared by an OD 1 + 1 pulse. The duration of the write signal is therefore 6 μsec (OD 3 to OD 1 + 1) (fig. 5–27).

While FF 1 is set, GT 3 is conditioned. Gate 3 is strobed by the 25-counter-equals-7 pulse, which occurs when the buffer register is about to apply the first data bit of an incoming message to the main storage register. If a previous message is contained in the main storage register, the incoming message will destroy the stored message. To indicate this condition, the 25-counter-equals-7 pulse is passed by GT 3 and is sent to the alarm circuit of the drum input section.

When the channel does not have a message in the main storage register, a set-channel-ready pulse is not applied to FF 1, which accordingly remains cleared, conditioning GT 1. The DD pulse is then passed through GT 1 to the drum demand circuit of the next priority channel.

Write and readout operations of a channel are halted if a faulty condition causes simultaneous up-level outputs from both sides of the channel ready flip-flop (FF 1). If both levels are present, a signal is applied to VRD1 via AND 1. The normally closed contacts of VRD1 open and prevent the output of GT 2 from initiating further write and readout signals. For maintenance test procedures, the CHANNEL READY TEST switch (simplex maintenance console) is used to simulate the above faulty conditions. With the switch in the TEST position, relay K1 is energized, causing +10V to be applied to both AND 1 inputs. The normally closed contacts of VRD1 should open, terminating the generation of write and readout signals and operations.

3.13 MAIN STORAGE READOUT CONTROL

The main storage readout control generates the readout signals that produce the readout of data from the main storage registers to the drum input system.

Three separate readout signals are required. The first readout signal is applied to the main storage register containing message word 1. The second readout is applied to the main storage registers for message words 2 and 3. The third readout is applied to the main storage registers for message words 4 and 5. In this manner of reading out message data, the five message words are converted into three words.

The circuit contains a 3-counter with a gated input (figs. 5–28 and 5–29). When a good message is stored in the main register and a DD pulse occurs (indicating an available slot on the drum), GT 2 is conditioned, permitting the counter to receive successive OD 4 pulses. The first, second, and third readout pulses are produced by the OD 4 pulses, and each has a duration of 10 μsec. After the third readout level, the input gate is no longer conditioned and the readout terminates.

A write level (produced in the drum demand circuit by a DD pulse when a good message is available for transfer to the drums) is applied through OR 1 to AND 4. The other two inputs to AND 4 perform safety or interlock functions, to be explained later. The output of AND 4 conditions GT 2, permitting OD 4 pulses to be counted. The AND 4 output is also sent as a good-message level through duplex switching to the drum input section; the function of this signal is discussed in Chapter 5.

The OD 4 pulses passing through GT 2 are applied to the complement input of FF 2 and through GT 1 to the complement input of FF 1. Flip-flops 1 and 2 are initially cleared. AND circuits 1, 2, and 3 are not conditioned, and GT 1 is closed before the application of the OD 4 pulse. The first OD 4 pulse sets FF 2. The set output of FF 2 and the cleared output of FF 1 cause AND 1 to produce an output level, designated first readout. The output of FF 2 is also used to condition GT 1 directly and is applied through OR 1 to AND 4. This is necessary to condition GT 2 since the write pulse previously applied through OR 1 has now terminated. The second OD 4 pulse passes conditioned GT 1 to the complement input of FF 1. Flip-flop 1 is set, and the 1 output is applied to AND 2. The second OD 4 pulse also clears FF 2, conditioning AND 2 and producing the second readout signal. The clearing of FF 2 closes GT 1. The third OD 4 pulse sets FF 2. The set outputs of FF's 1 and 2 are applied to AND 3, producing the third readout signal. The set output of FF 2 also conditions GT 1 after the third OD 4 pulse has terminated.

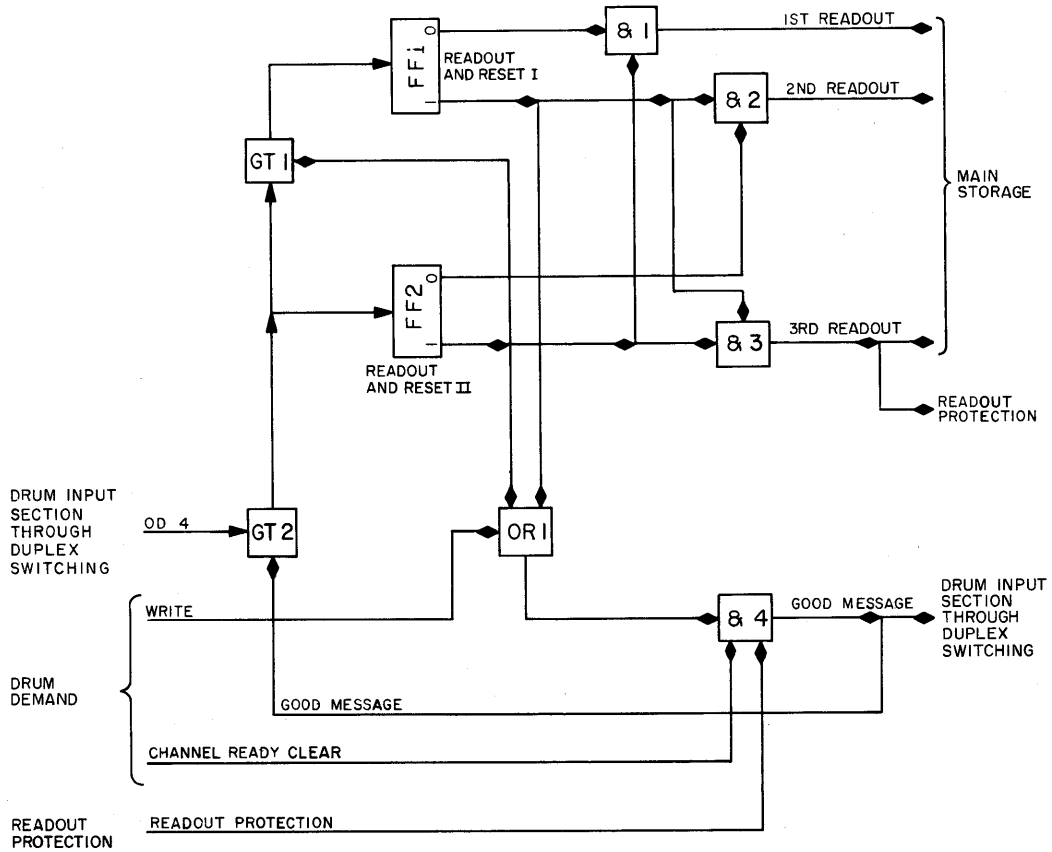


Figure 5–28. Main Storage Registers Readout Control, Simplified Logic Diagram

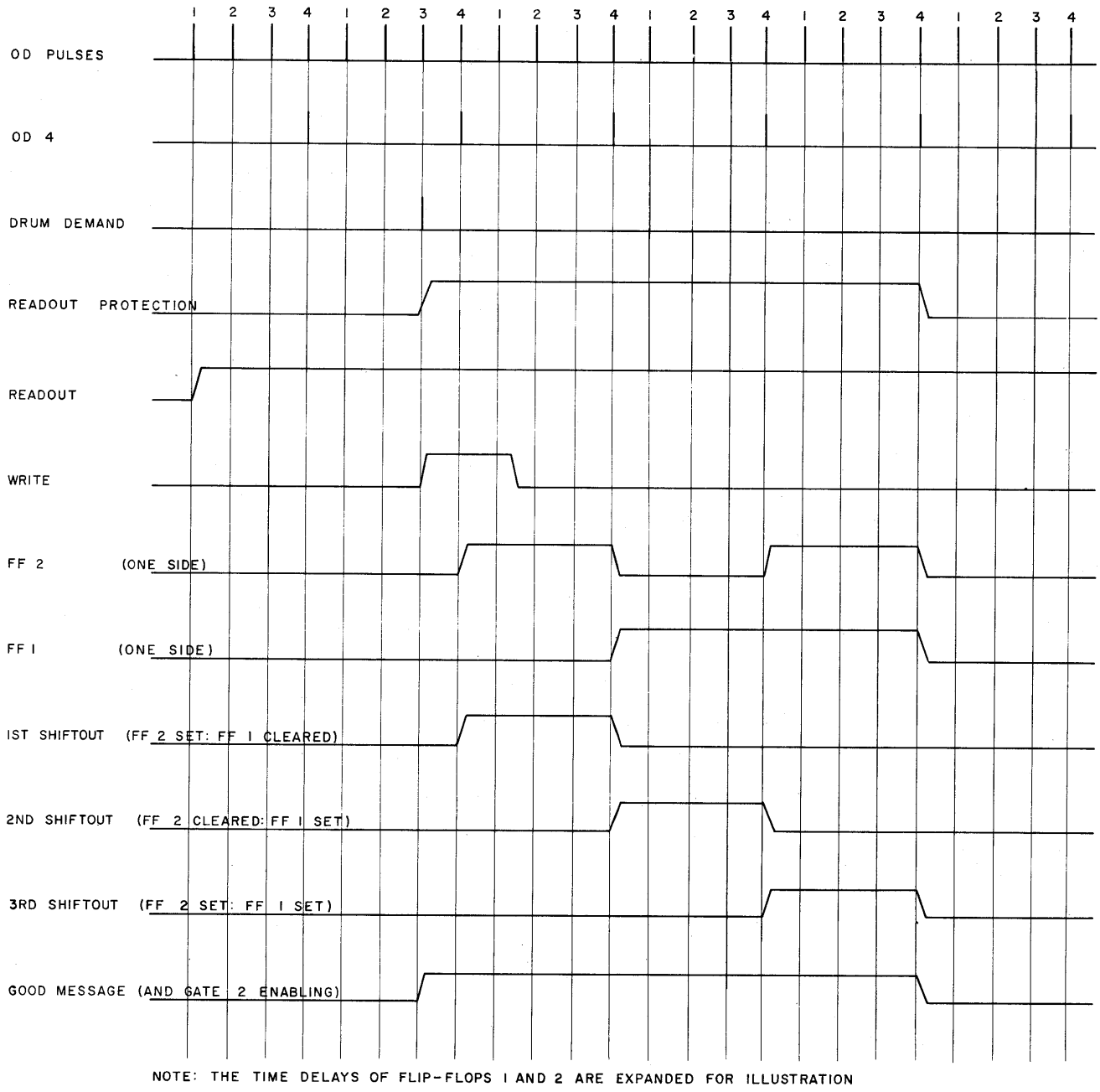


Figure 5–29. Main Storage Registers Readout Control, Timing Chart

The fourth OD 4 pulse clears FF's 1 and 2, terminating the third readout signal and removing one of the inputs to AND 4. AND 4 no longer has an output so that GT 2 is now closed, preventing further OD 4 pulses from passing. The circuit remains closed until a new message is ready for transfer to the drum.

The two safety inputs to AND 4 are the channel-ready-clear signal and the readout-protection signal. The channel-ready-clear signal originates in the clear side of the channel-ready flip-flop (drum demand circuit) and offers protection against the sticking of the flip-flop to the 1 side. The readout-protection signal protects against continuous message readout due to circuit malfunction; its generation is discussed below.

3.14 READOUT PROTECTION

The readout-protection signal prevents a constant readout to the XTL common equipment section by disabling the good-message pulse as soon as the readout of a message is completed. The circuit (fig. 5–30) con-

sists of a readout protection flip-flop and a gate. The start-readout pulse (an OD 3 drum demand) sets the flip-flop. The third readout pulse from the main storage readout control, indicating the end of the readout, conditions the gate, permitting an OD 4 pulse to pass and to clear the flip-flop. The readout protection line is up only during readout and is down when a readout is completed.

3.15 MESSAGE WORD PARITY TRANSFER

The message word parity transfer circuit transfers the message word parity bits to the drum input section during readout of the main storage register. The circuit (fig. 5–31) receives the parity (17th) bit of each message word as it is shifted out of the main storage register.

When the first readout level is applied to the main storage register, the 17th bit (parity) of word 1 is applied to OR 2. The output of OR 1 goes to the drum parity circuit in the drum input section through duplex switching. When the second readout level is applied to the main storage register, the parity bits of words 2 and 3 are sent through OR 1 and OR 2, respectively, to the drum parity circuit through duplex switching. The third readout level sends the fourth and fifth word parity bits to OR 1 and OR 2, respectively. The transfer of the parity bits is necessary so that the drum parity section can produce correct drum word parity, as explained in Chapter 5.

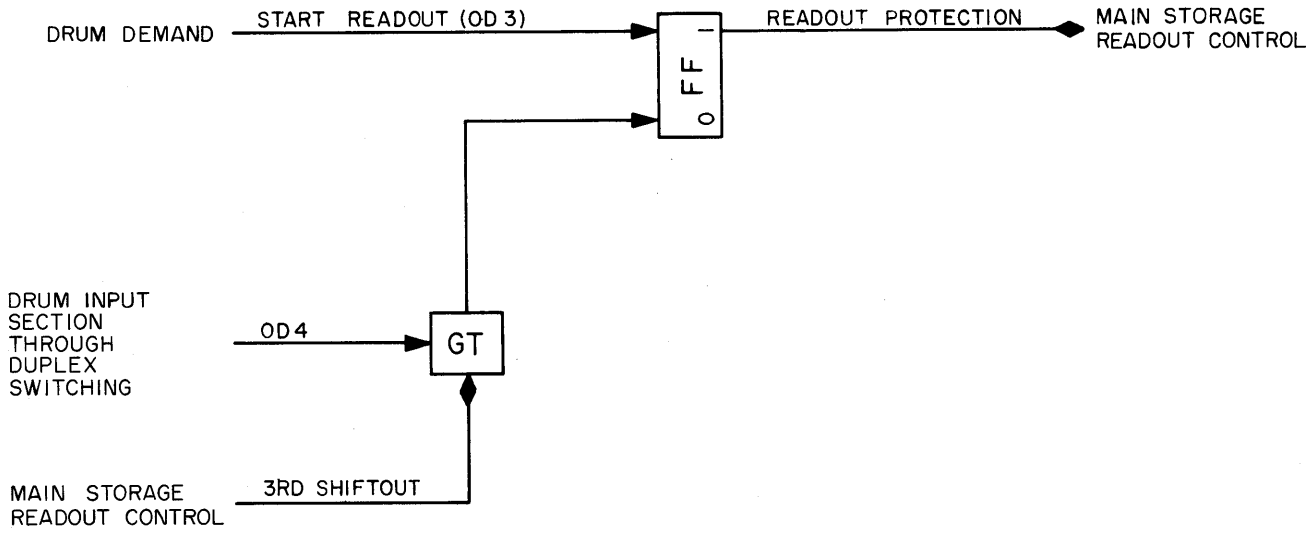


Figure 5–30. Main Storage Readout Protection, Simplified Logic Diagram

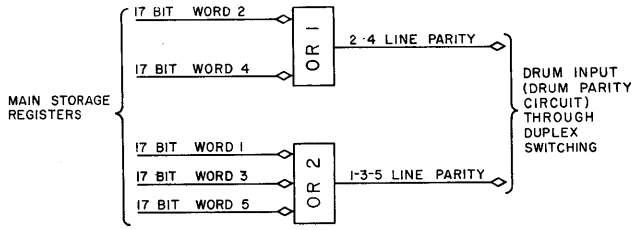


Figure 5–31. Message Word Parity Transfer, Simplified Logic Diagram

CHAPTER 4
DUPLEX SWITCHING

4.1 GENERAL

Duplex switching relates simplex equipment to the proper, A or B, duplex computer; that is, it associates simplex equipment in the active status with the duplex computer currently in the active status and standby simplex equipment with the standby duplex computer.

In the XTL element, duplex switching provides the circuitry required to perform the following specific functions:

a. Core data switching: transfers the five message words, including the message word parity bits, assembled in the main storage register, to the proper half (A or B) of the drum input section.

b. Write level switching: transfers the write level generated in the channel input section to the proper half of the drum input section. In spare channel switching (2.3, Ch 2), the write level generated in the spare channel circuits must be switched to the site identity can for the replaced channel; accordingly, write level switching involves both duplex and simplex switching when a spare channel is switched.

c. Site neon indication switching: energizes the proper set, A or B, of site neon indicators on the channel control panel (simplex maintenance console).

d. Good-message level and readout alarm switching: transfers the good-message level and (if produced) readout alarm signal from the channel input section to the proper half of the drum input section.

e. Drum demand switching: transfers DD pulses from the proper, A or B, Drum System to the channel input section of the various channels, on a priority basis.

f. OD and XTL timing switching: transfers the OD pulses and the XTL pulses and levels from the proper half of the drum input section to the channel input section.

g. Status indication switching: sends status indication signals from each channel to the proper half of the MDI element.

4.2 DRIVING OF A AND B SIGNAL RELAYS

The functions listed above are performed by means of sets of relays, designated A signal relays and B signal relays. The driving circuit for these relays is shown in figure 5–32. Voltage is applied to terminals of UNIT STATUS switch sections G and H. Section G controls the energizing of the A signal relays; section H, the B signal relays.

Assume that the A computer has been designated active and the B computer standby (by the duplex selection control at the duplex switching console). Relay driving voltage is then applied to terminal 1 (ACTIVE) of section G and to terminals 3-4 (STANDBY, STANDBY MC of the unit status switch of each channel). If this switch is placed in the ACTIVE position, driving voltage is applied to the A signal relays; if this switch is placed in the STANDBY or STANDBY MC position, driving voltage is applied to the B signal relays. Reversing the status of the A and B computers reverses the effect of the unit status switch positions on the signal relays.

The signal control relays for channel 1 are listed and their functions are indicated in table 5–3. Each contact group of a relay (if used) performs a specific function, and corresponding contact groups of paired A and B signal relays perform the same functions. Thus, when A signal relay 32AT(K4) is energized, contact group 5 causes transfer of the good-message level from channel 1 to the A drum input section; if the B signal relays are picked, contact group 5 of 32AT(K5) transfers the good-message level from channel 1 to the B drum input section.

The detailed operation of the signal relays for channel 1 is discussed by function below; different relays, tabulated in the Input System schematic books, are employed in other channels, but their operation is the same as that of analogous relays in channel 1.

4.3 CORE DATA SWITCHING CIRCUIT

The core data switching circuit switches the output of the main storage registers of each channel to drum input section A when the A signal relays are picked or to drum input section B when the B relays are picked. The outputs of the corresponding core (e.g., the LS core) of words 1, 3, and 5 and of words 2 and 4 are combined through diodes and connected to contacts of the A and B signal relays. The diodes serve to isolate the core data output of each channel from that of other channels.

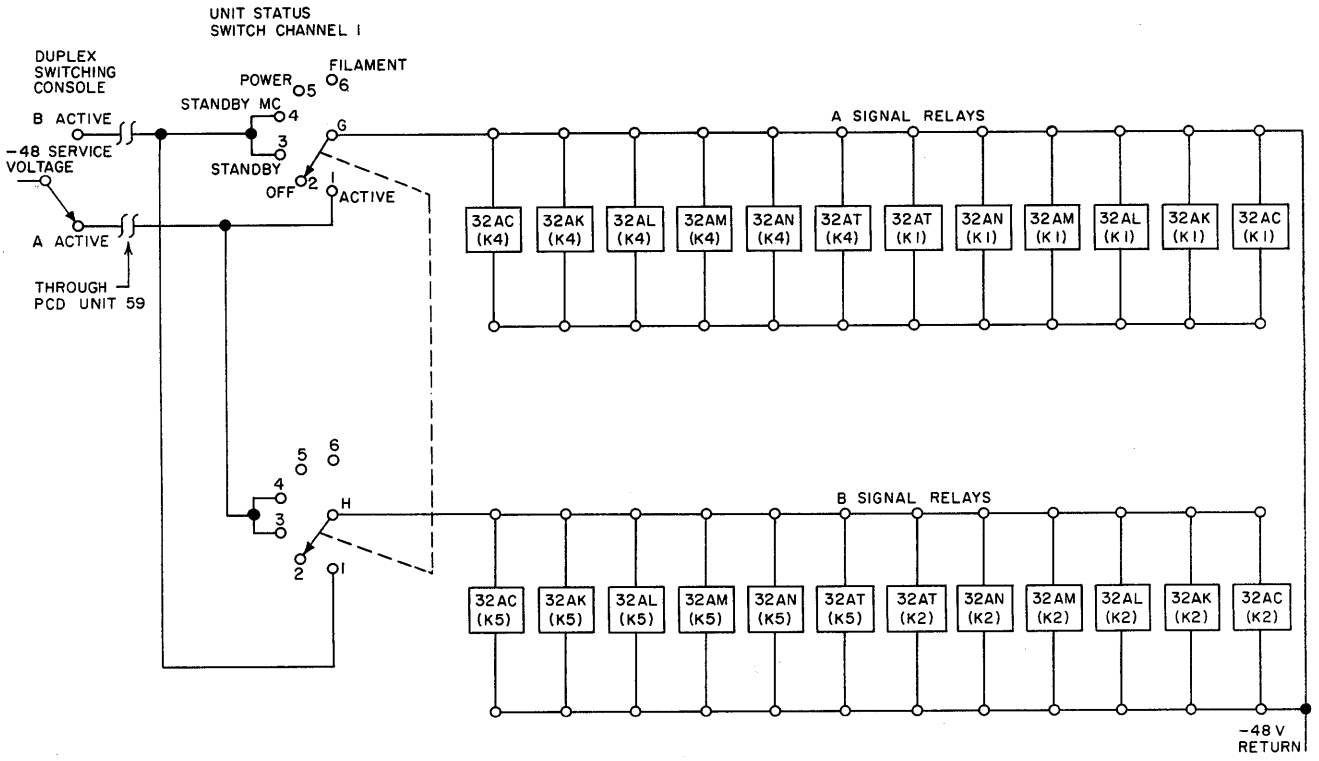
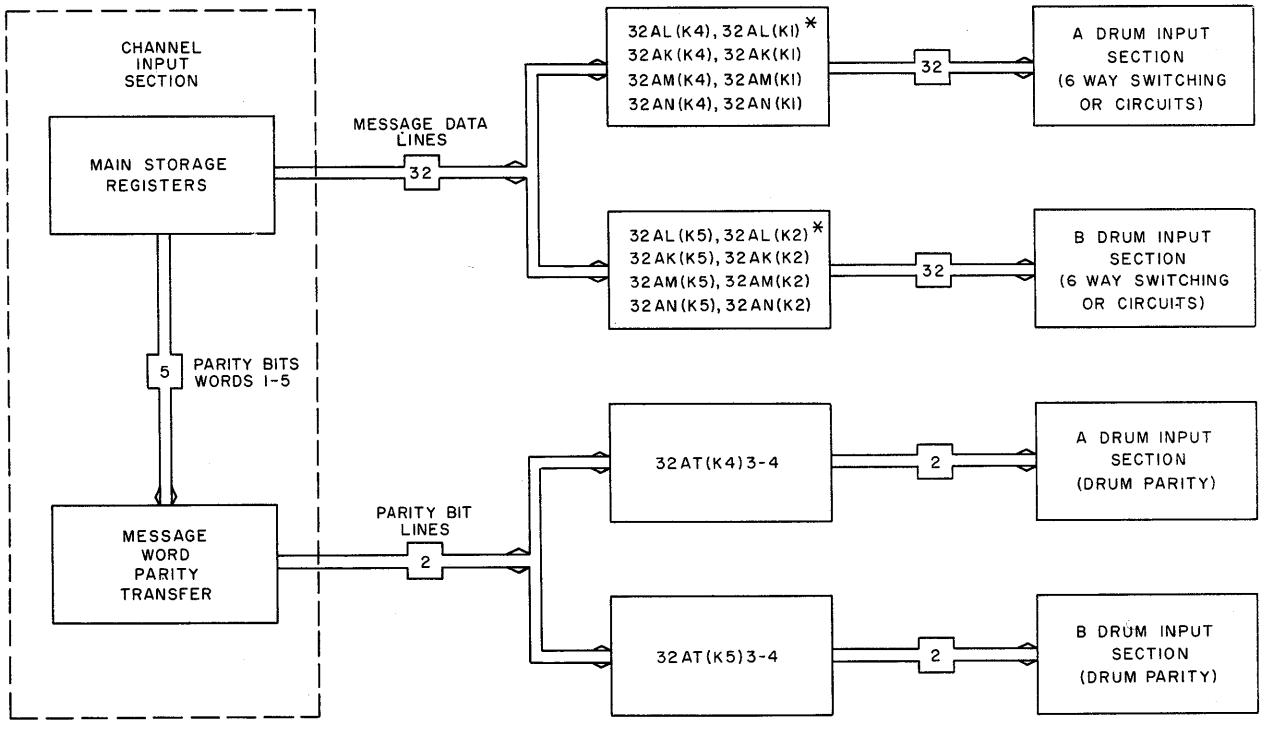


Figure 5–32. A and B Signal Relays Driving Circuit, Simplified Logic Diagram



* REFER TO TABLE 5-3 FOR CONTACT GROUPS EMPLOYED TO TRANSFER SPECIFIC BITS

Figure 5–33. Core Data Transfer, Simplified Schematic Diagram

The circuit for the LS core of words 1, 3, and 5 is shown in figure 5–33. When A signal relay 32AL(K4) has been energized, the 6a-6c contacts of 32AM(K4) and 32AM(K5) serve the same purpose for the RS bit of words 2 and 4. Refer to table 5.3 for the relay connections for the other bits of channel 1.

The parity lines for words 1, 3, and 5 are combined in an OR circuit and connected to A signal relay contact 32AT(K4)4 and B signal relay contact 32AT(K5)4. Contacts 32AT(K4)3 and 32AT(K5)3 perform the same function for the parity bits of words 2 and 4. Coincidentally with word readout, the parity bits for the message words are transferred to appropriate circuits in the A or B drum input section.

4.4 WRITE LEVEL SWITCHING

Write level switching connects the write level produced by the drum demand circuit of the channel input section to the A or the B site can for the channel. In channel 1, the write level is applied to contact 2a of A signal relay 32AK(K1) and to contact 2a of B signal relay 32AK(K2). Depending on which relay is energized, the write level is applied to the site can for channel 1 in the A or B drum input section.

In spare channel switching, the write level generated in the spare channel (6) must be applied to the site can for the replaced channel, in the proper A or B drum input section. Write level switching and spare channel switching are both required to make the proper connection, as shown in figure 5–34. Assume that the spare channel has replaced channel 1 (CHANNEL SELECTOR switch set to 1) and that the A signal relays have been energized. The write level generated in channel 6, channel input section, is then applied through contact 2 of signal relay 32FK(K1) and contact 1 of spare channel relay 32FD(K1).

TABLE 5–3. FUNCTIONS OF SIGNAL RELAYS, CHANNEL 1

FUNCTION	B SIGNAL RELAY	A SIGNAL RELAY
Core data transfer: LS	32AL(K4)6	32AL(K5)6
L1	32AL(K4)5	32AL(K5)5
L2	32AL(K4)4	32AL(K5)4
L3	32AL(K4)3	32AL(K5)3
L4	32AL(K4)2	32AL(K5)2
L5	32AL(K1)5	32AL(K2)5
L6	32AL(K1)4	32AL(K2)4
L7	32AL(K1)3	32AL(K2)3
L8	32AL(K1)2	32AL(K2)2
L9	32AK(K4)6	32AK(K5)6
L10	32AK(K4)5	32AK(K5)5
L11	32AK(K4)4	32AK(K5)4
L12	32AK(K4)3	32AK(K5)3
L13	32AK(K4)2	32AK(K5)2
L14	32AK(K1)6	32AK(K2)6
L15	32AK(K1)5	32AK(K2)5
RS	32AM(K4)6	32AM(K5)6
R1	32AM(K4)5	32AM(K5)5
R2	32AM(K4)4	32AM(K5)4
R3	32AM(K4)3	32AM(K5)3
R4	32AM(K4)2	32AM(K5)2

TABLE 5–3. FUNCTIONS OF SIGNAL RELAYS, CHANNEL 1 (Cont'd)

FUNCTION	B SIGNAL RELAY	A SIGNAL RELAY
R5	32AM(K1)5	32AM(K2)5
R6	32AM(K1)4	32AM(K2)4
R7	32AM(K1)3	32AM(K2)3
R8	32AM(K1)2	32AM(K2)2
R9	32AN(K4)6	32AN(K5)6
R10	32AN(K4)5	32AN(K5)5
R11	32AN(K4)4	32AN(K5)4
R12	32AN(K4)3	32AN(K5)3
R13	32AN(K4)2	32AN(K5)2
R14	32AN(K1)3	32AN(K2)3
R15	32AN(K1)2	32AN(K2)2
Word 2-4 parity bit	32AT(K4)3	32AT(K5)3
Word 1-3-5 parity bit	32AT(K4)4	32AT(K5)4
Write level	32AK(K1)2	32AK(K2)2
Site neon indication (+150V)	32AT(K1)6	32AT(K2)6
Good-message level	32AT(K4)5	32AT(K5)5
Readout alarm	32AC(K1)4	32AC(K2)4
Drum demand: Into channel	32AC(K4)4	32AC(K5)4
To next channel	32AC(K4)6	32AC(K5)6
OD and XTL timing OD 1-D	32AC(K4)2	32AC(K5)2
OD 4	32AT(K1)4	32AT(K2)4
XTL 1	32AC(K1)6	32AC(K2)6
XTL 3-D	32AC(K1)2	32AC(K2)2
XTL 6	32AC(K1)3	32AC(K2)3
XTL 2/3	32AT(K4)6	32AT(K5)6
XTL 5/6	32AK(K1)3	32AK(K2)3

4.5 SITE NEON INDICATION SWITCHING

Each channel control panel (simplex maintenance console) contains two sets of site identity indicators, indicating, in 5-bit code, the identity of the site with which the channel communicates. The A set of indicators is active when the channel is in the same status as the A machine; the B set is active when the channel is in the same status as the B machine. Only one set of indicators (A or B) can be lighted at a time.

4.6 GOOD-MESSAGE LEVEL AND READOUT ALARM SWITCHING

The good-message level, generated in the main storage readout control circuit (3.13, Ch 3), is applied to A signal relay 32AT(K4) and B signal relay 32AT(K5). The level is transferred to the A drum input section when the A signal relays are energized and to the B drum input section when the B signal relays are energized.

The readout-alarm pulse is generated in the drum demand circuit (3.12, Ch 3) when a message is about to

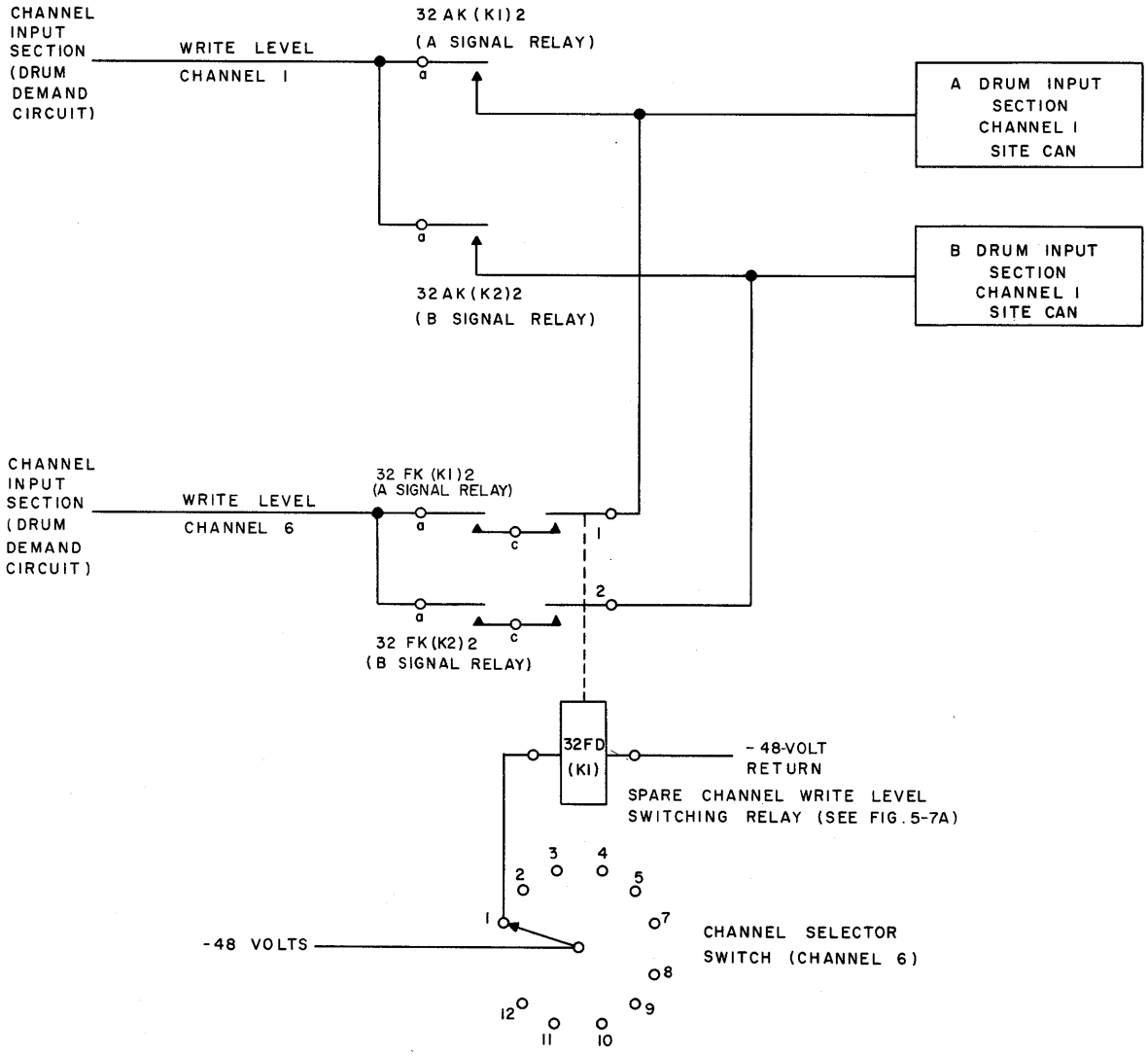


Figure 5–34. Write Level Transfer, Spare Channel Switching, Simplified Schematic Diagram

be shifted into main storage registers that already hold a message. The pulse is applied to A signal relay 32AC(K1) and to B signal relay 32AC(K2) and is transferred accordingly to the A or B half of the drum input section, depending on which set of signal relays has been energized.

Note

The 1 set of contacts on the A and B signal relays are series-connected with the A SIGNAL CONTACTORS CLOSED and B SIGNAL CONTACTORS CLOSED indicators, respectively, on the channel control panel. Thus, failure of one signal relay in the A or B group to energize will cause the appropriate indicator to remain unilluminated.

Corresponding relays for other channels are tabulated or indicated on logic schematic diagrams, as follows:

Core Data	S 2.3.4
Line Parity	S 2.3.2 Charts II-III
Write Level	S 2.3.3
Good-Message Level	S 2.3.2 Chart IV
Readout Alarm	S 2.3.2 Chart I
Drum Demand	S 2.3.2
OD and XTL Timing	A 2.3.5
	B 2.3.5

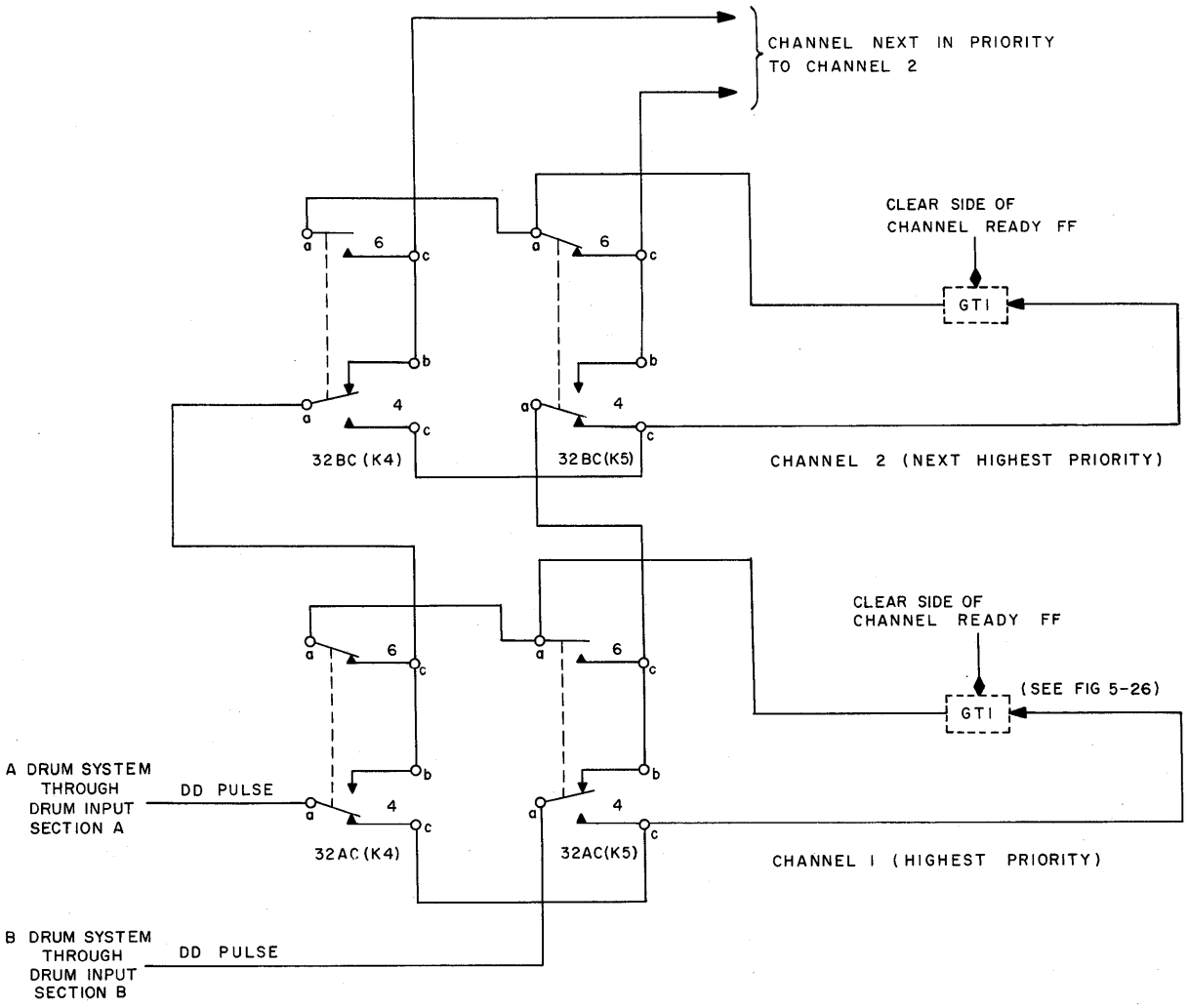
4.7 DRUM DEMAND SWITCHING

Drum demand pulses from the Drum System are supplied to the channel input section to indicate an

empty slot on the drum field assigned to XTL data. The DD pulses from the A Drum System are fed to channels in the same status, active or standby, as the A computer, whereas the B Drum System supplies the channels in the same status as the B computer.

The DD pulse is applied to channels on a priority basis. The pulse senses (in the drum demand circuit) for the presence of a good message prepared for transfer to the drum input section. If it does not find such a condition, it is passed without delay to the channel of the next highest priority, until all channels are sensed. Drum demand pulses from the A Drum System may be sensing channels associated with the A computer at the same time that DD pulses from the B Drum System sense channels associated with the B computer.

The drum demand switching circuit for each channel makes use of two sets of contacts on two relays (fig. 5–35). The DD pulse from the A Drum System is applied to contact 4a of A signal relay 32AC(K4). The DD pulse from the B Drum System is applied to contact 4a of B signal relay 32AC(K5). When the A signal relays are energized, the DD pulse from the A Drum System is fed to the channel. If the channel has not prepared a message for transfer to the drum input section, the DD pulse is applied to contact 6a of A signal relay 32AC(K4) and B signal relay 32AC(K5)



NOTE : AS SHOWN, CHANNEL 1 IS ASSOCIATED WITH A MACHINE (A SIGNAL RELAYS ENERGIZED) AND CHANNEL 2 IS ASSOCIATED WITH B MACHINE (B SIGNAL RELAYS ENERGIZED)

Figure 5–35. Drum Demand Switching, Channels 1 and 2, Simplified Schematic Diagram

and is passed by 6a and 6c of 32AC(K4) to the A drum demand input of the next channel. If the A signal relay is not energized, the A DD pulse passes through 4a-4b-6c of 32AC(K4) to the next channel, bypassing the channel completely. The B drum demand switching circuit is analogous to the A drum demand switching circuit.

4.8 OD PULSE AND XTL PULSE AND LEVEL SWITCHING

The OD pulse and XTL pulse and level switching circuitry switches the timing pulses and levels generated in, or made available by, the A and B drum input section to the channels associated with the A and B computer, respectively. Refer to 3.1, Ch 3, for a list of these timing pulses and levels and to table 5–3 for the A and B signal relays involved in their transfer.

4.9 STATUS INDICATION SWITCHING

Each computer is kept informed of the channels with which it is associated. When a signal relay is energized, 10V is applied to an assigned core in the direct entry section of the MDI element. Periodically, the cores (organized as a core matrix) are read out to the Central Computer. When the A signal relays for channel 1 are energized, the +10V is applied through contact 5 of relay 32AT(K1); when the B relays for channel 1 are energized, the +10V is applied through contact 5 of 32AT(K2).

CHAPTER 5

CROSSTELL DRUM INPUT (COMMON) SECTION

5.1 INTRODUCTION

The drum input section performs six basic functions in the processing of XTL messages:

a. It funnels the outputs of the 24 channels into one section. The outputs of the channels are the five message words and accompanying pulses and levels developed by the channel input sections and fed to the drum input section in the order of channel priority.

b. It adds to each message the Central Computer clock time, the identity of the site at which the message originated, and the drum word parity bits.

c. It transfers the XTL message in the form of three drum words to the Drum System.

d. It provides the channel input section with the synchronizing XTL pulses and levels that channel input operations require.

e. It indicates at the duplex maintenance console certain alarm conditions which may occur in the processing of the XTL message.

f. It informs one of two drum fields (in the Drum System) of an imminent message transfer.

Because failure of the drum input section would inactivate all XTL inputs to the Central Computer, the system is duplex. If the A machine is active, all channels in the active status are associated through duplex switching with the A drum input section; channels in the standby status are then associated with the B drum input section. If the statuses of the A and B machines are reversed, duplex switching automatically associates each channel, in accordance with its status, with the proper half of the drum entry section.

In the following discussion, it is assumed for simplicity that all channels are in the same status and consequently associated with the same half of the drum input section.

5.2 BLOCK DIAGRAM ANALYSIS OF DRUM INPUT SECTION

The block diagram (fig. 5—36) shows the major circuits in the drum input section. The operation of these circuits is first discussed generally in terms of the circuit contribution to the performance of basic drum input section functions (see listing in 5.1). Then the various blocks in figure 5—36 are discussed on the logic diagram level.

5.2.1 Consolidation of Output Lines of 24 Channels

The funneling of the outputs of 24 channels into one common section is possible because only one channel can send a message to the drum input section at one time. As explained in 3.12, Ch 3, when an empty drum slot is in a position to receive an XTL message, a DD pulse is sent to the drum demand circuit of channel 1 (top priority channel). If channel 1 contains a message that is ready for transfer to the Drum System, the DD pulse initiates the readout process. If channel 1 does not contain a message, the drum demand circuit will transfer the DD pulse to channel 2 (next priority channel) where it will initiate readout or pass to channel 3.

Consolidation of the outputs of the 24 channels is accomplished by OR circuits shown in figure 5—36. Previously, in the channel input section, like message-bit lines and parity-bit lines of the words 1, 3, and 5 main storage registers have been consolidated; similarly, output lines of the words 2 and 4 main storage registers have been consolidated. Consequently, each channel feeds 32 message bit lines and two parity lines to duplex switching. One hundred and twenty-eight 6-way switching OR circuits, which are physically part of duplex switching, followed by 32 4-way OR circuits, consolidate the like message-bit lines of the 24 channels. For example, the LS bit lines of channels 1 through 6 are consolidated in one 6-way switching OR; likewise, the LS bit lines for channels 7 through 12, 13 through 18, and 19 through 24 are consolidated in separate 6-way OR's for each group of channels shown. The output of the 6-way OR's are further incorporated by a 4-way OR to form one LS bit line. Each of the remaining bit lines (L1-L15, RS-R15) is combined in a similar manner to form a total of 32 bit lines which are fed to the XTL amplifiers.

The 24 good-message level lines are consolidated into two lines by two 12-way OR's; the two lines are then combined, by a 2-way OR, into a single good-message level line. The 24 readout alarm lines are consolidated in a similar manner to form one readout

alarm pulse line. The two parity bit lines from each of the 24 channels are consolidated into two lines; the combined clock and site parity line is incorporated with the words 2 and 4 parity line. Write-level lines are not combined; each is fed to the appropriate site identity generator.

Since only one channel is read out at a time, there can be only one input to each of the OR circuits referred to above and to the site identity generators.

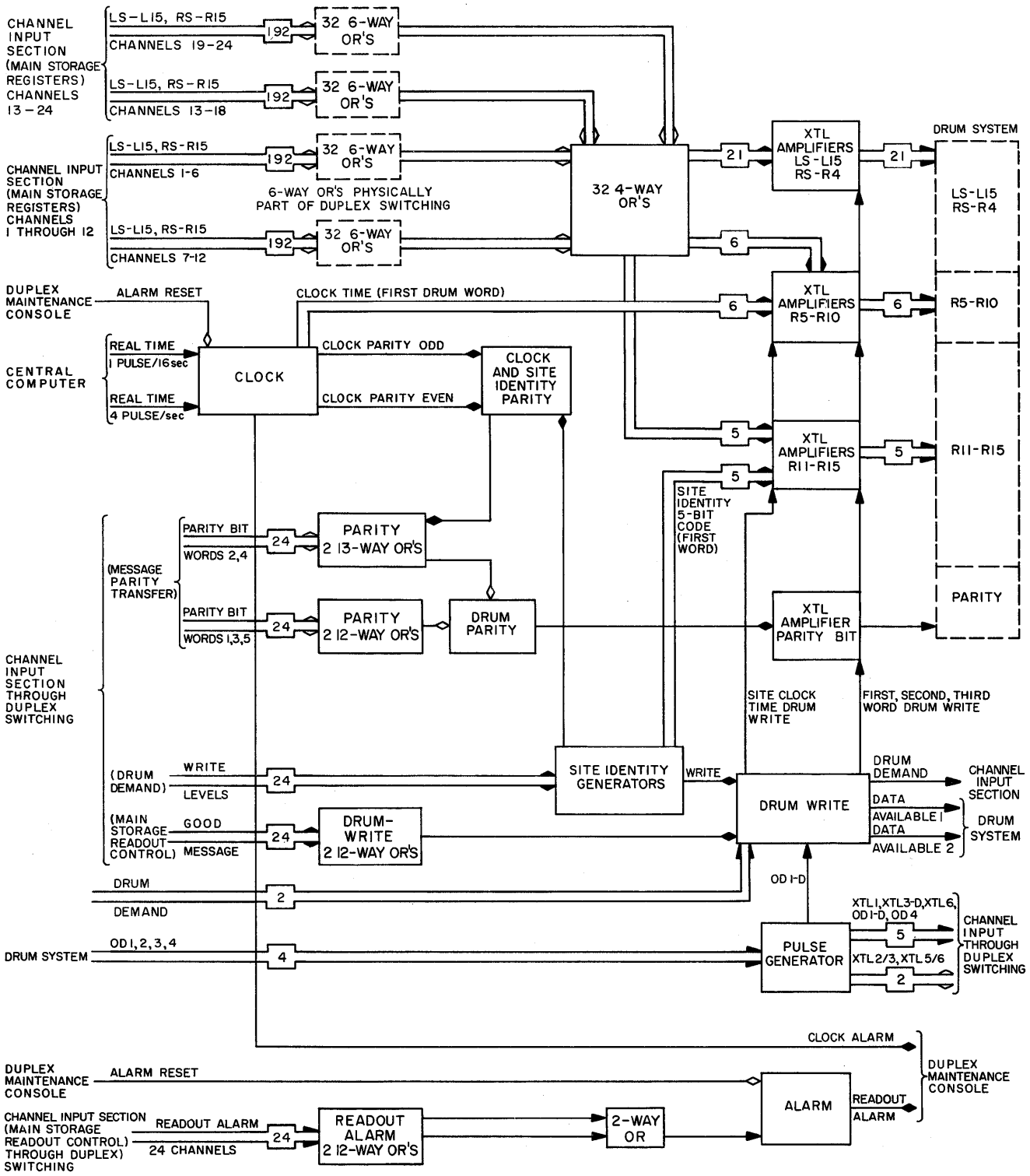


Figure 5–36. Drum Input (Common) Section, Simplified Block Diagram

5.2.2 Addition of Clock Time, Site Identity, and Drum Parity to the Message

The clock time indicates the time a message is received, relative to the real-time clock of the Central Computer.

Clock time is produced by the clock circuit. The circuit receives pulses from the Central Computer System real-time clock at 0.25- and 16-second intervals. These pulses, with the OD 1 and OD 3 pulses from the pulse generator, are used to originate the pulses that step the clock, check the clock operation, and initiate the parity count of the clock time.

The clock circuit indicates clock time by a 6-bit configuration which is fed to the R5 through R10 XTL amplifiers. A clock-parity-odd or clock-parity-even signal is delivered to the clock and site identity parity circuit to aid in drum parity determination. A malfunction of the clock circuit will cause a clock-alarm indication at the duplex maintenance console.

The site identity code identifies the Central that has sent the XTL message. A site identity generator circuit, referred to as a site can because of its physical structure, is assigned to each channel. When a write level from the channel is fed to the site can, it generates a distinctive 5-bit code, which is fed to the R11 through R15 XTL amplifiers. Since each channel is connected to a particular site, the code identifies the site at which the message originated. Parity of the 5 bit site identity code is also determined by a portion of the site identity generator circuit and sent to the clock and site identity parity circuit.

The clock and site identity parity circuit combines the parity count of the site identity with that of clock time to produce a single pulse, labeled site and time parity. This is delivered to the drum parity circuit to assist in establishing the parity of the first drum word (since both clock time and site identity become part of drum word 1).

The drum parity circuit receives a parity indication of each of the five message words in addition to the clock-site parity. Word 1 parity is received at the first readout, words 2 and 3 parities at the second readout, and words 4 and 5 at the third readout. The clock-site parity is combined with message word 1 parity to determine drum word 1 parity. The drum parity circuit operates to produce odd parity for each of the three drum words; that is, an odd number of 1's is contained in each drum word, including the parity bit.

5.2.3 Transfer of Message to Drum System

The drum input section composes the XTL message into three 33-bit words for transfer to the Drum System. The first step in this composition of the message has been accomplished in the channel input section where message data and word parities are transferred in three readouts. Message word 1 is transferred at readout 1; message words 2 and 3 are transferred at readout 2; and message words 4 and 5 are transferred at readout 3. The five message words are thus roughly re-formed into three words. The site-identity and clock-time bits are added to the first word, and a parity bit is added to each of the three words, to form the three 33-bit drum words. Briefly, the composition and transfer of the drum word are achieved as follows.

During the readout process, a good-message level is fed (from the main storage readout channel circuit of the channel reading out) through OR circuits to the drum write circuit. The good-message level permits the drum write circuit to pass three OD 1 + 1 pulses as drum-write pulses. These pulses are in synchronism with the three readout levels which last from OD 4 to the succeeding OD 4. The three drum-write pulses are applied to the XTL amplifiers. The first of the three is separately applied, as a site-and-clock-time-drum-write pulse, to the R5 through R15 XTL amplifiers.

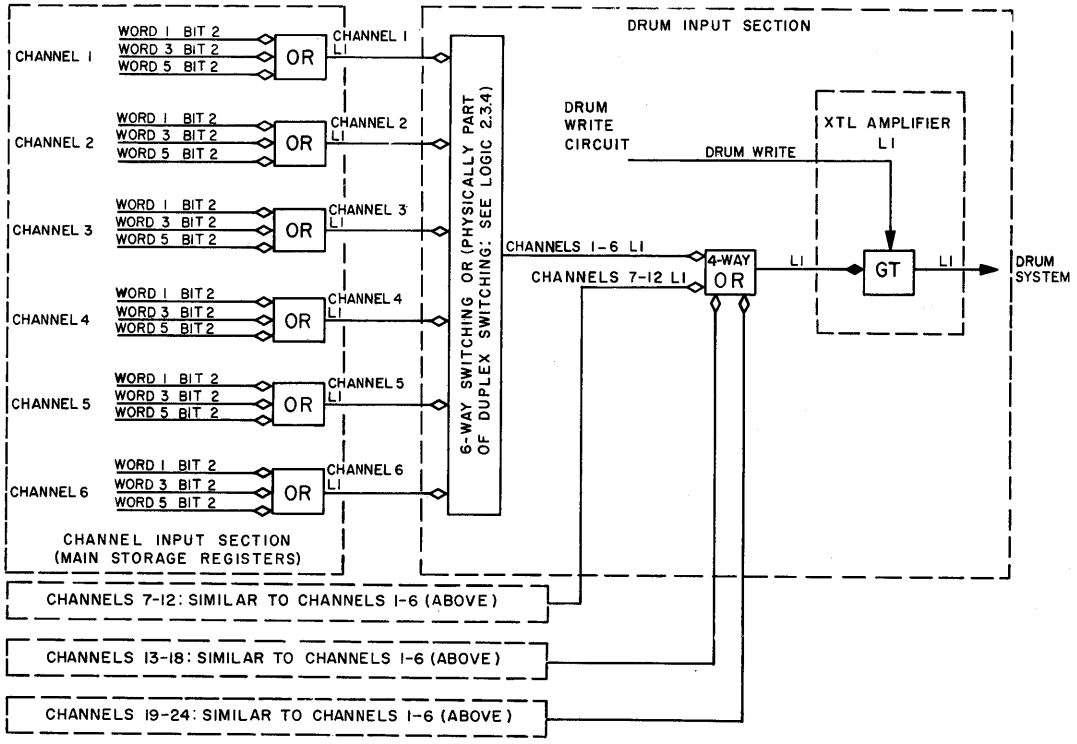
The XTL amplifiers transfer the three drum words to the Drum System. During readout 1, the first message word is applied to XTL amplifiers LS through L15. Concurrently, the clock-time bits, generated in the clock-time circuit, are fed to XTL amplifiers R5 through R10; the site identity bits, generated by the site identity generator, are applied to XTL amplifiers R11 through R15; and the first drum word parity bit is fed to the XTL parity amplifier. Whenever a 1 has been applied to an XTL amplifier, the first drum-write pulse (OD 1 +1) is gated through that amplifier to form a corresponding bit of the first drum word. Bit positions RS through R4 are blank in drum word 1. Message words 2 and 3 are applied during readout 2 to XTL amplifiers LS through L15 and RS through R15. Concurrently, the second drum word parity bit is applied to the parity bit XTL amplifier. Each XTL amplifier to which a 1 is applied gates through the second drum-write pulse to form a corresponding bit of drum word 2. Drum word 3 is formed, similarly to drum word 2, by message words 4 and 5, the third drum word parity bit, and the third drum-write pulse.

5.2.4 Generation of XTL Timing Pulses and Levels

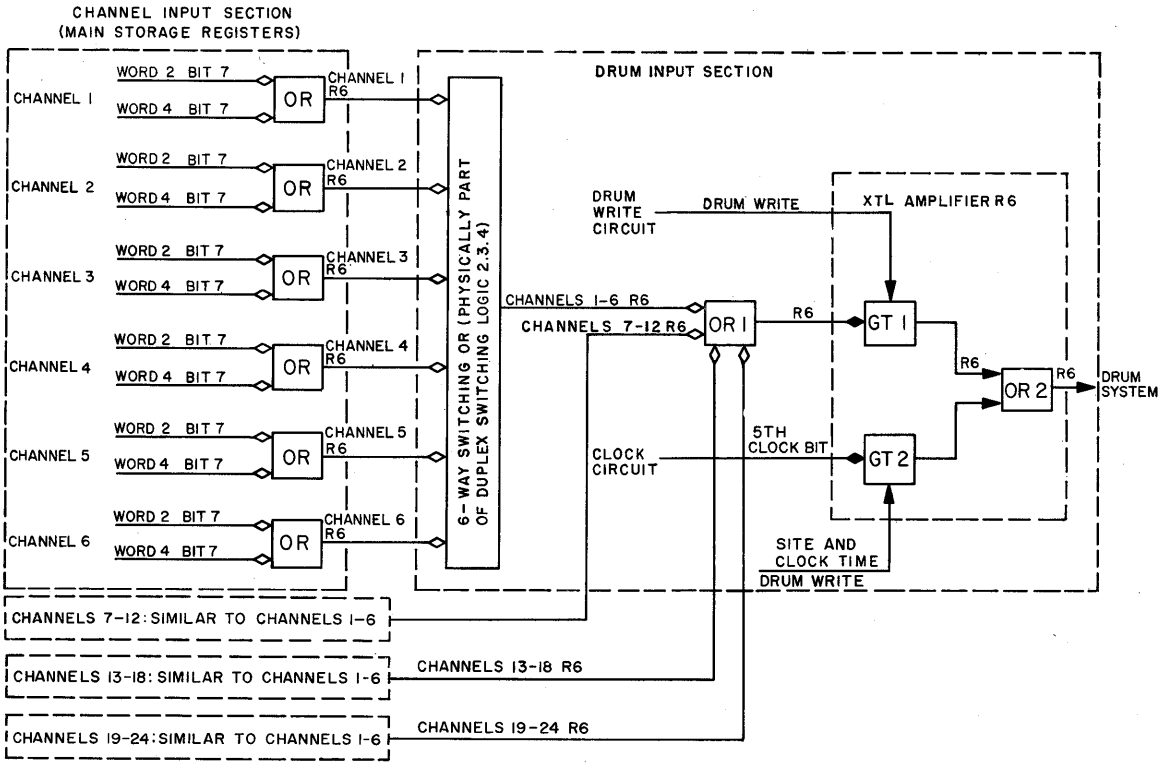
The pulse generator circuit receives OD 1, 2, 3, and 4 pulses and generates from them the XTL timing pulses and levels which other circuits require. These are OD 1 + 1, XTL 1, XTL 3 + 1, and XTL 6 pulses, and XTL 2/3 and XTL 5/6 levels. The pulse generator also passes OD 4 pulses to the channel input section.

5.2.5 Alarm Indications

Readout alarm indications are passed through the readout alarm OR's to the alarm circuit, which sends



A. CONSOLIDATION OF LI BIT LINES



B. CONSOLIDATION OF R6 BIT LINES

Figure 5–37. Consolidation of Message Bit Lines

an alarm signal to the duplex maintenance console (READOUT ALARM (XTL-DUPLEX EQUIPMENT) module D, lower section). The alarm, indicating malfunction of the clock circuit, is generated in the clock circuit and sent to the duplex maintenance console (CLOCK ALARM (XTL DUPLEX EQUIPMENT) module D, lower section). The CLEAR ALARMS switch on the duplex maintenance console (module D, lower section) resets the alarms.

5.2.6 Generation of Data-Available Pulse

The data-available pulse is generated to inform the Drum System that a good message is stored in the channel equipment and is about to be transferred to the drum. Since two drum fields (drum fields 1 and 2) are employed, it is necessary to distinguish to which drum field the message is being sent. The data-available pulse is sent to the drum field which originated the DD pulse. However, if both drum fields each originated a concurrent DD pulse, the data-available pulse is sent to drum field 1 only.

5.3 MESSAGE BIT OR CIRCUITS

The consolidation of the message bit lines, discussed briefly in 5.2.1, is illustrated for two typical bit lines, L1 and R6, in figure 5–37. As described in Chapter 3, like message-bit lines of the words 1, 3, and 5 main storage registers and of the words 2 and 4 main storage registers are consolidated into a total of 32 message-bit lines for each channel, LS through L15 and RS through R15. Each of the 32 like-bit lines from the 24 channels is further consolidated by four 6-way switching OR circuits, which are physically part of duplex switching. The detailed circuitry for these 6-way switching OR circuits is found in logic drawing 2.3.4. Each 6-way switching OR serves six channels, grouped as channels 1 through 6, 7 through 12, 13 through 18, and 19 through 24. The output of each 6-way OR circuit is led to a 4-way OR circuit and the output of each 4-way OR is applied to an XTL amplifier circuit designated by the drum word position to which it corresponds; thus, XTL amplifier L1, XTL amplifier R6, etc. The R5 through R10 XTL amplifiers also receive the outputs of the clock circuit, and R11 through R15 XTL amplifiers receive the outputs of the site identity generators.

5.4 CLOCK CIRCUIT

5.4.1 General

The clock circuit inserts the relative time of reception of an XTL message as the message is read out to the drum, so that the Central Computer may compute the time between message reception and message processing by the Central Computer. The relative time is inserted into the message as part of drum word 1.

The relative time at which the message is received is indicated by six binary bits. Each binary number represents a quarter-second in time; the time cycle is 64 quarter-seconds (16 seconds). The six binary bits are generated by the clock circuit, indicating the number of quarter-seconds that have passed since the start of the cycle. The clock resets itself to 0 every 16 seconds, and counting is continuous.

The clock circuit (fig. 5–38) is basically a 6-stage binary counter that provides a continuous indication of the total number of quarter-seconds that have elapsed since reset. The counter is stepped every quarter-second by a standard pulse from the Central Computer. The clock circuit also contains a parity generator which indicates the parity of the clock output at any time. A clock test circuit is included which tests the clock every 16 seconds and generates a clock alarm in the event of an incorrect reading. The logic discussion of the clock circuit is divided into four parts:

a. Clock stepping and synchronizing
b. Clock indication (6-stage binary counter)
c. Clock parity generator
d. Clock test

5.4.2 Clock Stepping and Synchronizing

The stepping and synchronizing section of the clock circuit consists of FF's 8, 9, and 10 and GT's 8, 9, and 10. Standard pulses from the Central Computer occurring at a rate of four per second (quarter-second pulses) set FF 9. The set output of FF 9 conditions GT 9, permitting an OD 3 pulse to pass. The OD 3 pulse sets FF 10, conditioning GT 10. An OD 1 + 1 pulse, passed by GT 10, clears FF's 9 and 10 and is used to step the clock. A single OD 1 + 1 pulse is passed for each quarter-second pulse applied to the circuit. Since the quarter-second pulses and the OD pulses are not synchronized, the time delay between then varies from a minimum of 6 μsec (OD 3 to OD 1 + 1) to a maximum of 16 μsec (OD 3 and quarter-second pulses occurring simultaneously). The clock is synchronized with the Central Computer clock by a synchronizing pulse which occurs every 16 seconds. This pulse sets FF 8. Flip-flop 8 conditions GT 8, which passes the following quarter-second pulse and clears the 6-stage binary counter. The next synchronizing 16-second standard pulse occurs, after 63 quarter-second pulses have been received, coincidently with the 64th quarter-second pulse. If the counter has operated correctly, the flip-flops will be cleared by the 64th quarter-second pulse, and the 16-second standard pulses serve only to check clock synchronization. If one or more of the flip-flops is set, an alarm is generated. The timing chart (fig. 5–39) shows the timing relationship in the clock-stepping and synchronizing section of the clock

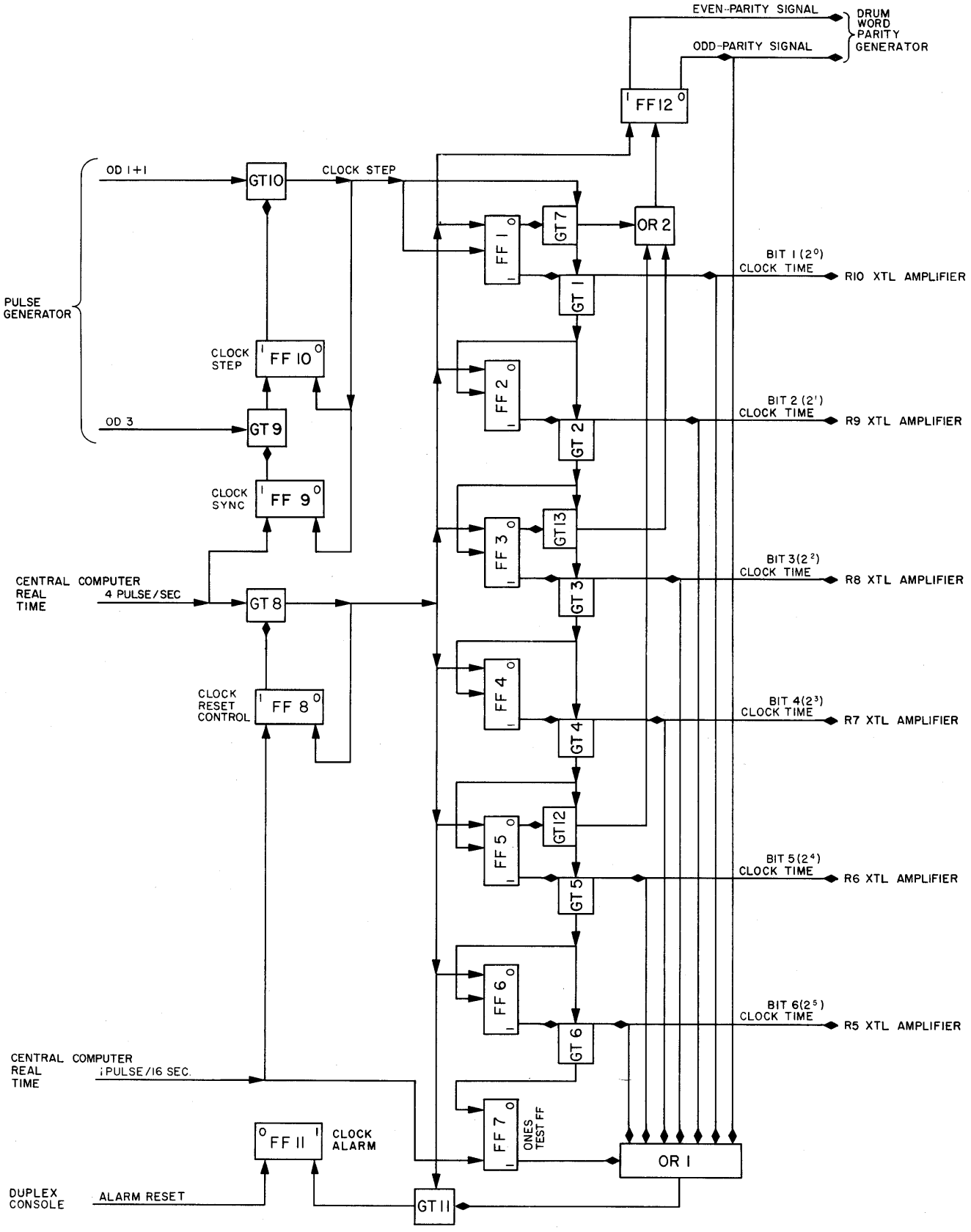


Figure 5–38. Clock Circuit, Simplified Logic Diagram

circuit. Because of the time delay of the stepping circuit, the reset pulse occurs between the 64th and 1st stepping pulse.

5.4.3 Clock Indication (6-Stage Binary Counter)

The six clock time bits are generated by a 6-stage binary counter (FF's 1 through 6 and GT's 1 through 6). The set output of each flip-flop is a single binary clock bit with the FF numbers corresponding to the clock bit numbers. The binary counter indicates the number of clock quarter-second stepping pulses that have occurred (since last sync) in binary notation. The timing chart (fig. 5–40) shows the output of the six flip-flops for any number of clock steps. The clock bit output is considered to be 1's when the flip-flops are set and 0 when the flip-flops are cleared. The six clock bits are sent to the R5 through R10 XTL amplifiers.

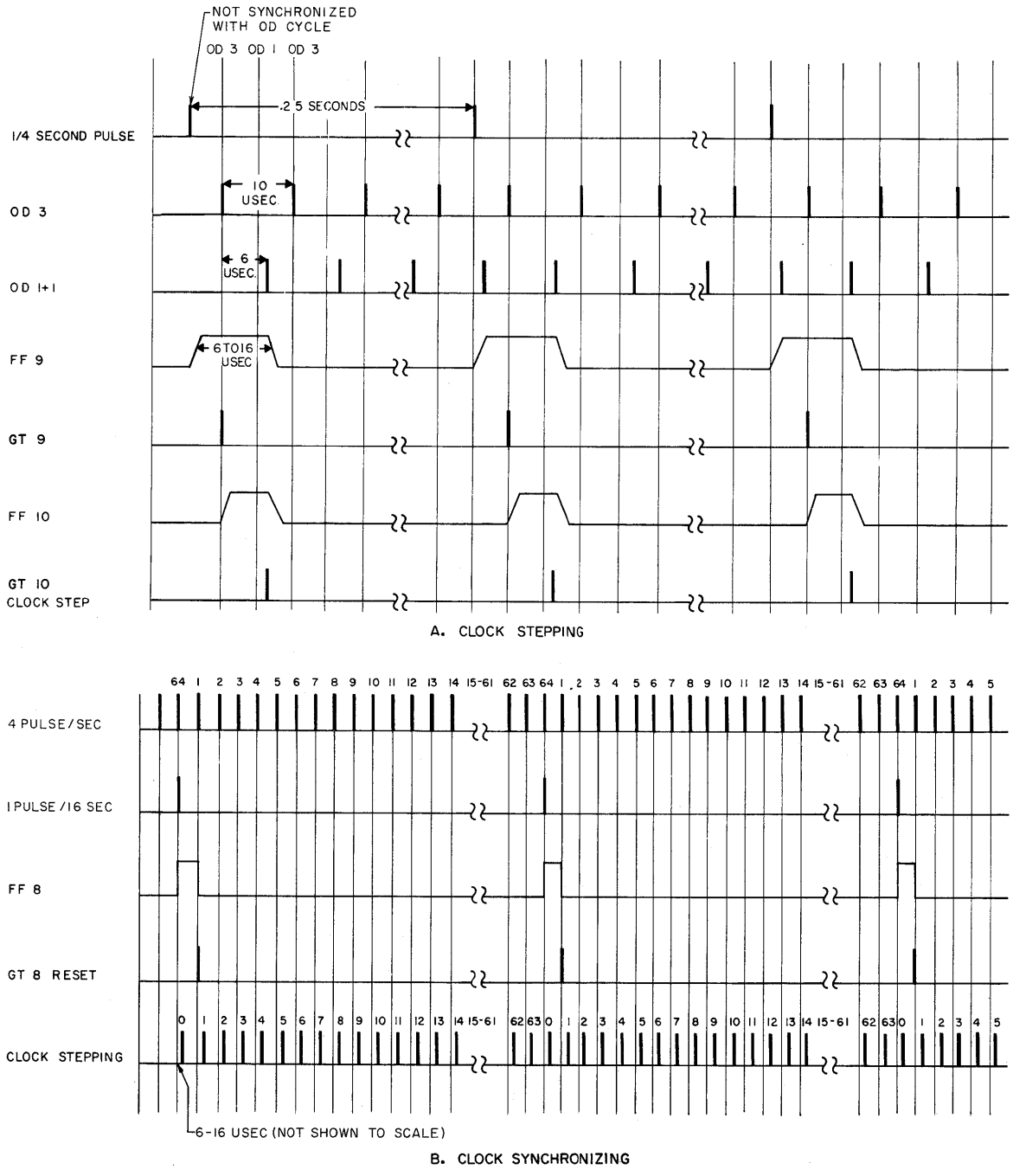


Figure 5–39. Clock Stepping and Synchronizing, Timing Chart

5.4.4 Clock Parity Generator

The parity (odd or even numbers of 1 bits) in the clock output at any time must be determined to permit the drum parity circuit to generate the correct parity for the first drum word (which includes the clock time). The parity of the clock output for each quarter-second is indicated on the timing chart (fig. 5–40).

The parity generator consists of FF 12, OR 2, and GT's 7, 13, and 12, as shown in figure 5–38. When the clock circuit is operating properly, an even number of 1's in the 6-binary-number clock count causes FF 12 to be set, and an odd number of 1's causes FF 12 to be cleared. The set condition of FF 12 sends an even-parity signal to the clock and site identity parity circuit. The clear condition of FF 12 sends an odd-parity signal to that circuit. The operation of this portion of the clock circuit follows.

The first 4-pps pulse following the 1-pulse-per-16-second pulse sets FF 12 and clears the 6-FF counter. Every time the clock-stepping pulse finds FF 1, FF 3, or FF 5 clear, this pulse will be applied through OR 2 to the complement input of FF 12. Analysis of counter

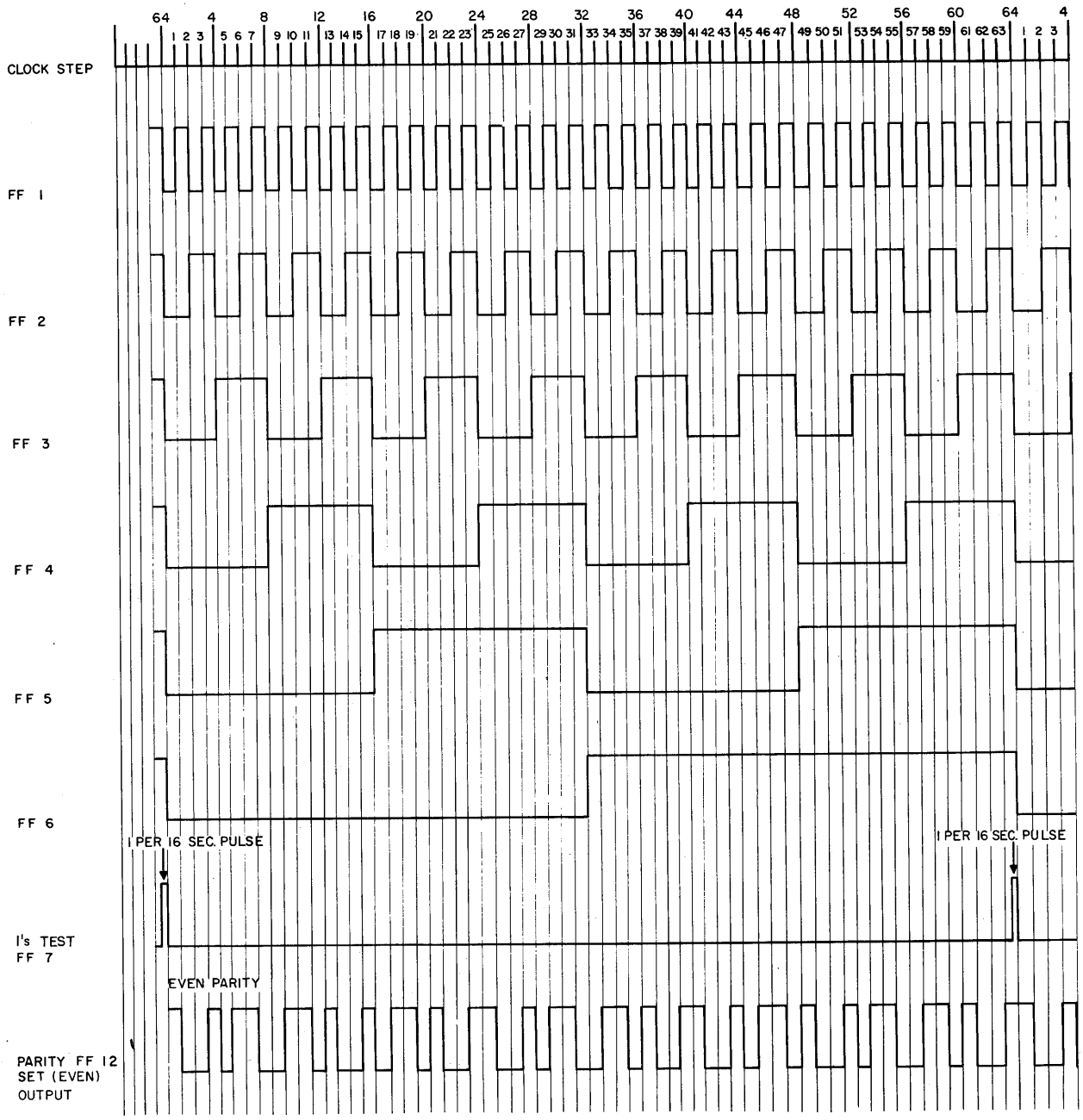


Figure 5–40. Clock Binary Counter, 1's Test and Parity Generator, Timing Chart

operation, with the assistance of figure 5–40, shows that every time the counter is stepped to a number with an odd-parity count the complement input to FF 12 sets FF 12. For example, the first clock-stepping pulse sets FF 1, placing 000001 in the counter. Parity is therefore odd. Because of the time lag in the setting of FF 1, GT 7 remains conditioned long enough to pass the first clock-stepping pulse. This pulse, applied through OR 2 to the complement input of FF 12, clears FF 12, causing an odd-parity signal, which is the desired indication. The second clock-stepping pulse clears FF 1 and sets FF 2, installing the number 000010 in the counter. Parity remains odd. Because of time lag again, GT 7 is not conditioned at this instant and does not pass the second clock-stepping pulse to OR 2. There is no complement input to FF 12, which accordingly remains clear. The third clock-stepping pulse installs 000011 in the counter. Parity is even. Finding FF 1 clear, the third clock-stepping pulse is passed by GT 7 to OR 2. Flip-flop 12 is accordingly complement-set, producing an even-parity signal; which is the desired indication. A similar analysis may be extended to the 64th clock-stepping pulse.

5.4.5 Clock Test

The clock is tested every 16 seconds to determine whether a correct and complete count has been made. After 63 quarter-seconds have elapsed, the six clock bits should all indicate 1's (FF's 1 through 6 set). If this condition is present, GT's 1 through 6 are all conditioned. The 16-second pulse, which occurs simultaneously with the 64th quarter-second pulse, then sets FF's 7 and 8. The 64th stepping pulse occurs at least 6.5 μsec after the 64th quarter-second pulse and passes through GT's 1 through 6, clearing FF 7. Concurrently, clock bits 1 through 6 are all changed to 0. Flip-flop 7 is called the 1's test flip-flop because it is cleared only if all clock bits 1 through 6 were 1's after the 63 count.

After the 64th stepping pulse has appeared, FF's 1 through 7 should be cleared and parity FF 12 set (even parity for 000000). This 0's condition is tested by applying the set (1) outputs of FF's 1 through 7 and the cleared (odd) output of FF 12 to OR 1. If any of these inputs to OR 1 contains a 1, the output of OR 1 will condition GT 11. Flip-flop 8, which was set by the 16-second pulse, conditions GT 8, which permits the first quarter-second pulse to strobe GT 11. When GT 11 is conditioned by a set output from FF's 1 through 7 or by an odd (cleared) output from FF 12, the first quarter-second pulse passes through GT 11 and sets clock alarm FF 11, which lights an alarm neon on the duplex maintenance console. The first quarter-second pulse also acts as a reset signal for the clock and is applied to the set side of FF 12. The clock is then stepped by the first clock-set pulse occurring at least 6.5 μsec after the first (reset) quarter-second pulse. When ever the clock correctly counts 64 pulses, the reset pulse occurring between the 64th and 1st stepping pulse has no effect.

5.5 SITE IDENTITY GENERATOR

In order to shorten message length and conserve transmission time, identification of the transmitting site is not included, as such, in the message. However, each Central transmits XTL messages to the receiving Central over a separate telephone line terminating in a specific channel. The site identity generator circuit generates a 5-bit code, the configuration of which is unique to the channel processing the message; i.e., it indicates the originating site of the message. This 5-bit code is added to the first word of the message operation in the following manner.

The write level (OD 3 to OD 1 + 1) from the drum demand circuit of each channel is sent, through duplex switching, to a separate site identity can. Each site identity can is wired so that the application of the write signal produces a binary address plus a site parity output on the six output lines. Figure 5–41 shows two site cans, one for channel 1 and one for channel 2. The binary address number is assumed to be 10101 for channel 1, 11101 for channel 2. The site identity can for channel 1 is wired so that the write signal from channel 1 produces 1's (+10V) on site bit lines 1, 3, and 5. Site bit lines 2 and 4 are connected to −30V, indicating 0's on these lines. Since the site number for channel 1 has an odd parity (odd number of 1's in 10101), the even parity line is connected to the −30V line (0). The channel 2 site is wired so that the channel 2 write signal produces 1's on site bit lines 1, 3, 4, and 5. The −30V supply places a 0 on site bit line 2. The parity of the channel 2 site number is even (11101). Therefore, the write signal also produces a 1 on the even-parity line. The site cans also pass the channel-write signal of their respective channels to the drum write circuit.

Since only one channel can produce a write level at any one time, the similar site bits of all channels and the write level are collected by 22-way OR circuits and sent to XTL amplifiers R11 through R15 where each 1 bit is converted into a standard pulse for transfer to the Drum System. The even-parity level (+10V) for even-parity count or the odd-parity level (−30V) for odd-parity count is sent to the clock and site identity parity circuit where the total parity of the clock and site identity is determined. When the spare channel, channel 6, is substituted for another channel, the write level generated in the channel 6 channel input section is applied to the site can for the replaced channel. Thus, if the spare channel replaced channel 1, the write level from the spare channel is applied to the channel 1 site

can. The philosophy and circuitry related to write level switching were described in Chapter 3.

5.6 CLOCK AND SITE IDENTITY PARITY

The clock and site identity parity circuit (fig. 5–42) indicates the combined parity of site identity and clock time to the drum parity circuit. The drum parity circuit generates the correct parity bit for each drum word as it is transferred to the Drum System. Since part of drum word 1 is made up of the clock time and site identity bits, the parity time and site identity must be known to generate the proper parity for the first drum word.

The constantly changing clock parity is indicated at any time by the outputs of the parity flip-flop in the clock circuit. The two outputs are clock-parity-even and clock-parity-odd, depending upon the number of 1's in the clock output at any instant. The parity of the site identity is indicated by a site-parity-even output from each side identity can. The site-parity-even output is produced by the application of the write signal to the site identity can which is so wired that the write signal (a 1 level of 6-μsec duration) appears on the site-parity-even output. When the number of 1 data bits in the site identity is odd, the site-parity-even output is a constant —30V (0).

The output of the clock and site identity circuit is

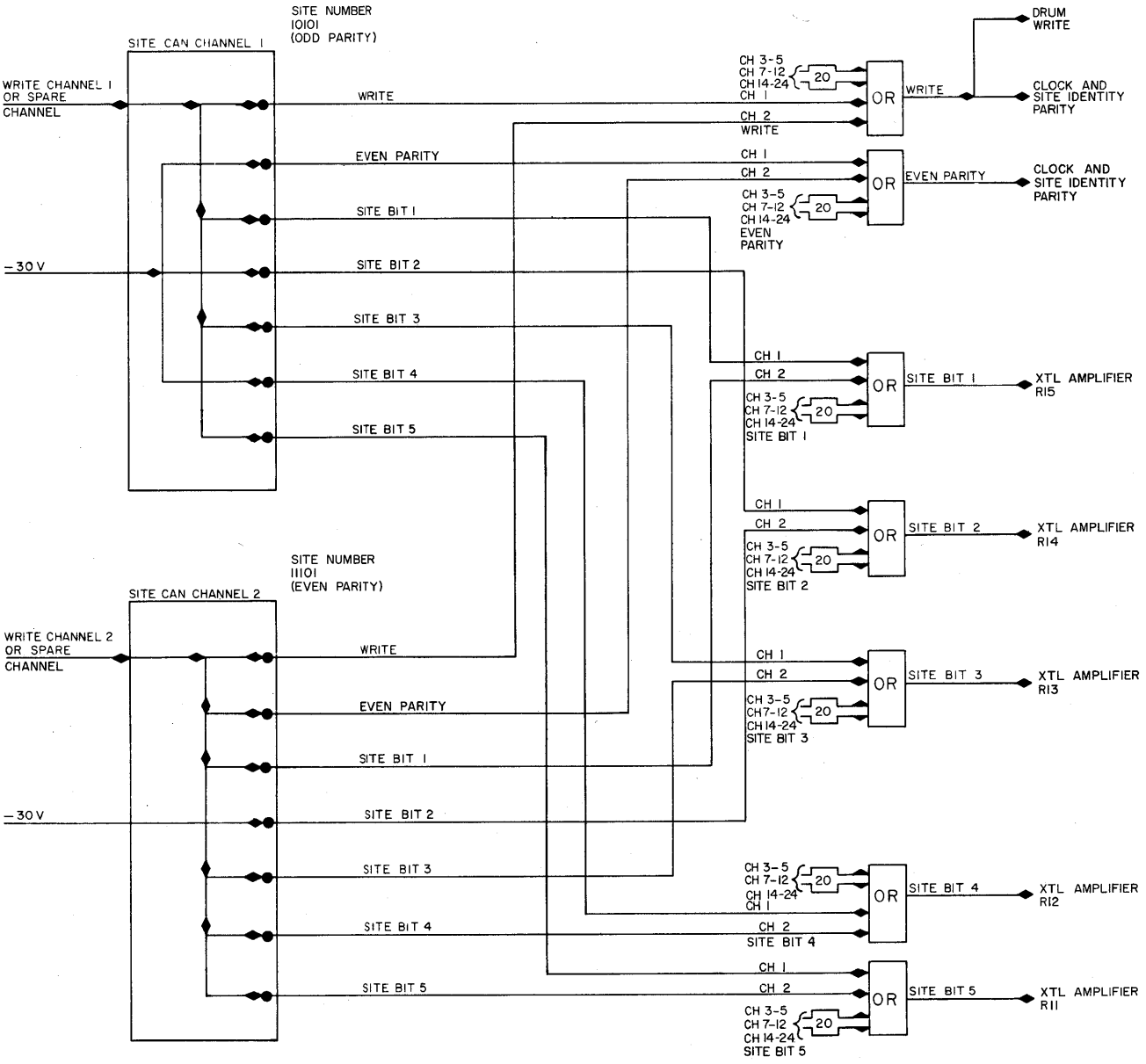


Figure 5–41. Site Identity Generator, Simplified Logic Diagram

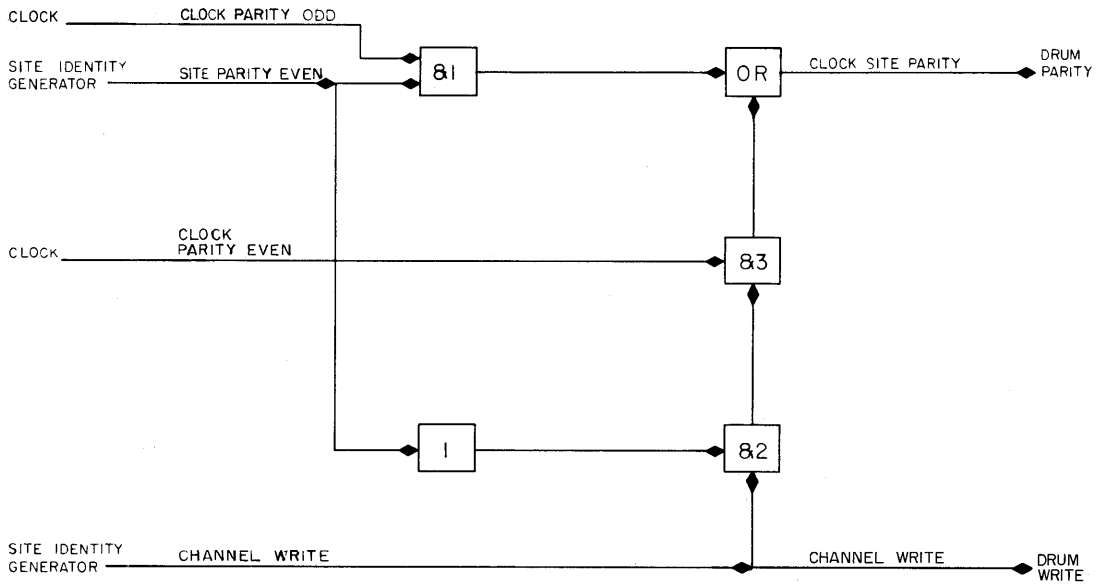


Figure 5–42. Clock and Site Identity Parity Circuit, Simplified Logic Diagram

a 0 whenever the total parity of clock and site identity is even and a 1 when the total is odd. The four possible combinations of parity and the resulting outputs are listed in table 5–4.

TABLE 5–4. PARITY COMBINATIONS AND OUTPUTS

CLOCK	SITE IDENTITY	TOTAL	OUTPUT TO DRUM
Odd	Even	Odd	1
Odd	Odd	Even	0
Even	Even	Even	0
Even	Odd	Odd	1

For the first case (clock odd, site identity even), the clock parity-odd input and the site parity-even input are applied to AND 1 which then passes a 1 output (+10V) to the drum parity circuit through the OR circuit. In the second case (clock parity odd, site identity odd), AND 1 has a 0 output (−30V) because the site-parity-even input is down (0). This site-identity-odd input is also passed through an inverter (1) which applies a 1 (+10V) to AND 2. When the write signal occurs, indicating readout of the first word data, it is applied to AND 2, which produces a 1 input to AND 3. AND 3, however, has a 0 output, since its second input, clock-parity-even, is down (0). Since neither input to the OR circuit is a 1, the output to the drum parity circuit is a 0.

In the third case (clock and site even), neither AND 1 nor AND 2 has a 1 output. In the fourth case (clock even, site odd), the 0 on the site-parity-even line is changed to a 1 by the inverter and applied to AND 2. The write signal then causes AND 2 to pass a 1 to AND 3 which also receives the clock-parity-even signal. The 1 output of AND 3 is sent through the OR circuit to the drum parity circuit. The clock and site identity circuit relays the channel-write signal to the drum write circuit.

5.7 DRUM PARITY

The drum parity circuit (fig. 5–43) determines the overall parity bit for each of the three drum words and applies the resulting parity bits to the parity XTL amplifier for transfer to the Drum System.

Basically, the circuit has two inputs, the parity indications of the right half and left half of each drum word. The total number of 1's in each drum word (32 bits plus parity bit) should be odd. Therefore, whenever the total parity count of the left and right halves of a drum word is even, a 1 is inserted into the drum parity bit position, making the overall parity (including the drum parity bit) odd. If an odd number of 1's is already contained in the drum word, the resulting drum parity bit is a 0.

Each of the five words of an XTL message contains a parity bit (bit 17) which is a 1 if the number of 1's in the 16 message (data) bits of the word is odd and a 0 if the number of 1's is even. These parity bits for the five words are sent to the drum parity circuit by the mes-

sage word parity transfer circuit on two separate lines. One line sends the parity bits of the first, third, and fifth message words; the other transmits the second and fourth message word parity bits. The two lines are designated 1-3-5 line parity and 2-4 line parity. The parity bit of a particular word appears on the proper line when that word is transferred to the common equipment by a readout signal. The parity bit of word 1 is transferred by the first readout signal. The second readout signal transfers the second and third word parity bits. The third readout signal transfers the fourth and fifth word parity bits. Since the right half of drum word 1 is made up of the clock time and site identity data, the drum parity circuit receives an indication of the combined parity of clock and site identity from the clock and site identity parity circuit. This clock and site identity appears during the first readout signal (coincidently with the write level) and is a 0 for an even number of 1 bits and a 1 for an odd number of 1's in the clock time and site identity data.

Four conditions are possible for any one drum word. These conditions, the parity of the complete drum word, and the resulting drum parity bit are summarized in table 5—5.

The circuitry for the generation of the drum parity bit for channels 1 through 12 is shown in detail in figure 5—43. Similar circuitry exists for channels 13 through 24. The output lines of the two similar circuits are consolidated by OR 5 and fed to the parity XTL amplifier. In the following discussion, the operation of the circuit is described with reference to channels 1 through 12 but applies equally to channels 13 through 24.

In the case in which the right and left half of a drum word is odd, OR 1 will receive a 1 from the clock and site identity parity circuit or from the 2-4 line parity, depending upon which word is being formed. The 1 output of OR 1 is then transferred to AND 1. AND 1 also receives the 1 parity bit appearing on the 1-3-5 line through OR 2. The output of AND 1 is changed to a standard level output by the LA and is passed through OR 4 and OR 5 to the parity bit XTL amplifier where it is transferred to the Drum System as the drum parity bit. The LA is necessary to change the nonstandard message word parity bits (which are outputs of CS's) to standard levels.

The other condition that produces a 1-drum-parity bit exists when the right half and the left half of drum parities are both even. In this case, the clock and site

TABLE 5—5. DETERMINATION OF DRUM PARITY BIT

RIGHT HALF OF DRUM WORD	LEFT HALF OF DRUM WORD	COMBINED RIGHT AND LEFT HALVES	DRUM PARITY BIT
Odd	Odd	Even	1
Odd	Even	Odd	0
Even	Odd	Odd	0
Even	Even	Even	1

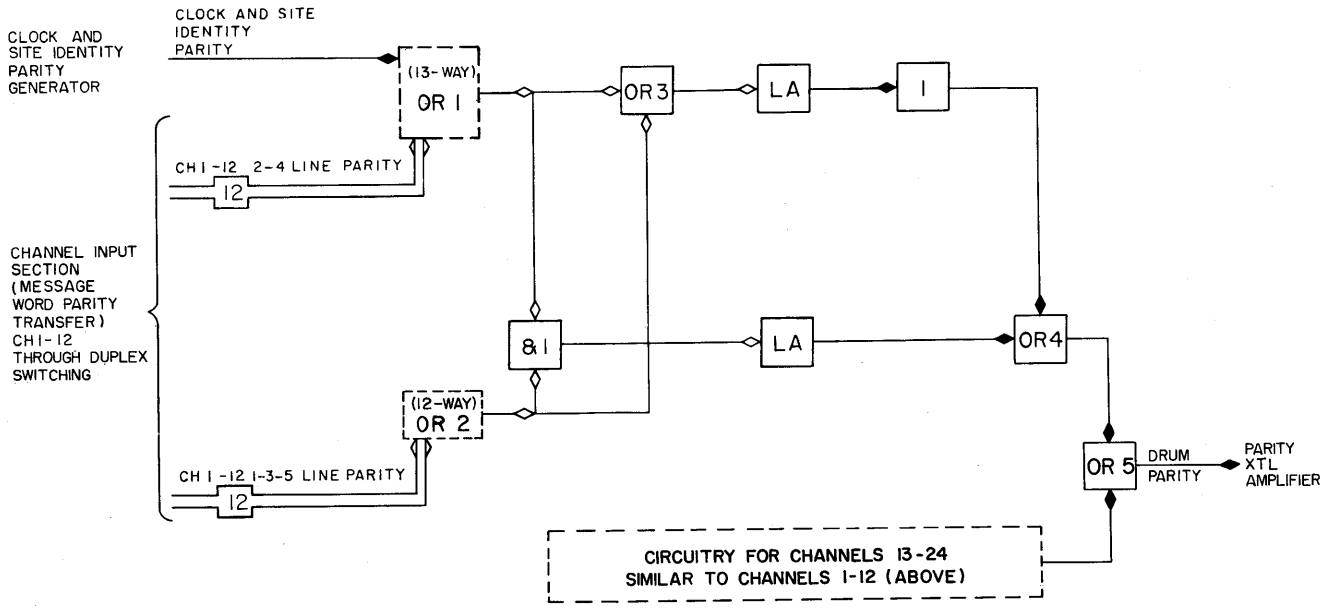


Figure 5—43. Drum Parity Circuit, Simplified Logic Diagram

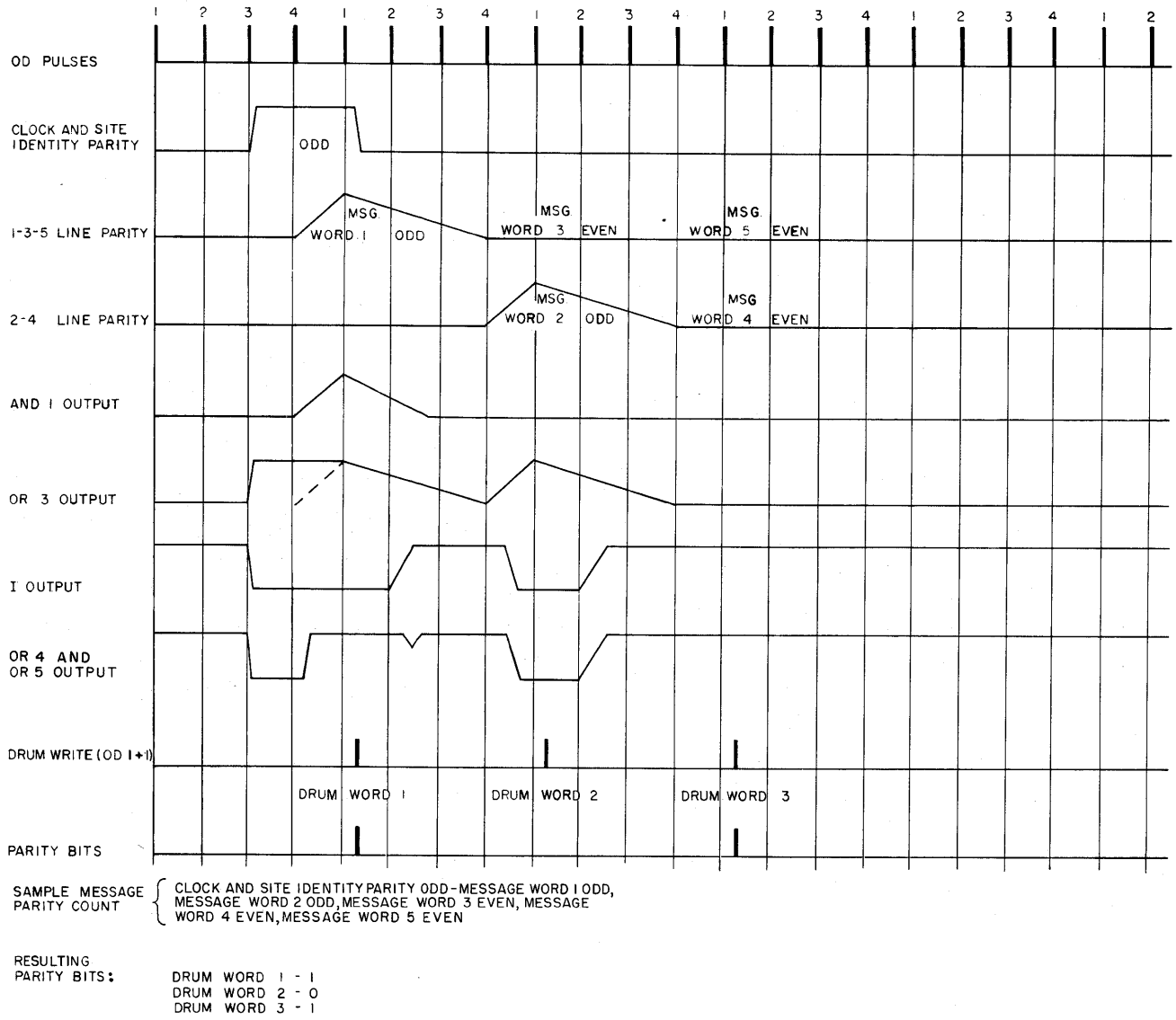


Figure 5—44. Drum Parity, Timing Chart

identity parity or the 2-4 line output, and the 1-3-5 line output will all be 0. The clock and site identity 0 and the 2-4 line 0 are passed through OR 1 to OR 3. The 1-3-5 line input to OR 2 is also a 0, producing a 0 output from OR 2 to OR 3. An OR circuit has a 0 output only when all inputs are 0 but has a 1 output if any input is a 1. The 0 output is changed to a standard level (—30V) by the LA and is then changed to a 1 by the inverter. This 1 output is passed through OR 4 and OR 5 as the drum parity bit.

For the other two conditions (right odd, left even, and left odd, right even), AND 1 does not have two 1 inputs, nor does OR 3 have two 0 inputs; the input drum parity bit is therefore a 0 for these cases.

The drum parity circuit receives the 2-4 line parity and the 1-3-5 line parity from all 24 channel inputs to the common equipment. The 24 2-4 lines are collected together by OR circuits into a single 2-4 output; the 24 1-3-5 lines are also combined. Since only one channel can transfer data to the common equipment at any one time, the outputs of the combined 2-4 and 1-3-5 lines are the parity bits of the message being transferred.

The timing chart (fig. 5—44) shows the timing relationships in the drum parity circuit during the transfer of a sample message. The clock and site identity parity is assumed to be odd, producing a 1 output on the clock and site identity line. Parity of the first message word is assumed to be odd, thereby presenting a 1 parity bit on the 1-3-5 line. Parity of the second message word was also assumed to be odd, thereby presenting a 1 parity bit on the 2-4 line. Parity of the third through fifth message word is assumed to be even, producing 0's

on their respective parity lines. The correct drum parity bits for this sample message are: first drum word, a 1 parity bit; second drum word, a 0 parity bit; and third drum word, a 1 parity bit.

5.8 DRUM WRITE

The drum write circuit furnishes drum-write pulses to the XTL amplifiers and data-available pulses to the Drum System. The circuit also relays DD pulses to the channel input section.

The drum write circuit (fig. 5–45) receives the channel-write level (OD 3 to OD 1 + 1), and a good-message level from the channel input section, when a channel is being read out. (The write level passes through the site identity generator.) The drum write circuit produces three drum-write pulses (OD 1 + 1) in synchronism with the three readouts of the XTL message, designated drum write 1, 2, and 3. These pulses are applied to the XTL amplifiers. In addition, a separate pulse, produced coincidentally with drum write 1 and designated site and clock-time drum write, is applied to the R5 through R15 XTL amplifiers. Drum demand pulses are received from either drum field 1 or drum field 2 of the Drum System, indicating which field is prepared to accept a message. Consequently, the data-available pulse (which informs the drum field that a message transfer is imminent) is directed to the drum field which originated the DD pulse. (If simultaneous DD pulses are received for each drum field, the circuit selects drum field 1 as the field to which the data-available pulse will be sent.)

Circuit operation follows (fig. 5–46). Gate 1 is continuously strobed by OD 1 + 1 pulses. When a channel is being read out, the good-message level from that channel conditions GT 1. The good-message level is up during the entire readout period. Accordingly, GT 1 passes three OD 1 + 1 pulses in synchronism with the three readout signals. The three OD 1 + 1 pulses are applied to all of the XTL amplifiers. They are also applied to GT 2. This gate is conditioned by the write level: OD 3 to OD 1 + 1 during the first readout. Accordingly, GT 2 passes only the first drum-write pulse which is applied as a site-and-clock-time-drum-write pulse to XTL amplifiers R5 through R15. The drum-write 1, 2, and 3 pulses are applied to GT's 4 and 5 for the generation of data-available pulses discussed below.

If a drum-demand-1 pulse is received from drum field 1, FF 1 is set, causing conditioned GT 3 to pass an OD 4 pulse, setting FF 2 and clearing FF 1. The set

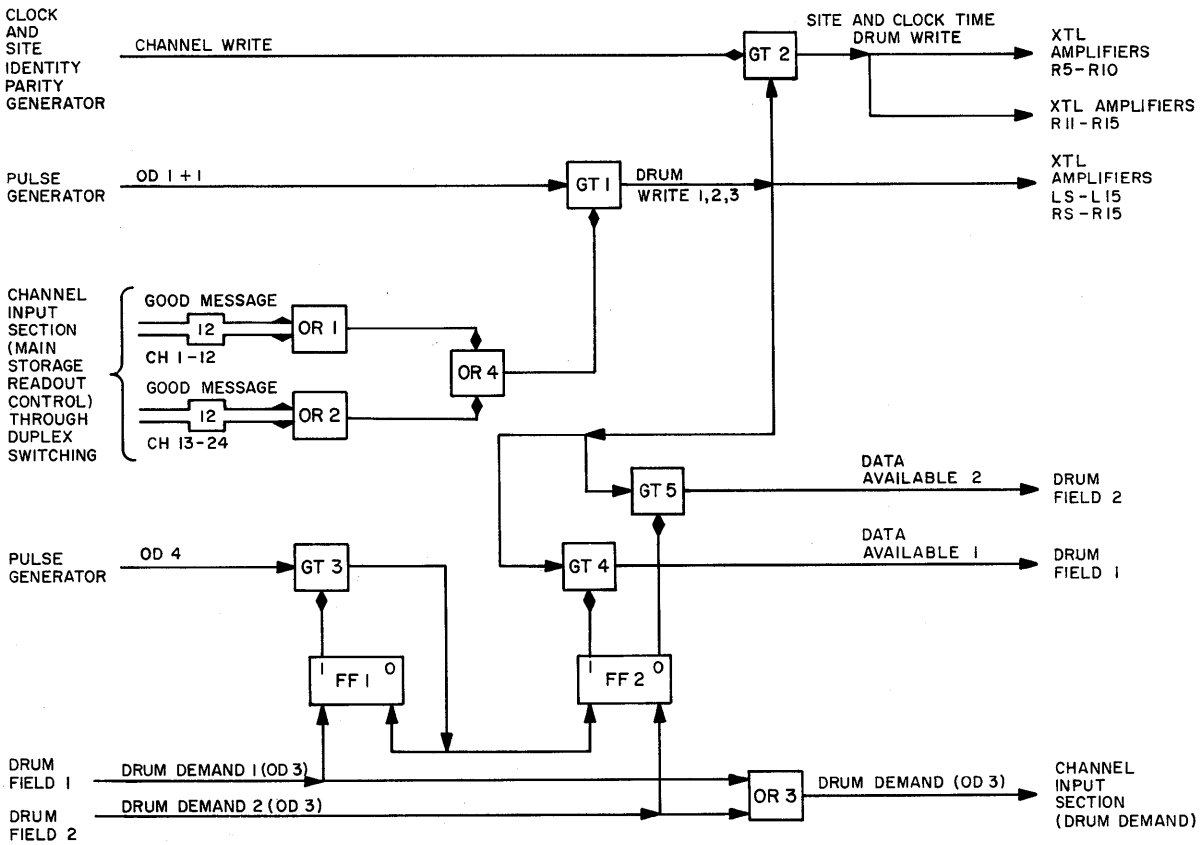


Figure 5–45. Drum Write Circuit, Simplified Logic Diagram

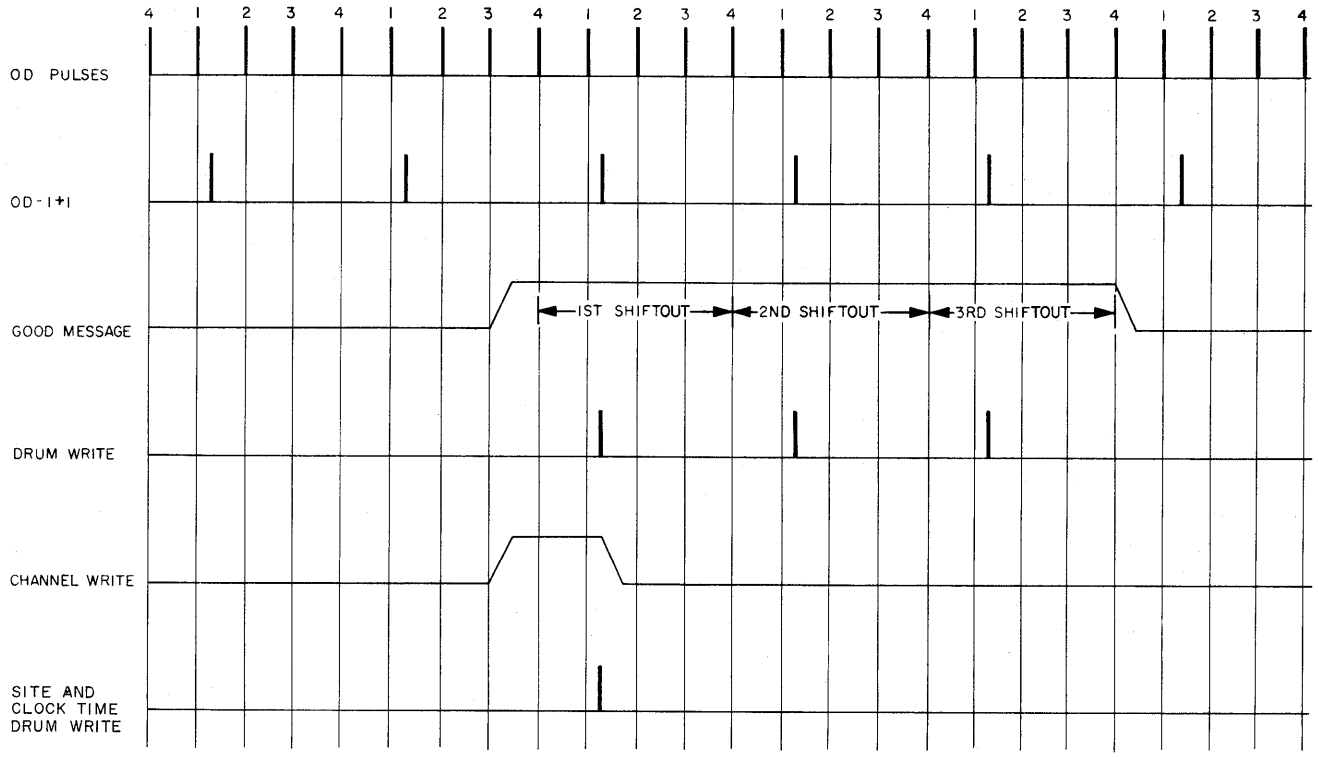


Figure 5–46. Drum Write Circuit, Timing Chart

output of FF 2 conditions GT 4 which passes the three successive drum-write pulses (as data-available-1 pulses) to drum field 1. If a DD-2 pulse is received (from drum field 2), FF 2 is cleared (or remains) clear and GT 5 passes the drum-write pulses (as data-available-2 pulses) to drum field 2. If a drum-demand-1 and drum-demand-2 pulse are received simultaneously, FF 1 is set and FF 2 is cleared. FF 2 is set by the following OD 4 pulses, and only data-available-1 pulses are generated.

5.9 XTL AMPLIFIERS

The XTL amplifiers form the drum words. One XTL amplifier is assigned to each of the 33 bit positions of the drum word and is designated by that position: R5 XTL amplifier, parity XTL amplifier, etc. Levels corresponding to bits of the drum word are furnished to the XTL amplifiers by the 32 4-way OR circuits, the site-identity generator, the clock circuit, and the drum parity circuits. The source of these pulses and levels has been described previously in this chapter and will only be reviewed at this point.

At the first readout, the levels representing the first message word are applied through 4-way OR circuits to the LS through L15 XTL amplifiers. The LS bit of the first message word is applied to the LS XTL amplifier, the L1 bit to the L1 XTL amplifier, etc. Concurrently, the six clock time bits are applied to the R5 through R10 XTL amplifiers; the five site identity bits are applied to the R11 through R15 XTL amplifiers; and the first drum word parity bit derived by the drum parity circuits from clock-time parity, site identity parity, and first message word parity, are applied to the parity XTL amplifier. At OD 1 + 1 time during the first readout, the first drum-write pulse is supplied to all the XTL amplifiers by the drum write circuit; coincidentally, the site-and-clock-time-drum-write pulse is supplied to XTL amplifiers R5 through R15. Each XTL amplifier to which a first message word, site identity, clock-time or parity pulse or level has been applied gates through the drum-write pulse as a corresponding bit in drum word 1. During readout 2, the pulses corresponding to message words 2 and 3 are applied to XTL amplifiers RS through R15 and LS through L15, respectively. Concurrently, drum word 2 parity is computed by the drum parity circuit on the basis of the parity of message words 2 and 3, and an appropriate parity bit is applied to the parity XTL amplifier. At OD 1 + 1 during readout 2, the drum-write-2 pulse is applied to all the XTL amplifiers, forming the second drum word. Message words 4 and 5, third drum word parity, and drum-write pulse 3 are similarly employed to form the third drum word.

Four typical XTL amplifiers are shown in figure 5–47. The LS pulse of message word 1, 3, or 5 is fed through a 4-way OR, clamped to standard levels by an LA, and applied to the gate of the LS XTL amplifier. This gate is strobed by the drum-write pulses. When the

gate is conditioned by an LS message bit level, it passes the drum-write pulse as the LS bit of the drum word. (The pulse is power-amplified for transmission to the Drum System.) The other XTL amplifiers operate similarly. However, the R5 through R15 XTL amplifiers have two inputs. For example, during the first readout, site bit 5 is applied to GT 2 of the R11 XTL amplifier. Gate 2 is strobed by the site-and-clock-time-drum-write pulse to supply bit R11 of the first drum word. Simultaneously, GT 1 is strobed by the first drum-write pulse, but there is no level input to GT 1 during the first readout. During readout 2, the R11 bit of message word 2 is applied to GT 1, which is strobed by the second drum-write pulse to supply bit R11 of drum word 2. There is no conditioning input or strobe to GT 2 during readout 2. During readout 3, the R11 bit of message word 4 is applied to GT 1 which is strobed by drum-write pulse 3 to form bit R11 of drum word 3. There is no conditioning input or strobe to GT 2 during readout 3.

Gate 2 of XTL amplifier R5 receives clock bit 6 during readout 1; otherwise, operation of XTL amplifier R5 is the same as XTL amplifier R11. The parity XTL amplifier receives the output of the drum parity circuit. The gate is strobed by the three drum-write pulses to produce the parity bits of the three drum words.

5.10 PULSE GENERATOR

The pulse generator circuit (fig. 5–48) receives an uninterrupted sequence of OD pulses. The effects of two cycles of OD pulses, OD 1, OD 2, OD 3, and OD 4, are shown in table 5–6 and in figure 5–49. At the start of the first cycle, FF 1 is set, conditioning GT's 1, 2, and 3, and deconditioning GT's 4 and 5. Flip-flops 2 and 3 are clear.

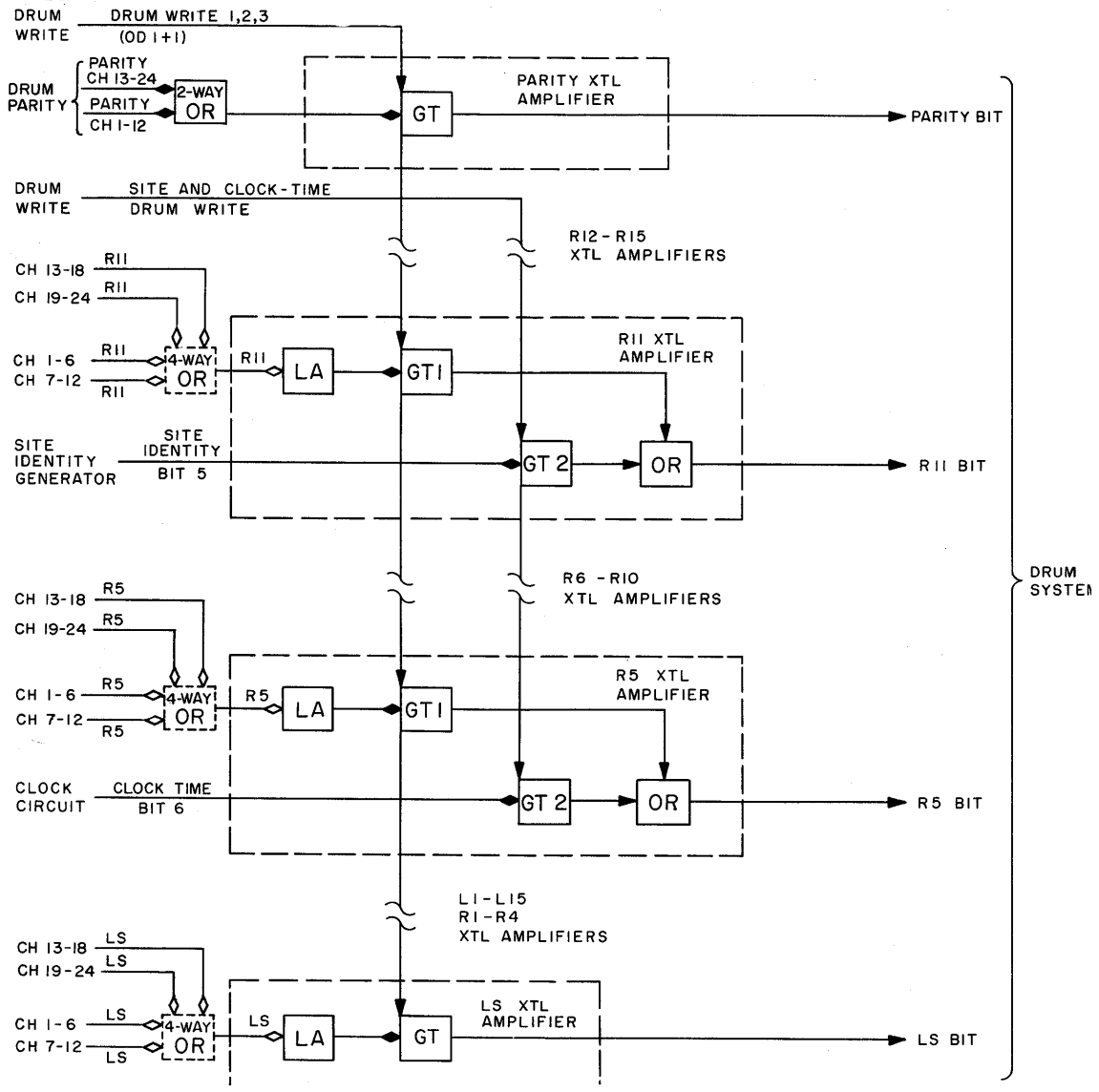
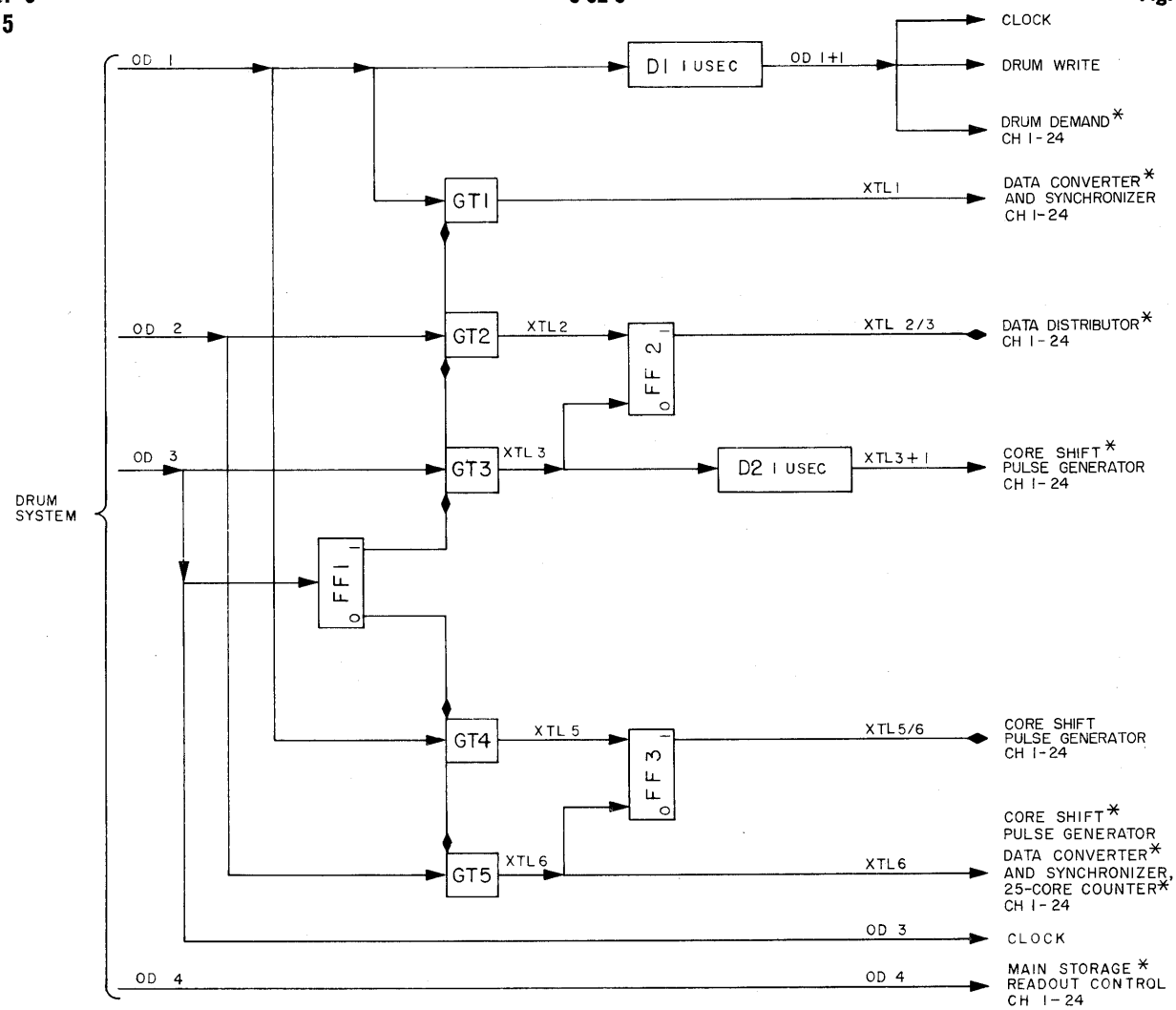


Figure 5–47. Typical XTL Amplifiers, Simplified Logic Diagram



*THROUGH DUPLEX SWITCHING

Figure 5–48. Pulse Generator, Simplified Logic Diagram

TABLE 5–6. OPERATION OF PULSE GENERATOR

INCOMING PULSE	EFFECT IN CIRCUIT	OUTPUT	WHERE USED
First OD 1	a. Delayed 1 μsec in delay circuit D 1	OD 1 + 1	Clock circuit, drum write circuit of drum input section; drum demand circuit of channel input section.
	b. Strobes conditioned GT 1	XTL 1	Data converter and synchronizer, channel input section
	c. Strobes deconditioned GT 4	None	—
First OD 2	a. Strobes conditioned GT 2, setting FF 2	—	—
	b. Strobes deconditioned GT 5	None	—

TABLE 5–6. OPERATION OF PULSE GENERATOR (cont'd)

INCOMING PULSE	EFFECT IN CIRCUIT	OUTPUT	WHERE USED
First OD 3	a. None	OD 3	Clock circuit, drum input section
	b. Strobes conditioned GT 3, clearing FF 2; FF 2 is therefore set from first OD 2 to first OD 3 pulse.	XTL 2/3	Data distributor, channel input section
	c. Output of GT 3 delayed 1 μsec in D2	XTL 3 + 1	Core shift pulse generator, channel input section
	d. Clears FF 1 through complement input; GT 1, GT 2, GT 3 are deconditioned. GT 4 and GT 5 are conditioned. However, because of time delay, GT 3 has already passed OD 3 pulse.	—	—
First OD 4	None	OD 4	Main storage readout control, channel input section
Second OD 1	a. Delayed 1 μsec in delay circuit D 1	OD 1 + 1	Same as first OD 1 + 1
	b. Strobes GT 1, now deconditioned	None	—
Second OD 2	a. Strobes GT 2, now deconditioned	None	—
	b. Strobes GT 5, now conditioned	XTL 6	Data converter and synchronizer, core shift pulse generator, 25-core counter, channel input section.
	c. Output of GT 5 clears FF 3. This flip-flop is therefore set between second OD 1 pulse and second OD 2 pulse.	XTL 5/6	Core shift pulse generator
Second OD 3	a. None	OD 3	Clock circuit, drum input section
	b. Strobes GT 3, still deconditioned.	None	—
	c. Sets FF 1 through complement input. GT 1, GT 2, GT 3 are conditioned; GT 4, GT 5 are deconditioned.	—	
Second OD 4	None	OD 4	Same as first OD 4

Note: All outputs to channel input section pass through duplex switching (Ch 4).

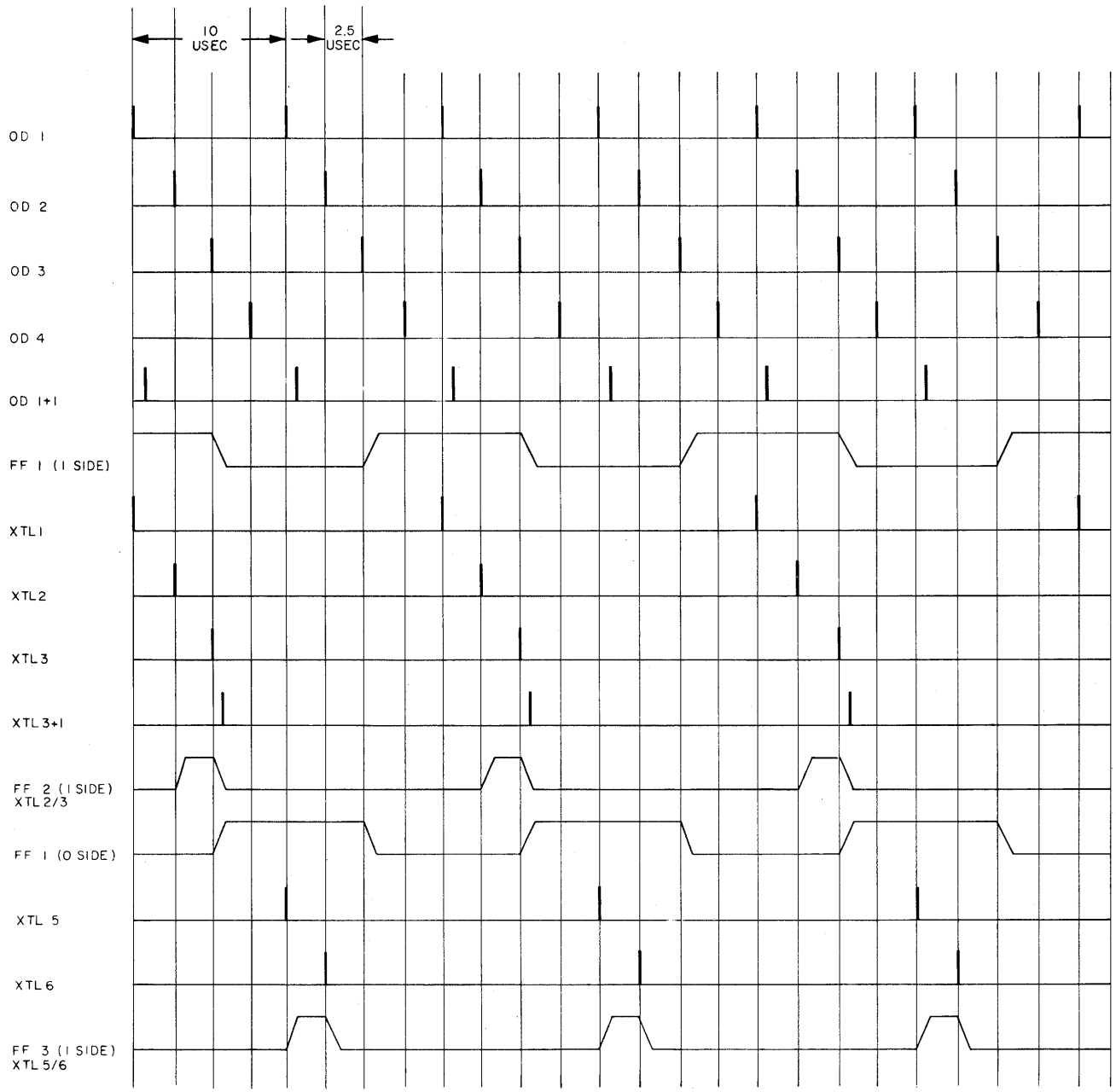


Figure 5—49. Pulse Generator, Timing Chart

5.11 READOUT ALARM

The readout alarm circuit (fig. 5—50) provides an alarm indication at the duplex maintenance console whenever a message in any one of the channels is destroyed. A message will be destroyed if another message is shifted into the main storage registers (channel input section) while the registers still contain the previous message: a slot has not yet been found for it on the drum. Under this circumstance, the channel drum demand circuit sends a readout alarm pulse through duplex switching to the drum input section.

The 24 readout alarm lines are consolidated into a single line by the two 12-way readout alarm OR circuits and the 2-way OR. The output of the 2-way OR sets the readout alarm flip-flop if a message is destroyed by any channel. When this flip-flop is set, it lights the READOUT ALARM neon (XTL DUPLEX EQUIPMENT, duplex maintenance console, module D, lower section). Operation of the CLEAR ALARMS switch applies a triggering voltage to the pulse generator which sends a reset pulse to the readout alarm flip-flop and to the clock alarm flip-flop.

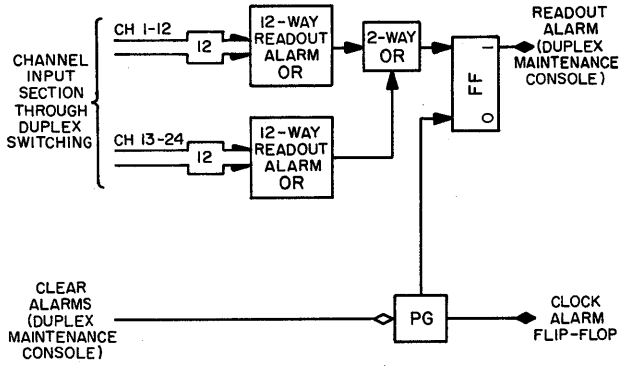


Figure 5–50. Readout Alarm Circuit, Simplified Logic Diagram

PART 6
TEST PATTERN GENERATOR TS-923/FSQ

CHAPTER 1
INTRODUCTION

1.1 SCOPE

This part presents the theory of operation of Test Pattern Generator TS-923/FSQ. The equipment consists of three independently operable TPG's: the LRI, XTL, and GFI. This chapter contains introductory information on all three TPG's; the next three chapters respectively concern the LRI, XTL, and GFI TPG's.

Note

In this part, Test Pattern Generator refers to an individual (LRI, XTL, or GFI) test pattern generator; the overall equipment is regarded as the combination of the three TPG's and is referred to as such, or by its official nomenclature.

1.2 PURPOSE OF EQUIPMENT

1.2.1 General

The purpose of the TPG's is to generate signals simulating the telephone line inputs to the LRI, XTL, and GFI elements of the Input System. These inputs originate outside the Direction Central: XTL inputs at other Direction Centrals and LRI and GFI inputs at radar sites. For this reason, these inputs introduce uncertainties in evaluating the performance of the LRI, GFI, and XTL elements, beyond those pertaining to these elements themselves. Accordingly, it is desirable to have a source of fully controllable test signals for the three elements. Such a source is provided by the TPG's. During installation, before the Direction Central is integrated into SAGE, the TPG's assist in preliminary tests and adjustments and subsequently provide a valuable maintenance tool.

The TPG outputs consist of a basic sine wave timing frequency and combinations of digital bits generated synchronously with the timing frequency in patterns similar to the information-conveying inputs from radar sites or other Direction Centrals. These simulated inputs are briefly described below and are fully described and related to the operation of the equipment in the chapters devoted to each of the TPG's.

1.2.2 LRI TPG

The LRI TPG generates a message variable in length from 32 to 64 bits. The first or sync bit indicates the beginning of the message or separates continuously repeated messages. Data bits form the remainder of the message.

Messages may be initiated, terminated, or continuously repeated, and their composition may be established under either manual or computer control.

1.2.3 XTL TPG

The XTL TPG message length is fixed at 92 bits; in other respects, the description of the LRI TPG message above is applicable to it.

1.2.4 GFI TPG

The GFI TPG generates azimuth and target signals in synchronism with a timing frequency, which is also referred to as the range signal. The azimuth cycle (time between azimuth signals) may vary from 8 to 255 range cycles. Every 256th azimuth signal is a north-azimuth signal which is composed of two azimuth signals at successive range cycles. Azimuths are counted from the north-azimuth signal. Range cycles are counted from each azimuth signal. Azimuth and range count may be used to establish the position of a target; e.g., 32nd range cycle of 51st azimuth.

The GFI TPG is capable of generating various target patterns or types of coverage and of simulating abnormal conditions, including missing or spurious azimuth signals and early or late north-azimuth signals. Operation may be initiated and terminated under either manual or computer control.

1.3 PHYSICAL DESCRIPTION

1.3.1 General

The TPG's are housed in unit 92 (fig. 6–1) located in the maintenance area of the Direction Central. Operating controls are distributed between unit 92 and module B of the simplex maintenance console.

Unit 92 comprises four standard modules, one for each TPG and a utility module. Each TPG module mounts standard pluggable units which provide the nec-

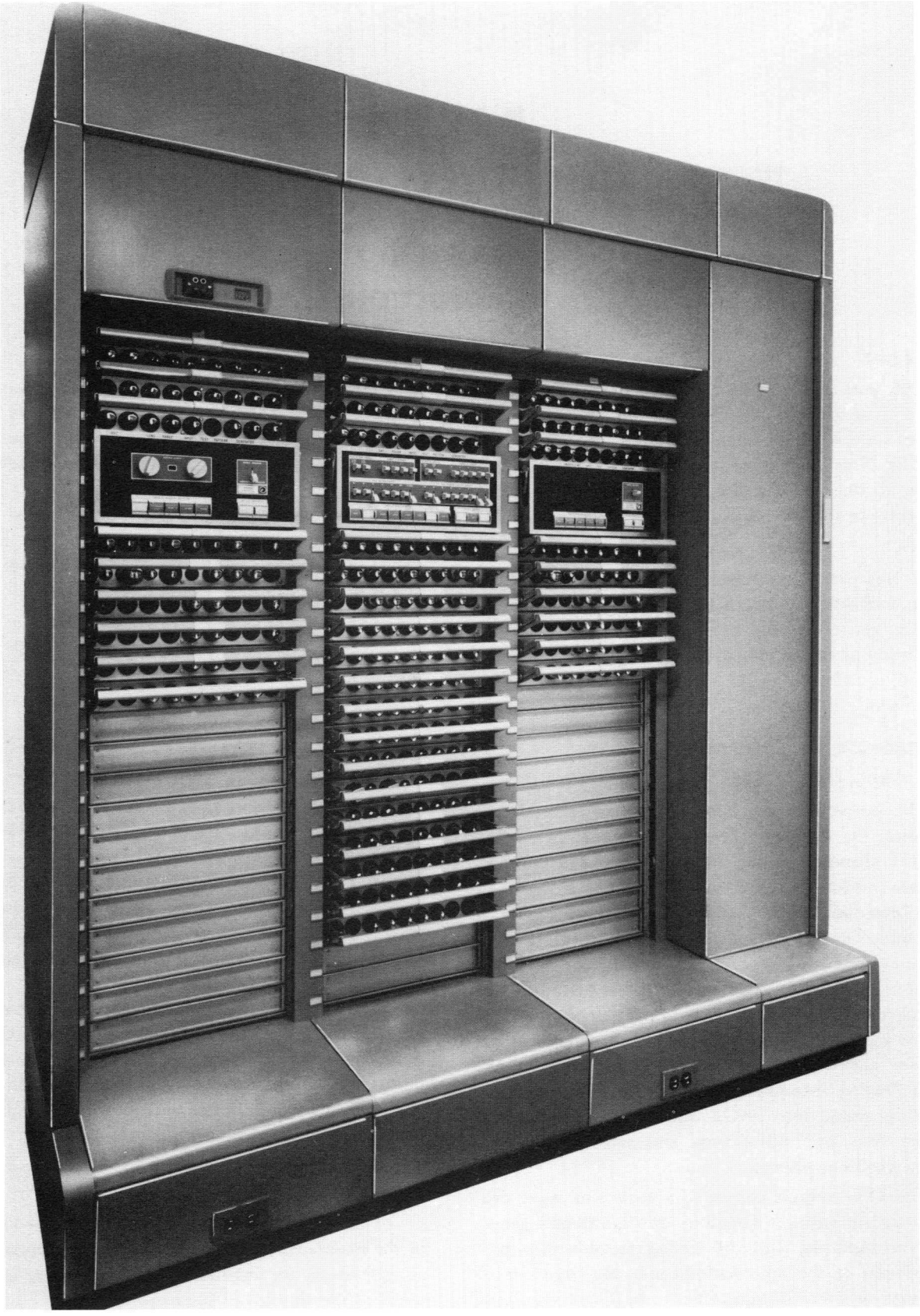


Figure 6–1. Test Pattern Generator TS-923/FSQ

essary TPG circuitry and a control panel. Module B of the simplex maintenance console mounts three control panels, one for each TPG. TPG controls are described below.

1.3.2 LRI TPG Controls

The TPG LRI control panel on module B of the simplex maintenance console (fig. 6–2) contains the

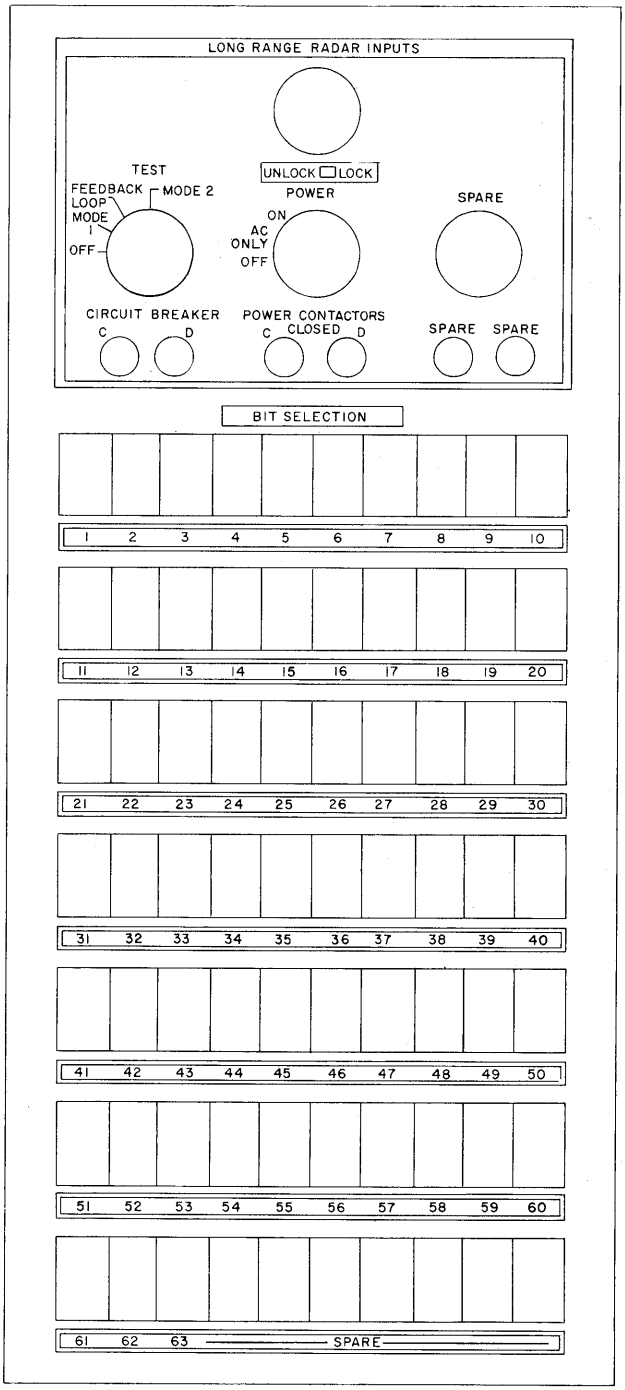


Figure 6–2. LRI TPG Control Panel, Simplex Maintenance Console

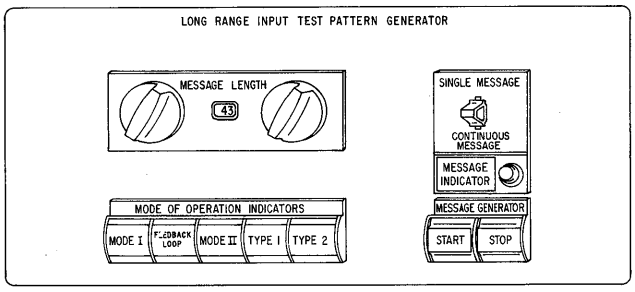


Figure 6–3. LRI TPG Control Panel, Unit 92

power control and indicators for this TPG, the TEST switch which determines the TPG mode of operation (discussed later in this chapter), and the BIT SELECTION switches which are used to manually establish the composition of a message.

The control panel on the LRI TPG module of unit 92 (fig. 6–3) contains the remaining controls and indicators for operating this TPG: START and STOP pushbuttons (these are signal, not power controls), a SINGLE MESSAGE-CONTINUOUS MESSAGE switch, a MESSAGE LENGTH control and indicator, and mode and mode-type indicators.

1.3.3 XTL TPG Controls

The XTL TPG controls (figs. 6–4 and 6–5) are similar in function and location to the LRI TPG controls. There are more BIT SELECTION switches because the message is longer; there is no MESSAGE LENGTH control because the message length is fixed.

1.3.4 GFI TPG Controls

The GFI TPG control panel on module B of the simplex maintenance console (fig. 6–6) contains only the power control and the TEST switch for this TPG. All other controls and indicators are located on the control panel of the unit 92 GFI TPG module (fig. 6–7). The START and STOP pushbuttons, mode and mode-type indicators, and the various controls establish the pattern and characteristics of the target and the azimuth and north-azimuth signals.

1.4 GENERAL FUNCTIONAL DESCRIPTION

There are certain fundamental similarities in the functioning of the TPG's. Each produces three outputs on as many lines. The outputs of the LRI and XTL TPG's are called timing, sync, and data signals. The outputs of the GFI TPG are called range, azimuth, and target signals, analogous to the timing, sync, and data signals produced by the LRI and XTL TPG's. The three outputs of each TPG are fed to individual bus bars which makes them available to the input switching section of the appropriate Input System elements.

In one type of operation, feedback loop, the LRI and XTL TPG's do not generate signals; they act only

as switching and impedance-matching devices in the transfer of signals from the Output System to the Input System. This use is incidental to the basic purpose of the TPG's and is not considered in the discussion below.

The overall operation of each TPG may be thought of in terms of two primary functions: signal generation

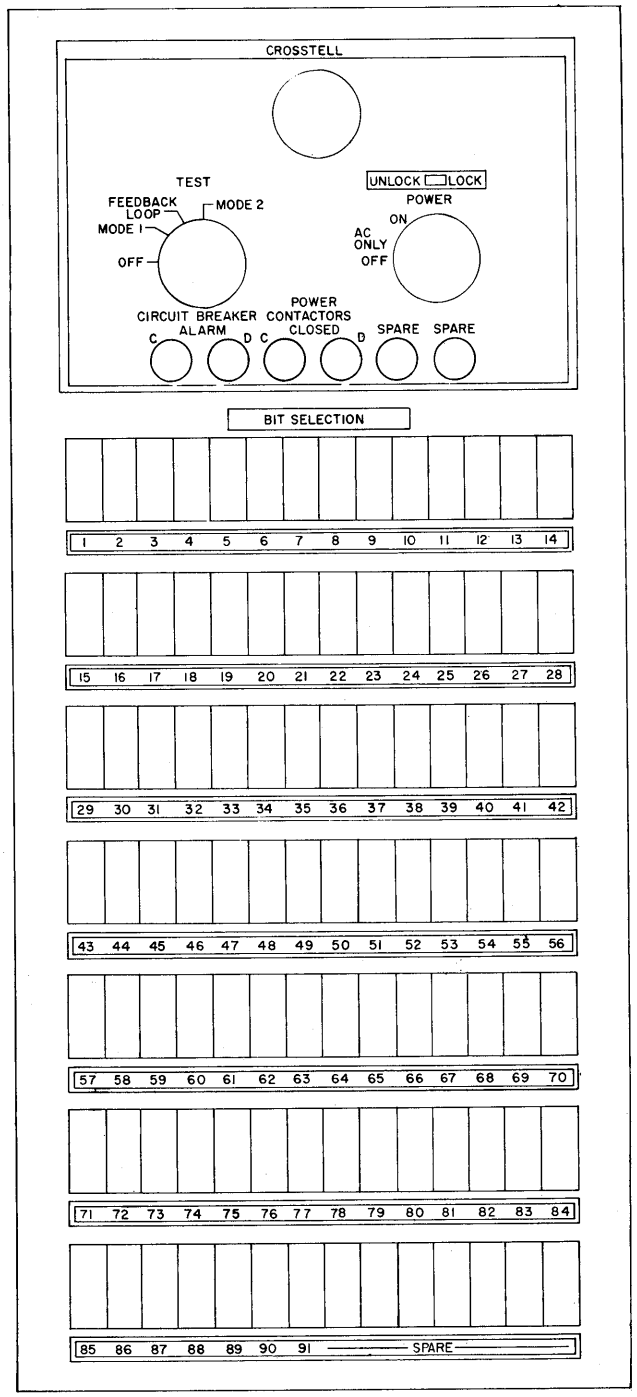


Figure 6–4. XTL TPG Control Panel, Simplex Maintenance Console

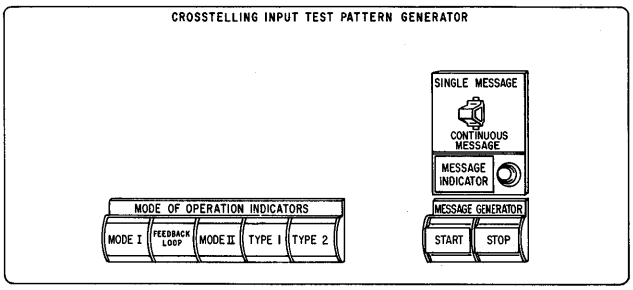


Figure 6–5. XTL TPG Control Panel, Unit 92

and signal control. Signal generation begins with a basic timing frequency: 1,300 cps in the LRI and XTL TPG and 1,600 cps in the GFI TPG. The timing frequency serves three purposes:

a. It serves as the timing output signal (range signal in the GFI TPG).

b. It provides the raw material for the other two outputs (sync and data or azimuth and target).

c. It provides timing for the logic operations of the TPG itself (counting, register reset, core shift, etc.).

The other operations of the TPG are control operations; they determine the start and stop of signal generation and the pattern or configuration of the sync and data, or azimuth and target, signals. Control, in turn, may be exercised manually, by the computer, or by a combination of both. The relationship between, and comparative importance of, manual and computer control define the mode of operation. These modes are discussed generally in 1.5 and in detail in subsequent chapters.

Figures 6–8 and 6–9 show the relationship between the TPG's and other portions of the Direction Central; the command pulses, by means of which the Central Computer exercises control (in mode II) of the TPG, are designated for convenience by the code number of the *OPERATE* instruction which produces them. (For example, the pulse designated *PER 63* is one of the results of a programmed *PER 63* instruction to the Central Computer.) The TPG, in turn, sends certain pulses to the Central Computer which the computer utilizes to maintain co-ordination with the TPG. These pulses are identified, for convenience, by the Central Computer sensing operation with which they are associated; e.g., *BSN 34*.

1.5 MODES OF OPERATION

1.5.1 General

The TPG's may be operated in several modes or mode types, differentiated mainly by the relative extent or potentialities of manual and computer control. The

LRI and XTL TPG's may be operated in mode I, mode II, FEEDBACK LOOP. The GFI TPG may be operated in mode I or mode II.

1.5.2 Mode I

All TPG's operating in mode I are completely under manual control; messages are initiated, terminated, and composed by means of manual controls. This mode is used for specific troubleshooting and for nonprogrammed maintenance in general.

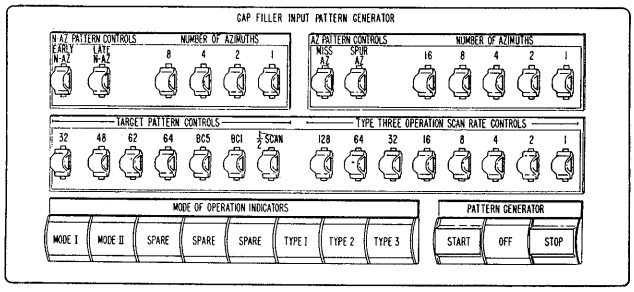


Figure 6–7. GFI TPG Control Panel, Unit 92

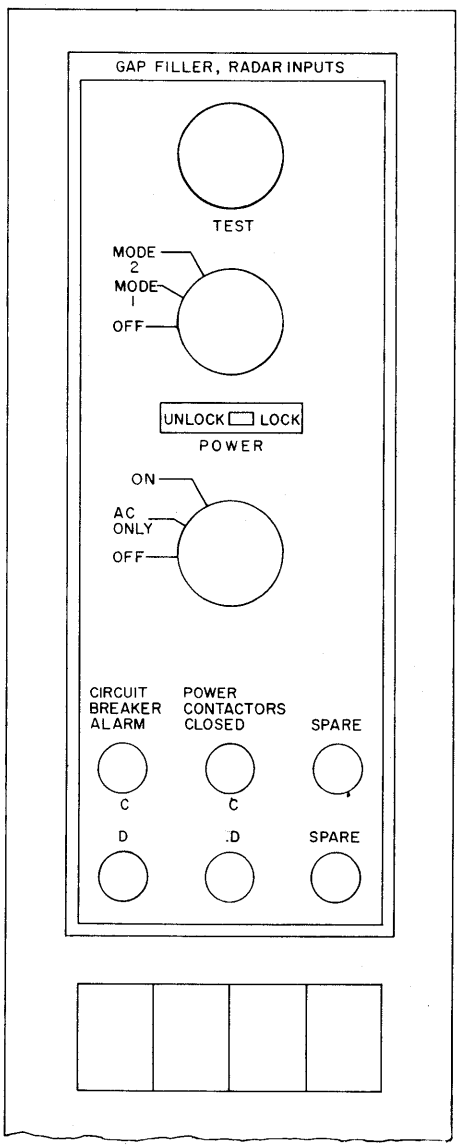


Figure 6–6. GFI TPG Control Panel, Simplex Maintenance Console

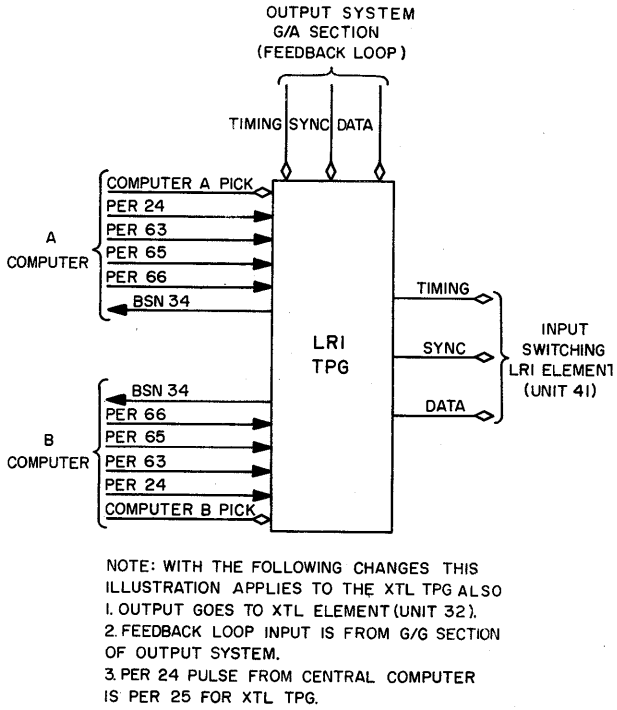


Figure 6–8. LRI TPG System Relationships

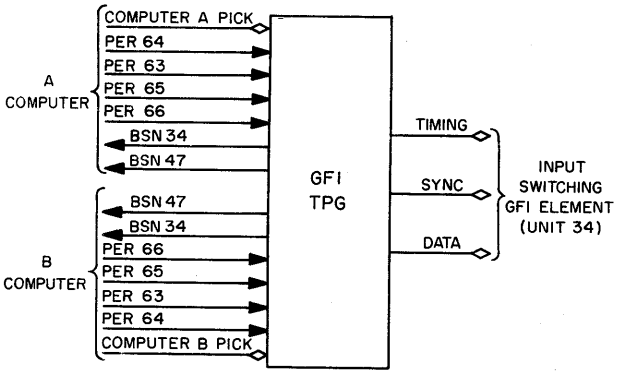


Figure 6–9. GFI TPG System Relationships

1.5.3 Mode II

Mode II operation is utilized for programmed maintenance, generally of a routine type. A TPG operating in this mode is always, to some extent, under computer control. The degree of computer control depends on the type of mode II operation in use. In LRI TPG and XTL TPG operation, mode II is differentiated into types 1 and 2. In GFI TPG operation, mode II is differentiated into types 1, 2, and 3. These types are discussed in detail in succeeding chapters. In general, mode II type 1 operation is characterized by complete computer control; the start and stop of signal generation and signal patterns are program-controlled. In other types of mode II operation, signal patterns are manually controlled, but the computer can resume complete computer control by means of a command pulse.

1.5.4 Feedback Loop

The LRI and XTL TPG's may also be employed in the feedback loop mode. In this form of operation, telephone line messages developed by the Output System are fed back, for test purposes, to the Input System through the TPG. The TPG's serve only as impedance-matching and switching devices in this use.

1.5.5 Mode Controls and Indicators

In all TPG's, the mode of operation is established by the TEST switch on the appropriate panel of the TPG module, simplex maintenance console. Indicator lamps on unit 92 then inform maintenance personnel of the mode and mode type in which the TPG is operating.

1.6 POWER

The TPG is simplex. (Generally, equipment is simplex if its failure will not seriously affect the defense functions of the Direction Central. This is the case with test equipment such as the TPG.)

Normally, a simplex unit may be associated with either the active or standby duplex machines and is provided with a unit status switch for that purpose. The TPG, however, is used to test equipment, whether duplex or simplex, in the standby condition only and is connected to the standby simplex power supply. Accordingly, it requires no unit status switch. Instead, each section of the TPG has a 3-position (ON, OFF, and AC ONLY) POWER switch mounted on its panel in the simplex maintenance console TPG module. Also on this panel are lights to indicate the simplex power supply to which the TPG is connected (C or D POWER CONTACTORS CLOSED) and an alarm condition in the power supply (C or D CIRCUIT BREAKER alarm).

CHAPTER 3
XTL TEST PATTERN GENERATOR

This chapter relates to the operation of the XTL TPG, describing how the output message is produced. The XTL TPG is almost identical, both functionally and physically, to the LRI TPG (Ch 2). Therefore, only the differences between the two TPG's are discussed in detail. Differences in the overall operation are described in 3.1; differences in the detailed operation, in 3.2.

3.1 OVERALL OPERATION

The overall operation of the XTL TPG and LRI TPG are fundamentally the same. The major difference between the two is the fact that the XTL message is fixed at 92 bits (initial sync bit plus 91 data bits). Therefore, no message length register is required. Instead, the terminal-sync pulse is produced by a message data register. Message composition is determined, as in the LRI TPG, by the setting of BIT SELECTION switches (simplex maintenance console) of which there are 91.

3.2 DETAILED OPERATION

All the sections and circuits found in the XTL TPG function identically to the corresponding sections and circuits in the LRI TPG, with the exception of mode switching, the message data register, and mode-type switching.

3.2.1 Mode Switching

The difference between LRI and XTL mode switching is that, in XTL feedback loop operation, the source of test signals is the G/G section of the Output System rather than the G/A section.

3.2.2 Message Data Register

Operation of the XTL and LRI message data register is fundamentally the same. However, to produce a message of 91 data bits, three 36-core registers are required in the XTL TPG. The 1 from CS 30 in the first register primes the first core in the second register. The 1 from the 30th core in the second register primes the first core in the third register. The last five DCG's in the first and second registers are permanently deconditioned by +90V, leaving a total of 91 DCG's in use. The 1 transferred out of the 29th core in the third register is fed to the message control section as the terminal-sync pulse. It leaves the register two shift pulses before the final data pulse, but, as in the LRI TPG, it is delayed three shift pulses in the message control section. Therefore, it enters the sync and data gating circuit one shift pulse after the final data pulse; this is the desired effect.

3.2.3 Mode-Type Switching

Mode-type switching in the XTL TPG differs from this operation in the LRI TPG operation only insofar as mode II type 1 operation is initiated by a *PER 25* pulse in the XTL TPG and by a *PER 24* pulse in the LRI TPG.

CHAPTER 4
GFI TEST PATTERN GENERATOR

4.1 GENERAL

This chapter presents the theory of operation of the GFI TPG. The outputs of the equipment are described in detail (4.2). Modes and mode-types of operation are defined next (4.3). The theory of operation of the equipment is then discussed on the section diagram level (4.4). Since the functions of various circuits depend on the mode or mode-type of operation in effect, circuit operation in each mode and mode-type is discussed on the section diagram level in 4.5. The remaining portion of the chapter (4.6 through 4.14) presents a detailed theory of operation of the equipment on the logic block level.

4.2 SIGNAL COMPOSITION

4.2.1 Types of Signals

The GFI TPG produces signals used to simulate telephone line inputs to the GFI element. The signals are of three types: range, azimuth (and north-azimuth), and target, fed out of the GFI TPG on three separate lines. The signals are briefly described below:

a. Range: 1,600-cps, 2V, peak-to-peak sine wave signal.

b. Azimuth (AZ) and north-azimuth (N-AZ): An azimuth signal is one cycle of a 1,600-cps, 2V, peak-to-peak sine wave produced in synchronism with the range signal. A north-azimuth signal consists of two consecutive cycles of 1,600-cps signal produced in synchronism with the range signal, normally in place of the 256th azimuth signal.

c. Target: One cycle of a 1,600-cps 2V, peak-to-peak sine wave, generated in various patterns, in synchronism with the range signal.

The range signal is continuous and unvarying. The pattern of azimuth and target signals may be varied, however, by manual or computer control or by a combination of the two. These variations are discussed below.

4.2.2 Azimuth and North-Azimuth Cycle

The azimuth cycle; i.e., the time between azimuth signals, may vary from 8 through 255 range cycles. One north-azimuth signal is produced every 256 azimuth cycles, with the exceptions noted in 4.2.4.

4.2.3 Missing and Spurious Azimuth Signals

The GFI TPG is capable of simulating missing azimuth and spurious azimuth conditions. A missing azimuth condition is one in which an azimuth signal is missing from the normal sequence of azimuth signals. A spurious azimuth signal is one inserted between normal azimuth signals. The GFI TPG may be set manually to miss from 1 to 31 azimuth signals following each north-azimuth signal or it may be set to insert spurious azimuth signals following one or more azimuth signals, to a maximum of 31, after the north-azimuth signal. These spurious azimuth signals will occur at the 32nd range cycle after the normal azimuth signal. (Since this is the case, spurious azimuths cannot be produced if the azimuth cycle, variable from 8 to 255 range cycles, is less than 33 range cycles in length.)

4.2.4 Early North and Late North

The GFI TPG is capable of simulating early north or late north conditions. An early north condition is one in which the north-azimuth cycle is less than 256 azimuth cycles. The late north condition is one which the north-azimuth cycle is more than 256 azimuth cycles. North azimuth may be manually advanced or delayed by 1 through 15 azimuth cycles.

4.2.5 Target Patterns

The GFI TPG is capable of generating various target patterns or types of coverage listed below:

a. Circular patterns (patterns forming a circle on a PPI display) of targets occurring in synchronizm with the 32nd, 48th, 62nd, or 64th range cycle of each azimuth; or concentric combinations of these patterns.

b. Blanket coverage of two types, BC-1 or BC-5. BC-1 coverage generates targets in synchronism with every range cycle except the one coincident with the azimuth signal itself. BC-5 coverage generates targets in synchronism with every range cycle except five: the two before, two after, and one coincident with the azimuth signal.

c. Half-scan. Half-scan operation displays targets generated only from the 129th through the 256th azimuth cycles. On a PPI display, targets will appear on only half the screen. The pattern of targets so displayed may be any one of the circular patterns or of the blanket coverage patterns described in a or b, above.

4.3 MODES AND MODE-TYPES OF OPERATION

4.3.1 General

The output signals described in 4.2 may be generated under manual or computer control or by a combination of the two. Control is determined by the mode or mode-type of operation. Two modes are available, selected by the GFI TEST switch (simplex maintenance console). In mode 1 operation, the GFI TPG is completely under manual control; in mode II operation, it is under computer control or under a combination of manual and computer control. There are three types of mode II operation differentiated by the relative extent of computer control over message generation. Modes and mode-types of operation are discussed in 4.3.2 through 4.3.5, below.

4.3.2 Mode I

In mode I operation, message generation is completely under manual control. Operation is initiated by the START pushbutton, and the various parameters of the message, as listed below, are established by manual controls on unit 92:

a. Length of azimuth cycle
b. Number of missing or spurious azimuth signals
c. Early or late north condition and the degree of this condition
d. Target pattern or coverage

Operation may be terminated by means of the STOP pushbutton or changed to mode II by placing the TEST switch in the MODE 2 position.

4.3.3 Mode II Type 1

Mode II type 1 operation is completely under computer control, exercised by means of command pulses from the Central Computer. Specifically, the computer performs the following functions:

a. Initiates message generation by means of a *PER 64* command pulse
b. Utilizes *PER 65* command pulses to generate azimuth or north-azimuth signals
c. Establishes by successive *PER 65* pulses the length of the azimuth cycle which will apply in type 2 operation should the computer program a change in this type of operation.
d. Utilizes *PER 66* command pulses to generate target signals

In type 1 operation, *BSN 34* pulses, synchronized with the 1,600-cps range signal, are returned to the Central Computer to co-ordinate the timing of the command pulses with that of TPG operation.

Type 1 operation may be terminated by the Central Computer or by means of the STOP pushbutton. It may be changed to type 2 operation by means of a *PER 63* pulse from the Central Computer or to type 3 operation by depressing the START pushbutton.

4.3.4 Mode II Type 2

In mode II type 2 operation, the GFI TPG is under a combination of manual and computer control. This type of operation may be initiated only during type 1 operation. The changeover is achieved by a *PER 63* pulse from the Central Computer. The length of the azimuth cycle established in type 1 operation immediately before the changeover continues to apply to type 2 operation and cannot be manually altered. All other message characteristics may be manually controlled however, by means of unit 92 controls. These include:

a. Number of missing or spurious azimuth signals
b. Number of azimuths by which north azimuth is advanced or delayed (early north or late north condition)
c. Target patterns of coverage

In type 2 (and type 3) operation, *BSN 47* pulses are returned to the Central Computer at north-azimuth time. These pulses permit the Central Computer to program transitions from one type of operation to another at north-azimuth time, a requirement of certain GFI maintenance programs.

Type 2 operation will revert to type 1 on receipt of a *PER 64* pulse from the Central Computer or may be changed to type 3 operation by depressing the START pushbutton.

4.3.5 Mode II Type 3

Mode II type 3 operation is initiated by depressing the START pushbutton and is manually controlled in all respects except one: it may be changed to mode II type 1 operation at any time upon receipt of a *PER 64* pulse. In all other ways, this form of operation is the same as mode I operation described in 4.3.2.

4.4 THEORY OF OPERATION ON THE SECTION DIAGRAM LEVEL

4.4.1 General

The theory of operation of the GFI TPG is discussed below on the section diagram level. The functions of the circuit sections listed below are described in general. The relationships between the sections during the various modes and mode-types of operation are discussed in 4.5 and illustrated in figures 6–18 through 6–20.

a. Tuning fork oscillator and pulse generator
b. Output signal generator
c. Mode switching
d. Output signal amplifier
e. Control unit
f. Range counter and storage register

g. Azimuth counter
h. Target pattern
i. Duplex switching

As in the case of the LR1 TPG (2.4 of Ch 2), overall operation can be analyzed as two primary functions: signal generation and signal control. Of the sections listed above, the TFO and pulse generator, output signal generator, and output signal amplifier sections are principally responsible for signal generation. Mode switching participates in both signal generation and control (discussed under signal generation below). The remaining sections perform the signal control function.

4.4.2 Signal Generation Function

4.4.2.1 TFO and Pulse Generator

The TFO and pulse generator produces a 1,600-cps sine wave signal and two standard timing pulses, DCR (—12) and the DCR (0). The 1,600-cps sine wave signal is the basic timing frequency; it is fed to the output signal generator. The DCR (—12) and the DCR (0) outputs (standard pulses occurring, respectively, 12 μsec before, and simultaneously with, the crossing, in a positive-going direction, of the 1,600-cps sine wave signal) are utilized for timing and synchronization in the other circuits of the equipment.

4.4.2.2 Output Signal Generator

The output signal generator generates the range, azimuth and north-azimuth, and target signals. The 1,600-cps signal becomes the range signal. Individual cycles of the 1,600-cps signal become the azimuth and target signals when gated through the output signal generator by azimuth gating and target gating pulses, respectively. These pulses, in turn, may be produced under manual or computer control.

4.4.2.3 Mode Switching

The range, azimuth, and target signals are fed through the mode-switching relays to the output signal

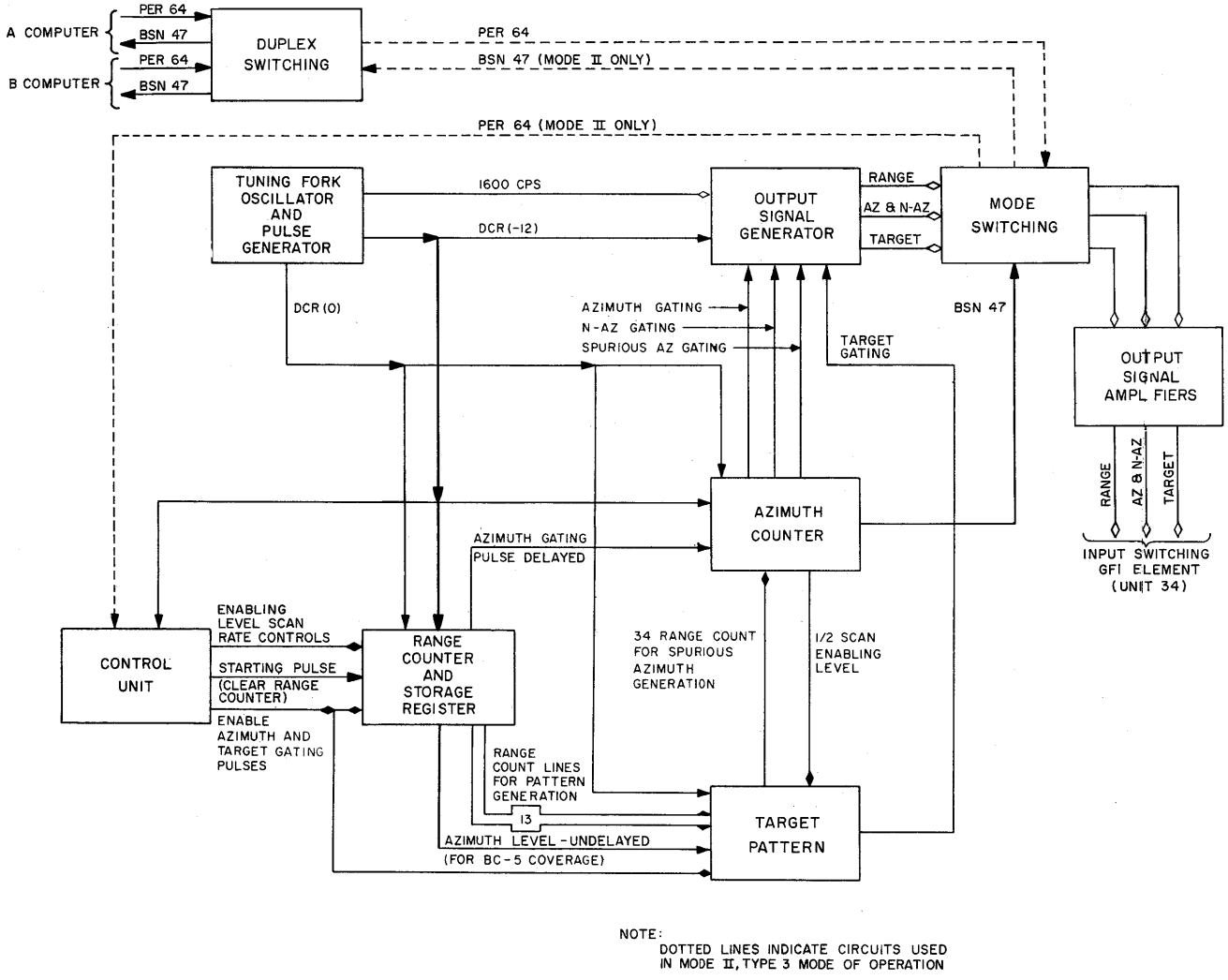


Figure 6—18. GFI TPG Mode I and Mode II Type 3 Operation, Section Diagram

amplifiers. In mode II, a mode-switching relay passes *PER 64* pulses from the Central Computer to the control unit and, during types 2 and 3 of mode II operation *BSN 47* pulses from the azimuth counter to the Central Computer.

4.4.2.4 Output Signal Amplifiers

The output signal amplifiers furnish amplification and impedance-matching for the signals fed from the mode-switching relays to the three (timing, sync, and data) output buses.

4.4.3 Signal Control Function

The control unit, range counter and storage register, azimuth counter, target pattern, and duplex switching sections participate on one form or another of signal control. The function of these sections is described, generally, below; their use in particular modes or mode-types of operation is discussed in greater detail in 4.5.

4.4.3.1 Control Unit

The basic purpose of the control unit is to effect the desired mode or mode-type of operation. For this purpose, it processes command pulses from the Central Computer and the pulses triggered by the START and STOP pushbuttons. The control unit also indicates the mode or mode-type of operation in effect.

4.4.3.2 Range Counter and Storage Register

The range counter and storage register performs the following functions:

a. It maintains a count of range cycles between successive azimuth signals.
b. In mode II type 1 operation, it stores the range count in a storage register; this count automatically establishes the length of the azimuth cycle upon transition to type 2 operation.
c. It incorporates controls (SCAN RATE) for manually establishing the length of the azimuth cycle in mode I and mode II type 3 operation.
d. In all except mode II type 1 operation, it generates the azimuth gating pulse by means of which the azimuth signal and its variations are developed.

4.4.3.3 Azimuth Counter

In all types of operation except mode II type 1 operation, the azimuth counter counts the azimuth gating pulses generated by the range counter and storage register in order to generate the north-azimuth signal; it also incorporates manual controls and circuits by means of which the north-azimuth pulses (missing or spurious azimuth) may be produced.

In mode II type 1 operation, the azimuth counter maintains a count of *PER 65* pulses gated through the control unit or continues without interruption the count developed in type 2 or 3 of mode II operation. This feature permits smooth transition from one type of mode II operation to another.

4.4.3.4 Target Pattern

The target pattern section incorporates the manual control and circuits by means of which various target patterns or types of coverage may be produced (in all modes and mode-types except mode II type 1).

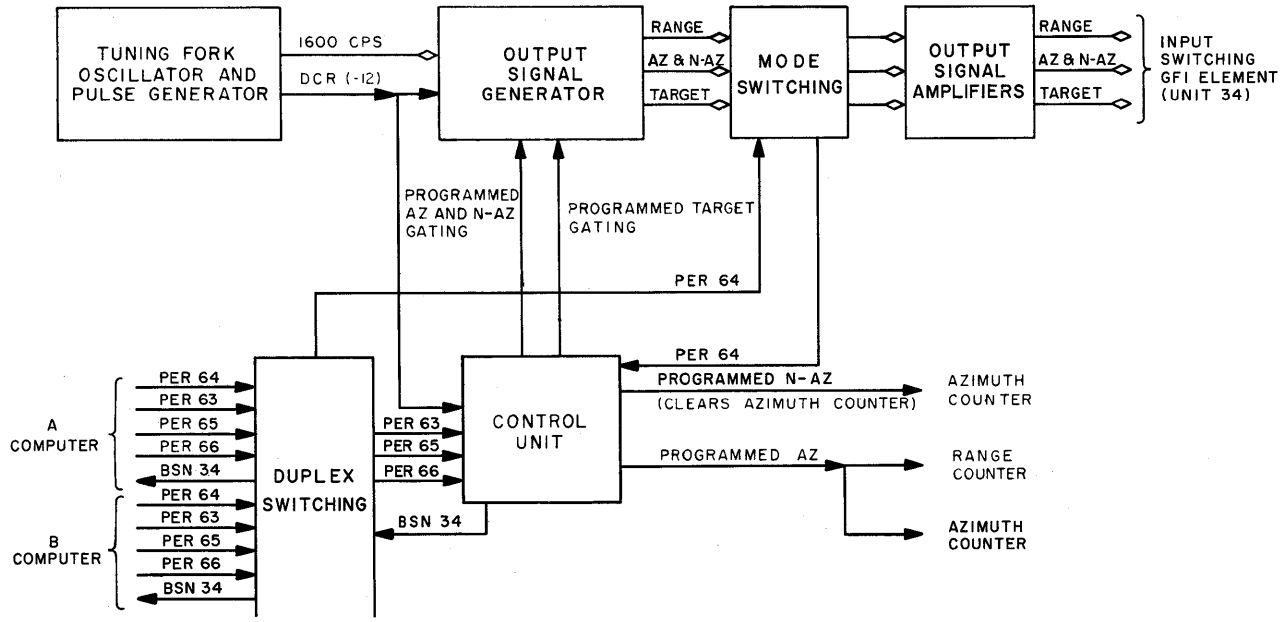


Figure 6–19. GFI TPG Mode II Type 1 Operation, Section Diagram

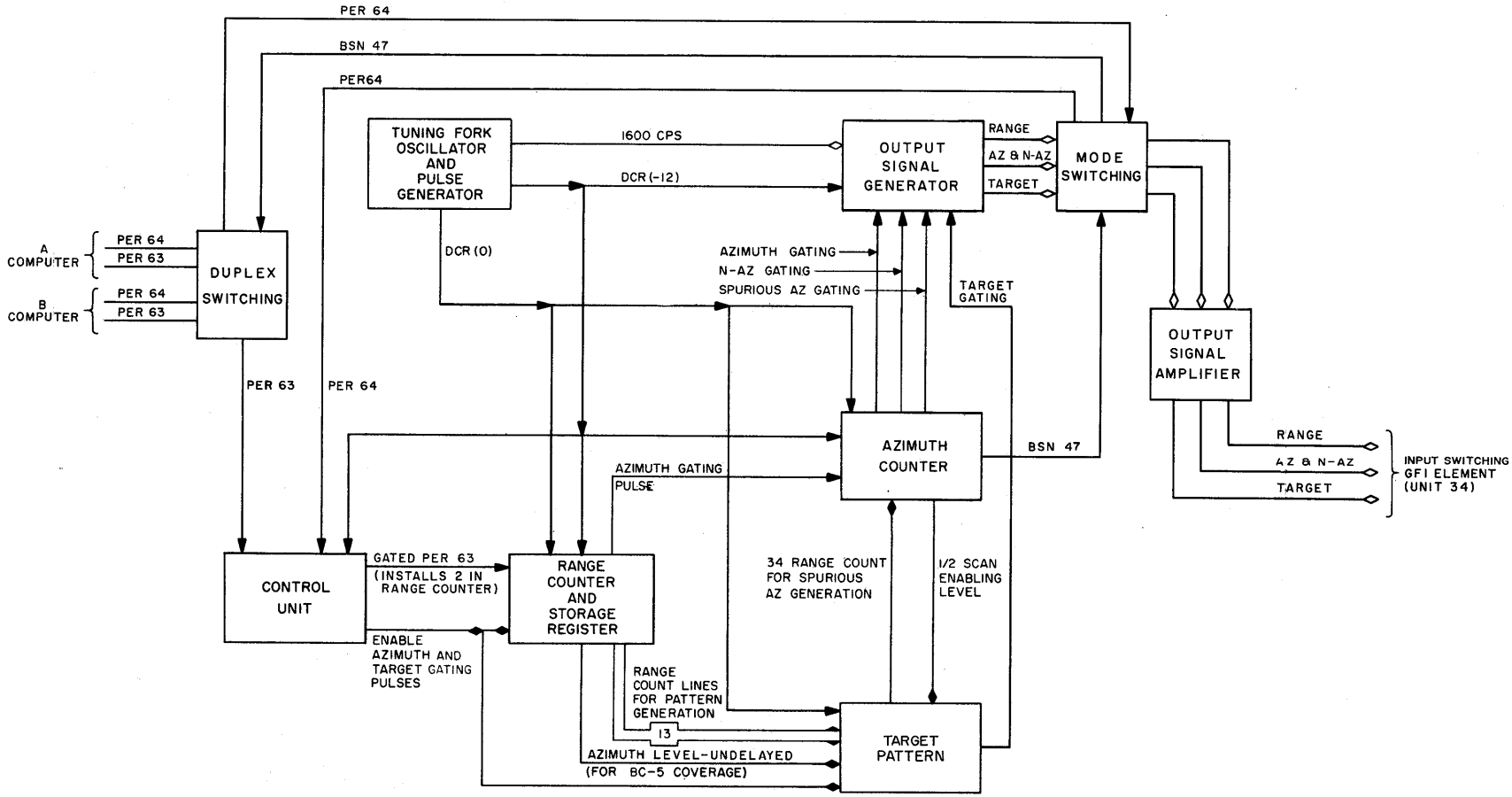


Figure 6–20. GFI TPG Mode II Type 2 Operation, Section Digaram

4.4.3.5 Duplex Switching

Duplex switching provides signal-control connections between the TPG and the standby Central Computer, permitting the TPG to accept command pulses from the standby computer only. There, pulses are routed to the control unit.

4.5 SECTIONAL OPERATION IN VARIOUS MODES AND MODE TYPES

4.5.1 General

The functions of the various sections generally described in 4.4 differ in the various modes and mode-types of operation. Therefore, a theory of operation on the section diagram level is presented below for each mode and mode-type of operation. Appropriate sectional block diagrams accompany the explanation.

4.5.2 Mode I

In mode I operation (fig. 6–18), pressing the START pushbutton clears the range counter, initiating counting action, and makes available an enabling level to the scan rate controls. When a range count equivalent to the setting of the controls is reached, an azimuth pulse is produced. Delayed by two range cycles, it performs the following functions:

a. If not suppressed by the missing azimuth circuitry in the azimuth counter, it is fed as a gating pulse to the signal generator where it gates the azimuth bit in the output message.

b. It steps the azimuth counter.

The azimuth counter maintains a count of azimuth pulses, normally generating a north-azimuth gating pulse, when the count of 256 is reached. However, the contents of the counter may be sensed, by means of manual controls, to substitute an early north or late north pulse for the normal north-azimuth pulse. Other manual controls may be used to similarly sense the contents of the azimuth counter to establish a pattern of missing or spurious azimuth pulses. The north-azimuth pulse, whether normal, early, or late, and the spurious azimuth pulses (if generated) are fed to the output signal generator where, like ordinary azimuth pulses, they gate through azimuth bits of the output passage. The target pattern section senses the range counter for a count selected by target pattern controls switches and generates target-gating pulses accordingly. For example, when target pattern controls switch 64 is operated, a target-gating pulse is generated at the 64th range cycle after every azimuth pulse. These pulses are fed to the signal generator where they gate through a corresponding pattern of target bits in the output message.

4.5.3 Mode II Type 1

In mode II type 1 operation (fig. 6–19), signal control is exercised by *PER 64, PER 65,* and *PER 66* pulses from the Central Computer, processed by the control unit. (In the case of *PER 64,* the pulse is applied to the control unit by way of a mode-switching relay activated by placing the *TEST* switch in the MODE 2 position).

The *PER 64* pulse causes certain gates in the control unit to be conditioned. The *PER 65* pulse is passed by one of these gates and the *PER 66* pulse is passed by another, to the output signal generator where they gate through the azimuth and target bits of the output message. Operation of the STOP pushbutton deconditions the gates referred to above, blocking the *PER 65* and *PER 66* pulses. Signal generation is controlled entirely by the control unit in mode II type 1 operation. In addition, the control unit prepares other circuits for other types of operation. Specifically, it passes *PER 65* pulses to clear the range counter and, at the same time, installs in the storage register the complement of the counter's contents. When type 2 operation is initiated (4.5.4), the count in the storage register at the instant of transition determines the length of the azimuth cycle during type 2 operation. In other words, it performs the same functions as the scan rate controls in mode I operation. In addition, when one programmed azimuth pulse is followed, at the next range cycle, by another, the control unit distinguishes the second pulse as a programmed north-azimuth pulse and utilizes it to clear various flip-flops in the azimuth counter circuit in preparation for a transition to other types of operation.

Following receipt of a *PER 64* pulse, the control unit performs the additional function of returning a *BSN 34* pulse at every range cycle to the computer. By means of these pulses, the computer maintains a range count which it utilizes in programming other instructional pulses furnished in mode II type 1 operation to the GFI TPG For example, in certain programs, transitions from one type of operation to another are made at $\frac{1}{2}$ scan time (128th azimuth cycle) or targets are programmed at $\frac{1}{4}$ scan time (64th azimuth cycle). An azimuth count developed from the range count permits these operations to be programmed at the desired time.

4.5.4 Mode II Type 2

The transition from computer type 1 to type 2 (fig. 6–20) operation is effected by a *PER 63* pulse from the Central Computer. This is passed by a gate conditioned by means of the *PER 64* pulse in type 1 operation. The gated *PER 63* pulse then performs the following functions within the control unit:

a. Deconditions the gates conditioned by the previous *PER 64* pulse, blocking further *PER 63, PER 65,* and *PER 66* pulses at the control unit; *PER 64* pulses are not blocked, however, and

if such a pulse is supplied by the computer, it will effect a transfer back to type 1 operation.

b. Produces an enabling level, utilized in the range counter and storage register and in the target pattern section to permit generation of azimuth-gating and target-gating pulses, respectively.

c. Place a count of two in the range counter to effect proper transition to type 2 operation in the functioning of the range counter and storage level (explained on the logic-level in 4.11.2). Operation of the range counter is essentially the same as mode II type 1 operation. However, the count in the storage register at the instant of transition to type 2 operation, rather than the scan rate controls, determines the length of the azimuth cycle. Operation of the azimuth counter and target pattern sections is essentially the same as in mode I operation. However, in mode II type 2 operation (and also in type 3), a *BSN 47* pulse supplied by the azimuth counter at north-azimuth time is fed back, through one of the mode-switching relays, to the Central Computer. There, it is utilized in programming certain transitions from one type of operation to another which must be referenced to north-azimuth time.

4.5.5 Mode II Type 3

The transition from type 2 or type 1 to type 3 operation is made by depressing the START pushbutton (fig. 6–18). The pulse produced has the following effect:

a. Deconditions or, in the transition from type 2 to type 3 operation, continues to decondition certain gates in the control unit. *PER 63, PER 65,* and *PER 66* pulses are thereby blocked; *PER 64* pulses are not blocked and, if such a pulse is supplied by the computer, type 1 operation is resumed.

b. Clears the range counter and the range storage register as in mode I operation; the range storage register remains cleared and is therefore not involved in determining the length of the azimuth cycle.

c. Makes available, as in mode I operation, an enabling level to the scan rate controls. These controls, in conjunction with the range counter, determine the length of the azimuth cycle.

4.6 TFO AND PULSE GENERATOR

The GFI TPG TFO and pulse generator (fig. 6–21) operated similarly to this section in the LRI TPG (refer to 2.5 of Ch 2). The output of the TFO is 1,600 cps. This output is processed by DCR 1 into DCR (—12) standard pulses which are supplied to the output signal generator, control unit, range counter and storage register, and azimuth counter. The DCR (—12) pulses are also converted, by SS 1 and PG 1, to DCR (0) pulses which are fed to the range counter and storage register, azimuth counter, and target pattern control. The TFO frequency is also fed directly to the output signal generator which utilizes it, after amplification, as the range signal.

4.7 OUTPUT SIGNAL GENERATOR

The output signal generator (fig. 6–22) operates similarly to this section in the LRI TPG (refer to 2.6 of Ch 2). Gating pulses supplied to this section by other sections gate through individual cycles of the 1,600-cps signal as azimuth (or north-azimuth) and target signals. The azimuth flip-flop, FF 2, may be set by a *PER 65* pulse passed by the control unit, a delayed azimuth-gating pulse developed by the range counter and storage register, a north-azimuth pulse developed by the azimuth counter, or a spurious azimuth pulse also developed by the azimuth counter. When set, FF 2 conditions LGT which then passes a cycle of the 1,600-cps

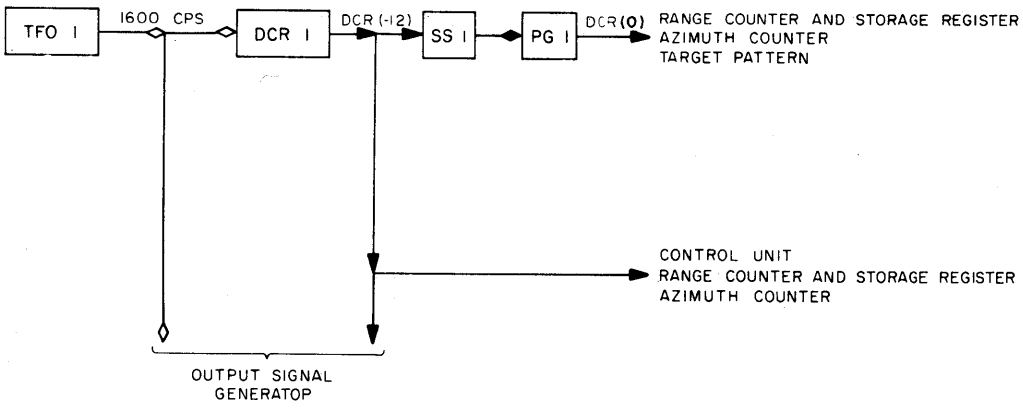


Figure 6–21. GFI TPG TFO and Pulse Generator, Simplified Logic Diagram

signal as one bit of the azimuth signal. The target flip-flop, FF 1, may be set by a *PER 66* pulse passed by the control unit as a target-gating pulse developed in the target pattern control section. The set side of the FF 1 conditions LGT 1, gating through a cycle of the 1,600-cps signal as one bit of the target signal. The command pulses from the computer are supplied in mode II type 1 operation; the nonprogrammed inputs, in all other types of operation.

4.8 MODE SWITCHING

Relay 92BD(K1) (fig. 6–22) is energized when the TEST switch is in the MODE 1 position passing the range, azimuth, and target signals from the output signal generator to the GFI test buses. Relay 92BD(K2) is energized when the TEST switch is placed in the MODE 2 position with the following effects. Relay 92BD(K1) is energized through contacts 6a and 6c of 92BD(K2). *PER 64* pulses from the Central Computer are fed through contacts 5a and 5c of 92BD(K2) to the control unit; in mode II types 2 and 3 operation, a *BSN 47* pulse is fed from the azimuth counter at north-azimuth time through contacts 4a and 4c to the Central Computer.

4.9 OUTPUT SIGNAL AMPLIFIERS

The GFI TPG output signal amplifiers consist of three DLD circuits, each of which provides amplification and impedance matching for one of the TPG outputs: range, azimuth and north-azimuth, and target.

4.10 CONTROL UNIT

Operation of the control units (fig. 6–23) differs for each mode and mode-type. The logic is therefore discussed separately.

4.10.1 Mode I Operation

In mode I operation, depressing the START push-button triggers PG 1, clearing FF 1 and FF 2 through OR 1 and OR 3; the output of AND 2 is therefore up, supplying an enabling level to the scan rate switches.

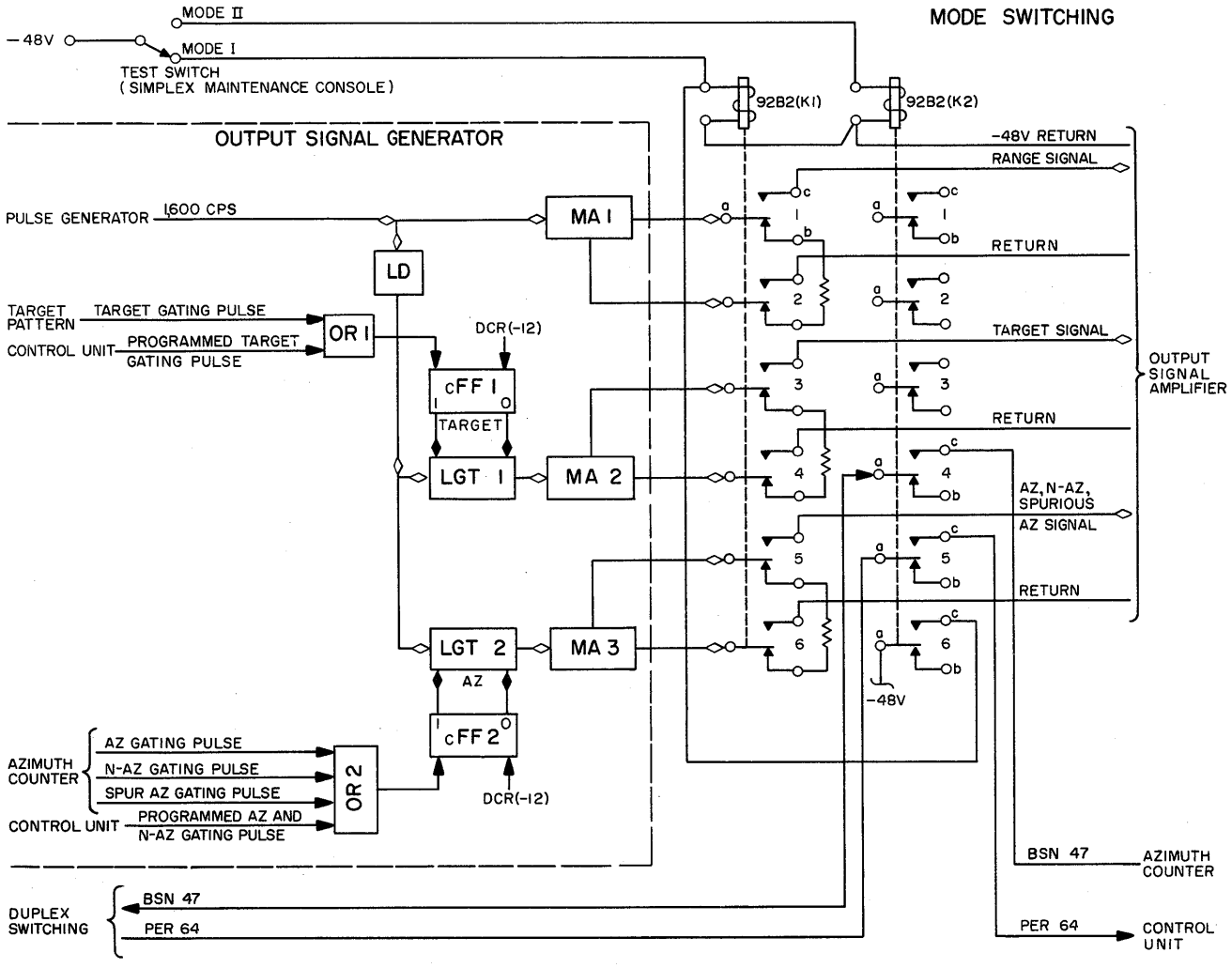


Figure 6–22. GFI TPG Output Signal Generator and Mode Switching, Simplified Logic Diagram

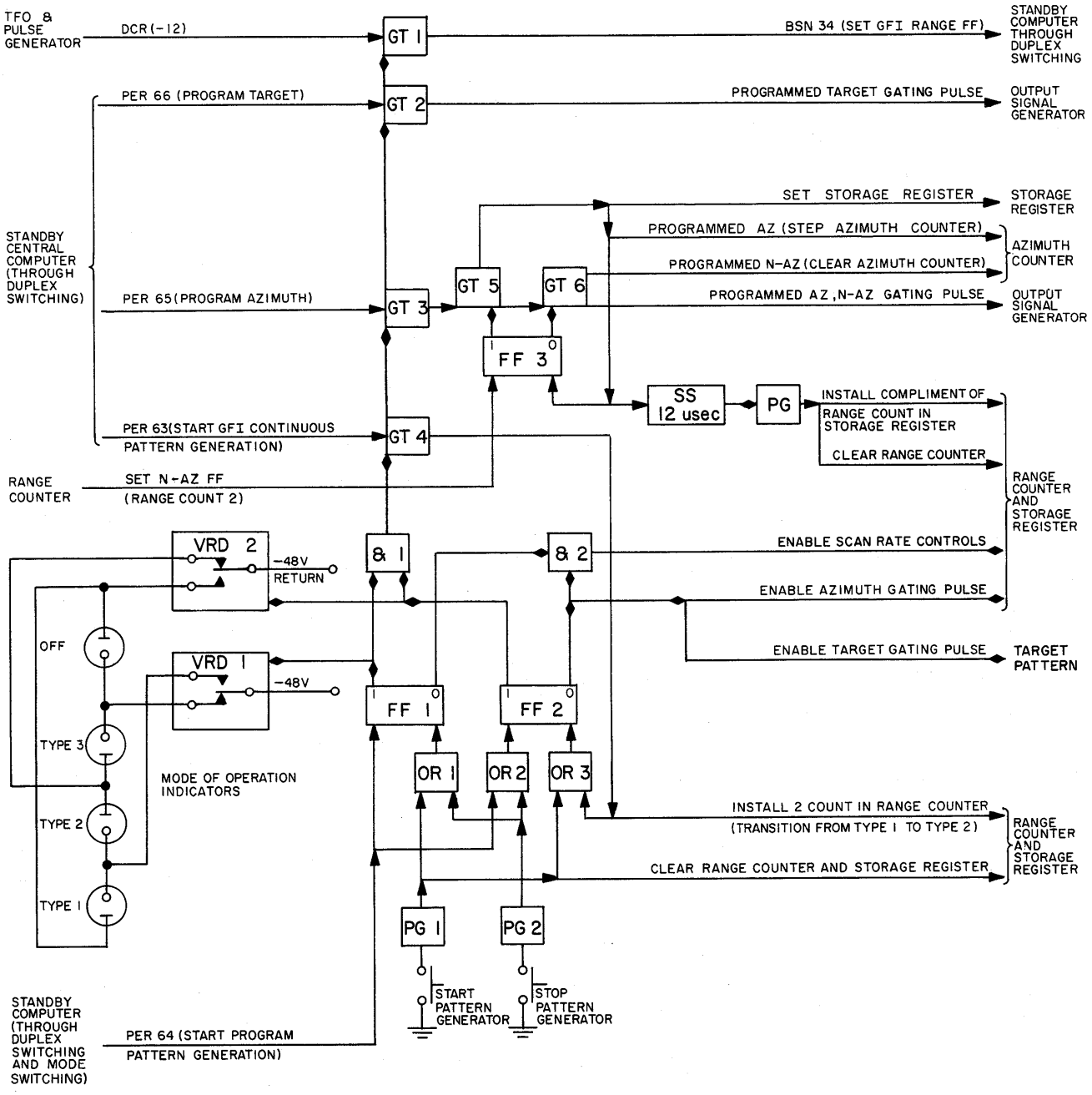


Figure 6–23. Control Unit, Simplified Logic Diagram

The clear side of FF 2 also supplies an enabling level to the range counter and storage register and to the target pattern control sections, the employment of which will be discussed in connection with these sections. Other circuits of the control unit are not essentially involved in mode I operation.

4.10.2 Mode II Type 1 Operation

In mode II type 1 operation, a *PER 64* pulse (fed through mode-switching relay 92BD(K2)) sets FF 1 and FF 2, the latter through OR 2. The output of AND 1 is thereby brought up, conditioning gates 1, 2, 3, and 4. The control unit is now prepared to accept further command pulses from the computer. In type 1 operation, the computer prepares a message by means of programmed *PER 65* and *PER 66* pulses. The *PER 65* pulse passes through conditioned GT 3 and is then fed to the output signal generator where it serves to gate through an azimuth bit in the output message.

The *PER 65* pulse is also fed to GT 5. Gate 5, GT 6, and FF 3 form a selective circuit to differentiate pro-

grammed north-azimuth and azimuth pulses. (A north-azimuth pulse is one which follows an azimuth pulse at the next range cycle.) The circuit operates as follows. FF 3 is set at range count 2 and GT 5 is conditioned. Gate 5 passes the *PER 65* pulse which sets the range storage register, steps the azimuth counter, clears FF 3, and, after a 12-μsec delay, causes the complement of the range count to be installed in the range storage register and the range counter to be concurrently cleared. At the next range count 2, FF 3 is again set. The action of the circuit is complete with respect to a single *PER 65* (normal-azimuth) pulse which has essentially been unaffected by the circuit. However, when a second azimuth pulse immediately follows the first azimuth pulse (N-AZ), it finds FF 3 cleared, GT 6 conditioned, and GT 5 down. Consequently, the second azimuth pulse is diverted through GT 6 to the azimuth counter circuit which recognizes it as a north-azimuth pulse. At the first range count 2, after the north-azimuth pulse, FF 3 is set, GT 5 is conditioned, and subsequent *PER 65* pulses pass through unaffected to the range counter until the next double (north-azimuth) pulse arrives, whereupon the action described above is repeated.

PER 66 pulses pass through conditioned GT 2 to the output signal generator where they serve to gate through the target bits of the output message.

Conditioned GT 1 passes DCR (—12) pulses as *BSN 34* pulses to the Central Computer as long as type 1 operation continues.

4.10.3 Mode II Type 2 Operation

The transition from type 1 to type 2 operation is affected by a *PER 63* pulse. Gate 4, conditioned by means of a previous *PER 64* pulse, passes the *PER 63* pulse which clears FF 2 through OR 3. The output of AND 1 is therefore down and gates 1, 2, 3, and 4 are no longer conditioned, thus, in effect, disconnecting the Central Computer except for the *PER 64* line itself. The clear side of FF 2 furnishes an enabling level, as in mode I operation, to the range counter and storage register and to the target pattern control section. Note, however, that unlike the condition in mode I, FF 1 remains set; therefore, the output of AND 2 is down and no enabling level is supplied to the scan rate switches.

4.10.4 Mode II Type 3 Operation

Mode II type 3, like mode I, operation is initiated by the START pushbutton. The control unit then operates as in mode I. However, relay 92BD(K2) is energized, making the control unit accessible to *PER 64* pulses, which is not the case in mode I operation. A *PER 64* pulse, if fed from the Central Computer, will cause type 3 to revert to type 1 operation.

4.10.5 Mode-Type Indications

The control unit also drives indicators showing the mode type of operation in effect. The circuits function as follows: in type 1 operations, FF 1 and FF 2 are set by the *PER 64* pulse, triggering both relay drivers VRD 1 and VRD 2. The —48V is thereby applied across the TYPE 1 indicator. (It is also applied to the TYPE 2, TYPE 3, and OFF indicators; these, however, are in series and the —48V is insufficient to light them.) In type 2 operation, FF 1 remains set, but FF 2 is cleared. Therefore, VRD 1 is triggered, but VRD 2 is not, and, consequently, —48V is applied across the TYPE 2 indicator. In type 3 operation, both FF 1 and FF 2 are clear; therefore, neither VRD 1 nor VRD 2 is triggered, and —48V is applied across the TYPE 3 indicator. When the STOP pushbutton is depressed, FF 1 is cleared and FF 2 is set. Correspondingly, VRD 2 is triggered and VRD 1 is not, and —48V is applied across the OFF indicator.

4.11 RANGE COUNTER AND STORAGE REGISTER

4.11.1 General

The range counter and storage register (fig. 6–24) produces the pulses that gate through the azimuth bits of the output message. It contains the circuitry which establishes, under either manual or computer control, the length of the azimuth cycle; i.e., the time between azimuth pulses measured in range cycles. Five major circuits are found in the section: range counter, storage register, 9-way AND, SCAN RATE controls, and an azimuth delay circuit. The range counter counts the range cycles in the azimuth cycle. In mode I type 1 operation, the programmed azimuth (*PER 65*) pulse delayed 12 μsec installs the complement of this count in the storage register. The AND circuit senses the contents of the range counter and, in mode II type 1 operation, the storage register, or, in other types of operation, the condition of the scan rate controls. When all inputs to the AND are up, an azimuth-gating pulse is generated. The output delay circuit delays this pulse by two range cycles to simplify generation of the BC-5 target function (4.13.4). Operation of the circuits is explained at the logic level below.

4.11.2 Range Counter

The range counter uses eight flip-flops, FF 1 through FF 8, and seven associated gates, GT 1 through GT 7, in a conventional counting operation. The counter is stepped by DCR (—12) pulses and cleared by a pulse fed through OR 1 from one of three sources. These sources are PG 1 in the control unit, when triggered by the START pushbutton, *PER 65* pulses gated through the control unit, or azimuth-gating pulses (undelayed) returned from the output delay circuit.

In mode I operation, the range counter is cleared initially by a pulse from PG 1 and subsequently by undelayed azimuth-gating pulses. The range counter thus maintains a range count between azimuth-gating pulses.

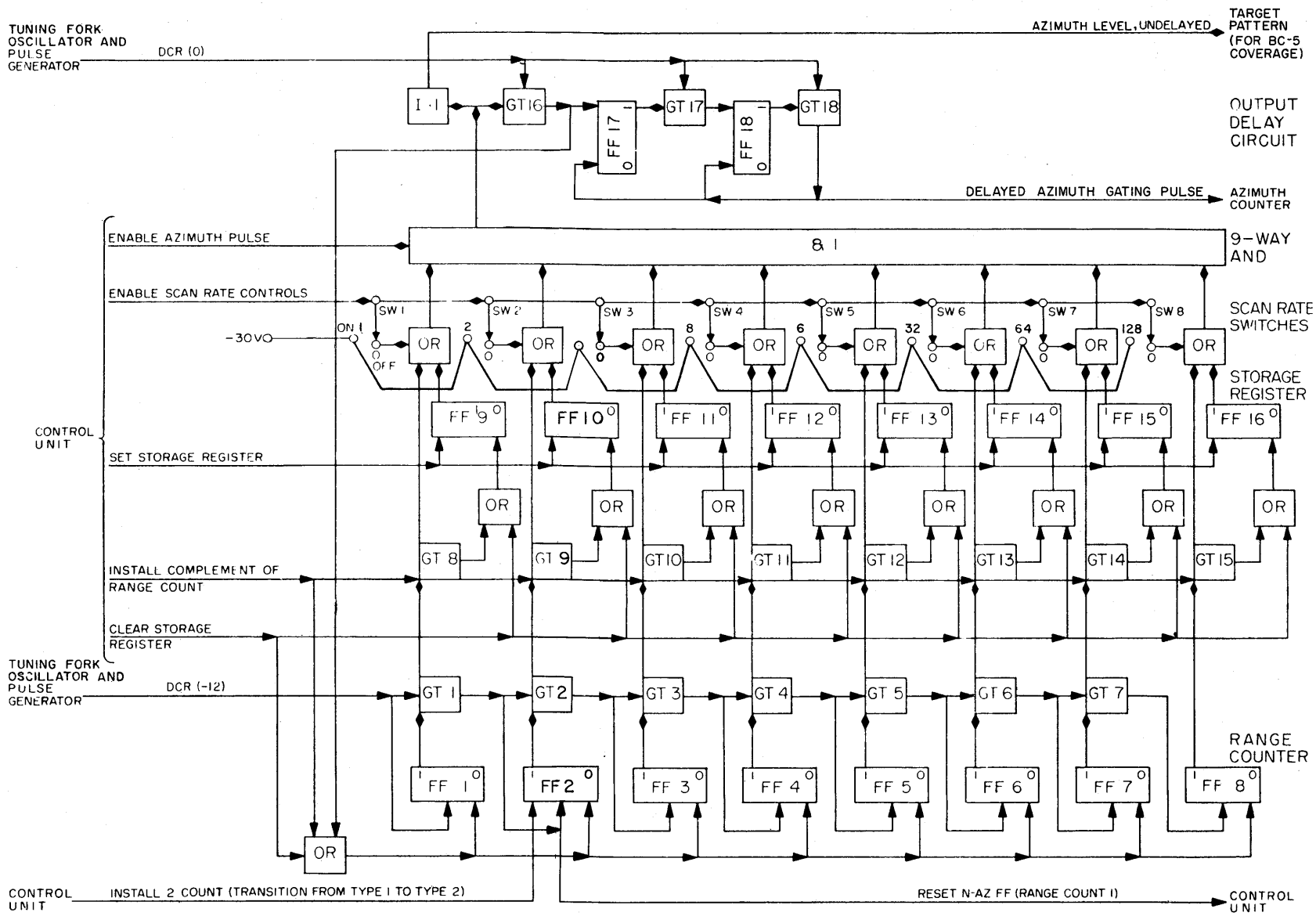


Figure 6–24. Range Counter and Storage Register, Simplified Logic Diagram

In computer type 1 operation, the range counter is cleared by *PER 65* pulses and maintains a range count between these pulses. This count is not significant in type 1 operation but will establish the length of the azimuth cycle in type 2 operation (4.11.3). No azimuth-gating pulses are produced in type 1 operation.

The transition from type 1 to type 2 is by means of a *PER 63* pulse, programmed to follow a *PER 65* pulse at north-azimuth or half-scan (128th azimuth) time. The *PER 63* pulse, gated through the control unit, installs a 2 count in the range counter. Advancing the initial count by a 2 co-ordinates the transition with the operation of the delay circuit, a feature explained in detail in 4.11.6. The counter is subsequently cleared by azimuth-gating pulses as in mode I operation.

Operation of the range counter in type 3 operation is the same as in mode I. However, in the event that type 1 operation is resumed, the first *PER 65* pulse clears the counter.

4.11.3 Storage Register

The storage register circuit consists of FF 9 through FF 16, GT 8 through GT 15, and eight OR circuits. In mode II type 1 operation, the complement of the contents of the range counter is installed in the storage register at azimuth time. These contents then determine the length of the azimuth cycle in the transition to type 2 operation. The logic operates as follows.

A *PER 65* pulse, gated through the control unit in type 1 operation, sets the storage register, preparing it for the following steps. The same pulse, delayed 12 μsec by SS 1 and PG 3 in the control unit, strobes GT 8 through GT 15 which are individually conditioned by the set side of the range counter flip-flops. The outputs of GT 8 through GT 15 are applied through OR circuits to the clear side of the storage register flip-flops. Thus, the *PER 65* pulse causes each set flip-flop in the range counter to clear a corresponding flip-flop in the storage register; i.e., installs the complement of the contents of the range counter in the storage register. (The 12-μsec delay referred to above ensures that the storage register is fully set before its new contents are installed.)

In mode II type 2 operation, *PER 65* pulses are blocked in the control unit; therefore, the storage register is not set and GT 8 through GT 15 are not strobed. The START pushbutton is not used; therefore, the storage register is not reset. Consequently, the contents installed in the storage register immediately before the transition from type 1 to type 2 operation remain available in type 2 for establishing the length of the azimuth cycle.

In mode I and mode II type 3 operation, the pulse triggered by the START pushbutton clears the storage registers. Gates 8 through 15 are not strobed, and the storage register remains clear, with no effect on operation.

4.11.4 AND Circuit

Nine +10V inputs are required to produce an output from the AND circuit, and thus an azimuth-gating pulse. The conditions under which this pulse occurs may be analyzed as follows:

a. One input to the AND is the enable-azimuth-gating-pulse level from the control unit. This level is not applied in mode II type 1 operation; therefore, the AND output can never be up in this type of operation. In all other types of operation, the level is applied, and inputs on the other eight lines can produce an output from the AND.

b. The other eight inputs are applied through OR circuits. Each input may originate in the set side of the range counter flip-flops, the set side of the storage register flip-flops, or through the scan rate switches (4.11.5).

c. In mode I and mode II type 3 operation, the scan rate controls and the contents of the range counter determine the inputs to the AND. When the levels applied by the scan rate controls complement the inputs from the range counter, the AND output is up.

d. In mode II type 2 operation, the scan rate controls are not enabled nor is the storage register cleared. The contents installed during mode II type 1 operation remain in the storage register and, together with the developing range count, determine the condition of the AND. When the range count complements the contents of the storage counter, the AND produces an output.

4.11.5 Scan Rate Switches

In mode I and mode II type 3 operation, the scan rate switches determine the length of the azimuth cycle. In these types of operation, a +10V enabling level is made available to the switches by the control unit. Each switch in the off position applies one +10V input to the AND circuit. In the on position, it applies a −30V input. Assume that a scan rate of 32 has been selected (by placing the scan rate 32 switch in the on position). A +10V input is then applied to the AND circuit on all switch lines except the scan rate 32 line. When the range count reaches 32, FF 6 in the counter is set, supplying the ninth input to the AND, and an azimuth-gating pulse is produced.

4.11.6 Output Delay Circuit

The output delay circuit comprises GT 16, GT 17, GT 18, FF 17, and FF 18.

The output of AND 1 conditions GT 16, which is strobed by a DCR (0) pulse, setting FF 17. The output of GT 16 also clears the range counter. The set side of FF 17 conditions GT 17, which is strobed by the next DCR (0) pulse, setting FF 18. The set side of FF 18 conditions GT 18, strobed by the following DCR (0) pulse to produce the azimuth-gating pulse. The output of GT 18 also resets FF's 17 and 18, concluding the azimuth cycle.

The effect of the above logic is to delay the azimuth-gating pulse by two cycles after the range counter is cleared. In other words, azimuth time is normally equivalent to range count 2 rather than range count zero. The delay is introduced to simplify the generation of BC 5 target coverage, described in 4.13.4. Other types of pattern generation make allowance for this delay in relating target-generation time to azimuth time.

In mode II type 1 operation, the range counter is cleared by the programmed azimuth-gating pulse. In this case, azimuth time is equivalent to range count zero rather than range count 2. This exception to the rule has no practical significance since targets are also programmed in type I operation and the proper relationship between target time and azimuth time is established by the Central Computer, not by the TPG target pattern circuitry. But when type 2 operation is initiated, the 2 cycle delay in azimuth time must be reinstalled to satisfy the requirements of the target pattern circuits. Therefore, the *PER 63* pulse responsible for the transition to type 2 operation is also used to install an initial 2 count in the range counter. In this way, the described relationship between range count and azimuth time is established during the first azimuth cycle following the transition. In subsequent azimuth cycles, the output delay circuit maintains this relationship in its normal fashion.

BC 5 coverage makes additional use of the output delay circuit by employing the inverted (by I 1) output of the AND circuit to suppress target generation at range counter zero time. This use is discussed in further detail in connection with BC 5 target coverage.

4.12 AZIMUTH COUNTER SECTION

4.12.1 General

The primary function of the azimuth counter (fig. 6–25) is to generate the north-azimuth-gating pulse. Normally, this pulse is produced every 256 azimuth cycles, but it may be advanced (early-north condition) or retarded (late-north condition) by means of manual switches and appropriate circuitry. In addition, the azimuth counter section controls certain features of the azimuth output signal by causing certain azimuth-gating pulses to be missed or spurious pulses to be inserted between normal ones.

The azimuth counter produces the north-azimuth-gating pulse by maintaining a count of the delayed azimuth-gating pulses. These pulses are produced by the range counter and storage register section in all types of operation except mode I type 1. The counter and, when utilized, early-north or late-north circuitry, supply inputs to a 9-way AND. When all inputs to the AND are up, a north-azimuth-gating pulse is produced. The missing azimuth and spurious azimuth circuitry also utilizes the count in the counter to control the generation of missing or spurious azimuth conditions.

In mode II type 1 operation, the azimuth counter section merely duplicates the programmed azimuth and north-azimuth signal and the missing or spurious azimuth circuitry is not operated; in short, the azimuth output signal is controlled by *PER 65* pulses from the Central Computer, not by the azimuth counter. However, the azimuth counter maintains a count of the *PER 65* pulses gated through the control unit; this count is maintained without interruption in the transition from one type of mode II operation to another. (But for this feature, the mappers would probably be thrown out of sync when changes from one type of operation to another were programmed.)

Operation of the various circuits is described on the logic level below. First, normal north-azimuth operation is described, followed by a description of early-north and late-north conditions. Then, missing and spurious azimuth conditions are discussed.

4.12.2 Normal North-Azimuth Operation

The north-azimuth pulse, programmed or non-programmed, clears the azimuth counter through OR 7. The counter is then stepped by the delayed azimuth-gating pulses or by programmed azimuth pulses. The flip-flops of the counter are sensed by AND 3 through OR 8 to OR 16. Flip-flop 9 is not involved in normal north-azimuth operation, since the count in the azimuth counter never exceeds 255. Instead, the LATEN-AZ switch, in the off position, applies a +10V level through OR 16. When the count in the counter reaches 255 (FF's 1 through 8 set), the output of AND 3 is up, conditioning GT 14. The following (256th) azimuth-gating pulse passes GT 14, setting FF 11, which conditions GT 13. This gate is strobed at the next range pulse (DCR (0)), producing the north-azimuth-gating pulse. This pulse is fed to the output signal generator where it gates through an azimuth bit in the usual manner. The bit occurs one range cycle after the 256th azimuth bit; together, these comprise the north-azimuth signal.

The north-azimuth-gating pulse is also fed back through OR 7 to clear the counter and to clear FF 11, deconditioning GT 13 until the north-azimuth cycle is complete.

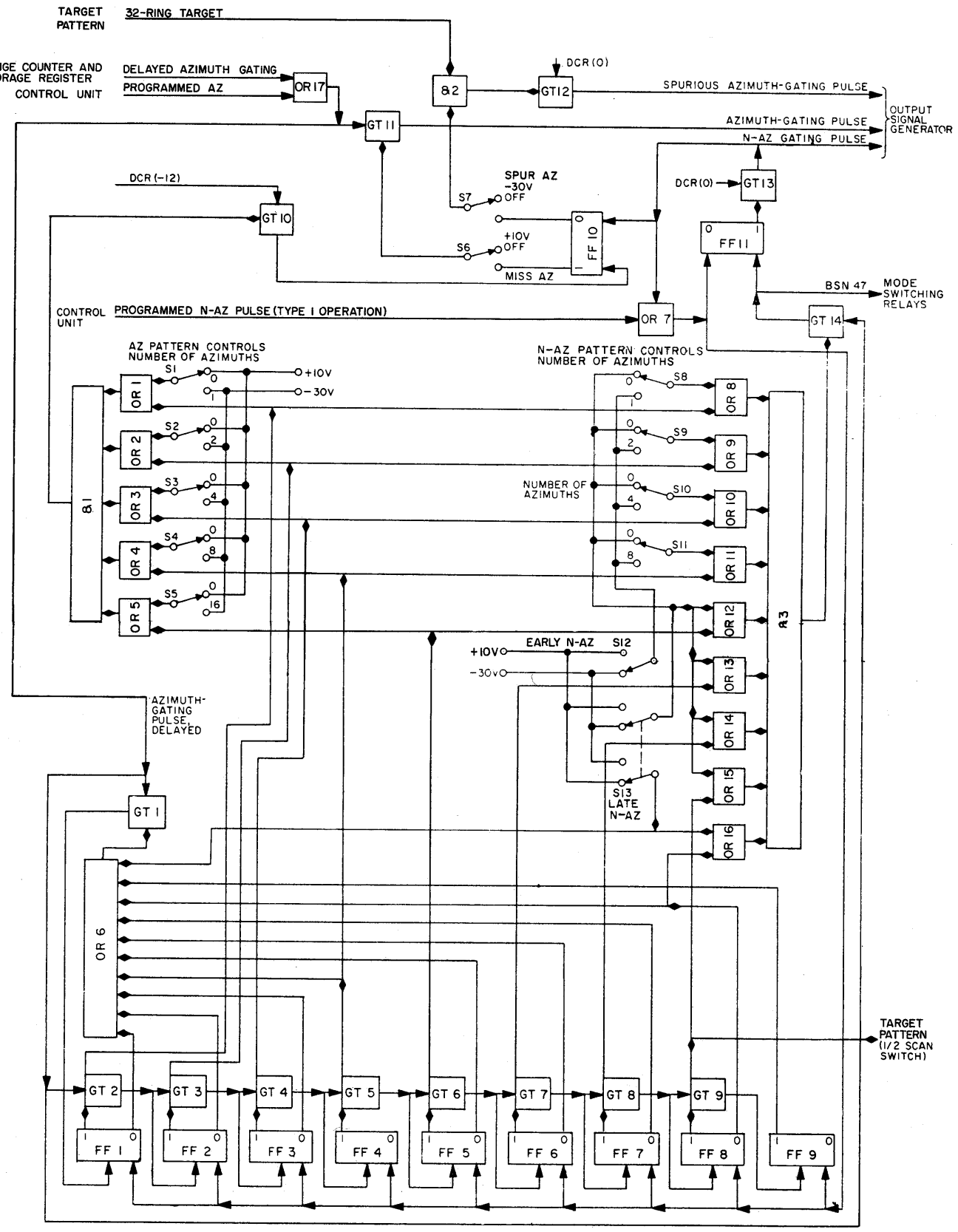


Figure 6–25. Azimuth Counter, Simplified Logic Diagram

4.12.3 Early-North Condition

The early-north condition is established by operating EARLYN-AZ switch S12 and setting the binary N-AZ PATTERN CONTROLS–NUMBER OF AZIMUTHS switches, S8 through S11, to the number of azimuths the north-azimuth signal is to be advanced. The operation is as follows.

The EARLY N-AZ switch provides a +10V enabling level to the S8 through S11 switches. Each operated switch furnishes a +10V input to AND 3, equivalent to a set condition in one of the first four flip-flops in the azimuth counter. When the switch settings complement the azimuth count, the AND output is up. For example, with the switches set to a binary five (by means of switches S8 and S10), the AND output is up at azimuth count 250 (FF 1, FF 3, FF 9 clear; all other flip-flops set). The north-azimuth-gating pulse is gated through GT 14 at the next (251st) azimuth pulse or five azimuth cycles early.

4.12.4 Late-North Condition

The late-north condition is established by operating LATE N-AZ switch S13 and setting the N-AZ PATTERN CONTROLS – NUMBER OF AZIMUTHS switches, S8 through S11, to the number of azimuths the north-azimuth signal is to be delayed. The LATE N-AZ switch then performs the following functions:

a. Applies +10V to OR 12 through OR 15
b. Applies +10V to the OFF bus of switches S8 through S11
c. Removes the +10V from OR 16; this input is then determined by the condition of FF 9.

Thus, four of the nine inputs (OR 12 through OR 15) required to bring up the output of AND 3 are always available. Four more inputs, OR 8 through OR 11, are determined by the condition of FF 1 through FF 4, by the setting of switches S8 through S11, or by a combination of the two. If a switch is off, or if the corresponding flip-flop is set, an input is available on that line. The ninth input is available when FF 9 is set. Normally, FF 9 is set when the count of 256 is reached. However, in late-north logic, the counter is stepped from the 247th count to the 249th, omitting the 248th. The count in the counter therefore leads the true azimuth count by one after the 247th azimuth, and FF 9 is set at a true azimuth count of 255.

The need for a skip is made evident by analyzing circuit operation when the LATE N-AZ switch is operated, but not the S8 through S11 switches. Under this circumstance, no delay in the north-azimuth gating pulse has actually been specified and the pulse should therefore occur at the normal (256th azimuth) time. The fact is, however, that the output of AND 3 would be up only when FF 9 in the counter was set, equivalent to a count of 256, and the north-azimuth-gating pulse would be produced at the 257th azimuth, or one azimuth pulse too late. By skipping the 248th count, FF 9 is set at the 255th count, as required.

The skip in the azimuth count is produced in the following manner. The azimuth-gating pulses which step the counter are gated through GT 1 by 10-input OR 6. Inspection of the logic shows an input to OR 6 at all times except when a count of 247 is found in the counter (all flip-flops except FF's 4 and 9 set). At this count, therefore, GT 1 is not conditioned. Accordingly, FF 1 is not cleared by the 248th azimuth pulse. The pulse rides through GT's 2, 3, and 4, clearing FF's 2 and 3, and setting FF 4, but is blocked at GT 5 because FF 4 has been clear. The 248th azimuth-gating pulse therefore sets all flip-flops except FF's 1 and 3, equivalent to a count of 249. The logic described above is summarized in table 6–1.

4.12.5 Missing Azimuth Operation

When the MISS AZ switch is operated, the AZ PATTERN CONTROLS–NUMBER OF AZIMUTHS switches, S1 through S5, determine the number of azimuth signals that are skipped following the north-azimuth signal. The missing azimuth circuitry comprises these switches, AND 1 with five OR inputs (OR 1 through OR 5), GT 10, GT 11, and FF 10. The logic operates as follows.

The delayed azimuth-gating pulses from the range counter and storage register are passed by GT 11 when this gate is conditioned. The gate is always conditioned (by +10V) when the MISS AZ switch is in the off posi-

TABLE 6–1. AZIMUTH COUNTER FLIP-FLOP CONDITIONS FOR COUNT SKIP

TRUE AZ COUNT	FF 1	FF 2	FF 3	FF 4	FF 5	FF 6	FF 7	FF 8	FF 9	COUNT IN COUNTER
247	1	1	1	0	1	1	1	1	0	247
248	1	0	0	1	1	1	1	1	0	249
249	0	1	0	1	1	1	1	1	0	250

tion. When the switch is operated, the condition of GT 11 is determined by the state of FF 10. This flip-flop is cleared by the north-azimuth-gating pulse and set by DCR (-12) after the output of AND 1 has been brought up. The output of AND 1 is up when the azimuth count equals the binary number set into switches S1 through S5. For example, if the switches are set to six in binary (by S2 and S3), the output of AND 1 is up when the azimuth count reaches six (FF's 2 and 3 set). Until then, GT 11 is not conditioned and consequently does not pass the first six azimuth gating pulses following north-azimuth.

4.12.6 Spurious Azimuth Operation

When the SPUR AZ switch is operated, the AZ PATTERN CONTROLS–NUMBER OF AZIMUTHS switches determine the number of azimuth signals after north-azimuth which will be followed, at the 32nd range cycle, by a spurious azimuth signal. The spurious azimuth circuitry consists of these switches, FF 10, AND 2, and GT 12. It also takes advantage of circuits in the target pattern control section to determine the 32nd range cycle of the azimuth cycle. The logic operates as follows.

When conditioned, GT 12 passes DCR (0) pulses as spurious azimuth-gating pulses. The condition of GT 12 is determined by the output of AND 2. With the SPUR AZ switch off, this output is always down; therefore, no spurious azimuth signals can ever be produced under this circumstance. When the SPUR AZ switch is operated, the clear side of FF 10 is connected to AND 2. The second input to AND 2 is supplied by the target pattern control circuitry at the 32nd range cycle of every azimuth cycle. Thus, whenever FF 10 is clear at the 32nd range cycle of an azimuth cycle, a spurious azimuth-gating pulse is produced.

The operation of FF 10 has been described in connection with missing azimuth circuitry (4.12.5). Flip-flop 10 is cleared by the north-azimuth-gating pulse and remains clear until the first DCR (-12) after the output of AND 1 has been brought up. The condition of AND 1, in turn, is determined by the developing azimuth count and by the setting of the NUMBER OF AZIMUTHS switches. For example, if the NUMBER OF AZIMUTHS switches are set to 6 in binary, the output of AND 1 is down (GT 10 is deconditioned and FF 10 clear) until the count in the azimuth counter reaches 6. At the 32nd range cycle of each of these six azimuth cycles, the output of AND 2 will be up, and a spurious azimuth-gating pulse will be passed by GT 12 to the output signal generator. There, it will gate through a corresponding spurious azimuth signal bit.

4.13 TARGET PATTERN GENERATION

4.13.1 General

The target pattern section generates (in all types of operation except mode II type 1) the pattern of target-gating pulses specified by the TARGET PATTERN CONTROLS switches. These pulses are fed to the output signal generator where they gate through a corresponding pattern of target bits.

The target pattern section (fig. 6–26) consists of the TARGET PATTERN CONTROLS switches, various AND and OR circuits, which, in combination, sense the range counter for the count required to generate a specific target pattern, OR 6, AND 6, and GT 1. The logic in the several types of pattern generation is described below.

AND 6 is the key logic block. When all inputs to AND 6 are up, GT 1 is conditioned, passing a target-gating pulse at DCR (0) to the output signal generator. Four inputs are required to bring up the AND output:

a. An enabling level: furnished by the control unit in all types of operation except mode II type 1. (The level is produced by a *PER 63* pulse or by use of the START pushbutton.)

b. A level furnished by the 1/2 SCAN target switch. This level is available at all times when the switch is off but only during the second half of the north-azimuth cycle (128th through 255th azimuth cycles) when the switch has been operated (refer to 4.13.5).

c. A level furnished through the BC 1 switch. This level is available at all times when the BC 1 switch has been operated and at all times except range count zero time when the switch is off.

d. An input through OR 6. This input, in turn, is fed through one of six TARGET PATTERN CONTROLS switches: 32, 48, 62, 64, BC 5, or BC 1.

Assume that inputs a, b, and c, above, are available. The AND 6 output is up whenever the target pattern circuitry furnishes an input through OR 6. Generation of the ring target pattern will be discussed first, followed by an explanation of BC 1 and BC 5 target coverage.

4.13.2 Ring Target Patterns

Ring or circular target patterns are those generated at the 32, 48, 62, or 64 range cycle of each azimuth cycle and are so called because they form a ring on a PPI type of display (such as the one provided by the mappers). To generate such a target pattern, a unique combination of AND and OR circuits senses the range counter, providing an input to OR 6 when the proper count is reached. This count will be two higher than the target pattern number to compensate for the two range cycles by which the azimuth-gating pulse is delayed in the output delay circuit (4.11.6). For example, to produce the 32 pattern, AND 4 senses the range counter (directly and through I 1 and OR 4) for a count of 34. This count is expressed by the following condition of

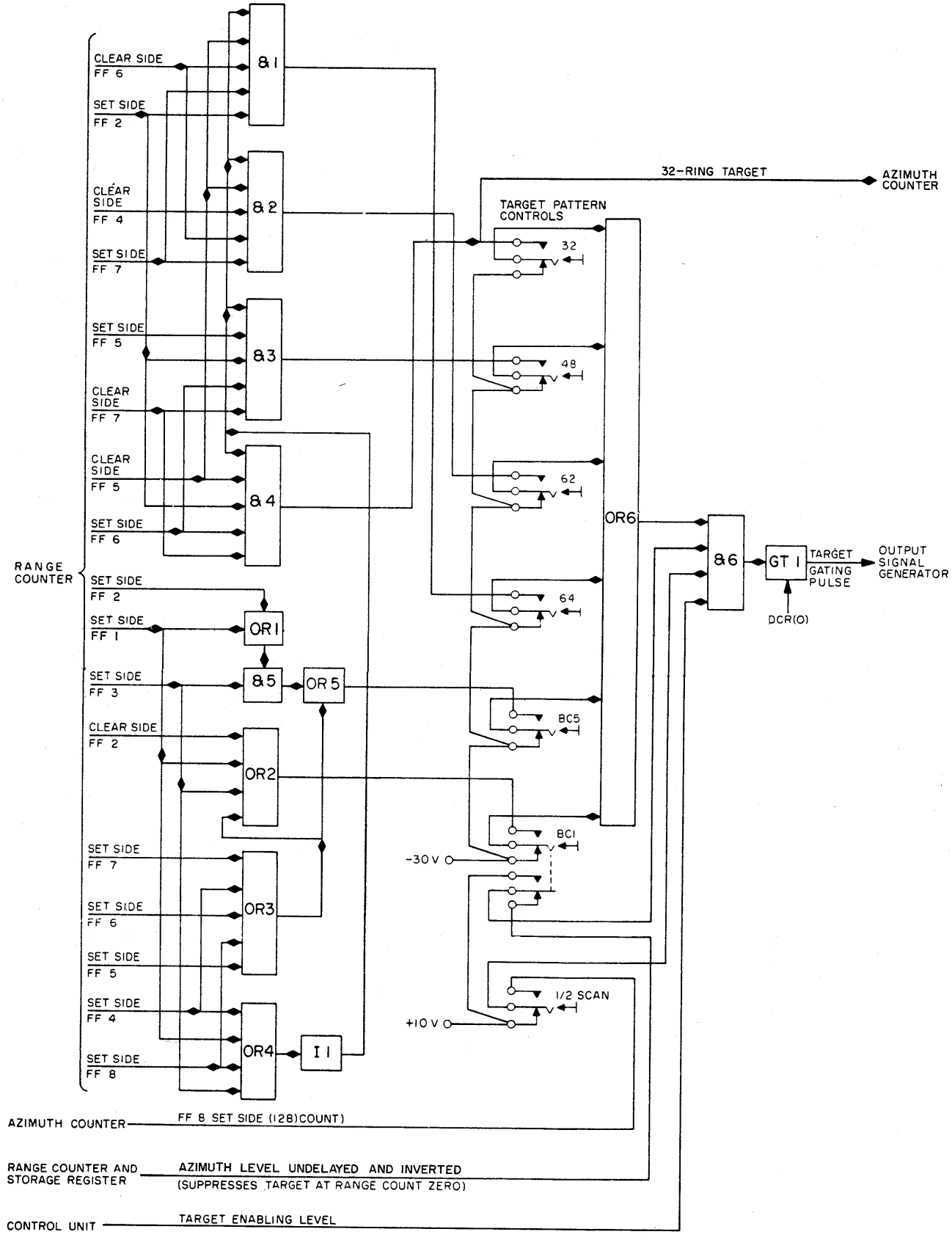


Figure 6–26. Target Pattern, Simplified Logic Diagram

the range counter: FF 2 and FF 6 set; all other flip-flops clear. The effect of this condition is to bring up the output of AND 4 for the following reasons:

a. There is no input to OR 4 since FF's 1, 3, 4, and 8 are clear; therefore, I 1 provides an input to AND 4.
b. The other four inputs required to bring up the output of AND 4 are also present since FF's 2 and 6 are set and FF's 5 and 7 are clear.

If the 32 TARGET PATTERN CONTROLS switch has been operated, the output of AND 4 is applied through OR 6 to AND 6. At range count 34, the output of AND 6 is up, and a target-gating pulse passes GT 1 at DCR (0) time. This pulse is fed to the output signal generator as a corresponding target-gating pulse 32 range cycles after the previous delayed azimuth-gating pulse.

Note

The circuitry for generating the 32 pattern is also utilized for spurious azimuth generation (4.12.6) since spurious azimuths are produced at the 32nd range cycle following the normal azimuth signal.

The other ring patterns are similarly generated by AND and OR combinations which sense the range counter for appropriate counts, in each case two more than the target pattern number; specifically, AND 1 senses for a 66 count, AND 2, for a 64 count, and AND 3, for a 50 count.

Any combination of the four available ring patterns may be generated at the same time. However, the length of the azimuth cycle must be long enough to accommodate the pattern. For example, to generate the 32 target pattern, the length of the azimuth cycle must exceed 34 range cycles. (If it equalled 34, I 1 in the range counter and storage register would have a negative output when the range count reached 34 and the output of AND 6 would not be up at that count.)

4.13.3 BC 1 Coverage

The BC 1 target pattern provides a target during every range cycle except the one coincident with the azimuth signal. The pattern is generated by operating the BC 1 switch. One pole of this dpdt switch then applies +10V continuously to AND 6. The other pole connects OR 2 to OR 6. Sensing the range counter directly or through OR 3, OR 2 provides an input to OR 6 (and to AND 6) for all range counts except 2 (FF 2 set; all other flip-flops clear). Range count 2 is equivalent to azimuth time because of the 2-count by which the azimuth-gating pulse is delayed (4.11.6). Consequently, two of the four inputs required to bring up the output of AND 6 are available at all times except azimuth time. When the other two inputs are made available (by the 1/2 SCAN switch and the control unit), target-gating pulses are generated.

4.13.4 BC 5 Coverage

The BC 5 target pattern provides a target during every range cycle except the two before, the two after, and one coincident with the azimuth signal. The pattern is generated by operating the BC 5 switch. Target-gating pulses are then generated at all range counts except five: 0 (range counter being cleared), 1, 2, 3, and 4. Because the azimuth-gating pulse is delayed two cycles with respect to the range counter, range count 0 through 4 is equivalent to two cycles before, two cycles after, and the cycle coincident with the azimuth-gating pulse. The logic operates as follows.

The BC 5 switch in the on position connects OR 5 to OR 6. Examination of the logic shows an input to OR 5 for all range counts except 1 through 4. Specifically, OR 3 provides an input to OR 6 when any of the last five flip-flops in the range counter are set (range counts 8 through 255) and AND 5 provides an input to OR 5 at count 5, 6, or 7. Since no input to OR 5 is provided by range counts 1 through 4, the output of AND 6 cannot be up during these counts. Consequently, no targets are generated by these counts.

Suppression of a target-gating pulse at 0 range count is performed by I 1 in the range counter and storage register. This suppression is necessary because GT 1 is strobed at the same time that the range counter is reset (DCR (0)) and an overlap might cause GT 1 to pass a target-gating pulse at this time.

4.13.5 ½ SCAN Target Pattern

When the 1/2 SCAN switch is operated, targets may be generated only during the second half of the north-azimuth cycle (azimuth count 128 through 255). Such a pattern assists in detecting spurious target indications generated by the GFI equipment.

The 1/2 SCAN circuit functions as follows. In the off position, the 1/2 SCAN switch applies +10V continuously to AND 6, permitting target generation throughout the north-azimuth cycle. In the on position, it applies this enabling level to AND 6 only when FF 8 in the azimuth counter is set; i.e., equivalent to an azimuth count of 128 through 255.

4.14 DUPLEX SWITCHING

Duplex switching consists of relays 92BF(K2) and 92BG(K1). When the A computer is in the standby status, relay 92BF(K2) is energized; command pulses from the A computer are made available to the TPG, and *BSN 34* and *BSN 47* pulses, if generated, are transferred to the A computer. When the B computer is in the standby status, relay 92BG(K1) is energized and similarly associates the B computer with the TPG.

PART 7
INPUT SYSTEM OF THE AN/FSQ-8 COMBAT CONTROL CENTRAL

CHAPTER 1
GENERAL

1.1 COMPARISON OF AN/FSQ-7 COMBAT DIRECTION CENTRAL AND AN/FSQ-8 COMBAT CONTROL CENTRAL

Operationally, the AN/FSQ-8 installation (refer to 1.2 below) and the AN/FSQ-7 installation are distinctly different. Functionally, however, they have great similarities. In fact, in this respect, the Combat Control Central may be regarded as the core of a Combat Direction Central. Since the Input System of the Direction Central is essentially peripheral, it is not surprising that only a small part of it (refer to 1.3 below) is retained in the Control Central.

1.2 PURPOSE OF AN/FSQ-8 COMBAT CONTROL CENTRAL

The AN/FSQ-8 Combat Control Central is assigned air-defense responsibility on the division level. Like the AN/FSQ-7 Combat Direction Central, it is a data-processing system of the high-speed, electronic, digital computer type. Its function is to develop information needed to analyze the air situation within the sector and to allocate weapons properly to meet the threat of hostile action. To perform this function, it processes summarized data received in binary form from Combat Direction Centrals associated with it and from other sources. The Combat Control Central also monitors the activities of associated Direction Centrals and transmits intelligence and command information to them. Additional functions of the Combat Control Central are to exchange information with adjacent Combat Control Centrals, order conditions of alert for its sector, and disseminate defense warnings to civilian and military agencies. Finally, the Combat Control Central implements prearranged defense measures and forward-tells summary data to the next higher echelon (Control Operations Center).

1.3 INPUT SYSTEM OF AN/FSQ-8 COMBAT CONTROL CENTRAL

Since operational input data to the Combat Control Central originates only in other Centrals, the XTL element, alone, suffices as an Input System (fig. 7–1). The XTL portion of the TPG is retained to assist in the maintenance of the XTL element. The functions of simplex maintenance console unit 47 are greatly reduced and the unit physically reflects this change.

The next chapter considers the Input System and the simplex maintenance console of the Combat Control Central in further detail.

The Input System equipments in the Control Central are similar, when not identical, to their equivalents in the Direction Central. To avoid redundancy, only the differences are described. For a detailed theory of operation, refer to the description of the equivalent equipment in the AN/FSQ-7 Combat Direction Central presented in previous parts of this manual.

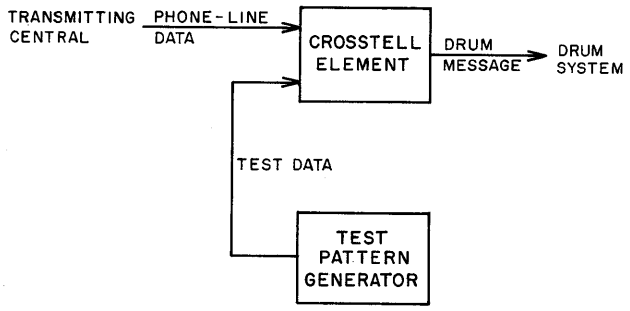


Figure 7–1. Input System of AN/FSQ-8 Combat Control Central, Block Diagram

CHAPTER 2

DIFFERENCES BETWEEN INPUT SYSTEM EQUIPMENTS OF AN/FSQ-8 COMBAT CONTROL CENTRAL AND AN/FSQ-7 COMBAT DIRECTION CENTRAL

2.1 XTL ELEMENT

The XTL element employed in the AN/FSQ-8 Combat Control Central is the 12-channel XTL element found in certain AN/FSQ-7 installations providing a maximum of 11 active and 1 spare channel. For details, refer to the discussion of the 12-channel XTL element in Part 5.

2.2 TEST PATTERN GENERATOR

The TPG, unit 92 (fig. 7–2), is composed of module A (the XTL TPG module) and module Z (the utility module) of Test Pattern Generator TS-923/FSQ. Modules B and C of this unit are not supplied since they service LRI and GFI elements.

The XTL TPG operates in the same manner as this equipment in the Direction Central.

2.3 SIMPLEX MAINTENANCE CONSOLE

Simplex Maintenance Console 0A-1518/FSQ, unit 47, (fig. 7–3) in the AN/FSQ-8 Combat Control Central is essentially a modification of Simplex Maintenance Console 0A-1010/FSQ, unit 47, in the AN/FSQ-7 Combat Direction Central; it is formed by substituting blank panels for control panels associated with equipment unique to AN/FSQ-7 installation. The resulting unit mounts the XTL TPG control panel in module B; six XTL control panels (for channels 7 through 12) in module C; six XTL control panels (for channels 1 through 6) in module D; one telephone (intercommunication) panel in module E; one computer entry punch panel and two power supply panels in module H; an MC control panel on module J; and centralized scope and probe facilities (under development) in module K. All other panels are blank.

The function of control panels is the same as that of the equivalent control panels in the AN/FSQ-7, unit 47.

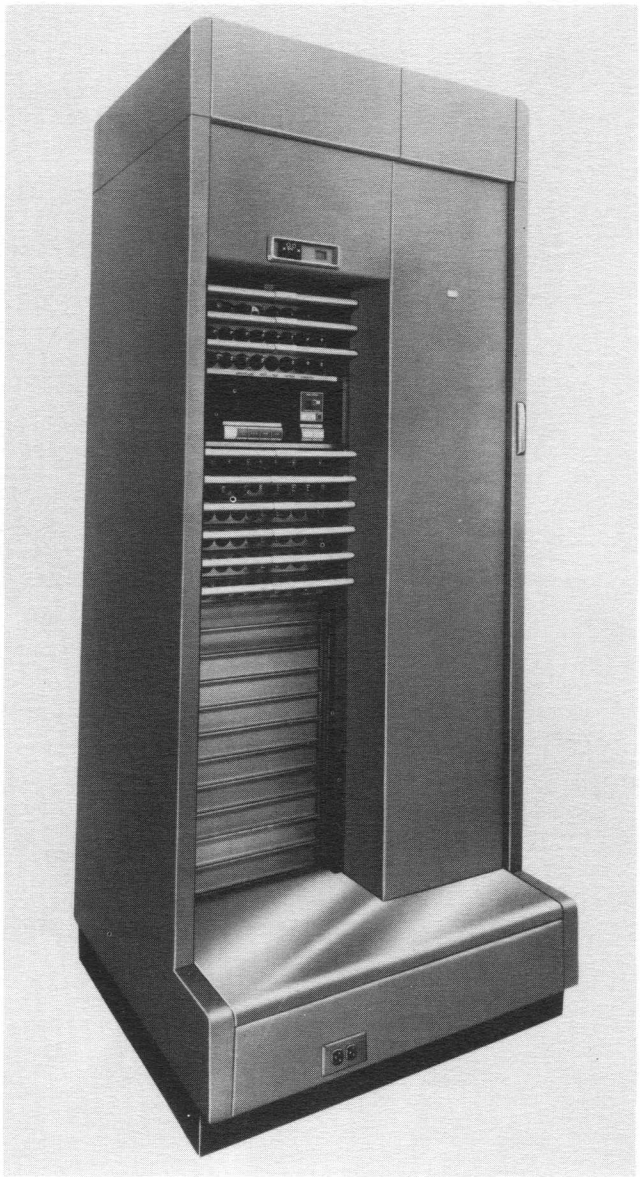


Figure 7–2. Test Pattern Generator, AN/FSQ-8 Combat Control Central

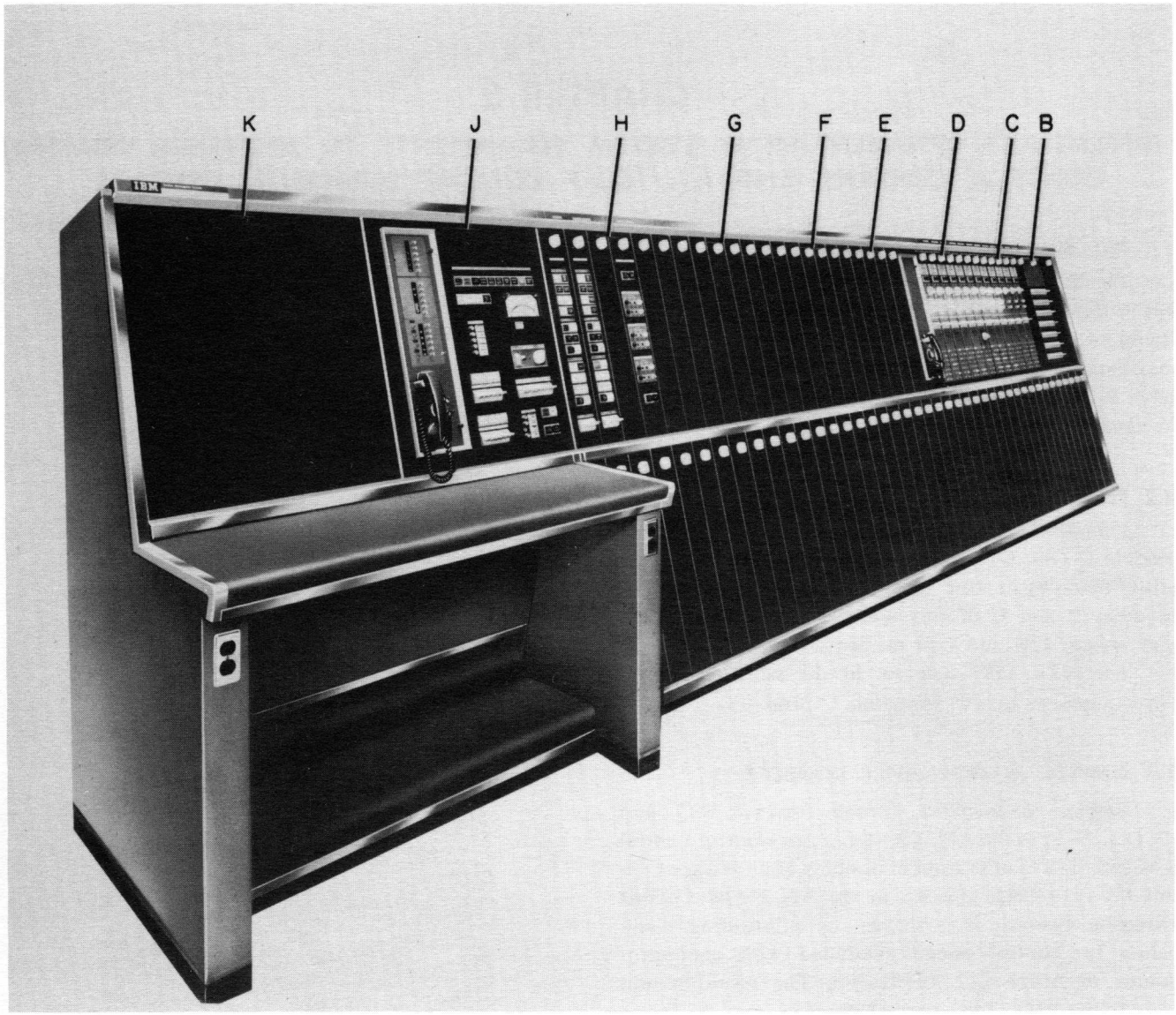
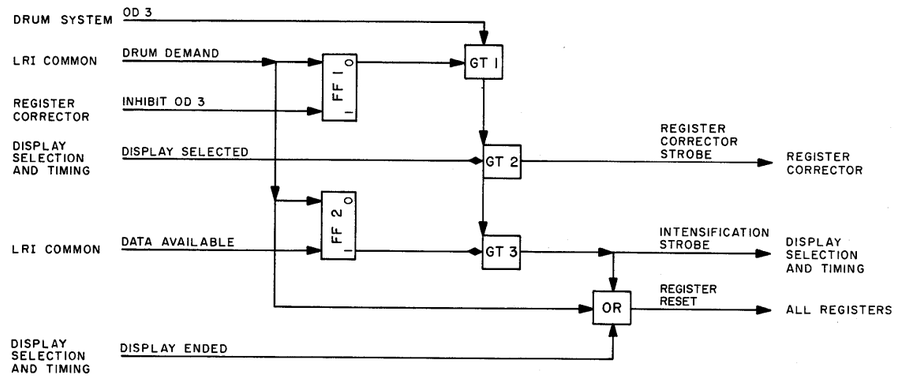
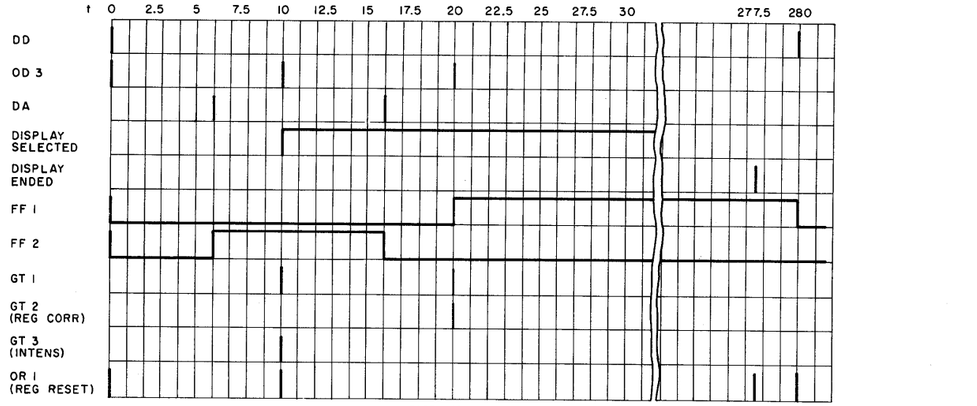


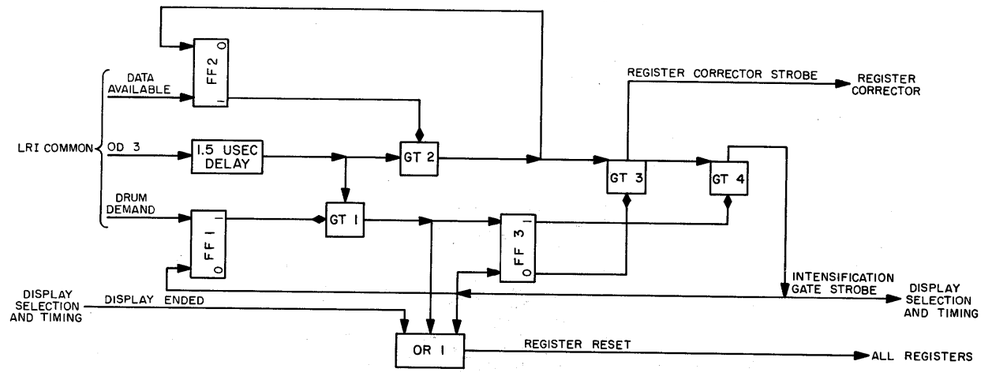
Figure 7–3. Simplex Maintenance Console OA-1518/FSQ

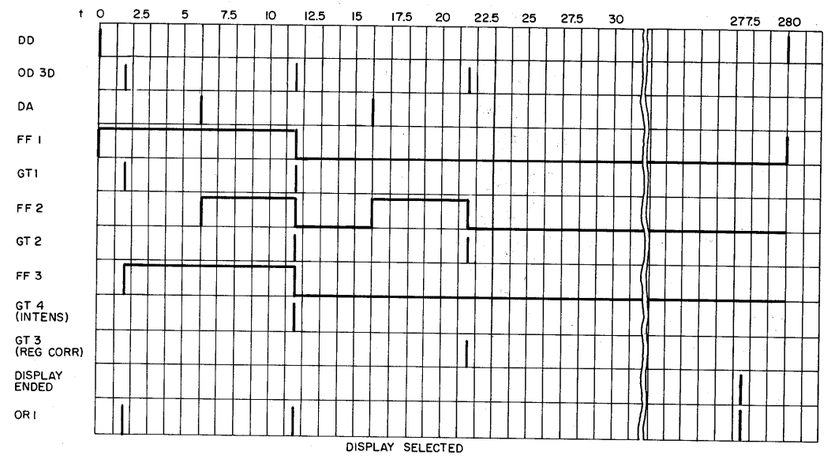


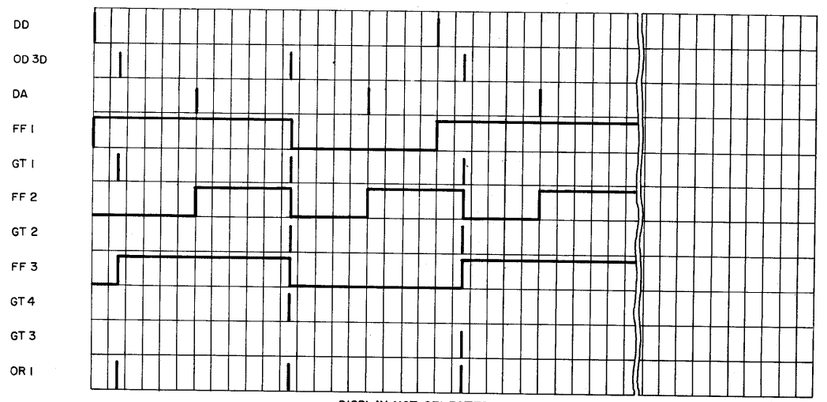


NOTE:
FF 1 ALWAYS CLEAR NO OUTPUT FROM GT 2

A. SYSTEM 17 AND BEYOND







B. SYSTEMS 1 THROUGH 16

Figure 3–18. Word Discriminator, Simplified Logic and Timing Diagrams

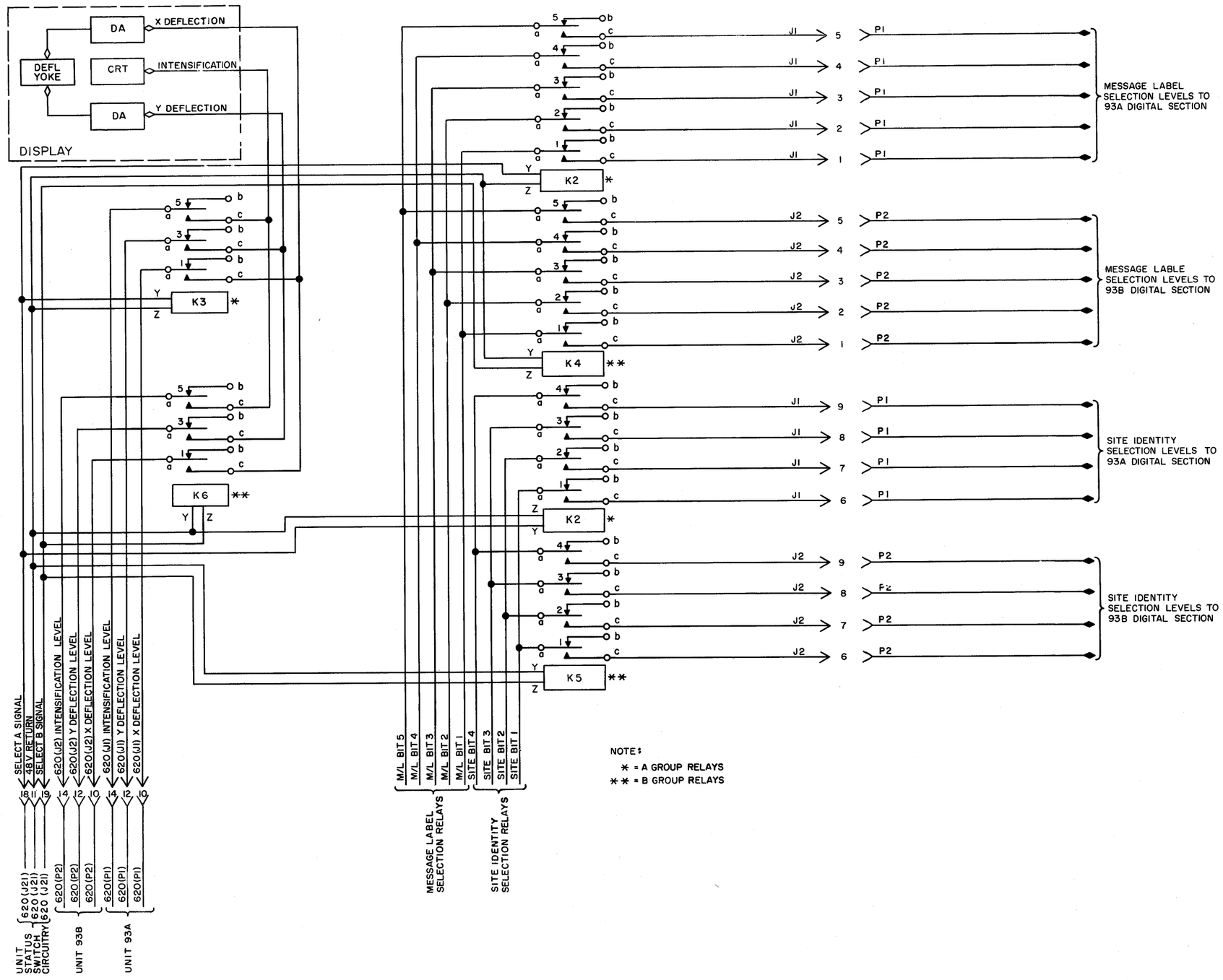
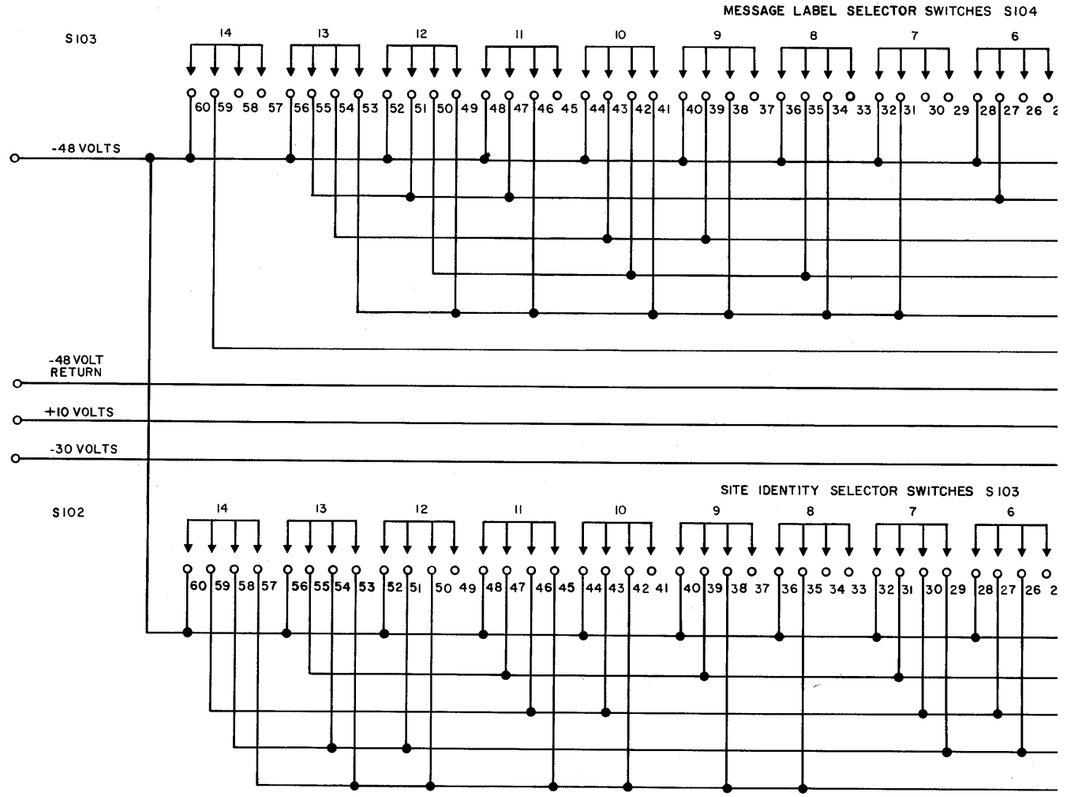


Figure 3–27. Signal Application Control Relay, Circuit Diagram


MESSAGE LABEL SELECTOR SWITCHES S104
S103
14
13
12
11
10
9
8
7
6
60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27 26
-48 VOLTS
-48 VOLT RETURN
+10 VOLTS
-30 VOLTS
S102
SITE IDENTITY SELECTOR SWITCHES S103
14
13
12
11
10
9
8
7
6
60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27 26

NOTE: CIRCUITRY SHOWN IS FOR UNIT 620. TO MAKE CIRCUITRY APPLICABLE TO OTHER CONSOLES–
UNIT 621: SUBSTITUTE FIGURE 3-29 FOR CIRCUITRY TO RIGHT OF DOTTED LINE
UNIT 622 AND 623: MESSAGE LABEL AND SITE IDENTITY PUSHBUTTONS ARE LOCATED DIRECTLY ON CONSOLES AND CONNECTIONS ARE DIRECTLY TO P3; OTHERWISE CIRCUITRY IS AS INDICATED

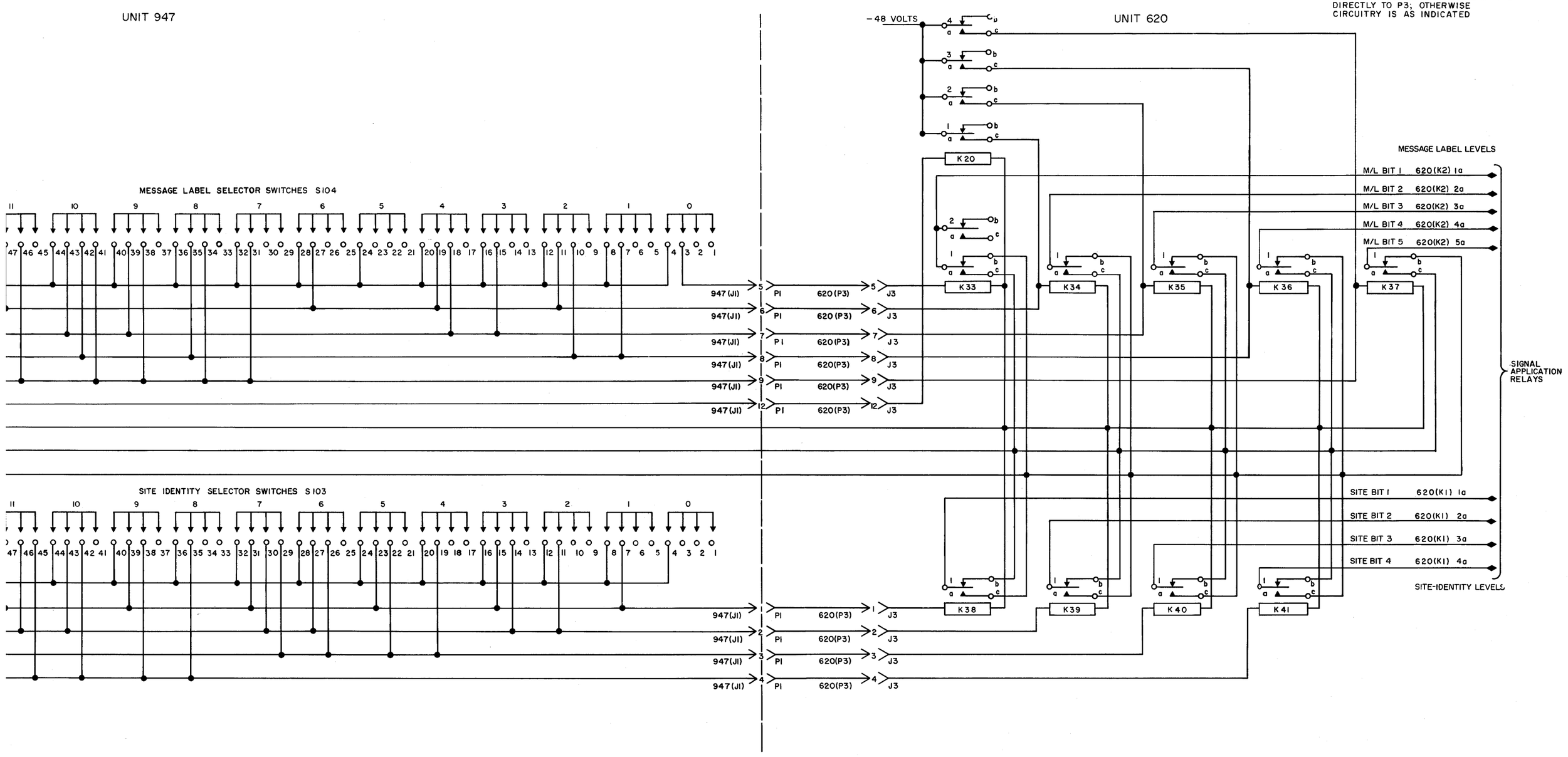
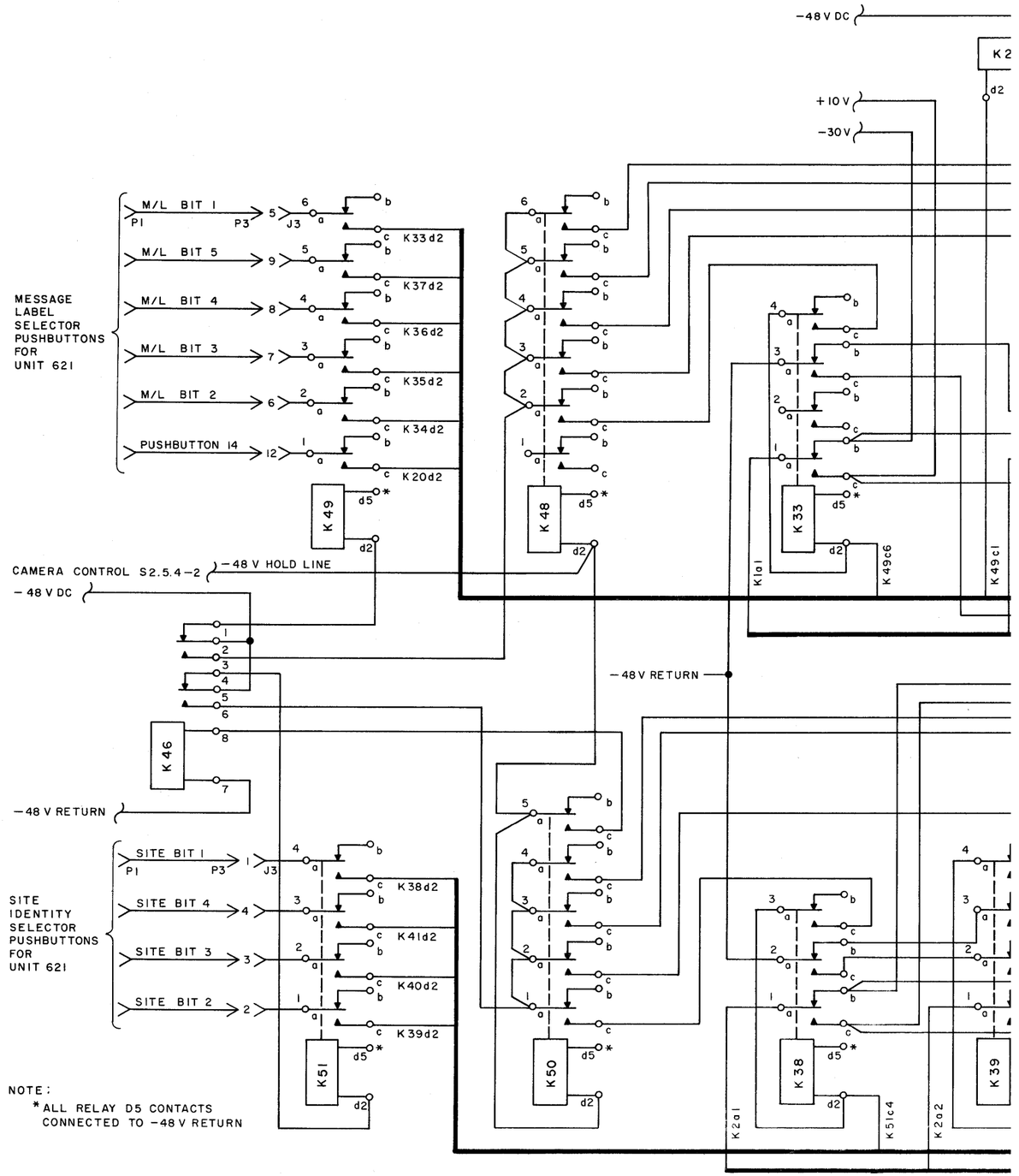


Figure 3–28. Site and Message Label Selector Switch and Relay, Circuit Diagram


-48 V DC
+10 V
-30 V
MESSAGE LABEL SELECTOR PUSHBUTTONS FOR UNIT 621
M/L BIT 1
M/L BIT 5
M/L BIT 4
M/L BIT 3
M/L BIT 2
PUSHBUTTON 14
P1
P3
J3
K33d2
K37d2
K36d2
K35d2
K34d2
K20d2
K49
K48
K33
K1a1
K49c6
K49c1
CAMERA CONTROL S2.5.4-2
-48 V HOLD LINE
-48 V DC
K46
-48 V RETURN
SITE IDENTITY SELECTOR PUSHBUTTONS FOR UNIT 621
SITE BIT 1
SITE BIT 4
SITE BIT 3
SITE BIT 2
K38d2
K41d2
K40d2
K39d2
K51
K50
K38
K39
K2a1
K51c4
K2a2
NOTE:
*ALL RELAY D5 CONTACTS CONNECTED TO -48 V RETURN

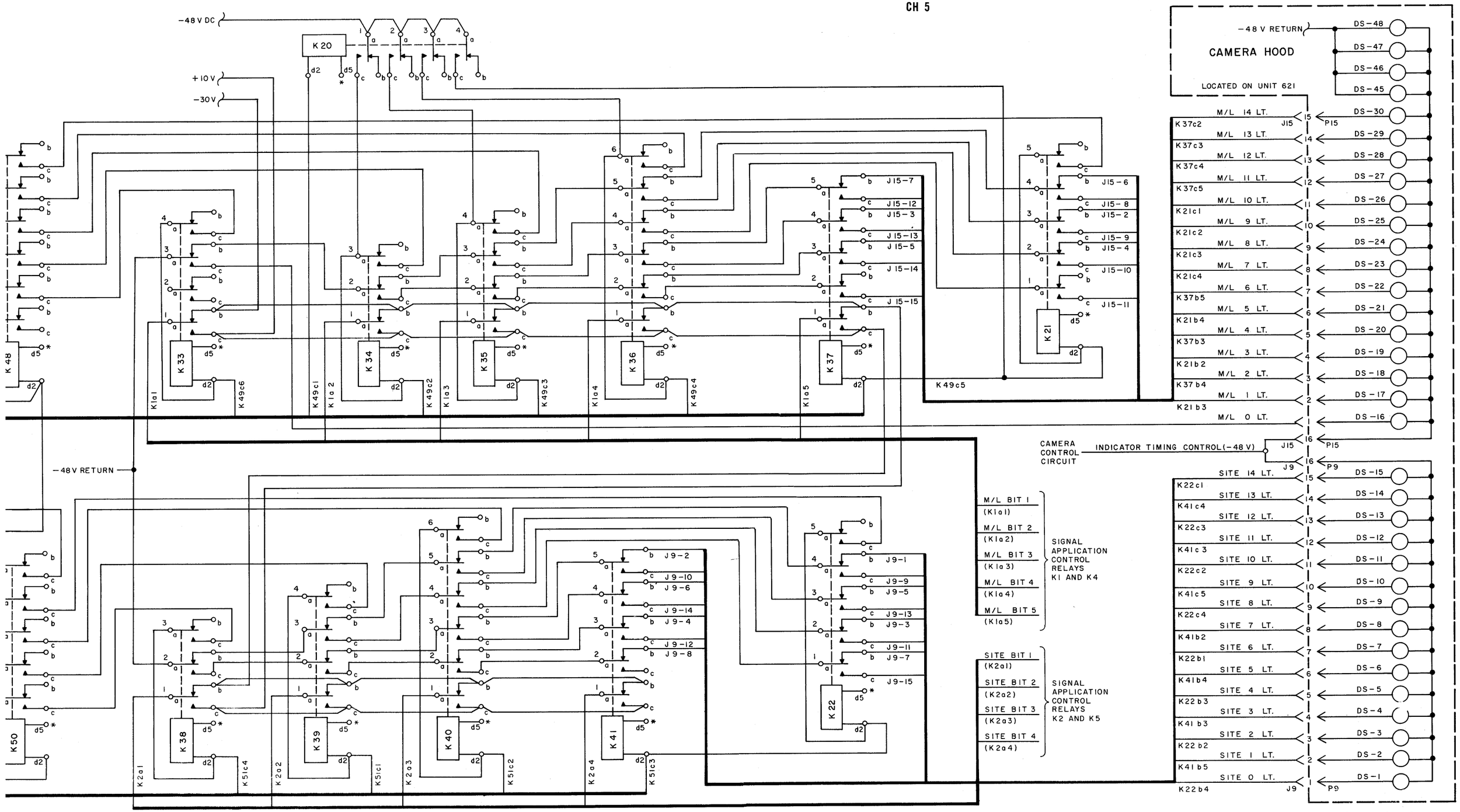
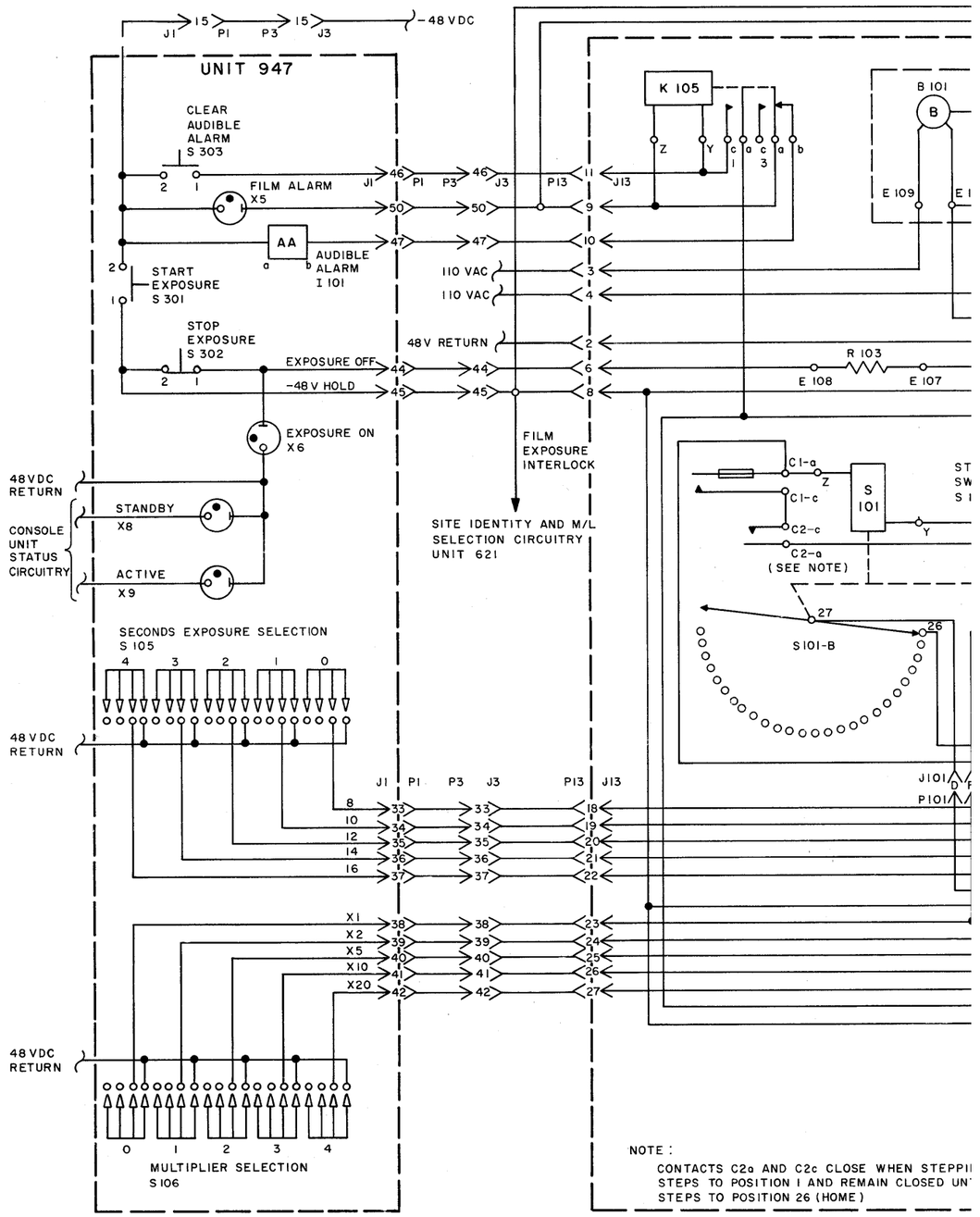


Figure 3–29. Camera Console Unit, Site and Message Label Selection Relay and Indicator Lamp, Circuit Diagram


J1
15
P1
P3
15
J3
-48 VDC
UNIT 947
CLEAR AUDIBLE ALARM S 303
FILM ALARM X5
AA
AUDIBLE ALARM I 101
START EXPOSURE S 301
STOP EXPOSURE S 302
EXPOSURE OFF
-48 V HOLD
EXPOSURE ON X6
48VDC RETURN
CONSOLE UNIT STATUS CIRCUITRY
STANDBY X8
ACTIVE X9
SECONDS EXPOSURE SELECTION S 105
48 VDC RETURN
MULTIPLIER SELECTION S 106
X1
X2
X5
X10
X20
K 105
B 101
110 VAC
110 VAC
48V RETURN
R 103
E 108
E 107
E 109
FILM EXPOSURE INTERLOCK
SITE IDENTITY AND M/L SELECTION CIRCUITRY UNIT 621
S 101
S101-B
(SEE NOTE)
J101
P101
NOTE :
CONTACTS C2a AND C2c CLOSE WHEN STEPPI
STEPS TO POSITION 1 AND REMAIN CLOSED UN
STEPS TO POSITION 26 (HOME)

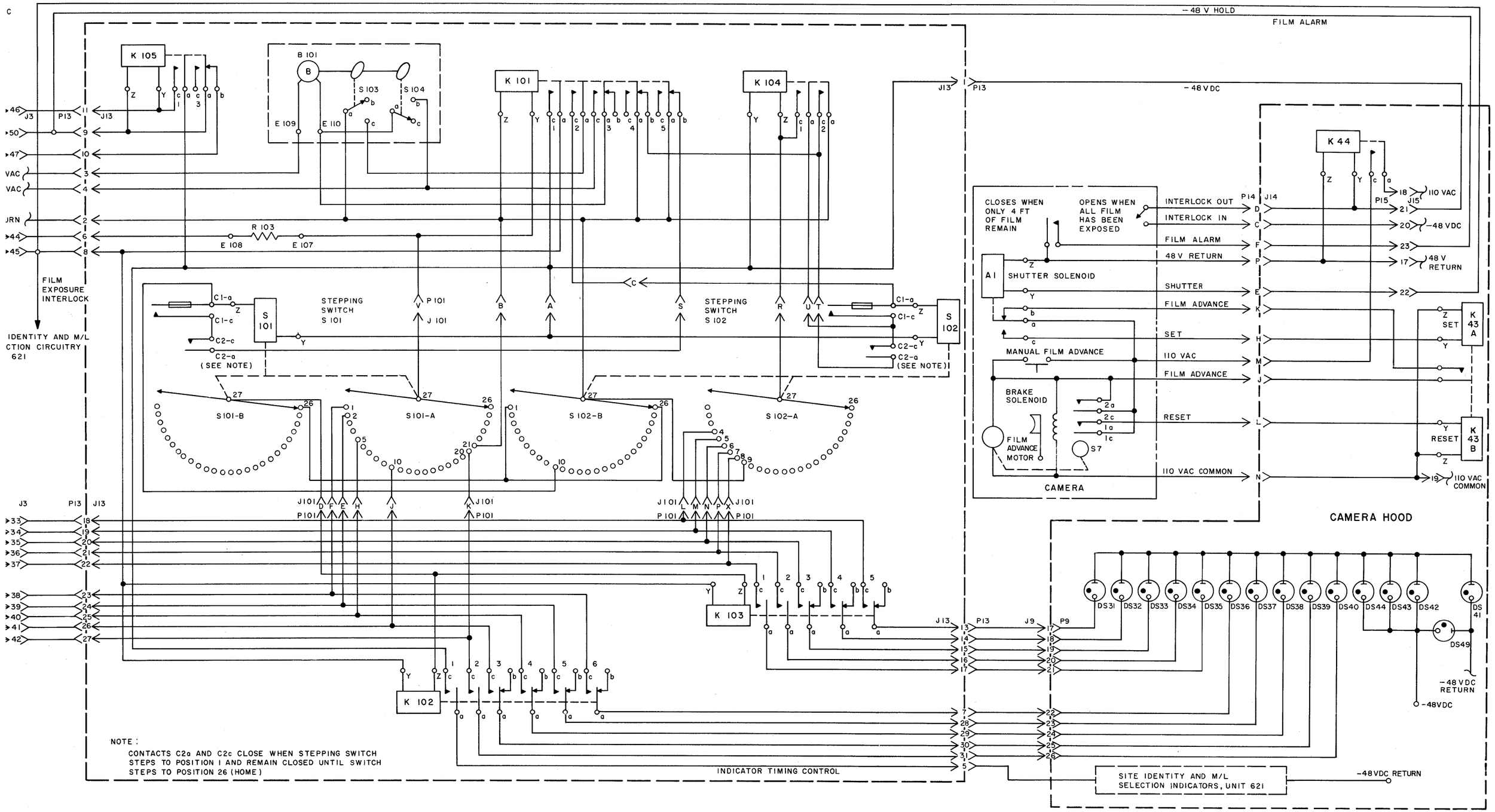


Figure 3–30. Camera Control, Circuit Diagram

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