HP 13255

CONTROL MEMORY W/ DUAL BANK SELECT MODULE

Manual Part No. 13255-91243

REVISED

JUN-10-80

HEWLETT PACKARD

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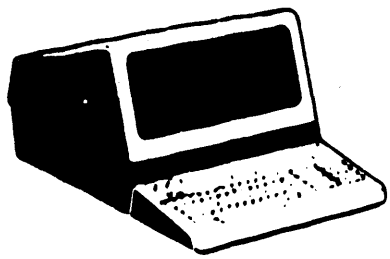
NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

DATA TERMINAL
TECHNICAL INFORMATION



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1.0 INTRODUCTION.

The Control Memory w/ Dual Bank Sel. Module provides 1K bytes of RAM and up to 96K bytes of ROM, organized in 2 selectable 48K banks. The module communicates with the processor over a top plane bus, thus allowing the processor to operate at its maximum rate by eliminating the bus contention and handshake protocol of the bottom plane bus.

The ROMs contain the operating firmware for the terminal. The RAM provides for a fast access scratchpad for stack operations and program variables.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Control Memory w/ Dual Bank Sel. Module is contained in tables 1.0 through 5.1.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60243	ROM Control Memory PCA	12.9 x 4.0 x 0.5	0.56

Number of Backplane Slots Required: 1

Table 2.0 Reliability and Environmental Information

Environmental:	(X) HP Class B ( ) Other:
Restrictions:	Type tested at product level
Failure Rate:	0.8537 (percent per 1000 hours) 2.8121 (with 12 ROMs loaded on PCA)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	+42 Volt Supply
0.580 mA	0 mA	0 mA	0 mA
	NOT APPLICABLE	NOT APPLICABLE	NOT APPLICABLE

115 volts ac	220 volts ac
0 A	0 A
NOT APPLICABLE	NOT APPLICABLE

Clock Frequency: MHz

NOT APPLICABLE

Table 4.0 Switch Definitions

PCA Designation	Function	
	CLOSE	OPEN
ROM ENABLE (RM) (1,2,3,....12)	The corresponding 8 block of ROM is enabled.	The corresponding 8 block of ROM is disabled.
BS0	Bank 0 responds to BANK SEL. line equal to a '0'.	Bank 0 responds to BANK SEL. line equal to a '1'.
DS0	Bank 0 responds to DISB. ROM line equal to a '0'.	Bank 0 responds to DISB. ROM line equal to a '1'.
BS1	Bank 1 responds to BANK SEL. line equal to a '0'.	Bank 1 responds to BANK SEL. line equal to a '1'.
DS1	Bank 1 responds to DISB. ROM line equal to a '0'.	Bank 1 responds to DISB. ROM line equal to a '1'.
LRE	The lower 512 bytes of RAM are disabled.	The lower 512 bytes of RAM are enabled.
URE	The upper 512 bytes of RAM are disabled.	The upper 512 bytes of RAM are enabled.
A10	RAM responds to ADDR10 equal to a '0'.	RAM responds to ADDR10 equal to a '1'.
A11	RAM responds to ADDR11 equal to a '0'.	RAM responds to ADDR11 equal to a '1'.
A12	RAM responds to ADDR12 equal to a '0'.	RAM responds to ADDR12 equal to a '1'.
A13	RAM responds to ADDR13 equal to a '0'.	RAM responds to ADDR13 equal to a '1'.
A14	RAM responds to ADDR14 equal to a '0'.	RAM responds to ADDR14 equal to a '1'.

5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
Pin -3 through Pin -21		Not Used
-22	GND	
P1, Pin -A	GND	Ground Common Return (Power and Signal)
-H		Not Used
Pin -C through Pin -S		Not Used
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
Pin -V through Pin -Z		Not Used

Table 5.1 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P3, Pin 1	GND	Ground
- 2	ADDR0	Address Bit 0
- 3	ADDR1	Address Bit 1
- 4	ADDR2	Address Bit 2
- 5	ADDR3	Address Bit 3
- 6	ADDR4	Address Bit 4
- 7	ADDR5	Address Bit 5
- 8	ADDR6	Address Bit 6
- 9	ADDR7	Address Bit 7
-10	ADDR8	Address Bit 8
-11	ADDR9	Address Bit 9
-12	ADDR10	Address Bit 10
-13	ADDR11	Address Bit 11
-14	ADDR12	Address Bit 12
-15	ADDR13	Address Bit 13
-16	ADDR14	Address Bit 14
-17	ADDR15	Address Bit 15
-18	$\overline{\text{TOP ACTIVE}}$	Negative True, (Low) Indicates Top Plane Module Address Recognition (High Causes a Bottom Plane Bus Cycle).
-19	READ	High Indicates Top Plane Bus Data Should Be Gated On.
-20	WRITE	High Indicates Top Plane Bus Data is Valid.
-21	SYNC.PHASE1	Sync signal from the processor (8080A-2) and PHASE1 clock are ANDed together.
-22	GND	Ground

Table 5.1 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P3, Pin A	GND	Ground
-R	DBIT0	Data Bit 0
-C	DBIT1	Data Bit 1
-D	DBIT2	Data Bit 2
-E	DBIT3	Data Bit 3
-F	DBIT4	Data Bit 4
-H	DBIT5	Data Bit 5
-J	DBIT6	Data Bit 6
-K	DBIT7	Data Bit 7
-L		Not Used
-M	BANK SEL.	Rank select bit ; one of the two bank select lines.
-N		Not Used
-P	$\overline{I/O}$	Negative True, (Low) Indicates (A15 A14 A13 A12) = (1000)H and output device selection.
-R	SYNC	Sync signal from the processor (8080A-2).
-S		Not Used
-T	WO	High Indicates Write or Output Cycle.
-U	DISABLE ROM	Used as another bank select bit.
-V		}
		} Not Used
-W		}
-X	MEMR	High Indicates Current Cycle is a Memory Read.
-Y		Not Used
-Z	GND	Ground

Table 5.2 Test Connector Information

Connector and Pin No.	Signal Name	Signal Description
P2, Pin 1	ABUS6	Internal Address Bus Bit 6
- 2	ABUS4	Internal Address Bus Bit 4
- 3	ROM00	Memory Block 1 Select Line
- 4	ABUS9	Internal Address Bus Bit 9
- 5	ROM02	Memory Block 3 Select Line
- 6	ABUS2	Internal Address Bus Bit 2
- 7	ABUS0	Internal Address Bus Bit 0
- 8	ROM04	Memory Block 5 Select Line
- 9		Not Used
-10		
-11	ROM11	Memory Block 8 Select Line
-12	ROM13	Memory Block 10 Select Line
Pin -13 through Pin -15		Not Used

Table 5.3 Test Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P2, Pin A	ABUS7	Internal Address Bus Bit 7
-B	ABUS5	Internal Address Bus Bit 5
-C	ABUS3	Internal Address Bus Bit 3
-D	ABUS8	Internal Address Bus Bit 8
-E		Not Used
-F	ROM01	Memory Block 2 Select Line
-H	ABUS1	Internal Address Bus Bit 1
-J	ROM03	Memory Block 4 Select Line
-K	ROM05	Memory Block 6 Select Line
-L	ROM10	Memory Block 7 Select Line
-M	ROM12	Memory Block 9 Select Line
-N	ROM14	Memory Block 11 Select Line
-P		Not Used
-R	ROM15	Memory Block 12 Select Line
-S		Not Used

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 3), timing diagram (figure 2), component location diagram (figure 4), and parts list (02640-60243) located in the appendix. The 02640-60243 ROM and 02640-60241 EPROM Control Memory PCA use the same block, and timing diagrams.

The Control Memory w/ Dual Bank Select Module provides program storage in Read Only Memory (ROM) for the Processor (8080A-2) Module which controls the functions of the terminal. By communicating over the top plane bus, the module permits the processor to operate without any wait states during instruction fetch and stack operations. The block diagram shows the functional configuration of the module.

The board is design to use MOSTEK MK36000-4/5 Roms with access times of 250/300 nanoseconds or MOTOROLA MCM68B364 Roms with access time of 250 nanoseconds.

Note: These ROMs have power down capability when they are not selected.

3.1 DATA AND ADDRESS DRIVER LOGIC .

3.1.1 The data drivers are bidirectional buffers which present minimum loading to the CPU and synchronize the movement of data along a bidirectional bus on the PCA. The drivers are enabled only when the control logic determines that data is required at the CPU or at the local RAM. There is one set of drivers for transferring information from the PCA to the CPU and another for bringing data from the CPU to the local RAM.

3.1.2 Data on the top plane bus (P3 connector) is applied to the inputs of U15 and driven onto the internal bidirectional data bus (DBUS0- DBUS7). Data from the ROMs (8K by 8 bits) is driven onto this same internal bidirectional bus. Address information is buffered on the processor (8080A-2) PCA, driven onto the top plane bus, and then through U24, and U25 to the ROM and RAM input pins.

3.1.3 The least significant 13, and 9 address lines distribute address information throughout the ROM and RAM arrays,respectively. The 7 highest order bits are examined to determine whether or not the PCA is being addressed.

3.2 ROM ARRAY AND RAM MEMORY.

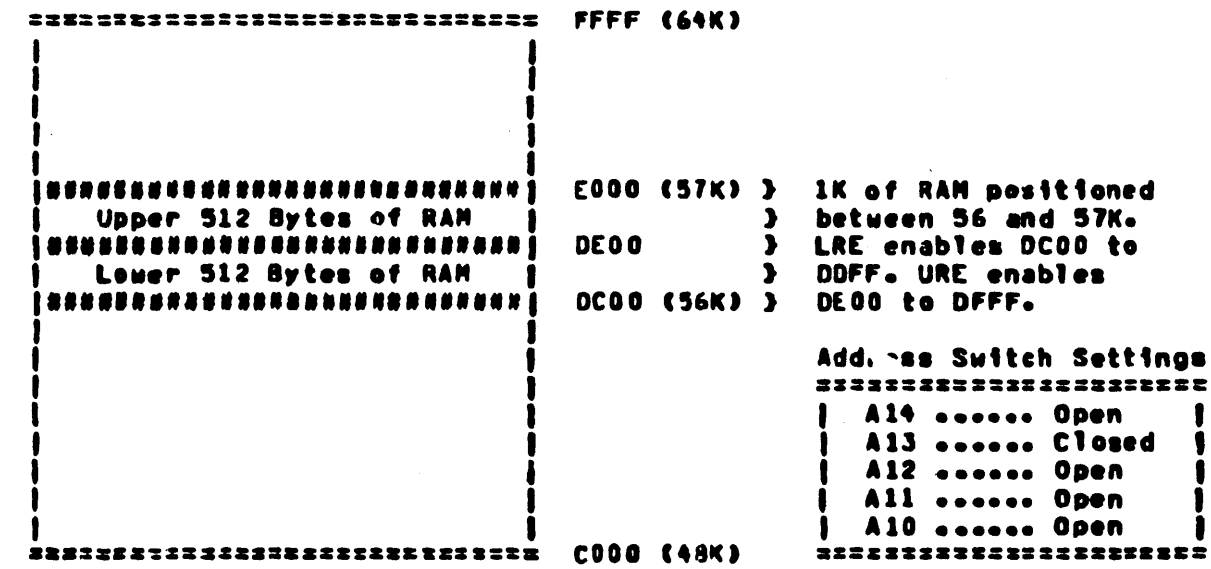
3.2.1 The Control Memory PCA is designed to work with the Mostek 64K ROM (part number 36000-4/5) or Motorola (part number MCM68B364). The ROM chips are mask programmed, 250/300 nanoseconds access time, 64K bits organized as 8K by 8 bits.

3.2.2 The RAM chips are static 4K N-channel MOS devices that are organized as 1K by 4 bits.

3.3 RAM ENABLE LOGIC .

3.3.1 The 1K RAM is made up of two 1K by 4 static N-channel mos chips. The RAM may be positioned anywhere within the range 36-64K by using the address select switches A14, A13, A12, A11, and A10. A 7-bit comparator determines when the RAM block is being addressed. The constant being applied to the comparator is set as per the description of the switch settings (see Table 4.0) . The URE and LRE select switches also allow the RAM to be configured as an upper or lower 512 byte block, or to be entirely disabled or enabled (see Table 4.0). When the comparator recognizes the address applied to it, the RAMs are enabled and the ROMs are disabled . The comparator logic also returns a $\overline{\text{TOP ACTIVE}}$ signal through the TOP ACTIVE logic.

Display Memory Map showing an example of RAM positioning.



Note: All the switches on the board can be replaced by jumpers. Insert jumpers for closed switches.

3.3.2 The CPU provides all the set up and hold times required by the memory chips. Figure 2 shows the read and write timing relationships. The write signal is used to disable the RAM outputs and the WO signal is used to direct data from the processor to the RAMs. The WRITE pulse causes the RAMs to store the current state of the data lines at the location addressed by the address lines.

3.4 ROM ENABLE AND BANK SELECT LOGIC .

3.4.1 Each of the 8K ROM chips may be individually disabled. This feature permits substitution of specialized firmware for specific applications without requiring a complete new set of mask programmed ROMs. If an 8K ROM is de-selected, the ROM ENABLE logic will not return a $\overline{\text{TOP ACTIVE}}$ signal when an access is made to that 8K block. By using an EPROM PCA, it is possible for an EPROM to reside in the same address space as a disabled ROM, thus a substitution may be accomplished.

3.4.2 The BANK SELECT LOGIC allows the placement of each 48K ROM array at 1 of 4 48K blocks. The bank number is selected by the DIS ROM and BANK SEL. lines. The switches BS0, DS0, BS1, and DS1 are used to set the bank address that each 48K bank responds to. On board logic prevents either bank from being accessed if both have been assigned the same bank number (see Table 4.0).

3.5 TOP ACTIVE . AND READ LOGIC .

3.5.1 The TOP ACTIVE LOGIC recieves enable signals from the ROM and RAM enable logic and returns a negative true $\overline{\text{TOP ACTIVE}}$ signal to the processor (8080A-2) PCA .

3.5.2 The READ LOGIC examines the status from the processor (8080A-2) PCA to determine if the cycle is going to be a read.

This allows the TOP ACTIVE LOGIC to return a $\overline{\text{TOP ACTIVE}}$ signal in time to prevent a bottom plane memory cycle .

4.0 TIMING CONSIDERATIONS.

4.0.1 The 8080A-2 Processor is driven by a clock which has a basic period of 400 nanoseconds. There are two clock signals which drive the CPU and are generated on the Processor (8080A-2) PCA. These clock signals govern the timing of addresses coming from the CPU and determine the set up times required for information that is returned from the memory to the processor. The timing diagram (figure 2), shows the timing for PHASE1 and PHASE2 and the resultant access time that is availabe at the pins of the CPU.

4.0.2 Addresses become valid at the pins of the processor a maximum of 195 nanoseconds after the rising edge of PHASE2. Data must be valid at the processor 147 nanoseconds before the leading edge of the T3 PHASF2. The time required from output of the address until the data must be valid at the CPU is 458 nanoseconds.

4.0.3 The time required to return the $\overline{\text{TOP ACTIVE}}$ signal is also shown in figure 2. The $\overline{\text{TOP ACTIVE}}$ signal prevents a bottom plane memory cycle. The timing required for the return of this signal is 26/126 nanoseconds for 400/500 nanoseconds processor's clock cycle.

Note: the timing diagram indicates the worst case possibilities.

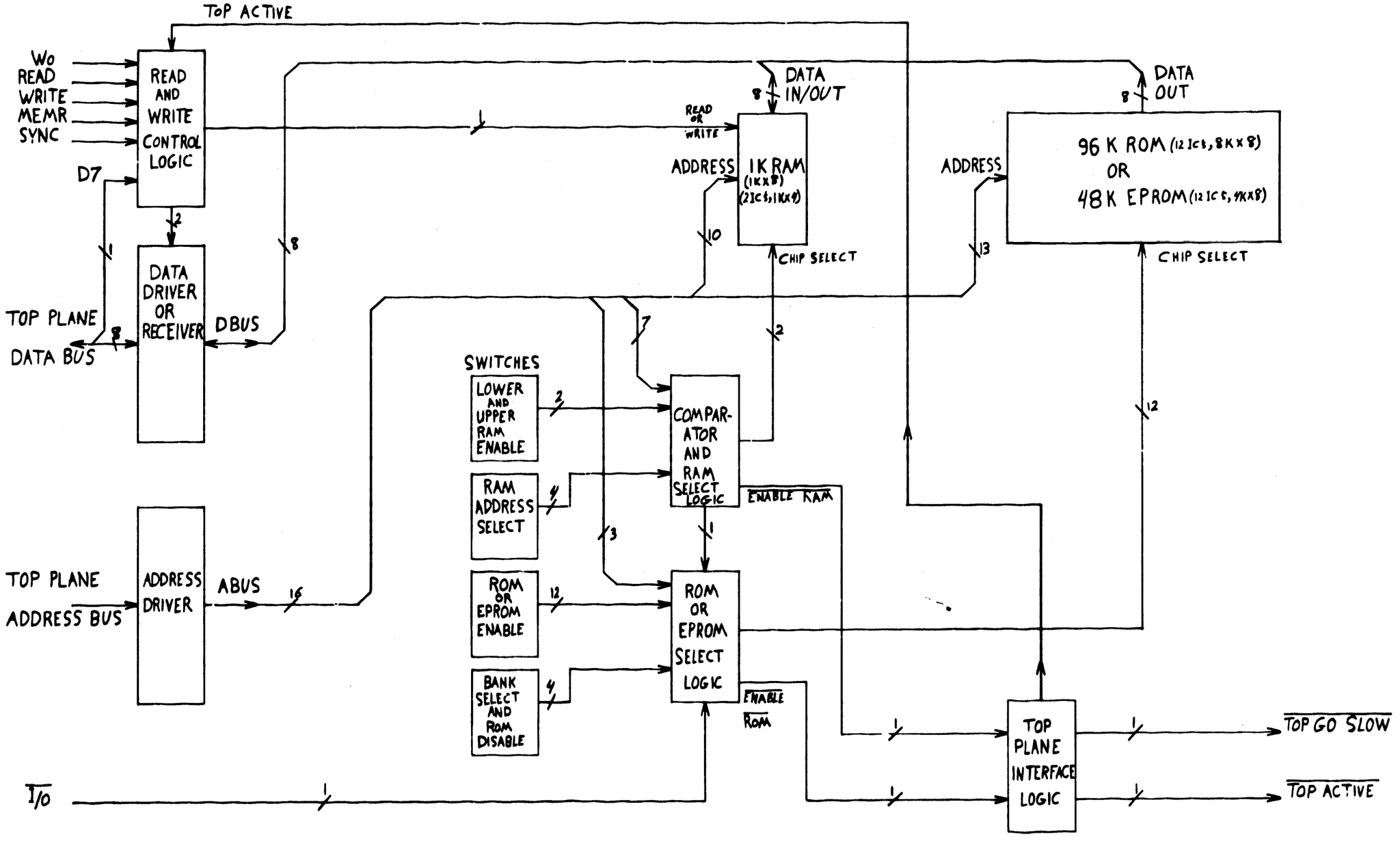
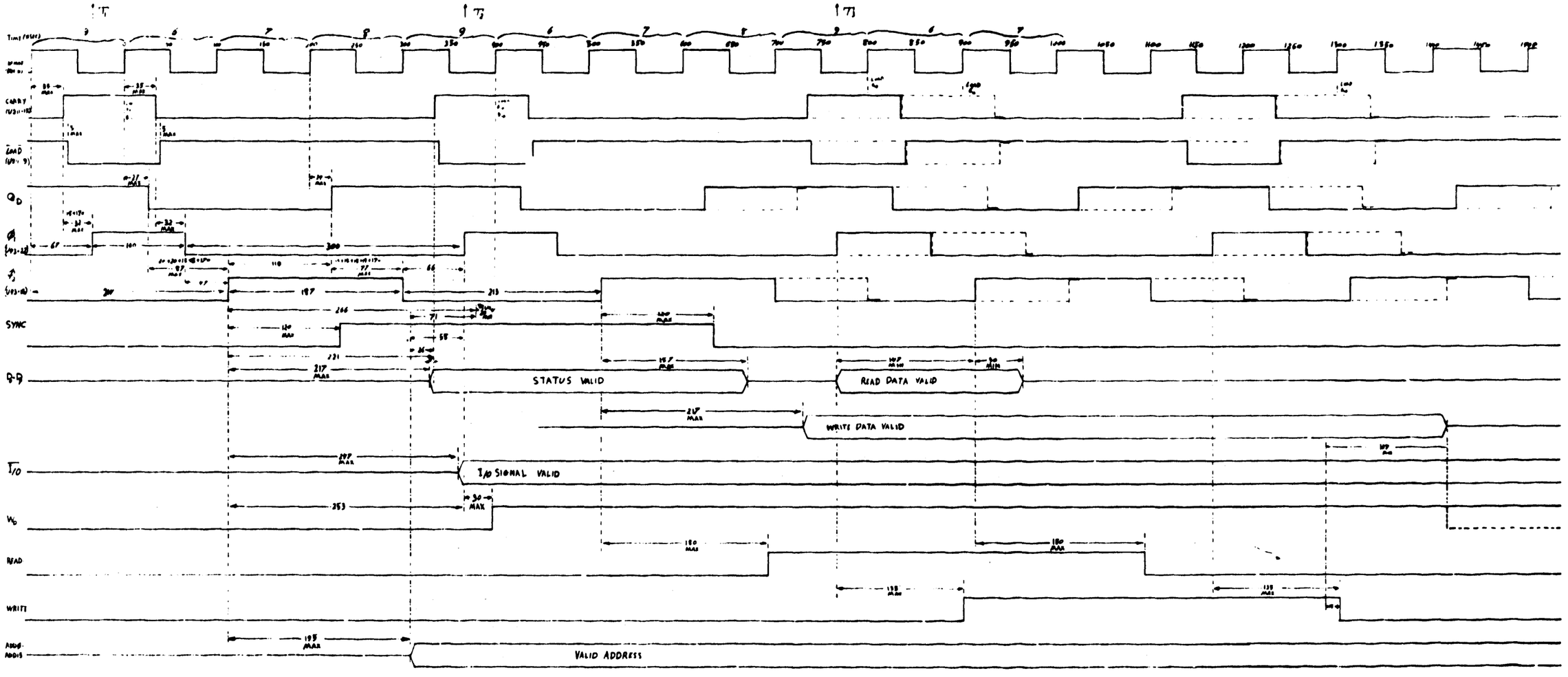


Figure 1
Control Memory Block Diagram
13255-91243



NOTE: ALL TIMING IN NANO SECOND
UNLESS INDICATED OTHERWISE.

Figure 2
Control Memory Timing Diagram
13255-91243

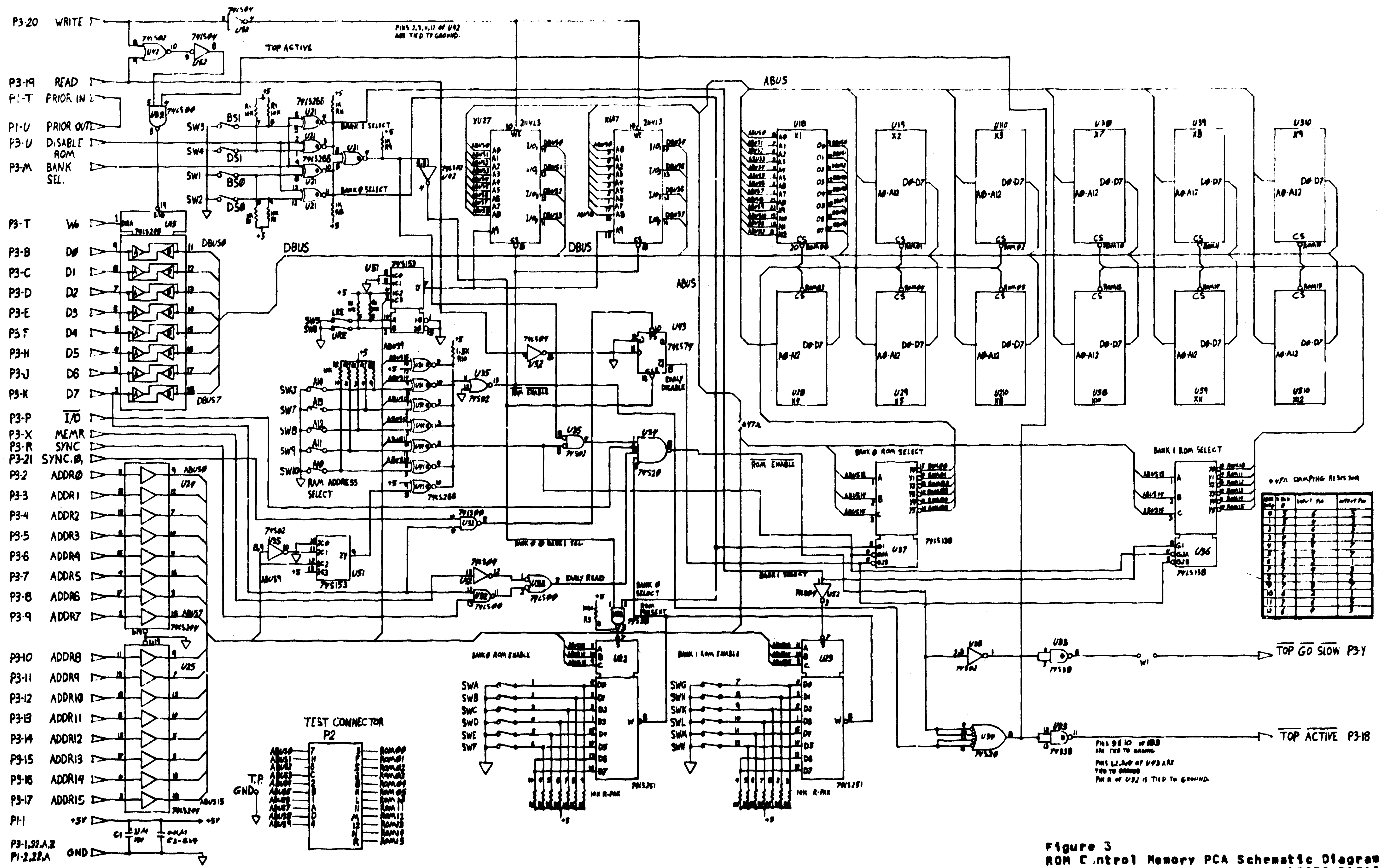


Figure 3
ROM Control Memory PCA Schematic Diagram
13255-91243
13255-91243

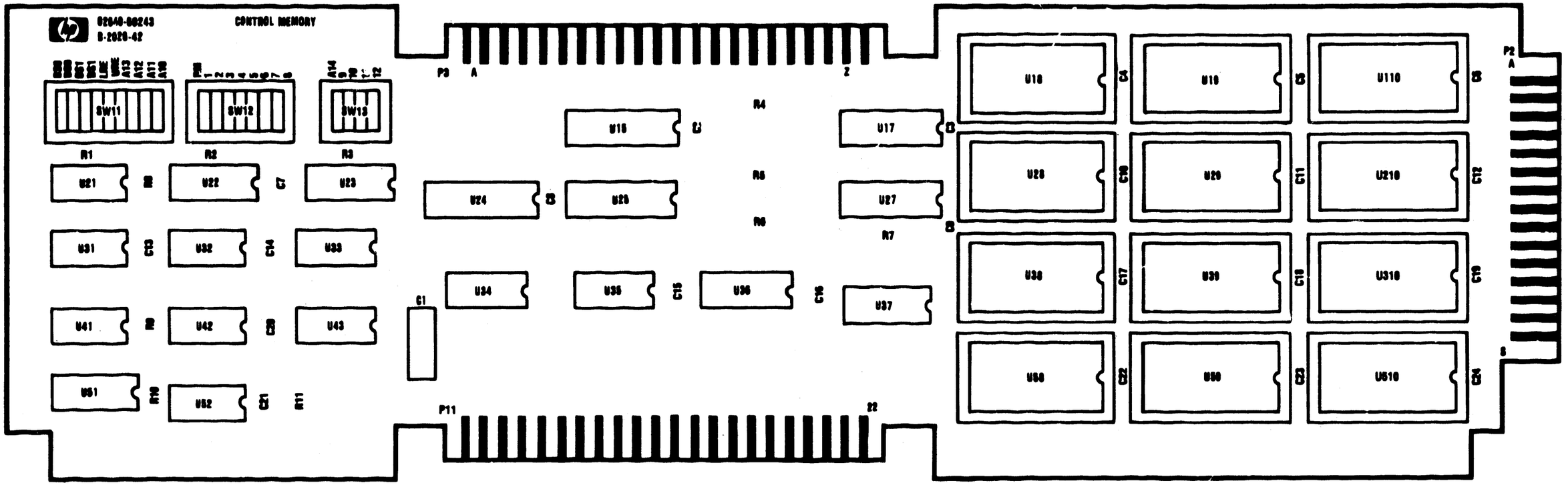


Figure 4
ROM Control Memory PCA Components Location Diagram
13255-91243

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	02A40-60043	3	1	96K CONTROL MEMORY-PCA DATA CODE:D-2026-42	28480	02A40-60043
C1	0180-2879	7	1	CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C2	0160-4554	7	23	CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C3	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C4	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C5	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C6	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C7	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C8	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C9	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C10	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C11	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C12	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C13	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C14	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C15	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C16	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C17	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C18	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C19	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C20	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C21	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C22	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C23	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C24	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
R1	1810-0280	8	3	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
R2	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
R3	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
R4	1810-0302	5	4	NETWORK-RES 8-SIP47.0 OHM X 4	01121	208D470
R5	1810-0302	5		NETWORK-RES 8-SIP47.0 OHM X 4	01121	208D470
R6	1810-0302	5		NETWORK-RES 8-SIP47.0 OHM X 4	01121	208D470
R7	1810-0302	5		NETWORK-RES 8-SIP47.0 OHM X 4	01121	208D470
R8	0683-1025	9	3	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R9	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R10	0683-1525	4	1	RESISTOR 1.5K 5% .25W FC TC=-400/+700	01121	CB1525
R11	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
SW11	3101-2862	7	1	SWITCH-TOGGLE 10-1A MS	28480	3101-2862
SW12	3101-1983	9	1	SWITCH-TOGGLE 8-1A MS	28480	3101-1983
SW13	3101-2156	8	1	SWITCH-TOGGLE 5-1A MS	28480	3101-2156
U15	1820-2875	4	1	IC MISC TTL LS	01295	SN74LS245N
U17	1810-0562	5	2	IC-2114A-5	34649	P2114A-5
U21	1820-1297	0	3	IC GATE TTL LS EXCL-NOR QUAD 2-INP	01295	SN74LS266N
U22	1820-1298	1	2	IC MUXR/DATA-SEL TTL LS 8-TO-1-LINE	01295	SN74LS251N
U23	1820-1298	1		IC MUXR/DATA-SEL TTL LS 8-TO-1-LINE	01295	SN74LS251N
U24	1820-2024	3	2	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U25	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U27	1810-0562	5		IC-2114A-5	34649	P2114A-5
U31	1820-1297	0		IC GATE TTL LS EXCL-NOR QUAD 2-INP	01295	SN74LS266N
U32	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2 INP	01295	SN74LS00N
U33	1820-1451	8	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U34	1820-0688	1	1	IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
U35	1820-1322	2	1	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U36	1820-1216	3	2	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U37	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U41	1820-1297	0		IC GATE TTL LS EXCL-NOR QUAD 2-INP	01295	SN74LS266N
U42	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U43	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U51	1820-0994	6	1	IC MUXR/DATA-SEL TTL S 4-TO-1-LINE DUAL	01295	SN74S153N
U52	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
XU18	1200-0541	1	12	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU19	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU28	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU29	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU38	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU39	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU58	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU59	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU110	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU210	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
XU310	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU510	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
	0360-1682	0	1	TERMINAL-STUD BGL-TUR PRESS-MTG	28480	0360-1682

MFR NO.	MANUFACTURER NAME	ADDRESS		ZIP CODE
01121	ALLEN BRADLEY CO	MILWAUKEE	WI	[illegible]
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	[illegible]
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	[illegible]
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	9404[illegible]
28480	HEWLETT PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE	CA	9408[illegible]
34649	INTEL CORP	MOUNTAIN VIEW	CA	[illegible]
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
71707	DALE ELECTRONICS INC	COLUMBUS	NE	68601