HP 13255

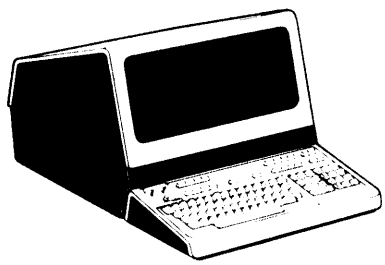
GRAPHICS DISPLAY MODULE

Manual Part No. 13255-91126

REVISED

DEC-12-77

DATA TERMINAL
TECHNICAL INFORMATION



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1.0 INTRODUCTION.

The Graphics Display Module is used with the Graphics M-Controller Module, Top Plane Connector and Controller Connector Assemblies.

The Graphics Display Module contains the storage for the 264XX Data Terminal graphics display 720 X 360 screen dot matrix. The read-write memory is accessible through the Graphics M-Controller and terminal bus for memory modification and test and through the Display Controller Module for display. It is organized as a 16,384 X 16 bit word linear array.

The module uses 16 16-pin MOS RAMs each organized 16,384 X 1 bit.

1.1 OPERATION.

The graphics display memory is read by the Graphics M-Controller during the visible portion of the terminal video display, and modified during the horizontal and vertical sweep retrace times.

The memory modification consists of modifying 1 bit at a time and may be a logical operation with the current state, the output of a serial pattern memory, or unconditionally set to '1' '0' or to the same state as the serial pattern memory output.

The pattern memory output may be scaled so that the ratio between the pattern memory bits and the memory bits may be changed from 1 to 16.

The display memory bits are displayed such that normally there is a one-to-one correspondence between the memory and display bits, automatic refresh is provided since every memory address is read during one ''frame''.
In Zoom mode the scaling or Zoom ratio may be changed from 1 to 16. Since the refresh is no longer automatic the last display bit of each block of repeated display bits in the 'X' and 'Y' direction is blanked, thus providing time for the memory refresh operation (during the 'X' blanked lines)

In addition, the 'window' resulting from Panning while in Zoom mode requires that the memory to be displayed on bit boundaries, the necessary memory word preshifting is done prior to the beginning of each display line.

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NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

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1.2 GRAPHICS M-CONTROLLER MODULE INTERFACE.

The Graphics M-Controller interfaces to the Graphics Display Module through the Controller Connector Assembly (02640-60194 or 02640-60022). This interface provides control input and timing status output signals for line and frame synchronization.

1.3 DISPLAY CONTROLLER MODULE INTERFACE.

The Display Controller Module interfaces to the Graphics Display Module through a Top Plane Connector Assembly (02640-60016 or 02640-60022). This interface provides timing input and graphics serial data output to the terminal display.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Graphics Display Module is contained in tables 1.0 through 6.3.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60126	Graphics Display PCA	12.5 x 4.00 x 0.5	0.5
02640-60016	5-Wide Top Plane Connector Assembly	N/A	N/A
02640-60022	4-Wide Top Plane Connector Assembly	N/A	N/A
02640-60194	Controller Connector Assembly	N/A	N/A
Number of Backplane slots Required: 1			

Table 2.0 Reliability and Environmental Information

Environmental:	(X) HP Class B ( ) Other:
Restrictions:	Type tested at product level
Failure Rate:	4.8 (percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	-42 Volt Supply
@ 1A	@ 600 mA	@ 200mA	N/A
115 volts ac N/A		220 volts ac N/A	
Clock Frequency: 21.06 or 17.60 MHz			

Table 4.0 Jumper Definitions

PCA Designation	Function	
	In	Out
Jumper Plug	(Note: This jumper must always be installed for proper operation of the PCA.)	
-5V	Applies -5V to the RAM array.	Disconnnects -5V generated on the PCA. Permits an external supply to be connected.

Table 5.0 Connector Information (Graphics Display PCA).

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3		Not Used
-4	-12V	-12V Power Supply
-5		Not Used
-6		
-7		
-8		
-9		
-10		
-11		
-12		
-13		
-14		
-15		
-16		
-17		
-18		
-19		
-20		
-21		
-22	GND	Ground Common Return (Power and Signal)

Table 5.0 Connector Information (Graphics Display PCA Cont'd).

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B		Not Used
-C	+12V	+12 Volt Power Supply
-D		Not Used
-E	BUS0	Negative True, Data Bus Bit 0
-F	BUS1	Negative True, Data Bus Bit 1
-H	BUS2	Negative True, Data Bus Bit 2
-J	BUS3	Negative True, Data Bus Bit 3
-K	BUS4	Negative True, Data Bus Bit 4
-L	BUS5	Negative True, Data Bus Bit 5
-M	BUS6	Negative True, Data Bus Bit 6
-N	BUS7	Negative True, Data Bus Bit 7
-P		
-R		
-S		Not Used
-T	PRIOR IN	Bus Controller Priority Out
-U	PRIOR OUT	Bus Controller Priority Out
-V		Not Used
-W		
-X		
-Y		
-Z		

Table 5.1 Connector Information (Graphics Display PCA).

Connector and Pin No.	Signal Name	Signal Description
P3, Pin 1		Not Used
- 2		
- 3	--- 103	Negative True, Column Count 103
- 4		Not Used
- 5		
- 6		
- 7		
- 8		
- 9		
-10		
-11		
-12		
-13		
-14		
-15		
-16		
-17		
-18		
-19		
-20	------ XBITS2	Negative True, External Bit Stream 2
-22	GND	Ground

Table 5.1 Connector Information (Graphics Display PCA Cont'd).

Connector and Pin No.	Signal Name	Signal Description
P3, Pin A	DSPY CLK	21.060 MHz Display Clock
-B	GND	Ground
-C	D2	Negative True, Character Dot Position 2
-D		Not Used
-E		
-F		
-H		
-J	VBLNK	Vertical Blanking
-K		Not Used
-L		
-M		
-N		
-P		

Table 5.4 Connector Information (Graphics Display PCA).

Connector and Pin No.	Signal Name	Signal Description
P3,Pin -R		}
-S		}
-T		} Not Used
-U		}
-V		}
-W		}
-X		}
-Y	GND	Ground
-Z		Not Used

Table 5.2 Connector Information (Graphics Display PCA).

Connector and Pin No.	Signal Name	Signal Description
P2,Pin 1	A0	Col or Row Address, Bit0
-2	A1	Col or Row Address, Bit1
-3	A2	Col or Row Address, Bit2
-4	A3	Col or Row Address, Bit3
-5	A4	Col or Row Address, Bit4
-6	A5	Col or Row Address, Bit5
-7	A6	Col or Row Address, Bit6
-8	X0	Bit Address, Bit0
-9	X1	Bit Address, Bit1
-10	X2	Bit Address, Bit2
-11	X3	Bit Address, Bit3
-12	RAS	Row Address Strobe
-13	CAS	Column Address Strobe
-14	$\overline{W}$	Negative True, Write Enable
-15	$\overline{LOAD}$	Negative True, Load

Table 5.2 Connector information (Graphics Display PCA Cont'd).

Connector and Pin No.	Signal Name	Signal Description
P2, Pin -A	CLK	10.5 MHz Clock
-B	GND	Ground
-C	CLK	Negative True 10.5MHz Clock
-D	103.D2	Negative True, Col 103 and Dot 2
-E	DI	Data In
-F	A7	Address Bit 7
-H	H	Inhibit Graphics Display
-J	STR3	Negative True, Strobe 3
-K	STR4	Negative True, Strobe 4
-L	STR5	Negative True, Strobe 5
-M	VR	Vertical Retrace
-N	STR6	Negative True, Strobe 6
-P		Not Used
-R	SAMPLE	Sample Bit
-S	GND	Ground

Table 6.0 Module Bus Pin Assignments

Function Performed: Load Mode Control Register Bits	Value	Bus Signal
Poll Bit: Not Used	1	ADDR 15
The M-Controller decodes address STR5 as follows	0	ADDR 14
	0	ADDR 13
Module Address:(ADDR 4,11,10,9) = (1100) , 14B	0	ADDR 12
	1	ADDR 11
Function Specifier: ADDR 6 = 1	0	ADDR 10
ADDR 5 = 0	0	ADDR 9
ADDR 0 = 1	X	ADDR 8
	X	ADDR 7
Data Bus Interpretation:	1	ADDR 6
	0	ADDR 5
B7 Not Used	1	ADDR 4
	X	ADDR 3
	X	ADDR 2
	X	ADDR 1
	1	ADDR 0
B6 Not Used	B7	BUS7
	B6	BUS6
B5 1 = Set Sample	B5	BUS5
0 = Clear Sample	B4	BUS4
	B3	BUS3
B4 1 = Enable Graphics Display	B2	BUS2
0 = Inhibit Graphics Display	B1	BUS1
	B0	BUS0
B3 1 = Enable Set or Clear Graphics Memory	1=Logical 1 = Bus Low	
0 = Inhibit Set or Clear Graphics Memory	0=Logical 0 = Bus High	
B2 1 = Enable ALU Pattern Memory Input	X= Dont care	
0 = Inhibit ALU Pattern Memory Input		
B1 1 = Enable ALU J Input		
0 = Clear ALU J Input		
B0 1 = Enable ALU K Input		
0 = Clear ALU K Input		

Table 6.1 Module Bus Pin Assignments

Function Performed: Load Pattern Memory	Value	Bus Signal
Poll Bit: Not Used	1	ADDR15
M-Controller decodes address STR3 as follows	0	ADDR14
	0	ADDR13
Module Address:(ADDR 4,11,10,9) = (1100) , 14B	0	ADDR12
	1	ADDR11
Function Specifier: ADDR 6 = 1	0	ADDR10
ADDR 5 = 0	0	ADDR9
ADDR 0 = 0	X	ADDR8
	X	ADDR7
Data Bus Interpretation:	1	ADDR6
	0	ADDR5
B7 Pattern Bit 7 (Shifted First)	1	ADDR4
	X	ADDR3
B6 Pattern Bit 6	X	ADDR2
	X	ADDR1
B5 Pattern Bit 5	0	ADDR0
B4 Pattern Bit 4	B7	BUS7
	B6	BUS6
B3 Pattern Bit 3	B5	BUS5
	B4	BUS4
B2 Pattern Bit 2	B3	BUS3
	B2	BUS2
B1 Pattern Bit 1	B1	BUS1
	B0	BUS0
B0 Pattern Bit 0 (Shifted Last)	1=Logical 1	1=Bus Low
	0=Logical 0	0=Bus High
	X=Don't Care	

Table 6.2 Module Bus Pin Assignments

Function Performed: Load Prescaler	Value	Bus Signal
Poll Bit: Not Used		
	1	ADDR15
M-Controller decodes address STR3 as follows	0	ADDR14
	0	ADDR13
Module Address:(ADDR 4,11,10,9) = (1100) , 14B	0	ADDR12
	1	ADDR11
Function Specifier: ADDR 6 = 0	0	ADDR10
ADDR 5 = 1	0	ADDR9
ADDR 0 = 1	X	ADDR8
	X	ADDR7
Data Bus Interpretation:	0	ADDR6
	1	ADDR5
B7 Not Used	1	ADDR4
	X	ADDR3
B6 Not Used	X	ADDR2
	X	ADDR1
B5 Not Used	1	ADDR0
B4 Not Used	B7	BUS7
	B6	BUS6
B3 Scale Factor-1 Bit 3 (Msb)	B5	BUS5
	B4	BUS4
B2 Scale Factor-1 Bit 2 Scale Factor 1 = 0000	B3	BUS3
	B2	BUS2
B1 Scale Factor-1 Bit 1	B1	BUS1
	B0	BUS0
B0 Scale Factor-1 Bit 0 (Lsb)		
	1=Logical 1	1=Bus Low
	0=Logical 0	0=Bus High
	X=Don't Care	

Table 6.3 Module Bus Pin Assignments

Function Performed: Load Magnifier,Preshift,and Dot Inhibit (Display Control Byte)			Value	Bus Signal
Poll Bit: Not Used			X	ADDR15
M-Controller strobe is STR6.			X	ADDR14
			X	ADDR13
			X	ADDR12
			X	ADDR11
			X	ADDR10
			X	ADDR9
			X	ADDR8
			X	ADDR7
M-Controller Bus Interpretation			X	ADDR6
			X	ADDR5
A7	Preshifter Bit 3 (Msb)	Preshifter is loaded with 1's complement	X	ADDR4
A6	Preshifter Bit 2		X	ADDR3
A5	Preshifter Bit 1		X	ADDR2
A4	Preshifter Bit 0 (Lsb)	zero preshift = 1111	X	ADDR1
			X	ADDR0
A3	Magnifier Bit 3 (Msb)	Magnifier is loaded with 2's complement	A7-A0 and X3-X0 1=Logical 1=M-Controller High	
A2	Magnifier Bit 2			
A1	Magnifier Bit 1	magnification 1 = 1111		
A0	Magnifier Bit 0 (Lsb)			
X3	Dot Inhibit Bit 3 (Msb)	Dot Inhibit is loaded with 2's complement		
X2	Dot Inhibit Bit 2			
X2	Dot Inhibit Bit 1	inhibit 1 dot = 1111		
X0	Dot Inhibit Bit 0 (Lsb)			

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), the timing diagrams (figures 3 and 4), the component location diagram (figure 5), and parts lists (02640-60016, 02640-60022, 02640-60126, and 02640-60194) located in the appendix.

The Graphics Display PCA is the graphics display memory for the terminal. It consists of memory drivers and recievers, series termination resistors, write enable decoder, memory array, memory output buffer, test header ALU, mode control register, pattern memory, prescaler, display register bit counter and shift logic, clock generator, dot inhibit, display enable, preshifter and magnifier.

3.1 MEMORY DRIVERS and RECEIVERS.

3.1.1 The memory drivers (with integral receivers) drive the memory array bus inputs consisting of column address strobe, row address strobe data in, and address inputs.

The drivers have a specified propagation delay for a capacitive load 1.5X the worst case memory array input bus capacitance.

3.1.2 The integral memory receivers are used in diagnostic mode; they allow the memory array bus inputs to be tested, since the state of these lines may be output to the test header or to the terminal display.

3.2 SERIES TERMINATION RESISTORS.

The series termination resistors minimize undershoot by terminating the bus lines with the line impedance. This approximates to 20 Ohms since it consists of an 80-Ohm line with distributed lumped capacitive loads. Current limit protection is provided free which limit the memory driver output current to 75 mA if two or more array inputs are shorted together.

3.3 WRITE ENABLE DECODER.

3.3.1 The write enable decoder (U54 , U55) decodes the Bit Address

X3 through X0, the output is enabled by the write pulse $\overline{W}$

therefore one RAM only will have $\overline{WE}$ (pin 3) asserted during a Read Modify write operation (figure 4). This mode is used for writing a vector into the graphics memory.

3.3.2 The graphics memory (terminal display) is set or cleared by asserting $\overline{WE}$ on all RAMs during a Read operation (figure 4) and setting Data from the ALU to set or clear. This is done by setting the C bit in the mode control register which is synchronized (U48, Pin 6) and then sets all RAM $\overline{WE}$ inputs low (U33,U43,U53,U63, Pins 3, 6, 8, and 11).

3.4 MEMORY ARRAY.

3.4.1 The memory array consists of sixteen 16K RAMs in ceramic DIP packages. Any Mostek MK4116-4 or equivalent RAM with a demonstrated reliability of < 0.3% failures per 1000 hours may be used.

The RAMs are used with sockets to allow field repair.

3.4.2. Each RAM is organized as a 128 X 128 cell array addressable by row and column. The 14-bit memory address is therefore multiplexed and strobed into the row and column latches with the row and column strobes.

3.4.3 The power distribution is via a low impedance 4-layer PC board structure. The ceramic capacitors which supply the transient current loads are organized so that some redundancy exists. This allows reliable operation with one open circuit component.

3.4.4 The linear array of 16,384 X 16 bit words (184 are unused) is read sequentially by the M-Controller so that in non-Zoom mode 45 words are read per line of display, and the display register output appears as a 720-bit stream.

3.5 MEMORY OUTPUT BUFFER.

The memory output buffer (U34,U64) drives the Schottky display register and the ALU. Since it has input hysterisis and a low input current, it provides the maximum isolation/noise immunity between the memory and display section.

3.6 TEST HEADER.

The test header (U65) is used in diagnostic mode only. By grounding TP1 and TP2 as shown in the table the operations indicated are possible.

TP1	TP2	Result
open	open	memory output buffer-> display register ALU and header
open	ground	header (external source) -> display register ALU
ground	XXXXXX	memory receiver -> display register ALU and header

3.7 ALU.

3.7.1 The ALU specifies the input data to the Memory Array in write or Read Modify Write mode.

3.7.2 Multiplexer (U36 , U66) selects 1 bit Rxy from the 16-bit word at the memory output buffer from the Bit address X3 through X0 as follows.

Bit Address X3 X2 X1 X0	Selects bit from memory output buffer to Rxy
0 0 0 0	D0 (U34,Pin 3)
0 0 0 1	D1 (U34,Pin 5)
etc....	
1 1 1 1	D15 (U64,Pin 18)

The output data bit Rxy is output to the M-Controller as DI (P2, Pin E). This is used for graphics self test and it also provides a means of dumping the memory to an IO device.

3.7.3 The ALU output (U46, Pin 6) may be a function of Rxy, Pattern memory or unconditional. This is controlled by the E, J and K bits of the Mode Control Register as follows:

E	J	K	Data to memory U45, Pin 10	ALU function
0	0	0	Rxy	same data
0	0	1	0	clear
0	1	0	1	set
0	1	1	--- Rxy	complement data
1	0	0	P	pattern
1	0	1	P.Rxy	clear if pattern bit is clear
1	1	0	P+Rxy	set if pattern bit is set
1	1	1	P xor Rxy	complement if pattern bit is set

3.8 MODE CONTROL REGISTER.

The mode control register is a 6-bit register (U79) used to control the ALU, write enable decoder, prescaler and dot inhibit as follows:

Terminal bus	Name	Function	Destination
Bit 0	K	Clear	ALU
Bit 1	J	Set	ALU
Bit 2	E	Enable Pattern Input	ALU
Bit 3	C	Set or Clear Memory	Write Enable Decoder
Bit 4	H	Enable Graphics Display	Dot inhibit (U510,Pin 5)
Bit 5	Sample	Prescalar Enable	Prescalar (U610,Pins 7 and 10)

3.9 PATTERN MEMORY.

This is an 8-bit serial recirculating memory which specifies the pattern to be used when writing a vector into the graphics display memory. (U69)
It is loaded with Strobe 4 and the pattern shifts after each WE pulse provided the enable from the Prescalar is true (U510-10).

The M.S.B. of the Pattern memory is output first (U69,Pin 7) therefore a vector drawn left to right with pattern enabled will be in the same bit order as the pattern byte loaded Bit 7 through Bit 0.

3.10 PRESCALER.

3.10.1 This is a variable modulus counter which determines the scaling between the pattern memory bits and the graphics display memory bits.

3.10.2 The prescaler is loaded with Strobe3 and initialized by Strobe4. Therefore whenever the pattern memory is changed the counter section (U610) of the prescalar is initialized to the latch (U710) value.

3.10.3 The scale factor can be changed from 1(normal) to 16 which effectively 'stretches' the pattern up to 16X.

3.10.4 The prescaler is enabled by the sample bit (U79, Pin 10).

3.11 DISPLAY REGISTER.

3.11.1 The display register (U37,38,68, and 78) is a 21MHZ synchronous universal shift register controlled by the Bit counter and shift logic and loaded from the memory output buffer data bus (D0 through D15). Its primary function is parallel to serial conversion, the 16-bit word bit-serial output (U37, Pin 15) connects to the display module top plane bus through the dot inhibit logic.

Since the display register provides a 1-word buffer the memory read and display register shift operations can be overlapped.

3.11.2 The mode of the display register is controlled as follows:

Display Register Mode		Function	Purpose
S0 (Pin 9)	S1 (Pin 10)		
0	0	Do Nothing	Used in Zoom mode -displays the same data for multiple clocks
0	1	Shift Left	Used to output the next bit to the display -the MSB D0 is shifted first
1	1	Load	Used to parallel load the next word from the memory output buffer

3.12 BIT COUNTER AND SHIFT LOGIC.

3.12.1 The Bit counter (U611) and shift logic (U39, Pin 3 and U49, Pins 6 and 12) control the display register mode and supply a load pulse for the M-Controller - Graphics Display handshake (see figure 4).

The load pulse indicates to the M-controller that the current memory word has been loaded into the display register and the next memory word can be read.

3.12.2 The bit counter consists of a modulo 16 counter, which is enabled by the magnifier (U611, Pin 7). During normal operation the output of the bit counter is decoded (U39, Pins 12 and 13) (U510, Pin 3) such that a shift is generated at each bit counter increment and a display register load is generated at each sixteenth bit counter increment.

3.12.3 Prior to the visible display the display register is loaded by 103.D2 (U39, Pin 1 and U49, Pin 3) and then preshifted (U49, Pin 4). In Pan mode the first dot displayed may be any bit position within a given word, the bit counter will correspond to that bit position.

3.13 CLOCK GENERATOR.

3.13.1 The clock generator consists of a modulo 2 counter (U210) and a synchronizing circuit (U28, Pins 1, 2 and 3). This generates a phase locked 10.5 MHz clock (P2, Pin A) used by the Graphics M-Controller.

3.13.2 Since the entire graphics system is synchronized with the 21 MHz display module clock, in a 50Hz terminal all of the operations will be 20% slower.

3.13.3 The graphics display is synchronized with the terminal display by decoding Col 103 and Dot2 (U29, Pin 4). This occurs 16 clocks before the first visible dot on the terminal display.

Prior to 103.D2 the M-controller reads the first memory word to be displayed. The 16clock period which follows is then used to preshift the data if required and read the second memory word to be displayed (figure 4).

3.14 DOT INHIBIT.

The dot inhibit logic inhibits the bit serial output from the display register to the Display Controller Module. There are three inputs which can cause the graphics display to be blanked.

3.14.1 The graphics display is blanked or inhibited by the Processor module (P2, Pin H) if the graphics display is turned off.

3.14.2 In Zoom mode the graphics M-controller blanks the last line of a group of repeated lines. This time is used to refresh the graphics memory, however the 'grid' of blank dots is useful for resolving the dot boundaries (U79, Pin 12).

3.14.3 In Zoom mode the dot inhibit logic blanks the last dot of each group of repeated dots. This is implemented with a variable modulus counter (U511) and inhibit flipflop (U210, Pin 7); the sequence is to enable the flipflop at each new bit, the carry from the counter (U511, Pin 15) then clears the inhibit flipflop at a particular dot position blanking the display bits in the group until a new bit is processed.

Since the algorithm is fixed (by M-Controller firmware) to always blank the last dot, the dot inhibit (U511) is always loaded with the 2's complement of the (magnifier (Zoom) value-1).

3.15 DISPLAY ENABLE.

3.15.1 The display enable is a modulo 16 latching counter which is used to determine the location of the first visible display dot (U711). It is initialized by 103.D2; after 16 clocks the display enable (U711, Pin 15) carry is output. This latches the counter by removing the count enable (U711, Pin 7) and the carry remains set until the next 103.D2 synchronizing pulse.

3.15.2 When display enable is not set, the bit counter and display register are controlled by preshift if required, and the magnifier and the dot inhibit is disabled. When display enable is on the bit counter and display register are controlled by the magnifier.

3.16 PRESHIFTER.

3.16.1 In Zoom mode >1 magnification the first visible bit displayed on a line may not be on a word boundary since Panning operates on bit boundaries. The preshifter preshifts the memory word loaded in the display register at 103.D2 to the specified bit position- prior to the first visible dot time. The preshift may be from 0 to 15 bits.

3.16.2 The latch (U310) is loaded with the 1's complement of the preshift bit number. At 103.D2 the latching counter (U410) is initialized it then increments until the carry output is set, at this time the state of the display register and bit counter remains static until the first visible display dot (U711-15 carry output).

3.17 MAGNIFIER.

3.17.1 In Zoom mode the vertical magnification is obtained by the M-controller reading a line a number of times equal to the magnification and blanking the last line. The horizontal magnification is obtained by the magnifier repeating each memory bit a number of times equal to the magnification and then blanking the last bit.

3.17.2 The magnifier consists of a variable modulus counter (U311). It is initialized at 103.D2 and is enabled by display enable during the visible display region. At this time the counter increments until the carry output appears (U311, Pin 15). The bit counter is then count enabled for one clock, the magnifier counter re-initialized, and the shift logic enabled to shift the display register one clock.

The modulus of the counter in the magnifier may be changed from 1 to 16 by loading the 2's complement of the magnification in the latch (U411). Therefore the ratio between memory bits and display bits may be changed over the same range.

4.0 TEST POINTS.

The principle timing signals on the Graphics Display Module are 103.D2 (TP3) and $\overline{\text{LOAD}}$ (TP4). 103.D2 may be used as a synchronizing reference point for observing memory and display operation. $\overline{\text{LOAD}}$ may be used to observe the M-controller/ graphics display handshake (figure 4).

4.1 MARCHING VECTOR SELF TEST.

The marching vector self test "built-in" to the Graphics Terminal is analogous to a "marching 1's and 0's" memory diagnostic. However, unlike a normal memory diagnostic, the operation can be directly viewed. It verifies that the graphics memory and M-controller are operational.

In other words, it verifies that the M-controller vector generator operates in all quadrants and that the graphic display memory contains 259,200 uniquely addressable points which can be set to 1 or 0.

Since malfunctions in the M-controller or Graphics Display PCA's may result in a memory pack error message, the failed RAM should be interchanged with another and self test rerun to confirm a RAM chip failure.

4.2 ADDRESS TEST.

The integral memory receivers may be connected to the display register by grounding $\overline{TP1}$ ADDR. This displays the column address of the memory word in the position on the terminal display normally occupied by the memory data associated with that word as follows:

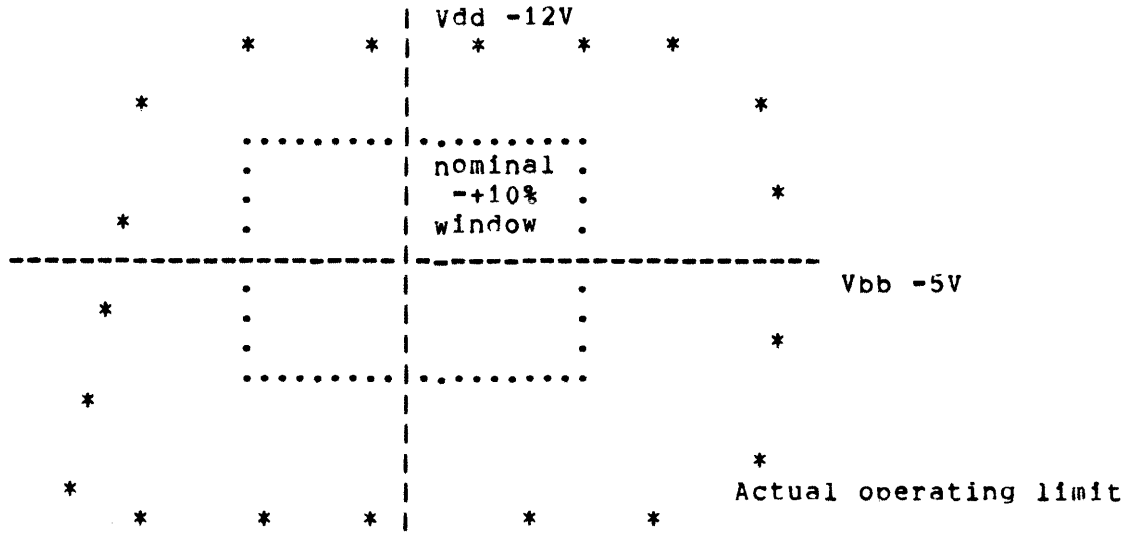
DISPLAY WORD															
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
				l	r	l	r								
				$\overline{RAS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{CAS}$	$\overline{DIN}$	A6	A5	A4	A3	A2	A1	A0
0	0	0	0												

This test may be used to verify that the M-controller / Graphics Display Module handshake operates and also verify the memory drivers are operational.

4.3 SCHMOO TEST*

Provision is made for disconnecting the Vbb -5V Zener regulator to run a schmoo test (jumper). The external -5V supply is connected to the -5V test point in the memory section.

* The following represents a typical plot of a system while running a diagnostic.



Example only.

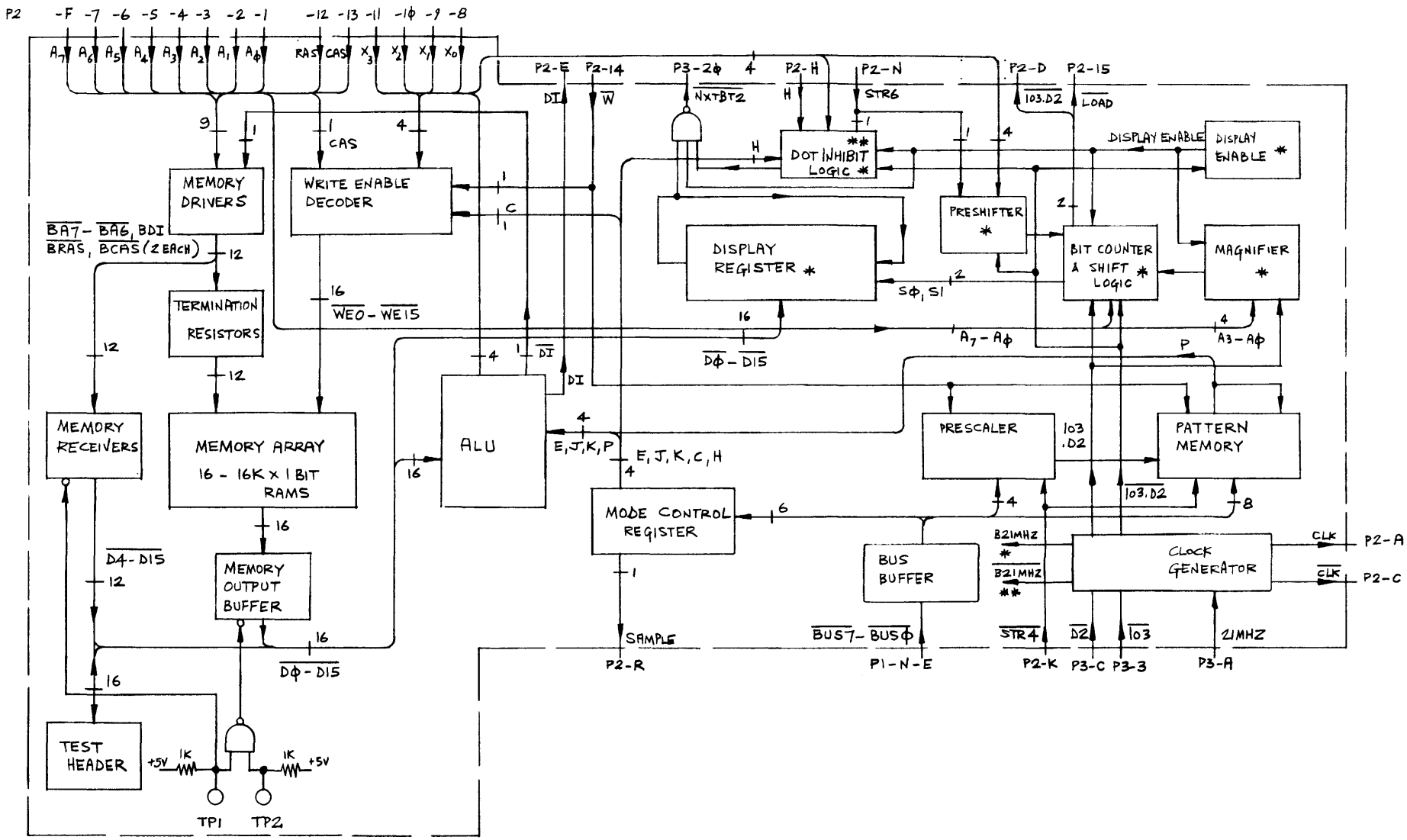


Figure 1
Graphics Display PCA Block Diagram
DEC-12-77 **13255-91126**

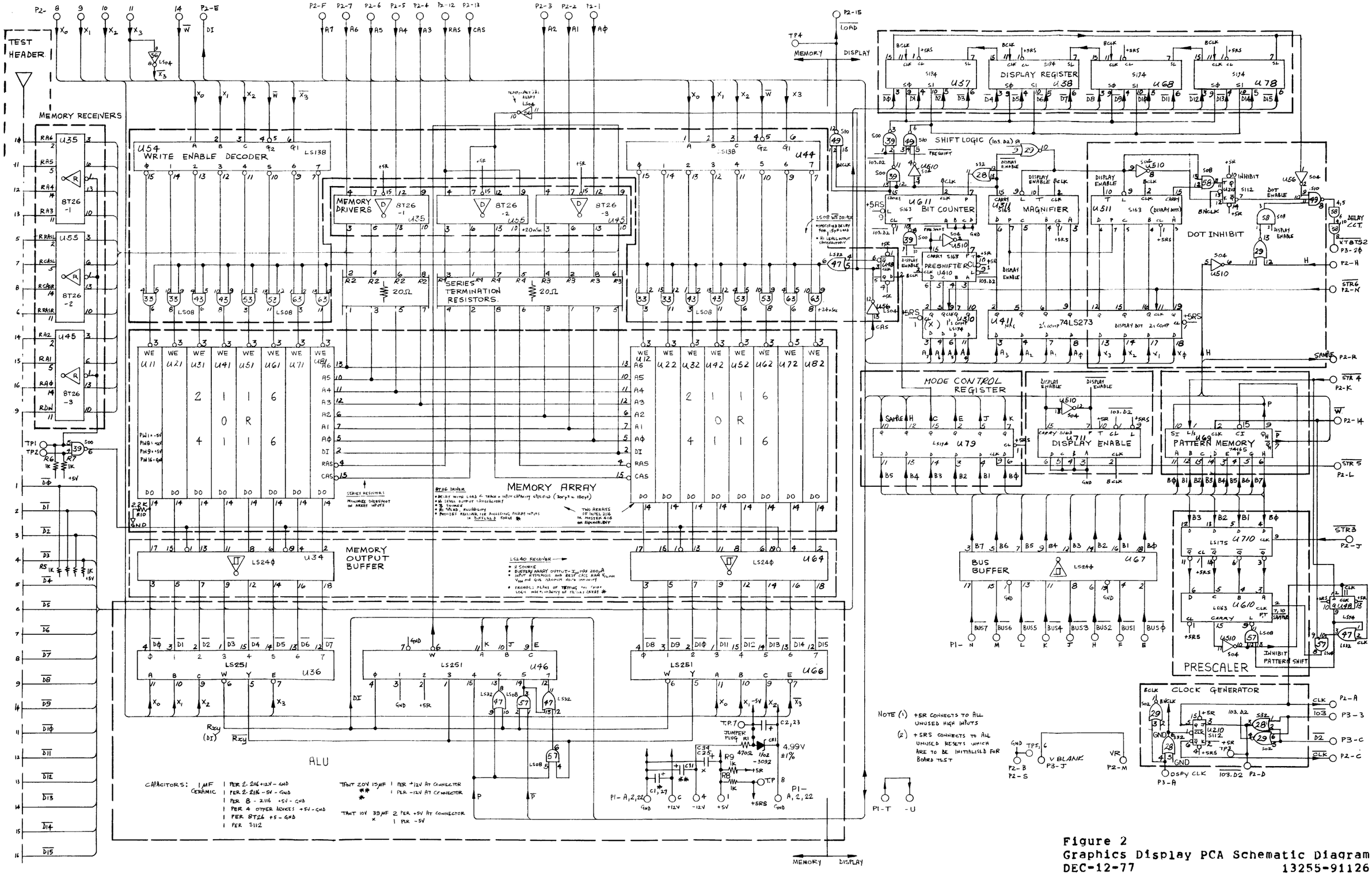
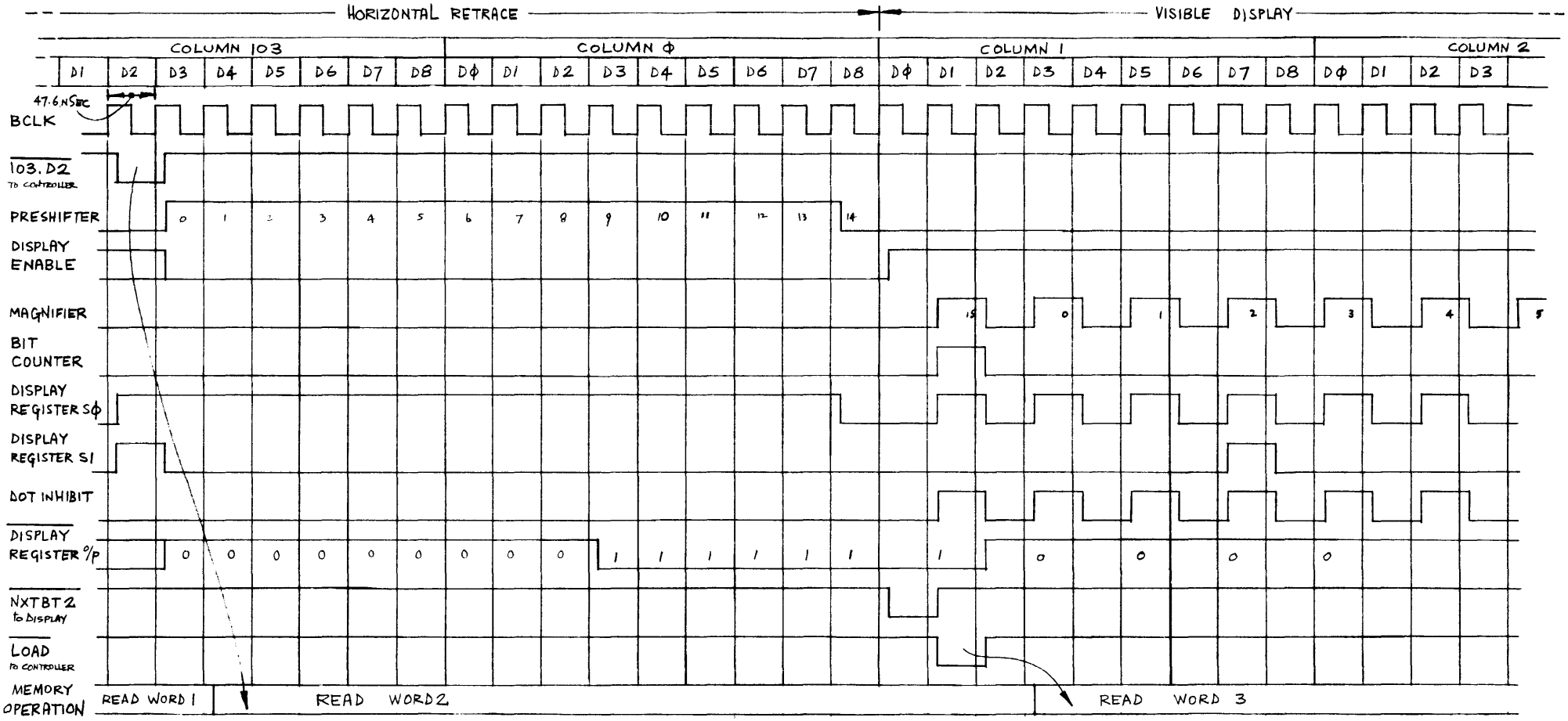


Figure 2
Graphics Display PCA Schematic Diagram
DEC-12-77 **13255-91126**



TYPICAL OPERATION OF DISPLAY TIMING

THE TIMING SHOWS THE FIRST WORD OF THE ADDRESS TEST (ΦΦΦ177B OR, ΦΦΦΦΦΦΦΦΦ111111)

ZOOM MAGNIFICATION = 2
START DISPLAY AT BIT 14

Figure 3
Graphics Display PCA Display Timing Diagram
DEC-12-77 13255-91126

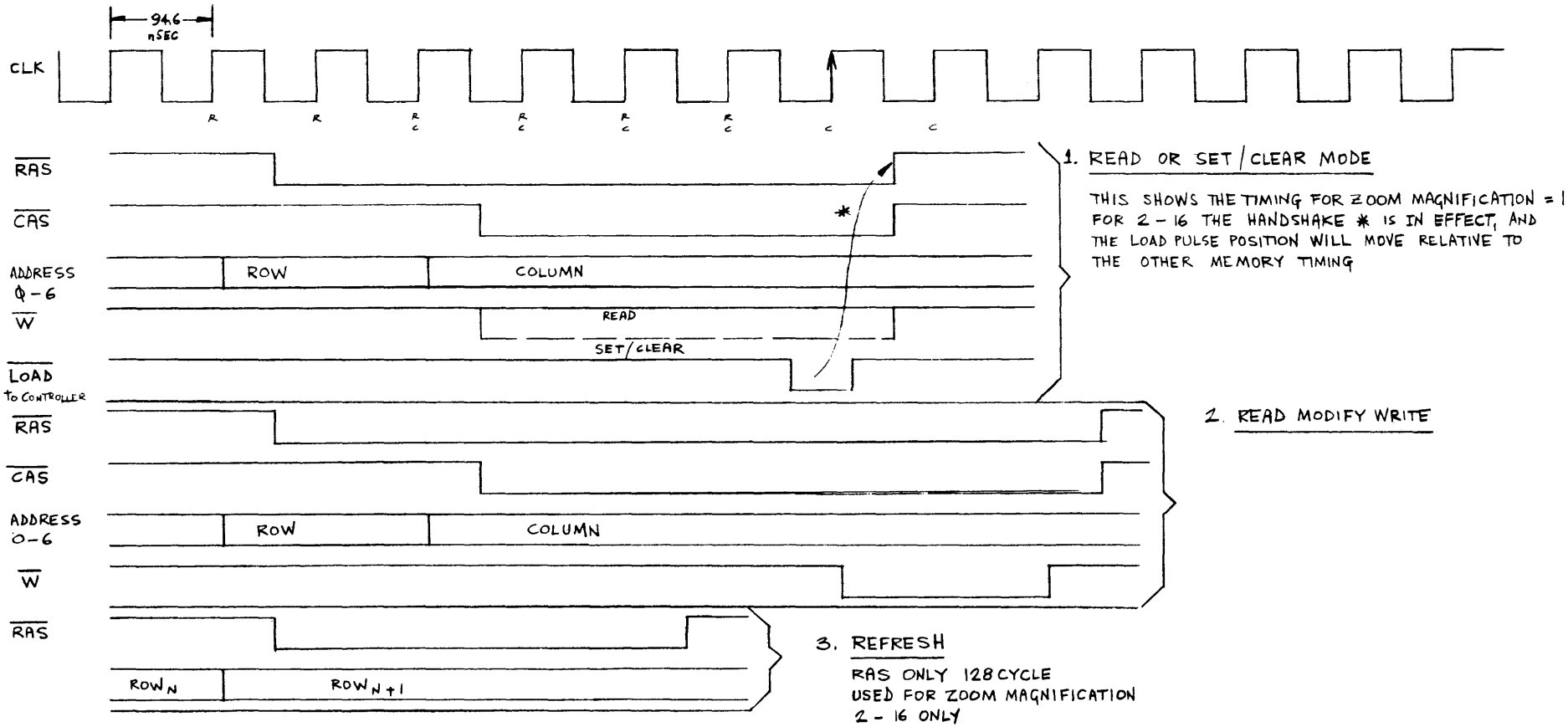


Figure 4
Graphics Display PCA Memory Timing Diagram
DEC-12-77 **13255-91126**

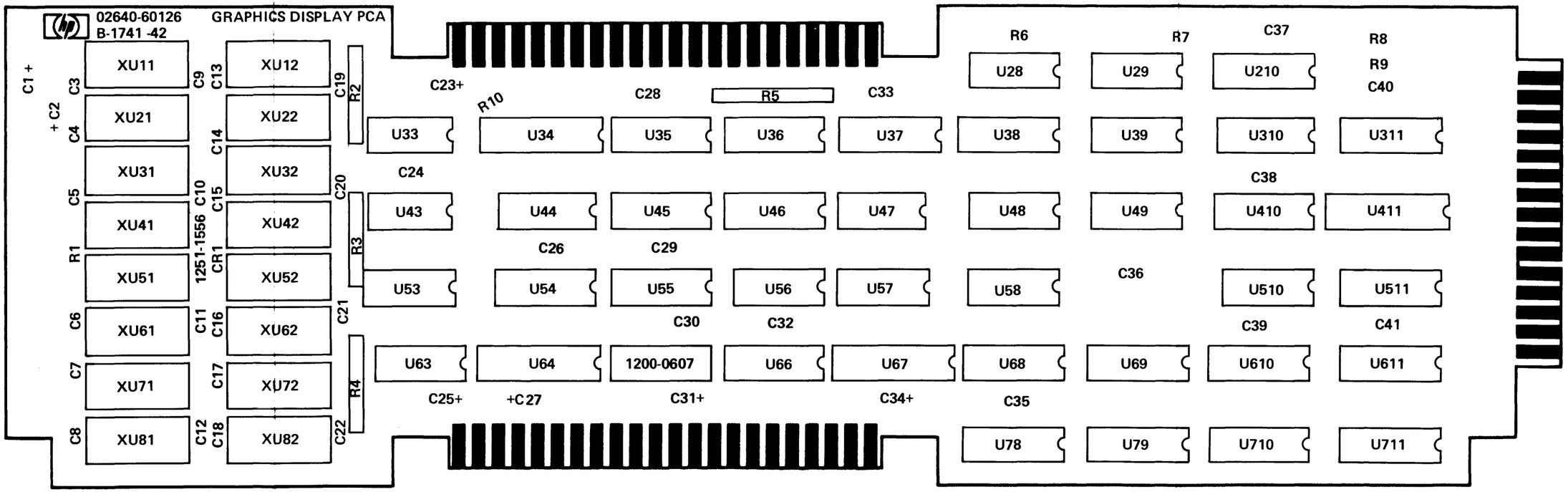


Figure 5
Graphics Display PCA Component Location Diagram
DEC-12-77 13255-91126

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60022	1	CONNECTOR (4) ASSEMBLY		
	0403-0347	4	BUMPER RUBBER		
	1251-1887	4	CONN PC 2 x 22.156D		

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60016	1	CONNECTOR (5) ASSEMBLY		
	0403-0347	4	RUBBER BUMPER		
	1251-1887	5	CONN PC 2 x 22.156D		

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60126	1	ASSEMBLY GRAPHICS DISPLAY		
			DATE CODE: B-1741-42		
C1	0180-1746	1	CAPACITOR 15uF 10%		
C2	0180-0393	1	CAPACITOR 39uF 10V		
C3 thru C22	0160-0127	20	CAPACITOR 1uF 25V 20%		
C23	0180-0393	1	CAPACITOR 39uF 10V		
C24	0150-0121	1	CAPACITOR 0.1uF		
C25	0180-0393	1	CAPACITOR 39uF 10V		
C26	0150-0121	1	CAPACITOR 0.1uF		
C27	0180-1746	1	CAPACITOR 15uF 10%		
C28 thru C30	0150-0121	3	CAPACITOR 0.1uF		
C31	0180-1746	1	CAPACITOR 15uF 10%		
C32 thru C33	0150-0121	2	CAPACITOR 0.1uF		
C34	0180-0393	1	CAPACITOR 39uF 10V		
C35 thru C41	0150-0121	7	CAPACITOR 0.1uF		
E1 thru E8	0360-0124	8	STUD SOLDER TERM		
R1	0683-4715	1	RESISTOR 470 5% .25		
R2 thru R4	1810-0322	3	RESISTOR PACK SIP		
R5	1810-0030	1	RESISTOR NETWORK 7 x 1K		
R6 thru R9	0683-1025	4	RESISTOR 1000 5% .25		
R10	0683-2225	1	RESISTOR 2200 5% .25		
CR1	1902-3092	1	DIODE Zener 4.99V		
U11 thru U12	5090-0114	2	16K RAM		
U21 thru U22	5090-0114	2	16K RAM		
U28	1820-1449	1	IC SN74S32N		
U29	1820-1322	1	IC SN74S02N		
U31 thru U32	5090-0114	2	16K RAM		
U33	1820-1201	1	IC SN74LS08N		
U34	1820-1917	1	IC SN74LS240N		
U35	1820-1081	1	IC N8T26B		
U36	1820-1298	1	IC SN74LS251N		
U37 thru U38	1820-1304	2	IC SN74S194N		
U39	1820-0681	1	IC SN74S00N		
U41 thru U42	5090-0114	2	16K RAM		
U43	1820-1201	1	IC SN74LS08N		
U44	1820-1216	1	IC SN74LS138N		
U45	1820-1081	1	IC N8T26B		
U46	1820-1298	1	IC SN74LS251N		
U47	1820-1208	1	IC SN74LS32N		
U48	1820-1112	1	IC SN74LS74N		
U49	1820-0685	1	IC SN74S04N		
U51 thru U52	5090-0114	2	16K RAM		
U53	1820-1201	1	IC SN74LS08N		
U54	1820-1216	1	IC SN74LS138N		
U55	1820-1081	1	IC N8T26B		
U56	1820-0683	1	IC SN74S04N		
U57	1820-1201	1	IC SN74LS08N		
U58	1820-1367	1	IC SN74S08N		
U61 thru U62	5090-0114	2	16K RAM		
U63	1820-1201	1	IC SN74LS08N		
U64	1820-1917	1	IC SN74LS240N		
U66	1820-1298	1	IC SN74LS251N		
U67	1820-1917	1	IC SN74LS273N		
U68	1820-1304	1	IC SN74S194N		
U69	1820-1042	1	IC SN74165N		
U71 thru U72	5090-0114	2	16K RAM		
U78	1820-1304	1	IC SN74S194N		
U79	1820-1196	1	IC SN74LS174N		
U81 thru U82	5090-0114	2	16K RAM		
U210	1820-0629	1	IC SN74S112N		
U310	1820-1196	1	IC SN74LS174N		
U311	1820-1453	1	IC SN74S163N		
U410	1820-1453	1	IC SN74S163N		
U411	1820-1730	1	IC SN74LS273N		
U511	1820-1453	1	IC SN74S163N		
U610	1820-1432	1	IC SN74LS163N		
U611	1820-1453	1	IC SN74S163N		
U710	1820-1195	1	IC SN74LS175N		
U711	1820-1453	1	IC SN74S163N		
U510	1820-0683	1	IC SN74S04N		

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60194	1	CONNECTOR ASSEMBLY		
	0380-0007	4	SPACER- RND .438LG		
	0403-0347	1	BUMPER RUBBER		
	1251-1886	2	CONN PC 2 x 15.156D		
	1251-4339	2	KEY-PLZG .040THK		
	2190-0851	4	LKWASHER 6 HEL		
	2420-0003	4	NUT 6-32 .250AF		
	02640-00073	1	HANDLE CONN		