HP 13255

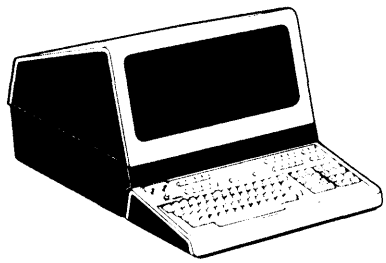
ASYNCHRONOUS DATA COMM MODULE

Manual Part No. 13255-91086

PRINTED

AUG-01-76

DATA TERMINAL
TECHNICAL INFORMATION



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1.0 INTRODUCTION.

The Asynchronous Data Comm PCA along with an interface cable assembly comprise the Asynchronous Data Comm Module and provide a communication link between the terminal and an external computer.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Asynchronous Data Comm Module is contained in tables 1.0 through 5.3.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60043	103/202 Cable Assembly	N/A	N/A
02640-60058	12531/12880 Cable Assembly	N/A	N/A
02640-60059	RS232C Cable Assembly	N/A	N/A
02640-60077	Test Hood Assembly	N/A	N/A
02640-60086	Asynchronous Data Comm PCA	12.9 x 4.0 x 0.5	0.38
02640-60131	US Modem Cable Assembly	N/A	N/A
02645-60002	DC Self Test Hood	N/A	N/A

Number of Backplane Slots Required: 1

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NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

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Number of Backplane Slots Required: 1

Table 2.0 Reliability and Environmental Information

Environmental: (X) HP Class B ( ) Other:
Restrictions: Type tested at product level
Failure Rate: 0.484 (percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	-42 Volt Supply
@ 100 mA	@ 40 mA	@ 80 mA	@ mA NOT APPLICABLE
115 volts ac @ A NOT APPLICABLE		220 volts ac @ A NOT APPLICABLE	
Clock Frequency: 4.915 MHz +/-0.1%			

Table 4.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
- 2	GND	Ground Common Return (Power and Signal)
- 3	SYS CLK	4.915 MHz System Clock
- 4	-12V	-12 Volt Power Supply
- 5		Not used
- 6		
- 7		
- 8		
- 9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10	$\overline{\text{ADDR5}}$	Negative True, Address Bit 5
-11	$\overline{\text{ADDR6}}$	Negative True, Address Bit 6
-12		Not used
-13		
-14	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-15	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-16	$\overline{\text{ADDR11}}$	Negative True, Address Bit 11
-17		Not used
-18		
-19		
-20		
-21	$\overline{\text{I/O}}$	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal)

Table 4.0 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B		Not Used
-C	+12V	+12 Volt Power Supply
-D	PWR ON	System Power On
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-H	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-J	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-K	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-L	$\overline{\text{BUS5}}$	Negative True, Data Bus Bit 5
-M	$\overline{\text{BUS6}}$	Negative True, Data Bus Bit 6
-N	$\overline{\text{BUS7}}$	Negative True, Data Bus Bit 7
-P	$\overline{\text{WRITE}}$	Negative True, Write/Read Type Cycle
-R		} Not
-S		} Used
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V		}
-W		} Not Used
-X		}
-Y	$\overline{\text{REQ}}$	Negative True, Request (Bus Data Currently Valid)
-Z	$\overline{\text{ATN}}$	Negative True, Data Comm Interrupt Request

Table 4.1 Connector Information

Connector and Pin No.	Signal Name	Signal Description *NOTE: Signals with an asterisk below are TTL levels and should not be connected to RS232C drivers.
P2, Pin 1 through P2, Pin 14		Not Used
P2, Pin 15	TEST*	Special Test Point - Preset Baud Rate Counters
P2, Pin A	GND	Terminal Logic Ground
-B	BA	Serial Data Out
-C	BB	Serial Data In
-D	CA	Request to Send
-E	CB	Clear to Send
-H	AB	Signal Ground
-J	CF	Receiver Carrier
-K	X8 CLK*	External x8 Baud Rate Clock Out
-L	X16 OUT*	External x16 Baud Rate Clock Out
-M	SA	Secondary Channel Transmit
-N	SB	Secondary Channel Receive
-P	CD	Data Terminal Ready
-S	X16 IN*	External x16 Baud Rate Clock In

Table 5.0 Module Bus Pin Assignments

Function Performed: Output Control Register Bits

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (0001)

Function Specifier: ADDR 5 = 0
ADDR 6 = 1

Data Bus Bit Interpretation:

B7 Not Used

B6 0 = No Break
1 = Break (SA is high, BA is low)

B5 0 = Parity Enable
1 = Parity Disable

B4 0 = Odd Parity
1 = Even Parity

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
0	ADDR 10
0	ADDR 9
X	ADDR 8
X	ADDR 7
1	ADDR 6
0	ADDR 5
1	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Transmit/Receive Baud Rate

	X16 IN	110*	150	300	1200	2400	4800	9600
B3	0	1	0	1	0	1	0	1
B2	0	0	1	1	0	0	1	1
B1	0	0	0	0	1	1	1	1

*Selects two stop bits.

B0 0 = CA is on
1 = CA is off

Table 5.1 Module Bus Pin Assignments

Function Performed: Input Received Data Character	Value	Bus Signal
	X	ADDR 15
Poll Bit: Not Applicable	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (0001)	X	ADDR 12
	0	ADDR 11
	0	ADDR 10
	0	ADDR 9
Function Specifier: ADDR 5 = 0	X	ADDR 8
ADDR 6 = 0	X	ADDR 7
	0	ADDR 6
	0	ADDR 5
	1	ADDR 4
	X	ADDR 3
	X	ADDR 2
Data Bus Bit Interpretation:	X	ADDR 1
	X	ADDR 0
B7 Receive Data Bit 7	B7	BUS 7
(Equals 0 if parity is selected, otherwise	B6	BUS 6
is equal to most signficant data bit)	B5	BUS 5
B6 Receive Data Bit 6	B4	BUS 4
	B3	BUS 3
	B2	BUS 2
B5 Receive Data Bit 5	B1	BUS 1
	B0	BUS 0
B4 Receive Data Bit 4	1=Logical 1=Bus Low	
	0=Logical 0=Bus High	
	X=Don't Care	
B3 Receive Data Bit 3		
B2 Receive Data Bit 2		
B1 Receive Data Bit 1		
B0 Receive Data Bit 0		

Table 5.2 Module Bus Pin Assignments

Function Performed: Output data character for transmission

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (0001)

Function Specifier: ADDR 5 = 1
ADDR 6 = 1

Data Bus Bit Interpretation:

B7 Transmit Data Bit 7 } If Parity is Enabled Bit 7 is replaced by proper parity.

B6 Transmit Data Bit 6

B5 Transmit Data Bit 5

B4 Transmit Data Bit 4

B3 Transmit Data Bit 3

B2 Transmit Data Bit 2

B1 Transmit Data Bit 1

B0 Transmit Data Bit 0

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
0	ADDR 10
0	ADDR 9
X	ADDR 8
X	ADDR 7
1	ADDR 6
1	ADDR 5
1	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 5.3 Module Bus Pin Assignments

Function Performed: Input module status byte

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (0001)

Function Specifier: ADDR 5 = 1
ADDR 6 = 0

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
0	ADDR 10
0	ADDR 9
X	ADDR 8
X	ADDR 7
0	ADDR 6
1	ADDR 5
1	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Data Bus Bit Interpretation:

B7 Always 0

B6 Secondary Channel Receive (SR)

B5 Clear to Send (CB)

B4 Carrier (CF)

B3 0 = No Parity Error
1 = Parity Error

B2 0 = No Overrun
1 = Overrun Error

Overrun and parity errors are set/reset after each character is received.

B1 0 = Transmit Holding Register Full
1 = Transmit Holding Register Empty

Transmit holding register is made "0" by outputting a data character for transmission.

B0 0 = No Data Received
1 = Data Received

Data received is made "0" by inputting a received data character (see table 5.1).

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), component location diagram (figure 3), and parts lists (02640-60043, 02640-60058, 02640-60059, 02640-60077, 02640-60086, 02640-60131, and 02645-60002) located in the appendix.

The Asynchronous Data Comm Module is the primary interface between the terminal and external data processing equipment. It provides character parallel data, status, and control information to the terminal microprocessor by way of firmware control. Individual characters are sent and received bit-serial and character-serial using an EIA RS232C electrical interface. The PCA can be connected to external data processing equipment directly or by modem depending on the interface cable assembly used. The module functional groups consist of the universal asynchronous receiver/transmitter (UART), bus decoder logic, control logic, baud rate generator, RS232C drivers, and RS232C receivers.

3.1 UART.

3.1.1 The UART is Western Digital's TR1602B and is the key element of the module. It accepts a parallel character from the terminal data bus, appends the necessary asynchronous character formatting and parity bits, and transmits the information serially at a rate determined by an input clock. The UART has a master reset input for power on initialization, control inputs and status outputs for firmware control of the interface, and clock inputs for determining the serial data bit rate. The UART receives serial data, deletes the start and stop framing bits, optionally checks incoming parity, and outputs a parallel character.

3.1.2 The UART (U24), provides all control logic and data storage necessary to implement an asynchronous parallel-to-serial (transmit) and serial-to-parallel (receive) converter. It has control inputs to determine character size and formatting, including an optional parity bit (generated on output and checked on input). The UART has status outputs for determining when the UART can accept another parallel character for transmission or for indicating that a character has been received and is ready for input. The UART has transmit and receive clock inputs which are clocked at 16 times the desired baud rate.

3.1.2.1 There are five control inputs (Pins 35, 39, 36, 37, and 38) for the UART which define character format and parity. The character size is always eight bits with the optional even or odd parity being placed in the most significant bit of the character when selected. If 110 baud is the bit rate used, an extra stop bit is added to the asynchronous character formatting. When transmitted, each character will consist of a start bit, eight data bits (optional parity) least significant bit first, and one or two (110 baud) stop bits.

3.1.2.2 Characters to be transmitted are loaded into the UART by $\overline{\text{DATA STROBE}}$. This output command from the bus decoder circuit strobes data into the UART using input THRL (Transmit Holding Register Load) at Pin 23. This causes the THRE (Transmit Holding Register Empty) at Pin 22 output to go low and remain false until the character in the buffer is transferred into the UART's serial output shifter. The character in the buffer is transferred to the shifter when the shifter is empty or has completed the previous character and the THRE output goes true again. Data bits and format bits (start, stop, and parity) are shifted out of the UART at TRO (Transmitter Register Output) at Pin 25 according to the inputs from the control logic. Each individual bit takes 16 transmit clocks to be shifted out.

3.1.2.3 The UART uses the RRC (Receiver Clock) signal at Pin 17 to sample the RI input (Receive Serial In) at Pin 20 for an asynchronous start bit. When it detects a valid start bit, the UART begins shifting data (16 clocks per bit) into the receive serial shifter. When the character is completed, the UART removes the asynchronous format bits (start and stop) transfers the character in parallel to UART outputs Pins 5 through 12 and sets DR (Data Received) at Pin 19 high. When one character is received, the UART updates two status bits, PE (Parity Error) at Pin 13 and OE (Overrun Error) at Pin 15. PE is set high only when odd or even parity is selected by the control logic and the input character had the incorrect parity. OE is set high when the UART has already received a character, DR (Pin 19) is high and a new character is loaded into it. When Data Input (U37, Pin 2) is decoded, the UART data outputs are gated onto the terminal bus and DRR (Data Received Reset) at Pin 18 is pulse, setting DR (Pin 19) low. The UART is then ready for another character.

3.2 BUS DECODER LOGIC.

3.2.1 The bus decoder logic provides the interface for the module and includes module address decoding and input and output enable signals. Module address and data bus control signals determine when the PCA will input (Processor Read) data or control and when it will output (Processor Write) data or status.

3.2.2 The address of the Asynchronous Data Comm PCA is determined by two logic gates, (U58, Pin 6 and U48, Pin 10). These connect to the terminal address lines ($\overline{\text{ADDR11}}$, $\overline{\text{ADDR10}}$, $\overline{\text{ADDR9}}$ and $\overline{\text{ADDR4}}$). The module is further addressed by inputs from the terminal bus to a 1-of-8 decoder (U42), which samples $\overline{\text{WRITE}}$, $\overline{\text{ADDR6}}$, and $\overline{\text{ADDR5}}$ with $\overline{\text{REQ}}$ and $\overline{\text{I/O}}$ enabling the decoder.

3.2.2.1 The normal bus addressing sequence is for all of the module address information to be placed on the terminal data bus and allowed to become stable. Then $\overline{\text{REQ}}$ which is the final enabling signal (execute or strobe command) is set true (low). This creates one of the following output strobes from the 1-of-8 decoder (U42): $\overline{\text{DATA STROBE}}$ (U42, Pin 15), $\overline{\text{CONTROL LOAD}}$ (U42, Pin 14), STATUS INPUT (U37, Pin 12), and DATA INPUT (U37, Pin 2).

3.2.2.2 Data output from the UART and interface status are available to the terminal data bus through buffers (U16, U17, U26, and U27). The two input commands (STATUS INPUT and DATA INPUT) enable status or data to be gated onto the terminal data bus. During a data input, DR at U24, Pin 19 is set while the data is gated to the terminal bus.

3.3 CONTROL LOGIC.

3.3.1 The control logic circuit is loaded from the terminal data bus by a microprocessor output command. There are seven bit positions which control interface signals, define UART controls, and select the data in/out bit rate (baud rate).

3.3.2 The control register is program loaded and consists of seven bits (U22 and one-half of U38). The inputs to the control register are $\overline{\text{BUS0}}$ through $\overline{\text{BUS6}}$. The control information is loaded into the register by $\overline{\text{CONTROL LOAD}}$ (U42, Pin 14). (Refer to table 5.0 for definition of control register bits.)

3.3.2.1 The three baud rate select bits (CB3, CB2, and CB1) go to the multiplexer and determine which part of the divider chain or if the X16 IN clock is to be used as the bit rate clock. The baud rate select code for 110 baud is detected by two gates (U48, Pin 13 and U58, Pin 8) indicating two stop bits to the UART control and enabling the preset function of the divider chain to obtain 110 baud.

3.3.2.2 The Break flip-flop controls DATA OUT by making it high without regard to data being transmitted from the UART. $\overline{\text{BREAK}}$ is used by the terminal for remote interrupt to data processing equipment. If the Break flip-flop is not set, data is treated normally by the RS232C driver.

3.4 BAUD RATE GENERATOR.

3.4.1 The baud rate generator defines bit timing during transmit and receive operations. It consists of a 12-bit counter chain and a multiplexer which selects one of eight possible baud rates. The counter chain divides the terminal data bus System Clock (SYS CLK) down into useable baud rate frequencies.

3.4.2 Three counters (U510, U410, and U59) and an eight-input multiplexer (U49) comprise the baud rate generator. Seven of the baud rates are generated from the terminal System Clock and the eighth is an external input. As outputs, the PCA generates external signals equal to the baud rate times sixteen and times eight (TTL level signals).

3.4.2.1 The three counters generate six baud rates directly by dividing System Clock by factors of two. The other baud rate (110 baud) is not directly derived by dividing by two. The select code for 110 baud is detected (U48, Pin 13 and U58, Pin 2) and a preset function is enabled when the counter chain overflows (U59, Pin 15). A constant is parallel-loaded into the last two counters (U59 and U410), which perform a divide by

175 instead of 256. This gives the transmit and receive clocks (X16) necessary for that baud rate (the frequency is exactly 1755 +/-1 Hz).

Baud Rate Summary

Baud Rate Select Bits Control Register 3	2	1	Baud Rate	Frequency (Hz)	System Clock (Divide by)
1	1	1	9600	153,600	32
1	1	0	4800	76,800	64
1	0	1	2400	38,400	128
1	0	0	1200	19,200	256
0	1	1	300	4,800	1024
0	1	0	150	2,400	2048
0	0	1	110	1,755	2800
0	0	0	External Clock In (max 10000)	(max 160 kHz)	-

3.4.2.2 The three baud rate select bits from the control logic go to a multiplexer (U49) in the baud rate generator. Seven of the baud rates are generated by the counter chain, the eighth is the $\overline{\text{X16 IN}}$ clock (U39, Pin 11) which can be no greater than 160 kHz (10,000 baud) and TTL specification levels. One output of the multiplexer goes to the UART clocks and the other to a buffer which provides a TTL level X16 baud rate clock (X16 OUT) at P2, Pin L. Flip-flop (U38, Pin 8) divides the baud rate clock to provide an external TTL level X8 Clock (X8 CLK) at P2, Pin K.

3.5 RS232C DRIVERS.

3.5.1 The interface between the Asynchronous Data Comm Module and external devices conforms to the EIA RS232C standard, which specifies electrical and logical operation, interface limitation, and defines the signal functions. The RS232C interface allows the PCA and thus the terminal to be connected locally to data processing equipment or to modems for remote operation using the telephone network. The RS232C drivers provide serial data out and three control outputs.

3.5.2 The interface signals are available at the PCA rear connector (P2) for connection to a cable assembly. The RS232C voltage outputs are signals converted from TTL levels (+5 volts and ground) by integrated circuit driver (U28).

The REQUEST TO SEND output comes directly from the control logic at U22, Pin 7 and is used in modem applications to begin a transmit operation. The DATA TERMINAL READY output is always high (+12 volts) when the terminal power is on. Secondary Channel Transmit (SA) is used on Bell 202 or equivalent data sets and is high unless the Break flip-flop (U38, Pin 6) is low or REQUEST TO SEND is low. Capacitors C4, C5, and C6 are used for slew rate control.

3.6 RS232C RECEIVERS. The RS232C receivers also meet the EIA standard and provide DATA IN and three control inputs. The RS232C inputs are converted to TTL levels by integrated circuit receiver (U18). Capacitors C7, C8, C9, and C10 on the input receivers are used for noise suppression. DATA IN (BB), is converted to TTL levels by the receiver and goes directly to the UART. Three inputs (CF, CB, and SB) are provided for modem status monitoring by the terminal processor.

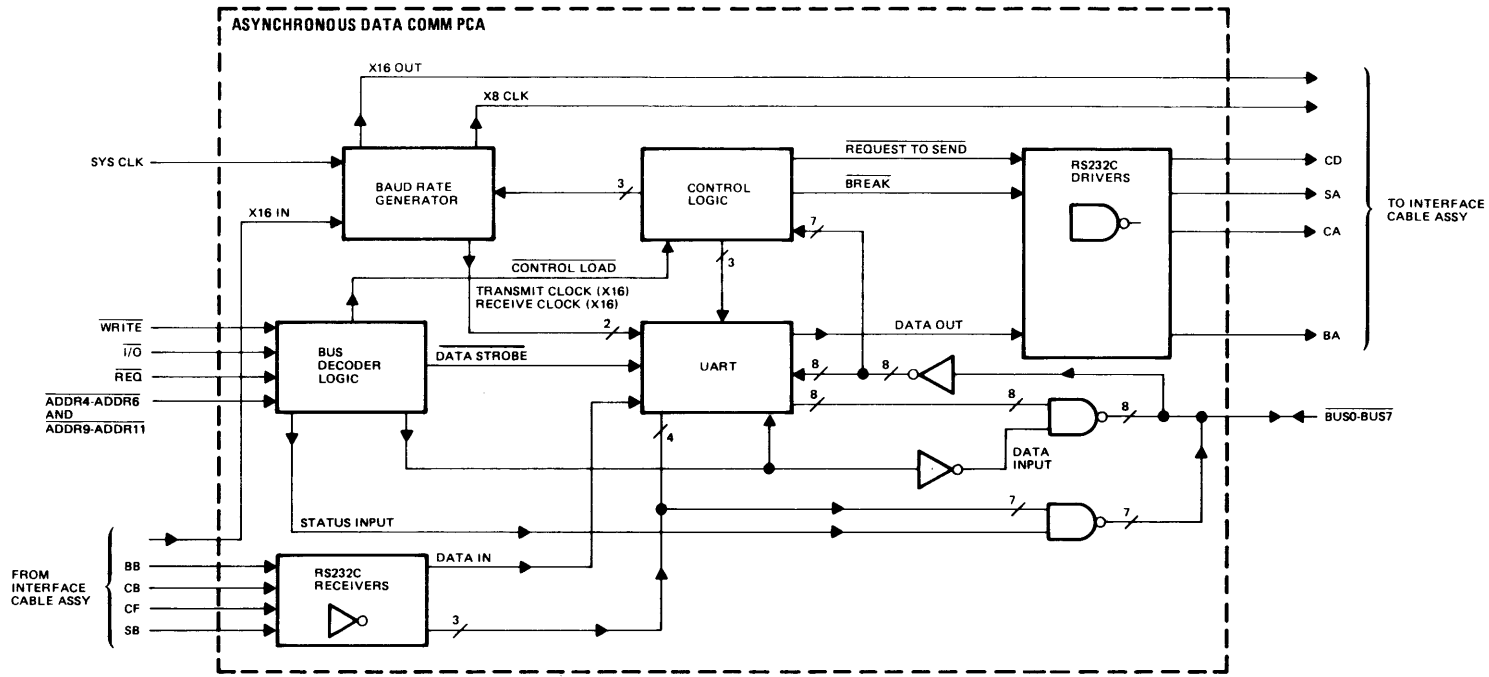

Figure 1
Asynchronous Data Comm Block Diagram
AUG-01-76 13255-91086

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60086	1	A-SYNC DATA COMM ASSEMBLY DATE CODE: A-1518-22 REVISION DATE: 04-15-76	28480	02640-60086
C1	0180-0393	1	CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C2	0160-2055	6	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C3	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C4	0160-3456	7	CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3456
C5	0160-3456		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3456
C6	0160-3456		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3456
C7	0160-3456		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3456
C8	0160-3456		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3456
C9	0160-3456		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3456
C10	0160-3456		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3456
C11	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C12	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C13	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C14	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
CR1	1901-0040	2	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR2	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
E1	0360-0124	1	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
R1	0683-1025	1	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R2	0683-4705	1	RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
U16	1820-1209	4	IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U17	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U18	1820-0990	1	IC-DIGITAL MC1489AL DTL QUAD NAND	04713	MC1489AL
U22	1820-1196	1	IC-DIGITAL SN74LS174N TTL LS HEX	01295	SN74LS174N
U24	1820-1219	1	IC-DIGITAL TR1602B TTL*	0026W	TR1602B
U26	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U27	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U28	1820-0509	1	IC-DIGITAL MC1488L DTL QUAD LINE	04713	MC1488L
U36	1820-1199	2	IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U37	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U38	1820-1112	1	IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
U39	1820-1056	1	IC-DIGITAL SN74132N TTL QUAD 2 NAND	01295	SN74132N
U42	1820-1216	1	IC-DIGITAL SN74LS138N TTL LS 3	01295	SN74LS138N
U48	1820-1074	1	IC-DIGITAL SN74128N TTL QUAD 2 NOR	01295	SN74128N
U49	1820-1217	1	IC-DIGITAL SN74LS151N TTL LS 8	01295	SN74LS151N
U58	1820-1202	1	IC-DIGITAL SN74LS10N TTL LS TPL 3 NAND	01295	SN74LS10N
U59	1820-0778	3	IC-DIGITAL 93L16DC TTL L BIN SYNCHRO	07263	93L16DC
U410	1820-0778		IC-DIGITAL 93L16DC TTL L BIN SYNCHRO	07263	93L16DC
U510	1820-0778		IC-DIGITAL 93L16DC TTL L BIN SYNCHRO	07263	93L16DC
	4330-0145		BEADS, INDIAN	28480	4330-0159

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60043	1	103/202 CABLE ASSEMBLY REVISION DATE: 03-31-76	28480	02640-60043
	0624-0098	2	SCREW-TPG 4-40 .438-IN-LG PAN-HD-POZI	28480	0624-0099
	1251-0159	1	CONNECTOR-PC EDGE 15-CONT/ROW 2-ROWS	71785	251-15-30-261
	1251-0352	1	CABLE BUSHING-CIRC STD CONN	71468	CA18220-6
	1251-2417	1	CONNECTOR 25-PIN M D SERIES	71468	D8C-25P-F0
	1251-3253	11	CONTACT-CONN MALE CRP .04-IN-CONT-SZ	71468	030-1952-002
	1251-3320	2	ACCESSORY-SUBMIN D CONN	71468	018-5000-167
	1251-3328	2	ACCESSORY-SUBMIN D CONN	71785	423-42-22-022
	1251-4339	1	POLARIZING KEY-PC EDGE CONN	28480	1251-4339
	2190-0078	2	WASHER-LK HLCL NO.-4 .115-IN-ID	28480	2190-0078
	2200-0149	1	SCREW-MACH 4-40 .625-IN-LG PAN-HD-POZI	28480	2200-0149
	2200-0757	2	SCREW-MACH 4-40 .688-IN-LG PAN-HD-POZI	28480	2200-0757
	2220-0010	2	SCREW-MACH 4-40 .5-IN-LG FIL-HD-SLT	28480	2220-0010
	2260-0001	2	NUT-HEX-DBL-CHAM 4-40-THD .094-THK	28480	2260-0002
	2260-0002	1	NUT-HEX-DBL-CHAM 4-40-THD .062-THK	28480	2260-0005
	3030-0009	1	SCREW-SET 6-32 .375-IN-LG SMALL CUP-PT	28480	3030-0009
	8120-1903		CA 15X 26 GA UL	28480	8120-1927
	5040-6003	1	CLAMP	28480	5040-6003
	5040-6072	1	MOUNTING BLOCK	28480	5040-6072
	5040-6086	1	HOOD, CONNECTOR	28480	5040-6086

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60058	1	12531 CABLE ASSEMBLY REVISION DATE: 05-15-76	28480	02640-60058
	0624-0098	4	SCREW-TPG 4-40 .438-IN-LG PAN-HD-POZI	28480	0624-0099
	0850-0312		TUBING-HS .25-D/.125-RCVD .025-WALL	06090	RNF-100-1/4-BLK
	0850-0706		TUBING-HS .093-D/.046-RCVD .02-WALL	06090	RNF-100-3/32-BLK
	1251-0159	1	CONNECTOR-PC EDGE 15-CONT/ROW 2-ROWS	71785	251-15-30-261
	1251-0335	1	CONNECTOR-PC EDGE 24-CONT/ROW 2-ROWS	28480	1251-0335
	1251-4339	1	POLARIZING KEY-PC EDGE CONN	28480	1251-4339
	2200-0091	1	SCREW-MACH 4-40 .562-IN-LG PAN-HD-POZI	28480	2200-0091
	2200-0149	1	SCREW-MACH 4-40 .625-IN-LG PAN-HD-POZI	28480	2200-0149
	2260-0002	2	NUT-HEX-DBL-CHAM 4-40-THD .062-THK	28480	2260-0005
	3030-0009	1	SCREW-SET 6-32 .375-IN-LG SMALL CUP-PT	28480	3030-0009
	3030-0143	1	SCREW-SET 6-32 .5-IN-LG SMALL CUP-PT ALY	28480	3030-0143
	8120-1856		CABLE-SHLD 22AWG 5-CNDCT JGK-JKT .27-OD	28480	8120-1856
	8150-2344		WIRE 24AWG BK 300V PVC 7X32 80C	28480	8150-2344
	5040-6004	2	CLAMP, CABLE, SMALL	28480	5040-6004
	5040-6071	1	HOOD, CONNECTOR	28480	5040-6071
	5040-6072	2	MOUNTING BLOCK	28480	5040-6072
	5040-6086	1	HOOD, CONNECTOR	28480	5040-6086

Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60059	1	RS232C CABLE ASSEMBLY REVISION DATE: 03-26-76	28480	02640-60059
	0624-0098	2	SCREW-TPG 4-40 .438-IN-LG PAN-HD-POZI	28480	0624-0098
	1251-0159	1	CONNECTOR-PC EDGE 15-CONT/ROW 2-ROWS	71785	251-15-30-261
	1251-0352	1	CABLE BUSHING-CIRC STD CONN	71468	CA18220-6
	1251-2416	1	CONNECTOR 25-PIN F D SERIES	71468	DBC-25S-F0
	1251-3251	12	CONTACT-CONN FEM CRP .04-IN-CONT-SZ	71468	030-1953-002
	1251-3320	2	ACCESSORY-SUBMIN D CONN	71468	018-5008-167
	1251-3328	2	ACCESSORY-SUBMIN D CONN	71785	423-42-22-022
	1251-4339	1	POLARIZING KEY-PC EDGE CONN	28480	1251-4339
	2190-0078	2	WASHER-LK HLCL NO.-4 .115-IN-ID	28480	2190-0078
	2200-0010	2	SCREW-MACH 4-40 .75-IN-LG RD-HD-SLT	28480	2200-0010
	2200-0091	1	SCREW-MACH 4-40 .562-IN-LG PAN-HD-POZI	28480	2200-0091
	2200-0757	2	SCREW-MACH 4-40 .688-IN-LG PAN-HD-POZI	28480	2200-0757
	2260-0001	2	NUT-HEX-DBL-CHAM 4-40-THD .094-THK	28480	2260-0002
	2260-0002	1	NUT-HEX-DBL-CHAM 4-40-THD .062-THK	28480	2260-0005
	3030-0143	1	SCREW-SET 6-32 .5-IN-LG SMALL CUP-PT ALY	28480	3030-0143
	8120-1903		CABLE-UNSHLD 26AWG 15-CNDCT JGK-JKT	28480	8120-1927
	8150-2344		WIRE 24AWG 8K 300V PVC 7X32 80C	28480	8150-2344
	5040-6003	1	CLAMP	28480	5040-6003
	5040-6072	1	MOUNTING BLOCK	28480	5040-6072
	5040-6086	1	HOOD, CONNECTOR	28480	5040-6086

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60077	1	TEST HOOD ASSEMBLY REVISION DATE: 03-26-76	28480	02640-60077
	0624-0098	2	SCREW-TPG 4-40 .438-IN-LG PAN-HD-POZI	28480	0624-0099
	1251-0159	1	CONNECTOR-PC EDGE 15-CONT/ROW 2-ROWS	71785	251-15-30-261
	2200-0149	1	SCREW-MACH 4-40 .625-IN-LG PAN-HD-POZI	28480	2200-0149
	2260-0002	1	NUT-HEX-DBL-CHAM 4-40-THD .062-THK	28480	2260-0005
	3030-0009	1	SCREW-SET 6-32 .375-IN-LG SMALL CUP-PT	28480	3030-0009
	8150-2344		WIRE 24AWG BK 300V PVC 7X32 80C	28480	8150-2344
	5040-6004	1	CLAMP, CABLE, SMALL	28480	5040-6004
	5040-6072	1	MOUNTING BLOCK	28480	5040-6072
	5040-6086	1	HOOD, CONNECTOR	28480	5040-6086

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60131	1	MODEM CABLE ASSEMBLY REVISION DATE: 09-10-76	28480	02640-60131
	0624-0098	2	SCREW-TPG 4-40 .438-IN-LG PAN-HD-POZI	28480	0624-0099
	1251-0159	1	CONNECTOR-PC EDGE 15-CONT/ROW 2-ROWS	71785	251-15-30-261
	1251-2417	1	CONNECTOR 25-PIN M D SERIES	71468	DBC-25P-F0
	1251-3253	16	CONTACT-CONN MALE CRP .04-IN-CONT-SZ	71468	030-1952-002
	1251-3320	2	ACCESSORY-SUBMIN D CONN	71468	018-5000-167
	1251-3328	2	ACCESSORY-SUBMIN D CONN	71785	423-42-22-022
	1251-4339	1	POLARIZING KEY-PC EDGE CONN	28480	1251-4339
	2190-0078	2	WASHER-LK HLCL NO.-4 .115-IN-ID	28480	2190-0078
	2200-0149	1	SCREW-MACH 4-40 .625-IN-LG PAN-HD-POZI	28480	2200-0149
	2200-0757	2	SCREW-MACH 4-40 .688-IN-LG PAN-HD-POZI	28480	2200-0757
	2220-0010	2	SCREW-MACH 4-40 .5-IN-LG FIL-HD-SLT	28480	2220-0010
	2260-0001	2	NUT-HEX-DBL-CHAM 4-40-THD .094-THK	28480	2260-0002
	2260-0002	2	NUT-HEX-DBL-CHAM 4-40-THD .062-THK	28480	2260-0005
	3030-0143	1	SCREW-SET 6-32 .5-IN-LG SMALL CUP-PT ALY	28480	3030-0143
	8120-1930		CABLE-UNSHLD 26AWG 18-CNDCT JGK-JKT	28480	8120-1930
	5040-6003	1	CLAMP	28480	5040-6003
	5040-6072	1	MOUNTING BLOCK	28480	5040-6072
	5040-6086	1	HOOD, CONNECTOR	28480	5040-6086
	0890-0291		TBG HS BLK .375D		

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02645-60002	1	DC SELF TEST ASSEMBLY REVISION DATE: 09-10-76	28480	02645-60002
	0624-0099	2	SCREW-TPG 4-40 .438-IN-LG PAN-HD-POZI	28480	0624-0099
	0890-0855		TUBING-HS .046-D/.023-RCVD .016-WALL	92194	FIT-221-3/64 CLEAR
	1251-0159	1	CONNECTOR-PC EDGE 15-CONT/ROW 2-ROWS	71785	251-15-30-261
	1251-4339	1	POLARIZING KEY-PC EDGE CONN	28480	1251-4339
	1901-0040	2	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
	2200-0091	1	SCREW-MACH 4-40 .562-IN-LG PAN-HD-POZI	28480	2200-0091
	2260-0002	1	NUT-HEX-DBL-CHAM 4-40-THD .062-THK	28480	2260-0005
	3030-0009	1	SCREW-SET 6-32 .375-IN-LG SMALL CUP-PT	28480	3030-0009
	8150-2344		WIRE 24AWG BK 300V PVC 7X32 80C	28480	8150-2344
	5040-6003	1	CLAMP	28480	5040-6003
	5040-6072	1	MOUNTING BLOCK	28480	5040-6072
	5040-6086	1	HOOD, CONNECTOR	28480	5040-6086

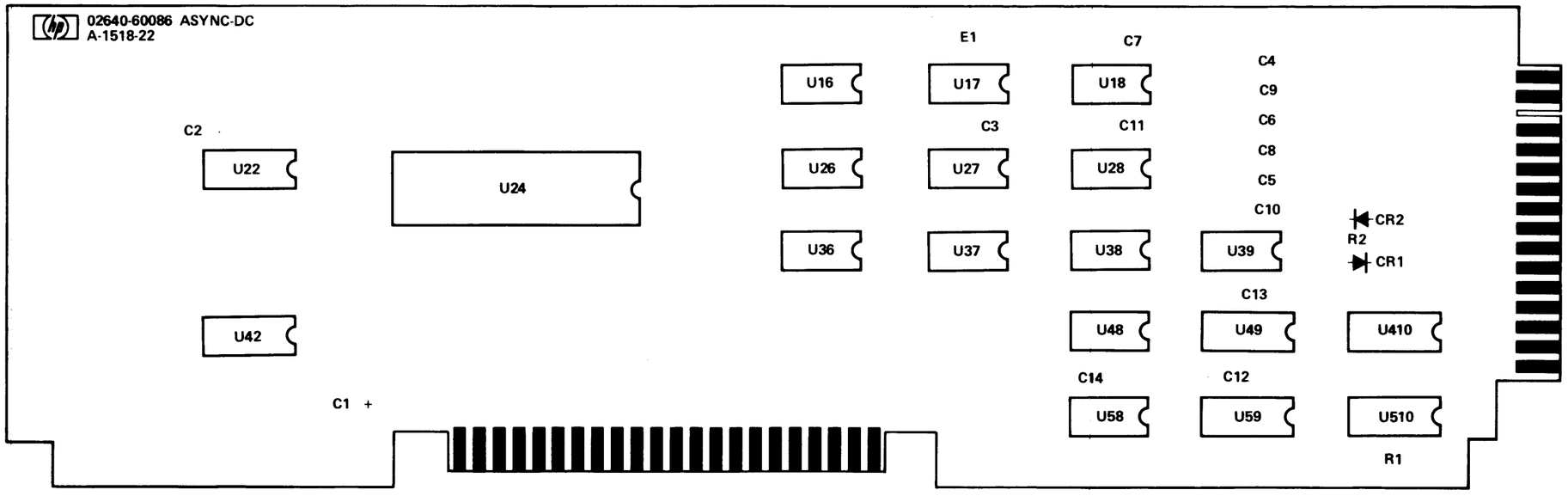

Figure 3
Asynchronous Data Comm PCA Component Location Diagram
AUG-01-76 13255-91086

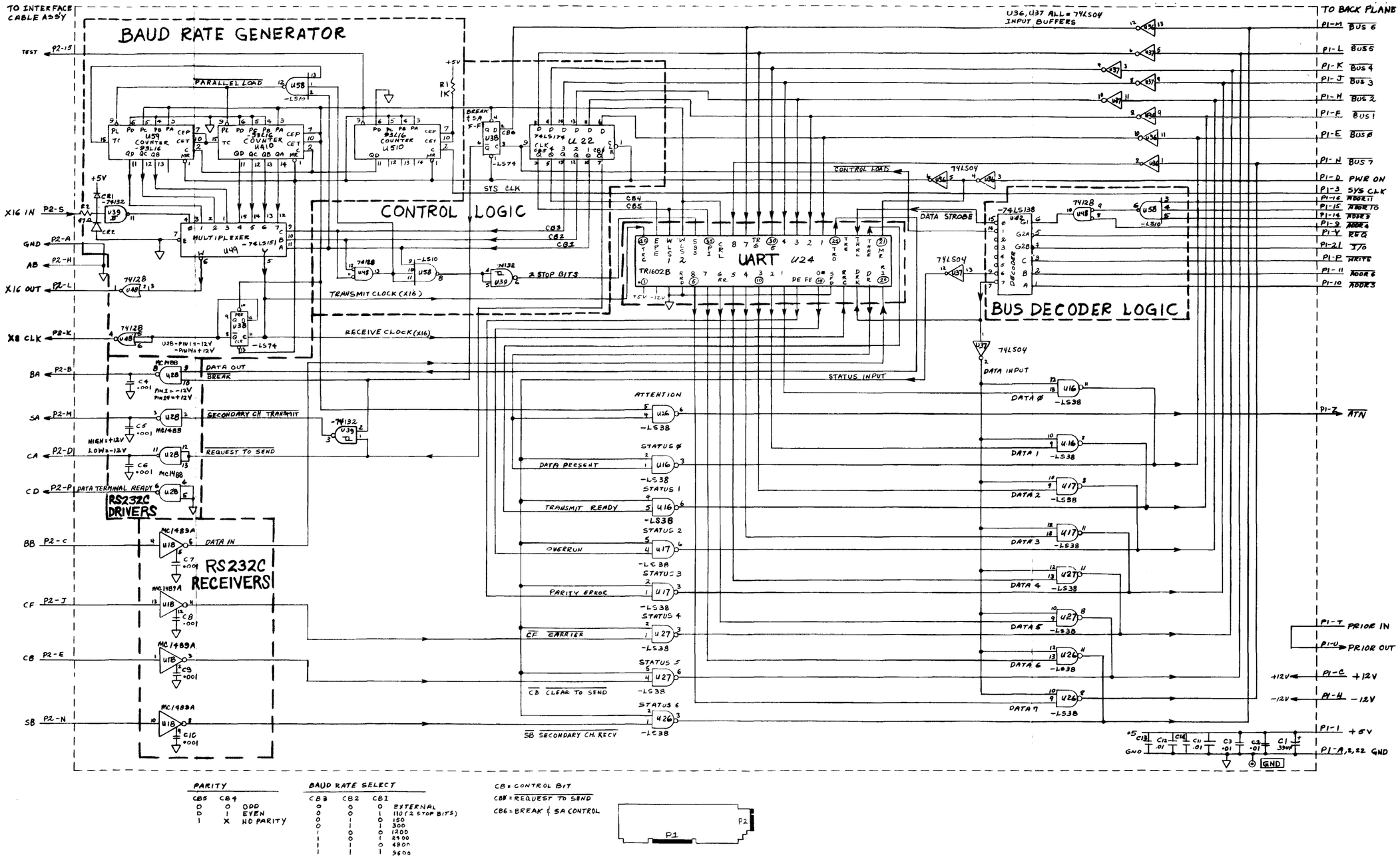

Figure 2
Asynchronous Data Comm PCA Schematic Diagram
AUG-01-76 13255-91086