HP 13255

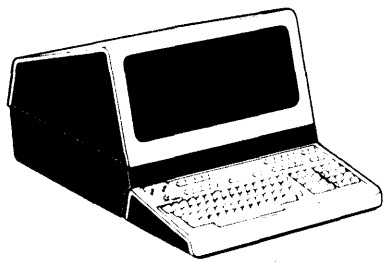
DISPLAY EXPANSION MODULE

Manual Part No. 13255-91024

REVISED

SEP-06-77

DATA TERMINAL
TECHNICAL INFORMATION



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1.0 INTRODUCTION.

The Display Expansion Module provides three additional display enhancements to the display subsystem: underline, half-bright, and blinking fields. It also adds the capability for supporting up to three alternate 128-character sets of either the alphanumeric or microvector type. All timing and control signals for the module are received from the Display Controller Module.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Display Expansion Module is contained in tables 1.0 through 6.0.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60022	Top Plane Connector Ass'y	N/A	N/A
02640-60024	Display Enhancement PCA	12.9 x 4.0 x 0.5	0.44
Number of Backplane Slots Required: 1			

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NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

1.0 INTRODUCTION.

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Number of Backplane Slots Required: 1			

Table 2.0 Reliability and Environmental Information

Environmental:	(X) HP Class B ( ) Other:
Restrictions:	Type tested at product level
Failure Rate:	1.094 (percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	-42 Volt Supply
@ 350 mA	@ mA	@ 22 mA	@ mA
	NOT APPLICABLE		NOT APPLICABLE

115 volts ac	220 volts ac
@ A	@ A
NOT APPLICABLE	NOT APPLICABLE

Clock Frequency: 21.06 MHz

Table 4.0 Jumper Definitions

PCA Designation	Function	
	In	Out
W1	Alternate Character Set 1 contains 128 Characters	Alternate Character Set 1 contains 64 Characters
W2	Alternate Character Set 1 is of the alphanumeric type	Alternate Character Set 1 is of the microvector type
W3	Alternate Character Set 2 contains 128 Characters	Alternate Character Set 2 contains 64 Characters
W4	Alternate Character Set 2 is of the alphanumeric type	Alternate Character Set 2 is of the microvector type
W5	Alternate Character Set 3 contains 128 Characters	Alternate Character Set 3 contains 64 Characters
W6	Alternate Character Set 3 is of the alphanumeric type	Alternate Character Set 3 is of the microvector type

Table 5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2		Not Used
-3		
-4	-12V	-12 Volt Power Supply
P1, Pin 5 through Pin 22		Not Used
P1, Pin A	GND	Ground Common Return (Power and Supply)
-B		Not Used
-C		
-D	PWR ON	System Power On
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F		Not Used
-H	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-J	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-K	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-L	$\overline{\text{BUS5}}$	Negative True, Data Bus Bit 5
P1, Pin M through Pin S		Not Used
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
P1, Pin V through Pin Z		Not Used

Table 5.1 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P2, Pin 1	GND	Ground
-2	LC0	Scan Line Counter Bit 0
-3	LC2	Scan Line Counter Bit 2
-4	BIT0	ASCII Bit 0
-5	BIT4	ASCII Bit 4
-6	BIT2	ASCII Bit 2
-7	BIT5	ASCII Bit 5
-8	$\overline{\text{BSS1}}$	Negative True, Buffered Set Select Bit 1
-9		Not Used
-10		
-11	$\overline{\text{DBIT1}}$	Negative True, Dot 1 Output
-12	$\overline{\text{DBIT3}}$	Negative True, Dot 3 Output
-13	$\overline{\text{DBIT5}}$	Negative True, Dot 5 Output
-14	$\overline{\text{DBIT7}}$	Negative True, Dot 7 Output
-15	GND	Ground

Table 5.1 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P2, Pin A	GND	Ground
-B	LC1	Scan Line Counter Bit 1
-C	LC3	Scan Line Counter Bit 3
-D	BIT6	ASCII Bit 6
-E	BIT3	ASCII Bit 3
-F	BIT1	ASCII Bit 1
-H	$\overline{\text{BSS0}}$	Negative True, Buffered Set Select Bit 0
-J		Not Used
-K		Not Used
-L	$\overline{\text{DBIT0}}$	Negative True, Dot 0 Output
-M	$\overline{\text{DBIT2}}$	Negative True, Dot 2 Output
-N	$\overline{\text{DBIT4}}$	Negative True, Dot 4 Output
-P	$\overline{\text{DBIT6}}$	Negative True, Dot 6 Output
-P	$\overline{\text{DBIT8}}$	Negative True, Dot 8 Output
-S	GND	Ground

5.2 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P3, Pin 1	D0	Negative True, Character Dot Position 0
-2		Not Used
-3	103	Negative True, Column Count 103
-4	BUFCLK	Enhancement Buffer Clock
-5	D1	Negative True, Character Dot Position 1
-6		} Not
-7		} Used
-8	EVEN	Even Row
-9	LBLOAD	Bus Buffer Load
-10		} Not
-11		} Used
-12	BBL	Negative True, Buffered Blink
-13		Not Used
-14	BUL	Negative True, Buffered Underline
-15	BUF HLF BRT	Negative True, Buffered Half-Bright
-16	BSS0	Negative True, Buffered Set Select Bit 0
-17	BSS1	Negative True, Buffered Set Select Bit 1
-18	81	Negative True, Column Count 81
-19		} Not
-20		} Used
-21	LOAD	Line Buffer Load
-22	XBITS1	Negative True, External Bit Stream 1

Table 5.2 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P3, Pin A	DSPY CLK	21.060 MHz Display Clock
-B	GND	Ground
-C		Not Used
-D	$\overline{D8}$	Negative True, Character Dot Position 8
-E	$\overline{14}$	Negative True, Scan Line Counter Reset
-F		Not Used
-H	VRTCLK	Scan Line Counter Clock
-J		Not Used
-K	OCIRC	Line Buffer Circulation
-L	OCIRCEN	Line Buffer Circulation Enable
-M	INTSET	Display Controller Interrupt
-N		Not Used
-P	$\overline{BIT0}$	Negative True, ASCII Bit 0
-R	$\overline{BIT1}$	Negative True, ASCII Bit 1
-S	$\overline{BIT2}$	Negative True, ASCII Bit 2
-T	$\overline{BIT3}$	Negative True, ASCII Bit 3
-U	$\overline{BIT4}$	Negative True, ASCII Bit 4
-V	$\overline{BIT5}$	Negative True, ASCII Bit 5
-W	$\overline{BIT6}$	Negative True, ASCII Bit 6
-X		Not Used
-Y	GND	Ground
-Z		Not Used

Table 6.0 Module Bus Pin Assignments

Function Performed: Put Data Bits B0, B2, B3, B4, and B5 Into Holding Register	Value	Bus Signal
	N/A	ADDR 15
Poll Bit: Not Applicable	N/A	ADDR 14
	N/A	ADDR 13
Module Address: Not Applicable	N/A	ADDR 12
	N/A	ADDR 11
	N/A	ADDR 10
	N/A	ADDR 9
Function Specifier: Not Applicable	N/A	ADDR 8
	N/A	ADDR 7
	N/A	ADDR 6
	N/A	ADDR 5
	N/A	ADDR 4
Data Bus Bit Interpretation: The data bits (B0, B2, B3, B4, and B5) are loaded under DMA control.	N/A	ADDR 3
	N/A	ADDR 2
	N/A	ADDR 1
	N/A	ADDR 0
B7: Not Used	B7	BUS 7
	B6	BUS 6
	B5	BUS 5
B6: Not Used	B4	BUS 4
	B3	BUS 3
	B2	BUS 2
	B1	BUS 1
B5: Holds the Set Select Bit 1	B0	BUS 0
	1=Logical 1=Bus Low	
	0=Logical 0=Bus High	
B4: Holds the Set Select Bit 0	X=Don't Care	
B3: Holds the Half-Bright Feature		
B2: Holds the Underline Feature		
B1: Not Used		
B0: Holds the Blink Feature		

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), timing diagram (figure 3), component location diagram (figure 4), and parts lists (02640-60022 and 02640-60024) located in the appendix.

The Display Expansion Module provides the additional display control word width and thus supports the three additional display features and the two set select bits. The module receives all of its timing and control information from the Display Controller Module and is slaved to it. The Display Expansion Module functions as an adjunct to the minimum display subsystem. The module's output consists of an external bit stream ($\overline{\text{XBITS1}}$) display enhancement control lines $\overline{\text{BUL}}$, $\overline{\text{BUF HLF BRT}}$, and $\overline{\text{BBL}}$, and the two set select lines $\overline{\text{BSS0}}$ and $\overline{\text{BSS1}}$. Electrically, its line buffers operate in parallel with those on the Display Memory Access (DMA) PCA.

3.1 REFRESH AND LOAD LOGIC.

3.1.1 The refresh and load logic drives the clock and control lines of the line buffers. In addition, the logic toggles the line buffers and sends to each one the appropriate clock signals and recirculate commands.

3.1.2 The refresh and load logic controls the line buffers and the dual two-line-to-one-line multiplexer. Its input signals are the circulation clock for the line buffers (the logical AND of OCIRC and OCIRCEN) and the LOAD signal from the Display Memory Access PCA. OCIRC is a continuous circulation signal gated into bursts of 80 pulses by OCIREN. The EVEN signal controls the multiplexer. When it is high, the DMA controls the clock lines of line buffers U42 and U22. Simultaneously, the display controller circulates the previously loaded information in line buffers U41 and U21 fifteen times, via the OCIRC signal. At the end of the fifteenth scan line of the row, EVEN changes state, the INTSET signal clears the holding register, and the roles of the pairs of line buffers are reversed.

3.2 HOLDING REGISTER.

3.2.1 The holding register (U31 and U51) is a 5-bit register which stores the display enhancement and set select bits received from the data bus.

3.2.2 Information in the holding register is strobed in by means of LBLOAD under controls of the DMA PCA. The information is buffered and subsequently available for entry into the off-screen line buffer (as determined by the EVEN signal). At the end of a row (end of the fifteenth scan line), INTSET clears out the holding register before a new row is started by the DMA PCA.

3.3 LINE BUFFERS.

3.3.1 The line buffer block consists of two pairs of shift registers (U21, U41, and U22, U42) which hold the underline, half-bright, and blinking enhancement bits along with the two set select bits. They are toggled by the Display Control PCA, each one alternately being loaded by the DMA PCA from the terminal data bus and then cycled 15 times for display on the CRT.

3.3.2 The two line buffers are each 5 bits by 80 bits in length. They operate in parallel with the line buffers on the DMA PCA and, therefore, expand the display control word width by five bits. The line buffers are toggled by the EVEN signal. While one line buffer is being recirculated fifteen times by OCIRC, the other is being loaded by the DMA PCA via LOAD. The outputs of the line buffers are routed to U11 and U32 which act as a five channel two-line-to-one-line multiplexer with latching outputs. The circulated line buffer is selected by EVEN and is loaded into the latch during character dot position 1 ($\overline{D1}$). The output of the latch then consists of the three display enhancement signals, HBEN, ULEN, BLEN and the two buffered set select bits, $\overline{BSS0}$ and $\overline{BSS1}$. The signals appear character synchronously with the corresponding ASCII from the DMA PCA.

3.4 64/128 CHARACTER SET.

3.4.1 Two 1024-word by 8-bit bipolar ROMs comprise one 128-character alphanumeric type character set. The 128-character microvector sets utilize two 1024-word by 9-bit ROMs.

3.4.2 Each 64-character alphanumeric character set is encoded into a 1024-word by 8-bit bipolar ROM. A 128-character set requires two ROMs. In the case of microvector type character sets, each 64-character set is encoded in a 1024-word by 9-bit ROM. Both types of ROMs have identical pinouts. The alphanumeric ROMs have an additional CHIP ENABLE pin which corresponds to an output line on the microvector ROMs.

3.5 CHARACTER SET DECODER.

3.5.1 The character set decoder selects the two buffered set select bits, $\overline{BSS0}$ and $\overline{BSS1}$, to enable the three alternate character sets.

3.5.2 The character set decoder selects $\overline{BSS0}$ as the LSB and $\overline{BSS1}$ as the MSB. The three output lines of U47 are negative true. As a character set is enabled, the corresponding ROM sockets are enabled via the $\overline{E1}$ signal at U210, U310, U410, U29, U39, and U49, Pins 21. If the base set (SET0) is utilized, then $\overline{BSS0}$ and $\overline{BSS1}$ are both high and the character ROMs on the Display Control PCA are enabled.

3.6 CHARACTER SET ENCODER.

3.6.1 The character set encoder's output signal reflects the state of the Set-Type Jumper (W2, W4, or W6) of the alternate character set being currently addressed by buffered set select bits $\overline{BSS0}$ and $\overline{BSS1}$.

3.6.2 The SHIFT ENABLE (U28, Pin 7) signal controls the shifter logic. When the selected set is of the alphanumeric type, $\overline{DBIT0}$ functions as the half-shift control bit. When the selected set is of the microvector type, then $\overline{DBIT0}$ and $\overline{DBIT8}$ are mapped into dot position 0 and 8 respectively.

3.7 CHARACTER SELECT LOGIC.

3.7.1 The character select logic is set up by means of Jumpers W1, W3, and W5 (each alternate character set to be either 64- or 128-characters in length). It also enables the appropriate upper case or lower case character ROM depending on the ASCII code from the DMA PCA being processed.

3.7.2 This logic selects which ROM of the selected set will be enabled. When $\overline{\text{BIT5}}$ and $\overline{\text{BIT6}}$ of the incoming ASCII are both high or both low, then the characters correspond to the control codes (00-37B) or lower case characters (140-177B) respectively. Otherwise, they are upper case characters (40-137B).

When the character select Jumpers W1, W3, and W5 are installed (128 characters), then the corresponding upper case ROM is enabled when $\overline{\text{BIT5}}$ and $\overline{\text{BIT6}}$ are the same. When the character set select jumpers are removed (64 characters), then the upper case ROM is disabled only when both $\overline{\text{BIT5}}$ and $\overline{\text{BIT6}}$ are high. This causes lower case codes to be upshifted to their respective upper case characters and control codes to display nothing.

3.8 SCAN LINE COUNTER.

3.8.1 The scan line counter is a local modulo 15 counter synchronized to the scan line counter on the Display Control PCA. It provides a local source of the four scan line count bits required by the character ROMs.

3.8.2 The scan line counter (U48) is a 4-bit synchronous counter driven by VRTCLK from the Display Control PCA logic. Every 15 lines, it is reset by $\overline{14}$. This forces the counter to sequence from a count of 0 to 14. The four output lines of the counter form the four least significant bits of the ROM address, the six most significant bits being the incoming ASCII codes.

3.9 SHIFTER LOGIC.

3.9.1 The shifter logic block generates the Shift Clock signal applied to the parallel-to-serial converter. It accepts the $\overline{\text{DBIT0}}$ signal from the character ROMs and if the accessed character set is of the alphanumeric type, it generates half-shifted clock signals. If the set is of the microvector type, the shifter logic accepts the $\overline{\text{DBIT8}}$ and inserts it into the serial bit stream along with $\overline{\text{DBIT0}}$.

3.9.2 The shifter logic generates the SHFT (U34, Pin 6) signal which clocks the parallel-to-serial converter. The logic is controlled by both $\overline{\text{DBIT0}}$ and the $\overline{\text{SHIFT ENABLE}}$ signal. When the selected character set is of the alphanumeric type, $\overline{\text{SHIFT ENABLE}}$ and SHIFT ENABLE at U36, Pin 6 allow the half-shift control bit ($\overline{\text{DBIT0}}$ of the character ROMs) to influence the shifter into U38, Pin 9. When the selected character set is of the microvector type, then $\overline{\text{DBIT0}}$ is interpreted as a data bit.

Shift pulses can occur on either the leading edge of the display clock (half-shifted) or on the trailing edge (not half-shifted), depending on the state of $\overline{\text{DBIT0}}$. A shift pulse always occurs during dot position 8 time to parallel load the data from the character ROMs into the parallel-to-serial converter.

3.10 PARALLEL-TO-SERIAL CONVERTER.

3.10.1 The parallel-to-serial converter is loaded with the ROM output word and receives a Shift Clock (SHFT) signal from U34, Pin 6. The parallel data is serially shifted out; is merged with $\overline{\text{DBIT8}}$ and $\overline{\text{DBIT0}}$; and becomes the external serial bit stream, $\overline{\text{XBITS1}}$.

3.10.2 The parallel-to-serial converter consists of U58 (which handles bits 1 through 7) and U46 (which merges those seven bits with $\overline{\text{DBIT0}}$ and $\overline{\text{DBIT8}}$). During dot position 8 time, the load line of U58 at Pin 15 is kept low and a shift pulse stream shifts the information serially into U46. If the selected character set is of the microvector type, $\overline{\text{DBIT0}}$ and buffered $\overline{\text{DBIT8}}$ are merged with the output of U58 to form the serial bit stream, $\overline{\text{XBITS1}}$. This serial signal, in turn, is sent to the Display Control PCA via the P3 connector where it is merged with the minimum system bit stream.

3.11 ENHANCEMENT GENERATOR.

3.11.1 The enhancement generator is a 3-bit register which receives the display enhancement signals from the line buffers; holds them for one character time; and outputs them to the Display Control PCA. A field position alignment one-shot allows the half-bright display feature to be positioned exactly over the character to which it is applied, thus compensating for accumulated delays in the video generator.

3.11.2 The three latches in the enhancement generator receive the enhancement signals from the line buffers and hold them during the read access cycle of the character ROMs. The underline and blinking latches are directly loaded by BUFCLK while the half-bright latch is clocked by one-shot U13. The FIELD alignment potentiometer is used to compensate the half-bright signal against the accumulated delays incurred by the video signal.

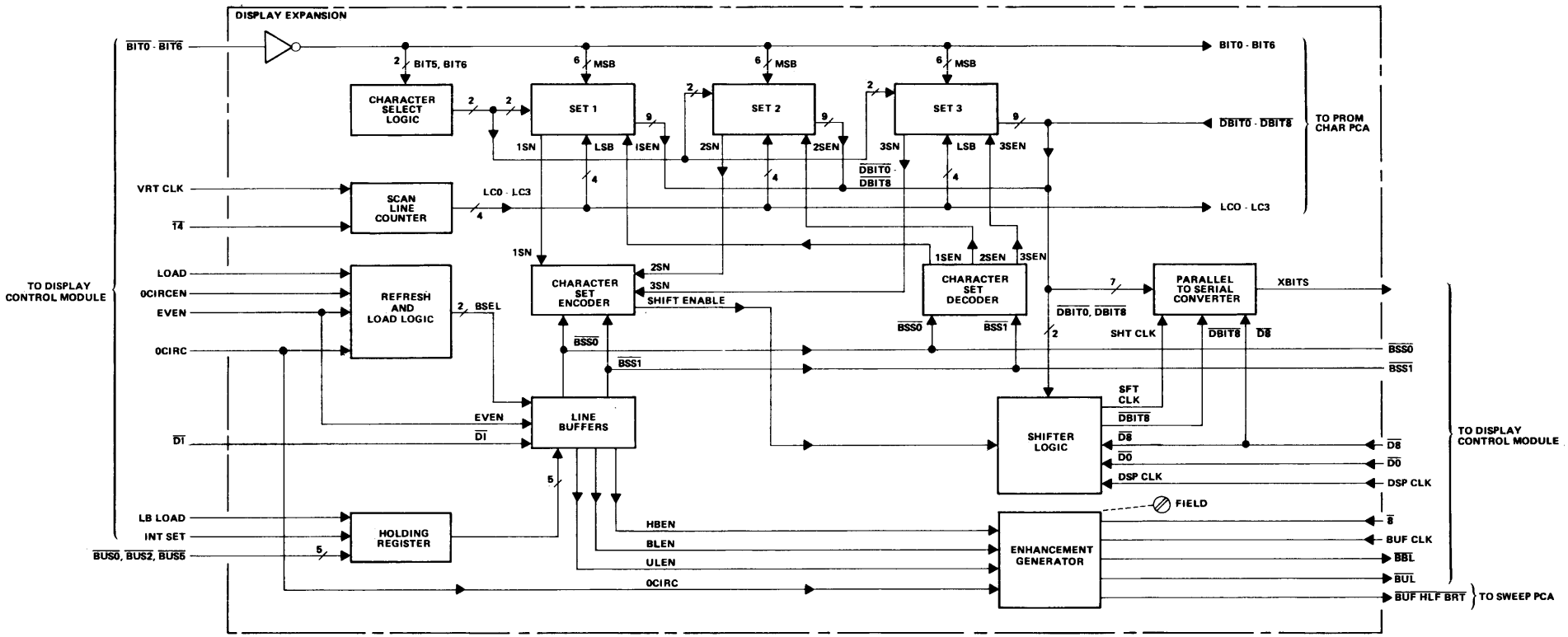

Figure 1
Display Expansion Module Block Diagram
SEP-06-77 13255-91024

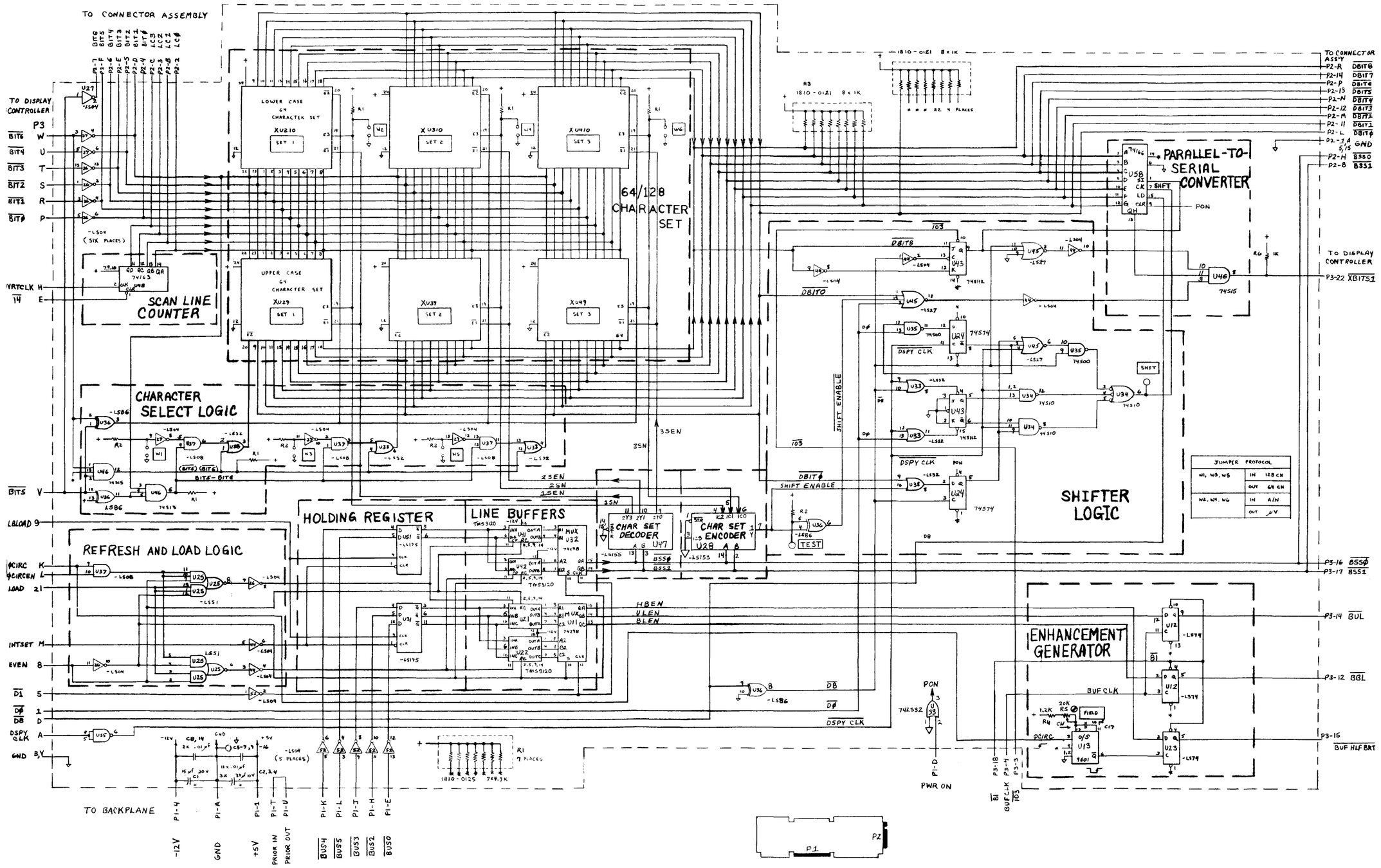

Figure 2
Display Enhancement PCA Schematic Diagram
SEP-06-77 13255-91024

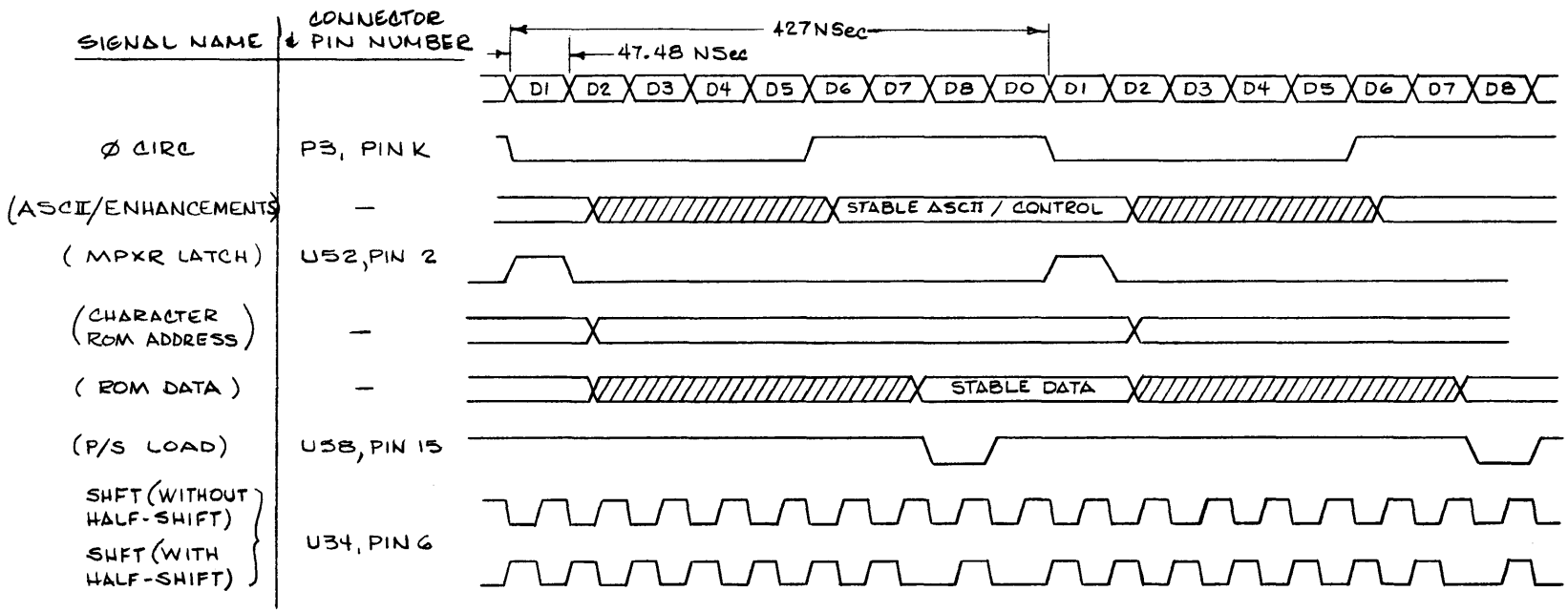

Figure 3
Display Expansion Timing Diagram
SEP-06-77 13255-91024

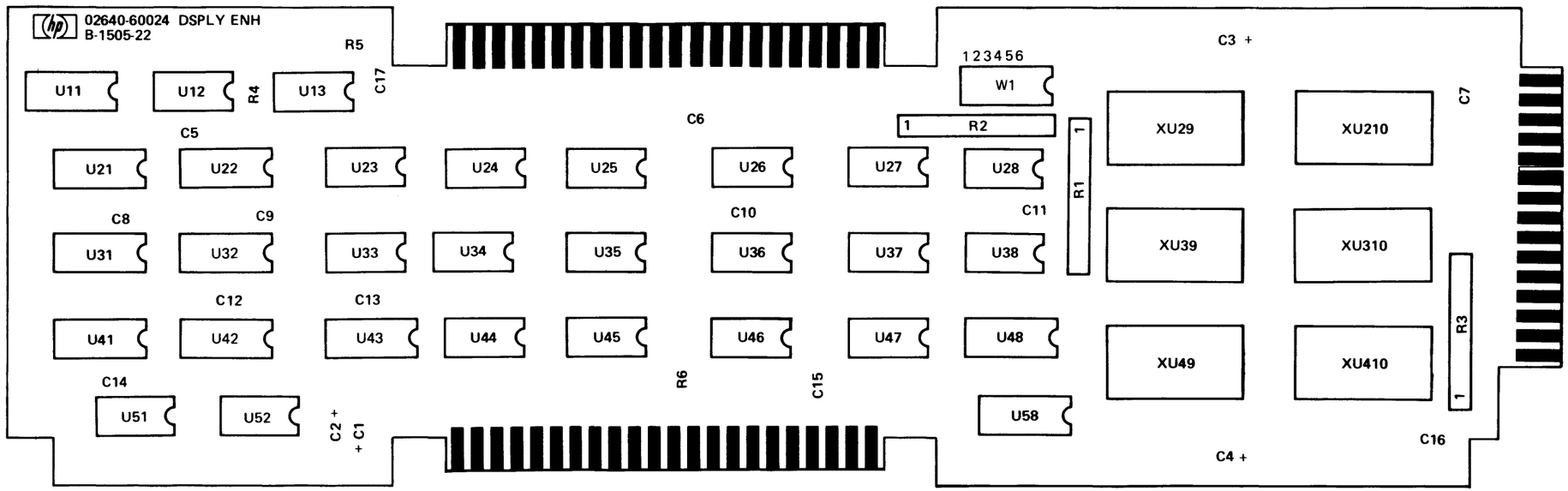

Figure 4
Display Enhancement PCA Component Location Diagram
SEP-06-77 13255-91024

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60022	1	CONNECTOR ASSEMBLY (4) REVISION DATE: 12-01-76	28480	02640-60022
	0403-0347	4	BUMPER FOOT, 0.25" W	13862	9668
	1251-1887	4	CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	71785	252-22-30-340

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60024	1	DISPLAY ENHANCEMENT ASSEMBLY DATE CODE: 8-1505-22 REVISION DATE: 07-15-77	28480	02640-60024
C1	0180-1746	1	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C2	0180-0393	3	CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C3	0180-0393		CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C4	0180-0393		CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C5	0160-2055	12	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C6	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C7	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C8	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C9	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C10	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C11	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C12	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C13	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C14	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C15	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C16	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C17	0160-2257	1	CAPACITOR-FXD 10PF +-5% 500WVDC CER	28480	0160-2257
E1	0360-0124	3	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E2	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E3	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
R1	1810-0125	1	NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R2	1810-0121	2	NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0121
R3	1810-0121		NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0121
R4	0683-2225	1	RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
R5	2100-3353	1	RESISTOR-TRMR 20K 10% C SIDE-ADJ 1-TRN	32997	3386X-Y46-203
R6	0683-1025	1	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
U11	1820-1100	2	IC-DIGITAL SN74298N TTL QUAD 2	01295	SN74298N
U12	1820-1112	2	IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
U13	1820-0207	1	IC-DIGITAL 9601PC TTL MONOSTBL	07263	9601PC
U21	1820-1346	4	IC-DIGITAL TMS3120NC PMOS QUAD	01295	TMS3120NC
U22	1820-1346		IC-DIGITAL TMS3120NC PMOS QUAD	01295	TMS3120NC
U23	1820-1112		IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
U24	1820-0693	1	IC-DIGITAL SN74S74N TTL S DUAL	01295	SN74S74N
U25	1820-1210	1	IC-DIGITAL SN74LS51N TTL LS DUAL 2	01295	SN74LS51N
U26	1820-1199	4	IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U27	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U28	1820-1244	1	IC-DIGITAL SN74LS153N TTL LS 4	01295	SN74LS153N
U31	1820-1195	2	IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
U32	1820-1100		IC-DIGITAL SN74298N TTL QUAD 2	01295	SN74298N
U33	1820-1208	2	IC-DIGITAL SN74LS32N TTL LS QUAD 2 OR	01295	SN74LS32N
U34	1820-0685	1	IC-DIGITAL SN74S10N TTL S TPL 3 NAND	01295	SN74S10N
U35	1820-0681	1	IC-DIGITAL SN74S00N TTL S QUAD 2 NAND	01295	SN74S00N
U36	1820-1211	1	IC-DIGITAL SN74LS86N TTL LS QUAD 2	01295	SN74LS86N
U37	1820-1201	1	IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U38	1820-1208		IC-DIGITAL SN74LS32N TTL LS QUAD 2 OR	01295	SN74LS32N
U41	1820-1346		IC-DIGITAL TMS3120NC PMOS QUAD	01295	TMS3120NC
U42	1820-1346		IC-DIGITAL TMS3120NC PMOS QUAD	01295	TMS3120NC
U43	1820-0629	1	IC-DIGITAL SN74S112N TTL S DUAL J-K	01295	SN74S112N
U44	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U45	1820-1206	1	IC-DIGITAL SN74LS27N TTL LS TPL 3 NOR	01295	SN74LS27N
U46	1820-0687	1	IC-DIGITAL SN74S15N TTL S TPL 3 AND	01295	SN74S15N
U47	1820-1245	1	IC-DIGITAL SN74LS155N TTL LS DUAL 2	01295	SN74LS155N
U48	1820-0713	1	IC-DIGITAL SN74163N TTL BIN SYNCHRO	01295	SN74163N
U51	1820-1195		IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
U52	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U58	1820-1107	1	IC-DIGITAL SN74166N TTL R-S PRL-IN	01295	SN74166N
W1	1200-0482	1	SOCKET-IC 16-CONT DIP-SLDR	91506	516-AG11D
W1A	1258-0124	6	PIN-PROGRAMMING JUMPER;.30 CONTACT	91506	8136-475G1
W1B	1258-0124		PIN-PROGRAMMING JUMPER;.30 CONTACT	91506	8136-475G1
W1C	1258-0124		PIN-PROGRAMMING JUMPER;.30 CONTACT	91506	8136-475G1
W1D	1258-0124		PIN-PROGRAMMING JUMPER;.30 CONTACT	91506	8136-475G1
W1E	1258-0124		PIN-PROGRAMMING JUMPER;.30 CONTACT	91506	8136-475G1
W1F	1258-0124		PIN-PROGRAMMING JUMPER;.30 CONTACT	91506	8136-475G1
XU29	1200-0541	6	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU39	1200-0541		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU49	1200-0541		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU210	1200-0541		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU310	1200-0541		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU410	1200-0541		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541