HEWLETT PACKARD

HP 7974A

SERVICE MANUAL

Part No. 07974-90030

8/1/84

THIS MANUAL IS INTENDED ONLY FOR SERVICE PERSONNEL
TRAINED IN ITS USE
BY HEWLETT-PACKARD

SAFETY CONSIDERATIONS

GENERAL - This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal.

WARNING The WARNING sign denotes a hazard. It calls attention to a procedure or practice which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure or practice which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source according to the input power configuration instructions provided in this manual.

If this product is to be operated with an autotransformer make sure that the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by service-trained personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged after the product has been disconnected from the main power source.

To avoid a fire hazard, fuses with the proper current rating and of the specified type (normal blow, time delay, etc.) must be used for replacement.

To install or remove a fuse, first disconnect the power cord from the device. Then, using a small flat-bladed screw driver, turn the fuseholder cap counterclockwise until the cap releases. Install either end of a properly rated fuse into the cap. Next, insert the fuse and fuseholder cap into the fuseholder by pressing the cap inward and then turning it clockwise until it locks in place.

This page intentionally left blank.

CONTENTS: SECTION I

---FIGURES---

[1] DESCRIPTION

1.1 PERFORMANCE

The HP 7974A is a 1/2 inch, HP-IB, read-after-write digital magnetic tape drive which operates at 50 ips in the start/stop mode and 100 ips in the streaming mode. The standard tape format is 1600 bpi. A dual density(800/1600 bpi) option is also available at purchase or it can be installed in the field. In the 800 bpi (NRZI) mode, the maximum transfer rate is 40 kilobytes at 50 ips and 80 kilobytes at 100 ips. For 1600 bpi (PE) mode the transfer rate is 80 and 160 kilobytes.

In the write mode, the tape drive stores the data to be written in an internal buffer and provides and "Immediate Response" back to the host system. The host system can then send additional data to the drive. Internally, the drive uses command queuing to keep the unit in the streaming mode. In the event that the host system does not supply data at a sufficient rate to keep the unit in the streaming mode the tape drive will revert to the start/stop mode.

In the read mode, tape access time is decreased by the "read ahead" feature. When the host system sends a read command to the tape drive, the drive fills its buffer in anticipation of another read command. Therefore, instead moving the tape during every read operation, data is transferred from the buffer. During lengthy read operations, the buffer is filled as needed.

1.2 AUTOMATIC RETRY

"Automatic retry" is used by the HP 7974A to compensate for data transfer errors caused by tape surface defects. Normally, a few data errors occur during read/write operations because a tape's magnetic signal becomes substantially weakened as the oxide coating wears out or minor scratches appear on the tape surface.

Whenever a data error is first encountered, the read/write electronics attempt to correct the signal and complete the data transfer. If the signal cannot be corrected the first time, the HP 7974A automatically repeats the operation which detected the error. The operation continues to repeat until the transfer is successful or a retry limit is reached. In the read mode, the drive will attempt to read a tape segment up to seven times. In the write mode, if an error prevents data from being written to a segment of tape, that segment is skipped and the next available space is used. If necessary, the drive will skip up to eighteen segments in a row.

NOTE

When a tape is mounted, a log of the "soft" (correctable) errors detected on that tape is kept by the HP 7974A in order to prevent possible damage to the read/write head. If an excessive soft error rate (more than 1 retry in 256 records) is detected, the message **>ERR** will appear briefly in the display. Frequent **>ERR** messages indicate that the tape should be replaced before data is permanently lost and damage to the read/write head occurs.

1.3 DIAGNOSTICS

The HP 7974A contains extensive internal diagnostic programs designed to identify equipment malfunctions and isolate the components that caused the failure. There are two diagnostic program groups: "100 Level" and "200 Level". The 100 Level programs check the operation of the ICU and general operations of the transport. These programs may be accessed by the host system or by operating the front panel. The 200 Level diagnostic programs isolate the transport mechanisms from the ICU operations and are accessible only by operating the front panel. For more detailed information, see Section VIII.

1.4 CABINET

The standard tape drive is a 1600 bpi unit mounted in a 19 inch (19" X 56") EIA cabinet. The cabinet can accomodate two HP 7974A tape drives and a two-drive option is available at the time of purchase or as an upgrade kit for installation in the field at a later date.

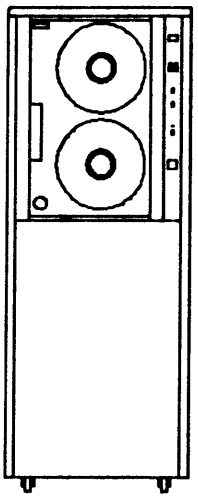


Figure 1-1 HP 7974A Cabinet

1.5 IDENTIFICATION

The serial number label consists of a four digit prefix, a letter, and a five digit suffix (0000A00000). The first four digits indicate design changes. The letter designates the country in which the subsystem was manufactured ("A" indicates the United States). The five digit suffix is a sequential number which increments with each tape unit shipped. This label is located on the dustcover door: in the lower right-hand corner, near the hinge.

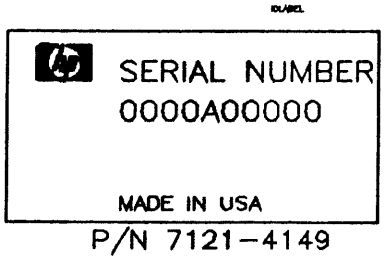


Figure 1-2 Serial Number Label

[2] OPTIONS

HP 7974A - Standard option; the 1600 cpi PE drive in an upright cabinet.

Option 131 - Add second drive option; a HP 7974A unit and all hardware necessary for on-site installation into an existing cabinet.

Option 800 - Dual density option; adds the 800 cpi NRZI board and a dual density read/write head.

[3] SPECIFICATIONS

PERFORMANCE

Tape Speeds	100 ips streaming mode 50 ips full start/stop mode 200 ips rewind speed (peak on 10.5 in. reel)
Speed Variation	±1% of nominal long-term ISV ±8%
Start/Stop Distance	4.83 mm, ±0.51 mm 0.19 in, ±0.02 in
Start/Stop Time	7.6 ms
Streaming Times (100 ips)	
Access	59 ms, nominal
Reposition to Stop	270 ms
Reposition to Start	329 ms
Command Reinstruct	4 ms, 0.7 IRG
Data Reliability (100% certified tape)	
Recoverable Write	<1 in 10^{8} bits
Recoverable Read	<1 in 10^{8} bits
Permanent Errors	<1 in 10^{11} bits

HARDWARE

Reel Motor Braking	Active for normal tape operations Dynamic in power failure.
Magnetic Head Assembly	Nine track, read/write with erase; factory preset for skew and azimuth. No adjustment required.

BOT/EOT Sensing	Reflective; LED/phototransistor
Tape Tension	269 gm (9.5 oz) nominal
Interface Protocol	HP-IB (IEEE-488) with Amigo Factory set to load of 2.

PHYSICAL CHARACTERISTICS

Height	1.6 m (63.0 in)
Width	600 mm (24 in)
Depth	775 mm (30.5 in)
Weight	180.0 kg (400 lbs)

ENVIRONMENT

Temperature

Hardware

Operating	15°C to 32°C (59°F to 90°F) Recommended: 18°C to 24°C (65°F to 75°F)
Standby	0°C to 55°C (32°F to 122°F)
Storage	-10°C to 65°C (14°F to 149°F)
Shipment	-40°C to 75°C (-40°F to 167°F)
Rate of Change	20°C (68°F) / Hour Maximum

Media

Operating	15°C to 32°C (59°F to 90°F)
Non-Operating	
Recorded:	5°C to 32°C (41°F to 90°F)
Unrecorded:	5°C to 48°C (41°F to 118°F)

Relative Humidity (non-condensing)

Operating	20% to 80% (media limited) Recommended: 40%-60%
Non-Operating	10% to 95%
Maximum Wet Bulb Temperature	25.5°C (78°F)
Standby	10% to 90%
Storage or Shipment	10% to 95%

Altitude (Above Sea Level)

Operating	3000 m (10,000 ft)
Non-Operating	15000 m (50,000 ft)

SHOCK

Operating	3 G 1/2 sine pulse, 10 ms duration
Packaged	15 G, 20 ms duration

VIBRATION

Operating	0.1 G (3-15 Hz); 0.5 G (15-300 Hz)
Non-Operating	0.75 G for 10 minutes

POWER REQUIREMENTS

Line Voltage	100 VAC ±10%
	110 VAC ±10%
(Can be configured to operate	115 VAC ±10%
over these ranges)	120 VAC ±10%
	200 VAC ±10%
	220 VAC ±10%
	230 VAC ±10%
	240 VAC ±10%
Line Frequency	48 Hz to 66 Hz; Single-Phase
Power Consumption	520 Watts Maximum
Heat Dissipation	2050 Btu/Hr Maximum

Line Current

Power On Surge

COLD
38 Amps at 120 VAC for one-half cycle max.
22 Amps at 220 VAC for one-half cycle max.

HOT
50 Amps at 120 VAC for one-half cycle max.
40 Amps at 220 VAC for one-half cycle max.

Operating

120 VAC	4.50 Amps
220 VAC	2.45 Amps

Standby	2 Amps RMS Maximum
Tolerated line dropout	1 cycle in 10 cycles

REGULATORY AGENCY COMPLIANCE

Agency	Compliance to:
Safety	
Underwriters Laboratories	UL 114,478
Canadian Standards Association	C22.2 No. 154-M1983
International Electrotechnical Commission	IEC 380,435
Emissions	
Federal Communication Commission	FCC-A
FTZ	VDE-B

AUDIBLE NOISE

<60 dBA

TAPE MEDIA

Width	12.7 mm (0.5 inches)
Base Thickness	.38 mm (1.5 mils)
	Use of 1 mil tape not supported

APPLICABLE STANDARDS

ANSI X3.39	Recorded Magnetic Tape for Information Interchange (1600 cpi, PE, 9 track)
ANSI X3.22	Recorded Magnetic Tape for Information Interchange (800 cpi, NRZI)
ANSI X3.40	Unrecorded Magnetic Tape for Information Interchange (9 track 200 and 800 cpi NRZI, 1600 cpi PE)
ECMA-12	Data Interchange on 9 track NRZI Magnetic Tape at 31.5/mm (800 cpi)
ECMA-36	Data Interchange on 9 track Phase-encoded Magnetic Tape at 63 bits/mm (1600 cpi)
ECMA-62	Data Interchange on 12.7 mm 9 track Magnetic Tape
BS 4503 Part 1	Specification for 9 track Magnetic Tape for Data Interchange at 800 Rows per Inch (NRZI)
BS 4503 Part 2	Specification for 9 track Magnetic Tape for Data Interchange at 1600 Rows per Inch (NRZI)

[4] RECOMMENDED SPARE PARTS

The recommended spare parts table below is a list of the most commonly needed parts. For a more complete version of the replaceable parts list see Section IX.

New Part Number	Description
07974-66501	PCA, Interconnect
07978-66504	PCA, Master Control
07978-66506	PCA, HP-IB
105678-TED	PCA, Power Supply
108702-TED	PCA, Read Logic
108705-TED	PCA, 5 Volt Regulator
108709-TED	PCA, Control/Motherboard
108710-TED	PCA, Data Formatter
108716-TED	PCA, NRZI
108708-TED	Strobe Light Assy
108714-TED	PCA, Switch Facia (panel)
108533-TED	BOT and EOT Sensor Assy
103575-TED	Tape Cleaner
78636-TED	Write Enable Assy
76332-TED	Door Switch Assy
78763-TED	Bridge Roller Assy
78764-TED	Roller Guide Assy
2110-0003	Fuse, 3A
2110-0051	Fuse, 10A
2110-0030	Fuse, 5A Slow-Blo
2110-0303	Fuse, 2A Slow-Blo
1826-0147	Regulator MC7812
1826-0221	Regulator MC7912
1826-0445	Regulator MC7905
108715-TED	Arm Drive Motor and Capacitor Assembly
108706-TED	PE/NRZI Head Assembly
108494-TED	Arm Drive Assembly
76952-TED	Reel Motor
78769-TED	Capstan Motor and Tachometer Assembly
103720-TED	Card Frame

Figure 4-1 Table of Recommended Spare Parts

[5] TOOLS AND TEST EQUIPMENT

The following tools and test equipment are needed to repair the HP 7974A.

5.1 MECHANICAL

Spring Balance (0-680 g;0-24 oz): P/N 8750-0039
Parallel Gauge (for arm roller angle adjustment): P/N 76120-TED
Set of Shims (0.0025;0.003; 0.004; 0.0045; 0.005 in)
Set of Metal Feeler Gauges (compatible with shim sizes given)
Micrometer (for shim measurement)
Metric and English sets of Allen Keys (with screwdriver handles)
Screwdrivers: flat small and large;posi-drives #1, #2 (extra-long)
Plastic Feeler Gauges (0.15 mm,0.28 mm; 0.006 in, 0.011 in)
Non-metallic Potentiometer Adjustment Tool: P/N 8730-0013

5.2 ELECTRICAL

(a) Multimeter. A general purpose multimeter capable of measuring: 10 mV - 250 V dc; up to 240 VAC

(b) Oscilloscope: HP 1740A or equivalent. (It must have a bandwidth of at least 50 MHz)

(c) Digital Frequency Counter (Optional). To check frequencies in the range of 1 kHz to 10 MHz.

5.3 TAPES

(a) Work Tape. A good quality tape (of a recommended type) know to the user to have no data drop-outs. The tape should not contain data of any consequence and should be available for write checks/tests. The transport supply reel must be fitted with a write-enable ring.

(b) Master Alignment (Skew) Reference Tape: P/N 9162-0027

(c) Master Amplitude Reference Tape (IBM # 432152)

(d) Length of looped tape (approximately 500 mm (20 in)). The loops are formed at each end using adhesive tape and must be large enough to pass over the rollers.

(e) A special tape, fitted with an EOT marker postioned 50 mm (2 in) from a BOT marker.

(f) A good quality tape, free from edge damage and known to track correctly, to be used exclusively for tape path checks/adjustments.

(g) Reel of adhesive reflective tape markers.

[6] CONSUMABLES

You should encourage customers to keep a supply of cleaning and other high-usage materials in stock at all times. Supplies and accessories can be ordered directly from the Computer Users Catalog . The following HP products are recommended for use with the HP 7974A:

- Magnetic Tape, 2400 ft (box of 10)	92150F
- Tape Head Cleaner, 6 - 4 oz bottles	92193X
- Foam Swabs (50 per package)	
wooden shaft	9300-0468
plastic shaft	9300-0767
- Lint-Free Wipes (100 per bag)	92193W
- Magnetic Head Cleaning Kit	92193H
2 - 4 oz bottles of Tape Head Cleaner	
50- Lint-Free Wipes	
10- Foam Swabs with plastic shaft	
1 - easy-pour dispensing cap	

Figure 6-1 Table of Recommended Consumables

[7] CUSTOMER ACCESSORIES

The following items are supplied to the customer with each shipment.

QUANTITY	ITEM	PART NUMBER
1	4 oz bottle of head cleaner	8500-1251
1	empty take-up reel	1490-0738
1	reel of magnetic tape (1/2" ; 2400 ft.)	9164-0158
1	2-meter HP-IB cable	5060-9456
1	package of foam swabs (50 swabs; wooden shaft)	9300-0468
1	Operator's Manual	07974-9000

Figure 7-1 Customer Accessory Kit

[8] GENERAL OPERATION

8.1 FRONT PANEL

The front panel buttons may be split into three groups corresponding to the online, offline, and diagnostic/address select modes of operation.

The ONLINE button puts the drive online to allow the host to control the drive's operation.

The offline buttons are OFFLINE RESET, LOAD, and REWIND. OFFLINE RESET exits the online mode, initializes the system, and aborts a loading sequence. LOAD initiates the tape loading sequence. REWIND either rewinds a tape positioned past the EOT (End-of-tape) marker or unloads a tape which is at the BOT (Beginning-of-tape) marker.

Buttons DIAGNOSTICS and ADDRESS activate either the diagnostics or address select features of the HP 7974A. When in the diagnostic/address select mode, the online and offline keys assume the secondary roles of Tens, Units, Fast, and Enter to allow the user to select diagnostic tests and set the HP-IB address.

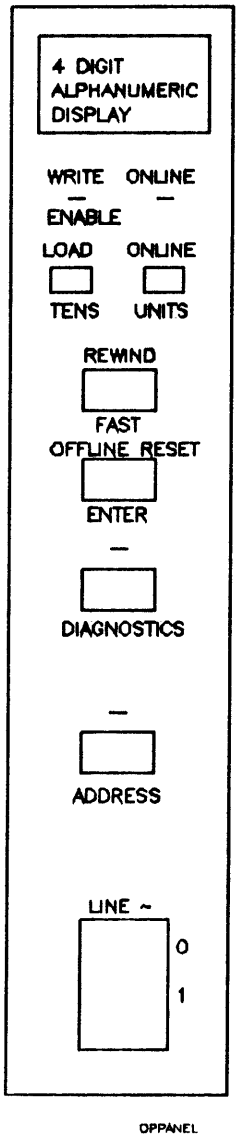


Figure 8-1 Front Panel

8.2 POWER-ON SELFTEST

Turn the power on and the selftest will begin automatically. The power-on selftest, diagnostic test *5*, is designed to check out as much of the HP 7974A drive as possible without using a work tape. About 75% of the drive is tested; including the Master Controller Assembly, the HP-IB Assembly, and the digital data path. Test *5* accomplishes its tasks by streaming nine diagnostic tests (Refer to Section VIII), shown in order, together: *6, 2, 7, 10, 11, 13, 14, 50, and 100.* When the power-on self test executes, the following messages appear one at a time in the display:

```
DISPLAY:        MEANING:

SELF          - Self Test beginning
TEST
R 06          - Running Test 6
R 02            "       "  2
R 07            "       "  7
0000          - Test 7 scrolls the
1111            display characters
 .              The indicators light
 .              after the * appears

 .
9999
****
R 10          - Running Test 10
R 11            "       "  11
R 13            "       "  13
R 14            "       "  14
R 50            "       "  50
R100            "       " 100
OK            - Test 5 passed
```

The testing process takes a little less than 30 seconds to complete. After successful completion of the power-on tests, the display message is **OK** or **DOOR**, if the door is open. Diagnostics mode is then exited at the end of the test and the HP 7974A is now ready for use.

If any test is not successful, you may have a hardware failure. Error codes, discussed in Section VIII, indicate which major component caused the problem.

NOTE

If a failure occurs, do not turn off the power: the diagnostic error log, test **1** is cleared when the power is cycled. The error log may contain information needed to diagnose the cause(s) of failure. Refer to Section VIII instructions on use and interpretation of the diagnostic error log.

8.3 MOUNTING THE SUPPLY REEL

(a) Set the power switch to I ("1") and wait until the self tests are complete.

(b) Press the release catch on the left-hand side of the tape transport and open the door. **DOOR** appears in the display.

(c) Before mounting the tape, ensure that the tape path is clean. Clean if necessary.(Section IV)

(d) Check the write-enable ring before mounting the tape. It should either be properly installed to permit writing or removed to safeguard existing data. (If the write-enable ring is not placed correctly on the reel, the tab may hit the sensor.)

(e) Place the tape reel onto the supply hub and, with fingers near the center of the reel, push until the reel snaps over the toggle catches on the hub and locks. **Do not press on the reel flanges;** it may cause edge damage and uneven tape motion.

If the toggle catches are pushed in on an empty hub, press the hub-release plate to return them to the proper position.

(f) If the Write Enable indicator does not come on when a write-enable ring is fitted to the supply reel, remount the tape.

8.4 THREADING THE TAPE

CAUTION

The tension arms must be in the loading position, the position farthest from the read/write heads, before a tape can be threaded. If the arms are not in the proper position, close the door.

Do not force the tension arms into the loading position. You could damage the mechanical arm assembly.

(a) Make sure your hands are clean then withdraw a short length of tape from the supply reel and guide it over the top two fixed rollers and below the upper tension arm roller. (Refer to either Figure 8-2 or the blue threading line on the tape path.)

(b) Feed the tape down through the head cover slot and around the the capstan.

(c) Route the tape over the lower tension arm roller; *below* the two fixed rollers by the take-up spool. Guide the tape to the right of the spool between the flanges and allow the tape to drop over the spool.

(d) Using the finger holes provided, wind the tape around the take-up spool, approximately three times, until the tape is taut and the supply reel begins to move.

(e) Make sure the tape is correctly located over the head and rollers.

(f) Close the dustcover door. The display changes from **DOOR** to **OK**. The tape is now ready to load.

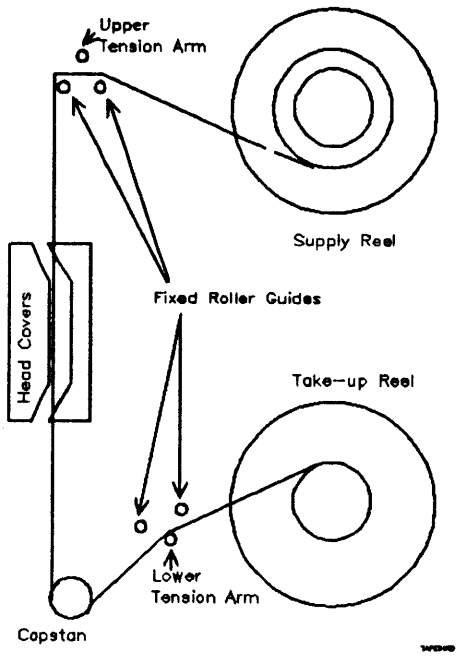


Figure 8-2 Tape Threading Diagram

8.5 LOADING SEQUENCE

(a) Press the LOAD button. The message **LOAD** should appear in the display.

The loading sequence starts when the arm drive mechanism retracts and the tension arms take up the tape between the fixed rollers. After the tension armsare set, the transport motors come on and establish the proper tape tension. After a short delay, the drive automatically searches for the beginning-of-tape (BOT) marker. When the marker is found, **BOT** will appear in the display.

CAUTION

Once the tape is tensioned, the tape tension arms or the hub release plate must not be touched. If the tension is disturbed, severe damage to the tape could occur when the reels begin to move.

(b) After **BOT** appears, press the ONLINE button. The ONLINE indicator will light when the host is able to access the drive.

8.6 UNLOADING SEQUENCE

(a) Press OFFLINE RESET. The ONLINE indicator should turn off.

> Pressing OFFLINE RESET twice in a row causes a hard reset; the transport electronics are re-initialized and the drive will "forget" that a tape has been loaded. Once the drive "forgets", the unload sequence will not work until the tape has been re-loaded.

(b) If **BOT** does not appear in the display, press REWIND to reposition the tape.

(c) With the tape at BOT, press REWIND to unload the tape. The **UNLD** messages appears in the display while the tape reverses, loses tension, and winds completely onto the supply reel.

> If the unload sequence is begun inadvertently, it can be cancelled by pressing OFFLINE RESET.

(d) When the tension arms return to the load position, the message **OK** indicates that the reel may be removed. Open the door, steady the outer edges of the supply reel flanges with both hands, press the central hub-release plate with both thumbs, and gently remove the supply reel. At this stage you may load another tape.

NOTE

To prolong the life of the **HP** 7974A, Hewlett-Packard recommends that the power be on continuously. However, the power may be turned off when a tape is mounted without damaging it. When the power is turned on again, you may reload the mounted tape after removing slack in the tape path and inspecting the threading.

8.7 OPERATING STATUS MESSAGES

The status messages indicate which functions are being performed by the drive and, more importantly, what errors occur during normal operation. The table is broken into three main parts: MESSAGE, CAUSE, and COMMENTS/CORRECTIVE ACTION. If the status message indicates an error, the most probable cause(s) are listed in the CAUSES section. In most cases, the operator should be able to correct error situations by following the instructions in the COMMENTS/CORRECTIVE ACTION section.

MESSAGE	CAUSE	COMMENTS/CORRECTIVE ACTION
BLNK	Blank tape; no data on first 9.1 m	1. New Tape 2. If tape not new, reload.
BOT	Beginning-Of-Tape marker found	Occurs after LOAD or REWIND
BOT?	1. BOT marker not found 2. No marker on tape	1. Reload Tape 2. Add/replace BOT marker 3. Check excess leader length
BUSY	Executing commands	OFFLINE RESET terminates execution
DIAG	Host is executing online diagnostics	
DOOR	Door open; switch not set	Close door; check switch
>ERR	Soft error rate exceeded: 1. Dirty tape path 2. Worn/Dirty tape	1. Clean tape path 2. Backup and discard worn tape
Fxxx	Diagnostic "xxx" failed	See Section VIII
*F3	Unknown hardware failure	See Section VIII
*F4	Unknown firmware failure	See Section VIII
*F5	Unable to communicate with host system	Reset drive. If problem persists, see Section VIII

MESSAGE	CAUSE	COMMENTS/CORRECTIVE ACTION
HOT!	Drive motors overheating: 1. Room temp. too high 2. Rear door vents blocked	NOTE: Tape motion ceases until drive is cool. 1. Lower room temperature 2. Check/clear rear vents
ID?	Tape density unknown: Not PE (1600bpi) or NRZI (800 bpi)	1. Unformatted/New tape 2. GRC format (6250 bpi)
LOAD	Load sequence operating	Press OFFLINE RESET to abort
NONE	Diagnostic does not exist	See Section VII
OK	Operation/Diagnostic done	
Pxxx	Diagnostic "xxx" passed	
RSET	OFFLINE RESET was pressed or host initiated a reset	
REWD	Rewinding tape to BOT	CAUTION: Do not turn off the power during rewind; it may damage the tape.
TAPE	No tape loaded;tape tension incorrect	1. Load tape 2. Check threading, remove slack
Rxxx	Running diagnostic "xxx"	
UNLD	Unload sequence operating	
V00	Requesting current firmware revision number	Firmware update in progress Press DIAGNOSTIC to exit
800 or 1600	Tape density= 800 bpi Tape density = 1600 bpi	Message appears after LOAD

CONTENTS: SECTION II

---FIGURES---

This page intentionally left blank.

SITE PREPARATION AND REQUIREMENTS

SECTION II

[1] SITE PREPARATION

The following paragraphs discuss the requirements for proper operation of the tape drive. For detailed site environmental information, refer to the Hewlett-Packard publication *Site Environmental Requirements for Tape Drives* (P/N 5955-3456).

[2] ENVIRONMENT

To minimize performance problems, place the HP 7974A in a clean, climate-controlled operating area. The area does not have to be air-conditioned but an operating room temperature between 18°C to 24°C (65°F to 75°F) and a relative humidity level between 40% to 60% (non-condensing) is recommended.

NOTE

When the HP 7974A is connected to Hewlett-Packard systems, the more stringent environmental specifications listed for any device within the system supersede these specifications.

[3] PRIMARY POWER AND EXTERNAL GROUND

3.1 Frequency

The tape unit is designed to operate with either 50 or 60 Hz single phase A.C. mains input. Maximum line variation is 48 Hz to 62 Hz.

3.2 Line Voltage

The unit can be operated on the following line voltages; 100,120,220,and 240 VAC. Maximum allowable line voltage variation is +/-10%.

Input voltage can be selected in the field via a voltage selector plug. The unit is shipped with a plug for either 110VAC, 115VAC or 230VAC. See *Configuration, Section III* for detailed plug descriptions.

3.3 Line Current

Power On Surge

```
COLD
38 Amps   120 VAC for one-half cycle max.
22 Amps   220 VAC for one-half cycle max.
HOT
50 Amps   120 VAC for one-half cycle max.
40 Amps   220 VAC for one-half cycle max.
```

Operating

120 VAC 4.50 Amps
220 VAC 2.45 Amps
Tolerated line dropout 1 cycle in 10 cycles.

3.4 Power Consumption

2050 BTU (600 Watts)

[4] LOCATION

Position the drive away form sources of particulate contamination such as frequently used doors and walkways, stacks of supplies that collect dust, and smoke-filled rooms. Ventilation and door clearance requirements also need to be considered when choosing an appropriate operating site. Figure 2-1 is provided to help you determine the space needed. A space of 600 mm (2 ft) behind the rear door is recommended; however, a minimum of 100 mm (4 in) may be used if adequate air circulation is provided. Maintain a clearance of at least 920 mm (3 ft) in front of the unit to provide adequate space for opening the front door (550 mm / 23 in.) and for servicing.

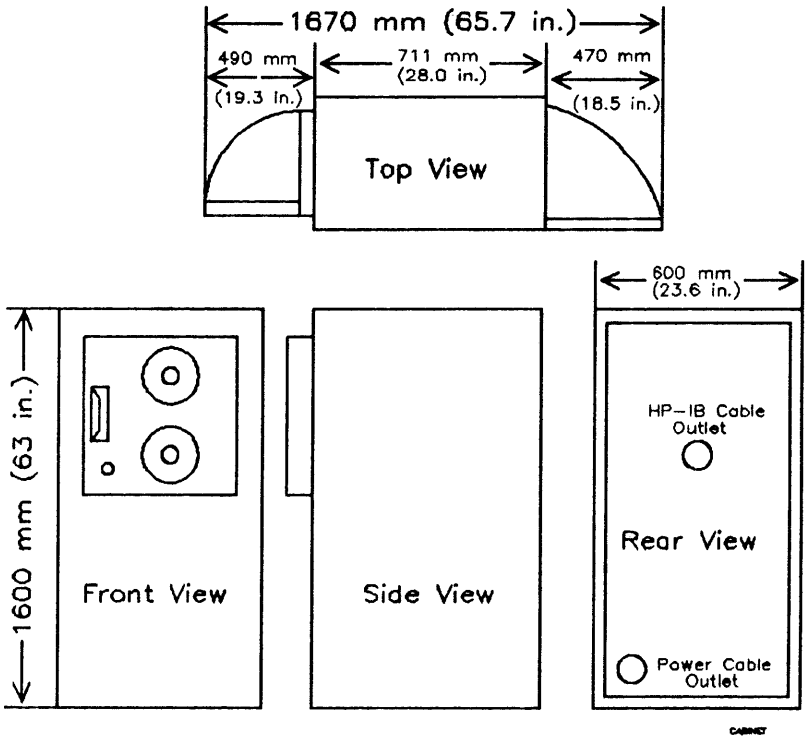


Figure 2-1 HP 7974A Cabinet Dimensions

CONTENTS: SECTION III

---FIGURES---

This page intentionally left blank.

INSTALLATION AND CONFIGURATION

SECTION III

[1] UNPACKING PROCEDURE

This procedure requires a sharp knife or scissors for cutting the plastic banding material and the cardboard carton, an adjustable wrench for raising the levelers and removing the wheel stops on the pallet, and at least two people to unload the unit.

WARNING

Protective glasses should be worn while cutting the strapping bands around the drive cabinet. These straps are under tension. When cut, they may spring back and cause serious eye injury or other injuries.

SEE UNPACKING INSERT FOR PHOTOS

a) Cut the strapping bands surrounding the carton.

b) Cut the shipping carton along one of the vertical edges and across one adjoining upper horizontal edge.

c) Fold back the edge that has been cut and remove the carton from the opposite side.

d) Cut the strapping bands surrounding the tape drive cabinet.

e) Remove the cushion, ramp piece, and plastic bag from the top of the unit. The cushion and ramp piece will be used in Steps g and h to form a ramp for rolling the tape drive down to the floor.

f) One end of the pallet has steel pins sticking up through the corners. Use the wrench to remove the wheel stop from that end of the pallet.

g) Build the ramp by placing the cushion behind the pallet so that the pins protrude through the holes in the deck of the cushion.

h) Place the ramp piece at the lower end of the cushion. Make sure the pins on the lower end of the cushion protrude through the holes in the ramp piece.

WARNING

Tighten the drive latch to ensure that the tape drive casting is properly secured before moving the unit. Severe injuries could result if the casting swings open while the cabinet is being pushed, especially on inclines.

WARNING

The tape drive is heavy and difficult to move. Use considerable care during unloading. Use a minimum of two people; one pushing and one guiding it down the ramp.

SEE UNPACKING INSERT FOR PHOTOS

WARNING

The leveler feet must be raised when the drive is rolled down the ramp. If not, they could catch on the ramp and cause the unit to tip over.

i) Check that the leveler feet are raised at least 1/2" above the pallet. Use the wrench to adjust them if necessary.

j) Carefully roll the unit down the ramp. k) Before placing the drive into its operating site, lower the rear levelers until they are 30 - 60 mm (1/8 -1/4 in.) above the floor.

CAUTION

Do not push the drive unit when the levelers are touching the floor. The levelers may bend or break.

l) Push the drive to the location where initial installation and checkout will be performed. If the front casting will be swung out during checkout, extend the stabilizer arms and lower the leveler feet to provide stability.

m) After initial installation and checkout, raise the leveler feet enough to clear the floor, retract the stabilizer arms, and roll the drive into final position. Lower the leveler feet to just touch the floor.

[2] PREPARATION

Before proceeding with configuration and checkout procedures, the following steps must be completed to ensure your safety and allow easy access to all transport assemblies.

(a) Make sure that the work space is in a clean area which allows adequate space for opening and closing the cabinet doors, placing equipment and tools within easy reach, and moving back and forth. The cabinet clearance requirements are specified in Section II.

(b) Completely raise the front and rear leveler feet and move the unit into the work area.

CAUTION

Do not move the unit when the leveler feet are touching the ground. They could cause the unit to tip over and/or become damaged.

(c) Lower the rear leveler feet completely to the floor.

(d) Remove the pins on the front levelers and fully extend the legs before lowering the feet. This will stabilize the unit and prevent it from tipping over when the casting is open.

(e) Open the casting. A two-stage latch secures the drive casting to the cabinet. The latch is balanced so that the second stage catches upon the cabinet if the latch screw becomes loose enough to dislodge the first stage (eg. due to shipping vibration). Its unique design also makes it somewhat tricky to open:

1. Using a 5 mm hex key, turn the drive latch screw clockwise until you can feel the latch move freely.

2. Once the latch is free, turn the screw counterclockwise approximately 1/4 turn and, while holding the latch in that position, gently pull the casting out of the cabinet. The casting will only travel about 2-3 cm (1-1.5 in.).

3. Turn the latch clockwise a 1/4 turn, until the second stage clears the cabinet rail, and slowly swing the drive out of the cabinet.

WARNING

Do not swing the casting out rapidly: it is heavy. A 90° door stop has been added to the drive, but it is still necessary to keep your fingers clear of the hinge and inside casting edge when opening and closing the front of the unit.

(f) Inspect the transport for physical damage. Reseat all circuit boards and make sure all the cables are securely connected.

[3] CONFIGURATION

3.1 POWER STRAPPING

CAUTION

Before power is applied, both the transport and ICU power supply voltage settings and fuses must be verified to ensure proper operation and to prevent damage to the equipment.

3.1.1 Transport

(a) Make sure the correct voltage-select plug and its corresponding fuse is installed. The following three plugs are provided with every drive:

Part Number	Voltage Range	Required Fuse
78528-TED	110VAC ±10%	5 A, Slo-Blo
78529-TED	115VAC ±10%	5 A, Slo-Blo
78532-TED	230VAC ±10%	2 A, Slo-Blo

(b) Verify the jumper wire connections on the voltage-select plug. Figure 3-1 lists the jumper wire connections. Figure 3-1 details the pin locations.

Figure 3-1 Jumper Wire Connections

VOLTAGE	LINK PIN NOs.			
100	1 to 3	2 to 13	5 to 15	12 to 14
110	1 to 4	2 to 10	5 to 15	12 to 14
115	1 to 7	2 to 11	5 to 15	12 to 14
120	1 to 8	2 to 9	5 to 15	12 to 14
200	1 to 3	--	5 to 13	12 to 14
220	1 to 4	--	5 to 10	12 to 14
230	1 to 7	--	5 to 11	12 to 14
240	1 to 8	--	5 to 9	12 to 14

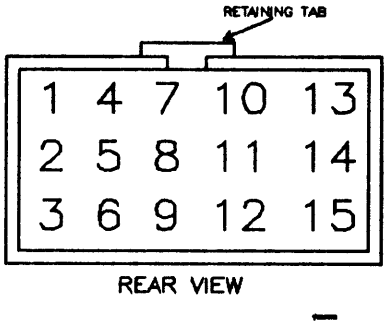
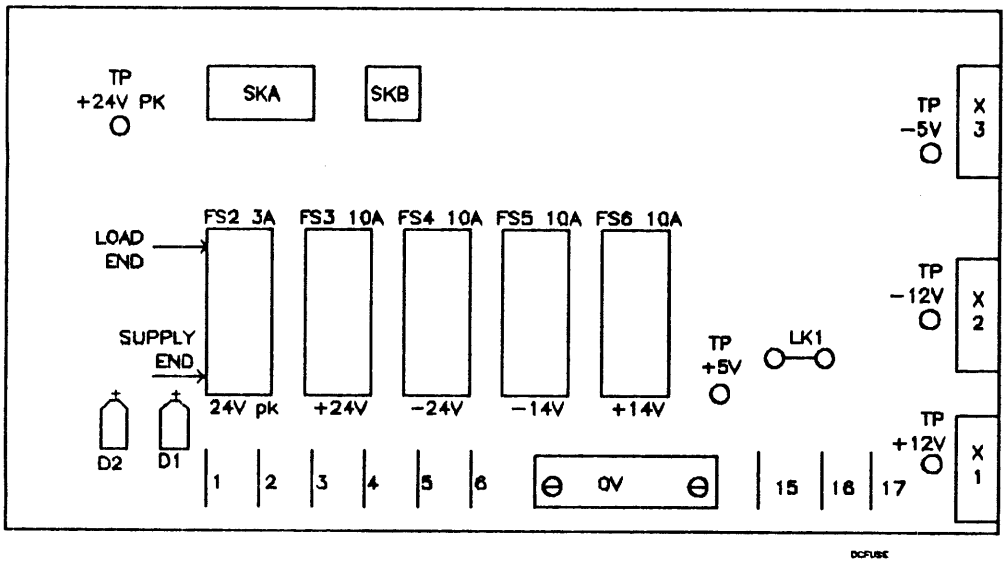


Figure 3-1 Voltage Selector Plug

(c) Double-check the transport power supply PCA (Fig. 3-2) connections:

Terminal No.	Wire
1	43 (yellow/orange)
2	42 (yellow/red)
3	2 (red)
4	7 (violet)
5	8 (grey)
6	3 (orange)
16	9 (white)
0V	0 (blacks)



TRANSPORT POWER SUPPLY PCA
105678-TED

Figure 3-2 Transport Power Supply

3.1.2 ICU Power

Make sure the "ON" switch of the ICU power supply is positioned as shown in Fig. 3-3, the voltage-select switch setting (115/230) corresponds to the operating line voltage, and the 3A fuse (P/N 2110-0003) is secure.

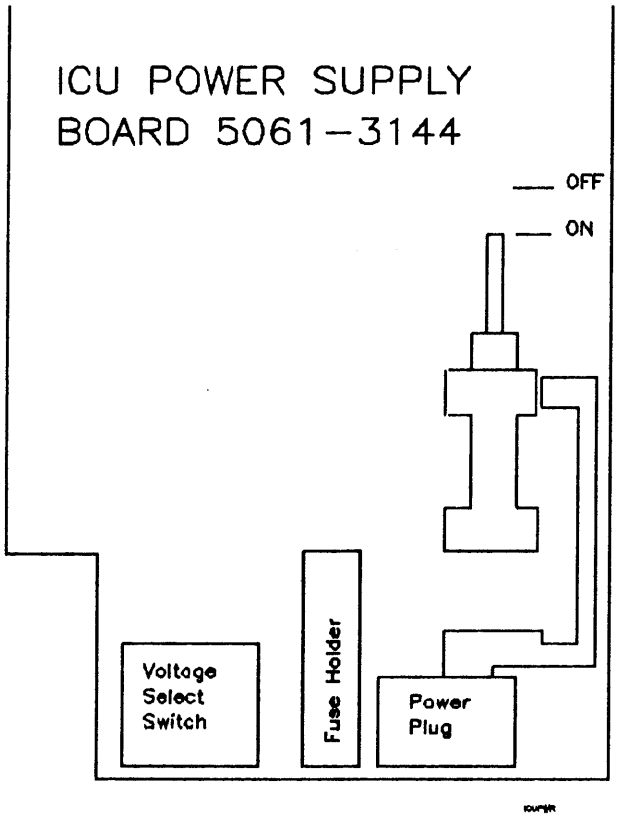


Figure 3-3 ICU Power Supply

3.2 LINKS AND SWITCH SETTINGS

3.2.1 Control/Mother Board Configuration

The Control/Mother board contains both wire links and a dip switch that must be set in order for the PCA to function properly. Check the configuration when installing or replacing the PCA. Refer to Figures 3-4, 3-6 and 3-7.

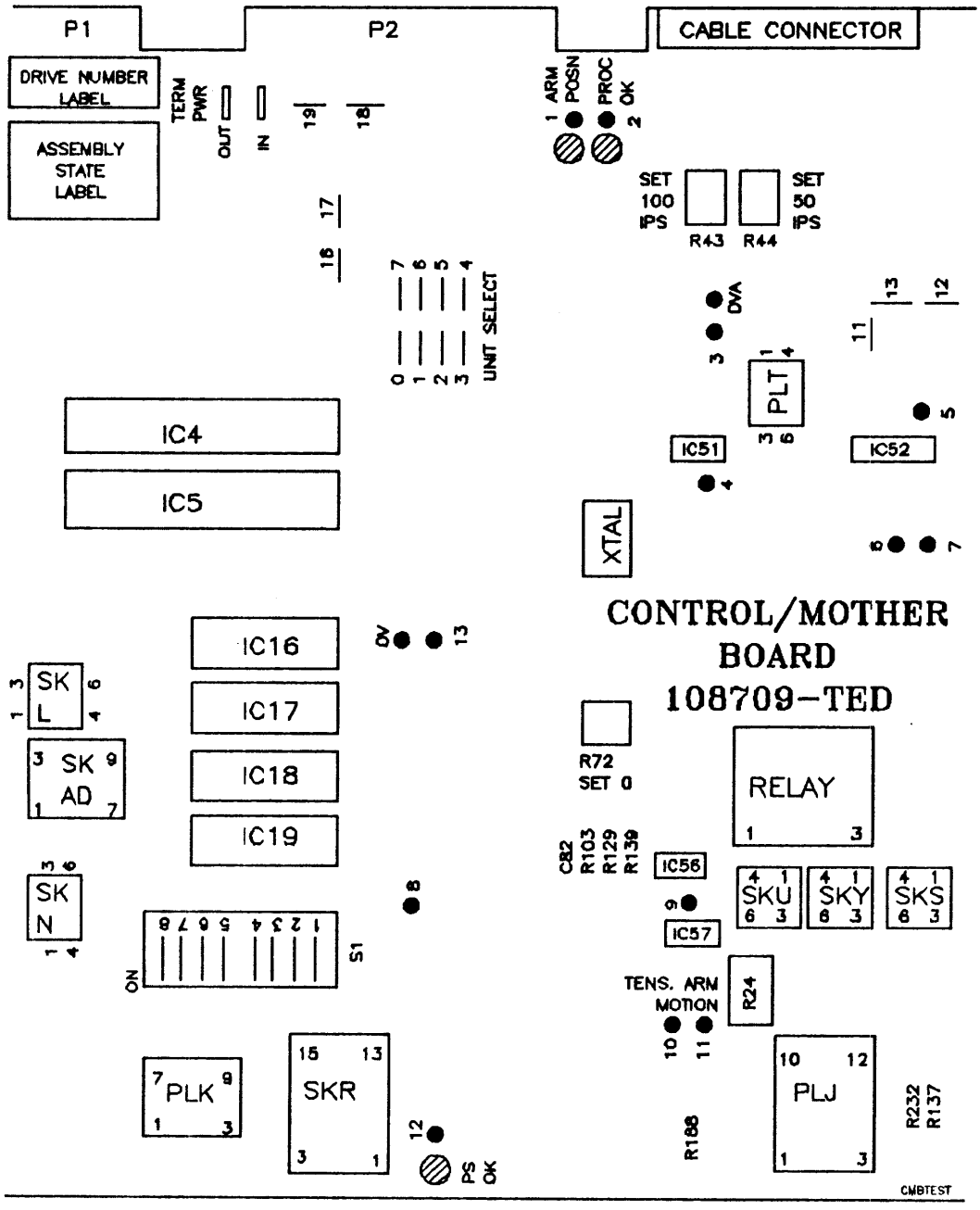


Figure 3-4 Control/Mother Board Test Points

Figure 3-6 Control/Mother Board Links

Number	Position	Description
0	IN	Select Transport Address
1	Out	
2	Out	
3	Out	
4	Out	
5	Out	Note: Does not affect
6	Out	HP-IB Address
7	Out	
8	Out	Not Used
9	Out	IC11 Not Installed
10	Out	Not Used
11	In	Electrocraft Capstan motor used
12	Out	
13	In	
11	Out	Torque System Capstan motor used
12	In	
13	Out	
14	Out	Not Used
15	Out	Not Used
16	In	FBY true on leading edge of GO
17	Out	"
18	In	Transport being used as "Master"
19	Out	"

Figure 3-7 Control/Mother Board Switch Settings

Number	Position	Result
1	Off	EOT latched upon detection
2	Off	Off-line command does not initiate a "Rewind"
3	On	Invalid command sets hard error
4	On	Over-temperature sets hard error
5	On	Selects PL1, pin 36=HISPD PL2 pin 50=HIDEN
6	Off	Density select only via driver
7	On	Power up default to 800 BPI
8	Off	Not used

3.2.2 Data Formatter

Ensure the wire links are in positions 2 and 3 for internal parity generation. Refer to Figure 3-8.

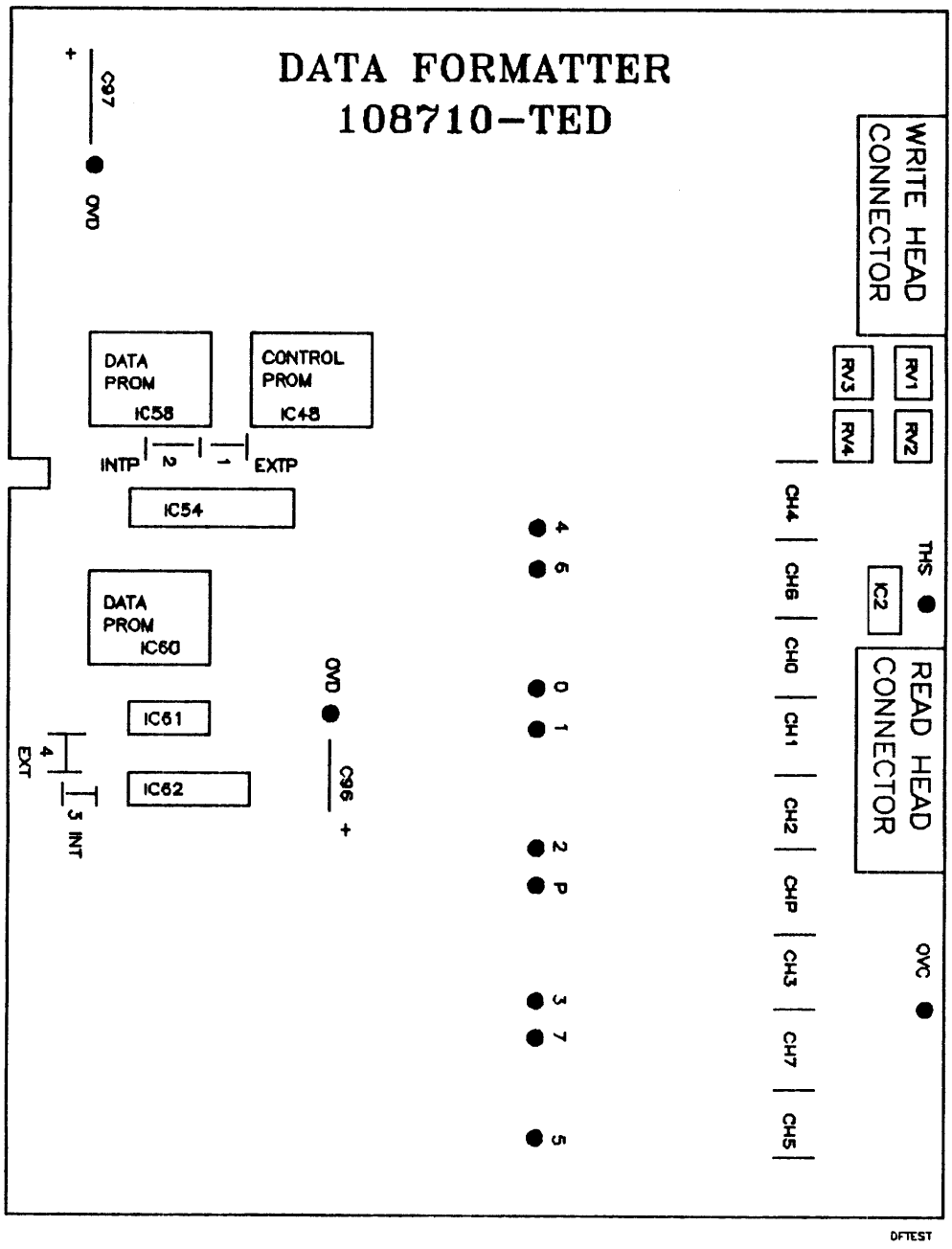


Figure 3-8 Data Formatter PCA

3.2.3 NRZI PCA (Option 800)

Disregard these instructions if Option 800 is not installed.

Place SW1 in position "0" and SW2 in position "1" in order to generate internal parity. The switch positions, Fig. 3-9, are defined as follows:

```
SW1:  0 - Passes check characters across the interface
      1 - Inhibits check characters from the interface

SW2:  0 - External parity selected
      1 - Internal parity selected
```

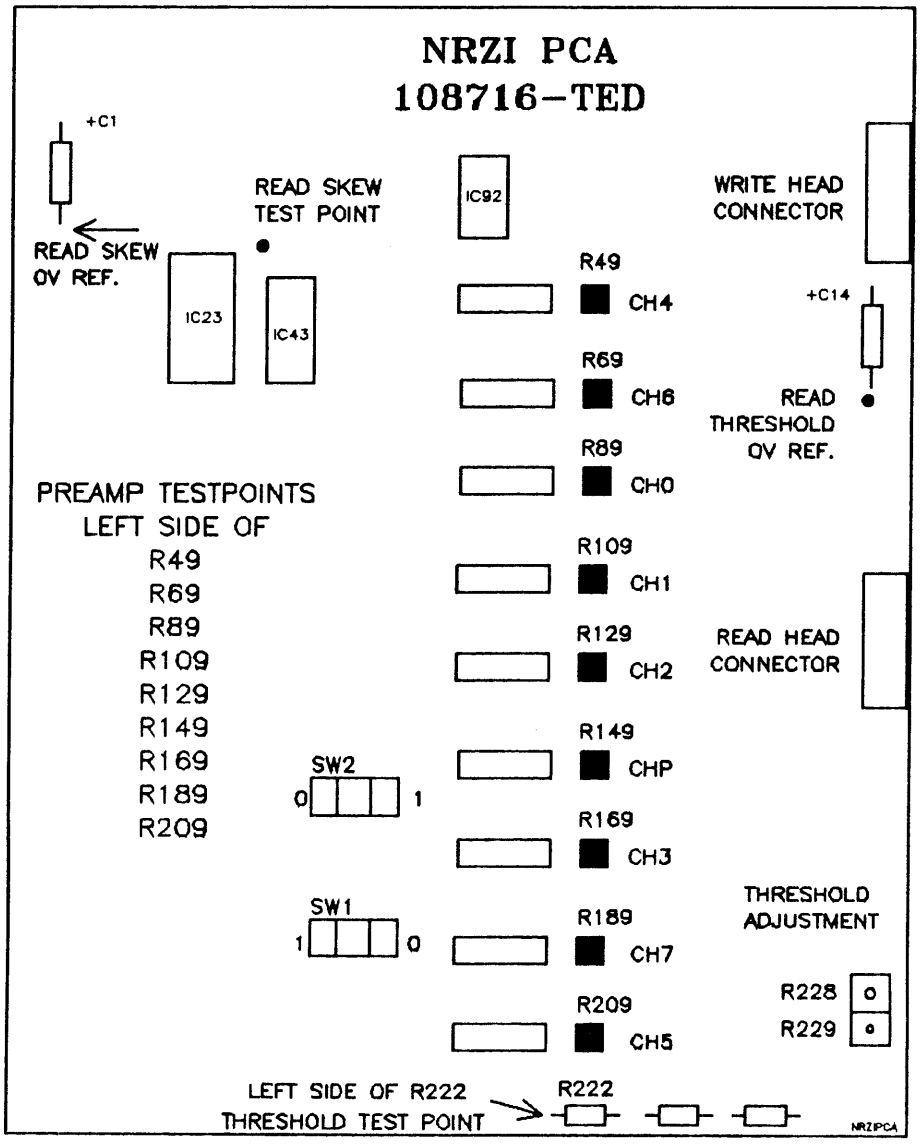


Figure 3-9 NRZI Board Test Points

3.2.4 +5V Regulator PCA

Set SW1 of the regulator to position "1". Refer to Fig. 3-10.

NOTE

Setting SW1 to "0" isolates the +5V output from the transport. If the switch is set to "0", the tension arms continuously cycle up and down. The symptom also occurs if FS8 has blown.

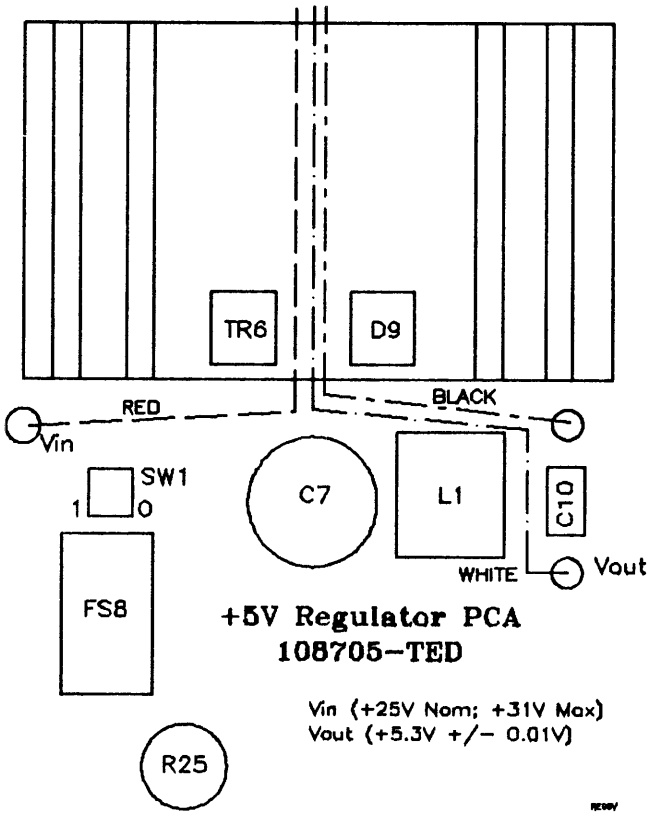


Figure 3-10 +5V Regulator PCA

3.3 CABLING

3.3.1 Internal

Figure 3-11 illustrates the internal cabling. Secure all connections before attempting the checkout procedure.

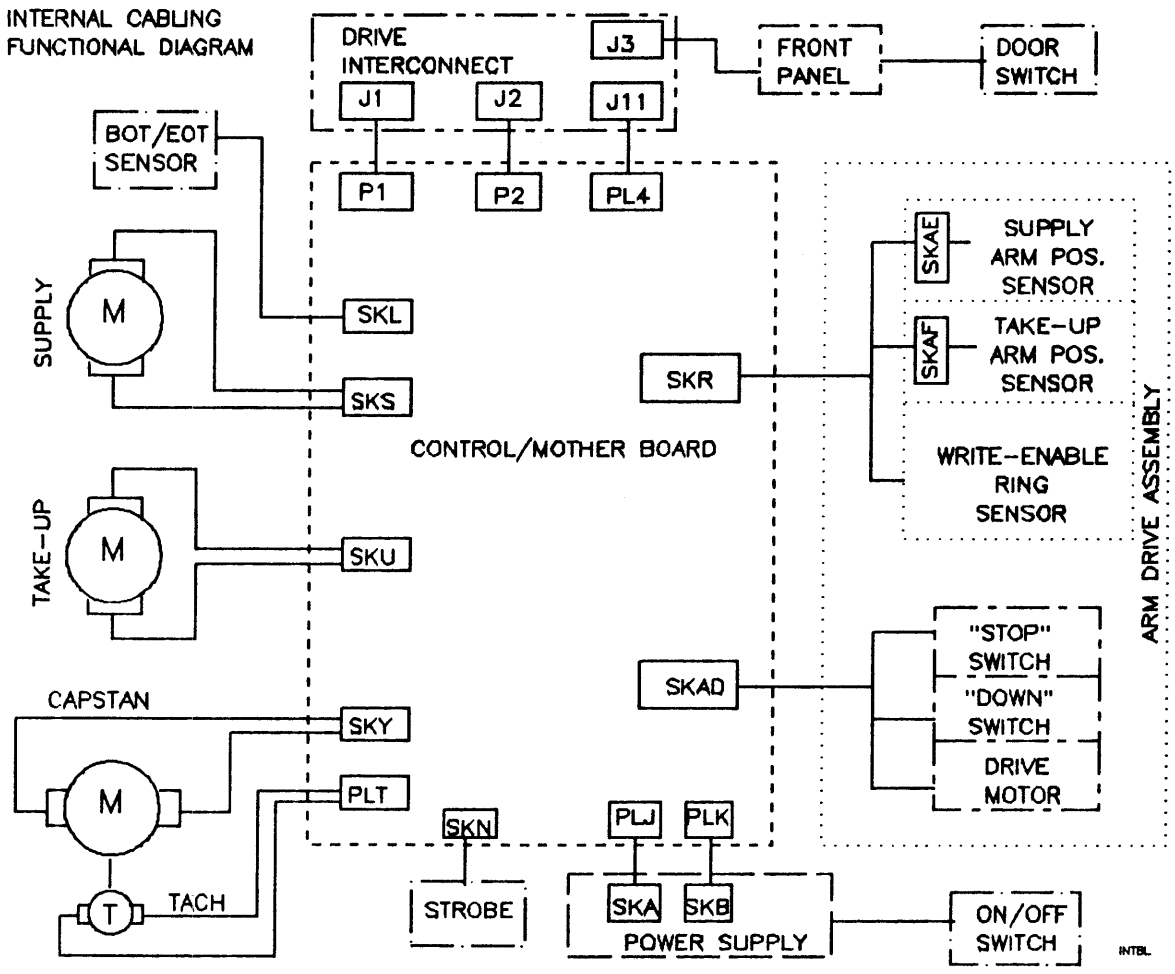


Figure 3-11 Internal Cabling Diagram

3.3.2 External

(a) Assuming the transport casting is open, remove the tie wrap which secures the power cord to the transport supply. Place the loose cord inside the cabinet and push the casting shut.

(b) Open the rear of the cabinet with a flat-blade screwdriver and remove the Customer Accessory Kit from the bottom of the cabinet. Remove the 2 m HP-IB cable from the kit and attach it to the door-mounted connector.

(c) Pull the power cord out through the lower hole in the cabinet door.

(d) Close the cabinet door and lock it.

CAUTION

1. Do not connect/disconnect any IEEE-488 (HP-IB) device to/from a live/active bus.

2. Ensure that the unit power switch is OFF before making connections to the system. (Static discharge from a floating cabinet will damage signal drivers/receivers on an active bus.) 3. Ensure the tape subsystem is plugged into a power receptacle that has an isolated ground.

(e) Connect the power cord and the HP-IB cable to the system.

(f) Change the HP-IB address if necessary.

3.3 SETTING THE HP-IB ADDRESS

CAUTION

Before changing the HP-IB address, make sure that:
1) the host computer is offline or has downed/disabled the tape subsystem
2) the new address is valid for a tape drive.

If the address is changed when the host computer is online or if the address is invalid, the host computer's operating system may halt and cause data loss.

The HP-IB address is factory preset to "1". The following procedure is provided for changing the address if needed. Press the ADDRESS button to display the current address (0-7). Press the Units button until the desired address appears in the display. Use Enter to assign the new address and ADDRESS to exit the address select mode.

[4] CHECKOUT

4.1 GENERAL INFORMATION

4.1.1 Required Equipment

HP 1740A oscilloscope with 10:1 probes (or equivalent with 50MHz bandwidth)
Multimeter: 10mV-250V dc, up to 240VAC
1 known good scratch tape (no edge damage or soft-error problems)
Spring scale (P/N 8750-0039): 0-680 gm; 0-24 oz

4.1.2 Overall Procedure

(a) Complete the preparation steps outlined in Section [2]. In particular, the casting must be open and the leveler feet must be extended.

(b) **Verify the configuration of all PCAs and power supplies.** See Section [3].

(c) Override the door interlock switch by pushing the door switch in and placingthe metal arm, located near the rear of the door switch, between the rear switch washer and the casting. The metal arm will maintain the switch in the "door closed" position until the interlock is reset by pressing the door switch.

Overriding the door interlock switch allows you to test electronic assemblies during tape movement/diagnostic operations. If the door interlock switch is not set, diagnostic programs used in the checkout procedures will not operate.

(d) **In order to ensure proper and safe operation,** perform the following tests of subsections 4.2-4.9 in their given sequence.

4.2 POWER SUPPLIES

(a) Verify the AC input (Figure 4-1), the dc output (Figure 4-2), and the supply voltages (Figure 4-3). Figure 4-4 illustrates the power supply PCA test

points.

(b) Verify that the +5V switched regulator is supplying +5V ±0.2V across C97 on the Data Formatter board (Fig. 3-8) *when all the boards are seated in the card cage.*

(c) When all power lines are present,** the PS OK indicator on the Control/Mother board (Fig. 3-4) should be lit and the voltage at TP12 should be low.

(d) After completing steps (a)-(c), verify the levels at the Vin and Vout test points (Fig. 3-10) of the +5V regulator PCA.

Vin - +25V Nom; +31V Max
Vout - +5.3 V ±0.01V

**Does not include +24 V servo power via FS3.

SUPPLY INPUT (measure at D1/D2 anode)	Nominal	Maximum	Minimum
Within ±10% of supply setting	18.5 V	20.6 V	15.6 V
Within ±1% of supply setting	18.5 V	18.9 V	17.2 V

Figure 4-1 AC Voltages

FUSE	MEASUREMENT (Assuming supply input voltage within ±1% of nominal voltage.)
FS2 (2A)	+24 Vpk ±10% fwr (use an oscilloscope)
FS3 (10A)	+25.4 V max; +20.1 V min
FS4 (10A)	-25.4 V max; -20.1 V min
FS5 (10A)	-15 V max; -12 V min
FS6 (10A)	+15 V max; +12 V min

Figure 4-2 DC Fuse Measurement

REGULATOR	TEST POINT	DC VOLTAGE (MEASURED) NOM	MAX	MIN
+5V *	TP +5V	+5.2V	+5.3V	+5.1V
-5V	TP -5V	-5.0V	-5.2V	-4.8V
+12V	TP +12V	+12.0V	+12.5V	+11.5V
-12V	TP -12V	-12.0V	-12.5V	-11.5V

*Refer to +5 V Adjustment Procedure

Figure 4-3 Regulated Voltage

4.3 MOTOR SPEED

(a) With the multimeter, check the voltage across C97 on the Data Formatter PCA for 5V ±2V.

(b) Mount the scratch tape and run to BOT.

(c) Run diagnostic program *200.* *

(d) Run diagnostic program **64** (High speed Read FWD to EOT).

(e) Time the drift of the capstan strobe dot. The dot should not drift more than 1 dot/2 seconds.**

(f) Run diagnostic program **65** (Low speed read REV to BOT).

(g) Time the drift of the capstan strobe dot. The dot should not drift more than 1 dot/2 seconds.

(h) Run diagnostic program **6** (FWD/REV speed comparison).

4.4 TAPE PATH

(a) Mount a scratch tape and run diagnostic program *200.*

(b) Run diagnostic program **52** (Alternate FWD/REV at low speed) and hold the ONLINE key down until the speed reaches its lowest setting.

(c) Observe the tape motion on the guides and capstan pulley. Tape should not be moving laterally across the capstan or move sufficiently on the guides to distort the edges of the tape.

4.5 TENSION ARM DAMPING

(a) Mount a scratch tape and run diagnostic program *200.*

(b) Run diagnostic program **62** (Write all 1's).

(c) Rewind tape to BOT. (program **30**)

(d) Connect oscilloscope to Channel 2 on the Data Formatter (Fig. 3-8) and trigger from TP4 on the Control/Mother Board (Fig. 3-4).

(e) Run diagnostic program **50** (step FWD, low speed).

(f) Compare the waveform on the oscilloscope to Fig. 4-4.

(g) Run diagnostic program **73** and position the tape to the middle of the reel.

(h) Run diagnostic program **50**. Observe the waveform.

(i) Run diagnostic program **73** and run tape to EOT.

---

*"0" and "100" level diagnostics are written in **BOLD**. "200" level diagnostics are written in *ITALICS*.

**As the capstan spins, an LED behind the capstan shines through the plastic ring and makes the dots appear to be a single dot moving slowly. By timing the "drift", an estimate of the capstan motor speed can be made.

(j) Run diagnostic program **30** for 5 to 6 seconds. This moves the tape back from EOT.

(k) Run diagnostic program **50**. Observe the waveform.

(l) The first overshoot on the waveform for all three tests should be less than 6% of the total waveform amplitude and the third waveform should be less than 2% of the total amplitude.

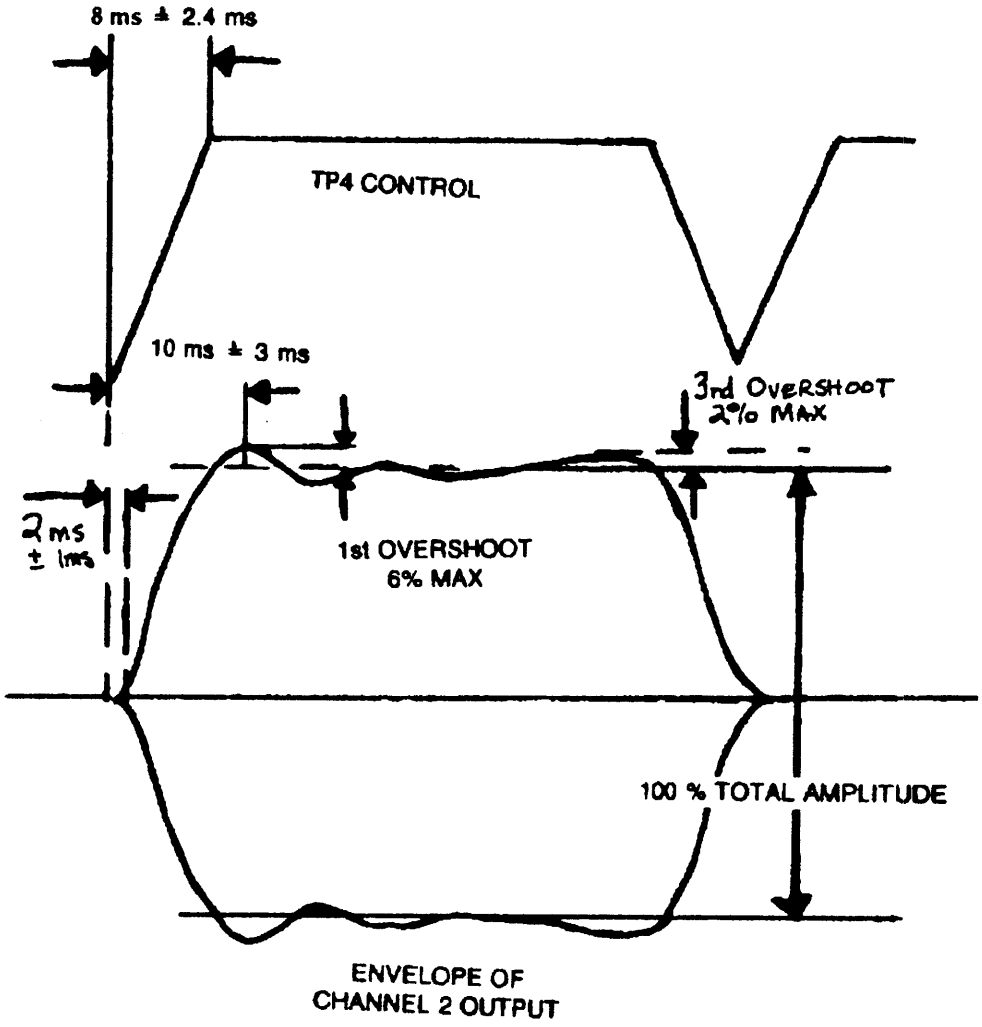


Figure 4-4 Desired TP4 Waveform

4.6 PE READ GAIN

(a) Load a scratch tape and run diagnostic program *200.*

(b) Run, in order, diagnostic program **28** (Select PE), **10** (low speed) and **62** (Write all 1's).

(c) Monitor the analog test points on the Data Formatter (Fig.3-8) for each channel. The peak-to-peak voltage should be 4 V ±1.5 V.

(d) Record the positive peak amplitude with respect to the the 0V test point for each channel.

(e) Calculate:

1. The average value of the nine channel amplitude measurements.
2. The maximum channel amplitude measurement to the minimum channel amplitude measurement ratio. The maximum channel to minimum channel ratio must not exceed 1.38.

(f) Monitor the +THS test point* on the Data Formatter and check for a level within 22%-28% of the the calculated positive peak average. If not within the limits, adjust RV4 until the signal is 25% of the calculated positive peak average.

(g) Rewind the tape (program **30) and run diagnostic programs 9** (high speed) and**62**. Repeat steps (c)-(g) and adjust RV3.

---

*Located on the left-hand side of IC2 in Issue A boards and to the right-hand side in subsequent issue boards.

4.7 NRZI READ GAIN (OPTION 800)

Disregard this procedure if Option 800 is not installed.

(a) Load a scratch tape and run diagnostic program *200.*

(b) Run, in order, diagnostic programs **27** (Select NRZI), **10** and **62.**

(c) Monitor the analog test points on the NRZI board (Fig. 3-9) for each channel and record the positive peak amplitude with respect to 0V TP.

(d) Calculate:

1. The average value of the nine channel amplitude measurements
2. The maximum channel amplitude measurement to the minimum channel amplitude measurement ratio. The maximum channel to minimum channel ratio must not exceed 1.38.

(e) Monitor the THS test point and check for level within 41% to 45% of the calculated positive peak average. If not within the limits, adjust R228 until the level is 43% of the calculated positive peak average.

(f) Rewind the tape (program **30**) and run diagnostic programs **9** and **62.** Repeat steps (c)-(e) and adjust R229.

4.8 DIAGNOSTIC WORKOUT

Load a scratch tape to BOT. Execute diagnostic program *101.* This test (described in Section VIII) checks the main transport operations: tape movement, read/write, and error recognition.

4.9 SYSTEM VERIFICATION

Run the appropriate system verifier.

[5] OPTION 800: 800 BPI NRZI BOARD

5.1 FUNCTION

Option 800 supplies a dual-density head and an 800 bpi NRZI PCA to enable the 7974A to read and write 800 bpi tapes in addition to 1600 bpi tapes.

5.2 TOOLS AND HARDWARE

The following parts and tools are required for installation:

Part Number	Description	Quantity
108716-TED	Tested NRZI PCA	1
108706-TED	Dual Density Head	1
109541-TED	Head Cable Adapter (Write)	1
109542-TED	Head Cable Adapter (Read)	1
07974-90032	Installation Note	1
1400-0249	Tie-cable	4
GS11318-TED	Toroid	1

NOTE

If Option #S10 has been ordered, the Dual Density Head (PN 108706-TED) is not supplied.

5.2.1 Tools Required

Oscilloscope (for Threshold and Read Skew adjustments)
Flat blade screwdriver
Side cutting pliers
Needle-nose pliers
Permanent marker
Electrical tape

5.3 INSTALLATION

(a) Open the casting and override the door switch.

CAUTION

Ground yourself to the cabinet and observe standard electrostatic-discharge (ESD) precautions when installing this option.

(b) Remove the head deskew prom, *in its socket*, from the carrier plate on the rear of the head plate assembly and insert it into the socket at position IC92 on the NRZI PCA (P/N 108716-TED). See Fig. 5-1.

(c) Place NRZI PCA switch SW1 in position "0" and SW2 in position "1". The switch positions are defined as follows:

SW1: 0 - passes check characters across the interface
1 - inhibits check characters from the interface

SW2: 0 - External parity selected
1 - Internal parity selected

(d) Insert the NRZI PCA into the far left (outermost) slot of the transport card cage. Place the Data Formatter PCA (P/N 108710-TED) into the adjacent slot.

(e) Attach the head cable adaptors (P/N 109541-TED and 109542-TED) to the NRZI and Data Formatter boards. Connect the head leads to the center connector.

(f) Apply two strips of electrical tape to the machined mounting pad on the rear of the Thorn casting (see Figure 5-4).

NOTE

If the assembly state of the +5V Regulator is "12" or above, omit steps (g) through (j). On these units the ferrite ring (toroid) is not required.

(g) Detach the spade plug from position 3 (red wire, clear plug leading to Vin on the +5V regulator PCA) on the transport power supply PCA. (See Fig. 5-2).

(h) Attach the ferrite ring (toroid) to the wire, wrapping it as shown in Figure 5-3. Re-connect the spade plug to the transport power supply PCA.

(i) Use the cable ties as follows (See Figure 5-2):
-to secure the ferrite ring (toroid) to the cable clip
-to wrap the cables as they pass over the +5V regulator PCA
-to secure the cables to the rear of the power supply PCA
-to wrap the cables close to the plug before connection to position 3

(j) With a permanent marker, mark out "11" on the assembly state label attached to the heat sink on the +5V regulator PCA.

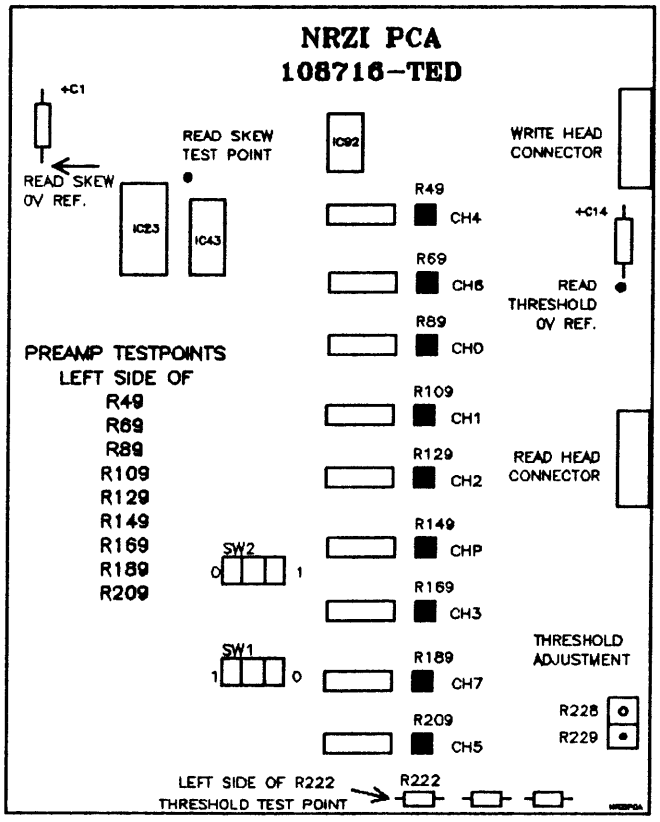
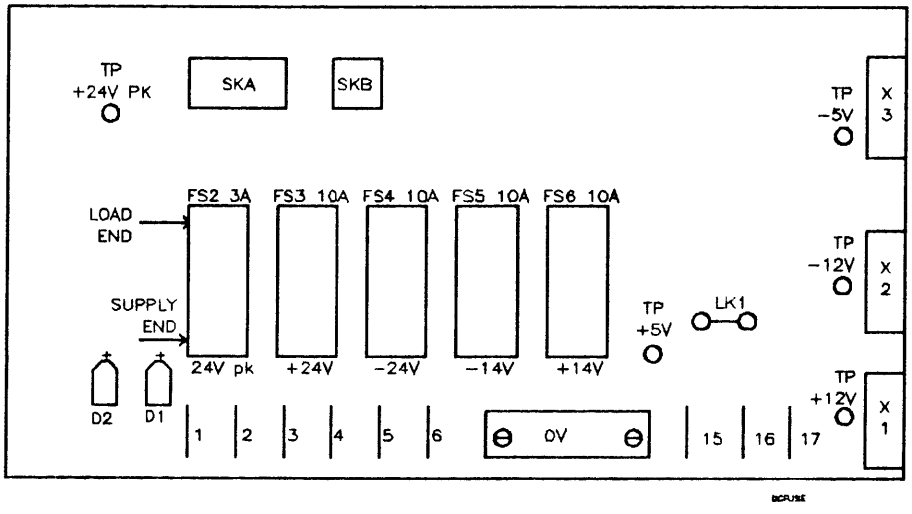


Figure 5-1 NRZI Board Test Points



TRANSPORT POWER SUPPLY PCA
105678-TED

Figure 5-2 Transport Power Supply PCA

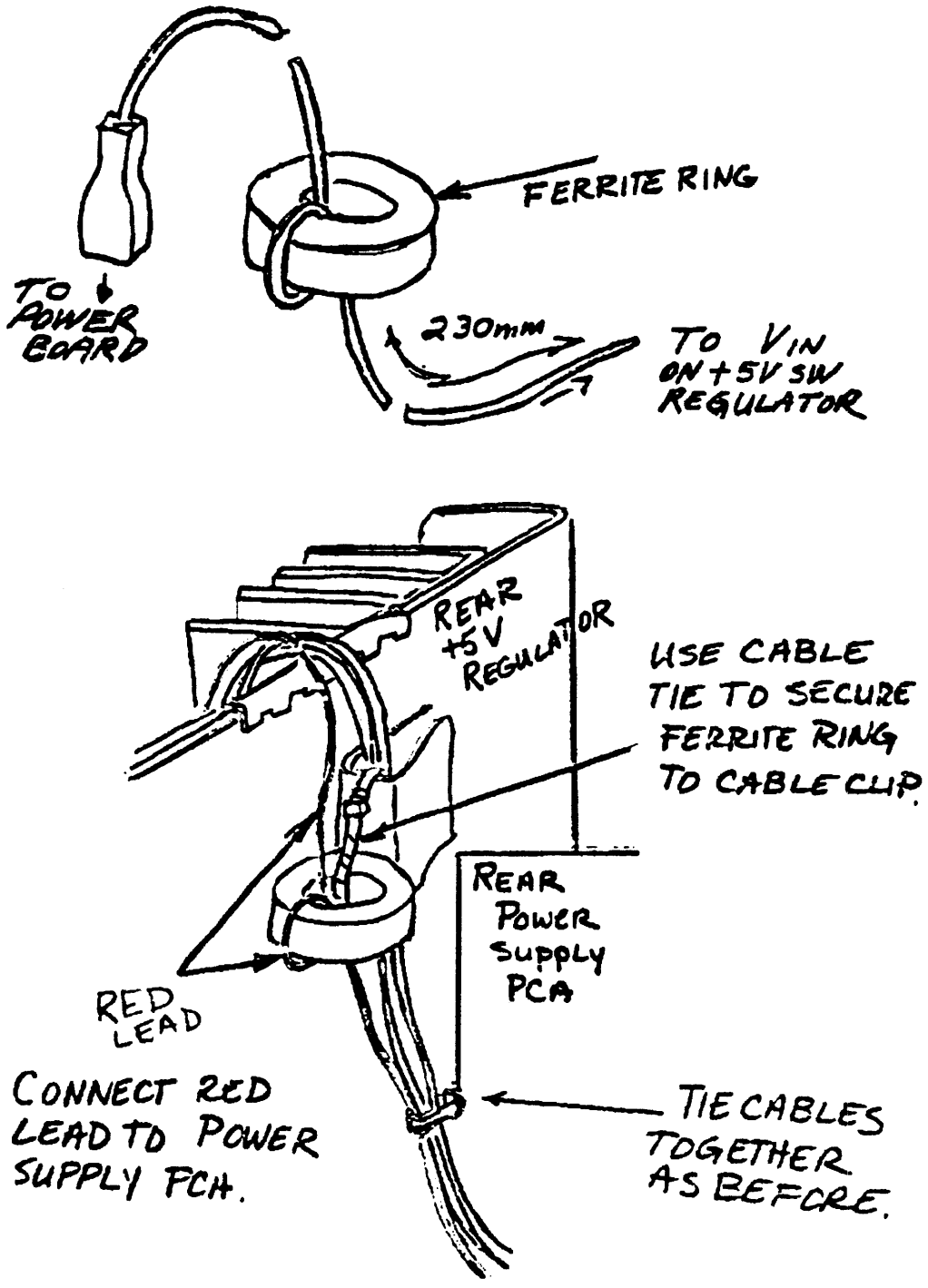


Figure 5-3 Ferrite Ring Placement

5.4 CHECKOUT

5.4.1 Read Gain

(a) Load a scratch tape and run diagnostic program **200**.

(b) Run, in order, diagnostic programs **27** (Select NRZI), **10**, and **62**.

(c) Monitor the analog test points on the NRZI board (Fig. 5-1) for each channel and record the positive peak amplitude with respect to 0V TP.

(d) Calculate:

1. The average value of the nine channel amplitude measurements.
2. The maximum channel amplitude measurement to the minimum channel amplitude measurement ratio. The maximum channel to minimum channel ratio must not exceed 1.38.

(e) Monitor the THS test point (R222) and check for level within 41% to 45% of the calculated positive peak average. If not within the limits, adjust R228 until the level is 43% of the calculated positive peak average.

(f) Rewind the tape (program **30**) and run diagnostic programs **9** and **62**.

(g) Repeat steps (c) through (e) and adjust R229.

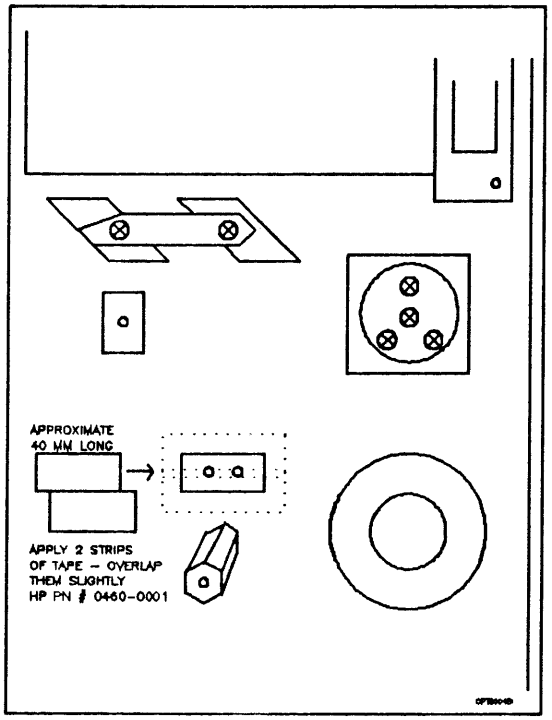


Figure 5-4 Tape Placement on Mounting Pad

5.4.2 Read Skew

(a) Load a master skew tape to BOT.

(b) Run diagnostic programs **10** (low speed) and **63** (Read FWD to EOT).

(c) Attach the oscilloscope to the read skew testpoint (Fig. 5-1), ground the scope at -VE end of C1, and observe the inverted-waterfall waveform (See Fig. 5-5). Measure the inter-channel displacement error TD, representing both static and dynamic skew. This should be within 3 microseconds when checking or 2.25 microseconds when adjusting.

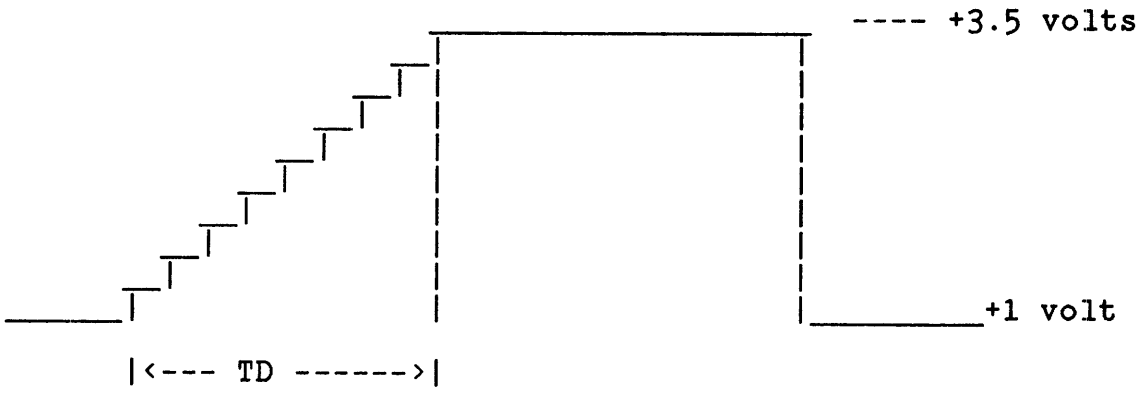


Figure 5-5 Inverted-waterfall Waveform

NOTE

If all 1's are read, nine steps should appear in the rise. However, if any other data pattern is read, the number of steps in the "waterfall" equals the total number of active channels, and the overall vertical displacement remains +1V to +3.5V.

d) Run diagnostic program **82** (NRZI read skew test) as a confidence check.

(e) Unload the master alignment tape and load a scratch tape.

(f) Select diagnostic program **83** (NRZI write skew test), and monitor the read skew test point (Fig. 5-1). Check that the skew is within the limits of step (c).

(g) Select diagnostic program **9** (high speed) and repeat step (f) for a 100 ips confidence test.

This page intentionally left blank.

CONTENTS: SECTION IV

---FIGURES---

This page intentionally left blank.

PREVENTIVE MAINTENANCE

SECTION IV

[1] CLEANING SCHEDULE GUIDELINES

There are no Preventive Maintenance duties other than having the customer clean the tape path on a regular basis. An emphasis is placed on the word **regular** because regular cleaning improves performance, reduces read/write errors, and lengthens tape life. Frequent cleanings also require fewer cleaning materials and are relatively quick. How often a unit must be cleaned depends upon three factors: usage, operating environment, and tape quality. The following definitions should be used as guidelines for developing an appropriate cleaning schedule.

MINIMUM: A thorough cleaning of the tape path every shift (eight hours). Minimum cleaning is appropriate under the following conditions:

- less than 10 reels are used per shift (eight hours)

- there is no visible debris on tape head after each reel of tape

- there is no reason to suspect a high level of dust in the computer center from vacuuming, delivery of supplies, etc.

NORMAL: A thorough cleaning of the tape path after every 10 reels of tape (roughly every 1.5 hours of continuous running). Normal cleaning is appropriate under the following conditions:

- more than 10 reels are used per shift

- there is no visible debris on the tape head after each reel of tape - there is no reason to suspect a high level of dust in the computer center.

HEAVY: A thorough cleaning of the tape path after each reel of tape under the following conditions:

- visible debris appears on the tape head after each reel of tape

- uncleaned interchange tapes from outside your computer center are being read

- uncleaned new tapes which have been used only once or twice are being used (new tapes usually contain additional debris from the slitting process during manufacture).

SPECIAL: One thorough cleaning of the tape path under the following conditions:

- abnormal dust level in the computer center because of custodial activity, equipment moves, supply delivery, etc.

- extended periods (days) of tape drive inactivity prior to use.

Most users find that they need to clean the transport once after every eight-hour work shift. Appearance of any of the problems listed in Section [3] or the excessive soft-error rate message >ERR, indicate that the cleaning cleaning schedule must be increased. If an increased cleaning schedule does not improve reliability, check the tapes being used. Are the tapes old, worn, or kept in a dirty environment? All old and worn tapes should be copied immediately and then discarded. If a dirty environment is suspected, consult with the customer on ways to remedy the situation. If problems persist after taking all the steps outlined, thoroughly check the transport for read/write problems or mechanical failure due to excessive wearing of the head.

[2] CLEANING SUPPLIES

2.1 Cleaning Solvent

HP supports ONLY the use of LIQUID Freon TF (trichlorotrifluorethane) as a tape path cleaning solvent. Freon TF cuts oil and grease, evaporates quickly, leaves no residue, and will not damage the transport. If a vendor other than Hewlett-Packard is used, make sure that the cleaning fluid is a high quality solution of 80% Freon TF and 20% isopropyl alcohol. Avoid solutions of Freon TF and other solvents.

CAUTION

Do not use cleaner solutions which contain lubricants. They deposit lubricant on the tape head and degrade performance.

Do not use soap and water on the tape path. Soap leaves a thick film and water may damage electronic parts.

Do not use standard hub cleaners or strong alcohol solutions (>20%). These solutions damage the tape guides and capstan.

Do not use aerosol cleaners; even if they are freon TF. The spray is difficult to control and often contains metallic particles which damage the tape head.

2.2 Wiping Materials

We recommend the use of disposable, lint-free foam swabs similar to the ones foam swabs similar to the ones supplied with the HP 7974A. They allow the cleaning fluid to be applied accurately and minimize cleaning waste.

CAUTION

Do not use facial tissues or cotton-tipped swabs. Although seemingly effective, they introduce highly abrasive lint into the tape path.

Discard all cleaning tools after use. Even if they appear clean, they will contaminate the tape path when re-used.

[3] TAPE RELATED TRANSPORT PROBLEMS

Many transport problems can be traced to either improper cleanings or the use of poor quality tapes that leave oxide and binder on the tape path. Without frequent cleaning, collected particles contaminate tapes, cause transport failure, and, in extreme cases, ruin the tape head. Replacing the head is costly and unnecessary if the system is cleaned regularly. When you clean the transport, inspect the path carefully and watch out for any of the following problems:

BROWN STAINING: Low humidity levels (<40%) cause brown deposits of oxide to accumulate on the head. Brown staining cannot be removed with ordinary cleaning solvent and will grow with continued exposure. As the stain grows, tape-to-head separation increases until the head becomes useless. Once ruined, the head must be replaced.

CLEAR FILMING: Every time a tape is used it sheds oxide and binder which forms a clear film upon the head and cause tape-to-head separation errors occur. If not removed frequently, clear films can build up until cleaning with solvent is no longer effective and replacement of the head becomes necessary.

CAPSTAN SHINING: This occurs when the urethane or neoprene coating is worn off the capstan. As a result, tapes slip and the drive loses track of the tape location.

NOTE

Worn tapes and/or a worn head significantly increase the chances of capstan shining. Watch out for excessive retries when reading a tape. Diagnostic test 105 can help you identify this problem.

[4] CLEANING PROCEDURE

(a) Run some tape and visually check for tape scraping on the guide flanges or uneven travel on the capstan pulley. If tape reel flanges scraping is observed, verify that the reel is properly seated on the hub.

(b) Rewind and remove tape.

(c) Remove the head covers to expose the head plate assembly.

(d) Lift up the flux shield and visually examine the read/write and erase heads. Look for tape deposits, scratches, or burrs.

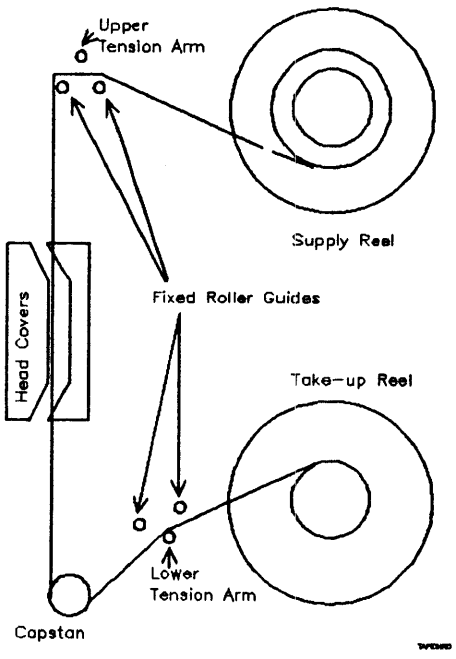


Figure 4-1 Tape Path

(e) While holding the flux shield open, clean the read/write and erase head with a foam swab dampened in HP head cleaner or freon. Apply pressure in the direction of the tape path.

CAUTION

Avoid contacting the EOT/BOT sensor. The solvent may degrade its performance.

(f) Use a lint-free cloth dampened with HP head cleaner or freon and clean the capstan pulley. Ensure that no lint remains.

(g) Use a foam swab dampened in HP head cleaner or freon and clean the tape cleaner and the fixed guides. Inspect the blade when cleaning: it must be sharp and free of nicks. Replace the blade if it appears damaged.

CAUTION

The tape cleaner has two sharp blades and should be cleaned with extreme care.

(h) Use a foam swab dampened in HP head cleaner or freon and clean the tape roller guides.

WARNING

Roller guides are pre-greased. Cleaning fluid should be used sparingly. At no time should spray cleaner be used on the roller guides.

(i) Replace the head cover and discard all used cleaning materials.

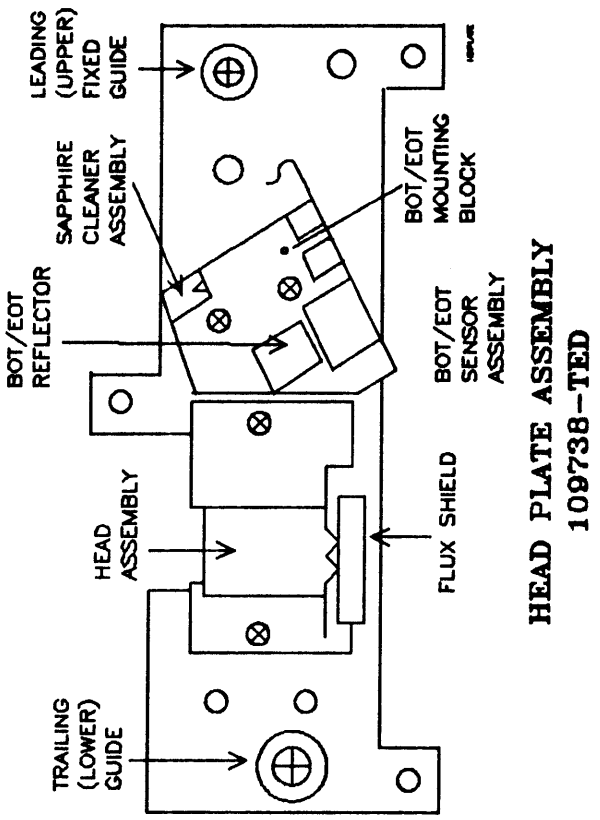


Figure 4-2 Head Plate Assembly

[5] TAPE MANAGEMENT

5.1 Tape Problems

Most tape failures are caused by physical abuse or poor storage methods. Accidental erasure rarely occurs because the tape packaging provides substantial protection in most office type of environments. The following list describes the most serious problems and their normal causes.

LEVEL ERRORS -- The "read" signal is too low. These errors are caused by excess particles on the tape head.

NOISE ERRORS -- The "read" signal is too high. These errors are most often caused by lack of oxide on tape (for example, a scratch or cut on the tape surface).

OXIDE SHEDDING -- Oxide coatings tend to become brittle or soft due to temperature extremes, age, and/or excessive use. The oxide then comes off of the binder, clogs the tape path and creates soft error problems.

NOTE

New tapes shed easily because excess oxide is leftover from the manufacturing process. After the first two or three times a new tape is used, you should clean the tape path before mounting the next tape.

TAPE STICK -- High temperatures and humidity cause tape binder to soften and stick to the drive head. Large areas of oxide are usually lost in the process.

BLOCKING -- High temperature causes layers of tape to stick together. The sticking disturbs tension and may remove oxide coating.

EDGE DAMAGE -- High pressures on the edge of the tape damage the outer tracks. Once deformed, the damage worsens with use. Edge damage is a major source of signal dropout on outer tracks.

CINCHING -- When a spinning reel is suddenly stopped, the outer layers of tape continue to spin momentarily and cause loose windings within the pack to bunch up.

PACK SLIP -- It appears as "steps" in an otherwise smooth winding. If a tape is wound at low tension, sections will shift when subjected to rough handling, impact, vibration, or thermal stress. Pack slip causes uneven winding and rewinding. As a result, edge damage frequently occurs when the tape is caught by the reel flange or transport guide edges.

5.2 Tape Care Guidelines

The suggestions in this section are mainly common sense. By following them whenever possible, you'll reduce recording errors and lengthen tape life.

Storage

Keep tapes in a clean environment at all times. Exposure to dust and other particles, such as food and cigarette smoke, degrades tape performance. Choose storage areas away from frequently used doors and walkways to reduce sources of contamination.

A constant temperature of between 18° and 24°C (65°F to 75°F) and a relative humidity between 40% to 60% (non-condensing) is recommended in the storage area. Tapes subjected to extremes in temperature or humidity are frequently ruined as a result of sticking problems or brittleness.

The end of the tape should always be secured either by a vinyl strip or a foam pad to prevent the pack from losing its tension.

All tape reels should be hung vertically in protective casings or canisters.

Horizontal stacking is not recommended because bottom tapes are subjected to pressures which may cause edge damage. If absolutely necessary, metal canisters can be used for stacking but care must be taken to prevent damage.

During long term storage, dust contamination is easily reduced by sealing canisters in plastic bags. Clean the bags before removing the tapes.

Transportation

When transporting tapes from one location to another, pack tapes in water-resistant containers. To maintain proper tensioning, the end of the tapes should be secured. Avoid physical shock and extreme changes in temperature.

Handling

Hold the reel by the outer edges.

Do not pick up the reel by the flanges; they are easily bent. Once bent, the tape cannot unwind evenly. Uneven winding interferes with tensioning and eventually causes edge damage.

Do not shake the tape. This causes pack slip.

Prevent sharp blows to the reels. The reel could fracture and damage the tape.

Winding

The HP 7974A drive establishes a nominal tape tension of 269 gm (9.5 oz) order to insure smooth tape movement and accurate data transfer. However, if the transport is not loaded correctly, your tapes can be damaged. For instance, excessive tension permanently distorts the tape's polyester backing while loose tension causes cinching. In short, to maintain the proper tape tension, you must load the transport properly.

To prevent the pack from losing its tension while in storage, secure the end of the tape with either a vinyl strip or a foam pad when you remove it from the transport.

Adopt a program of regular inspection, winding, and rewinding of stored tapes every six to nine months to insure wind quality.

Tapes can be contaminated if they are wound onto dirty reels. Clean empty reels before using them.

5.3 Resource Material

For those who wish to learn more about tape care, the publication *Handling and Storage of Computer Tape* can be obtained from:

Technical Service
Data Recording Products Divison
3M Corporation
3M Center
St. Paul, Minn 55101

CONTENTS: SECTION V

---FIGURES---

This page intentionally left blank.

[1] INTRODUCTION

Figure 1-1 gives the overall block diagram of the HP 7974A . To simplify the discussion slightly, the tape drive is divided into two functional groups: the Interface Controller Unit and the Tape Transport. The Interface Controller Unit (ICU) functions as the communications link between the host computer and the tape transport. Four boards compose the ICU: the HP-IB Interface, the ICU Power Supply, the Drive Interconnect, and the Master Controller. The remaining PCA's and mechanical assemblies are discussed as part of the Tape Transport.

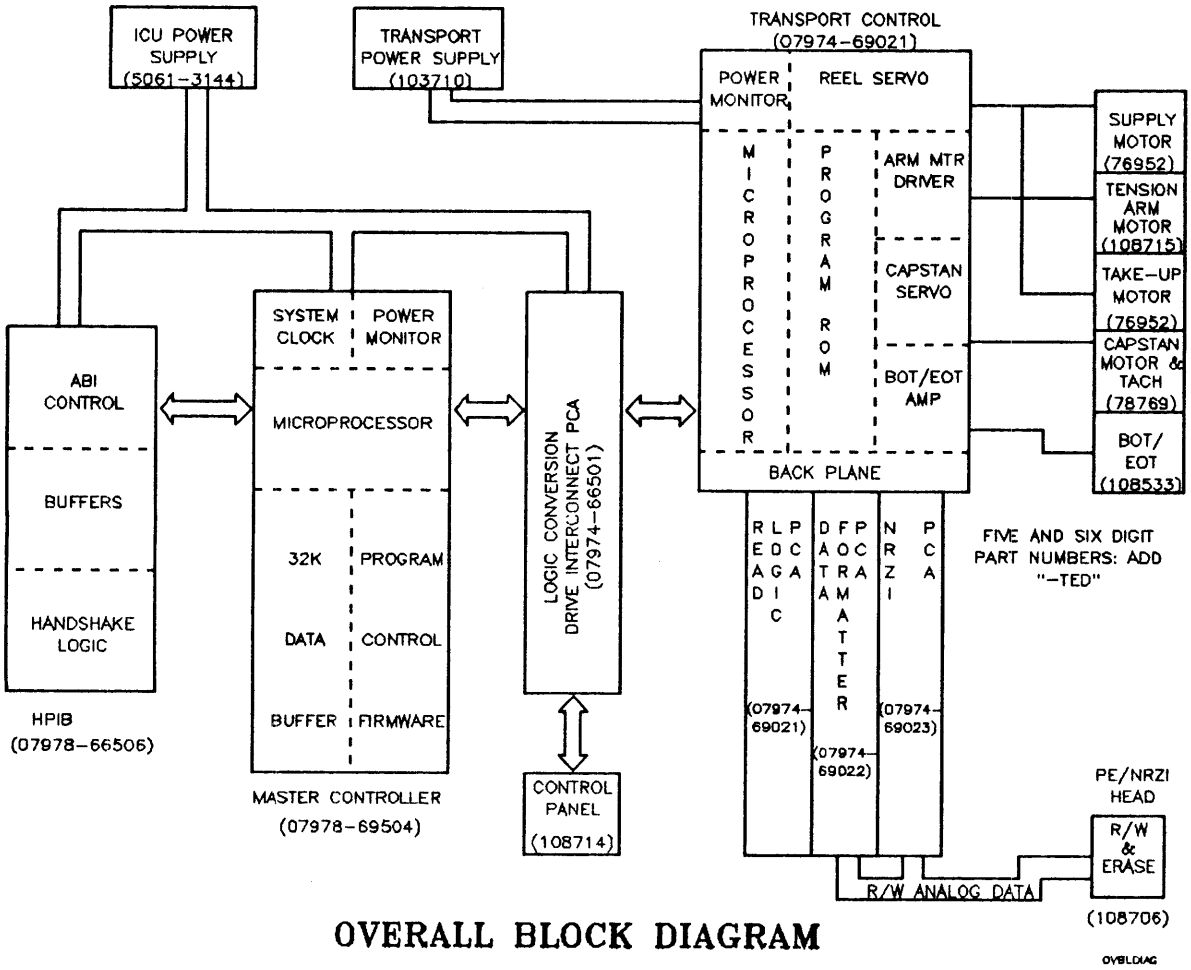


Figure 1-1 Overall Block Diagram

[2] INTERFACE CONTROL UNIT

2.1 HP-IB INTERFACE BOARD

The key component of the HP-IB Interface board is the ABI controller. It provides high speed interfacing between the HP-IB link, the Master Controller, and the Data Buffer. Also, together with the four transcievers on the board, the ABI chip provides complete electrical and logical interfacing. (Other major components of the HP-IB board include buffers and handshake logic circuits. However, these are not discussed because it is assumed that most people are familiar with their general purposes.)

To the Master Controller (MC) microprocessor, the HP-IB board appears as a set of registers. Eight of these registers are in the ABI. The MC interacts with the board by reading and writing to the ABI registers. This allows the MC to set the transfer conditions, transfer direction, HPIB address of the board, send data to the host, read the status of the ABI chip, determine the reason for an interrupt, receive data from the host, etc.

The lines provided by the ABI chip for interfacing to the Master Controller and buffer include the following:

- a 10-bit-wide data bus
- three register select lines for selecting among eight registers
- a data direction line for specifying either writing or reading to the selected register
- handshake lines to coordinate the data transfer
- an interrupt line to alert the Master Controller.

The interfacing between the I/O board and the Master Controller processor is done through the PROCESSOR CONTROL BUS, PROCESSOR DATA BUS, and the INT line. The interfacing between the I/O board and the buffer is done through the BUFFER CONTROL BUS, BUFFER DATA BUS, and the EOR and PAR lines.

The remaining registers on the HP-IB board are located in the EXT REG block. These registers are the CONTROL, STATUS, and LATCH registers. The CONTROL register is used to control the read/write operations for the HP-IB buffers and to enable/disable all interrupt. The STATUS register flags the operations presently being performed by the HP-IB interface. Finally, the LATCH register contains the last byte transferred from the ABI chip to the buffer. Also, to prevent data loss, the LATCH will hold a secondary command byte recieved from the host during an "HP-IB to buffer" transfer.

The formats for the CONTROL and STATUS registers are as follows:**

**-L and -H added to a line designator means active LOW and active HIGH respectively.

CONTROL REGISTER (write only) - address 18810H

MSB 6	5	4	3	2	LSB 1
INT CLR	PINT CLR	BUFF READ	BUFF WRITE	INT DIS	

BIT 1 - not used

BIT 2 - INT DIS. When this bit is set HIGH, the interrupts from the I/O board to the Master Controller board are enabled. When this bit is set LOW, the interrupts are disabled and the INT-L line is tri-stated

BIT 3 - BUFF WR. When this bit is set HIGH the transfers from buffer to ABI are enabled. This means that a buffer write request (IWRQ-L) is generated for the buffer and when a byte is received IOGO-L will be generated for the ABI. This bit should never be set HIGH when BIT 4 is HIGH.

BIT 4 - BUFF RD. When this bit is set HIGH the transfers from ABI to buffer are enabled. This means that IOGO-L is generated for ABI when a byte becomes available. Consequently, a read request for the buffer (IRRQ-L) is generated. This bit should never be set HIGH when BIT 4 is HIGH.

BIT 5 - PINT CLR. When this bit is set LOW the parity error interrupt (PAR INT) is cleared. This bit must be set HIGH to enable parity error interrupts.

BIT 6 - INT CLR. This bit has the same function as BIT 5 except for EOI interrupt, SEC interrupt, and EOR interrupt.

STATUS REGISTER (read only) - address 18812H

MSB 8	7	6	5	4	3	2	LSB 1
ABI INT	PAR INT	EOR INT	SEC INT	EOI INT	WR+RD	IRRQ-L	IWRG-L

BIT 1 - IWRQ-L. Represents the status of IWRQ-L line.

BIT 2 - IRRQ-L. Represents the status of IRRQ-L line.

BIT 3 - WR+RD. This bit is set when BUFF WR or BUFF RD bits are set in the CONTROL REGISTER.

BIT 4 - EOI INT. This bit is set when an End-of-Information interrupt is generated.

BIT 5 - SEC INT. This bit is set when a Secondary Command interrupt is generated.

BIT 6 - EOR INT. This bit is set when an End-of-Record interrupt is generated.

BIT 7 - PAR INT. This bit is set when a parity interrupt is generated.

BIT 8 - ABI INT. This bit is set when an ABI internal interrupt is generated.

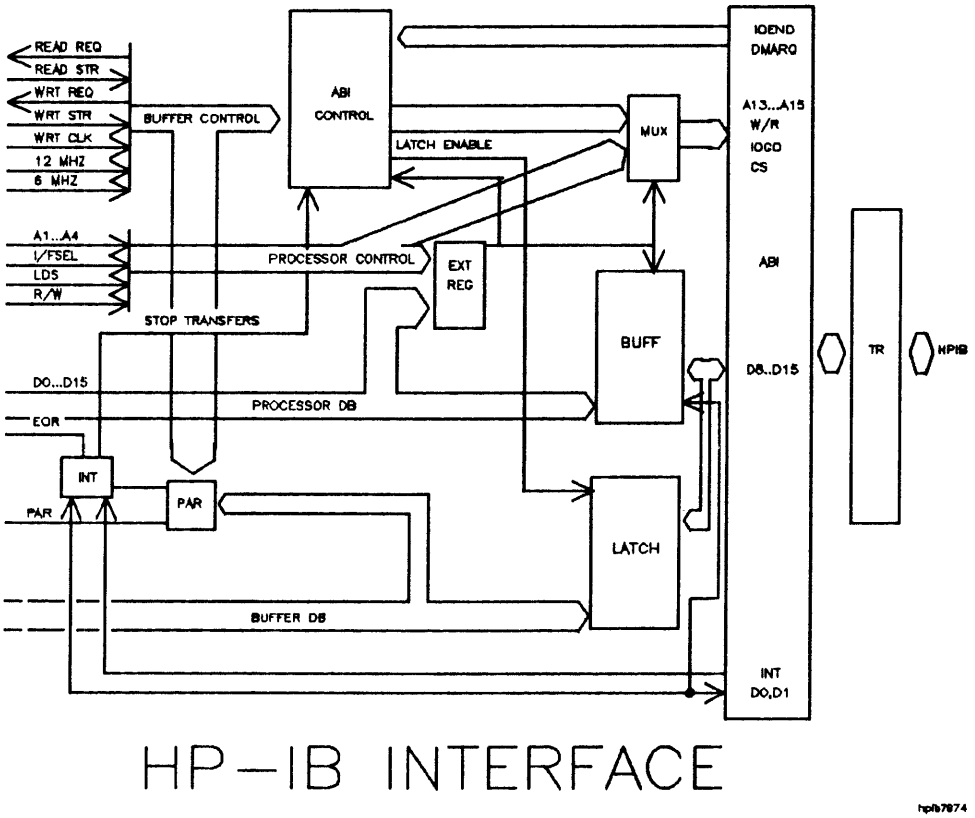


Figure 2-1 HP-IB Block Diagram

2.3 ICU POWER SUPPLY

The ICU power supply generates the logic levels needed by the other ICU boards. It operates at 50-60 Hz and may be configured for either 115 VAC or 230 VAC The signals generated are:

PVAL - Power Valid: Used by the Master Controller; Indicates that supply lines are up.

KEY - Not Used.

+12P - +12 V supply, unregulated: Used by ICU power supply control circuitry.

+12V - +12 V supply, regulated: Used by EEPROMS on Master Controller

+5V - +5 V supply, regulated: Logic supply for Master Controller, HPIB, and Drive Interconnect boards.

RET - DC Ground.

-12 V - Not Used.

As seen from the block diagram of Fig. 2-2, the supply is a simple switching supply. The switch transistor loads energy into the primary side of the output transformer when it is on. When the switch turns off, positive voltage appears at the secondary side of the output transformer and power is delivered to the output circuits. The switching cycle is regulated by the error amplifier and comparator control circuitry in order to adjust to load fluctuations.

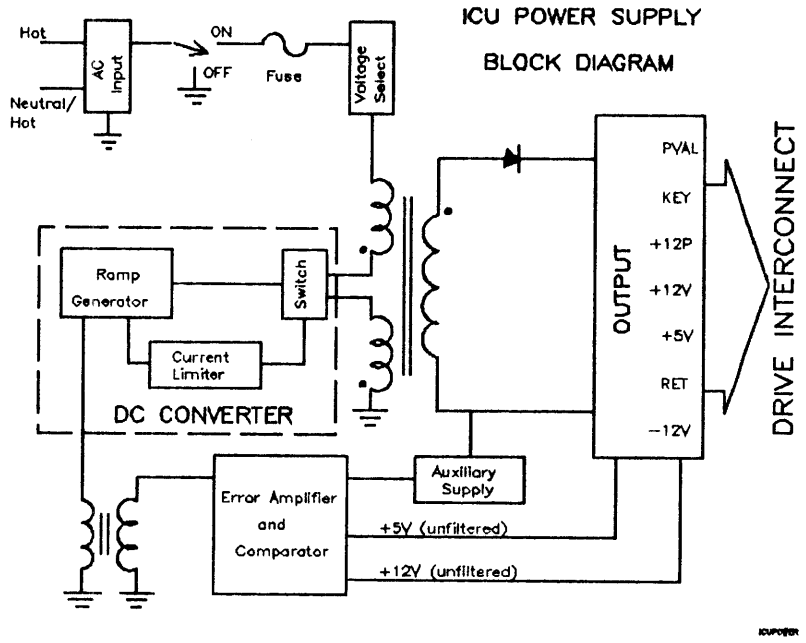


Figure 2-2 ICU Power Supply Block Diagram

2.4 DRIVE INTERCONNECT BOARD

The drive interconnect board links the ICU and Transport electronics. As seen in Fig. 2-3, its operation is dictated by the Master Controller (MC). The board is partitioned into three main modules: Front Panel Transfer, Command/Status Transfer, and Data Transfer. Their functions are outlined as follows.

Front Panel Transfer Module

Display:

- Loads Front Panel Display vial ASCII encoded data lines and write strobe
- Permits Latching of "Virtual Display" by transport and polling by MC

Buttons:

- Permits poling of Front Panel Buttons
- Permits latching of "Virtual Buttons" read by transport
- Buttons and switches are software debounced; except RESET is latched

LED's:

- Permits latching of LED's off/on drivers
- Permits polling of transport LED drivers

Command/Status Transfer Module

Drive Select:

- Grounds the Drive Select lines: permanently selects drive

Status:

- Allows for polling of transport status and handshake lines

Drive Commands:

- Permits transfer of 5 encoded command lines (plus IHISP,IDLG) synchronized with GO pulse
- Permits pulsing of Rewind command line
- Hardwires Offline command to +5V
- Permits enable/disable of Formatter Enable command line

Data Transfer Module

Data Transfer:

- Permits unattended Read/Write data transfer between the Data Buffer and the Data Formatter/NRZI board

Sense Byte Read:

- Allows the MC to read Sense Bytes via Read Data lines

Interrupts:

- Interrupts the MC when Overflow/Underflow error occurs
- Interrupts the MC at end of each Sense Byte read during Read Sense Byte Block command
- Interrupts the MC at end of each data record transferred
- Allows the MC to determine which interrupt was sent and the module state (i.e. Read, Write, Sense Byte)

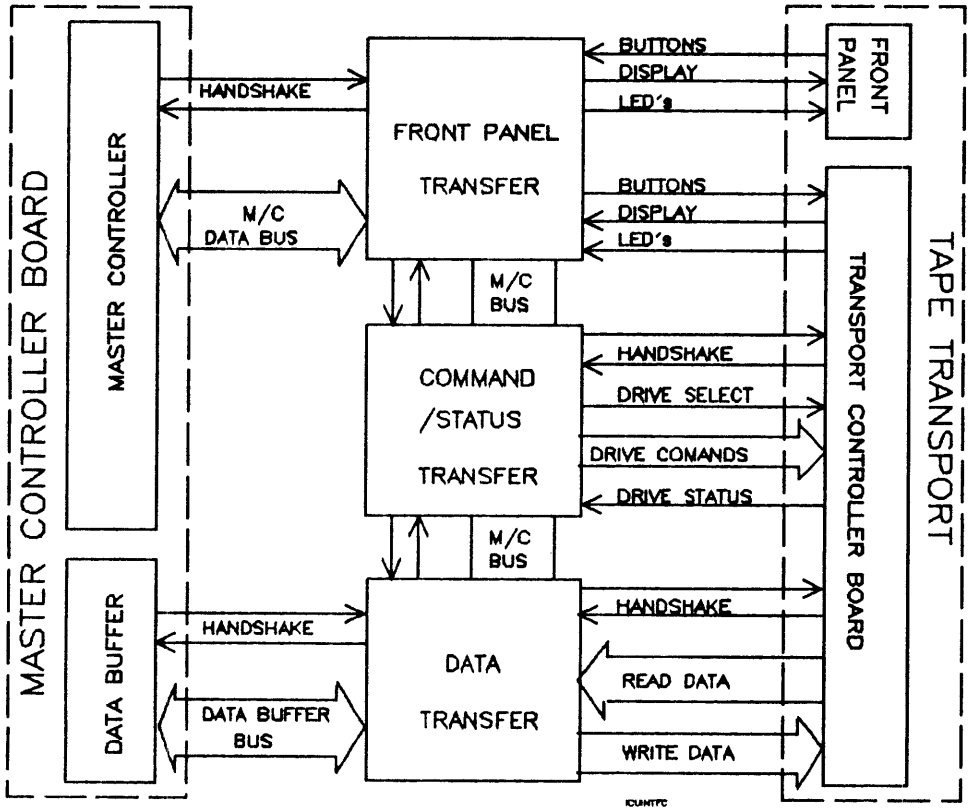


Figure 2-3 Drive Interconnect Block Diagram

2.5 MASTER CONTROLLER BOARD

The Master Controller PCA is unique because it contains two major subsystems: the Master Controller (MC) and the Data Buffer (DB). These subsystems share the same power and clock signals and many of the same bus lines. However, to simplify the discussion, the MC and the DB are examined as if they were completely independent. Power, clock, and bus lines are discussed within *Test Points and Connections*, subsection 2.5.3.

2.5.1 Master Controller

As seen from the block diagram of Fig. 2-4, the MC is a simple microcomputer. This microcomputer consists of a high performance MC68000 microprocessor, miscellaneous microprocessor bus control circuits, ROM, RAM, EEPROM, a programmable timer, I/O bus interface circuitry, system clock generators, and a +21 V supply for the EEPROM logic.** Basically, the MC monitors and coordinates all subsystem functions necessary for normal tape operation and running diagnostic programs. It intercepts commands from the host, dissemminates the information, and checks to make sure the information reaches its destination. The "checking" process can become a little tricky since the MC must communicate with two types of subsystems which have very different timing requirements. Subsystems which communicate with the MC by means of a custom designed universal state machine (USM) must do so only on certain clock edges, while other subsystems can perform transfers asynchronously.

Data transfers between the MC and USM-based subsystems (DB, Write Formatter, Data Detect and Deskew, Read Formatter) or the HP-IB Interface are accomplished by inserting wait states into the processor memory cycle until the subsystem hashad enough time to complete the transaction. The MC then waits for a handshake from the subsystem to be asserted before it completes the bus cycle. Each USM subsystem has a seperate handshake line, or Data Acknowledge (DTACK*) line, to the MC. When data is transfered to subsystems capable of asynchronous transfer the MC does not insert wait states into the bus cycle because it++ generates a generic DTACK* signal for them. In either case, if a valid DTACK* signal does not occur within about 25 microseconds, a bus error signal is generated. If a bus error occurs, the microprocessor executes an exeception routine which takes appropriate action according to the circumstances of the failure.

2.5.2 Data Buffer

The DB block diagram appears in Fig. 2-5. The design accomodates the interfaceprotocal needed when writing data records, read-ahead capability when reading data records, and autorecovery of tape recording errors. During normal read/write operations, the DB provides enough space for two 16 k-byte records tobe held or, if smaller records are used, more than two records can be held. When normal records (<= 16 k-bytes) are transmitted, retry and error correction is automatic.

**Only REV A boards contain +21 V supply circuitry. Subsequent revisions use EEPROMs which generate the +21 V internally.

++ The "*" indicates an active LOW signal throughout Section 2.5

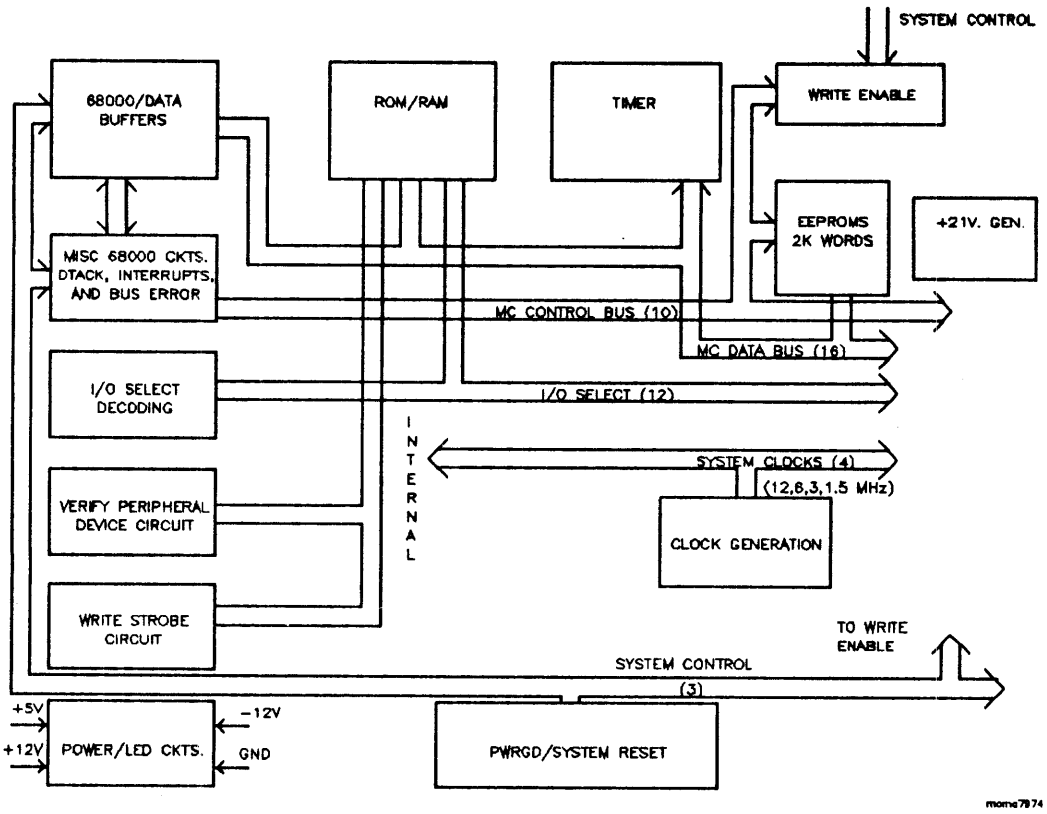


Figure 2-4 Master Controller Subsection

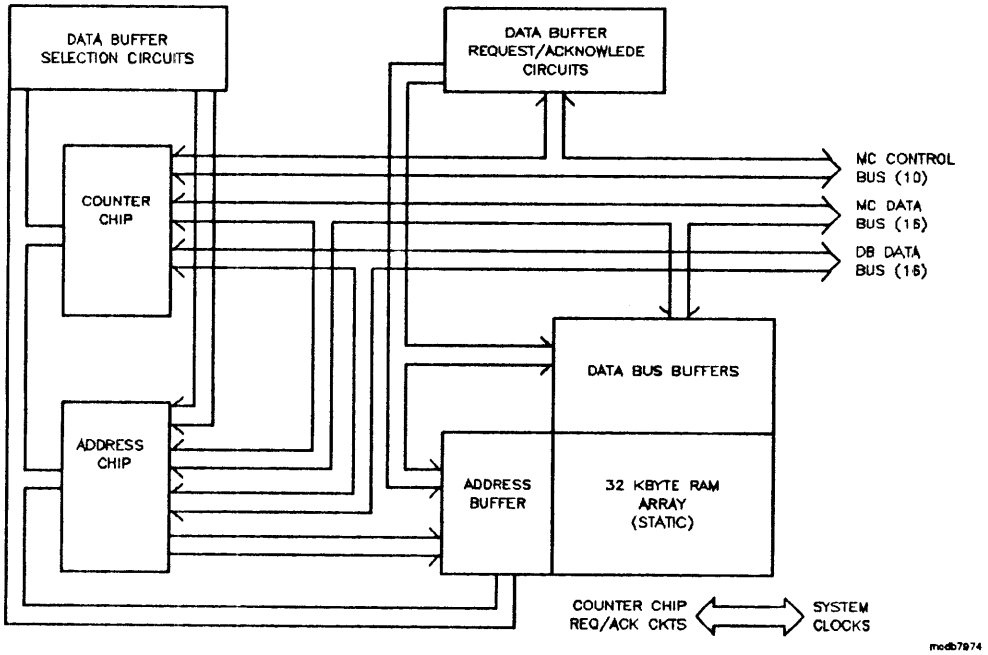


Figure 2-5 Data Buffer Subsection

2.5.3 Test Points and Connections

Figure 2-6 shows the approximate location of major subsections/components on the Master Controller PCA. The four segments of interest when servicing the HP 7974A are the MC Memory Circuits, Signal Test Points, Edge Connector Signals, and +21 V Supply.*

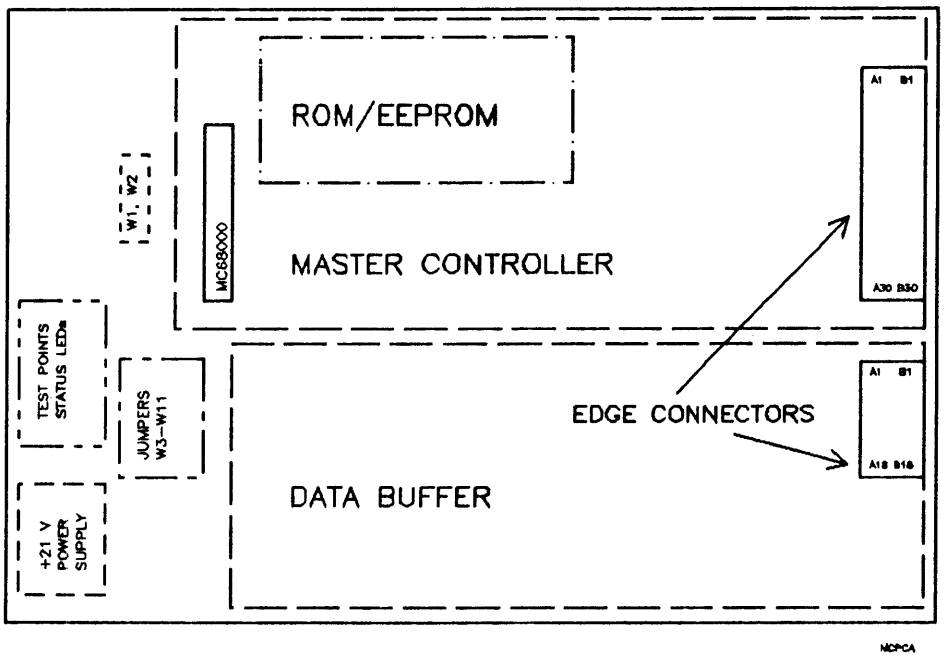


Figure 2-6 Master Controller Subassemblies

MC Memory Circuits

The memory for the MC currently consists of 128k bytes of ROM, 4k bytes of RAM, and 4k bytes of EEPROM. The ROM stores diagnostic firmware, the RAM stores miscellaneous operating values, and the EEPROM stores operating parameters and firmware update information. Operating parameters in the EEPROM include gain and address values that must be used to setup the subsystems after 'RESET' or power failure, reference values (eg., IRG length, allowed number of retries durring read, read/write gain values), software link addresses. About 3.5k bytesof EEPROM space is reserved for firmware update information. As updates become available, firmware patches for the ROM diagnostics will be stored in the EEPROM. (See Section VII for more information on firmware update procedures.)

The MC design makes it possible upgrade to larger firmware ROM devices as they become needed. Figure 2-7 illustrates the jumper locations W1-W11 as they appear on the Master Controller PCA. Make sure that the jumpers are correctly configured when installing new or replacement ROM/EPROM chips. The following paragraphs explain the ROM jumper configurations.

Jumpers W1 and W2 make it possible to use either ROM or EPROM devices, respectively, for diagnostic program storage. When ROM devices are used, W1 is installed and pin 1 of each ROM chip is tied to address line A15 from the microprocessor. When EPROM devices are used, W2 is installed and pin 1 of each EPROM chip is tied to Vcc.

*The +21 V Supply appears only on REV A boards.

CAUTION

Do not install both W1 and W2: You'll damage the MC68000 microprocessor.

Jumpers W3-W11 are used to accomodate either 8k x 8, 16k x 8, or 32k x 8 memory devices. By merely moving three jumpers at a time, the starting address locations of the RAM, Data Buffer, and EEPROM can be made to correspond to valid locations in the ROM devices used. Table 5-1 summarizes the necessary jumper groupings.

NOTE

The ROM/jumper configurations do not change the size of RAM or EEPROM chips used.

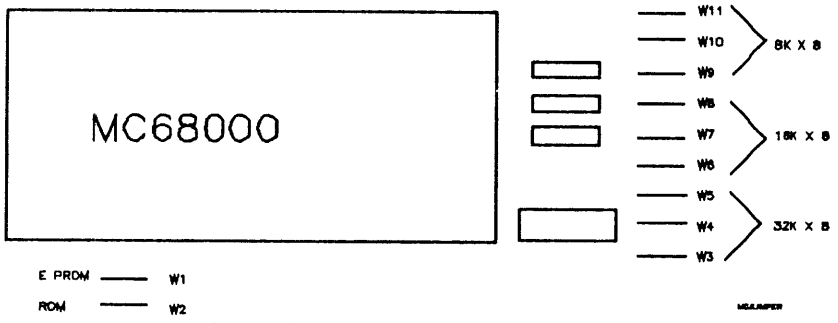


Figure 2-7 ROM Jumper Locations

Figure 2-8 Table of ROM Jumper Configurations

DEVICE	JUMPERS										
	W1	W2	W3	W4	W5	W6	W7	W8	W9	W10	W11
8k ROM	X								X	X	X
8k EPROM		X							X	X	X
16k ROM	X					X	X	X			
16k EPROM		X				X	X	X			
32k ROM	X		X	X	X						
32k EPROM		X	X	X	X						

Signal Test Points

As seen from Fig. 2-9, there are eight testpoints which correspond to eight status LEDs. During normal operation, all LEDs should be lit. These status lights give a gross indication that the corresponding power supply and process signals are available. However, they DO NOT indicate that the lines are within tolerance. (Use these points as a last resort when troubleshooting.)

CAUTION

The test points are not buffered from the signals. It is very easy to short them together and cause a hard failure.

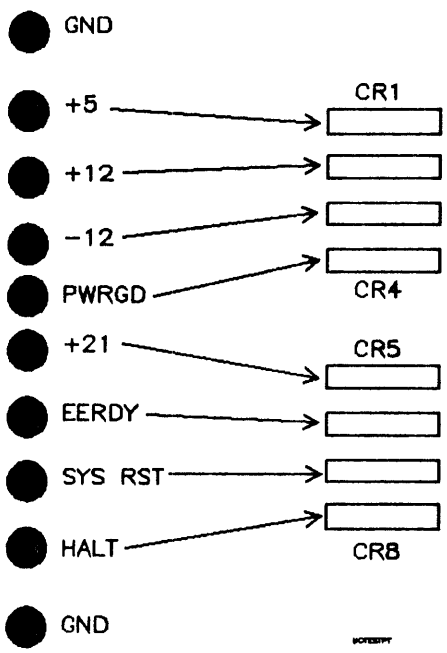


Figure 2-9 Signal Test Points

+5 V Indicates +5 V is available. Tolerance: +5.0 V ± 2%

+12 V Indicates +12 V is available. Tolerance: +12.0 V ± 3%

-12 V Indicates -12 V is available. Tolerance: -12.0 V ± 4%

PWRGD Indicates PWRGD signal from ICU power supply (i.e., PVAL) is high.

+21 V Indicates +21 V supply is within tolerance: 20 V < Supply < 22 V

EERDY Indicates EEPROMs are ready to be accessed.

SYS RST Indicates System Reset line state. The light toggles on and off when a software reset occurs (eg., during diagnostic testing).

HALT Indicates microprocessor is executing properly. This LED should always be on. If off, the system is hung and the MC board must be checked.

2.5.4 Edge Connector Signals

The edge connector signals and their purposes are divided into 8 functional groups, listed below.

1. Power - +12V, +5V, GND, -12V

2. System Clocks - 12MHZ, 6MHZ, 3MHZ, 1.5MHZ

3. System Control Lines
   PWRGD - Power Good
   SYS RES - System Reset
   GEN CLEAR - General Clear

4. MC Data Bus - D15..D0

5. MC Bus Control Lines
   R/W* - Read/Write; Vih=Read, Vil=Write
   WS* - Write strobe
   UDS* - Upper data strobe
   LDS* - Lower data strobe

   xxx DTACK* - Data Acknowledge from I/O systems
      a) DDD DTACK* - Data Detect and Deskew
      b) RF DTACK* - Read Formatter
      c) WF DTACK* - WRite Formatter
      d) IF DTACK* - HP-IB Interface

   xx INT* - INTERRUPTS
      a) IF INT* - HP-IB Interface
      b) SC INT* - Servo Controller

6. MC I/O Select Lines
   RS4, RS3, RS2, RS1 - Register Select
   DDD SEL* - Data Detect and Deskew
   RF SEL* - Read Formatter
   WF SEL* - Write Formatter
   IF SEL* - HP-IB Interface
   SC SEL* - Servo Controller
   READ BD SEL* - Read Board
   WRITE BD SEL* - Write Board
   FP SEL* - Front Panel (Buttons)

7. DB Data Bus - DB7..DB0, EOR (End-Of-Record bit), PAR (Parity bit)

8. DB Transfer Request Lines
   FRRQ* - Formatter Read Request
   IRRQ* - HP-IB Interface Read Request
   FWRQ* - Formater Write Request
   IWRQ* - HP-IB Interface Write Request

9. DB Read/Write Strobe Lines (acknowledges xxxRQ*)
   FRS* - Formatter Read
   FWS* - Formatter Write
   IRS* - HP-IB Interface Read
   IWS* - HP-IB Interface Write
   DBRS* - Data Board Read
   DBWS* - Data Board Write

[3] TAPE TRANSPORT

3.1 CONTROL/MOTHER BOARD

The Control/Mother board is mounted to a heatsink attached to the transport casting. Refering to the block diagram in Fig. 3-1, you can see that are a number of subassemblies that are responsible for the direct control of the HP 7974A drive mechanisms. Theseand other misc ellaneous functions of the Control/Mother board are discussed in the following subsections.

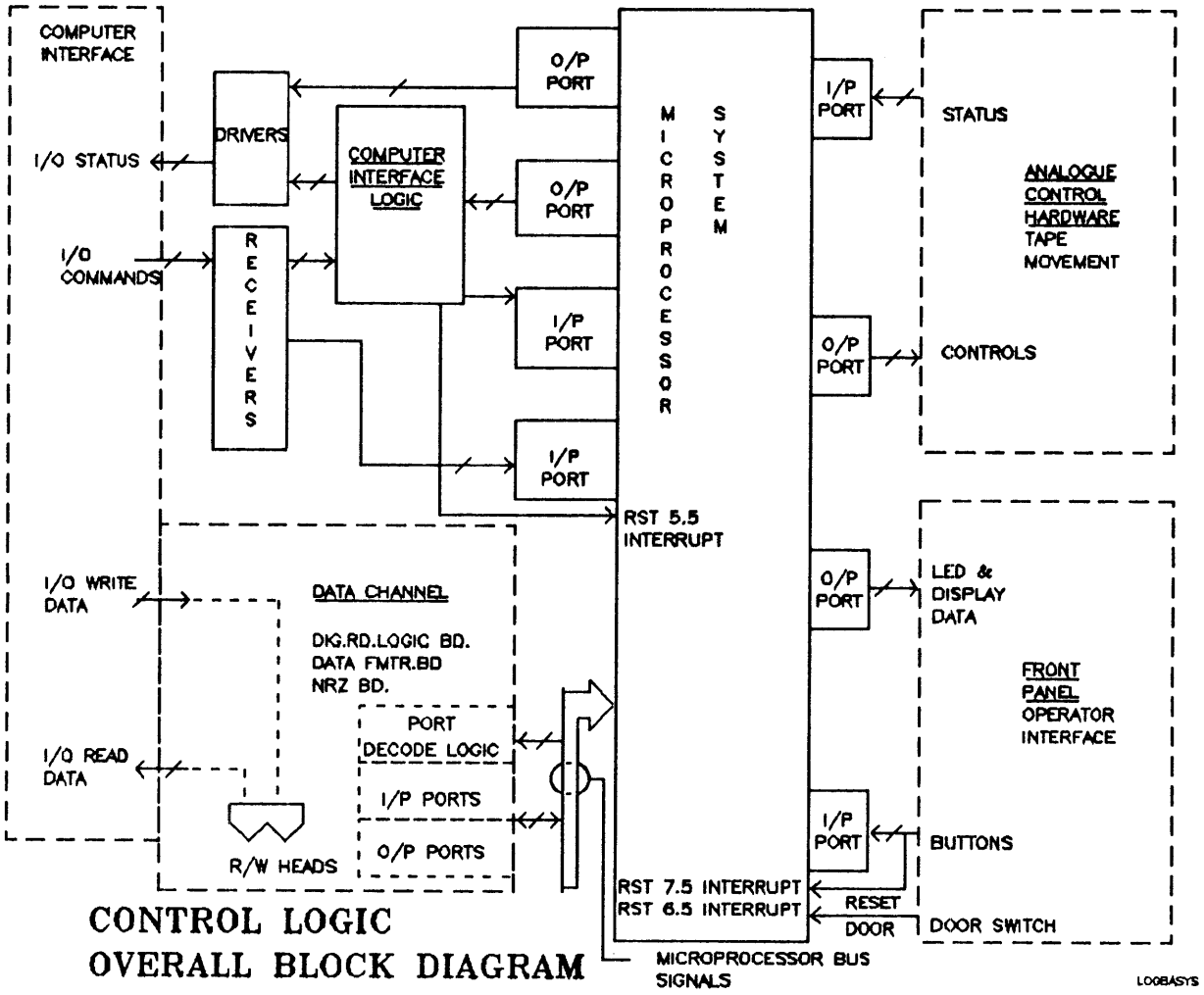


Figure 3-1 Control/Mother Board Block Diagram

3.1.1 Transport Control

Control servo circuit and data channel is an 8085-based microprocessor system. An overall block diagram of the control logic is given in Fig. 3-2. The control logic performs four basic functions:

1. Monitors the front panel inputs and responds by:
   - controlling analog servo circuits (tension tape , search to BOT, rewind tape, unload etc).
   - driving the front panel display with status and error messages.
   - settint the tape transport an-line to the I/O interface, rady to accept commands.
   - Setting the Tansport in the diagnostics mode (thus changing the purpose of the front panel controls).

2. Monitors I/O command signals (when online) and responds by:
   - controlling the servo circuits (to reposition the tape, if necessary, or ramp to speed ready for data transfer, rewind etc).
   - determining and generating the cecessary delays and control signals to the Digital Read Logic and Data/Formatter board, for writing the required data or control characters in the correct positon on the tape, and the correct data rate.
   - monitoring status signals from the Digital Read Logic, NRZI board, and Data/Formatter boards during Read, Read-after-Write or Erase operations, interpreting the signals and responding to the I/O interface with appropriate staus and error signals.
   - resetting, to front panel monitoring if the transport is taken offline remotely or, to diagnostics mode if such a command is received.

3. Implements diagnostic functions by controlling and monitoring the relevant ports.

4. Implements power-on and idle mod diagnostics by monitoring the relevant inputs (PWR FAIL, CON VAL, etc) and transferring to the front panel display.

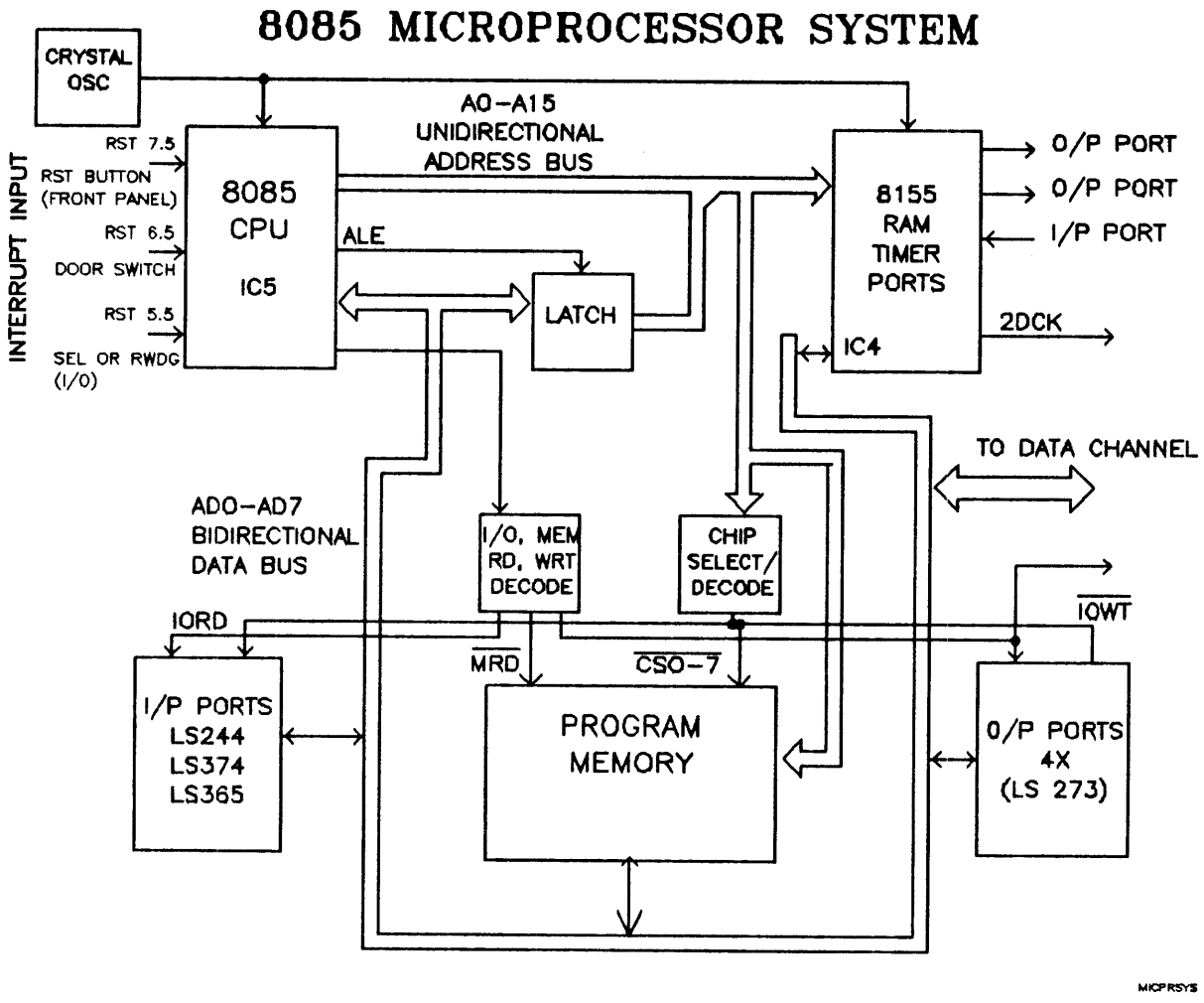


Figure 3-2 8085 Microprocessor System

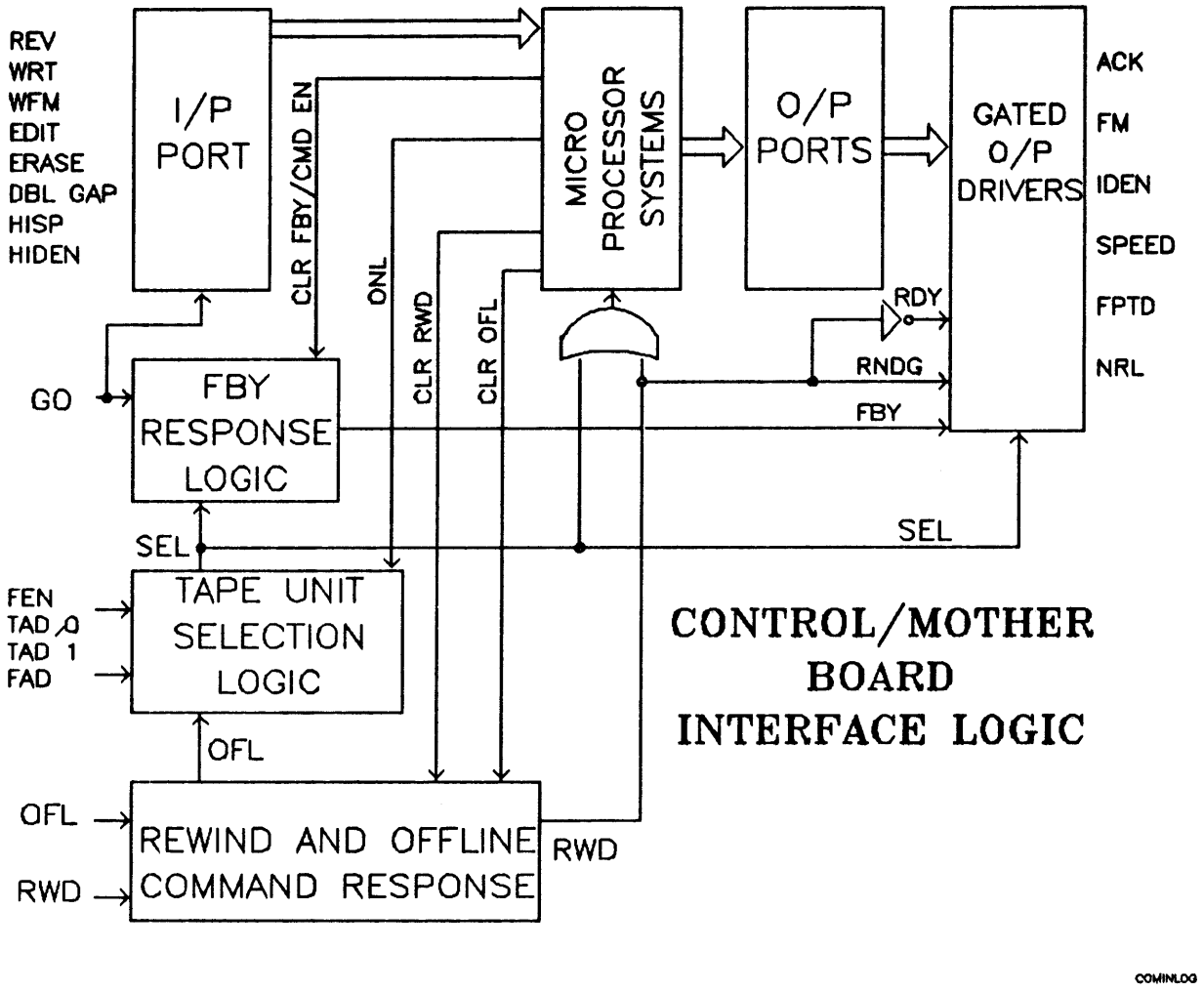


Figure 3-3 Control/Mother Board Interface Logic

3.1.2 Capstan Servo

The capstan servo electronics are located on the Control/Mother board. The speed demand, including the generation of start/stop ramps, is controlled by the 8085 microprocessor. The capstan servo is a standard velocity servo the speed of which is determined by the speed demand input and the feedback voltage from a tacho-generator, mechanically coupled to the capstan motor. Frequency compensation networks in the capstan servo amplifier ensure servo stability and provide the required servo response.

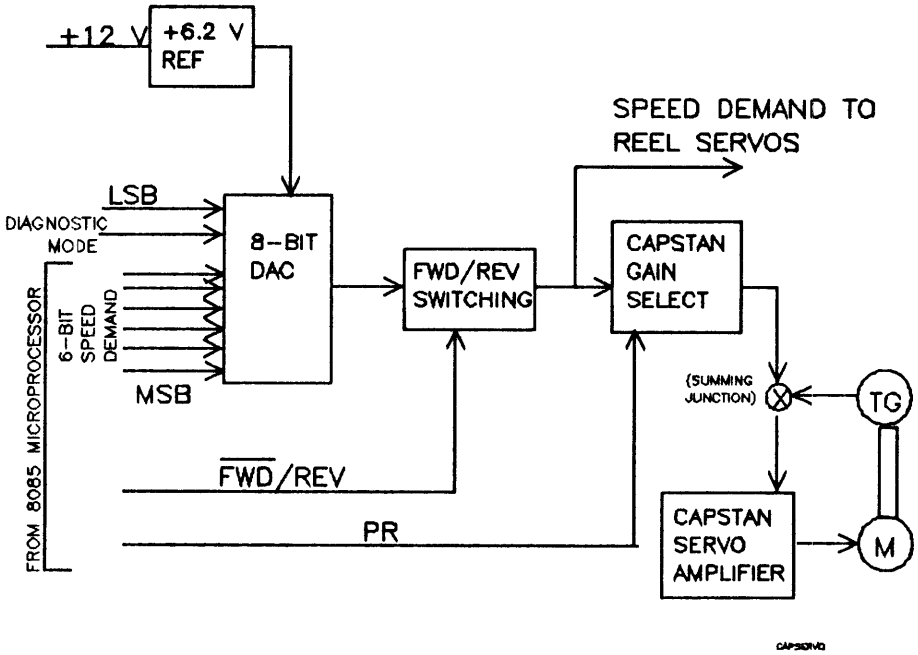


Figure 3-4 Capstan Servo Electronics Block Diagram

3.1.3 Reel Servo Systems

The servo systems are essentially identical for supply and take-up reels, for all modes except UNLOAD. Both reels are directly driven. A block diagram of the servo system is given as Fig. 3-5.

During normal RWD or REV operation a dc voltage propotional to the selected capstan speed is applied to the reel servo via an integrator, the time constant of which approximates the speed of response of the servo. This provides an aiming piont for the servo and ensures that the arm is biased to one side of the central position.

In the REWIND mode an output from the rewind speed optimising circuit is used to reduce the capstan servo dc speed demand signal when the reel is revolving too fast. For instance, the reel spins faster when comparatively little tape is wound onto the reel. If the speed is not reduced the arm limit detector would be activated, and completely stop all tape motion.

The UNLOAD mode affects the Supply and Take-up servos differently. The system drives the Supply servo in "reverse" until the end of the tape passes the BOT/EOT sensor. A dc level is then applied to the supply reel servo to control the reel rotation until all loose tape has been wound onto the supply reel. The Take-up servo maintains a constant speed until loss of tension is sensed. On loss of tension, the take-up reel is dynamically braked to a halt.

In addition, during the UNLOAD sequence, the upper tension arm is biased near its rest position and the lower tension arm is biased near the arm limit detector. This is done to minimize arm movement when tape tension is lost.

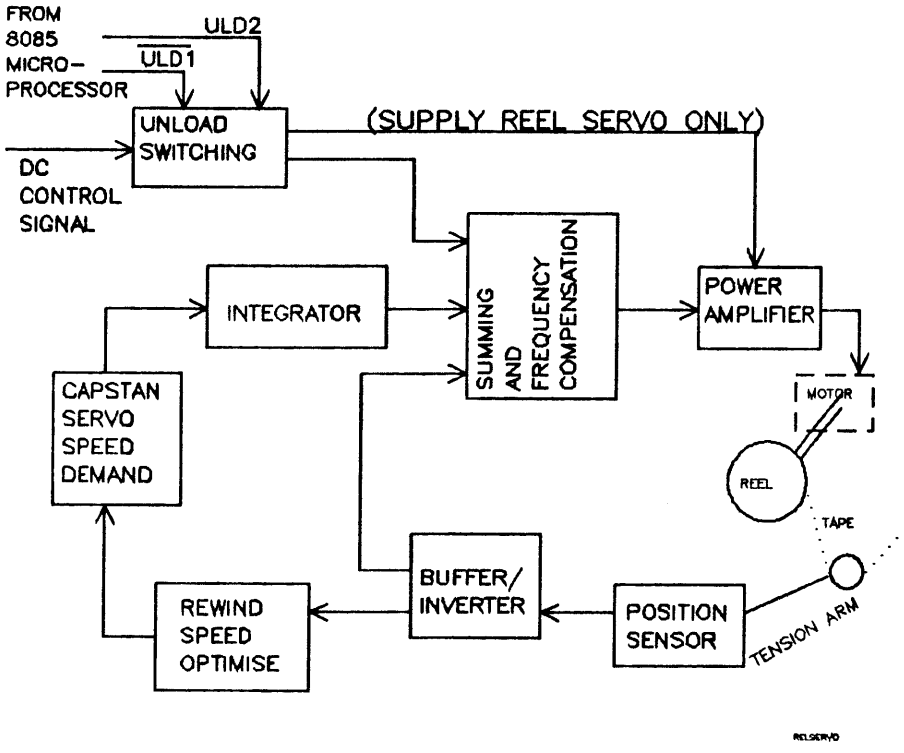


Figure 3-5 Reel Servo System Block Diagram

3.1.4 Arm Drive

The arm drive control circuit on the Control/Mother board enables rapid dynamic braking at top dead center, and controls speed when lowering the arms. The arm drive mechanism is shown in Fig. 3-6. The arm drive mechanism facilitates easy tape loading and is driven by a dc motor. Also, the upper arm is provided with viscous damping by means of an oil filled bearing housing. This damping improves tape start/stop and running performance. Overall, the mechanism performs the following functions:

(a) Lifts the arms, and maintains them in the upper position with power removed.

(b) Lowers the arms in a controlled manner, against the force of the tension arm.

(c) Provides, by means of the stop and up/down micro-swithces, status information to the microprocessor.

(d) Allows complete freedom for the tensioned arm, when the arms are lowered, enabling the arm to buffer the rapid capstan movements, from the relatively slow reel response.

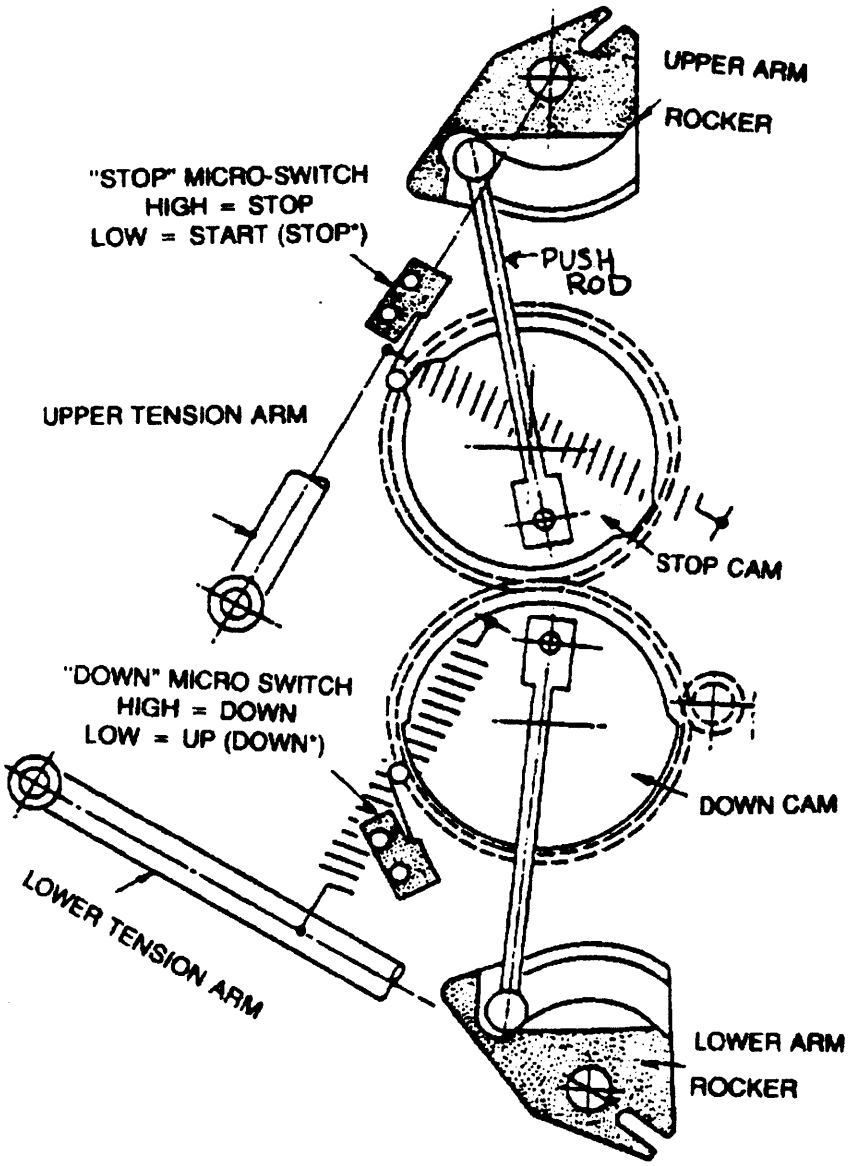


Figure 3-6 Arm Drive Mechanism

3.1.5 Write Ring Sensor

When a supply reel is used with a write enable ring fitted, the ring sensor switch is directly activated. This connects +12 V WRITE POWER to the Data/Formatter board and makes the write ring detect circuit, on the Control/Mother board, functional. During the tape load procedure, a signal is sent to the microprocessor to record that a write enable ring has been fitted, whereupon a command is given to energise the write ring solenoid. When the solenoid is energised, the write ring sensing mechanism is pulled clear of the ring to prevent contact during subsqent use. The solenoid normally remains energised until the tape is unloaded. A block diagram of the Write Ring Sensor circuit is given as Fig. 3-7.

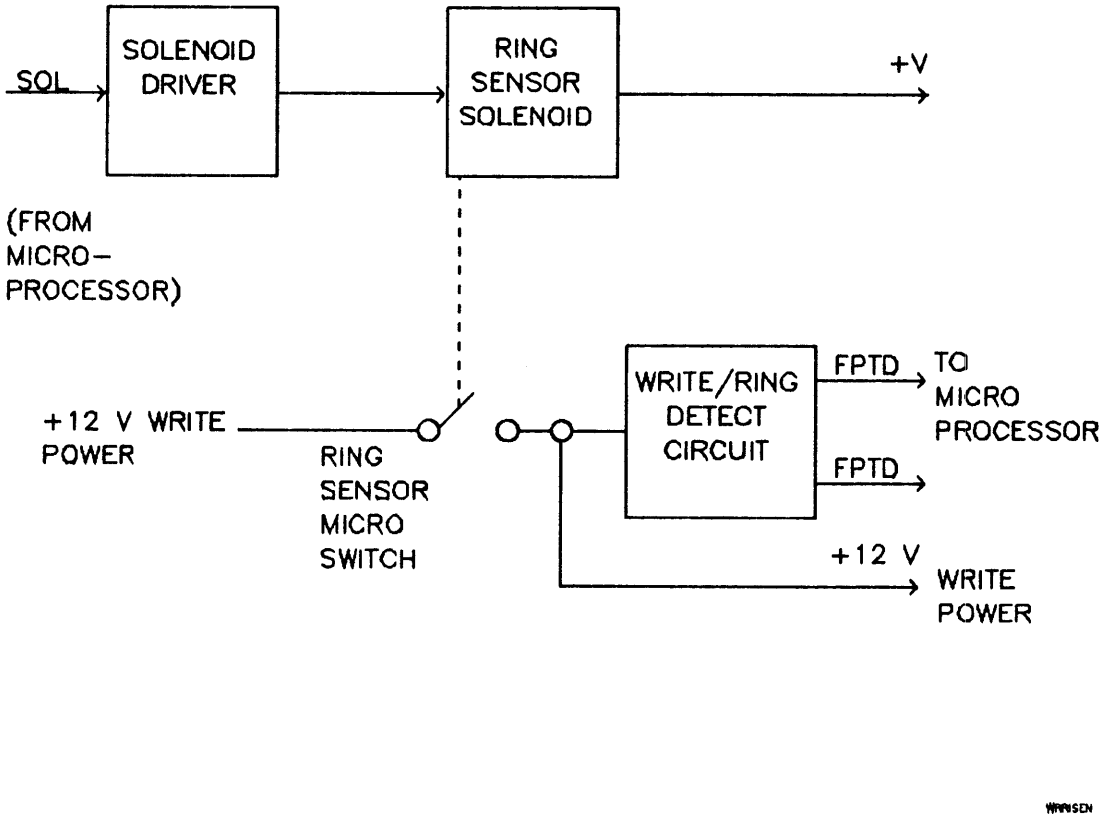


Figure 3-7 Write-enable Ring Sensor Block Diagram

3.1.6 Power Fail Protection

A block diagram of the power fail protection system is given in Fig. 3-8.

All dc voltage rails are monitored by the protection system, except the +24 V servo supply. If any of these voltages falls below a given minimum, or if the supplied power fails, the tape tension relay becomes de-energised. This disconnects the servo amplifier outputs via contacts of RL1 and provides dynamic braking to the capstan and reel motors. PW FAIL is sent to the microprocessor to enable the microprocessor control to be reset appropriately.

If all dc supplies are correct (except +24V) POWER LED on the Control board is illuminated. The tape tension relay is normally under microprocessor control, unless inhibited by the power fail protection circuit, or the arm drive interlock circuit. The +24 V servo supply is protected by fuse FS3.

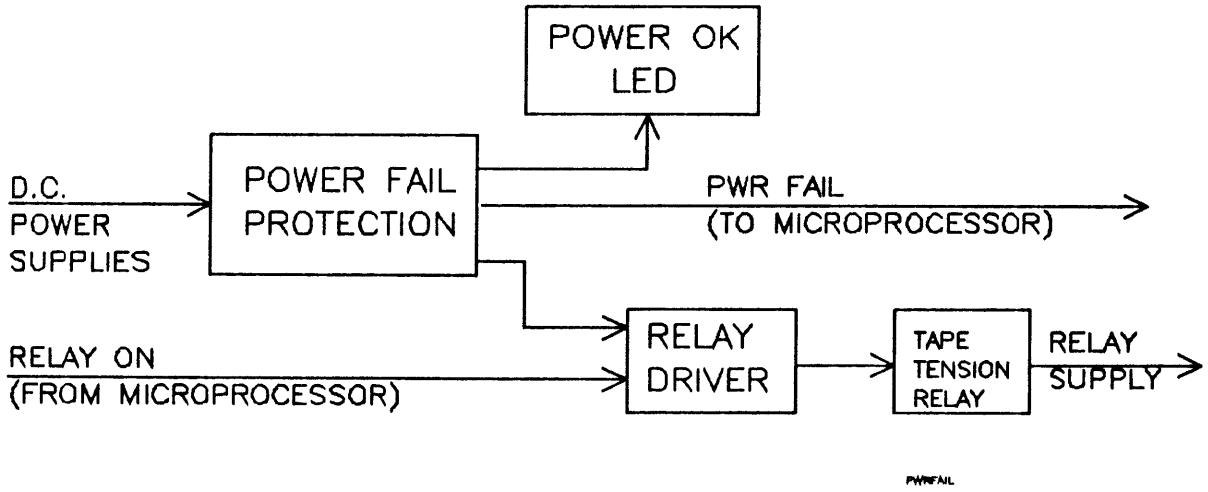


Figure 3-8 Power Fail Protection

3.1.7 Strobe Driver

A translucent disc, having a series of dots around its circumference, is attached to the capstan. When diagnostic Program 64 or 65 is selected, the microprocessor produces STROBE, a pulse train at a frequency which relates to the Transport speeed. An LED strobe 'torch' pulses at this frequency through the disc so that the dots appear stationary when the tape speed is correct.

3.1.8 Servo Supply Switching

The reel servos operate from +/- 14 Vdc supplies during FWD and REV modes. When 100 ips of REWIND modes are selected, PR from the microprocessor switches the reel servo power rails to +/- 24 Vdc, via TR33, 34,35, amd 36.

3.1.9 FET Switch Control

The FET swiching circuits ensure that the servo amplifier outputs are held at zero unless the relay contacts are closed. This prolongs the life of the relay contacts. A block diagram of the FET switching system is given as Fig. 3-9.

In all modes, except UNLOAD, enabling of the capstan and reel motor servo amplifiers is controlled by the RELAY ON signal from the processor. During UNLOAD, the microprocessor outputs ULD2 command and a constant current is provided to the supply reel motor which rotates the supply reel to take up the excess tape at the end of the UNLOAD sequence.

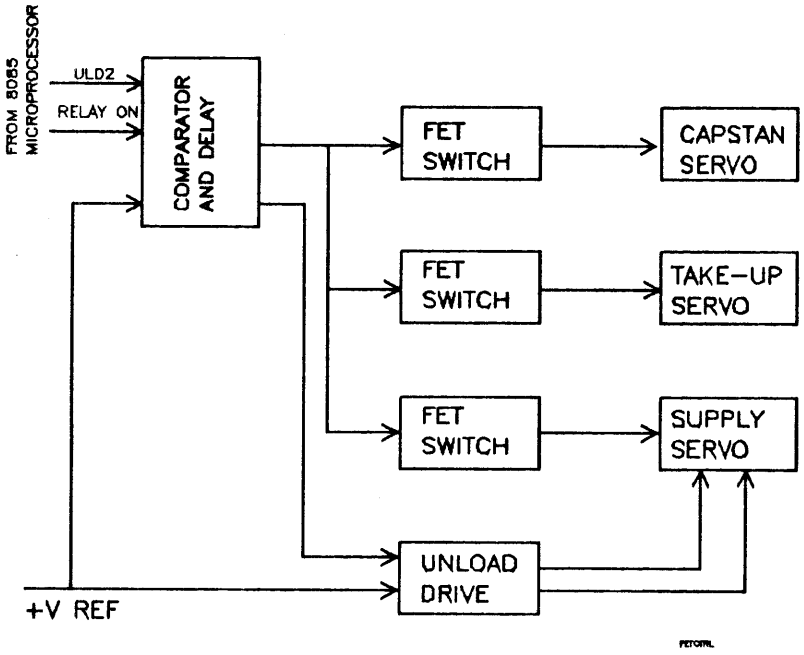


Figure 3-9 FET Switching System

3.2 DATA FORMATTER BOARD

The Data Formatter (D/F) board, in conjunction with the Digital Read Logic (DRL)board, handles all data transfer between the host system and the magnetic tape. The activities of the D/F are controlled by the 8085 microprocessor on the Control/Mother board. In the write mode, data from the host system is convertedto PE data with correct (industry compatible) format, before recording on magnetic tape. In read mode, recovered (read) data is amplified and passed to the host system via the Digital Read Logic (DRL) board, which performs a "deformatting" action. Odd parity is automatically generated and recorded on the designated parity channel.

A data prom on the D/F board contains the Identifcation and File mark formats associated with PE data and a series of pre-formatted data patterns used in diagnostic testing. These patterns are automattically generated when requested by the 8085 microprocessor.

Pre-formatted data is available to be used as an aid when tracing fault conditions either in an "offline" condition under operator control from the front panel, or remotely across the drive interface under host control. The data may be recorded on tape in the normal way or, if preferred, may be routed via the read multiplexers (IC63,64) to the Digital Read Logic (DRL) board, bypassing the analog read/write circuity, head and media. This is known as "loop-write-to-read mode. Data generation is independent of parity linking and external data lines. The five data patterns contained in the data proms simulate various data conditions. They are detailed as follows:

(a)	FIXED DATA	011001110 across the tape (C9H) - all characters identical down the tape.
(b)	PSUEDO RANDOM DATA (PRBS)	1111010110010000 down the tape, each track time displaced (by two bytes) from its physical neighbor.
(c)	PRBS DATA	Data as for (b) but with four byte drop outs in both channels 4 and 6.
(d)	PRBS DATA	Data as for (b) but with four byte drop outs in channel 6 only, together with all 1s bytes inserted into the postamble all 0s field on all channels.
(e)	PRBS DATA	Data as for (b) but with even parity bytes periodically inserted.

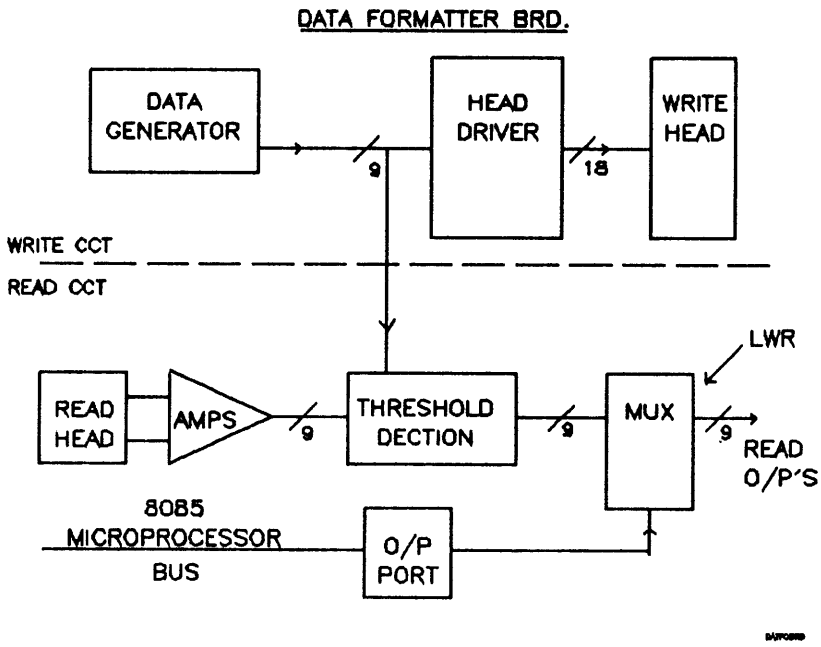


Figure 3-10 Data Formatter Block Diagram

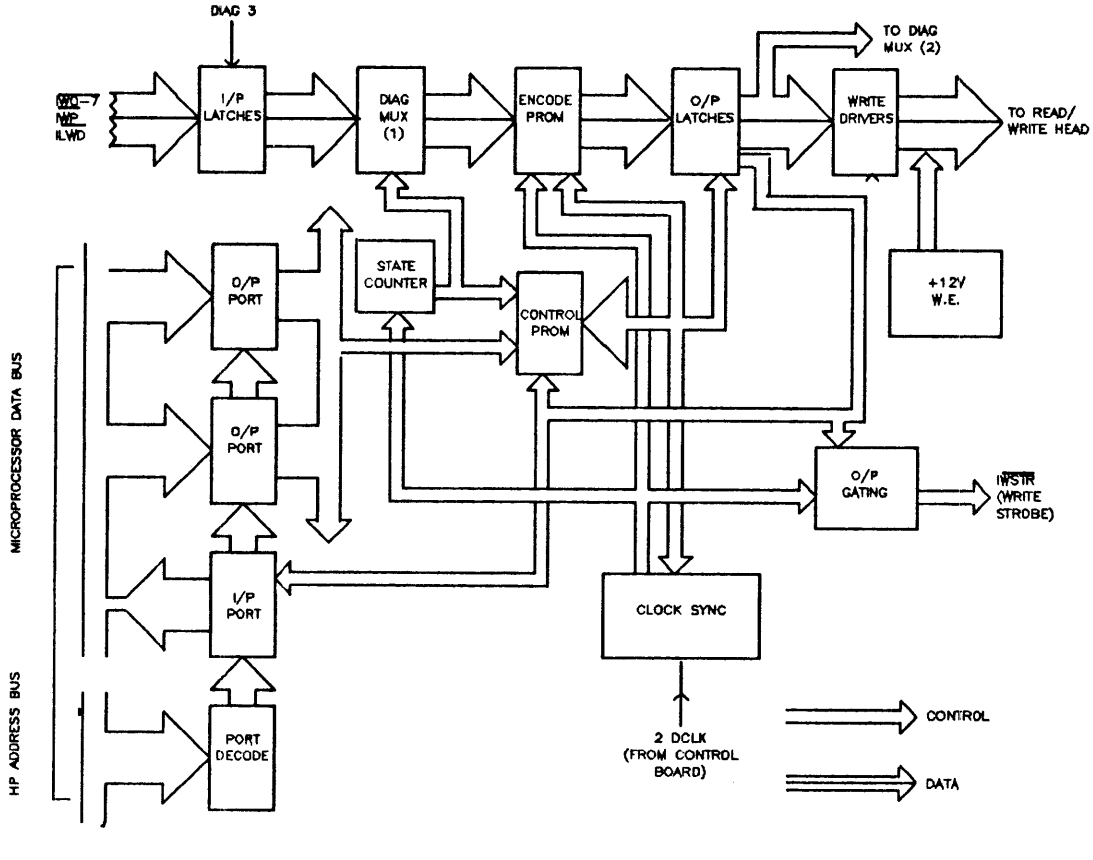


Figure 3-11 Write Logic Block Diagram

3.2.1 Formatting and Write Logic

Overal mode selection is under control of the 8085 microprocessor. It treats the D/F board as an extension of memory and communicates via the data bus, the one input port, and two output ports of the D/F. Ports are selected by a port decoder on the D/F. When the appropriate command is received from the 8085 microprocessor, the operation mode is then controlled by a finite state machine. The finite state machine consists of a control prom and an output latch. The operation is timed by the state counter which is synchronized by the master (2DCK) clock of the 8085 microprocessor.

On receiving the data encode command, the control prom initiates the preamble sequence through the encode proms. The data is "deglitched" in output latches and passsed to the write drives. Before completing the last preamble character,the first data byte is clocked into the input latches by the write strobe pulse (IWSTR).** On completing the preamble sequence, the control prom changes the encode prom address, terminates the preamble generation routine, and begins the data encode routine. The control prom then enters a HOLD STATE and waits for the transfer terminate command (ILWD) from the host. When ILWD is received, the control prom alters the encode prom address and begins the postamble. After completing the postamble sequence, the signal END is issued to the Control/Mother board via the input port and the encode proms. END also places the encode proms and the write drivers in the IRG state.

Upon instruction from the 8085 microprocessor, the control prom also select the proper encode prom address needed for writting the IDENtification burst and the File Mark sequences.

The IDEN burst is a 1 (continuous 1600 bpi signal) on the parity channel (P) only. All other other eight channels remain in the dc-erased IRG condition. The1600 bpi signal (1) is generated by toggling the appropriate command line on successive ENCL pulses. This continues as long as the ENCL command is asserted by the 8085 micropocessor and independent of the linking of the parity option, and of the external data lines.

The File mark consists of 40 all 1's in channels 2,6,7 and the remaining channels are dc-erased. the microprocessor. The operation is independent of the parity linking, and of the external data lines.

**The IWSTR is a write strobe line connected to the ICU Drive Interconnect board. It is used to indicate the transfor of one data bit to tape.

3.2.2 Read Circuit Operation

As previously stated, read circuit operation is also controlled by the Control/Mother board via the output ports. The read back signal from the read winding is amplified by a band limited amplifier, differentiated and converted to logic level signals which reflect the timing of the original recorded data. After this conversion, individual data/activity signal pairs from each channel are passed to the Digital Read Logic (DRL) board for further processing.

Analog Processing

Each read channel consists of differential amplifier (having switched gain) feeding an active differentiator. Since PE processing is used, the low frequency response of the chain is band limited to approximately 1kHz. Preamplifier gain switching is effected by the N-channel FET transistors within the feedback network. These are, in turn, controlled by an analog switch.

Digital Processing

In each channel, the differentiator drives a comparator pair, one of which gives a logic level output corresponding with the transitions through 0V of the differetianted signal (zero cross detection). The signal edges correspond with the peaks of the read back signal and, therefore, with the original write signal timing. Since noise causes spurious output during periods when no data is present (in the IRG), it is necessary to discriminate real data from noise. This is achieved by comparing the amplitude of the differentiated signal with a reference threshold or "clip" level (using the second comparator section). The comparator feeds an RC network which acts as an integrator. Data has to be present for approximately four data characters before the zero cross output (the real data) is allowed out of the Data/Formatter board (read activity detection).

The zero cross data for each channel is passed through the output multiplexers. Zero cross data for each channel is multiplexed with the corresponding encoded write data and output. This is necessary to support the loop-write-to-read mode. Then the data it is gated with its read active signal (RAC) and passed to the DRL.

3.2.3 Threshold Generation

Although each channel has switched gains, these are preset. A fixed gain/adjustable (common) threshold approach is used. The four reference levels associated with HIDEN/HISP, HIDEN/LOSP, LOWDEN/HISP and LOWDEN/LOWSP are set by potentiometers. The individual potentiometers are selected by the analog switch, according to mode, and controlled by amplifiers. Switching from a nominal threshold of 25% (read/write) to 12.5% (read only), the level switching is controlled by another analog switch and the write status (WSTS) line. When the assembly is disabled, is the analog switch deselected and the amplifier is pulled to +12V. The +THS line is then driven to +5.7 V and the activity comparators are inhibited to prevent data output.

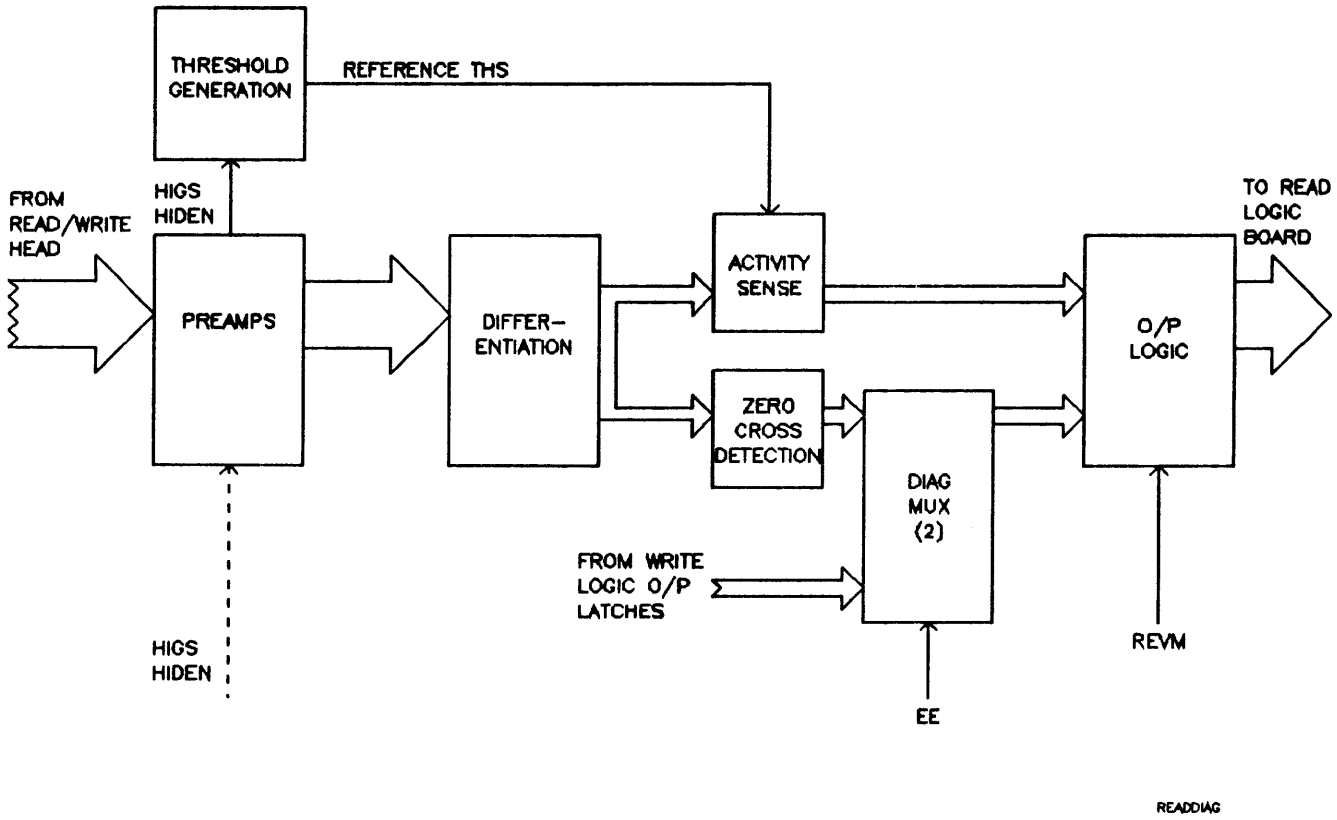


Figure 3-12 Read Circuitry Block Diagram

3.3 DIGITAL READ LOGIC BOARD

The Digital Read logic (DRL) board decodes and deskews PE read data received from the D/F board. The D/F produces two outputs for each of the nine data channels: read data (RDATA) and read active (RAC). All logic necessary for decoding data blocks, file marks, and identifier patterns, are contained on the DRL. It also contains logic to interface with the microprocessor control bus.

The DRL has two input and three output ports connected to the Control/Mother board. Input ports are controlled by memory write line IOWT; output ports by memory read line IORD.

NOTE

When the NRZI board (Option 800) is fitted, the DRL becomes inactive. REFER TO THE READ LOGIC CIRCUIT DIAGRAMS WHILE REVIEWING THIS SECTION.

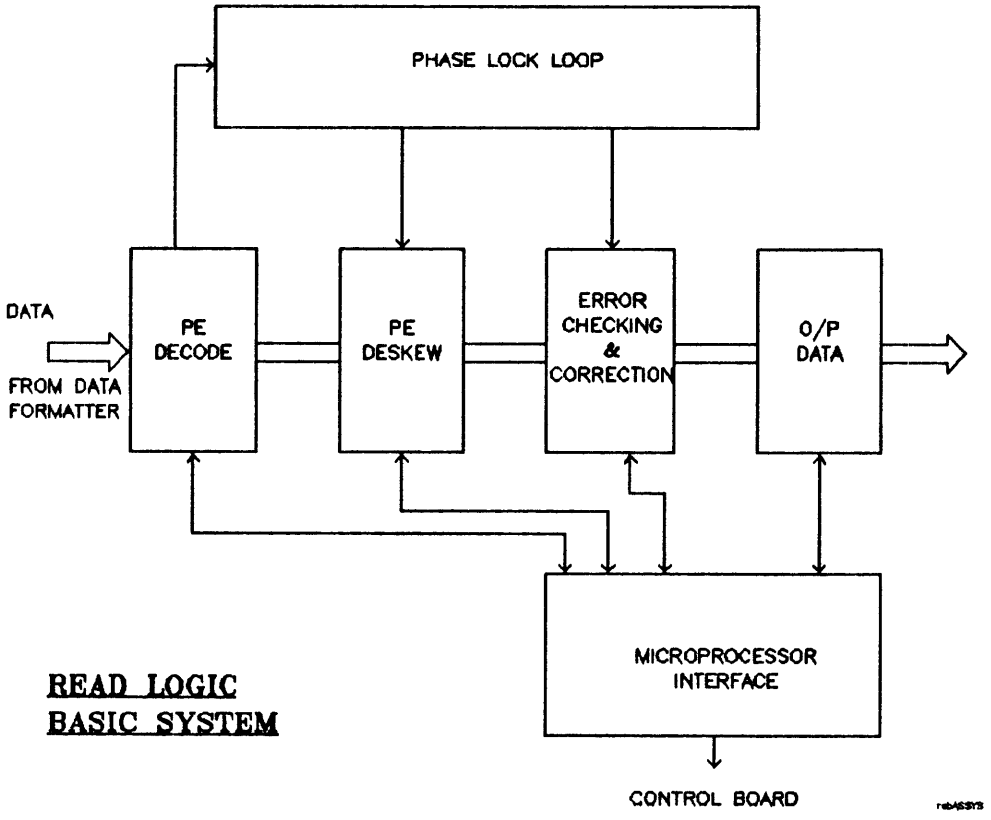


Figure 3-13 Simplified Read Logic Block Diagram

3.3.1 Block Dection

Signals RAC0-P, from the D/F board, address PROM A10. If any two, or more, of these signals are high (true), BLOCK is set true at A12 allowing clock at B13. Counter D12 counts up and, after 16 clock periods, clocks A12 to produce ENR and allow both elements of A11 to detect special conditions.

A11 pin 9 detects an identifier, which is defined as activity in Track P with all other tracks non-active.

A11 pin 5 detects a file mark, which is defined as activity in tracks 2,6, and 7 with tracks 1,3,4 dc-erased.

If neither of these special conditions exist, ENABLE is produced, allowing the data decoding logic.

3.3.2 Block Detection

All nine channels which decode read data (RDATA) are identical. The following description applies to Channel 0.

RDATA is retimed twice by TICK clock (24xdata rate) at C2 and edge detected during the second retiming by C#, producing a pulse for ever data and phase change in the data stream.

C1, the first 0 change bistable, synchonises the window generator, conter D4, whre the window is timed to open at a nominal 75% of data period (gating out any phase changes) and close at a nominal 125%. During the preamble data received from the D/F is arranged such that data changes are defined as logic 1 to logic 0, and phase changes as logic 0 to logic 1.

At the count of 8, D3 pin 9 is allowed and the puls from C3 pin 8 is clocked through the elements of C5 and returned to clear D4 to zero for the next data byte. First 1s latch C7 is set during the preamble all 1s byte. For subsequent data bytes D3 pulse is clocked into D9 to set the VALID signal which is used to initiate the memory write process. VALID is clocked off during the Channel SCAN period.

If a data change does not occur during the window open period, counter D4 overflows and clocks dad track bistable D6. DEAD inhibits further counter operation and VALID is forced by SUB clock (data rate).

When the DEAD status has been set for any channel , subsequent data in that track is ignored and DATA is forced low. The data, for a single dead track, can be reconstituted from the remaining tracks.

3.3.3 Data Deskewing

The nine data channels are deskewed by writing the data to a 128x1 RAM,E12, as it arrives, and clocking it out in 9-bit bytes.

Master scan counter D14 produces SCAN QA-QD which are used for write memory control, to produce SCAN 0-P, and for serialising the nine data channels.

When any channel detects a data change, VALID is set, and serialised via D10 and C13, to produce WRITE MODE. D12, D13, switch E12 addressing for read mode and write mode respectively, and allow the lower four address bits to be addressed by SCAN QA-QD, thus defining the position of data within the byte.

The position of the byte in the RAM is defined by length bits L1-L3. During RESET 1, at the start of every command, BEGIN is asserted and F16 outputs are tristated, presenting 1s to the A1-A3 inputs of full addre F15. At this time all B input to F15 are low thus F15 outputs are high, loading all 1s to all RAM E15 locations.

During BEGIN, WRITE MODE is forced true allowing all RAM locations to be written. When RESET 1 is cleared by the control system, BEGIN clears and F15 outputs go low and the first byte is directed to the low order address of the data RAM.

RAM E15 is addressed by counter D16 during the positive half-cycle of TOCK, (D16 is the next scan counter and is one count in advance of D14), and the length bits for the next scan are read, and latched into F16 at the end of the positive half-cycle. F15 adds on to the value of the length bits and the length advances cyclicly 0-7-0.

The length bits also address RAM F13, via E13, which is used to store the number of bits received in each byte. As the data bits are written to E12 the new length of the byte is written to F13 and, when all 9 bits of a byte are written to E12, F14 sets FULL true and initiates a read cycle from E12. Tranparent latch F12 is inhibited when WP occures ensuring that F14 address lines are steady during the time data is written to F13.

3.3.4 Read Control Logic

The read counters D17,E17, are clocked via READ CYCLE unless WRITE MODE is asserted (since write operations have priority). READ CYCLE is derived from FULL, one TICK clock period ofter F20 is set. Read counter outputs RSA-D drive the lower four address lines of RAM E12 and RSA-C address dead track serialiser B10. The count of 8 produces read data channel parity RDCP, the railing edge of which halts output clock (OC) which shifts data through the shift registers D19, B17.

When D17 overflows, read end of word (REOW) clock counter E17 which controls the higher, RSE-G, bits of RAM E12 address, E18 also clocks 1st word bistable F17 , for the first word only, to indicate that the first data byte has been clocked from E12 to the first of the output registers. For subsequent word REOW produces Drive Read Strove A (DRSA) which pulses read strobe monostable A20, and clock data into output register C17, A16.

3.3.5 Data Output

Data is clocked from deskew RAM E12 through a two-stage 9-bit shift register D19,B17 to output register C17, A16.

Deskwed serial data (DSD) is clocked into output register D19 and also into D20, odd vertical parity check, and B19, all zero data contents, by clock OC.

D20 is reset with pin 6 high and will toggle for every 1 in the data byte. A correct byte, for PE format, will end with D20 pin 6 low since all bytes must have odd totla parity. At the end of the bye A19 is clocked by the rrailing edge of RDCP and, if parity is incorrect, byte parity error (BPE) is produced.

B19 is reset with ALL true and any 1 in the data byte will cause ALL to go false.

If, when clocking data into the second shift register, B17, a BPE has been detected by D20, the data may be 'error corrected ' by C20,E2. BPE enables SDEAD (serialised dead track via C20 to E2 where the data from the dead track is inverted. Note that dead track serialiser B10 is controlled by the rad scan counter, whereas data nd valid serialisers are controlled by the write scan counter.

Dead track errors are detected by B19, B20, D20. If any one track is dead, STE (single track error) is set at B19. At the end of the data byte RDCP produces correctable errors (CERS) at D20 indicating that correction is being applied. Any further track in error will set multiple track eror (MTE) at B20, on of the conditions used by the Control board to produce hard error (HER).

Similarly, vertical parity error (VPER) will set B21, on data period after BPE has occured, unless CERS is true. VPER indicates that a byte with incorrect parity, but with all data channel active has been detected, and is used by the Control board to set HER.

The data byte is transferred to output register C17, A16, by the trailing edge of DRSA approximatly 1 microsec befor the rad strobe pulse is output. Controllers should clock data in with the trailing edge of read strobe.

B16 is used to detect a possible postamble. If an all 1s byte is followed by an all 0s byte, POSPOST is produced by B16, and clocked into E20 to set POST (Postamble detected).

POST enable E21 pin 13 and RDCP pulsed clock B20; if a non all-zero characters occur, ALLZ will be false and FPOS (false postambel) will be set, and the Control/Mother board will set HER.

POST< from E19, going true will route RDCP to counter D11 which, after 16 pulses, will overflow and reset E20. POST going low sets end of block (EOB) which inhibits further read processing by inhibiting READ CYCLE at F19. EOB is not reset until the Control/Mother board issues RESET 1 for the next read operation.

3.3.6 Phase Lock Loop

The phase lock loop comprises a phase-comparator (F5) and voltage-controlled oscillator (VCO) F2.

Loop input clock (LICO is selected by F10 which, when not processing data, is 'kept alive' by DCK, so that the loop is locked to the nominal frequency of data from tape. When processing a data block, LIC is switched to recovered clock, from data. Clock is normally recoverd from the master track2, but may be recovered from track 6 if track 2 drops out.

F2 outputs are at 48xdata rate, the correct output being selected by HISP.

F8 divides the clock by 2 to produce 24xclocks TICK and TOCK. TICK is further divided to form the feedback loop and data rate clock SUB.

3.4 NRZI BOARD (Option 800)

This section provides a very quick overview of the NRZI operation illustrated in Figure 3-14. A more detailed description of the functional blocks is contained in the following subsections. You should refer to the NRZI circuits diagrams when reviewing them.

The NRZI option consists of a single PCA that contains all the necessary electronics for write, read, and error detection functions. When installed, it is used in conjunction with the Digital Read Logic (DRL) boardto provide dual density(800/1600 bpi) capability. The NRZI board is positioned adjacent to the DRL board in the card cage. The read/write head assembly is then attached to a small connecting cable that joins both the NRZI and DRL boards.

All data transfer is controlled by the Control/Mother board 8085 microprocessor. Commands are sent to the microprocessor interface which contains the I/O ports. After decoding the appropriate port address, either the write or read control logic is activated.

During a write operation, data is first latched into the write data buffer. When the buffer is full, the data is gated across the data bus into the internal parity generator, CRCC generator, and write encoders. The write write drivers turn on when the write encoders begin their transfer and the write power control circuit becomes active.

During a read operation, the analog processing (detection) circuits send the data to the read input register. The data is then gated into the parity check, Character Assembly Time (CAT), and the block/check character logic for error detection. If no errors are detected, the data is then transferred to the read output register and eventually to the Control/Mother board.

The circuit diagram of the NRZI board is drawing No. D109538 and the component location diagram is No. D109530. The circuit diagram consists of five sheets:

1) write logic and write drivers
2) microprocessor interface and write control logic
3) digital read system and output logic
4) analog read circuits (tracks 4,6,0,1,2)
5) analog read circuits (tracks P,3,7,5) and threshold adjustment

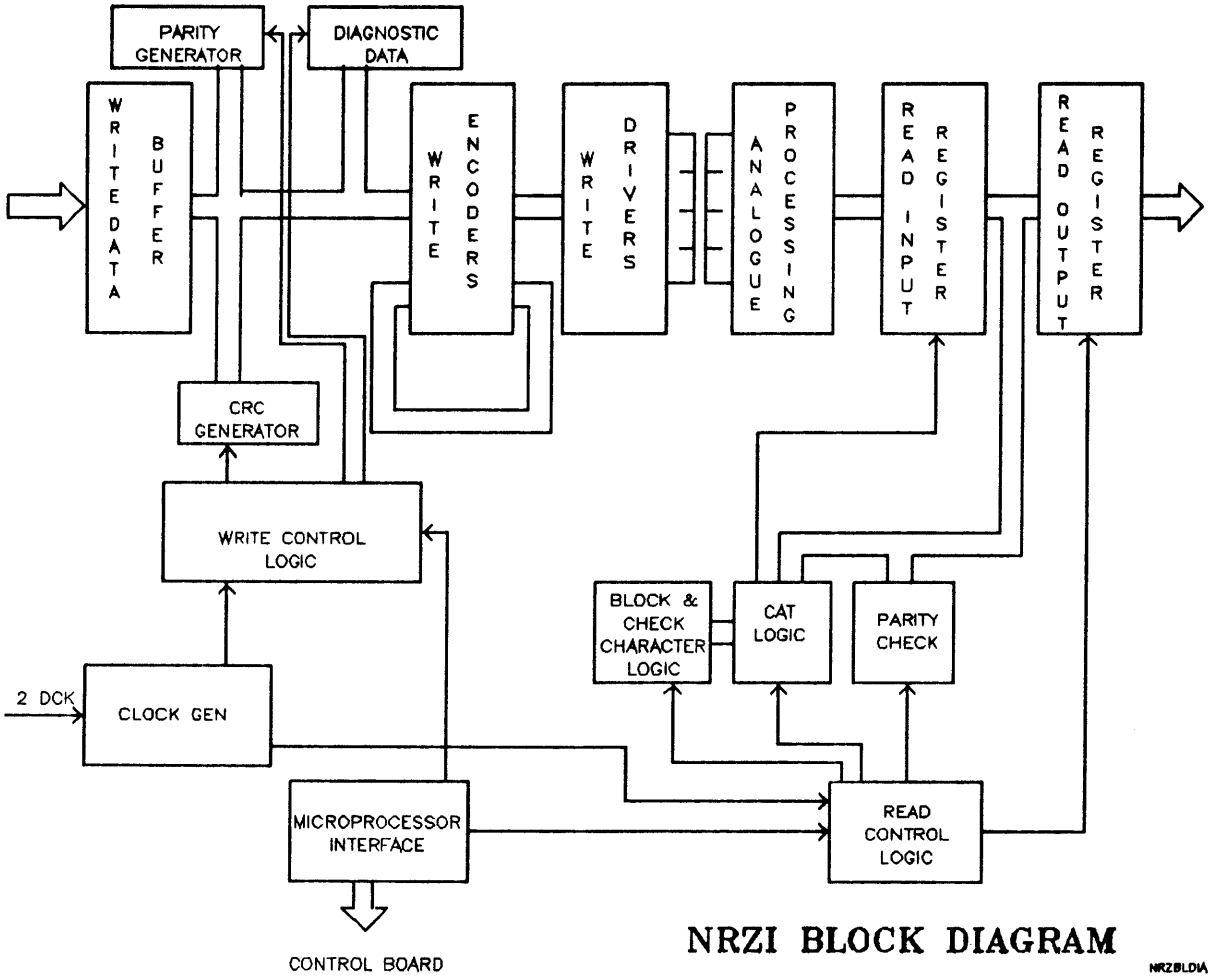


Figure 3-14 NRZI Block Diagram

3.4.1 Derivation of Clock Signals

The Control board issues a clock to the backplane which is used to synchronise all data to tape.

The clock is 2DCK which is a 2 x data rate for a 1600 bpi system. For ease of control program generation this clock is unchanged for a NRZI system and is divided by four to form a 800 bpi clock on the NRZI PCA. The division is performed by counter IC8 (2) and two phase related clock WC01 and WC02 are produced.

Additionally, the PCA contains a phase lock loop which is used to multiply the incoming 2DCK by 10 and form a 40 x data rate clock used for internal sychronisation. The phase lock loop consists of IC9, 10, 20, and 30, (3). The 40 x data rate clock is INTCK.

3.4.2 Processor Interface (Sheet 2)

IC46 decodes the microprocessor address bus and with gated IC15, addresses the four ports which communicate with the microprocessor.

IC4 and 14 are input ports to the processor. IC4 indicated error information, VPE (vertical parity error), CRCE (cyclic redundancy character error) and LRCE (longitudinal redundancy character error), information on the data being processed, Block, File Mark and Halt, a clock signal, used by the control and diagnostic programs to sense the presence of the PCA, and WTNG (write current flowing) signal which is utilised by the control program.

3.4.3 Write Data Logic (Sheet 1)

Data presented by the controller is clocked into the write data buffer IC6. This is an inverting element, since interface data is low true.

Data is clocked on the trailing edge of the write strobe pulse by the IC clock. If SW2 is set to external parity, this is clocked into IC7. During data transfers the output of IC6 is enabled onto the data bus, except during the generation of the check characters. This data is presented to the internal parity generator IC16 and to the CRC generator IC36, and via buffer IC56 to the JK bistables which are used to encode the data. The output of the encoding bistables are connected directly to the write drivers.

During the writing of the CRC IC6 is not enabled and the CRC information is enabled onto the bus via IC26. IC6 is disabled prior to the actual writing of the CRC to tape to ensure correct generation of the character.

For the LRCC, which ensures all tracks have even longitudinal parity, the outputs of the encoding bistables are fed to their input via IC93, thus any track containing an odd number of 1s will be left with its Q output at 1 and will toggle.

3.4.4 Write Control Logic (Sheet 2)

When the Transport is up to speed the control system will set the WCO line true to indicate the start of a write operation. This is clocked through the 2D type bistables of IC40 to enable the generation of IC clock. This is data rate clock and is used to generate the write strobe pulse and clock data into the input register.

Before the last write strobe is issued by the Transport, the controller sets the last word (LWD) line true and this is clocked into stat IC49 by IC clock to set the HALT signal true. This will, in turn, stop generation of IC clock at IC19 pin 4 and thus the generation of further write strobes.

The HALT signal is clocked into shift register IC69 by WCO1 and is clodked through this register to enable the generation of the check characters:

CRCC- Cyclic Redundachy Check Character

LRCC- Longitudinal Redundancy Check Character

Thee characters are positioned four and eight bytes from the last data character respectively.

The CRCC is generated in a single chip, IC36 (1), into which are clocked all data bytes and, to achieve a full rotation of the data, a final clock is applied with all inputs low.

Four byte periods after the HALT signal is set true, the signal CRC (cyclic redundancy enable) will set true at IC60 pin 11 and the CRCC will be enabled onto the data bus, via IC26. This is written to tape as for the data characters.

Three byte periods after CRD returns false, the signal EWARS will set true to enable the LRCC to be written to the tape. The LRCC is constructed by routing the Q outputs of the encoding bistables to their JK inputs, such that any data channel containing an odd number of changes will toggle and the total longitudinal parity will be even.

For certain data patterns which have an odd number of bytes it is possible for the CRCC to have all zero content.

3.4.5 Write File Mark

The tape file mark is a control character used in the tape system to separate data files.

The NRZI file mark consists of a single byte with tracks 3,6, and 7 written, followed eight periods later by an LRCC with the same tracks written. There is no CRCC for the NRZI file mark.

When the code for generation of a file mark is received from the Control board, the signals GFM and EDD which generate file mark and enable diagnostic data, are set true by IC25 (1). These condition the write logic for file mark generation and allow the diagnostic data prom onto the data bus. This prom contains the file mark information.

WC0 is set true for a write file mark, as for write data and, when the tape is up to speed, this is clocked throgh the two bistables of IC40 and allows one IC clock, which writes the file mark data character to tape. The next WC02 pulse sets IC40 pin 11 low and forces the HALT signal true, via gate IC50 pin 6. The check characters are then generated as for a normal data block, but generation of the CRE signal is inhibited at gate IC60 pin 13.

3.4.6 Diagnostic Write Commands

Diagnostic write commands are treated in the same manner as interface commands, except that all diagnostic data is stored in prom IC35 (1) and the DLWD signal (diagnostic last word) is used to indicate the end of date. This is gated to the input of the HALT bistable IC49.

3.4.7 Write Deskew

The deskew principle adopted is that the read head is mechanically diskewed to give parallel output data when reading a master skew tape. This is performed by minitoring TP1 (3) and adjusting for minimum scatter. The write head is then deskewed to achieve similar performance with read-after-write data and thus data written to the tape will be in parallel bytes.

The write deskew is performed by prom IC92 (2), counters IC82 and 72, and associated gating.

The deskew systems is arranged such that track 2, which is the centre track on the tape, is the fixed track, and it's clock pulse OC (output clock 2) is in the centre of the allowable deskew period. The deskew period consists of thirty-two counts of x40 clock (INTCK), and OC2 is arranged to occur after sixteen counts, thus allowing the other tracks to be dekewed to the read head in 2.5% increments. Each Transport is delivered with a deskew prom which will be matched to the head characteristics and should be installed in IC92 position, if the unit is field updated to NRZI.

3.4.8 Write Power Control

Signal WSTS from the control port is used to swtich the write power on via gate IC62 (2).

Write power may be inhibited by the local +5V power fail circuit D1, TR1, 2, or by the POWER FAIL detected by the Control board, backplane pin A10.

The write power control circuit is identical to that used on the Data Formatter board.

3.4.7 Read Analog Circuits

The analog read circuit amplifies the signals from the read head windings, converting the +VE and -VE peaks to +VE pulses, where the trailing edge corresponds to the peak of the readback signal. Since the read head drives the amplifiers of both the Data Formatter and NRZI board in parallel, a high input impedance is used to avoid loading effects.

The analog portion of the read circuits are shown on sheets 4 and 5, all nine circuits are identified and consist of an amplification stage, a buffer, a zero cross detector, and positive and negative threshold detectors. The outputs of the detectors are gated to form a positive-gong pulse for each change detected from the tape.

The pulses are uses to trigger JK bistables (on the left side of sheet 3); these bistables set for each 1 detected in the data. The first of the nine bistables to set will cause pin 10 of prom IC43 to go high and the CAT (character assembly time) bistable, IC34, to set true. This allows clock to the CAT logic fored by counters IC47,57, prom IC37 and shift register IC27. When counter IC57 overflows, the carry pulse is clocked into shift register IC27 which, in sequence, clocks the data into the output register IC13 and LRC checker IC23, clears the input registerk, clears the CAT logic and generates a read strobe.

The preamp consists of a fully differential configuration the gain of which is switched between high and low speed modes. Gain switching is effected by use of n- channel FETs chosen for low 'on' resistance. The first stage amplifier outputs feed a fully differential band-pass second stage, to produce a single-ended signal for used with the level detection comparators. Due to the high input impedance reqirement 'bifet' amplifiers are used having FET front ends. 1 Mohm resistors are used to control bias current effects. The preamp gain (differential in/single-ended out) is 50 dB at 50 ips, and 46 dB at 100 ips, and is flat between 100 Hz and 40 kHz.

The preamplifier feeds two comparator sections and an active differentiator stage (normal upper band edge 120 kHz). This feeds a comparator which generates edges corresponding with the transitions through 0 V of the derivative of the read head signal, and hence the read signal peaks (zero cross detection).

Reference threshold or 'clip' levels are set for high and low speeds, and are selected by the analog switch (IC60) under control of the HIGS line. The selected level is first amplified by 6 dB (RAW), or passed unmagnified (read mode), and then buffered by a non-inverting amplifier to produce +VE and -VE reference levels which are fultered by a simple RC state before passing to the level detection comparators.

The +VE and -VE peaks of the premamp signal are compared with the reference levels applied and must exceed these before the zero cross ginal can be processed in the final gating. Thus noise in the 'zero signal' condition (in long strings of rcorded 0 bits) is rejected. In the final logic the level comparator signals and the zero cross comparator signals are combined to form a composite pulse train of positive-going pulses, trailing edges of which contain the timing information corresponding with the original recorded data.

3.4.9 Digital Read Data

Output pulses from the analog read are used to set the JK bistables which form the read data input register. These bistables are shown on the left hand side of sheet 3. The clock pulses are routed via the OR gates which are alos used to clock the latches when pressing E-E data.

The first bistable to be set will cause the CAT Character Assembly Time) latch (IC34) to be set, via prom IC43. The CAT is the amount of the data cell which is allowed for the assembly of a complete character. Times used are:

RAW : 43%
READ : 50%
DIAG : 15%

The CAT is generated by counting-up counters IC47 and 57, until they carry. This is clocked into and through shift register IC27 to form the sequential clocks:

CLKOR : Clock Output Register - clocks data from the data input to data output registers and into LRCC check device IC23. Data output register is formed by IC13 and 44.

CLRIR : Clear Input Register - clears the input register to the all zero state ready for the next character.

CLRCAT : Clear CAT - clears the CAT bistable.

SOC : Send Output Character - fires the read strobe monstable IC28.

Each byte of data is checked for correct vertical parity (odd for 9-track systems) during a read operation. Parity is checked by prm IC43 and the result of the check is clocked into bistable IC12 by the CLKOR pulse. Should a data byte have incorrect parity the VPE flag (vertical parity error), will be set. This is one of the conditions used by the Control board to set HARD ERROR.

3.4.10 Block/Check Character Detection

The first time the CAT bistable sets in any data block it will cause the BLOCK bistable IC53 to set. This will allow clock to counters IC38 and IC39 which, with prom IC48, are used to separate data and control characters.

The second CAT sets the 2C bistable and the third CAT sets the 3C bistable.

Counters IC38 and 39 are loaded at the end of every CAT period by CLRIR. Approximately 2.5 data periods after procesing the last data byte, the signal CCCG (clock check character gate) will be isued, and the check character bistable IC21 will set to indicate that any further bytes transferred will be the check characters.

Unlike the data b ytes of the block, the check characters are not checked for vertical parity (inhibited at IC31 pin 5). However, bistable IC32 will toggle for every character in the data content, and the parity, but not content, of the CRCC will be checked. For an even number of data byted CRC parity is odd, and for an odd number of data bytes it is even. Should the CRC parity be incorrect the CRCE, (CRC Error), stat IC32 will set - this will set an interface HARD ERROR.

If, after six data periods, the CRC has not been detected (by IC21 pin 9), then it is assumed that the CRC has all zero content and AZC is issued to provide a read strobe and trigger the checking logic.

Some six data periods after the CRC is detected, the signal CCC is issued to check the validity of the LRC character.

When the counter chain overflows, some sixteen periods after the last character, CLRBLK (clear block) is issued and all stats are cleared ready for the next block.

3.5 POWER SUPPLIES

3.5.1 Transport Supply

The RFI filter and C7 to C10 across the rectifier bridge, are necessary to meet UK European mandates, (VDE class A and B, and FCC class A and B).

After rectification and smoothing, the unregulated outputs are fused and provide power to th reel servos (±14 V) at synchronous speed, and to the capstan and the reel servos (±24V) at high speed.

The +24 V pk unsmoothed, full-wave rectified, output supplies the load relay of the servo circuits to ensure fast switch-off.

-5V and +/- 12V supplies are derived from X3, C1 and C2 which provide current limiting and thermal protection.

D11,D12 provide protection to rail switching Darlington Power transistors in case of 24 V fuse failure.

D4,D5 and D6 protect the regulator devices against input failure, while D7,D8,D9 provide protection against reverse polarity of the output in case of inadvertent short circuit to other power rails.

0 V is completely isolated from chassis earth unless board connector 9 is connnected to the casting earth point. If the Transport is operated while isolated from chassis earth, 50 V potential MUST NOT BE EXCEEDED. This could cause breakdown of the head insulating washer.

3.5.2 +5 V Switched Mode Regulator

The +5 V regulator is a self-contained module whch has the functional appearance of a three terminal regulator, i.e. the only connections are Vin, Vout and ground. Internally the regulator consists of the power switch, low pass filter, control circuit overvoltage protection, overvoltage protection, overcurrent protection and under voltage protection.

The fundamental principle of operation is as follows. The input voltage is turned on and off by the power switch at a frequency of approximately 60 kHz. The mark/space ratio of the resulting rectangular waveform is adjusted by the controller to compensate for variations in the input voltage and ouput load, thus keeping the average voltage constant. The low pass filter (LPF) averages out the rectangular waveform to produce the output voltage.

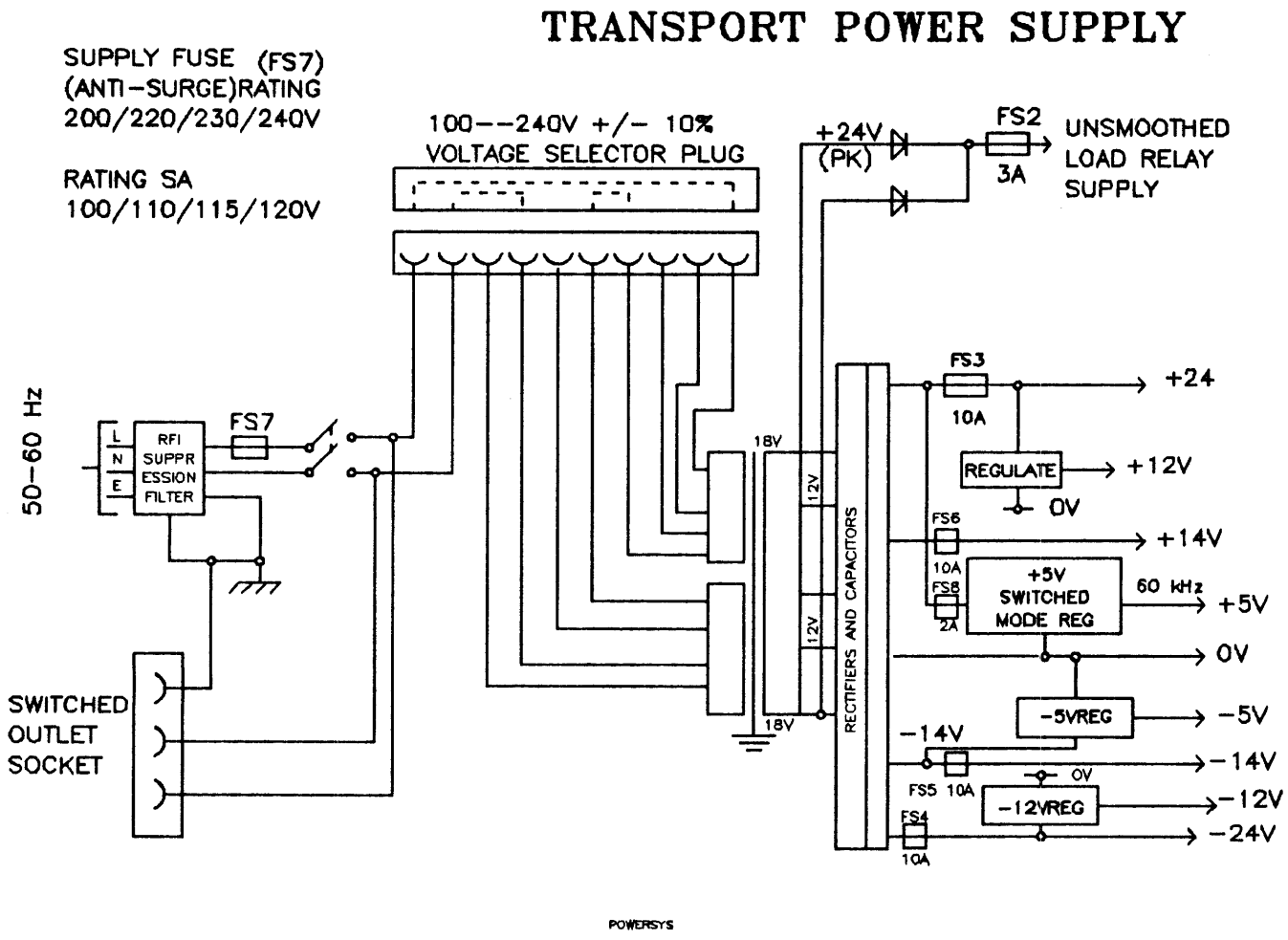


Figure 3-15 Transport Power Supply Block Diagram

This page intentionally left blank.

CONTENTS: SECTION VI

---FIGURES---

This page intentionally left blank.

REMOVAL AND REPLACEMENT

SECTION VI

[1] PREPARATION

Before proceeding with configuration and checkout procedures, the following steps must be completed to ensure your safety and allow easy access to all transport assemblies.

(a) Make sure that the work space is in a clean area which allows adequate space for opening and closing the cabinet doors, placing equipment and tools within easy reach, and moving back and forth. The cabinet clearance requirements are specified in Section II.

(b) Completely raise the front and rear leveler feet and move the unit into the work area.

CAUTION

Do not move the unit when the leveler feet are touching the ground. They could cause the unit to tip over and/or become damaged.

(c) Lower the rear leveler feet completely to the floor.

(d) Remove the pins on the front levelers and fully extend the legs before lowering the feet. This will stabilize the unit and prevent it from tipping over when the casting is open.

(e) Open the casting. A two-stage latch secures the drive casting to the cabinet. The latch is balanced so that the second stage catches upon the cabinet if the latch screw becomes loose enough to dislodge the first stage (eg. due to shipping vibration). Its unique design also makes it somewhat tricky to open:

1. Using a 5 mm hex key, turn the drive latch screw clockwise until you can feel the latch move freely.

2. Once the latch is free, turn the screw counterclockwise approximately 1/4 turn and, while holding the latch in that position, gently pull the casting out of the cabinet. The casting will only travel about 2-3 cm (1-1.5 in.).

3. Turn the latch clockwise a 1/4 turn, until the second stage clears the cabinet rail, and slowly swing the drive out of the cabinet.

WARNING

Do not swing the casting out rapidly: it is heavy. A 90° door stop has been added to the drive, but it is still necessary to keep your fingers clear of the hinge and inside casting edge when opening and closing the front of the unit.

(f) Inspect the transport for physical damage. Reseat all circuit boards and make sure all the cables are securely connected.

(g) Override the door interlock switch by pushing the door switch in and placing the metal arm, located near the rear of the door switch, between the rear switch washer and the casting. The metal arm will maintain the switch in the "door closed" position until the interlock is reset by pressing the door switch.

NOTE

Overriding the door interlock switch allows you to test electronic assemblies during tape movement/diagnostic operations. If the door interlock switch is not set, diagnostic programs used in the checkout procedures will not operate.

[2] TRANSPORT CASTING

2.1 FRONT PANEL ASSEMBLY

(a) Turn the main power off and disconnect the supply input lead.

(b) Remove the connections from the rear of the power switch and the grounding post. See Figure 2-1.

(c) Disconnect the switch PCA ribbon cable from the Data Formatter board.

(d) Disconnect the three spade plugs from the door interlock switch. See Figure 2-2.

(e) Release the front panel retaining screws and gently remove the assembly.

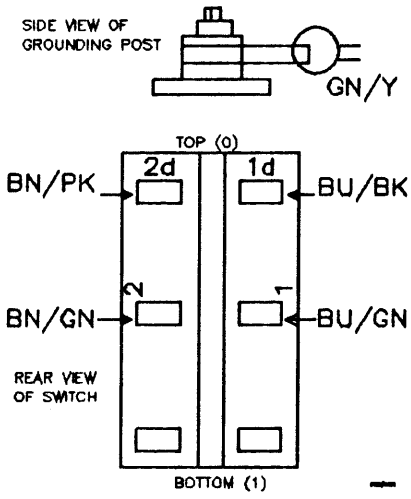


Figure 2-1 Power Switch Connections

When replacing the front panel assembly, reverse the removal procedure. Ensure that all wiring is correct and the wires cannot become trapped when the casting is shut.

2.1.1 Switch PCA

The switch PCA is mounted on five posts attached to the front panel plate. When re-mounting the board, be sure to replace all nuts, spring washers, and red fiber washers in the proper order. Ensure that all buttons and LEDs fit properly in the panel plate. If the PCA is not positioned correctly, the buttons have a tendency to stick.

CAUTION

The switch PCA is very susceptible to electrostatic discharge.

Replace all red fiber washers between the mounting posts and PCA to prevent grounding it to the casting.

2.1.2 ON/OFF Switch

The switch is held in place four plastic retaining clips. **Do not force the switch out of or into the panel: the clips may break.** To remove the switch, gently squeeze the clips and ease it out of the panel. Upon replacement, make sure the switch is connected and oriented correctly. See Figure 2-1.

2.2 DOOR ASSEMBLIES

2.2.1 Dustcover Door

(a) Remove the front panel assembly. (Section 2.1)

(b) Disconnect the earth bonding wire from the door.

(c) Release the screw securing the door stay to the transport casting. Retain the spring washer and spacers.

(d) Release the door hinge blocks and draw the door forward. Make sure that the upper hinge block does not fall as you remove the door.

When replacing the door assembly, reverse the removal procedure. You may need to adjust the door catch plate (Section VII).

2.2.2 Drive Interlock Switch

(a) Disconnect the three wires from the interlock micro-switch. Refer to Figure 2-2.

(b) Release the micro-switch retaining screws and remove the switch from the rear of the casting.

When replacing the micro-switch, reverse the removal procedure.

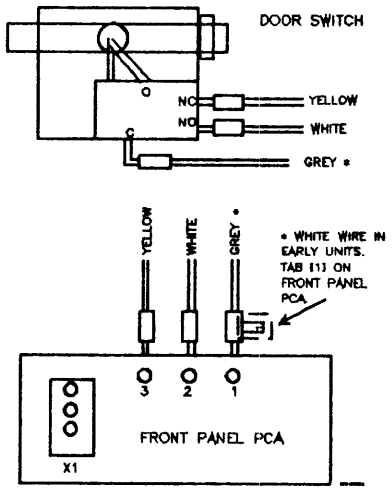


Figure 2-2 Door Interlock Switch Connections

2.3 CASTING COVER PLATE

(a) Open the door and remove the head covers.

(b) Remove the supply reel.

(c) Unfasten the three hub fixing screws and remove the take-up reel. Replace the screws and lock washers.

(d) Release the plate fasteners and **CAREFULLY** remove the cover plate.

CAUTION

Make sure the tension arms are in the load position when the plate is removed/replaced; otherwise the arm slot can catch upon the arm rollers and possibly damage them.

2.4 HUB ASSEMBLIES

2.4.1 Ejector Hub (Supply)

(a) Remove the front cover plate, Section 2.3.

(b) Release the hub ejector retaining screw (Figure 2-3) until the ejector button springs forward. Retain the ejector spring. Release the retaining screw a further five turns.

(c) Release the two clamp screws at the rear of the hub so that the clamp bar clears the step in the motor shaft. Rotate the hub assembly until the clamp falls clear of the step. Withdraw the hub assembly from the motor shaft.

When replacing the ejector hub, reverse the removal procedure. BEFORE THE HUB IS REFITTED AND THE CLAMP SCREWS HAVE BEEN TIGHTENED, insert the ejector button retaining screw and check that it enters the hole in the motor shaft. Verify that is seated properly by performing the the hub height check and adjustments.

2.4.2 Fixed Take-up Hub

(a) Remove the front cover plate, Section 2.3.

(b) Release the hub cover retaining fixings located on the front of the hub and remove the hub cover.

(c) Loosen the three screws clamping the motor shaft and carefully withdraw the hub assembly (Fig. 2-3).

When replacing the fixed hub assembly, reverse the removal procedure. After replacing the hub, check the take-up reel to see that is seated against platform when the three screws are tightened. If not seated properly, adjust the screws. Verify that it is seated properly by performing the hub height checks and adjustments.

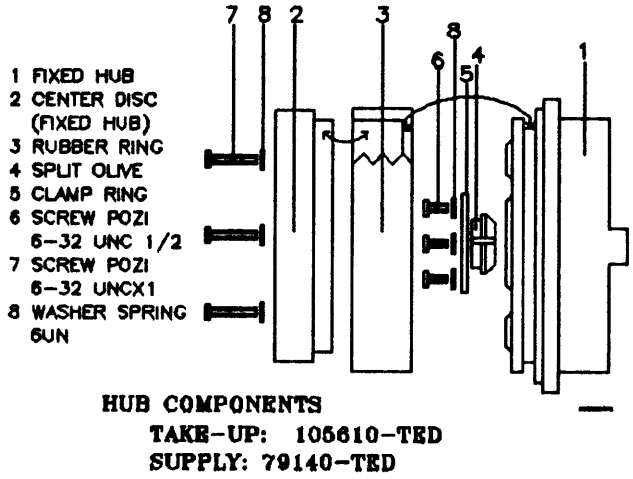


Figure 2-3 Hub Components

2.5 WRITE-ENABLE RING SENSOR

To remove the write-enable ringe sensor, unsolder the wires on the pillars and the cam micro-switch, remove the sensor retaining screws, and withdraw the assembly. When replacing the sensor, make sure that it is wired according to Fig. 2-4 and that the switch moves without rubbing against the supply reel motor.

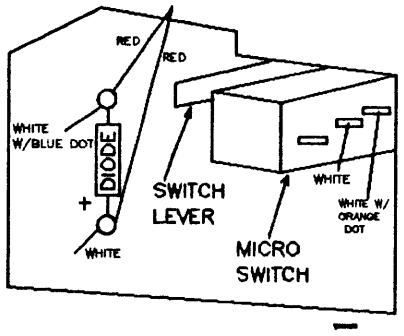


Figure 2-4 Write-enable Ring Sensor Connections

2.6 REEL MOTOR

(a) Remove the front cover plate and the hub on the defective motor.

(b) Disconnect the SKS (supply) or SKU (take-up) plug from the Control/Mother board. See Fig. 3-6.

(c) While supporting the motor from the rear, release the motor retaining screws from the front of the casting. Withdraw the motor from the casting.

When replacing a reel motor, reverse the removal procedure.

NOTE

On early units, the upper reel motor must be as close to the top of the casting as possible when the screws are tightened. This necessary to keep the write-enable ring sensor from striking the motor body.

Replacement motors are designed to be used for either the upper or lower reel. The adaptor plug supplied with the replacement units must be modified to match either the SKS or SKU connector.

2.6.1 Capstan and Reel Motor Brushes

If the motor brushes are suspected, take care not to damage the plastic threaded retainers when removing the brushes. Replace them if the length is less than 5 mm (0.2 in.).

2.7 ROLLER ASSEMBLIES

2.7.1 Bridge Rollers

CAUTION

The roller assembly is shimmed to the bridge casting during manufacture. Do not separate the assembly from the casting.

(a) Remove the front cover plate.

(b) Open the casting and remove the bridge roller retaining screws. If the lower assembly is to be removed, use a right angle posi-drive to reach the retaining screws behind the +5V regulator PCA.

(c) Release the bridge roller assembly from the rear of the casting and remove in a twisting motion.

(d) When replacing the assembly, reverse the removal procedure.

2.7.2 Roller Guides

When removing either assembly, support the roller pillar, release the retaining screws on the rear of the assembly, and discard the circular "cap" mounting plate. Because the "cap" was installed for shipping purposes only, it is not needed when a replacement assembly is installed.

If the upper roller guide is replaced, perform the arm roller angle check and adjustment.

2.8 CAPSTAN ASSEMBLY

2.8.1 Capstan

(a) Remove the front cover plate, Section 2.3.

(b) Grip the outside of the strobe disc with thumb and forefinger and, using a hex key, remove the capstan retaining screw.

(c) Pull the capstan off of the motor shaft. **Do not grip the capstan drive flange. It is a delicate component and will distort.**

After replacing the capstan, perform the capstan offset adjustment of Section VII.

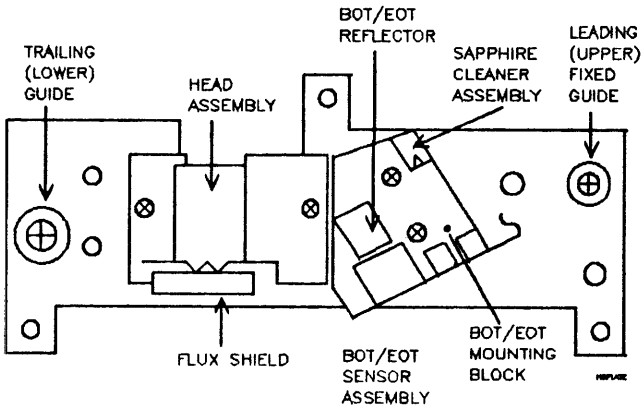
2.8.2 Capstan Motor

(a) Disconnect the PLT and SKY plugs from the Control/Mother board. See Fig. 3-6.

(b) Support the capstan motor from the rear of the casting and remove the capstan retaining screws, washers and shims from the front of the casting.

(c) When replacing the capstan motor, reconnect the plugs PLY and SKT and ensure that the motor orientation is correct (i.e. brushes in vertical axis; cables routed inwards).

2.9 HEAD PLATE ASSEMBLY



HEAD PLATE ASSEMBLY
109736-TED

Figure 2-5 Head Plate Assembly

2.9.1 Head Plate

This assembly is supplied for replacement as ready deskewed.

(a) Remove the head covers.

(b) Disconnect the write and read head connectors from the transport card cage.

(c) Disconnect SKL from the Control/Mother board (See Fig. 3-6) and remove it from the cable wrap. Pass SKL underneath the arm drive assembly, cut the tie wrap holding it to the casting (near the head plate), and let the wires hang next to the transport.

(d) Release the assembly retaining screws on the rear of the casting and remove the head plate assembly from the rear. If an NRZI dseskew PROM is attached to the head plate assembly, ensure it remains attached to the particular head plate assembly.

When replacing a head plate assembly, reverse the removal procedure and replace all tie wraps. Also, tighten the retaining screws sequentially by increments check, run diagnostic program 101 to verify its overall operation.

2.9.2 Tape Cleaner

(a) Remove the head covers.

(b) Remove the tape cleaner from the EOT/BOT assembly.

CAUTION

The edges of the blade are very sharp. Handle them with great care.

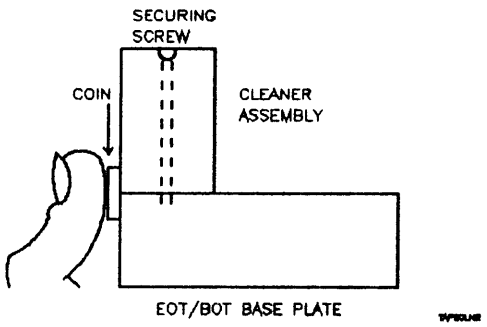


Figure 2-6 Aligning the Tape Cleaner

When replacing the tape cleaner fit the locating dowel in the positioning hole and press a coin to the side of the tape cleaner/EOT/BOT assembly. Tighten the securing screw. This ensures correct alignment of the cleaner assembly. Refer to Figure 2-6. On later models, the sapphire protrudes into the EOT/BOT base plate and, with the locating dowel, provides the correct alignment.

2.9.3 BOT/EOT Sensor

(a) Disconnect SKL from the Control/Mother board (See Fig. 3-6) and remove it from the cable wrap. Pass SKL underneath the arm drive assembly, cut the tie wrap holding it to the casting (near the head plate), and let the wires hang next to the transport.

(b) Remove the head covers and the front cover plate.

(c) Unfasten the sensor from the head plate assembly and remove sensor.

When replacing the sensor, reverse the removal procedure. Make sure that tape can clear the reflector block before completely tightening the screws. After replacing the assembly, perform the checks and adjustments of Section VII.

2.9.4 Read/Write and Erase Head

This procedure removes the head, independent of the complete head assembly.

(a) Remove the head covers.

(b) Disconnect the write and read head connectors and looms from the Data/Formatter board and NRZI board (if Fitted)

(c) Release the head retaining screws from the head plate assembly and remove the head by feeding each edge connector through the cable aperture.

When replacing the write/read head, reverse the removal procedure. Perform the checks and adjustments of Section VII.

2.10 ARM DRIVE CONTROL

2.10.1 Arm Drive Motor

(a) Disconnect the main power and remove the front cover plate.

(b) Cut the tie wraps from the spring anchors, and unhook the tension arm springs.

(c) Unsolder the arm drive motor connections.

(d) Release the motor retaining screws and withdraw the motor from the arm drive assembly.

When replacing the arm drive motor, reverse the removal procedure. Ensure that the motor pinion engages the arm drive gear and the white wire is connected to the arm drive motor +VE terminal. Perform the checks and adjustments of Section VII.

2.10.2 Position and Limit Sensors

(a) Remove the front cover plate.

(b) Disconnect SKAE or SKAF plug; appropriate to the arm sensor to be removed.

(c) Release the optical limit sensor from the arm drive assembly.

When replacing the arm position sensor or the optical limit sensor, reverse the removal procedure and replace the tie wraps on the springs. HOWEVER, BEFORE FITTING a new arm position sensor perform the tape path checks and adjustments of Section VII.

2.10.3 Tension Assembly

(a) Cut the tie wrap from the spring anchor, and unhook the tension arm spring.

(b) Remove the tension arm retaining screws and withdraw the tension arm assembly.

CAUTION

DO NOT RELEASE THE CAP-HEAD CLAMP SCREW.

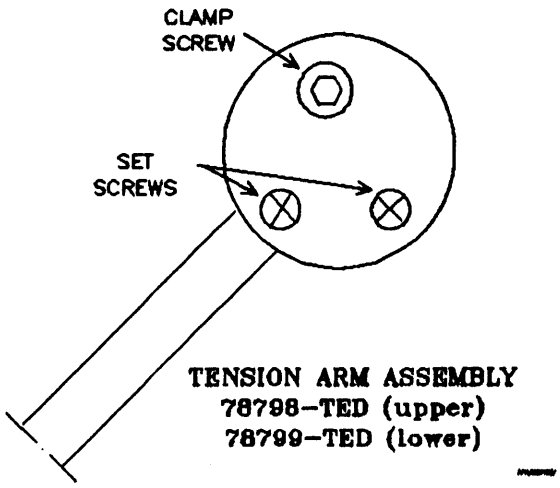


Figure 2-7 Tension Arm

When replacing the tension arm assembly, reverse the removal procedure and fit a new tie wrap. Make sure that the locating pins are not pushed onto the bearing housing after they have been replaced. Perform the checks and adjustments of Section VII.

2.10.4 Arm Drive/Housing Assembly

(a) Disconnect SKR and SKAD from the Control/Mother board. See Fig. 3-6.

(b) Release the arm housing/arm drive retainers at the front of the casting. Withdraw the assembly.

When replacing the arm drive/arm housing assembly, reverse the removal procedure. BEFORE FITTING the arm drive assembly ensure that both push rods are located correctly in the rocker arm moldings. Hold the assembly upright (vertically) while positioning on the casting After bolting it to the casting, check that the push rods are still located correctly before fitting the tension arm assemblies.

[3] CARD CAGE ASSEMBLIES

3.1 ICU CARD CAGE

(a) Disconnect all cables from the Drive Interconnect board.

(b) Disconnect the ICU supply from the transport supply.

(c) Remove the four screws which hold the Drive Interconnect board onto the cage and lift it off. (Figs. 3-1 and 3-2) Pull the HP-IB Interface and the Master Controller boards out of the cage.

(d) The ICU supply may be taken off of the card cage by first removing the protective shield and then releasing the four mounting screws. (Figs. 3-3 and 3-4). However, it does not affect the removal of the ICU card cage.

(f) Remove the six screws which hold the card cage to the Control/Mother board (Fig. 3-5).

(g) To replace, reverse the removal procedures.

3.2 TRANSPORT CARD CAGE

(a) Remove the head lead retaining clips, the interface cables plugged into the Control/Mother board, and all PCA within the guide.

(b) Remove the screws securing the card guide to the Control/Mother board main frame.

(c) When replacing the card cage, reverse the removal procedure.

3.3 CONTROL/MOTHER BOARD (AND HEATSINK)

(a) Disconnect all electric connectors on the Control/Mother board. See Figure 3-6.

(b) Remove the ICU card cage and the transport card guide.

(c) Release the retaining screw, located on the upper support bar, and remove the board from the transport mounting.

NOTE

Removing the screw attached to the lower support bar is unnecessary because it used as a guide and will lift out of the lower bar when you remove the heatsink.

(d) When replacing the Control/Mother board, reverse the removal procedure.

(e) Perform the checks and adjustments of Section VII.

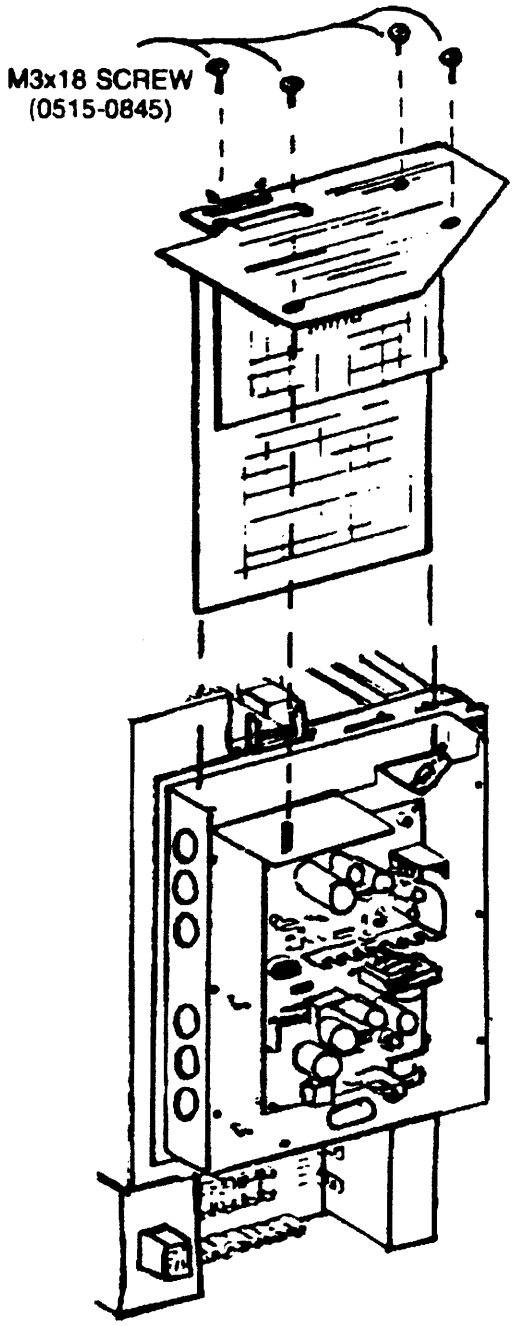


Figure 3-1 ICU Board Removal

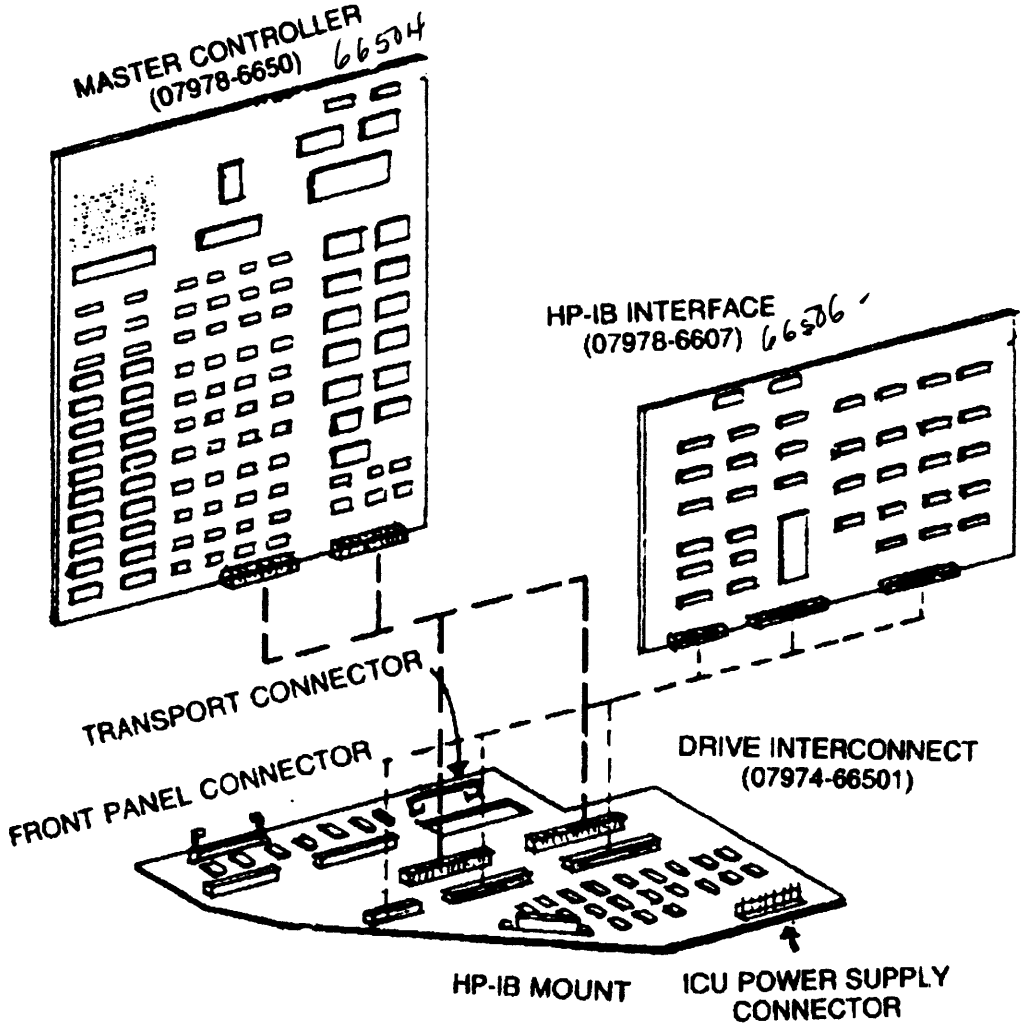


Figure 3-2 ICU Interconnections

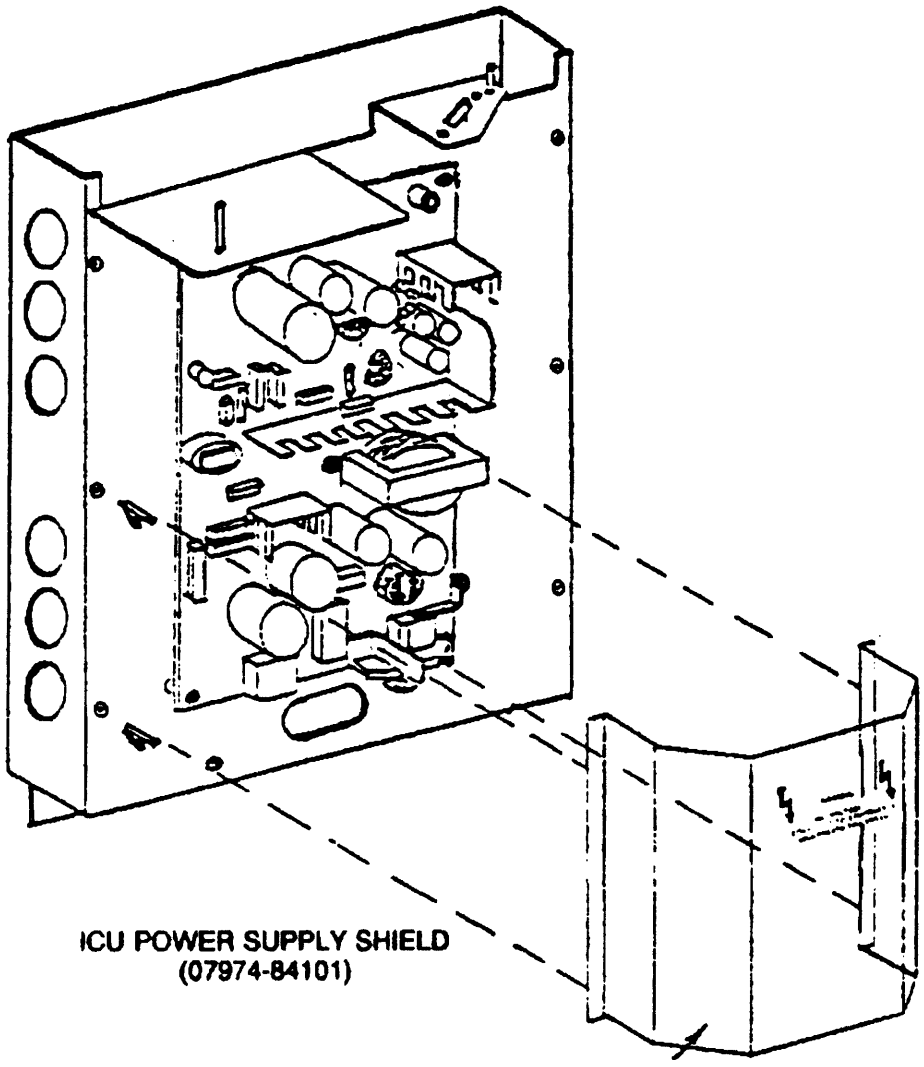


Figure 3-3 ICU Power Supply Shield

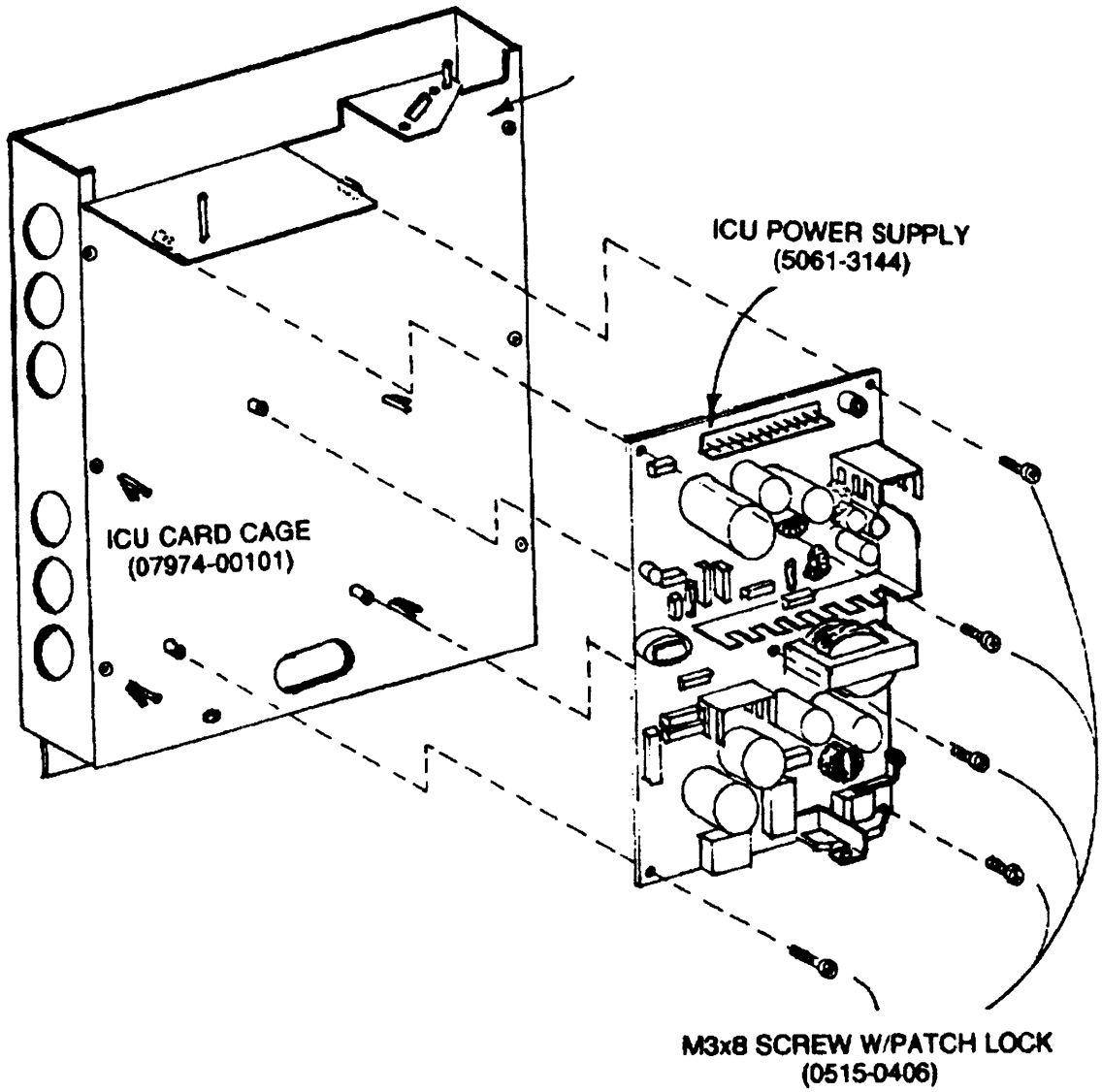


Figure 3-4 ICU Power Supply

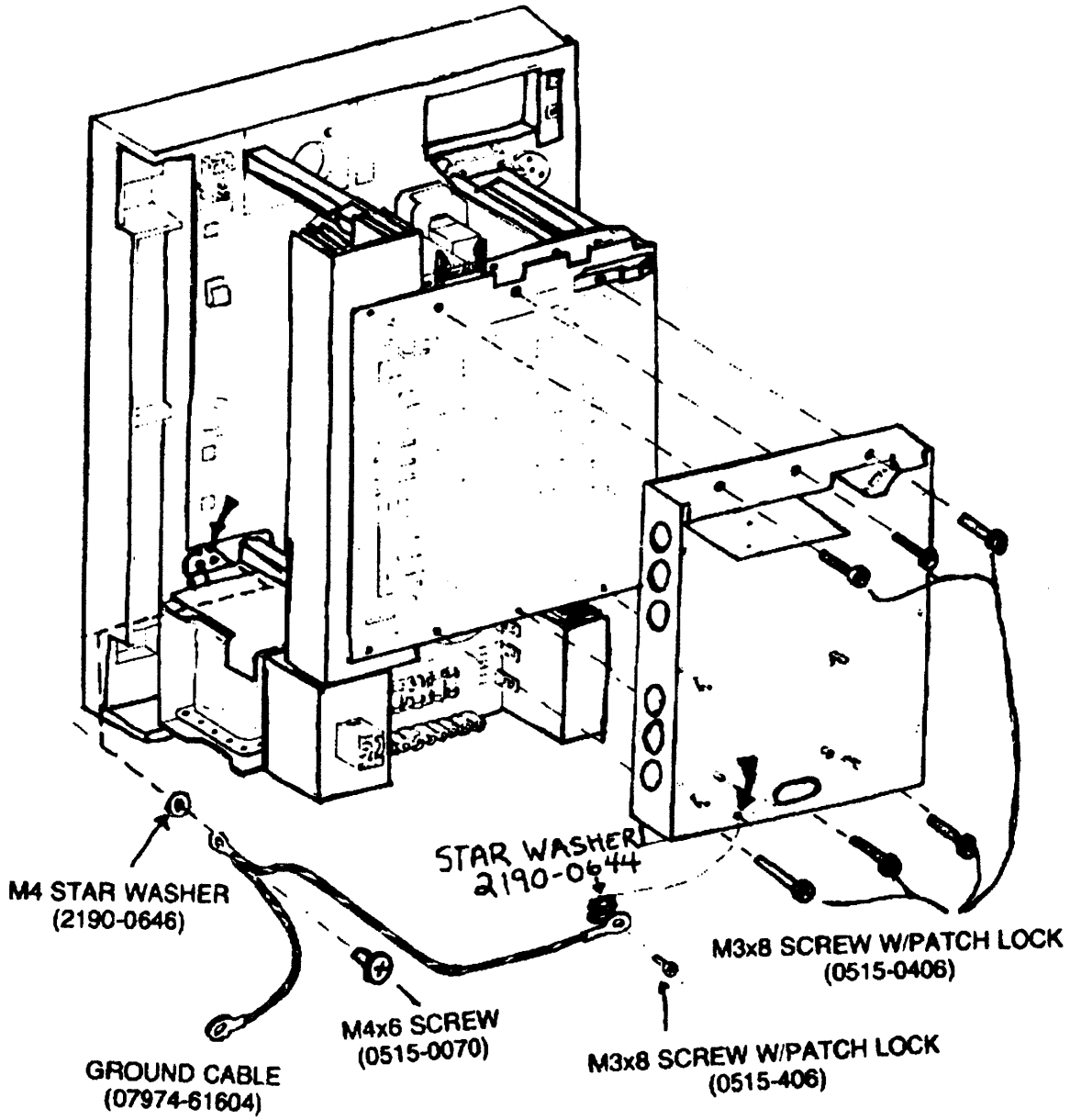


Figure 3-5 ICU Card Cage

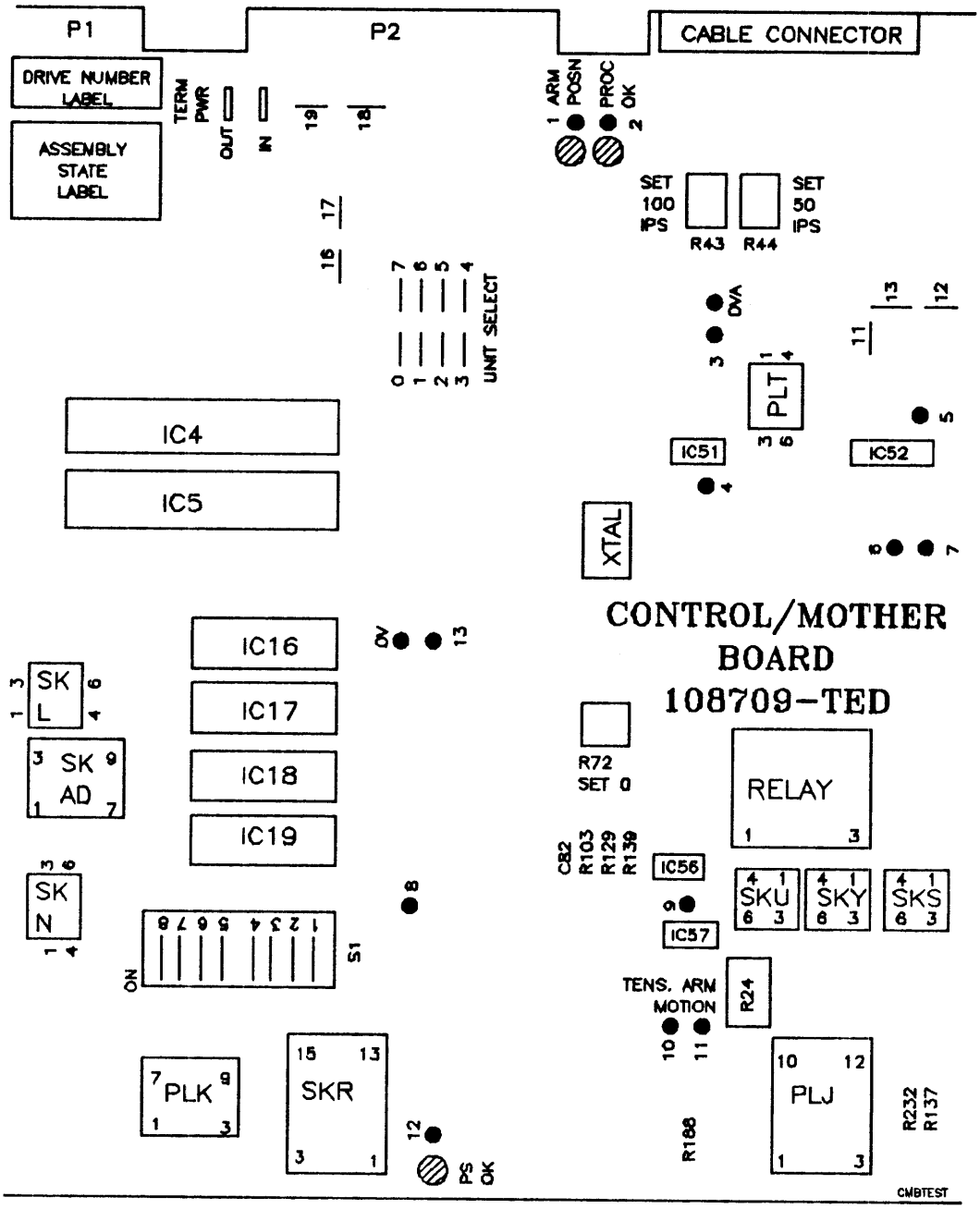


Figure 3-6 Control/Mother Board

[4] TRANSPORT POWER SUPPLY

4.1 MAIN SUPPLY

(a) Turn the power switch to off and disconnect the main power input lead.

(b) Disconnect SKA, SKB and 0 V link wire in PLB cableform.

(c) Remove the connections from the front panel assembly ON/OFF switch and earth lead.

(d) Disconnect the green and black chassis earth leads from the casting.

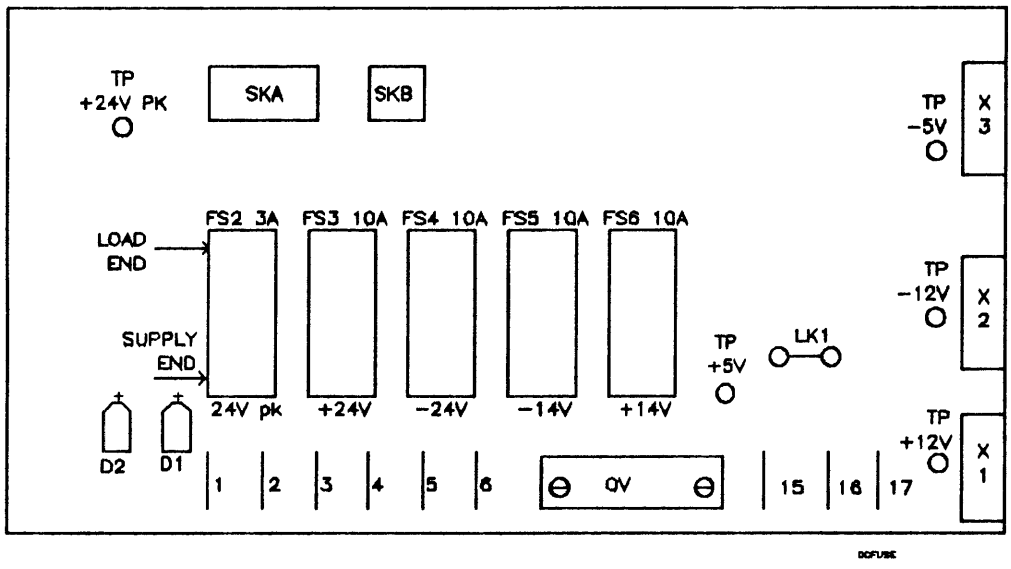
(e) Remove the five retaining screws. The power supply retaining screws are captive: they cannot be removed without a very long #2 posi-driver (eg. Stanley 64-592 2 pt POSI DRIV).

(g) Support the power supply unit while removing the unit retaining screws and carefully pull the unit clear of the locating dowel pins.

When replacing the power unit, reverse the removal procedure and perform the checks and adjustments of Section VII.

CAUTION

Check for the correct voltage selection and fuse rating when replacing the power supply unit.



TRANSPORT POWER SUPPLY PCA
105678-TED

Figure 4-1 Transport Power Supply PCA

4.2 LINEAR REGULATORS (X1,X2,X3)

(a) Turn off the power and disconnect the supply input lead.

(b) Remove the regulator retaining screw and insulating washer.

(c) Unplug and remove the regulator. Retain the mica washer.

When replacing the regulator: apply fresh heatsink compound, plug in the regulator and insulating washer, secure the retaining screw and ensure the regulator is seated correctly before tightening.

4.3 +5V SWITCHING REGULATOR

(a) Turn off the power and disconnect the supply input lead.

(b) Disconnect the following spade terminals from the power unit: 16 (white); 11 (black); 3 (red). See Fig. 4-1.

(c) Remove the regulator retaining screws and detach the assembly from the power unit.

When replacing the regulator assembly, reverse the removal procedure and perform the check and adjustments of Section VII.

NOTE

Ensure that the red fiber washer and insulating bush are inserted in the correct position when re-assembling the regulator.

4.4 POWER SUPPLY PCA

(a) Turn off the power and disconnect the supply input lead.

(b) Remove the linear regulators, Section 4.2.

(c) Remove the spade plug connectors.

(d) Unscrew the four retaining screws and remove the PCA.

To replace the assembly, reverse the removal procedure.

This page intentionally left blank.

CONTENTS: SECTION VII

CONTENTS: SECTION VII

---FIGURES---

This page intentionally left blank.

ADJUSTMENTS

SECTION VII

[1] GENERAL INFORMATION

These procedures complement the removal/replacement procedures of Section VI. Where applicable, the adjustments have been placed into functional groups such as "Tape Tension" or "Head Assembly". The tests and adjustments within each functional group should be performed in sequence.

After removal or replacement of an assembly, check its operation by performing the specific tests and adjustments for that assembly/functional group. Once the operation is verified on a "local" level, execute **01** * to test the "transport only" functions of the HP 7974A. If test **01** fails, use the diagnostic error log (Section VIII) to determine which adjustments are necessary to correct the problem. When you are sure that the transport is functioning properly, test the overall operation by executing the 100-Level tests *05* and *101*. If either of these tests fail, use the failure codes (Section VIII) to determine which test/adjustments are still needed.

[2] PREPARATION

Before proceeding with configuration and checkout procedures, the following steps must be completed to ensure your safety and allow easy access to all transport assemblies.

(a) Make sure that the work space is in a clean area which allows adequate space for opening and closing the cabinet doors, placing equipment and tools within easy reach, and moving back and forth. The cabinet clearance requirements are specified in Section II.

(b) Completely raise the front and rear leveler feet and move the unit into the work area.

CAUTION

Do not move the unit when the leveler feet are touching the ground. They could cause the unit to tip over and/or become damaged.

(c) Lower the rear leveler feet completely to the floor.

(d) Remove the pins on the front levelers and fully extend the legs before lowering the feet. This will stabilize the unit and prevent it from tipping over when the casting is open.

(e) Open the casting. A two-stage latch secures the drive casting to the cabinet. The latch is balanced so that the second stage catches upon the cabinet if the latch screw becomes loose enough to dislodge the first stage (eg. due to shipping vibration). Its unique design also makes it somewhat tricky to open:

1. Using a 5 mm hex key, turn the drive latch screw clockwise until you can feel the latch move freely.

---

*"0" and "100" level diagnostics are written in *ITALICS*. "200" level diagnostics are written in **BOLD**.

2. Once the latch is free, turn the screw counterclockwise approximately 1/4 turn and, while holding the latch in that position, gently pull the casting out of the cabinet. The casting will only travel about 2-3 cm (1-1.5 in.).

3. Turn the latch clockwise a 1/4 turn, until the second stage clears the cabinet rail, and slowly swing the drive out of the cabinet.

WARNING

Do not swing the casting out rapidly: it is heavy. A 90° door stop has been added to the drive, but it is still necessary to keep your fingers clear of the hinge and inside casting edge when opening and closing the front of the unit.

(f) Inspect the transport for physical damage. Reseat all circuit boards and make sure all the cables are securely connected.

(g) Override the door interlock switch by pushing the door switch in and placing the metal arm, located near the rear of the door switch, between the rear switch washer and the casting. The metal arm will maintain the switch in the "door closed" position until the interlock is reset by pressing the door switch.

NOTE

Overriding the door interlock switch allows you to test electronic assemblies during tape movement/diagnostic operations. If the door interlock switch is not set, diagnostic programs used in the checkout procedures will not operate.

(h) Relax the tension arms. *(NOTE: Perform this step only when needed)*

1. Unload work tape, if mounted.
2. Remove the right hand head cover, place a piece of paper between the EOT/BOT sensor and its reflective block, and close the door.
3. Press LOAD and the arms will drive to their relaxed positon.

CAUTION

If the arms are relaxed with the door open (i.e., the door interlock is overriden), keep clothing clear of the upper hub and take-up reel: they rotate for approximately three seconds after LOAD is pressed.

4. With the paper still in place, turn the power OFF. (The arms will return to their normal position when the paper is removed and the power is turned ON again.)

[3] TOOLS AND TEST EQUIPMENT

3.1 MECHANICAL

Spring Balance (0-680 g;0-24 oz): P/N 8750-0039
Parallel Gauge (for arm roller angle adjustment): P/N 76120-TED
Set of Shims (0.0025;0.003; 0.004; 0.0045; 0.005 in)
Set of Metal Feeler Gauges (compatible with shim sizes given)
Micrometer (for shim measurement)
Metric and English sets of Allen Keys (with screwdriver handles)
Screwdrivers: flat small and large;posi-drives #1, #2 (extra-long)
Plastic Feeler Gauges (0.15 mm,0.28 mm; 0.006 in, 0.011 in)
Non-metallic Potentiometer Adjustment Tool: P/N 8730-0013

3.2 ELECTRICAL

(a) Multimeter. A general purpose multimeter capable of measuring: 10 mV - 250 V dc; up to 240 VAC

(b) Oscilloscope: HP 1740A or equivalent. (It must have a bandwidth of at least 50 MHz)

(c) Digital Frequency Counter (Optional). To check frequencies in the range of 1 kHz to 10 MHz.

3.3 TAPES

(a) Work Tape. A good quality tape (of a recommended type) know to the user to have no data drop-outs. The tape should not contain data of any consequence and should be available for write checks/tests. The transport supply reel must be fitted with a write-enable ring.

(b) Master Alignment (Skew) Reference Tape: P/N 9162-0027

(c) Master Amplitude Reference Tape (IBM # 432152)

(d) Length of looped tape (approximately 500 mm (20 in)). The loops are formed at each end using adhesive tape and must be large enough to pass over the rollers.

(e) A special tape, fitted with an EOT marker postioned 50 mm (2 in) from a BOT marker.

(f) A good quality tape, free from edge damage and known to track correctly, to be used exclusively for tape path checks/adjustments.

(g) Reel of adhesive reflective tape markers.

[4] MECHANICAL TESTS AND ADJUSTMENTS

4.1 TAPE PATH ALIGNMENT

4.1.1 Head Travel

CHECK: Remove the head covers, load a good quality tape to BOT, and run diagnostics Program 04. Carefully push the spring flange of each fixed roller guide, in turn, away from the tape. If the tape movement away from the fixed flange (reference edge) is more than 0.25 mm (0.01 in.), adjust the arm roller angle and/or capstan tracking.

4.1.2 Hub Height

Hub height is pre-set at manufacture and should not require adjustment unless a replacement hub or motor has been fitted.

CHECK

(a) Mount a tape and check that the reels are seated correctly on the hubs. IT IS ESSENTIAL THAT THE REELS USED FOR THIS CHECK ARE UNDISTORTED.

(b) Run the tape forward at low speed, program **50**, and check that the tape does not rub the reel flanges.

(c) Run the tape to BOT in reverse at low speed, program **51**, and check that the tape does not rub the reel flanges.

(d) Repeat steps (a)-(b) at least two more times with different reels. If the tape rubs consistently, adjust the hub height.

ADJUSTMENT

The hub height must be adjusted by trial and error. The required height, from the casting face to the inside flange, is approximately 26mm. **After each adjustment, you must re-check the hub height and tape path travel.**

SUPPLY HUB

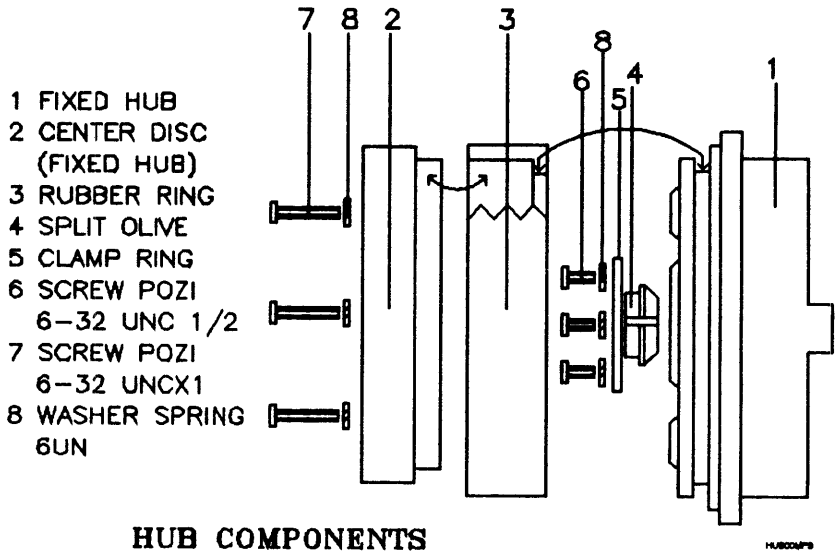
(a) Loosen the hub ejector button retaining screw (located behind one of the toggle arms) until the ejector button springs forward. Remove the button.

(b) Loosen the clamp bar screws and adjust the position of the hub on the motor spindle as necessary.

(c) Tighten the clamp bar and replace the ejector button.

TAKE-UP HUB

Remove the hub cover, loosen the inner hub screws, and adjust the hub as needed. After positioning the hub, tighten the inner screws, and replace the hub cover.



HUB COMPONENTS
TAKE-UP: 105610-TED
SUPPLY: 79140-TED

Figure 4-1 Hub Components

4.1.3 Arm Roller Angle

Arm roller angle adjustment is not normally necessary. Also, tape roller heights are factory pre-set and cannot be adjusted.

(a) **CHECK:** Load a good quality tape to BOT and run Program **04** (Servo Test). Look at the tape as it moves over the rollers. If the tape climbs the roller flanges, tracks to one side, or becomes puckered because of hard contact with the roller flanges, adjust the arm roller angle.

(b) Remove the transport cover and relax the tension arms.

(c) Disconnect the tension spring from the anchor clamp.

(d) Move the upper arm so that the roller is on the "load" side of the bridge rollers. See Fig. 4-2.

(e) Place the parallel gauge across the bridge rollers and move the arm so that the arm roller surface is against the surface of the gauge.

(f) Check that the arm roller is square to the gauge. If necessary, adjust the fit by releasing the arm clamp screw and rotating the arm. Tighten the arm clamp screw after adjustment. See Fig. 4-3. *Ensure that the effective length of the tension arm is not disturbed.* This can be judged by the protrusion of the arm at the rear of the clamp.

(g) Repeat steps (b)-(f) for the lower arm.

(h) Replace the tension springs and tie wraps on the anchor clamp.

(j) Repeat step (a) to verify the tracking. If adjusting the roller angle does not correct the situation, check the rest of the tape path alignment before replacing the arm roller assembly.

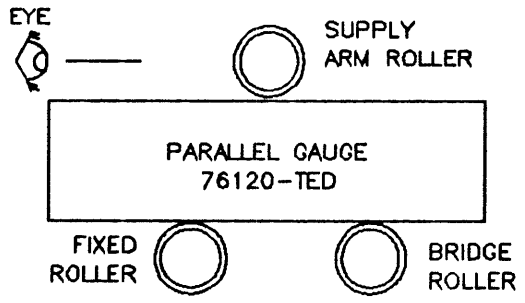


Figure 4-2 Arm Roller Angle Check

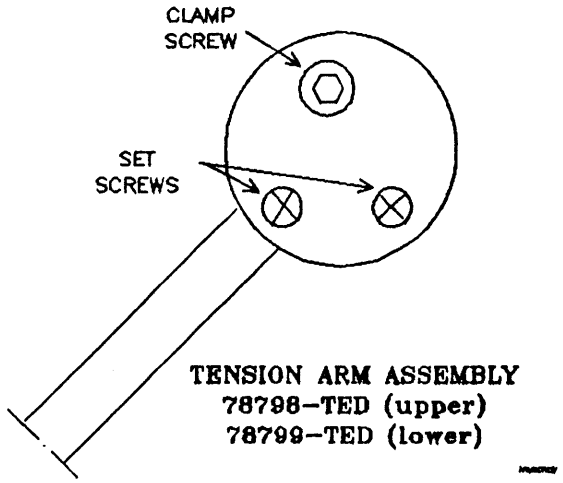


Figure 4-3 Clamp Screw Location

4.1.4 Capstan Tracking

CHECK

(a) Perform the hub height and arm roller angle checks.

(b) Remove the head plate assembly but leave the EOT/BOT sensor connected to the Control/Mother board.

(c) Place a piece of paper between the EOT/BOT sensor and reflector.

(d) Load a work tape and press RESET, after about 15 seconds, before automatic rewind begins.

(e) Run diagnostics program **52** (FWD/REV) and press ONLINE until the tape is moving at its slowest speed. (Pressing LOAD will increase the speed). If the lateral movement of the tape across the capstan is more than ±0.005 in, the capstan tracking needs to be adjusted.

ADJUSTMENT

This procedure assumes that the casting cover plate is on. However, it may be done with the plate removed.

(a) Remove the capstan pulley and strobe disc from the motor shaft.

(b) Remove the strobe disc from the pulley and replace the pulley on the motor shaft.

(c) Loosen the four motor mounting screws partially so that the motor is held against the mounting face by the pressure of the spring washers.

(d) Remove the head plate assembly from the transport. Do not disconnect.

(e) Place a piece of paper between the EOT/BOT sensor and reflector on the head assembly.

(f) Mount a scratch tape and press LOAD and allow the tape unit to search for BOT. Press RESET, after about 15 seconds, before the unit goes into automatic rewind.

(g) Run diagnostic program **52**. Use ONLINE and UNLOAD to adjust the forward/reverse transition time to 3-4 seconds. ONLINE decreases the motor speed and LOAD increases the motor speed.

(h) While tape is transitioning between forward and reverse, gently exert force up or down on the capstan motor (at a point near the casting) and observe the direction of the tape travel.

CAUTION

Do not press on the capstan tachometer, it will disturb the test and possibly damage the tachometer. The tachometer is the rear piece of the capstan motor assembly (behind the wires).

(i) Set POWER off and remove the tape from the capstan. Release the motor mounting screws sufficiently to insert a 0.1 mm (0.004 in) feeler gauge between the capstan motor face and the casting. Refer to Fig. 4-4.

If an upwards force was required, insert the feeler gauge BELOW THE BOTTOM PAIR of mounting screws but in contact with them. If a downwards force was required, insert the feeler gauge ABOVE THE TOP PAIR of mounting screws but in contact with them.

(j) Lightly tighten all the mounting screws to clamp the feeler gauge.

(k) Replace the tape. Set POWER on and repeat (f) to (j) using larger or smaller feeler gauges as required. The correct adjustment is achieved when lateral movements of less than 0.12 mm (0.005 in) coincide with transitions of 3-4 seconds.

(l) Set POWER off and remove tape from capstan. Remove capstan and loosen the capstan motor mounting screws. Re-assemble with the special shim of the correct value, determined in (k), inserted between the capstan motor and the transport casting. Tighten all screws evenly.

(m) Replace capstan and strobe. Repeat the tape tracking check to verify that the tape traverse has been corrected.

(n) Refit the head plate assembly. Tighten the screws sequentially and by increments. Replace the front cover plate, head plate covers and take-up reel.

(o) Perform tape speed and head deskew adjustments.

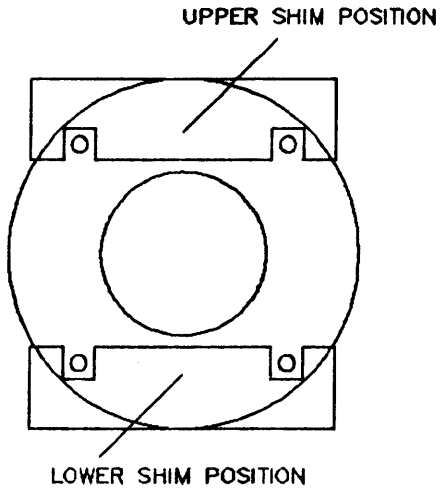


Figure 4-4 Capstan Shimming

4.2 TENSION ARM TRAVEL

4.2.1 Optical Arm-Limit Switch

(a) Open the casting and gain visual access to the LEDs on the Control/Motherboard. See Fig. 4-5

(b) Place a piece of paper between the EOT/BOT sensor and reflector and turn the "POWER" switch on. This will place the tension arm in the relaxed position. DO NOT THE TURN POWER OFF!

(c) Use a write enable ring to hold one of the tension arms in the operating position.

(d) Move the other tension arm off of the resting pad approximately 3/16 inch. The "ARM POSITION" light on the Control/Motherboard should go out.

(e) Continue to move the arm until the tension arm roller is approximately parallel to the fixed roller and the bridge roller. The light should come back on.

(f) Repeat steps (c) through (e) for the other tension arm.

(g) If the "ARM POSITION" LED does not light, replace the appropriate sensor. If the position of the arm is incorrect when the LED lights, adjust the position of the appropriate optical sensor.

4.2.3 Arm Postion

(a) Load a scratch tape.

(b) Slacken the arm position sensor clamp screws.

(c) Rotate the arm housing until the arm corresponds with the center mark on the casting. See Fig. 4-5.

(d) If correct position cannot be achieved, clamp the housing in mid-position and adjust the arm sensor coupling.

CAUTION

The position of the coupling on the shaft is different for each arm sensor assembly.

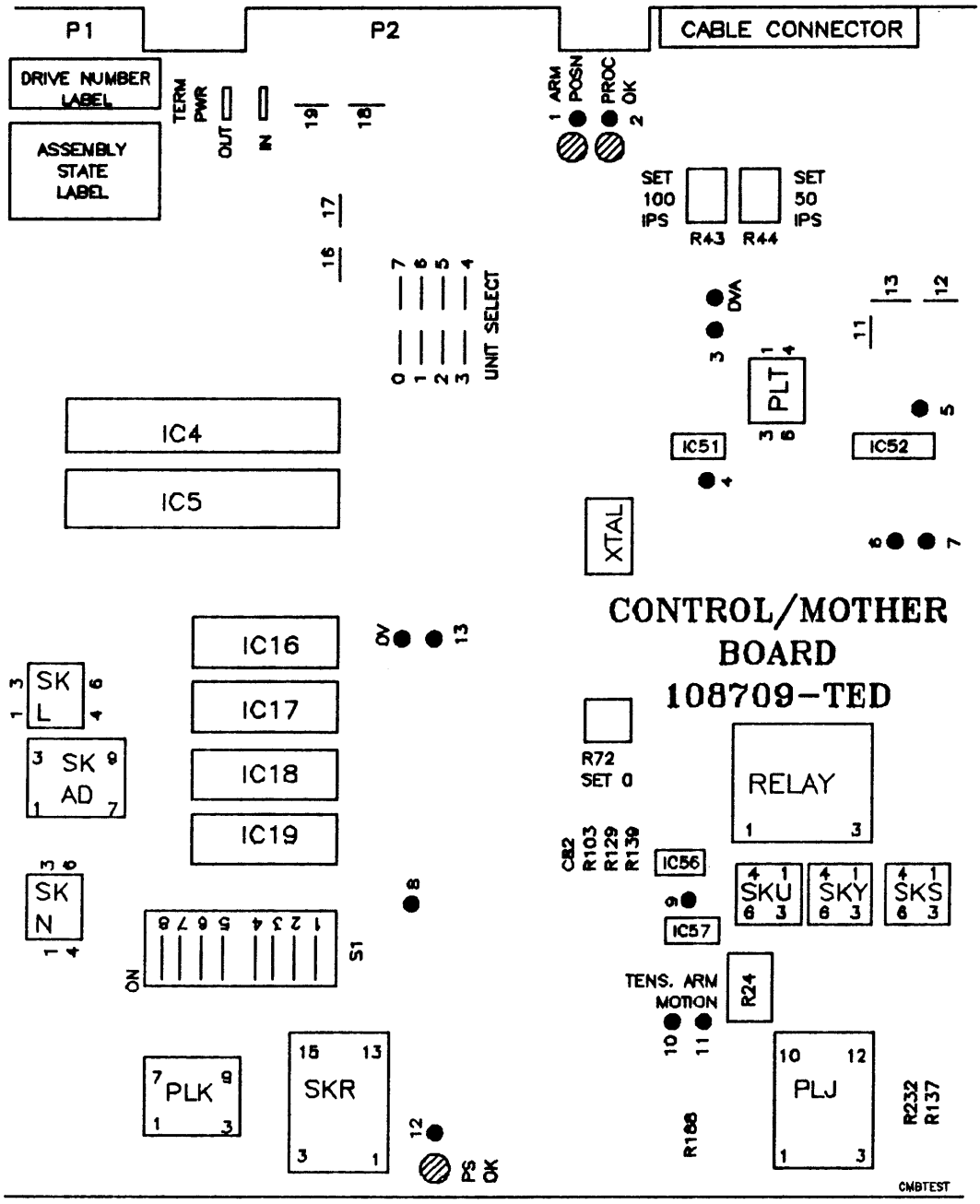


Figure 4-5 Control/Mother Board Test Points

4.2.4 Arm Sensor Coupling

This procedure is not normally necessary unless a new arm sensor assembly has been fitted.

(a) Remove the two arm position sensor retaining screws. Withdraw the sensor from the arm drive assembly. The sensor must be supported to protect the wiring loom from the optical sensor.

(b) Slacken the arm coupling grub screw and rotate the coupling counterclockwise on the shaft, to the position indicated in Fig. 4-5.

(c) Hold the coupling and shaft against the internal stop, and tighten the coupling set screw.

(d) Refit the arm position sensor and repeat the arm position adjustment.

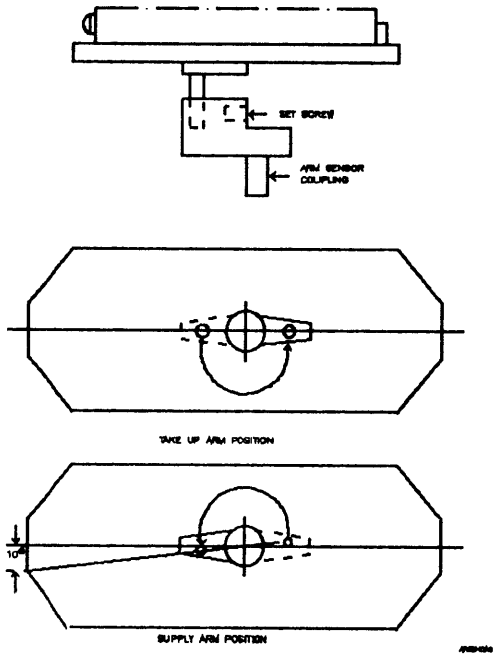


Figure 4-6 Arm Sensor Assembly

4.2.5 Arm Drive Micro-switches

STOP Micro-switch (upper)

When the upper arm is driven up, it should stop within 1 mm of the top dead center position of the arm path. (Refer to Fig. 4-7) If the arm drops slowly immediately after it has stopped, then the micro-switch has operated too far along the cam. If, on restart, the arm rises more than 1 mm before falling, then the micro-switch has operated too early on the cam. Adjust the micro-switch operating point by moving the switch plate via the mounting slots.

UP/DOWN Micro-switch (lower)

The up/down micro-switch plate is also adjustable via the mounting slots. As long as the switch operates on the cam, this adjustment is not critical.

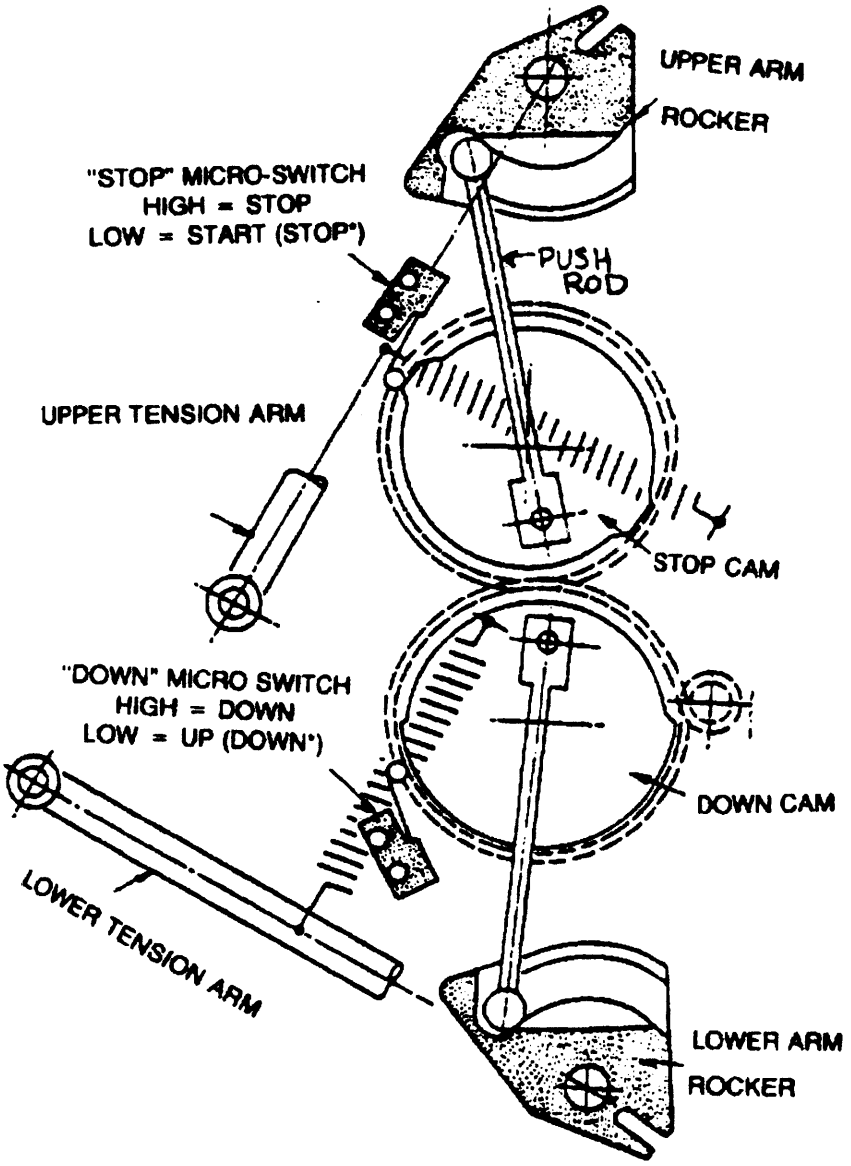


Figure 4-7 Arm Drive Assembly

4.3 TAPE TENSION

Tape tension resulting from the tension arm spring is balanced on either side of the capstan. If one arm and spring assembly is changed, the replacement assembly can be balanced against the other arm. If both assemblies are replaced, tension must be set on the upper arm and the lower arm adjusted to the upper arm.

4.3.1 Tension Balance Test

(a) Mount a scratch tape (8.5 inches in diameter maximum) so that the head and capstan are by-passed. Wind the tape by hand until there are 4 to 5 turns on the take-up reel.

(b) Insert a piece of paper between the EOT/BOT sensor and reflector.

(c) Hold the tape, as indicated in Fig. 4-8, and press the **LOAD** button.

(d) When tape is tensioned, press the RESET button, and momentarily retain your hold on the tape.

(e) Release the hold on the tape and observe the motion. The tape should remain stationary or gently move. If the tape winds to the supply reel or the take-up reel, the servo system is unbalanced.

If the tension of one arm is correct, adjust the other arm by repositioning the appropriate spring anchor until the tape remains stationary during the tension test. If the tension of both arms is incorrect, adjust the tension of the upper arm and balance the lower arm tension.

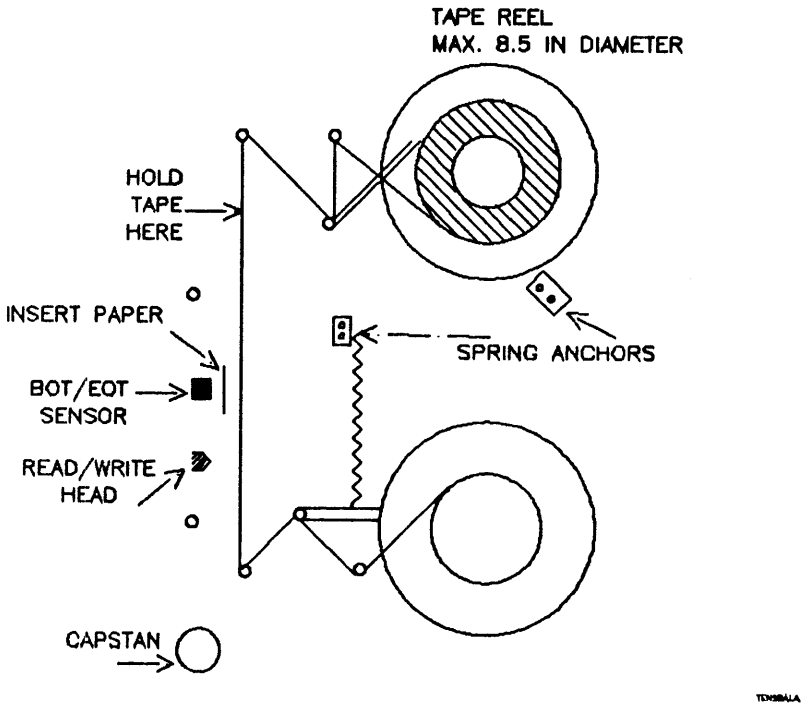


Figure 4-8 Tension Balance

4.3.2 Spring Tension (upper arm)

(a) Relax the tension arm by inserting a piece of paper between the EOT/BOT sensor and the reflector. Next, turn OFF the power. Do not turn the power on again until you are finished with the adjustment.

(b) Connect the tape test loop and spring scale as indicated in Fig. 4-8. Take two readings with the spring balance:

1. Pull the arm from the parked position to the center. The balance should indicate 300-310 gm.
2. Pull the arm from the parked position all the way to the top then slowly let it down until it reaches the center. The balance should indicate 250-260 gm.

(c) Adjust the spring anchor until the force required to position the tension arm to the center mark on the casting is nearly the mean of the two measurements in (b): 270 gm (9.5 oz)

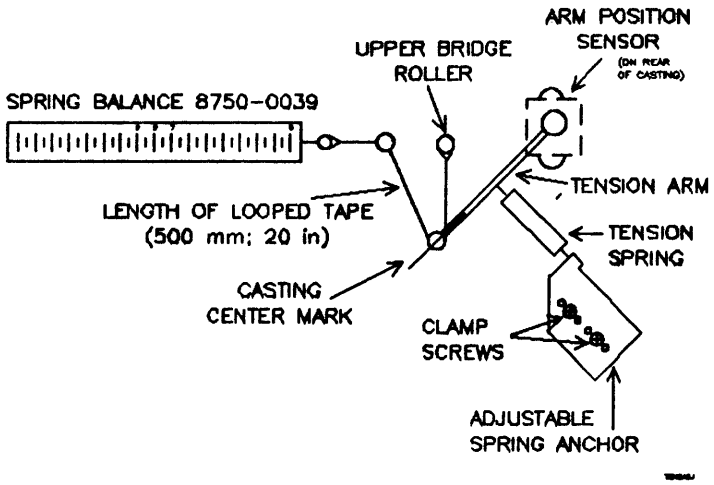


Figure 4-9 Tension Arm Spring Adjustment

4.3.3 Tension Arm Damping Check

(a) Mount a scratch tape and run diagnostic program *200*.

(b) Run diagnostic program **62** (Write all 1's).

(c) Rewind tape to BOT. (program **30**)

(d) Connect oscilloscope to Channel 2 on the Data Formatter (Fig. 5-7) and trigger from TP4 on the Control/Mother Board (Fig. 4-5).

(e) Run diagnostic program **50** (step FWD, low speed).

(f) Compare the waveform on the oscilloscope to Fig. 4-10.

(g) Run diagnostic program **73** and position the tape to the middle of the reel.

(h) Run diagnostic program **50**. Observe the waveform.

(i) Run diagnostic program **73** and run tape to EOT.

(j) Run diagnostic program **30** for 5 to 6 seconds. This moves the tape back from EOT.

(k) Run diagnostic program **50**. Observe the waveform.

(l) The first overshoot on the waveform for all three tests should be less than 6% of the total waveform amplitude and the third waveform should be less than 2% of the total amplitude.

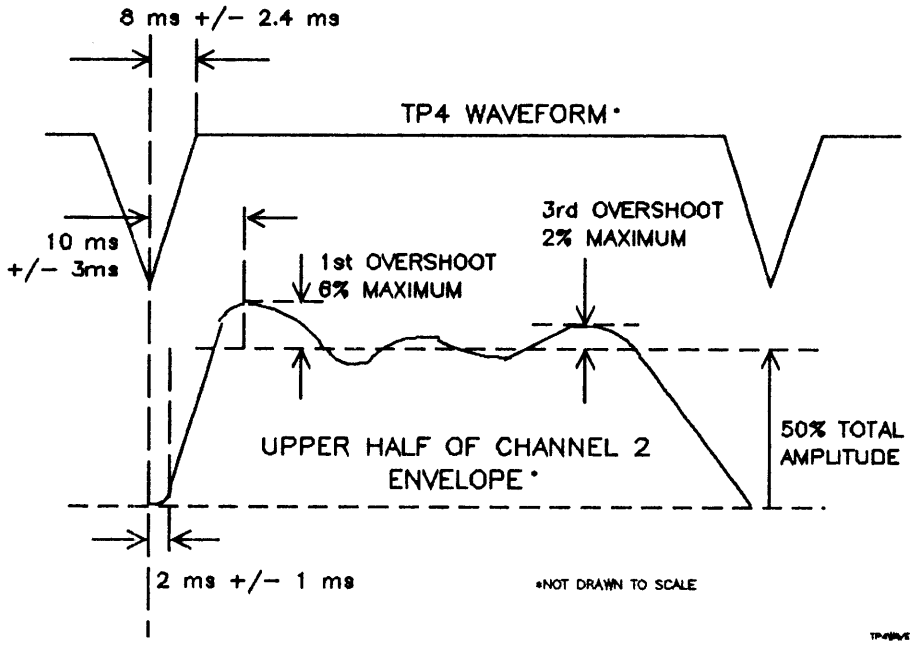


Figure 4-10 TP4 and Channel 2 Example Waveforms

4.4 MISCELLANEOUS ASSEMBLIES

4.4.1 Door Catch Plate

Set turn off the power and remove the front cover plate. Slacken the right-hand screw and adjust the catch so that the door shuts positively, and does not require excessive pressure to open. Tighten the screw. Adjust the two left-hand screws so that the door closes easily and the door seal is in contact with the casting. Tighten the screws.

4.4.2 Write Enable Ring Sensor

(a) Remove the head cover, and any tape you may be using, from the transport.

(b) Override the door interlock switch and turn the power on.

(c) With a straight edge (ruler), depress the ring sensor probe to the same height as the rear hub flange surface and check for +12 V (wrt power unit 0V) at W/Y terminals. (Fig. 4-11)

(d) If +12V is not available, depress the ring sensor probe further to determine whether the micro-switch will operate. If it operates, adjust the position of the plastic cone on the actuator rod shaft.

(e) If the micro-switch does not operate, load a write-enabled work tape to BOT and check the voltage across R188 on the Control/Mother board. Refer to Fig. 4-5. If it is not within 0.45V ±10%, the Control/Mother board is faulty.

(f) If the voltage across R188 is correct, adjust the position of the sensor.

(g) After trying steps (a)-(f), mount a write-enabled work tape. Press LOAD, followed by RESET after 3 seconds. If the Write Enable LED comes on, the adjustment was successful. If the Write Enable LED does not come on, replace the microswitch.

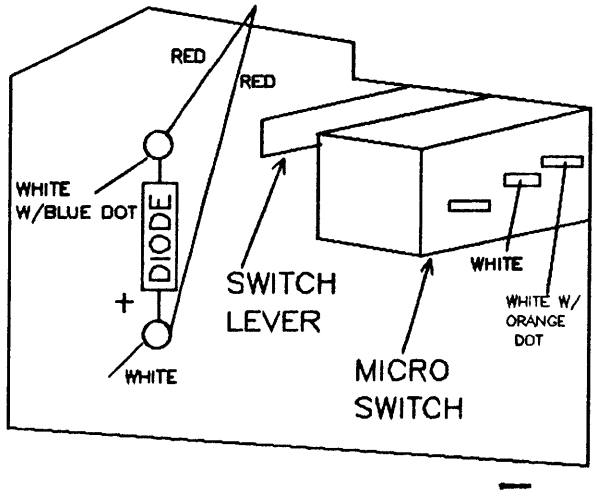


Figure 4-11 Write-enable Ring Sensor Connections

[5] ELECTRICAL TESTS AND ADJUSTMENTS

5.1 TRANSPORT POWER SUPPLY

Figure 5-4 illustrates the test points on the transport power PCA. When all power lines are present,* the PS OK indicator on the Control/Mother board should be lit and the voltage at TP12 (Fig. 4-5) should be low. If not, check the AC inputs (Figure 5-1) and dc fuses (Figure 5-2).

---

*Does not include +24 V servo power via FS3.

The output on the±5V and the ±12V regulated supplies should be within the ranges presented in Figure 5-3. Also verify the +5V switched regulator is supplying +4.8V to +5.2V across C97 on the Data Formatter board when all the boards are seated in the card cage. (Refer to Fig. 5-7).

SUPPLY INPUT (measure at D1/D2 anode)	Nominal	Maximum	Minimum
Within ±10% of supply setting	18.5 V	20.6 V	15.6 V
Within ±1% of supply setting	18.5 V	18.9 V	17.2 V

Figure 5-1 AC Voltages

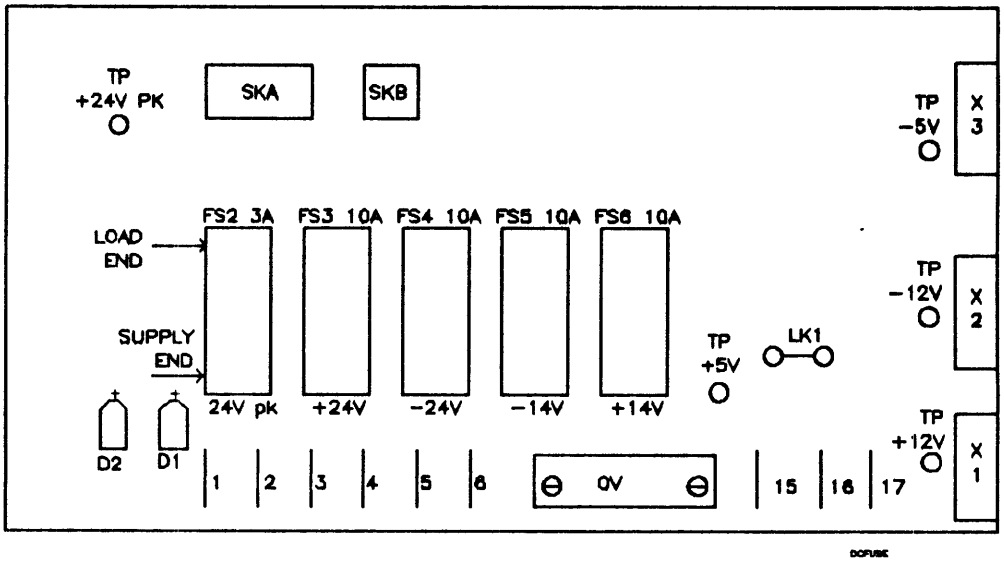
FUSE	MEASUREMENT (Assuming supply input voltage within ±1% of nominal voltage.)
FS2 (2A)	+24 Vpk ±10% fwr (use an oscilloscope)
FS3 (10A)	+25.4 V max; +20.1 V min
FS4 (10A)	-25.4 V max; -20.1 V min
FS5 (10A)	-15 V max; -12 V min
FS6 (10A)	+15 V max; +12 V min

Figure 5-2 DC Fuse Measurements

REGULATOR	TEST POINT	DC VOLTAGE (MEASURED) NOM	MAX	MIN
+5V *	TP +5V	+5.2V	+5.3V	+5.1V
-5V	TP -5V	-5.0V	-5.2V	-4.8V
+12V	TP +12V	+12.0V	+12.5V	+11.5V
-12V	TP -12V	-12.0V	-12.5V	-11.5V

*Refer to +5 V Adjustment Procedure

Figure 5-3 Regulated Voltages



TRANSPORT POWER SUPPLY PCA
105678-TED

Figure 5-4 Transport Supply PCA

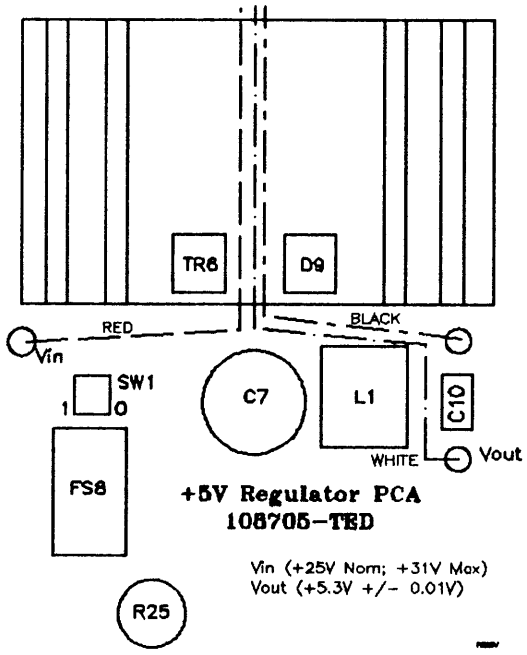


Figure 5-5 +5V Regulator PCA

5.1.1 +5V Adjustment

(a) Override the door interlock switch and turn the main power on.

(b) Check that SW1 on the +5V regulator PCA (Fig. 5-5) is in position "1".

(c) Monitor the +5V rail at Vout. If not at +5.3V ±0.01V, adjust R25.

(d) Check, with all the boards in the card cage, that the voltage across C97 on the Data/Formatter board is in the range +4.85V to +5.2V.

5.2 SPEED

(a) Mount a scratch tape

(b) Run diagnostic program **64** (Read FWD- High speed, strobe on). Adjust **R43** on the Control/Motherboard so that the dots on the capstan strobe disc do not drift more than 1 dot/2 secs.

(c) Run diagnostic program **65** (Read REV - Low speed, strobe on). Adjust **R44** on the Control/Motherboard so that the dots on the capstan strobe disc do not drift more than 1 dot/2 secs.

5.3 HEAD PLATE ASSEMBLY

5.3.1 Read/Write Head

After replacement/refitting the write/read head plate assembly, check the threshold and skew adjustments (Sections 5.4 and 5.5) and run test **01**.

5.3.2 EOT/BOT Sensor

CHECK

(a) Run diagnostics program **36**. This unloads the tape and should register asterisks for both BOT and EOT with no tape loaded.

(b) Remove the head covers and load a short work tape. The tape should run to and stop at BOT. *NOTE: A special tape with an EOT marker postioned 50 mm (2 in.) from BOT makes this check easier.*

(c) Run diagnostics program **64** and check that EOT is detected. Rewind tape (program **30**) and check that it stops at BOT.

(d) If steps (a)-(c) did not work correctly, adjust the EOT/BOT sensor.

ADJUSTMENT

(a) Turn power on and insure that the tape is unloaded.

(b) Verify that the reflector is clean and parallel to the EOT/BOT sensor.

(c) Connect the ground of the oscilloscope to 0V (terminal 1) of the EOT/BOT PCA.

(d) At the rear of the EOT/BOT sensor board, monitor the dc voltage at IC1 pin 9. Adjust R2 (BOT sensor) for, as close as possible, +200 mV. Reject the sensor if the voltage is more the +300 mV or less than +100 mV.

(e) Repeat step (c) for the EOT. This time monitor IC1 pin 7 and adjust R4.

(f) Load a scratch tape and cancel the load point search before BOT is reached.

(g) Check that more than +3.5 V is indicated at IC1 pins 7 and 9 (maximum of +5 V.) This check is to insure that sensor output exceeds the 1.5V threshold of IC1 with no BOT or EOT present.

(h) Press **LOAD** and continue to BOT.

(i) Run diagnostic program **63**. This runs the tape to EOT, at low speed, to check that the EOT marker is detected. Rewind, program **30**, the tape to check that BOT is detected.

5.3.3 Erase Head

The function of the erase head may be checked by running diagnostics program 60.

Because the write head can effectively erase (over-write) the width of its own tracks, reading and writing on the same tape seems to be correct. However, if the erase head is not functioning, erasure does not occur between tracks and when the tapes are interchanged, minor track misalignment adds incoherent data between tracks and causes errors.

Residual (Self) Erasure

(a) Load an amplitude reference tape (IBM 432152) to BOT.

(b) Select and run diagnostic program **10** (Select PE) followed by **62** (Write all 1s). Write approximately 3 minutes. Rewind tape (program **30**).

(c) Monitor and note positive peak signal levels on all channels.

(d) Select and run diagnostic program **60** (erase) for about 1 minute before rewinding the tape.

(e) Read forwared (low speed - program **63**) over the pre-recorded region. Rewind to BOT when the erased portion is encountered.

(f) Repeat (e) four more times and on the last read pass, monitor and note the channel positive peak levels, as in (c).

(g) Check that the signal reduction ((c) to (f)) of each channel does not exceed 10%, i.e. :

$$\frac{\text{Read Only signal}}{\text{Read/Write signal}} \times 100 \text{ is greater than } .9$$

(h) If any channel reduction is greater than 10%, the head assembly should be rechecked.

5.3.4 Head Wear

(a) Clean the head and the tape path.

(b) Override the door interlock.

(c) Check the tape speed (Section 5.2), channel threshold (Section 5.4), and the arm roller angle (4.1.2). Adjust if incorrect.

(d) Load a write-enabled master amplitude reference tape.

(e) Run diagnostics programs **28** and **62** to write 1600 bpi from BOT, for four minutes minimum. Halt the tape.

(f) Use diagnostic programs **65** (read reverse low-speed) and **63** (read forward low-speed) to run the recorded area of the tape over the heads five times. This allows self-magnetization effects to stabilize.

(g) On the sixth reverse pass, record the positive peak reverse voltage of each channel. Ensure that only data recorded in (f) is used.

(h) On the sixth forward pass, record the positive peak forward voltage of each channel. Ensure that only data recorded in (f) is used.

(i) Calculate, for each channel, the percentage reduction in signal amplitude of the reverse read signal compared with the forward read signal. If the reduction exceeds 20% for any channel, and its adjacent channels have similar differences, the head must be replaced. (Section VI)

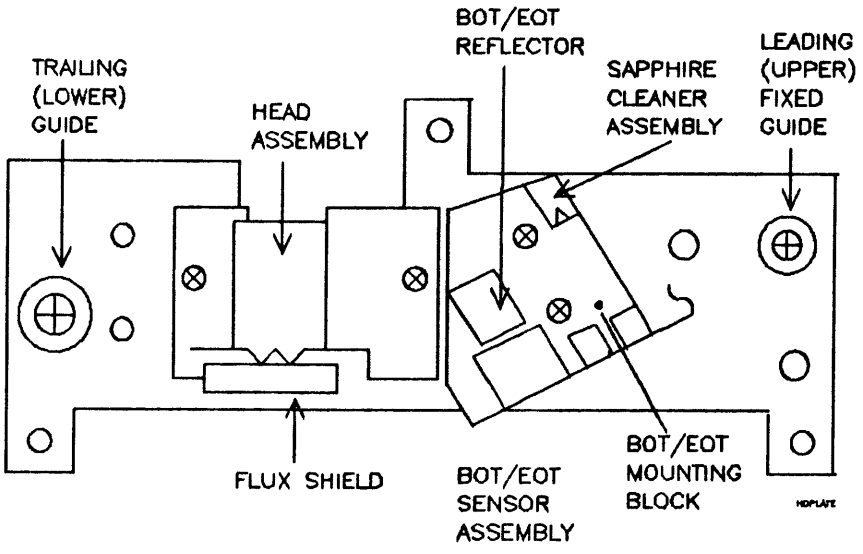


Figure 5-6 Head Plate Assembly

5.4 THRESHOLD

This procedure must be performed for both operating speeds, 50 ips and 100 ips, which are assumed to be correct. Fit the Data Formatter board in the outer slot of the card cage and check that the head cables are correctly connected. If NRZI is installed, check the connecting cables.

5.4.1 PE Read Gain

(a) Load a scratch tape and run diagnostic program *200*.

(b) Run, in order, diagnostic program **28** (Select PE), **10** (low speed) and **62** (Write all 1s).

(c) Monitor the analog test points on the Data Formatter (Fig. 5-7) for each channel. The peak-to-peak votage should be 4 V ±1.5 V.

(d) Record the positive peak amplitude with respect to the the 0V test point for each channel.

(e) Calculate:

1. The average value of the nine channel amplitude measurements.
2. The maximum channel amplitude measurement to the minimum channel amplitude measurement ratio. The maximum channel to minimum channel ratio must not exceed1.38.

(f) Monitor the +THS test point* on the Data Formatter and check for a level within 22%-28% of the the calculated positive peak average. If not within the limits, adjust RV4 until the signal is 25% of the calculated positive peak average.

(g) Rewind the tape (program **30**) and run diagnostic programs **9** (high speed) and**62**. Repeat steps (c)-(g) and adjust RV3.

---

*Located on the left-hand side of IC2 in Issue A boards and to right-hand side in subsequent issue boards.

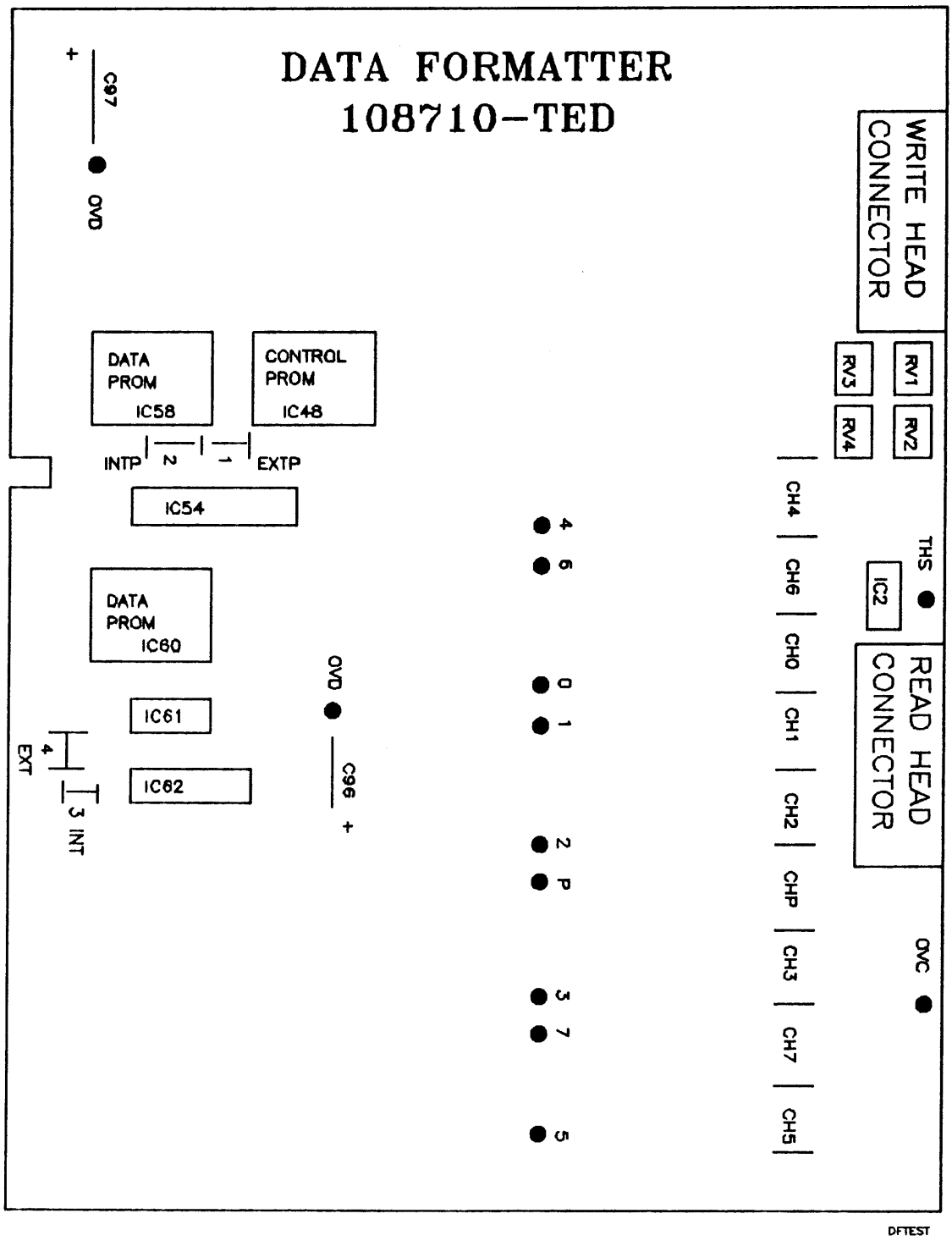


Figure 5-7 Data Formatter Board Test Points

5.4.2 NRZI Read Gain (Option 800)

Disregard this procedure if Option 800 is not installed.

(a) Load a scratch tape and run diagnostic program *200.*

(b) Run, in order, diagnostic programs **27** (Select NRZI), **10** (high speed) and **62** (Write all 1s).

(c) Monitor the analog test points on the NRZI board (Fig. 5-8) for each channel and record the positive peak amplitude with respect to 0V TP.

(d) Calculate:

1. The average value of the nine channel amplitude measurements
2. The maximum channel amplitude measurement to the minimum channel amplitude measurement ratio. The maximum channel to minimum channel ratio must not exceed 1.38.

(e) Monitor the THS test point and check for level within 41% to 45% of the calculated positive peak average. If not within the limits, adjust R228 until the level is 43% of the calculated positive peak average.

(f) Rewind the tape (program **30**) and run diagnostic programs **9** (high speed) and **62**. Repeat steps (c)-(e) and adjust R229.

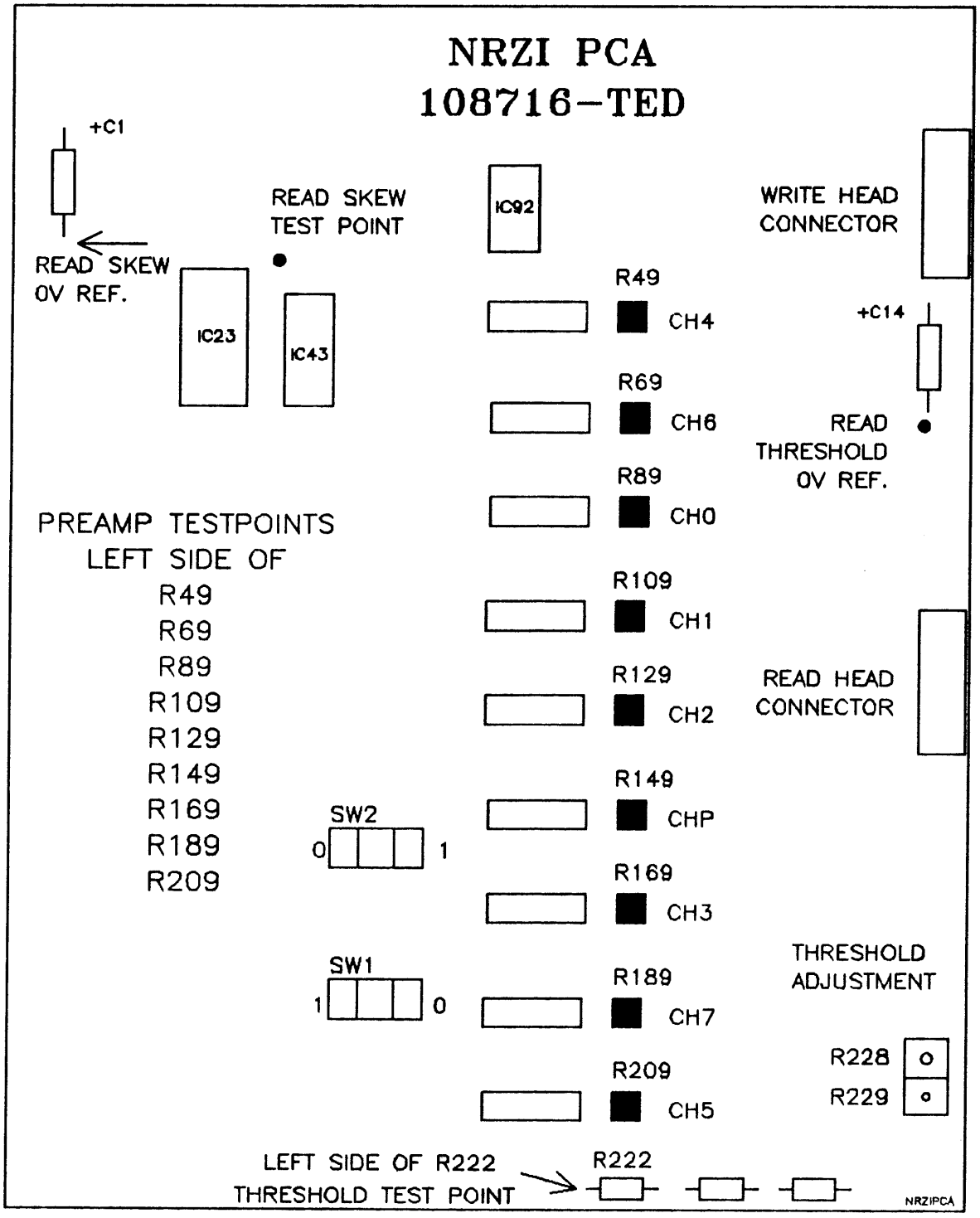


Figure 5-8 NRZI Board Test Points

5.5 DESKEW

The deskew adjustment is actually a mechanical adjustment, however it is performed to correct an electrical problem. The adjustment procedure is a two pass operation. The first pass establishes (and corrects if necessary) the read stack skew. The second pass verifies the composite skew characteristic of the combined read and write stacks.

5.5.1 Read Deskew Check

(a) Move the Data Formatter to the left card cage slot.

(b) Remove the head covers and load a master skew tape.

(c) Run diagnostic program **63** (read forward low speed).

(d) Connect channel A of the oscilloscope to Channel 2 TP (ground to 0V TP). Refer to Fig. 5-7.

(e) Adjust the scope trace so that the positive going signal crosses in the center of the screen. Refer to Fig. 5-9.

(f) Set the scope as follows:

Channel A and B sensitivity to 200-800 mV (set for best triggering)
Timebase to 1 microsecond/cm

(g) Monitor and record the deviation (left or right of center) the tape channels in the following sequence:
4, 6, 0, 1, P, 3, 7, 5.

(h) Add the highest value from the left and the right and let the sum represent "S". *NOTE: This equals total read head skew.* If "S" is less than 3 microseconds, no adjustment is necessary. Proceed to Section 5.5.3 to check the composite read/write skew.

(i) If "S" is greater than 3 microseconds, the head must be shimmed. Run program 65 to return tape to load point. Head shimming is accomplished by adjusting the height of the upper (leading) guide. *The lower (trailing) guide must never be changed from it's designed setting.*

NOTE

1. If tape channels 4, 6, 0, 1, generally lead (to the left of reference) and tape channels P, 3, 7, 5, generally lag (to the right of reference); **INCREASE** the leading guide shim.

2. If tape channels 4, 6, 0, 1, generally lag (to the right of reference) and tape channels P, 3, 7, 5, generally lead (to the left of reference); **DECREASE** the leading guide shim.

(j) Using "D", in seconds, as the difference between "S" in steps (h-i), and the nominal 3 microseconds compute: 10 x tape speed (ips) x D (seconds) = shim increment in inches.

NOTE

1. A shim increment of .0005 inch corresponds with approximately 50 micro-inches of effective skew.

2. The leading guide shimming must not be adjusted by more than +/-0.0025 inch. If the shim increment required is greater than 0.0025 inch increment by 0.0025 inch. If the shim increment required is less than 0.0025 inch, increment to the nearest 0.0005 inch.

(m) Insert the amount of shim required in step (l), as detailed in Fig. 4-4.

(n) After replacing the shims, recheck the head skew.

5.5.2 Example

Skew measurements for the nine tape channels (Channel 2 is reference.)

Channel	4	6	0	1	2	P	3	7	5
Microsec.	+2.5	+3.0	+1.0	+1.5	0	-1.0	-2.0	-3.5	-3.0

```
"S"     = 3.0 (Chan. 6) + 3.5 (Chan. 7)
        = 6.5 microseconds
 For 50 ips machines; "D" + 6.5 - 3 = 3.5 microseconds

 Required shim adjustment is, therefore;

 10 x 50 x 3.5/10*6
        = 0.00125
        = 0.0015 actual shim  (nearest .0005 increment)
```

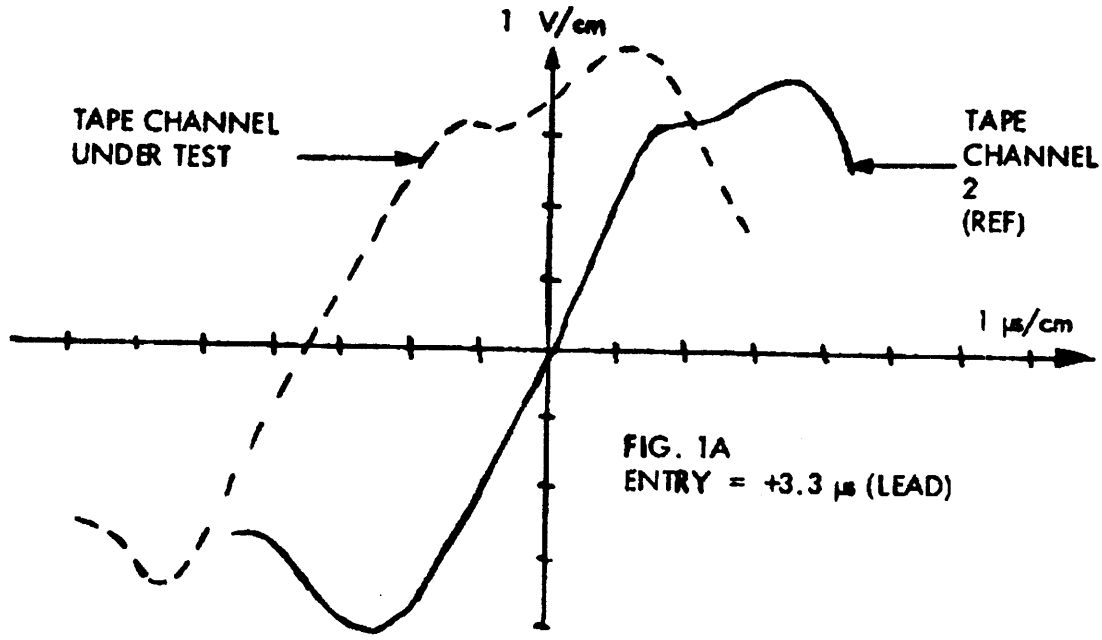
Since tape channels 4, 6, 0, 1, generally lead channel 2, and tape channels P, 3, 7, 5, generally lag channel 2 the leading guide shim must be increased by 0.0015 in, to 0.0065 in. This can be accomplished by removing the standard 0.005 inch shim and replacing it with a 0.004 and a 0.0025 inch shims.

5.5.3 Composite Read/Write Skew Check

(a) Load a scratch tape.

(b) Run diagnostic program **10** (low speed) followed by program **61** (Write alt. 1s and 0s).

(c) Recheck the channel skew spread (Section 5.5.1). Check that the total "S" does not exceed 6.3 microseconds.



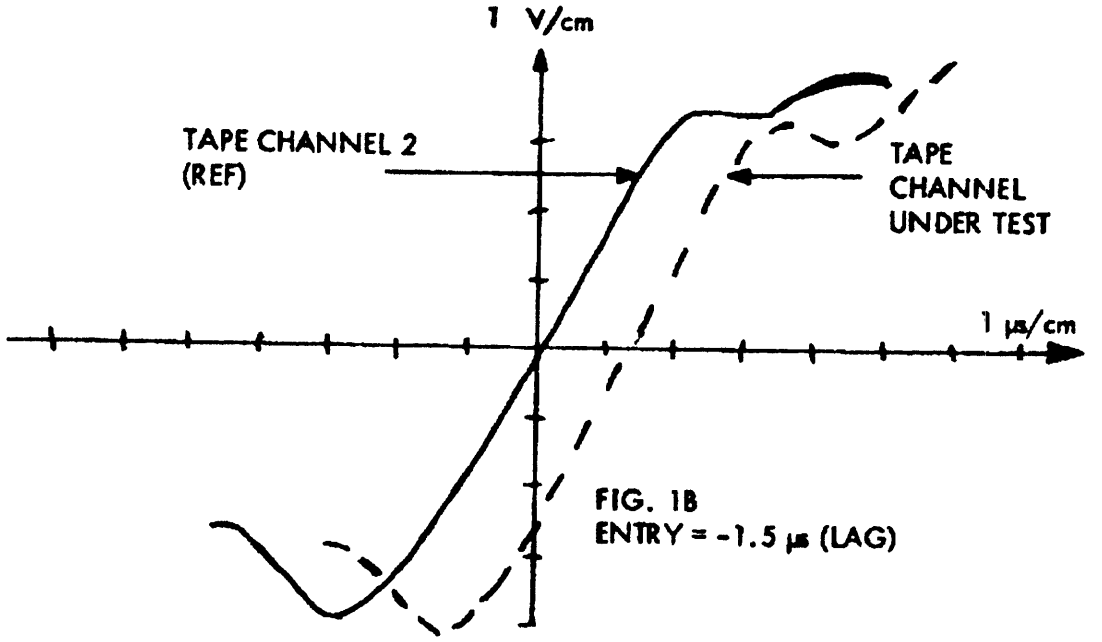


Figure 5-9 Read Deskew Waveform

This page intentionally left blank.

CONTENTS: SECTION VIII

---FIGURES---

This page intentionally left blank.

TROUBLESHOOTING AND DIAGNOSTICS

SECTION VIII

[1] APPROACH

The HP 7974A comes equipped extensive internal diagnostic programs designed to identify equipment malfunctions and isolate component failures. There are two diagnostic program groups: "100 Level" and "200 Level". The 100 Level programs are stored in the Master Controller and may be accessed by the host system or by operating the front panel. These programs check the operation of the ICU and general operations of the transport. The 200 Level diagnostic programs are stored in the Control/Mother board and are only accessible by operating the front panel. These programs isolate the transport mechanisms from the ICU operations to allow indepth testing. Both the 100 and 200 Level tests and their operations are explained more fully in Sections [2] and [3].

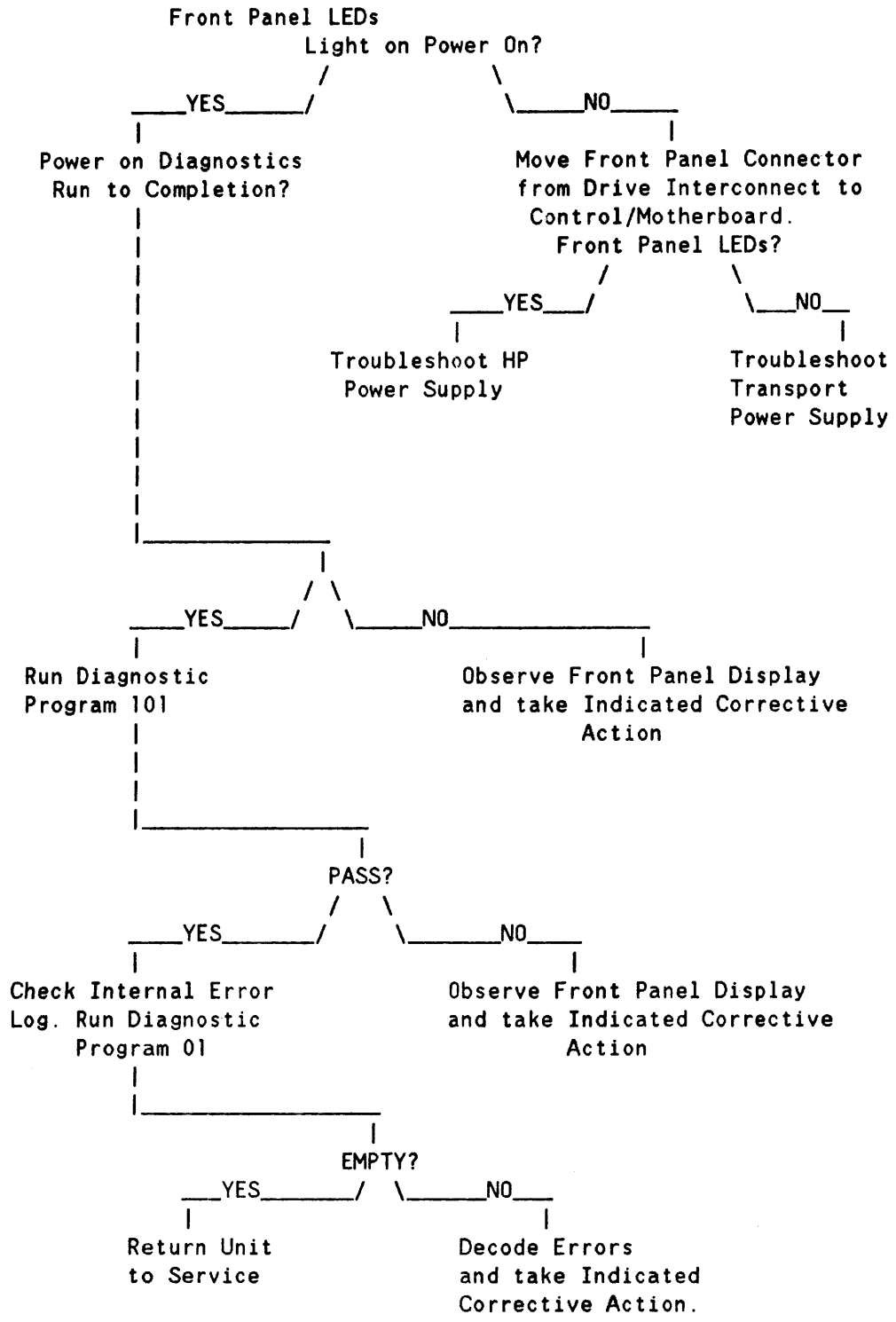
When the drive malfunctions, there are two 100 level programs you will be relying on to help you track down the problem. Figure 1-1 illustrates the overall method you should use. The first is the power-on selftest, program 5. It is initiated whenever the power is toggled and is designed to test the unit's electronics system. Because the testing is done without tape motion, approximately 75%-80% of the drive's operation are checked by the power-on selftest. When the selftest does not indicate an error, diagnostic 101 should be executed to test the tape motion circuitry.

If a failure occurs during either of these tests (5 and 101), the front panel displays a 100 Level error code which indicates the type of failure and possible causes. Armed with this knowledge, you then select either 100 or 200 Level diagnostic programs designed to check the questionable FRUs/operations individually. Continue to execute test after test until the fault is isolated. Once you've isolated the fault and made an appropriate adjustment/replacement to correct the problem, check your work by first testing corrections individually and then by executing programs 5 and 101 to ensure the drive is functioning properly.

CAUTION

Diagnostic tests which require the use of a write-enabled work tape are highlighted within the program descriptions. Many of these tests write to tape and destroy existing data. To be on the safe side, always use a known good tape that does not have any important information on it. Do not use an old or worn tape for these tests because they will introduce soft-error problems during read/write operations.

Figure 1-1 TROUBLESHOOTING FLOW CHART



[2] 100 LEVEL: HOST-AVAILABLE

2.1 Theory

The 100 Level diagnostic programs are immediately available when you enter "Diagnostics Mode". You might think of them as "outer level" diagnostics because they are stored in the Master Controller. Since the Master Controller communicates with the host, it allows the "outside world" to control these functions. In our case, the outside world includes an operator using the front panel or the host computer talking to the Master Controller.

Tests 0-100 deal mostly with the ICU and keeping track of important parameters such as the current Error Log or Firmware Revision Code. Tests 101-198 deal mainly with read/write and tape movement operations. They are identical to the 200 Level tests 01-98. However, by making these tests (101-198) available through the 100 Level, more extensive error information may be obtained.

2.2 Operating Sequence

(a) Make sure the drive is offline. Press **OFFLINE RESET** if the **ONLINE** indicator is lit.

CAUTION

Pressing **RESET** twice in a row causes a hard reset to occur. A hard reset initializes the system in as if the power were turned off. In particular, it will clear the Error Log and "forget" that a tape is loaded on the transport.

(b) Refer to Section 2.4 and find the test needed. If a tape must be loaded, do so.

(c) Press the **DIAGNOSTICS** button. The diagnostics mode indicator should light and the display should read **00**. If not, repeat step a.

(d) Press the **Units** button and hold it down until the desired units digit (0-9) appears.

(e) Press the **Tens** button and hold it down until the correct tens/hundreds digit appears (00-10-20-... 200).

The **Tens** and **Units** buttons are designed to continuously cycle at a rate of two digits per second. To speed up the display, hold the **Fast** button when pressing either button.

(f) Press **Enter** to execute the test.

A test may be repeated after either a pass or failure by pressing the **Enter** button again.

A running diagnostic test may be terminated by pressing the **Enter** button. When it is pressed, the diagnostic currently running terminates and the display shows only the selected test number. The diagnostics mode is still active and the test may be redone or another test may be selected.

If the **DIAGNOSTICS** button is pressed while in the diagnostics mode, the diagnostics mode is exited.

2.3 Error Code Interpretation

On completion of a test, either a pass designation, **Pxxx** (xxx: Test number that passed), or a five-part failure code sequence will appear and cycle continuously until the **Enter** button is pressed. Here is an example:

DISPLAY:	MEANING:
F00	- Failed Test 00
FRU	- Field Replaceable Unit (FRU) code is next
0087	- 8: FRU which failed
	7: Subassembly in FRU which failed
CODE	- Cause of failure next
0002	- 0: Action during test which caused failure
	2: Other FRUs or subassemblies that should be tested (Multi-test code), listed in order of probability

The error codes in Section 2.5 are made up of the 4 digits in the FRU and CODE sequence. Therefore, to determine the meaning of the code in the above example you would look up 8702 to find the interpretation.

FRU in error.	Subassembly within FRU in error.	The action which caused the failure.	The Multi-test code.

Figure 2-1 Diagnostic Error Messages

Figure 2-2 100-Level Diagnostic Programs

0 Error Message
1 Error Log
2 Clear Error Log
3 Not Used
4 Not Used
5 Power-on Selftest
6 Master Controller Board
7 Alphanumeric Display
8 Master Controller RAM
9 Master Controller Timer
10 Master Controller EEPROM
11 Data Buffer
12 Not Used
13 HP-IB Internal Loop
14 HP-IB External Loop
15-18 Not Used
19 EEPROM Cell
20 Front Panel Buttons
21-24 Not Used
25 Single Execution Mode
26 Infinite Execution Mode
27 Firmware Revision Code
28 Tape Usage Odometer
29 Tape Format
30 Firmware Update
31-49 Not Used
50 Drive Report
51-99 Not Used
100 Drive Interconnect Board
101 Diagnostic Workout
102 Not Used
103 Data Channel Verification
104 Servo Electronics and Mechanics
105 Capstan Test
106 Forward and Reverse Speed Ratio
107 Read Error Detection
108 Write/Read Test
109 Select High-speed Mode
110 Select Low-speed Mode
111-112 Not Used
113 Worst Case Data Pattern
114 Normal Data Pattern
115-116 Not Used
117 Write/Backspace/Read Data Check
118 Write Short Records (Start/Stop)
119 Write Long Records (Start/Stop)
120 Not Used
121 Write Long Records (Streaming)
122 Not Used
123 Repositioning Ramps Test
124 Test Error Detection Circuitry
125 Not Used
126 Clear Sense Byte Registers
127 NRZI Select
128 PE Select
129 Not Used
130 Rewind Tape
131-171 Not Used
172 Write/Check File Mark **
173-197 Not Used
198 Clear Program Stack **
200 Isolate Transport

**Not available from the front panel

2.4 Program Descriptions

Test 0 -- Error Message

Displays the most recent diagnostic error message.

Test 1 -- Error Log

Displays the diagnostic error log. The error log contains the last 10 error messages. The most recent error will be displayed first. Subsequent entries will be displayed each time the **Enter** button is pressed until all errors in the log have been displayed. The error log clears when the power is turned off.

Test 2 -- Clear Error Log

Clears the diagnostic error log.

Test 5 -- Power-On Selftest

The following tests are called in sequence:
6, 2, 7, 10, 11, 13, 14, 50, and 100.

NOTE

This diagnostic takes approximately 30 seconds to run. If the door is open, the selftest will hang. Close the door to complete the diagnostic.

Test 6 -- Master Controller Board Test

Checks the ROM and CPU. After completing those tasks, it calls tests 8 and 9 to finish testing the Master Controller Board (MCB).

Test 7 -- Alphanumeric Display Test

The digits are cycled through 0000...9999 and ****. The indicators are also lit one at a time. This is a good test to use if you suspect that any of the display lights aren't working.

Test 8 -- Master Controller RAM Test

A series of data bytes are written to RAM and verified.

Test 9 -- Master Controller Timer Test

The MCB's counters/timers are checked.

Test 10 -- Master Controller EEPROM Test

The EEPROM chips on the MCB are verified to be correct by reading some predefined addresses containing constant values, and performing a checksum.

Test 11 -- Data Buffer Test

Checks the data buffer's functionality by writing a set of data bytes to each buffer address and then verifying them.

Test 13 -- HP-IB Internal Loop Test

Checks the HP-IB board functions.

Test 14 -- HP-IB External Loop Test

This test verifies the HP-IB/Master Controller and the HP-IB/Data Buffer interfaces.

Test 19 -- EEPROM Cell Test

A test word is written into the Electrical Eraseable Programmable Read Only Memory (EEPROM) to determine if a cell is worn out, not working, or +12 volts are not available to the EEPROM chips. The test may be used a maximum of 20,000 times before cell wearout will occur. Therefore, this test cannot be used in the infinite execution mode.

Test 20 -- Front Panel Button Test

Use this test when you suspect a button is not functioning correctly. Pressing any button will display a button name to indicate the button is working. When the door is opened **DOOR** will be displayed. Press **REWIND** and **ADDRESS** simultaneously to exit this program.

Test 25 -- Single Execution Mode.

Sets the local looping environment to single test execution. Use it after executing Test 26.

Test 26 -- Infinite Execution Mode.

Use this utility to set the local looping environment to infinite execution. After entering Test 26, select the test you wish to execute repeatedly. The test will repeat until the **RESET** button is held down. The button must be pressed until **DONE"** appears in the display. Another test may be selected at this time. If an executing test fails, an FRU code sequence is displayed until the test is terminated by **Enter**. To re-enter single execution mode, execute test 25.

Test 27 -- Firmware Revision Code

This utility displays the current Master Controller firmware revision number. It will remain on the display until **Enter** is pressed or five seconds have elapsed.

Test 28 -- Tape Usage Odometer

Displays the current odometer value. The odometer increments by one after 20,000 ft. of tape (approximately nine 2,400 ft. reels) passes the read/write head. The odometer information is presented in two hexadecimal digits. The first is the most-significant-digit (MSD) and the second is the least-significant-digit (LSD). To calculate the footage, convert the odometer reading to its decimal equivalent and multiply by 20,000.

xxxx (MSD)	xxxx (LSD)

Test 29 -- Tape Format

Displays the tape densities supported by the drive. The messages **1600** or **1600** followed by **800** will appear until **Enter** is pressed.

Test 30 --Firmware Update

Firmware Update utility program. See Section III (Installation and Configuration) for instructions on use.

Test 50 -- Drive Report

The ICU verifies that the drive electronics are functional by polling the results of the transport's internal selftest (**01**).

Test 100 -- Drive Interconnect Board

It is used to verify that the board is able to communicate with the Drive Controller Board.

Test 101 -- Diagnostic Workout Program

A write-enabled work tape must be mounted. The diagnostic calls the following tests to exercise most of the functions of the tape drive (shown in order):

103,104,106,110,107,108,124,117,109,107,
124,117,168,172,130,198.

However, only the message **R101** is displayed during execution. This program should be run if the drive is suspected to be defective or for periodic performance checks.

Test 103 -- Data Channel Verification Test

This diagnostic verifies that both the Data Formatter and Read Logic boards are present.

Test 104 -- Servo Electronics and Mechanics Test

A write-enabled work tape must be mounted. The servo motors and their mechanical parts are tested by moving the tape backwards and forwards with a decreasing period.

Test 105 -- Capstan Test

A write-enabled work tape must be mounted. This diagnostic is incorporated as part of the selftest to discover if there is any tape slip on the capstan or if the servo speeds are incorrect.

Test 106 --Forward and Reverse Speed Ratio

A write-enabled work tape must be mounted. This diagnostic checks that the tape lengths of the forward streaming speed and the reverse non-streaming speed are in the correct ratio by running through the following sequence: a) The drive rewinds a work tape to BOT, b) runs it forward for 25.4 m and stops, c) runs it in reverse for 25.15 m, and d) searches for BOT. If BOT is found in the next 51 cm of tape, the test passes.

Test 107 -- Read Error Detection Test

A write-enabled work tape must be mounted. A variety of "random" error conditions are written to the tape and then read back. If the errors are recognized, the test passes.

Test 108 -- Write/Read Test

A write-enabled work tape must be mounted. "Good" data is written to tape and then read back. If the transfer is correct, the test passes.

Test 109 -- Select High-speed Mode

Enables the operator or host computer to set the drive to the high-speed mode. This is done prior to starting other programs.

Test 110 -- Select Low-speed Mode

Enables the operator or host computer to set the drive to the low-speed mode. This is done prior to starting other programs.

Test 113 -- Worst Case Data Pattern

The data pattern below is used to test the error detection circuitry at power up. You may select this pattern before starting programs 118 to 121.

```
0 1 1 0 0 1 1 1 0
```

Test 114 -- Normal Data Pattern

A repetitive sequence of 16 bytes, representing "random" data is used to test the error detection circuitry at power up. You may select this pattern before starting programs 118 to 121.

Test 117 -- Write/Backspace/Read Data Check

A write-enabled work tape must be mounted. Writes 256 records of the worst case data, backs up to the beginning of the data, and reads the records. Status errors are interrogated when writing; status and data are checked when reading.

Test 118 -- Write Short Records (Start/Stop)

A write-enabled work tape must be mounted. The test is performed in the start/stop mode. Writes 256 long records of formatted data. The data pattern is selected by either program 113 or 114. If program 110 (Select Low-speed Mode) has been selected, records are written at low speed. If program 109 (Select High-speed Mode) has been selected, records are written at high speed.

Test 119 -- Write Long Records (Start/Stop)

A write-enabled work tape must be mounted. The test is performed in the start/stop mode. Writes 256 long records of formatted data. The data pattern is selected by either program 113 or 114. If program 110 (Select Low-speed Mode) has been selected, records are written at low speed. If program 109 (Select High-speed Mode) has been selected, records are written at high speed.

Test 121 -- Write Long Records (Streaming mode)

A write-enabled work tape must be mounted. The test is performed in the streaming mode. It writes 256 long records of formatted data and the data pattern is established by either program 113 or 114. If program 110 (Select Low-speed Mode) has been selected, records are written at low speed. If program 109 (Select High-speed Mode) has been selected, records are written at high speed.

Test 123 -- Repositioning Ramps Test

A write-enabled work tape must be mounted. The drive rewinds the tape, then runs it forward and erases any data. A short record is written, the tape rewound, and then run forward and read at high speed. When the trailing edge of the record is detected, the tape is ramped to a halt. The tape is then run in reverse at low speed and the time taken to detect the trailing edge of the record is measured.

Test 124 -- Test Error Detection Circuitry

A write-enabled work tape must be mounted. This test is a tape motion version of test 107.

Test 126 -- Clear Sense Byte Registers

The sense byte registers are used by the host to monitor errors during normal operation. There is usually no need to clear these registers.

Test 127 -- NRZI Select

Selects NRZI read/write format for diagnostic tests. Execute program 128 to return to normal PE mode.

Test 128 -- PE Select

Selects PE read/write format for diagnostic tests.

Test 130 -- Rewind Tape

Rewinds a tape to BOT. This program may be used for positioning the tape while in the diagnostics mode.

NOTE

Tests 172 and 198 are available only as part of the diagnostic workout program 101. They are not accessible from the front panel.

Test 172 -- Write/Check File Mark

A write-enabled work tape must be mounted. The drive writes a File Mark to tape and checks that the status lines indicate a File Mark has been written.

Test 198 -- Clear Program Stack

Clears the current program stack.

Test 200 -- Isolate Transport

Allows access to the transport diagnostics contained in the Control/Mother board. See Section [3].

2.5 Error Codes

1____ Servo and Tape Motion Assembly

11___ Capstan motor and tachometer subassembly

110x The low speed ramps were too long.

111x The low speed ramps were too short.

112x The high speed ramps were too long.

113x The high speed ramps were too short.

12___ Tape motion mechanical assembly

121x Low speed servo failure.

122x High speed servo failure.

x: Multi-test codes

0 Multi-test code does not apply

1 speed adjustment, capstan assembly, power supply overload, mechanical guides and rollers.

2 mechanical rollers/guides/arms, capstan assembly, Control Board servo circuits, power supply overload, speed adjustments.

2____ NRZI Board

21yx NRZI parity circuitry failed

22yx NRZI LRC circuitry failed

23yx NRZI CRC circuitry failed

24yx Not Used

25yx No head current detected

26yx Identify status circuitry failed

27yx EOF detection circuitry failed

28yx Block valid signal timed out in test

29yx Block valid signal too long

2Ayx Failure during self-test

y: Actions that detected the failure.

0 Does not apply

1 Fixed data pattern

2 Random data pattern

3 Occurred during a write test only.

4 Occurred during a read test only.

5 No board installed or connector disconnected.

x: Multi-test codes

0 Does not apply

1 NRZI board

2 NRZI board, head connectors, head

3 NRZI board, tape, head

4 Connector missing, board missing, or power fail

4____ Master Controller Assembly

41___ CPU error on Master Controller assembly.

4110 CPU data register malfunction. The data value written was not the value read while verifying.

4120 CPU address register malfunction. The data value written was not the value read while verifying.

4130 CPU condition code malfunction.

4140 A CPU register had its data fade after a two second wait.

4160 CPU addressing malfunction.

42___ Master Controller RAM failure.

4210 March test failure.

4220 Selective one walking bit test failure.

4230 Selective zero walking bit test failure.

43___ Master Controller Data Buffer subassembly failure.

4300 Data Buffer is unresponsive.

4310 RAM failure in marching RAM test.

4320 Register failure in walking '1' bit test.

4330 Register failure in walking '0' bit test.

4340 Length counter/USM function failure.

4350 Usage counter/USM function failure.

4360 Parity/USM function failure.

4370 Data transferred not the data received.

4380 Transferred data missing an EOR.

4390 Data Buffer has incorrect pre-fetch status.

44___ Master Controller timer chip subassembly failure.

4410 Timer interrupt status error.

4420 Timer interrupt status could not be cleared.

4430 Timer 1 didn't count down to zero.

4440 Timer 1 or timer 2 is substantially faster than the other timer.

4450 Timer 1 or timer 2 is substantially slower than the other timer.

4460 Timer 1 or timer 3 is substantially faster than the other timer.

4470 Timer 1 or timer 3 is substantially slower than the other timer.

45___ Master Controller EEPROM chip subassembly failure.

4510 The read/write ready status was not present.

4520 The computed EEPROM check sum was not the same as the stored check sum.

4530 An EEPROM read value was incorrectly read.

4540 A write value into the EEPROM did not verify after write.

4550 The computed EEPROM check sum did not verify after being written.

4560 EEPROM is write enabled and should not be.

4570 EEPROM is not write enabled and should be.

4600 ROM checksum error

5____ Data formatter board

51yx Preamble circuit failure.

52yx Postable circuit failure.

53yx MTE circuit failure.

54yx Skew circuit failure.

55yx Vertical parity error circuit failure.

56yx Corrected error circuit failure.

57yx Data error.

5802 No head current detected.

5803 No block signal detected.

5Ayx Error encountered during selftest.

5Fyx No data formatter board detected.

y: Actions that detected the failure.

0 Action codes do not apply

1 Fixed data pattern.

2 Random data pattern.

3 Occurred during a write test only.

4 Occurred during a read test only.

5 Power fail,no board,no connector, connectors loose

x: multi-test codes

0 Multi-test code does not apply

1 Data Formatter board, Digital Read Logic board.

2 Data Formatter board, heads.

3 Digital Read Logic board, Data Formatter Board, tape, heads

4 Connectors loose, board missing, power supply problems

6_____ HP Interface Bus (HP-IB) Assembly

61___ HP-IB failure.

6100 HP-IB is unresponsive.

6110 The inbound FIFO was not empty after an attempt to clear.

6120 The internal HP-IB loopback has failed.

6130 The "end" bit in the interface is not functional.

62___ HP-IB/Master Controller interface failure.

6210 The data transferred was not received.

6220 The data transferred was missing an EOI.

7_____ Drive Interconnect Board

710x Data transfer module assembly.

711x Reset interface test error.

712x Write interface test error.

713x Read interface test error.

714x Sense byte test error.

715x Door opened during test.

716x Sense byte transfer test failure.

717x Sense byte value not returned correctly.

720x Front panel module failure

721x Virtual display circuit failure.

722x Virtual button circuit failure.

730x Command status module failure

731x Failure occured when sending diagnostic command to transport.

732x Sense byte handshake test failure.

x: Multi-test codes

0 Multi-test code does not apply

1 Cables, Drive Interconnect board, Control/Mother board

2 Cables, Drive Interconnect board

3 Cable, Drive Interconnect board, or Control/Mother board

4 (not used)

5 Cables, Drive Interconnect board, Data/Formatter board, Control/Mother board

6 Drive Interconnect board or Control/Mother board

8_____ Digital Read Electronics Board

81yx Corrected error circuit failure.

82yx False postamble detection circuit failure.

83yx Multiple track error circuit failure.

84yx Vertical parity error circuit failure.

85yx Read oscillator circuit failure.

86yx No ID status during an identify.

87yx No EOF status detected while trying to write a file mark.

88yx Block valid signal timed out during test.

89yx Block valid signal lasted longer than expected.

8A00 Error encountered during selftest.

8Byx No ID mark detected in a write from BOT.

8Cyx GAP found in ID mark.

8F00 The hardware is not present or responsive.

y: Actions that detected the failure.

0 Does not apply

1 Fixed data pattern.

2 Random data pattern.

3 Occurred during a write test only.

4 Occurred during a read test only.

5 No board installed or connector disconnected test

x: multi-test codes

0 Multi-test code does not apply

1 Digital read logic board, Data formatter board, Tape, Heads.

2 Digital read logic board, Data formatter board, Heads, Tape.

9_____ Head/Tape Interface Assembly

91yx False preamble detected.

92yx False postamble detected.

93yx Multiple tracks in error were detected.

94yx Skew error was detected.

95yx Vertical parity error was detected.

96yx Corrected error was detected.

97yx Data error detected in read test.

y: Actions that detected the failure.

0 Does not apply

1 Fixed data pattern.

2 Random data pattern.

3 Occurred during a write test only.

4 Occurred during a read test only.

5 No board installed or connector disconnected test

x: multi-test codes

0 Multi-test code does not apply

1 Tape, Heads, Read logic board, Data formatter board.

A_____ Drive Controller/Mother Board

A10x Servo forward speed slow or reverse speed fast.

A11x Servo forward speed fast or reverse speed slow.

A12x Servo high speed ramp too short or low speed ramp too long.

A13x Servo high speed ramp too long or low speed ramp too short.

A14x Repositions close to limit. Check speed adjustment.

A15x Repositions beyond limit. Check speed adjustment.

A20x The RAM circuits failed RAM tests.

A30x Loose connections detected.

A40x The power supply (not 5V) failed test.

A50x The ROMS failed checksum test.

A60x Either the data formatter or digital read board not inserted.

A71x Drive failed to enter NRZI density.

A72X Drive failed to enter PE density.

x: multi-test codes

0 Multi-test code does not apply

1 speed adjustment, Control Board circuits, capstan assembly, power supply overload, mechanical arms and guide assemblies.

B_____ Unexpected Exceptions

The MC68000 Central Processing Unit (CPU) is capable of responding to a number of unexpected conditions which rarely occur in the HP 7974A. If one of these errors is detected by the CPU, a hardware or firmware error is indicated. The drive will respond by shutting itself down and displaying the error code.

B100 Address error.

B200 Illegal instruction.

B300 Divide by zero.

B400 Register bounds violation.

B500 Overflow.

B600 Privilege violation.

B700 Trace exception.

B800 Emulation of future instruction.

B900 Spurious interrupt.

BA00 Unimplemented interrupt.

BB00 Unassigned vector.

Bus Error Exceptions

A Bus Error will occur whenever the Master Controller accesses subsystems which do not respond within an allowable amount of time. Since the error can occur during a CPU instruction, the drive is shut down immediately to prevent the Master Controller from executing unpredictably. These errors usually indicate a failure in the ICU: HP-IB, Master Controller or Drive Interconnect boards.

4300 The Master Controller Data Buffer subassembly is unresponsive.

6100 The HP-IB is unresponsive.

DTAK Master Controller did not recieve DaTa AcKnowledge.

D_____ Runtime-Detected errors

Run-time errors prevent the execution or completion of a diagnostic program. Errors D310, D330, D370, and D380 can be corrected by the operator and are the most commonly displayed sequences. All run-time errors are logged in the Error Log. If a fatal error occurs, test 1 (Display Error Log) and test 5 (Power-on Selftest) should be run for more detail.

D000 Operating System detected failure.

D100 Channel Program detected failure.

D177 Transaction ID mismatch.

D17A Missing PND command.

D17B Report Queue error.

D17C Report Queue full.

D17D Unknown command to device program.

D17E Full command Queue.

D183 Data buffer byte count mismatch.

D184 Bad message type.

D185 Processor handshake abort.

D186 Interface exception.

D187 Outbound data freeze.

D188 Inbound fifo error.

D189 EEPROM update failure.

D18A Device firmware error

D18B Hardware utility firmware error.

D18C Channel case error.

D200 Device Program detected failure.

D201 No data busy detected when expected in a command handshake.

D202 Data busy remained asserted when it should have deasserted.

D203 A polling loop terminated early.

D204 Unexpected status returned from the transport.

D205 Device write protected or failure to go online.

D206 Formatter busy did not assert upon receipt of a command.

D207 The HP interface board did not initialize correctly.

D208 The rewind command handshake failed.

D209 Load point was not detected when expected.

D20A Transport failed to be put in the intended density.

D20B Formatter busy remained asserted when it should have deasserted.

D20C Transport encountered an unrecognized command.

D20D A reposition took longer than expected. Speed adjustment required.

D20E Erase current not detected in head.

D20F A command was rejected by the transport.

D210 The sense bytes were lost when a sense byte read was attempted

D211 Power was lost partially or totally during the last operation.

D212 The door was open during a command.

D213 The transport failed to complete a command.

D214 Formatter busy was asserted too long during a sense byte read.

D215 Position was lost during retries.

D216 Online failure.

D22D Multiple track error.

D22F Gap in ID.

D231 ID found in read.

D233 Gap in block found.

D237 Door open error.

D239 Skew error.

D23A False preamble/postamble

D23B Corrected write error.

D253 Servo shutdown error.

D268 Erase failure.

D269 No read after write detected.

D26B Hardware failure.

D26C Timeout error.

D277 Transaction ID mismatch.

D27A Missing PND command.

D27B Report Queue error.

D27C Report Queue full.

D27D Unknown command to device program.

D27E Full command Queue.

D280 Missing EOR in data buffer.

D283 False EOR in data buffer.

D284 Bad message type.

D285 Processor handshake abort.

D286 Interface exception.

D287 Outbound data freeze.

D288 Inbound fifo error.

D289 EEPROM update failure.

D28A Device firmware error.

D28B Hardware utility firmware error.

D28C Channel case error.

D300 Diagnostic Program detected failure.

D310 No tape was loaded when a read or write diagnostic test was selected.

D320 Wrong density.

D330 No write ring was installed when a write test selected.

D340 A tape-related error has occurred during a local firmware update.

D350 A valid firmware update record was not found on the loaded tape.

D360 The EEPROM READY signal did not come true during a Tape Usage Odometer update.

D370 Door opened while running test.

D380 BOT/EOT was detected abnormally during a diagnostic operation.

D3F0 An unknown failure code was received from the transport.

D3F1 The user pressed the enter button during a test.

D3FF The selftest was terminated early.

E_____ Host Protocol Errors

E0A1 Command Queue not empty.

E0A2	Request DSJ expected.	E0B0	End complete expected.
E0A3	Request status expected	E0B2	End data expected.
E0A7	Data byte expected.	E0B4	Improper secondary.
E0A8	Missing EOI on data byte.	E0B8	Loopback protocol error.
E0AA	Command phase protocol error.	E0B9	Selftest protocol error.
E0AC	Read protocol error.	E0BC	Command parity error.
E0AD	Report phase protocol error.	E0BD	Reset by operator.
E0AE	Cold load protocol error.	E0BE	Device clear.

[3] 200 LEVEL: INTERNAL

3.1 Theory

The 200 Level transport diagnostics provide a soft* method of bypassing the ICU portion of the tape drive in order to isolate transport malfunctions. All 200 Level code is maintained in the Control/Mother board. Since the Master Controller is not used in this mode, these diagnostics are not available to the host and can only be run via the front panel.

3.2 Operating Sequence

In the transport diagnostic mode the description/function of three front panel buttons have been redefined as follows:

100 LEVEL	200 LEVEL
Rewind-Fast	Rewind-Enter (Fast)
Reset-Enter	Reset-Run/Stop
Address	Density

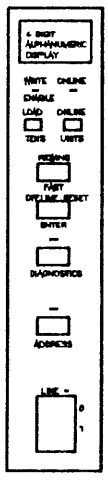


Figure 3-1 Front Panel

*The ICU can also be bypassed by disconnecting the front panel from the Drive Interconnect board and connecting it directly to the Control/Mother board. The diagnostic operation then begins at Step (d) of Section 3.2.

(a) Make sure the drive is offline. Press **OFFLINE RESET** if the **ONLINE** indicator is lit.

CAUTION

Pressing **RESET** twice in a row causes a hard reset to occur. A hard reset initializes the system in as if the power were turned off. In particular, it will clear the Error Log and "forget" that a tape is loaded on the transport.

(b) Press the **DIAGNOSTICS** button. The diagnostics mode indicator should light and the display should read **00**. If not, repeat step a.

(c) Select program 200 using the **Tens** and **Units** buttons. The display should indicate **00**.

NOTE

The **Tens** and **Units** buttons are designed to continuously cycle at a rate of two digits per second. To speed up the display, hold the **Fast** button when pressing either button.

(d) Refer to Figure 3-2 to find the test needed. If a tape must be loaded, do so.

(f) Press **Run/Stop** to execute the test.

The **Run/Stop** function is used to stop an executing program and resume execution of a halted program. When a program is stopped by this button, pressing it again will either restart the program from the beginning or, if a stack is executing, it will start the next program in the stack.

The **Enter** function is used to enter programs into the operator stack (program 97).

If the **DIAGNOSTICS** button is pressed while in the diagnostics mode, the diagnostics mode is exited.

Figure 3-2 200-Level Diagnostic Programs

0 Program enter point	50 Step FWD (Low Speed)
1 Auto program sequencer	51 Step REV (Low Speed)
2 Not Used	52 Alternate (Low Speed)
3 PE data channel present	53 Step FWD (High Speed)
4 Servo test	54 Not Used
5 Capstan test	55 Not Used
6 FWD/REV speed comparison	56 Not Used
7 Test error circuit (non cor)	57 Not Used
8 Write/Read test (non cor)	58 Not Used
9 Select high speed	59 Not Used
10 Select low speed	60 Erase to EOT
11 Set "n"	61 Write alternate 1 & 0 to EOT
12 Transport Only Selftest	62 Write all 1's to EOT
13 Select fixed data (default)	63 Read FWD to EOT (Low Speed)
14 Select random data	64 Rd FWD (Hi Speed-strobe on)
15 Fail Skip	65 Rd REV (Low speed-strobe on)
16 Not Used	66 Not Used
17 Write/back-space/read check	67 Not Used
18 Write "n" short records S/S	68 Write/Check ident
19 Write "n" long records S/S	69 Not Used
20 Write "n" short records STR	70 Space FWD "n" records
21 Write "n" long records STR	71 Space REV "n" records (low spd)
22 Not Used	72 Write/Check EOF
23 Repositioning test	73 Read FWD "n" records
24 Test error detection	74 Read REV "n" records (low spd)
25 Not Used	75 Not Used
26 Clear sense bytes	76 Not Used
27 Select NRZ	77 Not Used
28 Select PE	78 Not Used
29 Not Used	79 Not Used
30 Rewind	80 Not Used
31 Not Used	81 Not Used
32 Not Used	82 NRZ read skew test
33 Not Used	83 NRZ write skew test
34 Not Used	84 Not Used
35 Not Used	85 Not Used
36 Sensors test	86 Not Used
37 File protect test	87 Not Used
38 Not Used	88 Not Used
39 Not Used	89 Not Used
40 Display firmware rev. no.	90 Not Used
41 Display sense byte A	91 Not Used
42 Display sense byte B	92 Not Used
43 Display sense byte C	93 Not Used
44 Display sense byte D	94 Not Used
45 Display sense byte E	95 Not Used
46 Display sense byte F	96 Not Used
47 Display sense byte G	97 Modify operator stack
48 Display sense byte H	98 Clear operator stack
49 Not Used	99 Run operator stack

3.3 Program Descriptions and Error Codes

TEST	DESCRIPTION	ERROR MESSAGE(S)
0	Stack Entry	None
1	Auto Program Sequencer Program clears stack and runs tests 3,4,6,10,7,8,24,17,9,7, 8,24,17,72,10,30, & 98.	Refer to individual programs
3	PE Data Channel Present Checks the presence of PE Data Formatter or Read Logic PC assemblies.	1 No Data Formatter PCA 2 No Digital Read Logic PCA
4	Servo Test Tape is run FWD/REV with gradually increasing duration	1 Failure at low speed 2 Failure at high speed 91 BOT/EOT unexpectedly found
5	Capstan Test Checks the total distance of the start/stop ramps	1 Low speed ramps to long 2 Low speed ramps to short 3 High speed ramps to long 4 High speed ramps to short 89 No write ring 90 No head current 91 BOT/EOT detected 93 Timeout waiting for block 94 Timeout waiting for block end 96 No ID status on write from BOT 97 Premature end of ID.
6	FWD/REV Speed Comparison Checks that the FWD high speed and the REV low speed are the correct ratio.	1 Forward high speed is low or reverse low speed is high. Check Speed Adjustment 2 Forward high speed is high or reverse low speed is low. Check Speed Adjustment 91 Not moved off BOT

TEST	DESCRIPTION	ERROR MESSAGE(S)
7	Error Detection Test	
	LWR is performed with various data patterns	PE: 1 Failure of corrected error circuitry 2 Failure to detect false postamble. 3 Failure of MTE circuitry 4 Failure of VPE circuitry NRZI: 1 Failure of VPE circuitry 2 Failure of CRC circuitry 3 Failure of LRC circuitry PE/NRZI: 93 Timeout waiting on block. 94 Timeout waiting on block end.
8	Write/Read Test	
	LWR is performed with fixed and random data patterns Pattern 1 (Fixed Data) Pattern 2 (Random Data)	PE: 1 False preamble---pattern 1 2 False postamble--pattern 1 3 MTE----------pattern 1 4 VPE----------pattern 1 5 Corrected error--pattern 1 11 False preamble---pattern 2 12 False postamble--pattern 2 13 MTE----------pattern 2 14 VPE----------pattern 2 15 Corrected error--pattern 2 NRZI: 1 VPE----------pattern 1 2 CRC----------pattern 1 3 LRC----------pattern 1 11 VPE----------pattern 2 12 CRC----------pattern 2 13 LRC----------pattern 2 PE/NRZI: 17 Data Error (Read) 93 Timeout waiting on block. 94 Timeout waiting on block end.

TEST	DESCRIPTION	ERROR MESSAGE(S)
9	Select High Speed	None
10	Select Low Speed	None
11	Set "n" Sets "n" range from 1-FF Hex. Default value FF.	None
12	Transport Only Selftest	*PWR - DC power line failure *RAM - Control/Mother board RAM failure *CON - Connector missing or badly inserted *BRD - PCA board missing or badly inserted *PR1 - Incompatible control PROMs on Control/Mother board *PR2 - Incompatible diagnostic PROMs on Control/Mother board *PR3 - Diagnostic PROMS are incompatible with Control PROMs on Control/Mother board. *DT7 - Loop-Write-to-Read circuitry failure. *DT8 - Loop-Write-to-Read data transfer failure
13	Select Data Pattern 1 Sets data pattern to 09E Hex	None
14	Select Data Pattern 2 Sets data pattern to 16 bit random pattern	None
15	Failure Skip Causes the failing test in a sequence of test to be aborted if and error occurs	None

TEST	DESCRIPTION	ERROR MESSAGE(S)
17	Write/Back-space/Read Test Write "n" records of a fixed data pattern. See test 13 and 11.	PE: 1 False preamble (Write) 2 False postamble (Write) 3 MTE (Write) 4 Skew Error (Write) 5 VPE (Write) 6 Corrected error (Write) 96 No ID status (Write) 97 Premature end to ID.(Write) 11 False preamble (Read) 12 False postamble (Read) 13 MTE (Read) 14 Skew Error (Read) 15 VPE (Read) 16 Corrected error (Read) 97 Unexpected ID status (Read) NRZI: 1 VPE (Write) 2 CRC (Write) 3 LRC (Write) 11 VPE (Read) 12 CRC (Read) 13 LRC (Read) PE/NRZI: 17 Data Error (Read) 87 Reposition close to limit 88 Reposition outside limit 89 No write ring 90 No head current 91 BOT/EOT detected 93 Timeout waiting on block. 94 Timeout waiting on block end
18	Write "n" Short Records Writes "n" short record of a fixed data pattern in start/stop mode. See tests 13 and 11.	PE: 1 False preamble 2 False postamble 3 MTE 4 Skew Error 5 VPE 6 Corrected error 96 No ID status 97 Premature end to ID. NRZI: 1 VPE 2 CRC error 3 LRC error PE/NRZI: 87 Reposition close to limit 88 Reposition outside limit 89 No write ring 90 No head current 91 BOT/EOT detected 93 Timeout waiting on block. 94 Timeout waiting on block end

TEST	DESCRIPTION	ERROR MESSAGE(S)
19	Write "n" Long Records Writes long records of fixed data pattern in start/stop mode.	See program 18
20	Write "n" Short Records Writes short records of fixed data pattern in streaming mode	See program 18
21	Write "n" Long Records Writes long records of fixed data pattern in streaming mode	See program 18
23	Repositioning Test Checks accuracy of tape speed adjustment	1 High speed ramp too short, or low speed ramp to long 2 High speed ramp too long, or low speed too short 89 No write ring 90 No head current 91 BOT/EOT detected 93 Timeout waiting on block. 94 Timeout waiting on block end 96 No ID status 97 Premature end to ID.

TEST	DESCRIPTION	ERROR MESSAGE(S)
24	Error Detection Test Writes random data to tape and checks error detection	PE: 1 Corrected error inoperative 2 False post amble detection circuitry inoperative 3 MTE detection inoperative 4 VPE detection inoperative 96 No ID status 97 Premature end of ID. NRZI: 1 Failure of VPE circuitry 2 Failure of CRC circuitry 3 Failure of LRC circuitry PE/NRZI: 87 Repostion close to limit 88 Reposition beyond limit 89 No write ring 90 No head current 93 Timeout waiting on block. 94 Timeout waiting on block end
26	Clear Sense Byte Registers	None
27	Select NRZI	92 No NRZI
28	Select PE	None
30	Rewind Tape	None
36	Sensors Test Checks the BOT/EOT	None
37	File Protect Test Operator intervention required	1 Ring circuit active; no ring present 2 Ring circuit non-active, with write ring

TESTS	DESCRIPTION	ERROR MESSAGE(S)
40	Display Proms Revion Number (Control/Mother board) Hidden test. When run the display shows "NONE", if at this time the REWIND button is pressed, the current prom revision number is displayed.	None
41	Display Sense Byte A Contains a log of hard errors The error count is displayed on the front panel in Hex. See Sense Byte Register Table	None
42	Display Sense Byte B Contains a log of hard read errors. Front panel displays no. of errors in Hex See Sense Byte Register Table	None
43	Display Sense Byte C Contains the test number of the interface diagnostic See Sense Byte Register Table	None
44	Display Sense Byte D Contains the error code on interface diagnostics and the error count in fail skip mode See Sense Byte Register Table	None
45	Display Sense Byte E Track in error log. See Sense Byte Register Table	None
46	Display Sense Byte F Contains additional status See Sense Byte Register Table	None

TEST	DESCRIPTION	ERROR MESSAGE(S)
47	Display Sense Byte G Contains additional status See Sense Byte Register Table	None
48	Display Sense Byte H Contains additional status See Sense Byte Register Table	None
50	Step FWD - Low Speed Tape is stepped FWD at low speed to EOT. The size of the steps can be altered by the LOAD/ON-LINE button (LOAD= INCREASE SPEED/DURATION; ON-LINE= DECREASE SPEED/DURATION)	None
51	Step REV - Low Speed Tape is stepped REV at low speed to BOT. LOAD/ON-LINE button controls size of step (see INCREASE and DECREASE explanation in Test 50)	None
52	Alternate - Low Speed Tape run FWD/REV. Size of step controlled by LOAD/ON-LINE*	None
53	Step FWD - High Speed Tape is stepped FWD at high speed to EOT. LOAD/ON-LINE button controls size of step	None
60	Erase to EOT & Rewind	89 No write ring 90 No head current

TEST	DESCRIPTION	ERROR MESSAGE(S)
61	Write Alternate 1's & 0's Alternate 1's & 0's are written to EOT & rewind is initiated.	See program 60
62	Write All 1's All 1's are written to EOT and rewind is initiated.	See program 60
63	Read FWD to EOT (Low speed) (Automatically rewinds EOT)	None
64	Read FWD to EOT (High speed) Capstan strobe is enabled to adjust speed	None
65	Read REV to BOT (Low speed) Capstan strobe is enabled to adjust speed	None
68	Write Ident Test (PE) Writes until EOT or "RESET" is pressed	89 No write ring 90 No write current
70	Space FWD "n" Records Program 11 sets "n"	87 Reposition close to limit 88 Reposition beyond limit 90 EOT detected 93 Timeout waiting on block. 94 Timeout waiting on block end
71	Space REV "n" Records Program 11 sets "n" Fails if started BOT	87 Reposition close to limit 88 Reposition beyond limit 91 EOT detected 93 Timeout waiting on block. 94 Timeout waiting on block end

TEST	DESCRIPTION	ERROR MESSAGE(S)
72	EOF Test	1 No EOF status 87 Reposition close to limit 88 Reposition beyond limit 89 No write ring 90 No head current 91 BOT/EOT detected 93 Timeout waiting on block. 94 Timeout waiting on block end
73	Read FWD "n" Records "n" records of formatted data are read and status errors checked. Program 11 sets "n"	PE: 1 False preamble 2 False postamble 3 MTE 4 Skew error 5 VPE 6 Corrected error 97 Unexpected ID status NRZI: 1 VPE 2 CRC error 3 LRC error PE/NRZI: 87 Reposition close to limit 88 Reposition beyond limit 91 EOT detected 93 Timeout waiting on block. 94 Timeout waiting on block end
74	Read REV "n" Records "n" records of formatted data are read and status errors checked.	See Program 73
82	NRZI Read Skew Test Master skew tape is read	1 None all 1's data detected 92 No NRZI
83	NRZI Write Skew Test Writes all 1's to check write skew	1 None all 1's data detectd 89 No write ring 90 No head current 92 No NRZI 93 Timeout waiting on block.

TEST	DESCRIPTION	ERROR MESSAGE(S)
97	Modify Operator Stack	None
98	Clear Operator Stack	None
99	Run Operator Stack	See individual programs

3.4 Sense Bytes

During online operation of the HP 7974A, additional diagnostics and status information is logged in the sense byte registers. This information is accessible through the 200 level diagnostic programs 41-48. The sense byte values are displayed in a two-digit hexadecimal form. To interpret the meaning, you must convert the hexadecimal value to its equivalent binary value and then map it into the appropriate register in Figure 3-3.

Sense bytes may be cleared by running the 200 level program 26, or by toggling the power.

Only sense bytes C and D are updated when the drive is in diagnostics mode.

3.4.1 Sense Byte Description

Sense Byte A -- Logs all hard and correctable errors reported during online write operations.

Sense Byte B -- Logs all hard errors reported during online read operations.

Sense Byte C -- This register is used, in conjunction with Sense Byte D, to report the results of diagnostic tests at the interface. Read data lines 0-4 indicate the last diagnostic program run.

Sense Byte D -- In online diagnostics, the register represents the error code associated with Sense Byte C. In offline diagnostics, it becomes the error count register for Failure Skip mode.

Sense Byte E -- This register contains "track in error" information. It should be examined when a single track error has been reported. A single track error with no bit set in this register indicates a parity error. The register is cleared to zero when the tape unit is powered up, and at the start of all motion commands when online.

Sense Byte F -- Logs hard error information in both PE and NRZI mode. The register is cleared when the drive is powered up and at the start of all motion commands. Each bit flag is defined as follows:

PHASE ENCODED

Bit	Name	Definition
7	--	Set to 0 in PE
6	ID Found	ID detected while reading
5	CERS	Corrected Error (STE)
4	VPE	Vertical Parity Error
3	SKEW	Skew buffer overflow
2	MTE	Multi-track in Error
1	FPOST	False Postamble detected.
0	FPRE	False Preamble detected

NRZI

Bit	Name	Definition
7	--	Set to 1 in NRZI
6-3	--	Not used
2	LRCE	LRC Error
1	CRCE	CRC Error
0	VPE	Vertical Parity Error

Sense Byte G -- Contains miscellaneous error and status information. The register is cleared at power up and at the start of all motion commands. The flag bits 7-0 are defined consecutively:

RFAIL - No read-after-write data detected in write operation.

INCOMPLETE - Set if last operation terminated in unexpectedly:
(1) Drive suddenly offline; reset occured or door opened
(2) Forward file search passed EOT and timed out at 4 ft without detecting a file mark
(3) Reverse file search halted at BOT without finding file mark
(4) Space reverse command halted by detection of BOT marker

REJECT - Set if unable to perform requested tasks:
(1) tape command with tape not loaded
(2) reverse command with tape at BOT
(3) write command to tape without write-enable ring

BLANK - Set true when more than 9.1 m (25 ft.) of blank tape has been detected in a read or space operation.

IDENT ERROR - Set when the ID has not been detected in the PE mode.

PAST EOT - Set when the tape has passed the EOT marker in the forward direction. Resets when the EOT marker passes the sensor in reverse direction.

FMLB - File mark last block; set if the last data block seen had file mark status.

WTNG - Write head current is sensed.

Sense Byte H -- Contains additional error and status information. The bits 7-0 are defined as follows:

BOT TIMEOUT - Set if tape does not move off of BOT during a reposition from BOT.

TEMP LATCHED - Indicates the state of the temperature sensor at the end of the previous operation.

TEMP - Indicates that the temperature sensor was activated.

REP LAST BLK - Indicates that the last operation was preceded by a reposition.

REP ERR 2 - Indicates that a reposition has occurred which is out of limit.

REP ERR 1 - Indicates that a reposition has occurred which is close to the specified limits.

NOTE

The three reposition bits are updated at every reposition cycle. If an error is detected during reposition 1, then no error conditions will be rested during reposition 2.

TEMP 2 - Indicates that an extra long delay exists between online high speed commands.

TEMP 1 - Delay activated between high speed commands.

Figure 3-3 Sense Byte Registers

	MOST SIGN. HEX DIGIT				LEAST SIGN. HEX DIGIT				
BYTE	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	Data Channel
A	2**7	2**6	2**5	2**4	2**3	2**2	2**1	2**0	Write Error Log
B	2**7	2**6	2**5	2**4	2**3	2**2	2**1	2**0	Read Error Log
C	-	2**6	2**5	2**4	2**3	2**2	2**1	2**0	Diagnostic Test No.
D	2**7	2**6	2**5	2**4	2**3	2**2	2**1	2**0	Diagnostic Error Code
E	TRK 7	TRK 6	TRK 5	TRK 4	TRK 3	TRK 2	TRK 1	TRK 0	Dead Track
F PE	0	ID FOUND	CERS	VPE	SKEW	MTE	FPOST	FPRE	EXTRA
F NRZI	1	-	-	-	-	LRCE	CRCE	VPE	STATUS
G	RFAIL	INC'P	REJT	BLANK	IDENT ERROR	PAST EOT	FMLB	WTNG	
H	BOT T/OUT	TEMP LATCH	TEMP	REPOS LSTBL	REP ERR 2	REP ERR 1	TEMP2	TEMP1	

SENSE BYTES ARE NOT NORMALLY UPDATED (EXCEPT C AND D)
IN DIAGNOSTIC MODE.

This page intentionally left blank.

REPLACEABLE PARTS

SECTION IX

New Part Number	Description
108709-TED	Control/Motherboard (109590) 3/6
108710-TED	Data Formatter (109580) 07974-69022
108702-TED	Read Logic PCA (109570) 07974-69021
108716-TED	NRZI PCA (109530) 07974-69023
07978-66504	Master Control PCA
76952-TED	Motor Reel
79140-TED	Hub Assembly, File
105610-TED	Hub Assembly, Take up
103575-TED	Tape Cleaner
78641-TED	Roller Cap
108715-TED	Motor and Cap Assy
108533-TED	BOT and EOT Sensor Assy
108707-TED	Strobe Light Assy
108706-TED	Head Assy, PE/NRZI 4/14
108714-TED	Switch Facia PCB Assy
109541-TED	NRZ Head Adaptor (Write)
109542-TED	NRZ Head Adaptor (Read)
108494-TED	Arm Drive Assy
108705-TED	PCA, 5 Volt Regulator
105678-TED	PCA, Power Supply
103710-TED	Power Supply Assy
76449-TED	Capstan Motor Shim Kit
76881-TED	Head Deskew Kit
78535-TED	Voltage Selector 100 VAC
78528-TED	Voltage Selector 110 VAC
78529-TED	Voltage Selector 115 VAC
78530-TED	Voltage Selector 120 VAC
78531-TED	Voltage Selector 220 VAC
78532-TED	Voltage Selector 230 VAC
78533-TED	Voltage Selector 240 VAC
76332-TED	Door Switch Assy
78636-TED	Write Enable Assy
78758-TED	Arm Position Sensor
78762-TED	Capstan and Strobe Disk Assy
78763-TED	Bridge Roller Assy
78764-TED	Roller Guide Assy
78769-TED	Capstan Motor and Tach Assy
78798-TED	Tension Arm Assy (Upper)
78799-TED	Tension Arm Assy (Lower)

New Part Number	Description	
5061-3144	Power Supply (HP Controller)	
07978-66506	PCA, HPIB I/O	
07974-66501	PCA, Interconnect	
07974-89701	EEProm U23	
07974-89801	EEProm U7	
07974-89504	EProm 4.0 U21	4/6
07974-89604	EProm 4.0 U5	4/6
07974-89104	EProm 4.0 U19	4/6
07974-89204	EProm 4.0 U3	4/6
07974-89304	EProm 4.0 U20	4/6
07974-89404	EProm 4.0 U4	4/6
1826-0147	Regulator MC7812	
1826-0221	Regulator MC7912	
1826-0445	Regulator MC7905	
2110-0002	Fuse, 2AMP	
2110-0003	Fuse, 3AMP	
2110-0051	Fuse, 10AMP	
2110-0030	Fuse, 5AMP Slo-Blo	
2110-0303	Fuse, 2AMP Slo-Blo	
1490-0738	Reel, Take-up	
5060-9456	HPIB Cable, 2 Meter	
9164-0158	Magnetic Tape, 1 Reel	

CONTENTS: SECTION X

This page intentionally left blank.

[1] FIRMWARE UPDATE

1.1 PROCEDURE

(a) Mount the firmware update tape.

(b) Select diagnostic program *30* * and press ENTER The front panel LEDs will display **V00**. This indicates that the version number of the update should be entered.

(c) Input the version number using the Tens and Units buttons on the front panel and press ENTER.

After the ENTER button is pushed, the tape unit reads the update tape. The process takes approximately 10 seconds. During the update, the front panel displays a countdown from 8 to 0. When the countdown reaches 0, the tape unit goes into power-on selftest. The firmware update tape can be removed.

NOTE

If the RESET button is pressed during the update sequence, **D4** will be displayed at the end of the countdown sequence. **D4** indicates that the power should be cycled and the ROMs changed. This is a special feature which allows the EEPROM update locations to be cleared prior to a ROM change.

If the RESET button is pressed when the update version ID is requested, the update will be terminated.

1.2 ROM CHANGE/INITIALIZATION

When ROMs are changed, the previous update information must be cleared to allow the new code to function properly. To clear the EEPROMS, hold down the LOAD, ON-LINE, and the REWIND buttons for one second after the power is cycled. The display will show **BUSY**.

CAUTION

Do not use this procedure to initialize the EEPROMS unless you have an update tape available. There is no way to recover without a tape!!!

---

*100-Level diagnostics programs are written in *ITALICS* and 200-Level diagnostics are written in **BOLD**.

1.3 LOCAL UPDATE ERROR CONDITIONS

The following are a list of errors which can occur after an update tape is mounted. Refer to Section VIII for additional hardware errors.

D201	Timeout waiting
D202	Greater than 7 retries in reading a record
D203	Soft error in record just read.
D204	Tape runaway occurred while trying to find an update record.
D205	Tape position lost when trying to read update record.
D206	Controller error when trying to read update record.
D207	Servo error when trying to read update record.
D208	Door opened during an update read.
D209	Timing error during update read.
D20A	Formatter error during update read.
D20B	Transaction ID mismatch.
D20C	Command reject. Check out EEPROM circuits with associated tests.
D365	Data buffer parity error occurred during the update. Check out data buffer circuits on Master Control.
D368	Firmware update is too big. Verify update version on tape.
D369	Invalid ID for firmware update. Re-enter version number or get correct tape.
D36A	Invalid version ID. Re-enter version number or get correct tape.
D36B	Bad firmware update checksum. Retry tape or replace.
D36C	Less than the minimum four bytes of data were contained in the update data record. Retry tape or replace.
D36D	An odd number of bytes were in the firmware update record. Retry tape or replace.
D36E	Wrong update for current ROM revision. Replace update tape with correct version.
D36F	Operator pressed the RESET button instead of entering a version number on the front panel.
D4	Firmware update successful. If **D4** flashes during the countdown cycle, a set of ROMS must be changed after the update is complete. Refer to the instructions provided with the current update tape/kit for details.

PRODUCT HISTORY

SECTION XI

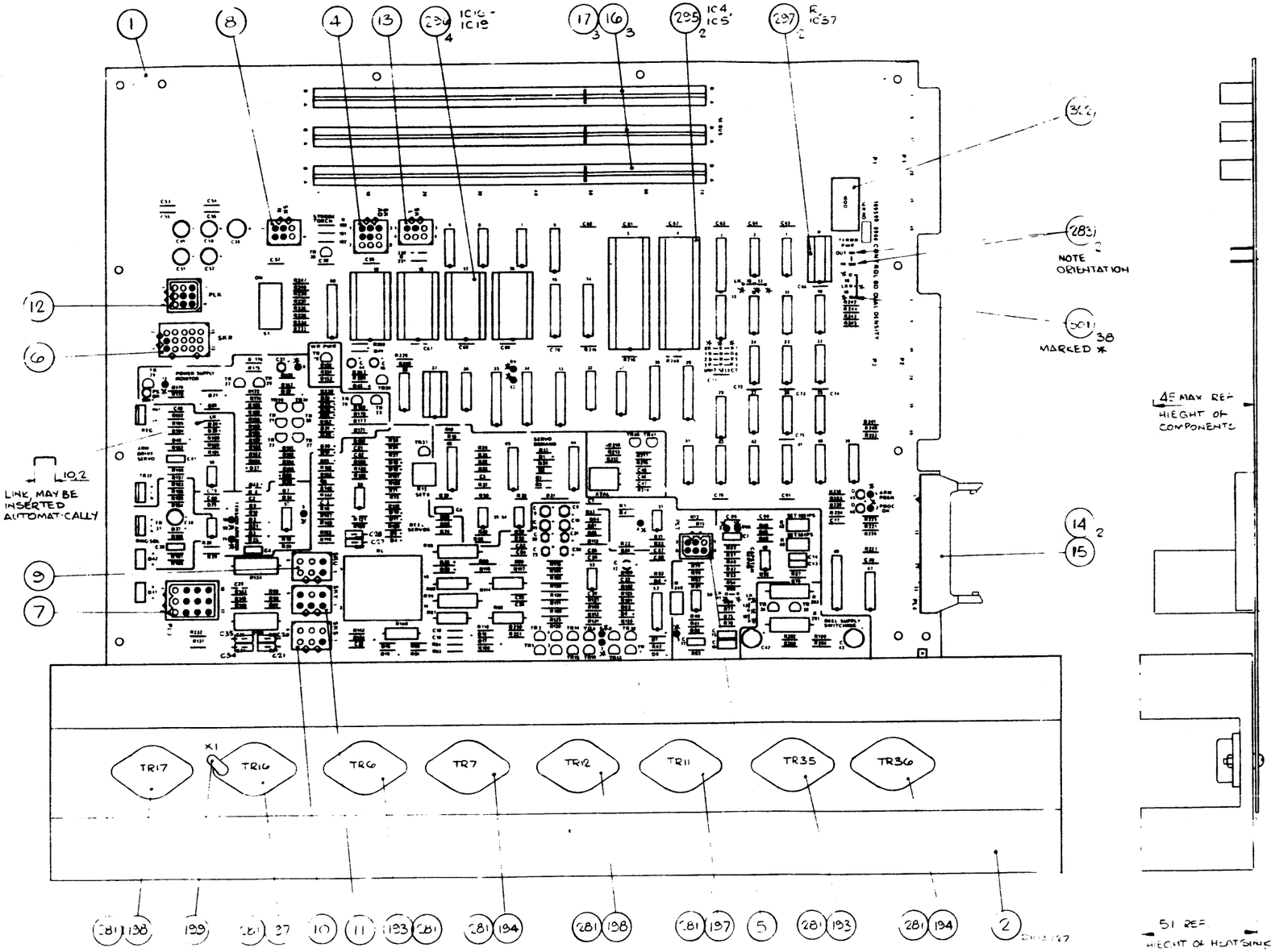
NOT AVAILABLE AT THIS PRINTING

DRG No D109590 SHT 1

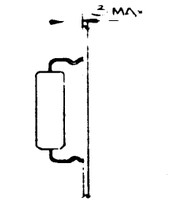
DRAWING COMPLIES WITH B.S. 308 AND B.S. 3939

3rd ANGLE PROJECTION — REMOVE ALL BURRS & SHARP EDGES UNLESS OTHERWISE STATED — WORK TO DIMENSIONS

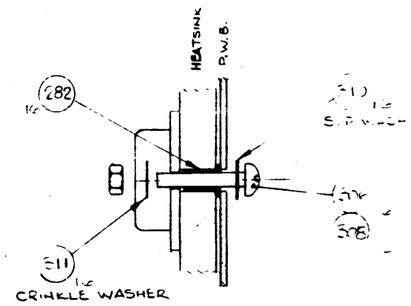
ISSUE NO	DATE	CHANGE NO	CLASS	CHECKED	DESCRIPTION OF CHANGE
2					



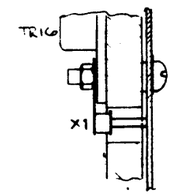
45 MAX REF HEIGHT OF COMPONENTS



RESISTORS LISTED BELOW TO BE MOUNTED AS SHOWN: 87, 88, 92, 95, 96, 114, 124, 149, 150, 201, 202, 177.



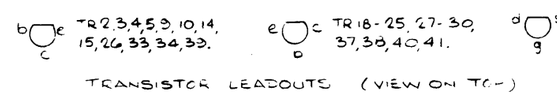
METHOD OF SECURING TO P.W.B. TIGHTEN NUT TO 6.0 lbf in DO NOT TURN SCREW



MOUNTING METHOD FOR X1

NOTE 1 WHEN ELECTROCRAFT MOTORS ARE USED, MAKE LINKS 11 & 13. WHEN TORQUE SYSTEM MOTORS, MAKE LINK 12.

2 WHEN DAISY CHAINING, ON MOST TRANSPORT FIT LINK 18 AND OMIT R NETWORK. ON INTERMEDIATE TRANSPORT FIT LINK 13 AND OMIT R NETWORK. ON END TRANSPORT FIT LINK 13 AND FIT R NETWORK.



TRANSISTOR LEADOUTS (VIEW ON TOP)

DRAWN	JW	MAY 79
CHECKED		
CERT'D		
TRACED		
CHECKED		
WEIGHT		DATE

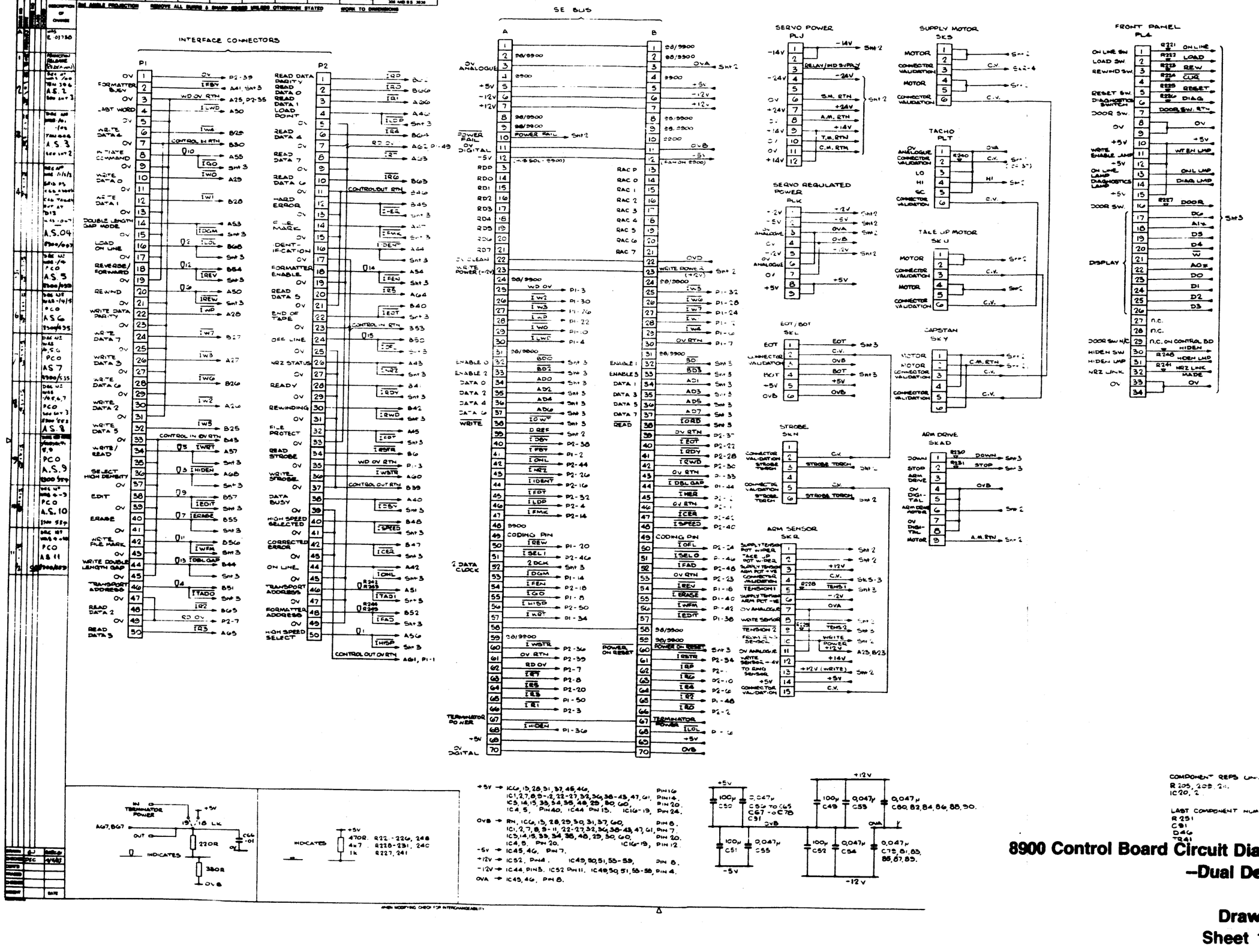
WHEN MODIFYING CHECK FOR INTERCHANGEABILITY

8900 Control Board PCA
--Dual Density

Drawing 1

8900 Control Board Circuit Diagram --Dual Density

Drawing 2
Sheet 1 of 3



109558/1

NOTE
FOR ELECTROCRAFT CAPSTAN MOTORS, FIT LINKS 11 & 13.
FOR TORQUE SYSTEM CAPSTAN MOTORS, FIT LINK 12.

8900 Control Board Circuit Diagram --Dual Density Drawing 2 Sheet 2 of 3

8900 Control Board Circuit Diagram --Dual Density

Drawing 2

Sheet 3 of 3

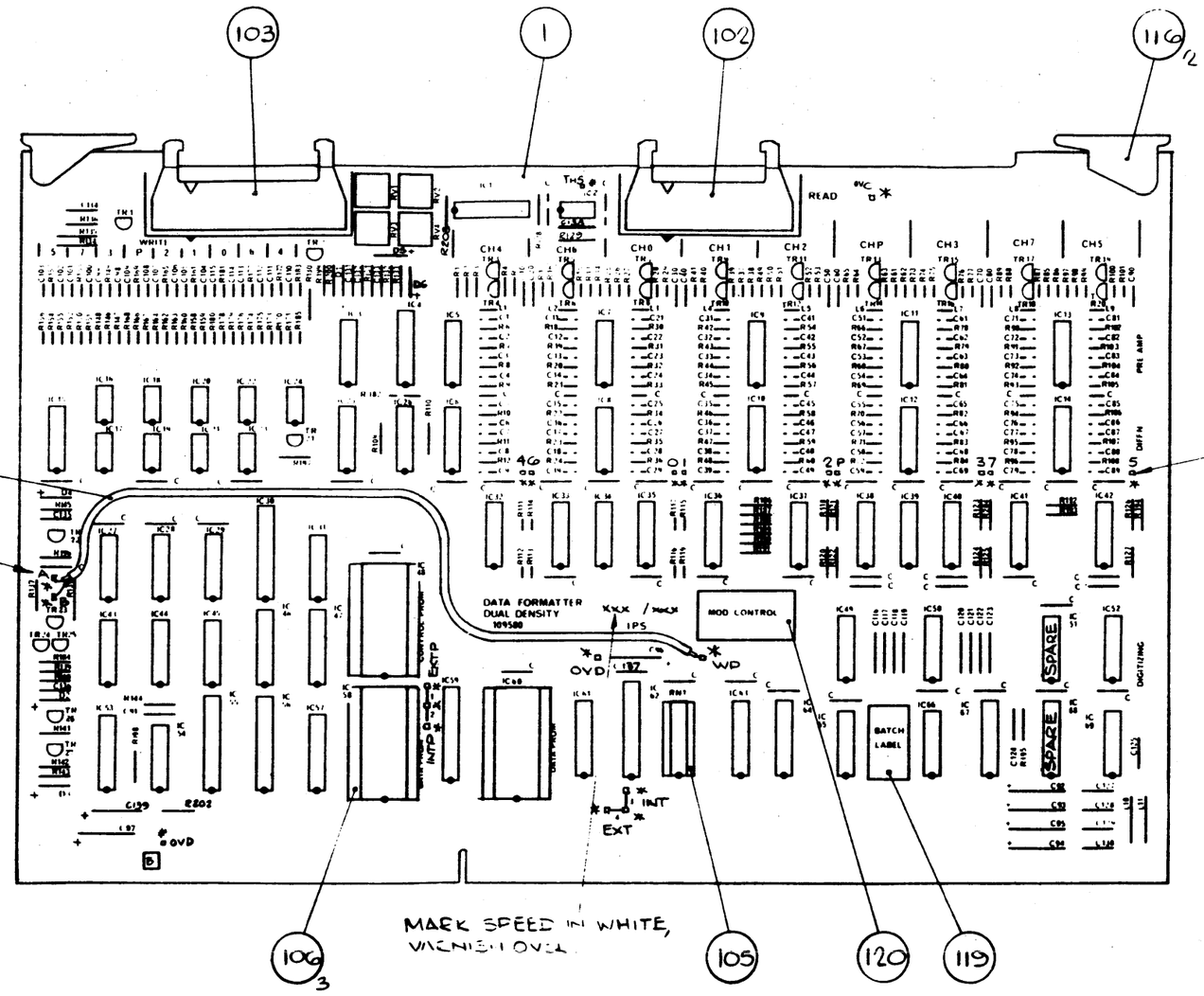
DRG No **C109580/05**

ISSUE NO	DATE	CHANGE NO	CLASS	CHECKED	DESCRIPTION OF CHANGE
1	27 6 83				PRODUCTION RELEASE
2	20 9 83				A/W 155 B TAN9 INC TED 8900-414 403 409.415 3800 352 358 9900-45 60
3	9 10 83				A/W 155C REF TAN 414 8900-421

SERIES REF
QUANTITY/UNIT
ASSEMBLED ON

DRAWING COMPLIES WITH B.S. 308 AND B.S. 3939

3rd ANGLE PROJECTION — REMOVE ALL BURRS & SHARP EDGES UNLESS OTHERWISE STATED — WORK TO DIMENSIONS



COMPONENTS LISTED BELOW VARY WITH SPEED.

SPEED IPS	25/50, 25/100	37.5/100	50/100
SYSTEM	8800 2200	8900 ICL	8900 STD
ASSY	109568	109569	109580
R3, 15, 27, 39, 51, 63, 75, 87, 99.	270R	NOT FITTED	NOT FITTED
R4, 16, 28, 40, 52, 64, 76, 88, 100.	1k6	1k	1k6
L1-9	1mH	WIRE LINK	WIRE LINK
R195	68k	47k	47k

DRAWN	CMO	UNLESS	
CHECKED			
CERT'D			
TRACED			
CHECKED			
WEIGHT		DATE	

NOTE.
1. FOR STAND-ALONE TRANSPORT FIT LINK 3 & RN1.
   WHEN DAISY-CHAINING : ON HOST FIT LINK 3 & OMIT RN1;
   ON INTERMEDIATE TRANSPORTS FIT LINK 4 & OMIT RN1;
   ON END-OF-LINE TRANSPORT FIT LINK 4 & RN1.
2. FOR STANDARD BUILD FIT LINK 2 (INT D)
3. FOR LINKS USE (107)

Data Formatter Assembly --Dual Density

Drawing 3

DRG No D109588/10 SHT 1 of 4

ISSUE NO | DATE | CHANGE NO | CLASS | CHECKED | DESCRIPTION OF CHANGE

3rd ANGLE PROJECTION — REMOVE ALL BURRS & SHARP EDGES UNLESS OTHERWISE STATED — WORK TO DIMENSIONS

DRAWING COMPLIES WITH B.S. 308 AND B.S. 3939

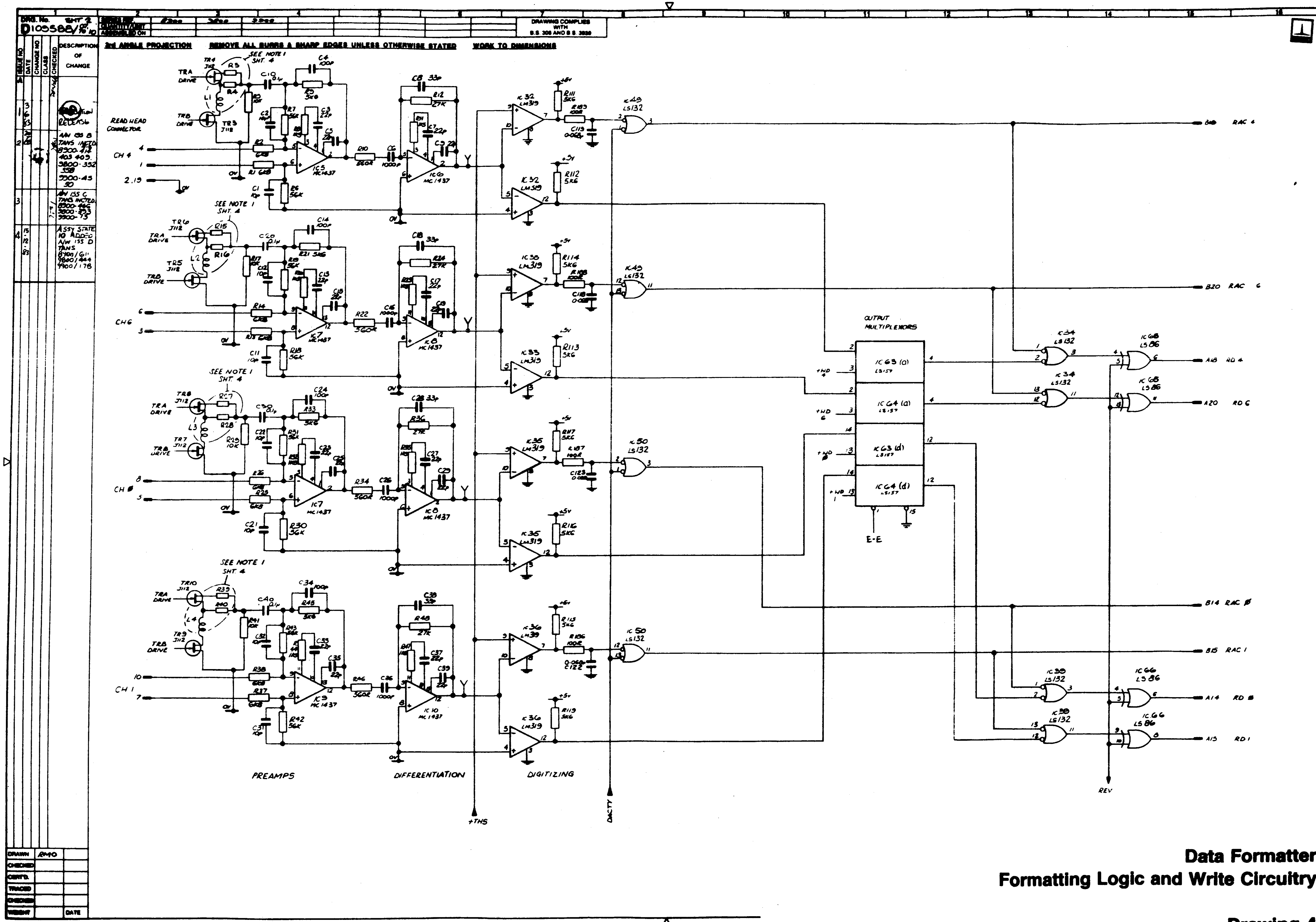
POWER FAIL / WRITE CONTROL

Data Formatter
Formatting Logic and Write Circuitry

Drawing 4
Sheet 1 of 4

DRAWN R140 | CHECKED | CERT'D | TRACED | CHECKED | WEIGHT | DATE

WHEN MODIFYING CHECK FOR INTERCHANGEABILITY



Data Formatter

Formatting Logic and Write Circuitry

Drawing 4

Sheet 2 of 4

DRG. No SHT 3. D109588/10

SERIES REF | 8500 | 3800 | 3500

QUANTITY/UNIT ASSEMBLED ON

DRAWING COMPLIES WITH BS 308 AND BS 3939

3rd ANGLE PROJECTION — REMOVE ALL BURRS & SHARP EDGES UNLESS OTHERWISE STATED — WORK TO DIMENSIONS

ISSUE NO	DATE	CHANGE NO	CLASS	CHECKED	DESCRIPTION OF CHANGE
A					PRODUCTION RELEASE
1					A/W 155 B TANS MKTG 8900 478 433 409 3800-357 -358 3500-45 -50
3					A/W 155 C TANS MKTG 8900-466 3800-393 3500-73
4					ASSY DRG -/11 ALSO TANS Symbol 444 478 A/W 155 D

DRAWN | CHECKED | CERT'D | TRACED | CHECKED | WEIGHT | DATE

WHEN MODIFYING - MEAN FOR INTERCHANGEABILITY

CH2 · CH3 · CH7 · CH5 · CH PARITY

TRA DRIVE · TRB DRIVE · SEE NOTE 1 SHT 4 · VOTE 1

IC 9 MC 1437 · IC 10 MC 1437 · IC 11 MC 1437 · IC 12 MC 1437 · IC 13 MC 1437 · IC 14 MC 1437 · IC 15 MC 1437

IC 37 LM319 · IC 38 LM319 · IC 40 LM319 · IC 41 LM319 · IC 42 LM319

IC 50 LS132 · IC 49 LS132 · IC 45 LS132

DACTY

R195 VALUE SPEED DEPENDANT SEE NOTE 1

IC 67 LS123

OUTPUT MULTIPLEXORS

IC 63 (b) LS157 · IC 64 (c) LS157 · IC 64 (b) LS157 · IC 63 (c) LS157

+HD 2 · +HD PAR · +HD 3 · +HD 7 · +HD 5

E-E

IC 68 LS132 · IC 69 LS158 · IC 52 LS86

IC 66 LS86 · IC 65 LS86 · IC 39 LS132 · IC 34 LS132

B1G RAC 2 · B1B RAC P · B17 RAC 3 · B21 RAC 7 · B19 RAC 5

A1G RD 2 · A1B RD P · A17 RD 2 · A21 RD 7 · A19 RD 5

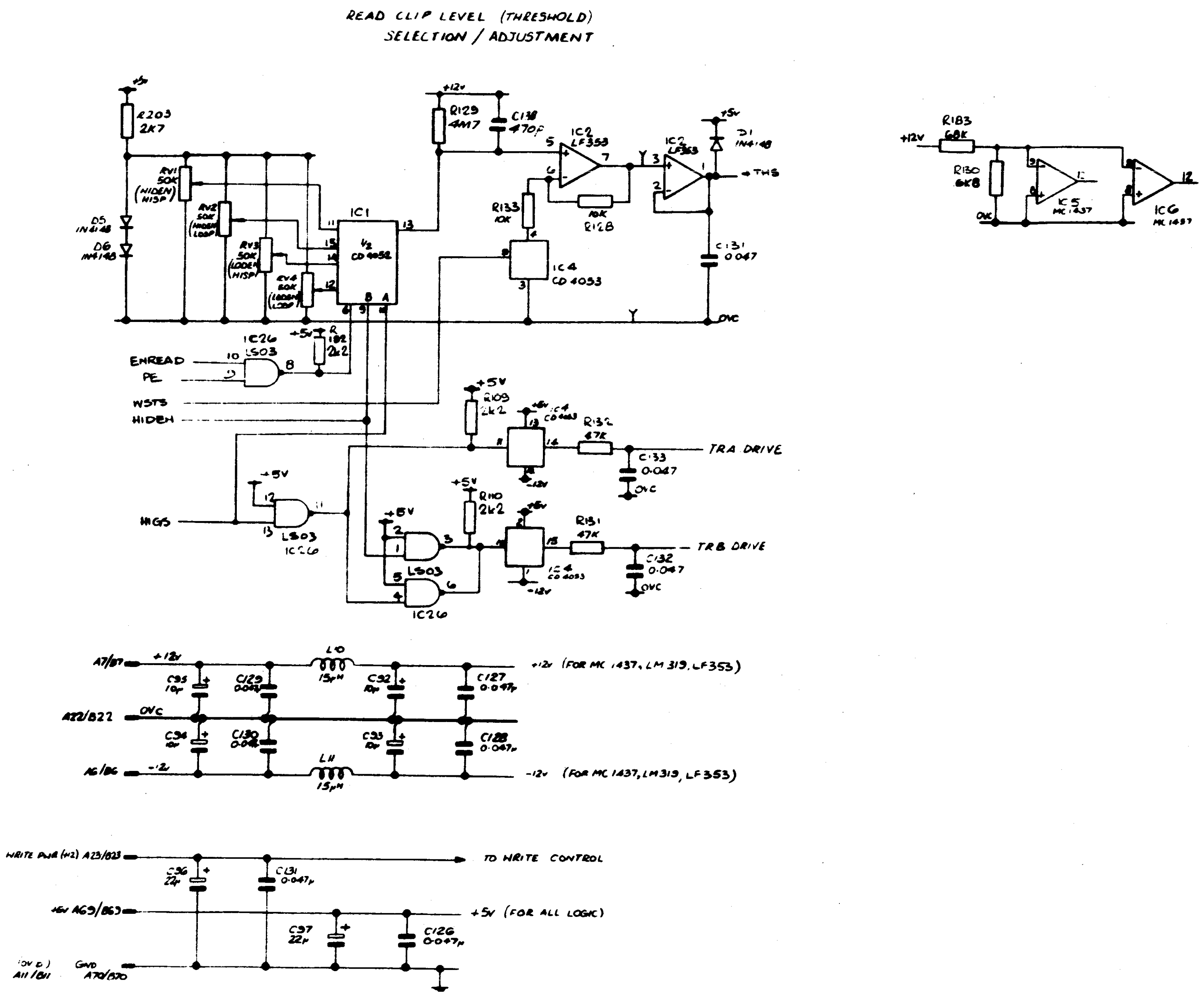
REV · +5V · +THS · 0V

Data Formatter
Formatting Logic and Write Circuitry

Drawing 4
Sheet 3 of 4

D109588/7 to /10

3rd ANGLE PROJECTION — REMOVE ALL BURRS & SHARP EDGES UNLESS OTHERWISE STATED — WORK TO DIMENSIONS



POWER CONNECTIONS

TYPE	CHIP IDENT	+12V	-12V	0V	GND	+5V	0V WIPER
MC1437	IC5-14	14	7				
LM319	32,33,35-38,40-42	11	6		3,8		
LS86	IC52,65,66				7	14	
LS132	IC34,39,45,50,63				7	14	
LS157	IC57,61,63,64				8	16	
LS04	IC15,25,44				7	14	
74H06	IC54				7	14	
LS00	IC31				7	14	
LS03	IC26				7	14	
LS37	IC3				7	14	
LS138	IC46				8	16	
LS273	IC30,55,56,59,62				10	20	
LS11	IC43				7	14	
LS74	IC28,29				7	14	
LS86	IC53				8	16	
2732	IC48,58,60				12	24	
LS33	IC47				7	14	
LS02	IC27				7	14	
LS32	IC45				7	14	
LS123	IC67				8	16	
CD4052	IC1			7	8	16	
CD4053	IC4		7		6,8	16	
LF353	IC2	8	4				
74S472	IC16-24					8	4

NOTE

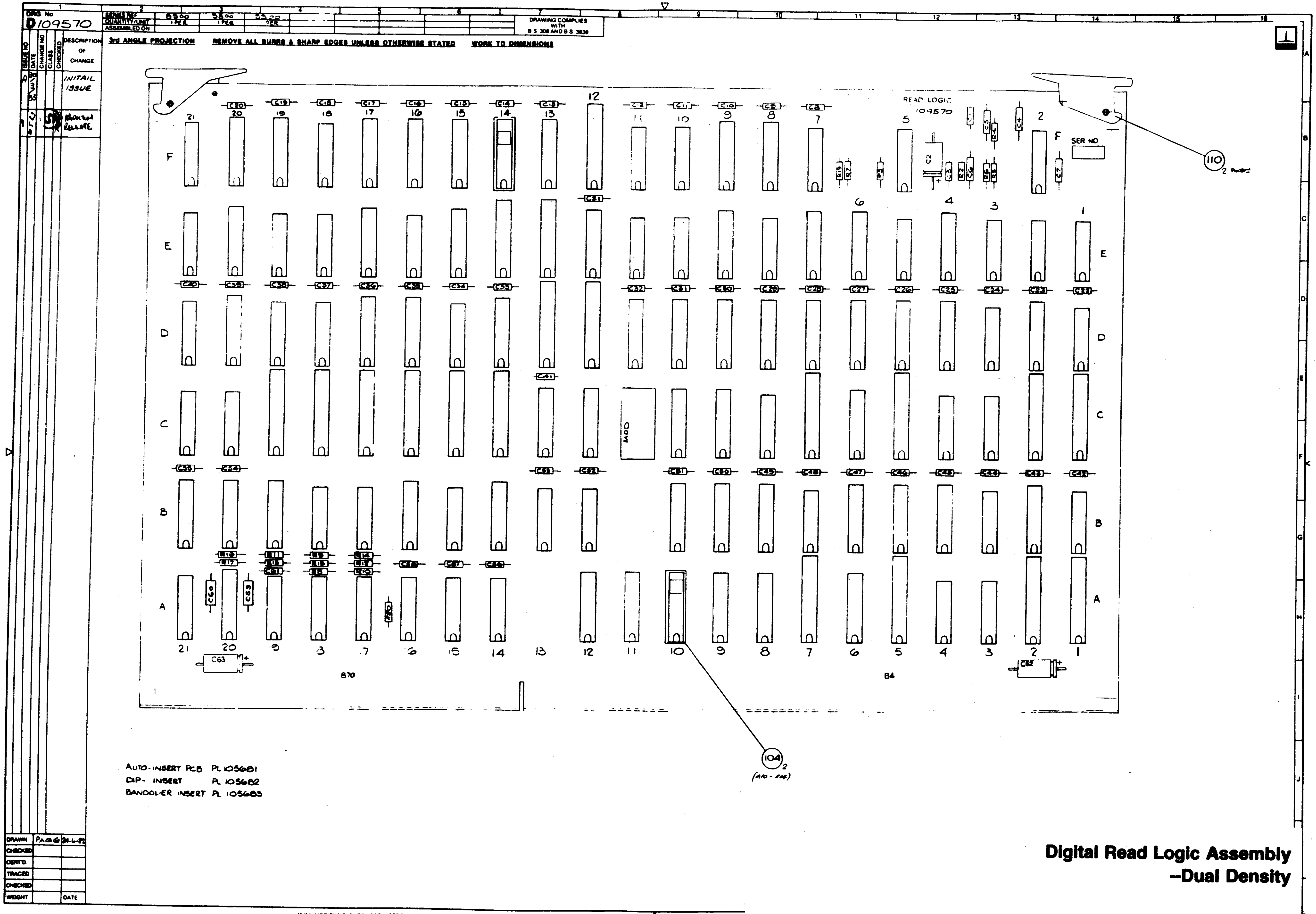
1. PREAMP COMPONENT VALUES ALTER WITH SPEED BUILD AS INDICATED BELOW :-

SPEED IPS	25/50 25/100	37.5/100	50/100
SYSTEM	9300 9200	8900 ICL	8900 STD
ASSY	103568	109569	109580
R3, R15, R27, R39, R51, R63, R75, R87, R99	270R	NOT FITTED	NOT FITTED
R4, R16, R28, R40, R52, R64, R76, R88, R100	1KG	1K	1KG
L1-L9	1mH	WIRE LINK	WIRE LINK
R195	68K	47K	47K

DRAWN RMO

WHEN MODIFYING CHECK FOR INTERCHANGEABILITY

Data Formatter
Formatting Logic and Write Circuitry



Digital Read Logic Assembly –Dual Density

Drawing 5

DRAWING COMPLIES WITH BS 308 AND BS 3939

3rd ANGLE PROJECTION — REMOVE ALL BURRS & SHARP EDGES UNLESS OTHERWISE STATED — WORK TO DIMENSIONS

DESCRIPTION OF CHANGE

INITIAL RELEASE

SPARE GATES :-

L500 IC NR 83 PIN NRS 1,2,8,9, 12,13 & 11

16 IC NR A17 PIN NRS 3 4 6

L532 IC NR PIN NRS CRY 5,10,6,8, 15,12 & 11

L581 B11

LSH2 B21

L500 E2

DATE

8900,9800,9900 Digital Read Logic Circuit Diagram (Dual Density)

Drawing 6

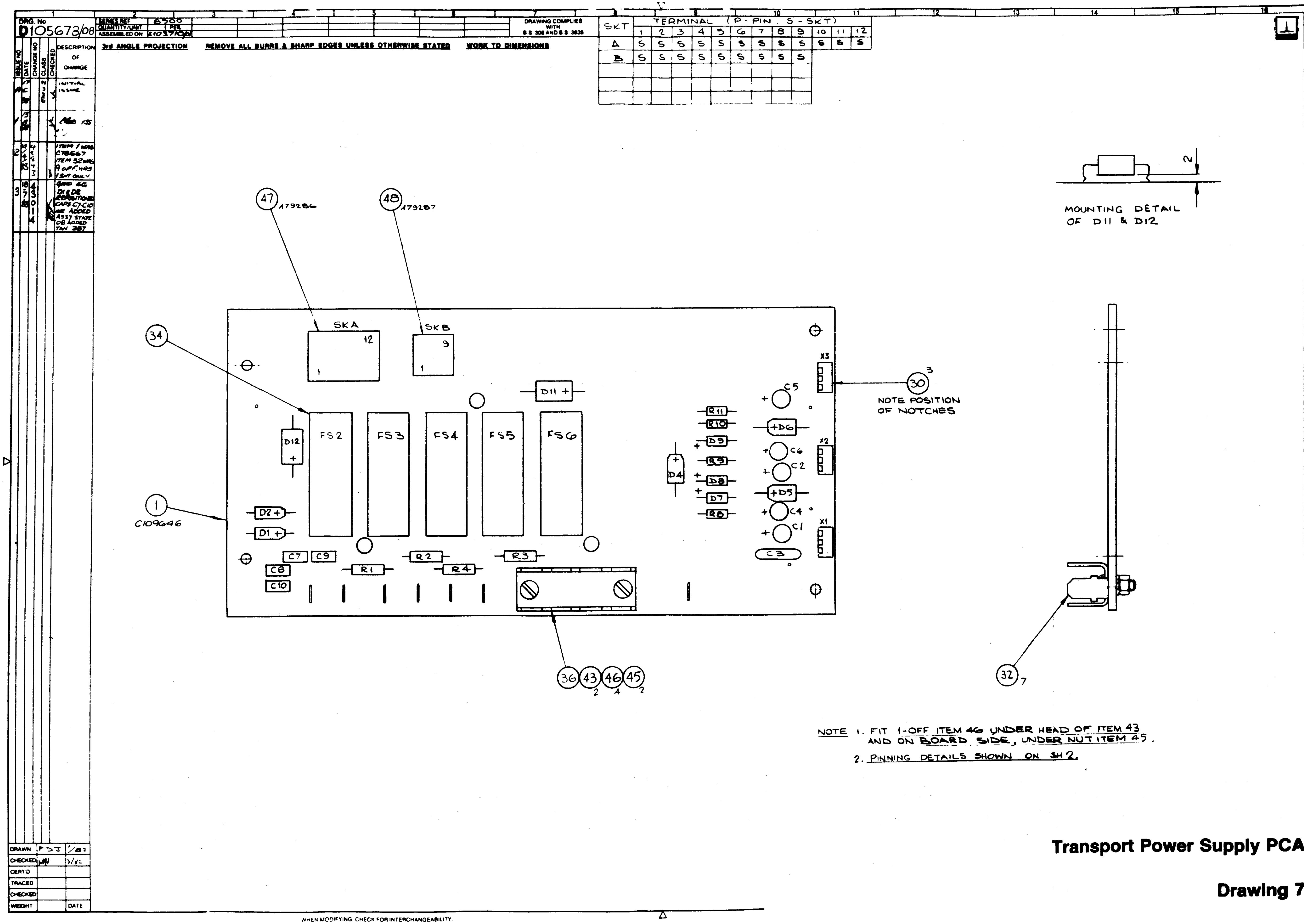
DRAWING COMPLIES WITH BS 308 AND BS 3939

3rd ANGLE PROJECTION — REMOVE ALL BURRS & SHARP EDGES UNLESS OTHERWISE STATED — WORK TO DIMENSIONS

DESCRIPTION OF CHANGE

8900,9800,9900 Digital Read Logic Circuit Diagram (Dual Density)

Drawing 6



Transport Power Supply PCA

Drawing 7

REMOVE ALL BURRS & SHARP EDGES UNLESS OTHERWISE STATED WORK TO DIMENSIONS

INITIAL ISSUE

BOARD CONNECTORS

VOLTAGE SELECT (240V SHOWN)

SWITCHED MAINS OUTLET

PLG

SK (3 WAY)

SKG (MOLEX 15 WAY)

BN

BU

GN/Y

E T A

BN/R 120V
BN/O 115V
BN/Y 110V
BN/V 100V
BN/BU 0V
BU/R 120V
BU/O 115V
BU/Y 110V
BU/V 100V
BU/GN 0V

T1

PRI

SEC

17.7V Y/RD

17.7V Y/O

10.5V PK

0V BK

TRANS. FRAME

GN/Y SCREEN ET1

TERMINAL TO DECK CASTING

S1 2600-11E

FRONT PANEL EARTH TERMINAL ET?

FRONT PANEL ASSEMBLY

BN/PK BU/PK

FS1 T2A 'TSA

BN R12

C14 0.1 250V AC

D1

E L N

ET1 ET2

PL A MAINS RECEPTACLE

+5V SWITCHING REGULATOR BOARD C105630

RD

W

BK

SEE NOTE 1

RC 1 SCBE1

RC 2 SCBE1

C7 22000 40V BK

C8 22000 40V BK

C9 33000 25V BK

C10 33000 25V BK

R1 1K(1W)

R2 1K(1W)

R3 1K(1W)

R4 1K(1W)

C11 1 50V

C12 1 50V

0V

0V BUS

D1 IN5401

D2 IN5401

FS2 3A

TP

24V PK

R11 10K

FS3 10A +24V

FS4 10A 24V

FS6 10A +VR (SERVO) +14V

FS5 10A -VR (SERVO) -14V

D11 60505

D12 60505

SKA (MOLEX 12-WAY)

+24V
-24V
+14V
-14V
0V
SERVO POWER

SKB (MOLEX 9-WAY)

+12V
-5V
0V
-12V
REGULATED POWER

+5V (5.25V NOM)

+24V

X1 MC7812

X2 MC7912

X3 MC7805

C1 2.2 35V

C2 2.2 35V

C3 .01 25V

C4 2.2 35V

C5 2.2 35V

C6 2.2 35V

R8 4K7

R9 4K7

R10 4K7

D4 5401

D5 5401

D6 5401

D7 4002

D8 4002

D9 4002

0.5A MAX

0.6A

+12V

-12V

-5V

TP

PCB ASSEMBLY D105678

NOTE 1 0V NORMALLY CONNECTED TO CHASSIS BY ADDITIONAL WIRE TO DECK CASTING

WHEN MODIFYING CHECK FOR INTERCHANGEABILITY

Transport Power Supply Circuit Diagram

Drawing 8

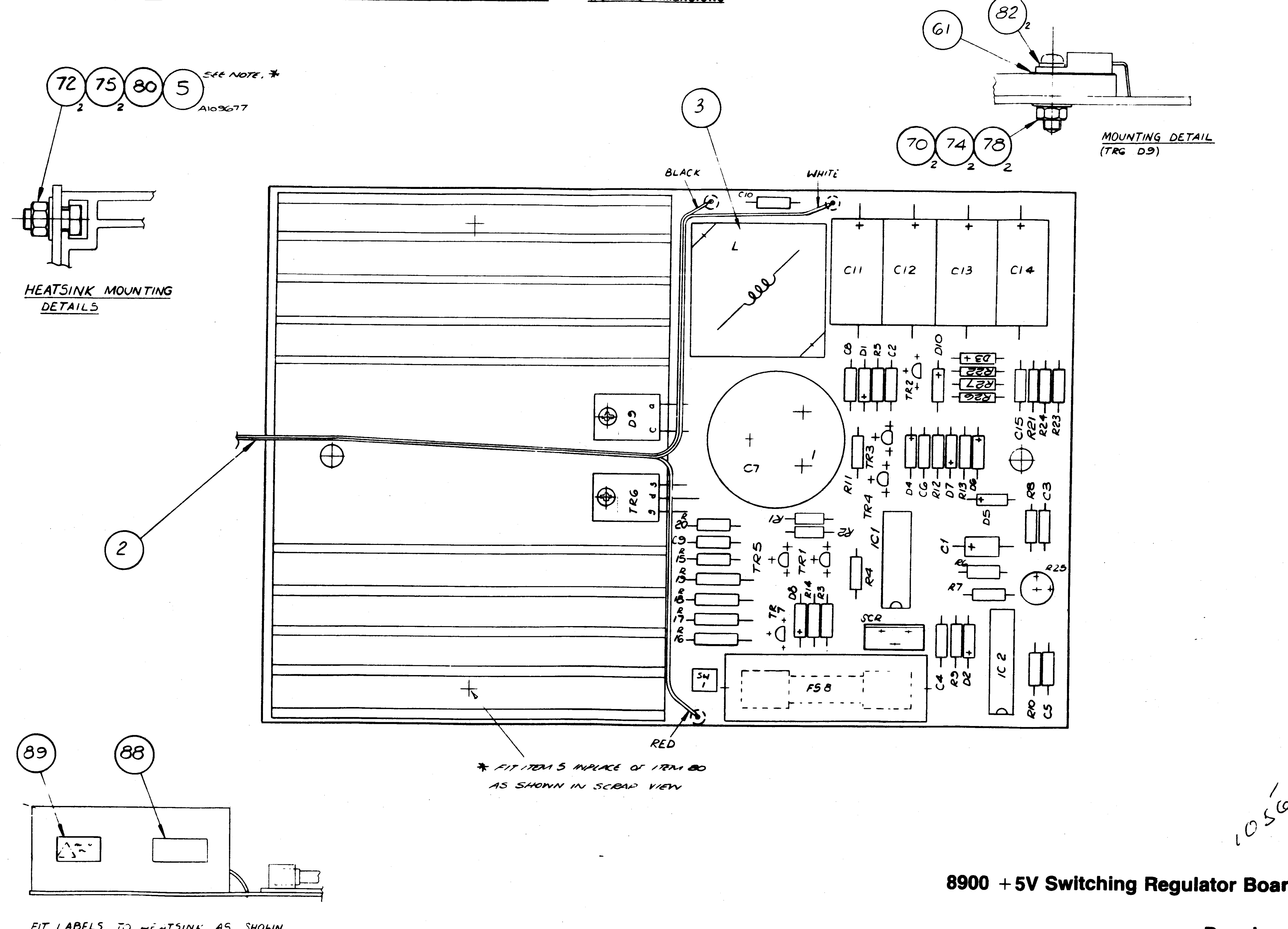
DRG No. C 105630/07

SERIES REF	8900
QUANTITY/UNIT	1 PER
ASSEMBLED ON	E103710

DRAWING COMPLIES WITH B S 308 AND B S 3939

3rd ANGLE PROJECTION **REMOVE ALL BURRS & SHARP EDGES UNLESS OTHERWISE STATED** **WORK TO DIMENSIONS**

ISSUE NO	DATE	CHANGE NO	CLASS	CHECKED	DESCRIPTION OF CHANGE
A					NEW LAYOUT
B				EMU	COMP. RE-POS ... SUT ISS ...
C					ORIENTATION ADDED TO XC, CABLEFORM ADDED. ITEM 88 ADDED. TANS INC'TED 8900/02,03, 08,011,016 ... ITEM 82 ADDED 025
1	17 6 82				PROD ISSUE
					'0' ADDED TO DRG NUMBER
2	17 1 83				A/W ISS 2 TANS. 226, 261 BROUGHT INTO LINE WITH ...
3	13 5 83				TAN 261 & 238, ITEM 5 ADDED, ITEM 80 WAS ...



DRAWN	RMO	30.1.82
CHECKED		
CERT D		
TRACED		
CHECKED		
WEIGHT		DATE

105630

8900 +5V Switching Regulator Board

Drawing 9

A2

WHEN MODIFYING CHECK FOR INTERCHANGEABILITY

DRG. No. D/105638/08/09

SERIES REF	8300
QUANTITY/UNIT	-
ASSEMBLED ON	/05680

DRAWING COMPLIES WITH B S 308 AND B S 3939

3rd ANGLE PROJECTION

REMOVE ALL BURRS & SHARP EDGES UNLESS OTHERWISE STATED

WORK TO DIMENSIONS

ISSUE NO	DATE	CHANGE NO	CLASS	CHECKED	DESCRIPTION OF CHANGE
A					
					REF 138 C. 8900/55 TAN 1008
					D1 ADDED TO DRG NUMBER
2					AJH 138 & TANS - 226 261
3					FSB W-3731 RBG.27 D10 ADDED V19 AND I WAS CONTD TO IC12.V4 TAN 261 238
					GRID SE R27 WAS 4702 D11,12,13 ADDED D10 13V BZX79C DELETED - D4,5 D9 WAS -16,7 A.S.9 TAN 8900/497

DRAWN RMO 7/7/82

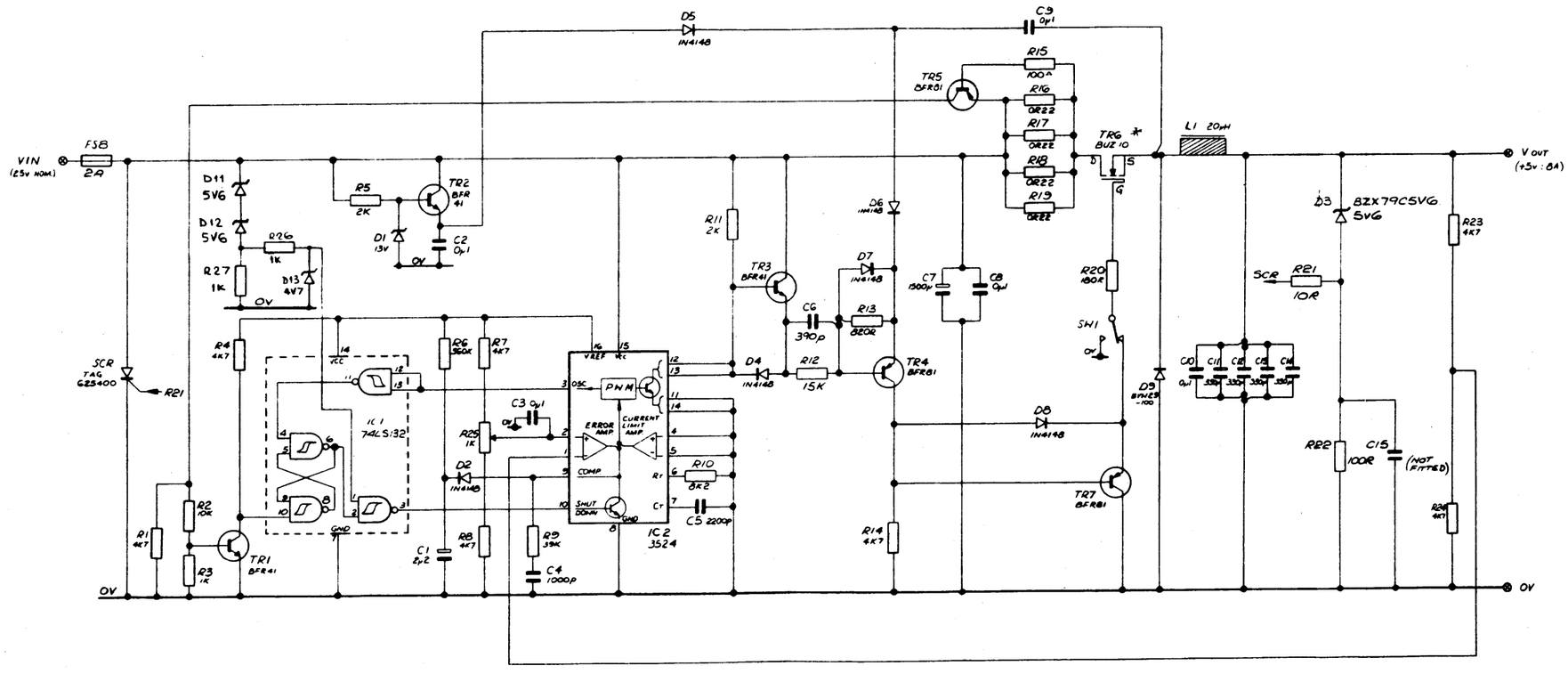
CHECKED R P H 82

CERT'D

TRACED

CHECKED

WEIGHT | DATE



STATIC SENSITIVE DEVICE'S DENOTED THUS *

8900 +5V Switching Regulator Circuit Diagram

Drawing 10

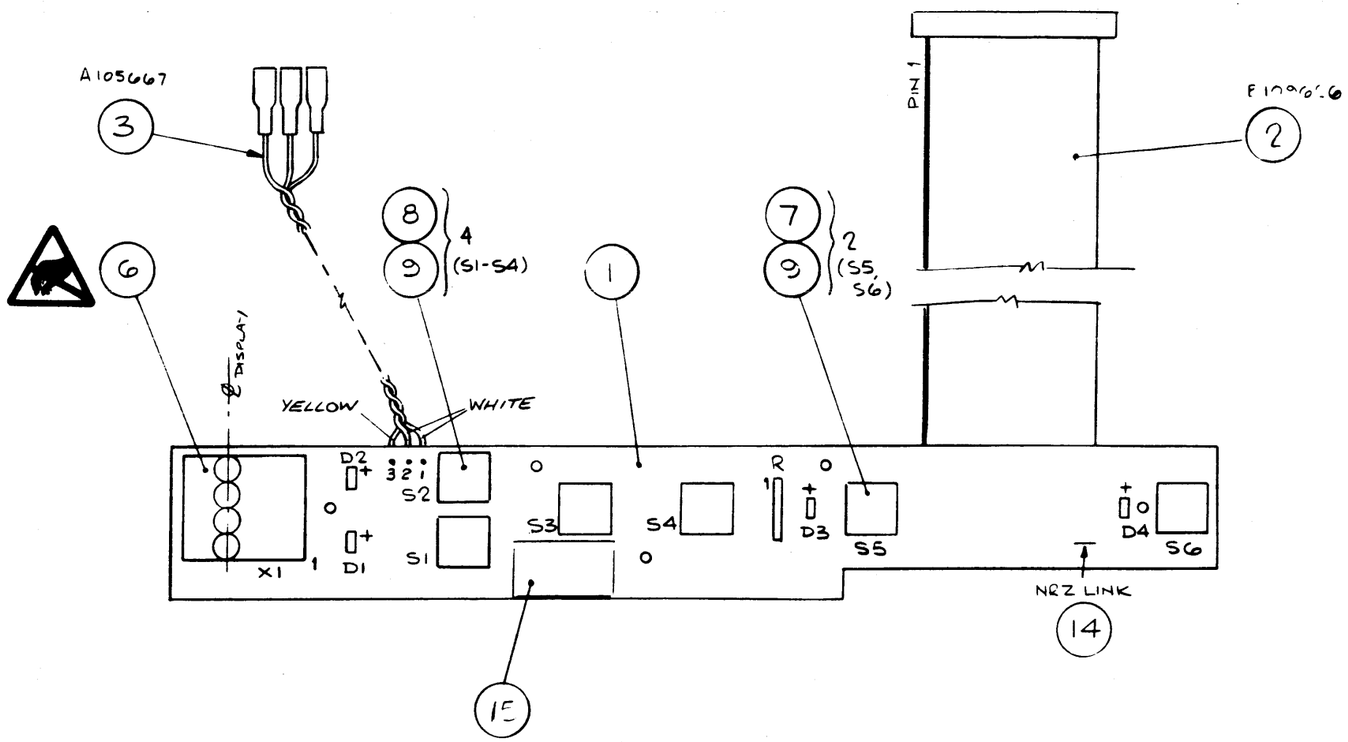
DRG No **C 102510**

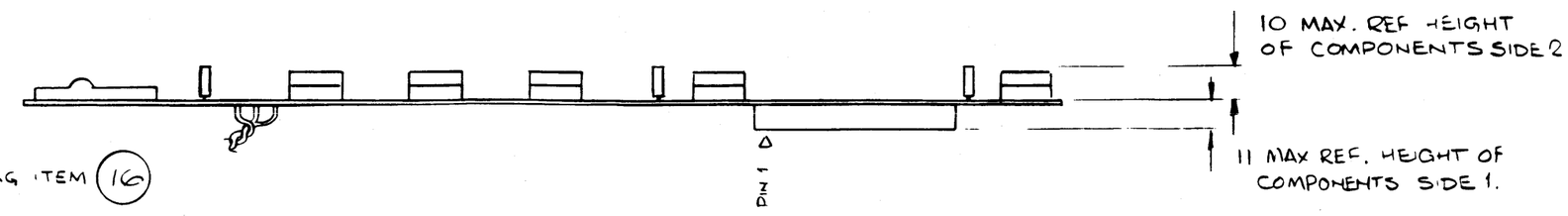
	2	3	4	5	6	7	8	9	10	11
SERIES REF	8200	8500								
QUANTITY/UNIT										
ASSEMBLED ON										

DRAWING COMPLIES WITH BS 308 AND BS 3939

3rd ANGLE PROJECTION **REMOVE ALL BURRS & SHARP EDGES UNLESS OTHERWISE STATED** **WORK TO DIMENSIONS**

ISSUE NO	DATE	CHANGE NO	CLASS	CHECKED	DESCRIPTION OF CHANGE
A					
B					ISS B AIN
1					PRODUCTION RELEASE
					NOTE 3 ADDED 8900/483





NOTE'S

1. ASSEMBLY TO BE PLACED IN BAG ITEM (16)
2. LOOMS ARE FITTED ON SOLDER SIDE.
3. L.E.D.'S (D1, D2, D3, D4) TO STAND OFF BOARD BY 1,0 TO 1,5MM.

PWB DRILLING - C109516
CIRCUIT DIAG. - C109518

8900 NRZ Switch Fascia PWB

Drawing 11

DRAWN	GJ	MAR 83
CHECKED		
CERT'D		
TRACED		
CHECKED		
WEIGHT		DATE

AARQUE 0082 83

WHEN MODIFYING, CHECK FOR INTERCHANGEABILITY

A2

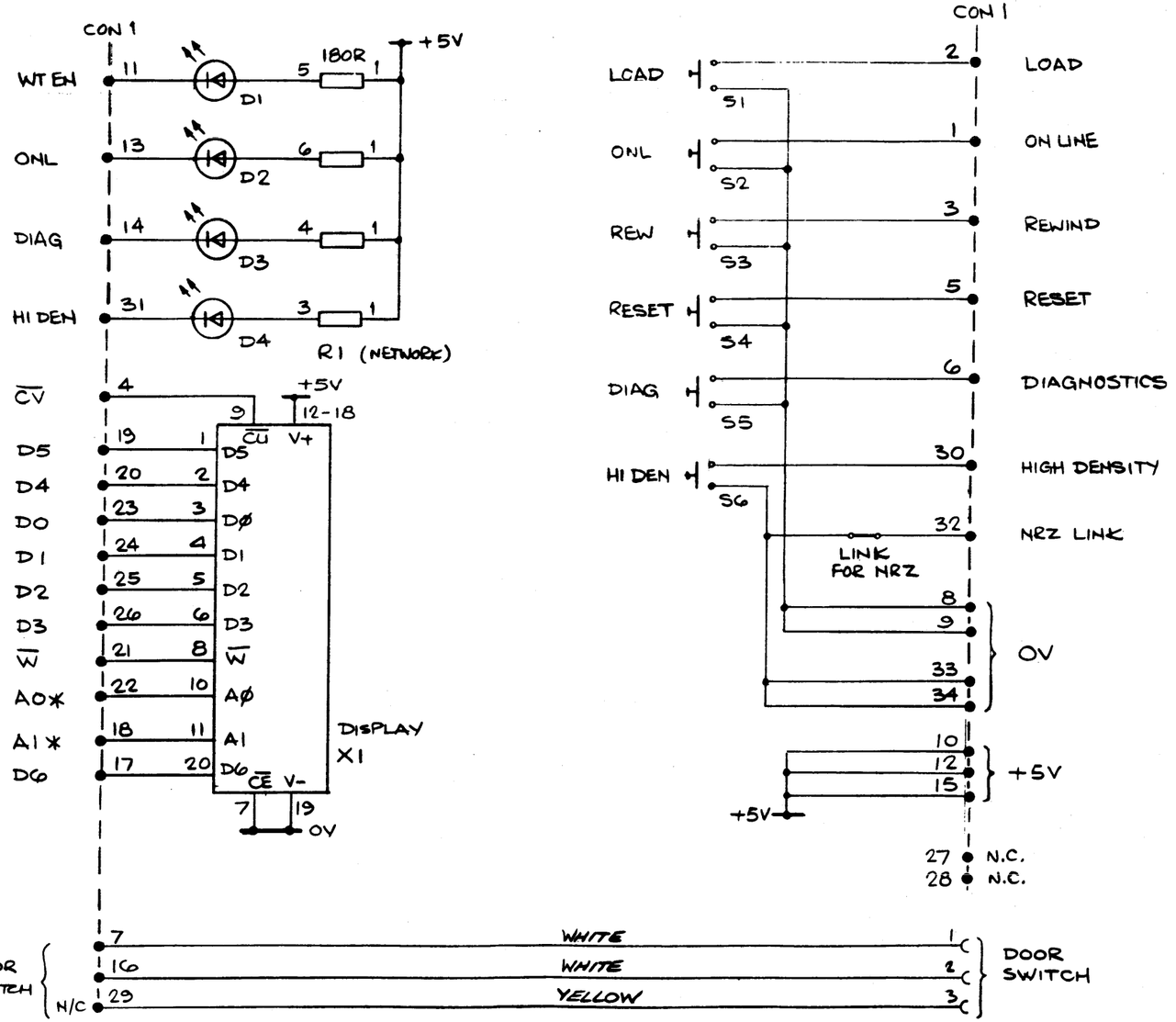
DRG. No. C 109518

ISSUE NO.	DATE	CHANGE NO	CLASS	CHECKED	DESCRIPTION OF CHANGE
D	MAY 87				
B	MAY 87				DOOR SWITCH N/C ADDED ISS B A/N
1	83				REACTION LEVENG

SERIES REF
QUANTITY/UNIT
ASSEMBLED ON

DRAWING COMPLIES WITH B.S. 308 AND B.S. 3939

3rd ANGLE PROJECTION — REMOVE ALL BURRS & SHARP EDGES UNLESS OTHERWISE STATED — WORK TO DIMENSIONS



DRAWN	JW	MAR 83
CHECKED		
CERT'D		
TRACED		
CHECKED		
WEIGHT		DATE

WHEN MODIFYING, CHECK FOR INTERCHANGEABILITY.

8900 NRZ Front Switch Fascia
Circuit Diagram

Drawing 12

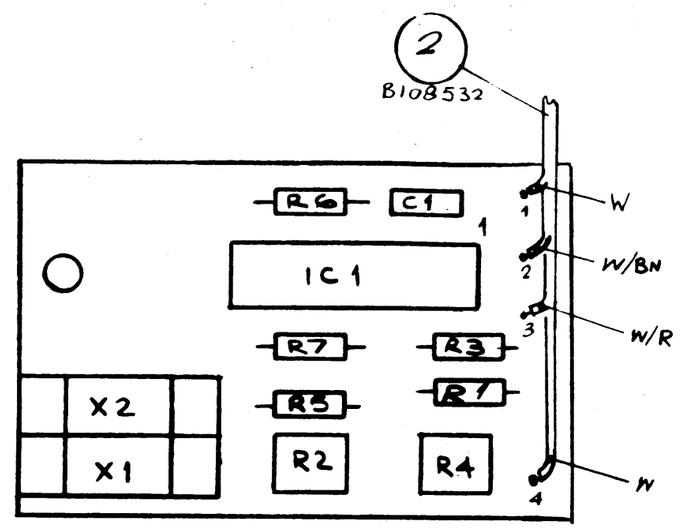
A2

DRG. No.	SERIES REF.	8800
B 108533	QUANTITY/UNIT	1
	ASSEMBLED ON	B103708

DRAWING COMPLIES WITH B.S. 308 AND B.S. 3939

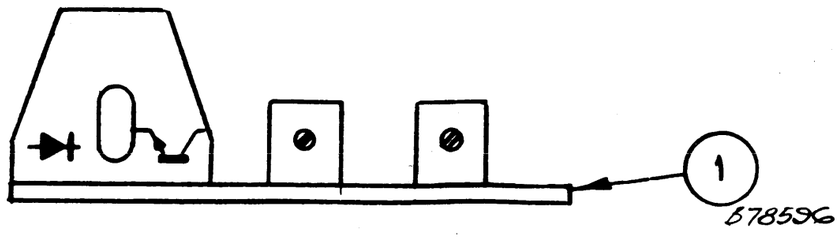
3rd ANGLE PROJECTION **REMOVE ALL BURRS & SHARP EDGES UNLESS OTHERWISE STATED** **WORK TO DIMENSIONS**

ISSUE NO.	DATE	CHANGE NO.	CLASS	CHECKED	DESCRIPTION OF CHANGE
1	3 = 82				INITIAL ISSUE



NOTE.

BEFORE ASSY TO PCB, COMPONENTS X1, X2 TO BE ALIGNED AND TEMPORARILY CLAMPED TOGETHER POSITION SQUARE WITH SIDES OF BOARD BEFORE SOLDERING IN POSITION.



DRAWN	PDJ	5/78
CHECKED	[illegible]	5 9 78
CERT'D.		
TRACED		
CHECKED		
WEIGHT		DATE

BOT/EOT Sensors PCA

Drawing 13

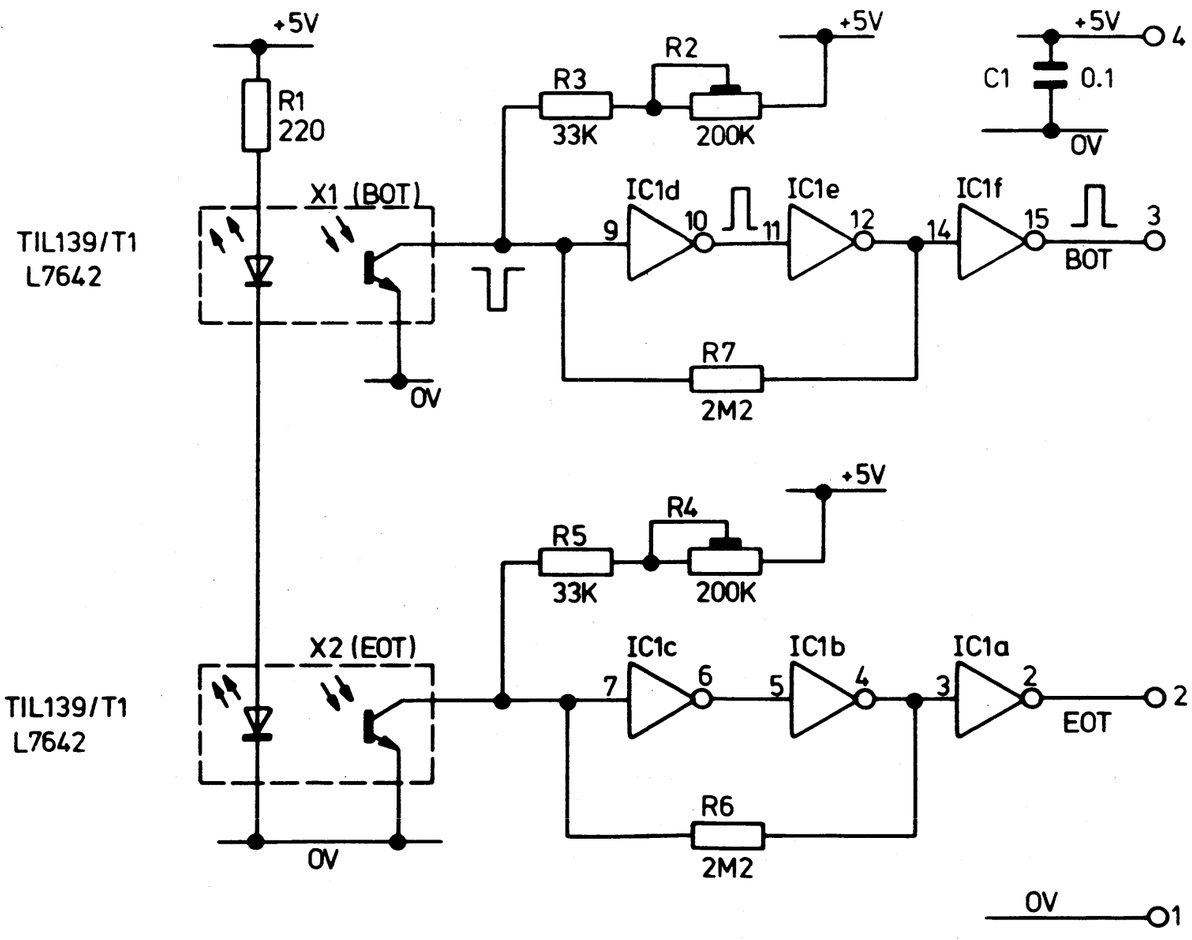
A3

DRG. No.		SERIES REF	8800
B78598		QUANTITY/UNIT	
		ASSEMBLED ON	B78590

DRAWING COMPLIES WITH B S 308 AND B S 3939

ISSUE NO.	DATE	CHANGE NO.	CLASS	CHECKED	DESCRIPTION OF CHANGE
2	15 80	4157			REDRAWN PCO
3	31-8-84	4202			R1 220 WAS 100 TAN 929 (ASSY STATE 5 HEAD ASSY)

3rd ANGLE PROJECTION **REMOVE ALL BURRS & SHARP EDGES UNLESS OTHERWISE STATED** **WORK TO DIMENSIONS**



NOTE,
IC1 = 4049
+5V ON PIN 1
0V ON PIN 8

DRAWN	P.D.J.	
CHECKED		
CERT'D.		
TRACED	C.G.T.	
CHECKED		
WEIGHT		DATE

BOT/EOT Sensors
Circuit Diagram

Drawing 14

A3

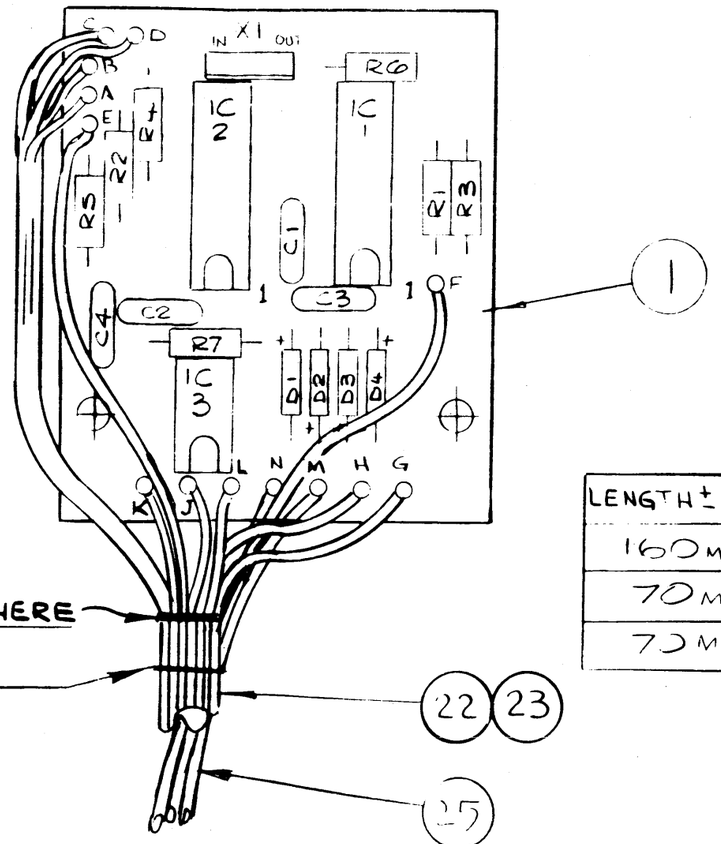
DRG. No. **B 18970**

SERIES REF	28800
QUANTITY UNIT	ea
ASSEMBLED ON	C 28758

DRAWING COMPLIES WITH BS 308 AND DES STD

ISSUE NO	DATE	CHANGE NO	CLASS	CHECKED	DESCRIPTION OF CHANGE
2	8.5.80	42081			REDRAWN AS 'C' SIZE NEW LAYOUT TO TS 1116

3rd ANGLE PROJECTION REMOVE ALL BURRS & SHARP EDGES UNLESS OTHERWISE STATED WORK TO DIMENSIONS



(1)

(24)

LACE LOOMS TOGETHER HERE

TEMPORARY TIE FOR 3 FLYING LEADS FROM PINS F.N.M.

(22) (23)

(25)

NOTE.
FOR CIRCUIT DIAGRAM, SEE C78978

CONNECTION TABLE

LOOM ITEM	WIRE COLOUR	DESTINATION
23	W/V	D
23	W/B	C
23	W/GN	B
23	W/R	A
22	W/BK	E
22	W/GN	G
22	W/R	H
22	W/Y	J
22	W/O	K
22	W/B	L
LENGTH ±15		
160MM	25	W F
70MM	25	W N
70MM	25	W M

DRAWN	PAG	9-12-80
CHECKED		
CERT'D		
TRACED		
CHECKED		
WEIGHT		DATE

Capacitor Sensor and Limit Switch

Drawing 15

A3

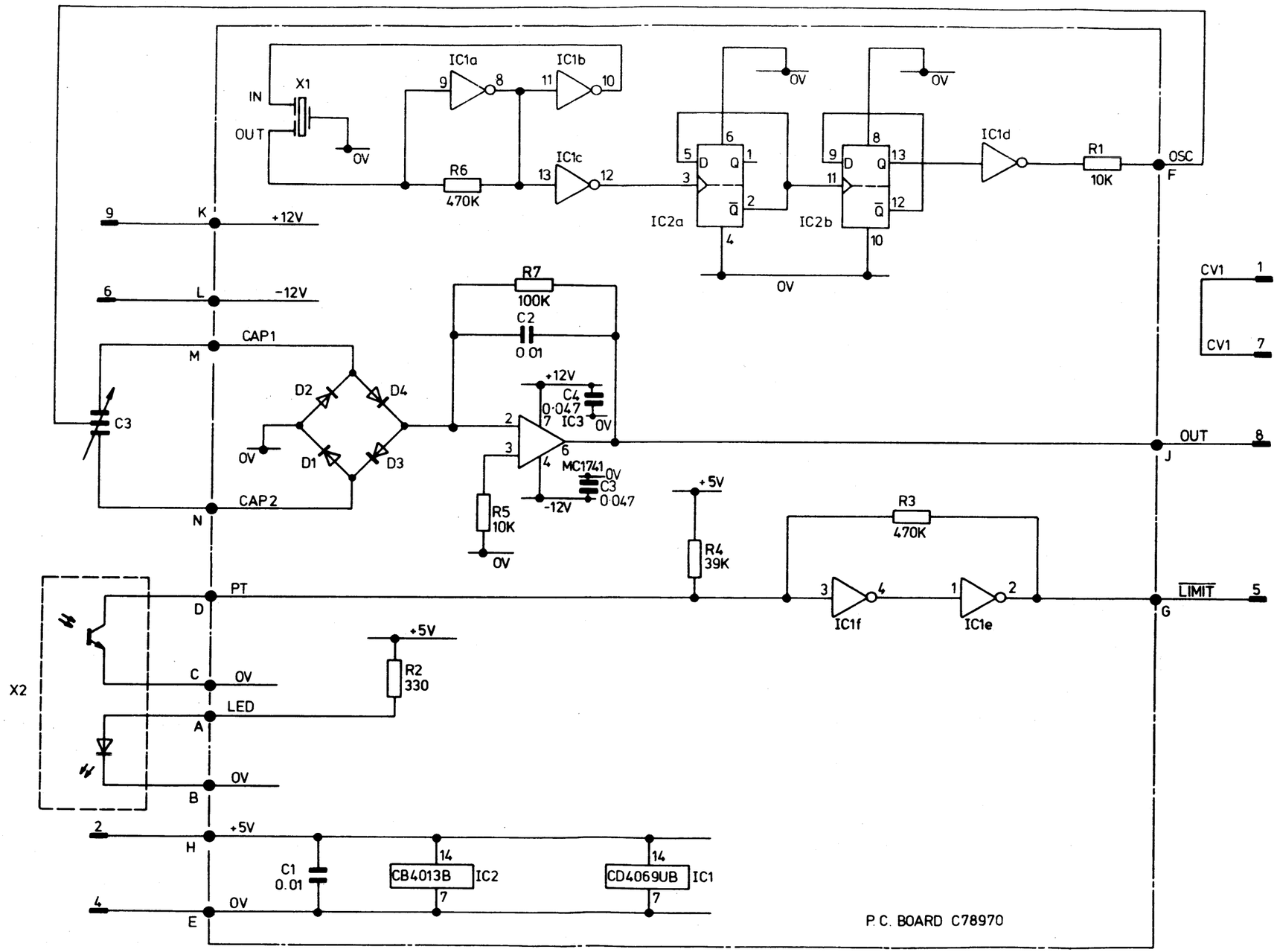
DRG No C 78978/02 & /03

SERIES REF 8800
QUANTITY UNIT
ASSEMBLED ON C78970

DRAWING COMPLIES WITH B.S. 308 AND B.S. 3939

3rd ANGLE PROJECTION — REMOVE ALL BURRS & SHARP EDGES UNLESS OTHERWISE STATED — WORK TO DIMENSIONS

ISSUE NO	DATE	CHANGE NO	CLASS	CHECKED	DESCRIPTION OF CHANGE
2	15 Sep 82	4			REDRAWN PCO MOD 1
3	29 Aug 82	2081			IC1 PIN N°S REALLOCATED C3 & C4 ADDED 102603 VAS 01



DRAWN	P.D.J.	
CHECKED		
CERT'D		
TRACED	C.G.T.	
CHECKED		
WEIGHT		DATE

WHEN MODIFYING, CHECK FOR INTERCHANGEABILITY

Capacitor Sensor and Limit Switch Circuit Diagram

Drawing 16

A2

DRG. No **D 109530**

SERIES REF
QUANTITY/UNIT
ASSEMBLED ON

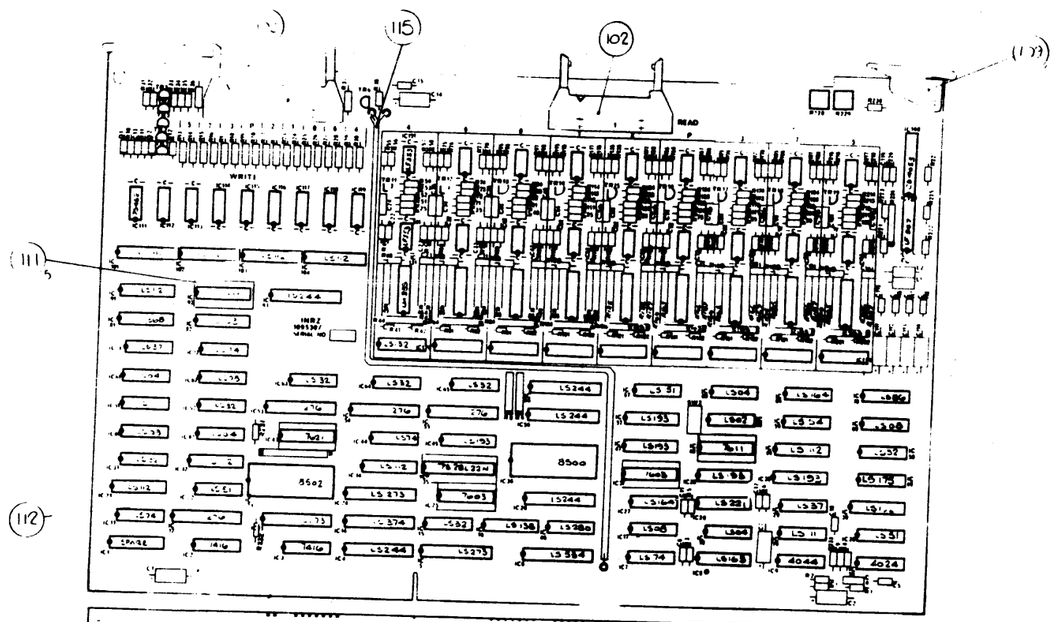
DRAWING COMPLIES WITH BS 308 AND BS 3939

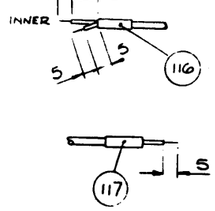
DB	ISSUE NO	DATE	CHANGE NO	CLASS	CHECKED	DESCRIPTION OF CHANGE
						ASSY TO 155 B ARTWORK 155 C CCT DIA
C						ADV. 11"BOOK ONLY

3rd ANGLE PROJECTION

REMOVE ALL BURRS & SHARP EDGES UNLESS OTHERWISE STATED

WORK TO DIMENSIONS





DETAIL OF PREPARATION OF CO-AX

NOTES.

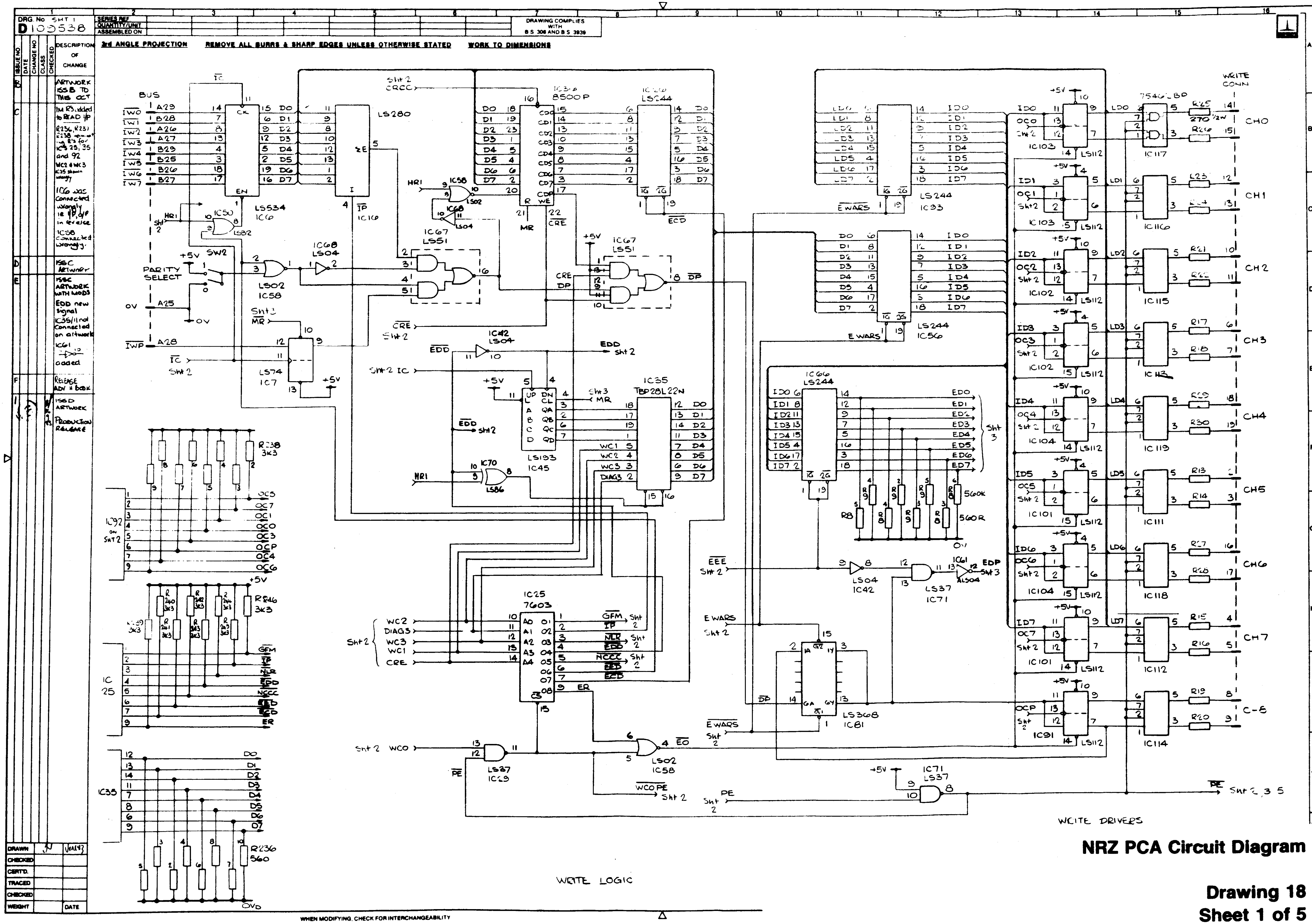
1. COMMON PINS ON RESISTOR NETWORKS SHOWN THUS :-

DRAWN	P.G.G.	
CHECKED		
CERT'D		
TRACED		
CHECKED		
WEIGHT		DATE

WHEN MODIFYING CHECK FOR INTERCHANGEABILITY

NRZ PCA

Drawing 17

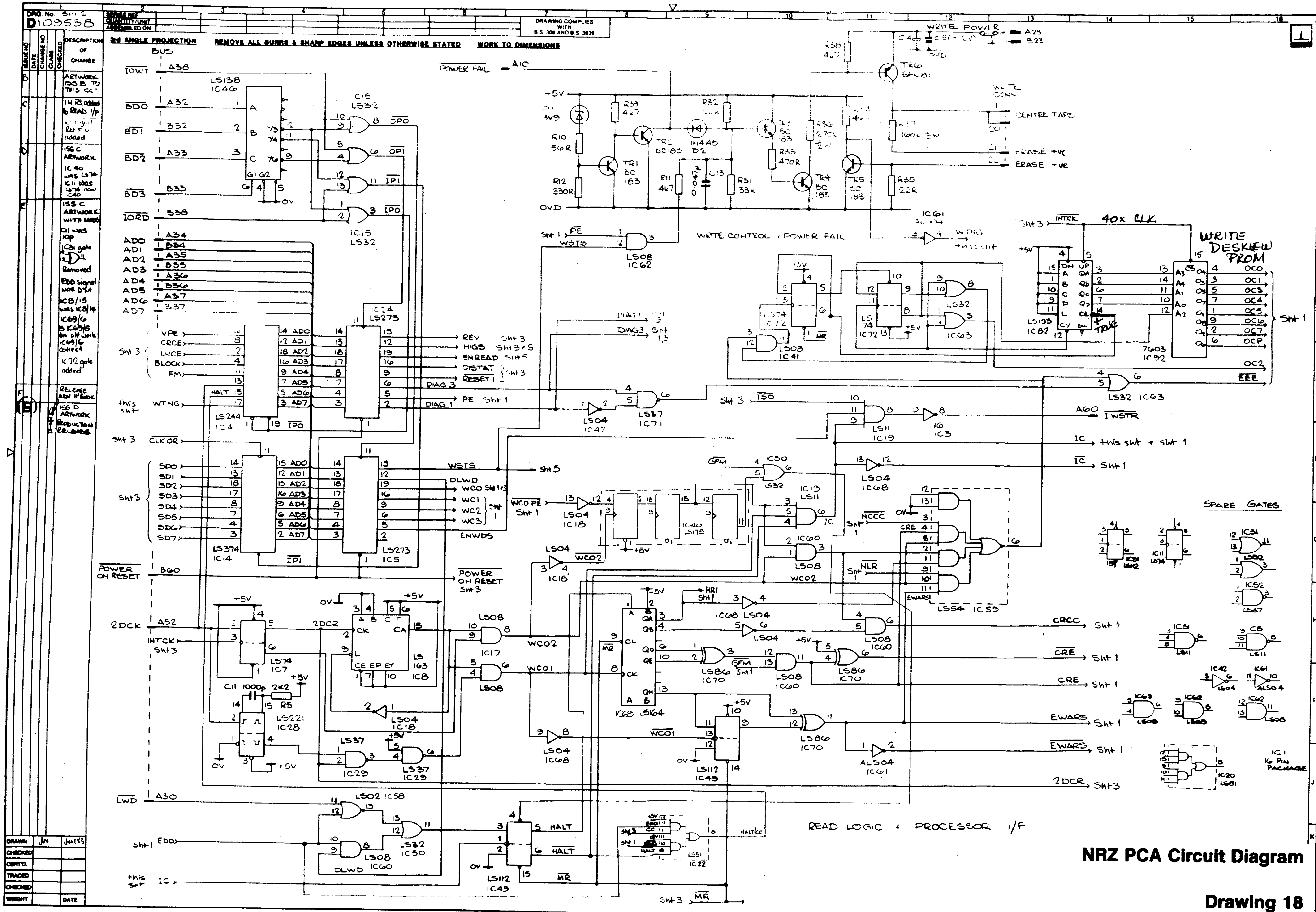


WRITE LOGIC

WRITE DRIVERS

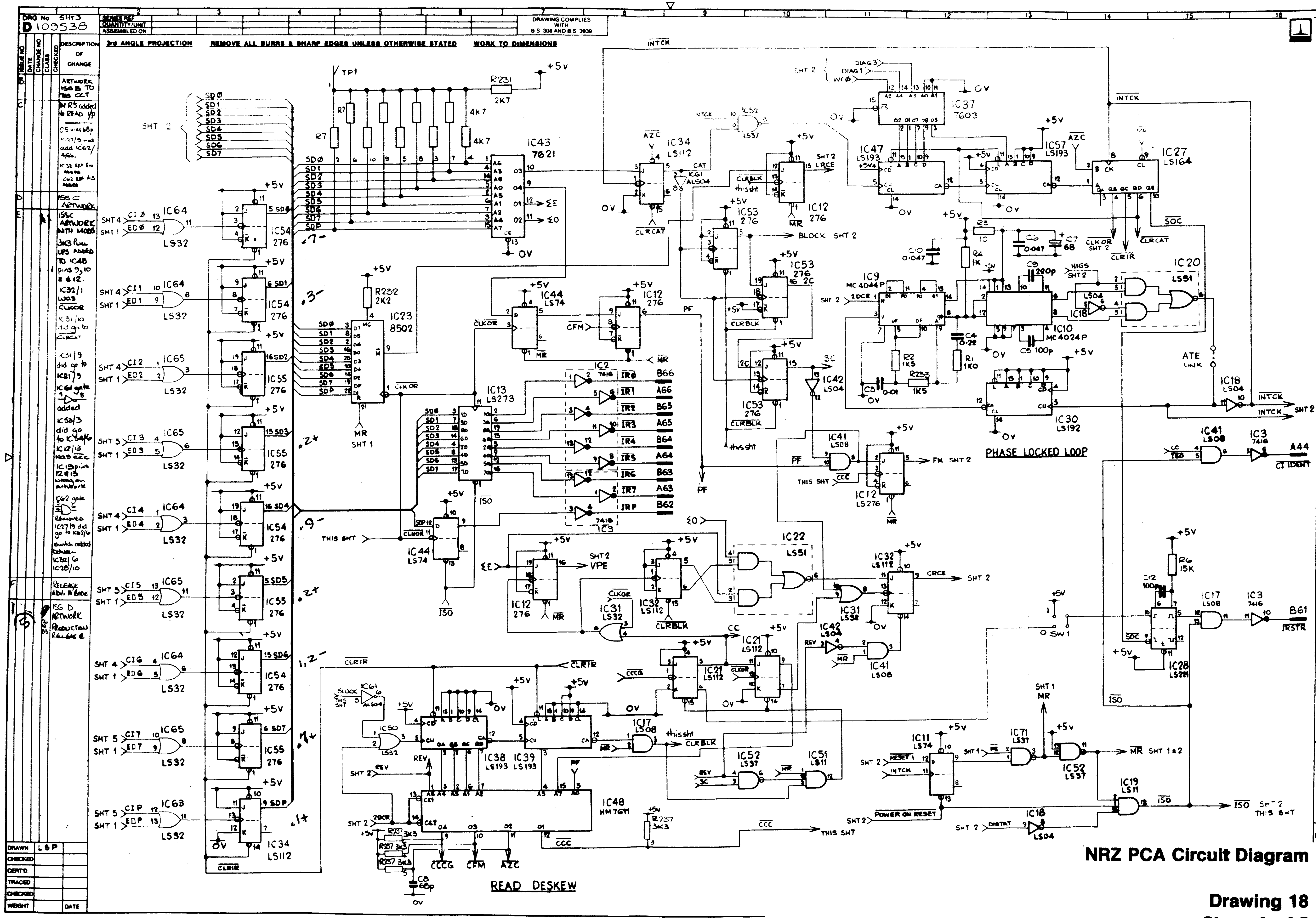
NRZ PCA Circuit Diagram

Drawing 18
Sheet 1 of 5



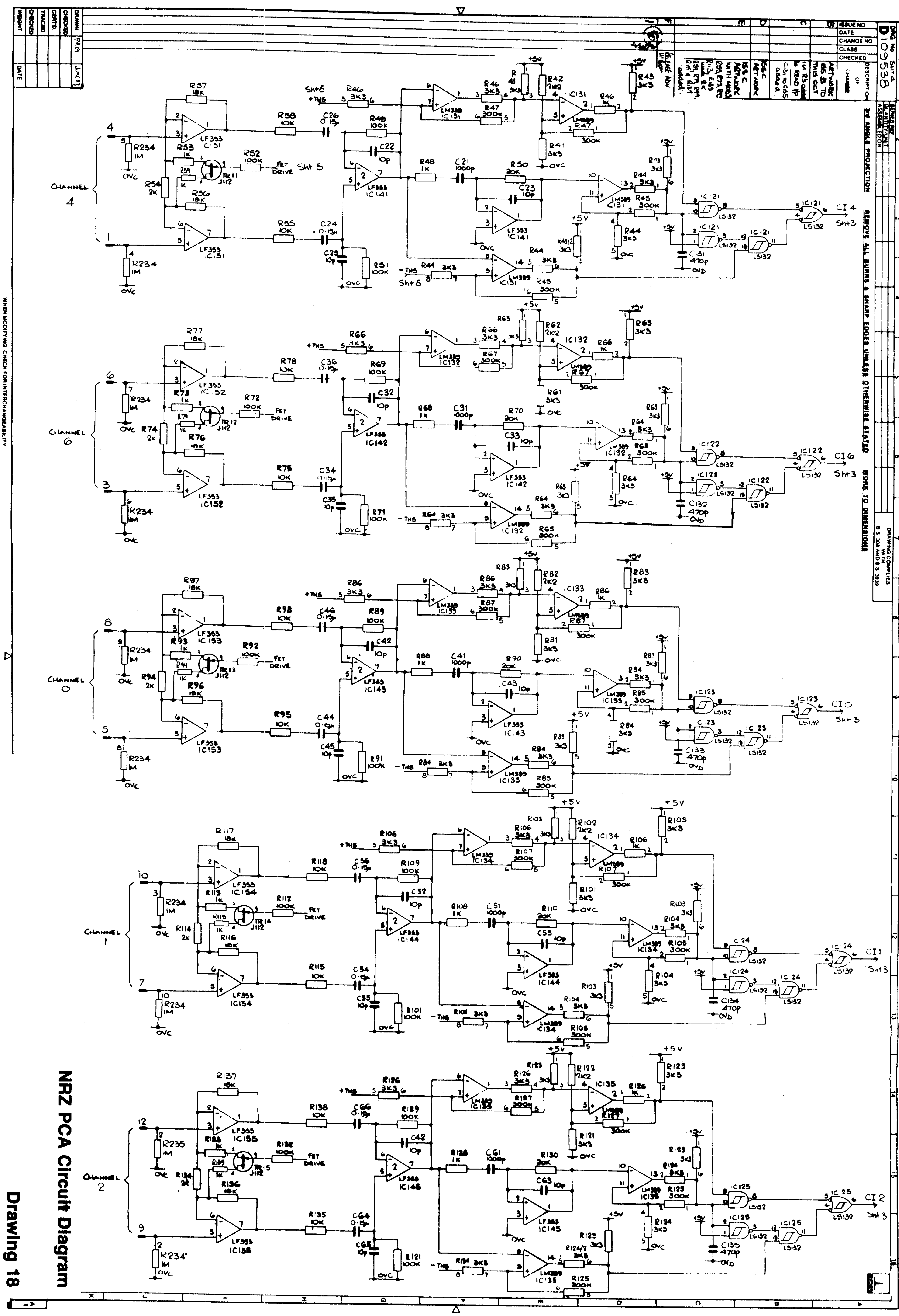
NRZ PCA Circuit Diagram

Drawing 18
Sheet 2 of 5



Drawing 18

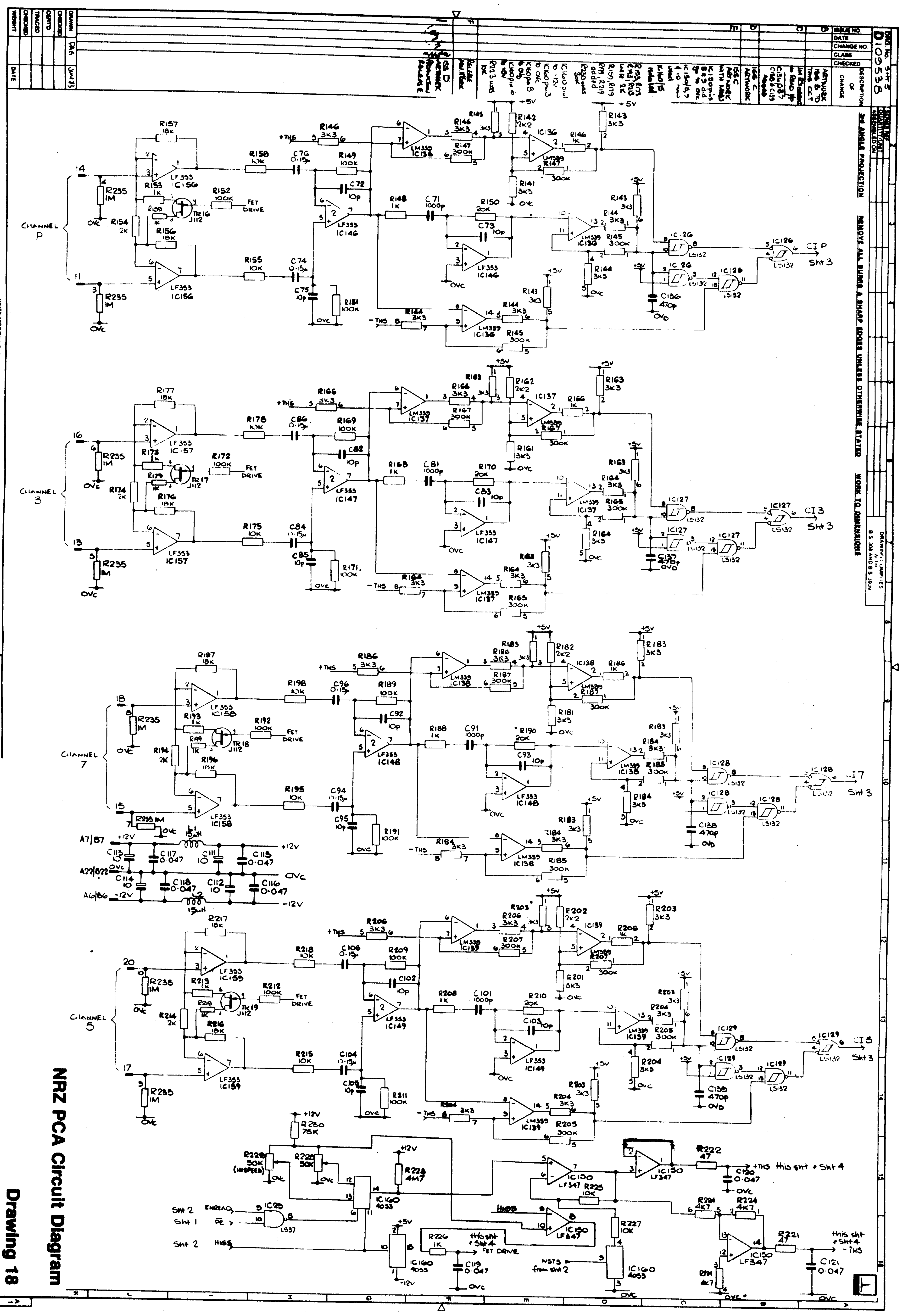
Sheet 3 of 5



NRZ PCA Circuit Diagram

Drawing 18

Sheet 4 of 5

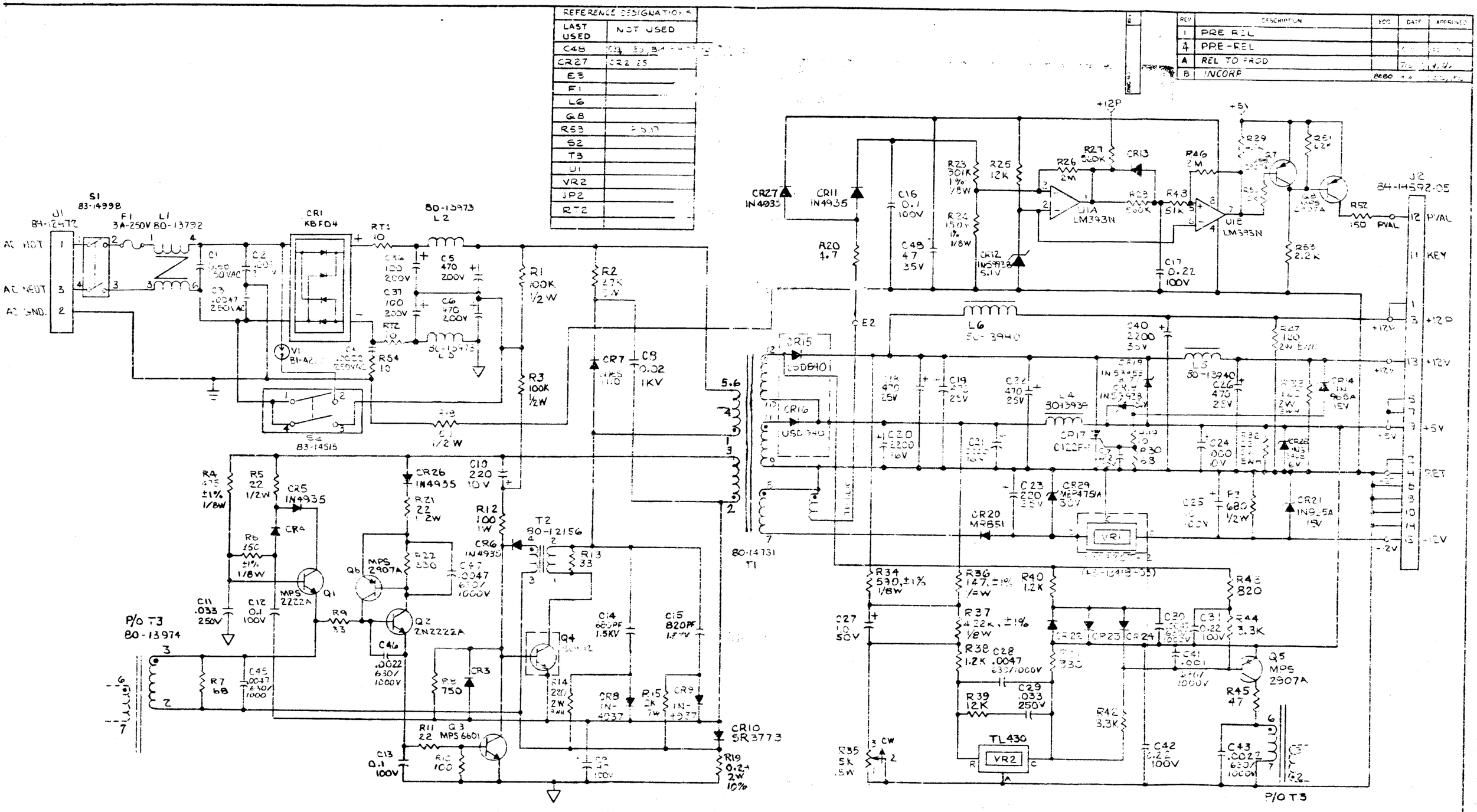


NRZ PCA Circuit Diagram

Drawing 18
Sheet 5 of 5

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C49	
CR27	CR22-25
E3	
F1	
L6	
Q8	
R53	
S2	
T3	
U1	
VR2	
JP2	
RT2	

REV	DESCRIPTION	ECO	DATE	APPROVED
1	PRE REL			
4	PRE-REL			
A	REL TO PROD			
B	INCORP	8680		

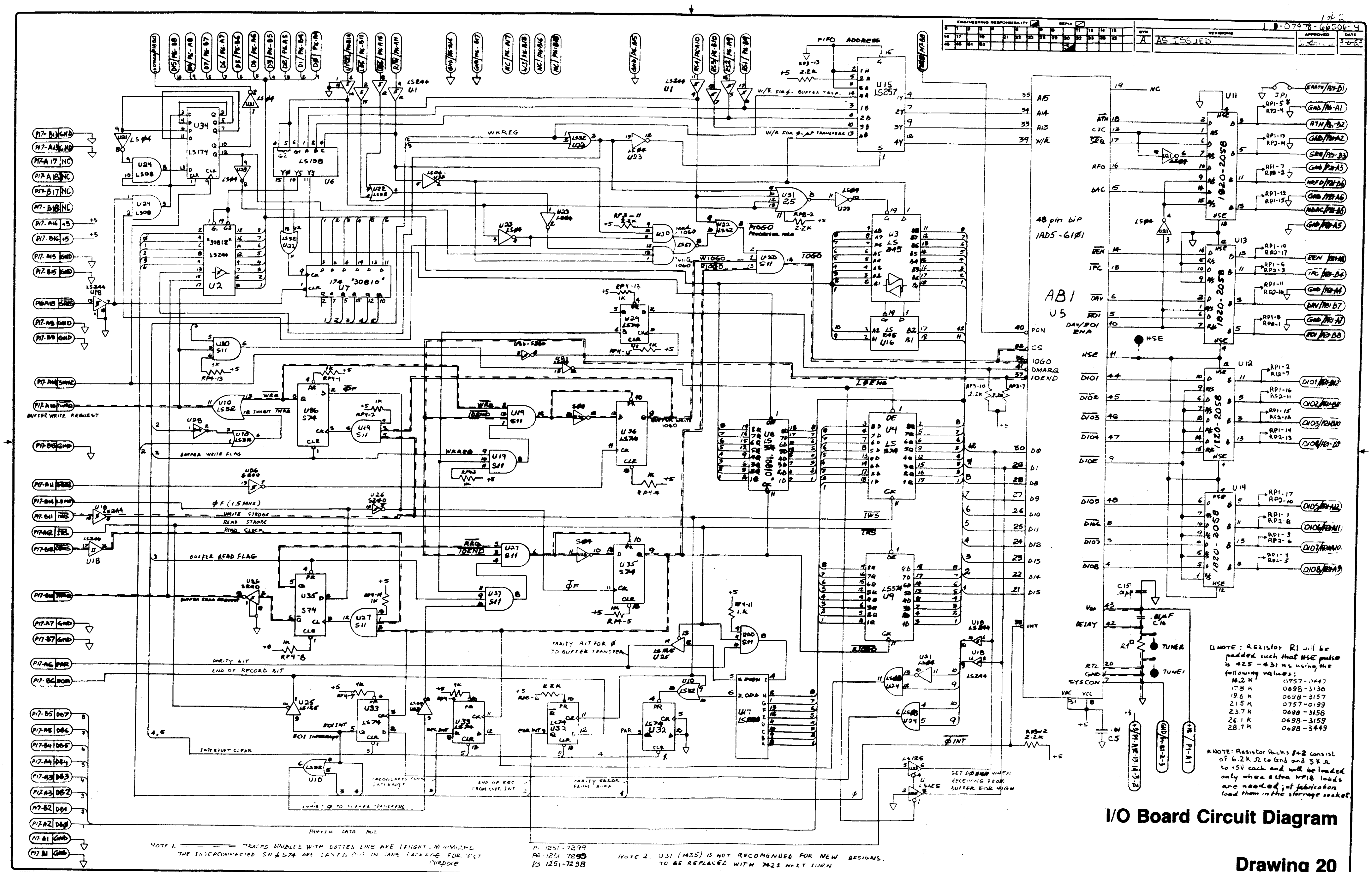


1. ALL CAPACITOR VALUES ARE IN MICROFARADS. VOLTAGE RATINGS ARE IN DC.
   ALL DIODES ARE 1N4448.
   RESISTORS ARE IN OHMS, ±5% ¼W.

NOTES: UNLESS OTHERWISE SPECIFIED:

Interface Power Supply
Circuit Diagram

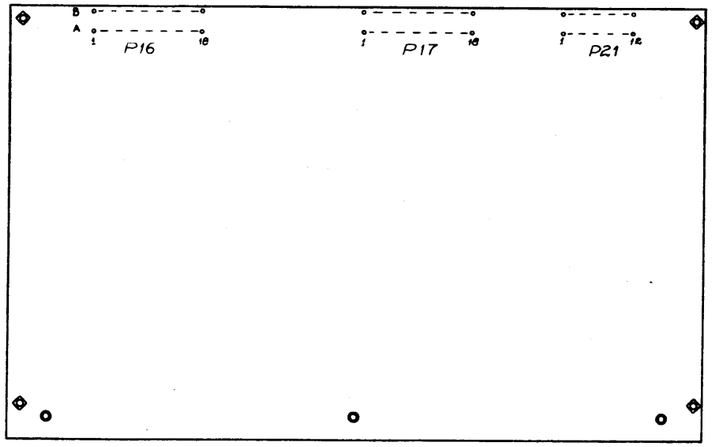
Drawing 19



I/O Board Circuit Diagram

Drawing 20

Sheet 1 of 2



P16

A1	+12v	B1	GND	
A2	+5v	B2	GND	
A3	+5v	B3	GND	
A4	DØ	B4	D1	
A5	D2	B5	D3	
A6	D4	B6	D5	
A7	D6	B7	D7	
A8	D14	B8	D15	
A9	RS2	B9	RS1	
A10	RS4	B10	RS3	
A11	R/$\overline{W}$	B11	$\overline{LDS}$	
A12	+5v	B12	I/O DTACK	
A13	+5v	B13		
A14	+5v	B14	T/F SEL	
A15	$\overline{UDS}$	B15	GND	
A16	GND	B16		
A17	——	B17	GND	
A18	SYS. RESET	B18		

P17

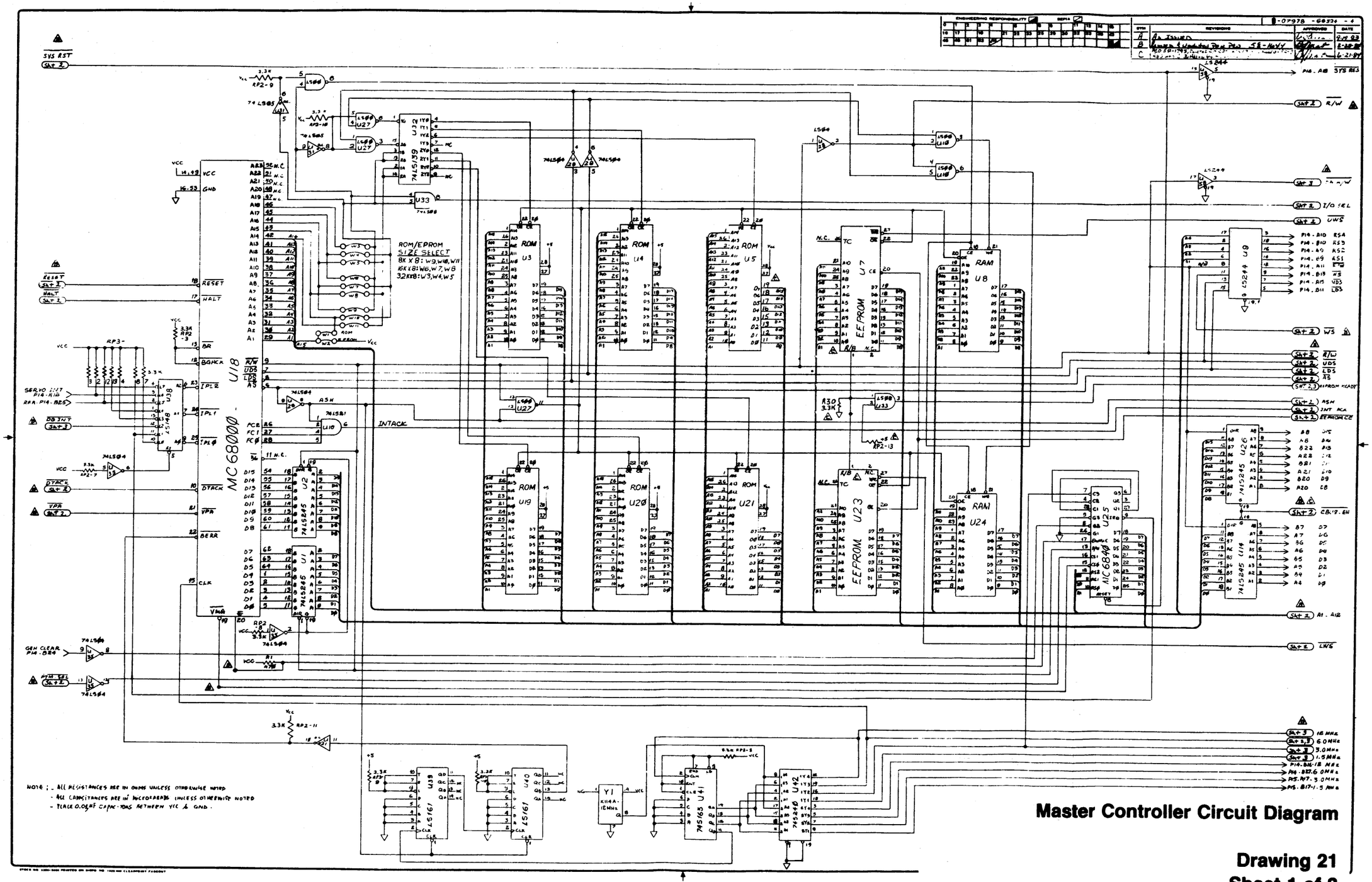
A1	GND	B1	GND	
A2	$\overline{DB0}$	B2	$\overline{DB1}$	
A3	$\overline{DB2}$	B3	$\overline{DB3}$	
A4	$\overline{DB4}$	B4	$\overline{DB5}$	
A5	$\overline{DB6}$	B5	$\overline{DB7}$	
A6	PAR	B6	$\overline{EOR}$	
A7	GND	B7	GND	
A8	——	B8	PWRGD	
A9	GND	B9	GND	
A10	$\overline{IWRQ}$	B10	$\overline{IRRQ}$	
A11	$\overline{DBRS}$	B11	$\overline{IWS}$	
A12	$\overline{IRS}$	B12	$\overline{DBWS}$	
A13	GND	B13	GND	
A14	3MHz	B14	1.5 MHz	
A15	GND	B15	GND	
A16	+5v	B16	+5v	
A17	——	B17	——	
A18	——	B18	——	

P21

A1	GND. LOGIC	B1	SHIELD	
A2	GND	B2	ATN	
A3	GND.	B3	SRQ	
A4	GND.	B4	IFC	
A5	GND.	B5	NDAC	
A6	GND.	B6	NRFD	
A7	GND	B7	DAV	
A8	REN	B8	EOI	
A9	DIO 8	B9	DIO 4	
A10	DIO 7	B10	DIO 3	
A11	DIO 6	B11	DIO 2	
A12	DIO 5	B12	DIO 1	

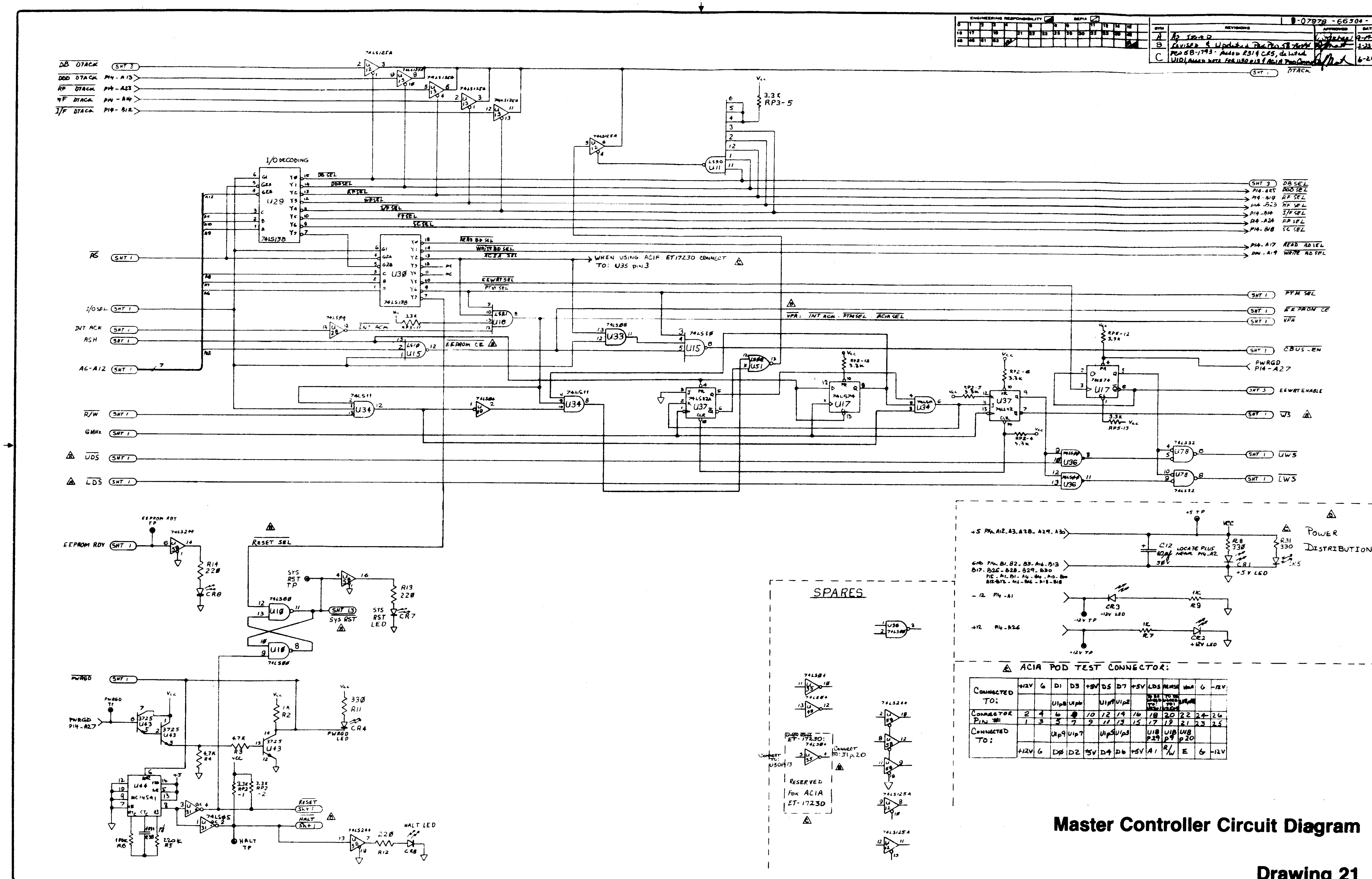
I/O Board Circuit Diagram

Drawing 20
Sheet 2 of 2



Master Controller Circuit Diagram

Drawing 21
Sheet 1 of 3

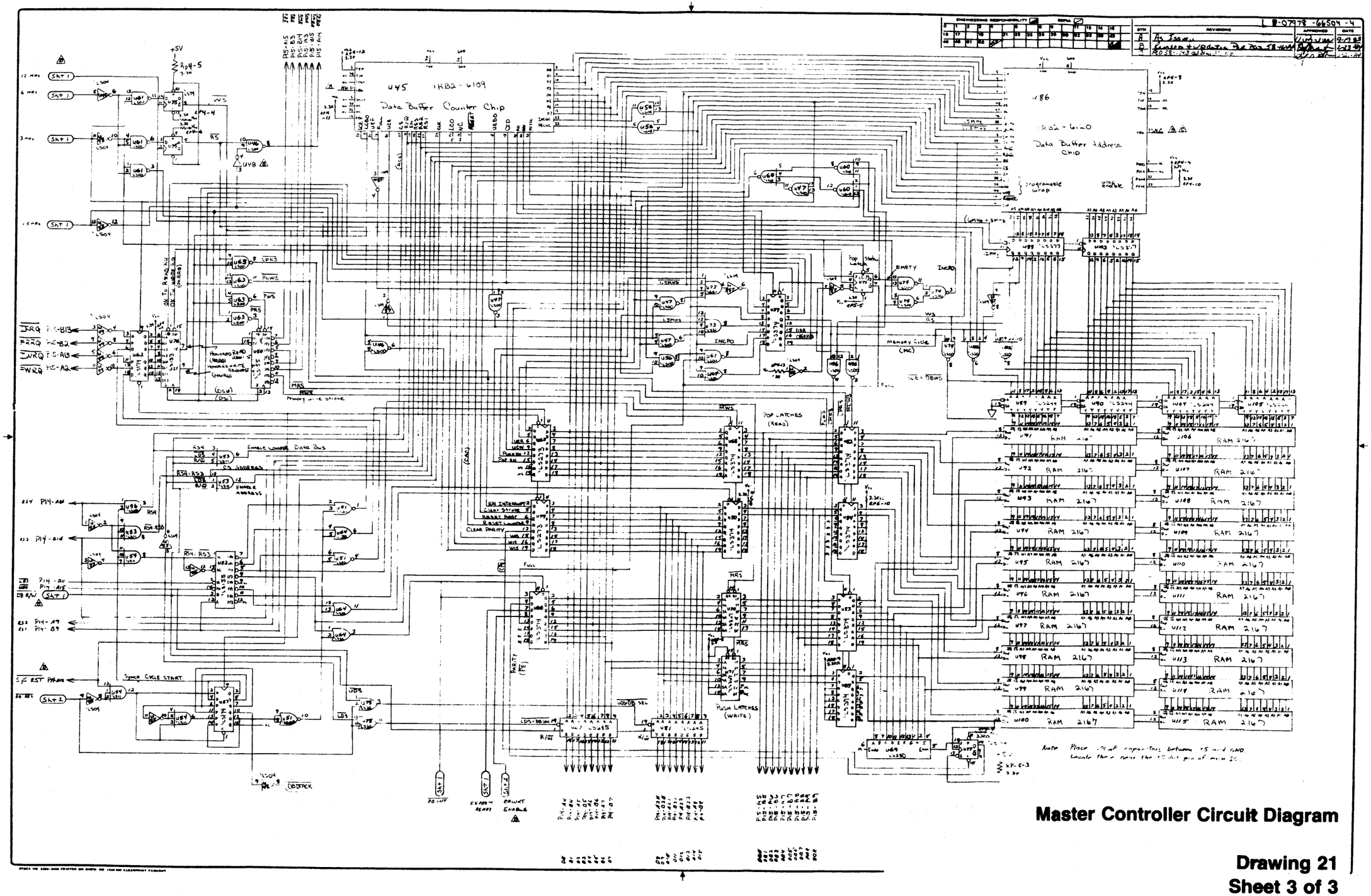


ACIA POD TEST CONNECTOR:

Connected To:	+12V	G	D1	D3	+5V	D5	D7	+5V	LDS	[illegible]	[illegible]	G	-12V
			U1p8	U1p6		U1p4	U1p2		[illegible]	[illegible]	[illegible]		
Connector Pin #	2	4	6	[illegible]	10	12	14	16	18	20	22	24	26
	1	3	5	7	9	11	13	15	17	19	21	23	25
Connected To:			U1p9	U1p7		U1p5	U1p3		U18 p29	U18 p9	U18 p20		
	+12V	G	DØ	D2	+5V	D4	D6	+5V	A1	R/W	E	G	-12V

Master Controller Circuit Diagram

Drawing 21
Sheet 2 of 3


U45 IRB2-6109
Data Buffer Counter Chip
U86 IRB1-6110
Data Buffer Address Chip
Programable Wrap
Writable
Master Controller Circuit Diagram
Drawing 21
Sheet 3 of 3

D-07914-1265X-4

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		11-7-83
B	SEE CHANGE PA2 PER ECO 58-1509		11-18-83
D	SEE CHANGE PA3 PER ECO 58-1647		1/6/84

INTERFACE DECODER

MASTER CONTROLLER DATA BUS

FRONT PANEL DISPLAY

VIRTUAL BUTTON REGISTER

LED REGISTER

FORMATTER ENABLE REGISTER

COMMAND REGISTER

BUTTON BUFFER

VIRTUAL LEDS

DRIVE STATUS BUFFER

VIRTUAL DISPLAY 4X8 REGISTERS

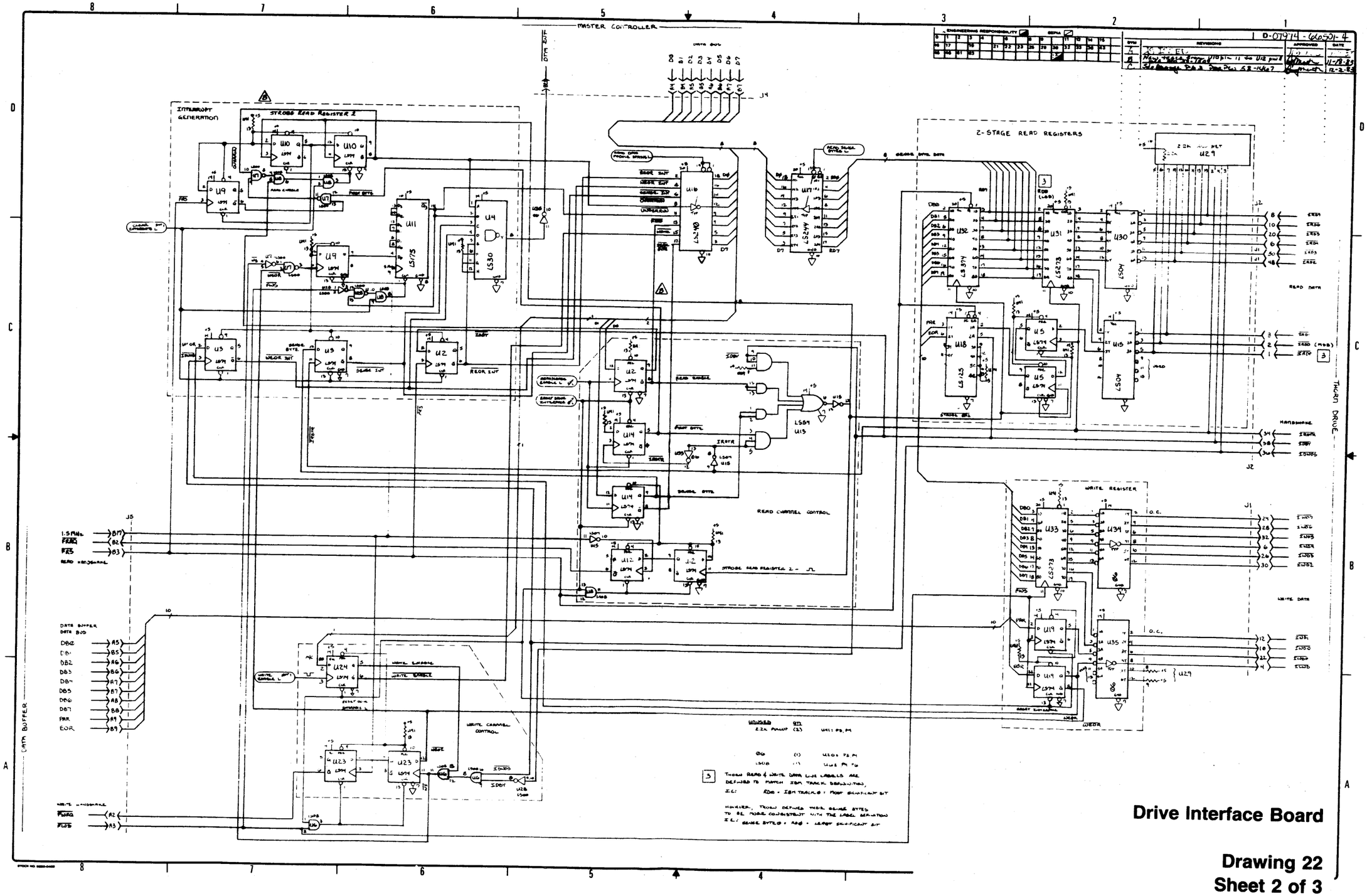
GO PULSE

BYPASS CAPACITORS

2 WHILE ALL PULLUPS ARE LABELED U41 - PA15, IN REALITY 2 ADDITIONAL RESISTORS, U42 - M,P,B ARE CONNECTED IN PARALLEL = 733 Ω COMBINED

Drive Interface Board

Drawing 22
Sheet 1 of 3



Drive Interface Board

Drawing 22
Sheet 2 of 3

J1	
PL1 INTERFACE	
MNEMONIC	8900
IFBY	2 (1)
ILWD	4 (3)
IWD4	6 (5)
IGO	8 (7)
IWDØ	10 (9)
IWD1	12 (11)
IDLG	14 (13)
IREV	18 (17)
IREW	20 (19)
IWDP	22 (21)
IWD7	24 (23)
IWD5	26 (25)
IWD6	28 (27)
IWD2	30 (29)
IWD3	32 (31)
IWRT	34 (33)
READ THRESHOLD E	36 (35) RESERVED
IEDIT	38 (37)
IERASE	40 (39)
IWFM	42 (41)
READ THRESHOLD I	44 48 RESERVED
ITADØ	46 (45)
IRD2	48 (47)
IRD3	50 (49)

J2	
PL2 INTERFACE	
MNEMONIC	8900
IRDP	1 (-)
IRDØ	2 (-)
IRD1	3 (-)
ILDP	4 (-)
IRD4	6 (5)
IRD7	8 (7)
IRD6	10 (9)
IHER	12 (11)
IFMK	14 (13)
IIDENT	16 (15)
IFEN	18 (17)
IRD5	20 (19)
IEOT	22 (21)
IOFL	24 (23)
NRZI	26 (25) RESERVED
IRDY	28 (27)
IRWD	30 (29)
IFPT	32 (31)
IRSTR	34 (33)
IDWDS	36 (35)
IDBY	38 (37)
ISPEED	40 (39)
ICER	42 (41)
IONL	44 (43)
ITAD1	46 (45)
ITAD	48 (47)
THISP	50 (49)

J3	
FRONT PANEL IN	
MNEMONIC	8900
ONLINE	1
LOAD	2
REWIND	3
DC	4
RESET	5
DIAG	6
FP7	7
GND	8
GND	9
FPIØ	10
WT EN L MP	11
FP12	12
ONL L MP	13
DIAG L MP	14
FP15	15
DOOR	16
DD6	17
DB	18
DD5	19
DD4	20
DW	21
DA	22
DDØ	23
DD 1	24
DD 2	25
DD 3	26
FP27	27
FP28	28
DOOR	29
DTOGGLE	30
DENSITY	31
NRZ	32
GND	33
GND	34

J11	
FRONT PANEL OUT	
MNEMONIC	8900
VONLINE	1
VLOAD	2
VREWIND	3
VDC	4
VRESET	5
VDIAG	6
FP7	7
GND	8
GND	9
FPIØ	10
VWT EN L MP	11
FP12	12
VONL L MP	13
VDIAG L MP	14
FP15	15
DOOR	16
VDD6	17
VDB	18
VDD5	19
VDD4	20
VDW	21
VDA	22
VDDØ	23
VDD1	24
VDD2	25
VDD3	26
FP27	27
FP28	28
—	29
VDTOGGLE	30
VDENSITY	31
NRZ	32
GND	33
GND	34

J4			
BUFFER / MC			
PIN #		PIN #	
B1	GND	A1	-12V
B2	GND	A2	+5V
B3	GND	A3	-5V
B4	D1	A4	DØ
B5	D3	A5	D2
B6	D5	A6	D4
B7	D7	A7	D6
B8	D15	A8	DI4
B9	RS1	A9	RS2
B10	RS3	A10	RS4
B11	LDS	A11	R/W
B12	I/O DTACK	A12	—
B13	WS	A13	—
B14	I/F SEL	A14	—
B15	GND	A15	UDS
B16	—	A16	GND
B17	GND	A17	—
B18	SC SEL	A18	SYS RES
B19	—	A19	WT BD SEL
B20	D9	A20	D8
B21	DII	A21	D10
B22	DI3	A22	D12
B23	—	A23	—
B24	GENCLEAR	A24	FP SEL
B25	DTM INT.	A25	—
B26	—	A26	+12V
B27	—	A27	PWRGD
B28	GND	A28	+5V
B29	GND	A29	+5V
B30	GND	A30	+5V

J6			
I/O CNCTR 1			
PIN		PIN	
B1	GND	A1	+12V
B2	GND	A2	+5V
B3	GND	A3	+5V
B4	D1	A4	DØ
B5	D3	A5	D2
B6	D5	A6	D4
B7	D7	A7	D6
B8	D15	A8	DI4
B9	RS1	A9	RS2
B10	RS3	A10	RS4
B11	LDS	A11	R/W
B12	I/O DTACK	A12	+5V
B13	—	A13	+5V
B14	I/F SEL	A14	+5V
B15	GND	A15	UDS
B16	—	A16	GND
B17	GND	A17	—
B18	—	A18	SYS RES

J7			
I/O CNCTR 2			
PIN		PIN	
B1	GND	A1	GND
B2	DB1	A2	DBØ
B3	DB3	A3	DB
B4	DB5	A4	DB
B5	DB7	A5	DB
B6	EOR	A6	PAR
B7	GND	A7	GND
B8	PWRGD	A8	—
B9	GND	A9	GND
B10	IRRQ	A10	IWRQ
B11	IWS	A11	DBRS
B12	DBWS	A12	IRS
B13	GND	A13	GND
B14	1.5 MHZ	A14	3 MHZ
B15	GND	A15	GND
B16	+5V	A16	+5V
B17	—	A17	—
B18	—	A18	—

J8			
I/O CNCTR 3			
PIN		PIN	
B1	SHIELD	A1	GND LOGIC
B2	ANT	A2	GND
B3	SRQ	A3	GND
B4	IFC	A4	GND
B5	NDAC	A5	GND
B6	NRFD	A6	GND
B7	DAV	A7	GND
B8	EIO	A8	REN
B9	DIO 4	A9	DIO8
B10	DIO 3	A10	DIO7
B11	DIO 2	A11	DIO 6
B12	DIO 1	A12	DIO 5

J9			
HPIB OUT-PUT			
PIN		PIN	
1	DIO 1	13	DIO 5
2	DIO 2	14	DIO 6
3	DIO 3	15	DIO 7
4	DIO 4	16	DIO8
5	EIO	17	REN
6	DAV	18	GND
7	NRFD	19	GND
8	NDAC	20	GND
9	IFC	21	GND
10	SRQ	22	GND
11	ATN	23	GND
12	SHIELD	24	GND

J10	
POWER SUPPLY	
MNEMONIC	PIN #
+12V POWER RESTORE	1
GND	2
+12V POWER RESTORE	3
GND	4
+5V	5
GND	6
+5V	7
GND	8
5V	9
GND	10
—	11
PWRGD	12
+12V	13
GND	14
−12V	15

J5			
DATA BUFFER			
PIN		PIN	
B1	GND	A1	GND
B2	FRRQ	A2	FWRQ
B3	FRS	A3	FWS
B4	GND	A4	GND
B5	DB1	A5	DBØ
B6	DB3	A6	DB2
B7	DB5	A7	DB4
B8	DB7	A8	DB6
B9	EOR	A9	PAR
B10	GND	A10	GND
B11	—	A11	—
B12	GND	A12	GND
B13	IRRQ	A13	IWRQ
B14	IWS	A14	DBRS
B15	DBWS	A15	IRS
B16	GND	A16	GND
B17	1.5 MHZ	A17	3 MHZ
B18	GND	A18	GND

D-CS-4-01501-4

SYM	REVISIONS	APPROVED	DATE
B	See change Tag 2 per PCO 58-1507		11-18-83
C	Delete Nds. one PCO 58-1467		12-2-83

Drive Interface Board

Drawing 22
Sheet 3 of 3