TACO

(40-6350)

EXTERNAL

REFERENCE

SPECIFICATION

December 20, 1976

CONTENTS

CHANGES AND PROBLEMS ON REV. A TACO

$\overline{\text{STS}}$ Sense of STS will change

Rev. A -- $\overline{\text{STS}}$ grounded is error condition

Rev. B -- $\overline{\text{STS}}$ floating is error condition

ERASE - Erase will not cause error on first hole

Rev. A -- Erase declares an error on first hole

Rev. B -- Erase declares an error on second hole.

READ COMMANDS

On Rev. A TACO, going from a read (G1=G3=1) to another command with G3=0 will cause WDT and WRT to glitch

GOING TO WRITE GAP PAST HOLE

On Rev. A TACO, if the hole bit is set and the command changes from a read or write (G1=1) command to a write gap, an error condition will occur.

END OF VALID DATA

On Rev. A TACO, EVD gaps can be declared during any instruction. The effect of this is that after rewinding over a blank tape or erasing a tape, the tape cannot be written because there is no way of clearing the EVD error. Rev. B TACO, only declares an EVD error on G1=1 or G5-GØ=000000, or 110000 instructions.

OVERVIEW

The TACO chip was designed to interface the IOC with the 09815-67901 transport. Additional circuitry is needed, however, to detect flux reversals, tach pulses, and to drive the motor. The TACO chip with this additional circuitry has the following capabilities:

SERVO

- The transport motor is controlled using simple commands: Fast/Slow, Forward/Reverse, Stop.
- Controlled acceleration and deceleration at 1200 in/s^2

READ/WRITE

- Reads and writes data on a 16 bit word basis using delta-distance coding.
- Double buffering of words of data.
- Capable of precompensating bits when writing

- Synchronizes to the bit pattern during read with continuous tracking of the one/zero threshold
- Calculation of checksum during read and write
- Reads and writes standard interchange format
- Reads and writes 9825 tapes
- Reads 9815 tapes
- Writes gaps of specified length.
- Writes individual bits on tape

OTHER

- Measures distance on the tape
- Counts gaps
- Detects End of Valid Data Marks
- Interfaces directly with the IOC
- Capable of interfacing with other processors
- Interrupts processor when instruction is completed or data is needed.

TACO REGISTERS

DATA REGISTER (IC1=IC2=0) This 16 bit register holds the data word when writing, each word to be written on tape is stored in this register. When reading, each word read from the tape can be loaded from this register.

INSTRUCTION REGISTER (IC1=1, IC2=0) This register has 6 bits of status information which can be read only and 10 bits of instruction which can be read or written. The 6 bits of status are:

5	4	3	2	1	0
TRB	GAP	WPR	ESTS	CART OUT	HOLE

Bit 0: This is the hole bit. It becomes a one on the falling edge of the HOL pin, this should correspond to a hole to tape transition. A clear status instruction zeros this bit.

BIT 1: This bit becomes a one on a low level of the CIN pin. This should correspond to the cartridge being removed. A clear status instruction zeros this bit if CIN is high.

Bit 2: This bit becomes a one on a low level of the $\overline{\text{ESTS}}$ pin. This bit can be used for an external status condition such as servo failure. A clear status instruction zeros this bit if $\overline{\text{ESTS}}$ is high.

Bit 3: This bit corresponds to the level of the WPR pin. This should correspond to the cartridge being write protected.

Bit 4: This bit corresponds to whether we are in gap or not on the tape. (See section on Gap Detection)

Bit 5: This bit is the track bit. It assumes the value of the MOD bit in a set track instruction. The TRB pin corresponds to this bit.

15	14	13	12	11	10	9	8	7	6
FWD	G5	G4	G3	G2	G1	G0	FGAP	FST	MOD

Bit 6: This is the mode bit. It is used to force a high threshold voltage level for flux reversal detection. (See section on external circuitry.) The MOD pin is related to this bit by the Boolean expression

$$\text{PIN} = \text{MOD} + \text{GAP} \cdot \overline{\text{FST}}$$

Bit 7: This bit is the fast bit. When FST = 1 the servo will run at 90 in/s. When FST = 0 the servo will run at 22 in/s. The FST pin corresponds to this bit. (It is used to set a high threshold value for flux reversal detection at fast speed. See section on external circuitry).

Bit 8: This bit is the file gap bit. When FGAP = 1 gap search instructions will only recognize as a gap those gaps that are greater than 1.5 inches in length. When FGAP = 0 gap search routines will recognize as gaps, any gap greater than 0.016 inches in length.

Bits: 9-14 These are the group qualifiers that determine the specific instruction to be executed. (See section on TACO instructions)

Bit: 15 This is the forward direction bit. It should correspond to the tape on the cartridge moving away from the load point hole and toward the early warning hole. When FWD=1, SIGN will be zero when accelerating from a stop.

TACH REGISTER (IC1=0, IC2-1) This register is incremented to zero to count gaps or tach pulses. To count N gaps or tach pulses, the twos- complement number -N is stored in this register. This register automatically counts tach pulses whenever the tape is being stopped. The count begins when the deceleration begins and ends when the GO pin goes low.

CHECKSUM REGISTER (IC2=1, IC1=1, DOUT =0)

This register holds the checksum calculated while reading or writing. It is cleared immediately after it is read. (This is a read-only register)

THRESHOLD REGISTER (IC2=1, IC1=1, DOUT=1)

(This is a write-only register) Into this register is stored a binary number giving the amount of precompensation and the value of the one/zero threshold. If t is the length of a zero bit in seconds, the least significant 13 bits of the threshold register should be a binary number equal to $5.586 \times 10^7 t$. For a read instruction, bits 13-15 should be zero. For a write instruction bits 13-15 should be a binary number equal to the number of 2MHz clock periods a zero bit should be shortened if preceded by a zero and followed by a one. (See section on Precompensation and Threshold Updating).

HOLDING REGISTER

The Holding Register is an internal register which accepts the 16 bit word when a I/O cycle with $\overline{\text{DOUT}}$ grounded is performed. When the algorithm for each instruction permits, the 16 bit word is transferred from the holding register to the proper register. As long as the holding register is full $\overline{\text{FLG}}$ will be high. When the holding register is empty and ready for new data $\overline{\text{FLG}}$ will be low. The maximum time it takes to empty the holding register is dependent on the current instruction. This time is given below:

CURRENT INSTRUCTION	MAX. TIME
Read type (G1=1,G3=1)	10.5us
Write type (G1=1,G3=0)	9 us
All others	2.5us

LOADING FROM A REGISTER

Any of the registers can be read at any time. The $\overline{FLG}$ pin has no meaning in this case.

WORKING REGISTER

The working register is an internal register used in read and write instructions.

TACO INSTRUCTION

This section is arranged as follows: Name of the instruction. The bit pattern of the group qualifier bits G5 through GØ. A description of the instruction. A flowchart of how the instruction works.

When an instruction is not being executed, TACO sits in a wait loop, looking to see whether the holding register is full. If it is full, the contents of the holding register are stored in the designated register (Data, Instruction, Tach, or Threshold). If the word was stored in the Instruction register, execution of that instruction begins.

In the flowcharts, END means execution of that instruction is over and TACO returns to the wait loop.

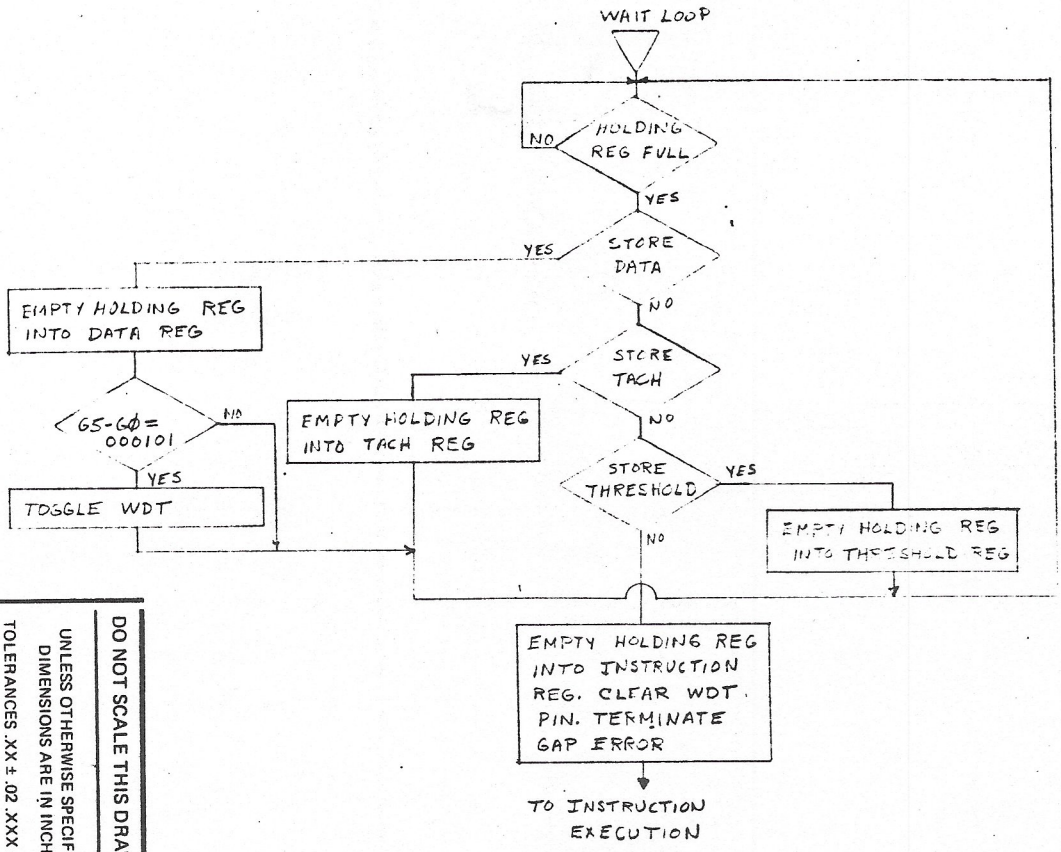
SET TRACK (001100) The value of the MOD bit is transferred to the TRB bit and pin.

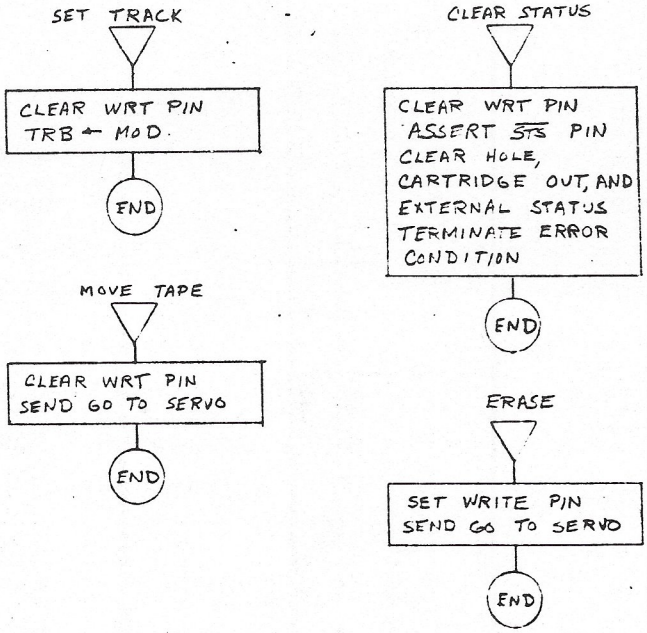
CLEAR STATUS (011100) clears the hole, cartridge out, and external status bits of the instruction register. Asserts the $\overline{STS}$ pin and terminates the error condition interrupt mode.

MOVE TAPE (010100) The tape is set in motion in the specified direction and speed.

ERASE (000100) The tape is set in motion in the specified direction and speed with the WRT pin set, the WDT pin clear.

WRITE FLUX REVERSAL (000101) TACO remains in the wait loop, but as long as this instruction is in the instruction register, each store into the data register, toggles WDT.





ENGINEERING RESPONSIBILITY

0	1	2	3	4		6	8	9	11	12	14	15			
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63												

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DRAWN BY J. BALZA	DATE 11/25/80	ITEM
ENGINEER		QTY.
RELEASE TO PROD.		MATERIAL-DESCRIPTION
SUPERSEDES DWG.		MAT'L-PART NO.
FINISH	NEXT ASSEMBLY	MAT'L-DWG NO
SCALE	PART NUMBER	MAT'L-SPEC
	B - - -	

TITLE WAIT LOOP, ERROR, MODE, CLEAR STATUS, SET TRACK

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STOP (001000) Stops the tape. During deceleration, each tach pulse increments the tach register by one until the GO pin is grounded.

STOP AND INTERRUPT (001001) This is identical to STOP except that an interrupt is requested when the GO pin is grounded.

INTERRUPT ON N TACH (111100) The tach register has previously been loaded with -N. Each tach pulse increments the tach register by one. When the tach register equals zero, an interrupt is requested.

INTERRUPT ON N TACH AFTER 22 IN/S. (110100) This instruction is identical to INTERRUPT ON N TACH except that the servo must reach 22 in/s in the currently specified direction before tach pulses increment the tach register.

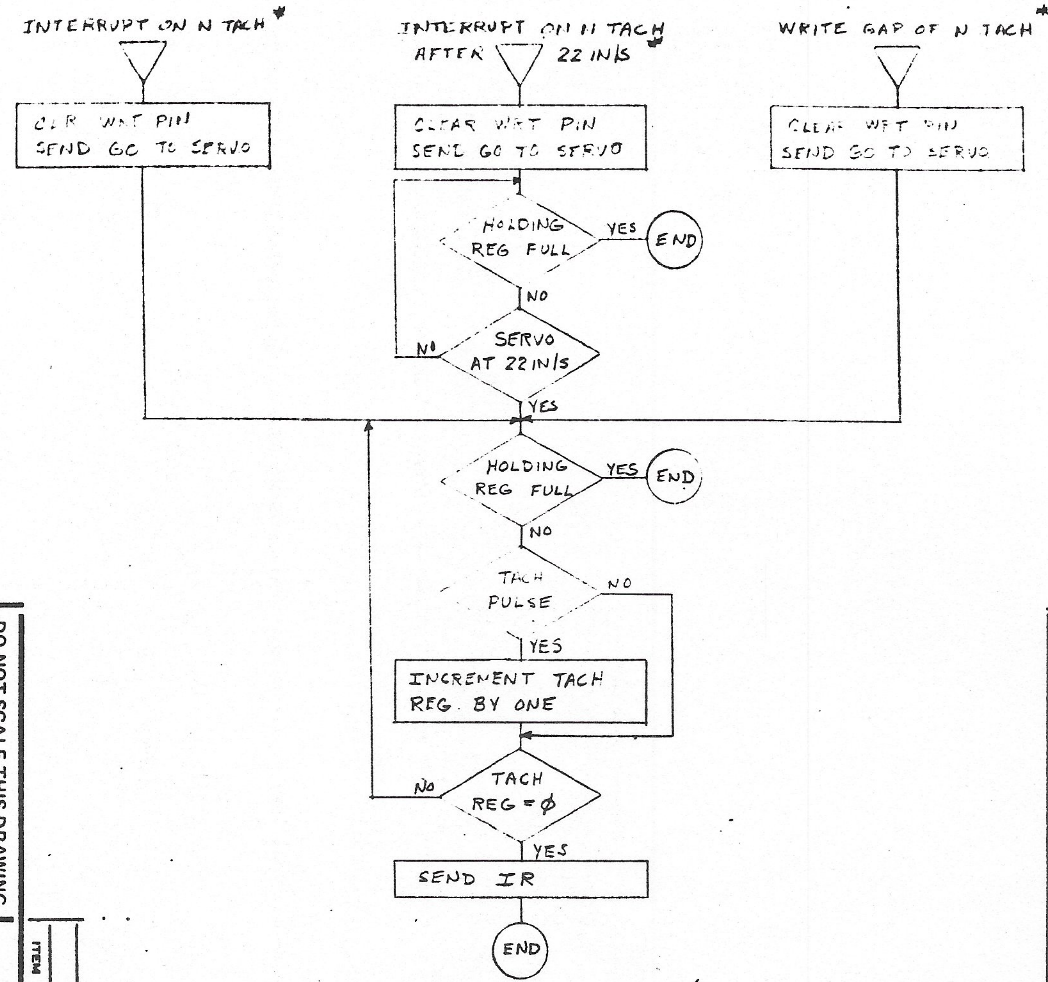
WRITE GAP OF N TACH (101100) This instruction is identical to INTERRUPT ON N TACH except that the WRT pin is set to a high level.

INTERRUPT AND STOP ON N TACH (11100x) The Tach register has previously been loaded with -N. Each tach pulse increments the tach register by one. When the tach register equals zero, a stop is sent to the servo. If GØ is zero, an interrupt is requested at this time. During deceleration each tach pulse continues to increment the tach register until the GO pin is grounded. If GØ is one, an interrupt is requested at this time.

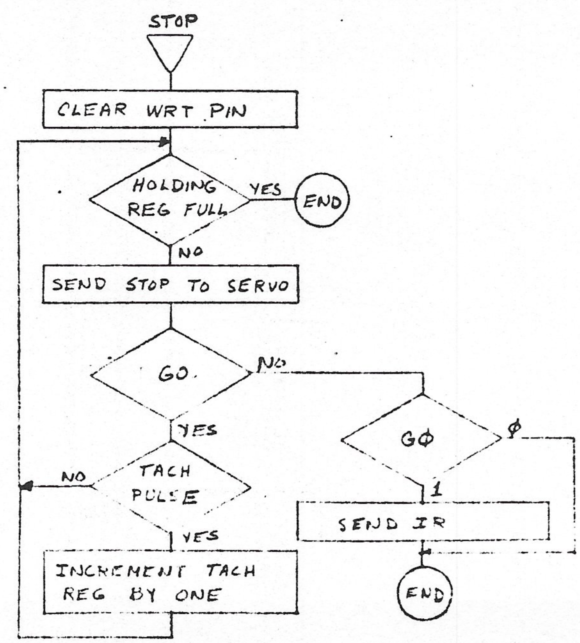
OPPOSITE DIRECTION ON N TACH (011000) The Tach register has previously been loaded with -N. Each tach pulse increments the tach register by one. When the Tach register equals zero, the FWD bit of the instruction register is toggled telling the servo to go in the opposite direction. An interrupt is requested when the servo reaches 22 in/s. in the new direction

INTERRUPT ON GAP (000000) Interrupts on seeing a new gap of 0.012 or 1.5 inches (FGAP = 1 is 1.5 inches) Note: if this instruction is executed while in a gap, the interrupt will occur on the next gap.

STOP IN GAP (10000x) This instruction searches for a new gap of 0.012 or 1.5 inches (FGAP = 1 is 1.5 inches) When a gap is found, the tach register is loaded with -256. Each tach pulse increments the tach register by one. When the tach register equals zero, a stop is sent to the servo.



* NOTE: TACH REGISTER MUST HAVE -N STORED BEFORE EXECUTING THESE INSTRUCTIONS



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L SPEC

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ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE STOP OR COUNT N TACH

NEXT ASSEMBLY

FINISH

SCALE

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PART NUMBER B-

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* THE TACH REGISTER MUST HAVE -N STORED BEFORE EXECUTING THESE INSTRUCTIONS.

ENGINEERING RESPONSIBILITY

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0	1	2	3	4	6	8	9	11	12	14	15				
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	48	61	63												

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ENGINEER		QTY.	MAT'L-PART NO.
RELEASE TO PROD.			MAT'L-DWG NO
SUPERSEDES DWG.			MAT'L-SPEC.

TITLE -ON N TACH

FINISH	NEXT ASSEMBLY	SCALE	PART NUMBER
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ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

ITEM | QTY. | MATERIAL-DESCRIPTION | MAT'L-PART NO. | MAT'L-DWG NO. | MAT'L-SPEC

TITLE: INTERRUPT ON GAP

NEXT ASSEMBLY

FINISH | SCALE

PART NUMBER B- - -

HEWLETT-PACKARD

SHEET OF

ENGINEERING RESPONSIBILITY

0	1	2	3	4		6		8	9		11	12	14	16	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63												

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SYM | REVISIONS | APPROVED | DATE

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If GØ=0, an interrupt is requested at this time.
During deceleration each tach pulse increments the tach register by one.
If GØ=1 on interrupt will be requested when the GO pin is grounded.

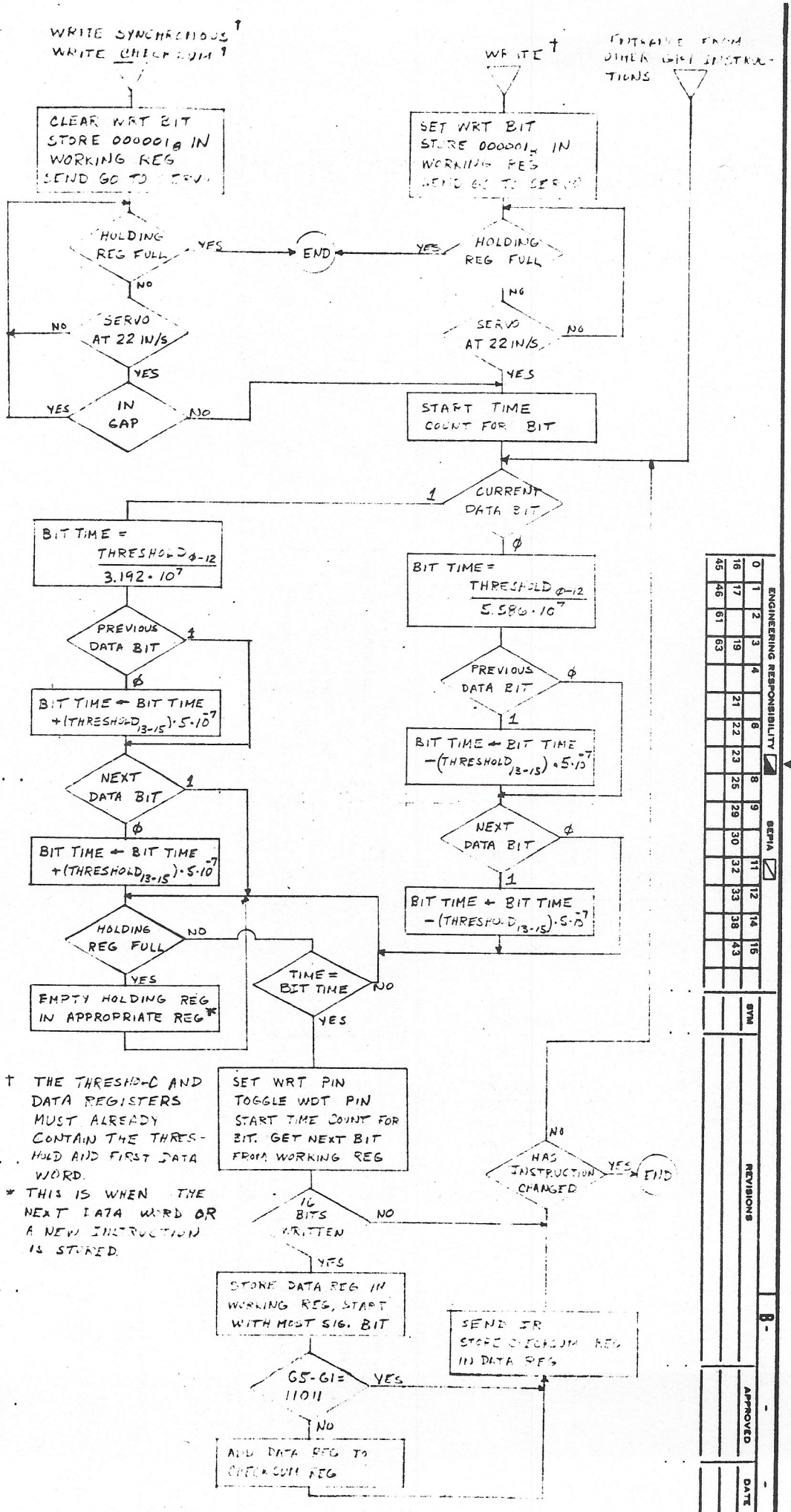
INTERRUPT ON N GAPS (110000) The tach register has previously been loaded with -N. Each new gap of 0.012 or 1.5 inches (FGAP =1 is 1.5 inches) increments the tach register by one. When the tach register equals zero, an interrupt is requested.

NOTE: The remaining instructions are read/write which is indicated by the fact that G1=1. Read instructions have G3 equal to one. Write instructions have G3 equal to zero. A preamble (15 zeros and a one) is written by write instructions whenever the previous instruction was not a read/write. A read instruction searches for a preamble whenever the previous instruction was not a read/write.

WRITE (000110) The threshold and data registers should have previously been loaded. The WRT pin is set and WDT cleared. After the tape reaches 22 in/s the preamble is written on tape. The data word is added to the checksum and then is stored in the working register to be written on tape, at this time an interrupt is requested to ask for another data word. This process is repeated for each data word. (Beginning at checksum addition).

WRITE SYNCHRONOUS (110010) The threshold and data registers should have previously been loaded. The WDT and WRT pins are cleared. After the tape reaches 22 in/s, the instruction waits for the tape to leave gap and enter data. The preamble is written with the WRT pin set at the same time WDT is first toggled. The data word is added to the checksum and then is stored in the working register to be written on tape. At this time an interrupt is requested to ask for another data word. This process is repeated for each word. (beginning at checksum addition)

WRITE CHECKSUM (110110) This instruction is identical to Write Synchronous except that the data word is not added to the checksum register. Note: the flowchart shows that all the write instructions leave the checksum



† THE THRESHOLD AND DATA REGISTERS MUST ALREADY CONTAIN THE THRESHOLD AND FIRST DATA WORD.

* THIS IS WHEN THE NEXT DATA WORD OR A NEW INSTRUCTION IS STORED.

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ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

DATE 11/23/71

TITLE WRITE INSTR. (16 BIT)

NEXT ASSEMBLY

FINISH

SCALE

PART NUMBER B- - -

HEWLETT PACKARD

ITEM

QTY.

MATERIAL-DESCRIPTION

MATL-PART NO.

MATL-DWG NO.

MATL-SPEC

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SYM

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DATE

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PRINTED ON DIEPO NO. 1023-10 CLEARPRINT FACEOUT

in the data register when the interrupt request for a new data word is given. Thus whenever data is not stored in the data register the checksum will be written next. This instruction guarantees that the checksum will not be added to itself in the checksum register.

WRITE 9825 (000111) This instruction is identical to write except that after every 16 bit word, a 17th one bit is written.

WRITE SYNCHRONOUS 9825 (110011) This instruction is identical to write synchronous except that after every 16 bit word, a 17th one bit is written.

WRITE CHECKSUM 9825 (110111) This instruction is identical to write checksum except that after every 16 bit word, a 17th one bit is written.

READ NO UPDATE (101010) The Threshold Register should already contain the threshold value. The WRT pin is cleared. After the tape reaches 22in/s., the instruction waits for the tape to leave gap and enter data. The first 8 bits of the preamble are read and ignored. After this any one bit signals the end of the preamble and the start of data. Each data word is read, then added to the checksum, stored in the data register and an interrupt requested. This process is repeated for each data word.

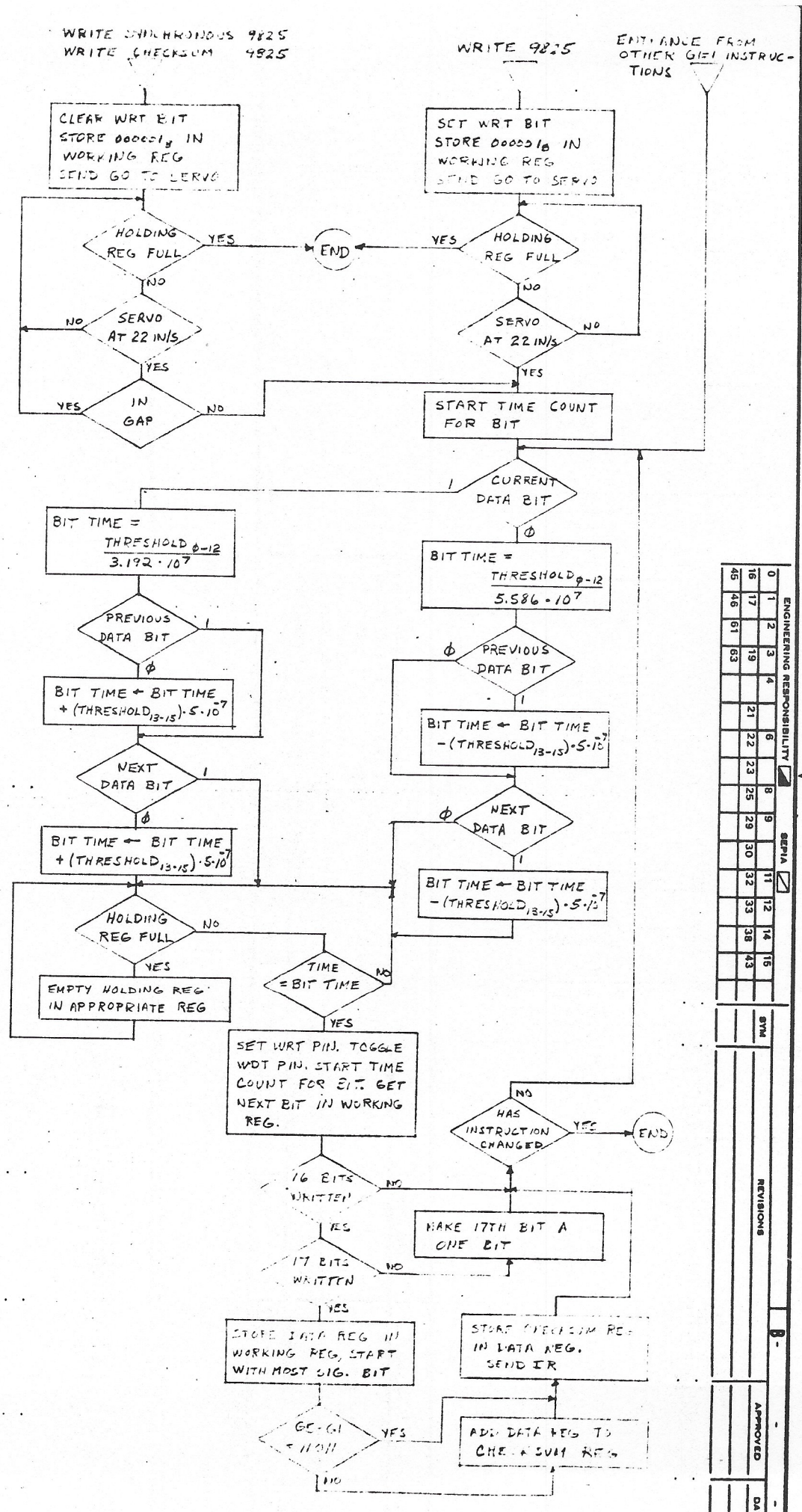
READ 6% UPDATE (111010) This instruction is identical to read except: 1) The first 8 bits of the preamble are used to update the threshold at a 50% rate in order to synchronize to the bit pattern. 2) Each data bit is used to update the threshold by 6%.

READ 12% UPDATE (011010) This instruction is identical to Read 6% except that the threshold is continually updated by 12% each bit time.

READ CHECKSUM 6% (111110) This instruction is identical to Read 6% Update except that the data word is not added to the checksum register.

READ CHECKSUM 12% (011110) This instruction is identical to Read 12% Update except that the data word is not added to the checksum register.

READ 9825 6% UPDATE (111011) This instruction is identical to Read 6% Update except that for each data word, a 17th bit is read and discarded.



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DRAWN BY J BILZA	DATE 11/23/76	ITEM
ENGINEER		QTY.
RELEASE TO PROD.		MATERIAL-DESCRIPTION
SUPERSEDES DWG.		MAT'L-PART NO.
NEXT ASSEMBLY		MAT'L-DWG NO
FINISH	SCALE	MAT'L-SPEC.

TITLE WRITE INSTR (9825)

HEWLETT PACKARD

PART NUMBER B - - -

SHEET OF

STOCK NO 9285-002 PRINTED ON DIEPO NO 1020-10 CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY ◪ SEPIA ◪

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63											

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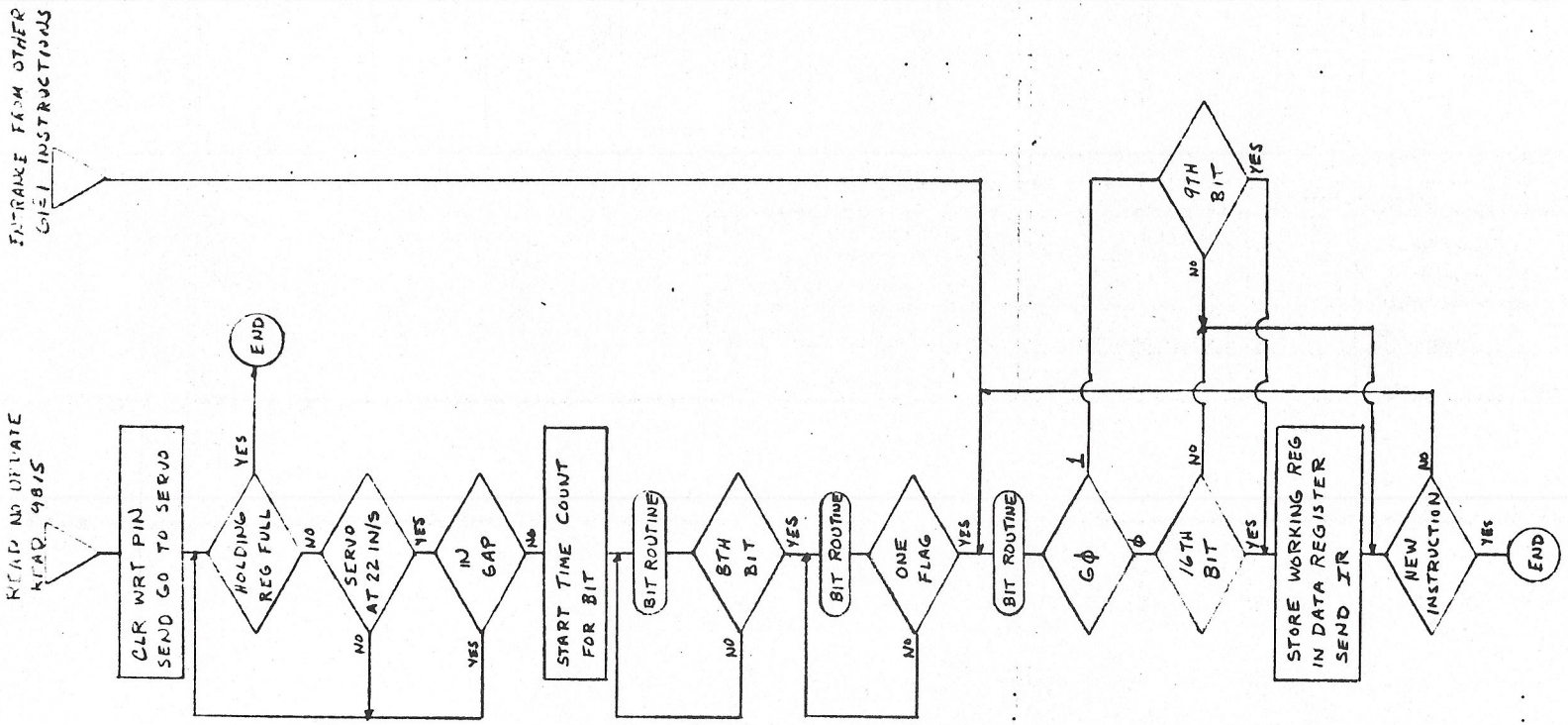

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

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DRAWN BY J. BALZA DATE 11/23/76

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE READ NO UPDATE
READ 9815

NEXT ASSEMBLY

FINISH SCALE

HEWLETT PACKARD

PART NUMBER B- - -

STOCK NO 9280-0062 PRINTED ON DIEPO NO. 1020-10 CLEARPRINT FADEOUT

SHEET OF

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0	1	2	3	4		6		8	9		11	12	14	16
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63											

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DRAWN BY	J. BALZA	11/23/76
ENGINEER		
RELEASE TO PROD.		
SUPERSEDES DWG.		

TITLE: BIT ROUTINE

NEXT ASSEMBLY	
FINISH	SCALE

HEWLETT-PACKARD

PART NUMBER B - - -

SHEET OF

ITEM | QTY. | MATERIAL-DESCRIPTION | MAT'L-PART NO. | MAT'L-DWG NO. | MAT'L-SPEC

STOCK NO. 8120-0003 PRINTED ON DIEPO NO. 1020-10 CLEARPRINT FADEOUT

READ 9825 12% UPDATE (011011) This instruction is identical to Read 12% Update except that for each data word a 17th bit is read and discarded.

READ 9825 CHECKSUM 6% (111111) This instruction is identical to Read Checksum 6% except that for each data word, a 17th bit is read and discarded.

READ 9825 CHECKSUM 12% (011111) This instruction is identical to Read Checksum 12% except that for each data word, a 17th bit is read and discarded.

READ 9815 (101011) The Threshold Register already contains the Threshold value. The WRT pin is cleared. After the tape reaches 22 in/s, the instruction waits for the tape to leave gap and enter data. The first 8 bits of the preamble are read and ignored. The preamble ends in a one bit which starts the data. Nine bits are read for each byte of data on tape. An interrupt is requested after each byte is read, the data byte is located in bits 0-7 of the data register. This process is repeated for each data byte. The checksum register has no meaning for this instruction.

INSTRUCTION SUMMARY

	G5	G4	G3	G2	G1	G0
SET TRACK	0	0	1	1	0	0
CLEAR STATUS	0	1	1	1	0	0
MOVE TAPE	0	1	0	1	0	0
ERASE	0	0	0	1	0	0
WRITE FLUX REVERSAL	0	0	0	1	0	1
STOP	0	0	1	0	0	0
STOP AND INTERRUPT	0	0	1	0	0	1
INTERRUPT ON N TACH	1	1	1	1	0	0
INTERRUPT ON N TACH AFTER 22	1	1	0	1	0	0
WRITE GAP OF N TACH	1	0	1	1	0	0
INTERRUPT AND STOP ON N TACH	1	1	1	0	0	x
OPPOSITE DIRECTION ON N TACH	0	1	1	0	0	0
INTERRUPT ON GAP	0	0	0	0	0	0
STOP IN GAP	1	0	0	0	0	x
INTERRUPT ON N GAP	1	1	0	0	0	0
WRITE	0	0	0	1	1	0
WRITE SYNCHRONOUS	1	1	0	0	1	0
WRITE CHECKSUM	1	1	0	1	1	0
WRITE 9825	0	0	0	1	1	1
WRITE SYNCHRONOUS 9825	1	1	0	0	1	1
WRITE CHECKSUM 9825	1	1	0	1	1	1
READ NO UPDATE	1	0	1	0	1	0
READ 6% UPDATE	1	1	1	0	1	0
READ 12% UPDATE	0	1	1	0	1	0
READ CHECKSUM 6%	1	1	1	1	1	0
READ CHECKSUM 12%	0	1	1	1	1	0
READ 9825 6% UPDATE	1	1	1	0	1	1
READ 9825 12% UPDATE	0	1	1	0	1	1
READ 9825 CHECKSUM 6%	1	1	1	1	1	1
READ 9825 CHECKSUM 12%	0	1	1	1	1	1
READ 9815	1	0	1	0	1	1

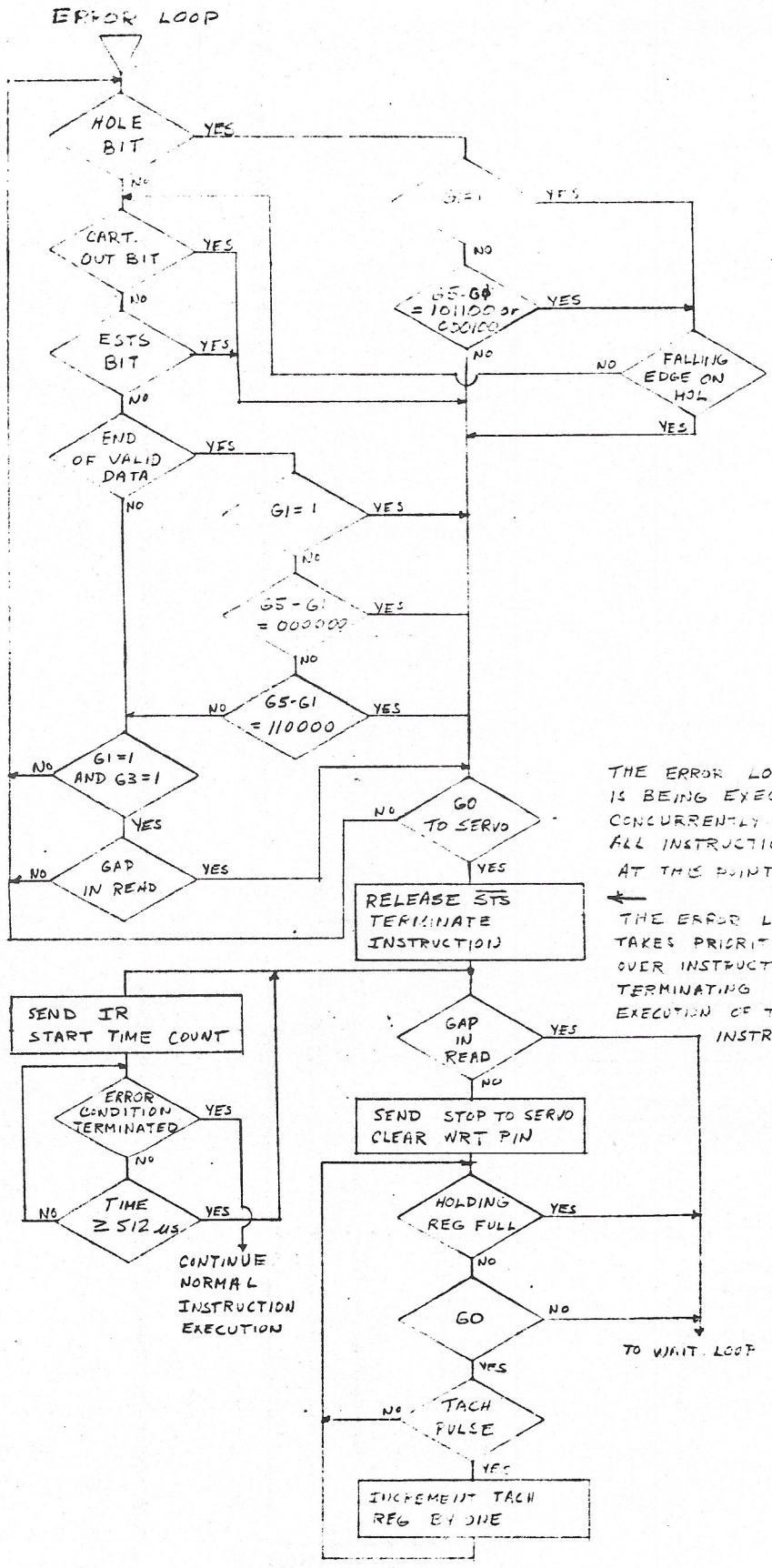
ERROR CONDITIONS

There are five occurances which can cause an error:

1) Hole detected
   a) If the present instruction has G1=0 and G5-GØ ≠ 101100, or 000100 (not a read or write and not erase or write gap) an error occurs if the HOLE bit of the instruction register is a one.
   b) If the present instruction has G1=1 or G5-GØ=101100, or 000100 (Read, Write, Erase, or write gap) an error occurs if the HOLE bit of the instruction register is already a one and another falling edge is seen on the HOL pin
2) Cartridge out. An error occurs if the CART OUT bit of the instruction register is a one.
3) External Status. An error occurs if the ESTS bit of the instruction register is a one.
4) End of Valid Data. An error occurs if a gap greater than 5.75 inches is encountered during an instruction which has G1=1, or G5-GØ=000000 or or 110000 (Read, Write interrupt on Gap, or interupt on N gaps)
5) Gap in Read. If the present instruction has G3=1 and G1=1 (read), the tape has reached 22 in/s. and the tape has left gap, an error occurs if another gap is seen. (This error condition was created for blind duplication of tapes and will not normally be encountered.)

If any of these errors are detected, and the current instruction is telling the servo to go, an error condition will commence. This error condition will:

1) Start requesting an interrupt every 512 microseconds until the error condition is terminated. (This allows software routines to continue, only recognizing errors at the end of the routine).
2) Release the $\overline{STS}$ pin until the error condition is terminated.
3) For all errors except Gap in Read, the Servo is told to stop. During deceleration each tach pulse increments the Tach register by one until the GO Pin is grounded. No new instruction will be allowed to send GO to the Servo until the error condition is terminated.



ENGINEERING RESPONSIBILITY																SEPIA
0	1	2	3	4			6	8	9	11	12	14	15			
16	17		19		21	22	23	25	29	30	32	33	38	43		
45	46	61	63													

SYM	REVISIONS	APPROVED	DATE

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 608

DRAWN BY J. BALTA	DATE 11/23/76	ITEM	
ENGINEER		QTY.	
RELEASE TO PROD.		MATERIAL-DESCRIPTION	
SUPERSEDES DWG.			
FINISH	TITLE ERROR LOOP	MAT'L-PART NO.	
NEXT ASSEMBLY		MAT'L-DWG. NO.	
SCALE		MAT'L-SPEC	
B -	PART NUMBER - -		

HEWLETT PACKARD

B - - -

SHEET OF

An error condition is terminated by a Clear Status instruction. In addition the Gap in Read error condition can be terminated by any new instruction, but $\overline{STS}$ will remain high.

NOTE: If the HOLE bit = 1 or G5-GØ=101100 or 000100 (Read, Write, Erase, or Write Gap) and the new instruction has G1=0 or G5-GØ≠ 101100, or 000100 (Not read or write and not erase or write gap) this instruction will cause an error condition and thus it will not be executed.

GAP DETECTION

TACO distinguishes between data and 3 types of gap: any gap, a file gap, and an end of valid data mark. Three signals are used to distinguish gaps from data: FR, the flux reversal pin; THR, the threshold pin; and FF, the frequency feedback or tach pulse pin. When the tape is moving at a speed less than or equal to 22 in/s. the FR pin is used by the gap detector to indicate data. When the tape is moving at a speed greater than 22 in/s. the THR pin is used by the gap detector to indicate data. This is because at high speed the flux reversal detection circuitry is outside its pass band of differentiation, but the threshold detection circuitry connected to the THR pin still functions. (See section on external circuitry).

The rules for distinguishing gaps from data are:

1) TACO enters data (and leaves all 3 types of gap) if four flux reversals (as indicated by the FR or THR pin) are encountered within sixteen tach pulses. The GAP bit of the instruction register is cleared on this occurence.
2) TACO declares a gap if sixteen tach pulses (approximately 0.016 inches of tape) are encountered without a flux reversal. The GAP bit of the instruction register is set on this occurence.
3) TACO decleares a file gap if 1452 tach pulses (approximately 1.5 inches of tape) are encountered without a flux reversal.
4) TACO declares an end of valid data mark if 5548 tach pulses (approximately 5.75 inches of tape) are encountered without a flux reversal. The EVD mark will only be declared if the 5548 tach pulses occurs during an

instruction where G1=1 or G5-GØ=000000 or 110000.

PRECOMPENSATION AND THRESHOLD UPDATING

PHYSICAL NATURE OF DATA BITS

Information is stored on the tape by causing the magnetic alignment of the tape surface to change direction at specified points along the tape. These changes in magnetic alignment are called "flux reversals." TACO uses a delta distance coding scheme to distingush one bits from zero bits, a one bit is nominally 1.75 times the length of a zero bit, where the length of a bit is the distance between flux reversals. A threshold value to distinguish one bits from zero bits is set at 1.33 times the nominal length of a zero.

PRECOMPENSATION Precompensation is a means of compensating for fringe effects encountered by the magnetic head during a read. Because of the high bit density written on the tape (up to 1600 flux reverslas per inch) the bit lengths approach the size of the magnetic head gap. Thus, when reading, the flux lines of the bits on either side of the current bit influence the apparent length of that bit. This effect is combatted during write by lengthening or shortening bits from their nominal length according to the following table:

Preceeding Bit	Current Bit	Following Bit	Precompensation on Current Bit
0	0	0	None
0	0	1	Shorten by Δ
0	1	0	Lengthen by 2Δ
0	1	1	Lengthen by Δ
1	0	0	Shorten by Δ
1	0	1	Shorten by 2Δ
1	1	0	Lengthen by Δ
1	1	1	None

Δ is defined as the number of clock periods specified in bits 13-15 of the threshold register.

THRESHOLD UPDATING

To further increase reliability the threshold value is being constantly updated based on the bit length of the bits currently being read. This allows TACO to track speed variations of the tape. The threshold is updated as follows: the length of a bit is normallized to the length of the threshold, i.e. one bit lengths are multiplied by 1.33/1,75; zero bit lengths, by 1.33/1.00. Then the following is executed

Threshold = Threshold - (Threshold-Normalized Length)· U

Where U = .5 if we have just left gap and are reading the first 8 zeros of the preamble

U = .125 if a read 12% Update

U = .0625 if a Read 6% Update.

Thus 8 zeros of the preamble are used to initially synchronize TACO to the bit length written on the tape. This is accomplished by a 50% update rate. Thereafter TACO can track speed variations of the tape by using a 12% or 6% update rate.

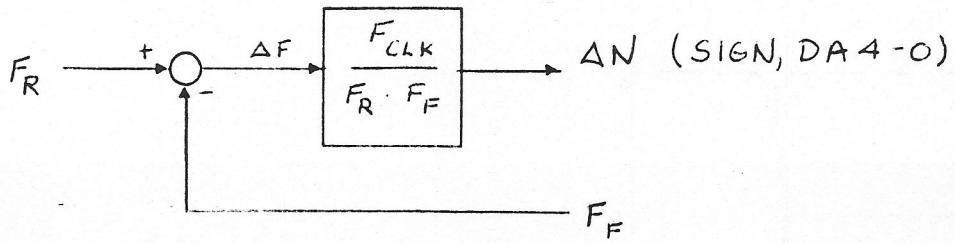
SERVO CONTROL

TACO provides for controlled acceleration and deceleration from 2in/s to 90 in/s at 1200 in/s^2 with an external clock rate of 4MHz (2 MHz internal) The servo uses the FF pin (frequency feedback) to control the servo. There should be 968 tach pulses on this pin for every 1 inch of tape.

At Slow speed FF=21276Hz, speed = 21.98 in/s.

At Fast speed FF=87196Hz, speed = 90.08 in/s.

At a 4MHz external clock rate the transfer function through TACO is



F_R = Frequency Reference

F_F = Frequency Feedback

F_{CLK} = Internal Clock Rate

At Frequency Lock

$$\frac{F_{CLK}}{F_R F_F} = \frac{2 \times 10^6}{(21{,}276 \times 10^3)2} = 4.418 \times 10^{-3}$$

The input to the servo control is the FF pin. Each rising edge is considered a tach pulse. The servo control has 7 pins as output. The GO pin is an open collector pin used to clamp the output drivers when the tape is stopped. The Servo control uses a controlled deceleration to stop the tape until the tape has reached 2 in/s. At this point the GO pin is grounded to stop the tape completely. It remains grounded until the Servo is told to go by an instruction. The other 6 pins are SIGN and DA4,3,2,1,0. These provide a sign magnitude form of error signal to the motor drivers. These error signals are as follows:

	SIGN	DA4	DA3	DA2	DA1	DA0
Stop FWD=1	1	0	0	0	0	0
Stop FWD=0	0	0	0	0	0	0
FWD, Initial ACC*	0	0	1	1	0	0
REV, Initial ACC*	1	0	1	1	0	0
FWD, too slow	0		E R R O R			
FWD, too fast	1		E R R O R			
REV, too slow	1		E R R O R			
REV, too fast	0		E R R O R			

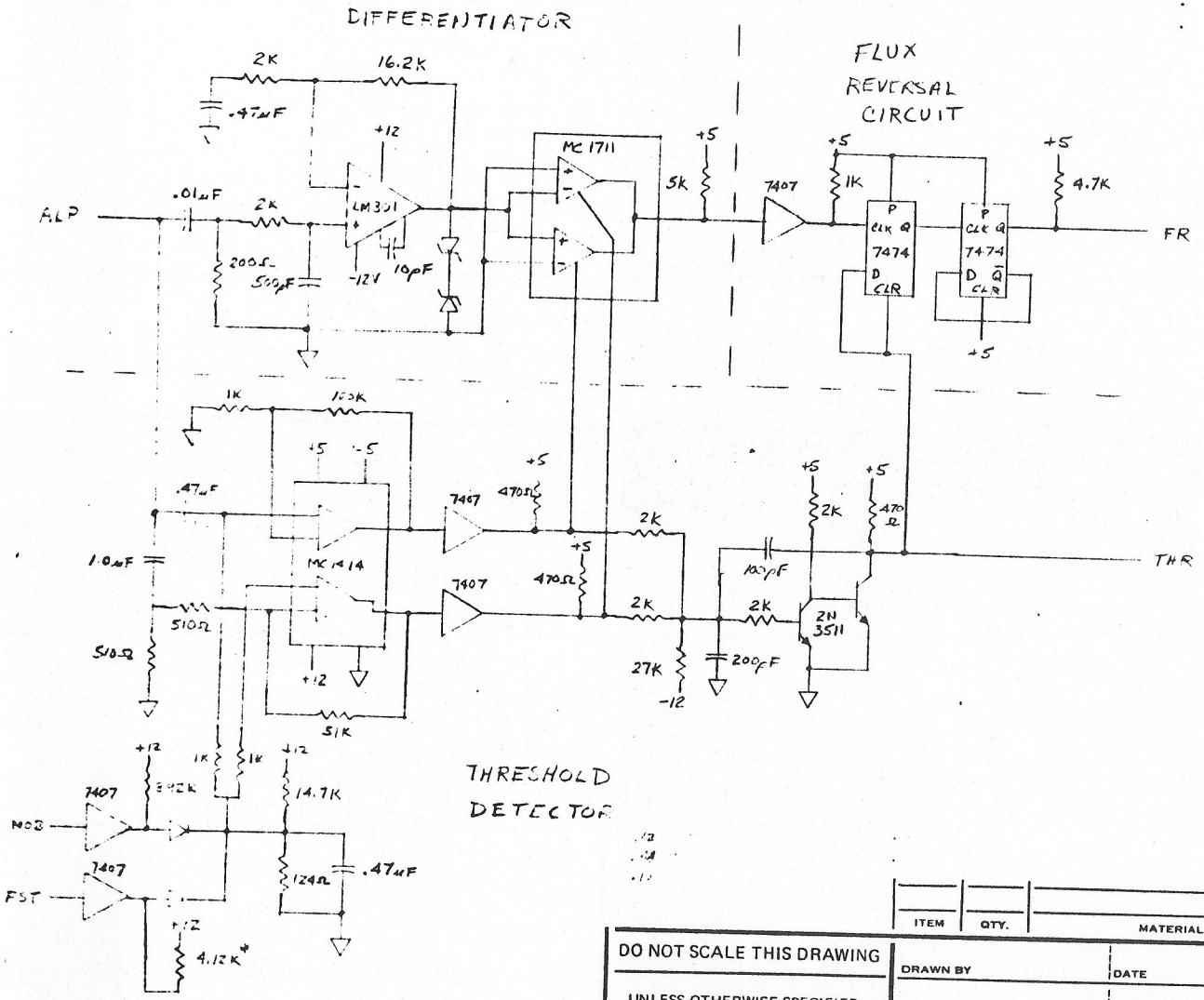
* From a stopped position, this is the initial error signal given, until the tape reaches 2 in/s.

EXTERNAL CIRCUITRY

This section will attempt to explain the external circuitry necessary to have a workable tape system using TACO. This will be accomplished by using a currently existing system as an example. Some of the reasons behind the circuitry will be explained. (Remember that this is an example only, and each system should be tailored to its own needs).

READ/WRITE CIRCUITRY

- The Read/Write Control circuitry uses half the magnetic head during write and the full head during read. During write, the read circuitry is isolated from the magnetic head and the WDT line changes the direction of current. It is important that some circuitry prevent accidental writing during power-up and power-down.
- The first stage amplifier has a gain of about 20 to increase signal strength. There are adjustable resistors to allow the same signal amplitude from both sides of the head and from one head to another.



ENGINEERING RESPONSIBILITY														
0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63											

SEPIA

SYM	REVISIONS	APPROVED	DATE

B - - -

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

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TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 608

DRAWN BY | DATE

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TITLE: FLUX REVERSAL DETECTOR

HEWLETT hp PACKARD

NEXT ASSEMBLY

FINISH | SCALE

PART NUMBER B - - -

SHEET OF

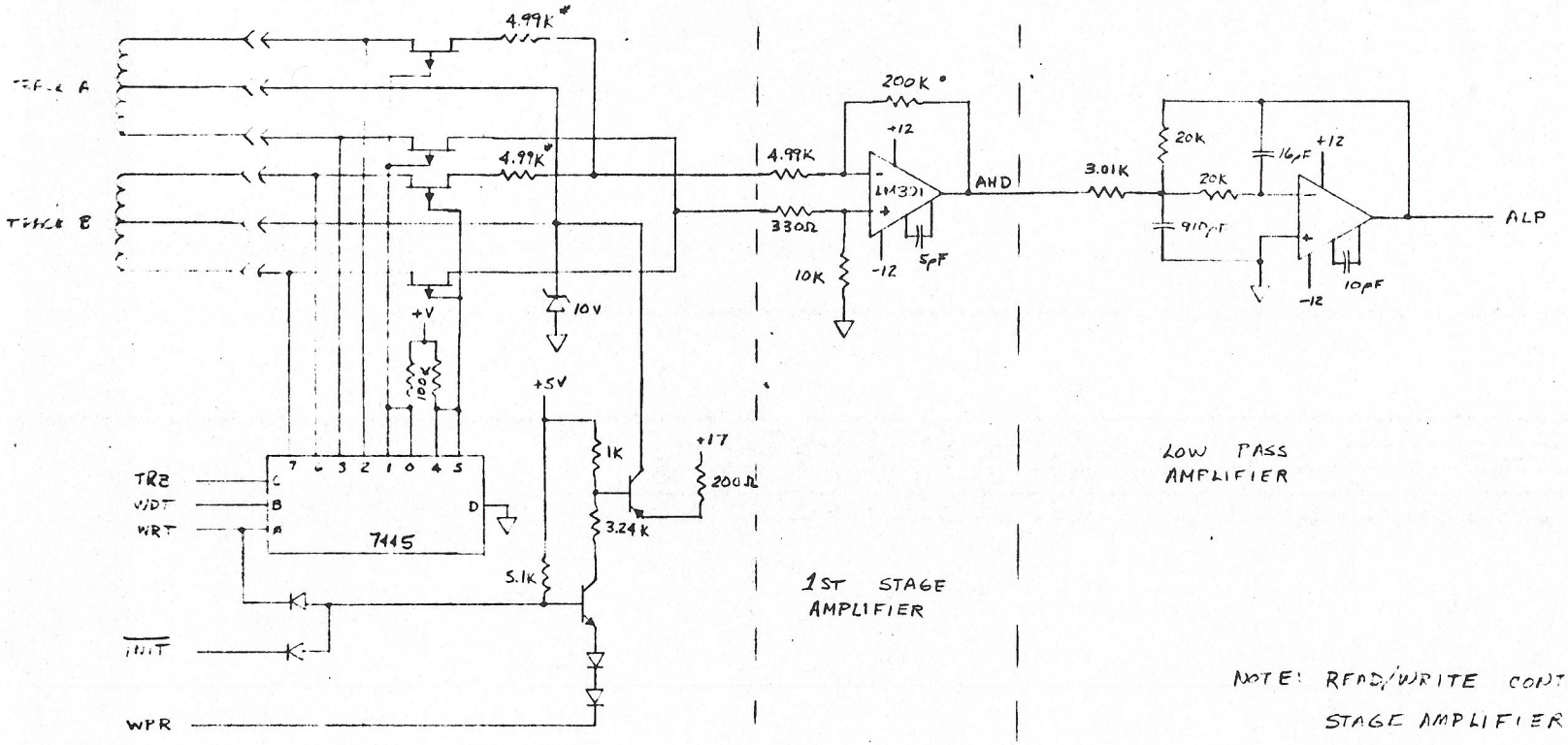
FORM NO. 5181-0002 PRINTED ON DIEPO NO. 1020-10 CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY															
0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63												

SEPIA

SYM	REVISIONS	APPROVED	DATE

B - - -



NOTE: READ/WRITE CONTROL AND THE 1ST STAGE AMPLIFIER EXIST ON THE 09815-66504 BOARD

* ADJUSTED VALUES

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG NO.	MAT'L-SPEC.

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TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 608

DRAWN BY	DATE	READ/WRITE CIRCUITRY	HEWLETT hp PACKARD
ENGINEER		TITLE	
RELEASE TO PROD.		NEXT ASSEMBLY	PART NUMBER
SUPERSEDES DWG.		FINISH / SCALE	B - - -

STOCK NO 9285-0502 PRINTED ON DIEPO NO 1020-10 CLEARPRINT FADEOUT

SHEET OF

- The low pass amplifier provides a signal gain and also reduces high frequency noise. The 3dB point for this amplifier is 55KHz. Thus there is no reduction of the gain at Read/Write speed. At search speed, however, there is a gain reduction but simultaneously the incoming signal amplitude is greater.
- The Threshold Detector detects when the signal from the head is greater than a threshold set by the TACO chip. This above threshold condition is used to enable the differentiator and to provide information to TACO. The threshold is nominally 0.10V; with MOD high, 0.44V; or with FST high, 0.42V.
- The Differentiator differentiates the signal off the magnetic head in order to detect the peak of the signal. The threshold detector enables either the negative or positive-poing zero crossing detector to determine the exact point of the flux reversal.
- The Flux Reversal Circuit creates an alternately positive or negative-going edge on each flux reversal. Note: The anding with THR done by this circuit is not necessary, since TACO does the same thing internally.
- TACO's FR and THR pins are designed internally to reject high frequency noise. Also THR must go high to allow FR to be accepted, then it must go low and high again before another FR will be detected.

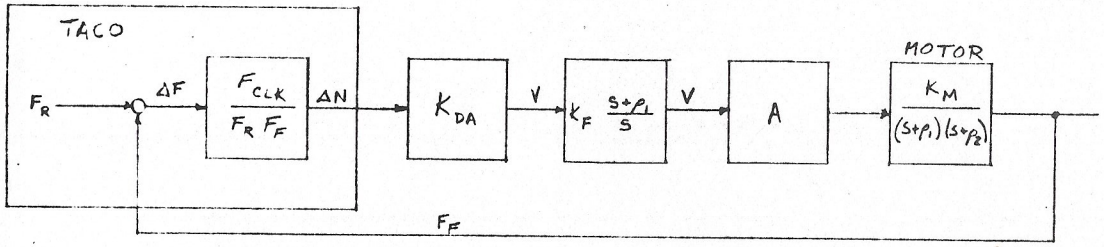
MOTOR CONTROL CIRCUITRY

The complete motor control circuitry has a control loop as shown on the next page. The open loop gain should be 1.044×10^6 for a $\zeta = .707$ which will give maximum band width without peaking.

$$K_{OL} = 1.044 \times 10^6 = (4.418 \cdot 10^{-3})(K_{DA})(K_F)(A)(5.76 \cdot 10^8)$$

$$K_{DA}\, K_F\, A = 0.410$$

- The D to A converter takes the DA4 through DA0 outputs and converts it to a current. For this circuit each count on DA4 through DA0 results in $\frac{5.11V}{(32)(2.49K)}$ = 64uA of current.



THIS IS A TYPE 1 (CONSTANT VELOCITY) SYSTEM

IN TACO: $\frac{F_{CLK}}{F_R F_F} = 4.418 \times 10^{-3}$ AT LOCK (22 in/s)

K_{DA} IS THE TRANSFER FUNCTION OF THE D TO A CONVERTER

A IS THE OUTPUT AMP GAIN

K_M OF THE MOTOR IS $5.76 \times 10^8 \frac{Hz}{V-sec^2}$

$\rho_1 = 30 \frac{rad}{s}$ $\rho_2 = 1445 \frac{rad}{s}$

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC

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TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 608

DRAWN BY | DATE

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

TRANSFER FUNCTION OF MOTOR CONTROL

TITLE

HEWLETT hp PACKARD

NEXT ASSEMBLY

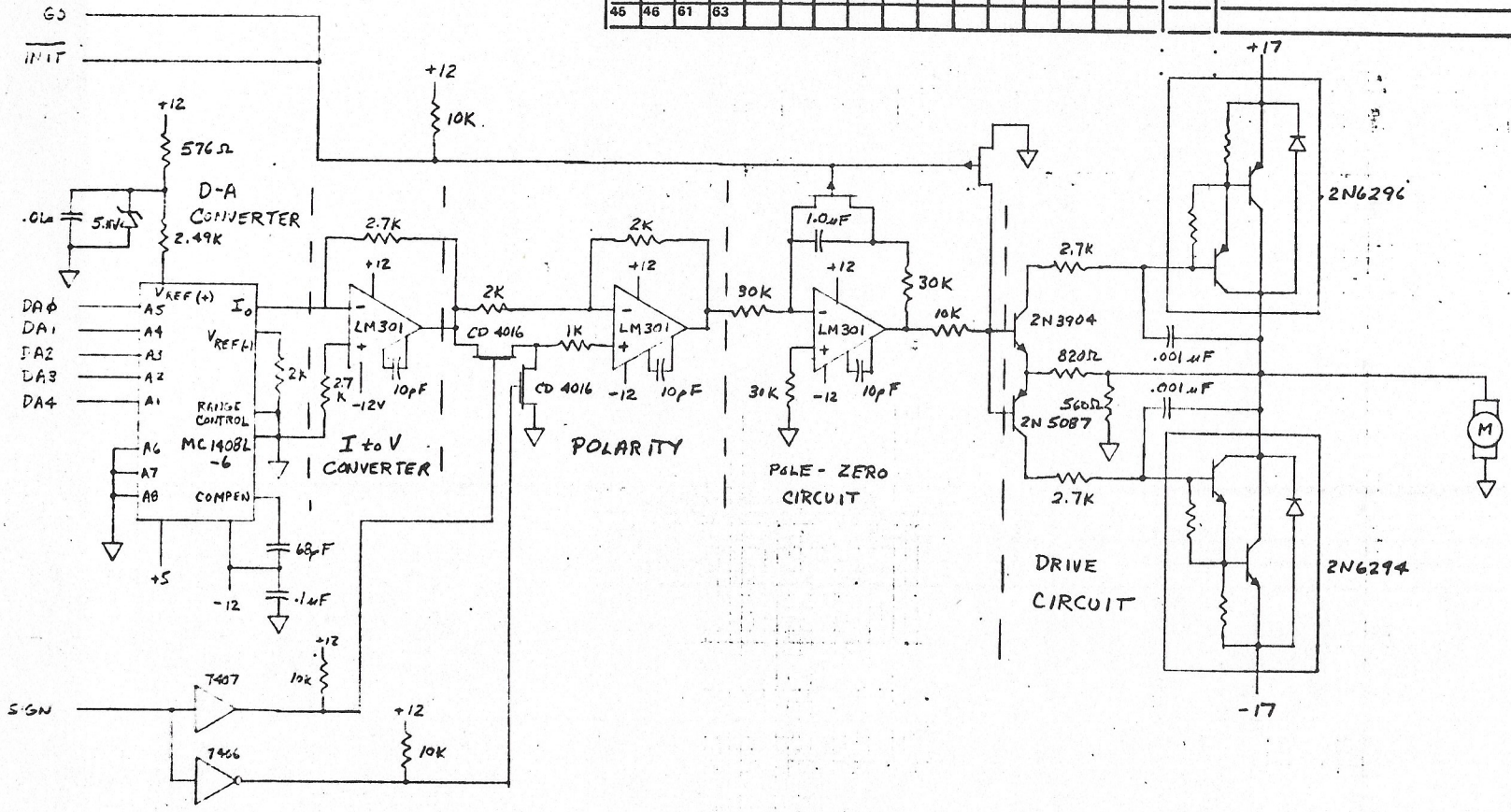
FINISH | SCALE

PART NUMBER B - - -

SHEET OF

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63											

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

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TOLERANCES .XX ± .02 .XXX ± .005

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DRAWN BY / DATE	
ENGINEER	
RELEASE TO PROD.	
SUPERSEDES DWG.	

MOTOR CONTROL CIRCUIT

TITLE

HEWLETT hp PACKARD

NEXT ASSEMBLY

FINISH / SCALE

PART NUMBER B - - -

SHEET OF

- The I to V Converter transforms the current from the D to A converter to a voltage level. The function is .17V per count of DA4 through DA0.
- The polarity circuit looks at the SIGN output and either inverts the voltage level or leaves it the same.
- The pole-zero circuit has the transfer function

$$\frac{30K}{30K} \quad \frac{S+(30K)1uF}{S} = \frac{S+33}{S}$$

This zero at 33 rad/s cancels the motor pole at 30 rad/s

- The drive circuitry drives the motor and has a gain of

$$\frac{820 + 560}{560} = 2.46$$

Note that when $\overline{INIT}$ or GO is grounded the drive circuitry will turn off. This eliminates creeping of the tape during power-on, power-off, or when the tape is supposed to stop.

- For this sample circuitry:

$$K_{DA}\ K_F\ A = (.17)(1)(2.46) = .418$$

HOLE AND TACH DETECTORS

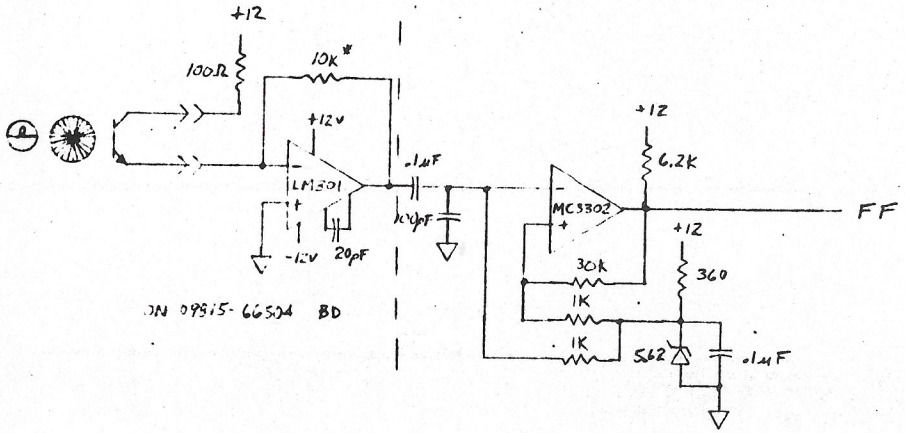
- The hole and tach detectors amplify the signals of the phototransistors on the transport and add some degree of noise immunity to them .

ENGINEERING RESPONSIBILITY														
0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63											

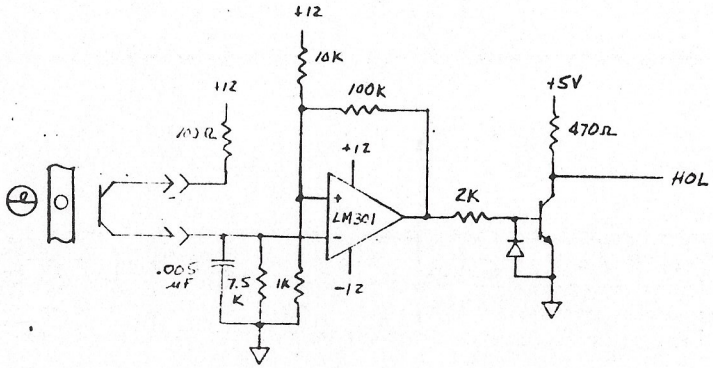
SEPIA

B - - -

SYM	REVISIONS	APPROVED	DATE



TACH PULSE DETECTOR



HOLE DETECTOR
(ON 09815-66504 BD)

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC

DO NOT SCALE THIS DRAWING

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TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 608

DRAWN BY / DATE	
ENGINEER	
RELEASE TO PROD.	
SUPERSEDES DWG.	

TACH AND HOLE DETECTOR — TITLE

HEWLETT hp PACKARD

NEXT ASSEMBLY

FINISH / SCALE

PART NUMBER B - - -

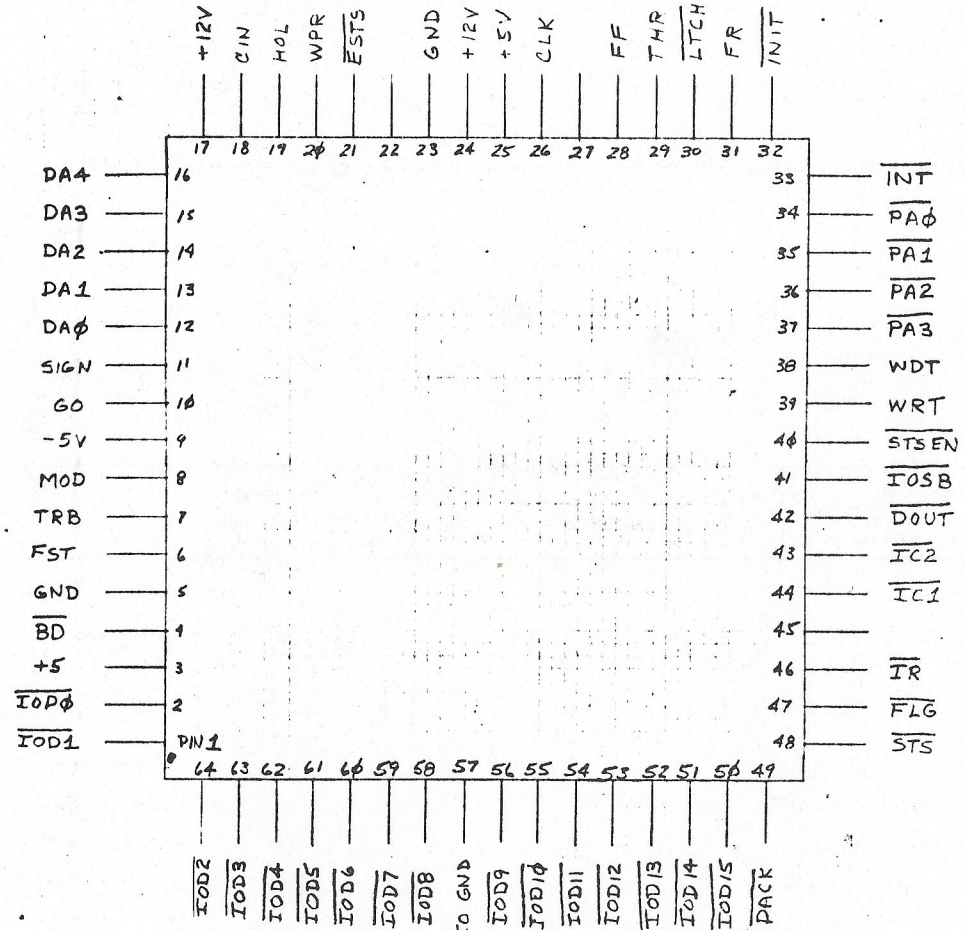
SHEET OF

ENGINEERING RESPONSIBILITY ◪ SEPIA ◪

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63											

B- - -

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 608

DRAWN BY | DATE

ENGINEER

RELEASE TO PROD.

SUPERSEDES DWG.

PINOUT VIEWED FROM ABOVE PACKAGE

TITLE

NEXT ASSEMBLY

FINISH | SCALE

HEWLETT hp PACKARD

PART NUMBER B- - -

TACO CHIP PINOUT

The pinout of the chip is shown on the following page. This section will define the use of each pin. The description format is: mnemonic, name, direction, type of output, additional explanation.

$\overline{IOD}$(0-15) I/O data, input-output, 5V active pullup. These are the 16 data bit lines which are used to communicate with the registers.

$\overline{BD}$ Bus Drive, output, open-collector. When $\overline{BD}$ is grounded the TACO chip is driving the IOD bus.

FST Fast, output, 5V active pullup. This pin corresponds to the FST bit of the instruction register. It is used to set a high threshold for flux reversal detection at fast speed.

TRB Track B, output, 5V active pullup. This pin corresponds to the TRB bit of the instruction register. It is used to select track A or track B on the magnetic head.

MOD Mode, output, 5V active pullup. This pin corresponds to the Boolean equation $MOD_{pin} = MOD_{bit} + \overline{FST} \cdot GAP$ of the bits in the instruction register.

GO Go, output, open-collector. GO is grounded by TACO's servo control to stop the tape when the tape speed is less than 2 in/s. It should ground the motor drivers to prevent creeping.

SIGN Sign of error, output, 5V active pullup. This pin indicates the sign of the error number to be given to the motor control circuitry.

DA(4-0) D to A, output, 5V active pullup. These pins give a count to the D to A converter indicating the magnitude of the error of the motor speed. DA0 being the least significant bit.

CIN Cartridge in, input. This pin is tied to the CIN bit of the instruction register. It is used to indicate that a cartridge is currently in the transport.

HOL HOLE, input. This pin should be high whenever a hole is seen on the tape. A high to low transition of this pin will set the HOLE bit of the instruction register.

WPR Write prevent, input. This pin is connected to the WPR bit of the instruction register. It should be high when the cartridge is write protected.

CLK Clock, input. This is the external clock input to the chip. It needs to be a 4MHz, 4V square wave.

FF Frequency Feedback, input. This is the tach pulse input to the chip. It is used to control the motor, count tach pulses and detect gaps. There must be 968 rising edges for each 1 inch of tape.

THR Threshold, input. This pin is used to indicate that the signal off the magnetic head is above a specified threshold value. Internally high frequency noise will be rejected from this pin. Threshold is used to detect gaps when the tape is moving faster than 22 in/s and furnishes an enable signal for the FR pin

$\overline{\text{LTCH}}$ Latch, input. When this pin is grounded the levels on the $\overline{\text{PA0}}$, $\overline{\text{PA1}}$, $\overline{\text{PA2}}$, $\overline{\text{PA3}}$, $\overline{\text{IC1}}$, and $\overline{\text{IC2}}$ pins are latched internally at their current levels. This allows for multiplexing the $\overline{\text{IOD}}$ lines with these addressing lines.

FR Flux reversal, input. This pin indicates that a flux reversal has been seen off the magnetic head. Internally high frequency noise is rejected and this signal will only be recognized after a low to high transition of the THR pin. There should be only one transition for each flux reversal seen. FR is used during read instructions to time the length of a bit and for gap detection when the tape speed is less than or equal to 22 in/s.

$\overline{\text{INIT}}$ Initialize, input. This initializes the TACO chip. Initialize should remain grounded until all power supplies are valid and the clock input is stable.

$\overline{\text{INT}}$ Interrupt, input. This pin indicates that an interrupt poll is in progress. (The chip will be unaddressed while $\overline{\text{INT}}$ is low)

$\overline{PAn}$ Peripheral Address, input. These are the address pins of TACO. TACO will be addressed when $\overline{PA3}$ through $\overline{PA0}$ are all grounded. These pins can be latched internally by the $\overline{LTCH}$ pin.

WDT Write Data, output, open-collector. This pin should be used to select the direction of current through the magnetic head. It is grounded when writing gaps, so all gaps have the same direction of flux.

WRT Write, output, open-collector. This pin should turn on the write current to the magnetic head when high.

$\overline{STSEN}$ Status enable, input. When this pin is grounded it allows the $\overline{STS}$ and $\overline{FLG}$ pins to pull low.

$\overline{IOSB}$ I/O Strobe, input. This is a timing signal for storing into a TACO register. Data is latched on the rising edge of this signal. This signal also answers an interrupt request when TACO is addressed. An IOSB will release the IR pin.

$\overline{DOUT}$ Data Out, input. This pin indicates the direction of data flow as referenced to the processor. $\overline{DOUT}$ going low will dump the addressed register on the IOD lines if TACO is addressed.

$\overline{ICn}$ input. These lines select a specified register in TACO to be read or written. These pins can be latched internally by the $\overline{LTCH}$ pin.

$\overline{IR}$ Interrupt request, output, open-collector. This pin is grounded whenever the chip is requesting an interrupt of the processor. Once grounded, the $\overline{IR}$ pin will remain grounded until an IOSB occurs with TACO addressed.

$\overline{FLG}$ Flag, output, open collector. This pin is grounded whenever TACO is addressed, $\overline{STSEN}$ is low, and the chip is ready to accept data from the processor.

$\overline{STS}$ Status, output, open-collector. This pin is grounded whenever TACO is addressed, $\overline{STSEN}$ is low, and the chip is not currently in an error condition.

$\overline{PACK}$ Poll acknowledge, output, open-collector. This pin acknowledges an interrupt poll. It will be grounded when $\overline{INT}$ is low, PA3 is low, and the chip is requesting an interrupt.

TACO CHIP (6300) PRELIMINARY SPECIFICATIONS

II. AC CHARACTERISTICS

1. CLOCK

PARAMETER	MIN.	TYP.	MAX.	UNIT
Frequency	3.98	4.00	4.02	MHz
Rise Time			25	Nsec
Fall Time			25	Nsec
Positive Pulse Duration	80	125	170	Nsec

2. CAPACITANCE

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITION
Cin (B)	Input Cap. on B: DIRECTIONAL PINS			10	PF	
Cin (I)	Input Cap. on input only pins			8	PF	
Clp	Capacitive load on IOD pins			150	PF	Worst case timing
Clt	Capacitive load on transport output pins			100	PF	

3. WRITE CYCLE TIMING (REF. TIMING DIAGRAM #1)

SYMBOL	PARAMETER	REF. POINT	MIN	TYP	MAX	UNITS
T1	Peripheral Address Valid	IOSB going false	400			NS
T2	Int Flase	false	400			NS
T3	Leading Edge of Reg. Code true (IC1-IC2)	false	250			NS
T4	Dout True	false	200			NS
T5	IOSB Pulse width		200			
T6	Leading Edge of IOD Data True	IOSB Going false	50			NS
T7	Trailing Edge of per.add., $\overline{\text{INT}}$.and Reg. code true.	IOSB Going false	50			NS
T8	Trailing Edge of IOD Data true	IOSB Going false	80			NS

TACO CHIP (6300) PRELIMINARY SPECIFICATIONS Cont'd

II. AC CHARACTERISTICS

4. READ CYCLE TIMING (REF. TIMING DIAGRAM #2)

SYMBOL	PARAMETER	Ref. Point	Min	Typ	Max	Units
T20	Peripheral Address Valid	Data Valid	300			Nsec
T21	Int. False	Data Valid	300			Nsec
T22	Leading Edge of Reg. Code True (IC1-IC2)	Data Valid	300			Nsec
T23	Dout False	Data Valid	50			Nsec
T24	Bus Drive True	Data Valid	0			Nsec
T25	Bus Drive True	Dout True	10		75	Nsec
T26	Data Not Valid	Dout True	10		75	Nsec

5. INTERRUPT POLL TIMING, (REF. TIMING DIAGRAM #3)

SYMBOL	PARAMETER	Ref. Point	Min	Typ	Max	Units
Ta	IR True	Pack True	85			Nsec.
Tb	INT true	Pack True	75			Nsec.
Tc	PA3 true	Pack True	75			Nsec.
Td	Dout False	Pack True	40			Nsec.
Te	IR false	Pack Release	20		50	Nsec.
Tf	INT False	Pack Release	20		50	Nsec.
Tg	PA3 False	Pack Release	20		50	Nsec.
Th	Dout True	Pack Release	10		25	Nsec.

6. FLG AND STS TIMING (REF TIMING DIAGRAM #4)

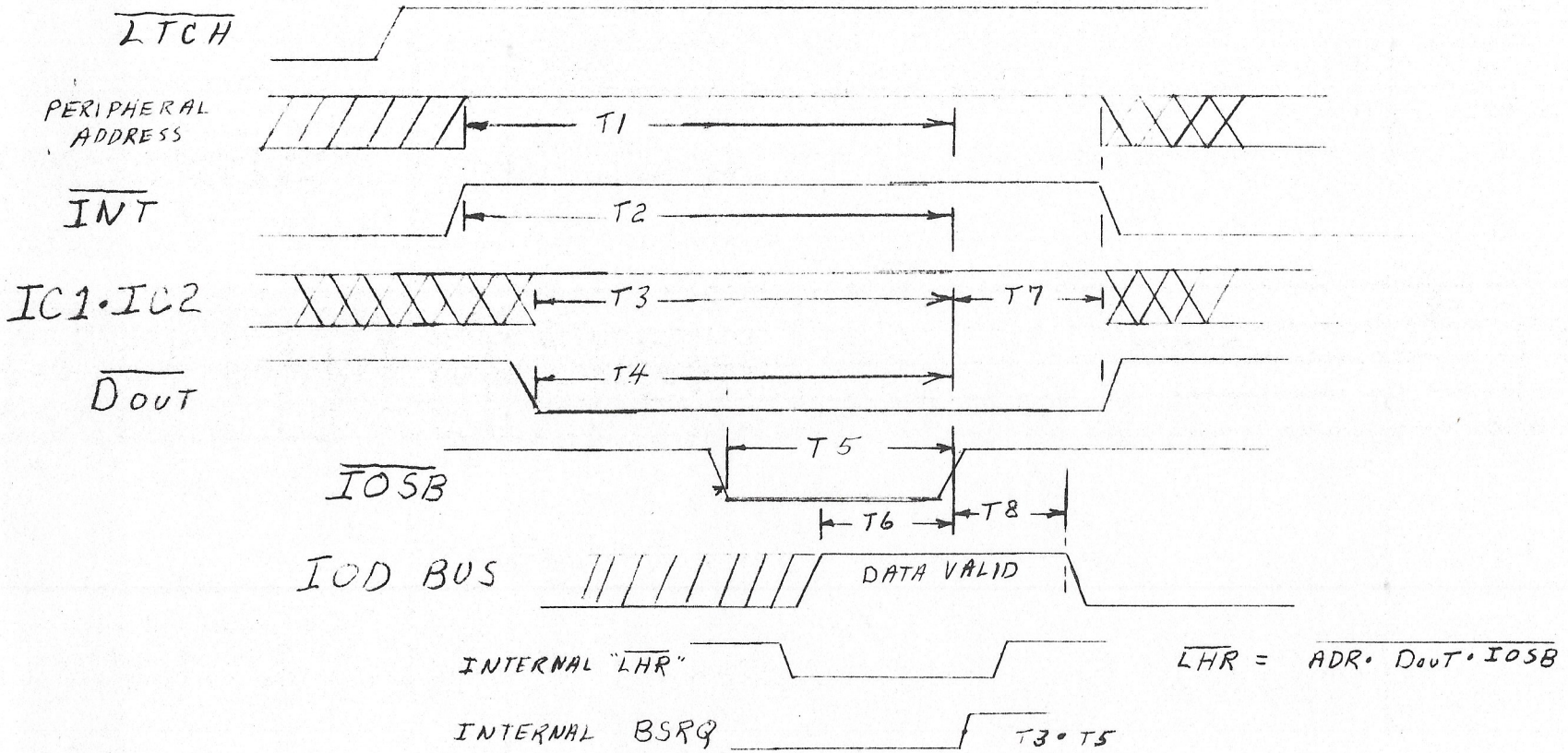
SYMBOL	PARAMETER	Ref. Point	Min	Typ	Max	Units
Tu	Peripheral add true	STS or FLG true	200			Nsec.
Tv	Status enable true	STS or FLG true	100			Nsec.
Tw	Peripheral add false	STS or FLG release			200	Nsec.
Tx	Status enable false	STS or FLG release			100	Nsec.

ENGINEERING RESPONSIBILITY ◪ SEPIA ◪

0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63												

A- - -

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

DRAWN BY: B THAYER	DATE: 11-23-76	TITLE: TACO CHIP 40-6350 WRITE CYCLE TIMING
ENGINEER: B Thayer	DATE: 11-23-76	
RELEASE TO PROD.		NEXT ASSEMBLY: TIMING DIAG. # 1
SUPERSEDES DWG.		FINISH / SCALE

HEWLETT hp PACKARD

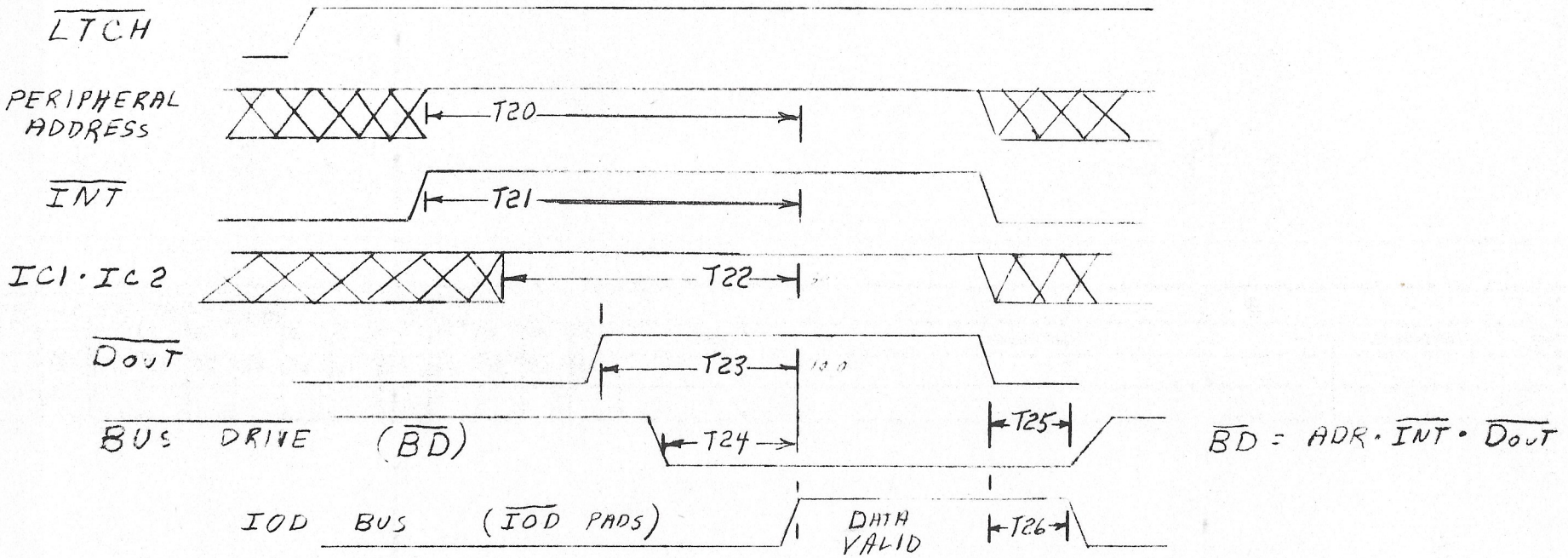
PART NUMBER: A- - -

ENGINEERING RESPONSIBILITY ◪ SEPIA ◪

0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63												

A- - -

SYM	REVISIONS	APPROVED	DATE



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

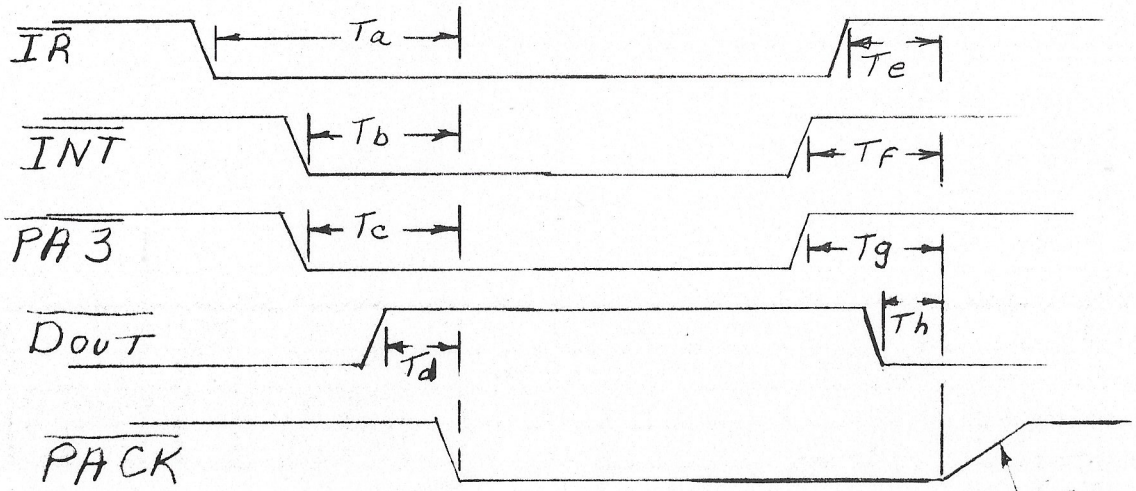
DRAWN BY: B THAYER	DATE: 11-23-76	TITLE: TACO CHIP 40-6350 READ CYCLE TIMING	HEWLETT hp PACKARD
ENGINEER: B Thayer	DATE: 11-23-76		
RELEASE TO PROD.		NEXT ASSEMBLY: TIMING DIAG. #2	PART NUMBER: A- - -
SUPERSEDES DWG.		FINISH	SCALE

ENGINEERING RESPONSIBILITY ◪ SEPIA ⊘

0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63												

A- - -

SYM	REVISIONS	APPROVED	DATE



(PACK = IR • INT • PA3 • $\overline{DOUT}$)

(SPEED OF THIS CHANGE IS A FUNCTION OF THE EXTERNAL PULL UP.)

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

DRAWN BY B THAYER DATE 11-23-76

ENGINEER B Thayer DATE 11-23-76

RELEASE TO PROD.

SUPERSEDES DWG.

THCO CHIP 40-6350 INTERRUPT POLL TIMING.
TITLE

TIMING DIAG #3
NEXT ASSEMBLY

FINISH SCALE

HEWLETT PACKARD

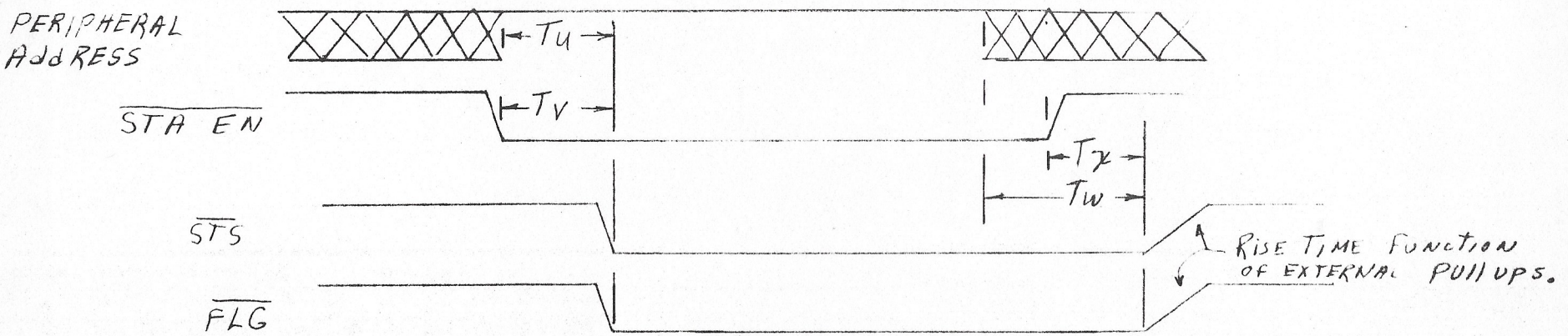
PART NUMBER A- - -

ENGINEERING RESPONSIBILITY ◪ SEPIA ⊘

0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63												

A - - -

SYM	REVISIONS	APPROVED	DATE



STS = PERIPHERAL Add • STATUS ENABLE • TACO CHIP STATUS CLEAR

FLG = PERIPHERAL Add • STATUS ENABLE • TACO CHIP READY FOR DATA

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

DRAWN BY: B THAYER	DATE: 11-23-76	TACO CHIP 40-6350	HEWLETT hp PACKARD
ENGINEER: B Thayer	DATE: 11-23-76	TITLE: FLG AND STS TIMING.	
RELEASE TO PROD.		NEXT ASSEMBLY: TIMING DIAG. # 4	PART NUMBER: A - - -
SUPERSEDES DWG.		FINISH	SCALE