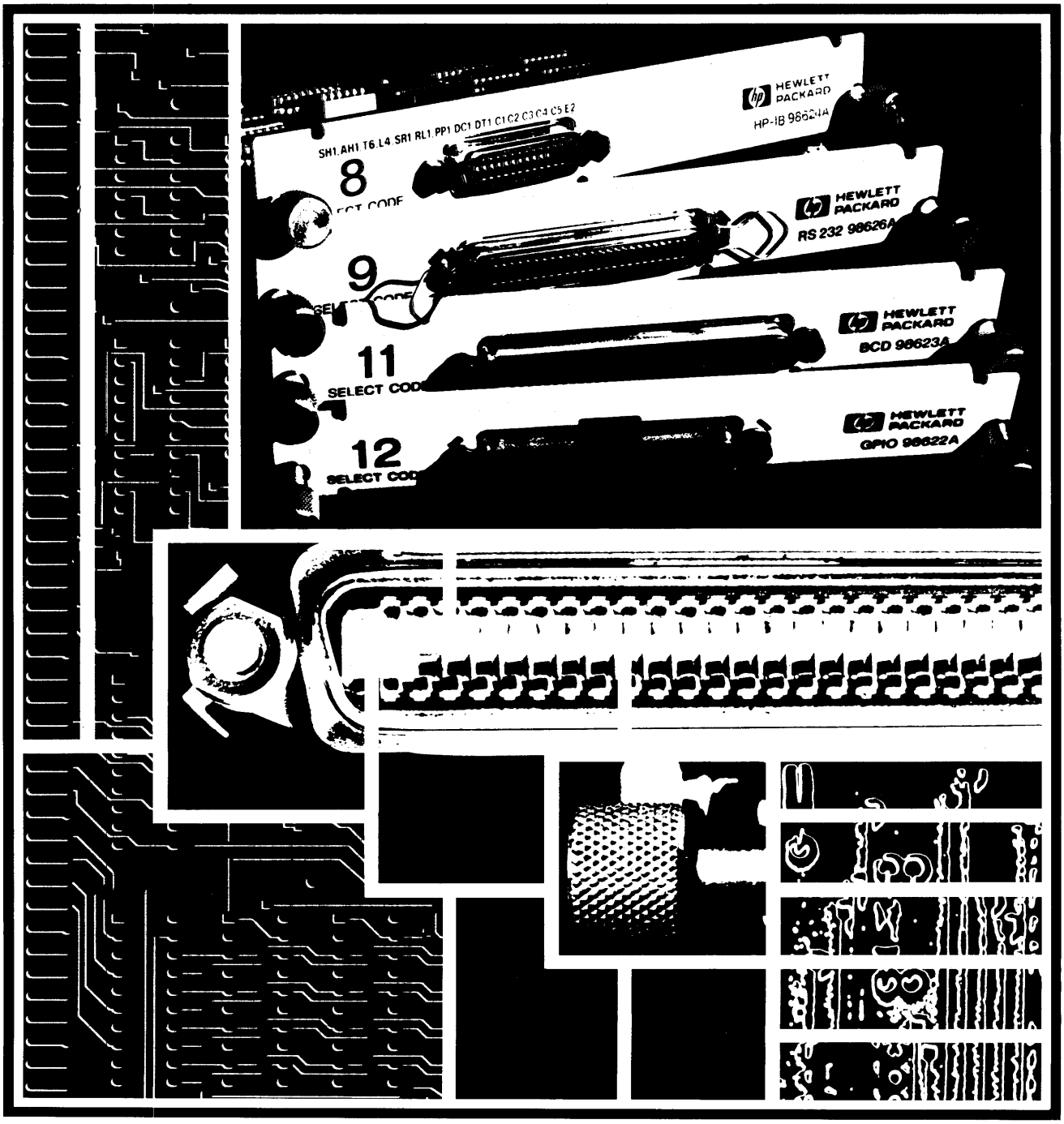
HP 98640A
7-Channel Analog Input Interface
Hardware
Installation and Reference Manual



HEWLETT PACKARD

HP Computer Systems

HP 98640A
7-Channel Analog Input Interface
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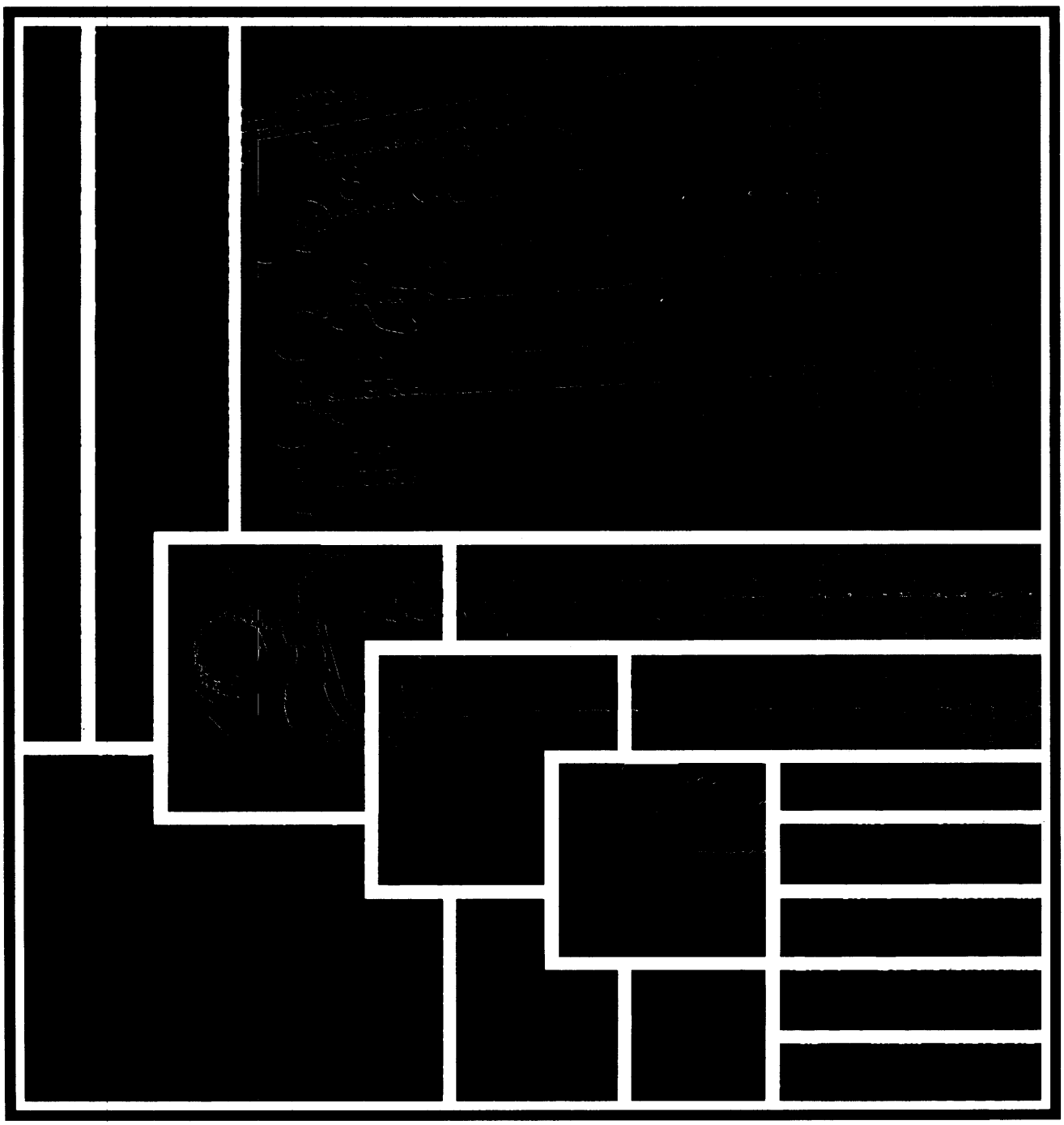

HEWLETT PACKARD

Warranty Statement

Hewlett-Packard products are warranted against defects in materials and workmanship. For Hewlett-Packard Desktop Computer Division products sold in the U.S.A. and Canada, this warranty applies for ninety (90) days from the date of delivery.* Hewlett-Packard will, at its option, repair or replace equipment which proves to be defective during the warranty period. This warranty includes labor, parts, and surface travel costs, if any. Equipment returned to Hewlett-Packard for repair must be shipped freight prepaid. Repairs necessitated by misuse of the equipment, or by hardware, software, or interfacing not provided by Hewlett-Packard are not covered by this warranty.

HP warrants that its software and firmware designated by HP for use with a CPU will execute its programming instructions when properly installed on that CPU. HP does not warrant that the operation of the CPU, software, or firmware will be uninterrupted or error free.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTIBILITY AND FITNESS FOR A PARTICULAR PURPOSE. HEWLETT-PACKARD SHALL NOT BE LIABLE FOR CONSEQUENTIAL DAMAGES.

*For other countries, contact your local Sales and Service Office to determine warranty terms.

HEWLETT PACKARD

ATTENTION:
Users of Series 300 Computer Systems

Please read this notice before installing card.

The HP 98640A has one application which may pose serious usage problems:
In Series 300 machines, the right angle posts which connect the ADC card to its Wire Termination Assembly can short out on the RFI suppression shield of the processor or other card if the cards are in adjacent slots. Since the HP 98640A must be installed in the lower of paired slots, this occurance is likely.

There are two possible solutions.

The recommended solution is to apply an insulating material (such as electricial tape) to the upper surface of the RFI shield on the processor or other card.

The second, while more difficult, is equally effective: Always place the ADC card in a slot where the contacts are clearly not touching any conductor. This is not always possible due to the installation constraint mentioned above.

HP 98640A

7-CHANNEL ANALOG INPUT INTERFACE

FOR HP 9000 SERIES 200 COMPUTERS

HARDWARE INSTALLATION AND REFERENCE MANUAL

Card Assembly: 98640-66501
Date Codes: A-2419
B-2420

HEWLETT PACKARD

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PRINTING HISTORY

The Printing History below identifies the Edition of this Manual and any Updates that are included. Periodically, update packages are distributed which contain replacement pages to be merged into the manual, including an updated copy of this Printing History page. Also, the update may contain write-in instructions.

Each reprinting of this manual will incorporate all past updates; however, no new information will be added. Thus, the reprinted copy will be identical in content to prior printings of the same edition with its user-inserted update information. New editions of this manual *will* contain new information, as *well* as updates.

FIRST EDITION.....July 1984

CONTENTS

PREFACE

The HP 98640A Analog Interface is designed to make putting an HP 9000 Series 200 computer in touch with the "real world" easy. In this manual we explain how to install the interface in your computer. We also present a very simple example of an assembly language program for making a single reading from an input. This example, in section four, is aimed at advanced assembly language programmers.

This manual's Appendix briefly explains how the HP 98640A Analog Input Interface may affect an existing application. A glossary follows the Appendix. Also in the back are two different reader comment forms. One form asks you to evaluate this manual, the other asks what follow-on products you may have a future need for.

One product that is already available is the HP 98645A Measurement Library. The library's set of subroutines that you can call from high level languages may save considerable development time. The following languages can call routines from the library:

BASIC 3.0 and 2.0 with 2.1 extensions
Pascal 3.0, 2.1, and 2.0

Contact your Hewlett-Packard sales representative for more information about the HP 98645A Measurement Library.

We strongly recommend the following books to anyone who intends to write his or her own assembly-language application programs for 9000 Series 200 computers:

- Pascal 2.0 System Designer's Guide, part number 09826-90074
- MC68000 User's Manual, part number 09826-90073

If you are interested in producing applications software, ask your Hewlett-Packard representative about HP+. We can help you get the word out about your application.

SAFETY CONSIDERATIONS

GENERAL - This product and relation documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

CAUTION

STATIC SENSITIVE DEVICES

When any two materials make contact, their surfaces are crushed on the atomic level and electrons pass back and forth between the objects. On separation, one surface comes away with excess electrons (negatively charged) while the other is electron deficient (positively charged). The level of charge that is developed depends upon the type of material. Insulators can easily build up static charges in excess of 20,000 volts. A person working at a bench or walking across a floor can build up a charge of many thousands of volts. The amount of static voltage developed depends on the rate of generation of the charge and the capacitance of the body holding the charge. If the discharge happens to go through a semiconductor device and the transient current pulse is not effectively diverted by protection circuitry, the resulting current flow through the device can raise the temperature of internal junctions to their melting points. MOS structures are also susceptible to dielectric damage due to high fields. *The resulting damage can range from complete destruction to latent degradation.* Small geometry semiconductor devices are especially susceptible to damage by static discharge.

The basic concept of static protection for electronic components is the prevention of static build-up where possible and the quick removal of already existing charges. The means by which these charges are removed depend on whether the charged object is a conductor or an insulator. If the charged object is a conductor such as a metal tray or a person's body, grounding it will dissipate the charge. However, if the item to be discharged is an insulator such as a plastic box/tray or a person's clothing, ionized air must be used.

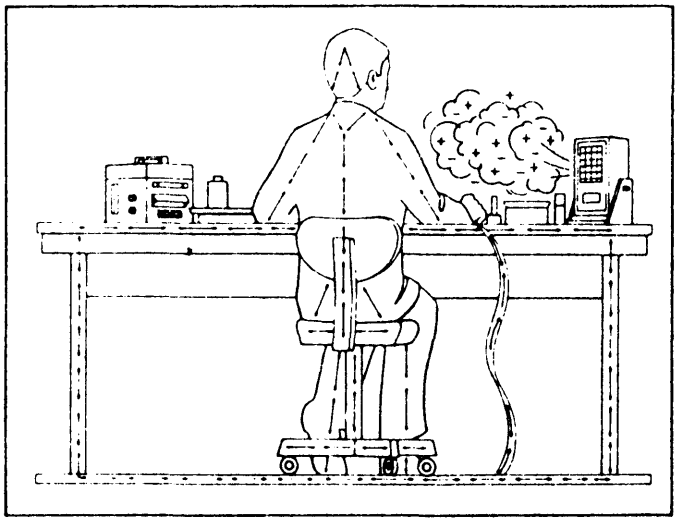
Effective anti-static systems must offer start-to-finish protection for the products that are intended to be protected. This means protection during initial production, in-plant transfer, packaging, shipment, unpacking and *ultimate use.* Methods and materials are in use today that provide this type of protection. The following procedures are recommended:

1. All semiconductor devices should be kept in "antistatic" plastic carriers. Made of transparent plastics coated with a special "antistatic" material which might wear off with excessive use, these inexpensive carriers are designed for short term service and should be discarded after a period of usage. *They should be checked periodically to see if they hold a static charge greater than 500 volts in which case they are rejected or recoated.* A 3M Model 703 static meter or equivalent can be used to measure static voltage, and if needed, carriers (and other non-conductive surfaces) can be recoated with "Staticide" (from Analytical Chemical Laboratory of Elk Grove Village, Ill.) to make them "antistatic."

2. Antistatic carriers holding finished devices are stored in transparent static shielding bags made by *3M Company.* Made of a special three-layer material (nickle/polyester/polyethylene) that is "antistatic" inside and highly conductive outside, they provide a Faraday cage-like shielding which protects devices inside. "Antistatic" carriers which contain semiconductor devices should be kept in these shielding bags during storage or in transit.

Individual devices should only be handled in a static safeguarded work station.

3. A typical static safeguarded work station is shown below including grounded conductive table top, wrist strap, and floor mat to discharge conductors as well as ionized air blowers to remove charge from nonconductors (clothes). Chairs should be metallic or made of conductive materials with a grounding strap or conductive rollers.



SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

WARNING

EYE HAZARD

Eye protection must be worn when removing or inserting integrated circuits held in place with retaining clips.

GENERAL INFORMATION

SECTION I

OVERVIEW

The HP 98640A 7-channel Analog Input Interface is an analog-to-digital converter (ADC) for Hewlett-Packard 9000 Series 200 computers. On each HP 98640A 8 analog channels are available for measuring small differential voltages with 13-bits resolution (including sign-bit). We call the HP 98640A a "7-channel" interface because in applications where an input offset voltage is less tolerable the two leads of one channel may be shorted together and grounded. The reading from the shorted channel serves as a reference you can use to correct readings made on the other channels.

The HP 98640A can sample its inputs in any order. You can control the amount of time between readings by programmatically setting the interface's pace timer. The interface will then do the pacing automatically. It can send an interrupt to the computer when a sample has been taken. Even the voltage range for a channel can be changed between samples. The maximum voltage for inputs is plus or minus 10 volts. The minimum full-scale voltage range is plus or minus 19.5 millivolts. The maximum differential voltage measurable is plus or minus 9.99756 volts (best case) at a gain of 1 (full scale voltage minus one least significant bit (lsb) value).

The interface's four input voltage ranges will accommodate signal sources ranging from control circuits to thermocouples. The voltage ranges are determined by the amplification of the input voltage by the card. You can select any of 4 gains for any channel. The four gain factors are 1, 8, 64, and 512. This allows the ADC integrated circuit (IC) on the card to always see a voltage between 0 and 10 volts.

The rest of this section describes the interface and includes the operational specifications.

DESCRIPTION

The HP 98640A is actually two printed circuit assemblies (PCA). The main PCA is the A-to-D card which includes the analog-to-digital converter, programmable gain amplifier (PGA), pace timer, and backplane interface circuitry. Unlike most interface cards for 9000 Series 200 computers, the cover plate is not attached to the main card. Instead, the plate is is attached to the second PCA.

The second PCA plus the attached cover plate is called the wire termination assembly (WTA). On this PCA are the wire termination blocks, input protection circuitry, and the control inputs for external pacing. The wire termination blocks accept individual solid hook-up wires up to 18 gauge. Each wire is clamped in a termination block's receptacle by turning a setscrew. The cover plate attached to the PCA has two captive thumbscrews (dog bolts) to secure the entire assembly to the back of the computer. The main PCA should never be operated unless a WTA or test assembly is attached.

NOTE

Additional wire termination assemblies may be ordered. By using several assemblies you can readily switch between several predetermined wiring arrangements. The assembly's part number is 98640-66502. Contact your HP representative or Hewlett-Packard's Corporate Parts Center (CPC) to place an order.

Also on the wire termination assembly are 9 termination receptacles tied to chassis ground and one receptacle tied to a low current (less than 50ma) +5 volt source, for use with the external control inputs. **THIS +5 VOLT SOURCE IS NOT INTENDED FOR USE AS A POWER SUPPLY.** The termination receptacles are listed in Section II.

STANDARD PRODUCT

When the HP 98640A was ordered one of three options had to be specified. The option specified determines what equipment you received. When you unpack the cards you may want to refer to the following lists:

Standard Product

- A-to-D card, part number 98640-66501
- Wire termination assembly (WTA), part number 98640-66502
- Test assembly, part number 98640-67950
- This installation manual, part number 98640-90001
- Verification option (only one may be selected)

Options

VERIFICATION OPTIONS

001 - Deletes test assembly
630 - Adds verification software on 3.5 inch disk, part number 98640-13301
655 - Adds verification software on 5.25 inch disk, part number 98640-13601

IDENTIFICATION

Five digits and a letter (98640A) identify the Analog Input Interface. As with most Hewlett-Packard products used with 9000 computers these five digits identify the product. The letter suffix represents the revision level of the product.

The main printed circuit assembly or PCA (printed circuit board with all components in place) is identified by a part number (also called a card assembly number) followed by a date code. On the

A-to-D card the part number is on the component side near the right-angle posts. The part number is 98640-66501. The line of characters below the part number is called the date code. It identifies the circuit (by letter) and electrical characteristics (the four-digit encoded date). If there is a suffix (typically a lower-case letter), it identifies additional revisions to the PCA.

If the date code on the A-to-D card does not correspond to the date code printed on the title page of this manual, there are differences between the interface described in this manual and the Analog Input Interface you have received. Contact your nearest Hewlett-Packard Sales and Service office (listed at the back of this manual) for manual update information.

SPECIFICATIONS

Electrical

Power Requirements:

.672W	(@ +12V)
.228W	(@ -12V)
+ 2.570W	(@ +5V)
3.5 Watts total	

Input overvoltage protection: Transorbs redirect voltage in excess of ±15 volts to ground.

Input resistance, each channel: 100megohms (power on)

WARNING

Each input is routed through a 1k (one thousand) ohm resistor to ground when the power is off.

Functional Specifications

On-board clock: 1.667Mhz

Resolution of Internally clocked Pace rate: 600 nanoseconds

Sample and hold aperture time: 25 nanoseconds

Time from first Read to Hold at 55k samples/second: 7 microseconds

Minimum sample cycle: 18µsec.

Linearity: 0.02% of full scale

Temperature coefficient for voltage offset: 10 microvolts per degree centigrade.

Common-mode rejection ratio (CMRR): 90db @ 60hz

Input voltage ranges: These ranges only specify the voltages acceptable at a particular gain. The differential voltage between a channel's inputs should not equal or exeed full scale (see below).

GAIN	INPUT VOLTAGE RANGE
1	+ to - 10V
8	+ to - 1.25V
64	+ to - 156mV
512	+ to - 19.5mv

Other sampling characteristics are listed in table 1-1.

Control

Minimum external trigger pulse width: 2.3 microseconds

Trigger voltage: +2 to +50volts (trigger voltage must not go below ground)

Table 1-1

SAMPLING CHARACTERISTICS

GAIN	1	8	64	512
FULL SCALE	±10V	±1.25V	±156mV	±19.5mV
LSB	2.44mV	305µV	38.1µV	4.77µV
RMS NOISE* STD DEVIATION	5mV	600µV	100µV	18µV
OFFSET AFTER CALIBRATION (WORST CASE)**	±7.3mV	±915µV	±152µV	±24µV
ACCURACY AFTER CALIBRATION (WORST CASE)**	±18mV	±3mV	±250µV	±75µV
INPUT AMPLIFIER SLEW RATE	400mV/µsec	50mV/µsec	4mV/µsec	40µV/µsec
MAX. SAMPLE RATE (ACROSS CHANNELS)	20k/sec	20k/sec	14k/sec	1k/sec
MAX. SAMPLE RATE (ON A SINGLE CHANNEL)	55k/sec	55k/sec	55k/sec	55k/sec

* By averaging readings noise can be reduced to less than one least significant bit (lsb).

** These figures are based on an HP 98640A whose data were processed and controlled by routines from the HP 98645A Measurement Library. The accuracy figures show the worst case affects of noise after the library's noise reduction routine is used.

INSTALLATION

SECTION II

UNPACKING AND INSPECTION

The procedures for unpacking this interface are described below. Please follow these procedures to preserve your rights under the laws governing freight shipments and to protect the hardware. You will find these procedures in many Hewlett-Packard hardware manuals.

Look for obvious signs of damage to the package. If the outside of the box is damaged or has water stains, or the box rattles, contact the carrier. Ask that a carrier's agent be present when you open the box. If there is no obvious reason to have the carrier's agent present read the cautions below and on the box before proceeding.

Cautions

Please read "Safety Considerations" at the front of this manual, especially the portion dealing with static electricity.

CAUTION

The A-to-D card (see figure 2-2 for an outline drawing of this card) contains static sensitive devices. Use anti-static handling procedures when working with it.

When you remove the A-to-D card from its packing material handle it by the edges or the plastic levers (extractors) in the corners next to the right-angle posts. Do not touch the gold-plated contacts at the end of the card opposite the right-angle posts. If you do get a fingerprint on the gold-plated contacts or the right-angle posts, clean them with a lintless tissue moistened with a small amount of isopropyl alcohol.

CAUTION

Never clean the contacts or the right-angle posts with an abrasive cleaner such as an eraser because the plating may be damaged.

Inspect contents

Check the contents of the package to verify that you have received the product and options you ordered. Refer to the description of the Standard Product and options in Section I, and your invoice. If any parts appear to be missing, notify your Hewlett-Packard Sales and Service office.

Inspect the contents carefully for hidden damage such as detached components, corrosion, or cracks and dents. Notify the carrier who delivered this product and your Hewlett-Packard Sales and Service office if you find any damage. Save the packing material for the carrier. A representative at our Sales and Service office will arrange for repair or replacement without waiting for the settlement of the claim against the carrier.

PREPARATION FOR USE

Calculating power requirements

Check your computer system manual to find how much power (in watts) is available from the computer's power supply at each voltage the supply provides. Add the power requirements at each voltage for all of the cards you already have in the computer. Then add the power requirements of each A-to-D card you will install to the totals.

If the power required at any voltage is greater than the power supply's rating at that voltage, you must make some adjustment to your computer. Either reconfigure your system by omitting unnecessary cards or arrange to buy bus expanders through your Hewlett-Packard Sales and Service office.

Component installation

There are no loose components to install on the A-to-D card or the wire termination assembly.

Boot-up ID number

The ID number of the card is a feature required by the operating system. The ID register on the card is hardwired to respond, "18", when polled during system boot-up. The operating system also checks the address (which we will explain how to set below) of the A-to-D card. The ID number and address are used by the operating system to associate the card with an application program.

SWITCH SETTINGS

The A-to-D card has a DIP (dual in-line package) block of switches (SW1) located as shown in figure 2-1. Switch numbers are on the switch block. These switches control the card's address and the priority level of any interrupt the card transmits. You must select part of the address for the card. The portion of the address you set on switches 1 to 5 is called the *select code*. The remainder of the address is already hardwired. If you use a program which requires the card to send a specific level hardware interrupt to the system, you must set the interrupt level the card will send before you install the card in the computer. Figure 2-1 shows the switches set as they are when the A-to-D card leaves the factory; the select code is 18 and interrupt level is 3.

The logical state of any switch corresponds to the numbers 0 and 1 silked-screened on the card just to the right of the block of switches (SW1). To set a specific select code or interrupt level just set the switches to the logical states shown in Table 2-2. When a switch is closed, the bit it controls is low (logical zero). When a switch is open, the bit it controls is high (logical one). You can use your fingernail or the tip of a ball-point pen to change a switch's setting.

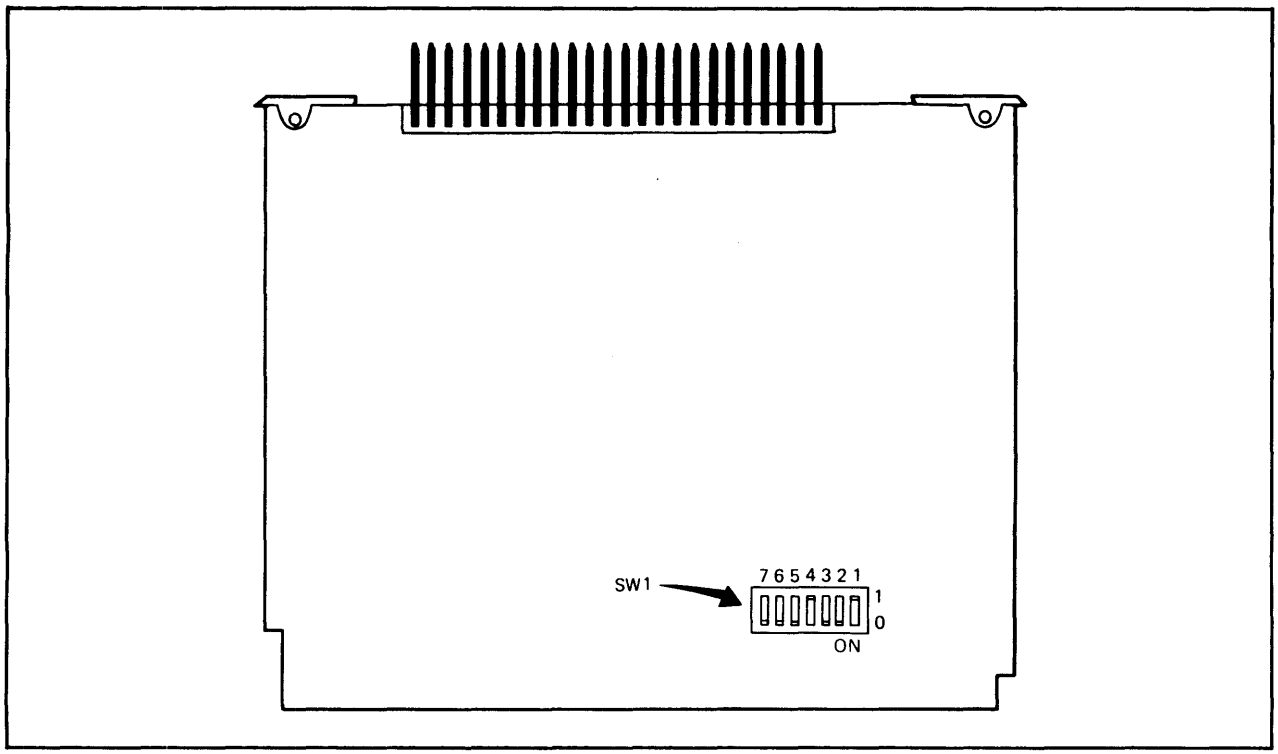


Figure 2-1. SW1 Location

Table 2-1. Standard device assignments.

STANDARD SELECT CODE ASSIGNMENTS

SELECT CODE	ASSIGNED DEVICE	SELECT CODE	ASSIGNED DEVICE
8	98624	19	- -
9	98626	20	98628
10	- -	21	98629
11	98623	22	- -
12	98622	23	- -
13	- -	24	- -
14	98625	25	- -
15	CUSTOM I/O #1	26	- -
		27	- -
16	CUSTOM I/O #2	28	98627 COLOR
		29	(color cont.)
17	- -	30	- -
18	98640	31	- -

Factory Settings

NOTE

When using BASIC or Pascal you must use a select code of 8 or higher. Codes 0-7 are reserved for the languages' internal input/output system.

The A-to-D card is shipped from the factory with the select code set to 18 and the interrupt level set to 3 (see table 2-2 for the switch settings).

INTERFACE SELECT CODES

SW1 Switches msb 12345 lsb	SELECT CODE	SW1 Switches msb 12345 lsb	SELECT CODE
01000	8	10100	20
01001	9	10101	21
01010	10	10110	22
01011	11	10111	23
01100	12	11000	24
01101	13	11001	25
01110	14	11010	26
01111	15	11011	27
10000	16	11100	28
10001	17	11101	29
10010	18	11110	30
10011	19	11111	31

HARDWARE INTERRUPT LEVELS

SW1 Switches 76	INTERRUPT LEVEL
00	3
01	4
10	5
11	6

Table 2-2. SW1 switch settings

Choose a select code for the A-to-D card which differs from that of any other interface card in your system. If you are using other interface cards at their "standard" select codes, Table 2-1 will help you locate the open select codes.

Interrupt Level

Switches 6 and 7 control the priority level of the interrupt the card can generate. The interrupt level must be set before the card is installed in the computer. See table 2-2 if you need to set an interrupt level that differs from the factory setting of 3.

INSERTING THE CARD

Where

CAUTION

Before inserting the A-to-D card be sure the computer or bus expander where you are going to install the card in is turned off. Any peripherals attached to the computer or expander box should be turned off also.

Refer to figure 2-2 while reading this explanation. Remove the cover plate from the computer that covers the accessory slot where you intend to install the A-to-D card. The card must be installed in any of the odd numbered card slots in the card cage of your computer. An odd-numbered slot is a slot just below the threaded mounting holes for a cover plate. Unlike many I/O devices for 9000 Series 200 computers, a cover plate is not attached to the A-to-D card so you can actually seat the card in the wrong slot.

How

To install the A-to-D card pickup the card by the corners where the extractors (plastic levers) are attached. Be sure the component side of the card is up. Check for any fingerprints on the contacts of the top (component side) and bottom of the card. Clean the contacts, as necessary, with a non-abrasive cleaner. Make a final check that the switches are set correctly.

CAUTION

The pressure required to seat the A-to-D card may be sufficent to cause some 9000 Series 200 computers to move.

Now, line up the card with the grooves in the card cage and begin to gently push the card into the grooves. Push until about one-half inch (1 5mm) of the A-to-D card projects from the card cage. Let go of the card, fold the extractor levers flat against the card and use your thumbs to push the card into place with a firm, even pressure. If you push on the extractors there is less of a chance you will accidentally damage one of the right-angle posts.

WARNING

THE RIGHT-ANGLE POSTS ARE SHARP ENOUGH TO CUT YOU IF YOU PUSH ON THEM.

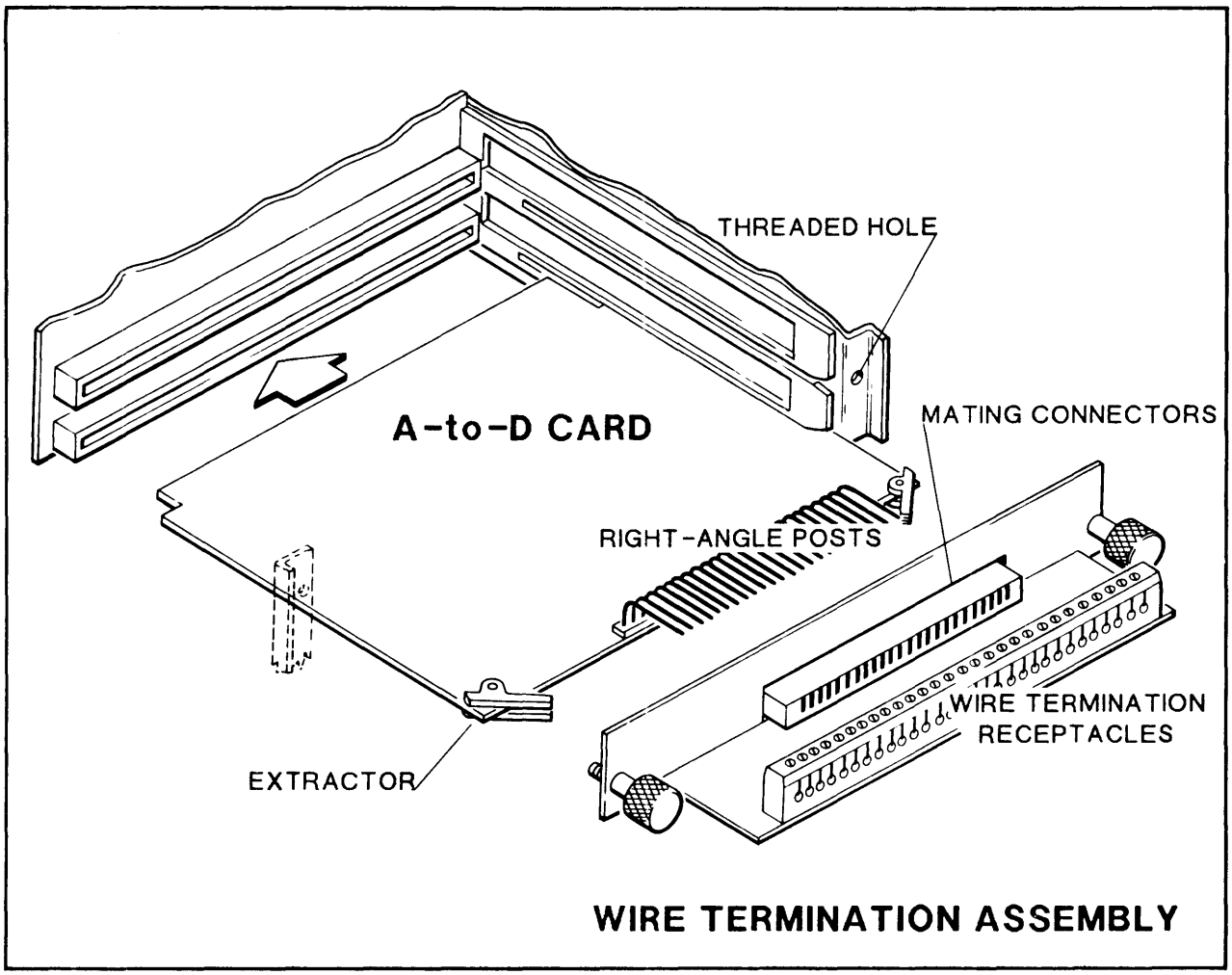


Figure 2-2. Installation

The A-to-D card must seat in order for the wire termination assembly to fit on the back of the computer. When correctly installed the card's extractors will be folded flat against the card with one edge of each extractor touching or almost touching the card cage.

Removal

CAUTION

The following instructions for removing the A-to-D card assume you have properly powered-down the computer and removed the wire termination assembly as explained in Section 5 under the heading "DISCONNECTING THE WTA". If you have not turned the power on yet, then the instructions below apply.

To remove the A-to-D card, pull the edge of the extractors nearest the right-angle posts outward. As the extractors swing outward their tips will pivot against the card cage and jack the card free of connectors at the other end. When the card is free of the connector, grasp the corners of the card and slowly slide it out of the card cage.

Checking a new A-to-D card

This is a good time to checkout the card's operation--before the wire termination assembly is attached. See Section 5 under the heading "Preparing to Test the A-to-D Card". Once you have verified the card is operating correctly, return to this section for an explanation of installing the wire termination assembly.

ATTACHING THE WIRE TERMINATION ASSEMBLY

Refer to figure 2-2 for help installing the wire termination assembly. Pick up the wire termination assembly and orient it such that the thumbscrews line up with threaded holes in the card cage and the mating connectors for the right-angle posts on the A-to-D card are also lined up.

Push the cover plate forward until the mating connectors engage the posts and the thumbscrews just enter their respective holes in the card cage. Tighten both screws simultaneously or they may bind. Tighten until the cover plate is seated against the card cage's outside edges. Tighten only finger tight; over-tightening may strip the threads of a thumbscrew or the card cage.

CAUTION

The right-angle posts must properly engage the mating connectors on the wire termination assembly. There is a connector for every post and no extras. The A-to-D card and/or the wire termination assembly may be damaged if power is applied with a post shorted to the cover plate or in the wrong receptacle of the mating connector.

If the thumbscrews bind do not force them. Unscrew the assembly and try again. If, after several trys you are unable to seat the cover plate you may have defective screws. Please contact the nearest Hewlett-Packard Sales and Service office. If the thumbscrews are defective, we will help you obtain a replacement wire termination assembly. Do not attempt to substitute conventional screws for the thumbscrews as you will void your warranty and may damage the card cage.

CAUTION

The A-to-D card may be damaged if the entire Analog Input Interface is not properly installed. Hewlett-Packard will not support an improperly assembled Analog Input Interface. You must operate the A-to-D card with either our wire termination assembly or our test assembly installed.

The wire termination receptacles on the wire termination assembly are arranged as shown in figure 2-3. You can open the throat of each receptacle by turning the screw above that receptacle counter-clockwise (as viewed from above) with a small, straight-bladed screwdriver.

CABLING

Wire

Since the HP 98640A Analog Input Interface measures differential voltage there must be at least two conductors coming from the voltage source you will measure. Your voltage source should have its own ground reference in any circuit that includes the interface . Where desired shielded cable may be used for the hook-up. For easy hook up to the wire termination assembly, we recommend insulated solid wire of any American Wire Gauge (awg) between 28 to 18 inclusive. Stranded wire may be used but should be tinned with solder to hold the strands together.

NOTE

You must provide strain relief for the wires attached to the wire termination assembly. The wire termination assembly is not designed to support the weight of a large cable or long lengths of individual conductors.

Connection

WARNING

THIS INPUT INTERFACE WILL APPEAR TO BE A LOW-RESISTANCE PATH TO GROUND FOR ANY VOLTAGE MORE THAN 15 VOLTS ABOVE OR BELOW GROUND.

WHEN POWER TO THE COMPUTER IS TURNED OFF EACH INPUT IS SHORTED TO GROUND THROUGH A ONE THOUSAND OHM RESISTOR REGARDLESS OF THE VOLTAGE ON THE INPUT.

Open the throat of the receptacle where you will install a wire by turning the screw above the opening counter-clockwise (as viewed from from above). Set the wire you will use in your strain-relief device but leave enough slack to reach the termination assembly and allow for stripping the wire. Strip between one-quarter and 9/32 inch (6 to 7 millimeters) of insulation from the end of the wire. Insert the bare wire into the receptacle and turn the screw clockwise (as viewed from above) until the wire is held firmly. Do not over tighten the screw as you may damage the termination block or the slot in the screw's head.

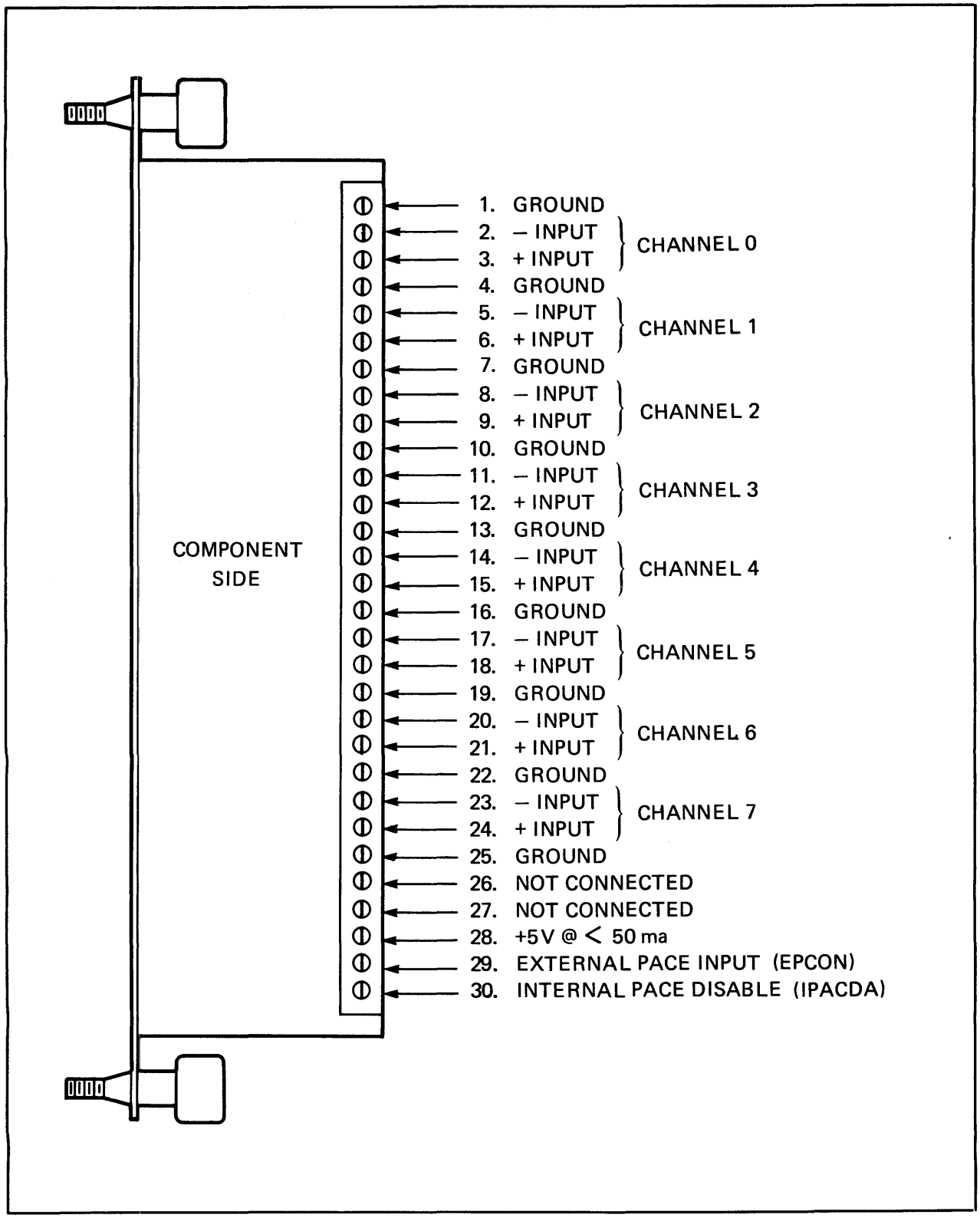


Figure 2-3. Wire termination assembly inputs.

Figure 2-4 shows the two recommended hook ups for a reference channel. Any channel may serve as a reference channel. If you determine by experiment that the offset voltages on an input channel are acceptable in your application, you can use all 8 channels for making measurements.

Figure 2-5 shows a few ways to wire a channel so a voltage source can be measured. Appendix A shows a possible circuit application. There are many circuits into which the interface can be added to make voltage measurements. We will not try to list them here.

Figure 2-6 has examples of hook-ups which are not recommended. The two problems the wiring arrangements in figure 2-6 cause are ground-loops or overvoltage on an input. A ground-loop will contribute unwanted noise to the input voltage. Also, if the difference in potential between chassis ground and the voltage source's ground is high enough, the current limiting resistor on the wire termination assembly may be damaged.

Once you have finished adding the wires to the wire termination assembly and the voltage sources you may wish to use cable ties to form the wires into bundles. If you have several wire termination assemblies you can fabricate several wire bundles allowing a rapid change of the 7 or 8 circuits you are making your measurements from.

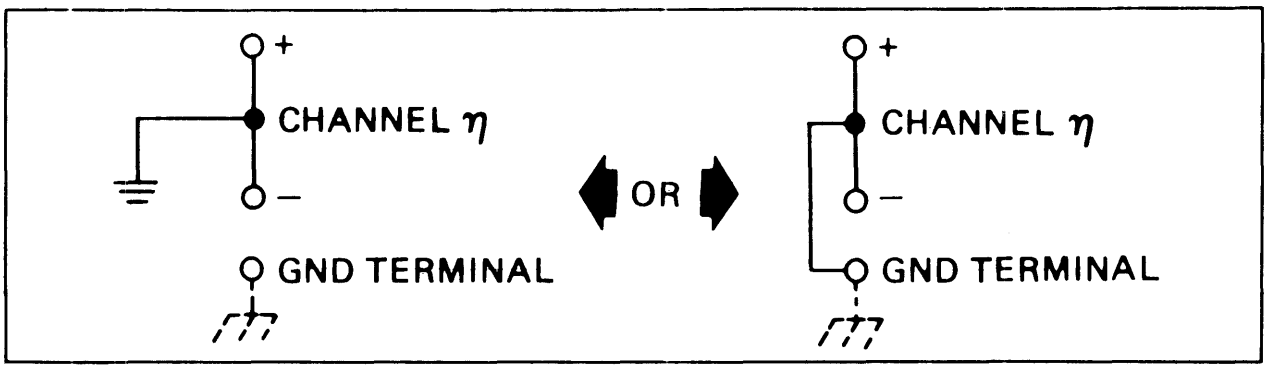


Figure 2-4. Wiring a reference channel.

CAUTION

Read Appendix A before you configure your system. The resistance between any input and ground is low when the A-to-D card's host is powered down.

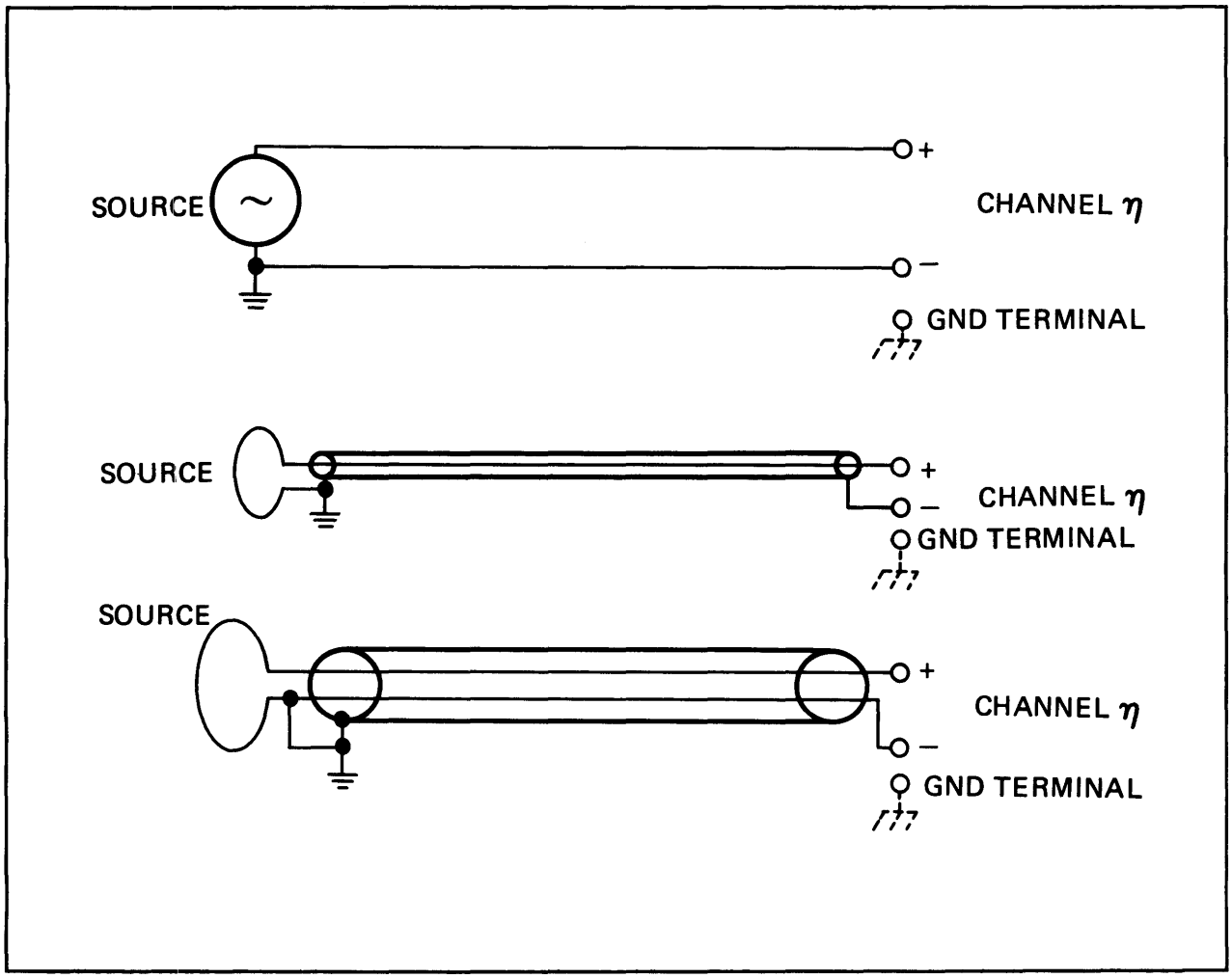


Figure 2-5. Wiring a channel's inputs.

Removal

WARNING

THESE INSTRUCTIONS FOR REMOVING THE WIRE TERMINATION ASSEMBLY ASSUME THE COMPUTER AND THE VOLTAGE SOURCES BEING SAMPLED ARE TURNED OFF. IF THEY ARE NOT, READ APPENDIX A BEFORE TURNING THE POWER OFF.

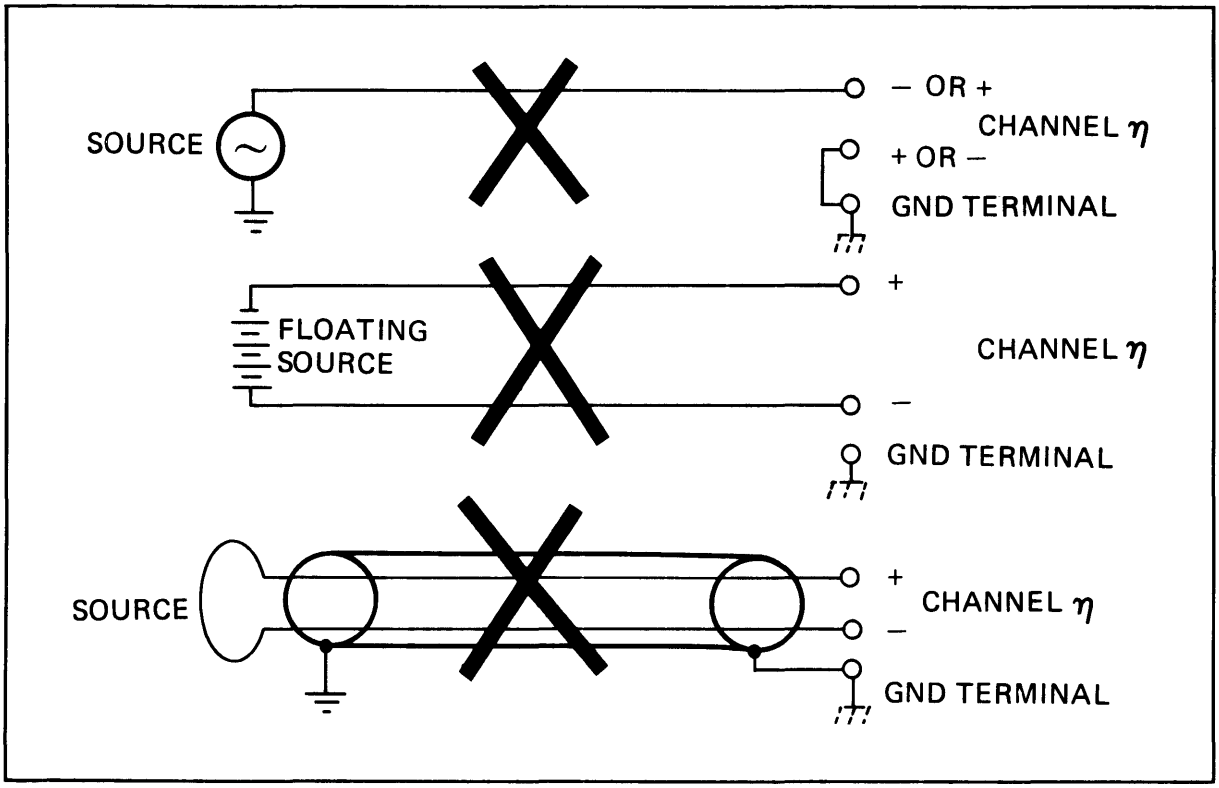


Figure 2-6. Unacceptable wiring of the inputs.

Be sure there is enough slack in the wires attached to the wire termination assembly to allow the assembly to be pulled straight back. If there is not enough slack you will have to remove the wires or release them from the strain relief.

Remove the assembly by unscrewing the two thumbscrews simultaneously to avoid binding caused by the plate not coming off straight. Be prepared to support the wire termination assembly as the screws run out. Pull the assembly straight back, away from the card cage, to avoid bending the the right-angle posts on the A-to-D card.

Do not use the wire termination assembly to hang up your wire bundle. The weight of the wire may cause damage to the assembly or the wires might slip out of the receptacles.

OPERATIONAL CONSIDERATIONS

The bottom of the wire termination assembly is exposed; do not allow conductors to come in contact with the bottom of the assembly when it is installed. If the computer is turned on or there is a voltage present on one of the channels, a short-circuit may result. The current through the short-circuit may be enough to damage the voltage source or the metal traces on the wire termination assembly, or both. If the traces on the wire termination assembly are damaged, you may purchase a replacement through your Hewlett-Packard Sales and Service office or our Corporate Parts Center (CPC). The part number is given in the description of the standard product in Section 1.

RETURN SHIPMENT

If any item needs repair, send it to your Hewlett-Packard Sales and Service office. Attach a tag to the item with the owner's name and address on it. Also, on the tag include a description of the service needed.

Pack the product in the original packing material. Please observe the anti-static-electrical procedures described at the front of this manual under the heading "Safety Considerations". If the original packing material is missing, you may use an equivalent commercially available anti-static packing material.

You may also have a reliable commercial packing company repack the item. Be sure to advise them the item being shipped is static sensitive.

THEORY OF OPERATION

SECTION III

This section describes the operation of the HP 98640A A-to-D card in considerable detail. To follow this description you should have a good working knowledge of the operation of the DIRECT-I/O backplane. If you need to beef up your background in this area, we suggest that you read the Pascal 2.0 System Designer's Guide (part number 09826-90074).

We will break our discussion down into the following topics:

Power and timing circuitry -- brief description of the power supply and the system clock.

Registers -- description of the registers that can be accessed via the backplane.

Analog circuitry -- description of the circuitry that transfers signals from the analog inputs to the analog-to-digital converter (ADC).

Digital conversion circuitry -- description of the section that controls the data conversion.

Digital backplane circuitry -- description of the backplane interface.

Sequence of operations -- summary of the interactions of the analog and digital sections; essentially an annotated timing diagram.

Analog pipeline -- summary of the interrelationships of successive analog readings.

Note that in this section we use the term "analog read" to refer to a read from one of the eight analog input channels on the A-to-D card, as contrasted with a read (or write) from (or to) the status, ID, or pace timing register.

In our discussion we will frequently refer to integrated circuits (ICs) by their "U" numbers. These U numbers can be found on the schematic diagrams of the card (in Section 7 of this manual) and in the replaceable parts list (in Section 6). We will make occasional references to schematic locations by grid numbers; these grid numbers are found on the outer edges of the schematic diagrams. Also, we will refer to two asynchronous state machines: the BUSY state machine and the Conversion state machine. Though running asynchronously, these state machines do influence each other.

In this section we will use the following convention for signals:

"BUSY" indicates a signal which is positive true.

"BUSY-" indicates a signal which is negative true.

Figure 3-1 shows a generalized functional block diagram of the A-to-D card.

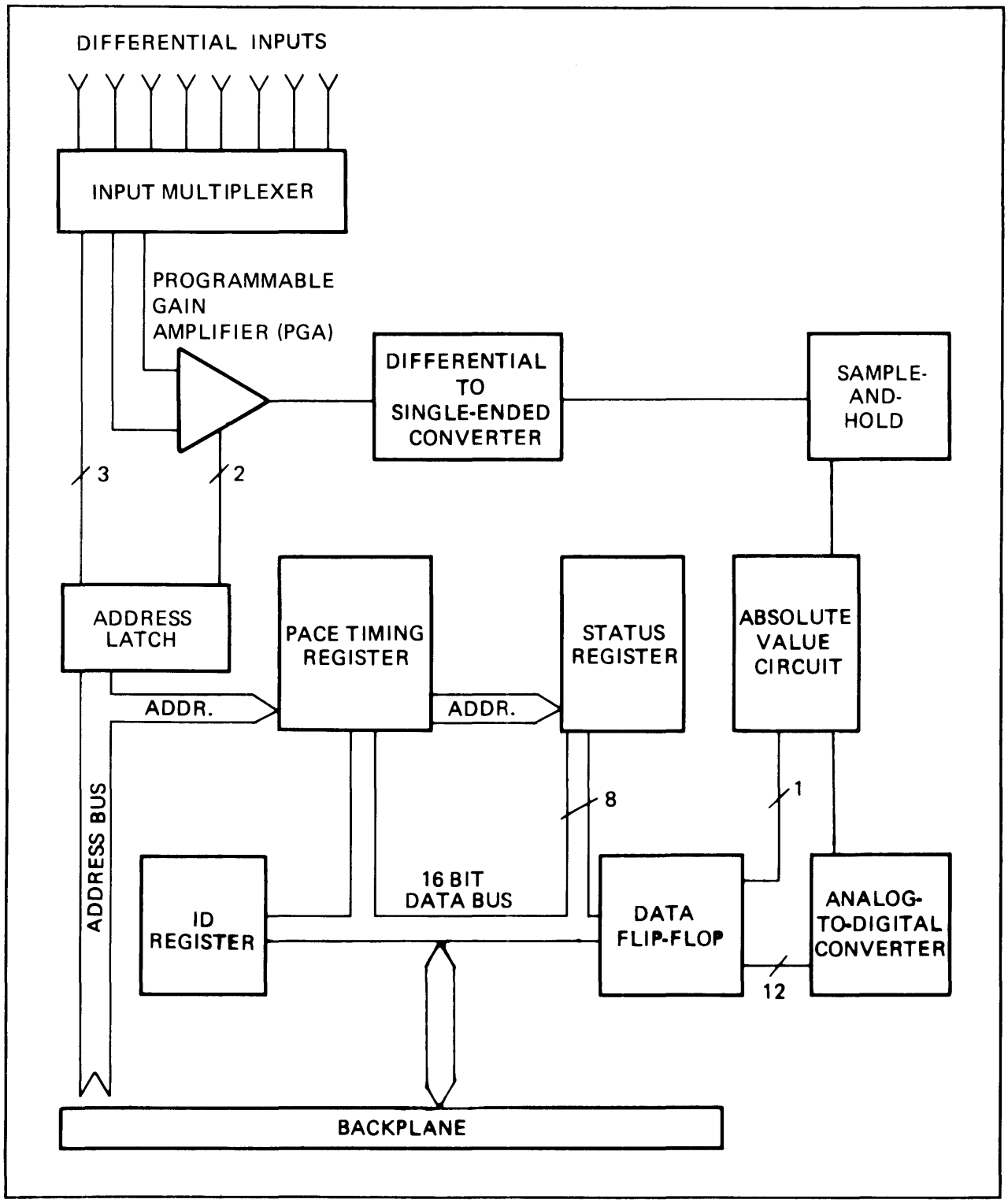


Figure 3-1. A-to-D card functional block diagram

POWER AND TIMING

Card Power Supply

The power that drives the A-to-D card is supplied by the host computer. The +5 volt, +12 volt, and -12 volt supplies come off the backplane and pass through appropriate inductors and capacitors to help stabilize the voltages. The +5 volt supply is also routed to terminal 28 on the wire termination assembly. (This voltage is supplied for your convenience in external pacing applications; it is not intended to be a general purpose power supply.)

System Clock

The system clock signal (SYCLK) for the A-to-D card is generated by the clock chip, U100. Since the clock generates TTL levels, no interface circuit is needed. The clock frequency is 1.667 MHz, or one clock cycle every 600 nanoseonds, hence the minimum increment available for internal pacing. Note that the clock on the card is not synchronized with the host computer's clock.

REGISTERS

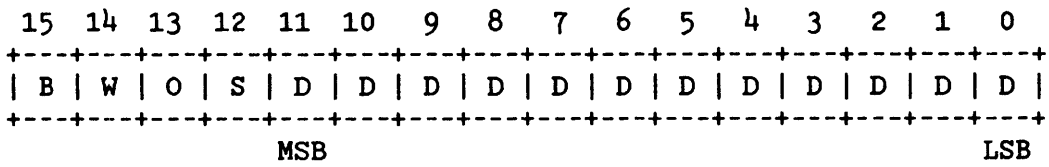
Data Registers

To make an analog read from the A-to-D card, you must specify a register address in your read request. The register address encodes the channel you want to read, and the gain at which you want to read it, in the following way:

Channel	Address for gain of 1	Address for gain of 8	Address for gain of 64	Address for gain of 512
0	64	80	96	112
1	66	82	98	114
2	68	84	100	116
3	70	86	102	118
4	72	88	104	120
5	74	90	106	122
6	76	92	108	124
7	78	94	110	126

For example, if you wanted to read from channel 3 at a gain of 8, you would specify a register address of 86 in your read request.

The value returned by an analog read is the voltage for the channel and gain specified <u>two analog reads previously</u>. (Refer to the paragraphs on the "Analog Pipeline" at the end of this section for a fuller explanation of this phenomenon.) The format for the returned value is:



where:

B = busy. If this bit is set to 1, the card is busy; the remaining bits in the data word are invalid, and the address provided in the read request is not accepted by the card. If this bit is set to 0, the data word is valid and the address is latched by the address latch on the card. This bit is the inverse of bit 6 of the status register.

W = wait. If this bit is set to 1, the card is in the wait state and the analog read will not be properly paced (according to the value programmed into the pace timing register). If this bit is set to 0, the card is not in the wait state and the read will be properly paced.

O = common mode overrange. This bit is negative true. If this bit is set to 0, a common mode overrange occurred during the reading; the value in the remainder of the data word is invalid. If this bit is set to 1, no common mode overrange occurred during the reading.

S = sign. If this bit is set to 0, the voltage value in the D bits is positive. If this bit is set to 1, the voltage value is negative.

D = data. These twelve bits give a binary value for the magnitude of the voltage. Bit 11 is the most significant bit (MSB); bit 0 is the least significant bit (LSB). This is the raw value provided by the ADC on the card; it has not been adjusted for gain.

The meanings of these bits are covered in greater detail in the remainder of this section.

Pace Timing Register

The pace timing register controls the pace interval between readings. This is a 16-bit register located at register address 4 on the A-to-D card. To calculate the register value that corresponds to a given pace period, use:

FFF6(hex) - *round*((period - 0.000018) / 0.0000006)

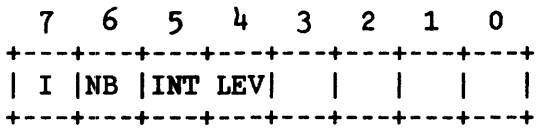
where period is the desired pace interval in seconds, and where *round* is a function that rounds a value to the nearest integer. To place that value into the pace timing register, simply write the value to register address 4. The A-to-D card allows pace periods from 18 microseconds to 39.3390 milliseconds, with a resolution of 600 nanoseconds.

ID Register

The ID register is an 8-bit register hard-wired with a value of 18 (the ID number of the A-to-D card). It is located at register address 1 on the A-to-D card. Reading from this register returns a value of 18. Writing to this register causes a soft reset of the A-to-D card; this sets the BUSY bit to 0 and resets the PROM counter to 0.

Status Register

The status register is an 8-bit register located at register address 3 on the A-to-D card. Its bits have the following meanings:



where:

I = interrupts. If this bit is set to 1, the card is enabled to interrupt the CPU every time it takes an analog reading. If this bit is set to 0, interrupts are not enabled. This is the only bit in this register that can be written to.

NB = not busy. If this bit is set to 0, the A-to-D card is busy. The card can not accept an address while it is in the busy state, and any voltage value read from the data register while the card is busy is invalid. If this bit is set to 1, the card is not busy; a voltage value read from the data register is valid, and the card can accept a new address for an analog read. This bit is the inverse of bit 15 of the data register.

INT LEV = interrupt level. Bit 5 and bit 4 are set by switches 7 and 6, respectively, on switch pack SW1. These two bits show the interrupt level of the card, and indicate which interrupt line is activated when an interrupt occurs. The meanings of the bits are:

Bit 5	Bit 4	Interrupt Level	Interrupt Line
0	0	3	IR3
0	1	4	IR4
1	0	5	IR5
1	1	6	IR6

ANALOG CIRCUITRY

The analog circuitry on the A-to-D card takes a differential input voltage from one of the eight analog input channels, amplifies it (if you tell it to), and prepares it for conversion to a digital value by the analog-to-digital converter. The next several paragraphs will trace that process.

Voltage Input

The input for the differential voltage to be measured is on the wire termination assembly that attaches to the A-to-D card proper. (The schematic diagram for this assembly is shown in Section 7 of this manual.) The input wiring is connected to the assembly by screw terminations. The input signals are routed to the A-to-D card proper, with overvoltage protection provided by transorbs (back-to-back zener diodes) connected to ground. This arrangement limits the maximum signal going to the card to the range of 14 to 20 volts. In addition, the analog ground of the card is protected by a resistor and a transorb, to guard against possible hazards caused by accidental connection of a signal line to ground.

The voltage input on the A-to-D card proper is found at location D-18 on the schematic diagram. This is where the voltage from the wire termination assembly enters the A-to-D card. A typical input is shown in detail in figure 3-2. The input voltages enter through 1000-ohm resistors contained in resistor arrays U61 and U71. These packs each contain 8 series resistors, and limit current to the overvoltage protection that follows. The overvoltage protection consists of two rail voltages (+10 volts and -10 volts), defined by diode CR1 for the positive side and by diode CR2 for the negative side. Each input signal path has a reverse-biased diode connecting it to each of the rail voltages. These diodes are contained in diode arrays U62 and U72.

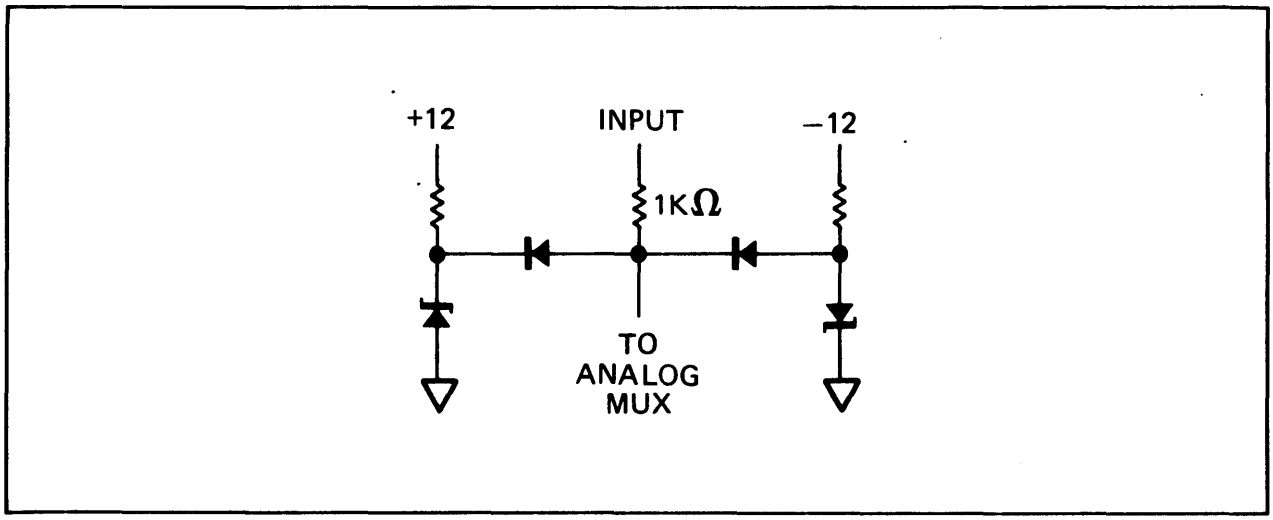


Figure 3-2. Input circuit

Resistors R5 and R6 maintain current through the zener diodes to keep them in the breakdown state. In the case of an overvoltage condition, the input voltage will exceed the zener value plus 0.7 volts. This will forward bias the appropriate diode in one of the arrays and allow current to flow through the zener diode. At this time the voltage at the diode array will not exceed approximately 10.7 volts and the rest of the voltage will be dropped across the 1000-ohm resistor. This circuit protects the inputs to the analog multiplexer (mux), U64, from overvoltage conditions at the inputs.

NOTE

The limitation on the amount of overvoltage depends on power dissipated by the 1000-ohm, 1/4-watt resistor: if too much voltage is applied, the resistor will fail.

All of the analog inputs are protected in this way.

Channel Selection

Channel selection is accomplished by U64, an analog multiplexer (mux). This mux switches one of eight differential channels into the programmable gain amplifier (PGA). Its operation is controlled by address lines AA1, AA2, and AA3, on pins 17, 16, and 15 of U64. The differential outputs, across pins 2 and 28 go directly into the positive inputs of op amps U44 and U54.

WARNING

THE ANALOG MUX SHORTS EACH INPUT TO GROUND THROUGH A 1kOHM RESISTOR WHEN POWER IS NOT APPLIED.

Programmable Gain Amplifier (PGA)

The PGA consists of two op amps (U44 and U54), an analog mux (U45) and a custom precision resistor network (U24). Figure 3-3 is a diagram of the PGA, and figure 3-4 shows the innards of the precision resistor network.

The PGA selects the gain for a reading by selecting the appropriate string of resistors from the network in U24. (This selection is accomplished by the analog mux, based on the values of address lines AA4 and AA5.) The resistor string thus selected becomes part of the feedback circuitry for the op amps.

An op amp's goal in life is to have its + input at the same voltage as its - input. When an op amp's output voltage is fed back into one of its inputs, the op amp can approach its goal (equal voltages at the inputs) by varying its output in some suitable manner. In the case of the PGA, the differential input voltages are brought into the + inputs of the two op amps. The output of each op amp is fed back into its - input.

GAIN OF 1

For a gain of 1, the operation of the feedback circuit for a single op amp is simple:

1) The input voltage comes in at the + input.

2) The op amp produces an equal output voltage.

3) That equal output voltage is fed directly back to the - input.

4) The op amp detects that the voltages at the two inputs are equal, and leaves things as they are. The resulting stable output voltage is available for use by the next stage of the analog circuitry.

Thus, for a gain of 1, the two op amps simply pass their input voltages on to the next stage.

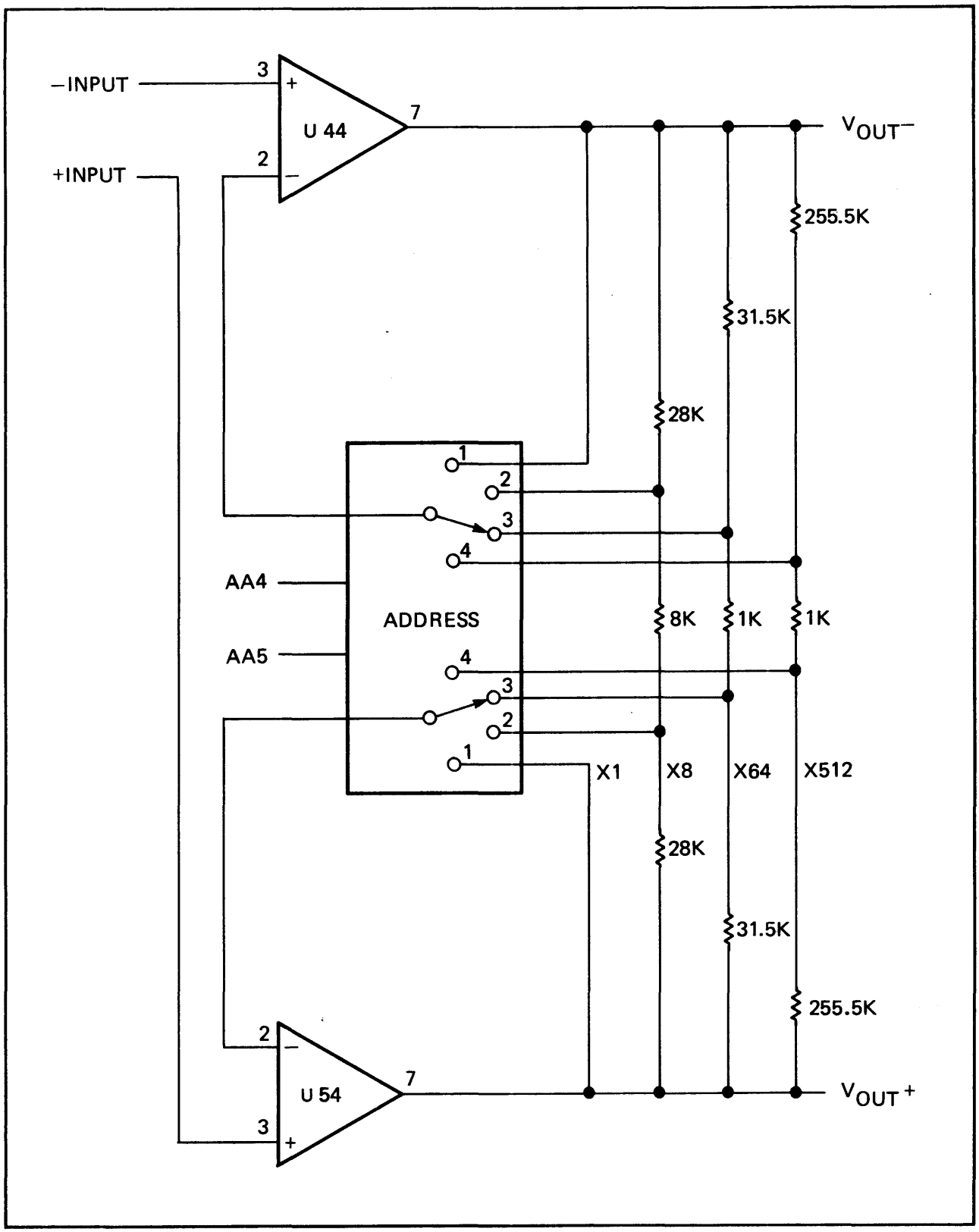


Figure 3-3. Programmable gain amplifier

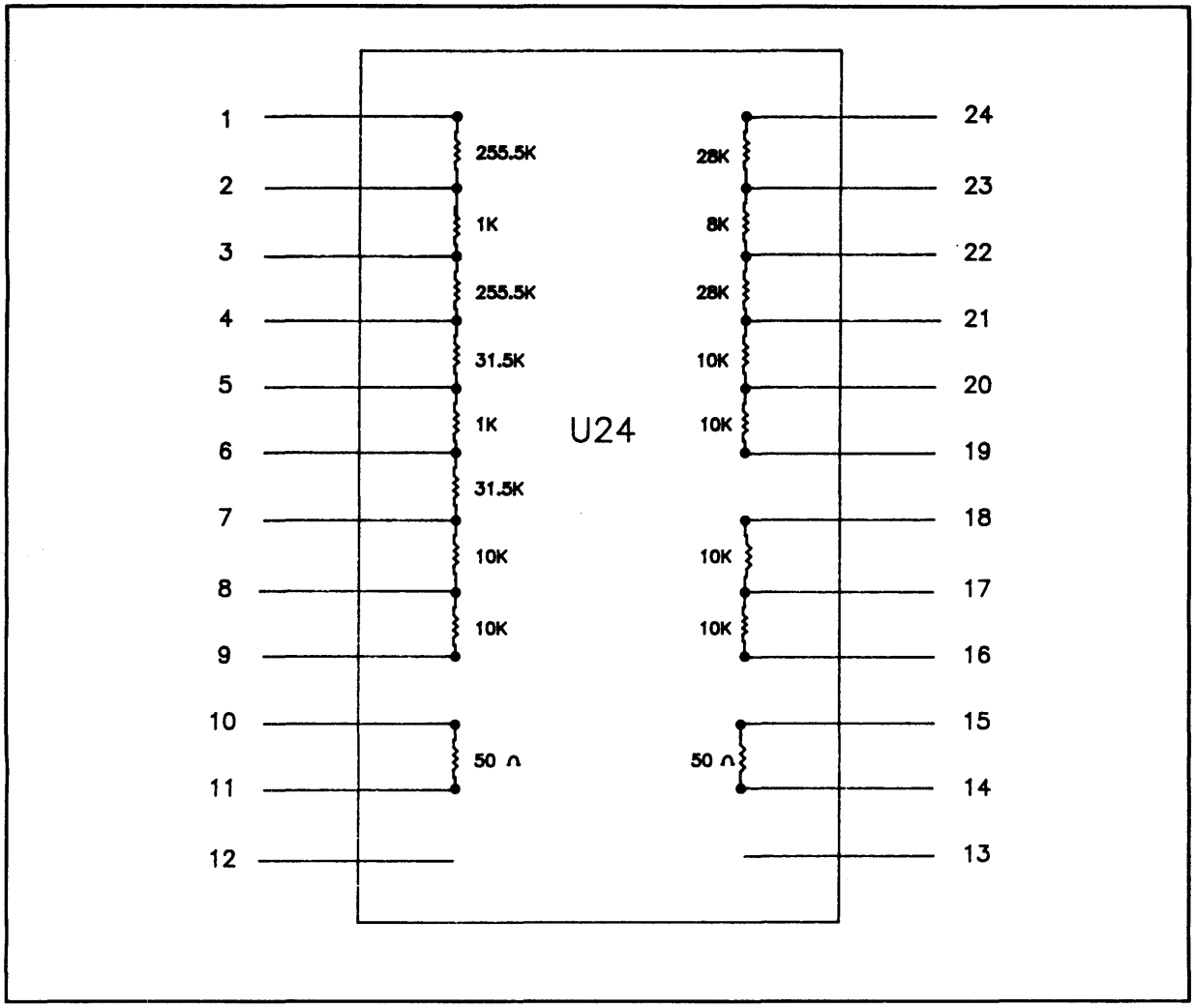


Figure 3-4. Precision resistor network (U24)

OTHER GAINS

The situation is slightly more complicated for gains greater than 1, since the resistor strings actually connect the two op amps together. As long as there is a difference between the two inputs, the op amps will have to adjust their outputs in order to equalize the voltages at their respective + and - inputs. When the circuit has reached equilibrium, the difference between the op amp output voltages will have been amplified by the appropriate gain factor. Let's look at an example.

Example
Assume that your A-to-D card is connected to a device that is supplying +3.01 volts to the + input of a channel and +3.00 volts to the - input. Assume also that you are measuring that voltage at a gain of 512. The + input (pin 3) of op amp U54 will see a voltage of +3.01 volts, and the op amp will adjust its output until the - input (pin 2) sees the same voltage. Similarly, the + input of U44 will see a voltage of +3.00 volts, and the output will adjust until the - input sees the same voltage.

In the equilibrium state, there will be a difference of 0.01 volts between the - inputs of the two op amps. As a result, there will be a current of 10 microamps flowing in the 1 kohm resistor in the feedback string. From this, we can calculate that the voltage across each of the 255.5 kohm resistors in the string will be 2.555 volts.

Thus, the output voltage from the positive op amp will be +3.01+2.555=+5.565 volts, and the output voltage from the negative op amp will be +3.00-2.555=+0.445 volts. The differential output from the op amps is 5.12 volts, which is 0.01 volts multiplied by a gain of 512.

The only time that the PGA does not work properly is when an input voltage causes an op amp to try to drive its output past ±10 volts. At that point the output clips and you have a common mode overrange condition.

Differential-to-Single-Ended Converter

The differential-to-single-ended converter is used to translate the differential output of the PGA to a single-ended voltage that the Sample and Hold (S/H) circuit can handle. The gain through this converter is unity (1). The resistors in this circuit are contained in the precision resistor network (U24), since high precision is necessary to keep the voltages accurate. Figure 3-5 is a diagram of the converter circuit.

The voltage at the positive input of the op amp (U32) is half the voltage coming from the positive op amp of the PGA (Vin+), due to the resistive divider network in U24. Similarly, the voltage at the negative input of op amp U32 is half way between the output voltage of U32 (Vout) and the voltage coming from the negative op amp of the PGA (Vin-). Op amp U32 drives its output (pin 7) so that the voltages at its negative input (pin 2) and positive input (pin 3) are equal; the resulting output voltage equals the difference between the positive and negative voltages coming from the PGA.

Example
Consider the case where the voltages coming in from the PGA (Vin+ and Vin-) are -3 volts and +1 volt: The voltage at the + input of the op amp is -1.5 volts. The op amp will drive its output (Vout) so that a voltage of -1.5 volts is present at the - input also. The output voltage thus produced will be -4 volts, and this voltage will be sent to the sample and hold circuit.

The two 330 pf capacitors in the converter circuit act as a low pass filter, which helps to reduce high frequency noise in the circuit.

Sample and Hold (S/H) Circuit

The S/H circuit (U12) is used to maintain a steady voltage to the analog-to-digital converter. Capacitor C4 is the hold capacitor for this circuit, and the BUSAMP (buffered sample) signal is the state control signal. When BUSAMP is high, the S/H circuit is in the sample mode and the capacitor is being charged with the voltage applied at pin 3. When BUSAMP is low, the S/H circuit is in hold mode, maintaining the voltage that it was charged to during the sample period. The S/H output (pin 5) feeds the next portion of the circuit.

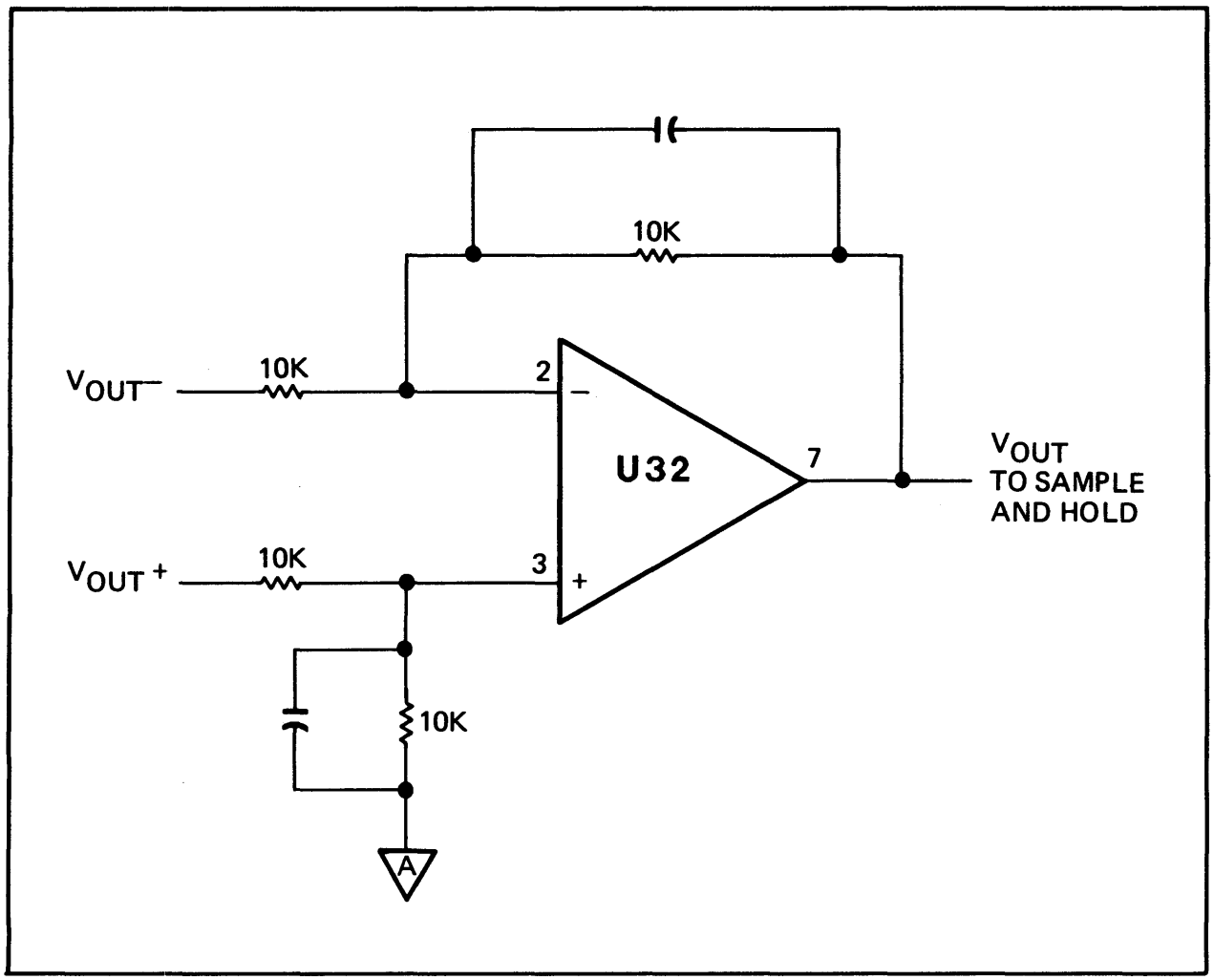


Figure 3-5. Differential-to-single-ended converter

Absolute Value Circuit

The absolute value circuit takes the voltage coming out of the S/H circuit and makes sure that it is positive when it goes to the analog-to-digital converter (ADC). This circuit also generates a polarity bit to indicate when a negative voltage has been converted to positive. This polarity bit shows up as the sign bit (bit 12) in the output data register. This circuit is made up of two op amps (U22 and U23), a handful of diodes (CR3, CR4, and CR6), a capacitor (C43), and 4 resistors (R7, R15, and two resistors in U24). The circuit is shown schematically in figure 3-6.

The output of the absolute value circuit is driven by the more positive of the two op amps. One of the op amps (U22) is a unity gain buffer, and the other (U23) is a unity gain inverter. Thus, one of the outputs will always be positive. Diodes CR3 and CR4 separate the negative and positive outputs, and cause the positive output to be sent to the ADC.

Resistors R7 and R15, and diode CR6 are used to generate a high logic signal if the analog input signal is negative. The pull-up resistor (R7) will pull the polarity signal high (+5 volts) whenever the output of the inverting op amp (U23) is greater than 0; this will be the case whenever the analog input to

that op amp is negative. Diode CR6 prevents the op amp output from driving the polarity signal any higher. When the analog input is positive, the inverting op amp will drive its output to the negative rail. When this happens, current will be drawn through diode CR6 and resistors R7 and R15; thus, the polarity signal will be pulled low. R15 and R7 will prevent the voltage of the polarity signal from going much below ground.

The 270 pf capacitor (C43) in the feedback loop of the inverting op amp is used as a low pass filter to reduce high frequency noise in the circuit.

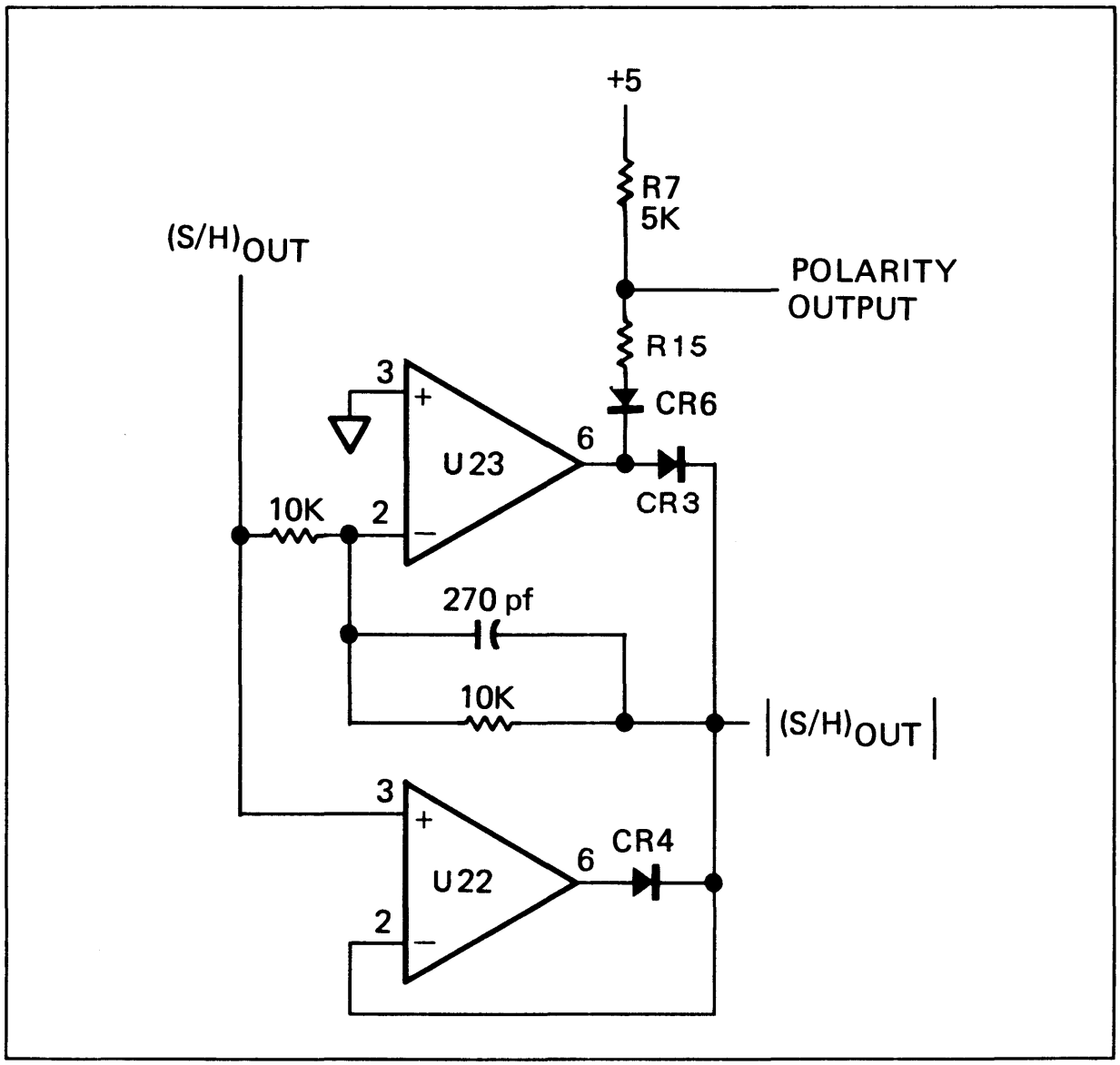


Figure 3-6. Absolute value circuit

Analog-to-Digital Converter (ADC)

The ADC (U65) receives its analog input from the absolute value circuit and converts it to a digital value. The converter will do a 12-bit analog-to-digital conversion in 7 microseconds; it is used in unipolar mode to digitize a voltage from 0 to +10 volts, with a straight binary coded output.

The data lines for the ADC are on pins 2 through 9. The output data bits are time multiplexed and require two reads from the chip to get the full 12 bits of data. Three of the data lines (pins 7, 8, and 9) are also used as input lines to program the mode in which the converter operates.

The ADC is controlled by four control lines. The first is CHIP SELECT. Since the A-to-D chip is always selected, this line (pin 14) is tied to ground. The other three control lines are BUWR- (NOT buffered write), BURD- (NOT buffered read), and BUC/D- (buffered control/NOT data.) Signals for these lines are generated by PROM U68 and buffered through filp-flop U67. (The signals generated by the PROM are discussed in more detail later.) The system clock, SYCLK, is brought into the converter on pin 13.

Four operations are carried out by the ADC chip:

Mode programming. During this operation, the A-to-D card programs the A-to-D chip for 12-bit unipolar output in straight binary coded form. To accomplish this programming, line BUWR- must be low, lines BUC/D- and BURD- must be high, and the first three data lines must be low. The control signals come from the PROM (U68) via the flip-flop (U67); the data signals come from BURD- through an inverting buffer (U86).

Conversion. The conversion of the analog voltage to digital form starts when lines BUC/D- and BUWR- go low. Once the conversion is started, it will run under control of the system clock until it is complete; this takes 12.5 clock cycles. Since the digital conversion circuitry of the A-to-D card runs on the same clock signals that the A-to-D chip uses, the digital circuitry simply waits an appropriate number of clock cycles before requesting the results of the the conversion from the chip.

First data read. The ADC chip doesn't have enough data lines to output all of the data bits at once, so two reads are needed to get the data out. The first read provides the 4 most significant bits of converted data. This read occurs when BUC/D- and BUWR- are high and BURD- is low.

Second data read. The second data read provides the 8 least significant bits of converted data. This happens when BUC/D- and BURD- are low and BUWR- is high.

Common Mode Overrange Detection

The common mode overrange detection circuit detects whether either of the op amps in the PGA is producing an output that is greater than +10 volts or less than -10 volts. The circuit uses 4 op amps with open collectors, contained in package U33.

The circuit works by comparing the outputs of the PGA op amps with the positive and negative voltage rails established in the input protection circuit. If one of the PGA op amps produces a voltage greater in magnitude than 10 volts, one of the op amps in U33 will detect it and turn on its open collector output, thus pulling the common mode overrange signal (OVD-) low. The state of the OVD- signal is provided in the O bit (bit 13) of the output data register.

DIGITAL CONVERSION CIRCUITRY

The analog-to-digital conversions made by the A-to-D card are controlled by a state machine and associated digital circuitry. The next several paragraphs describe that circuitry in considerable detail.

Generating Control Signals

The control signals that drive the Conversion state machine are generated by a PROM, U68. The PROM gets its addresses from counter U98, which is in turn driven by clock generator U100. The clock signal to the counter is gated through a NAND gate (U94); this allows the counter to be stopped when the output of flip-flop U93 is low. The state of U93 is determined by the output of AND-OR-INVERT gate U92. (The usefulness of this arrangement will become apparent presently.) When the counter is counting, the address sent to the PROM is incremented with every clock cycle. For each address, the PROM outputs the bit pattern that was programmed into it; these outputs are the control signals that drive the conversion circuitry. When the PROM reaches the end of its sequence of control signals, it outputs a control signal that resets the counter and causes the sequence to start over again. The timing diagram in figure 3-7 shows the sequence of control signals generated by the PROM.

Flip-flop U67 buffers the output of the PROM to remove any glitches that may appear on the output lines when the outputs change. The PROM outputs are clocked on positive transitions of the system clock; those signals are clocked into the flip-flop on the negative transition half a clock cycle later. Since the PROM outputs are unstable only on the positive clock edge, the control signals clocked into the flip-flop are always clean, and the outputs of the flip-flop are always free of glitches.

The A-to-D card makes use of both buffered and unbuffered control signals. To differentiate between them, the names of the buffered signals have "BU" added to the front of the unbuffered signal name. For instance, the latch signal is named LACH in its unbuffered form and BULACH in its buffered form. The buffered signals are used for most applications on the card, since most devices on the card use positive clock transitions; use of the negatively clocked buffered signals ensures that the signals will be waiting at the inputs when the positive clock transition occurs. There are, however, a few devices on the card that make use of negative clock transitions; unbuffered signals are supplied to the inputs of these devices.

Stopping the Counter

Each clock cycle takes 600 nanoseconds. Since there are 30 instructions in the control sequence, the minimum time for completion of the sequence is 18 microseconds. This minimum time is attained only in certain circumstances; there are some situations in which it is useful to stop the counter and extend the cycle time.

Stopping the counter is accomplished by the AND-OR-INVERT gate (U92) shown in figure 3-8. The output of this gate is driven through flip-flop U93 into NAND gate U94. When the output of U92 goes negative, the counter stops.

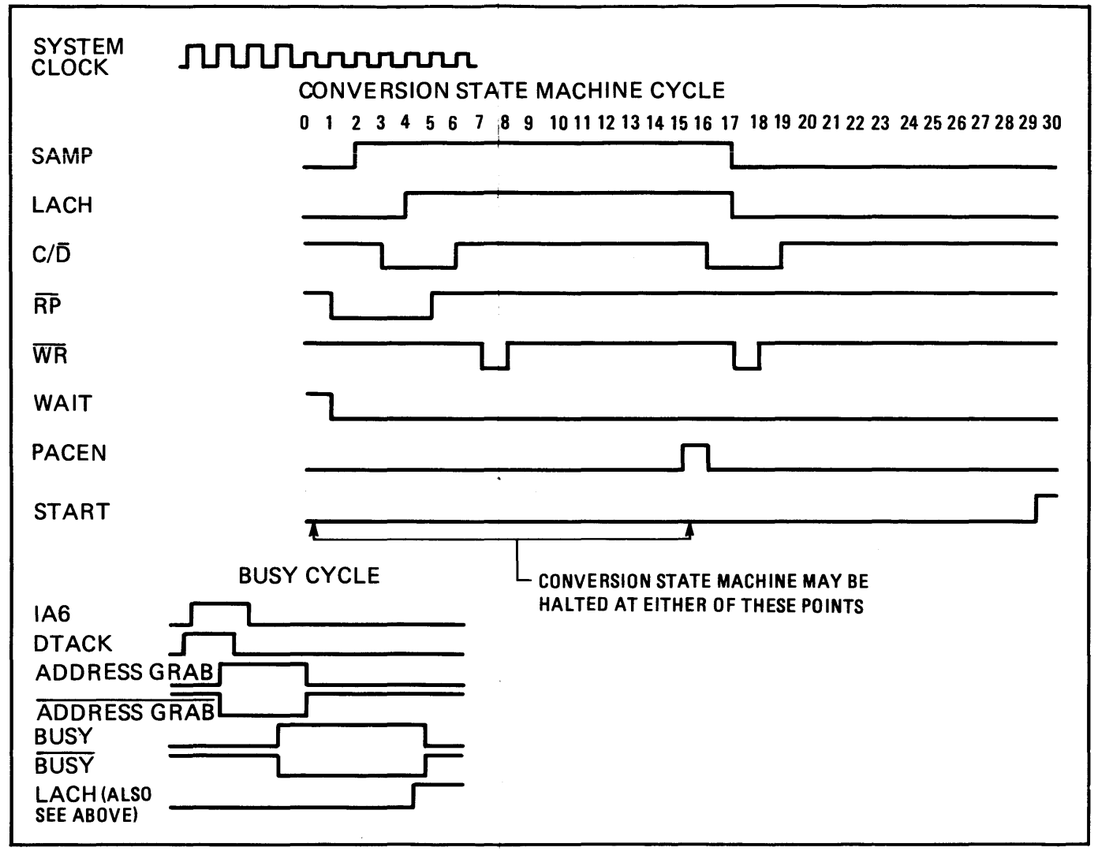


Figure 3-7. Control signal timing, PROM U68 and BUSY state machine.

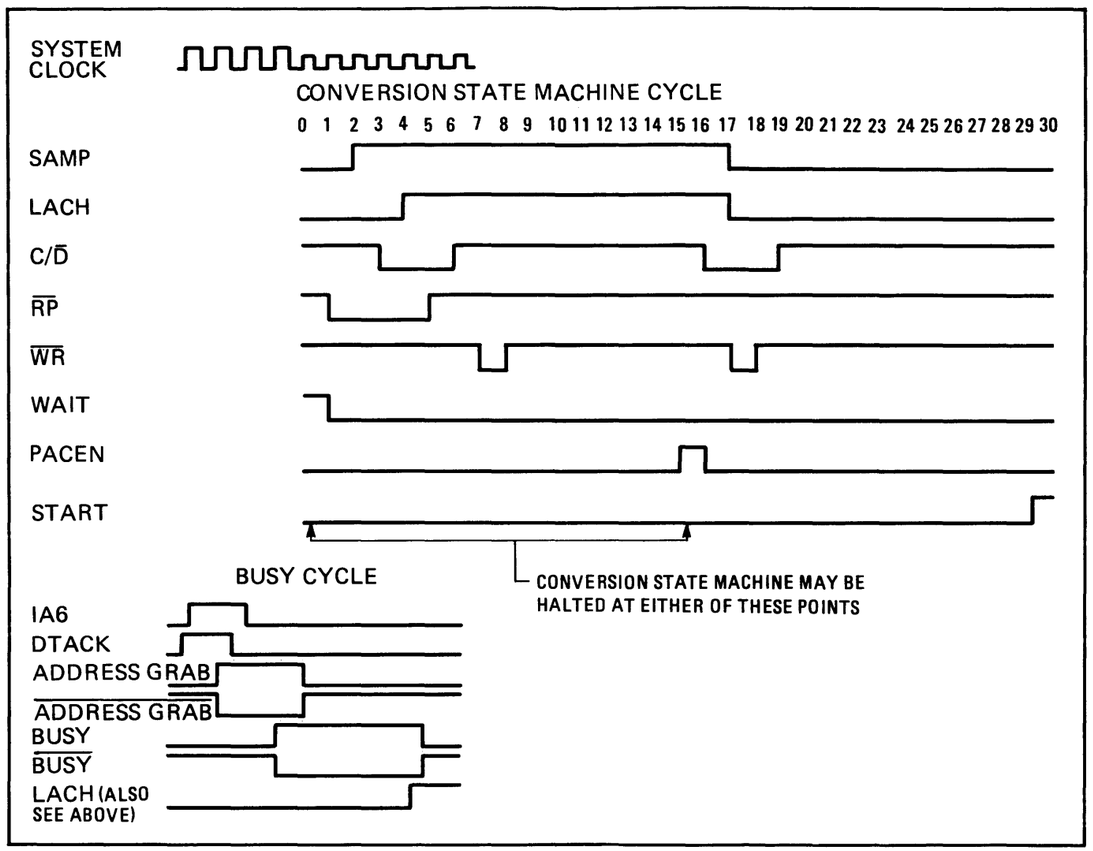


Figure 3-7. Control signal timing, PROM U68 and BUSY state machine.

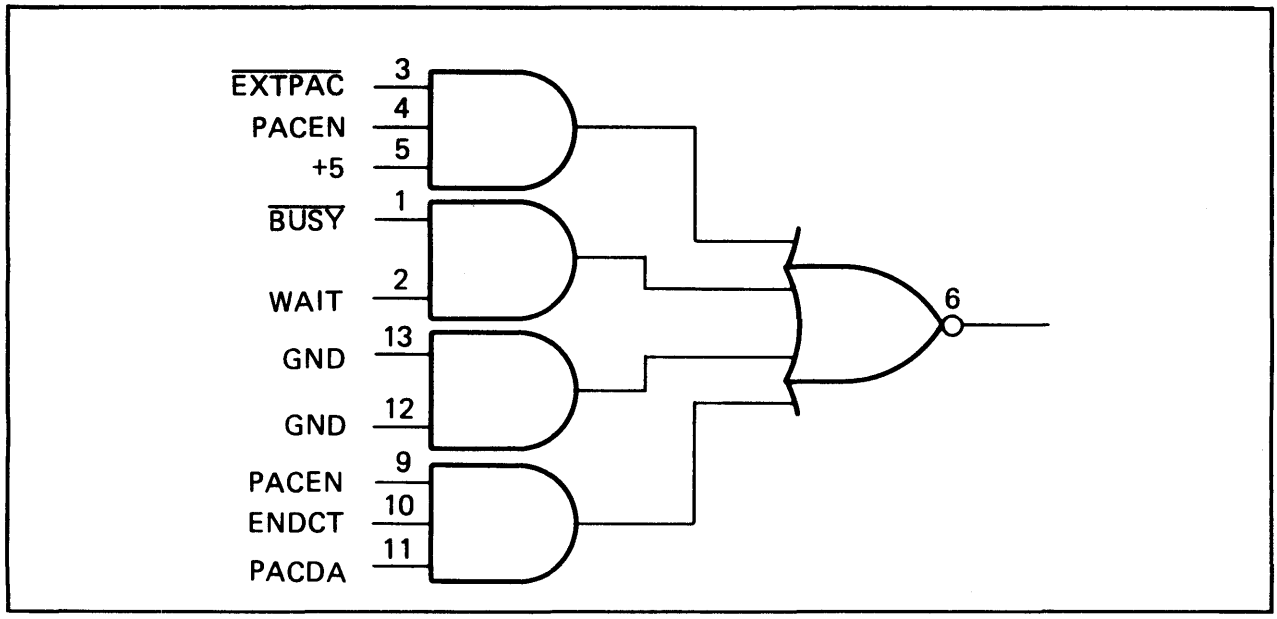


Figure 3-8. AND-OR-INVERT gate (U92)

There are two times during the conversion cycle that the counter can be stopped:

1) Clock cycle 0. The PROM sets the WAIT signal high at clock cycle 0. If BUSY- is also high, the output from U92 will go low and cause the counter to stop counting. This situation occurs when the card is waiting for an analog read. As soon as the CPU removes the card address from the backplane, BUSY- goes low on the next negative clock transition and U92 releases the counter, which starts counting again on the following positive clock transition.

2) Clock cycle 15. The PROM sets the PACEN signal high at clock cycle 15. This lets the counter be stopped by an external pacing circuit or by the pacing timer.

   a) An external pacing circuit will stop the counter if it holds the external pacing input of the card high. This holds EXTPAC low, and the inverted EXTPAC input into U92 stops the counter until the external pacing circuit lets the external pacing input go low again.

   b) The internal pacing timer uses the ENDCT signal to stop the counter. In this way, the pacing timer can stop the conversion cycle to let the programmed pace interval elapse between readings. The pacing timer holds ENDCT high until the timer counts up to FFFF(hex); at that point, ENDCT goes low and U92 releases the counter. (All this assumes that the PACDA (internal pace disable) line remains high; this must always be the case except in external pacing situations. Note that PACDA is controlled by you, not by the card, since it is derived from the internal pace disable input on terminal 30.)

Conversion Cycle Timing

In the next few paragraphs we will look at the conversion cycle and the way it is controlled by the signals coming from the PROM. You'll find figure 3-7 useful for following this discussion. We will refer to both buffered and unbuffered control signals; keep in mind that buffered signal transitions actually occur one half cycle after the corresponding unbuffered transitions.

Assume that we are starting at clock cycle 0 with BUSY low, waiting for an analog read. As described above, WAIT is high at clock cycle 0. With WAIT high and BUSY low (BUSY- high), the counter is stopped. When the analog read occurs, BUSY is set high, the counter is released, and the state machine moves into the conversion cycle. As the card leaves the wait state, BURD- is pulled low. On the next clock cycle, BUSAMP goes high. This accomplishes three things:

1) It puts the sample and hold circuit in the sample state.

2) It latches the overrange bit, the polarity bit, and the 4 most significant data bits (from the ADC) into data buffer U78.

3) It clocks the address from address buffer U50 into buffer U70.

On the next cycle BUC/D- goes low, enabling the ADC to release the 8 least significant data bits and loading the value from the pace timing register into the pace timer. LACH and BULACH go high on the following cycle; this sets BUSY low again and clocks those 8 data bits into data buffer U77.

In the next few cycles, BURD- goes high, causing the data lines at pins 9, 8, and 7 of the ADC to go low; BUC/D- goes high, enabling the pacing timer to start counting; and BUWR- goes low. On this last transition, the mode of the ADC is programmed. All of this activity takes us through clock cycle 7.

At clock cycle 15 the PACEN signal is raised. This allows the counter to be stopped by either the external pace input or the internal pacing timer. This stop condition will persist as long as the external pacing input is actuated, or until the internal pacing timer reaches full value. At that point the conversion cycle will continue. On the next cycle, BUC/D- will go low, followed by BUWR-, BULACH, and BUSAMP one cycle later. As a result, conversion begins on the voltage held by the sample and hold circuit; in addition, the polarity and overrange signals (POLAR- and OVD-) are clocked into the flip-flops in U96.

After allowing time for the conversion to complete, the START signal goes high. This resets the counter to 0, causing the PROM to start the conversion cycle over again.

The BUSY Cycle

As you might infer from the discussion of the conversion cycle, the BUSY signal plays a significant part in controlling the conversion. It is the signal that starts the conversion cycle, or causes it to stop in the wait state. The BUSY signal is controlled by its own state machine, which consists of two J-K flip-flops (U85) and a gaggle of gates (U84). Figure 3-7 shows a timing diagram of the BUSY cycle.

An analog read puts a valid address on the address bus, causing ININT to go high (after the card decodes its address via U39). The output of U46 is set on the next rising edge of the system clock, and this gates IA6 (the analog read "flag") through U85A. TACH- subsequently goes low, causing DTACK- to acknowledge the command from the backplane.

Assume that at this time BUSY- is high and the card is in the wait state; this combination (BUSY- and WAIT both high) will cause U92 to stop the counter. BUSY- will therefore gate the high output of U85A through U84A, causing ADDRESSGRAB to go high on the next falling edge of the system clock. When ADDRESSGRAB goes high, it clocks the address from the backplane into address buffer U50.

When the address is removed from the backplane and IA6 goes low, ADDRESSGRAB gates a high level through U84D, setting BUSY high and BUSY- low. This releases the counter, and the conversion cycle continues on the next rising edge of the system clock.

BUSY- sets ADDRESSGRAB low (and ADDRESSGRAB- high) on the next falling edge of the clock. ADDRESSGRAB- enables U85, and this situation is maintained until LACH goes high, which sets BUSY low. Thus, BUSY is high continuously from clock cycle 0 of the Conversion state machine to clock cycle 4.5; this allows the address to be clocked into the card and data to be moved to the output buffers without interruption.

The BUSY signal is available to the backplane as bit 15 of the data register; BUSY- is available as bit 6 of the status register. Whenever BUSY is low, the card can accept a new address from the backplane. The WAIT signal is available as bit 14 of the data register; if WAIT is high, it indicates that the interval before the next analog reading will be longer than the interval programmed into the pacing timer. (That's because the card is stopped and waiting for the next address.) Note that the BUSY and WAIT bits are not clocked to the output buffers (in contrast to the overrange, sign, and data bits); the current states of BUSY and WAIT are always available, regardless of what part of the cycle the state machine is in.

The Internal Pacing Timer

The internal pacing timer comprises four 4-bit counters, U36, U26, U47, and U48. These are set up in series such that they will count from a programmed start value up to FFFF(hex). The counters use the system clock as the time base, with each count taking 600 nanoseconds. When the BUC/D- signal goes low, it loads the pacing timer with the values contained in flip-flops U37 and U49. When BUC/D- goes high again, the pacing timer is enabled to count. It starts counting on the next positive transition of the system clock, and counts continuously until the BUC/D- goes low again to reload the timer.

The carry bit of the most significant counter (U47) drives the ENDCT signal. This signal is used to restart the Conversion state machine counter after the programmed pace interval has elapsed. ENDCT remains high while the pacing timer counts up toward FFFF. When the timer reaches FFFF, ENDCT is driven low.

A typical conversion cycle starts off with BUSY set high by an analog read. Shortly afterward BUSAMP goes high, and BUC/D- goes low on the following clock cycle. The BUC/D- transition presets the pacing timer with the values from flip-flops U37 and U49. On the next clock cycle BULACH goes high, setting BUSY low. Two cycles later, BUC/D- goes high, allowing the timer to count on positive clock cycles. Later in the conversion cycle PACEN will go high; since ENDCT stays high while the timer is counting up toward FFFF, PACEN and ENDCT will combine to cause U92 to stop the counter. (Yes, you must keep PACDA high, too. That's under your control. You keep PACDA high by keeping the internal pace disable input (IPACDA, terminal 30) low. IPACDA must always be low unless you are doing external pacing, as described below.) The counter will remain stopped until the timer reaches FFFF; that sets ENDCT low and releases the counter to continue the conversion cycle.

The value that you write to the pace timing register to obtain a given pace period is:

```
value = FFF6(hex) - round((period - 0.000018) / 0.0000006)
```

where the period is given in seconds and the *round* function rounds to the nearest integer. This formula compensates for the difference between when the timer starts counting (clock cycle 7) and when PACEN goes high (clock cycle 15). Remember that ENDCT goes low when the timer reaches FFFF, not when it rolls over to 0.

Note that you can squeeze in a few extra microseconds beyond the maximum pace period indicated by this formula if you specify a value between FFF7 and FFFF. For values in that range, the timer will

have passed FFFF and started counting over again by the time PACEN goes high. With both PACEN and ENDCT high, the counter will stop until the pacing timer counts all the way around again and ENDCT goes low a second time. (We doubt that you'll find much use for those additional counts; a few extra microseconds don't usually make much difference when you're pacing in the 39-millisecond range.)

External Pacing

You can use an external source to trigger the A-to-D card to take readings. This involves the use of the external pace control input (EPCON, on terminal 29 of the wire termination assembly schematic diagram) and the internal pace disable input (IPACDA, on terminal 30).

These inputs are shown at location D18 on the schematic diagram of the A-to-D card. They can be driven by voltages in the range of +2 to +50 volts. For each input, the signal comes in through a 10 kohm resistor to the base of a transistor (Q1 or Q2). The collector of the transistor is connected to a pull-up resistor and to the control gate that propagates the signal to its appropriate function on the card. When you apply a positive voltage to the input terminal, the transistor is turned on and the signal at the collector is pulled low.

The two input lines come into AND-OR-INVERT gate U92 (see figure 3-8) as control signals EXTPAC- and PACDA. (EXTPAC- is the inverted form of the EXTPAC signal shown on the schematic diagram.) These signals combine with the PACEN control signal to stop or start the Conversion state machine at the times that are appropriate for external pacing. If a voltage is applied at the external pace input, it sends EXTPAC- high. With EXTPAC- high, PACEN will stop the counter when it goes high at clock cycle 15 of the conversion cycle (see figure 3-7). Once stopped, the counter will not continue until the voltage at the external pace input is removed, causing EXTPAC- to go low.

With this mechanism, you can control the timing of readings by controlling the external pace control (EPCON) input. If you hold the EPCON input high and then have the CPU request an analog read, that read will return data with the Busy bit set. The Conversion state machine will be stuck at clock cycle 16 until you bring the EPCON input low. When EPCON goes low EXTPAC- will go low and the Conversion state machine will continue its cycle.

When you are doing external pacing, you should keep the PACDA control signal low. (Do this by applying a positive voltage to the IPACDA input, terminal 30.) This disables the internal pacing timer on the card and prevents the timer from stopping the state machine counter. This means that the EPCON input (terminal 29) is the only signal that controls the release of the counter. Refer to Section 4 of this manual for a discussion of the implications of this set-up. Whenever you are not using external pacing, you must keep PACDA high (IPACDA low).

DIGITAL BACKPLANE CIRCUITRY

The following paragraphs describe the circuits that interface with the CPU via the backplane.

Select Code

The select code circuit does two things for the card: first, it determines what the select code of the

card is; second, it compares the upper 8 bits of an address with the select code to determine whether the card is being addressed. This function is implemented with an 8-bit comparator (U39), 5 of the 7 switches on DIP switch SW1, and 5 of the 7 resistors in resistor pack R10.

One side of each resistor in the SIP is tied high to form a pull-up resistor. The other side of each resistor is tied to a switch that can be closed to ground. This connection also provides the signal to drive other devices.

Comparator U39 compares address lines A16 through A23 from the backplane with the select code switches (pins 9, 7, 5, 3, and 12) and the hard-wired bits (pins 14, 16, and 18). If the two sets of signals match, and if backplane address strobe BAS- coming in to pin 1 is low, the comparator will drive IIMA- (pin 19) low. This tells the card that it is addressed, and also enables the DTACK- and IMA- drivers to drive the backplane.

The Backplane Handshake

When the IIMA- signal goes low, the backplane data strobes (BUDS- and BLDS-) are enabled to drive ININT high. The logic for this operation is shown at location B27 on the schematic diagram, using two OR gates and a NAND gate. When ININT goes high, flip-flop U46B will drive its Q output high on the next rising edge of the system clock (SYCLK). One clock cycle later, that Q output will drive flip-flop U46A high and its Q- output will go low. This low output is designated the TACH- signal, and it drives the DTACK- signal on the backplane low.

When the CPU removes the card address from the backplane, the ININT signal goes low. This clears both flip-flops in U46 and leaves the circuit ready for another I/O operation.

Addressing

The several different operations that can be done on the A-to-D card are decoded with the circuitry at locations B to C6, 7, and 8 on the schematic diagram. Only the first 6 address lines, A1 through A6, are required to address the card. Because the backplane is capable of driving only one TTL load for each input signal, most of the lower address lines go through some sort of buffer gate before they reach a decoder or register.

Address bit 6 is used to designate an analog read (or write).

NOTE

Analog writes are emphatically NOT recommended because, if the the busy bit is low, the address data is retained but the data from two readings ago will have no where to go. It will be overwritten.

If address bit 6 is high and IIMA is high, signal IA6 is set high. This signal is used to disable the 3-bit decoder at U69, to tell the BUSY state machine that an analog read is taking place, and to enable analog data buffers U77 and U78 to drive the internal data bus.

Address bits 4 and 5 specify the gain used in an analog read. These address bits are first clocked into address buffer U50, and then into buffer U70. From there they drive the analog mux that selects the gain of the programmable gain amplifier.

The use of address bits 1, 2, and 3 depends on whether an analog read is taking place. In the case of an analog read (IA6 high), these bits are clocked from address buffer U50 into buffer U70; from there they generate the signals that determine which channel is used to take an analog reading. If it is not an analog read (IA6 low), these three bits enter decoder U69 and cause one of its output signals to go low. The decoder outputs combine with other signals to perform various card functions.

Resets

A reset occurs on the A-to-D card when the CPU drives the RESET- signal on the backplane low (hard reset) or when you write to address 1 on the card (soft reset).

In the case of a hard reset, the RESET- signal from the backplane is buffered by an OR gate in U97. Coming out of U97 as signal CLR1-, it takes two paths. The first sets the interrupt enable flip-flop (U93B) low; the second goes through NAND gate U94B and emerges as RESET. RESET makes its way to counter U98 via OR gate U95B, and resets the Conversion state machine to cycle 0, leaving it in the WAIT state.

A soft reset occurs when address 1 (the ID register) is written to. This is a normal write, and the write signal (BR/W-) comes on to the card and is buffered by AND gate U85B. The output of this gate is ORed with TACH- (U97C), and the result is ORed with ID- (U95C). Coming out of U95C as signal CLR2-, this result takes two paths. In the first, it goes through NAND gate U94B and, emerging as RESET, it travels through OR gate U95B and arrives at counter U98, resetting the Conversion state machine to cycle 0 (the WAIT state). In the second path, CLR2- clears the BUSY and ADDRESSGRAB flip-flops (U83). The soft reset does not affect the interrupt control.

Backplane Data Bus

Two bi-directional buffers, U38 and U29, drive the backplane data bus. Backplane signal BR/W- controls the direction of the data flow. The data buffers are enabled by BUDS-, BLDS-, and IIMA-. IIMA- must be valid for any data transfer to take place, and BUDS- and BLDS- control whether an odd byte, even byte, or full word is transferred. The logic that implements this function is shown at location B7 of the schematic diagram.

Reading From the Card

The gates that handle reading from the card are shown at location B4 on the schematic diagram. The READ signal, derived from BR/W-, is brought into these gates and one of three signals, ANEN-, IDEN-, or STATEN-, is driven low. Which signal is selected depends on the address at the time. These three signals control which of the three data buffers drives the internal data bus.

When the A-to-D card receives a read command, it drives the requested data onto the internal data bus immediately. If the address selection drives ANEN- low, data buffers U77 and U78 drive the data bus with results from the ADC. If IDEN- is driven low, the hard-wired ID code is driven onto the data bus from U27. If STATEN- goes low, it drives the status bits from U28 onto the data bus.

Writing to the Card

Writes to the A-to-D card use the same decoding method as do reads from the card. The primary difference in approach is that during a read the card releases the data to the backplane immediately, whereas during a write the incoming data must be clocked into flip-flops. For all writes the TACH- signal is used to clock the data in.

There are three locations that you can legitimately write to: the ID register (for a soft reset), the status register (to enable interrupts) and the pace timing register (to set the pace interval). We've already covered the ID register in the discussion of resets, above.

There is only one bit that you can write to in the status register. That is bit 7, the interrupt enable bit. The output from U97B (valid write) and the decoded status register address (from U69) combine in U81C to produce the STSTAT signal. This clocks bit 7 from the internal address bus into the interrupt enable flip-flop, U93B. The Q output of this flip-flop is wrapped around into bit 7 of the status register, so that the interrupt enable status is available on a status read.

Writing to the pace timing register is accomplished with the help of the TIME- signal (decoded from the address by U69) and the "valid write" signal that comes from U97B. These two combine in U81B to produce the signal that clocks the pace timer value from the internal data bus into flip-flops U37 and U49.

Interrupts

The interrupt level of the card is set by two resistors from SIP resistor pack R10 and two switches from DIP switch pack SW1, in the same way that the value of the select code is set. The two interrupt level lines, INT1 and INT2, drive bits 4 and 5 of the status register (U28) so that the interrupt level is available on a status read. INT1 and INT2 also drive the inputs of decoder U79. When interrupts are enabled by writing to bit 7 of the status register (as discussed above), the interrupt enable flip-flop (U93B) activates one of the two enable pins of U79. When the BUSY signal goes low, activating the other enable pin of U79, the appropriate backplane interrupt line (IR3, IR4, IR5, or IR6) goes high, generating an interrupt to the CPU.

SEQUENCE OF OPERATIONS

What follows is a summary of the operation of the A-to-D card. It is based on the timing diagram for the conversion cycle, but also includes events from the BUSY cycle. You will probably want to refer to the timing diagram in Figure 3-7 as you go through the sequence.

In the listing below, the numbers in front of each sequence of events indicate the conversion cycle clock time. Note that the conversion cycle will repeat without stopping only if:

1) the CPU always supplies a new register address (via an analog read) before the Conversion state machine enters the wait state, and

2) external pacing is not in effect, and

3) the value in the pace timing register is set for the minimum pacing interval (or, alternatively, the internal pace timer is disabled completely).

If these conditions are not maintained, the Conversion state machine's counter will stop the conversion cycle; the cycle will remain stopped until the condition that caused it to stop is reversed. (There's nothing wrong with stopping the conversion counter; in many situations it's positively the right thing to do. It's just that the timing diagrams look like they keep going continuously and don't stop for anything.)

In this listing we will mention only "significant" events in the clock cycle. That is, we will not bother reporting when a signal changes state solely to get back to where it started from.

Remember that the buffered control signals change state one half clock cycle after their unbuffered counterparts.

0.0 Start of cycle. WAIT goes high.

If BUSY- is low, the conversion cycle goes on without interruption. If BUSY- is high, the conversion counter stops until it goes low again. (In essence, BUSY- high means that the card is waiting for an analog read to take place. Once the analog read starts, it will take from 3 to 4 clock cycles before BUSY- goes low again and the conversion counter starts counting again. During that time the backplane reads the data, and the new address is clocked into the address buffer. Two clock cycles later, BUSY- goes low, the conversion counter is released, and the cycle continues.)

(Note that you can keep the cycle from stopping by making sure that the analog read takes place in time for the card to be busy (BUSY- low) when the WAIT signal goes high. The surest way to do this is to start your next analog read as soon as BUSY- goes high again. You can determine when that happens by checking bit 6 of the status register, or by repeatedly checking bit 15 of the returned analog data word.)

1.0 WAIT goes low.

1.5 BURD- goes low. This enables the transfer of the 4 most significant bits from the ADC.

2.5 BUSAMP goes high. This has three effects:

The sample and hold circuit starts sampling.

The polarity bit, the overrange bit, and the 4 most significant data bits are clocked into the internal data buffer and onto the internal data bus.

The address is clocked from the address buffer into buffer U70; this drives the channel and gain multiplexers.

3.5 BUC/D- goes low. This has two results:

It enables transfer of the 8 least significant data bits from the ADC.

It loads the value from the pace timing register into the timer.

4.0 LACH goes high.

4.5 As a result, BUSY- goes high.

BULACH goes high. This clocks the 8 least significant data bits into the internal data buffer and onto the internal data bus.

5.5 BURD- goes high.

6.5 BUC/D- goes high. This enables the pace timer to start counting.

7.0 The pace timer starts counting. It continues counting up on every positive transition of the clock.

7.5 BUWR- goes low. This programs the mode of operation of the ADC.

15.0 PACEN goes high. This allows the counter to be stopped by either the external pace input or the internal pace timer.

If the external pace control input (EPCON) stops the counter, the counter remains stopped until that input is released and EXTPAC- goes low. If the internal pace timer stops the counter, the counter remains stopped until the timer reaches FFFF and pulses ENDCT low. On either occurrence, the counter starts again and the conversion cycle continues.

16.5 BUC/D- goes low.

17.0 LACH- goes high. This sets up the BUSY state machine to go through its cycle when the card receives the next analog read.

17.5 BUSAMP goes low. This puts the sample and hold circuit into the hold mode.

BULACH goes low. This clocks the polarity and overrange bits into their various flip-flops and and onto the internal data bus.

BUWR- goes low. This starts the A-to-D conversion on the voltage held by the sample and hold circuit.

29.5 BUSTART goes high.

30.0 As a result, the counter resets to 0. This puts WAIT high and starts the conversion cycle over again.

THE ANALOG PIPELINE

The analog pipeline is implicit in the foregoing theory of operation; now we will make it explicit. If you follow the sequence of operations of the A-to-D card closely, you will see that the result you get back when you make an analog read does not come from the address that you specified in the read; it comes from the address that you specified two readings earlier. This is because the operations on the card are not all serial; several operations run in parallel. This gives the effect of a pipeline: You push addresses in at one end of the pipeline and results come out two readings later.

At any given time, the analog pipeline is working on three different analog readings. The following table shows the events that occur in an analog read cycle and which reading those events pertain to, assuming that you have just made the nth analog read.

EVENT	READING NUMBER
Address supplied from backplane	n
Address latched onto card	n
Address used to decode channel and gain	n-1
Voltage sampled at specified gain	n-1
Voltage converted to digital form	n-1
Digital value read onto backplane	n-2

Why does the A-to-D card use a pipeline? Not, as you would expect, to make successive readings happen faster. It turns out that single, non-pipelined readings could be made every 18 microseconds, the same rate as for pipelined readings. The problem with non-pipelined readings is that they would tie up the backplane for the full 18 microseconds, and the backplane simply doesn't allow that; two microseconds is about all that is available at a time. By breaking the analog read process down into a three-stage pipeline, the card can always be able to release a reading and take in a new address in that 2-microsecond window.

Once you understand that the pipeline exists, the effect it has on the way you take readings is fairly straightforward. For any series of readings, take two more than you need, and throw away the data returned by the first two.

PROGRAMMING AND EXTERNAL PACING

SECTION IV

In this section we will discuss how to program the A-to-D card to make voltage measurements. We will also discuss how to take externally paced readings.

Before you start writing assembly language programs for the A-to-D card, take a careful look at your application. You may be able to save time and effort by writing your programs in BASIC or Pascal and calling the subroutines from the HP 98645A Measurement Library to access the A-to-D card. The Measurement Library subroutines are able to take readings at the full speed of the A-to-D card. (The Measurement Library attains this speed by using the same sort of assembly language routines that we will discuss in this section.) You might find assembly language useful if your application demands high computational speed: an assembly language program could do the set-up for readings faster than the Measurement Library, and it could do data reduction after the readings faster than either BASIC or Pascal.

If you've determined that assembly language is the right language for your application, read on. We assume that you have a solid working knowledge of MC68000 assembly language and the Pascal operating system. (Refer to the Pascal 2.0 System Designer's Guide, part number 09826-90074, for more information.) We also assume that you have absorbed the information in Section 3 of this manual, particularly the paragraphs on registers and the analog pipeline.

PROGRAMMING CONSIDERATIONS

Channel and Gain

To take a reading from the A-to-D card you must supply channel and gain information, and you may supply pace information. The register number that you specify in your read request tells the card which channel and gain to use for the reading. This must be a 16-bit (word-wide) read. The following table shows which register to read for a given channel and gain.

Channel	Address for Gain of 1	Address for Gain of 8	Address for Gain of 64	Address for Gain of 512
0	64	80	96	112
1	66	82	98	114
2	68	84	100	116
3	70	86	102	118
4	72	88	104	120
5	74	90	106	122
6	76	92	108	124
7	78	94	110	126

For example, to take a reading from channel 3 at a gain of 8, you would read from register 86 of the A-to-D card.

The A-to-D card receives the register address on address lines A1 through A6 of the backplane. It decodes these lines as follows:

A1 through A3 specify which channel to read.

A4 and A5 specify what gain to use for the reading:

A5	A4	Gain
0	0	1
0	1	8
1	0	64
1	1	512

A6 indicates whether it is an analog read. If A6 is set to 1, it is an analog read; if it is set to 0, it is an ordinary access to the ID, status, or pace timing register.

A0 is ignored. Odd-numbered register addresses are used for accessing low bytes; since only full words are read by analog reads, odd-numbered addresses are not used. (There is no A0 line on the backplane; its function is handled by BUDS- and BLDS- which are, as the minus signs indicate, negative true.)

For example, if your read request specified a register address of 86, the A-to-D card would break down that address as follows:

A6	A5 A4	A3 A2 A1	A0
1	0 1	0 1 1	0
analog read	gain = 8	channel = 3	not used

The value returned by an analog read is the voltage for the channel and gain specified <u>two analog reads previously</u>. Thus, you must take n+2 readings to get the n values that you desire. For instance, the example program below takes 3 readings to get 1 valid voltage value. (Refer to the paragraphs on the "Analog Pipeline" at the end of Section 3 for a fuller explanation of this phenomenon.) The format for the returned value is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B	W	O	S	D	D	D	D	D	D	D	D	D	D	D	D
				MSB											LSB

where:

B = busy
W = wait
O = common mode overrange (0 = overrange; 1 = no overrange)
S = sign (0 = positive; 1 = negative)
D = data

(Refer to Section 3 for a more detailed explanation of the data word.)

Dealing with Data

NOTE

Any reading that returns a 1 as the busy bit is invalid; the address provided in such a reading is not latched into the address buffers on the A-to-D card. You can ensure valid readings by checking the busy bit (bit 15 of the data word) or the not busy bit (bit 6 of the status word) and making your analog read only when the card is not busy.

The value returned in the data word is a raw reading produced by the ADC chip and the absolute value circuit on the A-to-D card. The data word's 13 least significant bits (sign and magnitude) are not adjusted for gain or input offset voltage. The data in the 13 bits is in signed binary form; the most significant of the 13 bits reperesents the sign (polarity) of the voltage the A-to-D card measured, while the remaining 12 least significant bits (lsbs) are a magnitude, not a directly readable voltage. We call these 13 bits the raw reading.

To change a raw reading into a voltage you could multiply the number the 12 lsbs represent by the least significant bit value for the gain you used. Polarity is determined from the sign bit. That will work, but the accuracy of the voltage obtained may not be suitable for your needs. You must decide, based on experiments, if an uncorrected voltage reading is accurate enough for your needs.

One of the major factors affecting accuracy is noise. Later in this section we will devote several paragraphs to dealing with noise. Another major factor affecting accuracy is input offset voltages. We will deal with input offset voltages here.

CALIBRATION

Most of the A-to-D card's input offset voltage is caused by operational amplifiers (op amps) on the card. You can correct for most of these offsets by "calibrating" the card.

In order to calibrate the A-to-D card you will need to use one channel as a reference channel. Any channel can serve as your reference; just short the channel's two inputs together and tie them to ground.

Below we explain two algorithms you might use to calibrate the card. However, you can save considerable development time if you use the calibration subroutine contained in the HP 98645A Measurement Library.

Calibrating the A-to-D card requires measuring the input offset voltage. Simply reading the reference channel provides a gross offset value which may be acceptable in many applications. Tables 4-1 and 4-2, and the explanation of the quick calibration scheme may help you design your own quick calibration subroutine. If you need to write a subroutine offering greater accuracy, see the requirements for a detailed calibration. In either case, also see the discussion under the heading "Noise" in this section.

In our explanations of calibration we use names for variables, such as Named_Variable. Since these variable names are to clarify procedures, no attempt was made to limit a name's length.

Detailed Calibration

A detailed calibration compensates for the offset introduced by the programmable gain amplifier (PGA) and an offset effect caused by the ADC IC. The sign (polarity) of the PGA offset can be detected, but the ADC's cannot. Only the magnitude of the ADC's offset can be detected (see the theory of operation for an expalanation of the polarity bit's origin).

To make the calibration you will need to:

1. Measure the offset caused by the ADC.
2. Measure the offset due to the PGA.
3. Apply the offsets to a reading from an input channel.

Conditions

The procedure is described below, but the sequence shown is not the only one possible. The procedure assumes you have converted the signed magnitude to a real number. While you may perform bit manipulations on the 13 bits of the raw reading, remember it is in signed binary (not two's compliment) form and that zero may have positive or negative sign (polarity).

The polarity of zero is caused by offsets which are too small to measure but not too small to detect. For the mathematical operations described in the calibration procedures, normalize zero by removing the sign.

NOTE

Most high level languages do not permit signed zero (±0) in a numeric variable. You will have decide how to store it.

1. ADC offset

A. Read the reference channel with the gain set to 1. With the gain set to 1 you will minimize the affects of most offset sources except the ADC chip.

B. Ignore the sign bit; this offset is always positive. This value is ADC_Offset. The polarity bit you detected when you took the reading was caused by whatever offset existed at the PGA.

2. PGA offset

A. Read the reference channel with the gain set to 512. This reading will detect the combination of the PGA_Offset_X_512 (PGA offset multiplied by 512) and the ADC_Offset.

B. Subtract ADC_Offset from the absolute value of the reading. The difference is the |PGA_Offset_X_512|.

C. The correct sign for PGA__Offset__X__512 is the same as that you read in step 2A above. Correct the sign of PGA__Offset __X__512, if necessary.

D. Divide the PGA__Offset__X__512 by 512 to get the PGA__Offset.

3. Application of offsets

A. Read the input channel you are interested in. Save the Uncalibrated __Input__Reading and the gain (G).

B. Subtract ADC__Offset from |Uncalibrated__Input__Reading| (absolute value of Uncalibrated__Input__Reading). The difference is the |Partly __Corrected__Reading|.

C. The sign of the Partly__Corrected__Reading must be the same as the Uncalibrated__Input__Reading. Correct it, if necessary.

Now, to use the PGA__Offset to change Partly__Corrected__Reading to Calibrated__Reading we need gain (G).

D. Multiply G by PGA__Offset and then truncate the product to an integer. This corrected product is the Derived__PGA__Correction.

E. Subtract Derived__PGA__Correction from Partly __Corrected__Reading. The difference is Calibrated__Reading. Since this was a subtraction of signed numbers (not absolute values) the sign (polarity) will be correct.

NOTE

Calibrated__Reading may be less than, equal to, or greater than Uncalibrated__Input__Reading.

With the corrections done, we can convert Calibrated__Reading to a voltage. Multiply Calibrated__Reading by the lsb value for the gain used for the reading. The product is in volts with the sign indicating the polarity.

Quick Calibration

Read the paragraphs and note under the heading "Conditions" in the explanation of a detailed calibration. That information applies to this discussion also.

To make a quick calibration you will need to:

1. Measure the gross offset.

2. Apply the offset to a reading from an input channel

An outline of the procedure follows. The sequence shown is not the only one possible.

1. Measure offset

Read the reference channel at the same gain you will use to read the input channel. This reading is the Crude_Offset.

2. Apply offset

A. Read the input channel you are interested in. This is Uncalibrated _Input_Reading.

B. Subtract the Crude_Offset from Uncalibrated_Input_Reading. The difference is Roughly _Corrected_Reading.

Since Crude_Offset and Uncalibrated_Input_Reading are real numbers, Roughly_Corrected _Reading may be less than, equal to, or greater than Uncalibrated _Input_Reading.

Table 4-1. Comparison of offset ranges

	OFFSET RANGE			
GAIN	1	8	64	512
	(PERCENT OF FULL SCALE)			
UNCALIBRATED*	±0.32	±0.39	±0.96	±5.6
QUICK CALIBRATION (WORST CASE)**	±0.60	±0.60	±0.60	±0.60
DETAILED CALIBRATION (WORST CASE)	±0.10	±0.10	±0.12	±0.15
MEASUREMENT LIBRARY CALIBRATION (WORST CASE)***	±0.07	±0.07	±0.10	±0.12

*This is not a specification. It is a theoretical worst case.
**The offset's range and symmetry is polarity dependent. See table 4-2.
***See Table 1-1 where these values are expressed as voltages.

Table 4-2. Judging polarity effects.

EFFECTS OF POLARITY ON OFFSET RANGE (apply to Quick Calibration)		
IF INPUT POLARITY IS:	AND REFERENCE POLARITY IS:	OFFSET CORRECTED TO WITHIN n PERCENT OF FULL SCALE:
+	+	±0.15
+	-	-0.15 to +0.60
-	+	-0.60 to +0.15
-	-	±0.15

If you chose to ignore the polarity of the offset and the input, you must regard the offset as corrected to within ±0.60% of full scale. If you take into account polarity, you will be able to judge the correction of the offset more closely. See tables 4-1 and 4-2.

To convert to a voltage, multiply Roughly_Corrected_Reading by the lsb value for the gain used to read the input channel. The sign indicates the polarity of the voltage.

OVERRANGES

Normal mode

If all 12 data bits (bit 0 to bit 11) are set to 1, a normal mode overrange has occurred. You may be able to avoid this problem by taking subsequent readings at a lower gain.

Common mode

If the overrange bit (bit 13) is set to 0, a common mode overrange has occurred. Lowering the gain may also solve this problem.

SIMPLE SAMPLE

The following example shows a subroutine for taking a single analog reading. It is an assembly language routine callable from Pascal in the HP 9000 Series 200 Pascal language system environment.

```
        mname ADCFASTREAD

*
*  Assembly language routine to read one channel from the ADC
*  card at the specified gain and return the raw data value.
*

        src MODULE ADCFASTREAD;
        src
        src EXPORT
        src
        src TYPE  sc = 7..31;
        src       chan_num = 0..7;
        src       gain_index = 0..3; { Maps to 1,8,64,512 gains }
        src       raw_data = -32768..32767;
        src
        src PROCEDURE read_adc(select_code: sc;
        src                    chan: chan_num;
        src                    gain: gain_index;
        src                    VAR value: raw_data);
        src
        src
        src END;

        def adcfastread_adcfastread
        def adcfastread_read_adc

*
* module initialization routine
*

adcfastread_adcfastread rts

*
* If called from Pascal with normal checking enabled, no range checking
* required on parameters.
*
*   Stack Frame At Entry:
*
*     16(a6)  select_code
*     14(a6)  chan
*     12(a6)  gain
*      8(a6)  pointer to value
*      4(a6)  return address
*       (a6)  stack frame <-- SP
*
* register utilization:
*
*   A0    register address
*   D0    misc. temporary storage, pipeline counter
*   D1    physical register displacement, value temporary storage
*   D2    base address (select code * 10000H + 600000H)
*
```

```
adcfastread_read_adc equ *

        link    a6,#0           no local storage
        clr.l   d2
        move.w  16(a6),d2       get select code
        moveq   #16,d0          generate a 16 for shift
        asl.l   d0,d2           shift selectcode into place
        ori.l   #$600000,d2     set the external address bits

        clr.w   d1
        move.b  12(a6),d1       get gain
        asl.b   #3,d1           multiply by 8 possible channels
        move.b  14(a6),d0       get the channel number
        add.b   d0,d1           add in channel number
        asl.b   #1,d1           multiply by 2 for word alignment
        add.b   #64,d1          add in reading register offset

        movea.l d2,a0           get the base address
        adda.w  d1,a0           add in the register offset

        move.w  #2,d0           get 3 - 1 counter to clear pipeline

loop    equ     *

wait    move.w  (a0),d1         read the card
        bmi     wait            repeat until busy bit (15) is clear

        dbra    d0,loop         do this 3 times to clear the pipeline

        movea.l 8(a6),a0        get the address of value
        move.w  d1,(a0)         stuff the value

endit   unlk    a6              return to main program
        movea.l (sp)+,a0        get the return address
        adda.w  #10,sp          clear the stack
        jmp     (a0)            return
*
        end
```

This routine ignores all readings taken when the busy bit is high. (See the instruction labeled "wait" and the one after it.) The routine takes three readings in order to push one valid reading through the pipeline. (See the loop that starts at "loop" and continues for the next three instructions.)

Pace Interval

You can specify a pace interval by writing a 16-bit value to the pacing register (register address 4). The value that you write into this register should be

FFF6(hex) - *round*((period - 0.000018) / 0.0000006)

where period was in seconds and the *round* function rounds to the nearest least significant bit (lsb). If you are taking a series of readings and want to specify a pace interval before each reading, the timing of the write to the pace register is critical; it should come as soon as the busy bit goes low, and the analog read request should follow it immediately. This will allow you to maintain accurate pacing, and it will execute fast enough to keep up with the free run speed of the A-to-D card. Note that at high speeds there will not be enough time to calculate pace values or register addresses; you should precompute these values and store them in arrays for fast access.

For more information on the workings of internal pacing, refer to Section 3 of this manual.

Noise

You can minimize the effects of noise by averaging several readings from the same channel. Averaging is a crude filter of both random and periodic voltage fluctuations.

NOTE

The design of the A-to-D card permits a first order rolloff (6 db per octave) to begin when the signal on an input exceeds 55khz.

At low sample rates an error may occur if the sample rate is equal to, or nearly equal to, a periodic noise on an input. Under this condition, you may be measuring an alias of the periodic signal with the voltage you intended to measure superimposed on it. You may be able to detect this by comparing readings taken from the same channel at high and low sample rates over equal amounts of time. If your high speed samples found voltages that are higher or lower than you found with your low speed samples, you may have a problem with an alias. Increase the number of samples of the channel.

The paragraphs above are not a complete discussion of measurement techniques. They are intended to start you in the right direction in the design of your program.

EXTERNAL PACING

You might use external pacing for ADC readings if:

-- you want to use a pace interval longer than that allowed by the pacing timer (0.0393390 second)

-- you want the readings to be controlled by an external event, rather than by time

External pacing is primarily a hardware operation. It is largely controlled by two hardware control lines on the wire termination assembly, IPACDA (internal pace disable, terminal 29) and EPCON (external pace control, terminal 30). There's not a lot of software involvement, other than making the read requests that you would normally make for an internally paced read. The timing of the execution of those read requests is controlled by the hardware. (There's no way to control IPACDA and EPCON directly from software; you'll have to build your own circuits to control them.)

In the next several paragraphs we will look at some of the features of the hardware that affect external pacing, and then we will see how they work in external pacing applications. You may want to refer to Section 3 of this manual for more information on the internal workings of the hardware.

Control Lines

There are two control lines of interest for external pacing:

IPACDA determines whether the readings are paced by the internal pacing timer on the A-to-D card. If IPACDA is low, the internal pacing timer of the card is used; if IPACDA is high, the internal pacing timer is bypassed and readings are taken at the free run speed of the card (one reading every 18 microseconds). Note that IPACDA must be high when readings start in order for the timing of the first reading of a series to be accurately known. (IPACDA can be set low after the start of readings if you want the readings to be paced by the internal pacing timer.)

EPCON controls whether or not any readings are taken. If EPCON is low, readings are taken whenever they are requested. If EPCON is high, requested readings are held off; a read request will not complete until EPCON goes low again.

In summary, when EPCON is low (open), readings are taken at the free run speed of the card (if IPACDA is high) or at the time programmed into the internal pacing timer (if IPACDA is low [open]). When EPCON is high, readings stop.

Applications

External pacing applications divide into two general types: single externally-paced readings and bursts of externally-triggered internally-paced readings.

Single readings. The idea behind taking single externally-paced readings is that you keep EPCON high until you want to take a reading, set it low only long enough to take the reading, and then set it high again. The steps in taking a single reading are:

1) Set IPACDA high. IPACDA will remain high for the duration of externally paced readings.

2) Set EPCON high. This holds off all readings.

3) Issue an analog read request to the A-to-D card via a procedure similar to that use the program sample above.

4) When it is time to take a reading, set EPCON low. Keep it low for 1 to 15 microseconds, then set it high again. This will allow one (and only one) reading to be taken.

5) If your routine takes multiple readings, repeat step 4 until you have taken all of the readings. (Remember to take 2 extra readings to push your results through the pipeline.)

Bursts of Readings. The idea behind taking readings in bursts is that you request multiple readings with an assembly language routine, and then take those readings in one burst by setting EPCON low until all of the readings have been taken. These readings can be taken at the free run speed of the card, or they can be paced by the card's internal pacing timer. The following steps are for triggering burst readings that are paced by the internal pacing timer.

1) Set IPACDA and EPCON high.

2) Request a series of readings with an assembly language routine.

3) Set the EPCON line low. The analog-to-digital conversion for the first reading will start in approximately 3 microseconds.

4) Set the IPACDA line low. This must happen 1 to 15 microseconds after you set EPCON low.

5) Hold EPCON and IPACDA low until all of the requested readings have been taken.

Figure 4-1 shows a simple circuit that can be used to bring IPACDA low an appropriate amount of time after EPCON goes low. This circuit uses the +5 volt power supply from terminal 28 of the wire termination assembly.

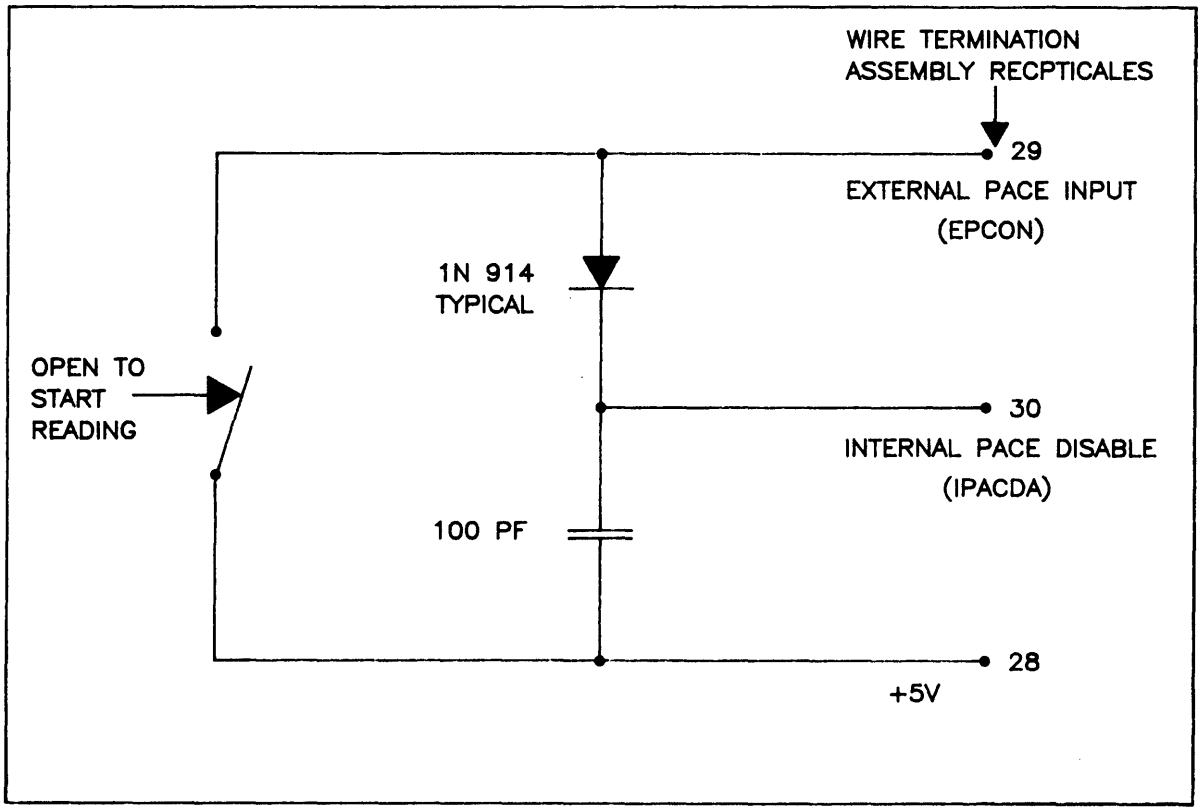


Figure 4-1. IPACDA timing circuit for externally paced burst readings

Combinations. You can combine the above two methods of external pacing if your application requires. We won't go into those combinations here; we leave that as an exercise for the interested reader. The methods above should give you enough information to make your combination work.

Note on BASIC Syntax

If you're programming an application in BASIC you can use the HP 98645A Measurement Library routines to access the HP 98640A card and avoid the burden of writing your own routines. If, however, you need to access the card directly from BASIC, you will have to use READIO and WRITEIO statements as the system IO handlers (such as STATUS, CONTROL, OUTPUT, ENTER) do not recognize this interface.

Remember that the pace and analog data registers on this card are 16 bit registers. To transfer 16 bits of data to/from the card simply specify a negative select code in the READIO/WRITEIO statement.

The following program segment writes a 16 bit value to the pace register:

```
10  Isc= 18                              !select code
20  Pace_reg = 4
30  WRITEIO -Isc,Pace_reg;12232          !sets pace register for 32 msec
```

MAINTENANCE

SECTION V

OVERVIEW

The HP 98640A's A-to-D card does not require adjustment but periodically you may want to verify that it is functioning properly. By following the procedures detailed below you can check the operation of all A-to-D cards installed in your system. Verifying the correct operation of the A-to-D card(s) may require you to attach certain peripherals which may not be part of the normal configuration of your 9000 Series 200 computer. Below we list the required peripherals.

PREPARING TO TEST THE A-TO-D CARD

Minimum equipment requirements

To run the verification program you will need the following peripherals, interfaces for the peripherals, and software for your computer:

a. Keyboard
b. Video display
c. Disk Drive
d. Diagnostic Diskette to fit your disk drive:
   3.5 inch disk, part number 98640-13301, or
   5.25 inch disk, part number 98640-13601
e. Test Assembly, part number 98640-67950

Installing test assembly

DISCONNECTING THE WTA

If you have already installed the wire termination assembly (WTA) you will have to power down your system before you remove it. If you have already wired your computer to an analog circuit with this analog interface DO NOT POWER DOWN YET. You must determine how to proceed based on your circuit design and the specifications of the HP 98640A. Also see Appendix A for more information.

WARNING

BEFORE POWERING-DOWN BE SURE THE PATH TO GROUND THROUGH A 1kOHM RESEITOR THAT WILL RESULT WILL NOT CAUSE EXCESSIVE CURRENT TO FLOW FROM SOURCES ATTACHED

TO THE WIRE TERMINATION ASSEMBLY OR ALTER THE CURRENT READ BY OTHER DEVICES IN THE SAME CIRCUIT WITH THIS INTERFACE.

Once you have taken action to ensure the power-down is safe, power down your system. Now, with the power off, you can disconnect any devices which may interfere with removal of the wire termination assembly(-ies). In some cases you may need to free a backplane slot to accomodate peripherals needed to run the verification program.

You may find it convenient to leave the wires attached to the wire termination assembly(-ies) you are removing. You may have to loosen your strain-relief or remove the wires if they prevent you from removing the wire termination assembly(-ies).

Remove a wire termination assembly by simultaneously unscrewing its thumbscrews. Be prepared to supported the assembly as the screws run out. Pull the assembly straight back, away from the card cage, to avoid bending the right-angle posts on the A-to-D card.

Put the wire termination assembly aside. If wires are attached to it you may be able to use a cable tie to hold the assembly out of your way. Do not allow long lengths of wire to dangle from the termination blocks on wire termination assembly as the wires may be pulled free.

INSTALL PERIPHERALS

Attach any peripherals required to run this test. The instructions for installing a peripheral in your system are included in the peripheral's documentation or your computer's manual. The peripherals required to run the verification program are listed above under the heading "Minimum equipment requirements".

CONNECTING TEST ASSEMBLY

The test assembly is supported by the right-angle posts on the A-to-D card and held in place by friction. If the test assembly is bumped once it is installed the right-angle posts may be damaged. A test assembly must be installed on every A-to-D card to be tested.

Orient the test assembly such that the components are up and the mating connectors line up with the A-to-D card's right-angle posts. Push the assembly forward evenly until the right-angle posts are well seated in the connectors.

CAUTION

Be sure each right-angle post goes into a mating connector otherwise the card may be damaged when the power is turned on. The pressure required to mount the test assembly may be enough to make some 9000 Series 200 computers move.

Now you can test the card by running the verification program.

VERIFICATION TEST

Overview

The verification program allows the user to make a fast check of the operation and accuracy of the A-to-D card. The program gives either a simple GO/NO-GO report, or an optional detailed report on the state of each channel. The floppy disk containing the verification program also contains a stripped-down, execute-only Pascal environment that is bootable on any 9000 Series 200 computer.

CAUTION

Do not touch the test assembly once it is installed and power is applied; you may alter the results of the verification program, if it is running, or you could receive a shock.

Loading the verification program

The verification program is run by inserting the floppy disk in the computer's boot disk drive and loading the system, "SYSTEM_A", from the disk. When the system finishes loading it will transfer control to the verification program "STARTA". There is no command interpreter, so if the verification program ever terminates the computer must be re-booted to restart the verification program. Also, there is no sub-routine to permit scrolling the screen back.

SEQUENCE

The verification program will ask you a few questions. Once the questions have been answered, the verification program will test the specified A-to-D cards in increasing select code order, reporting the results as specified on each card tested. When all the specified cards have been tested, the number of test passes is reported and the testing begins again until the number of test passes requested has been executed. Then the verification program branches and asks "Do you wish to repeat the program (Y/N) ?". If the answer is no, the program terminates, if yes, the verification program starts over from the beginning. We refer to this question as the "repeat program question" in the remainder of this description of the program run.

TESTS PERFORMED
Six tests are conducted on each A-to-D card specified for test. The six tests are:

Handshake Tests
Pace Tests
Calibration Tests
Reading Accuracy Tests
Amplifier Slew Rate Tests
Common Mode Overrange Tests

Program run

The verification program will first scan all the I/O cards searching for ID 18 (ADC) interface cards, and will report the select codes of all found. The select code(s) must correspond to those you set with switches 1 through 5 on the DIP switch (SW1). If the codes do not match and the switches are correctly set, the card has failed even if it passes all other verification tests. See the heading "On Failure" below.

If no A-to-D cards are found the verification program will report "No ADCs were found installed". Then the program will ask the repeat program question.

INSTALLED ADCs
After reporting the select codes of all installed A-to-D cards the verification program asks "Do you wish to verify all ADC cards (Y/N) ?". If the answer is no the programs asks "Verify ADC in select code *n* (Y/N) ?" for each A-to-D card installed replacing *n* with the select code. If all responses are negative, the verification program branches to the repeat program question.

SET REPETITIONS
If any card tests are to be done, the verification program then asks "Specify Repetitions, 0 Repeats Forever, Number of Times to Repeat (default 1) ?". The tests are repeated the specified number of times, looping forever if 0 or a negative number is specified. If the verification program is to loop forever, the message "Hit <STOP> To Terminate Tests" will be displayed. At any time the test may be aborted by hitting the <STOP> or <CLR I/O> key; the program will display a message "ADC Verification Program Stopped By User" and branch to the repeat program question.

Each repetition for each card will take about 2.5 seconds.

PACE TIMER TEST
Once the number of repetitions is specified, the verification program then asks "Include Pace Timer Tests (Y/N) ?". Since the pace timer tests take 99 seconds to execute it is sometimes advisable to skip these tests.

SELECT READINGS TO DISPLAY
Next the verification program will ask "Display All Readings On CRT (Y/N) ?". If the answer is yes, the verification program will display all tests it makes and the measurements taken for those tests. If the answer is no, the verification program will ask "Display Errors On CRT (Y/N) ?". If the answer is

yes, only failing tests and their measurements will be displayed. If the answer is no, only the passed or failed status of each A-to-D card will be displayed, along with the number of test passes that have been run.

RUN-ERROR REPORTING
If any run-time error occurs during execution of the verification program, the error is reported on the CRT and a branch is made to the repeat program question. The verification program tests for errors that correspond with HP 98645A Measurement Library errors. When a Measurement Library error occurs it is reported by both number and description. If some other run time error occurs it is reported by it's Pascal operating system error number or I/O error number as defined in the Pascal 2.1 Users Manual. Tables 5-1 and 5-2 list error codes.

If any run-time errors occur, write the down the error number then repeat the tests. If you still get an error, turn the system off. Gently wiggle the test assembly, turn the power back on and test the card again. If the error(s) still are reported, read the information under the heading "On Failure" below.

NOTE

Always repeat the test if the error code reported is 860 (Offset out of range). Transient noise can cause such an error.

Successful Verification

When an A-to-D card passes the test all you will have to do is:

1. Remove the verification program disk.
2. Power down your system
3. Remove the test assembly by pulling it straight back, away from the card cage, to avoid bending the mating post on the A-to-D card.
4. If you have performed the verification test as part the initial installation of the card go back to Section II, Installation, and pick up from where you were (probably under the heading "Checking a new A-to-D card").
5. If this was just a check of a previously installed A-to-D card, reconfigure your system, if necessary, to suit your application. Consult your system's and peripheral's manuals for help with installing the different pieces of hardware and software. Reattach the wire termination assembly.

On Failure

If your A-to-D card fails the verification test, turn your system off, and remove the test assembly from the A-to-D card. Remove the A-to-D from your system and return the card to your HP Sales and Service office for repair. Please include your list of errors with the card. There is more information on returning a card in Section II, Installation. Look under the heading "Return Shipment".

ERROR CODES

Measurement Library Messages

Message Number	Meaning	Message Number	Meaning
801	Unsupported model	854	Not allowed in interrupt mode
804	Array too small	855	Common-mode overrange
812	Name not configured	856	Normal ADC overrange
815	Use of uninitialized name	857	Pace timing error
835	Illegal select code	858	Unsupported units
837	Specified card not at select code	859	Max number of names exceeded
838	Illegal name	860	Offsets out of range (card deffective or calibration channel not shorted)
850	Unsupported gain		
851	Pace out of range		
852	Repeat specification error		
853	Illegal channel number		

Table 5-1. Measurement Library-related error codes

Pascal-related Messages

Message Number	Meaning	Message Number	Meaning
0	Normal termination	-15	Bad argument - SIN/COS
-1	Abnormal termination	-16	Bad argument - Natural Log
-2	Not enough memory	-17	Bad argument - SQRT
-3	Reference to NIL pointer	-18	Bad argument - real/BCD conversion
-4	Integer overflow	-19	Bad argument - BCD/real conversion
-5	Divide by zero	-20	Stopped by user
-6	Real math overflow; number too large	-21	Unassigned CPU trap
-7	Real math underflow; number too small	-22	Reserved
-8	Value range error	-23	Reserved
-9	Case value range error	-24	Macro parameter not 0 - 9 or a - z
-10	Non-zero I/O result	-25	Undefined macro parameter
-11	CPU word access to odd address	-26	Error in I/O subsystem
-12	CPU bus error	-27	Graphics error
-13	Illegal CPU instruction		
-14	CPU privilege violation		

Table 5-2. Operating system-related error codes

PARTS LISTS

SECTION VI

ORGANIZATION

The following pages contain the parts lists for the HP 98640A 7-channel Analog Input Interface. The lists are for the A-to-D card assembly (98640-66501), the wire termination assembly (98640-66502), and the test assembly (98640-67950). In some literature the test assembly is referred to as a "test hood".

The parts lists are organized as tables which contain the following information about components:

- Reference designation of the part.
- The Hewlett Packard part number.
- Part check digit (CD).
- Total quantity (QTY)
- Description of the part
- Code number identifying a manufacturer of a part
- The manufacturer's part number.

AVAILABILITY

Contact your local HP Sales and Service office if you need to order parts. They can also explain to you how doing your own repairs may affect your warranty. When you order, please give the Hewlett-Packard part number and the check digit.

To order a part not listed in the parts lists:

a. Identify the product containing the part
b. Describe the part and its function.
c. State how many of each part you need.

Table 6-1 (sheet 2). A-to-D card parts.

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	98640-66501	9	1	PCA DIO ADC	28480	98640-66501
C1	0160-4835	7	13	CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C2	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C3	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C4	0160-4847	1	1	CAPACITOR-FXD 1000PF +-10% 100VDC CER	28480	0160-4847
C5	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C6	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C7	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C8	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C9	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C10	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C11	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C12				NOT ASSIGNED		
C13	0180-0374	3	1	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C14	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C15	0180-1746	5	6	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C16	0160-4832	4	17	CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C17	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C18	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C19	0180-0197	8	1	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
C20	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C21	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C22	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C23	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C24	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C25	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C26	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C27	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C28	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C29	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C30	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C31	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C32	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C33	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C34	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C35	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C36	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C37	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C38	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C39	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C40	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C41	0160-4810	8	2	CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-4810
C42	0160-4810	8		CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-4810
C43	0160-4811	9	1	CAPACITOR-FXD 270PF +-5% 100VDC CER	28480	0160-4811
CR1	1902-0589	5	2	DIODE-ZNR 10V 2% DO-7 PD=.4W TC=+.066%	28480	1902-0589
CR2	1902-0589	5		DIODE-ZNR 10V 2% DO-7 PD=.4W TC=+.066%	28480	1902-0589
CR3	1901-0050	3	3	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR4	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR5	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
F1	2110-0297	4	3	FUSE .5A 125V NTD .281X.093	28480	2110-0297
F2	2110-0297	4		FUSE .5A 125V NTD .281X.093	28480	2110-0297
F3	2110-0297	4		FUSE .5A 125V NTD .281X.093	28480	2110-0297
J1	1252-0145	0	1	CONN-HEADER	28480	1252-0145
K1	9100-0539	3	2	INDUCTOR (MISC ITEM)	28480	9100-0539
K2	9100-0539	3		INDUCTOR (MISC ITEM)	28480	9100-0539
Q1	1854-0090	0	2	TRANSISTOR NPN SI TO-39 PD=1W FT=100MHZ	28480	1854-0090
Q2	1854-0090	0		TRANSISTOR NPN SI TO-39 PD=1W FT=100MHZ	28480	1854-0090
R1	0683-1035	1	4	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R2	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R3	0683-4725	2	4	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R4	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R5	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R6	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R7	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R8	0683-5645	7	1	RESISTOR 560K 5% .25W FC TC=-800/+900	01121	CB5645
R9	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R10	1810-0205	7	1	NETWORK-RES 8-SIP4.7K OHM X 7	01121	208A472

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1 (sheet 2). A-to-D card parts.

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R11	0811-3482	9	1	RESISTOR 100 5% .5W PW TC=0+-150	28480	0811-3482
R15	0757-0288	*	1	RESISTOR 9.09K 1% .125 FC TC=-400/+700	01121	CB90935
R16	0757-04432			RESISTOR 11K 1% .125 FC TC=-400/+700	01121	CB1135
U1-						
U11				NOT ASSIGNED		
U12	1826-0791	9	1	IC SMPL/HOLD 8-DIP-P PKG	27014	LFN398N
U13-						
U21				NOT ASSIGNED		
U22	[illegible] 1081	2	5	IC OP AMP PRCN 8-DIP-P PKG	28480	1826-1081
U23	1826-1081	2		IC OP AMP PRCN 8-DIP-P PKG	28480	1826-1081
U24	1810-0727	8	1	RES NTWK DIP	28480	1810-0727
U25				NOT ASSIGNED		
U26	1820-1432	5	4	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U27	1820-2024	3	2	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U28	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U29	1820-2075	4	2	IC MISC TTL LS	01295	SN74LS245N
U30				NOT ASSIGNED		
U31				NOT ASSIGNED		
U32	1826-1081	2		IC OP AMP PRCN 8-DIP-P PKG	28480	1826-1081
U33	1826-0138	8	1	IC COMPARATOR GP QUAD 14-DIP-P PKG	01295	LM339N
U34				NOT ASSIGNED		
U35				NOT ASSIGNED		
U36	1820-1432	5		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U37	1820-1997	7	5	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U38	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
U39	1820-2740	0	1	IC COMPTR TTL LS MAGTD 2-INP 8-BIT	01295	SN74LS688N
U40-						
U43				NOT ASSIGNED		
U44	1826-1081	2		IC OP AMP PRCN 8-DIP-P PKG	28480	1826-1081
U45	1826-0590	6	1	IC MULTIPLXR 4-CHAN-ANLG DUAL 16-DIP-C	27014	LF13509D
U46	1820-1112	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U47	1820-1432	5		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U48	1820-1432	5		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U49	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U50	1820-2056	1	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS378N
U51-						
U53				NOT ASSIGNED		
U54	1826-1081	2		IC OP AMP PRCN 8-DIP-P PKG	28480	1826-1081
U55-						
U60				NOT ASSIGNED		
U61	1810-0037	3	2	NETWORK-RES 16-DIP1.0K OHM X 8	11236	761-3-R1K
U62	1906-0074	1	2	DIODE-ARRAY 50V 400MA	28480	1906-0074
U63				NOT ASSIGNED		
U64	1820-2183	5	1	IC MULTIPLXR 8-CHAN-ANLG DUAL 28-DIP-P	28480	1820-2183
U65	1826-1226	7	1	IC 6112 ADC	28480	1826-1226
U66				NOT ASSIGNED		
U67	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U68	1816-1547	4	1	IC TTL LS 2048 (2K) PROM 70-NS 3-S	28480	1816-1547
U69	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U70	1820-2056	1		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS378N
U71	1810-0037	3		NETWORK-RES 16-DIP1.0K OHM X 8	11236	761-3-R1K
U72	1906-0074	1		DIODE-ARRAY 50V 400MA	28480	1906-0074
U73-						
U76				NOT ASSIGNED		
U77	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U78	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U79	1820-1427	8	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS156N
U80	1820-1201	6	3	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U81	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U82	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U83	1820-1574	6	1	IC FF TTL LS J-K PULSE CLEAR DUAL	01295	SN74LS73AN
U84	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U85	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U86	1820-1200	5	1	IC INV TTL LS HEX	01295	SN74LS05N
U87-						
U91				NOT ASSIGNED		
U92	1820-1285	6	1	IC GATE TTL LS AND-OR-INV 4-INP	01295	SN74LS54N
U93	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U94	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U95	1820-1208	3	2	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U96	1820-2488	3	1	IC FF TTL ALS D-TYPE POS-EDGE-TRIG	01295	SN74ALS74N
U97	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U98	1820-2096	9	1	IC CNTR TTL LS BIN DUAL 4-BIT	01295	SN74LS393N
U99	1820-1491	6	1	IC BFR TTL LS NON-INV HEX 1-INP	01295	SN74LS367AN

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1 (sheet 3). A-to-D card parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U30	1813-0431	2	1	XTAL OSC 1666 MHZ	28480	1813-0431
U101	1826-0220	9	1	IC V RGLTR TO-39	27014	LM320H-5*
	4040-0752	2	2	EXTR-PC BD YEL POLYC .062 BD-THKNS	28480	4040-0752
	98640-26501	5	1	PC BOARD	28480	98640-26501
	98640-81001	6	1	BURN-IN	28480	98640-81001
	1460-0116	6	2	PIN, GRV., 0.062 X 0.25 IN.		

Table 6-2. Manufacturers.

MANUFACTURER CODE LIST

MFR NO.	MANUFACTURER NAME	ADDRESS		ZIP CODE
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC, SEMICOND COMPNT DIV	DALLAS	TX	75222
11236	CTS OF BERNE	BERNE	IN	46711
19701	MEPCO/ELECTRA CORP	MINERAL WELLS	TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Wire termination assembly parts.

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	98640-66502	0	1	PCA SCR TERM	28480	98640-66502
CR1	1902-1404	5	20	DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	28480	1902-1404
CR2	1902-1404	5		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	28480	1902-1404
CR3	1902-1404	5		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	28480	1902-1404
CR4	1902-1404	5		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	28480	1902-1404
CR5	1902-1404	5		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	28480	1902-1404
CR6	1902-1404	5		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	28480	1902-1404
CR7	1902-1404	5		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	28480	1902-1404
CR8	1902-1404	5		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	28480	1902-1404
CR9	1902-1404	5		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	28480	1902-1404
CR10	1902-1404	5		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	28480	1902-1404
CR11	1902-1404	5		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	28480	1902-1404
CR12	1902-1404	5		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	28480	1902-1404
CR13	1902-1404	5		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	28480	1902-1404
CR14	1902-1404	5		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	28480	1902-1404
CR15	1902-1404	5		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	28480	1902-1404
CR16	1902-1404	5		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	28480	1902-1404
CR17	1902-1404	5		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	28480	1902-1404
CR18	1902-1404	5		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	28480	1902-1404
CR19	1902-1404	5		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	28480	1902-1404
CR20	1902-1404	5		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	28480	1902-1404
F1	2110-0297	4	1	FUSE .5A 125V NTD .281X.093	28480	2110-0297
P1				NOT ASSIGNED		
P2*	0360-2221	5	3	SCREW TERMINATION	28480	0360-2221
R1	0683-1515	2	1	RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
	1252-0164	3	2	CONN-SOCKET 12	28480	1252-0164
	98640-00001	6	1	98640A CVR PLATE	28480	98640-00001
	98640-26503	7	1	PCB TEST HOOD	28480	98640-26503
	2360-0200	8	2	SCREW, 6-32 X 0.5 IN.		
	0380-0004	0	2	STANDOFF, #8 X 0.188 IN.		
	2420-0003	7	2	NUT, 6-32		
	98640-00003	8	1	TERM. CVR. PLATE		
	98640-80004	7	1	WARNING LABEL		

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-4. Test assembly parts.

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	98640-67950	4	1	PCA TEST HOOD	28480	98640-67950
CR29				NOT ASSIGNED		
CR2	1902-3066	9	1	DIODE-ZNR 4.02V 2% DO-35 PD=.4W	28480	1902-3066
P1	1252-0164	3	2	CONN-SOCKET 12	28480	1252-0164
R1	0757-0288	1	1	RESISTOR 9.09K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-9091-F
R2	0698-3153	9	1	RESISTOR 3.83K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3831-F
R3	0757-0280	3	1	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R4	0757-0401	0	1	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
R5	0757-0346	2	2	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R6	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R7	0757-0398	4	1	RESISTOR 75 1% .125W F TC=0+-100	24546	C4-1/8-T0-75R0-F
R8	0757-0290	5	1	RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
W1	0811-3587	5	8	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
W2	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
W3	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
W4	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
W5	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
W6	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
W7	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
W8	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
	98640-66501	7	1	PCB TEST HOOD	28480	98640-26503

See introduction to this section for ordering information
*Indicates factory selected value

DIAGRAMS

SECTION VII

This section contains component location drawings, and schematic diagrams for the HP 98640A. The material is arranged as follows:

Figure

7-1. Custom resistor network (U24).
7-2. A component location diagram for the A-to-D card and the wire termination assembly.
7-3. A component location diagram for the test assembly.
7-4. Schematic diagrams of the A-to-D card circuit. Three sheets.
7-5. A schematic diagram of the wire termination assembly.
7-6. A schematic diagram of the test assembly.
7-7. PROM output codes

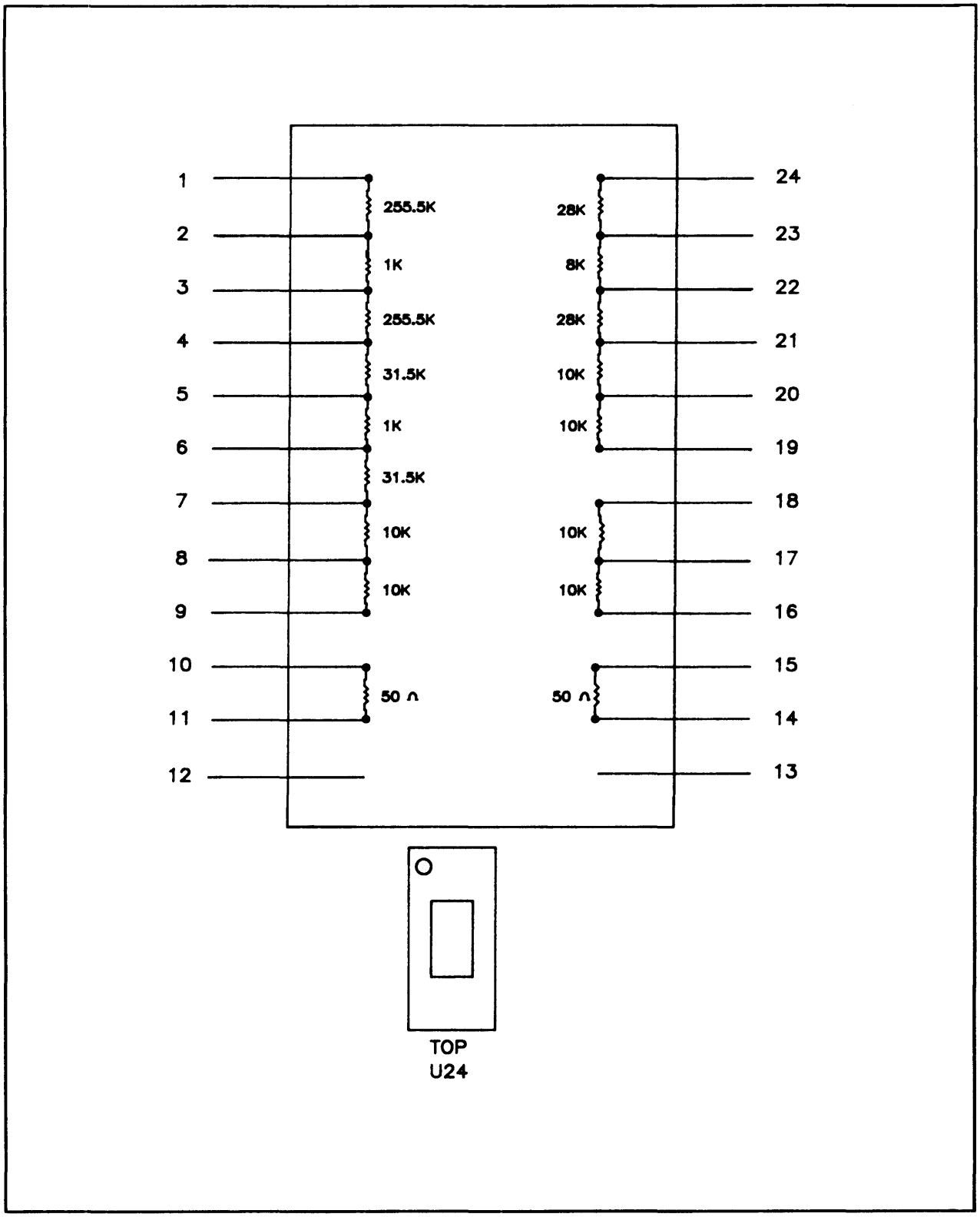


Figure 7-1. Custom resistor network.

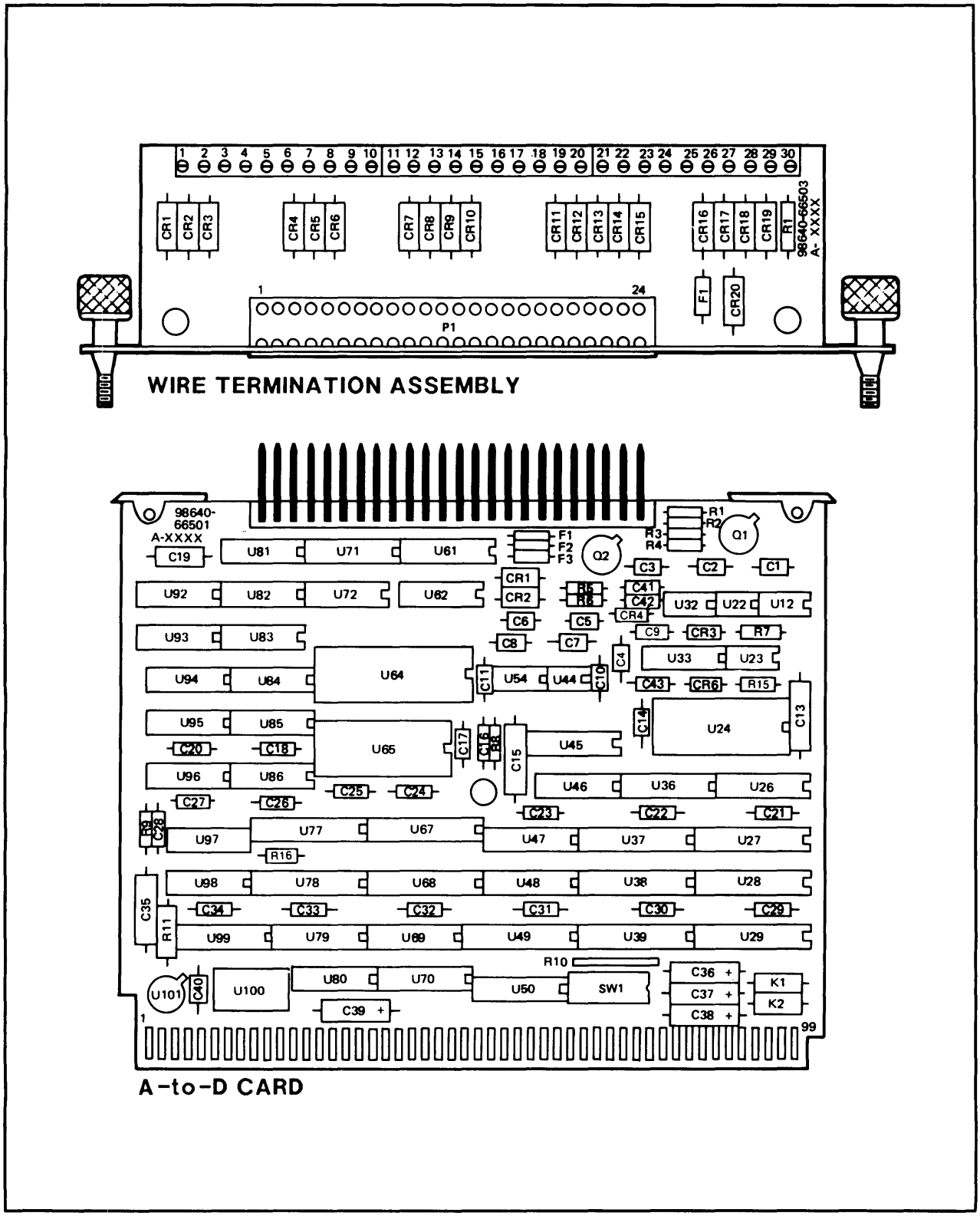


Figure 7-2. Component locations.

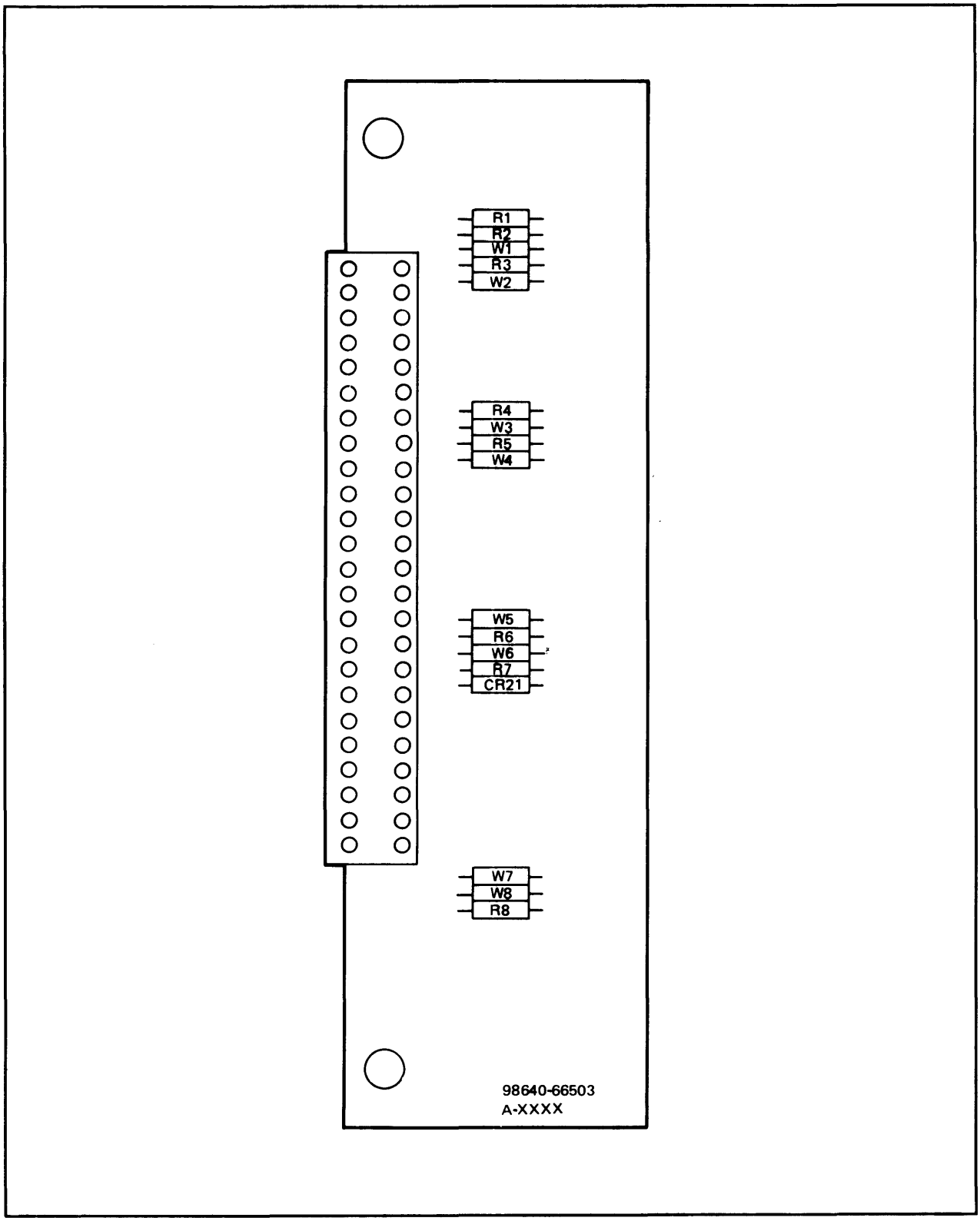


Figure 7-3. Component locations on the test assembly.

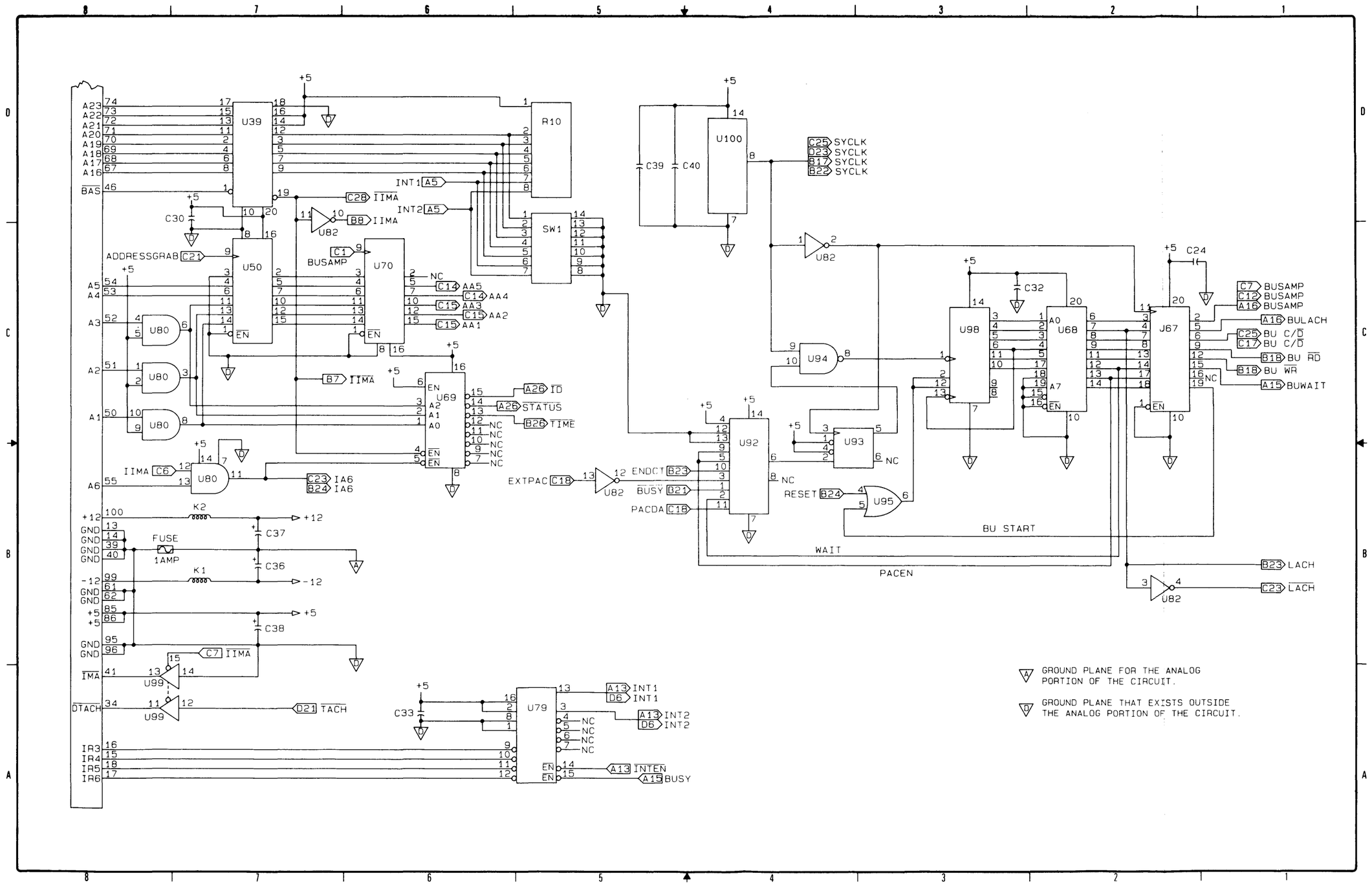


Figure 7-4. A-to-D card schematic diagram, sheet 1 of 3.

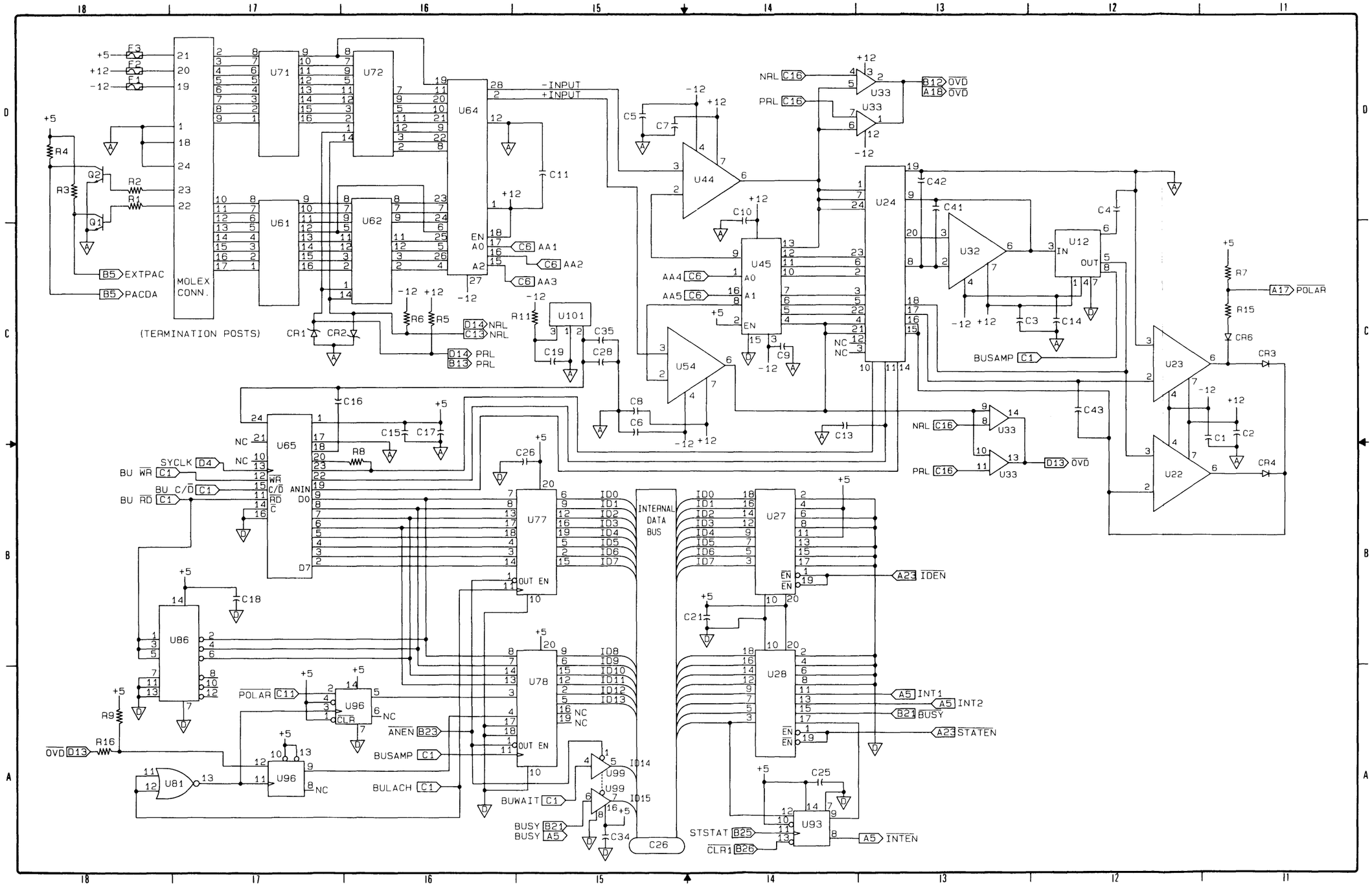


Figure 7-4. A-to-D card schematic diagram, sheet 2 of 3.

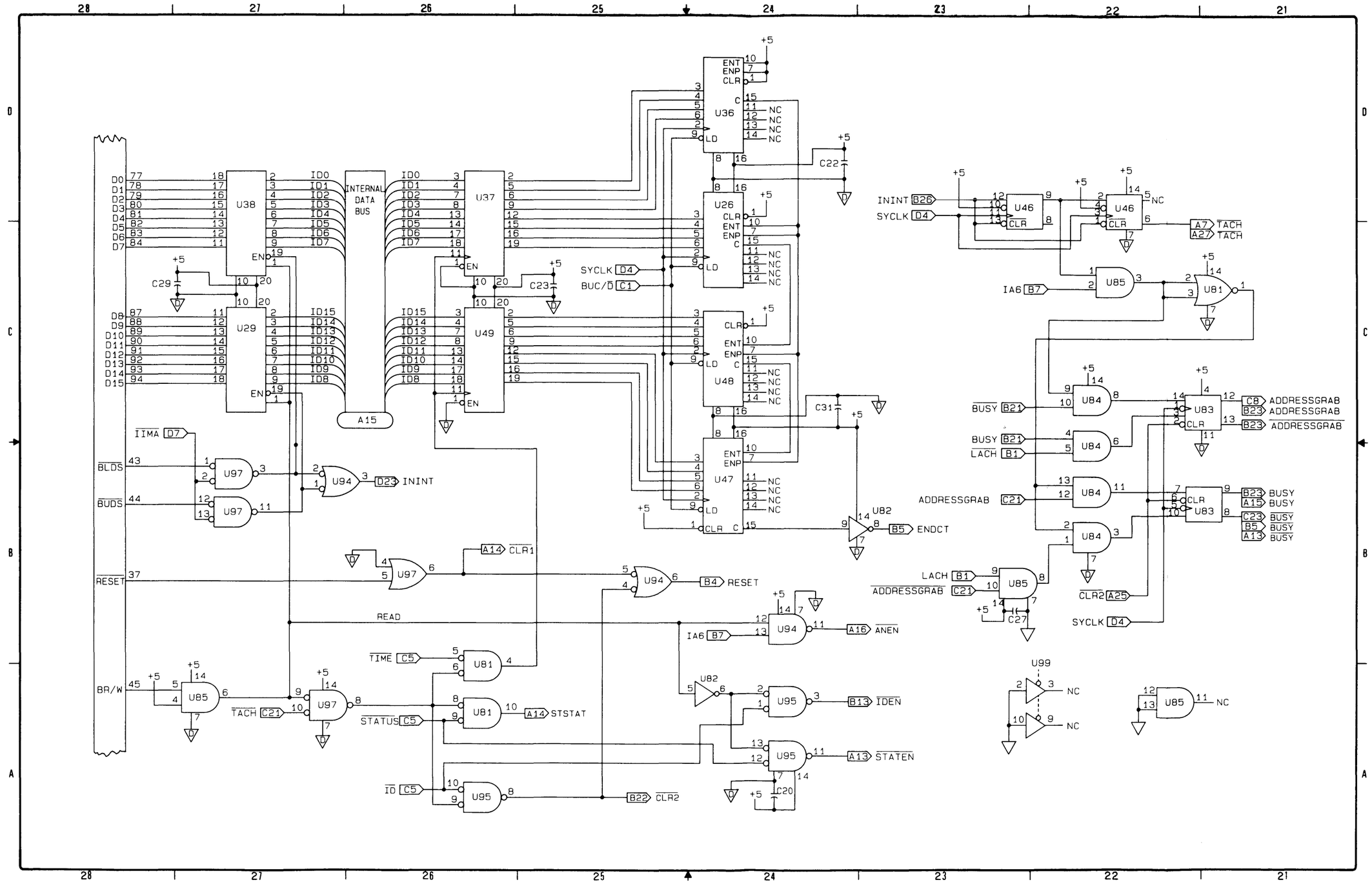


Figure 7-4. A-to-D card schematic diagram, sheet 3 of 3.
7-9/7-10

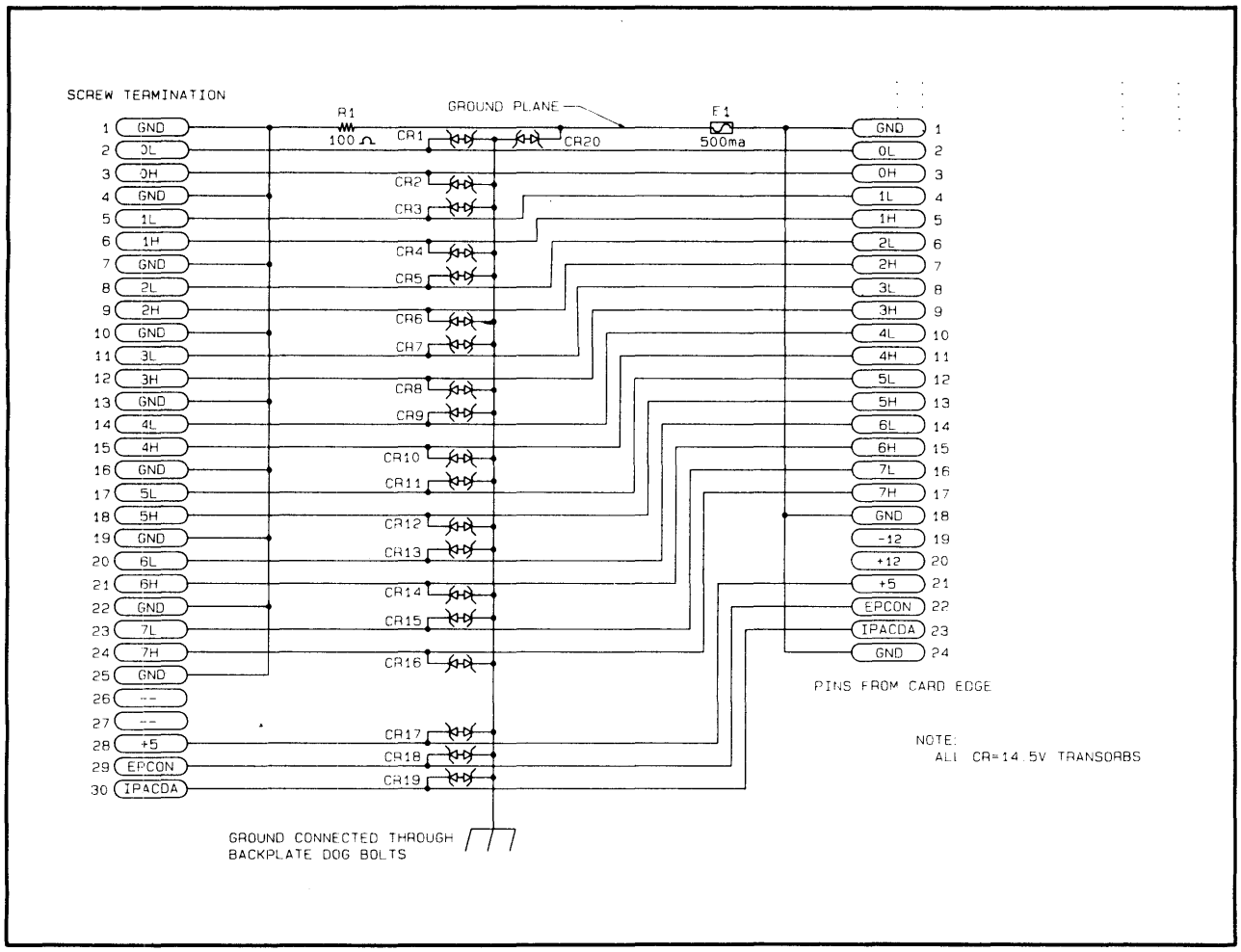


Figure 7-5. Wire termination assembly schematic diagram.

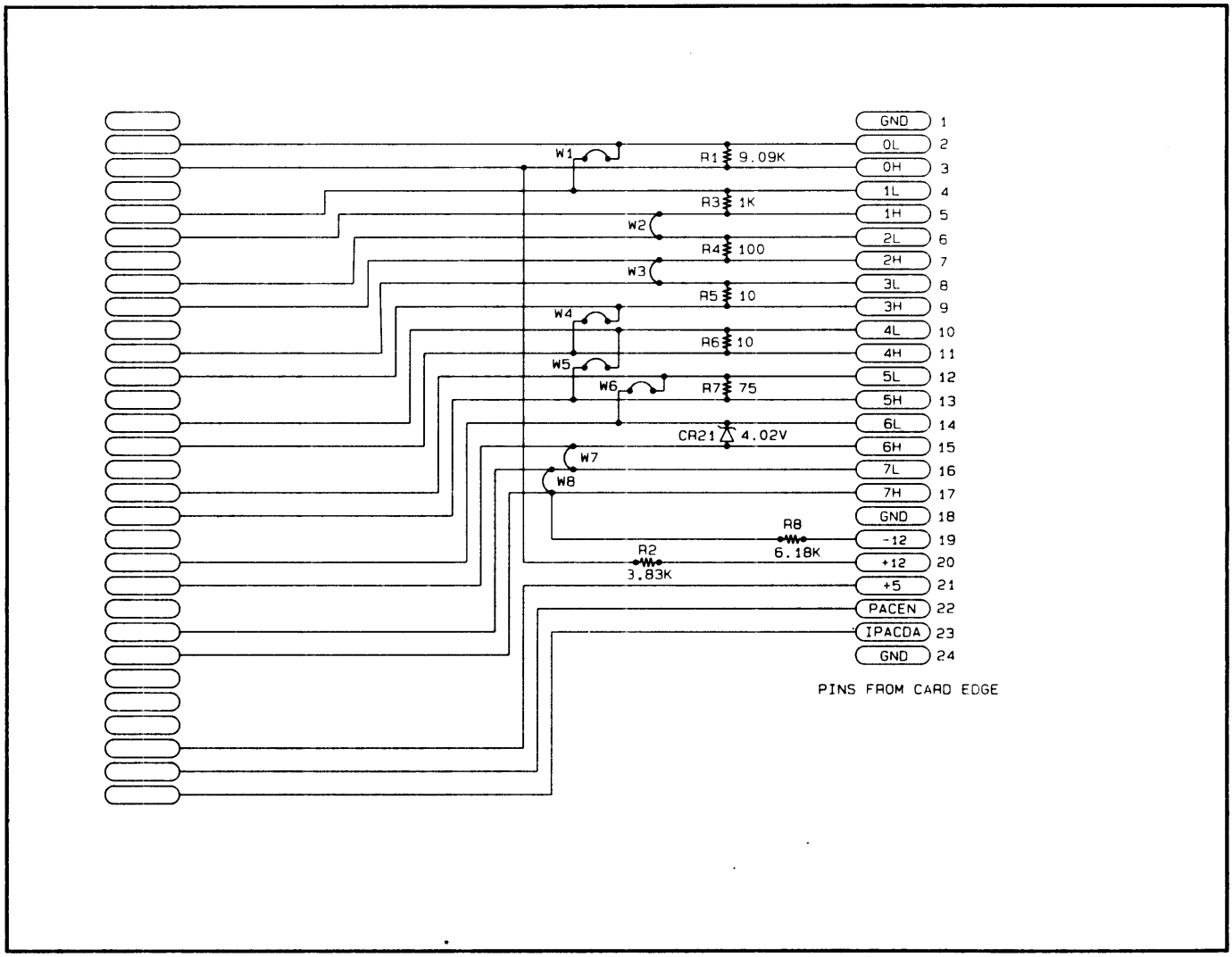


Figure 7-6. Test assembly schematic diagram.

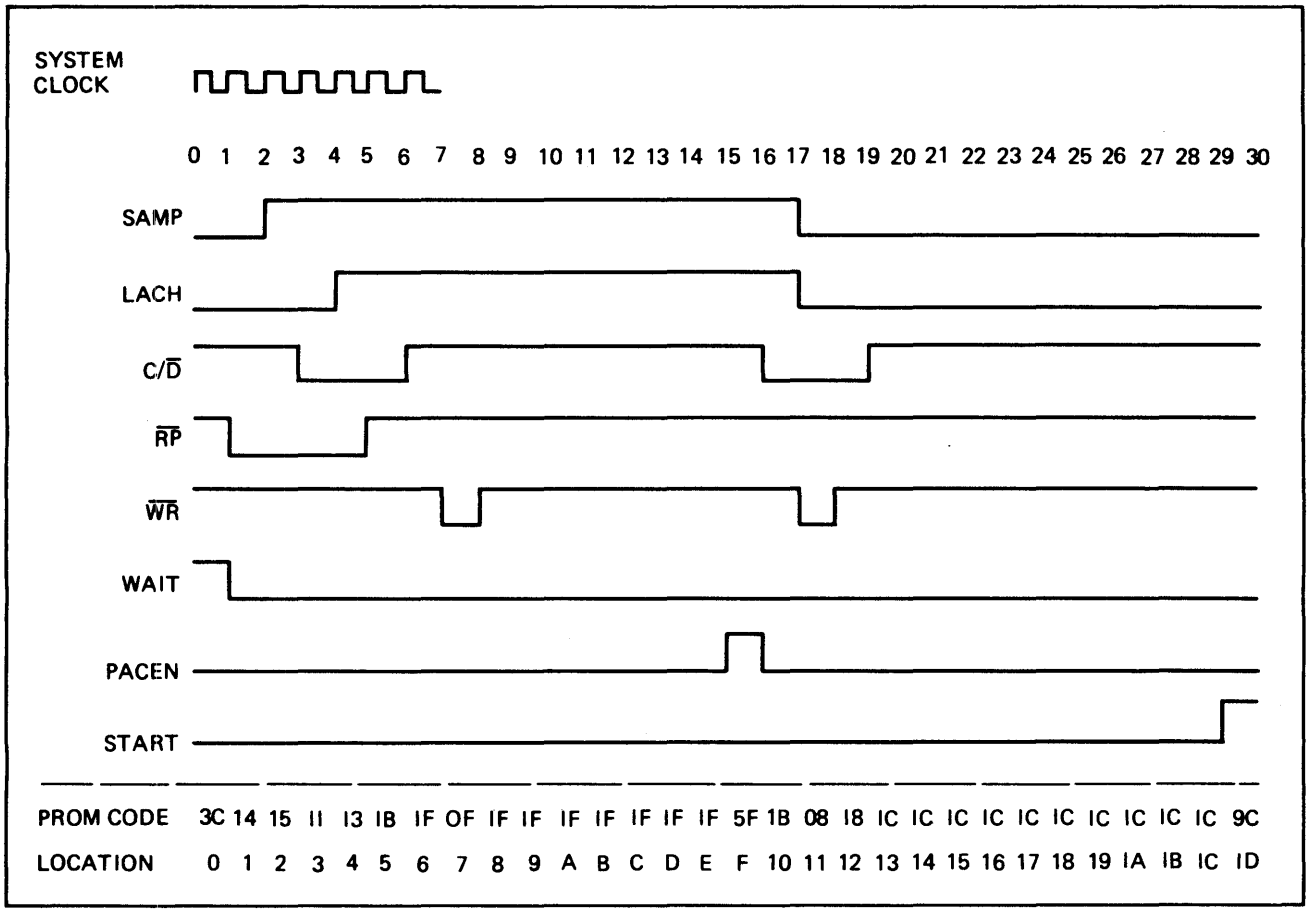


Figure 7-7. PROM code.

INADVERTANT GROUND: A SAFETY CONSIDERATION

APPENDIX A

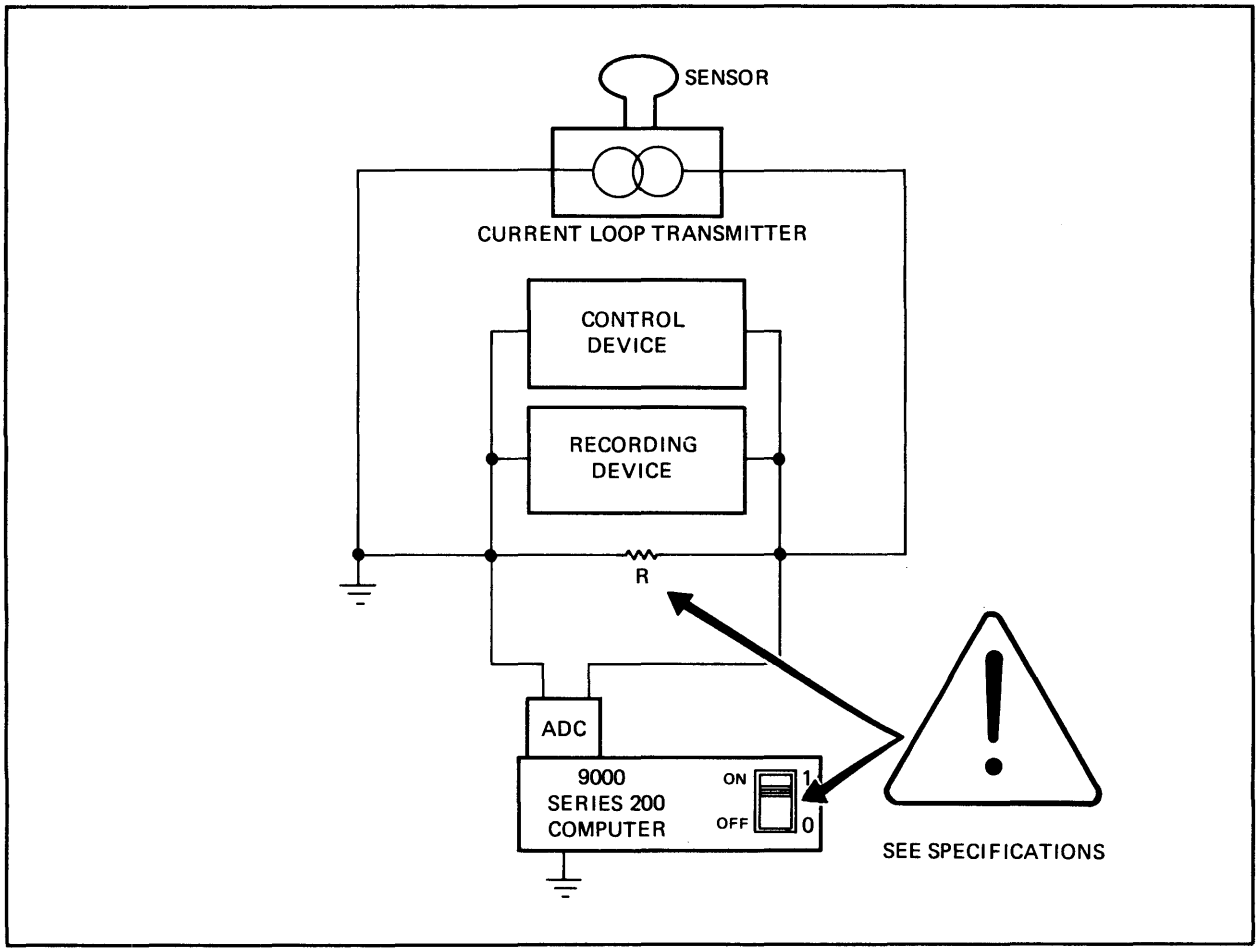


Figure A-1. Be cautious using the ON/OFF switch.

This circuit is an example of some of the circuits you may be considering attaching your ADC to. Please keep in mind any input's isolation from ground is only 1000 (one thousand) ohms when the computer is turned off or IF POWER TO THE COMPUTER FAILS. If the resistor R is not significantly smaller than 1000 ohms then the ADC will become a major secondary path to ground.

The resulting change in the voltage drop across R will affect other devices attached across R. In certain cases the effect could cause dangerous situations to develop because people or control devices would react to faulty data.

There may be many other circuits in use which may cause a similar problem. Please consider the all characteristics of the HP 98640A before adding it to a circuit.

GLOSSARY

This glossary provides a narrow definition of a term used in this manual. These should not be regarded as technically complete definitions.

ADC, A-to-D card - see analog-to-digital converter

address data - commands the card receives when the computer reads data from specific address offsets on the card. These commands specify the gain and channel the card will use to take a reading. See analog read.

alias - Two signals of different frequencies are aliases of one another if they cannot be distinguished from each other based on an analysis of samples taken at equally spaced intervals.

analog-to-digital converter - The integrated circuit (IC) which compares the differential input voltage on a channel to a reference voltage. The ADC reports what portion of the reference voltage the input was. A-to-D card refers to the main printed circuit assembly of the HP 98640A.

Analog read - a word-wide (16 bit) read of the A-to-D card where the address used includes an even offset of between 64 and 126 (decimal), inclusive. The A-to-D will retain the offset (less the unused lsb) and treat it as an encoded command if the busy bit was not set to one at the time of the read.

busy bit - 16th bit (D15) of data returned when an Analog read of the card is made. If this bit is set to one the remainder of data should be regarded as invalid. Further more, the address data will not be retained by the card. This bit provides immediate information about the status of the card.

card - Refers to the main printed circuit assembly of the HP 98640A.

center voltage - The voltage half-way between the voltages on the input leads of a channel.

common mode overrange - An error condition due to:

a. One or both input voltages on a channel exceed input voltage limits.
b. A center voltage so close to one of the input-voltage limits that when the signal is amplified a linear result would be a higher voltage than the amplifier can deliver.

current loop - Refers to a communications or control system which alters current in a circuit to transmit data or commands. Typically, such systems are referred to by the maximum current the system can produce such as "20ma current-loop".

dog bolts - The captive thumbscrews used to secure cover plates to the back of the computer.

floating source - A voltage source which is not referenced to ground. A battery is an example.

K, k - Upper-case K stands for 1024 (2 to the 10th power). Lower-case k stands for 1000 (10 to the 3rd power).

lsb - least significant bit

msb - most significant bit

one lsb sample-rate - The maximum rate the A-to-D card can sample a channel without introducing errors. The rate also depends on whether a single channel is being continuously sampled or the channel being read is changed after each sample.

op amp - see operational amplifier

operational amplifier - A linear voltage amplifier which has high open loop DC gain, high input impedance, wide bandwidth, and low output impedance. Operational amplifiers also have some characteristics which must be compensated for or lived with. Those are input offset voltage, slew rate limitations, and gain band-width limitations.

normal mode overrange - An error caused by excessive differential voltage across the inputs of any channel of the HP 98640A. Exactly what constitutes a normal mode overrange depends on the gain in use. See the specifications. This overrange will occur when the differential voltage is equal to or greater than the full scale voltage. Normal mode overrange at the time that a sample of a particular channel was made is indicated when the 12 least significant bits (D11 to D0) of the data from that sample are all set to one.

PCA - see printed circuit assembly

printed circuit assembly - The finished product made up of the printed circuit board plus any permanently attached components.

slew rate - The rate at which an op amp can change its output voltage. By convention the time period referred to is always one microsecond. As the gain goes up the slew rates go down.

thumb screws - see dog bolts

transorb - A switching device that begins to conduct at a specific voltage. In schematic diagrams it appears as back-to-back zener diodes.

WTA - see wire termination assembly

wire termination assembly - The a printed circuit assembly attached to the outside face of the ADC's cover plate. Among components on the wire termination assembly are wire termination blocks, mating connectors which engage right-angle posts on the A-to-D card, and transorbs to direct excessive voltage to ground.

INDEX

A

B

C

D

E

G

H

I

L

M

N

O

P

R

S

T

U

V

W

READER COMMENT SHEET

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