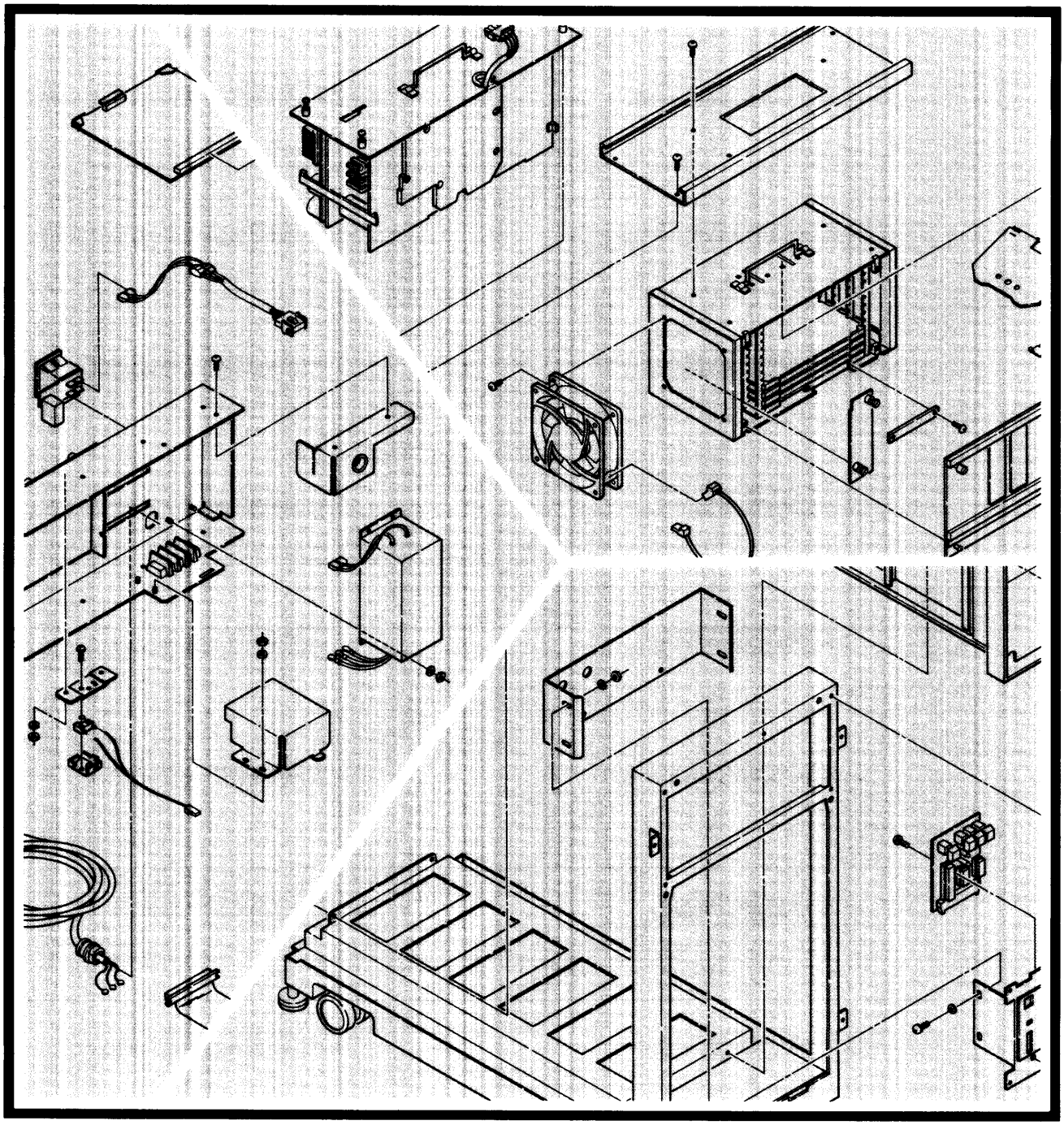
HP 9000 Series 500 Computers
Models 530/540

HEWLETT PACKARD

HP 9030/9040 Service Manual



HP 9030/9040 Service Manual

for the HP 9000 Series 500
Models 530/540 Computers

Manual Part No. 09040-90038

This service manual is part of the HP 9000 Models 530 and 540 Service Documentation Package, part number 09040-80030. The package consists of the following items:

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HP 9000 Models 530 and 540 Installation and Test Manual	09040-90011
HP Sales and Support Offices Brochure	5955-6587
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Hewlett-Packard Company
3404 East Harmony Road, Fort Collins, Colorado 80525

Printing History

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General Information

Chapter 1

Introduction

Note

Hewlett-Packard assumes no responsibility for customer repairs or modifications.

This manual contains servicing information for the Hewlett-Packard HP 9030/9040 Computers (hereinafter referred to as the computer). HP supports repairing the computer to the assembly level, that is, isolating the problem to the replaceable assembly. Then the defective assembly is exchanged for a new or rebuilt assembly.

Included in this chapter is general information about the computer and its servicing.

Additional information in this manual includes:

- Theory of Operation
- Troubleshooting Procedures
- Assembly Access Procedures
- Replaceable Parts
- Technical Data (Specifications and Options)
- Installation and Test
- Motherboard, I/O Backplane, and System Control Model (SCM) Pinout Data
- Option Installation Notes
- Sales and Support Offices

Note that the computer specifications and options are contained in Appendix A. Also, installation information is not contained in this chapter but is found in Appendix B.

Note

If you are unfamiliar with the computer, read the Installation and Test manual contained in Appendix B of this manual.

Description

The computer is a 32-bit system with integral processor stack, power supply, and I/O backplane with seven HP-CIO card slots. Other system assemblies include an ac power module, motherboard, user-accessible service panel with switches and LEDs, and system control module. The system control module contains the real-time clock and the operating system loader read-only memory (ROM).

The computer has a UNIX operating system which is random-access memory (RAM) based and loaded from an external disc.

The computer processor consists of an NMOS-III-based processor stack that at a minimum contains a central processor unit (CPU), an I/O processor (IOP), and memory assemblies. The CPU, IOP, and memory consist of NMOS-III chips. All cards reside in the stack and communicate via the common memory processor bus (MPB).

Cooling air is drawn through the stack between the boards to dissipate heat from the chips. The boards are accessible from the front of the computer.

The CPU chip is a microprogrammed 32-bit processor. The IOP chip interfaces to the system I/O bus. Each IOP supports eight select codes. Up to three IOPs can be included in the computer, enabling a total of 24 select codes. The RAM chips are addressed by a memory controller chip that corrects all single-bit errors. User memory ranges from 190K bytes to 10M bytes.

The I/O cards are accessible from the rear of the computer.

The computer is housed in an 8.75-inch System II rack enclosure (HP 9030) or in a stand-alone cabinet (HP 9040). Directional references in the following paragraph to left and right refer to the HP 9030; references to bottom and top refer to the HP 9040.

Three dc box fans provide cooling for the computer. The fans draw air through the left side (or bottom) and exhaust the air out the right side (or top). One fan is integral to the processor stack and is mounted at the left side (or bottom). The other fans are mounted to the chassis at the right side (or top), one in the power supply area and one in the I/O card cage area. The I/O card cage fan operates at a constant speed. The other two fans are variable, increasing in speed as the temperature increases. The computer shuts down if the temperature rises to 100°C in the stack or to 97°C in the power supply.

Standard features include CPU and IOP, 500K bytes of RAM, seven HP-CIO slots, the internal real-time clock, an operating system loader ROM, and a customer-accessible fault diagnostic display (service panel). Options include one or two additional CPUs, one or two additional IOPs which connect to 97098A I/O Expanders, and RAM expansion to a maximum of 10M bytes (including system and user memory). Refer to Appendix A (the Technical Data section) for additional information on options.

Warnings, Cautions, and Notes

Warnings, cautions, and notes are used throughout this manual. Warnings call attention to potential hazards for personnel. Cautions call attention to potential hazards for equipment. Notes emphasize important information or instructions.

Although all warnings, cautions, and notes are important, one warning and one caution are included here to acquaint you with computer considerations.

WARNING

WAIT AT LEAST 15 MINUTES AFTER TURNING OFF POWER, OR DISCHARGE POWER SUPPLY CAPACITORS USING POWER SUPPLY DISCHARGE TOOL, PART NUMBER 09855-67004, BEFORE REMOVING POWER SUPPLY FROM COMPUTER. FAILURE TO FOLLOW THIS PROCEDURE COULD RESULT IN EXPOSURE TO LETHAL SHOCK HAZARD.

CAUTION

TO PREVENT DAMAGE DUE TO ELECTROSTATIC DISCHARGE (ESD), FOLLOW THE PROCEDURES PROVIDED IN CHAPTER 4.

Repair Philosophy

The computer repair philosophy involves diagnosis of symptoms, overlapping levels of diagnostics, service utilities, and assembly replacement within 15 minutes.

The computer is repaired at an assembly replacement level. Parts that are most commonly replaced are exchange parts and are on the Computer Support Division (CSD) exchange program. When an exchange part fails, it should be returned to CSD for repair, and a rebuilt part should be obtained. If a new part is purchased instead, it is unnecessary to return the failed part. Chapter 5 contains a list of exchange parts with new and rebuilt part numbers, a list of module-level non-exchange parts, and a list of all replaceable parts.

In addition to the standard Field Service Inventory (FSI) sets, several other sets are available depending on the selected options. These are as follows:

- GP-IO I/O Card FSI
- HP-IB I/O Card FSI
- ASI I/O Card FSI
- PSI I/O Card FSI
- MUX I/O Card FSI
- LAN I/O Card FSI

Ac Components/Power Cords

WARNING

IF IT IS NECESSARY TO REPLACE THE POWER CORD, THE REPLACEMENT CORD MUST HAVE THE SAME POLARITY AS THE ORIGINAL CORD. OTHERWISE, A SHOCK HAZARD MIGHT EXIST WHICH COULD RESULT IN INJURY OR DEATH. ALSO, THE EQUIPMENT COULD BE SEVERELY DAMAGED IF EVEN A RELATIVELY MINOR INTERNAL FAILURE OCCURRED.

An attached power cord plugs into an ac outlet to provide primary power to the computer. Power cord part numbers are listed in Chapter 5. Chapter 4 contains a power cord replacement procedure.

The computer is wired for either 90-125V or 198-250V ac and can be converted from one to the other in the field. Conversion requires changing the power switch assembly, power supply cable, ac power cord, and label. Chapter 4 has procedures for changing these components.

Safety

WARNING

LETHAL VOLTAGES ARE PRESENT INSIDE THE COMPUTER. OBSERVE ALL WARNINGS IN THIS MANUAL, AND OBSERVE THE FOLLOWING SAFETY PROCEDURES AND GUIDELINES.

General Safety Procedure

- Do all possible operations with the computer power cord unplugged from the ac outlet.
- If installation, maintenance, or repair must be done with the computer energized, take the following precautions:
    a. Never work alone in high-voltage areas. In case of accidental shock, a life may depend on rapid removal from the energized source and appropriate first-aid action.
    b. Employees working in high-voltage areas should know where to obtain respiratory resuscitation and/or cardiopulmonary resuscitation (CPR), in case a fellow worker needs assistance.
    c. In case of burns, treat only after the person is breathing and has a normal heartbeat.
- If primary wiring change is made, perform continuity test between power cord ground and metal chassis. Record results on repair order.

These simple precautions can save a life.

Safety Guidelines for High-Voltage Testing

Here is a list of safety guidelines to be followed when working with voltages in excess of 50V dc or 50V ac root-mean-square (RMS).

1. Know each step of the test procedure. Check the test setup to be sure the instruments are connected properly and that all control settings are correct.
2. Never defeat interlocks.
3. Never have one hand on chassis or other ground while measuring high voltages with a probe held in the other hand. Use the one-hand method, that is, probe in one hand, the other hand behind the back or in a pocket.
4. Make sure the probe being used has voltage insulation higher than the voltage being measured. Check wires and probes for cracked insulation and defects. If any defects are noted do not use until repairs are made.
5. Make certain that the instrument to be serviced is turned off and all capacitors and high-voltage circuits are discharged before any component or hardware is removed or touched. Remember that a circuit can be lethally charged if a component is open or missing, or if a wire is disconnected or open, even with the ac power switch off. Isolated heat sinks can also be statically charged.
6. Make certain that instruments used for testing are used within their rated specification. Never use instruments floated above their specified rating.
7. Never reach around energized high-voltage circuits. Always turn equipment off and discharge the high voltage first.
8. NEVER WORK ALONE. Be familiar with location of power switches in your area and what they control. Turn off power to free a fellow worker from high voltage without energizing yourself.
9. Keep work area neat, free of any interfacing conductive material, and free of any sharp objects. Remember, a reaction to a shock can cause one to strike nearby objects which can result in a serious injury.
10. Always leave safety shields in place unless work must be done on circuits behind the shields.
11. Never leave work area with high-voltage equipment energized and high-voltage circuits exposed.
12. Have available and use approved warning signs and tags where high-voltage testing is in process.
13. Do not make measurements in a circuit where a corona is present. Corona can be identified by a pale-blue color, from a buzzing sound emanating from sharp metal points in the circuit, or from the odor of ozone.
14. Hands, shoes, floor, and workbench must be dry. Avoid making measurements under humid, damp, or other environmental conditions that could affect the dielectric-withstanding voltage of the test leads or instruments.
15. All test procedures and safety procedures should be strictly followed at all times.

Grounding Requirements

To protect operating personnel, the National Electrical Manufacturers' Association (NEMA) recommends that the computer chassis be grounded. The computer is equipped with a three-conductor power cable which, when connected to an appropriate power receptacle, grounds the computer chassis.

Computer Cleaning

Exterior case parts and the air intake filter (HP 9040 only) should be checked and cleaned as required per the following instructions.

Case

The computer has been painted with a durable, long lasting, water-based paint which is non-toxic and environmentally safe. It will preserve the appearance of the computer for many years. Clean the computer according to the following instructions to sustain the quality finish indefinitely. Should the finish be damaged, consult your local HP Sales and Support Office (Appendix G) for available touch-up paints.

CAUTION

CHEMICAL SPRAY-ON CLEANERS USED FOR APPLIANCES AND OTHER HOUSEHOLD APPLICATIONS MAY DAMAGE THE FINISH. THESE OR OTHER CHEMICAL CLEANERS SHOULD NOT BE USED. DO NOT USE DETERGENTS THAT CONTAIN AMMONIA, BENZENES, CHLORIDES, OR ABRASIVES. DISPLAY GLASS SHOULD NOT BE CLEANED WITH ANY CLEANER. ONLY CLEAN WATER SHOULD BE USED FOR CLEANING DISPLAY GLASS.

Before cleaning the computer, turn off the power switch, unplug the power cord, and remove any interconnecting cables. Dampen a clean, soft, lint-free cloth with a solution of clean water and mild soap. Wipe the soiled areas of the computer, ensuring that no cleaning solution gets inside the computer. For cleaning more heavily soiled areas, a solution of 80% clean water and 20% isopropyl alcohol may be used. Using a clean, soft, lint-free cloth dampened with clean water, wipe over all areas that were cleaned with cleaning solution. Then dry the computer with a clean, soft, dry cloth. A non-abrasive eraser may be used to remove pen and pencil marks.

Air Intake Filter (HP 9040 Only)

Cooling air is drawn through the air intake filter at the bottom of the computer and is exhausted at the top. Ensure that the filter is free of obstructions at all times. Vacuum or wash filter as necessary.

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Chapter 2. Theory of Operation

Theory of Operation

Chapter 2

Introduction

This chapter describes the theory of operation of the computer. Included are functional descriptions of each section of the computer. Figure 2-1 is a functional block diagram of the computer, showing all the functional modules described in this chapter. Figure 2-2 shows how the computer modules are interconnected. It provides cabling information, connector designations, and number of pins per connector.

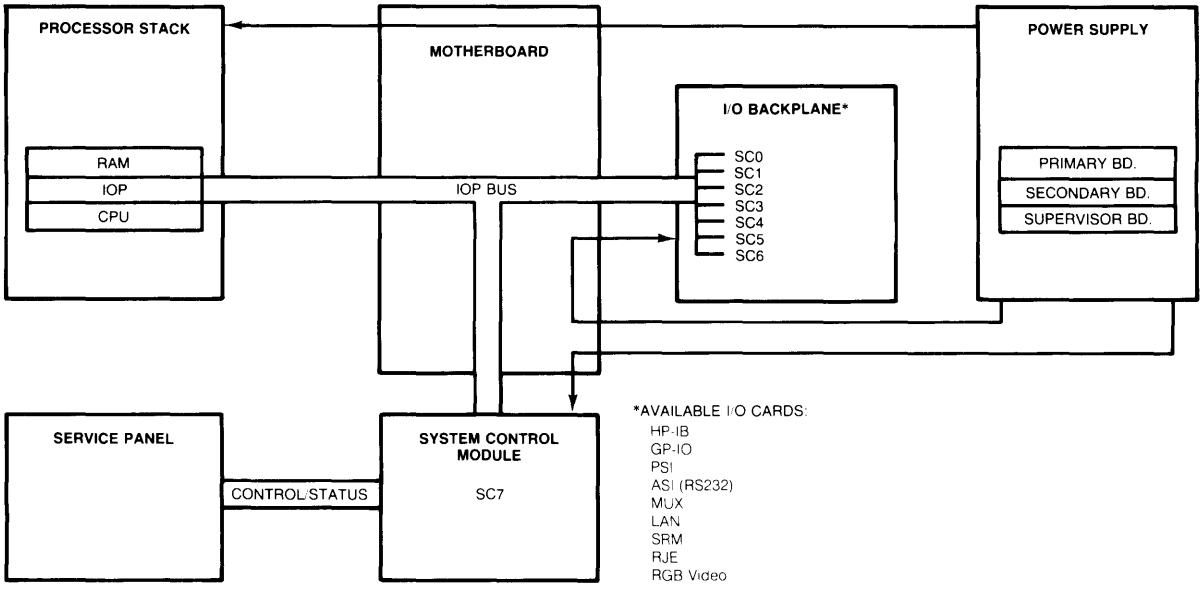


Figure 2-1. Computer Block Diagram

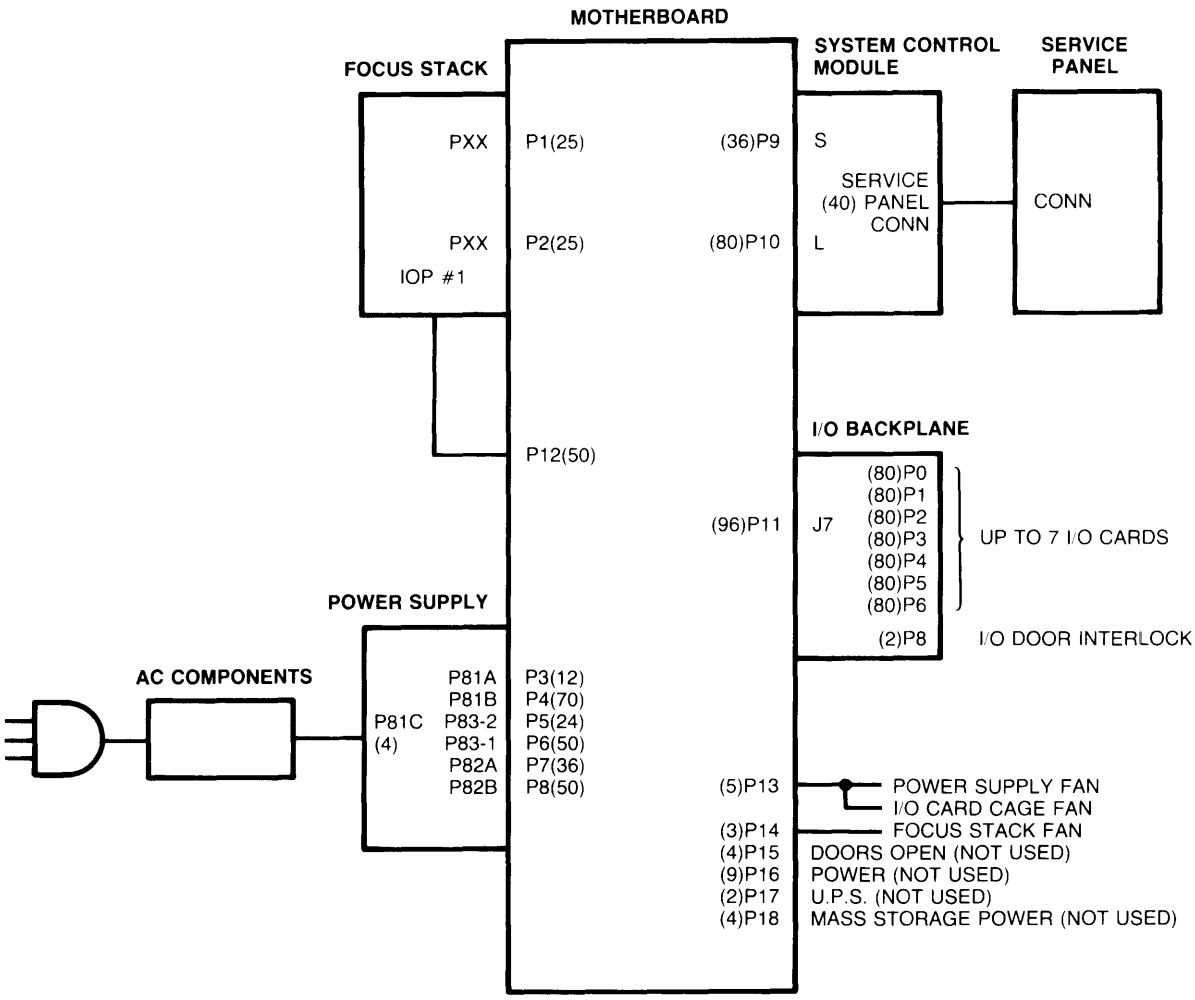


Figure 2-2. Computer Interconnection Diagram

The functional units described in this chapter are as follows:

- Power supply assembly
- Processor stack
- System control module
- Service panel

Power Supply Assembly

WARNING

DO NOT SERVICE THE POWER SUPPLY ASSEMBLY UNTIL THE COMPUTER POWER CORD HAS BEEN UNPLUGGED FROM THE AC OUTLET AND THE POWER SUPPLY CAPACITORS HAVE BEEN COMPLETELY DISCHARGED. SEE CHAPTER 4 FOR ADDITIONAL INFORMATION.

The power supply assembly is a switching regulator assembly that provides power to the entire computer. Figure 2-3 is a functional block diagram of the assembly. The power supply assembly converts ac line voltage to the following dc voltages. The actual voltages are listed first; the voltages in parentheses are the truncated designations used throughout the manual.

+17.5 to +23	(+19 unregulated)
−17.5 to −23	(−19 unregulated)
+16	(+16 bias supply voltage)
+12.1	(+12)
+12.1	(+12MM)
−12.1	(−12)
+6.7	(+6)
+5.1	(+5)
+3.85	(+3)
−2.0	(−2)

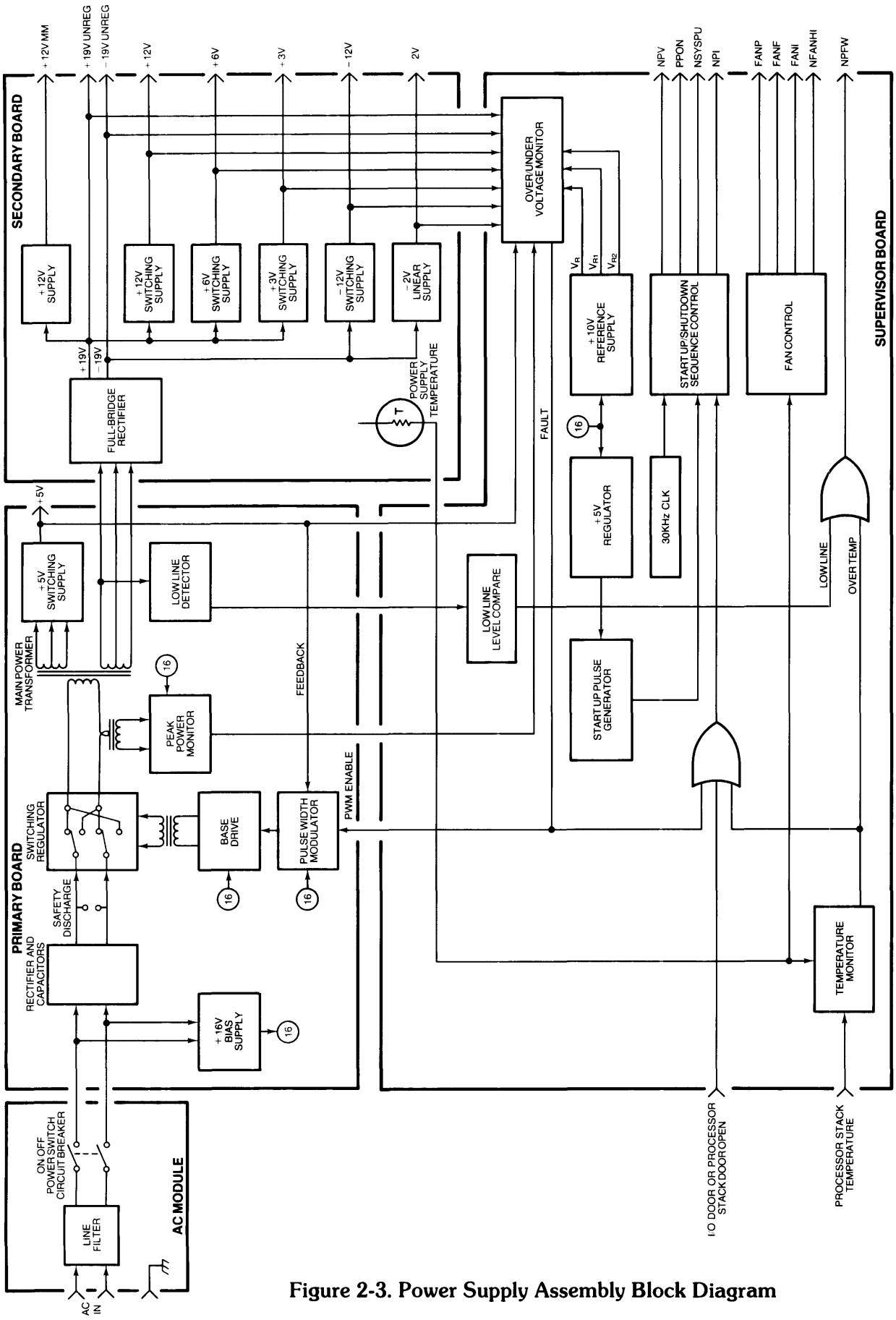


Figure 2-3. Power Supply Assembly Block Diagram

LEDs on the assembly indicate overvoltage or undervoltage conditions for dc supplies, as well as overtemperature, peak power exceeded, and I/O door or processor stack door open.

The ac module consists of an on/off power switch/circuit breaker assembly, line filter, and an attached ac power cord. Interconnection is made with two barrier strips and quick-disconnect terminals. A primary voltage change requires changing the switch assembly, power cord, and cable that interconnects the line filter and power supply.

The power supply assembly is cooled by a dc box fan mounted on the chassis. The fan is not an integral part of the assembly.

The power supply assembly has three printed circuit boards: the primary board, the secondary board, and the supervisor board. The following description is organized according to the functions performed by the ac module and these three boards.

The power supply assembly plugs into the motherboard in the computer base via six connectors, two per board. These connectors, and their associated motherboard traces, interconnect the power supply assembly boards, and carry voltage and signal lines between the power supply assembly and other computer modules.

Fifteen status-indicating, light-emitting diodes (LEDs) are contained on the supervisor board. They are described in a following subsection in this chapter.

Ac Module

The ac module has an attached 6-foot line cord that plugs into an ac outlet. The line filter reduces conducted emissions from the power supply assembly. It also presents the ac voltage to the on/off power switch/circuit breaker which enables/disables ac power to the computer.

The trip point of the circuit breaker depends on which power configuration is being used. The 110V breaker trips at 15 amps line or line overvoltage. The 220V breaker trips at 10 amps. Reset the circuit breaker by turning the switch off and then turning it back on.

Primary Board

After being rectified, the ac to the primary board charges two 2800μfd capacitors. Each capacitor is charged to 150-200V, depending on the line voltage and load.

The rectified dc voltage from the capacitors feeds a switching regulator. The regulator drives current through the main power transformer.

Rectifiers at the output of the main power transformer develop the +5V switching supply. This supply provides +5 volts for use throughout the computer. The +5V output is monitored by the supervisor board for overvoltage and undervoltage. Also, the +5V output feeds the pulse width modulator. The modulator output controls the base drive which in turn controls the switching transistors. The pulse-width-modulator-enable signal (PWM ENABLE) from the supervisor board enables the modulator as long as no fault signal is present. A fault signal disables the modulator, shutting down the power supply assembly.

The main power transformer has another secondary winding that provides ac power to the secondary board. This power is used to generate the unregulated +19V and −19V which in turn generate all the other secondary supplies.

The low line detector circuitry monitors the voltage on the secondary winding of the main power transformer. That voltage is transferred to the supervisor board where it is compared to a reference voltage. If the voltage on the secondary winding drops too low, a power-fail-warning (NPFW) is sent to the processor. This provides a 4 to 8 ms warning before the power is actually shut down by the fault circuitry.

The peak power monitor is a current sense transformer in series with the main power transformer primary winding. Its purpose is to protect the switching transistors from damage due to an excessive power condition. When the current exceeds 9A, the monitor generates a fault signal to shut down the power supply assembly.

A +16V bias supply provides power to various monitor and control circuits throughout the power supply assembly. This supply stays active when the power supply is shut down due to a fault condition. It controls the power supply LEDs and governs power supply start-up.

Secondary Board

Power from the main power transformer on the primary board is transferred via bus bars to the secondary board. There a tapped rectifier converts the raw ac power into unregulated +19V and −19V dc. These voltages in turn operate several switching regulators and one linear regulator. The voltages produced, which are used throughout the computer, are +12V, +12VMM, −12V, +6V, +3V, and −2V. The +6V, +3V, and −2V outputs are used exclusively by the processor stack.

A temperature-sensing thermistor is mounted on the secondary board heat sink. This thermistor is monitored by the supervisor board and controls the power supply fan and the processor stack fan. These two dc box fans operate at three speeds: low, medium, and high.

When the power supply assembly thermistor detects that the temperature of the secondary board heat sink has risen above 39°C, the circuitry steps the fans to medium speed. A further rise of temperature above 51°C causes stepping of the fans to high speed, and the user is notified that the fans have reached their maximum speed. At 97°C, a power fail warning (NPFW) is transmitted, and 4 to 8 ms later the power supply is shut down. The power supply assembly is also shut down if a temperature sensor on the CPU finstrate in the processor stack detects a temperature over 100°C.

When cooling off, the fans step from high to medium speed when the temperature drops below 46°C, and from medium to low speed when the temperature drops below 34°C.

Supervisor Board

The supervisor board contains most of the monitoring, control, and fault-indicating circuitry for the power supply assembly.

The overvoltage and undervoltage monitor checks the voltage outputs of all secondary board power supplies. The monitor also checks the +5V output and the peak power monitor from the primary board. If a fault is detected, the pulse width modulators are disabled, the shutdown sequence is enabled, and the appropriate LEDs are lit.

Temperature monitors check the power supply assembly thermistor, described in preceding paragraphs, and the processor stack thermistor. When the processor stack temperature exceeds 100°C or the power supply temperature exceeds 97°C, this board generates the power fail warning (NPFW) signal and initiates the shutdown sequence.

A +10V reference supply provides the voltage condition references for over and under voltage monitoring and temperature sensing. This supply is enabled by the +16V bias supply from the primary board.

The fan control circuitry provides a constant −10V to the I/O card cage fan (FANI on Figure 2-3) whenever power is on. This fan is not stepped and never changes speed. The fan control circuitry also provides −10V (low speed) to the power supply assembly fan (FANP) and processor stack fan (FANF) as long as the power supply assembly temperature does not exceed 39°C. When the power supply assembly thermistor detects between 39°C and 51°C, the fan control circuitry provides −12V (medium speed) to the two fans. Between 51°C and 97°C, the fans are provided with −14V (high speed). The fan high signal (NFANHI) is also sent to the processor which sends a message to the user, indicating that the computer is performing maximum cooling and that a further temperature increase could result in shutdown.

If either the I/O door or processor stack door is opened while the power supply assembly is operating, the shutdown sequence is initiated.

The start-up/shutdown sequence control circuitry is controlled by a 30-KHz clock. The signals generated by this circuitry are defined as follows:

PPON – Primary Power On; all outputs in specification.

NPV – Not Power Valid; this signal is the inverse of PPON, and therefore signifies "not all outputs in specification".

NPI – Not Pop In; used to reset the processor stack.

NSYSPU – Not System Pop Unsynchronized; used with NPI to cause the processor stack to perform a self-test.

Status LEDs

Four LEDs are contained on the service panel to indicate power supply status. In addition, thirteen LEDs on the top of the power supply can be accessed for additional information if desired. Specific reasons for power supply assembly failure are indicated by the LEDs.

The four service panel LEDs that indicate power supply status are defined as follows:

POWER ON – green; indicates that +5V supply is enabled, that no failures have been detected, and that the supervisor board is enabled and capable of detecting faults and shutting down the power supply assembly.

PS – red; indicates that power is applied to the assembly and +16V bias voltage is available from the primary board, but +5V supply is disabled; an open door or overtemperature condition does not light this LED.

TEMP – red; indicates that processor stack temperature has exceeded 100°C.

DOOR – red; indicates that I/O card cage door or processor stack door is open.

The thirteen LEDs on the top of the power supply assembly are labeled and defined as follows:

DOORS OPEN – same indication as **DOOR** LED on service panel. **OV** also lights.

STACK TEMP – same indication as **TEMP** LED on service panel.

SEC BOARD – indicates that the temperature in the power supply assembly has exceeded 97°C, or the +12V MM power supply has failed.

PWR – indicates that peak primary current exceeded 9A.

OV – used in conjuction with voltage LEDs described below; "on" indicates an overvoltage condition on one or more of the supplies or door open, "off" indicates an undervoltage condition.

−19
−12
−2
3
5
6
12
19

– indicates a fault condition on the applicable supply. If the **OV** LED is also lit, an overvoltage condition is indicated. If the **OV** LED is not lit, an undervoltage condition is indicated.

Processor Stack

The processor stack is a 32-bit computer system that controls all computer operations. The stack consists of an enclosing and supporting case, up to 12 boards, stack motherboard, and clock board. The boards may be either finstrates or polystrates.

Finstrates are copper-cored cards with NMOS-III chips bonded to them. Finstrates provide the combined functions of cooling fins and ceramic substrates.

Polystrates (from **poly**imide and fin**strate**) are polyimide boards without the copper core. However, copper heat sinks are mounted on the circuit side of the board, to dissipate heat from the chips.

All boards plug into the common Memory Processor Bus (MPB), provided on the motherboard (Figure 2-4).

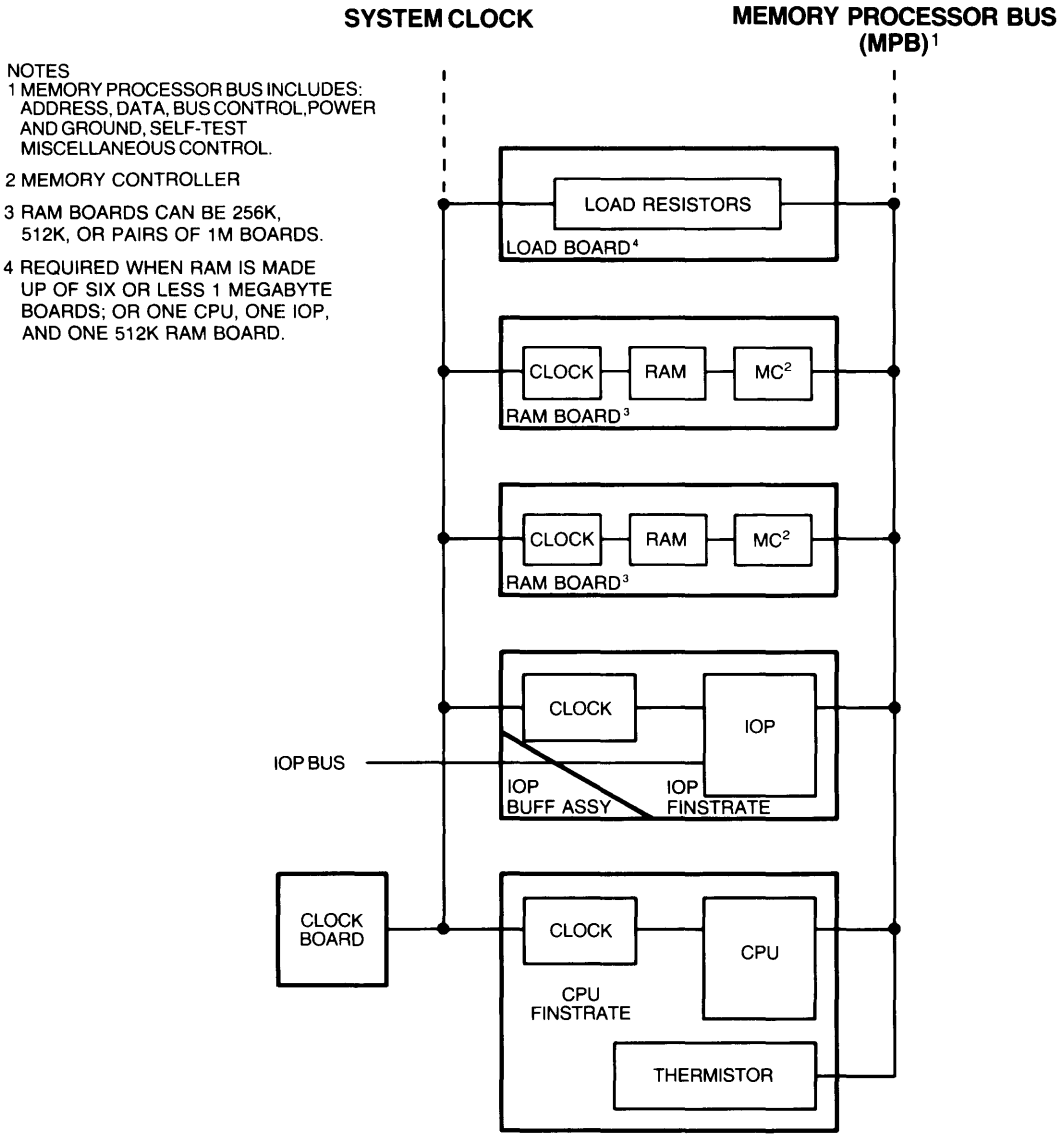


Figure 2-4. Processor Stack Block Diagram

The case has a door which can be opened to provide access to the upper 9 slots or removed to provide access to all 12 slots. A dc box fan attached to one end of the stack provides cooling air to the boards.

The stack interconnects with the computer motherboard via two 25-pin connectors and a 50-conductor input/output processor (IOP) cable. The 25-pin connectors on the bottom of the stack interconnect with connectors on the computer motherboard when the stack is positioned in the computer. These connectors provide power and control signals and send self-test information to the system control module (SCM). The internal IOP ribbon cable connects the motherboard to the IOP board in slot #2. Additional IOP cables interconnect IOP boards and the computer rear panel.

Stack Configurations

The stack has 12 slots numbered from 1 to 12, with slot #1 the bottom slot and slot #12 the top. All slots are interconnected by the memory processor bus via the stack motherboard. The memory processor bus (MPB), which has 32 data/address lines and 12 control lines, interconnects all boards to the IOP board(s). The IOP board in slot #2 is connected to the internal IOP cable which is routed to the motherboard.

Four types of boards can be used in the stack: central processor unit (CPU), input/output processor (IOP), and random access memory (RAM). A load board may also be required, depending on stack configuration. All are described in following paragraphs.

The stack can be configured with various combinations of boards. One or two CPU boards can be added. One or two IOP boards can be added. Any number of RAM boards are allowed. However, if 1 Megabyte RAM boards are used, they must be used in pairs.

The following rules must be observed for all configurations:

- Slot #1 must always contain a CPU card.
- Slot #2 must always contain an IOP card.
- If there is one additional IOP board, it must be in slot #3. If there are two additional IOP boards, they must be in slots #3 and #4.
- No empty slot is permitted between two finstrates.
- 1 Megabyte RAM boards must be used in pairs (2, 4, 6, 8, or 10).
- A load board must be used in the top occupied slot (adjacent to the RAM boards) any time the stack configuration is:
  a. One CPU, one IOP, and one 512K RAM card.
  b. RAM is composed of all 1 Megabyte RAM boards and there are less than 6 RAM boards. (The load board is not required if other types of RAM are included in the stack,or there are more than six 1 Megabyte RAM cards in the stack.)

Minimum and maximum configurations are as follows:

Finstrate	Minimum	Maximum*
CPU	1	3
IOP	1	3
RAM	2	10

* Maximum of 12 finstrates per stack.

Stack Boards

Board types and functions are described in the following paragraphs. Each board has a self-test that runs on powerup or system reset. Self-tests are described in Chapter 3.

CPU Board

Two types of CPU board perform all the central processing for the computer. The first type of CPU contains a clock buffer and a CPU chip. All CPU microcode, and the hardware to decode and execute instructions, are included in the CPU chip.

The second type of CPU board contains an additional three math chips (add/subtract, multiply, and divide) to provide floating point, 32 bit or 64 bit, double precision math solutions. The CPU sends control information and data to the math chip registers. The answer is returned to the CPU a few computer states later. These math chips are invisible to the operating system.

IOP Board

The IOP board performs I/O processing and drives the I/O bus. The IOP board actually consists of two parts: the board assembly itself and an attached buffer printed circuit board. The buffer pc board is attached to the IOP board by a 50-pin connector. Clamps and screws ensure a solid physical connection.

The clock buffer and the I/O processor chip are on the IOP board. The buffer pc board contains the five bi-directional buffer TTL packages that drive the I/O bus. The buffer pc board also contains several resistor packages and a transistor package. The resistor paks terminate the I/O bus and its characteristic impedance. The transistor pak holds the reset signal on the I/O bus during a power-up and power-down sequence.

RAM Board

There are three types of RAM boards available for use in the stack. They can be installed in any combination, but the 1 Megabyte boards must be used in pairs. The 256K byte RAM is a finstrate. The 512K byte boards and 1 megabyte RAM boards are polystrates. Each board has a memory controller, RAM chips, and clock buffers.

Load Board

The Load Board consists of load resistors to ensure the correct power supply load for certain stack configurations. The load board will be used when:

- The stack consists of one CPU, one IOP, and one 512K RAM board.
- The stack consists of one CPU, one IOP, and six or less 1 Megabyte RAM boards.

Stack Motherboard

The stack motherboard interconnects the 12 board slots via the memory processor bus. The two 25-pin connectors at the bottom of the stack provide power and some control signals to the stack motherboard.

Clock Board

The clock board provides clock signals to the processor. This board electrically interconnects to the stack motherboard via a 9-pin connector. The clock board attaches to the stack motherboard with two screws.

Power Interlock Switch

A power interlock microswitch causes power supply shutdown if the stack door is opened with power on. Shutdown results in all RAM data being lost. The power switch must be cycled to power up the computer. The power interlock switch prevents damage to boards caused by their removal or insertion with power on, and prevents a shock hazard to personnel.

Cooling

A dc box fan is mounted at one end of the stack to draw cooling air through the stack. An air controller is mounted in the stack. The air controller blocks air from circulating through the open area if the stack is not filled with boards and ensures that most of the cooling air is circulated between the boards.

The fan has three speeds that are varied according to the temperature sensed on the secondary board heat sink in the power supply assembly. Refer to the preceding Power Supply Assembly description for details on fan speeds and temperature thresholds.

Memory

This subsection describes the organization of RAM memory within the stack. It also describes error detection and correction, mapping, and healing.

Memory Organization - 256K Byte RAM Board

Up to 10 RAM boards can be configured in a processor stack. Each board has a Memory Controller (MC) and 256K, 512K, or 1 Megabyte of RAM. This section will cover the theory of operation of the 256K board (Figure 2-5), and following sections will cover the other RAM boards.

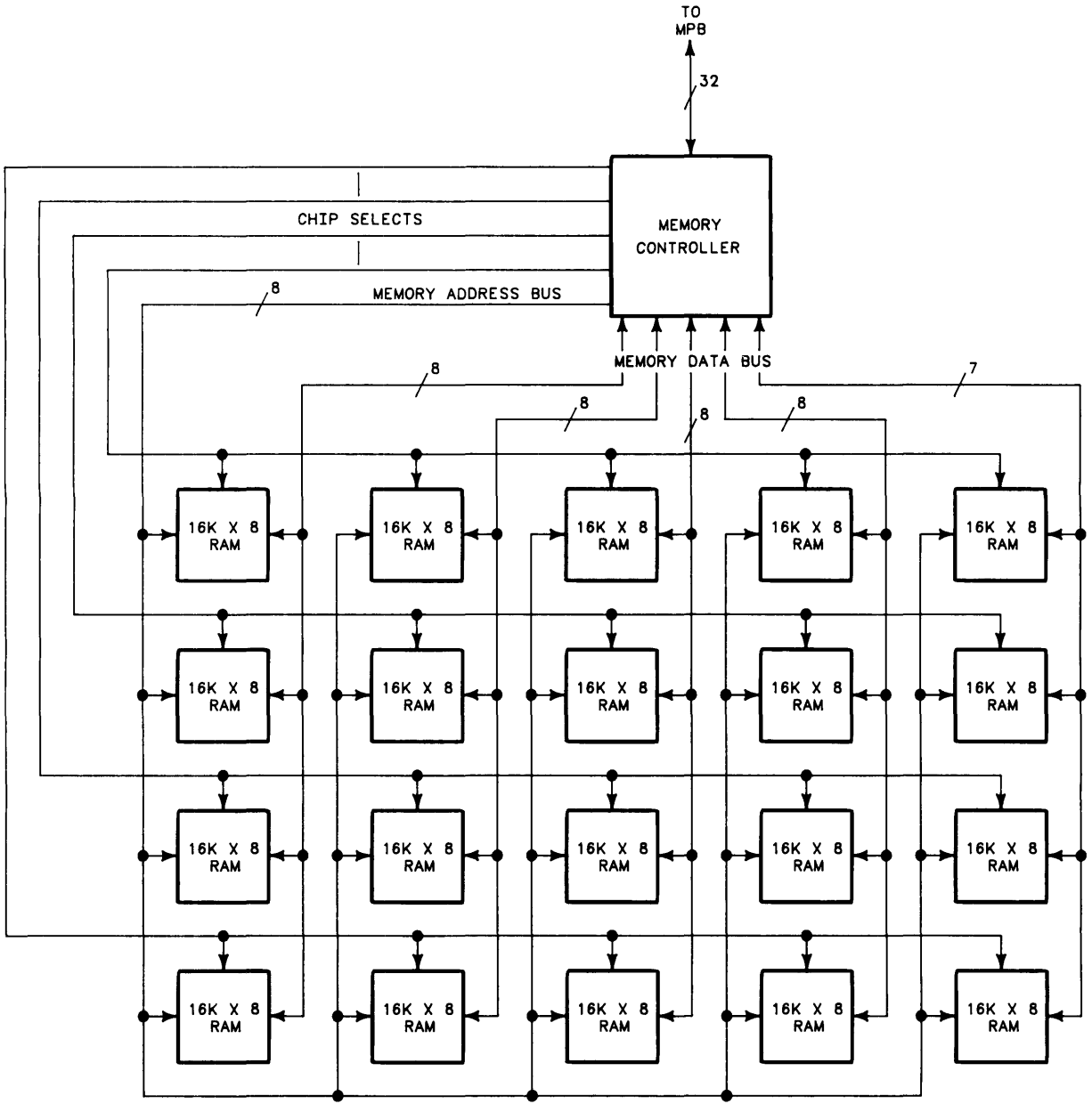


Figure 2-5. 256K RAM Finstate Block Diagram

The MC interfaces the memory on the RAM board to the MPB. The MC uses 27 bits of the MPB logical address to locate the physical memory address on the RAM board. 12 bits of the MPB address are used as part of the X and Y addresses. The other 15 bits select a mapper Content-Addressable Memory (CAM) register. The mapper CAM register output is used to provide Chip Select (CS) lines and 3 more Y address bits for block selection. One of four chip select lines selects one of four rows of RAM. Each row of RAM has four 4K word blocks of memory, for a total of 16K words (four 8 bit bytes per word). The row is actually comprised of five 16K by 8 bit RAM chips. Each word has 32 data bits and 7 checkbits for error detection and correction. Data and check bits are transmitted on the Memory Data Bus.

The 8-line Memory Address Bus multiplexes 15 address bits. The lower 8 bits comprise the X address and are transmitted from the MC first. The next 7 bits make up the Y address and are transmitted next. The most significant bit of the Y address is ignored in the RAM.

Memory Mapping

The Memory Controller has a memory mapping capability which provides a translation of logical addresses on the MPB to physical addresses in RAM. Mapping memory addresses from the logical address space of the MPB to the physical address space of the memory itself allows each MC to respond to only those addresses of memory under its control. It also allows logical addresses to be independent of physical addresses. The MC has 32 mapper CAM registers. Each register is associated with one 4K block of RAM.

Each row of memory is logically divided into four blocks of 4K words per block, 32-bits per word (Figure 2-6). Thus selecting a mapper CAM register selects a particular block of 4K words. The X and Y address bits then select a particular word in the block. Because the 256K byte RAM board has 64K words, only 16 mapper CAM registers are used. As shown in Figure 2-6, the registers that are used are 0-3, 8-11, 16-19, and 24-27. The remaining registers (4-7, 12-15, 20-23, and 28-31) are not used and their Map Out bits (bit 0) should be set. The Map Out bit is described in a following paragraph.

MAPPER CAM REGISTER ADDRESS	CS SELECTED ROW	Y ADDRESS SELECTED BLOCK NUMBER	X AND Y ADDRESS SELECTS WORD WITHIN THE BLOCK				
0	3	0	4K WORDS	4K BYTES	4K BYTES	4K BYTES	4K BYTES
1	3	1	4K WORDS	4K BYTES	4K BYTES	4K BYTES	4K BYTES
2	3	2	4K WORDS	4K BYTES	4K BYTES	4K BYTES	4K BYTES
3	3	3	4K WORDS	4K BYTES	4K BYTES	4K BYTES	4K BYTES
4			NOT USED				
5							
6							
7							
8	2	0	4K WORDS	16K BYTE RAM	16K BYTE RAM	16K BYTE RAM	16K BYTE RAM
9		1	4K WORDS				
10		2	4K WORDS				
11		3	4K WORDS				
12			NOT USED				
13							
14							
15							
16	1	0	4K WORDS	16K BYTE RAM	16K BYTE RAM	16K BYTE RAM	16K BYTE RAM
17		1	4K WORDS				
18		2	4K WORDS				
19		3	4K WORDS				
20			NOT USED				
21							
22							
23							
24	0	0	4K WORDS	16K BYTE RAM	16K BYTE RAM	16K BYTE RAM	16K BYTE RAM
25		1	4K WORDS				
26		2	4K WORDS				
27		3	4K WORDS				
28			NOT USED				
29							
30							
31							

Figure 2-6. 256K Memory Mapping Organization

The 32-bit memory address word on the MPB is shown in Figure 2-7. Bits 0-2 contain the function code, and bits 30 and 31 are used for half-word and byte modes, respectively. Bits 3-29 are the 27 bits that specify the logical memory address. The least significant 12 bits of the incoming address are not mapped. These point to individual locations within the 4K blocks. Eight of the 12 bits (MPB bits 22-29) comprise th X address. The remaining four bits (MPB bits 18-21) comprise bits 4-7 of the Y address. The 15 most significant bits are gated into the MC address mapper.

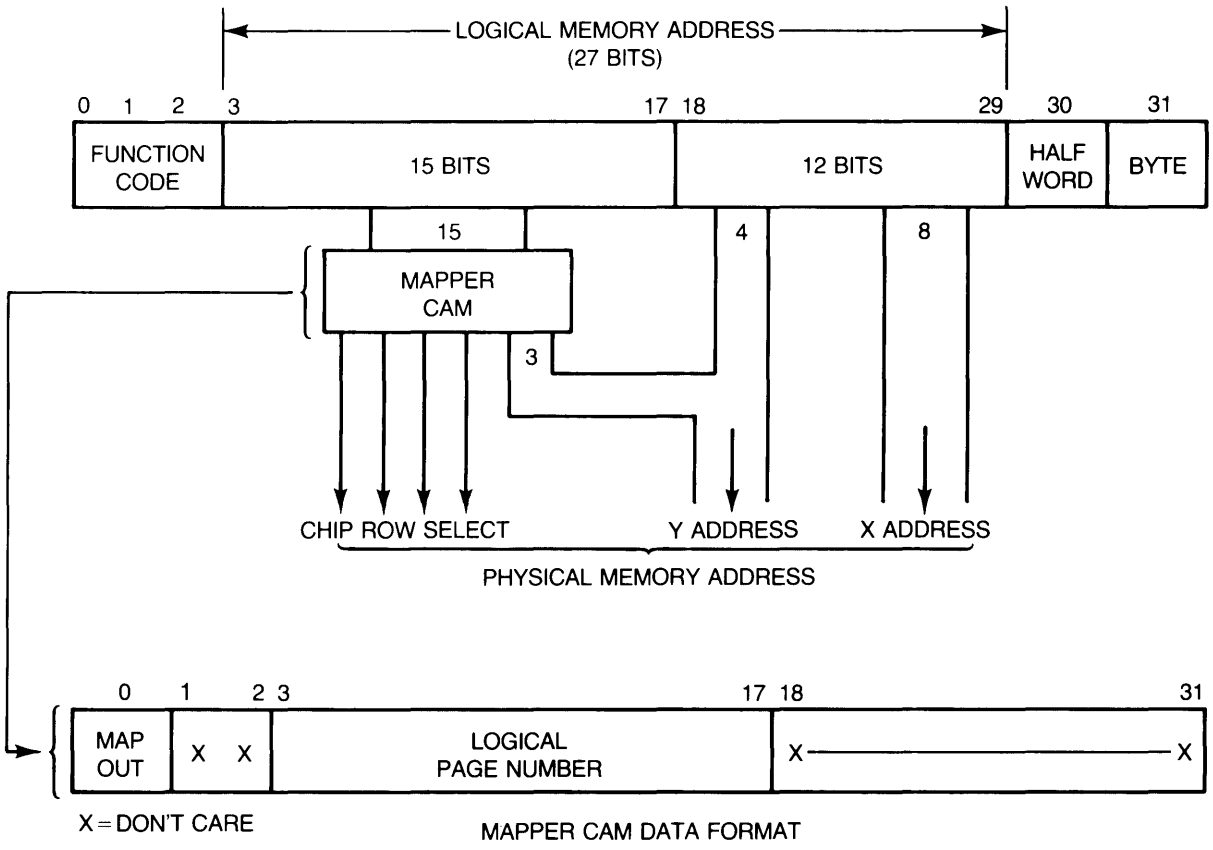


Figure 2-7. 256K Memory Mapping Operation

Bits 3-17 of the MPB logical memory address are compared with bits 3-17 of each mapper CAM register in the MC address mapper. If the compare is unsuccessful, nothing happens. If a compare is successful, bit 0 of the register is then checked. If bit 0 (the map out bit) is set, the addressed RAM block is considered nonexistent and cannot be accessed. This allows defective memory blocks to be removed from use and assures that no logical address will be mapped onto an empty block of memory.

If an address compare occurs and the mapper CAM register map out bit is clear, the MC produces a 19-bit physical memory address. The address mapper sets one of four chip select lines to select one of four chip rows. It also outputs three bits which are joined with MPB bits 18-21 to form the 7-bit Y address. MPB bits 22-29 are gated in as the 8-bit X address. The most significant bit of the Y address is not used. The next two bits select the 1-of-4 block number. The lower four bits of the Y address and the eight X address bits select one of 4K words in the block.

Error Detection and Correction

The memory controller detects and corrects single-bit errors in data read from RAM. It also detects double-bit errors. Each 32-bit word written to memory has a 7-bit Hamming code attached to it. When the data word is read, any single-bit or double-bit error is detected.

Any single-bit error that is detected is automatically corrected before the word is transferred to the MPB. No additional time is required for the correction. At the same time that a single-bit error is detected and corrected, the corrected data word is written into a healer location. Subsequent accesses of that location are to the healer location rather than to the memory location.

A double-bit error is detected but not corrected. A double-bit error causes the system to halt, preventing continuation of a program with bad data.

Healing is described in the following paragraphs.

Memory Healing

Each memory controller contains 32 words of CAM and 32 words of RAM which are used to replace up to 32 failed memory words (Figure 2-8). The physical address of a failed word is put in the healer CAM, the corrected data is placed in the corresponding healer RAM location, and bit 0 in the CAM is set to enable the address to match. Subsequent accesses to this physical address are to the healer RAM instead of the failed memory, causing the healer word to replace the failed word. Healing in no way affects the timing of the memory operation. Except for the healer, no record of healing is stored in memory.

All mapped addresses are sent to the healer CAM which compares each mapped address to all addresses of failed locations. Healer CAM addresses of failed locations have bit 0 set.

When all 32 locations of the healer are full, no further healing or automatic changes to the healer CAM occur on that memory controller. When all healer locations have been used, the healer overflow bit in the MC status register is set.

When all healer locations are full, the operating system checks each healed location to determine if the location is still faulty. If the location fault was caused by a momentary failure, the overflowed CAM can be cleared and reused by the operating system.

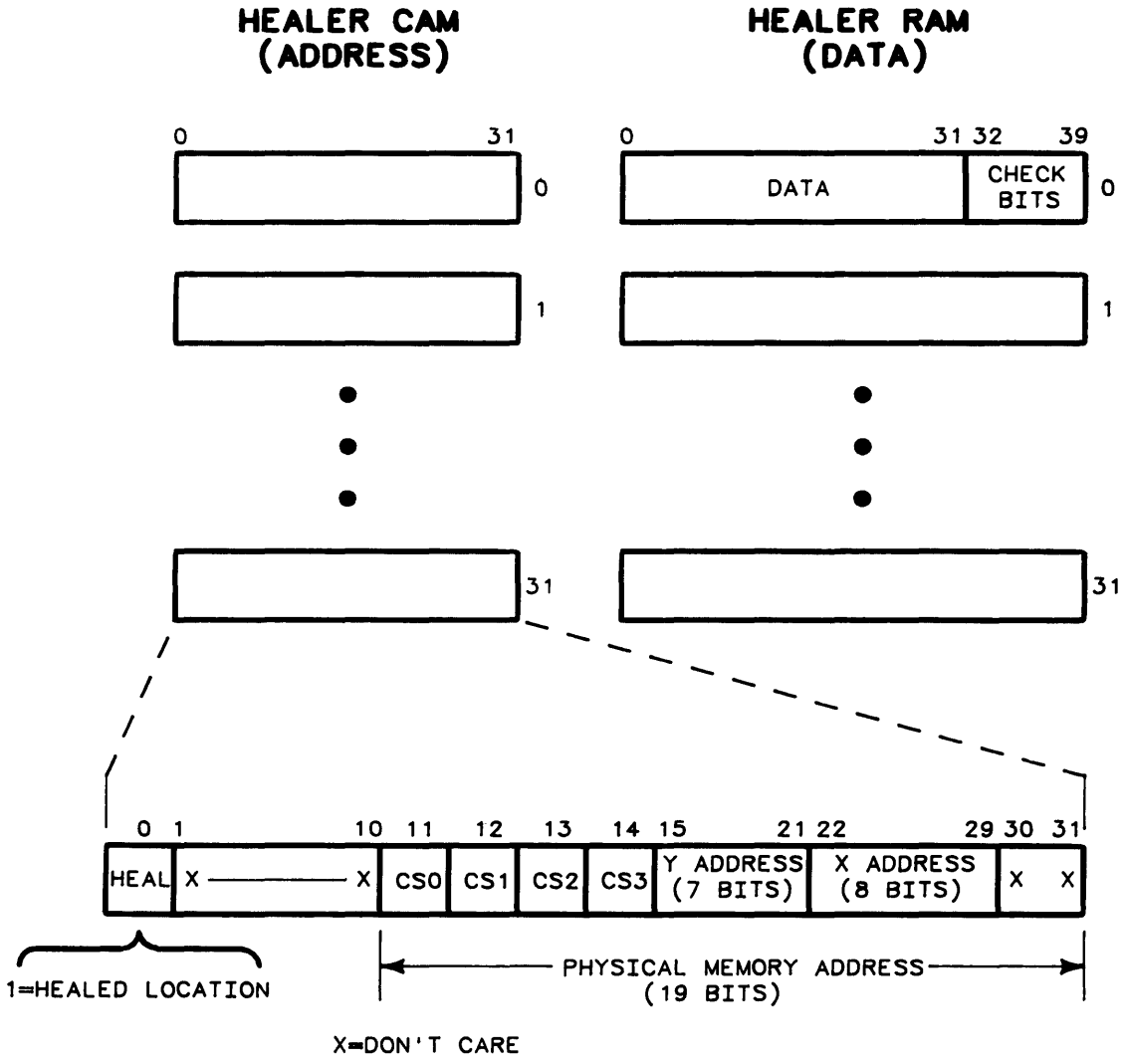


Figure 2-8. 256K Memory Healing

Memory Organization - 512K Byte RAM Board

The 512K RAM board is similar to the 256K RAM finstrate. The board itself is a polyimide board instead of a finstrate. It contains twice as many RAM chips on the board as the 256K RAM board (Figure 2-9). The RAM chips are the same as used on the 256K byte board.

The MC on the RAM board develops eight chip select lines, four even and four odd chip select lines. Each chip select line selects one row of 16K word RAM (note that a chip select line in Figure 2-9 goes to every other chip in each row. The effect is for a five chip row instead of ten chips, and the chip select goes to either the odd numbered chips or the even numbered chips.) Each word is still 32 data bits and 7 check bits, and the specific word that is addressed is selected within the block, by the X and Y address bits.

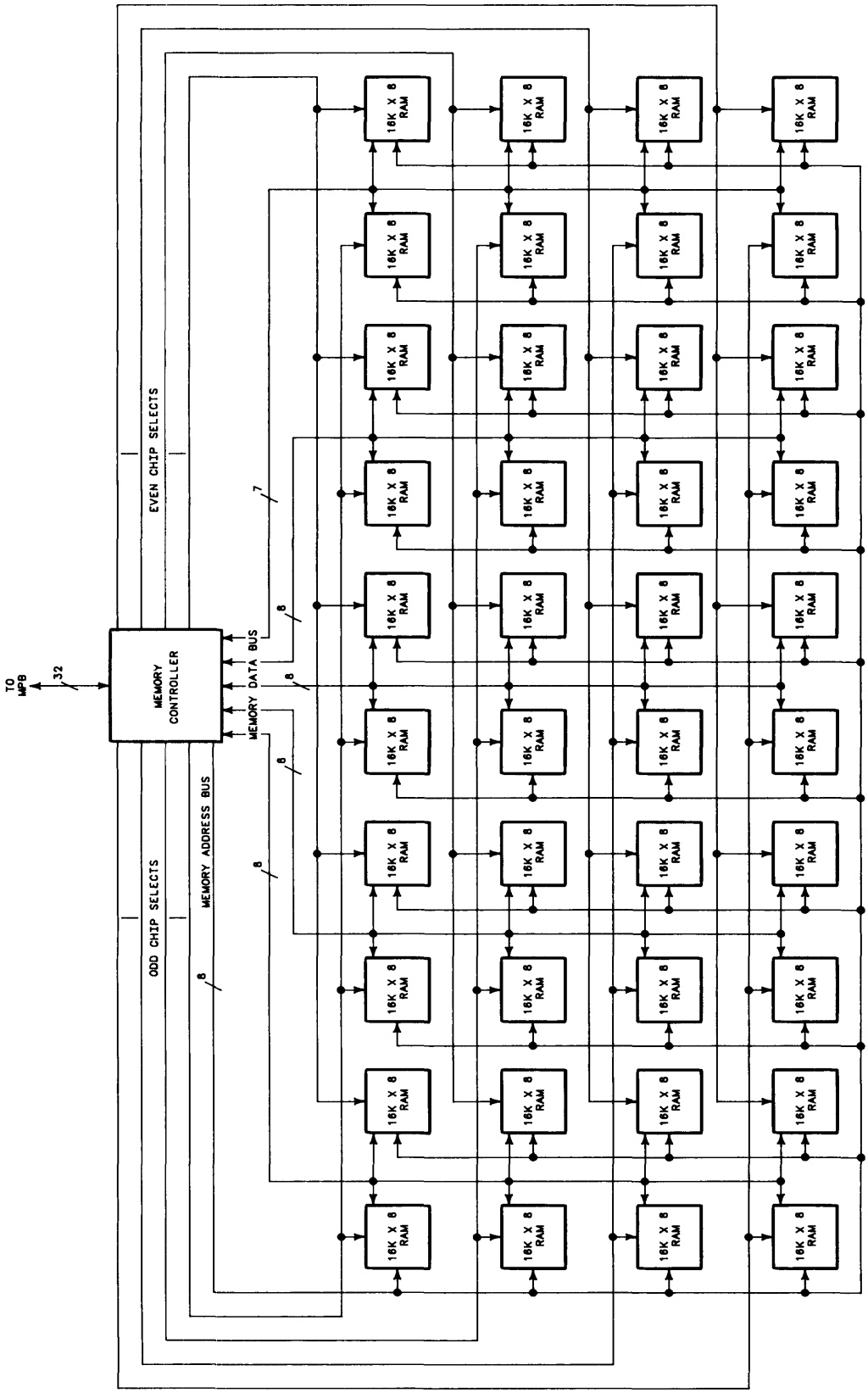


Figure 2-9. 512K RAM Board Block Diagram

Memory Mapping

The Memory Controller has the same memory mapping capability of translating logical addresses on the MPB to physical addresses in RAM as the 256K RAM Memory Controller. The difference is in the number of mapper CAM registers that are used to produce Chip Select signals for row selection, and the use of the most significant Y bit for determining whether the row is odd or even.

The 256K RAM used 16 of the 32 mapper CAM registers to produce chip select lines for selecting rows. The 512K RAM uses all 32 mapper CAM registers for selecting 8 rows instead of 4 rows (Figure 2-10). This is accomplished by multiplexing the Chip Select output of the mapper CAM, and using the most significant bit of the Y address to determine whether the multiplexed output is an odd numbered row or an even numbered row (Figure 2-11). The RAM chips still do not use the most significant bit of the Y address. It is only used by the multiplexer inside the Memory Controller.

MAPPER CAM REGISTER ADDRESS	CS SELECTED ROW	Y ADDRESS SELECTED BLOCK NUMBER	X AND Y ADDRESS SELECTS WORD WITHIN THE BLOCK				
0	7	0	4K WORDS	4K BYTES	4K BYTES	4K BYTES	4K BYTES
1	7	1	4K WORDS	4K BYTES	4K BYTES	4K BYTES	4K BYTES
2	7	2	4K WORDS	4K BYTES	4K BYTES	4K BYTES	4K BYTES
3	7	3	4K WORDS	4K BYTES	4K BYTES	4K BYTES	4K BYTES
4	6	0	4K WORDS	16K BYTE RAM	16K BYTE RAM	16K BYTE RAM	16K BYTE RAM
5		1	4K WORDS				
6		2	4K WORDS				
7		3	4K WORDS				
8	5	0	4K WORDS	16K BYTE RAM	16K BYTE RAM	16K BYTE RAM	16K BYTE RAM
9		1	4K WORDS				
10		2	4K WORDS				
11		3	4K WORDS				
12	4	0	4K WORDS	16K BYTE RAM	16K BYTE RAM	16K BYTE RAM	16K BYTE RAM
13		1	4K WORDS				
14		2	4K WORDS				
15		3	4K WORDS				
16	3	0	4K WORDS	16K BYTE RAM	16K BYTE RAM	16K BYTE RAM	16K BYTE RAM
17		1	4K WORDS				
18		2	4K WORDS				
19		3	4K WORDS				
20	2	0	4K WORDS	16K BYTE RAM	16K BYTE RAM	16K BYTE RAM	16K BYTE RAM
21		1	4K WORDS				
22		2	4K WORDS				
23		3	4K WORDS				
24	1	0	4K WORDS	16K BYTE RAM	16K BYTE RAM	16K BYTE RAM	16K BYTE RAM
25		1	4K WORDS				
26		2	4K WORDS				
27		3	4K WORDS				
28	0	0	4K WORDS	16K BYTE RAM	16K BYTE RAM	16K BYTE RAM	16K BYTE RAM
29		1	4K WORDS				
30		2	4K WORDS				
31		3	4K WORDS				

Figure 2-10. 512K Memory Mapping Organization

As in the 256K RAM, the MC uses 27 bits of the MPB logical address to locate the physical memory address on the RAM board (Figure 2-11). 12 bits of the MPB address are used as part of the X and Y addresses. The other 15 bits select a mapper Content-Addressable Memory (CAM) register. The mapper CAM register output is used to provide Chip Select (CS) lines and 3 more Y address bits for block selection. One of four chip select lines is input to the multiplexer where it is further modified by the most significant bit of the Y address to select one of four rows of odd, or one of four rows of even numbered RAM. Each row of RAM has four 4K word blocks of memory, for a total of 16K words (four 8 bit bytes per word). The row is actually comprised of five 16K by 8 bit RAM chips. Each word has 32 data bits and 7 check bits for error detection and correction. Data and check bits are transmitted on the Memory Data Bus.

The 8-line Memory Address Bus multiplexes 15 address bits. The lower 8 bits comprise the X address and are transmitted from the MC first. The next 7 bits make up the Y address and are transmitted next.

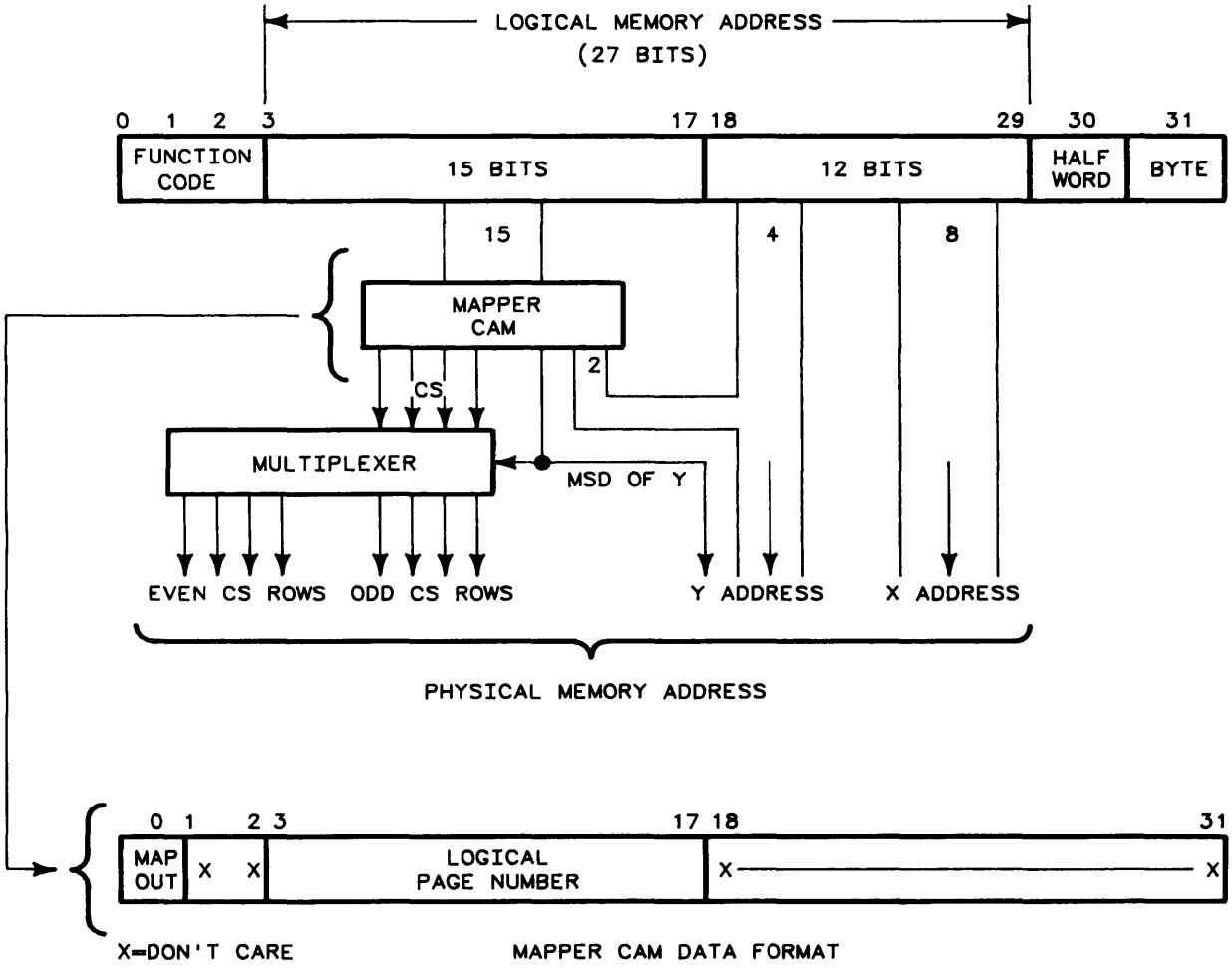


Figure 2-11. 512K Memory Mapping Operation

Error Detection, Correction, and Memory Healing

Error detection and correction is the same for the 256K RAM and the 512K RAM. The only differences are in the physical memory address in the healer CAM. The chip select portion of the address uses eight chip select lines instead of four (Figure 2-12).

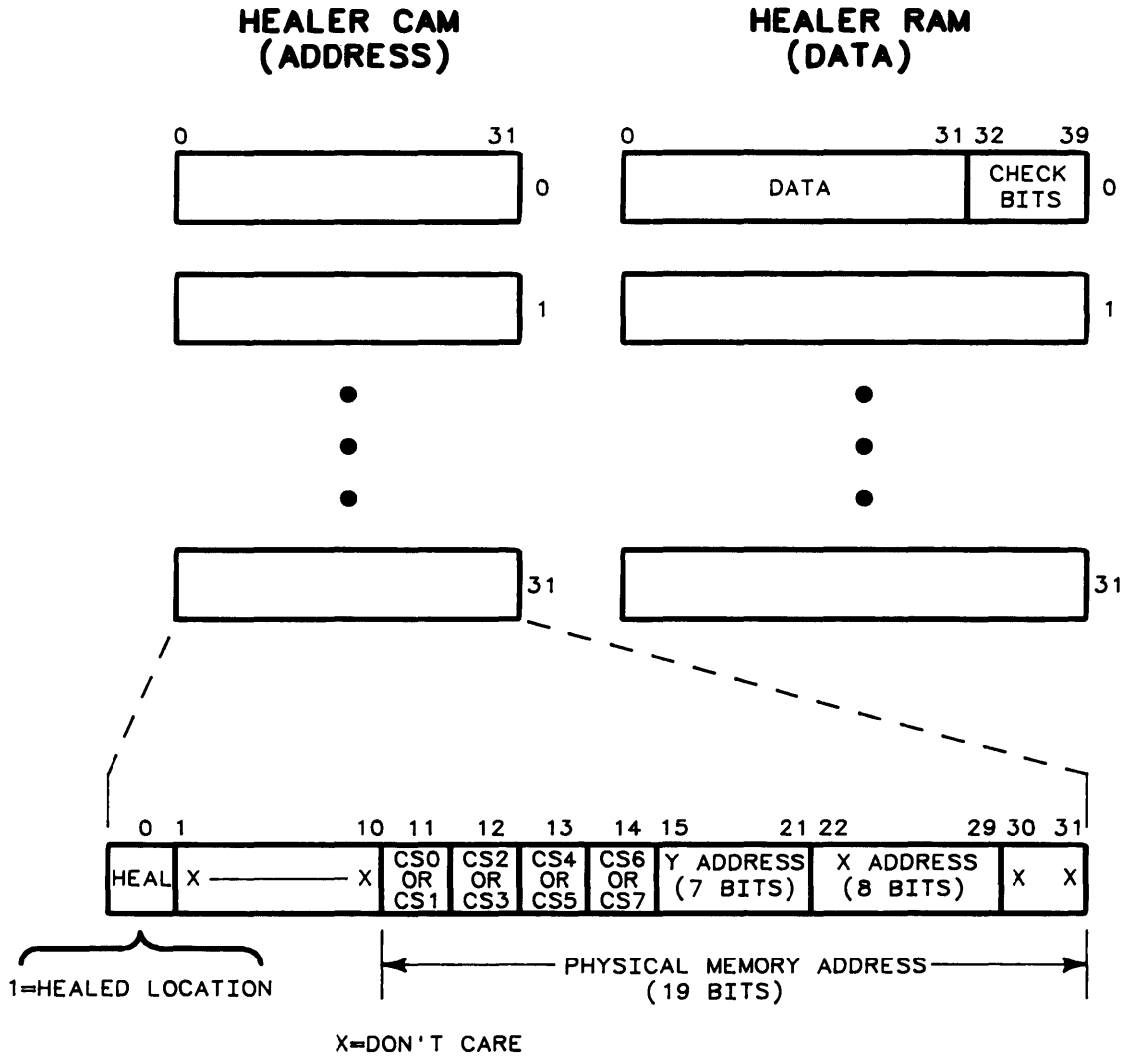


Figure 2-12. 512K Memory Healing

Memory Organization - 1 Megabyte RAM Board

The 1 Megabyte RAM board is a polyimide board which uses thirty-nine 256K by 1 bit chips. This allows an organization consisting of 256K words (four bytes per word) which can be addressed without the use of chip select lines, or "blocks" of RAM (Figure 2-13). The word stored in the RAM is 32 bits in length with 7 check bits.

The MC on the RAM board develops eighteen physical address bits from the logical address bits on the MPB, nine X address bits and nine Y address bits. The multiplexed physical addresses are routed to each chip by the Memory Address Bus. The X address is output first, with the the Y address following. Three control lines go to each RAM chip: Row Address Select (NRAS) - X address, Column Address Select (NCAS) - Y address, and Read/Write status (NRW).

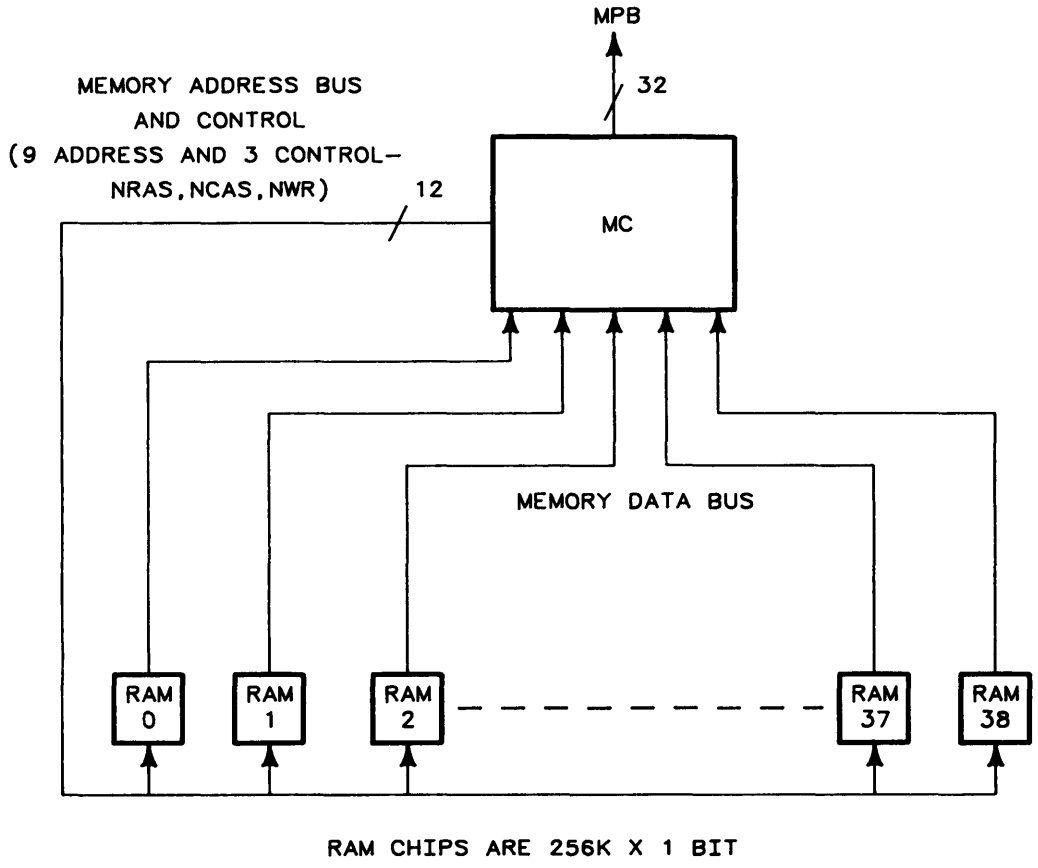


Figure 2-13. 1 Megabyte Memory Organization

Memory Mapping

The Memory Controller, as on other RAM boards, has the memory mapping capability of translating logical addresses on the MPB to physical addresses in RAM. The difference is the controller output (Figure 2-14). There is only one mapper Cam on the 1 Megabyte board. The mapper CAM uses bit zero for the Map Out bit to indicate whether the memory card is capable of storing data or is mapped out. Bits 3 through 11 are used for determining whether this 1 Megabyte board is being addressed by the logical memory on the MPB. If the MPB logical address bits 3 to 11 match the bits in the mapper CAM, the operational transaction is for this board. As all memory chips are addressed without the requirement for Chip Select signals or block addressing, the nine bits of X, and the nine bits of Y address are all that are required to locate the desired information in the RAM chips. The MC controls when the chips are addressed by output of the NRAS and NCAS control signals, along with the output of the X or Y address on the Memory Address Bus.

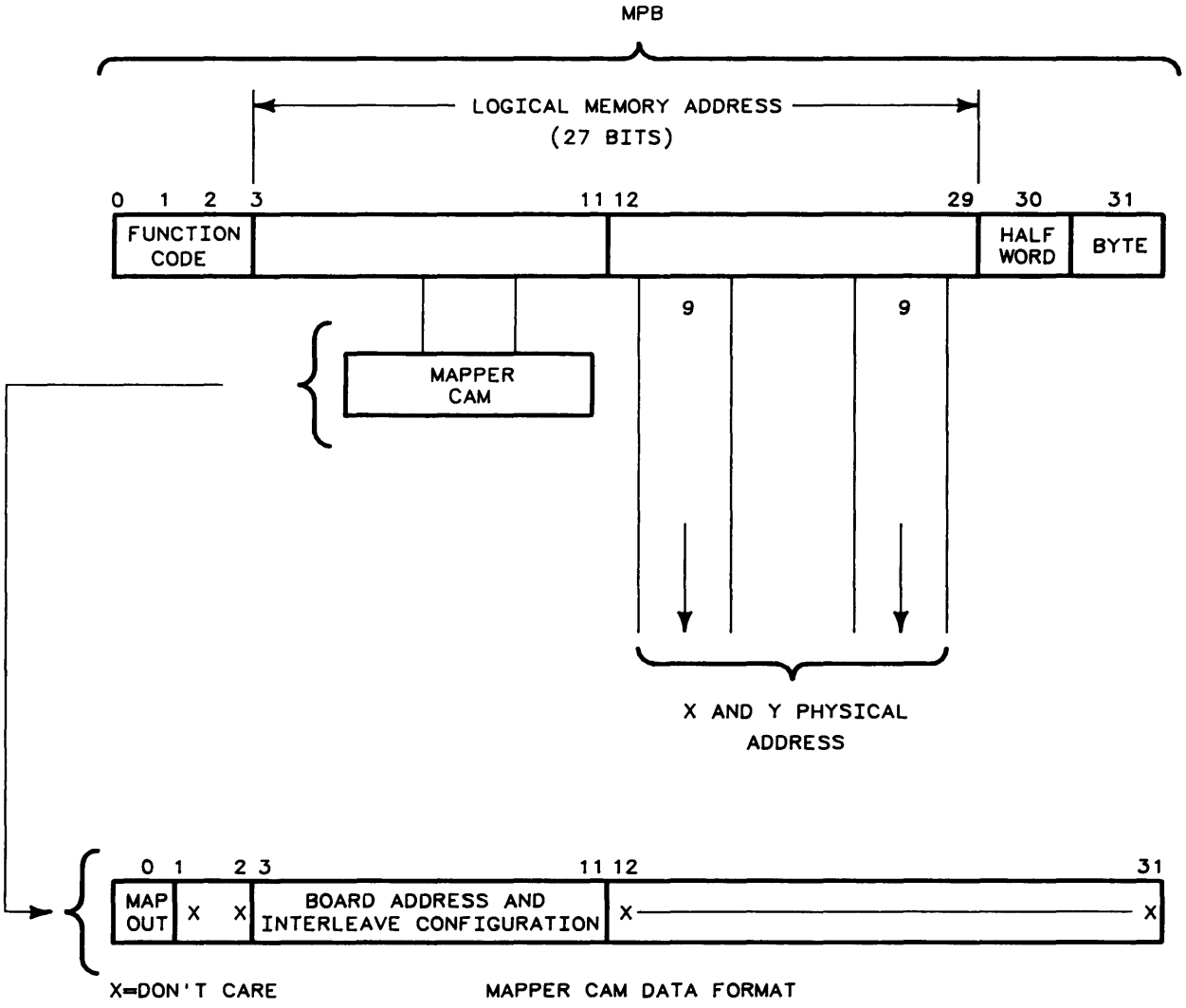


Figure 2-14. 1 Megabyte Memory Mapping Operation

When using the 1 Megabyte RAM boards, a unique feature is employed. The Ram boards are interleaved for better efficiency in memory access. This interleaving means that consecutive addresses are found on different 1 Megabyte boards. Interleaving can be between 2, 4, or eight boards. Whenever 1 Megabyte boards are used they will be used in pairs so this feature can be utilized to its best advantage. The stack can support up to ten 1 Megabyte boards and the appropriate interleave method for each configuration will be implemented automatically. If two boards are used, all the odd numbered addresses are on one board and the even numbered addresses are on the other board. Consecutive addresses will alternate between the boards. If four boards are used, consecutive addresses move from one board to the next. For example: address 0 may be on board one; address 1 on board two; address 2 on board three; address 3 on board four; and address 4 on board one; etc. It is not necessary to change anything on the boards, as the operating system automatically controls the set-up of interleaving for the best operation of the computer regardless of the number of RAM boards or the mixture of 256K, 512K, or 1 Megabyte boards. Mapper CAM data bits 9, 10, and 11 are used to ensure that the mapper CAM responds to the correct interleave method implemented by the operating system.

Even with the interleaving, the program speed of the 1 Megabyte RAM boards may be slightly slower on some programs, when compared to the program speed using the 256K or 512K RAM boards. This is due to the slower access time of the 1 Megabyte RAM boards.

Error Detection and Correction

As in the other memory boards, the Memory Controller detects and corrects single bit errors in data read from RAM. It also detects double bit errors. Each 32 bit word written to memory has a 7 bit Hamming code attached to it. When the data word is read, a single bit or double bit error is detected.

Any single bit error that is detected is automatically corrected before the word is transferred to the MPB. No additional time is required for the correction. At the same time that a single bit error is detected and corrected, the correct data is written into a healer location.

A double bit error is detected but not corrected. A double bit error causes the system to halt, preventing continuation of a program with bad data.

Memory Healing

Each Memory Controller contains 32 words each of CAM and RAM which are used to replace up to 32 failed memory words (Figure 2-15). The physical address of a failed word is put in the healer CAM, and the corrected data is put in the corresponding healer RAM location. Bit 0 in the CAM is set to enable the address to be matched. Subsequent accesses to this physical address are to the healer RAM instead of the failed memory, causing the healer word to replace the failed word. Healing does not affect the timing of the memory operation. Except for the healer, no record of healing is stored in memory.

All mapped addresses are sent to the healer CAM, which compares each mapped address to all addresses of failed locations. Healer CAM addresses of failed locations have bit 0 set.

When all 32 locations of the healer are full, no further healing or automatic changes to the healer CAM occur on that Memory Controller. When all healer locations have been used, the healer overflow bit in the MC status register is set. When all healer locations are full, the operating system checks each healed location to determine if the location is still faulty. If the location fault was caused by a momentary failure, the overflowed CAM can be cleared and reused by the operating system.

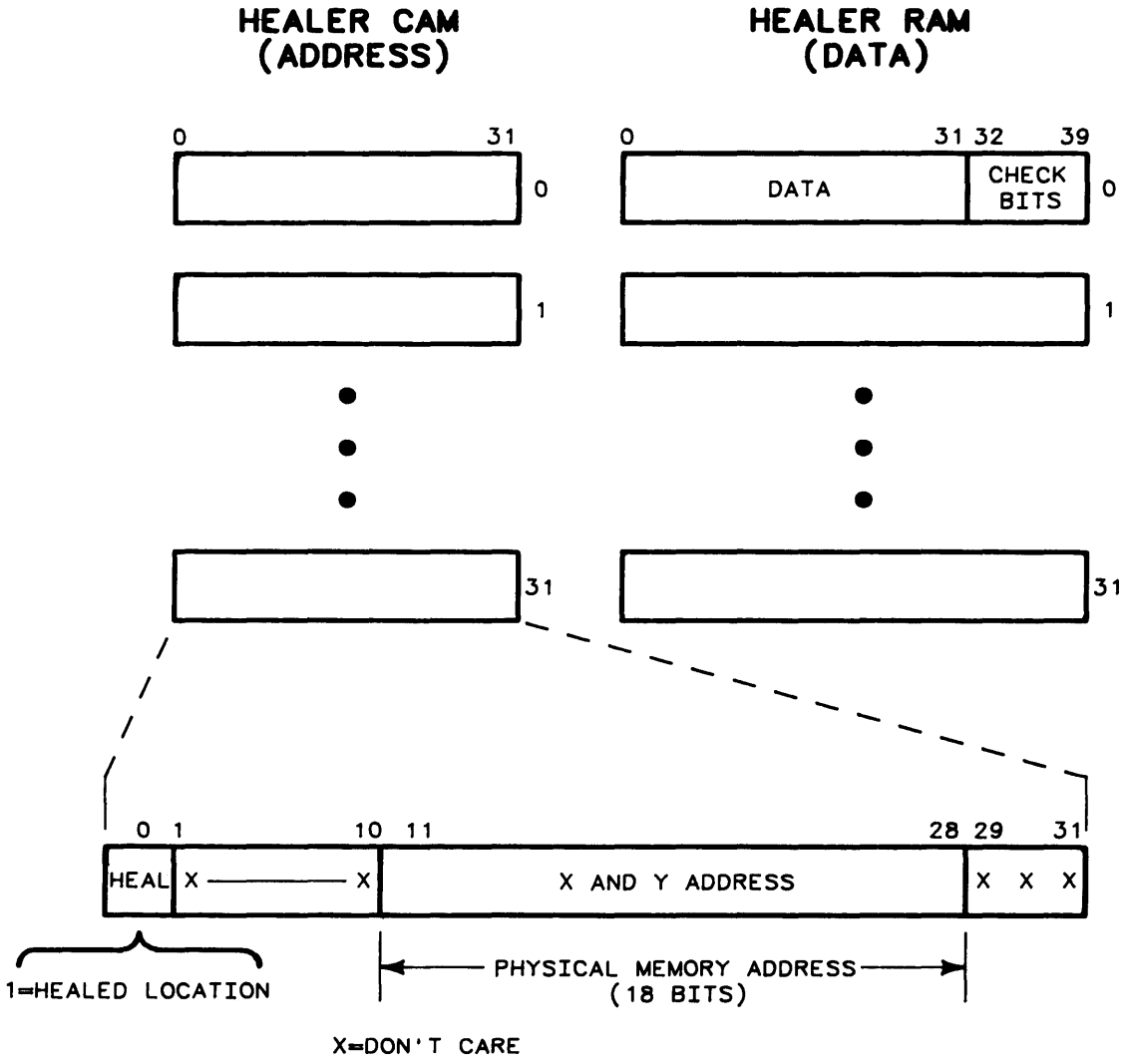


Figure 2-15. 1 Megabyte Memory Healing

IOP Bus

A 50-conductor IOP ribbon cable interconnects the motherboard with the IOP in slot #2. The IOP handles internal modules as well as the I/O backplane. Eight select codes are available per IOP. Select code 7 is assigned to the system control module, leaving seven select codes available to the user at the seven I/O backplane slots. Select codes 0-6 correspond to backplane slots 0-6, respectively. The backplane slots are physically labeled with the select code numbers.

One or two additional IOP boards can be added. Each is connected by a 50-conductor ribbon cable to a connector mounted on the computer rear panel. The ribbon cable provides the IOP bus from the boards to the connector.

A 97098A I/O Expander can be connected to each additional IOP via the rear panel connector. Each I/O expander provides eight I/O slots with signal buffering and power supplies. The select code configuration at the I/O backplane is unaffected by additional IOPs. Select codes 0-6 are assigned to the I/O backplane; select code 7 is assigned to the system control module; select codes 8-15 are assigned to the first additional IOP; select codes 16-23 are assigned to the second additional IOP.

System Control Module

The system control module (SCM) provides the operating system with the current time at power-up, controls the service panel, provides high-temperature and power-fail warnings to the operating system, supplies the loader ROM for the power-up routines, and provides 2K bytes of battery backed-up memory. Figure 2-16 is a block diagram of the SCM.

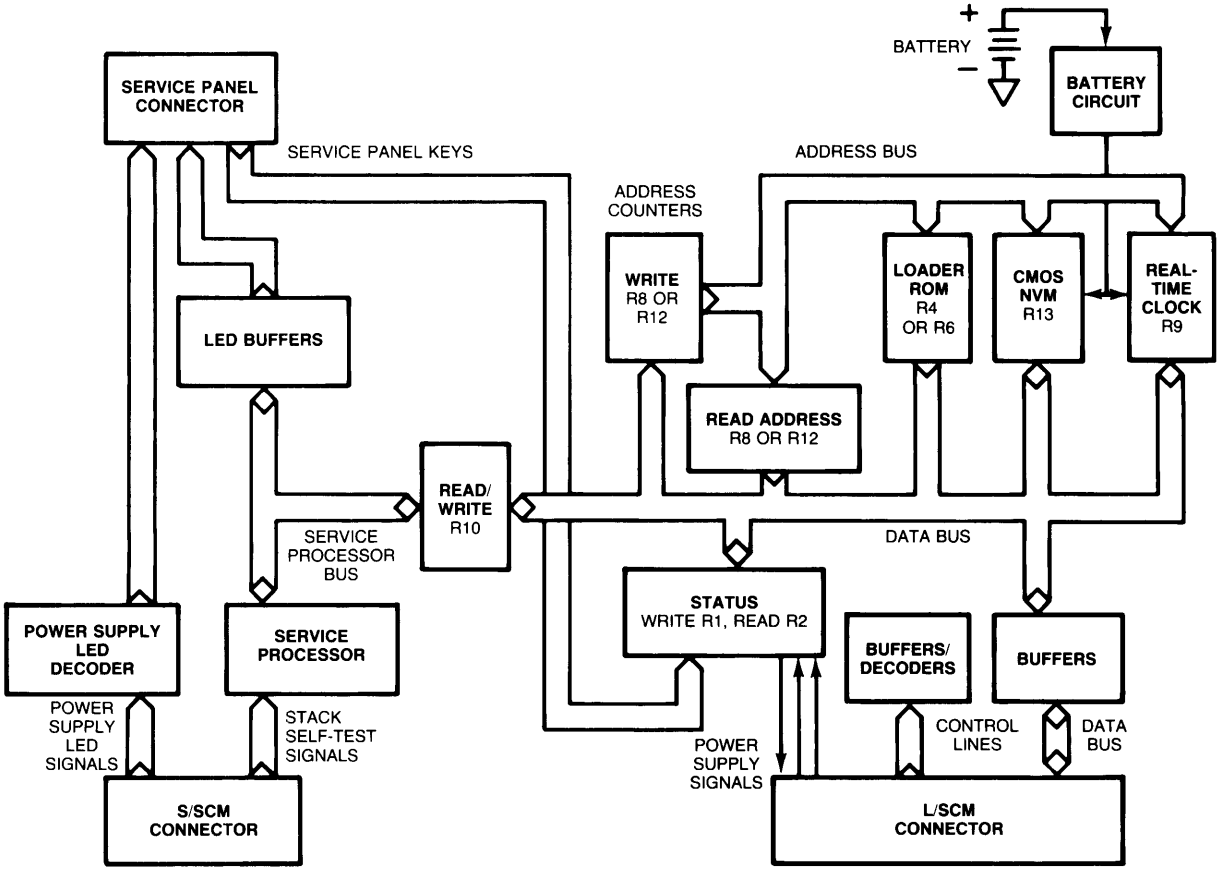


Figure 2-16. System Control Module Block Diagram

The real-time clock provides date, hour, minute, and second information. This information is valid for at least 10 days after power is switched off. The service panel interface includes the inputs and interrupts for four pushbutton switches, and a microprocessor to control the service panel LEDs.

Register Allocations

The SCM is assigned select code 7 (highest priority) because it contains the power fail interrupt. This makes it impossible for the power fail warning to be locked out by an I/O card with a higher priority. The register and bit allocations for the SCM select code (SC7) are:

Write R1

Bit 1 – Clear fan high warning; 1 = clear

Bit 2 – Enable self-test; 1 = enable, 0 = disable

Bit 3 – Clear uninterruptible power supply (UPS) warning; 1 = clear

Bit 4 – Clear key input interrupt; 1 = clear

Bit 5 – Initiate stack self-test; 1 = initiate

Bit 7 – ROM DMA enable; 1 = set address counters to all 1's and set continuous poll response, enable self-test; 1 = poll response set, 0 = clear

Read R2

Bit 0 – Reset; 1 = **RESET** switch pressed

Bit 1 – PFW; 1 = power fail warning

Bit 2 – Fan high; 1 = fan high warning

Bit 3 – Self-test enabled; 1 = self-test enabled

Bit 4 – UPS warning; 1 = UPS warning

Bit 5 – RTC/NVM battery fail; 1 = fail (latched at power up)

Bit 12 – Start; 1 = **START** switch pressed

Bit 13 – Continuous self-test; 1 = **SELF TEST** switch latched on

Bit 14 – Non-maskable interrupt; 1 = interrupt

Bit 15 – Memory dump; 1 = **MEM DUMP** switch pressed

Read R3

Self-identity code (4007 hex)

Read R4 or R6

Loader ROM data

Write R8 or R12

RTC/NVM/ROM address

Read R8 or R12

Read RTC/NVM/ROM address for testing the data bus. Bit patterns can be written to and read from this register to make sure there are no faults on the data bus.

Read R9

Bits 0-3 – Real-time clock data (RTC)

Read/Write R10

I/O to service processor and service panel

Read/Write R13
Bits 0-7 – Non-volatile memory (NVM)

After the computer is powered up, or after the interface clear (IFC) signal is issued, the SCM board status is as follows:

- High temperature warning off
- Self-test bit enabled
- All pushbutton switch interrupts off
- UPS warning off
- Memory address counters at FFFF hex

Real-Time Clock (RTC) and Non-Volatile Memory (NVM)

The real-time clock (RTC) chip contains 16 four-bit locations that store clock and data information initially loaded from the IOP. A 32.768 KHz crystal oscillator provides the time base. A 4-bit multiplexed address/data bus provides I/O for the chip.

Writing to R8 or R12 loads a 4-bit register address in the chip. The RTC data is then accessed by reads or writes of R9, either reading data from the addressed location or writing data to it. Once the initial address is accessed, succeeding reads or writes cause automatic increments of the address (address is complemented). This enables blocks of data to be read or written without updating the address from the IOP.

The accuracy of the RTC is partially dependent on the configuration, environment, and usage of the computer. Worst-case clock deviation will vary between 40 seconds per month and 3 minutes per month depending on the preceding factors.

The non-volatile memory (NVM) chip contains 2048 eight-bit bytes of CMOS RAM used to store configuration and service data. Writing a 16-bit address to R12 in complemented form loads the address of the NVM location. The data in that location is then accessed by a read or write of R13.

During power-off states, a nickel-cadmium (NICAD) battery assembly on the SCM provides power to the RTC and NVM chips for a minimum of 10 days.

The RTC and NVM chips must be disabled when power is coming up or going down. Otherwise, spurious data could be written onto the chips. When the power supply senses that the power output is out of specification, it sends an interface clear signal to disable communications with the IOP bus. This signal is translated on the SCM and disables the chips.

When the chips are disabled, the circuitry enables battery input to the chips, maintaining the memory data and keeping the clock running. During normal operation, the battery is being charged by the +12V supply.

A sample and hold circuit checks the voltage level of the battery assembly at powerup. When power is off, a capacitor is charged to the battery level. When power comes back on, the voltage level of the capacitor is automatically read. If the level is below 3 volts, the RTC and NVM data may be invalid and should be restored by the operating system. This fault condition is indicated to the IOP by the RTC/NVM battery fail bit (bit 5 of R2). This bit must be read within four seconds of powerup.

Loader ROM

The SCM contains the bootstrap loader ROM which contains the code to "boot up" the operating system from the system mass storage device. Figure 2-17 is a general flowchart of the loader ROM. The address for the 8K loader ROM is stored in the same locations used by the RTC and NVM. The starting address of the code is FFFF hex. The address is automatically decremented after each read.

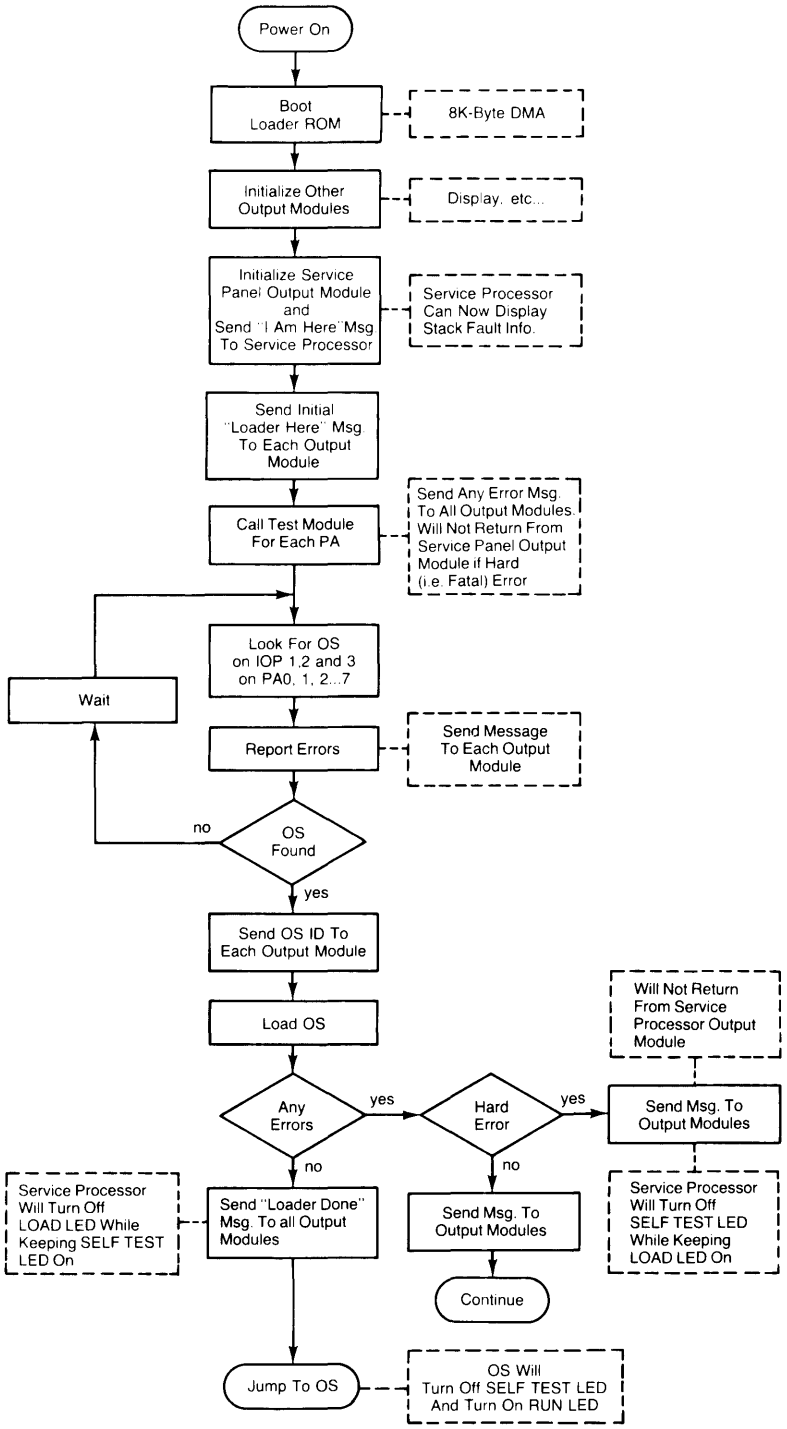


Figure 2-17. Loader ROM Flowchart

The power-up sequence begins with self-test execution by all processor stack chips. Then the CPU microcode instructs the IOP to read R3 of SC7. If bit 14 is set in this register, it identifies the presence of a loader. If bit 14 is not set, R3 of SC6 is read. All select codes are checked in descending order until a loader is identified as available by bit 14 set.

When the loader is found, an 84 hex is sent to R1 of the loader's select code to reset the address counter to FFFF hex (0 hex to the chip). This enables direct memory access (DMA) and the self-test bit. Through DMA, 2048 bytes of the loader are input from R4 with the final byte from R6. The ROM address is automatically decremented as the data is input. The initial 2K bytes of loader code enables the operating system to load the entire 8K loader.

The loader contains code which enables the operating system to be loaded in from the system disc. Several loader modules are contained in the loader ROM. These include a kernel module, output modules (for example, ASI/terminal), input modules (for example, HP-IB/CS80), and a test module. The test module is described and flowcharted in Chapter 3.

If the Processor Stack contains 1 Megabyte RAM boards, Boot Loader ROM Rev. B (09020-80001) must be used, and UNIX 4.0 or basic 2.0 software must be used.

Boot Loader ROM Rev A. (09020-80000) can be used with UNIX 4.0 or Basic 2.0 (or any previous software versions) as long as the stack **DOES NOT** contain a 1 Megabyte RAM board.

Boot Loader ROM Rev. B (09020-80001) can be used with any RAM configuration but **MUST** use UNIX 4.0 or Basic 2.0 software. (Any earlier versions of software cannot be used with this boot loader.)

Service Panel Interface

Register 10 of SC7 is reserved for communication between the service processor and the main system software. The service processor has the ability to read data from the IOP and to write data to the IOP via R10. Refer to Service Processor Code description in Chapter 3 for details.

Power-Fail Warning

When the power supply assembly detects an impending power failure, a power fail Warning (PFW) is issued. This causes a response to an I/O poll on SC7 and bit 1 to be set in R2. The time from when the warning is issued until power shuts down could be as little as 1 msec. If power is restored, PFW goes away and bit 1 in R2 is automatically cleared by the power supply assembly.

High Temperature Warning

When the fans switch to the highest speed because of high ambient temperature or heavy load on the power supply, a high temperature warning is issued to the system by setting bit 2 of R2 and responding to the next I/O poll. Once the bit is read it should be cleared by setting bit 1 of R1, because the signal is edge triggered and can come and go. The warning indicates that the power might be shut off at any time to prevent damage to the hardware.

Self-Test

Self-tests can be initiated in three ways: 1) Turn power on to automatically perform self-tests; 2) Set the enable self-test bit (bit 2) on R1 and write a 1 to bit 5 in R1; 3) Push the **SELF TEST** switch on the service panel with the enable self-test bit set.

The **SELF TEST** switch latches to allow continuous self-test. Bit 13 in R2 is set while the **SELF TEST** switch is latched. The service panel output module code in the loader ROM reads that bit to see if the **SELF TEST** switch is latched. If it is, and no loadee can be found to load, self-test is restarted by writing a 24 hex to R1 following a few seconds delay for stack cooling.

Non-Maskable Interrupt

This interrupt allows an I/O card to reset the processor. The software is informed of this interrupt by a poll response and bit 14 of R2 set. An I/O interface clear (IFC) is issued to remove the poll response. Jumpers on the SCM can connect this line to the power supply reset or self-test signals.

Service Panel Switches

Three momentary switches on the service panel cause a poll response and bits in R2 to be set. The switches are **RESET** (bit 0), **START** (bit 12), and **MEM DUMP** (bit 15). They can be cleared by writing a 10 hex to R1.

14.7456 MHz Clock

This clock is generated on the SCM, buffered, and sent to the I/O backplane. It is used by the I/O cards for baud rate generation and for driving state machines.

Service Panel

The service panel, located behind the computer front panel, provides all the information necessary to diagnose hardware failures to the level of a field-replaceable module. The control logic for the service panel is on the SCM and consists of a microprocessor and supporting circuits.

The service panel has 4 switches and 27 LEDs. The switches are defined as: **RESET**, **START**, **MEM DUMP**, and **SELF TEST**. The LEDs are defined as **POWER ON**, **RUN**, **SELF TEST**, and there are several fault-indicating LEDs.

Switches

The following paragraphs define the four switches on the service panel.

RESET Switch

When this momentary pushbutton switch is pressed it causes the system to reset via a software interpretation of an SCM board poll response and status message. All programs running in the machine are stopped and the **RUN** LED is turned off. After reset is complete, the system waits for the **START** or **MEM DUMP** switch to be pressed.

START Switch

When the **START** switch is pressed, the auto-start procedure is initiated. System powerup also initiates auto-start. The auto-start procedure automatically loads a selected program which starts up the user's application.

If no auto-start file is found, the system enters an idle state and waits for an external stimulus. If a system console or operator interface is attached to the computer, the operator or programmer has control of the system and can bring up the system manually.

MEM DUMP Switch

The **RESET** switch must be pressed to halt all program operations before the **MEM DUMP** switch is pressed. Then, when the **MEM DUMP** switch is pressed, the contents of main memory are dumped onto the 1/4-inch tape cartridge. When this completes, program operations begin where they left off. Pressing **MEM DUMP** when a load has failed (**LOAD** LED still on) displays an error number on the **I/O** LEDs. The error number assists in fault diagnosis. Refer to Chapter 3 for details on **I/O** LED error numbers.

SELF TEST Switch

When the **SELF TEST** switch is pressed, the computer initiates a continuous system self-test. In contrast to the single-pass self-test which is executed each time the system powers up, the continuous self-test is primarily for detecting intermittent failures. The **SELF TEST** switch is a latching switch. As long as the switch is down, the continuous self-test continues. When the switch is pressed again, releasing it, the continuous self-test is terminated at the end of this pass. The computer cannot be powered on when the **SELF TEST** switch is latched on.

The **SELF TEST** LED indicates the status of self-test mode. The LED and its operation are descibed in following paragraphs.

Light Emitting Diodes (LEDs)

The following paragraphs define the 27 LEDs on the service panel. The first two LEDs defined indicate normal operating conditions and are green. The remaining LEDs are red and define test-in-process or fault conditions. Whenever a self-test of the computer is initiated, all service panel LEDs light for about one second and then go off. This provides a quick check of LEDs.

POWER ON LED

This LED indicates that the +5V supply is operating. It implies that the power supply assembly is functional and that power is being provided to the system.

RUN LED

This LED indicates that the operating system has been loaded and is running. It is controlled by the service microprocessor from a status message from the operating system.

SELF TEST LED

The **SELF TEST** LED is on whenever self-test is in progress. It is turned on by the service processor at every powerup or when the **SELF TEST** switch is pressed. It is turned off when a hard failure is detected or when the self-test successfully completes. If a hard failure is detected, an indication of the failure is displayed on the service panel. The failure can only be cleared by a hard reset (cycle power or press **SELF TEST**). If no failures are detected, the operating system turns off the **SELF TEST** LED and turns on the **RUN** LED.

PROCESSOR 1-12 LEDs

These LEDs are controlled by the microprocessor and indicate which processor stack finstrate did not pass self-test. Only one finstrate LED can be on at a time except at powerup when all service panel LEDs are on briefly. The error must be cleared by a hard reset.

I/O 0-6 LEDs

These LEDs are controlled by the microprocessor and are turned on by the operating system or boot loader ROM (via a status word to the microprocessor) when it detects that a card failed self-test. More than one I/O card failure can be indicated at once. Only a hard reset clears I/O failures. These LEDs also indicate an error number when **MEM DUMP** is pressed on a load failure.

LOAD LED

This LED lights while the operating system is being loaded during the power-up sequence. The LED extinguishes after a successful load. If the LED remains lit, a load fault is indicated. Press the **MEM DUMP** switch for detailed information on the **I/O** LEDs. A hard reset must clear this failure.

DOOR LED

This LED indicates the power supply has shut down because the processor stack door or I/O card cage door is open. This fault must be cleared by a hard reset.

TEMP LED

When the power supply assembly shuts down because of an overtemperature in the processor stack, this LED is turned on. A hard reset must clear this failure.

PS LED

This LED is on when +5V is off but the +16V bias supply is valid. It indicates that main power has been shut down for some reason. This LED cannot be on if either the **TEMP** or **DOOR** LED is on. Therefore, if this LED is on, it cannot be due to stack overtemperature or door open. Reasons for this LED to come on include: a short or open on a power supply voltage, a power supply failure, a power outage of less than one second, and fast cycling of the on/off switch. The failure indication can only be cleared by a hard reset.

SCM LED

The **SCM** LED turns on if the diagnostic in the loader ROM detects a faulty SCM or if the service processor code on the SCM detects a failure. A hard reset is required to turn off the **SCM** LED.

Service Panel Lockout

The service panel switches can be temporarily disabled to prevent disasters resulting from accidental or malicious actions. The computer may have to be powered down to regain control of the system if a system failure occurs with the switches disabled.

I/O Overview

The computer provides seven HP-CIO slots numbered 0-6 and two optional expander ports for 97098A I/O Expanders. Each 97098A provides eight additional slots or select codes. The computer only provides seven slots (select codes 0-6) because select code 7 is used inside the mainframe for the system control functions.

Table of Contents

Testing and Troubleshooting

Chapter 3

Introduction

This chapter contains information to help you test the computer and diagnose failures. Troubleshooting and repair strategy is briefly described. Then, the problem isolation section relates service panel indications to probable faults.

The remainder of the chapter contains descriptions of the service processor code, loader ROM test module, loader error messages, self-tests and diagnostics, and early warning/fault tolerance features.

Troubleshooting and Repair Strategy

To troubleshoot a failing computer, perform the problem isolation procedures provided below. The diagnostics and service panel indicators are designed to enable fast fault isolation to a replaceable module. Every replaceable module can be replaced within 15 minutes from fully assembled machine, through disassembly and replacement, back to fully assembled machine.

Chapter 4 contains the procedures to access and replace failed modules in the computer, and Chapter 5 has exploded view drawings of the computer showing attaching parts. All replaceable parts are listed in Chapter 5.

Problem Isolation

Figure 3-1 shows the service panel indications of a normal, fault-free power-up sequence from power on to operating system running. A computer fault aborts this sequence. In most cases, the service panel indicates the fault.

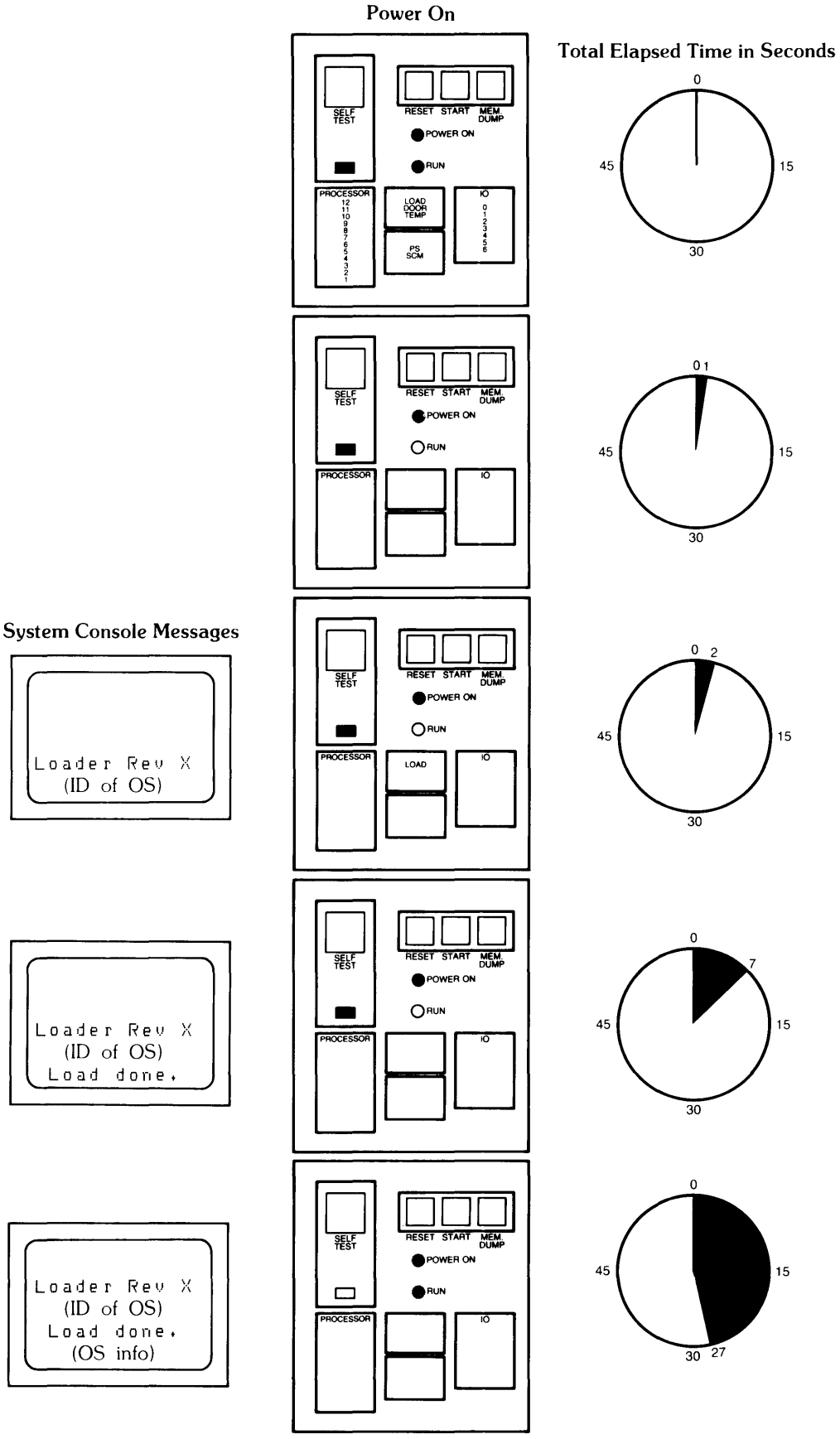


Figure 3-1. Fault-free Power-up Sequence

Figure 3-2 (three sheets) shows service panel indications of possible faults and provide the procedures to fix the fault. Perform the procedures in the order listed. Replacement procedures are provided in Chapter 4, and exploded view drawings in Chapter 5.

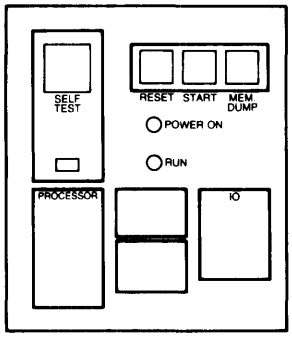
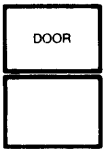
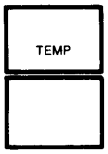
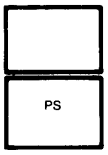
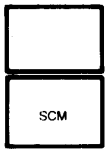
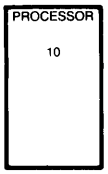
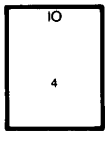
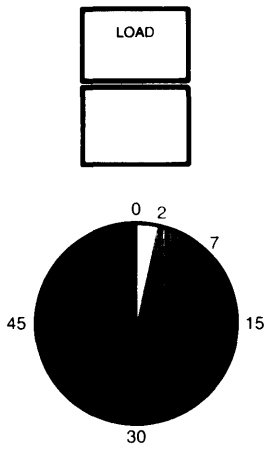
Indication	Procedure
 Note: No LEDs on.	Check/Replace: 1. Ac power cord 2. Service panel cable 3. Power supply cable 4. Power supply assembly 5. Ac module
	Close/Tighten: 1. I/O door 2. Processor stack door
	Check/Replace: 1. Ambient air temperature 2. Clogged filter/airflow blockage 3. Fans 4. Power supply assembly
	Check/Replace: 1. Power supply assembly 2. I/O cards 3. Finstrates 4. System control module 5. Motherboard/IO backplane
	Check/Replace: System control module
 Note: Any one of the 12 PROCESSOR LEDs may be on.	Check/Replace: Finstrate
Note: Any one or more of the 7 I/O LEDs may be on. 	Check/Replace: 1. I/O card 2. Peripheral device 3. Interface cable

Figure 3-2. Fault Indicators (Sheet 1 of 3)

Indication **Procedure**



Press:
MEM DUMP
(3 to 5 second delay)
All I/O LEDs on for 1/2 second? — No
Yes
Any I/O LEDs left on? → No → Check/Replace:
1. System control module
2. Service panel
3. Service panel cable
Yes
Read error number from table and fix problem.

Error No.	I/O LEDS (1 = on; 0 = off) 6 5 4 3 2 1 0	Description
0	0 0 0 0 0 0 0	*
1	0 0 0 0 0 0 1	*
2	0 0 0 0 0 1 0	Operating system not found; will retry
3	0 0 0 0 0 1 1	*
4	0 0 0 0 1 0 0	Bad operating system file
5	0 0 0 0 1 0 1	Not enough usable memory
6	0 0 0 0 1 1 0	I/O card or connected device failed self-test
7	0 0 0 0 1 1 1	*
8	0 0 0 1 0 0 0	*
9	0 0 0 1 0 0 1	Media or device not ready
10	0 0 0 1 0 1 0	*
11	0 0 0 1 0 1 1	Part of operating system not readable
12	0 0 0 1 1 0 0	Attempted address or read past end of volume
13	0 0 0 1 1 0 1	Controller/unit failed after passing self-test
14	0 0 0 1 1 1 0	I/O timeout; device did not respond in time
15	0 0 0 1 1 1 1	CS80 error occurred
16	0 0 1 0 0 0 0	Tape error occurred
17	0 0 1 0 0 0 1	Bad status from HP-IB (I/O card)
18	0 0 1 0 0 1 0	Bad I/O bus
19	0 0 1 0 0 1 1	NVM chip failed test
20	0 0 1 0 1 0 0	RTC chip not ticking
21	0 0 1 0 1 0 1	Service processor failed self-test
22	0 0 1 0 1 1 0	Test card found (Not an error)
23	0 0 1 0 1 1 1	Test module did not find SCM
24	0 0 1 1 0 0 0	Memory test in progress (Not an error)
25	0 0 1 1 0 0 1	Looking for operating system (Not an error)

* These codes are not used.

Figure 3-2. Fault Indicators (Sheet 2 of 3)

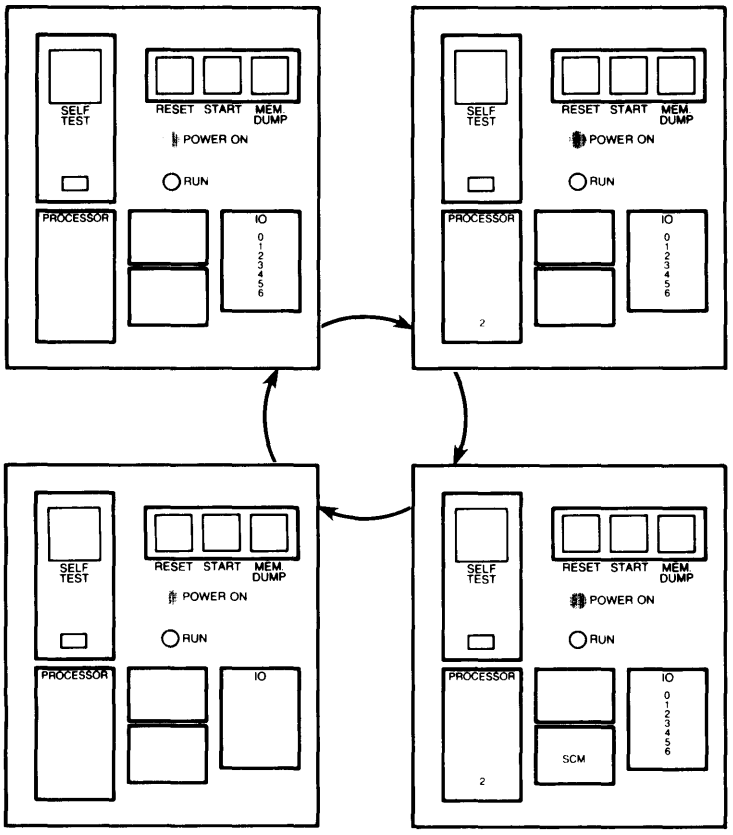
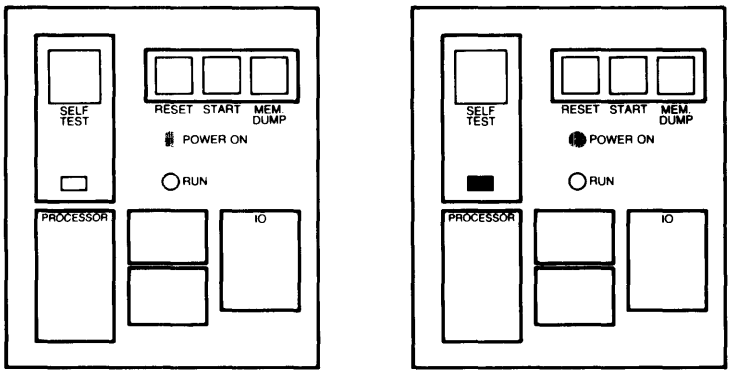
Indication	Procedure
	Check/Replace: 1. I/O cards 2. IOP in slot 2 3. System control module 4. IOP cable
	Check: 1. Operating system 2. Insufficient RAM

Figure 3-2. Fault Indicators (Sheet 3 of 3)

Service Processor Code

The service processor code gathers diagnostic data, interprets the data, and displays the information in a convenient form on the service panel. The code resides in ROM within the service processor chip which is located on the system control module (SCM).

The service processor code monitors the LED signal coming from the 12 processor stack boards. The code also receives instructions from the operating system or loader code through register 10 (R10) on the SCM.

Figure 3-3 is a flowchart of the service processor code.

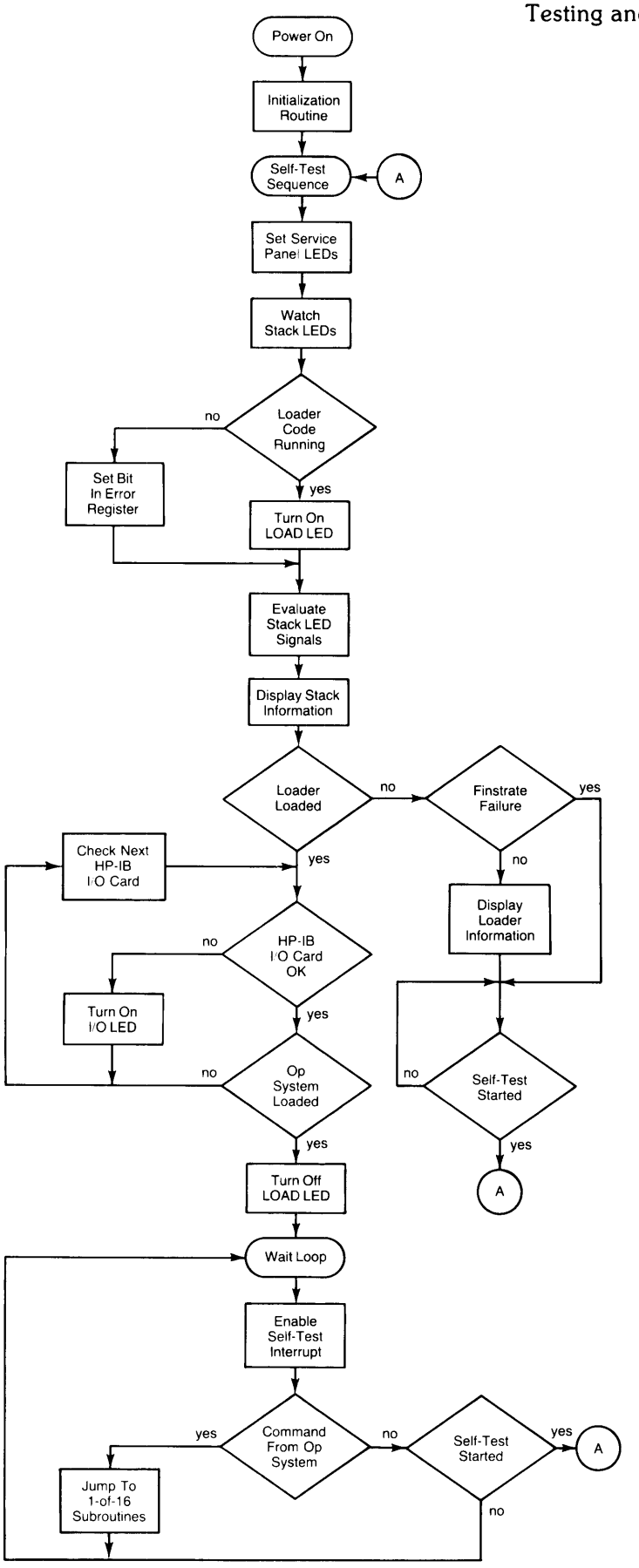


Figure 3-3. Service Processor Code Flowchart

Loader ROM Test Module

Figure 3-4 is a flowchart of the loader ROM test module. This module is contained in the 8K ROM on the SCM with the other loader ROM modules. Chapter 2 contains a description and general flowchart of the loader ROM.

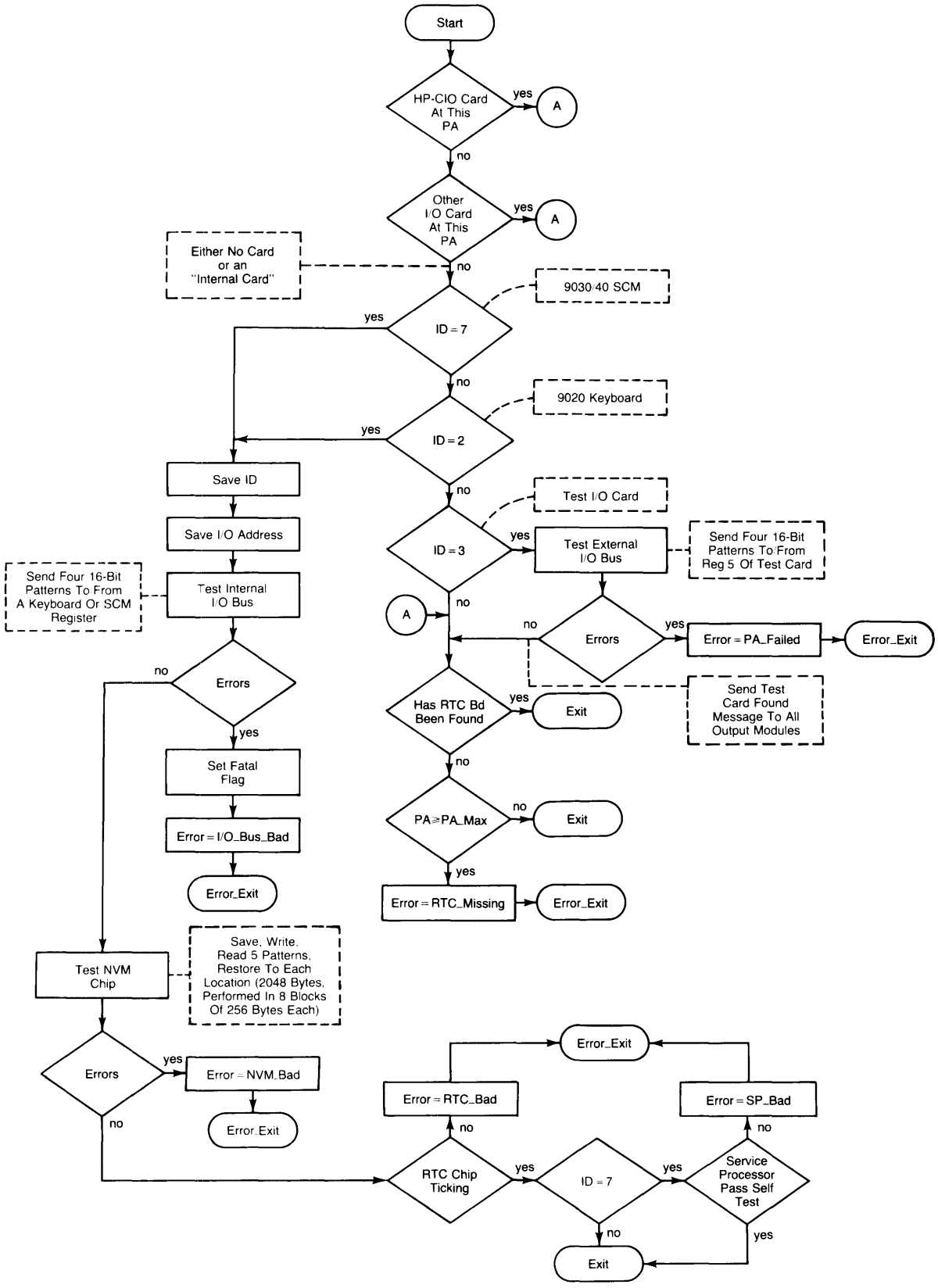


Figure 3-4. Loader ROM Test Module Flowchart

System Loader Messages

Introduction

The System Loader is a program which resides on ROM in the computer. It contains the loader self-tests and causes the computer to search for and load an operating system. If the computer is unable to locate and load the test system, or any operating system, a message is displayed on the system console and/or indicated by the **IO** LEDs after pressing **MEM DUMP** (Chapter 2). Each of these messages is explained below. Possible causes for many of the messages are provided. If the message begins with "ERROR:" the system halts after issuing the message. If the message begins with "NOTE:" the message provides information and the computer continues operating.

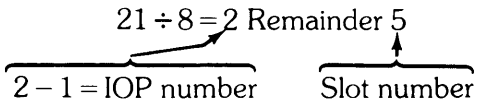
If the message you recieve indicates a hardware failure, call your HP Customer Engineer for service. If the operating system can be loaded, the system functional tests may be run to assist you in determining what component has failed.

Often the computer attempts to identify the device to which it was "talking" when the message was generated. The trailer "SELECT CODE NNNNN" (or "SELECT CODE NN") is appended to the message to indicate which select code (I/O port) of the computer caused the problem.

Trailer NNNNN indicates Rev. A loader select codes. To find the IOP divide the number by eight and subtract one. To find the Select Code (slot) divide the number by eight and the REMAINDER is the slot number.

Example:

Where: NNNNN is 21



Trailer SELECT CODE NN indicates Rev. B loader select codes; 0 through 7 = 1st IOP, 8 through 15 = 2nd IOP, and 16 through 24 = 3rd IOP.

The HP 9030 and HP 9040 have seven I/O slots available. They are associated with select codes 0 thru 6 with the top slot being select code 0. Select code 7 is used for the internal SCM board.

The upper left slot on an I/O expander, when viewed from the rear, is the lowest number select code on the I/O expander.

Messages

`Loader XXX` – Informational message identifying the revision of the system loader. This message is usually followed by a single line message identifying the operating system the computer is attempting to load.

Error Code #24 `Testing Memory...` – Informational message that follows the "Loader XXX" message indicating that the loader is performing memory tests and configuring memory. This can take up to 15 seconds. (NOT AN ERROR)

Error Code #25 `Looking for System...` – Informational message that follows the "Testing Memory..." message indicating that the loader is searching for an operating system.

`Please mount next volume.` – Informational message. The loader is ready to load another portion of the operating system. Mount the volume containing an unloaded portion of the operating system. Volumes may be mounted in any order without affecting the loading process.

Error Code #2 `SYSTEM NOT FOUND; WILL RETRY: XXX`
`SYSTEM NOT FOUND; WILL RETRY IN XXX`
– Unable to find an operating system on any mass storage device. The loader will attempt to find an operating system again in XXX seconds. Possible causes: mass storage device not powered up, no media in mass storage device, wrong disc in disc drive, computer or mass storage device hardware failure, media failure, incompatible loader/system revision numbers, etc.

Error Code #4 `BAD SYSTEM FILE: NNNNN`
`BAD SYSTEM FILE: SELECT CODE NN`
– Operating system loaded. However, an error has been detected in the operating system code during loading. Possible causes: corrupt system, media failure, mass storage hardware failure, or computer hardware failure.

Error Code #5 `INSUFFICIENT USABLE MEMORY: XXXX`
`NOT ENOUGH USABLE MEMORY; TOTAL IS XXXX`
– The amount of usable memory is too small to load the operating system. The total amount of good memory is "XXXX" bytes. However, the amount of memory available for the Rev. A operating system is "XXXX" minus 32K bytes. The amount of memory available for the Rev. B operating system is "XXXX" minus 98 304 bytes. Possible causes: corrupt system or hardware (memory) failure.

Error Code #6 `BAD CARD OR DEVICE: NNNNN`
`BAD CARD OR DEVICE: SELECT CODE NN`
– Informational message. A hardware failure has been detected (interface card or mass storage device did not pass the Module Self-Test). The loader continues searching for an operating system. Possible causes: bad interface card or mass storage device.

Error Code #9

DEVICE NOT READY: NNNNN
VOLUME NOT MOUNTED: NNNNN
MEDIA/DEVICE NOT READY: SELECT CODE NN
– While loading, the media (Volume) was removed from the device (e.g. a floppy disc was pulled out of a disc drive), the device went offline, or a hardware problem caused the device to become "not ready".

DMA FAILED: NNNNN – Data did not transfer properly from the mass storage device to the computer. Possible cause: Mass storage device hardware failure or computer hardware failure.

Error Code #11

UNRECOVERABLE DATA: NNNNN
UNRECOVERABLE DATA: SELECT CODE NN
– Part of the operating system is not readable. Possible causes: media failure or mass storage device hardware failure.

Error Code #12

END OF VOLUME: NNNNN
END OF VOLUME: SELECT CODE NN
– Attempt to address or read past the end of a volume. Possible causes: corrupt system, media failure or mass storage device hardware failure.

Error Code #13

CTRLR/UNIT FAULT: NNNNN
CTRLR/UNIT FAULT: SELECT CODE NN
– Hardware passed initial self-test. However, it failed while being used to load the operating system. Possible causes: computer (interface card) hardware failure or mass storage device hardware failure.

Error Code #14

IO TIMEOUT: NNNNN
IO TIMEOUT: SELECT CODE NN
– Mass storage device failed to respond fast enough while attempting to load from it. Possible cause: computer hardware failure or mass storage device hardware failure.

Error Code #15

CS80 DEVICE: NNNNN
CS80 DEVICE: SELECT CODE NN
– Indicates a mass storage device hardware failure.

Error Code #16

TAPE DEVICE: SELECT CODE NN –Usually indicates a tape device (HP 7970, HP 7974, HP 7978) hardware failure. Can also indicate a failure on the HP 27110A HP-IB Interface (or the Internal HP-IB interface). Tape errors covered are: "Command Rejected", "Interface Busy", "Rewinding", "Tape Runaway", "Data Timing Error", and "Command Parity Error".

Error Code #17

HPIB CARD: NNNNN
HPIB CARD: SELECT CODE NN
– Transaction to the indicated HPIB interface card was terminated due to a probable interface card failure.

Error Code #18

BAD IO BUS: NNNNN
BAD IO BUS: SELECT CODE NN
– Indicates a computer hardware failure on the computers first IOP.

Error Code #19

`BAD NVM: NNNNN`
`BAD NVM: SELECT CODE NN`
– Indicates that Non-Volatile Memory failed its self-test. Possible cause: computer hardware failure.

Error Code #20

`BAD RTC: NNNNN`
`BAD RTC: SELECT CODE NN`
– Indicates that the built in Real Time Clock is not operating correctly.

Error Code #21

`BAD SP: SELECT CODE NN` – Indicates that the HP 9030 and HP 9040 computer's service processor failed self-test.

Error Code #22

`Test card found` – (Not an error.)

Error Code #23

`Test module did not find SCM`

HP-UX 4.0 Operating System Error Messages

The self-test messages displayed by the operating system consist of:

1. Self-Test Warning and Error Messages.
2. Fatal Error Messages.
3. Software Failure Messages

Warning and Error Messages

`Clock and date not set.` – This message indicates that either the contents of the NVM are not valid at powerup or the clock has not been set since this condition was detected. Possible causes: a bad battery on the SCM board, or computer powered down for more than 2 weeks. The condition does not stop the system operation.

```
Self test error 1: I/O address AA, SS STATUS: XXXXXXXX
```

Where: AA = Select code

SS = Subaddress

XXXXXXXX = Device or card dependent error information (in hexadecimal).

This error message is displayed as a result of the self-test failure of an I/O device. The select code subaddress denote the device, and the device dependent error information indicates the nature of the failure. System operation can continue provided that use of the failed device is not required.

`Self test error 2: CHECKSUM for segment NN` – When the system is powered up, or a system reset is executed, the checksum for every code segment of the operating system is computed and compared to a checksum in the operating system code. When the checksums do not agree for a segment, the segment number is stored. As a result, the segment reported is the last segment for which a checksum error was detected. The operation of the system is not halted, however, further operation is at your own risk.

```
Self test error 3: XXXX NN
```

Where: XXXX = "CPU#", "IOP#", or "MC#_".

NN = The Nth of that type of component (counting from the bottom of the stack).

This error occurs when the system is able to get completely through the board self-test and the loader self-test, but a failed stack component is detected by the operating system. The message indicates the type of component which has failed and its relative position in the stack. Operation of the system can continue, if the failed board is not required,

```
Self test error 4: Memory reduced to: NNNNNNNN Bytes, MCs:<list>
```

Where: NNNNNNNN = number of bytes (in decimal) that are available.

<list> = A list of Memory Controller numbers which had failures. Up to 10 MC numbers are printed in 10 two character fields, with no intervening spaces. For example: "MCs: 1 210" indicates that Memory Controllers 1, 2, and 10 have failed the memory test. Memory boards (and memory controllers) are numbered from 1, starting at the bottom of the RAM.

This number represents all usable RAM in the system including memory used to hold code segments.

`Self test error 5: Fewer finstrates were found than expected.` – This message is displayed when the number of boards recorded in the Non-Volatile Memory (NVM) is greater than the actual number of boards in the stack. If the number of boards in the stack is greater than the number stored in the NVM, the number in the NVM is updated to reflect the larger stack size.

Fatal Error Messages

`System halted due to double bit memory error on MC # NN CCCCCCCC`

Where: NN = MC #

CCCCCCCC = Last healer content for that MC (in hexadecimal).

This message is displayed when a double bit error has been detected by the memory controller hardware. The MC# is in terms of memory controller boards (counting up from the bottom of the stack). This information is also recorded in the NVM.

If more than one MC with a double bit error is found, only the last error is displayed. If no double bit errors are found, "No DBE found" replaces NN XXXXXXXXX. DBE information is stored in the NVM.

`SYSTEM_HALTED: Insufficient memory to start system` – This message is displayed when there is insufficient memory for the operating system and user subsystem. Check the stack self-test lights to see if any stack components have failed self-test. Also, check the memory configuration of the computer to see if it is large enough to accomodate the system and options which are being loaded.

`SYSTEM HALTED: Incompatible IOPs` – This message indicates that an illegal combination of IOP boards were found at power up. IOPs of Revision 2.1 or earlier are not compatible with IOPs of Revision 2.2 or later.

System Error Message

`System halted->SYSTEM ERROR:....` – This message is displayed when the operating system software encounters either:

- an unanticipated trap,
- an unrecoverable system software error.

The "trap" is distinguished from the software error by the word "trap:" which is added to the first line of the message.

Before displaying any messages, the currently executing CPU disables its interrupts and causes all other CPUs to stop operating. The message text is multiple lines information dumped from memory and internal registers. The message starts on the top line on the Display and overwrites any other messages on the CRT. If a printer is the output device and the message is more than 25 lines in length, the message continues to print (up to 500 lines).

Self-Tests and Diagnostics Overview

Three levels of overlapping diagnostics provide the primary service support tool for the computer. These are the module self-tests, the self-test supervisory code, and the system diagnostics. The module self-tests and self-test supervisory code are executed at powerup or on program request. Some module self-tests are executed individually at user request. The system diagnostics are specific for each peripheral in the system and are run on request from the operator.

A power-up condition, a program request, or a command that simulates powerup causes the power supply to generate a signal to the processor stack that puts the stack in self-test mode. When stack self-test is completed, the stack signals all internal modules on the I/O interface to begin their self-tests. The self-test supervisory code located in the loader ROM begins executing its tests when the module self-tests are completed.

Module Self-Tests

The first level of diagnostics consists of the module self-tests. The module self-tests are low-level tests which are initiated by computer modules on powerup or on hardware or software request. A module is defined to be any section of the computer which is field replaceable. Test results are communicated to the user via LED indicators on the service panel. Each self-test is designed so that its results can be read by higher level diagnostics.

Each module's self-test is independent of the other self-tests. The failure of a module does not cause the other modules to fail their self-tests except in the case of a power supply failure.

Self-Test Supervisory Code

The second level of diagnostics is the self-test supervisory code (STSC). The STSC is divided into two parts. The first part is resident in the loader ROM and is run as part of the power-up sequence. The second part is resident in the power-up section of the operating system software.

The STSC in the loader ROM reads the self-test results of the I/O cards which could be used in loading the operating system and reports the results to the user. It also verifies the integrity of the internal I/O bus. The STSC performs other tests on the system control module including RTC and NVM checks.

The second part of the STSC salvages "mapped out" RAM blocks (16K bytes) which failed the memory controller self-test. It also checks the non-loader I/O card self-test results.

System Diagnostics

The third level of diagnostics is the system diagnostics. These diagnostics are programs written in high-level languages which can do further testing of the hardware system. If destructive testing is done (for example, disc writing), the user is warned of the effects of the testing before the test is run.

This code consists of two types of programs: 1) verification programs for each peripheral and for a minimum system of computer, terminal, and disc; 2) diagnostic program to diagnose problems in a CS80 disc drive to a replaceable module.

These diagnostics are a part of the HP-UX program (in directory `CE.utilities`) and are explained in Chapter 5, Diagnostics, of the Series 500 HP-UX Section of the CE Handbook.

Early Warning/Fault Tolerance

The computer provides early warning of several probable failures. These warnings enable the user to schedule maintenance at his convenience, reducing downtime due to unexpected failure. Early warning of machine failure is provided for overtemperature conditions and memory errors.

A battery assembly on the system control module maintains the contents of the real-time clock (RTC) and non-volatile memory (NVM) when power is removed. The battery assembly is fault tolerant in that four batteries comprise the assembly but the circuit requires only three batteries to maintain RTC/NVM data.

Overtemperature

The computer contains three dc box fans. One fan is in the I/O card cage and operates at a single speed whenever power is applied. The other two fans have three speeds and are associated with the power supply and the processor stack.

The power supply and the processor stack CPU contain temperature sensors. The power supply temperature sensor controls the two three-speed fans. When the temperature in the power supply rises above 39°C, the power supply steps both fans from low to medium speed. When the temperature rises above 51°C, the fans are stepped from medium to high speed. When high speed is required for proper cooling, a message is issued to the user, providing notice that shutdown is imminent if temperature increase continues.

When the temperature at the power supply sensor exceeds 97°C or the processor stack CPU sensor senses a temperature greater than 100°C, the power supply shuts down. The **TEMP** indicator on the service panel turns on if the stack temperature is too high; the **SEC BOARD** LED on the power supply assembly lights if a power supply overtemperature condition exists.

Memory Errors

The processor stack memory controller chip detects all single and double-bit RAM failures and corrects single-bit failures. These detection and correction procedures are done at run time.

When a double-bit or greater RAM failure is detected, the CPU is notified and the entire system halts. A message is issued indicating which memory finstrate has failed.

When a single-bit failure is detected, the failure can be corrected and healed by pointing future accesses of that location to a location in the healer RAM of the memory controller chip. Each memory controller has 32 locations reserved for healing of RAM. When all 32 locations have been used, the CPU is notified that the healer is full. The operating system then tests each of the healed locations to determine if that location is still faulty or if a soft error caused the failure. Overflowed healer CAMs can be cleared and reused by the operating system.

Real-Time Clock (RTC) and Non-Volatile Memory (NVM)

The system control module contains the RTC and NVM chips and the battery assembly to maintain data in both chips during power-off states.

The RTC and NVM chips store a clock, system configuration data, and service information of significance to users and service personnel. The clock is initially loaded from the IOP and is updated by a crystal oscillator. The RTC chip stores clock and calendar data in 16 four-bit locations; the NVM chip has 2048 eight-bit locations and stores service and configuration data. RTC/NVM locations and contents are as follows:

Byte 0 – Second
Byte 1 – Clock Check Byte
Byte 2 – Minute
Byte 3 – Stack Size (two times number of finstrates)
Byte 4 – Hour
Byte 5 – Century
Byte 6 – Day of Week
Byte 7 – Day of Month
Byte 8 – Month
Byte 9 – Year
Bytes 10-13 – Control Registers
Byte 14 – Timer Resolution
Byte 15 – Timeout Scan Resolution
Byte 16 – Keyboard Initialization Data
Bytes 17-24 – Default System Startup Subsystem
Bytes 25-44 – Default Mass Storage Unit Specifier (MSUS)
Byte 45 – Size of System I/O Buffer
Bytes 46-47 – NVM Checksum
Bytes 48-53 – Healer CAM Overflow Counter
Bytes 54-57 – Last Double Bit Memory Failure Data
Bytes 58-60 – Number of 10-Minute Periods Computer is On
Byte 61 – Number of Overheat Cycles
Bytes 62-63 – Number of Power-On Cycles

The system control module contains a nickel-cadmium battery assembly consisting of four batteries to maintain the RTC and NVM chips during a power-off condition. Because only three batteries are required, one is redundant. This enables the chips to operate without error if one of the batteries has a short circuit. The battery assembly maintain RTC and NVM data for a minimum of 10 days while power is off.

Table of Contents

Assembly Access

Chapter 4

Introduction

This chapter describes how to access all the replaceable computer assemblies. The table of contents of this manual lists the replaceable assemblies and the corresponding page numbers in this chapter where the access procedures are located. Read this introduction carefully before performing assembly access.

The procedures help you to disassemble the computer in order to access the assemblies. Reassembly procedures are the reverse of disassembly procedures. Special instructions required for reassembly are clearly noted.

This chapter is organized in several sections, as follows:

- General Safety Procedure
- Electrostatic Discharge
- Case Parts
- Replaceable Assemblies

The computer is either in a System II enclosure (HP 9030) or it is in a stand-alone cabinet (HP 9040). The assembly replacement procedures provide for both packaging configurations.

The following tools are required to disassemble the computer:

- #1 Pozidriv screwdriver
- #2 Pozidriv screwdriver
- Flat-blade screwdriver
- 7/16-inch nutdriver
- 5.5-millimetre nutdriver
- 1/8-inch Allen wrench
- Power supply discharge tool, HP PN 09855-67004
- Antistatic kit, HP PN 9300-0794

WARNING

UNPLUG COMPUTER POWER CORD FROM AC OUTLET BEFORE REMOVING ANY ASSEMBLY.

LETHAL VOLTAGES ARE PRESENT INSIDE THE COMPUTER. OBSERVE ALL WARNINGS IN THIS MANUAL, AND OBSERVE THE FOLLOWING SAFETY PROCEDURES.

General Safety Procedures

The following simple precautions can save a life.

- Do all possible operations with the computer unplugged from the power source.
- If installation, maintenance, or repair must be done with the computer energized, take the following precautions:
  a. Never work alone in high-voltage areas. In case of accidental shock, a life may depend on rapid removal from the energized source and appropriate first-aid action.
  b. Employees working in high-voltage areas should know where to obtain respiratory resuscitation and/or cardiopulmonary resuscitation (CPR), in case a fellow worder needs assistance.
  c. In case of burns, treat only after the person is breathing and has a normal heartbeat.
- If primary wiring change is made, perform continuity test between power cord ground and metal chassis. Record results on Repair Order.

CAUTION

THE COMPUTER HAS ASSEMBLIES AND COMPONENTS SENSITIVE TO ELECTROSTATIC DISCHARGE. READ THE FOLLOWING SECTION AND OBSERVE THE PROCEDURES TO AVOID DAMAGE TO THE COMPUTER AND ITS PARTS.

Electrostatic Discharge

Electrostatic discharge (ESD) causes failure in many PC assemblies, other assemblies, and components. Processor stack finstrates are particularly vulnerable to ESD damage. Static electricity doesn't appear to be dangerous because much of the ESD that can cause component or assembly failure is too small to be felt. Humans can sense ESD of 3500-5000V. However, a discharge of 300V is enough to destroy many components.

Assemblies and equipment containing ESD-sensitive parts are often as sensitive as the most sensitive part they contain. Protective circuitry in these assemblies and equipment provides varying degrees of protection from ESD applied to their terminals. Such assemblies and equipment, however, are still vulnerable to induced ESD caused by strong electrostatic fields or by contact of electrical connections or paths with a charged object.

Static damage is not always catastrophic. Sometimes a part slowly degrades, resulting in deteriorating performance. For example, internal resistance changes cause speed or voltage changes. Results include intermittent or latchup problems (for example, a line printer prints bad data).

When disassembling the computer, a portable conductive field service antistatic kit should be used to eliminate ESD when handling or temporarily setting aside ESD-sensitive parts. The kit contains a wrist strap, antistatic mat, and grounding cable.

Carefully observe the following procedures when disassembling the computer:

- Components, PC assemblies, finstrates, other assemblies and equipment should always be stored, transported, and shipped in antistatic or conductive containers.
- ESD-sensitive items must never be handled by ungrounded personnel, nor should they ever be stored on nonconductive surfaces or near nonconductive materials.
- Field support should keep all replacement PC assemblies and components in antistatic or conductive bags. The customer engineer should be grounded when working on products. A field service antistatic kit is available; it includes a static-free work station, ground cords, wrist straps, and board storage space. The failed board should be placed in a static-free bag for return to manufacturing site.
- Removal of ESD-sensitive devices from an assembly must be done at a static-safe work station using all precautions. Suspect or rejected components, PC boards, and subassemblies are to be treated with the same care as good devices. Otherwise, further damage may result which prevents tracing the cause of the original failure.
- Before removing devices from protective container:
    a. Clear work area of static hazards such as plastic cups, bags, envelopes, and papers.
    b. Connect wrist strap.
    c. Neutralize charges of ESD protective packaging containing an ESD-sensitive item and of tools by placing the packaged item on an ESD-grounded work bench surface to remove any charge prior to opening the packaging material. Alternately, charges can be removed by grounded personnel touching the package.
    d. Ensure that the computer is properly grounded before inserting ESD-sensitive items.
    e. Remove ESD-sensitive item from ESD protective packaging using finger or metal grasping tool only after grounding, and then place on the ESD-grounded work bench surface.
- Place PC boards, finstrates, and components on table mat when not in static-shielding bags or other protective containers.
- Clothing must never contact ESD-sensitive parts. Wrist strap does not bleed off charges from clothing.
- Personnel handling ESD-sensitive items should avoid physical activities which are static producing in the vicinity of those items. Such activities include wiping feet and removing or putting on jackets or sweaters.
- Where ground straps cannot be used, personnel should ground themselves prior to removing ESD-sensitive items from their protective packaging.
- Tools and test equipment used in ESD-protective areas should be properly grounded; hand tools should not contain insulation on the handles or, if used, tools with insulated handles should be treated with a topical antistat.
- Ensure that all containers, tools, test equipment, and fixtures used in ESD-protective areas are grounded before and during use either directly or by contacting with a grounded surface. Grounding of electrical test equipment should be via a grounded plug, not through the conductive surface of the ESD-grounded work station.
- Do not assume that insulators are fully discharged when placed on a conductive work surface. Once the insulator is lifted off the surface, it retains its charge.
- All PC boards and finstrates are to be handled only by grounded personnel. If possible, they should be held only by the ejectors. If necessary, they can be handled by the side edges.

Case Parts

The HP 9030 is the computer configured in a System II enclosure that can be installed in a system rack. The HP 9040 is the computer configured in a System II enclosure which is mounted in a stand-alone cabinet with casters, intended for use on any stable floor surface. Within the System II enclosure, the HP 9030 and HP 9040 are identical except for the service panel and cable. The HP 9030 service panel and cable are contained in the enclosure. In the HP 9040, the service panel is extended by cable to the cabinet frame. See the exploded view drawings in Chapter 5 when performing the following procedures.

HP 9030 (System II Enclosure)

The front panel is attached by four snap fasteners. To remove the front panel, grasp the panel by the side edges and pull straight out. The top, bottom, and side covers each have one #2 Pozidriv captive screw at the back of the box that attaches the cover to the box. To remove any cover, loosen the screw and slide the cover toward the back and away from the box.

HP 9040 (Stand-Alone Cabinet)

The stand-alone cabinet consists of an upper front panel, lower front panel, flip-top cover, and base assembly.

Upper Front Panel

The upper front panel is attached by four snap fasteners. Remove the panel by pulling it forward.

Lower Front Panel

The lower front panel is attached by two snap fasteners at the top and flanges engaged in slots in the base assembly at the bottom. Remove the panel by pulling it forward at the top and sliding it up and out of the base assembly.

Flip-Top Cover

The flip-top cover is held in place by four screws at the front of the cabinet and flanges in slots in the base assembly at the back. To remove the cover, first remove both front panels. Then remove the four screws that attach the front of the cover to the cabinet. Lift the cover at the front and tilt it backwards until it can be released from the back of the cabinet.

Replaceable Assemblies

The following procedures describe the removal of replaceable assemblies. The reassembly procedures are the reverse of the removal procedures. If specific procedures are required for reassembly they are provided.

The computer is in a System II enclosure (HP 9030) or a stand-alone cabinet (HP 9040). The procedures apply to both models with exceptions noted.

Note

References to top, bottom, right side, and left side covers are to the System II enclosure covers. Orientation is for a HP 9030 as viewed from the front (service panel end). When servicing a HP 9040, mounted in the stand-alone cabinet, realize that the System II enclosure is rotated 90 degrees counterclockwise. For example, a reference to a top cover actually refers to the left side cover of the cabinet-mounted HP 9040.

A list of the assemblies that have replacement procedures in this chapter follows:

- I/O Cards
- System Control Module
- Power Supply Assembly
- Processor Stack Finstrates
- Processor Stack Clock Board
- Processor Stack Motherboard
- Ac Power Cord
- Line Filter
- Power Switch
- Power Supply Cable
- Service Panel Board
- Service Panel Cable
- Processor Stack Fan
- Power Supply Fan
- I/O Fan
- Processor Stack Fan Cable
- Power Supply and I/O Fan Cable
- I/O Backplane
- Motherboard
- IOP Cable

See the exploded view drawings in Chapter 5 when performing the following procedures.

I/O Cards

1. SET THE POWER SWITCH ON THE REAR PANEL TO THE "0" POSITION AND DISCONNECT THE AC POWER CORD FROM THE WALL OUTLET.
2. Open I/O door on rear panel by turning both thumbscrews counterclockwise.
3. Disconnect I/O cable connector from I/O card to be replaced.

CAUTION

CAREFULLY HANDLE I/O CARD TO PREVENT DAMAGE TO CARD FROM ELECTROSTATIC DISCHARGE OR OTHER CAUSES. HOLD BY EJECTORS OR SIDE EDGES ONLY. DO NOT TOUCH EDGE CONNECTORS OR CARD PLANES. IMMEDIATELY PLACE CARD IN ANTISTATIC BAG OR ON ANTISTATIC SURFACE.

4. Pull out on card ejectors to release card from I/O backplane and slide card out of slot.

Note

Install replacement I/O card with ejectors out (extended). Seat card firmly in I/O backplane and push ejectors in to lock card in place.

System Control Module (SCM)

1. SET THE POWER SWITCH ON THE REAR PANEL TO THE "0" POSITION AND DISCONNECT THE AC POWER CORD FROM THE WALL OUTLET.
2. Remove both front panels and the flip-top cover as previously described (Model 40 only).
3. Remove the top cover from the System II enclosure as previously described.
4. Remove the I/O lid by releasing the ac module cable from the cable clamp and removing the four #2 Pozidriv screws that attach the I/O lid to the chassis.
5. Disconnect the service panel cable from the SCM.

CAUTION

CAREFULLY HANDLE SCM TO PREVENT DAMAGE TO MODULE FROM ELECTROSTATIC DISCHARGE OR OTHER CAUSES. HOLD BY EJECTORS OR SIDE EDGES ONLY. DO NOT TOUCH EDGE CONNECTORS OR MODULE PLANES. IMMEDIATELY PLACE SCM IN ANTISTATIC BAG OR ON ANTISTATIC SURFACE.

---

6. Pull out on ejectors to release SCM from motherboard and slide SCM out of slot.

Note

Install replacement SCM with ejectors out (extended). Seat module firmly in motherboard and push ejectors in to lock module in place.

Power Supply Assembly

WARNING

ENSURE THAT POWER SWITCH ON REAR PANEL IS SET TO "0" POSITION AND THAT AC POWER CORD IS DISCONNECTED FROM WALL OUTLET BEFORE REMOVING POWER SUPPLY. ALSO ENSURE THAT POWER SUPPLY CAPACITORS ARE COMPLETELY DISCHARGED AS DESCRIBED BELOW.

---

1. SET THE POWER SWITCH ON THE REAR PANEL TO THE "0" POSITION AND DISCONNECT THE AC POWER CORD FROM THE WALL OUTLET.
2. Remove both front panels and the flip-top cover as previously described (HP 9040 only).
3. Remove the top cover from the System II enclosure as previously described.

WARNING

WHEN POWER SUPPLY IS REMOVED FROM COMPUTER, YOU ARE EXPOSED TO LETHAL VOLTAGE FROM POWER SUPPLY CAPACITORS. DISCHARGE POWER SUPPLY CAPACITORS ACCORDING TO THE FOLLOWING STEPS. IF THE POWER SUPPLY DISCHARGE TOOL IS NOT AVAILABLE, WAIT AT LEAST 15 MINUTES AFTER REMOVING POWER FROM COMPUTER AND CONTINUE WITH STEP 8.

4. Familiarize yourself with the power supply discharge tool, HP PN 09855-67004, if you have not previously used it. The discharge tool consists of a meter and a switch-operated discharger. The meter indicates the approximate voltage across the energy storage capacitors in the power supply.

WARNING

WHEN PERFORMING THE NEXT STEP, ENSURE THAT NO METAL OBJECTS ARE IN YOUR HAND OR ON THE POWER SUPPLY. THE DISCHARGE TOOL PINS WILL HAVE HIGH VOLTAGE ACROSS THEM.

5. Carefully insert discharge tool pins directly into **SAFETY DISCHARGE** holes on top of power supply until tool rests on power supply lid. Little force is required if tool is straight when inserted. The meter gives an approximate indication of voltage across capacitors.

WARNING

ALTHOUGH THE DISCHARGE TOOL SWITCH CAN BE MOVED IN EITHER DIRECTION, THE TOOL DISCHARGES THE SUPPLY ONLY WHEN THE SWITCH IS PUSHED DOWN.

CAUTION

DO NOT USE DISCHARGE TOOL FOR MORE THAN TWO DISCHARGES IMMEDIATELY FOLLOWING ONE ANOTHER.

6. Push discharge tool switch down and hold down to discharge capacitors. Discharging takes a few seconds. Observe meter movement as switch is held down until capacitors are completely discharged.
7. Carefully remove discharge tool by pulling straight out of power supply.
8. Disconnect power supply cable from power supply.
9. Disconnect safety ground cable from lug on chassis.
10. Loosen four #2 Pozidriv captive screws that attach power supply to chassis.
11. Pull power supply straight out of chassis.

Processor Stack Boards

1. SET THE POWER SWITCH ON THE REAR PANEL TO THE "0" POSITION AND DISCONNECT THE AC POWER CORD FROM THE WALL OUTLET.
2. Remove the lower front panel (HP 9040) or the front panel (HP 9030).
3. From the front of the computer, remove the RFI shield by loosening the six thumbscrews.
4. If a board in slots 4-12 is being replaced, open stack door by loosening the two thumbscrews. If a board in slots 1-3 is being replaced, remove the stack door by loosening the two thumbscrews and the two #2 Pozidriv captive screws that attach the door to the stack.

CAUTION

CAREFULLY HANDLE BOARD TO PREVENT DAMAGE TO IT FROM ELECTROSTATIC DISCHARGE OR OTHER CAUSES. HOLD BY EJECTORS OR SIDE EDGES ONLY. DO NOT TOUCH EDGE CONNECTOR CONTACTS OR BOARD PLANES. IMMEDIATELY PLACE BOARD IN ANTISTATIC BAG OR ON ANTISTATIC SURFACE.

5. Pull out on board ejectors to release it from the stack motherboard and slide the board out of the slot. If IOP board is being removed, pull out on ejectors, slide board slightly out, open connector gate, remove ribbon cable connector, and then remove the board from stack.

Reassembly Notes

When installing board, hold by ejectors and use side edge of board to move air controller out of the way and onto the top of the board.

Insert board firmly in stack motherboard and push ejectors in to lock it in place.

Firmly tighten screws and thumbscrews on stack door and RFI shield to prevent RFI radiation.

Processor Stack Clock Board

1. SET THE POWER SWITCH ON THE REAR PANEL TO THE "0" POSITION AND DISCONNECT THE AC POWER CORD FROM THE WALL OUTLET.
2. Remove the lower front panel (HP 9040) or the front panel (HP 9030).
3. From the front of the computer, remove the RFI shield by loosening the six thumbscrews.
4. Loosen two captive thumbscrews on processor stack door and swing door open.

CAUTION

CAREFULLY HANDLE BOARD TO AVOID DAMAGE TO IT FROM ELECTROSTATIC DISCHARGE OR OTHER CAUSES. HOLD BY EJECTORS OR SIDE EDGES ONLY. DO NOT TOUCH EDGE CONNECTOR CONTACTS OR BOARD PLANES. IMMEDIATELY PLACE BOARD IN ANTISTATIC BAG OR ON ANTISTATIC SURFACE.

5. Remove boards in slots 5-12 by pulling out on ejectors to release it from stack motherboard and sliding boards out of slots.
6. Loosen two slotted captive screws that hold clock board to stack motherboard.
7. Disconnect clock board from processor stack motherboard at inline connector.
8. Pull clock board straight out of motherboard and out of stack.

Reassembly Notes

When installing board, hold by ejectors and use side edge to move air controller out of the way and onto the top of the board.

Insert board firmly in stack motherboard and push ejectors in to lock it in place.

The clock board connector and mating motherboard connector are not keyed; however, the clock board screws and motherboard holes do not align unless proper connection is made.

Firmly tighten screws and thumbscrews on stack door and RFI shield to prevent RFI radiation.

Processor Stack Motherboard

1. SET THE POWER SWITCH ON THE REAR PANEL TO THE "0" POSITION AND DISCONNECT THE AC POWER CORD FROM THE WALL OUTLET.
2. Remove both front panels and the flip-top cover as previously described (HP 9040), or remove front panel (HP 9030).
3. Remove the top cover from the System II enclosure as previously described.
4. From the front of the computer, remove the RFI shield by loosening the six thumbscrews.
5. Remove the stack door by loosening the two thumbscrews and the two #2 Pozidriv captive screws that attach the door to the stack.
6. Disconnect the ribbon cable(s) from the IOP finstrate(s).
7. Disconnect the service panel cable from the SCM.
8. Remove the four #2 Pozidriv screws that attach the processor stack lid to the chassis.

CAUTION

PERFORM THE FOLLOWING STEP CAREFULLY TO AVOID DAMAGING FAN CABLE OR CONNECTORS.

9. Lift stack and attached lid slightly, unplug fan cable from fan, and remove stack from box.

CAUTION

CAREFULLY HANDLE BOARDS TO AVOID DAMAGE FROM ELECTROSTATIC DISCHARGE OR OTHER CAUSES. HOLD BY EJECTORS OR SIDE EDGES ONLY. DO NOT TOUCH EDGE CONNECTOR CONTACTS OR BOARD PLANES. IMMEDIATELY PLACE THE BOARDS IN ANTISTATIC BAGS OR ON ANTISTATIC SURFACE.

10. Remove all boards by pulling out on ejectors to release the boards from the stack motherboard. Then slide the boards out of the slot.
11. Remove 16 #1 Pozidriv screws, 8 from the top of the case and 8 from the bottom, that attach the 4 card guides to the case, and remove the card guides.
12. Loosen two slotted captive screws that hold clock board to stack motherboard.
13. Disconnect clock board from processor stack motherboard at inline connector.
14. Pull clock board straight out of motherboard and out of stack.
15. Remove four #1 Pozidriv screws, two at top and two at bottom, that attach motherboard to case. Do not remove the two middle screws. They attach the motherboard supports to the motherboard.
16. Remove eight #1 Pozidriv screws, four at bottom and four at back, that attach the connector tie bar to the case.
17. Remove the motherboard and its attached supports and connector tie bar from the case.
18. Remove the connector tie bar and motherboard supports from the motherboard. Retain for installation on the replacement motherboard.

Reassembly Notes

Attach the connector tie bar to the case before attaching the motherboard to the case. This prevents connector misalignment.

The four card guides are identical; however, they must be replaced with flat ends up so the slots and connectors line up.

The clock board connector and mating motherboard connector are not keyed; however, the clock board screws and motherboard holes do not align unless proper connection is made.

When installing boards, hold by ejectors and use side edge to move air controller out of the way and onto the top of the board.

Insert board firmly in stack motherboard and push ejectors in to lock it in place.

Firmly tighten screws and thumbscrews on stack door and RFI shield to prevent RFI radiation.

Ac Power Cord

WARNING

AFTER REPLACING THE AC POWER CORD, PERFORM CONTINUITY TEST BETWEEN POWER CORD GROUND AND METAL CHASSIS. RECORD RESULTS ON REPAIR ORDER.

1. SET THE POWER SWITCH ON THE REAR PANEL TO THE "0" POSITION AND DISCONNECT THE AC POWER CORD FROM THE WALL OUTLET.
2. Remove both front panels and the flip-top panels as previously described (HP 9040 only).
3. Remove top cover from System II enclosure as previously described.
4. Remove the I/O lid by releasing the power supply cable from the cable clamp and removing the four #2 Pozidriv screws that attach the I/O lid to the chassis.
5. Remove the two nuts that attach the terminal block cover to the rear panel and remove the cover.
6. Disconnect the three line cord wires from the terminal block.
7. Snap out the line cord strain relief from the rear panel, and pull out line cord.

WARNING

THE REPLACEMENT CORD MUST HAVE THE SAME POLARITY AS THE ORIGINAL. OTHERWISE, A SAFETY HAZARD FROM ELECTRICAL SHOCK MIGHT EXIST WHICH COULD RESULT IN INJURY OR DEATH TO PERSONNEL.

Line Filter

WARNING

AFTER REPLACING THE LINE FILTER, PERFORM CONTINUITY TEST BETWEEN POWER CORD GROUND AND METAL CHASSIS. RECORD RESULTS ON REPAIR ORDER.

1. SET THE POWER SWITCH ON THE REAR PANEL TO THE "0" POSITION AND DISCONNECT THE AC POWER CORD FROM THE WALL OUTLET.
2. Remove both front panels and the flip-top panels as previously described (HP 9040 only).
3. Remove top and bottom covers from the System II enclosure as previously described.
4. Open I/O door on rear panel by turning both thumbscrews counterclockwise.
5. Disconnect I/O cable connectors from I/O cards.

CAUTION

CAREFULLY HANDLE I/O CARDS TO PREVENT DAMAGE TO CARDS FROM ELECTROSTATIC DISCHARGE OR OTHER CAUSES. HOLD BY EJECTORS OR SIDE EDGES ONLY. DO NOT TOUCH EDGE CONNECTORS OR CARD PLANES. IMMEDIATELY PLACE CARDS IN ANTISTATIC BAGS OR ON ANTISTATIC SURFACE.

6. Pull out on card ejectors to release cards from I/O backplane and slide cards out of slots.
7. Remove the I/O lid by releasing the power supply cable from the cable clamp and removing the four #2 Pozidriv screws that attach the I/O lid to the chassis.
8. Disconnect I/O door interlock cable connector from I/O backplane, and remove I/O door interlock switch from rear panel.
9. Remove both I/O card guides by pushing the two locating pins for each guide out of the casting while pulling the front of the guide toward the open door.
10. Disconnect the power supply cable from the power supply.
11. Remove the two nuts that attach the terminal block cover to the bottom of the rear panel, and remove the cover.
12. Loosen the four #2 Pozidriv screws that attach the terminal block to the rear panel until they clear the bottom of the rear panel. This allows the rear panel to be removed from the box unhindered by protruding screws.
13. Remove the eight #2 Pozidriv screws (four at the top and four at the bottom) that attach the rear panel to the enclosure, and slide the rear panel straight out.
14. Remove power switch cover by removing two #2 Pozidriv screws that attach cover to rear panel.
15. Disconnect three line filter wires from terminal block, and two line filter wires from power switch.
16. Remove four nuts and lockwashers that attach line filter to rear panel, and remove line filter.

Power Switch Assembly

WARNING

AFTER REPLACING THE POWER SWITCH, PERFORM CONTINUITY TEST BETWEEN POWER CORD GROUND AND METAL CHASSIS. RECORD RESULTS ON REPAIR ORDER.

1. SET THE POWER SWITCH ON THE REAR PANEL TO THE "0" POSITION AND DISCONNECT THE AC POWER CORD FROM THE WALL OUTLET.
2. Remove both front panels and the flip-top panels as previously described (HP 9040 only).
3. Remove top cover from System II enclosure as previously described.
4. Remove the I/O lid by releasing the power supply cable from the cable clamp and removing the four #2 Pozidriv screws that attach the I/O lid to the chassis.
5. Remove power switch cover by removing two #2 Pozidriv screws that attach cover to rear panel.
6. Remove two power supply cable wires from upper lugs of switch.
7. Remove two line filter wires from lower lugs of switch.
8. Push up on retaining snaps of switch while pulling out bottom of switch from outside of rear panel. While holding switch at angle, push down on upper retaining snaps, freeing switch. Pull switch out back of rear panel.

Power Supply Cable

WARNING

AFTER REPLACING THE POWER SUPPLY CABLE, PERFORM CONTINUITY TEST BETWEEN POWER CORD GROUND AND METAL CHASSIS. RECORD RESULTS ON REPAIR ORDER.

1. SET THE POWER SWITCH ON THE REAR PANEL TO THE "0" POSITION AND DISCONNECT THE AC POWER CORD FROM THE WALL OUTLET.
2. Remove both front panels and the flip-top panels as previously described (HP 9040 only).
3. Remove top cover from System II enclosure as previously described.
4. Disconnect power supply cable from power supply.
5. Remove the I/O lid by releasing the power supply cable from the cable clamp and removing the four #2 Pozidriv screws that attach the I/O lid to the chassis.
6. Remove power switch cover by removing two #2 Pozidriv screws that attach cover to rear panel.
7. Remove two power supply cable wires from upper lugs of switch, and remove power supply cable.

Service Panel Board

The HP 9030 and HP 9040 require different service panel board replacement procedures. Both are provided in the following paragraphs.

HP 9030

1. SET THE POWER SWITCH ON THE REAR PANEL TO THE "0" POSITION AND DISCONNECT THE AC POWER CORD FROM THE WALL OUTLET.
2. Remove front panel.

CAUTION

SERVICE PANEL CABLE IS CONNECTED TO BOARD BEHIND APPEARANCE PANEL, AND GROUND CABLE INTERCONNECTS BASE PLATE AND APPEARANCE PANEL. PERFORM NEXT THREE STEPS CAREFULLY TO PREVENT DAMAGE TO CABLE CONNECTORS OR BOARD.

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3. Remove four #2 Pozidriv screws (two on each side) that attach the appearance panel to enclosure.
4. Pull appearance panel out, tilt down from the top, and disconnect service panel cable from service panel board.
5. Disconnect ground cable that interconnects base plate and appearance panel from inside lower right of appearance panel.
6. Remove three #2 Pozidriv screws that attach service panel board to appearance panel, and remove board.

HP 9040

1. SET THE POWER SWITCH ON THE REAR PANEL TO THE "0" POSITION AND DISCONNECT THE AC POWER CORD FROM THE WALL OUTLET.
2. Remove both front panels and the flip-top cover as previously described.
3. Disconnect service panel cable from service panel board.
4. Remove three #2 Pozidriv screws that attach service panel board to appearance panel, and remove board.

Service Panel Cable

The HP 9030 and HP 9040 require different service panel cable replacement procedures. Both are provided in the following paragraphs.

HP 9030

1. SET THE POWER SWITCH ON THE REAR PANEL TO THE "0" POSITION AND DISCONNECT THE AC POWER CORD FROM THE WALL OUTLET.
2. Remove top cover and front panel.

CAUTION

SERVICE PANEL CABLE IS CONNECTED TO BOARD BEHIND APPEARANCE PANEL, AND GROUND CABLE INTERCONNECTS BASE PLATE AND APPEARANCE PANEL. PERFORM NEXT THREE STEPS CAREFULLY TO PREVENT DAMAGE TO CABLE CONNECTORS OR BOARD.

3. Remove four #2 Pozidriv screws (two on each side) that attach the appearance panel to enclosure.
4. Pull appearance panel out without straining ground cable, tilt down from the top, and disconnect service panel cable from service panel board.
5. Disconnect service panel cable from SCM, and remove cable.

HP 9040

1. SET THE POWER SWITCH ON THE REAR PANEL TO THE "0" POSITION AND DISCONNECT THE AC POWER CORD FROM THE WALL OUTLET.
2. Remove both front panels and the flip-top cover as previously described.
3. Disconnect service panel cable from service panel board.
4. Remove top cover from System II enclosure as previously described.
5. From the front of the computer, remove the RFI shield by loosening the six thumbscrews.
6. Disconnect service panel cable from SCM.
7. Remove four #2 Pozidriv screws (two on top and two on bottom) that attach appearance panel to enclosure.

CAUTION

DO NOT STRAIN GROUND CABLE WHEN PERFORMING FOLLOWING STEP.

8. Tilt appearance panel far enough to pull service panel cable out top of System II enclosure.

Processor Stack Fan

1. Remove processor stack from computer by performing steps 1 through 9 of the preceding Processor Stack Motherboard procedure.
2. Remove four 1/8-inch Allen screws that attach fan to stack, and remove fan.

Reassembly Note

Install replacement fan on stack with airflow direction arrow pointing in (toward stack) and plug receptacle in lower left corner of stack as viewed from fan end of stack.

Power Supply Fan

1. Remove power supply as described in the preceding Power Supply Assembly procedure.
2. Disconnect fan cable from power supply fan.
3. Remove right side cover from System II enclosure as previously described.
4. Remove four #2 Pozidriv screws that attach fan to computer, and remove fan.
5. Remove four clips at corners of fan and retain for installation on replacement fan.

Replacement Notes

Attach four clips to corners of fan before attempting to install fan in computer.

Install replacement fan in computer with airflow direction arrow pointing away from power supply and plug receptacle at upper right corner of fan (as viewed from right side of enclosure).

Ensure fan cable is not pinched when power supply is replaced.

I/O Fan

1. SET THE POWER SWITCH ON THE REAR PANEL TO THE "0" POSITION AND DISCONNECT THE AC POWER CORD FROM THE WALL OUTLET.
2. Remove both front panels and the flip-top cover as previously described (HP 9040 only).
3. Remove top and right side covers from System II enclosure as previously described.
4. Remove the I/O lid by releasing the ac module cable from the cable clamp and removing the four #2 Pozidriv screws that attach the I/O lid to the chassis.
5. Disconnect fan cable from I/O fan.
6. Remove four #2 Pozidriv screws that attach fan to computer, and remove fan.
7. Remove four clips at corners of fan and retain for installation on replacement fan.

Replacement Notes

Attach four clips to corners of fan before attempting to install fan in computer.

Install replacement fan in computer with airflow direction arrow pointing away from I/O cage and plug receptacle at lower left corner of fan (as viewed from right side of enclosure).

Processor Stack Fan Cable

The HP 9030 and HP 9040 require different processor stack fan cable replacement procedures. Both are provided in the following paragraphs.

HP 9030

1. SET THE POWER SWITCH ON THE REAR PANEL TO THE "0" POSITION AND DISCONNECT THE AC POWER CORD FROM THE WALL OUTLET.
2. Remove left side cover.

3. Disconnect cable from processor stack fan.
4. Disconnect cable from motherboard, and remove cable.

HP 9040

1. Remove processor stack from computer as described in steps 1 through 9 of the preceding Processor Stack Motherboard procedure.
2. Disconnect cable from motherboard, and remove cable.

Power Supply and I/O Fan Cable

1. Perform steps 1 through 14 of the Motherboard procedure which follows in this chapter.
2. Disconnect cables from power supply and I/O card cage fans.
3. Pull power supply fan cable plug out of cutout in bottom of power supply bucket.

I/O Backplane

1. SET THE POWER SWITCH ON THE REAR PANEL TO THE "0" POSITION AND DISCONNECT THE AC POWER CORD FROM THE WALL OUTLET.
2. Remove both front panels and the flip-top cover as previously described (Model 40 only).
3. Remove top cover from the System II enclosure as previously described.
4. Open I/O door on rear panel by turning both thumbscrews counterclockwise.
5. Disconnect I/O cable connectors from I/O cards.

CAUTION

CAREFULLY HANDLE I/O CARDS TO PREVENT DAMAGE TO CARDS FROM ELECTROSTATIC DISCHARGE OR OTHER CAUSES. HOLD BY EJECTORS OR SIDE EDGES ONLY. DO NOT TOUCH EDGE CONNECTORS OR CARD PLANES. IMMEDIATELY PLACE CARDS IN ANTISTATIC BAGS OR ON ANTISTATIC SURFACE.

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6. Pull out on card ejectors to release cards from I/O backplane and slide cards out of slots.
7. Remove the I/O lid by releasing the ac module cable from the cable clamp and removing the four #2 Pozidriv screw that attach the I/O lid to the chassis.
8. Disconnect I/O door interlock cable connector from I/O backplane, and remove I/O door interlock switch from rear panel.
9. Remove both I/O card guides by pushing the two locating pins for each guide out of the casting while pulling the front of the guide toward the open door.
10. Remove the nine #2 Pozidriv screws that attach the I/O backplane to the support plane.
11. Grasp I/O backplane by side edges, rock it gently back and forth to release from motherboard connector, and lift it straight up and out of enclosure.

Reassembly Note

Install I/O door interlock switch while holding it as close as possible to I/O door. Otherwise switch will not function.

Motherboard

Note

To replace the motherboard in the HP 9040, first remove the System II enclosure from the base assembly. The first 7 steps that follow describe this procedure. To replace the HP 9030 motherboard, begin with step 1 and then skip to step 8.

1. SET THE POWER SWITCH ON THE REAR PANEL TO THE "0" POSITION AND DISCONNECT THE AC POWER CORD FROM THE WALL OUTLET.
2. Remove both front panels and the flip-top cover as previously described.
3. Disconnect service panel cable from service panel board.
4. Remove four bolts and nuts (two on each side) that attach support bracket to service panel bracket.
5. Remove the two screws at lower front and two screws at lower back that secure System II enclosure in base assembly.
6. Lift System II enclosure out of base assembly.
7. Remove the two screws that attach the support bracket to the enclosure, and remove the bracket.
8. Remove all four covers (top, bottom, and both sides) from System II enclosure as previously described.
9. Remove processor stack, power supply, SCM, and I/O backplane as described in preceding procedures.
10. Disconnect IOP cable from motherboard.
11. Disconnect both fan cables from motherboard.
12. If one or two additional IOP cables are in place, disconnect cables at IOP finstrates and remove IOP cable strain relief clamp from bottom of base plate, freeing cables.
13. Remove eight #2 Pozidriv screws (four on each side) that attach base plate to enclosure.
14. Pull base plate with attached motherboard out bottom of enclosure.
15. Remove nine #2 Pozidriv screws that attach motherboard to base plate, and remove motherboard.

IOP Cable

1. Perform preceding Motherboard procedure.
2. Remove four #2 Pozidriv screws that attach IOP cable strain relief clamp to base plate, remove clamp, and remove cable.

Table of Contents

Replaceable Parts

Chapter 5

Introduction

This chapter lists all of the replaceable parts in the computer and provides information required to order replacement parts. The information is divided into the following sections:

- Exchange Parts
- Non-Exchange Parts
- Parts List

Any part number is located by using the parts list. All parts listed can be ordered from the Corporate Parts Center except for exchange assemblies, which are ordered from the Computer Support Division.

Exchange Parts

The computer is repaired at an assembly replacement level. Items most commonly replaced are exchange parts and are on the Computer Support Division (CSD) exchange program. When an exchange part fails, it should be returned to CSD for repair, and a rebuilt part should be obtained for the defective computer. Table 5-1 lists the exchange parts for the computer.

Table 5-1. Exchange Parts

New Part Number	Rebuilt Part Number	Description
09855-67980	09855-69980	Power Supply Assembly
5061-6803	97043-69803	Floating Point CPU
5061-6805	97047-69805	512K RAM Board
5061-7704	97046-69704	IM RAM Board
09955-66510	09955-69510	System Control Module

Non-Exchange Parts

Table 5-2 lists the module-level non-exchange parts for the computer.

Table 5-2. Non-Exchange Parts

Part Number	Description
09955-66500	Motherboard
09955-66511	Service Panel Board
09955-66501	I/O Backplane
5061-4224	Processor Stack Clock Board
5061-4225	IOP Finstrate
5061-4228	IOP Buffer Assembly
97043-69235	CPU Finstrate
5061-4232	256K RAM Board
3103-0377	Fan

Parts List

Figures 5-1 and 5-2 show all the computer modules and their attaching parts. Each of the figures has an associated parts list. The parts list provides the HP part number, description, and quantity of each part identified on the figure with an index number.

The **Index Number** in the parts list corresponds to the part in the figure identified by the same number.

The **Part Number** is the HP part number for the identified item. If no part number is provided, refer to the bulleted items which follow in the list for the specific part required. I/O card part numbers are card specific and are not provided here.

Bulleted items in the **Item Description** column either indicate subordinate parts under a higher level assembly or specific parts where only one is needed (for example, 7 power cords are listed).

A/R in the **Total Qty** column means "as required".

Table 5-3. Parts List (Figure 5-1)

Index Number	Part Number	Item Description	Total Qty
1		Front Panel, HP 9040	1
	1600-1318	• Window Clamp	1
	4114-0991	• Window	1
	5041-3470	• Window Frame	1
	0701-0715	• Upper Front Panel	1
	1600-1315	• Beltline Strip	1
2	07908-00002	Lower Front Panel, HP 9040	1
3	09955-67902	Flip-Top Cover, HP 9040	1
*4	5061-9436	Top Cover (System II)	1
*5	5061-9448	Bottom Cover (System II)	1
*6	5061-9523	Side Cover, Perforated (System II)	2
7	1600-1314	RFI Shield, HP 9040	1
8	1600-1300	Service Panel Bracket, HP 9040	1
9	09955-66511	Service Panel Board	1
	3101-2524	• Switch Assembly (4 switches)	1
	5041-0368	• Keycap	4
10	1600-1301	Support Bracket, HP 9040	1
11	1600-1299	Air Filter Frame, HP 9040	1
12	7121-3730	Air Filter, HP 9040	1

* These parts have been changed from "inch" to "metric". You may need to obtain metric hardware when replacing these parts.

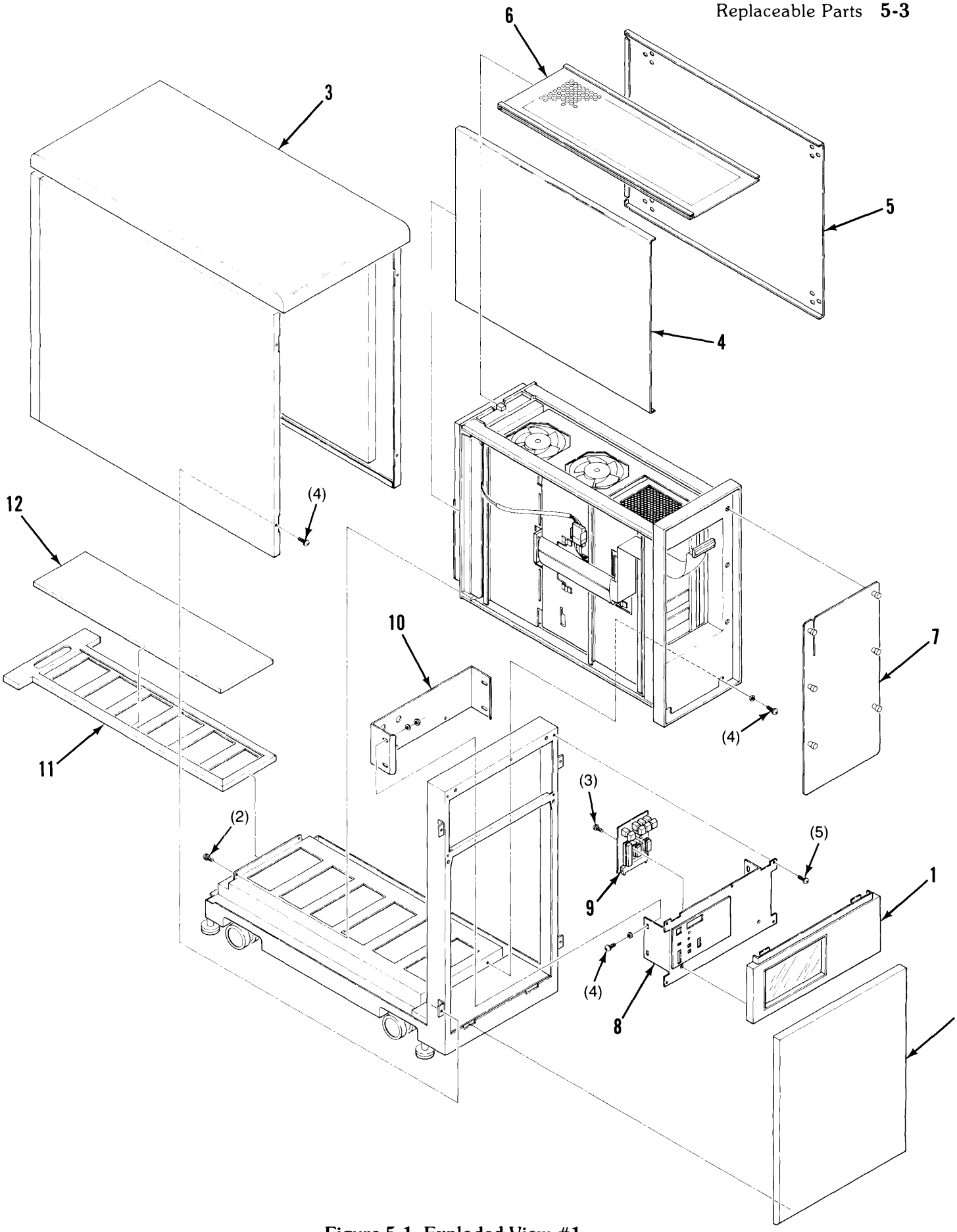


Figure 5-1. Exploded View #1

Table 5-4. Parts List (Figure 5-2)

Index Number	Part Number	Item Description	Total Qty
1		Front Panel, HP 9030	1
	1600-1318	• Window Clamp	1
	4114-0991	• Window	1
	5041-3470	• Window Frame	1
	7101-0702	• Cosmetic Panel	1
2	1600-1298	RFI Shield, HP 9030	1
3	7101-0701	Appearance Panel	1
4	09955-66511	Service Panel Board	1
	3101-2524	• Switch Assembly (4 switches)	1
	5041-0368	• Keycap	4
5	1600-1287	Processor Stack Lid	1
6		Processor Stack	1
7	97043-69235	• CPU Board	A/R
	5061-6803	• Floating Point CPU Board (New)	A/R
	97043-69803	• Floating Point CPU Board (Exchange)	A/R
	5061-6806	• IOP Board (Rev.3.1)	A/R
	5061-4228	• IOP Buffer Assembly	1
	09855-69232	• 256K RAM Board	1
	5061-6805	• 512K RAM Board (New)	1
	97047-69805	• 512K RAM Board (Exchange)	1
	5061-7704	• IM RAM Board (New)	1
	97046-69704	• IM RAM Board (Exchange)	1
8	5061-4224	• Processor Stack Clock Board	1
9	1460-1981	• Spring	2
10	4040-2114	• Air Controller	1
11	4040-2115	• Controller Pivot	1
12	5061-4264	• Processor Stack Door	1
13	3160-0377	• Processor Stack Fan	1
14	8120-3790	• Processor Stack Fan Cable	1
15	8120-4016	Service Panel Cable	1
16	09855-69980	Power Supply Assembly	1
17	3160-0377	Power Supply Fan	1
18	1600-1286	I/O Lid	1
19	09955-69510	System Control Module	1
	1420-0302	• Battery Assembly, 4.8V	1
20	09955-66501	I/O Backplane	1
21	0403-0466	I/O Card Guide	2
22	Cd Specific	I/O Card	A/R
23	3160-0377	I/O Fan	1
24	8120-3787	Power Supply and I/O Fans Cable	1
25	1600-1331	Terminal Block Cover	1

Table 5-4. Parts List (Figure 5-2), Continued

Index Number	Part Number	Item Description	Total Qty
26		Power Cord	1
	09855-61600	• U.S.A., 110V	
	09855-61605	• Great Britain	
	09855-61601	• Australia	
	09855-61602	• Europe	
	09855-61603	• U.S.A., 220V	
	09855-61604	• Switzerland	
	09855-61606	• Denmark	
27	9135-0177	Line Filter	1
28	1600-1312	Power Switch Assembly Cover	1
29		Power Switch Assembly	1
	09955-61901	• 110V	
	09955-61902	• 220V	
30		Power Supply Cable	1
	8120-3764	• 110V	
	8120-3763	• 220V	
31	3101-2565	I/O Door Interlock Switch	1
32	8120-4043	I/O Door Interlock Cable	1
33	7101-0704	Rear Panel	1
34	7101-0703	Base Plate	1
35	09955-66500	Motherboard	1
36	1600-1316	IOP #1 Cable Strain Relief Clamp	1
37	8120-4015	IOP #1 Cable	1
38	1600-1316	IOP #2 or #3 Cable Strain Relief Clamp	1
39	8120-4058	IOP #2 or #3 Cable	1

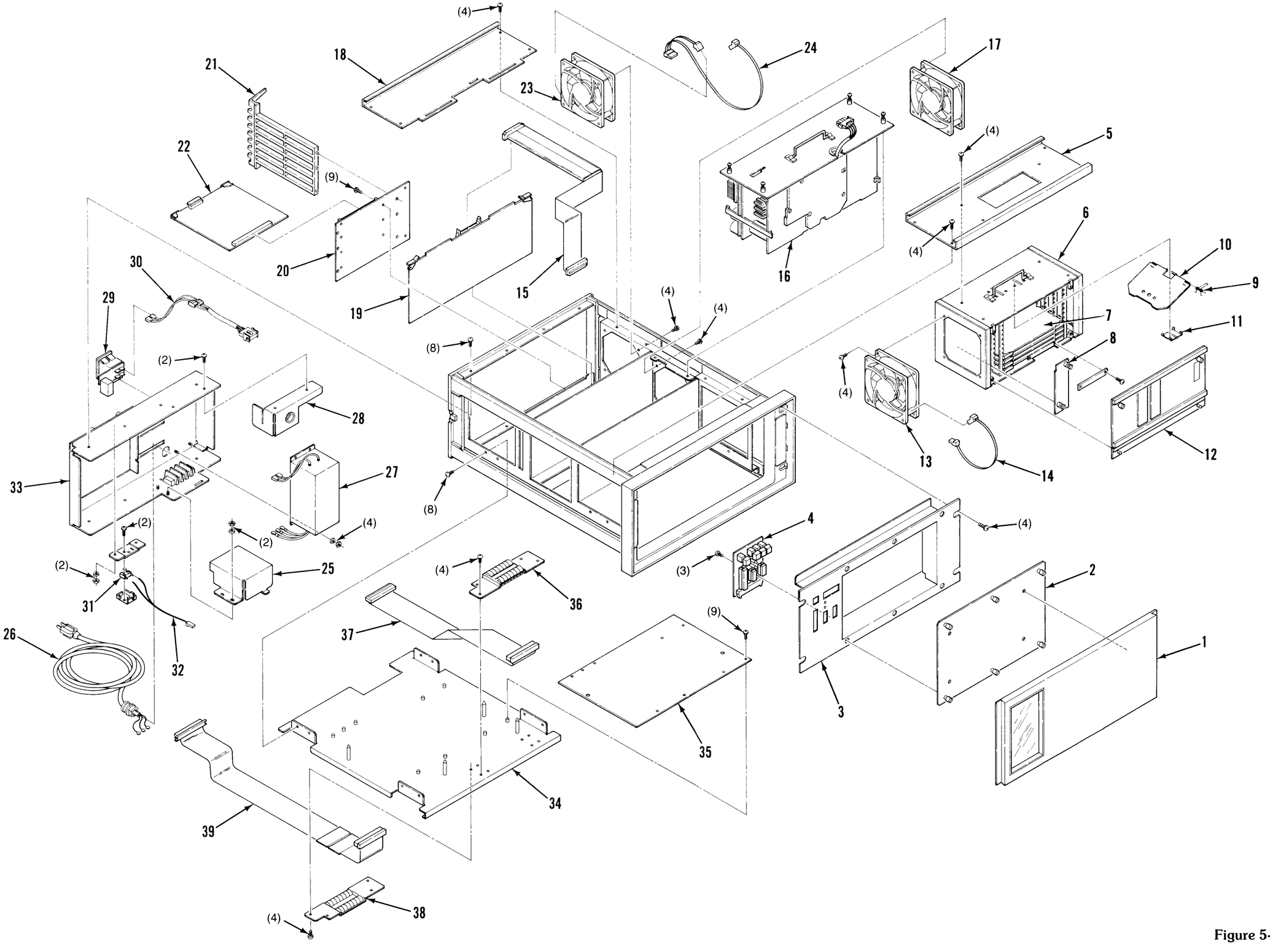
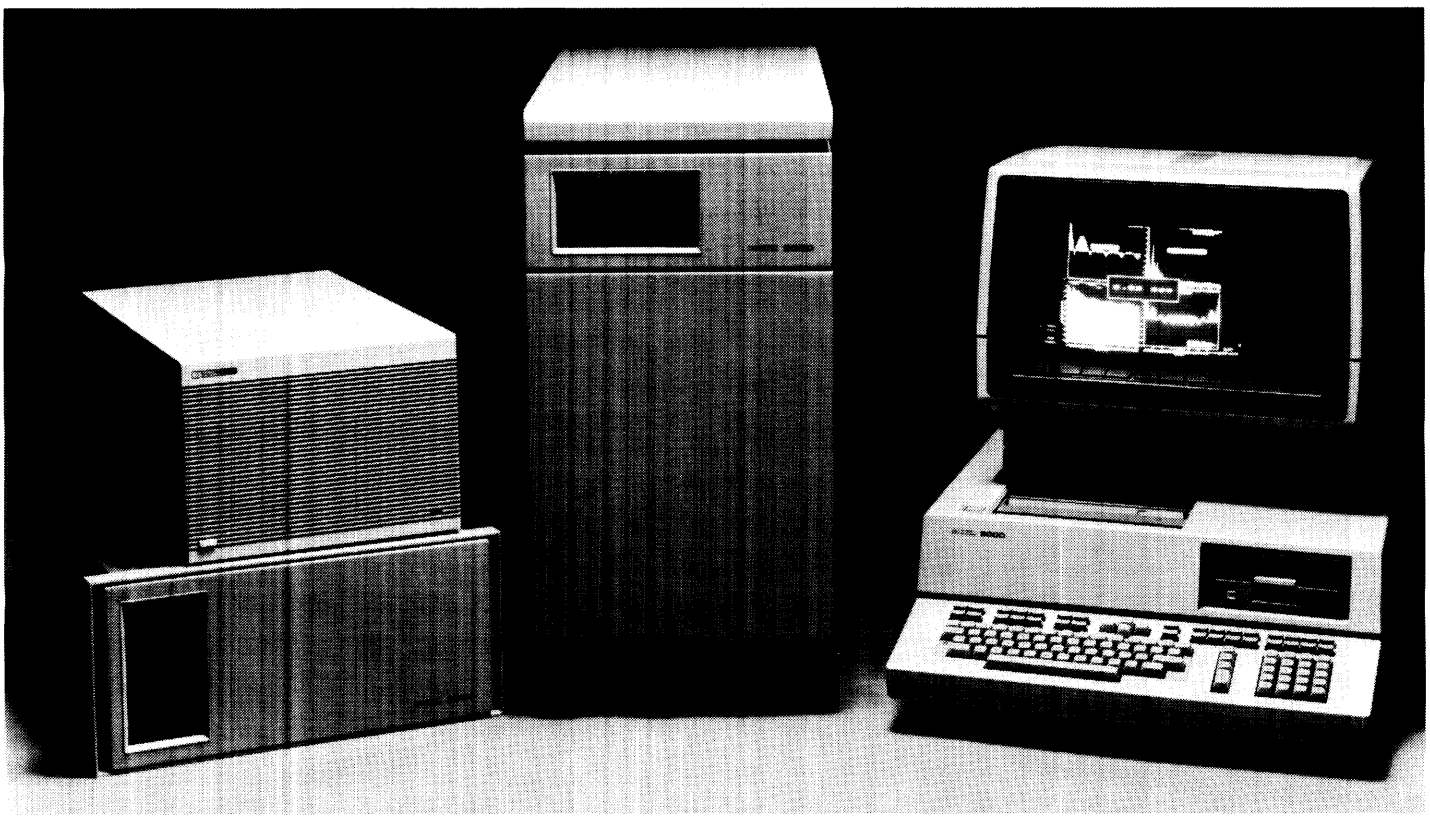


Figure 5-2. Exploded View #2

HP 9000 Series 500 Computers Models 520, 530, 540, 550 Hardware Technical Data

HEWLETT PACKARD

Effective: January 1, 1985*



Introduction

The HP 9000 Series 500 is a family of powerful 32-bit computers for scientific and engineering applications offering a variety of configurations – from integrated or modular workstations to multi-user systems. With the Series 500, Hewlett-Packard displays a major breakthrough in microprocessor technology by packaging a complete 32-bit processor in a single integrated circuit. This technology gives the Series 500 a significant price/performance improvement over traditional computer systems and eliminates the need for a 32-bit technical computer to operate in a temperature controlled environment. The result is a viable solution for personal, 32-bit engineering computation.

The Series 500 offers tremendous flexibility in configuring systems to solve a wide range of problems. The Model 550 is a powerful multi-user system in a compact size (13 inches wide x 9 inches high x 21 inches deep) designed for ease of use. As part of the HP "Design Plus Family", its standard size is compatible with a growing set of HP peripherals and furniture. It can be stacked in a taboret, a handy cabinet on wheels that easily rolls under a desk, or it can be used stand-alone, placed in a mini-rack or on a CAD worktable. The Model 520 is an integrated workstation with keyboard, printer, mass storage and graphics display all mounted in a desktop configuration. Or you have your choice of either a rack-mountable box (Model 530) or a mini-cabinet (Model 540) that permits selection of only those peripherals you need.

The Model 520 lets you choose between a UNIX† operating system (HP-UX) or HP's BASIC Language System. The HP BASIC system is single-user only while the HP-UX system offers single- or multi-user versions. The Model 530, 540 and 550 offer only the HP-UX system.

* *Data subject to change.*

† *UNIX is a trademark of AT&T Bell Laboratories, Inc.*

System Architecture

There are four main components in the Series 500 processor: the Central Processing Unit (CPU) chip, a 128 Kbit Random Access Memory (RAM) chip, a 256 Kbit Dynamic RAM (DRAM) chip, and an I/O Processor (I/OP) chip. These four components communicate via a common Memory-Processor Bus (MPB) and are the result of an advanced photolithography process that can achieve 1.5 micron devices with 1 micron spacings. This NMOS process was designed specifically to produce the high performance integrated circuits for the Series 500.

The chip set has self-test logic which automatically tests 99% of its devices at power-up.

The CPU, I/O Processor and RAM Boards are installed in a card cage called the Memory/Processor Module (M/PM). The cards are interconnected within the Module by a 36 Mbyte/sec. Memory Processor Bus.

Central Processor Unit

The Series 500 CPU features the following:

- A 32-bit, single-chip microprocessor comprised of 450,000 transistors based on a stack architecture.
- Three floating point math chips to provide superior performance.
- A direct address range of 500 Mbytes.
- An instruction set consisting of 230 operation codes implemented in a 9 K x 38-bit ROM control store. The set provides operations for stack manipulation, code/data segmentation, shared code in memory and I/O processing.
- An 18 MHz clock rate and a 55 nsec. micro-instruction cycle time.
- In conjunction with the memory controllers, a scheme of overlapped memory cycles ("pipelining") is implemented in the hardware. The result is a memory cycle time of 110 nsec.
- Series 500 typical execution times:

Load register from memory	550 nanoseconds
64 bit floating point multiply	1.28 microseconds
32 bit integer multiply	2.92 microseconds
64 bit floating point add	1.17 microseconds

The unique architecture of the HP 9000 Series 500 family allows multiple processors to work simultaneously – each sharing the workload by taking on the next available task. You can add up to two additional CPUs to the standard Series 500 for a total of three. Adding these CPUs is simply a matter of plugging in another CPU Finstrate board (done by an HP Customer Engineer). It does not require any operating system or software changes. And you can tune your task distribution to take full advantage of multiple CPUs.

Memory

The Series 500 Random Access Memory offers the following set of features:

- Each RAM Board has a Memory Controller (MC) chip that interfaces the RAM chips to the Memory Processor Bus and performs error detection/correction.
- Each memory address contains 32 bits for data and 7 bits to store a Hamming code which gives each Memory Controller the ability to locally detect and correct all single-bit errors and detect all double-bit errors and most multi-bit errors.
- The Series 500 memory utilizes overlapped memory cycles. With current technology, all models of the Series 500 can have up to 10 Mbytes of RAM.

During power-up of the Series 500, the system tests all of its memory by reading and writing various data patterns into each memory location. During this process, if any double-bit errors occur or if too many single-bit errors are detected, a block of memory containing the defective locations is mapped out by the Memory Controller with no loss of system integrity.

In addition to its power-up memory test, the Series 500 will correct any single-bit errors that occur during subsequent memory accesses. Double-bit or multi-bit errors are also detected.

I/O Processors

The I/O Processor (I/OP) is a microprogram-controlled interface between the Series 500's Memory Processor Bus and 8 I/O interface channels. The I/OP can handle direct CPU I/O, generate CPU interrupts and conduct simultaneous, independent Direct Memory Access transactions on all 8 I/O channels.

The modular design of the I/OP permits multiple I/OPs to reside on the Memory Processor Bus and function independently. To utilize the additional I/O channels of a second or third I/OP, an HP 97098A I/O Expander must be cabled to each I/OP.

Features

- Each I/OP supports 8 channels of I/O with Direct Memory Access capability on every channel.
- Up to three I/OPs and their associated 97098A I/O Expanders are supported on Models 520, 530 and 540; up to two with the Model 550.
- Nominal I/OP bandwidth = 900 Kbytes/sec. (multi-plexed across several channels).

Specifications

Model 520

The Series 500 Model 520 is a highly integrated, 32-bit engineering computer that features a keyboard, a choice of mass storage devices (removable media), three different CRT displays and up to 10 Mbytes of RAM in a single workstation package.

System Components

Component	Base Systems			Bundled Systems	
	9020A	9020B	9020C	9020AS	9020AT
CRT	Standard Color	Monochrome (green)	High Performance Color	Standard Color	Standard Color
Keyboard	ASCII is standard, others are available				
RAM (std.)	512 Kbyte			1 Mbyte	1.5 Mbyte
RAM (opt.)	Up to 10 Mbytes in 2 Mbyte increments or up to 5 Mbytes in 512 Kbyte increments				
Mass Storage	5¼" Flexible Disc Standard, 10 Mbyte Fixed Disc Optional			5¼" Flexible Disc *and* 10 Mbyte Fixed Disc	5¼" Flexible Disc Standard, 10 Mbyte Fixed Disc Optional
Thermal Printer	Optional			Standard	
CPU Options	Single is standard, up to 2 additional CPUs are allowed				
I/O Options	Single is standard, up to 2 additional I/O Processors with I/O Expanders allowed				
System Software	BASIC (single-user is standard) HP-UX (single-user is standard, multi-user is optional)			HP BASIC	HP-UX (single-user only) with FORTRAN, C and Pascal compilers, and Graphics

Physical Specifications

Width . . . . . 21.75 in. (55.2 cm)
Depth . . . . . 29 in. (73.6 cm)
Height . . . . . 24.5 in. (62.2 cm)
Net Weight:
9020A/R . . . . . 137 lbs. (62.1 kg)
9020B/S . . . . . 121 lbs. (55 kg)
9020C/T . . . . . 163 lbs. (74 kg)
Shipping Weight:
9020A/R . . . . . 168 lbs. (76.2 kg)
9020B/S . . . . . 152 lbs. (69 kg)
9020C/T . . . . . 194 lbs. (88 kg)
Temperature:
Operating . . . . . 10° to 40°C (w/disc media)
Storage . . . . . −40° to 75°C (flexible disc media excluded)
Slew Rate* . . . . . 10°C per hour
Humidity . . . . . 20 − 80% RH non-condensing (max. wet bulb, 25.5°), machine operating
Altitude . . . . . 15,000 ft. (570 mbars barometric pressure), machine operating
Voltage Ranges . . . . . 90 − 125 Vac or 189 − 250 Vac
Line Frequency Range . . . . . 48 − 66 Hz
Current Requirements† . . . . . 12.0 A at 108 Vac
8.0 A at 198 Vac
15.0 A at 90 Vac (Japan)
Power Dissipation . . . . . 850 Watts (2900 BTU/hr.)

* *Specification refers only to 10 MByte Internal Fixed Disc.*
† *If the Model 520 includes the High-Performance Color Display, the display will draw a maximum additional 6 A at 88 Vac or 3 A at 198 Vac.*

CRT Display Specifications

	Standard Color	High-performance Monochromatic	High-performance Color
Screen size (diagonal)	12.2 in.(310mm)	12.2 in. (310mm)	13 in. (330mm)
Screen brightness	50 Hz = 27 ft.-Lamberts 60 Hz = 31 ft.-Lamberts	To 30 ft.-Lamberts	To 30 ft.-Lamberts
X-ray emission	<0.5 mR/hr.	<0.5 mR/hr.	<0.5 mR/hr.
Refresh rate	50 or 60 Hz	60 Hz	60 Hz
Maximum altitude	15,000 ft.	15,000 ft.	15,000 ft.
Screen capacity	26 lines x 80 characters	26 lines x 80 characters	26 lines x 80 characters
Dot spacing	.017 in. (.428mm)	.013 in. (.328mm)	.013 in. (.343mm)
Character matrix	7 x 9 character in a 9 x 12 cell	7 x 9 character font in a 9 x 12 cell	7 x 9 character font in a 9 x 12 cell
Graphics			
No. of colors	16 displayed from 4,096	Monochrome	8 pure, 4,913
Raster size	8.5 in. x 6.4 in. (216 x 162.5mm)	7.24 in. x 5.86 in. (184 x 149mm)	7.55 in. x 6.14 in. (192 x 156mm)
Array size	512 x 390 dots	560 x 455 dots	560 x 455 dots
Dot resolution	.017 in. (.42mm)	.013 in. (.33mm)	.013 in. (.34mm)
Linearity	<3.0% full screen	1.5% full screen	<2% full screen
Cursor			
Plotting mode	Full screen or small crosshair	Full screen, small crosshair or blinking underline	Full screen or small crosshair
Letter mode	None	Blinking underline	Blinking underline
Character editing	Overstrike	Overstrike	Overstrike
Light Pen			
Min. intensity for pick of single pixel	N/A	10 ft.-Lamberts (white, blue, or green)	10 ft.-Lamberts (white, blue, or green)
Convergence	0.7mm, user adjustable	0.7mm, user adjustable	0.7mm, user adjustable

Internal Thermal Graphics Printer Specifications

The Series 500 Model 520 internal printer offers the following features:

- True overprinting.
- Printing enhancements such as inverse (white characters on black), underline, overline and 150% tall in any combination.
- Capability to dump graphics from CRT (pixel-by-pixel). BASIC only.
- Seven user-definable characters.
- Standard character sets are: US ASCII and Line Drawing, HP Roman Extension or Katakana.
- Programmable vertical pitch, lines per page and top/bottom margin.

Line width . . . . . 80 columns
Print speed . . . . . Up to 450 lines/min.
Character sets . . . . . Roman Extension or Katakana
Graphics resolution . . . . . 560 dots/line, 77 dots/in. (vert. and horiz.)
Plot speed:
Nominal plot . . . . . .49 in./sec. (12.5mm/sec.)
Plot all pixels on . . . . . .15 in./sec. (3.8mm/sec.)
Character matrix . . . . . 5 x 7 dots (7 x 12 field)
Paper dimensions . . . . . 8.27 in. x 197 ft. (210mm x 60m)
8.5 in. x 200 ft. (216mm x 61m)
Paper types . . . . . Black or blue print, perforated, fan fold, 330 sheets per pkg.

Note: *The Series 500 Model 520 printer is designed to print approximately 50,000 ft. of paper prior to print head replacement. The actual print head life will vary, however, with usage. If you expect to do a lot of printing, we recommend that you consider purchasing a heavy duty printer such as one of the HP impact printers.*

Internal Flexible Disc Specifications

Capacity . . . . . 270,336 bytes user available (formatted), less file directory allocation
Media . . . . . 5.25 in. (133mm) double-sided/double density disc
Average media life . . . . . More than 2.5 million revolutions (140 hrs. rotating)‡, stops when not accessed
Tracks per disc . . . . . 70 total, 35 per side, 66 user available
Sectors per track 16
Bytes per sector 256
Average access time . . . . . 300 msec.
Max. access time . . . . . 425 msec. (assumes no data errors)
Average throughput . . . . . 16 Kbytes/sec. (interleave factor of 1)

‡ *The internal disc drive is intended for program and data storage with a duty cycle of less than 25%. Greater duty cycles may reduce media life.*

Internal Fixed Disc Specifications

Capacity . . . . . 9.896 Mbytes (formatted), less directory file allocations
No. of platters 2
No. of tracks . . . . . 1224 (306 cylinders x 4 heads); 1208 user available
Sectors per track 32
Bytes per sector 256
Average access time . . . . . 85 msec.
Max. access time . . . . . 205 msec. (assumes no errors detected)
Average throughput . . . . . 115 Kbytes/sec. (interleave factor of 4)

Model 520 Keyboard Options

The following keyboards and character sets are available for the Series 500:

ASCII (standard)	Spanish	Katakana
French	German	Swedish/Finnish

Real Time Clock

The Series 500 Real Time Clock offers the following set of features:

- Accuracy to within 45 ppm over the range 0°C – 45°C. Note: 45 ppm is approximately 2 min./month.
- A "keep alive" time of 30 days (nominal) and 10 days (worst case).
- Provides date and time of day.

Models 530, 540 and 550

The Models 530 and 540 use the same Memory Processor Module as the Model 520 but they are packaged in either an HP System II rack-mount enclosure or in a stand-alone mini-cabinet. The Model 550 is housed in a small package, 325 mm wide. Modular packaging is useful for workstations and multi-user applications that have specific peripheral requirements.

System Components

	Base Systems			Bundled Systems			
	9030A	9040A	9050A	9040AT	9040AM	9050AT	9050AM
RAM (Std.)	512 Kbyte			1.5 Mbyte			
RAM (Opt.)	Up to 10 Mbytes in 2 Mbyte increments or up to 5 Mbytes in 512 Kbyte increments						
Service/ Diagnostic Panel	Standard						
CPU Options	Single is standard; up to two additional CPUs are allowed.						
I/O Options	Models 9030/9040 – Up to two additional I/O Processors (IOP) allowed. Model 9050 – Up to one additional I/O Processor. Each IOP adds eight DMA-capable I/O slots.						
System Software	Optional (HP-UX)			HP-UX plus additional software options and compilers (single-user)	HP-UX plus additional software options and compilers (multi-user)	HP-UX plus additional software options and compilers (single-user)	HP-UX plus additional software options and compilers (multi-user)

Physical Specifications

	Model 9030 System II Enclosure*	Model 9040A Stand-alone Mini-cabinet	Model 9050 Standard 325 mm Width
Width	17 in. (43.2 cm)†	14 in. (35.6 cm)	12.8 in. (32.5 cm)
Depth	23.0 in. (58.4 cm)	28.0 in. (71.1 cm)	20.9 in. (53.0 cm)
Height	8.75 in. (22.2 cm)	28.0 in. (71.1 cm)	9.2 in. (23.4 cm)
Shipping weight (typical)	65 lbs. (29.4 kg.)	141 lbs. (51.6 kg.)	40 – 60 lbs. (18 – 27 kg.)

* *Industry standard EIA mounting.*

† *Add 2 in. (7.6 cm) for rack-mount "ears".*

Temperature
Operating . . . . . 0° to 55°C
Storage . . . . . –40° to 75°C
Humidity . . . . . 95% RH at 40°C, machine operating
Altitude . . . . . 15,000 ft. (570 mbars barometric pressure), machine operating

Frequency range . . . . . 48 – 66 Hz
Vibration (peak-to-peak amplitude deflection) . . . . . .125 in. at 5 to 10 Hz
.060 in. at 10 to 25 Hz
.015 in. at 25 to 55 Hz

	Model 9040/9030	Model 9050
Current requirements/ Voltage ranges	90 – 125 Vac, 11A 198 – 250 Vac, 5.5A	90 – 108 Vac, 9A 108 – 125 Vac, 7.6A 198 – 250 Vac, 4.3A
Maximum power dissipation	650 Watts (2200 Btu/hr.)	580 Watts (220 Btu/hr.)

Series 500 I/O

The Series 500 I/OP communicates to external devices through a specially designed I/O channel and interface cards. This combination of I/O Processors, I/O channel and interface cards conforms to the HP channel I/O (HP-CIO) standard.

These interface cards can receive and transmit data in multiple-word "bursts." The I/OP also communicates with the Series 500 CPU in this fashion. These "bursts" permit communication overhead to be spread over a number of data words thereby increasing the capacity of the system to handle half-word or byte-oriented I/O transactions.

HP-IB (HP 27110A)

The HP-IB Interface Card for the Series 500 allows connection of up to 14 HP-IB compatible devices. These devices include flexible and hard discs, printers, plotters, magnetic tape drives, tablets and an extensive list of instruments.

Features

- IEEE-488-1978 compatible.
- Supports DMA with two modes of performance: High Speed Mode for operation with fixed discs or other high speed peripherals and Medium Speed for instruments and slower peripherals.
- Supports up to 7 high-speed devices or 14 standard-speed devices.
- Selectable HP-IB controller or slave capabilities and parallel poll capabilities.
- Built-in hardware self-test.

Operation

Eight bidirectional data bus lines carry coded messages in bit-parallel, byte-serial form to/from other devices on the bus with each byte transferred from one "talker" to one or more "listeners." Data is exchanged asynchronously using interface messages to set up, maintain and terminate an orderly flow of device-dependent messages. Three data transfer control lines control the transfer of each byte of coded data on the eight lines. Five general interface management lines ensure the orderly flow of information.

Supported HP-IB functions as detailed in IEEE Standard 488-1978 are: C1-C5, SR1, RL1, PP1, DC1, DT1, SH1, AH1, T5, TE5, L3, LE3.

Cable Specifications

Maximum cable length for Standard Mode operation is 2m (6.5 ft.) per device connected, with a 20m (65 ft.) total length. The maximum number of devices is accommodated by interconnections using shorter-than-maximum cable length.

Maximum cable length for High Speed operations is 1m (3.2 ft.) per device connected with a 15m (48.8 ft.) total length.

Internal HP-IB (Model 550)

The Series 500 Model 550 features a built-in, standard speed HP-IB interface. It is recommended for general purpose HP-IB applications at transfer rates of 300 Kbytes/sec. Although it can be used to control the root disc, it is not recommended because of loss of performance. The feature set supported is IEEE-1978 compatible.

General Purpose I/O (HP 27112A)

The 27112A General Purpose I/O Interface is designed to provide multi-purpose 8- or 16-bit parallel communication with Direct Memory Access between external devices and the Series 500 using the standard architecture.

Features

- Choice of programmable operating modes (clocked or transparent) for ease of use with instrumentation.
- Supports +5V on all input and output signals, plus an optional +12V level on output signals.
- Programmed data detection for either positive true or ground true levels.
- Independent 16-bit input and output lines and storage registers.
- Two control and two status lines.

Operation

The GP-IO Interface supports either 8- or 16-bit transfers without byte packing on the 8-bit transfers. All data is latched in a 16-bit input or output data register.

This interface supports two modes of operation: Clocked and Transparent. With the Clocked mode, data may be latched externally with a rising or falling clock pulse, or internally with a Series 500 BASIC READ command. The Transparent mode is useful for communicating with one or several asynchronous external devices. While in this mode, all data is read and sent programmatically and independent of hardware handshakes.

In addition, all input, output, status and control lines can be configured independently to detect a true condition on a high or low voltage level. Included in this set of signals are two control and two status lines which are latched and available to the user for unique communication requirements.

Line Characteristics

PDIR		Peripheral Data
DIN	(0 – 15)	Data Input
DOUT	(0 – 15)	Data Output
STS	(0 – 1)	Status Input
CTL	(0 – 1)	Control Output
PFLAG		Peripheral Flag
PCNTL		Peripheral Control
PEND		Peripheral End
PRESET		Peripheral Reset

Asynchronous Serial (HP 27128A)

The 27128A is a single-channel, asynchronous serial interface suitable for interfacing to RS-232C peripherals and terminal emulation. An on-board microprocessor and buffering offer a wide range of protocol, timing and editing features to simplify application programming and reduce central processing overhead.

Features

- Switch selectable and software programmable baud rate; up to 19200 bits per second.
- EIA RS-232C, CCITT V.24, and CCITT V.28 compatibility.
- Asynchronous transmission in simplex, full duplex and echoplex mode. Note: modem support for full duplex and echoplex.

- Programmable format control and built-in framing error, overrun error and parity checking.
- Break detection, support for X-ON/X-OFF and terminal emulation mode.

Operation

The serial interface permits the following baud rates to be configured by program control or by a switch that selects the rate to be configured at power-up: 50, 75, 110, 134.5, 150, 300, 600, 900, 1200, 1800, 2400, 3600, 4800, 7200, 9600, 19200.

Note: *Not all data recognition features are supported for continuous data transfer at 19200 baud.*

The following formats and protocols are also programmable:

- Parity: none, odd, even, "0" or "1".
- Number of bits per character: 5, 6, 7, or 8 plus parity.
- Number of stop bits: 1, 1.5, or 2.
- Handshaking: ENQ/ACK and X-ON/X-OFF

The on-board microprocessor and buffering of the 27128A offer efficient, high-performance terminal handling. The 27128A card has enough buffer space to store up to 485 characters on input and 500 on output. The on-board processor allows the user to edit the buffer with delete character and delete line commands. These features significantly reduce the time spent by the CPU to handle data entry from terminals.

In addition, the 27128A offers numerous features for satisfying more specialized data communication and serial interfacing requirements. The features listed below are currently accessible to user programs through the Series 500 BASIC Language System only. Many of these features are also accessible through HP-UX's Asynchronous Communication software and BASIC's Asynchronous Terminal Emulator. These two packages are designed to help develop readily configured, asynchronous data communication solutions.

The 27128A offers four alternatives for signaling the Series 500 when an incoming record is complete and ready for processing.

- User-specifed single text terminators. The user can specify up to eight characters and, with the quoting mode, specify a terminator which should be inserted in the text buffer without terminating the record.
- A user-specifed double text terminator.
- Activation of an interrupt mode which will signal the Series 500 when new data is available.
- Expiration of a character counter.

Additional character recognition capabilities allow the following features:

- automatic and conditional appendage of separators on transmitted text,
- programmable prompt sequence detection and
- signal character checking.

The 27128A can ease real-time programming requirements with the following:

- break detection and generation,
- a no-activity and lost receiver disconnect timer, and a host ENQ/ACK timer.

Asynchronous 8-Channel Multiplex (HP 27130A)

The 27130A Asynchronous Multiplexer is an economical solution for interfacing up to eight RS-232C or RS-423A compatible devices to the Series 500 with a single hardware interface. The 27130A can easily be configured to support a wide range of terminals, printers and other asynchronous devices.

Features

- CCITT V.10/28, EIA RS-232C compatible.
- Supports simplex, echoplex or full-duplex mode (asynchronous transmission only).
- Selection of data transmission attributes can be performed independently on each channel.
- Local intelligence reduces time consumed by the CPU during I/O transactions by offering edit functions, special character recognition and handshake protocol control.
- Parity, overrun and framing errors are sensed locally to detect transmission errors.
- X-ON/X-OFF (both directions) and ENQ/ACK (one direction, host sending ENQ) handshaking.

Operation

Programmable attributes:

Baud rates	110, 134.5, 150, 300, 600, 1200, 2400, 4800, 9600 or 19200
Parity	Odd, even or none
Stop bits	1 or 2
Character size	5, 6, 7 or 8 bits
Handshakes	ENQ/ACK and X-ON/X-OFF

Note: *Not all data recognition features are supported for continuous data transfer at 19200 baud.*

The 27130A uses microprogrammed capabilities to offer efficient, high performance device handling. The interface buffers each channel with two 512 byte memories for transmission and receiving. The intelligence of the interface permits users to edit these memories and use character recognition to insert or strip characters, which results in a streamlined peripheral interface.

I/O Expander (HP 97098A)

The HP 97098A I/O Expander is an external card cage supported by the Series 500. It provides user access to the second and third I/O Processors for additional I/O interface card capacity. With the 97098A, you can access an additional eight channels with Direct Memory Access capability on each channel. Thus, two 97098A I/O Expanders will increase the capacity to 20 user-available I/O slots on the Model 520, and 23 on the Models 530 and 540, and 15 on Model 550 (with one additional 97098A).

Specifications

No. of I/O slots	8
Line requirements	90 – 132 Vac, 2.5 A max. or 198 – 250 Vac, 2.5 A max.
Max. power dissipation	180 watts
Input frequency	47 – 66 Hz
Dimensions:	
Height	7.4 in. (18.7 cm)
Width	16.75 in. (42.5 cm)
Length	19.85 in. (50.4 cm)
Cable length	6 ft. (1.82m)

Note: *There must be an additional I/OP for each Expander. Limit = 2 I/OPs.*

LAN 9000 Local Area Network (HP 2285A)

LAN 9000 is a bundled software and hardware product that provides high performance local area networking of HP 9000 Series 500 computers running the HP-UX Operating System. Its implementation is Ethernet* Version 1.0 and it is essentially transparent to its users. In addition to its multi-user, multi-service and multi-connection capabilities, it provides:

Remote File Access – access to directories, data files, special files and peripherals across the network.
Network File Transfer – transfer of files within the network.
Remote Process Management – starting or stopping processes on systems throughout the network.
Interprocess Communication – communication between simultaneously running processes. LAN 9000 can link processes local to one machine or remotely across the network while maintaining the same user interface.

* *Ethernet is a registered trademark of Xerox Corporation.*

Features

- Coax cable with baseband signalling.
- 10 Mbps data signalling rate.
- Minimum separation between nodes is 2.5m.
- Nodes can be up to 50m from the coax cable.
- Masterless protocol, Carrier-Sense Multiple Access with Collision Detection (CSMA/CD).
- Up to 500m segment coax length and up to 100 nodes per segment.
- Supports broadcast and multicast addressing.
- User-executable diagnostics which can be run simultaneously with other network services.

Operation

LAN 9000 consists of a self-contained Ethernet Interfacing Unit (LAN Unit), a transceiver branch cable, a transceiver, LAN 9000 software and a dedicated HP-IB interface cable (HP 27110A). LAN 9000 is microprocessor based and is downloaded with link protocol software over the HP-IB interface from the host CPU (see Figure 1 for the physical configuration).

When addressed by another node on the network, the HP 2285A LAN Unit receives packets and checks the accuracy of data before passing the packet on to the host CPU. For transmission of packets, the host transfers the packet to the LAN Unit over the HP-IB cable and the LAN Unit in turn transmits the packet onto the network according to the Network Access Protocol.

To increase the length of the transceiver branch, up to two additional 15-metre cables can be ordered (HP Part No. 1150-1629).

The Ethernet cable installed must meet Ethernet Version 1.0, Sept. 30, 1980, Section 7.3 specifications. HP Computer Supplies Operation has two cables available: Ethernet Cable (92179E) and Non-Conduit Ethernet Cable (92179F). The 92179F is made with a Teflon† outer jacket and Teflon dielectric. This cable can be installed in air plenums. The 97179E cable must be installed in cable trays or conduit.

† *Teflon is a trademark of DuPont.*

Specifications

Transmission mode	Baseband digital
Impedance	50 Ohm
Electrical specifications	3 A, 50 Watts (115 Vac, 50 Hz) 1.5 A, 50 Watts (230 Vac, 60 Hz)
Dimensions	LAN Unit: 13.2cm (5.2 in.) high 43.2cm (17.0 in.) wide 35.6cm (14.0 in.) deep Transceiver: 3.5cm (1.4 in.) high 10.5cm (4.1 in.) wide 13.0cm (5.1 in.) deep
Weights	LAN Unit: 9.5 kg (21 lbs.) Transceiver: .83 kg (1.8 lbs.) Branch Cable: 1.9 kg (4.3 lbs.) HP-IB Interface: 234 grams (8.2 oz.) HP-IB Cable: 445 grams (15.6 oz.)
Environmental requirements	Temperature: 0° – 40°C (operating) –20° – 65°C (storage) Humidity: 5% – 80% (operating) 5% – 90% (storage) Altitude: 4,545m (15,000 ft.) operating 7,575m (25,000 ft.) storage

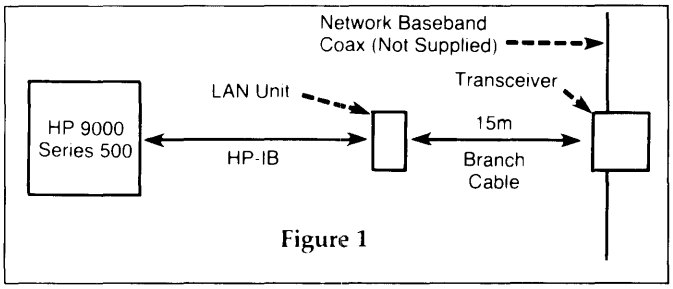


Figure 1

Local Area Network Installation Kit (HP 28656A)

This kit provides the connectors and tools needed to install the Ethernet standard coax cable and to connect the transceivers used in the LAN 9000 product. It is recommended that the installation kit be supplied for every network and not for every 2285A ordered.

The kit includes:

- Special Ethernet Cable Stripper (8710-1508)
- Precision engineered N-Type Connector Crimp Tool (8710-1507) that prevents over- and under-crimping
- F-F and M-M N-Type Adaptors (1250-0777, 78)
- 50 Ohm Terminator (1150-1627)
- M Crimp on N-Type Connector (1250-1627)
- Insulated N-Type Adaptor (5061-4932)
- Boot insulators (1150-1623)
- Cable Installation Manual (2285-90002)

A special Option 001 deletes the Ethernet cable stripper and the N-Type Crimp Tool. This option is recommended when there is more than one installed network per site.

RJE Interface (HP 27122A)

The RJE interface, used in conjunction with the RJE software (97077A or 97087A) under HP-UX, allows the HP 9000 Series 500 to emulate an IBM 2780 or 3780 workstation. It permits the Series 500 to be used as a Remote Job Entry station for batched job communication with IBM 360/370 (or other compatible) computers using the IBM Bisync protocol.

The RJE interface features a plug-in card incorporating microprocessor intelligence that offloads all communications overhead from the host. This means the interface card performs all protocol generation and interpretation, as well as modem control tasks and pre-processing functions such as character conversion, blocking and deblocking.

The specific needs of many different RJE applications are met by selecting programmable configuration parameters.

Full trace log, communications status and statistics, as well as hardware self-test, are provided to facilitate complete monitoring and check-out of the interface.

Features

- 1200 to 19200 baud rates
- Compatible with EIA RS-232C and CCITT V.24 specifications
- Supports Bell type 208B, 2096 and 212 data sets or equivalent
- Supports Seimens MSV2 protocol
- Works with full or half duplex modems and supports AUTO ANSWER and ORIGINATE
- Provides link control functions: line bid, normal and transparent data modes, all responses, and link termination
- Assures data integrity with CRC error checking
- EBCDIC character recognition
- Space compression/truncation

Operation

The RJE interface works with modems (or modem eliminators) over switched or non-switched lines. The maximum data rate supported by the interface is 19.2 Kbps but it also operates at slower rates to accommodate different modems.

Link control is managed entirely by the on-card microprocessor. All functions and responses (ACK/NAK/WACK/TTD/RVI) are implemented by the card upon request by software from the Series 500.

Card parameters and special character handling may be configured from the HP 9000 Series 500 or allowed to retain their default values. Configurable parameters include: record and block sizes, timeouts, retry counts, conversion tables, record separators and formatting functions. Special character handling includes: character code translation, automatic record terminations, adding and stripping, record and block separator sequences, blank truncating and padding, and repeated character compression and expansion.

To assist in line quality and link troubleshooting, the RJE interface card accumulates communication statistics. A continuous trace log can collect all sent-or-received link control characters and independently collect all sent-or-received data characters. You can review the link control character trace log without having access to the data character trace log, thus permitting link trouble shooting without violating data security. A trace log also collects all internal firmware state changes.

The RJE interface does not recognize horizontal tabulation and vertical forms control codes. This capability must be host-resident.

Specifications

Max. current requirements	+5V = 1.62 Amps +12V = .087 Amps −12V = .108 Amps
Dimensions	172.7mm (6.8 in.) long 172.0mm (7.75 in.) wide
Weight	Interface Card: 235 grams (8.3 oz.) Modem Cable: 560 grams (19.7 oz.)
Environmental requirements	Operating temperature: 0° − 55°C Operating humidity: 5% − 95% RH @ 40°C Operating altitude: 4600 metres (15,000 ft.)

Shared Resource Manager Interface (HP 27123)

The HP 27123 Shared Resource Management (SRM) Interface allows an HP 9000 Series 500 HP-UX system or BASIC Language System to interconnect to an HP SRM system.

The SRM system consists of a dedicated Series 200 controller that manages shared peripherals and a hierarchical file system on a shared disc connected to it. BASIC, Pascal, and HP-UX workstations are linked to the SRM controller via SRM cables and multiplexers. The benefits of an SRM system are cost savings by sharing peripheral devices and the convenience of being able to access common information on a shared disc from multiple workstations.

HP 9000 Series 500 BASIC Language systems can perform the same mass storage operations to the SRM disc that are available with a local disc, except for system boot. HP-UX systems can copy files from the local HP-UX disc to the SRM disc and vice versa.

- Cable Specifications
- The HP 272123A Interface is connected to the SRM system by any of the following SRM cables:

- 97061A − 10 Metres
- 97061B − 25 Metres
- 97061C − 60 Metres
- 97061D − 60 Metres (unterminated on one end to facilitate pulling cable thru cable trays.)

Refer to the HP 9000 Data Communications Technical Supplement (Publication Number 5953-4692) for detailed configuration and ordering information concerning the SRM system.

HP 97060A Graphics Processor

The 97060A Graphics Processor is an intelligent external graphics processor implemented with LSI/VLSI bipolar and MOS technology. Its bit-slice processor features a high-level instruction set which offers full access to a 1024 x 768 x 8 graphics display system. Fast vector generation speeds are obtained by interfacing the HP 9000 with the 27112A's 16-bit parallel, direct memory access interface. The 97060A's drawing processor can perform area shading at speeds approaching 16M pixels per second.

The 97060A can interface the HP 13279B Color Monitor or any other RS-343 compatible color monitor which can support the 97060A's horizontal scan rate. Included in the 97060A is a built-in HP-IB Interface which can communicate with the 9111A Graphics Tablet. While using the Graphics/9000 DGL/AGP libraries, this connection permits the 97060A to offload the HP 9000 of cursor tracking responsibilities and improve the interaction of the HP 9000 system.

Specifications

Dimensions	172.7mm (6.8 in.) long 172.0mm 6.75 in.) wide
Weight	Interface Card: 235 grams (8.3 oz.)
Environmental requirements	Temperature: 0° – 55°C (operating) Humidity: 5% – 95% RH @ 40°C (operating) Altitude: 4,572m (15,000 ft.) operating
Resolution	1024 x 768 x 8 (33 Hz refresh) or 735 x 550 x 8 (60 Hz non-interlaced)
Colors	256 displayed from 2^{24}
Horizontal scan rate	28.3 KHz at 33 Hz vertical 35.4 KHz at 60 Hz vertical
Cables	3 meter, 75 ohm cables with BNC termination
Power	200 Watts nominal
Line	90 – 125V or 198 – 250V at 48 – 66 Hz
Max. current	3A (nominal) 4A (in-rush)
Dimensions	17″ x 5¼″ x 21″

Color Video Interface (HP 97062A)

The 97062A is a lower-cost, medium-resolution interface to a color graphics monitor. The Interface consists of two printed circuit boards which plug into the Series 500's I/O backplane and produce RS-343-compatible signals across three coaxial cables. It has four planes of memory to implement a 16 element color map and utilizes gate-array technology to perform vector generation. It supports all Graphics/9000 plotter commands including area shading. If a terminal interface to the host computer is desired, a display terminal is necessary.

Resolution	576 x 455 x 4 (60 Hz, non-interlaced)
Colors	16 displayed from 4,096
Horizontal scan rate	29.4 KHz
Cables	Includes three 75 Ohm, 2m cables with BNC termination (red, green/sync, blue)

HP 13279B 19″ Color Monitor

The HP 13279B is a high-quality 19-inch color display monitor designed for video output of computer generated information. The product, utilizing raster scan display technology, finds numerous applications in CAD/CAM, general graphics display, process control and computer imaging.

Features

- Precision In-Line (PIL) CRT technology
- Selectable Horizontal Scan Frequency
- High Density Shadow Mask CRT
- Preset Calibration Control

Specifications

Visual performance:	
Resolution	1080 Horiz. x 809 Vert. pixels
Pitch	0.012 in. (0.31 mm)
Brightness	P22 Phosphor – 9.37 fl. (nom.) A22 Phosphor – 13.07 fl. (nom.)
Phosphor	P22 Short persistance A22 Long persistance
Circuit performance:	
Video bandwidth	100 Hz to 40 Mhz @ –3 dB
Pulse response	Rise time: 8.5 nanoseconds Fall time: 13 nanoseconds
Scan rate	15 – 37 KHz interlaced or non-interlaced with three 8 KHz wide, jumper-selectable scam ranges
Environmental requirements:	
Temperature	32°C to 122°F (50°C)
Humidity	10% to 90% relative, non-condensing
Altitude	Up to 10,000 feet (3000 meters)
Power requirements:	
Voltage	100, 117, 200, 234 Vac ± 10%
Frequency	50 – 60 Hz, ± 10%
Consumption	155 watts nom., 170 watts max, at 117 Vac
Physical specifications:	
Dimensions	15.7 in. height x 18.97 in. width x 23.56 in. depth
Weight	81.00 lb. (36.74 Kg)

System Software

The Series 500 can be configured with the HP BASIC System or with HP-UX, a UNIX system that has been specially enhanced for the engineering environment. The HP BASIC System can only be ordered for the Model 520 Integrated Workstation version. HP-UX can be ordered on all models. Both systems require a mass storage device from which the operating system can be loaded into memory as part of the power-up procedure.

HP BASIC Language System

The HP BASIC System provides the BASIC Language and Operating System (single-user) which allows access to the following BASIC software:

Description	HP Prod. No.
BASIC 2D-3D Graphics	97052B
IMAGE/QUERY-9000 DBMS	97053B
BASIC Asynchronous Terminal Emulator	97056A
Shared Resource Management Software	97058A

For more information on the Series 500 BASIC System consult the Series 500 BASIC Language System Technical Supplement (HP Publication No. 5953-4691).

HP-UX Operating System

The HP-UX System offers both single- and multi-user capabilities. The "C" language is standard.

Model 520	HP Prod. No.	Models 530, 540, 550	HP Prod. No.
Single-user HP-UX	97070B	Single-user HP-UX	97079B
Multi-user HP-UX (to 16-user)	97080B	Multi-user HP-UX (to 16-user)	97089B
Multi-user HP-UX (to 32-user)	97078B	Multi-user HP-UX (to 32-user)	97088B

The HP-UX System provides access to the following software:

	HP Product No.	
	Single-user	Multi-user
FORTRAN 77 Compiler	97071A	97081A
HP Pascal Compiler	97072A	97082A
IMAGE-9000 DBMS	97073A	97083A
HP-UX Graphics (AGP)	97075A	97085A
RJE Communications Software	97077A	97087A
Local Area Network	2285A	
Applications Migration Package	97086A	

For more information on the HP-UX System, consult the HP 9000 HP-UX Technical Supplement (HP Publication No. 5953-9509).

All Series 500 HP-UX software is available only on the 88140L/S ¼" Tape. The HP BASIC software is available only on 5¼" Flexible Disc.

Accessories and Support

Documentation

Part No.	Manual Title
5957-7925	Software Status Bulletin
0900-90007	HP-UX Reference
09020-90011	Installation and Test (Model 520)
09040-90010	Installation and Test (Models 530 & 540)
09050-90010	Installation and Configuration (Model 550)
09050-90040	Series 200/500 Site Preparation Manual
92836-90005	Structured FORTRAN 77 Programming with HP Computers
97050-80020	HP BASIC Manual Package (includes the following five HP BASIC manuals):
97050-90000	BASIC Programming Techniques (Model 520)
97050-90005	BASIC Language Reference (Model 520)
97050-90015	BASIC Condensed Reference
97050-90090	BASIC – Where Do I Start? (Brochure)
97052-90000	BASIC Graphics Programming Techniques (Model 520)
97053-90000	IMAGE-9000 Programming Techniques
97053-90001	QUERY User's Guide
97053-90002	Data Base Design Kit
97056-90000	HP BASIC Asynchronous Terminal Emulator User's Manual
97058-90000	SRM Supplement for HP 9000
97059-90000	LAN Local Area Network User's Guide
97059-90001	LAN Node Manager's Guide
97070-87901	HP-UX Manual Package (includes all HP-UX and C manuals for Series 500)
97070-90090	HP-UX 9000 Series 500 4.0
97076-90001	HP-UX Asynchronous Communications Guide
97077-90000	RJE User's Guide
97080-90092	Series 500 HP-UX Unpacking Instructions
97081-90001	FORTRAN/9000 Reference (Series 500 only)
97082-90001	Pascal/9000 Reference (Series 500 only)
97082-90002	Programming in Pascal with Hewlett-Packard Pascal
97084-90000	GRAPHICS/9000 DGL Programmer's Reference Library
97084-90001	HP-UX Supplement for above
97084-90002	Instruction DGL/AGP Demo
97084-90025	GRAPHICS/9000 Device Handler's Manual
97085-90000	Advanced Graphics Package (AGP) User's Guide
97085-90001	Supplement for HP-UX systems
97085-90005	AGP Reference Manual
97089-90000	The C Programming Language by Kernighan & Ritchie
97089-90002	HP-UX Selected Articles
97089-90004	HP-UX Concepts and Tutorials
97089-90048	HP-UX System Administrator's Manual
97098-90020	I/O Expander Installation and Service
98183-90000	HPSPICE User's Guide
98183-90005	HPSPICE Reference
98680-90021	FORTRAN Comparison Notes for the Series 200/500
98680-90025	Introducing the UNIX System

Documentation *(cont'd.)*

Part No.	Manual Title
27110-90001	HP 27110 HP-IB Installation Manual
27112-90001	HP 27112A GP-IO Interface Installation
27122-90001	27122A RJE Interface Installation Manual
27123-90001	27123A SRM Interface Installation Manual
27132A	MP-CIO Technical Reference Package
27128-90001	HP 27128A ASI Installation Manual
27130-90001	HP 27130A 8-channel Multiplex Interface Installation Manual
27132-90001	HP 27132A Reference Manual
27132-90003	27112A GP-IO Installation Manual
27132-90004	27122A RJE Interface Firmware Reference
27132-90006	27128A ASI Technical Reference Manual
27132-90005	PSI Hardware Reference Manual

Accessories Supplied

The following items are supplied with the Model 520:

Installation and Test Manual . . . . . HP Part No. 09020-90011
Flexible Disc Media . . . . . 2 each, 256 Kbyte
Special Function Key Overlays . . . . . 2 blank, HP Part No. 7120-3107
System Integrity Software . . HP Part No. 09020-10010

If a color CRT is ordered with the Model 520, add:

Fuse . . . . . 2110-0051 for 100 – 120 Vac
2110-0056 for 220 – 240 Vac

If optional Thermal Printer is ordered, add:

	HP Part No.
Paper Tray	09855-67951
For Opt. 590:	
Thermal Paper (8½" wide, black-on-white, 1 pkg. of 330 sheets)	9270-0640
For Opt. 591:	
Thermal Paper (210mm wide, black-on-white, 1 pkg. of 330 sheets)	9270-0642

The following items are supplied:

	HP Part No.
Installation and Test Manual	09040-90010 (Models 530 and 540)
Installation and Configuration	09050-90010 (Model 550)

Accessories Available

Here is a list of some of the key accessories and supplies available. See the Computer User's Catalog, HP Pub. No. 5953-2450(D) for a complete listing.

	HP Part/Prod. No.
Thermal Printer Paper (4 packs/box, 330 sheets/pack)	
8½" wide, black on white	9270-0640
8½" wide, blue on white	9270-0641
210mm wide, black on white	9270-0642
210mm wide, blue on white	9270-0643
5¼" Flexible Discs (box of 10)	92190A
Flexible Disc Head Cleaner Kit	92193A
Power Line Conditioner	35030A
Workstation Table (designed for the Model 540, same style, height and color)	92170G
Workstation Table (designed for the Model 520, two tiered)	92213A

HEWLETT PACKARD

Printed in U.S.A (11/84)
5953-9525

Motherboard Pinout Data

Appendix C

Figure C-1 is a layout drawing of the computer motherboard. It identifies all motherboard connectors and shows every pin and its corresponding signal name. Table C-1 lists every motherboard connector and its usage. Table C-2 alphanumerically lists all the signal names used on the motherboard and provides their definitions.

Table C-1. Motherboard Connectors

Designator	Connecting Assembly
P1	Processor Stack
P2	Processor Stack
P3	Power Supply
P4	Power Supply
P5	Power Supply
P6	Power Supply
P7	Power Supply
P8	Power Supply
P9	System Control Module
P10	System Control Module
P11	I/O Backplane
P12	IOP Finstrate
P13	Power Supply Fan, I/O Fan
P14	Processor Stack Fan
P15	Processor Stack Door, I/O Door
P16	(Not Used)
P17	Uninterruptible Power Supply
P18	Mass Storage Device

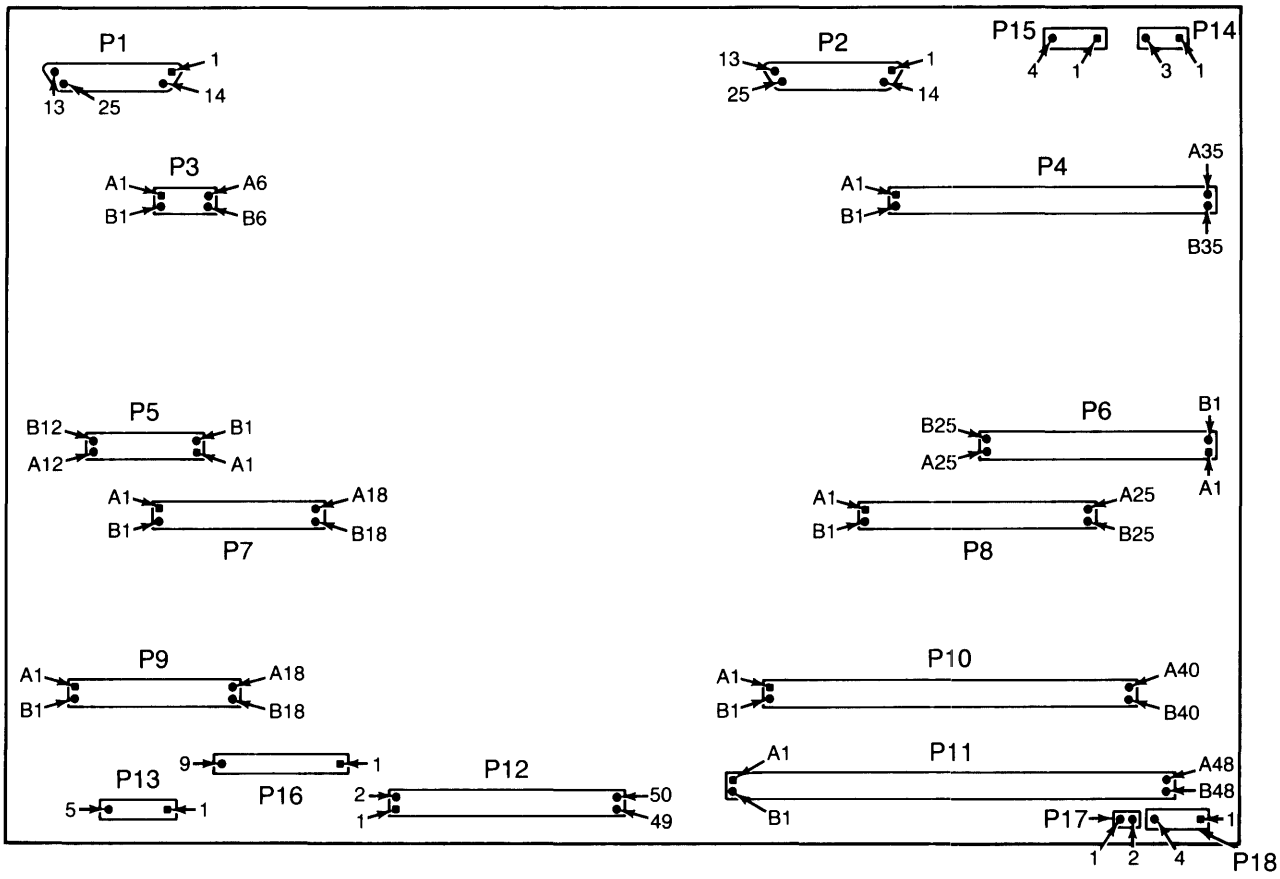
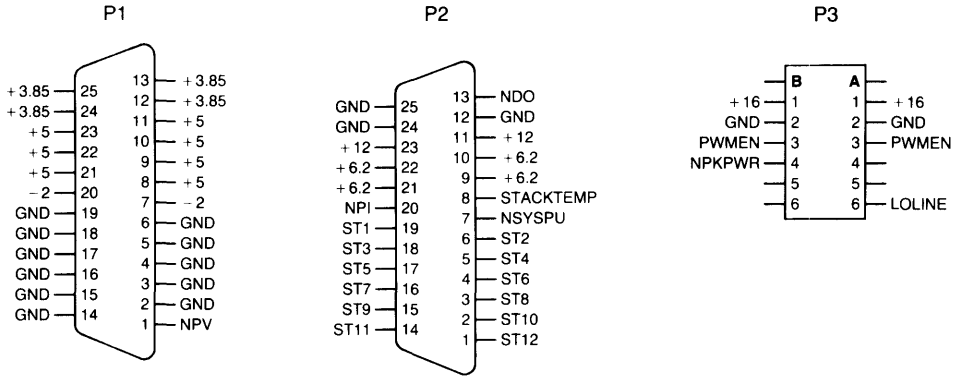
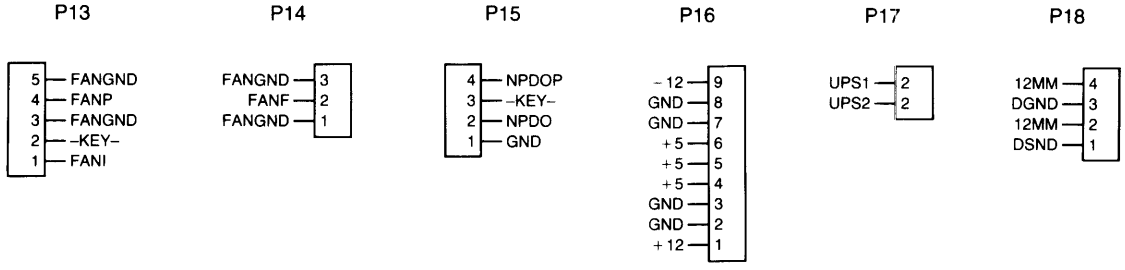


Figure C-1. Motherboard Connectors Locater Drawing





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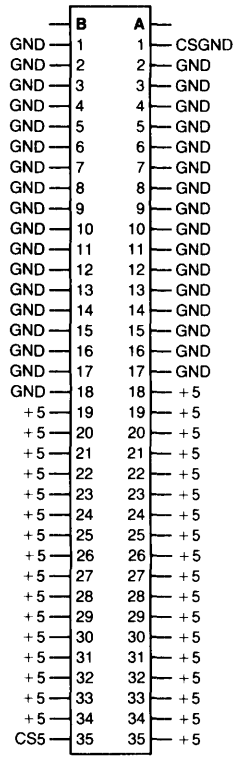

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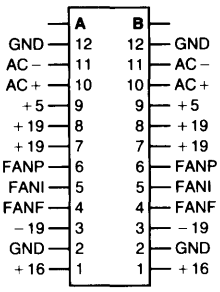

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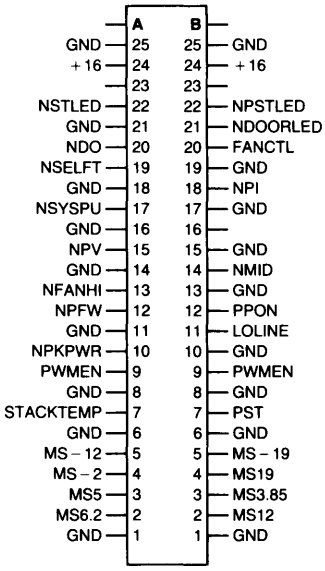

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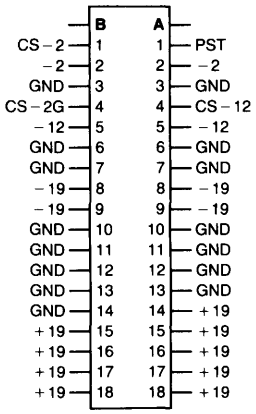

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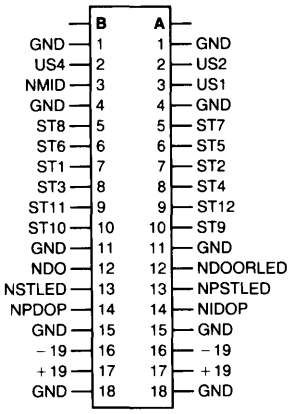

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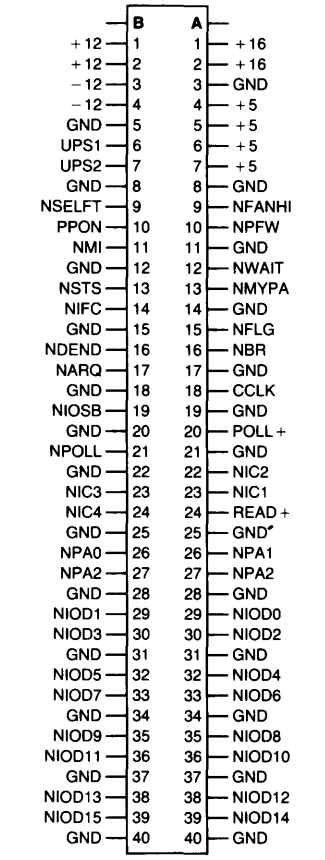

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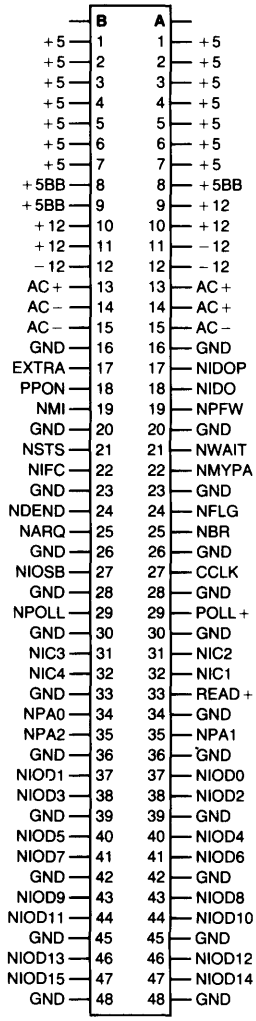

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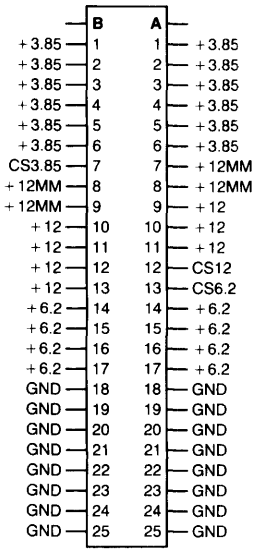

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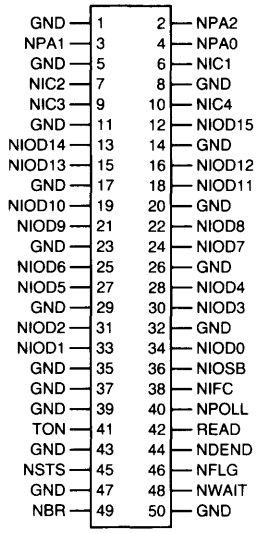


Table C-2. Motherboard Signal Definitions

Signal	Definition
– KEY –	Keyed hole in connector.
– 12	– 12 volt supply.
– 19	– 19 volt supply.
– 2	– 2 volt supply.
12	12 volt supply.
12MM	12 volt supply to mass storage devices only.
16	16 volt bias supply voltage.
19	19 volt supply.
3.85	3.85 volt supply.
5	5 volt supply.
5BB	5 volt battery backup.
6.7	6.7 volt supply.
AC +	25 KHz ac sine wave from power supply.
AC –	25 KHz ac sine wave from power supply.
CCLK	Baud rate generator on SCM board for I/O backplane.
CS – 12	Control sense for – 12 volt supply.
CS – 2	Control sense for – 2 volt supply.
CS – 2G	Control sense for – 2 volt supply ground.
CS12	Control sense for 12 volt supply.
CS3.85	Control sense for 3.85 volt supply.
CS5	Control sense for 5 volt supply.
CS6.7	Control sense for 6.7 volt supply.
CSGND	Control sense for 5 volt supply ground.
DGND	Dirty ground return.
FANCTL	Fan control. Connected to PST.
FANF	Power to processor stack fan (negative voltage).
FANGND	Fan ground return.
FANI	Power to I/O card cage fan (negative voltage).
FANP	Power to power supply fan (negative voltage).
GND	Ground plane of motherboard.
LOLINE	Low line indication.
MS – 12	Monitor sense for – 12 volt under/over voltage.
MS – 19	Monitor sense for – 19 volt under/over voltage.
MS – 2	Monitor sense for – 2 volt under/over voltage.
MS12	Monitor sense for 12 volt under/over voltage.
MS19	Monitor sense for 19 volt under/over voltage.
MS3.85	Monitor sense for 3.85 volt under/over voltage.
MS5	Monitor sense for 5 volt under/over voltage.
MS6.7	Monitor sense for 6.7 volt under/over voltage.
NARQ	HP-CIO card requests attention (negative true).
NBR	I/O bus burst mode DMA request (negative true).
NDEND	I/O bus device end (negative true).
NDO	Door open (negative true). Wired OR of NPDO and NIDO.
NDOORLED	Doop open (negative true).
NFANHI	Power supply fan at highest speed (negative true).
NFLG	I/O bus ready for data (negative true).
NIC1	I/O bus interface control bit 1 (negative true).
NIC2	I/O bus interface control bit 2 (negative true).
NIC3	I/O bus interface control bit 3 (negative true).
NIC4	I/O bus interface control bit 4 (negative true).

Signal	Definition
NIDO	I/O cage door open (negative true). OR'd with NPDO.
NIDO0	I/O bus input/output data bit 0 (negative true).
NIDO1	I/O bus input/output data bit 1 (negative true).
NIDO2	I/O bus input/output data bit 2 (negative true).
NIDO3	I/O bus input/output data bit 3 (negative true).
NIDO4	I/O bus input/output data bit 4 (negative true).
NIDO5	I/O bus input/output data bit 5 (negative true).
NIDO6	I/O bus input/output data bit 6 (negative true).
NIDO7	I/O bus input/output data bit 7 (negative true).
NIDO8	I/O bus input/output data bit 8 (negative true).
NIDO9	I/O bus input/output data bit 9 (negative true).
NIDO10	I/O bus input/output data bit 10 (negative true).
NIDO11	I/O bus input/output data bit 11 (negative true).
NIDO12	I/O bus input/output data bit 12 (negative true).
NIDO13	I/O bus input/output data bit 13 (negative true).
NIDO14	I/O bus input/output data bit 14 (negative true).
NIDO15	I/O bus input/output data bit 15 (negative true).
NIDOP	I/O cage door open (negative true.
NIFC	I/O bus interface clear (negative true).
NIOSB	I/O bus data transfer strobe (negative true).
NMI	Non-maskable interrupt.
NMID	Non-maskable interrupt.
NMYPA	HP-CIO card recognized its address has been asserted (negative true).
NPA0	I/O bus peripheral address bit 0 (negative true).
NPA1	I/O bus peripheral address bit 1 (negative true).
NPA2	I/O bus peripheral address bit 2 (negative true).
NPDO	Panel door open (negative true). OR'd with NIDO.
NPDOP	Panel door open (negative true). Signals SCM board.
NPFW	Power fail warning (negative true).
NPI	Not pop in (negative true). Resets the stack.
NPKPWR	Shut down command indicator due to peak power (negative true).
NPOLL	I/O bus interface poll (negative true).
NPSTLED	Power supply overtemperature (negative true).
NPV	Not power valid; all outputs in spec (negative true).
NSELFT	Leading edge causes power supply to send stack into self-test via NSYSPU and NPI (negative true). Originates on SCM board.
NSTLED	Stack overtemperature (negative true).
NSTS	I/O bus status (negative true).
NSYSPU	Not system pop unsynchronized (negative true). Used with NPI to cause stack to perform a self-test.
NWAIT	I/O bus lengthen IOSB (negative true).
POLL	I/O bus interface poll.
PPON	Primary power on; all outputs in spec.
PST	Power supply temperature indicator; connected to FANCTL.
PWMEN	Pulse width modulator enable.
READ	I/O bus data direction (positive true; high indicates data to IOP).

Signal	Description
ST1	Stack self-test from slot 1.
ST2	Stack self-test from slot 2.
ST3	Stack self-test from slot 3.
ST4	Stack self-test from slot 4.
ST5	Stack self-test from slot 5.
ST6	Stack self-test from slot 6.
ST7	Stack self-test from slot 7.
ST8	Stack self-test from slot 8.
ST9	Stack self-test from slot 9.
ST10	Stack self-test from slot 10.
ST11	Stack self-test from slot 11.
ST12	Stack self-test from slot 12.
STACKTEMP	Stack temperature indicator.
TON	(Not used)
US1	Open trace.
US2	Open trace.
US4	POLL ANDed with NSELFT.
UPS1	Uninterruptible power supply.
UPS2	Uninterruptible power supply.

I/O Backplane Pinout Data

Appendix D

Figure D-1 is a layout drawing of the computer I/O backplane. It identifies all I/O backplane connectors and shows every pin and its corresponding signal name. Table D-1 lists every I/O backplane connector and its usage. Table D-2 lists all the signal names used on the I/O backplane and their definitions.

Table D-1. I/O Backplane Connectors

Designator	Connecting Assembly
P0	I/O Card (Slot/Select Code 0)
P1	I/O Card (Slot/Select Code 1)
P2	I/O Card (Slot/Select Code 2)
P3	I/O Card (Slot/Select Code 3)
P4	I/O Card (Slot/Select Code 4)
P5	I/O Card (Slot/Select Code 5)
P6	I/O Card (Slot/Select Code 6)
J7	Motherboard (Connector P11)
P8	I/O Door Interlock Switch

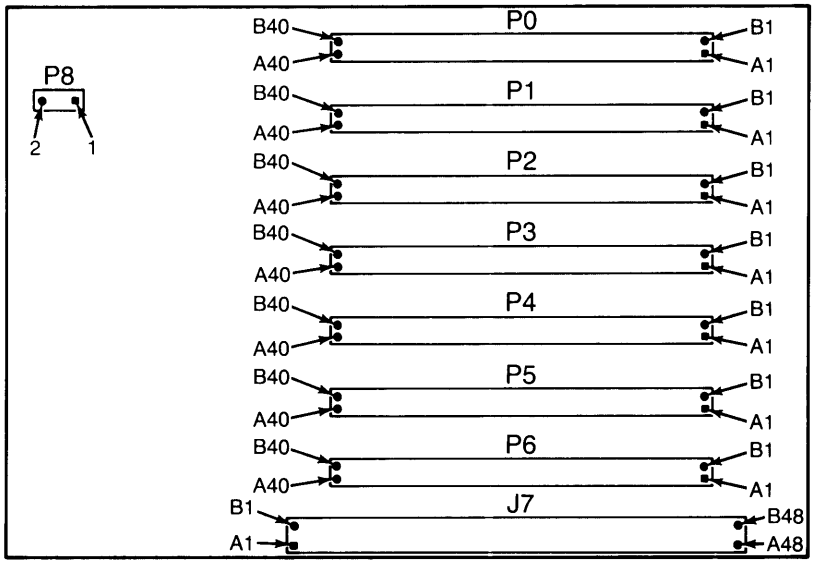


Figure D-1. I/O Backplane Connectors Locater Drawing

P0-P6

	A	B	
5P	40	40	5P
5S	39	39	5S
12	38	38	12
−12	37	37	−12
AC+	36	36	AC+
AC−	35	35	AC−
GND	34	34	GND
PPON	33	33	SPON
NPFW	32	32	NNMI
NOT USED	31	31	NOT USED
NSW0	30	30	NOT USED
NSW2	29	29	NSW1
NDPA	28	28	NSTS
GND	27	27	GND
NMYPA	26	26	NIFC
NFLG	25	25	NDEND
NBR	24	24	NARQ
GND	23	23	GND
CCLK	22	22	NIOSB
GND	21	21	GND
NSYNC	20	20	NPOLL
NIC2	19	19	NIC3
NIC1	18	18	NIC4
READ	17	17	NUAD
GND	16	16	GND
NPA0	15	15	NPA1
NPA2	14	14	NPA3
GND	13	13	GND
NIOD0	12	12	NIOD1
NIOD2	11	11	NIOD3
GND	10	10	GND
NIOD4	9	9	NIOD5
NIOD6	8	8	NIOD7
GND	7	7	GND
NIOD8	6	6	NIOD9
NIOD10	5	5	NIOD11
GND	4	4	GND
NIOD12	3	3	NIOD13
NIOD14	2	2	NIOD15
SGND	1	1	SGND

P8

GND	2	1	IDO

J7

	A	B	
5	1	1	5
5	2	2	5
5	3	3	5
5	4	4	5
5	5	5	5
5	6	6	5
5	7	7	5
5BB	8	8	5BB
2	9	9	5BB
12	10	10	12
−12	11	11	−12
−12	12	12	−12
AC+	13	13	AC+
AC+	14	14	AC−
AC−	15	15	AC−
GND	16	16	GND
IDOP	17	17	NOT USED
NIDO	18	18	PPON
NPFN	19	19	NNMI
GND	20	20	GND
NWAIT	21	21	NSTS
NMYPA	22	22	NIFC
GND	23	23	GND
NFLG	24	24	NDEND
NBR	25	25	NARQ
GND	26	26	GND
CCLK	27	27	NIOSB
GND	28	28	GND
NSYNC	29	29	NPOLL
GND	30	30	GND
NIC2	31	31	NIC3
NIC1	32	32	NIC4
READ	33	33	GND
GND	34	34	NPA0
NPA1	35	35	NPA2
GND	36	36	GND
NIOD0	37	37	NIOD1
NIOD2	38	38	NIOD3
GND	39	39	GND
NIOD4	40	40	NIOD5
NIOD6	41	41	NIOD7
GND	42	42	GND
NIOD8	43	43	NIOD9
NIOD10	44	44	NIOD11
GND	45	45	GND
NIOD12	46	46	NIOD13
NIOD14	47	47	NIOD15
GND	48	48	GND

Table D-2. I/O Backplane Signal Definitions

Signal	Definition
−12	−12 volt supply.
12	12 volt supply.
5	5 volt supply.
5BB	5 volt supply, battery backup.
5P	Primary 5 volt supply.
5S	Secondary 5 volt supply.
AC−	25 KHz ac sine wave from power supply.
AC+	25 KHz ac sine wave from power supply.
CCLK	Common clock.
GND	Ground plane of I/O backplane.
IDO	I/O door open.
IDOP	I/O door open (not used).
NARQ	HP-CIO card requests attention (negative true).
NBR	I/O bus burst mode DMA request (negative true).
NDEND	I/O bus device end (negative true).
NDPA	Internal select code available (negative true).
NFLG	I/O bus ready for data (negative true).
NIC1	I/O bus interface control bit 1 (negative true).
NIC2	I/O bus interface control bit 2 (negative true).
NIC3	I/O bus interface control bit 3 (negative true).
NIC4	I/O bus interface control bit 4 (negative true).
NIDO	I/O door open (negative true).
NIFC	I/O bus interface clear (negative true).
NIOD0	I/O bus input/output data bit 0 (negative true).
NIOD1	I/O bus input/output data bit 1 (negative true).
NIOD2	I/O bus input/output data bit 2 (negative true).
NIOD3	I/O bus input/output data bit 3 (negative true).
NIOD4	I/O bus input/output data bit 4 (negative true).
NIOD5	I/O bus input/output data bit 5 (negative true).
NIOD6	I/O bus input/output data bit 6 (negative true).
NIOD7	I/O bus input/output data bit 7 (negative true).
NIOD8	I/O bus input/output data bit 8 (negative true).
NIOD9	I/O bus input/output data bit 9 (negative true).
NIOD10	I/O bus input/output data bit 10 (negative true).
NIOD11	I/O bus input/output data bit 11 (negative true).
NIOD12	I/O bus input/output data bit 12 (negative true).
NIOD13	I/O bus input/output data bit 13 (negative true).
NIOD14	I/O bus input/output data bit 14 (negative true).
NIOD15	I/O bus input/output data bit 15 (negative true).
NIOSB	I/O bus data transfer strobe (negative true).
NMYPA	HP-CIO card recognized its address has been asserted (negative true).
NNMI	Non-maskable interrupt (negative true).
NPA0	I/O bus peripheral address bit 0 (negative true).
NPA1	I/O bus peripheral address bit 1 (negative true).
NPA2	I/O bus peripheral address bit 2 (negative true).
NPA3	I/O bus peripheral address bit 3 (negative true).
NPFW	Power fail warning (negative true).
NPOLL	I/O bus interface poll (negative true).

Signal	Definition
NSTS	I/O bus status (negative true).
NSW0	Select code switch 0 (negative true).
NSW1	Select code switch 1 (negative true).
NSW2	Select code switch 2 (negative true).
NSYNC	Synchronize (negative true).
NUAD	Your address; slot/select code select (negative true).
NWAIT	(Not used)
PPON	Primary power on; all outputs in spec.
READ	I/O bus data direction (positive true; high indicates data to IOP).
SGND	Safety ground.
SPON	Same as PPON.

SCM Pinout Data

Appendix E

Figure E-1 is a layout drawing of the system control module (SCM). It identifies the SCM connectors and shows all pins and their corresponding signal names. Table E-1 lists each SCM connector and its usage. Table E-2 lists all the signal names used on the SCM and their definitions.

Table E-1. SCM Connectors

Designator	Connecting Assembly
L	Motherboard (Connector P10)
S	Motherboard (Connector P9)
Service Panel Conn.	Service Panel

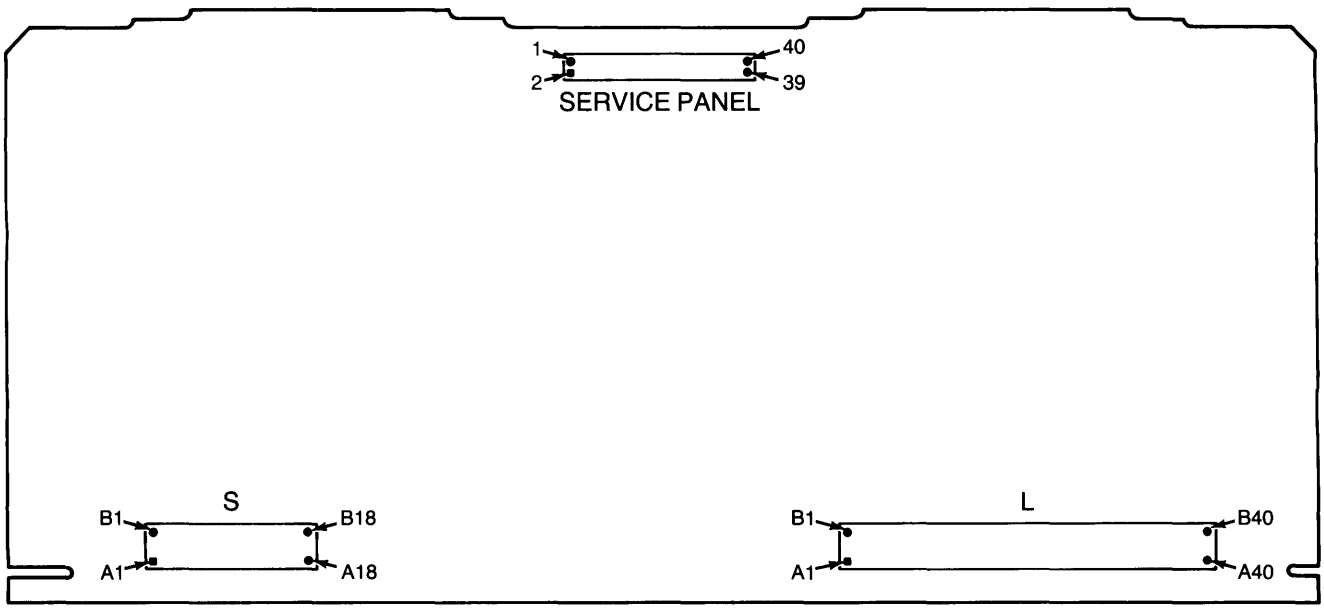
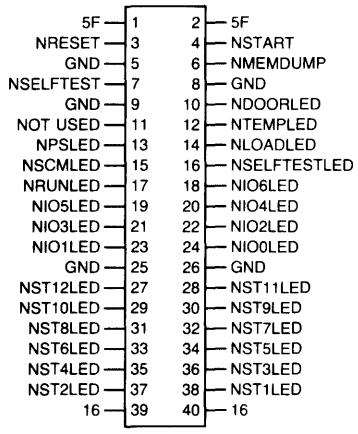


Figure E-1. SCM Connectors Locater Drawing

Service Panel Connector



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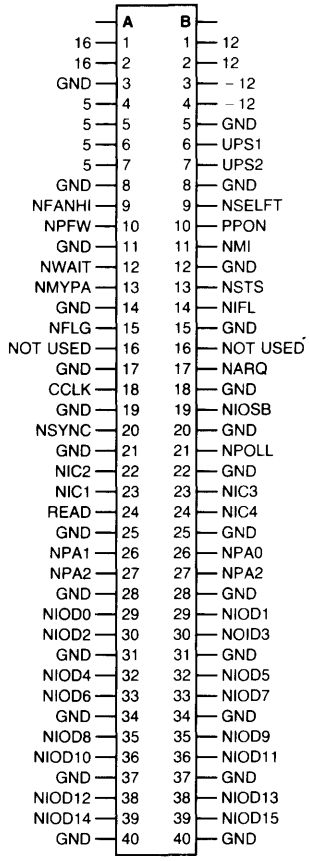

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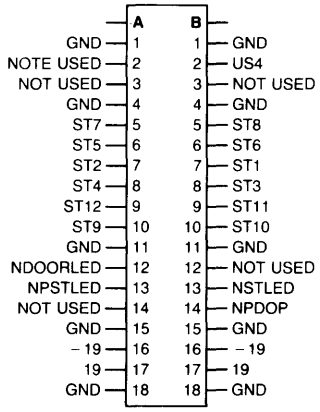

Table E-2. SCM Signal Definitions

Signal	Definition
−12	−12 volt supply.
−19	−19 volt supply.
5	5 volt supply
5F	5 volt fused supply.
12	12 volt supply.
16	16 volt bias supply.
19	19 volt supply.
CCLK	Baud rate generator for I/O backplane.
GND	Ground plane of SCM.
NDOORLED	Door open (negative true).
NFANHI	Power supply fan at highest speed (negative true).
NFLG	I/O bus ready for data (negative true).
NIC1	I/O bus interface control bit 1 (negative true).
NIC2	I/O bus interface control bit 2 (negative true).
NIC3	I/O bus interface control bit 3 (negative true).
NIC4	I/O bus interface control bit 4 (negative true).
NIDO0	I/O bus input/output data bit 0 (negative true).
NIDO1	I/O bus input/output data bit 1 (negative true).
NIDO2	I/O bus input/output data bit 2 (negative true).
NIDO3	I/O bus input/output data bit 3 (negative true).
NIDO4	I/O bus input/output data bit 4 (negative true).
NIDO5	I/O bus input/output data bit 5 (negative true).
NIDO6	I/O bus input/output data bit 6 (negative true).
NIDO7	I/O bus input/output data bit 7 (negative true).
NIDO8	I/O bus input/output data bit 8 (negative true).
NIDO9	I/O bus input/output data bit 9 (negative true).
NIDO10	I/O bus input/output data bit 10 (negative true).
NIDO11	I/O bus input/output data bit 11 (negative true).
NIDO12	I/O bus input/output data bit 12 (negative true).
NIDO13	I/O bus input/output data bit 13 (negative true).
NIDO14	I/O bus input/output data bit 14 (negative true).
NIDO15	I/O bus input/output data bit 15 (negative true).
NIFC	I/O bus interface clear (negative true).
NIO0LED	I/O slot **0** LED on service panel (negative true).
NIO1LED	I/O slot **1** LED on service panel (negative true).
NIO2LED	I/O slot **2** LED on service panel (negative true).
NIO3LED	I/O slot **3** LED on service panel (negative true).
NIO4LED	I/O slot **4** LED on service panel (negative true).
NIO5LED	I/O slot **5** LED on service panel (negative true).
NIO6LED	I/O slot **6** LED on service panel (negative true).
NIOSB	I/O bus data transfer strobe (negative true).
NLOADLED	**LOAD** LED on service panel (negative true).
NMEMDUMP	**MEM DUMP** switch on service panel (negative true).
NMI	Non-maskable interrupt.
NMYPA	HP-CIO card recognized its address has been asserted (negative true).
NPA0	I/O bus peripheral address bit 0 (negative true).
NPA1	I/O bus peripheral address bit 1 (negative true).
NPA2	I/O bus peripheral address bit 2 (negative true).
NPDOP	Panel door open (negative true).

Signal	Definition
NPFW	Power fail warning (negative true).
NPOLL	I/O bus interface poll (negative true).
NPSLED	**PS** LED on service panel (negative true).
NPSTLED	Power supply overtemperature (negative true).
NRESET	**RESET** switch on service panel (negative true).
NRUNLED	**RUN** LED on service panel (negative true).
NSCMLED	**SCM** LED on service panel (negative true).
NSELFT	Leading edge causes power supply to send stack into self-test (negative true).
NSELFTEST	**SELF TEST** switch on service panel (negative true).
NSELFTESTLED	**SELF TEST** LED on service panel (negative true).
NST1LED	Stack **1** LED on service panel (negative true).
NST2LED	Stack **2** LED on service panel (negative true).
NST3LED	Stack **3** LED on service panel (negative true).
NST4LED	Stack **4** LED on service panel (negative true).
NST5LED	Stack **5** LED on service panel (negative true).
NST6LED	Stack **6** LED on service panel (negative true).
NST7LED	Stack **7** LED on service panel (negative true).
NST8LED	Stack **8** LED on service panel (negative true).
NST9LED	Stack **9** LED on service panel (negative true).
NST10LED	Stack **10** LED on service panel (negative true).
NST11LED	Stack **11** LED on service panel (negative true).
NST12LED	Stack **12** LED on service panel (negative true).
NSTART	**START** switch on service panel (negative true).
NSTLED	Stack overtemperature (negative true).
NSTS	I/O bus status (negative true).
NSYNC	I/O bus interface poll (negative true).
NTEMPLED	**TEMP** LED on service panel (negative true).
NWAIT	I/O bus lengthen IOSB (negative true).
PPON	Primary power on; all outputs in spec.
READ	I/O bus data direction (high indicates data to IOP).
ST1	Stack self-test from slot 1.
ST2	Stack self-test from slot 2.
ST3	Stack self-test from slot 3.
ST4	Stack self-test from slot 4.
ST5	Stack self-test from slot 5.
ST6	Stack self-test from slot 6.
ST7	Stack self-test from slot 7.
ST8	Stack self-test from slot 8.
ST9	Stack self-test from slot 9.
ST10	Stack self-test from slot 10.
ST11	Stack self-test from slot 11.
ST12	Stack self-test from slot 12.
US4	POLL ANDed with NSELFT.
UPS1	Uninterruptible power supply.
UPS2	Uninterruptible power supply.

HP 97060A
Graphics Processor

This note provides the necessary information for you to install the HP 97060A Graphics Processor. In addition to the materials included with the HP 97060A, you need an HP 27112A GPIO interface card and cable option 001, and an RS-343-compatible monitor which accepts the sync pulse on the green signal.

The HP 97060A Graphics Processor provides high resolution (1024 × 1024 pixels), rapid graphics processing and a large variety of colors. The display format is 1024 pixels horizontal by 768 pixels vertical. You can also attach an HP 9111A Data Tablet for graphics input.

Materials Supplied

Check that the following materials are included with your HP 97060A.

Item	Quantity
HP 97060A Graphics Processor	1
Power Cord	1
Fast-Blow Fuses	
4A for 110V	1
6.3A for 220V	1
1.8 metre BNC cable	3
Installation Note	1

All software for the Graphics Processor is included with the BASIC 3D Graphics software and with the HP-UX DGL Graphics software.

The Model 520 BASIC Graphics Programming Techniques manual explains how to use the HP 97060A with the BASIC language system. The GRAPHICS/9000 Device Handler's manual explains how to use the HP 97060A with HP-UX.

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HEWLETT PACKARD

Technical Specifications

The HP 97060A Graphics Processor supports a monitor for graphics display. Separate outputs are provided for red, green and blue color data. Sync data is combined with the green signal.

Physical Description

Size: 432mm wide × 140mm high × 533mm deep
Weight: 13.6 Kg

Environmental Specifications

Temperature: 0°C to 55°C operating, −40°C to 75°C storage
Humidity: 5-95% RH @ 40°C
Maximum Operating Altitude: 15,000 ft. or 570 millibars

Electrical Specifications

Rated Line Voltage:

110V range: 90 to 132 Vac
220V range: 180 to 264 Vac

Frequency Range:

47 to 66Hz

Power Consumption:

110V: 4A
220V: 6.3A

Video Output Level

Levels and timing are RS-343 compatible.

Red and Blue Signals:

0.9V peak to peak into 75Ω nominal

Sync/Green Composite Output Mixture:

Video composite 1V peak to peak.

Video - 0.7V typical
Sync - 0.3V typical

Display Format

Standard:
1024 × 768, 33Hz, interlaced

Colors

256 entry color map for 16,777,375 colors.

Cables

1.8m, 75Ω BNC cable; three total

Monitor Bandwidth Requirements

36 MHz

The monitor must have a composite sync (on Green) capability.

Unpacking and Inspection

If the shipping package is damaged, ask the carrier's agent to be present when the equipment is unpacked. If the equipment is damaged or fails to operate properly, notify the carrier and the nearest HP Sales and Support office immediately. Retain the shipping carton for the carrier's inspection. The Sales and Support office will arrange for the repair or replacement of your equipment without waiting for the claim against the carrier to be settled.

Installing the HP 97060A

There are three major pieces which you must install, the HP 27112A GPIO interface card, the HP 97060A Graphics Processor and the monitor.

Note

Make sure that power to the computer is turned off before attempting to install an interface card. Opening the computer's interface card cage door while the computer is on results in an immediate powerdown of the system. Any data and programs resident in memory at that time are lost.

Should this occur, turn the computer's power switch to the 0 (OFF) position and then complete the interface installation procedure.

---

1. Turn off the computer.
2. If you have a Model 520, open the cosmetic door on the right side of the computer. If you have a Model 530 or 540, go to step 3.
3. Open the interface card cage door by turning both thumbscrews counterclockwise and pulling the door open. On the Model 520, it is behind the cosmetic door. On the Model 530 and 540, it is at the back of the computer. With the HP 97098 I/O Expander, you can use either card cage.
4. Interface cards are plugged into the computer's interface card cage. Each slot in the interface card cage is assigned a unique number called a select code. An interface card occupying a slot assumes that slot's unique select code. The computer uses the select code to interface with the card, and thus with the device(s) connected to that card. Select codes are assigned to the slots sequentially. With the Model 520, four slots are available, from top to bottom, 2 thru 5. With the Models 530 and 540, seven slots are provided, 0 thru 6. The first I/O Expander, assignments are from 8 thru 11 and 12 thru 15. For the second, they are 16 thru 19 and 20 thru 23.

CAUTION

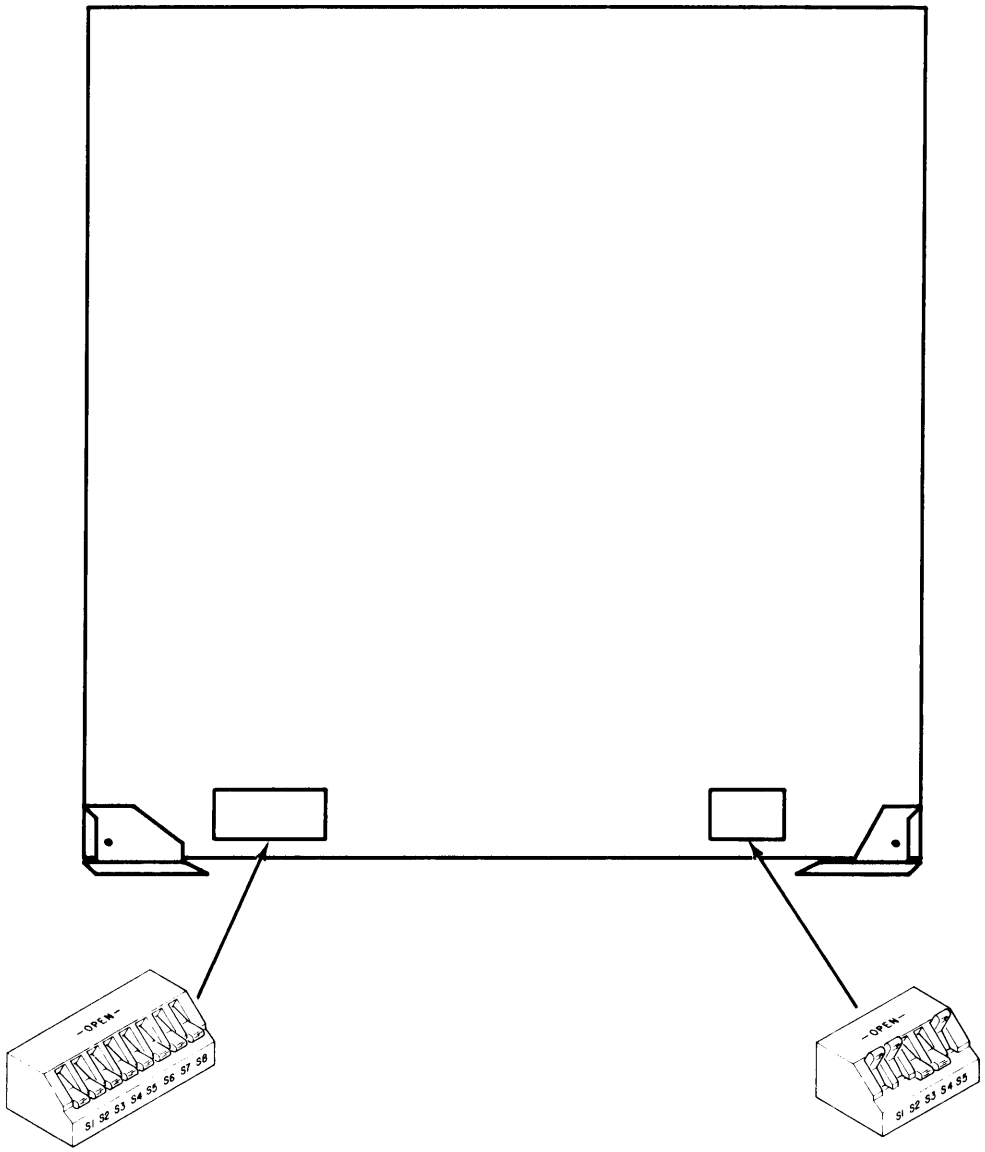
STATIC DISCHARGE CAN DESTROY COMPONENTS ON AN INTERFACE CARD. HANDLE THE CARD BY USING ITS ANTI-STATIC CONTAINER OR BY THE EJECTORS ON THE CARD. DO NOT TOUCH THE ELECTRICAL TRACES OR SET THE CARD ON ANY SURFACE OTHER THAN ITS ANTI-STATIC CONTAINER.

---

5. If the interface card has not already been installed, remove it from its anti-static bag and set it on the bag.

6. There are two sets of switches along the cabling side of the card. The Graphics Processor requires the following GPIO switch settings. Note that a switch that is Up is in the open position and represents a logic one; a switch that is Down is in the closed position and represents a logic zero.

   For more information, see the HP 27112A General Purpose I/O Interface (GPIO) Installation manual.



HP 27112A Switch Settings for use with the HP 97060A

7. BASIC and HP-UX assume slot 4 (select code 4) as the default location of a HP 97060A interface but any slot may be used. If your interface card is already installed the way you want it, skip to step 11.
8. Orient the card so that the connector is facing into the card cage and is on the right side of the slot. Holding the interface card by its ejectors, slide the card into its slot.
9. To seat the card, push firmly on the ejectors of the card with your thumbs. The ejectors should be flush with the edge of the interface card.
10. Connect the interface cable to the female connector on the interface card. The cables feed out the right side of the card cage door.
11. Close the interface card cage door. Push in and turn the thumbscrews clockwise until they are tight.
12. If you have a Model 520, shut the cosmetic door.
13. Unpack and set up your monitor near your computer. See the monitor's documentation for more instructions.
14. Unpack the HP 97060A Graphics Processor and set it near your computer.
15. If you intend to use an HP 9111A Data Tablet with your system, also set that up. One common configuration is to place the tablet directly in front of the monitor.
16. When the equipment is in place, connect the GPIO interface cable to the connector in back. This connector is labelled "J9/GPIO HOST". The connector only fits one way so if you have trouble attaching it, check its orientation.
17. Connect one of the 1.8 metre BNC cables from the red signal output jack of the Processor to the red signal input jack of the monitor. The Processor's jack is labelled "J1 RED". Check your monitor's documentation to determine which input jack to use.
18. Use the other two BNC cables to connect the green and blue jacks in a similar manner.
19. The video signal must be terminated with 75Ω. To do this, check your monitor to see if it has a 75Ω/HI IMPEDANCE switch or switches. Set it to 75Ω. Some monitors do not have this kind of switch. In this case, check the monitor's documentation.
20. If you intend to use the HP 9111A Data Tablet, connect an HP-IB cable from the Data Tablet to the input jack on the Processor labelled "J10/GPIB TABLET". Ensure that the Data Tablet's device address is set to 6. Ensure that no other interface cable is connected to the Data Tablet.

CAUTION

ENSURE THAT THE PROCESSOR IS CONFIGURED TO MATCH THE INPUT LINE VOLTAGE.

21. Now connect the power cords to the Processor and monitor and optionally to the Data Tablet.
22. Turn on your computer, your Processor, monitor and Data Tablet.
23. If you have a Model 520, load the SYSTEM INTEGRITY TESTS system into your computer and run the HP 97060 test.
24. Adjustment of your monitor's horizontal or vertical hold may be necessary to get a stable picture. If so, see the monitor's documentation for instructions.

25. If there are any problems, go through the preceding steps to determine if you have done anything wrong. In particular, make sure the interface card is seated squarely and tightly in the interface card cage, the cable is firmly connected to the interface card, that there are no broken cables, that the interface is properly connected to the Processor, that the Processor is properly connected to the monitor and that the monitor works properly. If you still have a problem, call your HP Sales and Support office for assistance.

Manual Comment Sheet Instruction

If you have any comments or questions regarding this manual, write them on the enclosed comment sheets and place them in the mail. Include page numbers with your comments wherever possible.

If there is a revision number, (found on the Printing History page), include it on the comment sheet. Also include a return address so that we can respond as soon as possible.

The sheets are designed to be folded into thirds along the dotted lines and taped closed. Do not use staples.

Thank you for your time and interest.

MANUAL COMMENT SHEET

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for the HP 9000 Models 530/540

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