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NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline).

Ltr	REVISIONS	DATE	INITIALS
A	as issued	10-16-85	DLK

Model No. 98546A	Stock No.
Title Theory Of Operation	
Description	Date
By Dave Dahms	Sheet No. 1 of 16
Supersedes	Drawing No. A-98546-66570-9

9320-3246 (6/75)

HEWLETT PACKARD

THEORY OF OPERATION
98546-66570 COMPOSITE VIDEO ALPHA BOARD

1 SCOPE AND GENERAL DESCRIPTION

1.1 Scope

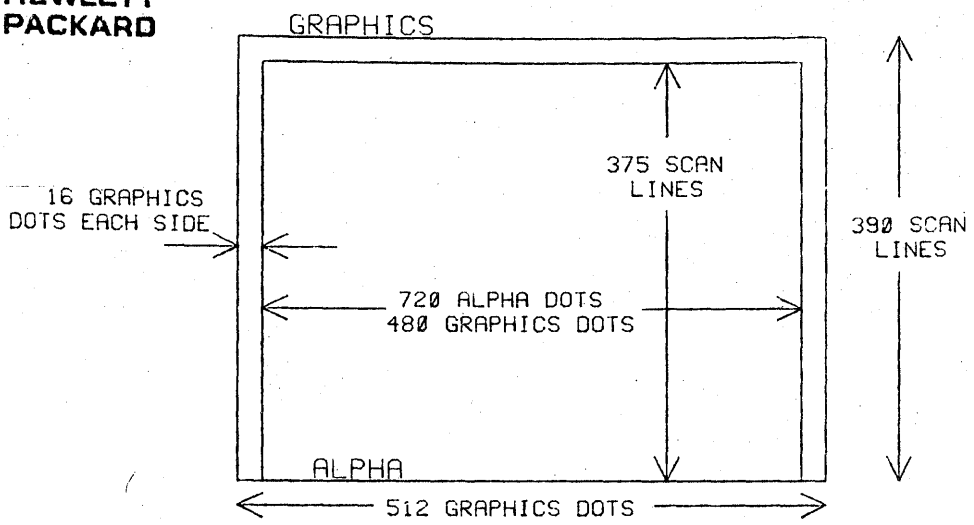
This document describes the circuitry contained on the 98546- 66570 display board. The board includes digital logic which controls monitor timing and produces the alpha display. The output of the board is a 1-volt composite video signal from a 75-ohm source impedance.

The following documents are referenced in this theory of operation:

D-98546-66570-4	Schematic	1 sheet
B-98204-66578-6	Block Diagram	1 sheet
B-98204-66578-7	Timing Diagrams	3 sheets
A-1820-3603-1	PAL Functional Description	4 sheets
A-1820-3604-1	PAL Functional Description	3 sheets
A-1820-3605-1	PAL Functional Description	5 sheets

1.2 Display Capability:

The 98546A card set provides memory mapped video capability identical to that of the 9817A for Series-300 computers with bit-mapped alpha systems. The card set interfaces to an external monitor via a 75-ohm cable carrying a composite video signal. The external monitor must be capable of operating with 50 or 60 Hz vertical rate, 24.9 kHz horizontal, and a video bandwidth of at least 20 MHz. The 98546-66570 card provides the alpha-numeric function for the 98546A card set, generates the composite video output signal, and also interfaces to the 98204-66577 graphics card. The card contains a character ROM programmed with two different character sets of 256 characters each, which are selectable by means of a switch on the card. Each set provides all 128 std ASCII characters, but they differ in the other 128 characters which are available, as well as in the manner in which the characters are mapped. The card also provides character attributes. These are: half-bright, underline, inverse video and blinking. These functions are stored independently in separate memory so they may be used in any combination at each character location without reducing the number of characters displayable on the screen. The alpha-numeric display capacity is 25 lines of 80 characters per line. The alpha character cell size is 9x15 pixels, with most characters fitting into a 7x9 pixel format. This gives a total alpha display area that is 720 pixels wide and 375 scan lines high. The 98204-66577 graphics card provides an array of pixels 512 wide and 390 high. Alpha and graphics dots do not overlay. One graphics dot = 3/2 of an alpha dot in the horizontal dimension, but their vertical spacings are identical. On a properly adjusted screen, graphics dots will be isotropic, i.e. spaced the same in the horizontal direction as they are in the vertical. The graphics display area extends outside the alpha area by 16 graphics dots on each side, and extends 15 scan lines above the alpha area in the vertical direction. (See diagram below.)



The video mixer circuitry exclusive-OR's alpha and graphics dots as they are being displayed so that where they overlap the resulting pixel will be turned off. The only exception to this occurs when the alpha information is being displayed in half bright: In such a case, the graphics information will be displayed in full brightness regardless of the the alpha information coincident with it. This standard was adopted by the 9836A display in an effort to maintain compatibility with the 9826A display. Where possible, the 98546A cards have been designed to be compatible with the 9836A display. The alpha and graphics displays are both memory mapped. Access to the display memory is time multiplexed, or windowed. After each character cycle to the display, a time slot is available for read/ write access by the mainframe to the display memory. The interface is asynchronous, which means that the access time of the display memory is variable. The best case time from address strobe true to DTACK* true is about 320 nsec. The worst case is about 1000 nsec. The alpha and graphics displays can be turned on and off independently of each other without disturbing the memory contents of either. The alpha display is turned on and off by writing a byte to the LSI controller chip. The graphics display is turned on if its memory is accessed (either a read or a write) with A15 low, and turned off if A15 is high. The 98546-66570 is very similar to the 98204-66578. The only difference is the 98546 contains a BNC video input jack and a relay to switch between the normal video and the externally provided video.

2 SOFTWARE ACCESS

2.1 Accessable Features

Software may access the following portions of the alpha card: display character memory, display attribute memory, CRT Self-identify register, 6845 crt controller, and two mode-control registers. There are 2K bytes of read-write memory available for character storage, and 2K bytes of attribute (inverse video, blinking, etc.) memory. This memory is organized word-wide on the data bus, with character information on the lower data bus (D0-D7; odd addresses) and attribute information on the upper data bus (D8-D15; even addresses). Each

address contains the information for a single character position, and all memory can be written to or read via the DIO bus. The desired starting address for the displayed screen is written to the 6845 CRT controller, and the character located at this address is displayed at the upper left corner of the screen. The characters at the addresses following the starting addresses are displayed sequentially from left to right until 80 characters have been displayed; the character at the next address becomes the first character in the next line, and so the screen is filled with 25 lines of 80 characters. The remaining 48 characters in memory are not displayed. The soft key label area is implemented by using the half bright, inverse video, and underline attributes. The 6845 supports a mechanism for blanking either the text or soft key areas of the screen or both, without affecting the contents of display memory. A CRT self-identify register is provided, which gives information concerning the type of CRT, initialization constants, graphics format, presence of attributes, 50 or 60 Hz refresh, and type of character ROM. This register is accessed by reading the highest address in alpha memory. The alpha card also supports the 9836A method of indicating 50 or 60 Hz refresh by connecting the highest bit in the attribute byte to the 50/60 Hz select switch during reads. A 6845 CRT controller chip handles most of the screen formatting. This is a programmable part, and must be initialized by software to supply proper timing for the system. These setup parameters are iden- tical to those used by the 9836A, and are listed in section 2.3. The hardware supports both reads and writes to the 6845, which allows the current cursor position to be read. (The cursor position and type are programmed by writes to the appropriate registers in the 6845.) The alpha card also contains two registers used for mode controls: one register is used to provide proper graphics positioning for 50 or 60 Hz operation. The other controls the relay that selects which video signal to send to the monitor. Both of these mode controls are exercised by accesses to appropriate memory addresses.

2.2 Memory Space Usage

2.2.1 Display Memory Addressing and Functions

Screen memory begins at address 512000 (hex). The attributes are stored in the high (even) bytes, and the character codes in the low (odd) bytes, with each word corresponding to a single displayable character. Screen memory consists of 2K words, and may be accessed to either byte individually or as words. The screen memory is multiply mapped in the rest of the space above 514000, and accesses to these addresses result in the activation of other features: A write to screen memory addresses where A15=1 (51A000 and above) will activate the relay to send the externally provided video to the monitor. Address line A14 is used to enable access to the 50/60 Hz selector for graphics timing, with the state of A2 used as data to the latch. For example, a read or write to 516004 (A14=1, A2=1) sets the graphics vertical retrace timing for 60 Hz operation; a read or write to 516000 (A14=1, A2=0) sets up the timing for 50 Hz. (Note that graphics timing only is affected by this latch; alpha timing is changed by writing different parameters to the 6845.) The addresses at the very top of alpha memory include the CRT-ID (self-identify) register. See section 2.2.2 for exceptions to the above

rules in the CRT-ID addresses.

2.2.2 CRT Self-Identify Register (CRTID)

A self-identification register is provided to give the host computer the necessary information to initialize the 6845 CRT controller properly, and also to provide such inputs as graphics parameters, 50 or 60 Hz operation, presence of alpha attributes, and type of character set. This register was intended to be read as a word at address 51FFFE, but the way the circuitry decodes the register select line, it is accessed only by memory reads, and at any address at or above 51FC02 where A15, A14, A13, A12, A11, A10, and A1 are all equal to 1. The circuitry disables access to the 50/60 Hz latch (see section 2.2.1) when the CRTID register is being accessed. The information contained in the CRTID register is given below. For more detailed information, refer to the boot ROM documentation for your processor board.

```
CRTID<15>      - 0; not self-initializing
CRTID<14>      - 0; reserved value
CRTID<13>      - 0= 9826 extended Roman character set;
                 1= USASCII plus Roman8 character set
CRTID<12:11>   - 0; monochrome display
CRTID<10:8>    - 2; alpha highlights, 512 x 390 graphics,
                    80-wide alpha
CRTID<7:4>     - 1; 6845 constants identical to 9836A
CRTID<3>       - 0= 60 Hz;
                 1= 50 Hz
CRTID<2:0>     - 0; 6845-based alpha board
```

For example, a card with its switches set for the old-style (9826) character set and 60 Hz refresh would return a CRTID of 0210 hex.

2.2.3 6845 Access

The 6845 CRT controller is accessed by first writing to the pointer register at address 510001. The byte written to this address points to the internal 6845 register to be accessed at the next read or write. A read or write to 510003, then, will access the intended register. The address space from 510001 to 511FFF and 518001 to 519FFF contains multiple mappings of these functions because only the value of A1 is used in this space. The circuitry will respond to reads and writes to either the high or low byte or to words, but only the lower (odd) byte contains valid data. Also, note that not all registers of the 6845 will return valid data on a read. Consult a Motorola or Hitachi data book for details of 6845 register accesses.

2.3 6845 Register Definition

The 6845 contains 16 registers, R0-R15. The first 12 registers should not be changed from their power-up initialization, as they affect hardware timing. The last 4 may be modified as required by the system software. The functions of these registers are listed below:

R12 - Start address (H)
R13 - Start address (L)
These two registers determine the address of the character which appears in the upper left corner of the screen, and also perform some control functions. (see 2.4 Display "Areas.")
R14 - Cursor position (H)
R15 - Cursor position (L)

For a more complete description of the internal registers, consult a manufacturer's databook by Hitachi or Motorola.

Each of the 16 registers of the 6845 CRT controller must be initialized at power-up before any writes to alpha or graphics memory. This function is typically performed by the boot ROM as soon as it determines that the card requires the same initialization values as used in the 9836A. These values are as follows:

	60 Hz Data		50 Hz Data	
Register	Dec	Hex	Dec	Hex
R0	114	72	114	72
R1	80	50	80	50
R2	76	4C	76	4C
R3	6	06	6	06
R4	26	1A	32	20
R5	10	0A	3	03
R6	25	19	25	19
R7	25	19	28	1C
R8	0	00	0	00
R9	14	0E	14	0E

The remaining registers may be set up as desired. For a two-line cursor which blinks at 1/16 the frame rate, R10=76 Dec, R11=13 Dec.

2.4 Display "Areas"

The 6845 has 14 address lines, which are intended to be used to access the display memory. However, since only 11 lines (MA0- MA10) are needed to address the 2K words of display memory, this leaves 3 lines, nicely synchronized with the screen information. As in other Series 200 displays, the 98204B alpha card makes use of these lines to provide a convenient way of dividing the screen into two areas, typically "text" and "soft key" areas. The boundary of the two areas occurs where MA11, the "field " (FLD) line changes between 1 and 0. Thus, by proper selection of the starting address in the display memory, the screen may be defined as being all text (MA11=0), all soft key area (MA11=1), or change from text to soft keys (or vice versa) at any desired point on the screen. Address lines MA12 (KEYS) and MA13 (TEXT) are defined as mode control lines for the soft key and text areas of the screen, respectively, and are used to independently turn the alpha information on and off in these areas without modifying the contents of display memory. The modes are defined so that a "1" means that the alpha

information will be turned on when the FLD line indicates that information is being displayed in the appropriate area.

TEXT	KEYS	Function
0	0	Alpha off in both areas
0	1	Information in soft key area displayed; text off
1	0	Information in text area displayed; soft keys off
1	1	Information in both areas displayed

Like FLD, values are assigned to the TEXT and KEYS lines by specifying the starting address to the 6845. (The "starting address" is the address in display memory of the character to be displayed in the upper left corner of the screen.) Since the display memory is multiply mapped in the 6845's address space, a starting address of 30D0 will give a screen with two lines of soft keys at the bottom of the screen, and both text and soft keys turned on, while a starting address of 20D0 will give the same screen except the characters and attributes in the soft key area will be turned off. This method of mode control does complicate the way the display memory maps into the screen: Note that in the last example the character that was stored at address 512001 appears as the first character in the soft key area. The character at the top, left corner of the screen was stored 208 characters later (D0 hex): This amounts to 2 lines of 80 characters per line plus 48 characters which will not be displayed (2048- 2000). In terms of the system address, the offset is doubled because screen information is stored one word per character. This gives a memory offset of 416 dec, 1A0 hex. Thus, the character at the top, left corner of the screen was stored at address 5121A1.

3 FUNCTIONAL DESCRIPTION

3.1 System Overview

The 98546-66570 Alpha card contains the character and attribute R/W memory, the character set ROM, a 6845 controller chip, a digital-to-analog converter, and miscellaneous circuitry necessary for system interface and control. A detailed discussion of these parts is presented below. The discussion makes references to the block diagram, timing diagrams, and schematic for the 98546-66570 assembly.

3.2 Definition of Signals

Reference is made in this discussion to the following signals on the block diagram or timing diagrams:

3.2.1 System Interface Signals

BD0-BD7	lower 8 bits of the system data bus
BD8-BD15	upper 8 bits of the system data bus
BA1-BA23	the system address bus
BR/W	the system read/write line (low = write)
DTACK*	system data transfer acknowledge (negative true)
BLDS*	system lower data strobe (negative true)
BUDS*	system upper data strobe (negative true)
BAS*	system address strobe (negative true)
IMA*	"I'm addressed" line (negative true) used by bus expander

3.2.2 Alpha Card Internal Signals

CLK	alpha dot clock (25.7715 MHz)
CCLK	character clock (1/9 of CLK frequency)
S/L	shift/load timing signal
X,Y	state counter outputs
AGSYNC	alpha-to-graphics synchronization
DLE*	data latch enable (active low)
SEL	synchronized alpha memory selected
EXADR*	external (system) access to CRT RAM (negative true)
ROE*	RAM read output enable (negative true)
WOE*	write to RAM output enable (negative true)
WE*	write to RAM enable timing (negative true)
ACS*	alpha card selected (negative true)
E	6845 register enable
ES	6845 register access select
CSYNC	composite horizontal and vertical sync

3.2.3 Interface to Graphics Card

GRES*	graphics reset (negative true)
WRITE	inverted BR/W (high = write)
GVIDEO*	graphics video data input (low = pixel on)
GHRTC	horizontal sync for graphics
GVRTC*	vertical sync for graphics
AGSYNC	alpha-to-graphics synchronization
ACLK	alpha dot clock (25.7715 MHz)
G GND	ground return for ACLK

3.3 Block Diagram Subsystems

The following discussion of alpha circuitry is organized according to the blocks of the block diagram. Component references are made to the circuit schematic, and timing reference to the timing diagrams.

3.3.1 Address Decode Logic

U45, U46, U39, and parts of U12, U19, U20, U30, and U31 are included in the address decode function. U45 buffers certain of the address lines and the upper and lower data strobes so that they present a single gate load to the system bus. Portions of U20 and U30 do the same thing for BR/W and BAS*. U46 serves as an address comparator on the top 8 bits of the address bus to provide an "alpha select" function, since all alpha addresses are contained in the range of 51xxxx. U39 is a PAL programmed to do most of the address-based system selection. For instance, U39 provides the select signals for the CRTID registers, memory output latches, and 6845 register access enable based on their appropriate addresses. In addition, it provides a memory address select signal which is synchronized to the dot clock by U31 to produce SEL. U39 also drives DTACK* and IMA* of the system bus. For details of U39's internal code, see the drawing A-1820-3603-1.

3.3.2 Data Bus Buffer

U47 and U48 are bidirectional tristate buffers used to minimize loading on the system data lines. This buffer is enabled by ACS* whenever the alpha card is addressed, and its direction is controlled by the system read/write line.

3.3.3 CRT ID Register and Configuration Switches

U41 and U42 are tristate buffers used to output the self-identify code to the system bus when selected by the proper address. Most of the code is hard-wired to the inputs of the buffers, but two bits of data are switch selectable: These are the bits for 50/60 Hz screen refresh and for the character set selection. These bits are provided by SW1 and its pull-up resistors, R5 and U3 pin 5. The 50/60 Hz line goes to the internal data buffer (see 3.3.4) as well, where it is tied to the highest bit of the attributes buffer on memory reads. This was done to insure compatibility with the 9836A, which does not contain an ID register but uses this method instead for indicating whether 50 or 60 Hz refresh has been selected. The character set select bit goes to the character ROM (see 3.3.7) where it makes the actual selection between the two character sets stored therein.

3.3.4 Internal Data Buffer

This block includes two tristate buffers, U35 and U36, and two tristate latches, U33 and U34. These components serve to isolate the internal data bus from the buffered external system bus. The buffers are enabled during writes to the RAM after the RAM outputs have been disabled. The latches are used during memory reads to hold the RAM data as long as the system requires to read it, which is necessary because the RAM must be accessed immediately by another screen refresh cycle.

3.3.5 Character and Attribute RAM

U9 and U10 are the character and attribute RAMs, respectively. These parts are 2K x 8 static RAMs with 100 nsec access times, which specification is necessary to allow two RAM accesses during one character cycle--one for CRT refresh and the other for system access (if requested). Timing for these access cycles is controlled by the state machine, des- cribed in section 3.3.16.

3.3.6 Character and Attribute Latches

U27 and U28 are used to latch the character and attribute data from RAM, as well as the row address data produced by the 6845 CRT controller. The character data and the 4 row address lines go to the character ROM. The attribute data goes to the video mixer. These latches are clocked once per character cycle by the S/L signal.

3.3.7 Character ROM

U8 is an 8K x 8 ROM programmed with two different character sets. The pinout and speed requirements of the part make it compatible with 300 nsec 2764A EPROMs. The characters patterns are programmed such that the most significant bit of the ROM is used to select between the two character sets. This bit is tied to the character set select switch. (See 3.3.3.) The 8 next most significant bits are used as the character code, and the 4 least significant bits define which row of the character is to be displayed. The 8 outputs of the ROM, then, contain the dot information for the specified row of the desired character, plus a single bit which indicates whether or not the information on that row is to be shifted by half a dot. The 7 dots are centered in the 9-wide cell, and blank spaces are inserted at either side to fill out the 9 dots. Most of the characters fit into a 7 x 9 format, although some use the available space for ascenders or descenders. The ROM contains

sufficient space for characters to extend the full 15 dots of the cell height if necessary.

3.3.8 Parallel to Serial Shifter

U13, U14, and part of U31 form a parallel to serial converter. U13 and U14 are parallel-in, serial-out 4-bit shift registers which are loaded with one row of a character pattern on the rising edge of CLK while S/L is in its "load" state. The character is shifted out, then, on subsequent positive transitions of CLK. U31 adds one dot of delay in the bit stream to center the character pattern in its cell. It was an unfortunate bit of myopic design stealing, because the identical function could have been performed using the Qd output (pin 12) of U13, which would have freed up the latch for another purpose. (Sigh.) Apparently the original design used a FAST device for U31 to gain some timing margin going into the half shift circuit.

3.3.9 Half Shift and Dot Stretcher

The half shift circuit consists of parts of U11, U6, and U20. One of the gates of U6, an AS804, is used to invert the clock going to U11, an F74 D-type flip flop. U11 latches the data from the parallel to serial shifter on the falling edge of CLK, yielding the same data but delayed by half a clock period (i.e. half a dot). Three more gates from U6 and an inverter from U20 are combined to form a 2-to-1 data selector: If the input to U20 (the half shift select bit, latched and inverted by U15) is a "1", the data selector will select the output of U31; if a "0", the output of U11, the half-shifted data, will be selected. The dot stretcher circuit includes R2, C2, C3, and parts of U1 and U2. The circuit inverts alpha dots and stretches them, i.e. increases their "on" time, to compensate for the limited bandwidth of typical video amplifiers in display monitors. Without this function, vertical lines appear dimmer than horizontal lines. The dot is stretched by the RC response of U1 pin 13 (470 ohms) and C2 (22 pF), and by the saturation recovery time of the transistor.

3.3.10 Video and Attribute Mixer

The attributes are stored in the attribute RAM as follows:

BD8	Inverse Video
BD9	Blinking
BD10	Underline
BD11	Half Bright

Where there is no graphics or cursor information to complicate things, the attributes act in the following way: Underline adds a line (i.e. turns on all the dots) across the bottom row of the character cell. Inverse video inverts the character data in a cell as it is displayed: Characters and underlines appear as dark dots on a lighted background. Blinking causes the characters and underlines to appear and disappear with respect to their background colors (dark or light) at about a 1 Hz rate. Half bright causes all of the lighted dots in the affected cell to appear dimmer than normal. The video and attribute mixer consists of U15, U25, and parts of U32. The mixer takes all of the signals which affect the presence, absence, or intensity of the dots on the screen and combines them logically to produce two signals, HALF*

and FULL*, which directly turn the dots on and off. U32 pin 12 provides a "1" when the scan count reaches 14, indicating the bottom scan of the character cell, where the underline will be placed if it has been selected via the appropriate attribute bit. U32 pin 8 ANDs the blinking attribute bit with a square wave produced by U25 which has a frequency equal to 1/64 the vertical scan rate. This yields a "0" when the blinking attribute is not set, or a square wave of 0.94 or 0.78 Hz (depending on the vertical scan rate) when set. U25 is an 8-stage ripple counter which gets its input from the vertical retrace signal generated by the 6845 CRT controller; only the output of the 6th stage is used, however, to produce the desired blink rate. U15 is a PAL programmed to do the rest of the logical combination of video-related data. The part is a 16R4A, with 4 data internal latches which share a common clock, in this case S/L. One of the latches is used by the half-shift bit. (See 3.3.9.) The other three are used to delay the attributes by one character time so they will be properly phased with the character information. The video and attribute mixer implements the rules for combining the attributes with cursor, alpha dots, and graphics dots as they were established by the 9836A. The following table describes the mixing function as implemented in the 98546-66570. (For the exact PAL equations, see A-1820-3604-1.) Please note that the interface to the Digital to Analog Video Output circuit was designed so that a half-bright dot yields a logic true (i.e. low) on the HALF* signal, while a normal dot yields a logic true on both the HALF* and FULL* outputs.

KEY: GRAPHICS =Graphics video (dots)
HALF = Half Bright attribute
INV = Inverse Video attribute
ALPHA = Alpha video (includes dots, underline attribute, and blinking attribute)

F = Full-bright pixel
H = Half-bright pixel

GRAPHICS	HALF	INV	ALPHA	CURSOR OFF OUTPUT	CURSOR ON OUTPUT
0	0	0	0	0	F
0	0	0	1	F	0
0	0	1	0	F	0
0	0	1	1	0	F
0	1	0	0	0	H
0	1	0	1	H	0
0	1	1	0	H	0
0	1	1	1	0	H
1	0	0	0	F	0
1	0	0	1	0	F
1	0	1	0	0	F
1	0	1	1	F	0
1	1	0	0	F	F
1	1	0	1	F	F
1	1	1	0	F	F
1	1	1	1	F	F

3.3.11 Digital to Analog Video Output

The video output circuit produces a nominal 1.12 Vp-p composite video signal into a 75 ohm load. Components of the circuit are Q1, C7, CR1-CR3, L1, and most of U1 and U2. U1 is a custom resistor array whose values have a 5% absolute tolerance, but have been matched to 1%. The three transistors of U2 are all connected in a common-base arrangement, with their bases tied to a resistive divider voltage reference. The emitters of the transistors are driven by the HALF* and FULL* video data lines and by the CSYNC signal through resistors. Because the voltage reference is 2.7 V, TTL output levels will drive the transistors into their active region at logic low and cut-off at logic high. Resistance values were chosen to give emitter currents in the desired ratios. Also, the logic functionality was chosen so that HALF* and FULL* must both be true for full-bright dots so that the currents in the three emitters would be roughly equal, and to minimize the current the FULL* driver must sink. The collectors of the transistors are tied together so that the sum of their collector currents will be sourced through the 68.1 ohm resistor (U1 pin 15) and CR1. The voltage drop across CR1 is essentially constant due to the fact that it is always biased "on" by U1 pin 7; hence, the voltage across the 68.1 ohm resistor is directly proportional to the sum of the currents being drawn through the transistors plus this bias current. Q1 is connected in a pseudo current mirror arrangement: Its base is connected to the current summing

junction at the cathode of CR1 such that the voltage across the base-emitter junction of Q1 is essentially equal to the voltage across CR1, and the voltage across the 34.8 ohm resistor at its emitter (U1 pin 14) is essentially equal to the voltage across the 68.1 ohm resistor. In this way, CR1 compensates for the Vbe drop of Q1, and the emitter current is equal to 68.1 / 34.8 times the current out of the summing junction. With the exception of the base current, this current shows up as the current out of the collector. The 51.1 ohm resistor at U1 pin 10 to ground provides a load resistance for the collector, and the 23.7 ohm resistor from U1 pin 10 to pin 9 adds to bring the output impedance to 74.8 ohms. The gain of the entire system has been designed to give the specified 1.12 Vp-p when a 75 ohm load is connected at the output terminal. CR2 and CR3 protect the circuit against electrostatic discharge at the output terminal, and the inherent nature of the design makes it immune to damage caused by operating with the output either open- or short-circuited. L1 is a common-mode inductor and was added to the circuit to reduce electromagnetic interference by helping to insure that video currents flow only through the video output cable. C7 serves to filter high frequency power supply noise out of the base bias circuit.

3.3.12 6845 LSI CRT Controller

For the purpose of this discussion, the CRT Controller section consists of U4, U5, and U7. U5 is the actual 6845 CRT Controller, an LSI chip containing circuitry to address screen memory for screen refreshes, generate horizontal and vertical timing signals, place a cursor on the screen, and blank the screen. U4 is a latch used to synchronize control signals with the character cycle, and U7 is a data selector used to do the screen "areas" mode control decoding (see 2.4). The 6845 controls the screen format, positioning of characters on the screen, and cursor position based on data written into its internal registers. Most of these values are written into the 6845 by the boot ROM in an initialization routine. The exceptions to this are the start address registers and the cursor position registers, which are modified as needed by the system. For more details of register definition, see section 2.3.

3.3.13 Crystal Oscillator

The crystal oscillator circuit includes Y1, L2, L3, and part of U6. Y1 is an integrated crystal oscillator which produces a 25.7715 MHz clock signal with a symmetry (duty cycle) between 45% and 55%. This symmetry specification is necessary to insure proper operation of the half-shift feature and the graphics "divide by 1.5" circuit. U6 is used as a buffer to provide sufficient drive capability to drive the clock loads on the board. Two gates are used to provide an easy way to attach an external clock signal during 3060 testing. L2 and L3 provide RFI protection which is necessary mainly because the clock is sent via ribbon cable to the graphics board.

3.3.14 Sync Pulse Conditioners

U17, U23, U29, U37, U18, and parts of U38, U44, U19, and U20 provide the sync pulse conditioning (i.e. stretching, delaying, etc.) necessary to convert the horizontal and vertical timing signals from the CRT Controller into the needed waveforms. U29 and U37 are 4-bit synchronous

counters which are used to generate the vertical retrace signal for the graphics board (GVRTC*). This signal is delayed as necessary depending on the contents of the 50/60 Hz register (part of U26) by controlling the values which are preloaded into the counters. U23 and half of U38 are used to generate the horizontal portion of the composite sync signal (CSYNC), with the assistance of some gates from U18 and U44. U17 and the rest of U18 are used to generate the vertical portion of CSYNC and tc combine the two together.

3.3.15 6845 R/W Timing

U43 and parts of U11, U12, and U19 control the timing of the Enable (E) signal to the 6845 and DTACK* to the system processor during accesses to the registers of the 6845. Timing cycles are initiated when the Address Decode Logic pulls E Select line (ES) "high." Two different cycles may be performed: One for writes to the 6845, the other for reads. These different cycles are necessary because the 6845 latches data into its internal registers on the falling edge of E during write cycles, which means that DTACK* may be asserted coincident with that transition; E must be held "true" after DTACK* is asserted during read cycles, however, to allow the system to latch the data being read. (The 6845 stops driving the bus when E goes "false.") Note that the circuit expects that BAS* will not be reasserted for at least 116 nsec after it has been released by the system: If this condition is not met, it is possible that a glitch may appear on the E line shortly after a read cycle. For timing details, see the timing diagrams (B-98204-66578-7).

3.3.16 Timing and Control State Machine

Timing and control are handled by a state machine consisting of U40, U26, and parts of U20, U30, U31, U32, U44, U16, and U12. References will be made to the Display Memory Timing diagram (B-98204-66578-7) in the following discussion of the operation of the state machine. The state machine runs a 9-dot cycle which is divided into specific access windows for screen refresh (CRT cycle) and for system access (CPU cycle). The screen refresh function is performed during every character cycle (so called because the characters are displayed in a 9 dot wide font which fixes the cycle to 9 states) in order to keep a steady stream of video information going to the screen. System accesses are performed in their allotted states only when the system requests them in order to make reads or writes to the display memory. Signals associated with the screen refresh include S/L, the shift/load signal to the latches and shift registers; DLE*, used to latch the 6845 outputs; AGSYNC, sent to the graphics board for synchronization with alpha; and CCLK, used as a clock by the 6845 to update the screen refresh address and other display timing. The system access portion of a character cycle uses the signals SEL and R/W as inputs: SEL is a synchronized access request signal which must be true by state S11 to initiate a system access; otherwise, the system must wait for the next time S11 comes around. R/W is used to determine whether a read or write to the memory will be performed. During system accesses, the state machine generates the proper signals on EXADR*, ROE*, WOE*, WE*, and DTACK* to complete the access. EXADR* is used by the RAM address multiplexer to select the system bus for address, and by other portions of the state machine itself. ROE* is used to enable the RAM outputs during data reads and to disable (tristate) them for writes. ROE* is also used to add a second stage of

synchronization in case SEL is not a stable signal after insufficient set-up time: ROE* must go high at S12 or the system access is aborted and the system is held off until the next character cycle for its access. WOE* and WE* control the internal data write buffers and the RAM write enable inputs, respectively, during memory writes. DTACK* is asserted when EXADR* goes false (high), indicating that the memory access is complete and, in the case of a memory read, that data is valid on the system bus. Most of the state machine functions are performed by U40, a 16R8A PAL programmed for the task. For details of the state machine code, see A-1820-3605-1. U26 contains two latches, one of which (pins 5 and 6) is used to control the video switching relay depending on the state of A15 during writes to the memory space. (See 2.2.1.) The other latch (pins 9 and 8) is used to select between 50 and 60 Hz refresh for graphics vertical timing: A "1" at pin 9 (the "Q" output) results in 60 Hz timing. This latch is addressed by setting A14=1 on a memory access other than reads of the CRTID register; data for the latch is taken from A2. (See 2.2.1.) Part of U38 is used to hold the state of the DTACK enable. Two of the latches of U31 are used in the state machine to generate the WE* and DLE* signals.

3.3.17 Address Multiplexer

U16, U21, and U22 are data selectors used to multiplex the external (system) address and the refresh address ontc the RAM address lines. The EXADR* signal is used to select the appropriate address.

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