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NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline).

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Model No.	Stock No.
Title	Monochrome Display Card Theory of Operation
Description	Date
By Steve Wolf	Sheet No. 1 of 11
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HEWLETT
PACKARD

MONOCHROME DISPLAY CARD

THEORY OF OPERATION

Revision 18 Jun 1985

Steve Wolf

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Introduction	Chapter 1

1.1 Coverage

This document covers the internal workings of the two flavors of monochrome display boards for 98542A made from the 98542-26570 printed circuit board. These two products are the medium-resolution (1024 x 400 pixels) display board (98542A) and the high-resolution (1024 x 768 pixels) display board (98544A).

1.2 Nomenclature

In this document and on the 98542-66570 schematic, an 'N' before a signal name denotes that the signal is active-low, or 'negative true'.

Bus signals are differentiated from buffered signals by the presence or absence of the DIO 'B' nomenclature. For example, NBAS is Bus Address Strobe (active-low) and NAS is Address Strobe after it has gone through the 74ALS244 input buffer.

A dollar sign before a number indicates that the number is in hexidecimal representation.

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2.1 Address Decoding Circuit

The heart of the address decoding on the Display Board is a 16L6 Programmed Logic Array (U28). In order to get all the needed address and control lines into the sixteen inputs of the PLA, two groups of five address lines (A2-A6 and A7-A11) are fed through five-input NOR gates (U44) and then into the PLA. When the lower bits of the address are in the range $000 - $003, the outputs of the NOR gates are high.

The PLA's decoding signals are as follows:

Output Signal	Address Range (hex)	Signals
Pin 16 (NLOREG)	560000:560003	NAS low
Pin 17 (NHIROM)	560004:563FFF	NAS low, R/NW high
Pin 18 (NIMAC)	020000:02FFFF; 560000:56FFFF	NAS low
Pin 20 (NTC)	020000:02FFFF; 564000:565FFF	NAS low
Pin 21 (NFB)	020000:02FFFF	NAS low

2.1.1 NLOREG

This signal indicates that either the ID Register or the Interrupt Register is being addressed. It is further decoded by the 74ALS138 3-to-8 Demultiplexer (U36) into NREAD1 (Read ID Register), NWRITE1 (Write ID Register), NREAD3 (Read Interrupt Register), and NWRITE3 (Write Interrupt Register).

2.1.1.1 NREAD1

The ID of the Display Board is contained in the 2764 Display ID ROM (U11). This signal enables the ROM.

2.1.1.2 NWRITE1

A write to the ID Register is defined as a soft reset. The effects of a soft reset are discussed in Section 3.1.

2.1.1.3 NREAD3

The Interrupt Register (U37) contains the interrupt level bits (3) and interrupt enable bit. The interrupt request bit comes from the CRT Controller. These bits are sent through a 74ALS244 Buffer (U38) to the Data Bus. The NREAD3 signal enables this buffer.

2.1.1.4 NWRITE3

This signal, combined with the NDTACK generation signal (U32-8), clocks the Interrupt Register (U37), which contains the interrupt level and interrupt request bits. The inputs to the four latches are connected to the appropriate data lines.

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2.1.2 NHIROM

NHIROM enables the 2764 Display ID ROM (U11). The contents of this ROM are discussed in the Display ID ROM Definition.

2.1.3 NIMAC

When the Display Board is addressed, it must return an "I Am Addressed" signal within 50ns if it is connected to a DIO Expander. For testing purposes, the NIMA signal is made available on the Display Board, but is not connected to anything.

NIMAC ("I Am Addressed Control") enables the NIMA and NDTACK buffers (U27A and U27D). It is AND'ed with NAS because when NAS goes away, the Display board must stop driving NIMA and NDTACK sooner than the time it takes for NIMAC to go inactive.

NIMAC also determines when the Bidirectional Buffers (U31 and U40) handling the data signals are enabled.

2.1.4 NTC

The TOPCAT Enable signal is doubly synchronized through a Hex Flip-Flop (U18) to become NSTC (Syncronized TOPCAT Enable). It then drives the Chip Select pin of the TOPCAT Chip (U5).

2.1.5 NFB

The Frame Buffer signal tells when the frame buffer is being addressed. This signal, after being inverted to FB, drives the FB/NTC pin of the TOPCAT Chip. It also enables some grounded buffers (U27B, U27C, U45B, and U29) so that the seven "unused planes" on the board return zeros during frame buffer reads.

2.2 Generating NDTACK

NDTACK comes from one of two places. If the CRT Controller (U5) is being accessed, it generates NTCDTACK by itself, which is passed on as NDTACK. If anything in the $560000 - $56FFFF address space other than the CRT Controller is addressed, NDTACK is generated by a shift register (U42). A BEGINDTACK signal is generated through U41D when either NLOREG or NHIROM is active. This signal pulls the RESET pin of the shift register up so that the register can start shifting ones.

On the low-resolution board (98542A), the third clock pulse to the shift register generates NDTACK, and on the high-resolution board (98544A), the fifth clock pulse generates NDTACK. The ROM access time remains constant (200nS), but the clock is faster on the high-resolution board than on the low-resolution board. NDTACK is generated for any access to the display address space, whether or not valid data is returned. For example, a byte read to location $560000 will receive a data acknowledge, even though the "data" is garbage.

2.3 Data Signals

The direction of the Bidirectional Buffers handling the data signals (U31 and U49) is determined by the R/NW signal. However, they are enabled only when the Display Board address space is addressed (indicated by NIMAC being active). In addition, only the byte(s) addressed are enabled (indicated by NUDS and NLDS).

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Reset Circuitry

3.1 Soft Resets

A soft reset can occur by writing to Register 1 ($560001) or by pulling the NRESET signal active while NHALT remains inactive. The soft reset is not allowed to alter the setup parameters of the CRT Controller (U5). The only function of this write is to clear the Interrupt Register (U37). Note that a soft reset does not clear the bit that indicates a pending interrupt from the CRT Controller.

After a soft reset, the interrupt level is set to zero, and interrupts to the DIO bus are disabled by disabling the 74LS156 3-to-8 Demultiplexer chip (U47) that drives those interrupt lines (NIR1 - NIR7). If interrupts are enabled before changing the interrupt level with a write to Register 3, there still will be no interrupts to the processor, since the non-maskable interrupt (NIR0) is not on the bus.

3.2 Hard Resets

A hard reset occurs when NRESET and NHALT are both active. It clears the Interrupt Register in the same way a soft reset does. In addition, it is doubly synchronized through two D-type Flip Flops (U35) and drives the NRESET pin on the TOPCAT Chip. This causes all registers in the TOPCAT to do whatever the TOPCAT ERS says they do, wiping out all initialization that may have been done.

Hard resets get the entire card, including the TOPCAT Chip, into a known state, with the exception of syncronizing the clock circuit. The clock runs and runs and runs with total disregard for hard resets. When a hard reset goes away, the aforementioned synchronizer guarantees that the TOPCAT Chip is synchronized with the clock circuit, rather than having to synchronize the clock circuit to the TOPCAT Chip.

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Interrupts

The Interrupt Register is defined in the DIO spec. Part of this register is the interrupt level bits, which define a level from one to seven. These three bits are sent to a 3-to-8 Demultiplexer with open-collector outputs (U47) which drives the appropriate interrupt line.

Another bit in the Interrupt Register enables or disables interrupts from the card. This bit has to be high for an interrupt from the TOPCAT Chip to enable U47 and drive an interrupt line.

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How the Clock Circuit Works

The clock signal originates, of course, in the oscillator (Y1). It is immediately buffered by a screaming-fast inverter (U32C). This buffered signal runs the video output shift register (U16) and two pairs of J-K Flip-Flops (U33 and U17).

The first pair of J-K Flip-Flops (U33) is set up so the first toggles on each clock (divide-by-two) and the second toggles on every other clock (divide-by-four). Thus, the Flip-Flop pair runs through four distinct states, which can be defined by the Q-outputs as 00, 10, 01, and 11.

The TOPCAT chip takes the clock supplied to its NCLK pin, which is the oscillator frequency divided by two, and internally divides it by two again. The outside world must keep track of the internal clock, so it knows when the video information on pins V1 - V4 is valid.

If the NRESET signal to TOPCAT is pulled high during a certain window of the NCLK signal, the internal clock phase is known. The double synchronizer in the NRES circuit guarantees that NRESET goes high between states 10 and 11 of the clock circuit, since the synchronizer Flip-Flops are clocked by the Q-output of the second (divide-by-four) J-K Flip-Flop.

With the state of the internal TOPCAT clock known, the Video Shift Register (U16) is loaded at the transition from State 01 to State 11. This is what the second pair of J-K Flip-Flops (U17) accomplishes. The first half of the pair delays the divide-by-four signal by one state. The second half has a 25% duty cycle and loads the Video Shift Register at the appropriate state. The following table shows the outputs of various gates in the four states.

State	U33-6	U33-10	U33-6	U17-9	U16 mode
00	0	0	1	0	SHIFT
10	1	0	0	0	SHIFT
01	0	1	0	1	LOAD
11	1	1	1	0	SHIFT

The synchronizer circuit for the NSTC, NSLDS and NSUDS signals (U25B and U18) is triggered on the transition from State 00 to State 10. By a quirk of fate, the D-type Flip-Flop output (U25-8) has the same signal as J-K Flip-Flop output U17-6. This was a design oversight and could be eliminated if the board is turned. U25 and its pullup (R16) can be removed and U17-6 can be connected to U18-9.

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6.1 Low-resolution Video Circuit

The low-resolution circuit is designed to send a composite video signal out to the monitor, with sync signals from 0 - .3V and video from .3 - 1.0V. This circuit was leveraged from the 98204B Composite Video Card.

Transistor Q2 is held at a certain bias level by the diodes and resistors around it. Syncs and video pull various amounts of current out of its base, changing the voltage level at its collector. Since the 98204B card had a half-bright mode, the circuit uses two transistors for the video signals, and one for horizontal and vertical sync. For more detail on this circuit, see the Theory of Operation for the 98204B Card.

6.2 High-resolution Video Circuit

The high-resolution circuit sends a TTL-level video signal out of a BNC connector, and horizontal and vertical sync out of a D-subminiature connector. This circuit was leveraged from the 9837.

The sync signals and 12V that go out on the D-subminiature connector go through a "T-filter" that helps to keep the video signal off of the board if it bleeds onto these lines in the monitor. The protection diodes are to keep bad things from happening if the user accidentally plugs an RS-232 cable onto the sync connector.

The 12V is used in the 98781A monitor to enable its power supply (with a relay) and power an HP-HIL repeater (which in turn can power up to seven HP-HIL devices).

The video signal runs through a drive transistor in the transistor pack, which is kept out of saturation (and thus sped up) with a Shottky diode (CR4) from base to collector.

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RAM Management	Chapter 7

The TOPCAT Chip nicely takes care of all RAM refreshing and RAS/CAS generation, so I didn't have to.

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