64000

HP64000 Logic Development System

Model 64941A Flexible Disc (Floppy) Drive Controller

HEWLETT PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard system product is warranted against defects in materials and workmanship for a period of 90 days from date of installation. During the warranty period, HP will, at its options, either repair or replace products which prove to be defective.

Warranty service of this product will be performed at Buyer's facility at no charge within HP service travel areas. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses. In all other cases, products must be returned to a service facility designated by HP.

For products returned to HP for warranty service, Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTIBILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Product maintenance agreements and other customer assistance agreements are available for *Hewlett-Packard products.*

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

HEWLETT PACKARD

SERVICE MANUAL

MODEL 64941A
FLEXIBLE DISC DRIVE

REPAIR NUMBERS

This manual applies to 64941A Flexible Disc Drive with a repair number prefix of 2301A. For further information on repair numbers refer to "Instruments Covered by This Manual" in Section I.

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LOGIC SYSTEMS DIVISION
COLORADO SPRINGS, COLORADO, U.S.A.

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Manual Part No. 64941-90902

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SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with the power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

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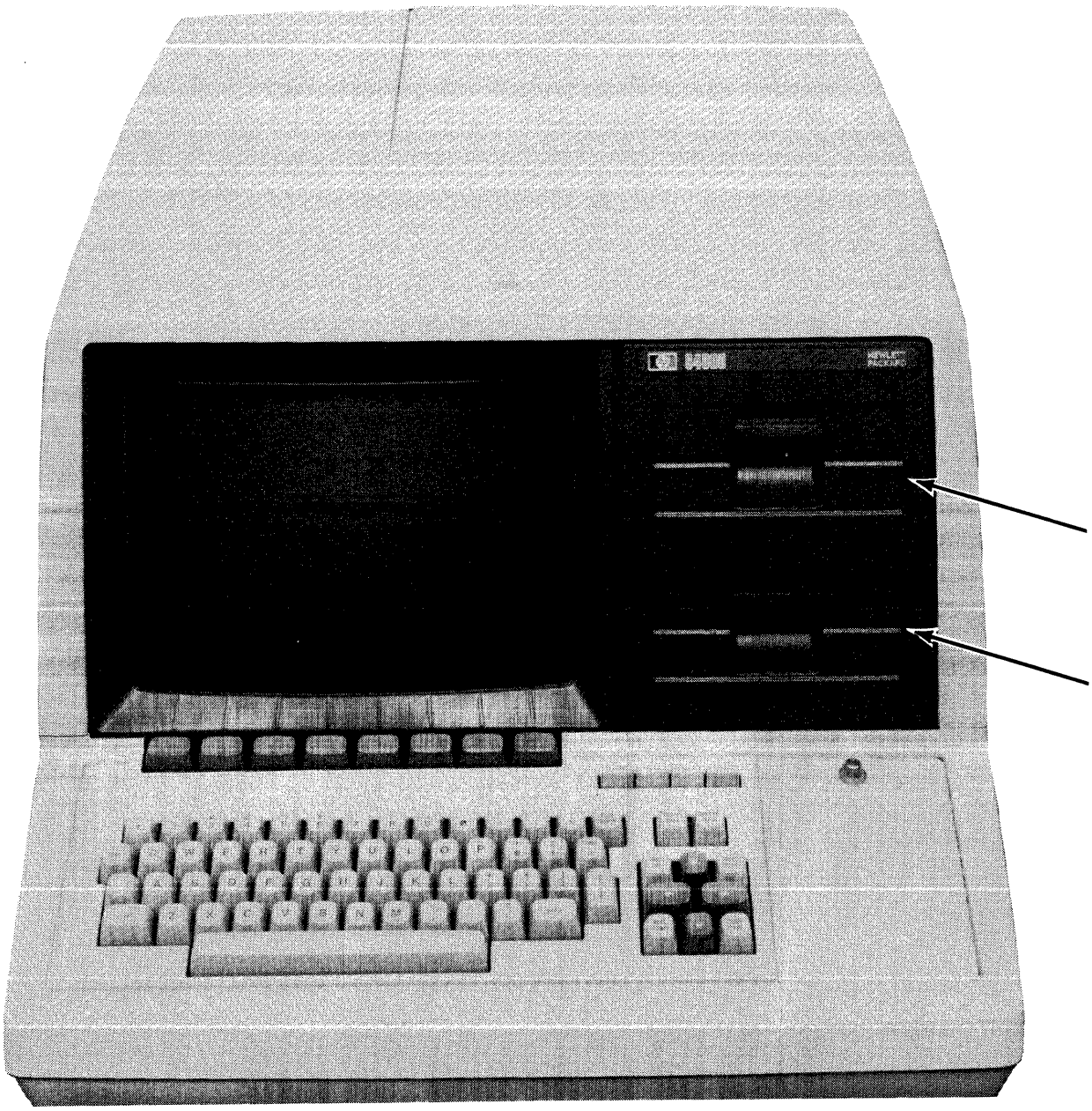


Figure 1-1. 64100A Flexible Disc Drive(s)

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual contains information and theory necessary to operate, install, maintain, and troubleshoot the Floppy Disc Drive option. Operating instructions are provided in a separate operating manual supplied with the instrument. It should be kept with the instrument for use by the operator.

1-3. INSTRUMENTS COVERED BY THIS MANUAL.

1-4. Attached to the instrument or printed on the printed circuit board is the repair number. The repair number is in the form 0000A0000. It is in two parts; the first four digits and the letter are the repair prefix, and the last five are the suffix. The prefix is the same for all identical instruments. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the repair number prefix(es) listed under REPAIR NUMBERS on the title page.

1-5. An instrument manufactured after the printing of this manual may have a repair number prefix that is not listed on the title page. This unlisted repair number prefix indicates that the instrument is different than those described in this manual. The manual for this newer instrument is accompanied by a Manual Changes supplement. This supplement contains "change information" that explains how to adapt the manual for the newer instrument.

1-6. In addition to change information, the supplement contains information for correcting errors in the manual. To keep this manual as current as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page.

1-7. For information concerning a repair number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard Sales/Service Office.

1-8. SAFETY CONSIDERATIONS.

1-9. The Local Mass Storage unit is installed in a 64100A Mainframe (see figure 1-1) and contains voltages in +-12 V AND +5 V range.

1-10. There are high voltages present in the mainframe. Exercise EXTREME CAUTION when removing or installing the Flexible Disc Drive(s). Lethal Voltages exist under the high voltage cover and around the CRT. Review the Mainframe Service Manual for WARNINGs and CAUTIONs before servicing.

1-11. PHYSICAL DESCRIPTION.

1-12. Each Mini Flexible Disc Drive is a semi-random access mass storage system employing a flexible magnetic medium. It consists of a Mini Disc Drive, a Servo Electronics circuit board, a Drive Electronics circuit board, and a Mini Control board.

1-13. Each drive module contains all the mechanical parts necessary for physically handling the disc. These include the drive spindle and motor, 2 heads each having read/write and erase capability, write protect sensor, track 0 sensor, index sensor, and activity LED on the front panel. Each drive module also contains a Servo Control board which controls the DC drive motor speed and a Drive Electronics board which interprets and generates control signals, controls movement of the read/write head to the correct position, and also reads and writes data.

1-14. The flexible magnetic medium used for Local Mass Storage is called a flexible disc. A disc measures 133.4 mm (5.25 inches) on a side and has a 3.8 cm (1.5 inch) hole for alignment on the disc drive spindle. The disc is enclosed in a protective polyvinylchloride (PVC) jacket with a slot for access to the recording surface. Both sides of the flexible disc are used for data storage.

1-15. The recording head in the drive module is positioned by a mechanism driven by a stepper motor and taut metal band. The head positioning mechanism operates in an open loop configuration, that is, there is no feedback to the Drive Electronics board to determine the actual position of the head.

1-16. The heads are mechanically coupled to the door mechanism so that closing of the door (pushing down the latch) causes the heads to make contact with the media.

1-17. ENVIRONMENTAL AND PHYSICAL SPECIFICATIONS.

1-18. OPERATING ENVIRONMENT.

1-19. The Flexible Disc Drive Local Mass Storage unit may be operated in environments within the following limits:

a. Temperature: +10*C to +44*C (50*F to 111.2*F)
b. Relative Humidity: 20% to 80% while at +29.4 C (85 F)
c. Altitude: 0 to 4572 m (0 to 15000 ft)

It should be protected from temperature extremes which cause condensation within the instrument.

1-20. STORAGE ENVIRONMENT.

1-21. The Flexible Disc Drive Local Mass Storage may be stored or shipped in environments within the following limits:

a. Temperature: -41°C to +71°C (-40.5°F to +159.8°F)
b. Relative Humidity: 20% to 80% at +29.4°C (+85°F)
c. Altitude: 0 to 4572 m (0 to 15000 feet)

1-22. RECORDING CHARACTERISTICS.

1-23. HP PHYSICAL TRACK FORMAT.

a. Recording Mode: Modified Frequency Modulated (MFM)
b. Rotational Speed: 300 RPM +-1.5% (+-4.5 RPM)
c. Bit Density: 5456 BPI on Track 34
d. Tracks Per Inch: 48
e. Sides Per Disc: 2
f. Tracks Per Sides: 35
g. Sectors Per Track: 16
h. Bytes Per Sector: 256 (362 including overhead bytes)
i. Bytes Per Disc: 286,720 (formatted) 420,000 (unformatted)

1-24. ALIGNMENT LIMITS.

a. Radial Alignment: 1.1 mils maximum of track center at track 16 measured at 20°C (68°F) and 50% humidity.
b. Azimuth: 18 degrees maximum clockwise/counterclockwise on tracks 16 and 34.

1-25. PHYSICAL DIMENSIONS.

1-26. Figure 1-2 illustrates the physical dimensions of a single flexible disc drive unit.

1-27. POWER REQUIREMENTS.

1-28. Table 1-1 gives the power requirements for a single or double flexible disc drive plus a Mini Control board. The values include the ON transient which is considered to be the most limiting case.

Table 1-1. Power Requirements

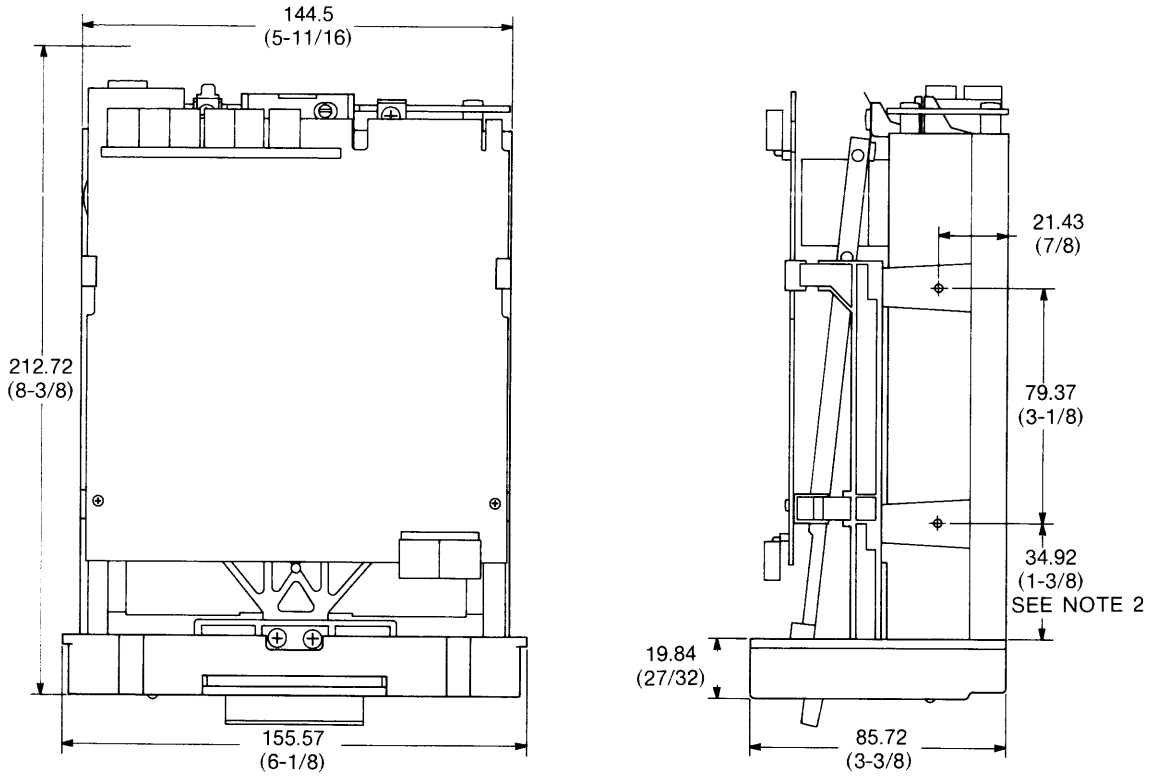
Total (1) Drive	+5V current use =	1.7A - 1.8A	During PV
Total (2) drives	+5V current use =	3.4A - 3.6A	During PV

1-29. MINI DRIVE ASSEMBLIES.

1-30. The flexible disc drives used in the 64000 system are HP9130K drives with the following options.

1-31. OPTION #010. This option consists of drive board P/N 09130-66501. Refer to figure 1-3.

1-32. OPTION #052. This option consists of the mechanical drive assembly with Servo board and front panel P/N 4040-1915 and brown latch P/N 4040-1913 and associated hardware. Refer to figure 1-3. This option also has an exchange assembly number HP P/N 09130-69600.



NOTES:
1. DIMENSIONS GIVEN AS MILLIMETRES (INCHES).
2. THIS DIMENSION FROM BACK OF FACEPLATE.

Figure 1-2. Physical Dimensions

1-33. RECOMMENDED TEST EQUIPMENT.

1-34. Refer to table 1-2 for a list of recommended test equipment.

Table 1-2. Recommended Test Equipment

Product Support Package	
Service Kit	
Alignment tool or small shank screwdriver	
HP 5314A or equivalent frequency counter	
Spindle motor adjustment tool	P/N 8710-1385
Oscilloscope	HP 1740A or equivalent
Alignment Disc	P/N 9164-0151
Torque Driver	P/N 8710-0670
#1 Posidriv Screwdriver	P/N 8710-0899
#2 Posidriv Screwdriver	P/N 8710-0900
3/16 Thin Wall Nutdriver	P/N 8720-0001
5004A or 5005A Signature Analyzer	

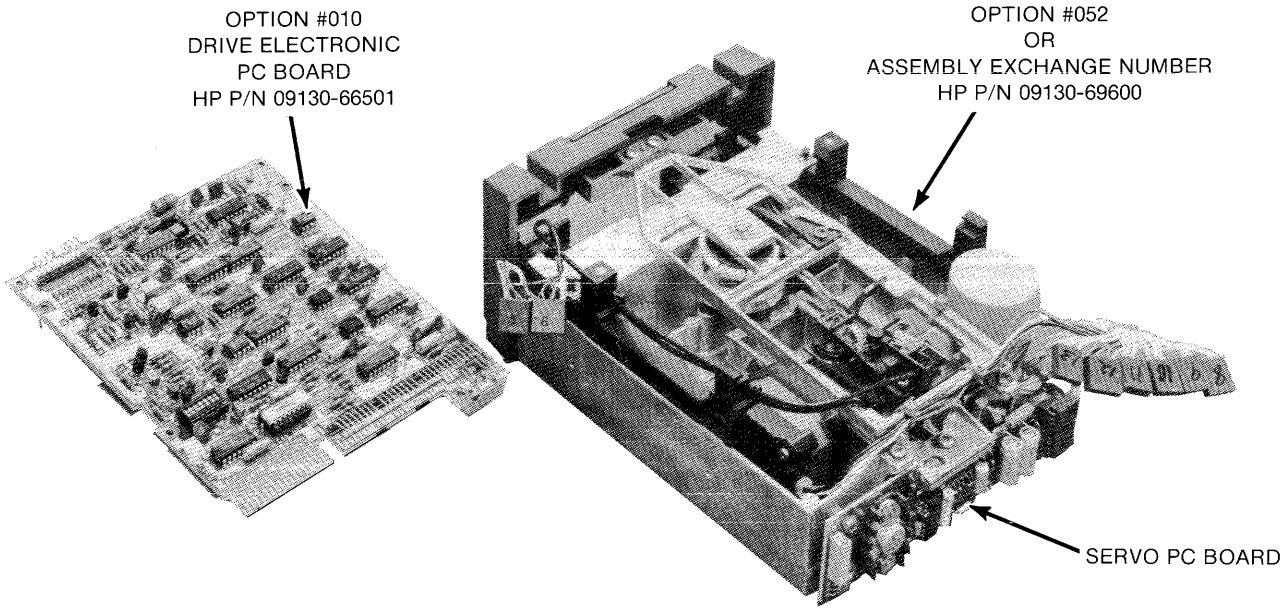


Figure 1-3. Drive Option Breakdown

NOTE

Refer to Section II for jumper configuration when installing a new drive assembly or drive option.

SECTION II

INSTALLATION AND REMOVAL

2-1. INTRODUCTION.

2-2. This section contains information for unpacking, initial inspection, installation and removal of the Local Mass Storage (Mini Flexible Disc Drives and Mini Control board).

2-3. The initial inspection procedure assumes the unit is installed. An installation and removal procedure is included for installing a new unit or removing a defective unit.

a. Unpack the Local Mass Storage unit.

b. Keep the shipping carton and cushioning material until the contents have been checked. The carrier will wish to inspect the shipping materials if a claim is made.

c. Visually inspect the unit for mechanical damage.

d. Install the Mini Drive(s) using the installation procedures in paragraphs 2-4 (Installation of new Mini Drive and Mini Control board Procedure) or paragraph 2-6 (removal and installation for servicing).

e. Run the performance verification tests as specified in this service manual. See section IV for more information.

f. If the contents are not complete, or there is mechanical damage, or defect, or it does not pass the performance verification, then notify the carrier as well as the Hewlett-Packard Field Sales/Service Office. Addresses and numbers are located at the back of this manual. HP will arrange for repair or replacement at HP option without waiting for the claim against the carrier to be settled.

2-4. INSTALLATION OF NEW MINI DRIVE AND MINI CONTROL BOARD PROCEDURE.

2-5. The following procedure should be used when installing a Local Mass Storage unit into a 64100A Mainframe. This procedure assumes that no Local Mass Storage option is installed.

a. Switch power OFF on the mainframe and disconnect the AC power cord.

b. Completely remove the five screws that secure the top cover. Remove the two (or four) Rear-Panel screws holding the state and timing grounding clips. Lift and remove cover.

c. Remove the four display bezel attach screws and washers. See figure 2-1.

d. Pull the display bezel forward.

e. Remove the four screws and washers attaching the blank cover panel. See figure 2-2.

f. Attach the Mini Drive cover panel using the four screws and washers from step (e).

g. Remove the cardboard from inside the drive unit that is protecting the drive heads.

h. Place the Mini Drive cables into and through shield box as shown in figure 2-3.

i. Mount the drive unit(s) into the shield box using the four attach screws provided for each drive.

j. Mount the drive unit onto the display bezel using the four attach screws provided.

k. Plug upper drive 0's keyed power cable P2 into J2 on drive 0 and connect (W1) ribbon control cable P1 onto J1 on drive 0. Make sure that pin one on the plug, indicated by a triangle molded on the connector, is attached to pin one on the jack.

l. Plug lower drive 1's keyed power cable P2 into J2 on drive 1 and connect (W1) ribbon control cable P1 onto J1 on drive 1. Make sure that pin one on the plug, indicated by a triangle molded on the connector, is attached to pin one on the jack.

m. Remove the two plug IOD cable from the CPU and I/O board in the card cage. See figure 2-6.

n. Insert the Mini Control board into slot 0 in the card cage behind the CPU board.

o. Attach the three plug IOD cable so that the I/O, CPU and Mini Control boards are connected on the I/O bus. See figure 2-6.

p. Attach drive 0's control and power cables P1 and P2 into J4 and J2 on the Mini Control board. Make certain that pin one on the plug is attached to pin one on the Mini Control board jack.

q. Attach drive 1's control and power cables P1 and P2 into J3 and J1 on the Mini Control board. Make certain that pin one on the plug is attached to pin one on the Mini Control board jack.

r. Push the display bezel back enough so the drive cables are lose.

s. Pull the two control cables W1 back and fold. Attach them to the clip on the top of the shield box. See figure 2-6. Note: Make sure that the cables are not lying near the CRT.

t. Push the display bezel all the way back and secure it with the four attach screws and washers.

u. Put on the top cover making sure not to pinch the drive power cables and secure it with the five top cover screws. Attach the state and timing ground clips to the Rear-Panel with the two (or four) screws given.

v. Installation complete.

2-6. MINI DRIVE REMOVAL PROCEDURE.

a. Switch power OFF on the mainframe and disconnect the AC power cord.

b. Completely remove the five screws that secure the top cover. Remove the two (or four) Rear-Panel screws holding the state and timing grounding clips. Lift and remove cover.

c. Disconnect both Mini Drive power and ribbon cables from the Mini Control board.

d. Remove the four display bezel attach screws and washers. See figure 2-1.

e. Pull the display bezel forward.

f. Remove the four screws and washers that attach the shield box to the mainframe. See figure 2-4.

g. Remove the shield box from the mainframe. The Mini Drives are located inside the shield box. There are four screws for upper drive 0 and four screws for lower drive 1 which attach the shield box to each of the drives. Remove the applicable screws. Remove the Mini Drive(s) from the shield box. See figure 2-3 thru 2-5.

NOTE

The power and control cables are routed through the back of the shield box. Use CAUTION when removing the Mini Drive(s). Damage may occur to cables if they are not treated carefully when being pulled through the rear of the shield box.

2-7. MINI DRIVE INSTALLATION PROCEDURE.
(After Servicing Drive)

a. Place Mini Drive(s) cables into and through shield box as shown in figure 2-3. Make sure cables are not bent or twisted.

b. Plug upper drive 0's keyed power cable P2 into J2 on drive 0 and connect (W1) ribbon control cable P1 into J1 on drive 0. Make sure that pin 1 on the plug, indicated by a triangle molded on the connector, is attached to pin 1 on the jack.

c. Plug lower drive 1's keyed power cable P2 into J2 on drive 1 and connect (W1) ribbon control cable P1 into J1 on drive 0. Make sure that pin 1 on the plug, indicated by a triangle molded on the connector, is attached to pin 1 on the jack.

d. Attach drive 0's control and power cables P1 into J4 and P2 into J2 on the Mini Drive Control board. Make certain that pin 1 on the plug is attached to pin 1 on the jack.

e. Attach drive 1's control and power cables P1 into J4 and P2 into J2 on the Mini Drive Control board. Make certain that pin 1 on the plug is attached to pin 1 on the jack.

f. Attach the four screws that attach each of the Mini Drives to the shield box.

g. Reattach the shield box to the bezel with four screws and washers. See figure 2-5. Be careful not to drop the screws or washers into the mainframe.

h. Pull up the lock bracket on the left side of display bezel and push bezel back into mainframe. See figure 2-1.

i. Fold ribbon cables as shown in figure 2-6. Make SURE the power cables (P2) are away from the CRT.

j. Reattach the four display bezel attach screws and washers. See figure 2-1.

k. Place the top cover on the mainframe and reattach the five attach screws that secure the top cover. Reattach the state grounding clip(s) with the two (or four) attach screws.

2-8. MINI DRIVE JUMPER CONFIGURATIONS.

2-9. Each disc drive is shipped with a jumper block installed on the Drive Electronics board. The specific configuration of the jumper block installed depends on the board part number and the particular installation. All jumpers are installed except for the HM jumper on the Drive Electronics board.

2-10. The jumper configurations described here are found on the 09130-66501 Drive Electronics board.

2-11. The jumpers on the 09130-66501 Drive Electronics are located in a 16 pin DIP socket designated U1E. For use with the 64000 system, all jumpers should be intact except the HM jumper (U1E pins 8 and 9). The drives are normally shipped this way. The jumpers and their functions are listed in table 2-1.

Table 2-1. Mini Drive Jumpers and Functions

Jumper Name	Installed	U1E Pin Numbers	Function
HS	X	1 and 16	The head load solenoid is activated when the drive is selected if this jumper is left intact.
DS0	YES	2 and 15	When this jumper is intact, the drive responds to drive address 0.
DS1	X	3 and 14	When this jumper is intact, the drive responds to drive address 1.
DS2	X	4 and 13	When this jumper is intact, the drive responds to drive address 2.
DS3	X	5 and 12	When this jumper is intact, the drive responds to drive address 3.
MUX	YES	6 and 11	This jumper should only be used in installations having more than one drive on the controller.
NOT USED	X	7 and 10	This jumper is not used.
HM	NO	8 and 9	This jumper is not installed on the 64000 system. This jumper is not installed because the Motor ON and Drive Select signals are to operate independent of each other.

X = Don't Care

2-12. TERMINATION RESISTOR PACKAGE.

2-13. On the Drive Electronics board P/N 09130-66501, the 16 pin DIP socket U2F is for insertion of the termination resistor package. The resistor package must be installed.

2-14. SOLDERED JUMPERS.

2-15. On the 09130-66501 board, Jumper wires are soldered in R50 and R56. Locations R51 and R57 are left open.

2-16. PACKAGING.

2-17. ORIGINAL PACKAGING.

2-18. Containers and packaging are available through Hewlett-Packard offices.

2-19. OTHER PACKAGING.

2-20. The following general instructions should be used for re-packing with commercially available materials:

a. Wrap the 64941A in heavy paper or plastic.

b. Use a strong shipping container. A double-wall carton made of 350 pound test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 inches) thick around all sides of the 64941A to provide firm cushioning and prevent movement inside the container.

d. Seal the shipping container securely.

e. Mark the shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to the instrument by model number and full serial number.

2-21. FLEXIBLE DISC MEDIA.

2-22. The storage medium used in the Mini Flexible Disc Drive, is a flexible feromagnetic disc. Both sides of the flexible disc are used for data storage. Each disc must be initialized before it can be used for data storage. The initialization procedure marks each disc track, checks for defective tracks, and establishes file directories. Refer to the formating procedure in section III of this manual and the Flexible Disc Drive Reference Manual for specific details.

********** CAUTION **********

Disc drive performance and reliability are dependent on the type of media used. Disc drive specifications can be assured only when using HP media. The use of improper media can result in premature disc failure or damage to the disc drive.

On some disc products HP may qualify other non-HP media. When tested, this media met HP specifications; however, HP does not warrant or support this media and can not control changes in its specifications or quality. The selection and use of such products is to the customer's responsibility. HP RESERVES THE RIGHT TO EXCLUDE FROM WARRANT AND MAINTENANCE AGREEMENT COVERING ANY REPAIRS WHICH HP REASONABLY DETERMINES OR BELIEVES WERE CAUSED BY THE USE OF MEDIA NOT PROVIDED BY HP. HP WILL UPON REQUEST PROVIDE SUCH REPAIRS ON A TIME AND MATERIALS BASIS.

Warranty and maintenance agreement coverage of such repairs not caused by the use of non-HP media is unaffected.

The new statement on the drives will say "Use HP media - Part No. XXXX-XXXX".

2-23. FLEXIBLE DISC DRIVE HEAD CLEANING PROCEDURES.

2-24. The flexible disc drive READ/WRITE HEAD should be cleaned ONLY when a HEAD failure is suspected. Use the HP head cleaning kit, HP Model No. 92193A, to service the READ/WRITE HEAD. Contact the nearest HP Sales/Service Office for ordering information.

2-25. If a head failure is apparent, then clean it with the 92193A head cleaning kit. Follow the steps given below to clean the head.

```
********************************** NOTE ***********************************
*                                                                         *
*                                                                         *
*  The READ/WRITE HEAD should ONLY be cleaned when a HEAD failure is      *
*  suspected. Excessive cleaning of the READ/WRITE HEAD may damage        *
*  flexible disc drive media. The cleaning solution on the HEAD           *
*  CLEANING DISC will destroy the lubricant on the flexible disc media    *
*  if the cleaning disc is excessively used.                              *
*                                                                         *
***************************************************************************
```

2-26. The mainframe must be configured for Performance Verification. To do this, either press CNTR/RESET or turn the mainframe OFF and configure the control source switches on the Rear-Panel to the performance verification mode. Then power ON the mainframe. The display test pattern, figure 4-1 should be on the screen. Then perform the following:

a. The flexible disc media used in the 64941A flexible disc drive is double sided. Configure the head cleaning disc for "double sided" according to the instructions given with the 92193A head cleaning kit. Insert the cleaning disc into the failing drive unit and close latch.

b. Press the DIAG softkey. The display will change to the diagnostic level.

c. Press the DIAG softkey. The display will change to the next lower level.

d. Press the TEST softkey. A list of tests will appear on the screen.

e. Press the ALT_SEEK softkey. This will step the head in and out across the head cleaning disc. Let this step run for approximately 2 minutes.

f. Press ALT_SEEK again to end the test. Then press STOP_TEST to exit into the next display level. Then press END_DIAG....then END_TEST to reset the mainframe.

NOTE: If the control source switches on the Rear-Panel were configured to Performance Verification for the head cleaning procedure, then they must be reconfigured to the previous state to get out of the Performance Verification mode.

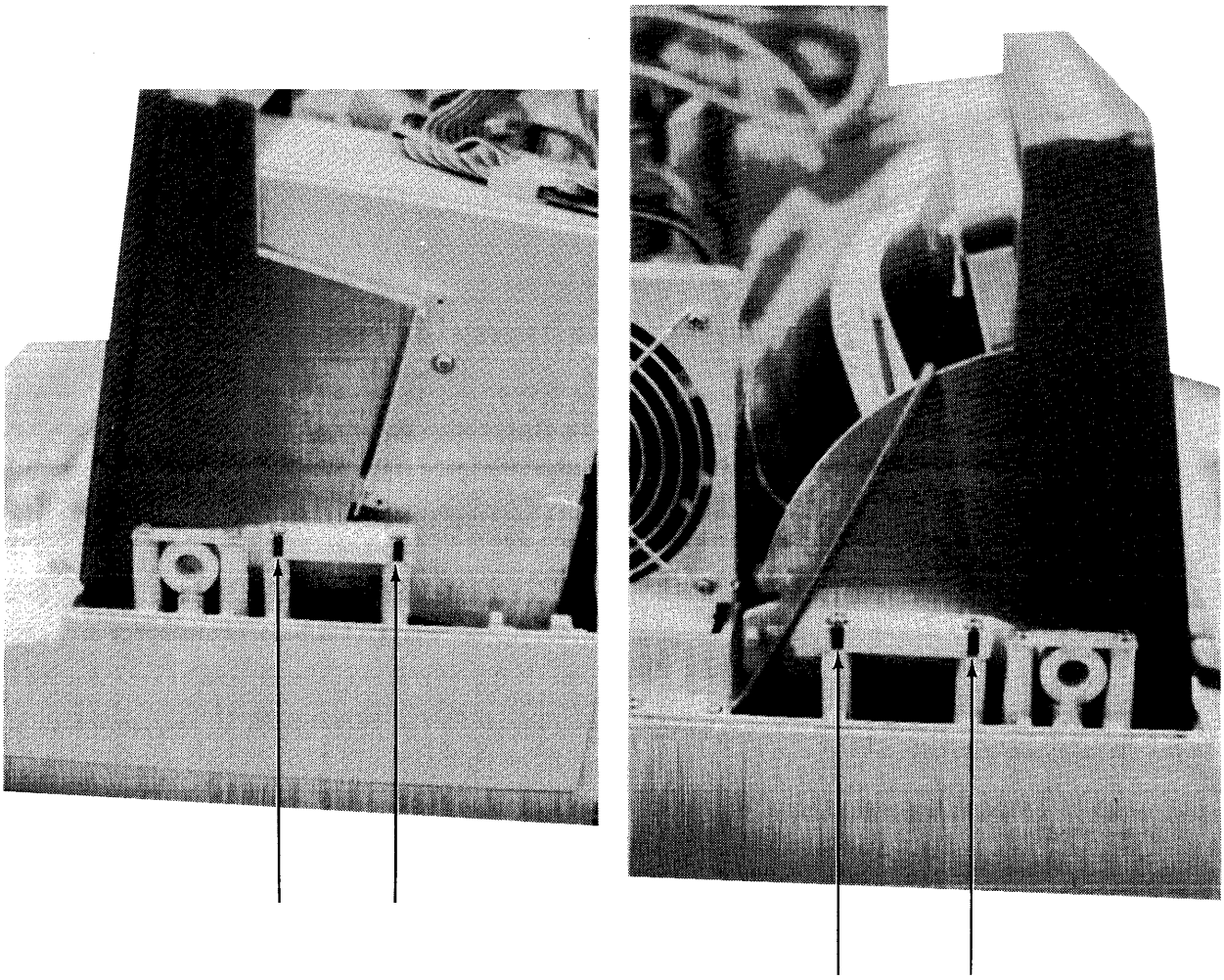


Figure 2-1. Display Panel Attach Screw Locations

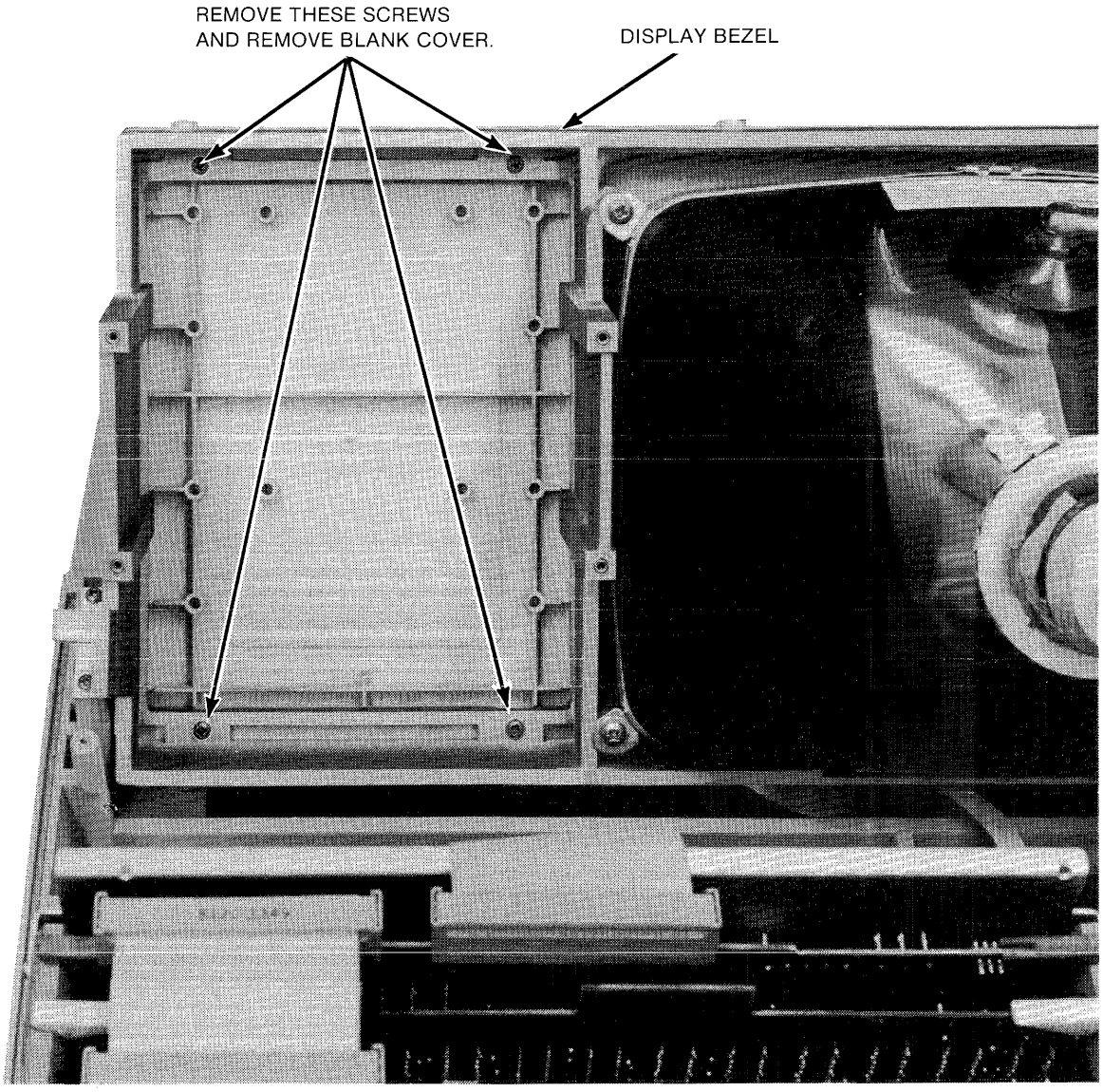


Figure 2-2. Blank Panel Screw Locations

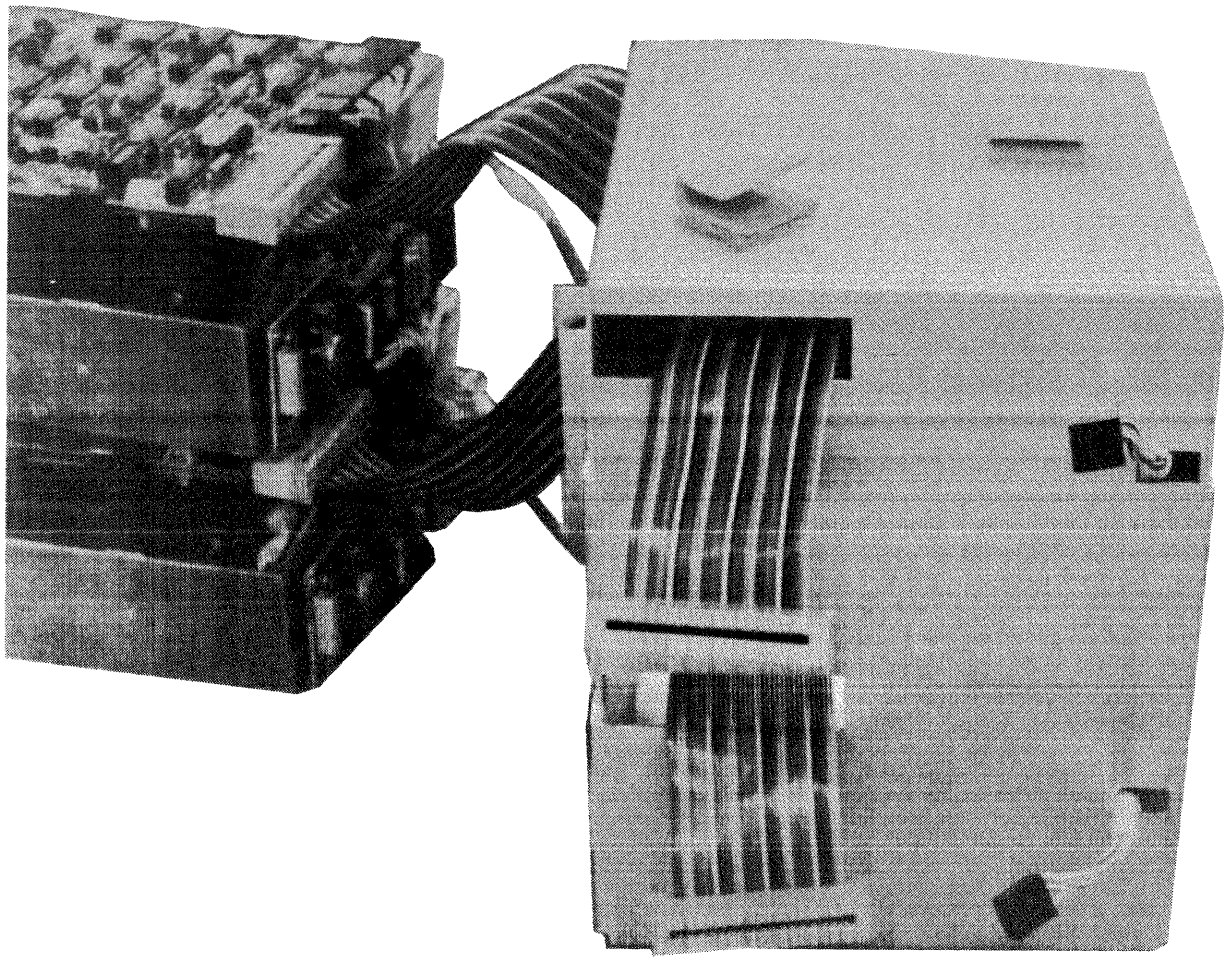


Figure 2-3. Mini Drive Cable Installation

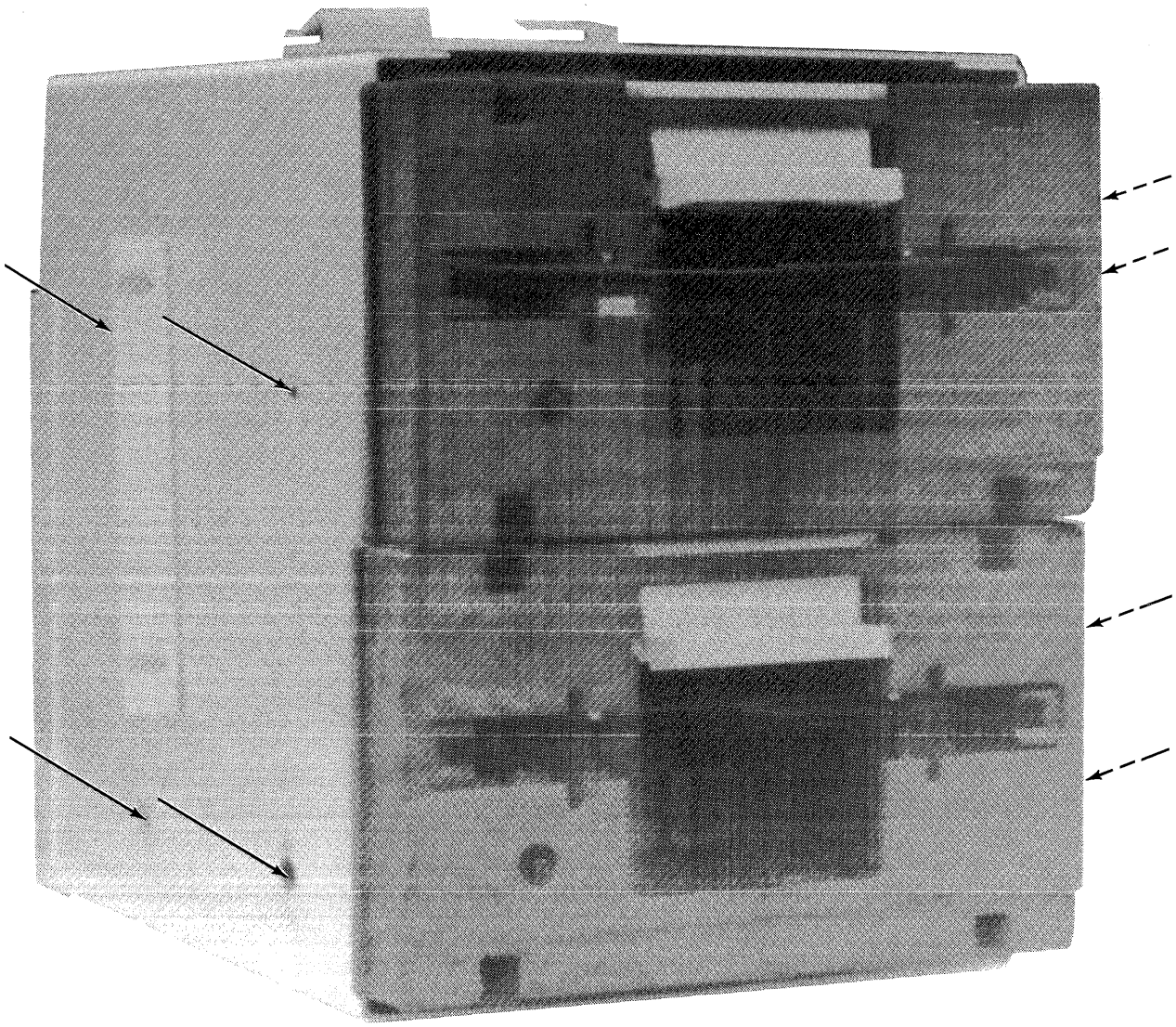


Figure 2-4. Mini Drive Mount Screw Locations on Shield Box

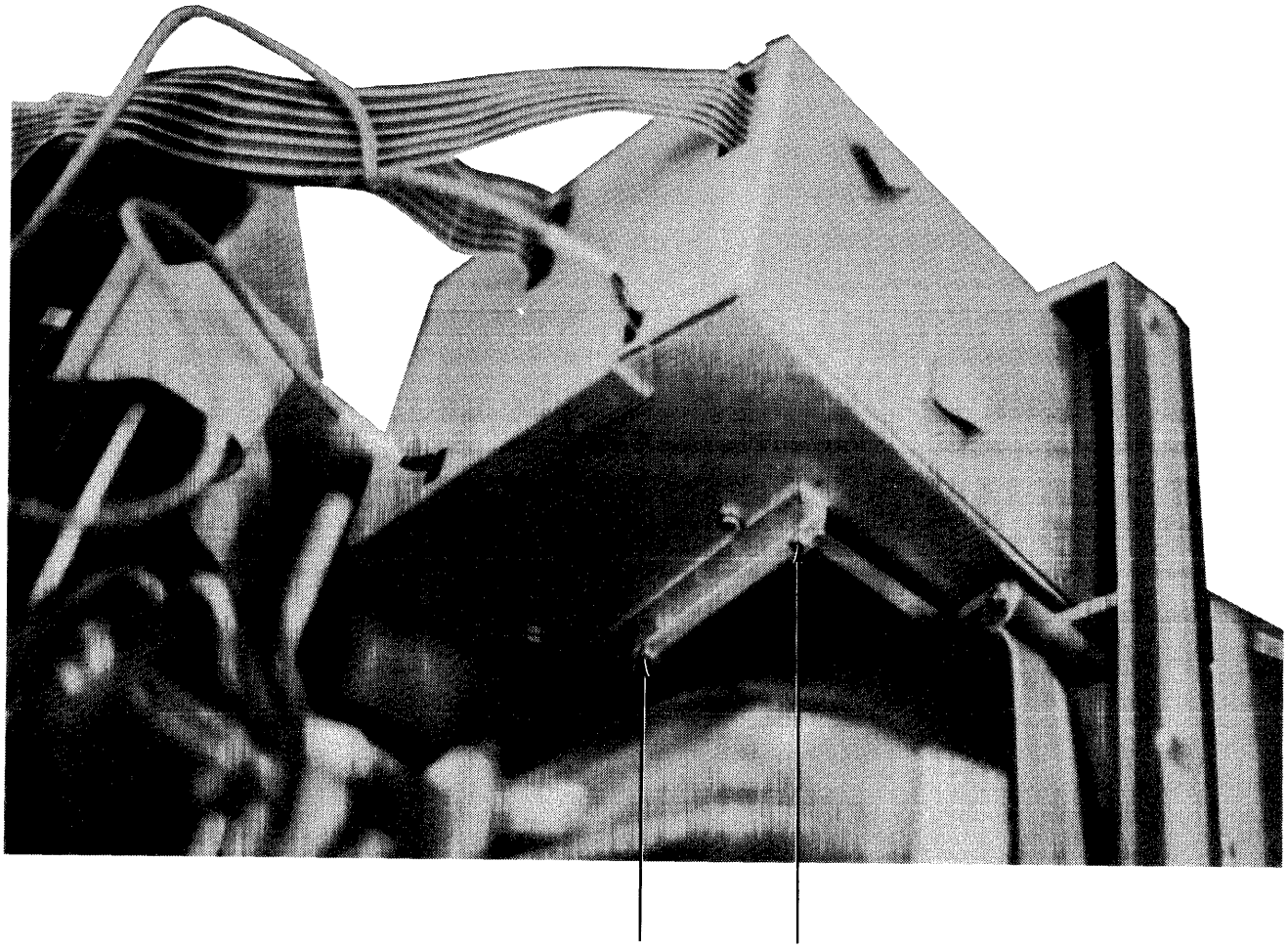


Figure 2-5. Shield Box Screw Locations for Mounting to Display Bezel

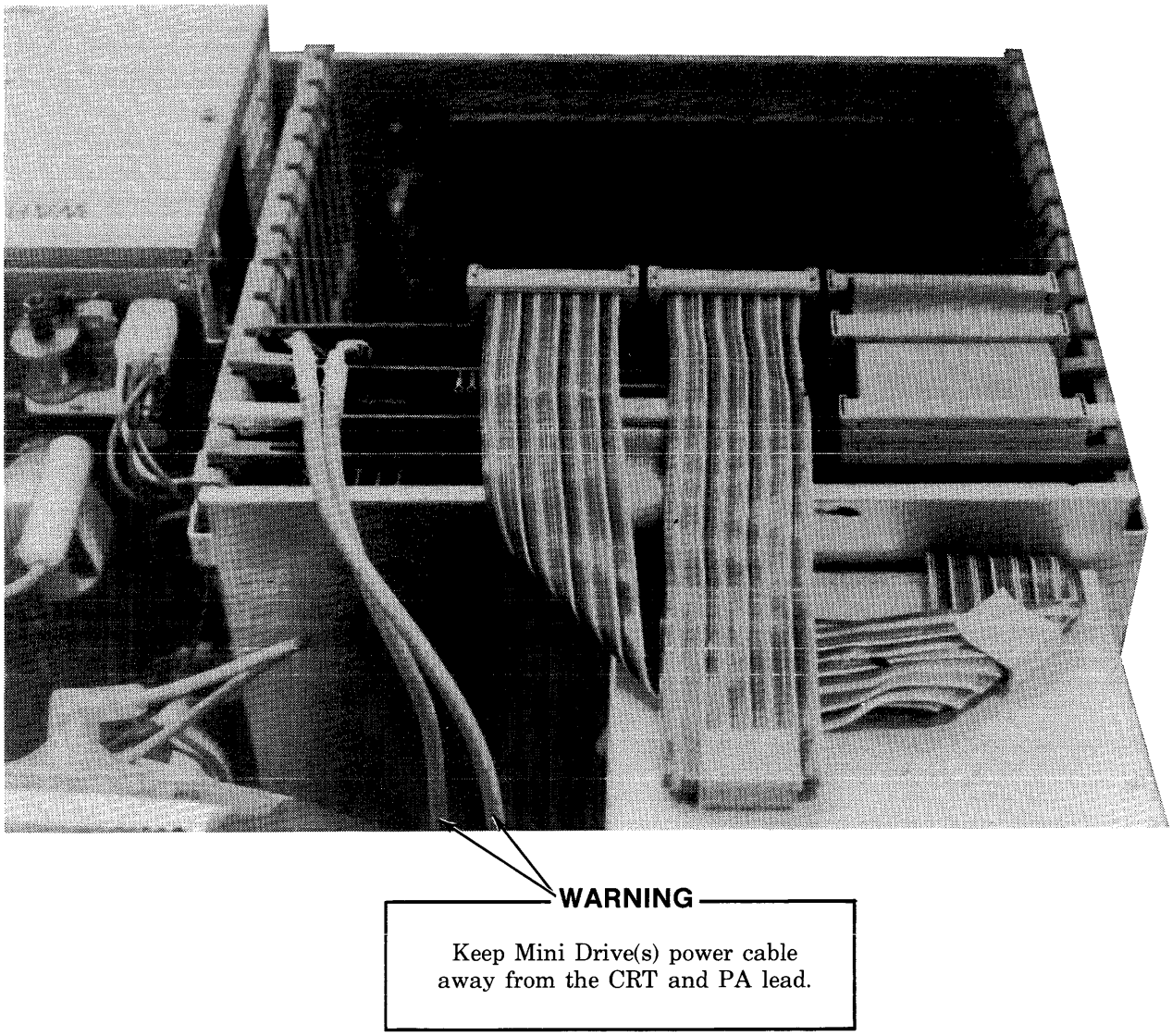


Figure 2-6. Mini Drive Ribbon Cable Position and Fold

SECTION III

OPERATION

3-1. INTRODUCTION.

3-2. Complete operation of the Flexible Disc Drive is beyond the scope of this manual. Please refer to the Flexible Disc Drive Reference Manual for complete operating instructions.

3-3. OPERATING CLEANLINESS.

3-4. To prevent potential damage or data loss, it is extremely important to maintain the cleanliness of the disc and air within the disc drive. The disc drive should not be operated in an environment in which dust, smoke, moisture, oil or chemical vapor or other foreign matter are present. Also, be sure to strictly follow the disc handling guidelines, found in the Flexible Disc Drive Reference Manual.

3-5. DISC LOADING.

3-6. Insert the flexible disc into the drive (be sure that the label faces up and the notch is facing left). Push the disc in until it bottoms out against the rear of the disc drive, then close the door latch. Never force the latch, as the media can be latched off center within the protective jacket.

3-7. WRITE PROTECTION.

3-8. The disc has the capability of being write protected. This feature prevents the accidental erasure of data previously recorded on the disc. The write protect is enabled when the write protect notch on the jacket of the disc is covered (see Figure 3-1). When the notch is uncovered, data can be written on the disc.

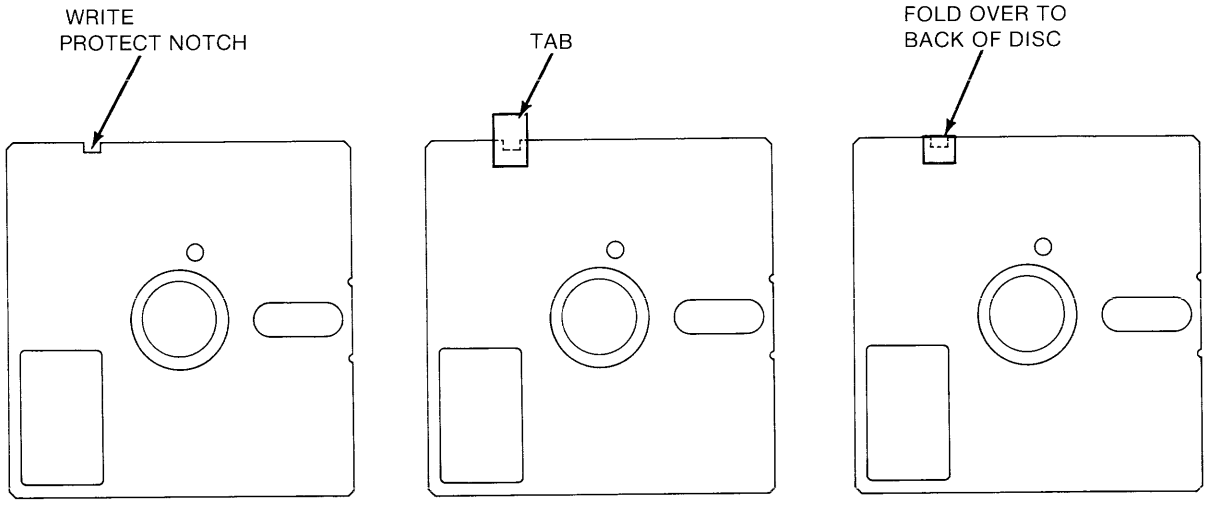


Figure 3-1. Write Protect Tab Installation

3-9. FORMATTING THE DISC.

3-10. Use the following procedure to format a disc:

```
****************** CAUTION ******************
*                                             *
*    Formatting a disc causes all data on     *
*    that disc to be destroyed.               *
*                                             *
***********************************************
```

NOTE: The floppy drives can operate in a "stand alone" or "system" configuration. The "system" configuration must have the "BUS_OP_SYS" software module. In the "stand alone" configuration, the system must have the "FLOPPY_OP_SYS" and "FLOPPY_UTILITIES" modules. Contact the nearest Sales/Service Office for more information.

(Floppy Drives In The System Configuration)

a. Turn ON mainframe. Press the "---ETC---" softkey twice until the "-BACKUP-" softkey appears.

b. Press the "-BACKUP-" softkey. The next level of softkeys will appear.

c. Press the "floppy" softkey.

d. Press the "utilities" softkey and then the carriage return key.

e. Press the "format" softkey.

f. Type in the number of the drive (0 or 1) that the formatting is to is to occur on (0=left drive, 1=right drive).

g. Press return.

3-11. FLOPPY DISC DIAGNOSTIC TEST.

3-12. Follow these steps to get into the Floppy Diagnostic Tests:

a. Either configure the Rear-Panel switches for performance verification and turn the mainframe OFF then ON or press CNTL/RESET to get PERFORMANCE VERIFICATION TEST DISPLAY to appear.

b. Press the DIAG softkey to get FLOPPY DISC DIAGNOSTIC to appear on the screen. Refer to figure 3-2.

c. With the FLOPPY DISC DIAGNOSTIC displayed, press the DIAG softkey to get into the first level of the floppy menu. Refer to figure 3-3.

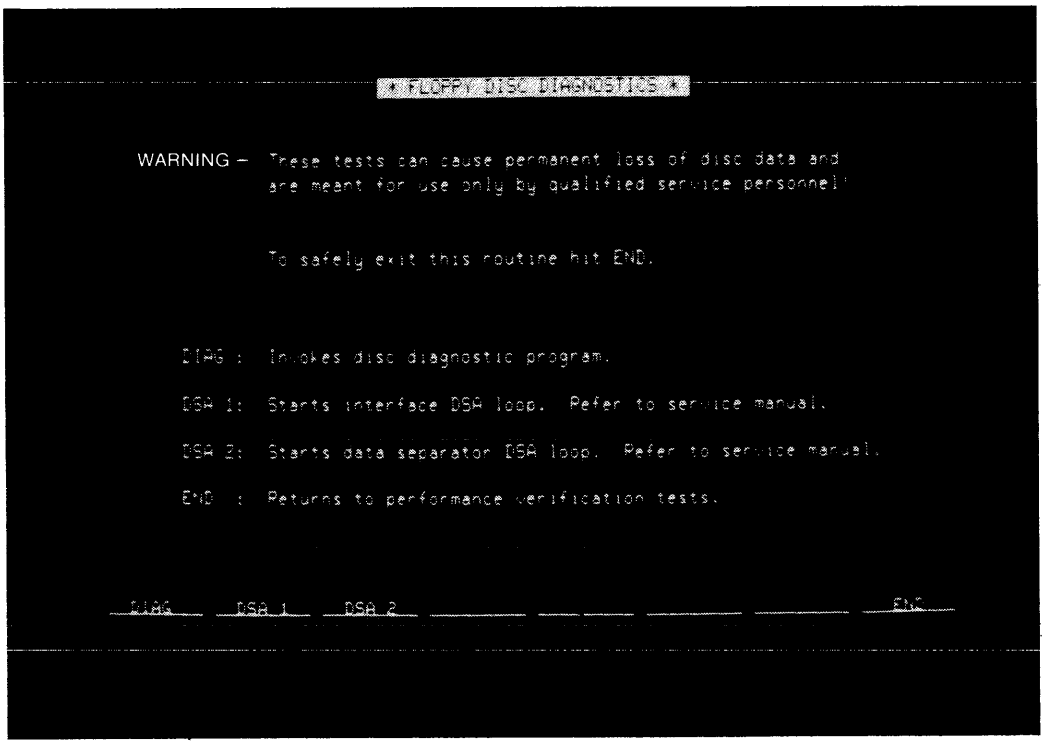


Figure 3-2. Floppy Disc Diagnostic Display

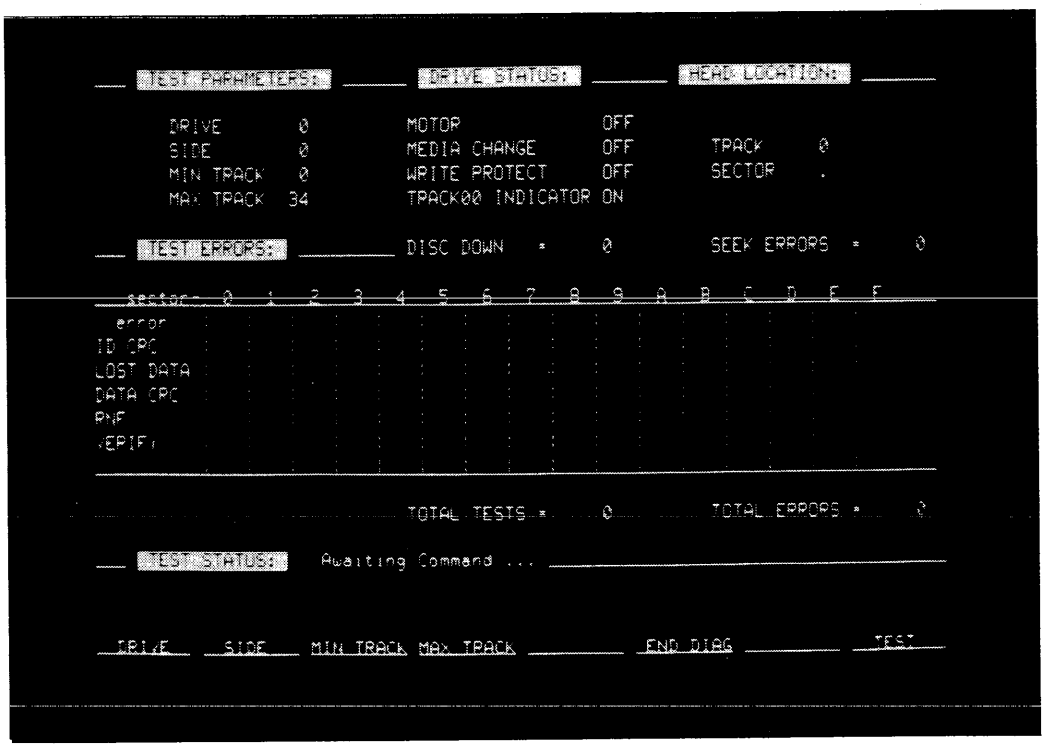


Figure 3-3. Floppy Test Menu First Level

3-13. The floppy disc diagnostic test uses two levels of floppy menu. The first level allows the user to set the Diagnostic test parameters by pressing the four softkeys (see figure 3-3). These are:

DRIVE	0/1	Alternately selects DRIVE 0 or 1 to be tested when the TEST softkey is pressed. The LED will be ON on the DRIVE selected.
SIDE	0/1	Alternately selects SIDE 0 or 1 to be tested when the TEST softkey is pressed.
MIN TRACK	0-34	Sets the minimum track to be used with the ALT SEEK command (between 0 to 34). The MIN TRACK softkey must be pressed first then the track # and then the return key.
MAX TRACK	0-34	Sets the maximum track to be used with the ALT SEEK command (between 0 to 34). The MAX TRACK softkey must be pressed first then the track # and then the return key.

3-14. The DRIVE STATUS will be displayed in the first level also (see figure 3-3). These are:

MOTOR	ON/OFF	Motor will only be ON when in second (TEST) level of diagnostic.
MEDIA CHANGE	ON/OFF	Indicates a write protect switch closure has occurred. Reset by selecting other drive.
WRITE PROTECT	ON/OFF	Indicates the state of the write protect switch (ON=open).
TRACK00 INDICATOR	ON/OFF	Indicates the state of the track00 signal (ON=head over track00).

3-15. After the TEST PARAMETERS have been set up, press the TEST softkey. The floppy second level menu will appear (see figure 3-4). The display will remain the same (motor status will now be ON), only the softkeys will change.

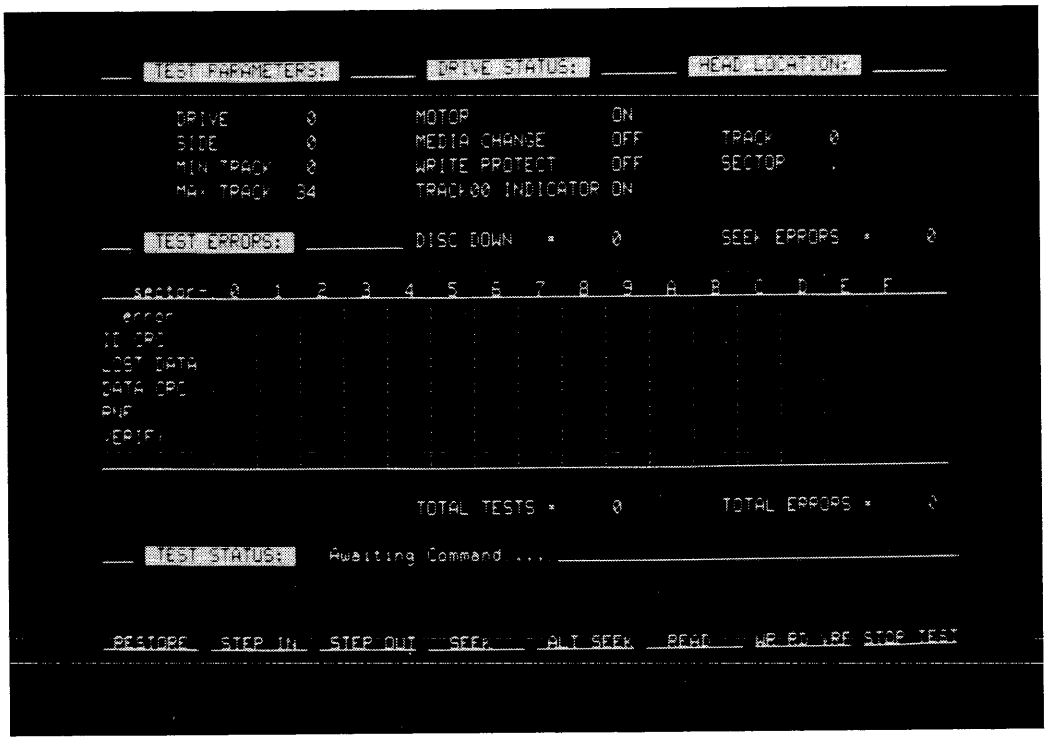


Figure 3-4. Floppy Test Menu Second Level

3-16. There are eight different tests on the softkeys. The functions of each are explained from left to right (the user is facing the terminal).

a. RESTORE - Issues 255 step pulses to step the head toward track 00. The user should check track 00 indicator status to make sure that it is ON.

b. STEP IN - Each time this softkey is pressed the head is stepped in toward track 34.

c. STEP OUT - Each time this softkey is pressed the head is stepped out toward track 00.

d. SEEK - Each time this softkey is pressed it must be followed by the track number to be SEEKED. When the return key is pressed, the head will move to the selected track and read the ID information on that track and compare it to the track being SEEKed. If they do not match, a error message will appear on the command line (Seek Error, Track not Verified). If the ID information is verified then the message, Seek Verified will appear on the command line.

e. ALT SEEK - Causes the head to alternate between MIN TRACK and

MAX TRACK. Each time the head is moved, the CPU reads the ID information on the MIN TRACK or MAX TRACK and compares it to the desired head position. If an error occurs, it will be displayed as a SEEK ERROR. There are four messages given for this test, SEEK ERROR, DISC DOWN, TOTAL ERRORS, TOTAL TESTS (the last three are updated with each test). To exit this test, press the ALT SEEK softkey again.

f. READ - The READ TEST reads each sector of the the track which has been selected by the STEP IN/OUT or SEEK softkeys. Each time a sector is read, the CPU checks the status register in the MDC chip for the follow- errors: ID CRC (Cyclic Redundancy Check), LOST DATA, DATA CRC, RFN (Record Not Found). If an error occurs, the read error field will be updated.

g. RD/WR/VRF - In addition to the tests performed in the read test, the RD/WR/VRF test also writes a random data pattern on each sector of the selected track then reads this information back and verifies that it is the same as the information written. If not the VRF error field will be updated to indicate the type of error and sector of the occurrence.

h. STOP TEST - This softkey allows the user to go from the floppy test menu second level into the first level.

3-17. TEST ERRORS.

ID CRC If the CRC error bit has been set in the status register after the ID field has been read, the number of ID CRC errors in that sector will be incremented.

LOST DATA When this error occurs, it indicates the host system did not respond to LDRQ (Low Data Request) in one byte time (32uS). The number of LOST DATA errors will be displayed in the sector of occurrence.

DATA CRC If the CRC error bit has been set in the data register, the number of occurrences will be displayed in the sector where it took place.

RNF When this error occurs, it indicates that the desired track, sector, or side which was read in the ID field, did not correspond to the track, sector, or side being tested.

VERIFY When this error occurs, it indicates that that data pattern read was not the same as the data pattern written by the host system.

SECTION IV

PERFORMANCE VERIFICATION

4-1. INTRODUCTION.

4-2. This section describes the Performance tests for the Flexible Disc Drive Local Mass Storage. There are two modes of testing, performance verification and operation verification. Refer to the Mainframe Service Manual for more information on initiating performance verification.

4-3. The Performance Verification test will verify to an 85% confidence level that the flexible disc drive(s) are operational.

4-4. The Operation Verification procedures allow the operator to verify all specifications. With the aid of the error code and descriptions in the troubleshooting portion of Section VIII, troubleshoot the mini flexible (floppy) disc drives from the mainframe keyboard.

4-5. PERFORMANCE VERIFICATION TEST PROCEDURE.

4-6. In order to initiate mainframe performance verification (PV) the following methods may be used:

a. Place the control source switches in the performance verification position shown on the control source label on the Rear-Panel.

b. Turn power OFF then back ON. The display test pattern, figure 4-1, should be on screen.

c. Press the PVTESTS softkey.

d. Press the NEXT TEST soft key until the FLOPPY DISC DRIVE test is displayed. See figure 4-2.

e. Press START to initiate the test. Press START again to stop test.

f. If no more tests are required, change control source switches to the desired boot source and press END TESTS and the system will reboot.

OR

g. There is another method that can be initiated from the front panel when a boot is from a hard disc or flexible disc (floppy) if the operating software has been loaded. To do this Press CNTL and RESET together.

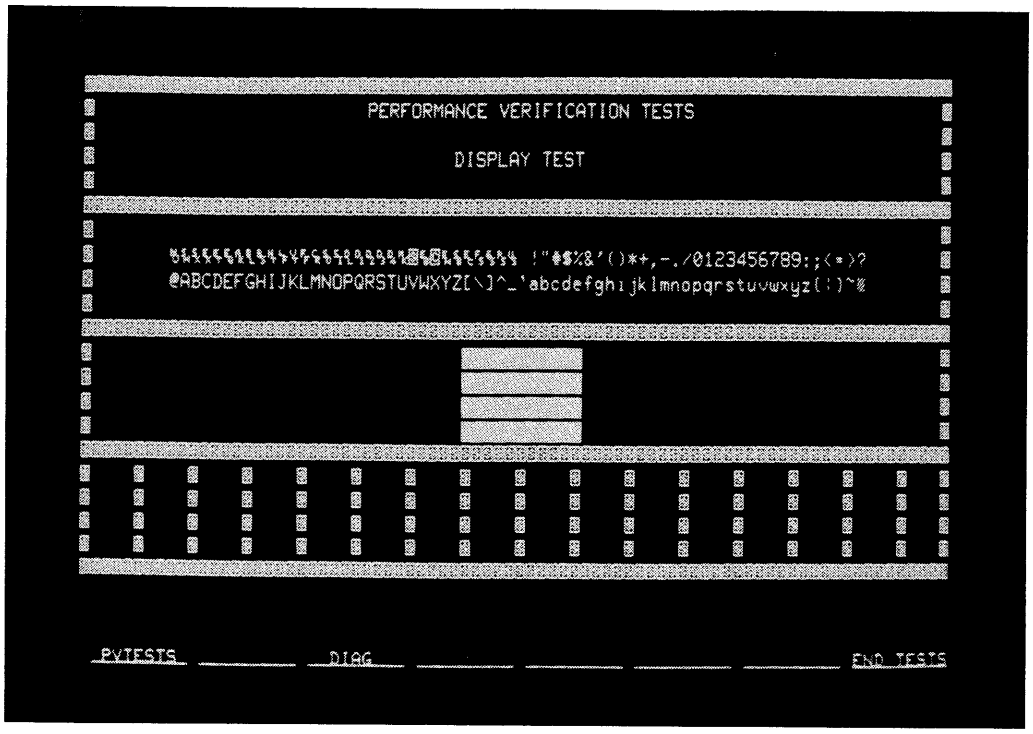


Figure 4-1. Display Test Pattern

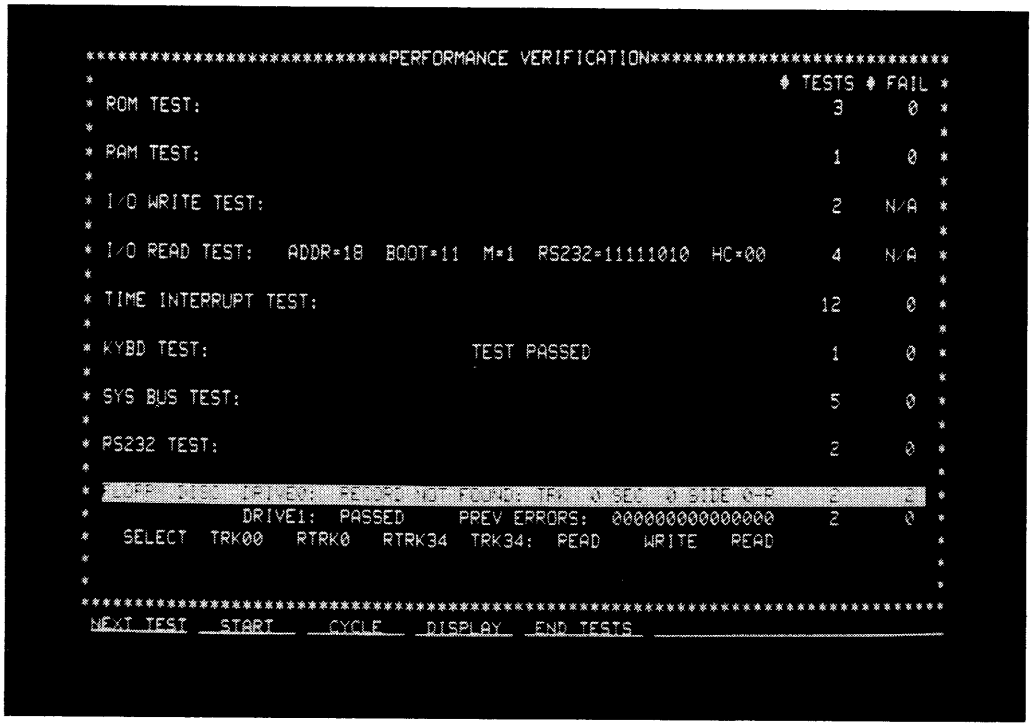


Figure 4-2. PV Test Display

4-7. During the Floppy test the mainframe software will perform eight tests on the flexible disc drives. A description of each test is given in section VIII. The following is the sequence of events that occurs during a test cycle.

NOTE

It is required that a formatted disc be used when performing the floppy PV. Also, the WRITE electronics are not tested if a disc containing data on track 34 is present in the drive being tested. Furthermore, the floppy PV will only verify to an 85% confidence level that the mini drives are operational. In order to completely test the drives, the floppy drive diagnostics (operation verification) must also be done.

Purpose:

The FLOPPY DISC TEST tests several functions of the two floppy disc drives and the controller board electronics.

Area Tested:

CPU and I/O data lines, Disc Drive Controller board electronics, the cable from the Controller board to the drives, Drive READ/WRITE electronics and mechanics, and the CPU, I/O and disc drive I/O data and control line cable.

Operation:

a. Response from the Disc Drive Controller chip is tested by writing a pattern to the track register in the Mini Disc Controller chip (MDC) and reading it back.

b. When initiated, each disc drive is cycled through the following series of tests:

1. The drive is selected.

2. The drive is restored (head moved to track 00).

3. Step inward to track 1 (check TRK00 indicator OFF)

4. Step out to track 00, check track 0 indicator ON.

5. Read all sectors on track 0, side 0; check for all errors.

6. Step to track 34, read all sectors on both sides.

c. The PV routines now check to see if there is any data on track 34. Track 34 will be a spare track on a disc with no bad tracks. However, if there is a bad track on a disc, then track 34 is allocated as useable even though it may contain information.

d. If data exists on track 34, a READ/WRITE test is not performed and a message indicating this is displayed on the CRT. If track 34 is available, the following is performed:

   7. Known data on side 0, sector 0 is READ.

   8. A random data pattern is written to side 0, sector 1.

   9. The pattern is read from side 0 sector 1 and compared with what was written.

   10. Steps 7, 8 and 9 are repeated on track 34, side 1.

4-8. When a test fails an error message is displayed. Refer to table 8-1 (Mini Floppy PV Error Messages) for a quick reference explanation of the error messages, and refer to table 8-2 for a detailed description of each error message and some possible trouble and corrective measures to service a failure.

4-9. When the test passes, a binary error word is displayed which indicates the area of previous failures. This word will contain a one wherever a failure has previously occurred and can be decoded to correspond with the error messages normally displayed. Refer to table 8-1 for an explanation of the error messages.

4-10. OPERATION VERIFICATION TESTS.

4-11. In order to perform the operation verification tests, the following sequence should be used to access the DIAG mode tests:

a. Place the control source switches in the performance verification position shown on the control source label on the Rear-Panel.

b. Turn power OFF then back ON. The display test pattern, figure 4-1, should be on screen.

c. Press the DIAG soft key. Figure 4-3 should be displayed.

d. Press the DIAG soft key again. Figure 4-4 should be displayed.

e. Set up desired tests and press the TEST soft key to initiate. Figure 4-5 should be displayed.

f. When the desired test is finished press the STOP TEST soft key.

g. Press END DIAG to exit the DIAG mode. The display test pattern should be on screen.

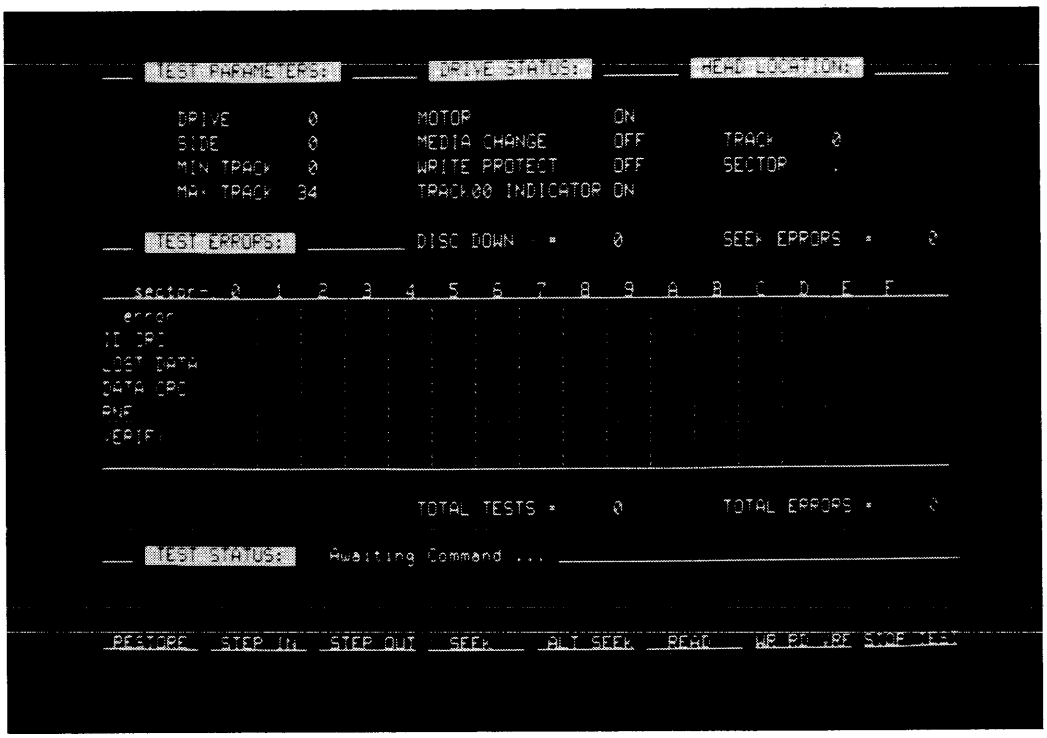


Figure 4-3. Floppy Disc Diagnostic Display

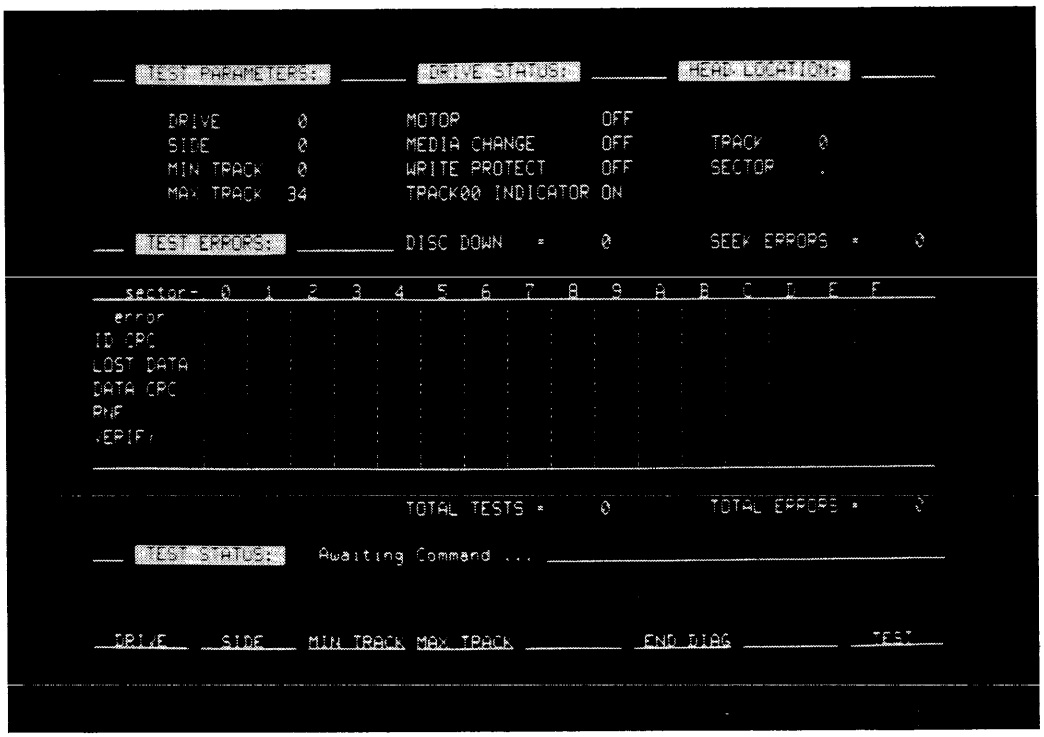


Figure 4-4. Floppy Test Menu First Level

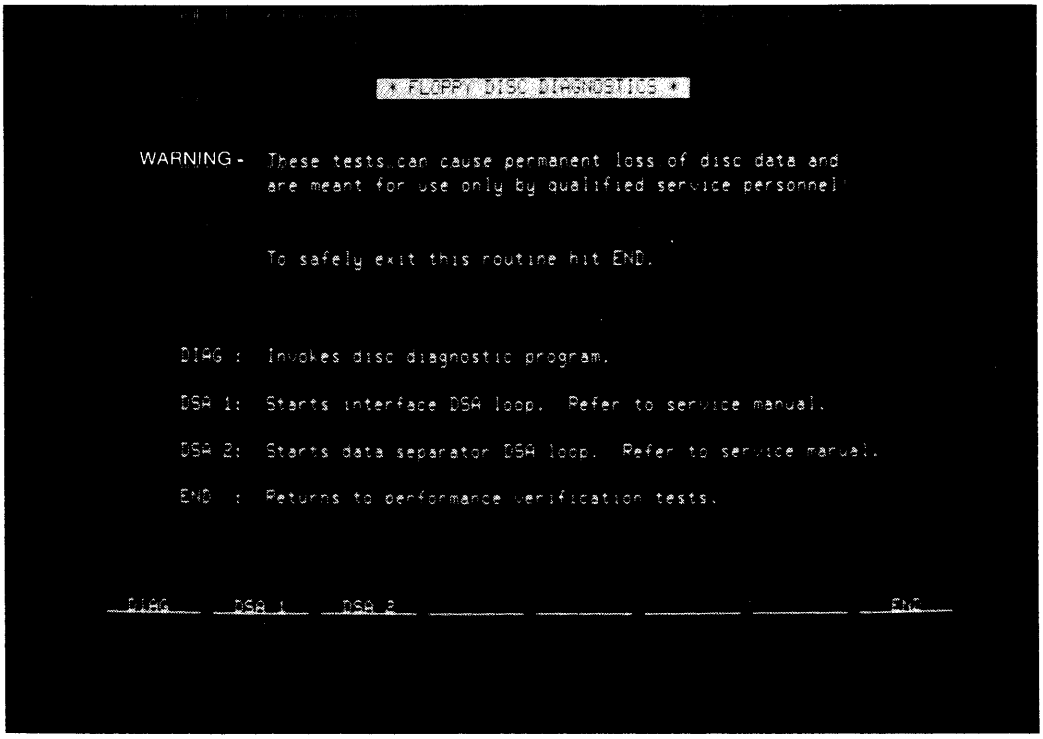


Figure 4-5. Floppy Test Menu Second Level

4-12. Perform all or part of the following tests to verify that the mini drives are operating properly:

NOTE

The Performance Verification procedure should be performed prior to the Operation Verification procedures. When the DIAG mode is required, use the sequence described in paragraph 4-10 to access the DIAG tests.

4-13. MEDIA CHANGE TEST.

a. Go to DIAG mode and make sure media change indication "ON" occurs when media is removed and reset, "OFF" when other drive is selected.

4-14. MOTOR CONTROL TEST.

a. Remove both discs from drives and leave doors open.

b. Go to DIAG mode and observe that drive spindle only turns when motor indication for that drive is in the "TEST" mode.

4-15. DRIVE READY TEST.

a. When running the Operation Verification "READ" test, open the door of each drive and observe "...Disc Down..." failure for the drive being tested.

4-16. DRIVE SELECT TEST.

a. Go to DIAG mode and observe drive select LEDs to make sure that the corresponding LED is only ON when drive is selected.

4-17. FORMAT A DISC.
(check for index pulses at the MDC)

a. Refer to disc format procedure given in Section III of this manual.

4-18. HEAD ALIGNMENT TEST.

```
********************* CAUTION *********************
*                                                 *
*  All previous tests should have passed before   *
*  executing this test to prevent possible        *
*  damage to the alignment disc.                  *
*                                                 *
***************************************************
```

4-19. This test requires performing Steps (a) through (i) of the Radial Head Alignment procedure and then the Head Azimuth Alignment Check. The Radial Head Alignment procedure is found in Section V.

NOTE

The Radial Head Alignment is a difficult procedure!
(Steps (a) through (i) are a check only.)

4-20. HEAD AZIMUTH ALIGNMENT CHECK.

4-21. The head azimuth is not field adjustable due to its very delicate nature. For this reason, the nearest HP Sales/Service Office should be contacted to have this adjustment done. To determine whether the head azimuth is out of limits, perform the following procedures:

a. Use the procedure in section V to setup Mini Drive as shown in figure 5-1.

b. Call up the DIAG test on the mainframe.

c. Insert the alignment disc P/N 9164-0151 into drive and close the latch. the latch.

d. Select side and drive to be checked.

e. Step to Track 16.

f. Connect and setup the scope as follows:

Trigger	Ch. A (pos)
Display	Ch. B
Sensitivity	Ch. A 1V/Div
	Ch. B .1V/Div
Time/Div	.5msec/Div
Coupling	Ch. A DC
	Ch. B AC

Connections (Drive Electronics Board)

	Channel A	Channel B
Signal	TP7(INDEX)	TP4(READ DATA)
Gnd	TP6 (GND)	TP10 (GND)

g. Observe the waveform at TP4 should look similar to that of Figure 4-6. Examine the waveform for heads 1 and 2. If lobe A is greater in amplitude than lobe B or if lobe D is greater in amplitude than lobe C, then the head azimuth is out of alignment.

h. Check both heads by selecting one side, perform the check then select the other side. The side selection is made during test set-up from the mainframe.

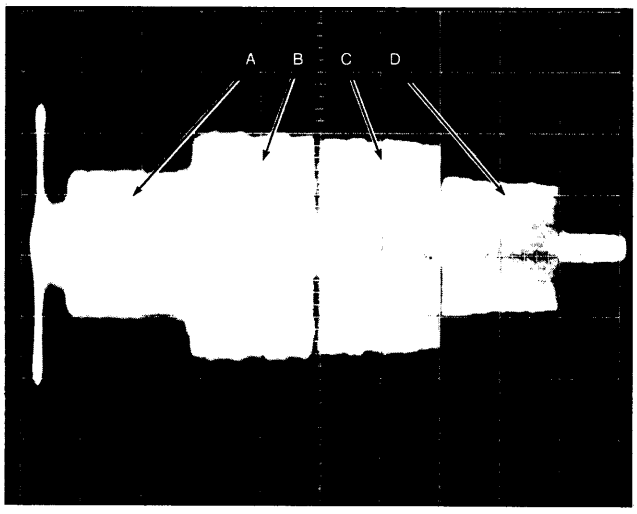


Figure 4-6. Head Azimuth Waveform

SECTION V

ADJUSTMENTS

5-1. INTRODUCTION.

5-2. This section provides the adjustment procedures for the mini flexible disc drive. These procedures are recommended to return the drive to its original optimum performance after maintenance or repair. Included at the beginning of each procedure is a list of required tools. Table 1-2 in section I is a list of all the required tools. All these procedures assume the access to the service equipment listed in table 1-2 of this manual is available.

5-3. There are two catagories of adjustments given in this section. The first two procedures are the spindle motor speed and spindle motor drive adjustments. These first two adjustments may be performed in the field. The second set of adjustments are; Radial head alignment, track 0 switch adjustment, index emitter/detector adjustment, and the write protect switch adjustment. These adjustments should not be performed except in emergency situations due to their delicate nature. These adjustments are NEVER to be performed at the customers location. If a non-field adjustment needs to be done, contact the nearest HP Sales/Service Office. Locations and addresses are given at the back of this manual.

5-4. TEST AND ADJUSTMENT DRIVE ACCESS PROCEDURE.

5-5. The following procedure is a general set up procedure which allows access to the flexible disc drive for testing and adjustments:

a. Remove flexible disc drive from mainframe by reversing the installation procedure (paragraph 2-4 in section II) and place it along side the mainframe.

b. Supply power and control to the flexible disc drive by connecting the power and control extender cables between the control board and the drive unit. Make SURE that pin one on the control board is connected to pin one on the drive under test. The part number for the mini power extender cable is HP P/N 64110-61620, and the part number for the mini control extender cable is HP P/N 8120-4020.

5-6. FIELD ADJUSTMENTS.

5-7. SPINDLE MOTOR SPEED ADJUSTMENT.

5-8. The spindle motor speed should be re-adjusted whenever a new spindle motor or Servo Electronics board is installed. Refer to figure 5-1 while making this adjustment.

a. Required Tools:

1. Alignment tool or small insulated shank screwdriver.

2. HP 5314A or equivalent frequency counter (if primary power frequency is unknown or unstable or when adjusting motor speed under incandescent lighting).

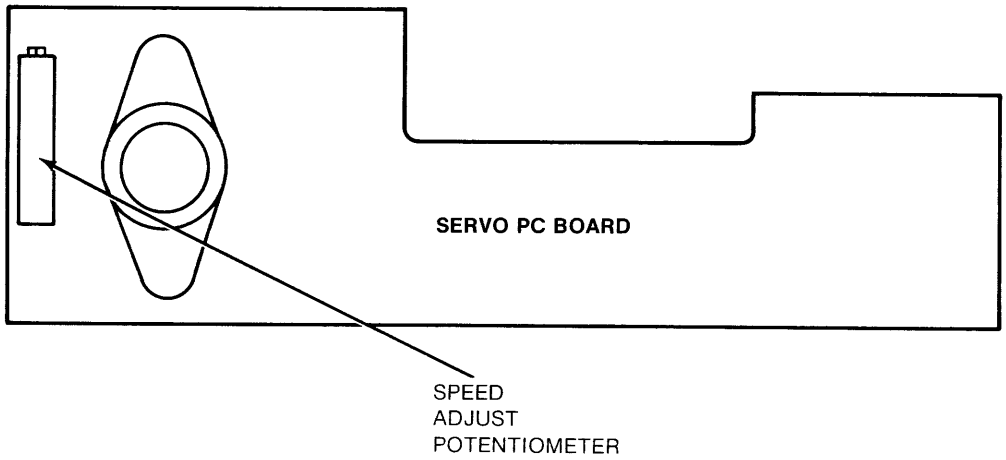


Figure 5-1. Spindle Motor Speed Adjustment

5-9. KNOWN PRIMARY POWER AND FLUORESCENT LIGHTING.

5-10. Follow these instructions when primary power is a known 50 or 60 Hz and this adjustment is done under fluorescent lighting.

a. Check the spindle pulley to see that it has a strobe label P/N 7121-1451.

b. Enter the DIAG Test on the mainframe. Refer to section IV, operation verification tests.

c. Select the drive to be adjusted.

d. Press TEST and note the motor status light is ON indicating the drive motor is running.

e. Observe the strobe pattern on the spindle pulley. For 50Hz primary power observe inner pattern. For 60Hz, observe the outer pattern.

f. Locate and adjust the potentiometer on the servo board until the proper pattern on the strobe label stabilizes. Refer to figure 51.

5-11. PRIMARY POWER FREQUENCY IS UNSTABLE OR UNKNOWN.

5-12. If the primary power frequency is unstable or unknown, follow these instructions:

a. Connect the frequency counter input to TP7 (index) and TP6 (ground) on the Drive Electronics board.

b. Enter the DIAG Test on the mainframe. Refer to section IV operation verification tests.

c. Select the drive to be adjusted.

d. Press TEST and note the motor status light is ON indicating the drive motor is running.

e. Locate and adjust the potentiometer on the servo board until a 200ms +/-1% period is observed on the counter display. This will assure a 300 RPM spindle speed. Refer to figure 5-1.

5-13. SPINDLE DRIVE BELT ADJUSTMENT.

5-14. This adjustment is to ensure proper drive belt tension. This adjustment should be made whenever the drive belt or drive spindle motor is replaced.

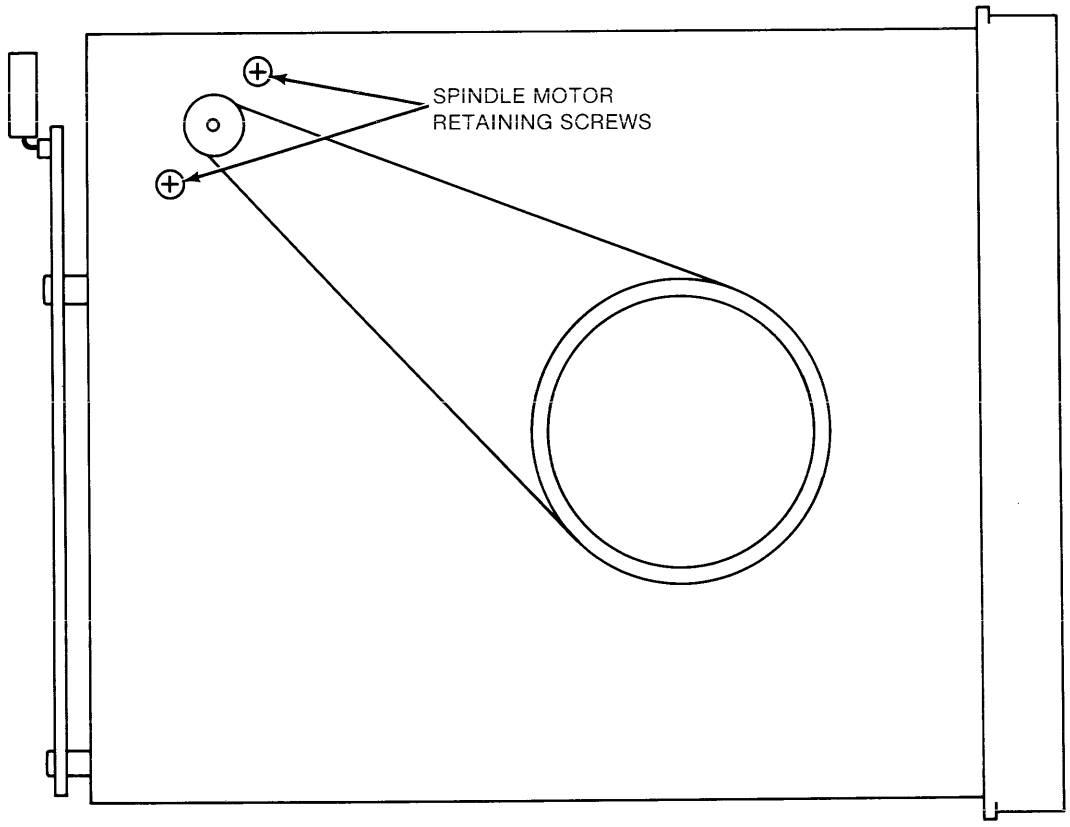


Figure 5-2. Spindle Drive Belt Adjustment

a. Required Tools:

1. #1 Pozidriv screwdriver or equivalent

2. Spindle motor adjustment tool P/N 8710-1385

b. Refer to Figure 5-2 while performing these steps:

c. Place the drive assembly on its side so that the bottom of the drive faces you.

d. Remove the drive belt.

e. Place the spindle motor adjustment tool on the bottom of the drive as shown in Figure 5-1 so that the small end of the adjustment tool rests against the motor pulley and the large end rests against the spindle pulley.

f. Slightly loosen the spindle motor retaining screws and move the motor until it rests firmly against the adjustment tool.

g. Re-tighten the spindle motor retaining screws and reinstall the drive belt.

NOTE

There is a good chance that the drive motor is not exactly perpendicular to the drive casting on which it is mounted. This will cause the drive belt to slip from the drive pulley when it is rotated. After a belt is installed, rotate the drive spindle approximately 10 revolutions to insure the belt will not slip from the drive pulley.

5-15. FACTORY ADJUSTMENTS.

5-16. The following adjustments should not be performed except in emergency situations due to their delicate nature. These adjustments are NEVER to be performed at the customers location.

5-17. The adjustments described in this section are:

a. Radial Head Alignment
b. Track 0 Switch Adjustment
c. Index Emitter/Detector Adjustment
d. Write Protect Switch Adjustment

5-18. REQUIRED TOOLS AND TEST EQUIPMENT.

a. Oscilloscope.....HP 1740A or equivalent
b. Alignment Disc.....P/N 9164-0151
c. Torque Driver.....P/N 8710-0670
d. #1 Pozidriv Screwdriver or equivalent.....P/N 8710-0899
e. #2 Pozidriv Screwdriver or equivalent.....P/N 8710-0900
f. 3/16 Thin Wall Nutdriver or equivalent.....P/N 8720-0001

5-19. RADIAL HEAD ALIGNMENT.

NOTE

Steps (a) through (i) serve as a radial head alignment check.

NOTE

If radial alignment steps (j) through (l) are performed, track 0 adjustment will be required. The track 0 adjustment is an extremely difficult adjustment.

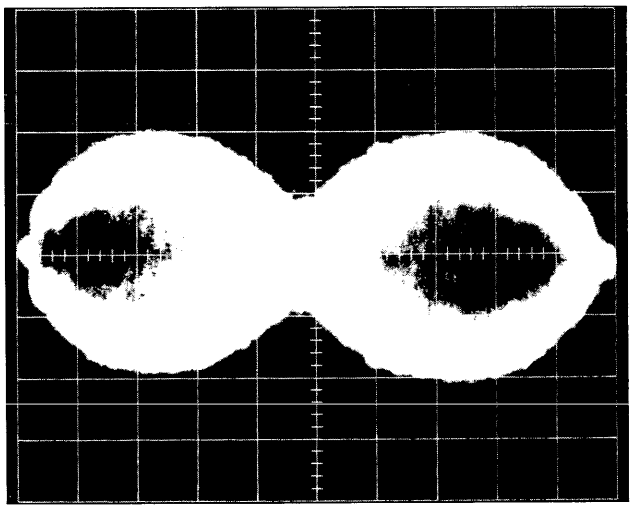


Figure 5-3. Radial Head Alignment Waveform

5-20. To properly align the read/write heads, perform to the following steps in the order shown. Refer to table 8-2, section VIII for head misalignment symptoms.

a. Connect equipment as in procedure in paragraph 5-5.

b. Enter the DIAG test on the mainframe. Refer to section IV operation verification tests.

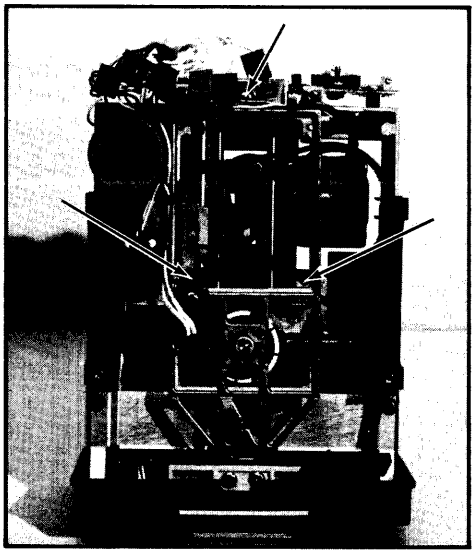


Figure 5-4. Head Assembly Retaining Screws

c. Insert the Alignment disc P/N 9164-0151 into the drive and close the latch.

d. Select the drive and side to be tested and press the TEST softkey.

e. Press the RESTORE softkey.

f. Step to track 16

g. Connect and setup the scope as follows:

Trigger	Ch. A (Pos)
Display	Ch. B
Sensitivity	Ch. A 1V/Div
	Ch. B .1V/Div
Time/Div	20msec
Coupling	Ch. A DC
	Ch. B AC

Connections (Drive Electronics Board)

	Channel A	Channel B
Signal	TP7 (INDEX)	TP4 (READ DATA)
Gnd	TP6 (GND)	TP10 (GND)

h. With the scope connected, the pattern shown in Figure 5-3 should be observed.

i. Both lobes of the pattern should be within 80% in amplitude of each other. If doing a check repeat steps (a) through (i) with the other side of disc selected.

j. If the amplitude of one of the lobes of the waveform is less than 80% (.8 mils) of the other, slightly loosen the three screws shown in figure 5-4 and adjust the radial head alignment by gently turning the head alignment cam screw.

k. After the radial alignment has been completed, retighten the three screws loosened in step (j) while observing the scope pattern. Tighten the retaining screws with the torque-driver set at 8 inch-pounds.

l. Check the other side by selecting the other side in the DIAG test set-up.

5-21. TRACK 0 SWITCH ADJUSTMENT.
(extremely difficult adjustment)

5-22. Track 0 switch adjustment should be performed whenever the radial head alignment is changed. To properly adjust the track 0 switch, follow these steps in the order shown:

a. Connect the equipment as in the procedure in paragraph 5-5.

b. Insert a formatted disc into the drive.

c. Go to DIAG mode (refer to section IV operation verification tests) and set MIN TRACK to 0 and MAX TRACK to 4.

d. Press TEST then RESTORE and then ALT SEEK.

e. Connect and setup the scope as follows:

Trigger	Internal on Ch. A (POS)
Display	Ch. B
Sensitivity	Ch. A 1V/Div
	Ch. B 2V/Div
Time/Div	5mS/Div
Coupling	Ch. A DC
	Ch. B AC

Connections (Drive Electronics Board)

	Channel A	Channel B
Signal	TP12 (STEP)	U4F pin 1
Gnd	TP10 (GND)	TP6 (GND)

f. With the scope connected and setup, the waveform should be similar to that of figure 5-5. The duration from T0 to T1 must be less than 18mS and the duration from T0 to T2 must be less than 24mS. If these times are within the limits, no adjustment is necessary. If either of the time limits is exceeded, proceed with steps (g) thru (l).

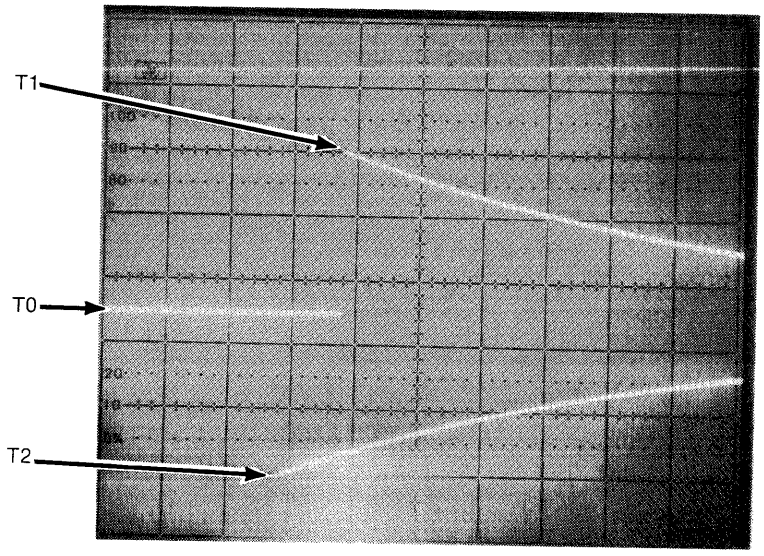


Figure 5-5. Track 0 Waveform

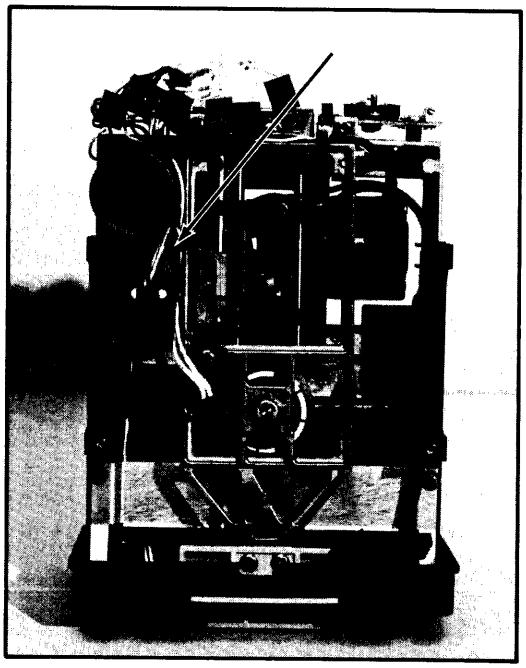


Figure 5-6. Track 0 Retaining Screw

g. Remove connectors P5 and P6 from the front of the drive board.

h. Rest the drive board on a piece of insulating material such as cardboard.

i. Slightly loosen the track 0 switch retaining screw shown in figure 5-6.

j. Adjust the switch position until the time requirements in step (f) are met.

k. With the torque driver adjusted to 8 inch-pounds, retighten the track 0 switch retaining screw while observing the oscilloscope pattern (refer to Figure 5-5).

l. Reinstall the drive board and connectors P5 and P6. Tighten the board retaining screws with the torque driver set to 8 inch pounds.

5-23. INDEX EMITTER/DETECTOR ADJUSTMENT.

5-24. This adjustment is required when the index emitter/detector assembly has been replaced. Perform this adjustment as follows: steps:

a. Connect the equipment as in the procedure in paragraph 5-5.

b. Place drive on its side with bottom facing you as in figure 5-7.

c. Go to DIAG mode. See section IV operation verification tests.

d. Insert alignment disc into the disc and close the latch.

e. Select drive to be tested and press TEST soft key.

f. Press RESTORE, step to track 16, side 0.

g. Connect and setup the oscilloscope as follows:

Trigger	Ch. A (Pos) Internal
Display	Ch. B
Sensitivity	.02V/DIV (using 10:1 probe)
Time/DIV	.1ms/DIV

Connections (Drive Electronics Board)

	Channel A	Channel B
Signal	TP7 (INDEX)	TP1 (READ DATA)
Gnd	TP6 (GND)	TP10 (GND)

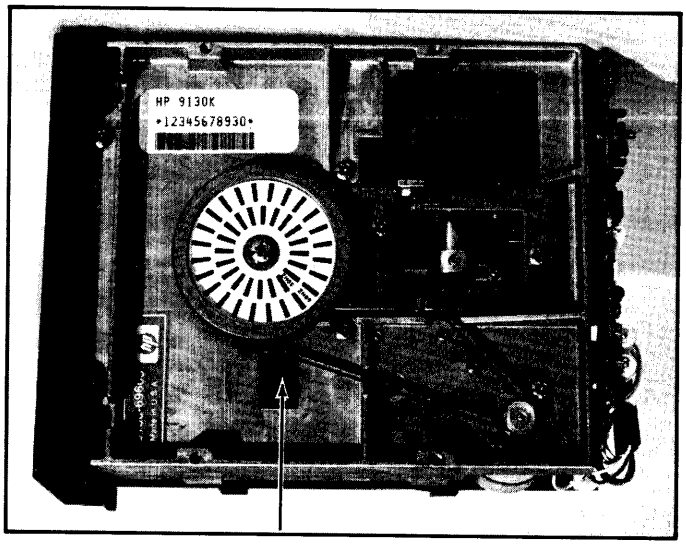


Figure 5-7. Index Detector Retaining Screw

h. The oscilloscope presentation should appear as shown in Figure 5-8.

i. Loosen the index detector retaining screw (Figure 5-7) and move the detector until the INDEX to DATA burst time is approximately 400 uS +/= 300 uS for side 0.

j. Retighten the index detector retaining screw using the torque driver set to 8 inch pounds while observing the scope.

k. Check the INDEX and DATA time for head 1 by going to the DIAG mode and selecting side 1, then press TEST.

l. If the INDEX to DATA time is too far out, adjust the index emitter located on the top side of the drive assembly and then redo steps (i) through (k).

m. Tighten the index emitter and detector retaining screws using the torque driver set to 8 inch pounds.

n. Reassemble the drive assembly.

5-25. WRITE PROTECT SWITCH ADJUSTMENT.

5-26. The disc drive head assembly may be severely damaged while performing this adjustment. For this reason, replacement or adjustment of this switch is not to be done in the field.

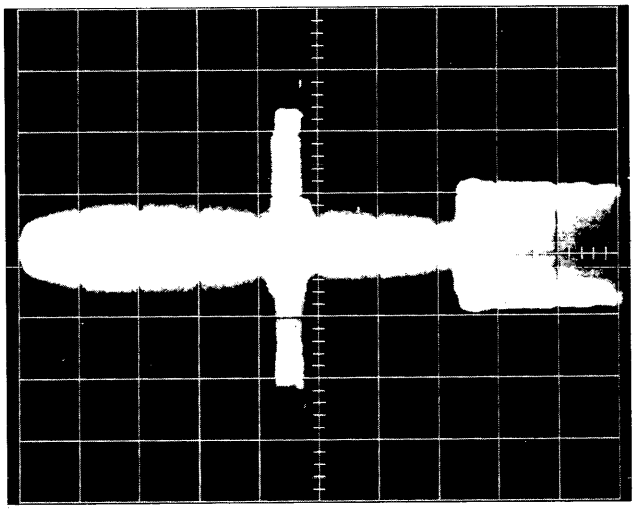


Figure 5-8. Index to Burst Waveform

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts list and throughtout the manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturer's five-digit code numbers.

6-3. ABBREVIATIONS.

6-4. Table 6-1 lists abbreviations used in the parts list, schematics, and throughout the manual. In some cases, two forms of the abbreviation are used: one, all in capital letters; and two, partial or no capitals. This occurs because the abbreviations in the parts list are always capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lowercase and uppercase letters.

6-5. REPLACEABLE PARTS LIST.

6-6. Table 6-2 is the list of replaceable parts and is organized as follows:

a. Chassis-mounted parts in alphanumerical order by reference designator.

b. Electrical assemblies and there components in alphanumerical order by reference designator.

c. Miscellaneous.

6-7. ORDERING INFORMATION.

6-8. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard Sales/Service Office.

6-9. DIRECT MAIL ORDER SYSTEM.

6-10. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount form parts ordered through a local HP Sales/Service Office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices - to provide these advantages, a check or money order must accompany each order.

6-11. Mail-order forms and specific ordering information are available through your local HP Sales/Service Office. Addresses and phone numbers are located at the back of this manual.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without

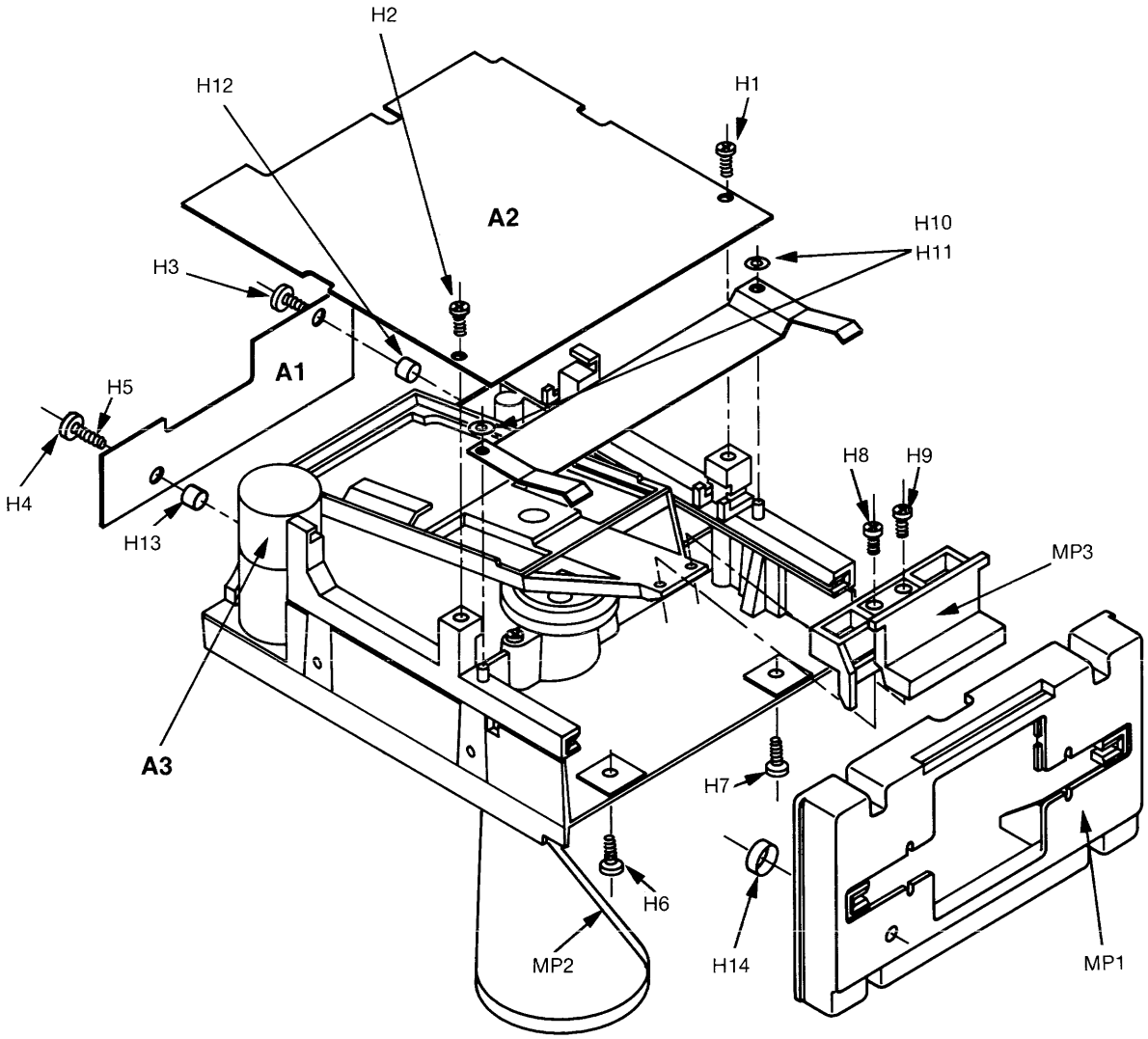


Figure 6-1. A9 or A10 Flexible Disc Drive Exploded View

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A9	09130-69600	1	1	DISK DRIVE EXCHANGE(DOES NOT INCL. A9A2)	28480	09130-69600
A9MP1	4040-1915	8	1	DRIVE-FRONT PANEL	28480	4040-1915
A9MP2	0950-0448	5	1	BELT-DRIVE	28480	0950-0448
A9MP3	4040-1913	6	1	HP LATCH (BROWN)	28480	4040-1913
A9W1	8120-3772	4	1	CABLE-MINI (LEFT)	28480	8120-3772
A9W2	64941-61603	1	1	CABLE-MINI (POWER)	28480	64941-61603
A9A1	09130-66500	4	1	SERVO ELECTRONICS BOARD	28480	09130-66500
A9A2	09130-66501	5	1	DRIVE ELECTRONICS BOARD	28480	09130-66501
A9A3	09130-67920	4	1	MOTOR ASSEMBLY-SERVO	28480	09130-67920
A9A4	09130-67923	7	1	INDEX ASSEMBLY	28480	09130-67923
A9A5	09130-67917	9	1	SWITCH ASSEMBLY-TRACK (LEFT)	28480	09130-67917
A9A6	09130-61604	9	1	LED ASSEMBLY-FRONT PANEL	28480	09130-61604
A10	09130-69600	1	1	DISK DRIVE EXCHANGE(DOES NOT INCL.A10A2)	28480	09130-69600
A10MP1	4040-1915	8	1	DRIVE (FRONT PANEL)	28480	4040-1915
A10MP2	0950-0448	5	1	BELT-DRIVE	28480	0950-0448
A10MP3	4040-1913	6	1	HP LATCH (BROWN)	28480	4040-1913
A10W1	8120-3772	3	1	CABLE-MINI (RIGHT)	28480	8120-3772
A10W2	64941-61603	1	1	CABLE-MINI (POWER)	28480	64941-61603
A10A1	09130-66500	4	1	SERVO ELECTRONICS BOARD	28480	09130-66500
A10A2	09130-66501	5	1	DRIVE ELECTRONICS BOARD	28480	09130-66501
A10A3	09130-67920	4	1	MOTOR ASSEMBLY-SERVO	28480	09130-67920
A10A4	09130-67923	7	1	INDEX ASSEMBLY	28480	09130-67923
A10A5	09130-67417	4	1	SWITCH ASSEMBLY-TRACK (RIGHT)	28480	09130-67417
A10A6	09130-61604	9	1	LED ASSEMBLY(FRONT PANEL)	28480	09130-61604
A10A1	09130-6650	4		SERVO ELECTRONICS BOARD Refer to jumper configuration, Section II when placing Servo Electronics Board	28480	09130-66500
A10A1C1	0180-0058	0	2	CAPACITOR-FXD 50UF+75-10% 25VDC AL	56289	30D506G025CC2
A10A1C2	0180-0058	0		CAPACITOR-FXD 50UF+75-10% 25VDC AL	56289	30D506G025CC2
A10A1C3	0160-4557	0	1	CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A10A1C4	0180-0291	3	1	CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A10A1C5	0160-5334	3	1	CAPACITOR-FXD .01UF 100VDC	28480	0160-5334
A10A1C6	0160-4833	5	1	CAPACITOR-FXD .022UF +-10% 100VDC CER	28480	0160-4833
A10A1H1	1205-0438	5	1	HEAT SINK SGL TO-66-CS	28480	1205-0438
A10A1H2	2420-0001	5	1	NUT-HEX-W/LKWR 6-32-THD .109-IN-THK	00000	ORDER BY DESCRIPTION
A10A1H3	2360-0454	4	2	SCREW-MACH 6-32 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A10A1H4	2360-0454	4		SCREW-MACH 6-32 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A10A1H5	2360-0121	2	1	SCREW-MACH 6-32 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A10A1H6	2190-0060	7	1	WASHER-LK INTL T 1/4 IN .256-IN-ID	28480	2190-0060
A10A1H12	0380-0340	7	2	SPACER-RND .25-IN-LG .143-IN-ID	00000	ORDER BY DESCRIPTION
A10A1H13	0380-0340	7		SPACER-RND .25-IN-LG .143-IN-ID	00000	ORDER BY DESCRIPTION
A10A1J1	1251-4051	3	1	CONNECTOR 10-PIN M POST TYPE	28480	1251-4051
A10A1L1	9140-0607	0	1	INDUCTOR RF-CH-MLD 3.3UH 10% .2DX.45LG	28480	9140-0607
A10A1Q1	1854-0648	4	1	TRANSISTOR NPN 2N6300 SI DARL TO-66	04713	2N6300
A10A1Q2	1854-0215	1	1	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A10A1R1	0683-2035	3	1	RESISTOR 20K 5% .25W FC TC=-400/+800	01121	CB2035
A10A1R2	0683-1055	5	1	RESISTOR 1M 5% .25W FC TC=-800/+900	01121	CB1055
A10A1R3	0757-0280	3	2	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A10A1R4	2100-3154	7	1	RESISTOR-TRMR 1K 10% C SIDE-ADJ 17-TRN	02111	43P102
A10A1R5	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A10A1R6	0757-0469	0	1	RESISTOR 150K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1503-F
A10A1R7	0683-4715	0	2	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A10A1R8	0683-1025	9	3	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A1R9	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A10A1R10	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A1R11	0811-1668	9	1	RESISTOR 1.5 5% 2W PW TC=0+-400	75042	BWH2-1R5-J
A10A1R12	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A1R13	0683-1225	1	1	RESISTOR 1.2K 5% .25W FC TC=-400/+700	01121	CB1225
A10A1R14	0683-2225	3	1	RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A10A1U1	1826-0842	1	1	IC CONV FREQ/V 14-DIP-P PKG	27014	LM2917N
				Subassemblies A9A1 thru A9A6 are the same as A10A1 thru A10A6. Refer to the A10 Listing for these parts and numbers.		

The part number given for the mini drive is an exchange assembly part number. It inlcudes all parts listed for A9 or A10 except A9/A10A2, Drive Electronics Board.

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A10A2	09130-66501	5		DRIVE ELECTRONICS BOARD	28480	09130-66501
A10A2C1	0180-0197	8	1	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A10A2C2	0160-5205	7	3	CAPACITOR-FXD 470PF +-10% 200VDC CER	28480	0160-5205
A10A2C3	0160-5206	8	1	CAPACITOR-FXD 68PF +-10% 200VDC CER	28480	0160-5206
A10A2C4	0160-4441	1	4	CAPACITOR-FXD .47UF +-10% 50VDC CER	28480	0160-4441
A10A2C5	0160-4441	1		CAPACITOR-FXD .47UF +-10% 50VDC CER	28480	0160-4441
A10A2C6	0160-2055	9	16	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C7	0160-4441	1		CAPACITOR-FXD .47UF +-10% 50VDC CER	28480	0160-4441
A10A2C8	0160-4441	1		CAPACITOR-FXD .47UF +-10% 50VDC CER	28480	0160-4441
A10A2C9	0160-5219	3	1	CAPACITOR-FXD 4700PF 100VDC	28480	0160-5219
A10A2C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C11	0160-5208	0	1	CAPACITOR-FXD 270PF +-10% 200VDC CER	28480	0160-5208
A10A2C12	0160-5205	7		CAPACITOR-FXD 470PF +-10% 200VDC CER	28480	0160-5205
A10A2C13	0160-5205	7		CAPACITOR-FXD 470PF +-10% 200VDC CER	28480	0160-5205
A10A2C14	0160-5207	9	1	CAPACITOR-FXD 1200PF +-10% 100VDC CER	28480	0160-5207
A10A2C15	0160-4835	7	2	CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
A10A2C16	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
A10A2C17	0180-0100	3	8	CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
A10A2C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C19	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C20	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C21	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C22	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C23	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C25	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C26	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
A10A2C27	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C28	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C29	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C30	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
A10A2C32	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C33	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C34	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C35	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C36	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
A10A2C37	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
A10A2C38	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
A10A2C39	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
A10A2C40	0160-5209	1	2	CAPACITOR-FXD 330PF +-10% 200VDC CER	28480	0160-5209
A10A2C41	0160-5209	1		CAPACITOR-FXD 330PF +-10% 200VDC CER	28480	0160-5209
A10A2C42	0180-1746	5	1	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A10A2C43	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
A10A2C44	0180-0374	3	1	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A10A2CR1	1901-0050	3	18	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR2	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR3	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR4	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR5	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR6	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR7	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR8	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR9	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR10	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR11	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR12	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR13	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR17	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR18	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR19	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR20	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR21	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR23	1901-0704	4	1	DIODE-PWR RECT 1N4002 100V 1A DO-41	01295	1N4002
A10A2H1	0380-1331	8	2	SPACER	00000	ORDER BY DESCRIPTION
A10A2H2	4040-1854	4	1	SHIELD	28480	4040-1854
A10A2J2	1251-4617	7	1	CONNECTOR 4-PIN M UTILITY	28480	1251-4617
A10A2J3	1251-4051	3	1	CONNECTOR 10-PIN M POST TYPE	28480	1251-4051
A10A2J4	1251-5855	7	1	CONNECTOR 16-PIN M POST TYPE	28480	1251-5855
A10A2L1	9100-2283	8	2	INDUCTOR RF-CH-MLD 390UH 10% .105DX.26LG	28480	9100-2283
A10A2L2	9100-2283	8		INDUCTOR RF-CH-MLD 390UH 10% .105DX.26LG	28480	9100-2283
A10A2L3	9100-2281	6	1	INDUCTOR RF-CH-MLD 270UH 10% .105DX.26LG	28480	9100-2281
A10A2L4	9140-0118	8	1	INDUCTOR RF-CH-MLD 500UH 5% .2DX.45LG	28480	9140-0118

Subassemblies A9A1 thru A9A6 are the same as A10A1 thru A10A6. Refer to the A10 Listing for these parts and numbers.

The part number given for the mini drive is an exchange assembly part number. It inlcudes all parts listed for A9 or A10 except A9/A10A2, Drive Electronics Board.

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A10A2Q1	1854-0215	1	6	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A10A2Q2	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A10A2Q3	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A10A2Q5	1853-0036	2	4	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A10A2Q6	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A10A2Q7	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A10A2Q8	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A10A2Q9	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A10A2Q10	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A10A2Q11	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A10A2R1	0757-0441	8	4	RESISTOR 8.25K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8251-F
A10A2R2	0757-0441	8		RESISTOR 8.25K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8251-F
A10A2R3	0757-0441	8		RESISTOR 8.25K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8251-F
A10A2R4	0698-3159	5	2	RESISTOR 26.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2612-F
A10A2R5	0698-3159	5		RESISTOR 26.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2612-F
A10A2R6	0683-3625	9	1	RESISTOR 3.6K 5% .25W FC TC=-400/+700	01121	CB3625
A10A2R7	0683-1025	9	23	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R8	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R9	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R10	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R11	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R12	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R13	0683-1825	7	1	RESISTOR 1.8K 5% .25W FC TC=-400/+700	01121	CB1825
A10A2R14	0683-1515	2	3	RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
A10A2R16	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R17	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R18	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R19	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R20	0683-7515	4	4	RESISTOR 750 5% .25W FC TC=-400/+600	01121	CB7515
A10A2R21	0683-3915	0	5	RESISTOR 390 5% .25W FC TC=-400/+600	01121	CB3915
A10A2R22	0683-1035	1	4	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A10A2R23	0683-3915	0		RESISTOR 390 5% .25W FC TC=-400/+600	01121	CB3915
A10A2R24	0698-4438	5	1	RESISTOR 3.09K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3091-F
A10A2R25	0698-4462	5	2	RESISTOR 768 1% .125W F TC=0+-100	24546	C4-1/8-T0-768R-F
A10A2R26	0683-3925	2	1	RESISTOR 3.9K 5% .25W FC TC=-400/+700	01121	CB3925
A10A2R27	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R28	0683-4735	4	1	RESISTOR 47K 5% .25W FC TC=-400/+800	01121	CB4735
A10A2R29	0683-2225	3	2	RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A10A2R30	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A10A2R31	0698-3495	2	1	RESISTOR 866 1% .125W F TC=0+-100	24546	C4-1/8-T0-866R-F
A10A2R34	0698-4425	0	1	RESISTOR 1.54K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1541-F
A10A2R35	0698-4462	5		RESISTOR 768 1% .125W F TC=0+-100	24546	C4-1/8-T0-768R-F
A10A2R36	0683-7515	4		RESISTOR 750 5% .25W FC TC=-400/+600	01121	CB7515
A10A2R37	0683-3915	0		RESISTOR 390 5% .25W FC TC=-400/+600	01121	CB3915
A10A2R38	0683-8225	5	2	RESISTOR 8.2K 5% .25W FC TC=-400/+700	01121	CB8225
A10A2R39	0683-3915	0		RESISTOR 390 5% .25W FC TC=-400/+600	01121	CB3915
A10A2R40	0683-7515	4		RESISTOR 750 5% .25W FC TC=-400/+600	01121	CB7515
A10A2R41	0683-8225	5		RESISTOR 8.2K 5% .25W FC TC=-400/+700	01121	CB8225
A10A2R42	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R43	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R44	0683-3025	3	1	RESISTOR 3K 5% .25W FC TC=-400/+700	01121	CB3025
A10A2R45	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A10A2R47	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R48	0683-3015	1	1	RESISTOR 300 5% .25W FC TC=-400/+600	01121	CB3015
A10A2R49	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R52	0683-1515	2		RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
A10A2R53	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R54	0757-0289	2	1	RESISTOR 13.3K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-1332-F
A10A2R55	0698-3449	6	1	RESISTOR 28.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2872-F
A10A2R58	0698-3624	9	1	RESISTOR 150 5% 2W MO TC=0+-200	28480	0698-3624
A10A2R59	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R60	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R61	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R62	0683-1515	2		RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
A10A2R63	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A10A2R64	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R65	0683-7515	4		RESISTOR 750 5% .25W FC TC=-400/+600	01121	CB7515
A10A2R66	0683-3915	0		RESISTOR 390 5% .25W FC TC=-400/+600	01121	CB3915
A10A2R68	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R69	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R70	0757-0416	7	1	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A10A2R71	0698-3158	4	1	RESISTOR 23.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2372-F
A10A2R72	0757-0441	8		RESISTOR 8.25K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8251-F
A10A2R73	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A10A2R74	0683-5125	8	1	RESISTOR 5.1K 5% .25W FC TC=-400/+700	01121	CB5125

Subassemblies A9A1 thru A9A6 are the same as A10A1 thru A10A6. Refer to the A10 Listing for these parts and numbers.

The part number given for the mini drive is an exchange assembly part number. It inlcudes all parts listed for A9 or A10 except A9/A10A2, Drive Electronics Board.

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A10A2R75	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R76	0683-5105	4	1	RESISTOR 51 5% .25W FC TC=-400/+500	01121	CB5105
A10A2U1E	1251-4292	4	1	SHUNT BLOCK	28480	1251-4292
A10A2U1F	1820-0621	2	3	IC BFR TTL NAND QUAD 2-INP	01295	SN7438N
A10A2U2B	1820-0471	0	1	IC INV TTL HEX 1-INP	01295	SN7406N
A10A2U2C	1820-2520	4	1	IC DRVR TTL DUAL	01295	SN75463N
A10A2U2D	1826-0408	5	1	IC 8-DIP-P PKG	32293	ICL8212CPA
A10A2U2E	1820-1416	5	1	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A10A2U2F	1810-0325	2	1	NETWORK-RES 16-DIP150.0 OHM X 8	01121	316B151
A10A2U3A	1826-0064	9	1	IC WIDEBAND AMPL VID 14-DIP-C PKG	04713	MC1733CL
A10A2U3B	1820-1204	9	2	IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
A10A2U3C	1820-0621	2		IC BFR TTL NAND QUAD 2-INP	01295	SN7438N
A10A2U3D	1820-0174	0	1	IC INV TTL HEX	01295	SN7404N
A10A2U3E	1820-0668	7	1	IC BFR TTL NON-INV HEX 1-INP	01295	SN7407N
A10A2U4A	1826-0194	6	1	IC WIDEBAND AMPL VID 14-DIP-P PKG	18324	NE592A
A10A2U4B	1820-1204	9		IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
A10A2U4C	1820-1112	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A10A2U4D	1820-2208	5	2	IC DRVR TTL DUAL	01295	SN75462P
A10A2U4E	1820-2208	5		IC DRVR TTL DUAL	01295	SN75462P
A10A2U4F	1820-0621	2		IC BFR TTL NAND QUAD 2-INP	01295	SN7438N
A10A2U5B	1826-0065	0	1	IC COMPARATOR PRCN 8-DIP-P PKG	S0545	UPC311C
A10A2U5C	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A10A2U5D	1820-1211	8	1	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A10A2U5E	1820-1260	7	1	IC MV TTL MONOSTBL DUAL	01295	SN74221N
A10A2XU1E	1200-0853	8	2	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
A10A2XU2F	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
A10A3	09130-67920			SERVO MOTOR ASSEMBLY	28480	09130-67920
A10A3B1	3140-0654		1	MOTOR-SPINDLE DRIVE	28480	3140-0654
A10A3H1	3050-1056		2	WASHER-SHOULDERED	51506	15250-050-065-N-1
A10A3H2	2360-0332		2	SCREW-MACH 6-32	28480	2360-0332
A10A3MP1	1401-0180		1	CAP-MOTOR END	28480	1401-0180
A10A3MP2	1600-1024		1	SHIELD-MOTOR	28480	1600-1024
A10A3P2	1251-4273		1	CONNECTOR-5-PIN FEMALE	28480	1251-4273
A10A4	09130-67923	7		INDEX ASSEMBLY	28480	09130-67923
A10A4CR1	1990-0443	5	1	LED-INFRARED BVR=2V	28480	1990-0443
A10A4H1	2360-0331	6	1	SCREW-MACH 6-32	28480	2360-0331
A10A4H2	2360-0119	8	1	SCREW-MACH 6-32	00000	ORDER BY DESCRIPTION
A10A4H3	3050-0635	7	1	WASHER-FLAT	28480	3050-0635
A10A4MP1	4040-1852	2	1	HOLDER-EMITTER	28480	4040-1852
A10A4MP2	4040-1851	1	1	HOLDER-DETECTOR	28480	4040-1851
A10A4P10	1251-3965	6	1	CONNECTOR-4-PIN FEMALE	28480	1251-3965
A10A4Q1	1990-0792	7	1	TRANSISTOR-PHOTO	01295	TIL99
A10A5	09130-67917	9		SWITCH ASSEMBLY-TRACK LEFT	28480	09130-67917
A10A5H1	2360-0331	6	1	SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	28480	2360-0331
A10A5H2	2200-0149	6	2	SCREW-MACH 4-40 .625-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A10A5H3	3050-0222	8	2	WASHER-FL MTLC NO. 4 .125-IN-ID	28480	3050-0222
A10A5H4	1600-1059	6	2	SPRING-MODULE	28480	1600-1059
A10A5H5	2360-0370	3	2	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A10A5MP1	1600-1025	6	1	BRACKET-SWITCH	28480	1600-1025
A10A5MP2	0590-1312	0	1	NUT PLATE 4-40	00000	ORDER BY DESCRIPTION
A10A5MP3	4040-1847	5	1	HOLDER-SPRING	28480	4040-1847
A10A5P11	1251-3965	6	1	CONNECTOR-4-PIN FEMALE	28480	1251-3965
A10A5S2	3101-2438	1	2	SWITCH-TRACK (LEFT OR RIGHT)	28480	3101-2438
A10A6	09130-61604	9		LED ASSEMBLY-FRONT PANEL	28480	09130-61604
A10A6CR3	1990-0794	9	1	DIODE-LED (RED)	71744	CM4-23
A10A6H14	1250-0610	0	1	BUSHING-COLLAR LED	28480	1250-0610
A10A6P9	1251-3965	6	1	CONNECTOR-4 PIN FEMALE	28480	1251-3965
A10A7	64100-65501	3	1	SHIELD BOX ASSEMBLY	28480	64100-65501

Subassemblies A9A1 thru A9A6 are the same as A10A1 thru A10A6. Refer to the A10 Listing for these parts and numbers.

The part number given for the mini drive is an exchange assembly part number. It inlcudes all parts listed for A9 or A10 except A9/A10A2, Drive Electronics Board.

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A11	64941-66501	2	1	FLOPPY CONTROL BOARD	28480	64100-66501
A11C1	0180-0374	3	3	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A11C2	0160-2055	9	19	CAPACITOR-FXD .01UF+80-20% 100VDC CER	28480	0160-2055
A11C3	0180-0116	1	2	CAPACITOR-FXD 6.8UF +- 10% 35VDC TA	56289	150D685X9035B2
A11C4	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C5	0160-0300	3	1	CAPACITOR-FXD 2700PF +-10% 200VDC POLYE	28480	0160-0300
A11C6	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C7	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C8	0180-0116	1		CAPACITOR-FXD 6.8UF +-10% 35VDC TA	56289	150D685X9035B2
A11C9	0180-0309	4	1	CAPACITOR-FXD 4.7UF +-20% 10VDC TA	56289	150D475X0010A2
A11C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C12	0160-0298	8	2	CAPACITOR-FXD 1500PF +-10% 200VDC POLYE	28480	0160-0298
A11C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C15	0140-0226	0	2	CAPACITOR-FXD 320PF +-1% 300VDC MICA	72136	DM15F321F0300WV1C
A11C16	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C19	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C20	0140-0226	0		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0140-0226
A11C21	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C22	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C23	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C24	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C25	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C26	0180-1731	8	3	CAPACITOR-FXD 4.7UF +-10% 50VDC TA	56289	150D475X9050B2
A11C27	0180-1731	8		CAPACITOR-FXD 4.7UF +-10% 50VDC TA	56289	150D475X9050B2
A11C28	0180-1731	8		CAPACITOR-FXD 4.7UF +-10% 50VDC TA	56289	150D475X9050B2
A11C29	0160-0298	8		CAPACITOR-FXD 1500PF +-10% 200VDC POLYE	28480	0160-0298
A11C30	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C31	0180-0374	3		CAPACITOR-FXD 10UF +-10% 20VDC TA	56289	150D106X9020B2
A11C32	0180-1731	3		CAPACITOR-FXD 10UF +-10% 20VDC TA	56289	150D106X9020B2
A11C33	0160-0336	0	3	CAPACITOR-FXD 100PF +-1% 300VDC MICA	28480	0160-0336
A11C34	0160-0336	0	3	CAPACITOR-FXD 100PF +-1% 300VDC MICA	28480	0160-0336
A11C35	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C36	0160-0336	0		CAPACITOR-FXD 100PF +-1% 300VDC MICA	28480	0160-0336
A11CR1	1901-0040	1	2	DIODE-SWITCHING 30V 50MA 2MS D0-35	28480	1901-0040
A11CR2	1901-0040	1	6	DIODE-SWITCHING 30V 50MA 2MS D0-35	28480	1901-0040
A11CR3, CR4	1901-0028	5	2	DIODE-PWR RECT 400V 750MA D0-29	28480	1901-0028
A11E1	1258-0151	0	1	PROGRAM HEADER	28480	1258-0151
A11E2	1258-0151	0	1	PROGRAM HEADER	28480	1258-0151
A11H1	1205-0449	8	1	HEAD SINK	28480	1205-0449
A11H2	2420-0001	5	6	NUT-HEX-W/LKWR 6-32-THD .109-IN-THK	00000	ORDER BY DESCRIPTION
A11H3	2360-0115	4	4	SCREW-MACH 6-32 .312-IN-LG	00000	ORDER BY DESCRIPTION
A11H4	2360-0121	2	2	SCREW-MACH 6-32 .5-IN-LG PAN-HD-POZ1	27014	LM338K
A11J1, J2	1251-4837	3	2	CONNECTOR 4-PIN M METRIC POST TYPE	28480	1251-4837

See introduction to this section for ordering information

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A11R1	0757-0442	9	8	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A11R2	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A11R3	0757-0280	3	7	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A11R4	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A11R5	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A11R6	0757-0273	4		RESISTOR 3.01K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3011-F
A11R7	0757-1094	9	1	RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A11R8	0757-0438	3	1	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A11R9	0757-0273	4		RESISTOR 3.01K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3011-F
A11R10	0757-0455	4	2	RESISTOR 36.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3625-F
A11R11	0757-0455	4		RESISTOR 36.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3625-F
A11R12	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A11R13	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A11R14	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A11R15	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A11R16	0698-3154	0	4	RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A11R17	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A11R18	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A11R19	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A11R20	0698-3156	2	1	RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A11R22	0698-3154	0		RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A11R23	0698-3154	0		RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A11R24	0698-3154	0		RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A11R25	0698-7401	1	1	RESISTOR 1.71K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1621-F
A11R26	0698-7518	8	1	RESISTOR 200 .25% .125W F TC=0+-50	19701	MF4C1/8-T2--200R-C
A11R27	0757-0429	2	2	RESISTOR 1.82K 1% .125W F TC =0+-100	24546	C4-1/8-T0-1821-F
A11R28	0757-0280	3		RESISTOR 1K 1% .125W F TC =0+-100	24546	C4-1/8-T0-1001-F
A11R29	0757-0429	2		RESISTOR 1.82K 1% .125W F TC =0+-100	24546	C4-1/8-T0-1821-F
A11R30	0757-0280	3		RESISTOR 1K 1% .125W F TC =0+-100	24546	C4-1/8-T0-1001-F
A11R31	0757-0461	2	2	RESISTOR 68.1K 1% .125W F TC =0+-100	24546	C4-1/8-T0-6812-F
A11R32	0757-0280	3		RESISTOR 1K 1% .125W F TC =0+-100	24546	C4-1/8-T0-1001-F
A11R33	0757-0461	2	2	RESISTOR 68.1K 1% .125W F TC =0+-100	24546	C4-1/8-T0-6812-F
A11R34	0757-0416	7	1	RESISTOR 511 1% .125W F TC =0+-100	24546	C4-1/8-T0-511R-F
A11TP's	0360-0535	0	20	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A11U1	1820-1470	1	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A11U2	1810-0271	7	1	NETWORK-RES 10-SIP200.0 OHM X 9	01121	210A201
A11U3	1820-1633	8	2	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
A11U4	1820-2456	5	1	IC-FD1791A-01	28480	1820-2456
A11U5	1810-0280	8	1	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
A11U6	1820-1425	6	1	IC SCHMITT-TRIG TTL LS NAND QUAD 1-INP	01295	SN74LS132N
A11U9	1820-1112	8	3	IC FF TTL LS D-TYPE POS-FDGE-TRIG	01295	SN74LS74AN
A11U10	1820-1112	8		IC FF TTL LS D-TYPE POS-FDGE-TRIG	01295	SN74LS74AN
A11U11	1820-0535	8	1	IC DRVR TTL AND DUAL 2-INP	01295	SN75451BP
A11U12	1826-0207	2	1	IC OP AMP WB 8-DIP-P PKG	01295	LM318P
A11U13	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
A11U14	1820-1858	9	1	IC FF TTL LS D-TYPE OCTL	1295	SN74LS377N
A11U17	1820-1212	9	5	IC FF TTL LS J-K NEG-EDGE-TRIG	1295	SN74LS112AN
A11U18	1820-1244	7	1	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS153N
A11U19	1820-1212	9		IC FF TTL LS J-K NEG-EDGE-TRIG	1295	SN74LS112AN
A11U20	1820-1212	9		IC FF TTL LS J-K NEG-EDGE-TRIG	1295	SN74LS112AN
A11U21	1820-1212	9		IC FF TTL LS J-K NEG-EDGE-TRIG	1295	SN74LS112AN
A11U22	1820-1997	7	6	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A11U23	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A11U24	1820-1730	6	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A11U25	1820-2024	3	2	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A11U26	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A11U27	1820-1260	7	2	IC MV TTL MONOSTBL DUAL	1295	SN74221N
A11U28	1820-1428	9	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAL	01295	SN74LS158N
A11U29	1820-1989	7	2	IC CNTR TTL LS BIN DUAL 4-BIT	01295	SN74LS02N
A11U30	1820-1433	6	1	IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
A11U31	1820-1260	7		IC MV TTL MONOSTBL DUAL	01295	SN74221N
A11U32	64110-10001	5	1	ROM-ASM CONTROL	28480	64110-10001
A11U33	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A11U34	1820-1212	9		IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
A11U35	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS138N
A11U36	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS240N
A11U37	1820-1997	7		IC FF TTL LS D-TYP POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A11U38	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A11U39	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A11U40	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A11U41	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A11U42	64110-10002	6	1	ROM-ASM OUT DC	28480	64110-10002
A11U43	1820-1246	9	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS09N

See introduction to this section for ordering information

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A11U44	1820-1197	9	3	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS00N
A11U45	1820-1428	9		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS158N
A11U46	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A11U47	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01121	210A103
A11U48	1820-1989	7		IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
A11U49	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A11U50	2830-1423	4	1	IC MV TTL LS MONOSTBLE RETRIG DUAL	01295	SN74LS123N
A11U51	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A11VR1	1826-0677	0	1	IC V RGLTR-ADJ-POS 1.2/32V TO -3 PKG		
A11XU4	1200-0654	7	1	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A11XU7	1200-0638	7	7	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A11XU8	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A11XU15	1200-0639	8	19	SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU16	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU18	1200-0607	0	6	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A11XU22	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU23	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU24	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU25	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU26	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU27	1200-0607	0		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0607
A11XU29	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU31	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A11XU32	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A11XU33	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU37	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU38	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU39	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU40	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU41	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU42	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU43	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU44	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU47	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU49	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU50	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A11W1	8120-3772	3	1	CABLE-MINI	28480	8120-3772
A11Y1	0410-1298	1	1	CRYSTAL-QUARTZ 4MHZ HC-18/U-HLDR	28480	0410-1298

Table 6-3. List of Manufacturers' Codes

Mfr No.	Manufacturer Name	Address	Zip Code
S0545	NIPPON ELECTRIC CO	TOKYO JP	
00000	ANY SATISFACTORY SUPPLIER		
01121	ALLEN-BRADLEY CO	MILWAUKEE WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS TX	75222
02111	SPECTROL ELECTRONICS CORP	CITY OF IND CA	91745
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX AZ	85008
16299	CORNING GLASS WKS COMPONENT DIV	RALEIGH NC	27604
18324	SIGNETICS CORP	SUNNYVALE CA	94086
19701	MEPCO/ELECTRA CORP	MINERAL WELLS TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD PA	16701
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO CA	94304
32293	INTERSIL INC	CUPERTINO CA	95014
51506	ACCURATE SCREW MACHINE CO	MONTVALE NJ	07645
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS MA	01247
71744	CHICAGO MINIATURE LAMP WORKS	CHICAGO IL	60640
72136	ELECTRO MOTIVE CORP	FLORENCE SC	06226
75042	TRW INC PHILADELPHIA DIV	PHILADELPHIA PA	19108

SECTION VII

MANUAL BACKDATING

7-1. GENERAL.

7-2. There is no backdating material at the printing of this manual.

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2. This section provides information to service the flexible disc control and drives. If an error has occurred while using the flexible disc drive option, use this section to diagnose the problem and troubleshoot it.

8-3. This section is divided into two groups. The first contains the fundamentals of flexible disc recording, and block and component level theory-of-operation. This information should help the user understand the operation of the flexible disc drive. The second portion contains troubleshooting information. This includes descriptions of the error messages given during PV and DIAG tests, troubleshooting using signature analysis, troubleshooting hints, and detailed service sheets.

8-4. SAFETY CONSIDERATIONS.

8-5. Read the Safety Summary at the front of this manual before servicing this instrument. Review each procedure before performing it for CAUTIONs and WARNINGs given in the procedures. For example, when working around the power supply and the display circuitry in the mainframe; CAUTION should be taken to avoid the potentially lethal voltages! In general however, the flexible disc drives use only +-12 Volts and +5 Volts.

8-6. FLEXIBLE DISC RECORDING FUNDAMENTALS.

8-7. To better understand the operation of the flexible disc drive, read this brief description of disc recording principles. Refer to figures 8-1 through 8-3 while reading this section.

8-8. The flexible magnetic media used with the 64100A option 041 disc drive measures 5.25 inches in diameter. Both surfaces are coated with a ferromagnetic iron oxide. Both sides are used for data storage. Each side contains 35 circular tracks. Each track is divided into 16 pie slice shaped regions called sectors. A sector can contain up to 256 bytes of data. Surface, track and sector information is used to reference data location on the disc. Data is encoded on the disc (ones and zeros) by changing the orientation of small magnetic dipoles in the magnetic coating on the disc. There is no correlation between magnetic polarity of the dipoles and the ones and zeros. The ones and zeros are indicated by the location of the dipole polarity transitions.

8-9. The disc is soft sectored; that is, there is no hardware indication of where each sector begins. In order to allow soft sectoring, each sector is divided into two fields. For each sector there is an ID field which contains information to identify the sector. Next there is a data field which contains the actual data. Thus, the ID field serves as a fixed marker for the beginning of each sector.

8-10. The makeup of the ID and DATA fields are similar. Both fields begin with a series of synchronization bytes (zeros). These bytes allow the decoder circuitry of the controller time to synchronize itself with the data on the disc. Following the synchronizing bytes, is the address mark byte which indicates that the beginning of an ID or DATA field has been located. The address mark is a specially recorded data pattern that does not occur in any data stream and is used to sychronize the data decoding circuits in the Mini Disc Controller (MDC).

8-11. A series of information bytes follows the address mark. In an ID field, these bytes indicate the logical cylinder, head and sector address. In a DATA field, these bytes are the data being stored in the sector.

8-12. At the end of each field are two cyclic redundance check (CRC) bytes. This check word (16 bits long) allows detection of most errors that occur in the data storage and recovery of information from a disc.

8-13. There are two gaps following each field on a track. The gaps allow for variations in disc rotational speed, index detector alignment variations and time for the hardware to prepare for the next field.

8-14. The logical sectors are numbered consecutively. However, the sectors (see figure 8-2) may occur in any physical order around the track. This allows the sectors to be staggered to optimize system performance (interleaving).

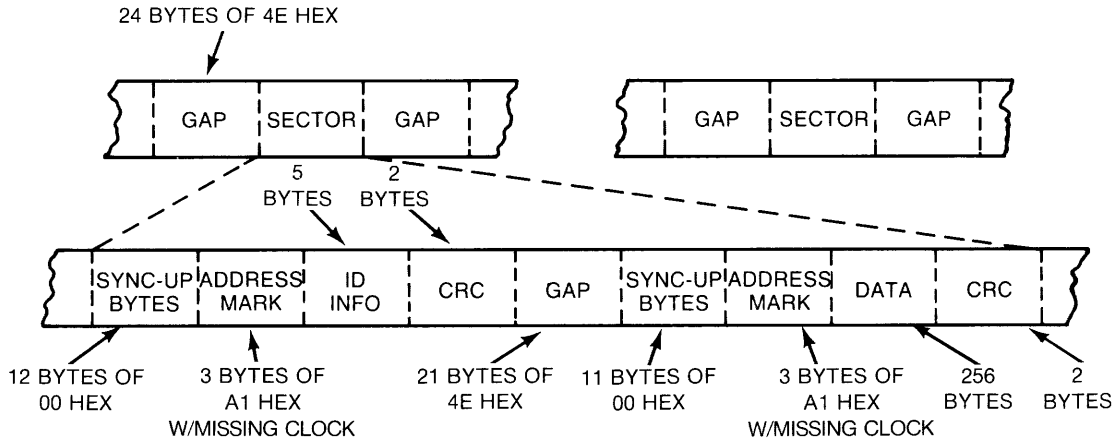


Figure 8-1. ID and Data Field Content

8-15. The outermost track on the disc is track 0 and the intermost track is 34. Each track has a physical address as described previously. There is also a logical track address associated with each good track. The logical track address is written in the ID field of each sector on the track.

8-16. The recording head (see Figure 8-3) is moved in and out by a stepper motor assembly. Write current passes through the head coil to selectively magnetize portions of the disc. To read back data, the magnetized material is passed under the head.

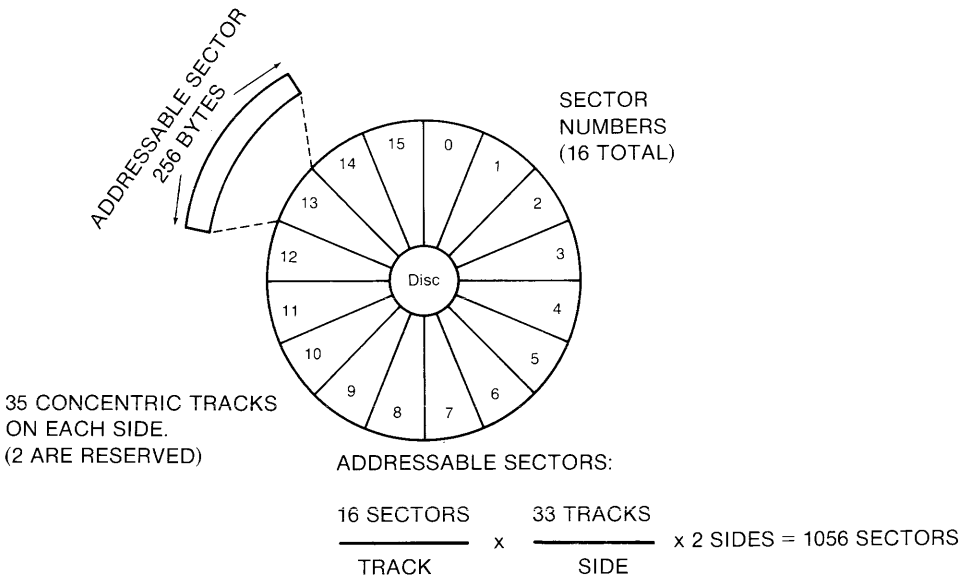


Figure 8-2. Media Sector and Track Structure

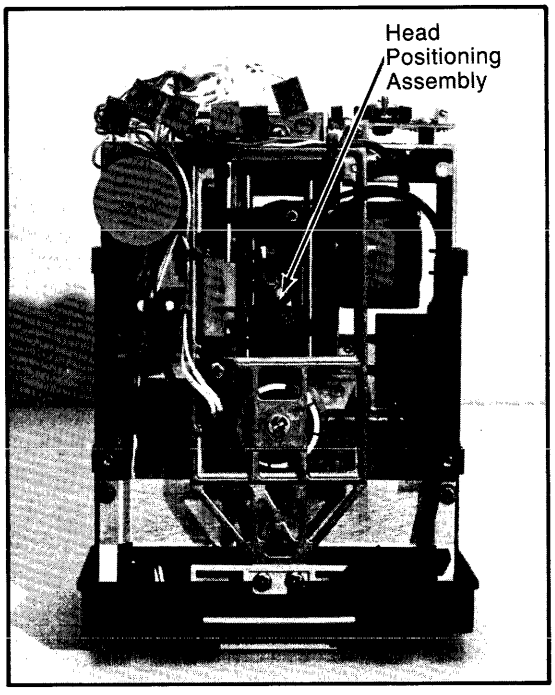


Figure 8-3. Head Positioning Assembly

8-17. BLOCK DIAGRAM THEORY.

8-18. The Local Mass Storage is divided into two major functions; the first function is the Mini Controller, and the second is the flexible disc drives.

8-19. The block diagram for the Mini Controller and Flexible Disc Drive functions is shown on figure 8-4. The left half of the Block diagram is the Mini Control board A11 and the right half is showing the Flexible Disc Drives (Drive 0 and 1) with drive 0 showing the internal functions. Figure 8-5 is a more detailed block diagram of the flexible disc drives.

8-20. MINI CONTROL BLOCK THEORY.

8-21. The Mini Controller is part of the 64100A mainframe. It interfaces the flexible disc drives with the mainframe by supplying the drive with power, data, timing, and control signals.

8-22. The Mini Controller is divided into eleven subfunctions.

a. Interface Control Latch

b. DMA/CPU Address Selector

c. SA Stimulus Latch

d. CPU Interface/DMA State Machine

e. Data Latches

f. 4MHz Oscillator

g. Mini Drive Controller

h. Drive Control Latches/Buffers

i. Drive Status Buffers

j. Data Separator

k. Disc Drive Multiplexer and Control Buffering

8-23. INTERFACE CONTROL LATCH.

8-24. Refer to figure 8-4. The control latch is responsible for capturing the upper byte of I/O data and providing this information to the DMA/CPU Address selector.

8-25. DMA/CPU ADDRESS SELECTOR.

8-26. Refer to figure 8-4. The address selector, which is gated by the state machine, generates control signals to the Mini Drive Control chip (MDC). The state of the control signals is determined by the output of the interface control latch.

8-27. SIGNATURE ANALYSIS STIMULUS LATCH.

8-28. Refer to figure 8-4. The output of the SA stimulus latch can be connected to either the input of the DMA state machine, jumper E2, or to the inputs of the data separator circuitry, jumper E1. This facilitates troubleshooting of the DMA state machine and data separator by forcing them into known state sequences.

8-29. CPU INTERFACE/DMA STATE MACHINE.

8-30. Refer to figure 8-4. The CPU Interface/DMA State Machine performs two functions. First, a major portion of the circuitry does byte packing and unpacking so that the 16 bit I/O bus can interface to the 8 bit bus of the MDC. Second, the state machine provides signals for enabling the data latches and providing next state information for itself.

8-31. DATA LATCHES.

8-32. Refer to figure 8-4. The data latches are used for loading and transfering 8 bit read/write, status and control signals to and from the drive circuitry from the 16 bit 64100A I/O bus. The enabling and clocking of the data latches is performed by the DMA state machine.

8-33. 4 MHZ OSCILLATOR.

8-34. Refer to figure 8-4. The oscillator block is comprised of a 4Mhz crystal oscillator that is used to clock a 4 bit binary counter. The 2Mhz and 500Khz outputs are used to clock the data separator and the 1Mhz output is used to clock the Mini Drive Controller chip.

8-35. MINI DRIVE CONTROLLER (MDC) CHIP.

8-36. Refer to figure 8-4. The Mmini Drive Controller (MDC) chip is divided into two functions. The first is the microprocessor interface that uses control signals to determine whether it is in a read or a write mode. Then, once it has determined it's R/W status it will then read or write data via the data access lines to the data latches. The second section, the disc interface, implements the commands from the microprocessor interface section. The disc interface section processes commands and status signals from the disc drive MUX. Also, the MDC will provide encoded information to be written onto the disc and a means of decoding read data to be output to the system.

8-37. DRIVE CONTROL LATCH/BUFFER.

8-38. Refer to figure 8-4. This block is responsible for providing control signals to each disc drive.

8-39. DRIVE STATUS BUFFERS.

8-40. Refer to figure 8-4. The drive status buffers provide the system with information necessary to determine the status of the disc drives.

8-41. DATA SEPARATOR.

8-42. Refer to figure 8-4. This block is responsible for dividing the 1's and 0's on the data stream into half bit cells, and phase locking this data for use by the MDC. The data stream consists of raw encoded information from the disc. Furthermore, the raw read information is delayed and phase locked with a read clock as soon as seven sync bytes have been read from the disc.

8-43. DISC DRIVE MULTIPLEXER AND CONTROL BUFFERING.

8-44. Refer to figure 8-4. This block is the final interface to the disc drives. The multiplexer selects between the two sets of signals going to/from the two flexible disc drives depending on which drive is currently active.

8-45. DISC DRIVE BLOCK THEORY.

8-46. This section describes the block digram theory for the disc drives. Figure 8-5 is a detailed block diagram of the disc drives.

8-47. INDEX PULSE SHAPING NETWORK.

8-48. The index pulse circuitry consists of an index LED, photo transistor and pulse shaping network. The index hole in the flexible disc passes between the index LED and photo transistor, causing the photo transistor to conduct. The detected signal is then shaped and buffered and output on the Index Pulse interface line (J1-8). This signal although inverted may be observed at TP7 on the Drive Electronics board.

8-49. WRITE PROTECT SENSOR.

8-50. The write protect sensor consists of a switch which is opened when a write protected disc is inserted into the drive. This signal is delayed by an RF filter to eliminate transient noise from the switch. This will cause the write protect line (J1-28) to go low and TP9 to go high.

8-51. TRACK 0 SWITCH.

8-52. The level on the Track 0 interface is a function of the head assembly position. When the head assembly is positioned at track 0 and the stepper motor indicates phase 0, J4-19 is pulled low, causing TP8 and the Track 0 interface line to be pulled low.

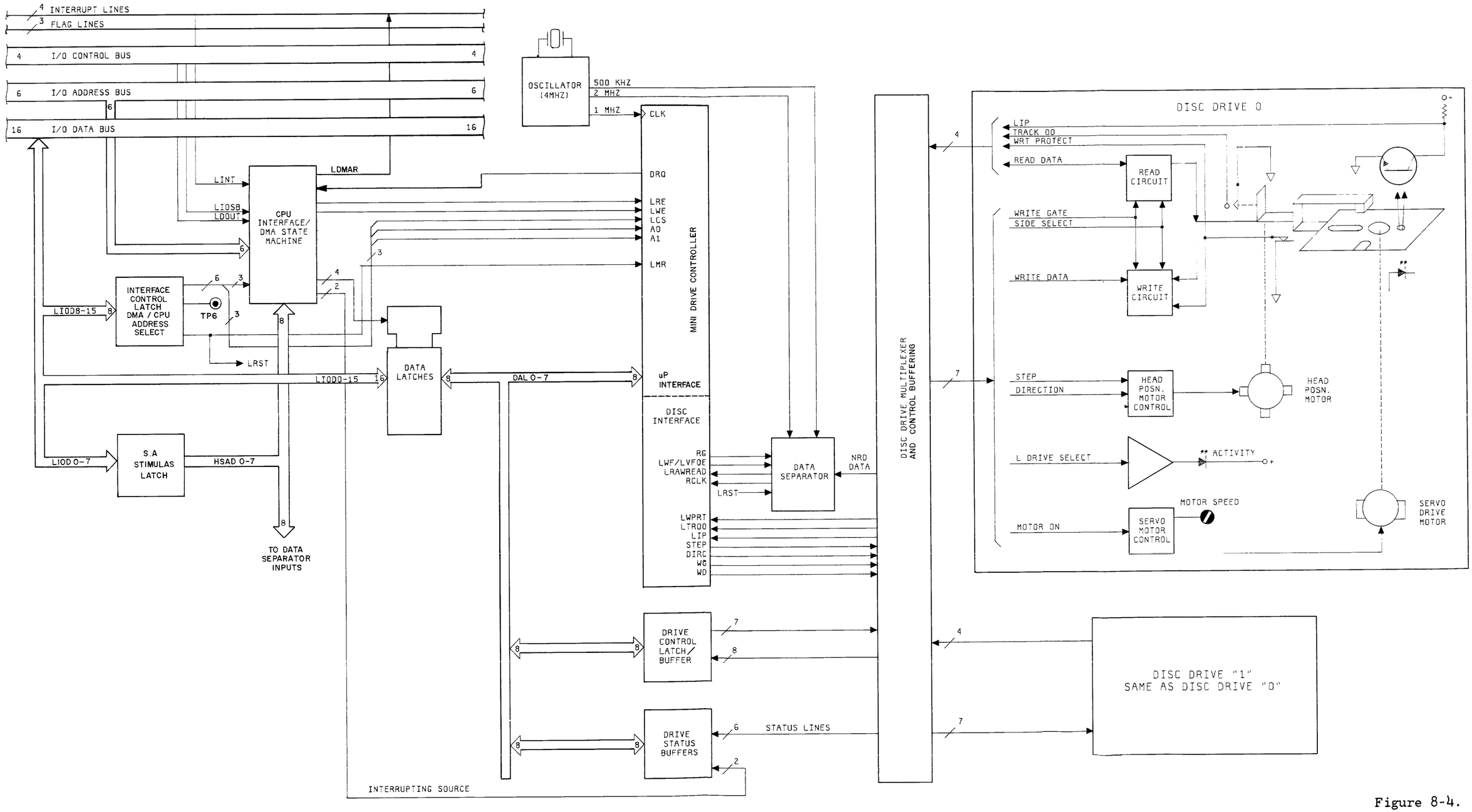


Figure 8-4.
Mini Control Block Diagram

8-53. SPINDLE MOTOR DRIVE CONTROL.

8-54. The spindle drive system consists of a spindle assembly driven by a DC motor-tachometer combination and the Servo Electronics board.

8-55. The Servo Electronics includes a current limiter and interface control line.

8-56. When the Drive Motor Enable line is low, the drive motor is allowed to come up to speed. This speed is adjustable by potentiometer R4 located on the Servo Electronics board.

8-57. A current sensing resistor, also located on the servo electronics board limits the motor current to 900mA. If this limit is exceeded, the motor is disabled.

8-58. HEAD POSITION CONTROL.

8-59. The head position control consists of a four phase stepper motor drive which changes one phase for each track advancement of the head assembly. In addition to the logic for motion control, a gate is provided to inhibit repositioning during a write operation.

8-60. POWER ON CIRCUIT.

8-61. This circuit detects when the +5VDC and +12VDC are valid and prevents writing/reading/erasing/stepping until such time.

8-62. DATA CIRCUITRY.

8-63. All signals required to control the data circuitry are provided by the host system and are shown in the functional block diagram of Figure 8-5. These signals are as follows:

a. Drive Select
b. Write Enable
c. Write Data
d. Side Select

8-64. There are 4 drive select lines connected to the data electronics. A shunt block determines the drive number. The drive number is established by clipping three of the jumpers on the shunt block or adding a shunt to an empty block. When the selected drive select line is pulled low, the data circuitry is enabled and the drive is conditioned to respond to step or read/write commands. On the 64100A option 041 all of the jumpers are intact and the drive is enabled with DS0.

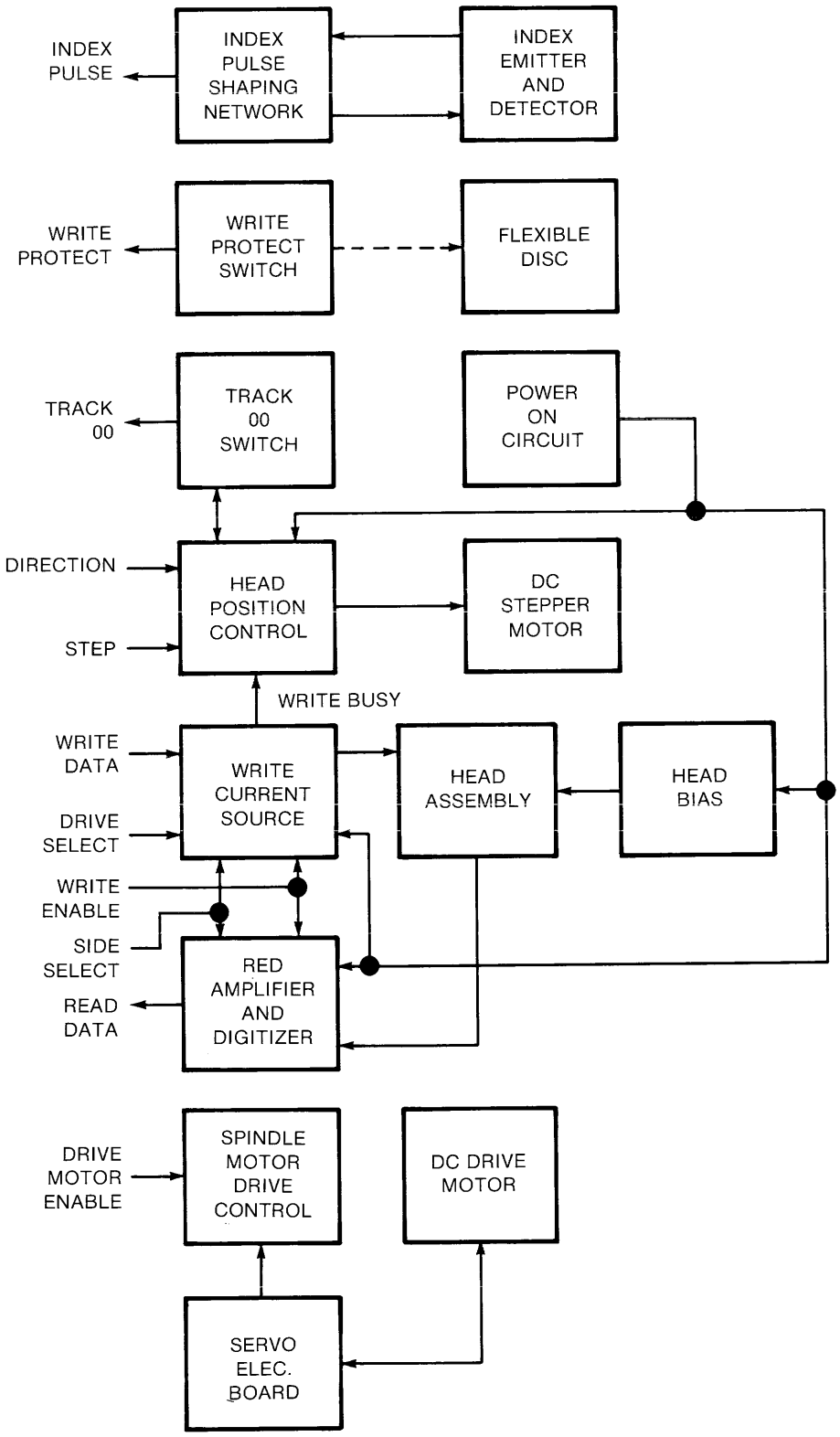


Figure 8-5. Mini Drive Block Diagram

8-65. WRITING DATA.

8-66. The write electronics consists of the following circuits:

a. Write/erase current source
b. Waveform generator
c. Trim erase current source
d. Head select logic
e. Bias Source

8-67. The read/write winding on the head is center tapped. During a write operation, the current from the write current source flows in the alternate halves of the winding under the control of the write waveform generator.

8-68. Before recording can begin, certain conditions must be satisfied . The conditions required before writing (i.e., unit ready) must be established by the host system as follows:

a. Drive speed stabilization. This will exist 250mS after starting the drive motor.

b. Subsequent to any step operation, the positioner must be allowed to settle. This requires 20mS total after the last step pulse is initiated, i.e., 5mS for the step motion and 15mS for settling.

8-69. The following operations are performed when writing data. These operations may be overlapped if required.

8-70. Figure 8-6 shows the relevent timing diagram for a write operation. At T=0 when the unit is ready, the write enable line goes low. This enables the write current source and bias circuitry.

8-71. Since the trim erase gaps are behind the read/write gap, the TRIM ERASE control goes true 390uS after the WRITE ENABLE interface line. It should be noted that this value is optimized between the requirements at track 0 and track 34 so that the effect of the trim erase gaps on previous information is minimized.

8-72. Figure 8-6 shows the information on the WRITE DATA interface line, and the output of the write waveform generator which toggles on the leading edge of every WRITE DATA pulse.

8-73. At the end of recording, at least one additional pulse on the WRITE DATA line must be inserted after the last significant WRITE DATA pulse to avoid excessive peak shift effects.

8-74. The TRIM ERASE signal must remain true for 800uS after the termination of WRITE ENABLE to ensure that all recorded data are trim erased. This value is again optimized between the requirements at track 0 and 34.

8-75. The duration of a write operation is from the true going edge of WRITE ENABLE to the false going edge of TRIM ERASE. This is indicated by the internal WRITE BUSY waveform shown.

8-76. READING DATA.

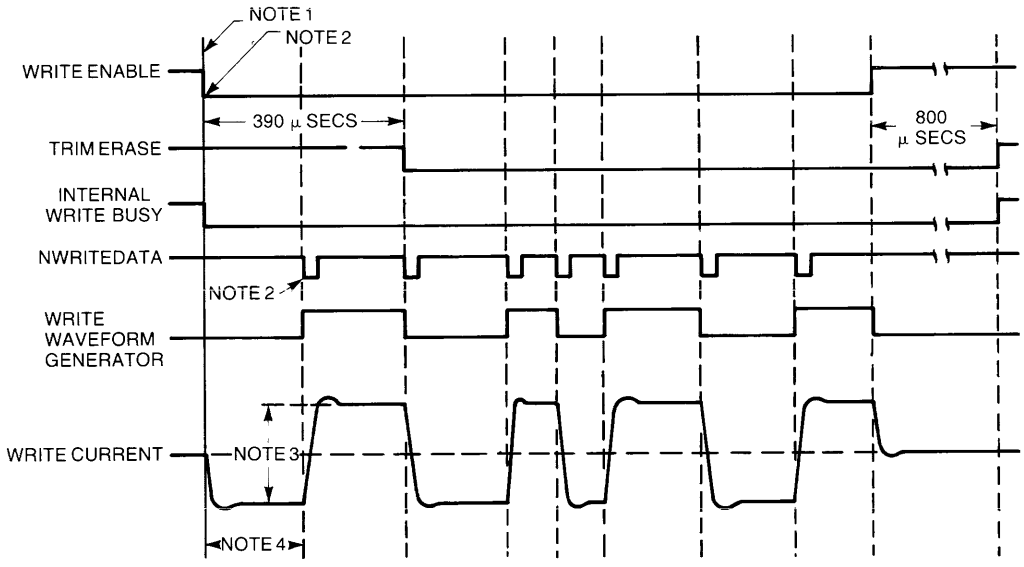
8-77. The read electronics consists of the following circuitry:

a. Read switch/side select
b. Read amplifier
c. Filter
d. Differentiator
e. 0 Crossing detector

8-78. The read switch is used to isolate the read amplifier from the voltage excursion across the magnetic head during a write operation. The side select is used to enable one of the read/write/erase heads.

8-79. Before reading can begin, the drive must be in a ready condition. As with the data recording operation, this ready condition must be established for data recording. A 100uS delay must exist from the trailing edge of the TRIM ERASE signal to allow the read amplifier to settle after the transient caused by the read switch returning to the read mode.

8-80. Referring to figure 8-7, the output signal from the read/write head is amplified by a read amplifier and filtered to remove noise by a linear phase filter. The linear output from the filter is passed to the differentiator which generates a waveform whose zero crossovers correspond to the peaks of the read signal. This signal is then fed to the comparator and digitizer circuit.



NOTES: 1. 1 = 0 = 250 Milliseconds after drive motor starts or 20 milliseconds after last step pulse, (whichever is the latest time)
2. Unsynchronized
3. 8.5 ma peak to peak
4. 4 μ seconds minimun, 8 μ seconds maximum

Figure 8-6. Write Timing Diagram

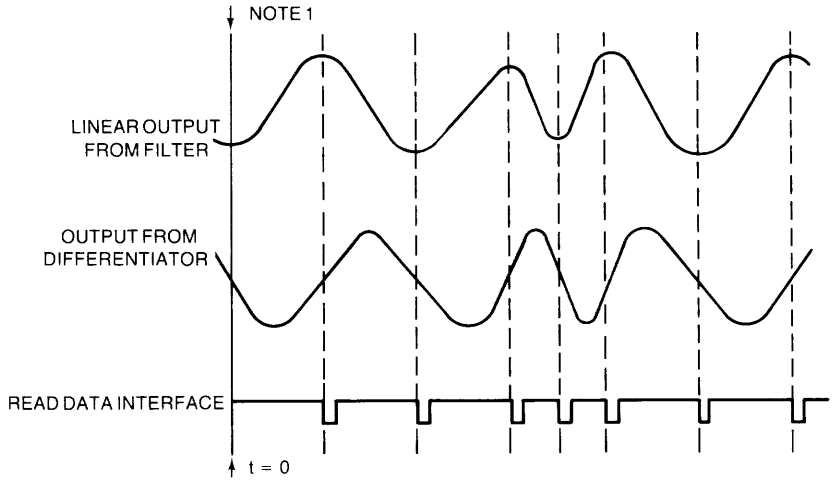
8-81. The comparator and digitizer circuitry generates a 1uS READ DATA pulse corresponding to each peak of the read signal. This composite read data signal is then sent to the host system via the READ DATA interface line.

8-82. MINI CONTROL THEORY OF OPERATION.

8-83. MINI CONTROL.
(See service sheets 11A, 11B figures 8-9 and 8-11)

8-84. The CPU may execute I/O to any 1 of 16 peripheral addresses (defined by LPA 0-3) and to any one of four registers at each address. The state of the CPU registers are defined by the state of LIC1 and LIC2:

LIC2	LIC1	Register	Function
H	H	R4	All DMA except last byte
H	L	R5	Command
L	H	R6	Last byte of DMA
L	L	R7	SA test



NOTES: t = 0 = 250 milliseconds after drive motor starts, or 20 milliseconds after step command, or 100 μ seconds after termination of write busy, (whichever is the latest time)

Figure 8-7. Read Timing Diagram

8-85. Address and register information is guaranteed valid while LIOSB is low or, in other words, LIOSB is the I/O bus clock. U36 causes LMYPA to go low whenever peripheral address 4 is addressed. If the access is a write to R5 (a command) the data is clocked into U10 and U24 (PCMD) via U45. A write to R7 (used only for SA testing) enables U14. Through U45, a write to any register other than R7 (DMA or command) enables U23 and U38. Whereas, a read from R4 or R6 (DMA) reads data from U22 and U37 (LRD).

8-86. U10B enables DMA upon command through R5 (PCMD). HDMAEN allows U9B to be set on the rising edge of HDMARQ from the state machine output U41. This generates a DMA request through U9B and U43C. An access through R6 (LR6), the last byte of DMA, clears the enable. This in turn, generates an interrupt (LIR3) through U6C, U34B, U44A,B and U43A indicating the end of a DMA cycle.

8-87. U26, U32 U42 and U41 comprise the controller state machine. U26 and U41, used to syncronize the state machine, are clocked by the normal and inverted outputs of a 2 MHz clock which runs asynchronously to the CPU clock. U32 and U42 are programmed ROMs. The purpose of the state machine is to interface between the CPU's 16 bit I/O bus and control bus, to U4's 8 bit bus. The state machine provides packing and and unpacking of words into bytes thru the Mini Disc Controller internal registers when required (during DMA), and passing single bytes through without waiting for a second byte during commands.

8-88. U39 and U40 form a data control register. One example of this registers operation is as follows: During a read operation the Mini Disc Controller U4 is reading data from disc 0 and needs to write to disc 1 after its read routine is executed. First, the disc 0 drive operating conditions will be captured by the control latch U39. Then, the MDC will execute a read on disc 0. After the read is done the control latch is loaded with the operating conditions for disc 1 via the data latches. Then, the MDC will execute a write on disc 1. The drive control buffer U40 is used for determining drive status and to provide a return path for SA stimulus.

8-89. U24, U25 and U10 form a drive status register that informs the system if the drives are operating, media has changed, write protected, requesting DMA, or the MDC, U4, has generated an interrupt.

8-90. U35 the DMA/CPU address selector is used to generate control signals for the internal data register of the Mini Disc Controller, U4.

8-91. U50 is used to detect that there is media in the drives and that the motor is turning. Index pulses will occur every 200 mS, which will keep the monostables retriggered. U51 detects a media change by monitoring the write protect switch.

8-92. U13, U1 and U3 are the final interface to the disc drives. Control and data signals are sent to U13 and U3 from U4 and control latch, U39. Status information from the drives is multiplexed by U1. The reason for multiplexing this information is that the Mini Drive Controller is designed for single drive operation.

8-93. The control board clock generation is done by the circuitry surrounding Y1, a 4 MHz crystal oscillator. R27, R28 and R29 bias U47C,D so the chip will operate in the linear region if the crystal is not oscillating. The crystal oscillates in the series-resonant mode.

8-94. MINI CONTROL DATA SEPARATOR.
(See service sheet 11C figure 8-13)

8-95. Due to the encoding scheme used, data from the disc drive consists of a train of pulses whose pulse-to-pulse spacing may be 4uS, 6uS or 8uS. In practice, up to 200nS of jitter may exist around these nominal values. The function of the data separation circuitry is to recover a clock from this data stream. Each block of data to be recovered is proceeded by a sync field consisting of 96 pulses spaced at 4uS (12 bytes of 0's).

8-96. U29 and U43B detect the presence of the sync field in the following manner: U29B counts a 2 MHz clock so if 5uS or more elapses between sent pulses on pin 12, U29A will be reset by U43B. Since the sync field pulses occur at a nominal 4uS, U29A will count sync field pulses and QD will present a positive edge to U30 after 8, 24, 40, 56 pulses. U30 QB and QD will transition from low to high after 24 (3 bytes) and 56 (7 bytes) pulses respectively. After U4 has recognized four bytes of the sync field, it will set HRG high which will prevent U30 from being reset by the inter-pulse spaces of 6uS and 8uS which will occur in the data. However, HRG will be reset if an address mark is not found in 16 bytes or if the head is in the incorrect position.

8-97. U17, U18, U19, U11, U12 and U31 comprise a phase locked loop. U31, the VCO, runs at a nominal 500KHz. When no data is being inspected off the disc, the PLL is locked to a 500KHz reference in order to keep the loop in its active region. The DC voltage at TP1 should be within +- 2V of ground under these conditions.

8-98. U18 is responsible for three operations. First, when no data is being inspected it will lock the VCO, U31, to the 500KHz reference signal. Second, after U30 QB goes high U18 will lock the VCO to the 250KHz signal while inspection is done of the sync field. Last, when U30 QD goes high the VCO is locked to the 4uS, 6uS, or 8uS data pulses.

8-99. U20, U21, and U17 cause an in phase switch between the 500KHz reference and the sync field (these signals have a random phase relationship). Assume that U30 QB has just gone high: The next time U17 pin 9 transitions low, U20A will be clocked true. This will lock U17 pins 9 and 5 low (the PLL will be locked to the reference) and stop the VCO, U31. The second sync pulse which occurs after this will clock U21 true which will switch U18. Then, the sync field is presented to the PLL and the VCO is restarted in phase. The second sync pulse is the one necessary to insure that both halves of U31 have timed out before they are restarted.

8-100. U27A moves the data transition, either 1-0 or 0-1, to the center of each half bit cell. U27B then sets the data transition pulse width for U4.

8-101. The +12V motor supply is provided by VR1, a voltage regulator, that uses the +17V supply and converts it to +12V. R25 and R26 provide the output voltage adjustment. CR3 and CR4 are used for protection to prevent C26 and C27, filter capacitors, from discharging through low current points in the regulator. +12V motor, +5V, and GND are distributed to the drives through J1 and J2.

8-102. MINI DRIVE THEORY OF OPERATION.

8-103. There is no theory-of-operation on the flexible disc drives at this time.

8-104. TROUBLESHOOTING.

8-105. This section contains troubleshooting information for the Flexible Disc Drive System when installed in the 64100A Logic Development Station. Contained are descriptions of each of the eight PV tests, descriptions of the PV error codes, the use of signature analysis, and service sheet layout.

8-106. PERFORMANCE VERIFICATION (PV) TEST DESCRIPTIONS (see paragraphs 8-108 thru 8-123).

8-107. The following is a description of each of the eight tests performed during a single performance verification (PV) test cycle.

8-108. FLOPPY CONTROLLER RESPONSE TEST.

8-109. During this test the CPU writes AA hex to the track register in the Mini Disc Controller chip and then reads it back and compares it. If this test fails Error message 14 (NO RESPONSE FROM DISC CONTROLLER) is displayed.

8-110. SELECT TEST.
(SELECT will be in inverse video)

8-111. This test selects the drive to be tested, turns ON the motor and checks for drive ready indication from the drive. If this test fails error message 1 (... DISC DOWN...) will be displayed.

8-112. TRACK 00 TEST.
(TRK 00 will be in inverse video)

8-113. This test issues a restore command to the drive and checks for the TRACK 00 indicator line to be active over track 0 and inactive over track 1. If this test fails error messages 2, 3, or 4 may be displayed. These are:

```
TRACK 00 INDICATOR ON OVER TRACK XX
TRACK 00 INDICATOR NOT ON OVER TRACK 0
TRACK 0 NOT FOUND
```

8-114. READ TRACK 0 TEST.
(RTRK0 will be in inverse video)

8-115. This test reads all 16 sectors of track 0 on both sides of the disc. The possible error messages generated are message 1, 5, 6, ,7, 8 and 9. These are:

```
...DISC DOWN...
LOST DATA:              TRK XX SEC XX SIDE X-R/W
DATA CRC ERROR:         TRK XX SEC XX SIDE X-R/W
ID CRC ERROR:           TRK XX SEC XX SIDE X-R/W
RECORD NOT FOUND:       TRK XX SEC XX SIDE X-R/W
SEEK ERROR:             TRK XX NOT VERIFIED
```

8-116. READ TRACK 34 TEST.
(RTRK34 will be in inverse video)

8-117. This test reads all 16 sectors of track 34 on both sides of the disc. The possible error messages generated are message 1, 5, 6, 7, 8 and 9. These are:

```
...DISC DOWN...
LOST DATA:                TRK XX SEC XX SIDE X-R/W
DATA CRC ERROR:           TRK XX SEC XX SIDE X-R/W
ID CRC ERROR:             TRK XX SEC XX SIDE X-R/W
RECORD NOT FOUND:         TRK XX SEC XX SIDE X-R/W
SEEK ERROR:               TRK XX NOT VERIFIED
```

8-118. TRACK 34 CHECK TEST.
(The first READ after TRK 34: will be in inverse video)

8-119. This test checks track 34 to determine if it has been used. This is done by reading the data on track 34, sector 0 on both sides. If the track is not used the data read will be all zeros. The possible error messages are 1, 5, 6, 7, 8, 9, 11, and 12. These are:

```
...DISC DOWN...
LOST DATA:                TRK XX SEC XX SIDE X-R/W
DATA CRC ERROR:           TRK XX SEC XX SIDE X-R/W
ID CRC ERROR:             TRK XX SEC XX SIDE X-R/W
RECORD NOT FOUND:         TRK XX SEC XX SIDE X-R/W
SEEK ERROR:               TRK XX NOT VERIFIED
READ KNOWN DATA ERROR:    SIDE X
NO DISC SPACE AVAILABLE FOR WRITE TEST
```

8-120. TRACK 34 WRITE TEST.
(The WRITE after TRK 34: will be in inverse video)

8-121. This test writes to track 34 sector 1 on both sides of the disc. The error messages that can be generated are 1, 5, 6, 7, 8, 9, and 10. These are:

```
...DISC DOWN...
LOST DATA:                TRK XX SEC XX SIDE X-R/W
DATA CRC ERROR:           TRK XX SEC XX SIDE X-R/W
ID CRC ERROR:             TRK XX SEC XX SIDE X-R/W
RECORD NOT FOUND:         TRK XX SEC XX SIDE X-R/W
SEEK ERROR:               TRK XX NOT VERIFIED
NO WRITE--DISC PROTECTED
```

8-122. TRACK 34 READ/VERIFY WRITE.
(The second READ after TRK 34: will be in inverse video)

8-123. This test reads the data written in the previous test and verifies that it is the same as the data written. The error messages that can be generated are 1, 5, 6, 7, 8, 9, and 13. These are:

```
...DISC DOWN...
LOST DATA:                TRK XX SEC XX SIDE X-R/W
DATA CRC ERROR:           TRK XX SEC XX SIDE X-R/W
ID CRC ERROR:             TRK XX SEC XX SIDE X-R/W
RECORD NOT FOUND:         TRK XX SEC XX SIDE X-R/W
SEEK ERROR:               TRK XX NOT VERIFIED
WRITE ERROR:  SIDE X
```

8-124. PV ERROR MESSAGES.

8-125. While running the floppy PV test an error may be encountered and an error number given. Table 8-1 gives the error number to message conversion.

Table 8-1. Mini Floppy PV Error Messages

ERROR #	ERROR MESSAGE
1	...DISC DOWN...
2	TRACK 00 INDICATOR ON OVER TRACK XX
3	TRACK 00 INDICATOR NOT ON OVER TRACK 0
4	TRACK 0 NOT FOUND
5	LOST DATA: TRK XX SEC XX SIDE X-R/W
6	DATA CRC ERROR: TRK XX SEC XX SIDE X-R/W
7	ID CRC ERROR: TRK XX SEC XX SIDE X-R/W
8	RECORD NOT FOUND: TRK XX SEC XX SIDE X-R/W
9	SEEK ERROR: TRACK XX NOT VERIFIED
10	NO WRITE--DISC WRITE PROTECTED
11	READ KNOWN DATA ERROR: SIDE X
12	NO DISC SPACE AVAILABLE FOR WRITE TEST
13	WRITE ERROR: SIDE X
14	NO RESPONSE FROM DISC CONTROLLER
15	not currently used

When the current test passes a record of previous errors is displayed in the form of an error mask. A "1" is set in each of the bit positions corresponding to the ERROR # of previous errors.

```
                ERROR # ->  15 --------------1
PREVIOUS ERROR MASK:     XXXXXXXXXXXXXXX
```

For example, an error message reads:

```
PASSED    PREV ERRORS: 000000001000001
```

This indicates that the present test passes but during one or more of the previous tests, errors occurred due to the disc being down (ERROR #1) and ID CRC errors (ERROR #7).

8-126. DESCRIPTION OF ERROR CODES AND TROUBLESHOOTING.

8-127. Table 8-2 is a description of each error code in table 8-1. Also, possible troubleshooting and corrective measures are listed.

Table 8-2. Description Of PV Error Codes.

CODE # DESCRIPTION

1 "...DISC DOWN..." This message indicates that the drive ready line of the disc being tested was not read in the true state.

Possible trouble/corrective measure:

a. No media in drive/Insert media and close door.

b. No index pulses from drive or motor not running/Check index pulse circuitry and servo motor.

c. Index pulses but no drive ready indication/Check drive ready circuitry.

d. Drive ready signal true on floppy control board/Check CPU interface with interface DSA loops.

2 "TRACK 00 INDICATOR ON OVER TRACK XX" This message indicates that the MDC was able to verify, by reading the ID portion of the track data, that the head was positioned over track XX. However, the CPU read the TRACK 00 status bit from the Mini Drive Controller (MDC) to be in the true state.

Possible trouble/corrective measures:

a. Go to DIAG mode (see section IV operation verification tests) and select correct drive and step to TRACK XX.

b. TRACK 00 signal is true at input to Mini Controller Chip (MDC)/Troubleshoot TRACK 00 detector circuitry, may have to do TRACK 00 switch adjustment.

c. TRACK 00 signal is false at input to MDC/Troubleshoot CPU interface circuitry with DSA interface loops.

3 "TRACK 00 INDICATOR NOT ON OVER TRACK 0" This message indicates that it was verified by reading the ID portion of the track data, that the head was positioned over track 0 but the CPU read the TRACK00 status bit from the MDC to be in the false state.

Possible trouble/corrective measures:

a. Go to DIAG mode (see section IV operation verification tests) and select correct drive and restore it.

b. TRACK00 signal is false at input to MDC/Troubleshoot track 00 detector circuitry, may have to do a Track 00 switch adjustment.

c. TRACK00 is true at input to MDC/Troubleshoot CPU interface circuitry with DSA interface loops.

4 "TRACK 0 NOT FOUND" This message indicates that after the restore command the CPU read the TRACK00 indicator to be false and that the head was not positioned over track 0.

Possible trouble/corrective measures:

a. Go to DIAG mode (see section IV operation verification tests) and try the RESTORE command for the drive that failed.
b. Bad head positioning circuit/Check step and direction lines from the mini drive controller and stepper motor circuitry.

c. CPU interface to MDC bad/Check interface circuitry using DSA interface loops.

5 "LOST DATA TRK XX SEC XX SIDE X R/W" This message indicates that the CPU did not respond to either an interrupt or a DMA request from the mini drive controller. Also, that the data in the MDC was lost.

Possible trouble/corrective measures:

a. CPU interface to MDC is bad/Check interface circuitry using DSA interface loops.

b. DMA path to CPU bad/Check using logic probe or ohmmeter.

c. Mainframe interrupt circuitry bad/Troubleshoot with DSA in mainframe I/O write test.

6 "DATA CRC TRK XX SEC XX SIDE X R" This message is generated when the mini drive controller chip detects a CRC error in the data portion of a sector read operation.

Possible trouble/corrective measures:

a. Bad media/Reformat a new disc and repeat test.

b. Data separator circuit bad/Check using DSA data separator loops.

c. Bad drive read electronics/Check read data waveforms with the ones shown in the drive and drive head alignment procedures. See radial head alignment procedure in Section V, paragraph 5-19.

7 "ID CRC TRK XX SEC XX SIDE X R/W" When this message is generated the MDC chip has detected a CRC error in the ID portion of a sector read operation.

Possible trouble/corrective measure:

a. Same as trouble/corrective measures used in code 6 above.

8 "RECORD NOT FOUND TRK XX SEC XX SIDE X R/W" This message is generated when the code for the desired track, sector, and side were not found on the current track in any of the ID fields.

Possible trouble/corrective measure:

a. Bad media/Reformat a new disc and repeat test.

b. Data separator circuit bad/Check using DSA data separator loops.

c. Bad Drive Electronics/Check the read data waveforms with the waveforms given in the drive and drive head alignment procedures given in Section V.

d. Bad head positioning circuit/Check the step and direction lines from the mini drive controller and stepper motor circuitry.

9 "SEEK ERROR: TRK XX NOT VERIFIED" When this message is generated the code for the desired track is not found in the ID field.

Possible trouble/corrective measure:

a. The trouble and corrective measures are the same as code 8 above.

10 "NO WRITE DISC WRITE PROTECTED" This message is generated when the CPU reads the write protect line (through the activity register) for the selected drive in the true state during a write operation.

Possible trouble/corrective measure:

a. Disc write protected/Use disc that is not write protected.

b. The write protect signal is true when the disc is not write protected/Troubleshoot the write protect circuitry.

c. Write protect line operates correctly, but, the CPU interface is bad/Check CPU interface using DSA with activity buffer moved to mode buffer location.

11 "READ KNOWN DATA ERROR: SIDE X" When the data read on track 34, during the track 34 check, is not all zeros then an error is displayed.

Possible trouble/corrective measure:

a. Bad media/Reformat a new disc and perform test again.

b. Data separator circuit bad/Check using DSA data separator loops.

c. Bad drive read electronics/Check the read data waveforms with the waveforms given in the drive and head alignment procedures given in Section V.

d. Bad head positioning circuit/Check step and direction lines from the mini drive controller and stepper motor circuitry.

12 "NO DISC SPACE AVAILABLE FOR WRITE TEST" This message is generated when the first byte of data read on track 34, during the track 34 check, is not all zeros.

Possible trouble/corrective measure:

a. The trouble and corrective measures are the same as code 11 above.

13 "WRITE ERROR: SIDE X" When the data written to track 34 during the track 34 write test does not match the data read back during the track 34 read/verify test this message will be generated.

Possible trouble/corrective measure:

a. Bad media/reformat a new disc and perform the test again.

b. Bad write circuitry/check write gate, write data, and write protect signals to the MDC and the write waveforms to the drive units.

14 "NO RESPONSE FROM DISC CONTROLLER" This message is generated when the CPU cannot write 55 Hex to the track register in the Mini Drive Controller and read it back correctly.

Possible trouble/corrective measure:

a. CPU interface to MDC bad/check interface circuitry using DSA interface loops.

8-128. TROUBLESHOOTING USING SIGNATURE ANALYSIS (SA).

8-129. Signature analysis may be used to troubleshoot the Mini Control board to component level. Signature analysis is a technique that enables the signature analyzer to display a compressed, four digit "fingerprint" or signature of the data stream at a given node. Any fault associated with a device on that node will force a change in the data stream and, therefore, result in an erroneous signature.

8-130. Do the following when troubleshooting the flexible disc drive system: first, configure the Rear-Panel switches to the PV mode or press CONTROL/RESET simultaneously (figure 4-1 should appear); second, press the DIAG softkey figure 4-2 should appear). This will give access to the floppy disc diagnostic menu. This menu consists of two signature stimulus loops, DSA1 and DSA2. DSA1 starts the CPU interface DSA loop. DSA2 starts the data separator DSA loop. SA tables 86 thru 8-18 are represented by a black letter at a given node that correlates to the letter given with the SA table. For example, Table 8-6, Loop A. The black letter "A" is given on the schematic where loop A signatures can be taken.

8-131. KEY SIGNATURES.

8-132. While using SA on the Floppy Control Board, some of the loops may contain key signatures. Using the key signatures should reduce troubleshooting time. A key signature is indicated with a "+" next to the node on the SA table and will be a red shaded black letter on the service sheet. The key signatures should be checked before doing all of that loop. If the key signatures are good, then the rest of the signatures in that loop are good.

8-133. INTERFACE LOOP.

8-134. The SA tables for the interface loop contain key signatures. However, key signatures in loops A, B and M should be taken first. If all of the key signatures are good, then no more signatures need to be taken in the interface loop. Although, if some of the key signatures in loops A, B and M are wrong, then performing other SA loops may be necessary to fix a problem.

8-135. In the interface loop, SA tables A-J are used to exercise the CPU/MDC interface circuitry. In this loop, test jumper E2 must be in the interface TEST position, XU15. This connects the output of the SA stimulus latch to the inputs of DMA state machine. This allows the CPU to directly control the state machine. Also, the clock for the state machine is connected to LMYPA so that the state machine is clocked only when the CPU communicates with register 4. This makes all interface circuitry synchronous with the CPU and thus allows SA. SA tables A-J are outlined below:

Table A -- Check overall interface

Table B -- Check Floppy ASM

Table M -- Check all Data (I/O Bus) to/from Floppy Controller

Table C -- To check I/O bus decoding

Table D -- Check Data written to Floppy drives

Table E -- Checks Floppy Read Latches

Table F -- Check Data out of U23

Table G -- Check Data from U38

Table H -- Check Data from mode buffer U40

Table I -- Check Data from the MDC (MSB)

Table J -- Check Data from the MDC (LSB) and from U40

8-136. DATA SEPARATOR LOOP.

8-137. In this loop, test jumper E1 must be in the Data Separator TEST position, XU7. This connects the output of the SA latch to the data separator inputs. Also, LMYPA is connected to the L2MHZ input to the data separator. This makes all of the data separator circuitry synchronous to the CPU and thus allows for SA. SA tables K and L are outlined below:

Table K -- Check Data Separator circuitry

Table L -- To check U18 multiplexer to make sure it is multiplexing the HDATA1US signal properly. There are no signature nodes for this loop. just check for correct VH.

8-138. SERVICE SHEET LAYOUT.

8-139. Each service sheet shows the circuitry that controls each of the functional areas listed in table 8-3. Reduced block diagrams and component locators are given with each service sheet. These are gray shaded to correlate the general relationships of the particular circuitry to the overall system.

8-140. MINI CONTROL AND DRIVE SERVICE SHEET LAYOUT.

8-141. The circuitry for the mini control board is shown on service sheets 11A-11C and the circuitry for the mini drives is shown on sheets 1 and 2. Refer to table 8-3 for a list of service sheets and the functional circuitry shown on each sheet.

Table 8-3. Service Sheet To Function

Service Sheet Number		Functions Shown
11A	Figure 8-9	Microprocessor Interface/DMA State Machine
		CPU Decode
		DMA/CPU Address Selector
		Interrupt Circuitry
		DMA Request
		SA Stimulus Latch
		DMA Acknowledge Latch
		Processor Request Latch
		DMA Enable Latch
		Interface Control Latch
		Data Latches
11B	Figure 8-11	¼ MHz Oscillator
		Drive Ready Monostables
		Media Change Latches
		CPU/Drive Interface
		Drive Control Latch and Buffer
		Drive Status Buffer
		Disc Drive Multiplexer and Control Buffering
11C	Figure 8-13	Data Separator Circuitry
		Voltage Controlled Oscillator
		Zero Detection
		Phase Detection
		Drive Power Supply
1	Figure 8-15	Servo Electronics
2	Figure 8-17	Drive Electronics

8-142. LOGIC CONVENTION.

8-143. The positive logic convention is used for the circuits of the 64941A floppy drive option. Positive logic defines a logic 1 as a more positive voltage (high) and a logic 0 as the more negative voltage (low). Ideally, the low and high voltage levels are 0V and +5V, respectively. Actual levels may vary from these ideal values. Therefore, the voltage levels for a logic 1 and 0 are defined as follows:

TTL Voltage Levels

Binary Quantity	Voltage Limit
Input 0	< 0.8 V
Input 1	> 2.0 V
Output 0	< 0.4 V
Output 1	> 2.4 V

8-144. LOGIC SYMBOLOGY.

8-145. Table 8-4 gives a summary of the logic symbology used in this manual.

Table 8-4. Logic Symbology

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term.)

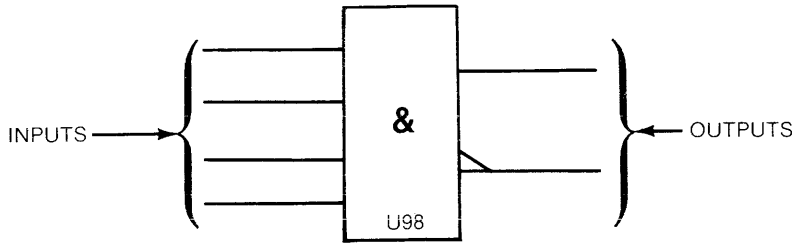
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

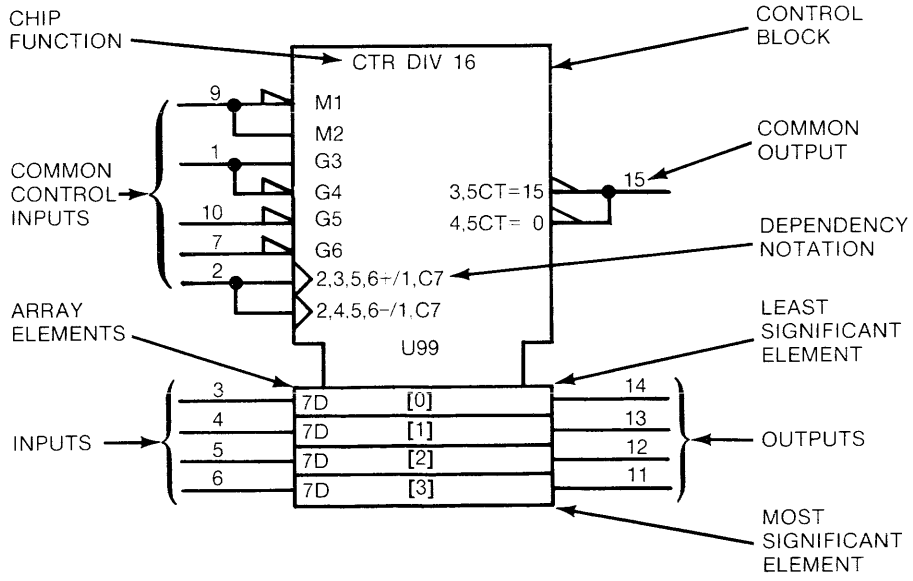
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. Unless indicated, the least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in **[ ]**).

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Table 8-4. Logic Symbology (Cont'd)

OTHER SYMBOLS

Analog Signal	Inversion	→ Shift Right (or down)
& AND	O Negation	/ Solidus (allows an input or output to have more than one function)
Bit Grouping	Nonlogic Input/Output	▽ Tri-State
Buffer	Open Circuit (external resistor)	, Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.
! Compare	Open Circuit (external resistor)	( ) Used for factoring terms using algebraic techniques.
Dynamic	≥1 OR	[ ] Information not defined.
=1 Exclusive OR	Passive Pull Down (internal resistor)	Φ Logic symbol not defined due to complexity.
Hysteresis	Passive Pull Up (internal resistor)	
? Interrogation	Postponed	
— Internal Connection	← Shift Left (or up)	

LABELS

BG	Borrow Generate	CO	Carry Output	J	J Input
BI	Borrow Input	CP	Carry Propagate	K	K Input
BO	Borrow Output	CT	Content	P	Operand
BP	Borrow Propagate	D	Data Input	T	Transition
CG	Carry Generate	E	Extension (input or output)	+	Count Up
CI	Carry Input	F	Function	–	Count Down

MATH FUNCTIONS

Σ	Adder	>	Greater Than
ALU	Arithmetic Logic Unit	<	Less Than
COMP	Comparator	CPG	Look Ahead Carry Generator
DIV	Divide By	π	Multiplier
=	Equal To	P-Q	Subtractor

CHIP FUNCTIONS

BCD	Binary Coded Decimal	DIR	Directional	RAM	Random Access Memory
BIN	Binary	DMUX	Demultiplexer	RCVR	Line Receiver
BUF	Buffer	FF	Flip-Flop	ROM	Read Only Memory
CTR	Counter	MUX	Multiplexer	SEG	Segment
DEC	Decimal	OCT	Octal	SRG	Shift Register

DELAY and MULTIVIBRATORS

	Astable
100 ns	Delay
1	Nonretriggerable Monostable
NV	Nonvolatile
	Retriggerable Monostable

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8-146. MNEMONICS.

8-147. Signals in the 64941A flexible disc drive option have been assigned mnemonics that describe the active state and function of the signal (see table 8-4). A prefix letter (H, L, P, or N) is used to indicate the active state of the signal and the remaining letters indicate its function A "H" prefix indicates that the function is active in the "high" state; a "L" prefix indicates that the function is active in the "low" state; a "P" prefix indicates the clock signal is active on the positive edge of the clock; a "N" indicates the clock is active on the negative edge of the clock. Table 8-5 is a listing of the mnemonics used on the service sheets.

Table 8-5. Mnemonics

MNEMONIC	DESCRIPTION
DS0-3	Drive Select 0 through 3. When low, the drive is selected and will respond to step or read/write commands. This system uses DS0 only.
HA 0-1	High Address 0-1. These inputs in conjunction with the chip select and write inputs select between the status register, track register, sector register, data register and command registers internal to the Mini Disc Controller chip.
HBYTE 3	High Byte 3. When true, this signal indicates that three consecutive bytes of zeros or ones have been received from the disc.
HBYTE 7	High Byte 7. When true, this signal indicates that seven consecutive bytes of zeros or ones have been received from the Flexible Disc Drive electronics.
HDATA1US	High Data 1 Microsecond. This signal pulses true for 1 microsecond whenever a flux transition is detected from the disc drive.
HDIRC	High Direction. When high the heads are stepped out (away from center) and when low the heads are stepped in with each step pulse.
HDMAEN	High DMA Enable. This signal is set true by the CPU when it is ready for a DMA operation. This signal is set to the false state when the DMA operation is completed.

Table 8-5. Mnemonics (Cont'd)

MNEMONIC	DESCRIPTION
HDMARQ	High DMA Request. Signal from CPU Interface/DMA state machine that indicates that the Mini Disc Controller chip is requesting a DMA cycle.
HDRQ	High Data Request. When high, indicates that the Mini Disc Controller's data register is full, if a read operation is occurring, or empty during a write operation. This line is cleared when the CPU does a read or write to the data register.
HINHIBIT	High Inhibit. Signal in data separator circuitry which halts the VCO during a sink-up cycle. When this signal goes to the false state, the VCO is again started in phase with incoming data.
HMDCRQ	High Mini Disc Controller Request. HMDCRQ is a signal from Mini disc Controller chip which, when true, indicates that the Mini Disc Controller chip wishes to interrupt the CPU operation.
HR5,6	High Register 5, 6. When in the true state indicates that the CPU is communicating with the Mini Disc Controller via either register 5 or register 6 internal to the CPU. The state of the registers is determined by LIC1 and LIC2.
HRCLK	High Read Clock. Clock signal from data separator circuitry which is in phase with the LRAWRD signal.
HRG	High Read Gate. Signal from the Mini Disc Controller chip which indicates to the data separator circuitry that a field of zeros or ones has been encountered. When true, it does not allow the data separator to re-synchronize.
HSA D0-7	High Signature Analysis Data 0-7. These signals are the outputs of the SA stimulus latch. The lower byte of the LIOD (0-7) bus is used by the CPU to make the interface and data separator circuitry synchronous with the CPU.
HVCOE	High Voltage Control Oscillator Enable. Complement of LVCOE.

Table 8-5. Mnemonics (Cont'd)

MNEMONICS	DESCRIPTION
H2MHZC	High 2 MHz Clock. The inverted 2 MHz clock used to clock data from the output of the state machine.
LA0-2	Low Address 0-2. Address bits from CPU which are used to select the address of the Mini Disc Controller chip or other registers in which read and write operations are to occur.
LBEN	Low Buffer Enable. When low, this signal enables the drive status buffers and also resets the processor request flip-flop.
LCS	Low Chip Select. Input signal from the CPU which enables the Mini Disc Controller chip.
LCRMC0,1	Low Clear Media Change 0, 1. These signals clear their respective media change flip-flops, and are controlled by the CPU.
LDAL 0-7	Low Data Access Lines 0-7 Bi directional lines that carry data and commands to and from the Mini Disc Controller chip, drive status register, etc.
LDMAAK	Low DMA Acknowledge. Signal to the CPU interface state machine which indicates that the DMA request from the Mini Disc Controller has been acknowledged.
LDMAEN	Low DMA Enable. Complement of HDMAEN.
LDMAI	Low Direct Memory Access Interrupt. An interrupt to the CPU when the MDC is requesting DMA and LDMAEN is not true.
LDMAR	Low Direct Memory Access Request. When low, indicates to the CPU that the MDC wants direct access to memory.
LDOUT	Low Data Out. Signal from CPU which indicates read or write operation on the I/O bus (Low = Write). This is valid when LIOSB is low.

Table 8-5. Mnemonics (Cont'd)

MNEMONIC	DESCRIPTION
LDRQ	Low Data Request. Complement of HDRQ.
LIC1-2	Low Interface Control 1 and 2. These lines can provide up to four states used to control peripheral devices. How these lines are controlled is determined by software.
LINT	Low Interrupt. The microprocessor pulls this line low to poll the Input/Output Bus to determine which peripheral device requested the interrupt.
LIOD0-15	Low Input/Output Data 0 through 15. The LIOD bus is a bi-directional bus. The CPU uses this bus to communicate with I/O ports. Information is low true, and is used in conjunction with LPAB0-3.
LIOSB	Low Input/Output Strobe. When this signal goes from low to high, the data on the I/O bus is valid.
LIR3	Low Interrupt Request 3. Interrupt request from Mini Controller board to the interrupt circuitry on the I/O board that the mini controller is in need of service by the CPU.
LLL	Low Latch Least. Signal from CPU interface state machine which latches the least significant byte of data during a CPU read cycle.
LLM	Low Latch Most. Signal from CPU interface state machine which latches the most significant byte of data during a CPU read cycle.
LMDCI	Low Mini Disc Controller Chip Interrupt. Flag signal to CPU that indicates that the Mini Disc Controller chip is currently requesting an interrupt.
LMCIR	Low Media Change Interrupt Request. Interrupt signal from media change flip-flops indicating that media has been changed on the disc.
LMDCHG0,1	Low Media Change 0,1. When low, the corresponding signal indicates that the media has been changed on the appropriate disc.

Table 8-5. Mnemonics (Cont'd)

MNEMONICS	DESCRIPTION
LMR	Low Master Reset. Input to the Mini Disc Controller chip, when true, resets internal status registers.
LMDCRQ	Low Mini Disc Controller Request. Complement of HMDCRQ.
LMYPA	Low My Peripheral Address. Goes low when the CPU is communicating with the mini drive circuitry. This signal is formed when Peripheral Address 4 is accessed by the CPU. Also, LMYPA is used as the clock during SA.
LNTRDY0,1	Low Not Ready 0,1 When true, these signals indicate that the corresponding disc drive is not ready, i.e, index pulses have dropped below a specified rate.
LOEL	Low Output Enable Lower. When true, this signal enables the least significant 8 bits of data to appear on the disc interface bus during a microprocessor write cycle.
LOEM	Low Output Enable Most. When true, this signal enables the 8 most significant bits to the disc interface bus during a microprocessor write cycle.
LPOP	Low Power On Pulse. This signal pulses low when power is cycled. When pulsed low, it will initialize and reset the CPU and mini drive control circuitry.
LPOPB	Low Power On Pulse Buffered. When low, resets drive and interface control latches.
LPA0-3	Low Peripheral Address 0 through 3. Identifies which one of the 16 peripheral devices will be involved in a I/O operation.
LPRQ	Low Processor Request. When true, this signal indicates that the CPU is requesting a cycle from the the CPU interface/DMA state machine.
LRAWRD	Low Raw Read. Signal which enables a read data cycle from the data separator circuitry and is in phase with HRCLK.

Table 8-5. Mnemonics (Cont'd)

MNEMONICS	DESCRIPTION
LR7	Low Register 7. When true, this signal indicates that the CPU is communicating on the I/O bus through register 7.
LRDDATA	Low Read Data. When true, indicates to the data separation circuitry that a flux transition has occurred on the disc.
LRD	Low Read. When true, this signal indicates that the microprocessor is executing a read cycle from the Mini Disc Control circuitry through the data latches.
LRST	Low Reset. Signal from the microprocessor which resets the Mini Disc Controller circuits.
LRSTINT	Low Reset Interrupt. Signal from the microprocessor. When true, it resets the Mini Disc Controller chip interrupts and DMA interrupt request flip-flops.
LVCO	Low Voltage Control Oscillator. Low true output of VCO oscillator.
LVCOE	Low Voltage Control Oscillator Enable. Signal from Mini Disc Controller chip which is made true when the Mini Disc Controller is inspecting data coming from the disc. When true, enables data separator circuitry.
LWE	Low Write Enable. Signal to Mini Disc Controller chip which enables write circuitry in conjunction with Low Chip Select (LCS).
LWRT	Low Write. When true, corresponding signal indicates that the CPU is executing a write to the mini disc circuitry through the data latches.
LWRTSM	Low Write State Machine. Signal from microprocessor which indicates whether a read or write operation should be executed during the next CPU/DMA state machine interface cycle.
LWPRT0,1	Low Write Protect 0,1. When true, corresponding signal indicates that the disc installed in the disc drive is write protected. See Write Protect. Also, used to set corresponding media change flip-flop.

Table 8-5. Mnemonics (Cont'd)

MNEMONICS	DESCRIPTION
LRE	Low Read Enable. Input to Mini Disc Controller chip which enables read circuitry in conjunction with Low Chip Select (LCS).
L2MHZ	Low 2 MHz. 2 MHz signal derived from the 4 MHz oscillator circuit.
L2MHZC	Low 2 MHz Clock. Used to clock data to the input of the state machine.
L500KHz	Low 500 KHz. A 500 KHz signal derived from the 4MHz oscillator circuit. This signal is used by the Phase Lock Loop (PLL) to sync the VCO while inspecting data from the disc.
PCMD	Positive Command. Control signal from the CPU which pulses low during a write to the mini disc through register 5. The positive edge of this signal latches data into the interface control latch and the DMA enable latch and sets the processor request latch.
VCODATA	Voltage Controlled Oscillator Data. This signal is compared with VCOOSC in the phase comparator circuitry.
VCOOSC	Voltage Control Oscillator. This signal is compared with VCODATA in phase comparator circuit.
HIGH DECREASE FVCO	Signal from phase detector. When true, decreases the frequency of the Voltage Control Oscillator (VCO).
LOW INCREASE FVCO	When in the true state, this signal changes the voltage to the Voltage Control Oscillator in such a way as to increase its frequency.
INDEX	An index pulse occurs once every revolution of the disc (200 milli sec. nominal) to indicate the beginning of a track.
MOTOR ON	A low logic level on this line causes the drive motor to accelerate and stabilize in less than 250 milli sec. When this line goes high, the drive motor decelerates to a stop.

Table 8-5. Mnemonics (Cont'd)

MNEMONICS	DESCRIPTION
SIDE ONE SELECT	A high logic level selects the side "0" read/write head and a low logic level selects the side "1" read/write head.
STEP	Pulses low to step the head in or out. Direction is controlled by HDIRC.
TRACK0	This line indicates to the controller that the read/write head is positioned on track 0. The track 0 signal remains low until the head is moved from track 0. This is accomplished by ANDing the track 0 switch and phase 0 of the stepper motor control.
WRITE DATA	When the disc drive is selected, this line provides the bit serial composite write data pulses that control the switching of the write current in the selected head. The write electronics must be enabled by the write gate line.
WRITE GATE	When this line is low, the write electronics are enabled for writing data (read electronics are disabled). This line enables write current to flow in the selected read/write head
WRITE PROTECT	This line goes low when the disc is write protected to disable the write electronics.

8-148. TROUBLESHOOTING HINTS.

8-149. The following are some things to check before troubleshooting the Mini Control board.

a. Make sure the clocks on U26 pin 11 and U41 pin 11 are clocking at 2MHz.

b. Check that U36 pin 12 (LMYPA) is toggling. This indicates that the CPU is working and communicating with the Mini Disc Controller.

c. The CPU will not work at all if LIR3 or LDMAR are pulled low at the wrong time. U43 may be removed to disable these signals.

d. To isolate a problem to a drive, swap the drive control cables (A9W1 and A10W1) and see if the symptom changes from one drive to the other.

e. If both drives fail, the problem is probably on the Mini Control board.

f. If the problem is on the Mini Control board (A11) and no bad signatures are found, and the data separator is good then check the signals that go between the Mini Disc Control (MDC U4) and the drives using diagnostic mode (DIAG).

g. Test STEP and RESTORE commands before a READ or WRITE to disc. These require that a lot less circuitry be functional.

h. The phase detector U19 locks the NEGATIVE transitions of "VCO Data" and "VCO OSC" together.

i. For a simple analysis, consider U12 to be an integrator.

j. Check that the VCO will lock to the 500KHz reference record.

8-150. To completely check the Data Separator Circuitry perform the following checks in the order given:

1) Set-up SA loop K and check the following key signatures:

U11-1 7CA3
U11-2 7CA3
U11-6 55AP
U11-7 55AP

IF FAILURE - Use SA loop K to isolate problem.

2) Set-up SA loop L and check the following:

VH = 72A2

IF FAILURE - Check for 1uS pulses on U18 pins 11 and 13. If good then replace U18.

Waveform at TP1 is correct. (schematic 11C).

IF FAILURE - Check components in Intergrator and Phase Detector circuits. (schematic 11C)

Pulse width (low) at TP4 (U27A pin 4) is 1uS +-50nS.

IF FAILURE - Check U27A, R20 and C33.

Pulse width (high) at U4 pin 27 is 170nS +-20nS.

IF FAILURE - Check U27B, R21 and C34.

3) Return instrument to normal operating configuration and check for 2MHz square wave (period 500nS +-25nS) at U29B pin 13 and for 500KHz square wave (period 2uS +-100nS) at U17 pin 13.

IF FAILURE - Check oscillator circuit on schematic 11B.

4) Short TP1 to ground and check TP5 for a period of 1.9uS +-100nS with asymmetry less than 5% and U4 pin 26 for 250KHz square wave.

IF FAILURE - Check U31A,B, R10,11,22,23, C15 and C20.

8-151. The following are some specification that should be tested before troubleshooting.

a.	U4 pin 24	1MHz +-1% square wave
b.	U50 pins 5 and 13	225mS <= PW <= 300mS
c.	U27 pin 13 U27 pin 12	1uS +- 50nS 150nS <= PW <= 190nS
d.	U31 pin 4 U31 pin 13 with TP1 grounded	period = 2uS +- 100nS asymmetry of square wave <= 5%
e.	TP1 PLL locked to 500KHz reference	+-2V of ground

Table 8-6. SA Loop A

INTERFACE LOOP-A

PC BOARD: 64941-66501 Floppy Control

CIRCUITRY TESTED: Overall Interface

PROCEDURE: Remove U25 mode buffer (U25 can be tested by exchanging with U40). Remove all option boards. Move E2 TEST jumper to interface TEST position in XU15. Press DSA 1 soft key to initiate test.

SETUP:
CLOCK - neg. edge TP9 (LMYPA)
START - neg. edge TP6 (SA GATE)
STOP - pos. edge TP6 (SA GATE)
VH - PCP5
+ - KEY SIGNATURE
! - This signature is with drive 1 connected.
% - This signature is with drive 0 connected.

U 1- 1	FHP9	U 9- 1	UC35	U 15- 1	5U1F	U 16-17	559F +
		U 9- 2	PCP5	U 15- 2	1199	U 16-18	H50F +
U 3- 1	FHP9	U 9- 3	PCP5	U 15- 3	12HU	U 16-19	H42F +
U 3- 3	FHP9 +	U 9- 4	PCP5	U 15- 4	P57A	U 16-20	2C8P +
U 3- 7	2603 +	U 9- 6	10H0	U 15- 5	P6CC		
U 3-13	FHP6	U 9- 8	PCP5	U 15- 6	C4PA	U 22- 1	PCP5
U 3-14	0000 +/FHP9 +!	U 9-11	UC35 +	U 15- 7	7U1F	U 22- 3	059F +
U 3-17	260F	U 9-12	5430 +	U 15- 8	P943	U 22- 4	059F +
		U 9-13	PCP5	U 15- 9	PCP5	U 22- 7	H700 +
U 4- 2	C6F7			U 15-10	0000	U 22- 8	H700 +
U 4- 3	CH09	U 10- 1	588P	U 15-11	0000	U 22-11	PU2A
U 4- 4	H180	U 10- 3	PCP5	U 15-12	PCP5	U 22-13	4F81 +
U 4- 5	CU94	U 10- 6	FU75	U 15-13	P943	U 22-14	9P1H +
U 4- 6	5944	U 10- 8	5430	U 15-14	7U1F	U 22-17	C8H3 +
U 4- 7	H700 +	U 10- 9	CUH5	U 15-15	C4PA	U 22-18	9P1H +
U 4- 8	9P1H +	U 10-10	PCP5	U 15-16	P6CC		
U 4- 9	H700 +	U 10-11	PCP5	U 15-17	P57A	U 23- 1	1UFH
U 4-10	C8H3 +	U 10-13	PCP5	U 15-18	12HU	U 23- 2	059F
U 4-11	059F +			U 15-19	1199	U 23- 5	059F
U 4-12	9P1H +	U 13- 1	2603	U 15-20	5U1F	U 23- 6	H700
U 4-13	059F +	U 13- 3	FHP9 +			U 23- 9	H700
U 4-14	4F81 +	U 13- 7	FHP9 +	U 16- 1	5U1F	U 23-11	PCP5
U 4-19	PCP5	U 13-12	0000/2603 %	U 16- 2	1199	U 23-12	4F81
U 4-38	0000	U 13-13	260F	U 16- 3	12HU	U 23-15	9P1H
U 4-39	2814	U 13-17	260F	U 16- 4	P57A	U 23-16	C8H3
				U 16- 5	P6CC	U 23-19	9P1H
U 6- 1	0000	U 14- 1	248A	U 16- 6	C4PA		
U 6- 2	AHA7	U 14- 2	5U1F	U 16- 7	7U1F	U 24- 2	C215
U 6- 3	PCP5	U 14- 5	12HU	U 16- 8	P943	U 24- 5	PCP5
U 6- 4	559F	U 14- 6	P6CC	U 16- 9	PCP5	U 24- 6	7316
U 6- 5	CUH5	U 14- 9	7U1F	U 16-10	0000	U 24- 9	FUU2
U 6- 6	AHA7	U 14-11	PCP5	U 16-11	PCP5 +	U 24-11	PCP5
U 6- 8	10H0	U 14-12	P943	U 16-13	FU75 +	U 24-12	19A1
U 6- 9	CUH5	U 14-15	C4PA	U 16-14	5F17 +	U 24-15	0000
U 6-10	UC35	U 14-16	P57A	U 16-15	PCP5 +	U 24-16	6PH0
U 6-11	080F	U 14-19	1199	U 16-16	10H0 +	U 24-19	2922
U 6-12	3A65						
U 6-13	CH09						

Table 8-6. SA Loop A (Cont'd)

U 25- 1	588P +	U 32-11	H42F	U 37- 8	H700 +	U 41- 3	8H32
U 25- 3	H700	U 32-12	2C8P	U 37-11	6624	U 41- 4	U66C
U 25- 5	H700	U 32-13	0000	U 37-13	4F81 +	U 41- 5	UC35
U 25- 6	FHP9 +	U 32-14	0000	U 37-14	9P1H +	U 41- 6	C6F7
U 25- 7	059F	U 32-15	PAC6	U 37-17	C8H3 +	U 41- 7	51A1
U 25- 8	6UF8 +			U 37-18	9P1H +	U 41- 8	9U2U
U 25- 9	059F	U 33- 1	0000			U 41- 9	H180
U 25-11	CFCA +	U 33- 2	2814	U 38- 1	AHU4	U 41-11	0000
U 25-12	4F81	U 33- 3	0000	U 38- 2	059F	U 41-12	PU2A
		U 33- 4	277U	U 38- 5	059F	U 41-13	P27A
U 25-14	9P1H	U 33- 5	3A65	U 38- 6	H700	U 41-14	03C4
U 25-15	2603 +	U 33- 6	4FC1	U 38- 9	H700	U 41-15	1UFH
U 25-16	C8H3	U 33- 7	0000	U 38-11	PCP5	U 41-16	6624
U 25-18	9P1H	U 33- 8	03U5	U 38-12	4F81	U 41-17	U067
U 25-19	588P +	U 33- 9	0000	U 38-15	9P1H	U 41-18	67F7
		U 33-11	PCP5	U 38-16	C8H3	U 41-19	AHU4
U 26- 1	0000	U 33-12	P810	U 38-17	79H8		
U 26- 2	A199	U 33-13	PCP5			U 42- 1	67F7
U 26- 3	7U1F	U 33-14	A754	U 39- 1	PCP5	U 42- 2	U067
U 26- 4	5U1F	U 33-15	H180	U 39- 2	FHP6	U 42- 3	03C4
U 26- 5	3199	U 33-16	FF9A	U 39- 3	H700 +	U 42- 4	P27A
U 26- 6	88FF	U 33-17	PCP5	U 39- 4	H700 +	U 42- 5	8H32
U 26- 7	1199	U 33-18	F3U1	U 39- 5	FHP6	U 42- 6	U66C
U 26- 8	12HU	U 33-19	0000	U 39- 6	260F	U 42- 7	51A1
U 26- 9	096U			U 39- 7	9P1H +	U 42- 9	9U2U
U 26-11	PCP5	U 34- 1	F3U1	U 39- 8	4F81 +	U 42-10	2C8P
U 26-12	PAC6	U 34- 2	0000	U 39- 9	260F	U 42-11	H42F
U 26-13	P943	U 34- 3	PCP5	U 39-10	0000	U 42-12	H50F
U 26-14	P57A	U 34- 4	PCP5	U 39-11	CHHU	U 42-13	559F
U 26-15	6FAA	U 34- 5	842H	U 39-12	FHP6	U 42-14	0000
U 26-16	PH4A	U 34- 6	6UF8	U 39-13	059F +	U 42-15	0000
U 26-17	P6CC	U 34- 7	CFCA	U 39-14	059F +		
U 26-18	C4PA	U 34- 9	575U	U 39-15	FHP6	U 43- 1	3897 +
U 26-19	4462	U 34-10	PCP5	U 39-16	260F	U 43- 2	000U +
		U 34-11	PCP5	U 39-17	C8H3 +	U 43- 3	000U
U 28- 1	P810	U 34-12	0000	U 39-18	9P1H +	U 43- 8	PCP5 +
U 28- 2	FF9A	U 34-13	10H0	U 39-19	260F	U 43- 9	PCP5
U 28- 3	FF9A	U 34-14	19A1			U 43-10	PCP5
U 28- 4	277U	U 34-15	19A1	U 40- 1	080F		
U 28- 5	277U			U 40- 2	260F	U 44- 1	CFCA +
U 28- 6	PCP5	U 35- 1	559F	U 40- 3	H700	U 44- 2	6UF8 +
U 28- 7	03U5	U 35- 2	PCP5	U 40- 4	260F	U 44- 3	H372
U 28- 9	277U	U 35- 3	FUU2	U 40- 5	H700	U 44- 4	H372
U 28-10	FF9A	U 35- 4	CU94	U 40- 6	260F	U 44- 5	H372
U 28-11	PCP5	U 35- 5	PCP5	U 40- 7	059F	U 44- 6	3897
U 28-12	248A	U 35- 6	2922	U 40- 8	260F		
U 28-13	FF9A	U 35- 7	5944	U 40- 9	059F	U 45- 1	A754
U 28-14	0000	U 35- 9	CH09	U 40-11	FHP6	U 45- 2	277U
U 28-15	0000	U 35-10	7316	U 40-12	4F81	U 45- 3	277U
		U 35-11	0000	U 40-13	FHP6	U 45- 4	PCP5
U 32- 1	A199	U 35-12	5F17	U 40-14	9P1H	U 45- 5	0000
U 32- 2	4462	U 35-13	6PH0	U 40-15	FHP6	U 45- 6	03U5
U 32- 3	PH4A	U 35-14	C215	U 40-16	C8H3	U 45- 7	PCP5
U 32- 4	6FAA	U 35-15	0000	U 40-17	FHP6	U 45- 9	PCP5
U 32- 5	3199			U 40-18	9P1H	U 45-10	248A
U 32- 6	88FF	U 37- 1	PCP5	U 40-19	080F	U 45-11	0000
U 32- 7	096U	U 37- 3	059F +			U 45-12	PCP5
U 32- 9	559F	U 37- 4	059F +	U 41- 1	0000	U 45-13	0000
U 32-10	H50F	U 37- 7	H700 +	U 41- 2	588P	U 45-14	248A

Table 8-6. SA Loop A (Cont'd)

U 45-15 PCP5

U 47- 1 PCP5
U 47- 2 FHP6
U 47- 3 2603 +
U 47- 4 PCP5
U 47- 5 260F
U 47- 6 FHP9 +

U 49- 4 FHP6
U 49- 5 2603
U 49- 6 2603
U 49- 8 FHP9
U 49- 9 FHP9
U 49-10 260F
U 49-11 260F
U 49-12 FHP6

U 49-13 000U

U 51- 1 260F
U 51- 2 PCP5
U 51- 3 PCP5
U 51- 4 0000
U 51- 5 PCP5
U 51- 6 FHP9

U 51- 8 2603
U 51- 9 PCP5
U 51-10 0000
U 51-11 PCP5
U 51-12 PCP5
U 51-13 FHP6

Table 8-7. SA Loop B.

INTERFACE LOOP-B

PC BOARD: 64941-66501 Floppy Control

CIRCUITRY TESTED: Floppy State Machine

PROCEDURE: Remove U25 mode buffer (U25 can be tested by exchanging with U40). Remove all option boards. Move E2 TEST jumper to interface TEST position in XU15. Press DSA 1 soft key to initiate test.

SETUP:
CLOCK - neg. edge TP9 (LMYPA)
START - neg. edge TP7 (LRST)
STOP - pos. edge TP7 (LRST)
VH - H9A0
+ - KEY SIGNATURE

U 4- 2 PCF9 +
U 4- 4 12P3 +

U 6- 4 1875 +
U 6-10 7226
U 6-12 FC43 +

U 9- 1 7226 +
U 9-11 7226 +

U 10- 1 1046 +

U 14- 1 0001
U 14- 2 8211
U 14- 3 8211
U 14- 5 7C65
U 14- 6 2137
U 14- 9 33FH
U 14-11 H9A0
U 14-12 635A
U 14-15 FP0C
U 14-16 C623
U 14-19 25CF

U 22-11 A240 +

U 23- 1 F020 +

U 25- 1 1046 +
U 25-19 1046 +

U 26- 1 0000
U 26- 2 99P6
U 26- 3 33FH
U 26- 4 8211
U 26- 5 U478
U 26- 6 92HP
U 26- 7 25CF
U 26- 8 7C65
U 26- 9 CHC2
U 26-11 H9A0
U 26-12 04HH
U 26-13 635A
U 26-14 C623
U 26-15 6P61
U 26-16 25PC
U 26-17 2137
U 26-18 FP0C
U 26-19 H275

U 32- 1 99P6
U 32- 2 H275
U 32- 3 25PC
U 32- 4 6P61
U 32- 5 U478
U 32- 6 92HP
U 32- 7 CHC2
U 32- 9 1875
U 32-10 6P9H
U 32-11 9354
U 32-12 UH4A
U 32-13 0000

U 32-14 0000
U 32-15 04HH

U 33- 5 FC43
U 33- 9 0000
U 33-11 H9A0
U 33-15 12P3

U 37-11 A0P5 +

U 38- 1 C425 +

U 41- 1 0000
U 41- 2 1046
U 41- 3 4A6F
U 41- 4 P44F
U 41- 5 7226
U 41- 6 PCF9
U 41- 7 CH73
U 41- 8 4U26
U 41- 9 12P3
U 41-11 0000
U 41-12 A240
U 41-13 2P61
U 41-14 PAA0
U 41-15 F020
U 41-16 A0P5
U 41-17 2C2C
U 41-18 02AA
U 41-19 C425

U 42- 1 02AA
U 42- 2 2C2C
U 42- 3 PAA0
U 42- 4 2P61
U 42- 5 4A6F
U 42- 6 P44F
U 42- 7 CH73
U 42- 9 4U26
U 42-10 UH4A
U 42-11 9354
U 42-12 6P9H
U 42-13 1875
U 42-14 0000
U 42-15 0000

Table 8-8. SA Loop M

INTERFACE LOOP-M

PC BOARD: 64941-66501 Floppy Control

CIRCUITRY TESTED: All data (I/O bus) to and from floppy controller

PROCEDURE: Remove U25 mode buffer (U25 can be tested by exchanging with U40). Remove all option boards. Move E2 TEST jumper to interface TEST position in XU15. Press DSA 1 soft key to initiate test.

SETUP:
CLOCK - pos. edge TP9 (LMYPA)
START - neg. edge TP6 (SA GATE)
STOP - pos. edge TP6 (SA GATE)
VH - PCP5
+ - KEY SIGNATURE

U 10-12 407C +

U 14- 3 HP0C +
U 14- 4 AC42 +
U 14- 7 FF31 +
U 14- 8 H582 +
U 14-13 403H +
U 14-14 8198 +
U 14-17 HF8A +
U 14-18 F858 +

U 22- 2 UCA9 +
U 22- 5 438U +
U 22- 6 P366 +
U 22- 9 F596 +
U 22-12 6HA3 +
U 22-15 407C +
U 22-16 3841 +
U 22-19 CF2H +

U 23- 3 UCA9 +
U 23- 4 438U +
U 23- 7 P366 +
U 23- 8 F596 +
U 23-13 6HA3 +
U 23-14 407C +
U 23-17 3841 +
U 23-18 CF2H +

U 24- 3 UCA9 +
U 24- 4 438U +
U 24- 7 P366 +
U 24- 8 F596 +
U 24-13 6HA3 +
U 24-14 407C +
U 24-17 3841 +
U 24-18 CF2H +

U 37- 2 H582 +
U 37- 5 FF31 +
U 37- 6 AC42 +
U 37- 9 HP0C +
U 37-12 403H +
U 37-15 8198 +
U 37-16 HF8A +
U 37-19 F858 +

U 38- 3 H582 +
U 38- 4 FF31 +
U 38- 7 AC42 +
U 38- 8 HP0C +
U 38-13 403H +
U 38-14 8198 +
U 38-17 HF8A +
U 38-18 F858 +

Table 8-9. SA Loop C

INTERFACE LOOP-C

PC BOARD: 64941-66501 Floppy Control

CIRCUITRY TESTED: I/O bus decoding

PROCEDURE: Remove U25 mode buffer (U25 can be tested by exchanging with U40). Remove all option boards. Move E2 TEST jumper to interface TEST position in XU15. Press DSA 1 soft key to initiate test.

SETUP:
CLOCK - pos. edge TP1 I/O board (LIOSB)
START - pos. edge TP2 I/O board (I/O SA LATCH)
STOP - neg. edge TP2 I/O board (I/O SA LATCH)
VH - 9CCH
+ - KEY SIGNATURE

U 7- 6	H164	+
U 9- 3	H164	+
U 9-13	H164	+
U 10- 3	1FAA	+
U 10-10	H543	+
U 10-11	1FAA	+
U 14- 1	188H	+
U 14-11	H164	+
U 15- 9	H164	
U 16- 9	H164	+
U 22- 1	02HP	+
U 23-11	FC37	+
U 24-11	1FAA	+
U 26-11	H164	+
U 28- 1	3H75	
U 28- 2	P552	
U 28- 3	P552	
U 28- 4	7PPU	
U 28- 5	7PPU	
U 28- 6	9CCH	
U 28- 7	6662	
U 28- 9	CP45	
U 28-10	P552	
U 28-11	9CCH	
U 28-12	188H	
U 28-13	P552	
U 28-14	0000	
U 28-15	0000	
U 33- 4	7PPU	
U 33- 6	9962	
U 33- 7	0000	
U 33- 8	A6F8	
U 33- 9	4AH9	
U 33-11	H164	
U 33-12	3H75	
U 33-13	9CCH	
U 33-14	02HU	
U 33-16	P552	
U 36- 1	FF56	
U 36- 2	3CHU	
U 36- 3	190F	
U 36- 4	0000	
U 36- 5	0000	
U 36- 6	8CU1	
U 36-12	H164	
U 37- 1	02HP	+
U 38-11	FC37	+
U 41-11	4AH9	+
U 45- 1	02HU	
U 45- 2	CP45	
U 45- 3	CP45	
U 45- 4	H543	
U 45- 5	0000	
U 45- 6	6662	
U 45- 7	1FAA	
U 45- 9	FC37	
U 45-10	188H	
U 45-11	0000	
U 45-12	02HP	
U 45-13	0000	
U 45-14	188H	
U 45-15	H164	

Table 8-10. SA Loop D

INTERFACE LOOP-D

PC BOARD: 64941-66501 Floppy Control

CIRCUITRY TESTED: Data written to floppy drives

PURPOSE: Remove U25 mode buffer (U25 can be tested by exchanging with U40). Remove all option boards. Move E2 TEST jumper to interface TEST position in XU15. Press DSA 1 soft key to initiate test.

SETUP:
CLOCK - pos. edge TP14 LWRT
START - pos. edge TP2 I/O board (I/O SA LATCH)
STOP - neg. edge TP2 I/O board (I/O SA LATCH)
VH - 399F
+ - KEY SIGNATURE

U 4-19 6C35 +	U 22-16 U834 +	U 34-14 6651 +
	U 22-19 52PF +	U 34-15 6651 +
U 6- 5 0A66 +		
U 6- 9 0A66 +	U 23- 3 C4F8 +	
	U 23- 4 98F4 +	
U 9-12 33UA	U 23- 7 71P3 +	U 35- 3 9064 +
	U 23- 8 606H +	U 35- 6 086P +
U 10- 3 5613 +	U 23-13 HA15 +	U 35-10 19P9 +
U 10- 8 33UA +	U 23-14 U74A +	U 35-13 H45F +
U 10- 9 0A66 +	U 23-17 U834 +	U 35-14 5U64 +
U 10-10 6U8U +	U 23-18 52PF +	
U 10-11 5613 +		U 37- 2 46CA +
U 10-12 U74A +	U 24- 2 5U64	U 37- 5 46CA +
	U 24- 3 C4F8	U 37- 6 1443 +
U 14- 3 1443 +	U 24- 4 98F4	U 37- 9 1443 +
U 14- 4 1443 +	U 24- 5 6C35	U 37-12 7C48 +
U 14- 7 46CA +	U 24- 6 19P9	U 37-15 29C1 +
U 14- 8 46CA +	U 24- 7 71P3	U 37-16 29U0 +
U 14-13 7C48 +	U 24- 8 606H	U 37-19 29C1 +
U 14-14 29C1 +	U 24- 9 9064	
U 14-17 29U0 +	U 24-11 5613	U 38- 3 46CA +
U 14-18 29C1 +	U 24-12 6651	U 38- 4 46CA +
	U 24-13 HA15	U 38- 7 1443 +
U 22- 2 C4F8 +	U 24-14 U74A	U 38- 8 1443 +
U 22- 5 98F4 +	U 24-15 U7UC	U 38-13 7C48 +
U 22- 6 71P3 +	U 24-16 H45F	U 38-14 29C1 +
U 22- 9 606H +	U 24-17 U834	U 38-17 29U0 +
U 22-12 HA15 +	U 24-18 52PF	U 38-18 29C1 +
U 22-15 U74A +		

Table 8-11. SA Loop E

INTERFACE LOOP-E

PC BOARD: 64941-66501 Floppy Control

CIRCUITRY TESTED: Floppy read latches

PROCEDURE: Remove U25 mode buffer (U25 can be tested by exchanging with U40). Remove all option boards. Move E2 TEST jumper to interface TEST position in XU15. Press DSA 1 soft key to initiate test.

SETUP:
CLOCK - pos. edge TP10 (LRD)
START - neg. edge TP6 (SA GATE)
STOP - pos. edge TP6 (SA GATE)
VH - 0007
+ - KEY SIGNATURE

U 22- 2 0003	U 23- 3 0003 +	U 37- 2 0002	U 38- 3 0002
U 22- 5 0003	U 23- 4 0003 +	U 37- 5 0002	U 38- 4 0002
U 22- 6 0003	U 23- 7 0003 +	U 37- 6 0002	U 38- 7 0002
U 22- 9 0003	U 23- 8 0003 +	U 37- 9 0002	U 38- 8 0002
U 22-12 0003	U 23-13 0003 +	U 37-12 0001	U 38-13 0001
U 22-15 0003	U 23-14 0003 +	U 37-15 0001	U 38-14 0001
U 22-16 0003	U 23-17 0003 +	U 37-16 0001	U 38-17 0001
U 22-19 0003	U 23-18 0003 +	U 37-19 0001	U 38-18 0001

Table 8-12. SA Loop F

INTERFACE LOOP-F

PC BOARD: 64941-66501 Floppy Control

CIRCUITRY TESTED: Data out of U23

PROCEDURE: Remove U25 mode buffer (U25 can be tested by exchanging with U40). Remove all option boards. Move E2 TEST jumper to interface TEST position in XU15. Press DSA 1 soft key to initiate test.

SETUP:
CLOCK - pos. edge TP13 (LOEM)
START - neg. edge TP6 (SA GATE)
STOP - pos. edge TP6 (SA GATE)
VH - 0003
+ - KEY SIGNATURE

U 4- 7 0002 +	U 23- 2 0002	U 39- 7 0002 +
U 4- 8 0002 +	U 23- 5 0002	U 39- 8 0002 +
U 4- 9 0002 +	U 23- 6 0002	U 39-13 0002 +
U 4-10 0002 +	U 23- 9 0002	U 39-14 0002 +
U 4-11 0002 +	U 23-12 0002	U 39-17 0002 +
U 4-12 0002 +	U 23-15 0002	U 39-18 0002 +
U 4-13 0002 +	U 23-16 0002	
U 4-14 0002 +	U 23-19 0002	

Table 8-13. SA Loop G

INTERFACE LOOP-G

PC BOARD: 64941-66501 Floppy Control

CIRCUITRY TESTED: Data from U38

PROCEDURE: Remove U25 mode buffer (U25 can be tested by exchanging with U40). Remove all option boards. Move E2 TEST jumper to interface TEST position in XU15. Press DSA 1 soft key to initiate test.

SETUP:
CLOCK - pos. edge TP11 BY U41 (LOEL)
START - neg. edge TP6 (SA GATE)
STOP - pos. edge TP6 (SA GATE)
VH - 0UP7
+ - KEY SIGNATURE

U 4- 7 0A2H +	U 38- 6 0A2H	U 39- 3 0A2H +
U 4- 8 0F24 +	U 38- 9 0A2H	U 39- 4 0A2H +
U 4- 9 0A2H +	U 38-12 0408	U 39- 7 0F24 +
U 4-10 0F14 +	U 38-15 0F24	U 39- 8 0408 +
U 4-11 0201 +	U 38-16 0F14	U 39-13 0201 +
U 4-12 0F24 +	U 38-19 0F24	U 39-14 0201 +
U 4-13 0201 +		U 39-17 0F14 +
U 4-14 0408 +		U 39-18 0F24 +

Table 8-14. SA Loop H

INTERFACE LOOP-H

PC BOARD: 64941-66501 Floppy Control

CIRCUITRY TESTED: Data from U40

PROCEDURE: Remove U25 mode buffer (U25 can be tested by exchanging with U40). Remove all option boards. Move E2 TEST jumper to interface TEST position in XU15. Press DSA 1 soft key to initiate test.

SETUP:
CLOCK - pos. edge TP8
START - neg. edge TP6 (SA GATE)
STOP - pos. edge TP6 (SA GATE)
VH - 0003
+ - KEY SIGNATURE

U 37- 3 0002 +	U 37-17 0001 +	U 40- 7 0002
U 37- 4 0002 +	U 37-18 0001 +	U 40- 9 0002
U 37- 7 0002 +		U 40-12 0001
U 37- 8 0002 +	U 40- 1 0000	U 40-14 0001
U 37-13 0001 +	U 40- 3 0002	U 40-16 0001
U 37-14 0001 +	U 40- 5 0002	U 40-18 0001
		U 40-19 0000

Table 8-15. SA Loop I

INTERFACE LOOP-I

PC BOARD: 64941-66501 Floppy Control

CIRCUITRY TESTED: Data from floppy controller (MSB)

PROCEDURE: Remove U25 mode buffer (U25 can be tested by exchanging with U40). Remove all option boards. Move E2 TEST jumper to interface TEST position in XU15. Press DSA 1 soft key to initiate test.

SETUP:
CLOCK - pos. edge U22-PIN 11 (LLM)
START - neg. edge TP6 (SA GATE)
STOP - pos. edge TP6 (SA GATE)
VH - 07U3
+ - KEY SIGNATURE

U 4- 7 07H3	U 22- 3 07H3 +	U 25- 1 0020
U 4- 8 07H3	U 22- 4 07H3 +	U 25- 3 07H3
U 4- 9 07H3	U 22- 7 07H3 +	U 25- 5 07H3
U 4-10 07H3	U 22- 8 07H3 +	U 25- 7 07H3
U 4-11 07H3	U 22-13 07H3 +	U 25- 9 07H3
U 4-12 07H3	U 22-14 07H3 +	U 25-12 07H3
U 4-13 07H3	U 22-17 07H3 +	U 25-14 07H3
U 4-14 07H3	U 22-18 07H3 +	U 25-16 07H3
		U 25-18 07H3
		U 25-19 0020

Table 8-16. SA Loop J

INTERFACE LOOP-J

PC BOARD: 64941-66501 Floppy Control

CIRCUITRY TESTED: Data from floppy controller (LSB) and data from mode buffer U40.

PROCEDURE: Remove U25 mode buffer (U25 can be tested by exchanging with U40). Remove all option boards. Move E2 TEST jumper to interface TEST position in XU15. Press DSA 1 soft key to initiate test.

SETUP:
CLOCK - pos. edge U37-PIN 11 (LLL)
START - neg. edge TP6 (SA GATE)
STOP - pos. edge TP6 (SA GATE)
VH - 001U
+ - KEY SIGNATURE

U 4- 7 000A	U 37- 7 000A +	U 40- 1 001F
U 4- 8 0011	U 37- 8 000A +	U 40- 3 000A
U 4- 9 000A	U 37-13 0011 +	U 40- 5 000A
U 4-10 0011	U 37-14 0011 +	U 40- 7 000A
U 4-11 000A	U 37-15 001U +	U 40- 9 000A
U 4-12 0011	U 37-16 001U +	U 40-12 0011
U 4-13 000A	U 37-17 0011 +	U 40-14 0011
U 4-14 0011	U 37-18 0011 +	U 40-16 0011
		U 40-18 0011
		U 40-19 001F

Table 8-17. SA Loop K

DATA SEPARATOR LOOP-K

PC BOARD: 64941-66501 Floppy Control

CIRCUITRY TESTED: Data separator circuitry

PROCEDURE: Remove all option boards. Move E1 TEST jumper to separator TEST position in XU7. Press DSA 2 soft key to initiate test.

SETUP:
CLOCK - pos. edge TP9 (LMYPA)
START - neg. edge U14-PIN 15 (SA GATE HDSA5 TP3)
STOP - pos. edge U14-PIN 15 (SA GATE HDSA5 TP3)
VH - HCH5
+ - KEY SIGNATURE

U 7- 1	5944	U 18- 1	0000	U 21- 1	0000	U 33- 4	0000
U 7- 2	5U2F	U 18- 2	P733	U 21- 2	0000	U 33- 6	0000
U 7- 3	8P80	U 18- 3	5A44	U 21- 3	6P1C	U 33- 8	5690
U 7- 4	CAHF	U 18- 4	0000	U 21- 4	HCH5	U 33-12	8H45
U 7- 5	5A44	U 18- 5	4H3A	U 21- 5	5C86	U 33-14	HCH5
U 7- 6	0000	U 18- 6	4H3A	U 21- 6	8053	U 33-16	HCH5
		U 18- 7	4FA6	U 21-11	5944		
U 11- 1	7CA3 +	U 18- 9	4U2F	U 21-15	0HA5	U 43- 4	CH11
U 11- 2	7CA3 +	U 18-10	H015			U 43- 5	82F8
U 11- 6	55AP +	U 18-11	0000	U 24- 4	UUCF	U 43- 6	82A4
U 11- 7	55AP +	U 18-12	0000	U 24- 5	165A	U 43-11	5623
		U 18-13	0000	U 24-11	8H45	U 43-12	8053
U 14- 1	5690	U 18-14	5C86			U 43-13	0HA5
U 14- 2	5944	U 18-15	0000	U 27- 4	HCH5		
U 14- 3	HPU6			U 27-10	HCH5	U 44- 8	0000
U 14- 4	27PU	U 19- 1	4FA6	U 27-11	5944	U 44- 9	HCH5
U 14- 5	8P80	U 19- 2	0000	U 27-12	HCH5	U 44-10	HCH5
U 14- 6	5A44	U 19- 3	HCH5	U 27-13	0000	U 44-11	HCH5
U 14- 7	H8U7	U 19- 4	HCH5			U 44-12	0000
U 14- 8	64A3	U 19- 5	7CA3	U 28- 1	8H45	U 44-13	0000
U 14- 9	846P	U 19- 7	55AP	U 28-12	5690		
U 14-11	0000	U 19-10	HCH5	U 28-13	HCH5	U 45- 1	HCH5
U 14-12	C107	U 19-11	HCH5			U 45- 5	0000
U 14-13	OP71	U 19-12	0000	U 29- 1	HCH5	U 45- 6	5690
U 14-14	5691	U 19-13	4U2F	U 29- 2	82A4	U 45- 7	8H45
U 14-15	0000	U 19-14	4FA6	U 29- 6	488C	U 45- 9	8H45
U 14-16	CAHF	U 19-15	4U2F	U 29- 8	82F8	U 45-10	5690
U 14-17	19F6			U 29-10	CH11	U 45-12	HCH5
U 14-18	P8F9	U 20- 1	H015	U 29-12	0000	U 45-14	5690
U 14-19	5U2F	U 20- 2	0000	U 29-13	0000	U 45-15	0000
		U 20- 3	0HA5				
U 17- 1	5A44	U 20- 4	165A	U 30- 1	HCH5	U 46- 1	82A4
U 17- 2	HCH5	U 20- 5	2P64	U 30- 2	HCH5	U 46- 2	84U9
U 17- 3	383P	U 20- 6	383P	U 30- 4	0HA5	U 46- 3	F82F
U 17- 5	4H3A	U 20- 9	6P1C	U 30- 6	P733	U 46-11	84U9
U 17- 9	H015	U 20-10	HCH5	U 30- 8	488C	U 46-12	5U2F
U 17-11	383P	U 20-11	2P64	U 30- 9	F82F	U 46-13	HCH5
U 17-12	HCH5	U 20-12	0000				
U 17-13	CAHF	U 20-13	0000	U 31- 9	2P64		
		U 20-14	0HA5				
		U 20-15	5623				

Table 8-18. SA Loop L

DATA SEPARATOR LOOP-L

PC BOARD: 64941-66501 Floppy Control

CIRCIUTRY TESTED: U18 multiplexer

PROCEDURE: Remove all option boards. Move E1 TEST jumper to separator TEST position in XU7. Check U18 multiplexer to make sure it is multiplexing the HDATA1US signal properly. There are no signature nodes for this loop, just verify that VH is correct. Press DSA 2 soft key to initiate test.

SETUP:
CLOCK - pos. edge U18-PIN 9
START - pos. edge U21-PIN 11
STOP - pos. edge U21-PIN 11
VH - 72A2

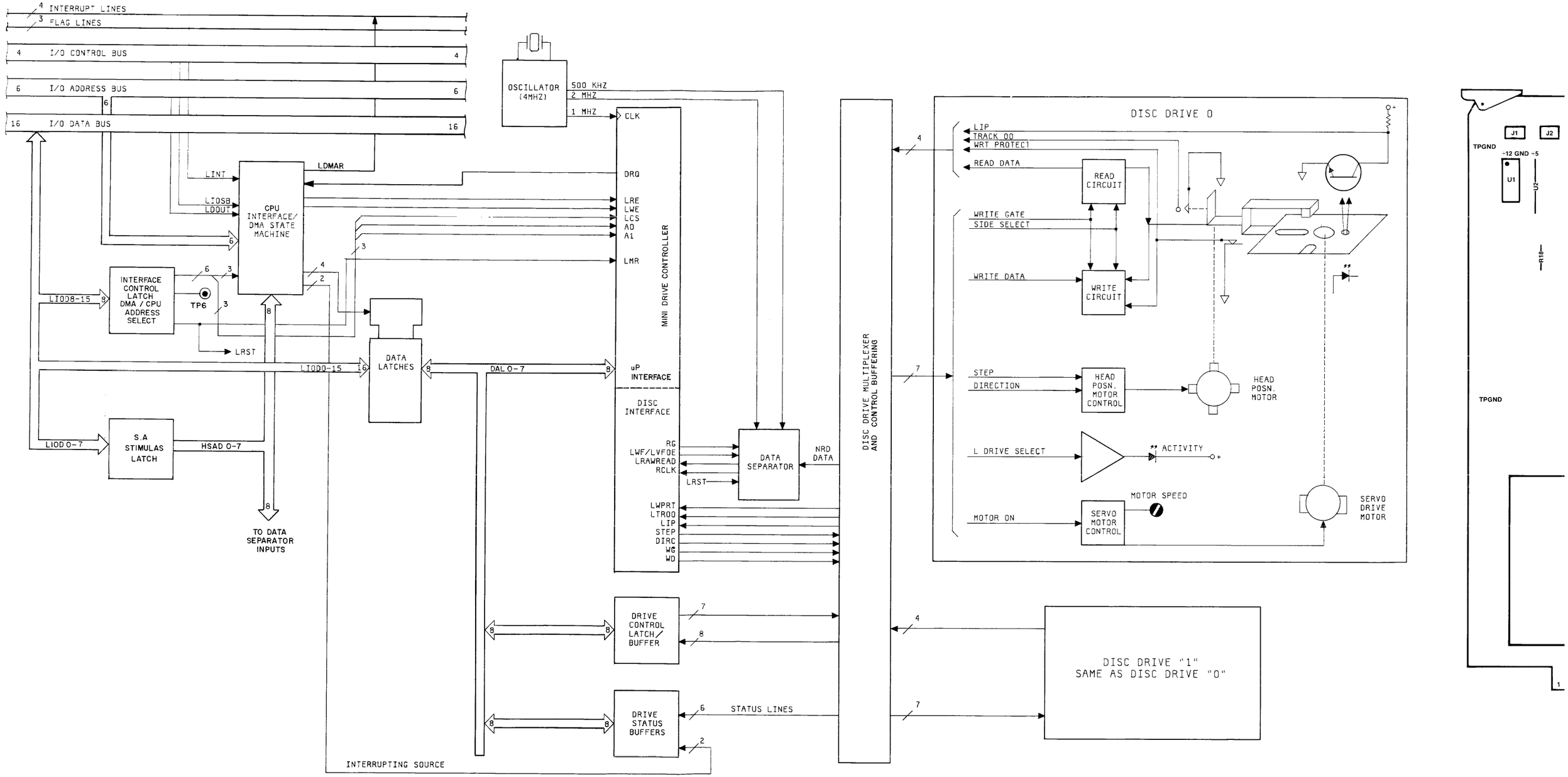
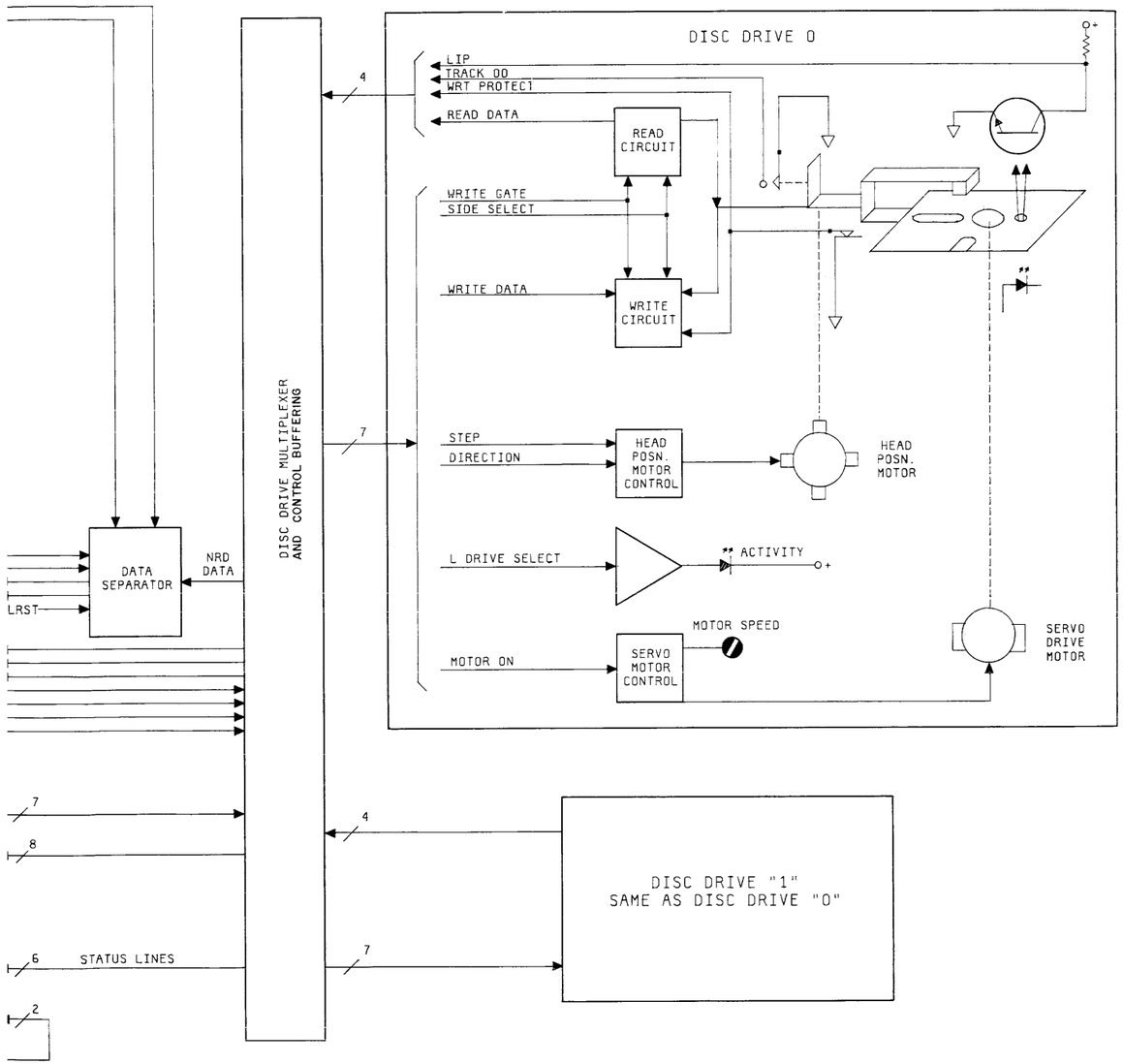
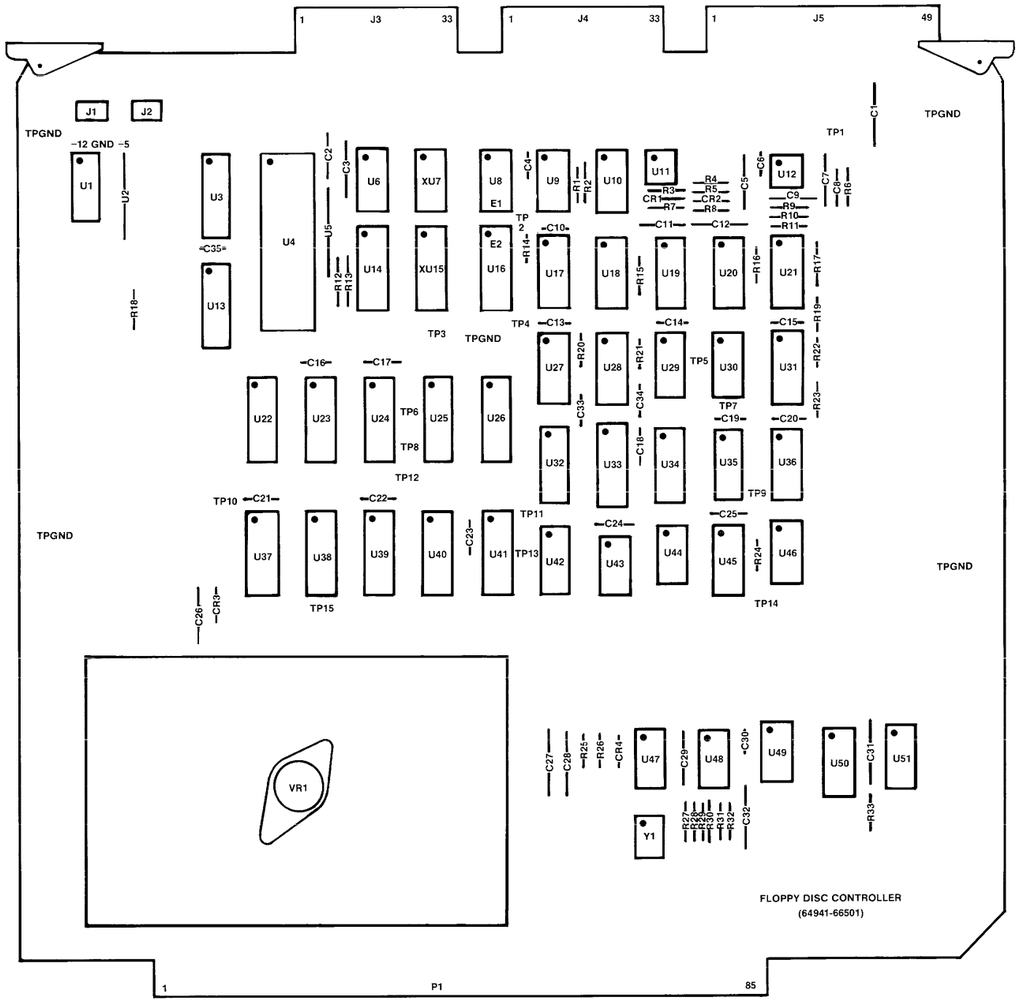


Figure 8-8.
Component Locator and Block Diagram for Service Sheet 11A.


DISC DRIVE 0
LIP
TRACK 00
WRT PROTECT
READ DATA
READ CIRCUIT
WRITE GATE
SIDE SELECT
WRITE DATA
WRITE CIRCUIT
STEP
DIRECTION
HEAD POSN. MOTOR CONTROL
HEAD POSN. MOTOR
L DRIVE SELECT
** ACTIVITY
MOTOR ON
MOTOR SPEED
SERVO MOTOR CONTROL
SERVO DRIVE MOTOR
4
7
DISC DRIVE MULTIPLEXER AND CONTROL BUFFERING
DATA SEPARATOR
NRD DATA
LRST
7
8
4
DISC DRIVE "1"
SAME AS DISC DRIVE "0"
6
STATUS LINES
7
2


J3
J4
J5
J1
J2
TPGND
-12 GND -5
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
TP14
TP15
VR1
Y1
FLOPPY DISC CONTROLLER
(64941-66501)
P1

P/O MINI CONTROL BOARD
(64941-66501)

P/O W5

P/O J5
LIOD0
LIOD1
LIOD2
LIOD3
LIOD4
LIOD5
LIOD6
LIOD7
LIOD8
LIOD9
LIOD10
LIOD11
LIOD12
LIOD13
LIOD14
LIOD15

B 13 LMCIR
B 11 LMDCRQ
B 28 LPOPB
B 10 HDRQ
B 9 L2MHZC
B 8 H2MHZC

P/O J5
LPA3
LIOSB
LPA0
LPA1
LPA2
LIC1
LDOUT
LIC2
LINT
NC
+12
+5
-12
TP GND

DMUX
U36
P/O U33
MUX
U28
U45
CPU DECODE
ACK
HIC1
HIC2
HR5
HR6
LWRT
LRD
PCMD
LR6
TP9
AC

INTERFACE CONTROL LATCH
D-FF
U24
PCMD ACDK
LIOD12 DKM
LIOD8 DM
LIOD15 DM
LIOD9 DM
LIOD13 DM
LIOD10 DM
LIOD14 DM
LIOD11 DM
ADK
AD
TP6

DMA/CPU ADDRESS SELECTOR
MUX
U35
LA0
LA1
LCS
LWRTSM

INTERRUPT CIRCUITRY
U34A
U34B
U6C
LASTINT

SA STIMULUS LATCH
D-FF
U14
CKBA
LIOD0 KMD
LIOD1 KMD
LIOD2 KMD
LIOD3 KMD
LIOD4 KMD
LIOD5 KMD
LIOD6 KMD
LIOD7 KMD
HSAD0 ABK
HSAD1 ABK
HSAD2 ABK
HSAD3 ABK
HSAD4 ABK
HSAD5 ABK
HSAD6 ABK
HSAD7 ABK
XU15
TEST
P/O E2
TP3
RUN

LWYPA
LIOD13
LAST
LWRTSM
LDMAAK
LPRQ
LDMAEN
LDRQ

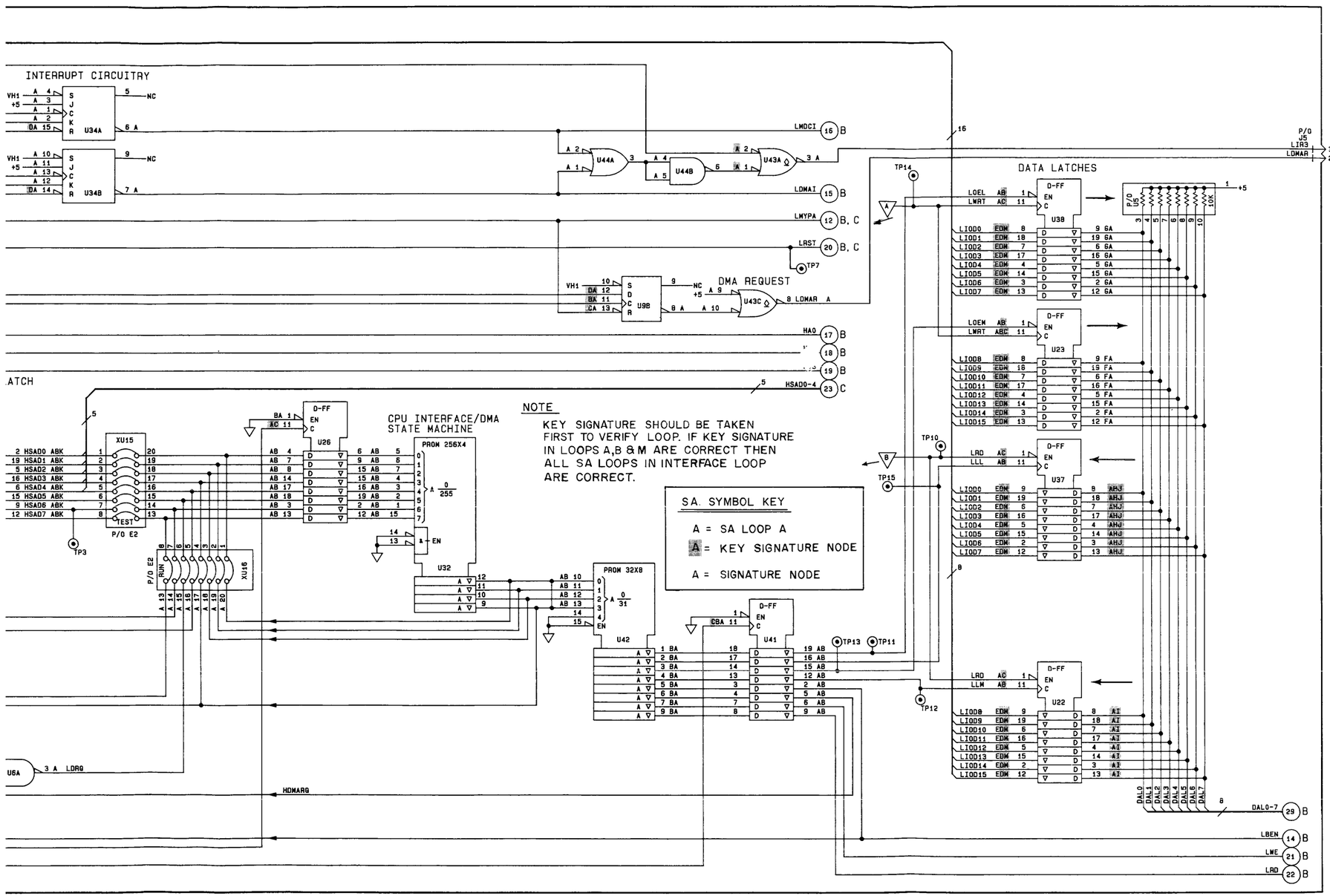
R34 511
C36 100PF

DMA ACKNOWLEDGE LATCH
U9A

PROCESSOR REQUEST LATCH
U10A

DMA ENABLE LATCH
U10B
HDMAEN

U6B
U6A



11A

ICs ON THIS SCHEMATIC

Ref Des	HP Part No.	Mfr Part No.
U5	1810-0280	210A102
U6	1820-1425	74SL132
U9, 10	1820-1112	74LS74
U14	1820-1858	74LS377
U22, 23, 26, 37, 38, 41	1820-1997	74LS374
U24	1820-1730	74LS273
U28, 45	1820-1428	74LS 158
U32	64110-10001	64110-10001
U33	1820-1917	74LS240
U34	1820-1212	74LS112
U35	1820-1470	74LS157
U36	1820-1216	74LS138
U42	64110-10002	64110-10002
U43	1820-1246	74LS09

PARTS ON THIS SCHEMATIC

U6, 9, 10, 14, 22, 23, 24, 26, 28, 32-38, 41-45

E2

POWER CONFIGURATIONS

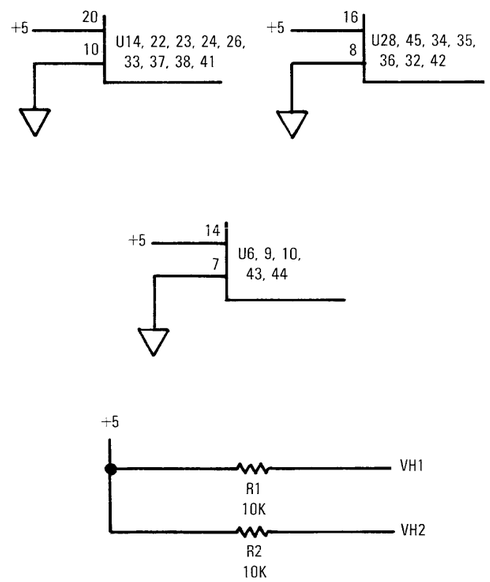
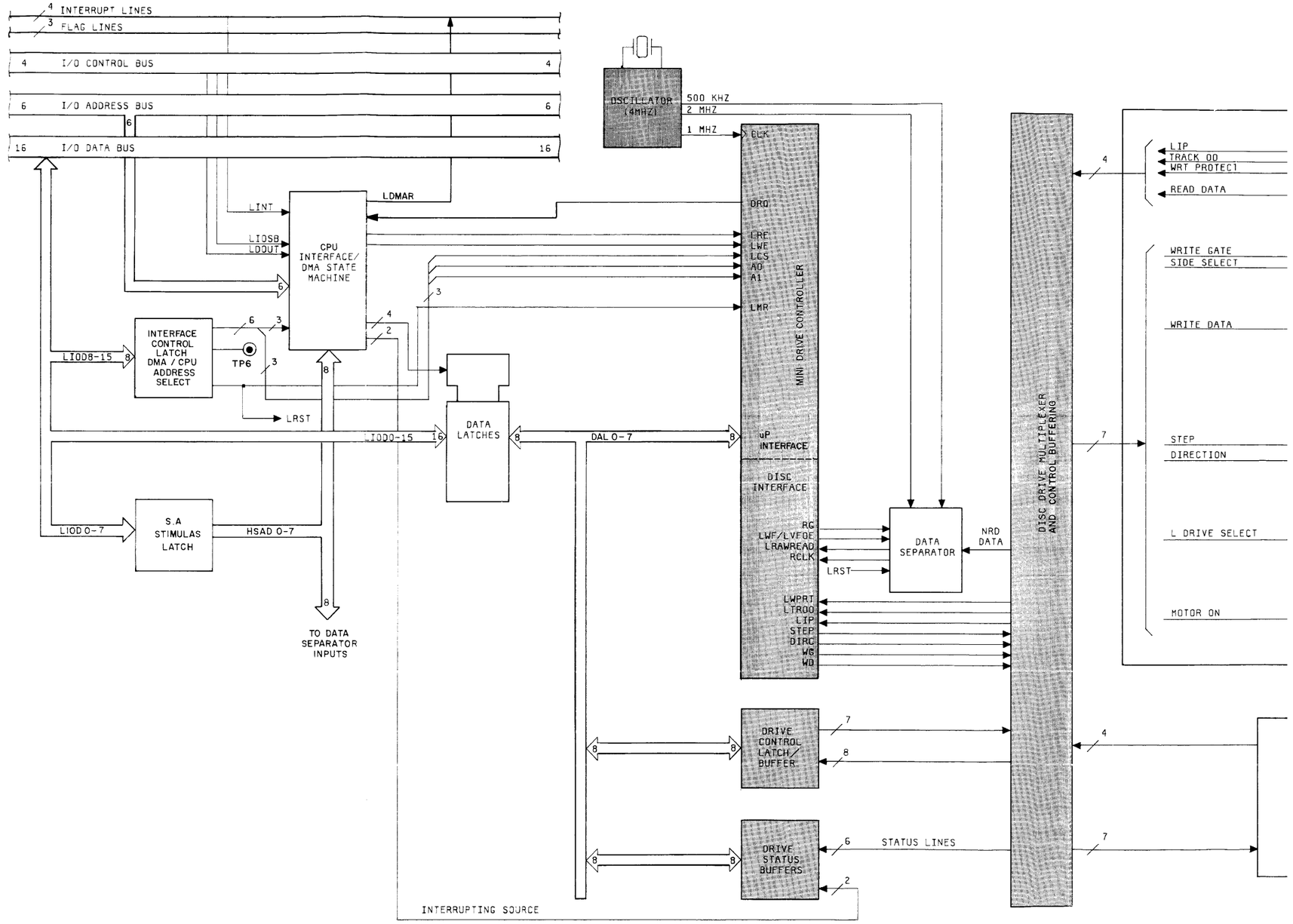
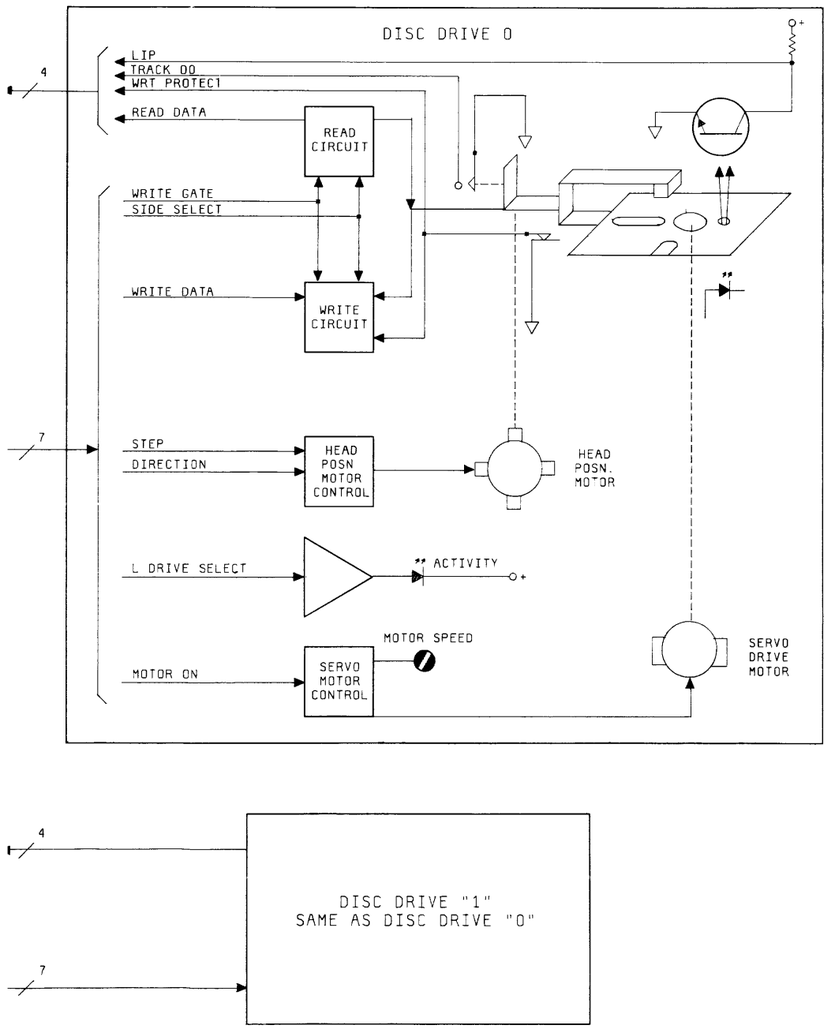


Figure 8-9.
Mini Control Service Sheet 11A


4 INTERRUPT LINES
3 FLAG LINES
4 I/O CONTROL BUS 4
6 I/O ADDRESS BUS 6
16 I/O DATA BUS 16
OSCILLATOR (4MHZ)
500 KHZ
2 MHZ
1 MHZ
CLK
LINT
LIOSB
LDOUT
LDMAR
CPU INTERFACE/ DMA STATE MACHINE
DRQ
LRE
LWE
LCS
A0
A1
LMR
MINI DRIVE CONTROLLER
INTERFACE CONTROL LATCH DMA / CPU ADDRESS SELECT
LIOD8-15
TP6
LRST
LIOD0-15
DATA LATCHES
DAL 0-7
uP INTERFACE
DISC INTERFACE
RG
LWF/LVFOE
LRAWREAD
RCLK
LRST
DATA SEPARATOR
NRD DATA
LWPRT
LTR00
LIP
STEP
DIRC
WG
WD
S.A STIMULAS LATCH
LIOD 0-7
HSAD 0-7
TO DATA SEPARATOR INPUTS
DRIVE MULTIPLEXER CONTROL BUFFERING
DISC DRIVE MULTIPLEXER AND CONTROL BUFFERING
LIP
TRACK 00
WRT PROTECT
READ DATA
WRITE GATE
SIDE SELECT
WRITE DATA
STEP
DIRECTION
L DRIVE SELECT
MOTOR ON
DRIVE CONTROL LATCH / BUFFER
DRIVE STATUS BUFFERS
STATUS LINES
INTERRUPTING SOURCE



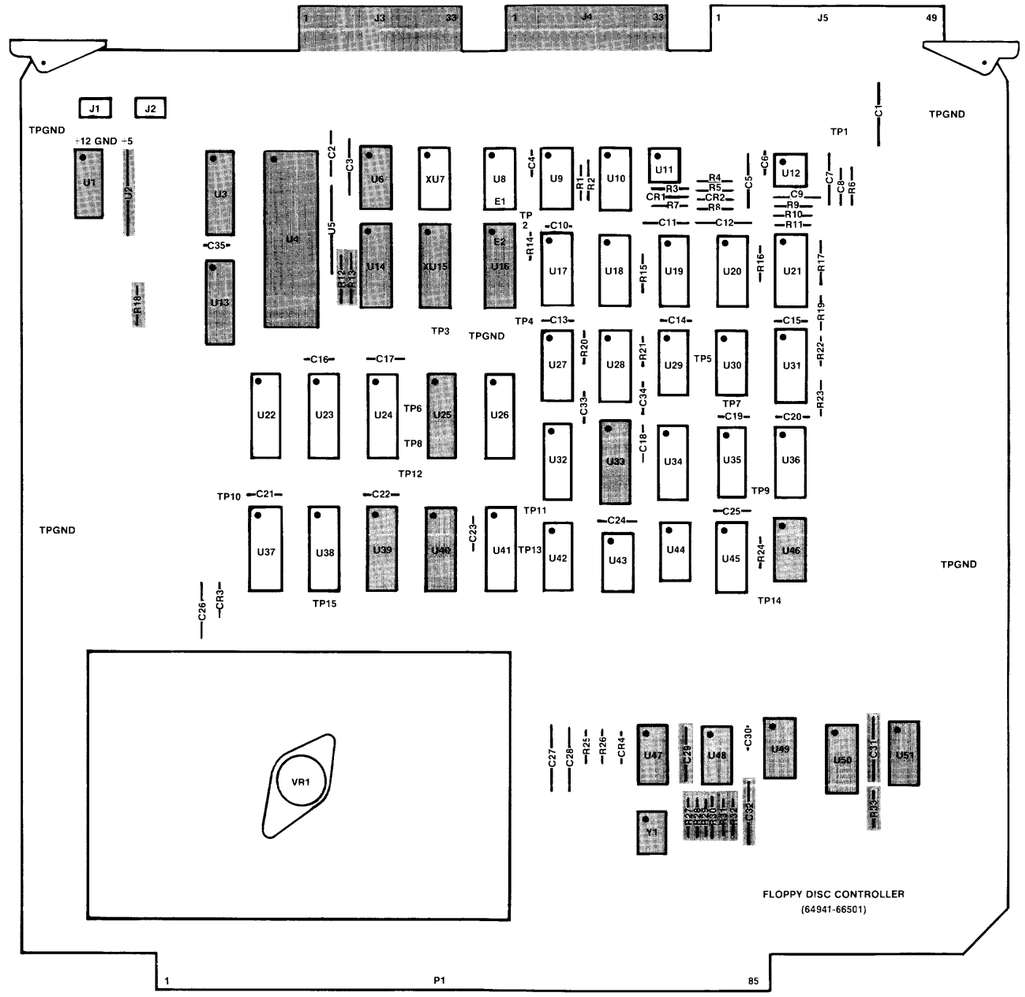


Figure 8-10. Component Locator and Block Diagram for Service Sheet 11B

TO DRIVE

P/O A11 MINI CONTROL BOARD
(64941-66501)

W1 J4

DRIVE SEL0
STEP
WRITE GATE
WRITE DATA
DIRECTION SEL
MOTOR ON
SIDE 1 SEL
READ DATA
INDEX
TRK00
WRITE PROTECT
READ DATA

P/O U13

HSTEP
HWS
HMD
HDIAC

TP7

A, C 20 LAST
A 17 HA0
A 18 HA1
A 19 LCS
A 21 LWE
A 22 LRD
A 28 LPOPB

76 P/O P1 LPOP

P/O U33

U49A U46B U46C U47A U47B U48

DRIVE CONTROL LATCH

U39 D-FF

DAL0 DAL1 DAL2 DAL3 DAL4 DAL5 DAL6 DAL7

LCRMC0
LCRMC1

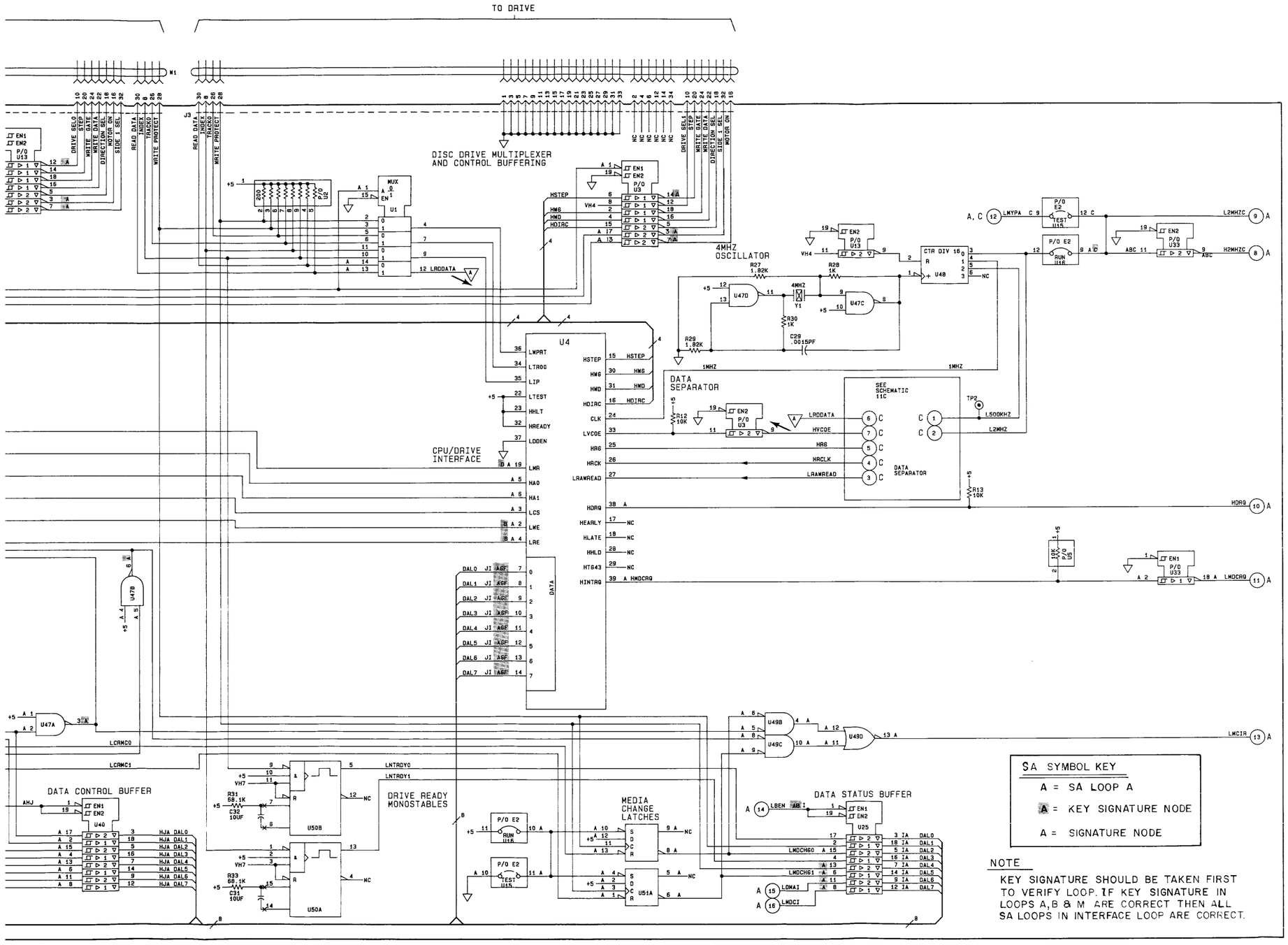
TP8

DATA CONTROL BUFFER

U40

HJA DAL0
HJA DAL1
HJA DAL2
HJA DAL3
HJA DAL4
HJA DAL5
HJA DAL6
HJA DAL7

A 29 DAL0-7



11B

ICs ON THIS SCHEMATIC

Ref Des	HP Part No.	Mfr Part No.
U1	1820-1470	74LS157
U2	1810-0271	
U3, 13	1820-1633	74S240
U4	1820-2456	FD1791A-02
U6	1820-1425	74LS132
U25, 40	1820-2024	74LS244
U33	1820-1917	74LS240
U39	1820-1730	74LS273
U46, 47	1820-1197	74LS00
U48	1820-1989	74LS393
U49	1820-1144	74LS02
U50	1820-1423	74LS123
U51	1820-1112	74LS74
Y1	0410-1298	

PARTS ON THIS SCHEMATICS

C29, 31, 32
E2
R12, 13, 27-31, 33
U1-4, 6, 13, 25, 33, 39, 40, 46-51
Y1

POWER CONFIGURATION

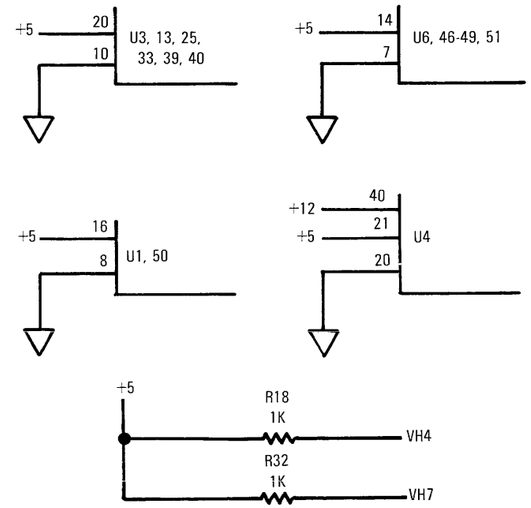
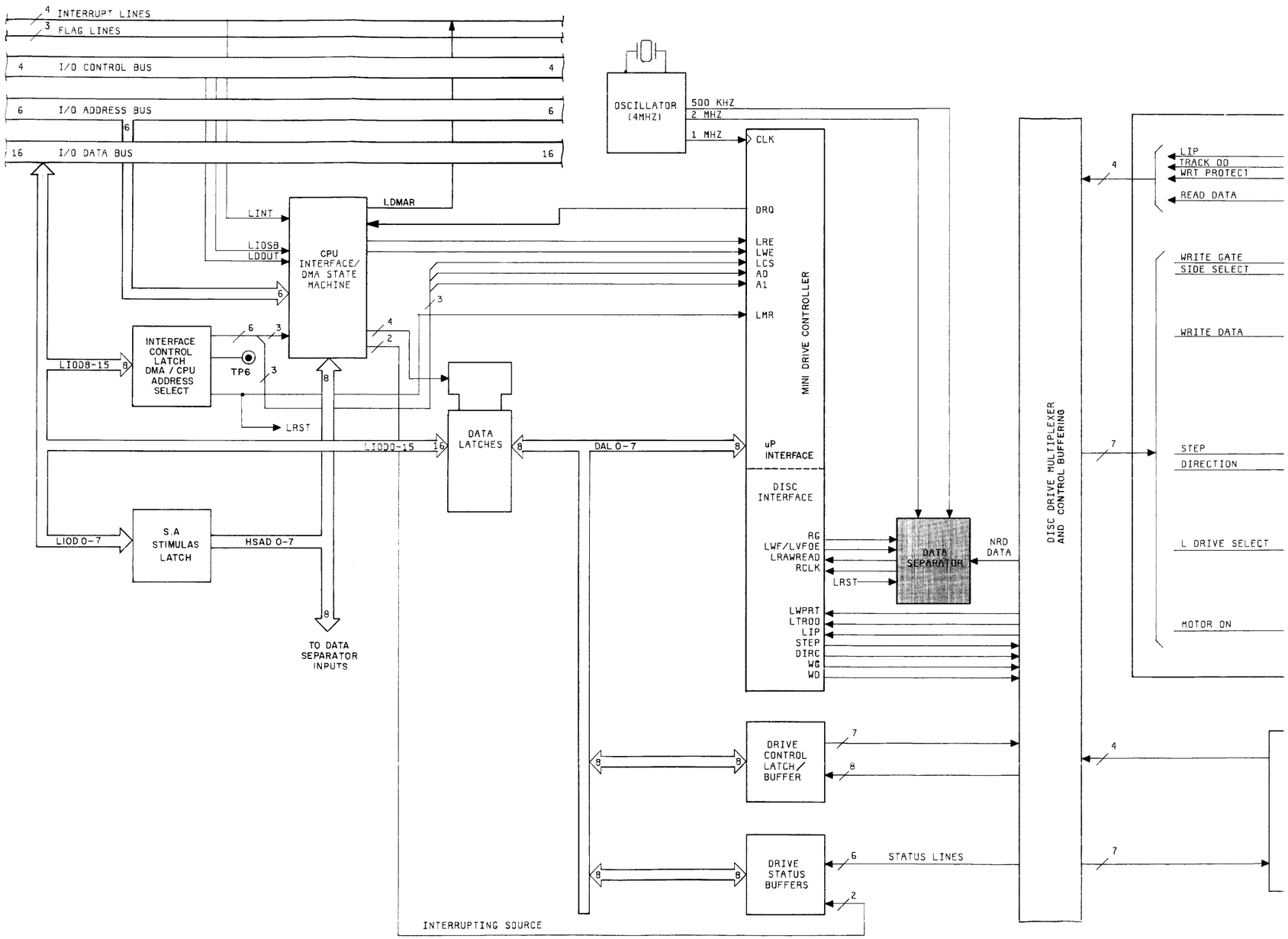
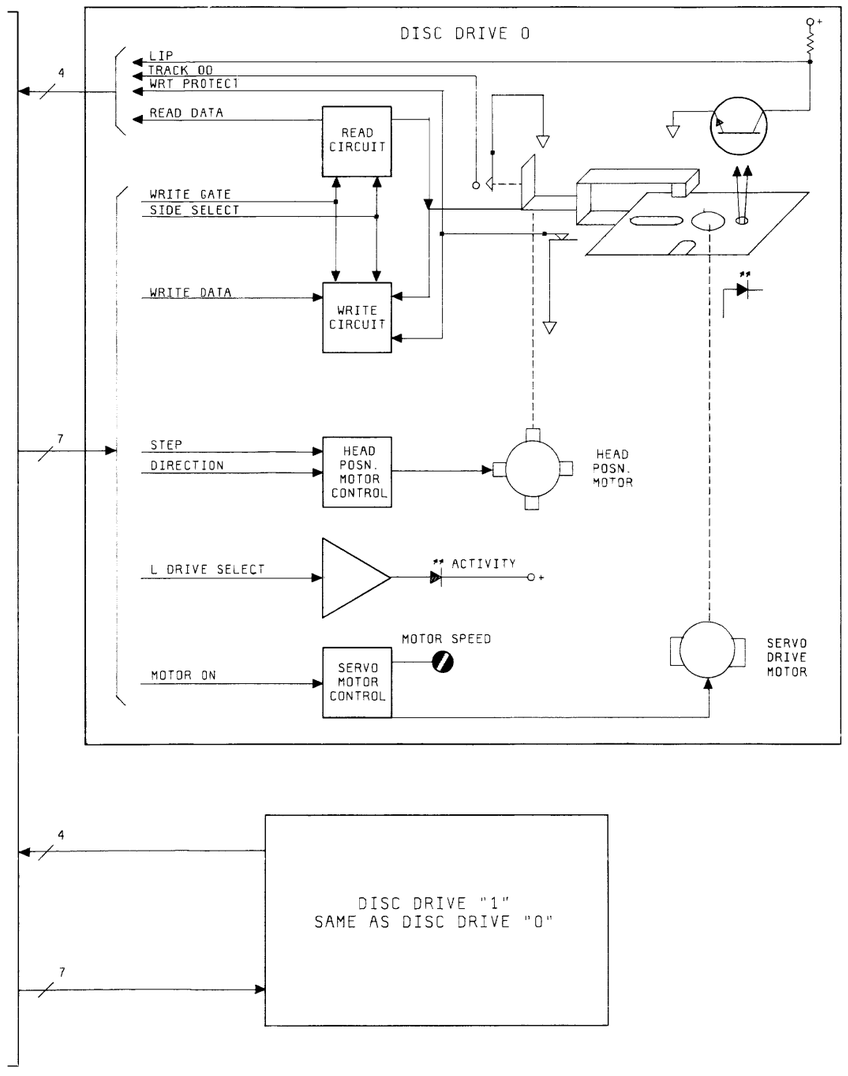


Figure 8-11.
Mini Control Service Sheet 11B
8-53


4 INTERRUPT LINES
3 FLAG LINES
4 I/O CONTROL BUS 4
6 I/O ADDRESS BUS 6
6
16 I/O DATA BUS 16
OSCILLATOR (4MHZ)
500 KHZ
2 MHZ
1 MHZ
CLK
LINT
LDMAR
DRQ
LIOSB
LDOUT
CPU INTERFACE/ DMA STATE MACHINE
LRE
LWE
LCS
A0
A1
LMR
MINI DRIVE CONTROLLER
INTERFACE CONTROL LATCH DMA / CPU ADDRESS SELECT
LIOD8-15
TP6
LRST
LIOD0-15
DATA LATCHES
DAL 0-7
uP INTERFACE
DISC INTERFACE
RG
LWF/LVFOE
LRAWREAD
RCLK
LRST
DATA SEPARATOR
NRD DATA
LWPRT
LTR00
LIP
STEP
DIRC
WG
WD
S.A STIMULAS LATCH
LIOD 0-7
HSAD 0-7
TO DATA SEPARATOR INPUTS
DRIVE CONTROL LATCH/ BUFFER
DRIVE STATUS BUFFERS
STATUS LINES
INTERRUPTING SOURCE
DISC DRIVE MULTIPLEXER AND CONTROL BUFFERING
LIP
TRACK 00
WRT PROTECT
READ DATA
WRITE GATE
SIDE SELECT
WRITE DATA
STEP
DIRECTION
L DRIVE SELECT
MOTOR ON



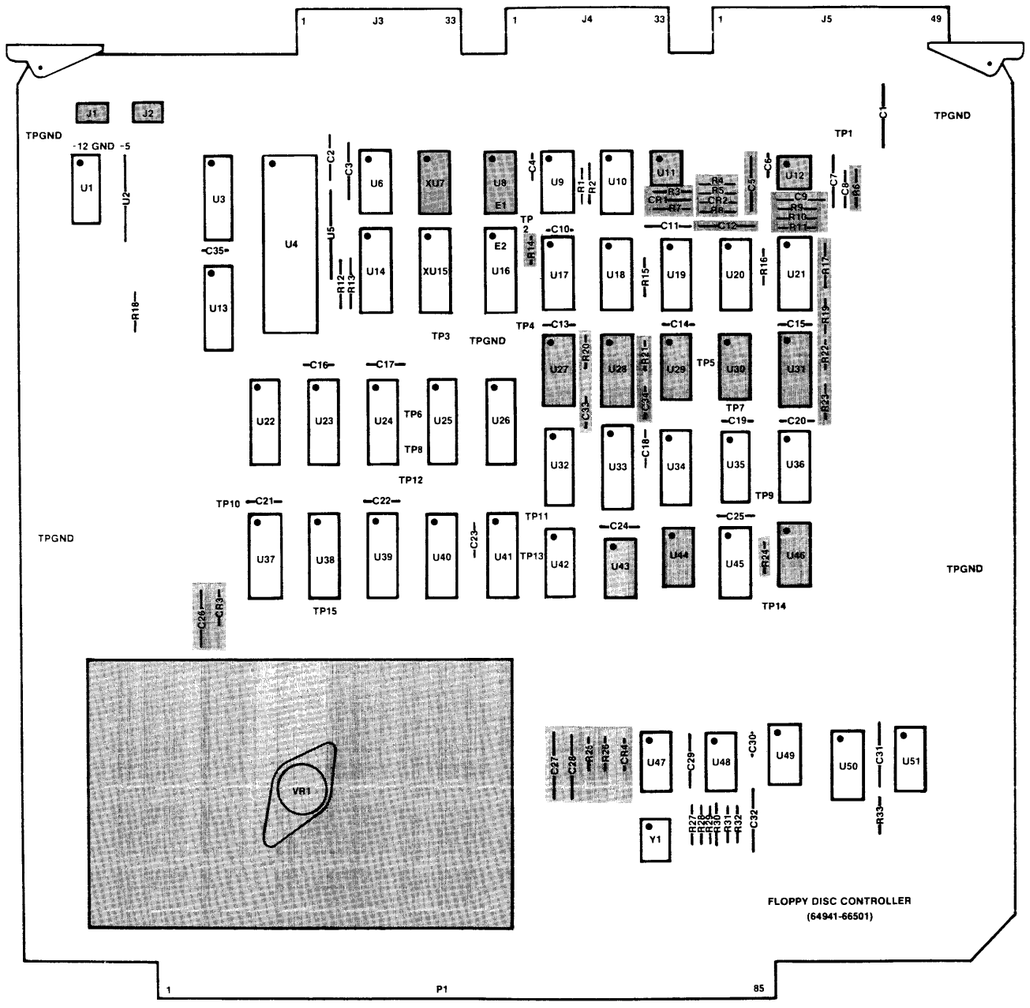
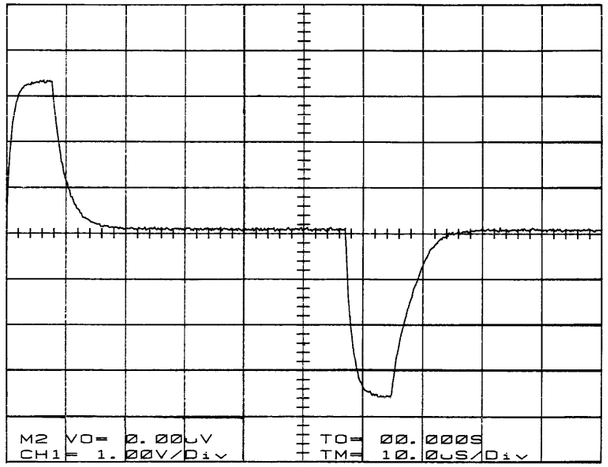
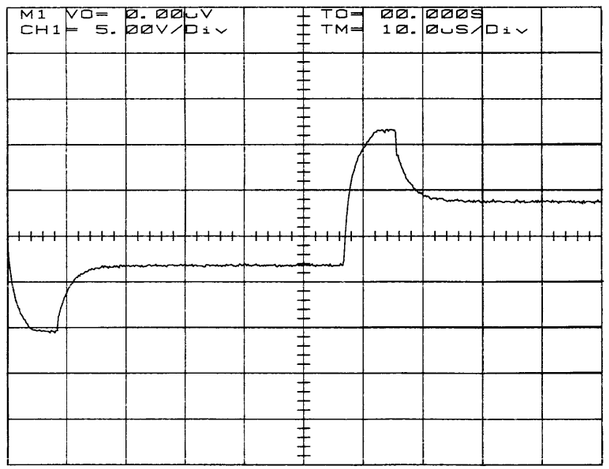


Figure 8-12. Component Locator and Block Diagram for Service Sheet 11C



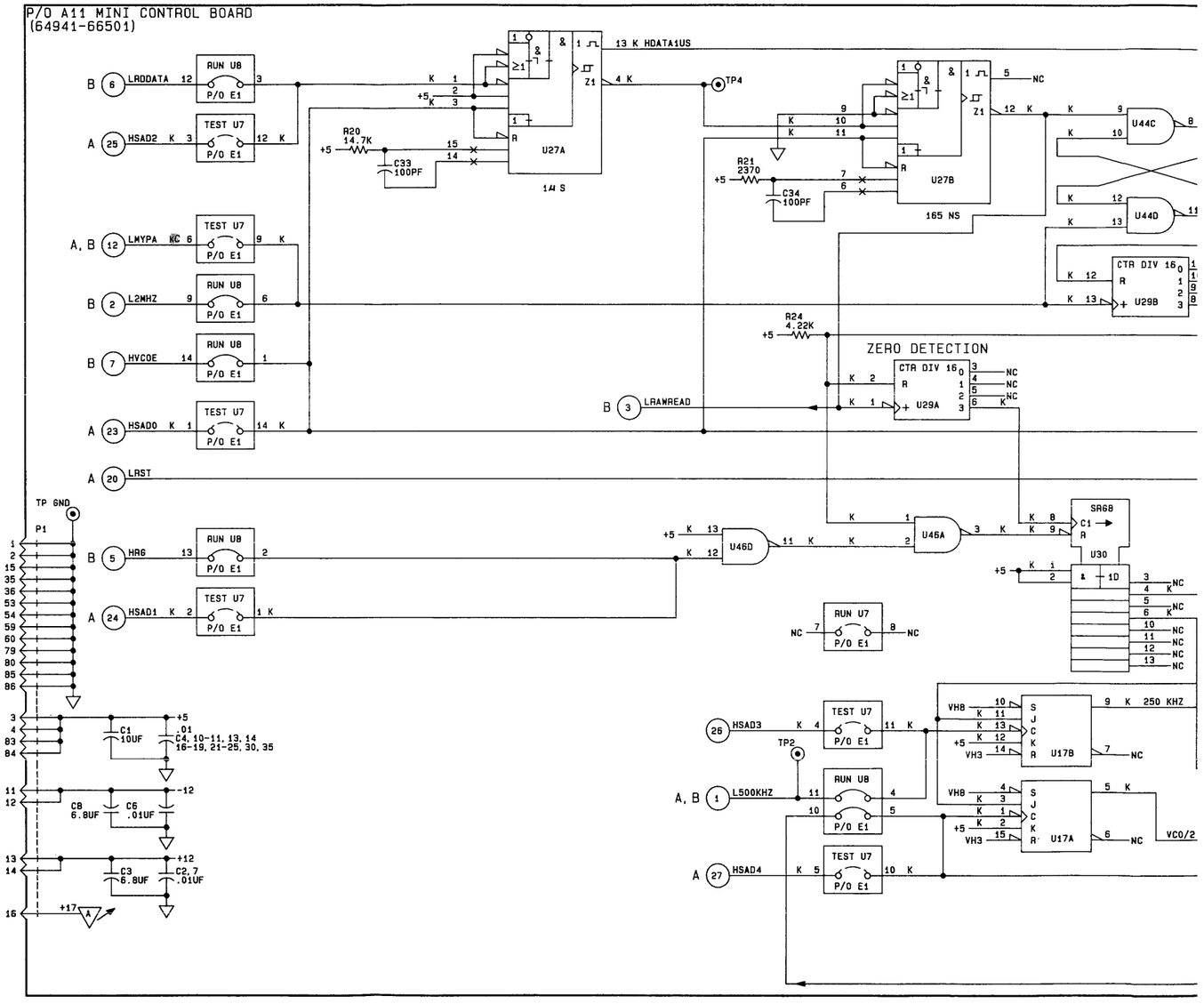
① AC COUPLED
TRIG-INT, POSITIVE

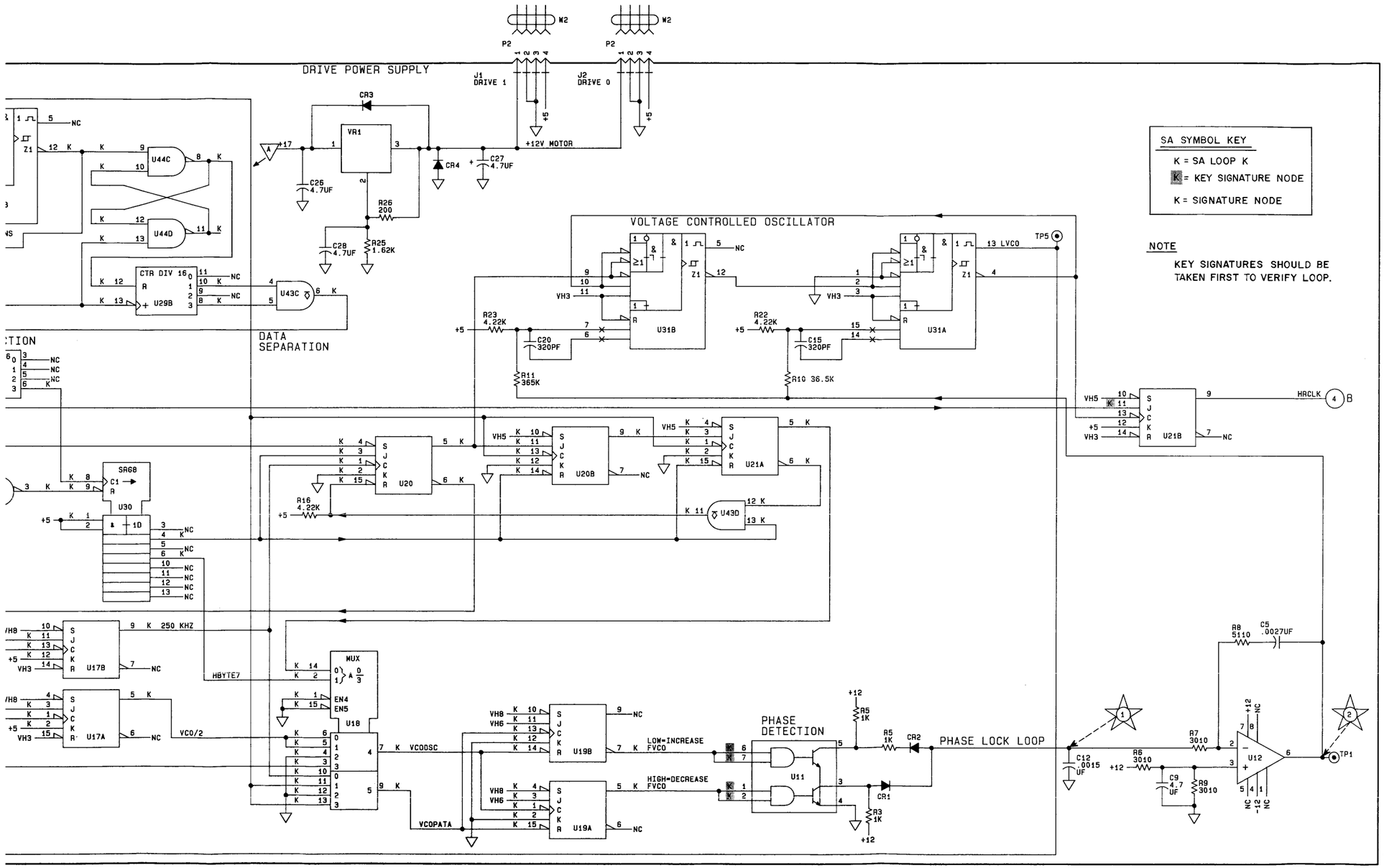
E1 TEST JUMPER IN XU7
PRESS DSA 2 SOFT KEY



② DC COUPLED
TRIG-INT, NEGATIVE

E1 TEST JUMPER IN XU7
PRESS DSA 2 SOFT KEY





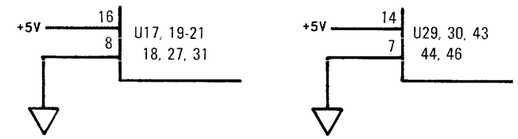
ICs ON THIS SCHEMATIC

Ref Des	HP Part No.	Mfr Part No.
U11	1820-0535	75451N
U12	1826-0207	LM318
U17, 19-21	1820-1212	74LS112
U18	1820-1244	74LS153
U27, 31	1820-1260	74221
U29	1820-1989	74LS393
U30	1820-1433	74LS164
U43	1820-1246	74LS09
U44, 46	1820-1197	74LS00
VR1	1826-0677	LM338

PARTS ON THIS SCHEMATIC

C1, 30, 33-35
CR1-4
E1
R3-9, 10, 11, 14, 15, 17, 19-26
V11, 12, 17-21, 27, 29-31, 43, 44, 46
VR1

POWER CONFIGURATIONS



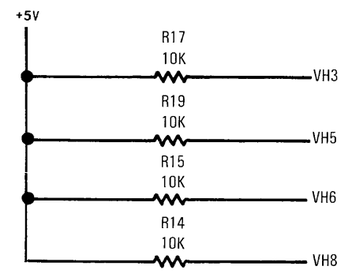


Figure 8-13.
Mini Control Service Sheet 11C
8-55

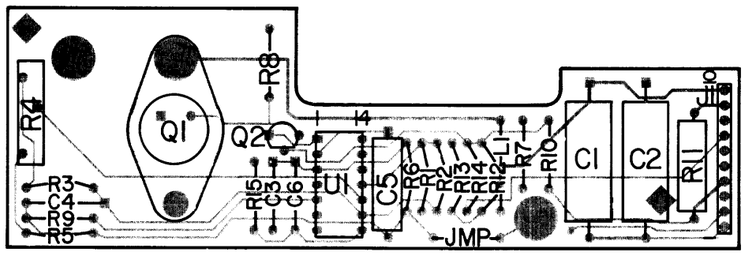


Figure 8-14. Component Locator for Service Sheet 1

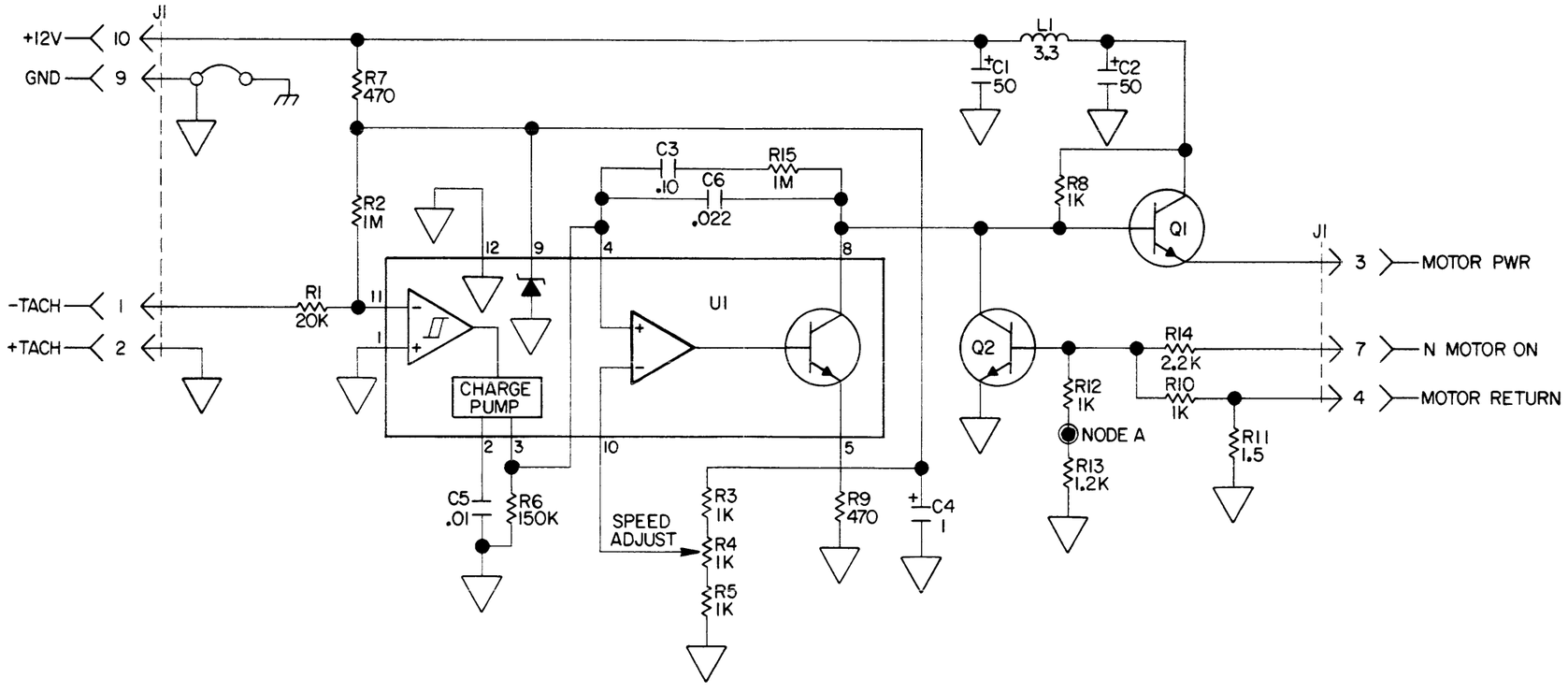


Figure 8-15.
Servo Electronics Service Sheet 1

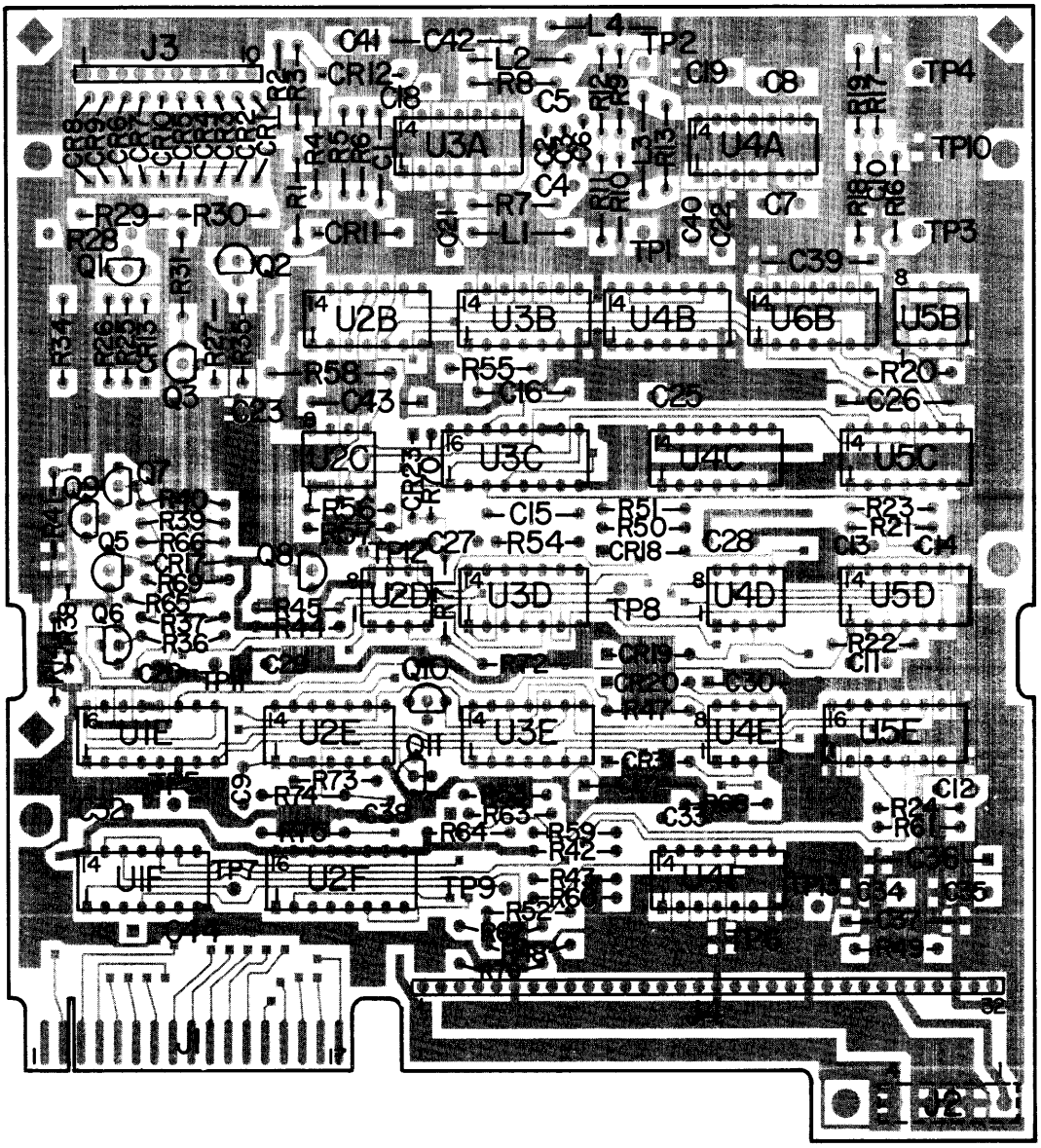


Figure 8-16. Component Locator for Service Sheet 2

NOTES:
1. COMPONENT NOT ON TANDON BOARD.
2. COMPONENTS ON TANDON BOARD ONLY.
3. R31 IS 768Ω ON TANDON BOARD.

Figure 8-17.
Drive Electronics Service Sheet 2
8-59

64941-90902, APRIL 1983
Replaces: 64941-90902, February 1982

PRINTED IN U.S.A.