64000

HP64000 Logic Development System

Model 64215A 6809 Emulator Pod

HEWLETT PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard system product is warranted against defects in materials and workmanship for a period of 90 days from date of installation. During the warranty period, HP will, at its options, either repair or replace products which prove to be defective.

Warranty service of this product will be performed at Buyer's facility at no charge within HP service travel areas. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses. In all other cases, products must be returned to a service facility designated by HP.

For products returned to HP for warranty service. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

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THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

CW&A 2/81

SERVICE MANUAL
MODEL 64215A
6809 EMULATOR

REPAIR NUMBERS

This manual applies directly to Model 64215A Emulator Pods with repair numbers prefixed 2250A. For more information about repair numbers see Section I, paragraph 1-3.

Manual Part Number 64215-90902
Microfiche Part Number 64215-90802

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SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

SS-1-1/76

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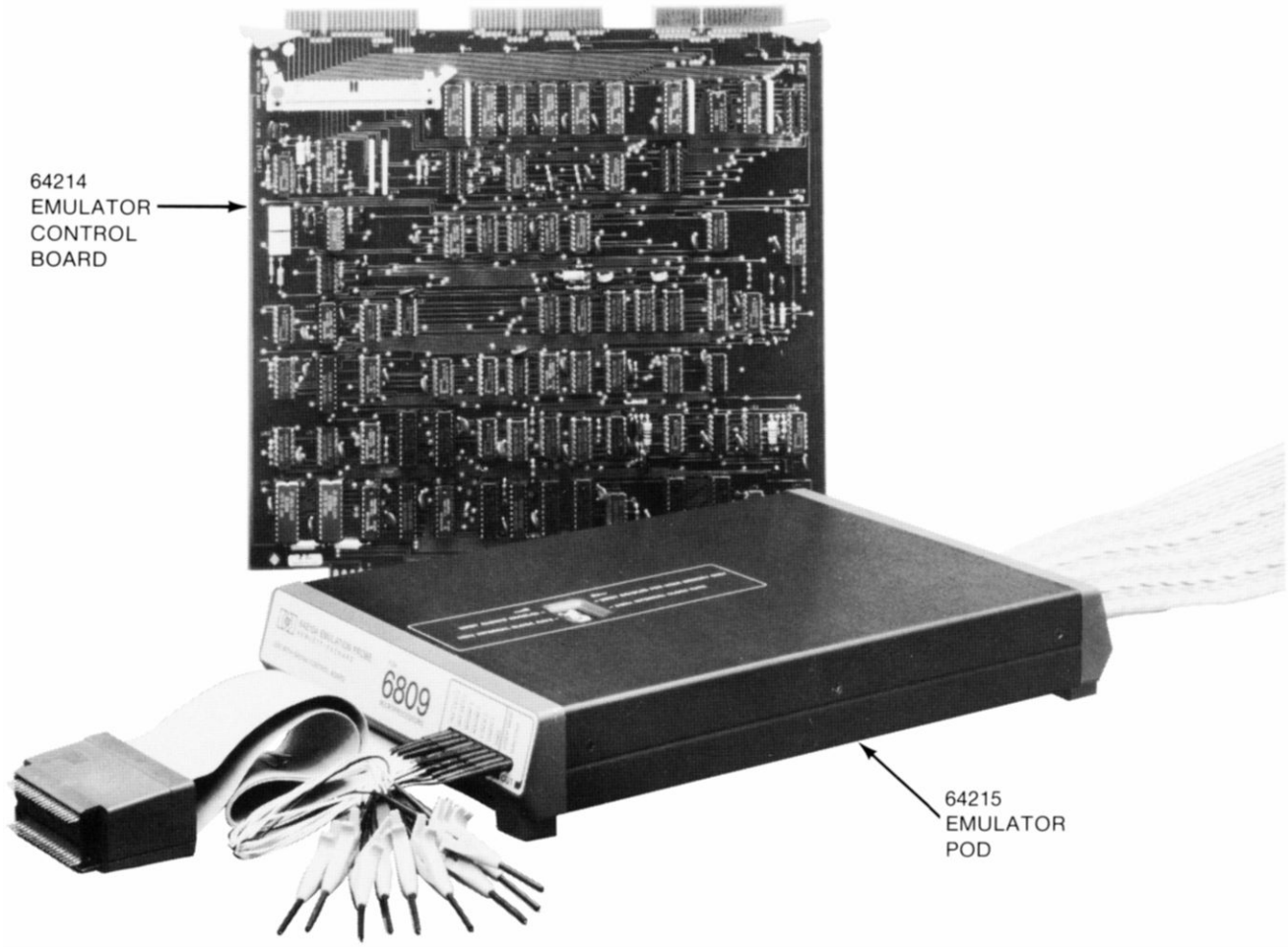


Figure 1-1. 6809 Emulation Subsystem

SECTION 1

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual contains preliminary information concerning the installation, maintenance, and troubleshooting for the Model 64215A 6809 Emulator Pod used in the 64000 Logic Development System.

1-3. This manual is organized with eight sections: Section I gives a brief physical and functional description. Section II contains installation and removal procedures. Section III refers to another manual for Operation information. Section IV includes Performance Verification and troubleshooting data. Section V describes adjustments Section VI lists replaceable parts. Section VII is for future manual changes. Section VIII contains service data, including the component locators and the schematics.

1-4. INSTRUMENTS COVERED BY THIS MANUAL.

1-6. Attached to the instrument or printed on the printed circuit card is the repair number. The repair number is in the form: 0000A00000. It is in two parts; the first four digits and the letter are the repair prefix and the last five are the suffix. The prefix is the same for all identical instruments. The suffix is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the repair number prefixes listed under REPAIR NUMBERS on the title page.

1-7. An instrument manufactured after the printing of this manual may have a repair prefix that is not listed on the title page. This unlisted repair number prefix indicates that the instrument is different from those described in this manual. Updating the manual for this newer instrument is accomplished by a manual changes supplement. The supplement contains "change information" that explains how to adapt this manual for the newer instrument.

1-8. In addition to change information, The supplement contains information for correcting errors in this manual. To keep this manual as current as possible, Hewlett-Packard recommends that you periodically request the latest manual changes supplement. The supplement for this manual is identified with the manual print date and the part number, which both appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-9. For information concerning a repair number prefix that is not listed on the title page or in the manual changes supplement, contact your nearest Hewlett-Packard Office.

1-10. DESCRIPTION.

1-11. The 6809 Emulator consists of a Model 64214A Emulator Control Board and the Model 64215A 6809 Emulator Pod. The Model 64214A Emulator Control Board is installed within the 64000 mainframe. The 6809 Emulator Pod consists of a user plug which contains an oscillator circuit and replaces the user's microprocessor in the target system, the pod assembly, and the interconnecting cables. The pod assembly contains two printed circuit boards, the Processor Board and the Synchronizer Board.

CAUTION

Before installing the user plug into the target system read the installation instructions in Section II of this manual. Damage to the emulator pod may result if the user plug is inserted improperly.

1-12. The Processor Board in the emulator pod houses the emulation microprocessor, and the buffers, timing, and control circuits which provide the interface to the user's target system and to the Emulator Control Board. A microprogrammed sequencer on the Synchronizer Board is used to develop intermediate timing for analysis and emulator control. The Emulator Control Board provides the interface to the optional memory and analysis functions and to the 64000 Development Station. The 64000 Development Station controls emulation functions through the interface with the Emulator Control Board.

1-13. ACCESSORIES SUPPLIED.

1-14. No accessories are supplied with the emulation pods.

1-15. ADDITIONAL EQUIPMENT REQUIRED.

1-16. The emulator pod requires a Model 64214A Emulator Control Board installed in a Model 64000A Development Station in order to complete a minimum configuration for in-circuit emulation.

1-17. POWER SUPPLY REQUIREMENTS.

1-18. The power requirements for the 6809 Emulation Subsystem are given in Table 1-1.

Table 1-1. Power Supply Requirements

	64214A	64215A	Total
+5 V	1.5 A	3.4 A	4.9 A
-5 V		Approx. 2 ma.	

No other voltages are used.

1-19. ELECTRICAL CHARACTERISTICS.

1-20. MAXIMUM CLOCK SPEED. The maximum clock speed of the 6809 emulator (without wait states) is 2 MHz.

1-21. EMULATOR POD TO TARGET SYSTEM INTERFACE. The following load characteristics are imposed on the target system by the emulator.

For all address, data and control lines the input and output characteristics are equivalent to low-power Schottky TTL levels and impedances plus approximately 20 pf.

A circuit is provided within the 6809 user plug, which will act as the oscillator for circuits which use the on-board oscillator of the 6809, or as a buffer for circuits using an external oscillator. This circuit meets Motorola 6809 specifications plus 20 pF.

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information for installing and removing the 6809 Emulator Pod. Included are initial inspection procedures and instructions for repacking emulators for shipment.

2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until contents of the shipment have been checked mechanically and electrically. If the contents are not complete, if there is mechanical damage or defect, or if the instrument does not pass the performance tests, notify the carrier as well as the Hewlett-Packard Sales/Service office. Keep the shipping materials for the carrier's inspection. The Hewlett-Packard Sales/Service office will arrange for repair or replacement at Hewlett-Packard option without waiting for claim settlement.

2-5. INSTALLATION.

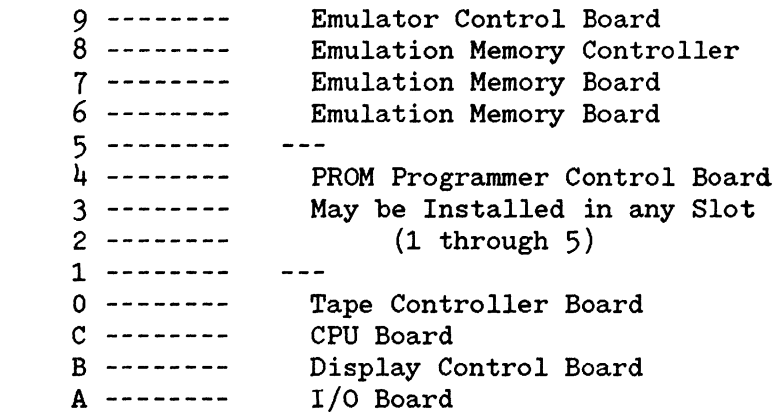
2-6. Figure 2-1 shows a top view of the 64100A mainframe card cage. The recommended slot for the emulator control board is the rearmost position. This maximizes the free cable length to the emulator pod.

WARNING

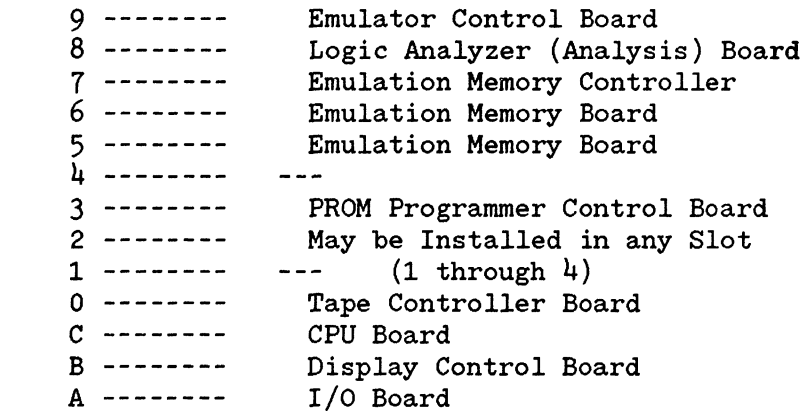
To prevent personal injury, refer to the safety requirements listed in the 64000 mainframe service manual before installing this option

CAUTION

Emulators must be installed and removed with the 64000 power turned off to prevent damage to the system.



A. EMULATION AND MEMORY



B. EMULATION/ANALYSIS AND MEMORY

Figure 2-1. Recommended Card Cage Configuration

2-7. To install the Emulator proceed as follows:

a. Turn 64100A power OFF

b. Loosen the two hold down screws and remove the card cage access cover.

c. Connect the selected emulator pod to the Emulator Control Board prior to the installation of the board in the card cage. This is done to simplify the connection of the multiconductor pod bus cables to the board. Two multicolored ribbon cables are used to connect the pod to the Emulator Control Board. One cable terminates in a female card-edge connector, the other terminates in a female socket-type connector. Pin 1 is indicated by a triangle molded into the body of each connector. The mating connectors for the cable connectors are located at the top left corner of the board as viewed from the component side. Pin 1 of the card-edge connector (J1) is indicated by a "1" etched into the board. Pin 1 of the connector block located directly below J1 (J4) is indicated by a triangle molded into the connector block. The connector block and the mating female connector on the cable have matching colored dots on their surfaces. The connector block is a latching type connector. Before installing the cable connector into the connector block insure that the latching tips are open (spread toward the outside edges of the board). Connect the card-edge connector first, then connect the socket-type connector to the connector block. Push the socket-type connector into the connector block until the latching tips snap over the top of the connector.

d. Grasp the board by the extractor levers located at the top of the card. Be very careful not to dislodge the cables. Hold the card with the component side toward the front of the development station and the card-edge connector labeled P1 toward the bottom of the card cage. Insert the card into the selected card slot guide rails, make sure P1 and the motherboard connector are aligned, and push the card down until seated firmly in the connector.

e. The bus cables supplied with the Emulator Control Board are used to connect to the optional Emulation Memory Controller. The bus cables are keyed so that they will seat on the edge connectors in only one position.

f. Stack the emulator pod cables flat through one of the cable slots at the back of the development station.

CAUTION

The following precautions should be taken while using Hewlett-Packard Emulator Pods. Damage to the emulator circuitry may result if these precautions are not observed.

POWER DOWN TARGET SYSTEM.

Turn off power to the user target system and the emulation development station before inserting the user plug to avoid circuit damage resulting from voltage transients or mis-insertion of the user plug.

VERIFY USER PLUG ORIENTATION.

Make certain that Pin 1 of the target system microprocessor socket and Pin 1 of the user plug are properly aligned before inserting the user plug in the socket. Failure to do so may result in damage to the emulator circuitry.

PROTECT AGAINST STATIC DISCHARGE.

The emulator pod contains devices which are susceptible to damage by static discharge. Therefore, operators should take precautionary measures before handling the user plug to avoid emulator damage.

CAUTION

NOTE

When the user plug is installed in the target system it is important to understand the output driving and input loading characteristics which the emulator system presents to the target system. These are presented in Section I of this manual.

2-8. REMOVAL.

2-9. Emulators are removed using the following procedure:

a. Turn the 64000 mainframe power OFF.

b. Remove the bus cables from the card.

c. Remove the Emulator Control Board from the card cage.

2-10. OPERATING ENVIRONMENT.

2-11. Emulators may be operated in environments within the following limits:

Temperature.....0°C to +40°C
Humidity.....5% to 80% relative humidity
Altitude.....4600 m (15 000 ft)

They should be protected from temperature extremes which cause condensation within the units.

2-12. STORAGE AND SHIPMENT ENVIRONMENT.

2-13. These units may be stored or shipped within the following limits:

Temperature.....-40°C to +75°C
Humidity.....5% to 80% relative humidity
Altitude.....15 000 m (50,000 ft)

2-14. PACKAGING.

2-15. ORIGINAL PACKAGING. Containers identical to those used in factory packaging are available through Hewlett-Packard offices.

2-16. OTHER PACKAGING. The following general instructions should be used for repacking with commercially available materials:

a. Wrap the unit in heavy paper or plastic.

b. Use a strong shipping container. A double-wall shipping container of 350 pound test material is adequate.

c. Use a layer of shock absorbing material 7- to 100 mm (3- to 4 inch) thick around all sides of the unit to provide firm cushioning and to prevent movement inside the container.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to the unit by model number and full repair number.

SECTION III

OPERATION

3-1. INTRODUCTION.

3-2. Operation of the 6809 Emulator is beyond the scope of this manual. Refer to the Emulator/Analyzer Operator's manual for an explanation of emulation and the use of the emulator subsystem.

SECTION IV

PERFORMANCE VERIFICATION

4-1. INTRODUCTION.

4-2. This section describes the Performance Verification for the 6809 Emulation Control Card. The scope of the Performance Verification is to detect problems at the board level only. Board level troubleshooting is in support of the Blue Stripe Program.

4-3. For convenience, the figures for the Performance Verification are grouped together at the end of this section.

4-4. RUNNING 64214A EMULATION PERFORMANCE VERIFICATION.

4-5. The Performance Verification (P.V.) for the 64214A 6809 Control Board is a subsection of the Option Test P.V. The Option Test P.V. tests all possible option modules that can be configured within the expansion slots of the Mainframe.

The option_test P.V. can either be run with a 64000 development station configured in a network arrangement (hard disk based); or it may be run from a 64000 station in a stand-alone configuration (mini disk based). When running the option_test performance verification on a Model 64214A Control board from a stand-alone 64000 configuration, the following modules must be present on the current local disk system:

FLOPPY_OP_SYS OPTION_TEST PV_EMUL_6809

4-6. To test the 64214A, proceed as follows:

a. With the operating system initialized and awaiting a command, use the softkey (or manually type the lower case command):

option_test RETURN

Refer to Figure 4-1.

b. The P.V. will now display a directory of the installed option boards and their card slot number (Figure 4-2). Locate the 6809 Controller - No Pod and enter the card slot number. For example, in Figure 4-2 the 64214A is in slot 9. Therefore, enter:

9 RETURN

c. A menu will now be displayed showing the test available to exercise the 64214A. This is the Mapper Control Test (refer to Figure 4-3). The following softkeys will appear at the bottom of the display:

<end>	Returns the user to the option test card slot listing.
<disp_test>	Advances the user to the detailed view of the mapper control test; that is, the test execution display.
<print>	Copies the display to the system line printer (if one is attached).

d. Press the <disp_test> softkey. This will advance the P.V. to the Control Board test execution display (refer to Figure 4-4). The following softkeys are listed at the bottom of the display:

<start>	Begins execution of the tests listed.
<exit_test>	Returns the user to the Mapper Control Test overview display described previously.
<print>	Copies the display to the system line printer (if one is attached).

e. To initiate testing of the 6809 Control Card, press the <start> softkey. The key will be highlighted in inverse video on the display and test execution will proceed. If all tests pass, testing can be terminated as described in the next paragraph. However, if any failures occur, refer to the description of the Control Board Test in the following sections.

f. Termination of testing on the 64214A is possible in one of two ways:

1) The <start> softkey may be pressed. The test will terminate at the end of the current test cycle and the start softkey on the display will return to normal video. To completely exit the performance verification from this point, press the <exit_test> softkey. This returns the user to the Mapper Control Test display. Press the <end> softkey while in this display. This returns the user to the option_test card slot listing, at which point the <end> softkey can be pressed to exit the performance verification software.

2) The <exit_test> softkey may be pressed. The test will terminate at the end of the current test cycle and the display will be returned to the Mapper Control Test overview display. At this point, the user may press the <end> softkey, returning the display to the option_test card slot listing level. When the <end> softkey is pressed at this point, the option_test performance verification is completely exited and the display is returned to the "Awaiting command" status.

4-7. PERFORMANCE TESTS.

4-8. Five groups of tests are included in the 6809 PV: the Processor Control Tests, Parts 1 and 2, the Emulation Bus Tests, the Foreground Tests, and the Analysis Stimulus Tests. Each segment of a test exercises a selected function of the emulator. The tests should be run in the sequence they are given to ensure the results are valid. The following paragraphs provide a brief description of each test.

4-9. TEST ERROR COUNTS. The performance test displays include two columns labeled # Fail and # Test. The # Fail column increments for each pass of a test in which an error is detected. The # Test column increments for each pass of a test which is executed.

4-10. STATUS DISPLAY. The processor control tests and the foreground tests use a status display to report the results of certain tests. This display reports the results of comparisons of the expected test results with the actual test results. It is not a display of the current status of these bits. These bits are numbered to correspond to the numbered bits of the Emulator Status register 5100.

```
          5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0
Status= 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
                                                Status Error
                                                Indicated
        - - - - - - - - - - - - - - - - 1       RESET
        - - - - - - - - - - - - - - - 1 -       BA
        - - - - - - - - - - - - - - 1 - -       XFER
        - - - - - - - - - - - - - 1 - - -       MRDY
        - - - - - - - - - - - - 1 - - - -       HALT
        - - - - - - - - - - - 1 - - - - -       BREQ
        - - - - - - - - - - 1 - - - - - -       SISR
        - - - - - - - - - 1 - - - - - - -       HISR
        - - - - - - - - 1 - - - - - - - -       BKG INT
        - - - - - - - 1 - - - - - - - - -       MEM BRK
        - - - - - - 1 - - - - - - - - - -       ILLOP
        - - - - - 1 - - - - - - - - - - -       BKG
        - - - - 1 - - - - - - - - - - - -       CLOCK
        1 1 1 - - - - - - - - - - - - - -       JAM INTERRUPT
        VECTOR
                                                (A3,A2,A1)
```

4-11. PROCESSOR CONTROL TEST-PART 1.

4-12. The Processor Control Tests-Part 1 check the ability of the mainframe processor in the development station to control the emulator. Each of the major control functions is tested and the background memory is checked. Tests included in the Processor Control-Part 1 tests are; the Reset Test, the Background test, the Release Test, and the Run Test. A failure detected by any of these tests indicates a problem in the emulator control board or the pod Processor board except for failures in HISR or SISR status. HISR and SISR status errors indicate the pod Synchronizer Board may have failed.

4-13. RESET TEST. The Reset Test performs a preliminary check of the status reporting capabiltity of the emulator. The mainframe processor resets the emulator and then reads the status reported back. The test results are then compared to the expected results.

4-14. BACKGROUND TEST. This test checks the background memory. In the Reset Test segment, the mainframe processor writes a data pattern to the background memory, while the emulation processor is held reset. The data is then read back and compared to the expected results. In the Not Reset test the identical memory test is performed again while the emulation processor is executing a short program. When the Background Test fails, the results of the following tests may not be valid. The test results are displayed as the address and the data received as a result of the memory test.

4-15. RELEASE TEST. The release test verifies that the emulator can be released to run programs in the background memory. A short program which modifies the contents of a memory location in the background memory is loaded into the background memory. The emulator is released to run the program and then the location is checked to verify that the memory contents of that location were changed. The error indication from this test is a status word equal to the data read from the memory location.

4-16. RUN TEST. A short program is loaded into the background memory and executed. The program is then modified causing a branch to a memory test. Failures occur when the background program is not successfully modified during the program run. The test returns the address error from the memory test. The status display contains the address which failed in the memory test.

4-17. PROCESSOR CONTROL TEST-PART 2.

The Processor Control Test-Part 2 tests check other emulator functions. These tests include the Background Interrupt, the Illegal Opcode Test, the Slow Clock Test, and the Emulation Memory Test. The emulation memory test is unavailable if optional emulation memory is not installed.

4-18. BACKGROUND INTERRUPT TEST. The background interrupt test attempts to execute a single step command. If a background interrupt does not occur a failure is reported. A failure of this test indicates a problem in the control board.

4-19. ILLEGAL OPCODE TEST. An illegal opcode is loaded into the background memory and an attempt is made to execute the illegal instruction code with the illegal opcode detector enabled and disabled. The status display shown below is returned when a failure is detected.

```
Status = 1 1 1
         1 - -  Illegal Opcode Masking Failure.
                Emulator Control Board problem
                indicated.
         - 1 -  Illegal Opcode Detector failure.
                Pod Synchronizer or Control Board
                problem
                indicated.
         - - 1  Illegal Opcode Detector did not clear.
                Emulator Control Board problem
                indicated.
```

4-20. SLOW CLOCK TEST. A CWAIT instruction is executed from the background memory. In approximately one-half second the SLOW CLOCK status bit should set. Failures are reported as shown below.

```
Status = 1 1
         1 -   Slow Clock Detector Failure
         - 1   Clear Failed
```

Failures indicate a problem on the pod Synchronizer board or the Emulator Control Board.

4-21. EMULATION MEMORY TEST. The Emulation Memory Test checks the emulation RAM and the associated control, address and data lines. Two test segments are used: a Data Test and an Address Test. To begin the test the emulator is reset by the mainframe processor. The mainframe processor then writes data to the memory and reads it back. The test is repeated with a short program executing in background. Failures detected during the Reset Test indicate a problem on the Emulation Memory Controller Board. Failures detected during the Not Reset Test indicate a problem on the Emulator Control Board or the Emulation Memory Controller Board.

4-22. EMULATION BUS TEST.

4-23. The Emulation Bus Test verifies the operation of the emulation bus address and data lines. The emulation bus is used to connect the Emulator Control Board to the optional Memory Control and Logic Analyzer Boards. This test requires the successful completion of the Processor Control Tests for both the Emulator Control Board and the Static Memory Control Board PV. The Emulation Bus Test consists of two subtests: the Data Test, and the Address Test.

4-24. DATA TEST. The mainframe processor tests two blocks of emulation memory for this test. In the first part of the test the memory is loaded through the memory control board and read through the emulator control board. In the second part of the test the inverse pattern is written to memory through the emulation control board and read back through the memory control board. A failure indicates a problem in the emulator control or memory control boards, or in the the memory bus cables.

4-25. ADDRESS TEST. The Address Test operates similarly to the data test except a pattern of addresses is used and the data lines are assumed to be good. Any failure detected is reported as an address error and indicates the same sources for errors.

4-26. FOREGROUND TEST.

4-27. The Foreground Test checks the ability to emulate in foreground memory. The Foreground Test consists of seven subtests: the Release Test, the Run Test, the Processor Break Test, the Illegal Memory Reference Test, the Last Opcode Address Test, the Last Memory Address Test, and the SISR,XFER Test. A description of each tests is provided below.

4-28. RELEASE TEST. The Release Test loads a program into emulation memory and releases the emulation processor to execute the program. The program is designed to modify a specific memory location. The host processor waits a suitable amount of time and then checks to see that the memory location has been modified. A failure detected by this test indicates a problem on the pod Processor Board, the Emuator Control Board or the pod Synchronizer Board. The errror indication from this test is a status word equal to the data read from the memory location.

4-29. RUN TEST. For the Run Test, a program is loaded into emulation memory and the emulation processor is released to execute the program. The host processor monitors the emulator status during the program run. Status errors detected by the host processor indicate a problem on the pod Processor Board, Emulator Control Board or the pod Synchronizer Board.

4-30. PROCESSOR BREAK TEST. For the Processor Break Test a program is loaded into emulation memory and the emulation processor is released to execute the program. The host processor then tries to break the program run. The contents of the PC register and the status of the NMI occurance bit are checked. An error indicates a problem in the pod Processor Board, Emulator Control Board or the pod Synchronizer Board.

4-31. ILLEGAL MEMORY REFERENCE TEST. In the Illegal Memory Reference Test, the mainframe maps blocks of the available memory into RAM, ROM and Illegal Memory space. The emulation processor then executes programs which attempt to reference these areas of memory. The host processor monitors the operation and checks that the proper break and illegal reference status bits are reported. Failures detected by this test indicate a problem in the Memory Control Board or the Emulation Control Board.

4-32. LAST OPCODE ADDRESS. For the Last Opcode Address test the emulation processor executes programs which cause bit patterns to be stored in the last opcode register on the Emulator Control board. The host processor checks the address stored against the expected results. Errors indicate a problem on the Control Board or the pod Processor Board.

4-33. LAST MEMORY ADDRESS. This test is identical to the Last Opcode Address test except that the patterns are stored in the last memory address register.

4-34. SISR, XFER. The SISR, XFER test check the operation of the pod Synchronizer Board. The host monitors the operation of the SISR and XFER control lines while the emulation processor is running a test program. Any error detected indicates a problem on the pod Synchronizer Board or the Emulator Control Board.

4-35. ANALYSIS STIMULUS.

4-36. The Analysis Stimulus Test consists of four subtests: the Analysis Status test; the Measurement Complete Test; the Data Test; and the Address test. The purpose of this test is to verify the operation of the interface to optional Logic Analyzer. These tests require that the performance verification tests for the Logic Analyzer described in the Logic Analyzer Model 64300A manual, be successfully completed. All PV tests described above must also be completed. The Analysis Stimulus Test checks the interface with the optional Logic Analyzer and can only be executed when one is present.

4-37. ANALYSIS STATUS. The Analysis Status Test verifies the ability to store status information. When an error is detected a problem is indicated in the bus cable, the Logic Analyzer, or the Emulator Control Board.

4-38. MEASUREMENT COMPLETE. The Measurement Complete Test verifies the ability of the Logic Analyzer to stop the emulator on measurement complete, and the ability of the mainframe processor to recognize that the emulator has been stopped. Any failures detected indicate a problem with the Emulator Control Board, the bus cables or the Logic Analyzer.

4-39. DATA TEST. In the Data Test, the mainframe processor causes the emulator to provide predetermined data to the Logic Analyzer. The data captured by the Logic analyzer is then checked against the expected results. A failure indicates a problem in the Logic Analyzer or the bus cables.

4-40. ADDRESS TEST. The Address Test is similar to the Data test except a failure is assumed to be in the address lines. Any error indicates a problem in the Logic Analyzer or the bus cables.

4-41. MEMORY AND ANALYSIS BOARD PV.

4-42. The Emulation Bus and Foreground Tests of the memory controller board PV, and the Emulation Stimulus Test of the analysis board PV, cannot be used with the 6809 Emulation Subsytem. Figure 4-9 contains the PV Selection Menu Displays for the PV of both boards. The message "Select Slot #9 for Emulation Bus and Foreground Tests" appears in the memory board PV. The message "Select Slot #9 for Emulation Stimulus Tests" appears in the analysis board PV display.

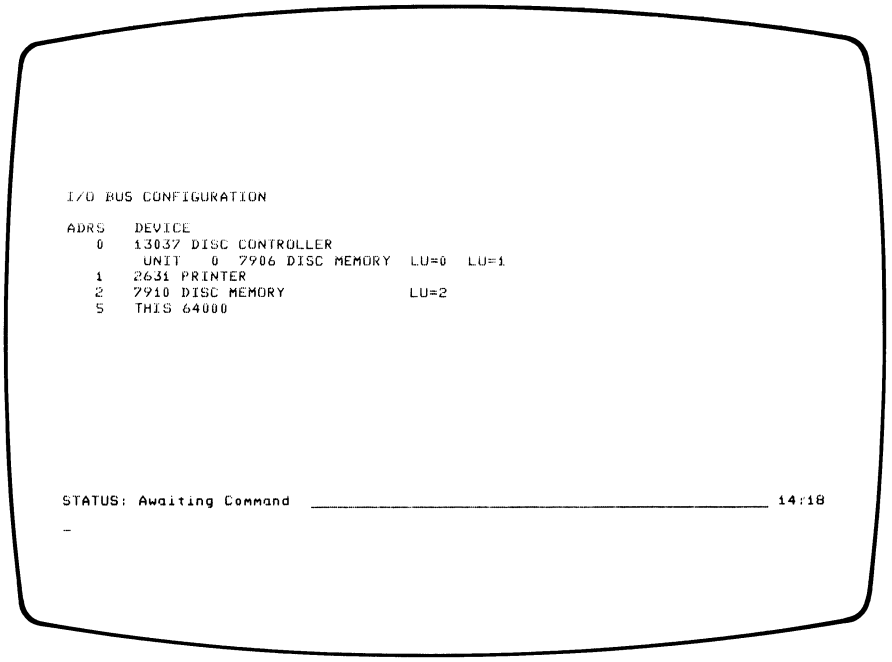


Figure 4-1. Awaiting Command Display

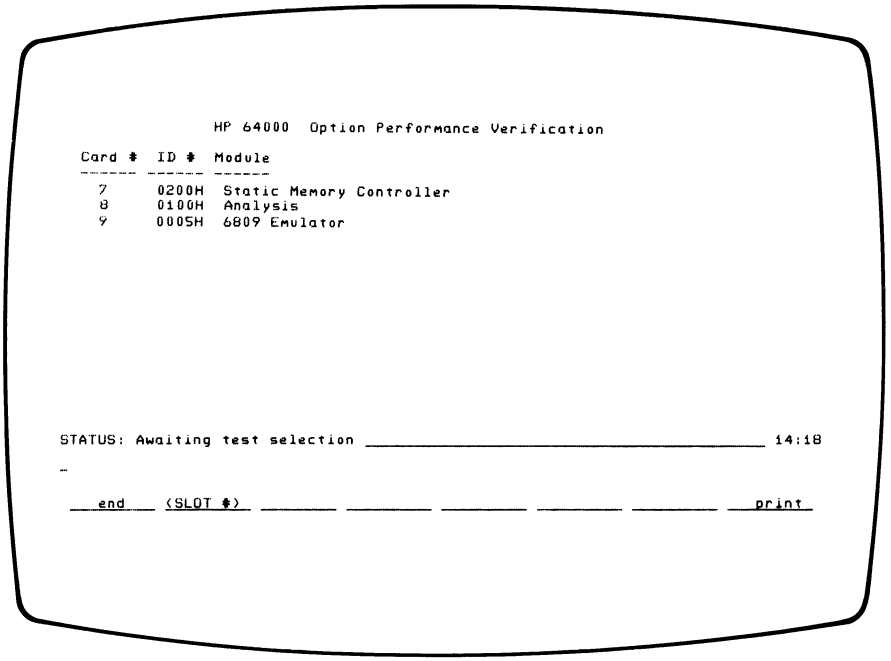


Figure 4-2. Option Map

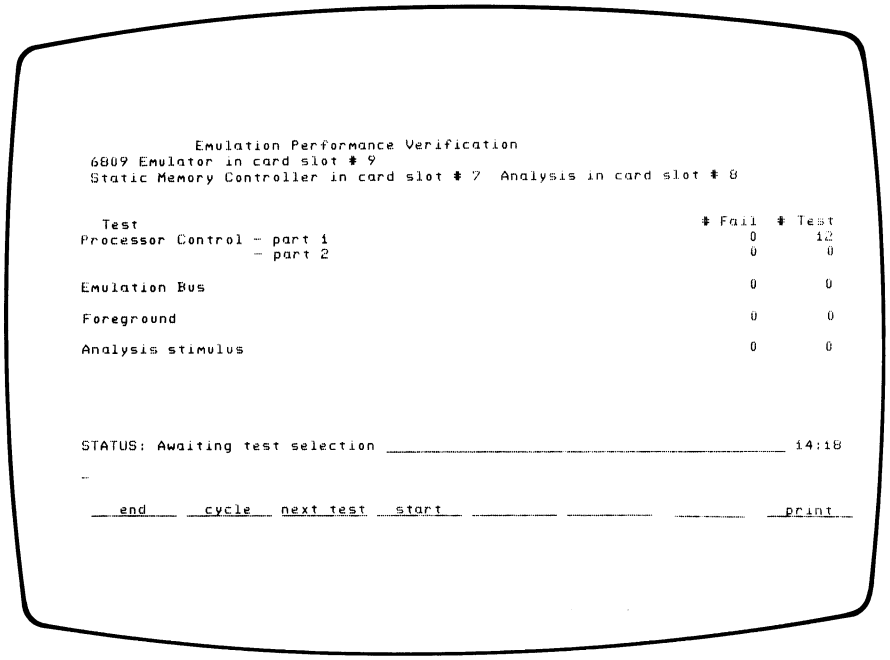
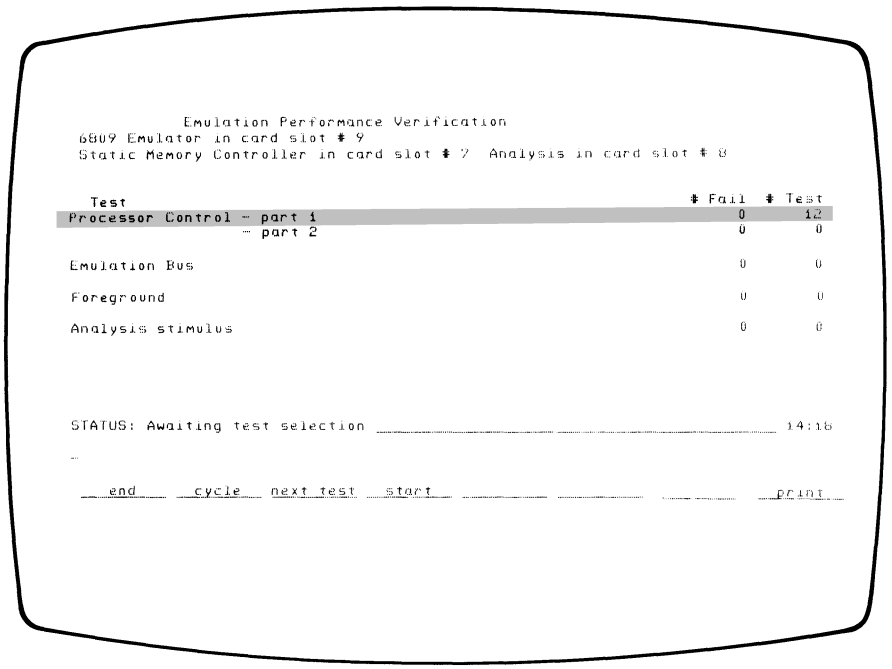
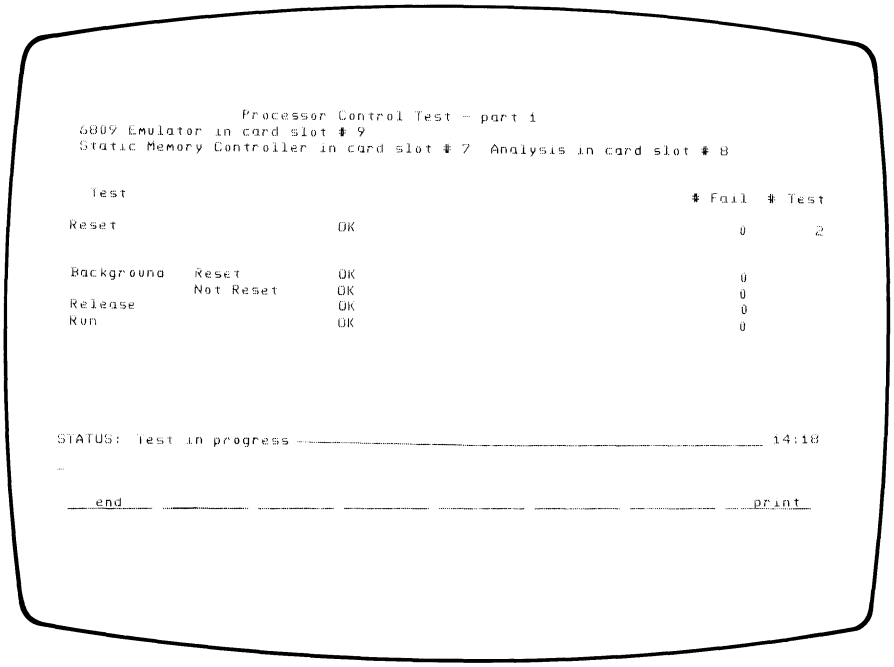


Figure 4-3. Emulator PV Menu

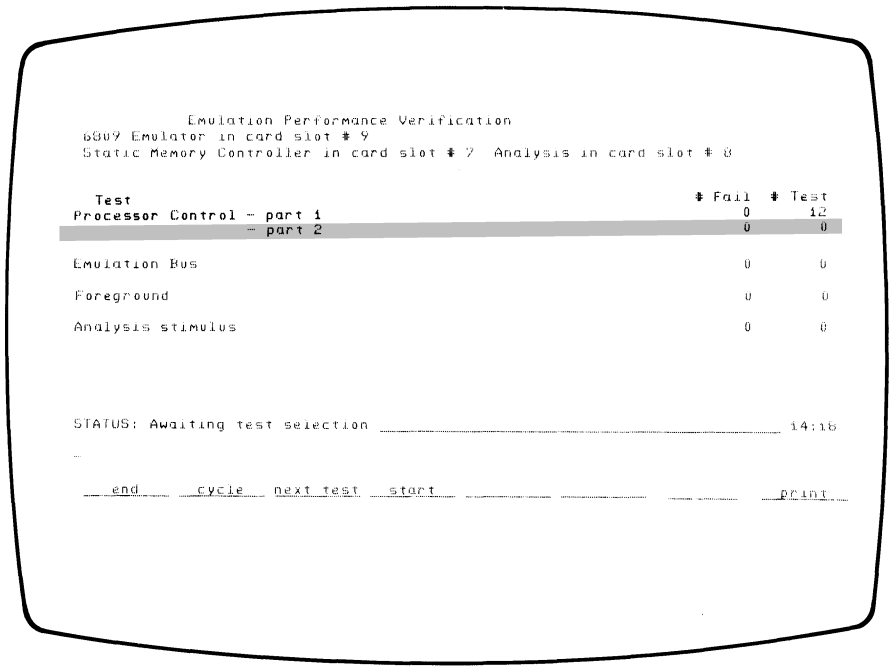


Entry Display

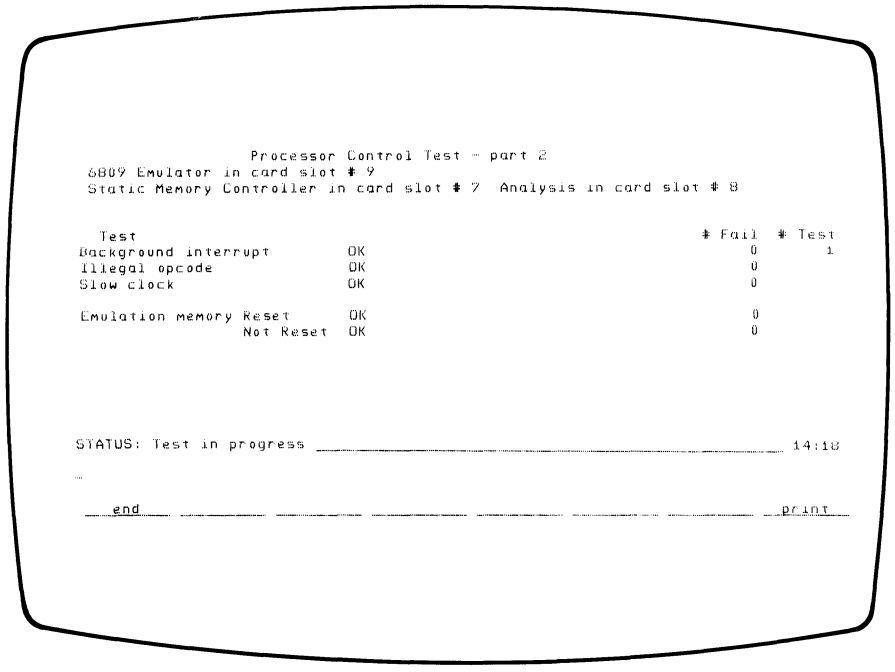


Test Summary

Figure 4-4. Processor Control Test-Part 1 Displays

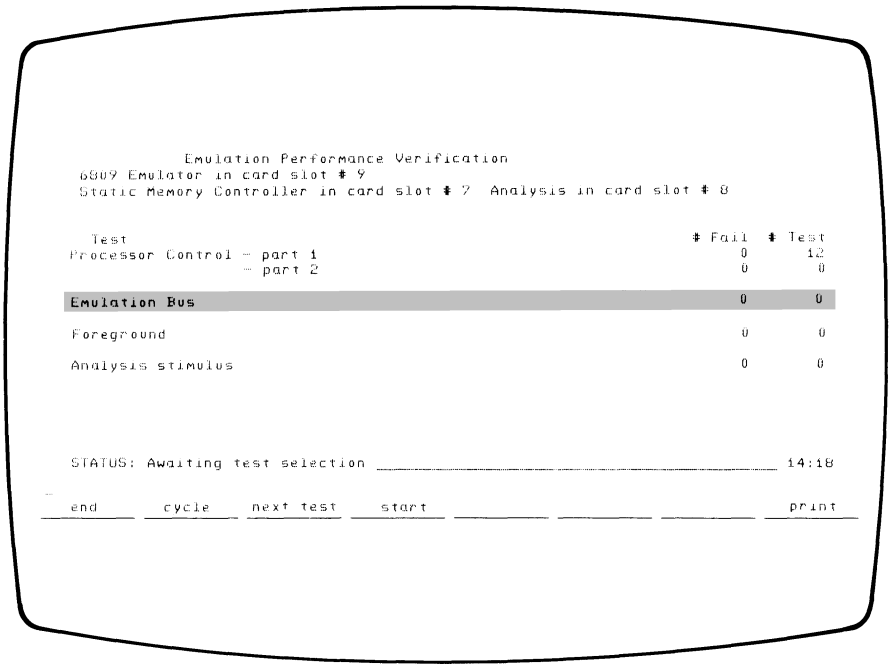


Entry Display

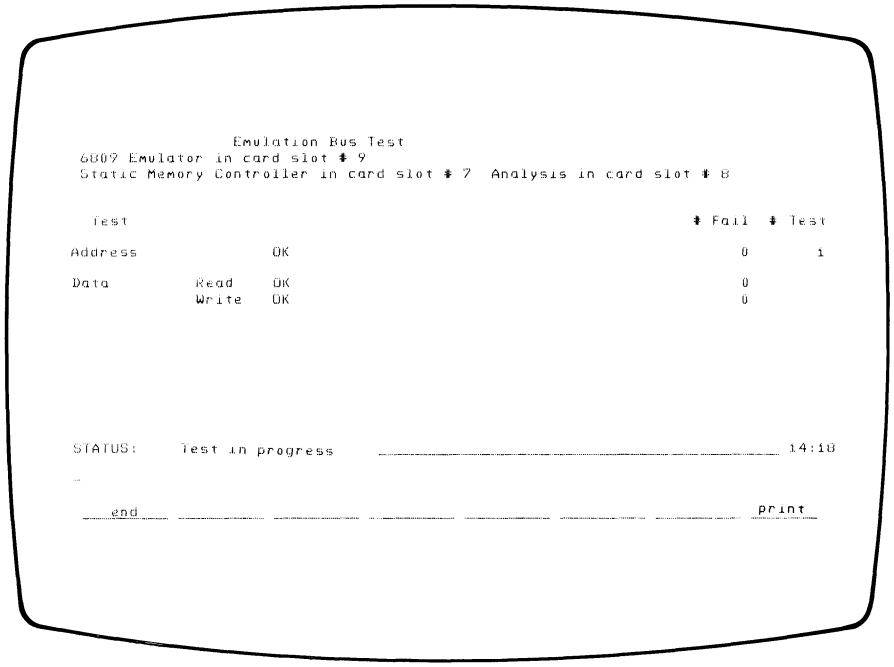


Test Summary

Figure 4-5. Processor Control Test-Part 2 Displays

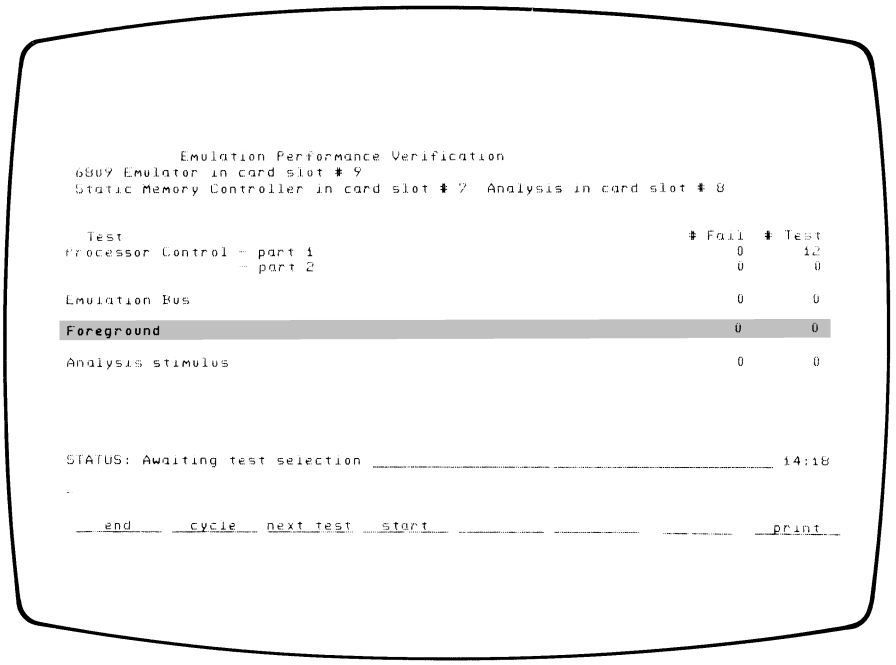


Entry Display

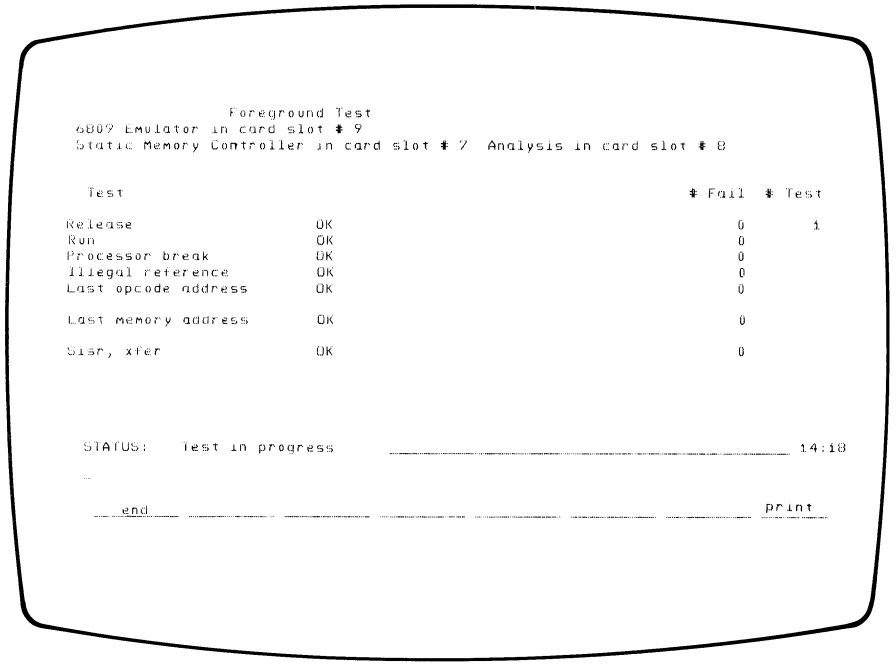


Test Summary

Figure 4-6. Emulation Bus Test Displays

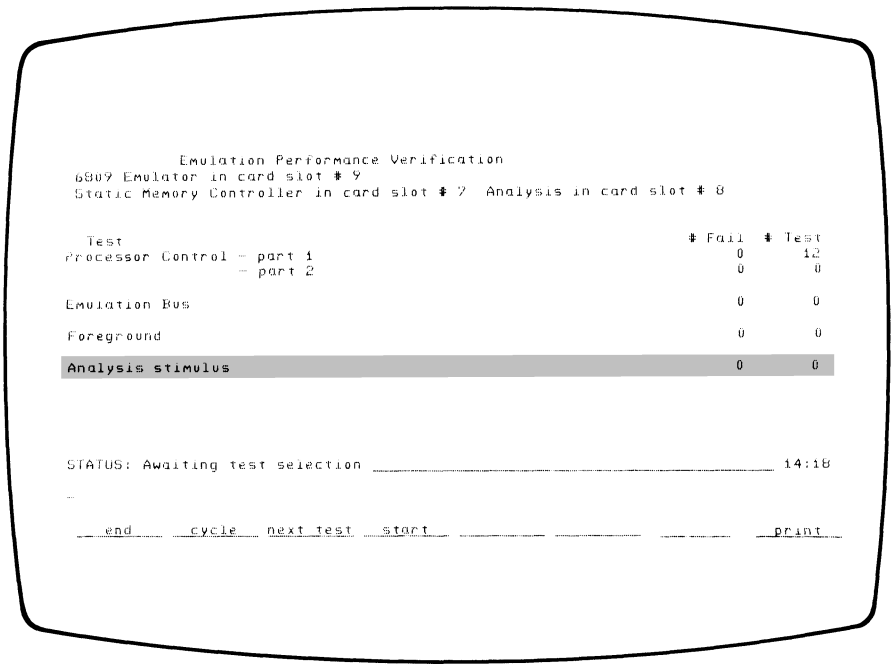


Entry Display

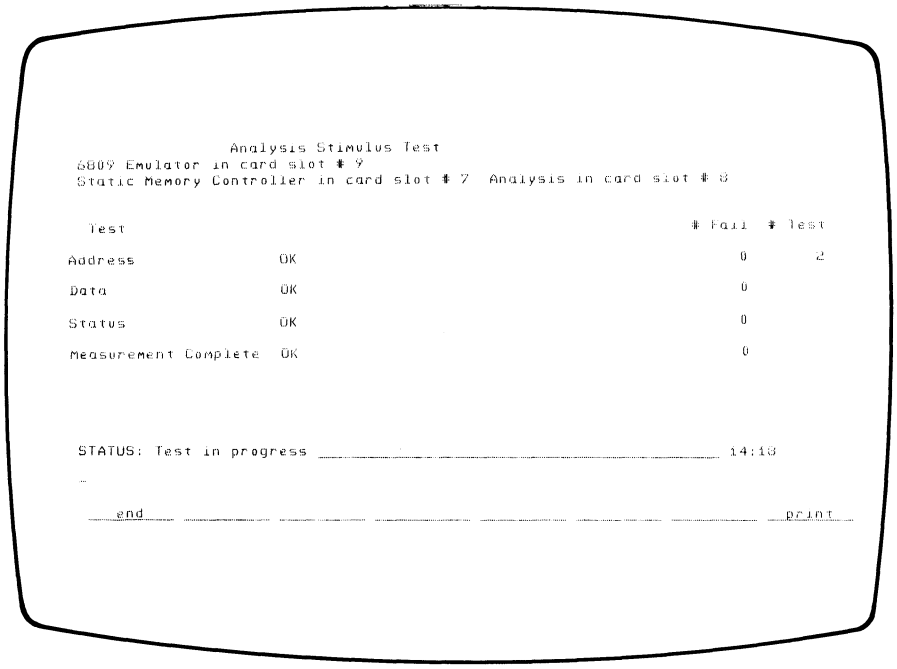


Test Summary

Figure 4-7. Foreground Test Displays

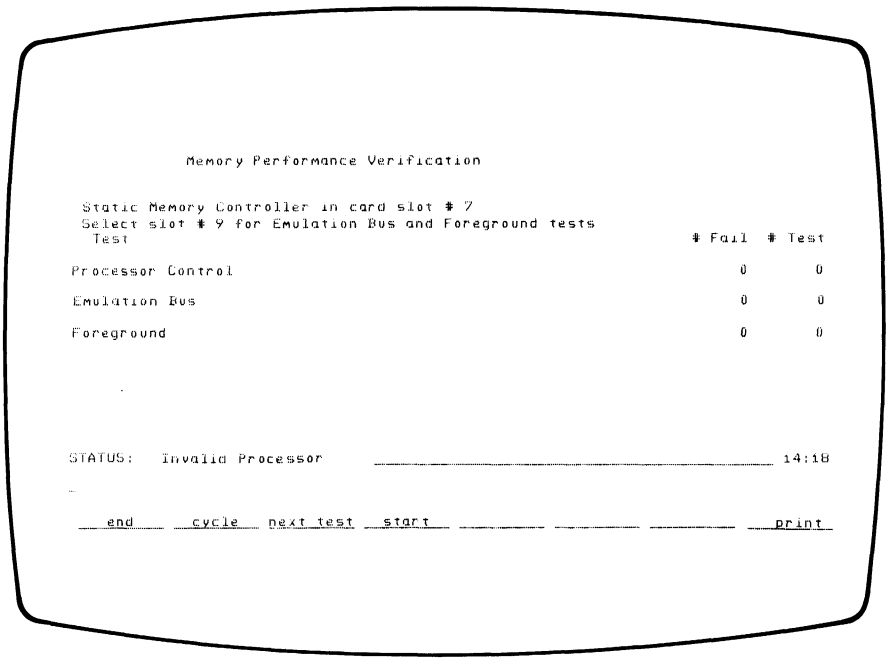


Entry Display



Test Summary

Figure 4-8. Analysis Stimulus Test



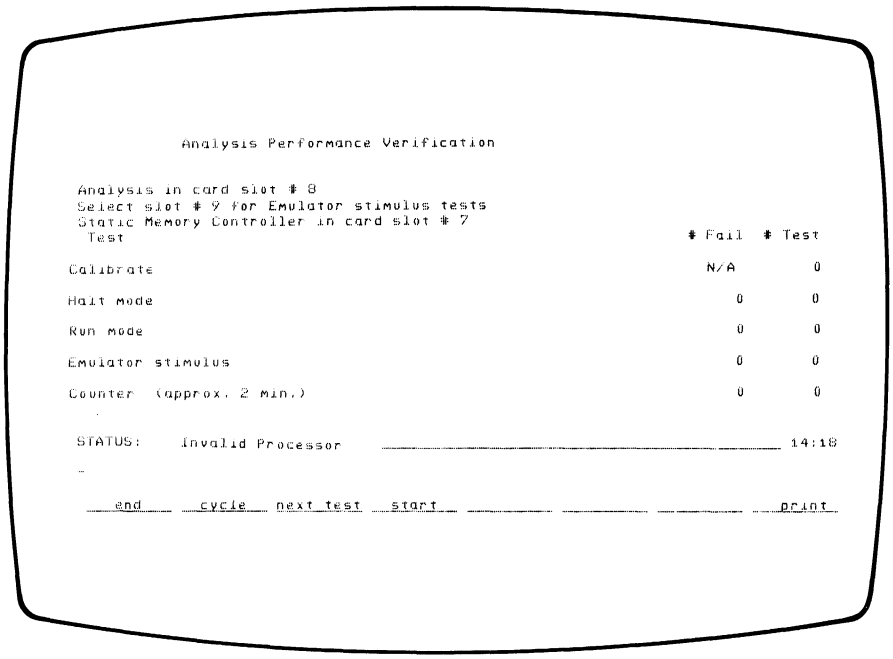


Figure 4-9. Memory and Analysis P.V. Displays

SECTION V

ADJUSTMENT

5-1. INTRODUCTION.

5-2. There are no adjustments to be made on the 6809 Emulator Pod.

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information needed to order replacement parts. Table 6-1 lists the Blue Stripe Program replaceable assemblies. Table 6-2 lists reference designators and abbreviations used throughout the manual. Table 6-3 lists the replaceable parts for the 6809 Emulator Pod. The replaceable parts are listed in assembly/reference designator order.

6-3. BLUE STRIPE PROGRAM.

6-4. The Blue Stripe Program offers factory repaired and tested re- placement boards, on an exchange basis only. Exchange assemblies carry a part number different from brand new assemblies and are available at a reduced cost. Exchange assemblies are available through the Hewlett-Packard Corporate Parts Center. Table 6-1 lists both the exchange and the new assembly Part Numbers for each printed circuit assembly.

Table 6-1. Blue Stripe Exchange Assembly Part Numbers

Board	Exchange	New
Processor Board	64215-69501	64215-66501
Synchronizer Board	64215-69502	64215-66502
Control Board	64214-69501	64214-66501

6-5. ABBREVIATIONS.

6-6. Table 6-2 lists the reference designators and abbreviations used in the parts list, the schematics and throughout the manual. Abreviations are always presented in upper case in the parts list. Abreviations using both upper and lower case letters are used in the schematics and other parts of the manual. This results in two forms of the abreviation. Table 6-2 lists only the upper case form of the abbreviation.

6-7. REPLACEABLE PARTS LIST.

6-8. Table 6-3 is the list of replaceable parts for the Model 64215A 6809 Emulator Pod. The parts list is organized as follows:

a. Chassis-mounted parts in alphanumerical order by reference designation.

b. Electrical assemblies and their components in alphanumerical order by reference designation.

c. Miscellaneous.

The information given for each part consists of the following:

a. The Reference Designator and Manufacturers Part Number.

b. The Hewlett-Packard Part Number.

c. The Quantity for the assembly.

6-9. ORDERING INFORMATION.

6-10. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number, indicate the quantity required, and address the order to the nearest Hewlett-Packard Sales/Service office.

6-11. To order a part that is not listed in the replaceable parts table include the instrument model number, instrument repair number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office. 6-12. DIRECT MAIL ORDER SYSTEM.

6-13. Within the USA Hewlett-Packard can supply parts through the direct mail order system. The advantages of using the system are as follows:

a. Direct ordering and shipment from the Hewlett-Packard parts center in Mountain View, California.

b. No minimum amount on any mail order (there is a minimum order amount for parts ordered through a local HP office when the order requires billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No-invoices. To receive these advantages, a check or money order must accompany each order.

6-14. Mail-order forms and specific ordering information are avail- able through your local HP office. Addresses and phone numbers are provided at the back of this manual.

Table 6-2. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without

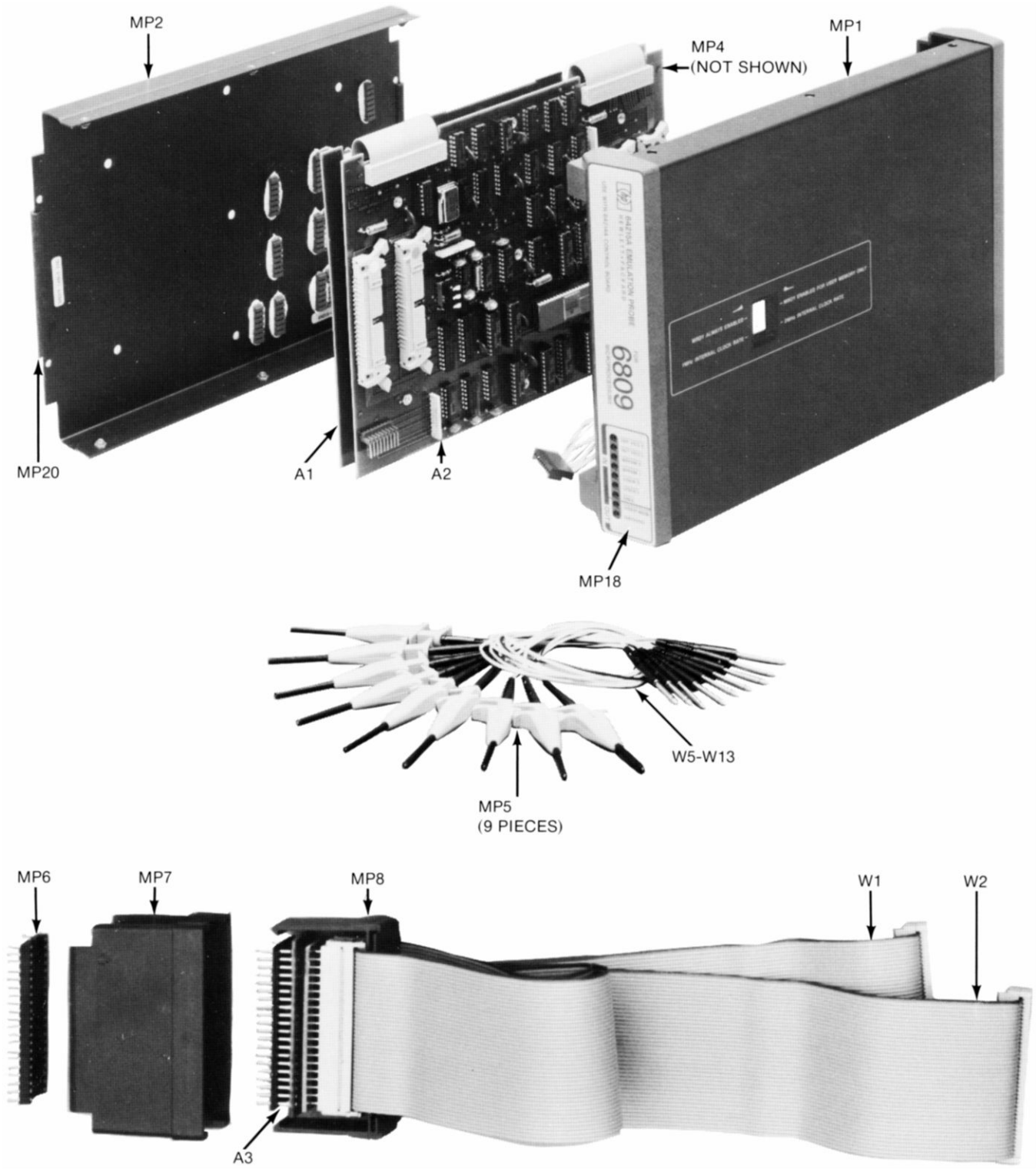
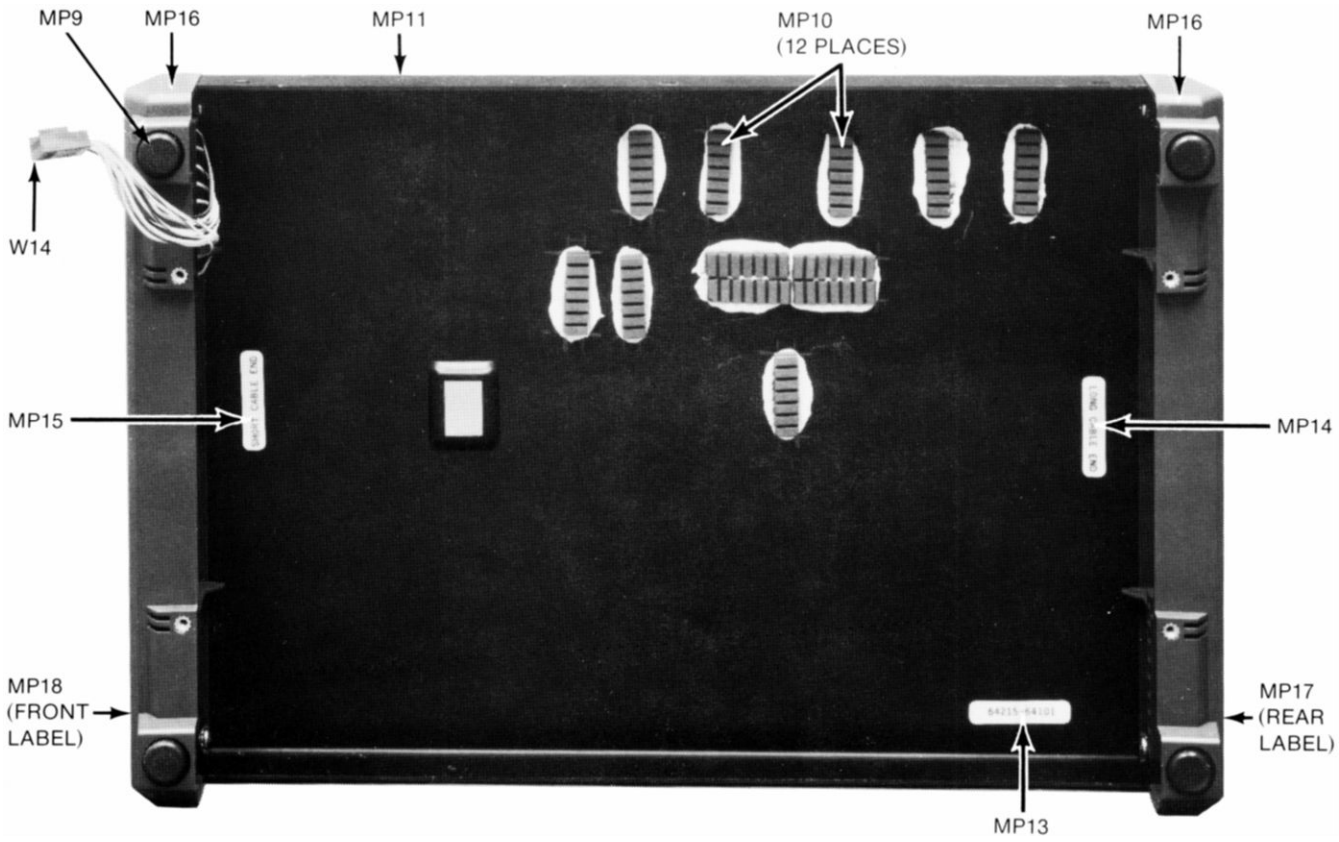
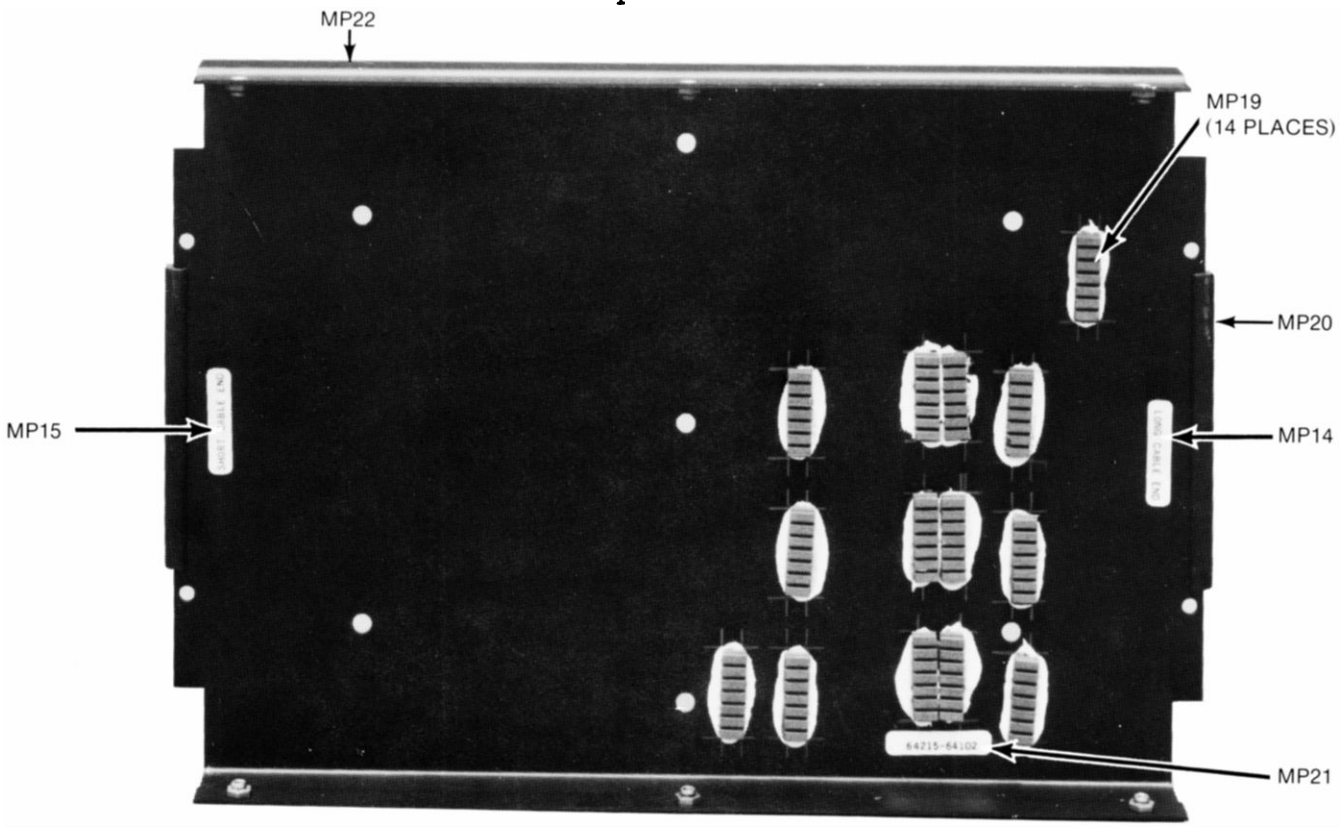


Figure 6-1. 6809 Emulator Pod Illustrated Parts Breakdown (Sheet 1)



Top Cover



Bottom Cover

Figure 6-1. 6809 Emulator Pod Illustrated Parts Breakdown (Sheet 2)

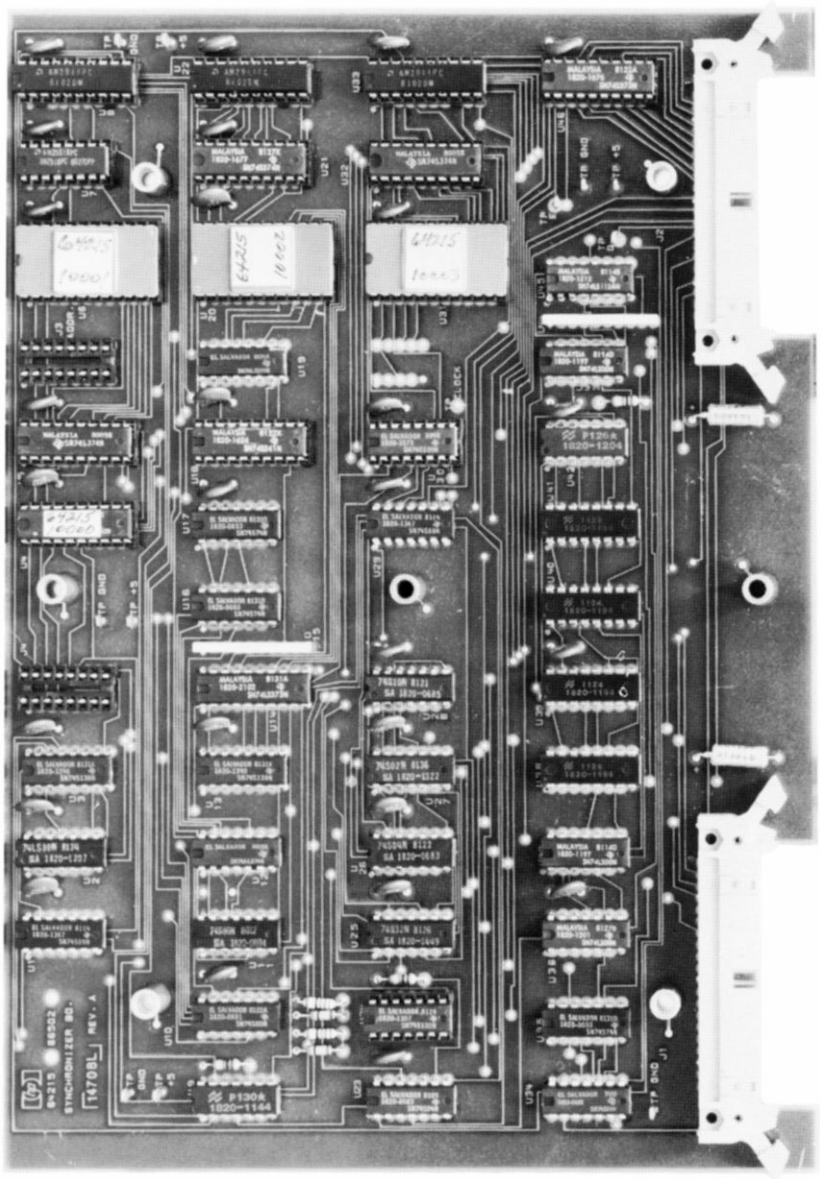


Figure 6-2. 6809 Emulator Pod Processor Board

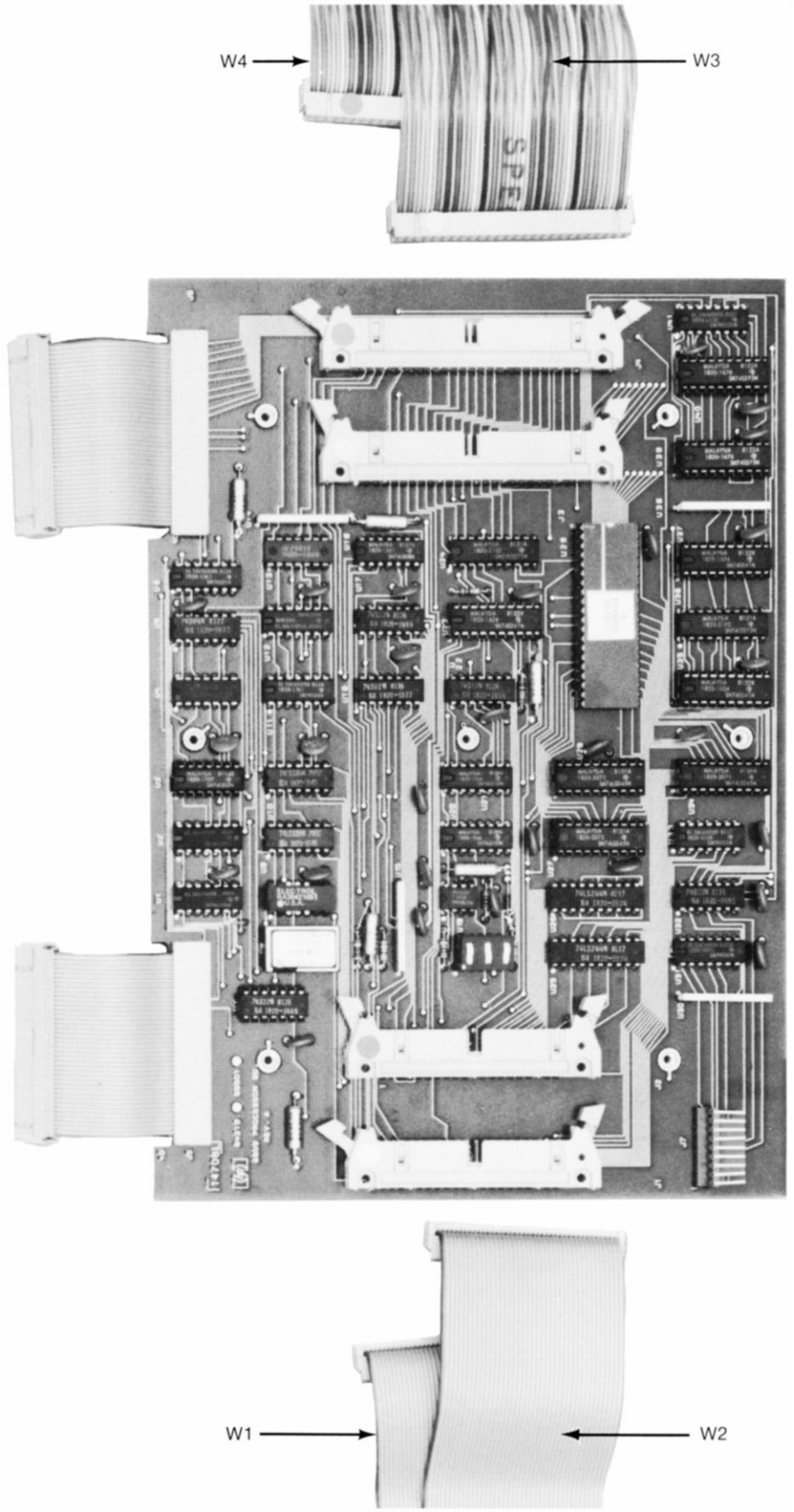


Figure 6-3. 6809 Emulator Pod Synchronizer Board

Table 6-3. 6809 Emulator Pod Replaceable Parts

Reference Designator	Description	Part Number	Quantity
	64215A		
MP4	GASKET-REF BLK	0905-0924	2
MP5	GRABBER ASSY	10230-62101	9
MP6	SOCKET 40 PIN AG	1200-0682	1
MP7	PIN BASE-PLUG	4040-1566	1
MP8	CLIP-TOP	4040-1574	1
W5	PROBE-LEAD ASSY	5061-1215	1
W6	PROBE-LEAD ASSY	5061-1217	1
W7	PROBE-LEAD ASSY	5061-1218	1
W8	PROBE-LEAD ASSY	5061-1219	1
W9	PROBE-LEAD ASSY	5061-1220	1
W10	PROBE-LEAD ASSY	5061-1221	1
W11	PROBE LEAD ASSY	5061-1222	1
W12	PROBE LEAD ASSY	5061-1223	1
W13	PROBE LEAD ASSY	5061-1224	1
W3	CBL-EMUL TMG	64215-61601	1
A3	BD ASY-ACTVE CKT	64215-62103	1
MP1	COVER ASY-TOP	64215-64101	1
MP2	COVER ASY-BOT	64215-64102	1
A1	BD ASY-SYNC 6809	64215-66502	1
A2	BD ASY-PCR 6809	64215-66501	1
W4	CBL-EMUL ADS	64232-61602	1
W1	CBL ASY-1	8120-3724	1
W2	CBL ASY-2	8120-3722	1
MP9	BUMPER PLASTIC	0403-0179	4
MP10	HEAT SINK-RUBBER	4040-1907	12
MP11	COVER-TOP 6809	64215-04101	1
W14	CBL-JPR 9 CDTR	64215-61603	1
MP13	LABEL-IDENT	64215-94301	1
MP14	LBL-LG CBL END	64222-94303	1
MP15	LBL-SH CBL END	64222-94304	1
MP16	END CAP-ASSY	64232-60201	2
MP17	LBL-GEN 16 BIT	7121-1780	1
MP18	LABEL-SPEC 6809	7121-2106	1
MP19	HEAT SINK-RUBBER	4040-1907	14
MP20	CHANNEL-RUBBER	4320-0095	.5500FT
MP21	LABEL	64215-94302	1
MP22	COVER-BOT 16 BIT	64242-04102	1

Table 6-3. 6809 Emulator Pod Replaceable Parts (Cont'd)

Reference Designator	Description	Part Number	Quantity
	A1		
C1-3,6-9,11,12,14-17,19,20,22-34	CF CE .01UF 100V	0160-2055	28
C10,18	CF TA 4.7U 50V	0180-1731	2
C4,5,13,21	CF TA 15U 20V	0180-1746	4
K1	RLY-REED IC	0490-0617	1
R7	RF.25CC 1000 5	0683-1025	1
R1	RF.12MF 100 1	0757-0401	1
R6	RF.12MF 562 1	0757-0417	1
R5	RF.12MF 2.43K 1	0757-0431	1
R4	RF.12MF 20K 1	0757-0449	1
R3	RF.12MF 51.1K 1	0757-0458	1
R2	RF.12MF 75K 1	0757-0462	1
XU8,3,4,7	SOCKET-IC 14 PIN	1200-0638	4
XU23,27,28,34,35,37,39,40	SOCKET-IC 20 PIN	1200-0639	8
XU29	SOCKET-IC 40P	1200-0654	1
XSW1	SOCKET-IC 10 PIN	1200-0945	1
MP1	POLARIZING KEY	1251-5595	8
J1,2	CONN-40 P MREJT	1251-5652	2
J3,4	CONN-50 P MREJT	1251-5653	2
J7	CONN-WAFER 9	1251-5968	1
U15,30	ID RES PACK	1810-0275	2
U14,38	RES NET SPEC S	1810-0430	2
U8	CRYSTAL-CSC 8 MHz	1813-0188	1
U19	IC LIN OP AMP	1820-0217	1
U31	IC 74S00	1820-0681	1
U5	IC 74S04	1820-0683	1
U32	IC 74S10	1820-0685	1
U41	IC 74S133	1820-1130	1
U33	IC 74S51	1820-1158	1
U3	IC 74LS00	1820-1197	1
U4	IC 74LS04	1820-1199	1
U18	IC 74LS08	1820-1201	1
U13	IC 74LS11	1820-1203	1
U20,21	IC 74LS153	1820-1244	2
U12	IC 74LS54	1820-1285	1
U16	IC 74S02	1820-1322	1
U6,11	IC 74S08	1820-1367	2
U7,17,22	IC 74S32	1820-1449	3
U23,35,37	IC 74S241	1820-1624	3
U9,10	IC 74LS126AN	1820-1645	2
U39,40	IC 74S373	1820-1676	2
U25,26	IC 74LS244N SLT	1820-2024	2
U27,28,34	IC 74LS245	1820-2075	3
U24,36	IC 74LS373	1820-2102	2
U1,2	IC 74ALS74	1820-2488	2
U29	IC MPU MC68B09L	1820-2770	1
CR1	DIODE SCHOTTKY	1901-0535	1
SW1	SWITCH SPDT	3101-2471	1
MP2	LBL-MADE IN USA	5957-2260	1
J5,6	CBL ASY-BD INTCN	64215-61602	2
MP3	LABEL-WHITE DOT	7120-8723	AR
MP4	LABEL-BLUE DOT	7124-0266	AR
MP5	LABEL-RED DOT	7124-0269	AR
MP6	LABEL-YELLOW DOT	7124-0270	AR

Table 6-3 6809 Emulator Pod Replaceable Parts (Cont'd)

Reference Designator	Description	Part Number	Quantity
	A2		
C1-29	CF CE .01UF 100V	0160-2055	29
C30,31	CF TA 4.7L 50V	0180-1731	2
TP1-12	TERMINAL-TEST PT	0360-2050	12
R1,6,7	RF .2500 1000 5	0683-1025	3
R3,5	RF .12MF 221 1	0757-0282	2
R2,4	RF .12MF 274 1	0757-0409	2
XU6,20,31	SOCKET 24 PIN	1200-0541	3
J3,4	SOCKET-IC 16 PIN	1200-0607	4
XU7,30	SOCKET-IC 16 PIN	1200-0607	4
XU24	SOCKET-IC 14 PIN	1200-0638	1
XU4,5,8,18,21,22,32,33,46	SOCKET-IC 20 PIN	1200-0639	9
MP1	POLARIZING KEY	1251-5595	4
J1,2	CONN-40 P MREJT	1251-5652	2
U15,44	IK RES PACK	1810-0275	2
U10	IC 74S00	1820-0681	1
U26,23	IC 74S04	1820-0683	2
U28	IC 74S10	1820-0685	1
U34	IC 74S20	1820-0688	1
U16,17,35	IC 74S74	1820-0693	3
U11	IC 74S86	1820-0694	1
U30	IC 74S139	1820-1072	1
U9	IC SN74LS02	1820-1144	1
U38-41	IC 74LS193	1820-1194	4
U37,43	IC 74LS00	1820-1197	2
U36	IC 74LS08	1820-1201	1
U42	IC 74LS20	1820-1204	1
U2	IC 74LS30	1820-1207	1
U45	IC 74LS112	1820-1212	1
U3,13	IC 74S138	1820-1240	2
U24	IC 74S132	1820-1307	1
U27	IC 74S02	1820-1322	1
U1,29	IC 74S08	1820-1367	2
U25	IC 74S32	1820-1449	1
U18	IC 74S241	1820-1624	1
U46	IC 74S373	1820-1676	1
U5,21,32	IC 74S374	1820-1677	3
U14	IC 74LS373	1820-2102	1
U8,22,33	IC 2911	1820-2260	3
U19	IC 74LS399	1820-2384	1
U7	IC BIT SLICE SUP	1820-2415	1
U12	IC 74ALS74	1820-2488	1
MP2	LBL-MADE IN USA	5957-2260	1
U4	INSTR-DECODER	64215-10000	1
U6	MICROCODE-MSE	64215-80000	1
U20	MICROCODE-MIDDLE	64215-80001	1
U31	MICROCODE-LSB	64215-80002	1

Table 6-3. 6809 Emulator Pod Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				A3		
A3A1	64215-66504	6	1	BOARD ASSEMBLY-GROUNDING	28480	64215-66504
A3A1J1	1251-5943	4	2	CONN-POST TYPE	28480	1251-5943
A3A1J2	1251-5943	4		CONN-POST TYPE	28480	1251-5943
A3A2	64215-66505	7	1	BOARD ASSEMBLY-ACTIVE CKT	28480	64215-66505
A3A2C1	0160-3647	7	2	CAPACITOR-FXD 22PF +/-5% 100VDC CER 0+/-30	28480	0160-3647
A3A2C2	0160-3647	7		CAPACITOR-FXD 22PF +/-5% 100VDC CER 0+/-30	28480	0160-3647
A3A2C3	0160-3470	2	2	CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A3A2C4	0160-3470	2		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A3A2C5	0650-3443	1	1	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A3A2J1	1251-7948	3	2	CONNECTOR-20PIN ROW	28480	1251-7948
A3A2J2	1251-7948	3		CONNECTOR-20PIN ROW	28480	1251-7948
A3A2J3	1525-7851	7	1	CONNECTOR-40 PIN HEADER	28480	1251-7851
A3A2P1-1 THROUGH A3A2P1-40	1200-0475	0	40	CONNECTOR-SGR CONTSKT .017-IN-BSC-SZ	28480	1200-0475
A3A2R1	0698-3113	1	1	RESISTOR 100 5% .125W CC TC=-270/+540	01121	BB1015
A3A2R2	0698-5426	3	1	RESISTOR 10K 10t .125W CC TC=-350/+857	01121	BB1031
A3A2R3	0675-1021	8	1	RESISTOR 1K 10% .125W CC TC=-270/+540	01121	BB1021
A3A2R4	0698-5422	9	2	RESISTOR 5.6K 10% .125W CC TC=-350/+857	01121	BB5621
A3A2R5	0698-5422	9		RESISTOR 5.6K 10% .125W CC TC=-350/+857	01121	BB5621
A3A2R6	0698-7926	2	1	RESISTOR 470 10% .125W CC TC=-330/+800	01121	BB4711
A3A2U1	1820-1198	0	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS03N
W1	8120-3724	5	1	USER CABLE 1	28480	8120-3725
W2	8120-3722	3	1	USER CABLE 2	28480	8120-3723

SECTION VII

MANUAL CHANGES

7-1. INTRODUCTION.

7-2. This section contains information required to backdate or update this manual for models with repair numbers prior to those shown on the title page.

7-3. MANUAL CHANGES.

7-4. This manual applies directly to the instrument having the same serial prefix shown on the manual title page. If the serial prefix of the instrument is not the same as the one on the title page, find your serial prefix in the Table 7-1 and make the changes to the manual that are listed for that serial prefix. When making changes listed in Table 7-1, make the change with the highest number first. Example: if backdating changes 1,2, and 3 are required for your serial prefix, do change 3 first, then change 2, and finally change 1.

7-5. If the serial prefix of your instrument is not listed either on the title page or in Table 7-1, refer to an enclosed MANUAL CHANGES sheet for updating information. Also, if a MANUAL CHANGES sheet is supplied, make all indicated ERRATA changes.

Table 7-1. Manual Changes

Serial Prefix	Make Changes
2150	3,2,1
2250	2,1

CHANGE 1

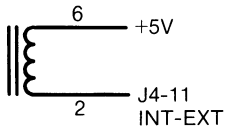
Section VI Replaceable Parts:

A1

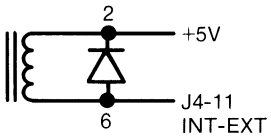
Change	K1	Rly-Reed IC	to	0490-0617
	J5,6	Cbl Asy-Bd Intcn	to	64215-61602

Schematics:

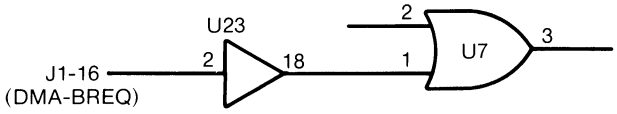
was:



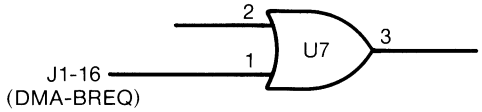
now:



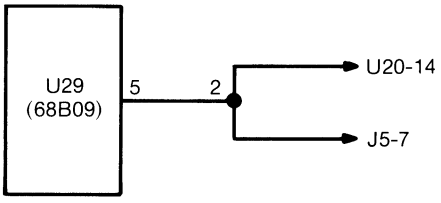
was:



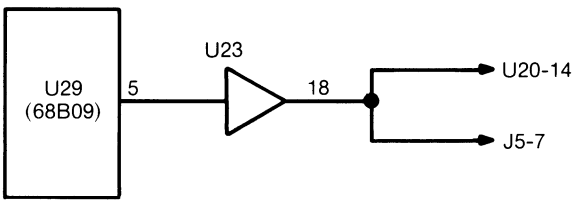
now:



was:



now:



CHANGE 2

Section VI Replaceable Parts:

Change

Board Synchronizer 64215-66506

To

Board Synchronizer 64215-66502

A2U6	Microcode-MSB	to 64215-10001
A2U20	Microcode-Middle	to 64215-10002
A2U31	Microcode-LSB	to 64215-10003

Section VIII Theory and Schematics:

Synchronizer Board, Microsequencer, Service Sheet 1

Parts on this Schematic

U6	64215-10001
U20	64215-10002
U31	64215-10003

CHANGE 3

Section VI Replaceable Parts:

A3*	Bd Asy Active Ckt	64215-62103	to	64215-62102
MP7	Pin Base-Plug	4040-1566	to	64215-44101

*A3--64215-62102 is not serviceable

SECTION VIII

THEORY AND SCHEMATICS

8-1. INTRODUCTION.

8-2. This section provides the Component Locator and Schematic Diagrams used to service the 6809 Emulator Pod. Tables are provided to explain the techniques used in the preparation of the schematics.

8-3. SAFETY.

8-4. Read the safety warnings at the front of this book and at the front of the mainframe service manual and the service overview manual before servicing this emulation pod.

CAUTION

Read the installation instructions given in Section II of this manual before attempting to connect the user plug to the target system. Damage to the emulator may result when the user plug is improperly installed.

8-5. COMPONENT LOCATOR.

8-6. The component locator provides the reference designator and location for each replaceable part contained on the printed circuit assembly. Each component locator is provided as a fold-out drawing preceding the schematic.

8-7. SCHEMATIC DIAGRAMS.

8-8. The schematic diagrams are presented as fold-out sheets at the end of this section. A list of standard reference designators and abbreviations is presented in Section VI of this manual. Table 8-1 describes the techniques used in the development of the logic symbols. Table 8-2 describes the development of the schematic symbols.

8-9. BLOCK THEORY.

8-10. EMULATION SUBSYSTEM. The Model 64215A Emulator Pod is part of a 64000 emulation subsystem used for software development and target system emulation. Figure 8-1 is a block diagram of the Emulation System.

8-11. The target system microprocessor is replaced by an emulation user plug which connects the target system to the emulation pod where the emulation processor is housed.

8-12. The Emulator Pod consists of two boards. A Processor board contains the emulation 6809 processor, buffers, and control circuitry which interface the target system with the emulation system. The second board is a Synchronizer Board which monitors the processor bus and generates status signals which are provided to the emulation control board.

8-13. The emulation control board housed in the mainframe is the primary link between the mainframe BPC and the emulation system. The emulation system can operate by executing user programs loaded in user/emulator memory (fore- ground operation), or it can operate from programs loaded by the mainframe BPC in background memory which is located on the emulator control board (background operation).

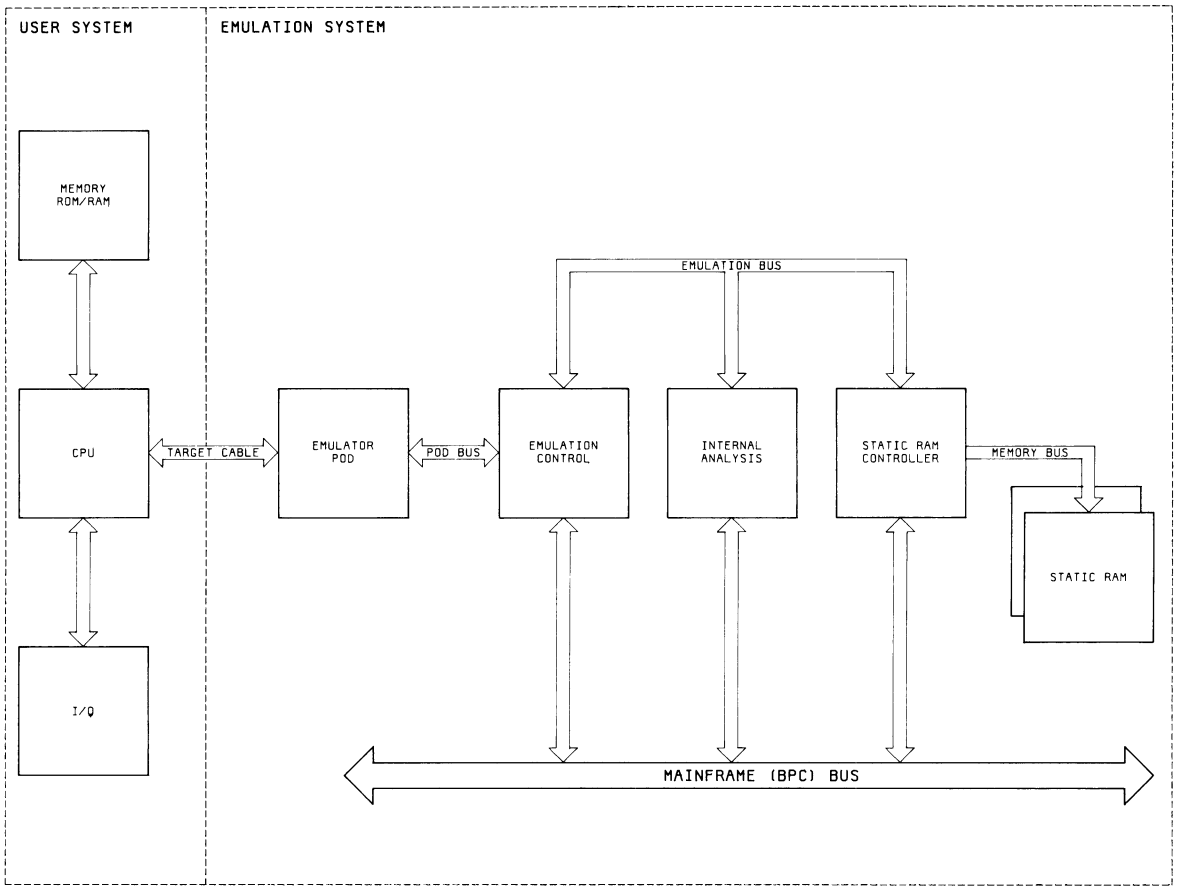


Figure 8-1. Emulation Subsystem Block Diagram

8-14. SYNCHRONIZER BOARD. Figure 8-2 is a block diagram of the 6809 Synchronizer Board. The Synchronizer Board monitors the Processor activity and generates status line signals to indicate the status of each processor cycle. In addition to status generating logic, the Synchronizer Board consists of an instruction decoder, address generator, microinstruction ROMs, an instruction latch, and interrupt service routine counters.

8-15. The current microinstruction is stored in the instruction latches. The decoder uses this microinstruction to generate control signals for the address generator which sends a new microinstruction to the ROMs. The ROMs then send the next microinstruction to the latches.

8-16. The Synchronizer Board generates HISR and SISR to indicate that a hardware or software interrupt service routine has been called. The selected status line remains high until the service routine has been completed. Nested service routines are accounted for by incrementing a counter which holds the appropriate ISR line high until subsequent subroutine returns decrement the counter to its original level.

8-17. PROCESSOR BOARD. The Processor Board consists basically of input and output buffers, a 6809 processor, timing circuitry, and control circuitry. Figure 8-3 is a block diagram of the 6809 processor, timing circuitry, and control circuitry. Figure 8-2 is a block diagram of the 6809 Processor Board.

8-18. Buffers.

8-19. The user address buffers are divided into two groups. U27 and U28 buffer the processor's address lines and drive the user probe during normal operation while U25 and U26 are tri-stated. During DMA activity U27 and U28 buffer the address lines from the target system to the emulator's address bus. U28 and U29 drive the address bus when the emulator is in background operation; at this time U27 and U28 are tristated.

8-20. The user data buffer is U34, a bidirectional buffer/driver.

8-21. The emulation address latches, U39 and U40, buffer the address busessor from the Processor Board to the control board and provide address hold time for analysis and emulation memory.

8-22. The emulation data bus is buffered by U35 and U37 while U36 provides the latching function for the data bus.

8-23. Microprocessor and Timing.

8-24. The microprocessor chip is a 68B09 which runs at a maximum clock speed of 2 MHz. The clock source for the processor comes either from a crystal or a TTL level oscillator in the user's system or an oscillator located on the processor board itself. When executing programs the processor generates the appropriate address, data and status signals to read and write memory. It generates the E and Q clocks that control timing in the rest of the emulator.

8-25. Control Circuitry.

8-23. The control circuitry illustrated in Service Sheet 2 provides directional and timing control for the buffers.

8-27. MNEMONICS.

8-28. Signals in the Model 64216A have been assigned mnemonics which describe the active state and function of the signal line. A prefix letter (H, L, P or N) indicates the active state of the signal and the remaining letters indicate its function. An H prefix indicates that the function is active in the high state; an L prefix indicates that it is active in the low state. For devices that are edge sensitive the prefix "P" indicates that the function is active on the positive going edge; the prefix "N " indicates that the device is active on the negative going edge. These mnemonics are listed in table 8-1.

Table 8-1. Mnemonics

TO/FROM USER SYSTEM

UBA	BUS AVAILABLE. Output signal to the target system, goes high when the user address bus is available to the target system. Normally low indicating the emulation processor is driving the bus.
UBS	BUS STATUS. Output signal to the target system, goes high when user address bus is being used by an interrupt or halt cycle. Normally low indicating that the emulation processor is driving the bus, or that the emulation processor is waiting for external synchronization on an interrupt line.
UD0-7	DATA 0-7. Bidirectional buffered data bus between the emulation processor and the target system.
UFIRQ	FAST INTERRUPT REQUEST. Input from the target system which goes low to request an interrupt of the emulation processor. LFIRQ has priority over LIRG but is honored only if fast mask bit is clear.
UHALT	HALT. Input from target system which goes low to halt all activity in the emulation processor. Held high for normal operation. Also an inter-schematic mnemonic.
UIRQ	INTERRUPT REQUEST. Input from target system which goes low to request an interrupt of the emulation processor. This request is honored only after the current instruction cycle is completed, and only if the interrupt mask bit is cleared. Also an inter-schematic mnemonic.
ULDMA	LOW DIRECT MEMORY ACCESS. This input signal to the emulator indicates that the user system is performing a DMA transfer.

Table 8-1. Mnemonics (Cont'd)

LUSER	LOW FORCE USER. A low signal on either of these input lines to the emulator subsystem will force the emulator to access user memory.
LIV1	LOW INTERRUPT VECTOR. These inputs to the emulator subsystem are only sensed during interrupt vector fetch cycles. If one or both are pulled low during a vector fetch cycle, the vector will be fetched from the vector generation logic in the target system instead of from emulation memory.
BLUSER	LOW USER. This signal is an output to the user system which is generated on the Emulator Control Board. When this signal is low the memory location being addressed has been mapped to user memory.
LWROM	LOW WRITE TO ROM. These are input signals to the emulator subsystem. During a write cycle the emulator will be forced to access user memory when one or both of these lines are brought low.
ULNMI	NON-MASKABLE INTERRUPT. This is an edge sensitive input from the target system which goes low to request an interrupt of the emulation processor. This request will be honored immediately following the current instruction cycle. Also an inter-schematic mnemonic.
UQ/E	Clock inputs required by the 6809E processor. These inputs may be taken from the user system or may be generated on on the 6809E Processor Board.
ULRESET	RESET. A level sensitive, low active input from the the target system used to reset the emulation processor. When the time constraints listed in the 6800 specifications are observed this input can also function as a power up reset. Also an inter-schematic mnemonic.
UR/LW	READ/LOW WRITE. Output to target system which defines the emulation processor operational state. When high the emulation processor is in a read state, when low the emula- tion processor is in a write state.
UA0-15	ADDRESS 0-15. Buffered address bus from the emulation processor to the target system.
VCC/VSS	These inputs from the VCC and VSS pins of the target system microprocessor socket signal the Emulator pod that the user plug is connected to a target system which is operating. This signal is used to enable in-circuit emulation functions.

Table 8-1. Mnemonics (Cont'd)

TO/FROM EMULATION CONTROL BOARD

A0-15	EMULATOR ADDRESS 0-15. Buffered emulation processor address bus.
BLBA	BUS AVAILABLE. Buffered HBA from emulation processor. Goes high to indicate the address bus is available as during a processor halt or a wait state.
D0-7	EMULATION DATA 0-7. Eight bit wide bidirectional emulation data bus from U39 and U41.
FG	FOREGROUND. Goes high whenever a reference is made to memory addresses mapped as foreground memory. Also an inter-schematic mnemonic.
INT/EX	INTERNAL/EXTERNAL CLOCK. Clock select signal sent to the pod from the mainframe processor through the control register to operate U36 and U37. When high the internal oscillator in the pod is enabled, when low the target system clock is used. Also an inter-schematic mnemonic.
LBKG	LOW BACKGROUND. Goes low when the background controller enters the background state.
LREFREQ	LOW REFRESH REQUEST. Not used with current memory and analysis boards. When used, would provide for stopping the emulator processor for an emulation memory refresh cycle. Held high.
LUSER	LOW USER. Buffer control signal to emulator. Goes low when address on emulator address bus is mapped to user memory space.
PFG	EMULATOR PRE-FOREGROUND. Goes high to indicate the background controller is going to change from background to foreground mode.
FORCE-	A signal generated by the Mainframe BPC to force a non-maskable interrupt when the emulator leaves background
FORCE-	Forceuser inhibits HMAV (High Memory Available) which inhibits the emulator Memory and forces user memory access.

Table 8-1. Mnemonics (Cont'd)

LDEFIB	LOW DEFIBRILATION. Goes low when the mainframe processor resets the emulation processor in the pod.
HALT	LOW HALT. A microprocessor pin status register bit from the pod emulator processor HALT pin.
LRESET	LOW RESET. Emulation reset line. Goes low whenever a reset is applied to the emulation processor.
MRDY	MRDY. This is an input to the Pod processor to allow stretching of E and Q to extend data access time.
UR/LW	READ/LOW WRITE. The emulation processor sets this line high for read operations and low for write operations.
VMA	VALID MEMORY ADDRESS. Modified HVMA from the emulator processor. Goes high to indicate a valid memory address is present on the address bus (A0-15).
HISR	These signals are simply bussed across the Processor Board from the Synchronizer Board where they are generated to the control board. Please refer to TO/FROM SYNCHRONIZER BOARD the definitions.

PROCESSOR BOARD INTERNAL MNEMONICS

ADDRESS	This signal generated by multiplexer, U21, turns on the bidirectional address buffers, U27 and U28, and is gated with USER DMA, USER MEM and LICE to turn on U25 and U26 when the emulator is operating in background.
BE	BUFFERED E. This is a timing signal generated by the pod processor which controls timing in the rest of the emulator.
BLR/W	BUFFERED LOW READ/WRITE. This signal is generated by the pod processor, buffered by U9 and inverted by U5 then gated by U12 to generate DATA BUS OUT.
BLRESET	BUFFERED LOW RESET. ULRESET and HBKG are ored to generate this signal which is anded with LDEFIB to generate LRESET.
BR/W	BUFFERED READ/WRITE. This signal is generated by the pod processor then buffered by U9 and gated to produce directional controls and inverted to produce HR/W for the emulator control board.

Table 8-1. Mnemonics (Cont'd)

BQ BUFFERED Q. This is a timing signal generated by the pod processor which controls timing in the rest of the emulator.

DATAIN This signal, generated by U3A, turns on the user data buffer, U34.

DATAOUT This signal, generated by U12, turns on data buffer U35 and U37 to drive data bus to the emulator control board.

H=IN HIGH = IN. This signal, generated by multiplexer U21, enables the data bus from the user system when low, from the pod when high.

HBA HIGH BUS AVAILABLE. This signal, generated by U5, enables the address bus from the user system when low, from the pod when high.

HBKG HIGH BACKGROUND. This signal, generated by U31, is ored with UFIRQ to produce FIRQ; with UNMI to produce LIRQ; with ULRESET to produce BLRESET.

HICE HIGH IN-CIRCUIT EMULATION. This signal goes high when the user plug is installed in the microprocessor socket of the target system and power is present on the Vcc pin of the socket. It signals the pod that in-circuit emulation is now possible.

LDMA/BREQ LOW DIRECT MEMORY ACCESS/BUS REQUEST. This signal generated by U7A is used to turn on the LDMA/LBAE pin (33) on the pod processor.

LHLT LOW HALT. This signal, generated by U3, is used to turn on the LHALT pin (40) on the pod processor.

PA0-15 POD ADDRESS 0-15. This is the pod address bus driven by U28 and U27.

PD0-7 POD DATA 0-7. This is the pod data bus driven by U34.

UMRDY This is an input to the pod processor to allow stretching of E and Q to extend data access time.

TO/FROM SYNCHRONIZER BOARD

A0-2 ADDRESS 0-2. Buffered emulation processor addresses.

ADDR ADDRESS FFF8-FFFF. This address range, detected on the Processor Board, is used by the Synchronizer Board to generate reset and opcode status signals.

Table 8-1. Mnemonics (Cont'd)

CLOCK	A clock signal generated on the Processor Board to clock the TRANSFER, HISR, and SISR logic. It is high when E is high, Q is low and the emulator is in foreground or exiting background operation.
FETCH	FETCH. This status line, generated on the synchronizer board, is high for the first instruction cycle and stays high until the first operand fetch or write cycle.
HFETCH	HIGH FETCH 1. This status signal, generated on the Synchronizer Board, is high only during the first instruction cycle.
HISR	HARDWARE INTERRUPT SERVICE ROUTINE. This signal, generated on the Synchronizer Board, signals the analyzer that a hardware interrupt has occurred and also signals the end of the subroutine.
PD0-7	POD DATA 0-7. Buffered emulation processor data bus.
Q	Q and E are the two clock lines required by the 6809E processor, are buffered on the Synchronizer Board before being used. Q is the master clock for the synchronizer board although under microcode control the E clock may be exclusive or'd with the Q to clock the Synchronizer Board on the falling edge of Q.
INTRV	INTERRUPT VECTOR. This signal, generated on the synchronizer board, gates BS and BA to generate INTRV which is high when an interrupt vector fetch is occurring.
SISR	SOFTWARE INTERRUPT SERVICE ROUTINE. This status line is generated on the Synchronizer Board to signal the analyzer that a software interrupt routine has been called, or completed.
VMA	VALID MEMORY ADDRESS. This signal, generated on the Synchronizer Board, identifies most non-valid instruction cycles.
XFER	TRANSFER. This status signal generated on the synchronizer board signals a transfer of control from the emulator to the target system.

Table 8-1. Mnemonics (Cont'd)

SYNCHRONIZER BOARD INTERNAL MNEMONICS

AD0-11 ADDRESS DATA 0-11. This is the address bus for the micro-instruction store located in the PROMS U20, 31 and 6.

DMAVMA DIRECT MEMORY ACCESS/VALID MEMORY ADDRESS. This signal is high when the processor is releasing or regaining control of the busses for DMA activity.

EXTREG EXTERNAL REGISTER CLOCK. This signal is used to clock the external data register U21 and U7.

HFFFF HIGH FFFF. This is a signal used by the instruction decoder and the VMA circuitry to determine the next address output from the decoder and the bus status for the VMA circuitry.

HRESET HIGH RESET DETECT. Synchronizer board inputs A0-2 and FFFX are monitored to produce this signal. When it goes high it resets the control circuitry which generates the status signals which are output from the synchronizer board.

INA INCREMENT ADDRESS. If an interrupt has occurred a low signal on this line forces the next sequential address stored in the address generator to be held over unmodified to the next clock cycle.

JUMP0 JUMP 0. When this signal is 0 the normally selected address source is used. When it is a 1 a fetch is forced from location 0000H for the next microinstruction.

PD0-7 PROCESSOR DATA 0-7. This is a data bus from the processor board to the Synchronizer Board.

RE REGISTER ENABLE. A 0 on this signal enables the internal register to the Address Generator which will save the external data bus contents on the next synchronizer clock.

SBA SYNCHRONIZER BUS AVAILABLE / SYNCHRONIZER BUS STATUS. Bus available and bus status signals from the processor latched and used to generate synchronizer status outputs.

SBE STATUS BUS ENABLE. This signal is used to enable U46. If this signal is 0 the outputs will follow the D inputs. If this signal is 1 the inputs will be latched.

Table 8-1. Mnemonics (Cont'd)

SCALL	SUBROUTINE CALL. This signal goes high when a subroutine call is detected, enabling the hardware or software subroutine counters.
SD0-7	STATUS DATA 0-7. This is the data bus for the micro-instruction store located in the PROMS U20, 31 and 6.
SEL0-3	SELECT 0-3. These outputs from the instruction decoder are buffered by U18 and used as the direct inputs to the address generators.
SELOREN	SELECT OVERRIDE ENABLE. When this signal is 0, S0 and S1 are passed unchanged to the address generator. When Seloren is 1, S0 and S1 are forced to 0.
S0-3	STATUS 0-3. These signals are microinstructions from a microinstruction store ROM U21 to latch U14.
SRET	SUBROUTINE RETURN. This signal goes low when a subroutine return is detected causing either the hardware or software counter to begin decrementing. SS SYNCHRONIZER STATUS. This signal combines the Q and E inputs to clock U14. If the outputs are enabled a high SS signal will allow the Q outputs to follow the D inputs.
SS0	SYNCHRONIZER STATUS 0,1. SS0 and SS1 are used to determine the next microprogram address.
SYNCCLK	SYNCHRONIZER CLOCK. The E and Q clocks are exclusive- or'd by U11A to produce this signal which clocks the syn- chronizer board on the falling dege of Q.

Table 8-2. Logic Symbols

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term.)

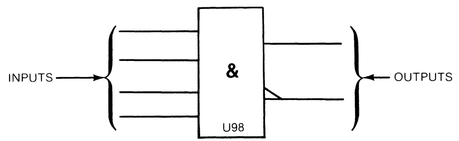
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

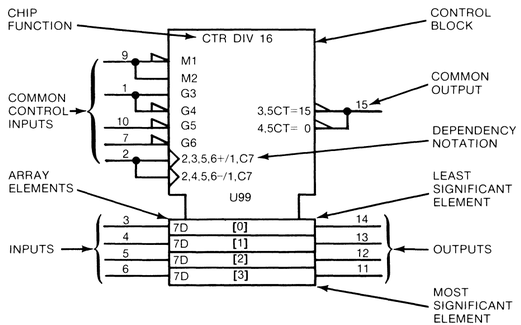
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. Unless indicated, the least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in **[ ]**).

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INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.

b. Interconnection (Z) indicates connections inside the symbol.

c. Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.

d. Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.

e. Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).

f. Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.

g. Address (A) identifies the address inputs.

h. Transmission (X) identifies bi-directional inputs and outputs that are connected together when the transmission input is true.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (compliments state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection
		X	Transmission

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OTHER SYMBOLS

Analog Signal	Inversion	Shift Right (or down)
& AND	O Negation	Solidus (allows an input or output to have more than one function)
Bit Grouping	Nonlogic Input/Output	Tri-State
Buffer	Open Circuit (external resistor)	, Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.
! Compare	Open Circuit (external resistor)	( ) Used for factoring terms using algebraic techniques.
Dynamic	≥1 OR	[ ] Information not defined.
=1 Exclusive OR	Passive Pull Down (internal resistor)	Φ Logic symbol not defined due to complexity.
Hysteresis	Passive Pull Up (internal resistor)	
? Interrogation	Postponed	
Internal Connection	← Shift Left (or up)	

LABELS

BG	Borrow Generate	CO	Carry Output	J	J Input
BI	Borrow Input	CP	Carry Propagate	K	K Input
BO	Borrow Output	CT	Content	P	Operand
BP	Borrow Propagate	D	Data Input	T	Transition
CG	Carry Generate	E	Extension (input or output)	+	Count Up
CI	Carry Input	F	Function	-	Count Down

MATH FUNCTIONS

Σ	Adder	>	Greater Than
ALU	Arithmetic Logic Unit	<	Less Than
COMP	Comparator	CPG	Look Ahead Carry Generator
DIV	Divide By	π	Multiplier
=	Equal To	P-Q	Subtractor

CHIP FUNCTIONS

BCD	Binary Coded Decimal	DIR	Directional	RAM	Random Access Memory
BIN	Binary	DMUX	Demultiplexer	RCVR	Line Receiver
BUF	Buffer	FF	Flip-Flop	ROM	Read Only Memory
CTR	Counter	MUX	Multiplexer	SEG	Segment
DEC	Decimal	OCT	Octal	SRG	Shift Register

DELAY and MULTIVIBRATORS

Astable

100 ns Delay

Nonretriggerable Monostable

NV Nonvolatile

Retriggerable Monostable

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Table 8-3. Schematic Diagram Notes

ETCHED CIRCUIT BOARD

FRONT PANEL MARKING

REAR-PANEL MARKING

MANUAL CONTROL

SCREWDRIVER ADJUSTMENT

TP1 ELECTRICAL TEST POINT TP (WITH NUMBER)

NUMBERED WAVEFORM NUMBER CORRESPONDS TO ELECTRICAL TEST POINT NO.

LETTERED TEST POINT NO MEASUREMENT AID PROVIDED

COMMON CONNECTIONS. ALL LIKE-DESIGNATED POINTS ARE CONNECTED.

1 3 NUMBER ON WHITE BACKGROUND = OFF-PAGE CONNECTION. LARGE NUMBER ADJACENT = SERVICE SHEET NUMBER FOR OFF-PAGE CONNECTION.

A CIRCLED LETTER = OFF-PAGE CONNECTION BETWEEN PAGES OF SAME SERVICE SHEET.

INDICATES SINGLE SIGNAL LINE

NUMBER OF LINES ON A BUS

4

(925) WIRE COLORS ARE GIVEN BY NUMBERS IN PARENTHESES USING THE RESISTOR COLOR CODE

[(925) IS WHT-RED-GRN]
0 - BLACK 5 - GREEN
1 - BROWN 6 - BLUE
2 - RED 7 - VIOLET
3 - ORANGE 8 - GRAY
4 - YELLOW 9 - WHITE

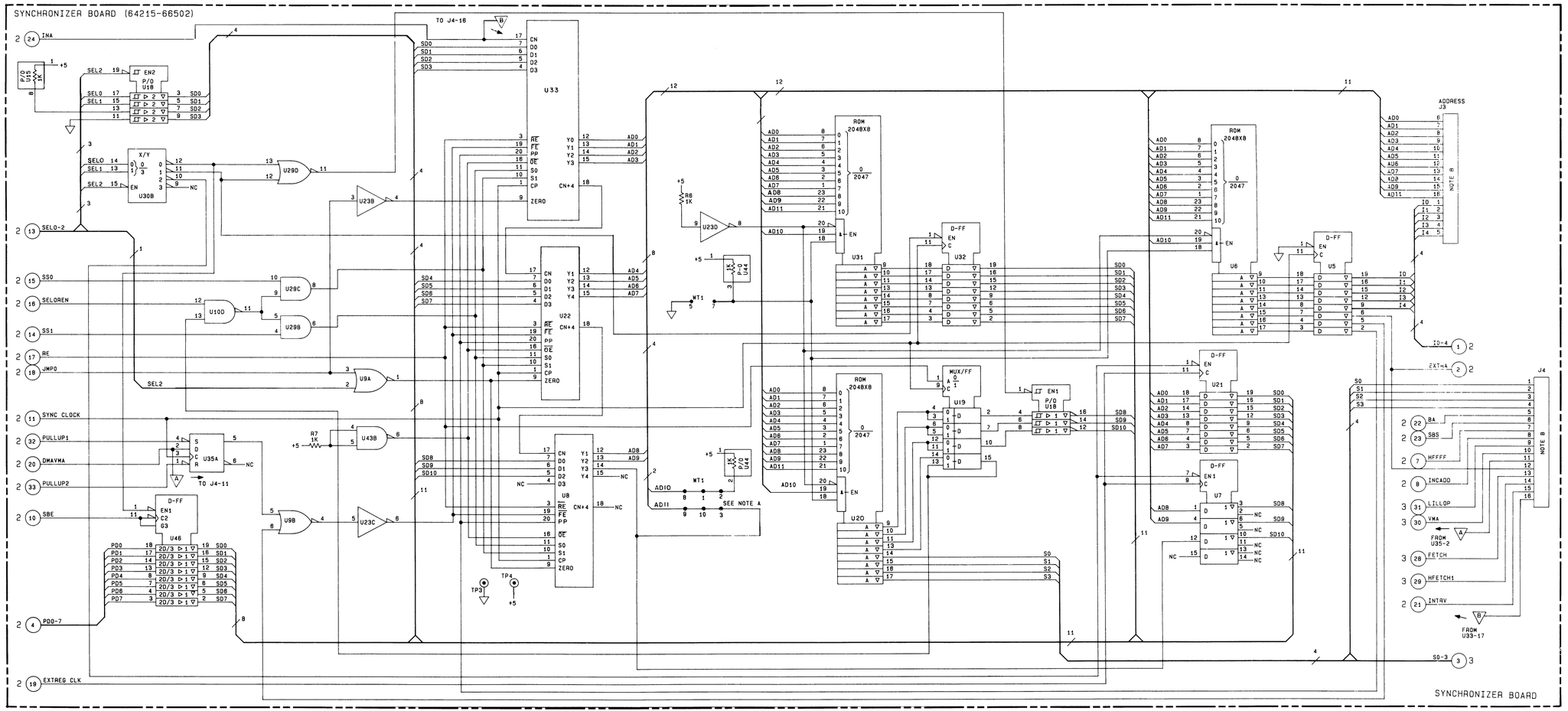
* OPTIMUM VALUE SELECTED AT FACTORY, TYPICAL VALUE SHOWN; PART MAY HAVE BEEN OMITTED.

UNLESS OTHERWISE INDICATED:
RESISTANCE IN OHMS
CAPACITANCE IN PICOFARADS
INDUCTANCE IN MICROHENRIES

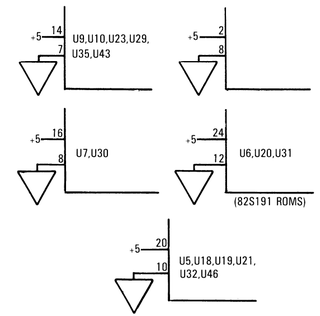
μP = MICROPROCESSOR
P/O = PART OF
NC = NO CONNECTION
CW = CLOCKWISE END OF VARIABLE RESISTOR

STD-20-09-81

Figure 8-2. Synchronizer Board, Component Locator



IC POWER SUPPLY PIN CONFIGURATION



NOTE A:
WT1 IS PROVIDED FOR FUTURE APPLICATIONS ONLY. NO FIELD MODIFICATION SHOULD BE PERFORMED.

NOTE B:
16 PIN IC SOCKET PROVIDED FOR TEST PURPOSES.

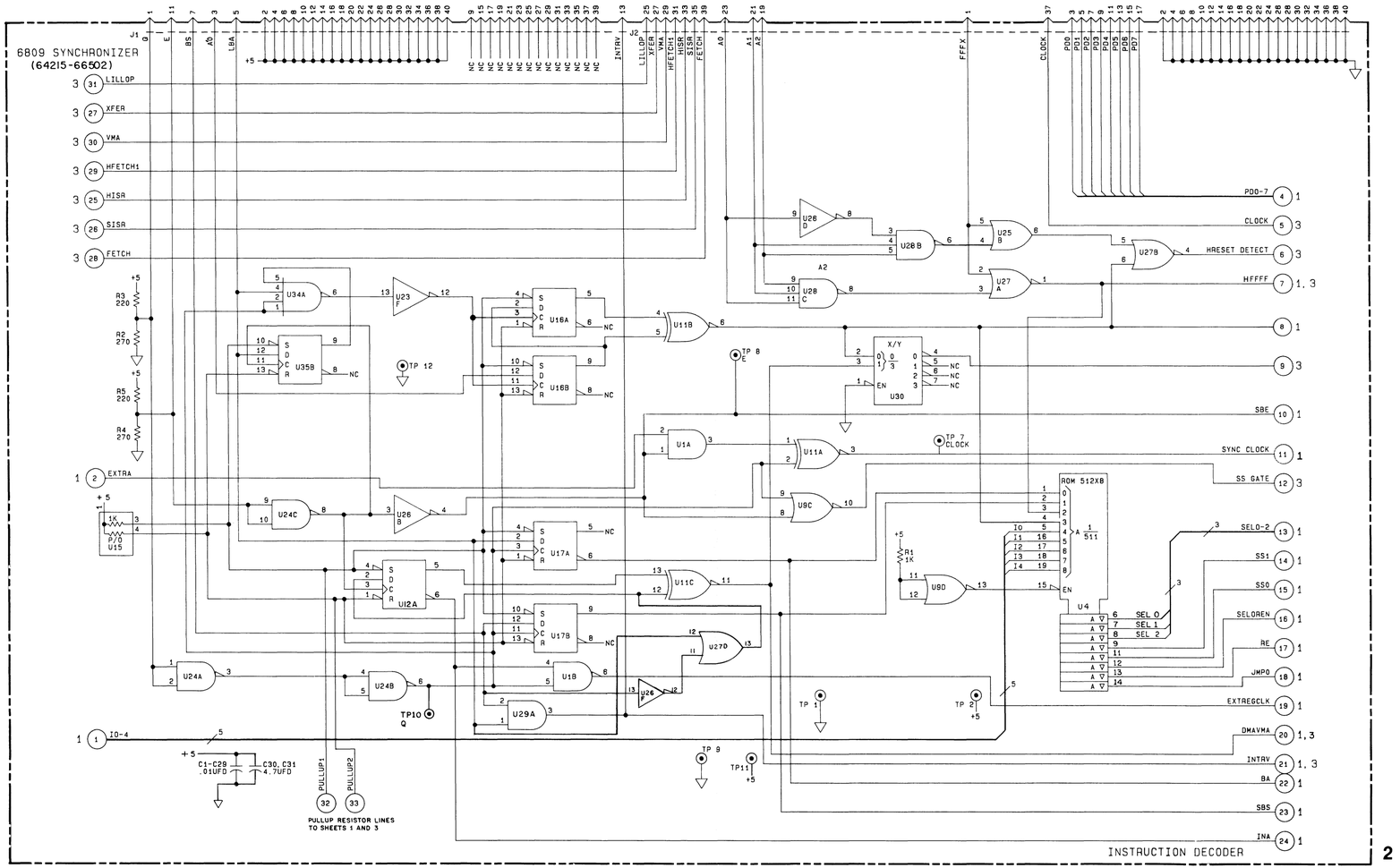
ICS ON THIS SCHEMATIC

Ref Des	HP Part No	Mfr Part No
U5,U21,U32	1820-1677	74S374
U6	64215-10001	64215-10001
U7	1820-2415	AM2918
U8,U22,U33	1820-2260	AM2911
U9	1820-1144	74LS02
U10	1820-0681	74S00
U18	1820-1624	74S241
U19	1820-2384	74LS399
U20	64215-10002	64215-10002
U23	1820-0683	74S04
U29	1820-1367	74S08
U30	1820-1072	74S139
U31	64215-10003	64215-10003
U35	1820-0693	74S74
U43	1820-1197	74LS00
U46	1820-1676	74S373

PARTS ON THIS SCHEMATIC

J3,J4
R6,R7
TP3,TP4
U5-U10,U15,U18-U23,U29,U30-U33,U35,U43,U44,U46
WT1

Figure 8-3.
Synchronizer Board, Microsequencer, Service Sheet 1
8-15/(8-16 blank)



ICS ON THIS SCHEMATIC

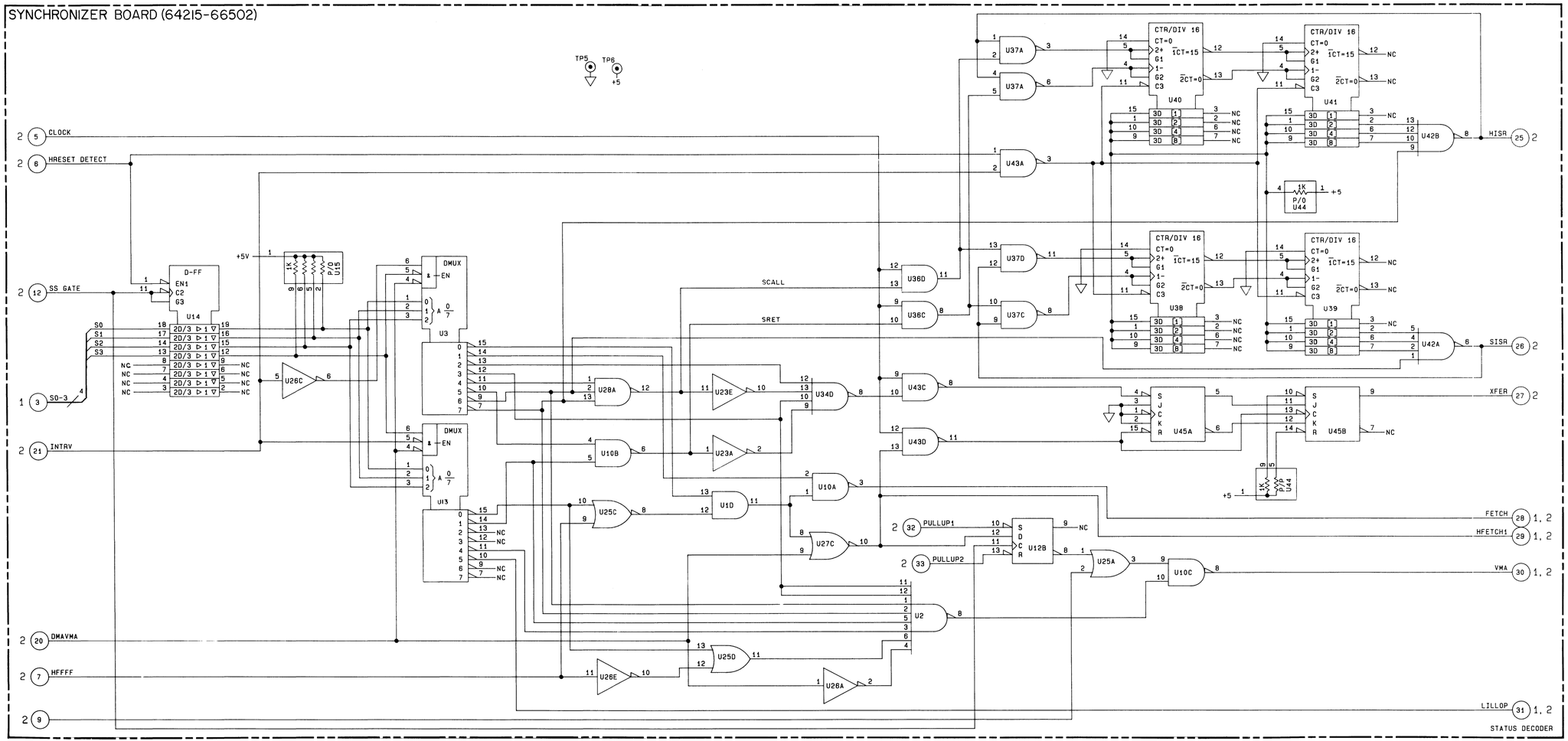
Ref Des	HP Part No	Mfr Part No
U1,U29	1820-1367	74S08
U4	64215-10000	64215-10000
U9	1820-1144	74LS02
U11	1820-0694	74S86
U12	1820-2488	74ALS74
U16,U17,U35	1820-0693	74S74
U24	1820-1307	74S132
U25	1820-1449	74S32
U23,U26	1820-0683	74S04
U27	1820-1322	74S02
U28	1820-0685	74S10
U30	1820-1072	74S139
U34	1820-0688	74S20

PARTS ON THIS SCHEMATIC

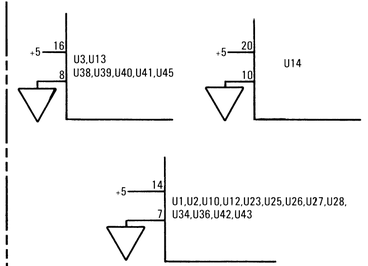
C1-C31
R1-R5
TP1,TP2,TP7-TP12
U1,U4,U9,U11,U12,U15-U17,U23-U30,U34,U35

IC POWER SUPPLY PIN CONFIGURATION

Figure 8-4.
Synchronizer Board, Instruction Decoder, Service Sheet 2
8-17/(8-18 blank)



IC POWER SUPPLY PIN CONFIGURATION



ICS ON THIS SCHEMATIC

Ref Des	HP Part No	Mfr Part No
U1	1820-1367	74S08
U2	1820-1207	74LS30
U3,U13	1820-1240	74LS138
U10	1820-0681	74S00
U12	1820-2488	74ALS74
U14	1820-2102	74LS373
U23,U26	1820-0683	74S04
U25	1820-1449	74S32
U27	1820-1322	74S02
U28	1820-0685	74S10
U34	1820-0688	74S20
U36	1820-1201	74LS08
U37,U43	1820-1197	74LS00
U38,U39,U40,U41	1820-1194	74LS193
U42	1820-1204	74LS20
U45	1820-1212	74LS112

PARTS ON THIS SCHEMATIC

U1-U3,U10,U12-U15,U23,U25-U28,U34,U37-U45

Figure 8-5.
Synchronizer Board, Status Decoder, Service Sheet 3
8-19

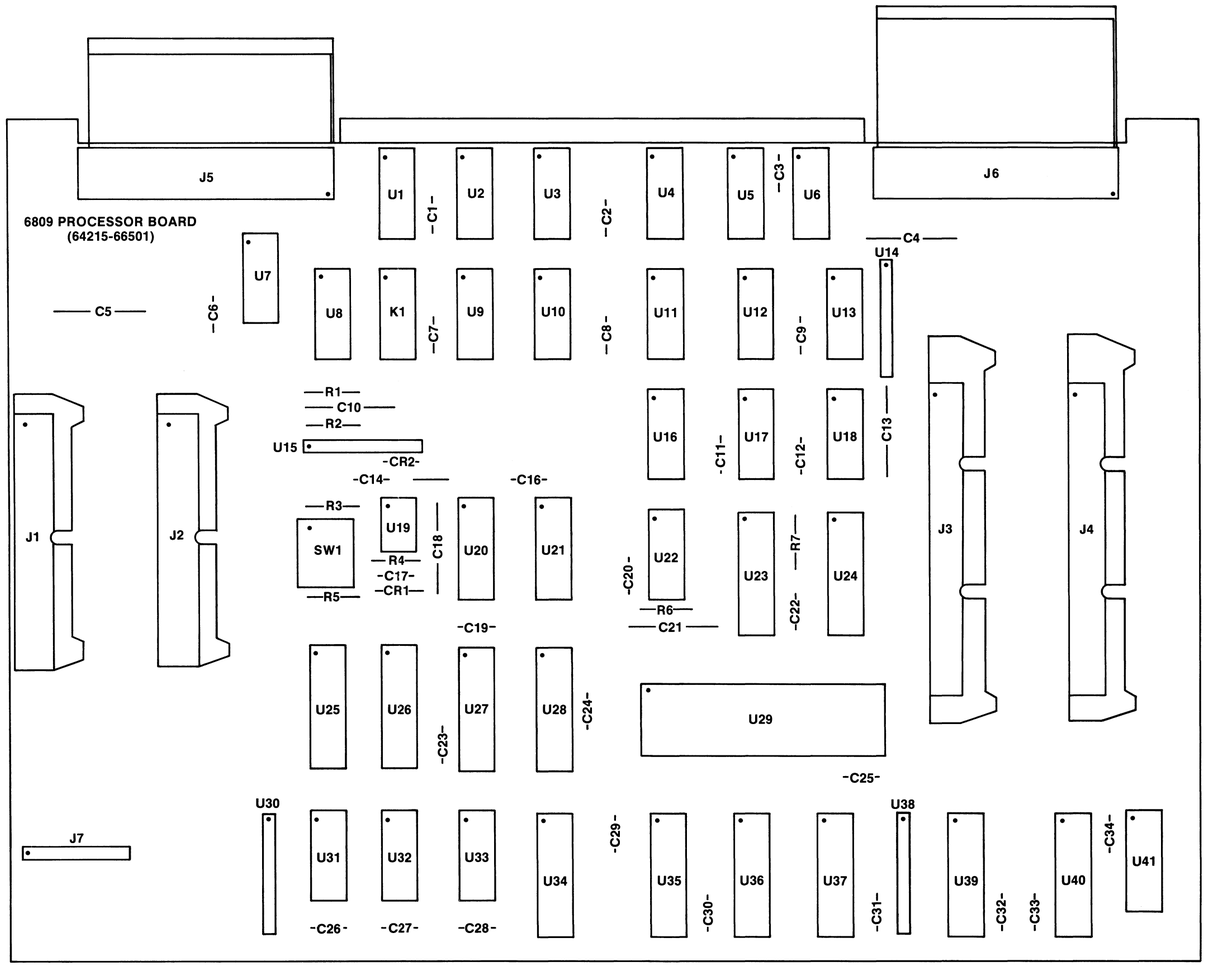
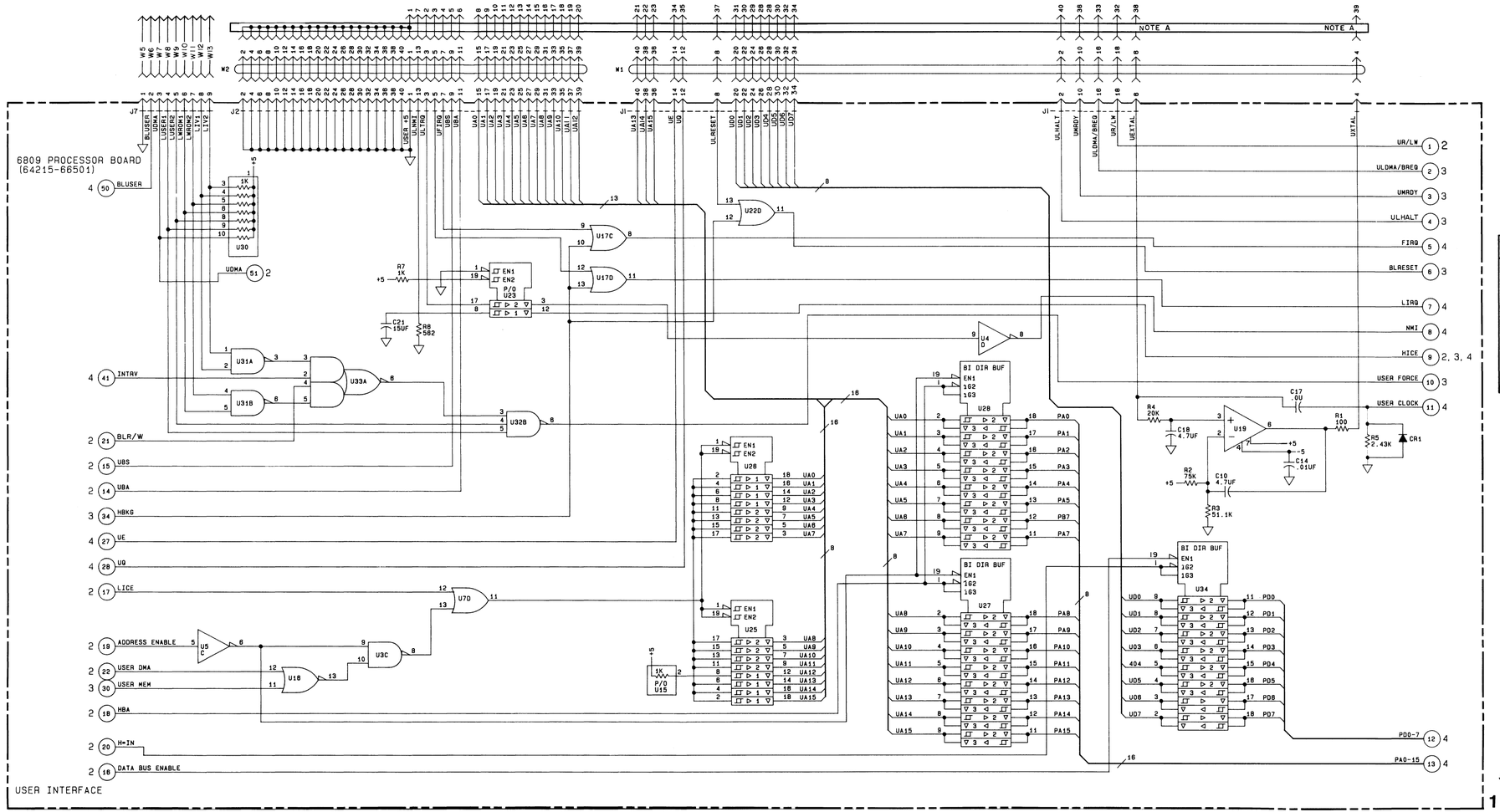


Figure 8-6. Processor Board, Component Locator



IC POWER SUPPLY PIN CONFIGURATION

ICS ON THIS SCHEMATIC

Ref Des	HP Part No	Mfr Part No
U3	1820-1197	74LS00
U4	1820-1199	74LS04
U5	1820-0683	74S04
U7,U17,U22	1820-1449	74S32
U16	1820-1322	74S02
U19	1820-0217	741
U23	1820-1624	74S241
U25,U26	1820-2024	74S244
U27,U28,U34	1820-2075	74LS245
U31	1820-0681	74S00
U32	1820-0685	74S10
U33	1820-1158	74S51

PARTS ON THIS SCHEMATIC

C10,C14,C17,C18,C21
CR1
J1,J2
K1
R1-R7
U3-U5,U7,U15-U17,U19,U22,U23,U25-U28,U30-U34
W1,W2

NOTE A:

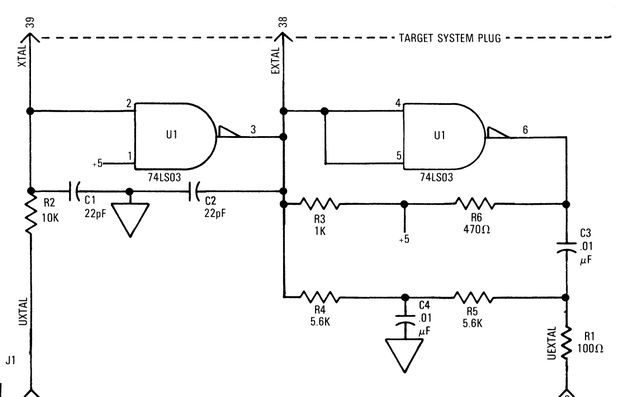
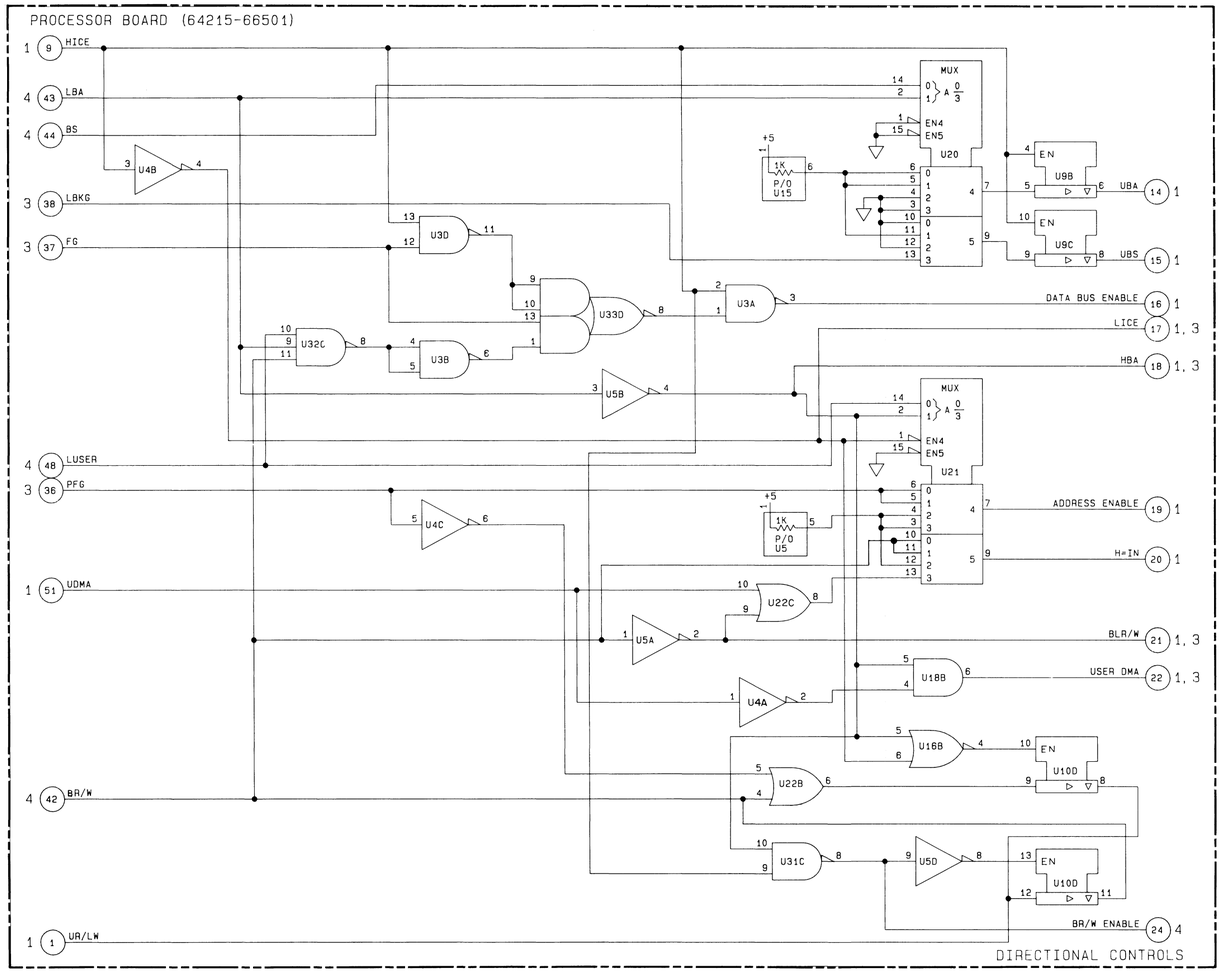
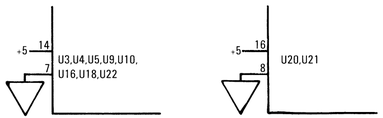


Figure 8-7.
Processor Board, User Interface, Service Sheet 1
8-21/(8-22 blank)



IC POWER SUPPLY PIN CONFIGURATION



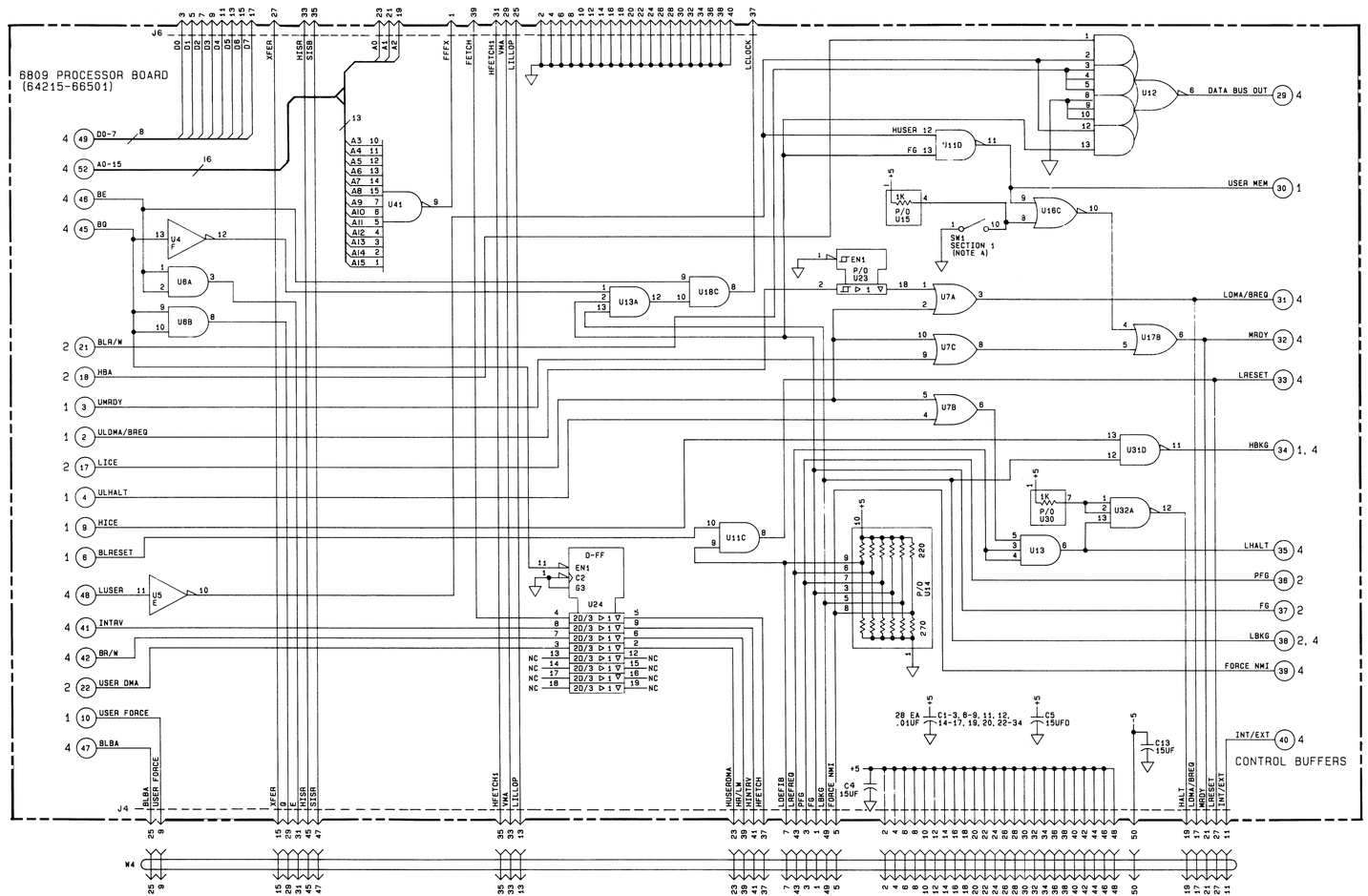
ICS ON THIS SCHEMATIC

Ref Des	HP Part No	Mfr Part No
U3	1820-1197	74LS00
U4	1820-1199	74LS04
U5	1820-0683	74S04
U9,U10	1820-1645	74LS126
U16	1820-1322	74S02
U18	1820-1201	74LS08
U20,U21	1820-1244	74LS153
U22	1820-1449	74S32

PARTS ON THIS SCHEMATIC

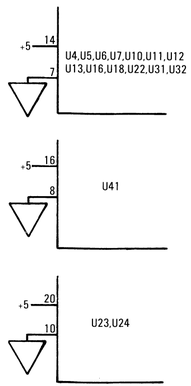
U3-U5,U9,U10,U15,U16,U18,U20-U22

Figure 8-8.
Processor Board, Directional Controls, Service Sheet 2
8-23/(8-24 blank)



3

IC POWER SUPPLY PIN CONFIGURATION



ICS ON THIS SCHEMATIC

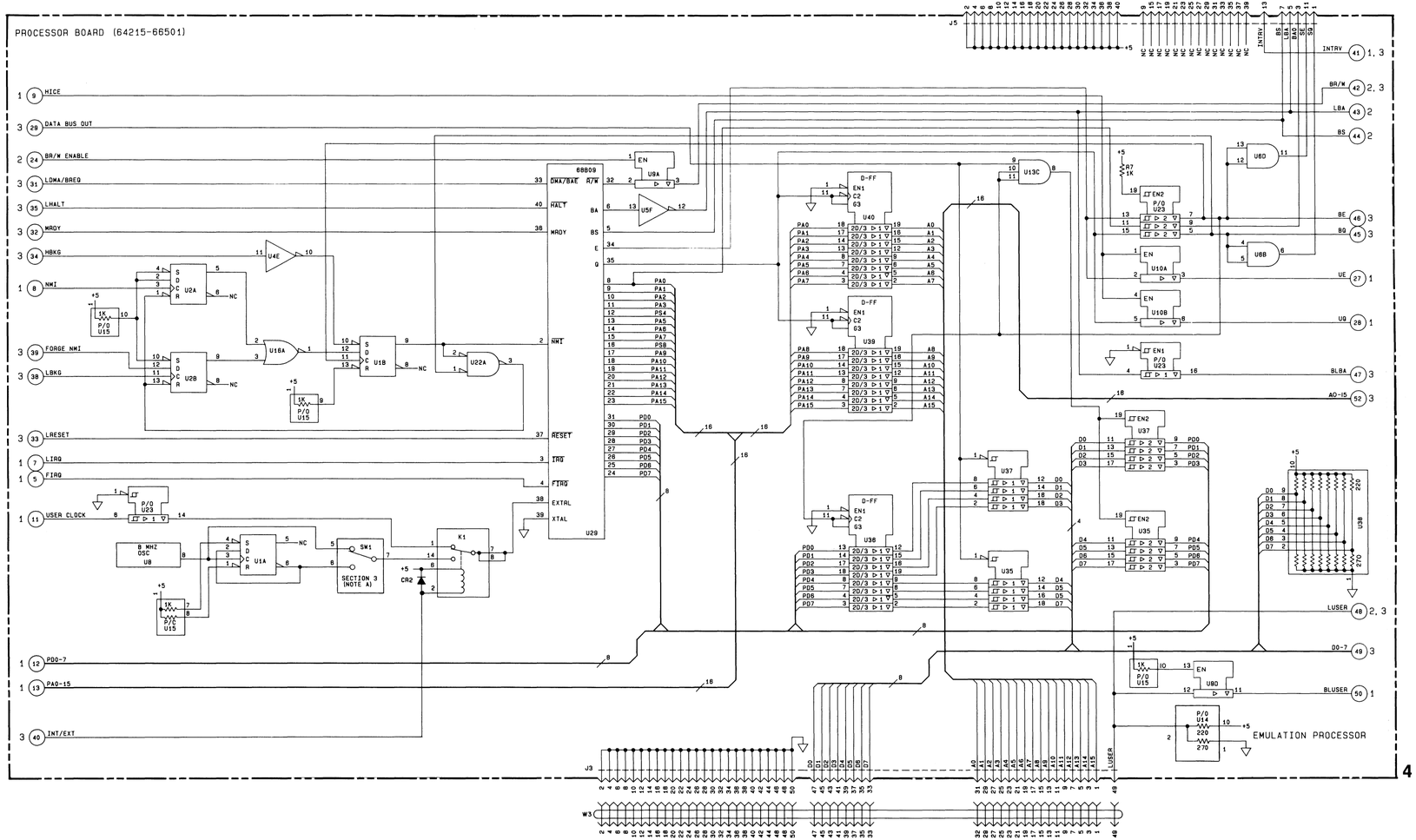
Ref Des	HP Part No	Mfr Part No
U4	1820-1199	74LS04
U5	1820-0683	74S04
U6,U11	1820-1367	74S08
U7,U22	1820-1449	74S32
U10	1820-1645	74LS126
U12	1820-1285	74LS54
U13	1820-1203	74LS11
U16	1820-1322	74S02
U18	1820-1201	74LS08
U23	1820-1624	74S241
U24	1820-2102	74LS373
U31	1820-0681	74S00
U32	1820-0685	74S10
U41	1820-1130	74S133

PARTS ON THIS SCHEMATIC

C1-C9,C11-C17,C19,C20,C22-C34
J4,J6
U4-U7,U10-U16,U18,U22-U24,U30-U32,U41
W4

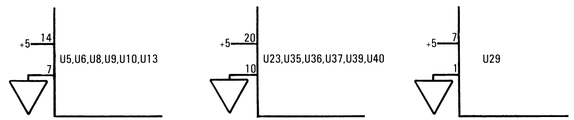
NOTE A:
FOR SW1
SECTION 1 OPEN = MRDY ENABLED ALWAYS
SECTION 1 CLOSED = MRDY ENABLED ONLY IN FOREGROUND

Figure 8-9.
Processor Board, Control Buffers, Service Sheet 3
8-25/(8-26 blank)



4

IC POWER SUPPLY PIN CONFIGURATION



ICS ON THIS SCHEMATIC

Ref Des	HP Part No	Mfr Part No
U5	1820-0683	74S04
U6	1820-1367	74S08
U8	1813-0188	8 MHz OSC
U9,U10	1820-1645	74LS126
U13	1820-1203	74LS11
U23,U35,U37	1820-1624	74S241
U29	1820-2770	68B09
U36	1820-2102	74LS373
U39,U40	1820-1676	74S373

PARTS ON THIS SCHEMATIC

CR2
J3,J5
R7
U1,U2
U4-U6,U8-U10,U13-U15,U22,U23,U29,U35-U40
SW1
W3

NOTE A:
SECTION 3 SELECTS CLOCK RATE.
4X 1 MHz AS SHOWN.
4X 2 MHz IN OPPOSITE POSITION.

Figure 8-10.
Processor Board, Emulation Processor, Service Sheet 4

SALES & SUPPORT OFFICES

Arranged Alphabetically by Country

Product Line Sales/Support Key

Key	Product Line
A	Analytical
CM	Components
C	Computer Systems Sales only
CH	Computer Systems Hardware Sales and Services
CS	Computer Systems Software Sales and Services
E	Electronic Instruments & Measurement Systems
M	Medical Products
MP	Medical Products Primary SRO
MS	Medical Products Secondary SRO
P	Personal Computation Products
*	Sales only for specific product line
**	Support only for specific product line

IMPORTANT: These symbols designate general product line capability. They do not insure sales or support availability for all products within a line, at all locations. Contact your local sales office for information regarding locations where HP support is available for specific products.

HP distributors are printed in italics.

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E,M,P

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Hewlett-Packard Argentina S.A.
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Martinez 1640 **BUENOS AIRES**
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Telex: 17595 BIONAR
Cable: HEWPACKARG
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Telex: 17595 BIONAR
M

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THE GAP, Queensland 4061
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Telex: 42133

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***SANTIAGO** 21*
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Telex: 340-892 OLYMP CK
Cable: Olympiachile Santiagochile
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A,CM,E,P

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M

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Kasr-el-Aini
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Informatic For Systems
22 Talaat Harb Street
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P

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Hewlett-Packard France
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F-25000 **BESANCON**
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F-38320 **EYBENS**
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CH

Hewlett-Packard France
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A

Blue Star Ltd.
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***SECUNDERABAD** 500 003*
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Telex: 0155-459
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Blue Star Ltd.
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Hewlett-Packard Italiana S.p.A.
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Hewlett-Packard Italiana S.p.A.
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Hewlett-Packard Italiana S.p.A.
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000 **ATSUGI**, Kanagawa, 243
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Yokogawa-Hewlett-Packard Ltd.
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Telex: NZ 3380
A,M

NORTHERN IRELAND

See United Kingdom

NORWAY

Hewlett-Packard Norge A/S
Folke Bernadottes vei 50
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N-5033 **FYLLINGSDALEN** (Bergen)
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Telex: 16621 hpnas n
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N-1345 **ÖSTERÅS**
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OMAN

Khimjil Ramdas
P.O. Box 19
MUSCAT
Tel: 722225, 745601
Telex: 3289 BROKER MB MUSCAT
P

Suhail & Saud Bahwan
P.O.Box 169
MUSCAT
Tel: 734 201-3
Telex: 3274 BAHWAN MB

PAKISTAN

Mushko & Company Ltd.
1-B, Street 43
Sector F-8/1
ISLAMABAD
Tel: 26875
Cable: FEMUS Rawalpindi
A,E,M

Mushko & Company Ltd.
Oosman Chambers
Abdullah Haroon Road
***KARACHI** 0302*
Tel: 524131, 524132
Telex: 2894 MUSKO PK
Cable: COOPERATOR Karachi
*A,E,M,P**

PANAMA

Electrónico Balboa, S.A.
Calle Samuel Lewis, Ed. Alfa
Apartado 4929
PANAMA 5
Tel: 64-2700
Telex: 3483 ELECTRON PG
A,CM,E,M,P

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Arranged alphabetically by country

PERU
Cía Electro Médica S.A.
Los Flamencos 145, San Isidro
Casilla 1030
***LIMA** 1*
Tel: 41-4325, 41-3703
Telex: Pub. Booth 25306
CM,E,M,P

PHILIPPINES
The Online Advanced Systems Corporation
Rico House, Amorsolo Cor. Herrera Street
Legaspi Village, Makati
P.O. Box 1510
*Metro **MANILA***
Tel: 85-35-81, 85-34-91, 85-32-21
Telex: 3274 ONLINE
A,CH,CS,E,M

Electronic Specialists and Proponents Inc.
690-B Epifanio de los Santos Avenue
*Cubao, **QUEZON CITY***
P.O. Box 2649 Manila
Tel: 98-96-81, 98-96-82, 98-96-83
Telex: 40018, 42000 ITT GLOBE MACKAY BOOTH
P

PORTUGAL
Mundinter
Intercambio Mundial de Comércio S.A.R.L.
P.O. Box 2761
Avenida Antonio Augusto de Aguiar 138
P-LISBON
Tel: (19) 53-21-31, 53-21-37
Telex: 16691 munter p
M

Soquimica
Av. da Liberdade, 220-2
*1298 **LISBOA** Codex*
Tel: 56 21 81/2/3
Telex: 13316 SABASA
P

Telectra-Empresa Técnica de Equipmentos Eléctricos S.A.R.L.
Rua Rodrigo da Fonseca 103
P.O. Box 2531
***P-LISBON** 1*
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CH,CS,E,P

PUERTO RICO
Hewlett-Packard Puerto Rico
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CAROLINA, Puerto Rico 00628
Calle 272 Edificio 203
Urb. Country Club
RIO PIEDRAS, Puerto Rico
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A,CH,CS

QATAR
Computearbia
P.O. Box 2750
DOHA
Tel: 883555
Telex: 4806 CHPARB
P

Eastern Technical Services
P.O.Box 4747
DOHA
Tel: 329 993
Telex: 4156 EASTEC DH

Nasser Trading & Contracting
P.O.Box 1563
DOHA
Tel: 22170, 23539
Telex: 4439 NASSER DH
M

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Modern Electronic Establishment
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CH,CS,E,M,P

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CM

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CH,CS,M

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A,CS,MS,P

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Hewlett-Packard Sverige AB
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CH-8967 **WIDEN**
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E

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M,P

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A

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Unimesa
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P

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CM,E,M,P

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Tunisie Electronique
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E,P

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M

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Teknim Company Ltd.
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E

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M

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C*,E*,MS**

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MS

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3
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