64000

HP64000 Logic Development System

Model 64214A 6809 Emulator Control Board

HEWLETT PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard system product is warranted against defects in materials and workmanship for a period of 90 days from date of installation. During the warranty period, HP will, at its options, either repair or replace products which prove to be defective.

Warranty service of this product will be performed at Buyer's facility at no charge within HP service travel areas. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses. In all other cases, products must be returned to a service facility designated by HP.

For products returned to HP for warranty service. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

CW&A 2/81

MODEL 64214A

6809 EMULATOR CONTROL BOARD

REPAIR NUMBERS

This manual applies directly to Emulator Control Boards with repair numbers prefixed 2250A. For additional information about repair numbers see Section I, paragraph 1-3.

Manual Part No. 64214-90901
Microfiche Part No. 64214-90801

PRINTED: MARCH 1983

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

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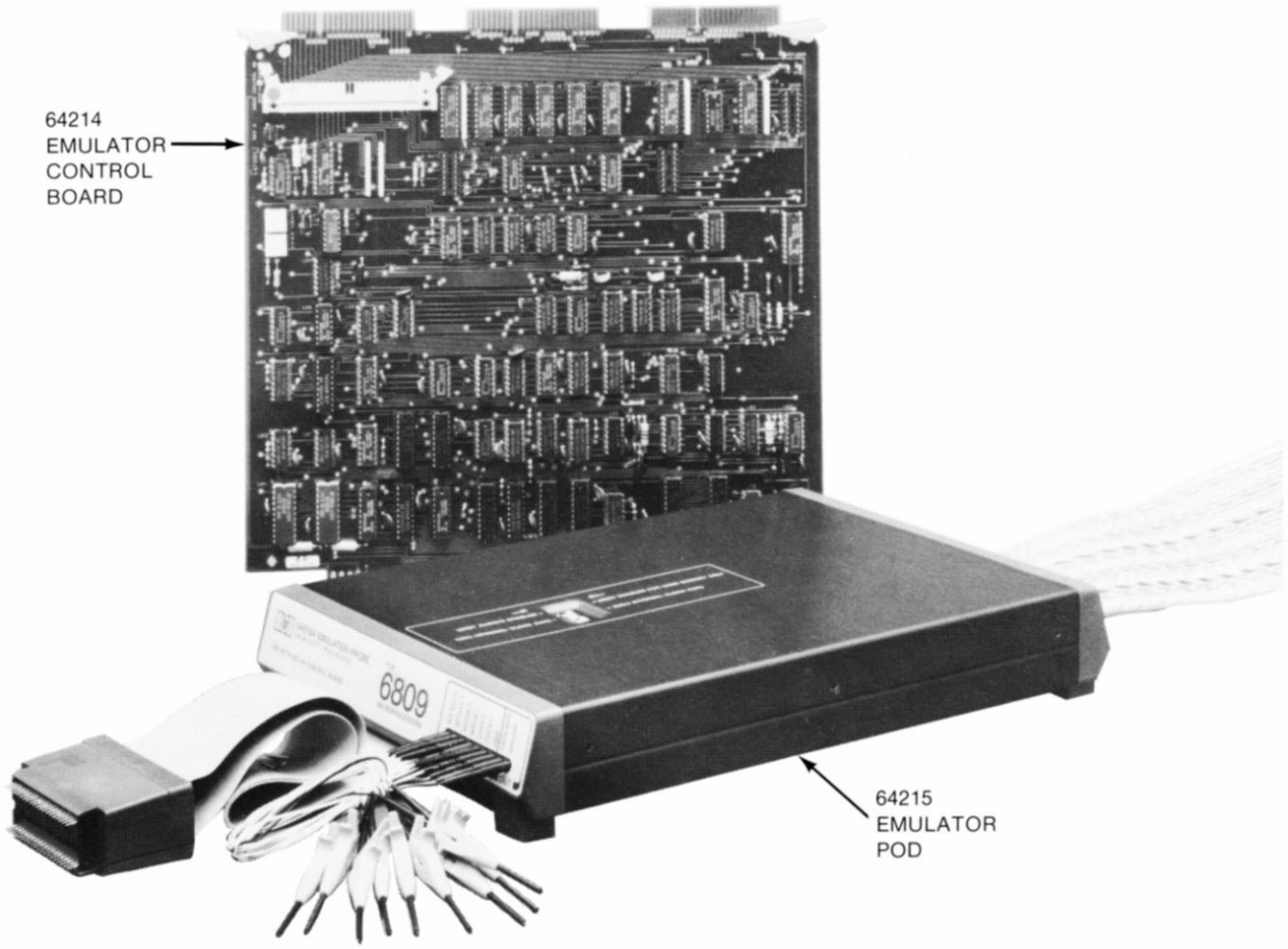


Figure 1-1. 6809 Emulation Subsystem

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This Service Manual contains information required to install, test and service the Model 64214A 6809 Emulator Control Board.

1-3. This manual is organized with eight sections: Section I provides a brief physical and functional description. Section II outlines installation and removal. Section III, Operation, refers to another manual which contains operations information. Section IV, Performance Verification, discusses the Performance Verification tests. Section V describes Adjustments. Section VI lists replaceable parts. Section VII explains backdating needed to make this manual applicable to older units. Section VIII contains the component locator, and the schematic diagrams.

1-4. INSTRUMENTS COVERED BY THIS MANUAL.

1-5. Printed on each 64214A 6809 Emulator Control Board is the repair number. The repair number is in two parts, in the form 0000A00000. The first four digits and the letter are the repair prefix and the last five are the suffix. The prefix is the same for all identical boards. The suffix is assigned sequentially and is different for each board. The contents of this manual apply to boards with the repair number prefixes listed under REPAIR NUMBERS on the title page.

1-6. Any board manufactured after the printing of this manual may have a repair prefix that is not listed on the title page. This unlisted repair number prefix indicates that the board may be different from those described in this manual. Updating the manual for this newer board is accomplished by a manual changes supplement. The supplement contains "change information" that explains how to adapt this manual for the newer board.

1-7. In addition to change information, the supplement contains information for correcting errors in this manual. To keep this manual as current as possible, Hewlett-Packard recommends that you periodically request the latest manual changes supplement. The supplement for this manual is identified with the manual print date and the part number, which both appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-8. For information concerning a repair number prefix that is not listed on the title page or in the manual changes supplement, contact your nearest Hewlett-Packard Sales/Service Office.

1-9. DESCRIPTION.

1-10. The Model 64214A 6809 Emulator Control Board is a single printed circuit board which installs in the 64000 mainframe. This board provides emulation control for the 6809 Emulator Subsystem. The 6809 Emulator Card requires a 6809 Emulator Pod, Model 64215A, to perform software development and in-circuit emulation.

1-11. ACCESSORIES SUPPLIED.

1-12. Supplied with the Emulator Control Board are two 8120-3351 bus cables which are required to connect the board to the Model 64151A Emulation Memory Controller option. The installation of these cables is discussed in Section II.

1-13. ADDITIONAL EQUIPMENT REQUIRED.

1-14. The Model 64214A must be plugged into the 64000 mainframe and connected to an emulation pod to have a minimum emulation subsystem.

1-15. POWER SUPPLY LOADING.

1-16. The power requirements of the Emulator Control Board when configured with the emulator pod are listed in Table 1-1.

Table 1-1. Power Supply Requirements

	64214A	64215A	TOTAL
+5 V	1.5 A	3.4 A	4.9 A
-5 V		Approx. 2ma	

No other voltages are required.

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information required to install the Model 64214A in the Model 64000 mainframe. Also included are the initial inspection procedures, damage claim information, and the operating, storage, and shipment environmental considerations.

2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until contents of the shipment have been checked mechanically and electrically. Procedures for checking performance are provided in Section IV of this manual. If the contents are not complete, if there is mechanical damage or defect, or if the board does not pass the performance tests, notify the carrier as well as Hewlett-Packard Sales/Service office. Keep the shipping materials for carriers inspection. The Hewlett-Packard Sales/Service office will arrange for repair or replacement at HP option without waiting for claim settlement.

2-5. INSTALLATION AND REMOVAL.

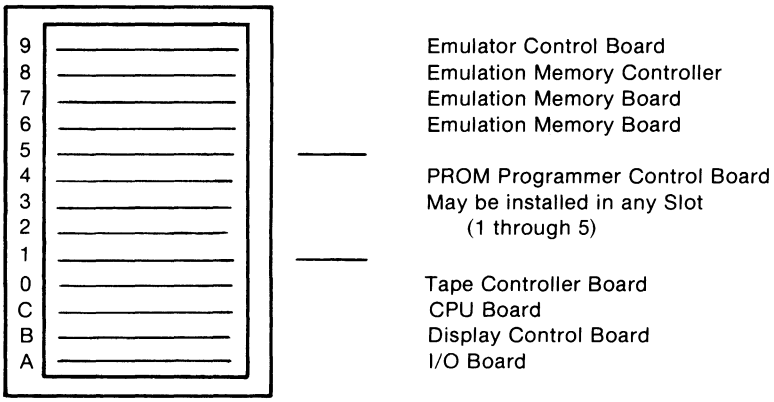
2-6. Figure 2-1 shows a top view of the 64100A mainframe card cage and the recommended position for the Emulator Control Board and for the Static RAM Controller Board, Static RAM Boards, and the Internal Analysis Boards which are optional. The recommended slot for the 64214A is the rearmost position. This maximizes the free cable length to the emulator pod.

WARNING

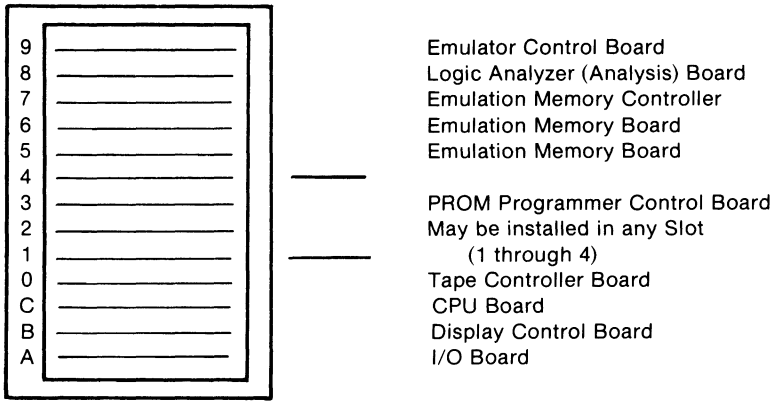
To prevent personal injury, refer to the safety requirements listed in the mainframe manual before installing this option.

CAUTION

The 64214A Emulator Control Board must be installed and removed with the 64000 power turned off. Damage to the unit may otherwise result.



A. EMULATION AND MEMORY



B. EMULATION/ANALYSIS AND MEMORY

Figure 2-1. Recommended Card Cage Configuration

2-6. To install the 64214A, proceed as follows:

a. Turn 64100A power OFF.

b. Loosen the two hold down screws and remove the card cage access cover.

c. Connect the selected emulator pod to the Emulator Control Board prior to the installation of the board in the card cage. This is done to simplify the connection of the the multi-conductor pod bus cables to the board. Two multi-colored ribbon cables are used to connect the pod to the Emulator Control Board. One cable terminates in a female card-edge connector, the other terminates in a female socket-type connector. Pin 1 is indicated by a triangle molded into the body of each connector. The mating connectors for the cable connectors are located at the top left corner of the board as viewed from the component side. Pin 1 of the card-edge connector (J1) is indicated by a "1" etched into the board. Pin 1 of the connector block located directly below J1 (J4) is indicated by a triangle molded into the connector block. The connector block and the mating female connector on the cable have matching colored dots on their surfaces. The connector block is a latching type connector. Before installing the cable connector into the connector block insure that the latching tips are open (spread toward the outside edges of the board). Connect the card-edge connectors first, then connect the socket-type connector to the connector block. Push the socket-type connector into the connector block until the latching tips snap over the top of the connector.

d. Grasp the board by the extractor levers located at the top of the board. Be very careful not to dislodge the cables. Hold the board with the component side toward the front of the development station and the card-edge connector labeled P1 toward the bottom of the card cage. Insert the board into the selected card slot guide rails, make sure P1 and the motherboard connector are aligned, and push the board down until seated firmly in the connector.

e. The bus cables supplied with the Emulator Control Board are used to connect to the optional Emulation Memory Controller. The bus cables are keyed so that they will seat on the edge connector in only one position.

f. Stack the emulator pod cables flat across one of the cable rests at the back of the development station.

g. Reinstall the card cage access cover and tighten the two screws.

2-7. To remove the 64214A, reverse the installation procedure.

2-8. If the optional Emulation Memory Controller is installed, connect the emulation bus cables as follows. Align pin one of each ribbon cable connector, indicated by the dark stripe on the side of the cable and by a colored dot on the connector, with pin one on the card edge connectors J2 and J3 of each board, also indicated by a colored dot. Press the connector on until it seats firmly on the edge connector.

2-9. OPERATING ENVIRONMENT.

2-10. The 64214A may be operated in environments within the following limits:

Temperature	0° to +40° C
Humidity	5% to 80% relative humidity
Altitude	4 600 m (15 000 ft)

It should be protected from temperature extremes which cause condensation within the unit.

2-11. STORAGE AND SHIPMENT ENVIRONMENT.

2-12. The 64214A may be stored or shipped within the following limits:

Temperature	-40° C to +75° C
Humidity	5% to 80% relative humidity
Altitude	15 300 m (50 000 ft)

2-13. PACKAGING.

2-14. ORIGINAL PACKAGING. Containers identical to those used in factory packaging are available through Hewlett-Packard offices.

2-15. OTHER PACKAGING. The following general instructions should be used for repacking with commercially available materials:

a. Wrap the Emulator Control Board in heavy paper or plastic.

b. Use a strong shipping container. A double-wall shipping container of 350 pound test material is adequate.

c. Use a layer of shock absorbing material 70- to 100 mm (3- to 4 inch) thick around all sides of the board to provide firm cushioning and to prevent movement inside the container.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to the board by model number and full repair number.

SECTION III

OPERATION

Operation of the 6809 Emulation Subsystem is beyond the scope of this manual, please refer to the 6809 Operation Manuals for operating instructions.

SECTION IV

PERFORMANCE VERIFICATION

4-1. INTRODUCTION.

4-2. This section describes the Performance Verification for the 6809 Emulation Control Card. The scope of the Performance Verification is to detect problems at the board level only. Board level troubleshooting is in support of the Blue Stripe Program.

4-3. For convenience, the figures for the Performance Verification are grouped together at the end of this section.

4-4. RUNNING 64214A EMULATION PERFORMANCE VERIFICATION.

4-5. The Performance Verification (P.V.) for the 64214A 6809 Control Board is a subsection of the Option Test P.V. The Option Test P.V. tests all possible option modules that can be configured within the expansion slots of the Mainframe.

The option_test P.V. can either be run with a 64000 development station configured in a network arrangement (hard disk based); or it may be run from a 64000 station in a stand-alone configuration (mini disk based). When running the option_test performance verification on a Model 64214A Control Board from a stand-alone 64000 configuration, the following modules must be present on the current local disk system:

FLOPPY_OP_SYS OPTION_TEST PV_EMUL_6809

4-6. To test the 64214A, proceed as follows.

a. With the operating system initialized and awaiting a command, press the softkey option_test followed by a return.

option_test RETURN

b. The CRT will now display a directory of the installed option boards and their slot numbers. (Figure 4-2). Locate the 6809 Controller and enter the card slot number. For example, in Figure 4-2 the 64214A is in slot 9. Therefore, enter:

9 RETURN

At this point you may receive a prompt to select a slot number for one of the other option boards loaded in the mainframe. This prompt will be displayed when more than one board is loaded which performs the same function. For example, if two analysis boards are loaded in the mainframe the display will prompt:

Select analysis board for test:9

c. A menu will now appear which lists the tests available to exercise the emulator (figure 4-3). This is the Emulator PV Menu (refer to Figure 4-3). The following softkeys will appear at the bottom of the display.

<end>	Returns the user to the option test card slot listing
<disp_test>	Advances the user to the detailed view of the mapper control test; that is, the test execution display.
<print>	Copies the display to the system line printer (if one is attached)

d. Press the <disp_test> softkey. This will advance the P.V. to the Control Board test execution display (refer to Figure 4-4). The following softkeys are listed at the bottom of the display:

<start>	Begins execution of the tests listed.
<exit_test>	Returns the user to the Mapper Control Test overview display described previously.
<print>	Copies the display to the system line printer (if one is attached).

e. To initiate testing of the 6809 Control Card, press the <start> softkey. The key will be highlighted in inverse video on the display and test execution will proceed. The <cycle> softkey is used to cycle through the tests executing each test once per pass. When the <cycle> key is used, the display maintains a count of the number of times each test is executed (#Test) and the number of failures detected (#Fail). If all tests pass, testing can be terminated as described in the next paragraph. However, if any failures occur, refer to the description of the Control Board Test in the following sections.

f. You can end testing of the 64214A in one of two ways:

1. The <start> softkey may be pressed. The test will terminate at the end of the current test cycle and the start softkey on the display will return to normal video. To completely exit the performance verification from this point, press the <exit_test> softkey. This returns you to the Performance Verification Menu display. Press the <end> softkey while in this display. This returns you to the option_test card slot listing, at which point the <end> softkey can be pressed to exit the performance verification software.

2. The <exit_test> softkey may be pressed. The test will terminate at the end of the current test cycle and the display will be returned to the Performance Verification Menu display. At this point, you may press the <end> softkey, returning the display to the option_test card slot listing level. When the <end> softkey is pressed at this point, the option_test performance verification is completely exited and the display is returned to the "Awaiting command" status.

4-7. PERFORMANCE TESTS.

4-8. Five groups of tests are included in the 6809 PV: the Processor Control Tests, Parts 1 and 2, the Emulation Bus Tests, the Foreground Tests, and the Analysis Stimulus Tests. Each segment of a test excercises a selected function of the emulator. The tests should be run in the sequence they are given to ensure that the results are valid. The following paragraphs provide a brief description of each test.

4-9. TEST ERROR COUNTS. The performance test summary displays include two columns labeled # Fail and # Test. The # Fail column increments for each pass of a test in which an error is detected. The # Test column increments for each pass of a test which is executed.

4-10. STATUS DISPLAY. The Processor Control Tests and the Foreground Tests use a status display to report the results of certain tests. This display reports the results of comparisons of the expected test results with the actual test results. It is not a display of the current status of these bits. These bits are numbered to correspond to the numbered bits of the Emulator Status register 5100.

	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	
Status=	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
																	Status Error Indicated
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	RESET
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	BA
	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	-	XFER
	-	-	-	-	-	-	-	-	-	-	-	-	1	-	-	-	MRDY
	-	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	HALT
	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	-	BREQ
	-	-	-	-	-	-	-	-	-	1	-	-	-	-	-	-	SISR
	-	-	-	-	-	-	-	-	1	-	-	-	-	-	-	-	HISR
	-	-	-	-	-	-	-	1	-	-	-	-	-	-	-	-	BKG INT
	-	-	-	-	-	-	1	-	-	-	-	-	-	-	-	-	MEM BRK
	-	-	-	-	-	1	-	-	-	-	-	-	-	-	-	-	ILLOP
	-	-	-	-	1	-	-	-	-	-	-	-	-	-	-	-	BKG
	-	-	-	1	-	-	-	-	-	-	-	-	-	-	-	-	CLOCK
	1	1	1	-	-	-	-	-	-	-	-	-	-	-	-	-	JAM INTERRUPT VECTOR (A3,A2,A1)

4-11. PROCESSOR CONTROL TEST-PART 1.

4-12. The Processor Control Tests-Part 1 check the ability of the mainframe processor in the development station to control the emulator. Each of the major control functions is tested and the background memory is checked. Tests included in the Processor Control-Part 1 tests are; the Reset Test, the Background Test, the Release Test, and the Run Test. A failure detected by any of these tests indicates a problem in the emulator control board or the pod Processor board except for failures in HISR or SISR status. HISR and SISR status errors indicate the pod Synchronizer Board may have failed.

4-13. RESET TEST. The Reset Test performs a preliminary check of the status reporting capabiltity of the emulator. The mainframe processor resets the emulator and then reads the status reported back. The test results are then compared to the expected results.

4-14. BACKGROUND TEST. This test checks the background memory. In the Reset Test segment, the mainframe processor writes a data pattern to the background memory, while the emulation processor is held reset. The data is then read back and compared to the expected results. In the Not Reset Test the identical memory test is performed again while the emulation processor is executing a short program. The test results are displayed as the address and the data received as a result of the memory test.

NOTE

When the Background Test fails, the results of the following tests may not be valid.

4-15. RELEASE TEST. The release test verifies that the emulator can be released to run programs in the background memory. A short program which modifies the contents of a memory location in the background memory is loaded into the background memory. The emulator is released to run the program and then the location is checked to verify that the memory contents of that location were changed. The error indication from this test is a status word equal to the data read from the memory location.

4-16. RUN TEST. A short program is loaded into the background memory and executed. The program is then modified causing a branch to a memory test. Failures occur when the background program is not successfully modified during the program run. The test returns the address error from the memory test. The status display contains the address which failed in the memory test.

4-17. PROCESSOR CONTROL TEST-PART 2.

The Processor Control Test-Part 2 tests check other emulator functions. These tests include the Background Interrupt, the Illegal Opcode Test, the Slow Clock Test, and the Emulation Memory Test. The emulation memory test is unavailable if optional emulation memory is not installed.

4-18. BACKGROUND INTERRUPT TEST. The background interrupt test attempts to execute a single step command. If a background interrupt does not occur a failure is reported. A failure of this test indicates a problem in the control board.

4-19. ILLEGAL OPCODE TEST. An illegal opcode is loaded into the background memory and an attempt is made to execute the illegal instruction code with the illegal opcode detector enabled and disabled. The status display shown below is returned when a failure is detected.

```
Status = 1 1 1

         1 - -  Illegal Opcode Masking Failure.
                Emulator Control Board problem indicated.
         - 1 -  Illegal Opcode Detector failure.
                Pod Synchronizer or Control Board problem
                indicated.
         - - 1  Illegal Opcode Detector did not clear.
                Emulator Control Board problem indicated.
```

4-20. SLOW CLOCK TEST. A CWAIT instruction is executed from the background memory. In approximately one-half second the SLOW CLOCK status bit should set. Failures are reported as shown below.

```
Status = 1 1
         1 -   Slow Clock Detector Failure
         - 1   Clear Failed
```

Failures indicate a problem on the pod Synchronizer board or the Emulator Control Board.

4-21. EMULATION MEMORY TEST. The Emulation Memory Test checks the emulation RAM and the associated control, address and data lines. Two test segments are used: a Data Test and an Address Test. To begin the test the emulator is reset by the mainframe processor. The mainframe processor then writes data to the memory and reads it back. The test is then repeated with a short program executing in background. Failures detected during the Reset Test indicate a problem on the Emulation Memory Controller Board. Failures detected during the Not Reset Test indicate a problem on the Emulator Control Board or the Emulation Memory Controller Board.

4-22. EMULATION BUS TEST.

4-23. The Emulation Bus Test verifies the operation of the emulation bus address and data lines. The emulation bus is used to connect the Emulator Control Board to the optional Memory Control and Logic Analyzer Boards. This test requires the successful completion of the Processor Control Tests for both the Emulator Control Board and the Static Memory Control Board PV. The Emulation Bus Test consists of two subtests: the Data Test, and the Address Test.

4-24. DATA TEST. The mainframe processor tests two blocks of emulation memory for this test. In the first part of the test the memory is loaded through the memory control board and read through the emulator control board. In the second part of the test the inverse pattern is written to memory through the emulation control board and read back through the memory control board. A failure indicates a problem in the emulator control or memory control boards, or in the the memory bus cables.

4-25. ADDRESS TEST. The Address Test operates similarly to the data test except a pattern of addresses is used and the data lines are assumed to be good. Any failure detected is reported as an address error and indicates the same sources for errors.

4-26. FOREGROUND TEST.

4-27. The Foreground Test checks the ability to emulate in foreground memory. The Foreground Test consists of seven subtests: the Release Test, the Run Test, the Processor Break Test, the Illegal Memory Reference Test, the Last Opcode Address Test, the Last Memory Address Test, and the SISR, XFER Test. A description of each tests is provided below.

4-28. RELEASE TEST. The Release Test loads a program into emulation memory and releases the emulation processor to execute the program. The program is designed to modify a specific memory location. The host processor waits a suitable amount of time and then checks to see that the memory location has been modified. A failure detected by this test indicates a problem on the pod Processor Board, the Emulator Control Board or the pod Synchronizer Board. The error indication from this test is a status word equal to the data read from the memory location.

4-29. RUN TEST. For the Run Test, a program is loaded into emulation memory and the emulation processor is released to execute the program. The host processor monitors the emulator status during the program run. Status errors detected by the host processor indicate a problem on the pod Processor Board, Emulator Control Board or the pod Synchronizer Board.

4-30. PROCESSOR BREAK TEST. For the Processor Break Test a program is loaded into emulation memory and the emulation processor is released to execute the program. The host processor then tries to break the program run. The contents of the PC register and the status of the NMI occurrence bit are checked. An error indicates a problem in the pod Processor Board, Emulator Control Board or the pod Synchronizer Board.

4-31. ILLEGAL MEMORY REFERENCE TEST. In the Illegal Memory Reference Test, the mainframe maps blocks of the available memory into RAM, ROM and Illegal Memory space. The emulation processor then executes programs which attempt to reference these areas of memory. The host processor monitors the operation and checks that the proper break and illegal reference status bits are reported. Failures detected by this test indicate a problem in the Memory Control Board or the Emulation Control Board.

4-32. LAST OPCODE ADDRESS. For the Last Opcode Address test the emulation processor executes programs which cause bit patterns to be stored in the last opcode register on the Emulator Control board. The host processor checks the address stored against the expected results. Errors indicate a problem on the Control Board or the pod Processor Board.

4-33. LAST MEMORY ADDRESS. This test is identical to the Last Opcode Address test except that the patterns are stored in the last memory address register.

4-34. SISR, XFER. The SISR, XFER test checks the operation of the pod Synchronizer Board. The host monitors the operation of the SISR and XFER control lines while the emulation processor is running a test program. Any error detected indicates a problem on the pod Synchronizer Board or the Emulator Control Board.

4-35. ANALYSIS STIMULUS.

4-36. If an internal analysis board is connected to the emulation bus, it will monitor data operations on the emulation bus. The analyzer may be used to collect or store data. There may be more than one internal analyzer connected to the emulation bus and will be indicated, to the user, by the option_test card cage menu. The Analysis Stimulus test checks to make sure that the analyzer is monitoring data operations correctly. If no analyzer board is present in the mainframe, the performance verification screen will tell the user that the analysis tests cannot be performed. For failures that occur during the analysis tests, refer to the appropriate analyzer manual for test details.

4-38. MEMORY AND ANALYSIS BOARD PV.

4-39. The Emulation Bus and Foreground Tests of the memory controller board PV, and the Emulation Stimulus Test of the analysis board PV, cannot be used with the 6809 Emulation Subsytem. Figure 4-9 contains the PV Selection Menu Displays for the PV of both boards. The message "Select Slot #9 for Emulation Bus and Foreground Tests" appears in the memory board PV. The message "Select Slot #9 for Emulation Stimulus Tests" appears in the analysis board PV display.

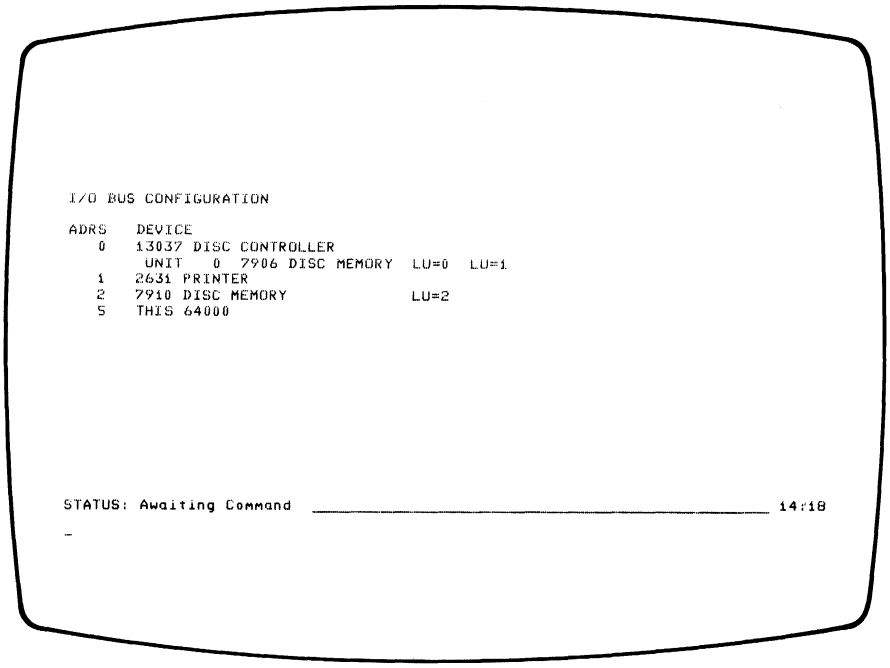


Figure 4-1. Awaiting Command Display

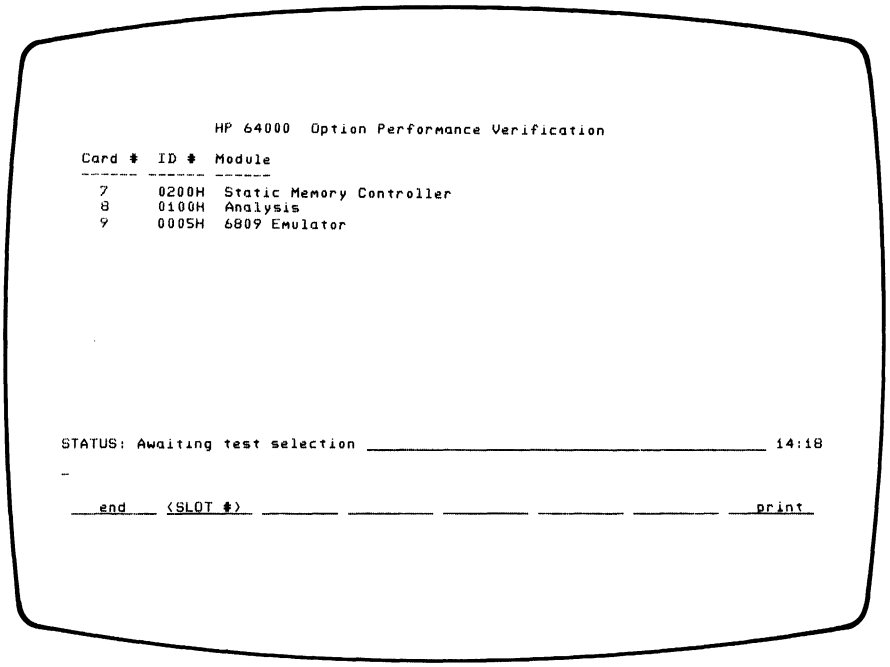


Figure 4-2. Option Map

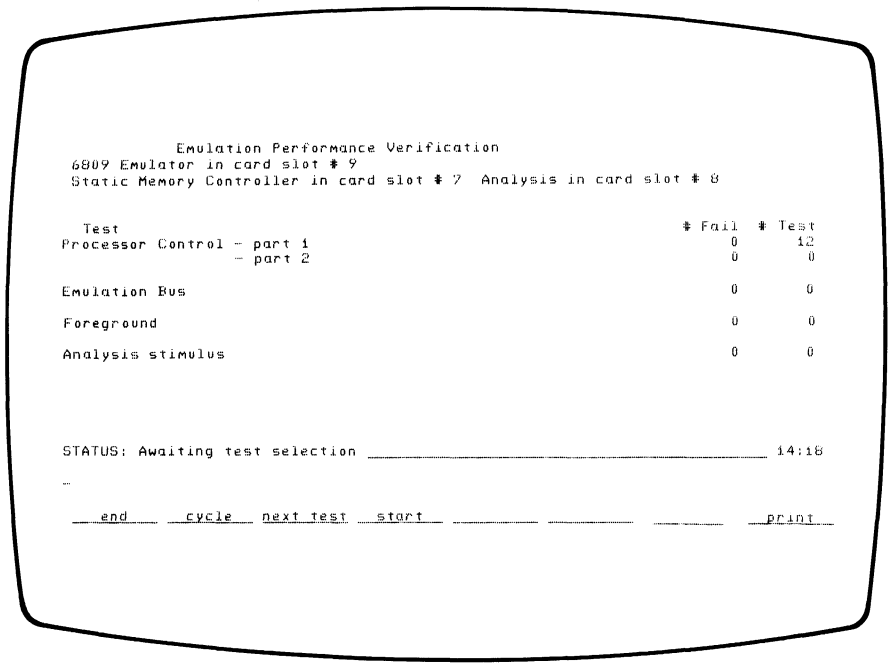
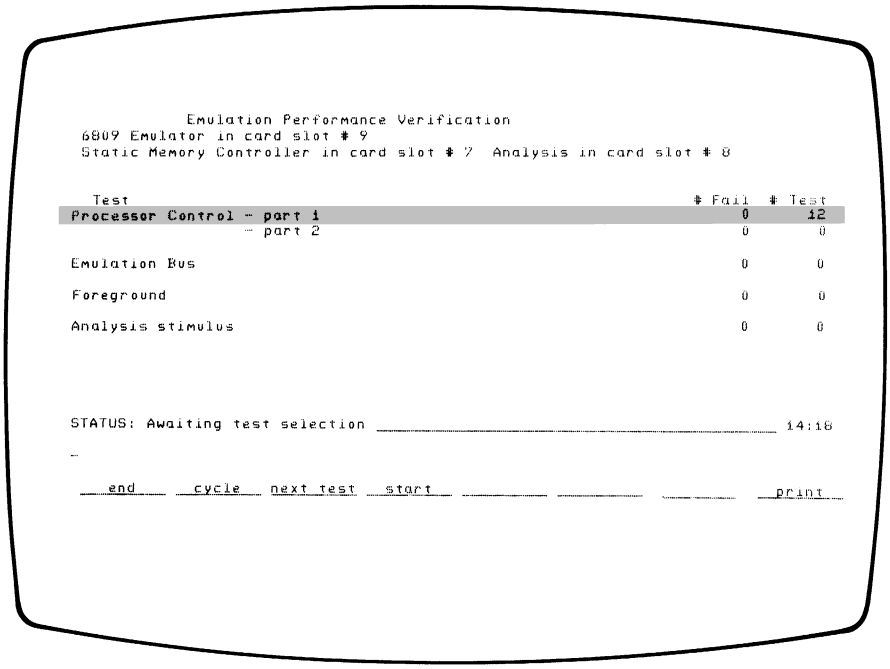
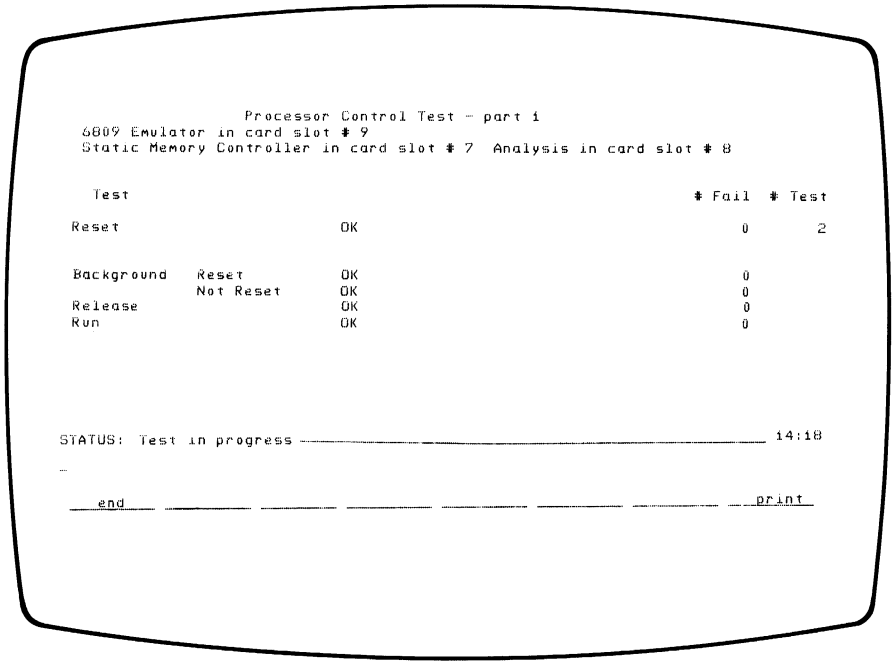


Figure 4-3. Emulator PV Menu

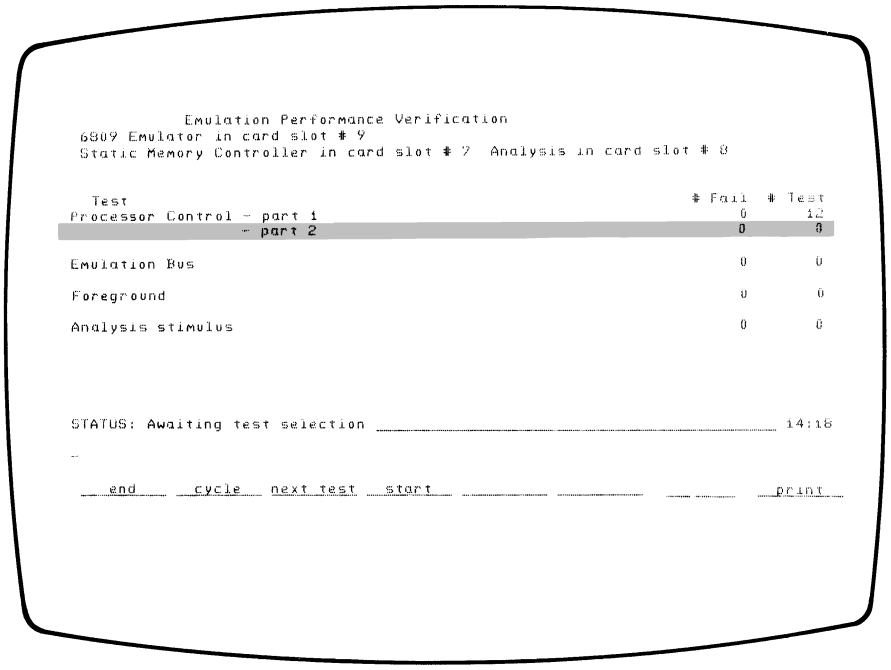


Entry Display

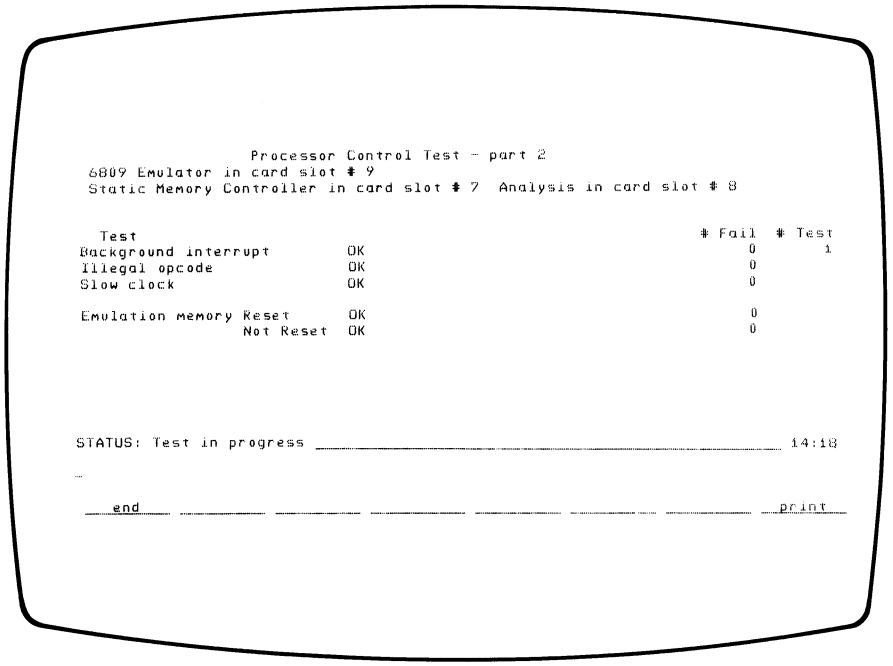


Test Summary

Figure 4-4. Processor Control Test-Part 1 Displays

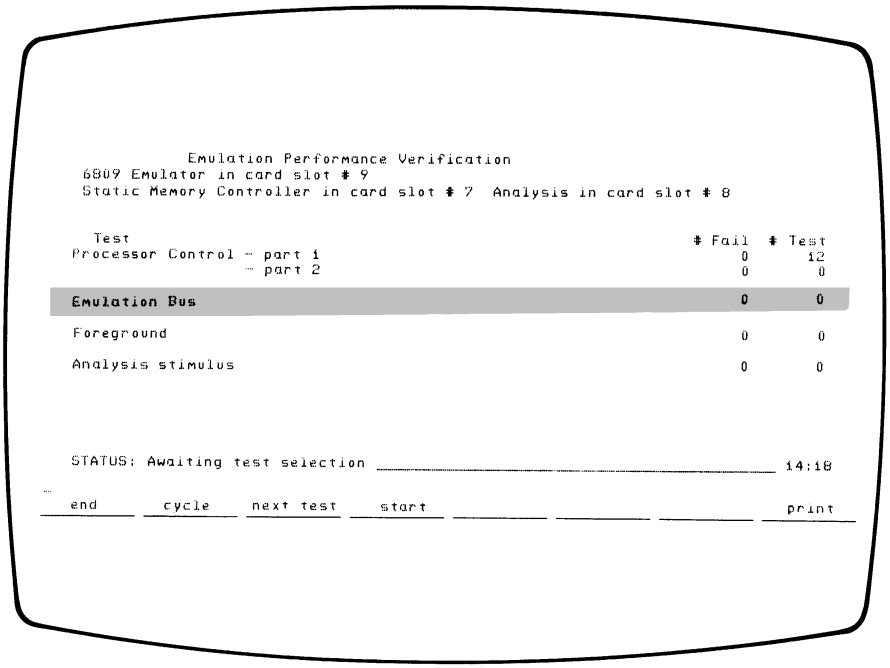


Entry Display

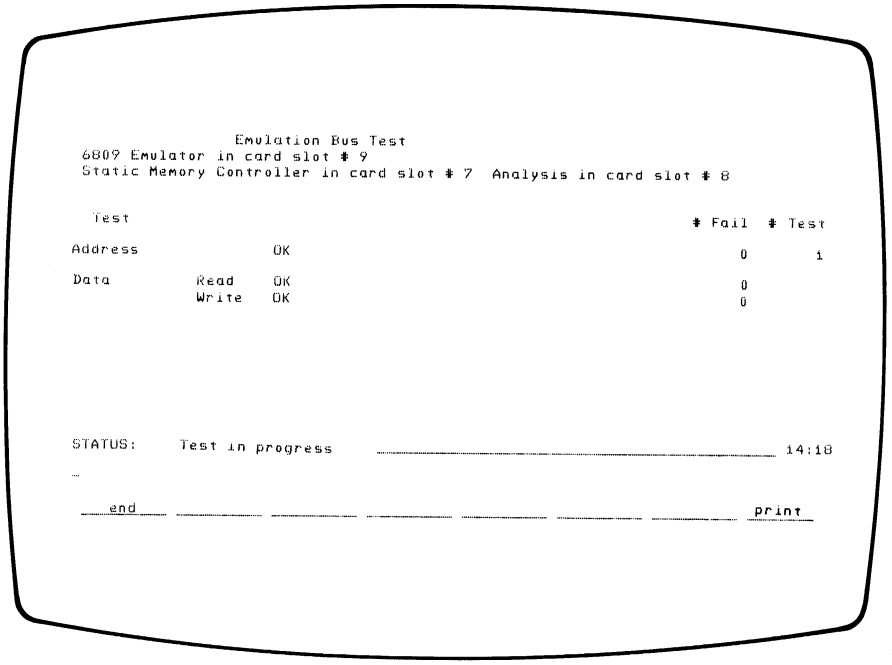


Test Summary

Figure 4-5. Processor Control Test-Part 2 Displays

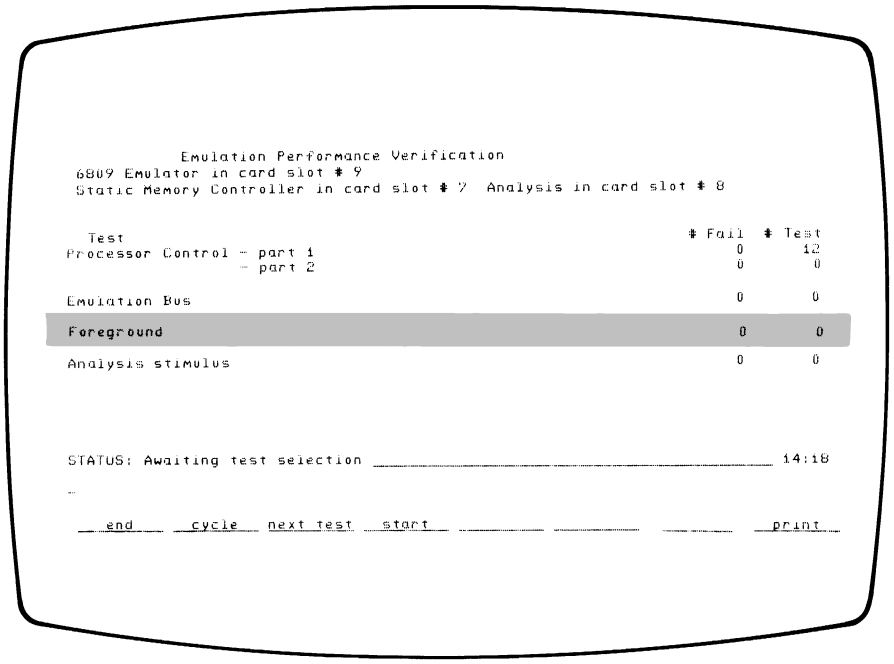


Entry Display

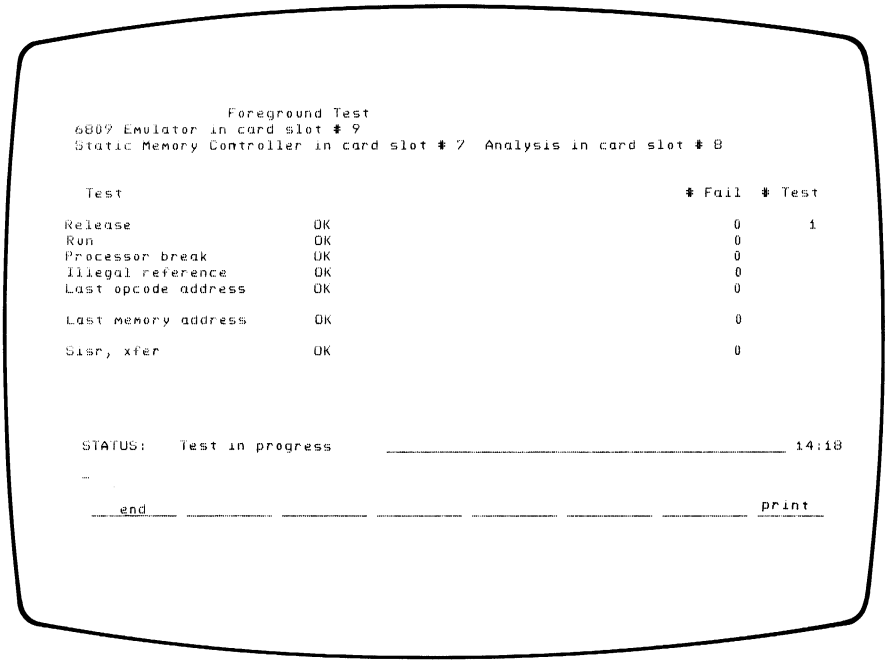


Test Summary

Figure 4-6. Emulation Bus Test Displays

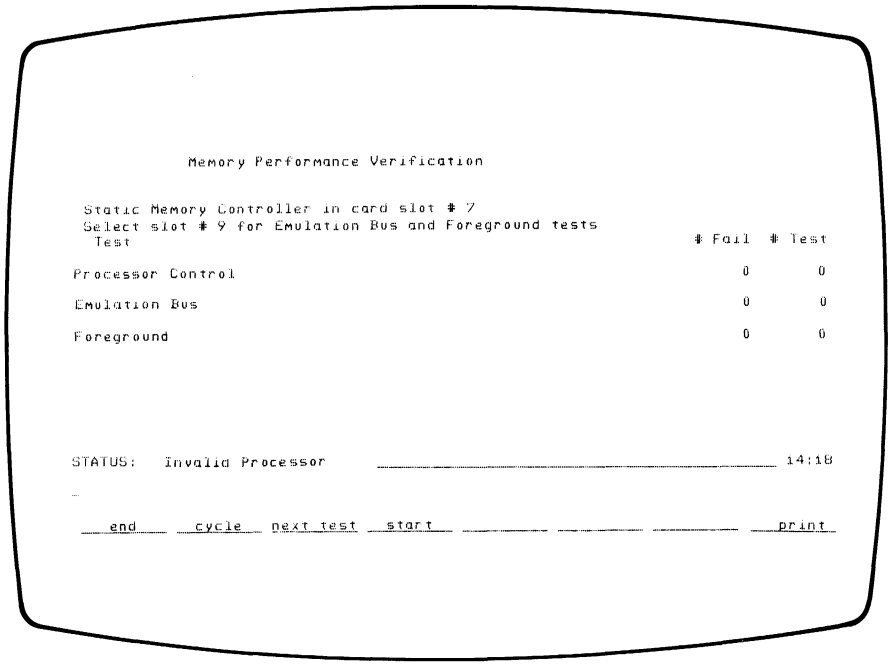


Entry Display

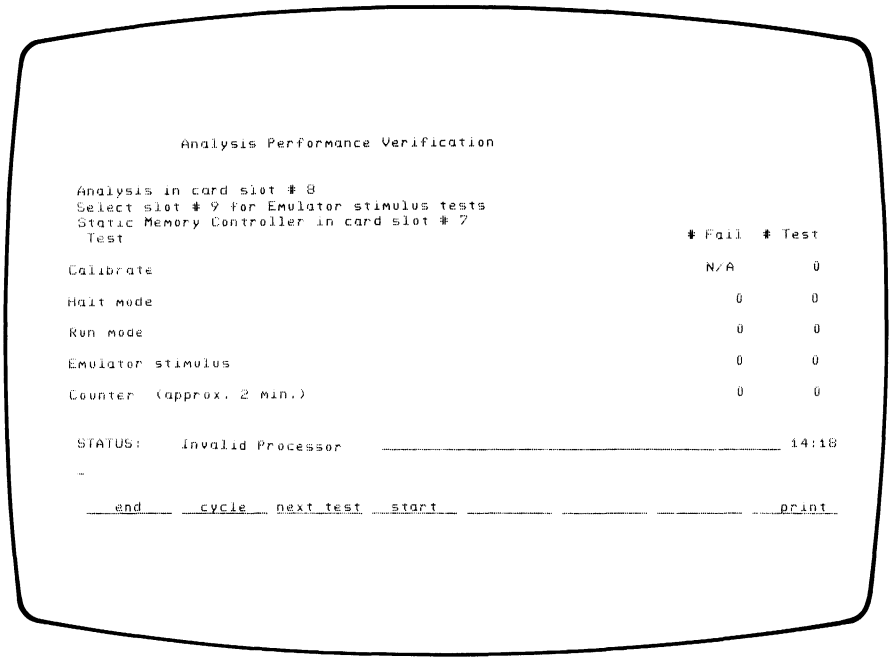


Test Summary

Figure 4-7. Foreground Test Displays



Entry Display



Test Summary

Figure 4-8. Memory and Analysis PV Displays

SECTION V

ADJUSTMENTS

5-1. INTRODUCTION.

5-2. This section provides the adjustment procedures required to return the emulation subsystem to peak operating condition following repairs. The assemblies provided under the Blue Stripe Program for system repair have had these adjustments performed at the factory and should not require readjustment. Included in this section are the adjustment location illustration, the adjustment procedures and the waveforms.

5-3. SAFETY REQUIREMENTS.

5-4. Although this instrument has been designed in accordance with international safety standards, general safety precautions must be observed during all phases of operation, service, and repair of the instrument. Failure to comply with the precautions listed in the Safety Summary at the front of this manual, or with the specific warnings given throughout the manual, could result in serious injury or death. Service adjustments should be performed only by qualified service personnel.

5-5. EQUIPMENT REQUIRED.

5-6. The equipment required to perform the adjustments given in this section is limited to a dual-channel oscilloscope Hewlett-Packard Model 1743 or equivalent. This instrument is a dual channel unit with a delayed sweep, has a bandwidth of 100 MHz, and is capable of time interval measurements with 0.1 nsec resolution and 0.5 nsec accuracy.

5-7. ADJUSTMENTS.

5-8. The adjustment procedures provided in this section are not interrelated and may be performed separately. R-12 is used to adjust the HMAV delay, and R-11 is used to adjust the LWDV delay. The location of the potentiometers and U19 is shown in figure 5-1.

5-9. These adjustments are made at the factory and should not require readjustment. When repairs are made to the board, these adjustments should be checked. For best results allow the instrument to warm up for 15 minutes before making any adjustments.

5-10. ADJUSTMENT PROCEDURES.

WARNING

Adjustment procedures are performed with the power supplied to the instrument and should be performed only by trained service personnel who are aware of the hazards involved (for example, fire and electrical shock).

5-11. For these adjustments the following preliminary steps should be performed:

a. Turn 64000 development station power OFF.

b. Install the extender board (PN 64100-66510) into the option slot to be used for the control board.

c. Install the control board using the procedure given in Section II, Installation, but inserting the control board into the extender board instead of the motherboard.

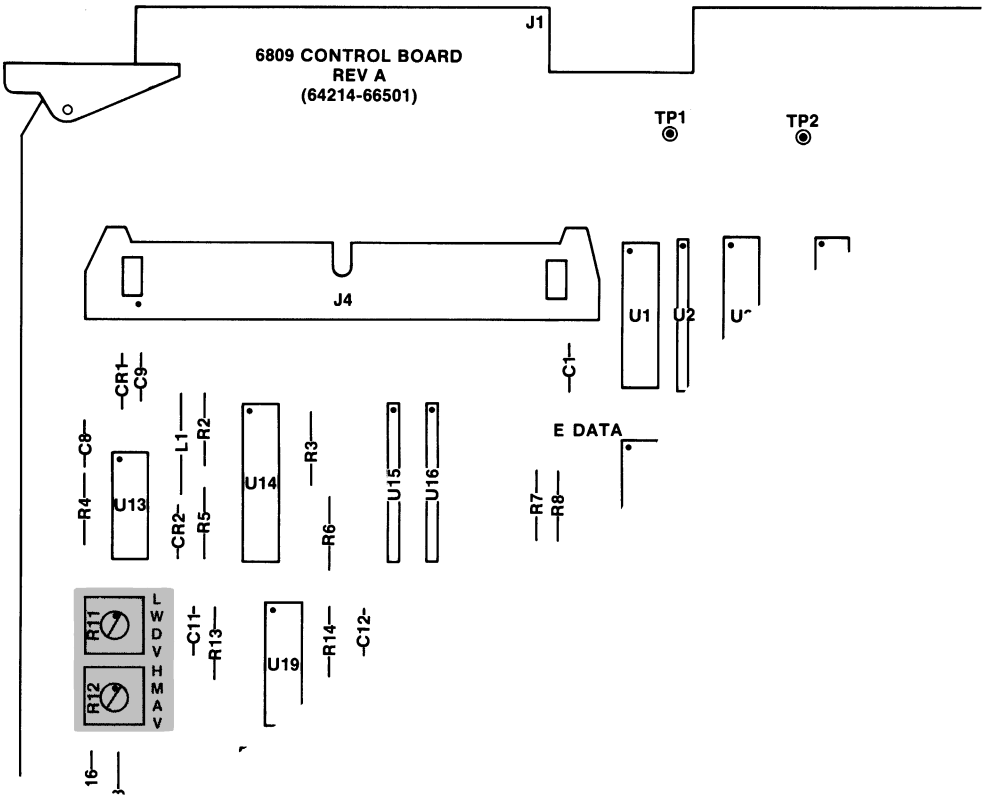


Figure 5-1. Adjustment Locations

5-12. HMAV DELAY ADJUSTMENT.

5-13. The HMAV delay is set using the following procedure:

a. Connect the oscilloscope channel A to U19 pin 4.

b. Connect the oscilloscope channel B to U19 pin 6.

c. Adjust the oscilloscope to trigger on the rising edge of the pulse on channel A and adjust the horizontal sweep for at least a 100 nsec sweep.

d. Adjust R-12 until the wave form shown below is obtained.

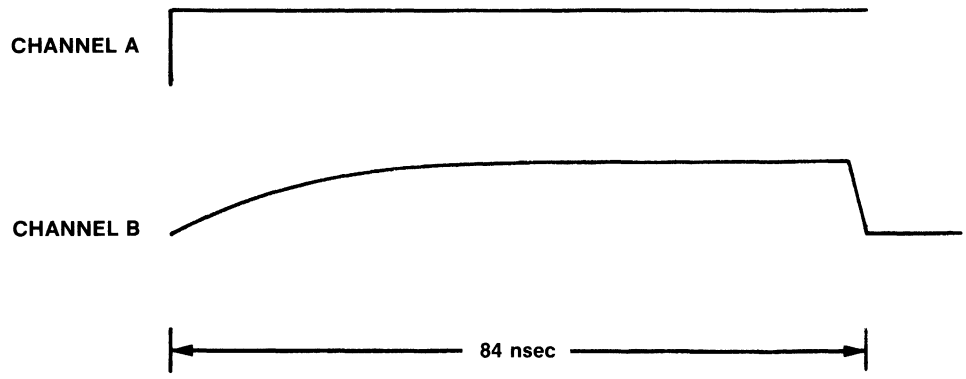


Figure 5-2. HMAV Adjustment Waveforms

5-14. LWDV DELAY ADJUSTMENT.

5-15. The LWDV delay adjustments is set using the following procedure:

a. Connect the oscilloscope channel A to U19 pin 12.

b. Connect the oscilloscope channel B to U19 pin 10.

c. Adjust the oscilloscope to trigger on the rising edge of the pulse on channel A and adjust the horizontal sweep for a sweep of 200 nsec minimum.

d. Adjust R-11 until the waveform shown below is obtained.

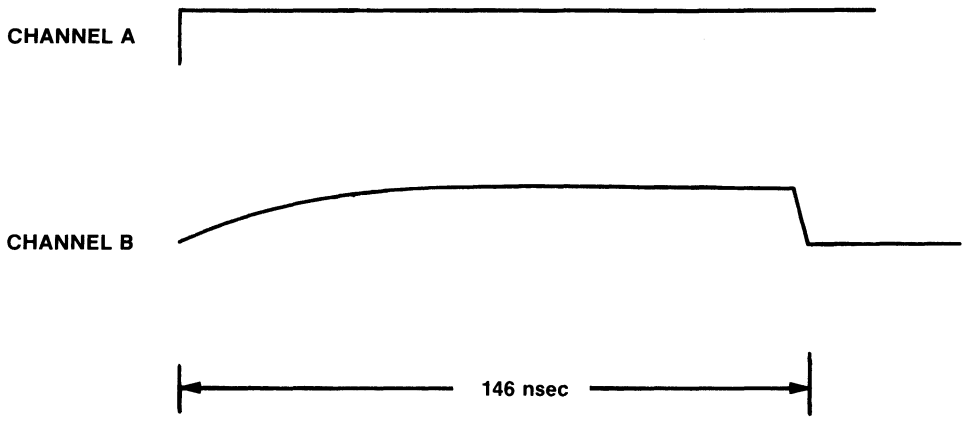


Figure 5-3. LWDV Adjustment Waveforms

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information needed to order replacement parts. Section 6-3 explains the Blue Stripe Program for replaceable assemblies. Table 6-1 lists reference designators and abbreviations used throughout the manual. Table 6-2 lists all Emulator Control Board replaceable parts in assembly/reference designator order.

6-3. BLUE STRIPE PROGRAM.

6-4. The Blue Stripe Program offers factory repaired and tested replacement boards, on an exchange basis only. Exchange assemblies carry a part number different from brand new assemblies and are available at a reduced cost. Emulator Control Board exchange assemblies, Part Number 64214-69501 are available through the Hewlett-Packard Corporate Parts Center. New boards are ordered using Part Number 64214-66501.

6-5. REFERENCE DESIGNATORS AND ABBREVIATIONS.

6-6. Table 6-1 lists the reference designations and abbreviations used in the parts list, schematics and throughout the manual. Reference designations are presented in upper case only. Abbreviations are presented in upper case only in the parts list. Abbreviations with both upper and lower case letters are used in the schematics and other parts of the manual. This results in two forms of the abbreviation. Table 6-1 lists only the upper case form of each.

6-7. REPLACEABLE PARTS LIST.

6-8. Table 6-2 is a preliminary list of replaceable parts. The board components are listed by HP Part Number. The information given for each part consists of the following:

a. The Reference Designator and Manufacturers Part Number.

b. The Hewlett-Packard part number.

c. The quantity in the assembly.

6-9. ORDERING INFORMATION.

6-10. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number and indicate the quantity required to the nearest Hewlett-Packard sales/service office.

6-11. To order a part that is not listed in the replaceable parts table include the instrument model number, instrument repair number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard sales/service office.

6-12. DIRECT MAIL ORDER SYSTEM.

6-13. Within the USA Hewlett-Packard can supply parts through the direct mail order system. The advantages of using the system are as follows:

a. Direct ordering and shipment from the Hewlett-Packard parts center in Mountain View, California.

b. No minimum amount on any mail order (there is a minimum order amount for parts ordered through a local HP office when the order requires billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No-invoices. To receive these advantages, a check or money order must accompany each order.

6-14. Mail-order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are provided at the back of this manual.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without

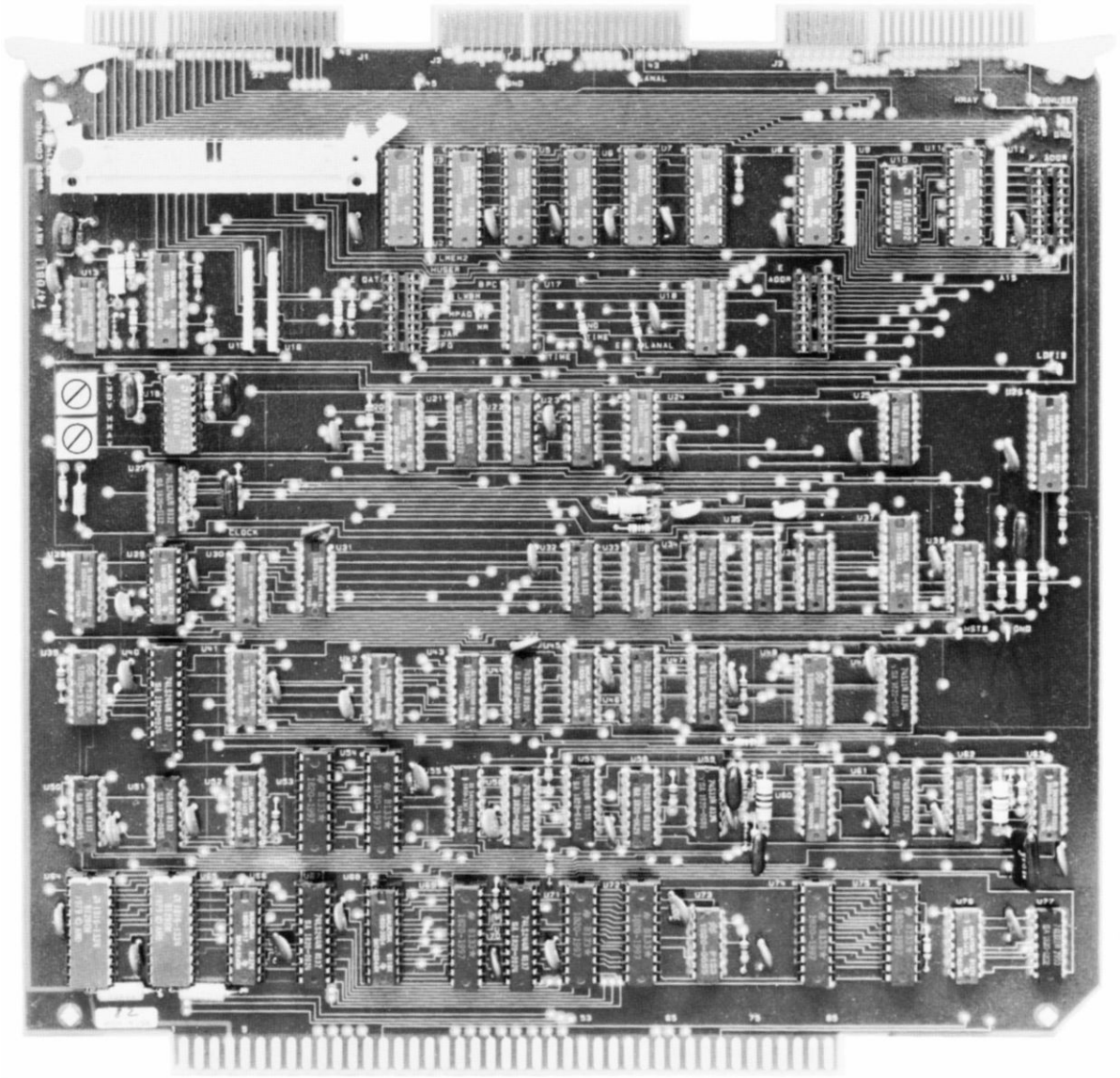


Figure 6-1. 6809 Emulator Control Card

Table 6-2. Replaceable Parts

Reference Designator	Description	Part Number	Quantity
A1	BD ASY-CTL 6809	64214-66501	1
W1,W2	CABLE-MEMORY	8120-3351	2
	A1		
C19,41	CF MI 330P 500V	0140-0207	2
C1-8,10,13-17,21,22,24-40, 42,44,45,47-56	CF CE .01UF 100V	0160-2055	46
C9,20,43	CF MI 100P 300V	0160-2204	3
C23	CF MI 360PF 300V	0160-2209	1
C46	CF MI 510P 300V	0160-2211	1
C11,12	CF MI 27P 300V	0160-2306	2
C18	CF TA 4.7UF 10V	0180-0309	1
C57,58	CF TA 15U 20V	0180-1746	2
TP1-19	TERM-TEST POINT	0360-0535	19
R1,3,6,15,18,20,21,23-29	RF .2500 1000 10	0684-1021	21
R17,R40	RF .12MF 316 1	0698-3444	1
R2,7	RF .12MF 221 1	0757-0282	2
R9,10	RF .12MF 10 1	0757-0346	2
R30	RF .12MF 121 1	0757-0403	1
R5,8,37	RF .12MF 274 1	0757-0409	3
R4,19,22,31,32	RF .12MF 511 1	0757-0416	5
R13	RF .12MF 4.75K 1	0757-0437	1
R16	RF .12MF 243K 1	0757-0474	1
R14	RF .12MF 1.47K 1	0757-1094	1
U10,19,29	SOCKET-IC 16 PIN	1200-0607	6
U64,65	SOCKET 22 PIN	1200-0612	2
U1,3-8,11,40,53,54 66-72,74,75	SOCKET-IC 20 PIN	1200-0639	20
MP1	POLARIZING KEY	1251-5595	2
J4	CONN-50 P MREJT	1251-5653	1
MP2	PIN-GRV .062X .250	1480-0116	2
U2,9,12,15,16	RES NET SPEC SIP	1810-0430	5
U10	IC-27LS00N RAM	1816-1092	1
U64,65	IC 93422 RAM	1816-1334	2
U34-36,46,47,56,58	IC-74S112	1820-0629	7
U48,73	IC 7425N	1820-0655	2
U13,17,18,24,33,42,60	IC 74S00	1820-0681	7
U57	IC 74S04	1820-0683	1
U32,50,51	IC 74S10	1820-0685	3
U49,59,61	IC 74S11	1820-0686	3
U28,38,63	IC 74S74	1820-0693	3
U30	IC 7412N	1820-0907	1
U27	IC 74LS74AN SLT	1820-1112	1
U39	IC 74LS175N SLT	1820-1195	1
U77	IC-74LS10	1820-1202	1
U41	IC 74LS128	1820-1216	1
U23,21,62	IC 74S02	1820-1322	3
U31,43,55	IC 74S08	1820-1367	3
U76	IC 74LS14	1820-1416	1
U29	IC 74LS123	1820-1423	1
U20,45	IC 74LS161	1820-1430	2
U52	IC 74LS163	1820-1432	1
U22,25,44	IC 74S32	1820-1449	3
U14,26	IC 74S241	1820-1624	2
U1,3-8,11,37	IC 74S240N	1820-1633	9
U19	IC 26S02	1820-1782	1

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	Description	Part Number	Quantity
U66	IC 74LS 240N	1820-1917	1
U53,54,69,71,72,74,75	IC 74LS374N SLT	1820-1997	7
U40,67,68,70	IC 74LS244N SLT	1820-2024	4
CR1-8	DIODE SCHOTTKY	1901-0535	8
R12	RV CMT 2K .5W	2100-0567	1
R11	RV CMT 5K .5W	2100-3252	1
MP3	EXTRACTOR-PC BD	64214-85001	1
MP4	EXTRACTOR-PC BD	64214-85002	1
MP5	LABEL-WARNING	7120-6492	1
MP6	LABEL-RED DOT	7124-0269	AR
MP7	LABEL-YELLOW DOT	7124-0270	AR
L5	LFMO 15.0UH 40MC	9100-1620	1
L3	LFMO .22UH 510MC	9100-2251	1
L1,L2	LFMO 8.2UH 50MC	9140-0105	2
L4	LFMO 10UH 45MC	9140-0114	1

SECTION VII

MANUAL CHANGES

7-1. INTRODUCTION.

7-2. This section contains information required to backdate or update this manual for a specific instrument.

7-3. MANUAL CHANGES.

7-4. This manual applies directly to the instrument having the same serial prefix shown on the manual title page. If the serial prefix of the instrument is not the same as the one on the title page, find your serial prefix in Table 7-1. and make the changes to the manual that are listed for that serial prefix. When making changes listed in Table 7-1, make the change with the highest number first. Example: if backdating changes 1,2,and 3 are required for your serial prefix, do Change 3 first, then Change 2, and finally Change 1.

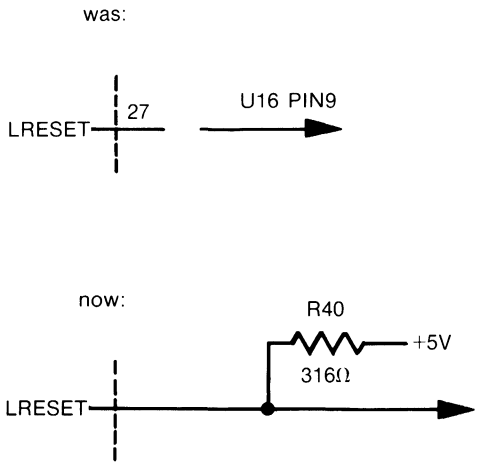
7-5. If the serial prefix of your instrument is not listed either on the title page or in Table 7-1, refer to an enclosed manual changes sheet for updating information. Also, if a MANUAL CHANGES sheet is supplied, make all indicated ERRATA changes.

Table 7-1. Manual Changes

64214A

Serial Prefix	Make Changes
2150A	1

CHANGE 1



SECTION VIII

THEORY AND SCHEMATICS

8-1. INTRODUCTION.

8-2. This section contains information for servicing the Emulator Control Board. Figure 8-1 is a component locator for the board and figures 8-2 through 8-8 are the schematic.

8-3. SAFETY.

8-4. Read the safety warnings at the front of this book and at the front of the mainframe service manual, the service overview manual and the applicable emulator subsystem manual before servicing this Emulator Control Board.

8-5. COMPONENT LOCATOR.

8-6. The component locator provides the reference designators and locations for each replaceable part contained on the printed circuit assembly. The component locator is provided as a fold-out drawing.

8-7. SCHEMATIC DIAGRAMS.

8-8. The schematic diagrams are presented as fold-out sheets located at the end of this section. A list of standard reference designators and abbreviations is presented in Section VI of this manual. Table 8-1 describes the techniques used in the development of the logic symbols. Table 8-2 describes the development of the schematic symbols.

8-9. MNEMONICS.

8-10. Signals in the Model 64214A have been assigned mnemonics which describe the active state and function of the signal lines. A prefix letter (H,L,P or N) indicates the active state of the signal and the remaining letters indicate its function. An "H" prefix indicates that the function is active in the high state; an "L" prefix indicates that it is active in the low state. For devices that are edge sensitive the prefix "P" indicates that the function is active on the positive going edge; the prefix "N" indicates that the device is active on the negative going edge. These mnemonics are listed in table 8-1.

Table 8-1. Mnemonics

TO/FROM EMULATION POD

A0-15	EMULATOR ADDRESS 0-15. Buffered emulation processor address bus.
DMA	DIRECT MEMORY ACCESS. This input signal to the emulator indicates that the user system is performing a DMA transfer.
DMA/BREQ	DIRECT MEMORY ACCESS/BUS REQUEST. This signal generated by U7A is applied to the emulation processor.
ED0-ED7	EMULATION DATA 0-7. Eight bit wide bidirectional emulation data bus from U39 and U41.
EFG	EMULATION FOREGROUND. Goes high whenever a reference is made to memory addresses mapped as foreground memory. Also an interschematic mnemonic.
EINT/EXT	EMULATION INTERNAL/EXTERNAL CLOCK. Clock select signal sent to the pod from the mainframe processor through the control register to operate U36 and U37. When high, the internal oscillator in the pod is enabled, when low, the target system clock is used. Also an inter-schematic mnemonic.
ELBKG	EMULATION LOW BACKGROUND. Goes low when the background controller enters the background state.
ELREFREQ	EMULATION LOW REFRESH REQUEST. Not used with current memory and analysis boards. When used, would provide for stopping the emulator processor for an emulation memory refresh cycle. Held high.
EPFG	EMULATION PRE-FOREGROUND. Goes high to indicate the background controller is going to change from background to foreground mode.
EVMA	EMULATION VALID MEMORY ADDRESS. Modified HVMA from the emulator processor. Goes high to indicate a valid memory address is present on the address bus (A0-15)
FETCH	This status line, generated on the synchronizer board, is high for the first instruction cycle and stays high until the first operand fetch or write cycle.
FORCENMI	FORCE NMI. A signal generated by the mainframe BPC to force a non-maskable interrupt when the emulator leaves background.
FORCEUSER	FORCE USER. Forceuser inhibits HMAV (high Memory Available) which inhibits the emulator memory and forces user memory access.
R/W	READ/WRITE. The emulation processor sets this line high for read operations and low for write operations.

Table 8-1. Mnemonics (Cont'd)

HFETCH	HIGH FETCH. High Fetch 1. This status signal, generated on the synchronizer board, is high only during the first instruction cycle.
HISR	HARDWARE INTERRUPT SERVICE ROUTINE. This signal, generated on the Synchronizer board, signals the analyzer that a hardware interrupt has occurred and also signals the end of the subroutine.
INTRV	INTERRUPT VECTOR. This signal, generated on the synchronizer board, gates BS and BA to generate INTRV which is high when an interrupt vector fetch is occurring.
LBA	LOW BUS AVAILABLE. Buffered HBA from emulation processor. Goes high to indicate the address bus is available as during a processor halt or a wait state.
LDEFIB	LOW DEFIBRILLATION. Goes low when the mainframe processor resets the emulation processor in the pod.
LHALT	LOW HALT. A microprocessor pin status register bit from the pod emulator processor HALT pin.
LRESET	LOW RESET. Emulation reset line. Goes low whenever a reset is applied to the emulation processor.
SISR	SOFTWARE INTERRUPT SERVCIE ROUTINE. This status line is generated on the Synchronizer Board to signal the analyzer that a software interrupt vector fetch is occurring.
Q/E	Clock inpurt required by the 6309 processor. These inputs may be taken from the user system or may be generated on the Processor Board.
TRANSFER	TRANSFER. This satus signal generated on the synchronizer board signals a transfer of control from the emulator to the target system.

Table 8-1. Mnemonics (Cont'd)

MAINFRAME INTERFACE

LA0-7 LOW ADDRESS 0-7. The low-order eight bits from the mainframe processor address bus. Also an Inter-schematic mnemonic.

LA8 LOW ADDRESS 8. The ninth bit from the mainframe address bus. Also an Inter-schematic mnemonic.

LD0-7 LOW DATA 0-7. Bidirectional 8-bit data bus. Lower half of 16-bit communications path from the mainframe processor to the emulator control card. Also an Inter-schematic mnemonic.

LD8-15 LOW DATA 8-15. Bidirectional 8-bit data bus. Upper half of the 16-bit communications path from the mainframe processor to the emulator control card.

LIDEN LOW IDENTIFICATION ENABLE. Goes low when the mainframe processor scans the ID codes of the cards on the mainframe bus to enable each card to respond with its ID.

LMSYN LOW MEMORY SYNC. Goes low to force the mainframe processor to wait for the current read or write cycle to be completed by the emulation subsystem. Also an Interschematic mnemonic.

LSEL LOW SELECT. Input from mainframe (LSS0-9) I/O board. Goes low when the mainframe processor selects this board. Also an interschematic mnemonic.

LSTB LOW STROBE. Goes low during a mainframe processor read to allow the selected device to drive the data bus. Goes low during a mainframe processor read to indicate bus data is valid. Also an interschematic mnemonic.

LSTM LOW START MEMORY. Goes low when the mainframe processor initiates a memory cycle and address bus and bus data is valid. Also an Interschematic mnemonic.

LWRT LOW WRITE. Goes low to indicate a mainframe processor write to the selected device. Also an interschematic mnemonic.

Table 8-1. Mnemonics (Cont'd)

EMULATION SUBSYSTEM INTERFACE

BA0-15 BUFFERED ADDRESS 0-15. Used to access background and emulation memory. Also a Memory and Analysis Interface mnemonic.

BA BUS AVAILABLE. Input from Emulation microprocessor. Goes high to indicate a processor halt or wait state. Also a Pod Interface, and a Memory and Analysis Interface mnemonic.

CNREGCLK CONTROL REGISTER CLOCK. Gates mainframe processor data into the control register.

ENILLOP ENABLE ILLEGAL OPCODE DETECTOR. Enables the illegal opcode detector under control of the control register.

ENJAMCTR ENABLE JAM COUNTER. Goes high to enable the Jam counter.

E2D0-7 SECOND EMULATION DATA BUS. Nonmultiplexed 8-bit bidirectional data bus used for background memory, illegal opcode detector and synchronizer operations.

FG FOREGROUND. Goes high to indicate the emulation subsystem is running in the foreground memory.

HANAL HIGH ANALYSIS. Goes high to store the last referenced memory address into the last address register.

HBGKCS HIGH BACKGROUND CHIP SELECT. Enables Background Memory RAMs.

HBMR HIGH BACKGROUND MEMORY REQUEST. Goes high when the mainframe processor requests a Background Memory operation.

HBREAK HIGH BREAK. Goes high to cause an emulator processor break.

HERD HIGH EMULATION READ. Buffered R/W signal. Goes high when emulator is in a read cycle.

HEWRT HIGH EMULATOR WRITE. Inverted R/W signal. Goes high to indicate the emulation processor is performing a write operation.

HFETCH1 HIGH FETCH 1. Goes high during an emulator opcode fetch.

HILLOP HIGH ILLEGAL OPCODE. Goes high to indicate an illegal opcode was detected.

HMAV HIGH MEMORY AVAILABLE. Goes high when the emulator is not using memory.

Table 8-1. Mnemonics (Cont'd)

HUSER	HIGH USER. Goes high when the current address on the emulation address bus is mapped to user memory.
INT/EXT	INTERNAL/EXTERNAL CLOCK. Clock select signal sent to the pod by the mainframe processor through the control register. When high the oscillator in the pod is selected, when low the target system clock will be used.
JAM	JAM. Goes high when the Background Controller is outputting the jam addresses onto the address bus.
JAMP	JAM PRIME. Goes high to enable the JAM counter and the address buffer from the JAM counter to the lower 8 bits of BA0-7.
LANAL	LOW ANALYSIS. Goes high to store analysis data nto the internal analysis board.
LAB	LOW AVAILABLE BUS. Inverted BA signal. Goes low when the emulation processor is not using the bus.
LBDEFIB2	LOW BUFFERED DEFIBRILATE 2. Buffered LDEFIB2 signal which is part of the emulation reset function. Goes low when mainframe processor resets the emulator.
LBKG	LOW BACKGROUND. Goes low when the background controller enters the background mode.
LBKGP	LOW BACKGROUND PRIME. Goes low to signal the pod that the system is in the background mode.
LBKGWR	LOW BACKGROUND WRITE. Goes low to indicate a write to background RAM is enabled.
LDEFIB	LOW DEFIBRILLATION. Goes low when the mainframe processor resets the processor in the emulator pod.
LDEFIB2	LOW DEFIBRILLATION 2. Goes low to initialize timing circuits when the mainframe processor resets the emulation subsystem.
LDEFIB3	LOW DEFIBRILLATION 3. Goes low to initialize the memory operation sequence in the background controller when the mainframe processor resets the emulation subsystem.
LD0-7	LOW DATA 0-7. Bidirectional 8-bit data bus. Communications path from the mainframe processor the emulator control card.
LEBREAK	LOW EMULATION BREAK. Goes low when the emulation bus requests a break of the emulation system.

Table 8-1. Mnemonics (Cont'd)

LEWRT LOW EMULATOR WRITE. Buffered emulator R/W signal. Goes low when the emulator is in a write cycle.

LFG LOW FOREGROUND. Goes low when the Background Controller is in the foreground mode.

LHOST LOW HOST. Goes low when the mainframe processor initiates a background cycle.

LHOSTBRK LOW HOST PROCESSOR BREAK. Goes low when the mainframe processor requests an interrupt of the emulation processor.

LIDEN LOW IDENTIFICATION ENABLE. Goes low when the Mainframe processor scans the ID codes of the cards on the mainframe bus to enable each card to respond with its ID.

LIMPJAM LOW IMPENDING JAM. Goes low to indicate that a JAM cycle will occur on the next falling edge of LMEM1.

LIQ LOW INTERRUPT QUALIFIER. Inverted IQ signal.

LJAM LOW JAM. Goes low to indicate the emulator is in the JAM mode.

LJAMP LOW JAM PRIME. Used to select the source for the emulator address signals on the emulation bus. Selects between the Jam Counter and the emulation processor.

LLADDREAD LOW LAST ADDRESS READ. Goes low when the mainframe processor reads the Last Opcode Address Register.

LMBRKS LOW MEMORY BREAK STATUS. Goes low when the Emulation Memory Board asserts a break.

LMEM LOW MEMORY. Used to synchronize the background memory controller to the emulation processor.

LMEM2 LOW MEMORY 2. Goes low to indicate that the address currently on the address bus is valid, used as a clock by the Background Controller.

LMSYN LOW MEMORY SYNC. Goes low to force the mainframe processor to wait until completion of the current read or write cycle by the emulator.

LLOPREAD LOW LAST OPCODE READ. Goes low when the mainframe processor reads The Last Opcode Register.

Table 8-1. Mnemonics (Cont'd)

LREFREQ LOW REFRESH REQUEST. Not used with current memory and anaylsis boards. When used, would allow the emulation processor in the pod to be stopped for emulation memory refresh cycles. Since no dynamic memory is now used, this line is held high.

LRESET LOW RESET. Buffered emulation reset line. Goes low whenever a reset is applied to the emulation processor.

LSEL LOW SELECT. Input from mainframe I/O board LSS0-9. Goes low when the mainframe processor selects this board.

LSTB LOW STROBE. Goes low during a mainframe processor read to allow the device addressed to drive the data bus. Goes low during a write when the bus data is valid.

LSTM LOW START MEMORY. Goes low when the mainframe processor initiates a memory cycle to indicate the address bus data is valid.

LSTREAD LOW STATUS REGISTER READ. Goes low when the mainframe processor reads the contents of the microprocessor pin status and miscellaneous status registers.

LUSER LOW USER. Goes low to indicate the current address on the emulation address bus is mapped to user memory.

LWBM LOW WRITE BACKGROUND MEMORY. Goes low to enable writes to background memory.

LWDV LOW WRITE DATA VALID. Goes low during a memory or I/O write cycle when data on the emulation data bus is valid. Also a Memory and analysis Interface mnemonic.

LWRT LOW WRITE. Goes low to indicate a mainframe processor write to the addressed device.

MEM MEMORY. Goes high to indicate the address on the emulation address bus is valid. Used to clock the start Jam Counter flip-flop.

PFG PREFOREGROUND. Goes high to indicate the background controller is going to change from background to foreground mode.

PMOP PRE-MEMORY OPERATION. Goes high to indicate a read or write operation on user memory by the emulator will take place on the next falling edge of LMEM2.

RDBKGSTB READ BACKGROUND STROBE. Goes low to indicate the mainframe processor is performing a read of background memory.

Table 8-1. Mnemonics (Cont'd)

R/W	READ/LOW WRITE. The emulation processor holds this line high for read operations and low for write operations.
WRBKGSTB	WRITE BACKGROUND STROBE. Goes low to indicate a mainframe processor write to background memory.

Table 8-2. Logic Symbols

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term.)

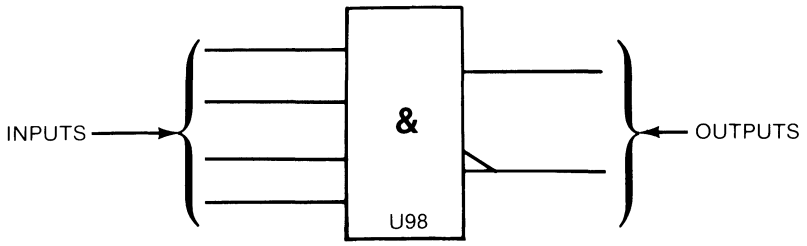
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

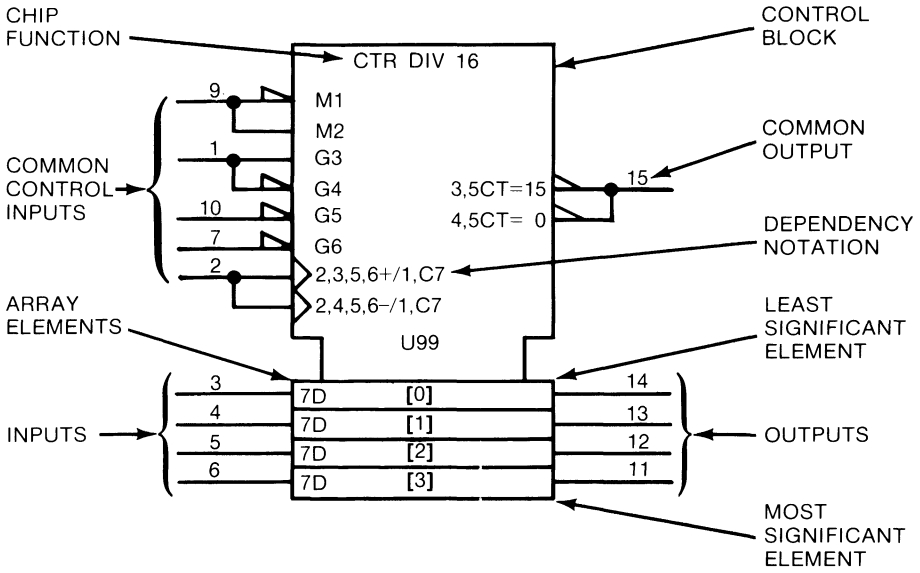
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. Unless indicated, the least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in **[ ]**).

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Table 8-2. Logic Symbols (Cont'd)

INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.

b. Interconnection (Z) indicates connections inside the symbol.

c. Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.

d. Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.

e. Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).

f. Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.

g. Address (A) identifies the address inputs.

h. Transmission (X) identifies bi-directional inputs and outputs that are connected together when the transmission input is true.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (compliments state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection
		X	Transmission

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Table 8-2. Logic Symbols (Cont'd)

OTHER SYMBOLS

Analog Signal	Inversion	Shift Right (or up)
& AND	O Negation	/ Solidus (allows an input or output to have more than one function)
Bit Grouping	Nonlogic Input/Output	▽ Tri-State
Buffer	Open Circuit (NPN) (external resistor)	, Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.
! Compare	Open Circuit (PNP) (external resistor)	( ) Used for factoring terms using algebraic techniques.
Dynamic	≥1 OR	[ ] Information not defined.
=1 Exclusive OR	Passive Pull Down (internal resistor)	Φ Logic symbol not defined due to complexity.
Hysteresis	Passive Pull Up (internal resistor)	
? Interrogation	Postponed	
— Internal Connection	← Shift Left (or down)	

LABELS

BG	Borrow Generate	CO	Carry Output	J	J Input
BI	Borrow Input	CP	Carry Propagate	K	K Input
BO	Borrow Output	CT	Content	P	Operand
BP	Borrow Propagate	D	Data Input	T	Transition
CG	Carry Generate	E	Extension (input or output)	+	Count Up
CI	Carry Input	F	Function	–	Count Down

MATH FUNCTIONS

Σ	Adder	>	Greater Than
ALU	Arithmetic Logic Unit	<	Less Than
COMP	Comparator	CPG	Look Ahead Carry Generator
DIV	Divide By	π	Multiplier
=	Equal To	P-Q	Subtractor

CHIP FUNCTIONS

BCD	Binary Coded Decimal	DIR	Directional	RAM	Random Access Memory
BIN	Binary	DMUX	Demultiplexer	RCVR	Line Receiver
BUF	Buffer	FF	Flip-Flop	ROM	Read Only Memory
CTR	Counter	MUX	Multiplexer	SEG	Segment
DEC	Decimal	OCT	Octal	SRG	Shift Register

DELAY and MULTIVIBRATORS

	Astable
100 ns	Delay
1	Nonretriggerable Monostable
NV	Nonvolatile
	Retriggerable Monostable

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Table 8-3. Schematic Diagram Notes

ETCHED CIRCUIT BOARD

FRONT PANEL MARKING

REAR-PANEL MARKING

MANUAL CONTROL

SCREWDRIVER ADJUSTMENT

TP1 ELECTRICAL TEST POINT TP (WITH NUMBER)

NUMBERED WAVEFORM NUMBER CORRESPONDS TO ELECTRICAL TEST POINT NO.

LETTERED TEST POINT NO MEASUREMENT AID PROVIDED

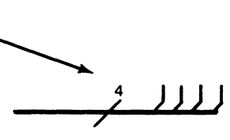
COMMON CONNECTIONS. ALL LIKE-DESIGNATED POINTS ARE CONNECTED.

① **3** NUMBER ON WHITE BACKGROUND = OFF-PAGE CONNECTION.
LARGE NUMBER ADJACENT = SERVICE SHEET NUMBER FOR OFF-PAGE CONNECTION.

Ⓐ CIRCLED LETTER = OFF-PAGE CONNECTION BETWEEN PAGES OF SAME SERVICE SHEET.

INDICATES SINGLE SIGNAL LINE

NUMBER OF LINES ON A BUS



(925) WIRE COLORS ARE GIVEN BY NUMBERS IN PARENTHESES USING THE RESISTOR COLOR CODE

[(925) IS WHT-RED-GRN]

0 - BLACK	5 - GREEN
1 - BROWN	6 - BLUE
2 - RED	7 - VIOLET
3 - ORANGE	8 - GRAY
4 - YELLOW	9 - WHITE

* OPTIMUM VALUE SELECTED AT FACTORY, TYPICAL VALUE SHOWN; PART MAY HAVE BEEN OMITTED.

UNLESS OTHERWISE INDICATED:
RESISTANCE IN OHMS
CAPACITANCE IN PICOFARADS
INDUCTANCE IN MICROHENRIES

μP	=	MICROPROCESSOR
P/O	=	PART OF
NC	=	NO CONNECTION
CW	=	CLOCKWISE END OF VARIABLE RESISTOR

STD-20-09-81

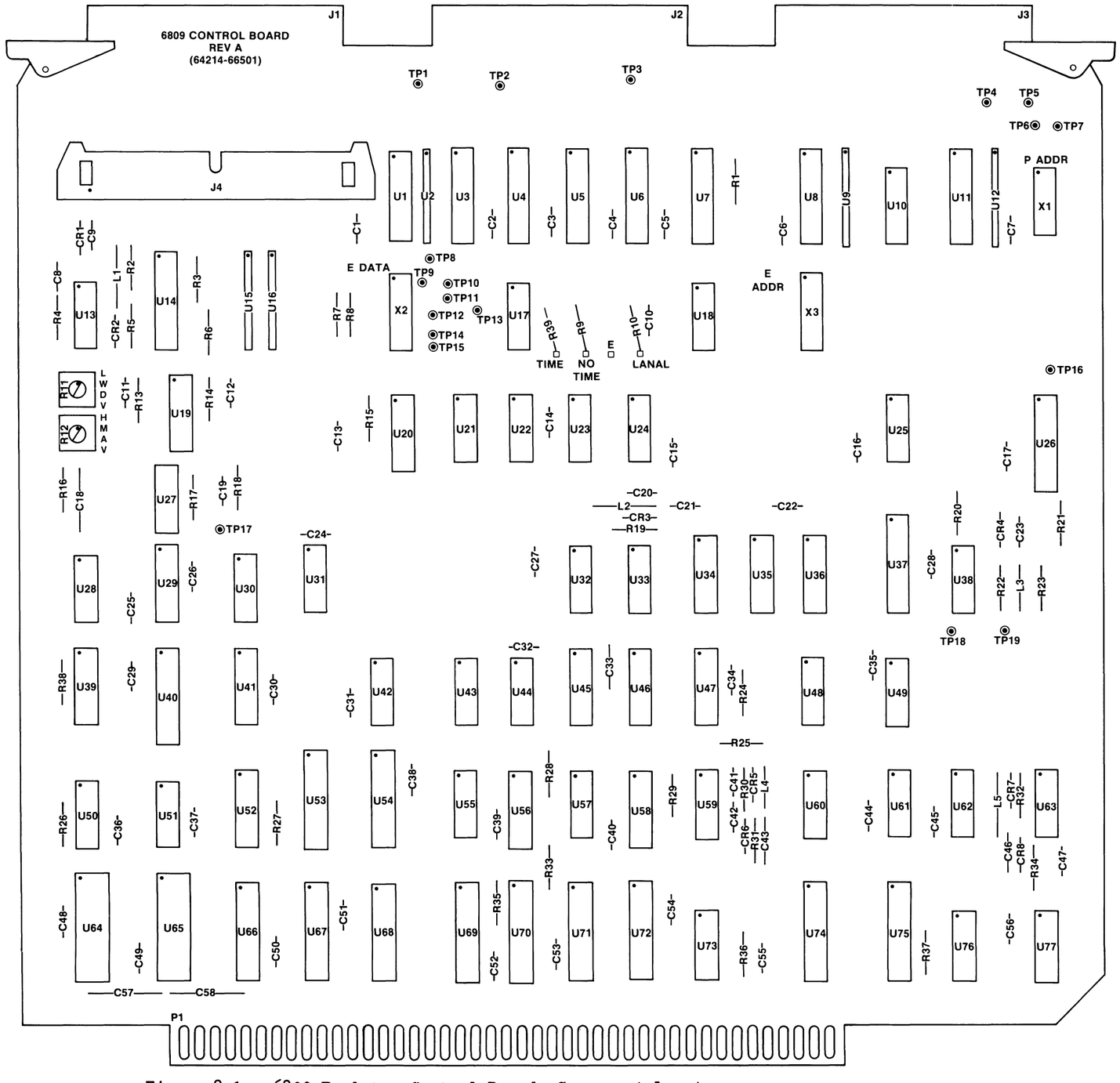
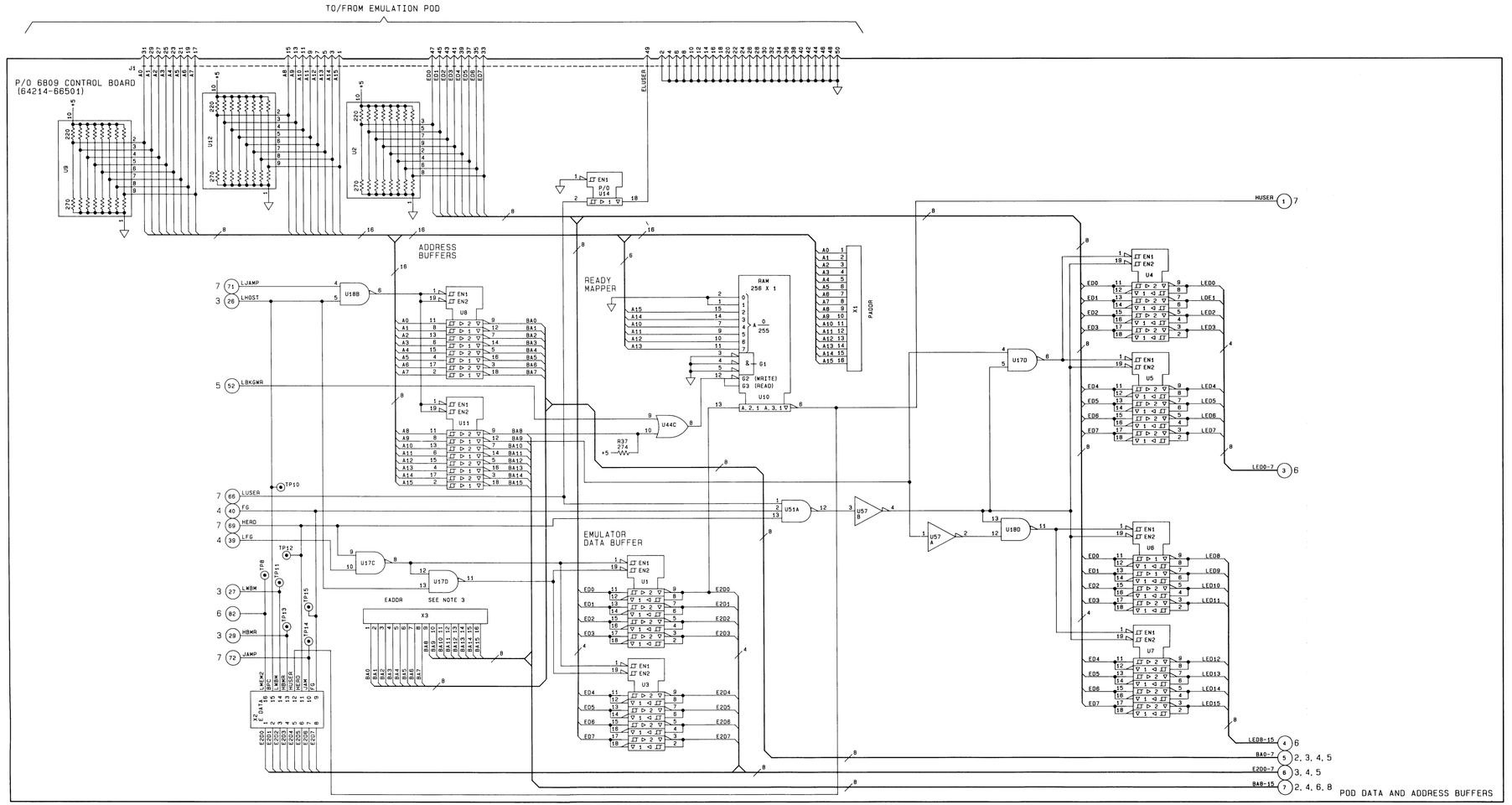
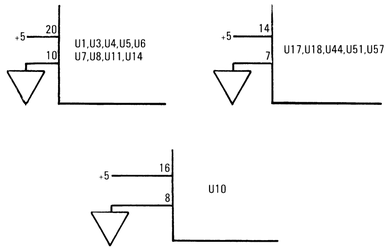


Figure 8-1. 6809 Emulator Control Board, Component Locator



IC POWER SUPPLY PIN CONFIGURATION



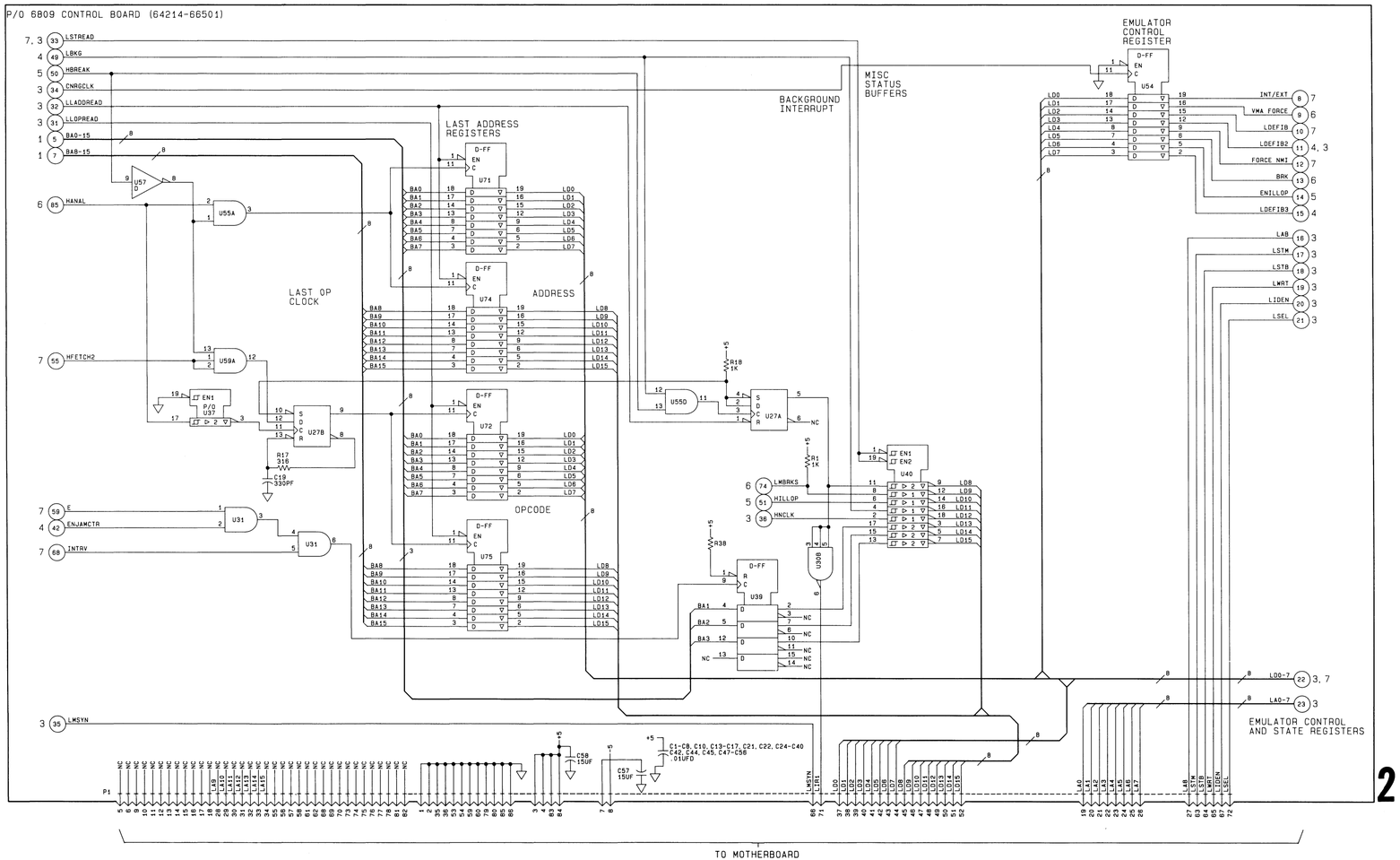
ICS ON THIS SCHEMATIC

Ref Des	HP Part No	Mfr Part No
U1,U3-U8,U11	1820-1633	74S240
U10	1816-1092	27LS00
U14	1820-1624	74S241
U17,U18	1820-0681	74S00
U44	1820-1449	74S32
U51	1820-0685	75S10
U57	1820-0683	74S04

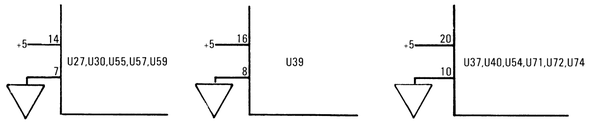
PARTS ON THIS SCHEMATIC

J1
R37
TP8-TP15
U1-U12,U14,U17,U18,U44,U51,U57
X1-X3

Figure 8-2. Service Sheet 1, Data and Address Buffers
8-15/(8-16 blank)



IC POWER SUPPLY PIN CONFIGURATION



ICS ON THIS SCHEMATIC

Ref Des	HP Part No	Mfr Part No
U27	1820-1112	74LS74
U30	1820-0907	7412
U37	1820-1633	745240
U39	1820-1195	74LS175
U40	1820-2024	74LS244
U54,U71,U72, U74,U75	1820-1997	74LS374
U55	1820-1367	74S08
U57	1820-0683	74S04
U59	1820-0686	74S11

PARTS ON THIS SCHEMATIC

C1-C8,C10,C13-C17,C19,C21,C22,C24-C40,C42, C44,C45,C47-C56,C57,C58
P1
R1,R17,R18,R38
U27,U30,U37,U39,U40,U54,U57,U59,U71,U72,U74,U75

Figure 8-3. Service Sheet 2 , Mainframe Interface Logic

P/O 6809 CONTROL BOARD (64214-66501) HOST ADDRESS BUFFER

BACKGROUND MEMORY ACCESS CONTROLLER

HOST DATA BUFFER

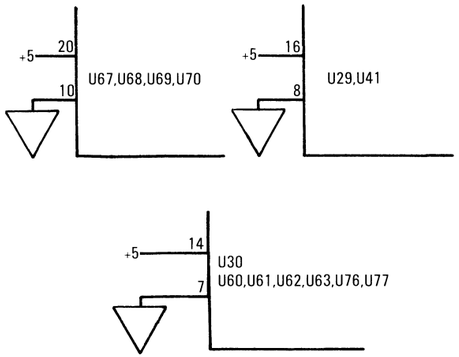
ID BUFFER

P/O ADDRESS DECODER

BACKGROUND MEMORY ACCESS CONTROLLER AND HOST BUFFERS
SLOW CLOCK DETECTOR

3

IC POWER SUPPLY PIN CONFIGURATION



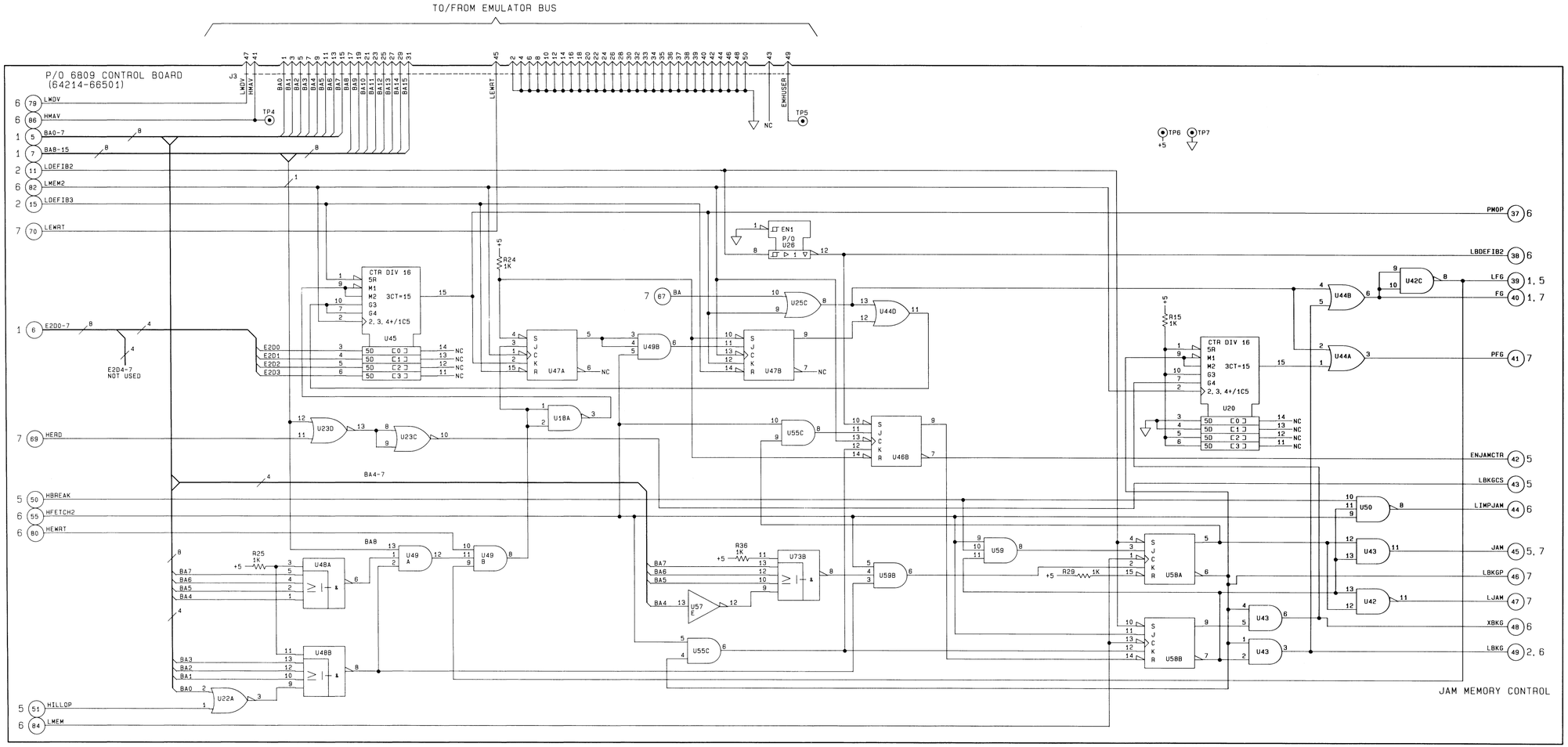
ICS ON THIS SCHEMATIC

Ref Des	HP Part No	Mfr Part No
U29	1820-1423	74LS123
U30	1820-0907	7412
U41	1820-1216	74LS138
U60	1820-0681	74S00
U61	1820-0686	74S11
U62	1820-1322	74S02
U63	1820-0693	74S74
U67,U68,U70	1820-2024	74LS244
U69	1820-1997	74LS374
U76	1820-1416	74LS14
U77	1820-1202	74LS10

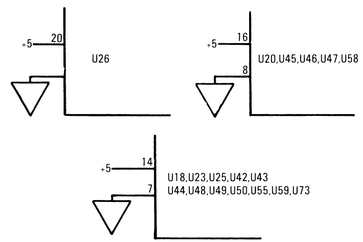
PARTS ON THIS SCHEMATIC

C18,C41,C46
CR7,CR8
L5
R16,R30,R32,R34,R35
TP16,TP18,TP19
U29,U30,U41,U60-U63,U67-U70,U76,U77

Figure 8-4. Service Sheet 3, Background Memory Controller



IC POWER SUPPLY PIN CONFIGURATION



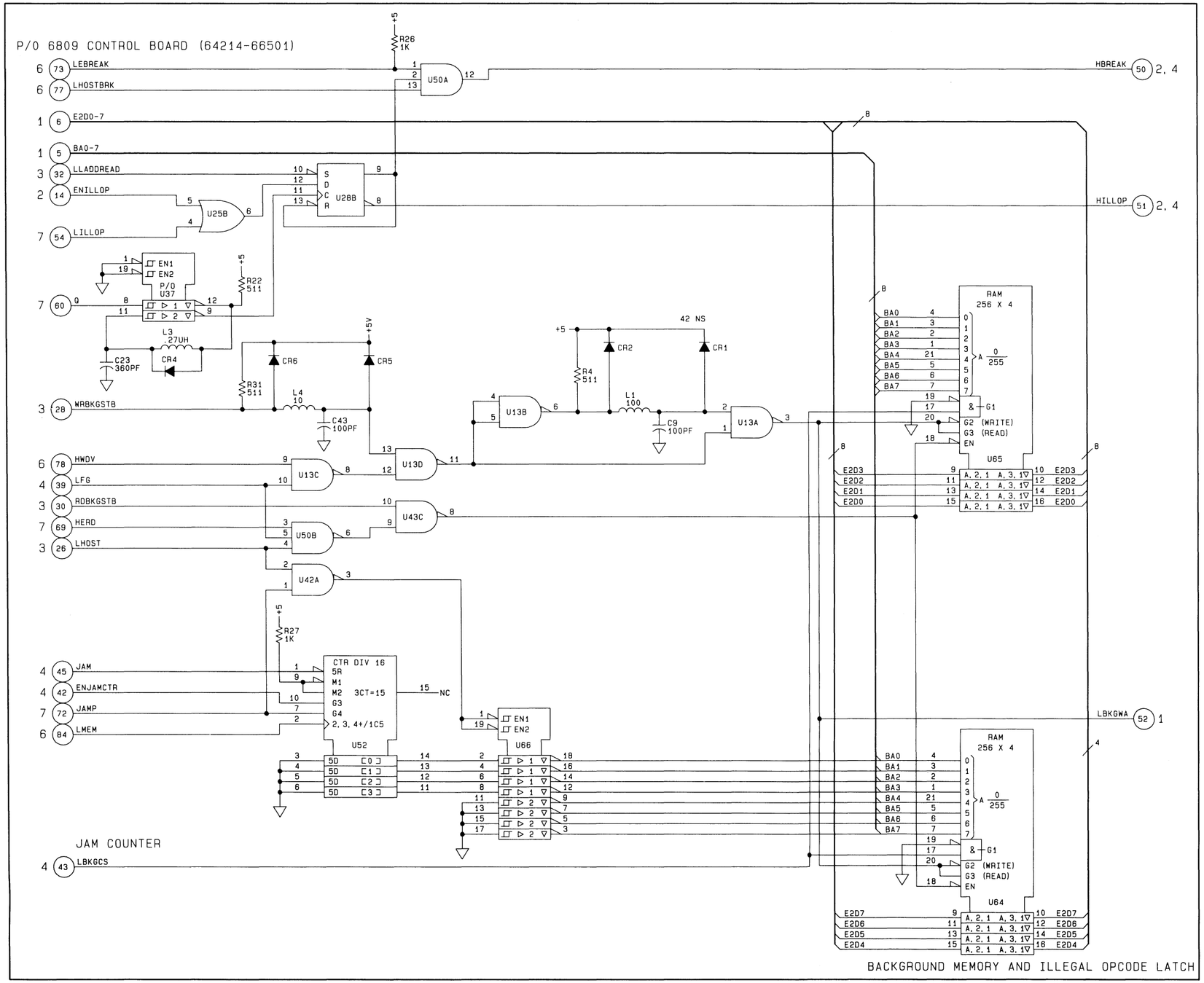
ICS ON THIS SCHEMATIC

Ref Des	HP Part No	Mfr Part No
U18,U42	1820-0681	74S00
U20,U45	1820-1430	74LS161
U23	1820-1322	74S02
U25,U44	1820-1449	74S32
U26	1820-1624	74S241
U43,U55	1820-1367	74S08
U46,U47,U58	1820-0629	74S112
U48,U73	1820-0655	7425
U49,U59	1820-0686	74S11
U50	1820-0685	74S10

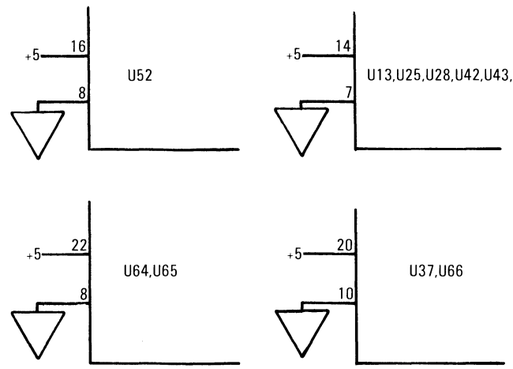
PARTS ON THIS SCHEMATIC

J3
R15,R24,R25,R29,R36
TP4-TP7
U18,U20,U22,U23,U25,U26,U42-U50,
U55,U57-U59,U73

Figure 8-5. Service Sheet 4, Jam and Foreground Memory Control
8-21/(8-22 blank)



IC POWER SUPPLY PIN CONFIGURATION



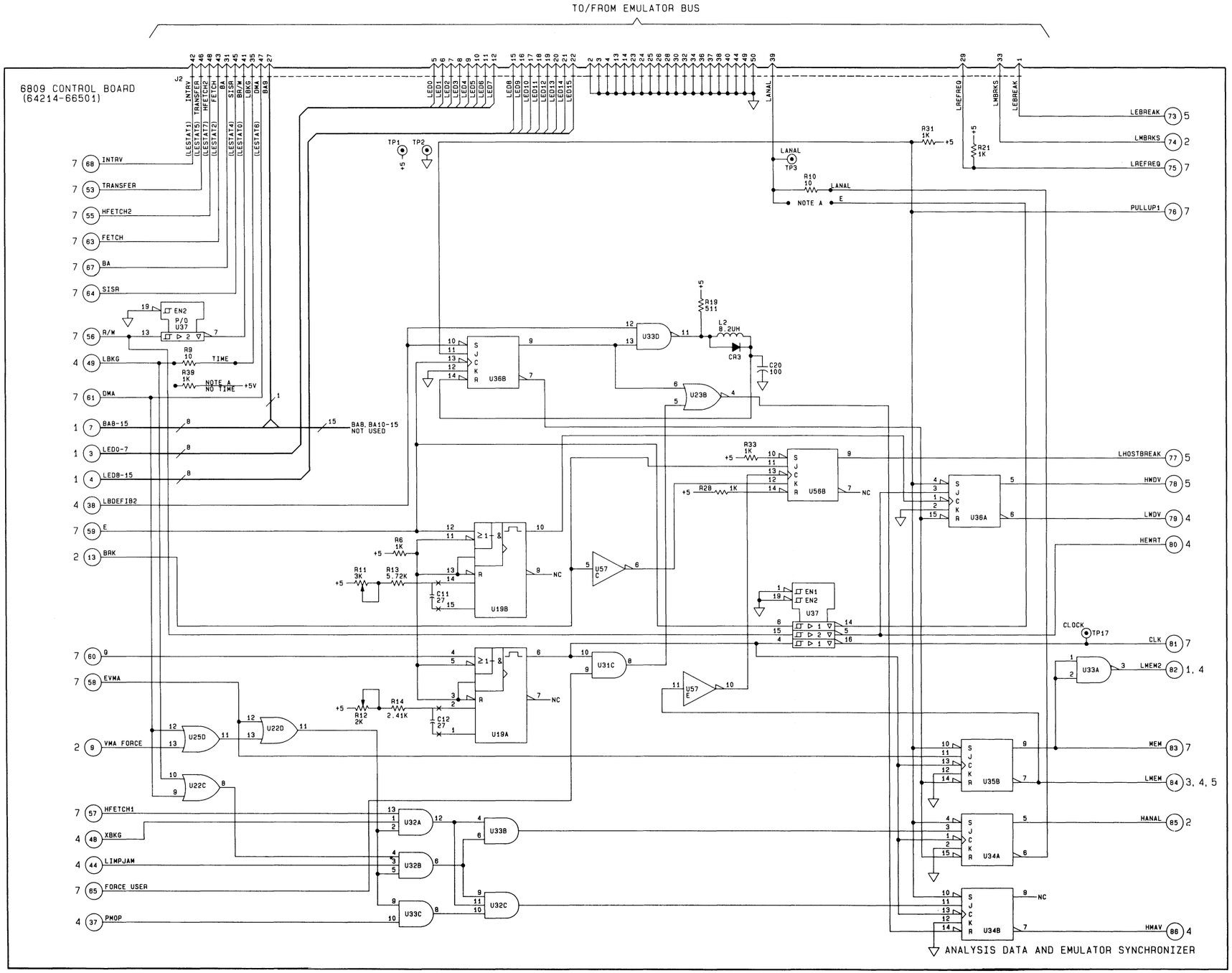
ICS ON THIS SCHEMATIC

Ref Des	HP Part No	Mfr Part No
U13,U42	1820-0681	74S00
U25	1820-1449	74S32
U28	1820-0693	74S74
U37	1820-1633	74S240
U43	1820-1367	74S08
U50	1820-0685	74S10
U52	1820-1432	74LS163
U64,U65	1816-1334	9S422
U66	1820-1917	74LS240

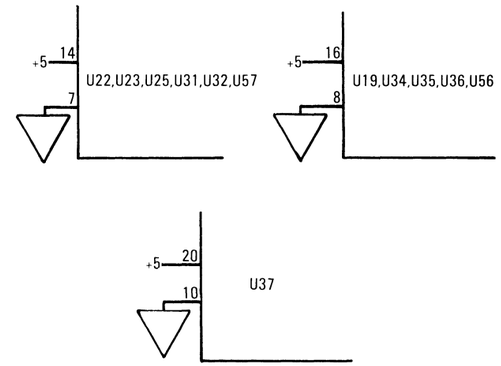
PARTS ON THIS SCHEMATIC

C9,C23,C43
CR1,CR2,CR4,CR5,CR6
L1,L3,L4
R4,R22,R26,R27,R31
U13,U25,U28,U37,U42,U43,U50,U52,U64-U66

Figure 8-6. Service Sheet 5, Background Memory



IC POWER SUPPLY PIN CONFIGURATION



ICS ON THIS SCHEMATIC

Ref Des	HP Part No	Mfr Part No
U19	1820-1782	26S02
U22,U25	1820-1449	74S32
U23	1820-1322	74S02
U31	1820-1367	74S08
U32	1820-0685	74S10
U33	1820-0681	74S00
U34-U36,U56	1820-0629	74S112
U37	1820-1633	74S240
U57	1820-0683	74S04

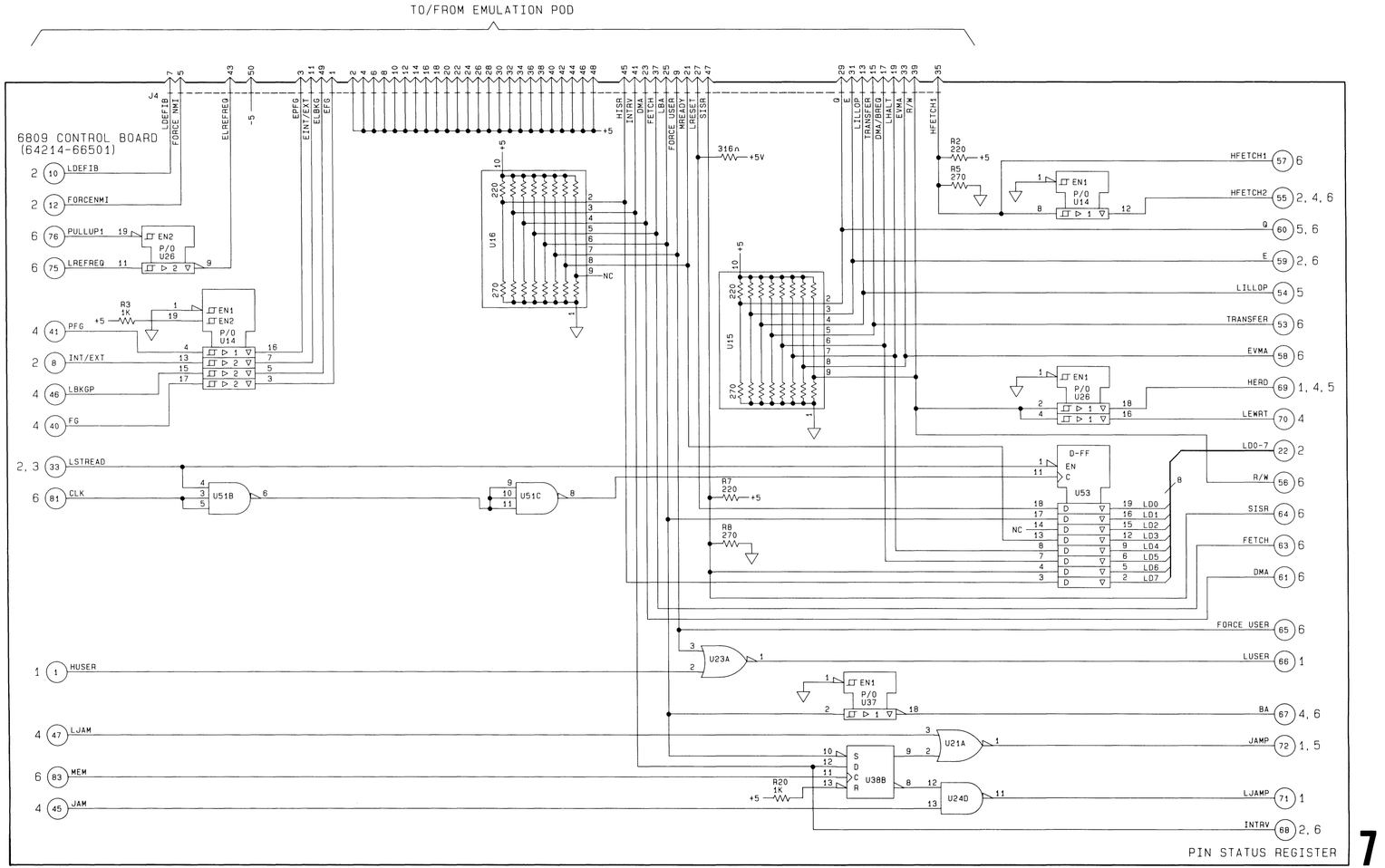
PARTS ON THIS SCHEMATIC

C11,C12,C20
CR3
L2
J2
R6,R9-R14,R19,R21,R23,R28,R33,R39
TP1,TP2,TP3,TP17
U19,U22,U23,U25,U31-U37,U56,U57

NOTE A

For normal operation the Model 64214A should be configured as illustrated on this schematic. The alternate configuration is for factory diagnostics only.

Figure 8-7. Service Sheet 6, Mainframe/Emulator Synchronizer



IC POWER SUPPLY PIN CONFIGURATION

ICS ON THIS SCHEMATIC

Ref Des	HP Part No	Mfr Part No
U14,U26	1820-1624	74S241
U21,U23	1820-1322	74S02
U24	1820-0681	74S00
U37	1820-1633	74S240
U38	1820-0693	74S74
U51	1820-0685	74S10
U53	1820-1997	74LS374

PARTS ON THIS SCHEMATIC

J4
R2,R3,R5,R7,R8,R20
U14-U16,U21,U23,U24,U26,U27,U38,U51,U53

Figure 8-8. Service Sheet 7, Analysis Data and Pin Status

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CS	Computer Systems Software Sales and Services
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Motorola Israel Ltd.
16 Kremenetski Street
P.O. Box 25016
TEL-AVIV 67899
Tel: 3-338973
Telex: 33569 Motil IL
Cable: BASTEL Tel-Aviv
CH,CM,CS,E,M,P

ITALY
Hewlett-Packard Italiana S.p.A
Traversa 99C
Via Giulio Petroni, 19
I-70124 **BARI**
Tel: (080) 41-07-44
M

Hewlett-Packard Italiana S.p.A.
Via Martin Luther King, 38/111
I-40132 **BOLOGNA**
Tel: (051) 402394
Telex: 511630
CH,E,MS

Hewlett-Packard Italiana S.p.A.
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I-95126 **CATANIA**
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Telex: 970291
C,P

Hewlett-Packard Italiana S.p.A.
Via G. Di Vittorio 9
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Hewlett-Packard Italiana S.p.A.
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Capodimonte, 62/A
I-80131 **NAPLES**
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Telex: 710698
A,CH,E

Hewlett-Packard Italiana S.p.A.
Viale G. Modugno 33
I-16156 **GENOVA PEGLI**
Tel: (010) 68-37-07
Telex: 215238
E,C

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Via Turazza 14
I-35100 **PADOVA**
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A,CH,E,MS

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Telex: 610514
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I-10149 **TORINO**
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Telex: 221079
CH,E

JAPAN
Yokogawa-Hewlett-Packard Ltd.
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000 **ATSUGI**, Kanagawa, 243
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CM,C*,E

Yokogawa-Hewlett-Packard Ltd.
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2-3, Kaigan-dori, 2 Chome Chuo-ku
KOBE, 650
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C,E

Yokogawa-Hewlett-Packard Ltd.
Kumagaya Asahi 82 Bldg
3-4 Tsukuba
KUMAGAYA, Saitama 360
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CH,CM,E

Yokogawa-Hewlett-Packard Ltd.
Asahi Shinbun Daiichi Seimei Bldg.
4-7, Hanabata-cho
KUMAMOTO,860
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CH,E

Yokogawa-Hewlett-Packard Ltd.
Shin-Kyoto Center Bldg.
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Karasuma-Nishiiru
Shiokoji-dori, Shimogyo-ku
KYOTO, 600
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Yokogawa-Hewlett-Packard Ltd.
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MITO, Ibaragi 310
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Sumitomo Seimei 14-9 Bldg.
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CH,CM,CS,E,MS

Yokogawa-Hewlett-Packard Ltd.
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Yodogawa-ku
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Telex: YHPOSA 523-3624
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Shinjuku-ku,**TOKYO** 160
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CH,E

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Telex: 232-2024 YHPTOK
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CH,E,M,P

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ADCOM Ltd., Inc., Kenya
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NAIROBI
Tel: 331955
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E,M

KOREA
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76-561 Yeoksam-Dong
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Telex: K27364 SAMSAN
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P.O. Box 830 Safat
KUWAIT
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Telex: 22481 Areeg kt
CH,E,M

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P.O. Box 270 Safat
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P

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LUXEMBOURG
Hewlett-Packard Belgium S.A./N.V.
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Woluwedal
B-1200 **BRUSSELS**
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Telex: 23-494 paloben bru
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Telex: MA 70904 PROTEL
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Philip Toledo Ltd.
Notabile Rd.
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P

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E

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P

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A,M

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Telex: 3289 BROKER MB MUSCAT
P

Suhail & Saud Bahwan
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Telex: 3274 BAHWAN MB

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Cable: FEMUS Rawalpindi
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Mushko & Company Ltd.
Oosman Chambers
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Telex: 2894 MUSKO PK
Cable: COOPERATOR Karachi
*A,E,M,P**

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Electrónico Balboa, S.A.
Calle Samuel Lewis, Ed. Alfa
Apartado 4929
PANAMA 5
Tel: 64-2700
Telex: 3483 ELECTRON PG
A,CM,E,M,P

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Arranged alphabetically by country

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***LIMA** 1*
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Telex: Pub. Booth 25306
CM,E,M,P

PHILIPPINES

The Online Advanced Systems Corporation
Rico House, Amorsolo Cor. Herrera Street
Legaspi Village, Makati
P.O. Box 1510
Metro MANILA
Tel: 85-35-81, 85-34-91, 85-32-21
Telex: 3274 ONLINE
A,CH,CS,E,M

Electronic Specialists and Proponents Inc.
690-B Epifanio de los Santos Avenue
*Cubao, **QUEZON CITY***
P.O. Box 2649 Manila
Tel: 98-96-81, 98-96-82, 98-96-83
Telex: 40018, 42000 ITT GLOBE MACKAY BOOTH
P

PORTUGAL

Mundinter
Intercambio Mundial de Comércio S.A.R.L.
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Avenida Antonio Augusto de Aguiar 138
P-LISBON
Tel: (19) 53-21-31, 53-21-37
Telex: 16691 munter p
M

Soquimica
Av. da Liberdade, 220-2
*1298 **LISBOA** Codex*
Tel: 56 21 81/2/3
Telex: 13316 SABASA
P

Telectra-Empresa Técnica de Equipmentos Eléctricos S.A.R.L.
Rua Rodrigo da Fonseca 103
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QATAR

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DOHA
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Telex: 4806 CHPARB
P

Eastern Technical Services
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DOHA
Tel: 329 993
Telex: 4156 EASTEC DH

Nasser Trading & Contracting
P.O.Box 1563
DOHA
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Telex: 4439 NASSER DH
M

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Modern Electronic Establishment
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Thuobah
AL-KHOBAR
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Telex: 671 106 HPMEEK SJ
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CH,CS,E,M,P

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Telex: 4027 12 FARNAS SJ
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Telex: 202049 MEERYD SJ
CH,CS,E,M,P

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CM

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A,CH,CM,E,MS,P

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CH,CM

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A,CH,E,MS

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A,CS,MS,P

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CH-1217 **MEYRIN** 1
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E

Middle East Electronics
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A

THAILAND

Unimesa
30 Patpong Ave., Suriwong
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P

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Tunisie Electronique
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TUNIS
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E,P

Corema
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TUNIS
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Telex: 12319 CABAM TN
M

TURKEY

Teknim Company Ltd.
Iran Caddesi No. 7
*Kavaklidere, **ANKARA***
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E

E.M.A.
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M

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CH,E,MS**

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CH,CS

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A*,CH,CS,E,MS

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9606 Aero Drive
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CH,CM,CS,E,MP

Hewlett-Packard Co.
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