HEWLETT-PACKARD

COMPUTER MAINTENANCE COURSE

VOLUME II

STUDENTS MANUAL

HP 2116B/HP 2115A
CENTRAL PROCESSOR UNITS

(HP STOCK NO. 5950-8704)

-NOTICE-

The information contained in this manual is for training purposes only. Consult the Hewlett-Packard documentation supplied with the computer for current information concerning the specific computer system furnished.

11000 Wolfe Road, Cupertino, California 95014 Area Code 408 257-7000 TWX 910-338-0221

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SECTION INDEX

logic control and timing

Logic Control and Timing Chart

A. INTRODUCTION

1. Objectives

a. Logic Equations

(1) In Lesson II, programming techniques were applied to implement selected instructions. In this lesson, logic equations will be introduced to show how the computer implements the selected instructions.

(2) A complete list of logic equations and definitions are contailed in the Student's Workbook.

b. Timing Chart

(1) A timing chart is given in Volume 1 (Basic Operation and Specifications). The timing chart provides answers to three basic questions:

(a) What instruction are we implementing?
(b) What phase are we in?
(c) What time is it?

(2) The timing chart translates instructions into machine phases and timing periods. From this information we may then determine the control functions required to implement a given instruction. The control functions are given by our logic equations. Thus, the problem becomes one of interpreting the timing chart and making the transition to the logic equations.

c. Instructions

(1) Instructions are basically microprograms. That is, an explicity defined sequence of operations must be performed to implement each instruction. The timing chart tells us, at any given period in time, what operation is being performed.

2. Logic Symbology (Figure 1-1)

a. Logic symbols and diagrams are a means of communication – a language. A logic symbol or diagram is a simplified version of a logic element or complex circuit. At the present time there is no single universal system for representing logic elements or circuits. The particular logic symbology used by HP is an adaptation of the Military Standard (MIL SPEC) designed to meet certain objectives commensurate with our customer service policy:

(1) Versatility
(2) Clarity
(3) Coverage
(4) Simplicity

b. HP Logic Symbology is given in HP Application Note 88. Logic symbols for logic circuits fall into four major classifications.

Gates
Amplifiers
Switches
Delay Elements

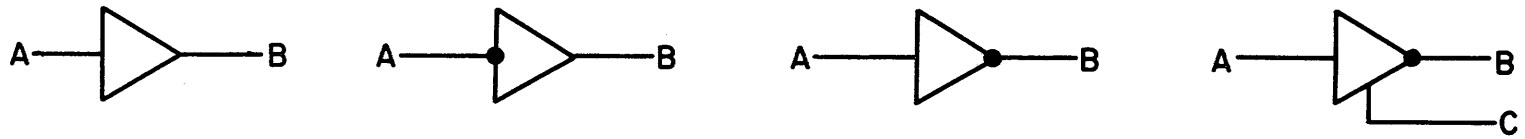
(1) A Gate is a logic element which produces a "true" or "false" output depending on the states of the inputs. All inputs are connected to the flat side of the sphere: all outputs are connected to the curved side.

(2) An Amplifier is used in logic circuitry to drive gates or restore voltage levels. The output depends on the state of the

FOUR MAJOR CLASSES OF HP LOGIC SYMBOLS

1. GATES–

2. AMPLIFIERS–



3. SWITCHING ELEMENTS–

4. DELAY ELEMENTS–

FIG. 1–1

LOGIC LEVELS:

1 = +4.5V

0 = 0.0V

input. The input is always connected to the flat side of a triangle: the output to the opposite vertex.

(3) Switching elements comprise the various forms of multivibrators (flip-flops, one-shot, monostable etc.)

(4) Delay elements are used to provide a time delay between application of a signal and the resulting output.

c. Logic Levels

(1) Positive and negative logic levels are used to distinguish the various input and output conditions. In the HP 2116B/HP 2115A Computer, all logic circuits use positive logic. That is, a positive level indicates a true (or "1") signal. A negative level indicates a false (or "0") signal.

3. Eight Basic Logic Devices

a. Types and Purpose

(1) The simplest and fastest circuits to develop are those having only two possible states "on" or "off". These circuits are capable of making "yes" or "no" decisions corresponding to their instantaneous states of "on" or "off", respectively. This leads directly to the binary number system wherein a "one" represents an "on" (or true) state and a "zero" represents an "off" (or false state). To obtain sufficient and accurate data in the minimum amount of time, it is required that the circuits involved perform millions of logical events per second. The circuits that perform these logic functions are called logic circuits. These logic circuits perform two basic functions:

(a) Logical and mathematical operations

(b) Store information

(2) The basic logic devices used are the:

(a) NOT Gate
(b) IOR Gate
(c) NOR Gate
(d) AND Gate
(e) NAND Gate
(f) INHIBIT Gate
(g) Flip-Flop
(h) Memory Core

These basic logic devices are combined in many ways to form complex logic circuits.

b. The NOT Gate (Figure 1-2)

(1) The NOT circuit provides pulse inversion. The $\overline{\text{bar}}$ over the indicated input indicates that the given variable A is "not" true. This circuit provides a "true" output only when the input is "false". That is, the output is always the inverse (or the one's complement) of the input.

c. The IOR Gate (Figure 1-3)

(1) The IOR gate is used for:

(a) Data Transfer
(b) Control
(c) One's Testing

The IOR circuit provides a true output when either, or both, inputs A or B are true.

d. The AND Gate (Figure 1-4)

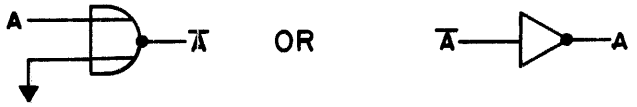
(1) The AND gate is used for:

(a) Data Transfer
(b) Control

THE "NOT" GATE OR INVERTER

PROVIDES PULSE INVERSION AND IS USED TO GENERATE LOGIC SIGNALS OR TO "COMPLEMENT" A BINARY INPUT

CMP
LOGIC



IF "A" GOES FALSE (GROUND) "$\overline{A}$" GOES TRUE (POSITIVE) INDICATING "NOT A."

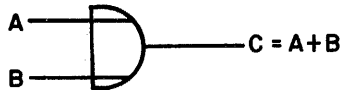
IF "$\overline{A}$" GOES FALSE (GROUND) "A" GOES TRUE (POSITIVE) INDICATING "A."

FIG. 1-2

THE "IOR" GATE (INCLUSIVE "OR")

"IOR" PROVIDES LOGICAL ADDITION

IOR
LOGIC



THE OUTPUT "C" IS TRUE (POSITIVE) WHEN "A" OR "B" OR "BOTH" ARE TRUE (POSITIVE).

THE ARITHMETIC ADDITION SIGN (+) ALWAYS INDICATES "OR" IN LOGIC EQUATIONS AND CIRCUITS. THE TERM C=A+B IS A LOGIC EQUATION MEANING EITHER "A" OR "B", OR "BOTH," MUST BE TRUE FOR "C" TO BE TRUE.

TRUTH TABLE

A	B	OUTPUT C=A+B
0	0	0
1	0	1
0	1	1
1	1	1

FIG. 1-3

THE "AND" GATE

"AND" PROVIDES LOGICAL MULTIPLICATION

THE OUTPUT "C" IS TRUE (POSITIVE) ONLY WHEN "A" AND "B" ARE BOTH TRUE (POSITIVE)

THE ARITHMETIC MULTIPLICATION SIGN (•) ALWAYS INDICATES "AND" IN LOGIC EQUATIONS AND CIRCUITS. THE TERM C=A·B IS A LOGIC EQUATION MEANING BOTH "A" AND "B" MUST BE TRUE FOR "C" TO BE TRUE.

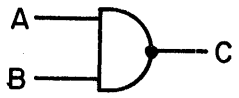
TRUTH TABLE

A	B	OUTPUT C=A·B
0	0	0
1	0	0
0	1	0
1	1	1

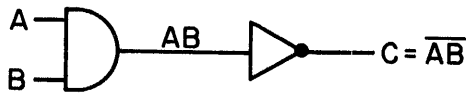
FIG. 1-4

The "NAND" Gate

PROVIDES THE LOGICAL OPERATION "NOT-AND"



THE OUTPUT "C" IS FALSE (NOT) ONLY WHEN BOTH "A" AND "B" ARE TRUE. THUS THE "NAND" GATE CAN BE CONSIDERED AS AN "AND" GATE FOLLOWED BY AN INVERTER



TRUTH TABLE

A	B	C
0	0	1
1	0	1
0	1	1
1	1	0

FIG. 1-5

(c) Decoding

(d) Pulse Shaping

The circuit provides a "true" output only when A and B are both true.

e. The NAND Gate (Figure 1-5)

(1) The NAND gate produces the operation $\overline{A\,B}$. Remembering the NOT and AND gates, it will be clear that the NAND gate is simply a "NOT-AND" circuit. The NAND gate is used for:

(a) Data Transfer

(b) Control

(c) Zero Testing

f. The NOR Gate (Figure 1-6)

(1) The NOR gate produces the operation $\overline{A+B}$. Remembering the NOT and IOR gates, it will be clear that the NOR gate is simply a "NOT-IOR" circuit. This circuit is logically complete – any logical expression can be achieved by a combination of NOR gates. The NOR gate is used for:

(a) Inversion

(b) Control

g. The INHIBIT Gate (Figure 1-7)

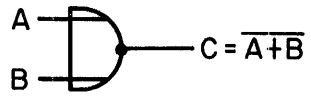
(1) The Inhibit Gate provides the operation $\overline{A}.\,B$. It is normally used to test the state of a given logic line, and is used in the Fairchild CT micrologic.

h. Flip-Flops

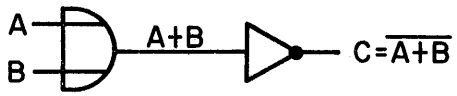
(1) A flip-flop is a bi-stable switching element; that is, it has two stable states, normally referred to as "set" and "reset." There are three basic Flip-Flops used in the HP 2116B/ HP 2115A Computer:

The "NOR" Gate

THE "NOR" GATE PROVIDES THE LOGICAL OPERATION "NOT-OR"



THE OUTPUT "C" IS FALSE (NOT) ONLY WHEN EITHER "A" OR "B" ARE TRUE. THUS THE "NOR" GATE CAN BE CONSIDERED AS AN OR GATE FOLLOWED BY AN INVERTER.



TRUTH TABLE

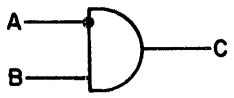
A	B	C
0	0	1
1	0	0
0	1	0
1	1	0

FIG. 1-6

THE "INHIBIT" GATE

"INHIBIT" PROVIDES THE OPERATION $\overline{A}B$

AND IS USED TO SAMPLE (OR DETECT) THE STATE OF A GIVEN LOGIC LINE.



WHEN LINE "A" IS TO BE SAMPLED, SIGNAL "B" IS MADE TRUE (POSITIVE).

IF LINE "A IS TRUE (POSITIVE) THE OUTPUT IS INHIBITED AND "C" IS FALSE (GROUND).

IF LINE "A" IS FALSE (GROUND) THE "B" LINE ALLOWS THE OUTPUT "C" TO GO TRUE (POSITIVE).

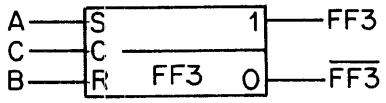
FIG. 1-7

THE R-S FLIP FLOP WITH CLOCK

SHIFT

LOGIC

IS A TOGGLE SWITCH USED AS A TIMING CONTROL FOR GATES, FREQUENCY DIVIDERS, AND SHIFT REGISTERS.



"A" AND "C" ARE REQUIRED TO SET (FF3 TRUE)
"B" AND "C" ARE REQUIRED TO RESET ($\overline{FF3}$ TRUE)

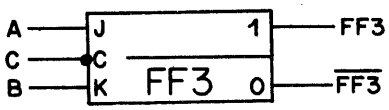
FIG. 1-8

The J-K Flip Flop

IS A LATCHING SWITCH USED FOR CONTROL, STORAGE, COUNTING AND COMPLEMENTING.

CMP

LOGIC



SIMULTANEOUS INPUTS "A" AND "B" REVERSE THE EXISTING STATE FF3 $\longrightarrow \overline{FF3}$

TRUTH TABLE

INPUTS A	INPUTS B	INITIAL STATE FF3	INITIAL STATE $\overline{FF3}$	FINAL STATE FF3	FINAL STATE $\overline{FF3}$
1	0	ANY		1	0
0	1			0	1
1	1	0	1	1	0
1	1	1	0	0	1
0	0	ANY		NO CHANGE	

FIG. 1-9

(a) RS with and without clock (Figure 1-8)

(b) JK (Figure 1-9)

(c) Latching (Figure 1-10)

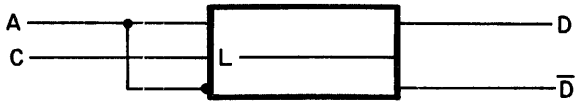
(2) The RS flip-flop has a minimum of two inputs, set (A) and reset (B). The flip-flop may also be directly set or reset using a direct set or direct clear input. The set output is usually denoted with the flip-flop's logic symbol such as FF3. The reset output is usually denoted as "not FF3" or simply $\overline{FF3}$. When FF3 is true, $\overline{FF3}$ is false and the flip-flop is "set". With FF3 false, and $\overline{FF3}$ true; the flip-flop is "reset".

The R-S Flip-Flop with Clock is the same as the basic R-S flip-flop except that a clock (C) input "and" a set or reset input are required to set or reset the flip-flop respectively. The clock (C) input and either the A or B input must be present simultaneously to set or reset the flip-flop.

(3) The J-K Flip-Flop is similar to the R-S Flip-Flop except that the condition when both inputs A and B are true is discretely defined. When A and B are both "true", the state of the flip-flop is reversed. It can therefore be "latched" in either state by the application of simultaneous inputs to J, K, and C.

(4) The latching flip-flop has a single input and a clock input. The symbol is identified by the letter L inside the symbol as shown. Note that the set input is responsive to true signals at A, and the reset input is responsive to false signals at A. The flip-flop will follow the input at A as long as the clock input is true. The flip-flop will "latch" into the state existing at A when the clock pulse transists from true to false.

LATCHING FLIP FLOP



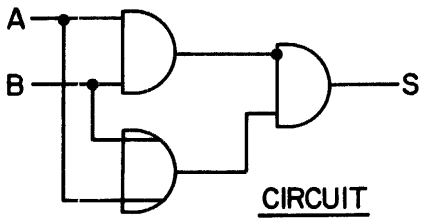
THIS FLIP FLOP WILL FOLLOW INPUT "A" AS LONG AS THE CLOCK INPUT (C) IS TRUE. THE FLIP-FLOP WILL LATCH IN-TO THE STATE EXISTING AT "A" WHEN THE CLOCK PULSE AT C TRANSITS FROM TRUE TO FALSE.

FIG 1-10

THE "XOR" GATE (EXCLUSIVE "OR")

PROVIDES THE OPERATIONS OF BINARY ADDITION AND SIGN COMPARISON.

XOR
LOGIC



CIRCUIT

THE "XOR" CIRCUIT IS CALLED A "QUARTER ADDER" BECAUSE IT CANNOT OPERATE ON A PREVIOUS CARRY NOR GENERATE A CARRY OF ITS OWN.

TRUTH TABLE

A	B	SUM
0	0	0
1	0	1
0	1	1
1	1	0

FIG.1-11

4. Digital Arithmetic Devices

   a. The XOR Gate (Figure 1-11)

      (1) The XOR (exclusive OR) circuit performs the basic arithmetic operation of binary addition — but its use as a digital adder is prohibited because it does not operate on a previous carry or generate a carry of its own. For these reasons it is called a "quarter-adder".

   b. The Half-Adder (Figure 1-12)

      (1) The exclusive OR circuit may be used to construct a "half-adder" which generates a carry but does not operate on a previous carry.

   c. The Full Adder (Figure 1-13)

      (1) Two half adders and additional logic comprise a "full adder." The parallel adder is used in the HP 2116B/HP 2115A arithmetic circuits.

5. Fairchild CT Micrologic (Figure 1-14)

   a. Definition

      (1) The Fairchild CT and CT^2 micro-packs are used exclusively in the HP 2116B/HP 2115A Computers. The term CT simply means "complementary transistor" logic. Thus, CT^2 logic uses dual complementary transistors and is therefore slower than CT logic. The HP 2115A uses CT^2 logic.

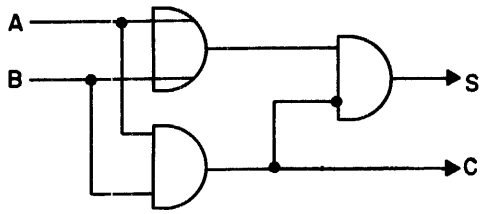
   b. Types

      (1) There are several types of micro-packs used in the HP 2116B/HP 2115A Computer. Each pack is identified by a unique 8-digit identifier. These identifiers may be found on a supplemental sheet in the Student's Workbook which cross-references the 8-digit identifier to the schematic symbol. The 8-digit identifier is also the HP Stock Number for each pack.

The Half Adder

THE HALF ADDER GENERATES A CARRY- BUT DOES NOT OPERATE ON A PREVIOUS CARRY.

HA
LOGIC



TRUTH TABLE

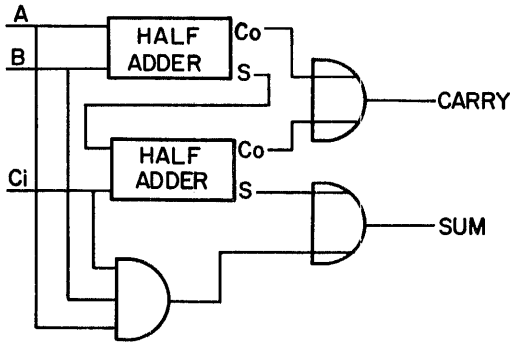
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

FIG. 1-12

THE FULL (PARALLEL) ADDER

GENERATES A CARRY AND OPERATES ON A PREVIOUS CARRY—THE "AND" GATE IS REQUIRED IN THE SPECIAL CASE WHEN ALL INPUTS ARE 1.

ADD
LOGIC

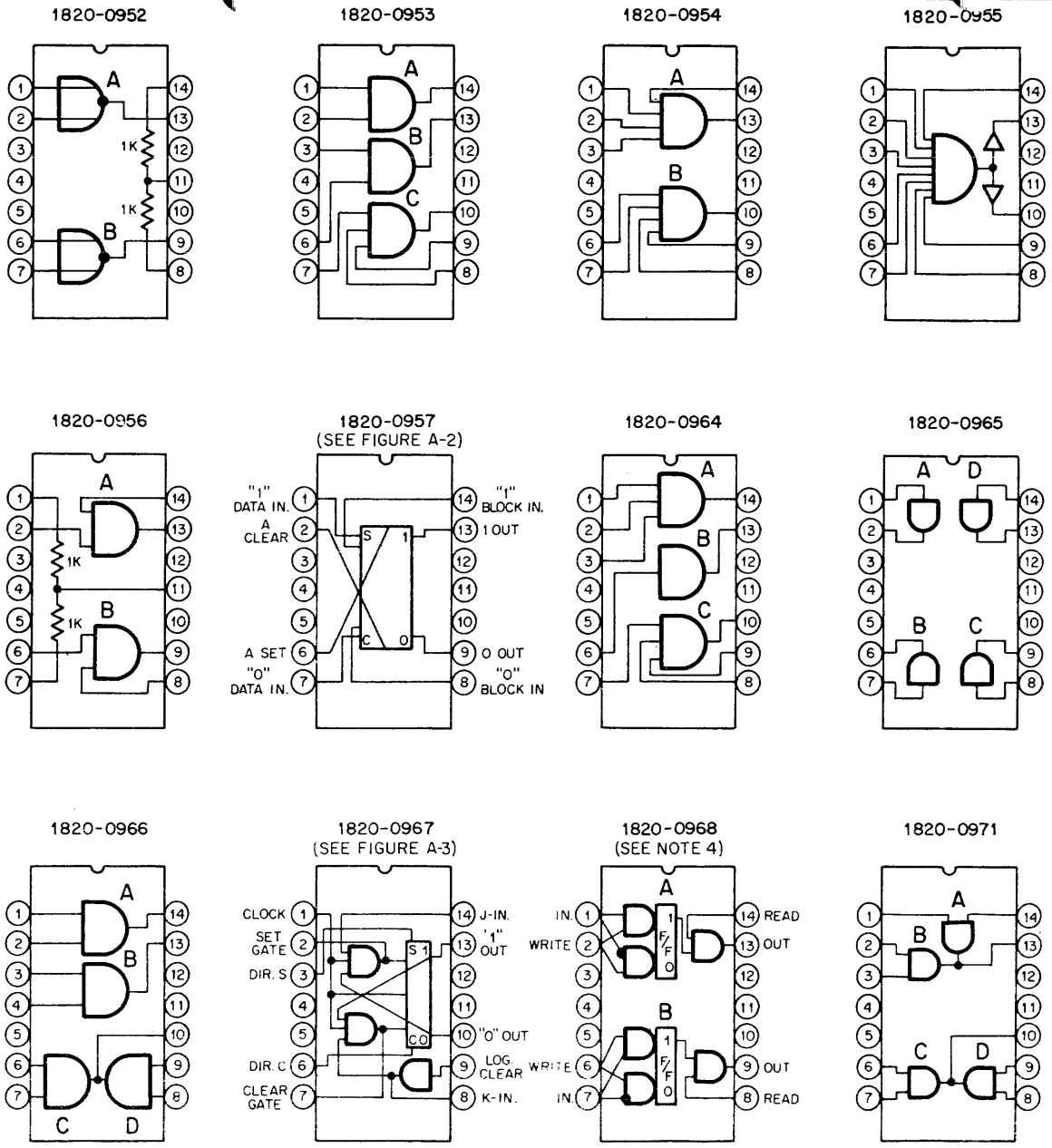


TRUTH TABLE

A	B	CI	SUM	CARRY
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	1	1
1	1	1	1	1

FIG. 1-13

CTμL
Pin Diagrams
(top view)



NOTES:

1. PIN 5 ON ALL MICROCIRCUIT PACKAGES IS GROUND.
2. PIN 11 ON ALL MICROCIRCUIT PACKAGES IS −2V ± 5%.
3. PIN 12 ON ALL MICROCIRCUIT PACKAGES IS +4.5V ± 5%.
4. PINS 8 AND 14 OF 1820-0968 ARE CONNECTED TO +4.5V. UNLESS OTHERWISE INDICATED ON A LOGIC DIAGRAM USING THE MICROCIRCUIT PACKAGE

FIG. 1-14

6. Review

   a. What are the objectives of this lesson?

   b. What is logic symbology?

   c. What two basic functions are logic circuits used for?

   d. What are the eight basic logic devices?

   e. What type micrologic is used in the HP2116B/HP 2115A Computer?

B. LOGIC EQUATIONS AND TIMING CHART

1. Boolean Algebra

a. Boolean Algebra - A Definition (Figure 1-15)

(1) A simple interpretation of Boolean Algebra is that given by a logical proposition. Variables such as A, B, C in this algebra correspond to a logical proposition. A unique characteristic of this algebra is that these variables may assume only one of two possible states, $\emptyset$ or 1. This fact makes the binary number system and this algebra as compatible as our ordinary algebra and the decimal number system.

(2) The sum of two variables (A+B) represents the proposition A "or" B. The product of two variables AB represents the proposition A "and" B.

(3) The negative, or complement, of a variable is indicated with a horizontal bar ($\overline{A}$ or $\overline{B}$) and read as a "not A" or "not B". The constants $\emptyset$ and 1 represents "no" and "yes", or "false" and "true" respectively.

b. Boolean Identities (Figures 1-16 and 1-17)

(1) There are eight basic identities common to ordinary algebra and the Boolean algebra. There are 10 basic identities unique to the Boolean algebra. Equations 6 and 7 of the 10 unique equations are sometimes referred to as D' Morgans Theorems. These identities are used to simplify complex logic circuits using "truth table", and also show the relationship between NOR and NAND gates.

c. The Truth Table

(1) Truth tables are used to prove Boolean expressions and are an aid to reducing complex circuits. The expression A(A+B)=A may be proven by constructing a truth table which

Boolean Algebra is

A SET OF LOGICAL PROPOSITIONS SIMILAR TO ORDINARY ALGEBRA WHICH IS A SET OF MATHEMATICAL PROPOSITIONS.

MATHEMATICAL SYMBOLOGY	BOOLEAN SYMBOLOGY
1 = ABSOLUTE NUMBER	1 = YES (TRUE)
$\underline{\emptyset}$ = ZERO	$\underline{\emptyset}$ = NO (FALSE)
$\overline{A}$ = LENGTH	$\overline{A}$ = "NOT A"
$\longrightarrow$ = APPROACHES LIMIT	$\longrightarrow$ = REPLACES
$\bullet$ = MULTIPLY	$\bullet$ = "AND"
$+$ = ADD	$+$ = "OR"
( ) = INNER PRODUCT	( ) = INNER "AND"
[ ] = AGGREGATE PRODUCT	[ ] = AGGREGATE "AND"
A+B = ADD A AND B	A+B = A "OR" B
AB = MULTIPLY A BY B	AB = A "AND" B

FIG. 1-15

Eight Basic Identities

THESE HOLD FOR BOTH ORDINARY AND BOOLEAN ALGEBRA.

1. $\emptyset + A = A$
2. $\emptyset \bullet A = \emptyset$
3. $1 \bullet A = A$
4. $A+B=B+A$
5. $AB=BA$
6. $A+(B+C)=(A+B)+C$
7. $A(BC)=AB(C)$
8. $A(B+C)=AB+AC$

ALL THESE EXPRESSIONS MAY BE CONSTRUCTED USING BASIC "AND-OR" GATES.

FIG. 1-16

TEN IDENTITIES UNIQUE TO BOOLEAN ALGEBRA

WHICH MAKE SIMPLIFICATION OF COMPLEX CIRCUITRY ECONOMICALLY FEASIBLE.

1. $A + A = A$
2. $A \cdot A = A$
3. $A + 1 = 1$
4. $A \cdot \overline{A} = \emptyset$
5. $A + \overline{A} = 1$
6. $\overline{A+B} = \overline{A} \cdot \overline{B}$
7. $\overline{AB} = \overline{A} + \overline{B}$
8. $A + AB = A$
9. $A(A+B) = A$
10. $A + BC = (A+B)(A+C)$

ALL THESE EXPRESSIONS MAY BE CONSTRUCTED USING BASIC "NOT," "AND," "OR," "NOR," AND "NAND" GATES.

FIG. 1–17

lists all possible combinations of variables and the two expressions A and A(A+B). If the two resulting expressions are equal, then the identity is proven. The following example will show the procedure for reducing a logic circuit.

(a) Write the Boolean expression for this circuit:

$$P = A(BC + AC)$$

(b) Reduce the expression using Boolean identities:

$$\begin{aligned} A\,(BC + AC) &= A.\,A(BC + C) \text{ Factoring A} \\ &= A\,(BC + C) \text{ Identity 2} \\ &= AC\,(B + 1) \text{ Factoring C} \\ &= AC\,(1) \text{ Identity 3} \\ &= AC \end{aligned}$$

(c) Construct a truth table:

A	B	C	A(BC + AC)	AC	P
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	1	1	1
1	1	0	0	0	0
1	1	1	1	1	1

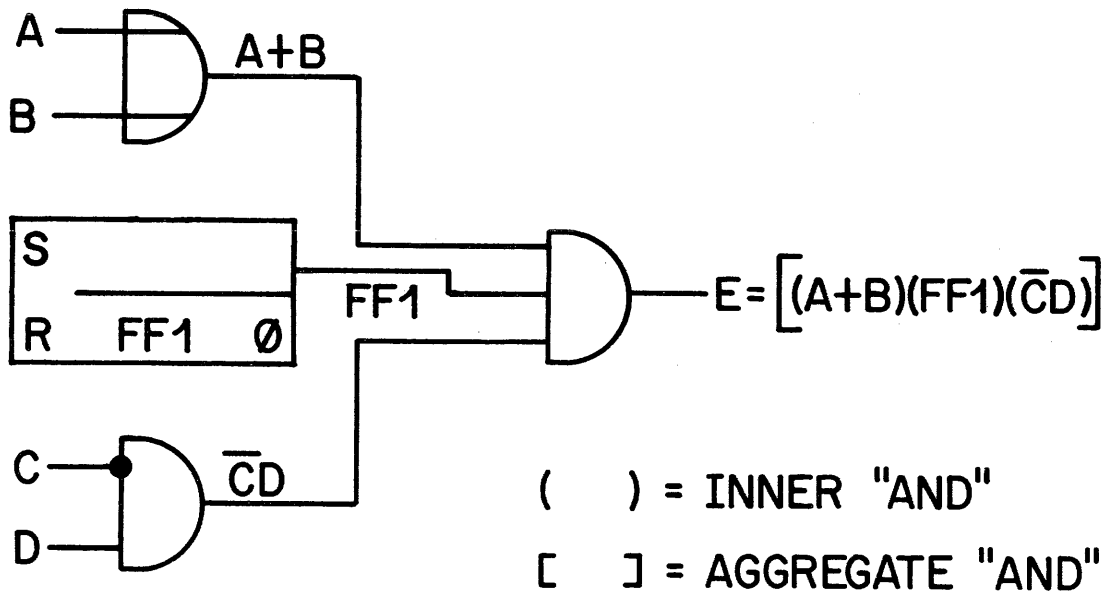
(d) Compare the resulting expressions AC and A (BC + AC). If equal, construct the reduced circuit AC.

2. Logic Equations (Figure 1-18)

a. Logic equations are used to conveniently describe logical circuits without resorting to logic diagrams. A logic equation is a series of Boolean expressions which describe certain conditions necessary

THE LOGIC EQUATION

COMPLETELY DEFINES A LOGIC CIRCUIT



IF "E" IS NOT TRUE, THE CONTROL FUNCTIONS A, B, FF1, $\overline{C}$ AND D MAY BE CHECKED TO ISOLATE A FAULTY COMPONENT.

FIG. 1-18

to generate a logic signal. Logic equations are used in the HP 2116B/ HP 2115A maintenance procedures as a troubleshooting tool.

b. The purpose of using logic equations is to facilitate troubleshooting. Once it is determined (from the timing chart) what instruction is being performed, what phase has control, and what time it is; then the logic equations may be used to find the control functions required to perform the instruction. These logic signals may then be measured.

3. Review

a. What is Boolean Algebra?

b. How many Boolean identities are common to ordinary algebra?

c. What are truth tables used for?

d. What is the primary application of Boolean Algebra?

e. What are logic equations used for?

f. What logic signals are required to "read the M register onto the S bus"?

C. TIMING CHART AND LOGIC CONTROL

1. Microprograms

a. Instructions

(1) Each instruction performed can be best illustrated by considering it as a "microprogram". For instance, to implement a flow-chart symbol such as "take the two's complement" requires two instructions: CMA and INA. Each instruction in turn requires a "micro program" to be implemented.

(a) The CMA micro program:

RARB
CMF
STBA

(b) The INA micro program:

RARB
SBØ
ADF
STBA

b. Phases

(1) The computer may be in one, and only one, phase at any given time.

(2) Memory reference instructions are the only instructions requiring more than one phase to execute. Indirect and Execute phases are associated with Memory Reference instructions only. In the case of all these instructions (except JMP), the action during the Fetch and Indirect phases is similar, so these phases are shown on the Timing Chart only once.

(3) The exception is the JMP instruction which does not use an Execute phase; execution can occur in either the Fetch (Direct JMP) or Indirect (Indirect JMP) phases.

(4) All Register Reference instructions are fully executed in only one phase (Fetch). Actual execution is accomplished during time periods T3 and T5. Actions during other time periods are similar to those required for Memory Reference instructions.

(5) Like the Register Reference instructions, Input/Output instructions are fully executed in only one phase (Fetch).

(6) The Interrupt Phase is a unique machine phase associated with the transfer of data. It is not used in the execution of Input/Output instructions as may be implied on the Timing Chart.

(a) Two operations are accomplished during the Interrupt Phase: The P Register is decremented because it will be incremented upon execution of the interrupt instruction. The "interrupt address" is transferred into the M Register and Phase 1 is set. Thus, the instruction contained in the "interrupt location" is executed.

c. Time Periods

(1) The basic machine cycle is 1.6 μs long (2.0 μs for HP 2115A). A machine cycle is further divided into 8 time periods (TØ-T7). Thus, each time period is 200 ns long (250 ns for HP 2115A).

(2) Memory is accessed (READ) only during the interval (TØ-T2) as shown on the Timing Chart. Memory writing (WRITE) occurs only during the interval (T3-T5).

(3) Each timing period has a TS pulse 50ns long which is delayed 50ns from the leading edge of the time period pulse (65 ns long

2. Implementation of Instructions

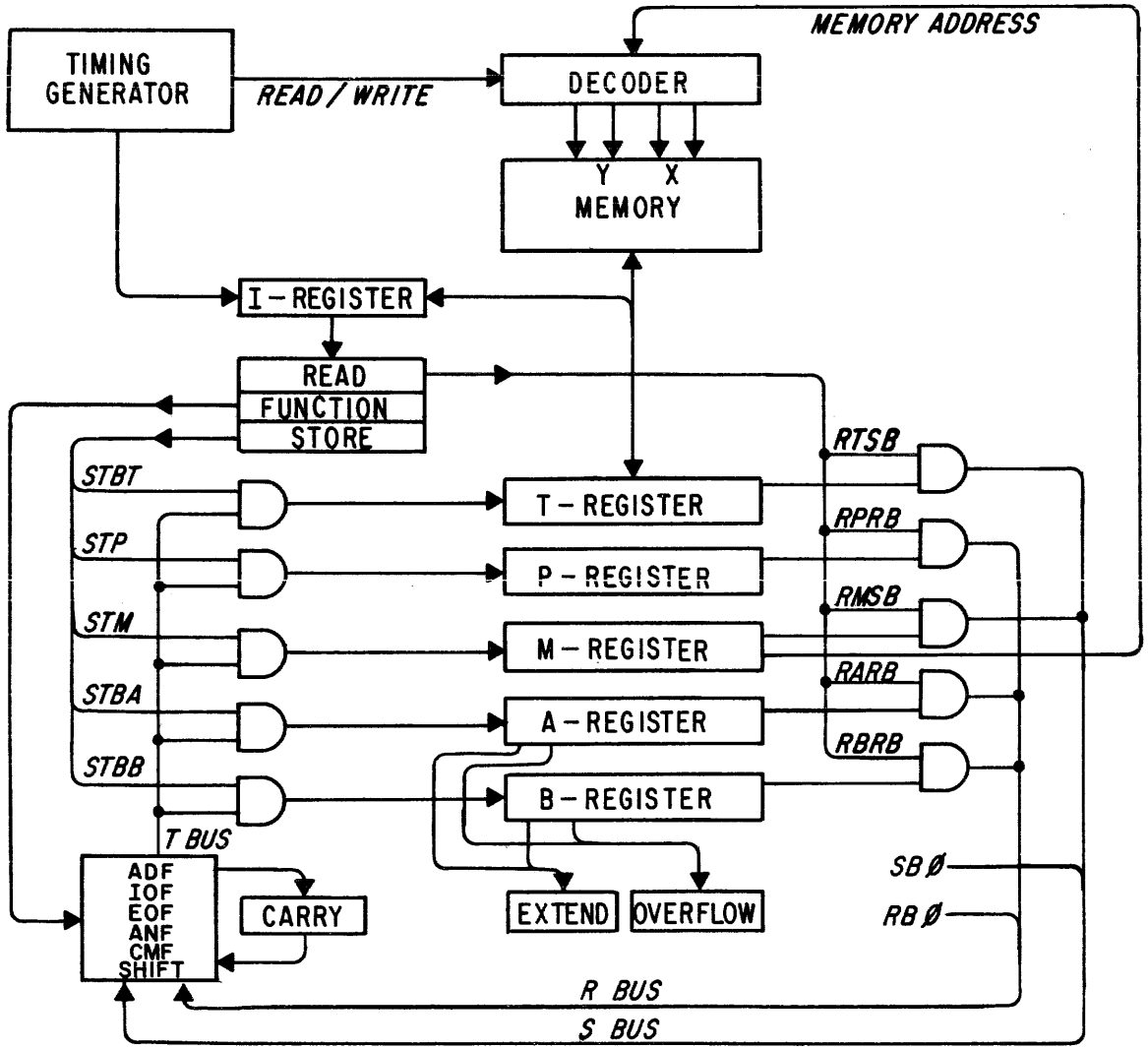
a. Mnemonic Signal Names

(1) Mnemonics are memory aiding terms used to describe control functions and logic signals. The student must become familiar with the mnemonics to effectively troubleshoot the computer.

b. Bus System Review (Figure 1-19)

(1) The HP 2116B/HP 2115A Computer uses an "R-S-T" bus configuration. This is a conventional notation designating a three-bus system which applies two input buses (R and S) to an arithmetic unit with output on the third bus (T). The use of two input buses permits arithmetic operations combining the contents of two registers. A common example would be the execution of the "ADA 100" instruction. In this example, the contents of location 100 is the number 22_8. During execution of the instruction, this number (22) would be read into the T-Register. The other number (1000_8) is in the A-Register. Simultaneously, both the T-Register and the A-Register are read onto their respective buses (S and R). The two numbers are added in the Arithmetic Logic circuits, and the result (1022_8) is stored, via the T bus, back into the A-Register as the accumulated sum.

(2) Note that several register combinations are possible as inputs to the Arithmetic Logic. One point worth noting is that since the A and B Registers are addressable as memory locations, the contents of these registers can be transferred via the R and T Buses into the T-Register. From this point, the contents can be combined in the manner described above with either



SIMPLIFIED BLOCK DIAGRAM

FIG. 1-19

accumulator (including combining the number with itself; e. g., "add A to A"). This is all accomplished in one instruction.

(3) As indicated, timing is essential to the operation of the Instruction Logic. The following descriptions do not detail all timing relationships, since these vary with instructions, but it should be understood that timing pulses are gated with each operation to make it occur in proper sequence.

(a) As shown, the six most significant bits read out of memory during each Fetch phase are stored in the 6-bit Instruction Register (I-Reg), which decodes the instruction. (Actually, the Instruction Register receives its information via the T-Register.) This instruction will be retained in the I-Register and be used in other phases required by the instruction. The decoded instruction enables three functional operations, which in turn will become active at specified times, depending on the instruction.

(b) READ. The Read signal, shown connected to the output gate of all five working registers, strobes the data of one or two registers onto their corresponding buses (R and S). This places the data at the input of the arithmetic logic circuits.

(c) FUNCTION. The Function signal activates one of the six listed arithmetic functions. The selected function alters or combines the data on the R and/or S Buses, and routes the resulting data out on the T Bus.

(d) STORE. The Store signal, shown connected to the input gate of all five working registers, effectively opens the

input of one or more of these registers to accept the data which appears on the T Bus (preceding paragraph). In many cases, depending on the instruction, only part of the information on the T Bus is stored into a register.

(4) As indicated, the Input/Output Control Logic is used to process all input/output operations. Input/Output Control operates in two ways:

(a) Processes input/output instructions.

(b) Processes service requests by peripheral devices.

These two types of operations are separately discussed in the following paragraphs.

(5) Input/Output instructions decoded by the Instruction Register and routed to Input/Output Control, which translates the instruction into appropriate driving signals. One such signal is an "In" signal, which strobes all interface positions for input (represented by two AND gates, one accepting data from a Buffer register and one accepting data from the Switch Register). Only one of these interface positions can be enabled, according to the Select Code (Bits 0 through 5 from the T-Register), and the corresponding data is strobed by the "In" pulse onto the S Bus. From there it is transferred via the T Bus into the A or B Register (as enabled by a Store signal at the A or B input gate).

(a) Another driving signal is the "out" signal. This signal strobes all interface positions for output. The Select Code from the T-Register enables one interface position, and permits the "Out" signal to strobe the data on the R Bus into the corresponding output Buffer. (The data on the R Bus was read out of the A or B Registers by a Read signal.)

(b) In addition to transferring data, as in the preceding two paragraphs, Input/Output Control can (according to instruction) send out signals to test the state of the Flag bit (F), or to set or reset the Control and Flag bits. The Select Code determines which interface will receive the signal from Input/Output Control. The Control and Flag bits are command signals for transferring data between the Buffer and the peripheral device (peripheral not shown).

(6) If a specific instruction has at some previous time enabled the interrupt system (considered to be in the Input/Output Control block), a peripheral device may request new data from the Computer (if output) or request to feed new data to the Computer (if input). This request for service is done by setting the interface Flag bit. The Flag signal, via Input/Output Control, interrupts the computer's operation by forcing the M-Register to be set (via the T Bus) to a memory address uniquely specified by the Flag. At the same time, the Fetch phase is set so that the computer must execute the instruction contained in the specified memory cell. Generally, this instruction will be a jump to a service subroutine. This subroutine consists of instructions that will prepare or accept the new data. On completion of service, it is the subroutine's responsibility to return the P and M Register to the values they contained before being interrupted.

3. Logic Control (Figure 1-19)

a. Indirect Logic

(1) The Indirect phase begins by clearing the T-Register during TØ. Then a new word is read into the T-Register from a memory location specified by the M-Register. This word is an address, not data, since indirect addressing really means: "go to another location for the data". During T6 and T7 of the Indirect phase, this address is transferred from the T-Register to the M-Register (all 16 bits). Note that it is possible for Bit 15 to again specify Indirect addressing; if so, Phase 2 remains set and the procedure of this paragraph is repeated, and could be repeated several times. When Bit 15 is a zero (Direct), Phase 3 is set.

		MEMORY READ		MST	MEMORY WRITE				
INSTRUCTION	PHASE	TØ	T1	T2	T3	T4	T5	T6	T7
ALL * MEMORY REFERENCE	2	CLEAR TR						READ TR ⟶ S BUS 1 ⟶ ADF STORE T BUS ⟶ M	

*EXCEPT JMP

b. LDA Logic

(1) During T3 and T4, the information read into the T-Register by the Read portion of the memory cycle is simply transferred to either the A or B Register via the S and T Buses.

		MEMORY READ		MST	MEMORY WRITE				
INSTRUCTION	PHASE	TØ	T1	T2	T3	T4	T5	T6	T7
LDA	3	CLEAR TR			READ TR ⟶ S BUS 1 ⟶ EOF STORE T BUS ⟶ A			P + 1 ⟶ P,M SET PHASE 1	

c. P + 1 Logic

(1) To advance the computer to the next instruction, the P and M Registers must be incremented by one. This is done during T6 and T7 of the Execute Phase. It is accomplished by reading the P-Register onto the R Bus and a "one" onto the S Bus; then adding the two buses (add function ADF) and storing the result into the P and M Registers.

		MEMORY READ		MST			MEMORY WRITE			
INSTRUCTION	PHASE	TØ	T1	T2	T3	T4	T5	T6	T7	
ALL * MEMORY REFERERENCE	3							READ P → R BUS 1 → SBØ 1 → ADF STORE T BUS → P, M		

*EXCEPT JMP

d. ADA Logic

(1) If Bit 11 of the Instruction Register indicates A (zero), the contents of the A-Register are combined with the T-Register contents by the add function (ADF), and stored into the A-Register. Similar action involving the B-Register occurs during this time (T3 through T4) if Bit 11 of the Instruction Register is a one.

		MEMORY READ		MST			MEMORY WRITE			
INSTRUCTION	PHASE	TØ	T1	T2	T3	T4	T5	T6	T7	
ADA	3	CLEAR TR			READ A → R BUS READ TR → S BUS 1 → ADF STORE T BUS → A			P + 1 → P, M SET PHASE 1		

e. STB Logic

(1) The STA/B instruction (Store A or B) deposits new information into a memory cell, with no concern for the existing memory contents. The memory data read out during the Read portion of the memory cycle is therefore inhibited while the A or B Register contents are read and stored into the T-Register (during T1 and T2). The Write portion of the memory cycle deposits this information into memory.

		MEMORY READ			MEMORY WRITE				
INSTRUCTION	PHASE	TØ	T1	T2	T3	T4	T5	T6	T7
STB	3	CLEAR TR, INHIBIT MEMORY DATA	READ B → R BUS 1 → EOF STORE T BUS → TR					P + 1 → P, M SET PHASE 1	

f. AND Logic

(1) The Fetch phase for the AND instruction is the same as for all other Memory Reference instructions listed with the exception that different functions will be set up at T2. The T-Register is cleared at time TØ, and the Read memory cycle reads the instruction word into the T-Register.

(2) The Execute phase begins by clearing the T-Register. The Instruction Register remains unchanged, since the various functions are still needed. This time, the Read portion of the memory cycle reads data from the memory into the T-Register. During T3 and T4, this data is read onto the S Bus and the A-Register contents are read onto the R Bus. The "and" function (ANF) previously set up by the Instruction Register, now combines the data on the two buses by "anding". The result on the T Bus is then stored into the A-Register.

		MEMORY READ		MST	MEMORY WRITE				
INSTRUCTION	PHASE	TØ	T1	T2	T3	T4	T5	T6	T7
AND	3	CLEAR TR			READ A → R BUS READ TR → S BUS 1 → ANF STORE T BUS → A			P + 1 → P, M SET PHASE 1	

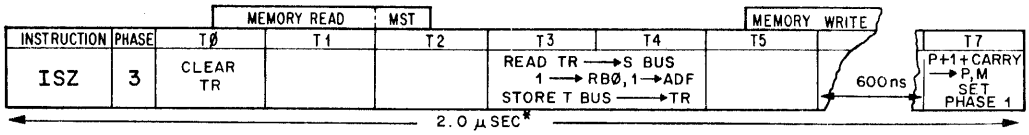
g. CPB Logic

(1) Depending on the status of Bit 11 of the Instruction Register, either the A-Register or the B-Register is combined with the T-Register contents by the "exclusive or" function. The result appears on the T Bus, but is not stored anywhere. Logic not shown tests the T Bus for a non-zero condition which, if it exists, sets the Carry Flip-Flop. Then during T6 and T7, the P and M Registers are incremented by either one (Carry not set) or two (Carry set).

		MEMORY READ		MST	MEMORY WRITE				
INSTRUCTION	PHASE	TØ	T1	T2	T3	T4	T5	T6	T7
CPB	3	CLEAR TR			READ TR → S BUS READ B → R BUS 1 → EOF IF T BUS ≠ Ø, SET CARRY FLIP-FLOP			P + 1 + CARRY → P, M SET PHASE 1	

h. ISZ Logic

(1) During the Execute phase of the ISZ instruction (Increment, Skip if Zero), the contents of the addressed memory cell must be altered and checked between the Read and Write portions of the memory cycle. These actions require more time than is normally available in this interval, so the Write portion is delayed. Once the word read from memory is in the T-Register (T3 and T4), it is incremented by reading onto the S Bus, adding "one" in the arithmetic logic and storing back into the T-Register. If previously the word read out was all ones, the addition of another one causes a rollover to all zeros, and produces a signal (C16) which sets a Carry Flip-Flop in the arithmetic logic. Then, at T5, the Write portion of the memory cycle is permitted to begin, and two Time Periods (0.4 or 0.5 microsecond) are inserted at this time for writing the incremented value back into memory. During T6 and T7, the P-Register is read onto the R Bus, and a "one" is read onto the S Bus. These are added together, and if the Carry Flip-Flop is set, another "one" is added and the result is stored in the P and M Registers. Thus, if the Carry Flip-Flop was set, the P and M Registers are incremented by two instead of one, skipping one memory location for the next Fetch phase. (The Carry Flip-Flop is automatically reset at the start of the next phase.)



i. JMP Logic

(1) The Fetch phase for all instructions, regardless of type, begins in exactly the same way, since at this time the computer logic cannot know anything about the instruction which is about

to be read out of memory. The only fact known is that the word from memory will be read as an instruction (not data); getting an instruction from memory is the first function of the Fetch phase. During the first three Time Periods of the Fetch phase, the following actions occur:

(a) During TØ the T-Register is cleared.

(b) The Read portion of the Memory Cycle begins to read the contents of the currently addressed memory cell into the T-Register. This continues until the middle of T2.

(c) During T1 the Instruction Register is cleared.

(d) Bits 10 through 15 (the instruction group and code identification) of the T-Register are transferred into the 6-bit Instruction Register.

(2) During the latter portion of T2, the functions to be used in implementing the JMP instruction are set up. This includes Read and Store as well as any arithmetic functions (none in the case of JMP). Functions are gated with Time Periods to occur in the correct sequence.

(a) At this point in time (end of T2), the instruction information is in Bits 10 through 15 of the T-Register, and in the Instruction Register. The Memory Address information is in Bits 0 through 9 of the T-Register. The next event to occur is to clear the P-Register at time T5 if the page Zero condition exists (i. e. , if Bit 10 of the Instruction Register is a zero). This is done by a "Store T Bus into P" function. Since nothing has been read onto any of the buses, the T Bus is in the all zero state, and 16 zeros are therefore stored into the P-Register. (Actually, for resetting the program to page Zero, it is only necessary to clear Bits 10 through

14 of the P-Register; however it is convenient to clear the entire P-Register at this time.) Note that the 6 most significant bits of the page Zero address are zeros; e. g., the last address on page Zero is: 1777.

(b) During Time Periods T6 and T7, the page Zero indicator (if present) clears Bits 10 through 15 of the M-Register (not the entire register). This is accomplished by RSM 10-15 at T7S. Thus at this time both P and M Registers point to page Zero, if so coded by Bit 10 being a zero (otherwise these registers are not changed, leaving bits 10 through 15 at the Current page indication).

(c) Also during T6 and T7, the Direct/Indirect bit (Bit 15) of the T-Register is looked at, to see if the Memory Address currently in the T-Register is the "effective address" (the final address being jumped to), or if another jump should be made from that address to whatever address is contained in that location (indirect addressing). Since the concept of indirect addressing is important and not always simple to grasp initially, it is treated separately in following paragraphs. For direct addressing, the execution is completed by the following steps:

1. The T-Register contents are Read onto the S Bus, and appear on the T Bus.

2. Bits 0 through 9 of the T Bus are stored into the P and M Registers. This directs the Computer to the "jump" location. (Remember from the preceding paragraphs that Bits 10 through 15 of the P and M Registers either have been reset to zero for page Zero or have been left alone for Current page.)

3. The Phase 1 (Fetch) condition remains set so that the contents of the "jump" location will be read out and interpreted as an instruction during the next machine phase.

		MEMORY READ		MST			MEMORY WRITE		
INSTRUCTION	PHASE	TØ	T1	T2	T3	T4	T5	T6	T7
JMP	1	CLEAR TR	CLEAR IR	TR (10–15) → IR			IF Z: 0 → P	READ TR → S BUS, 1 → ADF IF Z: 0 → M (10–15) IF D: TB → PM (0–9) AND SET PHASE 1 IF I: TB → M (0–9) AND SET PHASE 2	

j. JMP, I Logic

(1) Basically, the Indirect addressing indicator (Bit 15 of T-Register being a one) tells the computer logic that the contents of the location being jumped to is not the next instruction, but rather the address from another jump. This additional jump is a continuation of the same instruction, but requires an additional phase. During T6 and T7 of Phase 1, the T-Register contents are transferred to the M-Register (not both P and M as for the Direct condition). During T7 the Phase 2 condition (PH2) is set, and the Indirect phase begins.

(2) During TØ, the T-Register is cleared. Since the "jump" is still in progress, the Instruction Register is not cleared during T1. The contents of the location now addressed by the M-Register are read into the T-Register during the Read memory cycle. Then, during T6 and T7 (assuming Bit 15 of The T-Register is now 0 for Direct), all 16 bits of the T-Register are transferred into the P and M Registers in the usual way: Read T-Register onto S Bus, and Store T Bus (with no arithmetic) into P and M Registers. These registers now contain the effective address, so Phase 1 is set, and the next machine phase will be a Fetch phase, to read out the next instruction from that address. Note that if Bit 15 of the T-Register were again a one (for Indirect) a jump would be

made to still another location by repeating the process of these two paragraphs.

		MEMORY READ		MST		MEMORY WRITE			
INSTRUCTION	PHASE	TØ	T1	T2	T3	T4	T5	T6	T7
JMP	2	CLEAR TR						IF D: TB → P,M AND SET PHASE 1 IF I: TB → M AND SET PHASE 2 READ TR → S BUS, 1 → ADF	

k. JSB Logic

(1) The principal operation of the Execute phase for JSB (Jump to Subroutine) is to store the return address (Program Counter contents plus one) in the memory location being jumped to. This is done during TØ through T2. Since the only way into memory is through the T-Register, the T-Register must be loaded with the return address prior to the Write portion of the memory cycle. Therefore, the memory contents read out during the Read portion of the memory cycle must be inhibited, and instead (during T1 and T2) the current contents of the P-Register, plus one, is stored into the T-Register. (Action: Read P onto R Bus, Read "1" onto S Bus, Store with add function into T-Register.) This information is then stored into memory during Write. To complete the jump process, the contents of the M-Register (which received the "jump" memory address during the Fetch or Indirect phase) must be transferred into the P-Register. This is done during T3: Read M onto S Bus, Store T Bus in P. As usual, to advance the computer to the location of the next instruction both P and M Registers are incremented by one during T6 and T7, and the Fetch phase condition is set.

		MEMORY READ			MEMORY WRITE				
INSTRUCTION	PHASE	TØ	T1	T2	T3	T4	T5	T6	T7
JSB	3	CLEAR TR, INHIBIT MEMORY DATA	READ P → R BUS 1 → SBØ 1 → ADF STORE T BUS → TR		READ M → S BUS 1 → EOF STORE T BUS → P			P + 1 → P, M SET PHASE 1	

1. Interrupt Logic

(1) Two operations are accomplished during the Interrupt phase:

(a) The P-Register is decremented. This is done so that any instruction which has not been fully executed at the time of interrupt will be repeated. On the other hand, if the instruction is fully executed (which means that the P-Register has been advanced for the next instruction), it is still necessary to decrement. This is because the P-Register is incremented for a second time following execution of the instruction contained in the interrupt location.

(b) The "interrupt address" must be transferred into the M-Register, and Phase 1 is set. This causes the instruction contained in the interrupt location to be read out of memory for execution during the next machine phase. Note that the interrupt address is not placed into the P-Register. While the instruction in the interrupt location is being executed, the P-Register remains at the value one lower than the point at which interrupt occurred.

(2) Decrementing the P-Register is accomplished by complementing, incrementing, then complementing again. In simplified form, using only four binary digits for an example, this process is:

Original Value:	0110_2	(6_8)
Complement:	1001	
Increment:	1010	
Complement:	0101	(5_8)

(3) During T1 and T2 of the Interrupt phase (remember that there is no Read/Write memory cycle), the P-Register is read onto the R Bus. The complement function (CMF) reverses all bits before application to the T Bus, and then the T Bus is stored back into the P-Register. During T3 and T4 the P-Register is again read onto the R Bus. A "one" read onto the S Bus is combined with this by the add function (ADF), and the incremented result is stored back into the P-Register. During T5, the P-Register is read onto the R Bus for the third time, is complemented, applied to the T Bus, and stored back into the P-Register.

(4) The interrupt address is placed into the M-Register during T-7. Since no interrupt address is greater than 77_8, M-Register Bits 6 through 15 are first reset. The interrupt address is read directly onto the T Bus from Input/Output Control logic and Bits 0 through 5 are stored into the M-Register. Setting the Phase 1 condition completes the Interrupt phase.

	PHASE	TØ	T1	T2	T3	T4	T5	T6	T7
INTERRUPT	4		READ P ⟶ R BUS 1 ⟶ CMF STORE T BUS ⟶ P		READ P ⟶ R BUS 1 ⟶ SBØ, 1 ⟶ ADF STORE T BUS ⟶ P		READ P ⟶ R BUS 1 ⟶ CMF STORE T BUS ⟶ P		0 ⟶ M (6-15) STORE T BUS (0-5) ⟶ M SET PHASE 1

m. INA Logic

(1) If Bit 2 of the T-Register is a one, the A or B Register is read onto the R Bus, and a "one" is read onto the S Bus. These are combined by an add function (ADF) and stored back into the A or B Register during the latter half of T5.

		MEMORY READ		MST		MEMORY WRITE			
INSTRUCTION	PHASE	TØ	T1	T2	T3	T4	T5	T6	T7
INA	1	CLEAR TR	CLEAR IR	TR(10-15) ⟶ IR		READ A ⟶ R BUS 1 ⟶ SBØ, 1 ⟶ ADF STORE T BUS ⟶ A		P + 1 ⟶ P, M SET PHASE 1	

n. CMB Logic

(1) To complement A or B, the register is read onto the R Bus, the complement function (CMF) reverses each bit before being released to the T Bus, and the T Bus is stored back into the B Register.

		MEMORY READ		MST		MEMORY WRITE			
INSTRUCTION	PHASE	TØ	T1	T2	T3	T4	T5	T6	T7
CMB	1	CLEAR TR	CLEAR IR	TR (10-15) → IR	READ B→R BUS 1 → CMF STORE T BUS→B			P+1 → P, M SET PHASE 1	

o. SZB Logic

(1) If Bit 1 of the T-Register is a one, the A or B Register is read onto the R Bus and transmitted to the T Bus. All bits of the T Bus are applied to an "inclusive or" gate. The output of this gate and Bit 0 of the T-Register are tested. The Carry flip-flop will be set if both TR0 and the gate output are zero (meaning: "skip if accumulator is zero"), or if both TR0 and the gate output are one (meaning: "skip if accumulator is not zero").

		MEMORY READ		MST		MEMORY WRITE			
INSTRUCTION	PHASE	TØ	T1	T2	T3	T4	T5	T6	T7
SZB	1	CLEAR TR	CLEAR IR	TR (10-15) → IR		READ B → R BUS 1 → ADF IF T BUS (0-15) = Ø SET CARRY FLIP-FLOP		P + 1 + CARRY → P, M SET PHASE 1	

p. SSA Logic

(1) If Bit 4 of the T-Register is a one, the A or B Register is read onto the R Bus. Bit 15 of the R Bus (sign bit) and Bit 0 of the T-Register (Reverse Skip Sense) are tested. The Carry Flip-Flop will be set if both bits are zero (meaning: "skip if sign bit is zero"), or if both bits are one (meaning: "skip if sign bit is not zero?). This is accomplished during T4.

			MEMORY READ	MST			MEMORY WRITE			
INSTRUCTION	PHASE	TØ	T1	T2	T3	T4	T5	T6	T7	
SSA	1	CLEAR TR	CLEAR IR	TR (10-15) → IR		READ A → R BUS	IF R BUS 15=Ø SET CARRY FLIP-FLOP	P+1+CARRY→P,M SET PHASE 1		

q. CLA Logic

(1) To clear the A or B Register, the Read function is omitted. This means that both R and S Buses are in the all-zero state. This "exclusive or" fuction, in combining zeros with zeros, can only produce zeros on the T Bus. Thus, when the T Bus is stored into A or B, the result is all zeros.

			MEMORY READ	MST			MEMORY WRITE		
INSTRUCTION	PHASE	TØ	T1	T2	T3	T4	T5	T6	T7
CLA	1	CLEAR TR	CLEAR IR	TR (10-15) → IR	1→EOF STORE T BUS →A			P+1 → P,M SET PHASE 1	

r. Shift-Rotate Logic (Figure 1-20)

(1) Shifts and rotates can be executed either during T3 or T5, or both. The shifts and rotates are executed simply by reading A or B Registers into the R Bus, applying a "Shift Function" to shift some or all of the bits to a different position on the T-Bus, then storing the T Bus back into the A or B Register. Since the Shift Function is the key to understanding how shifts and rotates occur, the following instruction descriptions concentrate on this aspect.

s. A/B LS Logic

(1) As shown, the desired end result is to have Bits 0 through 13 shifted left one place, with Bit 15 unchanged and a zero moved into Bit 0. Assuming that Bits 6 through 9 of the T-Register dictate an A/BLS during T3, an SLM (Shift Left Magnitude) signal at this time is "anded" with each of the 14 R Bus bits

SHIFT-ROTATE IMPLEMENTATION DIAGRAMS

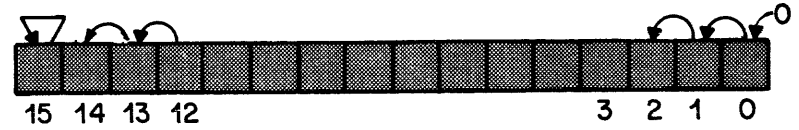
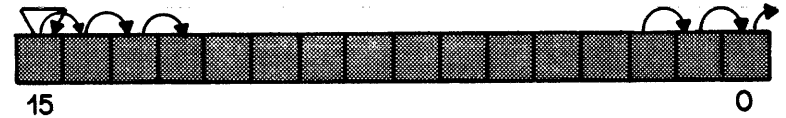
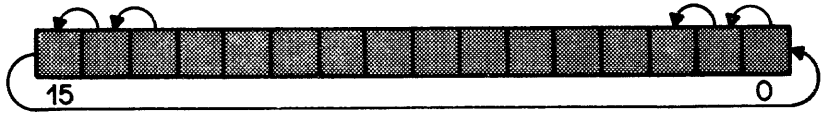
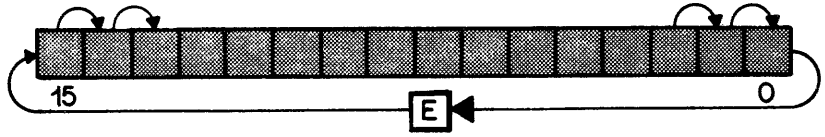
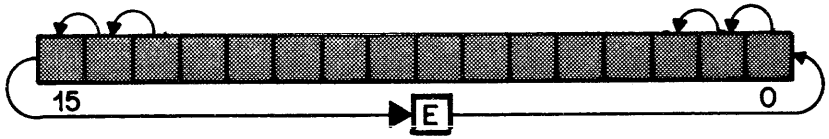
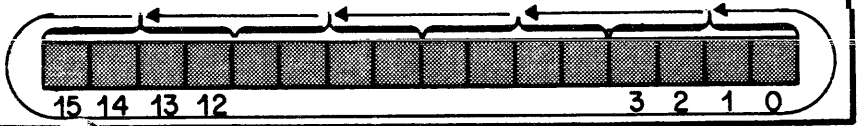
INSTRUCTION	FUNCTIONS	DIAGRAMS
A/BLS	$\overline{SLM}$·RB(0–13) RB15→TB15	
A/BRS	$\overline{SRM}$·RB(1–15) RB15→TB15	
RA/BL	$\overline{SLM}$·RB(0–13) $\overline{SL14}$·RB14 $\overline{RLL}$·RB15	
RA/BR	$\overline{SRM}$·RB(1–15) RRS·RB0	
ERA/B	$\overline{SRM}$·RB(1–15) E→TB15 RB0→E	
ELA/B	$\overline{SLM}$·RB(0–13) $\overline{SL14}$·RB14 E→TB0 RB15→E	
A/BLF	$\overline{RL4}$·RB(0–15)	

FIG. 1–20

(0 through 13), with the output of each "and" gate appearing on the next higher T Bus line. The Function listed in the Timing Chart for this instruction [SLM RB(0-13] is therefor to be read: Shift Left Magnitude "anded" with R Bus Bits 0 through 13. Bit 15 of the R Bus is routed directly out to Bit 15 of the T Bus. Since nothing has been placed onto Bit 0 of the T Bus, its state is "zero", and therefore no deliberate action is necessary to ensure storing a zero in Bit 0 of the A or B Register.

t. A/B RS Logic

(1) A Shift Right Magnitude "anded" with T Bus Bits 1 through 15 shifts these bits to Bits 0 through 14 of the T Bus. Bit 0 of the T Bus is not recognized, and Bit 15 (as well as moving onto Bit 14 of the T Bus) also is routed directly to Bit 15 of the T Bus.

			MEMORY READ	MST		MEMORY WRITE				
INSTRUCTION	PHASE	TØ	T1	T2	T3	T4	T5	T6	T7	
ALL "A" REGISTER SHIFTS & ROTATES	1	CLEAR TR	CLEAR IR	TR (10-15) → IR	READ A→R BUS 1 → SRM STORE T BUS →A		READ A→R BUS 1 → SLM STORE T BUS →A	P + 1 → P, M SET PHASE 1		

			MEMORY READ	MST		MEMORY WRITE				
INSTRUCTION	PHASE	TØ	T1	T2	T3	T4	T5	T6	T7	
OTB	1	CLEAR TR	CLEAR IR	TR (10-15) → IR	READ B → R BUS 1 → IOO			P + 1 → P, M SET PHASE 1		

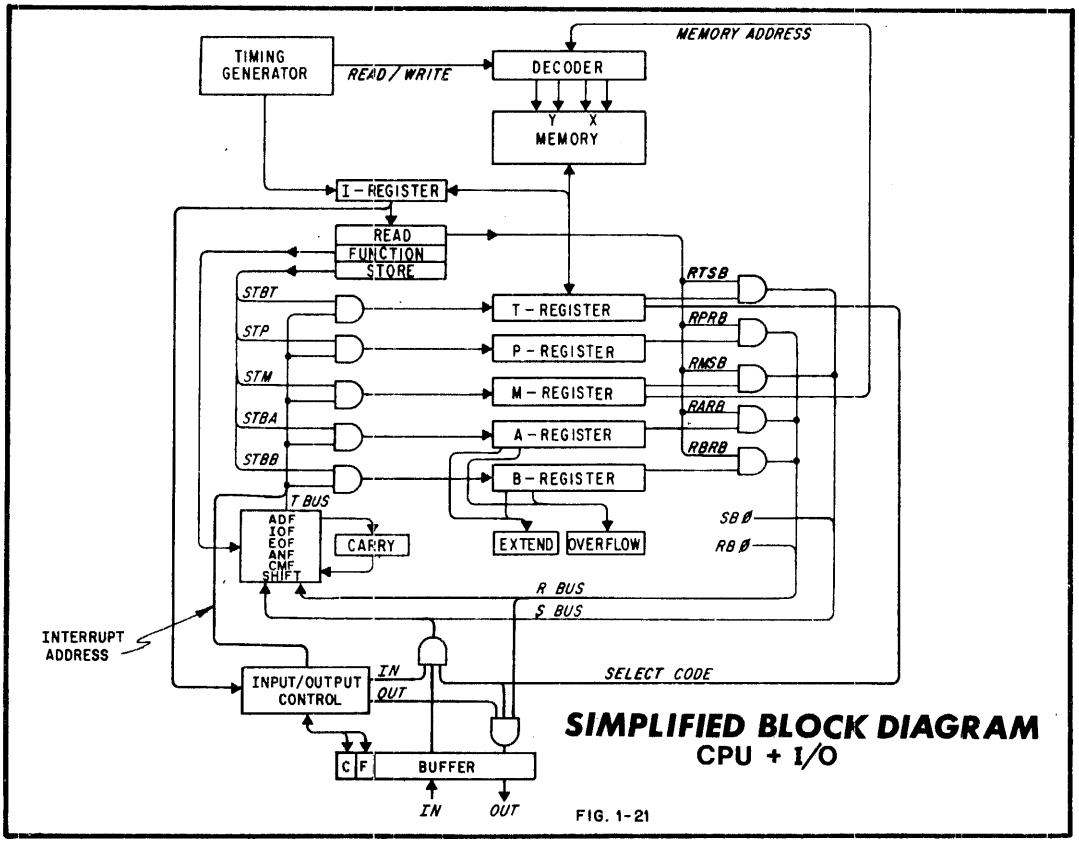
u. LIA Logic (Figure 1-21)

(1) The action for LIA/B (Load Input into A or B) is the same as for MIA/B except that nothing is read onto the R Bus. The "inclusive or" function therefore transmits the R Bus unchanged to the T Bus for storing into the A or B Register. As for MIA/B, Bit 9 can clear the Flag Flip-Flop.

		MEMORY READ		MST		MEMORY WRITE			
INSTRUCTION	PHASE	TØ	T1	T2	T3	T4	T5	T6	T7
LIA	1	CLEAR TR	CLEAR IR	TR(10—15) → IR		1 → IOI 1 → IOF STORE T BUS → A		P + 1 → P, M SET PHASE 1	

v. OTB Logic (Figure 1-21)

(1) During T4 and T5 the A or B Register is read onto the R Bus, which in turn is transferred by an IOCO signal (I/O Output Control) to the interface Buffer register. As for MIA/B, Bit 9 can clear the Flag Flip-Flop.



4. Review

(1) What is a micro-program?

(2) What type of instruction requires more than one phase?

(3) What is the Interrupt Phase used for?

(4) What two basic operations occur during the Interrupt Phase?

(5) How long is a basic machine cycle?

(6) How long is a machine cycle when executing an ISZ instruction?

(7) During which time period is memory accessed (READ)?

(8) During which time period is memory written (WRITE)?

(9) How many TS pulses occur during a machine cycle?

(10) What is the primary purpose of the RST bus?

(11) How many RST buses are there in the HP 2116B/HP 2115A Computer?

(12) How many working registers are there in the HP 2116B/ HP 2115A Computer?

(13) What is the purpose of each working register?

(14) What two operations are common to all I/O instructions?

(15) What is the "microprogram" for the Indirect Phase?

(16) What is the "microprogram" for P+1?

(17) How long is the machine cycle when implementing an ISZ instruction?

(18) What is the "microprogram" for an ISZ instruction?

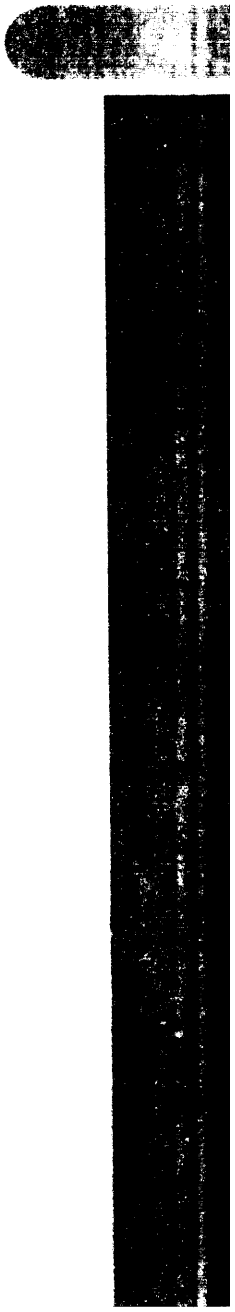
(19) What is the "microprogram" for a JMP instruction?

(20) What is the "microprogram" for JMP,I?

(21) What is the "microprogram" for a JSB instruction?

(22) What is the "microprogram" for the Interrupt Phase?

system timing and control



System Timing and Control

A. INTRODUCTION

1. Objectives

a. Purpose

(1) The student at this point in the course has used the selected instruction group in programming the Computer. He has also seen how the selected instructions are implemented through the use of simplified diagrams, timing charts and logic equations. At this point, the student is ready for a discussion of the Central Processor Unit logic. The purpose of this lesson is to introduce the student to the five basic boards comprising the CPU section.

b. Approach

(1) The primary teaching tool for the CPU section will be the schematic diagrams. Each major functional block of each logic board will be discussed as a unit using overhead slides. The discussion of each block should be concluded as quickly as possible. However, the unique circuitry of each board should be understood. The emphasis will be on signal tracing using the simplified logic diagrams as a guide to the overall operation in progress, and also to supply timing information.

2. The Central Processor Unit (Schematics)

a. System Timing Generator

(1) This board provides the basic 5 MHz (4.0 MHz in HP 2115A) clock and all timing signals for the computer. It consists of six basic circuits:

(a) An Oscillator and Frequency Divider which provides the basic 5 MHz (4.0 MHz) clock and generates the TS pulse each 200 ns (250 ns in HP 2115A). A TSA pulse is generated for use by the EAU.

(b) A Time Period Generator which provides the eight basic timing pulses TØ thru T7.

(c) A Memory Timing circuit which controls the reading and writing of data from or to memory.

(d) The Phase Decoder which provides the four basic machine phase signals: PH1, PH2, PH3, and PH4.

(e) The Run-Halt circuit which controls the operational modes Run, Halt, and Single Cycle.

(f) A Control Switch circuit which provides access to certain control signals originating on the front panel console.

b. Instruction Decoder

(1) This board determines which instruction is to be implemented, and also provides most of the control signals to implement that instruction. The board consists of four functional blocks:

(a) A Memory Reference and Group Instruction Decoder which decodes all memory reference instructions, and decodes the ASG, SRG, and I/O groups.

(b) A Read circuit which controls reading all register data onto the R-S-T buses.

(c) An Arithmetic circuit which allows performing the required logical and arithmetic operations.

(d) A Store circuit which controls storing data from the "T" bus into the various registers or memory.

c. Shift Logic

(1) This board derives its name from the fact that the shift and rotate functions are generated here. This board also performs the final decoding for the ASG, SRG and I/O Group instructions. This board consists of six functional blocks:

(a) A Halt Instruction and Preliminary Group Instruction Decoder which decodes the halt instruction, and determines whether a group instruction is in the SRG or I/O

group. Since these two groups cannot be active at the same time, a considerable savings of gates is realized by sharing the decoding network between both groups.

(b) An I/O Instruction Decoder which decodes all I/O instructions.

(c) A Shift-Rotate Decoder which decodes all SRG instructions.

(d) The Carry circuit which sets the Carry FF under certain circumstances.

(e) The A/B Addressable Flip-Flops which allow the A and B registers to be used as memory locations.

(f) The Extend/Overflow circuit which controls the Extend and Overflow Flip-Flops.

d. Arithmetic Logic

(1) These boards contain the five working registers and the required arithmetic logic circuits to read, store and transfer data. These boards contain two functional blocks:

(a) The Register Flip-Flops (A, B, T, P, and M).

(b) The Logic and Arithmetic circuits which control the actual logical or arithmetic operations.

e. Front Panel Coupler

(1) The Front Panel Coupler essentially provides the necessary communication between the front panel control switches and the central processor unit.

(2) The Front Panel Couplers for the HP 2116B and HP 2115A are not interchangeable.

3. Review

(1) What is the purpose of the Timing Generator board?

(2) In which circuit on the Timing Generator board is the TS pulse generated?

(3) In which circuit on the Timing Generator board are the basic TØ-T7 pulses generated?

(4) In which board are all memory reference instructions decoded?

(5) On which board(s) are the ASG, SRG and I/O instructions decoded?

(6) On which board is the Carry Flip-Flop located?

(7) On which board are the Addressable A and B Flip-Flops?

(8) On which board are the Extend and Overflow Flip-Flops located?

(9) On which board(s) are the five main working registers located?

(10) On which board are the actual logical and arithmetic operations performed?

B. SYSTEM TIMING GENERATOR

1. Oscillator and Frequency Divier (Figure 2-1)

a. Oscillator

(1) Transistor Q1 is a 10 MHz (8 MHz for HP 2115A) crystal controlled oscillator circuit. The circuit is a modified Colpitts.

(2) The output from pin 3 (Ext Clock) of the board is a series of sharp positive pulses approximately 2.5 volts peak to peak with a period of 100 nanoseconds for the HP 2116B and 125 nanoseconds for the HP 2115A.

b. Frequency Divider

(1) The frequency divider consists of two J-K flip-flops and two AND gates. The crystal oscillator frequency is the clock input for the first divider flip-flop MC82. The J and K inputs are tied to 4.5 volts so on the trailing edge of each clock pulse flip-flop MC82 changes state. The "1" side output of MC82 becomes the clock input to the second divider flip-flop MC72. The J and K inputs of this flip-flop are tied to 4.5 volts so this flip-flop also changes state on the training edge of each clock input. The output frequency of divider MC82 is one half the crystal frequency and the output frequency of MC72 is one half the frequency of MC82. The "1" output of MC82 is gated

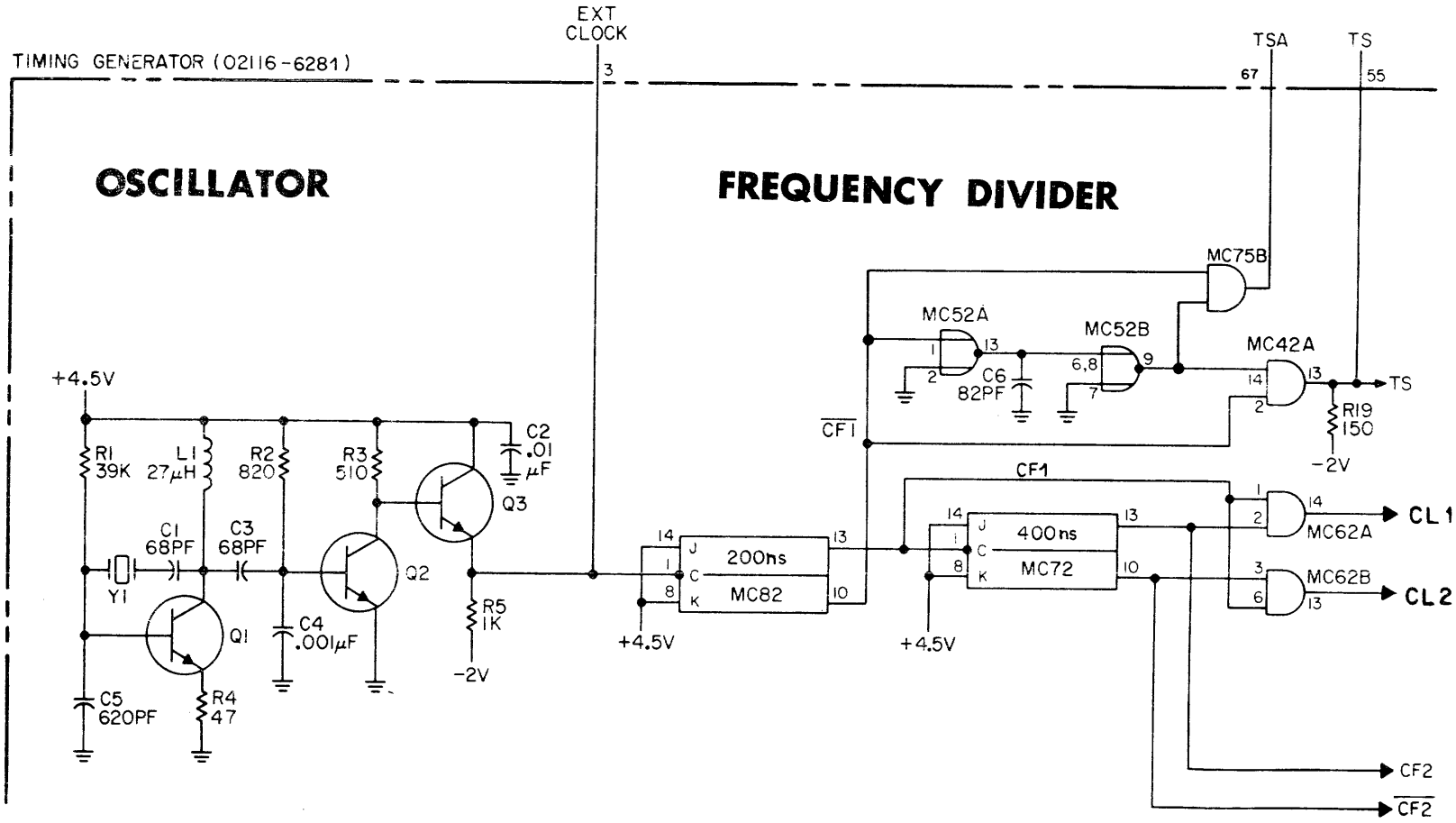
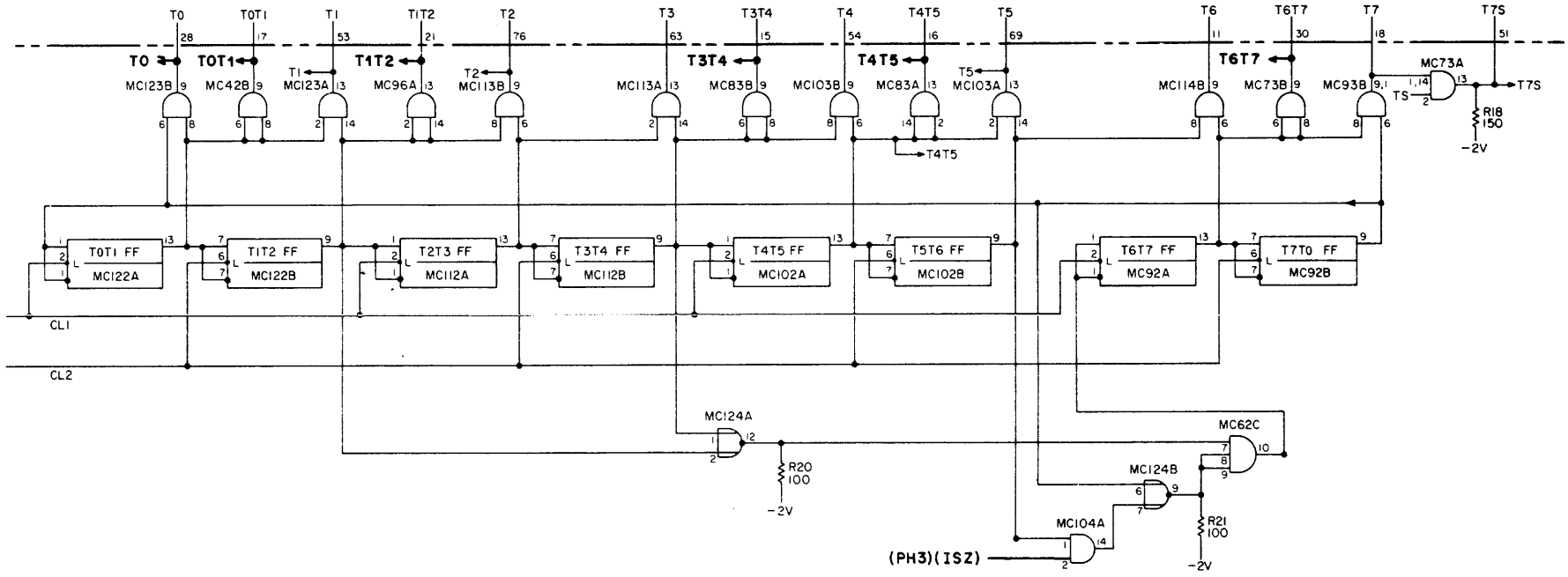

TIMING GENERATOR (02116-6281)
EXT CLOCK
3
TSA
67
TS
55
OSCILLATOR
FREQUENCY DIVIDER
+4.5V
R1 39K
L1 27μH
R2 820
R3 510
C2 .01 μF
Q3
C1 68PF
C3 68PF
Q2
Y1
Q1
C4 .001μF
R5 1K
-2V
C5 620PF
R4 47
200ns
MC82
+4.5V
MC75B
MC52A
MC52B
C6 82PF
MC42A
TS
R19 150
-2V
CF1
CF1
400ns
MC72
+4.5V
MC62A
CL1
MC62B
CL2
CF2
CF2

FIG. 2-1



TIME PERIOD GENERATOR

FIG. 2 -2

with the "1" and "0" outputs of MC72 to produce a 100 (125 for HP 2115A) nanosecond pulse every 400 (500 for HP 2115) nanoseconds from gates MC62A (CL1) and MC62B (CL2).

(2) The time period strobe signal (TS) developed by gating the "0" output of MC82 with the same signal delayed by approximately 50 nanoseconds. Thus, TS is approximately 50 nanoseconds long with the leading edge delayed by 50 nanoseconds and the trailing edge coincident with the MC82 output. In the HP 2116B, the $\overline{CF1}$ and delayed $\overline{CF1}$ signals are also used to generate a TSA signal for the EAU. This signal is routed out pin 67 via gate MC75B.

2. Time Period Generator

a. The Latching Flip-Flop (Refer to Figure 1-10)

(1) The latching flip-flop is used extensively in the Timing Period Generator. This type of flip-flop responds to input signals as follows: The flip-flop is free to follow the input signal (A) whenever the latching input (C) is true. When C goes false, the flip-flop is "latched" in its present state.

b. Modified Ring Counter (Figure 2-2)

(1) The Time Period Generator consists of 8 latching type flip-flops which form a modified ring counter. The ring counter has a start-up circuit that automatically provides proper circuit action with application of power. The outputs of the flip-flops are gated using 14 AND gates to provide the actual time period pulses. The basic machine cycle is divided into eight equal time periods of 200 (250 for HP 2115A) nanoseconds each. The periods are labeled TØ through T7. Each even numbered flip-flop in the ring counter is clocked by CL1. The odd numbered flip-flops are clocked by CL2. The frequency of each clock pulse itself is 2.5 (2.0 for HP 2115A) MHz but because of the interlacing of CL1 and CL2, the effective clock frequency is 5.0 (4.0 for HP 2115A) MHz.

(2) At turn on time assume that all flip-flops are in the reset state, and MC124A and MC124B are producing true outputs. This provides a true output from gate M62C. This signal combined with positive clock pulse CL1 causes flip-flop T6T7 to set. On the next active clock (CL2) flip-flop T7TØ sets. The setting of T7TØ disables gate MC124B and the start up circuit unlatches. On the next active clock pulse (CL1) flip-flop TØT1 will set and flip-flop T6T7 will reset. Since flip-flop T7TØ did not have an active clock pulse, it remains set. The normal condition for this circuit is for two adjacent flip-flops to be set and all others reset. The next clock pulse (CL2) will cause flip-flop T1T2 to set and flip-flop T7TØ to reset. Flip-flop TØT1 remains set because no active clock was present at the input. Flip-flop T1T2 disables gate MC124A which keeps the turn on circuit disabled even though gate MC124B is now producing a true output. Circuit operation continues in this manner until flip-flops T4T5 and T5T6 are both set. At this time the turn on circuit is again enabled such that when clock pulse CL1 appears the true output of gate MC62C causes flip-flop T6T7 to set at the same time causing T4T5 to reset. The circuit continues to operate in this manner with two, and only two, adjacent flip-flops in the true state regardless of the initial turn on state of the flip-flops themselves.

c. Timing Relationships (Figure 2-4 and 2-5)

(1) The timing period signals TØ-T7 are produced by gating the two adjacent flip-flops that are in the "1" state. The TØT1 FF gated with the T1T2 FF produce the timing signal T1. This method of operation produces timing pulses that are free of gating spikes. Time period T7 combined with TS produces a signal called T7S. Time periods TØT1, T1T2, T3T4, T4T5, and T6T7 are the actual outputs of the flip-flops themselves after passing through single input AND gates.

sustained by MC77A and MC77B. MRT is initiated by gate MC77A (TØT1 · $\overline{CF2}$) and sustained by MC77B. Capacitor C11 is removed if an 8K memory module is installed. MC47A output is normally false indicating that a protected location has not been addressed. MC47A enables a true output from MC46A. MC27C will provide MTE if the MEMORY NORMAL/OFF switch is in the NORMAL (MNS) position.

b. Memory Strobe Timing

(1) The memory strobe timing (MST) signal gates the output of the memory sense amplifiers to provide a clean logic level for the T-Register's direct set inputs. This signal is produced by gating MRT and T2. The AND gate MC57B is an inhibiting gate that prevents MST from coming up whenever the computer performs a Clear/Write memory cycle. Inhibiting factors are:

(a) Addressable A and B registers (AAF)(BAF)

(b) Load Memory Switch or Inhibit Strobe Generator (LMS) (ISG). (ISG is used with EAU and DMA only.)

(c) Phase 3 of JSB and STR (PH3)(JSB)(STR)

(2) In the HP 2116B, Jumpers W1 and W2 provide the means of delaying MST. With jumper W1 installed (14K-16K) MST is gated on at the start of T2. But with W1 removed and W2 installed, MST is not gated on until the middle of T2. This is done by gating CF1 with MTE via MC47B. This delayed MST is necessary in the HP 2116B if equipped with non-adjustable sense amplifiers.

c. Memory Write Timing

(1) The MWL signal is a level that is supplied to the Parity Error board and DMA so that whenever the computer writes new information into memory the proper status of bit 16 (Parity Bit) can be determined before Memory Write time. Gate MC104B enables MWL for Phase 3 and ISZ which is a unique Read/Increment/Write cycle.

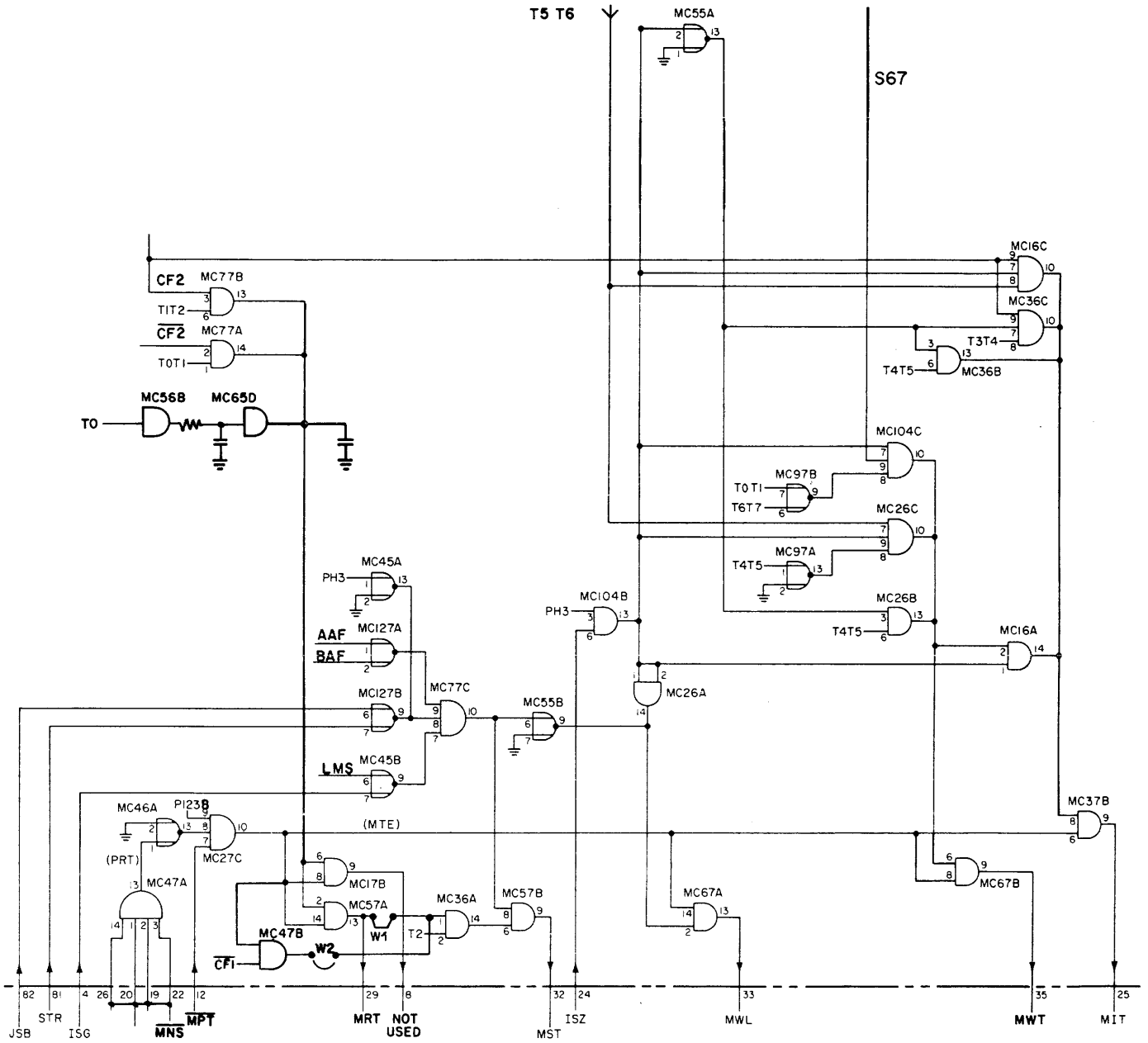
(2) Extended cycle Phase 3 ISZ. The Execute phase of the ISZ instruction is 2.0 (2.5 for HP 2115A) microseconds. The turn on circuit is used to extend the computer Execute cycle by two time periods. Assume flip-flops T4T5 and T5T6 are set. If ISZ and Phase 3, then MC104A will be enabled and the high input to gate MC124B disables the turn on circuit until flip-flops T4T5 and T5T6 are shifted clear. When flip-flop T5T6 goes false, the MC104A output goes false which enables the turn on circuit to provide a true output from gate MC62C. Clock signal CL1 then allows flip-flop T6T7 to be set and circuit operation returns to normal.

3. Memory Timing (Figure 2-3)

a. Memory Read Timing

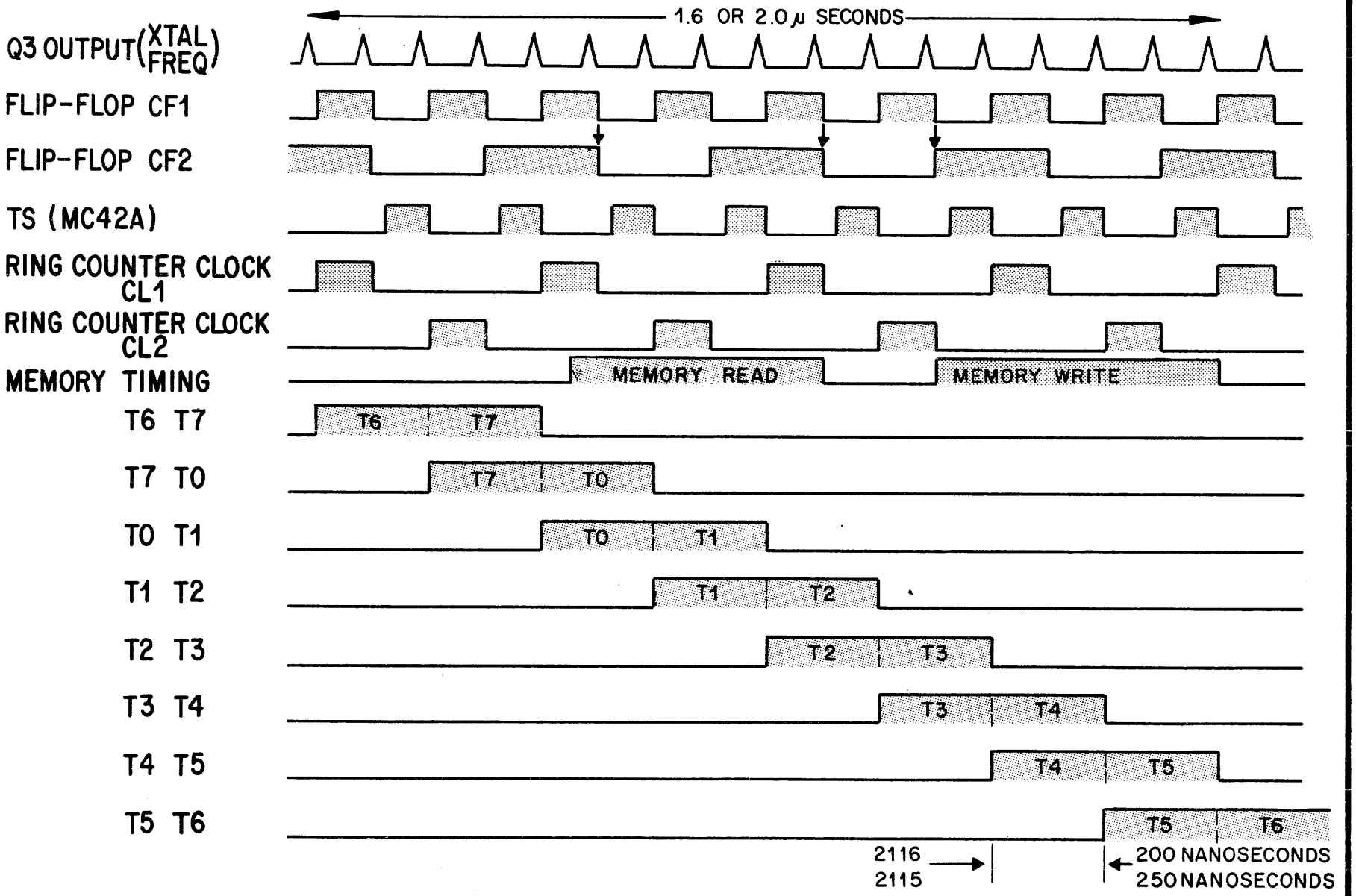
(1) Memory read timing (HP 2116B) pulses are 460 nanoseconds pulses starting 40 nanoseconds beyond the start of TØ and extending one half time period beyond the start of T2. Memory read timing is initated by gating TØ through a delay circuit made up of MC56B, C12, MC65D and C11. This circuit provides approximately 40 nanoseconds of delay. Read timing is sustained by gates MC77A ($\overline{CF2} \cdot T\emptyset T1$) and MC77B ($CF2 \cdot T1T2$). Gate MC47A inhibits memory read write timing signals when the MEMORY ON/OFF switch is in the OFF position. Under normal operating conditions gate MC47A output is false. This false output enables gate MC46A to produce a true output. Gate MC27C produces a true signal MTE (Memory Timing Enable) as long as a protected memory location is not addressed. Signal MTE is gated with the timing signals developed by MC65D, MC77A and MC77B to produce the actual timing signal MRT (Memory Read Timing) at gate MC57A.

(2) Timing in the HP 2115A is basically the same with only minor differences. The HP 2115A generates two Memory Read Timing pulses; MRT and MRTØ. The MRTØ is initiated at TØ delayed approximately 60 nanoseconds (MC47B, C12 and MC17A) and is



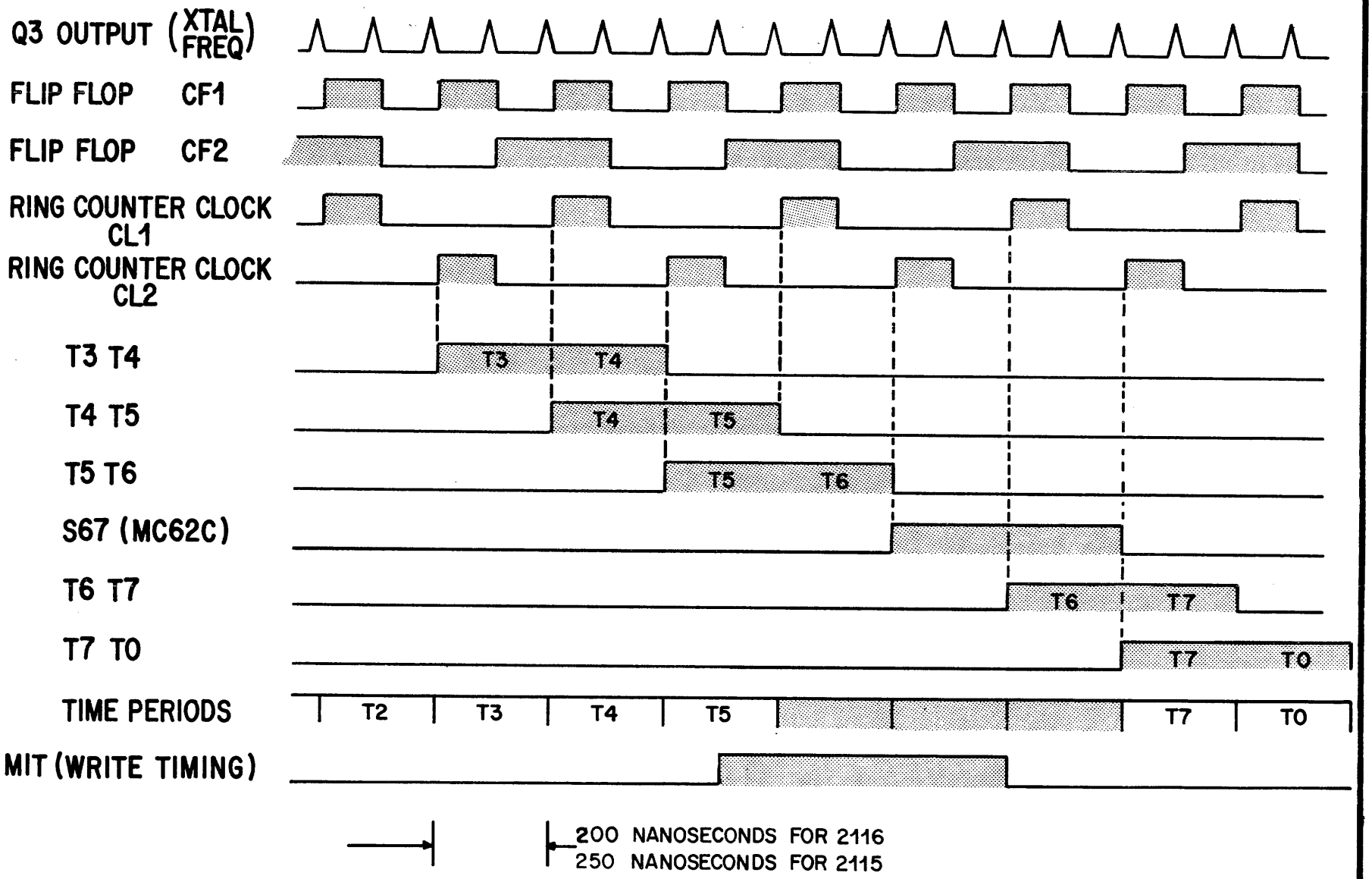
MEMORY TIMING

FIG. 2-3



COMPUTER TIMING CHART (BASIC CYCLE)

FIG. 2—4



COMPUTER TIMING CHART (Extended Cycle) 2.0 or 2.5 μ SECONDS

FIG 2-5

(2) Normal Memory write timing starts one-half time period beyond T3 and extends 500 (625 for HP 2115A) nanoseconds to the end of time period T5. Normal memory write timing is developed by gates MC36B and MC36C. The "1" side output of divider flip-flop MC72 is gated with T3T4 and Phase 3 $\overline{\text{ISZ}}$, using gate MC36C. The output of this gate provides the first portion of the timing signal. Gate MC36B inputs are Phase 3, $\overline{\text{ISZ}}$ and T4T5. The output of MC36B is "or" tied to MC36C to provide the last portion of the normal memory write timing signal. Normal memory write timing is gated with MTE (Memory Timing Enable) to produce MIT (Memory Inhibit Timing). The memory write timing signal MWT is generated at T4T5 or T5T6 (ISZ) by gating MTE with those timing signals from MC97B, MC97A, MC104C, MC26C, MC26B and MC67B.

(3) Delayed memory write (Phase 3, ISZ) timing is delayed by two full time periods when in Phase 3 ISZ. Normal memory write timing is inhibited by the false output of gate MC55A which inhibits MC36C and MC36B. The true output of MC104B inhibits gate MC55A and enables gate MC16C. The other inputs to MC16C are the "1" side of divider flip-flop MC72 and T5T6. The output of MC16C begins one half time period beyond T5 which is exactly two full time periods later than normal memory write time. At the end of T5, gate MC26C is enabled as gate MC16C is inhibited. Gate MC26C provides a true output until the T5T6 Flip-Flop MC102B is shifted clear. At that time, the start up circuit is enabled and gate MC26C provides a true output for gate MC104C which provides a true output until the next active clock sets flip-flop T6T7. At this time all "or" tied gates connected to the input of gate MC16A are inhibited, and the Phase 3 ISZ memory write time ends.

4. Phase Decoding (Figure 2-6)

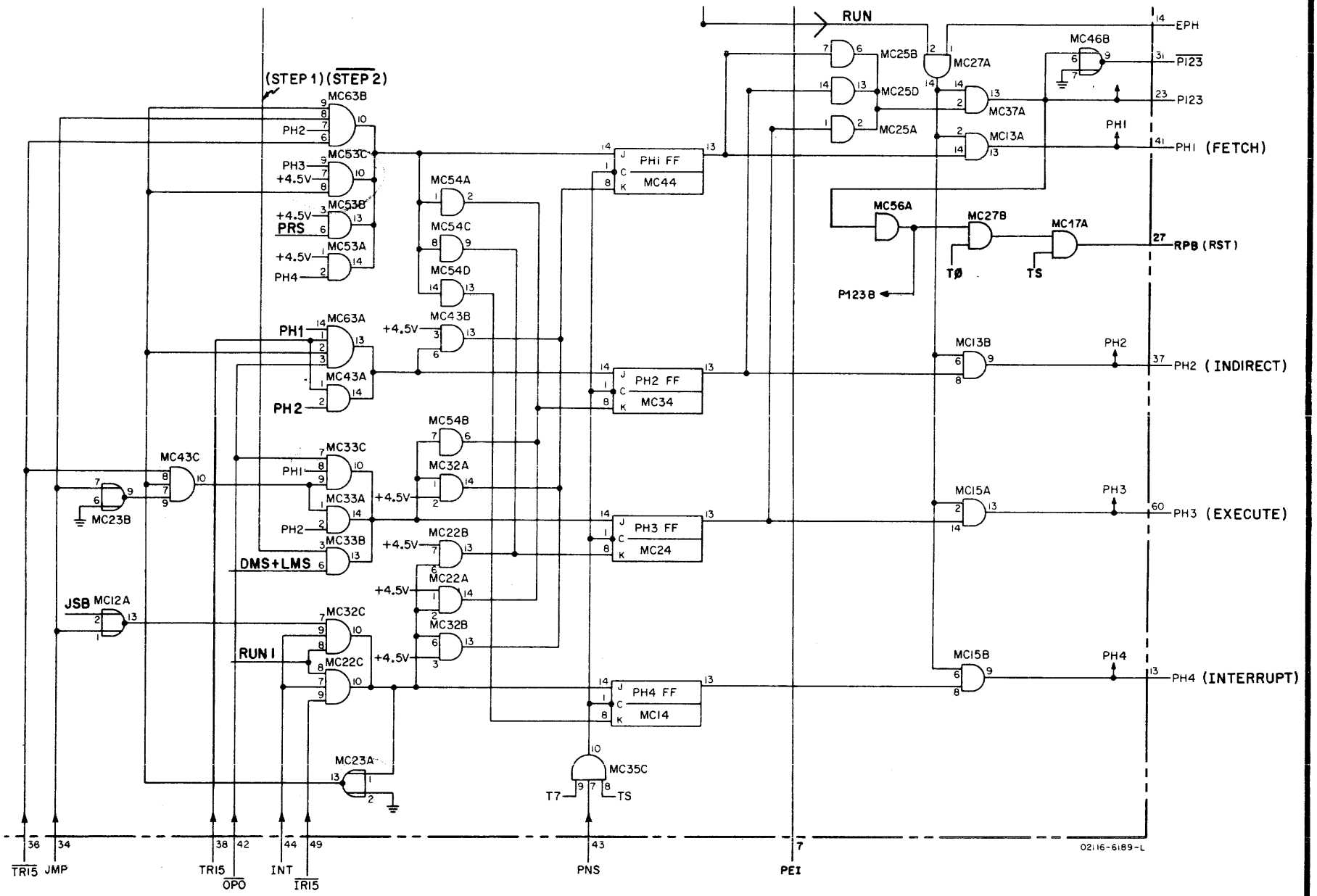
a. Phase Changes

(1) The phase logic section supplies Phase 1, 2, 3, or 4 signals to the remaining computer circuit boards. The computer may be in one, and only one, phase at any given point in time. The phase logic circuits ensure this and also provide for logical phase transition. The computer is initialized to the Fetch phase with application of power or by depressing the PRESET switch. It should be noted that a maintenance assisting signal PNS (Phase Normal Switch) will prevent any change in computer phase, and if power is applied with the switch in the maintenance position, the initialization to Fetch phase may not occur. Phase changes occur by setting the appropriate Phase Flip-Flop at the trailing edge of the clock pulse (T7· TS·PNS). Logical phase changes are:

(a) Phase 1 to Phase 1
(b) Phase 1 to Phase 2
(c) Phase 2 to Phase 3 except for JMP, I
(d) Phase 2 to Phase 1 JMP, I only
(e) Phase 1 to Phase 3
(f) Phase 3 to Phase 1
(g) Any Phase to Phase 4
(h) Phase 4 to Phase 1 only

b. Phase Logic

(1) Gate MC63B will set Phase 1 after JMP, I. Gate MC53C allows the setting of Phase 1 after a Phase 3 providing no Interrupt has occurred. Gate MC53B forces Phase 1 at turn on or pre-set time. Gate MC53A forces Phase 1 after Phase 4. Gate MC63A allows Phase 2 to be set after Phase 1 (providing the instruction fetched is an indirect memory reference instruction and no Interrupt has occurred). Gate MC43A forces the setting of Phase 2 during multi-level indirect operations. Gate MC33C allows the setting of Phase 3 after Phase 1 for direct memory reference instructions, except JMP, providing no Interrupt has occurred. MC33A allows the setting of Phase 3 after Phase 2



PHASE LOGIC

FIG 2-6

for all memory reference, except JMP, providing no Interrupt has occurred. Gate MC33B forces the computer to Phase 3 for a single cycle operation when the LOAD MEMORY or the DISPLAY MEMORY switches are depressed. Gates MC32C and MC22C allow the setting of Phase 4 providing no JSB, I or JMP, I is in progress and the computer is in the Run mode. All the gates connected to the reset side ("K" inputs) of the Phase Flip-Flops ensure that only one Phase Flip-Flop is set at any given time.

(2) A Phase 1 to Phase 1 transistion is made by default; that is, both "J" and "K" inputs to the Phase 1 Flip-Flop MC44 are "Ø". With this condition, the flip-flop remains set.

(3) The T-Register is normally cleared at every TØ and P123 by a signal RST (Reset T-Register) generated on the Instruction Decoder board. However, when the DMA option interrupts, the machine enters a Phase 5 operation and the RST signal is inhibited since no P123 signal is available to gate RST on. To clear the T-Register when entering a Phase 5 operation, a pseudo P123 signal is generated on the DML board (Direct Memory Logic) and sent to the Timing Generator board via pin 23. This P123 signal is also gated with TØ and TS (via MC27B and MC17A) to provide a RPB (Reset Parity Bit) signal via pin 27.

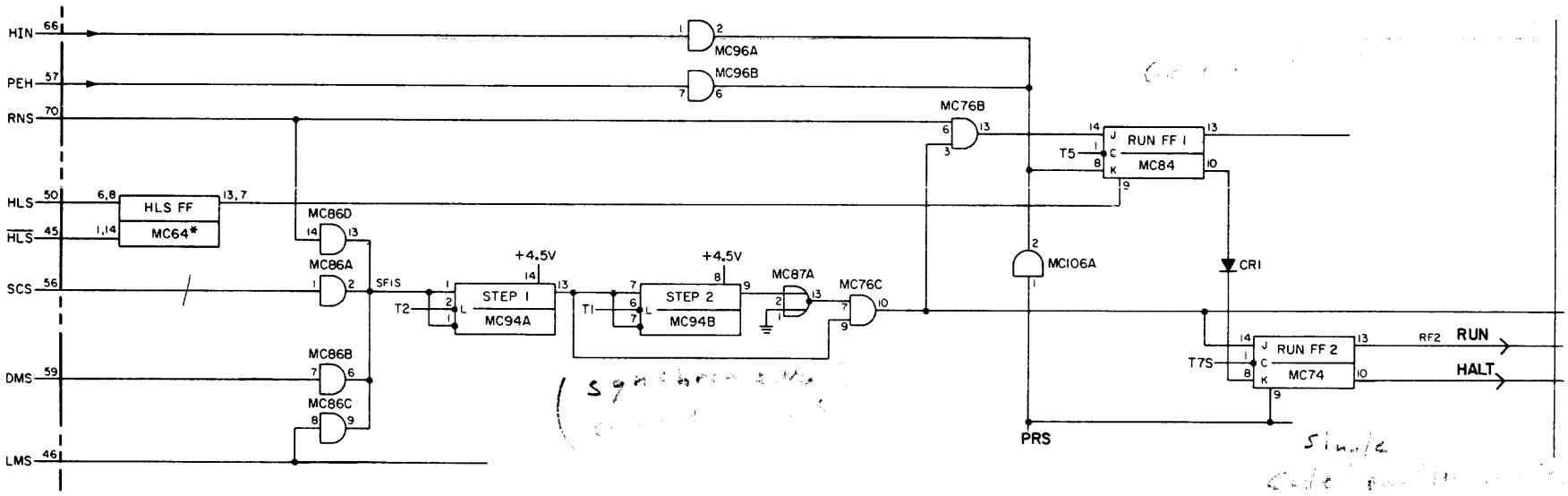
(4) The PEI (Parity Error Interrupt) signal enters the Timing Generator board at pin 7 to turn on Q9 (parity error halt lamp driver) whenever a parity error occurs.

5. Run-Halt Logic (Figures 2-7 and 2-8)

a. Run-Halt Mode

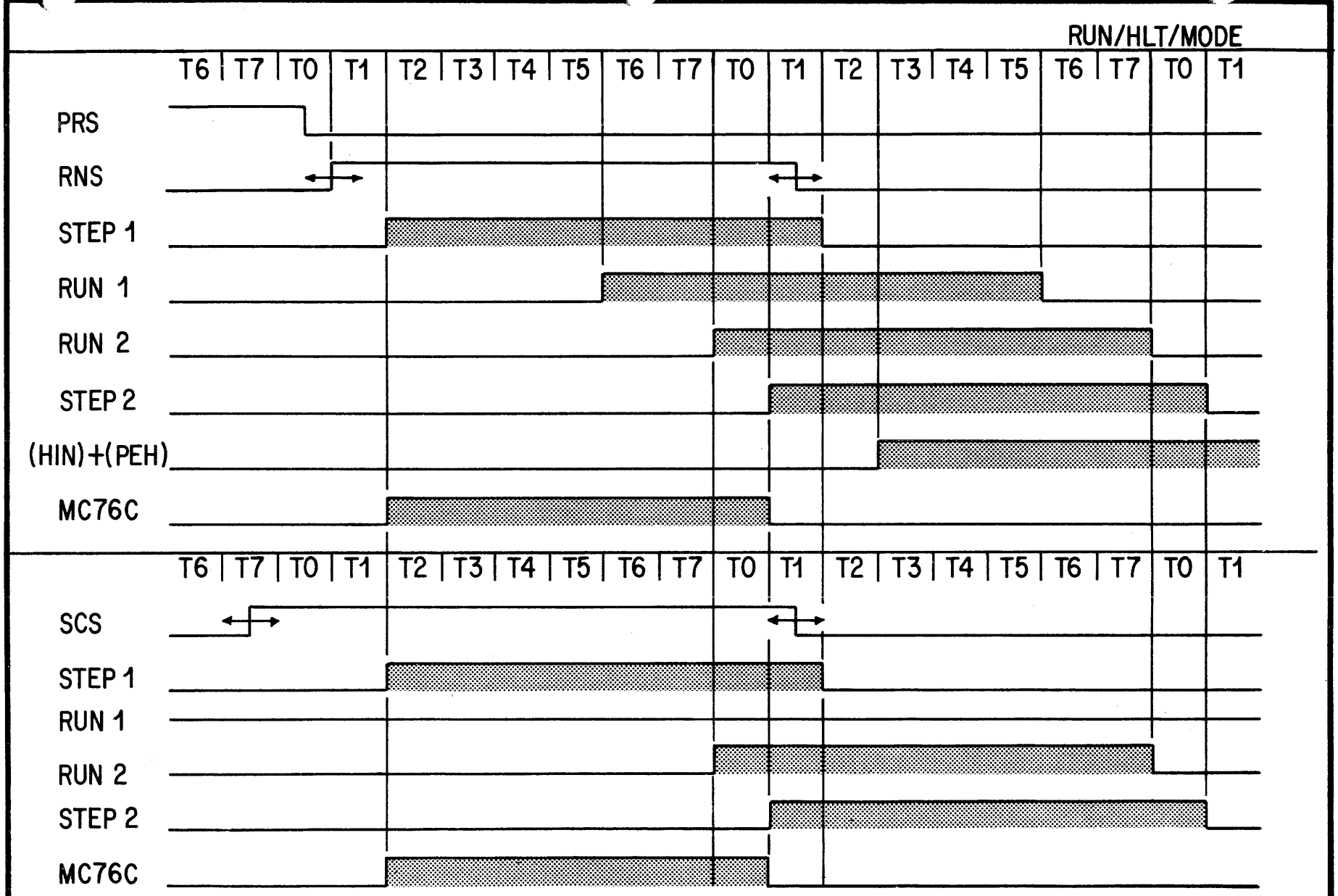
(1) The run-halt circuit provides the logic required to start, stop and single cycle the computer.

(2) Assume the computer is in the initialized state. Both Run and Step Flip-Flops are reset. At this point the RUN pushbutton



RUN / HALT / STEP CIRCUITS

FIG. 2-7



RUN/HALT/SINGLE CYCLE TIMING

FIG. 2-8

is depressed. The RNS signal being true will set Step 1 Flip-Flop MC94A at time T2. At time T5, Run 1 Flip-Flop MC84 sets. This action removes the true level from the "K" input of Run 2 Flip-Flop, and at T7S Run 2 Flip-Flops sets. At T1 time, Step 2 Flip-Flop MC94B sets; this inhibits the true output of gate MC76C and removes the true signal from the "J" input of Run 1 Flip-Flop MC84. Step 1 Flip-Flop will reset at T2 after the RNS signal goes false. The only logical halt path for the computer now is by resetting Run 1 Flip-Flop MC84. The Halt instruction or parity error (PEH), will cause Run 1 Flip-Flop to reset at T5. The HALT pushbutton uses the direct clear input to reset Run 1 Flip-Flop. Run 2 Flip-Flop resets at the next T7S after Run 1 Flip-Flop is reset. Run 2 Flip-Flop actually causes the computer to halt.

b. Single Cycle Mode

(1) The Single Cycle mode allows the computer to execute programs under manual control. Each time the SINGLE CYCLE switch (SCS) is depressed, one and only one, Phase 1, 2, or 3 operation will be completed. When SCS is true, Step 1 Flip-Flop will be set on the next T2. When Step 1 is set, gate MC76C is enabled which provides a true level to the "J" input of Run 2 Flip-Flop. At T7TS, Run 2 Flip-Flop will set. At T1, Step 2 Flip-Flop will set which inhibits gate MC76C, thus removing the true "J" input from the Run 2 Flip-Flop. Since the Run 1 Flip-Flop was never set, the "K" input to Run 2 Flip-Flop is true, and at T7TS the Run 2 Flip-Flop will reset. Step 1 Flip-Flop will stay set until the SINGLE CYCLE button is released. The T2 signal following SCS going false will cause the Step 1 Flip-Flop to reset. The T1 signal following this will cause the Step 2 Flip-Flop to reset. Single Cycle operation is only possible when the computer is in the Halt mode. No Phase 4 operations (Interrupt) can occur.

6. Control Switch Logic (Figure 2-9)

a. Power Turn On

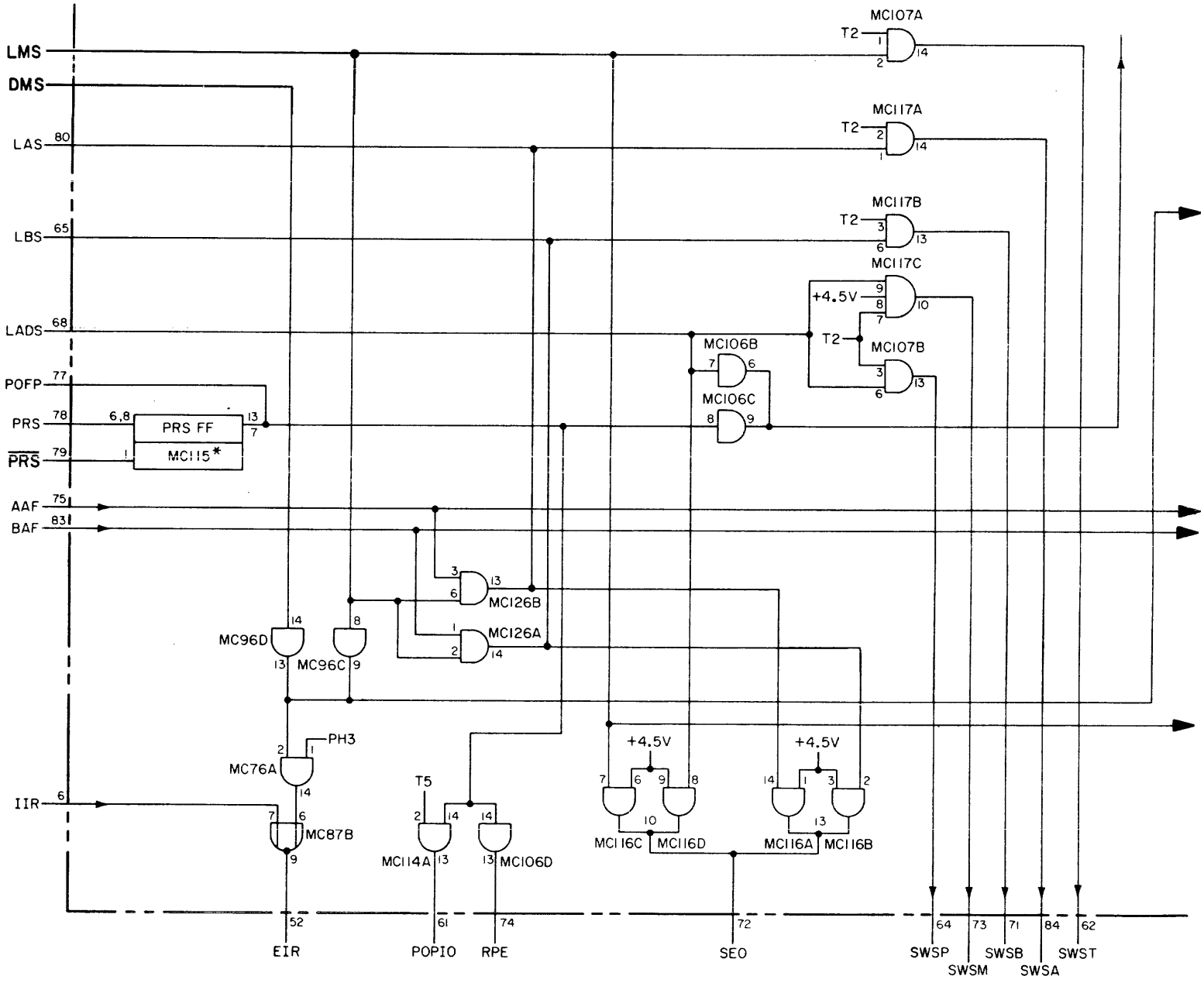
(1) At turn on time, signal POFP will be true for 200 to 500 milliseconds. This signal forces the "1" side of flip-flops MC115 to the true state but does not actually set the flip-flop. At the expiration of POFP, MC115 returns to the reset condition. Pressing the PRESET pushbutton holds the PRS signal high and releasing it enables level $\overline{\text{PRS}}$. These signals set and reset MC115 respectively. When the PRS Flip-Flop MC115 is set, signals POPIO (T5) and RPE are generated. POPIO is the initializing pulse for the I/O section and RPE will reset any parity error indication if the option is available. The true set side of flip-flop MC115 will reset the RUN 1 Flip-Flop MC84 at T5, and using the direct clear input, will reset RUN 2 Flip-Flop MC74. MC115 being true, also forces the computer to Fetch (Phase 1) at T7S.

b. Load A, B and Address

(1) Switch circuits LAS, LBS, and LADS operate when the LOAD A, LOAD B, or LOAD ADDRESS controls are enabled. When the switch is depressed, the debounce flip-flop sets and the SEO (Switch Exclusive OR) comes up and enables the Exclusive OR function and the appropriate Store function. The SEO signal also enables the Switch register circuits and brings up IOBI to transfer the Switch register data onto the "S" bus. This circuitry is on the Instruction Decoder and Shift Logic boards. The signal SWS means Store Switch Register into P, M, B, A, or T.

c. Load Memory and Display Memory

(1) The switch circuits for Load Memory work as described above to transfer the data from the Switch Register into the T register; but in addition, when performing a Load Memory or Display Memory operation, a single Phase 3 cycle is forced



CONTROL SWITCH LOGIC

FIG 2-9

by the switch logic. If Load Memory, the Step 1 Flip-Flop MC94A is set. This ensures a single cycle operation will be completed. The LMS signal will also set Phase 3 and inhibit MST (Memory Strobe Timing). The operation of LMS follows this sequence: a single Phase 3 cycle begins at TØ. At TØ the T-Register is cleared and memory read time starts. At T2 MST is inhibited and the data from the switches is stored into Register "T" using the "S" bus, the Exclusive OR circuits, and the Store "T" bus into T-Register control function. Once the data is in the T-Register, a normal memory write operation proceeds. Since the computer is completing a Phase 3 cycle at T6T7, the P and M Registers are incremented by one. The DISPLAY MEMORY switch simply forces the computer to do a normal Phase 3 memory read/write cycle which results in the contents of the addressed location being displayed in register "T". The P and M registers are incremented by one as above.

7. Review

(1) What frequency is used as the basic clock in the HP 2116B? In the HP 2115A?

(2) What is the duration of pulse TS? How long is it delayed?

(3) What is the purpose of having two dividers to generate a 5 MHz (4. 0 MHz) clock from a 10 MHz (8 MHz) oscillator frequency?

(4) What is the time period of each timing pulse (TØ-T7) in the HP 2116B? In the HP 2115A?

(5) Why are two adjacent Time Period Generator flip-flops set simultaneously?

(6) How long is an extended (ISZ) machine cycle in the HP 2116B? In the HP 2115A?

(7) How long are memory "read" timing pulses in the HP 2116B? In the HP 2115A?

(8) What mnemonic is used for memory read timing signals?

(9) What mnemonic is used for memory write timing signals?

(10) How long are memory "write" timing pulses in the HP 2116B? In the HP 2115A?

(11) What is the MST (Memory Strobe Timing) signal used for?

(12) When is the only time that the MWL signal is used?

(13) How are "phase" changes enabled?

(14) How many machine phases may be enabled at any given time?

(15) What is the purpose of the Run-Halt circuit?

(16) What does the POFP signal do?

(17) What does the POPIO signal do?

(18) What does the RPE signal do?

(19) Why must the PRESET pushbutton be depressed after every computer turn on?

(20) What signal must always be present to transfer Switch Register data to the five main working registers?

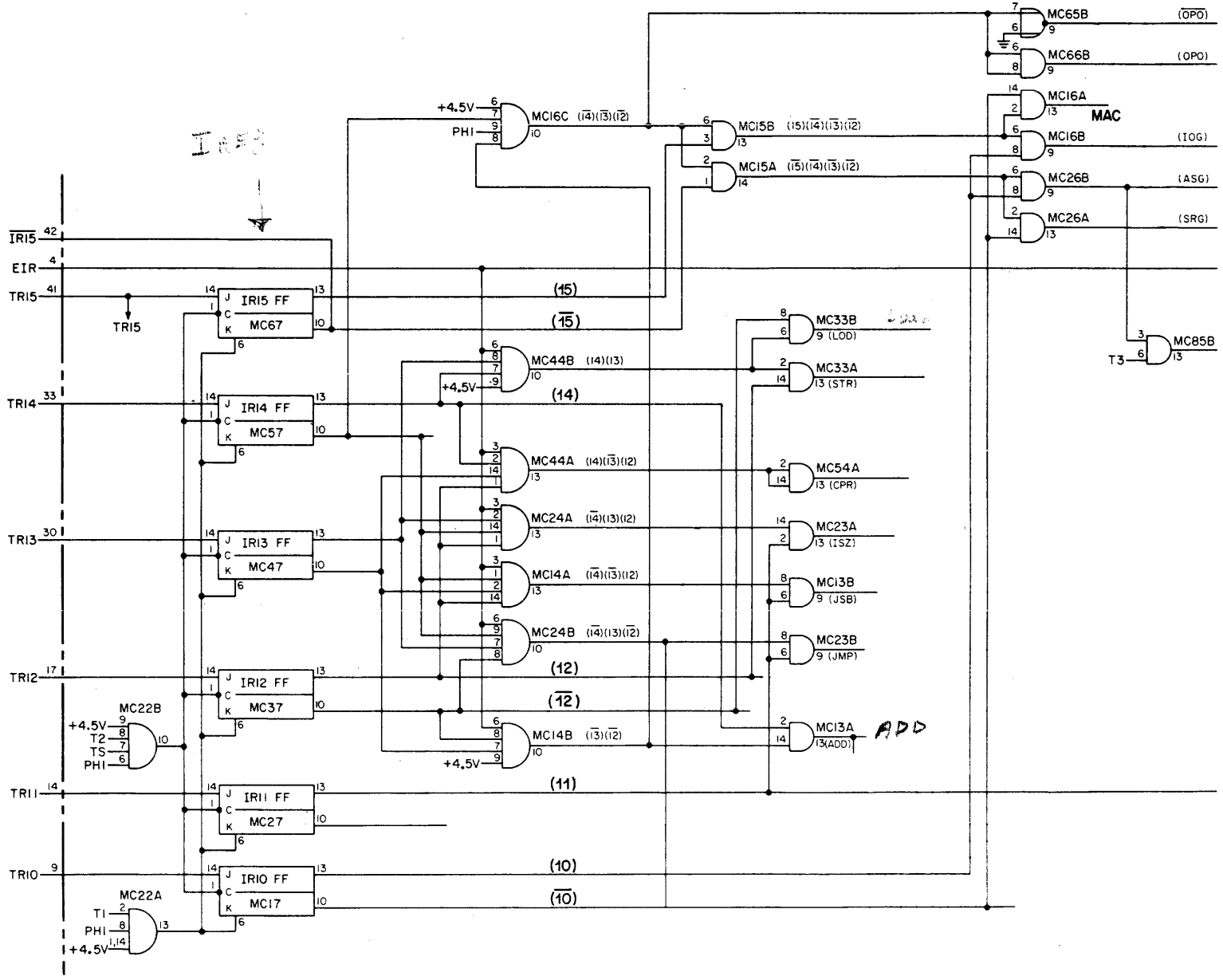
C. INSTRUCTION DECODER

1. Instruction Group Decoding (Figure 2-10)

a. Memory Reference and Group Decoding

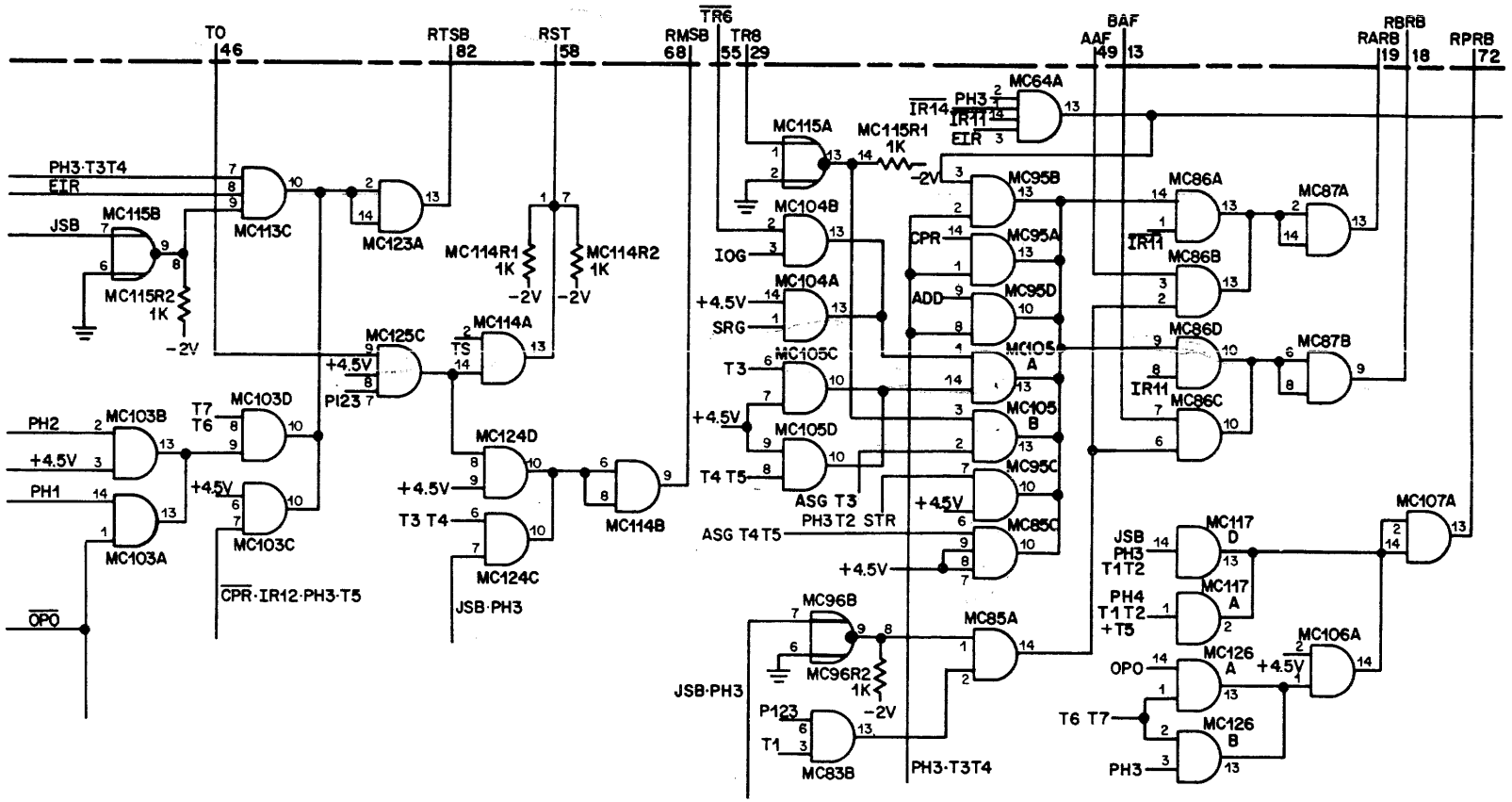
(1) Most instruction execution follows a simple pattern: decode instruction, enable Read function, enable Arithmetic function, and enable Store function. The required control functions, timing signals, and phase signals are generated on the System Timing Generator board.

(2) The computer Instruction Register is made up of six J-K flip-flops numbered IR15 through IR10. The "J" inputs are connected directly to the "1" side output of T-Register Flip-Flops T15 through T10. The "K" inputs are not used. At Phase 1 and time T1, the I-Register is cleared using the direct clear inputs. At Phase 1 and time T2, a clock pulse is supplied to



MEMORY REFERENCE AND GROUP DECODING

FIG. 2-10



READ CIRCUIT

FIG. 2-11

all I-Register Flip-Flops. If the "J" input to a flip-flop was true, that flip-flop will be set. If the "J" input was false, that flip-flop will remain reset. The output of the I-Register is decoded by a network consisting of 20 AND gates. If the instruction is not a Memory Reference type, it falls into one of four "single phase" instruction groups; ASG, SRG, IOG or MAC. The discrete single phase instruction decoding is performed on the Shift Logic board. Any single phase instruction brings up OPO which means One Phase Operation.

2. Read Logic (Figure 2-11)

a. RTSB

(1) The circuits for resetting the T-Register (RST) at TØ are located in the Read area on the Instruction Decoder schematic. At TØ, and every Phase 1, 2, or 3, the T-Register is cleared using RST as the input to the direct clear side of the T-Register.

(2) The Read "T" onto "S" bus signal is enabled during Phase 3 at T3T4 for every memory reference instruction except JSB. Gates MC113C and MC123A provide this capability with gate MC115B connected to inhibit RTSB during JSB Phase 3. Gate MC103D, combined with MC103B and MC103A, provides the ability to bring up RTSB for Phase 1 and Phase 2 memory reference instructions. In both cases, at T6T7 a transfer from register "T" to register "M" is made via the "S" bus. The last enabling input to the RTSB circuit is during addressable A or B Register operations for STA, STB, JSB, ISZ. During the execute phase of these instructions, the data in register "T" must be transferred via the "S" bus onto the "T" bus and then stored in the appropriate register. Gate MC103C provides this capability at Phase 3, T5, $\overline{\text{CPR}}$ and IR12. Notice that this gate is enabled for AND or IOR as well as STA, STB, JSB, and ISZ. In the case of AND or IOR, the data in the appropriate A

or B Register is rewritten when using addressable A or B. This causes no harm and saves one or more gates that would otherwise be needed to exclude AND or IOR instructions.

b. RMSB

(1) The Read "M" onto "S" bus signal is enabled by gate MC125C at TØ to Phase 1, 2, or 3 in order to determine if register "M" is addressing register A or B. This decision must be made early in the machine cycle to set the Addressable A or B Flip-Flops in time to inhibit MST (Memory Strobe Timing), and transfer the addressed register data to the T-Register. The other occasion that RMSB is enabled is during Phase 3 and T3T4 of a JSB instruction, when a data transfer from register "M" to register "P" must be made. Gate MC124C provides this function.

c. RARB

(1) The Read "A" onto "R" bus signal has many enabling functions. The purpose of each gate will be discussed briefly. The inputs to gate MC64A are $\overline{IR14}$, $\overline{IR11}$, Phase 3 and EIR. This circuit enables RARB for the logical instructions and is gated with T3T4, using gate MC95B. MC86A ensures selection of the A-Register only during logical operations.

(2) Gates MC105C and MC105D provide an enabling input to gate MC105A at T3 and T4T5. The other input to MC105A comes from gate MC104A or MC104B. Gate MC104A enables RARB for all SRG instructions, and gate MC 104B enables RARB for OTA instructions. Gate MC95A enables RARB for CPA instructions. Gate MC95D enables RARB for the ADA instruction. Gate MC105B enables RARB for ASG instructions that are enabled at T3. These latter instructions are CLA, CMA, and CCA. Gate MC115A inhibits gate MC105B when TR8 is true. The end result of all this is to enable RARB only when doing a CMA operation or when no operation with "A" is programmed. RARB is inhibited when doing CLA or CCA operations. Gate

MC95C enables RARB during Phase 3 and T2 when doing a STA operation. Gate MC85C enables RARB for all ASG instructions at T4T5. Gates MC96B, MC85A, MC83B, MC86B and MC86C provide RARB or RBRB at T1 of Phase 1, 2, or 3 when doing any addressable A or B Register operation. The exception to this is JSB; MC96B is connected to inhibit the appropriate RARB or RBRB signal. Gates MC86A and MC86D select RARB or RBRB depending onthe status of bit IR11. The A-Register instructions were used in this text to simplify circuit descriptions. These descriptions hold for B-Register instructions as well with slight modifications.

d. RPRB

(1) The Read "P" onto "R" bus signal is enabled during Phase 3 and T1T2 of a JSB (Increment P) instruction by gate MC117D, and at Phase 4 (Decrement P) and T1T2 or T5 by gate MC117A. RPRB is also enabled at T6T7 for OPO operations, or at T6T7 of Phase 3 for multiphase instructions by gates MC126A, MC126B and MC106A. This is required to increment "P" at the completion of each instruction.

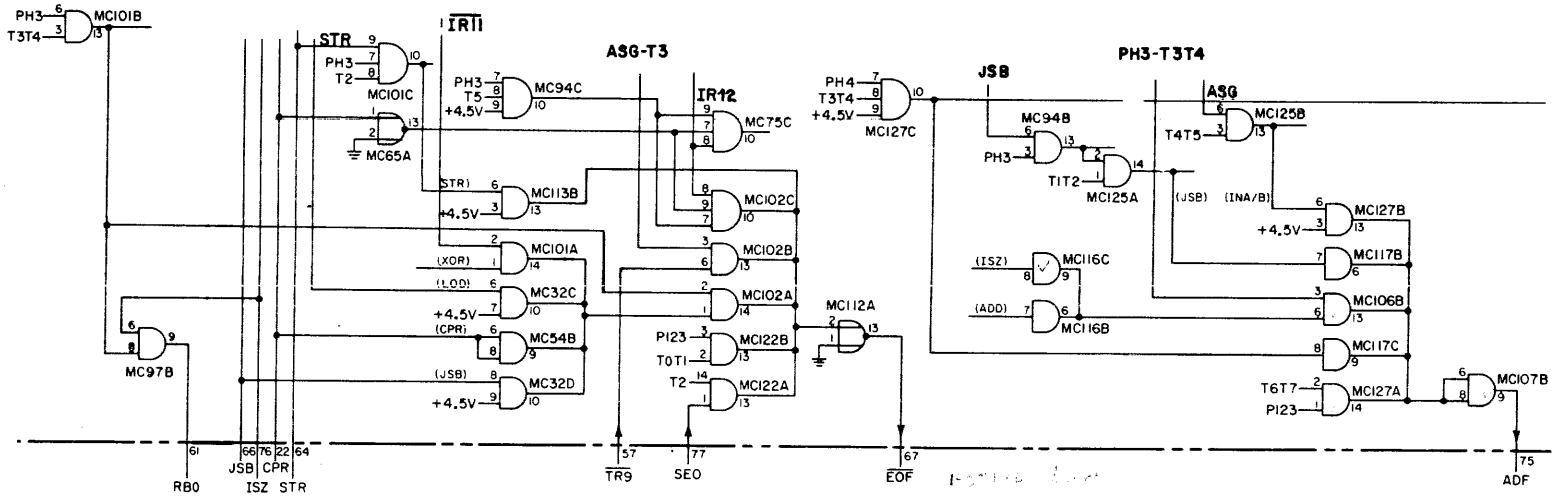
3. Function (Arithmetic) Logic (Figures 2-12 and 2-13)

a. RBØ

(1) The "R bus Zero" function provides a "1" on the "R" bus during Phase 3 and T3T4 of ISZ instructions only. Since the T-Register is connected to the "S" bus, "S bus Ø" cannot be used to increment the T-Register. Gates MC101B and MC97B provide the RBØ function.

b. EOF

(1) The "Exclusive OR Function" enabling inputs are best shown gate by gate. Gates MC101C, MC113B, and MC112A enable $\overline{\text{EOF}}$ for Phase 3, T2, and STR (Store) instructions. Gates MC94C, MC65A and MC102C enable $\overline{\text{EOF}}$ at Phase 3 and T5 for AND, IOR, STA, JSB, ISZ, and STB. This signal is provided



ARITHMETIC FUNCTIONS RBØ, EOF, ADF

FIG. 2-12

to route data fromthe T-Register and "S" bus to the A or B Register when performing the above instructions utilizing the addressable A or B feature. Remember - instead of writing "memory" we must now write A or B. Gates MC101A, MC101B, MC102A and MC112A enable EOF at Phase 3, T3T4, and XOR. Gates MC32C, MC101B, MC102A and MC112A enable EOF at Phase 3, T3T4, and LOD (Load Instruction). Gates MC54B, MC101B, MC102A and MC112A enable EOF at Phase 3, T3T4, and CPR (Compare Instruction). Gates MC32D, MC101B, MC102A and MC112A enable EOF at Phase 3, T3T4 and JSB (Jump Subroutine instruction). Gate MC102B enables EOF during T3, ASG, and TR9. This isolates the instruction to CLA or CLB.

(2) Gate MC122B enables EOF during Phase 1, 2 or 3 at TØT1. This enables data from register "M" to pass via the "S" bus to the "T" bus for decoding addressable A or B functions.

(3) Gate MC122A enables EOF at T2 whenever the manual switches are used to load data from the Switch Register. Data flow is from the switches to the "S" bus and through the enabled Exclusive OR circuits to the "T" bus (to be stored in the appropriate register).

c. ADF

(1) The "Add function" circuits are best shown gate by gate. Gates MC125B and MC127B enable the ADF every T4T5 of any ASG instruction. Gates MC94B, MC125A and MC117B enable the ADF during Phase 3 and T1T2 of a JSB (Jump Subroutine instruction). Gates MC116C, MC116B and MC106B combine to enable the ADF at Phase 3 and T3T4 of ADD or ISZ instructions. Gates MC127C and MC117C enable ADF during Phase 4 and T3T4 (Interrupt).

(2) Gate MC127A enables ADF during Phase 1, 2, or 3 operations at T6T7. This gate enables the Adder for incrementing registers "P" and "M" during Phase 1 for OPO instructions, and all Phase 3 operations. The ADF is used only to transfer data

from the "S" bus to the "T" bus during Phase 1 of multiphase instructions, and during all Phase 2 operations.

d. CMF

(1) The CMF function is enabled by gates MC72A and MC82B during ASG, T3, and TR9. This is for the instructions CMA/B and CCA/B. The other enabling gates for CMF are MC72C, MC72D, MC72B, and MC62B. These circuits enable CMF during Phase 4 (Interrupt) at T1T2 and again at T5. This function is used to decrement register "P".

e. IOF

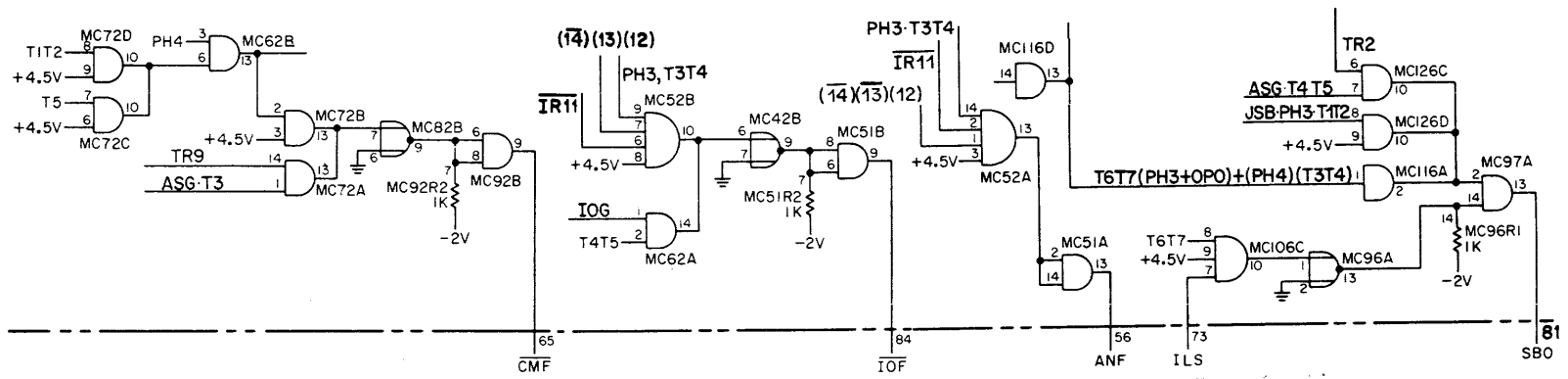
(1) The IOF function is enabled during Phase 3 and T3T4 of the IOR (Inclusive OR) instruction. The enabling gate is MC52B which drives MC42B. The other enabling input for IOF is gate MC62A which becomes true for all IOG instructions at T4T5.

f. ANF

(1) The ANF function is true only during Phase 3 and T3T4 of the AND instruction. The enabling gate is MC52A.

g. SBØ

(1) The "S Bus Zero" function provides a "1" level to "S" bus Ø. The function is used to increment any register normally connected to the "R" bus. These registers are A, B, and P. Gate MC126C enables SBØ during ASG and T4T5 for INA/B instructions. Gate MC126D is enabled during Phase 3 and T1T2 of a JSB (Jump Subroutine instruction). This enables the incrementing of register "P". Gates MC126A or B and MC116A enable SBØ during Phase 3, or OPO (One Phase Operation), and T6T7. This circuitry allows the incrementing of register "P" at the completion of each instruction. Gate MC116D is also enabled during Phase 4 and T3T4. This enables SBØ during the Interrupt phase, and allows the decrementing of register "P" by 1. (Complement, Increment, and Complement yeilds P-1). Gates MC106C and MC96A are connected to MC97A in an inhibiting



ARITHMETIC FUNCTIONS CMF, IOF, ANF, SBO

FIG.2 -13

configuration. Signal ILS (Instruction Loop Switch) is normally "0" so gate MC106C provides a false input to MC96A which then enables gate MC97A. If the ILS switch is placed in the LOOP position, the P-Register is not incremented. The current instruction will be executed repeatedly until the switch is returned to normal. The exceptional case is a Skip type instruction which may cause "P" to be incremented by another method, and cause the next sequential instruction to be executed.

4. Store Logic (Figures 2-14 and 2-15)

   a. STBA

      (1) The "Store T bus in A or B" function must be enabled in order to change the contents or status of registers A or B. Since the A-Register is the primary accumulator, a great many inputs to the STBA function exist. The function of each gate is described below:

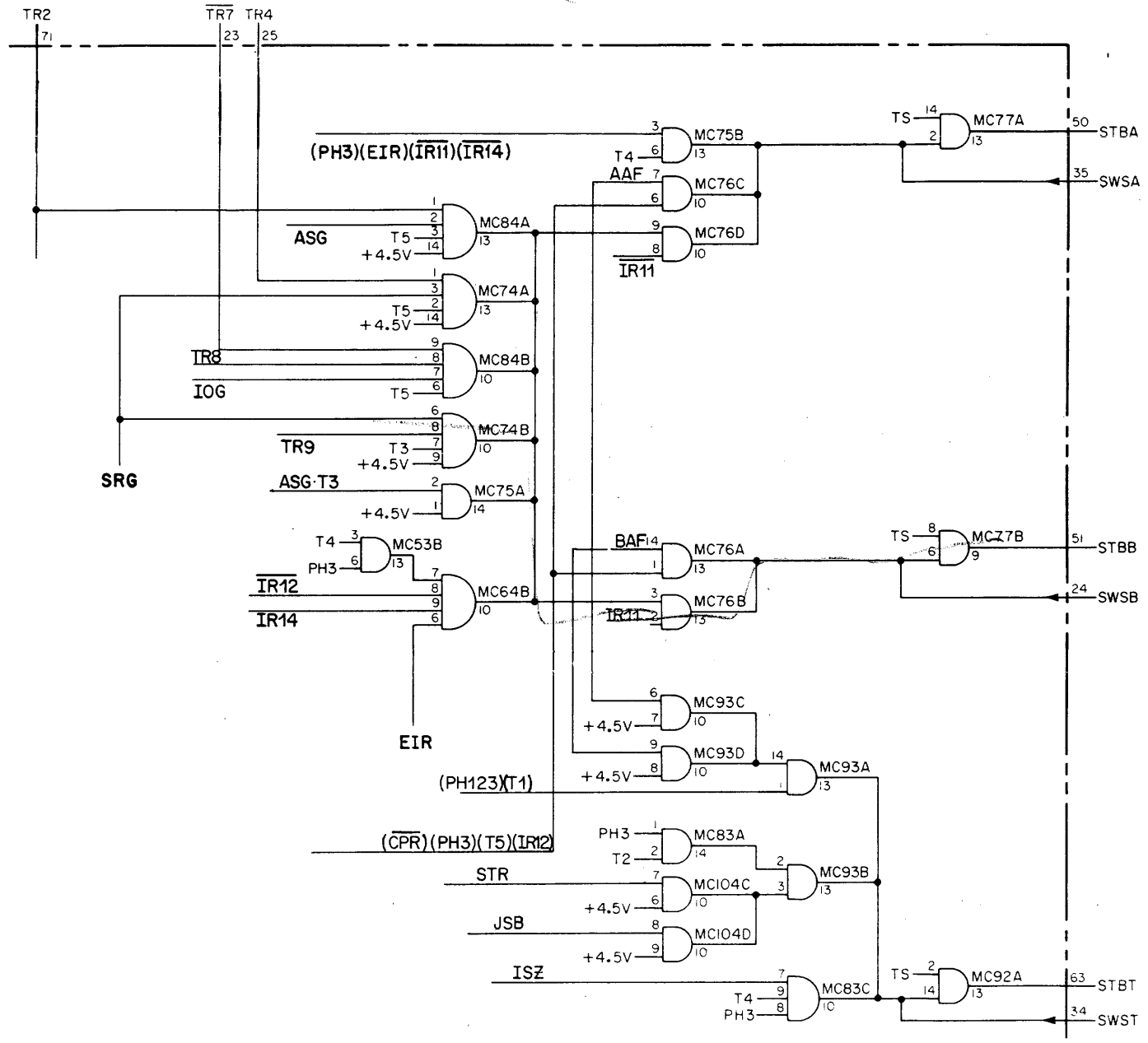
         (a) MC77A. This is the circuit that gates the enabling signal with TS. Signal SWSA (Switch Store A) is enabled by pushing the LOAD A pushbutton on the front panel.

         (b) MC75B is enabled during Phase 3 and T4 for the logical instructions AND, IOR, and XOR.

         (c) MC76C is enabled during addressable A-Register memory reference instructions STA, STB, ISZ, JSB, IOR, and AND during Phase 3 and T5. This signal is required to write new data into register "A" when addressed as memory. This signal is not required for IOR or AND instructions; but causes no harm if enabled at this time.

         (d) MC76D gates the enabling signal with $\overline{IR11}$. This ensures that register "A" is the selected register. With the exception of the logical instructions, this gate determines whether STBA or STBB is enabled.

         (e) MC84A is enabled at T5 for Increment instructions (INA/B).



STORE FUNCTIONS A, B, T, REGISTERS

FIG. 2-14

(f) MC74A is enabled for all SRG instructions at T5 if the Disable/Enable bit (TR4) is true. This provides STBA/B for Shift and Rotate instructions that occur in the last half of the machine cycle.

(g) MC84B is enabled for IOG (Input/Output group) instructions LIA/B and MIA/B at T5.

(h) MC74B is enabled for all SRG instructions at T3 if the Disable/Enable bit (TR9) is true. This provides STBA/B for Shift and Rotate instructions that occur in the first half of the machine cycle.

(i) MC75A is enabled for all ASG (Alter Skip Group) instructions at T3.

(j) MC64B (with inputs supplied by MC53B) is enabled for ADA/B and LDA/B instructions during phase 3 at T4.

(k) MC76B gates the enabling signal with IR11. This ensures that register "B" is the selected register.

(l) MC76A performs the same function as MC76C (step c above) when an addressable "B" operation is in progress.

b. STBT

(1) The "Store T bus in T-Register" function must be enabled to change the status of the T-Register via "T" bus inputs. Memory data uses the direct set input to the T-Register flip-flops so memory read does not require STBT.

(a) MC92A gates the enabling signal with TS to produce STBT.

(b) MC93C and MC93D enable STBT during Phase 1, 2, or 3 at T1 whenever the A or B-Registers have been addressed as memory. The data from register A or B must be transferred via the "R bus and the "Exclusive OR" circuits, and then be stored in the T-Register as if it were actually read from memory.

(c) MC83A, MC93B, MC104C, and MC104D enable STBT during Phase 3 and T2 of STA/B and JSB instructions.

(d) MC83C enables STBT during Phase 3 and T4 of an ISZ (Increment and Skip on Zero) instruction.

c. STM

(1) Gate MC66A provides the enabling signal with TS to produce STM (12-15) and STM (10-11), hereinafter called STM (10-15). The SWSM (Switch Store M) signal is enabled by depressing the LOAD ADDRESS pushbutton on the front panel.

(a) MC53A gates the enabling signal with T7. Whenever the output line of MC53A is true, then MC55B is true which enables MC56B and produces STM (6-9). Whenever the output line of MC43A is true, then MC55C is enabled which enables MC56A and produces STM (0-5). Whenever STM (10-15) is true, then STM (6-9) will be true; and whenever STM (6-9) is true, then STM (0-5) will also be true. STM (10-15), STM (6-9) and STM (0-5) will store all 16 "T" bus bits into register "M".

(b) MC63C enables STM (0-15) for OPO (One Phase Operations). This circuit allows P + 1 (on the "T" bus) to be stored in register "M".

(c) MC63D enables STM (0-15) for Phase 2 (Indirect) operations. This circuit allows "T" bus data (address information) to be stored in register "M".

(d) MC63B enables STM (0-15) for Phase 3 operation. This circuit allows P + 1 (on the "T" bus) to be stored in register "M". Gates MC63C, D, and B are all gated with T7 using gate MC53A.

(e) MC43A enables STM (0-9) for Phase 1 of memory reference instructions at T7. This circuit allows the transfer of bits 0-9 (word address) of register "T" to be transferred to register "M" in preparation for Phase 2 or Phase 3.

(f) MC45A enables STM (0-5) during Phase 4 (Interrupt) T7. This action allows the storage of "T" bus data (in this case the interrupting device select code) into register "M". Gates MC46B, MC55A and MC46A are enabled at the same time. These gates enable RSM (Reset M 6-9 and 10-15). RSM is applied to the direct clear input of the M-Register flip-flops. Resetting the high order bits of "M", at the same time the select code data is stored into register "M" (0-5), ensures a memory access to one of the Interrupt locations.

(g) MC45B enables the direct reset of bits 10-15 of register "M" during Phase 1 and T7 of memory reference instructions. This circuit is enabled by any Page Zero memory access.

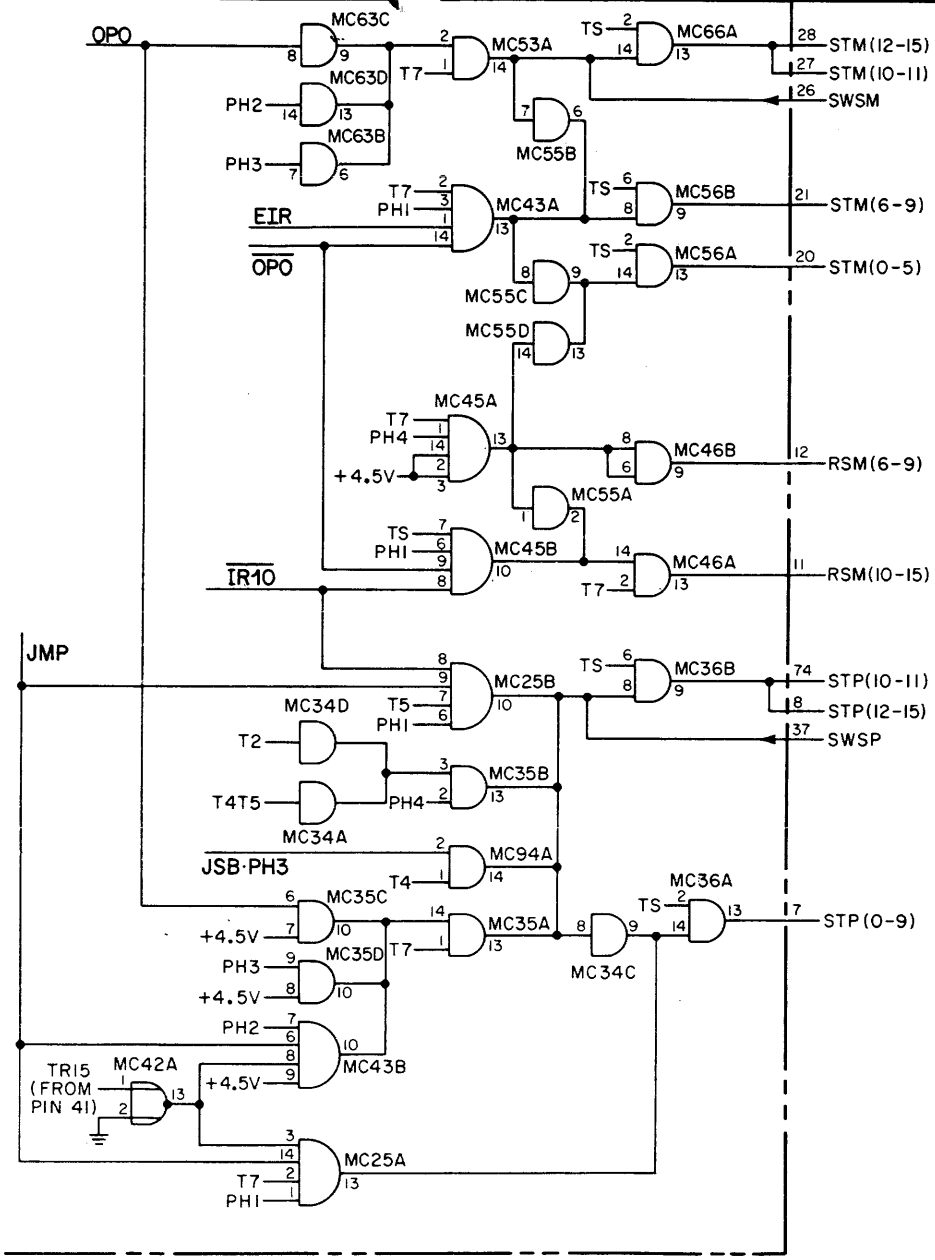
d. STP

(1) MC36B gates the enabling signal with TS to provide clean triggering for the P-Register flip-flops. SWSP (Switch Store P) enables STP (0-15) when the LOAD ADDRESS pushbutton is depressed.

(a) MC25B enables STP (0-15) at T5 of a Page Zero JMP instruction. Since no arithmetic or logic function is enabled at T5, the effect of this gate is to clear the P-Register bits 0-15.

(b) Gates MC34D, MC34A, and MC35B enable STP (0-15) during Phase 4 operations at time periods T2 and T4T5. This operation permits the decrementing of register "P" during Interrupt (Phase 4).

(c) MC94A enables STP (0-15) during Phase 3 and T4 of a JSB (Jump Subroutine) instruction. This circuit allows the transfer of data from register "M" to register "P", before "P" and "M" are incremented at T6T7.



STORE FUNCTIONS "P" and "M" REGISTER

FIG. 2 -15

(d) Gates MC35C, MC35D, MC35A and MC34C ensures that P + 1 ("T" bus data) is stored in register "P" (0-15) at T7 of any one phase or multiphase instruction.

(e) MC42A, MC43B and MC35A allow "T" bus data to be stored in register "P" for JMP, Phase 2 and T7. A jump indirect instruction allows a Phase 2 to be followed by a Phase 1. In case of a multilevel indirect, the P-Register remains constant until an address with bit 15 = Ø is found. Thus, the last indirect address contains the effective address of the indirect Jump.

(f) MC25A enables STP (0-9) for Phase 1 of a direct Jump instruction at T7. This allows "T" bus data to be stored in register "P". Notice that only STP (0-9) is enabled. This action restricts transfers to the Current page or Zero page only.

5. Review

(1) What is the "execution" pattern for most instructions?

(2) What is the purpose of the Instruction Decoder board?

(3) Where are the discrete single-phase instructions decoded?

(4) What signal is required to reset the T-Register? What time is "T" reset?

(5) When is RTSB enabled?

(6) When is RMSB enabled?

(7) What is the primary purpose of the RARB function?

(8) What are the three purposes for having the RPRB control function?

(9) Why is the RBØ control function required? When is it used?

(10) What is the primary purpose of the SBØ control function?

(11) What happens to the P-Register if the INSTRUCTION LOOP switch is placed in LOOP, and the current instruction is a skip type instruction?

(12) What control function enables T Register bits 10 through 15 to set bits 10 through 15 of the I Register?

(13) How is theSWSM (Switch Store M) control function enabled?

(14) How is the SWSP (Switch Store P) control function enabled?

(15) How is the P-Register cleared for a page zero JMP instruction?

D. SHIFT-ROTATE LOGIC

1. Single Phase (OPO) Instruction Decoding (Figure 2-16)

a. Halt Instruction

(1) Since it is impossible to have SRG and IOG enabled at the same time, a considerable saving of gates is realized by sharing the decoding circuits for bits TR8, TR7, and TR6 between these two groups. The Halt instruction is decoded completely as follows:

(a) The IOG function enables MC35A. If Halt, then we have $(\overline{TR8})$ $(\overline{TR7})$ $(\overline{TR6})$. This condition enables gates MC67B, MC57B and MC47B which in turn enable MC47C. This enables MC43A and produces HIN (Halt Instruction Normal). The same procedure is used to decode all SRG, ASG, and IOG instructions. Gates are provided to enable TR8, TR7, and TR6 decoding to occur during SRG at T3 only. By the same token, bits TR2, TR1, TRØ are decoded during SRG at T5 only. This circuitry allows shifts and rotates to be performed twice within a single machine cycle. The instruction decoding process is best explained by referring to the decoding diagrams where ASG, SRG and IOG decoding is shown.

b. I/O Instruction Decoding (Figure 2-17)

(1) The I/O decoding network is shown in Figure 2-17. These

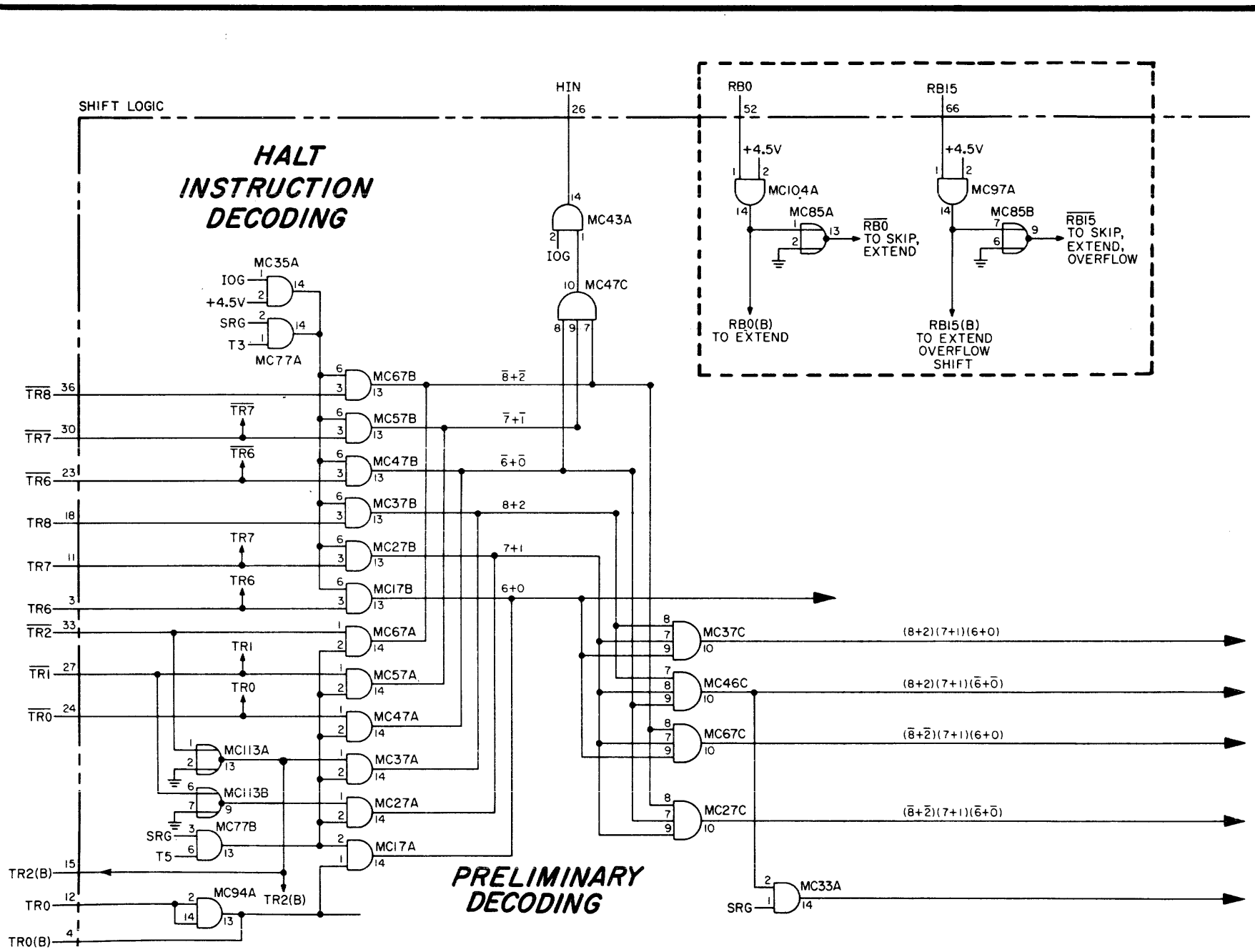
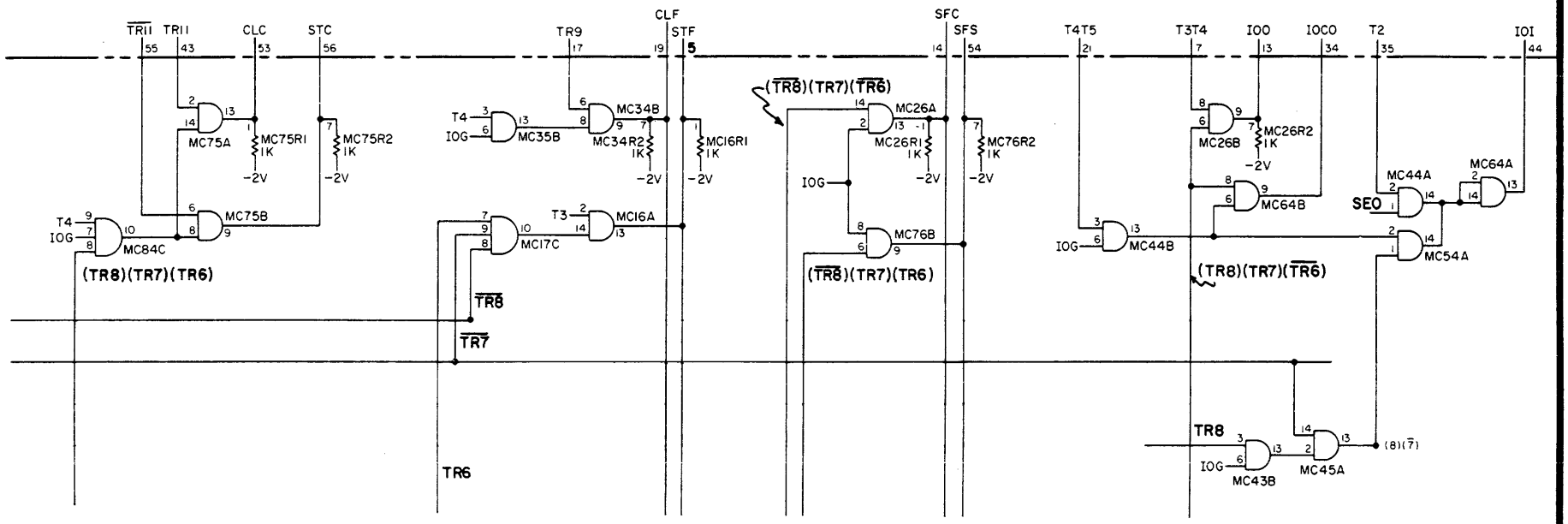

SHIFT LOGIC
HIN
26
HALT INSTRUCTION DECODING
RB0
52
RB15
66
+4.5V
MC104A
MC97A
MC85A
MC85B
RB0 TO SKIP, EXTEND
RB15 TO SKIP, EXTEND, OVERFLOW
RB0(B) TO EXTEND
RB15(B) TO EXTEND OVERFLOW SHIFT
MC43A
IOG
MC47C
MC35A
SRG
T3
MC77A
TR8
TR7
TR6
MC67B
MC57B
MC47B
MC37B
MC27B
MC17B
8+2
7+1
6+0
MC67A
MC57A
MC47A
MC37A
MC27A
MC17A
TR2
TR1
TR0
MC113A
MC113B
MC77B
T5
TR2(B)
MC94A
TR0(B)
MC37C
MC46C
MC67C
MC27C
MC33A
(8+2)(7+1)(6+0)
(8+2)(7+1)(6̄+0̄)
(8̄+2̄)(7+1)(6+0)
(8̄+2̄)(7+1)(6̄+0̄)
PRELIMINARY DECODING

FIG. 2-16



Input/Output Control Instruction Decoding

FIG. 2 – 17

circuits provide the final decoding process for I/O instructions. Gates MC84C and MC75B decode TR8, TR7, TR6, IOG and $\overline{TR11}$ at T4 to produce STC (Set Control). The same signals gated with TR11 (using MC75A) produce CLC (Clear Control).

(a) Gates MC35B and MC34B combine to produce CLF (Clear Flag) at T4 if IOG and TR9 are enabled.

(b) Gates MC17C and MC16A combine to decode $\overline{TR8}$, $\overline{TR7}$, and TR6 to produce STF (Set Flag) at T3.

(c) MC26A gates $\overline{TR8}$, TR7 and $\overline{TR6}$ to produce SFC (Skip if Flag Clear). MC76B gates $\overline{TR8}$, TR7 and TR6 to produce SFS (Skip if Flag set). The SFC, C or SFS, C combined instructions are valid for Select Code Ø1 only. The reason for this restriction is that only the Overflow Flip-Flop is a "J-K" clocked type. The Flag Flip-Flops used on the I/O Interface Boards are not clocked. In most cases, the flip-flop will be cleared before the test, which is in error. Since the Carry Flip-Flop, that produces the skip, triggers on the trailing edge of (T4)(TS); and the selected I/O Flip-Flop starts to reset at the leading edge of T4, the results are marginal and cannot be predicted in all cases.

(2) Gate MC26B will produce IOO (Input Output Out) at T3T4 if TR8, TR7, and $\overline{TR6}$ are enabled. This condition is produced by OTA/B only. Gates MC44B and MC64B produce IOCO (Input Output Control Output) if OTA/B and T4T5 are true. IOO is a signal that is supplied to the I/O section for gating purposes during an output operation. IOCO, on the other hand, is the signal that enables data on the "R" bus to be sent out on the I/O output bus. IOO comes up before IOCO to ensure that the I/O Interface Register is enabled prior to data being placed on the IOBO bus.

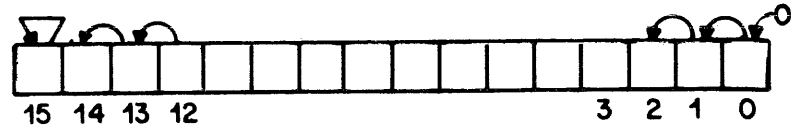
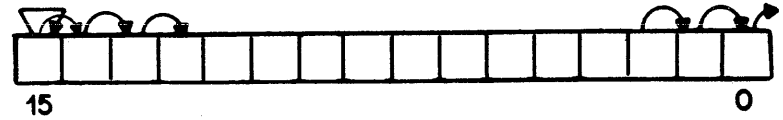
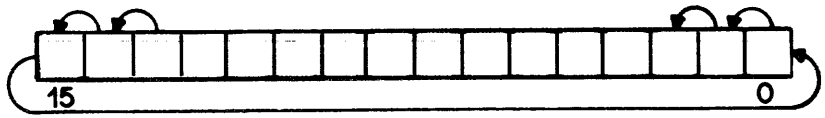
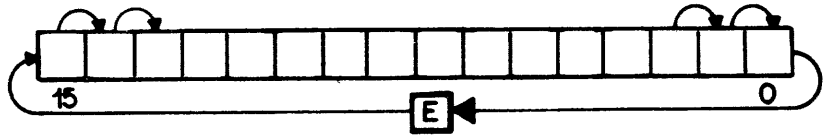
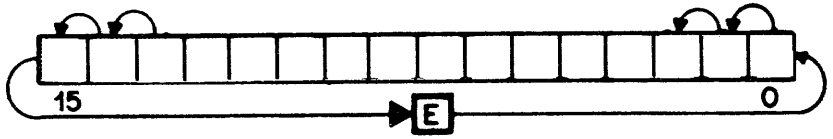
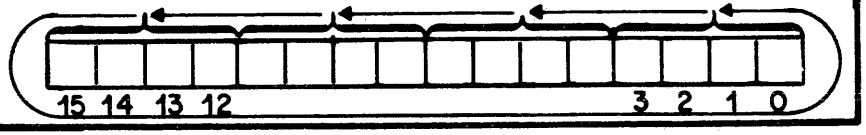
(3) Gates MC43B and MC45A combine to produce a true input to gate MC54A if TR8 and $\overline{TR7}$ are true. Gate MC45A is true for LIA/B and MIA/B instructions. Since MC44B is true at T4T5 for all I/O instructions, gates MC54A and MC64A will

produce IOI (Input Output Input) if MIA/B or LIA/B at T4T5. IOI is supplied to the I/O section for gating purposes and also gates data from the Input/Output Bus Input (IOBI) onto the "S" bus of the computer. Since IOI is true for two time periods (T4T5), there is no need for an IOCI (Input Output Control Input) signal.

(4) Gate MC44A is enabled at T2 and SEO (Switch Exclusive OR). Signal SEO is true whenever the LOAD A or B, LOAD ADDRESS, or LOAD MEMORY switches are used. This circuit brings up IOI which enables data to transfer from the Switch Register to the "S" bus, where it passes through the Exclusive OR circuits and is stored in the selected register.

c. Shift-Rotate Instruction Decoding

(1) The Shift-Rotate Implementation Diagram is shown in Figure 2-18. There are only three basic shift functions: SLM (Shift Left Magnitude), SRM (Shift Right Magnitude) and RL4 (Rotate Left Four). These basic shift functions are modified by three additional shift control functions. These additional functions are required to control specific bits within the total shifting or rotating environment enabled by SRM or SLM. These modifying control functions are: RRS (Rotate Right to Sign Bit), RLL (Rotate Left to Least Significant Bit) and SL14 (Shift Left Bit 14). All shift functions use the inverted output technique; that is, $\overline{SLM} = 0$ means SLM = 1, therefore Shift Left Magnitude is enabled. Remember all shifts and rotates can be performed twice within a single machine cycle. Bits TRØ, TR1 and TR2 control which operation will be performed at T5; and TR6, TR7 and TR8 control the operation to be performed at T3. The actual control is provided by TR4 and TR9 (the Disable/Enable control bits). To explain this further, suppose two ALS operations are to be performed. If TR4 and TR9 are both true, both operations will be performed. If TR4 and $\overline{TR9}$ are true, only the ALS at T5 will take place even though the SLM control

INSTRUCTION	FUNCTIONS	DIAGRAMS
A/BLS	$\overline{SLM}$·RB(0–13) RB15→TB15	
A/BRS	$\overline{SRM}$·RB(1–15) RB15→TB15	
RA/BL	$\overline{SLM}$·RB(0–13) $\overline{SL14}$·RB14 $\overline{RLL}$·RB15	
RA/BR	$\overline{SRM}$·RB(1–15) $\overline{RRS}$·RB0	
ERA/B	$\overline{SRM}$·RB(1–15) E→TB15 RB0→E	
ELA/B	$\overline{SLM}$·RB(0–13) $\overline{SL14}$·RB14 E→TB0 RB15→E	
A/BLF	$\overline{RL4}$·RB(0–15)	

SHIFT-ROTATE IMPLEMENTATION DIAGRAMS

FIG. 2–18

function is enabled at T3 and T5. This is because TR4 and TR9 control the "read" and "store" circuits located on the Instruction Decoder board.

(2) The decoding network is shown in Figure 2-19

(a) Gate MC33C is enabled by SRG and $\overline{TR6}$ or $\overline{TR\emptyset}$. By looking at the SRG decoding diagram, we can see that this includes all shifts and rotates that move left (with the exception of ALF which has a separate control function). Gate MC33C being true inhibits MC16B (through MC55A) and enables $\overline{SLM}$.

(b) Gate MC13A and MC13B will enable $\overline{SRM}$ if TRØ and TR1, "or" TR6 and $\overline{TR7}$, "or" TRØ and $\overline{TR2}$, "or" TR6 and $\overline{TR8}$ are true. This combination, when applied to the decoding chart, shows the SRM signal is enabled for ARS, ERA, and RAR.

(c) Gate MC23C is enabled for TRØ, TR1, and TR2 "or" TR6, TR7 and TR8. This combination inhibits MC45B (through MC36B) thus enabling RL4.

(d) Gate MC53B is enabled if TRØ, TR1, and $\overline{TR2}$ "or" TR6, TR7, and $\overline{TR8}$ are true. The decoding chart shows this gate to be enabled for RAR. MC53B inhibits MC66B which enables $\overline{RRS}$ (Rotate Right to Sign Bit). This function enables the circuits required on the arithmetic logic boards to rotate bit 0 around to bit 15 (Sign) when performing RAR.

(e) Gate MC53A is enabled if $\overline{TR\emptyset}$, TR1 and $\overline{TR2}$ "or" $\overline{TR6}$, TR7 and $\overline{TR8}$ are true. The decoding chart shows this gate to be enabled for RAL. Gate MC53A inhibits MC66A which enables $\overline{RLL}$ (Rotate Left to Least Significiant Bit). This function enables the circuits required on the arithmetic logic boards to rotate bit 15 around to bit 0 when performing RAL. Gate MC33B is also enabled for RAL. This circuit inhibits MC36A which enables $\overline{SL14}$ and allows bit 14

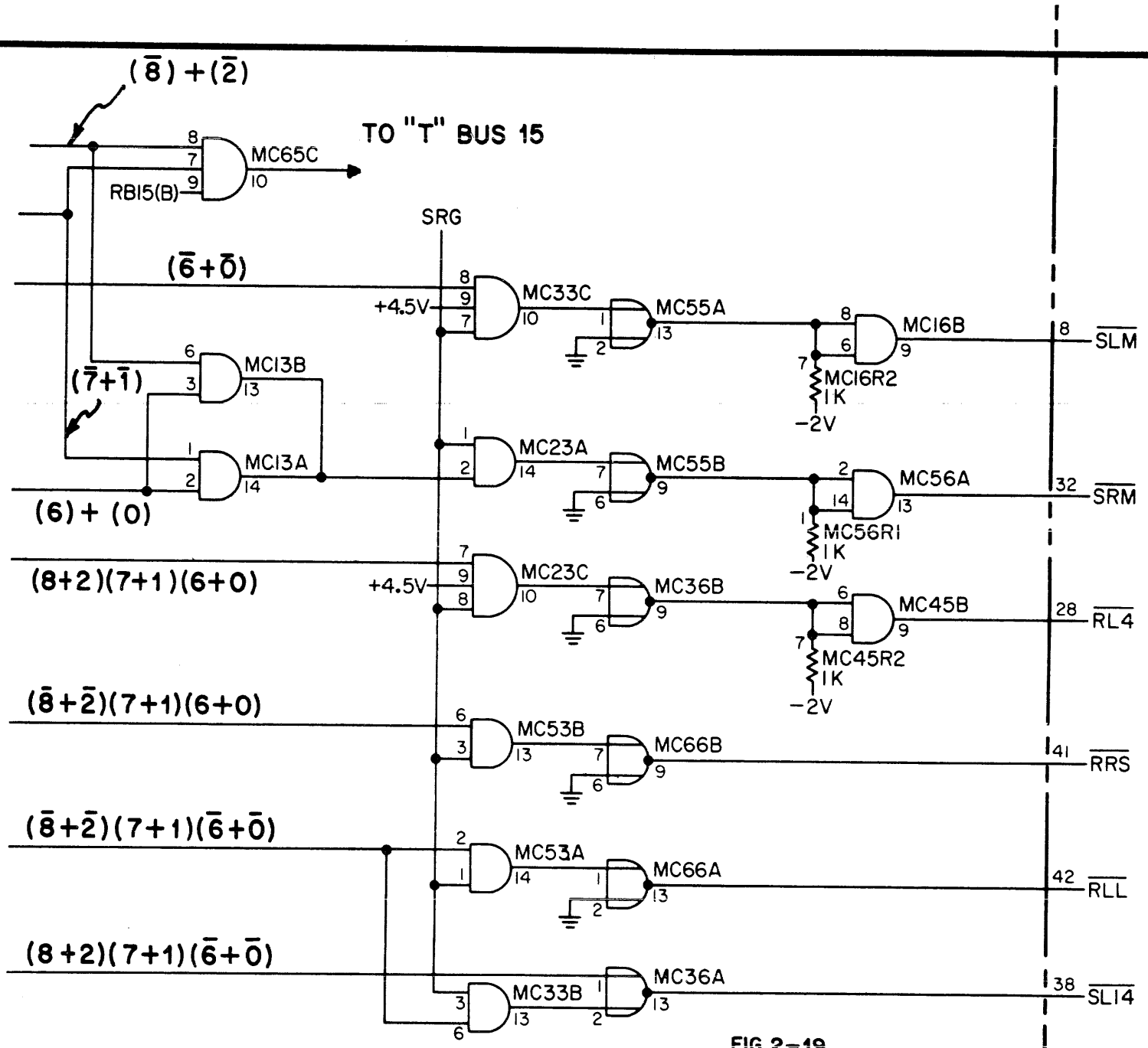


FIG. 2-19

SHIFT FUNCTION DECODING

to be rotated into bit 15. The other input to MC36A is $\overline{TR\emptyset}$, TR1, and TR2 "or" $\overline{TR6}$, TR7 and TR8 which are true for ELA. Since all bits must rotate when performing rotates to the left, $\overline{SL14}$ is always enabled for RAL and ELA.

(f) Gate MC65C is enabled by $\overline{TR2}$ and $\overline{TR1}$ "or" $\overline{TR8}$ and $\overline{TR7}$ and RB15. Decoding these bits shows that this circuit is enabled for ALS and ARS. The output of MC65C is connected to "T" bus 15 so that when doing an arithmetic shift (left or right) the status of bit 15 is enabled onto "T" bus 15 and written back into flip-flop of the A or B-Register.

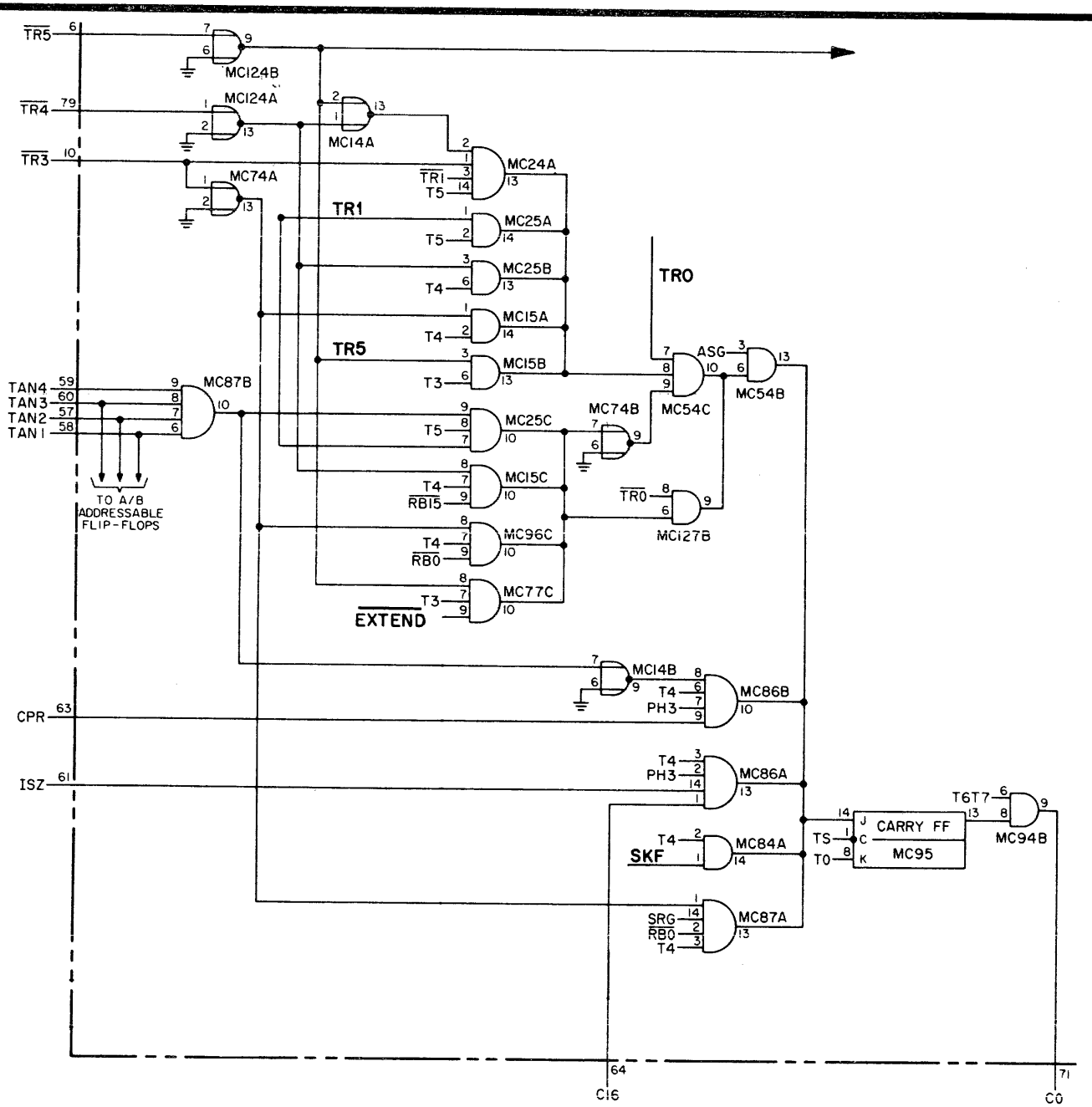
d. Carry Flip-Flop

(1) The purpose of the Carry Flip-Flop is to provide a true level at the carry input of Adder Zero when it is desired to increment the program counter (P-Register) by 2 instead of 1. All skip-type instructions use the Carry Flip-Flop circuit. It is in this way that a logical decision can be made by the programmer. The "1" side output of the Carry Flip-flop is enabled only at T6T7 by gate MC94B. (Time T6T7 is when the P-Register is incremented.) The reset side of the Carry Flip-Flop is connected to TØ and the clock input is TS. The function of all the input gates are described below.

(a) Gate MC86B is enabled if "T" bus (0-15) is <u>not</u> equal to zero, during Phase 3 and T4 of the Compare instruction. This circuit provides the Compare instruction with the "skip-if-not-equal technique".

(b) Gate MC86A is enabled during Phase 3 and T4 of an ISZ instruction (if C16 is true). This C16 is the carry out of Adder 15 and is true during ISZ if, and only if, +1 was added to -1 and the result is C16. This puts all 0's in the T-Register.

(c) Gate MC84A is enabled if SKF (Skip Flag) is true at T4 of a SFS or SFC (skip if Flag is Set or Clear) instruction.



"CARRY" FLIP-FLOP CIRCUITS

FIG. 2-20

(d) Gate MC87A is enabled during SRG instructions if TR3, $\overline{RB\emptyset}$ and T4 are true. This circuit provides the SLA/B capability for the SRG instructions. This instruction is used in both the SRG and ASG instruction groups.

e. Alter-Skip Instruction Decoding

(1) Gate MC54B is the enabling gate for all ASG instructions. The skip instructions in the ASG can be combined such that if one or more true skip conditions are present, the skip will occur. The only exception to this rule is the SSA/B, SLA/B, RSS combined instruction. This unique instruction requires both skip conditions to be met.

(a) Gate MC127B gates the normal true skip condition outputs with $\overline{TR\emptyset}$ (TRØ = RSS, Reverse Skip Sense).

(b) Gate MC25C is true if TR1 is true (SZA/B), the "T" buses are all zero, and the time is T5. Time T5 is the last enabling time period for ASG instructions.

(c) Gate MC15C is true if TR4 (SSA/B), $\overline{RB15}$ and T4 are true.

(d) Gate MC96C is true if TR3 (SLA/B), $\overline{RB\emptyset}$ and T4 are true.

(e) Gate MC77C is true if TR5 (SEZ), $\overline{EXTEND}$ and T3 are true.

(f) Gate MC74B output is true only if the skip condition for SZA/B, SSA/B, SLA/B or SEZ is not present, or if none of the ASG (Skip) instructions have been selected.

(g) Gate MC25A is true if TR1 (SZA/B) and T5 are true.

(h) Gate MC25B is true if TR4 (SSA/B) and T4 are true.

(i) Gate MC15A is true if TR3 (SLA/B) and T4 are true.

(j) Gate MC15B is true if TR5 (SEZ) and T3 are true.

(k) Gate MC24A is true at T5 if no other skip instructions have been selected; that is, $\overline{TR5}$, $\overline{TR4}$, $\overline{TR3}$, and $\overline{TR1}$. If MC24A is enabled and TRØ is true, then gates MC54C

and MC54B will be enabled and the Carry Flip-Flop will set at T5. Gate MC24A provides an unconditional skip feature when used alone; that is, not used in combination with other ASG instructions.

(1) Gate MC87B is true if "T" bus bits (0-15) are all zero.

2. Addressable A and B Logic (Figure 2-21)

a. Memory Address (0 and 1) Decoding

(1) The purpose of these circuits is to decode memory addresses 0 and 1, which by definition are the A and B-Registers. If either address 0 or 1 is selected by a memory reference instruction, then the appropriate A or B Addressable Flip-Flop is set. The setting of these flip-flops provide the enabling signals required to force the selected register to "act like" it was memory.

(a) Gate MC105A decodes addresses at TØ and Phase 1, 2, or 3. This circuit is true if "T" buses (0-14) are all zero.

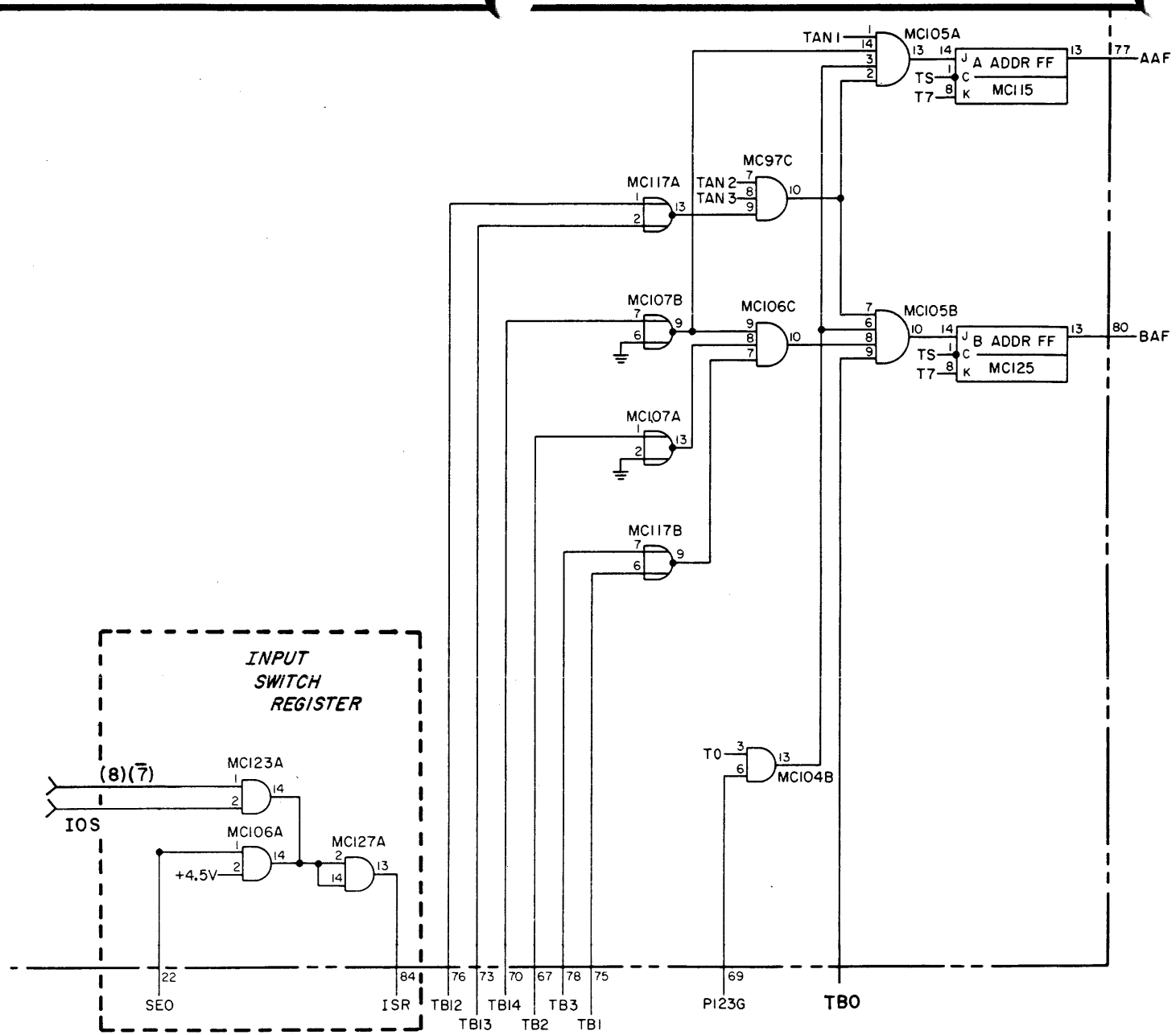
(b) Gate MC105B decodes addresses at TØ and Phase 1, 2, or 3. This circuit is true if "T" buses (1-14) are zero and TBØ is true.

b. Input Switch Register Section

(1) The purpose of this logic is to enable the Switch Register for data input.

(a) Gates MC106A and MC127A are true if the LOAD A, B, LOAD ADDRESS or LOAD MEMORY switches are depressed. The signal from MC127A is called ISR (Input Switch Register) and enables the Switch Register.

(b) Gate MC123 also enables ISR if TR8, $\overline{TR7}$ and IOS are true. TR8, $\overline{TR7}$ and IOG are true for LIA/MIA. Function IOS (I/O Switch Address) is enabled if the Select Code is Ø1.



"A" "B" ADDRESSABLE FLIP-FLOPS

FIG. 2-21

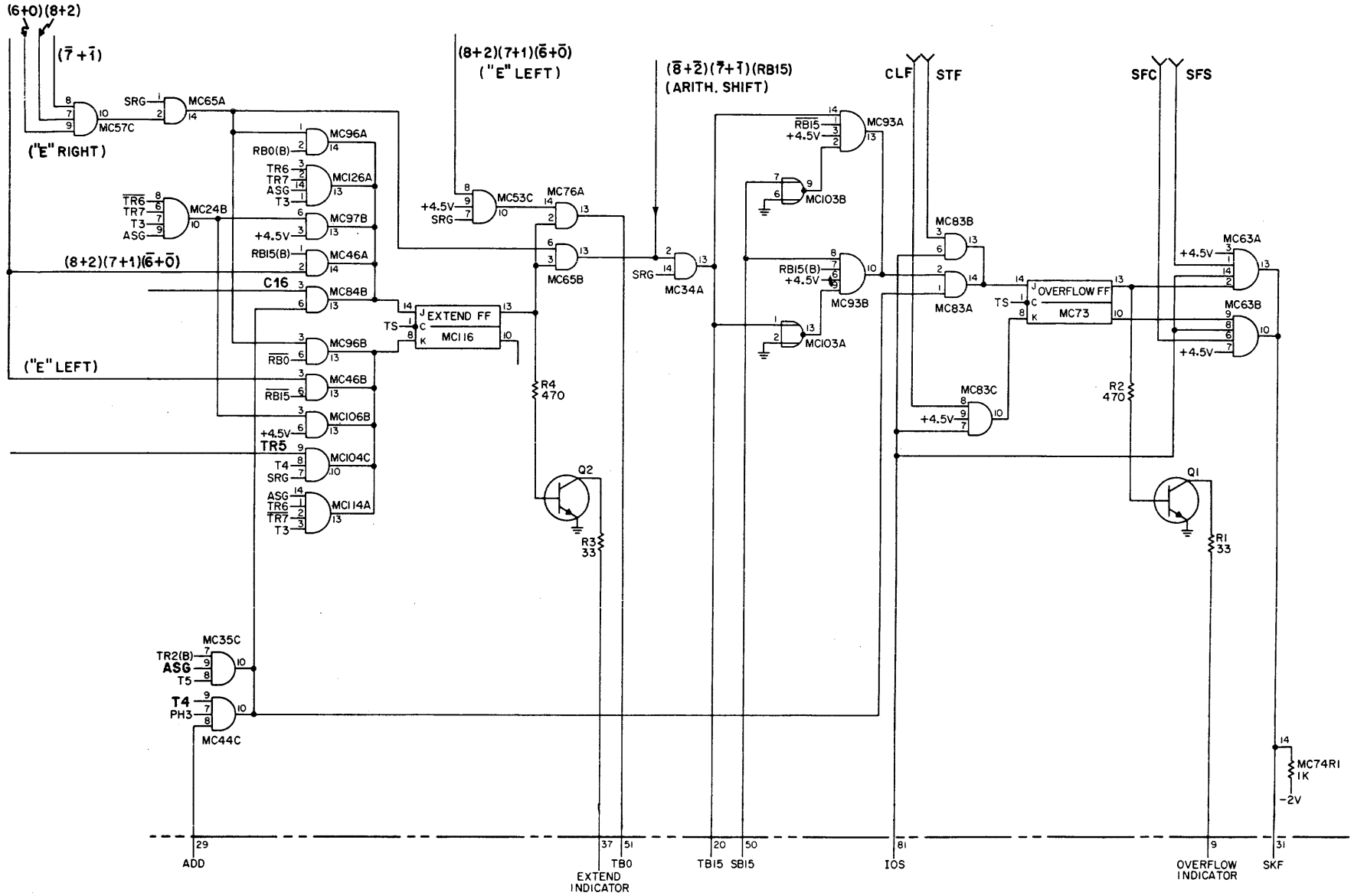
3. Extend Logic (Figure 2-22)

a. Shift-Rotate Operations

(1) The E-Register is a single J-K flip-flop that is set by a carry from the A or B-Register (bit 15) during arithmetic operations. The E-Register will not be complemented by subsequent carries. The E-Register can be cleared, set, complemented and tested by ASG instructions. The E-Register can be rotated with the A or B-Register and cleared by SRG instructions. The Overflow Register is also a single J-K flip-flop. Overflow is set by arithmetic overflow during add or increment operations only.

(2) The Extend Circuit is shown on Figure 2-22. Gate MC57C is enabled for TR2, $\overline{TR1}$ and TRØ, "or" TR8, $\overline{TR7}$ and TR6. The SRG decoding diagram shows this to be true for ERA (E right with A/B). Gate MC57C output is gated with SRG using gate MC65A. This enables gate MC96A if RBØ was true or gate MC96B if RBØ was false at the time of the instruction. The output of gates MC96A and MC96B will set or reset the E-Register Flip-Flop. The clock input to the E-Register is TS. Remember, SRG control functions are enabled at T3 and/or T5. The set side output of the E-Register is connected to gate MC65B which is enabled if E = 1 for ERA/B instructions. A true output from MC65B will enable MC34A and a true level will appear on TB15. At (T5)(TS) "or" (T3)(TS) the appropriate "Store T Bus" function will be enabled and "T" bus 15 data will be strobed into the A or B flip-flop 15. At the same time, the E-Register will reflect the status of RBØ. This circuit enables the rotating of "E" to the right with register A or B.

(3) Gates MC46A, MC46B, MC53C and MC76A are the gates required to implement "E" left with the A or B instructions. The operation is identical as above with the exception of the inputs and outputs. The E-Register inputs for ELA/B are RB15 and $\overline{RB15}$ while the set side of the E Flip-Flop is gated onto TBØ. Gate MC104C will reset the E-Register at T4 if SRG and TR5



EXTEND/OVERFLOW

FIG 2-22

are true. This circuit allows CLE to be combined with other SRG instructions. Gate MC34A is enabled by arithmetic shifts also. This will not affect "E", but enables bit 15 (Sign) through RB15 to TB 15. This action "rewrites" the Sign back into bit 15 during each arithmetic shift (A/BLS, A/BRS).

b. Alter-Skip Operations

(1) The ASG instructions for register "E" are:

(a) CLE Clear E
(b) CME Complement E
(c) CCE Clear, Complement E (Set E)

(2) Gate MC114A is enabled if ASG, TR6, $\overline{TR7}$ and T3 are true. This gate implements CLE. Gate MC126A is enabled if ASG, $\overline{TR6}$, TR7 and T3 are true. This gate implements CCE. Gates MC24B, MC97B, and MC106B are enabled if ASG, TR6, TR7 and T3 are true. Since both the J and K inputs are enabled, the E Flip-Flop will change state or toggle. These circuits implement CME.

c. Arithmetic Operations

(1) Gate MC44C is enabled during Phase 3 and T4 of the Add instructions (ADA or ADB). This gate enables one input to gate MC84B. If C16 is true, the E-Register will be set. C16 is the carry out of Bit 15 Adder. Gate MC35C is enabled during ASG and TR2 at T5 (INA/B). Its operation is identical to MC44C.

4. Overflow Logic (Figure 2-22)

a. Overflow Rules

(1) Positive Overflow - if the addend and augend are both positive, a carry from bit 14 to bit 15 causes overflow.

ADDEND	Ø77777
AUGEND	ØØØØØ1
SUM	1ØØØØØ

(2) Negative Overflow - if the addend and augend are both negative, no carry from bit 14 to bit 15 causes overflow.

ADDEND	1ØØØØ1
AUGEND	1ØØØØ1
SUM	ØØØØ1Ø

(3) The Overflow instructions are in the I/O Group. By definition, Input-Output Flag Flip-Flop Ø1 is the Overflow Register. The Overflow Flip-Flop can be cleared, set and tested using IOG instructions.

(4) Gate MC93A is the positive overflow enabling gate. Gate MC103B provides a true level to MC93A if SB15 is positive (zero). If SB15 = Ø, RB15 = Ø and TB15 = 1, then a positive overflow has occurred. Gate MC93A will produce a true level to one input of MC83A. The other inputs to MC83A are from MC35C or MC44C. These gates are enabled for Add or Increment instructions only. The output of MC83A is connected to the "J" input of the Overflow Flip-Flop. The clock input for the Overflow FF is the timing signal TS (for clean positive triggering).

(5) Gate MC93B is the negative overflow enabling gate. SB15 = 1, RB15 = 1 and TB15 = Ø produce a true output which is connected to overflow enabling gate MC83A. Once set, the Overflow Flip-Flop will remain set until cleared by program instruction. Subsequent overflow conditions will not complement the Overflow Flip-Flop.

(6) Gate MC83B enables the setting of the Overflow Flip-Flop by program instruction. A STF (Set Flag) instruction combined with an I/O select code of Ø1 (IOS) enables gate MC83B, which will set the Overflow Flip-Flop at (T3)(TS).

(7) Gate MC83C enables the clearing (reset) of the Overflow Flip-Flop by program instruction. A CLF (Clear Flag) combined with an I/O select code of Ø1 will cause the Overflow Flip-Flop to reset at (T4)(TS).

(8) Gates MC63A and MC63B provide the capability of testing the Overflow Flip-Flop status. If a SFS (Skip if Flag Set) instruction with a select code of Ø1 is executed, a SKF (Skip Flag) signal will be generated if the Overflow Flip-Flop was in the "1" state. The SFC (Skip if Flag Clear) works in the same manner, testing for the opposite condition ("0" state).

5. Review

(1) Why is it possible to use the same decoder logic to decode both SRG and IOG instructions?

(2) What select code must be used for SFC, (C) and SFS, (C) instructions?

(3) What is the main control function for outputting data? For inputting data?

(4) What control function enables data to be transferred from the Switch Register onto the "S" bus?

(5) What are the three basic shift control functions?

(6) To perform two ALS operations, what two control bits in the instruction word must be true?

(7) When using SRG instructions, what is the purpose of the Carry Flip-Flop?

(8) When performing an ISZ instruction, when will C16 be enabled? What will be the result of C16 being enabled?

(9) When using ASG instructions, when will a skip occur? What is the exception?

(10) What is the purpose of the Addressable A and B circuits?

(11) What four ASG instructions affect the E-Register?

(12) What positive bit "carry" causes the Overflow Register to set? What negative bit carry?

(13) What instruction group contains Overflow instructions?

(14) With the Overflow Register set, a subsequent overflow condition occurs. What is the state of the Overflow Register after the second overflow condition?

(15) How can the Overflow Register be cleared?

E. ARITHMETIC LOGIC

1. Registers and Data Buses (Figure 2-23)

a. Description

(1) The Arithmetic Logic boards contain all the circuits required to read data from the registers to the "R", "S" and I/O buses, the actual arithmetic and logic circuits, and of course, the data registers themselves. The boards are layed out such that four complete sets of circuits are physically located on one board. Four boards are required to furnish 16 complete circuits for registers P, M, T, B and A.

(2) Each of the 5 Register Flip-Flops are identical. The Schematic shows four complete register circuits on the board. Where unique backplane wiring is required, it is indicated by a different signal name for that particular pin number. For example, pin 41 is wired to $\overline{\text{SLM}}$ for cards that contain bits 0-3, 4-7, and 7-11; but it is wired to $\overline{\text{RRL}}$ for the card that contains bits 12-15. The wiring changes allow boards to be identical and interchangeable.

b. Reading and Storing Data

(1) For purposes of explanation, circuits for bit 1 are used:

(a) Gate MC95D enables T-Register data onto the "S" bus.
(b) Gate MC95C enables M-Register data onto the "S" bus.
(c) Gate MC94D enables P-Register data onto the "R" bus.
(d) Gate MC94A enables A-Register data onto the "R" bus.
(e) Gate MC94C enables B-Register data onto the "R" bus.
(f) Gate MC94B is enabled by IOI to read data from IOBI 1 onto "S" bus 1.

(g) Gate MC77A is enabled by IOCO to write data from "R" bus 1 onto IOBO 1.

(h) Gate MC47B gates the inverted output of all "T" bus circuits on the card and produces TAN1 if TBØ, TB1, TB2, and TB3 are zero.

(i) Gate MC75B is the "T" bus inverter for driving the "K" inputs of all data flip-flops and MC47B.

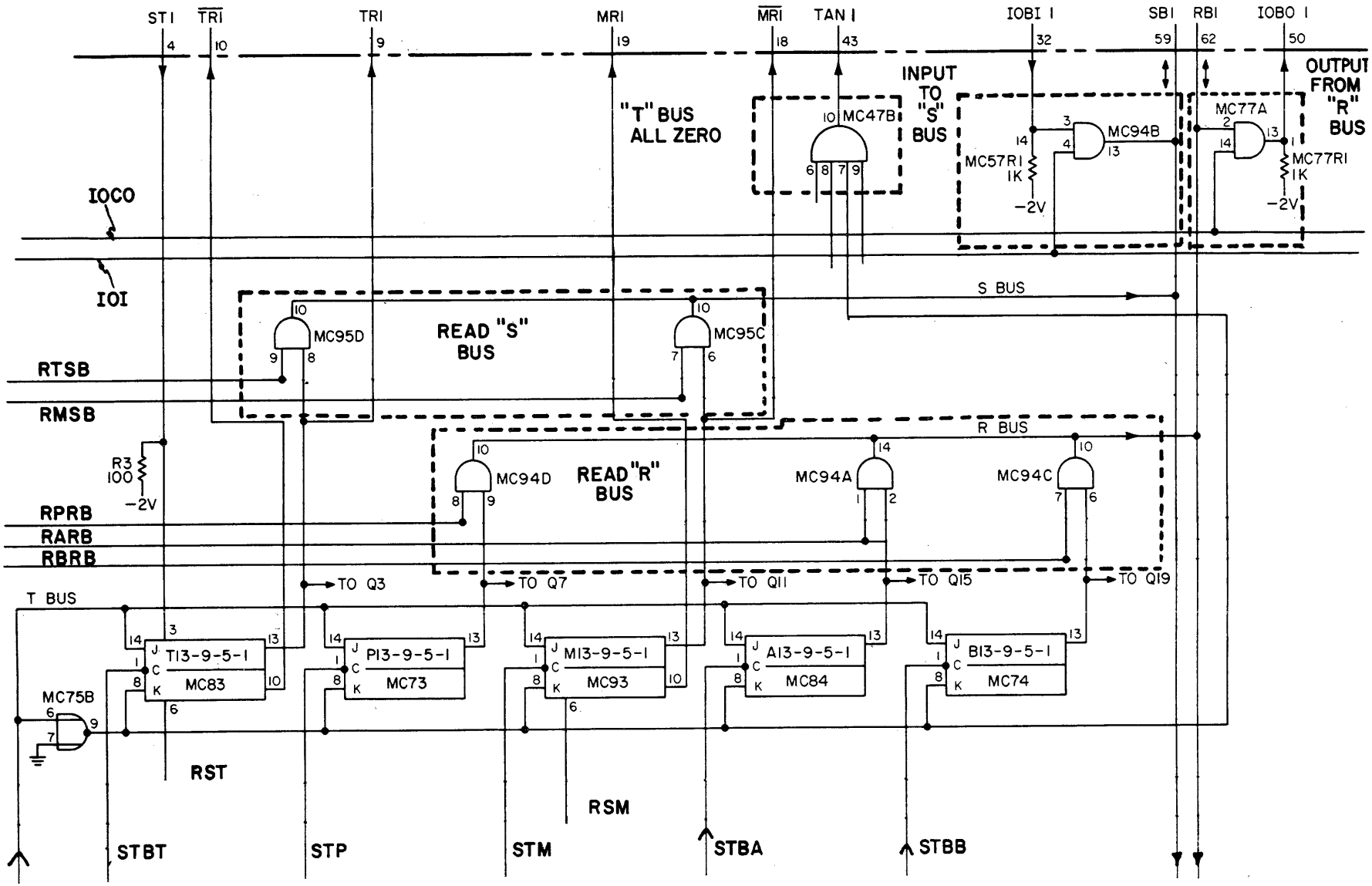
(2) The clock inputs to the Register Flip-Flops are the Store functions developed on the Instruction Decoder board. All Store signals were gated with TS on the Decoder board for clean triggering.

2. Logical and Arithmetic Functions (Figure 2-24)

a. Add

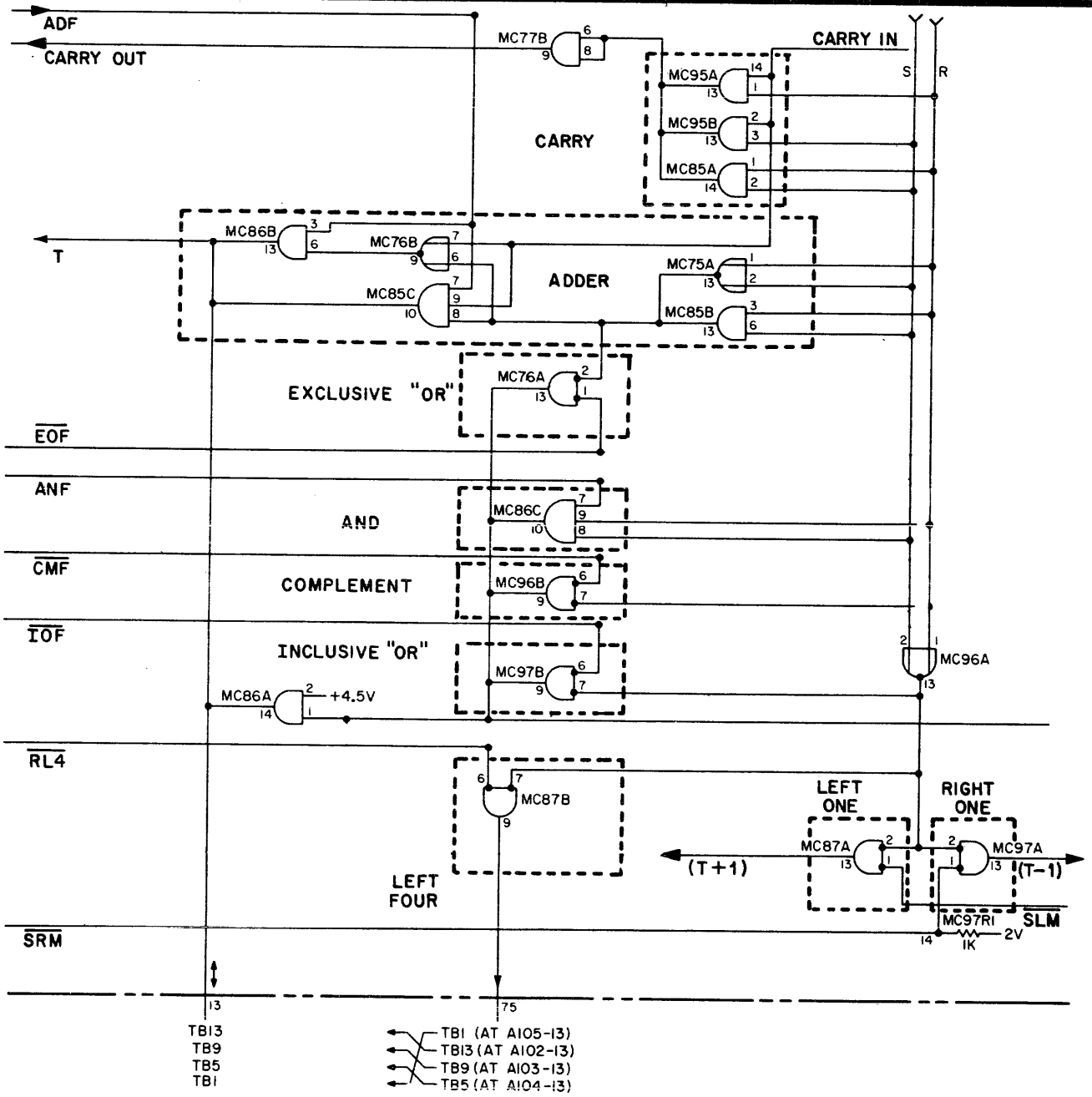
(1) Each bit in the computer word has its own Adder and logical circuits. With the exception of ADF and ANF, all other logical functions are enabled by a "0" (or false input level). In other words, if CMF = 1, then $\overline{CMF}$ = 0, and the function is enabled. However, if CMF = 0, then $\overline{CMF}$ = 1 and the circuit is inhibited. The circuits used for this operation are 0952 dual NOR gates. In this application they are shown as NAND gates. Two false inputs yield a true output.

(2) Gates MC75A, MC85B, MC76B, MC85C, and MC86B comprise the Adder (without carry) circuit. The inputs to the Adder are the "R" and "S" buses. Gates MC86B and MC85C are enabled by ADF. Gates MC75A and MC85B comprise an "Exclusive OR" gate. Gates MC76B and MC85C (when enabled) combine the "carry in" with the "sum" in a second "Exclusive OR" operation. Gates MC86B and MC85C produce the true sum. These gates are "or" tied at the "T" bus for storage into the appropriate register.



REGISTER FLIP-FLOPS AND DATA BUSES

FIG 2-23



Logical and Arithmetic Circuits

FIG. 2-24

(3) Gates MC95A, MC95B, MC85A and MC77B comprise the carry detection circuit which provides the "carry out" to the next higher order "carry in" circuit. The inputs to the carry circuits are the "R" bus, "S" bus, and "carry in". A "1" output from MC95A, MC95B or MC85A will provide a "carry out."

b. Exclusive OR

(1) Gate MC76A is the "Exclusive OR" function enabling gate. This circuit is enabled by $\overline{\text{EOF}}$. If either MC75A or MC85B produces a true output while $\overline{\text{EOF}}$ is present, then MC86A will produce a false output. If we examine the input conditions of the "R" and "S" inputs we see that this is correct. Gate MC76A provides the inversion required to produce the "Exclusive OR" of the "R" and "S" bus inputs.

c. AND

(1) Gate MC86C provides the AND capability. ANF being true enables this gate. If the "S" and "R" buses are ture, then MC86A will produce a true output to the "T" bus.

d. Complement

(1) Gate MC96B produces the "complement" of the "R" bus on the "T" bus if CMF is true.

e. Inclusive OR

(1) Gates MC97B and MC96A produce the "Inclusive OR" capability.

f. Shift One

(1) Gate MC87A produces a left shift of one bit when SLM is enabled.

(2) Gate MC97A produces a right shift of one bit when SRM is enabled.

g. Left Four

(1) Gate MC96A acts as an inverter for shift and rotate operations. Since only the "R" bus is used for shifting operations, the "S" bus input is always zero.

(2) Gate MC87B is enabled by RL4. If the "R" bus input to MC96A was a "1", the output of MC96A will be "0". Two "0" inputs to MC87B produce a "1" output to "T" bus 5.

3. Review

(1) How many Arithmetic Logic boards are required to furnish 8 circuits for the P, M, T, A and B registers?

(2) What functions are used to clock the registers? Where are they generated?

(3) What two control functions are enabled by high levels as contrasted to those that operate on low levels?

(4) What provides the inputs to the Adder?

(5) What provides the inputs to the "carry detection" circuit?

FRONT PANEL COUPLER

1. Debounce Network (HP 2116A/HP 2115A Schematics)

a. Controls

(1) The Front Panel Coupler board converts switch signals from the front panel controls to logic levels, and then distributes them throughout the Central Processor Unit. The Front Panel Coupler for the HP 2115A differs slightly from the HP 2116B board and they are <u>not</u> interchangeable. The switch register logic on the HP 2115A has been changed: gates for decoding the protected memory addresses were added, and the basic computer power turn on circuitry was added to the HP 2115A Front Panel Coupler Board.

(2) The following switch debounce circuits are identical; Single Cycle, Display Memory, Load Address, Load A, Load B, and Load Memory. At turn on time, signal POFP is a one level. This signal holds all debouncd flip-flops reset until the expiration of POFP. It is necessary to hold these flip-flops in the reset condition even through the normally closed contacts of the switch contact the reset side to +4.5 volts. This prevents the possible premature initiation of any switch operation that otherwise might take place. As soon as POFP becomes true, the computer is initialized and ready to perform. When

depressed, the "momentary on" type switches used in the computers connect +4.5 volts to one input of an AND gate. The other input to this gate is tied to $\overline{RF2}$ (Run Flip-Flop 2). This signal is true only when the computer is in the Halt mode. If $\overline{RF2}$ is true, the AND gate is enabled and true level is applied to the set input of the debounce flip-flop. The first positive excursion causes the flip-flop to set. Any negative excursions caused by switch bounce are then ignored by this circuit. When the switch is released, the normally closed contacts of the switch apply +4.5 volts to the reset side and the flip-flop is then reset. The Halt and Preset debounce Flip-Flops are located on the Timing Generator board. The Run Flip-Flop is on the FPC board but, like the Halt circuit, it is always enabled; that is, no inhibiting gate is present on the set side input.

2. Switch Register (HP 2116B/HP 2115A Schematics)

   a. The toggle switch input circuits on the HP 2116B consist of a SPDT toggle switch and an "AND" gate for each of the 16 bits. When the switch is closed, +4.5v is applied to one input of the associated gate. The gates are enabled by a signal called ISR (Input Switch Register). This signal is true when any of the LOAD switches are depressed, or if a LIA/B or MIA/B (Ø1) is being executed. The output of the different gates are tied directly to the IOBI lines.

3. Control Switches (HP 2116B/HP 2115A Schematics)

   a. Maintenance Switches

      (1) Both the HP 2115A and HP 2116B have switches on the back of the front panel that assist in troubleshooting. These switches are:

         (a) MEMORY-OFF-NORMAL
         (b) INSTRUCTION LOOP-OFF-NORMAL
         (c) PHASE LOOP-OFF-NORMAL

      (2) The PHASE LOOP and MEMORY switches produce a true level (+4.5 volts) in the NORMAL position while the INSTRUCTION LOOP switch produces a false (0 volt) level when in the NORMAL position.

(3) The LOADER PROTECT switch provides a true level (+4.5 volts) when in the PROTECTED position. This switch setting provides the true signal LPS to the Memory Module Decoder board and prevents memory accesses to the protected are of memory.

4. Review

(1) What signal holds all debounce flip-flops reset until computer power reaches optimum operating level?

(2) What signal prevents manual switch operation when the computer is in the "Run" mode?

(3) Why are the debound flip-flops required?

(4) What is the enabling signal for inputting Switch Register data to the Input bus?

(5) Do the Halt and Preset switches have debounce flip-flops?

central processor operation

Central Processor Operation

A. INTRODUCTION

1. Objectives

a. Approach

(1) In Lesson 4 the functional blocks of the CPU section were discussed in detail. In this lesson, the student will be shown how a typical instruction (ISZ) is implemented in the computer. The student will be required to trace, throughout the CPU section, each and every signal to implement this instruction.

(2) Extensive use will be made of the Timing Chart, Logic Equations, Back-plane Wiring List, and the CPU schematics throughout this presentation. The student should arrange these materials in a logical and easily accessible manner before the presentation begins.

2. Review Central Processor Unit (Schematics)

a. System Timing Generator

(1) This board provides the basic 5 MHz clock (4 MHz in HP 2115A) and all timing signals for the computer. It consists of six basic circuits:

(a) An oscillator and Frequency Divider which provides the basic 5 MHz (4.0 MHz) clock and generates the TS pulse each 200 ns (250 ns).

(b) A Time Period Generator which provides the eight basic timing pulses TØ thru T7.

(c) A Memory Timing circuit which controls the reading, writing and strobing of memory.

(d) The Phase Decoder which provides the four basic machine phase signals: PH1, PH2, PH3, and PH4.

(e) The Run-Halt circuit which controls program operation modes run and halt.

(f) A Control Switch circuit which provides access to certain control signals originating on the front panel console.

b. Instruction Decoder

(1) This board determines which instruction is to be implemented, and also provides most of the control signals to implement that instruction. The board consists of four basic circuits:

(a) A Memory Reference and Group Instruction Decoder which decodes all memory reference instructions, and decodes the ASG, SRG, and I/O groups.

(b) A Read circuit which controls reading all register data onto the R-S-T buses.

(c) An Arithmetic Function circuit which allows performing the required logical and arithmetic operations.

(d) A Store circuit which controls storing data from the T bus into the various registers.

c. Shift Logic

(1) This board derives its name from the fact that the shift and rotate functions are generated here. This board also performs the final decoding for the ASG, SRG and I/O Group instructions. This board consists of six basic circuits:

(a) A Halt Instruction and Preliminary Group Instruction Decoder which decodes the Halt instruction, and determines whether a group instruction is in the SRG or I/O Group. Since these two groups cannot be active at the

same time, a considerable savings of gates is realized by sharing the decoding network between both groups.

(b) An I/O Instruction Decoder which decodes all I/O instructions.

(c) A Shift-Rotate Decoder which decodes all SRG instructions.

(d) The Carry circuit which decodes ASG instructions and sets the Carry FF under certain circumstances.

(e) The A/B Addressable Flip-Flops which allow the A and B registers to be used as memory locations.

(f) The Extend/Overflow circuit which controls setting the Extend and Overflow Flip-Flops.

d. Arithmetic Logic

(1) These boards contain the five working registers and the required arithmetic logic circuits to read, store and transfer data. These boards contain two basic circuits:

(a) The Register Flip-Flops (A, B, T, P and M).

(b) The Logic and Arithmetic circuits which control the actual logical or arithmetical operations.

e. Front Panel Coupler

(1) The Front Panel Coupler essentially provides the necessary communication between the front panel control switches and the control processor unit.

(2) The Front Panel Couplers for the HP 2116B and HP 2115A are <u>not</u> interchangeable.

3. Review Timing Chart (Section 1)

a. Instructions

(1) The timing chart provides answers to three basic questions:

(a) What instruction are we implementing?
(b) What phase are we in?
(c) What time is it?

(2) The timing chart translates instructions into machine phases and timing periods. From this information we may then determine the control functions required to implement a given instruction. The control functions are given by our logic equations. Thus, the problem becomes one of interpreting the timing chart and making the transition to the logic equations.

(3) Instructions are basically micro programs. That is, an explicitly defined sequence of operations must be performed to implement each instruction. The timing chart tells us, at any given period in time, what operation is being performed. Each instruction performed can be best illustrated by considering it as a "micro program". For instance, to implement a flow-chart symbol such as "take the two's complement" requires two instructions: CMA and INA. Each instruction in turn requires a "micro program" to implement.

(a) The CMA micro program:

RARB
CMF
STBA

(b) The INA micro program:

```
RARB
SBØ
ADF
STBA
```

b. Phases

(1) The computer may be in one - and only one - phase at any given time.

(2) Memory reference instructions are the only instructions requiring more than one phase to execute. Indirect and Execute phases are associated with Memory Reference instructions only. In the case of all these instructions (except JMP), the action during the Fetch and Indirect phases is similar, so these phases are shown on the Timing Chart only once.

(3) The exception is the JMP instruction which does not use an Execute phase; execution can occur in either the Fetch (Direct JMP) or Indirect (Indirect JMP) phases.

c. Time Periods

(1) The basic machine cycle is 1.6 μs (2.0 μs) long. A machine cycle is further defined into 8 time periods (TØ-T7). Thus, each time period is 200 ns (250 ns) long.

(2) Memory is accessed (READ) only during the interval (TØ-T2) as shown on the Timing Chart. Memory writing (WRITE) occurs only during the interval (T3-T5).

(3) Each timing period has a TS pulse 50 ns long which is delayed 150 ns from the leading edge of the time period pulse. This TS pulse is used to "clock" various logic functions performed during a given time period.

d. The ISZ Instruction

(1) The ISZ instruction is a unique memory reference instruction. During the Execute phase of the ISZ instruction (Increment, Skip if Zero), the contents of the addressed memory cell must be altered and checked between the Read and Write portions of the memory cycle. These actions require more time than is normally available in this interval, so the Write portion is delayed. Once the word read from memory is in the T-Register (T3 and T4), it is incremented by reading onto the S Bus, adding "one" in the arithmetic logic and storing back into the T-Register. If previously the word read out was all ones, the addition of another one causes a rollover to all zeros, and produces a signal (C16) which sets a Carry Flip-Flop in the arithmetic logic. Then, at T5, the Write portion of the memory cycle is permitted to begin, and two time periods (0.4 microsecond or 0.5 microsecond) are inserted at this time for writing the incremented value back into memory. During T6 and T7, the P-Register is read onto the R Bus, and a "one" is read onto the S Bus. These are added together, and if the Carry Flip-Flop is set, another "one" is added and the result is stored in the P and M Registers. Thus, if the Carry Flip-Flop was set, the P and M Registers are incremented by two instead of one, skipping one memory location for the next Fetch phase. (The Carry Flip-Flop is automatically reset at the start of the next phase.)

4. Review Logic Equations

a. Control Functions

(1) Logic equations are used to conveniently describe logical circuits without resorting to logic diagrams. A logic equation is a series of Boolean expressions which describe certain

conditions necessary to generate a logic signal. Logic equations are used in the HP 2116B/HP 2115A maintenance procedures as a troubleshooting tool.

b. Timing Chart Relationships

(1) The purpose of using logic equations is to facilitate troubleshooting. Once it is determined from the Timing Chart what instruction is being performed, what phase has control, and what time it is; then the logic equations may be used to find the control functions required to perform the instruction. These logic signals may then be measured.

5. Review Back-plane Wiring List

a. Logic Equation Relationship

(1) Once the sequence number of a control function is extracted from the Logic Equations, the Back-plane Wiring List may be referenced to find the source and terminals of that control function.

6. Review

a. What six basic circuits are located on the STG board?

b. What four basic circuits are located on the Instruction Decoder Board?

c. What six basic circuits are located on the Shift Logic Board?

d. What two basic circuits are located on the Arithmetic Logic Board?

e. What is the normal pattern to be followed when tracing a control signal through the computer?

f. Why must the timing cycle be extended when executing an ISZ instruction?

g. Once the contents of memory is "read" into the T-Register, how is the T-Register incremented when executing an ISZ instruction?

h. When executing ISZ, what happens during T3T4 if the contents of the T-Register are all "ones"?

i. What determines whether the P and M Registers are incremented by one or two when executing an ISZ instruction?

j. If the Carry FF is set during Phase 3 of an ISZ instruction, how is it cleared?

IMPLEMENTING THE INSTRUCTION

NOTE

To make this presentation more meaningful, the Addressable A/B Registers and SINGLE CYCLE operation are used. The Computer should be initialized as follows:

POWER on	
HALT mode	
A-REGISTER	177777
B-REGISTER	034000
P, M-REGISTERS	000001

1. Phase One (FETCH) Operations (Figure 3-1)

   a. Setting Phase One

      (1) Front Panel Coupler Schematic

         (a) When the SINGLE CYCLE pushbutton is depressed, +4.5 volts sets the Single Cycle Switch (SCS) Debounce FF. The SCS (SIS) signal leaves the FPC board at pin 78.

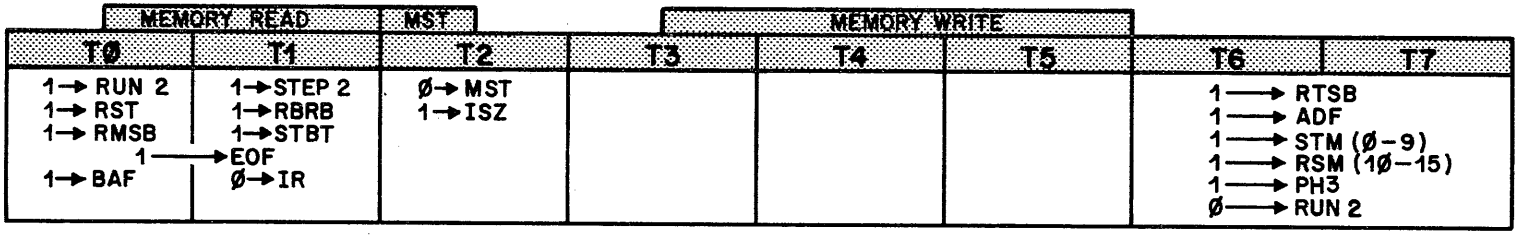
CLASS EXERCISE — ISZ INSTRUCTION EXECUTION

1. INITIAL CONDITIONS

REGISTER A = 177777
REGISTER B = 034000
COMPUTER IN HALT MODE
REGISTERS P and M = 000001
REGISTERS E and OVFLO = 0
PHASE 1 (FETCH PHASE)

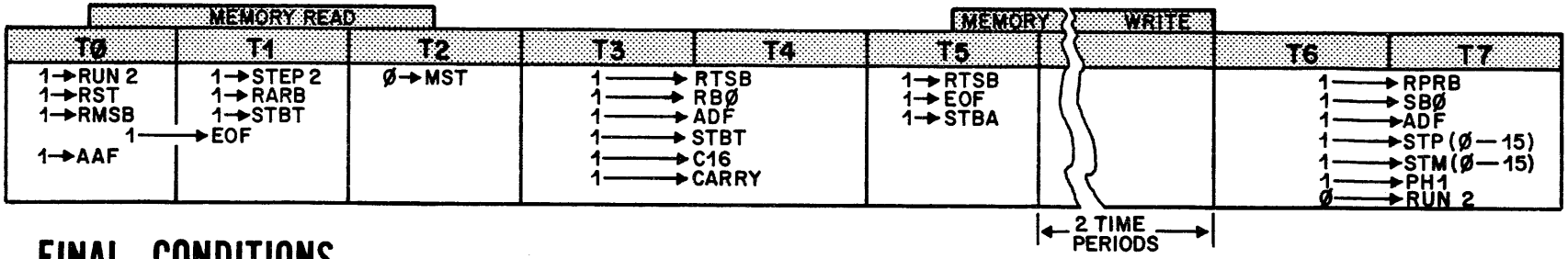
2. OPERATOR ACTION

DEPRESS SINGLE CYCLE BUTTON (FETCH PHASE BEGINS)



3. OPERATOR ACTION

DEPRESS SINGLE CYCLE BUTTON (EXECUTE PHASE BEGINS)



4. FINAL CONDITIONS

REGISTER A = 000000
REGISTERS P and M = 000003

FIG. 3-1

(2) Back-plane Wiring List

(a) The SCS (or SIS) signal is routed from the FPC board to A106-56 (STG board).

(3) STG Board (RUN-HALT section)

(a) The SCS signal appears at pin 56. SCS being true enables gate MC86A which provides a true input to the STEP 1 Flip-Flop MC94A. This flip-flop will set at the leading edge of T2. With STEP 1 set and STEP 2 (MC94B) reset, gate MC76C is enabled. This gate provides a true "J" input to the RUN 2 Flip-Flop MC74. At T7TS this flip-flop will set. The $\overline{RF2}$ signal is now a "0". This signal inhibits the front panel pushbuttons until the RUN 2 Flip-Flop is reset.

(b) Gate MC27A in the PHASE DECODER section is a two-input AND gate. One input to this gate is EPH (Enable Phase) which is normally true. The true RF2 signal enables MC27A. MC37A and MC13A enable the P123 (pin 23) and PH1 (pin 41) signals. Since the computer was initialized to Phase 1, and no "J" or "K" inputs were supplied to the J-K Flip-Flop MC44, the computer will remain in Phase 1.

b. Clearing the T-Register

(1) Instruction Decoder (READ section)

(a) Gate MC125C is enabled at TØ. This enables MC114 at TØTS and brings up the RST (Reset "T") function. This signal leaves the board at pin 58.

(2) Arithmetic Logic (Upper left diagram)

(a) The RST signal comes into this board at pin 7. This signal is applied to all T-Register Flip-Flops and the T-Register is cleared.

c. Testing the Addressable A and B Function

(1) Instruction Decoder (READ section)

(a) Gate MC125C enables gates MC124D and MC114B which bring up the RMSB (Read "M" onto "S" bus) function. This signal leaves the board at pin 68.

(2) Instruction Decoder (FUNCTION section)

(a) Gate MC122B is enabled at TØT1 which inhibits MC112A and enables the $\overline{\text{EOF}}$ (Exclusive OR Function). The purpose for doing this is to allow the M-Register data on the "S" bus to pass through the "exclusive OR" circuits to the "T" bus. The "T" bus will then be tested to determine if memory addresses 0 or 1 (A or B-Register) have been selected.

(b) The $\overline{\text{EOF}}$ signal leaves the board at pin 67.

(3) Back-plane Wiring

SIGNAL	SOURCE	FROM	TO
P123	STG	A106-23	A107-78
RST	SRF	A107-58	[A105-A102]-7
RMSB (RMS)	SRF	A107-68	[A105-A102]-8

(4) Arithmetic Logic (upper left diagram)

(a) The RMSB (RMS) signal enters the board at pin 8. This signal enables the M-Register data onto the "S" bus. The $\overline{\text{EOF}}$ signal enters the board at pin 76. This signal enables the M-Register data, appearing on the "S" bus, onto the "T" bus.

(5) Arithmetic Logic (upper center diagram)

(a) Gate MC47B would be true if all four "T" bus bits were zero. These signals are called either TAN1, TAN2, TAN3, or TAN4 on the schematics. However, since we are addressing the B-Register, TBØ is true and when inverted inhibits TAN4. This false TAN4 signal will be decoded on the Shift Logic Board to address the B-Register.

(6) Back-plane Wiring

SIGNAL	SOURCE	FROM	TO
TAN1 (T0R1)	RAF	A105-43	A108-58
TAN2 (T0R2)		A104-43	A108-57
TAN3 (T0R3)		A103-43	A108-60
TBØ		A105-69	A108-51
TB1		A105-13	A108-75
TB2		A105-55	A108-67
TB3		A105-17	A108-78
TB12		A103-81	A108-76
TB13		A103-75	A108-73
TB14		A103-84	A108-70

(7) Shift Logic (Addressable A and B section)

(a) Gate MC105B is enabled for addressing the B-Register (000001). At TØTS the B Addressable Flip-Flop MC125 sets. This completes the TØ time period operation.

(8) Backplane Wiring

SIGNAL	SOURCE	FROM	TO
BAF	ERS	A108-80	A107-13 A106-83

d. Loading the T-Register

(1) Timing Generator (RUN/HALT section)

(a) The STEP 2 Flip-Flop MC94B will set at T1 (this phase) which will inhibit gate MC76C. This action removes the true "J" input from the RUN 2 Flip-Flop.

(2) Instruction Decoder (READ section)

(a) The BAF signal appears on pin 13 and provides one true input to gate MC86C. The other input to this gate is ($\overline{JSB}$ $\overline{PH3}$), P123 and T1. At T1, MC86C enables MC87B and brings up the RBRB (Read "B" onto "R" bus) signal.

(3) Instruction Decoder (FUNCTION section)

(a) Gate MC122B is enabled at TØT1. This gate enables $\overline{EOF}$ and allows data from the "R" bus to pass onto the "T" bus.

(4) Instructor Decoder (STORE section)

(a) Gates MC93D and MC93A enable the STBT (Store "T" bus in "T" register) signal at T1TS. This circuit allows the "T" bus data to be stored in the T-Register. This occurs because the Addressable B Flip-Flop was set. The data

from the addressed register is then placed in the T-Register as if it came from memory. The B-Register to T-Register transfer is completed at the trailing edge of T1.

(5) Backplane Wiring

SIGNAL	SOURCE	FROM	TO
RBRB (RBR)	SRF	A107-18	[A105-A102]-28
STBT (STB)		A107-51	[A105-A102]-26

(6) Arithmetic Logic (upper left diagram)

(a) The RBRB (Read "B" onto "R" bus) signal appears at pin 28 and enables all gates required to read B-Register data onto the "R" bus. The $\overline{EOF}$ signal (pin 76) allows the "R" bus data to pass through to the "T" bus. The STBT (pin 51) signal being true will "store" the "T" bus data into the T-Register.

e. Clearing the I-Register

(1) Instruction Decoder (Memory Reference DECODING section)

(a) Gate MC22A resets the I-Register at Phase 1, T1. This completes the T1 time period operations.

f. Inhibiting Memory Read

(1) Timing Generator (MEMORY TIMING section)

(a) Gate MC127A is inhibited by the true BAF input (B Addressable Flip-Flop). MC127 being false inhibits gate MC77C which in turn inhibits gate MC57B. This circuit action inhibits the MST (Memory Strobe Timing) signal during the Addressable A or B Register operations and prevents the actual strobing of memory data into the T-Register.

g. Loading the I-Register

(1) The I-Register is loaded at (T2, TS) which gates the T-Register data (bits 10-15) directly into the I-Register.

h. Instruction Decoding

(1) Instruction Decoder (Memory reference DECODING section)

(a) The coding for the ISZ instruction is ($\overline{IR14}$) (IR13) (IR12) (IR11). This code inhibits gate MC65B which enables $\overline{OPO}$ (One Phase Operation Not). Gate MC24A is also enabled which enables gate MC23A. Gate MC23A is only true for ISZ instructions. This signal leaves the board at pin 76 and completes the T2 time period operations.

(2) Backplane Wiring

SIGNAL	SOURCE	FROM	TO
ISZ	SRF	A107-76	A108-61
			A106-24

i. Loading the M-Register

(1) Instruction Decoder (READ section)

(a) Gate MC103A is enabled by virtue of Phase 1 and $\overline{OPO}$. This gate provides a true input to gate MC103D. At T6T7, MC103D provides a true input to gate MC123A which enables the RTSB signal.

(2) Instruction Decoder (FUNCTION section)

(a) Gate MC127A is enabled at T6T7. This gate enables the ADF (Add Function) signal.

(3) Instruction Decoder (STORE section)

(a) Gate MC43A is enabled at T7 if EIR and $\overline{OPO}$ are true. This gate enables MC55C, MC56B and MC56A which brings up the STM(0-9) (Store "T" bus in M-Register) signal. MC45B is enabled during Phase 1 if $\overline{OPO}$ and $\overline{IR10}$ are true. This gate enables MC46A which brings up RSM(10-15). This signal is applied to the "Direct Clear" input of the M-Register Flip-Flops (15-10). This ensures a Page Zero memory access if $\overline{IR10}$ is true.

(4) Backplane Wiring

SIGNAL	SOURCE	FROM	TO
RSM (10-15)	SRF	A107-11	[A103-A102]-21 A102-14
STM(6-9)		A107-21	A104-22 A103-29
ADF		A107-75	[A105-A102]-5
STM(0-5)		A107-20	[A105-A104]-29 A105-22
RTSB(RTS)		A107-82	[A105-A102]-20

(5) Arithmetic Logic (upper left diagram)

(a) The RTSB (pin 20) signal enables the T-Register data onto the "S" bus. The ADF signal (pin 5) enables the Adder. With no "R" bus inputs present, the data from the "S" bus appears on the "T" bus unchanged. The STM (0-5) and STM(6-9) signals appear on pins 22 or 29 depending on the board location. This signal will store the "T" bus data into the M-Register prior to the "Operand" memory access performed during Phase 3. The RSM(10-15) signal appears on pin 21 or 14 depending

on the board location. The RSM signal is applied to the Direct Clear input of the M-Register Flip-Flops.

j. Setting Phase Three

(1) Timing Generator (PHASE DECODER section)

(a) Gate MC33C provides a true "J" input to flip-flop MC24 if $\overline{\text{OPO}}$, $\overline{\text{JMP}}$, $\overline{\text{TR15}}$, $\overline{\text{Interrupt}}$ and Phase 1 are true. In this example, MC33C will be true which allows MC24 to set at (T7)(TS).

(2) Timing Generator (RUN/HALT) section)

(a) At T7TS the RUN 2 Flip-Flop MC74 will reset. This inhibits gate MC27A and the Phase signals.

k. Review of Phase 1 Operations

(1) At this point the computer is halted with the Phase 3 (Execute) lamp on. During Phase 1 the instruction was "fetched" from location 000001 (B-Register) and placed in the T-Register. The Instruction Register was cleared and then loaded with the new instruction. The instruction was decoded and found to be an ISZ. The operand address was then transferred from register T to register M (0-9). Since this was a Page Zero memory reference, the high order bits (15-10) of the M-Register were cleared. The computer ended the single cycle by setting the Phase 3 (Execute) Flip-Flop and resetting the RUN 2 Flip-Flop.

2. Phase Three Operations

a. Addressing the A-Register

(1) Front Panel Coupler

(a) When the SINGLE CYCLE switch is depressed, this sets the SCS Debounce Flip-Flop and provides a true input to

pin 56 of the Timing Generator board as described before.

(2) Timing Generator (RUN/HALT section)

(a) The SCS signal being true enabled MC86A and set the STEP 1 Flip-Flop MC94A at T2. With STEP 1 set and STEP 2 reset, MC94B enables MC76C. This gate provides a true "J" input to the RUN 2 Flip-Flop MC74. At T7TS the RUN 2 Flip-Flop will set. The $\overline{RF2}$ signal is now a "0" level which inhibits the front panel pushbuttons.

(3) Timing Generator (PHASE DECODER section)

(a) Gate MC27A is enabled when the RUN 2 Flip-Flop is set. This gate enables MC37A and MC15A which provide signals P123 and PH3 to other circuits. This action allows a Phase 3 cycle to begin.

(4) Timing Generator (MEMORY TIMING section)

(a) Gate MC104B is enabled by PH3 and ISZ. (The instruction Register still holds the ISZ instruction from Phase 1). This gate provides an enabling input to gate MC104A and will result in a Phase 3 cycle that is two full time periods longer than normal. This circuit is not effective until later in the machine cycle. Gate MC104B also provides enabling inputs to gates MC16A, MC16C, MC26A, MC26C and MC104C which provide delayed "memory write" capability. Gate MC104B inhibits gate MC55A which then inhibits the normal "memory write" circuits.

(5) Instruction Decoder (READ section)

(a) Gate MC125C is enabled at TØ. This enables MC114 at TØTS and brings up the RST (Reset "T") signal. At the same time, gates MC124D and MC114B enable the RMSB (Read M onto "S" bus) signal; RST and RMSB are then applied to all Arithmetic Logic boards as shown previously.

(6) Instruction Decoder (FUNCTION section)

(a) Gate MC122B is enabled at TØT1. This inhibits gate M112A which then enables the $\overline{\text{EOF}}$ signal (Exclusive OR Function). This signal is applied to all Arithmetic Logic boards as shown previously.

(7) Arithmetic Logic

(a) With RMSB (Read "M" onto "S" bus) true and the $\overline{\text{EOF}}$ (Exclusive OR Function) signal present, the M-Register data appears on the "T" bus. Since the instruction was 034000 (ISZ register "A"), the "T" bus contains all zeros. Under these conditions TAN1, TAN2, TAN3 and TAN4 are all true. The TAN (1-4) and "T" bus signals are routed to the Shift Logic board as shown previously.

(8) Shift Logic (Addressable A & B section)

(a) Gates MC97C and MC105A are enabled for address 000000 (A-Register). These gates provide a true "J" input to the A Addressable Flip-Flop MC115. At TØTS this flip-flop will set. This completes the Phase 3 TØ operations.

(9) Backplane Wiring

SIGNAL	SOURCE	FROM	TO
AAF	ERS	A108-77	A107-49
			A106-75

b. Loading the T-Register with A-Register (0-15)

(1) Timing Generator (RUN/HALT section)

(a) The STEP 2 Flip-Flop MC94B will set at T1. The STEP 2 being set will inhibit gate MC76C. MC76C being false removes the true "J" input from the RUN 2 Flip-Flop MC74.

(2) Instruction Decoder (READ section)

(a) Gate MC83B is enabled at T1. This gate enables MC85A if $\overline{\text{JSB}}$ is true. With MC85A true, and the AAF (A-Addressable Flip-Flop) signal true, MC86B is enabled which enables MC87A and brings up the RARB (Read "A" onto "R" bus) signal.

(3) Instruction Decoder (FUNCTION section)

(a) Gate MC122B is enabled at TØT1. This gate inhibits MC112A and enables the $\overline{\text{EOF}}$ (Exclusive OR Function) signal.

(4) Instruction Decoder (STORE section)

(a) Gates MC93C and MC93A enable MC92A at T1 if the AAF (A-Addressable Flip-Flop) signal is true.

(5) Backplane Wiring

SIGNAL	SOURCE	FROM	TO
RARB (RAR)	SRF	A107-19	[A105-A102]-34

(6) Arithmetic Logic (upper left diagram)

(a) The RARB (Read "A" onto "R" bus) signal comes into the board at pin 34. This signal enables the A-Register data to appear on the "R" bus. The $\overline{\text{EOF}}$ (Exclusive OR Function) signal at pin 76 permits the "R" bus data to

appear unchanged on the "T" bus. The STBT (Store "T" bus in T-Register) signal at pin 51 provides the clock pulse required to "Store" the "T" bus data into the T-Register Flip-Flops. This occurs at the trailing edge of T1 and completes the Phase 3 T1 operations.

c. Inhibiting Memory Read

(1) Timing Generator (MEMORY TIMING section)

(a) The AAF (A-Addressable Flip-Flop) signal being true will inhibit MC127A, which in turn inhibits MC77C which then inhibits MC57B and inhibits the MST (Memory Strobe Timing) signal. This MST signal must be inhibited during AAF or BAF operations. This completes the T2 operations.

d. Incrementing the T-Register

(1) Instruction Decoder (READ section)

(a) Gate MC113C is enabled at T3T4 if the $\overline{\text{JSB}}$ and EIR (Enable Instruction Register) signals are true. MC113C enables MC123A and brings up the RTSB (Read "T" onto "S" bus) signal.

(2) Instruction Decoder (FUNCTION section)

(a) Gate MC97B is enabled by gate MC101B (Phase 3, T3T4) and the ISZ signal. These gates provide a true level to RBØ ("R" bus Ø). At the same time, gates MC116C, MC106B and MC107B are enabled and bring up the ADF (Add Function) signal.

(3) Instruction Decoder (STORE section)

(a) Gate MC83C is enabled at T4. This gate enables MC92A and brings up the STBT (Store "T" bus in "T" register) signal.

(4) Backplane Wiring

SIGNAL	SOURCE	FROM	TO
RBØ (PIR)	SRF	A107-61	A105-37

(5) Arithmetic Logic

(a) The T-Register data appears on the "S" bus. A "1" level appears on the "R bus Ø". The ADF (Add Function) signal is enabled. Since the original contents of register A (now contents of register T) was 177777, a "carry" is generated from each Adder circuit. The "carry" out of the most significant Adder becomes C16. All "T" bus circuits now contain Ø's. At the trailing edge of the STBT (Store "T" bus in T-Register) signal, all T-Register Flip-Flops are reset and the T-Register has now been incremented. This completes the T3T4 operations.

(6) Backplane Wiring

SIGNAL	SOURCE	FROM	TO
C16	RAF	A102-36	A108-64

e. Setting the Carry Flip-Flop

(1) Shift Logic (CARRY section)

(a) Gate MC86A is enabled at T4 if C16 is true. This gate provides a true "J" input to carry flip-flop MC95 and will set at the trailing edge of T4.

(2) Instruction Decoder (FUNCTION section)

(a) Gate MC94C is enabled at T5. This gate provides an enabling input to MC75C. The other inputs to this gate are the $\overline{\text{CPR}}$ and IR12 signals. MC75C is enabled for AND, IOR, STA, STB, JSB, and ISZ instructions. Gate MC75C enables MC103C and MC123A in the READ section of the board. These gates enable the RTSB (Read "T" onto "S" bus) signal. Gate MC102C has the same inputs as MC75C. This gate inhibits MC112A which then enables the $\overline{\text{EOF}}$ (Exclusive OR Function) signal.

(3) Instruction Decoder (STORE section)

(a) Gate MC76C is enabled by MC75C being true and the AAF (A-Addressable Flip-Flop) being true. This gate enables MC77A and brings up the STBA (Store "T" bus in A-Register) signal.

(4) Arithmetic Logic

(a) The RTSB (Read "T" onto "S" bus) signal being true allows the T-Register data to appear on the "S" bus. The $\overline{\text{EOF}}$ signal allows the "S" bus data to appear unchanged on the "T" bus. The STBA (Store "T" bus in A-Register) signal supplies the clock pulse at the trailing edge of T5 to allow the "T" bus data to be "written into" the A-Register Flip-Flops. This operation is required to write the "memory data" into register A. In the case of Addressable A or B operations the data is written into the appropriate register at T5. The actual "memory write cycle" is not required as a result, but to save additional circuits the memory write operation (into actual memory location 0 or 1) still takes place.

f. Extended Write Memory Cycle

(1) Timing Generator (MEMORY TIMING section)

(a) Gate MC16C is enabled one-half time period beyond T5. This provides one true input to gate MC37B. The other input to MC37B is the MTE signal which will be true. Gate MC37B being true enables the MIT signal. MIT is enabled for two and one-half time periods by gates MC62C, MC97B, MC104C, MC97A, MC26C and MC16A. Gate MC26C is enabled at the end of T5. This provides a true input to MC67B which is enabled by MTE. Gate MC67B being true enables MWT. MWT is maintained for two full time periods by gates MC97B, MC62C and MC104C. Gate MC62C in the TIME PERIOD GENERATOR section becomes enabled when Flip-Flop T5T6 (MC102B) is reset. Flip-Flop T6T7 (MC92A) cannot set until the next (CL1) clock pulse. Therefore, MC97B produces a true output which enables MC104C. When Flip-Flop T6T7 (MC92A) sets, MC104C is inhibited and the extended memory cycle (MIT and MWT) ends.

g. Incrementing P and M Registers

(1) Instruction Decoder (READ section)

(a) Gate MC126B is enabled at T6T7. This gate enables gates MC106A and MC107A which bring up the RPRB (Read "P" onto "R" bus) signal.

(2) Instruction Decoder (FUNCTION section)

(a) Gate MC127A is enabled at T6T7. This gate enables MC107B and brings up the ADF (Add Function) signal. MC116A is enabled by MC126B which in turn enables MC97A and produces the SBØ ("S" bus Ø) signal.

(3) Instruction Decoder (STORE section)

(a) Gates MC63B, MC53A, MC66A, MC55B, MC56B, MC55C and MC56A combine to enable the STM (0-15) signal (Store "T" bus in M-Register) at T7TS. Gates MC35D, MC35A, MC36B, MC34C and MC36A combine to enable the STP (0-15) signal (Store "T" bus in P-Register) at T7TS.

(4) Shift Logic (CARRY section)

(a) The Carry Flip-Flop MC95 was set as a result of C16 at time period T4. Gate MC94B is enabled at T6T7 to produce CØ (Carry into bit Ø).

(5) Backplane Wiring

SIGNAL	SOURCE	FROM	TO
CØ	ERS	A108-71	A105-67

(6) Arithmetic Logic

(a) The RPRB (Read "P" onto "R" bus) signal enables the P-Register data out onto the "R" bus. The CØ (Carry into Adder Ø) signal is also true. The SBØ ("S" bus Ø") signal is true. The ADF (Add Function) signal is true. The result of the addition (P register + 2) appears on the "T" bus. The STP (0-15) signal (Store "T" bus in P-Register) and the STM (0-15) signal (Store "T" bus in M-Register) are enabled at T7TS. This allows the "T" bus data to be stored into the P and M Registers at the trailing edge of T7TS.

h. Setting Phase One

(1) Timing Generator (RUN/HALT section)

(a) The RUN2 Flip-Flop MC74 is reset at T7S. The $\overline{RF2}$ signal enables the front panel pushbuttons.

(2) Timing Generator (PHASE LOGIC section)

(a) Gate MC27A is inhibited when the RUN 2 Flip-Flop (MC74) is reset. MC27A being false inhibits MC37A and MC13A. These gates inhibit P123 (Phase 1, 2 or 3) and PH1 (Phase 1) signals. At T7TS the PH3 Flip-Flop MC24 will be reset and the PH1 Flip-Flop MC44 will be set. Only the PH1 Flip-Flop has a true "J" input by virtue of Gate MC53C. When the PH1 Flip-Flop sets, the FETCH phase lamp comes on and the EXECUTE lamp goes off. The conputer has completed the instruction and is now ready for another operation.

3. Review

a. Questions

(1) What signal clears the T-Register?

(2) Why is the RMSB signal enabled at every TØ time period during Phase 1, 2 or 3?

(3) If the A-Register had been addressed as a memory location, which TAN signals would have been false?

(4) At what time period is the Addressable B Flip-Flop set?

(5) What control signals are used to transfer "unaltered" data between data buses?

(6) When is the I-Register always cleared in Phase One?

(7) When addressing the B-Register in Phase One, what signal inhibits the Memory Read cycle? Why is this cycle inhibited?

(8) What signal gates the T-Register data (10-15) into the I-Register?

(9) Why must the Memory Write cycle be delayed and extended two full time periods when doing an ISZ instruction?

(10) What signal on the R bus is used to increment the T-Register for an ISZ instruction? The P and M Registers?

memory

Memory

A. BASIC MEMORY CONCEPTS

1. The Core

a. Physical Description

(1) The ferrite magnetic core is basically a memory element. It has a stable hysteresis loop over the temperature range 0 to 55°C. The core is made of ferrite with a small amount of lithium, and has a diameter of only 0.03 inches.

(2) There are 69,632 cores in each 4K memory module, (4,096 on each of 17 planes including the parity bit).

(3) The cores used are manufactured by Ferox and/or Ampex.

b. Half-Current Relationships (Figure 4-1)

(1) The half-current addressing technique is used in the HP 2116B/HP 2115A computers. An X-axis current (I/2) and a Y-axis current (I/2) are required to change the state of the core.

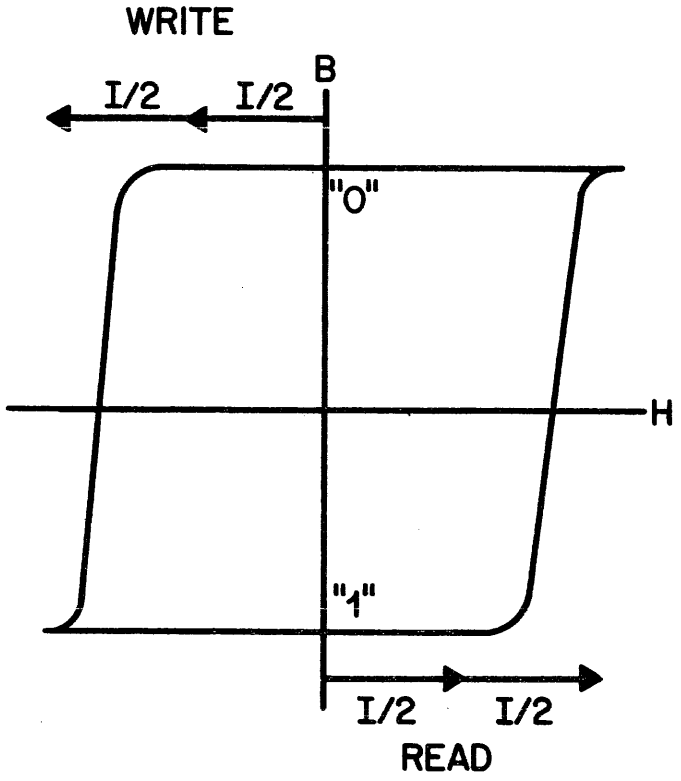
(2) The core is always saturated in one direction or the other. A change in state is required to either read or write a "1", no change indicates reading or writing a "0" (NRZI).

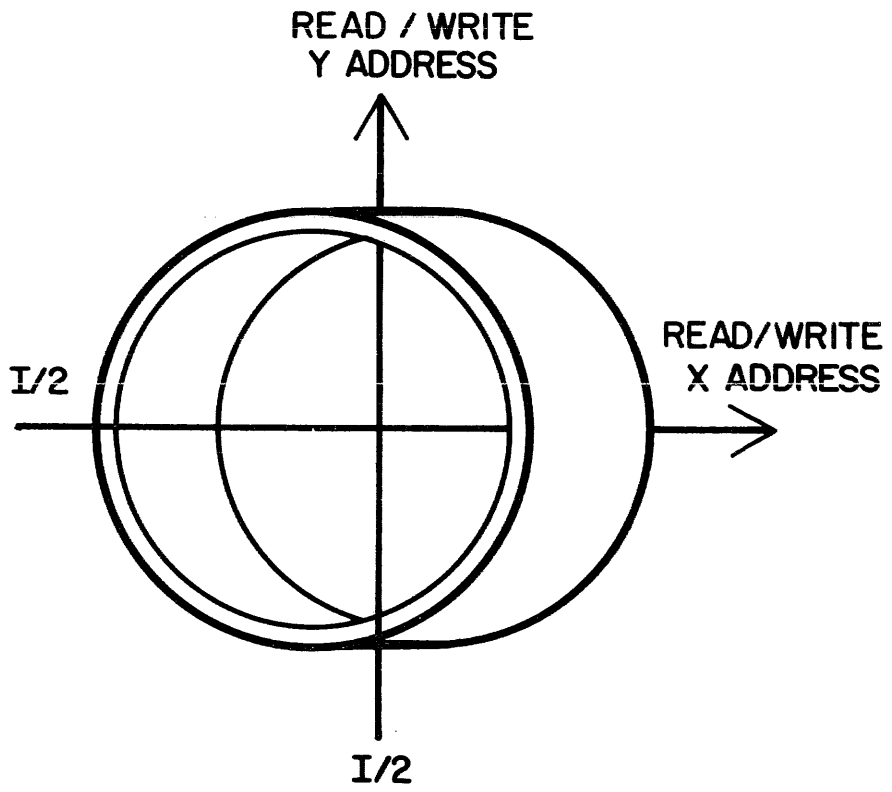
c. Read-Write Cycle (Figures 4-2 and 4-3)

(1) During the "read" cycle, the core addressed is sensed for state. If the X and Y currents change the state, a "1" will be sensed. If the X and Y currents do not change the state, a "0" will be sensed.

(2) During the "write" cycle, the core addressed may be inhibited, or not inhibited. If the core is inhibited by a reverse current (-I/2), the core cannot change states and a "0" is written into core. If the core is not inhibited, the X and Y currents change its state, and a "1" is written into core.

READ/WRITE CURRENTS



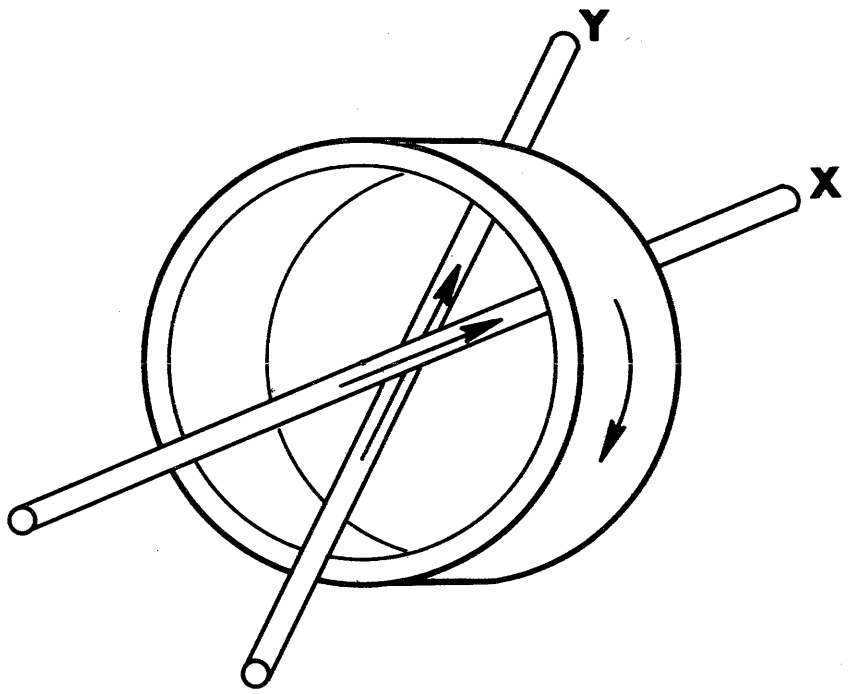


THE CORE IS ALWAYS SATURATED WHEN IN A STATIC STATE (NRZI)
A CHANGE OF STATE INDICATES READING OR WRITING A "1"

FIG. 4-1

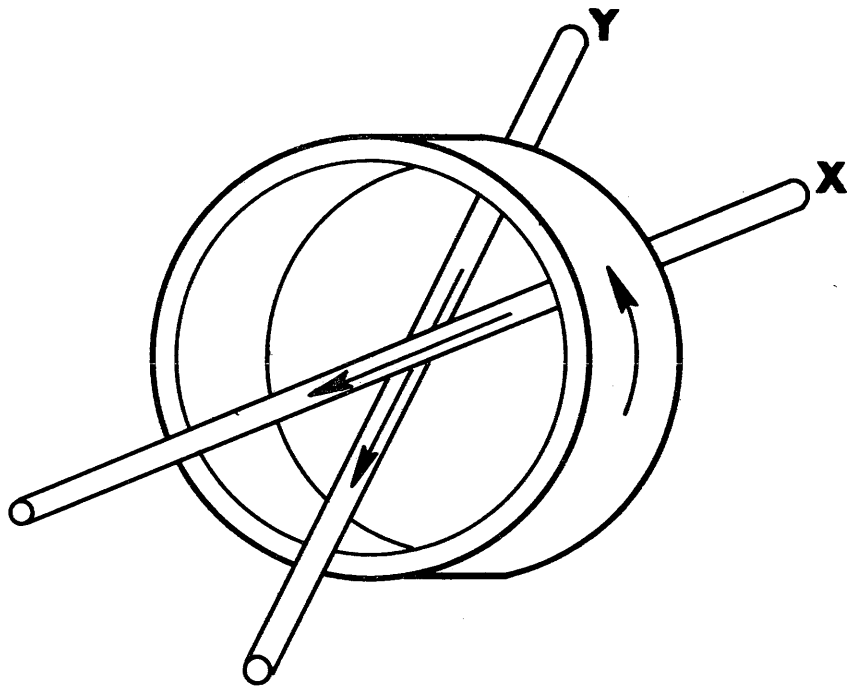
READ/WRITE CURRENTS VS CORE STATUS

READ CYCLE



MAGNETIZED IN "1" DIRECTION
READ CURRENT SWITCHES CORE

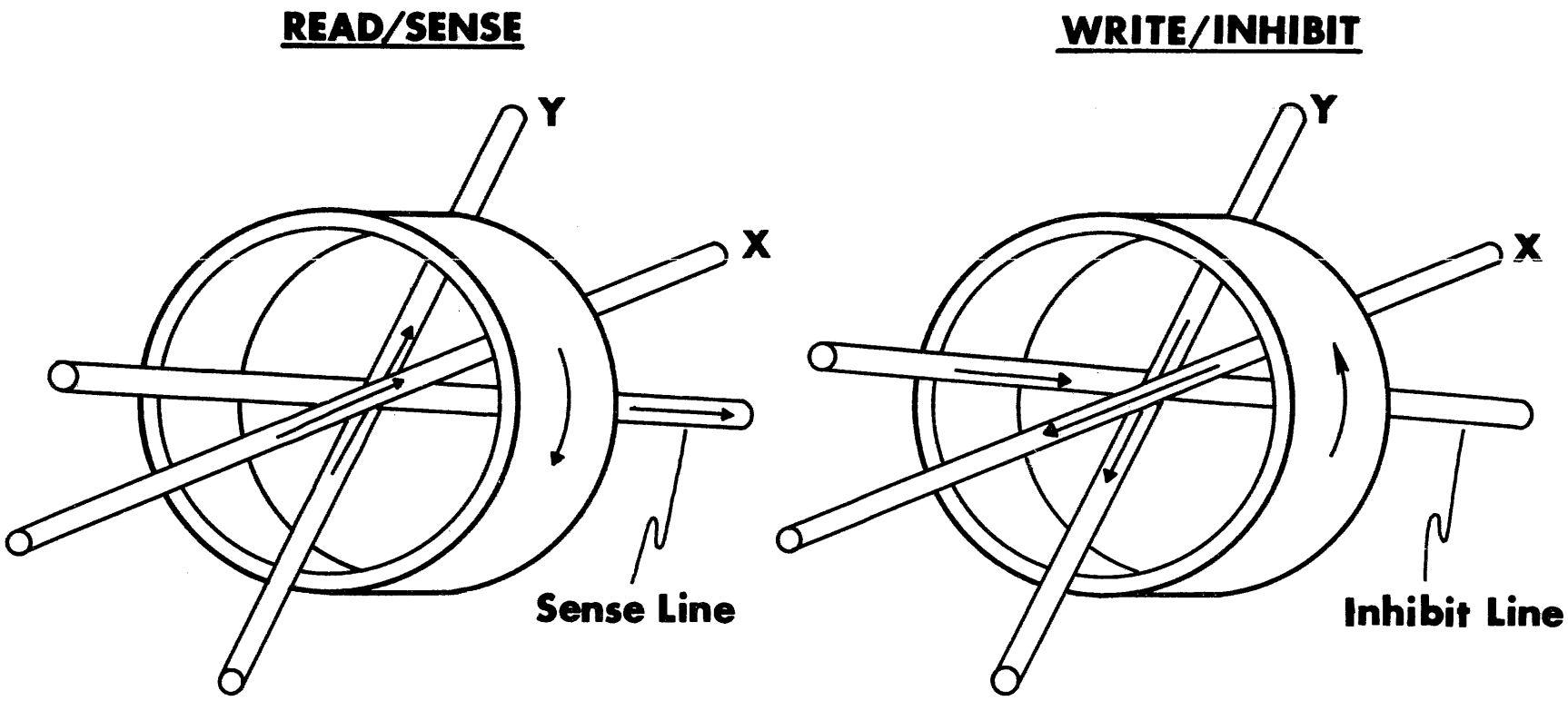
WRITE CYCLE



MAGNETIZED IN "0" DIRECTION
WRITE CURRENT SWITCHES CORE

FIG. 4-2

DETERMINING CORE STATUS



SENSE "1"

READ CURRENT SWITCHES CORE

WRITE "0"

INHIBIT CURRENT PREVENTS SWITCHING CORE

FIG.4-3

THE 4 - WIRE SYSTEM

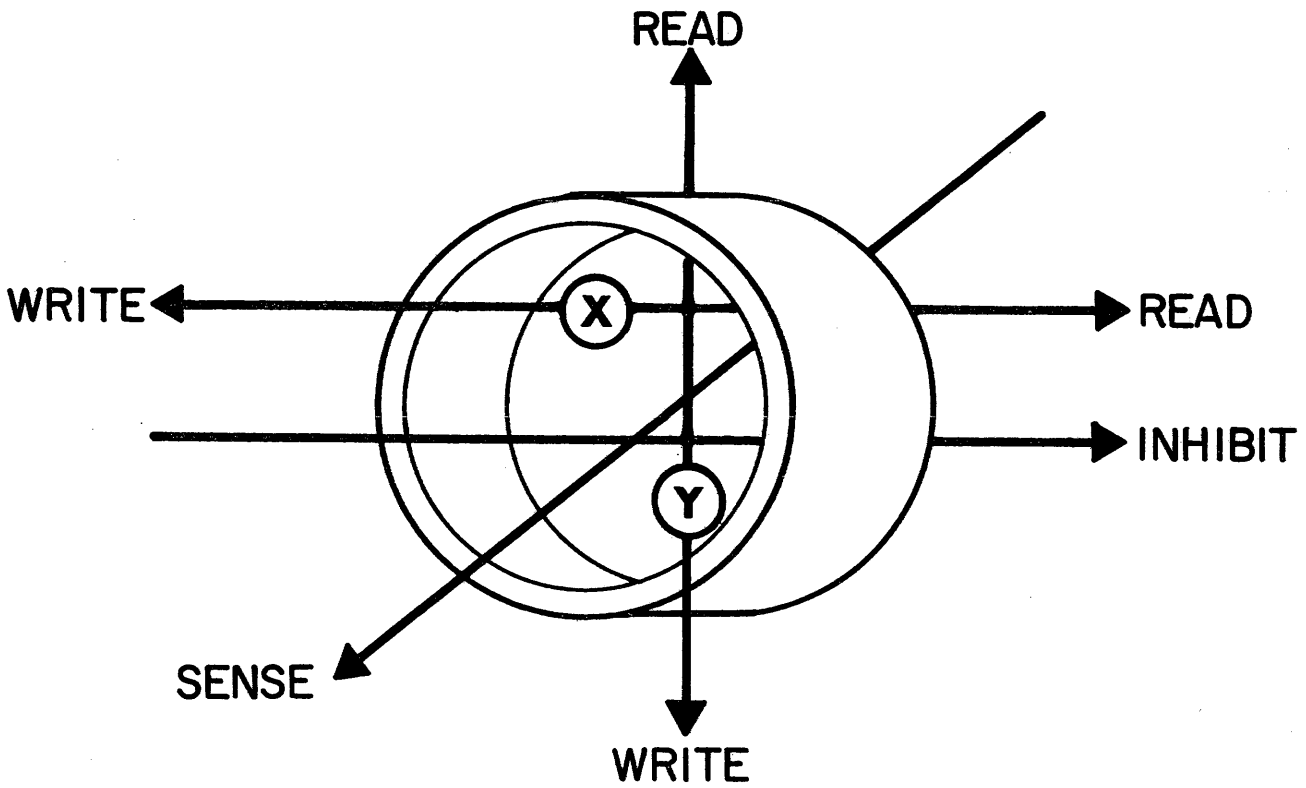


FIG. 4-4

d. The 4-Wire System (Figure 4-4)

(1) The HP 2116B/HP 2115A uses the 4-wire system:

(a) X-axis current (I/2)
(b) Y-axis current (I/2)
(c) Inhibit current (-I/2)
(d) Sense current (I)

(2) The sense wire has a current induced only when the core changes state.

2. The Core Stack

a. Core Stacks and Core Planes (Figure 4-5)

(1) The core stack has 17 core planes. There are 4, 096 cores on each plane. The 17 planes correspond to 16 bits (0-15) in the T-Register, and the parity bit from the Parity Bit Flip-Flop on the Parity Error Board (Option M2).

b. The Core Plane (Figure 4-6)

(1) A core plane contains 4, 096 cores. This corresponds to the $4,096_{10}$ ($10,000_8$) octal addresses possible with the basic 4K memory module.

(2) One, and only one, core on each plane is selected for any one octal address. The same numbered cores on all address planes are selected simultaneously. This is made possible by making each X and Y address wire common to all core planes.

(3) Each core plane also has its own unique sense and inhibit wires which are connected to the corresponding bit flip-flop in the T-Register.

c. Core Addressing (Figure 4-7)

(1) For convenience on schematics and wiring diagrams, each X and Y address wire has been designated with a unique alpha-numeric symbol. (Corresponding to the X and Y wires and octal numbers 0-7). This symbol further identifies an X or

ALL Core Stacks have 17 Core Planes

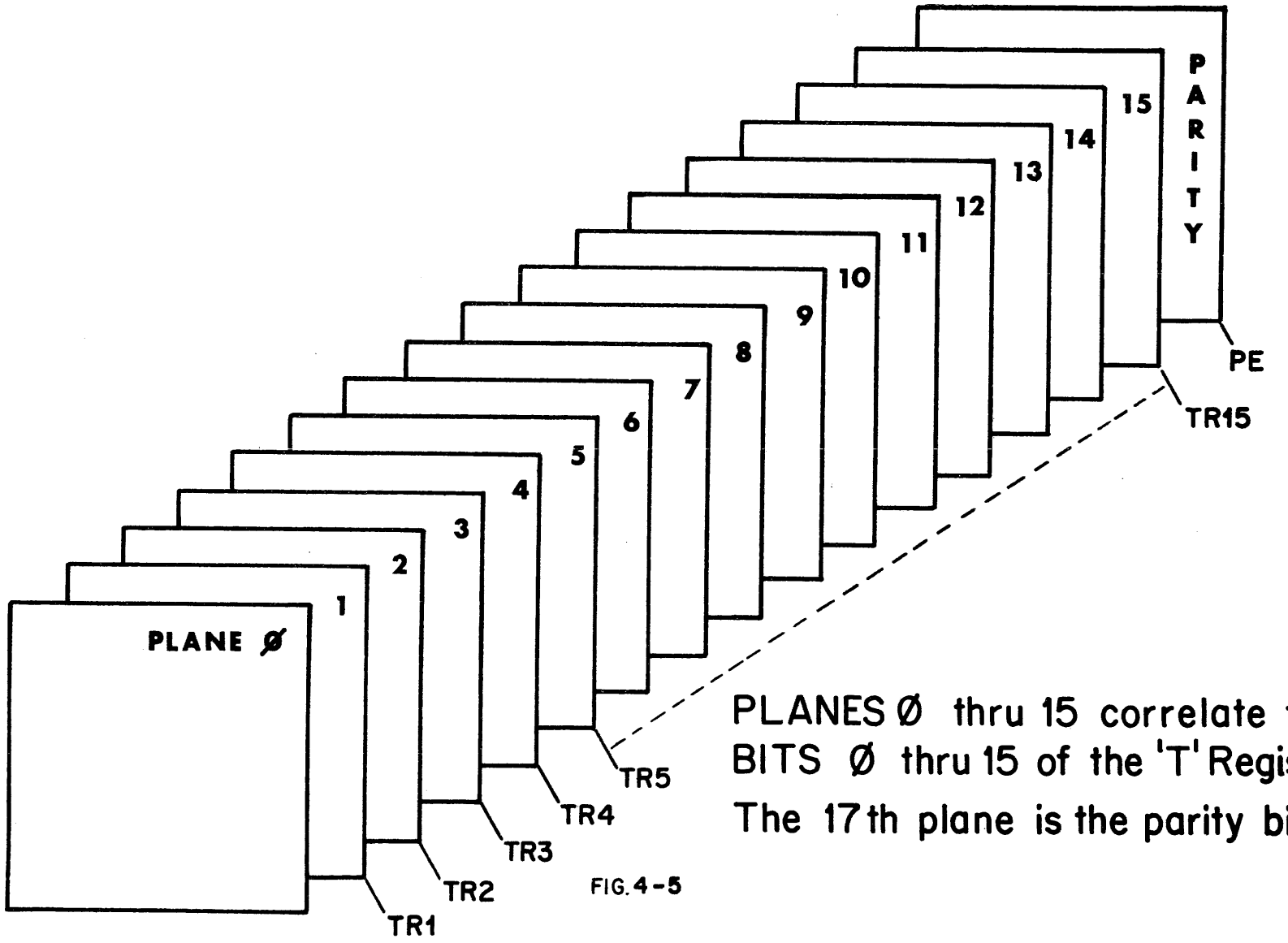
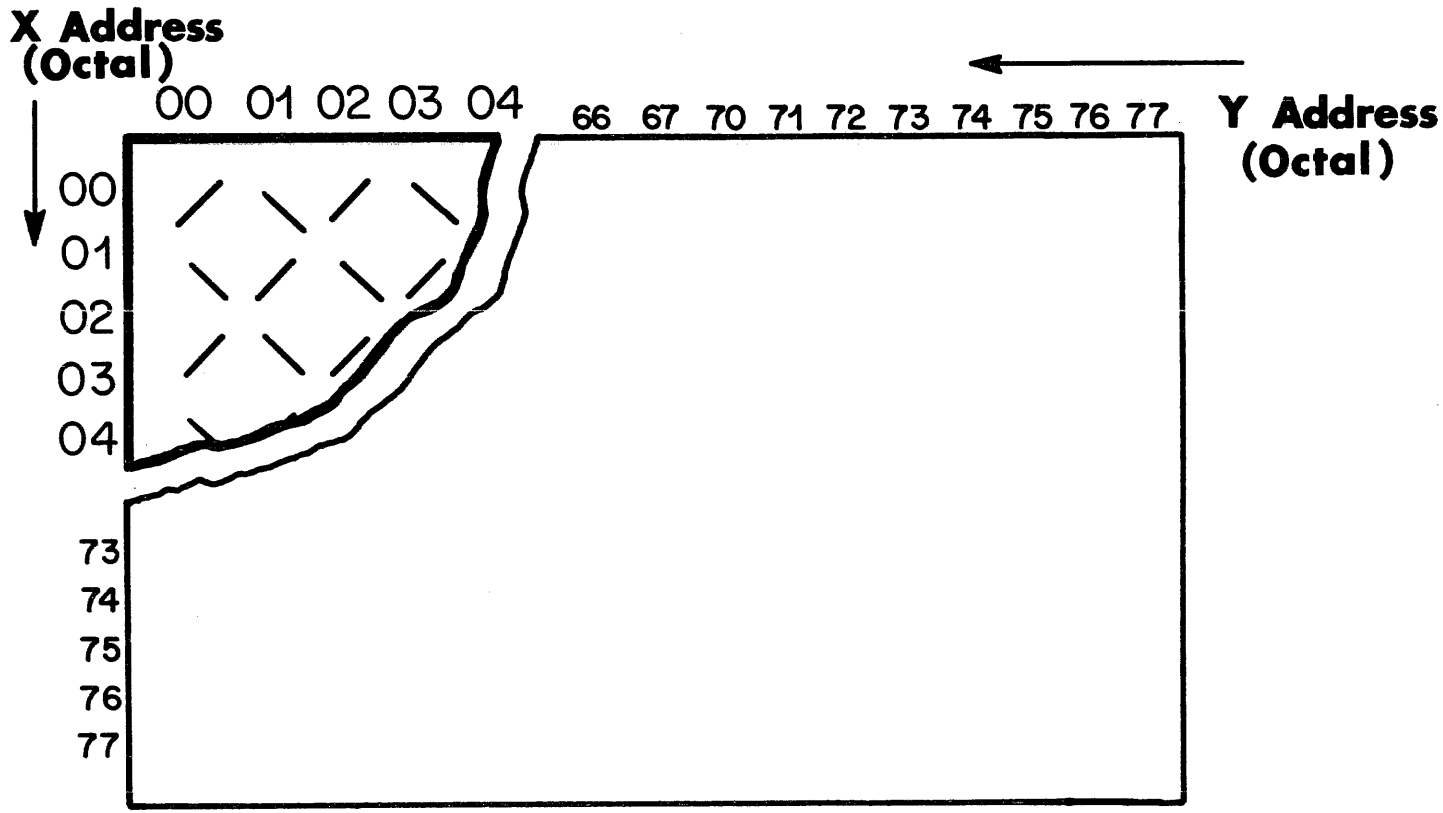


FIG. 4-5

PLANES Ø thru 15 correlate to BITS Ø thru 15 of the 'T' Register. The 17th plane is the parity bit.

THE CORE PLANE



EACH CORE PLANE CONTAINS $64 \times 64 = 4096_{10} (10{,}000_8)$ CORES

FIG. 4—6

MEMORY ADDRESS IDENTIFICATION

M-REGISTER

	Y		X	
	Dr.	Sw.	Dr.	Sw.
A	7	4	0	1
B	7	5	7	6

CØ – C7 ARE DRIVERS
CCØ – CC7 ARE SWITCHES

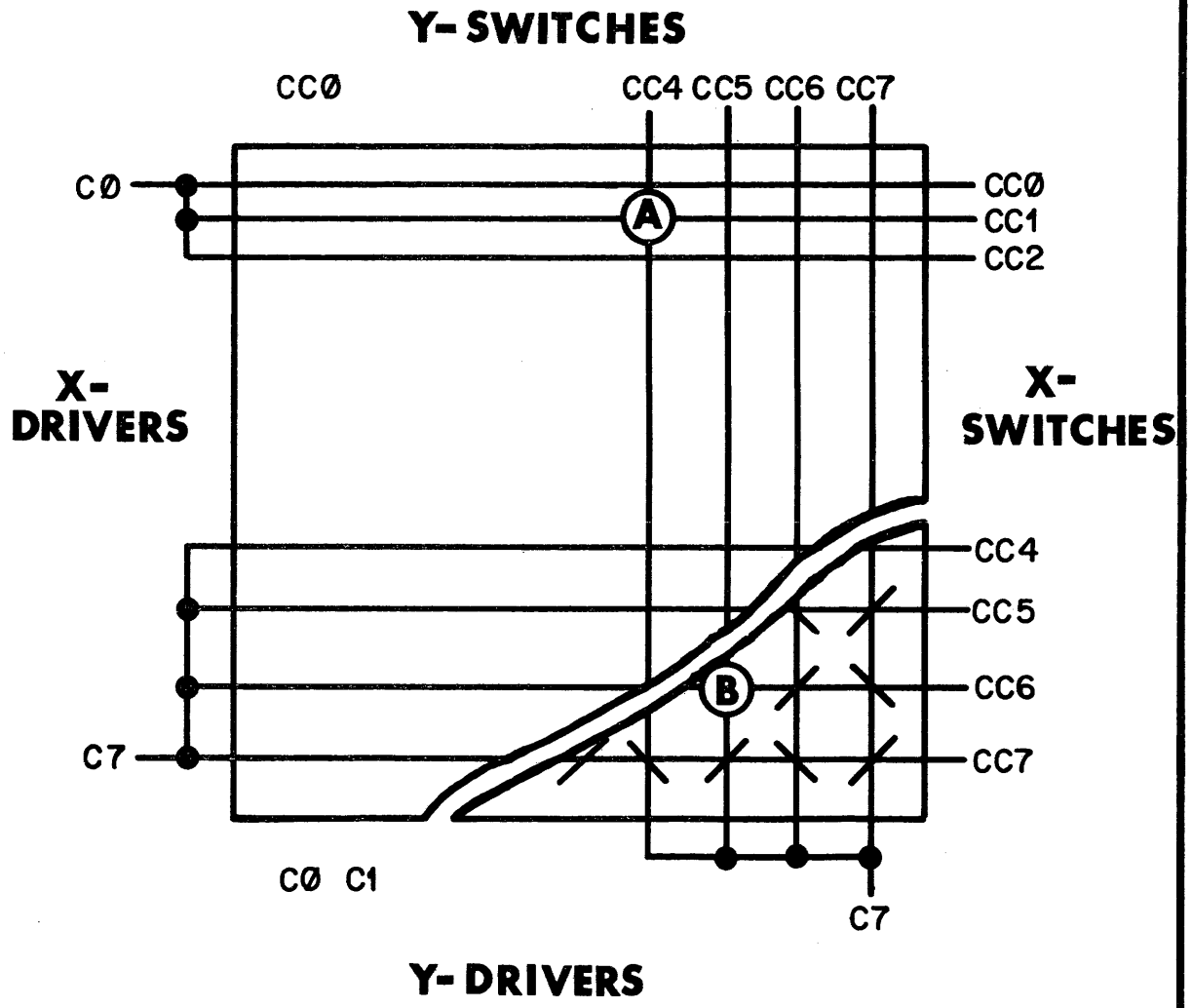


FIG. 4-7

Y wire Driver or Switch. In general, the number of switches and drivers required to select 4, 096 addresses is 64 (64 x 64 = 4096). But by arranging the switches and drivers in a unique matrix, the number of switches and drivers is reduced to only 8 each.

8 X-drivers times 8 X-switches = 64
8 Y-drivers times 8 Y-switches = 64
and 64 x 64 = 4, 096 addresses

(2) For convenience, we label switches as XCCØ-XCC7 and drivers as XCØ-XC7. The same technique is applied for the Y drivers and switches. As an example, to select octal address 07401 we select wires:

YC7 7
YCC4 4
XCØ Ø
XCC1 1

It is, of course, assumed that the required binary-to-octal conversion has already been accomplished.

d. Reading/Writing Core

(1) The electronics shown in Figure 4-8 for bit 9 is duplicated for each bit in the T-Register.

(2) Reading and writing of core must be controlled. That is, we cannot read and write at the same time less our information be trivial. Memory timing pulses such as MST and MIT prevent this occurence.

(3) Reading core is enabled by the MST signal (memory strobe timing). Similarly, writing core is controlled by the MIT signal (memory inhibit timing).

(4) Note that a "1" read from core sets FF9, while a "0" read from core has no effect (remembering the T-Register is always cleared at TØ). Similarly, when TR9 is reset (Ø), memory writing is inhibited.

TYPICAL DATA SENSE AND INHIBIT

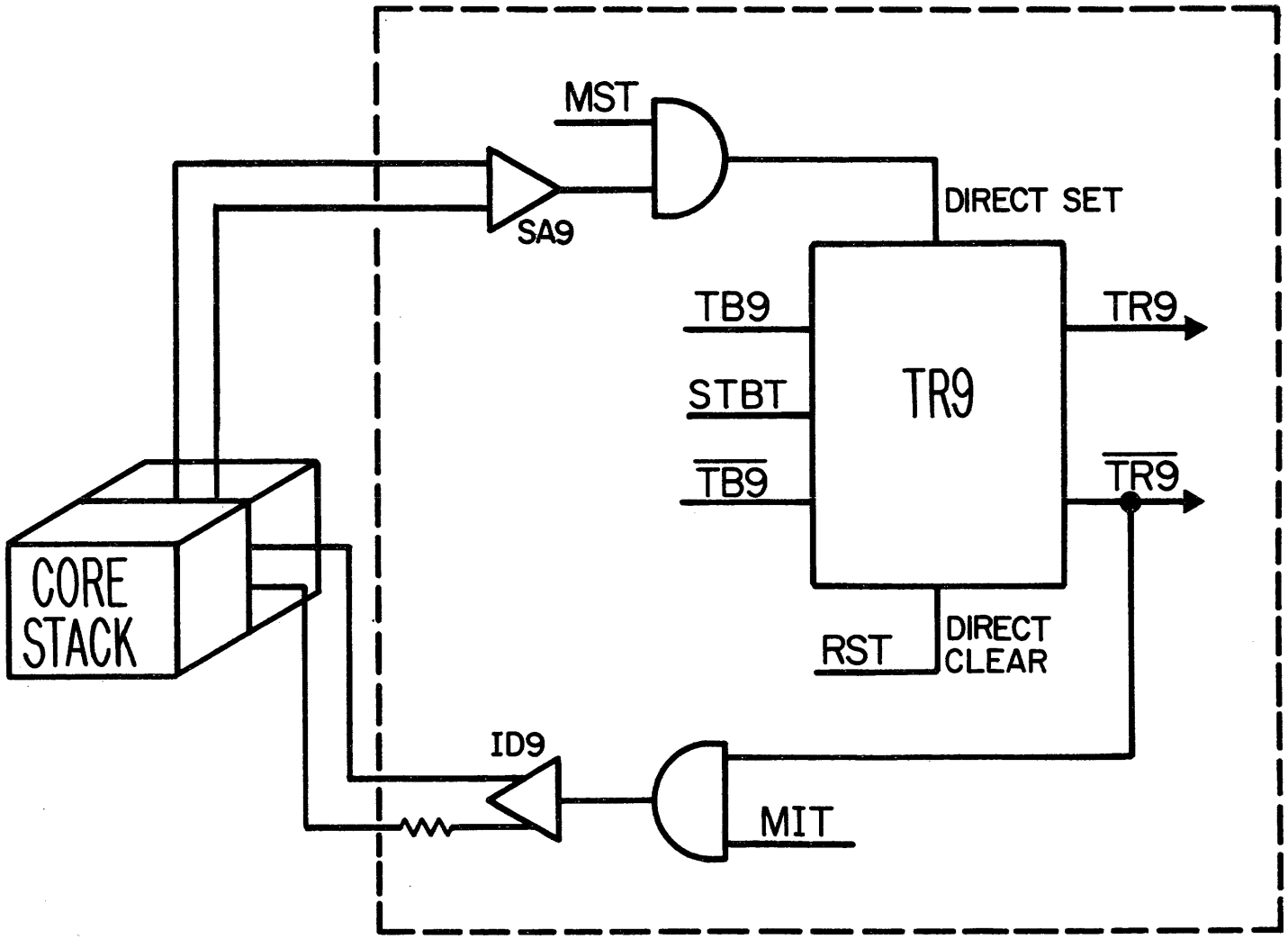


FIG. 4-8

B. HP 2116B/HP 2115A OPERATIONAL BLOCK DIAGRAM

1. Memory Addressing (Figure 4-9)

a. HP 2116B Addressing

(1) Memory addressing in the HP 2116B is facilitated by using a Memory Module Decoder board (MMD) which senses bits 12 thru 14 and selects either the lower 4K memory stacks or the upper 4K memory stacks. This follows from our paging index scheme where:

Bit 12 (Ø/1) = $4,096_{10}$ or 8, 192 addresses
Bit 13 (Ø/1) = 8, 192 or 16, 384 addresses
Bit 14 (Ø/1) = 16, 384 or 32, 768 addresses

Note that any combination of bits 12-14 may be used to select any 4K memory stack throughout the range 4K to 32K.

(2) The memory address is decoded on the X and Y Driver/Switch.

(3) A Diode Matrix then selects the appropriate X and Y wires in the memory stack to select the core location. The Driver-Switches determine which X and Y wires in the diode matrix will be selected for any given octal code.

(4) The Sense Amplifier and Inhibit Driver faciliate reading and writing memory.

b. HP 2115A Memory Addressing (Figure 4-10)

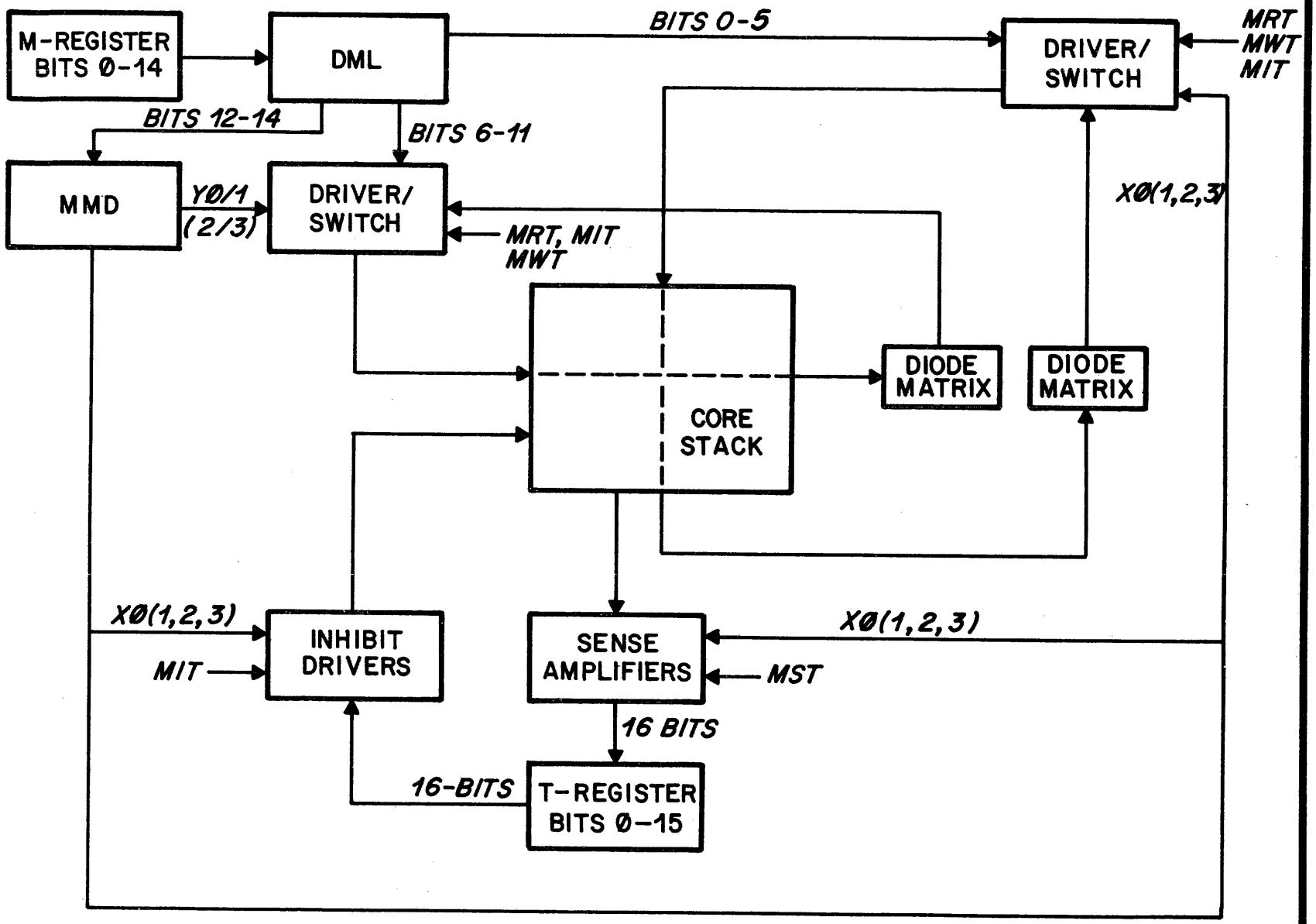
(1) Memory addressing in the HP 2115A is similar to that used for the HP 2116B except:

(a) The HP 2115A has capability for 8, 192 addresses only.

(b) The HP 2115A does not require a MMD board.

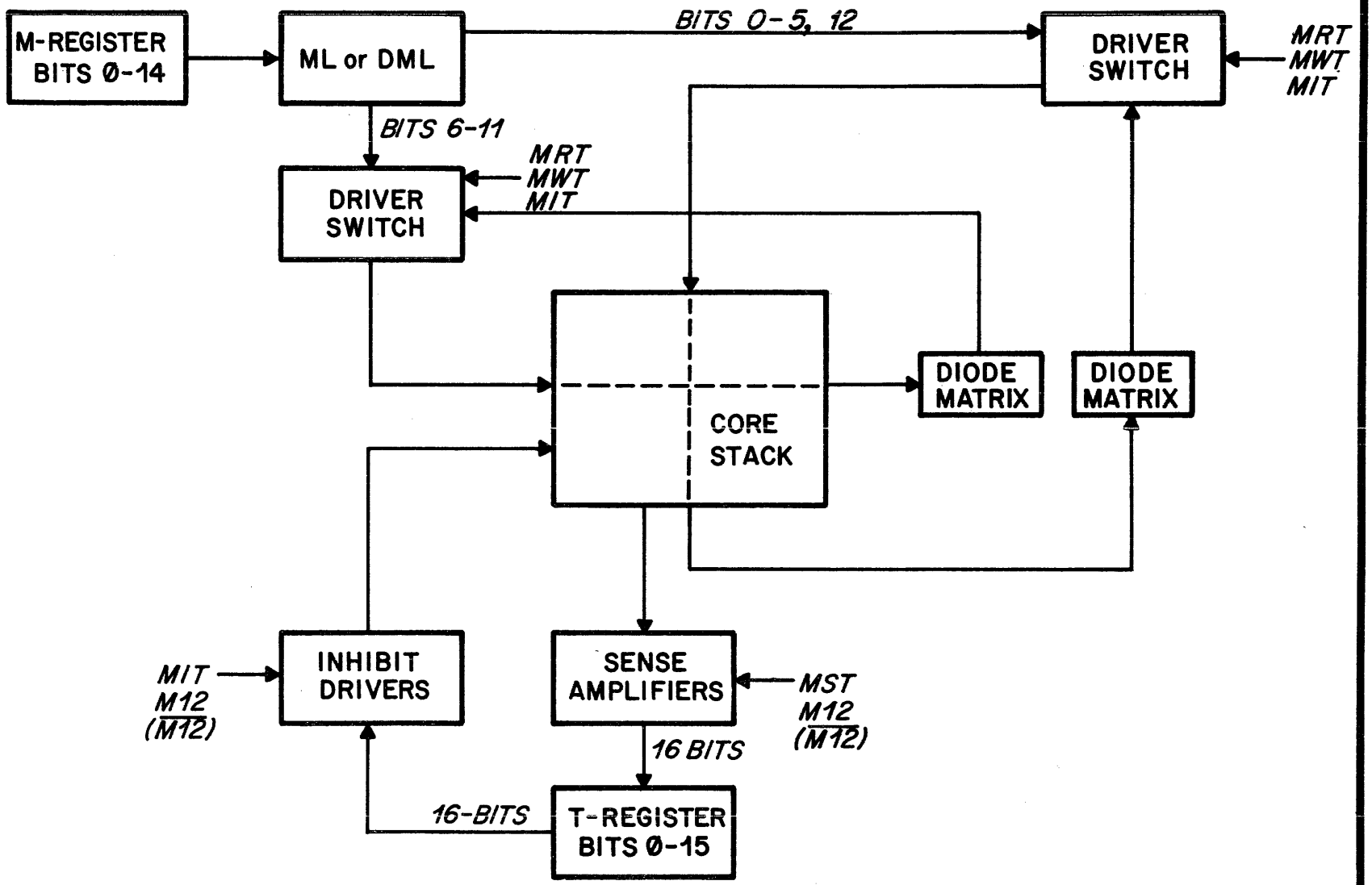
(2) The HP 2115A uses the same Diode Matrix and Sense Amplifiers as the HP 2116B.

(3) The HP 2115A uses a different core stack and Driver/Switch board.



HP 2116B
MEMORY BLOCK DIAGRAM

4-9



HP 2115A MEMORY BLOCK DIAGRAM

2. Memory Timing (Figure 4-11)

a. Basic Timing

(1) The MRT signal is 460 ns long. The MST pulse is only 100 ns long. The MIT signal is 500 ns long and the MWT signal is 400 ns long. Thus, over half (9/16) of the basic machine cycle is used for accessing memory.

(2) The basic machine cycle of the HP 2116B is 1.6 μs. The basic machine cycle for the HP 2115A is 2.0 μs.

b. Extended Timing

(1) The basic machine cycle must be stretched to 2.0 μs or 2.5 μs (HP 2115A) when implementing an ISZ instruction. This is required since memory accessing must be delayed during the "increment" operation. The MWT and MIT signals are delayed 400 ns to allow this operation to take place.

3. Memory Addressing Logic

a. Addressing (Figure 4-12)

(1) Since each core stack has 64 X-lines and 64 Y-lines, the M-Register must supply 6 bits of addressing data for each X and Y octal address ($2^6 = 64$). Bits 0-5 address the X-lines and bits 6-11 address the Y-lines. Bits 12-14 are used to select the module.

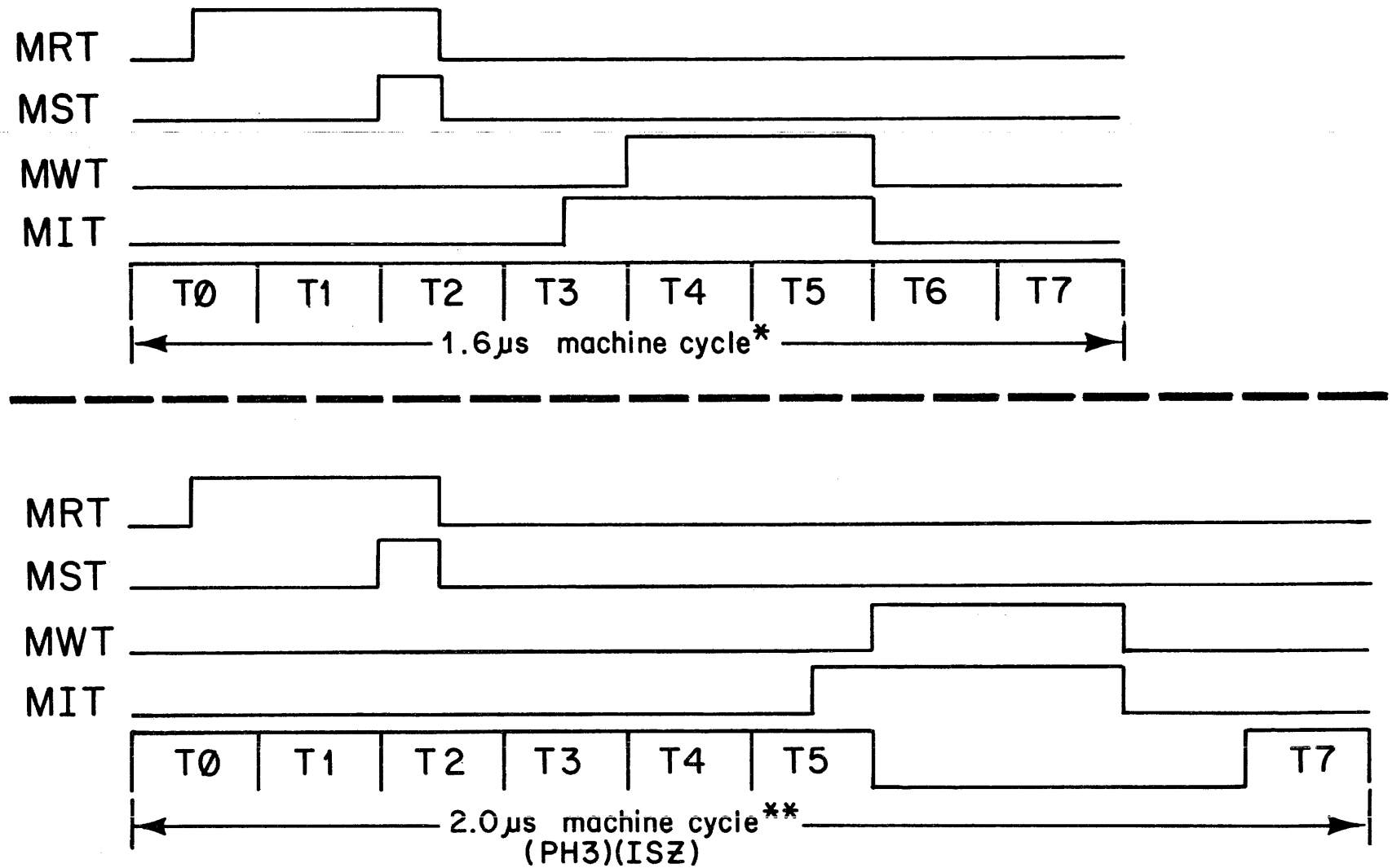
(2) Memory address decoding is done by the Driver/Switches and a decoding network.

b. Addressing Logic Diagram (Figure 4-13)

(1) The addressing logic for reading/writing upper and lower core stacks is shown in Figure 4-13.

(a) During each memory cycle, one address coordinate is selected by outputs from the Driver/Switch Boards. The X wire and the Y wire comprising the address coordinate carry read or write half-currents through the cores of the

MEMORY TIMING



*2.0µs in HP2115A
**2.5µs in HP2115A

FIG. 4-11

Memory Address Decoding Logic

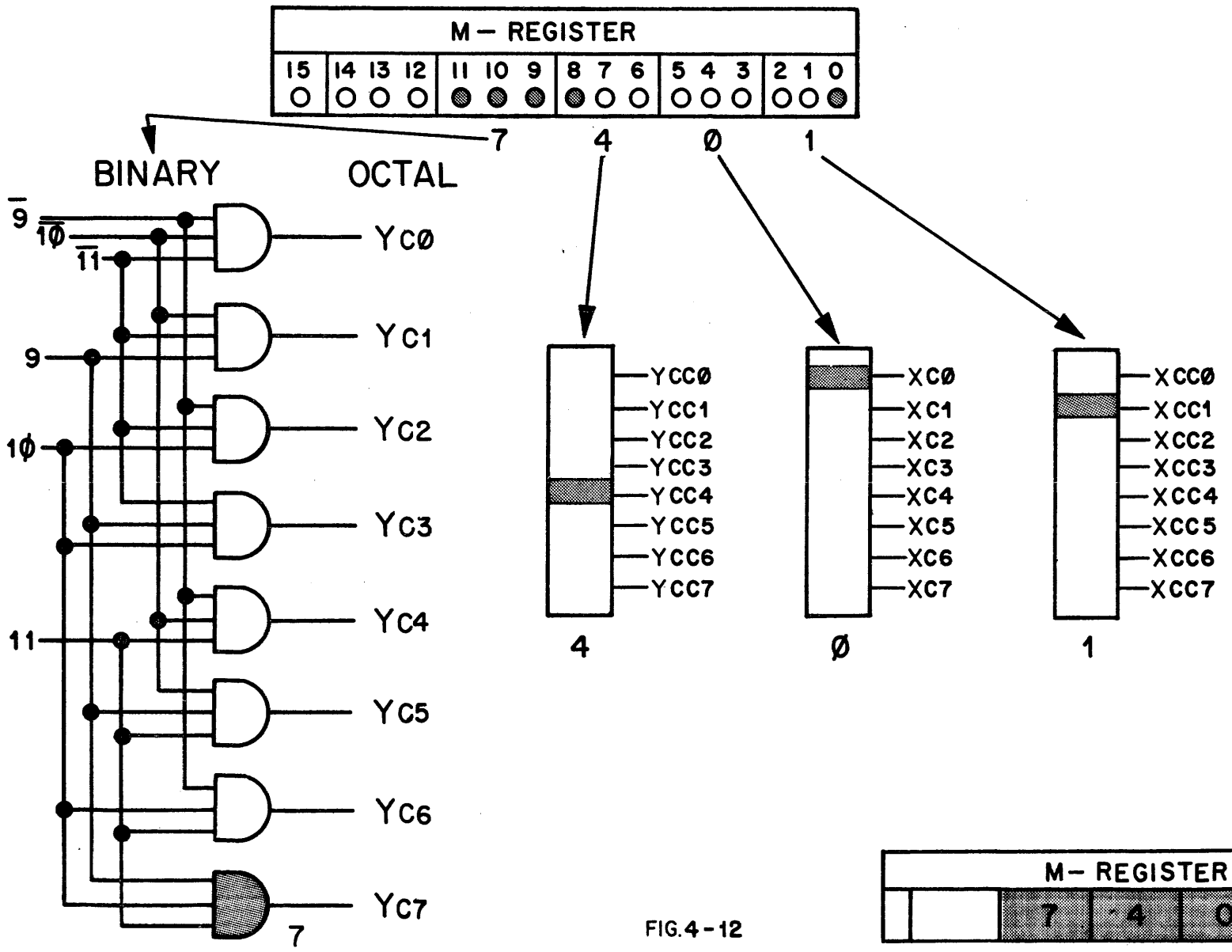


FIG. 4-12

Simplified Memory Addressing

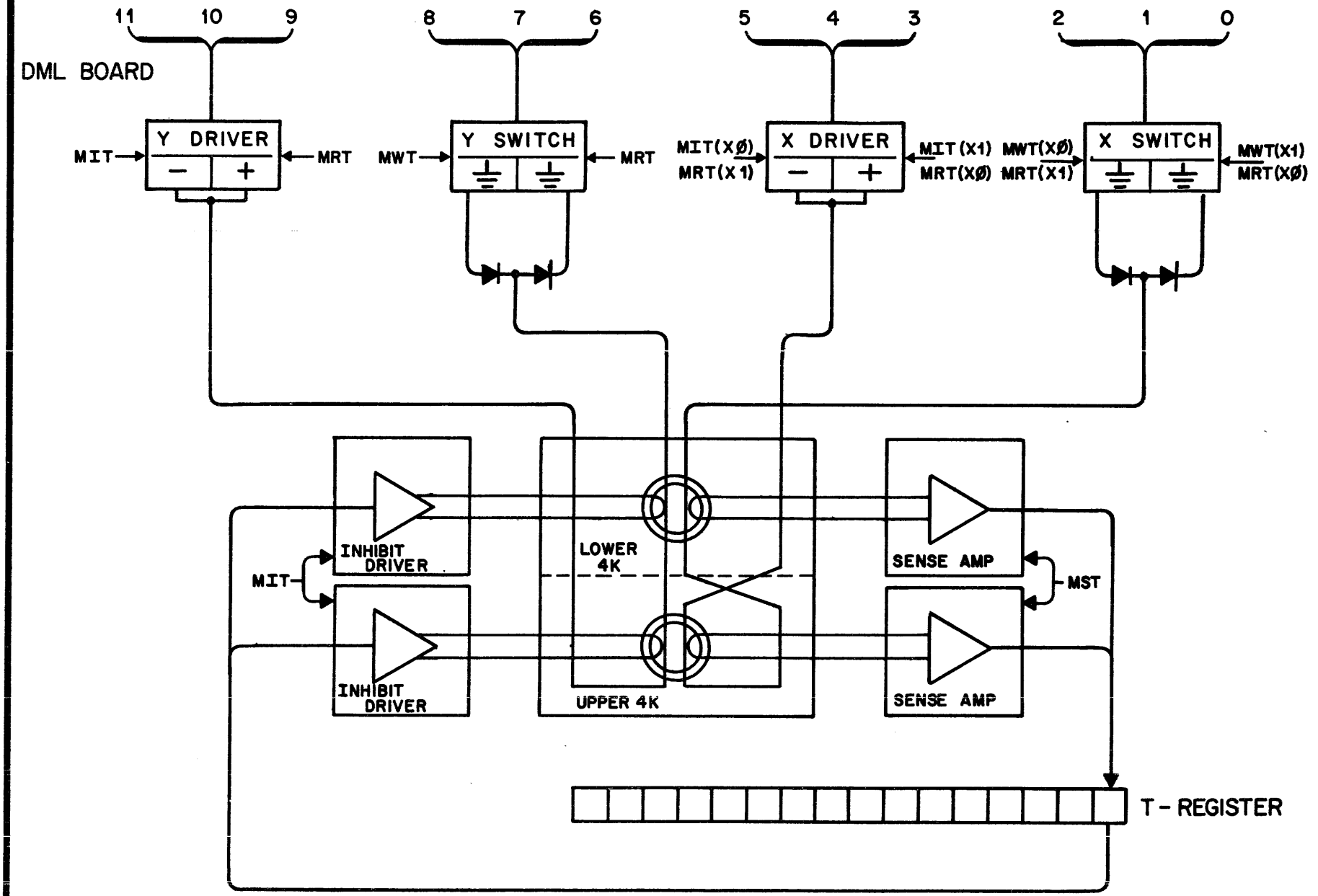


FIG. 4-13

two memory modules. The direction in which the half currents flow at the points where the two wires intersect, and hence their direction of flow through the cores of the memory locations, will either be coincident in one direction, causing data to be read out of the cores, or coincident in the other direction, causing data to be written into the cores. A third possibility is that the half currents will be anti-coincident (flowing in opposite directions through the cores), in which case they inhibit, or cancel and have no effect on the cores of the memory locations. This latter possibility is used to advantage to permit two memory modules to be serviced individually by any selected X/Y wire pair forming an address coordinate within the 8K core memory module. In other words, whenever current flow is coincident through the cores of one memory module on the address coordinate, current flow is anti-coincident through the cores of the other memory module on the address coordinate.

(b) From the discussion so far, it is evident that access to any memory location within the 8K core memory module is possible by selecting the one X wire and the one Y wire that form the address coordinate for the desired memory location. This selection is accomplished electronically during each memory cycle when address bits 0 through 11 are decoded by binary-to-octal decoders on Driver/Switch Boards. The decoded octal output from these decoders selects the two ends of one X wire loop and the two ends of one Y wire loop. The wires selected form the address coordinate for the memory location corresponding to the address stored in the M-Register. When the wires are selected, the normally open ends of the wires are completed through switching and driving circuits on the Driver/Switch Boards, and each wire carries read or write half currents through the cores of

all memory locations through which it threads. However, only the cores of two memory locations (addresses 05270 and 15270, for example) are threaded by both active X and Y wires and receive both the X and Y half currents. Further, the X and Y wires are threaded through these two locations in such a manner that both half currents flow in the same direction through the cores of only one memory location, and in opposite directions through the cores of the other memory location. Therefore, although the active or selected X and Y wires during any given memory cycle actually form the address coordinates for two memory locations (one in the lower position cores and one in the upper position cores), only the half currents flowing through one location are coincident and enable data to be read out of, or written into, the core positions for that address. The same half currents which flow simultaneously through the second memory locations are anti-coincident and effectively cancel each other with no net effect on the cores of that location. However, by reversing the direction of current flow in either the X-wire or the Y-wire, the situation will be reversed. That is, the half currents flowing through the first memory location will now be anti-coincident and cancel, and the current flowing through the second location will be coincident causing data to be transferred into or out of that location. Therefore, memory access is controlled in part by X and Y wire selection, and in part by the direction in which current flows in the selected wires. Access control, together with read/write control, are functions of the output currents received from the Driver/Switch Boards.

(c) The combined function of the Driver/Switch Boards is to furnish the 8K core memory module with any one of 16, 384 unique X/Y current output combinations selected

individually on command of control signals from the M-Register and the Timing Generator Board. Each selectable output is unique, in that it provides access to a discrete memory location and furnishes either read or write currents to the cores of the selected address. Therefore, each X/Y current output consists of a X half-current output from one Driver/Switch flowing in a specific direction on one of 64 X wires, and a Y half-current output from the other Driver/Switch flowing in a specific direction on one of 64 Y wires.

4. Matrix Logic (Figures 4-14 and 4-15)

a. As shown in Figure 4-14, X lines CCØ and C7 are routed through diode matrix intersection 56 to the lower and upper cores. The Y-lines CC2 and C5 are routed through intersection 42 to the lower and upper cores. Intersections 56 and 42 are shown more clearly in Figure 4-15.

C. DETAILED MEMORY THEORY

1. Direct Memory Logic (DML) (Figure 4-16)

a. Purpose

(1) The purpose of the DML board is two-fold:

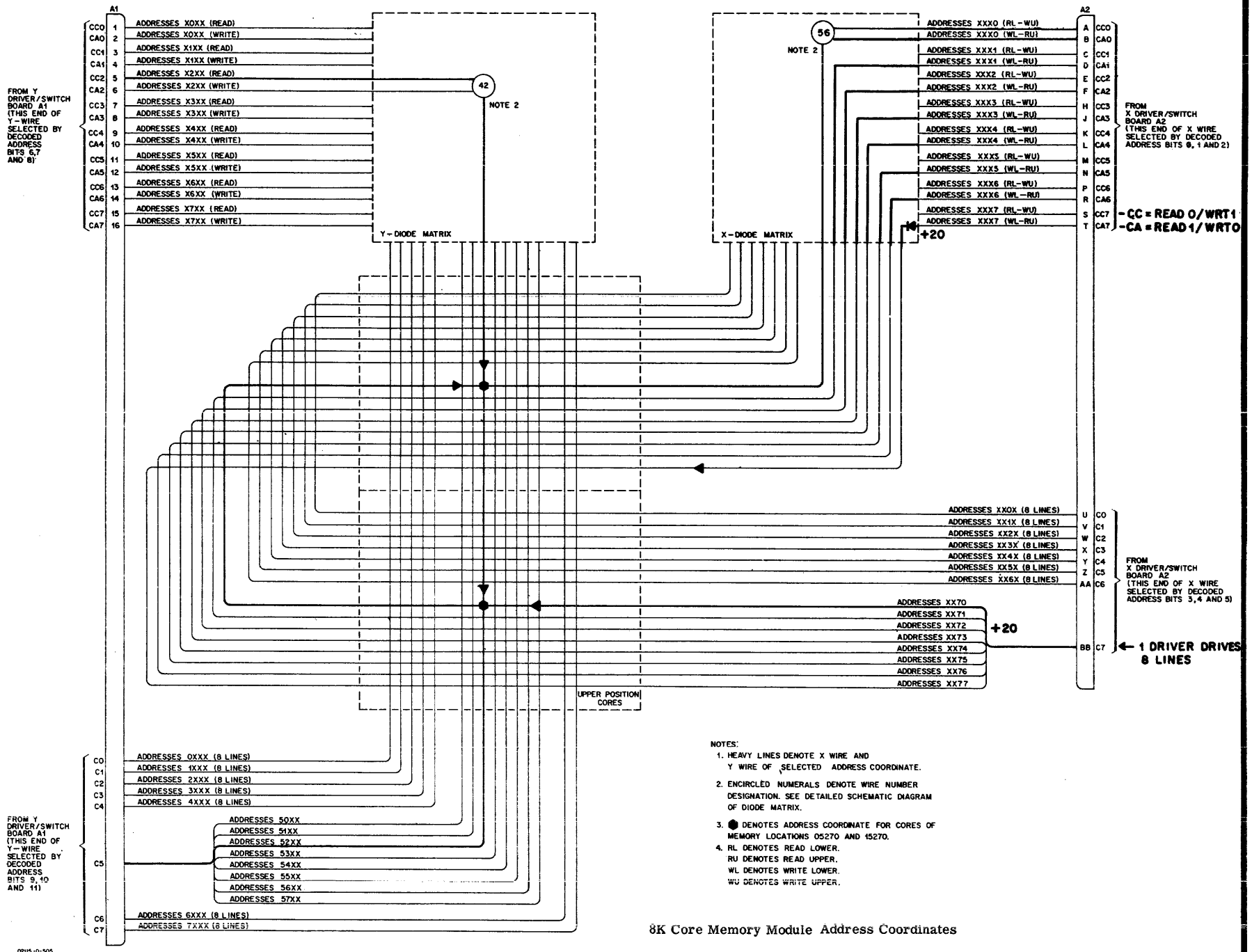
(a) it couples arithmetic function signals to the Arithmetic Logic boards from either the computer or the EAU (Extended Arithmetic Unit) board.

(a) it couples address bits to the Driver/Switches from either the Arithmetic Logic boards or the DMA (Direct Memory Access) board.

(2) The same type board is used in both the HP 2116B and HP 2115A.

b. Logic

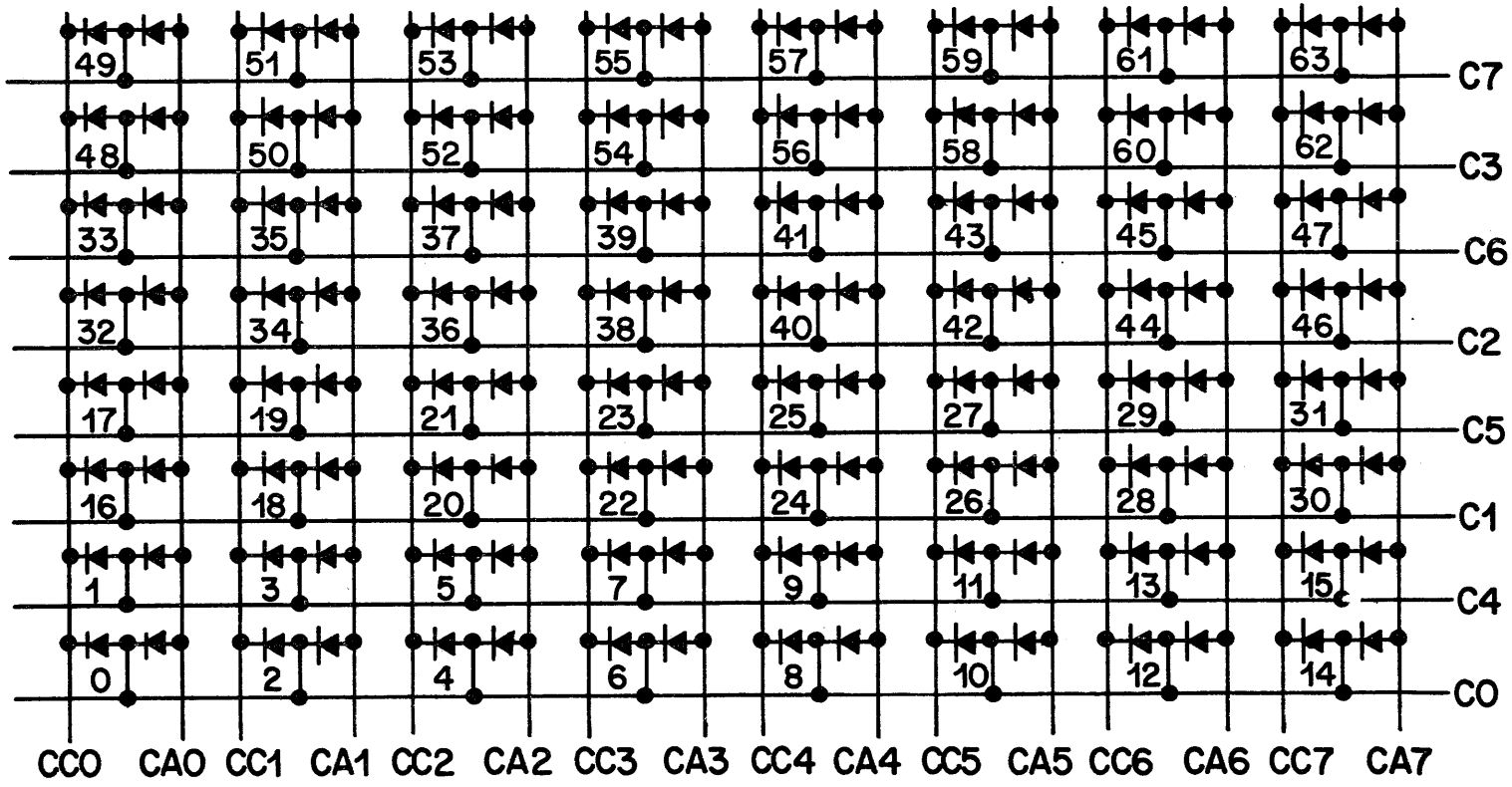
(1) As shown in Figure 4-16, this board accepts arithmetic function signals $\overline{\text{SLME}}$, $\overline{\text{SRME}}$, $\overline{\text{SL14E}}$, $\overline{\text{EOFE}}$ or $\overline{\text{CMFE}}$ from the computer and SLMH, SRMH, SL14H, EOFH or CMFH signals from



NOTES:
1. HEAVY LINES DENOTE X WIRE AND Y WIRE OF SELECTED ADDRESS COORDINATE.
2. ENCIRCLED NUMERALS DENOTE WIRE NUMBER DESIGNATION. SEE DETAILED SCHEMATIC DIAGRAM OF DIODE MATRIX.
3. ● DENOTES ADDRESS COORDINATE FOR CORES OF MEMORY LOCATIONS 05270 AND 15270.
4. RL DENOTES READ LOWER.
   RU DENOTES READ UPPER.
   WL DENOTES WRITE LOWER.
   WU DENOTES WRITE UPPER.

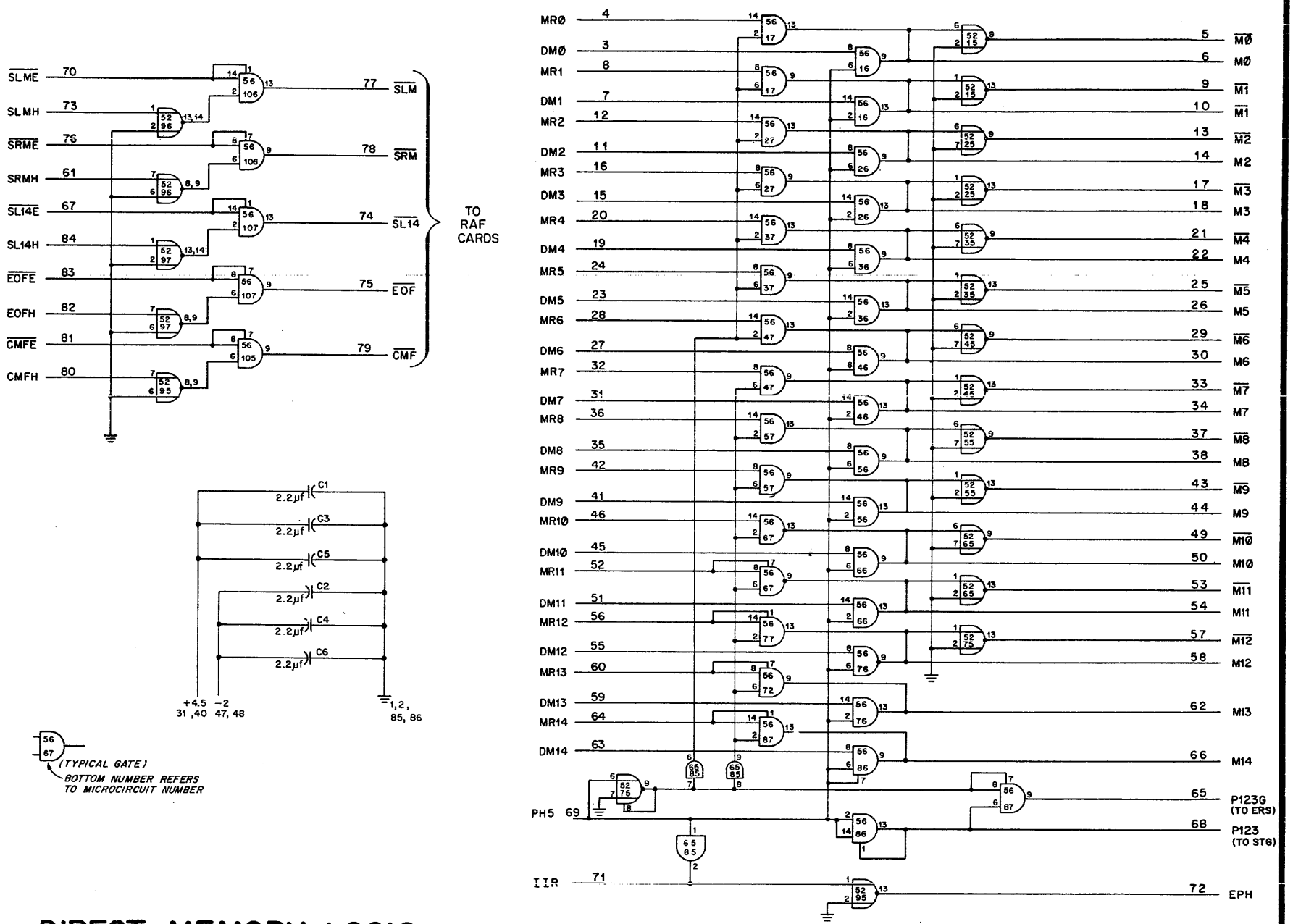
8K Core Memory Module Address Coordinates

FIG 4-14



COMMON ANODE FOR READ, COMMON CATHODE FOR WRITE

FIG. 4-15



DIRECT MEMORY LOGIC

FIG. 4-16

the EAU. Either $\overline{\text{SLME}}$ going low or SLMH going high will make the SLM output at pin 77 low. The other signals work similarly.

(2) Address bits MRØ-MR14 are supplied by the computer while address bits DMØ-DM14 are supplied by DMA. If Phase 5, then all DMA output gates are enabled and DMA address information from DMA is entered to the computer. Phase 5 also inhibits the computer address bits at the same time. The Phase 5 signal also enables a pseudo P123 signal (pin 68) which facilitiates (during DMA interrupts) clearing the T-Register.

2. HP 2116B Memory Module Decoder (MMD) A2 (Figure 4-17)

a. Purpose

(1) The MMD board is used in the HP 2116B only since the HP 2115A is limited to 8K and it is not needed for that computer.

(2) The purpose of the MMD board is to sense M-Register bits 12-14 and select the proper 4K memory module. This board also senses bits M6-M11, the LPS (Loader Protect) signal, and MPT (Memory Protect) signals to determine which memory modules are to be protected for the ABL (higher 77 locations).

b. Logic

(1) As shown in Figure 4-17, bits 12-14 are sensed through a decoding network and used to enable addressing signals YØ/1, Y2/3, XØ, X1, X2 and X3.

(a) These addressing signals are routed as follows:

Signal	Selected Memory Module	Destination
YØ/1	4K-8K	Y Driver/Switch 0/1
Y2/3	8K-16K	Y Driver/Switch 2/3
XØ	4K	X Driver/Switch 0/1
X1	8K	X Driver/Switch 0/1
X2	12K	X Driver/Switch 2/3
X3	16K	X Driver/Switch 2/3

(b) The X signals are also routed to the Inhibit Drivers and Sense Amplifiers as follows:

Signal	Memory Module	Destination
XØ	4K	SAØ and IDØ
X1	8K	SA1 and ID1
X2	12K	SA2 and ID2
X3	16K	SA3 and ID3

(c) As an example, with $\overline{\text{MMD14}}$ and MMD13, gate MC15B will provide the Y2/3 signal (via pin 10) to the 12K-16K Y Driver/Switch (Y2/3). Gate MC45A will then provide the X2 signal (via pin 8) to the 12K X Driver/Switch (X2/3). This same signal (X2) will enable the 12K Sense Amplifier (SA2) and the 12K Inhibit Driver (ID2).

(d) The partial page address decoded on this board (Y2/3) and X2) will be decoded further (with bits 0-11) on the X and Y Driver/Switches to select one and only one octal address. The MMD board merely selects the module (2 in this case for 12K).

(e) A few peculiarities concerning the inputs to the MMD are:

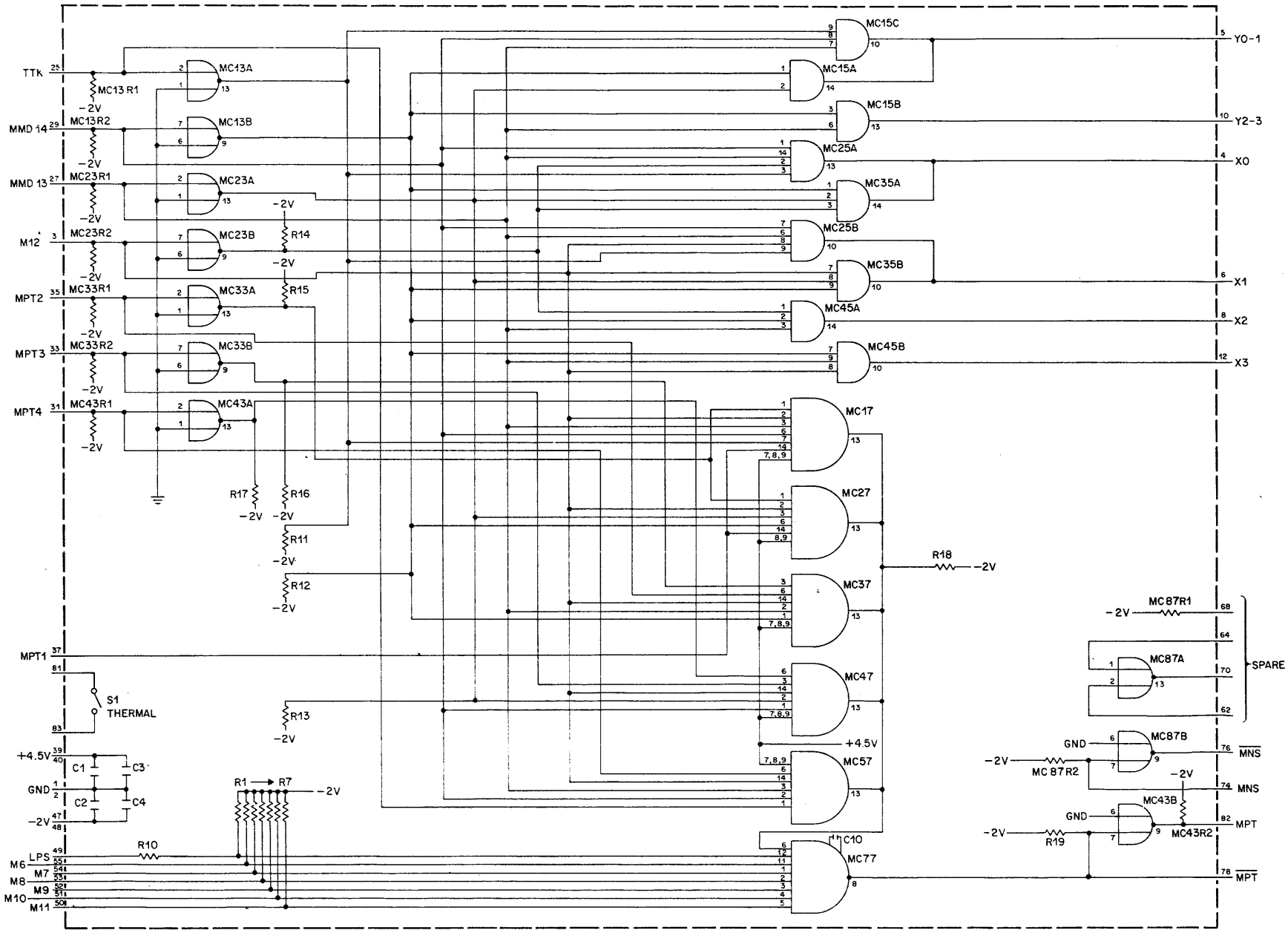
TTK - This signal is provided by the memory extender and will be true only if the machine is equipped with 32K of memory.

MMD14 - This signal is routed from the DML board to the MMD board via the memory extender. Bit 14 is only required in order to decode 24K-32K addresses in which case an extender would be present.

MMD13 - This signal is memory address bit 13 which is routed from the DML board thru the SA-2 board to MMD. This bit is required to decode an address in a 16K module. If 16K of memory is installed the signal will be applied to the MMD.

MPT1 - This signal from Inhibit Driver Ø indicates that 8K of memory is present.

MPT2 - This signal from Inhibit Driver 2 indicates that 16K of memory is present.



MEMORY MODULE DECODER

FIG. 4-17

MPT3 & MPT4 - These signals from the memory extender indicates that 24K or 32K(respectively) of memory is present.

(2) Gate MC43B enables the MPT signal (via pin 82) to the Parity Error board and gate MC77 enables the $\overline{\text{MPT}}$ signal (via pin 78) to the STG board. The MPT signal is true when the ABL locations are addressed and the LOADER switch is in the PROTECTED position. Gates MC17, 27, 37, 47 and 57 function to force the loader protected region to the highest memory module.

3. HP 2115A Driver/Switches (Refer to Logic Diagram)

a. Purpose

(1) The purpose of the X (A2) and Y (A1) Driver Switches in the HP 2115A is to select one, and only one, core location for any given octal address. Since this machine is limited to 4K and has no MMD board, bit 12 is sensed on X Driver/Switch board only to select the lower (4K) or upper (8K) memory module. Bits 0-5 are sensed on the X Driver/Switch and, with bits 6-11 on the Y Driver/Switch, the complete binary to octal decoding is done.

b. Logic

(1) The complete HP 2115A Driver Switch board schematic is given in the HP 2115A Maintenance Manual and the Student Workbook.

(2) Bit 12 is sensed (via pins 14 and 10) if a X Driver Switch; if a Y Driver Switch there is no connection pin 10 - but pin 14 ($\overline{\text{M12}}$) will always be high. In any case, gates MC17, MC67 and MC77 comprise the decoding network for Bit 12, MRT, MWT, MIT and MRTØ (remembering that the core location addressed is determined by all these signals). Transistors Q49-Q52 provide the drivers for the +4. 5V to the packs and +20V for the Drivers. Transistors Q53 and Q54 provide -2V bias (via diodes CT33-CR49) for the Switches.

(3) The Driver/Switch circuits are layed out in two banks. The upper bank is called Bank One and the lower bank is called Bank Two. Each bank consists of eight Driver/Switch circuits. Bank One senses bits 0-2 and 6-8. Bank Two senses bits 3-5 and 9-11. For any given octal address, only one circuit in each bank is enabled. If a driver is enabled, its output is +20V; if a Switch is enabled it provides a ground.

(4) For discussion, assume we are "reading" location Ø527Ø. In this case (for the Y Driver/Switch) the bit coding is $\overline{M12}$, $\overline{M11}$, $\overline{M10}$, $\overline{M9}$, $\overline{M8}$, $\overline{M7}$ and $\overline{M6}$. And since we are "reading", MRTØ will also be true. The $\overline{M12}$ signal being true (remembering $\overline{M12}$ at pin 14 is always true for the Y Driver/Switch) and MRTØ true (which is always up for reading) MC67 is made (pins 9-10), MC67 (pin 8) goes low and MC77 (pin 3) goes high. Thus, pin 5 on MC76-MC126 goes true. Also, with bits M11, $\overline{M10}$, and M9 true - pins 1, 2 and 4 are also true on MC106. This gate will enable Driver Q30 and provide +20V to pin 22 as the C5 signal to core. Also, with bits $\overline{M8}$, M7 and $\overline{M6}$ true, pins 9, 10, 12 and 13 on MC36 will be true. This gate will enable Switch Q3Q35 and provide a ground to pin 5 as the CC2 signal. Thus, the Y octal address 52 has been completely decoded. Both core locations Ø52 and 152 in Y are addressed by Y.

(5) The X octal address decoding is similar to the Y address decoding except that bit 12 is also sensed to select the upper or lower core location. In our example, the lower core at Ø527Ø is to be read. Bit $\overline{12}$ is therefore true at pin 14 on the X Driver/Switch board. Again, as in the Y example, gates MC67 (pins 9 and 10) and MC17 (pins 2 and 3) will be made. Gates MC77 (pins 1 and 2) and MC77 (pins 9 and 10) will then provide true signals to pins 5 on MC76-MC126 and 9 on MC16-MC66. With bits M3, M4 and M5 true, pins 1, 2 and 4 on MC126 will be true enabling Driver Q32 which provides the +20V as the C7 signal (pin 24). Now with bits $\overline{M2}$, $\overline{M1}$ and $\overline{MØ}$ true, pins 10, 12 and 13 on MC16 are also true. Gate MC16 will enable

the Switch Q1Q33 and provide a ground at pin 1 as the CCØ signal. Thus, X octal address 7Ø has been decoded. The entire address Ø527Ø has enabled lines YCC2 and YC5, and XCCØ and XC7. This is exactly the correct combination to select octal core location Ø527Ø.

4. HP 2116B Driver Switch (Refer to Logic Diagram)

a. Purpose

(1) The Driver Switch boards in the HP 2116B serve the same purpose as those boards in the HP 2115A. The only difference in the HP 2116B is the board circuit configuration as shown on the schematic.

(2) The primary difference in the HP 2116B is that the machine can be extended to a 32K core. The machine therefore has an MMD board to facilitate addressing core that exceeds 8K. This, of course, requires additional Driver/Switch boards as well. Also, the Driver/Switch boards are arranged in banks of Drivers and banks of Switches rather than combining Drivers and Switches as in the HP 2115A.

b. Logic

(1) Again we assume we are addressing core location Ø527Ø. With bit $\overline{M12}$ true, the MMD board provides a true input (XØ) at pin 14 (in the case of X). The signals to pins 14 and 10 from the MMD board can be listed as follows:

Module Address	Pin 14	Pin 10
Ø and 1	YØ1 or XØ	MMD GND or X1
2 and 3	Y2/3 or X2	MMD GND or X3

(2) Using the above listed signals, we will proceed to decode address Ø527Ø, first in Y then in X.

(a) Pin 14 is always true on the Y Driver Switch. Since we are reading, MRT is also true. These true inputs enable MC17 (pins 2 and 3) and MC67 (pins 9 and 10). The outputs at MC77 (pins 3) and MC77 (pin 8) are therefore true. MC77 (pin 3) will enable Driver Q57 (with bits M11, $\overline{M10}$ and M9 true) via MC106 pins 9, 10, 12 and 13. Driver Q57 will provide +20V to pin 22 as the C5 signal. Similarly, gate MC77 (pin 8) will enable MC36 (pins 9, 10, 12 and 13) with bits $\overline{M8}$, M7 and $\overline{M6}$ true. Switch Q14Q15 will then provide a ground at pin 5 as the CC2 signal. Thus, YCC2 and YC5 have been selected for Y octal address 52.

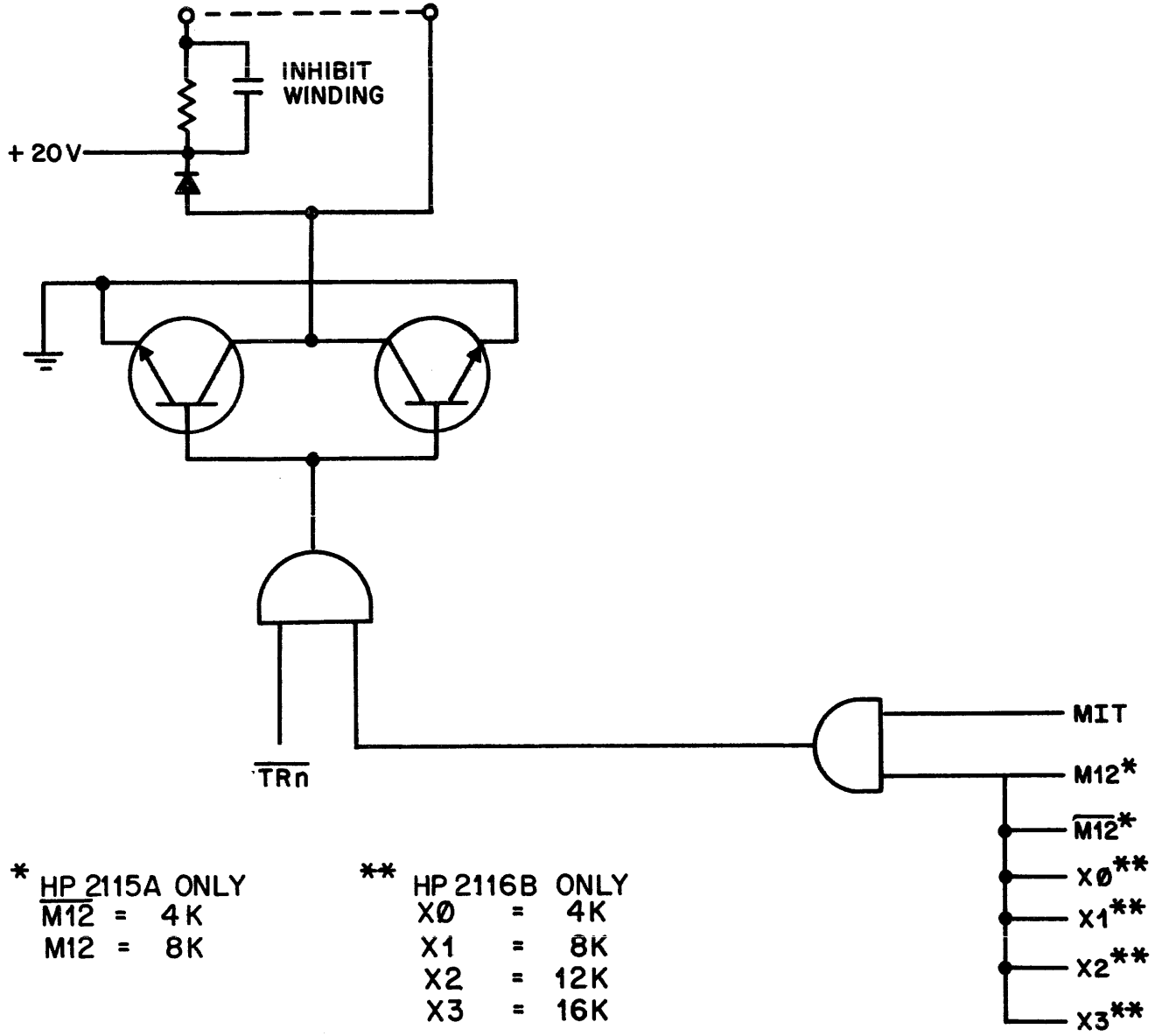
(b) For the X Driver/Switch board (with address Ø527Ø), a true XØ signal from the MMD board will enable MC77 (pin 8) as before. With bits M3, M4 and M5 true, gate MC126 (pins 9, 10, 12 and 13) is made. Gate MC126 then enables Driver Q63 which provides +20V at pin 24 as the C7 signal. Similarly, with bits $\overline{M2}$, $\overline{M1}$ and $\overline{MØ}$ true, gate MC16 (pins 9, 10, 12 and 13) is made. Gate MC16 then enables Switch Q4Q5 which provides a ground at pin 1 as the CCØ signal. Thus, XCCØ and XC7 have been enabled for X address 7Ø.

(c) The complete address decoding for Ø527Ø was accomplished by enabling lines YCC2, YC5, XCCØ and XC7. This conforms to our previous examples.

5. HP 2116B and HP 2115A Inhibit Drivers (Figure 4-18)

a. Purpose

(1) The purpose of the Inhibit Drivers is to gate memory inhibit timing (MIT) with the TR outputs and supply an inhibit current (-I/2) when writing zeros.



* HP 2115A ONLY
$\overline{M12}$ = 4K
M12 = 8K

** HP 2116B ONLY
X0 = 4K
X1 = 8K
X2 = 12K
X3 = 16K

SIMPLIFIED HP 2115A/HP 2116B INHIBIT DRIVER

FIG. 4 – 18

(2) The HP 2116B Inhibit Drivers are similar to the HP 2115A Inhibit Drivers except for the gating circuit configurations. Also, since theHP 2116B may be expanded to 32K, MIT is gated with the signals XØ, X1, X2 or X3 (provided by the MMD board) rather than with bit M12 or $\overline{M12}$.

b. Logic

(1) The Inhibit Driver schematic is shown in the Logic Diagrams. A simplified circuit is shown in Figure 4-18.

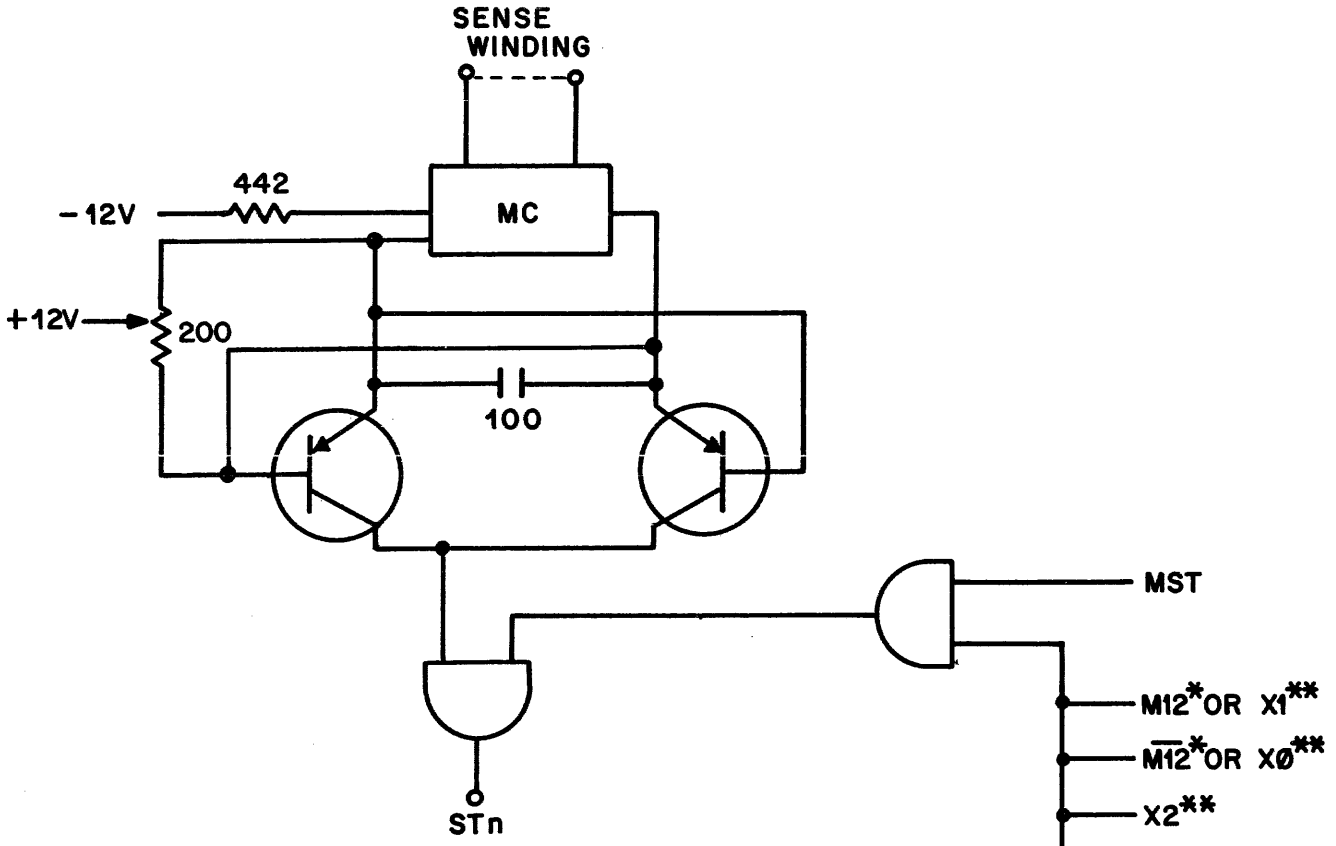
(2) The MIT signal is gated with M12 (A4) or $\overline{M12}$ (A3) depending on upper or lower core addressing respectively. Gate MC76 then provides one enabling input to each of 16 Drivers (MC16-MC106). The other inputs to these Drivers are the reset outputs from the T-Register ($\overline{TR}$*); when writing a "0", the respective $\overline{TR}$* signal is true. The enabling gate then triggers a dual parallel transistor circuit which provides a ground for the inhibit winding in core. The other side of this winding is connected to +20V so that an inhibit current is present. At the expiration of MIT, the parallel transistors are turned off, the field around the inhibit winding collapses forward biasing CR9 and the inhibit winding is shorted to prevent switching the core again.

(3) The HP 2116B Inhibit Driver is shown in the Logic Diagrams. Circuit logic is the same as the HP 2115A except for the exceptions listed above. Also, the MPTØ signal is used to generate the MPT1 signal used on the MMD board. For 16K machines, this MPT1 signal is also routed to ID2 which generates the MPT2 signal.

6. HP 2115A and HP 2116B Sense Amplifiers (Figure 4-19)

a. Purpose

(1) The HP 2115A and HP 2116B Sense Amplifiers are identical. The circuit schematic is shown in either Logic Diagrams. A simplified Sense Amplifier is shown in Figure 4-19.



* HP 2115A ONLY
$\overline{M12}$ = 4K
M12 = 8K

** HP2116B ONLY
X0 = 4K
X1 = 8K
X2 = 12K
X3 = 16K

SIMPLIFIED HP2115A/HP2116B SENSE AMPLIFIER

FIG. 4 - 19

(2) The purpose of the Sense Amplifier is to read core and strobe the resultant data into the T-Register.

b. Logic

(1) The memory strobe timing pulse MST is gated through MC55 with M12 or M12 (in the HP 2115A) to enable one input to the output gates of the Sense Amplifier. (In the HP 2116B, MST is gated with the XØ, X1, X2 or X3 signals provided on the MMD board). The other enabling inputs to these output gates (MC15-MC105) are the Sense Amplifier outputs.

(2) The Sense Amplifiers consist of a micro-circuit (MC1-MC161) and a transistorized switch (Q91-Q92). The sense pulse is gated through the output gate (MC15-MC105) by MST at T2. In the HP 2116B, when using higher order memory modules (above 16K), MST is delayed (on the Timing Generator board) until the middle of T2 to allow additional time for addressing core.

7. Memory Geography

a. Board Location

(1) All boards are located in the uppermost section of CPU, except the Memory Extender boards. These boards are located in the I/O section (slots 221 and 222).

b. Memory Cards

(1) All top connections go to core. The bottom connections remain within the CPU section.

8. Troubleshooting Procedures

a. Test Procedures

(1) Complete memory test procedures are contained in the Field Test Procedures Manual.

(2) The general approach to troubleshooting is:

(a) Check rear panel MON switch.

(b) Check timing pulses from MMD and STG board.

(c) Check ID and SA boards if problem is characteristic of a bit position.

(d) Check D/S boards and MAD board if problem is characteristic of octal address.

(e) Check RAF board if input to MAD is erroneous.

(f) Check core assembly if output of D/S boards is correct. Use diagnostics to check core.

9. Review

(1) What bit in the M-Register distinguishes an address in the lower 4K memory stack from the upper 4K memory stack?

(2) What number module is addressed when bit 12 is a zero?

(3) What two added components are required to increase memory beyond 16K?

(4) What board(s) in the HP 2116B and HP 2115A make the binary to octal address decoding?

(5) What is the purpose for having two different memory timing signals (MRT and MWT) control the Driver Switches?

(6) What is the specific purpose of the Driver/Switches?

(7) What register controls reading and writing of core?

(8) How does the HP 2115A increase core to 8K without adding additional Driver/Switches?

(9) How many cores on each plane are addressed for any given address?

(10) What memory timing signal enables the Sense Amplifier output?

(11) What signals are required to enable an Inhibit Amplifier?

power supply

A. HP 2116B POWER SUPPLY PHYSICAL DESCRIPTION (1.0 Hours)

1. Fuses (Figure 5-1 and 5-2)
   a. Location
      (1) All 14 fuses are accessible from front of power pack.
   b. Ratings
      (1) The fuse ratings are:

F1	(Main Power Fuse)	- 15A (SB)
F2	(-9V Supply)	- 6.25A (SB)
F3	(-82V Supply)	- 0.3A
F4	(+22V Supply)	- 6.25A (SB)
F5	(+12V Supply)	- 6.25A (SB)
F6	(-12V Supply)	- 6.25A (SB)
F7	(-22V Supply)	- 6.25A (SB)
F8	(+95V Supply)	- 0.3A
F9	(+32V Supply)	- 6.25A (SB)
F10	(+7V Supply)	- 4.0A (SB)
F11 -F14	(+4.5V and -2V)	- 30A

2. Printed Circuit Boards
   a. Location
      (1) A301, A302 and A303 are on top section of power pack.
      (2) A304 and A305 are heat sinks located on bottom of power pack.
      (3) A121 and A1 are located in CPU.
   b. Purpose
      (1) Logic Supply Regulator (A301)
         (a) This board contains the Voltage Regulators for +4.5V, +12V and -2V supplies.
         (b) The power turn-off circuit is also located on A301.

(2) Memory Supply Regulator (A302)

(a) This board contains the Voltage Regulators for the -12V, +22V, -22V and +32V supplies.

(3) Capacitor Board Assembly (A303)

(a) This board contains all the rectifiers and filters for the secondary transformer (T1).

(4) Large Heat Sink Assembly (A304)

(a) This board contains the Series Regulators for the +4.5V, +12V, and -2V regulated supplies.

(5) Small Heat Sink Assembly (A305)

(a) This board contains the Series Regulators for the -12V, +22V and -22V, and the +32V regulated supplies.

(6) Power Fail Interrupt Board (A1)

(a) This board senses the +4.5V, +12V, -12V and -2V regulated supplies and provides the power-on/off-pulse (POFP) to the STG board if any supply fails. It also enables the interrupt system if a power failure occurs.

(7) Overvoltage Protection Assembly (A121)

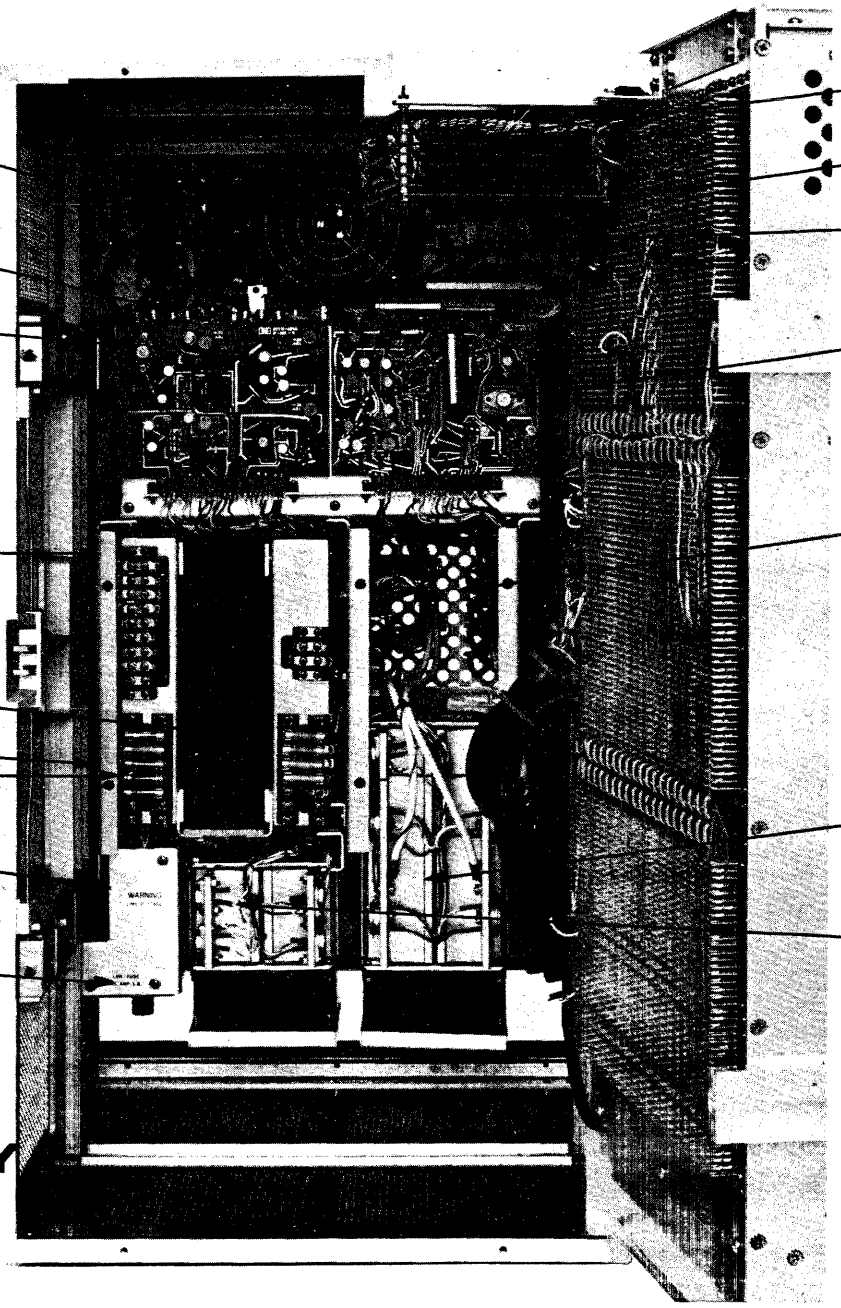
(a) This circuit senses all regulated supplies and provides over-voltage protection.

(b) This board also contains the test points for all regulated supplies.

3. Blowers

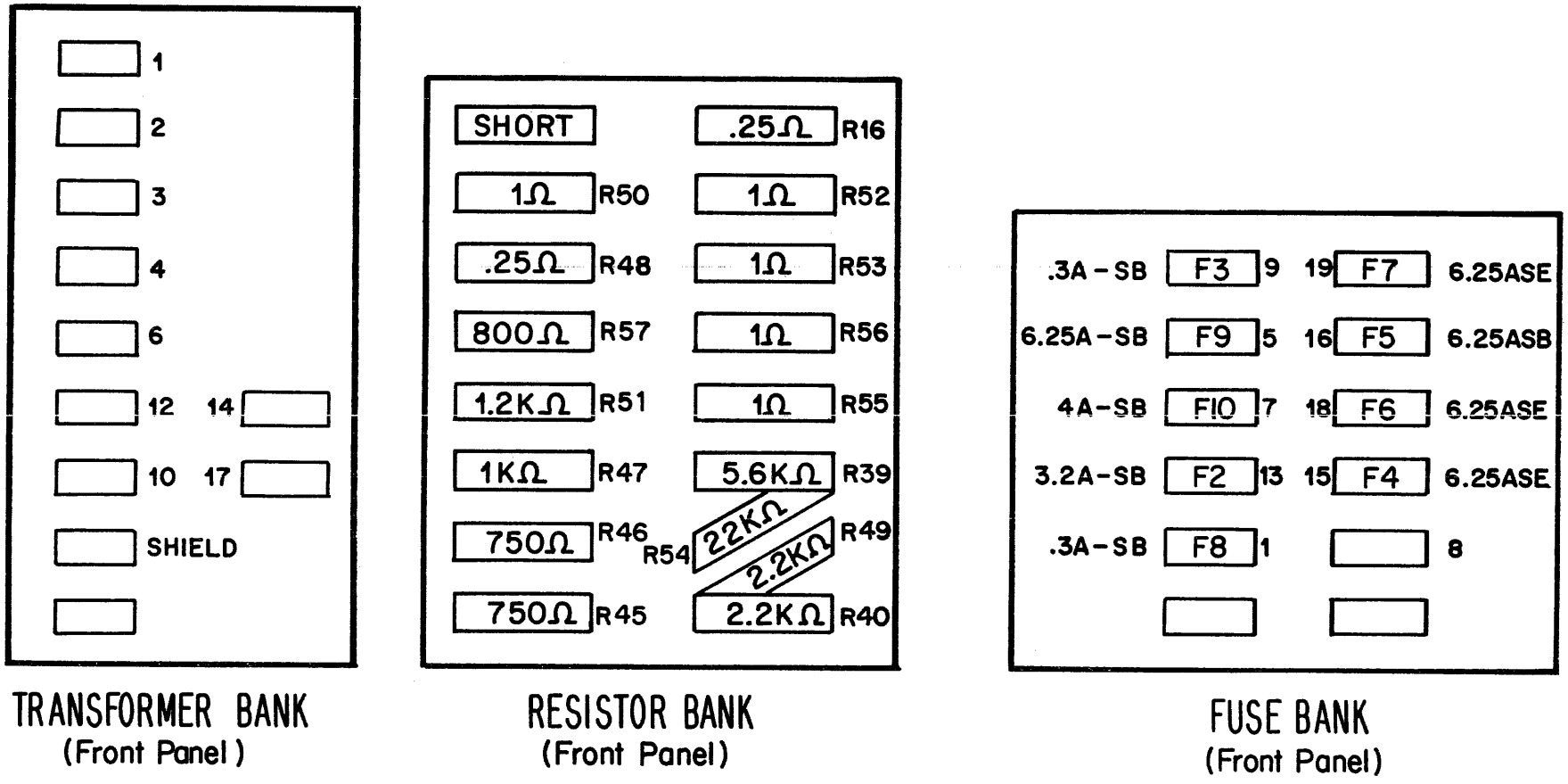
a. Location

(1) The six blowers are located as follows:



2116B POWER SUPPLY

FIG. 5-1



TRANSFORMER BANK
(Front Panel)

RESISTOR BANK
(Front Panel)

FUSE BANK
(Front Panel)

HP POWER SUPPLY COMPONENT LOCATION

FIG. 5-2

M1	- Top front of power pack
M2, M3	- Heat sink
M4, M5, M6	- Under Heat Sink Assemblies

b. Purpose

(1) All blowers are interchangeable.

4. Limiting Resistors

a. Location

(1) These resistors are negative coefficient resistors located on the upper right side of power pack.

b. Purpose

(1) The purpose of these resistors is to provide temperature compensation for the +4.5V and -2.0V regulated supplies and to limit current drain.

5. Power Relay and Line Filter

a. Location

(1) The Power Relay (K1) and line filter (FL1) are located on the lower left of power pack.

b. Purpose

(1) The purpose of the power relay is to transfer line power to the power transformer and to provide the +4.5V turn-on pulse to the Power Fail Board (A1).

(2) The purpose of the line filter is to filter line ripple.

B. HP 2116B POWER SUPPLY OPERATIONAL BLOCK DIAGRAM (1.0 Hour)

1. Primary Power (Schematic)

a. Power Relay (K1)

(1) The power relay is energized when the POWER pushbutton is depressed and the unregulated +4.5V bus comes up. The unregulated +4.5V bus is enabled via R1 and T1. When the +4.5V is enabled, K1 is energized and the line voltage is applied through the 7-10 contacts. Simultaneously, +4.5V is applied through thermal switches S301 and S302 to the Power Fail Interrupt Board (A1).

(2) Resistor R1 is a limiting resistor used to prevent surge.

(3) Power Relay K1 is latched through its own contacts.

b. Blowers

(1) Power to the blowers is taken off the transformer primary.

c. Thermal Interlocks

(1) The thermal interlocks S301 and S302 are located on A305 and A304 respectively. They open at approximately 65°C and remove the +4.5V from the Power Fail Interrupt board (A1).

2. Secondary Power (Schematic)

a. Fuses and Rectifiers

(1) The entire secondary is fused. All 6.25A fuses are slow-blo.

(2) The upper secondary rectifier is a half-full-wave combination used to develop the unregulated +4.5V and -5V to energize K1. A full-wave rectifier is used to develop -12V for the Series Regulators on A304.

(3) The middle secondary uses a voltage doubler to develop +35V, +23V, -22V and -36V for the Series Regulators on A305, and the voltage regulators on A301 and A302.

(4) The lower secondary uses four full-wave rectifiers. The uppermost three rectifiers develop -84V, +105V and +56V for the regulators on A301 and A302. The last rectifier provides +7V for the front panel lamps.

3. Memory Supply Regulator (A302)

   a. -12V Supply

      (1) The -12V regulated supply is developed from the -22V supply, the Series Regulator on A305, and the -12V Voltage Regulator on A302.

      (2) This supply controls the turn-off of all other supplies when any one regulated supply fails. This turn-off circuit is located on A301.

   b. +32V Supply

      (1) The +32V supply is developed from the +56 line, the Series Regulators on A305 and the Voltage Regulator on A302.

   c. +22V Supply

      (1) The +22V regulated supply is developed from the +35V line, the Series Regulator on A305 and the Voltage Regulator on A302.

4. Logic Supply Regulator (A301)

   a. +4.5V Supply

      (1) The +4.5V supply is developed from the unregulated +4.5V bus, the Series Regulators on A304, and the Voltage Regulator on A301.

      (2) This supply and the -2V supply are mutually dependent. That is, the maximum allowable current drain from the +4.5V supply is dependent upon the current drain on the -2V supply. The +4.5V supply may draw up to 22.5A plus the current drawn by the -2V supply.

      (3) This +4.5V supply and the -2V supply determine the state of the Power Fail Interrupt circuit (A1). If +4.5V fails, a power-on/off-pulse (POFP) is generated and the logic supply is turned off.

b. -2V supply

(1) The -2V supply is developed from the -5V unregulated supply, the Series Regulator on A304 and the Voltage Regulator on A301.

(2) This supply determines the maximum allowable current that can be drawn from the +4.5V supply. This -2V supply is capable of supplying 22.5A. If the -2V supply drain is 22.5A, then the +4.5V supply may draw 45A.

(3) This -2V supply may also generate a power off pulse (POFP) on the Power Fail Interrupt (A1) if it fails.

c. +12V Supply

(1) The +12V supply is developed from the +23V bus, the Series Regulator on A304 and the Voltage Regulator on A301.

(2) This +12V supply is also used to light the POWER lamp on the front panel and gives an indication of the state of the -12V supply. If the -12V supply is down, the +12V supply is turned off and the POWER lamp is not on.

d. Turn-Off Circuit (A301)

(1) The power turn-off circuit is located on A301. If any regulated supply fails, the -12V supply will be interrupted. This -12V supply being interrupted causes all other supplies to go down. When the +12V supply goes down, the POWER lamp goes out.

5. Overvoltage Protection Assembly (A121)

a. Over-voltage Protection

(1) The Overvoltage Protect Assembly provides protection against high over-voltage conditions. The over-voltage is shorted to ground until the overload is removed.

b. SCR Control

(1) An SCR is used in each circuit to short the overloaded bus to ground.

c. Test Points

(1) All regulated voltages are brought out to the front on the Over-Voltage Protection Assembly (A121). These test points are accessible in the CPU.

6. Power Fail Interrupt Board (A1)

a. This board provides the following signals:

(1) PSO - This signal is applied to the turn-on circuit on the logic supply regulator board if all thermal switches are closed.

(2) PON - This level enables the MEMORY ON/OFF Sw and collector voltage for the memory driver/switch cards if the +4.5V and -2V supplies are up.

(3) POFP - This signal performs the same function as PRESET when power is initially applied to or removed from the computer.

b. When a power failure occurs, this board generates an interrupt request to the I/O Control board. This power fail interrupt circuit has a priority code of Ø4.

7. Front Panel Coupler (A101)

a. 115V AC Switched

(1) 115V AC is applied to the front panel POWER switch and returned to R1.

b. +7V Lamp Supply

(1) The +7V supply is applied to all lamps on the front panel except the POWER lamp. This lamp is enabled by the +12V supply.

c. +12V Power Lamp Supply

(1) The +12V power lamp supply is routed through the Power Fail Interrupt Board (A1) to the front panel POWER lamp.

d. +4.5V and -5.0V Relay Supply

(1) These supplies are routed through the front panel POWER switch to K1. When the switch is turned off, -5V is routed to K1 and it cannot be energized. When the switch is on, +4.5V is routed through the switch to K1.

C. HP 2116B POWER SUPPLY DETAILED CIRCUIT THEORY

1. Logic Diagram (Figure 5-3)

a. Turn-On (A1)

(1) When power is applied initially, the +4.5V and -2V regulated supplies are low. The POFP pulse is therefore true.

(2) When these supplies come up, the POFP signal goes false.

(3) The turn-off circuit is temporarily disabled by the +4.5V supply until the remaining supplies come up.

b. I/O Logic Supplies

(1) The I/O and Logic Supplies are the +4.5V, -2V and +12V.

(2) The +12V supply is controlled by the -12V turn-off supply. Thus, if it or any of the memory supplies fail, the POWER lamp on the front panel will go out. This is an indication that we have a power failure.

(3) Notice that the +4.5V and -2V supplies are not affected by the turn-off circuit, but must be on to enable the turn-off circuit; and hence, the remaining supplies.

c. Memory Supplies

HP 2116B POWER SUPPLY BLOCK LOGIC

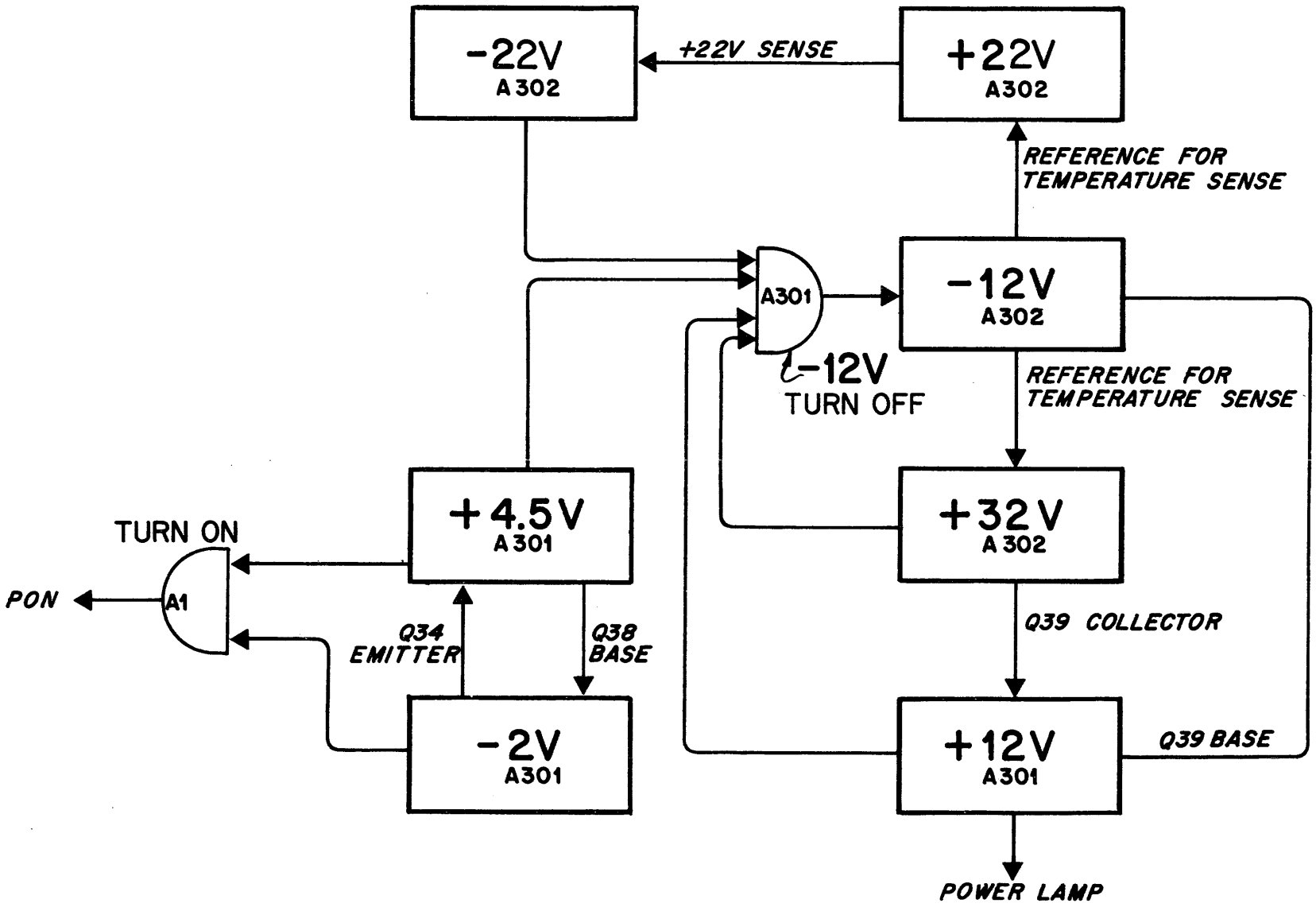
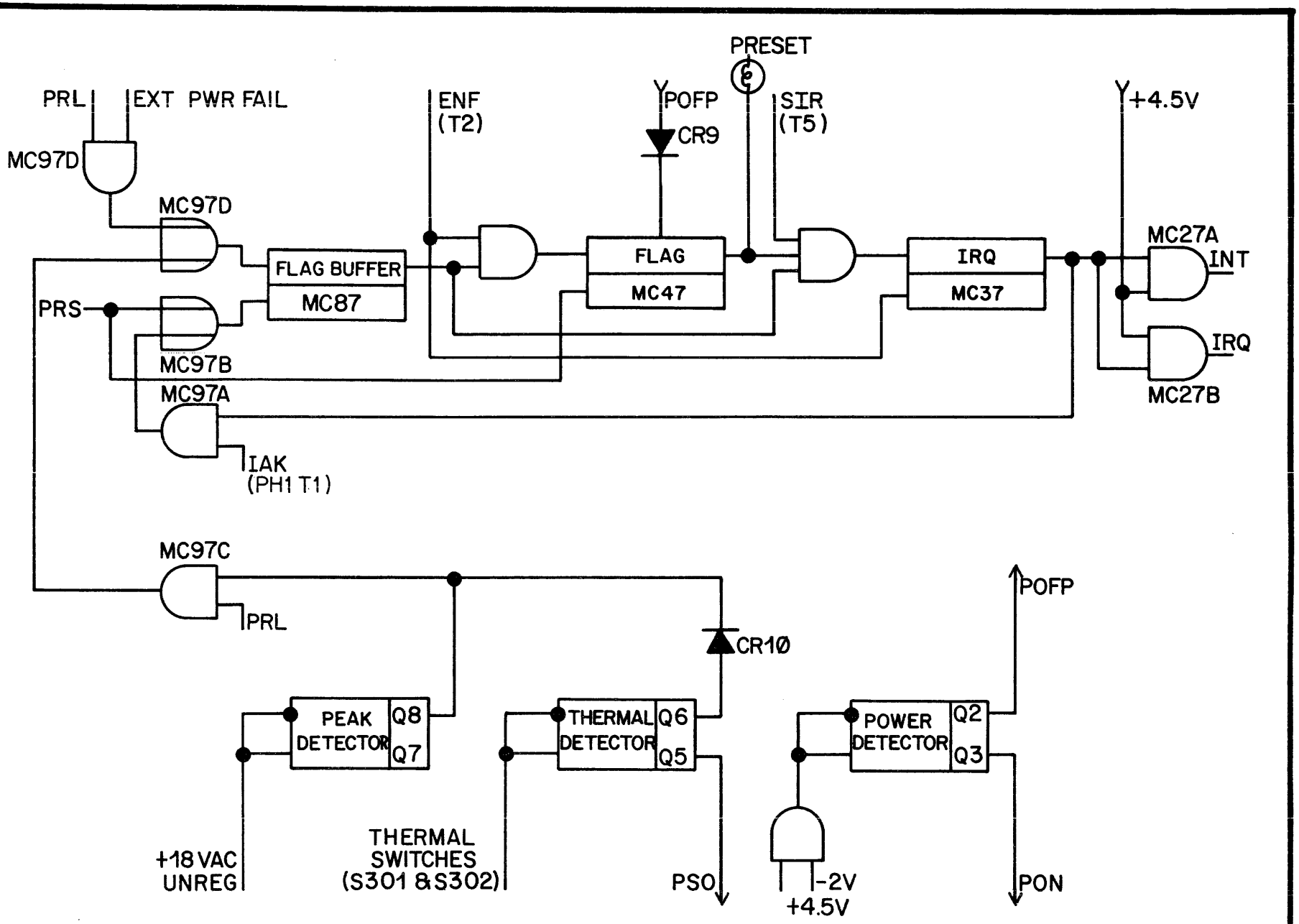


FIG. 5-3



SIMPLIFIED POWER FAIL INTERRUPT CIRCUIT

FIG.5-4

(1) The Memory Supplies are the -12V, +32V, +22V and -22V.

(2) The -12V supply provides the temperature sense reference for the +22V and +32V supplies. If the -12V fails, this reference is down and the turn-off circuit is enabled. The +22V supply then turns off the -22 supply. The +32V supply turns off the +12V supply.

d. Turn-Off Circuit

(1) The -12V turn-off circuit is located on A301. When this circuit is turned on, the -12V goes down. When the -12V goes down, the reference for the +32V and +22V supplies go down and these supplies are turned off.

(2) When the +32V shuts off, the reference for the +12V is down and the +12V supply goes down.

(3) When the +22V shuts off, the reference for the -22V goes down and the -21V supply is turned off.

2. Power Fail Interrupt (Figure 5-4)

a. Logic Control

(1) The interrupt logic is shown at the top of this board in the logic diagram. MC87 is the Flag Buffer FF, MC47 is the Flag FF, and MC37 is the IRQ FF. The Flag Buffer FF may be set by any of three signals: The EXT PWR FAIL signal from the HP 2160 Power Supply Extender, the unregulated +18V AC detector (Q8) signal, or the thermal switch detector (Q6) signal. The Flag Buffer FF is reset by one of two signals: The PRS (Preset) signal or the IAK (Interrupt Acknowledged) signal.

(2) With the Flag Buffer FF set, ENF is gated on at T2 to set the Flag FF (via MC47). This turns on the PRESET lamp (Q1). The output of the Flag Buffer FF is also gated with

SIR (Service Interrupt Request) at T5 and the set output of the Flag FF to set the IRQ FF. The IRQ FF then gates the INT and IRQ signals to the I/O Address Card and enables Phase 4.

(3) The Flag FF (when set) also provides a low PRL signal to the next lowest priority device.

(4) At T1 of the next machine phase, IAK resets the Flag Buffer FF ending the interrupt sequence.

(5) This board also supplies the PSO (Power Supply On). PON (Power On Normal) and POFP (Power On-Off Pulse) signals. The PSO and PON signals are normally true whereas the POFP signal becomes true only at initial turn-on time, or in the special case of a power failure.

b. Power Fail Interrupt Circuit (A1)

(1) Under normal operating conditions, the Flag Buffer, Flag and IRQ Flip-Flops are reset. Diodes CR1 and CR2 with their associated RC circuitry form a peak detector monitoring the unregulated +18V AC bus. Transistor Q7 is normally conducting and Q8 is held off. The collector supply for Q8 is taken through MC97 (pin 3) which is normally at a level just below ground. If the +18V AC unregulated bus begins to drop, Q7 is turned off and Q8 is turned on pulling pin 3 of MC97 true. With the PRL signal true also, the Flag Buffer FF is set and the machine will enter the Interrupt Phase.

(2) The +4.5V unregulated supply routed through the three thermal switches (S301, S302 and S1) normally holds Q6 off and Q5 on. If a thermal switch opens, Q6 turns on and Q5 is turned off pulling the PSO signal low. At the same time, CR10 is forward biased pulling MC97 (pin 3) high enabling the Interrupt circuit.

(3) Under normal operating conditions, Q3 is turned on by the +4.5V

and -2V buses (via Zener CR8). This action normally holds Q4 and Q2 off. The collector supply for Q2 is taken through MC57 (pin 6). A true PON signal is then taken off the collector of Q3 and through MC17. A false POFP signal is taken off MC57 (pin 13). If either the -2V or +4.5V supply begins to go low, Q3 is turned off and Q4 and Q2 are turned on. Under these conditions, the PON signal goes false and the POFP signal goes true forcing the machine to the HALT mode. At the same time, CR9 is forward biased and the Flag FF is set immediately. This lights the PRESET lamp but does not cause an Interrupt since the Flag Buffer FF does not get set.

(4) An EXT PWR FAIL signal from the HP 2160 will also cause an Interrupt. This signal goes true and sets the Flag Buffer FF via MC97.

3. -12V Turn-Off Circuit (Figure 5-5)

a. Logic Control

(1) The PSO signal generated on the Power Fail Interrupt Board (A1) is high if the thermal switches are closed and the +4.5V is up. This signal, the +4.5V, +12V, -22V and +32V, is applied to MC1A. The true output from MC1A then holds Q43 off and the -12V supply cannot be turned off.

(2) MC1B serves to hold off Q43 until the other supplies come up.

b. -12V Disable

(1) If any supply except -12V goes down, MC1A output goes false and Q43 conducts. When Q43 conducts, the collector goes toward ground and turns off Q52 in the -12V supply.

(2) When -12V goes down, the bias on Q39 in the +12V Regulator is decreased. This transistor conducts more essentially grounding the base on Q40. This causes Q41 to cut off and the +12V supply goes down.

HP2116B -12V TURN OFF CIRCUIT

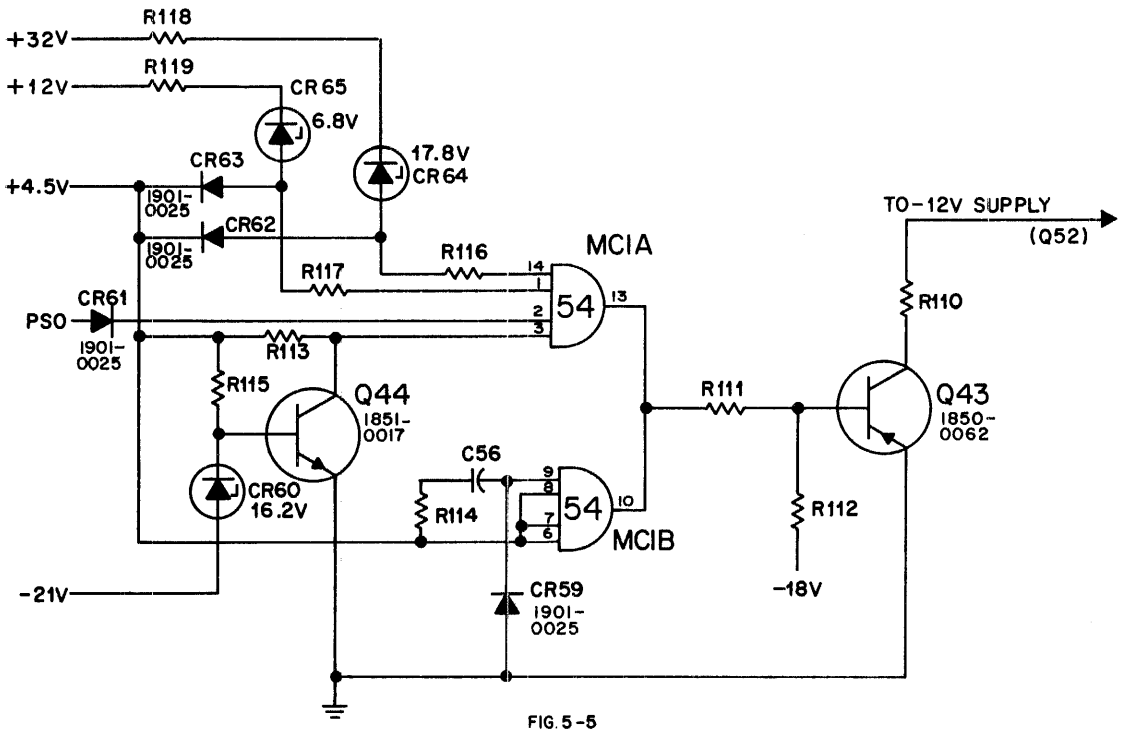


FIG. 5-5

HP2116B -12V REGULATOR

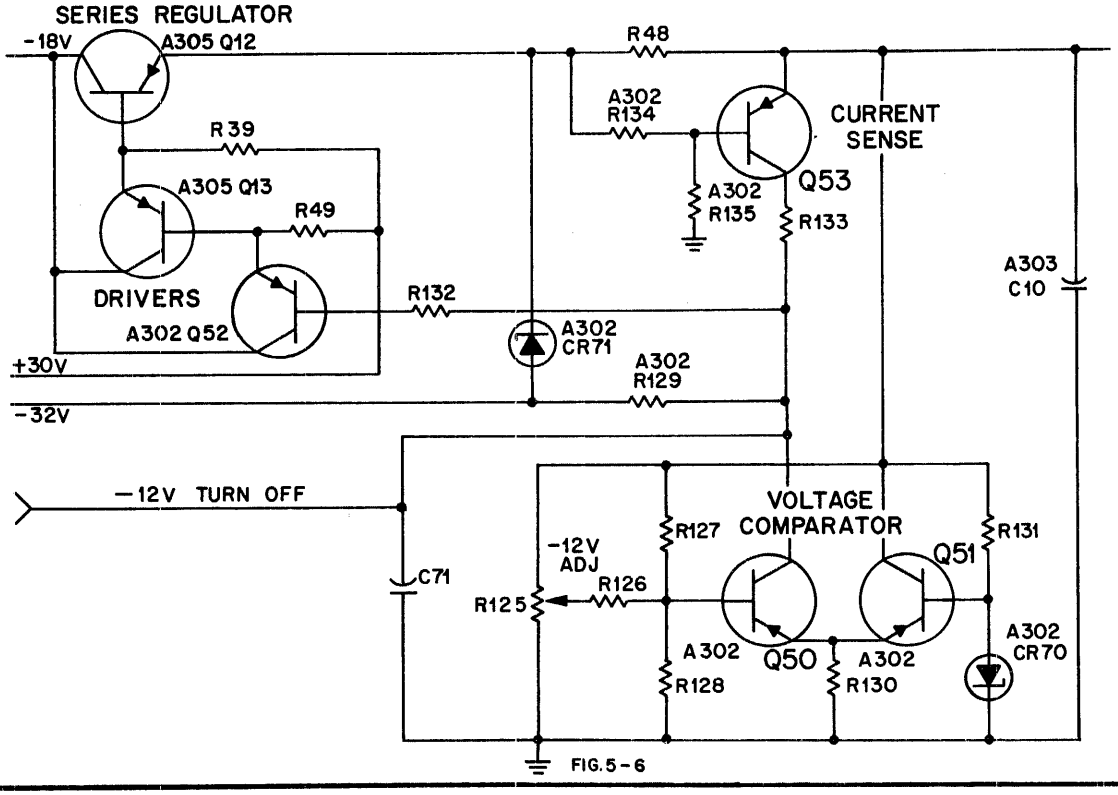


FIG. 5-6

(3) When +12V goes down, the Differential Amplifiers (Q54 and Q61) in the +22V and +32V Regulators, respectively, decrease in condition. This causes the drivers and emitter followers to increase in conduction which increases the conduction of the respective Series Regulators. This then saturates the Differential Amplifiers which turn off the respective drivers and emitter followers. Thus, we force ourselves into a current limiting condition which then shuts down the supplies.

(4) When the +22V goes down, Q57 in the -22V supply increases in conduction. This causes the same current limiting condition that we had for the +22V and +32V supplies.

(5) If a supply goes down other than the +4.5V, we may jumper C56 in the -12V turn-off circuit to bring up the supplies for troubleshooting.

c. Interlock Circuit

(1) The +4.5V and -2V interlock circuit is located on the Logic Supply Regulator (A301). A -9V bias voltage is applied through R88, CR56 and a voltage divider to +4.5V for bias on Q38 and Q33. If +4.5V goes down, a full -9V forward bias is applied and both the +4.5V and -2V supplies go into current limiting.

(2) The -2V supply may be brought up for troubleshooting by jumpering C54 to ground. This removes the -9V forward bias and allows the -2V supply to operate normally.

4. -12V supply (Figure 5-6)

a. Logic Diagram

(1) All regulated memory supplies (A302) work essentially the same. They have a rectifier and filter, a voltage regulator and current limiter, and a crowbar over-voltage protection circuit.

(2) The current limiter always takes control from the voltage regulator.

b. Rectifier and Filter

(1) The rectifier CR7, CR8 rectifies 18.3V AC. This is filtered across C22 and R32, then applied to Series Regulator Q12.

c. Regulator and Limiter

(1) The regulated -12V is taken from the emitter of Q12. Transistors A305Q13 and A302Q52 provide drive for the series regulator (current gain). Zener A302CR71 maintains a 20V drop between -32V and -12V.

(2) The Differential Amplifier (A302Q50 and A302Q51 with Zener A302CR70 senses any voltage change in the -12 line. This change is amplified in the amplifier and applied to the base of driver A302Q52 which controls the conduction of series regulator A305Q12.

(3) The current limiter (A30Q53) senses the voltage drop across R48. Under extreme loads, this drop will increase sufficiently to turn Q53 on. When Q53 turns on, the -22V line drops (goes positive) and turns Q52, Q13 and Q12 off. Thus, once in a current limiting condition - the voltage regulator loses all control and all supplies are shut down via the Turn-off Circuit on A301.

5. Overvoltage Protection Circuit (Crowbar) (Figure 5-7)

a. Over-Voltage Protection

(1) The Overvoltage Protection Board (A1) provides protection for over-voltage when loads are removed. The test points for all regulated voltages are also on this board.

(2) All crowbar circuits operate similarly, so the -12V crowbar will be described.

b. Circuit

(1) CR10 is a 12.7V Zener. When the Zener breaks down, the gate on SCR Q7 goes positive about 1V and Q7 is turned on. This action shorts the -12V supply to ground and current limiting is enabled. The supply remains in current limiting until the computer is turned off.

HP-2116B OVERVOLTAGE PROTECT (A121)

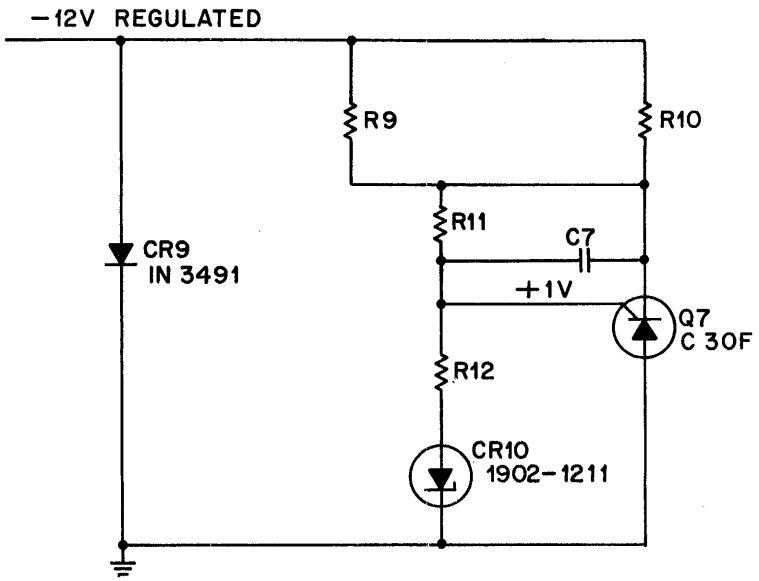


FIG. 5-7

LOGIC RECTIFIERS, FILTERS AND SERIES REGULATORS

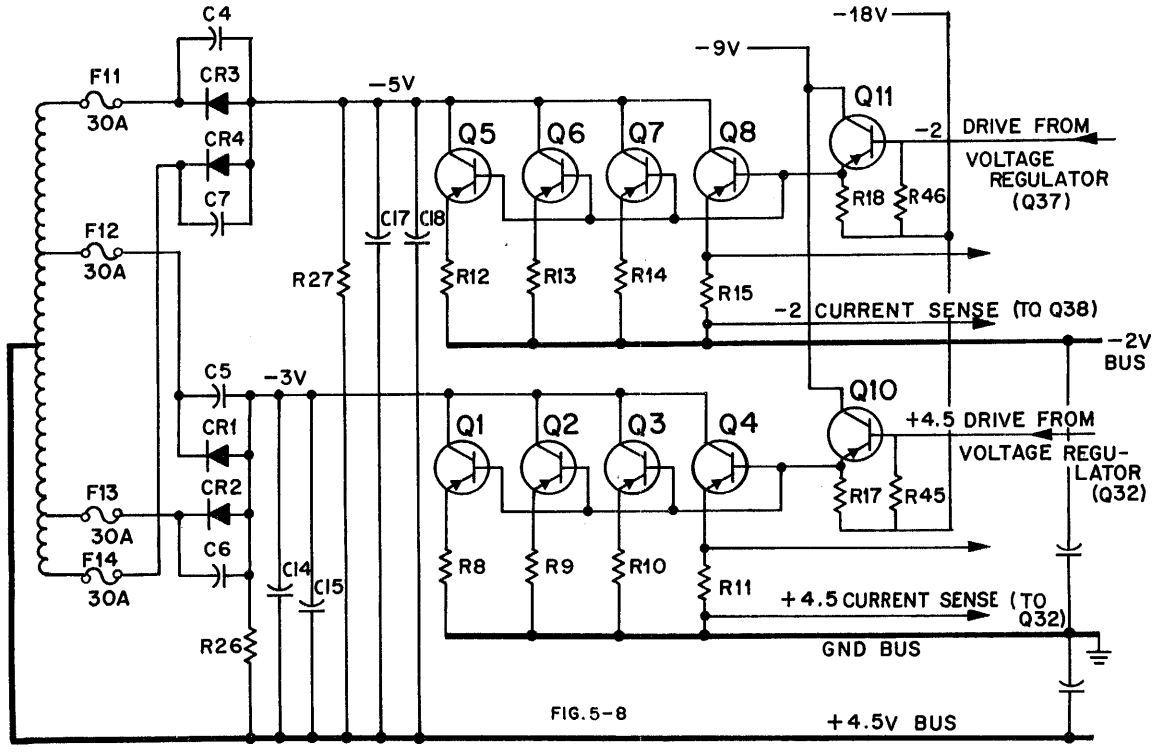


FIG. 5-8

(2) If the -12V supply tends to go positive, CR9 will be forward biased and current limiting will again result.

6. Logic Supply (Figure 5-8)

a. Logic Diagram

(1) The +4.5V and -2V buses are mutually dependent through a ground bus. This allows the +4.5V bus to draw additional current through the -2V bus. That is, the +4.5V bus may draw its current load plus an additional load equal to that drawn by the -2V bus. As an example:

Max I for -2V = 22.5A

Max I for +4.5V = I_L + 22.5A

Where I_L = load on -2V

b. Rectifiers and Regulators

(1) The +4.5V and -2V supplies use a stack of series regulators because of the heavy current requirements.

(2) Emitter followers Q10 and Q11 control the series regulators. These emitter followers are driven from the Voltage Regulators on A301.

(3) The emitters of Q8 and Q4 provide the current sense to the current limiters on A301.

c. +4.5V Regulator and Current Limiter (Figure 5-9)

(1) The +4.5V bus is applied to the base of Differential Amplifier Q30. This voltage comparator controls the +4.5V drive to the series regulators through Q32. Any change in the 4.5V bus changes the conduction of Q30 and Q31 which control Q32. If the bus tends to rise, Q30 conducts less and Q31 conducts more. This makes the base of Q32 go more positive and thus the emitter more positive. The base of Q10 is then driven more positive increasing the resistance of the series element and lowering the +4.5V bus.

HP2116B +4.5V REGULATOR

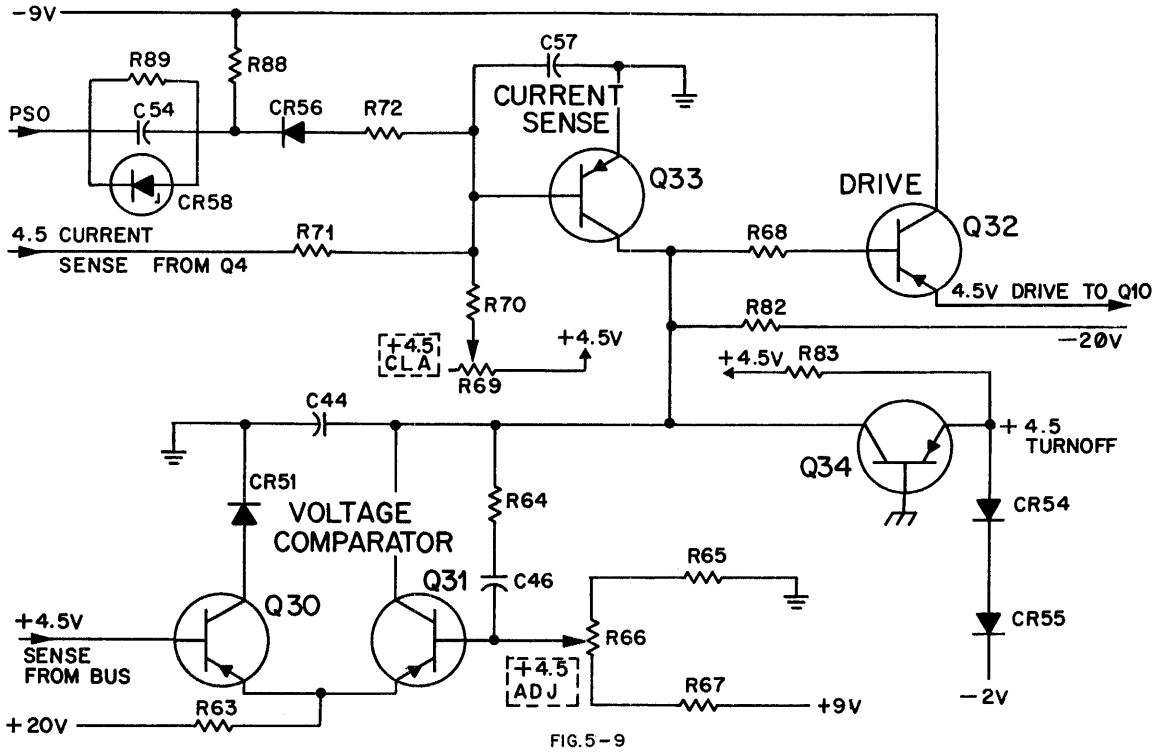


FIG.5-9

HP2116B -2V REGULATOR

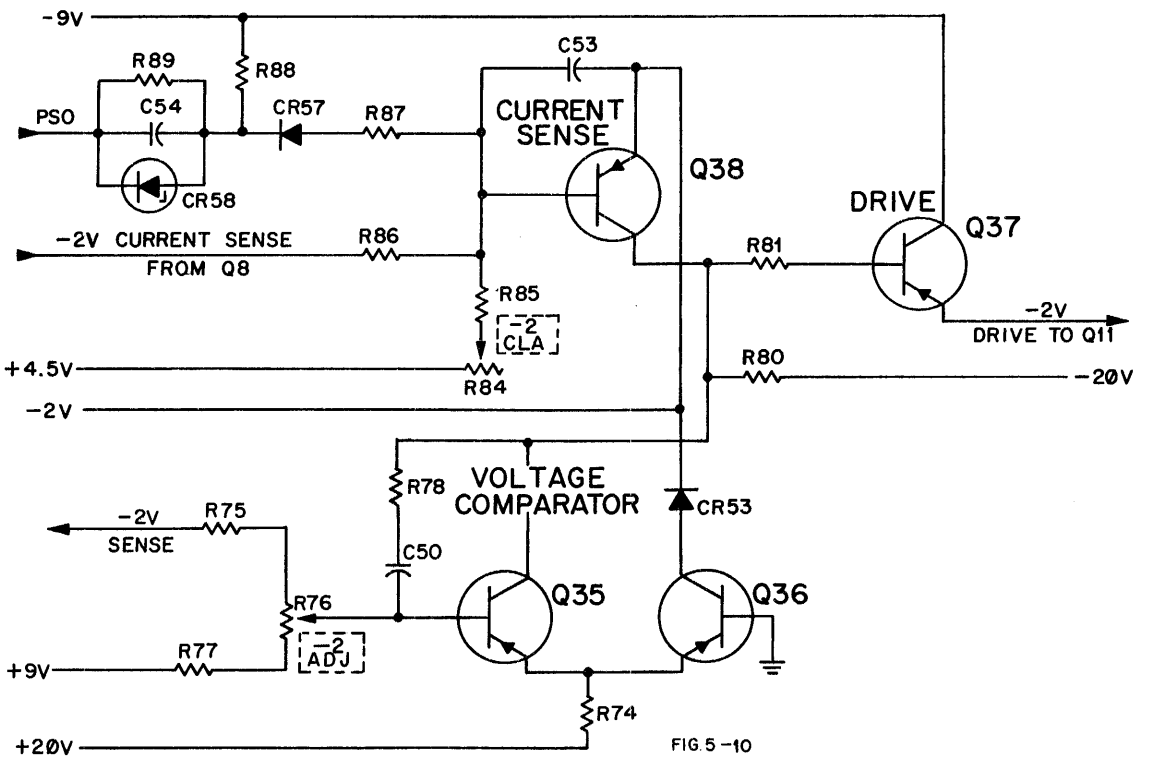


FIG.5-10

(2) Q34 is the +4.5V turn-off circuit. With -2V on the emitter Q34 is cut off. If the -2V does not come up, Q34 turns on. This makes the base of Q32 highly positive and the drive to Q10 is removed shutting down the +4.5V supply.

(3) If the current drawn through Q4 on the heat sink is excessive, the drop across R71 increases and Q33 goes into heavy conduction. This effectively grounds the base of Q32 and provides a positive voltage to the base of Q10 which shuts down the +4.5V bus.

(4) The +4.5V current limiting adjustment (R69) is factory set and should not be adjusted in the field. The +4.5V bus may be adjusted by the +4.5V ADJ (R66) on A301.

d. -2V Regulator and Current Limiter (Figure 5-10)

(1) The -2V Regulator works essentially the same as the +4.5V regulator. The major difference is the -2V turn-off circuit. The current sense transistor (Q38) receives its bias from the 4.5V bus. Thus, if +4.5V does not come up, Q38 is forward biased and current limiting is enabled which shuts down the -2V supply.

D. HP 2161A POWER SUPPLY PHYSICAL DESCRIPTION

1. Fuses (Figure 5-11)

a. Location

(1) Fuses F1, F12, and F13 are accessible on rear panel.

(2) All other fuses accessible under top cover.

b. Ratings

HP2161A POWER SUPPLY

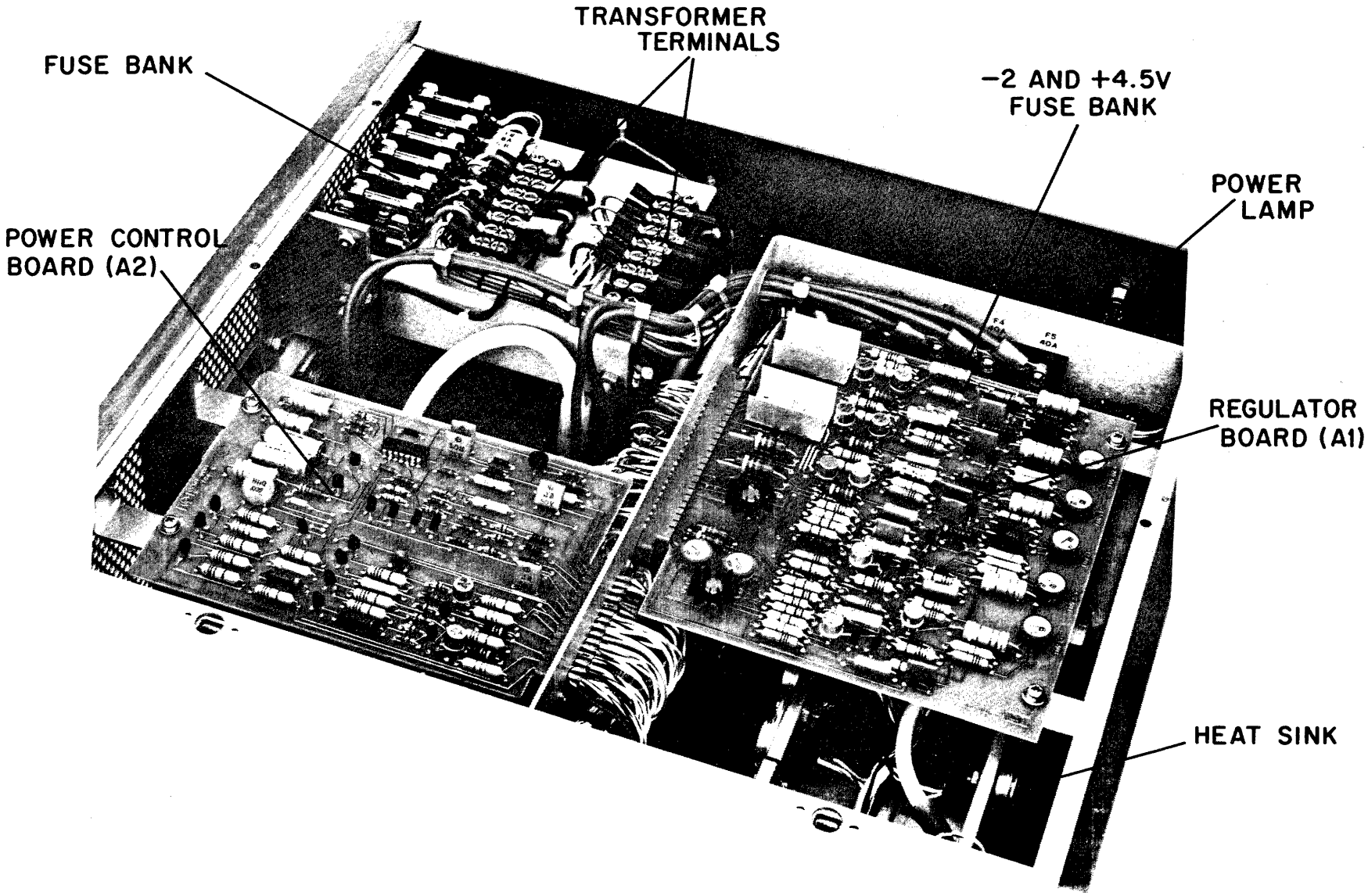


FIG.5−11

(1) The fuse ratings are:

F1	(Main Power Fuse)	-15A S. B.
F2	(-9V Supply)	-3. 2A S. B.
F3-F6	(+4. 5V & -2V Supply)	-40A
F7	(+18V Supply)	-8A S. B.
F8	(-18V Supply)	-8A S. B.
F9	(+33V Supply)	-8A S. B.
F10	(+50V Supply)	-0. 8A S. B.
F11	(-50V Supply)	-0. 8A S. B.
F12	(+6V Supply)	-4A S. B.
F13	(+33V Supply)	-1/4A

2. PC Boards

a. Location

(1) The Regulator Board (A1) and Power Control Board (A2) are located in the HP 2161A.

(2) The Crowbar Assembly (A201) is located on the bottom chassis in the HP 2115A.

b. Purpose

(1) Regulator Board (A1)

(a) This board contains the Voltage Regulators and Current Limiters for the five regulated supplies: +4. 5V, -2V, -12V and +20V.

(2) Power Control Board (A2)

(a) This board contains the power turn-on (PON) and power turn-off (POF) circuits. This board senses all regulated supplies for proper operation.

(b) This board also provides the drive for the POWER lamp.

(3) Crowbar Assembly (A201)

(a) This board provides the over-voltage protection for the +4.5V and -2V supplies. This board is located in the HP 2115A.

3. Blowers

a. Location

(1) Blowers M1 and M2 in the HP 2161A are located on the rear panel.

(2) Blowers M1 and M2 in the HP 2115A are located on the rear panel.

b. Purpose

(1) All blowers are interchangeable.

4. Limiting Resistors

a. Location

(1) These resistors are located on right-hand side of power pack.

b. Purpose

(1) These resistors are negative coefficient resistors used to provide temperature compensation for the +4.5V and -2V regulated supplies.

5. Line Filter

a. Location

(1) The line filter (FLI) is located in the HP 2161A.

b. Purpose

(1) The purpose of the line filter is to filter line ripple.

E. HP 2161A POWER SUPPLY OPERATIONAL BLOCK DIAGRAM (1.0 Hour)

1. Primary Power (HP 2161A Schematic)

   a. Line Power

      (1) Line power is provided via receptacle J1, the POWER switch on the HP 2115A, and power transformer T1.

      (2) Line Power is routed to the HP 2115A via connector J2 (pins A-B and C-D).

   b. Blowers

      (1) Power for blowers M1 and M2 in the HP 2161A is taken from terminals 1 and 3 on the power transformer.

      (2) Power for blowers M1 and M2 in the HP 2115A is taken from terminals 2 and 4 on the power transformer (via connector J2-Z, D).

2. Secondary Power (HP 2161A Schematic)

   a. Fuses and Rectifiers

      (1) The entire secondary is fused for maximum protection.

      (2) The rectifiers develop the following voltages:

          -5V
          -9V
          -3V
          +4.5V
          +18V
          -18V
          +33V
          +50V
          -50V
          +6V

   b. Series Regulators

      (1) Each regulated supply has a series current regulator. These regulators are located on the large heat sink assembly. The +4.5V, -2V, -12V and +20V supplies also have drivers.

          (a) The -2V series regulator consists of driver Q1 and series elements Q2 through Q4.

(b) The +4.5V series regulator consists of driver Q5 and series elements Q6 through Q8.

(c) The +12V series regulator consists of series element Q9.

(d) The -12V series regulator consists of driver Q10 and series element Q11.

(e) The +20V series regulator consists of driver Q12 and series element Q13.

(2) Resistors R10-R12 and R14-R16 are limiting resistors used as temperature compensation for the +4.5V and -2V regulated supplies.

3. Regulator Board A1 (Regulator Board Schematic)

a. +4.5V Regulator

(1) The +4.5V voltage regulator consists of differential amplifier Q3, Q4, and emitter-follower Q1.

(2) The +4.5V current limiter consists of Q2 and emitter follower Q1.

(3) The +4.5V and -2V interlock circuit consists of Q23 which is normally biased off by the -2V supply.

b. -2V Regulator

(1) The -2V voltage regulator consists of differential amplifier Q7, Q8 and emitter follower Q5.

(2) The -2V current limiter consists of Q6 and emitter follower Q5.

c. -12V Regulator

(1) The -12V voltage regulator consists of differential amplifier Q21, Q22 and emitter follower Q19.

(2) The -12V current limiter consists of Q20 and emitter follower Q19.

d. +12V Regulator

(1) The +12V regulator consists of differential amplifier Q17, Q18 and emitter followers Q15 and Q14. Two emitter followers are used here for added drive because of the light load this supply handles.

(2) The + 12V current limiter consists of Q16 and emitter followers Q15, Q14.

e. + 20V Regulator

(1) The + 20V voltage regulator consists of differential amplifier Q12, Q13 and emitter followers Q10 and Q9. Two emitter followers are used here also for added drive.

(2) The + 20V current limiter consists of Q11 and emitter followers Q10 and Q9.

f. Turn-Off Circuit

(1) There are two turn-off circuits on this board: The + 4.5V and -2V interlock (Q23), and the -12V turn-off circuit.

(a) The + 4.5V and -2V interlock ensures that the + 4.5V supply goes down when the -2V goes down.

(b) The normal turn-off circuit is enabled by the "power supply turn off" signal appearing at pin L. When this signal goes negative, all supplies are turned off.

4. Power Control Board A2 (Power Control Schematic)

a. Power Fail Circuit

(1) The power-fail circuit consists of three different configurations:

(a) A low-voltage sensing circuit, consisting of transistors Q-16-Q19, and associated Zeners, inhibits the PON signal (via MC1A). The "power-fail" signal enables the POFP signal on the Front Panel Coupler Board (A101) in the HP 2115A.

(b) The second power-fail circuit is comprised of Q1-Q12 and the "OR" circuit CR1-CR5. These circuits detect a current limiting condition on the Regulator Board (A1) and enable the "power-fail" signal.

(c) An "external power-fail" signal (from the HP 2160A Power Extender) will also enable the "power-fail" signal (via MC1B)

b. Power Turn-On Circuit

(1) The power turn-on circuit is simply MC1A. Initially, MC1A is disabled. After the five regulated supplies come up to rated voltage, MC1A is enabled and the PON signal is routed to the Front Panel Coupler. MC1B is used to detect an "external power fail" only.

c. Power Turn-Off Circuit

(1) The power turn-off circuit consists of transistors Q13 and Q14 (on the Power Control Board), thermal switch S1 on the heat sink, thermal switch S1 on the STG board (A13) in the HP 2115A, and thermal switch S1 in the HP 2160A Power Extender (Option K36).

(2) If any thermal switch opens, +4.5V is removed from Q13 and a "power supply turn-off" signal is generated to the Regulator Board (A1). This signal turns all regulated supplies off. Note that this is the only time all supplies are turned off (as contrasted to the HP 2116A).

5. Crowbar Assembly (HP 2115A-A201 and HP 2161A Power Supply Schematics)

a. Over-Voltage Protection

(1) The crowbar assembly consists of the Crowbar Board (A201) and the polarity sensing circuits in the HP 2115A. Over-voltage protection is provided for the +4.5V and -2V regulated supplies only.

b. SCR Control Circuit

(1) The SCR control circuit consists of Q1-Q3 on the Crowbar Assembly (A201) and Q1-Q2 on the back-plane panel in the HP 2115A. Either supply may short both supplies to ground under an over-voltage condition.

6. Front Panel Coupler (HP 2115A-A101 Schematic)

a. -2V Control

(1) The -2V is used to disable all SWITCH REGISTER gates when the switches are down. It is also used to load these gates when they are enabled.

b. +4.5V Control

(1) The +4.5V is used to enable all front panel controls on the HP 2115A. It is also used to enable the SWITCH REGISTER gates when the switches are up.

(2) The +4.5V also enables the LPS signal when the LOADER switch is in the PROJECTED position.

c. Power-On Control

(1) The PON signal originates on the Power Control Board (A2) in the HP 2161A. If it goes low, MC126A is enabled and the POFP signal is routed to the STG board (A13) in the HP 2115A.

d. Power-Fail Control

(1) The "power-fail" signal originates on the Power Control Board (A2) in the HP 2161A. This signal enables MC83B which generates a POFP signal to the STG board (A13) in the HP 2115A.

7. Review

a. How many regulated supplies are provided in the HP 2161A?

b. What are the five regulated supplies in the HP 2161A?

c. What is the purpose for the Series Regulator?

d. What are the limiting resistors used for?

e. What is the purpose of the Regulator Board (A1)?

f. What is the purpose of the Power Control Board?

g. What is the purpose of the Crowbar Assembly?

h. Where is the PON signal generated?

i. Where is the POFP signal generated?

j. Which supply enables the front panel controls on the HP 2115A?

HP 2161A POWER SUPPLY DETAILED CIRCUIT THEORY (1.5 Hours)

1. Series Regulator (HP2161A Power Supply Schematic)

   a. -2V Supply

      (1) The -2V series regulator consists of driver Q1 and series elements Q2-Q4. Limiting resistors R10-R12 provide temperature compensation.

      (2) The driver is driven by the -2V drive derived from the Regulator Board (A1).

      (3) Each series element's emitter is sensed (-2V current sense) to detect abnormal current drain.

      (4) The common -2V bus is sensed (-2V sense) by both the Regulator (A1) and the Power Control (A2) Boards to either regulate or shut down the -2V supply.

      (5) The emitter of the driver is also sensed (-2V drive sense) by the HP 2160A Power Supply Extender (via J4-9).

      (6) The -2V bus is routed to the HP 2115A (via J3-C) and then applied to the Crowbar Assembly (A201) and the crowbar circuit on the back plane.

   b. +4.5V Supply

      (1) The +4.5V series regulator is nearly identical to the -2V series regulator. The differences are:

         (a) Driver Q5 and series elements Q6-Q8.

         (b) Limiting resistors R14-R16.

         (c) The driver is driven by +4.5V.

         (d) The emitter of the driver is sensed (+4.5V drive sense) via J4-8.

         (e) The +4.5V bus is routed to the HP 2115A via J3-A.

c. +12V Supply

(1) The +12V series regulator consists entirely of series element Q9. The series element is driven by +12V and the bus is routed to the HP 2115A via J3-F.

d. -12V Supply

(1) The -12V series regulator consists of driver Q10 and series element Q11. The driver is driven by -12V and the bus is routed to the HP 2115A via J3-E.

e. +20V Supply

(1) The +20V series regulator consists of driver Q12 and series element Q13. The driver is driven by +20V and the bus is routed to the HP 2115A via J3-G.

2. Regulator Board (Power Supply Schematic)

a. Voltage Regulators

(1) The +4.5V and -2V voltage regulators are interlocked through Q23 and CR9-CR10. With CR9-CR10 forward biased and the -2V current limiter biased off, Q23 is normally biased off. If the -2V supply goes down, CR9-CR10 are reverse biased and Q23 is turned on. This drops the base voltage to the +4.5V driver (Q1) and the +4.5V supply is shut down.

(2) The voltage regulators and current limiters in the HP 2161A are nearly identical to those in the HP 2116B. The differences are:

(a) All three series elements for the -2V and +4.5V are sensed for current limiting.

(b) The turn-off circuit is enabled by a negative "power supply turn-off" signal originating on the Power Control Board (A2).

(c) The -2V supply is forced into current limiting, when the +4.5V shuts down, since it is forced to carry the current load for the +4.5V bus.

(d) The -12V regulator turns off only the +12V and +20V supplies when it shuts down.

(e) Amplifier Q24 is needed to ensure that the "power supply turn off" signal turns off the -12V regulator.

b. Adjustments

(1) Each regulator has a voltage adjustment accessible on top of the Regulator Board.

(2) Only the +4.5V and -2V regulators have current limiting adjustments. These adjustments are set so that current limiting is enabled when any series element draws more than 8.3A.

3. Power Control Board (Power Control Schematic)

a. Power Supply Turn-Off

(1) In the HP 2161A all regulated supplies are turned off only when a thermal switch opens. There are three thermal switches which may enable the "power supply turn-off" signal:

(a) S1 in the HP 2161A (located on heat sink).

(b) S1 in the HP 2115A (located on STG board).

(c) S1 in the HP 2160A (located on heat sink).

(2) The power supply turn-off circuit consists of Q13 and Q14. Transistor Q13 is normally biased off by +4.5V applied through the thermal switches. If a thermal switch opens, Q13 is forward biased and this turns Q14 off. When Q14 turns off, -9V is routed to the Regulator Board (A1) as the "power supply turn-off" signal.

b. Power Fail Circuit

(1) The "power fail" signal may be enabled in one of two ways:

(a) Initially, when power is applied, the regulated supplies are low. Zeners CR14-CR17 cannot fire and diodes

CR11-13 are forward biased. Transistor Q16 is turned on and this inhibits MC1A making the PON signal low. At the same time, the "power fail" signal is routed to the Front Panel Coupler (A201) in the HP 2115A. When all supplies come up, neither Q16, Q17, Q18 or Q19 can conduct, and MC1A is enabled.

(b) If any supply fails, a positive "power fail" signal is sent via CR1-CR5 directly to the Front Panel Coupler.

(2) The POFP signal is actually generated on the Front Panel Coupler when it receives the "power fail" signal.

(3) An "external power fail" signal from the HP 2160A may also enable MC1B and generate a "power fail" signal.

c. Power-On-Normal (PON)

(1) The PON signal is generated as described above. The "external power on" signal is used only with the Auto Restart Option. It enables the PON signal if the +12V supply should go down.

d. Power Lamp

(1) The POWER lamp is driven by Q15 when the PON signal comes up.

4. Crowbar Assembly (HP 2115A-A201)

a. +4.5 Protect

(1) The Crowbar Board (A201) in the HP 2115A contains only the control transistors (Q1, Q2 and Q3); the SCR (Q1) and the grounding diodes are located on the back plane.

(a) Q1 and Q3 are normally biased off. If the +4.5V rises above 5.5V, Zener CR1 fires and Q1 and Q3 are turned on. With Q3 turned on, the positive collector voltage is applied to both the +4.5V and -2V SCR's; both supplies are then shorted to ground and current limiting is enabled.

b. -2V Protect

(1) The -2V crowbar operates similarly to the +4.5V crowbar. When the -2V supply rises above -2.7V, Q2 is turned on. This again turns on Q3 and both SCR's fire shutting down both supplies.

(2) Note that if the -2V should go down, Q1, Q2 are again fired.

c. Polarity Protect

(1) The polarity protection diodes (CR1-CR5) operate identical to those in the HP 2116B. There is one diode for each regulated supply.

5. Review

a. Where does the "power supply turn off" signal originate?

b. What supplies are turned off when the +4.5V supply goes into current limiting?

c. What supplies are turned off when the -12V supply goes into current limiting?

d. Under what conditions do all supplies turn off?

e. When using the HP 2160A Extender, how many thermal switches are activated, and where are they located?

f. Where does the "power fail" signal originate and terminate?

g. Where does the POFP signal originate?

h. What signal from the HP 2161A enables the POFP signal?

i. What signal from the HP 2160A Extender enables the "power fail" signal in the HP 2161A?

j. What visual indication would be obvious if the PON signal were not to come up?

G. HP 2160A POWER SUPPLY EXTENDER (0.5 Hour)

1. HP 2116B/HP 2115A Interface (HP 2160A Schematic and Figure 5-12).

a. Power Requirements

(1) The HP 2160A Power Supply Extender (Option K36) provides 10A at -2V and 20A at +4.5V. As in the other power supplies, the +4.5V bus can provide its rated load plus the -2V load.

b. Connectors

(1) Connector J1 is the primary power line connector.

(2) Connector J2 connects to either the HP 2116B or the HP 2115A. This routes the -2V, +4.5V and power ground buses to the HP 2116B or HP 2115A.

(3) Connector J3 connects to either J2 on the HP 2116B, or connector J4 on the HP 2161A. This is the primary control interconnection.

(4) Connector J4 is used only with the HP 2150A I/O Extender (Option K38).

2. Primary Power (HP 2160A Schematic)

a. Fuses

(1) The primary and secondary of power transformer T1 are completely fused to provide maximum protection.

(a) Fuses and ratings are:

F1 (Primary power)	-5A S.B.
F2 (-9V Supply)	-2A S.B.
F3, F6 (-2V Supply)	-15A S.B.
F4, F5 (+4.5V Supply)	-15A S.B.
F7, F8 (±20V Supply)	-0.3A S.B.

b. Blower

(1) The HP 2160A has one blower (M1) connected across the primary of T1.

c. Lamp

(1) The power lamp DS1 is connected across the primary of T1.

3. Secondary Power (HP 2160A Schematic)

   a. Rectifiers

      (1) The bridge rectifier A1CR12-A1CR15 provides + 20V, -20V and -5.11V unregulated dc for internal use.

      (2) The bridge rectifier A1CR1-A1CR4 provides -9V unregulated dc for internal use.

      (3) Full-wave rectifier CR1 and CR4 provides the -2V regulated dc for external use.

      (4) Full-wave rectifier CR2 and CR3 provides the + 4.5V regulated dc for external use.

   b. Series Regulators

      (1) The series regulator for the -2V regulated supply consists of driver Q4, series elements Q5, Q6; and limiting resistors R10, R11.

      (2) The series regulator for the + 4.5V regulated supply consists of drivers Q1, series elements Q2, Q3; and limiting resistors R7, R8.

4. Supply Regulator (A1) (HP 2160A Schematic)

   a. + 4.5V Regulator

      (1) The + 4.5V regulator circuit is nearly identical to those used in the HP 2116B and HP 2161A.

         (a) The regulator consists of differential amplifier Q2, Q3; current sense amplifier Q4, and emitter-follower Q1.

         (b) The + 4.5 drive for the regulator is entered via J3-8.

   b. -2V Regulator

      (1) The -2V regulator is nearly identical to the + 4.5V regulator. It consists of:

         (a) differential amplifier Q8, Q9

         (b) current sense amplifier Q10

         (c) emitter-follower Q11

   c. + 20V Regulator

      (1) The + 20V bus uses Zener CR10.

   d. -20V Regulator

      (1) The -20V bus uses Zener CR11.

e. -5.11V Regulator

(1) The -5.11V bus uses Zener CR6

f. Power Fail Circuit

(1) The -2V external power fail circuit consists of Q12, Q7 and CR8. With the -2V series regulator operating properly, Q12 is normally conducting, and Q7 is biased off. If the series regulator is turned off, Q12 is biased off, Q7 is turned on, and a positive "external power fail" signal is coupled to the HP 2116B or HP 2161A via CR8 and J2-3.

(2) The +4.5V external power fail circuit consists of Q5, Q6 and CR7. Its operation is identical to the -2V circuit.

5. Review

a. How much current can the HP 2160A provide at -2V and +4.5V.

b. Which connector interfaces with the HP 2116B or HP 2115A?

c. Which connector interfaces with the HP 2116B or the HP 2161A?

d. Which connector interfaces with the HP 2150A?

e. In the +4.5V power fail circuit, which transistor is normally conducting?

HP 2116B POWER SUPPLY STATISTICS

V (volts)	% regulation	I (amps) max	Back Plane Current (amps)			
			4K		8K	
			(halt)	(run)	(halt)	(run)
+4.5	1	45				
-2.Ø	1	22.5				
+12	1	3				
-12	Ø.5	3				
+22*	Ø.5	1	Ø.16	Ø.46	Ø.32	Ø.62
-22**	Ø.5	2.5	1.2	1.4	2.3	2.6
+32***	Ø.5	2.5	Ø	2.Ø (TR=Ø)	Ø	2.Ø (TR=Ø)
+7	none	3.Ø	(current for all lamps lit)			

The 7V rms supply (full wave rectified and unfiltered) is used only for the front panel display lamps. One exception is the lamp behind the POWER pushbutton. This lamp is operated from the +12V supply and gives an indication of the status of the -12V TURN OFF circuit.

* +22V - (Ø.Ø4) (T-25°C) V Where T = ambient temperature of room

** -22V + (Ø.Ø4) (T-25°C) V Where T = ambient temperature of room

*** +32V - (Ø.Ø64) (T-25°C) V Where T = ambient temperature of room

HP 2116B POWER REQUIREMENT

REQUIREMENTS	SUPPLY CURRENTS (AMP)			
	+12V	-12V	-2V	+4.5V
CURRENT AVAILABLE FROM POWER SUPPLIES				
Computer Power Supply	3	3	22.5	*22.5
Computer and HP 2160A Power Supplies	3	3	32.5	**32.5
CURRENT REQUIRED BY COMPUTER WITH NO PROCESSOR OR INPUT/OUTPUT OPTIONS				
Computer with 8K Memory	540 ma	600 ma	15.2	26.4
Computer with 16K Memory	1.0	1.1	15.7	28.4
CURRENT AVAILABLE FOR OPTIONS				
Computer with 8K Memory	2.5	2.4	7.3	***11.3
Computer with 16K Memory	2.0	1.9	6.8	*** 9.8
Computer with 8K Memory and HP 2160A Power Supply Extender	2.5	2.4	17.3	***21.3
Computer with 16K Memory and HP 2160A Power Supply Extender	2.0	1.9	16.8	***19.8

NOTES:
* Plus the current drawn from the -2V supply by the Computer with memory and options. Maximum available from +4.5V supply is 45 amperes.

** Plus the current drawn from the -2V supply by the Computer with memory and options. Maximum available from +4.5V supply is 65 amperes.

*** Plus the current drawn from the -2V supply by the selected options.

POWER REQUIREMENTS FOR COMPUTER OPTIONS

OPTIONS		SUPPLY CURRENT REQUIRED (AMP)			
	PROCESSOR OPTIONS	+12V	-12V	-2V	+4.5V
12578A	Direct Memory Access	0.00	0.00	0.72	6.20
12579A	Extended Arithmetic Unit	0.00	0.00	3.30	4.68
12581A	Memory Protect	0.00	0.00	0.90	1.92
12582A	Direct Memory Increment	0.00	0.00	0.12	2.04
12588A	Power Fail with Auto Restart	0.06	0.04	0.00	0.00
12591A	Memory Parity Check	0.00	0.00	0.5	0.91
	INPUT/OUTPUT OPTIONS				
12531B	Teleprinter Input/Output,Buffered	0.05	0.10	0.05	0.76
12532A	High-Speed Punched Tape Input	0.03	0.01	0.48	1.10
12533A	Digital Voltmeter Program Output (2401C)	0.00	0.30	0.24	0.42
12535A	Crossbar Scanner Program Output	0.01	0.04	0.84	1.10
12536A	High-Speed Punched Tape Output	0.01	0.01	0.30	0.72
12537A	Incremental Magnetic Tape Output	0.00	0.06	0.48	0.90
12538A	Magnetic Tape Input/Output (7 Channel)	0.09	0.18	4.20	6.00
12539A	Time Base Generator	0.01	0.00	0.42	1.10
12540A	Data-Phone Interface (103A)	0.11	0.05	0.90	1.40
12541A 12543A	Digital Voltmeter Data Input (2401C and 3440A	0.05	0.01	0.30	0.96
12544A	Counter/Thermometer Data Input (8 Digits)	0.05	0.01	0.30	0.96
12548A	Counter Data Input (4, 5, 6 & 7 Digits)	0.05	0.01	0.30	0.96
12550A	Digital Voltmeter Program Output (2411A)	0.00	0.06	0.30	0.42
12551A	Relay Output Register (no Interrupt)	0.24	0.00	0.39	0.60
12551B	Relay Output Register (with Interrupt)	0.18	0.02	0.90	0.08
12554A	Duplex General Purpose Register	0.24	0.01	0.48	2.40
12555A	Digital-to-Analog Converter	0.25	0.30	0.90	2.00
12556A	40-Bit Output Register	0.07	0.00	0.06	0.80
12559A	9 Channel Magnetic Tape Input/Output	0.18	0.18	0.24	2.58
12561A	Disc Memory Interface	0.00	0.00	0.24	2.40
12564A	10-Bit A-to-D Converter	0.15	0.22	0.09	0.90
12566A	Microcircuit Interface	0.00	0.00	0.05	1.10
12596A	HP 2151A I/O Extender Interface	0.00	0.00	3.00	0.80
12597A	8-Bit Duplex Register (Positive-True)	0.18	0.02	0.80	0.05
	8-Bit Duplex Register Option 2 (Negative-True)	0.04	0.18	0.80	0.06

HP 2116B POWER SUPPLY

EXAMPLE OF CURRENT AVAILABLE AND REQUIRED

Computer Power Supply	+12V	-12V	-2V	+4.5V
Current Available	3	3	22.5	22.5*
				+15.7
				38.2
Current Required by 16K Memory	-1.0	-1.1	-15.7	-28.4
Current Available for Options	2.0	1.9	6.8	9.8
				+0.05
				9.85
Current Required by Teleprinter Option	-0.05	-0.10	-0.05	-0.76
	1.95	1.80	6.75	9.09
				+4.20
				13.29
Current Required by Mag Tape Option	-0.09	-0.18	-4.20	-6.00
CURRENT AVAILABLE FOR OTHER OPTIONS	1.86	1.62	2.55	7.29

* Plus current drawn from the -2V supply.

input/output

A. INTRODUCTION

1. I/O Cards

a. Control and Address Cards

(1) The computer contains one plug-in I/O Control card and one plug-in I/O Address card. The cards plug into the computer, adjacent to the interface cards. Both cards are connected in parallel with all interface cards in the computer. The I/O Control Card contains the master Interrupt System Enable FF, receives command and timing signals from the computer for transfer to the interface card slots, and provides the necessary gates and flip-flops for proper control of interface-card operation. The I/O Address card provides a decoding function for program selection of the desired interface card, and an encoding function for interface card interrupt identification.

b. Interface Cards

(1) Figure 6-1 illustrates the slots in the computer for the plug-in cards associated with Input/Output operation. Each of the interface-card slots actually has two Select Codes assigned to it. This provides for interface cards which contain both input and output logic circuits (e.g., Mag Tape Input and Output in Position 205). The input portion and the output portion of the card each require a separate Select Code. When an interface card contains addressable input and output logic, the adjacent slot (Position 206) cannot contain another addressable interface card. Instead, a Priority Jumper card must be inserted in the slot to maintain priority continuity. Since the slot connector wiring determines the Select Codes of the slots, and interface cards can be plugged into any slot, the interface card assumes the Select Codes of the slot it is plugged into.

HP 2116B BOARD LOCATION (FRONT VIEW)

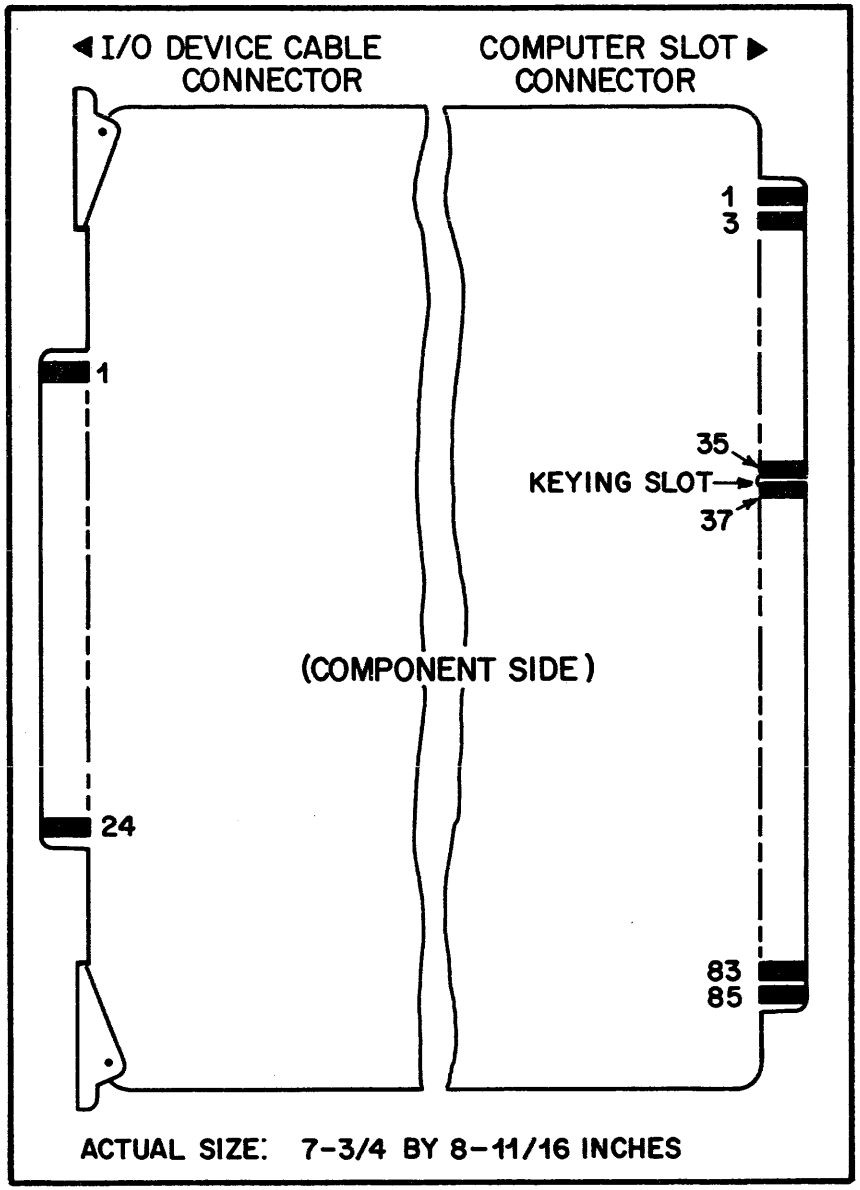
201	I/O CONTROL	02116-6041	101	FRONT PANEL COUPLER	02116-6184	1	PWR FAIL 02116-6175 PWR FAIL** (RESTART) 12588-6001
202	I/O ADDRESS ENCODE	02116-6194	102	ARITHMETIC 12-15	02116-6026	2	MMD 02116-6274
203	†(I/O 10/11)		103	ARITHMETIC 8-11	02116-6026	3	PE** 12591-6001
204	†(I/O 11/12)		104	ARITHMETIC 4-7	02116-6026	4	ID3 02116-6265
205	†(I/O 12/13)		105	ARITHMETIC 0-3	02116-6026	5	SPARE
206	†(I/O 13/14)		106	TIMING GENERATOR	02116-6281	6	ID2* 02116-6265
207	†(I/O 14/15)		107	INSTRUCTION DECODER	02116-6027	7	SPARE
208	†(I/O 15/16)		108	SHIFT LOGIC	02116-6029	8	DSY 2/3* 02116-6266
209	†(I/O 16/17)		109	EAU*	02116-6196	9	DSX 2/3* 02116-6266
210	†(I/O 17/20)		110	EAU*	02116-6202	10	SA3* 02115-6001
211	†(I/O 20/21)		111	SPARE		11	SA2* 02115-6001
212	†(I/O 21/22)		112	SPARE		12	SA 1* 02115-6001
213	†(I/O 22/23)		113	SPARE		13	SAØ 02115-6001
214	†(I/O 23/24)		114	SPARE		14	DSY Ø/1 02116-6266
215	†(I/O 24/25)		115	SPARE		15	DSX Ø/1 02116-6266
216	†(I/O 25/26)		116	DMA* 02116-6206 DMI* 02116-6221		16	ID1 02116-6265
217	†(I/O 26/27)		117	DMA*	02116-6206	17	SPARE
218	†(I/O 27/30)		118	DMA*	02116-6205	18	IDØ 02116-6265
219	**I/O EXTENDER	02116-6182	119	DMA*	02116-6204	19	SPARE
220	**I/O EXTENDER	02116-6183	120	DMA*	02116-6203	20	DML 02115-6044
221	** MEMORY EXTENDER	02116-6181		POWER SUPPLY TEST POINTS		21	MEMORY PROTECT** 12581-6001
222	** MEMORY EXTENDER	02116-6181				22	SPARE

* *OPTIONAL BOARDS MAY BE ADDED AT ANY TIME.*

** *OPTIONAL BOARDS MAY BE ADDED AFTER ADDITIONAL BACK PLANE WIRING*

† *I/O PLUG-IN OPTIONS MAY BE ADDED AT ANY TIME PROVIDING THE CURRENT REQUIREMENTS DO NOT EXCEED THE POWER SUPPLY RATINGS.*

FIG. 6-1



INTERFACE CARD CONNECTORS

FIG. 6-2

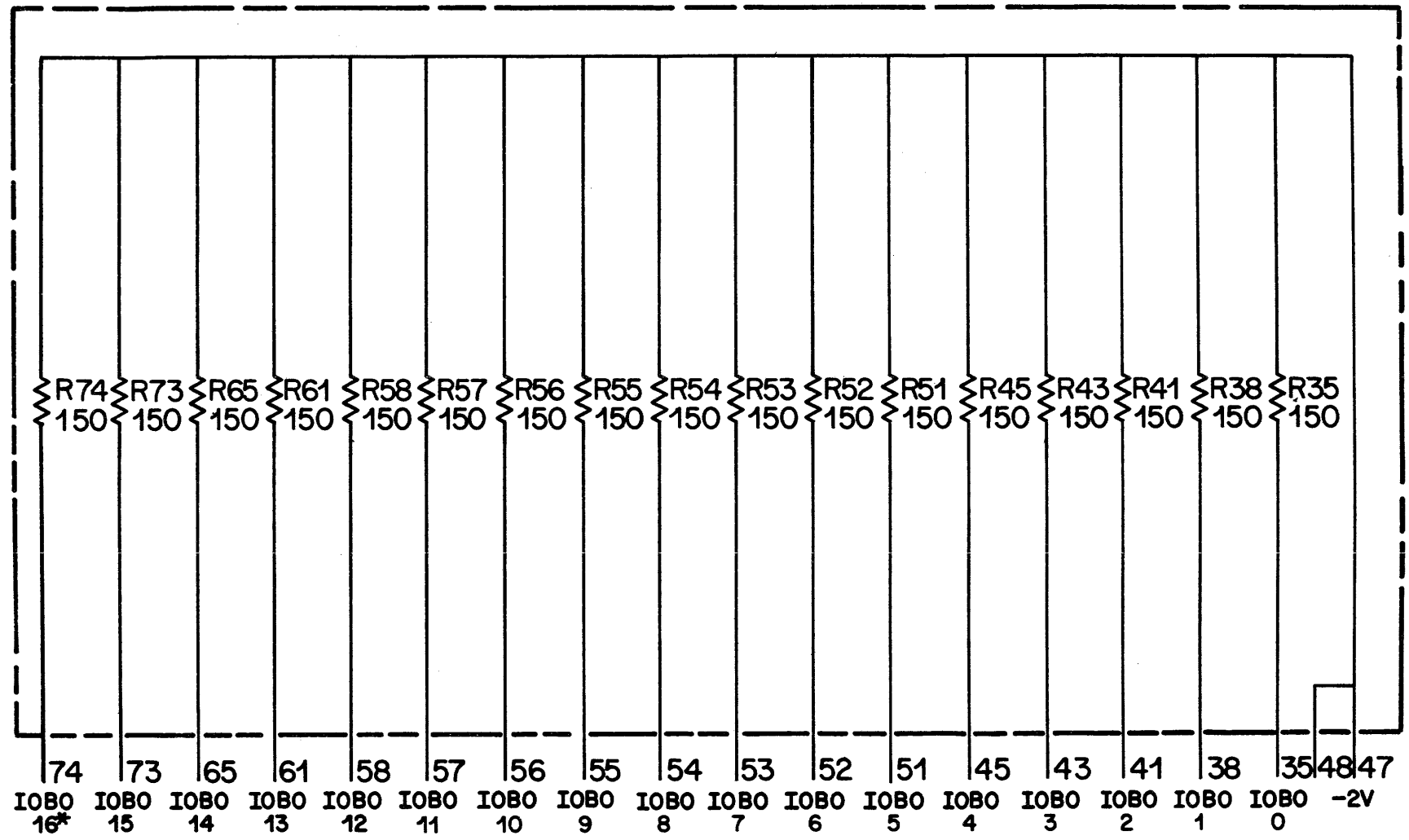
(Interface cards are assigned to particular slot positions before shipment of a computer system and may vary from system to system. The slot positions of the interface cards in Figure 6-1 are for illustration purposes only.)

(2) The interface cards provide channels through which data is transferred between the computer and the Input/Output devices, and provide control (via computer commands) of the Input/Output device operation. An interface card may contain up to 16 Buffer FFs for temporary storage of data to be transferred to the computer or the Input/Output device. The number of Buffer FFs on a particular interface card depends on the type of device connected to it. Other logic circuitry on the interface card also depends on the device to which it is connected. Certain devices are capable of interrupting the computer program, while for others this capability is not necessary; certain devices require control signals for movement of tape while others do not, and timing requirements for some devices must be provided on the interface card. In some special cases, more than one interface card is required for an external device.

(3) Each interface card has two connectors, one on each end of the card. The connector with pins numbered 1-24 receives the I/O device cable. The connector numbered 1-85 plugs into one of the 16 available I/O slots. Odd numbered pins are on the component side and even numbered pins are on the non-component side (Refer Figure 6-2).

c. Resistance Load Card (Figure 6-3)

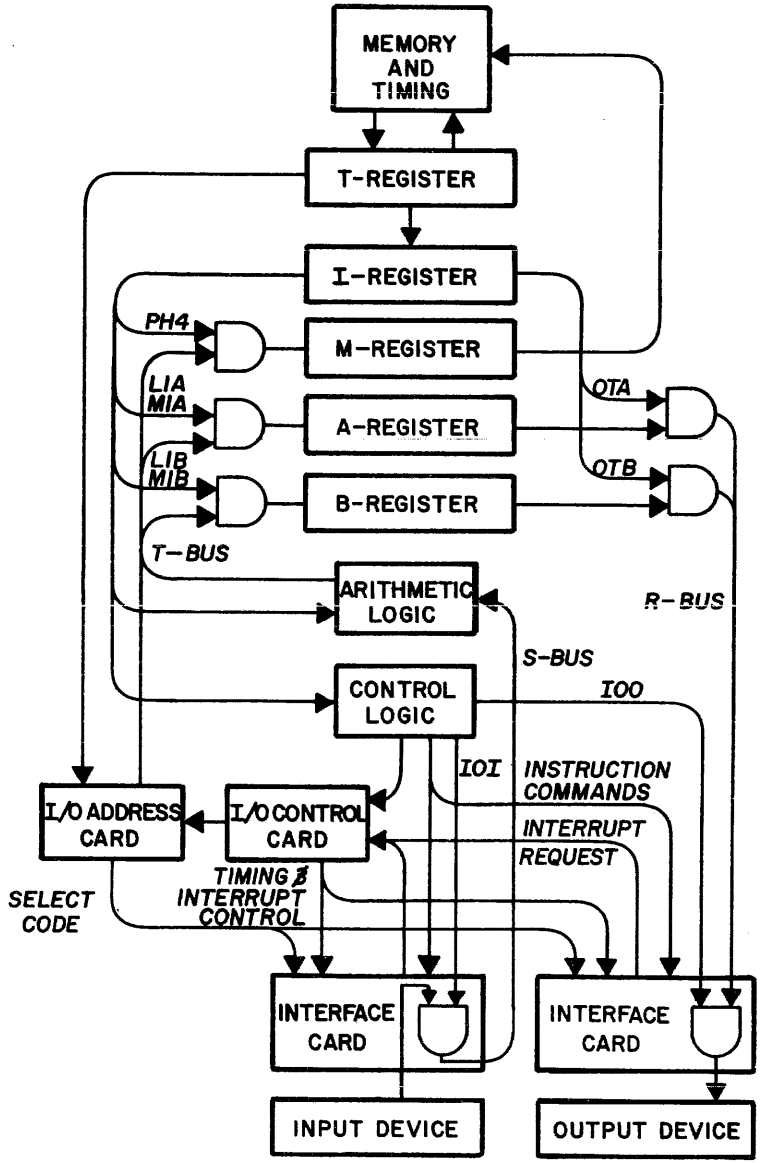
(1) The computer contains one plug-in Resistance Load card. This card provides 17 (150-ohm) resistors connected to the -2 volt supply to load the termination of the IOBO (I/O Bus Output) lines from the computer to the interface cards. The card plugs into Position 218 (the last interface-card slot) of the Input/Output slots of the computer. The card remains in slot position 218 unless the total interface and Priority Jumper cards used in the system equal 16. At that time, the card is no longer required and must be removed.



* NOT PRESENTLY USED

RESISTANCE LOAD CARD (Schematic Diagram)

FIG. 6-3



BLOCK DIAGRAM of SYSTEM INPUT/OUTPUT OPERATION

FIG. 6-4

2. Input/Output Block Diagram (Figure 6-4)

a. The I/O System

(1) Figure 6-4 shows the main elements concerned with the control of I/O operations. Interface arrangements are shown for only two external devices although as many as 55 devices may exist. The elements shown process all I/O operations as follows:

(a) process I/O instructions

(b) process interrupt requests from external devices

b. I/O Instruction Logic

(1) Input/Output instructions from memory via the T-Register are decoded by the I-Register and routed to the various register gate inputs, and to the Control Logic which translates the instructions into appropriate driving signals. Instruction commands are routed to a particular interface card and external device as determined by the Select Code from the T-Register via the I/O Address card. These signals can set or reset the Control and Flag Flip-Flops (FFs) on the interface cards and can test the set or reset condition of these FFs. The Control and Flag FFs are used for transferring data between the interface card and the external device.

(2) The IOI (I/O Input) signal strobes all interface cards for input data as a result of a Load Into A (LIA), Load Into B (LIB), Merge Into A (MIA), or a Merge Into B (MIB) instruction. Only the data from the interface card selected by the Select Code can be enabled. The data is strobed by the IOI signal onto the "S" bus. From there it is transferred via the Arithmetic Logic (to alter or combine the data) and the "T" bus to the A or B-Register. The particular register which will receive the data is determined by the LIA/B or MIA/B signal present at the register input gate.

(3) Another driving signal from the Control Logic, the IOO (I/O Output) signal, strobes all interface cards to output data as a

result of an OTA (Output from A) or an OTB (Output from B) instruction. The Select Code from the T-Register via the I/O Address card permits the IOO signal to strobe the data on the IOBO bus into the appropriate interface card and external device. (The data was placed on the IOBO bus from the A- or B-Register via the R Bus as a result of the OTA/B instruction.)

c. Interrupt Requests

(1) If a specific instruction to the I/O Control card has at some previous time enabled the interrupt system, an external device may request an interrupt to the computer program to obtain new data from the computer or to feed new data to the computer. This interrupt request is received by the I/O Control Card. The I/O Control card signal to the I/O Address card causes it to interrupt the computer program by forcing the M-Register to be set (via the "T" bus) to a memory location corresponding to the Select Code of the interrupting device. This occurs during the interrupt Phase 4 machine cycle. The Fetch phase is then entered to make the computer execute the instruction contained in the specified memory location. Generally, this instruction will be a jump (JSB) to a service subroutine which will prepare or accept the new data. On completion of service, the subroutine must cause a return to the proper location in the main program.

3. Review

(1) Which I/O card contains the master interrupt system?

(2) Odd-numbered pins on the I/O Interface cards are on which side of the cards?

(3) When should the Resistance Load card be removed?

(4) What determines where the I/O instruction commands generated in the Control Logic go?

(5) What are the Flag and Control Flip-Flops on the I/O Control Board used for?

(6) What signal strobes input data onto the "S" bus? When is it true?

(7) What signal strobes output data onto the "R" bus? When is it true?

(8) What phase always immediately follows an Interrupt Phase 4?

(9) Generally, what will be the first instruction contained in an interrupt location?

(10) Generally, what will be the last instruction in an interrupt subroutine?

B. INTERRUPT SYSTEM

1. Assignment and Priority

a. Select Code Assignment

(1) Select Code ØØ is the access to the master Interrupt System Enable FF on the I/O Control card. Codes Ø1 through Ø6 are reserved for processor Input/Output functions or options. Codes 1Ø through 77 (octal) are used for selection of the 55 possible Input/Output devices, each capable of causing an interrupt. The interrupt location in memory corresponds to the select code for each device.

b. Interrupt Requests

(1) An interrupt request from an external device occurs when the following conditions are met:

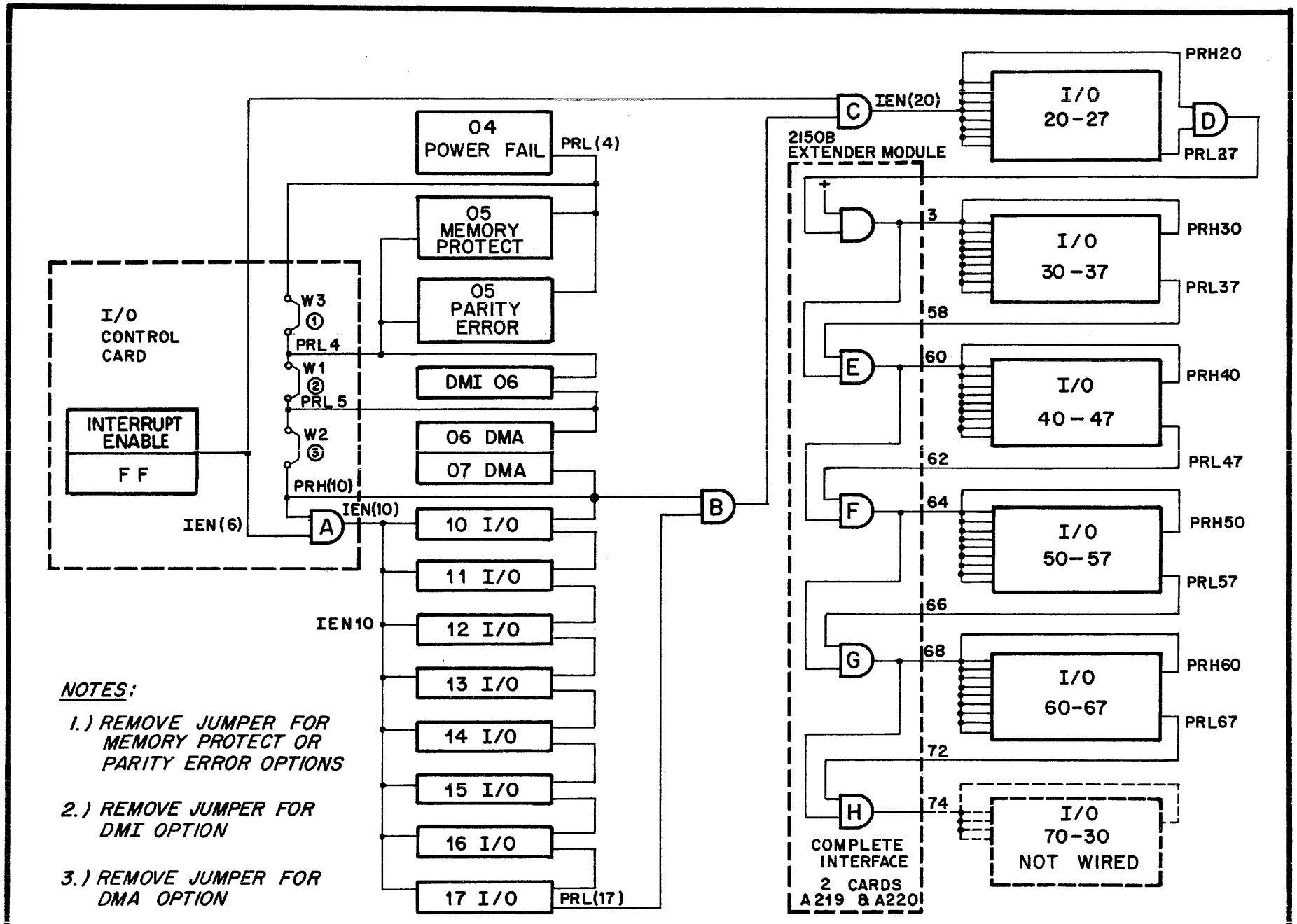
(a) The Interrupt System is enabled.

(b) The Flag FF of the specific device interface card is set.

(c) The Control FF of the specific device interface card is set.

(d) No priority-effecting instruction (STF, CLF, STC and CLC) is in progress.

(e) No higher-priority devices satisfy the conditions of steps "a" through "d".



INTERRUPT PRIORITY SYSTEM

FIG. 6-5

c. Interrupt Priority

(1) Figure 6-5 illustrates the continuity of the interrupt priority network for all possible Input/Output interface cards and processor option cards capable of interrupting the computer. The Interrupt System Enable FF and gates A, B, and C are located on the I/O Control Card. Gates D through H are contained in their respective Extender Module.

(2) Since the Power Failure Interrupt option (Select Code Ø4) is assigned the highest priority, it can interrupt the computer regardless of the state of the Interrupt System Enable FF. For all other interface cards and options, the FF must be set before an interrupt can occur. When an interface card requests an interrupt, its false PRL signal is applied to the next interface card as a false PRH signal to prevent it from requesting an interrupt. This sequence continues from card to card until the last interface card receives a flase PRH signal. If a large number of interface cards are used in the system and a card of high priority requests an interrupt, the switching times required by the cards may cause a delay sufficient to enable a card of low priority to interrupt before its PRH signal input becomes false, causing dual interrupt requests. To prevent this condition from occurring, AND gates are provided for each set of eight cards in parallel and therefore can disable all eight cards simultaneously. Thus, when an interrupt request occurs, the PRL-PRH switching sequence proceeds to the AND gate following the group of eight cards in which the interrupt request occurs. The false input to the AND gate causes a false IEN output and all following interface cards are immediately disabled.

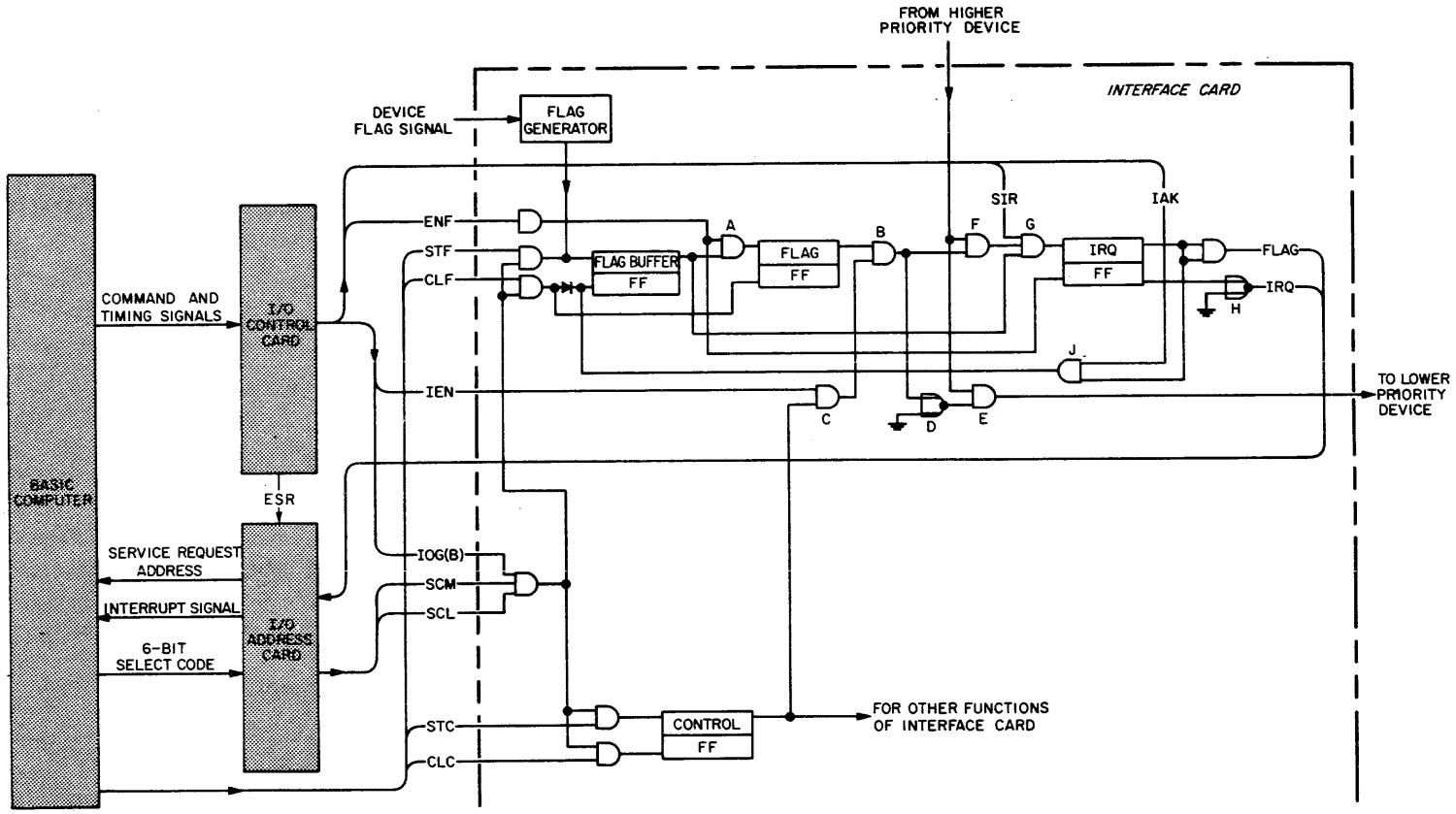
(3) An HP 2150B Extender Module must be used when more than 16 interface cards are required for the computer system. Since the basic computer control logic will not be present in the extender module, all three plug-in card sections are

available for expanding the memory and Input/Output capabilities. Up to 32 interface cards may be plugged into the extender module. (With the 16 interface cards plugged into the basic computer, the extender module extends the total interface-card capability of the computer system to 48 interface cards.)

d. Interrupt Operation (Figure 6-6)

(1) When the external device has completed its operation, it generates a Device Flag signal to the Interface-card Flag Generator which sets the Flag Buffer FF. The output of the Flag Buffer FF, in conjunction with the ENF (Enable Flag) signal from the I/O Control card at time T2 causes AND gate A to set the Flag FF. The Flag FF output is "anded" at gate B with the output of AND gate C. The gate C output is true when the Control FF is set and when the IEN (Interrupt Enable) signal is received from the I/O Control card. Unless the Control FF is set by a Set Control (STC) instruction, an interrupt request cannot occur.

(2) The Control FF is set under program control and therefore, may be set at any T4 time of a machine cycle, depending on the type of operation being performed. The STC instruction is enabled to the Control FF by the SCM (Select Code Most significant digit) and SCL (Select Code Least significiant digit) signals from the I/O Address card, and the IOGE (I/O Group instruction, Buffered) signal from the I/O Control card. The SCM and SCL signals are enabled on the individual interface card by the IOGE signal which occurs when the instruction to be performed is an I/O Group instruction. When the Control FF sets, a true input is applied to AND gate C. The inputs to AND gates B and C are then true and gate B applies a true output to inverting NOR gate D. The false output of gate D disables AND gate E, making the priority network bus to the lower-priority devices false. This prevents any device of lower priority from requesting an interrupt.



SIMPLIFIED INTERRUPT DIAGRAM

FIG. 6-6

(3) At the same time that gate B applied a true output to gate D, it also applied a true output to AND gate F. The priority network signal to gate F will be true if an interface card (device) of higher priority than the one represented is not requesting an interrupt. In this case, the true output of gate F is combined with the SIR (Set Interrupt Request) signal from the I/O control card at time T5 and the output of the set Flag Buffer FF to provide a true output from AND gate G. The gate G output sets the IRQ (Interrupt Request) FF.

(4) The IRQ FF outputs provide the Flag signal and the IRQ signal to the I/O Address card. (The IRQ signal is obtained by the inversion of the false reset-side output of the IRQ FF by inverting NOR gate H.) The Flag signal is "anded" in the I/O Address card with the Enable Service Request (ESR) signal from the I/O Control card to form an interrupt signal. However, the ESR signal is false for the remainder of the machine cycle during which an instruction occurs that effects device priorities (STC) as determined by the I/O Control card. At time T2, the IRQ FF is reset by the ENF signal to allow a higher-priority device to request an interrupt. If the Control FF is still set and no higher-priority devices have requested an interrupt, the IRQ FF will again be set at time T5 (SIR). The Flag and IRQ signals are again sent to the I/O Address card. The signals are used to form a 6-bit Service Request Address to be enabled to the computer at time T7 of Interrupt Phase 4. The Flag signal and the now-true ESR signal form the Interrupt signal which is sent to the computer. This signal causes an interrupt at the end of the current machine phase, switching the computer into the Interrupt Phase except when any of the following conditions occur:

(a) The computer is in the HALT mode.

(b) A Jump Indirect (JMP, I) or a Jump to Subroutine Indirect (JSB, I) instruction is not fully executed. (These instructions inhibit all interrupts until fully executed for any

number of indirect levels of addressing. At the earliest, an interrupt request will be granted at the end of the machine phase immediately following one or more JMP, I or JSB, I instructions.)

(c) A Direct Memory Access (DMA) option is in process of transferring data. Exception: The Power Failure Interrupt Option can interrupt a DMA transfer.

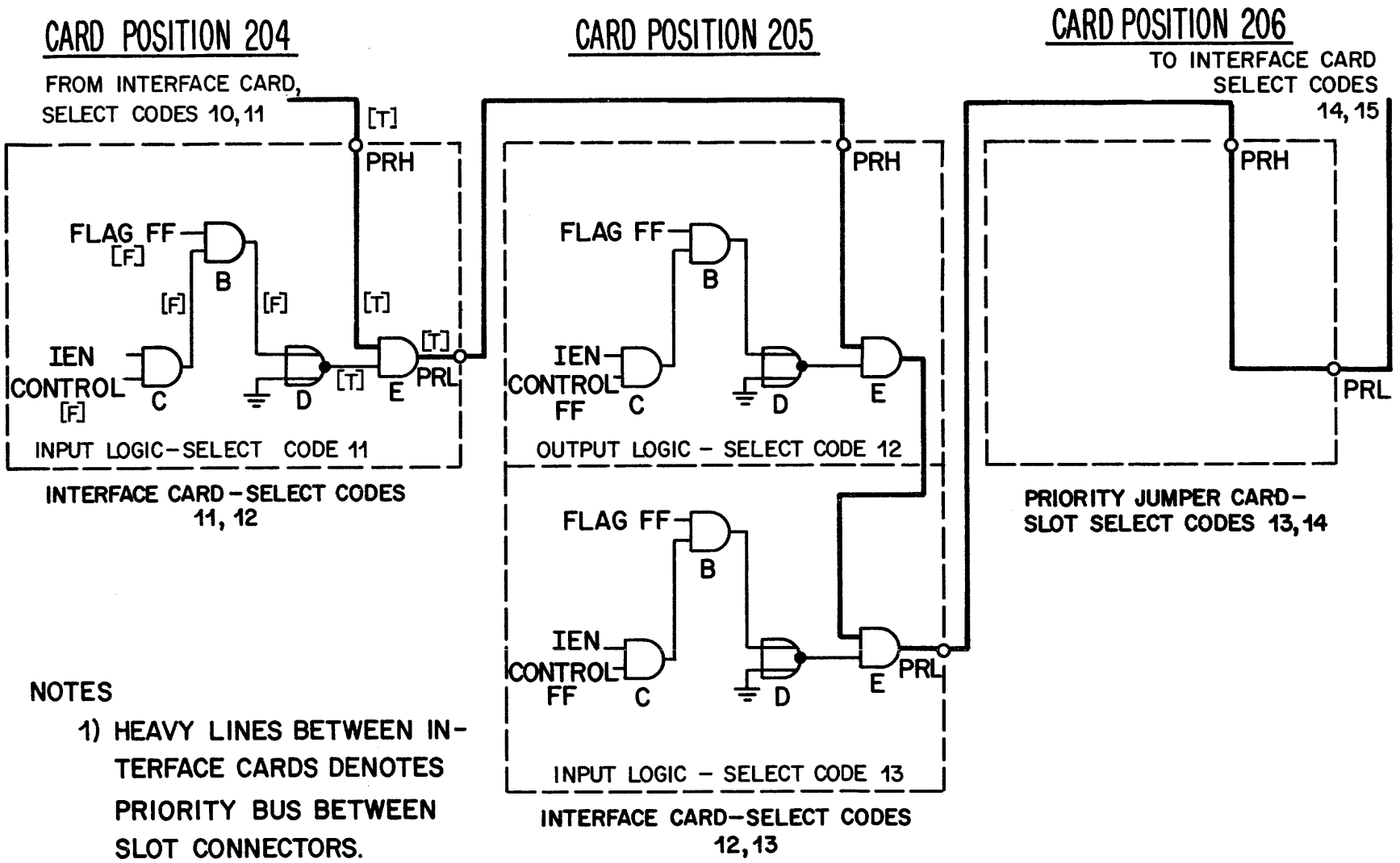
(5) During Interrupt Phase 4, the computer decrements the P-Register by one to ensure that the proper location in the main program will be returned to after the interrupt is processed. (The P-Register was incremented by one at time T7 of the last machine phase of the main program by the STP 0-15) signal. Also, the computer places the Service Request Address (which is always equal to the Select Code of the interrupt device) from the I/O Address card into the M-Register at time T7. This causes the next instruction to be read from the memory location having the same number as the Service Request Address (Select Code) during the Fetch (Phase 1). This location in memory is referred to as the "interrupt location" and is reserved for that particular device. Example: A device specified by a Select Code of 1Ø will interrupt to (i. e., cause execution of the contents of) memory location 00010. At time T3 of Phase 4, the interrupt system is inhibited by the false Enable Service Request signal until the Fetch Phase following the execution of the instruction at the interrupt location. This prevents interrupts from occurring until at least one instruction has been executed (except in the case of JMP, I and JSB, I instructions).

(6) At time T1 of Fetch Phase 1 the IAK (Interrupt Acknowledge) signal from the I/O Control card and the set-side output of the IRQ FF resets the Flag Buffer FF through AND gate J. Since the set-side output of the Flag Buffer FF is applied to AND gate G, resetting the FF prevents the setting of the IRQ FF

which would cause another interrupt from the same Flag signal when the SIR signal is again applied to gate G. The Flag Buffer FF can also be reset by a programmed CLF (Clear Flag) instruction. At time T2, the ENF signal resets the IRQ FF. The computer fetches the instruction in the interrupt location which will usually be a jump to a subroutine (JSB, I) instruction, although any legal instruction may be placed in the interrupt location. The contents of the P-register plus one are stored in the first location (X) of the subroutine. (Since the previous contents of the first memory location are destroyed when P+1 is stored, the first instruction of the subroutine should always be a no-operation (NOP) instruction or equivalent. The location of the subroutine (X+1) is placed in the P- and M-registers, and the computer resumes normal subroutine operation. Thus, the instruction at location X+1 is the first instruction of the subroutine to be executed. The contents of the working registers that were in use in the main program should be stored when entering the subroutine and restored before exit from the subroutine. The exit from the subroutine is made with a JMP, I to location X. This places the address of the interrupted program instruction in the P- and M-registers and normal program operation resumes.

d. Priority Network

(1) As shown in Figure 6-7, priority is established by a hardware-implemented priority chain. The AND-NOR gates are identified by letters. The true-false logic levels for an interface card which is not requesting an interrupt are illustrated on the first interface card (Select Codes 11, 12) with the Interrupt System enabled (IEN input is true). Also, the PRH (Priority High) signal is true, indicating that a device of higher priority is not requesting an interrupt. In this case, the "chain" is not broken and a true PRL (Priority Low) signal is available to the next interface card (Select Codes 12, 13) as a true PRH signal to that card.



NOTES

1) HEAVY LINES BETWEEN INTERFACE CARDS DENOTES PRIORITY BUS BETWEEN SLOT CONNECTORS.

INTERRUPT PRIORITY

FIG. 6-7

(2) The interface card with Select Codes of 12 and 13 contains both input and output logic. Each type of logic has a separate Select Code and corresponding interrupt priority, with the priority chain connected internally. The output logic of the interface card is always of higher priority than the input logic on cards containing both types of logic. Since this interface card uses both Select Codes assigned to its slot, an addressable interface card cannot be placed in the adjacent slot (Card Position 206). However, the adjacent slot must contain a Priority Jumper card to provide continuity for the priority network. There can be no gaps in the network for it to function properly. This card is shown in Card Position 206.

(3) If the output logic portion of the interface card with Select Codes of 12 and 13 requests an interrupt, all inputs to AND gate B will be true. Inverting NOR gate D will then apply a false input to AND gate E. The output of gate E is then false, breaking the "chain", and preventing any interface card of lower priority from interrupting the computer program. A service subroutine can then be entered to process the interrupt of the output logice.

2. Interrupt Subroutines

a. Priority Effecting Instructions

(1) Four instructions: STC, CLC, STF, and CLF, effect the priority structure of the Input/Output devices; whether a device can request an interrupt or not depends upon whether its interface-card Control FF is set or reset (STC, CLC) or its Flag FF is set or reset (STF, CLF). If a device cannot request an interrupt, all succeeding lower-priority devices assume a priority of one higher in the priority chain, and vice versa.

(2) The four instructions also inhibit all interrupts during the machine phase in which they occur by removing the Enable Service Request signal to the I/O Address card. This prevents interrupts during entry and exit from subroutines. Also, a

combination of two of the four instructions are normally the next-to-last instruction in a service subroutine processing an interrupt (the last being a JMP, I instruction to cause return to the main program or to an address in another service subroutine). If another Input/Output device could interrupt immediately after execution of these instructions (and before the JMP, I instruction), the possibility would exist that the first device may interrupt a second time before the JMP, I instruction is performed. In this event, the first main-program address (or the other service-subroutine address) stored in the beginning of the service subroutine would be destroyed, preventing a return to the main program or to the other service subroutine.

b. Multi-level Interrupts

(1) Figure 6-8 shows a symbolic multi-level interrupt operation in process. Note that two return addresses must now be stored in memory.

(a) X - return to main program.
(b) Y - return to lower priority interrupt subroutine.

3. Review

(1) What is the highest priority select code that may be assigned to an I/O device?

(2) What is select code ØØ used for?

(3) What is select code Ø1 used for?

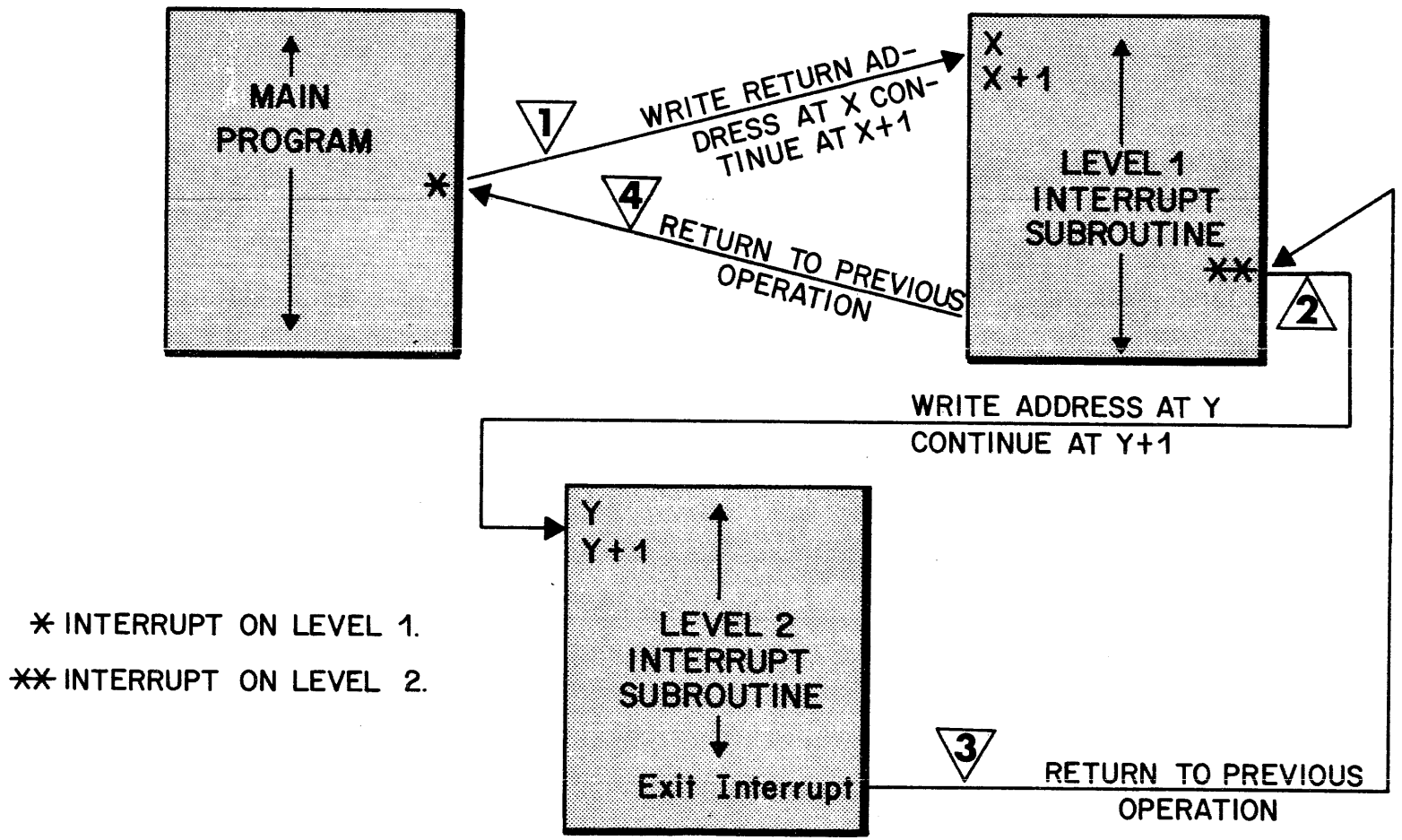
(4) What one select code can cause an interrupt regardless of the Interrupt Enable FF?

(5) When Memory Protect Option is installed, where should it be connected?

(6) How can more than 16 I/O devices be connected to the computer?

(7) How many interface cards may be inserted in the HP 2150B?

(8) Under what three conditions are interrupts always disabled?



MULTI-LEVEL INTERRUPT SYSTEM

FIG. 6—8

(9) What is normally the instruction contained in an interrupt memory location?

(10) How are exits made from an interrupt subroutine?

(11) On interface cards having two select codes, one for input and one for output, which device will have the highest priority?

(12) If both Select Codes on an interface card are being used, what card must be installed in the next sequential slot?

(13) What four instructions effect the priority structure of the interrupt system?

(14) In a 2-level interrupt structure, how many return addresses must be stored in memory?

(15) What two cards control the addressing and I/O operations?

C. I/O CONTROL AND ADDRESSING

1. I/O Control Card (Figure 6-9)

a. Power Control Functions

(1) When power is initially applied by pressing the POWER Switch on the front panel of the computer, the computer is preset to the Fetch Phase (Phase 1). At this time, the POPIO signal is received at pin 63 of the I/O Control Card. This signal is present for 100 milliseconds. (With power on, pressing the computer PRESET switch applies the POPIO signal to the I/O Control card for as long as the switch is pressed.) During the presence of the POPIO signal, the computer clock runs and continually repeats times TØ through T7 while remaining in Phase 1. When the POPIO signal drops, the computer is in Phase 1 and the initial conditions of the interface cards have been established for proper operation. The POPIO signal performs the following functions:

(a) Disables the Interrupt System

(b) Disables the Enable Service Request signal to the I/O Address card.

(c) Sets the Flag Buffer and Flag FFs, and resets the IRQ FF on all interface cards.

(d) Resets the Control FF on all interface cards.

(2) The POPIO signal resets the Interrupt System Enable FF (MC66) through diode CR1, disabling the interrupt system. (The FF consists of two inverting NOR gates which are connected such that the FF can be reset by a true signal to either the reset-side input or the reset-side output of the FF.)

(3) When the Interrupt System Enable FF was reset, the true reset-side output of the FF is applied to the input of inverting NOR gate MC27A through diode CR3. The output of gate MC27A is a false Enable Service Request signal to the I/O Address card. This prevents the I/O Address card from sending an Interrupt signal to the computer which would switch the computer into Interrupt Phase 4.

(4) The POPIO signal forms the buffered POPIO signal (POPIO(B)), through AND gate MC86A, to set the Flag Buffer FF on all interface cards. At time T2, the T2 clock signal to the I/O Control card (through AND gate MC87B) forms the ENF signal. This signal resets the IRQ FF on the interface cards and, with the set Flag Buffer FF output, sets the Flag FF on all interface cards.

(5) The POPIO signal forms the CRS signal through AND gate MC87A, to reset the Control FF on all interface cards and to reset the Interrupt Control FF (MC26) through diode CR2 on the I/O Control card. (The CRS signal can also be programmed by a CLC instruction with a Select Code of ØØ). Resetting the Control FFs prevents an interrupt from occurring when the interrupt system is initially enabled (Interrupt System Enable FF on the I/O Control card gets set). Resetting Interrupt Control FF MC26 ensures a false Enable Service Request signal to the I/O Address card when the POPIO signal drops. This prevents an interrupt from occurring until after time T7, of the

first machine phase after the POPIO signal drops, to permit the execution of at least one program instruction. (The reset-side output of the Interrupt Control FF enables AND gate MC35B to form the IAK signal at time T1 of Phase 1; the IAK signal has no effect on the interface cards during the presence of the POPIO signal.)

(6) At each T5 clock time, the T5 signal is received by the I/O Control card from the computer. This signal is applied to all interface-card slot connectors through AND gate MC57B. The SIR signal enables setting of the IRQ (Interrupt Request) FF on the interface cards to provide Flag and IRQ signals to the I/O Address card during an interrupt request. This signal is also applied to the set input of the PH4/5SYNC2 flip-flop (MC56) on the I/O Control card causing the flip-flop to apply a true output signal to pin 6 of "AND" gate MC47B. (PH4/5SYNC2 flip-flop will be discussed in detail later).

b. I/O Instruction Logic

(1) Whenever any of four I/O instructions are programmed (STC, CLC STF, and CLF), signals are received by the I/O Control card and applied to one of the MC77A through MC77D isolator gates. The applicable gate output is then a true input to AND gate MC37C. The MC37C gate output is then a true input to AND gate MC36B. The MC37C gate output becomes true on receipt of clock signal TS (pin 27) and the IOGE signal at time T3 plus 80 nanoseconds from AND gate MC57A.

(2) The IOGE signal from the computer (via the Power Fail Interrupt board) is sent to the I/O Control card at time T3 of each machine phase that an I/O Group instruction is performed, and is applied to one input of AND gate MC57A. The other input to gate MC57A is the IOGE signal which has been delayed by about 80 nanoseconds to eliminate any noise which may have been generated during its formation. (The delay is caused by inverting NOR gates MC55A and MC55B, resistor R3, and

capacitor C3.) At the end of the delay, gate MC57A provides a true output to AND gate MC37C and a buffered IOGE signal to all interface card slots. The IOGE signal is an enabling signal for the I/O Group instruction and the Select Code transferred to the selected interface card.

(3) The true output of gate MC37C is applied to AND gate MC36B. The other input to gate MC36B is true due to the inversion of the false PH 5 signal by inverting NOR gate MC27B. The true output of AND gate MC36B resets the Interrupt Control FF. The true reset-side output of the Interrupt Control FF is applied to inverting NOR gate MC27A, removing the Enable Service Request signal to the I/O Address card. Interrupt signals will not now be enabled to the computer for the remainder of the current machine phase.

(4) At time T7 of the current machine phase, the STM signal sets Interrupt Timing FF MC16. At time TØ, TS, of the next machine phase true TØ and TS signals are applied to AND gate MC36A. The true output of gate MC36A resets the Interrupt Timing FF. The set side output of this FF is applied to the Interrupt Control FF which is set at time TØ, TS, by the trailing (negative-going) edge of the pulse output of the Interrupt Timing FF. The false reset-side output of the Interrupt Control FF is inverted by inverting NOR gate NC27A, providing a true Enable Service Request input to the I/O Address card, and enabling Interrupt signals to the computer.

(5) The Control FF on all interface cards can be reset by the CLC instruction with a Select Code of ØØ. The CLC signal enters the I/O Control card at pin 75 and is applied to AND gate MC76B. The other input to gate MC76B is from the output of AND gate MC67C. This gate output is true when Select Code ØØ is received at pins 36 and 38, and the output of the IOGE AND gate MC57A is true. The true output of AND gate MC76B then applies a CRS signal to all interface card slots via pin 65. The CRS signal resets the Control FF on the interface cards to prevent an interrupt request from any Input/Output device.

(6) Through the use of the SFS and SFC program instructions, the next instruction in the computer program can be skipped depending on the set or reset condition of the Interrupt System Enable FF. When the Interrupt System Enable FF is set and an SFS instruction is programmed with a Select Code of ØØ, all inputs to AND gate MC97A are true. (The output of AND gate MC67C is true since the SFS instruction is an IOG instruction and provides the IOGE signal, and the SCM(0) and SCL(0) signals represent the Select Code used.) Gate MC97A causes AND gate MC17A to issue a true SKF signal to the computer. The SKF signal cuases the program to skip the next instruction since the Interrupt System Enable FF was set.

(7) Similarly, when the Interrupt System Enable FF is reset, and an SFC instruction is programmed with a Select Code of ØØ, all inputs to AND gate MC97B are true. Gate MC97B causes AND gate MC17A to issue a true SKF signal to the computer. The SKF signal again causes the program to skip the next instruction since in this case, the Interrupt System Enable FF was reset.

c. Register Selection

(1) Select Code Ø1 must be used to enter the computer Switch Register setting into the A or B Register when using Input/Output instructions LIA/B and MIA/B. Select Code Ø1 must also be used with Input/Output instructions STO, CLO, SOC, and SOS to perform operations using the 1-bit Overflow Register. Select Code Ø1 causes the SCM(0) and SCL(1) signals to be applied to the I/O Control card AND gate MC47C from the I/O Address card. The third input to gate MC47C is the IOGE signal which became true at time T3. The true output of gate MC47C causes AND gate MC76A to output the IOS signal. The IOS signal is sent to the computer to enable the applicable Switch Register or Overflow Register operations.

d. Phase Operation

(1) During Phase 4 (Interrupt Phase), the PH4 signal and the T3 clock signal are received by the I/O Control card as shown in Figure 6-10. The T3 signal, after passing through "and" gate MC35A is applied to "and" gates MC37A and MC36C as the T3(B) (buffered time-T3) signal. It is also sent out of the I/O Control card at pin 81 to all I/O interface-card slot connectors. The PH4 input signal is also applied to "and" gates MC37A and MC36C. When the PH4 signal and the T3(B) signal are simultaneously applied to "and" gate MC37A as input signals, (during time T3 of a Phase 4), a true output signal from gate MC37A is applied to the Interrupt Control flip-flop (MC26) as a reset pulse. The resulting true reset-side output signal of the flip-flop is inverted by inverting "or" gate MC27A and sent to the I/O Address card as a false ESR (Enable Service Request) signal. This action inhibits the INT (Interrupt) signal to the Computer until after the program counter steps (time T7 of Fetch Phase 1). The PH4 and T3(B) signals are also simultaneously applied to "and" gate MC36C at time T3 of Phase 4. This causes "and" gate MC36C to apply a true output signal to the direct-set input of the PH4/5 SYNC 1 flip-flop (MC46) which then applies its set-side true output signal to "and" gate MC47B. This signal, when true, remains in a true state as an input to "and" gate MC47B until the PH4/5·SYNC 1 flip-flop is directly reset by the POPIO pulse or is clocked by the IAK (Interrupt Acknowledge) signal at time T1 of Fetch Phase 1.

(2) At time T2 of Phase 1 (Fetch Phase), directly following the Interrupt Phase, the PH1 signal and clock signal T1 are applied as inputs to "and" gate MC37B. The true output of gate MC37B supplies one input of "and" gate MC35B. The other input to gate MC35B is the true reset-side output of the Interrupt Control flip-flop. When both of these inputs are true, gate MC35B sends its true output signal out of the I/O Control card to all interface-card slots as the IAK (Interrupt Acknowledge) signal.

This signal causes the Flag Buffer flip-flop on the Interface card which initiated the interrupt to be reset. The IAK signal is also applied to the PH4/5 SYNC 1 flip-flop (MC46), on the I/O Control card, as a clock pulse.

(3) The Enable Service Request signal is inhibited during the time between an Interrupt Phase 4 and time T7 of the Fetch Phase of the instruction in the computer-memory interrupt location unless further disabled by a JMP, I or JSB, I instruction in that interrupt location. This ensures full execution of at least one instruction before interrupts are again enabled. At time T7 of the Fetch phase, the STM signal sets the Interrupt Timing flip-flop. The flip-flop is reset at time T0, TS of the next machine phase by the true output of "and" gate MC36A. The trailing-edge output of the Interrupt Timing flip-flop sets the Interrupt Control flip-flop at time T0, TS. The false reset-side output of the Interrupt Control flip-flop is inverted by gate MC27A, providing a true Enable Service Request signal to the I/O Address card, and again allowing Interrupt signals to be sent to the Computer.

(4) Phase 5 is a one-cycle suspension of normal computer operation which is caused by the DMA (Direct Memory Access) and the DMI (Direct Memory Increment) Computer options. Since it is not one of the normal machine cycles, Phase 5 must be requested by an option when the option is ready to operate. When Phase 5 is requested (always at time T6 of the machine cycle immediately preceding a Phase 5), the HIS (Hold Interrupt System) signal is received by the I/O Control card. This signal is then applied to inverting "or" gate MC27A where it is inverted and sent to the I/O Address card as a false ESR signal. When Phase 5 begins actual operation (T0 of the Phase 5 machine cycle), the PH5 signal is received by the I/O Control card and is applied to inverting "or" gate MC27B and to "and" MC45B. The resulting false output of inverting "or" gate MC27B is sent to the

I/O Address card as the false Enable I/O Address (PH5) signal. The output of "and" gate MC45B during Phase 5 is dependent upon the state of the output signal from the set-side of the PH 4/5 SYNC 1 flip-flop (MC46). If Phase 5 has been immediately preceded by a Phase 4, pin 3 of "and" gate MC47B will receive a true input signal during all of Phase 5 from the PH4/5 SYNC 1 flip-flop. At time T5 of Phase 5, the SIR (Set Interrupt Request) signal from "and" gate MC57B is applied as a true signal to the set input of the PH4/5 SYNC 2 flip-flop (MC56). The resulting true output signal from the set-side of the flip-flop is then applied to pin 6 of "and" gate MC47B. This enables "and" gate MC47B which then applies a true output signal to pin 8 of "and" gate MC45B. With the PH5 signal at pin 6 and the true output signal from "and" gate MC47B at pin 8, "and" gate MC45B is now enabled (time T5 of Phase 5). When this occurs, "and" gate MC45B applies a true output signal to the PH4 line which distributes the signal, via Computer backplane wiring, to all Computer circuits normally receiving the PH4 signal.

(5) If a Phase 5 was not immediately preceded by a Phase 4, the input signal to pin 8 of "and" gate MC45B will be false throughout the entire Phase 5 machine cycle. In this case, "and" gate MC45B will not apply a true signal to the Phase 4 backplane wiring during a Phase 5.

e. Interrupt System Control

(1) The set or reset condition of the Interrupt System Enable flip-flop (MC66) determines whether the interrupt system is "on" or "off", under program control. If the flip-flop is set, the IEN signals to the interface cards will enable interrupt requests; if the flip-flop is reset, the IEN signals are removed and interrupt requests will not be enabled. Initially, the interrupt system is disabled by the POPIO signal.

(2) If the interrupt system is to function, the Interrupt System Enable flip-flop must be set by a STF instruction with a Select Code of 00. When this is programmed, the SCM(0) and SLC(0)

signals are received by the I/O Control card (from the I/O Address card) and applied to "and" gate MC67C. The remaining input to gate MC67C is the true IOGE signal. The true output of gate MC67C is "anded" with the STF signal at "and" gate MC67A at time T3. The true output of gate MC67A sets the Interrupt System Enable flip-flop.

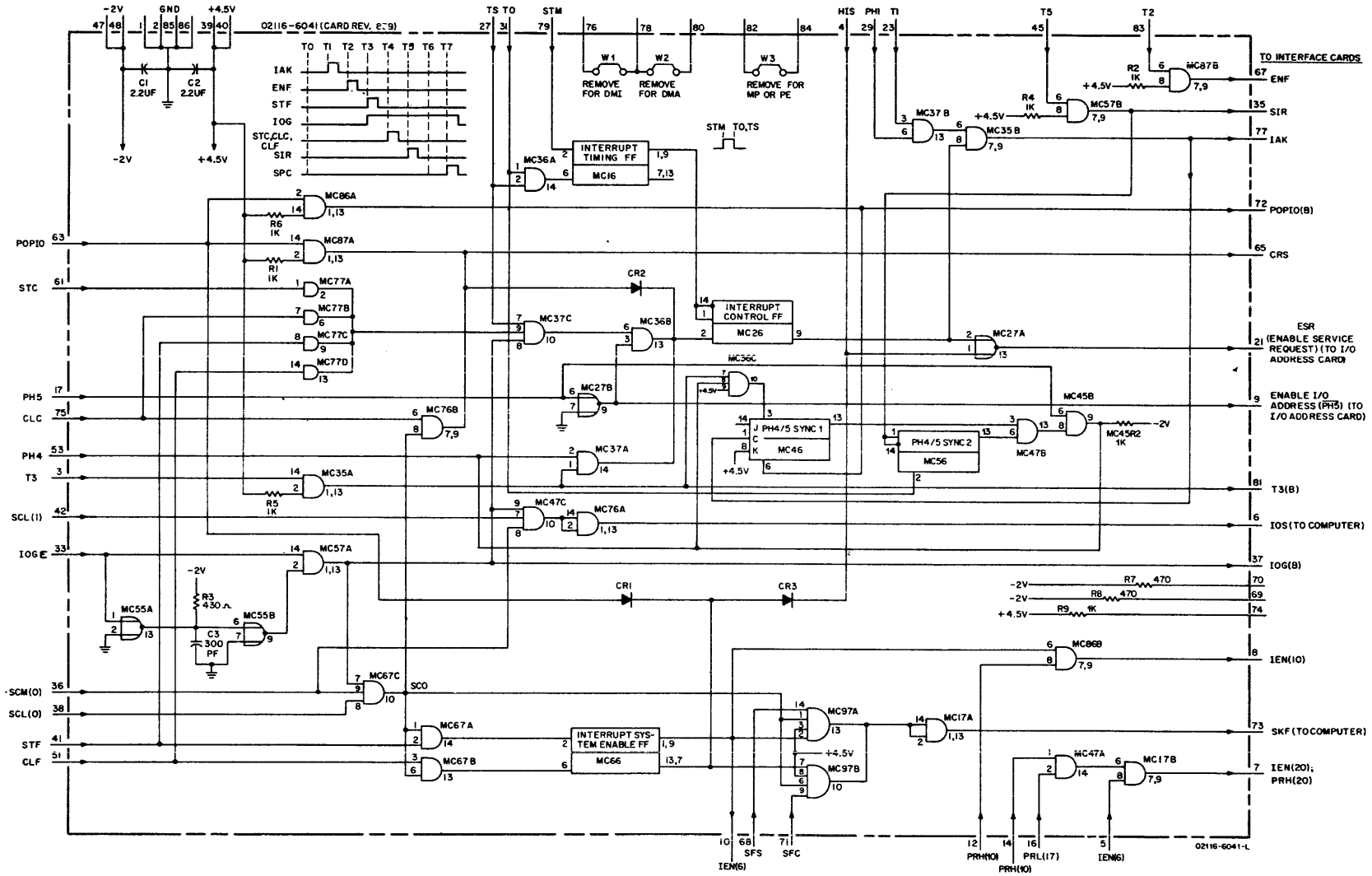
(3) The ESR (Enable Service Request) signal is produced when there is a false input to pin 1 and pin 2 of inverting "or" gate MC27A on the I/O Control card. The input to pin 1 is supplied by the HIS (Hold Interrupt System) signal (pin 4 of I/O Control card), the reset output signal from pin 13 of the Interrupt System Enable flip-flop (MC66), or the POPIO (Power On Pulse to I/O) signal. The input to pin 2 of gate MC27A is the reset output signal from the Interrupt Control flip-flop (MC26). When present, the ESR signal is applied to pin 21 of the I/O Address card from pin 21 of the I/O Control card.

(4) The true set-side output signal of the Interrupt System Enable flip-flop (MC66) is applied to "and" gate MC86B and also out pin 10 of the I/O Control card as the IEN(6) (Interrupt Enable, Select Code 06) signal. Pin 10 sends this signal, via computer backplane wiring, to the interface-card slot connectors which have Select Codes 05 and 06 and also back into the I/O Control card at pin 5 where it is applied to "and" gate MC17B. The Power Fail Interrupt card uses Select Code 04 and has the highest priority in the interrupt system. The Power Fail card generates the PRL(4) signal (Priority Low, Select Code 04) signal which is applied to the two interface-card slots using Select Code 05 as the PRH(5) signal. These two interface-card slot are reserved for the Memory Protect and Parity Error options. When neither of these two options are in the process of interrupting normal Computer operation, a true PRL(5) signal is sent to the DMI interface-card slot (Select Code 06) as the PRH(6) signal. If neither the Parity Error or the Memory Protect option is installed in the Computer, the PRH(6) signal

is received from the Power Fail card (as the PRL(4) signal) through jumper W3 on the I/O Control card, bypassing the two interface card slots which use Select Code 05, and is applied to the DMI interface-card slot (Select Code 06). If the DMI option is not installed in the Computer, the PRH(6) signal is sent through jumper W1 on the I/O Control card, bypassing the DMI interface-card slot, and is applied to the two interface-card slots reserved for the DMA option (Select Codes 06 and 07). Since the DMA option occupies two interface-card slots, there is no PRL(6)/PRH(7) signal sent from one of the DMA interface-card slots to the other. When DMA is installed in the Computer and not operating, the PRL(7) signal is generated by the DMA interface-card slot having Select Code 07. This signal is applied to "and" gates MC86B and MC47A and to the interface-card slot having Select Code 10 as the PRH(10) signal. If the DMA option is not installed in the Computer, the PRH(6) signal (from Power Fail, Memory Protect or Parity Error) is sent through jumper W2 on the I/O Control card, bypassing the DMA option interface-card slots, and effectively becomes the PRH(10) signal. This signal is then sent out of the I/O Control card and is applied to the same places as is the actual PRH(10) signal from the DMA option. If none of the Computer options described above (Memory Protect, Parity Error, DMI or DMA) are installed in the Computer, the PRL(4)/PRH(5) signal from the Power Fail card is sent through jumpers W3, W1, and W2 on the I/O Control card and then applied to the PRH(10) circuit as the PRH(10) signal.

(5) When "and" gate MC86B receives two true input signals, IEN(6) from the Interrupt System Enable flip-flop and PRH(10) from DMA, a true output signal, IEN(10), is sent to the interface card slots having Select Codes 10 through 17. The PRH(10) signal is also applied to the interface-card slot that has Select Code 10. With both the IEN(10) and the PRH(10) signals true, the I/O device using the interface-card slot having Select Code 10 may interrupt normal Computer operation whenever requested

by the Computer program or when the I/O device itself requests an interrupt. If one of the interface cards that has a higher priority (Power Fail, Memory Protect, Parity Error, DMI, or DMA) requests an interrupt, all succeeding interface-card slots of a lower priority will be disabled and the PRH(10) signal which is sent to "and" gate MC86B and to the interface-card slot having Select Code 10 will be false. When this happens, "and" gate MC86B in turn applies a false IEN(10) output signal to the interface-card slots having Select Codes 10 through 17. This action disables all eight I/O interrupt card slots (Select Codes 10 through 17). In this condition it is impossible for I/O devices using Select Codes 10 through 17 to interrupt the Computer program until both the IEN(6) and the PRH(10) signals to "and" gate MC86B are true once again. When this block of eight interface-card slots (Select Codes 10 through 17) are enabled and the interface-card slots having Select Codes 04 through 17 are not requesting an interrupt, a true PRL(17) signal is sent from the interface-card slot having Select Code 17 to pin 16 of the I/O Control card. After entering pin 16 of the I/O Control card, this signal is applied to pin 2 of "and" gate MC47A as a true input signal. Now that "and" gate MC47A is receiving the true PRH(10) signal at pin 1 and the true PRL(17) signal at pin 2, it is enabled and it applies a true output signal to pin 6 of "and" gate MC17B. At this time, "and" gate MC17B is also receiving the true IEN(6) signal at pin 8, which causes "and" gate MC17B to apply a true output signal out pin 7 of the I/O Control card as the IEN(20) signal. From pin 7 of the I/O Control card the IEN(20) signal is applied to the interface-card slot having Select Code 20 as both the IEN(20) signal and the PRH(20) signal. The IEN(20) signal is also applied to the interface-card slots having Select Codes 21 through 27. Each of these seven interface-card slots receive their respective PRH signals, PRH(21) through PRH(27), from the preceding interface-card slot having the Select Code of the next highest priority. Interrupt operation of these eight interface-card slots (Select Codes 20 through 21) is



NOTES:

1. ALL LOGIC IS POSITIVE-TRUE.
2. THE TIMING CHART DOES NOT RELATE SIGNALS TO THE MACHINE PHASE IN WHICH THEY OCCUR.

I/O CONTROL CARD

FIG 6-9

now the same as the preceding block of eight interface-card slots (Select Code 10 through 17). The determining factor for any interface-card slot requesting an interrupt is the PRH signal. If an I/O device of a higher priority (lower Select Code) is already interrupting or has requested an interrupt, this signal is false causing interface-card slots having lower priority Select Codes to be disabled. This same interrupt enabling process is extended to include the additional Select Codes whenever an I/O Extender module is used.

(6) To disable the interrupt system, the Interrupt System Enable flip-flop must be reset by a CLF instruction with a Select Code of 00. When this is programmed, the SCM(0) and SCL(0) signals are applied to "and" gate MC67C. Since the CLF instruction is an IOG instruction, the output of "and" gate MC57A (which is applied to gate MC67C) will be true about 80 nanoseconds after receipt of the IOG signal. All inputs to gate MC67C are then true. The true output of gate MC67C is applied to "and" gate MC67B. The true CLF signal is also applied to gate MC67B. The true output of this "and" gate resets the Interrupt System Enable flip-flop. The set-side output of the flip-flop becomes false, removing the IEN signal to all interface-card slot connectors. This immediately prevents any interface card (device) from requesting an interrupt.

2. I/O Address Card (Figure 6-10)

a. Decoding Function

(1) When an I/O instruction is programmed, the 6-bit Select Code portion (bits 0 through 5) of the instruction is received by the I/O Address card. The three least significant bits (Ø-2) and their NOT conditions are applied to eight AND gates, MC55A/B, MC65A/B, MC75A/B, and MC85A/B. The three most significant bits (3-5) and their NOT conditions are also applied to eight AND gates, MC95A/B, MC105A/B, MC115A/B, and

MC125A/B. All AND gates have a common enabling input from AND gate MC16A. The Enable I/O Address signal to gate MC16A is received from the I/O Control card and is always true except during Direct Memory Access (DMA) operations (Phase 5).

(2) The true output of eacn AND gate represents an octal digit and only one AND gate in each group of eight will be true for any given Select Code. The true outputs of the two AND gates form the SCM (Select Code Most significant digit) and the SCL (Select Code Least significant digit) signals. Each of the outputs of this first group of 16 AND gates are buffered out of the I/O Address card to the interface cards by a second group of 16 gates. These gates provide the drive necessary to apply signals of proper amplitude to the interface cards. The 1K resistor between each of the gates and the -2 volt supply minimizes the affect of any transient noise which may exist on the lines to the interface cards and reduces the fall time of the gate output voltage.

(3) Example: With a Select Code of 11 (001 001 binary) applied to the I/O Address card, only bit Ø and bit 3 are true input signals; each Select-Code bit input is applied to four AND gates as follows:

(a) The bit Ø input is applied to AND gates MC75B, MC55B, MC65B, and MC85B. The output of AND gate MC75B is true since the bit Ø, bit 1, and bit 2 inputs and the output of gate MC16A are true inputs. The outputs of the other three AND gates are false since the bit 1 and bit 2 inputs are false. The output of gate MC75B is applied to AND gate MC76B and then to pin 67 as a true SCL(1) signal to the interface cards.

(b) The bit 3 inputs is applied to AND gates MC105B, MC95B, MC115B, and MC125B. The output of AND gate MC125B is true since the bit 3, bit 4, and bit 5 inputs and the output of gate MC16A are true inputs. The outputs of the

other three AND gates are false since the bit 4 and bit 5 inputs are false. The output of gate MC125B is applied to AND gate MC126B and then to pin 77 as a true SCM(1) signal to the interface cards.

(4) The SCM and SCL signal combination determines the slot connector containing the interface card to which the instruction portion of the I/O instruction word is directed. Each slot connector, and therefore each interface card, contains two octal Select Codes. Note that the SCM(1) signal is applied to the most-significant-digit input pins on interface-card slot connectors with Select Codes of 1Ø through 17. The SCM(2) signal is applied to basic computer interface-card slot connectors with Select Codes of 2Ø through 27. Similarly, the SCM(3) through SCM(7) signals are applied to Module Extender options containing interface-card slot connectors with Select Codes of 3Ø through 47, 5Ø through 67, and 7Ø through 77. The SCM(0) signal is applied to the I/O Control card (Select Codes ØØ and Ø1) slot connector in the Input/Output section of the computer. It is also applied to the DMA 1 and DMA 2 option (Select Codes 02, 03, 06, and 07) and the Power Failure Interrupt option (Select Code 04) slot connectors in the logic section of the computer. The SCL(0) through SCL(7) signals are applied to the least-significant-digit input pins on the slot connectors in the computer and in the Module Extender options. The slot connectors in the Module Extender options are wired in the same manner as those in the basic computer.

(5) The SCM and SCL signals are applied to the same-numbered pins on all interface-card slot connectors as follows: (Figure 6-11)

(a) Pin 14: Lower Select Code, Most Significant digit. (LSCM).

(b) Pin 16: Lower Select Code, Least Signficant digit. (LSCL).

(c) Pin 37: Higher Select Code, Most Signficant digit. (HSCM).

(d) Pin 34: Higher Select Code, Least Significant digit. (HSCL).

b. Encoding Function

(1) When an Input/Output requests an interrupt of the computer program, the IRQ FF on the interface card for the device is set. The set-side output of the IRQ FF applies a true FLG (Flag) signal to the I/O Address card; the reset-side output of the FF is inverted by an inverting NOR gate to apply a true IRQ signal to the I/O Address card. These two signals are used to form the Interrupt signal and the Service Request Address to be transferred to the computer.

c. Interrupt

(1) An Interrupt signal is sent to the computer at time T5 of the current machine phase when a Flag signal is received from an interface card, and if the Enable Service Request signal is received from the I/O Control card. The Interrupt signal causes the computer to enter Interrupt Phase 4 at the end of the current machine phase.

(2) Four Flag signals (Ø through 3) can be received from the interface cards. These signals are described in steps "a" through "d". Receipt of a Flag signal applies a true input to AND gate MC16B through one of the CR33 through CR36 diodes. If the enable Service Request signal is true, the gate MC16B output is applied to the computer as a true Interrupt signal.

(a) Flag (0): This input is true when an interface card with a Select Code of Ø4 to 17 is requesting an interrupt.

(b) Flag (1): This input is true when an interface card with a Select Code of 2Ø to 37 is requesting an interrupt.

(c) Flag (2): This input is true when an interface card with a Select Code of 4Ø to 57 is requesting an interrupt.

(d) Flag (3): This input is true when an interface card with a Select Code of 6Ø to 77 is requesting an interrupt.

d. Service Request Address

(1) The 6-bit Service Request Address is the Select Code of the interface card requesting an interrupt in binary form. It is sent to the M-register of the computer via the "T" bus and specifies the interrupt location for that device in memory. (The interrupt location contains the instruction to be executed when the particular interrupt occurs.) While the Interrupt signal is sent to the computer at time T5 of the current machine phase, the Service Request Address is not enabled to the computer until time T7 of Interrupt Phase 4.

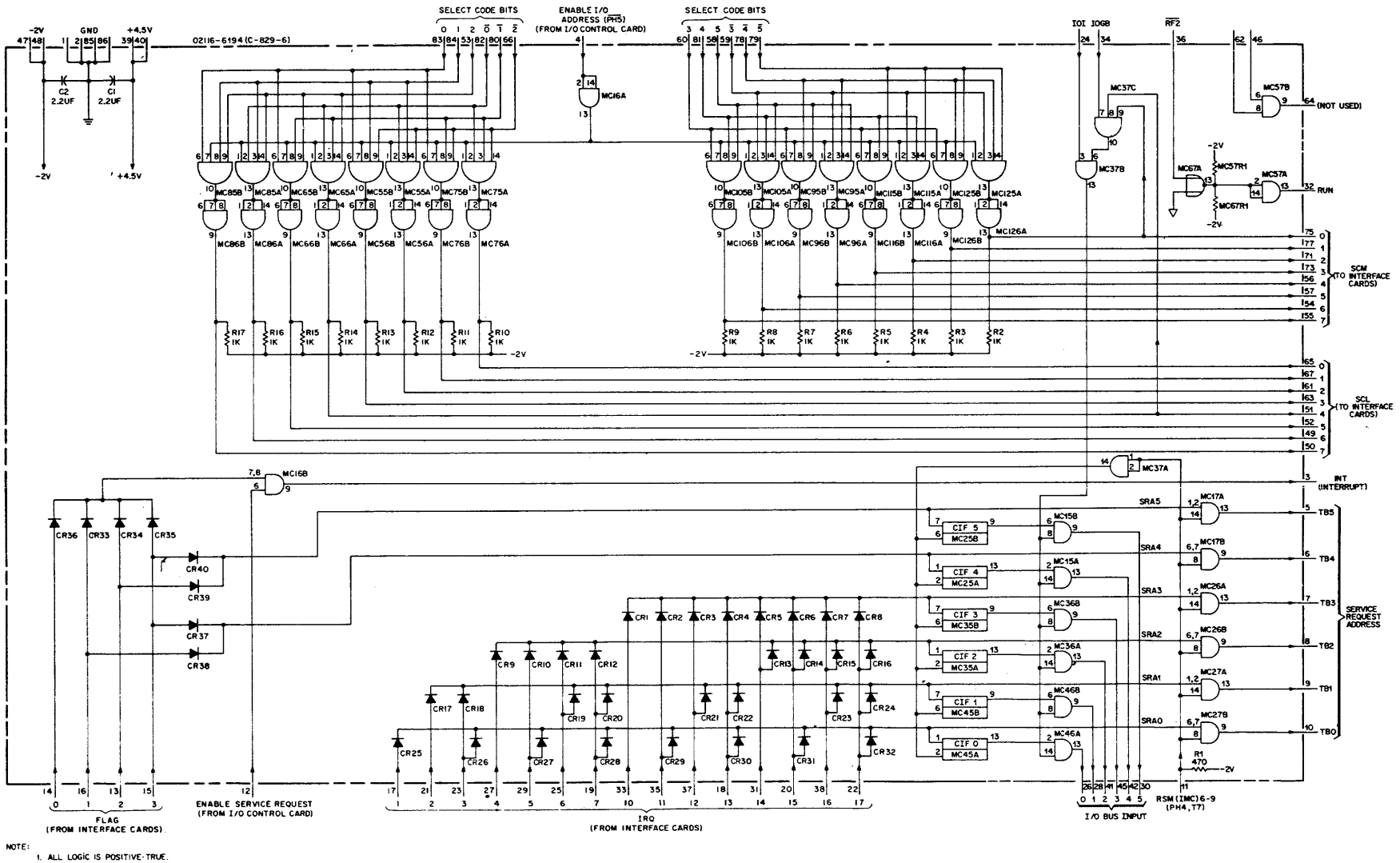
(2) The Service Request Address is formed by encoding the combination of Flag and IRQ signals from the interface card requesting an interrupt. The Flag (1) through Flag (3) signals determine the two most significant bits (bits 4 and 5) of the address and are applied to diodes CR37 through CR 40 and then to AND gates MC17A and MC17B. The Flag (0) signal has no affect on the Service Request Address since it is received only from interface cards with Select Codes of 04 (000 100 binary) to 17 (001 111 binary), where bits 4 and 5 are always zero (false). The IRQ signals determine the four least significant bits (bits Ø through 3) of the address and are applied to diodes CR1 through CR32 and then to AND gates MC26A, MC26B, MC27A, and MC27B. The remaining input to the Service Request Address AND gates is applied at time T7 of Interrupt Phase 4 by the RSM(IMC) 6-9 signal from the computer.

e. Run Signal

(1) The $\overline{RF2}$ (Run flip-flop 2, "not") signal from the Computer timing generator is input at pin 36 of the I/O Address card where it is applied to inverting "or" gate MC67A. When the Computer is running and is not in a HALT condition the $\overline{RF2}$ signal is always false. When the Computer is in a HALT condition the $\overline{RF2}$ signal is true. Inverting "or" gate MC67A inverts the $\overline{RF2}$ signal and applies it to "and" gate MC57A as an input. Since the two input pins (pin 2 and 14) of "and" gate MC57A are tied together, it produces a true output signal whenever it receives a true input from inverting "or" gate MC67A (whenever the Computer is in the RUN mode). This signal is then sent out of the I/O Address card at pin 32 as the RUN signal and is applied to pin 50 of all I/O interface-card slots (Select Codes 10 through 27). If an extender module is used with the Computer, the RUN signal is also applied to pin 50 of all interface-card slots in the extender.

f. Central Interrupt Register

(1) The Central Interrupt Register (Flip-Flops CIF0 through CIF5 and "and" gates MC15A, MC15B, MC36A, MC36B, MC46A, and MC46B) stores the Service Request Address. This information, or address, is always available during a Phase 4 I/O operation and is strobed into the Central Interrupt Flip-Flops, CIF0 through CIF5, at T7 of Phase 4. To utilize this address, the computer operator must execute an I/O load or merge instruction containing a Select Code of 04. These instructions would be LIA/B and MIA/B used with Select Code 04. Select Code 04, the Power Fail Interrupt Select Code, is not required for any Power Fail Interrupt function during a load instruction as has been used here. On the I/O Address card, the Phase 4, T7 signal enables gate MC37A which then applies its true output to all flip-flops of the Register (CIF0 through CIF5). This action causes the address to be written into the register flip-flops. In

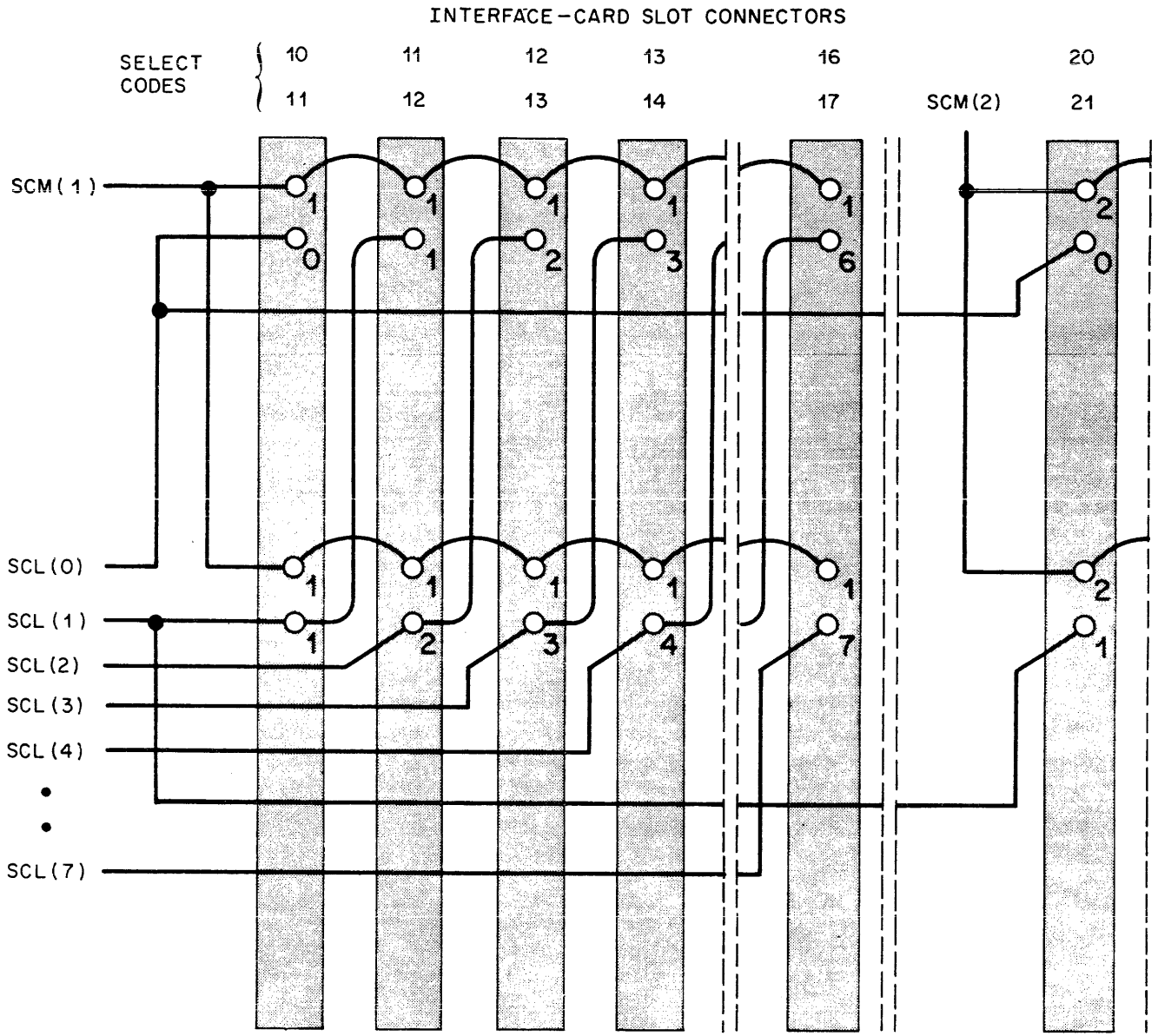


NOTE:

1. ALL LOGIC IS POSITIVE-TRUE.

I/O ADDRESS CARD

FIG 6-10



SCM & SCL SIGNAL PATHS

FIG. 6-11

order to then apply this address to the computer central processor, the IOGE signal and both Select Code signals (representing Select Code 04) must be applied to "and" gate MC37C. The output of gate MC37C is then applied to "and" gate MC37B simultaneously with the IOI signal. When all of these signals are presented, (having been generated by a computer program instruction of the type mentioned above) the output of gate MC37B is applied to all of the Central Interrupt Register output "and" gates (MC15A, MC15B, MC36A, MC36B, MC46A, and MC46B). This action enables all output gates of the register and the address that it contains is applied to the IOBI of the computer central processor.

3. I/O System Timing (Figure 6-12)

   a. Timing Relationships

      (1) The I/O system timing chart is shown on Figure 6-12. This diagram is self-explanatory, but it may be used for reviewing this section. The student should be able to logically relate these timing signals to the overall system operation.

4. Review

   a. Questions

      (1) How long is the POPIO signal true when power is initially applied to the Computer?

      (2) What function does the POPIO signal perform?

      (3) What signal enables setting the IRQ FF at every T5 time period?

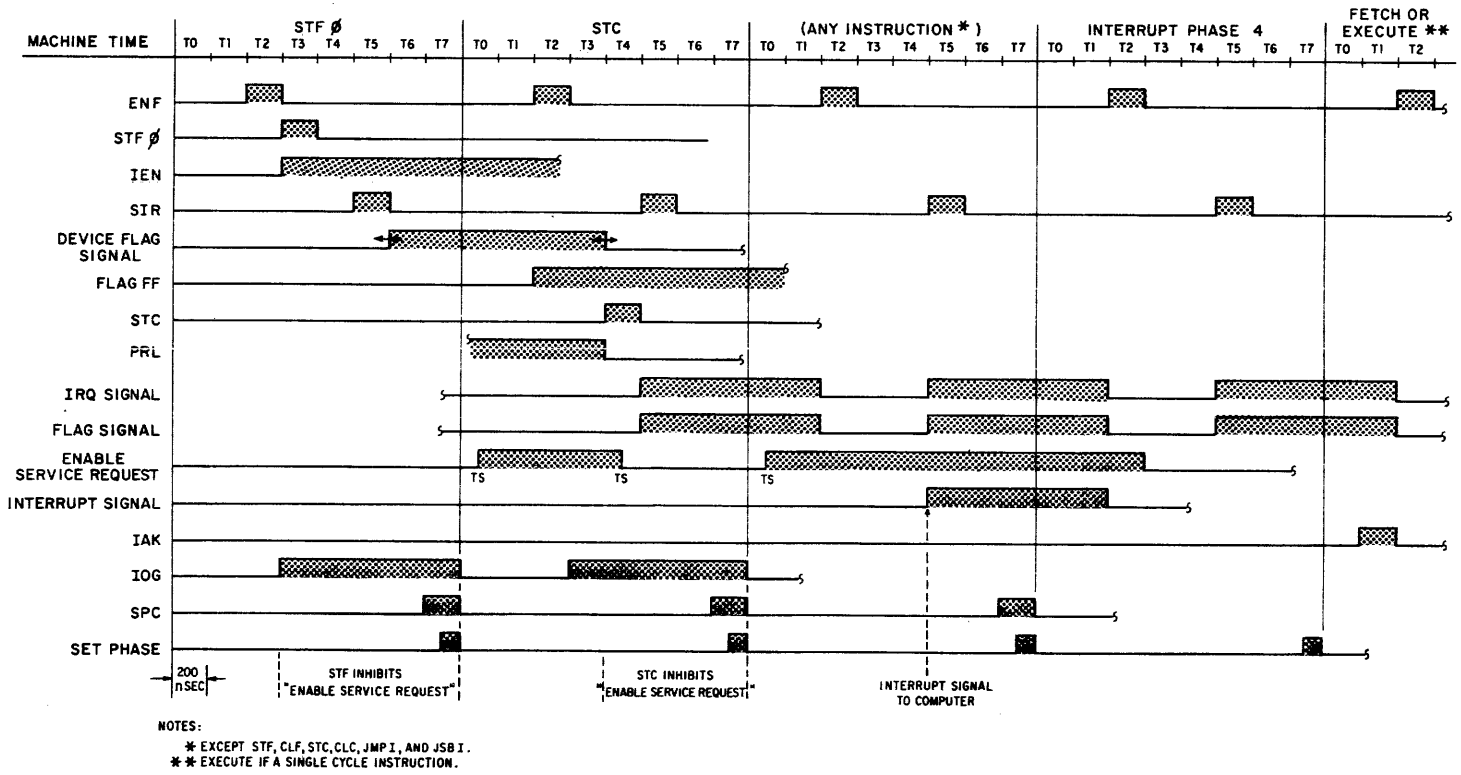
      (4) What instruction and Select Code is required to reset the Control FF?

      (5) What Select Code must be used to enter data from the Switch Register?

      (6) What I/O instructions effect the Overflow Register only?

      (7) When using SFS or SFC instructions, what determines if the next instruction will be skipped? When will it be skipped?

      (8) What determines if the interrupt system is on or off under program control? When is it on? When is it off?



NOTES:

* EXCEPT STF, CLF, STC, CLC, JMP I, AND JSB I.
** EXECUTE IF A SINGLE CYCLE INSTRUCTION.

INTERRUPT TIMING DIAGRAM

FIG. 6—12

(9) What instruction is used to turn the interrupt system off under program control?

(10) With a Select Code of octal 12, what bit signals to the I/O Address card will be true?

(11) What signals determine which interface card is selected for a given octal Select Code?

(12) How many flag signals to the I/O Address Card are required to select 77_8 I/O devices?

(13) What comprises the 6-bit Service Request Address?

(14) What determines the two MSB's (4, 5) of the Service Request Address?

(15) What determines the four LSB's (0, 1, 2, 3) of the Service Request Address?

test procedures and diagnostics

A. PROGRAMMED 8K LONG DIAGNOSTICS

1. This diagnostic automatically runs five basic tests. Tests 4, 5 and 6 are executed on both upper and lower portions of memory.

NUMBER	TEST	TIMES RUN
1	ASG Test	1000
2	MRG Test	2
3	SRG Test	10,000
4a	Low Memory Address Test	500
5a	Low word bit Checkerboard Ampex Stack	1000
6a	Low word bit Checkerboard Ferroxcube Stack	1000

If a diagnostic test fails the T-Register contains 1020XX, and the diagnostic that failed can be isolated simply by checking the printout on the Teleprinter. The location of the halt instruction in that diagnostic test will be M-1, where M is the address contained in the M-Register. The instruction that failed is then at address M-2.

2. Loading and Executing a Long Diagnostic

   a. Load the Long Diagnostic paper tape into the photoreader.

   b. Set the Switch Register to Ø777ØØ and press the LOAD ADDRESS pushbutton.

   c. Place the LOADER switch in the ENABLE position, and press the RUN pushbutton. The computer will halt with 1Ø2Ø77 in the T-Register, if the program was loaded properly.

   d. Set octal address 15 in the Switch Register and press the LOAD ADDRESS pushbutton.

   e. Enter into the switch register the Octal Select Code for the photoreader and press the LOAD A pushbutton.

f. Enter into the Switch Register the Octal Select Code for the ASR33 Teleprinter. If a buffered teleprinter interface is available, bit 15 should be set. Otherwise, bit 15 remains a zero. Press the LOAD B pushbutton.

g. Press the RUN pushbutton. The computer will halt with address 20 in the P-Register.

h. Set the SWITCH REGISTER to the upper limit of the core memory. For a 4K memory this will be address ØØ7677. On 8K memory the address is Ø17677. Press LOAD A pushbutton.

i. Set the SWITCH REGISTER to Ø77777, and press the RUN pushbutton. The first diagnostic test will be loaded into the computer. The Teleprinter will print out: "Number 1, ASG Test, 1000 Times".

j. From this point on, any halt indicates an error condition.

3. After the basic tests have been completed, the machine will attempt to load and execute the basic I/O test with central interrupts. If the central interrupt capability is not present, the machine will halt with the T-Register equal to 1Ø2Ø3Ø. This is a normal indication. Once this halt occurs, the execution of the long diagnostic is complete.

4. Alter-Skip Group Diagnostic

   a. This program is a reliability test of all legitimate code combinations in the Alter-Skip Group. The codes are tested using both the A and B-Registers, rendering a total of 2048 legitimate combinations. This test should be used as the initial reliability test to be executed. If successful, more advanced reliability and diagnostic programs should be attempted. This test does not use any memory reference instructions during the first execution pass.

5. Memory Reference Group Diagnostic

   a. This program is a reliability test of the 14 Memory Reference instructions. The instructions are tested utilizing both the A and B-Registers and the E-Register when appropriate. This test should be used only after the Alter-Skip Group test has been successfully executed. This test uses Alter-Skip type instructions during the testing of memory reference instruction codes.

6. Shift/Rotate Group Test

   a. This is a test of all legitimate code combinations in the Shift/Rotate Group, and the instructions used to control and sense the overflow logic. The codes are tested utilizing both the A and B-Registers, rendering a total of 612 legitimate and meaningful combinations. This test should be used only after the Alter-Skip group tests and the Memory Reference instruction tests have been successfully executed. This test uses Alter-Skip type and Memory Reference type instructions to execute the SRG combination.

7. Memory Address Test

   a. The Memory Address Test will allow a test to be conducted of the Memory Address register and a specified section of the core. The program is divided into three main sections. The first, is to select the section to be tested by using the switches to set the starting and ending addresses. The second section loads the core and the third section reads back what has been deposited in memory and tested for errors. If an error is detected, the program will halt with the error in the B-Register and the correct data will be in the A-Register.

8. Memory Checkerboard Test

   a. The Memory Checkerboard Program tests the core memory for failures while loading an alternating pattern of all ones or zeroes, and then reading it back and checking for errors. If an error occurs, the computer will halt on the address of the error.

B. THE ABSOLUTE BLOCK LOADER

1. If the diagnostic test program will not load and you do not get orderly halts at 1Ø2Ø77 and 1Ø2ØØØ, it is possible that the Absolute Block Loader is not loaded properly. This section describes the procedures to reload the Absolute Block Loader in 4K or 8K machines. The procedures for loading the ABL in an 8K machine with the photoreader at select code 10 will be given first. This procedure may be modified slightly for 4K machines and for photoreaders at select codes other than 10.

2. Loading the ABL Boot Strap Tape

a. Enter the following instructions in memory using the front panel controls:

ADDRESS (OCTAL)	CODE (OCTAL)	INSTRUCTION
ØØØØ2Ø	1Ø37XX	STC, CLF (reader address)
ØØØØ21	1Ø23XX	SFS
ØØØØ22	Ø24Ø21	JMP(21)
ØØØØ23	1Ø25XX	LIA (reader address)
ØØØØ24	ØØ1727	ALF, ALF
ØØØØ25	1Ø37XX	STC, CLF
ØØØØ26	1Ø23XX	SFS
ØØØØ27	Ø24Ø26	JMP(26)
ØØØØ3Ø	1Ø24XX	MIA (reader address)
ØØØØ31	17ØØØ1	STA(B), I
ØØØØ32	ØØ6ØØ4	INB
ØØØØ33	Ø24Ø2Ø	JMP(20)

XX = Octal address of photoreader in your configuration

b. Now load the ABL Boot Strap Loader Tape in the photoreader and proceed as follows:

(1) Set SWITCH REGISTER to Ø777ØØ, press LOAD B pushbutton.

(2) Set SWITCH REGISTER to ØØØØ2Ø, press LOAD ADDRESS pushbutton.

(3) Set the Loader Protect switch to ENABLE.

(4) Press PRESET and RUN pushbuttons, in that order.

NOTE

The computer will not halt automatically. After the Boot Strap Tape has passed through the photoreader and stopped, press the HALT pushbutton.

(5) The Absolute Block Loader is now in Memory.

(6) If the photoreader is not at Select Code 10, the contents of

three memory locations must be reset manually as follows:

(a) Load Memory Address Ø17763 with 1Ø37XX, where XX will be the select code of the photoreader in your configuration.

(b) Load Memory Address 1Ø7764 with 1Ø23XX.

(c) Load Memory Location Ø17766 with 1Ø25XX.

(d) Set Protective Loader Switch to the PROTECTIVE position.

NOTE

In an 8K machine, location Ø17772 should contain the constant 16Ø1ØØ. In a 4K machine this constant is 17Ø1ØØ.

C. MAINTENANCE PROCEDURES

1. Inspection

a. Be sure all power is OFF.

b. Check the mechanical condition of all connectors, switches, modules and PC boards.

c. Check that all PC boards are installed in proper locations. Refer to the board location diagram.

CAUTION

The component side of each PC board should be on the right-hand side when viewed from the front.

d. Check the three rear panel switches (located on front panel door) as follows:

MEMORY	NORM
PHASE	NORM
INSTRUCTION	NORM

2. Power Check

a. Press the front panel POWER pushbutton and check that power comes on. The POWER lamp will light.

b. Check that all six blower fans are running.

c. Open front panel door. Check all voltage test points on the Crowbar Assembly (A121) for proper voltages (±5%).

d. Press POWER pushbutton OFF. The Power Relay (K1), located in lower left rear of Power Supply Assembly, should "drop" out (click) within 1 second. If not, check relay K1 for welded contacts and proper operation.

3. Control Panel Checks

a. Indicator Checks

(1) Press POWER pushbutton ON and OFF several times and check front panel indicators each time as follows:

POWER	ON
RUN	OFF
HALT	ON
FETCH	ON
INDIRECT	OFF
EXECUTE	OFF
INTERRUPT	OFF

(2) If lamp(s) fail to light, check lamps.

NOTE

If the FETCH or HALT lights do not come on, or if more than one "phase" light comes on, check the "power on/off pulse" (POFP) at pin 56 on A1 and pin 77 on A106 (STG).

b. Register Checks

(1) Load all Registers with "ones" as follows:

(a) Turn MEMORY switch to OFF.

(b) Set SWITCH REGISTER to 177777.

(c) Depress LOAD MEMORY pushbutton. The T-Register should indicate 177777. If not, check for possible failed lamps. If test still fails, check A101 through A106.

(d) Depress LOAD A pushbutton. The A-Register should indicate 177777. If not, check for possible failed lamps. If test still fails, check a LIA (SC = Ø1) instruction using SINGLE CYCLE operation.

(e) Depress LOAD B pushbutton. The B Register should indicate 177777. If not, check for failed lamps. If test still fails, check a LIB (SC = Ø1) instruction using SINGLE CYCLE operation.

(f) Depress LOAD ADDRESS pushbutton. The P and M-Registers should both indicate 177777. If not, check for failed lamps. If test still fails, check the appropriate control functions:

P-Register	STP at pins 7, 8, and 74 on the Instruction Decoder Board (A107)
M-Register	STM at pins 20, 21, 26, 27 and 28 on the Instruction Decoder Board (A107)

If these functions are normal, check A101.

(2) Load all Registers with "zeroes" as follows:

(a) Set SWITCH REGISTER to ØØØØØØ.

(b) Press LOAD ADDRESS pushbutton. The P and M-Registers should indicate ØØØØØØ. If not, check the P or M-Registers on the RAF Boards (A102 through A105).

(c) Depress LOAD A pushbutton. The A-Register should contain ØØØØØØ. If not, check the A-Register on RAF Boards (A102 through A105).

(d) Depress LOAD B pushbutton. The B-Register should contain ØØØØØØ. If not, check the B-Register on RAF Boards (A102 through A105).

(e) Depress LOAD MEMORY pushbutton. The T-Register should contain ØØØØØØ. If not, check the T-Register on RAF Boards (A102 through A105). If test still fails, check A101-A106.

(3) Indexing Check

(a) Set all Registers to "zeroes".

(b) Depress LOAD MEMORY pushbutton several times. The contents of the P and M-Registers should be indexed by "one" each time the switch is depressed. If not, check the following control functions:

RPRB at pin 72 on the Instruction Decoder Board (A107)
SBØ at pin 81 on the Instruction Decoder Board (A107)
ADF at pin 75 on the Instruction Decoder Board (A107)
$\overline{\text{OPO}}$ at pin 16 on the Instruction Decoder Board (A107)
PH3 at pin 60 on the Instruction Decoder Board (A107)
T67 at pin 69 on the Instruction Decoder Board (A107)

(c) Depress DISPLAY MEMORY pushbutton. The contents of the P and M-Registers should be indexed by "one" each time the switch is depressed. If not, check the following control functions:

RPRB at pin 72 on the Instruction Decoder Board (A107)
SBØ at pin 81 on the Instruction Decoder Board (A107)
ADF at pin 75 on the Instruction Decoder Board (A107)
$\overline{\text{OPO}}$ at pin 16 on the Instruction Decoder Board (A107)
PH3 at pin 60 on the Instruction Decoder Board (A107)
T67 at pin 69 on the Instruction Decoder Board (A107)

(d) Depress SINGLE CYCLE pushbutton. The contents of the P and M-Registers should be indexed by "one" each time the switch is depressed. If not, check the following control functions:

RPRB at pin 72 on the Instruction Decoder Board (A107)
SBØ at pin 81 on the Instruction Decoder Board (A107)
ADF at pin 75 on the Instruction Decoder Board (A107)
$\overline{\text{OPO}}$ at pin 16 on the Instruction Decoder Board (A107)
PH3 at pin 60 on the Instruction Decoder Board (A107)
T67 at pin 69 on the Instruction Decoder Board (A107)

4. Logic Function Tests

a. The "NOP" Function

(1) Set all Registers to ØØØØØØ.

(2) Depress RUN pushbutton. The P and M-Register should "glow" dimly with bit 15 of both Registers flickering on and off. If the machine fails to run, check the following functions:

SWC at pin 79 on the Timing Generator Board (A106)
RNS at pin 70 on the Timing Generator Board (A106)

(3) Depress HALT pushbutton. The HALT lamp should come on and all Registers should stop flickering. If the machine does not halt, check the following control functions:

PEH at pin 57 on the Timing Generator Board (A106)
HLS at pin 50 on the Timing Generator Board (A106)
$\overline{\text{HLS}}$ at pin 45 on the Timing Generator Board (A106)

b. Addressable "A" and "B" Functions

(1) Set SWITCH REGISTER to ØØØØØØ.

(2) Depress LOAD ADDRESS pushbutton.

(3) Set SWITCH REGISTER to ØØØ777 and then press LOAD MEMORY pushbutton. The A and T-Registers should both contain ØØØ777, and both the P and M-Registers should be indexed by one (ØØØØØ1).

(4) Set the SWITCH REGISTER to 1774ØØ and press LOAD MEMORY pushbutton. The T and B -Registers should both contain 1774ØØ. The P and M-Registers should be indexed by one (ØØØØØ2).

(5) Set SWITCH REGISTER to ØØØØØØ and depress LOAD ADDRESS pushbutton.

(6) Depress DISPLAY MEMORY pushbutton. The A and T-Registers should contain ØØØ777. If not, check the AAF function at pin 77 on the Shift Logic Board (A108).

(7) Depress DISPLAY MEMORY pushbutton. The B and T-Registers should contain 1774ØØ. If not, check the BAF functions at pin 80 on the Shift Logic Board (A108).

c. The XOR Function

(1) Set all Registers to ØØØØØØ.

(2) Load the A-Register with Ø2ØØØ1 and note the status of the EXTEND and OVERFLOW panel lights.

(3) Depress SINGLE CYCLE pushbutton and check panel lights and Registers as follows:

T-Register	Ø2ØØØ1
P-Register	ØØØØØØ*
M-Register	ØØØØØ1*
A-Register	Ø2ØØØ1
B-Register	ØØØØØØ
EXTEND	Unchanged
OVERFLOW	Unchanged
FETCH	OFF
INDIRECT	OFF
EXECUTE	ON
INTERRUPT	OFF

*Note difference in P and M-Registers at start of EXECUTE phase.

If this test fails, check control functions as follows:

$\overline{\text{EOF}}$ at pin 67 on the Instruction Decoder Board (A107)
RTSB at pin 82 on the Instruction Decoder Board (A107)
RARB at pin 19 on the Instruction Decoder Board (A107)
STBA at pin 50 on the Instruction Decoder Board (A107)

(4) Now load the A-Register with ØØØ777 and the B-Register with 177ØØ.

(5) Depress SINGLE CYCLE pushbutton and check panel lights and registers as follows:

T-Register	177ØØ
P-Register	ØØØØØ1*
M-Register	ØØØØØ1*
A-Register	177Ø77
B-Register	177ØØ
EXTEND	Unchanged
OVERFLOW	Unchanged
FETCH	ON

*Note identical contents of P and M-Registers at start of FETCH phase.

INDIRECT	OFF
EXECUTE	OFF
INTERRUPT	OFF

If this test fails, check control functions as follows:

$\overline{\text{EOF}}$ at pin 67 on the Instruction Decoder Board (A107)
RTSB at pin 82 on the Instruction Decoder Board (A107)
RBRB at pin 18 on the Instruction Decoder Board (A107)
STBB at pin 51 on the Instruction Decoder Board (A107)

(6) If all tests described in steps b. (1) through b. (6) fail, check control functions as follows:

PH1 at pin 41 on the Timing Generator Board (A106)
PH3 at pin 60 on the Timing Generator Board (A106)
$\overline{\text{OPO}}$ at pin 42 on the Timing Generator Board (A106)

5. Memory Checks

a. Memory Turn-On

(1) Press POWER pushbutton to OFF.

(2) Set Rear Panel MEMORY switch to NORM.

(3) Press POWER pushbutton to ON.

b. Memory Module Test

(1) Set SWITCH REGISTER to all "zeros" and depress LOAD ADDRESS pushbutton.

(2) Set SWITCH REGISTER to 07000 and press LOAD A and SINGLE CYCLE pushbuttons (in that order).

(3) Set SWITCH REGISTER to all "ones" and press Load A pushbutton.

(4) Open the front door and set the Phase switch to the LOOP position.

(5) Press PRESET and RUN on front panel. The T-Register should contain all "ones" and the P&M registers will increment thru all addresses

(6) Depress HALT pushbutton and set the PHASE switch to OFF.

(7) Clear all registers to all "zeros" and load the A-Register with 060000.

(8) Press PRESET and SINGLE CYCLE in that order.

(9) Set the PHASE switch to the LOOP position.

(10) Press the RUN pushbutton. The T, A and B registers should contain all "ones" and the P & M Registers will increment through all addresses. If not, check the following memory timing signals.

MRT at pin 29 on the Timing Generator Board
MST at pin 32 on the Timing Generator Board
MTT at pin 25 on the Timing Generator Board
MWT at pin 35 on the Timing Generator Board

c. Sense Amplifier Check

NOTE

Perform this check for both Sense Amplifers (A12 and A13).

(1) Synchronize an Oscilloscope on the MST signal at pin 41 on A12 or A13, and measure the pulses appearing on the collectors of the transistors in each amplifier circuit.

(2) Adjust the variable resistors until the double-pulses are coincident.

Transistor	Resistor
Q1	R7
Q11	R17
Q21	R27
Q31	R37
Q41	R47
Q51	R57
Q61	R67
Q71	R77
Q81	R87
Q91	R97
Q101	R107
Q111	R117
Q121	R127
Q131	R137
Q141	R147
Q151	R157
Q161	R167

NOTE

There will not be any signal on Q161 unless the Parity Error Option is present.

ABSOLUTE BLOCK LOADER LISTING

No.	Location	Contents		Instruction	
ØØØ1	ASMB, A, B, L, T				
ØØØ2	177ØØ			ORG 177ØØB	
ØØØ3	177ØØ	1Ø77ØØ	LOAD	CLC Ø,C	TURN OFF ALL DEVICES.
ØØØ4	177Ø1	Ø6377Ø		LDA STAI	SET STORE INDIRECT INSTRUCTION.
ØØØ5	177Ø2	1Ø65Ø1		LIB 1	CHECK FOR OPTIONS.
ØØØ6	177Ø3	ØØ4Ø1Ø		SLB	SR (Ø) = 1?
ØØØ7	177Ø4	ØØ24ØØ		CLA	YES: CHECKSUM VERIFY OPTION.
ØØØ8	17705	ØØ6Ø2Ø		SSB	SR(15) = 1?
ØØØ9	177Ø6	Ø63771		LDA CPAI	YES: DUMP VERIFY OPTION.
ØØ1Ø	177Ø7	Ø73736		STA OPTI	STORE OPTION INSTRUCTION.
ØØ11	1771Ø	ØØ64Ø1		CLB,RSS	BYPASS EOT CHECK FOR LEADER.
ØØ12	17711	Ø67773	CONT	LDB CM11	SET B = -11 FOR EOT TEST.
ØØ13	17712	ØØ6ØØ6	EOTCH	INB,SZB	ENT OF TAPE?
ØØ14	17713	Ø27717		JMP LD1	NO: GET NEXT CHARACTER.
ØØ15	17714	1Ø77ØØ		CLC Ø,C	TURN OFF ALL DEVICES.
ØØ16	17715	1Ø2Ø77		HLT 77B	EOT HALT: T = 1Ø2Ø77.
ØØ17	17716	Ø277ØØ		JMP LOAD	START NEXT TAPE.
ØØ18	17717	Ø17762	LD1	JSB CHAR	GET A CHARACTER.
ØØ19	1772Ø	ØØ2ØØ3		SZA,RSS	IS IT THE WORD COUNT?
ØØ2Ø	17721	Ø27712		JMP EOTCH	NO: CHECK FOR EOT.
ØØ21	17722	ØØ31Ø4		CMA,CLE, INA	NEGATE & RESET E FOR OVER-FLOW CHE
ØØ22	17723	Ø73774		STA COUNT	SET WORD COUNT.
ØØ23	17724	Ø17762		JSB CHAR	SKIP THE NEXT CHARACTER.
ØØ24	17725	Ø17753		JSB WORD	GET STARTING ADDRESS.
ØØ25	17726	Ø7ØØØ1		STA 1	INITIALIZE CHECKSUM IN B.
ØØ26	17727	Ø73775		STA ADDRS	ALSO STORE IN LOADING ADDRESS POI
ØØ27	1773Ø	Ø63775	LD2	LDA ADDRS	CHECK LOADING ADDRESS TO PRE-VENT LOADER FROM SUICIDING.
ØØ28	17731	Ø43772		ADA MAXAD	
ØØ29	17732	ØØ2Ø4Ø		SEZ	IS LOADING ADDRESS GREATER THAN L
ØØ3Ø	17733	Ø27751		JMP ADERR	YES: TERMINATE LOADING.
ØØ31	17734	Ø17753		JSB WORD	GET NEXT WORD IN A.

ABSOLUTE BLOCK LOADER LISTING (Cont'd)

No.	Location	Contents		Instruction	
ØØ32	17735	Ø44ØØØ		ADB Ø	ADD IT TO THE CHECKSUM.
ØØ33‡	17736	ØØØØØØ	OPTI	NOP	OPTIONAL INSTRUCTION: STA Ø, I/CPA
ØØ34	17737	ØØ21Ø1		CLE, RSS	BYPASS FOLLOWING HALT EXCEPT FOR DUMP VERIFY ERROR HALT.
ØØ35	1774Ø	1Ø2ØØØ		HLTØ	
ØØ36	17741	Ø37775		ISZ ADDRS	INCREMENT LOADING ADDRESS POINTER ANY MORE WORDS IN BLOCK?
ØØ37	17742	Ø37774		ISZ COUNT	
ØØ38	17743	Ø2773Ø		JMP LD2	YES: LOOP TO LD2 TO LOAD NEXT WORD.
ØØ39	17744	Ø17753		JSB WORD	NO: GET CHECKSUM FROM TAPE.
ØØ4Ø	17745	Ø54ØØØ		CPB Ø	CHECKSUMS AGREE?
ØØ41	17746	Ø27711		JMP CONT	YES: CHECK FOR EOT.
ØØ42	17747	1Ø2Ø11		HLT 11B	NO: CHECKSUM ERROR
ØØ43				T = 1Ø2Ø11, A =	TAPE CHECKSUM, B = LOADER CHECKS
ØØ44	1775Ø	Ø277ØØ		JMP LOAD	START OVER.
ØØ45	17751	1Ø2Ø55	ADERR	HLT 55B	ERROR HALT FOR ILLEGAL ADDRESS: T
ØØ46	17752	Ø277ØØ		JMP LOAD	START OVER.
ØØ47‡	17753	ØØØØØØ	WORD	NOP	READS ONE WORD FROM TAPE.
ØØ48	17754	Ø17762		JSB CHAR	GET FIRST CHARACTER.
ØØ49	17755	ØØ1727		ALF, ALF	POSITION IT.
ØØ5Ø	17756	Ø73776		STA TEMP	SAVE IT.
ØØ51	17757	Ø17762		JSB CHAR	GET SECOND CHARACTER.
ØØ52	1776Ø	Ø33776		IOR TEMP	PACK WITH FIRST.
ØØ53	17761	127753		JMP WORD, I	RETURN WITH WORD IN A.
ØØ54‡	17762	ØØØØØØ	CHAR	NOP	READ A CHARACTER FROM PHOTOREADER.
ØØ55*	17763	1Ø37RA		STC PR, C	TURN ON PHOTOREADER.
ØØ56*	17764	1Ø23RA		SFS PR	WAIT FOR FLAG INDICATING DATA IS READY.
0057	17765	Ø27764		JMP *-1	
0058*	17766	1Ø25RA		LIA PR	LOAD CHARACTER INTO A.
ØØ59	17767	127762		JMP CHAR, I	RETURN.
ØØ6Ø	1777Ø	173775	STAI	STA ADDRS, I	NORMAL CONTENTS OF OPTIONAL INSTR

ABSOLUTE BLOCK LOADER LISTING (Cont'd)

No.	Location	Contents		Instruction	
ØØ61	17771	153775	CPAI	CPA ADDRS, I	DUMP VERIFY OPTIONAL INSTRUCTION.
ØØ62†	17772	16Ø1ØØ	MAXAD	ABS-LOAD	LOADER PROTECTION VALUE.
ØØ63	17773	177765	CM11	DEC-11	EOT CHARACTER COUNT.
ØØ64‡	17774	ØØØØØØ	COUNT	BSS 1	COUNTS WORDS IN BLOCK.
ØØ65‡	17775	ØØØØØØ	ADDRS	BSS 1	LOADING ADDRESS POINTER.
ØØ66‡	17776	ØØØØØØ	TEMP	BSS 1	HOLDS UPPER CHARACTER FOR PACKING PHOTOREADER I/O ADDRESS.
ØØ67	ØØØ1Ø		PR	EQU 1ØB	
ØØ68				END	
END					

*R/A Indicates Select Code of Photoreader.

†160100 = 8K 170100 = 4K

‡Contents Immaterial