HEWLETT hp PACKARD

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NEW PRODUCT
INFORMATION

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(Photos enclosed)

FOR IMMEDIATE RELEASE

TWO NEW COMPUTERS OFFER MORE CORE PER DOLLAR

New Memory Costs Less, Takes Much Less Space

Cost Of Additional Memory Greatly Reduced. Cost of Some Basic Computer Models Also Reduced.

A new high-density core memory developed by Hewlett-Packard makes it possible for two new HP computers to have twice as much memory capacity as their predecessors had in the same size main-frames. As a result, the computers do not require external add-on memory extenders, even when their core memories are expanded to maximum size. Elimination of external memory extenders and lower manufacturing costs for the new type memory have led to substantial cost reductions, especially for computers with more than the minimum amount of core. Viewed another way, the new computers offer substantially more memory for the same amount of money.

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The larger of the two new computers is the 2116C, a 16-bit machine with a memory cycle time of 1.6 microseconds. At a price of $20,000 including an 8K (8192-word) core memory, the 2116C is $4,000 less than its predecessor, the HP 2116B, used to cost. Additional core can be added to the 2116C in 8K increments at $10,000 per increment, up to a maximum total core memory of 32K. A 2116C with the maximum amount of core memory — 32,768 words — costs $50,000, or $19,000 less than a 2116B with the same amount of memory used to cost. What's more, the 2116C's maximum memory fits in the mainframe, whereas the 2116B requires an outside extender to reach 32K.

The smaller of the two new computers, Model 2114C, is also a 16-bit machine, but with a memory cycle time of 2.0 microseconds. The 2114C with 4K core memory will sell for $8,500, the same as its predecessor, Model 2114B. Additional core in 4K increments will cost $4,500 per increment. But while the 2114B's maximum memory was 8K, the new 2114C can have up to 16K, all of it in the mainframe.

For the present, the 2116B and 2114B will remain in the HP product line, along with the new C models. The 2116B's price is being reduced to $20,000, and prices of the extender and additional core memory for the 2116B are also being reduced. A 2116B with extender and 32 K core memory now costs $58,000.

Complete Software and Peripherals

The new computers will operate in the same system configurations as the earlier models, and are compatible with all existing HP software, peripherals, processor options, and accessories. Thus the new computers have a large repertoire of existing hardware and software supporting systems.

Software available includes FORTRAN, ALGOL, and BASIC compilers, drivers for peripherals and laboratory instruments, FORTRAN library, utility programs, diagnostics, assembler, loader, many special applications programs, and 6 operating systems — basic control system, disc operating system, magnetic-tape system, real-time executive system, time-shared BASIC system, and educational system. Peripherals available include all the standard computer peripherals, as well as many laboratory instruments.

Availability and Prices

First deliveries of the HP 2116C computer are scheduled for December 1970. Deliveries of the HP 2114C minicomputer are scheduled to begin in late January 1971. The two computers can either be purchased at the prices given above, or leased. The HP lease plan offers terms of 2 to 5 years, at monthly rates of 4.4% to 2.15% of the purchase price.

High-Density Memory

The new memory that makes the new computers possible takes full advantage of up-to-date core and integrated-circuit technology to achieve not only small size, but also better serviceability. Like many of the newest core memories, the HP-developed memory is of the planar type — but with a difference. In the HP memory, the plane containing the cores is folded so that it forms a thin stack, small enough to be mounted on one of the computer's printed-circuit boards. A complete 8K memory including the core stack and all peripheral circuitry fits on 3 printed circuit boards. These 3 boards replace 6 boards plus a separate two-inch-high core stack.

The new HP memory is a 3-wire memory (X address, Y address, and sense-inhibit) rather than a 4-wire memory with separate sense and inhibit wires as was the old memory. Elimination of the fourth wire saves assembly time and reduces the cost of the memory.

Serviceability of the memory has been improved by packaging the diodes used in the peripheral circuitry in pluggable modules that are easily replaced in the field. These diodes have always been among the more critical parts in core arrays.

Although the new memory simply plugs into the computer mainframes, it cannot be used in earlier HP computers. The mainframes of the 2116C and 2114C are different from earlier models.

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EXTENSION 2004

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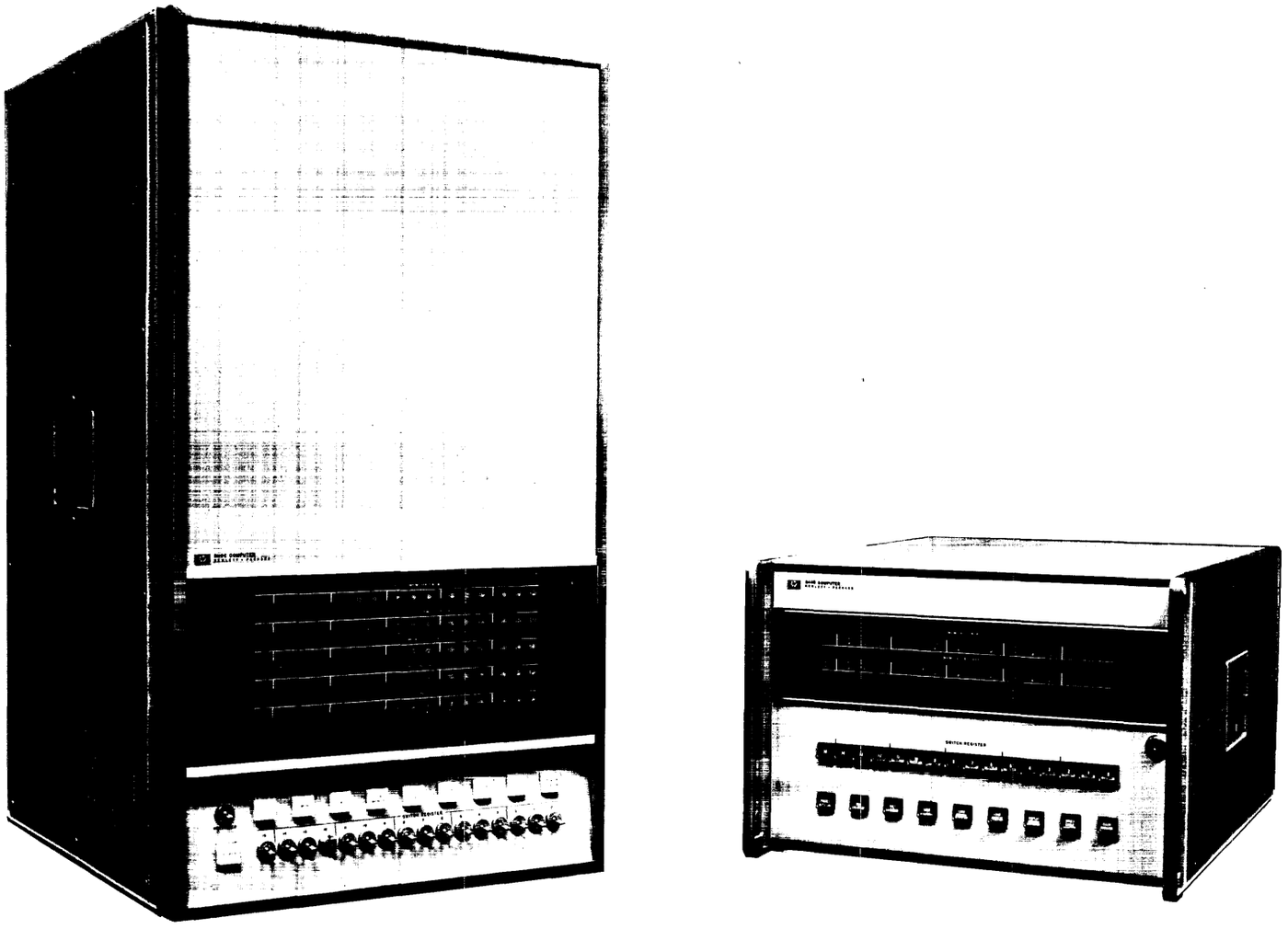
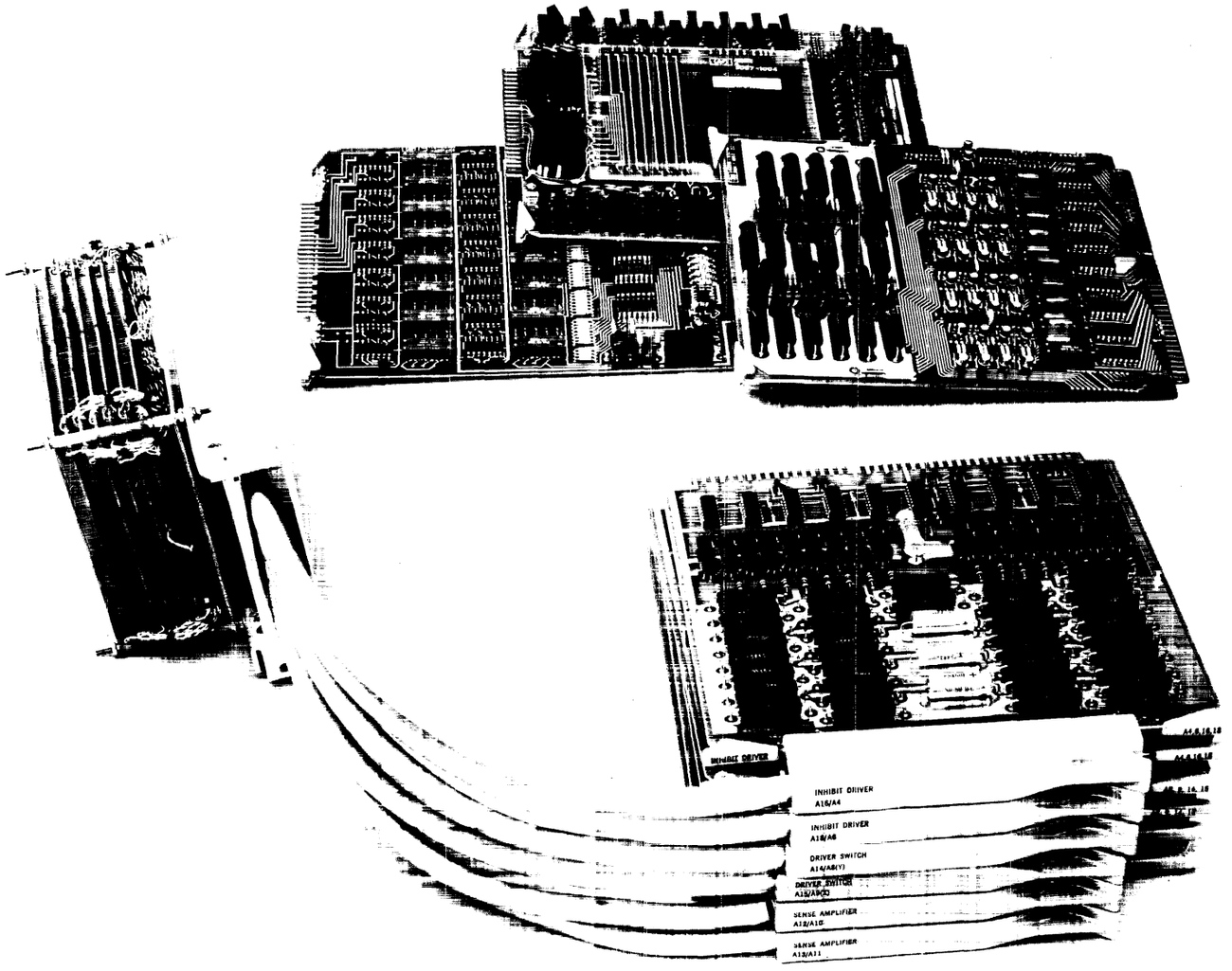
If you choose to review this item, fastest response to your readers' inquiries will be assured by mailing them to INQUIRIES MANAGER, Hewlett-Packard Company, 1601 California Avenue, Palo Alto, California 94304.



Hewlett-Packard 2116C (left) and 2114C Computers have new cost-saving and space-saving core memory.



Three boards at top of picture are complete 8K memory for Hewlett-Packard 2116C and 2114C Computers. 8K memory for 2116B is at bottom.

.1 BACKGROUND

Hewlett-Packard announced the HP 2116C in October 1970 and installed the first system in December 1970. The 2116C is a reengineered version of the successful 2116B which, in turn, was reengineered from the 2116A introduced in 1966. Notable improvements in the 2116C include a folded planar memory design that allows 32,768 words of core memory in the processor main frame and a lower price.

Hewlett-Packard has offered three compatible computer lines, the 2116, 2115, and 2114. The 2114 and 2115 processors are smaller and 25 percent slower than the 2116's. All use the same peripheral devices, and subject to configuration requirements, all use the same software. The only models currently marketed by Hewlett-Packard are the 2114B, 2114C, and 2116C.

Hewlett-Packard entered the digital computer field as a logical extension of its interest in digital instrumentation and testing systems. Its activity in the computer market has steadily progressed from the use of computers in conjunction with Hewlett-Packard measuring instruments to a much wider approach to the market, particularly in small-machine time-sharing and in educational applications. Hewlett-Packard has tended to concentrate on the production of complete computer systems for particular areas of computer application. An early application of the 2116A was in data acquisition, for which a specialized combined hardware/software system was marketed; this was followed by a hardware/software system for the automatic testing of printed-circuit boards using a special-purpose programming language called AuTest. These systems are still available with the 2116C.

In the past few years, however, Hewlett-Packard has developed and successfully marketed time-sharing systems using the Basic programming language in a conversational mode. One such system, using a Hewlett-Packard optical mark reader for the input of Basic language source programs, enables schoolchildren to prepare their own source programs simply by marking specially printed cards with an ordinary pencil.

A number of in-house and service bureau time-sharing systems use the 2116B or 2116C computer.

The larger Hewlett-Packard time-sharing systems, 32 terminals, use the 2114B or C as a front-end terminal processor for the 2116C. Hewlett-Packard also offers a Disc Operating System for conventional batch processing with the 2116C.

A basic system comprising a 2116C computer with 8,192 16-bit words of 1.6-microsecond core memory, a 2752A Teleprinter with paper tape input/output, 16 I/O channels, and 16 interrupt levels sells for $16,000.

.2 HARDWARE

.21 Central Processor and Working Storage

The basic HP 2116C computer has a main memory of 8,192 16-bit words, expandable to 32,768 words, with a cycle time of 1.6 microseconds. The instruction set is a straightforward single-address code, with a multilevel indirect addressing capability and the microprogramming of several shifting and testing operations into a single instruction. Addition is the only arithmetic operation in the basic instruction set; subtraction requires a complement instruction followed by an addition; hardware multiplication and division are among the extra instructions provided by the optional extended arithmetic unit. There are two accumulators, registers A and B, which are used as a single, double-word accumulator by the extended arithmetic unit instructions. There are no index registers, and list addressing must be performed using indirect addressing. There is, however, an instruction that increments a specified core location and skips the following instruction if the result is zero. This instruction can be useful in incrementing a stored address and is also used in counting and loop control. The core store is conceptually divided into 1,024-word sections called pages. Only locations in the current page or the base page can be addressed directly from an instruction, but the whole of main memory is indirectly addressable.

All the hardware arithmetic operations use single-word operands and results, except that the (optional) multiplication instruction provides a double-word result. There is no floating-point hardware, but a set of floating-point subroutines operate on double-word operands and results. There are no standard facilities for multiple-precision arithmetic.

The basic processor contains provision for 60 levels of interrupt, of which 56 are available for input/output devices; however, only 16 of the peripheral device interrupt levels can be used without additional optional equipment. The interrupt of highest priority is power fail, which has an optional automatic restart facility; a memory parity fail interrupt is available optionally. The optional memory protect interrupt facility provides for an interrupt when there is an attempt to alter a main memory location with an address lower than a value previously set by the program. Individual interrupts, all interrupts of lower priority than a specified level, or the whole interrupt system can be enabled or disabled by program.

.22 Mass Storage

Fixed-head disc and drum units provide up to a million words of mass storage for the HP 2116C; moving-head disc units with removable disc packs provide larger quantities of mass storage, over 20 million words.

The HP 2766A Disc Memory and the HP 2773A Drum Memory are fixed-head per track units and provide fast-access (8.7 milliseconds) mass storage. The HP 2766A provides from 262,144 to 1,048,576 16-bit words of storage in increments of 262,144 words. The HP 2773A provides from 393,216 to 1,048,576 16-bit words, the first increment containing 393,316 words and the second 262,144 words. Both units store 32 64-word sectors on each track, and the peak transfer rate is 118K words per second.

The HP 2883 Disc File and the HP 2870A Moving Head Disc provide slower-access mass storage.

The HP 2883 stores 11,776,000 16-bit words on an HP 12868A 11-disc pack, which is completely compatible with the IBM 2316 Disk Pack. The disc rotates at 2,400 revolutions per minute. The average access time for a random seek is 50.5 milliseconds, 38 milliseconds for head movement and 12.5 milliseconds for latency. (As a result of extensive benchmarks on the 2883, Hewlett-Packard lists the average overall access time as 32 milliseconds.) Data is stored in 23 128-word sectors per track. The peak transfer rate is 155,000 words per second. The controller can handle two HP 2883 Disc Files.

The HP 2870A stores 1,247,232 16-bit words. One fixed disc and one removable disc cartridge are serviced by the same moving head. The 12563A Cartridge is not IBM-compatible. The disc rotates at 1,500 revolutions per minute. The average access time is 90 milliseconds, 70 milliseconds for head movement and 20 milliseconds for latency. The peak data transfer rate is 38,400 words per second. Data is stored in twelve 128-word sectors on each track. The controller can handle up to four 2870A Disc Drives.

.23 Input/Output Channels and Devices

The basic HP 2116C computer contains logic for connecting up to 16 input/output channels; this total can be increased to a maximum of 48 with options. Each input/output channel is connected to a standard input/output interface card, which provides registers and flags for communication between the external device and the central processor, and each channel also has its own interrupt level. The normal mode of input/output operation uses commands to transfer information between one of the two accumulators in the processor and the data buffer in the input/output interface. This means that no more than 16 bits of information can be transferred with a single command. The only restrictions on the simultaneous use of different devices are those imposed by the execution rate of the coding needed to service the resulting interrupts; this imposes an overall restriction of about 60,000 words per second on the data transfer rate attainable by this method.

Normally, one input/output device is connected to each input/output channel, but devices such as magnetic tapes which need control information, must have two channels for their connection.

The direct memory access (DMA) option allows block transfers on a cycle-stealing basis at rates up to the cycling rate of the main memory (625,000 words per second). Not more than two devices can use the DMA at any one time. The DMA can be used to address any device connected to an input/output channel, and the device for which DMA is currently being used can be changed by program.

The principal input/output devices available are summarized in Table I. The disc and drum memory units require the DMA option for their use. Beside the devices listed, there is a wide range of analog/digital and digital/analog control equipment and a variety of interfaces to Hewlett-Packard measuring instruments such as electronic counters, quartz thermometers, and digital voltmeters.

.3 SOFTWARE

A comprehensive range of standard software is available for the HP 2116C. Hewlett-Packard has developed software for its computers as an extension of its gradual entry into the computer market and thorough exploration of one area of application at a time. The result is a number of special-purpose packages for data acquisition, testing of logic modules, and interactive use of the Basic language by a single user or by multiple users on a timesharing basis; but these systems are not unified under a single operating system. For general use, there is a collection of operating programs collectively known as the Basic Control System (not to be confused with the Basic language system) which includes assemblers, Fortran and Algol compilers, routines for loading, linking, and debugging relocatable programs and sets of library subroutines, and input/output device drivers. The Basic Control System is paper-tape based, but a magnetic tape version is also available.

The Hewlett-Packard Basic Language System is a separate operating system that provides a conversational programming capability in the Basic language for a single user using the console teletypewriter. More sophisticated Basic language systems, the HP 2000A, B, and C Time-Shared Basic Systems, allow the simultaneous use of Basic by up to 32 remote or on-site users on a time-sharing basis. The Basic language systems use an interpretive mode of execution to provide for the simple alteration of programs; Hewlett-Packard does not feel that this method of program execution seriously affects the overall efficiency of the system since its computing capacity is mainly governed by the fact that subroutines have to be used for all floating-point arithmetic operations.

The 2000A Time-Sharing System supports 16 terminals, while the 2000B and C support 32 terminals. A basic version of the 2000B is also available for 16 terminals. All of the time-sharing systems use a fast-access drum or disc unit to store system and user programs. The 2000A system requires a minimum of 393,000 words of mass storage, and the 2000B uses 512,000 (16 terminals) or 786,432 (32 terminals) words. The main differences between the A and B versions are the number of terminals supported and the maximum number and size of user files that can be stored.

The 2000C Time-Sharing System is a much more powerful system, which uses an HP 2114B or C computer as a front-end terminal processor for the 2116C. Users can store files that are up to 32,767 512-word records long. A "sleep" provision compacts the files stored on the disc, rolls the time sharing system out onto magnetic tape or removable disc, loads the Disc Operating System (DOS) for batch processing during off hours, and restores the time sharing system when required.

The time sharing systems support as terminals, the teleprinters, 2570A Coupler/Controller, 7200A Graph Plotter, 2761B Optical Mark Reader, and the 2600 CRT Keyboard. The 2570A and the 7200A are connected in series with a teleprinter.

The Real-Time Executive System provides an environment for running real-time programs, giving a rapid response to external events, and simultaneously running lower priority programs such as compilations and assemblies. Only one background processing program can be run at a time, but real-time programs can be either memory resident or disc resident depending on their priority.

The Disc Operating System (DOS) provides conventional batch processing of programs written in Algol, Fortran IV, or assembly language. DOS utilizes the new moving-head disc units offered by Hewlett-Packard.

TABLE I. HP 2116C INPUT/OUTPUT UNITS

Type of Input/Output	Peripheral Device	Rated Speed	Controller (1)
Console Typewriter	HP 2752A Teletypewriter (modified Teletype ASR 33)	10 char/sec	12531B
	HP 2754B Heavy-Duty Teletypewriter (modified Teletype ASR 35)	10 char/sec	12531B
Punched Tape	HP 2752A Teletypewriter (modified Teletype ASR 33)	10 char/sec	12531B
	HP 2754B Heavy-Duty Teletypewriter (modified Teletype ASR 35)	10 char/sec	12531B
	HP 2748A Punched Tape Reader	500 char/sec	12597A-002
	HP 2753A Tape Punch	120 char/sec	12597A-003
Punched Card	HP 2891A Card Reader	1,000 cards/min	12882A
	HP 2761A-007 Optical Mark and Card Reader	200 cards/min	12602A
Printer	HP 2778A Line Printer (120-col line)	300 lines/min	12617A
	HP 2767A Line Printer (80-col line)	300 to 1,100 lines/min	12653A
	HP 2778A-001 Line Printer (132-col line)	300 lines/min	12617A
Magnetic Tape	HP 2020B 7-track Magnetic Tape Unit	30 ips	12538B
	HP 7970A-200 9-track Magnetic Tape Unit	25 ips	13181A-001
	HP 7970A-202 9-track Magnetic Tape Unit	37.5 ips	13181A
	HP 3030G Magnetic Tape Unit	75 ips	12559A
Digital Plotter	Interface for 563 or 565 CalComp Plotter		12560A
Data Communications	Interface to asynchronous dataphone		12587A
	Interface for synchronous send and receive		12618A
	Interface for synchronous receive only		12621A
	Interface for synchronous transmit only		12622A
	HP 2600A CRT Keyboard Terminal	10 to 218 char/sec	12880A
	HP 2570A Coupler/Controller		
	HP 7200A Graph Plotter		
Other	12554A General-Purpose Duplex Register (16 bits)		Self-contained
	12551B Relay Output Register (16 form-A contacts)		Self-contained
	12555A Two D/A Converter Channels (8 bits/channel)		Self-contained
	HP 12566A Microcircuit Interface Kit (16 bits)		Self-contained
	12539A Time Base Generator (100-μsec to 1,000-sec intervals)		Self-contained
	12597A General-Purpose Duplex Register (8 bits)		Self-contained

Notes:

(1) Hewlett-Packard supplies I/O devices in interface kits that include cabinets, power supplies, the device, and the interface to an I/O channel. The numbers listed are the model numbers of the interface kits.

HP 2116C SYSTEM CONFIGURATION

The basic HP 2116C computer system consists of a central processor with 8,192 16-bit words of core storage and provision for 16 input/output channels. Memory parity checking is optional. Processor options provide for inclusion of up to 32,768 words of core storage in 8,192-word increments. All core is housed in the processor cabinet.

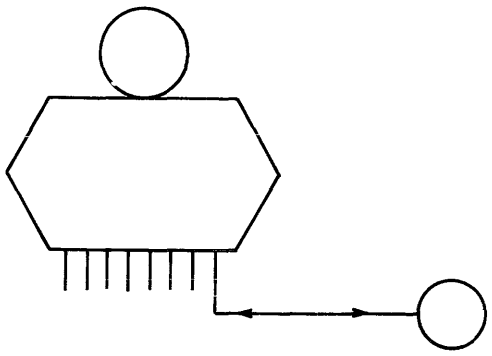
Optional features can increase the number of I/O channels by 16 or 32 to an overall maximum of 48 channels, each with its own interrupt level. Addition is the only arithmetic operation in the basic instruction set; subtraction is achieved by using a complement instruction followed by an addition; hardware multiplication and division are among the extra facilities provided by the optional extended arithmetic unit (EAU). If the optional direct memory access (DMA) feature is attached, any two of the input/output channels can be used in a high-speed block transfer mode; such channels are selectable and changeable by program.

A range of teleprinters, paper tape, punched card, OCR, magnetic tape, and printing devices is available. Drum units and fixed-head discs are available for mass storage. Each of the peripheral devices is connected to a standard input/output channel — optional features allow the sharing of channels. Subject to the overall data transfer capacity of the processor, there is no restriction on the combination of devices that can be connected to the available input/output channels. The disc units and drum units require the DMA option for their use. Discs, drums, and magnetic tape units require two I/O slots. The only restrictions on input/output simultaneity are those imposed by the cycle time of the main memory (1.6 microseconds) and the speed of execution of the interrupt response code needed to handle the resulting external device interrupts. Only two devices can use the DMA option at any one time.

Data communications equipment includes teleprinters and a keyboard CRT terminal, which can be connected to a special multiplexor interface either by a direct cable up to a mile in length or via telephone lines. Interface kits provided by Hewlett-Packard include interfaces to simplex, half-duplex, and full-duplex synchronous data sets.

.1 DESKSIZE SCIENTIFIC SYSTEM (CONFIGURATION IX)

Deviations from standard configuration: . . . . . core storage capacity is 18% smaller.*

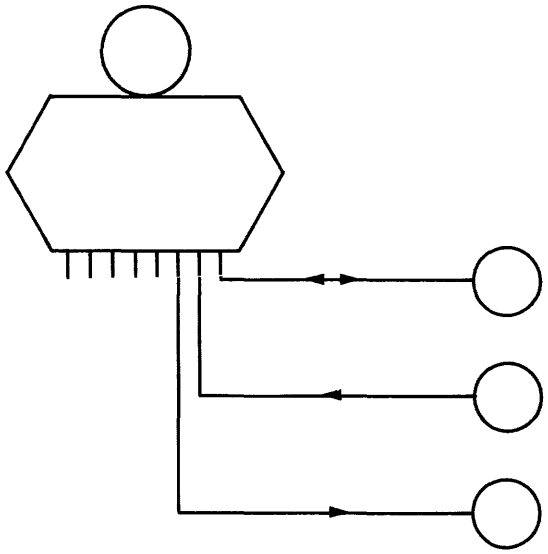


Equipment	Purchase Price
2116C Computer: includes 8,192 16-bit words of core storage	$14,000
2752A Teleprinter: includes keyboard, printer, paper tape reader, and paper tape punch (all 10 char/sec)	2,000
Optional feature included: . . . . . 12579A Extended Arithmetic Unit, for automatic multiplication and division	2,000
TOTAL PURCHASE PRICE	$18,000

* Storage requirement is based on storing two digits per 16-bit word; effective storage capacity can be increased by storing digital data in binary form.

.2 PUNCHED TAPE SCIENTIFIC SYSTEM (CONFIGURATION X)

Deviations from standard configuration: . . . . . core storage is 18% smaller.*
paper tape reader is 50% faster.
paper tape punch is 20% faster.
no index registers.
no floating-point hardware.

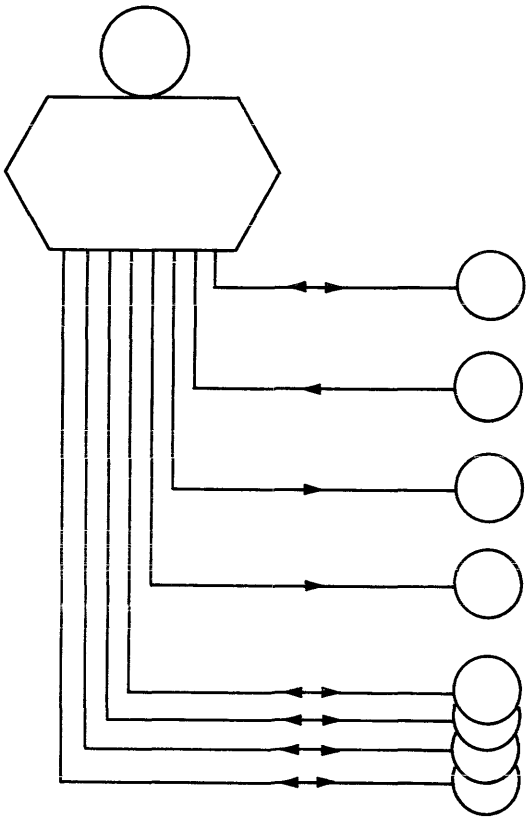


Equipment	Purchase Price
2116C Computer: includes 8,192 16-bit words of core storage	$14,000
005 Option: provides total main memory of 16,384 words	8,000
2752A Teleprinter: includes keyboard, printer, paper tape reader, and paper tape punch (all 10 char/sec)	2,000
2748A Punched Tape Reader: 500 char/sec	2,200
2753A Tape Punch: 120 char/sec	4,150
Optional feature included: . . . . . 12579A Extended Arithmetic Unit, for automatic multiplication and division	2,000
TOTAL PURCHASE PRICE	$32,350

* Storage requirement is based on storing two digits per 16-bit word; effective storage capacity can be increased by storing digital data in binary form.

.3 4-TAPE SYSTEM (CONFIGURATION XI)

Deviations from standard configuration: . . . . . core storage capacity is 18% smaller.*
magnetic tape is twice as fast.
printer is three times faster.
paper tape punch is 40% slower.
no floating-point hardware.
no index registers.



Equipment	Purchase Price
2116C Computer: includes 8,192 16-bit words of core storage	$14,000
005 Option: provides total main memory of 16,384 words	8,000
2752A Teleprinter: includes keyboard, printer, paper tape reader, and paper tape punch (all 10 char/sec)	2,000
2748A Punched Tape Reader: 500 char/sec	2,200
2753A Tape Punch: 120 char/sec	4,150
2767A Line Printer and Interface: 300 lines/min	12,500
13181A-001 Interface with four 7970A-200 Magnetic Tape Units: peak transfer rate of 30,000 char/sec	24,725
Optional feature included: . . . . . 12579A Extended Arithmetic Unit, for automatic multiplication and division	2,000
TOTAL PURCHASE PRICE	$69,575

* Storage capacity is based on storing two digits per 16-bit word; effective storage capacity can be increased by storing digital data in binary form.

.1 GENERAL

Working storage for the HP 2116C computer is provided by core storage in the mainframe. Random-access auxiliary storage is provided by several disc and drum devices. The basic characteristics of these components are listed in Table I.

TABLE I. HP 2116C INTERNAL STORAGE UNITS

Characteristic	HP 2116C Core Memory	HP 2773A/ HP 2774A/ HP 2774A-003 Drum Memories	HP 2766A/ -002/-003/ -004 Disc Memories	HP 2883A/ HP 2884 Disc Files	HP 2870A/ HP 2870A-001 Cartridge Drive Memory
Basic Use	Working storage	Auxiliary storage	Auxiliary storage	Auxiliary storage	Auxiliary storage
Storage Capacity					
Minimum, words	8,192	393,216	262,144	11,776,000	1,247,232
Maximum, words	32,768	1,048,576	1,048,576	23,552,000	4,988,928
Reserved storage	Up to 128 words	None	None	None	None
Controller	Integral	12610B Interface Kit	12610C Interface Kit	12565A Interface Kit	12557A Interface Kit
Connection to System	Integral	DMA channel	DMA channel	DMA channel	DMA channel
Changeable Storage	No	No	No	Yes	Yes
Peak Transfer Rate	625,000 words/ sec	118,000 words/sec	118,000 words/sec	155,000 words/sec	38,400 words/sec
Access Time	—	8.7 msec (avg)	8.7 msec (avg)	32 msec (avg)	98 msec (avg)
Cycle Time	1.6 μsec	17.4 msec/ revolution	17.4 msec/ revolution	25 msec/ revolution	40 msec/ revolution

.131 Core Storage

The basic HP 2116C computer includes 8,192 words of core storage. Optional features 005, 006, and 007 provide 16,384, 24,576, and 32,768 words of storage, respectively. All core is housed in the computer mainframe.

Each word consists of 16 data bits and a parity bit; the parity bit, however, serves no useful purpose unless the computer includes the 12591A Memory Parity Check with Interrupt, which is a single printed-circuit board providing an interrupt in case of a main memory parity error.

Although the first 64 locations of main memory are reserved for interrupt handling, some of these locations are available to the program if it requires fewer interrupt levels than the 60 provided. The first four words of main memory are not used; memory addresses 0 and 1 are used to refer to the A and B accumulators. Memory protection is optional, but the top 64 locations of main memory can be protected without the option by setting a switch on the operator's console — these locations are conventionally used to hold the loader.

Memory cycle time is 1.6 microseconds. The effective transfer rate for transferring data within core storage, provided both locations are directly addressable, is 156,300 words per second using straight-line coding and 45,500 words per second using a programmed loop. If one of the operand locations is not directly addressable, the effective transfer rate for straight-line coding is 125,000 words per second.

.132 Disc Storage

Disc storage for the 2116C is provided by the 2773A and 2766A Series of fixed-head nonremovable disc units and by the movable-head 2883A Disc Files and the 2870A Cartridge Disc Memories. The 2883A uses a disc pack compatible with the 2316 pack used on the IBM 2314 discs. The 2870A systems include one fixed and one removable disc per drive; the 12563A cartridge used with the 2870A stores 623,616 words. Table II summarizes the characteristics of the available disc units.

All disc units interface to the 2116C via interface kits that include the cabinet, controller, power supplies, and interfaces to the programmed I/O and DMA channel. All disc units require two I/O slots in the 2116C.

.133 Drum Storage

Hewlett-Packard supplies three drum units for use with the 2116C; these units differ only in storage capacity. The 2773A stores 393,216 16-bit words, the 2774A stores 786,432 words, and the 2774A-003 stores 1,048,576 words. Expansion kits are available to upgrade the 2773A and the 2774A in the field. The 2773A can be upgraded to either a 2774A or a 2774A-003; the 2774A can be upgraded to a 2774A-003.

All drum units interface to the 2116C via the 12610B Interface Kit, which includes the controller, cabinet, power supplies, and interfaces to the DMA and programmed I/O slots in the 2116C.

Table II summarizes the characteristics of the drum units.

Characteristic	HP 2773A/ HP 2774A/ HP 2774A-003 Drum Memories	HP 2766A/ -002/-003/ -004 Disc Memories	HP 2883A/ HP 2884 Disc Files	HP 2870A Cartridge Disc Memory
PHYSICAL FORM				
Data Volume per Band of 1 Track				
Words	2,048	2,048	2,944	1,536
Characters	4,096	4,096	5,888	2,072
Instructions	2,048	2,048	2,944	1,536
Sectors	32	32	23	12
Bands per Unit	192/384/512	128/256/384/512	200	203 (3 spares)
DATA CAPACITY				
Recording Surfaces	1	1/2/3/4	20	4
Tracks	192/384/512	128/256/384/512	200/surface	200/surface
Cylinders	—	—	200	200
Words	393,216/786,432/ 1,048,576	262,144/524,288/ 786,432/ 1,048,576	11,776,000	207; 200/surface
Characters	Twice no. of words	Twice no. of words	Twice no. of words	Twice no. of words
Modules	1	1	2	4
ACCESS TIMING				
Move Head to Selected Track (cylinder)	0	0	15 msec track-to-track, 38 msec avg random move	30 msec track-to-track, 70 msec avg random move
Wait for Beginning of Selected Track	0-17.4 msec	0-17.4 msec	0-25 msec	0-40 msec
Transfer Data	544 μsec/sector	544 μsec/sector	1.08 msec/sector	3.33 msec/sector
PERFORMANCE				
Transfer Load Size, words	64-16,384	64-16,384	128-16,384	128-16,384
Effective Transfer Rate, words/sec	78,467 (1 track)	78,467 (1 track)	38,993 (1 track)	24,576 (1 cylinder)
Update Cycle Rate, references/sec (record size)	22.7 (64 words)	22.7 (64 words)	9.8 (1 track)	5.8 (128 words)
Read-Only Reference Rate, references/sec (record size)	108.2 (64 words)	108.2 (64 words)	19.4 (128 words)	10.7 (128 words)

.1 GENERAL

.11 Identity: ..... HP 2116C Computer.

.12 Description

.121 Data Structure

Storage Locations —

Name of Location	Size	Use
Word	16 bits	basic addressable unit of core storage
Sector	64/128 words	basic addressable unit of disc and drum storage
Page	1,024 words	second level unit of core storage (directly addressed operand must be located within current page or base page)
Card column	12 bits	binary data (card reader)
Character	6 or 8 bits	alphanumeric data (input/output devices)

Information Formats —

Type of Data	Representation
Operands	
Nonarithmetic	1 word
Fixed-point arithmetic	1 word
Floating-point arithmetic	2 words (7-bit exponent plus sign, 23-bit fraction plus sign)
Instruction	1 word

.122 Central Processor

The basic HP 2116C computer is a binary, parallel, single-address processor with a fixed word length of 16 bits. There are two 16-bit accumulators, registers A and B, which can be addressed as locations 0 and 1 of main memory. The overflow register (0V) can be set as the result of arithmetic operations on either accumulator, and a further single-bit register, the E-register, can be used to provide communication of carries between the two accumulators.

Arithmetic is performed in two's complement notation. Addition is the only arithmetic operation provided in the basic instruction set; subtraction is performed with a complement instruction followed by an addition. Hardware multiplication and division are among the extra instructions provided by the optional extended arithmetic unit (EAU); there is no hardware floating-point provision. The full instruction complement is listed in Tables I and II.

TABLE I. HP 2116C STANDARD INSTRUCTIONS

Mnemonic	Octal Code	Execution Time (μsec)	Description
Memory Reference Instructions			
AND	02	3.2	Logical AND of addressed memory location to accumulator A.
XOR	04	3.2	Exclusive OR of addressed memory location to accumulator A.
IOR	06	3.2	Inclusive OR of addressed memory location to accumulator A.
JSB	03	3.2	Jump to subroutine. The current value of the program counter is stored in the addressed main memory location, and control passes to the location following that in which the program counter is stored.
JMP	05	1.6	Jump unconditionally.
ISZ	07	3.6	Increment the addressed memory location and skip the next instruction if the result is zero.
ADA	10	3.2	Add the contents of the addressed main memory location to accumulator A or B.
ADB	11		
CPA	12	3.2	Compare the contents of the addressed main memory location with those of accumulator A or B and skip the next instruction if they are unequal.
CPB	13		
LDA	14	3.2	Load the contents of the addressed main memory location into accumulator A or B.
LDB	15		
STA	16	3.2	Store the contents of accumulator A or B into the addressed main memory location.
STB	17		
Overflow Instructions			
STO	1	1.6	Set overflow bit.
CLO	1	1.6	Clear overflow bit.
SOC	2	1.6	Skip next instruction if overflow bit is clear.
SOS	3	1.6	Skip next instruction if overflow bit is set.

TABLE I. (Contd.)

Mnemonic	Octal Code	Execution Time (μsec)	Description
Input/Output Instructions			
HLT	0	2.0	Halt program.
STF	1	2.0	Set flag bit of selected I/O channel.
CLF	1	2.0	Clear flag bit of selected I/O channel.
SFC	2	2.0	Skip next instruction if flag bit of selected I/O channel is clear.
SFS	3	2.0	Skip next instruction if flag bit of selected I/O channel is set.
MIA, MIB	4	2.0	Merge ("OR") selected I/O channel into accumulator A or B.
LIA, LIB	5	2.0	Load selected I/O channel into accumulator A or B.
OTA, OTB	6	2.0	Output accumulator A or B to selected I/O channel.
OTC	7	2.0	Set control bit of selected I/O channel.
CLC	7	2.0	Clear control bit of selected I/O channel.
Shift-Rotate Instructions			
NOP	00	*	No operation.
CLE	**	*	Clear E (Extend).
SLA, SLB	**	*	Skip if least significant bit of accumulator A or B is zero.
ALS, BLS	10	*	Shift accumulator A or B left one bit.
ARS, BRS	11	*	Shift accumulator A or B right one bit.
RAL, RBL	12	*	Rotate accumulator A or B left one bit.
RAR, RBR	13	*	Rotate accumulator A or B right one bit.
ALR, BLR	14	*	Shift accumulator A or B left one bit, clearing the sign bit.
ERA, ERB	15	*	Rotate E and accumulator A or B right one bit.
ELA, ELB	16	*	Rotate E and accumulator A or B left one bit.
ALF, BLF	17	*	Rotate accumulator A or B left four bits.

TABLE I. (Contd.)

Mnemonic	Octal Code	Execution Time (μsec)	Description
Alter-Skip Instruction*			
CLA, CLB	1	*	Clear accumulator A or B.
CMA, CMB	2	*	Form one's complement of accumulator A or B.
CCA, CCB	3	*	Clear and complement accumulator A or B, forming-1.
CLE	1	*	Clear E (Extend).
CME	2	*	Complement E.
CCE	3	*	Clear and complement E, setting E.
SEZ	**	*	Skip next instruction if E is zero.
SSA, SSB	**	*	Skip next instruction if sign of accumulator A or B is zero (positive).
SLA, SLB	**	*	Skip next instruction if least significant bit of accumulator A or B is zero.
INA, INB	**	*	Increment accumulator A or B by one.
SZA, SZB	**	*	Skip next instruction if accumulator A or B is zero.
RSS	**	*	Reverse sense of next instruction skip set by remainder of this microprogrammed instruction.

Notes:

* The operations within either the shift-rotate group or the alter-skip group can be combined by microinstructions in the combinations allowed by Table III. Each permissible microprogrammed combination has an execution time of 1.6 microseconds.

** These instructions are not executed as the result of particular operation code settings but by the setting of bits explicit to each in the relevant instruction format.

The main memory is divided into 1,024-word segments called pages. Each main memory reference instruction contains a memory address in a 10-bit field, and a single-bit flag indicates the current or base page. Thus, the only main memory locations that can be addressed directly from within an instruction are those in the current page or in the first 1,024 words of main memory. Access to the whole of main memory is provided by not more than two levels of indirect addressing. (The multiply, divide, double-load and double-store instructions provided by the optional EAU are an exception to these rules; they are in a two-word instruction format with a full word for the main memory address and hence can address the whole of main memory directly.)

No index registers are provided, but an instruction is provided which increments a main memory location and skips the next instruction if the result is zero, providing a method of loop control.

The register reference instructions, which address registers A, B and E only, fall into two groups called the shift-rotate group and the alter-skip group. Instructions in either group can be combined, subject to certain restrictions, to provide compound manipulations to be executed in a single instruction-time; HP calls this microprogramming. Up to four operations from the

TABLE II. HP 2116C EXTENDED ARITHMETIC UNIT (OPTIONAL) INSTRUCTIONS

Mnemonic	Octal Code	Execution Time (μsec)	Description
	Single-Word Format		
ASR	10	*	Arithmetic right shift N places of accumulators A and B together ($1 \leq N \leq 16$).
ASL	00	*	Arithmetic left shift N places of accumulators A and B together ($1 \leq N \leq 16$).
RRR	11	*	Rotate accumulators A and B together N places right ($1 \leq N \leq 16$).
RRL	01	*	Rotate accumulators A and B together N places left ($1 \leq N \leq 16$).
LSR	10	*	Logical shift of accumulators A and B together N places right ($1 \leq N \leq 16$).
LSL	00	*	Logical shift of accumulators A and B together N places left ($1 \leq N \leq 16$).
	Double-Word Format		
MPY	02	19	Multiply the number in accumulator A by the contents of the addressed main memory location, leaving the double-length product in accumulators A and B.
DIV	04	21	Divide the double-word in accumulators A and B by the contents of the addressed main memory location.
DLD	42	6.4	Double load of two consecutive main memory locations, starting with the one addressed, into accumulators A and B.
DST	44	6.4	Double store of accumulators A and B in two consecutive main memory locations, starting with the location addressed.

* Shift-rotate execution times —

Number of places shifted	Execution time (μsec)
1 to 4	3.2
5 to 8	4.8
9 to 12	6.4
13 to 16	8.0

shift-rotate group can be combined, and up to eight operations from the alter-skip group. As an example of microprogramming, the shift-rotate instructions to rotate A one bit right, test the least significant bit of A, and rotate A one bit left can be combined in a single instruction to provide for the following instruction to be skipped if bit one of A is a zero. The condition causing the skip can be reversed by the additional use of the reverse skip sense instruction. The rules for combining instructions to form microprogrammed instructions are summarized in Table III. Note that register A or B can be rotated eight bits left in a single microprogrammed instruction; this facility has been included for use in character packing and unpacking operations.

The interrupt facility provides for the automatic passing of control to a location address that is dependent on the particular interrupt taken. Sixty locations are wired for use as interrupt locations. The highest interrupt priority is reserved for the optional power failure interrupt, and the next highest is reserved for the optional memory parity failure interrupt and for the optional memory protect violation interrupt. Two further interrupt levels are reserved for the two optional direct memory access (DMA) channels, and the remaining 56 interrupt levels are

TABLE III. PERMISSIBLE COMBINATIONS OF MICROINSTRUCTIONS*

Shift-Rotate Group			
ALS ARS RAL RAR ALR ERA ELA ALF BLS BRS RBL RBR BLR ERB ELB BLF	CLE CLE	SLA SLB	ALS ARS RAL RAR ALR ERA ELA ALF BLS BRS RBL RBR BLR ERB ELB BLF

Alter-Skip Group							
CLA CMA CCA CLB CMB CCB	SEZ SEZ	CLE CME CCE CLE SME CCE	SSA SSB	SLA SLB	INA INB	SZA SZB	RSS RSS

* Any instruction is permissible that is formed by taking microinstructions from different columns of the same instruction group.

available to peripheral devices. It should be noted that although 56 interrupt levels are available for peripheral devices, the basic HP 2116C computer contains the prewired slots to support only 16 of these levels; facilities for 32 more levels can be added optionally.

When an interrupt occurs, control passes to the associated interrupt location. This location generally contains a subroutine jump (JSB) instruction to store the program counter, giving the address at which interruption occurred. Further interrupts are inhibited for one instruction after an interrupt is taken; otherwise, interrupts are taken in the priority defined by the order in which the interrupt locations are assigned. This order can be altered by reordering printed-circuit cards in the central processor cabinet. Individual interrupts, all interrupts of lower priority than a specified level, or the whole interrupt system can be enabled or disabled by program.

Processor options available include the power fail interrupt option, which is wired to the highest interrupt priority, and the memory parity check interrupt option. There is a memory protect option, which consists of a printed-circuit card containing a special register to hold a "fence address." The fence address is changeable by using output instructions, and attempts to change the contents of a memory location with a lower address than the current value of the fence cause an interrupt. The extended arithmetic unit option provides hardware multiplication and division instructions and a range of shift, rotate, double-load, and double-store instructions that act on accumulators A and B together.

.123 Console

Table IV lists the 2116C console buttons, switches, and displays.

TABLE IV. CONSOLE DISPLAYS AND PUSHBUTTON CONTROLS

Control/Display	Function
T register display	Shows the information last transferred into or out of main memory.
P register display	Shows the address of the next instruction to be fetched from main memory.
M register display	Shows the address of the next main memory location to be accessed.
A register display	Shows the current contents of accumulator A.
B register display	Shows the current contents of accumulator B.
PRESET pushbutton	Performs CLC and STF for all input/output devices.
RUN pushbutton	Starts operation at the current state of the registers.
HALT pushbutton	Stops computer operation.
LOAD MEMORY pushbutton	Transfers the setting of the operator's switches into main memory at the address given by the current setting of the M register.
LOAD A pushbutton	Transfers the current setting of the operator's switches into accumulator A.
LOAD B pushbutton	Transfers the current setting of the operator's switches into accumulator B.
LOAD ADDRESS pushbutton	Transfers the current setting of the operator's switches into the P register and the M register.
DISPLAY MEMORY pushbutton	Displays the contents of the main memory location addressed by the M register in the T register and increments of the P register.
SINGLE CYCLE pushbutton	Steps the program one machine cycle.
LOADER switch	Has two positions — "protected" and "enabled." When this switch is in the protected position, the top 64 words of memory are protected and cannot be accessed by a program in any way; the switch must be in the enabled position before the loader stored in these locations can be used.

.125 Instruction List

A list of the HP 2116C basic instructions is given in Table I and the extra instructions provided by the optional EAU are listed in Table II. Table III summarizes the rules for the combination of microinstructions.

.126 Data Codes

The data codes used by input/output devices for the HP 2116C are summarized in the Input/Output section, S512:071.

.13 Availability: . . . . . 6-8 weeks.

.14 First Delivery: . . . . . December 1970.

.2 PROCESSING FACILITIES

.21 Operations and Operands

	Operand and Variation	Provision	Radix	Size
.211	Fixed point —			
	Add:	automatic	binary	1 word.
	Subtract:	programmed	binary	1 word.
	Multiply:	subroutine*	binary	1-word operands; 2-word result.
	Divide:	subroutine*	binary	2-word dividend; 1-word divisor, quotient, and remainder.
.212	Floating point —			
	Arithmetic operations:	subroutine	binary	2-word operands and results.
.213	Boolean —			
	AND:	automatic	binary	1 word (16 bits).
	Exclusive OR:	automatic	binary	1 word (16 bits).
	Inclusive OR:	automatic	binary	1 word (16 bits).
.214	Compare:	automatic	binary	1 word (16 bits).

* Automatic if EAU option is included.

.215	Code translation:	no direct provision.
.216	Radix conversion:	no direct provision.
.217	Edit format:	no direct provision.
.218	Table lookup:	no direct provision.

.22 Special Cases of Operands

.221	Negative numbers:	high-order bit is sign; form of negative numbers is two's complement.
.222	Zero:	1 form only (all zeroes).
.223	Operand size determination:	fixed at 1 word.

.23 Instruction Formats

.231 Instruction structure: . . . . . 1 word.

.232 Instruction layout —

Memory Reference Instructions:

Part	D/I	Instruction	Z/C	Memory Address
Size (bits)	I	4	1	10

Register Reference Instructions, Shift-Rotate group:

Part	Class	A/B	SR	Not Used	First Instruction	CLE	Not Used	SLA/B	Second Instruction
Size (bits)	4	1	1	1	3	1	1	1	3

Register Reference Instructions, Alter-Skip group:

Part	Class	A/B	AS	First Instruction	Second Instruction	SEZ	SSA/B	SLA/B	INA/B	SZA/B	RSS
Size (bits)	4	1	1	2	2	1	1	1	1	1	1

Input-Output Instructions:

Part	Class	A/B	MAC	H/C	Instruction	Select Code
Size (bits)	4	1	1	1	3	6

EAU Instructions (single-word):

Part	Class	Instruction	L	A	Count
Size (bits)	4	6	1	1	4

EAU Instructions (double-word):

Part	Class	Instruction	Zero	Memory Address
Size (bits)	4	6	6	16

.233 Instruction parts —

Memory Reference Instructions

D/I: . . . . . specifies direct or indirect addressing.

Instruction: . . . . . specifies operation to be performed.

Z/C: . . . . . specifies zero page or current page.

Memory address: . . . . . specifies main memory address.

Register Reference Instructions, Shift-Rotate group

Class: . . . . . set to 0000 to indicate a register reference instruction.

A/B: . . . . . specifies the accumulator to which the instruction refers.

SR: . . . . . set to 0 to indicate shift-rotate group.

First instruction: ..... first microinstruction for execution, selected from the shift-rotate group of instructions whose octal codes are quoted in Table I.

CLE: ..... set to 1 if the CLE (clear E) operation is to be included as a microinstruction.

SLA/B: ..... set to 1 if the SLA/B (skip if least significant bit of accumulator A or B is 0) operation is to be included as a microinstruction.

Second instruction: ..... second microinstruction for execution, selected from the shift-rotate group of instructions whose octal codes are quoted in Table I.

Note: The microinstructions specified are executed in the order in which they are specified from left to right in the instruction word. References to accumulators A and B cannot be mixed in the same instruction, the accumulator concerned being indicated by the setting of the A/B bit in the instruction format.

Register Reference Instructions, Alter-Skip group

Class: ..... set to 0 to indicate register reference instruction.

A/B: ..... specifies the accumulator to which the instruction refers.

AS: ..... set to 1 to indicate alter-skip group.

First instruction: ..... first microinstruction for execution, selected from CLA, CLB, CMA, CMB, CCA and CCB listed in Table I.

Second instruction: ..... second microinstruction for execution, selected from CLE, CME and CCE listed in Table I.

SEZ: ..... set to 1 if the SEZ (skip if E register is 0) operation is to be included as a microinstruction.

SSA/B: ..... set to 1 if the SSA/B (skip next instruction if accumulator A or B has a 0 sign bit) operation is to be included as a microinstruction.

SLA/B: ..... set to 1 if the SLA/B (skip next instruction if the least significant bit of accumulator A or B is 0) operation is to be included as a microinstruction.

INA/B: ..... set to 1 if the INA/B (increment accumulator A or B by one) operation is to be included as a microinstruction.

SZA/B: ..... set to 1 if the SZA/B (skip next instruction if accumulator A or B is 0) operation is to be included as a microinstruction.

RSS: ..... set to 1 if the RSS (reverse skip sense) operation is to be included as a microinstruction, reversing the sense of the skip condition set up by the remainder of the current instruction.

Note: The microinstructions specified are executed in the order in which they are specified in the instruction word. References to accumulators A and B cannot be mixed in the same instruction, the accumulator concerned being indicated by the setting of the A/B bit in the instruction format.

Input/Output Instructions

Class: ..... set to 1000 to indicate input/output or EAU instruction.

A/B: . . . . . specifies the accumulator to which the instruction refers.
MAC: . . . . . set to 1 to identify this as an input/output instruction.
H/C: . . . . . specifies whether the flag flip-flop of the selected device is to be held or cleared after instruction execution.
Instruction: . . . . . specifies the input/output operation to be performed.
Select code: . . . . . selects the input/output device or function to which this instruction refers.

EAU Instructions (single-word)
Class: . . . . . set to 1000 to indicate input/output or EAU instruction.
Instruction: . . . . . specifies the operation to be performed.
L: . . . . . set to 1 for a left shift of rotate and to 0 otherwise.
A: . . . . . set to 1 for an arithmetic shift and to 0 otherwise.
Count: . . . . . specifies the number of positions to be shifted or rotated.

EAU Instructions (double-word)
Class: . . . . . set to 1000 to indicate input/output or EAU instruction.
Instruction: . . . . . specifies the operation to be performed.
Zero: . . . . . set to all zeroes.
Memory address: . . . . . set to the main memory address for this instruction.

.234 Basic address structure: . . . . . 1-address.
.235 Literals: . . . . . none.
.236 Directly addressed operands
.2361 Internal storage type —
Minimum size: . . . . . one 16-bit word.
Maximum size: . . . . . one 16-bit word.
Volume accessible: . . . . . the first 1,024-word page of core storage or the page containing the instruction.

.2362 Increased address capacity —

Method	Volume accessible
Indirect addressing:	all of core store (8,192 words maximum).

.237 Addressing indexing: . . . . . none.
.238 Indirect addressing —
.2381 Recursive: . . . . . yes; any number of levels.
.2382 Designation: . . . . . indirect flag (D/I) in instruction; high-order bit in subsequent locations.
.2383 Control: . . . . . last indirect address has high-order bit set to 0.
.2384 Indexing with indirect addressing: . . . no.
.239 Stepping: . . . . . one stepping instruction, ISZ, which increments a core location by one and causes skipping of the following instruction if the result is 0.
.2391 Specification of increment: . . . . . plus one, implied by ISZ instruction.
.2392 Increment sign: . . . . . plus.
.2393 Size of increment: . . . . . 1.
.2394 End value: . . . . . 0, implied by ISZ instruction.

.24 Special Processor Storage

Category of Storage	Number of Locations	Size in Bits	Program Usage
T register*	1	16	memory data register; holds a copy of the last word of information transferred to or from main memory.
P register*	1	15	program counter; holds the address of the next instruction to be fetched from main memory.
M register*	1	16	memory address register; holds the memory address used for the last main memory access.
A register	1	16	accumulator; can also be addressed as main memory location 0. Holds least significant half of double-word numbers.
B register	1	16	accumulator; can also be addressed as main memory location 1. Holds most significant half of double-word numbers. The same single-word operations are available for both accumulators except that boolean operation instructions are provided only for register A.
E register	1	1	extend register; used for communication of a single-bit setting between the A and B registers in rotate instructions, or to indicate a carry out of the sign bit position after an add or an increment instruction.
Overflow (OV)	1	1	overflow; used to indicate an arithmetic overflow in the A or B register.
Core memory	1	16	return point for power fail interrupt, the interrupt of highest priority.
Core memory	1	16	return point for memory parity fail interrupt and memory protect interrupt (both optional), the interrupts of second highest priority.
Core memory	2	16	return points for two optional interrupt levels available with the DMA feature.
Core memory	56	16	return points for up to 56 levels of peripheral device interrupts, arranged in order of decreasing priority.
Core memory	64	16	the top 64 words of memory are generally used to hold the loader and may be protected by setting the Loader switch on the console to the "protected" position.

* The T, M and P registers are not accessible by instructions, but their current settings are displayed by rows of lamps on the console. The P register setting is loaded into main memory by a subroutine jump (JSB) instruction.

.3 SEQUENCE CONTROL FACILITIES

.31 Instruction Sequencing:	sequential; instructions that test a condition cause the following instruction to be skipped if the condition is satisfied.
.32 Lookahead:	none.
.33 Interruption	
.331 Possible causes —	
Internal interrupts (two priority positions): . .	power failure; memory parity and/or memory protect failure if options chosen.
DMA interrupts (two positions):	two interrupt positions reserved for the use of the two optional DMA channels in reporting completion of a transfer.
Peripheral device interrupts (56 positions): . .	interrupt positions reserved for the use of peripheral devices, arranged in order of decreasing priority. Standard use is in reporting completion of a transfer.

Note that when the memory protect option is used, memory protect interrupts are also caused by:

- An attempt to execute a HALT instruction.
- An attempt to execute an input/output instruction other than LIA/B 1 or OTA/B 1.
- The specification of more than two levels of indirect addressing.
- An attempt to execute a JSB or a JMP instruction to a destination address below the "fence" register.

It should be noted that both the memory protect and the memory parity error interrupts pass control to location 5. The subsequent execution of an LIA/B 5 instruction causes the address of the offending memory location to be read from a buffer register. A single-bit flag associated with this address indicates whether the interrupt was caused by a parity error or a memory protect violation.

.332 Control by routine:	interrupts from a particular device can be enabled or disabled by program instructions in conjunction with the control flip-flop for the particular device; the flag flip-flop for a device can be used to inhibit interrupts from devices of lower interrupt priority; whole interrupt system can be enabled or disabled with one instruction. Priority levels are not changeable by instruction but can be changed easily by rearranging plug-in boards in the processor housing.
.333 Operator control:	none.
.335 Interruption process —	
Disabling interruption:	further interrupts are inhibited until the instruction in the interrupt location has been fully executed except that instructions other than jump instructions pass through only two indirect addressing levels before interrupts are reenabled.

Registers saved: ..... none; conventionally a subroutine jump (JSB) instruction is used in the interrupt location which preserves the address of the point at which the interrupt was taken.
Destination: ..... one of 60 fixed locations depending on the origin of the interrupt.

Note: a more detailed description of the interrupt system, and of the way in which it interfaces with input/output devices, is given in the Input/Output section.

.34 Multiprogramming

.341 Method of control: ..... the interrupt system and own coding.
.342 Maximum number of programs: ..... depends on the user's coding and the configuration available.
.343 Precedence rules: ..... depends on the user's coding.
.344 Program protection: ..... none.

.35 Multisequencing: ..... none.

.4 PROCESSOR SPEEDS

.41 Instruction Times in Microseconds

Note: EAU refers to the optional extended arithmetic unit.

.411 Fixed point —
Add: ..... 3.2.
Subtract: ..... 4.8 (2 instructions).
Multiply: ..... 150*; 19 with EAU.
Divide: ..... 310*; 21 with EAU.

* By subroutine.

.412 Floating point —
Add: 900*
Subtract: 900*
Multiply: ..... 750; 344* with EAU.
Divide: ..... 1500*; 448* with EAU.

* By subroutine.

.413 Additional allowance for —
Indexing: ..... none provided.
Indirect addressing: ..... 1.6 μsec per level.
Recomplementing: ..... 0.
.414 Control —
Branch: ..... 1.6.
Microprogrammed register test and skip: ... 1.6.
Compare and skip: ..... 3.2.
.415 Counter control —
Step and test (skip): ..... 3.2.
.416 Edit: ..... no direct provision.
.417 Convert: ..... no direct provision.

.418 Shift: ..... short shifts are microprogrammed, and any two of the shift operations given in the shift-rotate group in Table I can be microprogrammed together for joint execution in one shift-rotate group instruction time of 1.6 microseconds. Double shifts of accumulators A and B together are provided by the extended arithmetic unit option, and details of these are given in Table II.

.42 Processor Performance in Microseconds

.421 For random addresses —

	Fixed point	Floating point (by subroutine)
c = a + b:	9.6	912.8
b = a + b:	9.6	912.8
Sum N items:	3.2	900.0
c = ab:	156.4; 25.6*	762.8; 356.8*
c = a/b:	318.0; 28.8*	1512.8; 460.8*

.422 For arrays of data —

$c_i = a_i + b_j$:	36.4	1181.5; 946.0*
$b_j = a_i + b_j$:	36.4	1181.5; 946.0*
Sum N items:	13.6	914.0
$c = c + a_i b_j$:	181.2; 50.4*	1996.2; 1282.8*

* With optional extended arithmetic unit (EAU).

.423 Branch based on comparison —	
Numeric or alphabetic data:	32.0
.424 Switching —	
Unchecked:	11.2
Checked:	30.4
List search:	28.8 + 19.0N
.426 Table lookup, per comparison —	
For a match:	13.6
For least or greatest:	28.0
For interpolation point:	20.0
.427 Bit indicators —	
Set bit in separate location:	6.4
Set bit in pattern:	9.6
Test bit in separate location:	6.4
Test bit in pattern:	8.8
Test AND for B bits:	10.4
Test OR for B bits:	8.8
.428 Moving —	
Straight line coding:	6.4 per word.
Programmed loop:	22.0 per word.

.5 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Overflow:	check	set testable indicator.
Underflow (float-pt):	check	set testable indicator; return zero.
Zero divisor:	check	set testable indicator.
Invalid data:	none.	
Invalid operation:	none	undefined machine state; result will depend on the invalid code concerned.
Invalid address:	none	address wraparound.
Receipt of data:	none.	
Dispatch of data:	none.	

.1 GENERAL

.11 Identity: . . . . . see Table I.

.13 Availability: . . . . . see Table I.

.14 First Delivery: . . . . . see Table I.

.15 Input/Output Techniques

.151 Input/Output Channels

All peripheral devices are connected to the computer via standard input/output channels, and each of the standard channels is uniquely associated with a particular interrupt location in the main store. Although 48 interrupt locations are available for standard input/output channels, the basic HP 2116C contains only enough prewired slots for 16. Additional input/output channels are provided by two optional extender modules — the HP 2151A Extender Module provides prewired slots for the use of 16 extra channels while the HP 2150B Extender Module provides prewired slots for 32 extra channels.

The peripheral device on an input/output channel is connected to the computer through a standard input/output interface card. This is a plug-in printed circuit card, which consists of a buffer up to 16 bits long for the transfer of data, a flag flip-flop controlling interrupts originating from the device connected to the interface, and a control flip-flop, which enables the peripheral device to perform its input or output operation and also controls the interrupt capability of the device. The interrupt location to which each input/output interface is connected, and its consequent interrupt priority, is determined only by the position each interface card occupies in a rack in the main computer cabinet; the interrupt locations used need not be contiguous provided a special "jumper" card is inserted in each location that is skipped.

In general, one device is connected to each input/output channel, but devices such as magnetic tape units and discs for which more than one operation can be programmed require the use of two adjacent input/output channels; one of these is used to transfer control information and the other is used to transfer data.

Data is transferred between the input/output interface and the computer one buffer full at a time; instructions are provided to pass information between either accumulator and the buffer in the interface. The size of the buffer depends on the particular peripheral device concerned, but it is generally 8 or 16 bits. Transfers between the buffer and the peripheral device are initiated by issuing a Set Control Flag (STC) command. On completion of a transfer, the device controller sets the flag flip-flop on the input/output interface card, causing an interrupt. The total data throughput attainable by this method depends on the length of the interrupt servicing routines, but a typical overall limit is about 60,000 transfers per second.

Direct memory access (DMA) is an optional feature providing autonomous block transfer facilities working not through the standard input/output channel interface but by direct "stealing" of main memory cycles. The feature provides two direct memory access channels capable of a combined transfer rate as fast as the cycling rate of main memory (625,000 words per second). Two high-priority interrupt levels are reserved for the DMA channels. There is no hardware connection between the DMA channels and particular peripheral devices, and these channels can be used to address any device on a standard input/output channel. DMA is a required feature if drum or disc memory units or 9-channel magnetic tape units are used.

Transfers taking place via the DMA feature are specified to the DMA by a control word. The setting of the control word defines the device concerned in the transfer, the state in which the control flip-flop in the interface is to be left between each byte of the transfer and after the end of the transfer, and also the data format, whether the information transferred to and from core store is packed two bytes to a word. While the transfer is taking place, registers within the DMA hardware maintain the number of words remaining to be transferred and the next memory address to be used; these registers also require initialization before a DMA transfer is started.

TABLE I. HP 2116C INPUT/OUTPUT UNITS

Type of Input/Output	Peripheral Device	Rated Speed	Controller (1)	Availability, weeks, (2)	First Delivery
Console Typewriter	HP 2752A Teletypewriter (modified Teletype ASR 33)	10 char/sec	12531B	6-12	12/66
	HP 2754B Heavy-Duty Teletypewriter (modified Teletype ASR 35)	10 char/sec	12531B	6-12	12/66
Punched Tape	HP 2752A Teletypewriter (modified Teletype ASR 33)	10 char/sec	12531B	6-12	12/66
	HP 2754B Heavy-Duty Teletypewriter (modified Teletype ASR 35)	10 char/sec	12531B	6-12	12/66
	HP 2748A Punched Tape Reader	500 char/sec	12597A-002	6-12	
	HP 2753A Tape Punch	120 char/sec	12597A-003	6-12	
Punched Card	HP 2891A Card Reader	1,000 cards/min	12882A	6-12	
	HP 2761A-007 Optical Mark and Card Reader	200 cards/min	12602A	6-12	
Printer	HP 2778A Line Printer (120-col line)	300 lines/min	12617A	6-12	
	HP 2767A Line Printer (80-col line)	300-1,100 lines/min	12653A	—	—
	HP 2778A-001 Line Printer (132-col line)	300 lines/min	12617A	—	—
Magnetic Tape	HP 2020B 7-track Magnetic Tape Unit	30 ips	12538B	6-12	1/68
	HP 7970A-200 9-track Magnetic Tape Unit	25 ips	13181A-001	6-12	
	HP 7970A-202 9-track Magnetic Tape Unit	37.5 ips	13181A	—	—
	HP 3030G Magnetic Tape Unit	75 ips	12559A	—	—
Digital Plotter	Interface for 563 or 565 CalComp Plotter		12560A		
Data Communications	Interface to asynchronous dataphone		12587A	6-12	
	Interface for synchronous send and receive		12618A	6-12	
	Interface for synchronous receive only		12621A	6-12	
	Interface for synchronous transmit only		12622A	6-12	
	HP 2600A CRT Keyboard Terminal	10-218 char/sec	12880A	6-12	
	7200A Graph Plotter				
	2570A Coupler/Controller				

TABLE I. (Contd.)

Type of Input/Output	Peripheral Device	Rated Speed	Controller (1)	Availability, weeks (2)	First Delivery
Other	HP 12554A General-Purpose Duplex Register (16-bit)		Self-contained	6-12	4/68
	HP 12551B Relay Output Register (16 form-A contacts)		Self-contained	6-12	3/68
	HP 12555A Two D/A Converter Channels (8 bits/channel)		Self-contained	6-12	11/67
	HP 12566A Microcircuit Interface Kit (16 bits)		Self-contained	6-12	8/68
	HP 12539A Time Base Generator (100 μsec to 1,000-sec intervals)		Self-contained	6-12	3/67
	HP 12597A General-Purpose Duplex Register (8-bit)		Self-contained	6-12	5/69

Notes:

(1) Hewlett-Packard supplies I/O devices in interface kits that include cabinets, power supplies, the device, and the interface to an I/O channel. The numbers listed are the model numbers of the interface kits.

(2) Hewlett-Packard delivers complete systems in 6 to 12 weeks. Minimum delivery time for in-stock items is about 2-1/2 weeks.

.152 Input/Output Procedure

The HP 2116C input/output instructions are listed in Section :051.125, and their layout is described in Section :051.232. Instructions are provided to output the contents of either accumulator to the data buffer on the input/output interface card, and to load either accumulator from this buffer after an input operation. Further input/output instructions provide the setting, clearing, and testing of the flag and control flip-flops associated with each input/output interface. Each input/output instruction includes a six-bit select code field, which selects the input/output interface addressed by the instruction by referring to its interrupt level number. Fifty-six of the 64 possible select code values are available to address input/output interfaces, the other values select special functions concerned with input/output, the overflow register, and the direct memory access channels. A list of the select code assignments is given in Table II.

Computer control of input/output operations is exercised by means of the instructions which set, test, and clear the flag and control flip-flops in the standard input/output interface. An external device is commanded to perform its input/output operation by setting the control flip-flop in the input/output interface, and interrupt signals originating from the device are passed on to the computer only if the control flip-flop in the interface is set. Thus, the control flip-flop turns on the device connected to the interface.

The flag flip-flop is set by a signal from an external device when the device has completed an operation; it can also be set explicitly by the Set Flag instruction. Once it is set, it remains set until it is cleared, either by an explicit Clear Flag instruction or by the issuing of an

input/output instruction with the Clear Flag bit set in the instruction format. Provided the control flip-flop for the device is set and no device of higher priority has its flag set, the setting of the flag causes an interrupt in the processor, and all interrupts originating from devices of lower priority are inhibited until the flag is cleared. Successive interrupts for one device can occur on receipt of a flag signal without executing a Clear Flag instruction, thus making it possible to inhibit lower priority devices indefinitely until a desired number of high-priority transfers is completed. The flag can be set and cleared even if its interrupt capability is inhibited or disabled, and can be tested by Skip If Flag Set or Skip If Flag Clear instructions.

TABLE II. SELECT CODE ASSIGNMENTS

Select Code (Octal)	Interrupt Location (Octal)	ASSIGNMENT
00	None	STF Ø turns interrupt system on; CLF Ø turns interrupt system off.
01	None	Overflow Register: STO, CLO, SOC, SOS
02	None	Initialize DMA Channel 1 (select code 6)
03	None	Initialize DMA Channel 2 (select code 7)
04	00004	Power Fail Interrupt Interrupt Source Identification (LIA/B 4 = select code of last interrupting device)
05	00005	Memory Protect Interrupt Parity Error Interrupt (LIA/B 5 = address of offending location. If bit 15 = "1," parity error interrupt. If bit 15 = "0," memory protect interrupt.)
06	00006	DMA Channel 1 Completion Interrupt
07	00007	DMA Channel 2 Completion Interrupt
10 thru 77	00010 thru 00077	I/O Device, highest priority through I/O Device, lowest priority

The operations performed by the program when it receives an interrupt originating from a device being used via a standard input/output channel to input data can be summarized as follows (the output sequence is similar):

- A command is sent to the device by execution of a Set Control flip-flop instruction, usually accompanied by a Clear Flag instruction.
- The device reads from the external medium into the buffer on the interface card.
- When the transfer is completed, the device passes a flag signal to the interface card.
- The flag flip-flop is set, and an interrupt signal is passed from the interface card to the computer.

- The interrupt causes entry to an interrupt service routine, which unloads the data just received from the buffer in the interface to one of the accumulators.

Transfers using one of the optional DMA channels must be preceded by instructions to set up the control word, memory address register, and word count register for the DMA channel concerned. As shown in Table II, two select codes are reserved for each of the DMA channels — one of these is used for initialization, and the initial memory address and word count register settings are passed to this channel with Output from Accumulator instructions. An OTA/B instruction to a DMA initialization channel with its control flip-flop clear transfers an initial memory address register setting, while the same instruction with the control flip-flop of the channel set transfers an initial word count register setting. The sign bit of the memory address register setting must be a one for a transfer into main memory and a zero otherwise. The initial setting of the word count register is the two's complement of the number of words of data to be transferred.

The control word setting for the use of a DMA channel is transferred to the DMA prior to the transfer. Its setting specifies the select code of the device to be used, an indication of whether the information in memory is packed two bytes to a word, and markers specifying the setting and clearing of the control flip-flop of the device while it is being used. Unlike the memory address register and word count register settings, the control word setting is unchanged by the transfer; hence it need not be altered except when the DMA is switched to address another device.

The select codes to be used for the DMA initialization channel and the DMA completion interrupt channel depend on the DMA used and are given in Table II. The operations required to start a DMA transfer on a channel not previously addressed via this DMA can now be summarized as follows:

- The control word setting is output from an accumulator using an OTA/B instruction addressing the DMA completion interrupt channel.
- The control flip-flop of the DMA initialization channel is cleared and the initial memory address register setting is transferred to it from an accumulator using an OTA/B instruction.
- The control flip-flop of the DMA initialization channel is set, and the initial word count register setting is transferred to it from an accumulator using an OTA/B instruction.
- The control bit of the peripheral device is set to start the transfer.
- The control bit of the DMA completion interrupt channel is set to activate the DMA.

.153 Simultaneous Operations

Since there are two DMA channels, only two devices can use the DMA at a time.

All devices transferring data to or from the accumulator can operate simultaneously.

The 2116C places no restrictions on input/output simultaneity apart from those imposed by the overall throughput capacity of the system. Input/output operations proceed concurrently with computation, the normal input/output channels causing an interrupt after each data transfer and the DMA channel accessing the main store on a cycle-stealing basis.

.154 Input/Output Interface

Each of the standard input/output devices is connected to an input/output channel via an interface card which supplies an external interface tailored to the requirements of the device concerned. The interface card can contain up to 16 or more buffer flip-flops for temporary storage of data to be transferred to the computer or device. The number of buffer storage flip-flops on the card and the other logic circuitry on the card are determined by the device connected to the card.

A range of general-purpose interface cards is available from Hewlett-Packard for users who wish to connect their own, nonstandard input/output devices. These consist of the HP 12554A General-Purpose Duplex Register and the HP 12566 series of microcircuit interfaces, which are discussed in Paragraph .167. Each of these interface cards provides 16 input and 16 output lines, which are fully buffered on the card. The HP 12566A has 5-volt logic levels, and the HP 12554A has 12-volt logic levels.

.16 Input/Output Devices

For each peripheral device, Hewlett-Packard supplies an interface kit which consists of:

- One or more printed circuit cards that fit into input/output channel positions in the computer housing.
- A connecting cable.
- The appropriate software driver packages, which usually include both a System Input/Output (SIO) driver for use without interrupt control and a Basic Control System (BCS) driver for input/output with interrupt control.

For OEM devices such as the California Computer Products (CalComp) plotter, Hewlett-Packard supplies the interface kit only. A number of general-purpose interface kits (described in Paragraph .167) are also available to provide interfaces for user-supplied measuring equipment.

.161 Console Typewriter Input/Output

Console input/output and paper tape facilities are provided by the HP 2752A teletypewriter, which is a modified Teletype ASR 33. The HP 2754B is an alternative heavy-duty version of the HP 2752A; — it is a modified Teletype ASR 35. Both units perform all printing, reading, and punching operations at a maximum speed of 10 characters per second using an eight-bit ASCII standard character code. In the heavy-duty HP 2754B, either or both of the output devices (paper tape punch and printer) can be selected by program for output, but in the HP 2752A, the paper tape punch cannot be operated independently of the printer.

.162 Punched Tape Input/Output

Besides the paper tape facilities provided by the teletypewriters, the HP 2748A Punched Tape Reader and the HP 2753A Tape Punch are available.

The HP 2737A Punched Tape Reader is a photoelectric tape reader that reads paper tape punched with any 5- through 8-channel code at a speed of 500 characters per second. No code translation or tape spooling facilities are provided in the basic model. The HP 2758A has automatic spooling capability. The unit has a starting time of 6 milliseconds and a stop time of 1 millisecond. This rapid stop time enables the unit to stop on a single character.

The HP 2753A Tape Punch punches 5-, 7-, or 8-channel tape at 120 characters per second. It includes a supply tape spooler, which holds approximately 1,000 feet of tape. There are no provisions for code translation.

.163 Punched Card Input/Output

Hewlett-Packard supplies the 12882A interface kit for using an HP 2891A Card Reader with the HP 2116C. This device reads standard 80-column cards at a speed of 1,000 cards per minute. No provision is made for code translation; the device transfers a binary image of each card column. The input and output hoppers each have a capacity of 1,000 cards. The HP 2761A-007 is a Hewlett-Packard device that reads either punched or marked cards (see Paragraph .168).

.164 Printed Output

Hewlett-Packard supplies three line printers. The 2778A is a drum printer that prints 120 characters per line at speeds up to 300 lines per minute. The ASCII character set is used. Format control is by paper tape loop. The 2778A-001 prints 132-column lines at 300 lines per minute. The 2767A Line Printer prints 80-column lines at 300 to 1,100 lines per minute.

.165 Magnetic Tape Input/Output

Two types of magnetic tape units are available for the HP 2116C, 7- and 9-channel magnetic tape transports. All the units use IBM-compatible tape formats; the 7-channel tape format is compatible with that of the IBM 729 Series units and the 9-channel format is compatible with that of the IBM 2400 Series units. The basic characteristics of all the units are summarized in Table III.

TABLE III. CHARACTERISTICS OF HP 2116C MAGNETIC TAPE UNITS

Model No.	Tape Speed, inches/sec	Recording Density, bits/inch	Peak Speed, char/sec	Interblock Gap Lengths			Efficiency, % (3)		
				inches	msec (1)	chars (2)	100-char blocks	1,000-char blocks	Rewind Speed, inches/sec
HP (H27) 2020AB 7-Channel Magnetic Tape Units	30	200 556	6,000 16,700	0.75 0.75	25 25	150 417	40.0 19.3	86.9 70.5	150 150
HP (H01) 3030G 9-Channel Magnetic Tape Unit	75	800	60,000	0.6	8	480	17.2	67.5	150
HP 7970A-200 9-Channel Magnetic Tape Unit	25	800	20,000	0.6	24	480	17.2	67.5	—
HP 7970A-202 9-Channel Magnetic Tape Unit	37.5	800	30,000	0.6	16	480	17.2	67.5	—

Notes:

(1) Time in milliseconds to traverse each interblock gap when reading or writing consecutive blocks.

(2) Effective number of character positions occupied by each interblock gap.

(3) Effective speed at the indicated block size, expressed as a percentage of peak speed.

All magnetic tape units perform conventional read-after-write, character parity, and cyclic redundancy checks.

All the magnetic tape units are connected to the computer via standard input/output channels. The HP (H01) 3030G 9-channel unit requires the DMA option for its use, but the other units can be used directly on the programmed I/O channels. All units require two I/O channel slots.

.166 Data Communications Input/Output

Hewlett-Packard provides interface kits for connecting a Bell System (or equivalent) data set to a standard input/output channel. A Teletype multiplexor interface, developed for use as part of the HP 2116C time-sharing system, enables up to 16 local and remote teletypewriters to be connected to a single standard input/output channel through dataphone connections or hard-wired cable up to a mile in length.

An unusual communications device, the HP 2761A-007 Optical Mark Reader supplied by Hewlett-Packard, can be connected to a remote HP 2116C computer via a Bell System dataphone interface. This device uses standard-size tab cards for data entry. Each card contains a maximum of 12 rows and 80 columns of data. Data on the card can be punched as for a conventional card reader, marked in preprinted marking boxes with an ordinary lead pencil, or coded by a combination of punched holes and marks. Reading, which is controlled by clock marks printed along the bottom edge of the card, is at 200 cards per minute. The HP 2761A-007 has an automatic feed mechanism. A 7200A Graph Plotter can be connected in series with a teleprinter and plots data that would normally be printed on the teletype unit. The 7200A accepts ASCII characters, four digits for the x coordinate and four digits for the y coordinate. Plotting area is 11 by 17 inches.

Hewlett-Packard also provides an HP 2600A CRT Keyboard, which can be used as a keyboard console to the 2116C, the 2600A can be located on-site or used as a remote terminal. The 2600A transfers data at a rate of 10 to 218 characters per second.

The 2570A Coupler/Controller allows laboratory measuring devices to interface with a time-sharing system. The 2570A is connected in series with a Teletype unit that also inputs data to the time-sharing system.

.167 Analog/Digital Input/Output

Hewlett-Packard provides a number of interface kits for attaching analog/digital measurement and control devices to standard input/output channels. The interfaces available are summarized in Table I, and include general-purpose units as well as interfaces for specific Hewlett-Packard measuring instruments.

.168 Other Input/Output Devices

Hewlett-Packard supplies an interface kit for the use of a CalComp 563 or 565 Digital Plotter with the HP 2116C.

.18 Data Codes

The seven-bit ASCII code used as a standard for the HP 2116C computer is shown in Table IV.

To allow the recording of one character per row of the tape, information recorded on 7-channel magnetic tape units is converted by the standard software from ASCII to a six-bit character format, and converted back to ASCII by standard software after reading.

TABLE IV. HP 2116C ASCII CHARACTER SET

b_7				0	0	0	0	1	1	1	1
b_6				0	0	1	1	0	0	1	1
b_5				0	1	0	1	0	0	0	1
b_4	b_3	b_2	b_1								
0	0	0	0	NULL	DC_0	*	0	@	P		
0	0	0	1	SOM	DC_1	'	1	A	Q		
0	0	1	0	EOA	DC_2	"	2	B	R		
0	0	1	1	EOM	DC_3	#	3	C	S		
0	1	0	0	EOT	DC_4 (STOP)	$	4	D	T	UNASSIGNED	UNASSIGNED
0	1	0	1	WRU	ERR	%	5	E	U		
0	1	1	0	RU	SYNC	&	6	F	V		
0	1	1	1	BELL	LEM	' (APOS)	7	G	W		
1	0	0	0	FE_0	S_0	(	8	H	X		
1	0	0	1	HT / SK	S_1	)	9	I	Y		
1	0	1	0	LF	S_2	*	:	J	Z		
1	0	1	1	V_{TAB}	S_3	+	;	K	[		
1	1	0	0	FF	S_4	, (COMMA)	<	L	\		ACK
1	1	0	1	CR	S_5	-	=	M	]		ⓘ
1	1	1	0	SO	S_6	.		N	↑		ESC
1	1	1	1	SI	S_7	/	?	O	←		DEL

Standard seven-bit set code positional order and notation are shown below with B_7 the high-order and b_1 the low-order bit position.

LEGEND

NULL	Null/idle	DC_1-DC_3	Device control
SOM	Start of message	DC_4 (Stop)	Device control (stop)
EOA	End of address	ERR	Error
ECM	End of message	SYNC	Synchronous idle
EOT	End of transmission	LEM	Logical end of media
WRU	"Who are you?"	S_0-S_7	Separator information
RU	"Are you . . . ?"		Word separator (space, normally nonprinting)
BELL	Audible signal		
FE_0	Format effector	<	Less than
HT^0	Horizontal tabulation	>	Greater than
SK	Skip (punched card)	↑	Up arrow (exponeniation)
LF	Line feed	←	Left arrow (implies/replaced by)
V_{TAB}	Vertical tabulation	\	Reverse slant
FF	Form feed	ACK	Acknowledge
CR	Carriage return	ⓘ	Unassigned control
SO	Shift out	ESC	Escape
SI	Shift in	DEL	Delete/idle
DC_0	Device control reserved for data line escape		

TABLE V. HP 2116C ASCII TO BCD CONVERSION TABLES FOR 7-CHANNEL MAGNETIC TAPE UNITS

Symbol	ASCII (Octal Code)	BCD (Octal Code)	Symbol	ASCII (Octal Code)	BCD (Octal Code)
(Space)	4Ø	2Ø	A	1Ø1	61
:	41	52	B	1Ø2	62
"	42	37	C	1Ø3	63
#	43	13	D	1Ø4	64
$	44	53	E	1Ø5	65
%	45	34	F	1Ø6	66
&	46	60 (1)	G	1Ø7	67
'	47	36	H	11Ø	70
(	5Ø	75	I	111	71
)	51	55	J	112	41
*	52	54	K	113	42
+	53	6Ø	L	114	43
,	54	33	M	115	44
-	55	4Ø	N	116	45
.	56	73	O	117	46
/	57	21	P	12Ø	47
			Q	121	50
Ø	6Ø	12	R	122	51
1	61	Ø1	S	123	22
2	62	Ø2	T	124	23
3	63	Ø3	U	125	24
4	64	Ø4	V	126	25
5	65	Ø5	W	127	26
6	66	Ø6	X	13Ø	27
7	67	Ø7	Y	131	30
8	7Ø	1Ø	Z	132	31
9	71	11	[	133	75 (2)
:	72	15	]	135	55 (2)
;	73	56	'	136	77
<	74	76	-	137	32
=	75	35			
>	76	16			
?	77	72			
@	1ØØ	14			

Notes:

(1) BCD code of 60 always converted to ASCII code 53 (+).
(2) BCD code of 75 always converted to ASCII code 50 (( ) and BCD code of 55 always converted to ASCII code 51 ()).

The Hewlett-Packard 2114C and 2116C computers share the same software, subject to the configuration requirements of each package. All the software described in this section is currently available.

.1 UTILITY ROUTINES

Hewlett-Packard does not include provisions for simulation of other computers, data sorting and merging, report writing, or data transcription in any of the standard programming packages for the 2116C.

.2 PROBLEM-ORIENTED LANGUAGES

No problem-oriented languages are included in any of the standard programming packages for the 2116C.

.3 ASSEMBLERS

.31 HP 2116C Basic Assembler

The HP 2116C Basic Assembler is a straightforward, machine-oriented language. Source coding is written in a free-field format; each source-code statement consists of a single line of up to 80 characters. Character positions 73 to 80 on each line are ignored by the assembler. Labels consist of up to five characters selected from the alphanumeric characters and the period character; the first character of a label cannot be numeric. There is no macro facility. Pseudo-instructions provide facilities for the allocation of data storage, specification of constants, and manipulation of the program location counter. All memory address references in an assembly language program can be specified as either direct or indirect. Direct references to locations in the base page do not require any special action by the programmer as the assembler detects these and sets the instructions generated to address the base page.

The binary program generated by the assembler can be in either absolute or relocatable binary form. Relocatable subprograms can be assembled separately and linked when they are loaded; directives are available for the specification of entry points, external references, and common working space for relocatable programs. Programs written for assembly into relocatable binary form can be coded in assembly language as if the whole of main memory were directly addressable, indirect address references being provided where necessary by means of loader-generated constants in the base page. Parts of a relocatable assembly can be specified by the programmer for inclusion in the base page.

The first program statement in each assembly must be a control statement specifying the output required; the options include a binary program tape in absolute or relocatable form, a source code listing, and a symbol table. Diagnostic messages are printed during the assembly if necessary.

The minimum configuration necessary for assembling an object program consists of 4,096 words of memory and a teletypewriter. Other peripheral devices can be assigned for the use of the assembler. The assembler is usually loaded from paper tape but it can be supplied on magnetic tape for faster loading. Any number of separate assemblies can be performed without reloading the assembler; but if both absolute and relocatable assemblies are to be undertaken, all the relocatable assemblies must be completed before any of the absolute assemblies.

An assembly normally requires two passes; but if the same device must punch the binary program and list the source code, three passes are needed. The binary program is punched during the second pass and the source program is listed during the third pass.

There are no critical restrictions on the size of the program that can be assembled. Programs containing 250 to 300 symbols can be assembled on a machine with 4,096 words of main memory, a paper tape reader, a paper tape punch, and a teletypewriter.

.32 HP 2116C Extended Assembler

The HP 2116C Extended Assembler is an extended version of the HP 2116C Basic Assembler designed to use a main memory of 8,192 words. The extra facilities provided include a range of pseudo-instructions to control the format of the assembler output listing, and the specification of literals as operands for main memory reference instructions. The literals specified are generated by the assembler as constants, which are placed in main memory at the end of the generated program and addressed from the instructions in which they were specified. Source programs for processing by the extended assembler can be written as if the whole of the main memory were directly addressable. Where necessary, the extended assembler generates indirectly addressed references via loader-generated constants in the base page.

There is no macro facility, but a pair of pseudo-instructions provide for marking off sections of code for optional inclusion in the assembled program, using additional parameters specified at the start of the assembly. Two parameters are available, either (but not both) of which can be specified to request the inclusion of one or more sections of code marked off by the appropriate pseudo-instructions. Optional sections of code cannot be nested or overlapped.

.4 COMPILERS

.41 HP 2116C Fortran

HP 2116C Fortran is an extended version of USASI (formally ASA) Basic Fortran, X.3. 10-1966 published by the United States of America Standards Institute in 1966 and also published in the October 1964 issue of the Communications of the ACM as the ASA proposed Basic Fortran language. The extensions to the Basic Fortran language include:

- Format specifications can be entered at execution time.
- COMMON array declarations are permitted.
- A function subprogram can change the values of its arguments and of COMMON storage; that is, the arguments of function subprograms are "called by name."
- External functions are included for Boolean operations.
- The "$" sign is included in the character set.
- A two-branch form of the IF statement is included.
- A facility for octal constant specification is provided.

The Fortran compiler is available in paper tape and magnetic tape versions. The minimum configuration for the paper tape version of the compiler is 4,096 words of main memory and a 2752A teleprinter, but the addition of a paper tape reader and punch significantly increases the compilation speed. Both versions of the compiler produce an object program in relocatable binary format for loading by the Basic Control System. The program can be linked to relocatable binary subprograms originating from assembly code or Algol source code. The Basic Control System is described in Paragraph .5.

The paper tape version of the Fortran compiler operates in two passes on a computer with a main memory of 8,192 words. Each pass of the paper tape compiler produces an intermediate binary tape for input to the next pass. The magnetic tape Fortran compiler uses a work area on the tape to store the intermediate results. Each Fortran program to be compiled starts with a control statement giving the output required from the compilation — any combination of the source code listing, the relocatable binary program, and the object code listing in assembly language can be requested. The four-pass Fortran compiler for machines with a 4,096-word main memory uses a fifth pass if both the object program listing and the binary program tape are to be output on the same device. Hewlett-Packard also provides a full implementation of Fortran IV for use under the Real-Time and Disc Operating Systems.

.42 HP 2116C Basic

HP 2116C Basic is a system built around an interpretive compiler which provides conversational computing facilities for a single user via the console typewriter. The minimum configuration requires an HP 2116C computer with 8,192 words of main memory and a 2752A teleprinter; if a paper tape reader and punch are available, these devices can be used as well as the teleprinter for the input and output of Basic language programs. Programs stored externally on paper tape are in source language; there are no facilities for external storage of programs in binary or in any intermediate language.

The HP 2116C Basic system uses the Basic programming language developed by Dartmouth College with the support of the National Science Foundation. Basic is designed for interactive scientific computing applications, and is particularly well suited to the "desk calculator" type of application. It is somewhat similar to Fortran or a simplified form of Algol. Standard functions available include trigonometric, logarithmic, and exponential functions and square root; these functions can be freely used within arithmetic expressions. A series of statements provides facilities for matrix operations, including inversion, acting on data stored in two-dimensional Basic language arrays. The Boolean operators AND, OR, and NOT can be combined to form composite conditional statements, assigning the function values zero (false) or +1 (true). Subroutines can be used within a Basic program, nested to a maximum depth of nine. The whole of the user's program is stored in source code form and can be modified at any time, the Basic subsystem maintains statement numbers for each line of the source program referenced for program modification purposes.

The HP 2116C Basic language is the same as standard Dartmouth Basic with two additional statements — the WAIT statement, which suspends operation of the program for a specified number of milliseconds, and the CALL statement. The CALL statement allows the calling, from within a Basic program, of subroutines, which have been incorporated into the Basic system; in particular, this allows the use of input/output drivers when no provision for the device exists in standard Basic.

A configured Basic system including input/output driver subroutines for the Teletype, optical reader, and paper tape punch occupies 6,200 words of core, leaving 2,000 words for the user area. Since there is no optical reader and paper tape punch in this system, 50 words are transferred from the system to the user area. Any binary subroutines added to this system for use by CALL statements reduce the user area by an amount corresponding to their storage requirements. The user area is dynamically divided among the current program (including its symbol table), arrays required by the current program, and working space used during execution for evaluating expressions, bookkeeping on active loops, and inverting matrices. There are no restrictions on the proportions of user space allocated among the above; as long as any space remains, it can be claimed for any purpose.

Statistical examination of Basic programs has given a rule of thumb on program size. The amount of user space occupied by a program and its symbol table averages 10 or 11 words per Basic statement. Arrays occupy two words per declared element. Fifty words suffice for execution working space; six words are required per level of loop nesting. Matrix inversion requires additional working space sufficient to copy the array to be inverted.

Additional memory provided by larger hardware configurations (e.g., 16,384 words of main memory) is assigned entirely to the user area.

The Basic language used in the time-shared system is an extension of HP 2116C Basic. The language has been augmented by including string variables and facilities for their manipulation and by the addition of disc-resident data files, accessible by a user program. Data files can hold both numeric and string information.

Before HP 2116C Basic is used on any particular computer configuration, it must be configured to reflect the device and channel assignments required and to include any special-purpose subroutines that the user wishes to include for use via the CALL statement. The input/output drivers for the peripheral devices must also be incorporated. The configuration of the Basic

system is performed by using the Prepare Basic System (PBS) program supplied by Hewlett-Packard; the PBS tape includes relocatable drivers for the teleprinter, paper tape reader, and paper tape punch which are included in the generated system when necessary. Details of the peripheral complement of the configuration for which the Basic system is being generated are input to PBS via the console typewriter.

.43 HP 2116C Algol

HP 2116C Algol incorporates all the major features of the Algol language as described in the Algol 60 Revised Report, published in the Communications of the ACM for January 1963. Input/output statements are the same as for HP 2116C Fortran. All variables are treated as OWN variables. Other features of the source language include:

- Facilities for intermixing identifiers of types REAL and INTEGER in the same assignment statement.
- Provision for initializing variables and arrays.
- An EQUATE statement.

The HP 2116C Algol compiler requires a main memory of 8,192 words and a teleprinter. The compiler operates in a single pass of the source code and produces an object program in relocatable format for loading by the Basic Control System. Relocatable programs generated from Algol source language can be linked to subprograms generated from Fortran or assembly language source code. There are essentially no restrictions on the size of the Algol program that can be compiled.

.5 OPERATING ENVIRONMENT

.51 The Basic Binary Loader and Facilities for Absolute Programs

The Basic Binary Loader loads an absolute binary program tape into main memory for execution. Once loaded, the Basic Binary Loader generally remains in the top 64 locations of main memory; the information stored in these locations cannot be altered, and the Basic Binary Loader cannot be executed, when the Loader switch on the console is set to the Protected position. The operator starts execution of the Basic Binary Loader at any time by manually passing control to the loader starting address by means of the keys on the console. When a program has been loaded by the Basic Binary Loader, execution of the loaded program is started by depressing the Run button on the operator's console.

A set of System Input/Output (SIO) subroutines is supplied for the use of absolute binary programs. These provide input/output driver facilities for the teleprinter, paper tape, and magnetic tape equipment. When the SIO subroutines are to be used by absolute binary programs, they are loaded in absolute form by the Basic Binary Loader and are reached via a system linkage table held in a standard position in main memory. The SIO subroutines transfer a buffer full of data at each entry. Interrupt control is not used; except in the case of magnetic tape rewind operations, these subroutines retain full control until the operation requested is completed.

The assemblers and the Fortran and Algol compilers are supplied as absolute binary programs that can be loaded by the Basic Binary Loader; all can use the SIO subroutines. This means that these programs do not overlap input/output operations with one another or with computation.

.52 The Basic Control System and Facilities for Relocatable Programs

The Basic Control System (BCS) provides an environment for the loading, debugging, and running of relocatable binary programs. The system is constructed to fit a particular computer configuration from a series of relocatable programs used as input to a standard Prepare

Control System (PCS) program. PCS accepts information on the target configuration via the console typewriter.

The BCS itself consists of a relocating loader and input/output subroutines. Associated with the BCS are the program library and the Debugging System.

The BCS Relocating Loader is the component of the Basic Control System that provides program loading and linking facilities. It is available in two versions for main memory sizes of 4,096 words or 8,192 words and larger. The loading of Algol programs and searching of the magnetic tape program library are facilities provided only for machines with main memory of 8,192 words or larger. The BCS loader accepts as input relocatable binary program tapes originating from the assembler, the Fortran compiler, or the Algol compiler. There are no restrictions on the linking of subprograms originating from different source languages. During program loading, terms requiring relocation are relocated relative to the base page, the position of the user's program, or the location of common storage according to directions on the relocatable binary program tape. Memory references to points not in the current page or base page, or resolved by the creation of indirect references via locations in the base page set up during program loading, and cross-references between separately compiled subprograms are resolved in the same way. When loading is complete, BCS searches the program library for any library routines required by unresolved external references.

The input/output drivers that can be used via the input/output control facilities provided through the BCS supply extensive block transfer facilities for the whole range of available peripheral devices. Provision is made for use of the direct memory access channel. These input/output drivers are fully interrupt controlled, giving input/output simultaneity that is limited only by the capabilities of the hardware.

The BCS provides a facility for the output of a program in absolute binary form together with the input/output control, interrupt handling, and program library routines it uses. Production programs output in this form can be loaded rapidly using the Basic Binary Loaders.

The program library, supplied as a series of relocatable subroutines for use with the Basic Control System, includes extensive arithmetic, input/output, and mathematical subroutines. Floating-point arithmetic subroutines are provided, as are multiplication and division subroutines for use on machines without the optional extended arithmetic unit. The mathematical subroutines include the evaluation of exponential, logarithmic, trigonometric, and hyperbolic functions and the summation of Chebyshev series.

The Debugging System, a relocatable program for use with BCS, is loaded into memory after the user's program but before the library subroutines. It is a conversational system operating via the console typewriter. Dump and trace facilities are provided, as well as facilities for modifying the contents of memory locations and registers and restarting execution at any point in the program. Breakpoints can be placed in the program, and the whole execution process is fully controlled from the console typewriter. An interpretive method of program execution is used.

The Basic Control System, in conjunction with the Basic Binary Loader described in Paragraph .51, supplies a comprehensive set of operating programs and facilities for use in cases where a full-scale, integrated operating system is not required. All the programs in the Basic Control System, as well as the assemblers and compilers, are available in versions which use magnetic tape for the storage of systems programs and relocatable and absolute binary object programs, leading to substantial savings in program running times. The magnetic tape version of the Basic Control System has a minimum main memory requirement of 8,192 words.

.53 Time-Shared Basic Systems

The HP 2000 Time-Shared Basic Systems are Basic language programming systems that provide conversational program entry and interpretive program execution for up to 32 users simultaneously. The Time-Shared Basic Systems are 2000A, B, and C. The 2000A is the minimum system for 16 terminals. It is upward compatible with the 2000B, which supports

32 terminals. The 2000B is upward compatible with the 2000C, which also supports 32 terminals but includes much more mass storage.

A minimum 2000A hardware configuration requires the 2116C computer, with 16,384 words of core storage, 524,000 words of mass storage, high-speed tape reader, and a heavy-duty system console. The processor must include the following options: direct memory access, extended arithmetic unit, power fail interrupt with automatic restart, memory parity check, time base generator, and Teletype multiplexor.

The minimum 2000B hardware configuration also includes an HP 2114 system that operates as a terminal processor.

The minimum 2000C configuration includes both fixed-head and movable-head mass storage units, magnetic tape storage, and 32,768 words of core storage in the 2116C. Mass memory is used for storage of systems programs, current user programs, saved user programs and tables required by the library, and accounting systems which are part of the HP 2000 software.

The remote terminals supported by the timesharing systems are the teleprinters, the 2570A coupler/controller, the 7200A Graph Plotter, the 2761B Optical Mark Reader, and the 2600 CRT Keyboard. These can be connected to the computer either by direct cables up to a mile long or via the telephone network and suitable data sets.

The Basic language is used throughout for user programming, and file space on the disc is available to user programs. The 2000A system provides 393,000 words of file storage, the space for about 200 programs of 100 statements each. Additional storage can be provided initially or in the field by expanding the basic system or by adding up to three fixed-head discs or drums.

The 2000B system includes up to 786,432 words of file storage. In addition, the software allows a program to call another program and to access an almost unlimited number of files. Common storage facilities are also provided.

Because the 2000C includes very large mass storage devices, it is a much more powerful system than either the 2000A or B. Maximum file size is 32,767 records of 512 eight-bit bytes each. The system can copy selected files on 9-track magnetic tape for processing on another system. The complete system can be dumped onto a magnetic tape or a removable disc pack or cartridge ("sleep the system"), and the Disc Operating System (DOS) loaded for conversion to the DOS mode for batch processing programs written in Algol, Fortran, or assembly language. The timesharing system can be reloaded, and the timeshare mode reentered.

The 2000C System backup is maintained on magnetic tape.

.54 Data Acquisition and Control Executive

The Data Acquisition and Control Executive (DACE) is a software package designed for use with test equipment. It provides for real-time operation of the system and permits modification of the stored program with respect to system timing and channel assignments directly through the teleprinter keyboard without program recompilation. The system is programmed to perform tasks involving measurement, computation, and output of data from one or a group of channels. The system includes a 24-hour clock, maintained by software, which allows the user to cue tasks at desired elapsed times from program start. The system can be switched to a "manual" operating mode, in which task constants can be examined and modified via the teleprinter keyboard. This allows a test engineer to modify testing procedures as testing proceeds. DACE requires a minimum of 8,192 words of main memory.

.55 Real-Time Executive System

The Real-Time Executive System is a self-contained operating system for a HP 2116C computer with 16,384 words of main memory and a disc memory unit. It provides facilities for servicing events in real-time multiprogrammed with background processing. Each user

program in the system is classified as either real-time memory resident, real-time disc resident, or background disc resident; the fetching of programs from the disc for execution is performed automatically by the executive. Only one background disc resident program can be in the system at one time — there is no multiprogramming of background processing programs. The Assembler and the Fortran compilers are available in segmented versions that can be run as background disc resident programs in the Real-Time Executive System.

.56 Disc Operating System

The Disc Operating System (DOS) provides a tool that simplifies the creation, checkout, and operation of user programs. Some of the features provided are:

- Keyboard or batch (card input) control.
- Compile or assemble with load and go capability.
- Centralized control of I/O processing.
- Disc file arrangement including the ability to load, store, delete, and list user files and edit user source statement files.
- Job accounting giving both run and execut times for each job.

Programs written in Fortran IV, Algol, or assembly language can run under DOS. DOS utilizes the moving-head disc units now supplied by Hewlett-Packard.

.6 APPLICATIONS PROGRAMS

A number of special-purpose software packages have been developed by Hewlett-Packard for particular applications. These are generally not based on any of the standard operating systems but are self-contained software systems, which are marketed as complete packages that include hardware. The following sections describe some of these special-purpose systems from a software standpoint.

.61 Educational Basic System

The Educational Basic System is a package designed especially for the educational market. The software supplied is the standard Basic language system with one addition — a Marked Card Basic program is included. This is the same as the standard (single-user) Basic language program except that the HP 2761A Optical Mark Card Reader is supported as an input device for Basic language programs. Special preprinted cards are available on which Basic language source statements can be entered simply by marking boxes on the cards with an ordinary lead pencil; thus, pupils can prepare their own source programs without any data preparation equipment. When the reader is loaded, the programs are run under the Basic language system with printout on a teleprinter in the usual way. The teleprinter and reader can be either local to the computer or connected to it via telephone lines.

.62 HP 2060A Digital Logic Module Test System

This is a special-purpose combined hardware/software system which is designed for the automatic testing of digital logic modules. All types of integrated circuit and discrete-component logic can be tested without special adaptation. The system is based on a 2116C computer with 8,192 words of main memory and includes an HP 12660A Module Adaptor, which is a unit that enables two plug-in modules to be mounted side by side — the module under test and a fault-free module of the same type. A series of tests is carried out on both modules and any differences between the two are logged on the console typewriter. The software provided includes a special-purpose programming language called AuTest for writing test programs. AuTest has been designed for use by digital logic engineers and includes statements listing all the module signal connector pins and specifying power supply voltages, high and low logic

levels, current limits, and comparison tolerances. The TEST statements include facilities for a programmed delay between changes of logic level to satisfy module timing requirements. There is a PERMUTE instruction which initiates the testing, in a single statement, of all possible combinations of logic levels on up to 16 pins. The maximum speed of the system is 10,000 tests per second per pin with no delays programmed. Between tests, the 2060A system is in a conversational mode, receptive to commands typed on an input keyboard.

HP 2116C
PHYSICAL CHARACTERISTICS

Unit	Width, inches	Depth, inches	Height, inches	Weight, pounds	Power, kva	BTU/ hr
HP 2116C Computer	16.75	19.38	31.5	230	1.0-1.6	5,500 max
HP 2752A Teleprinter	25.5	18.5	33.0	77	0.23	
HP 2754B Teletypewriter	40.0	24.0	33.5	225	0.23	
HP 2745A Punched Tape Reader	19.0*	9.4	7.0	15	0.04	
HP 2753A Tape Punch	19.0*	?	?	59	0.45	
HP 2020B Magnetic Tape Unit	19.0*	16.0	42.0	193	0.97	

*Mounting in standard 19-inch rack.

General Requirements

Temperature:	32° to 131°F
Relative Humidity:	to 95% at 104°F
Power:	115V, 50Hz ± 10%
	230V, 60Hz ± 10%

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HP 2116C
PRICE DATA

CLASS	IDENTITY OF UNIT			PRICES		
	Model Number	Feature Number	Name	Monthly (2) Rental $	(1) Purchase $	Monthly (3) Maint. $
CENTRAL PROCESSING AND WORKING STORAGE	2116C		Computer (includes 8,192-word memory; operates on 115V/230V, 50- to 60-Hz supplies)		14,000	
			Processor Options			
		005	16,384-Word Memory		8,000*	
		006	24,576-Word Memory		16,000*	
		007	32,768-Word Memory		24,000*	
		015	230-Volt Operation		N/C	
		12578A	Direct Memory Access		1,500	
		12579A	Extended Arithmetic Unit		2,000	
		12581A	Memory Protect		1,000	
		12588A	Power Fail Interrupt (with automatic restart)		500	
		12591A	Memory Parity Check (with interrupt)		500	
		12615A	Field Installation of 8,192-Word Memory		8,000	
			I/O Extension			
	2151A		I/O Extender (operates on 115V, 50- to 60-Hz supplies; provides power and slots for 16 additional I/O channels)		3,500	
		015	230-Volt Operation		100	
	12596A		Interfaces 2151A to 2116C (for a total of 32 I/O channels)		1,500	
	2150B-001		I/O Extender (cabinet provides power supplies and prewired slots for 32 additional I/O channels for a total of 48 I/O channels; operates on 115V, 50- to 60-Hz supplies)		10,000	
		015	230-Volt Operation		N/C	
AUXILIARY RANDOM ACCESS STORAGE	12610C(4)		Interface Kit (includes HP 2772A Power Supply and an HP 2766A Disc Memory)			
			With HP 2766A Disc Memory (262,144 16-bit words of storage, average access time of 8.7 msec, transfer rate of 118K words/sec)		27,500	
			With HP 2766A-002 Disc Memory (similar to HP 2766A except 524,288 words of storage)		32,000	
			With HP 2766A-003 Disc Memory (similar to HP 2766A except 786,432 words of storage)		36,500	
			With HP 2766A-004 Disc Memory (similar to HP 2766A except 1,048,576 words of storage)		41,000	
	12865A		Expansion Kit (field expansion of the 2766A, 002, and -003 by 262,144 words)		6,500	
	12610B(4)		Interface Kit (includes a drum memory and HP 2776A Power Supply)			
			With 2773A Drum Memory (373,216 16-bit words of storage, average access time of 8.7 msec)		30,000	
			With 2774A Drum Memory (similar to 2773A except 786,432 words of storage)		36,500	
			With 2774A-003 Drum Memory (similar to 2773A except 1,048,576 words of storage)		41,000	
	12553A-001		Expansion Kit (field expansion of the 2773A by 393,216 words of storage)		7,500	
	12553A		Expansion Kit (field expansion of the 2773A and 2774A by 262,144 words of storage; 2773A requires prior installation of the 12553A-001)		5,500	
	12557A		Interface Kit for Cartridge Disc Memory (includes HP 2870 Moving Head Disc; HP 2871A Disc Controller can handle up to 4 drives, HP 2881 Power Supply, and HP 2882A Cabinet)			
			With HP 2870A Moving Head Disc (one fixed and one removable disc, total storage of 1,247,232 16-bit words, average random access time of 98 msec, transfer rate of 38,400 words/sec)		16,000	

CLASS	IDENTITY OF UNIT			PRICES		
	Model Number	Feature Number	Name	Monthly[2] Rental $	Purchase $[1]	Monthly[3] Maint. $
AUXILIARY RANDOM ACCESS STORAGE (CONT'D.)	HP 2870A-001		Moving Head Disc Drive (an additional 2870A Drive for the 12557A provides 1,247,232 words of storage; the same controller can handle 4 drives, but the third and fourth drives require another cabinet and power supply)		8,700	
	HP 12563A		Cartridge (for the HP 2870A Discs)		110	
	12565A[4]		Interface Kit (includes HP 2883A Disc File and Controller; can handle up to 2 disc files; each file stores 11,776,000 16-bit words, average access time of 32 msec, transfer rate of 155,000 words/sec)		39,000	
	HP 2884A		Disc File (additional file for the 12565A)		26,000	
	HP 12868A		Disc Pack (for the HP 2883A and HP 2884)		600	
INPUT/OUTPUT			Console Typewriters			
	12531B		Console Typewriter Interface Kit			
			With HP 2752A Teleprinter (modified Teletype ASR 33)		2,000	
			ASR 33			
			For 230V, 50-Hz power source, add		200	
			With HP 2754B Teleprinter (modified Teletype ASR 35)		4,600	
			Paper Tape			
	12597A-002		Interface Kit			
			With HP 2748A		2,100	
			Punched Tape Reader (500 char/sec)			
			With HP 2758A Tape Reader Reroller (500 char/sec)		3,600	
	12597A-003		Interface Kit			
			With HP 2753A Tape Punch (120 char/sec)		4,100	
	HP 12575A		Tape Winder (hand held)		50	
			Punched Card			
	12602A		Interface Kit			
			With HP 2761A-007 Optical Mark Reader (reads punched and marked cards, 200 cards/min)		3,700	
	12882A		Interface Kit			
			With HP 2891A Card Reader (1,000 cards/min)		8,000	
			Printers			
	12653A		Interface Kit			
			With HP 2767A Line Printer (80-col line, 300 to 1,100 lpm, ASCII char set)		12,500	
	12617A		Interface Kit			
			With HP 2778A Line Printer (120-col line, 300 lpm, ASCII char set)		23,000	
			With HP 2778-001 Line Printer (132-col line, 300 lpm, ASCII char set)		24,000	
			Magnetic Tape			
	12538B[4]		Interface Kit			
			With HP (H27) 2020B Magnetic Tape Unit (7-channel IBM-compatible tape, 200 and 556 bpi switch selectable, 30 ips)		13,895	
	13181A-001[4]		Interface Kit (can handle up to 4 mag tape units)			
			With HP 7970A-200 Magnetic Tape Unit (9-channel IBM-compatible tape, 800 bpi, 25 ips)		9,500	
	HP 7970A-200		Additional Magnetic Tape Unit (for the 13181A-001)		5,075	

CLASS	IDENTITY OF UNIT			PRICES		
	Model Number	Feature Number	Name	Monthly[2] Rental $	Purchase $[1]	Monthly[3] Maint. $
INPUT/OUTPUT (CONT'D.)	13181A		Interface Kit With HP 7970A-202 Magnetic Tape Unit (same as HP 7970-200 except 37.5 ips)		9,700	
	HP 7970A-202		Additional Magnetic Tape Unit (for the 13181A)		5,275	
	12559A[4]		Interface Kit With HP (H01) 3030G Magnetic Tape Unit (IBM-compatible 9-channel tape, 800 bpi, 75 ips)		18,500	
			Data Communications			
	12587A		Interface (for asynchronous dataphones)		2,000	
	12589A		Interface (for Bell System 801 automatic calling unit)		1,500	
	12618A		Interface (for synchronous send and receive data transmission)		3,000	
	12621A		Interface (for synchronous data receive only)		2,000	
	12622A		Interface (for synchronous data send only)		2,000	
	12880A		CRT Keyboard (includes HP 2600A CRT Keyboard Terminal (data transfer rate 10 to 218 char/sec))		6,250	
			Digital to Analog			
	12555A		Provides 2 D/A conversion channels, 8 bits/channel		1,000	
			Other			
	12539A		Time Base Generator (provides real-time intervals of 100 μsec to 1,000 sec for software clocks)		1,250	
	12551B		Relay Output Register (provides 16 form-A contacts for operating external devices)		750	
	12566A		Microcircuit Interface (provides a dual 16-bit flip-flop register; permits bidirectional data transfer between computer and external device at DTL/TTL voltage levels)		900	
	12597A		Dual 8-Bit General-Purpose Duplex Register (permits bidirectional data transfer between computer and external devices)		600	
	12560A		Digital Plotter Interface (to CalComp 563 or 565)		2,500	

N/C — No Charge

* Installed at time of original purchase.

Notes:

(1) Prices quoted for peripheral devices are for 120V, 60-Hz input power line; prices for 230V, 50-Hz input power line are slightly higher.
(2) Hewlett-Packard leases the 2116C on a 5-year lease plan. Monthly rate is 2.6 percent of the purchase price; 70 percent of the lease charges can be applied to payment if equipment is purchased; only 85 percent of the total list price of purchased equipment can be paid for by accrued lease payments.
(3) Hewlett-Packard is currently changing its maintenance prices.
(4) Requires two I/O slots.

HP 2116C REPORT UPDATE

In May 1971, Hewlett-Packard (HP) announced new 7970 Magnetic Tape Units and a new 7900A Disc Drive for use with the HP 2114, 2116, and 2100A computers. At the same time, HP announced new Accounting and Financial Information Systems software packages to run under the Disc Operating System (DOS).

The new 7970 drives are 7- and 9-track. Recording densities are 200, 556, and 800 bits per inch for 7-track tapes and 800 bits per inch for 9-track tapes. Tape speeds are 37.5 and 45 inches per second. The following chart presents the new tape models and the required interface kits.

Model Number	Description	Purchase Price, $
7970B	Magnetic Tape Uni⁴	4,600
-200	9-track, 800 bits/inch, 37.5 inches/sec	200
-202	9-track, 800 bits/inch, 45 inches/sec	400
-204	7-track, 200/556/800 bits/inch, 37.5 inches/sec	50
-206	7-track, 200/556/800 bits/inch, 45 inches/sec	250
13181A	Interface Kit for 9-track tape, 37.5 inches/sec (controller can handle up to 4 tape units)	4,900
-003	Adapts Interface Kit to handle tape speed of 45 inches/sec	No charge
13182A	Interface Kit for 7-track tape, 37.5 inches/sec (controller can handle up to 4 tape units)	5,750
-003	Adapts Interface Kit to handle tape speed of 45 inches/sec	No charge

The 7900A Cartridge Disc Drive is similar to the HP 2870A Disc Drive, using one fixed disc and one removable disc cartridge to store data. The 7900A can store 2.5 million words of data, twice the storage capacity of the 2870A. A summary of 7900A characteristics follows.

Model Number	Description	Purchase Price, $
7900A	Cartridge Disc Drive (includes 1 fixed and 1 removable disc cartridge, storage capacity 2.5 million 16-bit words, avg access time 47.5 msec, avg head positioning and settling time 35 msec, and avg latency 12.5 msec, transfer rate 156K words/sec)	9,750
13210A	Interface Kit for the 7900A (controller can handle up to 4 disc drives)	6,150

The Accounting and Financial Information Systems software packages cover payroll, accounts payable, accounts receivable and inventory, and financial statements. All packages access a common data base and operate under DOS on any HP computer.

The new disc and tape units are scheduled for delivery in October 1971.

HP 2116C
PRICE DATA

CLASS	IDENTITY OF UNIT			PRICES		
	Model Number	Feature Number	Name	Monthly Rental $ (2)	Purchase $ (1)	Monthly Maint. $ (3)
CENTRAL PROCESSOR AND WORKING STORAGE	2116C		Computer (includes 8,192-word memory; operates on 115V/230V, 50- to 60-Hz supplies)		14,000	74.00
			Processor Options			
		005	16,384-Word Memory		8,000*	6.50
		006	24,576-Word Memory		16,000*	13.50
		007	32,768-Word Memory		24,000*	21.00
		015	230-Volt Operation		N/C	—
		12578A	Direct Memory Access		1,500	11.00
		12579A	Extended Arithmetic Unit		2,000	6.00
		12581A	Memory Protect		1,000	3.00
		12588A	Power Fail Interrupt (with automatic restart)		500	3.00
		12591A	Memory Parity Check (with interrupt)		500	3.00
		12615A	Field Installation of 8,192-Word Memory		8,000	6.50
			I/O Extension			
	2151A		I/O Extender (operates on 115V, 50- to 60-Hz supplies; provides power and slots for 16 additional I/O channels)		3,500	15.00
		015	230-Volt Operation		100	
	12596A		Interfaces 2151A to 2116C (for a total of 32 I/O channels)		1,500	7.00
	2150B-001		I/O Extender (cabinet provides power supplies and prewired slots for 32 additional I/O channels for a total of 48 I/O channels; operates on 115V, 50- to 60-Hz supplies)		10,000	42.00
		015	230-Volt Operation		N/C	
AUXILIARY RANDOM ACCESS STORAGE	12610C (4)		Interface Kit (includes HP 2772A Power Supply and an HP 2766A Disc Memory)			
			With HP 2766A Disc Memory (262,144 16-bit words of storage, average access time of 8.7 msec, transfer rate of 118K words/sec)		27,500	25.00
			With HP 2766A-002 Disc Memory (similar to HP 2766A except 524,288 words of storage)		32,000	26.50
			With HP 2766A-003 Disc Memory (similar to HP 2766A except 786,432 words of storage)		36,500	27.50
			With HP 2766A-004 Disc Memory (similar to HP 2766A except 1,048,576 words of storage)		41,000	29.00
	12865A		Expansion Kit (field expansion of the 2766A, 002, and -003 by 262,144 words)		6,500	(5)
	12610B (4)		Interface Kit (includes a drum memory and HP 2776A Power Supply)			
			With 2773A Drum Memory (373,216 16-bit words of storage, average access time of 8.7 msec)		30,000	110.00
			With 2774A Drum Memory (similar to 2773A except 786,432 words of storage)		36,500	121.00
			With 2774A-003 Drum Memory (similar to 2773A except 1,048,576 words of storage)		41,000	127.00
	12553A-001		Expansion Kit (field expansion of the 2773A by 393,216 words of storage)		7,500	(5)
	12553A		Expansion Kit (field expansion of the 2773A and 2774A by 262,144 words of storage; 2773A requires prior installation of the 12553A-001)		5,500	(5)
	12557A		Interface Kit for Cartridge Disc Memory (includes HP 2870 Moving Head Disc; HP 2871A Disc Controller can handle up to 4 drives, HP 2881 Power Supply, and HP 2882A Cabinet)			
			With HP 2870A Moving Head Disc (1 fixed and 1 removable disc, total storage of 1,247,232 16-bit words, average random access time of 98 msec, transfer rate of 38,400 words/sec)		16,000	76.50

CLASS	IDENTITY OF UNIT			PRICES		
	Model Number	Feature Number	Name	Monthly Rental $ [2]	Purchase $ [1]	Monthly Maint. $ [3]
AUXILIARY RANDOM ACCESS STORAGE (CONTD.)	HP 2870A-001		Moving Head Disc Drive (an additional 2870A Drive for the 12557A provides 1,247,232 words of storage; the same controller can handle 4 drives, but the third and fourth drives require another cabinet and power supply)		8,700	49.00
	HP 12563A		Cartridge (for the HP 2870A Discs)		110	—
	12565A [4]		Interface Kit (includes HP 2883A Disc File and Controller; can handle up to 2 disc files; each file stores 11,776,000 16-bit words, average access time of 32 msec, transfer rate of 155,000 words/sec)		39,000	155.00
	HP 2884A		Disc File (additional file for the 12565A)		26,000	123.00
	HP 12868A		Disc Pack (for the HP 2883A and HP 2884)		600	—
	13210A		Interface Kit for 7900A Disc Cartridge Drive (includes power supplies and controller for up to four 7900A Drives)		6,150	25.00
	7900A		Disc Cartridge Drive (includes one fixed disc and one removable cartridge disc; total storage capacity of 2.5 million words, avg access time of 47.5 msec, transfer rate of 126K words/sec)		9,850	86.50
INPUT/OUTPUT			Console Typewriters			
	12531B		Console Typewriter Interface Kit			
			With HP 2752A Teleprinter (modified Teletype ASR 33)		2,000	64.00
			For 230V, 50-Hz power source, add		200	—
			With HP 2754B Teleprinter (modified Teletype ASR 35)		4,600	48.00
			Paper Tape			
	12597A-002		Interface Kit			
			With HP 2748A Punched Tape Reader (500 char/sec)		2,100	19.00
			With HP 2758A Tape Reader Reroller (500 char/sec)		3,600	33.00
	12597A-003		Interface Kit			
			With HP 2753A Tape Punch (120 char/sec)		4,100	30.00
	HP 12575A		Tape Winder (hand held)		50	—
			Punched Card			
	12602A		Interface Kit			
			With HP 2761A-007 Optical Mark Reader (reads punched and marked cards, 200 cards/min)		3,700	5.00
	12882A		Interface Kit			
			With HP 2891A Card Reader (1,000 cards/min)		8,000	53.00
			Printers			
	12653A		Interface Kit			
			With HP 2767A Line Printer (80-col line, 300 to 1,100 lpm, ASCII char set)		12,500	70.00
	12617A		Interface Kit			
			With HP 2778A Line Printer (120-col line, 300 lpm, ASCII char set)		23,000	138.00
			With HP 2778-001 Line Printer (132-col line, 300 lpm, ASCII char set)		24,000	138.00
			Magnetic Tape			
	12538B [4]		Interface Kit			
			With HP (H27) 2020B Magnetic Tape Unit (7-channel IBM-compatible tape, 200 and 556 bpi switch selectable, 30 ips)		13,895	100.50

CLASS	IDENTITY OF UNIT			PRICES		
	Model Number	Feature Number	Name	Monthly (2) Rental $	Purchase $ (1)	Monthly (3) Maint. $
INPUT/OUTPUT (CONTD.)	12559A (4)		Interface Kit With HP (H01) 3030G Magnetic Tape Unit (IBM-compatible 9-channel tape, 800 bpi, 75 ips)		18,500	104.50
	13181A		Interface Kit for 7970B-200 Magnetic Tape Drives (includes controller for up to 4 drives)		4,900	15.50
	13181A-003		Interface Kit for 7970B-202 Magnetic Tape Drives (includes controller for up to 4 drives)		4,900	15.50
	13182A		Interface Kit for 7970B-204 Magnetic Tape Drives (includes controller for up to 4 drives)		5,750	40.00
	13182A-003		Interface Kit for 7970B-206 Magnetic Tape Drives (includes controller for up to 4 drives)		5,750	40.00
	7970B		Magnetic Tape Drive, basic unit		4,600	51.50
		200	9-track, 800 bits/inch, 37.5 inches/sec		200	N/C
		202	9-track, 800 bits/inch, 45 inches/sec		400	N/C
		204	7-track, 200/556/800 bits/inch, 37.5 inches/sec		50	N/C
		206	7-track, 200/556/800 bits/inch, 45 inches/sec		250	N/C
			Data Communications			
	12587A		Interface (for asynchronous dataphones)		2,000	6.50
	12589A		Interface (for Bell System 801 automatic calling unit)		1,500	3.50
	12618A		Interface (for synchronous send and receive data transmission)		3,000	4.50
	12621A		Interface (for synchronous data receive only)		2,000	4.50
	12622A		Interface (for synchronous data send only)		2,000	4.50
	12880A		CRT Keyboard (includes HP 2600A CRT Keyboard Terminal (data transfer rate of 10 to 218 char/sec))		6,250	4.00
			Digital to Analog			
	12555A		2 D/A conversion channels, 8 bits/channel		1,000	3.00
			Other			
	12539A		Time Base Generator (provides real-time intervals of 100 μsec to 1,000 sec for software clocks)		1,250	3.00
	12551B		Relay Output Register (provides 16 form-A contacts for operating external devices)		750	2.00
	12566A		Microcircuit Interface (provides a dual 16-bit flip-flop register; permits bidirectional data transfer between computer and external device at DTL/TTL voltage levels)		900	3.00
	12597A		Dual 8-Bit General-Purpose Duplex Register (permits bidirectional data transfer between computer and external devices)		600	2.00
	12560A		Digital Plotter Interface (to CalComp 563 or 565)		2,500	3.00

N/C — No Charge

*Installed at time of original purchase.

Notes:

(1) Prices quoted for peripheral devices are for 120V, 60-Hz input power line; prices for 230V, 50-Hz input power line are slightly higher.
(2) Hewlett-Packard leases the 2116C on a 5-year lease plan. Monthly rate is 2.6% of the purchase price; 70% of the lease charges can be applied to payment if equipment is purchased; only 85% of the total list price of purchased equipment can be paid for by accrued lease payments.
(3) Maintenance prices quoted are for a 7 a.m. to 6 p.m. shift, 5 days per week.
(4) Requires two I/O slots.
(5) Maintenance price is listed for the item produced by the field installation.

HEWLETT hp PACKARD

CUPERTINO DIVISION • 11000 Wolfe Road, Cupertino, California 95014, Telephone 408-257-7000,

FROM Bob Yeager

TO Distribution

DATE January 25, 1971

SUBJECT Inquiries Regarding Cupertino Repricing

A number of you have received telephone inquiries from editors, brokers, etc. regarding the repricing of the 2116C and time-share computers of the Cupertino Division. In order that you might know what the official position is of the division regarding this repricing and therefore be in a better position to answer outside inquiries, we have provided the attached statement for your perusal.

Bob Y.

RLY/bg
Attachment

HEWLETT hp PACKARD

CUPERTINO DIVISION • 11000 Wolfe Road, Cupertino, California 95014, Telephone 408-257-7000, TWX 910-338-0221

COMPUTER REPRICING

Effective January 1st, the Hewlett-Packard Company announced a change in pricing on its 2116C computer, 2000 Series Time-Shared Systems and its functional discount for original equipment manufacturers.

This resulted in price reductions of about 10 percent in the total amount a customer typically spends on a computer, its options, accessories and peripherals.

In all cases, these lower prices strike a fair balance between the value our data products and services provide to our customers and an adequate level of profit to the company.

We are not involved in a price war. The minicomputer industry is characterized by frequent price-changing, largely due to new product introductions providing improved technology, more efficient manufacturing and, thus, lower costs.

Hewlett-Packard's 2116C computer was announced at a slightly lower price than its predecessor, the 2116B. Now that it has been in production for several months, we found we were able to make further cost improvements. These new prices are a result of savings made possible by a new, HP-designed folder-planar core memory, new production methods and volume of business.

The new prices also include increasing the company's functional discount to original equipment manufacturers by five percent.

OEM functional discounts are offered due to cost savings afforded the computer manufacturer. The OEM customer does not require the extensive warranty service, customer training and other support included in the price of a computer sold to an end user.

After carefully analyzing our experience in doing OEM business, we found that our costs permitted the five percent increase in functional discount. The new 15 percent discount would then be used in all future OEM pricing on CPU's.

This new pricing provides our customers with a greater value per dollar spent, provides us with greater competitive strength in the marketplace and still affords us an equitable return for the investment made in these products.

1-25-71