PAPER TAPE NO. 24335-16001
DATE CODE 1717

HP 12889A HARDWIRED SERIAL INTERFACE DIAGNOSTIC

reference manual

For HP 2100 Series Computers

NOTICE

The absolute binary code for this diagnostic is contained on one or more media (e.g., paper tape, cartridge tape, disc, and magnetic tape). The binaries also exist on single as well as multiple files. For the current date code(s) associated with these media, refer to appendix A in the *Diagnostic Configurator Manual*, part no. 02100-90157, dated August 1976 or later.

HEWLETT-PACKARD COMPANY
11000 WOLFE ROAD, CUPERTINO, CALIFORNIA, 95014

MANUAL PART NO. 02100-90169
MICROFICHE PART NO. 02100-90243

Printed: FEB 1978
Printed in U.S.A.

LIST OF EFFECTIVE PAGES

Changed pages are identified by a change number adjacent to the page number. Changed information is indicated by a vertical line in the outer margin of the page. Original pages do not include a change number and are indicated as change number 0 on this page. Insert latest changed pages and destroy superseded pages.

Change 0 (Original) ..... FEB 1978

NOTICE

The information contained in this document is subject to change without notice.

HEWLETT-PACKARD MAKES NO WARRANTY OF ANY KIND WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Hewlett-Packard shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance or use of this material.

Hewlett-Packard assumes no responsibility for the use or reliability of its software on equipment that is not furnished by Hewlett-Packard.

Library Index No.
12889.070.02100-90169

CONTENTS

CONTENTS (continued)

ILLUSTRATIONS

TABLES

SECTION I
INTRODUCTION

1-1. GENERAL

The HP 12889A Hardwired Serial Interface Diagnostic verifies the proper operation of the inter-computer HP 12889A Hardwired Serial Interface (HSI). It is one of the HP 2100 series computer system diagnostics executed in conjunction with the Diagnostic Configurator required for these diagnostics. The diagnostic can be executed in two different modes as follows:

a. A single CPU and a single interface Printed Circuit Assembly (PCA).

b. Interconnected dual CPU's and dual interface PCA's.

1-2. REQUIRED HARDWARE AND OPTIONS

The following hardware is required for a single CPU and single interface PCA:

a. A HP 2100 series computer with a minimum of 4k-words of memory. References to HP 2100 series computers in this manual applies to the 21MX M-Series and E-Series, 2100A/S, 2114A, 2115A, and 2116A computers.

b. A 12889A Hardwired Serial Interface PCA and one cable assembly, part no. 12889-60004.*

c. A loading device for loading the Diagnostic Configurator and the Diagnostic.

d. A console device for message reporting (recommended but not required).

e. DCPC (Dual Channel Port Controller), or DMA, installed in the computer (optional).

f. RG 59/U (Belden No. 9259 or equivalent) coaxial cable assembly, 1000 ft., 305 m (optional).

For dual CPU's and dual interface PCA's, two sets of the above hardware list are required.

*Replaces 12889-60003 cable which has BNC type connectors.

1-3. SOFTWARE REQUIREMENTS

The following software is required:

a. HP 12889A Hardwired Serial Interface Diagnostic binary tape, part no. 24335-16001.

b. HP 12889A Hardwired Serial Interface Diagnostic Reference Manual, part no. 02100-90169.

c. Diagnostic Configurator Absolute Binary Tape, part no. 24296-60001, and Diagnostic Configurator Reference Manual, part no. 02100-90157.

The diagnostic serial number (DSN), which is contained in memory location 126 (octal) is 103207 (octal).

1-4. LIMITATIONS

This diagnostic is forward and backward compatible with the exception of TEST 13 on the HP 2114 and HP 2115 computers.

PROGRAM ORGANIZATION

SECTION II

2-1. ORGANIZATION

This diagnostic program consists of 16 tests plus Initialization and Control sections. The Initialization and Control sections accept the select code, mode, and test selection entered by the operator. These parameters are entered via the S and A Registers. The select code of the 12889A Hardwired Serial Interface (HSI) is entered into the S-Register bits 0-5. The mode (single or dual CPU/HSI) is entered into S-Register bit 8 and the test selection is entered into the A Register.

The following table lists all tests of the diagnostic and their utilization in conjunction with the test mode selection:

Table 2-1. Test Description

Test No.	Description	Test Mode	
		Single	Dual
TST00	Header Message	X	X
TST01	Basic I/O, Interrupt Circuitry	X	X
TST02	Basic I/O, Interrupt Off	X	X
TST03	Basic I/O, Interface PCA Flag Test	X	X
TST04	Basic I/O Select Code Screen Test	X	X
TST05	Basic I/O, Interrupt Hold Off	X	X
TST06	Basic I/O, Interface PCA Control Test	X	X
TST07	Basic I/O, Preset	X	X
TST08	100 Word Transfer without interrupt and DCPC (DMA)	X	X
TST09	100 Word Transfer with interrupt and without DCPC (DMA)	X	X
TST10	Watch Dog Timer Test	X	X
TST11	Checks CLC	X	X
TST12	CRC Testing after 100 Word Transfer	X	X
TST13	Handshake Mode Verification		X
TST14	Listen/Repeat Mode Verification		X
TST15	Tag Bit and Interrupt of DCPC (DMA) Transfer		X

2-2. TEST CONTROL AND EXECUTION

The program outputs a title message to the console device for operator information if the console is present and was selected during configuration. The program then executes according to the options selected on the S Register. The Control Section primarily checks S-Register bits 15, 13 and 12.

The Control Section keeps count of the number of passes that have been completed and will output the pass count at the completion of each pass (if S-Register bit 10 is clear). The count will be reset only if the program is restarted.

Test sections are executed one after another in each diagnostic pass. User selection or default will determine which test sections will be executed. Refer to paragraph 2-3.

2-3. TEST SELECTION BY OPERATOR

The control portion of the program allows the option of selecting a test or sequence of tests to be executed. Set S-Register bit 9 to indicate that a test selection is desired and press RUN. The computer will come to a halt 102075 (octal) to indicate it is ready for selection. If the program is running, the test in progress will be completed and then the program will halt. Load the A-Register with the test(s) desired. A-Register bit 0 represents Test 00, bit 1 represents Test 01, and so on up to A-Register bit 14. Press RUN to execute the selected tests. If the A-Register is cleared, all tests possible with the available hardware and selected mode will be executed.

2-4. MESSAGE REPORTING

Messages report errors and give operator information. Error messages occur when the PCA fails to respond to a given control sequence. Information messages concern the progress of the diagnostic or provide instructions on performing some operation related to the CPU or the PCA. For each information message, an associated CPU halt will occur in the T (Memory Data) Register which allows the operator to perform the required procedure. To continue, press RUN.

If a console device is used, the printed message will be either an error or an information message. The first error message within a test is preceded by a line giving the test number. For example, the following messages may be output:

a.	Error with halt:	Message	TEST 00008 FLAG NOT SET ON DATA TRANSFER
		Halt Code	102010_8 (T Register)
b.	Information with halt:	Message	PRESS PRESET (EXTERNAL AND INTERNAL) PRESS RUN!
		Halt Code	102000_8 (T Register)

Test options can be selected by setting the S-Register bits before the diagnostic is run. These include the suppression of error messages, the suppression of error halts which is useful when looping on a test, and the suppression of information messages. The available options vs. S-Register bits are given in Table 3-2 in the Operating Procedures section of this manual.

OPERATING PROCEDURES

SECTION III

3-1. OPERATING PROCEDURE FLOWCHART

Depending upon the hardware available, the user utilizes either the single CPU/single-HSI mode or the dual CPU/dual-HSI mode. Set up the hardware as shown in Figure 3-1. In the dual CPU/HSI mode, the configurator and diagnostic must be loaded into each CPU. The diagnostic plus the diagnostic configurator requires a minimum of 4k-words of memory. Refer to the flowchart of Figure 3-2 for the diagnostic operating procedure. Initial S Register settings for the I/O Select Code and the setup mode are given in Table 3-1.

Table 3-1. Initial S-Register Settings

Bits	Function
0-5	Select Code of CPU I/O Slot used for 12889A
6-7	Reserved
8	Clear if Single Mode, set if Dual Mode
9-15	Reserved

3-2. RUNNING THE DIAGNOSTIC

The program will execute the diagnostic according to the options selected in the S Register as listed in Table 3-2. At the completion of each pass of the diagnostic, the pass count is printed on the console. If S Register bit 12 was not set, the CPU will halt with 102077_8 in the T (Memory Data) Register. At this point, the A Register contains the pass count. To execute another pass, press RUN.

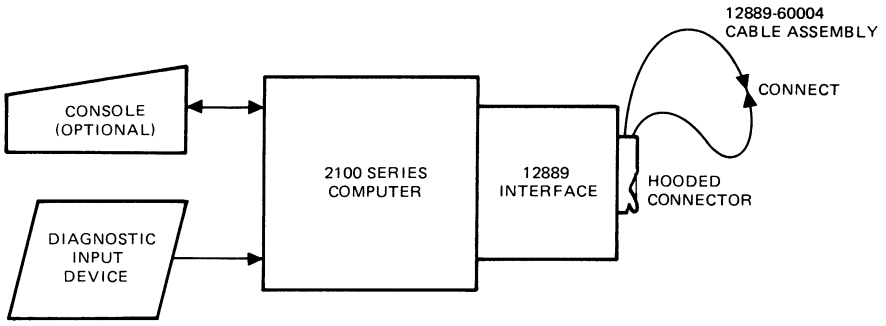
3-3. RESTARTING

The program may be restarted by setting the P Register to 2000_8. When restarting, select the S Register options according to Table 3-2, and press RUN.

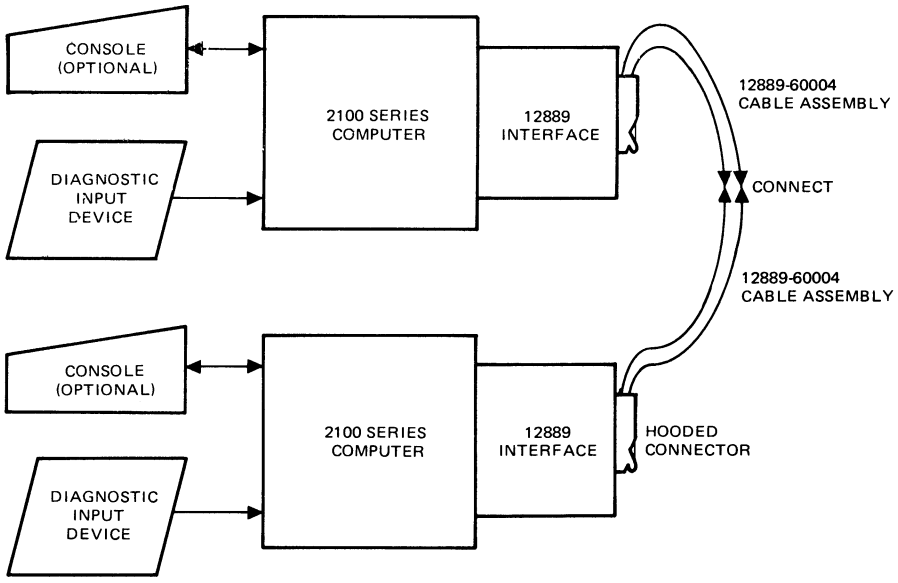
If a trap cell halt occurs ($1060nn_8$), the user must determine the cause of the interrupt or transfer of control to the location shown in the M Register or specified by *nn*. The program may need to be reloaded to continue.

Table 3-2. S-Register Test Options

Bits	Function When Set
0	Reserved
1	When set in Dual Mode, CPU acts as receiver. (When clear, CPU acts as transmitter.)
2	Abort receiver wait loop (first set then clear). If bit not cleared within 15 seconds, the CPU will abort the receive mode with bit set.
3-7	Reserved
8	Output all messages to line printer (line printer must have been configured in the configurator).
9	Abort at end of test with halt 102075_8. User may specify a new group of tests in the A Register (see Table 2-1).
10	Suppress non-error messages.
11	Suppress error messages.
12	Loop on all selected tests. Tests requiring manual intervention are omitted.
13	Loop on last test.
14	Suppress error halts.
15	Halt at end of each test with 102076_8. A Register holds test number.



a. Single CPU/single interface (single mode).



b. Dual CPU/dual interface (dual mode).

Figure 3-1. Setup and Connections for Single and Dual Operating Modes

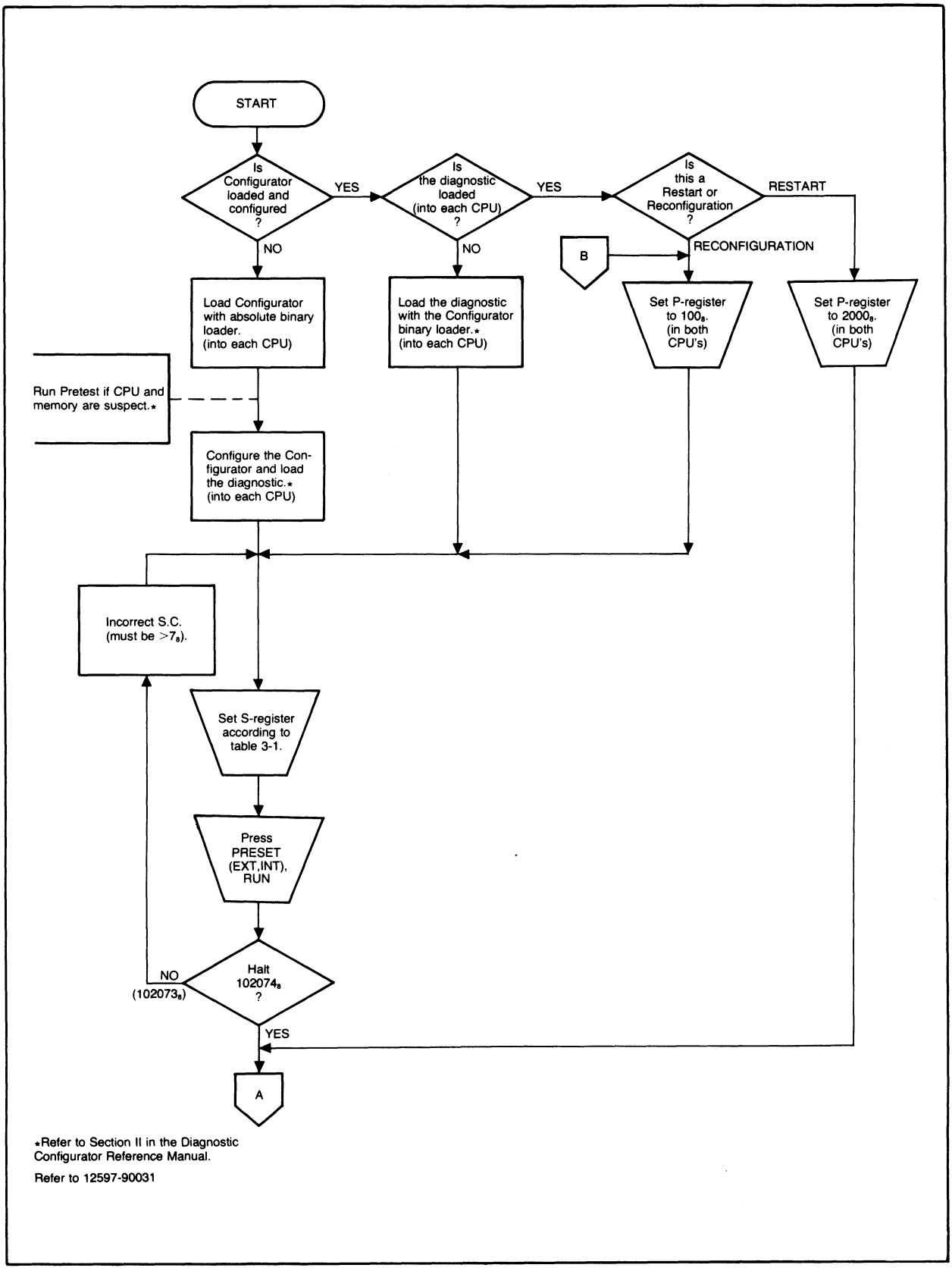


Figure 3-2. Operating Procedure Flowchart (Sheet 1 of 2)

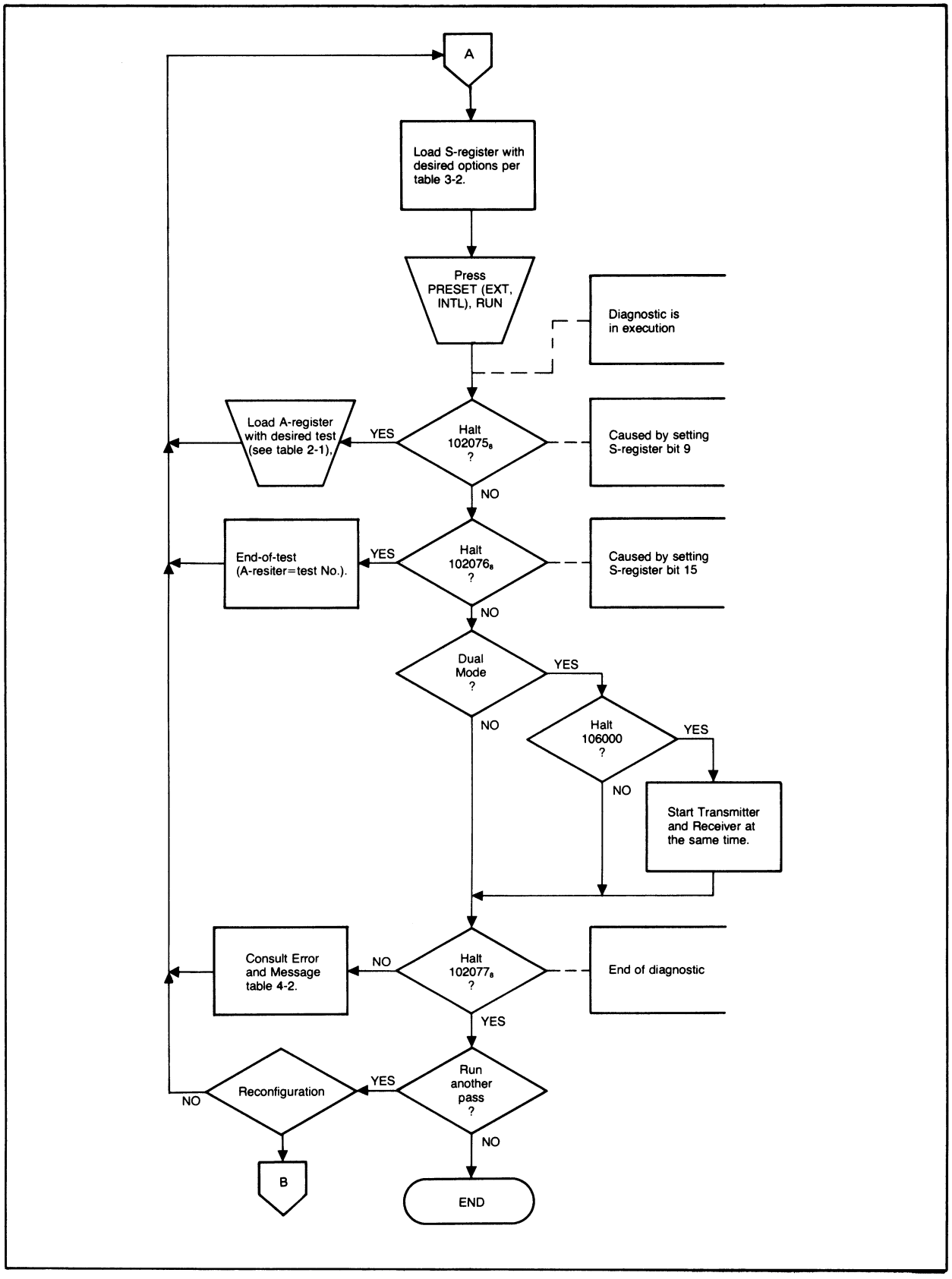


Figure 3-2. Operating Procedure Flowchart (Sheet 2 of 2)

DIAGNOSTIC PERFORMANCE

SECTION IV

4-1. TEST DESCRIPTION

The HP 12889A Hardwired Serial Interface diagnostic test sections are divided into two groups. Group one contains the Basic I/O Tests (tests 0-7) and group two contains PCA I/O Tests (tests 8-15). PCA I/O tests 13, 14 require two computers linked by two HP 12889A HSI's.

4-2. BASIC I/O TESTS

The basic I/O tests are described below:

Test 0

Print diagnostic header message (no test actually performed).

Test 1

A test is performed of the ability to clear, set, and test the interrupt system. The assembly language test sequence is the following:

```
STF 0
CLF 0
SFC 0
SFS 0
STF 0
SFC 0
SFS 0
```

Test 2

Test is performed for the absence of interrupt when the Test HSI Select Code (TSC) flag flip-flop (FF) is set, the TSC* control FF is set, and the interrupt system is off.

---

*TSC = Test Select Code.

Test 3

Test is performed for the ability to clear, set, and test the TSC flag. Assembly language test sequence is the following:

```
STF   TSC
CLF   TSC
SFC   TSC
SFS   TSC
STF   TSC
SFC   TSC
SFS   TSC
```

Test 4

Select code screen test is performed. The flag of every select code (10_8 through 77_8) except the TSC is set. A check is made to insure that the TSC flag is not set in the process.

Test 5

A test is performed of the ability of the TSC to interrupt. With the flag and control FF's set and the interrupt system on, there should be an interrupt on the TSC channel.

Test is then made for the interrupt to occur where expected. The interrupt should *not* occur before a string of priority-affecting instructions are executed.

Finally it is verified that another interrupt does not occur when the interrupt system is turned back on.

Test 6

A test is performed with the interrupt system on and the TSC control and flag FF's set to insure that no interrupt occurs following a *CLC TSC* instruction. A *CLC TSC* instruction should reset the TSC control FF. The check is also made to insure that a *CLC 0* instruction indirectly resets the TSC control FF.

Test 7

Test is performed to insure that the PRESET switch (External and Internal, if applicable) sets the TSC flag (POPIO signal line) and clears the interrupt system.

4-3. HSI I/O TESTS

Test 8

Checks that program transmit and program receive data modes function. Each transmit and each receive should set the HSI flag. A 100 word block of data is sent and received with the interrupt system off. The two blocks are compared to test for errors.

Test 9

The block of data is transmitted with the interrupt system disabled; this block is then received with the interrupt system enabled. The two blocks are compared to test for errors.

Test 10

The Watch Dog Timer is checked; this is the Wait On Overtime Function (WOOF). One word is transmitted and received with the interrupt system OFF. After a 15 ms. wait, the flag is tested and the status word is checked for the Watch Dog Timer WOOF Flag.

Test 11

The clear CRC bit in the command word is checked. The CRC is cleared, then transmitted and received between both computers or from one to self. The status word is then checked for the error bit which is set if a one is detected.

Test 12

CRC accumulation is checked at the transmit CPU and receive CPU. The received hardware accumulated CRC is compared to the software calculated CRC. Likewise the transmit hardware accumulated CRC is compared to the software calculated CRC. The receiver CPU responds to the data transmission by sending back its CRC check value (should be zero). This CRC check value is verified. The error bit in the status word is also checked.

Test 13

Check of the Hardware Intercomputer Handshake (HIH) mode is made. The handshake word will first be sent in burst mode. The control words will then be set up to transmit and receive the handshake. When this Computer Link and Synchronization Procedure (CLASP) is achieved, words are compared to detect errors. A 100 word block of data is then transmitted from sender to receiver in HIH mode and verified.

Test 14

The listen/repeat and address recognition functions are tested. The transmitting CPU sends all even octal addresses from 2 to 176. The receiving CPU starts out expecting octal address 2. When it is received, receiving CPU sends confirmation to transmitter and then increments by 2 its next expected address. This cycle is repeated until all addresses to 176 have been received and confirmed. Original transmitter CPU verifies all confirmations.

Test 15

This test checks the interruption of DMA (DCPC) with a tag one bit word received and the Interrupt Request (IRQ) bit set. The receive CPU is initialized to expect more words than the transmit CPU will send before the tag one bit word is sent. An interrupt should occur before completion of the DMA transfer. The DMA residue is also checked.

4-4. ERROR INFORMATION MESSAGES AND HALT CODES

Refer to Table 4-1 for a summary of the halt codes. Refer to Table 4-2 for a list of the diagnostic messages with their associated halt codes.

4-5. DIAGNOSTIC MESSAGES

There are two general categories of messages output to the operator: program/operator communication messages and interface test failure (error) messages. Table 4-2 lists diagnostic messages ordered by their likely order of appearance. Communication messages are coded with a "C," error messages with an "E" in the table. Communication messages are printed if switch register bit 10 is clear. Error messages are printed if S-Register bit 11 is clear. T (Memory Data) Register contents are listed in the HALT code column; A- or B-Register contents, if applicable, are also listed in the column enclosed by parentheses.

Table 4-1. Halt Code Summary

Halt Code*	Significance
102000	Initializing Halt for test 7. Press PRESET and RUN to continue.
1020*nn*	Test Failure Halt; *nn*= test number.
102073	Select Code Input Error, correct the input selection.
102074	Input Accepted (select code good).
102075	Halt to allow new test selection in A Register.
102076	End of Test number *n*; A Register holds *n*.
102077	End of complete pass through diagnostic; A Register hold last test selection.
106000	Start Receiver and Transmitter at the same time.
1060*nn*	Unexpected Trap Cell Halt; *nn*= Select Code of interrupting HSI I/O slot. This halt requires a restart at 2000_8 unless *nn*=0 in which case the halt is irrecoverable.

*Code in T (Memory Data) Register. Codes are given in octal.

Table 4-2. Error Information Messages and Halt

Message	C/E	Halt Code** T-Reg. (A- & B-Regs.)	Test	Meaning
HARDWIRED SERIAL INTERFACE DIAGNOSTIC DSN *nnnnnn*	*C*	–	0	Diagnostic header message *nnnnnn* = Current Diagnostic Serial Number
STF0-CLF0-SFS0-SFC0 FAILURE (A = X)	*E*	102001 (A-register = X)	1	Basic interrupt failed; A-register value X indicates type code: A = 1 means CLF0-SFS0 = 2 means CLF0-SFC0 = 3 means STF0-SFS0 = 4 means STF0-SFC0
INT AFTER CLF0	*E*	102002	2	Basic interrupt control failed
STF TSC-CLF TSC-* SFS TSC-SFC TSC FAILURE (A = X)	*E*	102003 (A-register = X)	3	Basic card control failure for Tested HSI Select Code (TSC); A-register value X indicates type code: A = 0 means SKF signal held up = 1 means CLF TSC-SFC TSC = 2 means CLF TSC-SFS TSC = 3 means STF TSC-SFC TSC = 4 means STF TSC-SFS TSC
STF *ss* SET TSC FLAG	*E*	102004 (A-register = *ss*)	4	Select code screen test failed; *ss* = select code that caused failure on interface PCA
INT DURING HOLD OFF INSTRUCTION	*E*	102005 (A-register = 1)	5	Interrupt occurred during I/O instruction or JMP
SECOND INT OCCURRED	*E*	102005 (A-register = 2)	5	TSC interrupted again after interrupts were turned back on
NO INT	*E*	102005 (A-register = 3)	5	No interrupt occurred with TSC CONTROL and FLAG SET and interrupt system ON. (Check for established priority string)
INT INCORRECT	*E*	102005 (A-register = 4)	5	Interrupt system did not handle interrupt properly

*TSC = Test Select Code.
**Octal Values.

Table 4-2. Error Information Messages and Halt (Continued)

Message	C/E	Halt Code** T-Reg. (A- & B-Regs.)	Test	Meaning
CLC 0 OR CLC TSC* FAILED (A = *X*)	*E*	102006 (A-register = *X*)	6	Interrupt occurred after CLC0 or CLC TSC; value *X* indicates type code: *X* = 1 means CLC TSC = 2 means CLC0
PRESS PRESET (EXTERNAL & INTERNAL), PRESS RUN	*C*	102000	7	Operator keys in PRESET at computer operator panel.
FLAG NOT SET AFTER POPIO	*E*	102007 (A-register = 1)	7	PRESET did not set the flag
INT SYSTEM NOT CLEARED AFTER PRESET	*E*	102007 (A-register = 2)	7	Manual entry of PRESET did not clear interrupt
BASIC I/O (TESTS 1-7) COMP	*C*	—	—	All Basic I/O tests (1-7) selected have been completed
START RCVR AND XMTR AT SAME TIME	*C*	106000	—	Operator is notified to start both computers at same time
TEST *nnnnn* COMPLETED	*C*	—	8-15	Operator is notified that test *nnnnn* is passed
TEST ABORT	*C*	1020*nn* (A-register = -1) (B-register = -1)	8-15	Test aborted due to setting of switch register bit 2; *nn* = test number
FLAG NOT SET ON DATA TRANSFER	*E*	1020*nn* (A-register = -1)	8-15	Data transmit or receive did not set this flag; *nn* = test number
FLAG SET ON DATA TRANSFER BY STATUS WORD = *n*	*E*	1020*nn* (A-register holds value *n*)	8-15	Status word flag set on data transfer; *n* is octal status word; *nn* = test number
RCVR WAIT LOOP ABORTED	*E*	1020*nn* (A-register = 0)	8,9,10, 12,13,14	Waiting loop of receiving computer was aborted either by timeout (approximately 4 min.) or switch register bit 2 set *nn* = test number
ERROR IN DATA TRANSFER	*E*	1020*nn* (A-register = 1)	8,9, 12,13	The block of received data does not compare with memory resident transmit data; *nn* = test number

*TSC = Test Select Code.
**Octal Values.

Table 4-2. Error Information Messages and Halt (Continued)

Message	C/E	Halt Code** T-Reg. (A- & B-Regs.)	Test	Meaning
NO INT IN DATA TRANSFER	*E*	102011 (A-register = 7)	9	Interrupt service routine timed out
NO WATCHDOG TIMEOUT (A = *X*)	*E*	102012 (A-register = *X*)	10	Watchdog error after 15 ms. wait; Value *X* indicates type code: A = 1 means flag not set = 2 means bits not set in status word
CLEAR CRC ERROR	*E*	102013 (A-register = 0)	11	Error bit set in status word after clear CRC (Cyclic Redundancy Check)
THIS CONFIGURATION CANNOT RUN THIS TEST	*C*	1020*nn* (A-register = 0) B-register = -1)	13-15	Requested test requires two CPU's or DMA (DCPC) while present configuration does not include them; *nn* = test number
c CRC SHOULD BE *n*, IS *nn*	*E*	102014 (A-register = value of n; B-register = value of *nn*)	12	Calculated CRC and transmitted CRC do not compare; *c* = T, message is from transmitting CPU *c* = R, message is from receiving CPU
CRC TO CRC EQUAL *n*	*E*	102014 (A-register = value of n; B-register = 0)	12	Reception of CRC from transmitter did not set receiver CRC to zero; *n* = value of receiver CRC sent to transmitter
TEXT CRC ERROR	*E*	102014 (A-register = 2)	12	Error bit set in status word after receiver CRC sent to transmitter
HANDSHAKE ERROR— SHOULD BE *n*, IS *nn*	*E*	102015 (A-register = 1)	13	Handshake word received does not compare with word transmitted
LISTEN-REPEAT ERROR: SENT *n* RECEIVED *nn*	*E*	102016 (A-register holds *n*; B-register holds *nn*)	14	Transmitted address does not equal repeated address; *n* = transmitted address *nn* = repeated address
TAG BIT SET WITH ADDRESS CONFIRMATION	*E*	102016 (A-register = 0)	14	Tag bit should not be set on reception of address confirmation

**Octal Values.

Table 4-2. Error Information Messages and Halt (Continued)

Message	C/E	Halt Code** T-Reg. (A- & B-Regs.)	Test	Meaning
RECOGNITION ERROR: SHOULD BE *n*, IS *nn*	*E*	102016 (A-register = *n*, B-register = *nn*)	14	Address that caused interrupt and sent as confirmation not equal to transmitted address; *n* = transmitted address *nn* = confirmation address
NO RECOGNITION-ADDRESS *n*	*E*	102016 (A-register = n; B-register = 0)	14	*n* = address that did not reply with confirmation address
NO INT IN LISTEN-REPEAT	*E*	102016 (A-register = 1; B-register = 1)	14	Intercomputer communication terminated; either switch register 2 used to abort the interrupt wait loop or time-out (approximately 4 min.) occurred
TAG ONE WORDS DO NOT COMPARE	*E*	102017 (A-register = 1)	15	Word that caused interrupt not equal to special word sent
TAG BIT NOT SET IN STATUS WORD	*E*	102017 (A-register = 2)	15	Word that caused interrupt did not set tag bit in status word
ABORTED DMA TRANSFER	*E*	102017 (A-register = 3)	15	DMA (DCPC) transmit routine timed out and caused abort
NO INT WHILE DMA	*E*	102017 (A-register = 4)	15	Switch register bit 2 was set to abort DMA (DCPC) transmission interrupt wait loop or wait loop timed out and caused abort
HAD A DMA INT	*E*	102017 (A-register = 5)	15	DMA (DCPC) interrupted when not enabled
RESIDUE WRONG; = *n*, SHOULD BE 17716	*E*	102017 (A-register = *n*, B-register = 17716)	15	*n* = incorrect DMA (DCPC) residue
PASS *n*	*C*	—	—	Pass through all selected tests of diagnostic completed; *n* = pass number
DIAG COMPLETE, PASS *nnnnnn*	*C*	102077	—	Diagnostic run completed. Switch Reg. options may be changed. (A-Reg. has pass count). To continue press RUN

**Octal Values.