HEWLETT PACKARD

HP 1000 SERIES INTERFACE MODEL 10278B

Model 10278B

OPERATING NOTE/JULY 1981

1. DESCRIPTION.

2. The HP Model 10278B Interface provides a method for easy, fast connection between a Hewlett-Packard Logic Analyzer and a HP 1000 Minicomputer. The interface boards plug directly into HP 1000 slots and allows access to all signals of interest on the bus. Circuits on the interface boards generate a clock signal for the Logic Analyzer from the synchronous bus activity which allows address and data information to be captured. In addition, switches on the boards provide qualification of bus activity so that reads, writes, I/O transactions, memory transactions, or DMA transfers can be selectively captured for detailed analysis. Refer to table 1 for complete specifications.

3. INTERFACE CONNECTIONS.

4. Ribbon cables from the HP Model 10277B (described in paragraph 6) may be connected to the 10278B Interface Boards from the minicomputer, or data and clock probe leads can be connected to pins on the interface connectors.

NOTE

Follow the HP 1000 Series Service Manual instructions for removal and installation of printed circuit boards when using the Model 10278B.

5. ACCESSORY AVAILABLE.

6. For maximum measurement flexibility, an HP Model 10277B Option 003 General Purpose Probe Interface is available for easy connection to the 10278B Interface. Connection to the system under test is accomplished with two ribbon cables between the interfaces, and the Logic Analyzer probe pods plug directly into the 10277B. Changing of electrical configurations for analysis of address and data flow or bus arbitration is achieved by simply changing the A and B cables to be plugged into J1A and J1B, or J2A and J2B, or J3A and J3B. see table 2 for the three choices.

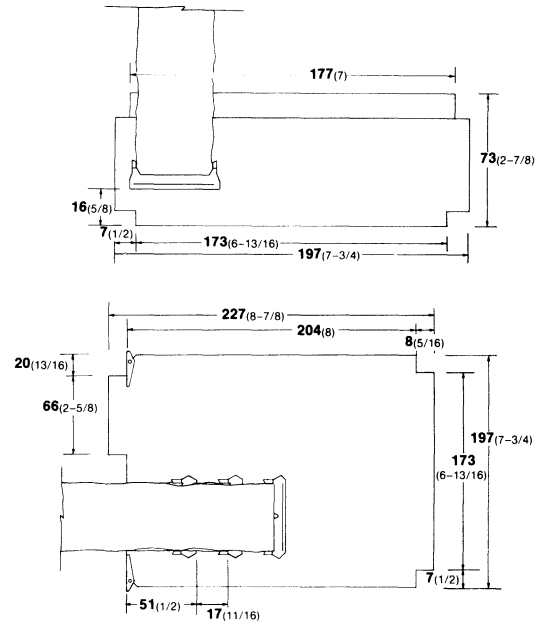
7. APPLICATIONS.

8. SOFTWARE DEVELOPMENT. The 10278B combined with a Logic Analyzer becomes a very powerful software debugging tool because it captures program state flow in real time and permits analysis of software timing loops. Once the software is debugged, optimization can be achieved via information available from the Logic Analyzer.

9. SERVICE AND MAINTENANCE. System signals can be accessed quickly by simply plugging the 10278B into the minicomputer backplane. Detailed analysis of program execution or the bus arbitration process with elapsed time intervals between events permits rapid troubleshooting with minimum computer downtime when software techniques are marginal or cannot be used.

10. PRODUCTION. The ability to analyze program execution during integration allows you to observe how the system reacts as peripherals are added. By directing the analyzer to trace only the activity to a specific peripheral, problems can be detected and isolated.

Table 1. Specifications



BUS LOADING: logical address bus, physical address bus and data bus, IRSTF, $\overline{\text{P5NF}}$ = 1 standard TTL load. All other lines = < 1/4 standard TTL load.

GENERAL

Power: 3000 mA maximum at 5 Vdc (nominally 1500 mA), supplied by the minicomputer.

Dimensions: see outline drawing.

Operating Environment: temperature, +5°C to +40°C; humidity to 95% relative humidity at 40°C; altitude 4600 m (15 000 ft); vibration, vibrated in three planes for 15 min each with 0.3 mm (0.015 in) excursions, 10 to 55 Hz.

Operating Note Part No. 10278-90902
Microfiche Part No. 10278-90802

For more information, Call Your Local HP Sales Office or, in U.S., East (201) 265-5000. Midwest (312) 677-0400. South (404) 436-6181 West (213) 877-1282. Or, write: Hewlett-Packard, 1501 Page Mill Road, Palo Alto, California 94304. In Europe, Post Office Box 85, CH-1217 Meyrin 2, Geneva, Switzerland. In Japan, YHP, 1-59-1, Yoyogi, Shibuya-ku, Tokyo, 151.

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11. HARDWARE DEVELOPMENT. During the design of new devices, interactions on the bus can be viewed in real time. This permits checking handshake protocol and tracing program execution while recording the times to perform various functions.

12. INSTALLATION.

13. Install the 10278B Interface in the HP 1000 Series Computer as follows:

a. Turn power off to the HP 1000 system.

b. Connect the shortest of the three ribbon cables supplied to J2 on the 10278-66504 A1 board, making sure to align pin 1 of the board connector and pin 1 of the ribbon cable connector (indicated by a triangle molded into each connector).

c. Remove the memory protect card from the HP 1000 mainframe and install the A1 board in its place.

d. Plug the memory protect card into the female socket (labeled J1) of the A1 board.

e. Remove the flat ribbon cable bus from the front left side of the memory card stack.

f. If the memory controller board is not in the bottom slot of the HP 1000 card cage, move it to that location.

g. The slot directly above the memory controller board in the card cage is used for the 10278-66505 A2 board. If this slot has a memory card installed, remove the card and re-install it in the next available slot up.

h. Connect the two longer cables supplied (labeled "A" and "B") to JA and JB on the A2 board, making sure to align pin 1 of the board connector and pin 1 of the ribbon cable connector on both cable sets. Verify that cable "A" is connected to JA and cable "B" is connected to JB.

i. Connect the cable from the A1 board into J2 of the A2 board, making sure that pin 1 of the board connector and pin 1 of the ribbon cable connector are aligned.

j. Install the A2 board in the slot directly above the memory controller.

k. Re-install the flat ribbon cable bus on the front left edge of the memory card stack, making sure it seats properly and that all cards are engaged.

l. Connect the cables marked "A" and "B" to their respective locations on the 10277-66509 board. See table 2 to select the desired group of signals to be sent to the analyzer.

14. PRINCIPLES OF OPERATION.

15. BLOCK DIAGRAM DESCRIPTION.

16. The 10278B is an HP Logic Analyzer Interface for HP 1000 M/E/F Computers. The 10278B provides signal buffering, clock qualification, data storage and convenient signal access.

17. The circuitry of the 10278B is divided between two printed circuit boards. The A1 board buffers the input/output select code and control lines. These signals are then sent to the A2 board where the majority of the cicuitry is located. (See figure 1).

18. Memory, DMA, and other control lines are first buffered and then combined with the input/output control lines from the A1 board and clock qualify switches. Signals generated in the control section determine when the address and data latches capture information and when to clock that information into the analyzer.

19. The logical address bus (MB0-MB150) is monitored by the logical address latch and under direction of the control section captures valid address at the appropriate time. This information is multiplexed with the input/output code from the A1 board to give memory address or input/output address during memory or I/O transactions respectively.

20. The physical memory address after the memory expansion module (physical address (A0-A19)) is captured by the physical address latch. Similarly, the data bus (SB0-SB15) is latched by the data bus latch. All of this information, address, data, and status, is then made available to the analyzer and a clock signal is provided to enter the information into the analyzer.

21. DETAILED CIRCUIT DESCRIPTION.

22. There are two boards in the 10278B. The A1 board buffers signals necessary to monitor input/output transactions and supplies them to the A2 board. It also acts as an extender board and passes all bus signals through to the memory protect board. (See figure 4).

23. The A2 board receives all other necessary signals through its backplane connector (P1) and contains the majority of the 10278B circuitry. (See figure 6).

24. Inverting buffer U2 on the A1 board buffers the IOI and IOO (input and output transfer signals) and sends these signals to the A2 board through the J1 connector. Non-inverting buffer U4 buffers the I/O select code (SCB0-SCB5) and also sends it to the A2 board. U1 and U3 are resistor termination networks to reduce interference noise on these lines.

Table 2. Signal Connection Using Option 003 Interface Card

TO 1610B			FROM 10278B VIA 10277B OPTION 003 INTERFACE CARD											
POD-PIN	SIG A1J4	PIN	J1A	PIN	J1B	PIN	J2A	PIN	J2B	PIN	J3A	PIN	J3B	PIN
CLK-0	CLK J	17	MEM CLOCK	5		–	MEM CLOCK	5		–	MEM CLOCK	5		–
CLK-1	CLK K	19		–	COMBINED CLOCK	5		–	COMBINED CLOCK	5		–	COMBINED CLOCK	5
CLK-2	CLK L	21	I/O CLOCK	3		–	I/O CLOCK	3		–	I/O CLOCK	3		–
CLK-3		–		–		–		–		–		–		–
CLK-4	QUAL-0	25	DMA	1		–	PHYSICAL A16	40		–		–		–
CLK-5	QUAL-1	27	OPCODE	14		–	PHYSICAL A17	39		–		–		–
CLK-6	QUAL-2	29	MEM I/O	16		–	PHYSICAL A18	38		–		–		–
CLK-7	QUAL-3	31		–		–	PHYSICAL A19	36		–		–		–
CLK-8		–		–		–		–		–		–		–
CLK-9		–		–		–		–		–		–		–
CLK-10	GND	†		†		†	GND	†	GND	†	GND	†	GND	†
POD1-0	DATA 0	48		–	LOGICAL A0	40		–	LOGICAL A0	40		–	LOGICAL A0	40
POD1-1	DATA 1	46		–	LOGICAL A1	39		–	LOGICAL A1	39		–	LOGICAL A1	39
POD1-2	DATA 2	44		–	LOGICAL A2	38		–	LOGICAL A2	38		–	LOGICAL A2	38
POD1-3	DATA 3	42		–	LOGICAL A3	36		–	LOGICAL A3	36		–	LOGICAL A3	36
POD1-4	DATA 4	34		–	LOGICAL A4	34		–	LOGICAL A4	34		–	LOGICAL A4	34
POD1-5	DATA 5	38		–	LOGICAL A5	32		–	LOGICAL A5	32		–	LOGICAL A5	32
POD1-6	DATA 6	36		–	LOGICAL A6	30		–	LOGICAL A6	30		–	LOGICAL A6	30
POD1-7	DATA 7	34		–	LOGICAL A7	28		–	LOGICAL A7	28		–	LOGICAL A7	28
POD1-8														
POD1-9														
POD1-10	GND	†	GND	†	GND	†	GND	†	GND	†	GND	†	GND	†
POD2-0	DATA 0	32		–	LOGICAL A8	26		–	LOGICAL A8	26		–	LOGICAL A8	26
POD2-1	DATA 1	30		–	LOGICAL A9	24		–	LOGICAL A9	24		–	LOGICAL A9	24
POD2-2	DATA 2	28		–	LOGICAL A10	22	PHYSICAL A10	17		–	PHYSICAL A10	17		–
POD2-3	DATA 3	26		–	LOGICAL A11	20	PHYSICAL A11	15		–	PHYSICAL A11	15		–
POD2-4	DATA 4	24		–	LOGICAL A12	18	PHYSICAL A12	13		–	PHYSICAL A12	13		–
POD2-5	DATA 5	22		–	LOGICAL A13	16	PHYSICAL A13	11		–	PHYSICAL A13	11		–
POD2-6	DATA 6	20		–	LOGICAL A14	14	PHYSICAL A14	9		–	PHYSICAL A14	9		–
POD2-7	DATA 7	18		–	*LOGICAL OR R/$\overline{W}$ A15	12	PHYSICAL A15	7		–	PHYSICAL A15	7		–
POD2-8														
POD2-9														
POD2-10	GND	†	GND	†	GND	†	GND	†	GND	†	GND	†	GND	†
POD3-0	DATA 0	16		–	D0	37		–	D0	37	PHYSICAL A16	40		–
POD3-1	DATA 1	14		–	D1	35		–	D1	35	PHYSICAL A17	39		–
POD3-2	DATA 2	12		–	D2	33		–	D2	33	PHYSICAL A18	38		–
POD3-3	DATA 3	10		–	D3	31		–	D3	31	PHYSICAL A19	36		–
POD3-4	DATA 4	8		–	D4	29		–	D4	29		–		–
POD3-5	DATA 5	6		–	D5	27		–	D5	27		–		–
POD3-6	DATA 6	4		–	D6	25		–	D6	25		–		–
POD3-7	DATA 7	2		–	D7	23		–	D7	23		–		–
POD3-8														
POD3-9														
POD3-10	GND	†	GND	†	GND	†	GND	†	GND	†	GND	†	GND	†
POD4-0	DATA 0	1		–	D8	21		–	D8	21		–		–
POD4-1	DATA 1	3		–	D9	19		–	D9	19		–		–
POD4-2	DATA 2	5		–	D10	17		–	D10	17		–		–
POD4-3	DATA 3	7		–	D11	15		–	D11	15		–		–
POD4-4	DATA 4	9		–	D12	13		–	D12	13	DMA	1		–
POD4-5	DATA 5	11		–	D13	11		–	D13	11	OPCODE	14		–
POD4-6	DATA 6	13		–	D14	9		–	D14	9	MEM I/O	16		–
POD4-7	DATA 7	15		–	D15	7		–	D5	7		–	R/$\overline{W}$	12
POD4-8														
POD4-9														
POD4-10	GND	†	GND	†	GND	†	GND	†	GND	†	GND	†	GND	†
BNCSIG A1JC	TRIG OR MEAS ENABLE	–		–	TRIG OR MEAS ENABLE	–		–	TRIG OR MEAS ENABLE	–		–	TRIG OR MEAS ENABLE	3

MEM/IO = 1 MEANS MEMORY CYCLE
SELECT NEGATIVE CLOCK EDGES
*SELECTED BY S5
† GND PINS ON A1J4 (35, 37, 39, 41, 43, 45, 47, 49, 50)
NOTE: CR1, CR2, CR3 ARE CONNECTED TO CLOCKS J, K AND L WITH CATHODES TO GROUND

25. The control section of the 10278B is located on the A2 board. It receives signals which indicate whether the current transaction on the bus is read or write, input or output, CPU, or DMA and timing signals to control these transfers. Outputs from this control section determine when address, data and status signals are to be captured from the computer buses and when to transfer this information to the analyzer.

26. The logical address bus (MB0-MB15) is latched by U28 and U29 on the falling edge of either the $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ signal. This control line is generated by parts of U32 and U23.

27. The physical memory address (A0-A19) enters through the J1 connector and is latched by U2-U4. Parts of U9 and U22 generate a latch enable signal that will latch the address on the rising edge of the $\overline{\text{WRITE}}$ signal during a write operation. During a read operation address is latched on the falling edge of $\overline{\text{P5NF}}$ following a $\overline{\text{READ}}$ pulse.

28. The data bus (SB0-SB15) is latched by U30 and U31. Parts of U14 and U23 instruct the latches to capture data on the rising edge of every $\overline{\text{P4NF}}$ signal.

29. During an input or output cycle the select code is sent to the analyzer in place of the logical address. This multiplexing is performed by U16, U17, U24 and U25. A signal generated by U13-U15 indicates whether the current cycle is I/O or memory and controls the multiplexers.

30. A signal to clock the analyzer is generated by U19-U21. This clocking occurs on the rising edge of $\overline{\text{TEN}}$ during a read operation or the rising edge of $\overline{\text{WRITE}}$ during a write operation. During input or output cycles the analyzer is clocked on the falling edge of IOI or IOO respectively. Switches S1-S4 allow the user to qualify the types of cycles to reach the analyzer. S1 selects between DMA and non-DMA cycles and S2 selects between memory and I/O cycles. The center switch position is a "don't care" and both types of cycles will be clocked into the analyzer. By sending the measurement enable signal from the 1610 back to the 10278B the type of cycle selected can be different before the analyzer triggers and after. When this is done S3 and S4 perform a similar selection for post-trigger. Furthermore, the actual gating is done by U6, U7, U11 and U12 to make qualification possible.

31. REPLACEABLE PARTS.

32. Replaceable parts are illustrated in figures 3 and 5 and listed in table 3. To order a replaceable part from Hewlett-Packard, address the order to the nearest HP Sales/Service Office. Include the interface model number, reference designation of the part and the HP part number. If a part is not listed, provide a complete description of the part, including function and location.

Table 3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	10278-66504	1	8	HP 1000 BUFFER EXTENDER BOARD	28480	10278-66504
A1C1-4	0160-2055	4	9	CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
A1C5	0180-0229	1	7	CAPACITOR-FXD 33μF +-10% 10VDC TA	56289	150D336X9010B2
A1F1	2110-0568	1	2	FUSE 4 AMP 125V .281x.093	75915	276004
A1J1	1251-6018	1	6	CONNECTOR-PC EDGE 86-PIN	28480	1251-6018
A1J2	1251-7138	1	3	CONNECTOR 40-PIN	28480	1251-7138
A1U1	1810-0182	1	9	NETWORK RESISTOR 14-DIP MULTI-VALVE	28480	1810-0182
A1U2	1820-1633	1	8	IC-BFR TTL S INV OCTL 1-INP	01295	74S240N
A1U3	1810-0183	1	0	NETWORK-RESISTOR 9-SIP 6.0K OHMx7	28480	1810-0183
A1U4	1820-1624	1	7	IC BFR TTL S OCTL 1-INP	01295	74S241N
A2	10278-66505	1	9	HP 1000 INTERFACE BOARD	28480	10278-66505
A2C1-3	0160-2055	28	9	CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
A2C5-8	0160-2055		9	CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
A2C10-17	0160-2055		9	CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
A2C18-20	0160-4789	3	0	CAPACITOR-FXD 15PF +-5% 100VDC CER 0 +-30	28480	0160-4789
A2C21-27	0160-2055		9	CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
A2C28	0180-0229	1	7	CAPACITOR-FXD 33μF +-10% 10VDC TA	56289	150D336X9010B2
A2C29-34	0160-2055		9	CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
A2F1	2110-0568	2	1	FUSE 4 AMP 125V .281x.093	75915	276004
A2JA	1251-7138		3	CONNECTOR 40-PIN	28480	1251-7138
A2JB	1251-7138		3	CONNECTOR 40-PIN	28480	1251-7138
A2J2	1251-7138	3	3	CONNECTOR 40-PIN	28480	1251-7138
A2R1	0683-2225	1	3	RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A2R2	0684-4711	1	8	RESISTOR 470 10% .25W FC TC=-400/+600	01121	CB4711
A2U1	1810-0280	1	8	NETWORK-RES 10-SIP 10.0K OHMx9	01121	210A103
A2U2	1820-1676	5	9	IC LCH TTL S D-TYPE OCTL	01295	74S373N
A2U3	1820-1676		9	IC LCH TTL S D-TYPE OCTL	01295	74S373N
A2U4	1820-1676		9	IC LCH TTL S D-TYPE OCTL	01295	74S373N
A2U5				NOT USED		
A2U6	1820-0689	2	4	IC-GATE TTL S AND DUAL 4-INP	01295	74S22
A2U7	1820-0689	2		IC-GATE TTL S AND DUAL 4-INP	01295	74S22
A2U8	1820-0694	9	1	IC-GATE TTL S X-OR QUAD 2-INP	01295	74S86
A2U9	1820-0693	8	3	IC-FF TTL S D-TYPE POS EDGE TRIG	01295	74S74
A2U10				NOT USED		
A2U11	1820-0689	2		IC-GATE TTL S AND DUAL 4-INP	01295	74S22
A2U12	1820-0689	2		IC-GATE TTL S AND DUAL 4-INP	01295	74S22
A2U13	1820-0693	8		IC-FF TTL S D-TYPE POS EDGE TRIG	01295	74S74
A2U14	1820-1367	5	1	IC-GATE TTL S AND QUAD 2-INP	01295	74S08
A2U15	1820-0681	4	2	IC-GATE TTL S NAND QUAD 2-INP	01295	74S00
A2U16	1820-1077	4	4	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	74S157N
A2U17	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	74S157N
A2U18	1810-0182	9	1	NETWORK-RESISTOR 14-PIN-DIP .1-PIN-SPCG	01295	314E221331
A2U19	1820-1322	2	1	IC-GATE TTL S NOR QUAD 2-INP	01295	74S02
A2U20	1820-0693	8		IC-FF TTL S D-TYPE POS EDGE TRIG	01295	74S74
A2U21	1820-0683	6	1	IC-INV TTL S HEX 1-INP	01295	74S04
A2U22	1820-0681	4		IC-GATE TTL S NAND QUAD 2-INP	01295	74S00
A2U23	1820-1449	4	1	IC-GATE TTL POS-OR QUAD 2-INP	01295	74S32
A2U24	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	74S157N
A2U25	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	74S157N
A2U26	1810-0277	3	1	RESISTOR PACK 10-PIN-SIP .1-PIN-SPCG	01121	210A222
A2U27	1820-1633	8	1	IC-BFR TTL S INV OCTL 1-INP	01295	74S240
A2U28	1820-1677	0	2	IC-FF OCTAL D-TYPE TTL 3-STATE OUTPUT	01295	74S374
A2U29	1820-1677	0		IC-FF OCTAL D-TYPE TTL 3-STATE OUTPUT	01295	74S374
A2U30	1820-1676	9		IC LCH TTL S D-TYPE OCTL	01295	74S373N
A2U31	1820-1676	9		IC LCH TTL S D-TYPE OCTL	01295	74S373N
A2U32	1820-1440	5	1	IC-GATE TTL QUAD S-R LATCHES	01295	74LS279

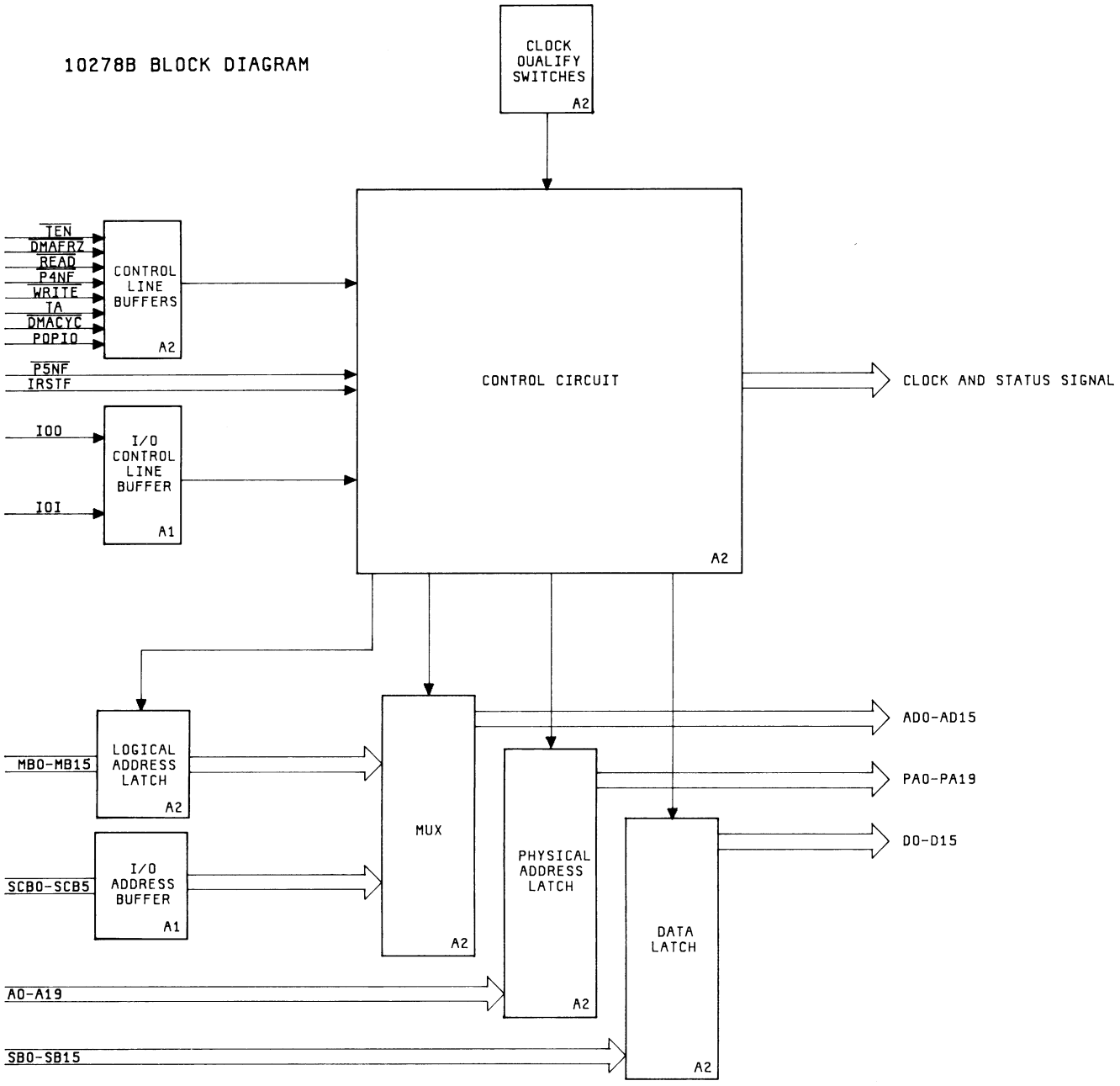


Figure 1. Model 10278B Block Diagram

Table 4. Signal Mnemonics

Mnemonic	Description
A0-19	ADDRESS 0-19.
AD0-15	ADDRESS 0-15.
BDMACYC	BUFFERED DIRECT MEMORY ACCESS CYCLE.
BDMAFRZ	BUFFERED DIRECT MEMORY ACCESS FREEZE.
BP4NF	BUFFERED PHASE 4 CLOCK NON-FREEZE.
$\overline{\text{BPOPIO}}$	BUFFERED POWER ON PRESET I/O (low true).
BREAD	BUFFERED READ.
BSCB0-5	BUFFERED SELECT CODE BUS 0-5.
$\overline{\text{BTA}}$	BUFFERED TIME A (low true) Indicates the current time period.
BTEN	BUFFERED T-REGISTER ENABLE (high true).
BWRITE	BUFFERED WRITE (high true).
CLK	CLOCK.
D0-15	DATA 0 - 15.
$\overline{\text{DMACYC}}$	DIRECT MEMORY ACCESS CYCLE (low true) parallels the actual data transfer and primarily freezes the control processor during T2, 3, 4 and 5, insuring no interfering activities. Disables CPU from driving SCB.
$\overline{\text{DMAFRZ}}$	DIRECT MEMORY ACCESS FREEZE (low true). From the DMA Board. Indicates that DMA is using the S-BUS and the CPU is frozen. Prevents error-checking the S-BUS until the CPU has control of it again.
$\overline{\text{DMAOP}}$	DIRECT MEMORY ACCESS OPERATION (low true).
DMA ONLY	DIRECT MEMORY ACCESS ONLY.
I/O	INPUT/OUTPUT.
$\overline{\text{IRSTF}}$	INSTRUCTION REGISTER STORE (low true) From CPU. Indicates that data is being loaded into the Instruction Register on the CPU, and is currently present on the S-BUS. Used to setup error-detection logic for the current instruction. Lasts one T-period, broken up by freeze time.
IOO+IOI	I/O OUTPUT OR I/O INPUT.
MB0-15	M-BUS 0-15, HP 1000 16-bit address bus.
MEAS ENBL	MEASURE ENABLE (high true); Logic analyzer signal signifying to the system under test that the analyzer is ready to make a measurement.
MEM	MEMORY.
NO DMA	NO DIRECT MEMORY ACCESS.
OUT	OUTPUT.

Table 4. Signal Mnemonics (Cont'd)

Mnemonic	Description
OP CODE	OPERATION CODE.
$\overline{\text{P4NF}}$	PHASE 4 CLOCK NON-FREEZABLE (low true) HP 1000 clock period.
$\overline{\text{POPIO}}$	POWER ON PRESET I/O (low true).
$\overline{\text{READ}}$	READ (low true) Memory begins a read operation on the falling edge of this signal.
R/$\overline{\text{W}}$	READ/WRITE Selects either read or write mode (read when high and write when low).
SB0-15	S BUS 0-15, HP 1000 16-bit data bus.
TA	TIME A (high true) Indicates the current time period of the HP 1000.
$\overline{\text{TEN}}$	T-REGISTER ENABLE (low true). Gates the read memory data onto the S-bus after the READ signal has become inactive in a read cycle.
$\overline{\text{WRITE}}$	WRITE (low true) Indicates a write cycle.
$\overline{\text{WRT}}$	WRITE (low true) Memory begins a write cycle on the falling edge of this signal.

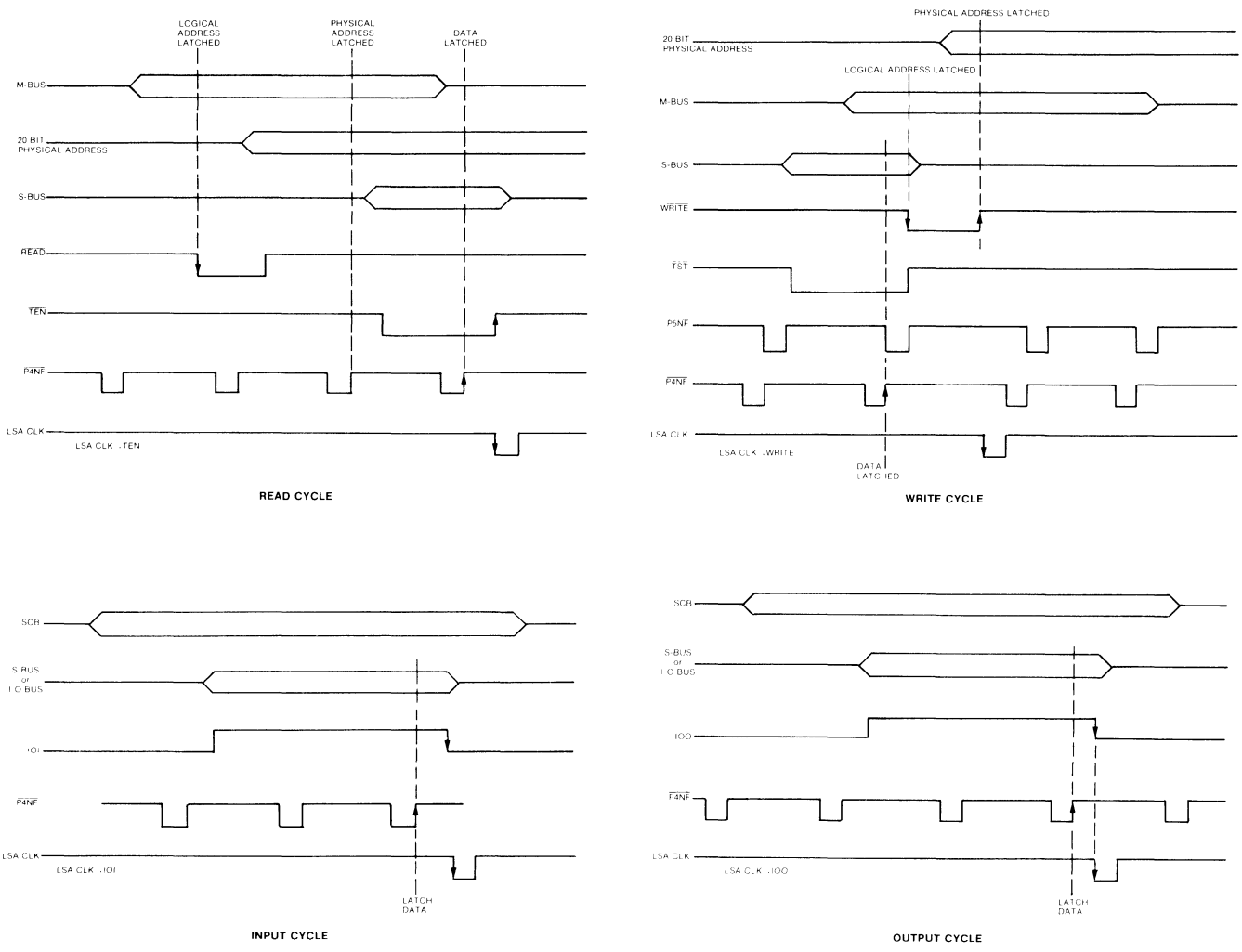


Figure 2. Timing Diagrams

Table 5. A1 Control Signal Connections

Pin	J1	J2	P1
1	GND	_____	GND
2	GND	_____	GND
3	SB15	_____	SB15
4	MB15	_____	MB15
5	MBCND	_____	MPCND
6	RME	_____	RME
7	SB14	_____	SB14
8	MB14	_____	MB14
9	READ	_____	READ
10	DMAFRZ	_____	DMAFRZ
11	SB13	_____	SB13
12	MB13	_____	MB13
13	CTL5	_____	CTL5
14	MPV	_____	MPV
15	SB12	_____	SB12
16	MB12	_____	MB12
17	HLTPE	_____	HLTPE
18	MPINTON	_____	MPINTON
19	SB11	_____	SB11
20	MB11	_____	MB11
21	P4NF	_____	P4NF
22	SCB0	_____	SCB0
23	SB10	BSCB1	SB10
24	MB10	_____	MB10
25	IRSTF	BSCB5	IRSTF
26	SCB1	_____	SCB1
27	SB9	BSCB0	SB9
28	MB9	_____	MB9
29	FLGS	BIOO	FLGS
30	SCB2	_____	SCB2
31	SB8	BSCB4	SB8
32	MB8	_____	MB8
33	SCB3	BSCB2	SCB3
34	SCB4	_____	SCB4
35	SB7	BIOI	SB7
36	_____	_____	_____
37	MB7	_____	MB7
38	SB6	_____	SB6
39	+5V	_____	+5V
40	+5V	_____	+5V
41	ENF	_____	ENF
42	MB6	_____	MB6
43	+12M	_____	+12M
44	+12M	_____	+12M
45	SB5	_____	SB5
46	MB5	_____	MB5
47	-2V	_____	-2V
48	-2V	_____	-2V
49	SB4	_____	SB4
50	MB4	_____	MB4
51	SCB5	_____	SCB5
52	MB3	_____	MB3
53	SB3	_____	SB3
54	MB2	_____	MB2
55	SIR	_____	SIR
56	MPCK	_____	MPCK
57	FTCH	_____	FTCH

Table 5. A1 Control Signal Connections (Cont'd)

Pin	J1	J2	P1
58	SB2	_____	SB2
59	PE	_____	PE
60	RSPE	_____	RSPE
61	MB1	_____	MB1
62	SFS	_____	SFS
63	IOI	_____	IOI
64	SB1	_____	SB1
65	STC	_____	STC
66	IOGSP	_____	IOGSP
67	IOO	_____	IOO
68	IOG	_____	IOG
69	-12M	_____	-12M
70	-12M	_____	-12M
71	SB0	_____	SB0
72	MB0	_____	MB0
73	MEV	_____	MEV
74	POPIO	_____	POPIO
75	SKF	_____	SKF
76	INCI	_____	INCI
77	IAK	_____	IAK
78	STF	_____	STF
79	IENS	_____	IENS
80	CLF	_____	CLF
81	PRL4/PRHS	_____	PRL4/PRHS
82	SFC	_____	SFC
83	IRQ5	_____	IRQ5
84	P5NF	_____	P5NF
85	GND	_____	GND
86	GND	_____	GND

_____ indicates no connection

Table 6. Labels of Selectable Settings

Switch	Name	Function
E1	MEASURE ENABLE	If the MEASURE ENABLE signal from the logic analyzer is to be used, jumper E1 should be in place for active low or not used for an active high signal.
S1	NO DMA DMA ONLY	Pre-trigger selection of DIRECT MEMORY ACCESS ONLY or NO DIRECT MEMORY ACCESS.
S2	I/O MEM	Pre-trigger selection of I/O or MEMORY.
S3	NO DMA DMA ONLY	Post-trigger selection of DIRECT MEMORY ACCESS ONLY or NO DIRECT MEMORY ACCESS.
S4	I/O MEM	Post-trigger selection of I/O or MEMORY.
S5	A15 R/$\overline{W}$	Selection of Address 15 or Read/$\overline{\text{Write}}$.

10278B COMPONENT LOCATOR (1)

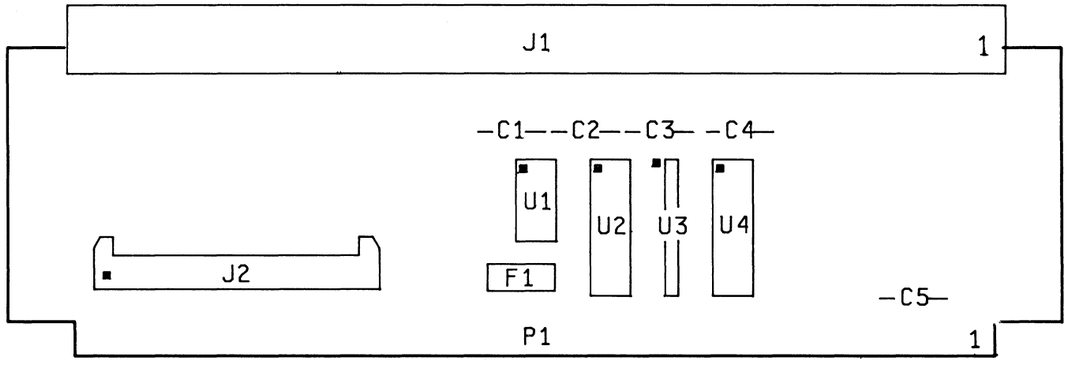


Figure 3. A1 Component Locator

7/27/81

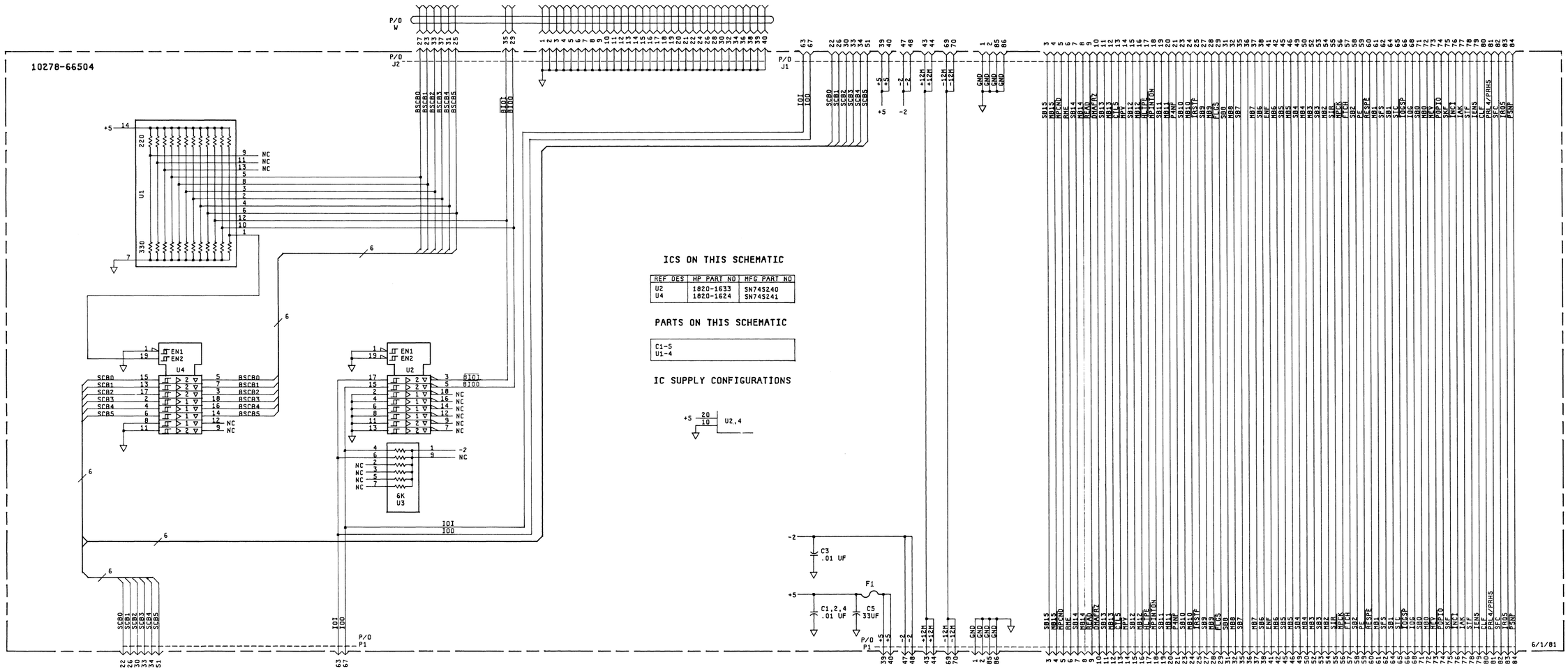


Figure 4.
A1 Schematic
Page 11

Table 7. A2 Control Signal Connections

Pin	J1	J2	P1	CONN A	CONN B
1	A10	___	____	BDMAOP	____
2	___	____	____	____	____
3	A11	____	SB15	I/O CLK	MEAS ENBL
4	A0	____	MB15	____	____
5	A12	____	$\overline{\text{WRITE}}$	MEM CLK	CLK
6	A1	____	____	____	____
7	A13	____	SB14	PA15	D15
8	A2	____	MB14	____	____
9	A14	____	$\overline{\text{READ}}$	PA14	D14
10	A3	____	$\overline{\text{DMAFRZ}}$	____	____
11	___	____	SB13	PA13	D13
12	A4	____	MB13	$\overline{\text{WRT}}$	AD15
13	A15	____	____	PA12	D12
14	A5	____	____	IRSTF	AD14
15	A16	____	SB12	PA11	D11
16	A6	____	MB12	MEM/I/O	AD13
17	A17	____	____	PA10	D10
18	A7	____	____	____	AD12
19	A18	____	SB11	PA9	D9
20	A8	____	MB11	____	AD11
21	A19	____	____	PA8	D8
22	A9	____	____	____	AD10
23	___	BSCB1	SB10	PA7	D7
24	___	____	MB10	____	AD9
25	___	BSCB5	____	PA6	D6
26	___	____	____	____	AD8
27	___	BSCB0	SB9	PA5	D5
28	___	____	MB9	____	AD7
29	___	____	____	PA4	D4
30	___	____	____	____	AD6
31	___	BSCB4	SB8	PA3	D3
32	___	____	MB8	____	AD5
33	___	BSCB2	$\overline{\text{IRSTF}}$	PA2	D2
34	___	____	____	____	AD4
35	___	BIOI	SB7	PA1	D1
36	___	____	____	PA19	AD3
37	___	BSCB3	MB7	PAO	D0
38	___	____	SB6	PA18	AD2
39	___	____	____	PA17	AD1
40	___	____	____	PA16	AD0
41	___	____	____	____	____
42	___	____	MB6	____	____
43	___	____	____	____	____
44	___	____	____	____	____
45	___	____	SB5	____	____
46	___	____	MB5	____	____
47	___	____	____	____	____
48	___	____	____	____	____
49	___	____	SB4	____	____
50	___	____	MB4	____	____
51	___	____	____	____	____
52	___	____	MB3	____	____
53	___	____	SB3	____	____
54	___	____	MB2	____	____
55	___	____	____	____	____
56	___	____	$\overline{\text{DMACYC}}$	____	____
57	___	____	____	____	____

Table 7. A2 Control Signal Connections (Cont'd)

Pin	J1	J2	P1	CONN A	CONN B
58	___	____	SB2	____	____
59	___	____	____	____	____
60	___	____	TA	____	____
61	___	____	MB1	____	____
62	___	____	____	____	____
63	___	____	$\overline{\text{P4NF}}$	____	____
64	___	____	SB1	____	____
65	___	____	____	____	____
66	___	____	____	____	____
67	___	____	____	____	____
68	___	____	____	____	____
69	___	____	____	____	____
70	___	____	____	____	____
71	___	____	SB0	____	____
72	___	____	MB0	____	____
73	___	____	____	____	____
74	___	____	POPIO	____	____
75	___	____	____	____	____
76	___	____	____	____	____
77	___	____	____	____	____
78	___	____	____	____	____
79	___	____	____	____	____
80	___	____	$\overline{\text{TEN}}$	____	____

____ indicates no connection

10278B COMPONENT LOCATOR (2)

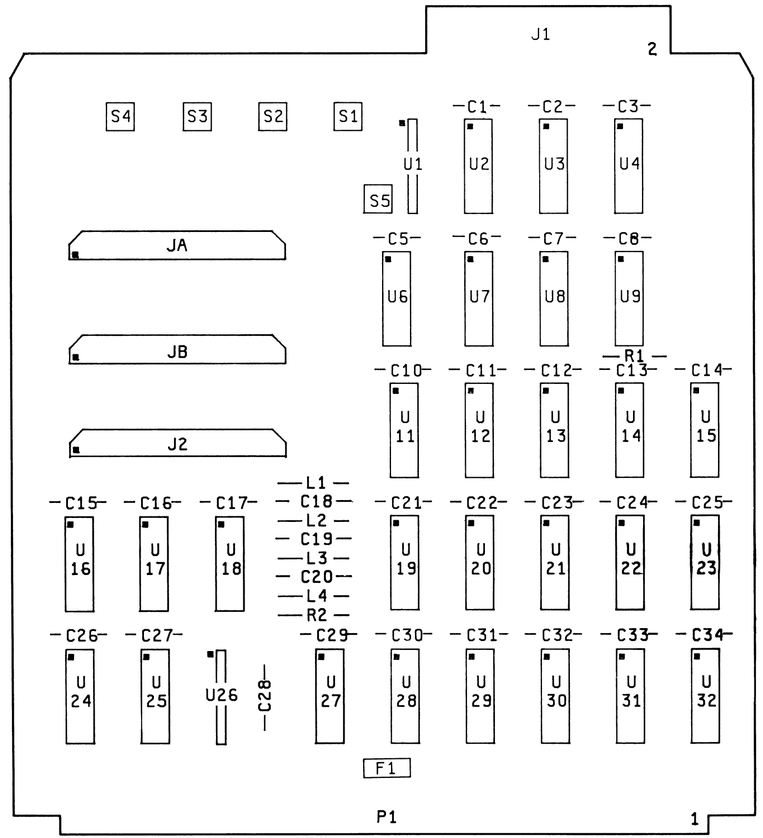
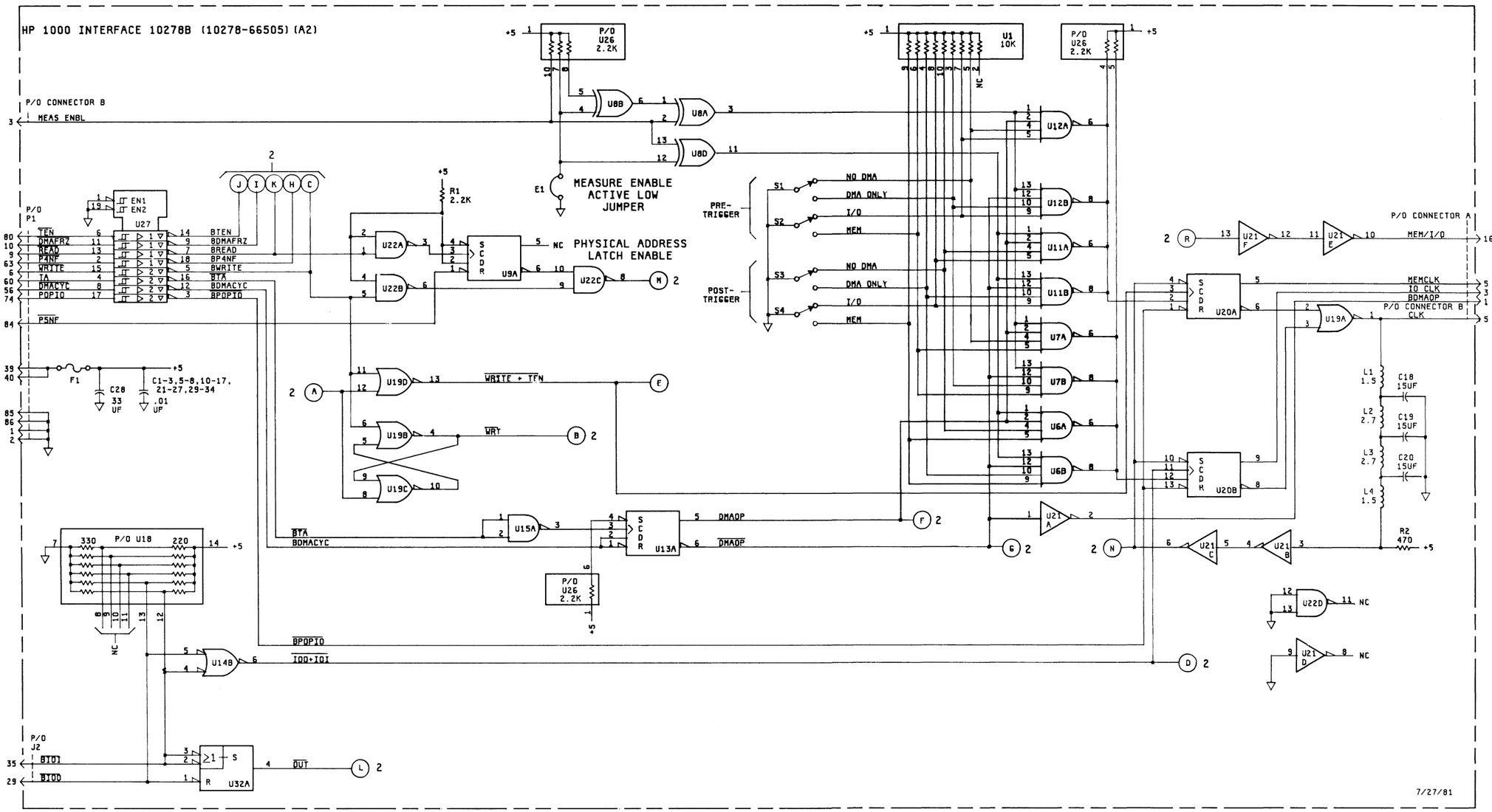


Figure 5. A2 Component Locator

7/27/81



1

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REF. DES.	HP PART NO.	MFR. PART NO.
U1	1810-0280	S10A103
U6,7,11, 12	1820-0689	74S22
U8	1820-1211	74S86
U9,13,20	1820-0693	74S74
U15,22	1820-0681	74S00
U18	1810-0182	1810-0182
U19	1820-1322	74S02
U21	1820-0683	74S04
U26	1810-0277	S10A222
U27	1820-1633	74S240
U32	1820-1440	74LS279

PARTS ON THIS SCHEMATIC

E1
U1,6-9,11-13,15,18-22,26,27,32
R1,2
L1-4
S1-4

IC POWER SUPPLY CONFIGURATIONS

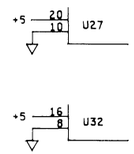
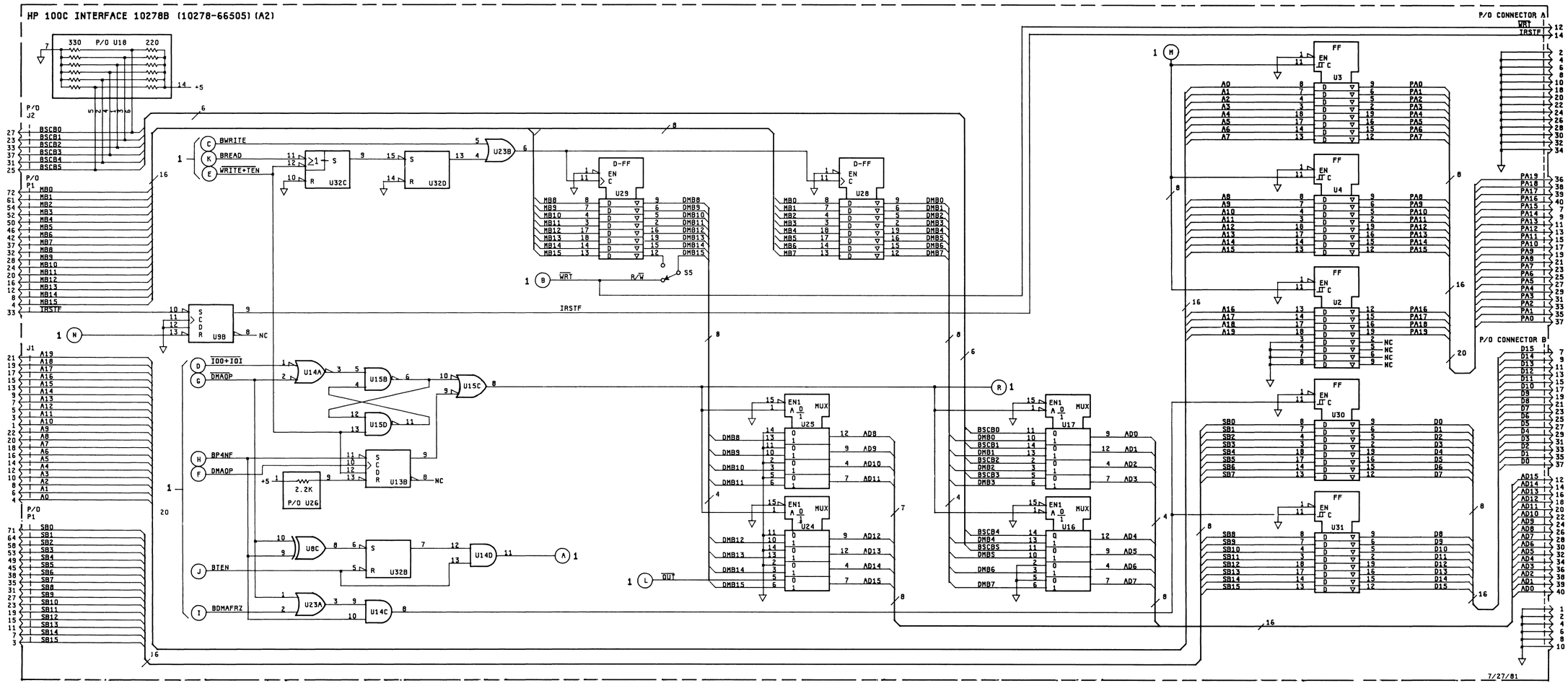


Figure 6.
A2 Schematic (1)
Page 13/(14 blank)



ICS ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U2-4, 30,31	1820-1676	74S373
U8	1820-1211	74S86
U9,13	1820-0693	74S74
U14	1820-1367	74S08
U16,17, 24,25	1820-1077	74S157
U18	1820-0182	1810-0182
U23	1820-1449	74S32
U26,29	1820-1677	74S374
U32	1820-1440	74LS279

PARTS ON THIS SCHEMATIC

U2-4,8,9,10,14,16-18,23-25,28-32

IC POWER SUPPLY CONFIGURATION

+5 — 14 — 7 — U8,9,13,14, 23

+5 — 16 — 8 — U2-4,16,17,24, 25,28,29,30-32

2

Figure 7.
A2 Schematic (2)
Page 15

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