Honeywell

SERIES 60 LEVEL 6

TYPE DCM9101 DUAL ASYNCHRONOUS COMMUNICATIONS LINE ADAPTER MANUAL

Doc. No. 71010232-200 Order No. FL50, Rev. 1

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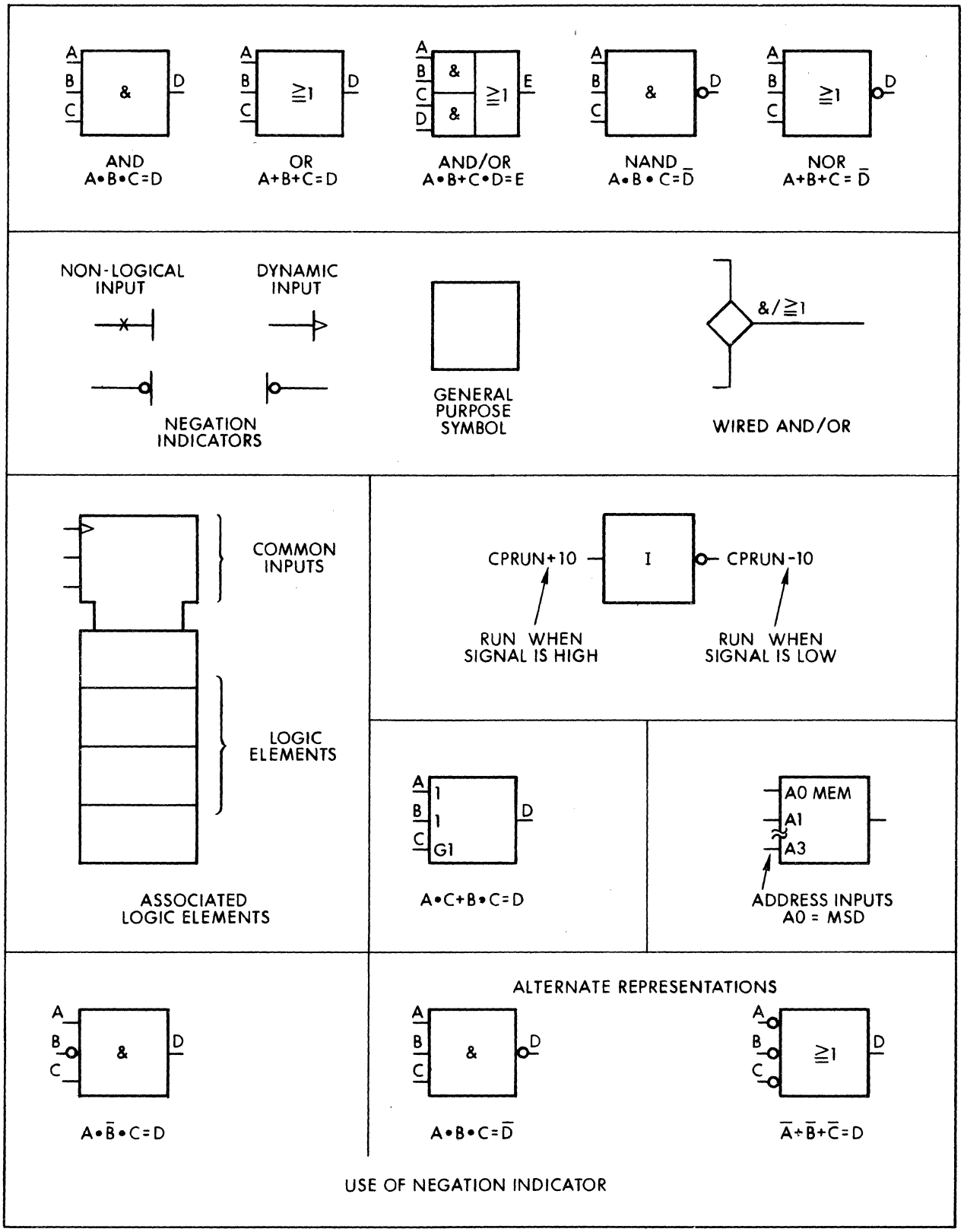

1 INTRODUCTION

1.1 GENERAL DESCRIPTION

The Type DCM9101 Dual Asynchronous Communications Line Adapter (ACLA), one of a series of Communications-Pacs, is a solid-state module used with the multiline communications processor (MLCP) associated with a Honeywell Series 60 Level 6 computer. As shown in Figure 1-1, up to four compatible line adapters can be used with an MLCP, and from one to four of these adapters can be an ACLA. Each dual ACLA can support two full duplex lines, and each direction (receive and transmit) of a line is a separate channel into the MLCP. Note that in this manual ACLA refers to a dual asynchronous communications line adapter.

An ACLA contains the logic for data handling, control, and interface between the MLCP and data communication equipment (DCE). Essentially, the ACLA contains a group of line registers which the MLCP continually sets to effect required operational functions. Note that all formatted control procedures used in communicating with the DCE are performed in the MLCP.

The ACLA can be used with the following typical data communication equipment (DCE):

- Dataphone Data Set 103 (or equivalent) or modem bypass
- Dataphone Data Set 113 (or equivalent) or modem bypass
- Dataphone Data Set 202 (or equivalent) or modem bypass

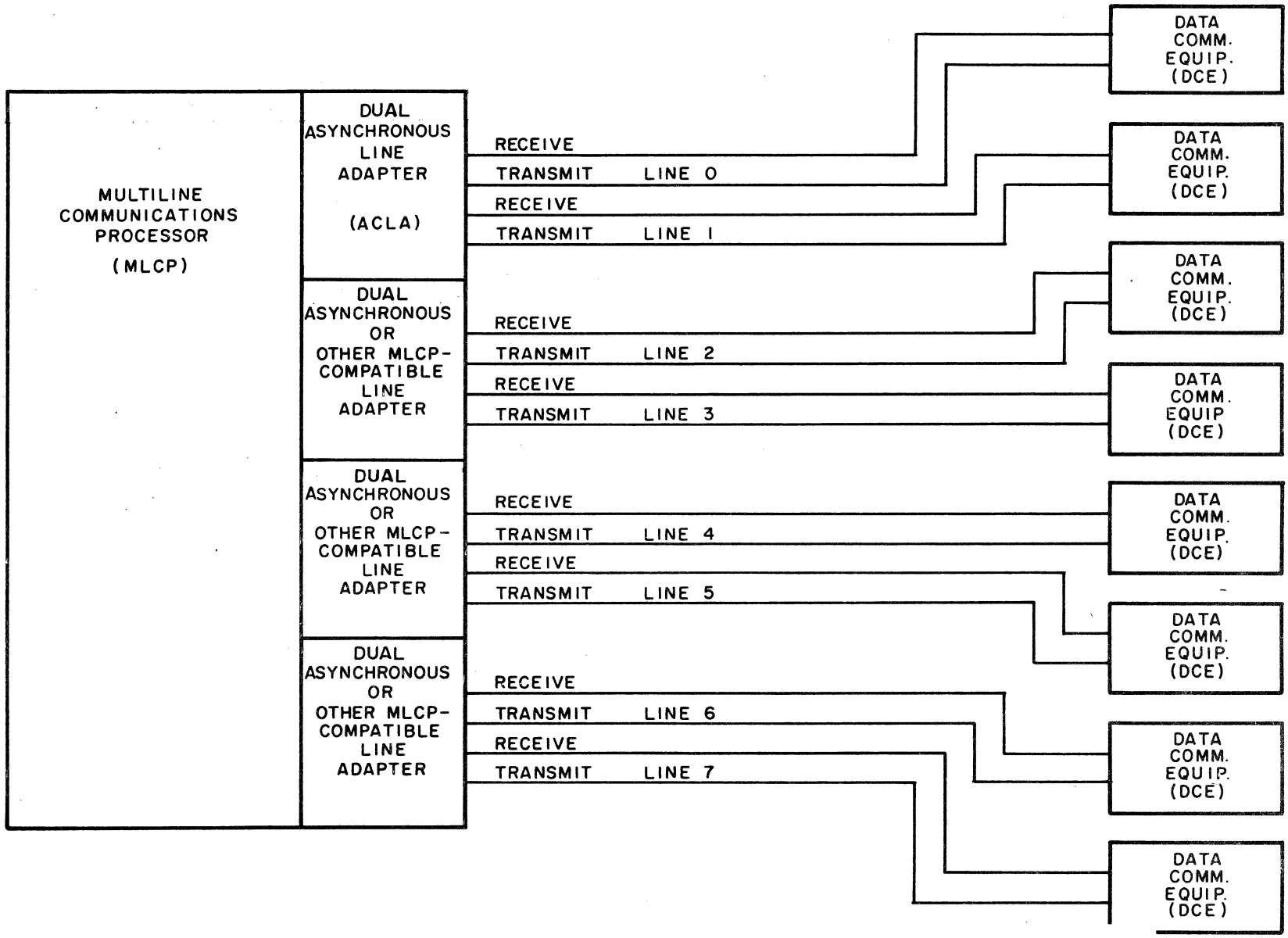

Figure 1-1 Configuration Diagram, Dual Asynchronous Communications Line Adapter (ACLA)

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1.2 INTERFACE

The data interface between the ACLA and the DCE is full duplex for each line. All input and output data information is in a serial stream consisting of communication-type characters. Five-, 6-, 7-, or 8-bit characters are used, depending upon software instructions. One or 2 stop bits are appended to each 6-, 7-, or 8-bit character, depending upon the configuration of the ACLA. One or 1.5 stop bits are appended to each 5-bit character, depending upon the configuration.

In addition to the data interface between the ACLA and the DCE, there are also eight control line interconnections between the ACLA and the DCE for each line. (See Table 2-2 for explanations of the use of these lines.)

All transmissions between the ACLA and the DCE is at a level specified by Specification RS232C of the Electronic Industries Association (EIA). To conform with this specification, 0V and 5V signals generated in the ACLA are changed to +12V and -12V respectively if they are transmitted to the DCE. Conversely, +3 to +25V and -3 to -25V levels generated in the DCE are changed to 0V and 5V respectively when they are received in the ACLA.

The interface between the ACLA and MLCP is half duplex. All input data, output data, and control signals are carried on lines which use connectors on the bottom of the line adapter to connect to the MLCP. All data is transferred in parallel (byte form) between the ACLA and MLCP.

The transmission rate between the ACLA and the DCE can be set at various speeds between 50 and 19,200 baud, depending upon the software configuration. (See Figure 2-7 and Figure 2-8.)

1.3 PHYSICAL CHARACTERISTICS

The dual asynchronous communications line adapter (BD2ASC) can be attached to any Communications-Pac position on the MLCP module (BF4MLC). The physical dimensions of the MLCP and the Communications-Pac are indicated in Figure 1-2.

The BD2ASC board has two 25-pin connectors (Z01 and Z02) which are used for the physical and electrical connection of the Communications-Pac to the MLCP. A 28-pin connector, Y01, is used to connect the DCE cable to the BD2ASC board. For information pertaining to installation and cabling, refer to the Model 34/36 Systems Manual.

1.4 OPTIONS

The ACLA can be used in a direct connect application, which allows the MLCP to interface with another computer without the use of data communications equipment (DCE). The direct connect application is enabled when the ACLA DCE cable is connected to a direct connect cable and attached to another system. Information pertaining to direct connect cables is in the Model 34/36 Systems Manual.

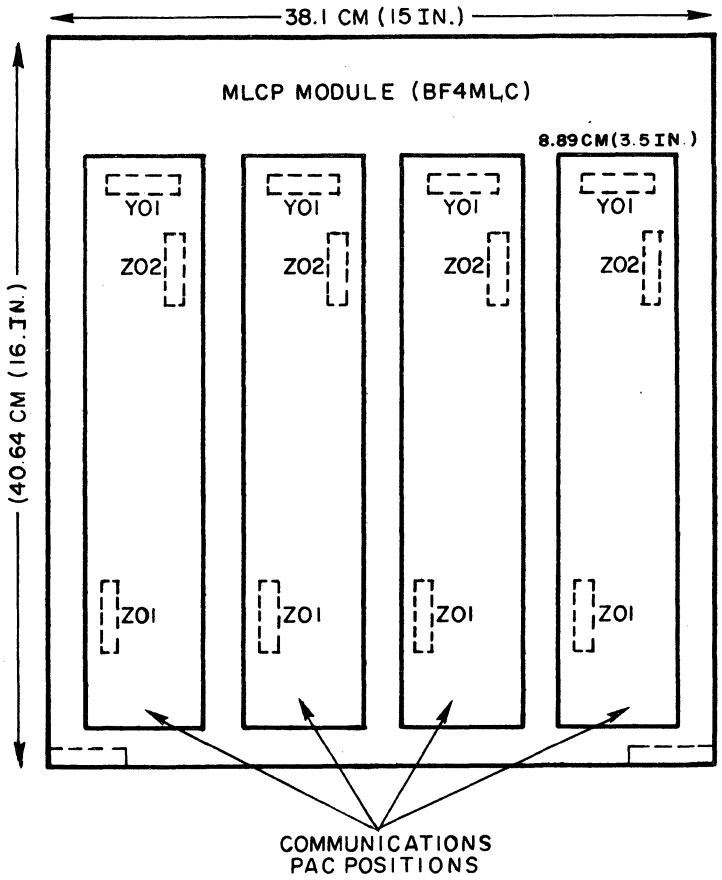

Figure 1-2 ACLA Layout and Dimensions

1.5 REFERENCE DOCUMENTS

The following documents supplement the information contained in this manual.

Title	Document No.	Order No.
Model 34/36 Systems Manual	71010200-200	FL35
Type MLC9103 Multiline Communications Processor Manual	71010230-200	FL48
Type DCM9101 Communications Line Adapter Reference Manual	71010382-200	FL53
Level 6 Minicomputer Handbook	--	AS22
MLCP Programmer's Reference Manual	--	AT97
Level 6 System Checkout and Operator's Guide	--	AW94

II THEORY OF OPERATION

2.1 BLOCK DIAGRAM DESCRIPTION

The asynchronous communications line adapter (ACLA) provides the multiline communications processor (MLCP) with two independent interfaces with standard asynchronous communications lines. Figure 2-1 is a block diagram of the logic used in interface A (between the MLCP and line 0). Interface B (between the MLCP and line 1), which has similar logic, is not shown. Note, however, that the ACLA control blocks, the input status multiplexer, and the test multiplexer shown in Figure 2-1 are common to both interface A and Interface B.

The basic function of the ACLA is to control the data flow between the MLCP and the lines. Data bytes received in parallel from the MLCP are transformed into standard communication-type characters and transferred to the lines in a serial stream. Communication-type characters received from the lines in a serial stream are converted to data bytes and sent to the MLCP in parallel-byte form. A secondary function of the ACLA is to interchange control information between the MLCP and the data communications equipment (DCE).

All interconnections between the ACLA and the MLCP are via hardware connectors on the bottom of the ACLA. There are four control lines and three address lines between the MLCP and the ACLA. The ACLA control logic uses these lines to generate signals for control of the ACLA hardware. (See subsection 2.2.3 for details on the decoding of the control and address lines and the use of the generated control signals.) The data input lines (8) are used to transfer

either data bytes from the receiver or an input byte from the input status multiplexer into the MLCP. The MLCP data output lines (8) are used to transfer data bytes to the ACLA transmitter; configure the transmitter/receiver (XMTR/RCVR); load the clock speed register in the baud rate generation logic (type 5307 baud rate generator); load the input control gates for the baud rate generation logic (type 5016 baud rate generator); and to load the data set control register. The MLCP continually samples the ready flip-flops in the ACLA to see if the receiver has an assembled data byte to transfer to the MLCP or if the trasmitter requires another byte for sending to the line.

Prior to receiving data from the line, the channel program configures the data channel to handle 5-, 6-, 7-, or 8-bit data characters, and to look for 1, 1.5, or 2 stop bits to be appended to the end of the character. Parity checking of received characters is accomplished in the MLCP; therefore, no parity error checking is accomplished in the receiver. During an input data operation from the line to the MLCP, the receiver checks each character for stop bits and generates an error signal when they are not detected. If the receiver assembles two characters before one is transferred into the MLCP, an overrun error signal is generated. When the receiver sends a data character to the MLCP, it strips the stop bits from the character. (See subsection 2.2.7 for more details on a receive operation.)

Prior to transmitting data to the line, the channel program configures the transmitter/receiver to handle 5-, 6-, 7-, or 8-bit characters and to append 1, 1.5, or 2 stop bits to the outputted characters. No parity or error information is generated by the transmitter. (See subsection 2.2.6 for more details on a transmit operation.)

The input status multiplexer inputs ACLA error and line status information into the MLCP from either interface A or interface B as selected. (See subsection 2.2.8 for specific information carried by the input signals.)

The test multiplexer provides a wraparound mode for use by diagnostic software. The wraparound mode allows the serial data stream out of the transmitter to be sent directly back to the MLCP via the receiver in data-byte form. The diagnostic software then checks the operation of the ACLA by comparing transmitted and received characters. (See subsection 2.2.9 and the Appendix for further details.)

The data set control logic consists of an 8-bit register which stores control information from the MLCP. This information is then used by the ACLA for controlling the interface to its associated data communications equipment (DCE). (See subsection 2.2.4 for details on the use of the stored information.)

The baud rate generation logic is used to generate a clock signal which is 16 times the transmitting or receiving baud rate. This clock signal is required for operation by both the transmitter and

the receiver. The baud rate can be varied by the MLCP in steps between 50 and 9600 baud for the type 5307 baud rate generator, and between 50 and 19,200 baud for the type 5016 baud rate generator. (See subsection 2.2.5 for details.)

The EIA interface logic enables the ACLA to use transmitters and receivers designed to Specification RS232C of the Electronic Industries Association (EIA). This interface changes the level of signals out of the ACLA from the TTL 0V and +5V to +12V and -12V respectively for use by the data communications equipment (DCE). Conversely, the EIA interface logic changes signals received at +3 to +25V and -3 to -25V levels from the DCE to 0V and +5V respectively for use by the ACLA.

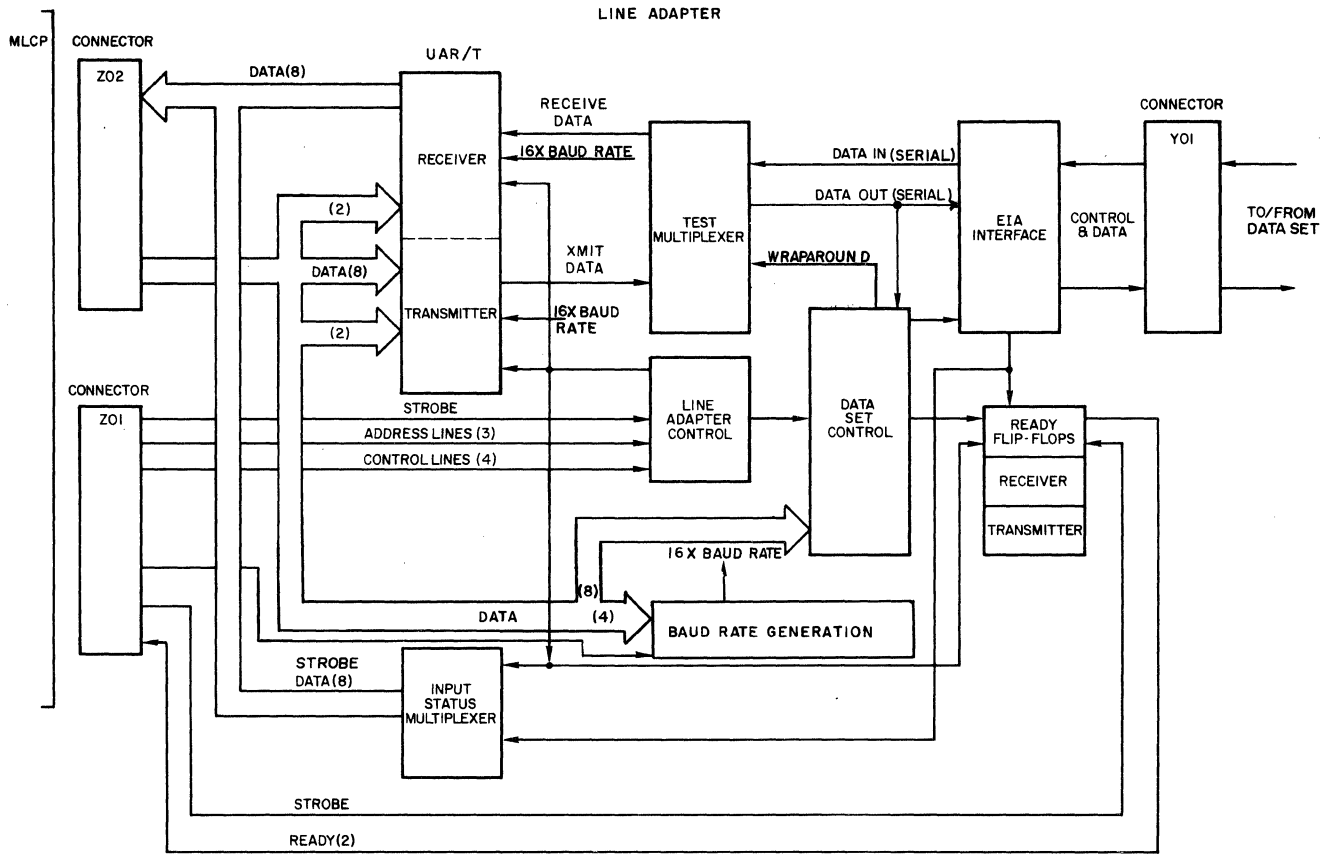

Figure 2-1 Dual ACLA, Block Diagram

2.2 FUNDAMENTAL HARDWARE DESCRIPTION

2.2.1 Interconnections

Figure 2-2 shows the interconnections between the multiline communications processor (MLCP) and the ACLA. Table 2-1 describes the function of the signals carried by these interconnections.

Figure 2-3 shows the interconnections between the ACLA and the lines. Table 2-2 describes the function of the signals carried by these interconnections.

2.2.2 Subchannel Identification Code Lines

The subchannel identification code lines (see Figure 2-2) are used by the MLCP to identify the type of ACLA attached. The MLCP then uses this information to form a software identification word. The specific word assigned to the asynchronous line adapter is hexadecimal 2108 or 2118, depending on the type of baud rate generator used.

The ACLA utilizes interface lines LACOD1 through LACOD4 (located at the MLCP side of the interface connector) to input its portion of the subchannel identification code to the MLCP. Table 2-3 identifies the MLCP data bus bit positions to which the ACLA ID code is transferred, the binary and hexadecimal configuration of the subchannel ID code, and the voltage levels to which LACODx lines are hardwired in the ACLA to produce its portion of the ID (i.e., xx08 or xx18). The 21xx is generated in the MLCP, and the entire ID word (2108 or 2118) is transferred to the Megabus when requested by software.

As shown in Table 2-3, the ID code for an ACLA containing a type 5307 baud rate generator, board assembly number 60127918, is 2108, and for a type 5016 baud rate generator, board assembly number 60130510, is 2118.

2.2.3 Line Adapter Control

As shown in Figure 2-4, the ACLA control logic consists of five 2-line to 4-line decoders and numerous gates and inverters. The function of this logic is to develop control signals for performing operations in the hardware of the ACLA. All of these control signals are developed from the address lines (3), control lines (4), and the strobe signal (1) sent out by the MLCP.

Table 2-4 lists the general decoding of the address and control lines from the MLCP. Table 2-5 lists the specific use of the address and control information received from the MLCP in developing control signals.

The programming interface to the ACLA is achieved through line registers (Figure 2-5) located in the ACLA. Each communications line is serviced by a different set of line registers. Each channel (transmit or receive) of a line has a dedicated set of registers and also shares four registers with the other channel of the same line.

As shown in Figure 2-5, line registers 0, 3, and 7 are not used. Line registers 1 and 6 are located in the Universal Asynchronous

Transmitter/Receiver (Figure 2-10 and 2-11) and are accessed through the specified input gates. Line register 2 contains data set control information (Figure 2-6 and 2-7); and line register 5 is the status register (Figure 2-12).

For a detailed description of the line register contents, refer to the MLCP Programmer's Reference Manual.

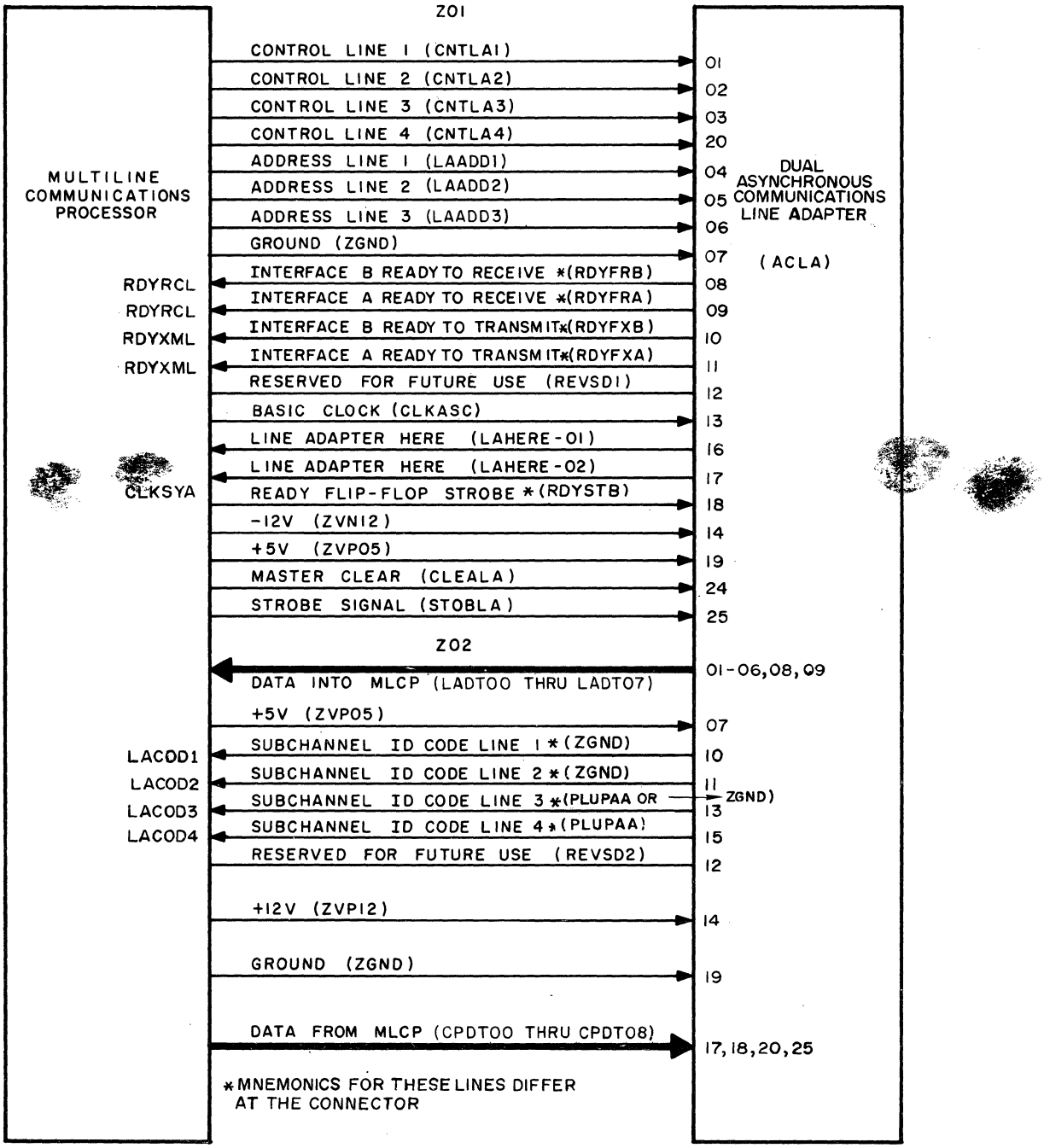

Figure 2-2 Interconnections Between MLCP and Dual ACLA

Table 2-1 Interconnections-Dual ACLA To/From MLCP

MNEMONIC	NAME OF LINE	FUNCTION
CLEALA	Master Clear	Clears hardware in the ACLA when ordered by the MLCP.
CLKASC	Basic Clock	Basic clock signal from the MLCP (921.6 kHz) - Input to baud rate generator (chip type 5307 only). Not used in systems employing type 5016 baud rate generator.
CNTLA1 thru CNTLA4	Control	Selects functions to be performed by ACLA hardware.
CPDT00 thru CPDT07	Data Output Byte	Data output byte from the MLCP. Used to transfer both data and control information.
LAADD1 thru LAADD3	Address	Selects line and channel to be serviced
LACOD1 thru LACOD4	Subchannel ID Code	Lines by which the MLCP identifies the specific type of ACLA attached to it.
LADT00 thru LADT07	Input Byte	Data input byte into the MLCP. Depending upon the operating condition of the ACLA, this byte can be either data or status from either interface A or interface B.
LAHERE-01 LAHERE-02	Line Adapter Here	Notifies the MLCP that an ACLA is installed.
RDYFRA	Interface A Ready to Receive	Indicates that interface A is ready to transfer a data character into the MLCP.
RDYFRB	Interface B Ready to Receive	Indicates that interface B is ready to transfer a data character into the MLCP.
RDYFXA	Interface A Ready to Transmit	Indicates that interface A is ready to receive a new data character from the MLCP for transmission to the line.
RDYFXB	Interface B Ready to Transmit	Indicates that interface B is ready to receive a new data character from the MLCP for transmission to the line.
RDYSTB	Ready Flip-Flop Strobe	Used to synchronize the ready flip-flops in interface A and B of the ACLA with the MLCP, and to clock the baud rate generator.
STOBLA	Strobe Signal	Strobe from the MLCP to the ACLA for generating various control signals. Indicates that data from MLCP is valid.
REVSD1 REVSD2	Reserved	Reserved for future use.
ZGND	Ground	Ground
ZVP05	+5V	+5V
ZVN12	-12V	-12V
ZVP12	+12V	+12V

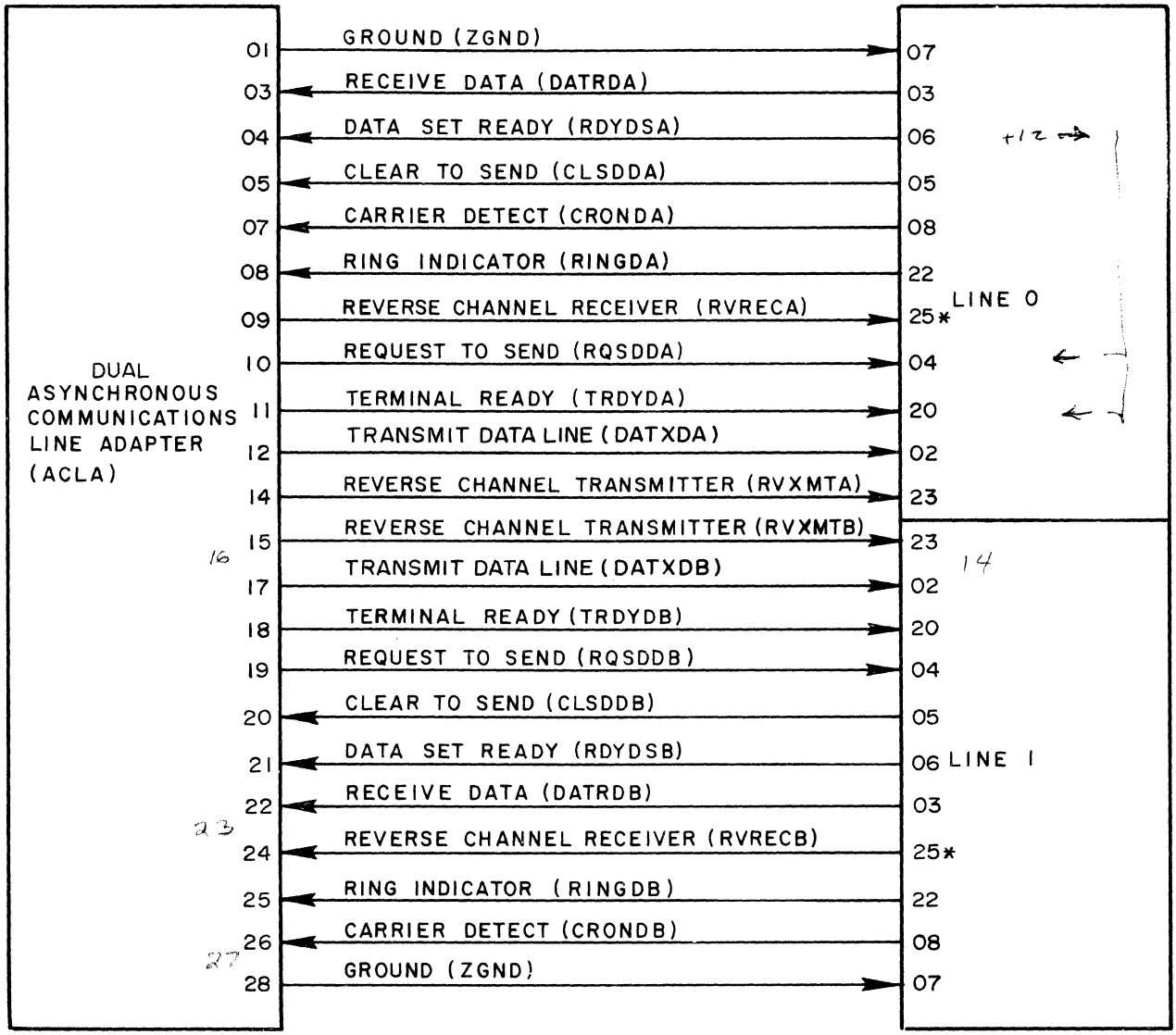

Figure 2-3 Interconnections Between Dual ACLA and Lines and Standard EIA Pin Connections

Table 2-2 Interconnections-Line Adapter To/From Lines

MNEMONIC	NAME	FUNCTION
NOTE The signals listed below are for line 0. Line 1 has an identical set of signals, but the last letter of the mnemonic is B instead of A.		
CLSDDA	Clear to Send	A response by the data communication equipment (DCE) to a Request to Send signal from the adapter.
CRONDA	Carrier Detect	Indicates to the adapter that the basic carrier frequency of the communication line is present.
DATRDA	Receive Data	The serial data line from the DCE to the adapter.
DATXDA	Transmit Data	The serial data line from the adapter to the DCE.
RDYDSA	Data Set Ready	A signal from the DCE to the adapter indicating that it is ready to operate.
RVRECA	Reverse Channel Receiver (Supervisory Received Data)	This line allows supervisory signals to be sent from the DCE to the adapter.
RVXMTA	Reverse Channel Transmitter (Supervisory Transmitted Data)	This line allows supervisory signals to be sent from the adapter to the DCE.
RINGDA	Ring Indicator	Indicates that the line is in a ringing condition and is trying to get the attention of the adapter.
RQSDDA	Request to Send	A request to transmit from the adapter to the data communications equipment (DCE).
TRDYDA	Terminal Ready	A signal from the adapter to the DCE indicating that the adapter is ready for an operation.
ZGND	Ground	Ground.

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Table 2-3 ACLA ID Code Generation

ID WORD	MLCP DATA BUS															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
LACOD1-4 Lines at MLCP/ACLA Interface Connector										1	2	3	4			
Type 5307 Baud Rate Generator																
Binary	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0
Hex	2				1				0				8			
Hardwired Connections in ACLA										GND	GND	GND	+5V			
Type 5016 Baud Rate Generator																
Binary	0	0	1	0	0	0	0	1	0	0	0	1	1	0	0	0
Hex	2				1				1				8			
Hardwired Connections in ACLA										GND	GND	+5V	+5V			

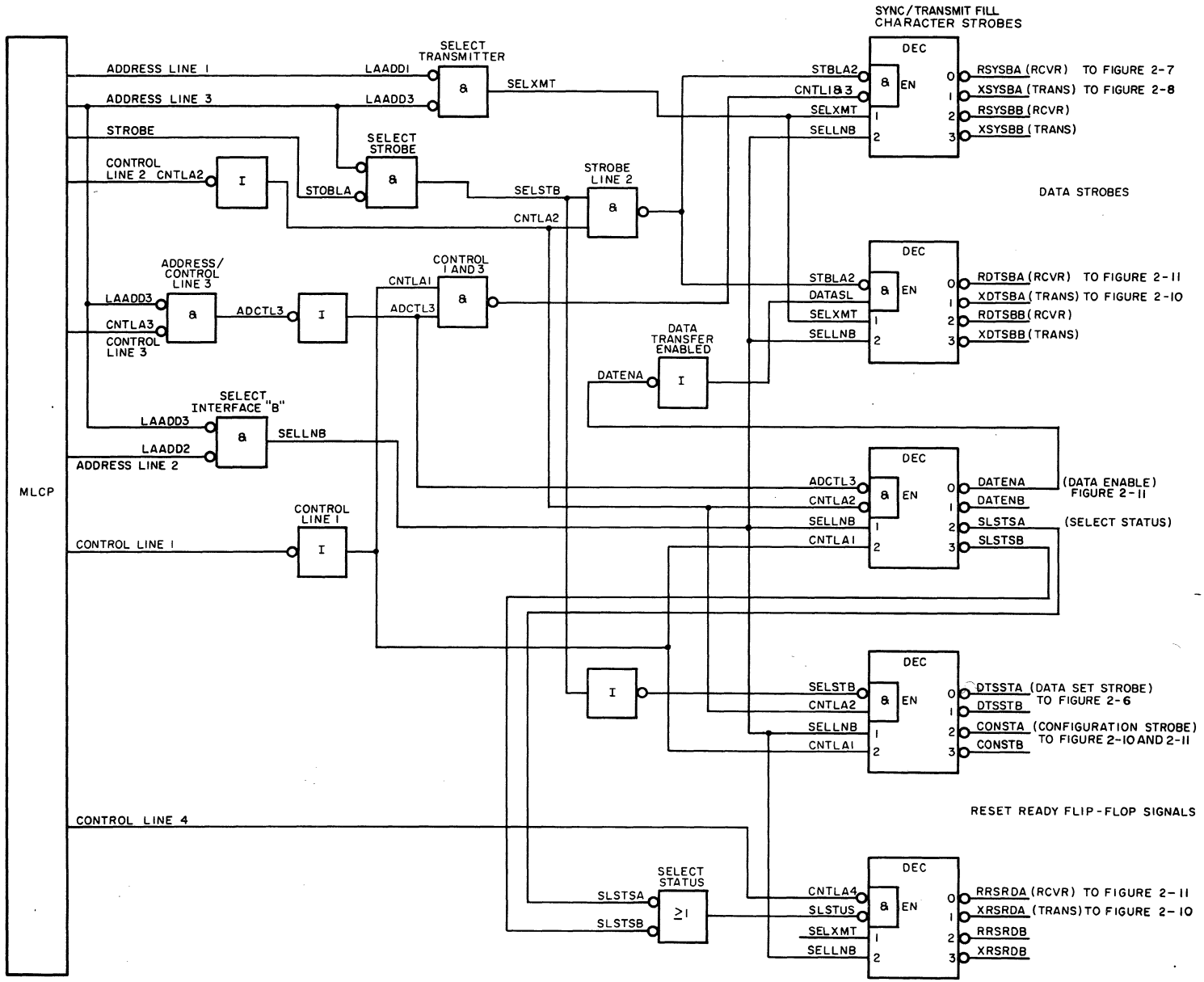

Figure 2-4 Dual ACLA Control, Address and Control Line Decoding

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Table 2-4 Address and Control Lines, General Decoding

ADDRESS LINE			GENERAL FUNCTION & COMMENT
1	2	3	
1	0	1	Select transmitter
0	0	1	Select receiver
X	1	1	Select interface B
X	0	1	Select interface A
X	X	1	Indicates to the ACLA that it has been selected by the MLCP. The MLCP can control up to four ACLAs but enables only the ACLA with address line 3 set.
X	X	0	Indicates to the ACLA that it has not been selected by the MLCP. Address line decoding is not performed by the ACLA when address line 3 is reset.

NOTE

X = Decoding logic not affected by status of this bit when determining indicated control function.

LINE REGISTER SELECT	CONTROL LINE				GENERAL FUNCTION & COMMENT
	1	2	3	4	
4	1	0	0	X	Load clock rate
2	0	1	0	X	Load data set register
6	1	1	0	X	Load receiver/transmitter with configuration information
1	0	0	1	X	Output/input data to/from transmitter or receiver
5	1	0	1	X	Input status
5	1	0	1	1	Reset data request ready flip-flop

NOTE

X = Decoding logic not affected by status of this bit when determining indicated control function.

Table 2-5 Decoding-Control and Address Lines

LINE REGISTER SELECT	CONTROL LINES				ADDRESS LINES			OUTPUT OF DECODER	ADAPTER INTERFACE	FUNCTION OF DECODED CONTROL SIGNAL
	1	2	3	4	1	2	3			
6	1	1	0	X	X	0	1	CONSTA	A	Load receiver/transmitter with configuration information
6	1	1	0	X	X	1	1	CONSTB	B	Load receiver/transmitter with configuration information
1	0	0	1	X	1	0	1	XDTSBA	A	Load transmitter data buffer
1	0	0	1	X	1	1	1	XDTSBB	B	Load transmitter data buffer
1	0	0	1	X	0	0	1	DATENA	A	Enable input from receiver to MLCP
1	0	0	1	X	0	0	1	RDTSBA	A	Input receiver data to MLCP
1	0	0	1	X	0	1	1	DATENB	B	Enable input from receiver to MLCP
1	0	0	1	X	0	1	1	RDTSBB	B	Input receiver data to MLCP
4	1	0	0	X	0	0	1	RSYSBA	A	Load clock rate
4	1	0	0	X	0	1	1	RSYSBB	B	Load clock rate
2	0	1	0	X	X	0	1	DTSSTA	A	Load data set control register
2	0	1	0	X	X	1	1	DTSSTB	B	Load data set control register
5	1	0	1	X	X	0	1	SLSTSA	A	Enable and select status multiplexer for this interface
5	1	0	1	X	X	1	1	SLSTSB	B	Enable and select status multiplexer for this interface
5	1	0	1	1	0	0	1	RRSRDA	A	Reset receiver ready flip-flop
5	1	0	1	1	1	0	1	XRSRDA	A	Reset transmitter ready flip-flop
5	1	0	1	1	0	1	1	RRSRDB	B	Reset receiver ready flip-flop
5	1	0	1	1	1	1	1	XRSRDB	B	Reset transmitter ready flip-flop

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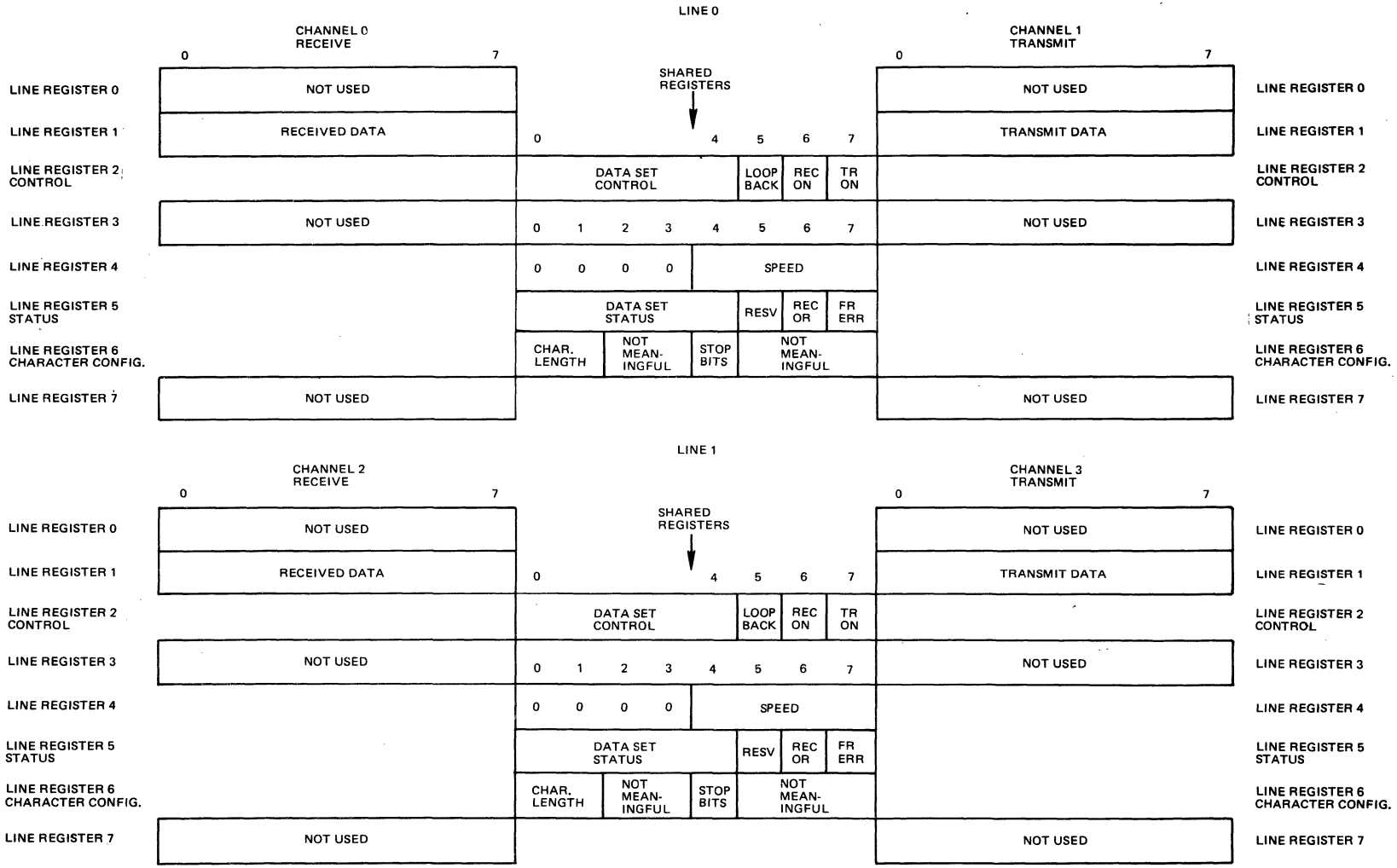

Figure 2-5 ACLA Line Registers

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2.2.4 Data Set Control

As shown in Figure 2-6, the data set control logic primarily consists of the data set control register, which is comprised of eight D-type flip-flops. The flip-flops are loaded by the data set strobe with information conveyed by the data information lines from the MLCP. The function of the output signal from each flip-flop is as follows.

1. TRDYDA - ACLA ready to the data communication equipment (DCE). This is commonly called Terminal Ready in communications systems.
2. RQSDDA - Request to transmit from the adapter to the DCE.
3. RVXMTA - Reverse channel transmitter. This line allows supervisory signals to be sent to the DCE.
4. SPACEA - Space data line constantly to the DCE.
5. MARKLA - Mark data line constantly to the DCE.
6. TESMDA - Set test mode in the ACLA. (See subsection 2.2.9 for details.) Note that interface B does not generate this signal but is placed in the test mode by the hardware of interface A.
7. RECONA - Enables the receiver in the ACLA. (See subsection 2.2.7 for details on use.)
8. XMTONA - Enables the transmitter in the ACLA. (See subsection 2.2.6 for details on use.)

2.2.5 Baud Rate Generation Logic (Figures 2-7 and 2-8)

The baud rate generator, chip type 5307, logic (shown in Figure 2-7) consists of a 4-bit clock speed register and the baud rate generator. The MLCP sets the baud rate for a transmit or receive operation by setting the clock speed register to a specific code (see the table on Figure 2-7). The baud rate generator divides the basic clock (921.6 kHz) frequency by the ordered divisor to obtain the desired baud rate. The output of the baud rate generator (16X baud rate) is sent to both the transmitter and the receiver which require this frequency for operation. (Chip type 5307 is used on board assembly 60127918.)

The baud rate generator chip type 5016 logic shown in Figure 2-8 consists of a 4-bit MLCP-coded input and the baud rate generator. The MLCP sets the baud rate for a transmit or receive operation by setting the input to the baud rate generator to a specific code (see the table on Figure 2-8). The baud rate generator divides the Ready Strobe (4.213 MHz) frequency by the ordered divisor to obtain the desired baud rate. The output of the baud rate generator (16 X baud rate) is sent to both the transmitter and the receiver which require this frequency for operation. (Chip type 5016 is used on board assembly 60130510.)

Note that the baud rate generator logic (line register 4) can be loaded only by the receive channel's channel control program, through the clock speed strobe (RSYSBA).

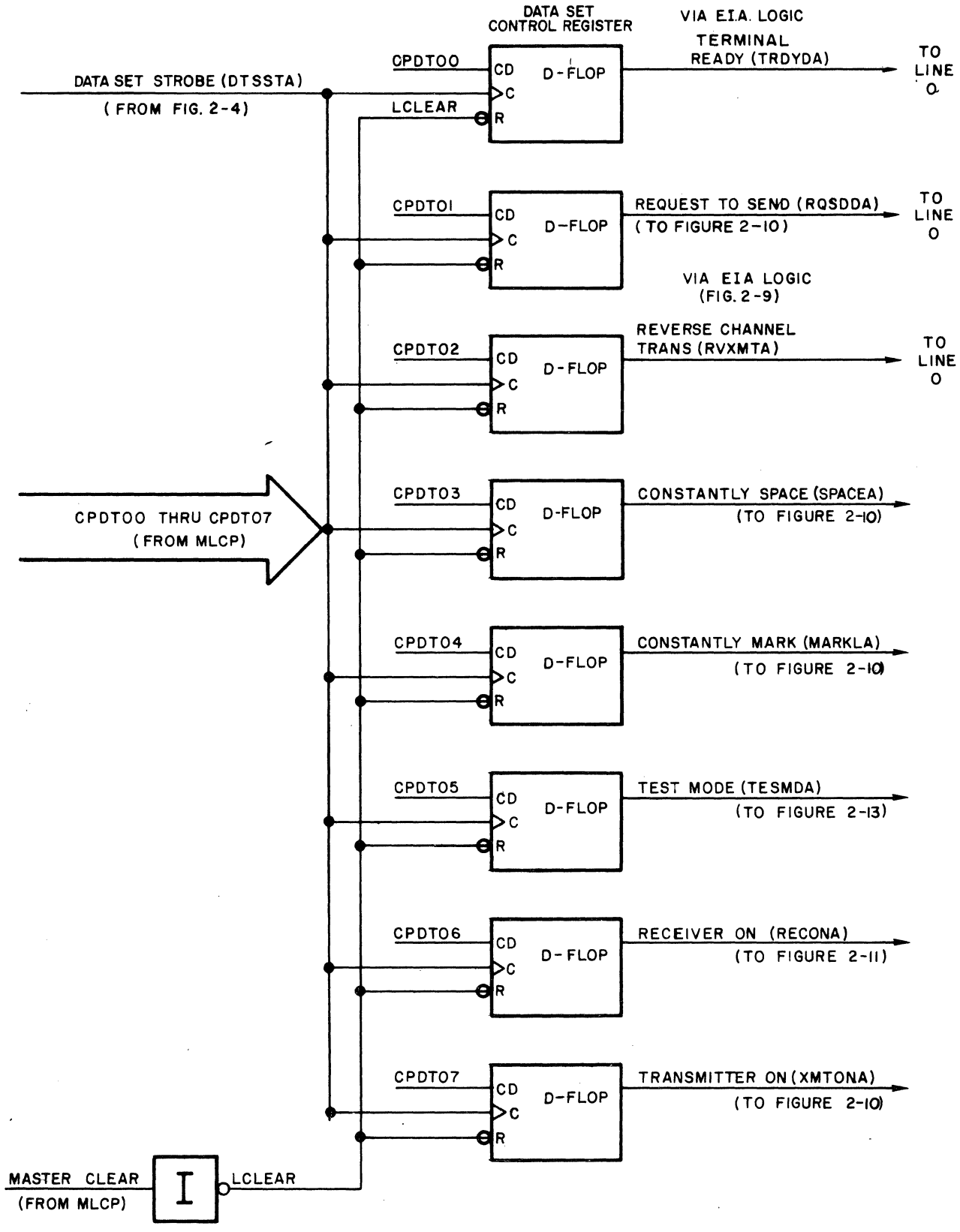
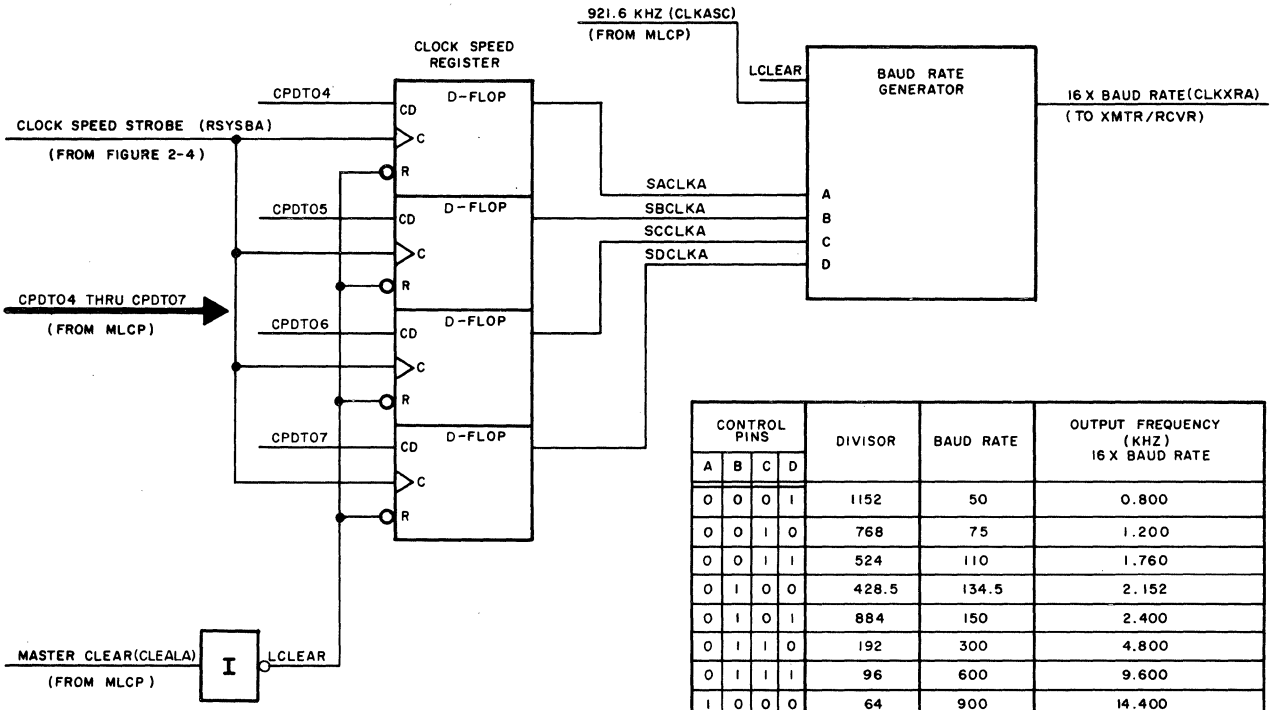
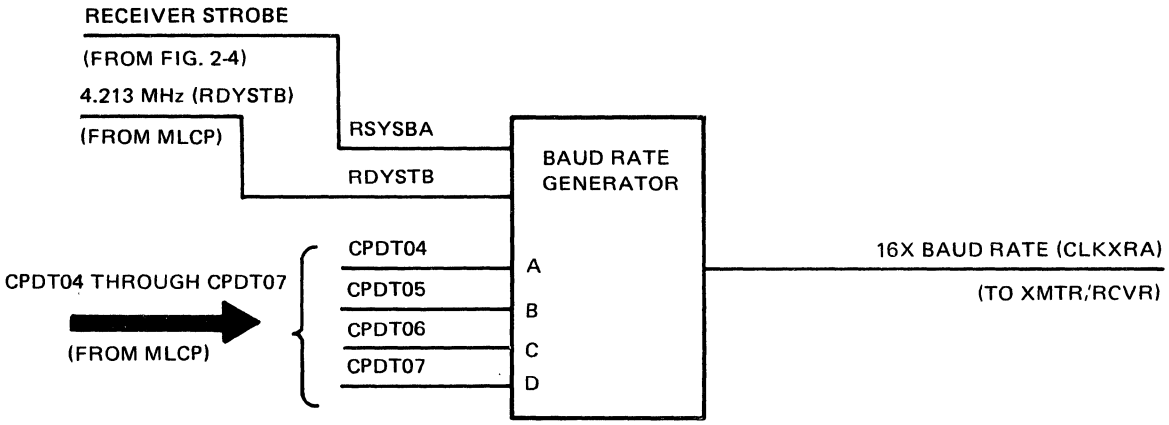


Figure 2-6 Data Set Control Logic



CONTROL PINS				DIVISOR	BAUD RATE	OUTPUT FREQUENCY (KHZ) 16 X BAUD RATE
A	B	C	D			
0	0	0	1	1152	50	0.800
0	0	1	0	768	75	1.200
0	0	1	1	524	110	1.760
0	1	0	0	428.5	134.5	2.152
0	1	0	1	884	150	2.400
0	1	1	0	192	300	4.800
0	1	1	1	96	600	9.600
1	0	0	0	64	900	14.400
1	0	0	1	48	1200	19.200
1	0	1	0	32	1800	28.800
1	0	1	1	24	2400	38.400
1	1	0	0	16	3600	57.600
1	1	0	1	12	4800	76.800
1	1	1	0	8	7200	115.20
1	1	1	1	6	9600	153.600

Figure 2-7 Baud Rate Generation Logic, Chip Type 5307



CONTROL PINS				DIVISOR	BAUD RATE	OUTPUT FREQUENCY (kHz) 16X BAUD RATE
A	B	C	D			
0	0	0	0	5266	50	0.800
0	0	0	1	3511	75	1.200
0	0	1	0	2394	110	1.760
0	0	1	1	1958	134.5	2.152
0	1	0	0	1755	150	2.400
0	1	0	1	1317	200	3.199
0	1	1	0	878	300	4.798
0	1	1	1	439	600	9.597
1	0	0	0	251	1050	16.784
1	0	0	1	219	1200	19.238
1	0	1	0	146	1800	28.856
1	0	1	1	132	2000	31.917
1	1	0	0	110	2400	38.300
1	1	0	1	55	4800	76.600
1	1	1	0	27	9600	156.040
1	1	1	1	14	19200	300.930

Figure 2-8 Baud Rate Generation Logic,Chip Type 5016

2.2.6 Data Output

The ACLA sends out data to the data communications equipment (DCE) in the form of 5-, 6-, 7-, or 8-bit communication-type characters. (See Figure 2-9 for an example of an 8-bit data character.) The transmitter in the ACLA always appends a start bit to the beginning of each character and 1, 1.5, or 2 stop bits to the end of the character, depending upon how the transmitter is configured. Parity generation is inhibited in the transmitter, but transmitted characters may include a parity bit which was generated in the MLCP.

As shown in Figure 2-10, before the MLCP sends a message, it loads a configuration parameter into the transmitter/receiver (XMTR/RCVR) register by setting CPDT00, 01, and 04 to establish the size of the characters to be transmitted and the number of stop bits to be used. (See Table 2-5.) The ACLA then strobes this configuration information into the transmitter by means of signal CONSTA. (See Table 2-4 and Figures 2-4 and 2-8.) Note that a constant +5V always inhibits parity generation by the transmitter.

When the transmitter is ready to transmit a byte, it causes signal RDYXMA to go true. Then, if either the Clear to Send or the Test Mode Set signal is true and the Request to Send signal is also true, the CJ input to the transmitter ready flip-flop is enabled. Then at the next Ready Flip-Flop Strobe from the MLCP, the flip-flop sends a Ready for a Transmit Data Byte (RDYFXA) to the MLCP. The channel program (output or send) then responds by strobing a data byte to the transmitter (XDTSBA) and resets the Transmitter Request (RDYXMA) line. The ready flip-flop is then reset by the channel program (wait) with a second strobe (XRSRDA). The transmitter then sends the character to the data communication equipment (DCE) in a serial stream with an appended start bit and stop bits as configured. During the transition from the transmitter to the DCE, the voltage level of the bits is changed from the TTL levels of 0V and +5V to +12V and -12V respectively by the EIA logic. (See Figure 2-9).

Complete output messages are sent out byte by byte (in a serial stream) as described above. At the end of the operation, the channel program resets the Request to Send signal to the DCE and turns off the transmitter.

Note in Figure 2-10 that normally, when characters are being transmitted, neither the constantly spacing nor the constantly marking signals are ordered. When the constantly space flip-flop is set in the data set register (Figure 2-6), +12V is constantly sent out to the DCE. When the constantly mark flip-flop is set, -12V is constantly sent out to the DCE.

On the bottom of Figure 2-10 is the logic which comprises the reverse channel receiver. This receiver provides the DCE with a path of communication for sending supervisory signals to the MLCP.

DATA FROM MLCP		TTL LOGIC	OUTPUT RS-232C
BIT	1 or 0	0V	+12V
7	0		
6	1		
5	0	+5V – 12V	
4	0		
3	1		
2	1		
1	0		
0	0		

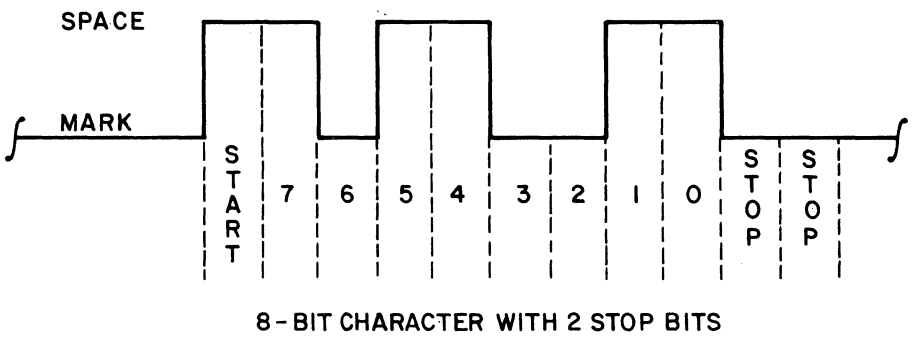


Figure 2-9 Character Example

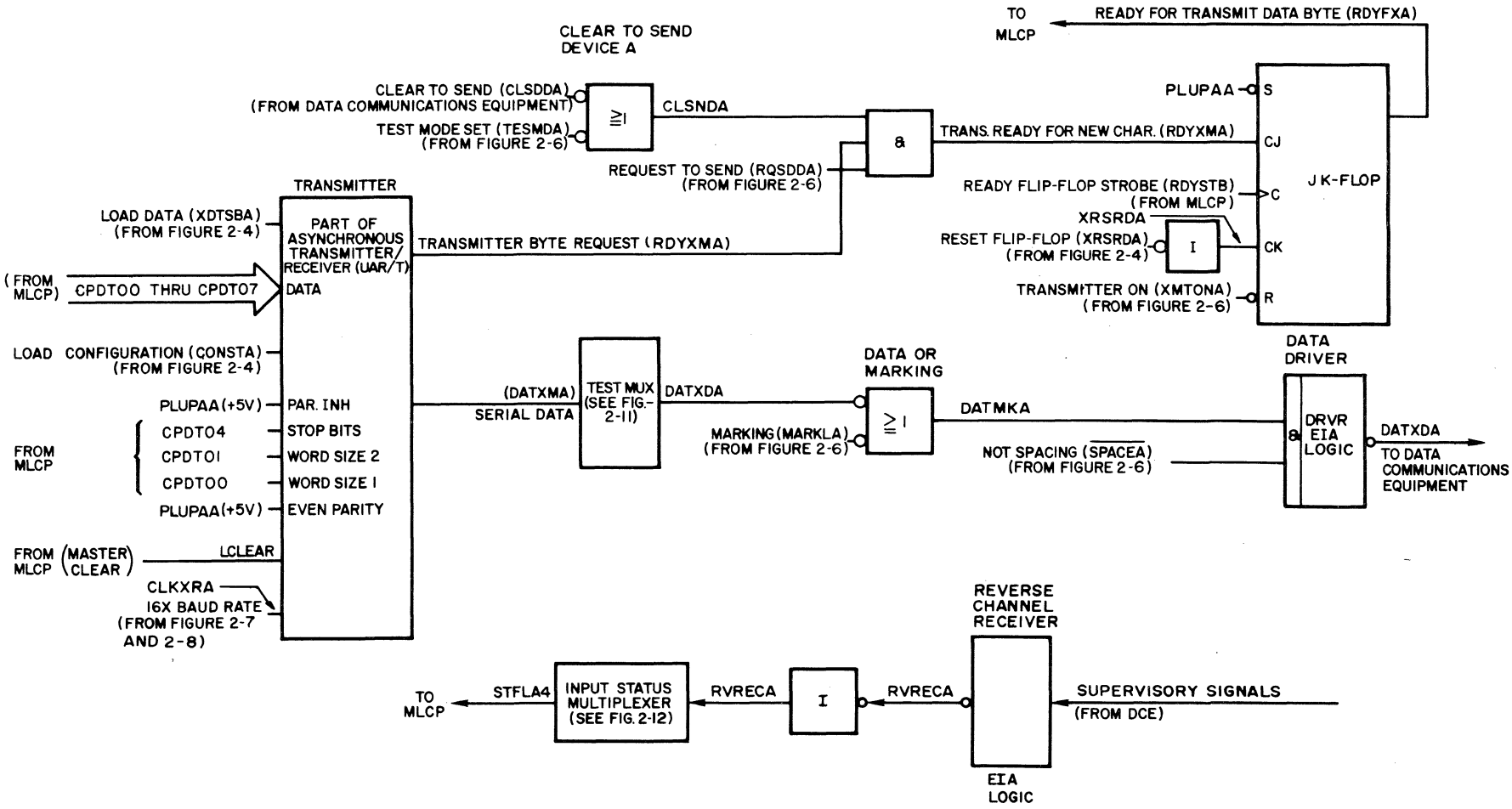


Figure 2-10 Data Output to Data Communications Equipment

2.2.7 Data Input

The ACLA receives data serially from the data communications equipment (DCE) in the form of 5-, 6-, 7-, or 8-bit communication type characters. (See Figure 2-9 for an example of an 8-bit character.) The receiver in the ACLA then strips the start bit and all stop bits from the character prior to sending it to the MLCP in parallel-byte form. The receiver makes no parity checks on received characters. However, characters may have parity bits which are transparent to the receiver but are checked in the MLCP. The receiver checks the character for the presence of a stop bit and generates an error (framing error) signal if a stop bit is not detected. The receiver also generates an error (overrun) signal if it has two data bytes ready before one is transferred into the MLCP.

As shown in Figure 2-11, prior to the beginning of each message, the channel program (output) loads the configuration into the configuration register of the transmitter/receiver (XMTR/RCVR). First it sets (or resets) CPDT00, 01, and 04 to the expected bit size of the characters to be received and the number of stop bits to be seen. (See Table 2-6.) The channel program (output) then strobes this configuration information into the XMTR/RCVR configuration register by means of signal CONSTA (see Table 2-4 and Figures 2-4 and 2-11). Note that PLUPAA (+5V) inhibts parity checking and parity error reporting at all times.

After the receiver is configured, further action does not occur until a data character is serially received from the DCE via the EIA logic (at TTL level at the receiver). (See Figure 2-9.) The receiver then checks the character for a stop bit and, if none is detected, generates an error signal (RAFRER). The start and stop bits are then stripped from the character, and the basic data byte is placed in a holding register in the receiver for transfer to the MLCP. At this time the receiver also enables the CJ input to the receiver ready flip-flop (RDYRCA). Then at the next ready flip-flop strobe (RDYSTB) from the MLCP, signal RDYFRA notifies the MLCP that the receiver has a byte ready to transfer.

To input the data byte from the receiver, the channel program (input or receive) first connects the holding register of the receiver to the MLCP by causing a data enable (DATENA) signal to be issued (see Figure 2-6 and Table 2-4). Then the MLCP transfers the byte with a Received Data Strobe (RDTSBA). This also resets the receiver request (RDYRCA) to the receiver ready flip-flop. The channel program (wait), when ready, resets the ready flip-flop with an RRSRDA signal. Successive bytes are then transferred as described above from the DCE to the MLCP until the input operation is completed.

During an input operation, if no stop bit is detected on a character received from the DCE, a framing error (RAFRER) signal is generated. If the receiver has two characters ready for transfer before one is taken by the MLCP, an overrun (RAOVRN) signal is generated. When either the RAFRER or RAOVRN signal is generated, they will remain set until the receiver processes the next character from the DCE.

On the bottom of Figure 2-11 is the logic which comprises the reverse channel transmitter. This auxiliary transmitter provides a path to the DCE from the MLCP. It is used for transmitting supervisory signals to the DCE.

Table 2-6 Transmitter/Receiver Configuration

CPDT00	CPDT01	CPDT04	START BITS	DATA BITS	STOP BITS
0	0	0	1	5	1
0	0	1	1	5	1.5
0	1	0	1	6	1
0	1	1	1	6	2
1	0	0	1	7	1
1	0	1	1	7	2
1	1	0	1	8	1
1	1	1	1	8	2

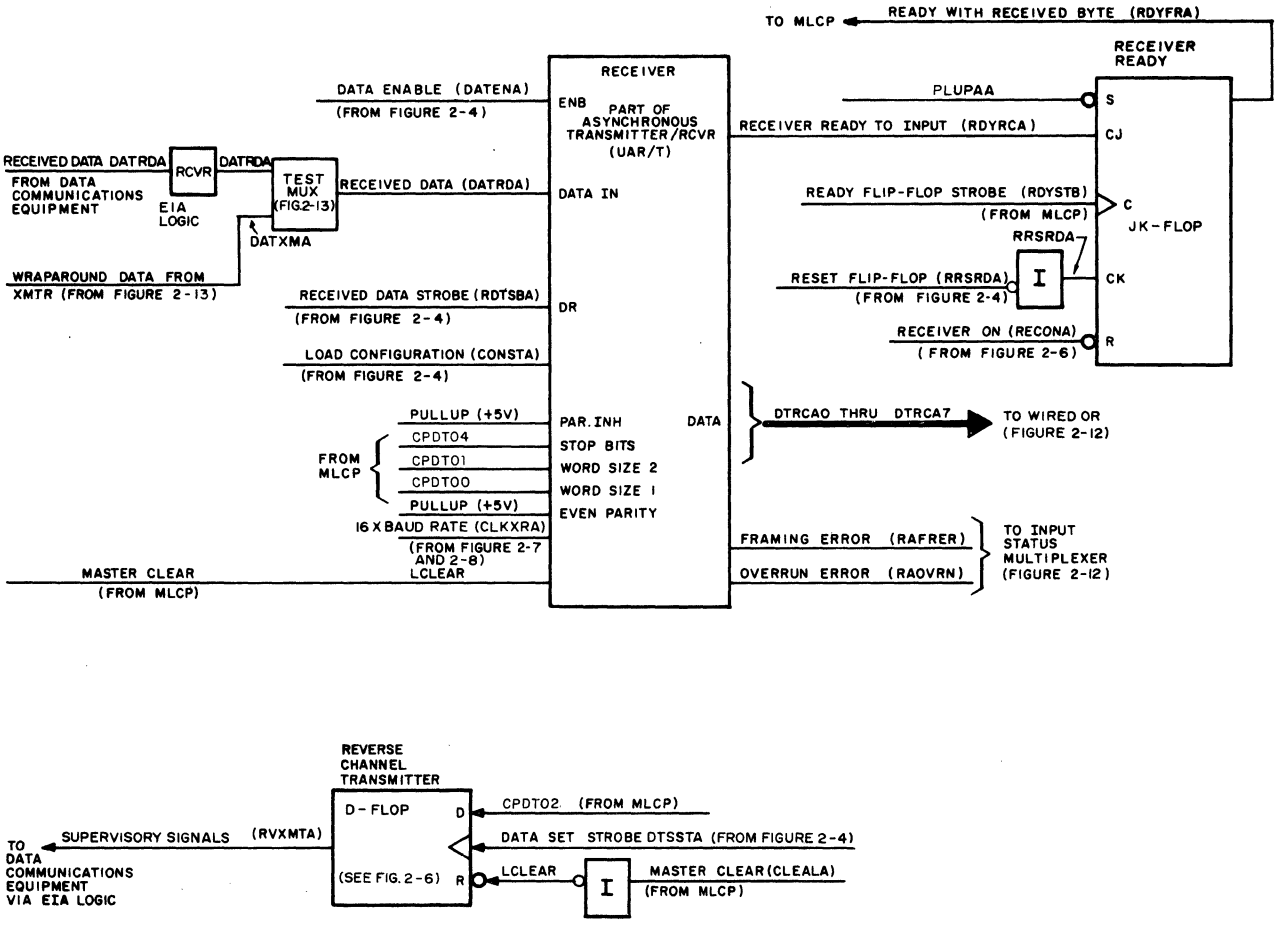


Figure 2-11 Data Input from Data Communications Equipment

2.2.8 Input Status Multiplexer

The input status multiplexer (Figure 2-12) provides a means of sending both error status in the ACLA and status and control information from the data communications equipment (DCE) to the MLCP. The information sent from the multiplexer to the MLCP can originate in either interface A or interface B or in its respective DCE, depending upon the decoding of the control and address lines from the MLCP. When interface B has not been selected ($\overline{SLSTSB}$), the multiplexer assumes that interface A and its associated DCE has been selected.

The multiplexer requires an enable signal because it is a tri-state device. When not enabled, all the outputs of the multiplexer are at infinite impedance (floating), thereby disconnecting all logical inputs from the multiplexer into the MLCP. As shown in Figure 2-12, the multiplexer is enabled when the Select Status signal for either interface A or B is true.

Each output bit of the multiplexer is hardwired to the corresponding data input bit from both interface A and interface B prior to being sent to the MLCP. All data input and status bytes are sent to the MLCP via the LADT00 through LADT07 connections. Table 2-7 lists the source and functions of all inputs into the status input multiplexer.

2.2.9 Test Multiplexer

The test multiplexer (Figure 2-13) provides both interfaces of the ACLA with a wraparound feature. This feature allows serial data out of the transmitter to be sent directly back to the receiver. Diagnostic software uses the wraparound feature to check the operation of the transmitter and receiver by comparing a data byte sent out by the MLCP to the byte received back. Operations with the data communications equipment (DCE) are precluded when the wraparound logic is enabled. Refer to the Appendix for supplemental information pertaining to wraparound.

As shown in Figure 2-13, a zero (ground) is placed on the enabling input of the multiplexer. This, in effect, negates the tri-state feature of the multiplexer so that the outputs are always logically connected to either the selected Zero or One input. When operating on line (test mode not set), the One inputs are connected to the corresponding outputs. This makes the following normal operating connections within the multiplexer.

INPUT	OUTPUT
Line - interface B	Receiver - interface B
Transmitter - interface B	Line - interface B
Line - interface A	Receiver - interface A
Transmitter - interface A	Line - interface A

When the test mode is set, the Zero inputs are connected to the outputs. This makes the following connections in the multiplexer.

INPUT	OUTPUT
Transmitter - interface B PLUPAA (+5V) Transmitter - interface A PLUPAA (+5V)	Receiver - interface B Line - interface B Receiver - interface A Line - interface A

The PLUPAA (+5V) input to the multiplexer keeps the line at the Mark level while the multiplexer is in the test mode (see Figure 2-9).

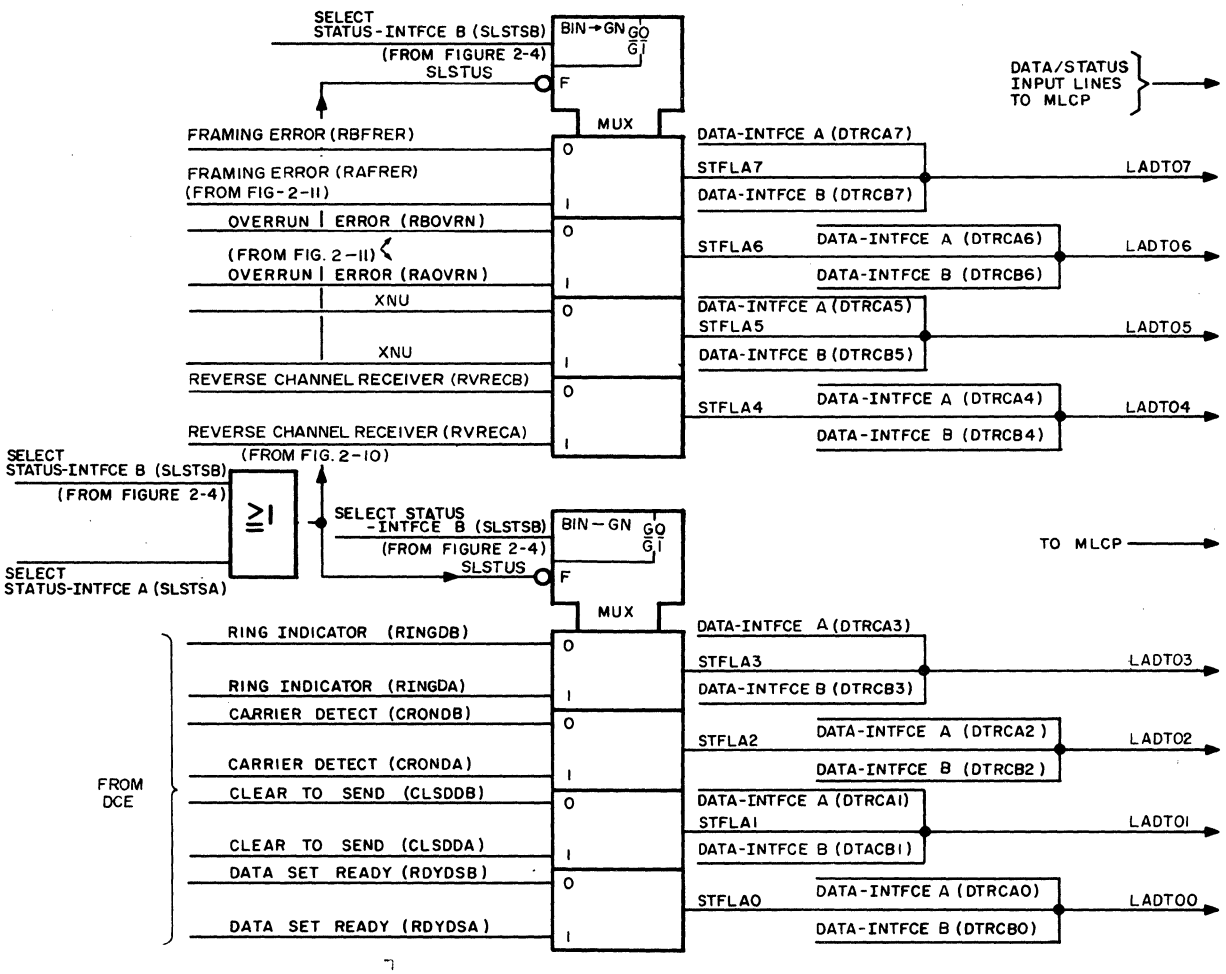


Figure 2-12 Input Status Multiplexer Logic

Table 2-7 Input to Input Status Multiplexer

INPUT SIGNAL	SOURCE	COMMENT
RVRECB RVRECA	DCE of interface B DCE of interface A	Provides a path for supervisory signals to be sent from the DCE to the MLCP.
RBOVRN RAOVRN	Adapter receiver-interface B Adapter receiver-interface A	Indicates that the receiver has two data bytes ready before one is transferred to the MLCP (overrun error).
RBFRER RAFRER	Adapter receiver-interface B Adapter receiver-interface A	Indicates that the receiver has detected no stop bit on the last data character received from the DCE (framing error).
RINGDB RINGDA	DCE of interface B DCE of interface A	The associated line is ringing and is trying to get the attention of the MLCP.
CRONDB CRONDA	DCE of interface B DCE of interface A	Indicates that the basic carrier frequency of the associated communication line is present.
CLSDDB CLSDDA	DCE of interface B DCE of interface A	A response by the associated DCE to a Request to Send signal from the adapter.
RDYDSB RDYDSA	DCE of interface B DCE of interface A	A signal from the associated DCE indicating that it is ready to operate.

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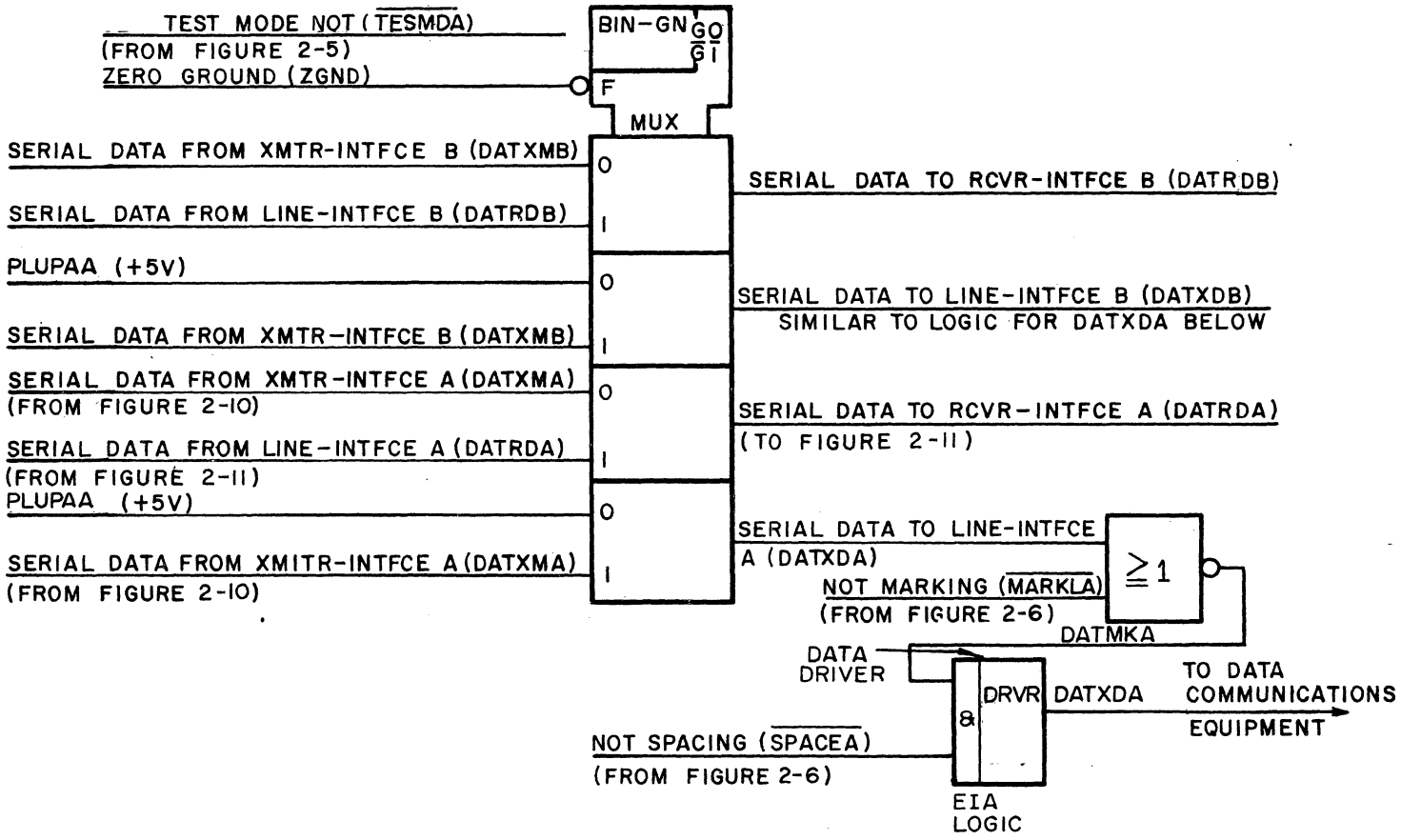


Figure 2-13 Test Multiplexer Logic

III
THEORY OF OPERATION - CYCLE FLOW

The firmware associated with the asynchronous communications line adapter (ACLA) is physically located in the multiline communications processor (MLCP). Because the overall operation of the MLCP firmware is indivisible, it is impractical to describe the functions pertaining to the ACAL separately. Accordingly, the MLCP manual (Document No. 71010230-200) should be used to obtain specific information on firmware related to the ACLA.

APPENDIX A
WRAPAROUND TEST

Through the use of a Test and Verification Program, two wraparound tests can be performed on the ACLA.

The first test, DCMT1-mode A, performs an internal wraparound of the ACLA, checking the integrity of the ACLA to transmit and receive data properly. Serial data is sent out of the transmitter and returned directly back to the receiver. The received data must match the transmitted data to verify integrity.

The second test, DCMT1-mode C, performs an external wraparound of the DCE interface and the DCE cable. This test verifies the integrity of the DCE interface and cable. To perform the external wraparound test, the DCE connectors D and F, at the DCE end of the DCE cable, are terminated by two EIA jumper connectors. These connectors are wired as indicated in the following table.

For information pertaining to the sequence of steps required to run these programs, refer to the Level 6 System Checkout and Operator's Guide. For cabling information, refer to the Model 34/36 Systems Manual.

EIA Connector Jumpers for
DCMT1-Mode C Loop Test

EIA CONNECTOR PIN NUMBERS TO BE JUMPERED	INTERFACE SIGNAL NAMES
02 to 03	Transmit Data to Receive Data
06 to 20	Data Set Ready to Terminal Ready
04 to 05 to 08	Request to Send to Clear to Send to Carrier Detect
14 to 15	Used in SCLA (Optional in ACLA)
17 to 22 to 23 to 25	Jumper to 17, optional in ACLA - Ring Indicator (22) to Reverse Channel Transmitter to Reverse Channel Receiver

APPENDIX B
CABLING

The Type DCM9101 Dual Asynchronous Communications Line Adapter (ACLA) is cabled in accordance with the system configuration, which may specify one of three possible environments.

In most system configurations, the Communications-Pac is connected to the data communications equipment (DCE) or to a remote Communications-Pac via modems and a telephone line. Figure B-1 illustrates a typical communications configuration and identifies the type of cable used and the connector type, i.e., male (M).

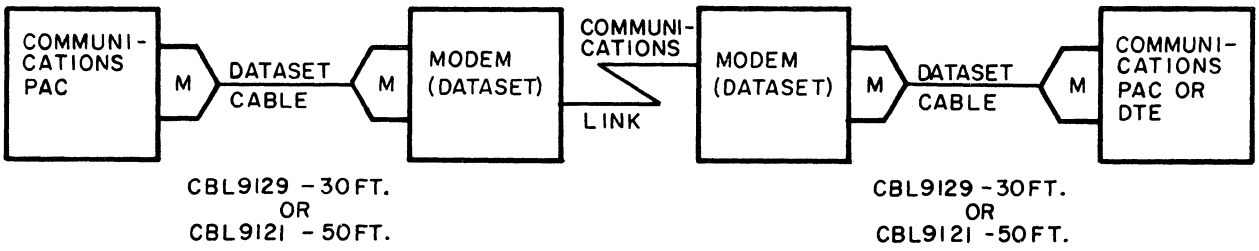
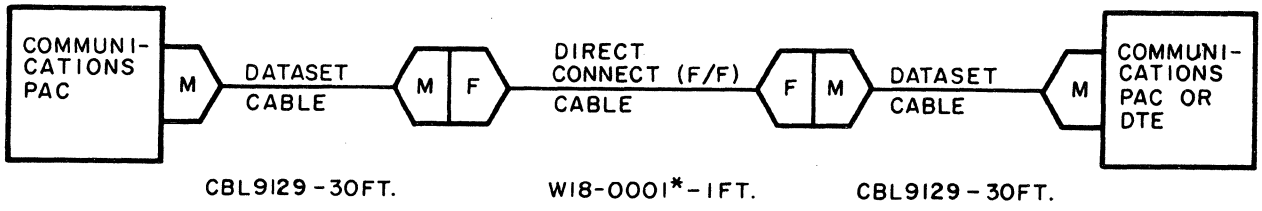


Figure B-1 Typical Modem Configuration

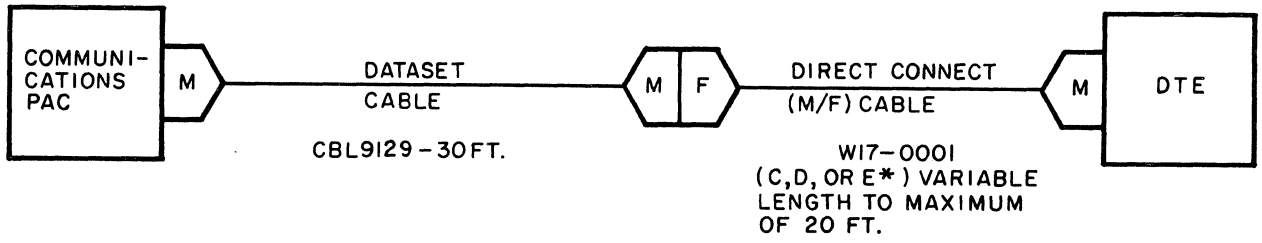
The system can also be configured for either of two direct connect applications. If the two pieces of equipment are close to each other (less than 61 feet apart for RS232C applications), a short jumper cable (direct connect female to female) replaces the modem/telephone line combination. Figure B-2 shows the cabling requirements for this configuration, i.e., two data set cables with male (M) connectors and one direct connect cable with female (F) connectors.



*CONNECTORS ASSEMBLED TO BOTH ENDS

Figure B-2 Direct Connect Female/Female

For direct connect applications, where the Communications-Pac is connected directly to another Connunications-Pac or to data terminal equipment without the use of data communications equipment, the use of a direct connect cable (male or female) and a dataset cable is required. One cable cannot be used for this application due to signal inconsistencies at the connector pinouts. Figure B-3 shows the cable requirements for this configuration, i.e., one data set cable with male connectors (M) and one direct connect cable with a male (M) and a female (F) connector. The total combined length of the two cables must not exceed 50 feet.



* C-CONNECTORS ASSEMBLED TO BOTH ENDS
D-DISASSEMBLED WITH TWO CONNECTORS SHIPPED UNATTACHED
E-ONE CONNECTOR ASSEMBLED TO CABLE (PADDLE BOARD SIDE); THE OTHER CONNECTOR SHIPPED BUT NOT ATTACHED.

Figure B-3 Direct Connect Male/Female

USERS' REMARKS FORM

TITLE:

DOC. PART NO. _____

DATED _____

ERRORS NOTED:

Fold

SUGGESTIONS FOR IMPROVEMENT:

Fold

DATE _____

FROM: NAME _____

COMPANY _____ M/S _____

TITLE _____

ADDRESS _____

_____ ZIP _____

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