SERIES 60 (LEVEL 6)

COMMUNICATIONS HANDBOOK

ADDENDUM B

SUBJECT

Corrections and Changes to the Handbook, and a New Appendix, Covering the Synchronous Broadband HDLC Communications-Pac

SPECIAL INSTRUCTIONS

This is the second addendum to Revision 2, dated October 1978. Bars in the margins indicate technical changes and additions; asterisks denote deletions. Appendix H, being entirely new, does not contain change bars or asterisks.

Note:

Insert this cover after the manual cover to indicate the updating of the document with Addendum B.

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COLLATING INSTRUCTIONS

To update this manual, remove old pages and insert new pages as follows:

Remove	Insert
vii, viii	vii through x
2-11, blank	2-11, blank
3-5 through 3-8	3-5 through 3-8
4-13 through 4-16	4-13 through 4-16
4-23, 4-24	4-23, 4-24
5-5, 5-6	5-5, 5-6
D-1, D-2	D-1, D-2
—	H-1 through H-65

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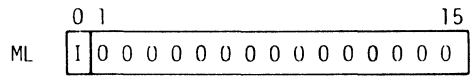
Figures

Tables

IO (Output MLCP/DLCP Control) Instruction

This instruction (function code: 01) transfers, from ML, a control word to the Processor. All Processor channels are affected by this control word. Any channel can be specified in CF, provided that channel is serviced by an adapter.

The format of ML is shown below.



If *I* is set to 1, MLCP initialization will be performed; otherwise, no action is taken. DLCP initialization will occur unconditionally (i.e., the value of *I* may be 1 or 0). Initialization comprises the following actions:

- o The Processor executes its basic logic test.
- o Each line register 2 of each adapter is reset to zero; channel request interrupts are thus inhibited.
- o All of RAM is reset to zero.
- o LCT byte 1 of channel 0 contains the hexadecimal number of the firmware revision.
- o All channels are initialized. (This operation is described under the "IO (Output Channel Control) Instruction," earlier in this section.)
- o The Processor is placed in a quiescent state; no interrupts or data transfers can occur.
- o Clears the adapters.

Soft Initialize

The pressing of the Clear (CLR) push button on the central processor control panel causes the Processor to perform a "soft initialize" which does the following:

- o Clears the adapters.
- o Clears LCT bytes 8, 9, 40 and 41 of each channel.
- o Clears the Processor internal registers.

The soft initialize differs from the hard initialize caused by the command Output Processor Control (code: 01) in that the hard initialize, in addition to performing the soft initialize functions defined above, also clears the RAM (software-visible).

When in a software debug mode, it is preferable that the RAM not be cleared so that meaningful dumps can be taken to indicate the Processor condition.

The contents of the address field are increased as data characters are physically transferred between the CDB and the MLCP based on the CCP's execution of format 1 LD (Load) or ST (Store) instructions.

The address field value is increased by *1* each time execution of a format 1 LD (Load) or ST (Store) instruction causes *one* data character to be physically transferred between the CDB and the MLCP. This case applies only upon execution of the first (or last) LD or ST instruction pertaining to a CDB that begins (or ends) at an odd byte boundary.

The address field value is increased by *2* each time execution of a format 1 LD (Load) or ST (Store) instruction causes *two* data characters to be physically transferred between the CDB and the MLCP. This case applies upon execution of the *first* of two LD instructions or upon execution of the *second* of two ST instructions. (Execution of the *second* LD instruction or of the *first* ST instruction does not cause a physical data transfer between the CDB and the MLCP; hence the address field value is not increased as either of these instructions is executed.)

DLCP

The *address* field occupies bytes 0, 1, and 2 of the CCB. This field is written from the main memory program by an IOLD (Output CCB Address and Range) instruction. When first written, the address field contains the starting *word* address of a CDB in the main memory program; the low-order end of the starting byte address is contained in byte 1 of the CCB. Bits 6 and 7 of byte 2 contain the two most significant bits (refer to Figure 3-2) of the address with bit 6 the high-order bit.

The address field value is increased by one every *second* time a format 1 LD or ST instruction is issued, which action causes a word to be physically transferred between a CDB and the DLCP.

NOTE: The format 1 LD or ST is a byte transfer and therefore two uses are required to transfer a word.

An exception to this occurs at an odd byte boundary, in which instance the address field value is increased by one when the *first* format 1 LD or ST causes the first *byte* to be physically transferred between a CDB and the DLCP. (An odd byte boundary would normally occur only on the very first format 1 LD or ST.)

CCB Range Field

The *range* field occupies bytes 3 and 4 of the CCB. This field is written from the main memory program by an IOLD (Output CCB Address and Range) instruction. When first written, the range field indicates the number of bytes in the CDB. The low-order end of the range value is contained in byte 3 of the CCB for the MLCP and in byte 4 for the DLCP.

The contents of the range field are decreased by 1 each time a format 1 LD (Load) or ST (Store) instruction is executed in the CCP (regardless of whether that instruction causes a physical data transfer between the CDB and the Processor).

CCB Control Field

The *control* field occupies byte 5 of the CCB. The control field is written from the main memory program by an IO (Output CCB Control) instruction. The format and significance of this field are shown below.

0	1	2	3	4	5	6	7
I	V	LB	0	0	0	0	0

I – Interrupt V – Valid LB – Last Block

Bit 0 – interrupt control
- 0 – No action.
- 1 – Interrupt the main memory program when this CCB is marked as completed (CCB byte 7, bit 3 for MLCP; CCB byte 6 bit 3 for DLCP). The interrupt will occur at the interrupt level assigned to this channel. If no interrupt level has been assigned, no interrupt will occur.

Bit 1 – "valid" CCB
- 0 – This is not a "valid" CCB; it cannot be used as an "active" CCB. This condition exists before this bit is set to 1 by an IO (Output CCB Control) instruction. This bit is reset to 0 by firmware when this CCB is marked as completed (bit 3 of CCB byte 7 (MLCP), byte 6 (DLCP) after it has been used during processing of a CDB.
- 1 – This is a "valid" CCB; it is usable as an "active" CCB. This bit must be set to 1 complete setup of the CCB.

Bit 2 – last CDB
- 0 – No action.
- 1 – This CCB pertains to the last CDB in a message. This is a flag that can be used by the CCP for special processing of the last CDB in a message. If this bit is set to 1, the Processor's LB-indicator will be set to 1 when this CCB is "active." The CCP can test the LB-indicator by means of BLBT (Branch if Last Block True) and BLBF (Branch if Last Block False) instructions.

CCB Status Field

The *status* field comprises bytes 6 and 7 of the CCB. The CCB status field is reset to zero as setup of the CCB is completed by execution of an IO (Output CCB Control) instruction. Later, as processing ends relative to a CCB, its status field is updated by firmware and the CCB status complete bit (CCB byte 7, bit 3 for MLCP and byte 6, bit 3 for DLCP) is set to 1. (Table 3-1 indicates the conditions under which processing relative to a CCB can end.)

The CCB status field is updated with information from the two LCT status bytes combined with other information. The LCT status bytes are bytes 16 and 17 for a receive channel and bytes 48 and 49 for a transmit channel. Once the status field of the CCB has been updated, the CCB's status is said to be "meaningful."

The status bytes of the "status" CCB can be read from the main memory program, whenever appropriate, by an IO (Input CCB Status) instruction. An IO (Input Next CCB Status) instruction moves the "status" CCB pointer to the following CCB (which then becomes the "status" CCB) and reads the status field of this new "status" CCB.

The format of the two bytes of CCB status field is shown on the following page. The entire word is passed from the LCT status bytes. Note that, in the CCB status field, status byte 1 is stored *above* status byte 2; this order is the opposite of the order of the status bytes in the LCT.

Status Byte 1
(CCB Byte 7, MLCP) (CCB Byte 6, DLCP)

Bit 0 interrupt main memory program from CCP
- 0 No action.
- 1 The main memory program has been interrupted due to execution of an INTR instruction in the CCP.

	0	1	2	3	4	5	6	7
BYTE 6 CCB STATUS BYTE 2	RESERVED	DATA CHECK ERROR	RECEIVE NONZERO RESIDUAL RANGE TRANSMIT LAST BLOCK (SEE NOTE)	DATA SET OR COMMUNICA-TIONS-PAC STATUS CHANGE	CORRECTED MEMORY ERROR	INVALID MEMORY ADDRESS	MEGABUS PARITY ERROR	UNCORRECTED MEMORY ERROR
BYTE 7 CCB STATUS BYTE 1	INTERRUPT MAIN MEMORY PROGRAM FROM CCP	INTERRUPT MAIN MEMORY PROGRAM FROM CCB	DATA SERVICE ERROR	CCB STATUS COMPLETE	CCB SERVICE ERROR	FOR PROGRAMMING USE	FOR PROGRAMMING USE	RESERVED

NOTE: For transmit, bit 2 equals last CCB block.

Figure 3-3. MLCP CCB Status Bytes 1 and 2

	0	1	2	3	4	5	6	7
BYTE 6 CCB STATUS BYTE 1	INTERRUPT MAIN MEMORY PROGRAM FROM CCP	INTERRUPT MAIN MEMORY PROGRAM FROM CCP	DATA SERVICE ERROR	CCB STATUS COMPLETE	CCB SERVICE ERROR	FOR PROGRAMMING USE	FOR PROGRAMMING USE	RESERVED
BYTE 7 CCB STATUS BYTE 2	RESERVED	DATA CHECK ERROR	RECEIVE NONZERO RESIDUAL RANGE TRANSMIT LAST BLOCK	DATA SET OR COM-MUNICATIONS PAC STATUS CHANGE	RESERVED	RESERVED	RESERVED	UNCORRECTED MEMORY ERROR OR INVALID MEMORY ERROR

NOTE: FOR TRANSMIT, BIT 2 EQUALS LAST CCB BLOCK.

Figure 3-4. DLCP CCB Status Bytes 1 and 2

Bit 1 – interrupt main memory program
- 0 – No action.
- 1 – The main memory program has been interrupted when processing ends relative to this CCB. This bit is set to 1 in either of two cases: (1) if bit 0 of CCB byte 5 has been set to 1 – by an IO (Output CCB Control) instruction in the main memory program or (2) if bits 0 and 2 of LCT byte 8/40 have been set to 1 and a data set or adapter status change has been recorded in LCT byte 14/46 (Data Set Scan).

Bit 2 – data service error
- 0 – No data service error has occurred.
- 1 – A data "timing window" has been missed. On receive, the adapter has detected a receive overrun (see bit 6 of LCT byte 14/46 in Section 5). On transmit, the adapter has detected a transmit underrun (see bit 7 of LCT byte 14/46 in Section 5).

Bit 3 – CCB status complete

This bit is always set to 1 as the CCB status field is written by Processor firmware. This setting indicates that processing relative to this CCB has ended and the contents of its status field are meaningful. Table 3-1 indicates the conditions under which processing relative to a CCB can end.

Bit 4 – CCB service error
- 0 – No CCB service error has occurred.
- 1 – This bit setting pertains to an error that occurred before this CCB became "valid."

On receive, a format 1 ST (Store) instruction was attempted when there was no "valid" CCB. The instruction was not executed; instead, Processor firmware set this bit to 1 (in LCT status byte 1) and proceeded to the next sequential instruction in the CCP.

On transmit, a format 1 LD (Load) instruction was attempted when there was no "valid" CCB. The instruction was not executed; instead, Processor firmware set this bit to 1 (in LCT status byte 1), returned the CCP pointer to the address of this LD instruction, and executed a WAIT (Wait) instruction. At the next channel request interrupt for this channel, this instruction was attempted again.

See the description of bit 4 of LCT byte 16/48 in Section 5.

Bits 5 and 6 – for programming use

Within LCT status byte 1, these two bits can be used by the CCP for application-specific purposes. Later, when the contents of the LCT status bytes are transferred to the CCB status field, these two bit positions become available for scrutiny by the main memory program as it issues an IO (Input CCB Status) or IO (Input Next CCB Status) instruction. Thus, these two bit positions can be used as a means for the CCP to pass application-specific status information to the main memory program.

Status Byte 2
(CCB Byte 6, MLCP) (CCB Byte 7, DLCP)

Bit 1 – data check error
- 0 – No data check error has occurred.
- 1 – A data parity error has been detected by firmware, or the CCP has set this bit after detecting a cyclic redundancy check error. (In both cases, this bit setting is relevant only to receive operations.)

Bit 2 – CCB nonzero range residue for receive only (see "NOTE" on previous page under diagram)
- 0 – No CCB range residue exists.
- 1 – The CCB has been terminated before its range field value decreased to 0.

Bit 2 – last block for transmit only
- 0 – Not last block
- 1 – Last block

Bit 3 – data set or adapter status change
- 0 – No data set or adapter status change has been recorded.
- 1 – Bits 0 and 1 of LCT byte 8/40 were set to 1 and a data set or adapter status change was recorded in LCT byte 14/46.

Bit 4 – corrected memory error (MLCP only; bit not used in DLCP)
- 0 – No corrected memory error has occurred.
- 1 – One or more hardware-corrected memory errors occurred in the CDB related to this CCB.

Bit 5 – invalid memory address (MLCP only; bit not used in DLCP)
- 0 – No invalid memory address has occurred.
- 1 – A reference to a CDB has resulted in an invalid memory address on the Megabus; main memory has issued a NAK. This condition has caused the CCB to be terminated.

Bit 6 – Megabus parity error (MLCP only; bit not used in DLCP)
- 0 – No Megabus parity error has occurred.
- 1 – Incorrect parity existed on the Megabus as a data character was transferred *to* the MLCP. This condition has caused the CCB to be terminated.

TABLE 4-8. TIMINGS FOR GENERIC INSTRUCTIONS

Instruction	MLCP (μs)	DLCP (μs)
NOP	1.7	2
WAIT	15.0 (Note 1)	41.0 (Note 3)
GNB	n (Note 2)	n (Note 4)
SFS	5.6	21-71
CCH	8.4	Note 5
DEC	2.0	2
RET	4.9	8
SR	2.4	2
INTR	11.0	125-154
INZ	200.00	650

NOTES:

1. (MLCP)
   This figure includes the time necessary to perform a context swap from the currently running CCP to the next CCP (approximately 8 μs).

2. (MLCP)
   GNB-receive mode and previously active CCB causes interrupt to central processor: 32.2 μs
   GNB-receive mode without interrupt: 25.2 μs
   GNB-transmit mode with interrupt: 28.8 μs
   GNB-transmit mode without interrupt: 21.8 μs

3. (DLCP)
   This figure includes the time only to suspend the currently executing CCP.

4. (DLCP)
   GNB-receive mode and previously active CCB causes interrupt to central processor: 239 μs
   GNB-receive mode without interrupt: 120 μs
   GNB-transmit mode with interrupt: 314 μs
   GNB-transmit mode without interrupt: 195 μs

5. (DLCP)
   Timings for CCH are as follows:
   49 μs for LRC
   73 μs for CRC 16
   73 μs for CRC ITT
   82 μs for CRC 12

TABLE 4-9. MLCP BIT MAP OF CCP EXECUTABLE INSTRUCTIONS' OP CODE WORDS – RECEIVE MODE

Instruction Type/Format	Bits 0-3 (Bit 0= MSB)	Bits 4-7 (Bit 7 = LSB)															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Generic	0	NOP	WAIT	GNB	SFS	CCH	DEC	RET	SR	INTR	INZ						
Double Operand – Reference to CDB	1		ST														
Input Output IN[a]	2	LR0	LR1	LR2	LR3	LR4	LR5	LR6	LR7								
Input Output OUT[a]	3	LR0	LR1	LR2	LR3	LR4	LR5	LR6	LR7								
Reserved	4																
Double Operand – Reference to LCT Byte n	5	LD	ST	C	AND	OR	XOR	TLU									
Reserved for transmit channel[c]	6																
Reserved	7, 8																
Double Operand-Reference to IMO	9	LD		C	AND	OR	XOR										
Send Receive RECV	A	RECV 0 No Parity or CRC[b]	RECV 1 CRC[b]	RECV 2 Parity[b]	RECV3 Parity and CRC[b]												
Reserved	B,C,D																
Branch – Branch True	E	B	BET	BZT	BLCT	BLBT	BART	JUMP	BVBT								
Branch – Branch False	F	BS	BEF	BZF	BLCF	BLBF	BART		BVBF								

[a]Existence of line register is dependent on type of Communications-Pac being used. If a nonexistent line register is used in the IN or OUT statement, the statement will be treated as a no-op.

[b]Indicates whether the parity check and/or cyclic redundancy check information in LCT byte 2 applies to the data character being transferred to the MLCP's R-register from the receive channel's line register 1 in the Communications-Pac.

[c]Do not use.

TABLE 4-10. MLCP BIT MAP OF CCP EXECUTABLE INSTRUCTIONS' OP CODE WORDS – TRANSMIT MODE

Instruction Type/Format	Bits 0-3 (Bit 0= MSB)	Bits 4-7 (Bit 7 = LSB)															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Generic	0	NOP	WAIT	GNB	SFS	CCH	DEC	RET	SR	INTR	INZ						
Double Operand– Reference to CDB	1	LD															
Input/Output – IN[a]	2	LR0	LR1	LR2	LR3	LR4	LR5[a]	LR6	LR7								
Input/Output – OUT[a]	3	LR0	LR1	LR2	LR3	LR4	LR5	LR6	LR7								
Reserved	4																
Double Operand– Reference to LCT Byte n	5	LD	ST	C	AND	OR	XOR	TLU									
Send/Receive–SEND	6	SEND0 No Parity or CRC[b]	SEND1 CRC[b]	SEND2 Parity[b]	SEND3 Parity and CRC[b]												
Reserved	7, 8																
Double Operand– Reference to IMO	9	LD		C	AND	OR	XOR										
Reserved for Receive Channel[c]																	
Reserved	B,C,D																
Branch– Branch True	E	B	BET	BZT	BLCT	BLBT	BART	JUMP	BVBT								
Branch– Branch False	F	BS	BEF	BZF	BLCF	BLBF	BARF		BVBF								

[a]Existence of a line register is dependent on type of Communications-Pac being used. If a nonexistent line register is used in the IN or OUT statement, the statement will be treated as a no-op.

[b]Indicates whether the parity generation and/or cyclic redundancy check information LCT byte 34 applies to the data character being transferred from the MLCP's R-register to the transmit channel's line register 1 of the Communications-Pac. The parity generation is done before the CRC operation (i.e., the parity bit is included in the CRC calculation).

[c]Do not use.

Branch Instructions

Fifteen (MLCP) or thirteen (DLCP) branch instructions are available to the CCP. The BART and BARF branch instructions are not available to the DLCP.

In the discussion that follows, differences between the MLCP and DLCP are noted with respect to displacement and internal instruction format. The expanded formats shown for DLCP should be understood in terms of the number of bytes for the expansion. The contents of these bytes are for DLCP firmware and microprocessor use only and are not visible to the user.

Short Displacement Instructions

Format of Short Displacement Macro Call:

macro-name operand (comments)

macro-name

B BS BET BEF BZT BZF BLCT BLCF BLBT BLBF BVBT BVBF (MLCP and DLCP)
BART BARF (MLCP only)

operand

An internal value expression that identifies the target of the branch instruction.

MLCP: The displacement d is between the current byte address and the target byte address and must be in the following range:

$-128 \leq d \leq +127$

The displacement is from P (the current value of the MLCP P-register, which is pointing to the byte that contains the displacement).

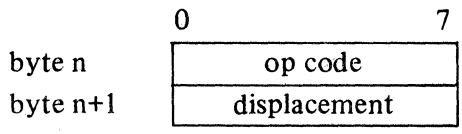
DLCP: The displacement d is from the byte address of the next op code to the target byte address and must be in the following range:

$-128 \leq d \leq +127$

The displacement is from P+1 (P is the current value of the DLCP P-register).

Internal Format of Instructions:

MLCP: All short displacement branch instructions for the MLCP have the same internal format as follows. Recall that displacement is from the current byte address.

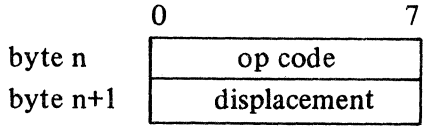


$-128 \leq d \leq +127$

DLCP: The internal formats are shown in the diagrams that follow. The actual byte contents are not visible to the user. Recall that displacement is from the byte address of the next op code.

Instruction: Branch (B)

Internal Format:



$-128 \leq d \leq +127$

XOR (Exclusive OR) – Perform an exclusive OR operation on the contents of the R-register and the contents of byte n of the LCT for this channel. Store the results of this operation in the R-register.

TLU (Table Look-Up) – This instruction permits the contents of a "table location" in RAM to be evaluated so as to produce either a "translation" of the contents of that location or a branch to another location in the CCP. Appendix A provides a sample use of the TLU instruction.

Examples:

```
LD 31
LD WORK
LD WORK+2
```

Format 3

Double operand instructions in this format refer to the R-register and an immediate operand.

All of the double operand instructions usable in this format are valid in either transmit or receive mode.

Format of Macro Call:

macro-name=operand(comments)

macro-name

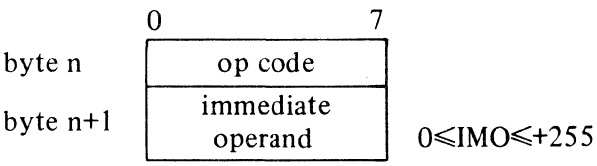
LD C AND OR XOR

operand

An internal value expression that, when resolved, is an integer value from 0 to 255, inclusive. This integer value is an immediate operand, which is stored directly after the byte that contains the op code. Note that the internal value expression must be preceded by an equals sign (in the macro call).

Internal Format of Instructions:

MLCP:

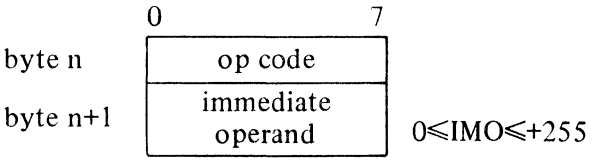


0≤IMO≤+255

DLCP:

Instructions: LD AND OR XOR

Format:



0≤IMO≤+255

Instruction: Compare (C)

Format:

	0 7	
byte n	op code	
byte n+1	immediate operand	
byte n+2	op code	
byte n+3	op code	
byte n+4	constant	0≤IMO≤+255

Description of Instructions

LD (Load) – Load the immediate operand into the R-register.

C (Compare) – Compare the immediate operand with the contents of the R-Register. If the comparison is equal, set the E-indicator to 1; otherwise, reset it to 0.

AND (Logical AND) Perform a logical AND operation on the immediate operand and the contents of the R-register. Store the results of this operation in the R-register.

OR (Inclusive OR) – Perform an inclusive OR operation on the immediate operand and the contents of the R-register. Store the results of this operation in the R-register.

XOR (Exclusive OR) Perform an exclusive OR operation on the immediate operand and the contents of the R-register. Store the results of this operation in the R-register.

Examples:

```
LD =X'02'
LD =STX        NOTE: Format must conform to the macro preprocessor.
LD =VAL+2
```

Input/Output Instructions

These instructions are used to transfer control, synchronization, transmit fill, status, and character configuration information between the Processor R-register and the appropriate line registers of a line adapter. The input/output instructions can also be used to transfer data characters between the Processor and line register 1 of an adapter; however, input/output instructions do not provide parity checking or generation, cyclic redundancy checking, or receive overrun or transmit underrun checking and notification.[3]

Format of Macro Call:

macro-name operand (comments)

macro-name

IN,OUT

operand

An internal value expression that, when resolved, is an integer value from 0 to 7, inclusive. This integer is the number of an adapter line register that will be read or written.

NOTE: The line register must be legitimate for the connected adapter. If the register does not exist and the instruction is in the CCP, the IN or OUT will be treated as no-op. The IN will cause the R-register to be altered.

[3] Send/receive instructions, described in the following subsection, offer these capabilities.

execution of SEND (Send) and RECV (Receive) instructions whose operand values are 1 or 3. The resultant cyclic redundancy check residue in LCT bytes 3/35 and 4/36 may be examined from the CCP. These bytes must be initialized by the CCP or the main memory program whenever a block CRC calculation is restarted. LRC is in bytes 3/35; and LCT 4/36 is zeros.

The appropriate initial value for LCT byte 3/35 and 4/36 is all 1s for a CRC polynomial code equal to 01 (HLDC) (MLCP only). For the other CRC polynomial codes (CRC 16, LRC, CRC 12), the appropriate initial value is all zeros (MLCP and DLCP). The program, typically the CCP, must ensure that these initial values are provided.

Byte Layout:

The format of these bytes is governed by which cyclic redundancy check polynomial is used; see Section 6.

LCT BYTES 6/38 AND 7/39 – CCP POINTER

Description:

These bytes store the 12-bit RAM address at which the CCP will begin execution when it is started again. When the Processor services this CCP, this RAM address will be loaded into the P-register (program counter).

Programming Considerations:

The initial starting address of the CCP must be written into these bytes from the main memory program.

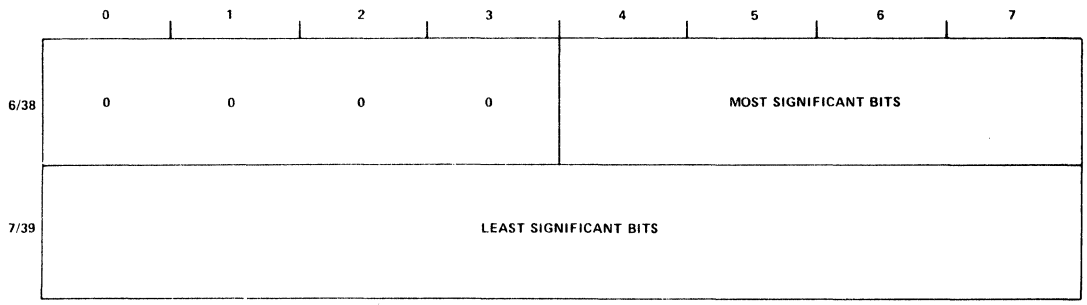
During processing, Processor firmware uses these bytes to store the contents of the P-register whenever the CCP executes a WAIT (Wait) instruction or whenever a firmware pause occurs (MLCP only) or the executing CCP is swapped out (DLCP). When the CCP resumes, firmware restores the contents of these bytes to the P-register, thereby allowing the CCP to begin at its next sequential instruction.

The contents of these bytes may be modified from the main memory program, if you wish to have the CCP resume at an address other than the one stored here. IO (Output LCT Byte) instructions can be used for this purpose. However, the CCP must not be running at the time or the results are unspecified.

When LCT byte 6/38 is written, bits 0 through 3 must always be reset to zero.

These bytes must not be modified by the CCP.

Byte Layout:



LCT BYTE 8/40 – CHANGE CONTROL FOR DATA SET AND ADAPTER STATUS

Description:

This byte may be written from the CCP to control (1) whether the Processor firmware will scan for changes in data set status and line adapter (Communications-Pac) status, recording these changes in LCT byte 14/46 and (2) what action(s) will be taken when a status change is recorded. (A mask in LCT byte 15/47 governs exactly which types of status change will cause LCT byte 14/46 to be updated with the contents of adapter line register 5.)

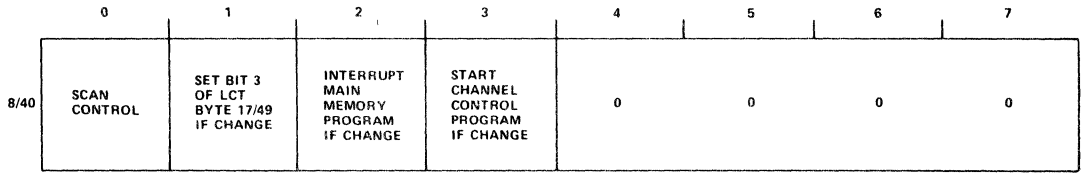
Programming Considerations:

This byte may be initially written from the main memory program or from the CCP. It may subsequently be changed by either program – at points in time appropriate to the communications application.

Whenever this byte is written, bits 4 through 7 must always be reset to zero. If bits 2 and 3 are both set to 1, only bit 2 (terminate the active CCB and interrupt the main memory program) will be acted upon when a data set or adapter status change is recorded in LCT byte 14/46.

Refer also to the programming guidelines in Appendix A.

Byte Layout:



Bit 0 – scan control
- 0 – The Processor firmware will not scan adapter line register 5 for changes in data set status and adapter status.
- 1 – The Processor firmware will scan adapter line register 5 for changes in data set status and adapter status. Firmware will write the entire contents of line register 5 into LCT byte 14/46 whenever it detects a difference between the contents of a bit position in line register 5 and the contents of the same bit position in LCT byte 14/46 *(provided* there is a 1 in the corresponding bit position of the mask contained in LCT byte 15/47). Next, the action(s) specified in bits 1, 2, and 3 of LCT byte 8/40 will be taken.

Bit 1 – set bit 3 of LCT byte 17/49 if change
- 0 – No action.
- 1 – When a data set or adapter status change is recorded in LCT byte 14/46, set to 1 bit 3 of LCT byte 17/49 (LCT status byte 2).

Bit 2– interrupt main memory program if change (refer also to LCT status byte 16/48)
- 0 – No action.
- 1 – When a data set or adapter status change is recorded in LCT byte 14/46, terminate the active CCB and interrupt the main memory program at the interrupt level established for this channel. (Ignore the setting of bit 3 of this byte and set bit 1 of LCT status byte 16/48.)

Appendix D

Synchronous Line Communications-Pacs/Adapters

A Synchronous Line Communications-Pac/Adapter (Type DCM9103 or DCM9104 (MLCP) and Type DCM9302 or DCM9303 (DLCP)) provides an interface between the MLCP or DLCP respectively, and one or two completely independent synchronous communications lines.[1] For each line, the synchronous line adapter provides the following services:

- o Serial/parallel data conversion for synchronous bit-serial data transfers
- o Character synchronization by use of a synchronization character such as the ASCII SYN
- o Control of data sets
- o Monitoring of data set status

Each communications line comprises a receive channel and a transmit channel and is thus capable of half-duplex or full-duplex data communications operations. Each line has a clocked, independently configurable speed (up to 20,000 bits per second for MLCP or up to 9600 bits per second for DLCP)[2] and an independently configurable data character size (from five to eight bits—including parity, if used); each channel of a line uses the configured line speed and data character size. The synchronous line adapter supports BSC, Basic Mode ASCII, and similarly formatted control procedures.

The following data communications equipment and data terminal equipment is supported through an EIA RS-232-C interface:

- o Bell System 201A, B, C, or equivalent
- o Bell System 203A, B, or equivalent
- o Bell System 208A, B, or equivalent
- o Bell System 209 or equivalent

Figure D-1 illustrates the Synchronous Line Communications-Pac's interface position between the MLCP and synchronous communications lines. (Note that the MLCP can connect any combination of Synchronous Line Communications-Pacs and Asynchronous Line Communications-Pacs up to a total of four.) Figure D-2 illustrates the DLCP interface.

LINE REGISTERS

The programming interface to the synchronous line adapter is achieved through its line registers. These line registers are illustrated in Figure D-3.

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[1] Throughout this appendix, descriptions are based on a Synchronous Line Communications-Pac/Adapter that services *two* lines. The *single*-line version of the synchronous line adapter is identical except for the number of lines it services.

[2] Each line's speed is governed by the associated data set, or by either the MLCP's fixed-rate clock, or the DLCP clock settable for each line. Details appear under "Data Transfer Clocks," later in this appendix.

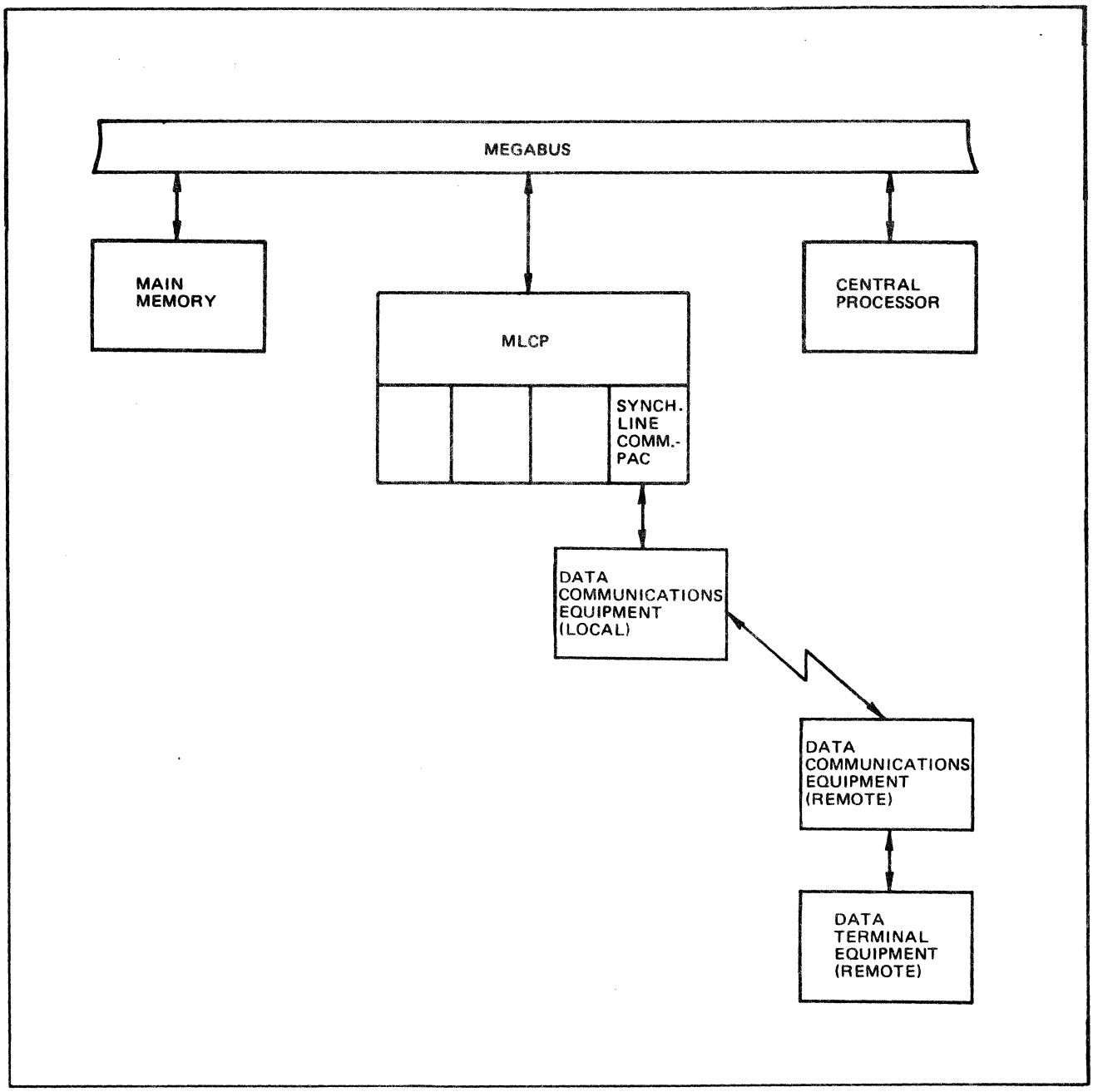


Figure D-1. Interface Provided by Synchronous Line Communications-Pac (MLCP)

Appendix H

Synchronous Broadband HDLC Communications-Pac

INTRODUCTION

The Synchronous Broadband HDLC (high-level data link control) Communications-Pac (Types DCM9112, 9113, and 9121) provides an interface between the MLCP and one broadband synchronous communications line (72,000 bps maximum). The Synchronous Broadband HDLC Communications-Pac provides for the application of the following control procedures (protocols):

- o American National Standard for Advanced Data Communication Control Procedure (ADCCP), Draft 7, BSR X3.66, 14 December 1977.
- o ISO HDLC (Draft No. ISO/TC 97/SC 6N 1339, dated February 1973)
- o Honeywell HDLC procedure

The communications line comprises a receive channel and a transmit channel, and is capable of either full- or half-duplex operation. Operation of the two channels is completely independent except that they share the same modem and a change in data set control signal will affect both channels.

The Synchronous Broadband HDLC Communications-Pac supports the following interfaces:

- o DCM9112 – Bell 303-compatible interface, supporting the following connections:
  Bell System 301B modem or equivalent
  Bell System 303 modem or equivalent
  Direct connect, 303-compatible
- o DCM9113 – CCITT V35 interface supporting the following connections:
  Data communications equipment using V35
  Bell System Digital Data Service (DDS) using Data Service Units at 56kbs
- o DCM9121 – MIL188C, supporting the following connections:
  Modems or equivalent supporting a MIL-STD-188C interface

In addition, the Communications-Pac may be used in direct connect arrangements where the MLCP supplies the clock. The direct connect cable is identified by specifying W18-0001C.

Figure H-1 illustrates the Synchronous Broadband HDLC Communications-Pac's interface position between the MLCP and a synchronous broadband communications line. Note that a single broadband line can be intermixed with other line types on a single MLCP, subject to overall throughput considerations, but one broadband line per MLCP is a limit.

HDLC FRAME STRUCTURE

The HDLC frame structure, illustrated in Figure H-2, eliminates the need for control characters of other protocols (such as bisynchronous) and maximizes the ratio of information (data) to control in bits. It offers field transparency and code independence facilitating the sending of binary information (i.e., the frame structure is bit-oriented). In addition, the HDLC frame structure has the potential for handling very high speed lines to accommodate growth in networking or other data communications applications.

Specifications may change as improvements and modifications are introduced.

The elements of the HDLC procedure supported by the Communications-Pac are zero-bit insertion and deletion, character assembly/disassembly, and the handling of flag, abort, idle and partial byte.

The Cyclic Redundancy Check (CRC) Frame Check Sequence (FCS) is calculated and checked automatically by the Communications-Pac. Extended address field, extended control field, logical control field, and byte size switching are supported.

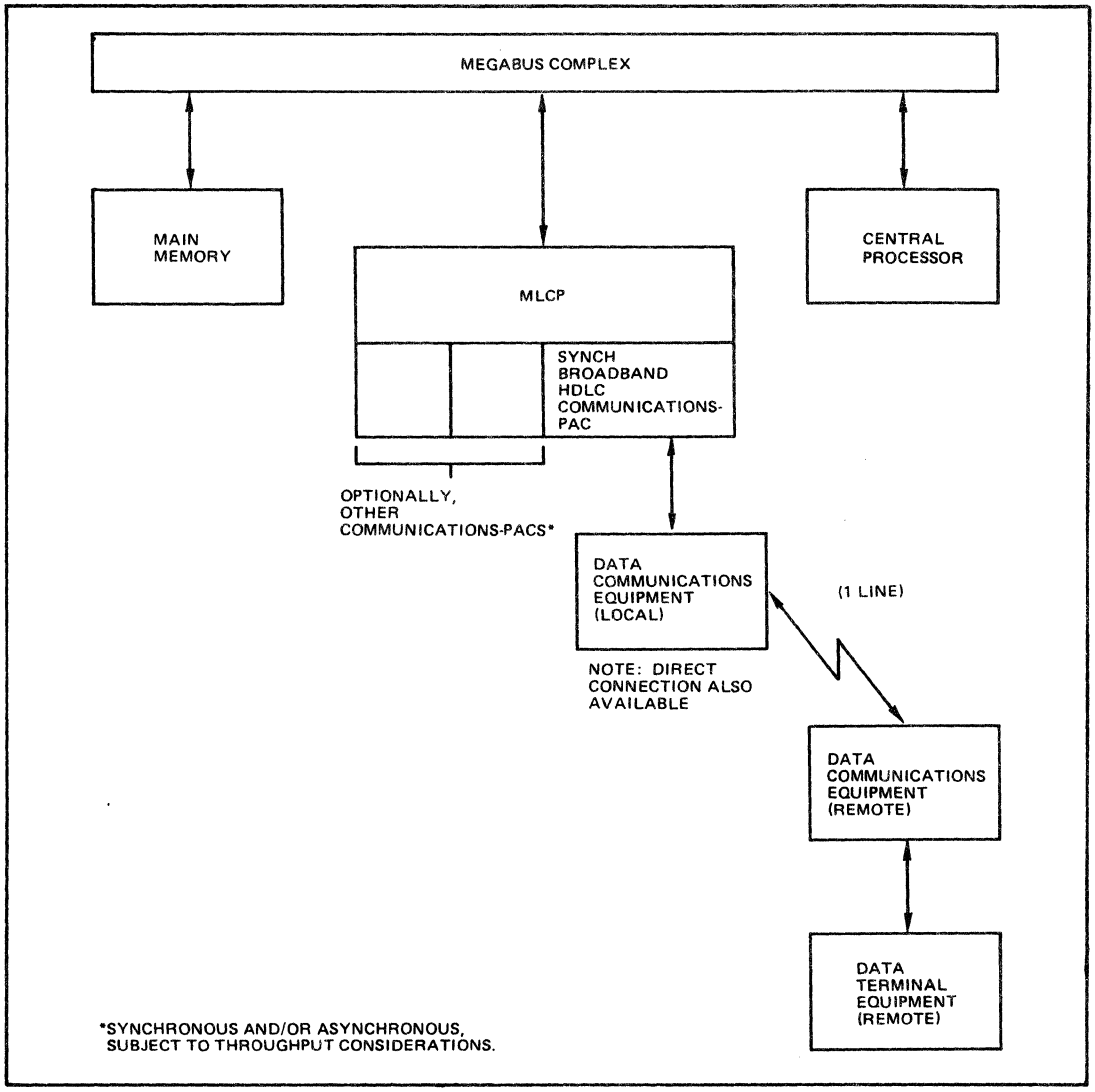


Figure H-1. Interface Provided by Synchronous Broadband HDLC Communications-Pac

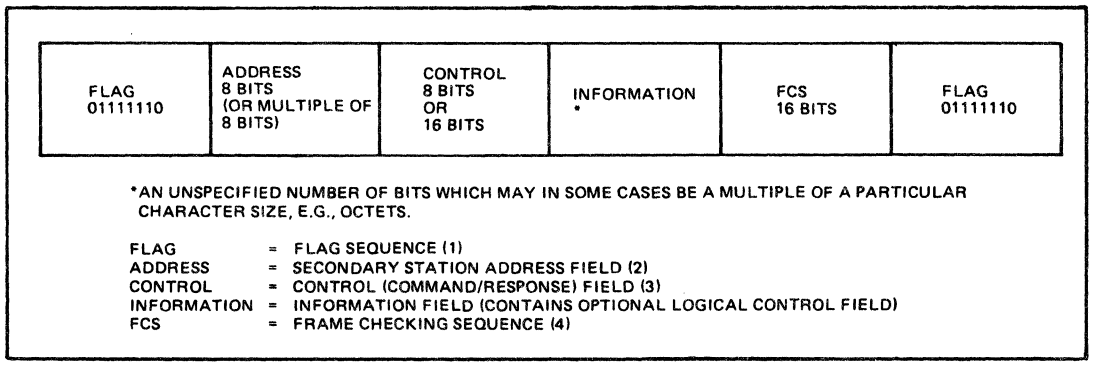


Figure H-2. HDLC Frame

In HDLC, all transmissions are in "frames" and each frame conforms to the structure of Figure H-2. In this section, an eight-bit string is called an "octet." (Frames containing only supervisory control sequences constitute a special case in which the information field is omitted. This is protocol-dependent.) The fields of the frame are defined in the paragraphs that follow.

Flag Sequence

All frames start and end with the flag sequence. This sequence is a zero-bit followed by six one-bits followed by a zero-bit (01111110). All stations attached to the data link continuously hunt, on a bit-by-bit basis, for this sequence. A transmitter must send only complete flag bit sequence; however, the sequence of 01111101111110 at the receiver is two flag sequences. The flag is used for frame synchronization. Flag detection is performed by the Communications-Pac under programmer control.

In order to achieve transparency, the flag sequence is prohibited from occurring in the Address, Control, information and FCS fields via a "zero-bit insertion" procedure performed by the Communications-Pac. (See the paragraph entitled "Transparency" later in this section.)

The flag sequence which closes a frame may also be the opening flag sequence for the next frame. Any number of complete flags may be used between frames.

Address Field

The *address field* contains the link level address of a secondary station or stations. The length of this field is normally one octet.

For extended addressing, this field may optionally contain multiple octets. Field extension is accomplished by the use of the least significant bit of each address field octet as a continuation bit. In this case all octets in the field (except the last) will have a zero in their continuation bit position.

Whether or not extended mode applies is under program control and must be determined by prior agreement between the transmitter and receiver. In the Synchronous Broadband HDLC Communications-Pac, the mode is indicated to the Communications-Pac via a bit in the appropriate configuration register of the Communications-Pac (transmit line register 7 and receive line register 6).

Normally, transmitted address field bytes must be program generated and transferred like data to the MLCP-Communications-Pac for transmission. Similarly, received address field bytes are normally input to the main memory program (MMP) as part of the data block.

Control Field

The *control field* contains a command or response and may contain sequence numbers. The control field is used by the transmitting (primary) station to instruct the addressed secondary station what operation it is to perform. It is also used by the secondary station(s) to respond to the remote primary station(s). The length of the control field is one octet in the case of the basic control field. It is two octets in length in the case of the extended control field.

The first bit of the octet (i.e., the low order bit, bit 7 – first octet if in extended mode) provides information about the format of the remainder of the frame. When a zero, it indicates the frame is in Information Transfer format and byte size of the text field is specified in the "Logical Control field"[1] or the appropriate configuration register of the Communications-Pac. When a one, it indicates the frame is in supervisory format or non-sequenced format and all data for the remainder of the frame is in 8-bit bytes.

The specification as to whether or not extended mode applies is under program control and must be determined by prior agreement between the transmitter and receiver. In the Synchronous Broadband HDLC Communications-Pac, the mode is indicated to the Communications-Pac via a bit in the appropriate configuration register of the Communications-Pac (transmit line register 7 and receive line register 6).

[1] Refer to the paragraph entitled "Information Field," and to the discussion on the Logical Control Field.

Output Control field bytes must be program generated and transferred as data to the MLCP-Communications-Pac for transmission. Similarly, received Control bytes are input to the MMP as part of the data block.

Information Field

The *information field* may be any number and sequence of bits; the data link procedures are completely transparent. Data contained in the Information field is unrestricted with respect to code or grouping of bits.

IMPORTANT: If the optional Logical Control field feature is not used, bits 2 and 7 of receive line register 6 and bits 2 and 7 of transmit line register 7 *must be zero*.

Logical Control Field

A feature has been provided to include a *logical control field* (LCF) as part of every frame containing an Information field. This field consists of at least three octets and is recursively extendable. Field extension is accomplished by use of the most significant bit of each LCF octet as a continuation bit. The last LCF octet has its continuation bit set to a one.

Whether or not a logical control field exists is under program control and must be determined by prior agreement between the transmitter and the receiver. In the Synchronous Broadband HDLC Communications-Pac this mode is indicated to the Communications-Pac via a bit in the Communications-Pac configuration register (transmit line register 7 and receive line register 6). An additional bit indicates whether or not a text control byte is present to specify the byte size of the text field data (see Table H-1).

The LCF consists of a Text Control Byte (TCB), a Frame Type Byte (FTB) and one or more of the following fields which consists of one or more bytes each: Local Routing Field (LRF), Network Control Field (NCF), Stream Control Field (SCF), and Endpoint Control Field (ECF).

The TCB (when present) contains in its low order three bits (bits 5-7) a code which defines the character size used in the Text field, which immediately follows the LCF. The Communications-Pac uses these bits to control the packing/unpacking of the text field bytes. The most significant bit of the TCB is a continuation bit. The remainder of the TCB is not used by the Communications-Pac. Refer to Table H-1, below, for the byte size encoding.

TABLE H-1. TEXT CONTROL BYTE

TCB Bit 5 6 7	Number of Bits/Byte in Text Field
100	4
101	5
110	6
111	7
000	8
011	Native Byte Size – Bit Stream Mode
001	Reserved
010	Reserved

The only LCF bits which have significance to the Communications-Pac are the continuation bit in each byte and the text byte size bits in the TCB as described above.

Output LCF bytes must be program generated and transferred as data to the MLCP-Communications-Pac for transmission. Similarly, received LCF bytes are input to the main frame memory as part of the data block.

Text Field

The optional *text field* follows the LCF. This field may contain any number of text characters (including none at all). The text field ends with the start of the FCS field which occupies the 16 bits prior to the next flag.

None of the data in this field is of significance to the MLCP-Communications-Pac. The Communications-Pac packs/unpacks the number of bits in the bytes transferred between it and main memory when receiving/transmitting, according to the text character size defined in the TCB and/or the appropriate configuration register of the Communications-Pac.

Output text data must be program generated and transferred to the MLCP-Communications-Pac for transmission. When the CCB range is exhausted, the CCP sets an indication in the Communications-Pac which causes it, after transmitting the last data character, to revert to eight-bit byte mode and to transmit the CRC residue (which it has been calculating during transmission of the frame as a 16-bit FCS). It then generates and transmits the closing flag.

Input text data is input to main memory as part of the data block. Recognition of the closing flag by the Communications-Pac causes it to complete the CRC residue calculation using the 16-bit FCS. The completion of the frame is signalled to the CCP. The FCS and closing flag are not transferred to main memory.

Frame Check Sequence

All frames include a 16-bit *frame check sequence* (FCS) just prior to the closing flag for error detection purposes. The Communications-Pac uses algebraic procedure based on a modulo 2 division process using a generation polynomial to automatically generate and check the FCS.

At the transmitter, the initial remainder of the divison is set to all one's. This initial remainder is then modified by division by the generator polynomial. This division is performed on the contents of the Address, Control, and Information fields, excluding zero-bits inserted for transparency. When these fields have completed the division process, the one's complement of the resulting remainder is transmitted (high-order bit first) as the 16-bit FCS.

At the receiver, the initial remainder is preset to all one's, and the same division process takes place on the serial incoming bits. All bits between the opening and closing flag are included, except zero-bits inserted for transparency. In the absence of transmission errors, the final remainder is 1111000010111000 (LSB to MSB) in reading from left to right.

The generation polynominal is that polynomial according to CCITT recommendation V41: $x^{16} + x^{12} + x^{5} + 1$.

The checking polynomial for output (transmit) frames is automatically generated by the Communications-Pac as it transmits the Address, Control and Information fields. When transmission of these fields is complete, the FCS is appended to the end of the frame before the closing flag is transmitted.

Similarly, when receiving a frame, the necessary operations are automatically performed on the incoming data stream. When the ending flag is received, the generated remainder is compared with the correct remainder for an errorless transmission. The result of this comparison is made available to the programmer as part of the interrupt status.

Order of Bit Transmission

The Flag, Address, Control and LCF fields are transmitted least significant bit (LSB) first. The text field is normally transmitted LSB first but when bit stream mode is invoked, it is transmitted MSB first. The FCS is transmitted most significant Bit (MSB) first.

Abort

Abort is the procedure by which a station in the process of sending a frame ends the frame in an unusual manner such that the receiving station will ignore the frame.

On transmit, the Communications-Pac automatically sends an abort of eight ones on underrun. On receive, a sequence of 7 ones is detected as an abort by the Communications-Pac. In both cases, the appropriate status is reported to the CCP by the Communications-Pac. A control bit is also provided so that the CCP may terminate a transmit frame with an abort sequence instead of a flag sequence.

Transparency

HDLC provides transparency for data coded in the information field. The occurrence of the flag sequence within the frame is prevented via a "zero-bit insertion" technique.

The transmitter inserts a zero-bit following five contiguous one-bits anywhere between the beginning and ending flag of a frame. The receiver continuously monitors the received bit stream. Upon receiving a zero-bit followed by five contiguous one-bits, the receiver inspects the following bit. If a zero, the five one-bits are passed and the zero-bit is deleted. If the sixth bit is a one, the receiver inspects the seventh bit. If the seventh bit is a zero, a flag has been received; if a one, an abort sequence has been received.

Interframe Time Fill

The Communications-Pac is capable of sending either flag sequences or continuous ones between frames under control of the CCP.[2]

Intraframe Time Fill

The HDLC protocol does not provide the intraframe time fill. All bytes within a frame are contiguous.

Idle Link State

A string of fifteen (or more) contiguous one-bits indicates the idle link state. On receive, the Communications-Pac reports this condition to the CCP via the receive status word in receive line register 7. On transmit, the Communications-Pac can send this condition under control of the CCP via transmit configuration word 2 in transmit line register 6.

LINE REGISTERS

The programming interface to the Synchronous Broadband HDLC Communications-Pac is achieved through its ten visible line registers. A "One" bit in one of these registers corresponds to a one-bit for a data bit or to ON for a control or status signal at the modem interface. The line register numbers correspond to the line register numbers of the MCLP instruction set.

For the specific use and sequence of loading and reading registers, refer to the flow charts later in this section.

The Communications-Pac and the MLCP exchange parallel data elements on a channel basis through the line register 1 FIFO stacks using Adapter Ready (bit 4 of line register 5) to inform the MLCP of the need to continue FIFO service. The Communications-Pac converts parallel data to bit serial data for transmission and converts bit serial data to parallel data on receive. Each channel of the Communications-Pac contains a serial buffer of at least three bytes for inserting/deleting the FCS and flag bytes which are normally not present in the FIFO stacks.

The channel request interrupt (CRI) generated by the Communications-Pac for each channel causes the execution of the channel control program (CCP) to begin. The CCP then performs transfers of status, control, and/or data bytes between the Communications-Pac and the MLCP. The Adapter Ready bit in line register 5 may be used (via the BART and BARF instructions, if desired) to allow the CCP to completely service the FIFO needs (i.e., to fill the transmit FIFO or empty the receive FIFO) without the necessity to revert to the more time-consuming WAIT procedure.

[2] The normal mode is the sending of flag sequences.

Refer to Figure H-3 for a diagram of the Synchronous Broadband HDLC Communications-Pac line registers.

The Receive and Transmit registers described separately are receive line registers 1, 6, and 7 and transmit line registers 1, 6, and 7. Registers in common are Line Registers 0, 2, 3 and 5. First, the format of the line registers is presented, followed by definitions of the fields of the register. These definitions are accompanied by text and/or notes clarifying or explaining key programming points. Tables are included where appropriate to provide a visual "picture" of the register operation.

The configuration registers (transmit line register 7 and receive line register 6) have variable formats depending upon the point in processing. These formats are uniquely identified for later reference for use in the flow charts (Figures H-18 and H-20). An example is R6-1, referring to the receive line register 6 initialization format, or T7-2, referring to the transmit line register 7 start-of-frame format. A list of these formats can be referenced in Table H-6.

NOTE TO READERS: When reading this material for the first time, concentrate on gaining an understanding of the register general functions. Do not attempt to memorize the programming details. Then, reread the discussion for detail.

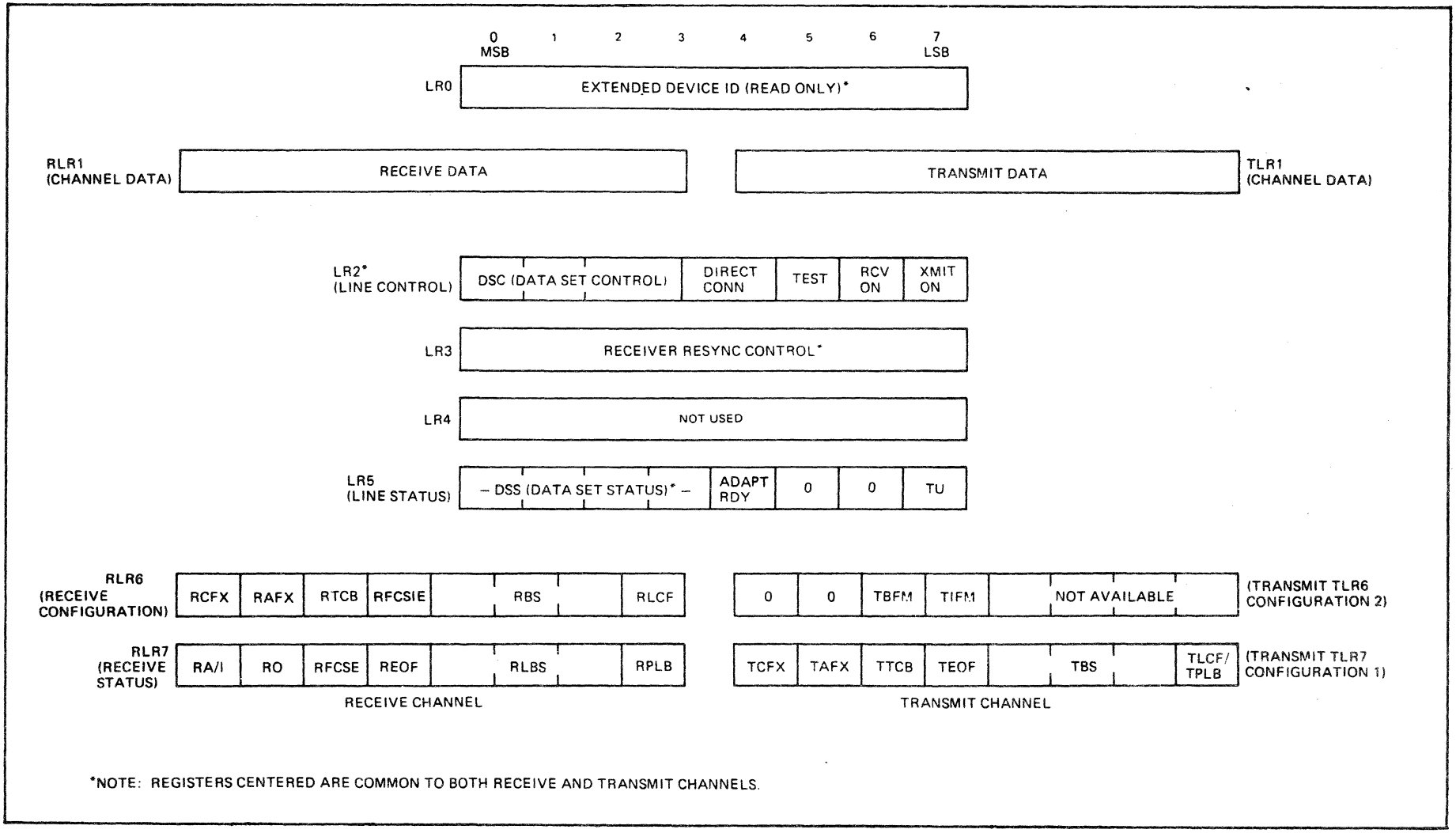


Figure H-3. Synchronous Broadband HDLC Communications-Pac Line Registers

Shared Line Registers

Line Register Zero-Extended Device Identification Number

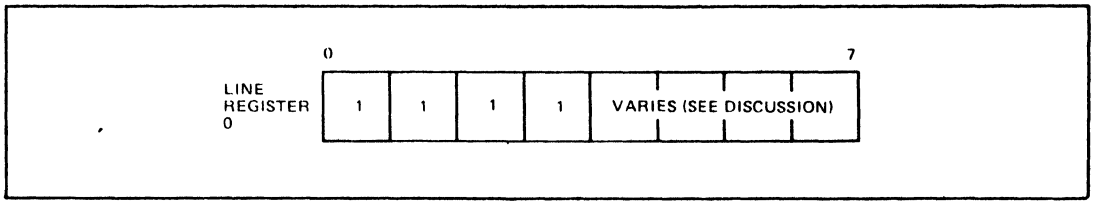


Figure H-4. Line Register Zero

Line register zero is common to the transmit and receive channels. It provides a device identification number when read: $F6_{16}$ for the DCM9112 (Bell 303-compatible interface) and $F7_{16}$ for the DCM9113 (CCITT V35 interface) and $F8_{16}$ for the DCM9121 (MIL188C).

Line register zero may be read from either the transmit or receive channel via the IN 0 instruction, or from the main memory program via the IO (Input Extended Identification Number) instruction.

Line register zero cannot be changed by the MLCP – it is a read-only register.

Line Register 2 – Line Control

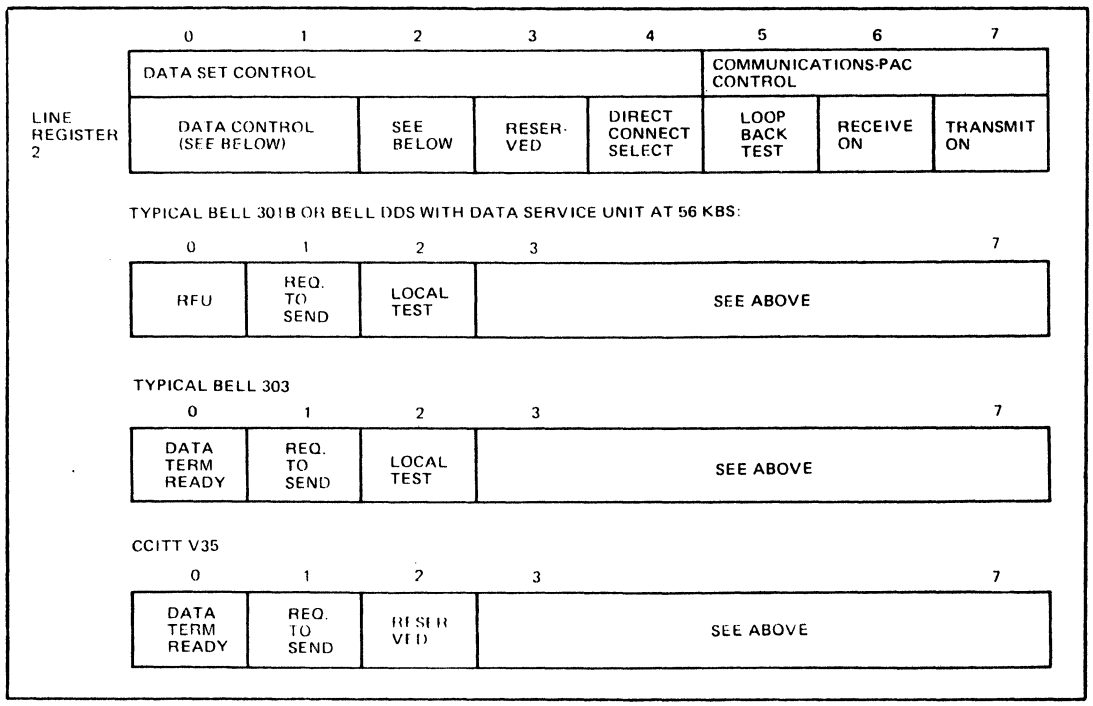


Figure H-5. Line Register 2

This register may be accessed on both channels of the Communications-Pac via the OUT 2 instruction. It may only be written; if read, will cause unspecified results. Line register 2 is loaded by the CCP with information obtained from LCT byte 20. The significance of each bit position is described under "LCT Byte 20 – Data Set and Communications-Pac Control" in Section 5. Bit definitions are as follows:

- o Data Terminal Ready – Data Terminal Ready signal to the modem.
  0 = Off
  1 = On

- o Request to Send – Request to Send signal to modem.
  0 = Off
  1 = On
  This bit must be on to enable transmit data transfer interrupts by the Communications-Pac.
- o Local Test (bit 2) – used only for Bell 303-compatible interface (DCM9112).
  0 = Off
  1 = On
  Refer to appropriate DCE literature for the use of these signals. This bit must be zero for direct connect.
- o Bit 4 – reserved. *This bit must be zero for direct connect.*
- o Direct Connect – When this bit (5) is set, the Communications-Pac takes its clock source from the MLCP to which it connects and provides a clock to the remote data terminal equipment.
  0 = Normal mode (DCE clock)
  1 = Direct Connect mode (MLCP clock)
- o Test – When this bit is on, the transmit data is looped back to the received data instead of being connected to the modem. Communications-Pac initialize sets this bit to one as distinguished from all other line register bits which are set to 0. Initialize is fully described later in this section. In the test mode condition, the transmit data line to the modem is marking (all ones).
  0 = No test
  1 = Test
  In normal mode, the transmit and receive clocks are provided by the DCE (or direct connect mode clock), the receive data is provided by the DCE, and adapter generated or MLCP provided transmit data is sent to the DCE.
  In test mode, the transmit and receive clocks are taken from the MLCP, the receive data is taken from Communications-Pac-generated or MLCP-provided transmit data and the transmit data to the DCE is held in the marking (abort) state. Refer to the paragraph entitled "Data Transfer Clocks" later in this section.
- o Receive(r) On – Receive(r) On enables the received Communications-Pac channel to generate channel request interrupts for each received data character. When the receiver is off, data within the adapter is not lost (unless overrun occurs), but receive channel request interrupts are not generated.
  0 = Receive not enabled (CRIs inhibited) CRI = Channel Request Interrupt
  1 = Receive enabled (CRIs enabled)
- o Transmit(ter) On – Transmit(ter) On enables the transmit Communications-Pac channel to generate channel request interrupts for each required transmit data character.
  0 = Transmit not enabled (CRIs inhibited)
  1 = Transmit enabled (CRIs enabled)

Line Register 3 – Receive Resynchronization

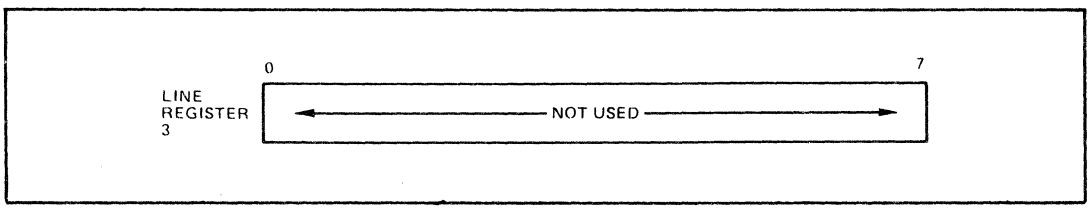


Figure H-6. Line Register 3

An OUT 3 instruction initializes the receiver, causing it to discard all previous data and status information and to search for an idle link state condition or start of frame flag. The actual register bits are not used. A resynchronization command may be issued from either channel via the OUT 3 instruction.

Line Register 4 – Not Used

Line Register 5 – Data Communications Equipment (DCE) Status

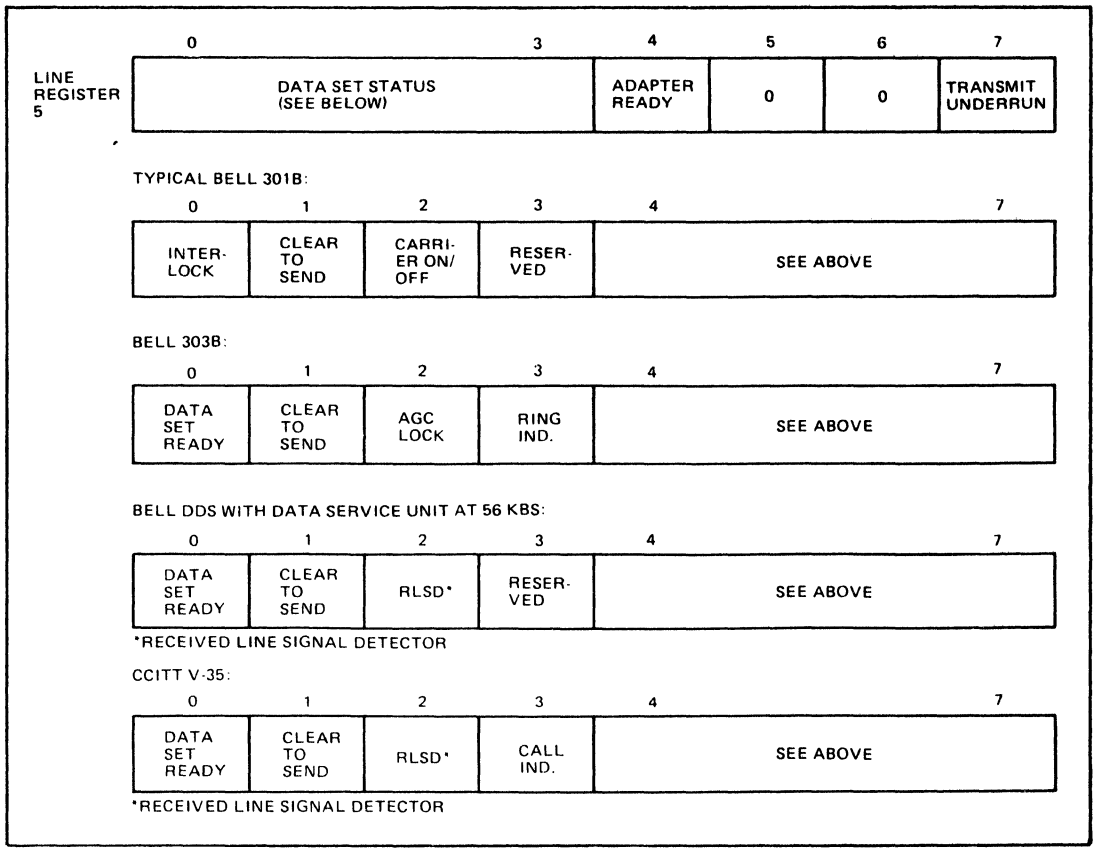


Figure H-7. Line Register 5

Status is made available to the CCP via line register 5 which may be read as appropriate. The four bits which represent transmit and receive status, bits 4, 5, 6 and 7 may be set in combination or individually.

Line register 5 is shared by the receive channel and the transmit channel of the same line. Line register 5 can be read by the main memory program through use of an IO (Input Data Set Status) instruction.

Bit definitions are as follows:

- o Data Set Ready – indicates the Data Set Ready signal from the modem
  0 = Off
  1 = On
- o Interlock – indicates whether the data set is powered up and not in a test condition
  0 = Off. Data set is not in a condition to transmit or receive data.
  1 = On. Power is on and data set is not in a test condition.
- o Clear to Send – indicates the Clear to Send signal
  0 = Off
  1 = On
  Clear to Send must be On for the adapter to generate data transfer channel request interrupts.
- o Carrier On – indicates the state of Carrier On (or equivalent signal) from the modem
  0 = Off
  1 = On

NOTE: Consult the appropriate DCE literature for the actual use of these signals.

- o ACG Lock – indicates whether signals on the receive data lead are reliable
  0 = Off – unreliable
  1 = On – reliable

- o Adapter Ready – transmit and receive Adapter Ready status is indicated as follows:
  0 = Adapter Ready false
  1 = Adapter Ready true
  Adapter Ready indicates transmit status when line register 5 is read from a transmit CCP and receive status when read from a receive CCP. For receive, Adapter Ready is true whenever there is data and/or status available in the receive FIFO memory. For transmit, Adapter Ready is true under the following conditions: RTS = 1, CTS = 1, TEOF = 0, and the transmit FIFO memory is not full.
  Where:
  RTS = Request to Send (Bit 1 of line register 2)
  CTS = Clear to Send (Bit 1 of line register 5)
  TEOF = Transmit End of Frame (Bit 3 of transmit line register 7)

- o Transmit Underrun – transmit end of frame status is indicated by this bit as follows:
  0 = No underrun
  1 = Underrun
  This bit is valid only for the first transmit interrupt after the last byte of each frame has been transferred to the Communications-Pac. Note that the bit is not automatically reset to zero for receive channel interrupts.

Transmit Line Registers

Transmit Line Register 1 – Output Data Transmit Channel

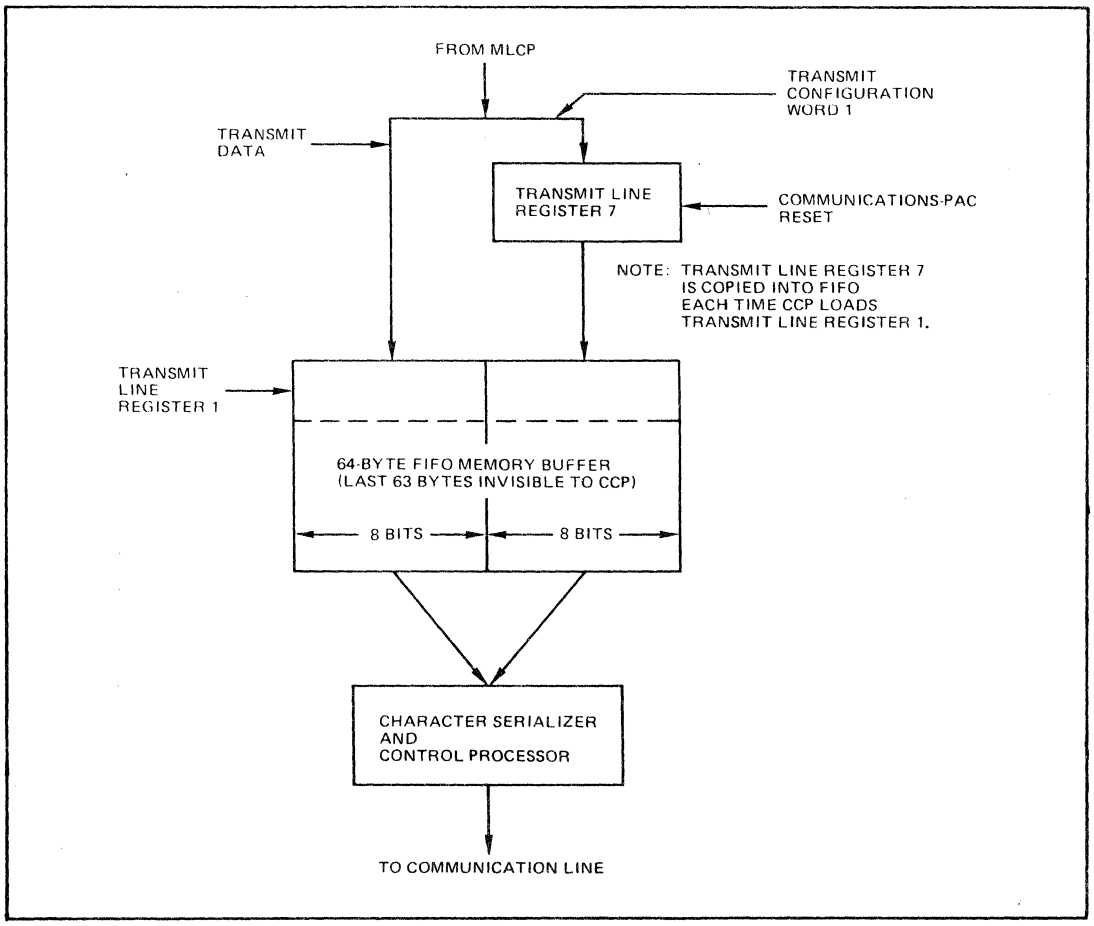


Figure H-8. Transmit Line Registers 1 and 7 and FIFO Memory

Transmit Line Register 1, Output Data, is constructed as the input to one-half of a FIFO stack (see Figure H-8). The stack consists of 64 locations of 16 bits each; 8 of these bits are transmit data and are written into by the MLCP through transmit line register 1; the remaining 8 bits are transmit configuration information and are written into by the MLCP through transmit line register 7. The 64-byte buffer is a temporary storage facility that is automatically filled by the Communications-Pac hardware as the CCP transfers each data character to line register 1. This buffer, with the exception of the 8-bit transmit line registers 1 and 7, is not visible to the CCP. It is the top (input) location of the stack which is written into by the MLCP. The Communications-Pac reads out the stack at the bottom (output) location as characters are transmitted to the line and this advances the stack (both line register 1 and line register 7 portions). The act of writing into line register 1 enters both those contents and the line register 7 information into the stack at the same time. During the frame, it is not necessary to perform a write into line register 7 for each write into line register 1, but only when a change to line register 7 is required (such as at end of frame). However, between frames, when TEOF is set to inhibit channel request interrupts, the Communications-Pac resets line register 7 to cause a channel request interrupt. Line register 7 must therefore normally be loaded by the CCP at each channel request interrupt (see also the transmit line register 7 discussion later in this section).

This register may be written by either the SEND or OUTPUT (LR1) instruction. Since CRC/FCS calculation is performed by Communications-Pac, the OUTPUT instruction is recommended because of its faster execution time.

Whether or not the buffer is full can be tested by the BART and BARF instructions. (Refer to the description of line register 5 bit 4 later in this section.) The buffer prevents underrun by allowing the accumulation of data characters to be transmitted.

The receive channel can prevent the servicing by the MLCP of the receive channel's companion transmit channel (because receive is a higher priority channel than transmit), causing a potential underrun situation. A possible solution is shown in the system flowchart, Figure H-18, under the routine entitled "T-SOF," buffer fill mode, which provides a method for preloading the transmit FIFO before starting frame transmission.

The length of each character in transmit line register 1 may be 8 bits or less. If the length is fewer than 8 bits, the data character is normally right-justified in line register 1. In this mode, bit 7 is the first bit transmitted, and the extra left-hand bits will not be transmitted. When operating in bit stream mode, bit zero is the first bit transmitted, and if the byte size is less than 8, the extra right-hand bits will not be transmitted. For specific detail, refer to the portion of this section entitled "Transmit and Receive Line Register Formats."

If parity is to be generated, the parity bit (the leftmost bit of the defined character length) must be specified as a zero (when the data character is transferred to line register 1); the MLCP generates the correct parity during the transfer to line register 1. The parity bit is inserted in the leftmost bits of the defined character length and is included in transmissions.

Transmit Line Register 6 — Transmit Configuration Word 2

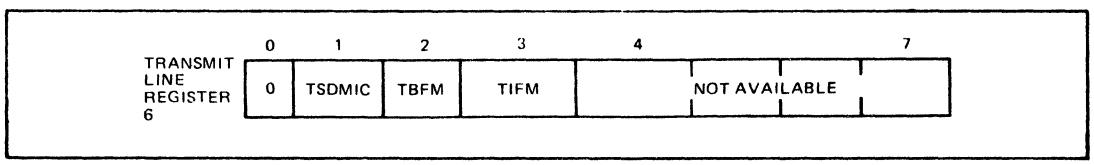


Figure H-9. Transmit Line Register 6, Configuration Word 2

The purpose of this line register is to provide control of the bit stream that is transmitted between frames (i.e., flags or marking line), and to provide control for preloading the transmit FIFO buffer at the start of frame.

Bit definitions are as follows:

- o TSDMIC – Transmit Slow-Down Mode Interrupt Control
  This bit must be set to zero.
  0 = Normal Mode (do not generate special interrupt)
- o TBFM – Transmit Buffer Fill Mode
  0 = May begin transmission of frame
  1 = Do not start transmission of frame
  When this bit is a one, the transmitter does not begin transmission of a frame (to the DCE/terminal interface); however, it will proceed to fill its buffer (the transmit FIFO stack) and will transmit interframe fill. This bit does not affect transmission of any frame which has already started transmission. If this bit is a zero, the transmitter begins transmission of a frame as soon as at least one character of the frame has been loaded into the FIFO stack. To prevent underrun, this bit is set to allow the transmit buffer to fill. Refer to the "T-SOF" and "T-INTRA" portions of Figure H-18.
- o TIFM – Transmit Interframe Fill Mode
  0 = Mark line (all ones) between frames (idle link state)
  1 = Send flag sequences between frames

Transmit Line Register 7 – Transmit Configuration Word 1

The format of this line register varies depending upon at what point in transmission (e.g., interframe, beginning of frame, etc.) processing is occurring. These formats and the meanings of the bit positions in the register are defined below.

Transmit Line Register 7 is logically constructed as the input to one-half of a FIFO stack (see Figure H-8). The stack consists of 64 locations of 16 bits each; eight of these bits are transmit data and are written by the MLCP through line register 1, the remaining eight bits are configuration word 1 information and are written by the MLCP through line register 7. It is the top (input) location of the stack which is written into by the MLCP. The act of writing into line register 7 does not directly cause anything to enter the stack but simply provides information to be copied in on succeeding line register 1 entries when they are made. It is the act of writing line register 1 which causes an entry of both line register 1 and line register 7 information to be made into the stack. The Communications-Pac reads out the stack at the bottom (output) location as characters are needed for transmission to the line; this action causes the stack to advance. The bits of line register 7 have different meanings depending upon whether in initialization, start of frame transmission, at end of frame or between frames.

A special comment is in order regarding the *transmit end of frame* (TEOF) bit in this line register. At end of frame, and between frames, it is the set condition of this bit (i.e., bit =1) that inhibits the Communications-Pac from generating channel request interrupts. At the appropriate time, the Communications-Pac causes a channel request interrupt by resetting the entire line register (which includes TEOF). At end of frame, this action occurs when the Communications-Pac is ready to report the transmit end of frame status; between frames it occurs at byte (flag or abort) boundaries. In response to these interrupts, the CCP must (unless it is ready to start a new frame immediately) respond by executing an OUT 7 with TEOF set, in order to prevent an immediate additional interrupt. Refer to "T-INTER" in Figure H-18.

Interframe Format (Format T7-1)

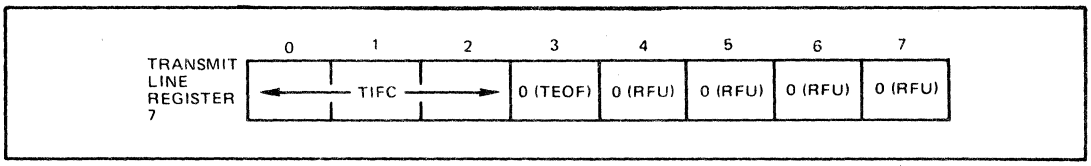


Figure H-10. Transmit Line Register 7, Interframe Format

The interframe format is used to control the channel request interrupt rate when idling between frames.

Bit definitions are as follows:

- o TIFC – Transmit Interframe Fill Count
  These bits are a binary count, divided by 2, of the number of interframe fill sequences to be transmitted between transmit channel request interrupts. For example, a TIFC value of 011 specifies 3 x 2 = 6 eight-bit fill sequences (flags or aborts (8 ones) between interrupts).
- o TEOF – Transmit End Of Frame
  1 = Indicates the end of frame format of line register 7 when it follows the start of frame format (and indicates the last byte of frame is in line register 1). Otherwise indicates interframe format of line register 7.

  The value of this bit must be a one for interframe format.

Bits 4 through 7 are reserved for future use and must be set to zero.

Start-of-Frame Format (Format T7-2)

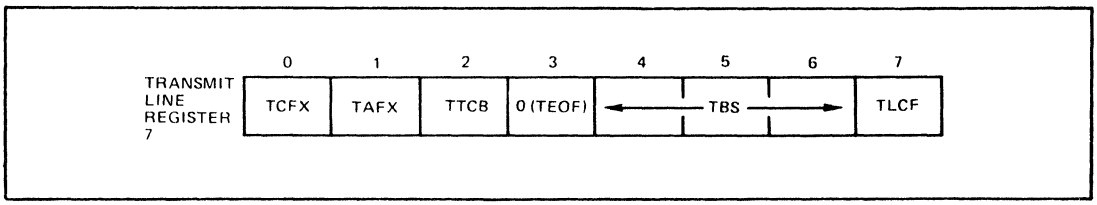


Figure H-11. Transmit Line Register 7, Start-of-Frame Format

The start-of-frame format is used at the start of the frame to specify the entire format of the coming frame. Refer to "T-SOF" in Figure H-18.

Bit definitions are as follows:

- o TCFX – Transmit Control Field Extension
  0 = Control field of frame comprises one octet
  1 = Control field of frame comprises two octets (extended control field format)
- o TAFX – Transmit Address Field Extension
  0 = Address field of frame comprises one octet
  1 = Address field of frame is recursively extendable (extended address field format)
- o TTCB – Transmit Text Control Byte
  0 = Frame does not contain a text control byte
  1 = Frame contains a text control byte

  If the Logical Control Field (LCF) is *not* present in the application the value of this bit must be zero for all frames.
- o TEOF – Transmit End Of Frame
  0 = Indicates the start of frame format of line register 7.
  The value of this bit must be zero for start-of-frame format.
- o TBS – Transmit Byte Size
  The number of bits per byte for the text field portion of the frame is sometimes determined by TBS as shown in the table below. (For additional transmit byte size control information, refer to the portion of this section entitled "Byte Size Control.") This table does *not* apply for the last byte of the frame. Note that a TBS value of 011 indicates bit stream mode and overrides the setting of either TTCB or TLCF.

TBS	Text Field Byte Size
000	5
001	RFU (8)
010	6
011	Bit Stream Mode (8)
100	7
101	RFU (8)
110	8
111	4

NOTE: A TBS value of 011 indicates bit stream mode and overrides the setting of either TTCB or TLCF. Byte size is 8 in MLCP mode, and 6 in HMLC mode.

o TLCF – Transmit Logical Control Field
0 = Frame does not contain a logical control field.
1 = Frame contains a logical control field. Note that if a text control byte is specified, and if its continuation bit is a one, then the text field immediately follows the TCB. This is not an expected frame format, however.

End-Of-Frame Format (Format T7-3)

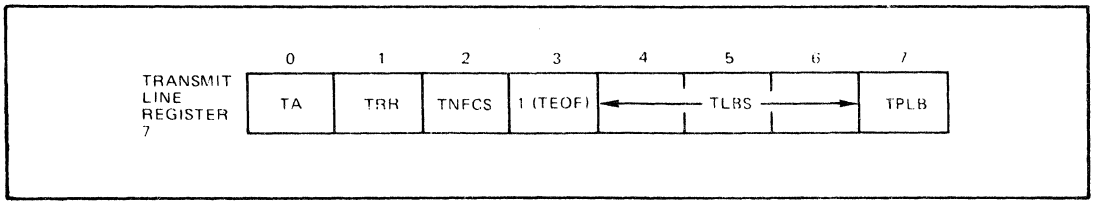


Figure H-12. Transmit Line Register 7, End-of-Frame Format

The end-of-frame format is used to notify the Communications-Pac that the last byte of the frame is in the FIFO and to provide information about the size of that byte, and how the frame should be terminated. See "T-EOF" in Figure H-18.

Bit definitions are as follows:

o TA – Transmit Abort
0 = End frame with Flag sequence
1 = End frame with Abort sequence (the last data byte and FCS are not transmitted)
o TRR – Transmit Resynchronization Receiver
0 = Do not resynchronize receiver
1 = Issue resynchronization command to receive logic (at end of frame)
o TNFCS – Transmit No FCS
0 = End frame in normal manner with FCS before closing flag (applies only if TA = 0)
1 = Do not insert FCS between last byte and closing flag (applies only if TA = 0)

NOTE: This is used either for test purposes or if the user has generated a different checking sequence and has loaded it into the transmit FIFO as part of the data stream.

o TEOF – Transmit End Of Frame
1 = Indicates the end of frame format of line register 7 when follows the start of frame format (and indicates the last byte of frame is in line register 1). Otherwise indicates interframe format of line register 7.

The value of this bit must be a one for the end-of-frame format.

- o TLBS – Transmit Last Byte Size
  The number of bits in the last byte of the frame, when operating in MLCP mode, is sometimes determined by TLBS as shown in the table below. (For additional transmit byte size control information, refer to the portion of this section entitled "Byte Size Control.")

	Last Byte Size	
TLBS	TPLB = 0	TPLB = 1
000	5	5
001	RFU (8)	1
010	6	6
011	RFU (8)	2
100	7	7
101	RFU (8)	3
110	8	8
111	4	4

TPLB = Transmit Partial Last Byte. See bit description that follows.

- o TPLB – Transmit Partial Last Byte
  0 = Last byte of frame is a full byte
  1 = Last byte of frame is a partial byte

Initialization Format (Format T7-4)

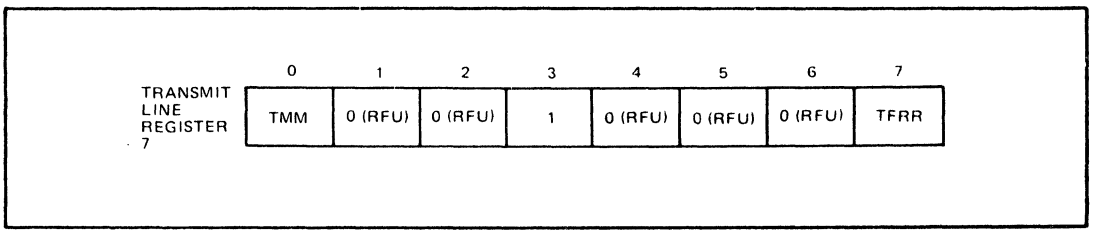


Figure H-13. Transmit Line Register 7, Initialization Format

The initialization format applies only directly after a master clear has been issued to the Communications-Pac. This format provides initialization information for the transmitter as described by the bit definitions below. For Figure H-18 references, see "T-START," "T-F/W REV," "T-START 3," and "T-START 4."
Bit definitions are as follows.

- o TMM – Transmit Major Mode
  0 = The Communications-Pac is attached to an MLCP. This bit must be zero.
- o Bit 3 must be a one; bits 2, 4, 5 and 6 are reserved for future use and must be reset to zero.
- o TFRR – Transmit Firmware Revision Report
  0 = Do not report transmit firmware revision level
  1 = Report transmit firmware revision level

Receive Line Registers

Receive Line Register 1 – Input Data Receive Channel

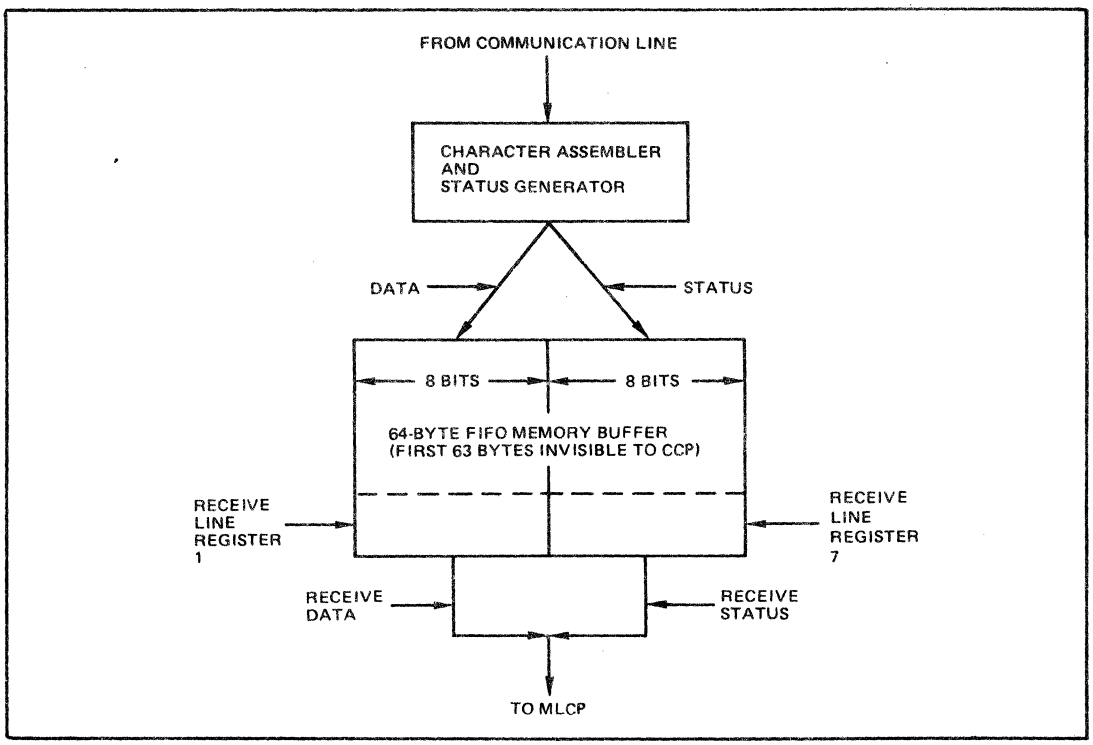


Figure H-14. Receive Line Registers 1 and 7 and FIFO Memory

Receive Line Register 1, Input Data, is constructed as the output of one-half of a FIFO stack (see Figure H-14). The stack consists of 64 locations of 16 bits each; 8 of these bits are receive data and are read by the MLCP through receive line register 1; the remaining 8 bits are receive status information and are read by the MLCP through receive line register 7. The 64-byte buffer is a temporary storage facility that is automatically filled by the Communications-Pac hardware as data is received over the line. This buffer, with the exception of the 8-bit receive line registers 1 and 7, is not visible to the CCP. It is the bottom (output) location of the stack which is read by the MLCP. The act of reading line register 1 advances the stack (both line register 1 and line register 7 portions); thus a given data byte can be read only once by the MLCP. The Communications-Pac loads the stack at the top (input) location with data and channel status information as characters are received from the line. This register can only be read by the MLCP (an attempt to write it will cause unspecified results).

This register may be read by either the RECV or INPUT (LR1) instruction. Since CRC/FCS calculation is performed by the Communications-Pac, the INPUT instruction is recommended because of its faster execution time.

Whether or not the buffer is empty can be tested by the BART and BARF instructions. (Refer to the description of line register 5 bit 4 later in this section.) The buffer prevents overrun when other channels are active; it is the responsibility of the programmer to ensure that the accumulated data characters are accepted by the CCP.

The length of each data character in line register 1 may be eight bits or less. If the length is fewer than eight bits, the data character is normally right-justified and the leftmost bits are zero-filled. In this mode, bit 7 is the first bit received and if the byte size is less than eight, the data will be right-justified with unused left-hand bits being zeros. When operating in bit-stream mode, bit 0 is the first bit received, and if the byte size is less than eight, the data will be left-justified with unused right-hand bits being zeros. Refer to the portion of this section entitled "Transmit and Receive Data Formats."

Receive Line Register 6 – Receive Configuration

Receive Line Register 6 is a configuration register whose format depends on whether an initialization or the receipt of an actual frame is taking place.

Initialization Format (Format R6-1)

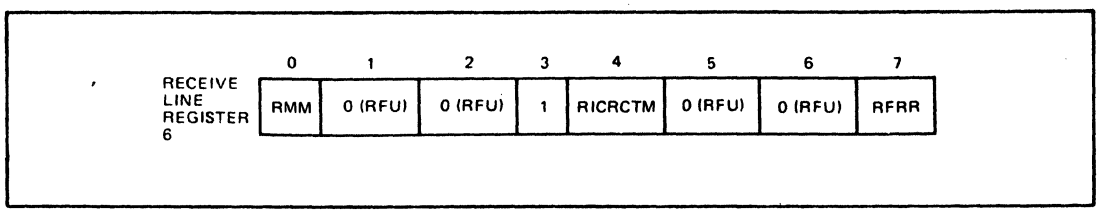


Figure H-15. Receive Line Register 6, Initialization Format

The initialization format applies only directly after a master clear to the Communications-Pac. It provides initialization information for the receiver as described by the bit definitions below. Refer to the system flow chart, Figure H-20 at "R-START," "R-F/W REV," "R-START 3" and "R-START 4" for examples of the use of the initialization format.

Bit definitions are as follows:

- o RMM – Receive Major Mode
  0 = MLCP mode
  This bit must be zero.
- o RICRCTM – Receive Input CRC Test Mode
  0 = Normal mode. FCS and CRC not transferred to MLCP.
  1 = Test mode. Received FCS and calculated CRC remainder are transferred to MLCP.
  This bit is normally set only for test and verification or maintenance use.
- o Bit 3
  Bit 3 must be set to 1 to guarantee a non-zero value of line register 6 after it has been initially set up.

  IMPORTANT: Since the Communications-Pac will interpret any nonzero value of this register as the initialization format, no CCP should load any nonzero value into this register (refer to Note 2 of Figure H-20).

- o RFRR – Receive Firmware Revision Report
  0 = Do not report receive firmware revision level
  1 = Report receive firmware revision level

Frame Format (Format R6-2)

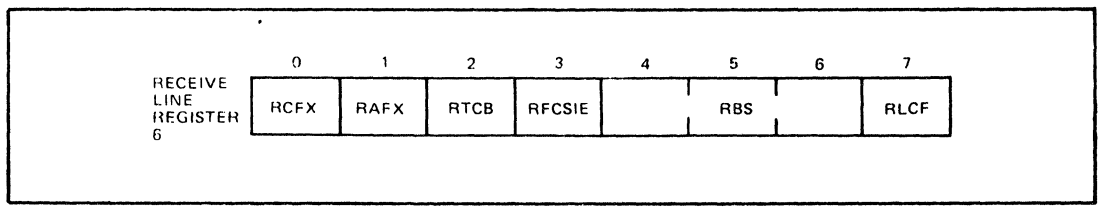


Figure H-16. Receive Line Register 6, Frame Format

The purpose of the frame format is to specify the format of the frame being received. This format (called for convenience R6-2) applies at all times other than when the initialization format is used (see previous discussion). An example of when the R6-2 format is used may be found at "R-RESYNC" in Figure H-20.

Bit definitions are as follows:

- o RCFX – Receive Control Field Extension
  0 = Control field of frame comprises one octet
  1 = Control field of frame comprises two octets
- o RAFX – Receive Address Field Extension
  0 = Address field of frame comprises one octet (basic address format)
  1 = Address field of frame is recursively extendable (extended address format)
- o RTCB – Receive Text Control Byte
  0 = Frame does not contain a text control byte
  1 = Frame contains a text control byte
- o RFCSIE – Receive Frame Check Sequence Input Enable
  0 = Received FCS is checked but not transferred to MLCP
  1 = Received FCS is not checked but instead is transferred to MLCP

NOTE: This is used either for test purposes or if the user is testing the check sequence himself, in which case the check sequence has been loaded into the receive FIFO as part of the data stream.

- o RBS – Receive Byte Size

  The number of bits per byte for the text field portion of the frame is sometimes determined by RBS as shown in the table below. For additional byte size control information, refer to the portion of this section entitled "Byte Size Control." Note that an RBS value of 011 indicates bit stream mode and overrides the setting of either RTCB or RLCF.

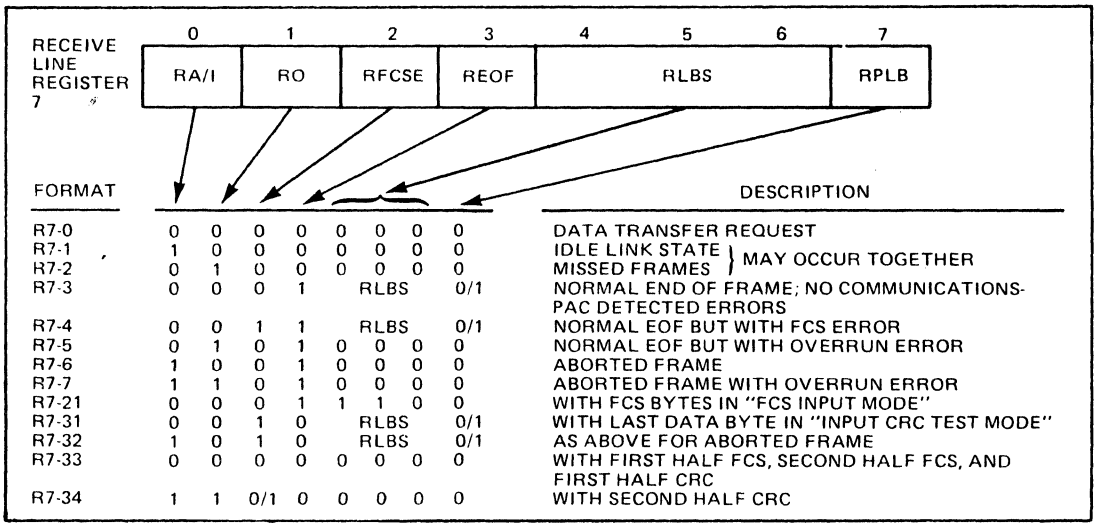
RBS	Text Field Byte Size
000	5
001	RFU (8)
010	6
011	Bit Stream Mode (8)
100	7
101	RFU (8)
110	8
111	4

- o RLCF – Receive Logical Control Field
  0 = Frame does not contain a logical control field
  1 = Frame contains a logical control field. Note that if a text control byte is specified and if its continuation bit is a 1, then the text field follows the TCB immediately. This is not an expected frame format, however.

Receive Line Register 7 – Receive Status

Receive Line Register 7 is constructed as the output of one-half of a FIFO stack. The stack consists of 64 locations of 16 bits each; 8 of these bits are dated and are read by the MLCP through line register 1; the remaining 8 bits are channel status information and are read by the MLCP through line register 7. It is the top (output) location of the stack which is read by the MLCP. The act of reading line register 7 does not advance the stack; a given channel status byte could thus be read more than once if desired. The act of reading line register 1 does advance the stack (both the line register 1 and line register 7 portions). The Communications-Pac loads the stack at the bottom (input) location with data and channel status information as characters are received from the line.

Figure H-17 shows diagrammatically the layout of the register and the values of each bit position for the various receive conditions. Descriptions of the bit positions are found following the figure.



FORMAT									DESCRIPTION
R7-0	0	0	0	0	0	0	0	0	DATA TRANSFER REQUEST
R7-1	1	0	0	0	0	0	0	0	IDLE LINK STATE } MAY OCCUR TOGETHER
R7-2	0	1	0	0	0	0	0	0	MISSED FRAMES } MAY OCCUR TOGETHER
R7-3	0	0	0	1	RLBS			0/1	NORMAL END OF FRAME; NO COMMUNICATIONS-PAC DETECTED ERRORS
R7-4	0	0	1	1	RLBS			0/1	NORMAL EOF BUT WITH FCS ERROR
R7-5	0	1	0	1	0	0	0	0	NORMAL EOF BUT WITH OVERRUN ERROR
R7-6	1	0	0	1	0	0	0	0	ABORTED FRAME
R7-7	1	1	0	1	0	0	0	0	ABORTED FRAME WITH OVERRUN ERROR
R7-21	0	0	0	1	1	1	0	0	WITH FCS BYTES IN "FCS INPUT MODE"
R7-31	0	0	1	0	RLBS			0/1	WITH LAST DATA BYTE IN "INPUT CRC TEST MODE"
R7-32	1	0	1	0	RLBS			0/1	AS ABOVE FOR ABORTED FRAME
R7-33	0	0	0	0	0	0	0	0	WITH FIRST HALF FCS, SECOND HALF FCS, AND FIRST HALF CRC
R7-34	1	1	0/1	0	0	0	0	0	WITH SECOND HALF CRC

Figure H-17. Receive Line Register 7, Receive Status

Bit definitions are as follows.

- o RA/I – Receive Abort/Idle Link State
  0 = No abort or idle link state
  1 = As follows: 1. If this bit = 1 and REOF = 1, indicates that the frame was terminated with an abort sequence of seven or more ones.
  2. If this bit = 1 and REOF = 0, indicates that fifteen or more ones have been received which specifies that the input line is in an idle link state.
- o RO – Receive Overrun
  0 = No overrun
  1 = Overrun
  Indicates that the Communications-Pac was not serviced fast enough and one or more characters or frames in the Communications-Pac data path have been over-written or lost.
- o RFCSE – Receive Frame Check Sequence Error
  0 = No FCS error
  1 = FCS error
  Indicates that the frame was received in error (CRC check by Communications-Pac failed). This bit is normally zero and has a valid meaning only when REOF is set (see below).
- o REOF – Receive End of Frame
  0 = No end-of-frame condition
  1 = End-of-frame. Indicates that the frame was terminated. The associated data byte in line register 1 is the last byte of the frame.
- o RLBS – Receive Last Byte Size
  These bits specify the number of valid bits in the last text byte of the frame for both full and partial last bytes. Normally, these bits are zeros and may take on some other value only when REOF = 1. When valid, these bits are as shown below:

RLBS			Number of bits in last byte
0	0	0	5
0	0	1	1
0	1	0	6
0	1	1	2
1	0	0	7
1	0	1	3
1	1	0	8
1	1	1	4

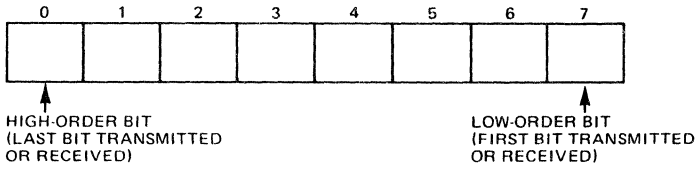
o RPLB – Receive Partial Last Byte
  0 = Last byte received is a full byte
  1 = Last byte received is a partial byte

NOTE: A status word of "FD" (hexadecimal) is provided in Receive Line Register 7 at initialization with the firmware revision level if the firmware revision level is ready by the IN1 or RECV NO CRC instruction.

TRANSMIT AND RECEIVE DATA FORMATS

Formats for data being transferred via line register 1 (either the transmit or the receive register) are presented below. For applications using the Logical Control Field (LCF), note the distinction between the LCF and the "text" field. Otherwise the 'information' field use is described as shown. For mnemonics, refer to Table H-6.

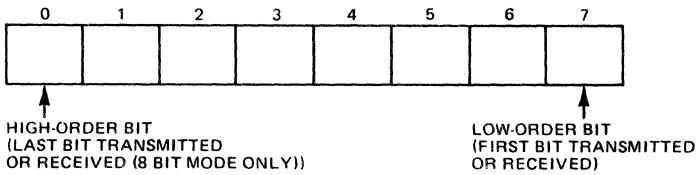
Address, Control, and Logical Control Fields



NOTES:
1. The format is the same for transmit and receive operation.
2. Bit 7 is the first bit transmitted or received.
3. All bytes should be full bytes of eight bits, in which case bit zero is the last bit. However, partial last bytes can be transmitted via TPLB and TLBS, and received via RPLB and RLBS. Partial bytes are right-justified. On receive, unused (leftmost) bits are set to zero by the Communications-Pac.
4. In extended address field mode, the first bit transmitted (bit 7, the low-order bit) of each address field octet is the continuation bit. This bit specifies the end of the address field as follows: bit 7 = 0 indicates that another address field octet is to follow; bit 7 = 1 indicates that this is the last address field octet.
5. For the logical control field, the last bit transmitted (bit 0, the high-order bit) of each logical control field (LCF) octet is the continuation bit. This bit specifies the end of the logical control field as follows: bit 0 = 0 indicates that another LCF octet is to follow; bit 0 = 1 indicates that this is the last LCF octet.

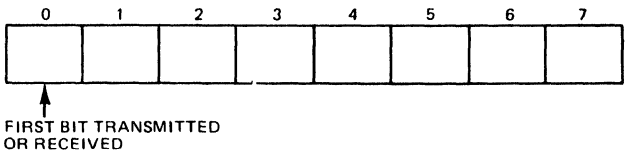
Text Field

Normal (Non-Bit Stream) Mode



NOTES:
1. The format is the same for transmit and receive operation.
2. Bit 7 is always the first bit transmitted or received.
3. Bytes of less than eight bits are right-justified (by the MLCP for transmit; by the Communications-Pac for receive). On receive, the adapter sets unused left-most bits to zero.

Bit Stream Mode



NOTES:

1. The format is the same for transmit and receive.
2. Bit zero is always the first bit transmitted or received.
3. With the possible exception of the last byte, all bytes contain eight bits, with bit 7 being the last bit transmitted or received. If the last byte contains less than eight bits, it is left justified (by the MLCP for transmit; by the Communications-Pac for receive). On receive, the Communications-Pac sets unused (rightmost) bits to zero.

BYTE SIZE CONTROL

Byte sizes (i.e., data elements) of 5, 6, 7, or 8 bits are defined for the Communications-Pac through the Text Control byte of the frame or the configuration register. The Communications-Pac performs the sensing and dynamic switching without assistance from the MLCP. The transmit and receive channels of a line need not have the same byte size. Byte size includes all valid bits that are to be transmitted or received including any programmed parity bits.

Transmit Byte Size

The reference tables (H-2 through H-5) that follow are to be used in conjunction with the line register information presented earlier (refer specifically to line registers 6 and 7). Information is presented on the coding for the Transmit Byte Size, Transmit Last Byte Size and Transmit Text Control Byte (bits in line register 7). Differences between the companion Receive line register 7 bits are noted at the end of this section. The tables specify text field byte size control. The byte size of address field, control field, and logical control field bytes is normally eight bits. Although partial last bytes (i.e., less than eight bits) may be accommodated, this would be an abnormal situation.

Table H-2. Text Field Byte Size

Frame Type	Applies When:	Text Field Byte Size		
			Last	
		All Except Last	Full (TPLB = 0)	Partial (TPLB = 1)
A. Supervisory or non-sequenced format	First bit of (link) control field = 1	8	8	TLBS
B. Information field format with no text control byte and not bit steam mode.	First bit of control field = 0; TTCB = 0; and TBS ≠ 011.	TBS	TLBS	TLBS
C. Information field format with text control byte but not bit stream mode	First bit of control field = 0; TTCB = 1; TBS ≠ 011; and TCB bits 5,6,7 ≠ 011.	TCB (bits 5,6,7)	TCB (bits 5,6,7)	TLBS
D. Information field format and bit stream mode	First bit of control field = 0; TTCB = 1; and TCB bits 5,6,7 = 011. OR First bit of control field = 0; and TBS = 011.	8	8	TLBS

Notes:

1. See Table H-3 for TBS encoding.
2. See Table H-4 for TLBS encoding.
3. See Table H-5 for TCB encoding.
4. When bit stream mode is specified by TBS = 011, the text field immediately follows the control field regardless of TTCB and TLCF.

Table H-3. TBS Encoding

TBS	Text Field Byte Size
000	5
001	RFU (8)
010	6
011	Bit Stream Mode (8)
100	7
101	RFU (8)
110	8
111	4

Table H-4. TLBS Encoding

TLBS	Full Byte (TPLB = 0)	Partial Byte (TPLB = 1
000	5	5
001	RFU (8)	1
010	6	6
011	RFU (8)	2
100	7	7
101	RFU (8)	3
110	8	8
111	4	4

Table H-5. TCB Encoding

Text Control Byte (Bits 5,6,7)	Text Field Byte Size
000	8
001	RFU (8)
010	RFU (8)
011	Bit Stream Mode
100	4
101	5
110	6
111	7

Receive Byte Size

Receive byte size control is basically the same as transmit. A set of tables could be generated similar to the preceding tables with the following two differences:

1. Note the following mnemonic changes:

   TTCB becomes RTCB
   TBS becomes RBS
   TPLB becomes RPLB
   TLBS becomes RLBS

2. Note that for transmit, TPLB and TLBS are output control to the Communications-Pac; whereas for receive, RPLB and RLBS are input status from the Communications-Pac. RPLB always provides an exact count of the number of bits in the last byte.

INITIALIZATION AND STARTUP GENERAL GUIDELINES

When the Communications-Pac is initialized (see Figures H-18 and H-20), it enters test mode, loops back transmit to receive, marks the line and sets most register bits to zero. The following actions perform initialization:

- o MLCP Initialize
- o CPU Clear (BSMCLR – Signal on Bus)
- o Power On

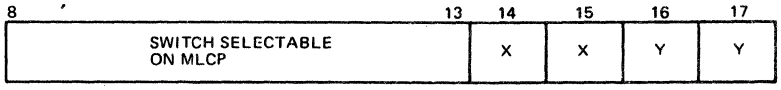
Master Clear

Execution of an IO (Output MLCP Control) instruction by the main memory program causes (among other operations) a master clear of each Communications-Pac.

A master clear causes each Communications-Pac to be unconditionally placed in a quiescent state: line register 2 is reset to zero, channel request interrupts are inhibited, and the Communications-Pac is placed in test mode.

Channel Number Assignment

The Communications-Pac occupies two MLCP channels and makes two additional channels usable. This is shown by the following:



where xx denotes MLCP adapter slot:

00 = highest adapter
11 = lowest priority adapter

yy: 00 = Communications-Pac Receive Channel
01 = Communications-Pac Transmit Channel
10 = Not usable
11 = Not usable

Device ID Assignment

Line register zero of both transmit and receive sides of the Communications-Pac provides a device identification number when read. This number is:

$F6_{16}$ for DCM9112
$F7_{16}$ for DCM9113
$F8_{16}$ for DCM9121

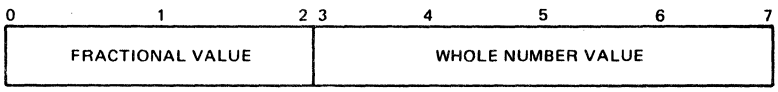
An Input Device ID I/O order (FC=26) addressed to an MLCP channel to which the Communications-Pac is connected will return the Device ID escape code of $(2178)_{16}$. An Input Extended ID I/O Order (FC=08) addressed to an MLCP channel to which the Communications-Pac is connected will return the number provided by the adapter in the high order 8 bits, i.e.:

$F6xx_{16}$ for DCM9112
$F7xx_{16}$ for DCM9113
$F8xx_{16}$ for DCM9121

Firmware Revision Level

The Communications-Pac contains two firmware microprograms – one for transmit and one for receive. The CCP can determine the revision level of either at initialization. The procedure for doing this is shown in Figure H-18 for transmit and Figure H-20 for receive. TFRR and RFRR (see Table H-6 for definitions of these bits) specify that the report shall be made. The format for transmit after the counting loop has been completed is shown below. For example, a value of 93 hexadecimal (10010011) translates into a value of 19.4 decimal.

The firmware revision levels are available in printout upon execution of the Honeywell-supplied diagnostic program for the Communications-Pac.



Data Transfer Clocks

The line may use one of two clock sources: one external (e.g., modem), one internal (the MLCP clock common to all lines).

The data set clock of the communications line is connected to the Communications-Pac by means of data communications equipment and is used if data transfers are taking place in "normal" (i.e., not "loop-back" test) mode. (If the data set clock permits data transfers at either of two speeds, bit 3 of line register 2 can be used to indicate which of the two speeds is desired.)

The MLCP's fixed-rate clock is used if the communications line is direct-connected to the Communications-Pac and/or if data transfers are taking place in "loop-back" mode (see bits 4 and 5 of line register 2). A switch on the MLCP determines the rate and is selectable at installation. The possible settings of the MLCP's fixed-rate clock are shown in Table 6-5.

There is only one fixed-rate clock per MLCP, which forces all lines that are directly connected to run at the selected speed of the fixed-rate clock.

TRANSMIT OPERATIONS

The programming guidelines for transmit operations presented in the paragraphs that follow are accompanied by a system flowchart that defines the specific sequence in which the functions are to be done (Figure H-18). The reader should be familiar at this point with the frame structure, line registers, and initialization procedures, discussed previously. Table H-6 provides a convenient key to the abbreviations used in the flowchart.

Startup and Interframe Considerations

Refer to the startup procedure portion of the flowchart, Figure H-18 ("T-START", "T-F/W REV", "T-START 3", "T-START 4"). Transmit operation is initialized whenever a Master Clear is received (see Note 3 of Figure H-18). This action sets the test mode (bit 5 in line register 2) which action, internally to the Communications-Pac, connects the transmit output to the receive output. That is, the transmit data in transmit line register 1 is shifted into the receive data register, receive line register 1, instead of being sent to the modem. The normal transmit data signal to the modem is forced to the marking (idle link) state. The normal receive data signal from the modem is ignored. Other bits in line register 2 are reset (to zero), effectively disconnecting the DCE interface. The Direct Connect Clock, provided by the MLCP, may be used for clocking. The CCP must perform the functions specified starting at "T-START" whenever the Communications-Pac is initialized.

When transmit operation to the modem is to begin, the CCP loads common line register 2, and transmit line registers 6 and 7 with the appropriate control and configuration information. Refer to "T-TURN ON" in the flowchart, Figure H-18. This connects the modem to the transmit side of the Communications-Pac and the transmitter begins sending flag or abort sequences as specified by the Transmit Interframe Fill Mode (bit 3 in transmit line register 6).

Assuming that Transmit On (bit 7 of line register 2) is set, and that Request to Send (bit 1 of line register 2) and Clear to Send from DCE (bit 1 of line register 5) are set, the transmitter generates a channel request interrupt. And, since the 64-byte FIFO buffer (transmit line registers 1 and 7) is initially "not full", the Adapter Ready signal is in the on state (which is indicated by the setting of bit 4 of line register 5). The CCP, when ready, should begin to fill the FIFO buffer with configuration and data bytes. As soon as the FIFO buffer contains data and the Transmit Buffer Fill Mode (bit 2 of line register 6) allows it, the transmitter generates and transmits a flag and then begins transmitting data from the FIFO. Refer to "T-INTER", "T-SOF", and "T-INTRA A" in Figure H-18.

Data Transfer During Frame

Refer to "T-INTRA B" in the flowchart (Figure H-18) and also to the transmit loop (Figure H-19). Each data byte sent by the MLCP is loaded into the FIFO stack input and at the same time a copy of line register 7 is made into the configuration-1 portion of that FIFO location. The Adapter Ready signal will remain true as long as the stack is not full. As characters reach the bottom of the stack, the Communications-Pac continues to unload and transmit characters, advancing the stack as it goes.

The Communications-Pac senses the address and control fields in accordance with the Transmit Address Field Extenstion and Transmit Control Field Extenstion (bits 1 and 0 respectively of transmit line register 7). The Communications-Pac likewise senses the logical Control Field, if present (bits 2 and 7 of transmit line register 7) and extracts Text Size and information from the Text Control Byte; at the appropriate time it will load this value into its character size control register so that text characters are correctly dissassembled into serial bits. The transmit loop CCP performed by the MLCP loads characters into the FIFO as long as the Adapter Ready signal is true. After a WAIT instruction has been executed, the Communications-Pac will send a channel request interrupt to the MLCP whenever the transmit FIFO memory has space available, and will set Adapter Ready true at the same time.

A suggested transmit loop CCP is shown in Figure H-19. The intraframe loop, being the most critical, is shown in the most detail. Note the use of the BART instruction.

Once the CCP has begun servicing a FIFO as a result of a channel request interrupt, it senses the state of Adapter Ready and continues to send it characters as long as Adapter Ready is true, without the need for a channel request interrupt on each character (since a wait state is not entered).

Transmit channel request interrupts are also controlled on a line basis through the Transmit On bit in line register 2. If Transmit On is reset, the transmitter will not generate channel request interrupts.

End of Frame

Refer to "T-EOF" in Figure H-18. The data load and unload of the FIFO, disassembly, serial shifting, and CRC calculation continues until a last character condition is detected by the CCP. The CCP then loads a one into the Transmit End of Frame (TEOF) bit of line register 7. It does this before sending the last character to the Communications-Pac; when it sends the last character to the Communications-Pac, that character will enter the FIFO with the TEOF bit in the corresponding configuration-1 field of the FIFO location set to true state. The Communications-Pac then immediately puts Adapter Ready to false state and the CCP then enters the wait state.

Meanwhile, the Communications-Pac continues to shift out the data characters as they are retrieved from the bottom of the stack. When the TEOF bit drops out of the bottom of the stack, the Communications-Pac switches back to 8-bit mode, transmits the CRC residue (FCS sequence) and then transmits a flag. It then clears line register 7, resetting the TEOF bit, and, assuming that Transmit On is still true, sends a channel request interrupt to the MLCP. Since there is no underrun condition stored, it also resets the Transmit Underrun bit in line register 5. As the result of this channel request interrupt, the CCP starts executing, reads the status word in line register 5, and reports the condition of the transmit Underrun bit to the MMP.

If Clear to Send is still On, the Communications-Pac sends another channel register interrupt to the MLCP. If the CCP wishes to proceed with the next frame, it loads line register 7 with the appropriate frame specification, gets the next block and proceeds to deliver data to the Communications-Pac FIFO. Until this data is ready and the Transmit Buffer Fill Mode bit allows its transmission, the Communications-Pac sends interframe fill characters as specified by Transmit Interframe Fill Mode.

If the CCP, instead of proceeding with the next frame, wishes to loop on interframe fill characters, it may load line register 7 with TEOF set instead of with the next frame specification. The CCP then enters the wait state. The Communications-Pac transmits the specified number of interframe fill characters, clears line register 7, and assuming

that Transmit On is still true, sends a channel request interrupt to the MLCP. This loop may be repeated indefinitely until terminated by the CCP.

Byte Size Switching and FCS Handling

Dynamic byte size switching and FCS handling are preformed automatically by the Communications-Pac depending upon the value of the configuration word. Refer to the previous discussions of line registers and byte control.

Underrun Processing

Transmit underrun occurs if the stack underflows due to failure of the CCP to load the FIFO soon enough. If underrun occurs, the transmitter generates and sends an abort sequence followed by the flag interframe fill. It continues to request data from the MLCP but does not transmit it to the line. When end of frame is detected by the CCP (which then sets Transmit End of Frame – bit 3 of line register 7), the transmitter ceases to request data (as it does at the end of every frame) and the CCP enters a wait state. When the Transmit End of Frame bit drops out of the bottom of the stack, the Communications-Pac will send a channel request interrupt to the MLCP after having set Transmit Underrun – bit 7 of line register 5. The CCP inputs line register 5 and tests Transmit Underrun and, finding it true, branches to its underrun handling routine. On completion of this routine, the CCP again enters a wait state; the Communications-Pac senses this and clears its internally stored underrun condition. If Transmit On is still true, the Communications-Pac sends a channel request interrupt to the MLCP with the Adapter Ready signal in the true state and normal startup of the next frame may begin. Refer to "T-EOF" at "Examine TU" in Figure H-18.

Underrun is a fatal error to the frame from an HDLC procedural aspect. Treatment of the condition from this aspect is under control of the CCP/MMP.

Preloading the Transmit Buffer to Prevent Underrun

A technique to "preload" the transmit buffer is shown in Figure H-18, "T-SOF" and "T-INTRA". This technique involves the use of the TBFM (Transmit Buffer Fill Mode) (bit 2 of line register 6). (For a definition of this bit, refer to the line register discussion earlier in this section.) By preloading the transmit FIFO stack in this manner (before allowing transmission of the frame to begin), the CCP can reduce the possibility of underrun occurring. (Recall from the line register discussion that this possibility exists due to the requirements of the Communications-Pac's higher priority receive channel or to higher priority Communications-Pacs sharing the same MLCP.) If the frame is 64 bytes or less, the complete frame may be preloaded, thus unconditionally guaranteeing no underrun.

RECEIVE OPERATIONS

The programming guidelines for receive operations are presented in the paragraphs that follow and are accompanied by a system flowchart that defines the sequence in which the functions are done (Figure H-20). The reader should be familiar at this point with the frame structure, line registers, and initialization procedures, discussed previously. Table H-6 provides a convenient key to the abbreviations used in the flowchart.

Startup and Interframe Considerations

Refer to the Startup Procedure in Figure H-20 ("R-START", "R-F/W REV", "R-START 3", and "R-START 4"). The receive operation is initialized by a Master Clear from the MLCP (see Note 1 in Figure H-20). (This action sets the Test mode (bit 5 in line register 2) which, internally to the Communications-Pac, connects the transmit output to the receive input. Other bits in line register 2 are reset (to zero) effectively disconnecting the modem interface.) The CCP must perform the functions specified at "R-START" whenever the Communications-Pac is initialized.

When receive operation from the modem is desired, the CCP loads line register 2 and line register 6 with appropriate information. Refer to "R-TURN ON" in the

flowchart, Figure H-20. This connects the modem to the receive side of the Communications-Pac and the receiver begins shifting in serial data bits from the modem at a rate determined by the modem receive clock.

As each bit is shifted in, the receiver examines that bit and the seven preceding bits in search of a flag sequence (01111110). Once a flag is detected, the receiver has achieved frame synchronization; thereafter the receiver inspects each received octet for a non-flag or non-abort sequence. If additional flags are received, synchronization is maintained; if an abort (a sequence of seven contiguous ones) is found, synchronization is lost and must be reestablished.

When, in synchronization, a non-flag, non-abort octet is received, it is shifted further into the receiver as a byte. After 32 bits have been received (indicating a valid frame), the first octet is loaded into the data portion of the receive FIFO, and a status value of 00 (hexadecimal) is loaded into the status portion. When this reaches the bottom of the FIFO, a channel request interrupt is generated, causing the CCP to read status and detect the start of the frame condition ("R-INTER" to "R-INTRA").

Data Transfers

Refer to "R-INTRA" in Figure H-20. Each data byte received after the flag is loaded into the line register 1 portion of the FIFO stack by the Communications-Pac under control of its internal character size control register; at the same time and in parallel, the Communications-Pac also loads receive status information (which is 00 hexadecimal during the frame) into the line register 7 portion of the stack. Since the FIFO may in some cases be initially empty, Adapter Ready (bit 4 of line register 5) could be zero. The act of loading into the FIFO with Adapter Ready a zero would then cause the Communications-Pac to send a channel request interrupt to the MLCP; and Adapter Ready would also become a one at this time, indicating the presence of information in the FIFO. The Communications-Pac continues to load characters and receive status information into the FIFO, maintaining Adapter Ready in the proper state. The Communications-Pac senses the Address and Control fields in accordance with the Receive Address Field Extension and Receive Control Field Extension (bits 1 and 0 of line register 6 respectively). It likewise senses the Logical Control field if the frame is in Information Transfer Format and the Receive Logical Control Field (bit 7 of line register 6) so indicates. It extracts text size information from the Receive Text Control Byte and at the appropriate time sets the value into the character control register so that text characters are correctly assembled from the serial bits.

Once it has begun servicing a FIFO as a result of a channel request interrupt, the CCP senses the state of Adapter Ready and continues to send/accept characters as long as Adapter Ready is true, without the need for a channel request interrupt on each character (since a wait state is not entered). When Adapter Ready is found false, the wait state is entered. After this, the Communications-Pac will send a channel request interrupt to the MLCP whenever the FIFO has data and/or status information in it, and will set Adapter Ready true at the same time.

Receive channel request interrupts are also controlled through the Receive On bits in line register 2. If Receive On is reset, the receiver will not generate channel request interrupts.

The Receive loop CCP performed by the MLCP removes characters from the FIFO, by reading line register 1, as long as Adapter Ready is true. (The stack advances one location for each ready.) Refer to the example of a receive loop in Figure H-21.

End of Frame

Refer to "R-EOF" and subsequent end-of-frame processing routines in Figure H-20. The data shifting, character assembly, and FIFO load and unload process continues until a flag or abort sequence is detected by the Communications-Pac, denoting end of frame.

In the case of an abort, the Communications-Pac sets Receive Abort and Receive End of Frame (bits 0 and 3 of line register 7 respectively) at the top of the stack. No further loading of the stack occurs until synchronization is reestablished and a new frame begins to be received; it will then be loaded into the stack in the usual manner. When

the abort bit reaches the bottom of the stack it results in the CCP becoming aware of the abort at the point in the message stream at which it occurred. The condition is reported to software which takes further action. The CCP reads line register 1, thus advancing the stack and allowing the next frame to be read by the MLCP.

In the case of a normal frame termination by a flag sequence, the Communications-Pac sets Receive End of Frame in line register 7 at the top of the stack (the last character of the frame is concurrently loaded into the line register 1 half). It also sets the result of the FCS residue check into Receive Frame Check Sequence Error (bit 2 of line register 7) and sets the Receive Last Byte Size (bits 4-7 of line register 7) to indicate the number of valid bits in this last character at the same time. The internal character size register is reset to eight-bit size. If another frame follows after the flag, the Communications-Pac will proceed to load this into the top of the FIFO stack as previously described. When the Receive End of Frame bit reaches the bottom of the stack, it results in the CCP becoming aware of the end of frame at the proper point. The CCP tests the Receive Frame Check Sequence Error and Receive Last Byte Size bits of line register 7, passing this information on to software; it then reads line register 1 to obtain the last character of the frame, thus advancing the stack, and then prepares to receive the next frame.

Receive Overrun

Receive overrun occurs when the stack overflows due to the failure of the CCP to unload characters soon enough. When overrun occurs, the remainder of the frame is discarded by the Communications-Pac. When a flag or abort is received indicating end of frame, Receive Overrun and Receive End of Frame (RO and REOF, respectively) are loaded into the top of the FIFO. If the FIFO is still full, this action will be delayed until a location is available. When the Receive Overrun bit reaches the bottom of the stack it results in the CCP becoming aware of the overrun at the point in the message stream at which it occurred. The condition is reported to software which takes further action. The CCP then reads line register 1, thus advancing the stack and allowing the next frame to be read by the MLCP. Refer to "R-EOF" in Figure H-20.

Missed Frame Condition

A missed frame condition occurs if the overrun situation becomes so severe that entire frames are discarded in the Communications-Pac. This situation will be reported to the CCP by setting Receive Overrun, with Receive End of Frame a zero, in line register 7.

Idle Link State

The input line is defined to be in the idle state when a sequence of fifteen or more ones are received. This event causes the Communications-Pac to report abort without Receive End of Frame being set into line register 7 at the top of the stack. Succeeding action is similar to the abort case except that since normally there is no more data the FIFO will become empty, Adapter Ready will remain zero, and the CCP will remain in a wait condition. Refer to "R-INTER" in Figure H-20.

Receiver Resynchronization Control

Refer to "R-RESYNC" in Figure H-20. If a transmit or receive CCP performs a write to line register 3, the receiver FIFO stack will be cleared and no further data characters will be accepted into the stack until the receiver next senses a flag or idle link sequence. Normal operation then resumes.

DATA SET CONTROL AND STATUS

Bits 0 through 3 of line register 2 supply the data set control signals to the modem. Bits 0 through 3 of line register 5 represent the corresponding status signals from the modem. The Communications-Pac does a minimum with these signals except to pass them through between the CCP and the modem. The only exception is that the Communications-Pac will not generate channel request interrupts on transmit until Clear to

Send comes on from the modem and will stop generating channel request interrupts when Clear to Send goes off. The character in the process of being sent when Clear to Send, plus any characters in the FIFO, goes off will be sent (assuming the clock from the DCE keeps running).

The proper interpretation of data set status and the issuing of the data set control signals are a function of the CCP and/or the main memory program.

Timing

The data set control bits are output to the modem immediately upon loading line register 2. Because the Communications-Pac provides many characters of buffering via the FIFO memory, data set control changes (in particular Data Terminal Ready or Request to Send, bits 0 and 1 of line register 1 respectively) should not occur until the closing flag has had time to clear the Communications-Pac. Refer to "T-TURN OFF 2" in Figure H-18.

TABLE H-6. KEY TO ABBREVIATIONS AND CONFIGURATION FORMATS USED IN TEXT AND FLOWCHARTS (FIGURES H-18 AND H-20)

Abbreviation	Meaning	Line Register Bits Where Applicable
CCP	Channel Control Program	
CRI	Channel Request Interrupt (i.e., CCP execution started by interrupt from line adapter)	
CRC	Cyclic Redundancy Check	
EOF	End of Frame	
EOT	End of Transmission	
FCS	Frame Check Sequence	
FIFO	First-in, First-out memory (refers to stack)	Line registers 1 and 7, transmit and receive
H'xx'	Indicates a hexadecimal value of xx	
INTER	Inter-frame (between frames)	
INTRA	Intra-frame (within a frame)	
IRLC	Internal Revision Level Counter	
LCF	Logical Control Field	
LCT	Line Control Table	
LR	Line Register	
PB	Partial Byte	
RAFX	Receive Address Field Extension	Bit 1 of LR6, receipt of frame format
RA/I	Receive Abort/Idle Link State	Bit 0 of receive LR7
RBS	Receive Byte Size	Bits 4-6 of LR6, receipt of frame format
RCFX	Receive Control Field Extension	Bit 0 of LR6, receipt of frame format
REOF	Receive End of Frame	Bit 3 of LR7
RFCSE	Receive Frame Check Sequence Error	Bit 2 of receive LR7
RFCSIE	Receive FCS Input Enable	Bit 3 of receive LR6, frame format
RFRR	Receive Firmware Revision Report	Bit 7 of receive LR6, initialization format
RI	See RA/I	
RICRCTM	Receive Input CRC Test Mode	Bit 4 of receive LR6, initialization format

TABLE H-6 (CONT.) KEY TO ABBREVIATIONS AND CONFIGURATION FORMATS USED IN TEXT AND FLOWCHARTS (FIGURES H-18 AND H-20)

Abbreviation	Meaning	Line Register Bits Where Applicable
RLBS	Receive Last Byte Size	Bits 4-6 of receive LR7
RLCF	Receive Logical Control Field	Bit 7 of receive LR6, frame format
RMM	Receive Major Mode	Bit 0 of receive LR6, initialization format
RO	Receive Overrun	Bit 1 of receive LR7
RPLB	Receive Partial Last Byte	Bit 7 of receive LR7
RTCB	Receive Text Control Byte	Bit 2 of receive LR6, frame format
TAFX	Transmit Address Field Extension	Bit 1 of transmit LR7, start of and during frame transmission format
TBFM	Transmit Buffer Fill Mode	Bit 2 of transmit LR6
TBS	Transmit Byte Size	Bit 4-6 of transmit LR7, start of and during frame transmission format
TCFX	Transmit Control Field Extension	Bit 0 of transmit LR7, start of and during frame transmission format
TEOF	Transmit End of Frame	Bit 3 of transmit LR7, start of and during frame transmission format, end of frame format, between frames format
TFRR	Transmit Firmware Revision Report	Bit 7 of transmit LR7, initialization format
TIFC	Transmit Interframe Fill Count	Bits 0-2 of transmit LR7, between frames format
TIFM	Transmit Interframe Fill Mode	Bit 3 of transmit LR6
TLBS	Transmit Last Byte Size	Bits 4-6 of transmit LR7, end of frame format
TLCF	Transmit Logical Control Field	Bit 7 of transmit LR7, start of and during frame transmission format
TMM	Transmit Major Mode	Bit 0 of transmit LR7, initialization format
TNFCS	Transmit No FCS	Bit 2 of transmit LR7, end of frame format
TPLB	Transmit Partial Last Byte	Bit 7 of transmit LR7, end of frame format
TRR	Transmit Resync Receiver	Bit 1 of transmit LR7, end of frame format
TTCB	Transmit Text Control Byte	Bit 2 of transmit LR7, start of and during frame transmission format
TU	Transmit Underrun	Bit 7 of transmit LR5
Configuration and Status Formats		
R6-1	Receive line register 6, initialization format	
R6-2	Receive line register 6, frame format	
R7-x	See Figure H-17 for status information	
T7-1	Transmit line register 7, interframe format	
T7-2	Transmit line register 7, start-of-frame format	
T7-3	Transmit line register 7, end-of-frame format	
T7-4	Transmit line register 7, initialization format	

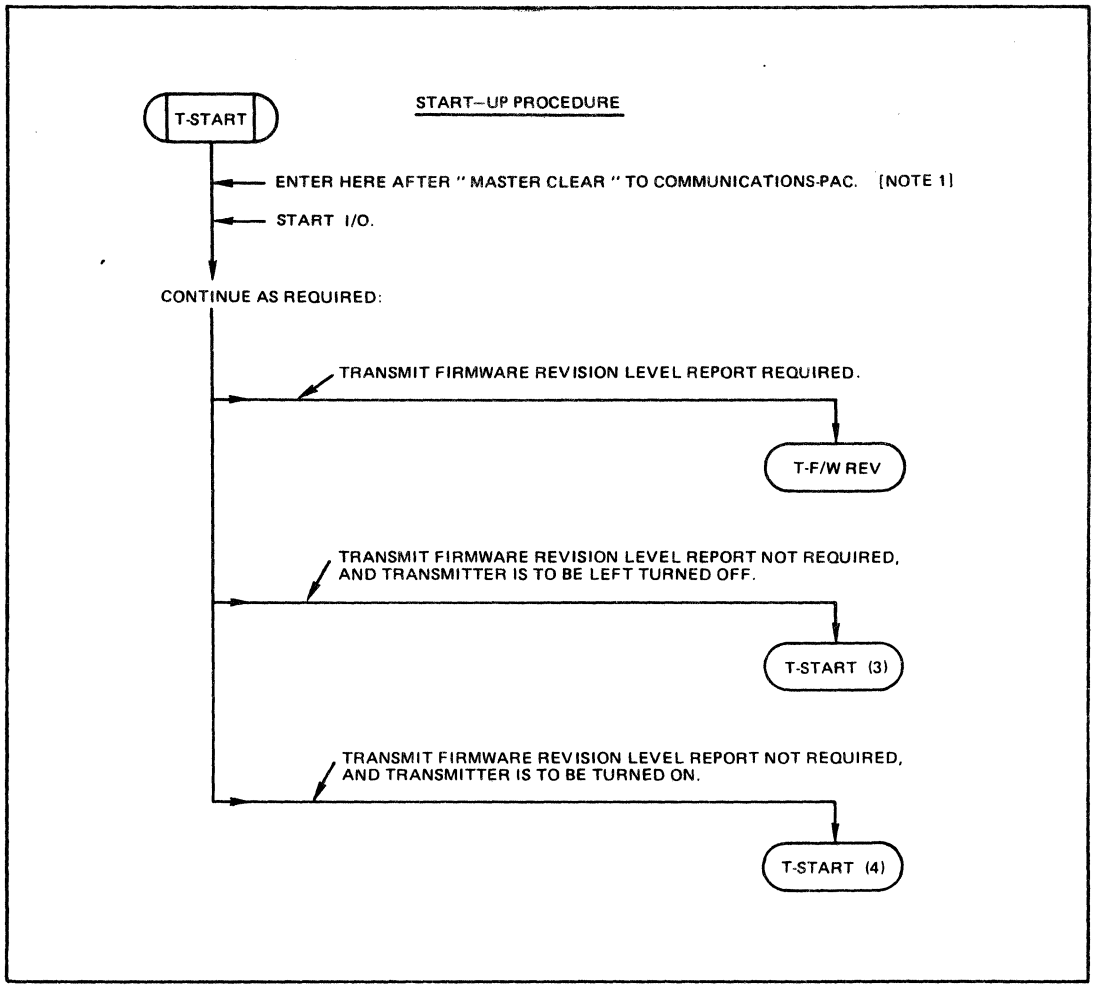


Figure H-18. Transmit Flowchart

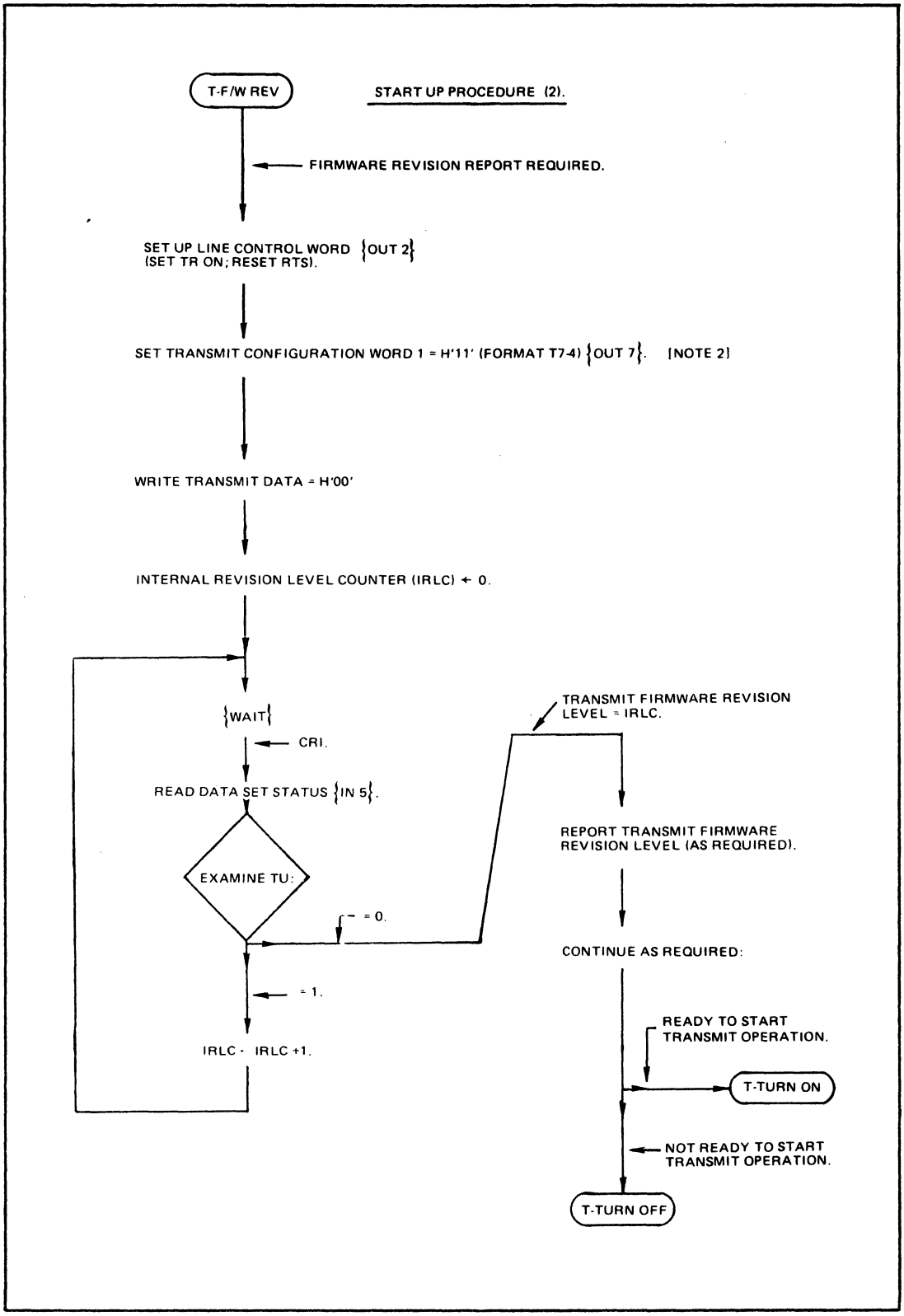


Figure H-18 (cont). Transmit Flowchart

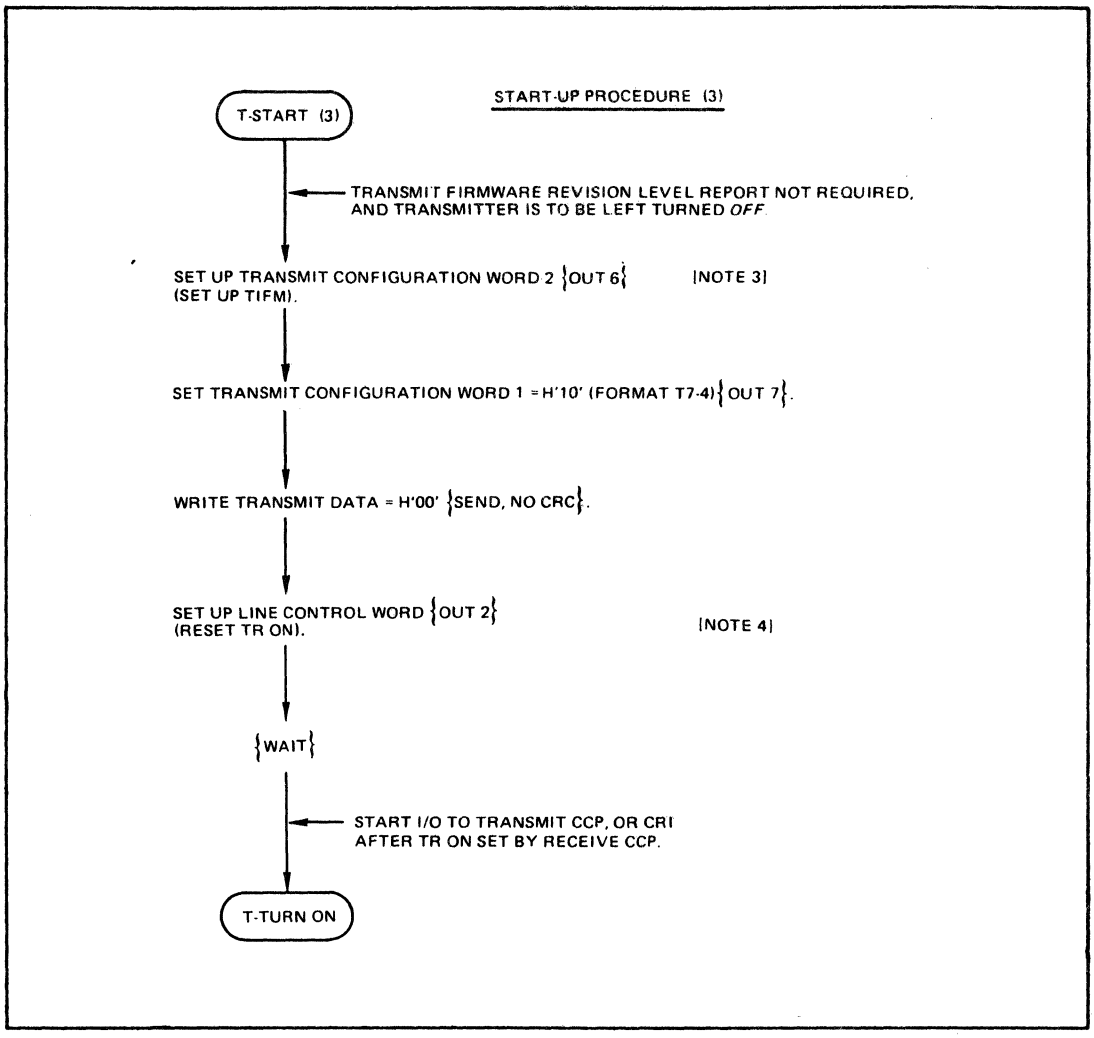


Figure H-18 (cont). Transmit Flowchart

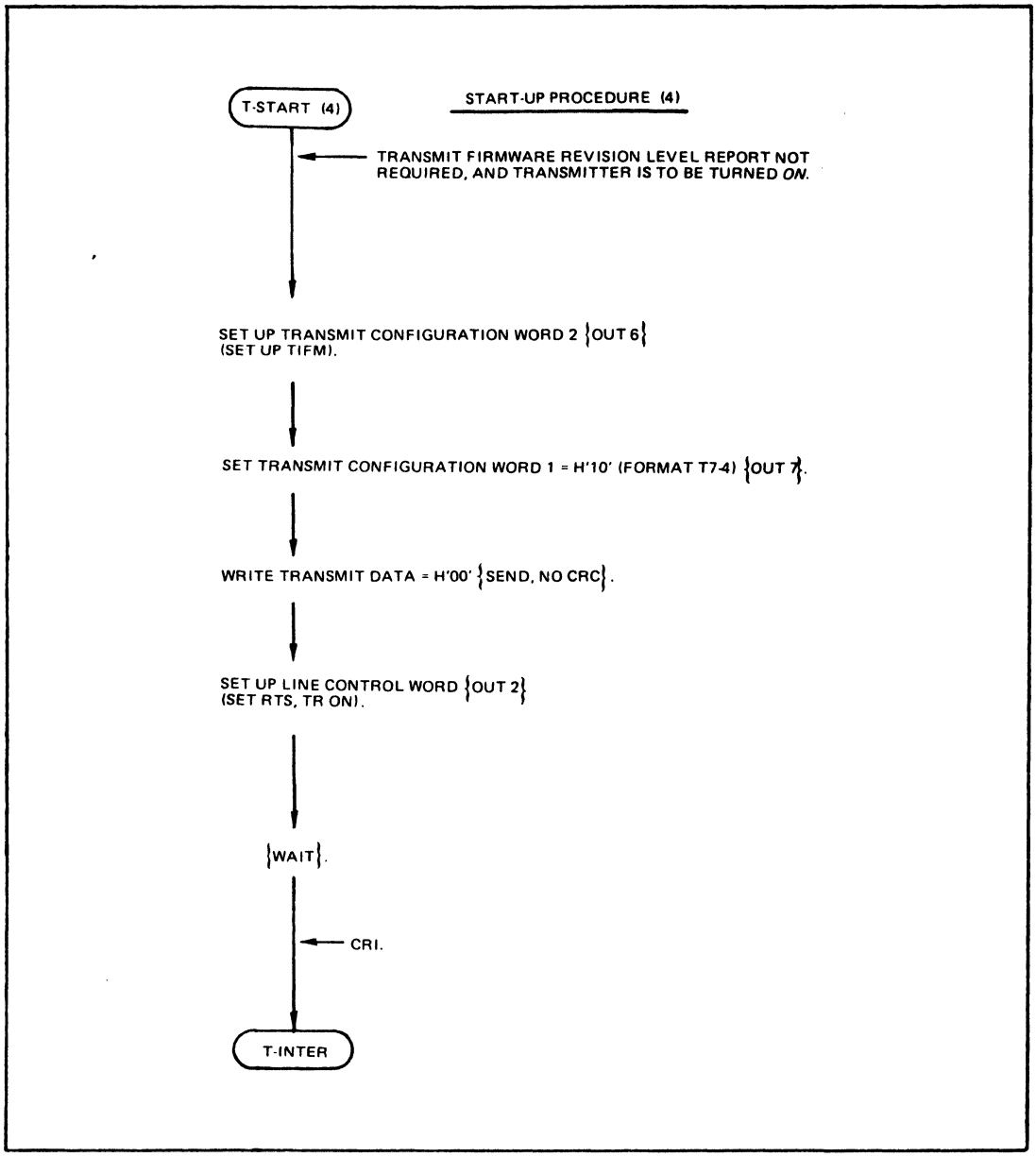


Figure H-18 (cont). Transmit Flowchart

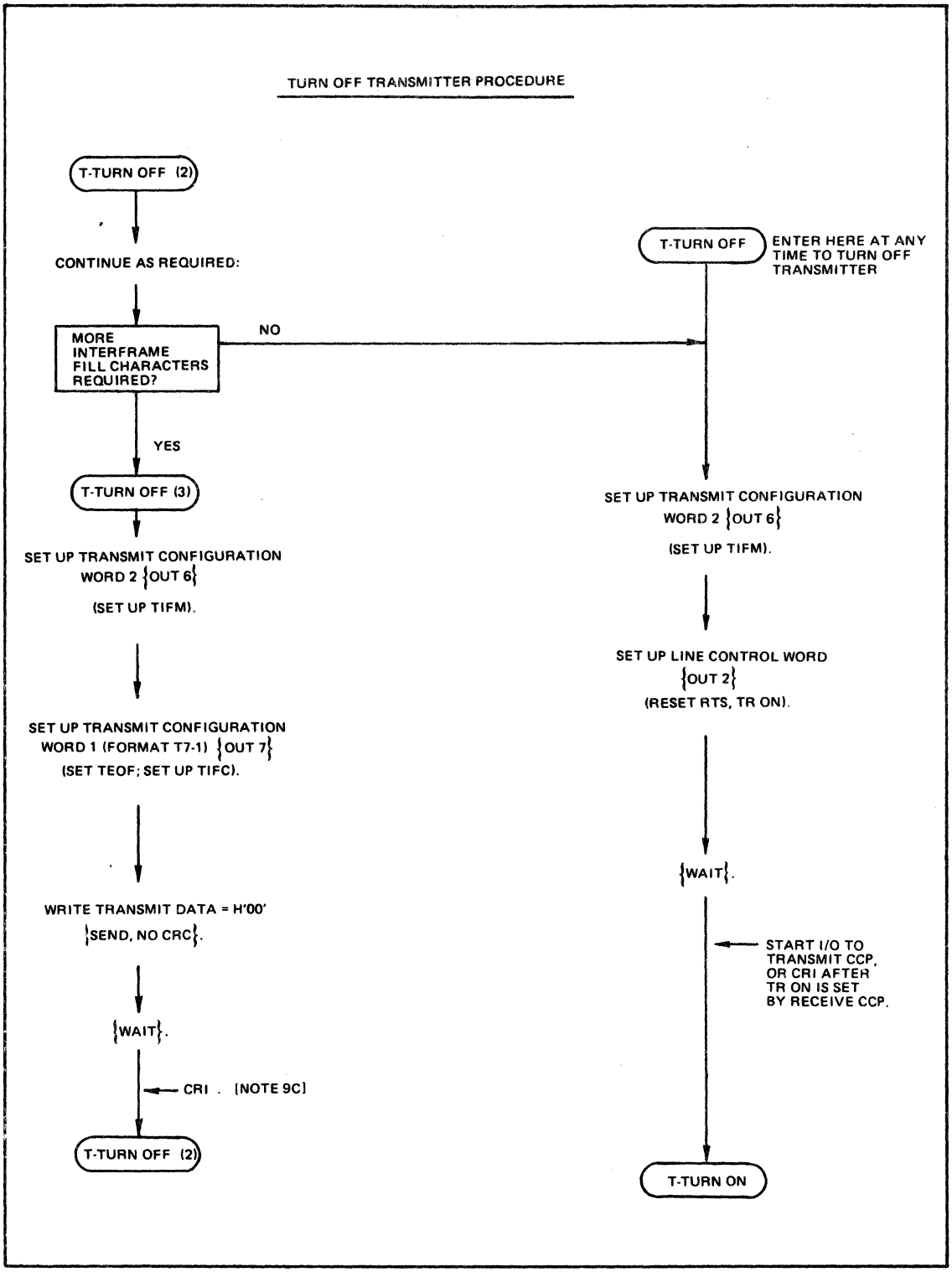


Figure H-18 (cont). Transmit Flowchart

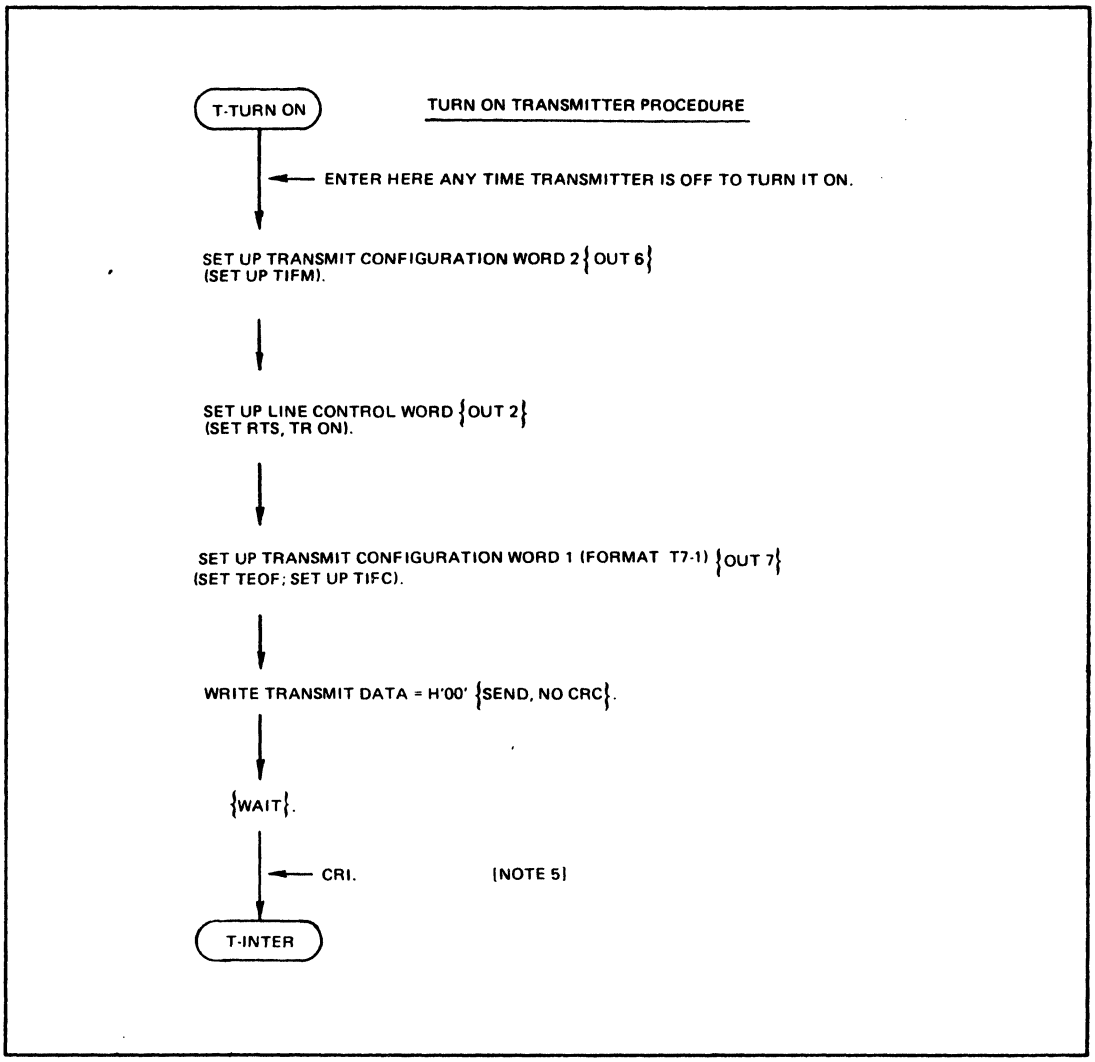


Figure H-18 (cont). Transmit Flowchart

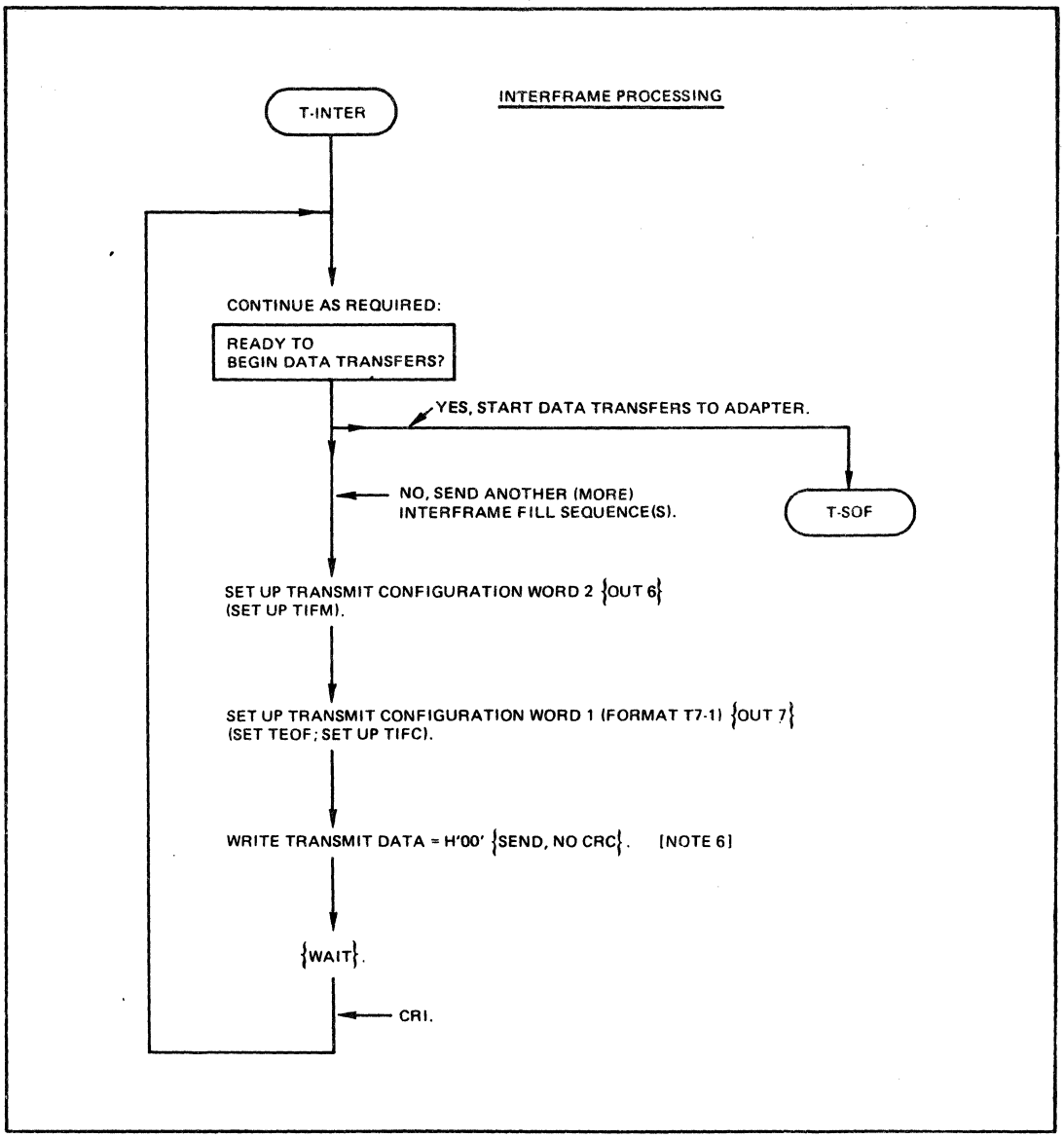


Figure H-18 (cont). Transmit Flowchart

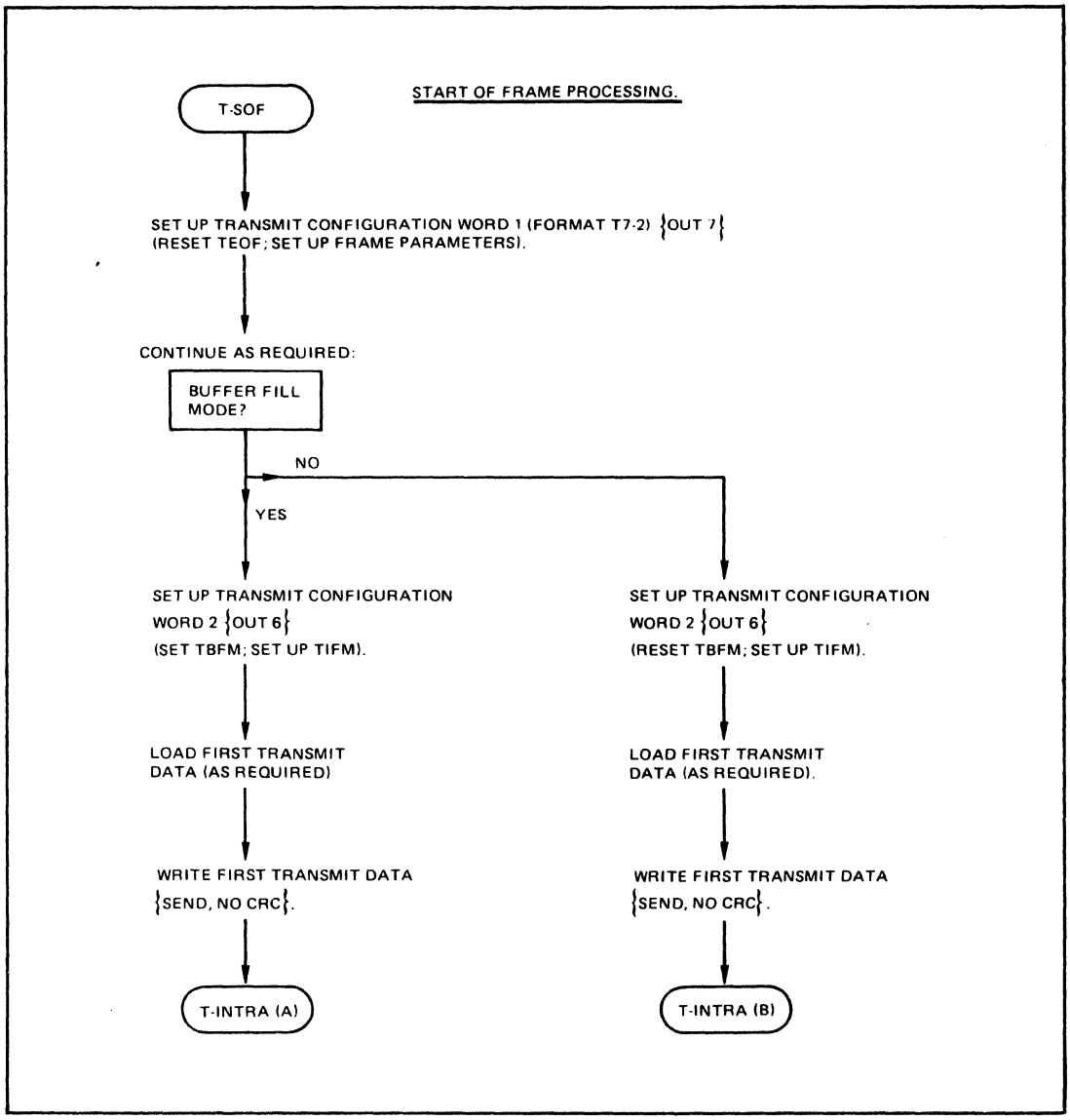


Figure H-18 (cont). Transmit Flowchart

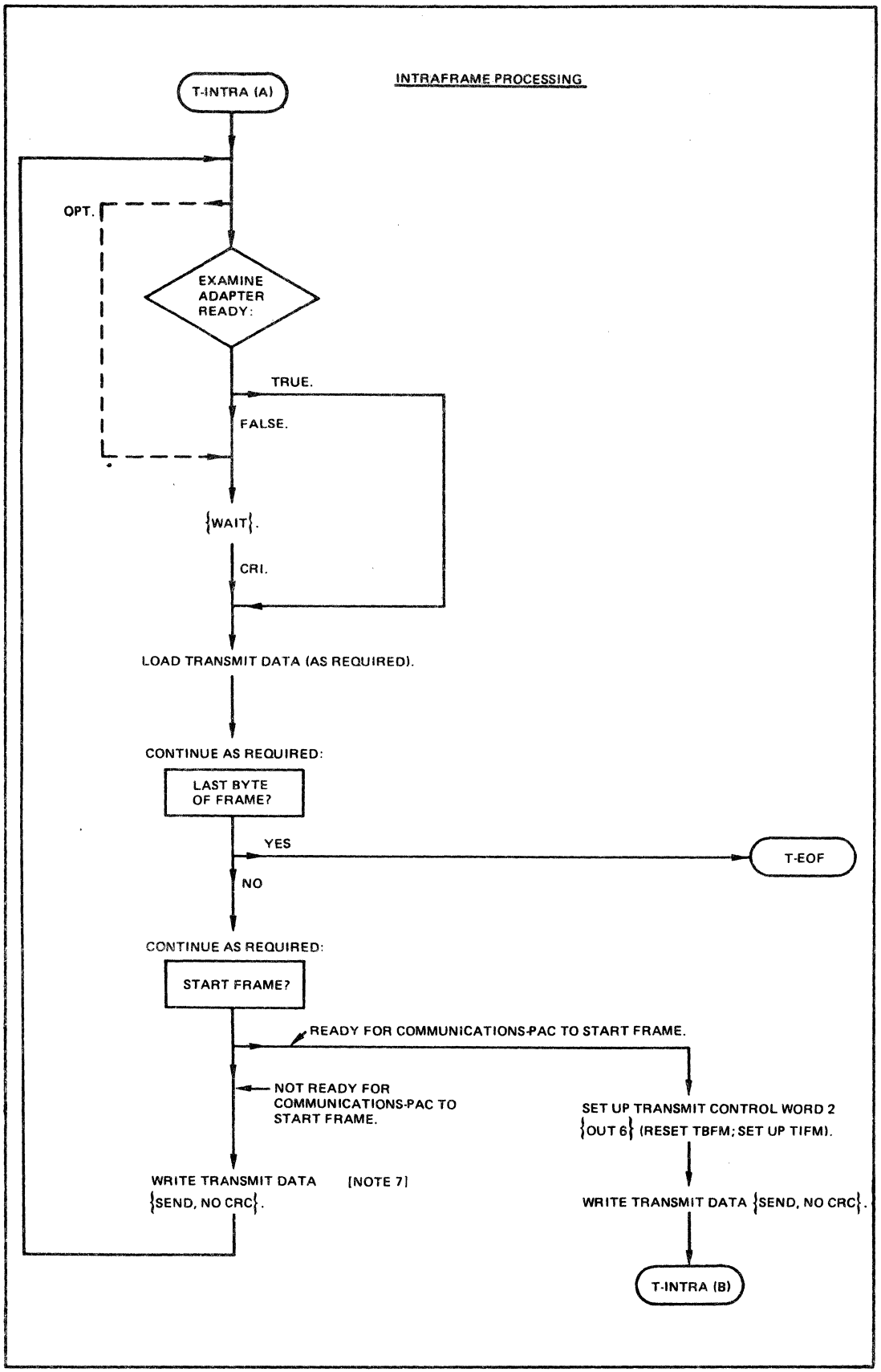


Figure H-18 (cont). Transmit Flowchart

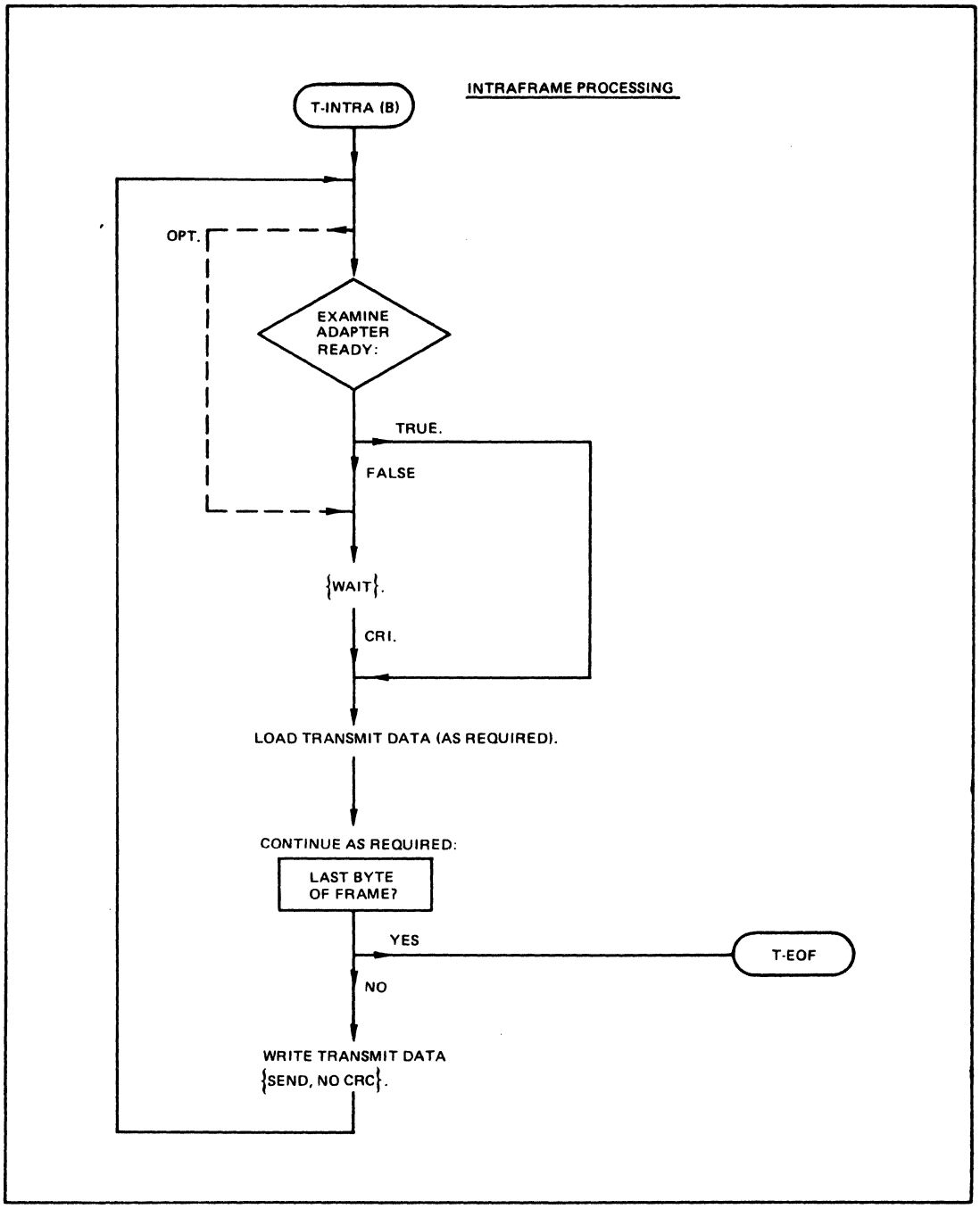


Figure H-18 (cont). Transmit Flowchart

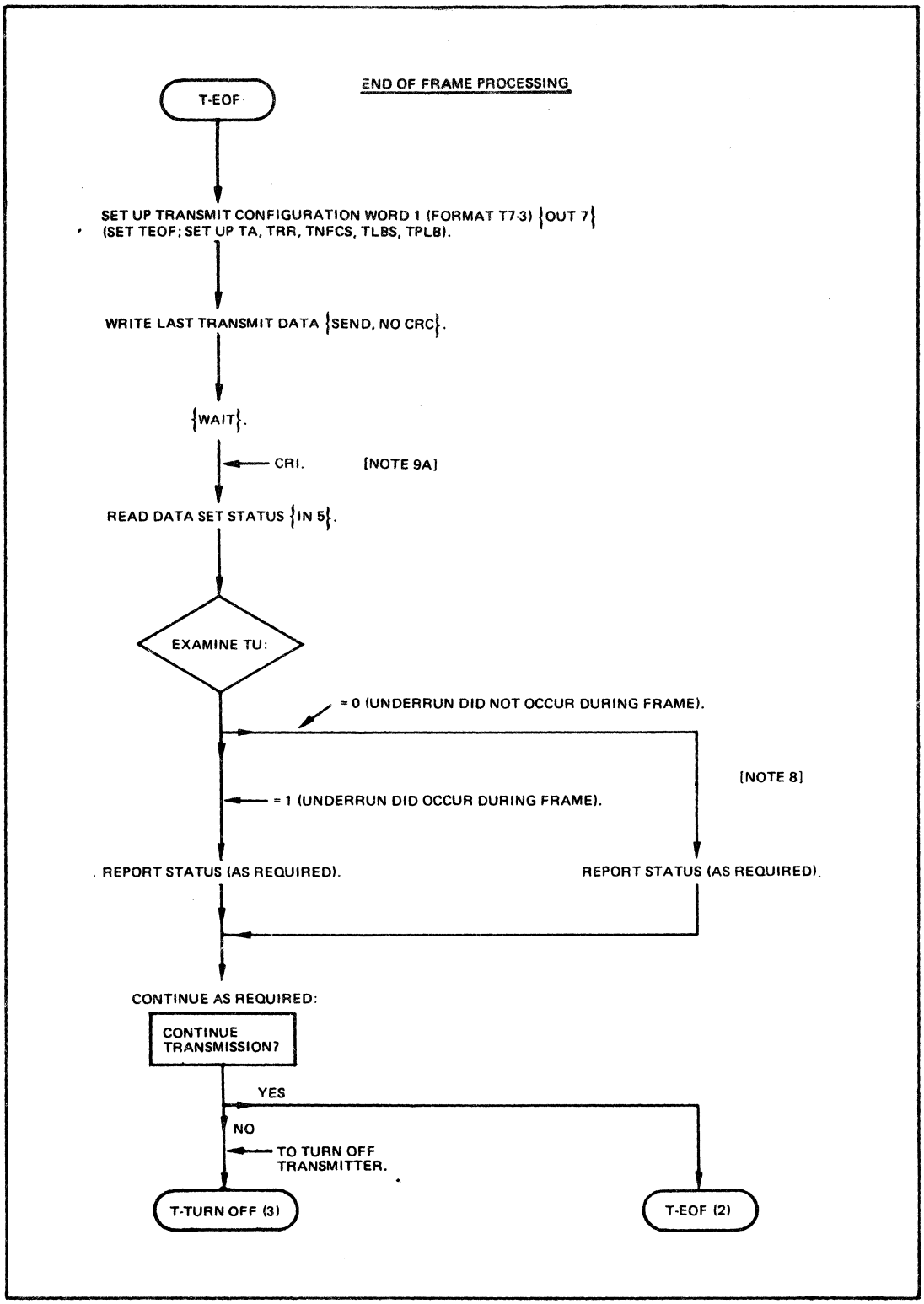
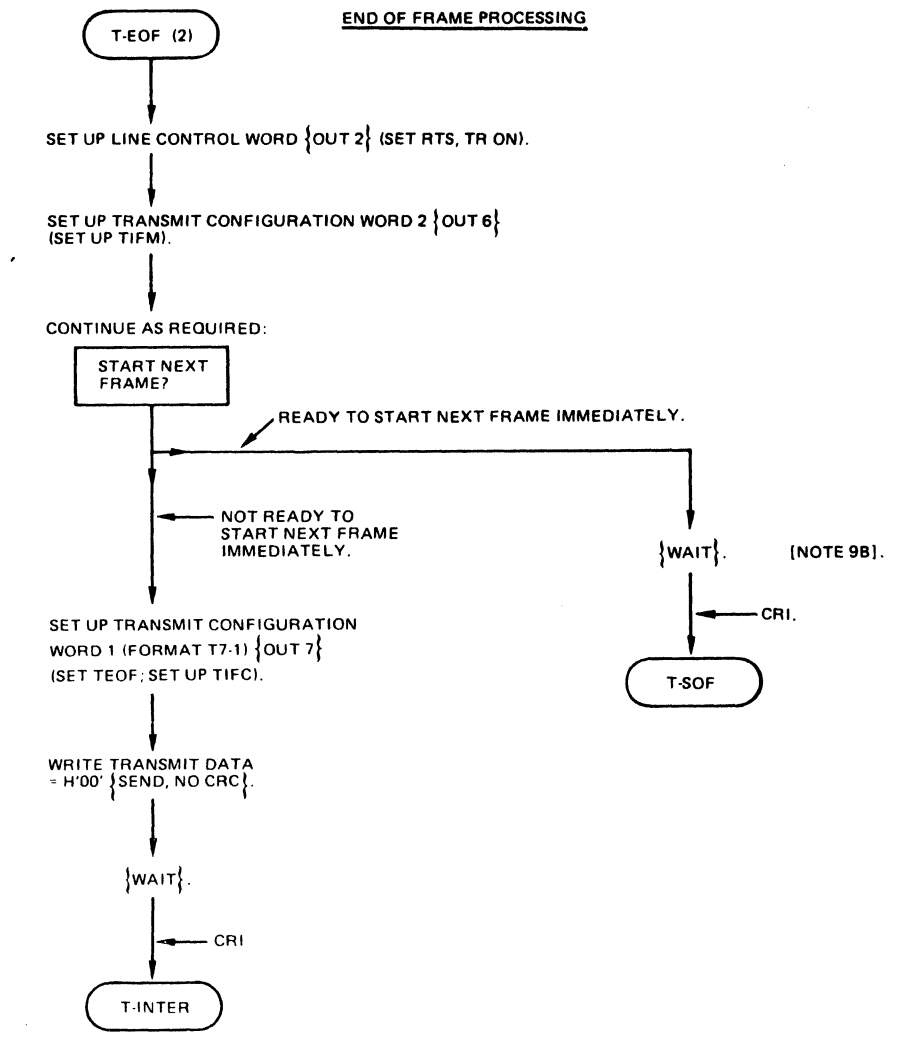


Figure H-18 (cont). Transmit Flowchart



NOTES:

1. EACH OF THE FOLLOWING EVENTS CAUSES THE MLCP TO ISSUE A MASTER CLEAR TO THE COMMUNICATIONS-PAC:
   - o THE COMPUTER IS POWERED UP;
   - o THE CONTROL PANEL CLR BUTTON IS DEPRESSED (WHEN IN STOP STATE); OR
   - o AN IO (OUTPUT MLCP CONTROL) INSTRUCTION WITH BIT 0 = 1 IS ISSUED TO THE MLCP.
2. H'xx" INDICATES A HEXADECIMAL VALUE OF xx.
3. IT IS NECESSARY TO OUTPUT TO LR6 ONLY WHEN ITS CONTENTS REQUIRE CHANGING.
4. IT IS NECESSARY TO OUTPUT TO LR2 ONLY WHEN ITS CONTENTS REQUIRE CHANGING.
5. EXCEPT FOR START-UP PROCEDURE AND STATUS REPORTING AT END OF FRAME, CRIs ARE GENERATED ONLY UNDER THE FOLLOWING CONDITIONS:
   - o THE FIFO MEMORY IS NOT FULL;
   - o TEOF IN LR7 IS RESET;
   - o RTS IN LR2 IS SET; AND
   - o CTS FROM THE DCE IS SET (OR TEST IN LR2 IS SET).
6. IF ONLY ONE INTERFRAME FILL SEQUENCE IS SELECTED (I.E., IF THE IDLE COUNT IN LR7 IS SET TO ZERO); THEN THIS SEND IS NOT REQUIRED.
7. TRANSMIT DATA MAY BE TRANSFERRED TO THE COMMUNICATIONS-PAC BY THE OUTPUT (LR1) INSTRUCTION, ASSUMING NO PARITY IS BEING GENERATED SINCE THE COMMUNICATIONS-PAC IS PERFORMING THE CRC/FCS GENERATION. THE OUTPUT INSTRUCTION IS RECOMMENDED BECAUSE OF ITS FASTER EXECUTION TIME.
8. NOTE THAT STATUS (I.E., UNDERRUN) REPORTING IS *NOT* ACCOMPLISHED BY THE SEND COMMAND.
9. END OF FRAME INTERRUPT TIMING:
   - A. THIS END OF FRAME INTERRUPT (THE INTERRUPT WHERE UNDERRUN SHOULD BE TESTED) IS GENERATED BEFORE THE CLOSING FLAG OR ABORT SEQUENCE HAS BEEN SENT. THEREFORE, IT SHOULD NOT BE USED AS A TIMING SIGNAL TO CHANGE DCE CONTROL SIGNALS.
   - B. SINCE TEOF HAS NOT BEEN SET AGAIN, THIS INTERRUPT WILL OCCUR IMMEDIATELY. HOWEVER, EVEN IF DATA FOR THE NEXT FRAME IS PROVIDED VERY QUICKLY, FOUR INTERFRAME FILL CHARACTERS WILL BE SENT BEFORE TRANSMISSION OF THE NEXT FRAME BEGINS.
   - C. FOR THE FIRST END OF FRAME INTERRUPT, THIS CRI DOES NOT OCCUR UNTIL THE CLOSING FLAG OR ABORT PLUS THREE INTERFRAME FILL SEQUENCE (PER TIFM) HAVE BEEN SENT. THIS MEANS THAT THE DCE CONTROL SIGNALS (E.G., REQUEST TO SEND) MAY BE CHANGED AT THIS TIME WITHOUT AFFECTING THE FRAME JUST SENT OR THE IDLE LINK STATE, IF APPLICABLE.

Figure H-18 (cont). Transmit Flowchart

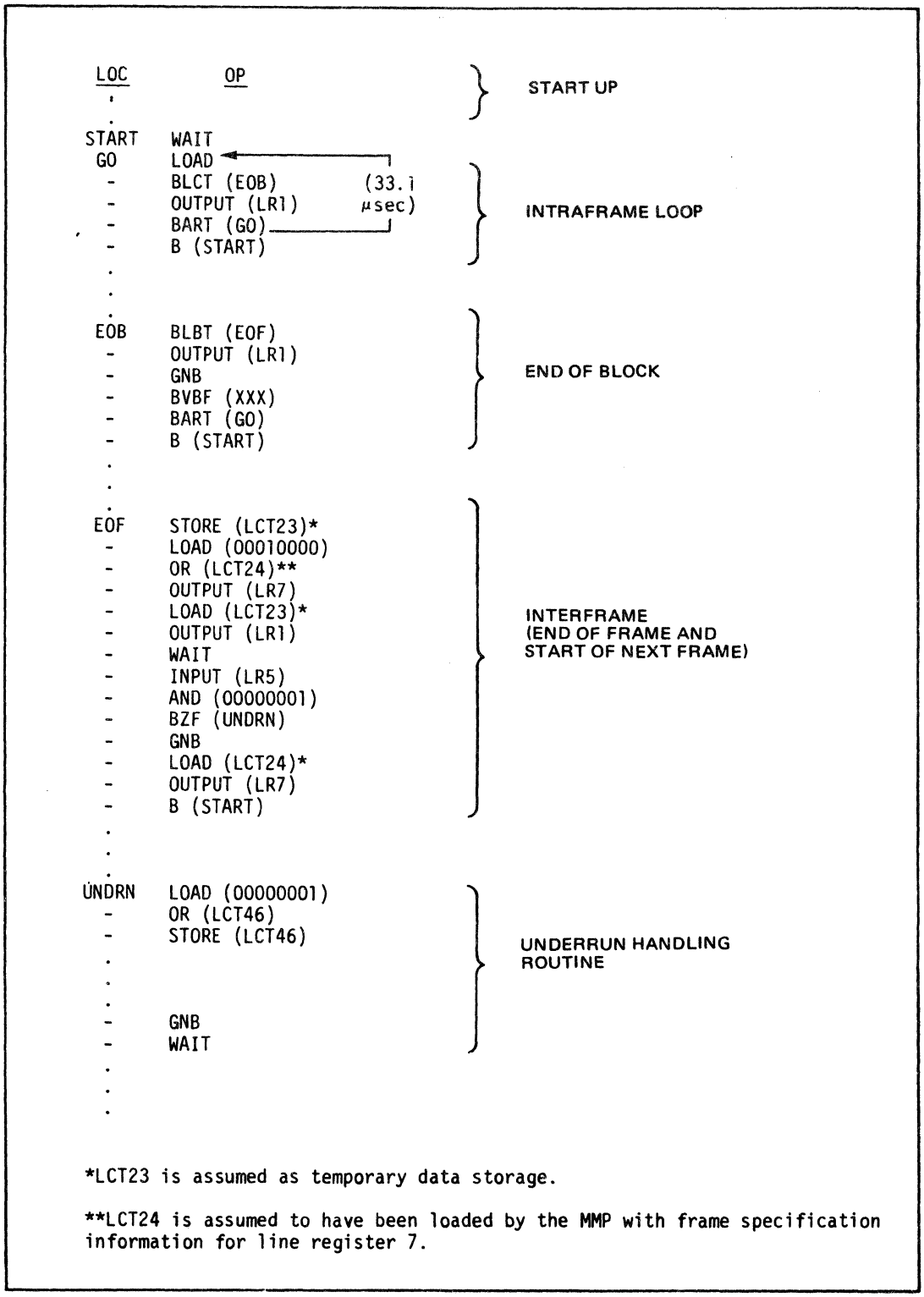


Figure H-19. Transmit Loop

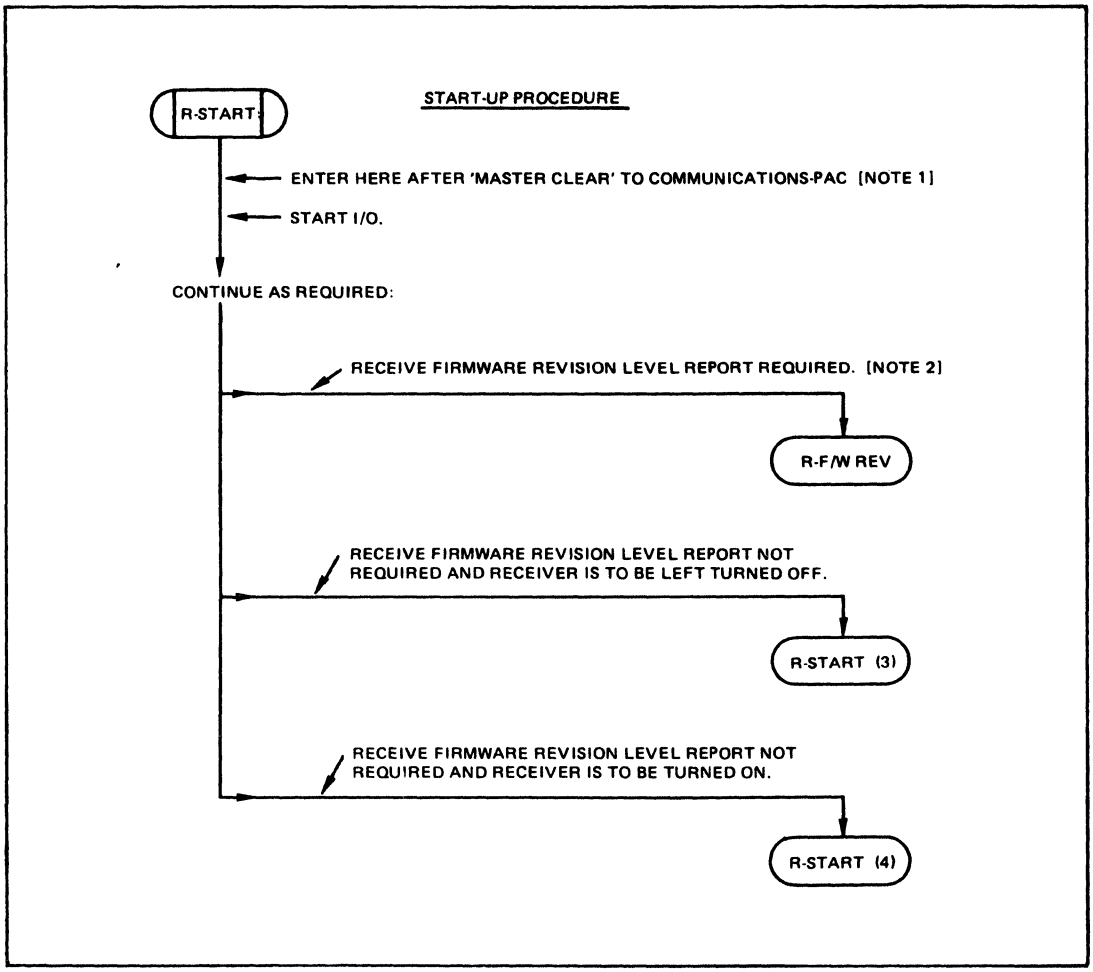


Figure H-20. Receive Flowchart

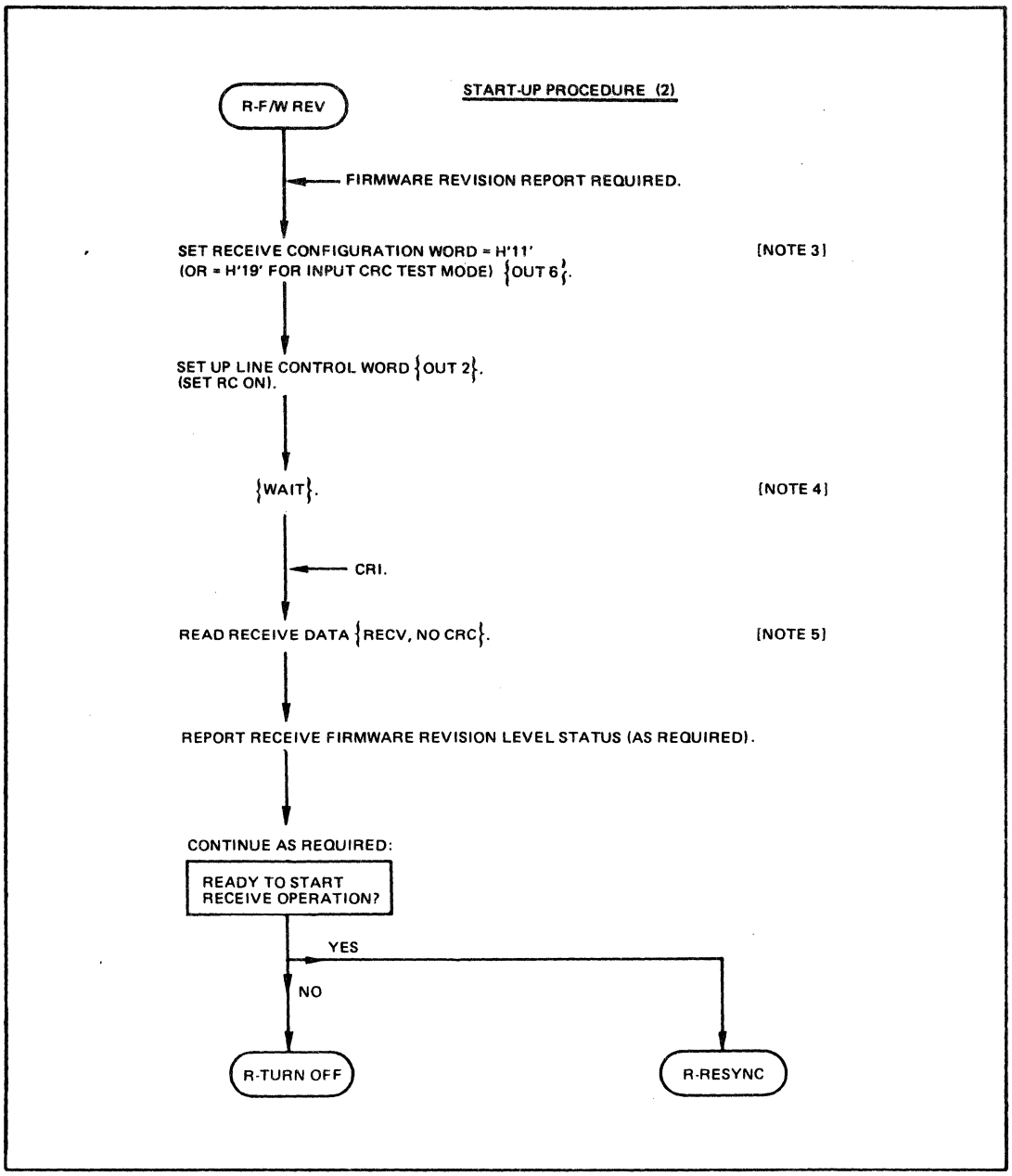


Figure H-20 (cont). Receive Flowchart

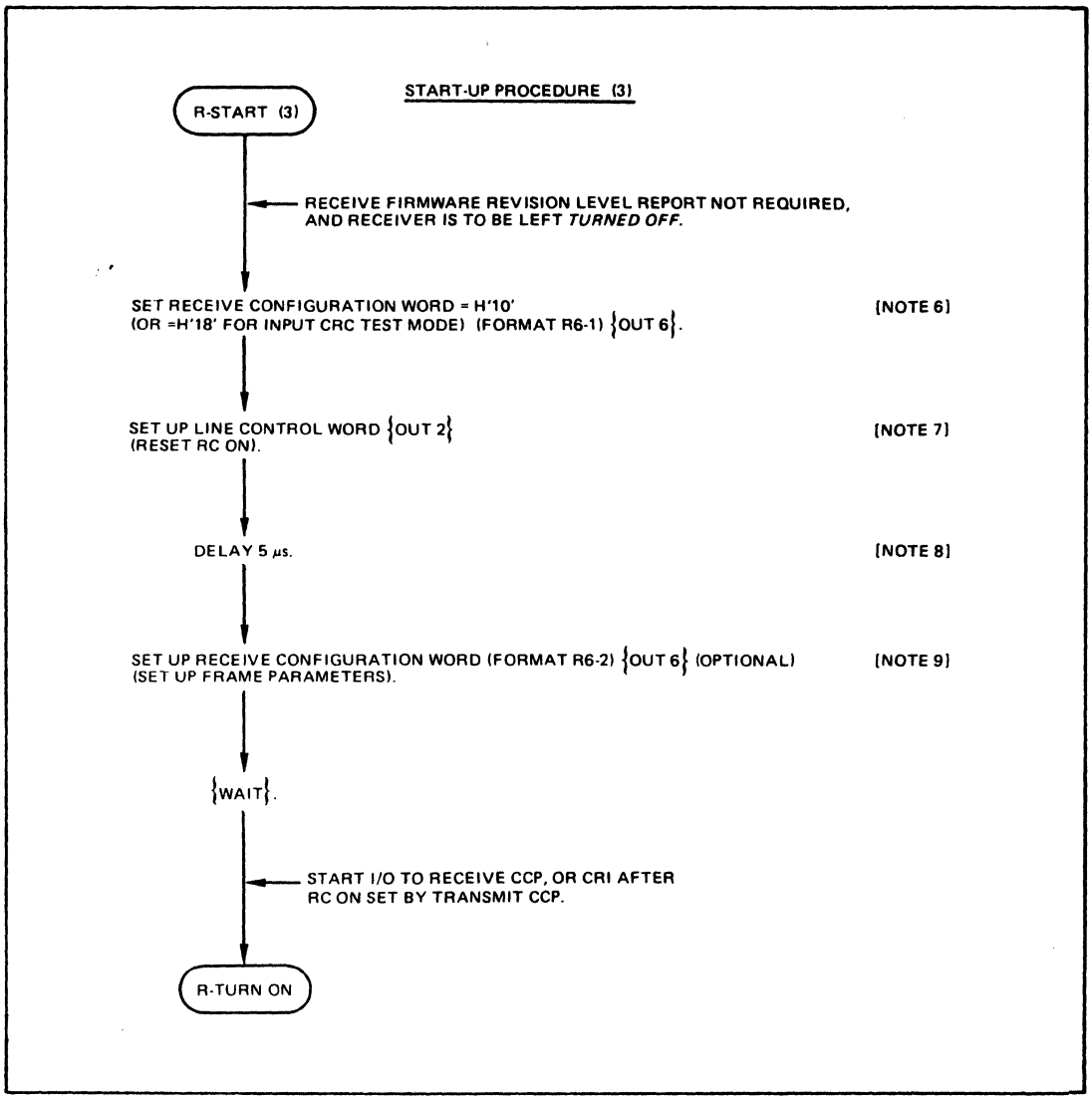


Figure H-20 (cont). Receive Flowchart

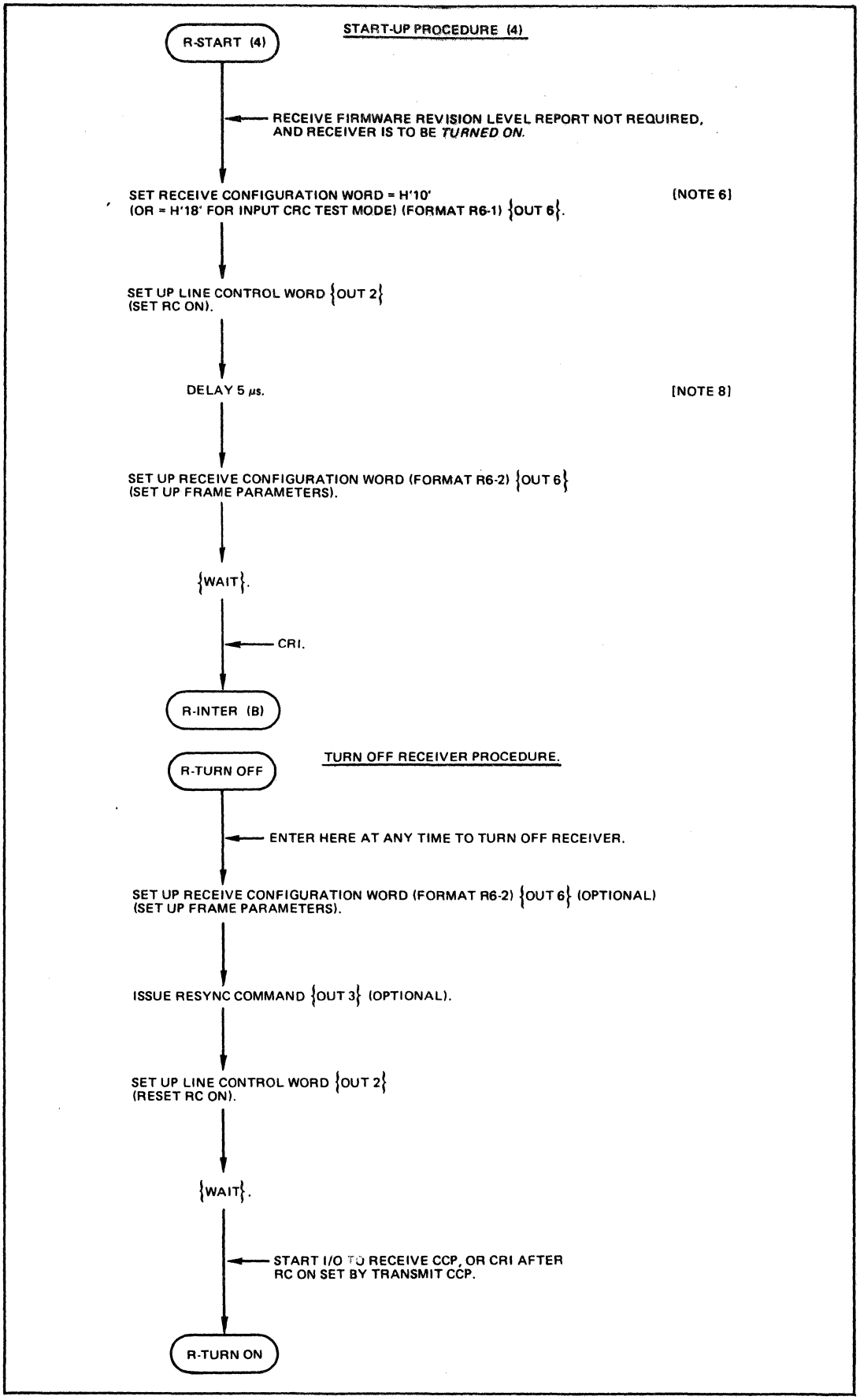


Figure H-20 (cont). Receive Flowchart

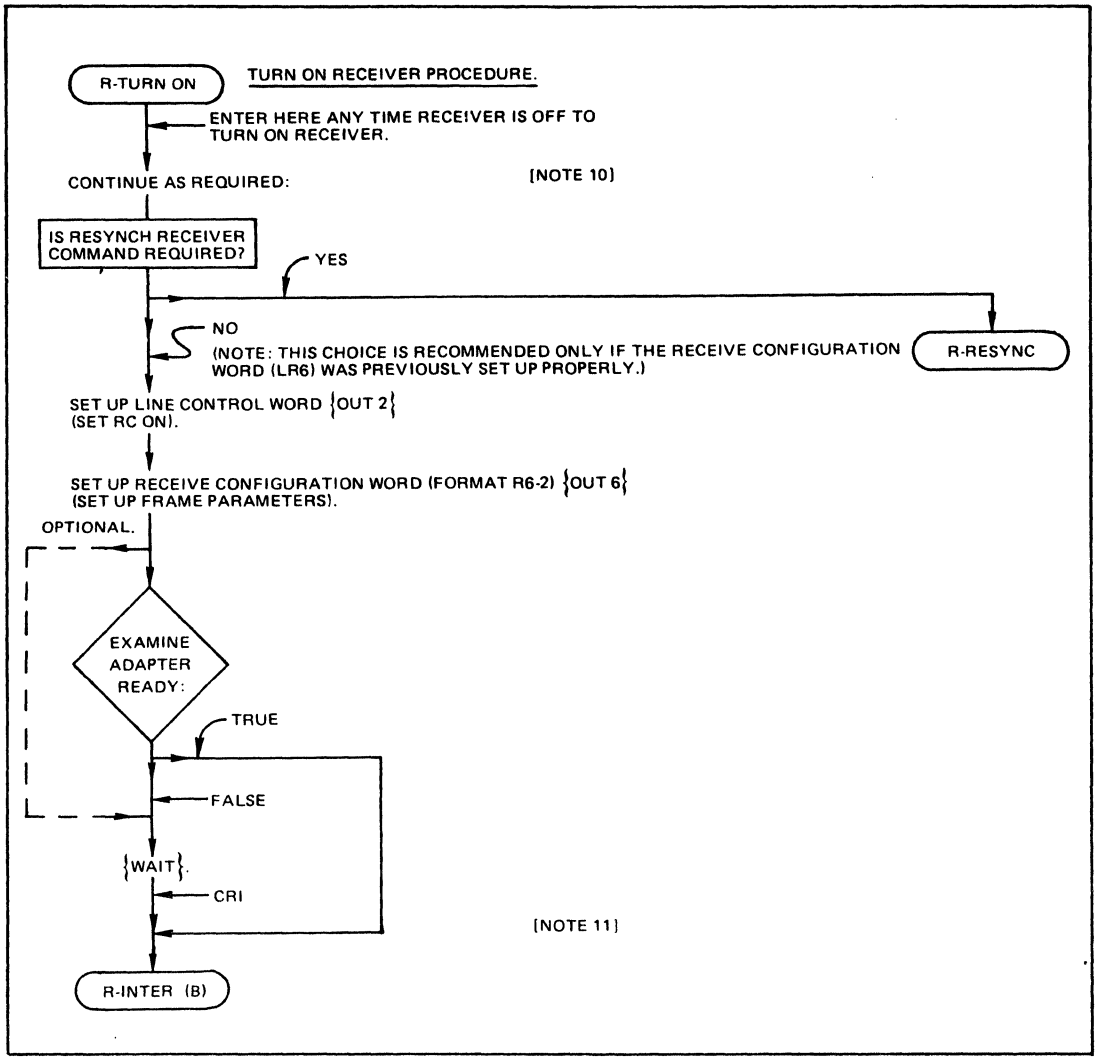


Figure H-20 (cont). Receive Flowchart

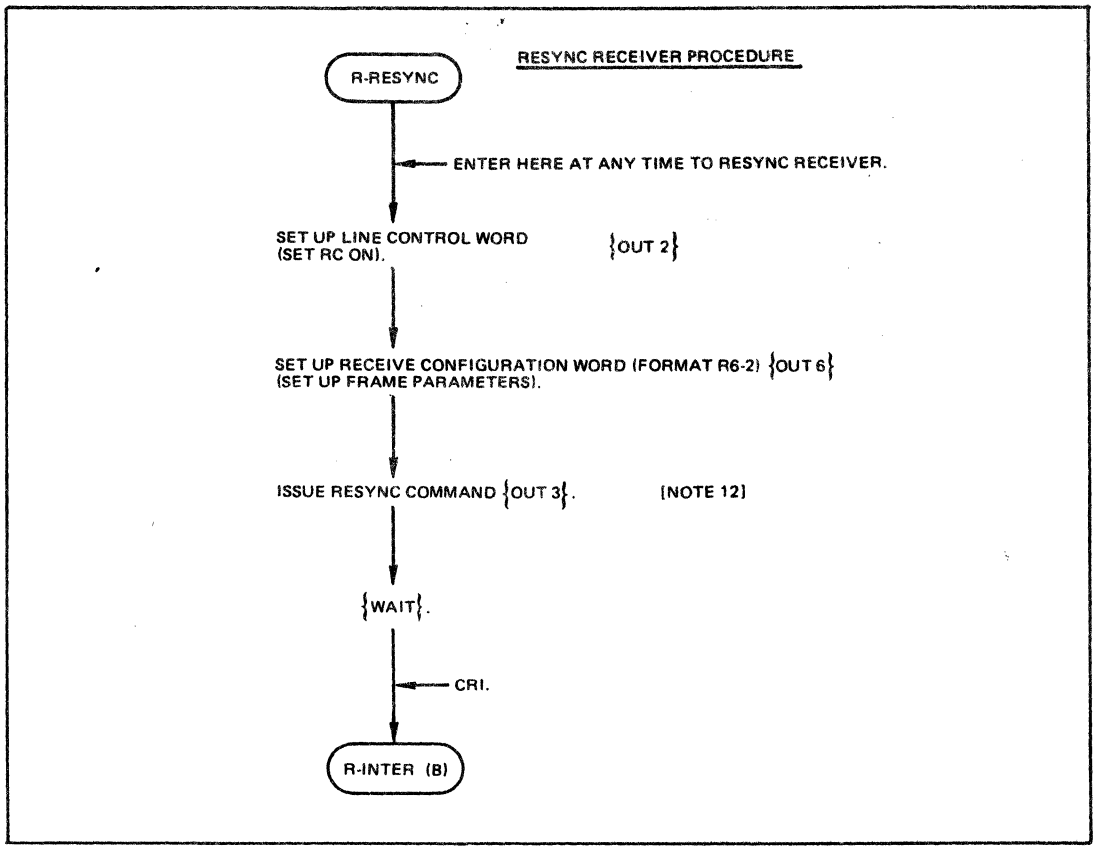


Figure H-20 (cont). Receive Flowchart

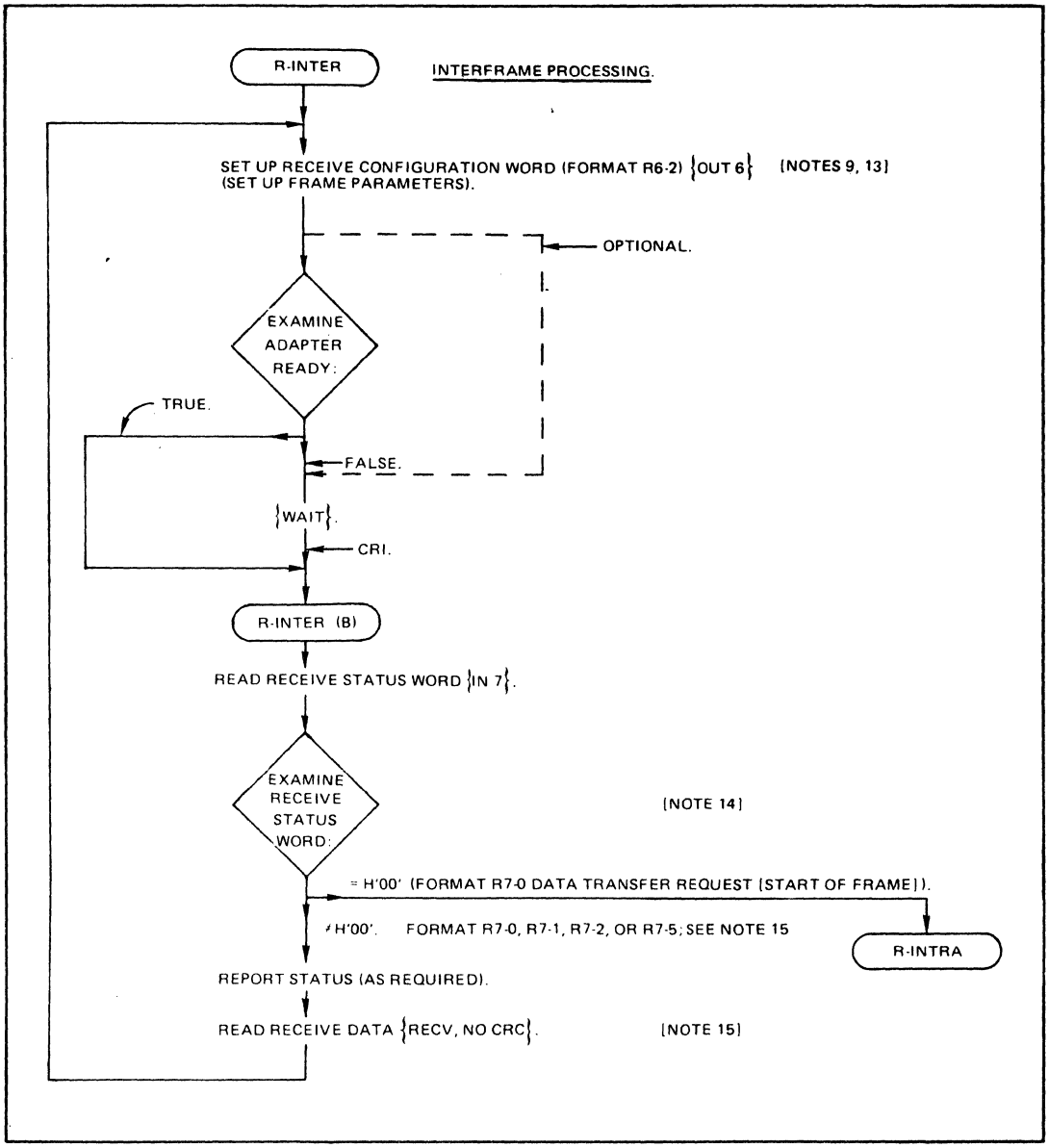


Figure H-20 (cont). Receive Flowchart

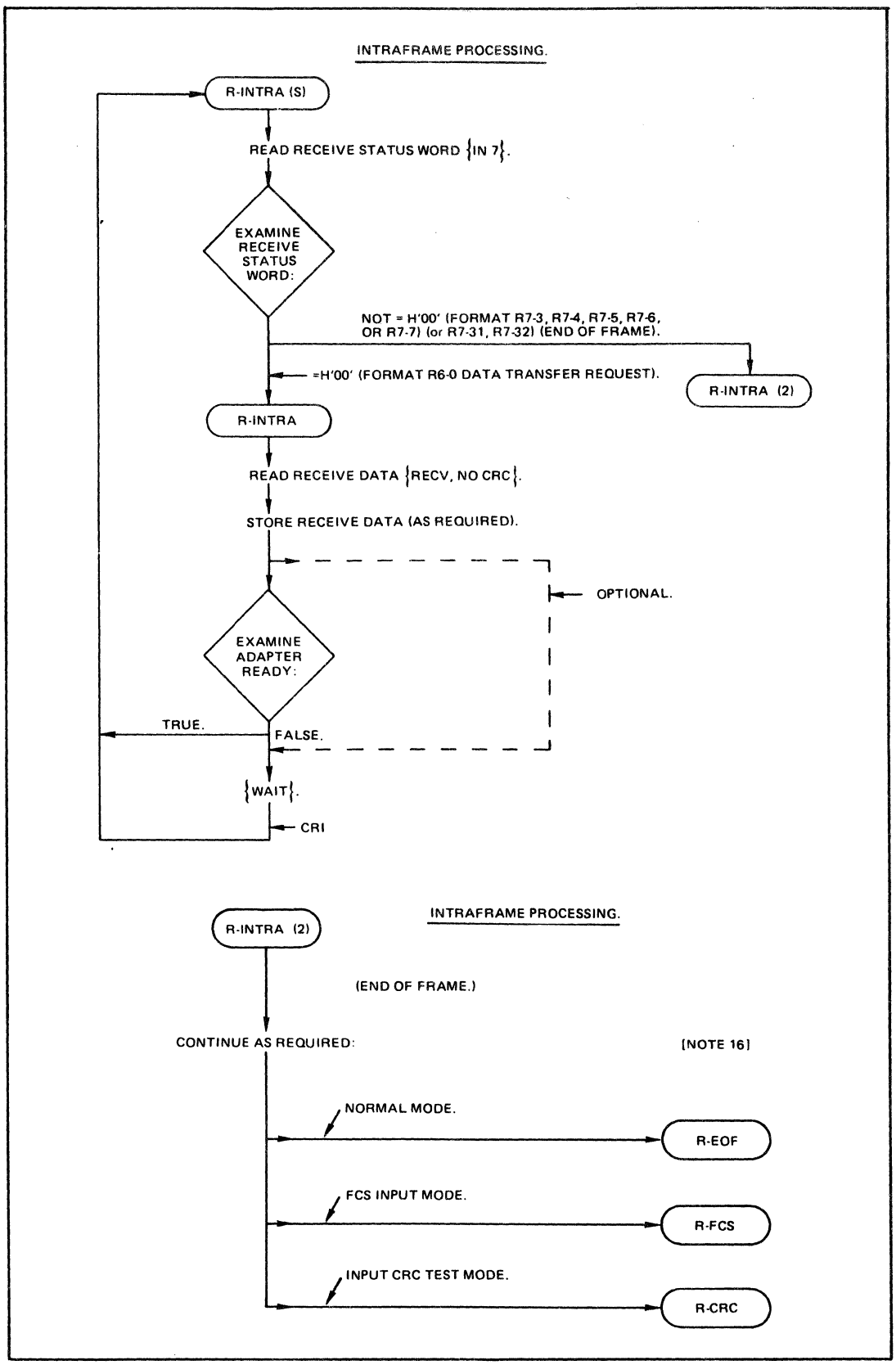


Figure H-20 (cont). Receive Flowchart

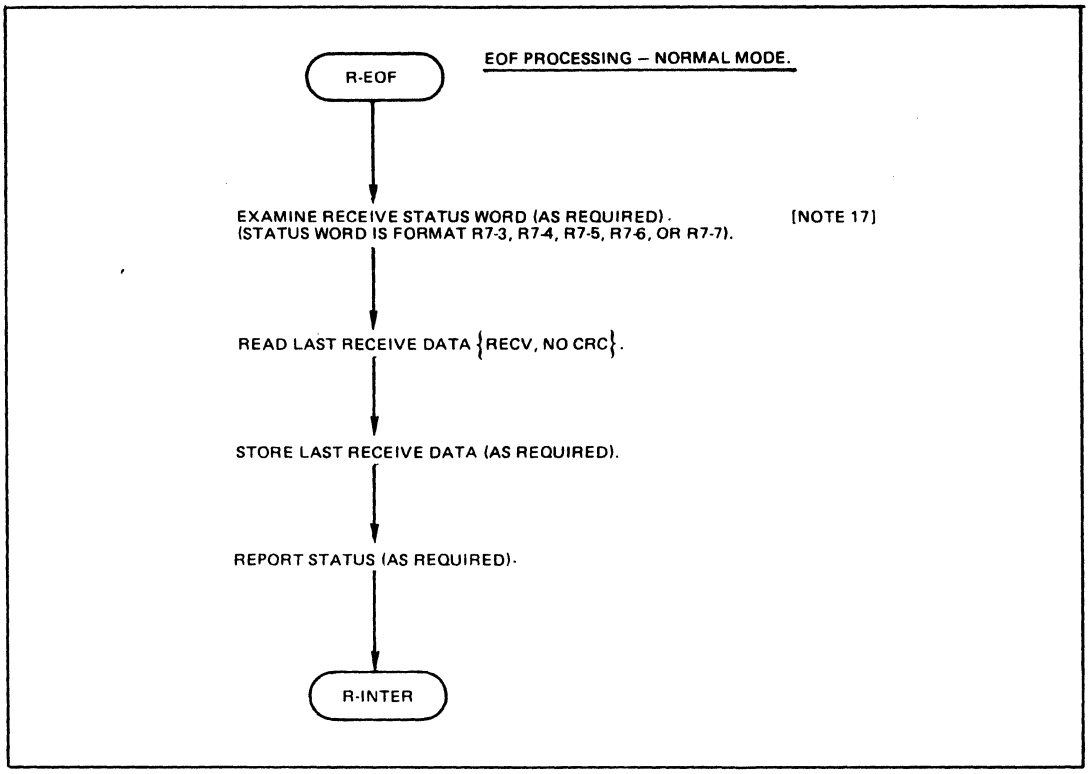


Figure H-20 (cont). Receive Flowchart

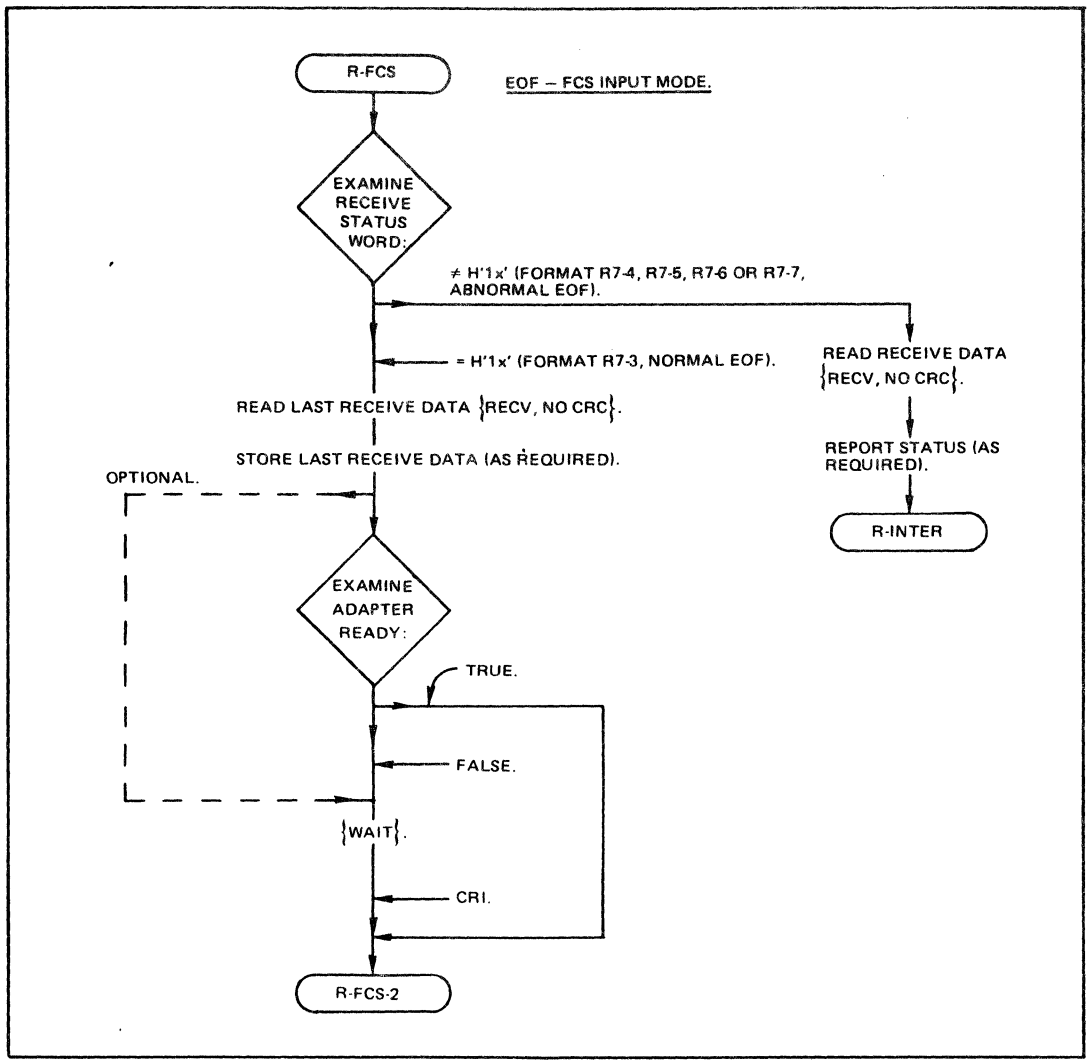


Figure H-20 (cont). Receive Flowchart

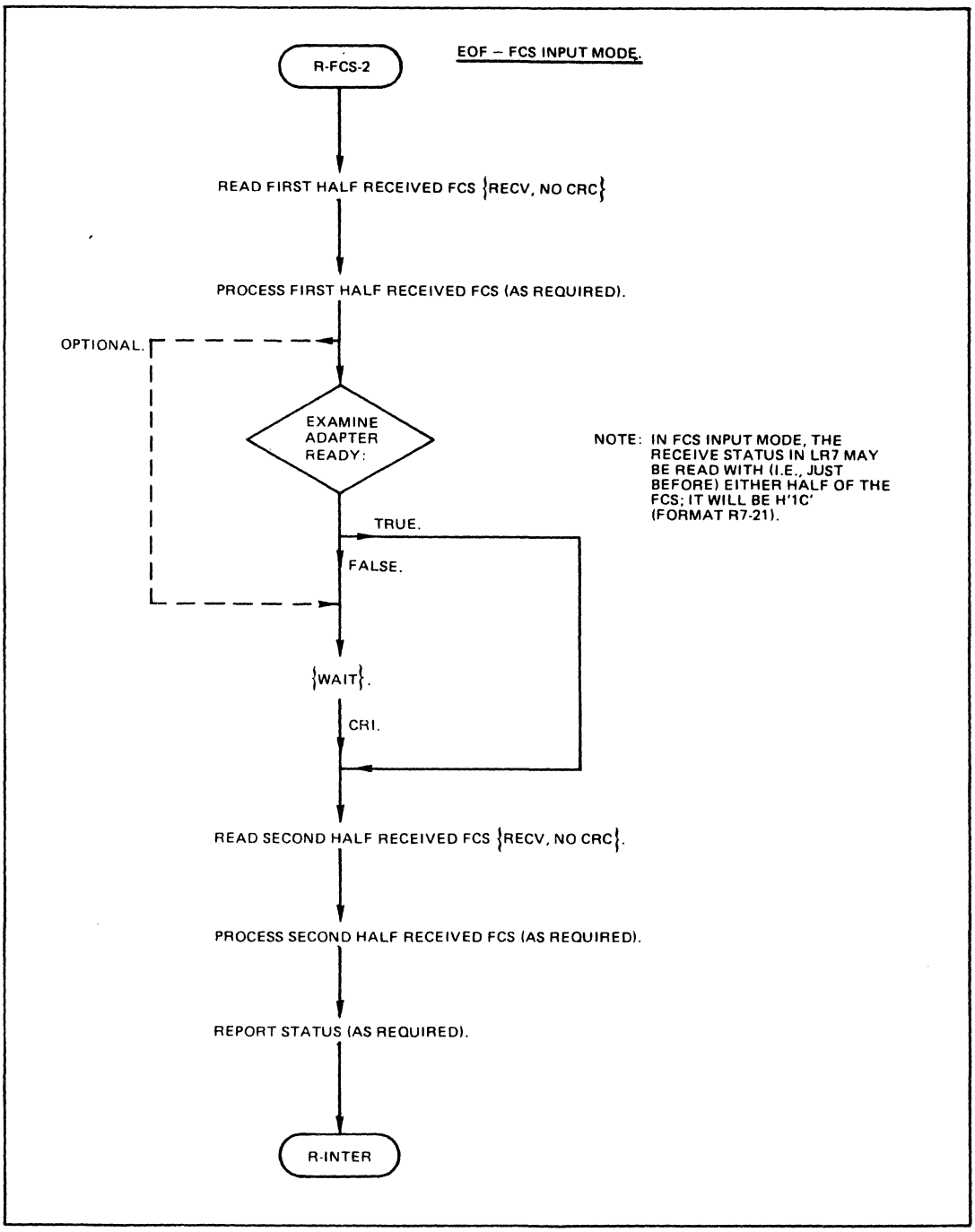


Figure H-20 (cont). Receive Flowchart

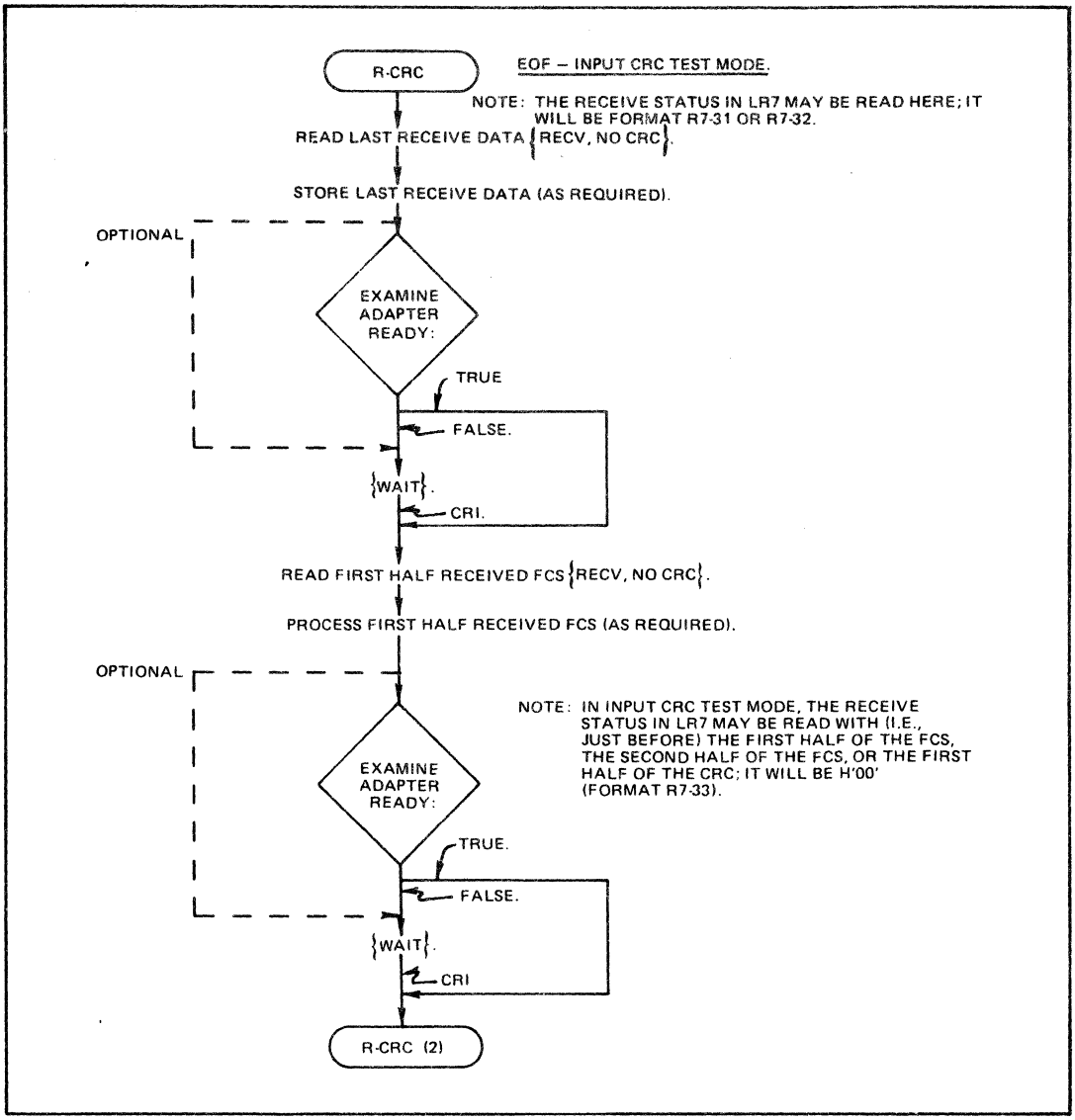


Figure H-20 (cont). Receive Flowchart

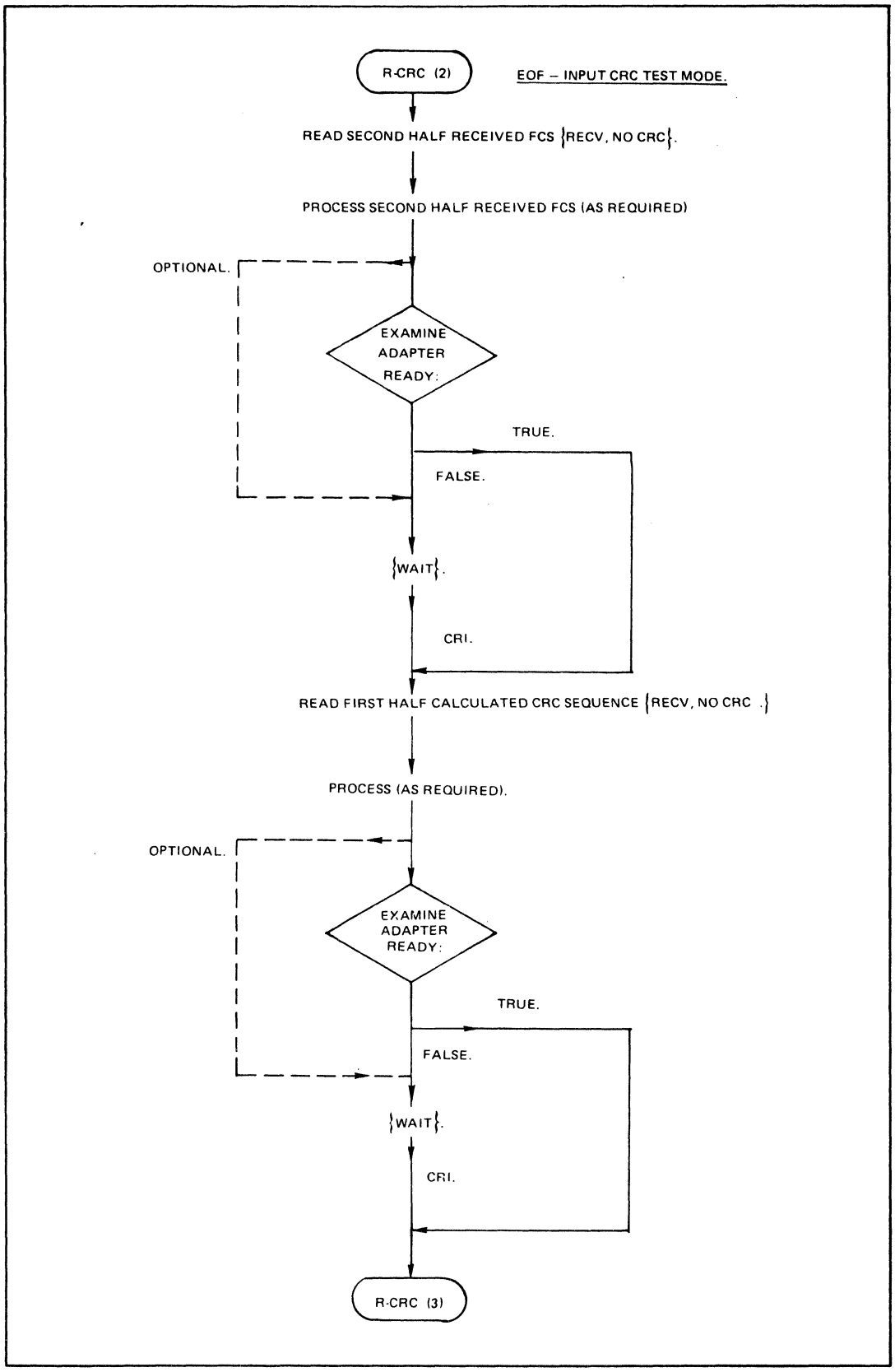
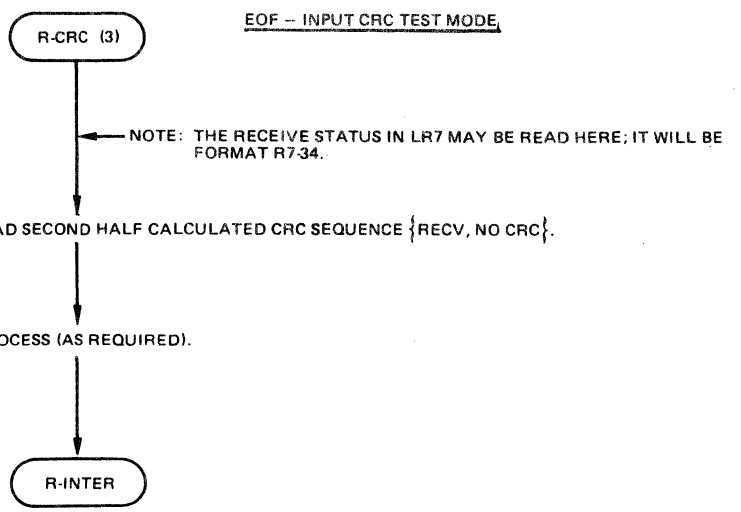


Figure H-20 (cont). Receive Flowchart



NOTES:

1. EACH OF THE FOLLOWING EVENTS CAUSES THE MLCP TO ISSUE A "MASTER CLEAR" TO THE COMMUNICATIONS-PAC:
   - o THE COMPUTER IS POWERED UP
   - o THE CONTROL PANEL CLR BUTTON IS DEPRESSED (WHEN IN STOP STATE); OR
   - o AN IO (OUTPUT MLCP CONTROL) INSTRUCTION WITH BIT 0 = 1 IS ISSUED TO THE MLCP
2. AFTER EVERY MASTER CLEAR TO THE COMMUNICATIONS-PAC, WHICH ACTION CLEARS RECEIVE LR6 TO H'00', THE RECEIVE FIRMWARE CONTINUALLY EXAMINES RECEIVE LR6 FOR A NON-ZERO VALUE. WHEN A NON-ZERO VALUE IS DETECTED, IT IS ASSUMED THAT THE REGISTER IS IN THE INITIALIZATION FORMAT, AND THE PERTINENT BITS ARE STORED FOR FUTURE USE. THUS, NO DATA SHOULD BE WRITTEN INTO RECEIVE LR6 AFTER A MASTER CLEAR UNLESS THE DATA IS THE INITIALIZATION WORD. THIS MEANS, ALSO, THAT NO *OTHER* CCP SHOULD WRITE INTO RECEIVE LR6.
3. H'xx' INDICATES A HEXADECIMAL VALUE OF xx.
4. RECEIVE CHANNEL REQUEST INTERRUPTS (CRI's) ARE GENERATED BY THE COMMUNICATIONS-PAC ONLY WHEN *BOTH* OF THE FOLLOWING CONDITIONS ARE TRUE:
   - o RC ON (IN LR2) IS SET; AND
   - o DATA AND STATUS (OR JUST STATUS) IS IN THE FIFO BUFFER CAUSING RECEIVE "ADAPTER READY" TO GO TRUE.
5. THE STATUS IN LR7 WHEN THE FIRMWARE REVISION LEVEL IS READ IS H'FD'.
6. FOR HMLC, SET = H'90' (OR –H'98' FOR INPUT CRC TEST MODE).
7. IT IS NECESSARY TO OUTPUT TO LR2 ONLY WHEN ITS CONTENTS REQUIRE CHANGING.
8. THIS DELAY IS REQUIRED TO INSURE THAT LR6 IS NOT CHANGED BEFORE THE COMMUNICATIONS-PAC HAS HAD TIME TO READ THE PREVIOUS CONTENTS. IF THE DELAY HAS ALREADY BEEN PROVIDED BY OTHER PROCESSING (E.G., MLCP INSTRUCTIONS), OR IF LR6 IS NOT GOING TO BE CHANGED, NO SPECIAL DELAY IS REQUIRED.
9. IT IS NECESSARY TO OUTPUT TO LR6 ONLY WHEN ITS CONTENTS REQUIRE CHANGING.
10. A START I/O (OUTPUT CHANNEL CONTROL INSTRUCTION, FUNCTION CODE 05, WITH BIT 1 SET) SHOULD BE ISSUED TO A COMMUNICATIONS-PAC WHICH ALREADY HAS RC ON SET FOR ONLY THE FOLLOWING REASONS:
    - o TO RESET RC ON; OR
    - o TO RESYNC THE RECEIVER.
11. IF THE RECEIVER WAS TURNED OFF IN THE MIDDLE OF A FRAME AND WAS NOT RESYNCHRONIZED, GO TO R-INTRA(S) INSTEAD OF R-INTER(B).
12. THE RECEIVER MAY BE RESYNCHRONIZED BY THE RECEIVE CCP BY MEANS OF THE OUT 3 COMMAND. (THIS IS THE ONLY WAY FROM THE RECEIVE CCP.)
    THE RECEIVER MAY BE RESYNCHRONIZED BY THE TRANSMIT CCP IN EITHER OF TWO WAYS: 1) BY THE OUT 3 COMMAND; OR 2) BY TRR IN TRANSMIT LR7 AT THE END OF FRAME. FOR THIS SECOND CASE, THE RESYNCHRONIZATION IS PERFORMED WHEN THE CLOSING FLAG (OR ABORT IN THE CASE OF A USER ABORTED FRAME) IS LOADED INTO THE TRANSMIT SHIFT REGISTER; EXCEPT WHEN UNDERRUN OCCURS IN WHICH CASE THE RESYNCHRONIZATION IS ISSUED WHEN UNDERRUN IS FINALLY REPORTED.
13. NOTE THAT CARE MUST BE TAKEN IN CHANGING RECEIVE LR6 BETWEEN FRAMES BECAUSE THE COMMUNICATIONS-PAC, WITH ITS FIFO BUFFER, MAY ALREADY BE PROCESSING ONE OR MORE FOLLOWING FRAMES.

Figure H-20 (cont). Receive Flowchart

14. THE FOLLOWING STATUS VALUES ARE POSSIBLE BETWEEN FRAMES:

VALUE (HEX)	FORMAT ID	DESCRIPTION
00	R7-0	DATA TRANSFER REQUEST (START OF FRAME)
80	R7-1	IDLE LINK STATE
40	R7-2	MISSED FRAMES (A SECOND (OR MORE) FRAME ENDED BEFORE STATUS FOR PREVIOUS FRAME WAS COMPLETED)

NOTE: FORMATS R7-1 AND R7-2 MAY OCCUR SIMULTANEOUSLY.

50	R7-5	OVERRUN (A SECOND FRAME STARTED BEFORE STATUS FOR PREVIOUS FRAME WAS COMPLETED, BUT STATUS WAS COMPLETED BEFORE SECOND FRAME ENDED)

15. IN CASES WHERE THE RECEIVE DATA IS MEANINGLESS, IT IS STILL NECESSARY TO EXECUTE THE RECV (OR IN 1) INSTRUCTION IN ORDER TO CAUSE THE FIFO STACK IN THE COMMUNICATIONS-PAC TO ADVANCE.
16. MODE SELECTION CONTROL IS SUMMARIZED BELOW:
    - o INPUT CRC TEST MODE IS IN EFFECT WHEN RICRCTM IN RECEIVE LR6 IS SET AT INITIALIZATION.
    - o FCS INPUT MODE IS IN EFFECT WHEN RICRCTM IS RESET AND RFCSIE IN LR6 (FRAME FORMAT) IS SET.
    - o NORMAL MODE IS WHEN NEITHER OF THE ABOVE MODES IS SELECTED.
17. NOTE THAT OVERRUN STATUS REPORTING IS *NOT* ACCOMPLISHED BY THE RECV COMMAND.

Figure H-20 (cont). Receive Flowchart

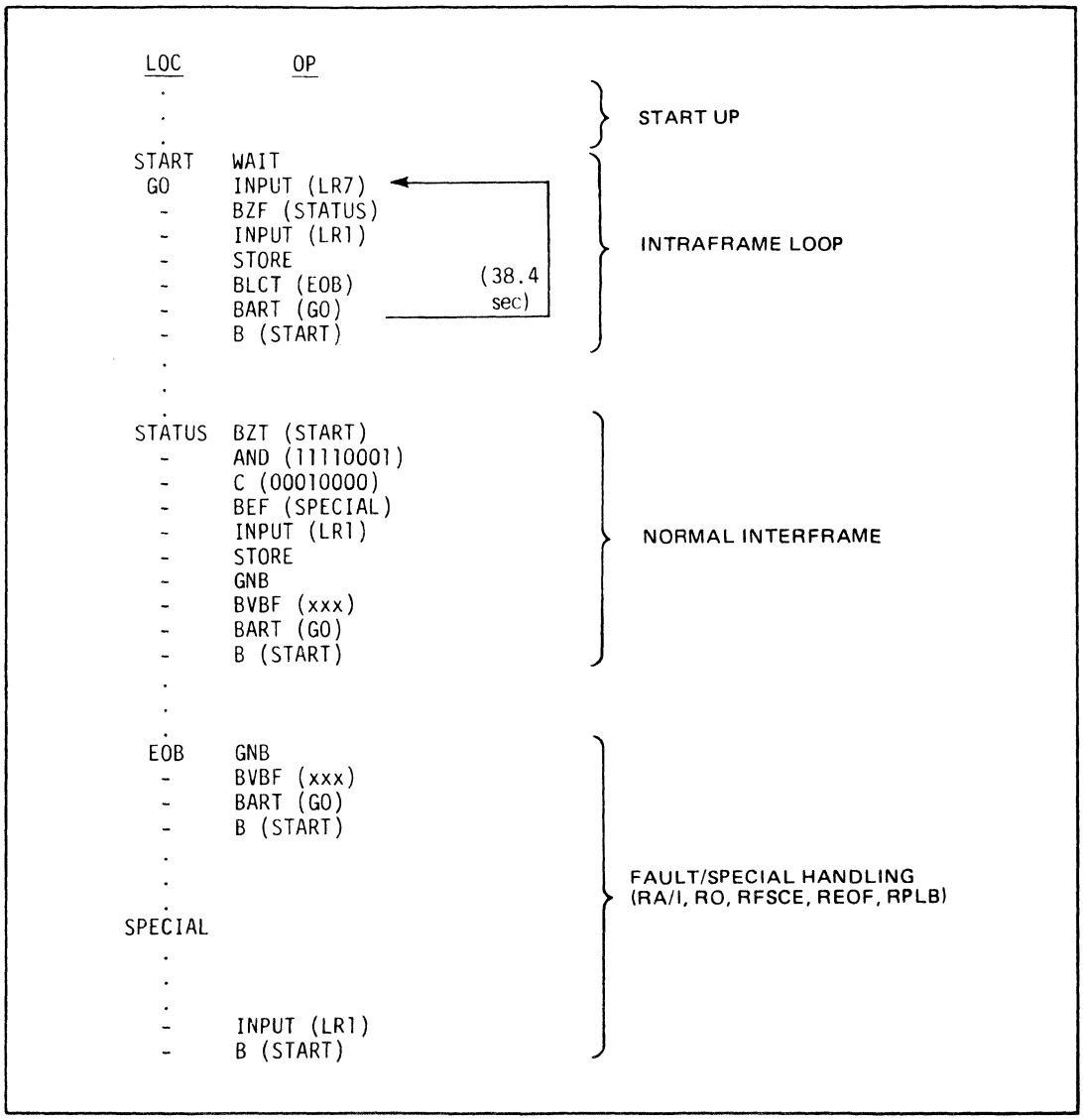


Figure H-21. Receive Loop

PHYSICAL INTERFACE TO DATA COMMUNICATIONS EQUIPMENT AND DATA TERMINAL EQUIPMENT

The Synchronous Broadband HDLC Communications-Pac provides a physical interface for the communications line. This interface is designed to permit connection of data communications equipment or data terminal equipment compatible with current mode interface (for Bell System 301 or equivalent, 303 or equivalent), a standard CCITT-V35 interface (Bell DDS with DSU at 56 kbs), or a MIL188-C interface.

The Communications-Pac may be used in the normal manner where transmit and receive data clocking (signal element timing) is provided by the DCE (or equivalent), or it may be used in a direct connect mode where system clocking is provided by the MLCP via the Communications-Pac. In direct connect mode, data terminal equipment (DTE) may be connected directly to the Communications-Pac without the use of any intermediary DCEs and communications network or modem bypass equipment. In this mode, the Communications-Pac hardware operates in the same manner as in normal mode except that the MLCP-provided clock is enabled to specific pins of the interface cable.

The clock (or clocks) must now be routed to the appropriate pins on the DTE as well as back to the Communications-Pac. This requires an additional special direct connect cable or interface cable. Specific information regarding the pin where the direct connect clock(s) is (are) provided is given below. Direct connect mode is selected in accordance with the Direct Connect bit of line register 2.

The Synchronous Broadband HDLC Communications-Pac's physical interface comprises 15 signals plus ground per line. See Table H-7 for the interface supporting the Bell 301 and 303 and/or equivalent; Table H-8 for the CCITT-V35 interface (supporting Bell DDS with DSU at 56 kbs), and Table H-9 for the MIL188-C interface.

DCM9112

The DCM9112 is provided with a 15 signal plus ground interface for attachment to Bell 301B/303 data sets as well as functionally similar and electrically compatible DCE. In direct connect mode, two synchronized signal element timing signals are provided by the Communications-Pac to the center conductor and outer conductor of External Serial Clock Transmit (pin H). These signals must be wrapped around by a special cable (or by the attached DCE or DTE) to send the transmit and receive signal element timing signals to both the attached DCE or DTE and back to the Communications-Pac. Refer to Table H-7 for the DCM9112 physical interface.

TABLE H-7. BELL 301, 303-COMPATIBLE INTERFACE

Bell 303 Pin	Function	Bell 301B Pin	To/From DCE
C	Clear to send	C	F
D	Send request	D	T
E	Send data	E	T
F (Note 1)	Data set ready	–	F
F (Note 2)	Ring indicator	–	F
–	Interlock	F	F
H	External serial clock transmit	H	T
J	Serial clock transmit	J	F
K	Receive data	K	F
L	Serial clock receive	L	F
M (Note 1)	AGC lock	–	F
M (Note 2)	Data terminal ready	–	T
–	Carrier On/Off	M	F

NOTES: 1. Center conductor
2. Outer conductor

DCM9113

The DCM9113 Communications-Pac is provided with a 16 signal plus ground interface for attachment to CCITT – V35 compatible DCE and Bell DDS using data service units at 56 KBS. In direct connect mode, a signal element timing signal (data clock) is provided by the Communications-Pac pins U and W. This signal must be "wrapped around" by a special cable (or by the attached DCE or DTE) to send the transmit and receive clocks to both the attached DCE or DTE and back to the Communications-Pac. Refer to Table H-8.

TABLE H-8. CCITT-V35 INTERFACE (INCLUDING BELL DDS AT 56 KBS)

Bell DDS DSU Pin	Function	CCITT V35 Pin	CCITT Circuit No.	Direction
A	Protective ground or earth	A	101	common
B	Common return (Signal Ground)	B	102	common
C	Request to send	C	105	from DTE
D	Ready for sending (Clear to Send)	D	106	to DTE
E	Data set ready	E	107	to DTE
F	Data channel received line signal detector	F	109	to DTE
–	Connect data set to line	–	108/1	from DTE
–	Data terminal ready	H	108/2	from DTE
–	Calling indicator (Ring)	J	125	to DTE
–	–	K (Note 1)	–	–
–	–	L (Note 1)	–	–
–	–	M (Note 1)	–	–
–	–	N (Note 1)	–	–
R	Received data A-wire	R	104	to DTE
T	Received data B-wire	T	104	to DTE
V	Receiver signal element timing A-wire	V	115	to DTE
X	Receiver signal element timing B-wire	X	115	to DTE
Y	Transmitter signal element timing A-wire	Y	114 (Note 2)	to DTE
a	Transmitter signal element timing B-wire	AA	114 (Note 2	to DTE
P	Transmitted data A-wire	P	103	from DTE
S	Transmitted data B-wire	S	103	from DTE
–	Direct connect clock A-wire	U	113	from DTE
–	–	Z (Note 1)	–	–
–	Direct connect clock B-wire	W	113	from DTE
–	–	BB (Note 1)	–	–
–	–	CC (Note 1)	–	–
–	–	DD (Note 1)	–	–
–	–	EE (Note 1)	–	–
–	–	FF (Note 1)	–	–
–	–	HH (Note 3)	–	–
–	–	JJ (Note 3)	–	–
–	–	KK (Note 3)	–	–
–	–	LL (Note 3)	–	–
m (Note 4)	–	MM (Note 1)	–	–
–	–	NN (Note 1)	–	–

NOTES:

1. Pin number reserved for future International Standard and should not be used for domestic use. This pin is currently not supported.
2. When the transmit clock wraparound is enabled, CCITT circuit 114 will be wrapped around to CCITT circuit 113.
3. Pin number permanently reserved for (domestic) U.S. use. This pin is currently not supported.
4. Reserved for DSU testing.

DCM9121

Refer to Table H-9 for the connections for the MIL188-C interface. In direct connect mode, two synchronized signal element timing signals are provided by the Communications-Pac in place of New Synch (pin 14) and Data Signalling Rate Selector (pin 23). These signals must be "wrapped around" by a special cable (or by the attached DCE or DTE) to send the transmit and receive signal element timing signals to both the attached DCE or DTE and back to the Communications-Pac.

Note that the value of the slope control capacitor on the Transmit Data circuit is determined by the baud rate of each particular application. (This also applies to New Sync and Data Signalling Rate Selector also when operating in direct connect mode.)

A hexadecimal rotary switch, mounted on the Communications-Pac, must be set in accordance with the type of MIL188-C interface being used. For a MIL188-C application where a MARK on the transmit and receive data lines is a positive polarity, this switch must be set to position "D." For applications where the MARK on the data lines is a negative polarity, the switch must be set to position "2". Any other positions of this switch are not allowed.

TABLE H-9. MIL188-C INTERFACE (DCM9121)

Pin Number	Function	EIA	To/From DCE
2	Transmitted Data	BA	T
3	Received Data	BB	F
4	Request to Send	CA	T
5	Clear to Send	CB	F
6	Data Set Ready	CC	F
7	Signal Ground	AB	–
8	Received Line Signal Detector	CF	F
14	New Sync	–	T
15	Transmitter Signal Element Timing	DB	F
17	Receive Signal Element Timing	DD	F
20	Data Terminal Ready	CD	T
22	Ring Indicator	CE	F
23	Data Signalling Rate Selector	CH	T

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