Section 1
System Summary

This section provides a hardware overview of the Level 6 minicomputer family. Described are the various Level 6 models, system hardware elements, and packaging options.

MODELS

The Level 6 minicomputer family currently consists of four standard models: 23, 33, 43, and 53 – and two commercial models: 47 and 57. Figure 1-1 shows the field expansion and performance path for Level 6. A detailed comparison of the six models is given in Table 1-1.

Model 23

Model 23 is the smallest, low-cost, entry-level member of the Level 6 minicomputer family. It is ideally suited to serve as either a small online system or as a multifunction terminal communicating with other Level 6 systems or with larger Honeywell or other vendors' data processing systems. To keep the cost of the system as low as possible, Honeywell has modified the standard Level 6 system architecture for the Model 23; as a result, it is not directly field-upgradable.

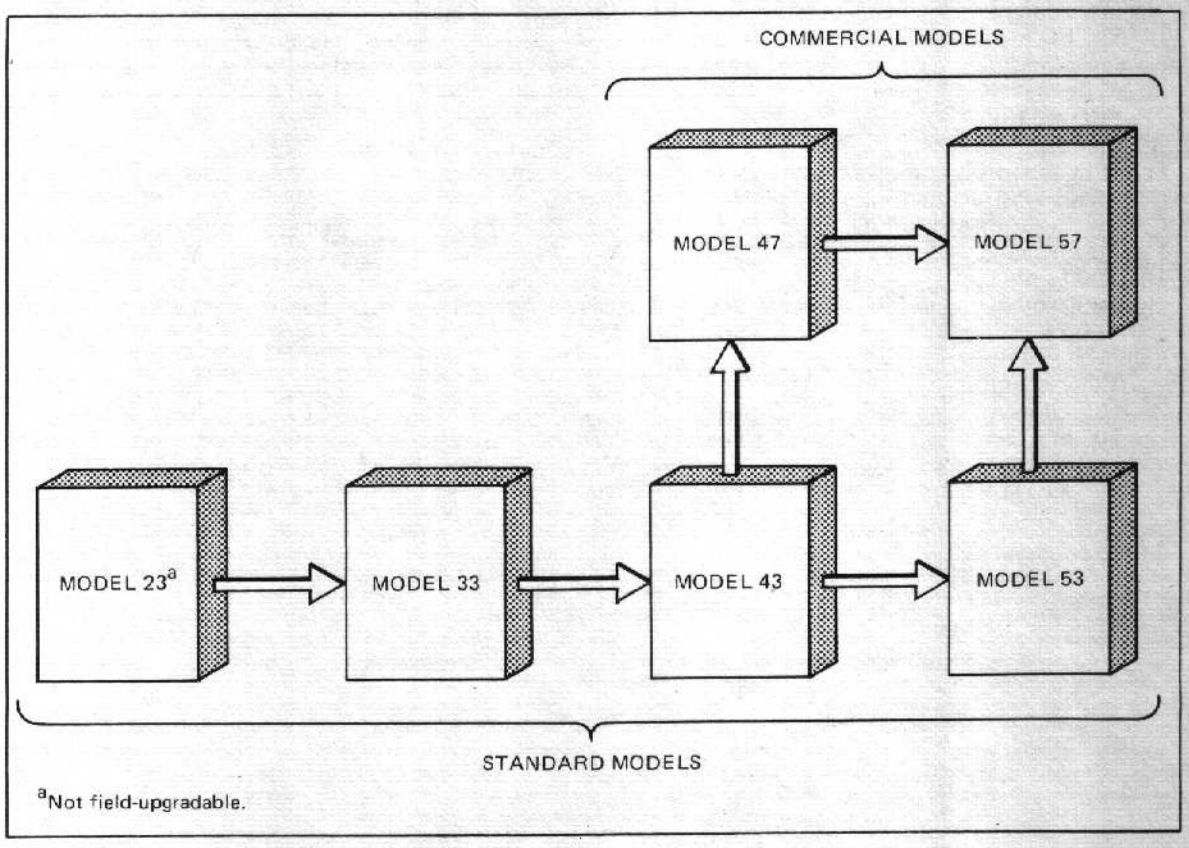


Figure 1-1. Level 6 Model Growth and Performance Path

TABLE 1-1. LEVEL 6 MODEL COMPARISON

CHARACTERISTICS	MODELS 23	33	43	47	53	57
Slots on bus chassis	7/11	5/10	5/10	10	10	10
Maximum bus slot expansion	11	23	23	23	23	23
Megabus	No	Yes				
Firmware driven processor	Standard					
Control panel	Basic or Full				Full	Full
Power supply	Standard					
Hardware multiply/divide	Standard					
Real-time clock	Standard					
ROM bootstrap loader	Standard					
Watchdog timer	Std	Opt	Std	Std	Std	Std
Power failure interrupt	Standard					
64 priority levels	Standard					
Maximum memory size (words)	64K	64K	1M	1M	1M	1M
Registers	18	18	26	26	26	26
Standard instruction set	108	108	124	154	124	154
Scientific instruction set	Sim	Sim	Opt	Opt	Opt	Opt
Commercial instruction set	Sim	Sim	Sim	Std	Sim	Std
Addressing modes	16	17	17	17	17	17
Multiple accumulators	Yes	Yes	Yes	Yes	Yes	Yes
Indexing	Yes	Yes	Yes	Yes	Yes	Yes
Hardware stack/queue	No	No	Yes	Yes	Yes	Yes
Double-fetch memory technique	No	No	Yes	Yes	Yes	Yes
Cache memory	No	No	No	No	Std	Std
Memory management unit	No	No	Opt	Opt	Std	Std
DMA as I/O method	Comm	Standard				
Automatic logic tests	Standard					
Firmware for task dispatching and I/O control	Standard					
Additional plug-in memory	Optional					
Scientific instruction processor	No	No	Opt	Opt	Opt	Opt
Commercial instruction processor	No	No	No	Std	No	Std
General purpose DMA interface	No	Opt	Opt	Opt	Opt	Opt
Field upgradability	No	Yes	Yes	Yes	Yes	–
MOD 200 software	Yes	Yes	Yes	Yes	Yes	Yes
MOD 400 software	Yes	Yes	Yes	Yes	Yes	Yes
MOD 600 software	No	No	Yes	Yes	Yes	Yes
Cabinetry options:						
– Tabletop unit	No	Yes	Yes	No	No	No
– 60" cabinet	No	Yes	Yes	Yes	Yes	Yes
– 30" minirack	Yes	Yes	Yes	Yes	Yes	Yes
– Office furniture package	Yes	Yes	Yes	Yes	Yes	Yes
– 60" RETMA cabinet	Yes	Yes	Yes	Yes	Yes	Yes

Legend:

Std	–	Standard
Opt	–	Optional
Sim	–	Simulated
Comm	–	Communications only

Model 23 utilizes a unique, low-cost, synchronous bus that can accommodate up to ten memory and I/O adapters, viz., console, printer, diskette, and communication adapters (see Figure 1-2). Maximum memory is 65,536 words and is completely contained on a single board. Model 23 is offered either in a rackmountable version or, for end-user convenience, in a prepackaged "minimount" version. The latter includes the processor, either 16K, 32K, or 64K words of memory, either 5 or 9 additional slots for I/O adapters, a basic or full control panel, and a power distribution unit, all packaged in a 30-inch minirack. The office packaging option allows housing of Model 23 in a desk-style configuration.

Features

- o Performance level approximately 60 percent of Model 33
- o Memory sizes from 16K to 64K words
- o Memory utilizes advanced 16K-chip technology
- o Real-time clock and watchdog timer standard
- o Same internal organization and instruction set as Model 33
- o 64 levels of priority
- o Up to ten memory and I/O adapters
- o Supports GCOS 6 MOD 200 and MOD 400 software

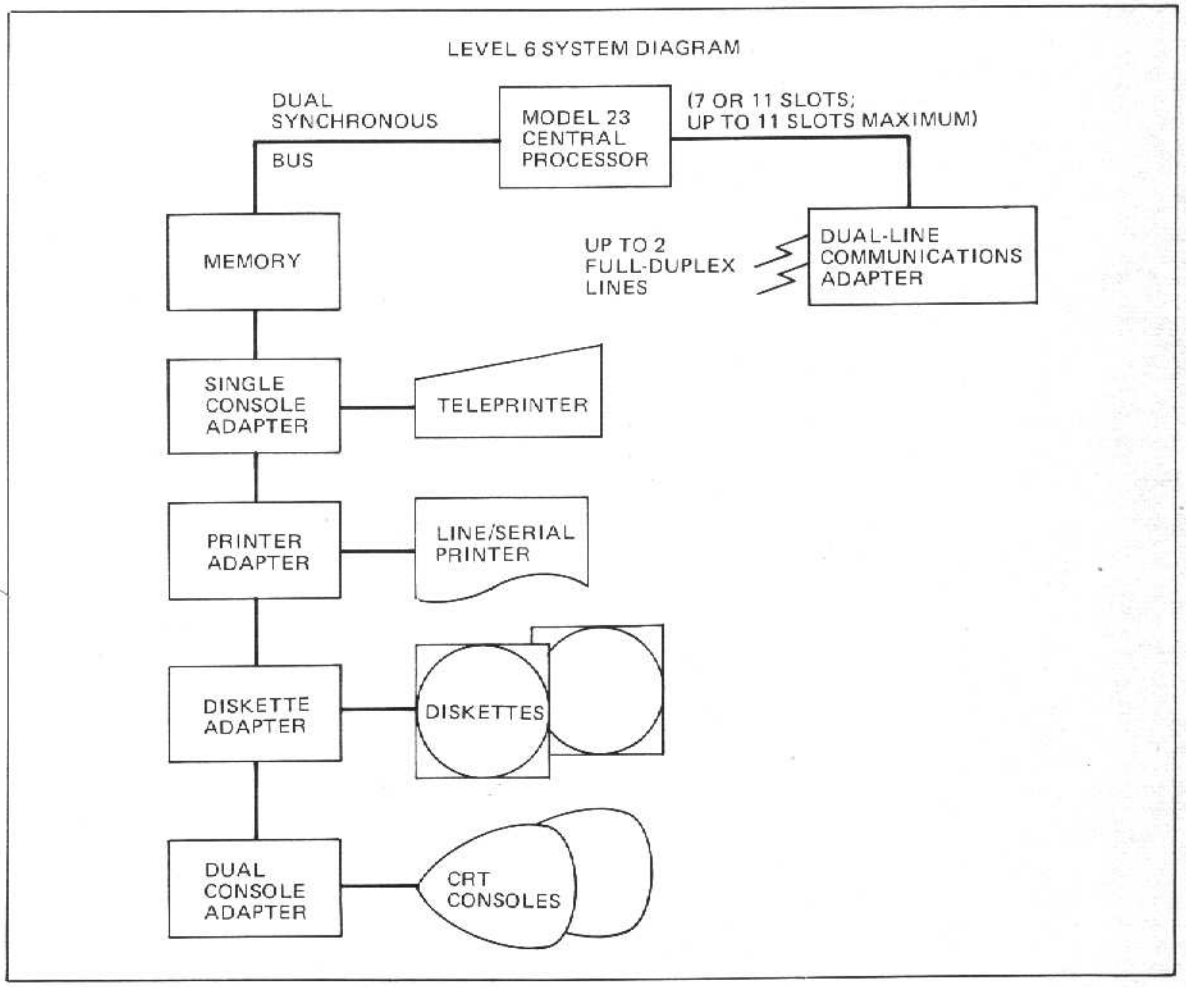


Figure 1-2. Model 23 Configuration

Model 33

Model 33 is the entry-level, upgradable alternative to Model 23. It features the same advanced asynchronous Megabus architecture as the higher performance Models 43, 47, 53, and 57, and supports the full range of Level 6 peripheral and communications options.

The Model 33 central processor is mounted in a five- or ten-slot Megabus chassis (both expandable to 23 slots) and includes a basic or full control panel, multiply/divide hardware, real-time clock, power supply, and ROM bootstrap loader. Maximum (single-fetch) memory is 65,536 words. Users may choose from a varied list of options, controllers, and peripheral devices for optimum configurability and economy (see Figure 1-3).

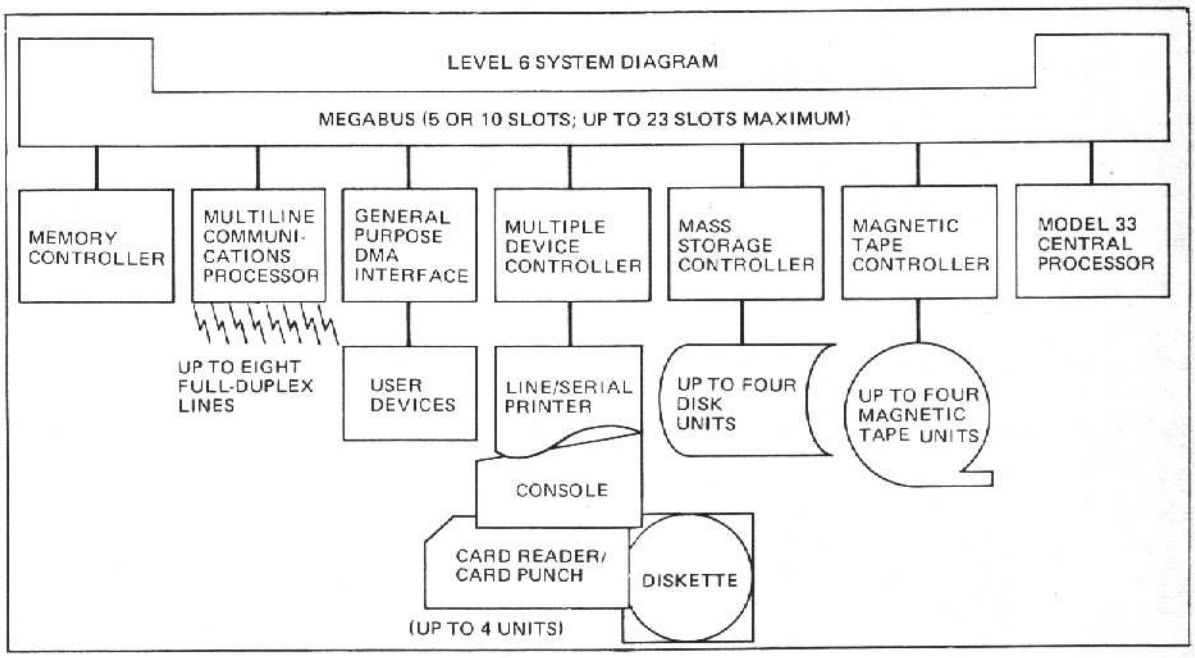


Figure 1-3. Model 33 Configuration

Features

- o Performance level approximately 40 percent higher than Model 23
- o Field upgradable to Model 43 or 53
- o Maximum memory size 64K words
- o Standard MOS, high-density MOS and core memory available
- o Superior peripheral and communications configurability compared to Model 23
- o Megabus permits interleaved transfers with a peak throughput rate of six megabytes and 300 nanosecond cycle time
- o Supports GCOS 6 MOD 200 and MOD 400 software.

Models 43 and 47

Models 43 and 47 are mid-range members in Honeywell's Level 6 family of minicomputers. They offer high levels of functionality and performance to help provide efficient communications and data processing capabilities and extensive system building possibilities.

Model 43 central processor is mounted in a five- or ten-slot Megabus chassis (both expandable to 23 slots) and includes a basic or full control panel, multiply/divide hardware, real-time clock, power supply, watchdog timer, and ROM bootstrap loader.

Model 47 central processor is mounted in a ten-slot Megabus chassis (expandable to 23 slots) and includes the above Model 43 hardware plus a Commercial Instruction Processor (CIP). The CIP is an additional hardware processor tailored to perform string operations that can significantly increase COBOL performance. It operates on a powerful set of 30 commercial instructions which include numeric, alphanumeric, edit, and branch instructions.

The CIP was designed to support, in hardware, the processing functions most often required by COBOL and RPG programs. It supports decimal arithmetic, character string manipulation, conversion between binary and decimal forms, and data editing. These functions are performed at speeds previously associated only with far more expensive systems, and with a degree of flexibility that minimizes software pre-processing or post-processing of CIP data.

The CIP and CP normally operate in parallel. First, the CP extracts an operation code and determines that a commercial instruction has been programmed. Then, it sends the operation code, data descriptions, and data addresses to the CIP over the Megabus. At that point, the CIP begins autonomous operation. The CP is free to proceed with the next instruction and if it is not a commercial instruction, it is executed and the CP continues. If the CP encounters another commercial instruction before CIP execution of the first one is over, it will wait for the CIP to become free and then initiate another Megabus dialog.

A system may have both a CIP and a Scientific Instruction Processor (SIP) and they may both operate simultaneously with the CP.

The Level 6 system architecture facilitates model configurability and upward compatibility, whether simply upgrading from a Model 43 to a Model 47 or 53, or from a Model 47 to a Model 57. With a maximum of one million words of directly addressable memory and a wide range of options, controllers, and peripheral devices (see Figure 1-4), the Models 43 and 47 may be the best mid-sized minicomputers on the market today.

Features

- o Faster logic than Model 33 (with "single-fetch" memory), resulting in 30 percent performance increase
- o Optional "double-fetch" memory capability, resulting in an additional 30 percent performance increase
- o 16-bit data and 20-bit address registers
- o COBOL performance level of Model 47 is approximately 4.1 times that of Model 43
- o Commercial Model 47 includes a commercial instruction processor
- o Field upgradable to Model 53 or 57
- o Direct addressing of up to 1 million words
- o Additional instructions compared with Model 33, including move, queue, and dequeue commands
- o Optional Memory Management Unit providing memory segmentation and MULTICS-like storage protection with four rings of read/write/execute access
- o Optional Scientific Instruction Processor (SIP) providing single- and double-precision hardware floating-point capability
- o Supports GCOS 6 MOD 200, 400, and 600 software

Models 53 and 57

Models 53 and 57 are the high-end, high-performance members of the Level 6 family offering the features and functionality of a full-size computer at a mini price. They are ideally suited for large jobs involving time sharing, transaction processing, and data base management all running simultaneously under the GCOS 6 operating system.

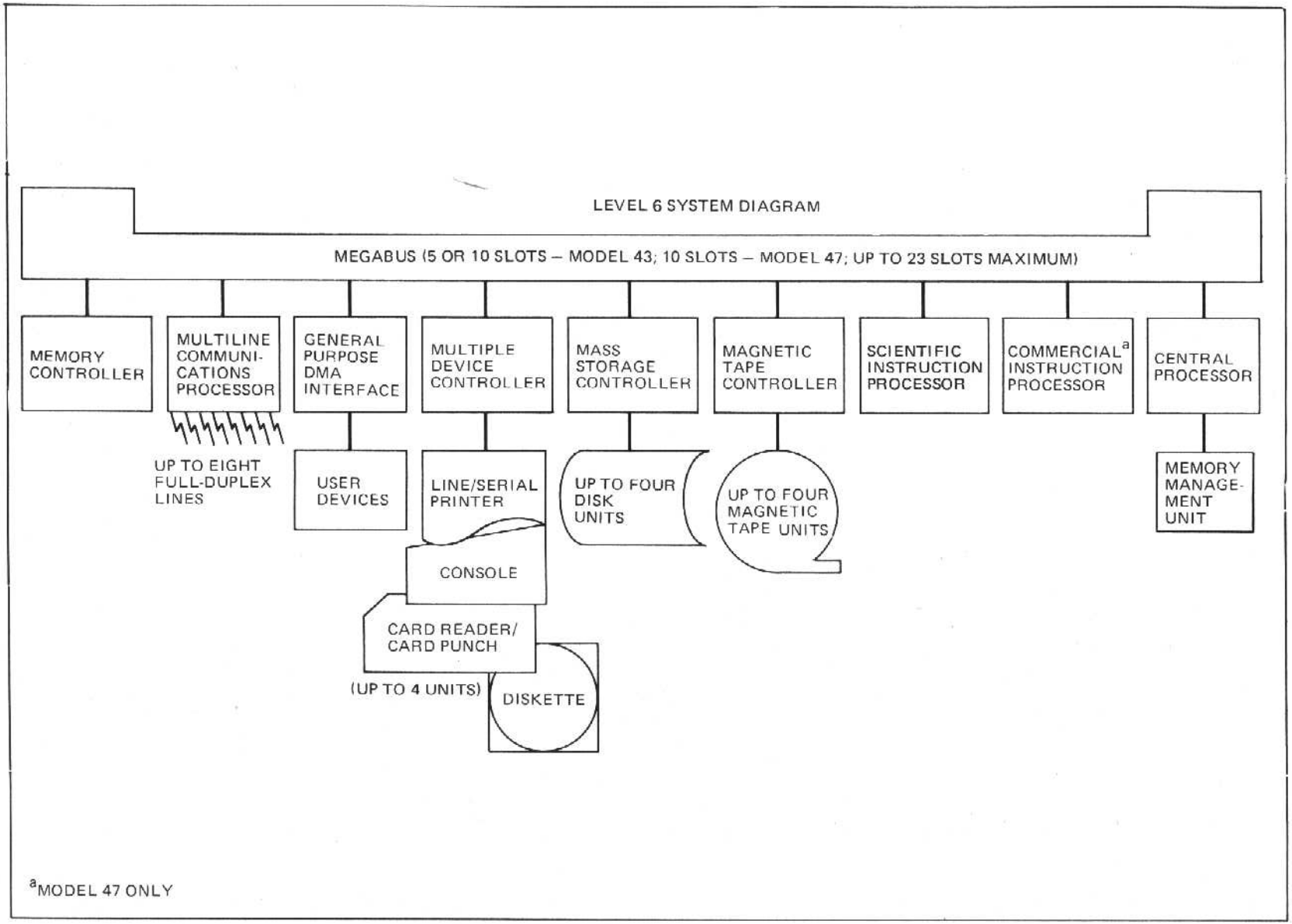


Figure 1-4. Models 43 and 47 Configuration

Model 53 central processor is mounted in a ten-slot Megabus chassis (expandable to 23 slots) and includes a full control panel, multiply/divide hardware, real-time clock, power supply, watchdog timer, ROM bootstrap loader, a 4K-word high-speed cache memory, and a Memory Management Unit (MMU). Maximum memory is one million words.

Model 57 central processor is mounted in a ten-slot Megabus chassis (expandable to 23 slots) and includes the above Model 53 hardware plus a Commercial Instruction Processor (CIP). The CIP is an additional hardware processor tailored to perform string operations that can significantly increase COBOL performance. It operates on a powerful set of 30 commercial instructions which include numeric, alphanumeric, edit, and branch instructions. (Refer to the Model 47 CIP description for further details.)

The 4K-word cache memory enhances the performance of the central processor by decreasing the time required to receive (i.e., fetch) instructions and data from main memory. This decrease in time is achieved both by anticipatory main memory reads and storage of previously used data and instructions for future iterations of the currently executing program.

The MMU permits the allocation and assignment of memory among users and provides for segmentation and read/write/execute protection based on four rings of privilege. Base relocation and descriptor validation are also provided.

The configurability (see Figure 1-5) and compatibility of Models 53 and 57 with the Models 33, 43, and 47 enable maximum flexibility and economy of growth. These two models are the most powerful and versatile of the Level 6 minicomputers.

Features

- o Performance level of Model 53 approximately 50 percent higher than Model 43
- o Up to one million words of directly addressable memory
- o Standard Memory Management Unit provides memory segmentation and protection for two or more concurrent users
- o Standard 4K-word high-speed cache memory enhances CP performance
- o Most powerful and versatile of Level 6 models
- o Supports MOD 200, 400 and 600 software
- o Commercial Model 57 includes a commercial instruction processor
- o COBOL performance level of Model 57 CIP approximately twice the speed of Model 47 CIP
- o Performance level of Model 57 central processor approximately 1-1/2 times the throughput of the Model 47 CP

BOARD TECHNOLOGY

Model 33 and larger models use a primary circuit board measuring 15 inches wide by 16 inches deep which, depending upon its function, may have a number of plug-in pacs inserted. The rear of the circuit board is connected to the Megabus, while devices are connected to the front of the board. Both small-scale and medium-scale integration are used. Figure 1-6 shows a variety of Level 6 circuit boards.

A high-density MOS memory board can contain up to 128K words of memory in four modules (called Memory-Pacs) of 32K words each. As an alternative to the 32K-pac/128K-board, a standard MOS 8K-pac/32K-board is also available. Each Memory-Pac is implemented as a small board, 6.5 inches wide by 6.5 inches deep, plugged directly into the primary board.

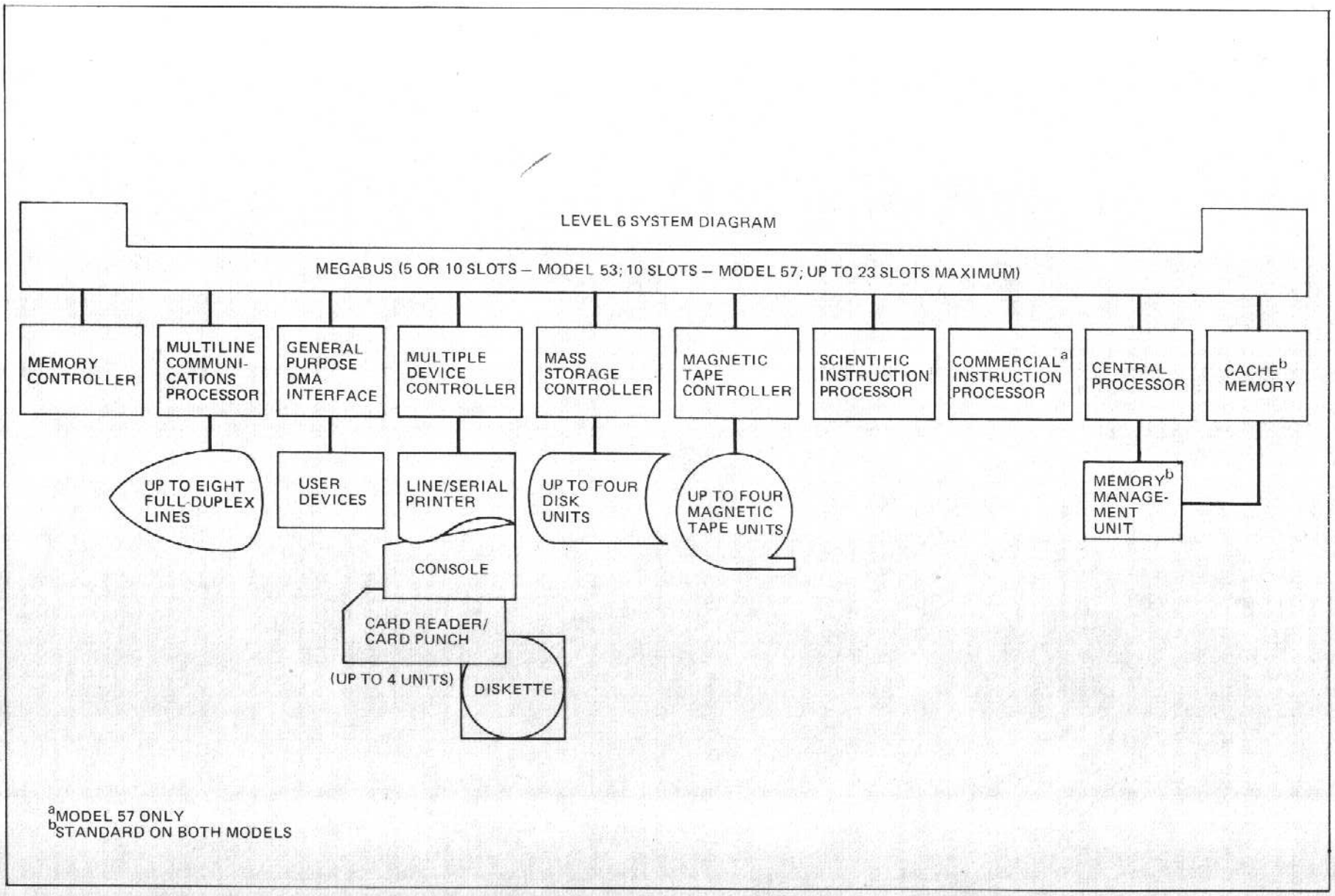


Figure 1-5. Models 53 and 57 Configuration

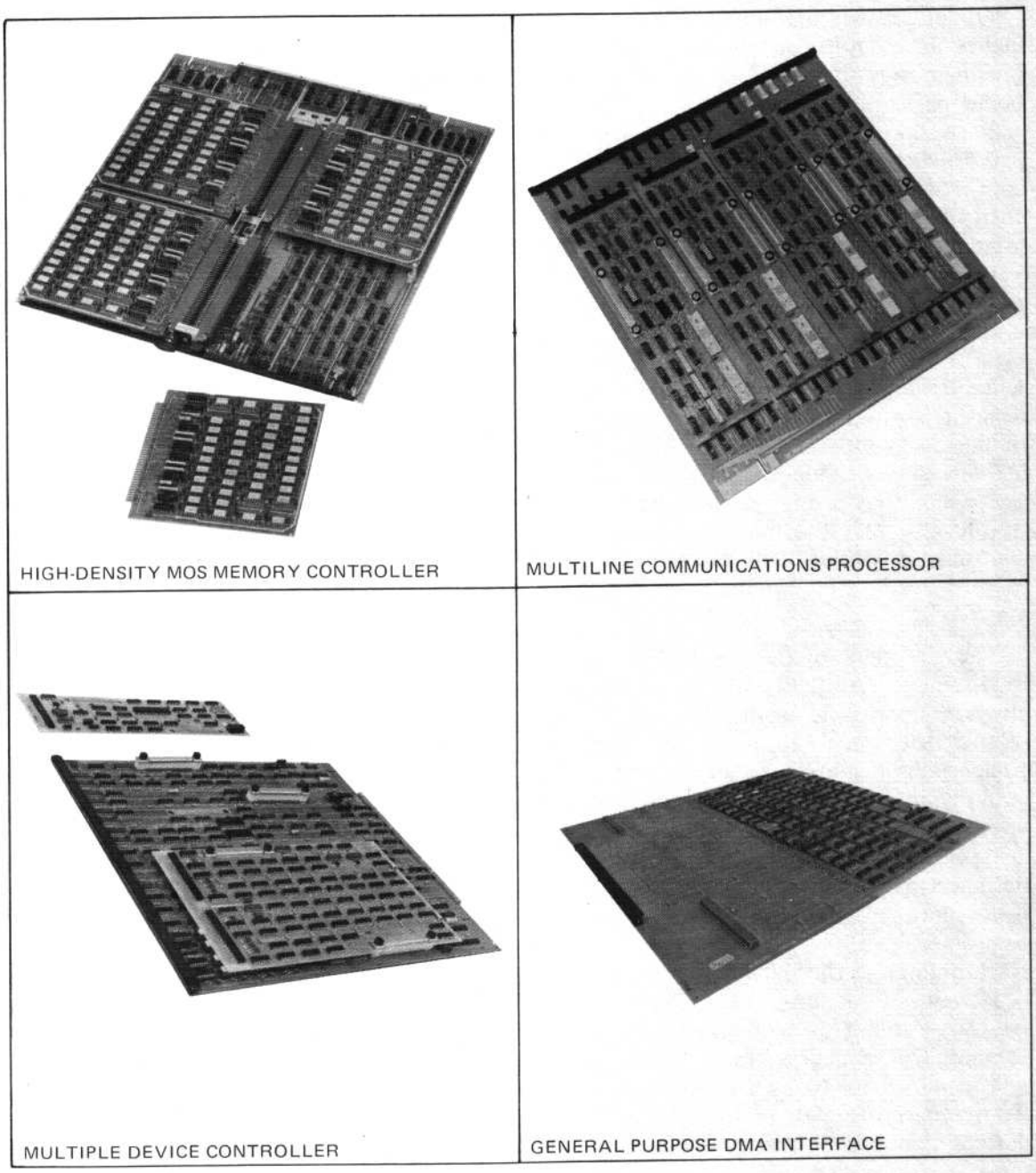


Figure 1-6. Level 6 Circuit Boards

A similar arrangement is used for device and communication controllers. The Multiple Device Controller (MDC) consists of a primary board (containing a microprocessor) onto which up to four device adapter boards (3.5 x 11 inches), called Device-Pacs, can be plugged. Each Device-Pac can support one device, viz., an ASR/KSR teleprinter, teleprinter-compatible CRT display, keyboard typewriter console, card reader, serial printer, or line printer. The diskette Device-Pac is a double-size pac and supports either one or two diskette drives. The primary board/pac concept is also used in the Mass Storage Controllers (MSCs), Magnetic Tape Unit Controllers (MTCs), and the Multiline Communications Processors (MLCPs).

Model 23 uses a full-width central processor board measuring 15 inches wide by 13.6 inches deep, and up to ten adapter boards measuring 7.3 inches wide by 13.6 inches deep for memories, peripherals, and communications. These boards do not use the primary board/pac concept.

Each Level 6 primary board and Device-Pac is individually replaceable. Each board and pac provides so much functionality that Level 6 is physically more compact than most of its competitors. Furthermore, the use of the primary board/pac concept permits the sharing of costly logic (memory error correction, controller microprocessors) among an unusually high number of basic elements (memory, devices) with very flexible configurability. Thus the Level 6 approach satisfies user's demands for economy in four critical areas: space, power, cabling, configurability.

In addition, board addresses (channel numbers) are easy to configure. There are 2^{10} possible channels. Users can configure a channel number by setting a hexadecimal rotary switch (establishing a starting channel number for each controller). This feature is important to all users, and especially to system builders planning to develop software on a large configuration and then use it on many smaller, differently configured systems. Level 6 also includes a device-identification feature, so users will not have to keep changing their software when they change controller or device channel numbers.

Note also that the microprocessors make these controllers more capable, relieving the central processor of many tasks, and also enhance their diagnostic capability.

PACKAGING

The packaging of the Level 6 models has been designed to satisfy a variety of cabinetry requirements. Available are: 1) rackmountable units for mounting in a user's own RETMA (Rackmounted Electronics Terminal Manufacturer's Association) cabinet, 2) Honeywell 60-inch cabinet, 3) Honeywell 30-inch minirack, 4) tabletop units, and 5) office furniture package. An example of a Model 43 5-card chassis and the five types of cabinetry in which it could be mounted is shown in Figure 1-7.

All Level 6 packaging options provide easy front access and require only front-to-rear airflow for cooling. (In many other minicomputer systems, large backboard areas force designers to use side-to-side cooling with the attendant difficulties of avoiding recirculation in cabinet configurations.)

Rackmountable Units

Honeywell rackmountable devices are designed to be installed in a customer-supplied RETMA cabinet using the same physical configuration rules as for the Honeywell 60-inch cabinet. These devices range in height from 3.5 in. (8.8 cm) for the Memory Save and Autorestart Unit to 24.5 in. (62.2 cm) for the magnetic tape unit, and have side-mounted fittings permitting them to slide into a standard 19 in. (48.2 cm) RETMA cabinet. Other devices that can be installed in the RETMA cabinet include a central processor, diskette units, cartridge disk units, and a power distribution unit.

Honeywell 60-inch Cabinet[1]

The 60-inch cabinet provides standard EIA (Electronic Industries Association) rack space and allows optimum placement of devices. A magnetic tape unit or diskettes and Memory Save Unit mount above the CP while CP expansion options, cartridge disk units, and power distribution unit mount below the CP. The cabinet is offered with or without a table attachment designed to hold tabletop peripherals. A matching expansion cabinet for additional peripherals is also available.

---

[1] Not applicable to Model 23.

Figure 1-7. Level 6 Packaging and Cabinetry Options

Honeywell 30-inch Cabinet

The 30-inch cabinet (also called a "minirack") serves as a compact assembly for housing Level 6 central processors. The cabinet accommodates the standard rackmounted peripherals with the exception of magnetic tape units. A tilt-up vertical control panel with a power on/off switch and security keylock is also available. For expansion purposes, additional cabinets can be added to accommodate Level 6 peripherals.

Tabletop Units[2]

Tabletop units are completely enclosed and portable. The tabletop devices have the same physical, mechanical, and electrical characteristics as their rackmounted counterparts except that they are self-contained and can be placed on desks, tables, or other flat-surface support areas. These tabletop units include central processor, Memory Save Unit, CRT keyboard console, single/dual diskette unit, serial printer, card reader, and/or CRT display terminal.

[2] Applicable to Models 33 and 43 only.

Office Furniture Package

The office furniture package incorporates handsome, desk-styled cabinetry for optimum operator interface with documents, keyboard, and CRT. With the basic unit, the keyboard, power switch, and keylock are integrated into the surface area forefront, which is constructed of metal. The molded-plastic, table surface provides a dedicated mounting space to secure a CRT at the proper height and angle to reduce reflections and enhance readability. There is ample surface space for mounting desk top peripherals as well as a spacious operator work surface.

Users may choose to mount a tilt-up control panel inside the base cabinet or have the control panel integrated into the tabletop surface and concealed by a hinged dress cover. For the system builder, two additional models are available: one provides a flat tabletop surface; the other features a flat tabletop with a recessed keywell for keyboard placement.

The cabinet interior is designed to house the user's choice of central processor, diskettes, cartridge disk units, power distribution unit, and other system options. For system expansion, additional 30-inch cabinets are available.

QUALITY LOGIC TESTS

A portion of the firmware on the CP, CIP, SIP, and peripheral controller (MDC, MLC, MSC, and MTC) boards is reserved for hardware verification routines called the Quality Logic Tests (QLTs). Their purpose is to verify basic data paths and to supply a go/no-go visual identification of a hardware failure prior to running the test and verification programs. The CP QLT tests the CP and memory. The CIP, SIP, and I/O controller tests are tailored for each unit.

The QLTs are automatically executed as part of the normal bootstrap load process, in response to a Master Clear on the Megabus or an initialize command (issued by software). Results of the QLT appear as a visual indication on the central processor control panel and on the edge of the particular board failing the QLT. A light-emitting diode (LED) indicator lights up during execution of the QLT and turns off only if the QLT is successfully completed.

In addition, on the MLC board, each of the eight lines has program-usable loop-back of data transmit to data receive to facilitate diagnosis. The SIP and CIP can execute a mini-QLT via a standard CP command, which selectively tests the functional operation of the SIP/CIP without affecting the contents of the mode registers, indicator registers, or status word, etc.

SYSTEM ELEMENTS

Bus

The bus is the heart of a Level 6 system and central to its performance. All system elements – central processor, memories, peripheral device controllers, communications processors, scientific processor, commercial instruction processor, and general purpose DMA interfaces – are attached to the bus, and all transfers (memory, interrupts, and instructions) between them take place on the bus. Communication among these elements may be synchronous or asynchronous, depending upon the type of bus a model has.

Model 23 has a dual, synchronous, bidirectional bus with shared data and address lines. All Model 23 peripheral data transfers are in the direct multiplex control (DMC) mode whereby I/O or memory transfers are controlled by the CPU (via registers maintained in CPU scratchpad memory). Communications, however, occurs in the direct memory access (DMA) mode whereby transfers are controlled by the communications adapter(s), thus freeing the central processor for other tasks. The maximum I/O transfer rate in the DMC mode is 165K bytes per second; in the DMA mode, it is 1.88M bytes per second (500 nanoseconds per 16-bit transfer cycle).

Model 33 and larger models have a single, asynchronous, split-cycle, bidirectional bus with separate data and address lines. Because of its speed and versatility, it is also referred to as the "Megabus." The Megabus offers a peak transfer rate of six million bytes (i.e., half-words) per second (300 nanoseconds per 16-bit transfer cycle). Based on TTL technology, the Megabus uses etched wires to join connectors, meaning fewer connections, lower costs, and higher reliability.

The Megabus transfers words; however, controller transfers can start or end on arbitrary byte boundaries. All transfers are direct memory access; each device controller maintains its own information about the location in memory to/from which data is to be transferred and accesses that location directly. Each unit on the Megabus contains all the control and timing it needs to use the Megabus, without dependence on the central processor.

All Level 6 models have 64 vectored-interrupt levels and an automatic interrupt identification feature that causes an interrupting device to identify itself to the central processor. No private wires are required for interrupts; an interrupt is handled as just one more type of message transmitted on the bus. Parity checking ensures the integrity of data transfers.

Central Processor

The Level 6 central processor, using TTL technology, is a state-of-the-art device – open-ended, powerful, and flexible. The word size is 16 bits – which makes the most of combined economy and functionality. Key features of the architecture may be summarized as follows:

- o 18 to 26 program-visible general registers, including multiple accumulators and multiple address, index, and control registers and a program counter
- o Bit, byte, word, and double-word instructions
- o Bit test, set, and mask capability
- o Immediate, register-to-register, and register-to-memory operations
- o 64 vectored interrupt levels
- o Multiple vectored trap structure
- o Hardware-supported context save and restore
- o Multiple addressing modes, including indexing, indirect addressing, base plus displacement, program-counter-relative, auto increment/decrement, etc.
- o Permanent bootstrap
- o Power failure detection
- o Real-time clock and watchdog timer
- o Automatic restart

The watchdog timer feature enables interruption of central processor operations at preset time intervals. It is optional with the Model 33 and standard on all the other Level 6 models.

The instruction set is programmer-oriented, facilitating the writing of compact, efficient programs and offering the right instruction for each function. The multiple word-length capability makes it easy to handle data elements of varying size, while the indexing techniques are completely integrated into the architecture.

The instruction set design strikes a highly effective compromise between two groups of conflicting user requirements: on the one hand the desire for more operation codes, operands, and flexible ways of addressing an operand; on the other hand, the reluctance to devote extra space in costly memory for these instructions, many of which are infrequently used.

The Level 6 approach defines a 16-bit instruction format that is extended in a number of ways. For example, a 16-bit instruction does not contain a direct memory address (though it does allow the programmer to address memory). For a direct address, a field is added to the instruction: this may be a 16-bit direct address. Thus a 32-bit instruction is achieved as needed. Another method is to use a 16-bit displacement relative to the program counter. The result of this approach is to realize added power only when it is required without compromising the design of the 16-bit instruction in which most of each program is actually written.

A bootload capability is included on the CP board. It is a ROM stored process and therefore permanent. There is no elaborate load procedure or multiple keying. Users can select any device through the control panel and bootload from there, providing only the device address (if the bootload is not from the default bootload device). Other outstanding characteristics of the central processor are as follows:

The maximum Level 6 memory (one million words) can be *addressed directly* (i.e., without an "indirect address" elsewhere in memory); the complexities and overhead of paging/segmentation units are avoided.

The Level 6 indexing technique permits *addressing and manipulating bits and bytes* in memory. Bit instructions allow testing, setting, resetting, complementing, etc. addressed bits. Byte instructions allow logical and arithmetic operations. Both facilitate the writing of compact, efficient programs.

The 18 *programmable registers* available with the Models 23 and 33 include 7 address registers, 7 data registers, 3 index registers (using data registers), 3 control registers, and a program counter. This is a large complement for a minicomputer. Programs can be more compact and execution times faster than on machines with fewer registers. The Models 43 and above have 26 registers.

The Level 6 *interrupt structure*, with its associated firmware-level dispatching and automatic context save/restore efficiently maintains a 64-level priority system while eliminating the need for complex software to perform this function.

Hardware trap support of up to 20 trap conditions allows quick handling of exceptional conditions (e.g., overflow) and permits a source program to run even if a facility it requires is not installed.

Level 6 includes instructions that facilitate *stack and queue manipulation* (Models 43 and above), including subroutine calls, re-entrant and recursive programming, and data buffer management.

Main Memory

Level 6 offers Model 33 and larger model users the choice and flexibility of MOS and core memory. Model 23 is limited to high-density MOS, single-fetch, parity memory. Maximum memory configurations range from 64K words on the Model 23 and 33 to one million words on Models 43 and above. The memory, like other elements of Level 6, is a bus-compatible subsystem that communicates directly with and in the same fashion as any other element on the bus.

- *MOS Memory* – incorporates state-of-the-art semiconductor technology, N-channel, 4096-bit (standard) or 16,384-bit (high-density) MOS dynamic RAMs as the storage media. The design emphasizes high reliability, low cost, modularity, and simplified field maintenance. TTL MSI circuitry minimizes power and space requirements for the extensive functionality provided. Two kinds of MOS memory are offered: byte-parity memory and Error Detection and Correction (EDAC) memory.
  - *Byte-parity* includes two parity bits per word for an actual word size in memory of 18 bits. The parity bits are returned to anyone reading the memory. This memory is the most economical.
  - *EDAC* includes six additional bits (EDAC code) per word, which are derived from the data bits. When the 22-bit word is read, memory corrects any internally caused single-bit data error, reporting the results over two dedicated leads on the Megabus. Each lead sets a specific status bit depending on whether the error has been corrected or not. All single-bit errors are corrected while all double-bit errors are detected. The EDAC memory is particularly desirable for large systems, where extended reliability is required.

For both EDAC and parity memory, users may choose from among three different types of memory controllers, two of which enable single- or double-word fetch capabilities using 8K-word Memory-Pacs (32K-words per controller). The third memory controller type is user-configurable to operate in either single- or double-word fetch mode and uses 32K-word Memory-Pacs (128K-words per controller).

Memory is increased by adding Memory-Pacs singly for the single-fetch memories, or in pairs for the double-fetch memories. The 8K-word and 32K-word Memory-Pacs are not interchangeable.

- *Core Memory* — useful where a nonvolatile memory is required. It is offered on Models 33 and above in either 16K- or 32K-word modules and can be intermixed with interleaved MOS memory. Core memory systems have the capability of preserving their contents for a indefinite length of time during a power failure and of automatically restarting when power is resumed. All words are 18 bits in length, consisting of 16 data bits and two parity bits.

With either kind of memory, address parity accompanies the most significant eight bits on the address bus. When memory detects an error on these bits, it does not respond; the result is a bus timeout. Note also that each device controller/communication processor on the bus checks parity on information received from the bus and indicates an error by setting a parity error status bit. Table 1-2 lists the various kinds of memory configurations possible.

TABLE 1-2. MEMORY CONFIGURATIONS

Memory Type	Type No.	Memory-Pac/ Controller	Memory Size	Parity/ EDAC	Model Used On	Prerequisite
Semiconductor	CMC9001	Controller	8K Words	Parity	33, 43, 47, 53, 57	Slot
(MOS) Memories	CMM9001	Memory-Pac	8K Words	Parity	33, 43, 47, 53, 57	CMC9001
(Single-Fetch)	CMC9002	Controller	8K Words	EDAC	33, 43, 47, 53, 57	Slot
	CMM9002	Memory-Pac	8K Words	EDAC	33, 43, 47, 53, 57	CMC9002
	CMM9307	Memory-Pac and Controller	16K Words	Parity	23	Slot
	CMM9308	Memory-Pac and Controller	32K Words	Parity	23	Slot
	CMM9309	Memory-Pac and Controller	64K Words	Parity	23	Slot
Interleaved	CMC9501	Controller	16K Words	Parity	43, 47, 53, 57	Slot
Semiconductor	CMM9501	Memory-Pac	16K Words	Parity	43, 47, 53, 57	CMM9501
(MOS) Memories	CMC9502	Controller	16K Words	EDAC	43, 47, 53, 57	Slot
(Double-Fetch)	CMM9502	Memory-Pac	16K Words	EDAC	43, 47, 53, 57	CMC9502
Interleaved	CMC9009	Controller	32K Words	Parity	33, 43, 47, 53, 57	Slot
Semiconductor	CMM9006	Memory-Pac	32K Words	Parity	33, 43, 47, 53, 57	CMC9009
(MOS) Memories	CMC9010	Controller	32K Words	EDAC	33, 43, 47, 53, 57	Slot
(Single- or Double-Fetch)	CMM9007	Memory-Pac	32K Words	EDAC	33, 43, 47, 53, 57	CMC9010
Core Memory	CMC9005	Controller	16K Words	Parity	33, 43, 47, 53, 57	Slot
	CMC9006	Controller	32K Words	Parity	33, 43, 47, 53, 57	Slot

Memory Save and Autorestart Unit (PSS9001/9002/9303)

The Memory Save and Autorestart Unit is an optional device available on all Level 6 models (see Figure 1-8). Its purpose is to provide for the retention of the contents of up to two MOS memory boards (64K words using standard MOS or 256K words using high-density MOS memory) for up to ten minutes on a Model 23 and up to two hours on a Model 33 or larger model in the event of a power failure or fault. PSS9303, a single, plug-in board, is used on the Model 23; PSS9001 and 9002, used on the other Level 6 models, are contained within a separate cabinet.

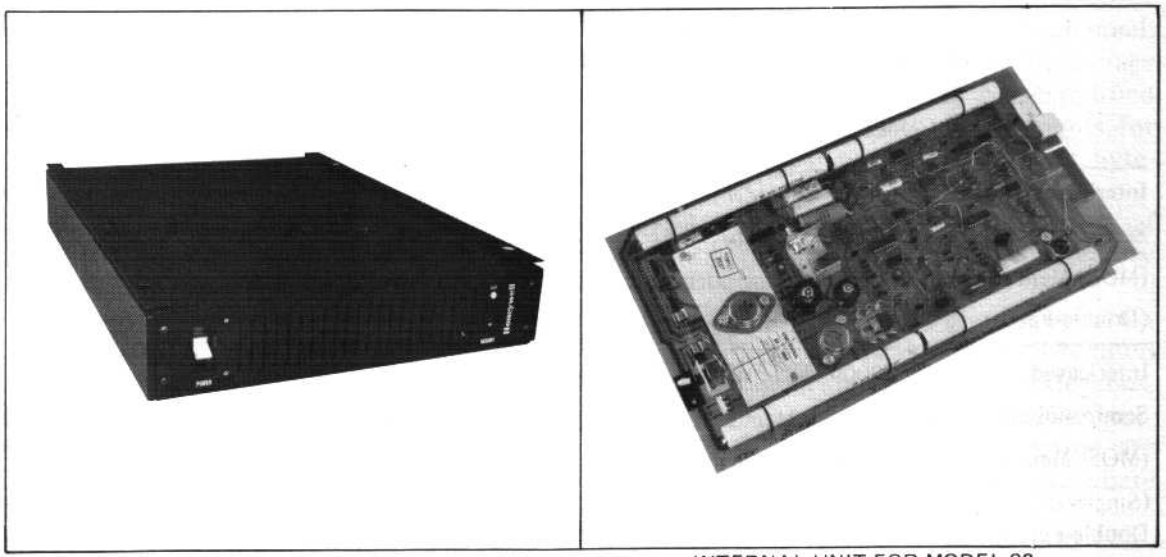
The Memory Save and Autorestart Unit provides the necessary voltage to maintain the contents of the Level 6 memory as well as to charge its batteries when ac is available on input. In the event of a normal operator system power down, the memory contents are safely retained until the system is manually powered up again.

The Memory Save and Autorestart Unit supplies power to memory at all times and as long as there is no line disruption, the memory contents will be retained. The device is plugged into a standard 120-volt receptacle and also has an outlet for connection to the central processor.

An on/off switch enables the selection of one of two states. When placed in the off position, memory contents are not protectable. When placed in the on position, however, CP memory contents are protected and retainable for up to ten minutes/two hours in the event of a power failure or indefinitely when the CP is manually powered down.

The Autorestart feature provides for the generation of an interrupt upon the detection of an impending power failure. The interrupt handler within the user's program has 1.5 ms in which to perform a save status operation storing the restart information considered essential, e.g., registers and memory locations. Following the power failure, operations will be automatically resumed with the first instruction at memory location zero, which should contain a branch to a software routine that will perform the restart operations.

The device also contains a "Memory On" indicator (LED) which when lit indicates the proper functionality of the device and its associated CP memory. Loss of ac power for longer than ten minutes (Model 23)/two hours or a malfunction in the device causes the power supply and the "Memory On" indicator to be turned off. A manual reset is then necessary to light the indicator again, thereby restoring power and enabling a restart operation.



EXTERNAL UNIT FOR MODEL 33 AND LARGER

INTERNAL UNIT FOR MODEL 23

Figure 1-8. Memory Save and Autorestart Unit

Features

- o Supplies power to support 64K/256K words of MOS memory during normal computer operation
- o Maintains contents of two MOS memory boards during power outages of up to two hours on Models 33 and up; up to ten minutes on Model 23
- o Retains memory contents when system is manually powered down, not in active use, or is under repair as long as ac power is not removed from the device
- o Available in either tabletop (PSS9001) or standard rackmountable (PSS9002) versions for Models 33 and larger; plug-in board for Model 23

Memory Management Unit (CPF9501)

To facilitate multi-user systems, a Memory Management Unit is offered that permits the allocation and assignment of memory among users and provides for segmentation and Read/Write/Execute protection based on four rings of privilege. The unit also provides base relocation and descriptor validation. The MMU is optional with the Models 43 and 47 and standard with the Models 53 and 57.

Features

- o Memory relocation and protection suitable for two or more concurrent users
- o Based on "ring" approach pioneered by Honeywell's MULTICS system
- o Non-bypassable, hardware-enforced control
- o Selective sharing of information through controlled access
- o Double protection of information via access rights and ring protection
- o Support of both Short Address Form (SAF) and Long Address Form (LAF)
- o Executes with no degradation in performance

Controlled Access

The MMU permits the controlled access and sharing of programs and data among various users. This is accomplished by organizing information into segments with each segment described by a 32-bit segment descriptor. The segment descriptor defines the segment base, size, access rights (read, execute, write, a combination of these, or none of these), and the lowest-privileged ring in which it can read, write, or execute. Each segment is relocated independently and need not be contiguous, in order, or have any other particular relationship. Access control is interpreted by the software, but enforced by the hardware on each reference to the information.

Ring Protection

The MMU utilizes a ring structure to control its users and protect its operating system. In this ring structure there are four rings of protection. The rings are numbered 0 through 3 with ring 0 being the most privileged and ring 3 the least privileged. Ring 0 can be used for the most critical system functions; Ring 1 for less critical system functions; Ring 2 to create a "user supervisor" or for well-checked-out user programs; and Ring 3 for the majority of user software. Programs operating in one ring cannot access code or data reserved for rings of higher privilege and access rights checking is still required.

Major Benefits

- o Maintains source data integrity – data to be read, but not modified, can be given a read only access.
- o Aids program checkout – many programming errors can be detected quickly by making data segments non-executable and code segments non-writeable.

- o Prevents copying – proprietary routines that a user is permitted to execute can be made inaccessible to read operations.
- o Safeguards sensitive data – critical system control data can be placed in a user's address space so that operating system routines executing on a user's behalf can access it efficiently, but made inaccessible to user programs.
- o Increased productivity – several users can currently use the system with/without the selective sharing of programs and data.

Scientific Instruction Processor (CPF9503)

The Scientific Instruction Processor (SIP) is an optional single-board processor available for Models 43 and up. It operates on a powerful set of 30 scientific instructions. This set includes arithmetic operations on single-precision and double-precision floating-point operands, and single-word and double-word integer operands.

The SIP contains three variable-length scientific accumulators that may contain floating-point values of two or four words. Control bits define both the accumulator length and length of memory operands directed to that accumulator.

All operands stored in the SIP are in floating-point format. Operands directed to the SIP from main memory are also in floating-point format, while those from the CP are in integer format. Integer operations directed to the SIP are converted to floating-point values prior to entering into the scientific calculations.

Features

- o 32- or 64-bit floating-point formats provide accuracy of 6 or 14 hexadecimal characters.
- o Three scientific accumulators in SIP each hold either single-precision (32-bit) or double-precision (64-bit) floating-point quantities.
- o Floating-point operands in main memory or in a SIP accumulator can be arithmetically combined with another operand in an accumulator, same or mixed precision.
- o Mixed mode arithmetic between integer values in certain CP general registers (either single-word or double-word) and floating-point values in the SIP scientific registers is effected with the integer value being automatically converted to floating-point prior to processing.
- o Upon decoding of a scientific instruction, the CP sends the command and the operand memory address (if required) to the SIP, and goes on to the next instruction. The SIP gets the operands from memory under DMA control and overlaps processing with the CP processing.
- o The SIP includes "double-fetch" logic and gets operands from memory two words at a time if interleaved memory is included in the system. Table 4-1 lists the instructions implemented by the Scientific Instruction Processor.

Peripheral and Communications Controllers

The Models 33 and larger use microprocessor-based peripheral and communications controllers that attach a number of plug-in Device-Pacs or Communications-Pacs to which a peripheral unit/modem connects. The Model 23 uses peripheral and communications adapters which are also microprocessor-based, but have their pacs integrated into the adapter and connect fewer peripheral units/modems.

Single/Dual Console Adapter (KCM9301/9302)

The KCM9301 Single Console Adapter and the KCM9302 Dual Console Adapter provide Model 23 users with the capability of attaching up to two keyboard typewriter (TWU9104/9106) and/or CRT keyboard (DKU9101/9102/9103/9104) consoles to their system. See Figure 1-9.

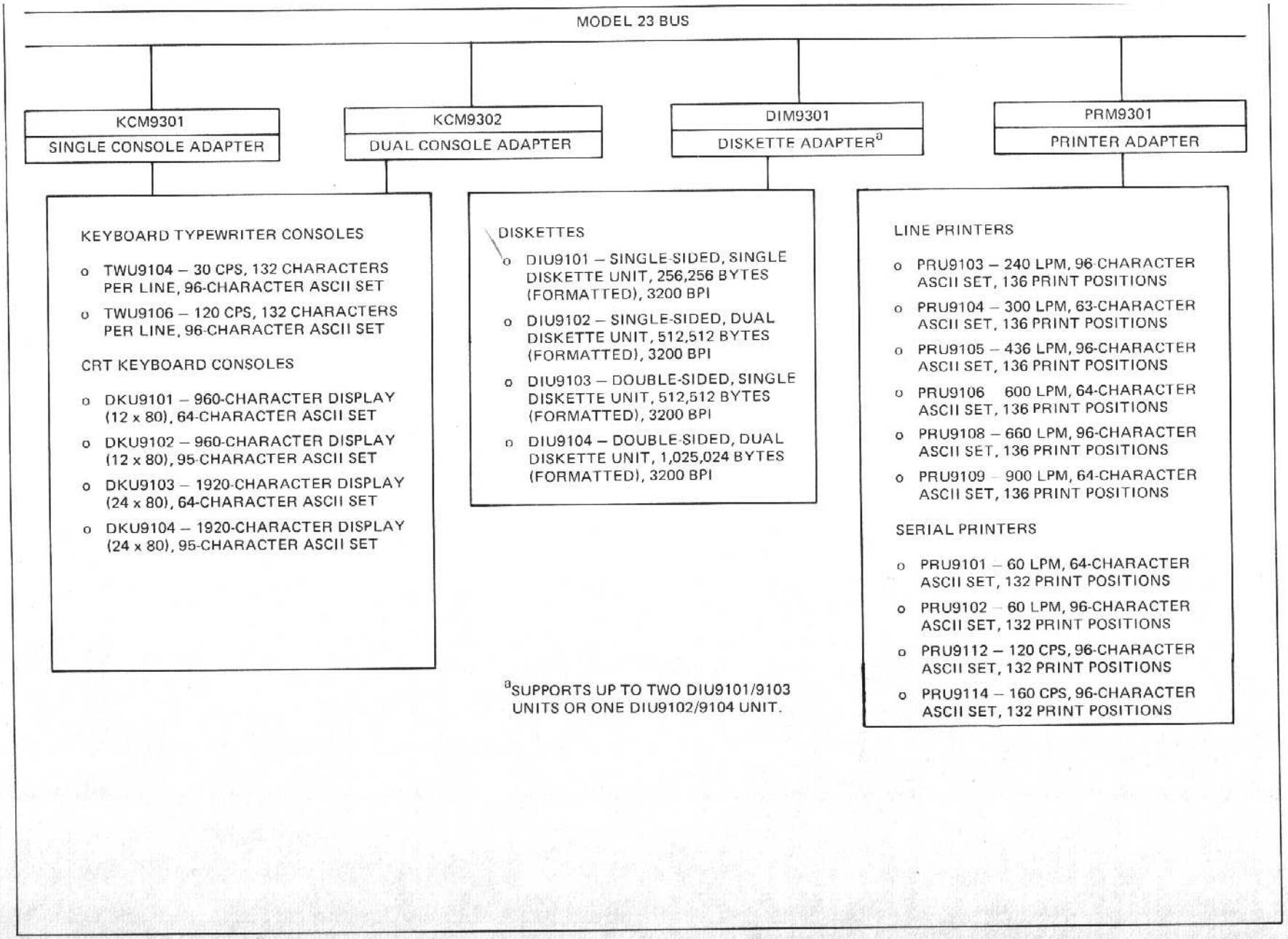


Figure 1-9. Model 23 Peripheral Configurations

Diskette Adapter (DIM9301)

The DIM9301 Diskette Adapter enables Model 23 users to attach single and dual diskette units (up to four single diskette units or two dual diskette units). A choice of units capable of single-sided (DIU9101/9102) or double-sided (DIU9103/9104) recording is offered. Storage capacity ranges from 256,256 bytes up to a maximum of 2,050,048 bytes. See Figure 1-9.

Printer Adapter (PRM9301)

The PRM9301 Printer Adapter allows Model 23 users to connect a 120-160 cps serial printer (PRU9101/9102/9112/9114) or 240-900 lpm line printer (PRU9103/9104/9105/9106/9108/9109). See Figure 1-9.

Dual-Line Asynchronous Communications Adapter (DCM9301)

The DCM9301 Dual-Line Communications Adapter provides Model 23 users with two 9600-baud asynchronous lines. See Figure 1-10.

Single-Line Synchronous Communications Adapter (DCM9302)

The DCM9302 Single-Line Communications Adapter for the Model 23 enables the control of one 9600-baud synchronous line. See Figure 1-10.

Dual-Line Synchronous Communications Adapter (DCM9303)

The DCM9303 Dual-Line Synchronous Communications Adapter enables the Model 23 to control up to two 9600-baud synchronous lines. See Figure 1-10.

Dual-Line Asynchronous/Synchronous Communications Adapter (DCM9304)

The DCM9304 Dual-Line Asynchronous/Synchronous Communications Adapter enables the Model 23 to control one synchronous and one asynchronous line up to 9600-baud. See Figure 1-10.

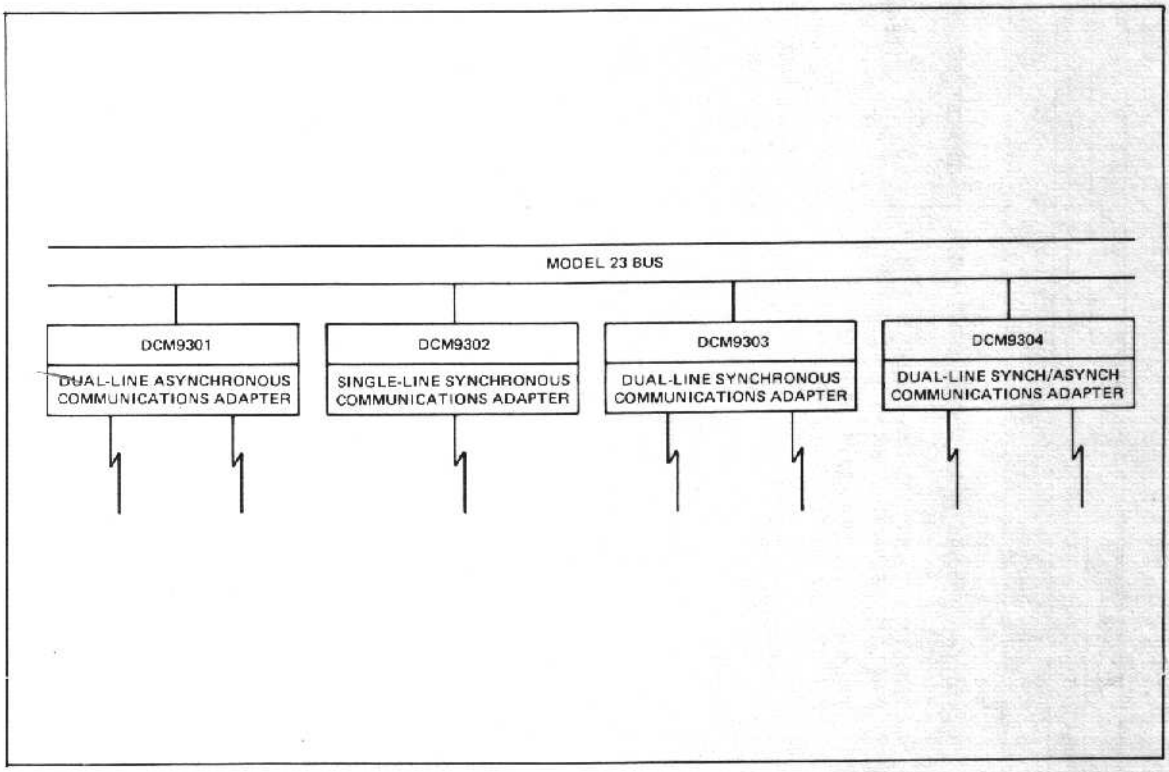


Figure 1-10. Model 23 Communications Configurations

Multiple Device Controller (MDC9101)

The Multiple Device Controller provides Level 6 Model 33 and larger model users with a low-cost capability to attach and control up to four low- to medium-speed peripheral devices. Multiple MDCs can be attached to the Level 6 Megabus, and a variety of devices can be attached to any MDC, thus offering considerable versatility and flexability in the choice and complement of peripherals. Peripheral devices interface to the MDC9101 via their Device-Pacs, which contain all the hardware unique to a particular peripheral device. Each MDC has space for up to four Device-Pacs; certain Device-Pacs (diskette and card punch) are double-sized and thus take up two of the four channels (ports) on an MDC. The Device-Pacs and the peripherals with which they interface are shown in Figure 1-11. Peripherals include a cable that attaches directly to the Device-Pac.

Features

- o Attaches up to four of the following peripheral devices: card readers, card punches, line printers, serial printers, consoles, and diskettes
- o Enables up to four levels of simultaneity
- o Provides maximum throughput rate of 120K bytes per second
- o Executes all data transfers in DMA mode
- o Fixed-length sector recording of either 256 or 576 bytes

Mass Storage Controller (MSC9101)

The MSC9101 Mass Storage Controller offers Level 6 Model 33 and larger model users the capability of attaching medium-capacity cartridge disk units to their system. Incorporating sophisticated hardware and firmware, the MSC9101 microprogrammed control supports the connection of up to four DCU9114/9115/9116 Cartridge Disk Units in configurations of single removable cartridge disk or removable and fixed cartridge disk units.

The cartridge disk units interface with the MSC9101 via a Disk Device-Pac (CDM9101). Each Device-Pac can connect up to four disk units of the same density. Only one Device-Pac per MSC is permitted. See Figure 1-12.

Features

- o Attaches single removable or removable and fixed cartridge disk units
- o Offers disk configurations of from one to four units (5.0M bytes to 44.8M bytes)
- o Enables multiple disk seeks concurrent with one data transfer operation
- o Provides maximum throughput rate of 312K bytes per second
- o Executes all data transfers in DMA mode
- o Fixed-length sector recording of either 256 or 576 bytes

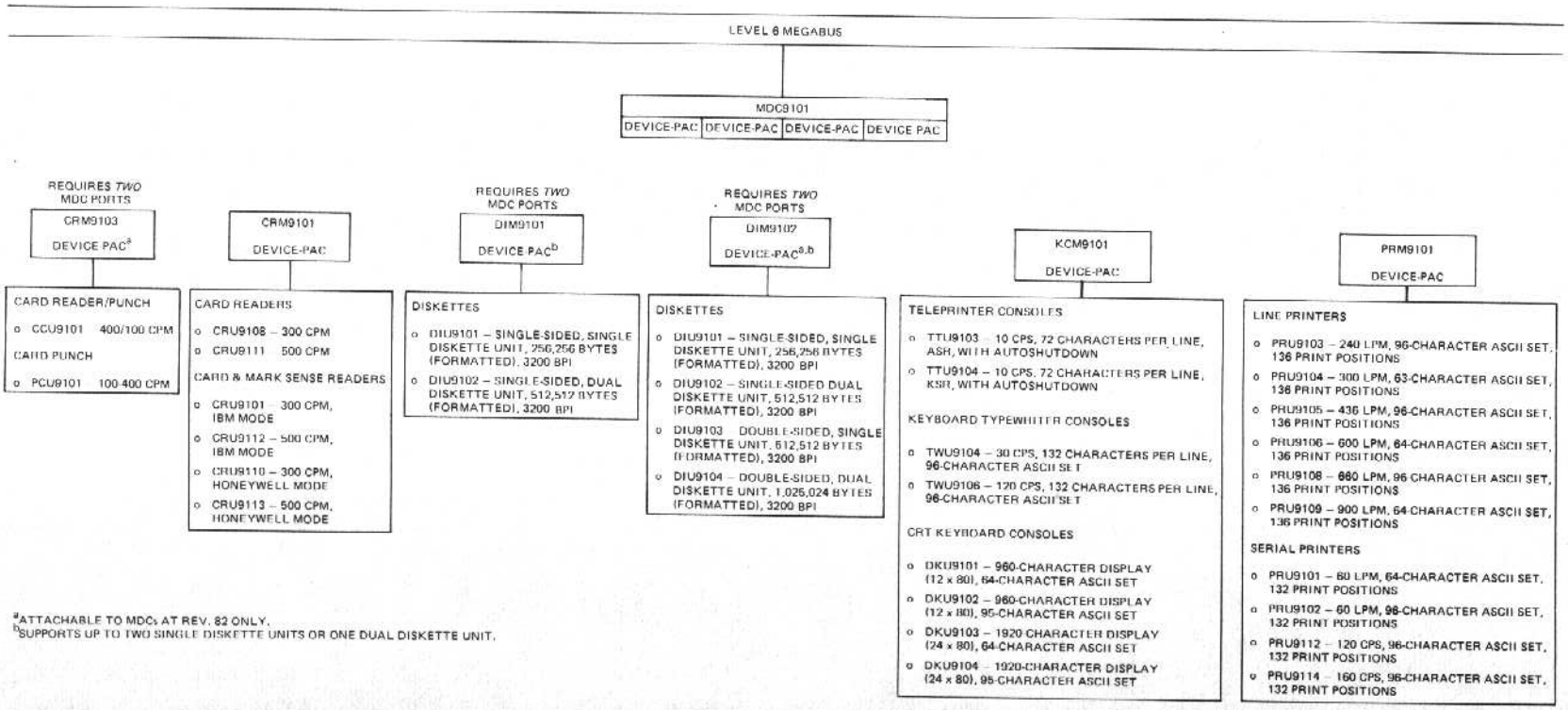


Figure 1-11. MDC Configurations

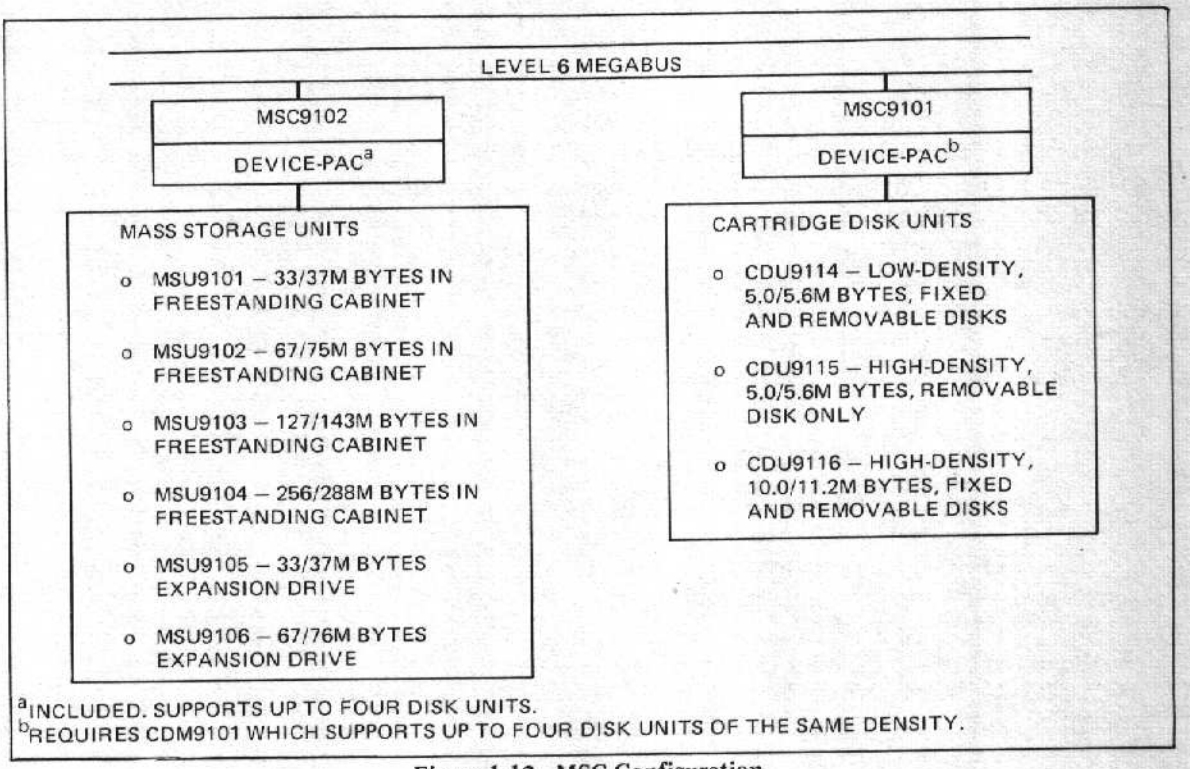


Figure 1-12. MSC Configuration

Mass Storage Controller (MSC9102)

The MSC9102 Mass Storage Controller is part of the Mass Storage Subsystem that offers Level 6 Model 33 and larger model users the capability of attaching high-capacity removable disk units to their system. Consisting of a controller and 1 to 4 MSU9101/9102/9103/9104/9105/9106 removable disk units, a subsystem can provide for online data bases ranging from 33M bytes to over 1 billion bytes.

The removable disk units interface with the MSC9102 via a common Device-Pac that is included in the basic subsystem. The Device-Pac can connect up to four units. See Figure 1-12.

Features

- o Offers disk configuration of from one to four units (33M bytes to 1 billion bytes)
- o Transfer rate of 1.2M bytes per second
- o Fixed-length sector recording of either 256 or 2304 bytes
- o Multiple-sector read/write capability with automatic track and cylinder switching
- o EDAC (Error Detection and Correction) recording to help ensure high reliability
- o Device-Pac included
- o Executes all data transfers in DMA mode

NRZI Magnetic Tape Controller (MTC9101)

The NRZI Magnetic Tape Controller offers Level 6 Model 33 and larger model users the capability of attaching magnetic tape units as well as unit record devices to their system with a single controller. Incorporating sophisticated hardware and firmware, the MTC9101 micro-programmed control supports the connection of up to four 7-track magnetic tape units (MTU9112/9113), or up to four 9-track magnetic tape units (MTU9104/9105), or a combination of tape units and unit record devices (serial/line printers and card readers), up to a maximum of two tape units and two unit record devices.

Seven- and nine-track magnetic tape units may not be mixed on the same MTC9101; however, they may be mixed on the same Level 6 system if a second MTC9101 is configured. Multiple MTC9101s can also be configured if users require extra functionality such as read-write simultaneity, additional tape drives, and additional unit record devices. Tape speeds of 45 ips and 75 ips may be mixed on the same MTC.

The tape units interface to the MTC9101 via a single 9-track NRZI Magnetic Tape Device-Pac (MTM9102) or single 7-track NRZI Device-Pac (MTM9101). Up to four 7-/9-track tape units are supported by either Device-Pac. An alternate configuration of two 7-/9-track tape units and two unit record devices is also permitted. The unit record devices require their own Device-Pac. See Figure 1-13.

Features

- o Connects up to four 7- or 9-track tape units
- o Alternately connects up to two tape units and two unit record devices
- o Executes all data transfers in DMA mode
- o Speeds of 45 ips and 75 ips may be mixed on same MTC

PE Magnetic Tape Controller (MTC9102)

The PE Magnetic Tape Controller offers Level 6 Model 33 and larger model users the capability to attach up to four 9-track magnetic tape units. The units may be either single-density, 1600-bits-per-inch (bpi), phase-encoded units (MTU9114/9115) or they may be dual-density (switchable), 1600-bpi, phase-encoded and 800-bpi NRZI units (MTU9109/9110).

A maximum throughput capability of 120,000 bytes per second is available. Up to four drives of mixed speeds may be attached to a single controller. The controller consists of two printed circuit modules that require two slots on the Megabus of a Level 6 system. All input/output transfers are effected in DMA mode directly to/from main memory via the Megabus.

When an MTC9102 is ordered, the appropriate Device-Pac is included and does not have to be ordered separately. No devices other than phase-encoded tapes may be attached (i.e., unit record devices are *not* attachable via the controller). See Figure 1-13.

The Level 6 MTC9102 tape subsystem is able to read tapes from foreign systems that conform to ANSI standards (i.e., specifically ANSI standard x3.39-1973 and x3.40-1973).

Features

- o Connects up to four 9-track PE tape units
- o Maximum throughput of 120K bytes per second
- o Executes all data transfers in DMA mode
- o Device-Pac included

Multiline Communications Processor (MLC9103)

The Multiline Communications Processor interfaces multiple asynchronous and/or synchronous data communications lines enabling Level 6 Model 33 and larger model users to easily plan and implement a powerful data communications system at a reasonable cost. The primary functions of the MLCP are to provide message delimiting, check-character detection and generation, and editing functions to "off-load" the central processor by reducing the amount of processing required.

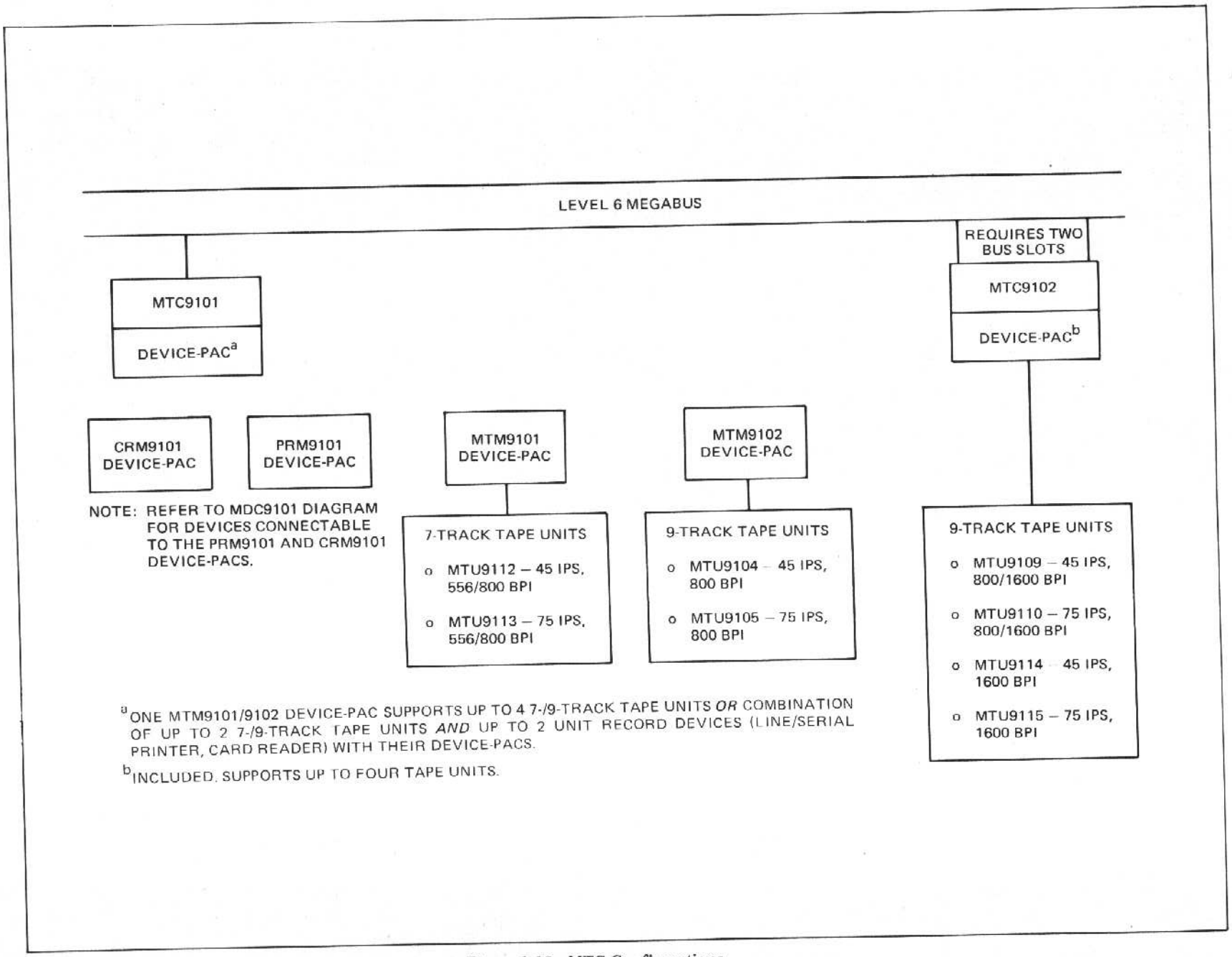


Figure 1-13. MTC Configurations

The Multiline Communications Processor (MLCP) is a programmable communications processor that provides an interface between the Megabus and up to eight full-duplex low- (300 bps or less) and medium- (600 to 10,800 bps) speed lines. Alternatively, four broadband lines can be attached: within the overall throughput limit, each such line may operate at speeds of up to 72,000 bps.

The MLCP is a single primary circuit board; it uses a single interface slot of the Megabus. The MLCP provides the common elements shared by all communications lines. These elements include the firmware-controlled microprocessor, a 4096-byte random access memory (RAM), block-check logic, and the Megabus interface.

Line-specific logic is contained on Communications-Pacs, which plug into the MLCP. Each Communications-Pac connects either one or two lines. Different types of Communications-Pacs can coexist on an MLCP, which has an identical interface to each Communications-Pac. A total of four Communications-Pacs can be plugged into a single MLCP. See Figure 1-14.

Features

- o Maximum subsystem throughput of approximately 16K characters per second
- o User-programmable to provide for message delimiting, message editing, checking of algorithms, etc.
- o 3000 bytes of read/write memory for user programming procedures
- o Instruction set designed specifically for communications processing (43 instructions)
- o Program load of data stream control and configuration data
- o Synchronous/Asynchronous Communications-Pacs (one or two lines/Communications-Pac)
- o Synchronous High-level Data Link Control (HDLC) Communications-Pac (one line/Communications-Pac)
- o Synchronous Broadband Communications-Pac (one line/Communications-Pacs)
- o Assignment of program interrupt levels dynamically
- o Hardware checking (e.g., CRC, LRC, and parity)
- o Individual Direct Memory Access (DMA) for each line and transmission direction
- o Channel control and status information (e.g., underrun/overrun protection)
- o Built-in maintenance aids (e.g., line looping)
- o Auto Call Pacs (two lines/Auto Call Pac)
- o Three specially configured Multiline Communications Subsystems offered

General Purpose Direct Memory Access Interface (GIS9001)

The GIS9001 General Purpose Direct Memory Access (DMA) Interface offers Level 6 Model 33 and larger model users the added capability and flexibility of interfacing special devices. Completely contained on one board is all the necessary interface circuitry, storage, and control logic required to maintain functionality with the system Megabus. The GPI is designed for users who want to extend the capabilities of their Level 6 system or tailor it to special applications.

The General Purpose DMA Interface (GPI) is divided into two distinct areas: an area containing fixed logic providing bus and user interfacing, and an area reserved for user-supplied logic (see Figure 1-15). The GPI operates in Direct Memory Access (DMA) mode and supports a single bidirectional channel. Data to/from the user area is transferred in 16-bit parallel form, controlled by a simple, asynchronous handshake operation. Data transfer between the GPI and the Megabus is also in 16-bit parallel form via DMA control. The data transfer rate from memory to user device (or in the opposite direction) is 500K words per second/1000K bytes per second.

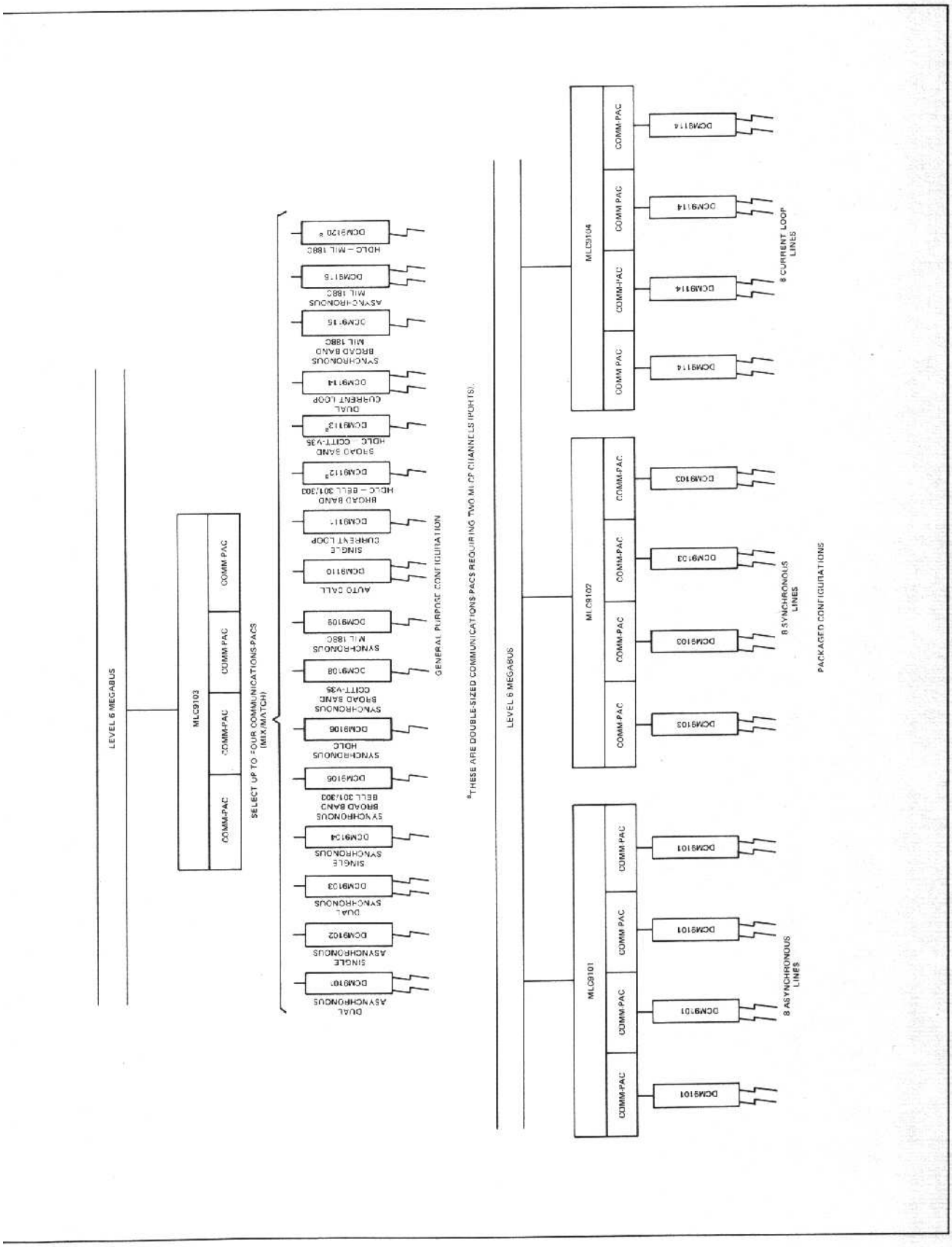


Figure 1-14. MLC Configurations

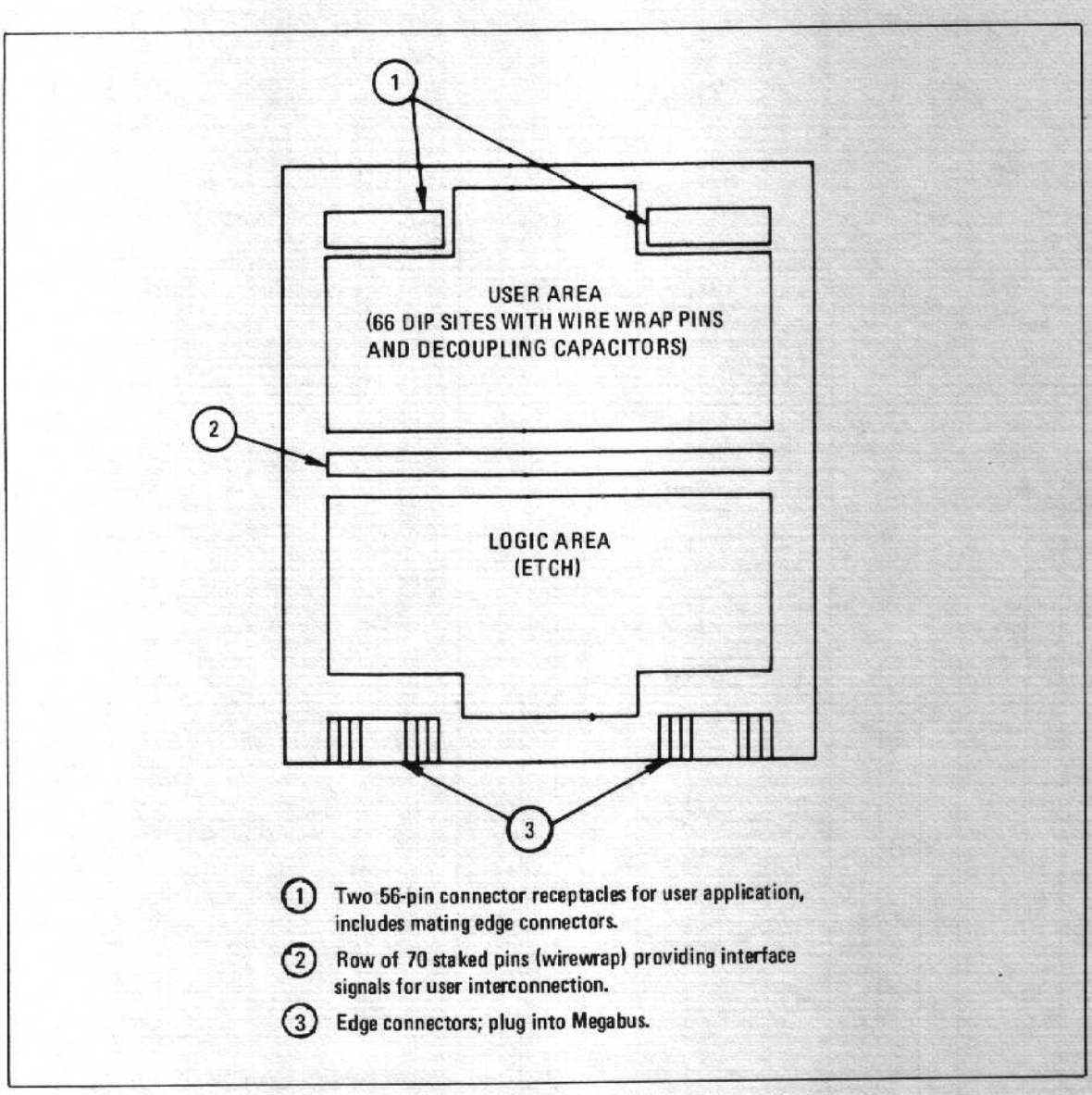


Figure 1-15. Layout of General-Purpose DMA Interface Board

Features

- o Single, compact 15 x 16-inch board contains GPI-logic area and user-logic area
- o Operation in DMA mode, supporting a single bidirectional channel
- o Intermediate data buffering for both input and output operations
- o 66 DIP sites for user-specified logic and two 56-pin connector receptacles for attaching cables to user devices
- o Twelve 16-bit user-specific registers available
- o 70 wirewrap pins that provide GPI logic area to user logic area interface signals
- o CP interrupt capability
- o Software isolation test routines that enable quick, effective fault diagnosis
- o Extender board option available for GPI board debugging

Control Panels

Two types of operator control panels are being offered on Level 6 systems: full and basic. These control panels allow users to choose the amount of flexibility, security, and economy that will best help meet their operational and application requirements. Control panel usage is described in Section 5.

Full Control Panel

Systems being used for program development and testing should be equipped with the full control panel (or basic control panel with the portable plug-in panel option). Full panel functionality is also required for maintenance purposes in systems that do not have a system console (CRT, teleprinter, or keyboard printer).

The full panel allows the CP register and main memory contents to be entered and displayed. It controls, in a step-by-step fashion, the system initialization sequence by single-stepping a program, and stopping and starting program execution. It includes a 7-digit hexadecimal display and a 16-key hexadecimal pad.

Basic Control Panel

The basic control panel[3] is an important feature for customers who do not want their operators at remote locations to be able to modify the software. It is also less expensive than the full panel. As an option to the basic control panel, Honeywell offers a portable plug-in panel. By plugging this unit into the basic panel, full panel functionality is effected. A single portable plug-in panel can support a multitude of systems with basic control panels.

For security, the basic panel does not allow visibility to CP registers or main memory. Its only control capability is to initiate and control the system initialization procedure. This includes clearing the system, running quality logic tests (QLTs), and invoking either automatic restart (if memory contents are preserved) or bootload (if powering up the system initially or if the Memory Save and Autorestart option is not present). Displays indicate gross system status. The basic panel also provides a connector to facilitate interfacing the portable plug-in panel.

Options

- Portable Plug-in Panel[3] – a self-contained, full control panel (Figure 1-16) that can plug into any Model 33, 43, or 47 basic panel. It provides security, economy, and flexibility of operation in multisystem environments.
- Vertical Panel Mounting Option – available for any rackmountable system where physical space limitations exist and replaces the standard inclined panel mounting (Figure 1-17). It is designed for OEMs with their own cabinetry.

[3] Not available on Models 53 and 57.

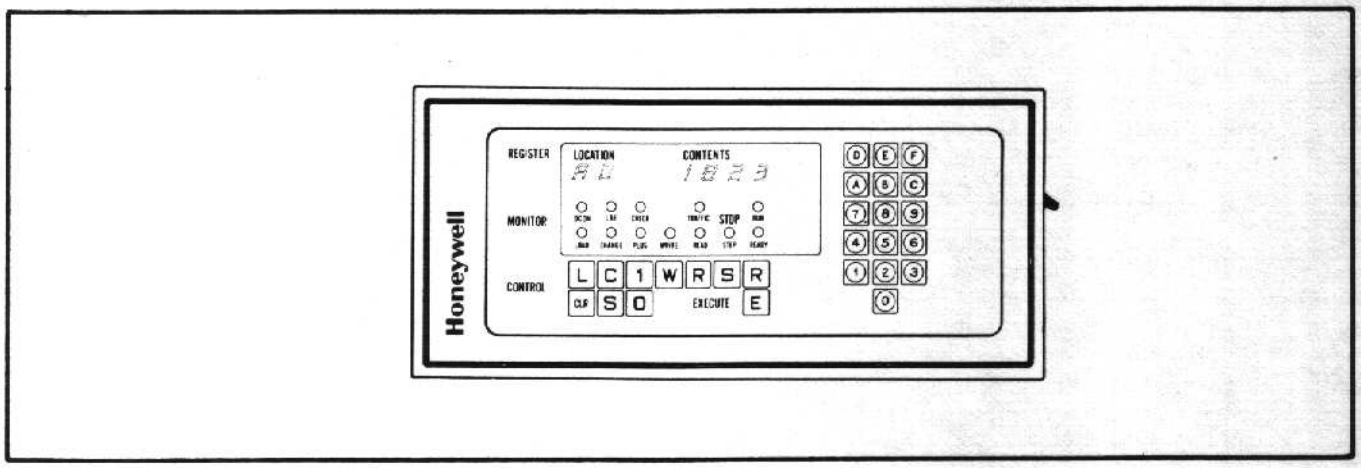


Figure 1-16. Portable Plug-in Panel

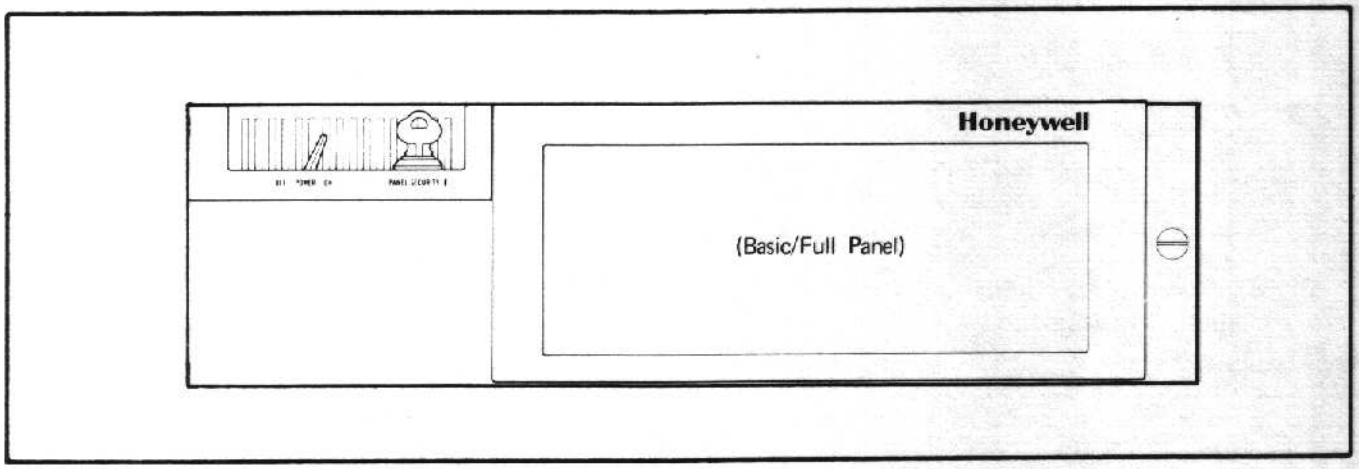


Figure 1-17. Vertical Panel Mounting Option