# ERRATA INFORMATION - PLEASE READ FIRST

## CPU-30 Rev.3 PRODUCT INFORMATION

Dear Valued Customer,

Thank you for choosing to purchase this FORCE COMPUTERS' CPU-30 Single Board Computer.

Please note that for your convenience the jumper setting for the density control of the Floppy disk drive is set to allow a software controlled selection between single or double density read/write operations.

In order to be fully compatible with the previous generation CPU-30 revision 2 boards, the switch 5 must be set to position "ON". This will permanently select the double density operations. Within this mode, the Floppy drive hardware must have an automatic detection possibility of the single density mode. Most of todays drives provide this feature as well. For a detailed description, please refer to CPU-30 Rev.3 User's Manual, Chapter 3.10.2.1 "Disk Density Control".

For additional details, please do not hesitate to consult your nearest FORCE COMPUTERS' office or representative.

Sincerely Yours,

FORCE COMPUTERS GmbH

- Built-in data separator
- Built-in write precompensation
- 128, 256, 512 or 1024 byte sector lengths
- 3 1/2" or 5 1/4" single and double density
- Programmable stepping rate (2 to 6 ms)

### 3.10.1 Address Map of the FDC

The registers of the WD1772 are accessible via the 8 bit local I/O bus (byte mode). The following table shows the register layout of the WD1772 FDC. Additional information is provided in the WD1772 data sheet included in Register No. 5 of this manual entitled "Copies of Data Sheets."

**Table 3-23: WD1772 Register Layout**

| Default I/O Base Address : $FF800000<br>Default Offset : $00003800 | | | | | |
|---|---|---|---|---|---|
| Address HEX | Offset HEX | Mode | Reset Value | Label | Description |
| FF803800 | 00 | R | 7C | FSTR | Status Register |
| FF803800 | 00 | W | -- | FCR | Command Register |
| FF803801 | 01 | R/W | FF | FTR | Track Register |
| FF803802 | 02 | R/W | 01 | FSR | Sector Register |
| FF803803 | 03 | R/W | 00 | FDR | Data Register |

### 3.10.2 Double Density Control

Many floppy disk drives are able to read and write both single density (360K) and double density (720) floppy diskettes. These drives include a high/low density select pin on the interface conector. On some drives, this pin is an input to the drive from the floppy disk controller (FDC) while on others, it is an output from the drive to the FDC. In other words, some drives need to be told which format to use, and others tell the FDC which format it is using based on the diskette that is inserted. In order to support all reasonable combinations of these conditions, the CPU board features two switches to select floppy disk density.

### 3.10.2.1 Disk Density Control Output

The density of the floppy disk drive may be controlled from the CPU board in two ways. Normally, the floppy disk controller (FDC) and the floppy disk drive itself are both controlled by software through the PI/T. However, there is also a unique hybrid method, in which the floppy disk controller and the floppy disk drive are controlled separately.

To control the disk density from the CPU board, PI/T #1 pin PB5 must be programmed as an output. The double density input pin of the WD1772 FDC is then controlled by the level of this pin. When this bit is low ("0") the selection is double density, and when it is high ("1"), then the selection is single density.

| PB5 | Description |
|---|---|
| 0 | Double Density |
| 1 | Single Density |

**It is possible to control the density input pin of the WD1772 FDC and the density input line of the floppy disk drive itself separately, if desired. This is useful if the floppy disk drive does not support the density select signal, or if density select is driven as an output from the drive. To separate the density select signals of the FDC and the drive, a switch at location SW6 must be open. The table below summarizes the options available.**

| SW6-6 | Description |
|---|---|
| Off | Controller, Drive Controlled Separately |
| On | Controller, Drive Controlled Together |

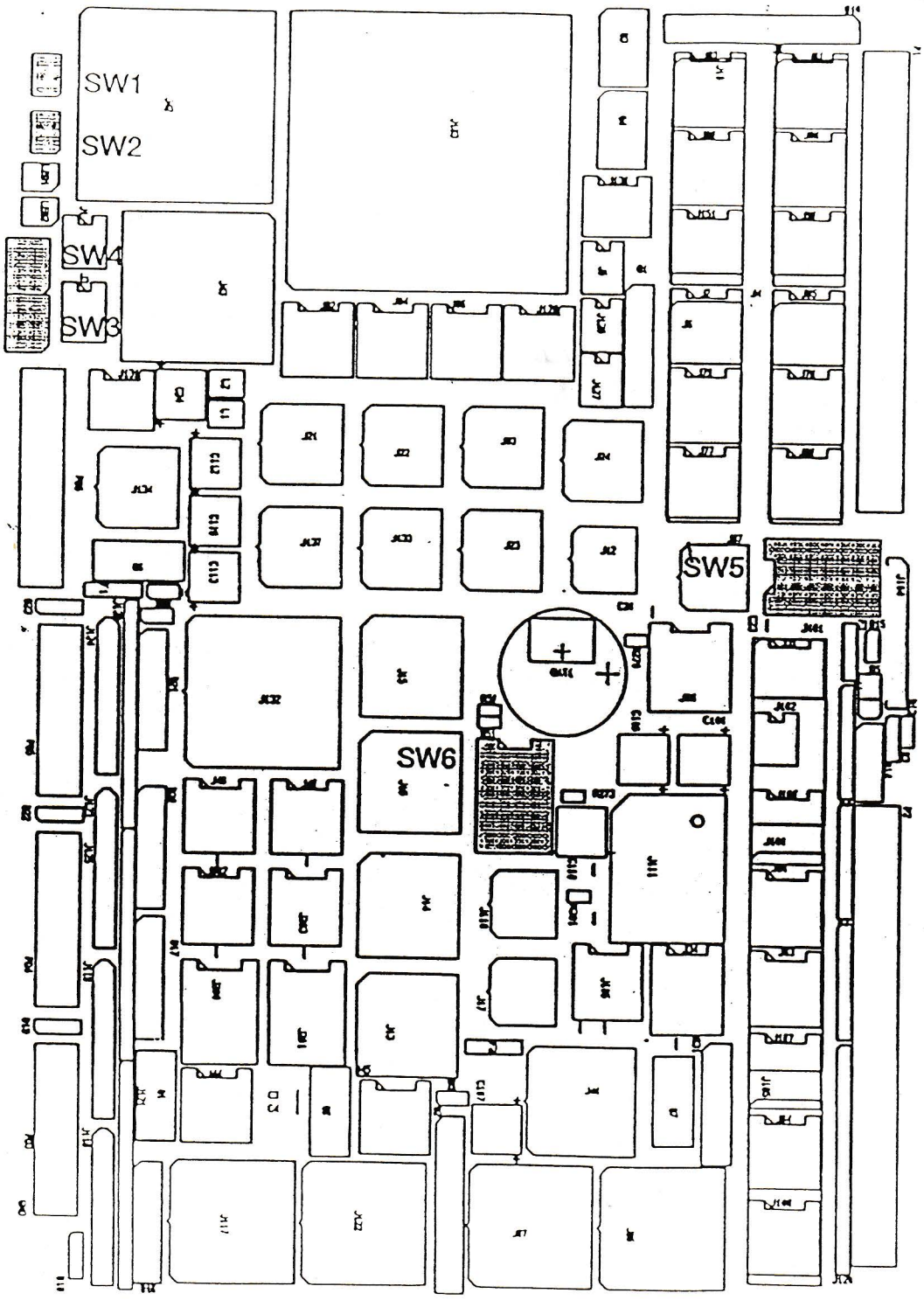
**By default, this switch is off.**

**When switch SW6-6 is in the "Off" position and densities are controlled separately, the FDC will be controlled by the PI/T #1 pin PB5, as above. The floppy disk drive itself will be controlled by another switch at location SW5.**

| SW5-8 | Description |
|---|---|
| Off | Single Density |
| On | Double Density |

When FDC and drive density are controlled together (SW6-6 = "On"), the hardware density switch (SW5-8) must be set to "Off." By default, this switch is off.

Figure 2: Location Diagram for All Switches



Dear Customer,

Following is the Globally/Universally Assigned 48-bit Ethernet Address of your VME/PLUS board that is provided by the IEEE. The accompanying user tutorial gives a description of the implications and use of the address.

Some products have Ethernet address numbers stored in FLASH-EPROM, which are consistent with the description in the related User's Manuals.

The Ethernet address has a general structure which ensures a unique number assignment for every board:

| | |
|---|---|
| **CPU-60** | **0080420D xxxx** |
| **CPU-40B/xx-01** | **00804204 xxxx** |
| | (xxxx = last four digits of the board number) |
| **CPU-30 Family** | **00804203 yyyy** |
| | (yyyy = hex (xxxx + 10000)) |

The board serial numbers are the last four digits of the number printed underneath the bar-code on the products, which is on the VMEbus P1 connector.

**CPU-60 and CPU-40**

For a CU-60 and a CPU-40, the board serial number needs to be added to the above listed board identification number to get the 12-digit Ethernet address for your new FORCE product.

**CPU-30 Family**

For the CPU-30 Family, the above listed offset needs to be added to the board serial number first. The result of the addition needs to be converted into a hexadecimal number. This hexadecimal number added to the above listed identification number is your 12-digit Ethernet address unique for your new FORCE board.

## Discussion of the use of **48-Bit LAN Globally Assigned address block**

The concept of Global/Universal Addressing is based upon the idea that all potential members of a network need to have a unique identification number if they are to exist in a network. The advantage of a Global LAN Address is that a node with such an address can be attached to any LAN network in the world with a high degree of assurance that no other node on that network will share its address. The concept of the 48-bit address scheme originated with Xerox's ETHERNET, and has been taken over by the IEEE committee address assignment protocol methods.

The 48-bit Address is divided into two parts. The upper 24 bits are assigned to FORCE COMPUTERS by the IEEE. The lower 24 bits are uniquely assigned to each board. Unlike the UPC concept used for grocery items which identifies a brand or group of similar priced products by a manufacturer, the lower 24 bits of this address identify each equipment uniquely. There are no two items produced with the same number. The entire purpose of the 48-bit addressing scheme is to provide a unique number/address for each equipment/note.

# VMEPROM

VMEPROM™ is the PDOS® real-time operating system in EPROM. VMEPROM resides on this Force Computer board and provides a complete, real-time operating system run-time environment. VMEPROM includes the PDOS operating system kernel and file manager. It also includes the Force monitor, debugger, and utilities. VMEPROM supports, but does not require, hard disks, floppy disks, and a console terminal.

***VMEPROM Upgrades & Options*** VMEPROM/PXNET™ is available for board-resident Ethernet support and provides Ethernet drivers to support downloading and task to task communication over Ethernet. The VMEPROM on this board implements PDOS version 3.3. To support Ethernet, contact Eyring Corporation for information on the upgrade options which are required for VMEPROM/PXNET. Upgrades are also available from Eyring to support multiprocessing, PC-VME backplane communications, and complete TCP/IP software products.

***PDOS Kernel*** The PDOS kernel is written in 680x0 assembly language for fast, efficient execution. It provides all of the PDOS kernel services including preemptive, prioritized task scheduling; extremely fast, deterministic real-time response; multitasking execution; multiuser capabilities; dynamic Installable System Modules support; floating point support; real-time clock; event processing; and memory management. ***(Continued on reverse side)***

**BY USING VMEPROM YOU SIGNIFY ACCEPTANCE OF THE FOLLOWING LICENSE AGREEMENT**

*Eyring Corporation grants the LICENSEE the non-exclusive right to use the PDOS modules incorporated in VMEPROM and LICENSEE agrees that he will not duplicate or disassemble the firmware and will take reasonable precautions to assure that no other person or entity does so.*

*In no event shall Eyring Corporation be liable for loss of profit, good will, or any special or consequential damages suffered by licensee or any other person, firm, or entity as a result of licensee's use of the licensed software, irrespective of whether such loss of profit, good will, or other special or consequential damages was disclosed to Eyring Corporation or could have been reasonably foreseen by Eyring Corporation.*

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To receive additional PDOS and VMEPROM information, please detach and return this card. Before doing so, please take a moment to answer the following questions. Your answers will enable us to send you information related to your specific requirements. Thank you!

Company _____

Contact _____

Address _____

_____

Phone _____

FAX _____

*1. What host systems will you be developing on?*

PC ___ SUN ___ HP ___ DEC ___ Other _____

*2. Please number your Real-time OS priorities:*

Price ___ Performance ___ Support ___

Development Tools ___ Networking ___

3. For additional information:
Send me literature ____
Place me on your mailing list ____
Have a salesperson contact me ____

***File Manager*** The VMEPROM file manager provides low level disk I/O and basic file services which allow you to access various file storage devices. File access may be performed on a sequential, random, read only, or shared access basis. The file manager module supports multiple RAM or ROM disks. Support for floppy and hard disks is optional, depending on the hardware implementation.

***Application Development*** VMEPROM application development is performed on a number of development host platforms. Application code is downloaded to the target VMEPROM-resident board via Ethernet, serial, or the VMEbus. PDOS development tools include industry recognized compilers, source level and symbolic level debuggers. When development is complete, the application code and a startup file may be placed in a ROM disk for turnkey execution. This configuration allows applications to be downloaded and executed from a host on powerup, rather than burning the application program into EPROM.

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