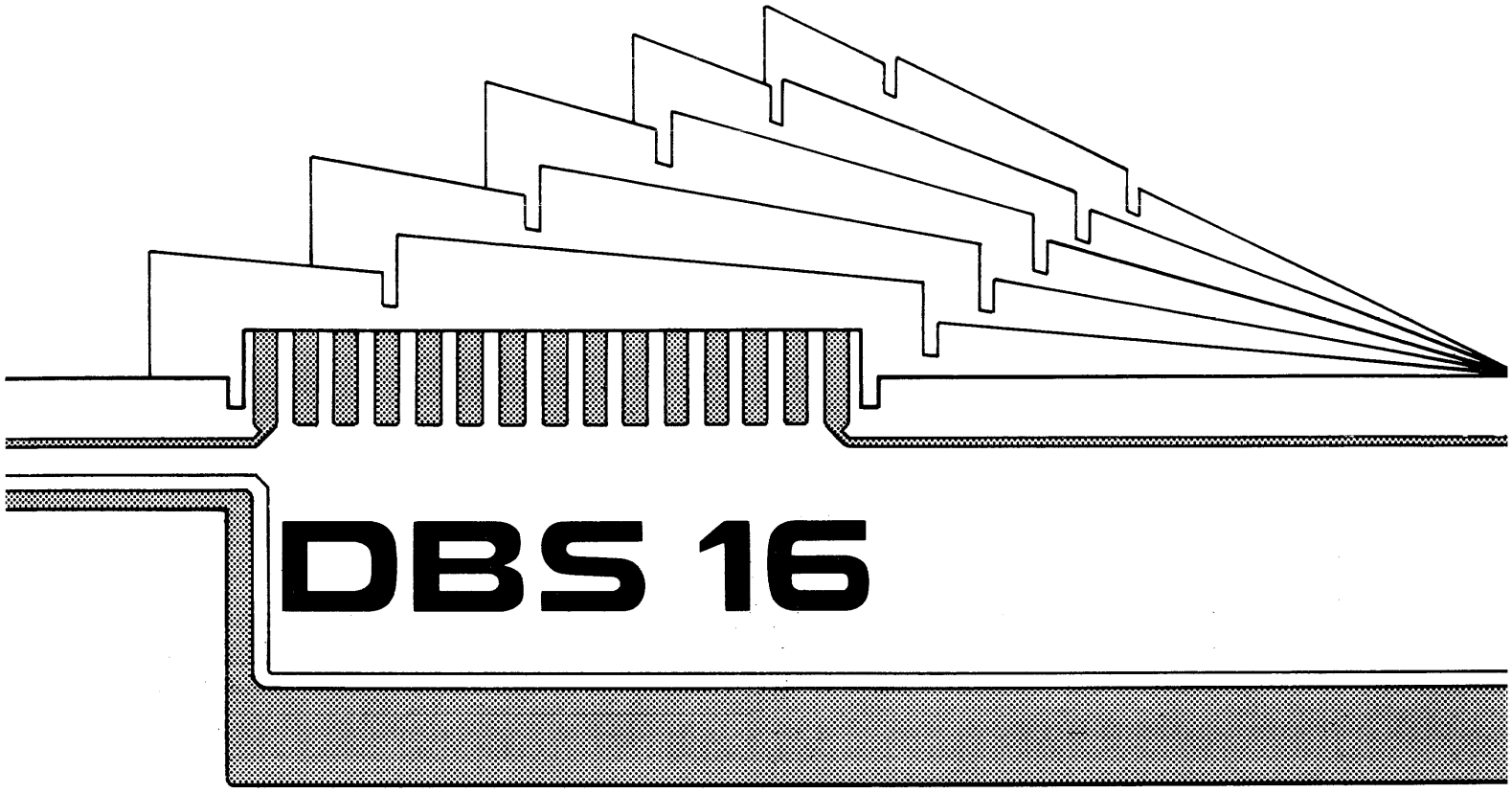

DBS 16

HARDWARE DESCRIPTION AND MAINTENANCE MANUAL

DBS 16

HARDWARE DESCRIPTION AND MAINTENANCE MANUAL

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PREFACE

PURPOSE AND SCOPE

The DBS 16 Hardware Description and Maintenance Manual is intended for use by both the computer electronics technician and the programmer. It is an aid to the technician in repairing the DBS 16 system, and it can help the programmer to customize the system to fit specific requirements.

*** WARNING ***

ONLY TRAINED SERVICE PERSONNEL ARE TO REMOVE THE COVERS OF THE DBS 16 DESKTOP UNIT AND EXPANSION BOX. NON-TECHNICAL PERSONNEL ARE NOT TO ATTEMPT TO MAKE ANY INTERNAL REPAIRS OR CONNECTIONS. PERSONAL INJURY AND/OR DAMAGE TO THE CIRCUITRY MAY RESULT (AND ANY WARRANTY WOULD BE INVALIDATED).

This manual focuses on making repairs at the board or subassembly level, rather than at the chip level. Those wishing to make repairs to the chip level will still find the functional block diagram descriptions helpful, but will need to use the schematic diagrams in Section 4 extensively. No schematics are furnished for the optional Hard Disk Controller and power supplies, because of manufacturer restrictions.

The circuits in two components of the system, the Desktop Unit and the Expansion Box, are explored through the use of functional block diagrams and text. These functional descriptions of the major components will help the technician isolate and identify faults in the hardware system.

Also included as Appendix B of this manual is information on accessing, through the use of software, the various I/O interfaces and memory, to allow for changes in I/O devices and MULTIBUS boards. Instructions on how to install the DBS 16 System, terminals, and peripherals can be found in the DBS 16 User's Manual.

ORGANIZATION OF MANUAL

The material in this manual is basically organized into two self-contained units -- the Desktop Unit (Section 2) and the Expansion Box (Section 3). The two sections are organized identically for cross-referencing, should that be necessary. Sections 1 and 4 contain information common to both components.

The manual is composed of the following sections:

Section 1 - System Overview

This section surveys the major components of the DBS 16 System, their applications and configurations in both the single-user mode and the multi-user mode of up to 28 terminals. A table of specifications is also included for both the Desktop Unit and the Expansion Box.

Section 2 - DBS 16 Desktop Unit

This section covers the DBS 16 Desktop Unit, which contains the master processing unit and supports up to four terminals. When used with the Expansion Box, it acts as the controlling unit for up to 28 terminals. The Desktop Unit also supports serial and parallel printers, or a parallel printer and modem. The section describes the circuitry, lists adjustments and describes routine maintenance, advises on troubleshooting procedure, and explains the repair procedure.

Section 3 - DBS 16 Expansion Box

This section covers the DBS 16 Expansion Box, which, when connected to the Desktop Unit, supports a system of up to 28 users. It allows the user to install standard MULTIBUS cards. The section also describes the function of the circuitry, lists adjustments and describes routine maintenance, advises on troubleshooting procedure, and explains the repair procedure.

Section 4 - Electrical and Mechanical Drawings

This section contains the schematics and parts lists for the Desktop Unit, Expansion Box, and Slave Board.

Appendix A - Connector Pin Lists

This appendix lists all the connectors, their pins, and the signals to be found at each pin.

Appendix B - Programmer's Hardware Reference

This appendix provides information on command sequences used to change operating modes, baud rates, and addresses, to alter the programming of the various devices in the DBS 16 System to accommodate the user's needs. Covered are memory and I/O maps, the Slave Board, Master Board, and MULTIBUS.

Appendix C - DBS 16 Diagnostics Program

This appendix describes the tests included on the diagnostics program diskette and how to use it.

RELATED READING

For further information on the DBS 16 System, contact your computer dealer for copies of these other manuals:

1. DBS 16 User's Manual
2. DBS 16 CP/M-86 System Reference Manual
3. DBS 16 MP/M-86 and DBS-Net Systems Reference Manual

DBS 16 HARDWARE DESCRIPTION AND MAINTENANCE MANUAL

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SECTION 1
INTRODUCTION

1.1 SYSTEM OVERVIEW

The DBS 16 System is a highly flexible business computer system that can serve from one to 28 users. Expanding the system from one to four users merely requires plugging in additional terminals, and using the MP/M-86 and DBS-Net operating system; the DBS 16 Desktop Unit itself requires no added hardware. For a system of from four to 28 users, you connect the Desktop Unit to the top of the DBS 16 Expansion Box, and slide in as many Slave Cards as are necessary to support your additional terminals and expanded memory requirements. The MP/M-86 and DBS-Net operating system is also used in this configuration.

The DBS 16 System uses highly advanced electronic circuitry for optimum speed and power. The operating systems and application software available for the DBS 16 represent the latest in business applications.

Contained within the Desktop Unit are two disk drives. These can be two floppy disk drives, or one floppy and one Winchester drive. The floppy drives are either 48 TPI with 330K bytes or 96 TPI with 780K bytes. The Winchester drive data storage capacity is 5M bytes, 10M bytes, 15M bytes, 40M bytes, or more. The Desktop Unit also concurrently supports a parallel printer and a serial printer, or other device using a serial asynchronous or synchronous interface.

In its basic configuration, the DBS 16 System consists of one terminal (video display terminal and keyboard) connected to the Desktop Unit. Operating systems that can be used in this configuration are CP/M-86 and MP/M-86. See Figure 1-1.

Should up to four terminals be needed, they are simply plugged into the Desktop Unit, and MP/M-86 is the operating system used. The printers or printer and modem operate as before. See Figure 1-2.

Figure 1-1. Single-User Configuration

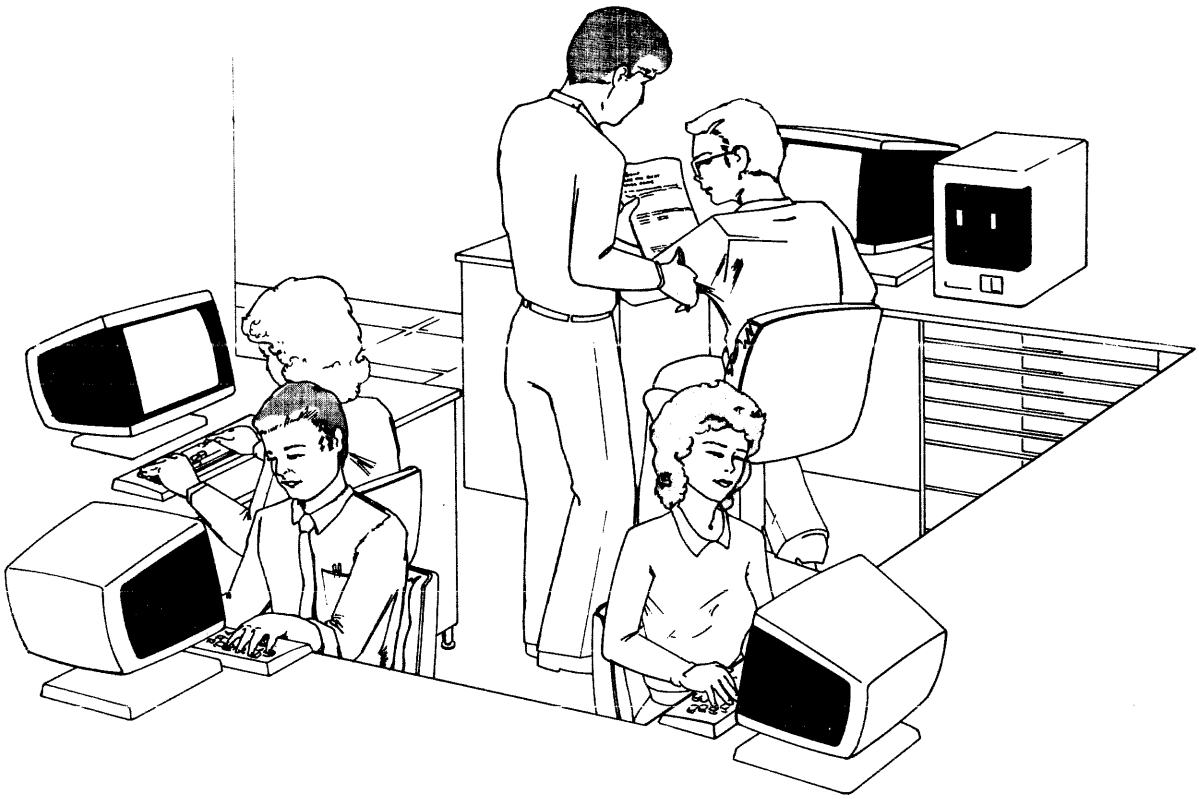


Figure 1-2. Multi-User, Single Processor Configuration

For a system involving more than four users, or to make use of the many MULTIBUS boards available, you add the DBS 16 Expansion Box to your system. The DBSI Slave Cards (available from your dealer) enable the addition of terminals. Each Slave Card can support up to four terminals. The maximum number of terminals that can be used with the system is 28, divided among the Desktop Unit and six Slave Cards (the maximum number of MULTIBUS slots in the Expansion Box).

When you are using a DBSI Slave Card, you must use the DBS-Net operating system. See Figure 1-3.

The Expansion Box is extremely useful, even when you are operating four or fewer terminals, because of the wide variety of MULTIBUS-standard boards (available from your dealer and other sources) that can be used. If you install other MULTIBUS-standard cards, software changes will be required to integrate operation in the system. This software is available from your dealer.

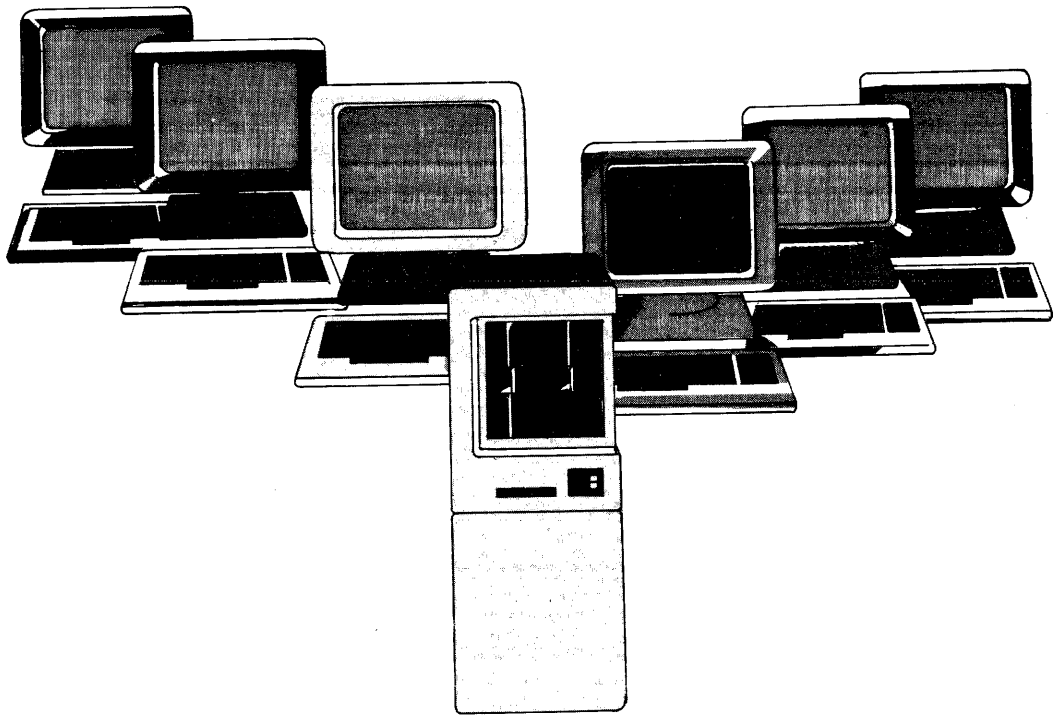


Figure 1-3. Multi-User, Multi-Processor Configuration

The Desktop Unit comes with a standard RAM memory of 256K bytes; an optional expansion board can add another 256K bytes. Each Slave Card for the Expansion Box also contains a standard 256K bytes; you can connect an optional expansion board to bring the total memory available to the terminals using the Slave Card to 512K bytes.

The following table lists the physical and functional characteristics of the DBS 16 System components:

Table 1-1. DBS 16 System Specifications (Part 1 of 3)

DESKTOP UNIT		
Physical Characteristics	Width:	9-1/8 inches
	Height:	12 inches
	Depth:	15 inches
	Weight:	Approx. 30 lbs., depending on drives
Power	Voltage:	115 V/220 V
	Frequency:	60 Hz/50 Hz
	Consumption:	Approx. 120 W
Software	CP/M-86, MP/M-86 (single user) MP/M-86 (1-4 users) MP/M-86 and DBS-Net (4-28 users) Assembly Language: 80186	
Microprocessor	Type:	80186
	Word Size:	16 bits
	Speed:	8 MHz
Memory	Type:	Dynamic RAM
	Size:	256K bytes standard (additional 256K bytes optional)
Mass Storage	Type:	5-1/4 inch Winchester hard disk
	Maximum Number of Drives:	1 as option
	Data Format:	Soft sector
	Data Area:	5M, 10M, 15M, 40M bytes, or more
	Transfer Rate:	5M bps

Table 1-1. DBS 16 System Specifications (Part 2 of 3)

Backup Storage	Type:	5-1/4 inch floppy disk drive
	Number of Drives:	1 or 2
	Data Format:	Soft sector
	Data Area:	780K for 96 TPI 330K for 48 TPI
	Transfer Rate:	250K bps
Parallel Printer Interface	Type:	8-bit
	Transmission Speed:	Greater than 2000 cps
	Printers Supported:	Centronics-compatible, NEC, Okidata, etc.
Serial Interface	Type:	RS-232C/CCITT V.24
	Mode:	Asynchronous/Synchronous
	Transmission Speed:	Up to 19,200 bps
	Printers Supported:	Serial RS-232C compatible
Terminal Interface	Type:	SDL (Shielded Data Link) serial ports
	Number:	4
	Mode:	Asynchronous
	Transmission Speed:	Up to 9600 bps

EXPANSION BOX		
Physical Characteristics	Width:	9-1/8 inches
	Height:	12 inches
	Depth:	15 inches
	Weight:	Depends on number of boards
Power	Voltage:	115 V/220 V
	Frequency:	60 Hz/50 Hz
	Consumption:	Less than 150 W
Interface	Type:	MULTIBUS standard 86-pin
	Capacity:	6 slots
Memory	Type:	Static RAM
	Size:	4K bytes
DC Power Available	Power:	130 W maximum +5 V at 15 A +12 V at 4 A -12 V at .7 A

Table 1-1. DBS 16 System Specifications (Part 3 of 3)

SLAVE CARD		
System Interface	Type:	MULTIBUS standard 86-pin
Microprocessor	Type:	80186
	Word Size:	16 bits
	Speed:	8 MHz
Memory	Type:	Dynamic RAM
	Size:	256K bytes standard (additional 256K bytes optional)
Terminal Interface	Type:	SDL serial ports
	Number:	4
	Mode:	Asynchronous
	Transmission Speed:	Up to 19,200 bps
Power Required	+5 V at 2 A	
	+12 V at 50 mA	
	-12 V at 50 mA	

SECTION 2
DBS 16 DESKTOP UNIT

2.1 GENERAL

This section looks at the DBS 16 Desktop Unit. It explores the groups of electronic circuitry that accomplish specific tasks. Each paragraph refers to a sheet of the schematics found in Section 4. For example, paragraph 2.1.2.1 on the Master Board CPU is keyed to Sheet 2 of the Master Board schematics.

The major subassemblies of the Desktop Unit are illustrated by Figure 2-1.

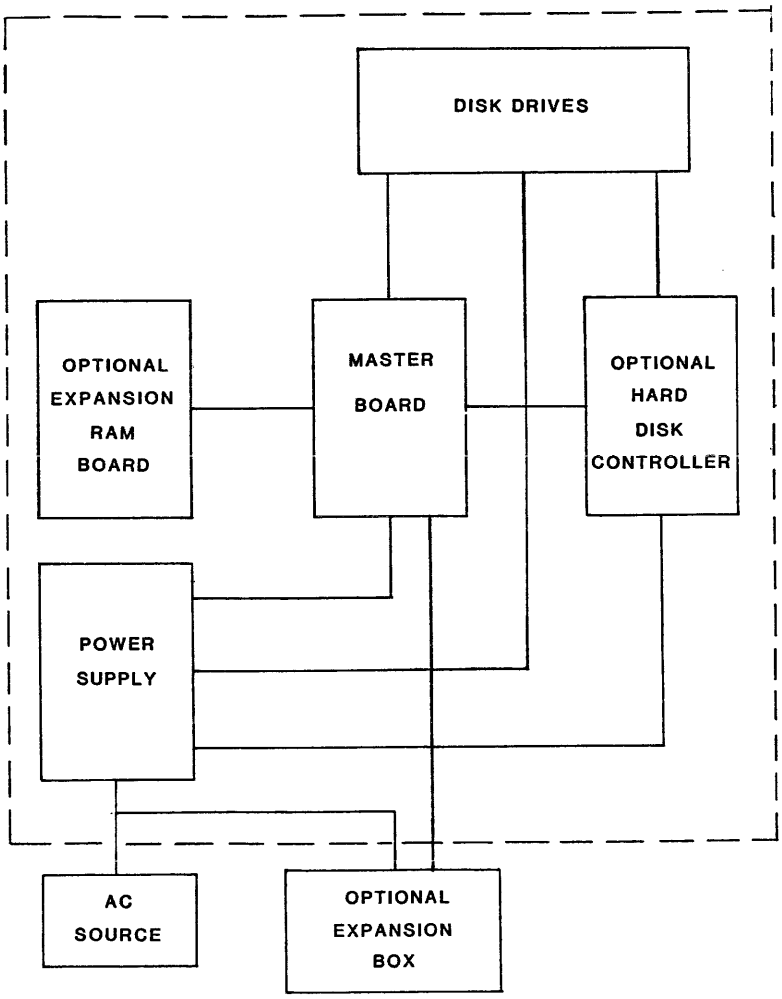


Figure 2-1. Desktop Unit: Major Subassemblies

The Desktop Unit subassemblies are:

- Power Supply
- Master Board
- Optional Expansion RAM Board
- Optional Hard Disk Controller
- Optional Hard Disk Drive
- Floppy Disk Drive

These subassemblies, except for the optional Hard Disk Drive and the Floppy Disk Drive, are the subjects of functional block diagram descriptions. The disk drives are not included because the type and the source of the drives can vary. Following the descriptions of the other subassemblies are paragraphs on adjustments, routine maintenance, troubleshooting, and disassembly.

*** WARNING ***

NEVER INSTALL ANY BOARDS WHILE THE POWER IS ON. DO NOT OPERATE THE UNIT WITH ANY OF THE SUBASSEMBLIES DISCONNECTED.

If your system is equipped with a Winchester drive, remember that it is a delicate piece of equipment, like any other hard disk drive. Care should be taken when the unit is moved.

2.1.1 Power Supply Circuit Functions

The Desktop Unit Power Supply is rated at 100 W, and for this application supplies +5 Vdc, +12 Vdc, -12 Vdc, and ground for the logic, I/O, and power to the disk drives.

NOTE

Although voltage settings on the DBS 16 are labeled 115V and 220V, the unit is also compatible with, and operable at, 110 Vac and 230 Vac.

When the Voltage Selector switch is set to 115V, the unit can operate in the range from 90 Vac to 132 Vac. When the Voltage Selector switch is set to 220V, the unit can operate in the range from 180 Vac to 264 Vac.

Features of this power supply include:

- Choice of 115 Vac or 220 Vac input
- Short circuit protection
- Overvoltage protection on the +5 Vdc output
- Input surge current protection
- 20 KHz minimum switching frequency

The ac power line is also passed down to the bottom of the Desktop Unit for connection to the Expansion Box, if that unit is attached.

The maximum allowable ripple on any output is 50 mV. The nominal voltage and maximum output current on the outputs are as follows: Output 1, 5 V, 10 A; Output 2, +12 V, 4 A; Output 3, +12 V, 1.5 A; Output 4, -12 V, 0.7 A.

2.1.2 Master Board Circuit Functions

The Master Board is a four-layer printed circuit board that contains all the circuitry to provide the following five basic functions:

1. Central Processing Unit (CPU)
2. RAM Memory
3. Input/Output
4. Hard Disk Controller Interface
5. MULTIBUS Interface

Figure 2-2, a functional block diagram, shows the interrelationship of the Master Board components.

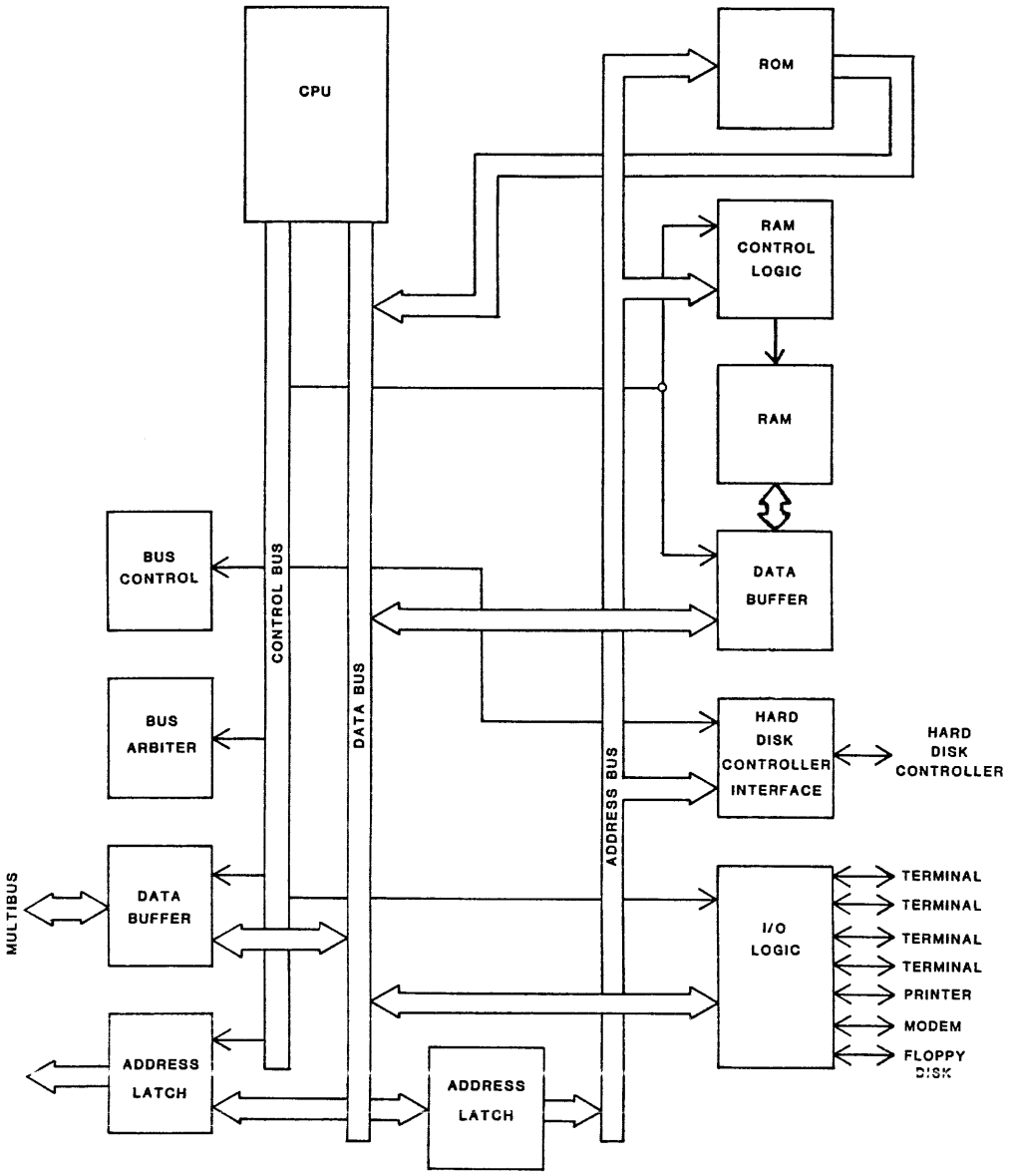


Figure 2-2. Master Board Functional Block Diagram

2.1.2.1 Master Board CPU

When the Desktop Unit is used in the single processor, multi-user configuration, the processor acts as the CPU for all terminals. In the multi-processor configuration, the Desktop Unit processor acts as a controller for the slave processors in the Expansion Box.

This description of the CPU area of the Master Board is keyed to Sheet 2 of the Master Board schematics in Section 4. The principal integrated circuits of this part of the logic are: one 80186 microprocessor, two 8259A Programmable Interrupt Controllers, and two 2732 PROMs. Figure 2-3 shows the interrelationship of these components.

The 80186 is a 68-pin microprocessor that uses a 16-bit time-multiplexed data/address bus. An additional four address lines are used, for a total of 20, allowing the addressing of one million locations. During the first pulse of the clock, T1, information on the bus is treated as an address and is latched into the address latches. For the next three clock pulses (T2, T3, T4), the information on the bus is treated as data. The microprocessor has a crystal input of 16 MHz, which is internally reduced to a clock pulse of 8 MHz for operations.

Control signals generated by the 80186 are: S0-S1, bus cycle status lines to Bus Arbiter; CSEXP, chip select expansion RAM; CSRAM, chip select RAM; CSROM, chip select ROM; DT/R, data transmit or receive (low) to control direction of data flow; DEN, data enable of data bus transceiver output; BHE, bus high (D8-D15), enable; M/IO, memory or input-output (low); ALE, address latch enable; LOCK, lock out other system bus masters; PCS0, enable I/O; PC2-3, Programmable Interrupt Controller (PIC) enables; PCS4, SCSI enable; INTA0-INTA1, interrupt acknowledges to PICs; RD, read; and WR, write.

Input signals to the 80186 are: INT0-INT1, interrupt requests from PICs; CLKIN, a 16 MHz clock; ARDY, asynchronous ready signals that a data transfer can and will take place; SRDY, synchronous ready signals ROM read will take place; DRQ0, direct memory access request; and RES, reset.

Depending on the software, the DBS 16 can use either polling or interrupts to determine when peripheral devices require service. When interrupts are used, the sources of these interrupts are:

- ACE (1-4) INT from terminals
- BUS (A-F) INT from the Expansion Box
- FDCINT from the floppy disks
- HDCINT from the Hard Disk Controller
- PTRINT from the printer
- TXINT from the serial port
- RXINT from the serial port
- PARITYINT onboard RAM
- EXPINT from the Expansion RAM Board

These 17 signals are reduced to two by the 8259A Programmable Interrupt Controllers (PIC), one from each. These signals are received by the CPU as INT0 and INT1. The CPU then internally determines priority between these two signals.

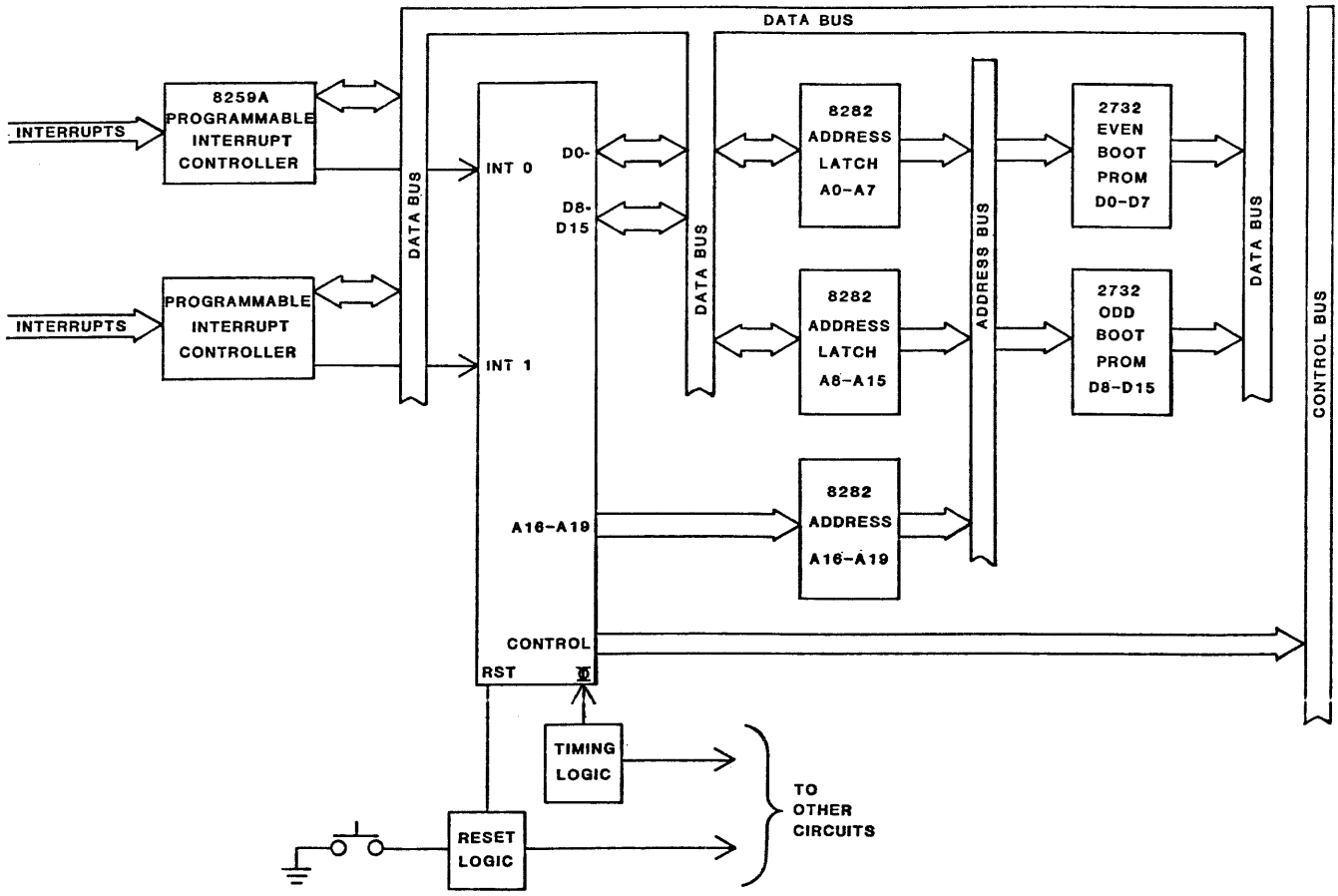


Figure 2-3. Master Board CPU Functional Block Diagram

The 8259A PIC has an 8-bit bi-directional data bus to receive programming, transmit status, and send vectoring data to the CPU. It can receive up to eight interrupt requests that it reduces to one interrupt that goes to the CPU. It then receives an interrupt-acknowledge from the CPU when the interrupt request is to be serviced. The PIC has one address line plus chip select to enable the read and write lines.

Two 2732 PROMs provide 8K bytes of "booting" or initializing instructions. The "even" PROM supplies D0-D7 and the "odd" PROM supplies D8-D15 of the instructions needed to load the "bootstrap" program from Track 0 of the disk drive. The bootstrap program then loads the "loader" program from the disk, which loads the operating system.

2.1.2.2 Master Board RAM Control and RAM

The memory on the Master Board is the standard 256K bytes of dynamic RAM, complete with RAM controller circuitry. This paragraph is keyed to Sheets 3 and 4 of the Master Board schematics. Figure 2-4 is a functional block diagram of this portion of the circuitry.

The DBS 16 uses an 8203 RAM Controller to interface with its array of thirty-six 64K RAMS. The 8203 receives address lines A0-A17, plus read, write, and chip select. It also receives a 25 MHz clock. It outputs row address lines, column address strobe lines, row address strobe lines, and write enable.

The RAM chips are arranged in four rows of nine 64K bit chips. This arrangement yields two complete sets of words, a high and a low set. Each word consists of two 8-bit bytes plus a parity bit for each byte. This yields a 256K byte dynamic RAM memory onboard the Master Board. An optional board can add another 256K bytes. That board, which is similar to this area of the Master Board, is covered in paragraph 2.1.3.

The output of the RAMs is latched into two 8282 tri-state octal latches, and the parity bits are latched into a 74LS75 quad latch. Data to be written into the RAMs passes through two 74LS244 octal buffers.

Any time data is read by the CPU, it is checked for parity. The 16 bits of data plus the two parity bits are fed into two 74LS280 odd/even parity checkers/generators. At this point, if the parity of both words is odd, a parity error signal is generated. Parity is generated whenever data is being written into RAM.

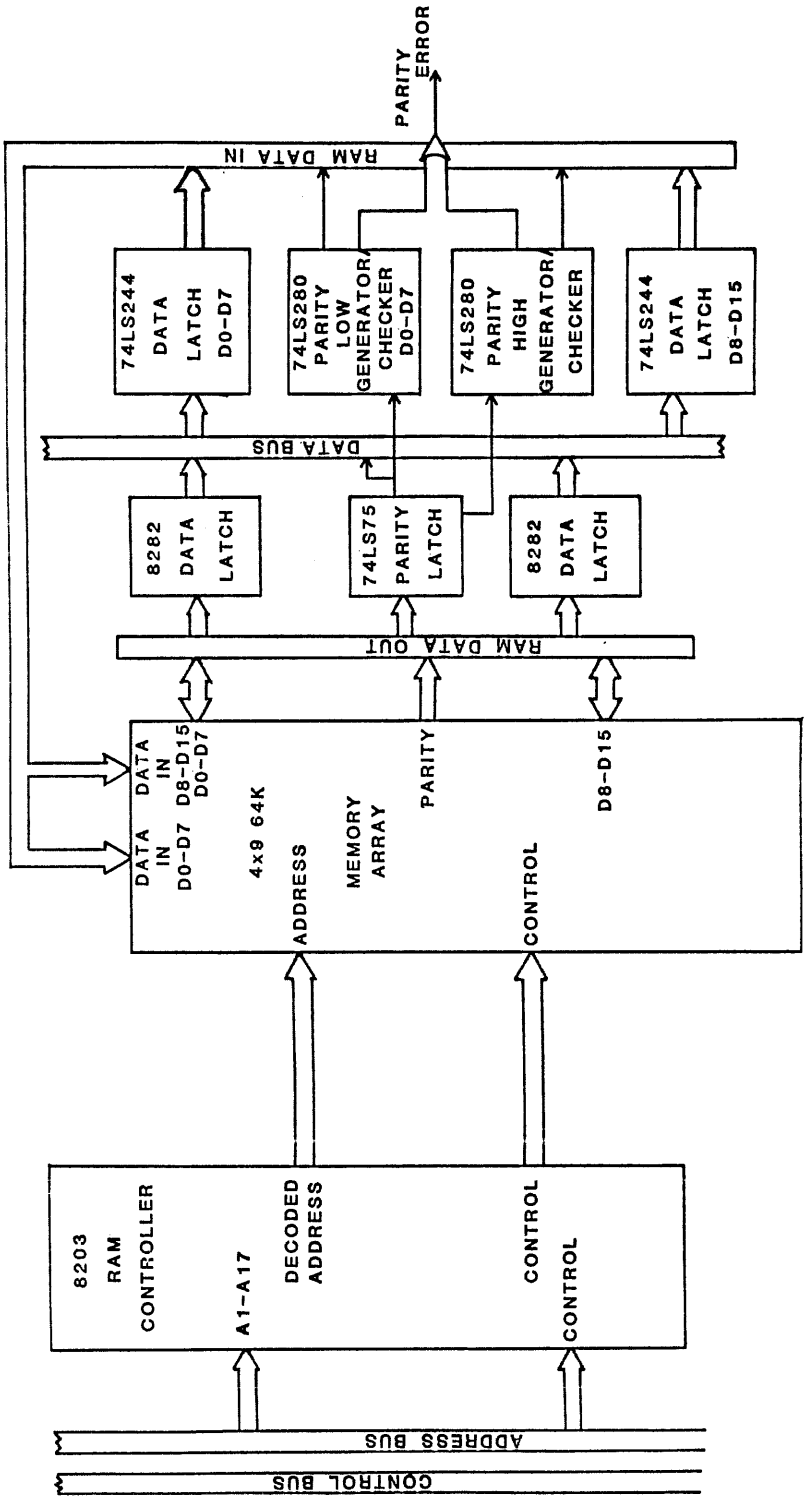


Figure 2-4. Master Board Memory Functional Block Diagram

2.1.2.3 Master Board Input/Output (I/O)

This paragraph is keyed to Sheet 5 of the Master Board schematics. Figure 2-5 is a functional block diagram of the I/O section of the Master Board.

The I/O operations are, for the most part, controlled by seven chips. They include: four 8250 Serial I/O Controllers for the terminals, an 8255A Programmable Peripheral Interface for the parallel output-only port, an 8251A Programmable Communication Interface for the synchronous/asynchronous serial port, and a 1793 Dual Floppy Disk Control.

All are enabled by chip select lines with signals from a 74LS138 three-to-eight line Decoder/Demultiplexer. Further addressing is carried out by three peripheral address lines. Other signals from the CPU are Read, Write, and Reset. All have 8-bit data busses from the system data bus. Each device generates its own interrupt request signal.

The first chips, the 8250s, are connected to the terminals by SDL (Shielded Data Link) four-pin connectors on the Desktop Unit end of the four-wire cable and DB-25 connectors on the terminal end. The 8250 has an 8-bit parallel data bus for I/O on the CPU side, and communicates serially with the terminals.

The 8250s use the 2 MHz clock and a software-controlled division factor to set their internal baud rate generators. These asynchronous ports support a baud rate of up to 9600, and transmit five, six, seven, or eight data bits. Odd, even, or no parity systems may be used.

The next I/O chip, the 8255A, has several functions. The chip is programmable, and has three separate 8-bit ports. One port is used for parallel output only to a printer. It is connected by a D-shell 15-pin connector. It has a maximum transmission speed in excess of 2000 characters per second and is TTL compatible. This interface can be used with Centronics, NEC, and other compatible printers.

The second port on the 8255A is used to read eight switches for configuration instructions. Switch 8, for example, determines which drive the system uses for booting. Refer to paragraph 2.2.1 for a complete listing.

The third port is used for control. Three of the eight lines in this bus provide strobe, acknowledge, and fault indication for the printer port. Two lines are head-select and drive-select for the floppy drives. Another line is the clock-select line for the asynchronous/synchronous serial I/O port circuitry described in the following paragraph.

The next I/O chip, the 8251A Programmable Communication Interface, takes the parallel data from the CPU and converts it to a serial stream for transmission to a printer or modem, and vice versa. A low level on the clock-select line from the Programmable Peripheral Interface causes the Communication Interface to use the output from an 8116 Baud Rate Generator, and a low level uses external clock inputs. The output of the 8116 Baud Rate Generator is software-determined. Between the two methods, a transmission and reception rate of up to 19,200 bits per second is possible.

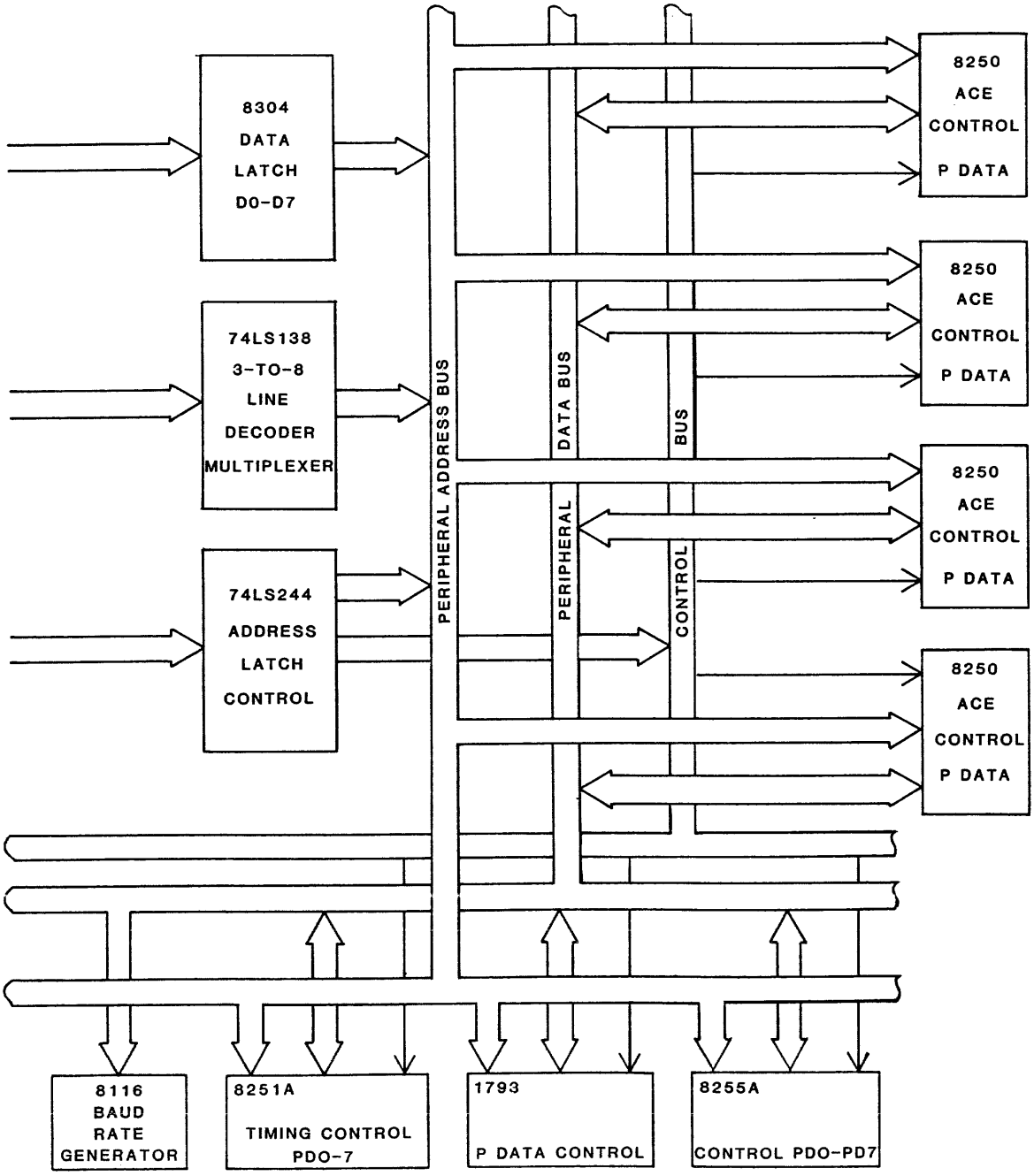


Figure 2-5. Master Board I/O Functional Block Diagram

This asynchronous/synchronous port uses an RS-232 standard D-shell 25-pin connector. It can transmit five, six, seven, or eight data bits with odd, even, or no parity. It features a full set of modem flags.

Finally, there is the 1793 Floppy Disk Controller, which controls one or two floppy disk drives. It is supported by a 9229 Floppy Disk Interface circuit.

The 1793 controls loading of the read/write heads, manages disk formatting, performs seek operations, and handles data transfers between memory and magnetic disk. The 1793 uses +12 V in addition to a +5 V supply. No inputs and outputs, however, ever exceed +5 V or ground.

The 9229 Floppy Disk Interface Circuit provides digital data separation, write precompensation logic, and head load timing. This device is strapped in this application to interface with a 5-1/4" disk drive and a 1793 Floppy Disk Controller.

The data separation logic, despite its name, does not actually separate the raw data from the clock pulse with which it is combined in the serial stream coming from the disk. It does adjust the frequency and phase of another clock pulse to the pulse embedded in or combined with the data, and uses this new pulse to strobe the raw data into the 1793. The purpose of the clock is to form a "frame" or "window", in the center of which a high pulse is written or a low is maintained to represent data.

The strapping of the 9229 provides a precompensation value of 125 nanoseconds for tracks 0-43, and 250 nanoseconds for tracks 44-79.

The other task of the 9229, head load timing, inserts an 80 millisecond delay between the time the Head Load signal becomes active and the Head Load Timing signal is activated, to ensure that the read/write head has had time to properly engage the disk surface.

2.1.2.4 SCSI Interface

Major interface circuitry for the SCSI Interface of a Hard Disk Controller consists of three 74LS244 octal buffers, a 74LS373 tri-state octal latch, a 74LS280 parity checker/generator, and a 74LS138 three-to-eight line Decoder/Demultiplexer. This paragraph is keyed to Sheet 6 of the Master Board schematics. Figure 2-7 is a block diagram of the circuitry.

The SCSI Interface sends and receives data between the CPU and the Hard Disk Controller Board via an 8-bit data bus. In addition, there are status and command signals to and from the controller and CPU. The purpose of this circuitry is to provide signal compatibility between the Master Board and the Hard Disk Controller.

Data going to the Hard Disk Controller is latched into a 74LS373 tri-state latch, and data coming from the controller is passed through a 74LS244 buffer. Only D0-D7 are used for data; D8-D15 are used for control. D8 and D9 serve as control bits from the CPU to the Hard Disk Controller. D10-D15 are controller status signals from the Hard Disk Controller to the CPU.

Figure 2-6 shows the relationship of these signals as they would appear on an oscilloscope.

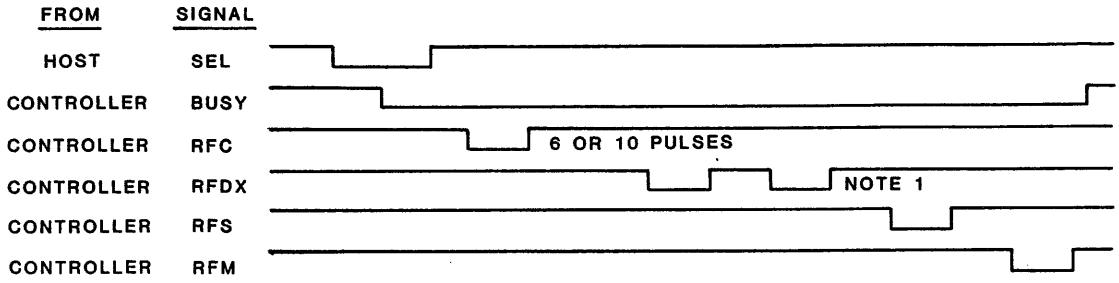


Figure 2-6. SCSI Wave Forms

The operation of the SCSI bus follows this sequence:

1. The computer sets the target address (of the controller) and the Select line. The controller responds with BUSY.

2. The computer then turns off SELECT, and the controller sets the RFC (ready for command) line.

3. The computer then sends the first byte of the command. The controller, after receiving this byte, resets the RFC line, and the computer sends the next command byte. This continues until all command bytes are received (typically six bytes).

4. The controller then sets RFDO (ready for data out) if it is a data transfer from the computer to the controller, or RFDI (ready for data in) if it is a transfer from the controller to the computer.

5. The computer then sends or reads the data bytes as the command indicated. When the transfer is complete, the controller sets RFS (ready for status).

6. The computer then reads the status byte and checks for errors. The controller then sets RFM (ready for message).

7. The computer then reads the message byte which is always all zeroes. The controller then turns off the BUSY line. The operation is now completed.

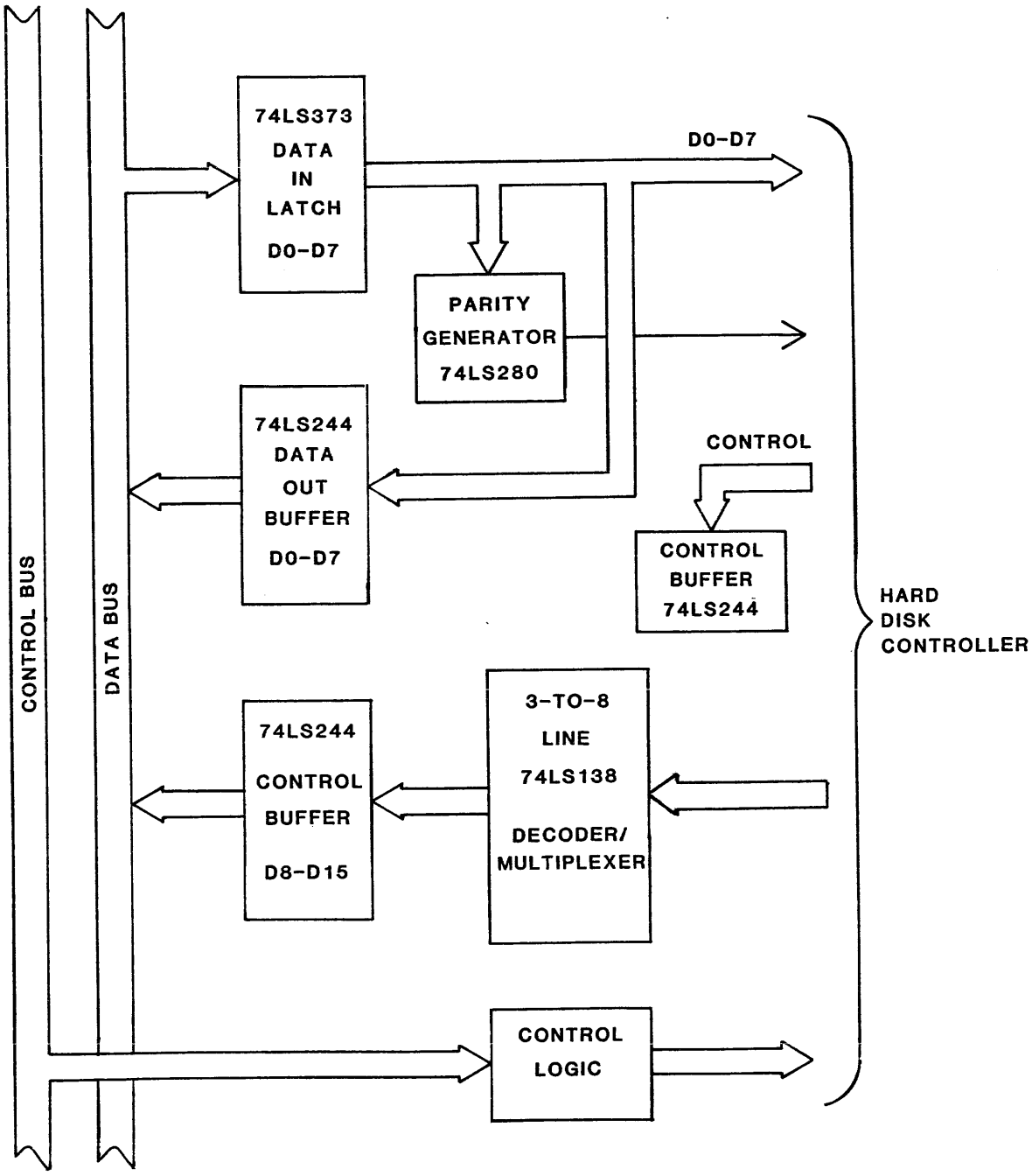


Figure 2-7. Master Board SCSI Functional Block Diagram

2.1.2.5 MULTIBUS Interface Circuit Functions

The MULTIBUS interface circuitry allows communication with the logic boards in the Expansion Box. This paragraph is keyed to Sheet 7 of the Master Board schematics. Figure 2-8 is a block diagram.

There are two methods of inputting and outputting data between the Master Board and the MULTIBUS in the Expansion Box, through the use of three 8303 bi-directional transceivers.

A 16-bit word is sent in parallel (first method) when one 8303 passes data bits D0-D7 onto the D0-D7 data bus, and another 8303 passes data bits D8-D15 to the D8-D15 data bus.

The third 8303, however, can pass data bits D8-D15 onto the D0-D7 data bus. Of course, data bits D0-D7 and D8-D15 are gated onto the D0-D7 data bus at different times. Through a second method, known as "swapping bytes," D0 through D7 are multiplexed so the low order byte, followed by the high order byte, can be sent over the same portion of the bus.

The second method allows the DBS 16 to be connected to other systems using 8-bit microprocessors, or 16-bit microprocessors using 8-bit data busses.

Addresses derived from the data bus during T1 clock pulse are latched into two 8283 inverting octal latches, while a third 8283 latches address lines A16-A19.

The MULTIBUS is controlled by an 8288 Bus Controller and an 8289 Bus Arbiter. The 8288 Bus Controller provides MULTIBUS command signals based on what it receives from the CPU status lines and its control input lines. Output of the chip also includes address latches, data transceivers, and interrupt control signals.

The 8289 Bus Arbiter, which is transparent to the CPU, intercepts CPU commands and presents a "not ready" status to the CPU until the Bus Arbiter acquires the use of the multi-master system bus. Once use is acquired, the 8289 allows the Bus Controller, data transceivers, and the address latches to access the system. The Bus Arbiter functions as a multiplexer between bus masters.

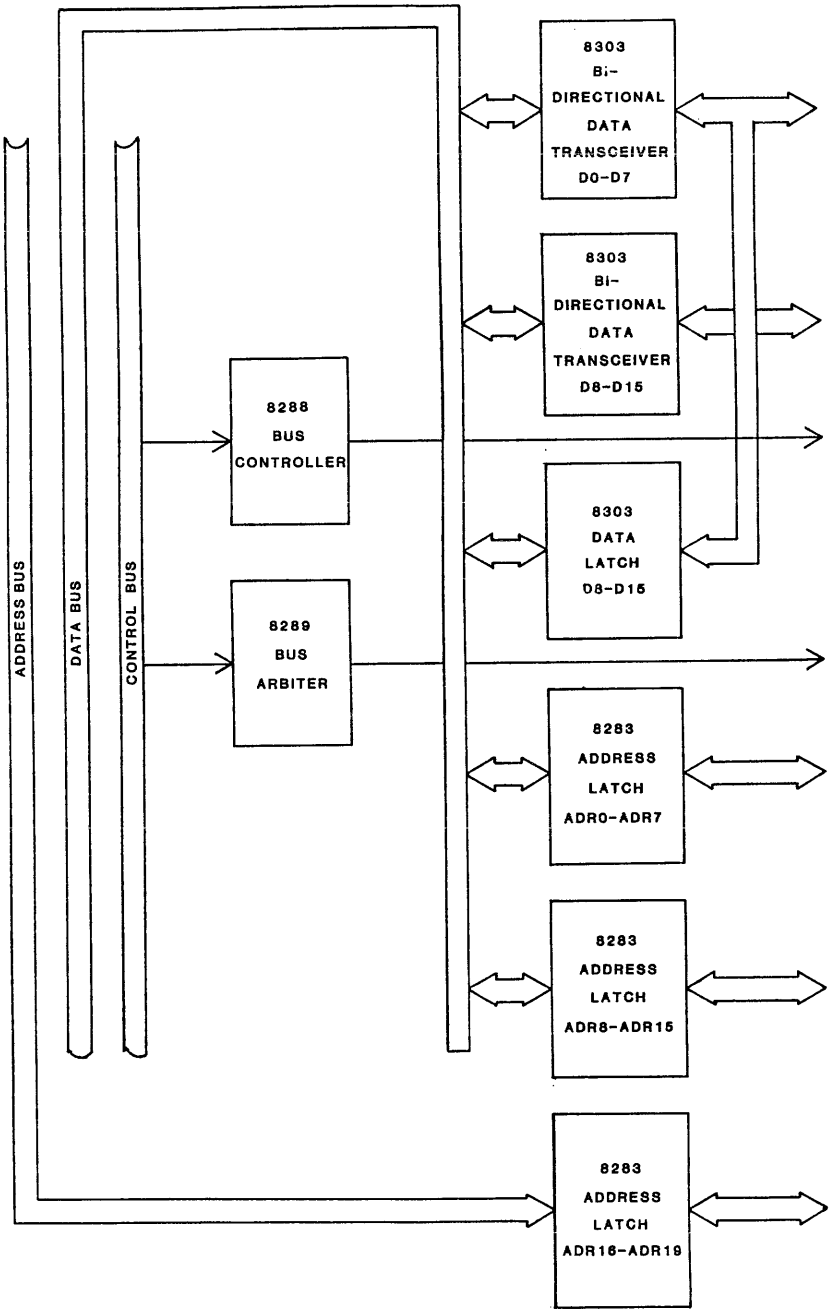


Figure 2-8. Master Board MULTIBUS Interface Functional Block Diagram

2.1.3 Expansion Board Memory Circuit Functions

The optional Expansion RAM Board circuitry is identical to the RAM circuitry on the Master Board (paragraph 2.1.2.2), except that CSEXP (Chip Select Expansion) is used instead of CSRAM to enable the 8203 RAM Controller on the Expansion RAM Board. This paragraph is keyed to Sheets 2 and 3 of the Expansion Board schematics.

The Expansion Board also contains 256K bytes of dynamic RAM controlled by an 8203 RAM Controller. Arrayed in four rows of nine 64K bit chips, the board outputs and inputs two 8-bit bytes per word, plus a parity bit for each byte. Output of the RAMs is latched into a 74LS75 quad latch, and data to be written in is passed through 74LS244 octal buffers. Parity is generated when data is written, and checked when it is read.

2.1.4 Hard Disk Controller Circuit Functions

The Hard Disk Controller board directs all communications and control signals between the hard disk drive and processor. This board also provides data buffering and error correction functions for the hard disk drive.

This board controls an ST506/412 or compatible 5-1/4 inch Winchester Disk Drive with a data transfer rate of 5 megabits per second. Parameter definition in the Hard Disk Controller is related to the type of hard disk drive being used, and is software-controlled. The parameters include such information as the maximum number of cylinders and number of heads.

On this board are jumper locations for determining bytes per sector and parity enable. In the first case, the choice is between 512 bytes per sector/18 sectors per track, or 256 bytes per sector/33 or 32 sectors per track (depending on the controller installed). The DBS 16 uses 256 bytes per sector.

The other jumper either enables or disables odd parity. This controller uses odd parity, so this jumper must be installed to enable parity checking and generation. Specific instructions for installing these jumpers are given in paragraph 2.2.1.

When this device is selected, both the Select line and Data Bus bit 0 go low, then the Busy signal goes low to acknowledge selection. The Request line goes low after the Select line goes high again to receive commands.

Schematics and details of the circuitry of this board are not available for publication because of manufacturer restrictions.

2.2 ADJUSTMENTS AND ROUTINE MAINTENANCE

2.2.1 Switch Settings

Internally, an 8-position DIP switch on the Master Board is provided to allow a variety of configurations. The switch location is shown in Figure 2-9.

At present, only switch 8 has been assigned a function. When this switch is ON, the system boots from floppy drive A in a two-floppy system. In a floppy and Winchester configuration, switch 8 in the OFF position causes the system to try booting from the floppy drive and then, if it fails to find a loader-type program, try the Winchester. If it fails to find a loader program on that drive, it continues to switch back and forth between the floppy and the Winchester. If switch 8 is in the ON position, the system attempts only to access floppy drive A.

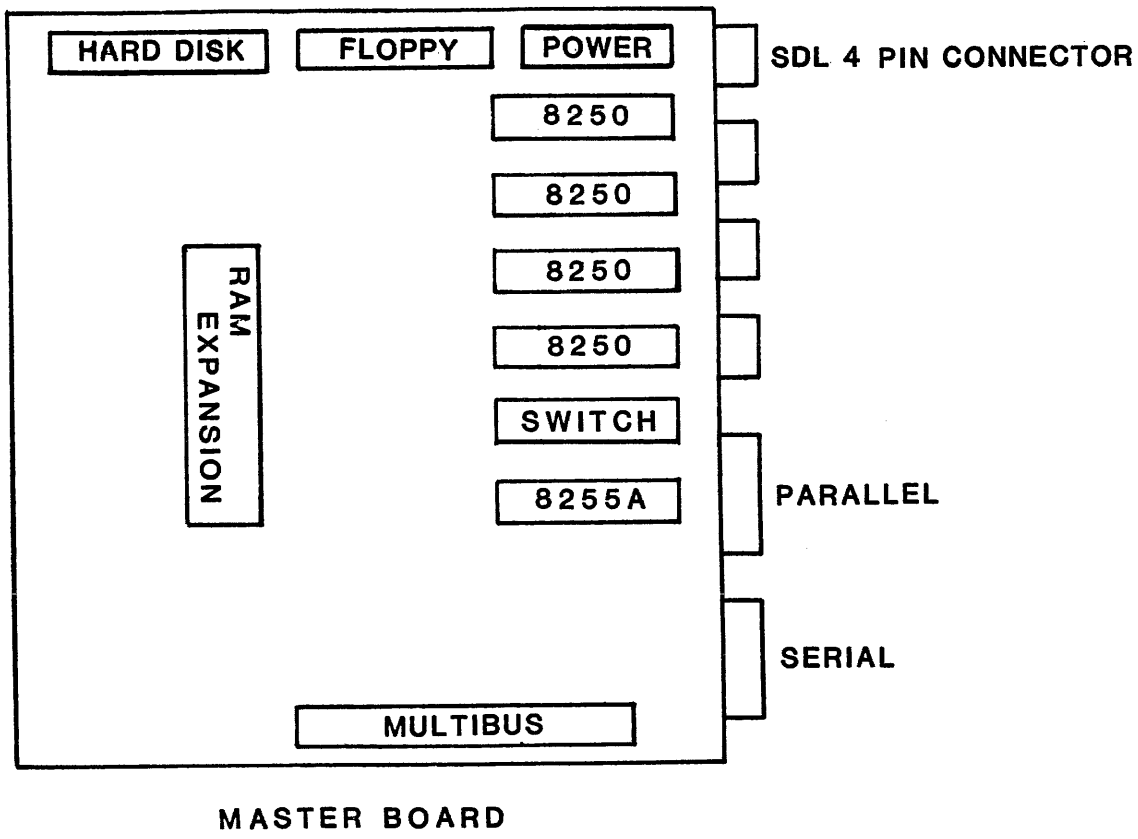
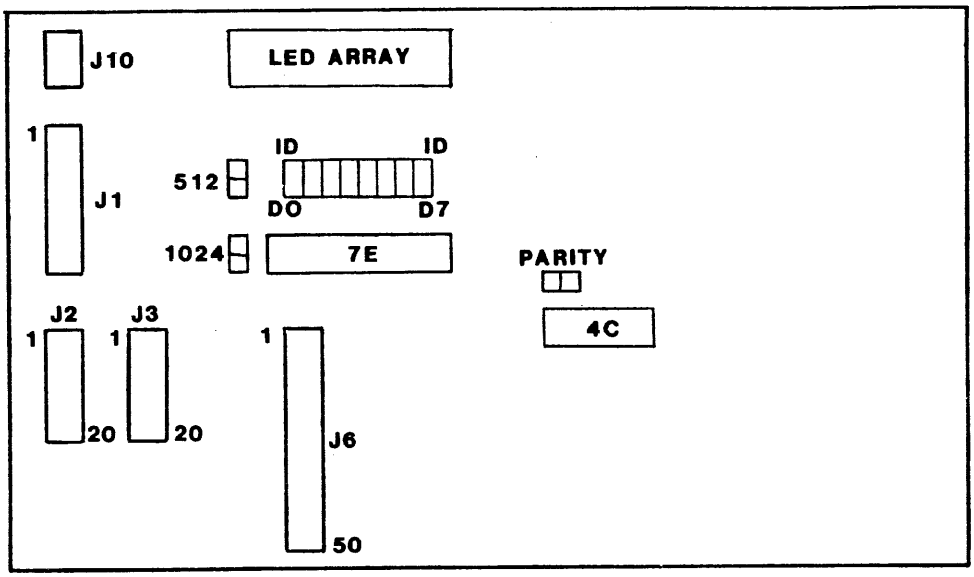


Figure 2-9. Master Board Switch Location

There are three jumper locations (see Figure 2-10) on the optional Hard Disk Controller. No connection should be made at W1. This sets the system at 256 bytes per sector and 33 sectors per track.

Jumper W2, when connected between A and B, enables parity checking and generation. When connected between B and C, it disables parity. Both the Master Board and the Hard Disk Controller Board must be operating in the same mode, so the connection should be made between A and B. Jumper W3 must always be installed.



J1.....DRIVE CONNECTOR CABLE

J2,J3..DRIVE RADIAL CABLE

J6.....HOST CABLE

J7.....NO CONNECTION

J10....DC POWER

Figure 2-10. Hard Disk Controller Jumper Location

External switch settings include setting the line voltage selector switch at the back of the Desktop Unit. The switch in the "up" position is for 95-135 Vac, and in the "down" position is for 198-250 Vac. The ON/OFF power switch is on the front panel of the Desktop Unit. The remaining switch is a pushbutton Reset switch which, when pressed, provides master reset, reinitializing the system.

2.2.2 Routine Maintenance

Because the Desktop Unit has no moving parts except the drives, routine preventive maintenance merely involves keeping the unit and its environment as clean as possible, and protecting the unit from impact. To keep the system trouble-free, be sure there is sufficient space around the Desktop Unit to allow proper ventilation.

Do not attempt to clean the disk drives, because damage to the heads and circuitry could result.

2.3 TROUBLESHOOTING

2.3.1 Environmental Problems

Although the DBS 16 Desktop Unit is a rugged and reliable piece of equipment, certain environmental conditions must be met to ensure trouble-free operation. Refer to Sections 2 and 3 of the DBS 16 User's Manual for detailed installation and power-up procedures.

The site should be clean and relatively dust-free to prevent data loss on the disks and fouling of the drive mechanism.

Also, allow approximately one foot of space behind the Desktop Unit for proper ventilation and cable connections. Excessive heat build-up can result in unreliability of the electronics, so room temperature should be kept at about 73 degrees Fahrenheit (23 degrees Celsius), although the system will operate in the range of 50 to 95 degrees Fahrenheit (10 to 35 degrees Celsius). Humidity must be controlled within a range of 20% to 90% and, again, the closer to mid-range the better. To guard against accidental disconnection of the terminals or printer, care should be taken to relieve any mechanical strain on the cables or their connectors.

To prevent glitches or induced currents, do not place the Desktop Unit near any strong electrical or mechanical energy sources, such as CB transmitters or large electric motors. When in operation, the Desktop Unit may cause interference with radio and television reception, and should not be placed near such appliances. Power cords should be as widely separated from signal cables as possible.

Be sure that the line voltage at the wall receptacle corresponds to the fuse and switch selection on the rear panel of the Desktop Unit. Plug the unit into a three-prong wall outlet that has been properly grounded. Be sure the proper fuse (2 A, 250 Vac, slow blow) is installed in the rear panel of the Desktop Unit. Again, check the DBS 16 User's Manual for original installation instructions.

*** WARNING ***

(FCC Rule 79-556 14687 Appendix B)

THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND IF NOT INSTALLED AND USED IN ACCORDANCE WITH THE INSTRUCTIONS MANUAL, MAY CAUSE INTERFERENCE TO RADIO COMMUNICATIONS. IT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR CLASS A COMPUTING DEVICES PURSUANT TO SUBPART J OF PART 15 OF FCC RULES, WHICH ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINST SUCH INTERFERENCE WHEN OPERATED IN A COMMERCIAL ENVIRONMENT. OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE INTERFERENCE IN WHICH CASE THE USER AT HIS OWN EXPENSE WILL BE REQUIRED TO TAKE WHATEVER MEASURES MAY BE REQUIRED TO CORRECT THE INTERFERENCE.

(This warning is quoted here and posted on each unit as required by Federal law.)

2.3.2 Problem Isolation

Whenever the system is malfunctioning, check first to see that the proper operating system is being used and that it has not been corrupted. To do this, use a backup copy of the operating system.

The purpose of this manual is to isolate problems to the subassembly, not the individual chip on a board. Therefore, effort should be concentrated on tracing signals from one board to another. When a subassembly is suspected of being faulty, it should be removed and replaced with a known good subassembly. An oscilloscope and a multimeter are required to troubleshoot this system.

Good troubleshooting techniques apply here as with any system. Check the obvious (but often overlooked) first. Make sure the unit is plugged in at both a good outlet and the backpanel, and check the fuse. Make sure the circuit serving the DBS 16 System is not overloaded. Ask the operator to demonstrate technique, to show the problems encountered. Operator error could be the problem. A RAM test is conducted each time the Desktop Unit is powered up.

If the problem cannot be detected externally, then open up the unit to look at the internals. Remember proper safety procedures. Be sure the power is off when removing any subassembly, and never try to operate the system with any part disconnected. This could reduce the total resistance in the circuit, and cause unacceptably high currents in other parts of the system.

Cable assemblies are another often overlooked problem source. Check both ends of a cable to see if the signals are consistent from origin to destination. Also, make sure the cable connections and the edge connectors are good. The edge connectors can become oxidized, and a simple cleaning often solves the problem.

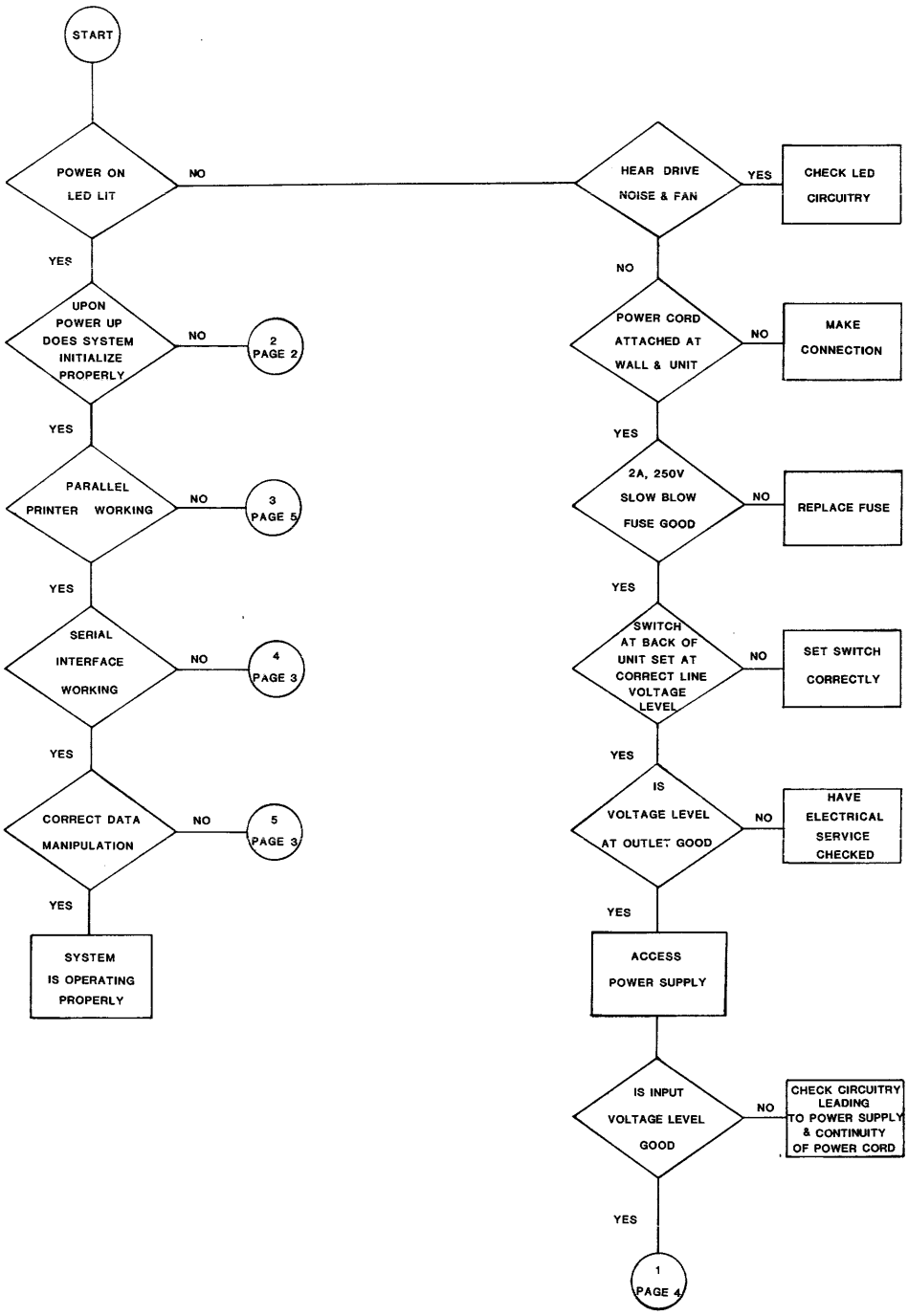


Figure 2-11. Problem Isolation Flowchart (Part 1 of 5)

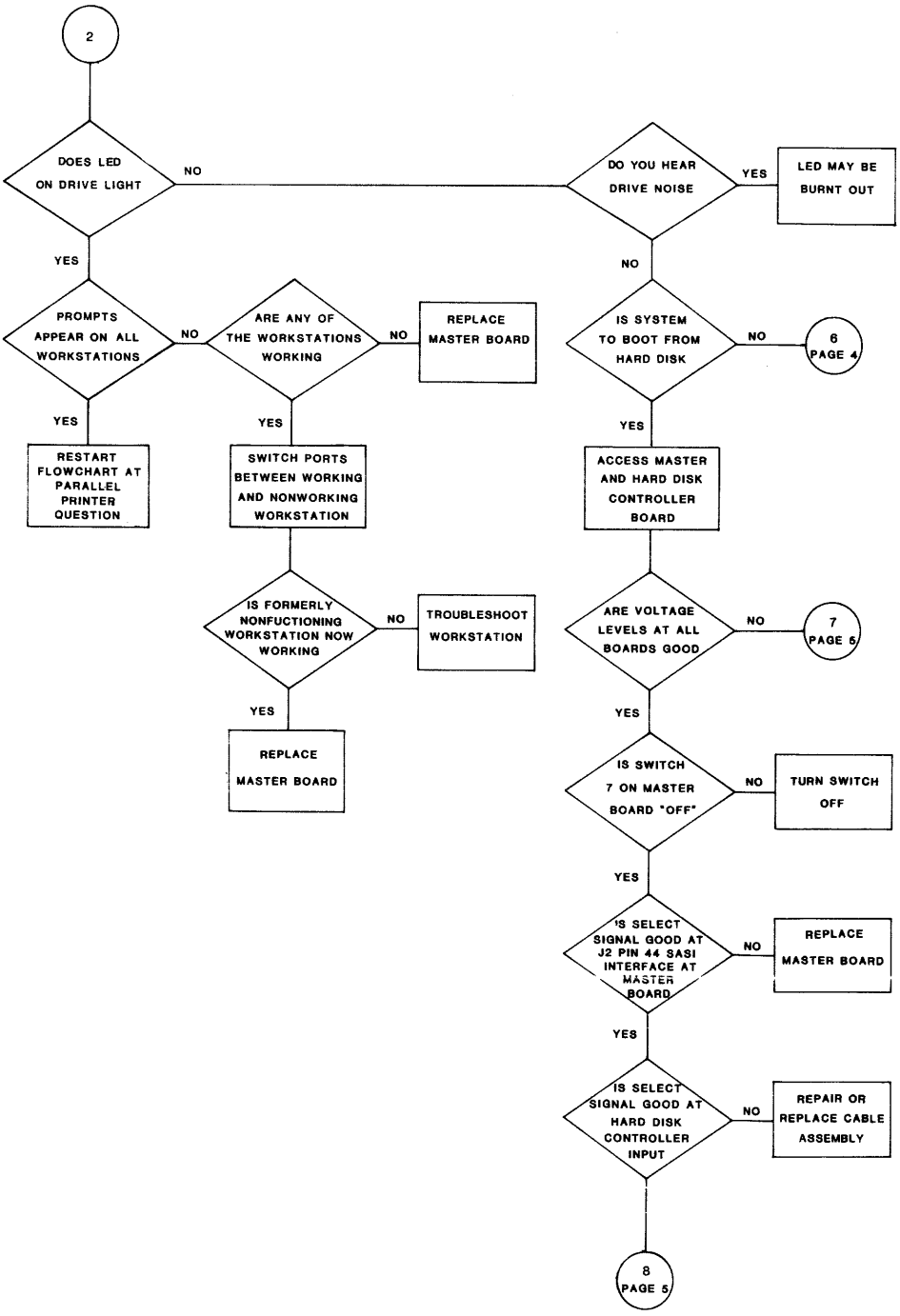


Figure 2-11. Problem Isolation Flowchart (Part 2 of 5)

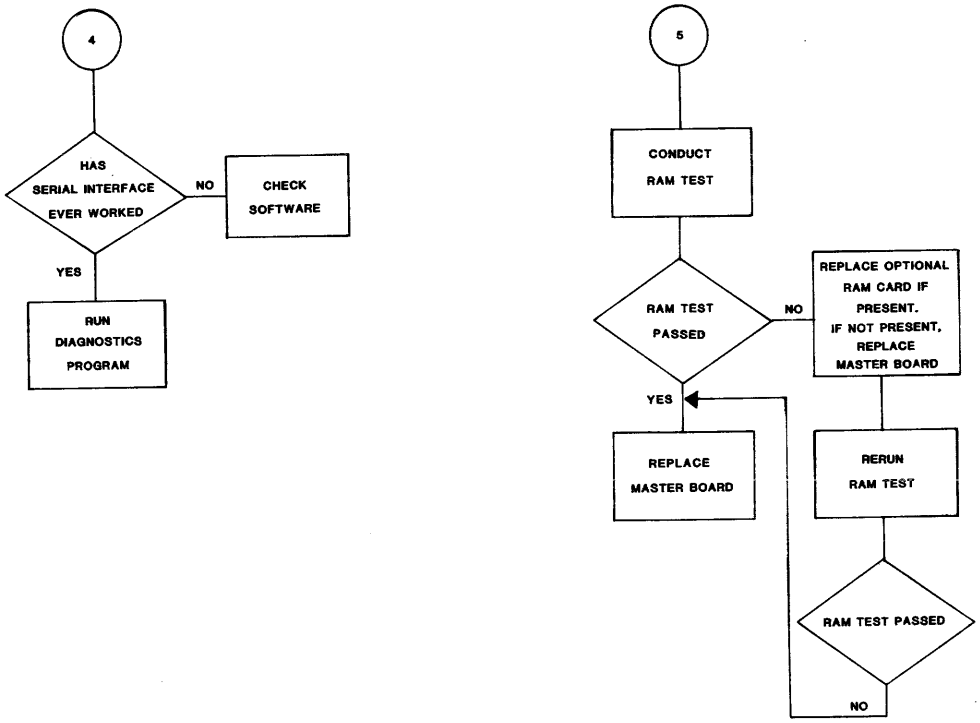


Figure 2-11. Problem Isolation Flowchart (Part 3 of 5)

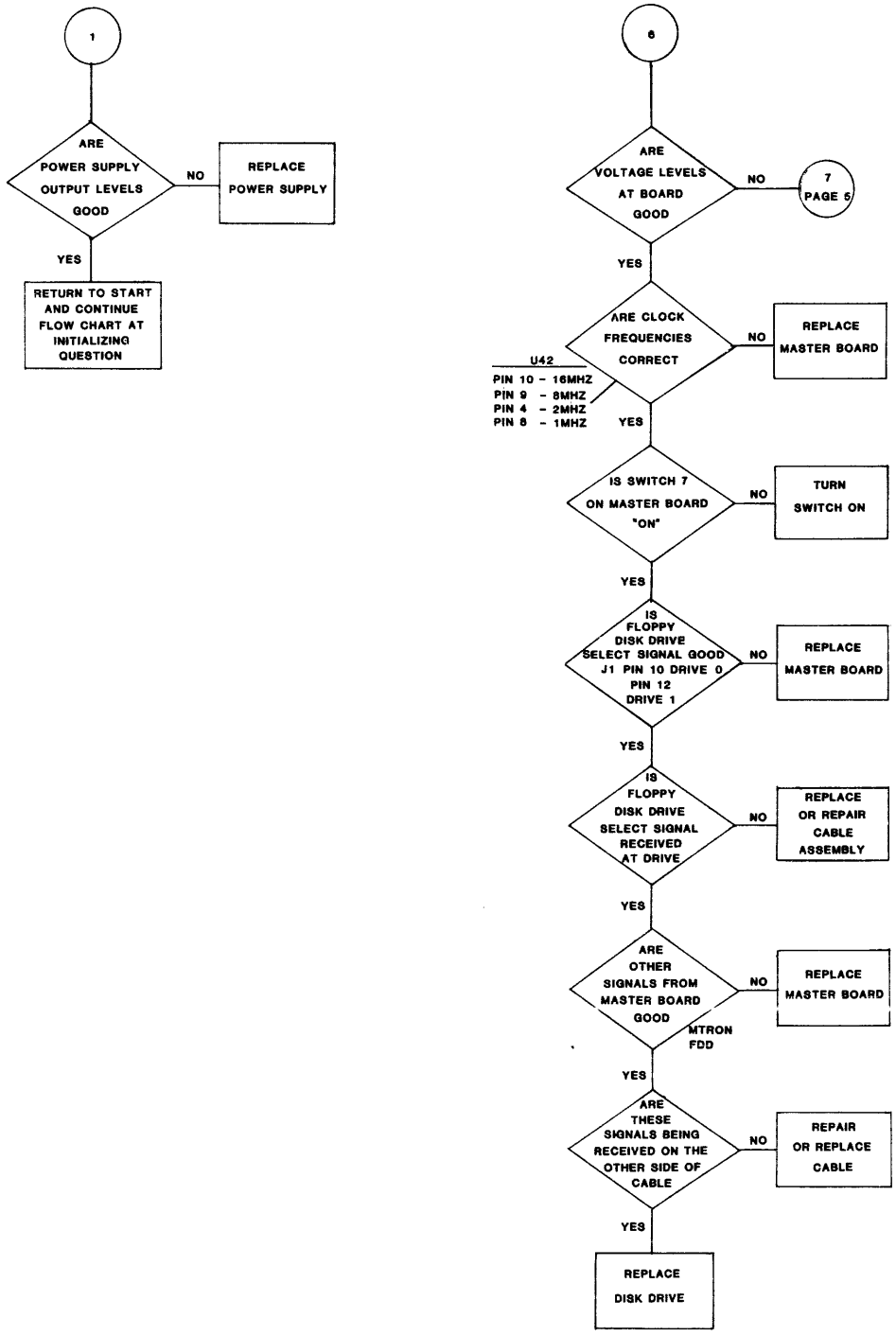


Figure 2-11. Problem Isolation Flowchart (Part 4 of 5)

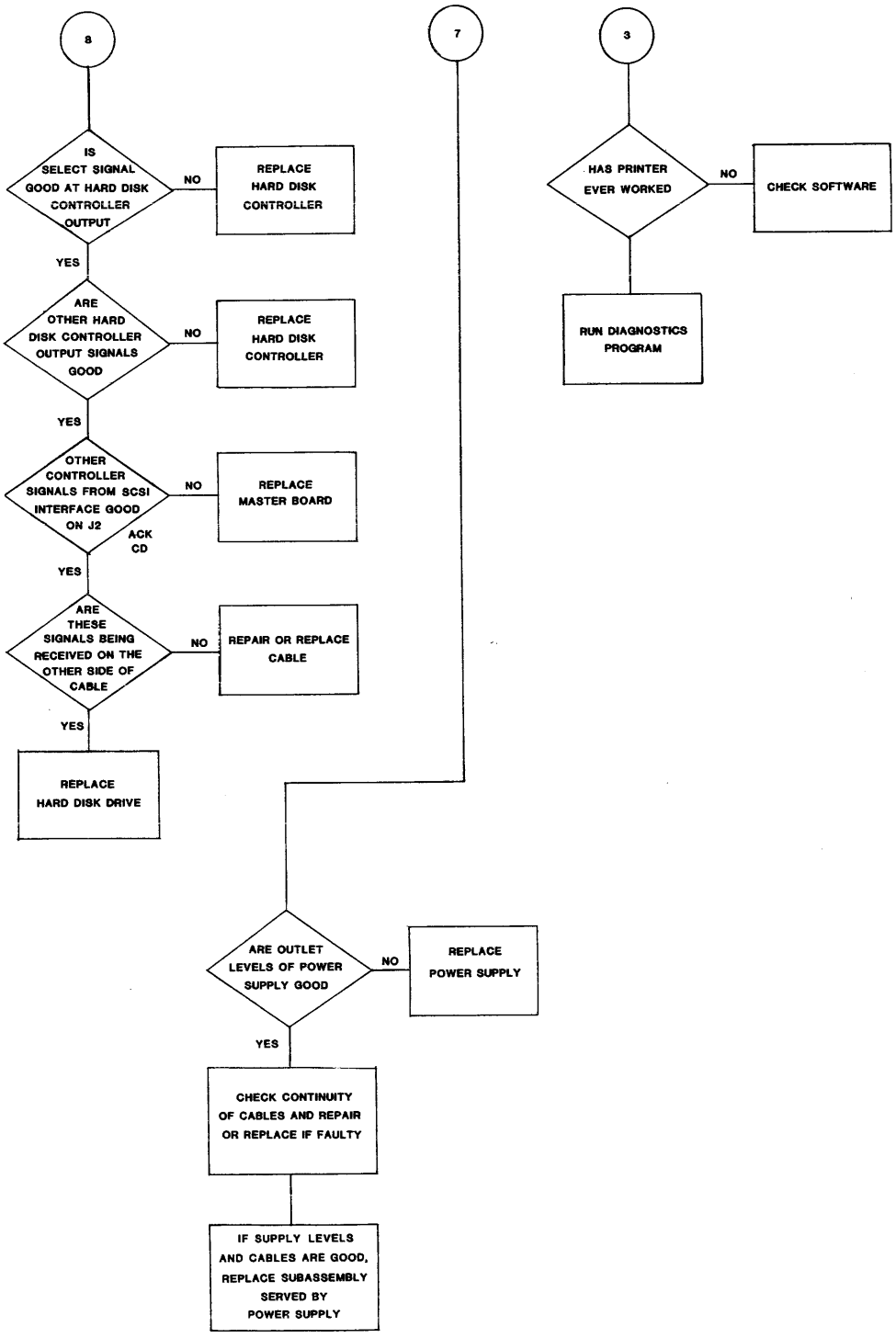


Figure 2-11. Problem Isolation Flowchart (Part 5 of 5)

If several terminals are being used with the system, but only one is malfunctioning, swap a known good terminal to see whether the terminal or the port is faulty. If only one terminal is used with the system, try it in another port, again to see whether the port or the terminal is faulty. To maintain and repair the terminal, refer to the appropriate manual.

If the problem has still not been detected, the next step is to check signal levels, using Appendix A and Figure 2-11, the Problem Isolation Flowchart.

A variety of software can be used in the DBS 16 System, requiring many different peripheral device configurations, which can complicate troubleshooting. When problems occur with the peripherals, use the DBS 16 Diagnostics Program diskette, available from your dealer.

2.4 DISASSEMBLY

This paragraph explains how to disassemble the DBS 16 for repair. An isometric drawing in Section 4 shows the interrelationship of the subassemblies.

When removing any subassembly from the Desktop Unit, label the cable connections and note the cable routing to aid in reinstallation.

Viewing the DBS 16 Desktop Unit from the rear, you will see that the top panel and two side panels are each secured by two 1/4-turn Phillips-head screws. The method of removal is the same for all three panels. Use a screwdriver to loosen the two 1/4-turn screws by turning them counterclockwise, then pull each panel toward the rear and lift it away.

The Master Board is located under the left panel (viewed from the front), the Hard Disk Controller (if present) is under the top panel, and access to the Power Supply is behind the right panel.

The Master Board solder side is on the outside. To expose the component side, remove the four slotted screws securing the board to the wire frame, and gently fold the Master Board down without loosening the cables.

NOTE

You cannot fold down the Master Board with the Desktop Unit plugged into the Expansion Box, because the bottom edge connector of the Master Board is plugged into the bottom box and this connection is not flexible.

The optional Expansion RAM Board (if present) is mounted on the Master Board with 7/16" plastic standoffs.

The other optional board, the Hard Disk Controller (if present), can be accessed (after the top panel is removed) by loosening the 1/4-turn Phillips-head screw toward the front of the mounting plate. Once loosened, the Hard Disk Controller Board can be folded back to expose the component side of the board.

After removing the covers, remove the Power Supply by loosening the two 1/4-turn screws on the solid metal plate on the lower left side and pulling out the tray. Cable ties may be securing the wiring harnesses to the frame. These have to be cut off before the Power Supply will slide out.

The disk drives are secured through the drive mounting spacer at the top of the fixed drive box of the wire frame, and at the bottom of the wire frame assembly. The Hard Disk Controller mounting plate must be folded back to gain access to the two screws holding each drive to the drive mounting spacer. Remove the Power Supply to access the two screws securing the bottom of the drives (a stubby screwdriver is needed for this action). Then slide the drives out the front of the unit.

To remove the front panel, unscrew the two screws securing it to the top of the wire frame assembly and the two screws on the bottom of the wire frame. To remove the drive mounting spacer from the disk drives, remove the two screws securing it to each disk drive. The power switch and LED are accessed by removing the Power Supply.

The line voltage selector switch, ventilation fan, and ac interface are located on the backpanel. The fan is accessible by removing the screws from the backpanel of the Desktop Unit and lifting off the left side panel. The Voltage Selector switch, fuse holder, ac line filter, and power cord interface are accessed by removing the Power Supply. Four screws secure the backpanel to the wire frame assembly.

2.5 INSTALLING EXPANSION RAM BOARD ON MASTER BOARD

1. Turn off the system and unplug it from power source.

2. Remove Master Board and lay it on a clean, flat, padded, static-free surface. Position it with chips facing up, and terminal connectors on the left side.

3. Locate the 3 holes on the right-half of the Master Board closest to locations R71, R93, and U76. Insert the 3 small stand-off clips into these holes from the bottom (solder side) of the Master Board.

4. Mount the 3 stand-offs on top of the stand-off clip. Apply pressure to both stand-off and clip until the clip ears protrude through the hole, locking the stand-off in place.

5. Hold the Expansion RAM Board with the 52-pin connector on the bottom side, left front position.

6. Mount the RAM Board on the Master Board.

> **CAUTION**
>
> DO NOT FORCE THE CONNECTORS TOGETHER. IF THE CONNECTORS DO NOT SLIDE EASILY TOGETHER, YOU HAVE NOT POSITIONED THEM CORRECTLY. BE SURE YOU HAVE READ STEPS 5 AND 6 CORRECTLY. FORCING A CONNECTOR PIN THROUGH THE PLASTIC PLUG IN THE RAM BOARD CONNECTOR WILL PUT 5 VOLTS ON THE GROUND PINS AND DAMAGE SYSTEM COMPONENTS.

   a. Position the connector of the RAM Board so that it is snug against the front edge of the 50-pin connector (location J6) on the Master Board.

   b. If you do this correctly, the connector pins will slide easily into place, and the top clip of the stand-offs will protrude through the holes in the RAM Board.

7. Squeeze the RAM and Master boards together at each stand-off to latch the boards securely in place. Gently press the connectors to ensure the pins are firmly seated.

8. Reassemble the system, taking care to insert cables in original positions. (Ribbon cable identifies pin 1 with a stripe along the cable edge; connectors identify pin 1 with an arrow, and "1" is printed on the board next to the connector.)

SECTION 3
DBS 16 EXPANSION BOX

3.1 GENERAL

This section looks at the DBS 16 System Expansion Box. Each paragraph is keyed to a sheet of the schematics in Section 4. For example, paragraph 3.1.2, Mother Board Circuit Functions, is keyed to Sheets 2 and 3 of the Mother Board schematics.

The major subassemblies of the Expansion Box are shown in Figure 3-1. These subassemblies are:

- Power Supply
- Mother Board
- Optional Slave Card

These three DBSI-produced subassemblies are the only ones covered in this manual, because of the variety of MULTIBUS-compatible boards that could be used in this unit. Following the subassembly descriptions are paragraphs on adjustments, routine maintenance, troubleshooting, and disassembly.

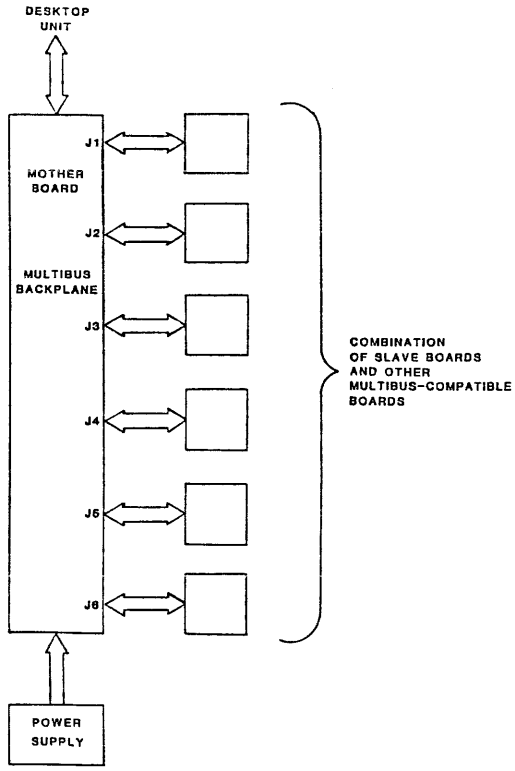


Figure 3-1. Expansion Box: Major Subassemblies

3.1.1 Power Supply Circuit Functions

The Expansion Box Power Supply is identical to the Power Supply used in the DBS 16 Desktop Unit, except for the addition of a large heat sink which increases the supply rating to 130 W. This supply delivers +5 V, +12 V, -12 V, and ground to the electronic circuitry in the Expansion Box.

> **NOTE**
>
> Although voltage settings on the DBS 16 are labeled 115V and 220V, the unit is also compatible with, and operable at, 110 Vac and 230 Vac.
>
> When the Voltage Selector switch is set to 115V, the unit can operate in the range from 90 Vac to 132 Vac. When the Voltage Selector switch is set to 220V, the unit can operate in the range from 180 Vac to 264 Vac.

Features of this power supply include:

- Choice of 115 Vac or 220 Vac input
- Short circuit protection
- Overvoltage protection on the +5 V output
- Input surge current protection
- 20 KHz minimum switching frequency

The maximum allowable ripple on any output is 50 mV. The nominal voltage and maximum output current of the Power Supply are as follows:

Output 1: +5 V, 15 A
Output 2: +12 V, 4 A
Output 3: +12 V, 1.5 A
Output 4: -12 V, 0.7 A.

The Expansion Box Power Supply receives ac input from the Desktop Unit Power Supply through a connection at the top of the Expansion Box.

3.1.2 Mother Board Circuit Functions

The Mother Board serves as the backplane in the Expansion Box. It contains the six-slot MULTIBUS and the "Mailbox" RAM. This paragraph is keyed to Sheets 2 and 3 of the Mother Board schematics, and is illustrated by Figure 3-2.

This board has six 86-pin slots that are used for MULTIBUS boards such as the Slave Cards. MULTIBUS (IEEE 796 standard) boards are produced by several manufacturers, and function, for example, as mass storage controllers, memories, I/O controllers, graphics, and other software.

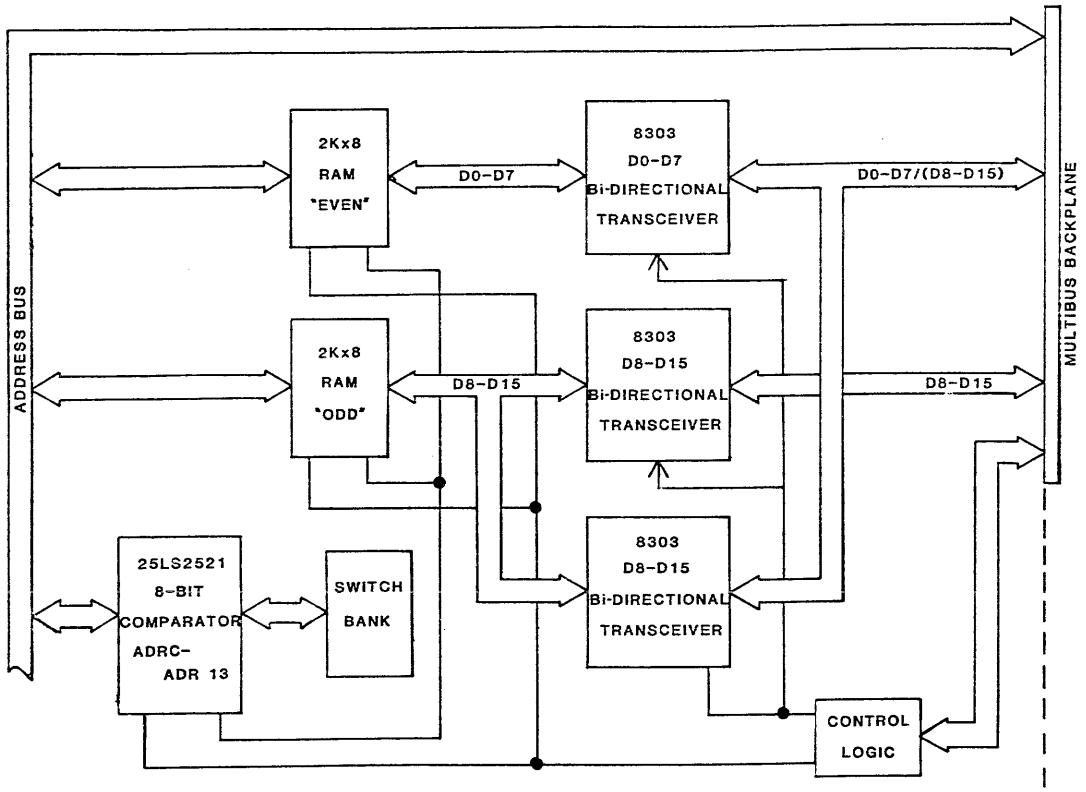


Figure 3-2. Mother Board Functional Block Diagram

Priority for attention among these boards is determined by parallel priority resolution through circuitry in the Expansion Box. A 74LS148 Priority Encoder receives bus access requests from the six slots and the Master Board circuitry (P1). P1 (Mother Board) has the highest priority, followed by J1 in the top slot of the card cage, then J2, J3, and so on. J6 in the bottom slot has the lowest priority. Decoding the output of the 74LS148, a 74LS138 Decoder/Demultiplexer returns an acknowledgement to one of the slots, giving it use of the MULTIBUS.

The other circuitry on the Mother Board is the Mailbox RAM. A 4K byte memory has two 2K by 8-bit static RAMs. The "even" RAM holds D0-D7 and the "odd" RAM holds D8-D15. This memory acts as go-between for the MULTIBUS-compatible boards and the Master Board processor and disk drives. The address of this memory is set by switches on the Mother Board (refer to paragraph 3.2.1). This RAM normally resides at address BF000 through BFFFF (hex), in systems running DBS 16 MP/M-86.

Two methods of inputting and outputting data are possible through the use of three 8303 bi-directional transceivers.

A 16-bit word is sent in parallel (first method) when one 8303 passes data bits D0-D7 onto the D0-D7 data bus, and another passes data bits D8-D15 to the D8-D15 data bus.

The third 8303, however, can pass data bits D8-D15 onto the D0-D7 data bus. Of course, data bits D0-D7 and D8-D15 are gated onto the D0-D7 data bus at different times. Through a second method, known as "byte swapping," the low order byte is sent over D0-D7, then the high order byte is sent over the same bus. This method allows the DBS 16 to be connected to other systems using 8-bit microprocessors, or 16-bit microprocessors using 8-bit data busses.

3.1.3 Slave Card Circuit Functions

The DBSI Slave Card allows expansion of the DBS 16 System from four to a maximum of 28 users. Any terminal(s) requiring more memory than others can be put on a Slave Card alone, or with one or two other terminals. Then, by changing the operating system software, more memory can be allocated to one terminal and less to the others.

The Slave Card is a MULTIBUS-compatible board containing the circuitry necessary to provide the following basic functions:

- Central Processing Unit (CPU)
- RAM Memory
- Input/Output
- MULTIBUS Interface

3.1.3.1 Slave Card CPU

This paragraph is keyed to Sheet 2 of the Slave Card schematics in Section 4. The principal integrated circuits of this part of the logic are: one 80186 microprocessor and two 2732 PROMs. Figure 3-3 is a functional block diagram illustrating the Slave Card CPU and RAM.

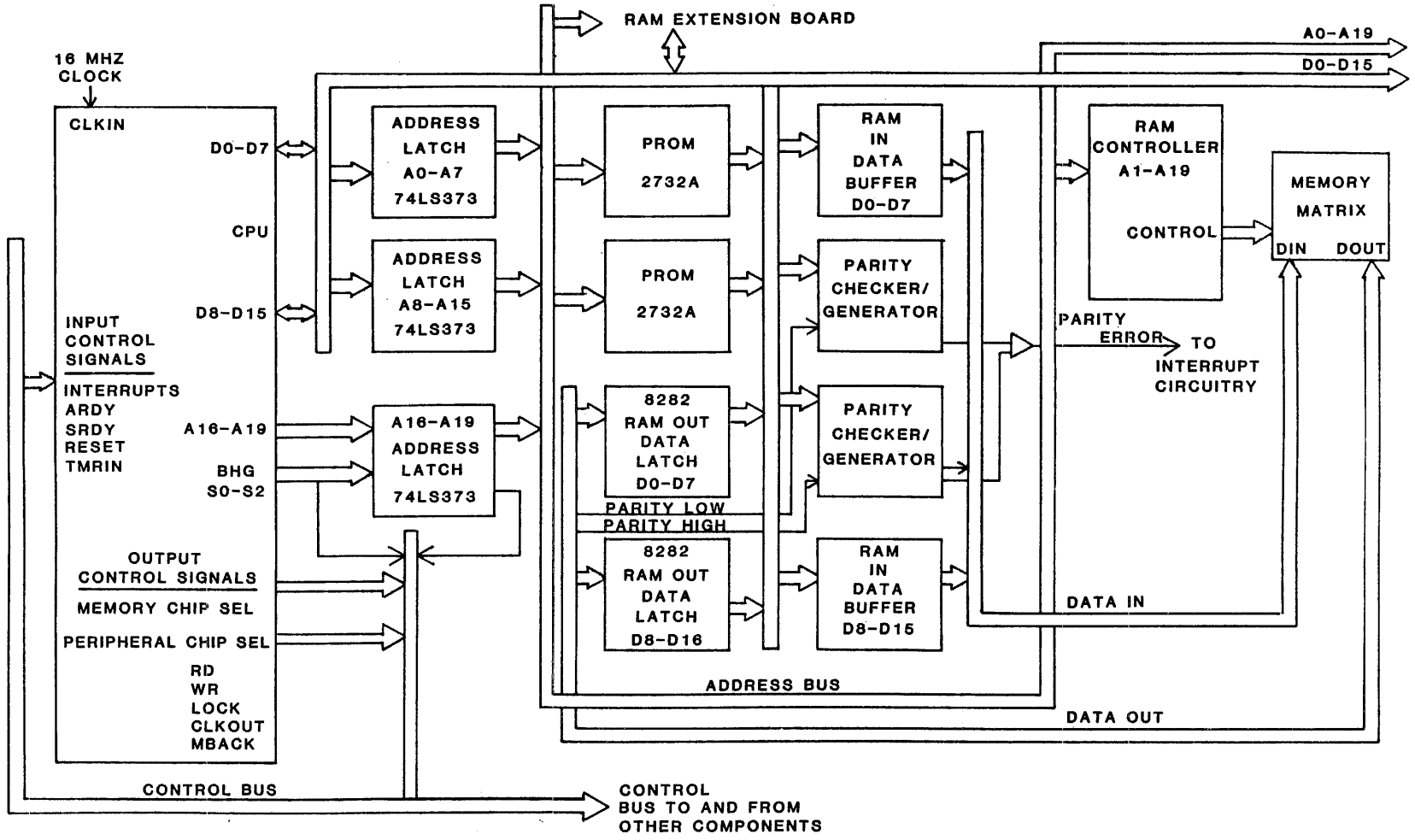


Figure 3-3. Slave Card CPU and RAM Functional Block Diagram

The 80186 is a 68-pin microprocessor that uses a 16-bit time-multiplexed data/address bus. An additional four address lines are used, for a total of 20, addressing on one million locations. During the first pulse of the clock, T1, information on the bus is treated as an address and is latched into the address latches. For the next three clock pulses (T2,T3,T4), the information on the bus is treated as data. The microprocessor has a crystal input of 16 MHz, which is internally reduced to a clock pulse of 8 MHz for operations.

Control signals generated by the 80186 are: S0-S2, bus cycle status lines to bus arbiter; CSEXP, chip select expansion RAM; CSRAM, chip select RAM; CSROM, chip select ROM; CALE, address latch enable; PCS0 and PCS1, peripheral chip select for the 2681-24s interfacing the terminals; RD, read command; WR, write command; LOCK, lock out other bus masters; M/IO, Memory or I/O; CLKOUT, an 8 MHz clock; and BHE, bus high enable.

Input signals to the 80186 are: INT0, parity error interrupt; INT1 and INT2, from terminals; INT3, from the MULTIBUS; SRDY, synchronous ready signals ROM read will take place; ARDY, asynchronous ready signals that a data transfer will take place from either RAM, Expansion RAM, or MULTIBUS; CLKIN, a 16 MHz clock; and RESIN, reset in.

Interrupts from the MULTIBUS and the terminals go directly to the CPU. These interrupts are:

- INT0 from Parity Error
- INT1 from a 2681-24 DUART controlling two terminals
- INT2 from a 2681-24 DUART controlling two terminals
- BUS INT from the MULTIBUS

In the case of the 2681-24s, the CPU requests a status word to determine which of the two channels contained in each 2681-24 is requesting service, and communication is established. An interrupt request from the MULTIBUS receives an MBACK (MULTIBUS Acknowledge) signal.

The software determines whether these interrupts or polling will be used to determine when service is required.

Two 2732A PROMs provide 8K bytes of booting instructions. At power-up, these PROMs are accessed and information is provided to program the 2681-24s.

3.1.3.2 Slave Card RAM Control and RAM

The memory on the Slave Card is the standard 256K bytes of dynamic RAM, complete with RAM controller circuitry. This paragraph is keyed to Sheets 2 and 4 of the Slave Card schematics. (Also see Figure 3-3.)

The Slave Card uses an 8203 RAM Controller to interface with its array of thirty-six 64K RAMs. The 8203 receives address lines A0-A17, plus read, write, and chip select. It also receives a 25 MHz clock. It outputs row address lines, column address strobe lines, row address strobe lines, and write enable.

The RAM chips are arranged in four rows of nine 64K bit chips. This arrangement yields two complete sets of words, a high and a low set. Each word consists of two 8-bit bytes plus a parity bit for each byte. This yields a 256K byte dynamic RAM memory onboard the Master Board. An optional board can add another 256K bytes. That board is identical to the Expansion Board used in the Desktop Unit and is covered in paragraph 2.1.3.

The output of the RAMs is latched into two 8282 tri-state octal latches, and the parity bits are latched into a 74LS75 quad latch. Data to be written into the RAMs passes through two 74LS244 octal buffers.

Whenever data is read by the CPU, it is checked for parity. The 16 bits of data plus the two parity bits are fed into two 74LS280 odd/even parity checkers/generators. At this point, a parity error signal is generated, unless the parity of both words is EVEN. Parity is generated whenever data is written into RAM.

3.1.3.3 Slave Card Input/Output (I/O)

This paragraph explains the means of communication used by the terminals and the CPU. It is keyed to Sheet 3 of the Slave Card schematics and is illustrated by Figure 3-4.

Communication with the four terminal ports is handled through two 2681-24 Dual Asynchronous Receiver/Transmitters (DUART). Each DUART controls two terminal ports. These two-channel devices are programmed by the onboard PROMs at power-up, and by the operating system. Along with an 8-bit data bus, each DUART has four address lines (A1-A4), which are used to select a particular channel and register.

A chip select line is used to enable the DUART. Each chip has an interrupt output to request that communications be opened between the CPU and a terminal. Other inputs include the read, write, and reset commands and a 3.6864 MHz clock.

Each of the two channels has a receiver input and transmitter output. The four-pin connections with the terminal are via Shielded Data Link (SDL) connectors on a four-wire cable.

Data is received by the DUART on the CPU side in parallel and converted to serial form for transmission to the terminal. The terminal serial stream is received by the DUART and converted to parallel form.

In addition to the data transmit and data receive lines, the line driver supporting the terminals is supplied with a +12 V, -12 V, and ground source.

3.1.3.4 Slave Card MULTIBUS Interface

The MULTIBUS interface circuitry allows communication with the Mother Board, and through that, other boards in the Expansion Box and the Master Board in the Desktop Unit. This paragraph is keyed to Sheet 3 of the Slave Card schematics and is illustrated by Figure 3-4.

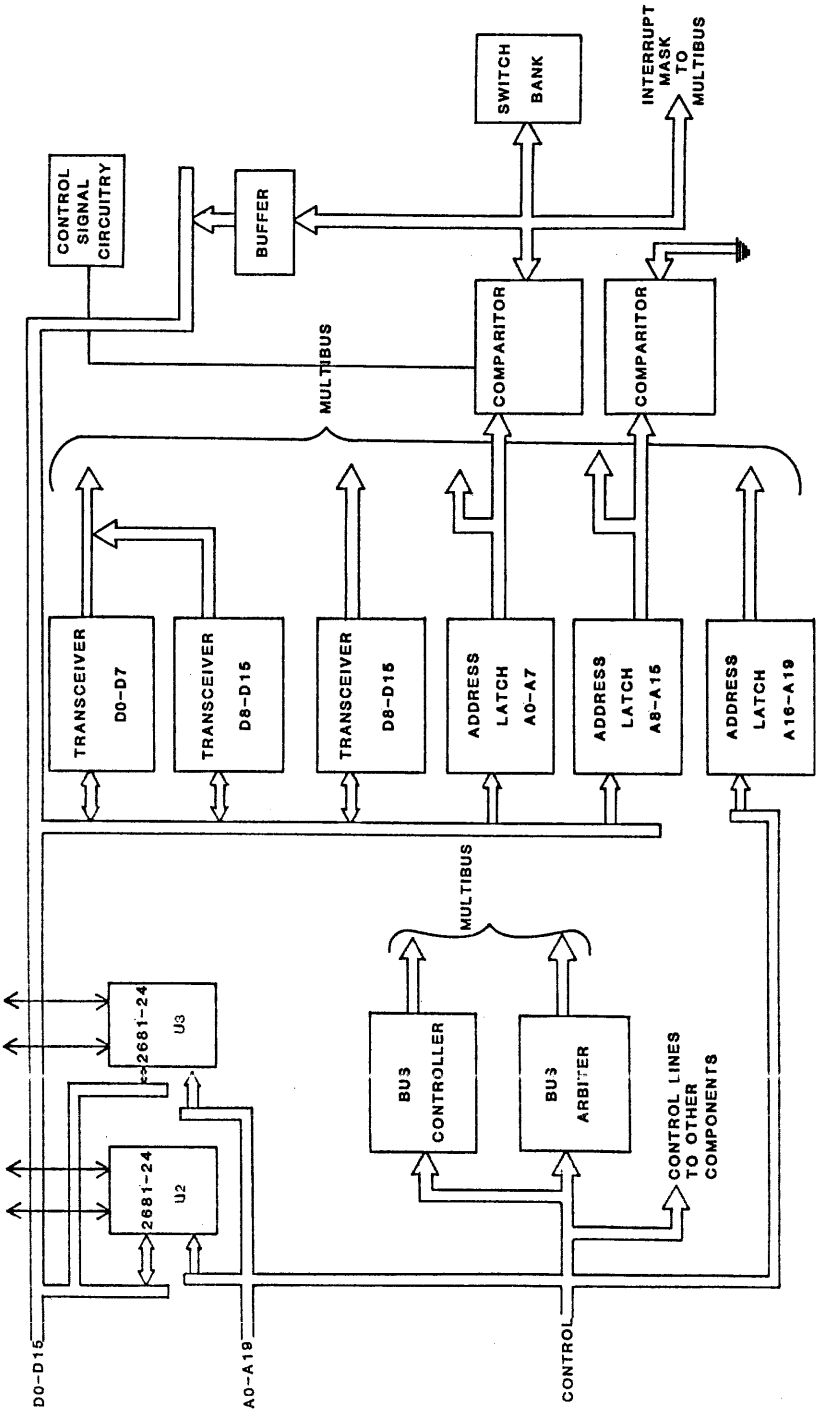


Figure 3-4. Slave Card I/O and MULTIBUS Interface Functional Block Diagram

Two methods for data input and output between the Slave Card and the MULTIBUS in the Expansion Box are possible through the use of three 8303 bi-directional transceivers.

A 16-bit word is sent in parallel (first method) when one 8303 passes data bits D0-D7 onto the D0-D7 data bus, and another 8303 passes data bits D8-D15 to the D8-D15 data bus.

The third 8303, however, can pass data bits D8-D15 onto the D0-D7 data bus. Of course, data bits D0-D7 and D8-D15 are gated onto the D0-D7 data bus at different times. Through a second method, known as "swapping bytes," D0-D7 are multiplexed so the low order byte, followed by the high order byte, can be sent over the same portion of the bus. The method used is determined by software.

Addresses derived from the data bus during T1 clock pulse are latched into two 8283 inverting octal latches, while a third 8283 latches address lines A16-A19.

The MULTIBUS interface is controlled by an 8288 Bus Controller and an 8289 Bus Arbiter. The MULTIBUS command signals provided by the 8288 Bus Controller are based on what the Controller receives from the CPU status lines and its control input lines. Output of the chip also includes address latches, data transceivers, and interrupt control signals.

The 8289 Bus Arbiter, which is transparent to the CPU, intercepts CPU status lines and returns a "not ready" status to the CPU until the Bus Arbiter acquires the use of the multi-master system bus. Once use is acquired, the 8289 allows the Bus Controller, data transceivers, and the address latches to access the system. The Bus Arbiter, controlled by the CPU status lines, functions as a multiplexer between bus masters.

To send a BUSINTSLV (Bus Interrupt Slave Card) signal to the onboard CPU, 25LS2521 Comparitor compares the interrupt mask set by a switch bank on the board with an address on the address bus. If the mask and address are the same and an IOWC (I/O Write Command) has been sent by the Bus Controller, together they clock through DAT0 as the interrupt signal to the onboard CPU and a TXACK (Transmit Acknowledge) to the MULTIBUS.

To send an interrupt to the MULTIBUS, a write command and a PCS4 command are OR-ed together to clock through D0, which is used to enable NAND gates onto the MULTIBUS. The mask they show is the Slave Card ID set by six switches on the Slave Card. For these switch settings, refer to paragraph 3.2.1.

3.1.4 Optional Expansion RAM Board

The optional Expansion RAM Board circuitry is identical to the optional board used in the Desktop Unit and to the RAM circuitry on the Slave Card except, in the latter case, CSEXP (Chip Select Expansion) is used instead of CSRAM to enable the controller on the Expansion RAM Board. This paragraph is keyed to Sheets 2 and 3 of the Expansion RAM Board schematics.

The Expansion RAM Board also contains 256K bytes of dynamic RAM controlled by an 8203 RAM Controller. Arrayed in four rows of nine 64K bit chips, the board outputs and inputs two 8-bit bytes per word, plus a parity bit for each byte. Output of the RAMs is latched into a 74LS75 quad latch, and data to be written in is passed through 74LS244 octal buffers. Parity is generated when data is written, and checked when it is read.

3.2 ADJUSTMENTS AND ROUTINE MAINTENANCE

3.2.1 Switch Settings

There are several locations in the Expansion Box where switches must be properly configured to insure proper operation. These are illustrated by Figures 3-5 and 3-6.

Externally, on the backpanel of the Expansion Box is a switch to set the unit Power Supply for either 95-135V (up position) or 198-250V (down position).

A nine-position switch on the Mother Board allows enabling and address selection of the shared RAM. See Figure 3-5. This RAM occupies 4K byte locations in the MULTIBUS address space, somewhere in the range of 80000 to BFFFF (Hex). The specific address location is determined by the switches. Normally, this RAM resides at addresses BF000 through BFFFF (hex), in systems running MP/M-86.

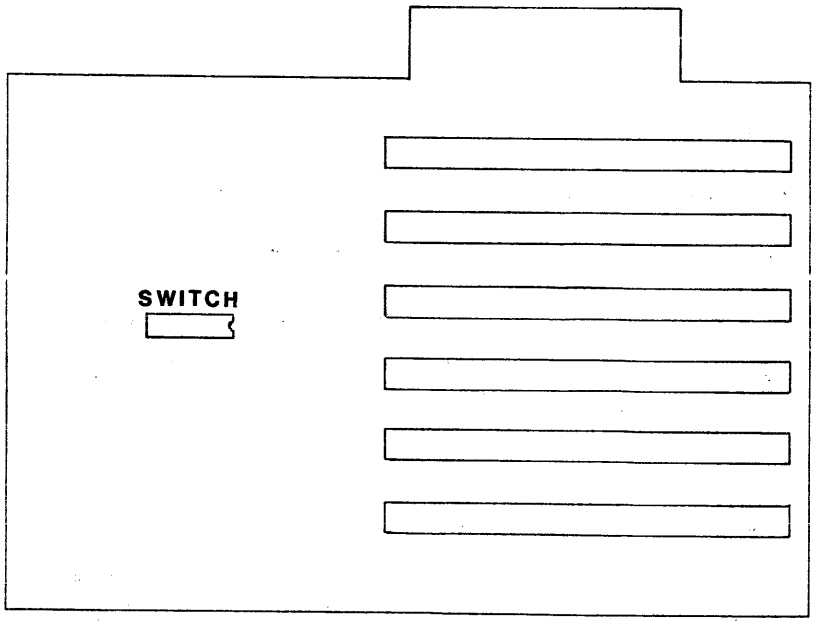


Figure 3-5. Mother Board RAM Address Switch

Switch 1 either disables or enables the shared RAM. ON enables, OFF disables. Switches 2 through 9 are used to determine the most significant bits of the address range. Switch 9 represents the most significant bit of the address range.

For example, to set the normal high order address, the switches would be set as follows:

S9	S8	S7	S6	S5	S4	S3	S2	S1	S1 is ON to enable memory
On	Off	On	On	On	On	On	On	On	

This would yield an address of 1011 1111 XXXX XXXX XXXX or BFXXX (hex), with the X's representing the lower order address within the shared RAM.

Each DBSI Slave Card contains circuitry to generate interrupts to the Master Board and to receive interrupts from any device on the MULTIBUS. This circuitry also enables each Slave Card to determine its own identity so that there is proper communication between the Master and each one of up to six Slave Cards. See Figure 3-6.

Each Slave Card contains several switches which are used to set the identity (ID) of that card. Six of the switches on the Slave Card are used for this purpose. The following listing gives the possible settings of these switches, the resulting addresses to be used by the Master to generate interrupts to that Slave, and the corresponding interrupts to the Master generated by that card.

In Table 3-1, BUS INT is the MULTIBUS interrupt generated by the Slave Card, READ ID is the value that a given Slave Card will read from its ID port, and INT ADDR is the MULTIBUS I/O address used by the Master to generate an interrupt to the Slave Card.

Table 3-1. Slave Card ID Switch Locations

S1	S2	S3	S4	S5	S6	BUS INT	READ ID	INT ADDR
Off	On	On	On	On	On	0	41	BFFC
On	Off	On	On	On	On	1	21	BFFA
On	On	Off	On	On	On	2	11	BFF6
On	On	On	Off	On	On	3	09	BFEE
On	On	On	On	Off	On	4	05	BFDE
On	On	On	On	On	Off	5	03	BFBE

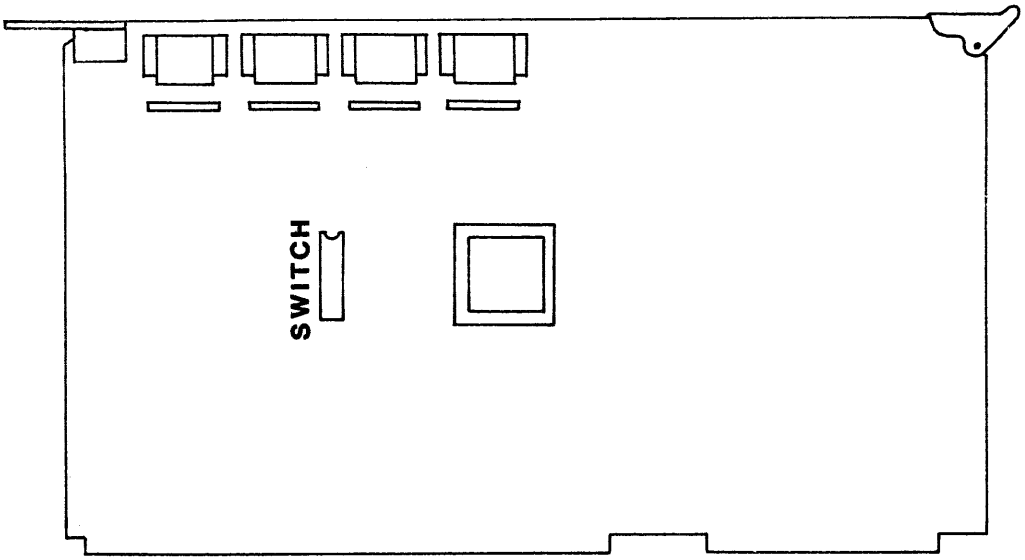


Figure 3-6. Slave Card ID Switch Location

3.2.2 Routine Maintenance

Because there are no moving parts in the Expansion Box, routine maintenance merely involves keeping the environment and the unit as clean as possible, and protecting the unit from impact. To keep the system trouble-free, be sure there is sufficient space around the Expansion Box to allow proper ventilation.

3.3 TROUBLESHOOTING

3.3.1 Environmental Problems

Although the Expansion Box, along with the entire DBS 16 System, is rugged and reliable, certain environmental conditions must be met for trouble-free operation. Refer to Sections 2 and 3 of the DBS 16 User's Manual for detailed installation and power-up procedures.

The same conditions that were detailed in paragraph 2.3.1 for the Desktop Unit, are required for the Expansion Box. If you have not read that paragraph, please do so now. Pay particular attention to the WARNING noted there in accordance with FCC Rules regarding radio frequency energy.

3.3.2 Problem Isolation

When the unit is malfunctioning, check first that the operating system has not been corrupted. Do this by using a backup copy of the operating system.

The purpose of this manual is to isolate problems to the subassembly, not the individual chip on a board. Therefore, effort should be concentrated on tracing signals from one board to another, rather than individual chips. When a subassembly is suspected of being faulty, it should be removed and replaced with a known good assembly. A multimeter and an oscilloscope are required to trace these signals and check the power supply levels.

Good troubleshooting techniques apply here as with any system. Check the obvious (but often overlooked) first. Make sure the Expansion Box is plugged into the Desktop Unit properly and check the fuse. Make sure the circuit serving the DBS 16 System is not overloaded. Ask the operator for a demonstration of technique, to show the problems encountered. The problem could be operator error.

If the problem cannot be detected externally, then open up the unit to look at the internals. Remember good safety procedures. Be sure the power is off before removing any subassembly, and never try to operate the system with any part disconnected. This could reduce the total resistance in the circuit and cause unacceptably high currents in other parts of the system.

The cable assemblies are often overlooked as a problem source. Check both ends of a cable to see if the signals are consistent from origin to destination. Also, make sure the cable connections and the edge connectors are good. The edge connectors can become oxidized, and a simple cleaning often solves the problem.

Check the output levels of the Power Supply. If they are found to be faulty, check to see if the ac input from the Desktop Unit is good. If the ac input is good, but the dc outputs are bad, replace the Power Supply. If the ac input from the Desktop Unit is bad, check the ac input to the Desktop Unit. If this ac input from the wall outlet is good, replace the Desktop Unit Power Supply. If the ac wall outlet levels are bad, call an electrician to check out the circuitry.

If more than one MULTIBUS board is malfunctioning, it is likely that the problems are not in the MULTIBUS board, but rather in the Mother Board or Desktop Unit. If only one board is malfunctioning, put it in another slot after resetting the Slave Board ID switches to conform to that location. If the board works in the new slot, then the problem is probably in the circuitry of the Mother Board or the Desktop Unit.

To check out the Desktop Unit, disconnect the Expansion Box and plug one of your terminals into port 1 of the Desktop Unit. Insert the CP/M-86 or MP/M-86 operating system diskette into the Desktop Unit to operate it as a single-user, single-processor computer. If it works properly, then the Desktop Unit circuitry is working. This leaves the possibility of a malfunction in the Mother Board circuitry, or a problem with the operating system.

To gain access to the boards in the Expansion Box to check signal levels, you will need a MULTIBUS extender board, available from your computer dealer. Refer to Appendix A for a listing of the signals on the various subassemblies.

3.4 DISASSEMBLY

The Expansion Box is connected to the Desktop Unit by an edge connector from the top of the Expansion Box to the bottom of the Desktop Unit, and by four screws from the top of the Expansion Box into the bottom of the Desktop Unit. To access the screws, remove the right side panel of the Expansion Box (viewed from the front of the unit). Another connection is the ac power connection.

An isometric drawing in Section 4 illustrates the assembly of the Expansion Box. The side panels are each secured by two 1/4-turn screws. After loosening them, you can remove the panels. Remove the right side panel to access the terminal connector side of the Slave Cards and the Power Supply. To remove the Power Supply, remove the two screws securing the tray to the wire frame, then slide out the tray. Be careful not to pull the cable connections out of the Power Supply without labeling the connections and noting the routing.

The four-wire flat cables that connect the terminals to the Slave Cards in the Expansion Box dress out from their SDL connections at the Slave Cards and through the slot between the left and back panels.

To remove the MULTIBUS boards, simply slide them along the plastic guide tracks, away from the edge connectors.

3.5 CONNECTING THE EXPANSION BOX TO THE DESKTOP UNIT

*** WARNING ***

ONLY AUTHORIZED SERVICE PERSONNEL SHOULD INSTALL THE DBS 16.

TURN OFF POWER TO ALL COMPONENTS BEFORE ATTEMPTING TO CONNECT CABLES. OTHERWISE, ELECTRICAL SHOCK CAN RESULT.

Follow this procedure to connect the Expansion Box and Desktop Unit:

1. Make sure power is turned off on all components before installing the DBS 16.

2. Set up the display terminal according to the instructions in the terminal user's manual.

3. Plug the 25-pin connector end of the terminal cable into the appropriate serial port at the rear of the display terminal.

4. On a clean, flat surface, place the Desktop Unit on its right side. DO NOT remove any side panels.

5. Remove the two adhesive-backed covers on the bottom of the Desktop Unit to expose the two connectors.

6. Glued to the bottom of the Desktop Unit are four rubber feet. Remove them with pliers.

CAUTION

THE EXPANSION BOX IS DESIGNED SOLELY FOR USE WITH THE DBS 16 DESKTOP UNIT. ANY OTHER USAGE MAY DAMAGE THE UNIT AND OTHER EQUIPMENT.

7. Remove the left panel of the Expansion Box (the side opposite the PC board connector), using a screwdriver to loosen the 1/4-turn fasteners. Carefully slide the panel toward the rear and lift it away from the box.

8. Place the Expansion Box on its side so that the open side is facing up.

9. Align the bottom of the Desktop Unit (still on its side) with the top of the Expansion Box (also on its side). Make sure the front of each unit is facing you.

10. Gently push the two units together until the exposed connector on the PC board in the Expansion Box mates with the connector in the bottom of the Desktop Unit.

11. Carefully, but firmly, fasten the Desktop Unit to the Expansion Box using the four supplied screws.

12. Take the 3-pin connector end of the attached power cable up through the top of the Expansion Box and connect it to the 3-pin connector in the bottom of the Desktop Unit. Note the connector pin arrangement to properly connect it.

13. Carefully stand both units up so that the Desktop Unit is on top of the Expansion Box. The Expansion Box has six card slots for plugging in DBSI Slave boards, and/or any other type of MULTIBUS board (i.e., a special printer or disk controller, Ethernet, or X.25).

*** WARNING ***

TURN OFF POWER BEFORE INSERTING OR REMOVING MULTIBUS CARDS. OTHERWISE, ELECTRICAL SHOCK CAN RESULT. DAMAGE TO CARDS AND/OR THE DBS 16 CAN ALSO RESULT.

14. Slide any MULTIBUS card into one of the slots in the Expansion Box. Make sure the card is firmly seated.

15. Plug the SDL 4-pin connector end of the terminal cable (the one referred to in step 3) into the first terminal port (nearest the rear of the box) on any DBSI Slave Board in the Expansion Box.

    Repeat steps 1 through 3, and continue at step 13 for each display terminal that you install.

16. Replace the right panel on the Expansion Box by simultaneously pushing and sliding it until it engages the slots at the front, and the 1/4-turn fasteners slip into their holes. Using a screwdriver, push and turn the fasteners to the right until resistance is felt.

17. Plug the female connector end of the Desktop Unit power cord into the power cord receptacle at the rear of the Desktop Unit, and plug the male connector end of the cord into three-prong wall receptacle, or other ac outlet that has been properly grounded. The power cord supplied with the unit is only acceptable for 115 volt operation.

    NOTE: Wall receptacles may be different in countries using 220V. A special power cord with a tandem blade plug is required for 220 volt operation.

3.5.1 Installation of Slave Boards and Other MULTIBUS Boards

1. Turn off the system and unplug it at the power source.

2. Remove the left panel (to your right as you face the unit) of the Expansion Box.

3. Hold board to be installed with chips face up. Align the board with the card guides on the inside front and rear surfaces of the Expansion Box.

4. Gently slide board into the unit, in the card guide tracks. Check alignment of edge connector with the MULTIBUS slot.

5. When edge connector and MULTIBUS slot are correctly aligned, push the board gently but firmly until the edge connector is fully seated.

6. Replace panel and restore power.

3.5.2 Installation of Expansion RAM Board on Slave Board

1. Turn off system and unplug it from power source.

2. Remove Slave Board from unit and lay it on a clean, flat, padded, static-free surface. Position it with the chips facing up, and the terminal connectors on the right side.

3. Locate the 3 holes in the Slave Board closest to locations C36, U5, and R10. Insert the 3 small stand-off clips into these holes from the bottom (solder side) of the Slave Board.

4. Mount the 3 stand-offs on top of the stand-off clip. Apply pressure to both stand-off and clip until the clip ears protrude through the hole, locking the stand-off in place.

5. Hold the Expansion RAM Board with the 52-pin connector on the bottom side, left-front position.

6. Mount the RAM Board on the Slave Board.

> **CAUTION**
>
> DO NOT FORCE THE CONNECTORS TOGETHER. IF THE CONNECTORS DO NOT SLIDE EASILY TOGETHER, YOU HAVE NOT POSITIONED THEM CORRECTLY. REVIEW STEPS 5 AND 6. FORCING A CONNECTOR PIN THROUGH THE PLASTIC PLUG IN THE RAM BOARD CONNECTOR WILL PUT 5 VOLTS ON THE GROUND PINS AND DAMAGE SYSTEM COMPONENTS.

   a. Position the connector of the RAM Board so that it is snug against the front edge of the 50-pin connector (location J5) on the Slave Board.

   b. If you do this properly, the connector pins will slide easily into place and the top clip of the stand-offs will protrude through the holes in the RAM Board.

7. Squeeze the RAM and Slave boards together at each stand-off to latch the boards securely in place. Gently press the connectors to ensure the pins are firmly seated.

8. Reassemble the system, taking care to insert cables in their original positions. (Ribbon cable identifies pin 1 with a stripe along the cable edge; connectors identify pin 1 with an arrow, and "1" is printed on the board next to the connector.

SECTION 4
ELECTRICAL AND MECHANICAL DRAWINGS

4.1 INTRODUCTION

This section contains the mechanical and electrical drawings necessary to support routine maintenance of the DBS 16 System.

The drawings in this section are arranged in a top-down manner. The first figures are line drawings showing the major components. Following the drawings are isometric drawings showing how the various components are physically related. The wiring diagram of the Desktop Unit and the schematics of the major components of the system complete the section. Included with the schematics are summary parts lists.

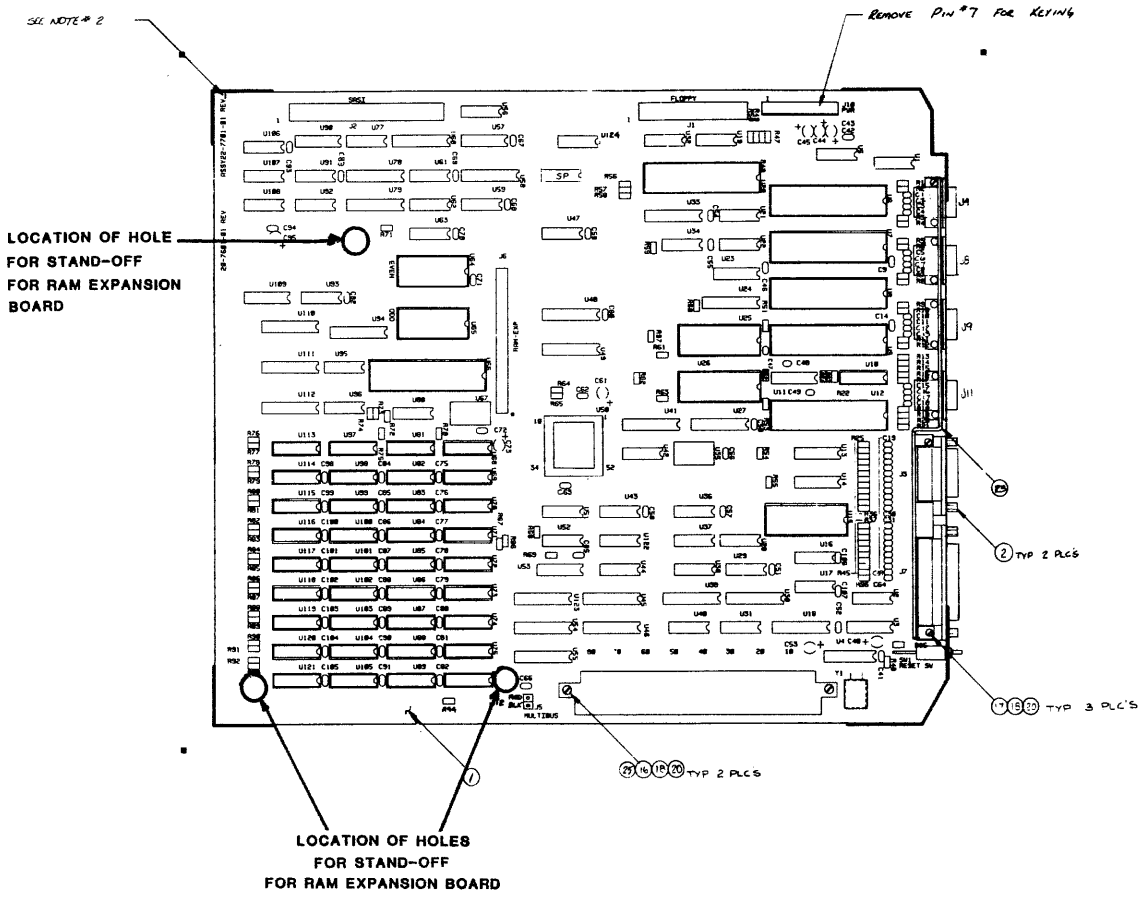


Figure 4-1. Master Board Component Assembly Schematic
(Part 1 of 7)

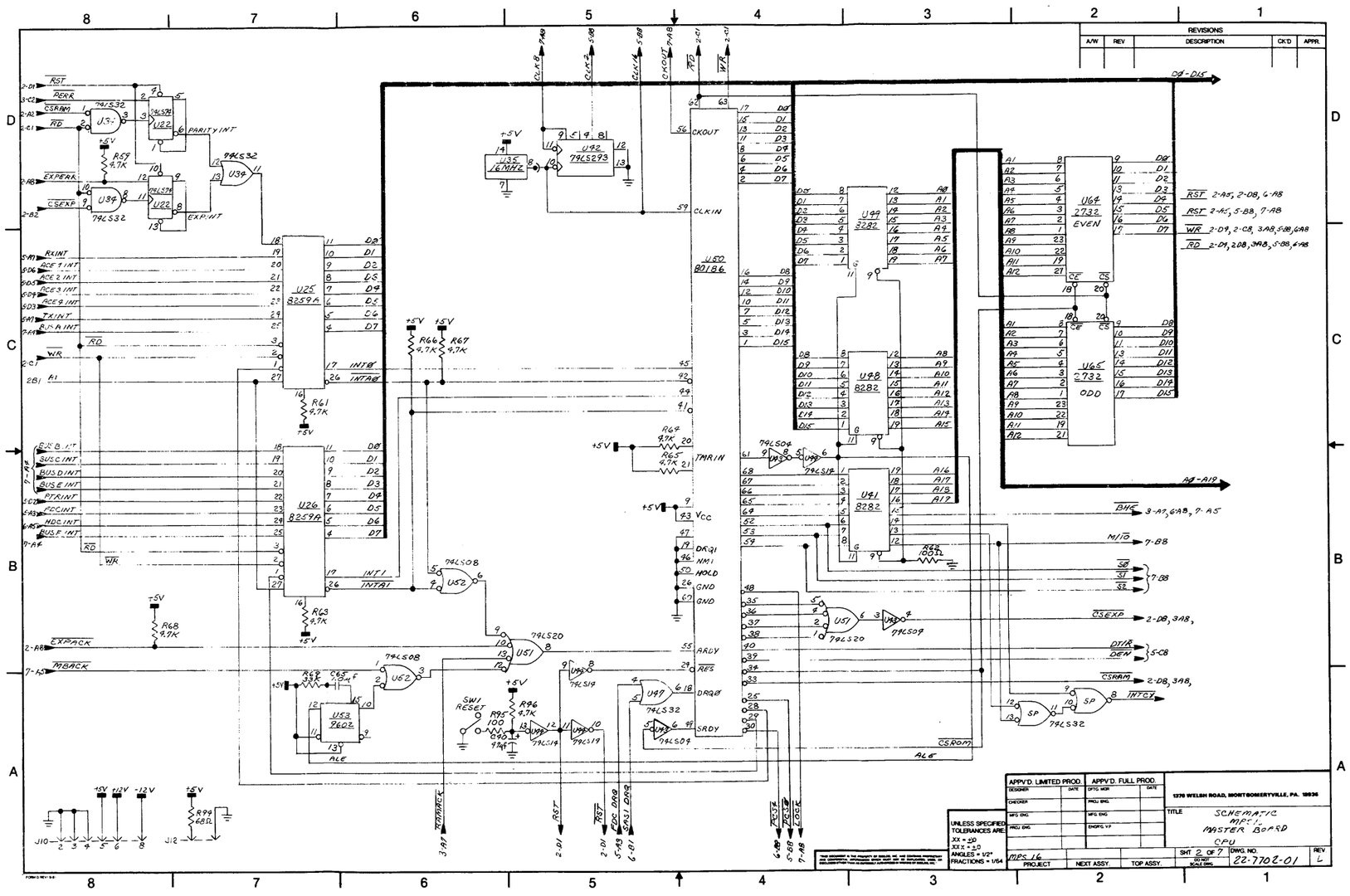


Figure 4-1. Master Board Component Assembly Schematic
(Part 2 of 7)

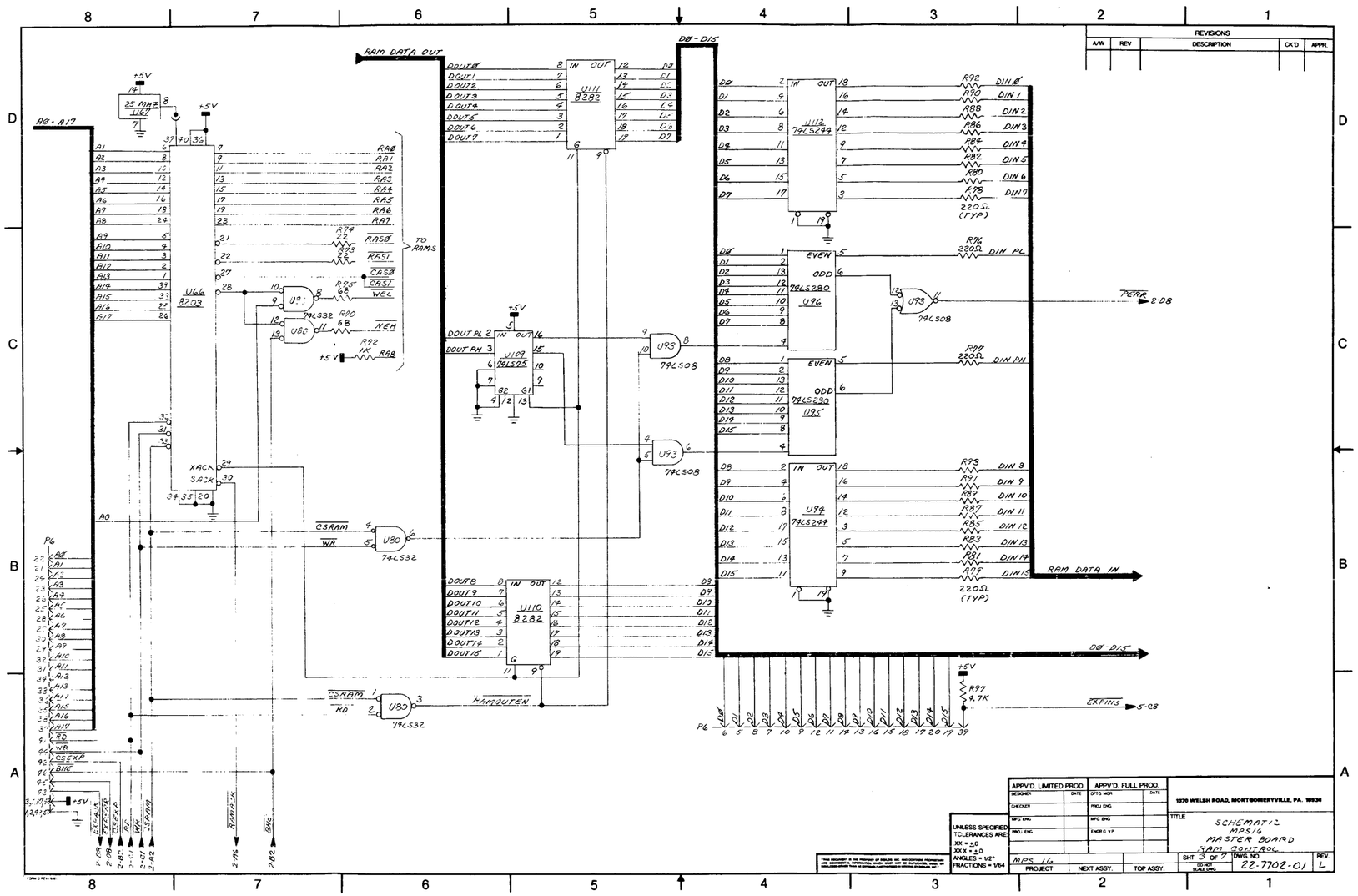


Figure 4-1. Master Board Component Assembly Schematic
(Part 3 of 7)

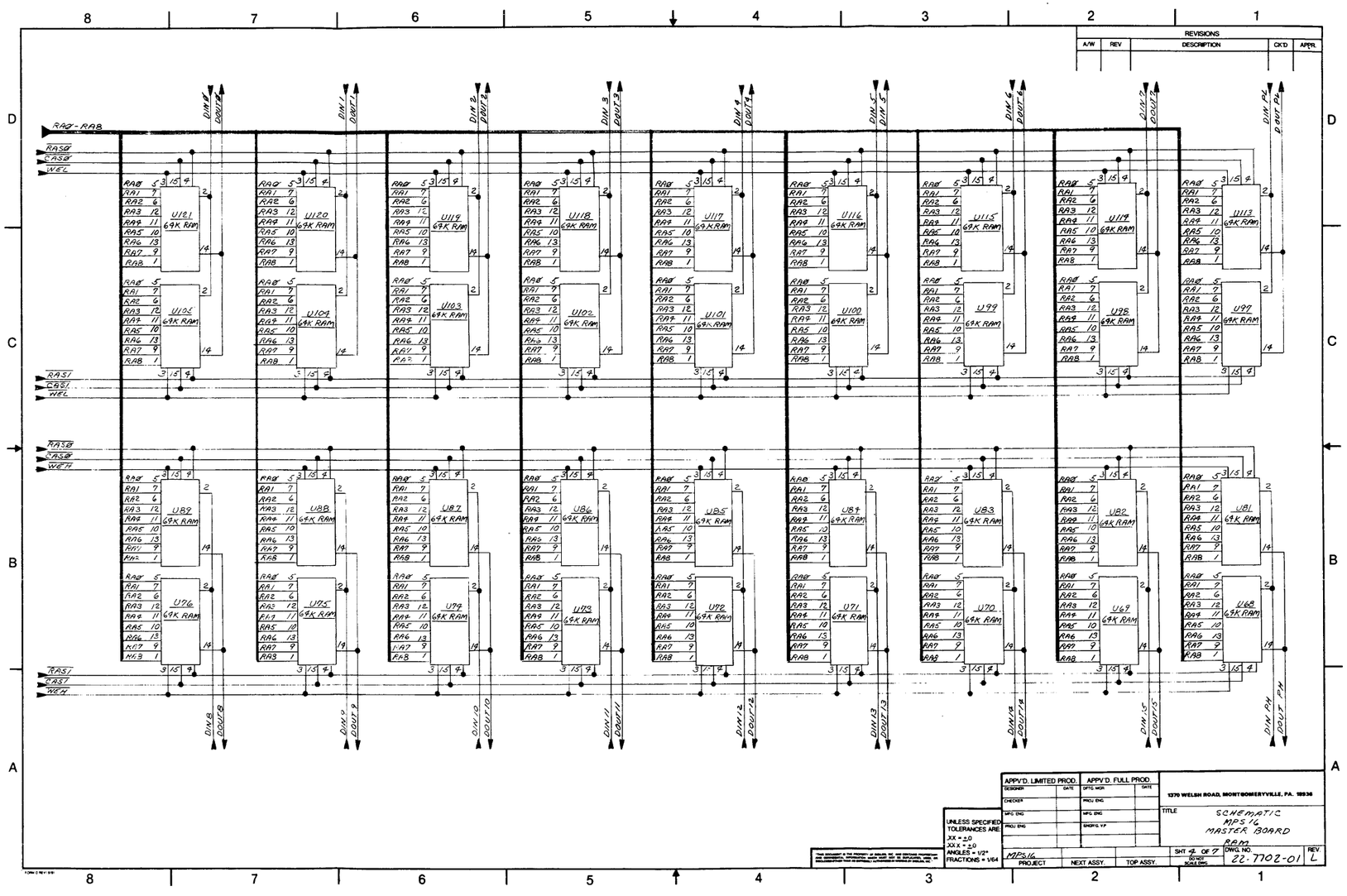


Figure 4-1. Master Board Component Assembly Schematic
(Part 4 of 7)

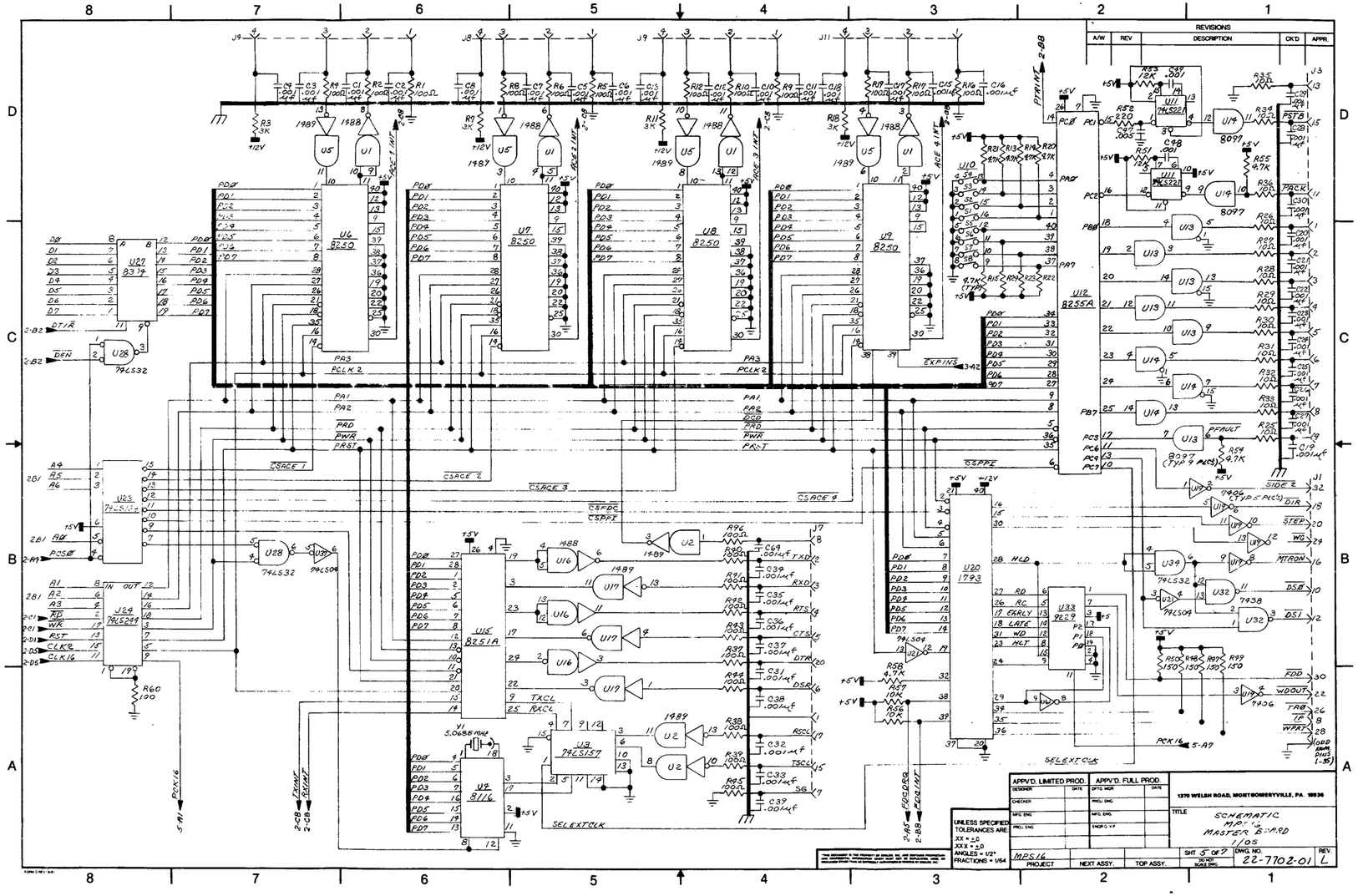


Figure 4-1. Master Board Component Assembly Schematic
(Part 5 of 7)

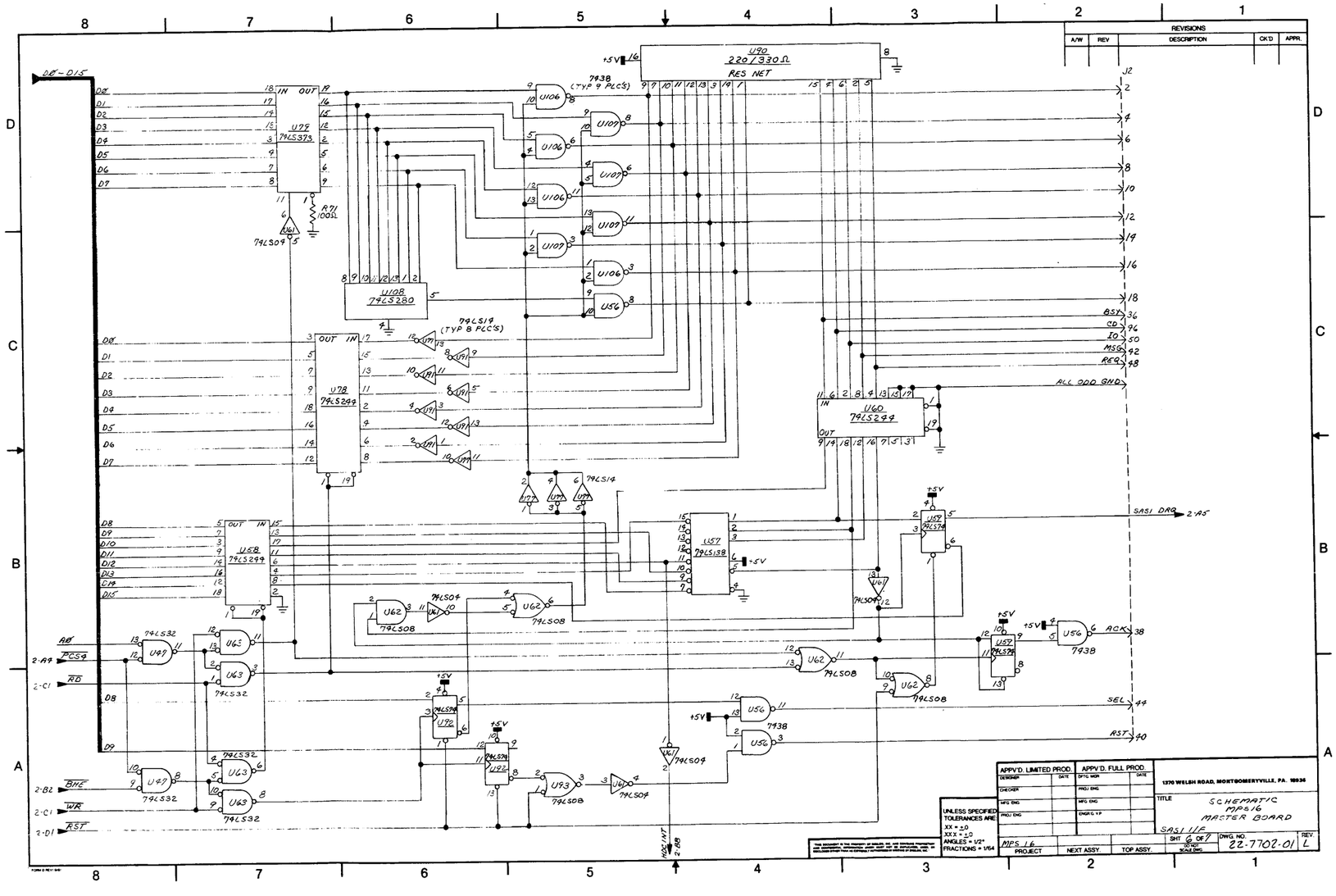


Figure 4-1. Master Board Component Assembly Schematic
(Part 6 of 7)

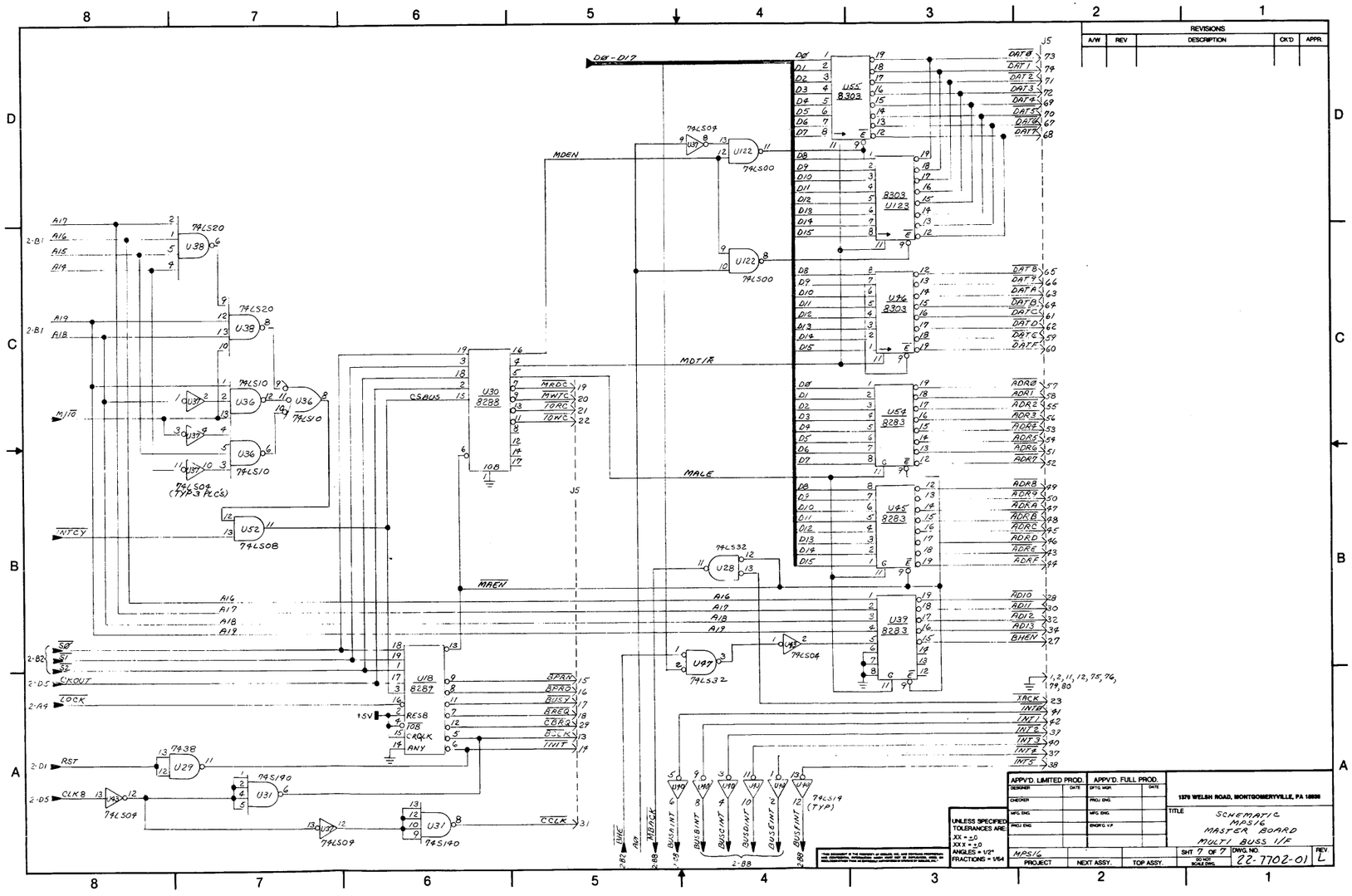


Figure 4-1. Master Board Component Assembly Schematic
(Part 7 of 7)

Table 4-1. Master Board Summary Parts List (Part 1 of 3)

PART NUMBER	DESCRIPTION	REMARKS
22-7702-01	Master Board Ass'y.	Board with components
65-0111-00	Connector, Fem., 4-Pos.	J4,J8,J9,J11
65-0100-50	Connector, Male, 50-Pos.	J2(SCSI),J6(RAM-EXP)
65-0100-34	Conn. Male, 34-Pos.	J1 (Floppy)
65-0094-00	Conn. Skt., 68-Pos.	U50
65-0065-40	Conn. DIP, 40-Pos.	U6-U9,U12,U20,U66
65-0065-28	Conn. DIP, 28-Pos.	U15,U25,U26
65-0065-16	Conn. DIP, 16-Pos.	U68-U76, U81-U89, U97-U105, U113-U121
65-0064-24	Conn. Fem., 24-Pos.	U64,U65
60-0034-0	Conn. Male, 8-Pos.	J10 (PWR)
65-0107-00	Conn. Fem., 40-Pos.	J5
65-0105-01	Conn. Fem., 15-Pos.	J3
65-0105-02	Conn. Fem., 25-Pos.	J7
65-0079-00	Conn. Male, 2-Pos.	J12
60-0425-0	Switch, P/B-SPDT	SW1
60-0437-0	Switch, DIP-SPSTx8	U10
50-0006-0	IC, TTL-7406	U19
50-0038-00	IC, TTL-7438	U29,U56,U106,U107, U32
50-4140-00	IC, TTL-74S140	U31
50-5024-0	IC, DM8097	U13,U14
50-5088-0	IC, LIN-1488	U1,U16
50-5089-0	IC, LIN-1489	U2,U5,U17
50-5123-00	IC, LIN-8303	U46,U55,U123
50-6036-0	IC, LSI-8255	U12
50-6088-0	IC, LIN-8304B	U27
50-6091-0	IC, INS8250	U6-U9
50-6105-00	IC, LSI-1793-02	U20
50-6109-00	IC, LSI-8116	U4
22-7109-00	IC, Boot PROM Set	U64,U65
50-6115-00	IC, RAM-64Kx1	U68-U76, U81-U89, U97-U105, U113-U121
50-6120-02	IC, uPC-80186	U50
50-6121-00	IC, LSI-8203	U66
50-6131-00	IC, LSI-8282	U41,U48,U49, U110-U111
50-6132-00	IC, LSI-8283	U39,U45,U54
50-6133-00	IC, LSI-8288	U30
50-6134-00	IC, LSI-8289	U18
50-6135-00	IC, LSI-8251A	U15

Table 4-1. Master Board Summary Parts List (Part 2 of 3)

PART NUMBER	DESCRIPTION	REMARKS
50-6136-00	IC, LSI-8259A	U25,U26
50-6137-00	IC, INT-FDC9229B	U33
50-7004-0	IC, SN74LS04N	U21,U37,U43,U61
50-7008-0	IC, SN74LS08N	U52,U62,U93
50-7010-0	IC, SN74LS10N	U36
50-7014-0	IC, TTL-74LS14	U40,U44,U77,U91
50-7020-0	IC, SN74LS20N	U38,U51
50-7032-0	IC, SN74LS32N	U28,U34,U47,U80, U63, Spare
50-7074-0	IC, SN74LS74N	U22,U59,U92
50-7075-0	IC, TTL-74LS75	U109
50-7221-0	IC, TTL-74LS221	U11
50-7138-0	IC, 74LS138N	U23,U57
50-7157-0	IC, TTL-74LS157	U3
50-7244-0	IC, TTL-74LS244	U24,U58,U60,U78, U94,U112
50-7280-00	IC, TTL-74LS280	U95,U96,U108
50-7293-0	IC, SN74LS293N	U42
50-7373-0	IC, 74LS373-0	U79
50-6041-0	IC, N9602B	U53
50-7000-0	IC, SN74LS00N	U122
55-0310-0	Resistor, 10K Ohms	R56,R57
55-0010-0	Resistor, 10 Ohms	R25-R36
55-0110-0	Resistor, 100 Ohms	R1,R2,R4-R6,R8-R10, R12,R16-R17,R19, R37-R45,R60,R62, R71,R95,R96
55-0115-0	Resistor, 150 Ohms	R47-R50
55-0122-0	Resistor, 220 Ohms	R76-R93, R52
55-0230-0	Resistor, 3K Ohms	R3,R7,R11,R18
55-0247-0	Resistor, 4.7K Ohms	R55,R54, R13-R15, R20-R24, R5,R65, R63,R68,R61, R59,R66,R67,R9
55-5114-00	Resistor, NET 220/330 Ohms	U90
55-0022-0	Resistor, 22 Ohms	R73,R74
55-0068-0	Resistor, 68 Ohms	R70,R75,R94
55-0210-0	Resistor, 1K Ohms	R72
55-0333-0	Resistor, 33K Ohms	R69
55-0312-0	Resistor, 12K Ohms	R51,R53

Table 4-1. Master Board Summary Parts List (Part 3 of 3)

PART NUMBER	DESCRIPTION	REMARKS
56-0053-0	Capacitor, TAN-22uF	C95,C44,C45,C43, C61,C53,C73
56-1102-00	Capacitor, CER-0.001uF	C1-C8, C10-C13, C15-C39,C48,C49,C64
56-0046-0	Capacitor, TAN-47uF	C40
56-0014-0	Capacitor, CER-0.005uF	C47
56-0081-0	Capacitor, CER-1.0uF	C65
15-1116-1	Crystal Osc., 5.0688MHz	Y1
57-1001-06	Crystal Osc., 25MHz	U67
57-1001-08	Crystal Osc., 16MHz	U35
51-0003-0	Diode, 1N914 or 1N3064 (alt)	CR1

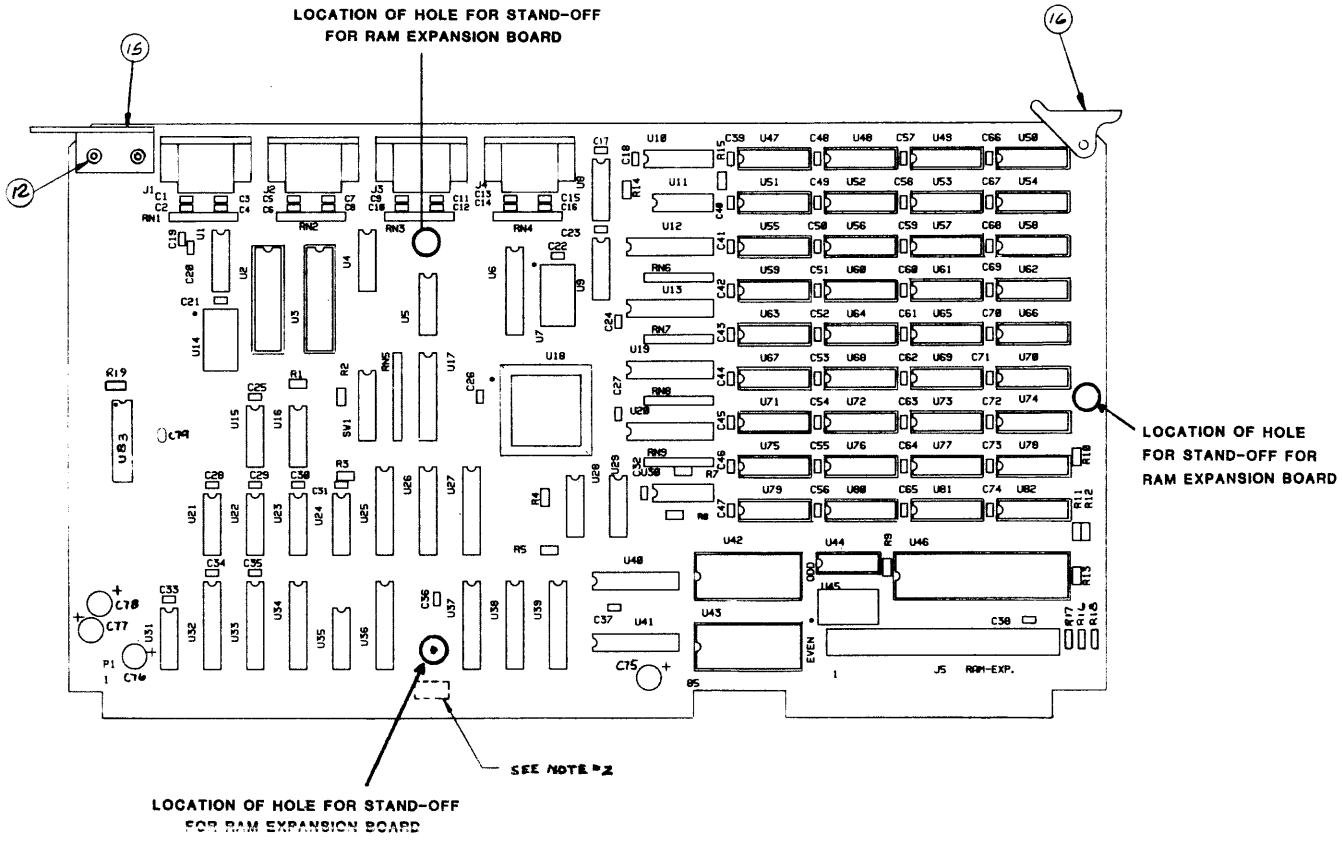


Figure 4-2. Slave Board Component Assembly Schematic
(Part 1 of 4)

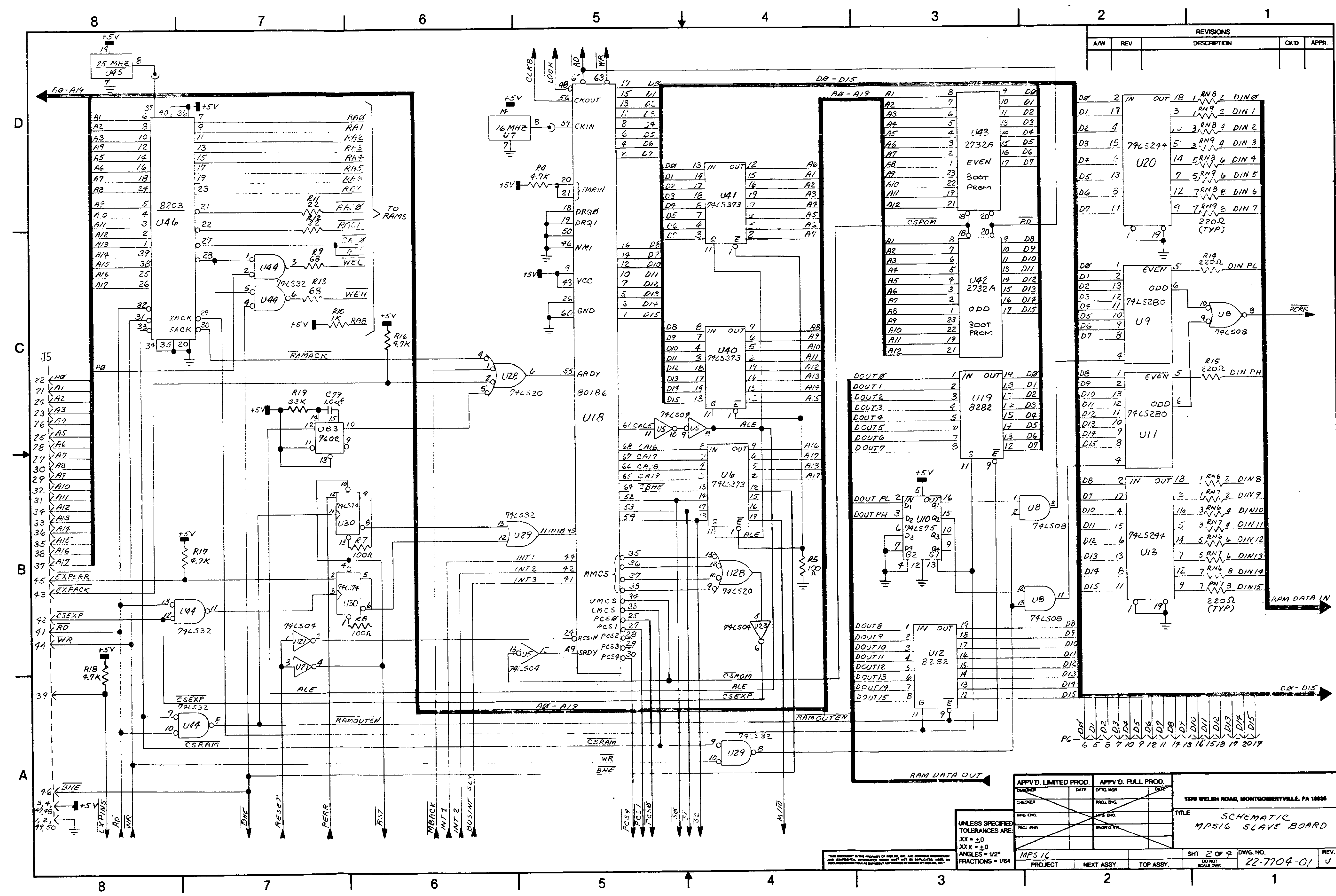


Figure 4-2. Slave Board Component Assembly Schematic
(Part 2 of 4)

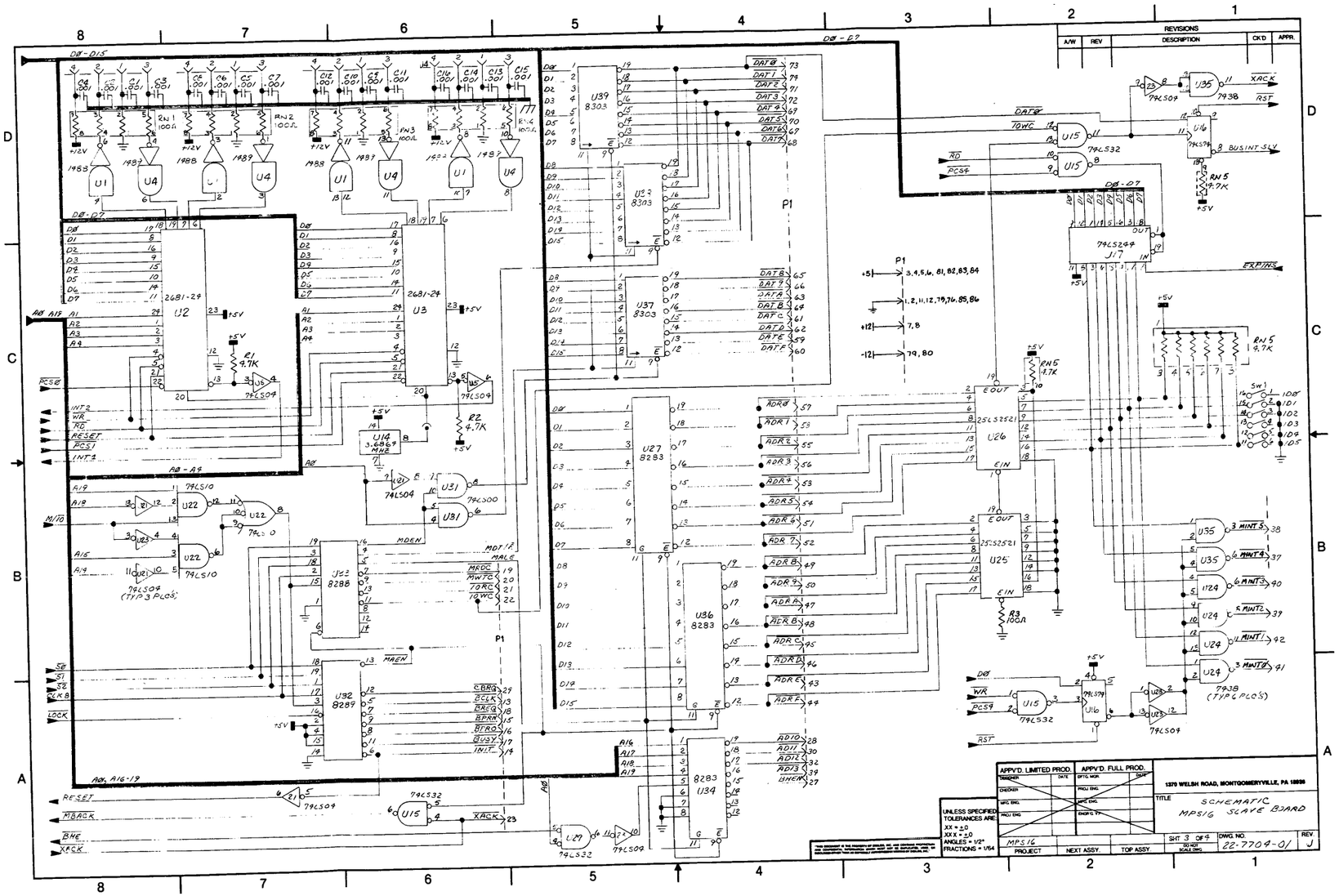


Figure 4-2. Slave Board Component Assembly Schematic
(Part 3 of 4)

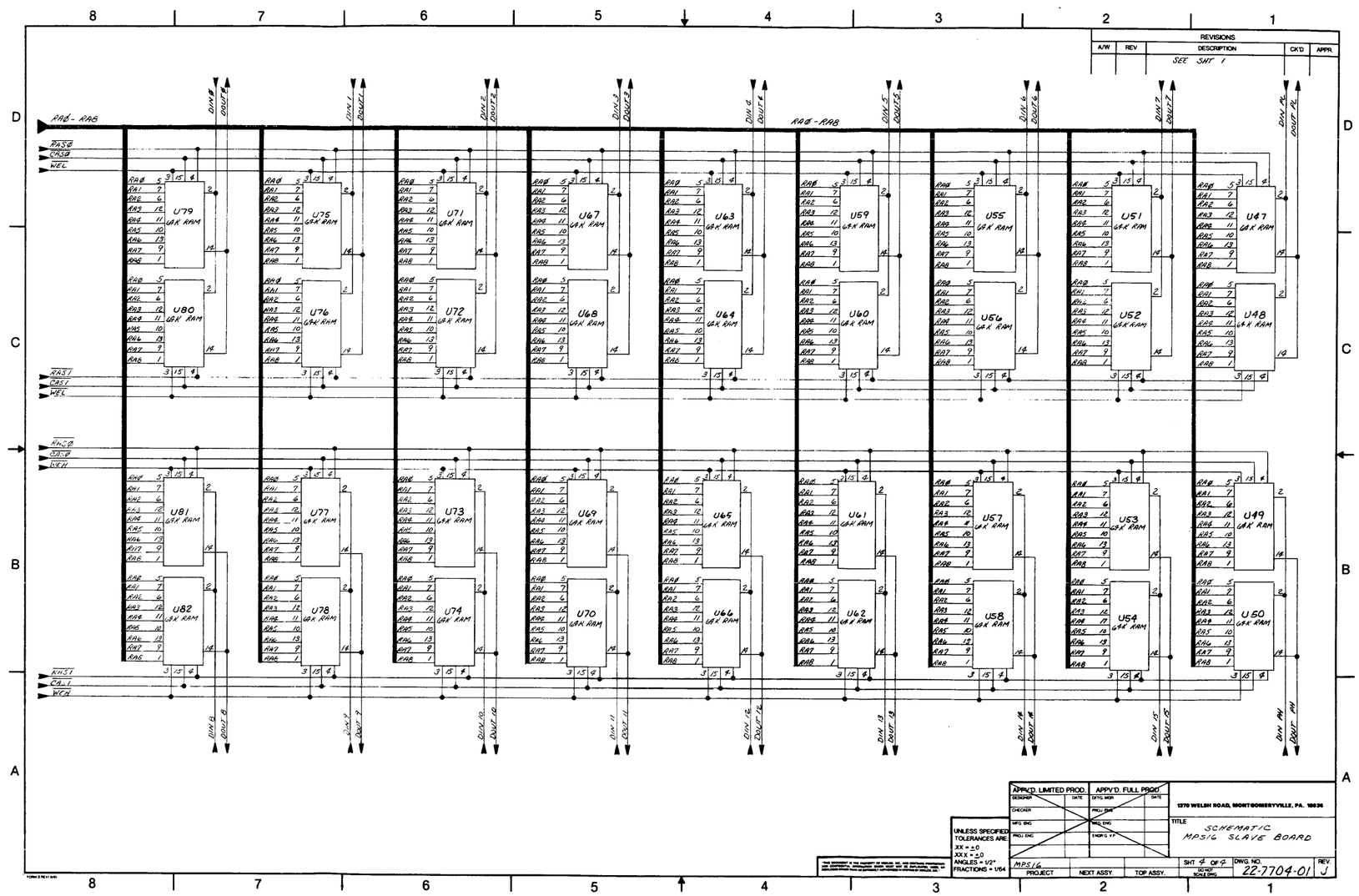


Figure 4-2. Slave Board Component Assembly Schematic
(Part 4 of 4)

Table 4-2. Slave Board Summary Parts List (Part 1 of 2)

PART NUMBER	DESCRIPTION	REMARKS
22-7704-01	Slave Board	Complete assembly
65-0111-00	Connector, Fem. 4 Pos.	J1-J4
65-0100-50	Connector, Male 50 Pos.	J5 (RAM-EXP.)
65-0094-03	Connector, SKT 68 Pos.	U18
65-0064-24	Connector, Fem. 24 Pos.	U42,U43
65-0065-16	Connector, DIP 16 Pos.	U47-U82
65-0065-40	Connector, DIP 40 Pos.	U46
65-0113-00	Connector, Fem. 24 Pos.	U2,U3
60-0437-0	Switch, DIP SPSTx8	SW1
50-5088-0	IC, LIN-1488	U1
50-5124-00	IC, LSI-DUAL UART	U2,U3
50-5089-0	IC, LIN-1489	U4
50-7004-0	IC, SN74LS04N	U5,U21,U23
50-7373-0	IC, 74LS373-0	U6,U40,U41
50-7008-0	IC, SN74LS08N	U8
50-7280-00	IC, TTL-74LS280	U9,U11
50-6131-00	IC, LSI-8282	U12,U19
50-7074-0	IC, SN74LS74N	U16,U30
50-6120-02	IC, uPC-80186	U18
50-7010-0	IC, SN74LS10N	U22
50-0038-00	IC, TTL-7438	U24,U35
50-7075-0	IC, TTL-74LS75	U10
50-6138-00	IC, LSI-25LS2521	U25,U26
50-6132-00	IC, LSI-8283	U27,U34,U36
50-7020-0	IC, SN74LS20N	U28
50-7000-0	IC, SN74LS00N	U31
50-6134-00	IC, LSI-8289	U32
50-6133-00	IC, LSI-8288	U33
50-5123-00	IC, LIN-8303	U37,U38,U39
22-7120-00	IC, Boot PROM Set	U43,U42
50-6121-00	IC, LSI-8203	U46
50-6115-00	IC, RAM 64Kx1	U47-U82
50-7032-0	IC, SN74LS32N	U13,U17,U20
50-6041-0	IC, N9602B	U83
50-7244-0	IC, TTL-74LS244	U13,U17,U20
57-1001-08	Crystal, 16MHz	U7
57-1002-00	Crystal, 3.6864MHz	U14
57-1001-06	Crystal, 25MHz	U45

Table 4-2. Slave Board Summary Parts List (Part 2 of 2)

PART NUMBER	DESCRIPTION	REMARKS
55-0068-0	Resistor, 68 Ohms	R9,R13
55-0110-0	Resistor, 100 Ohms	R3,R5,R7,R8
55-0210-0	Resistor, 1K Ohms	R10
55-0247-0	Resistor, 4.7K Ohms	R1,R2,R4,R16 R17,R18
55-0122-0	Resistor, 220 Ohms	R14,R15
55-5115-00	Res. Pak 4x100 Ohms	RN1-RN4
55-5116-00	Res. Pak 4x220 Ohms	RN6-RN9
55-5117-00	Res. Net 9x4.7K Ohms	RN5
55-0022-0	Resistor, 22 Ohms	R11,R12
55-0333-0	Resistor, 33K Ohms	R19
56-0053-0	Capacitor, TAN 22uF	C75-C78
56-0081-00	Capacitor, ELE 1uF	C79
56-1102-00	Capacitor, CER .001uF	C1-C16
56-1104-00	Capacitor, CER .1uF	C17-C26,C28-C74

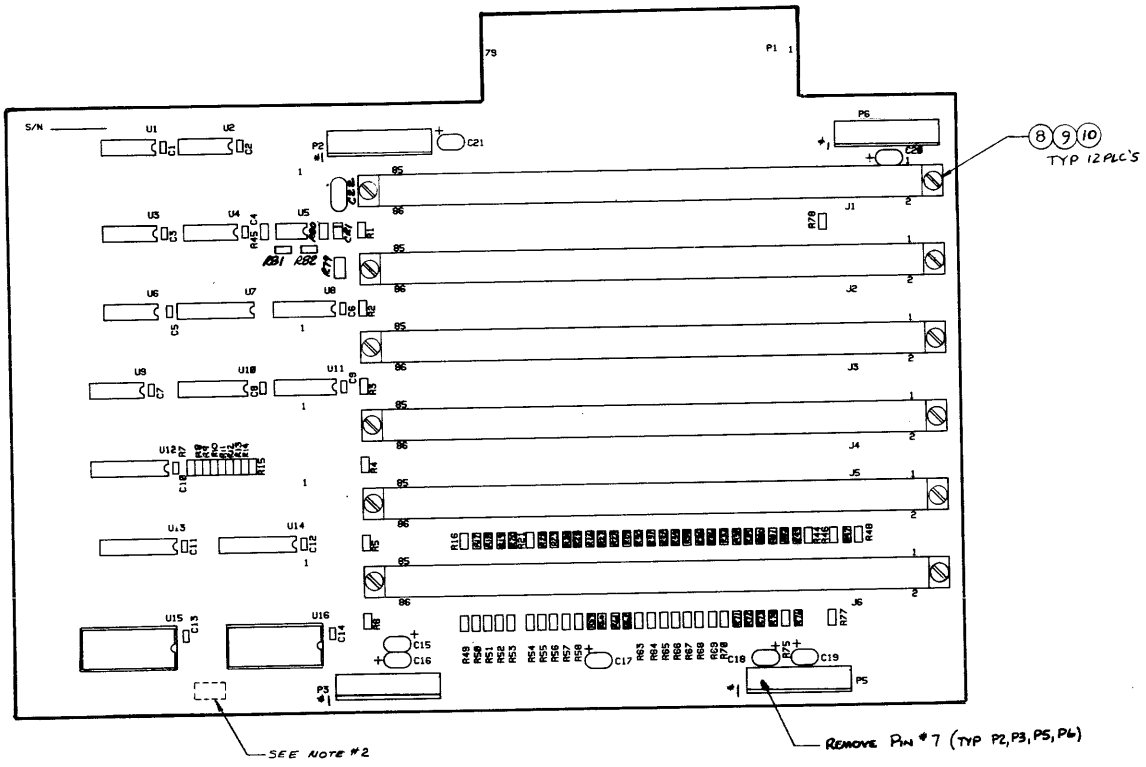


Figure 4-3. Mother Board Component Assembly Schematic
(Part 1 of 3)

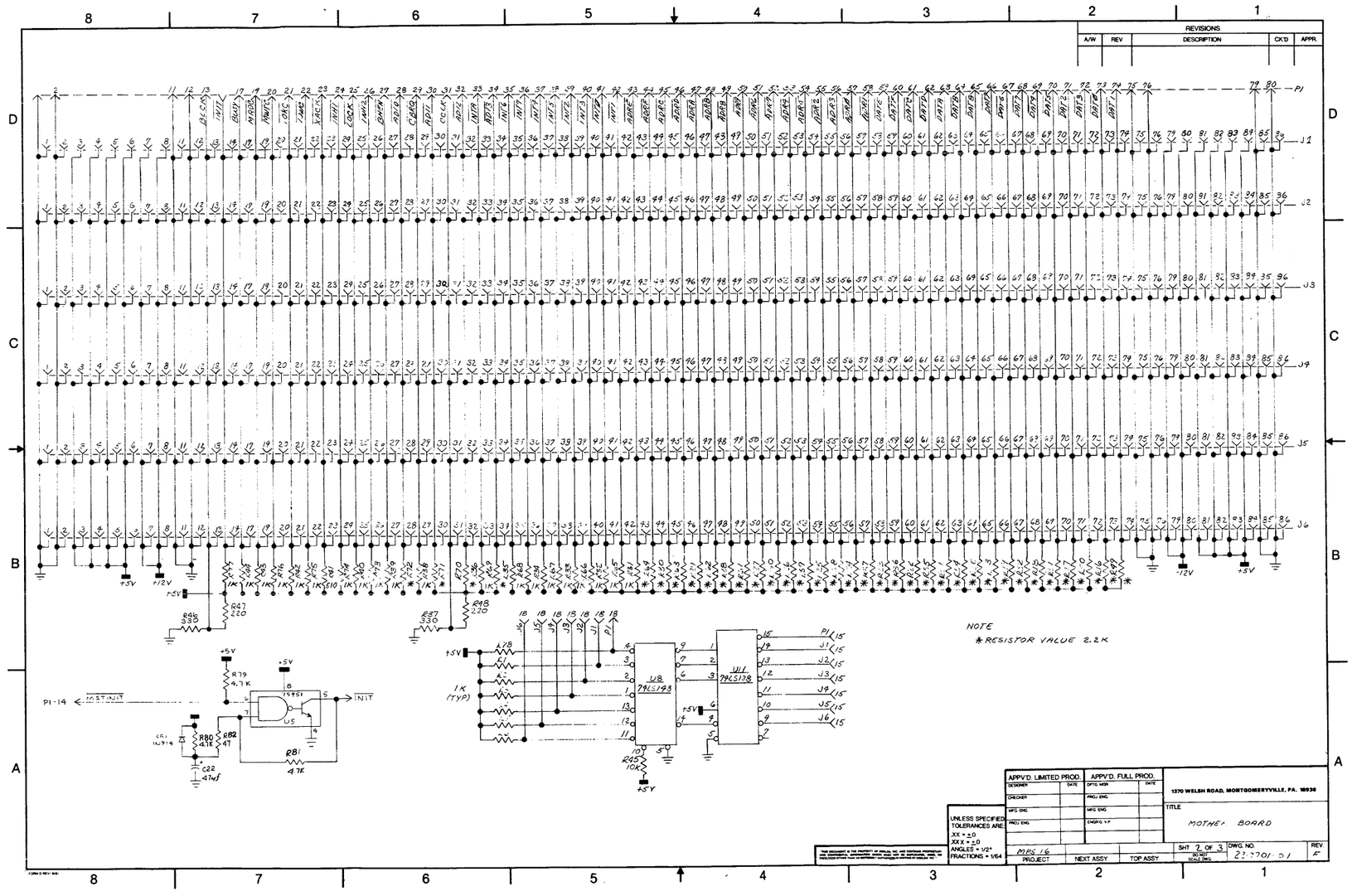


Figure 4-3. Mother Board Component Assembly Schematic
(Part 2 of 3)

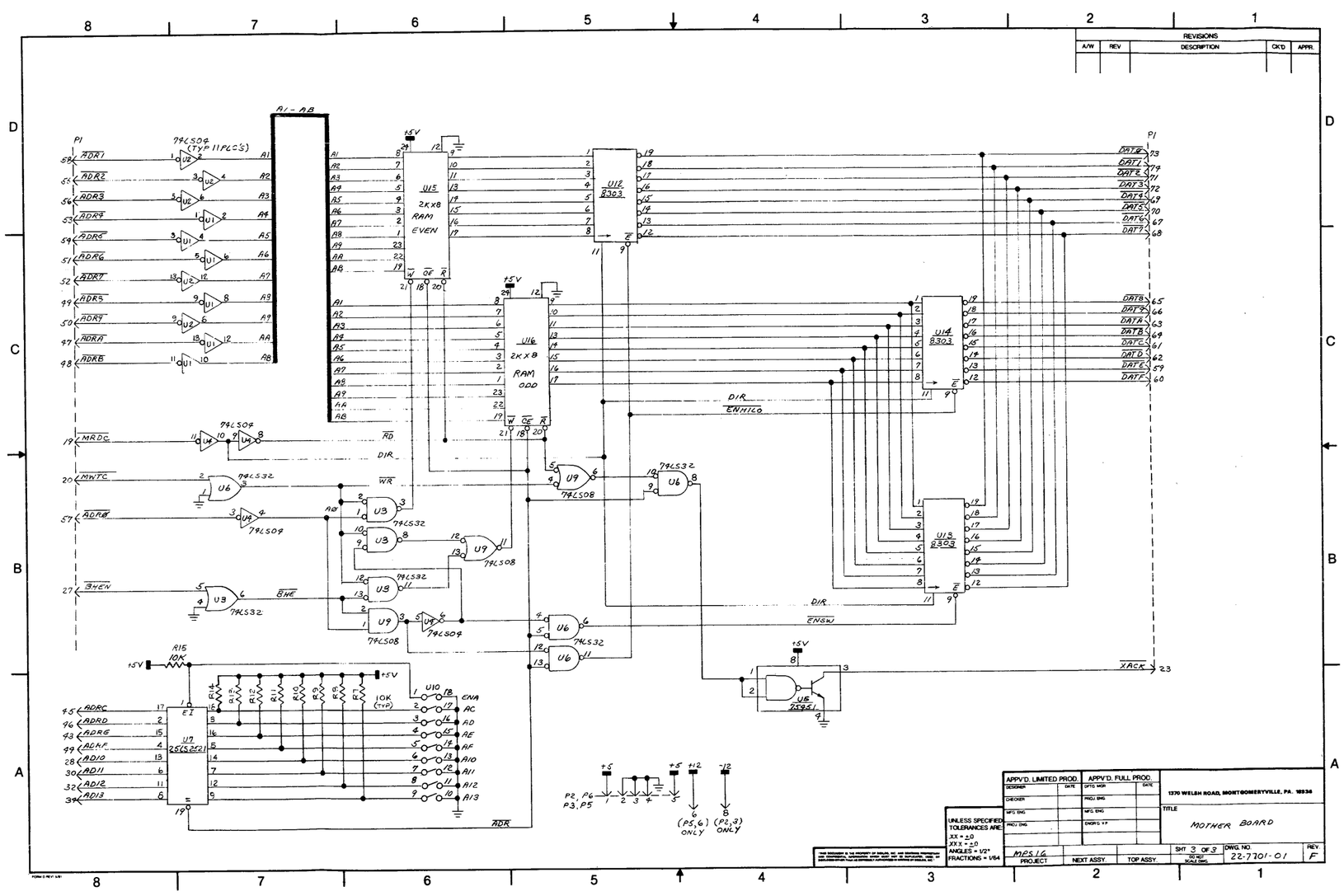


Figure 4-3. Mother Board Component Assembly Schematic
(Part 3 of 3)

Table 4-3. Expansion Box: Mother Board Summary Parts List

PART NUMBER	DESCRIPTION	REMARKS
22-7701-01	Mother Board Assembly	Complete
60-0034-0	Connector, Male, 8 pos.	P2,P3,P5,P6
65-0108-00	Connector, Fem., 43 pos.	J1-J6
65-0065-24	Connector, DIP 24 pos.	U15,U16
84-0032-09	Switch, DIP SPSTx9	U10
50-5123-00	IC, LIN-8303	U12-U14
50-5128-00	IC, 75451B	U5
50-6123-00	IC, RAM 16K, Static	U15,U16
50-6138-00	IC, LSI-25LS2521	U7
50-7004-0	IC, SN74LS04N	U1,U2,U4
50-7008-0	IC, SN741S08N	U9
50-7032-0	IC, SN74LS32N	U3,U6
50-7138-0	IC, 74LS138N	U11
50-7148-0	IC, TTL-74LS148	U8
55-0122-0	Resistor, 220 Ohms	R47,R48
55-0133-0	Resistor, 330 Ohms	R46,R37
55-0210-0	Resistor, 1K Ohms	R1-R6,R32-R36, R38-R40,R42-R44, R66-R68,R73-R78
55-0222-0	Resistor, 2.2K Ohms	R16-R31,R49-R64, R69-R73
55-0310-0	Resistor, 10K Ohms	R7-R15,R45
55-0151-0	Resistor, 510 Ohms	R41
55-0247-0	Resistor, 4.7K Ohms	R79,R80,R81
55-0047-0	Resistor, 47 Ohms	R82
56-0053-0	Capacitor, TAN-22uF	C15-C21
56-1104-00	Capacitor, CER-0.1uF	C1-C14
56-0046-0	Capacitor, TAN-47uF	C22
51-0003-0	Diode, IN914	CR1

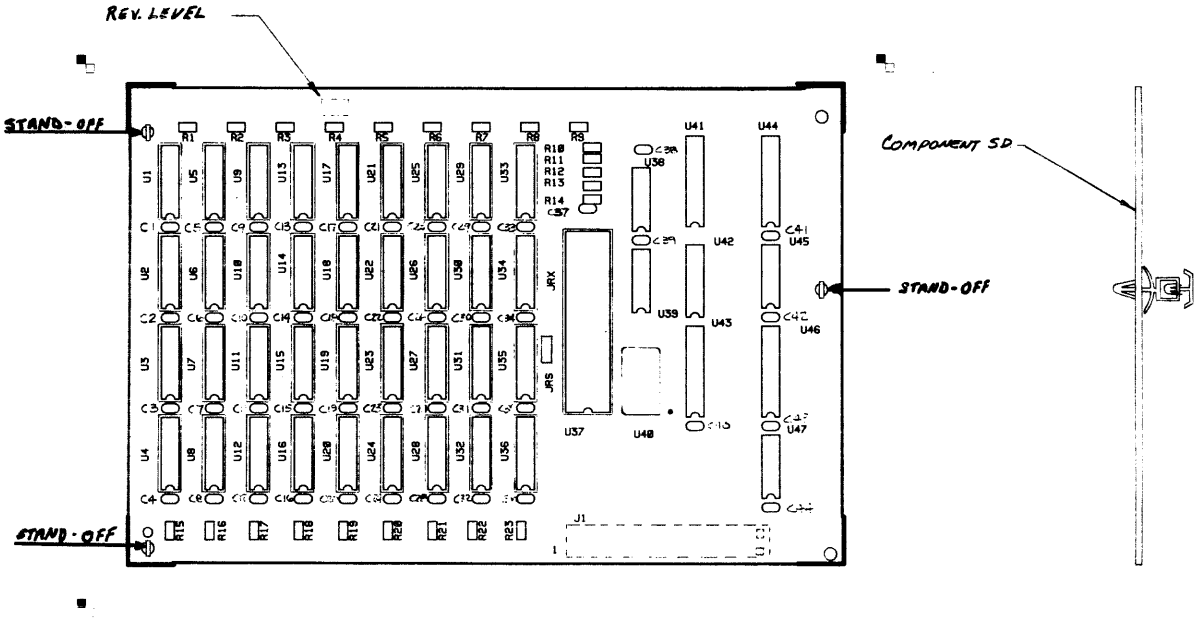


Figure 4-4. Expansion RAM Component Assembly Schematic
(Part 1 of 3)

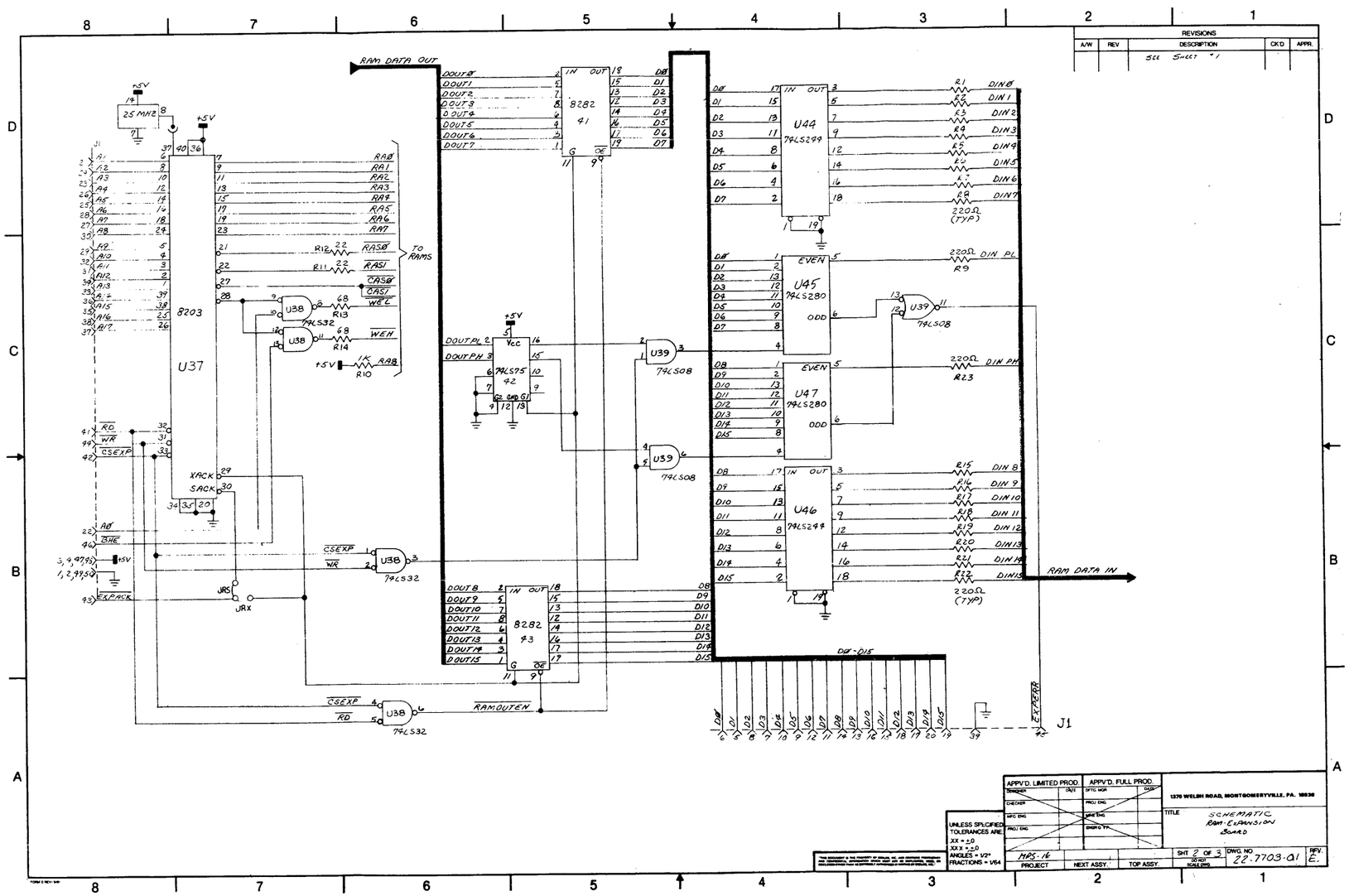


Figure 4-4. Expansion RAM Component Assembly Schematic
(Part 2 of 3)

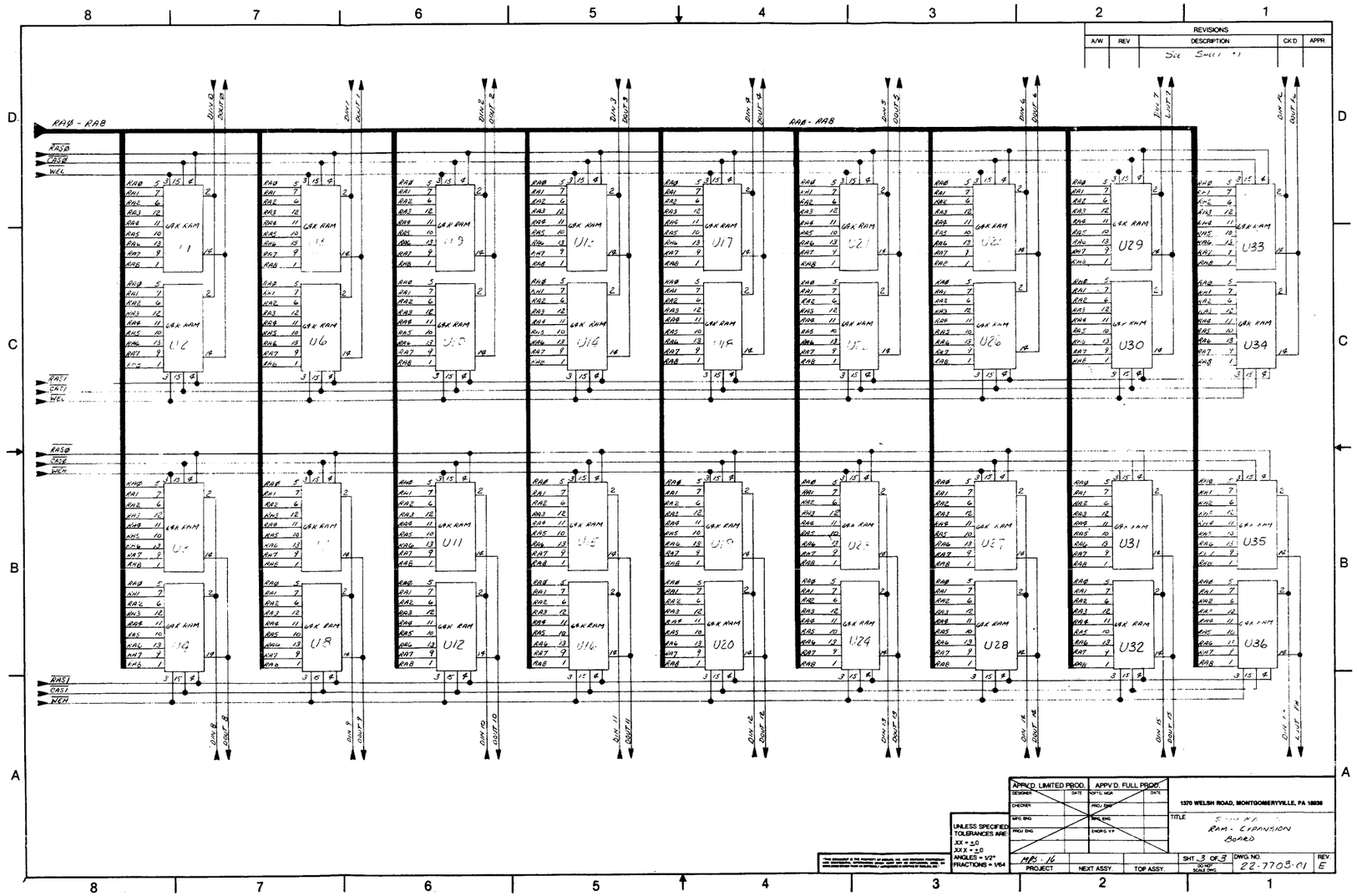


Figure 4-4. Expansion RAM Component Assembly Schematic
(Part 3 of 3)

Table 4-4. Expansion RAM Summary Parts List

PART NUMBER	DESCRIPTION	REMARKS
22-7703-01	Expansion RAM Board	Complete
65-0103-52	Connector, Fem., 52 Pos.	J1
65-0065-16	Connector, DIP, 16 Pos.	U1-U36
65-0065-40	Connector, DIP, 40 Pos.	U37
50-6115-00	IC, RAM 64Kx1	U1-U36
50-6131-00	IC, LSI-8282	U41,U43
50-6121-00	IC, LSI-8203	U37
50-7008-0	IC, SN74LS08N	U39
50-7032-0	IC, SN74LS32N	U38
50-7075-0	IC, TTL-74LS75	U42
50-7244-0	IC, TTL-74LS244	U44,U46
50-7280-00	IC, TTL-74LS280	U45,U47
55-0122-0	Resistor, 220 Ohms	R10-R14
55-0010-0	Resistor, 10 Ohms	JRS
55-0210-0	Resistor, 1K Ohms	R10
55-0022-0	Resistor, 22 Ohms	R11,R12
55-0068-0	Resistor, 68 Ohms	R13,R14
56-1104-00	Capacitor, CER .1uF	C1-C44
57-1001-06	Crystal, 25 MHz	U40

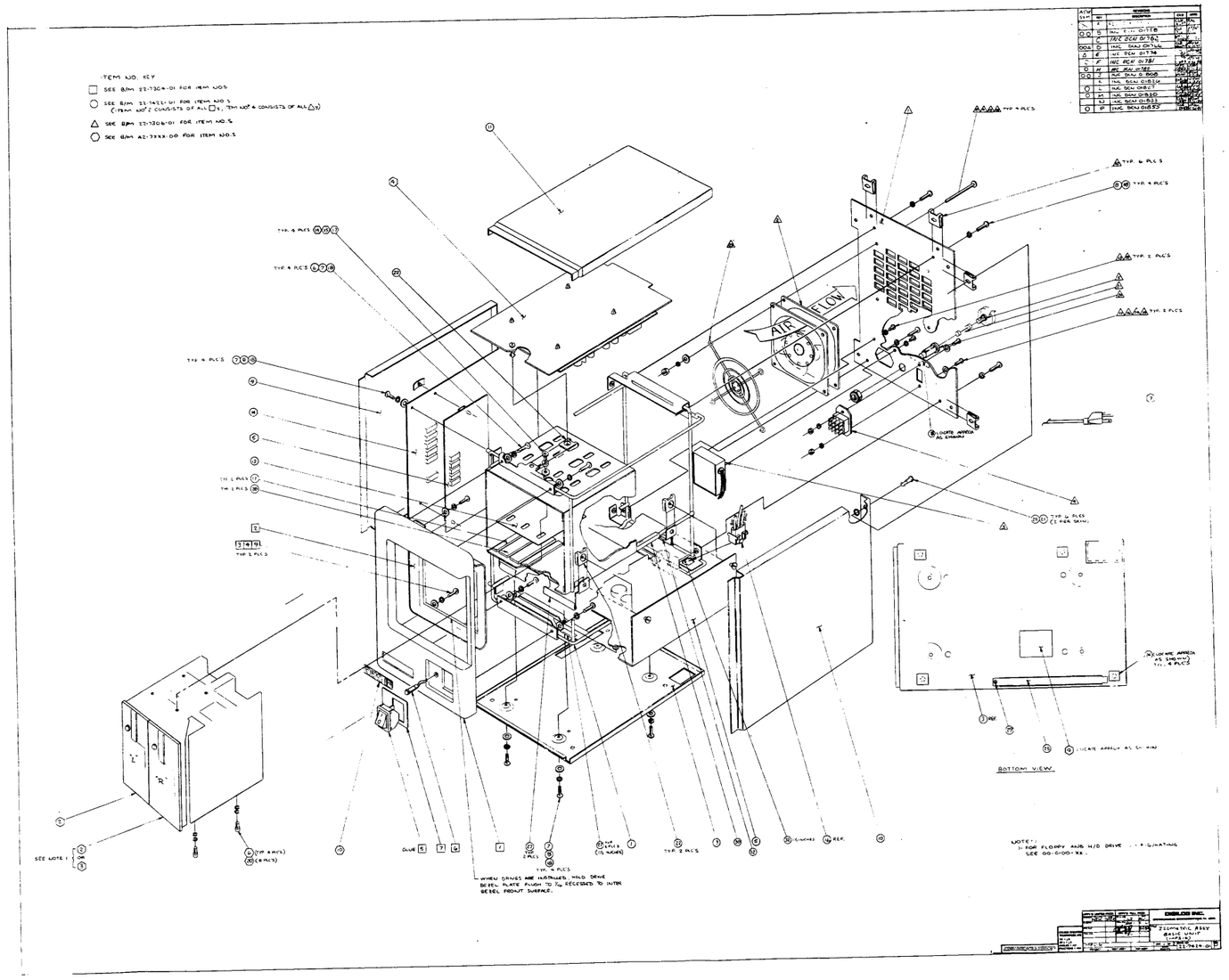


Figure 4-5. Desktop Unit: Isometric Assembly
(Part 1 of 2)

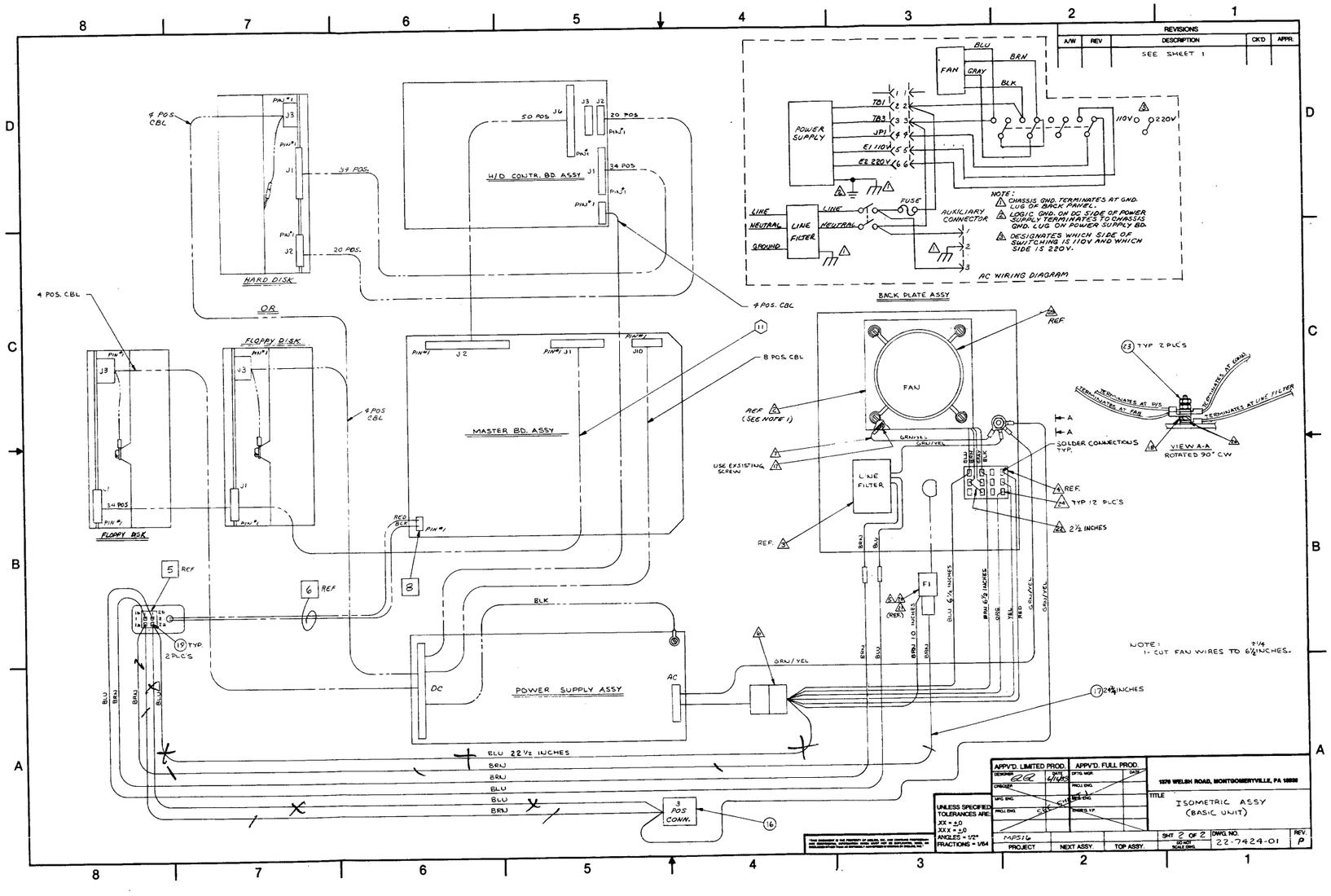


Figure 4-5. Desktop Unit: Isometric Assembly
(Part 2 of 2)

Table 4-5. Desktop Unit Summary Parts List

PART NUMBER	DESCRIPTION	REMARKS
22-7304-01	Front Bezel Assembly	Complete
22-7501-02	Front Cover	
22-7502-02	Bezel Insert	
84-0031-00	Switch, Rocker-DPST	
22-7106-01	Wire Assembly LED	
65-0071-00	Connector, Fem., 2 Pos.	1" center
22-7403-01	Top Cover	
22-7405-01	Side Panel (left)	
22-7407-01	Side Panel (right)	
22-7306-01	Back Plate Assembly	Complete
22-7413-02	Back Plate	
68-1002-00	Cooling Fan	
22-7219-01	Line Filter Assembly	
84-0033-00	Switch, SLD-4PDT	
80-0001-01	Prot, ACC-Fuseholder	
22-7208-01	Cable Assembly	Voltage Select to P/S Connector
19-4212-56	Wire Assembly (white)	
80-0002-0	ACC-Fuse carrier	
60-0460-0	Fuse 2A, 250 Vac	
60-0493-0	Fan Finger Guard	
78-0051-00	Hard Disk Controller	
22-7205-01	Cable Assembly	Disk to Controller
22-7206-01	Cable Assembly	Controller to Master
22-7212-01	Cable Assembly	Hard Disk Data
22-7301-01	Controller Mtg. Board	
78-0049-00	Power Supply	
22-7411-01	Power Supply chassis	
22-7210-01	Cable Assembly	Single Floppy Drive
22-7209-01	Cable Assembly	Master Board
22-7220-01	Cable Assembly	Hard Disk or Floppy
22-7202-01	Cable Assembly	Power Supply to Voltage Select Sw.
22-7204-01	Cable Assembly	Hard Disk Controller

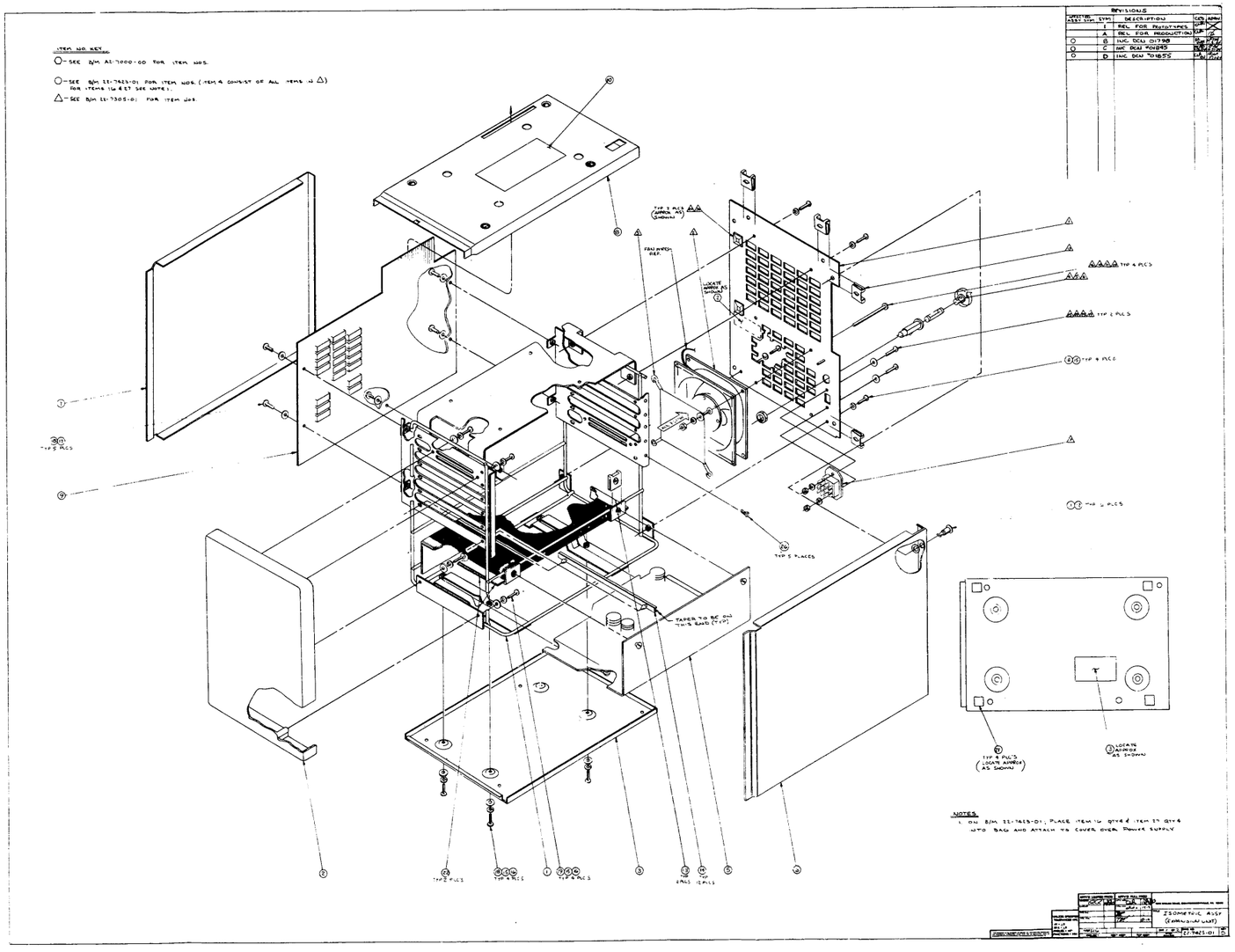


Figure 4-6. Expansion Box: Isometric Assembly
(Part 1 of 2)

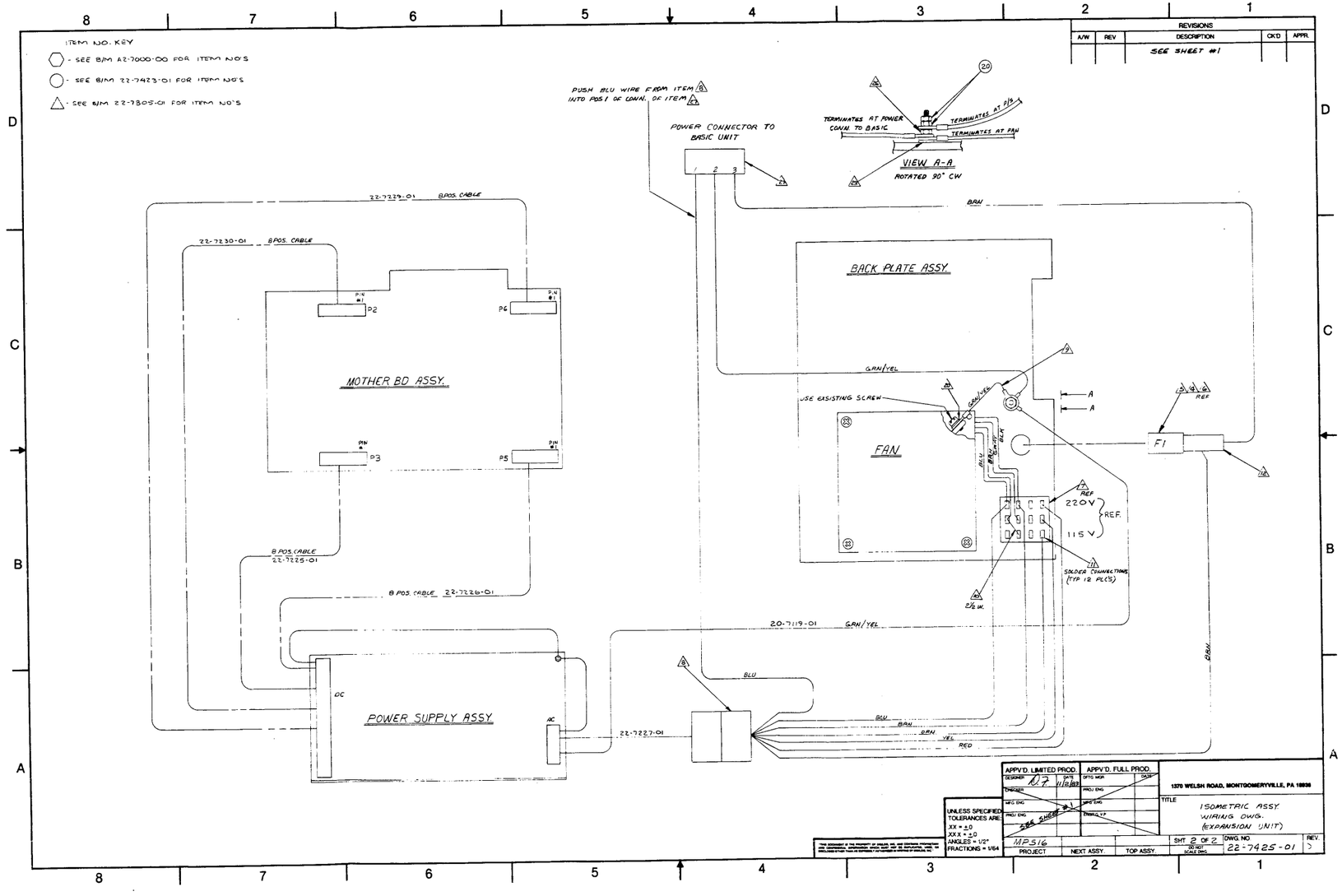


Figure 4-6. Expansion Box: Isometric Assembly
(Part 2 of 2)

Table 4-6. Expansion Box Summary Parts List

PART NUMBER	DESCRIPTION	REMARKS
A2-7000-00	Expansion Box	Complete
74-0026-01	Card Guide	
22-7503-02	Front Cover	
22-7410-01	Bottom Plate	
22-7402-01	Wire Frame	
22-7405-02	Left Panel	
22-7407-02	Right Panel	
22-7404-02	Top Cover	
22-7308-01	Power Supply	Complete
22-7411-02	Chassis (Power Supply)	
22-7226-01	Cable Assembly	Power Supply to Mother Bd. (+12)
22-7225-01	Cable Assembly	P.S. to Mother (-12)
22-7229-01	Cable Assembly	P.S. to Mother (+12)
22-7230-01	Cable Assembly	P.S. to Mother (-12)
22-7227-01	Cable Assembly	P.S. to Voltage Selector switch
68-1002-00	Fan	
80-0002-00	Fuse Carrier	
80-0001-00	Fuse Holder	
84-0033-00	Voltage Selector switch	
22-7211-01	Cable Assembly	Interconnect Expansion Box to Desktop Unit
22-7228-01	Cable Assembly	Voltage Sel. to P.S.
22-7414-02	Backplate	

DBS 16 HARDWARE DESCRIPTION AND MAINTENANCE MANUAL

APPENDIX A
CONNECTOR PIN LISTS

Pins not listed are not connected to any circuitry and should present a high impedance. The slash or "/" symbol before a signal name indicates a low level representing a true condition.

Table A-1. Desktop Unit

MASTER BOARD

J1 -- FLOPPY DISK CONTROL PORT

Pin	Signal	Purpose
8	/IP	Index pulse
10	/DS0	Drive select 0
12	/DS1	Drive select 1
16	/MTRON	Motor on
18	/DIR	Step direction select
20	/STEP	Step
22	/WDOUT	Precompensated write data (to disk)
24	/WG	Write gate enable
26	/TR0	Track 0
28	/WPRT	Write protected
30	/FDD	Raw floppy disk data
32	/SIDE2	Head select

J2 -- SCSI INTERFACE PORT

Pin	Signal	Purpose
All Odd	Ground	
2	D0	Data Line
4	D1	" "
6	D2	" "
8	D3	" "
10	D4	" "
12	D5	" "
14	D6	" "
16	D7	" "
18	/PARITY	Parity bit
36	/BSY	Hard disk busy
38	/ACK	Acknowledge
40	/RST	Reset
42	/MSG	Message - command completed

MASTER BOARD

Pin	Signal	Purpose
44	/SEL	Hard disk select
46	/CD	Command, message, or status (low); or data
48	/REQ	Request from Hard Disk
50	/IO	Input (low) or output

J3 -- PARALLEL OUTPUT ONLY PORT (PRINTER)

Pin	Signal	Purpose
1	PD0	Data Line
2	PD1	" "
3	PB2	" "
4	PD3	" "
5	PD4	" "
6	PD5	" "
7	PD6	" "
8	PD7	" "
9	/PFAULT	Printer fault
11	/PACK	Printer acknowledge
13	Ground	
15	/PSTB	Printer data strobe

J4, J8, J9, J11 -- SERIAL ASYNCHRONOUS PORTS A-D (TERMINALS)

Pin	Signal	Purpose
1	Ground	
2	Transmit	Transmit data
3	Receive	Receive data
4	+12 V	

J5 -- MULTIBUS INTERFACE PORT

Pin	Signal	Purpose
1	Ground	
2	Ground	
11	Ground	
12	Ground	
13	/BCLK	Bus clock
14	/INIT	Initialize = system reset

MASTER BOARD

Pin	Signal	Purpose
15	/BPRN	Bus priority in signals MULTIBUS available
17	/BUSY	MULTIBUS is in use
18	/BREQ	MULTIBUS request
19	/MRDC	Memory read command
20	/MWTC	Memory write command
21	/IORC	I/O read command
22	/IOWC	I/O write command
23	/XACK	Transfer of data acknowledged
27	/BHEN	Bus high enable
28	/AD10	Address line
29	/CBRQ	Common bus request
30	/AD11	Address line
31	/CCLK	Inverted 8 MHz clock
32	/AD12	Address line
34	/AD13	Address line
37	/INT4	Interrupt Line
38	/INT5	" "
39	/INT2	" "
40	/INT3	" "
41	/INT0	" "
42	/INT1	" "
43	/ADRE	Address Line
44	/ADRF	" "
45	/ADRC	" "
46	/ADRD	" "
47	/ADRA	" "
48	/ADRB	" "
49	/ADR8	" "
50	/ADR9	" "
51	/ADR6	" "
52	/ADR7	" "
53	/ADR4	" "
54	/ADR5	" "
55	/ADR2	" "
56	/ADR3	" "
57	/ADR0	" "
58	/ADR1	" "
59	/DATE	Data Line
60	/DATF	" "
61	/DATC	" "
62	/DATD	" "
63	/DATA	" "
64	/DATB	" "
65	/DAT8	" "
66	/DAT9	" "

MASTER BOARD

Pin	Signal	Purpose
67	/DAT6	Data Line
68	/DAT7	" "
69	/DAT4	" "
70	/DAT5	" "
71	/DAT2	" "
72	/DAT3	" "
73	/DAT0	" "
74	/DAT1	" "
75	Ground	
76	Ground	
79	Ground	
80	Ground	

J7 -- ASYNCHRONOUS/SYNCHRONOUS SERIAL PORT

Pin	Signal	Purpose
1	Ground	
2	TXD	Transmit Data Output
3	RXD	Receive Data Input
4	RTS	Request To Send
5	CTS	Clear To Send
6	DSR	Data Set Ready
7	SG	Signal Ground
8	/DCD	Data Carrier Detect
15	TSCL	Select Transceiver Clock
17	RSCL	Select Receiver Clock
20	DTR	Data Terminal Ready

J10 -- POWER SUPPLY CONNECTOR

Pin	Signal
2	Ground
3	Ground
4	Ground
5	+5 V
6	+12 V
8	-12 V

MASTER BOARD

P6 -- RAM EXPANSION CONNECTOR

Pin	Signal	Purpose
1	Ground	
2	Ground	
3	+5 V	
4	+5 V	
5	D1	Data Line
6	D0	" "
7	D3	" "
8	D2	" "
9	D5	" "
10	D4	" "
11	D7	" "
12	D6	" "
13	D9	" "
14	D8	" "
15	D11	" "
16	D10	" "
17	D13	" "
18	D12	" "
19	D15	" "
20	D14	" "
21	A1	Address Line
22	A0	" "
23	A3	" "
24	A2	" "
25	A5	" "
26	A4	" "
27	A7	" "
28	A6	" "
29	A9	" "
30	A8	" "
31	A11	" "
32	A10	" "
33	A13	" "
34	A12	" "
35	A15	" "
36	A14	" "
37	A17	" "
38	A16	" "
39	/EXPINS	Expansion RAM Installed
41	/RD	Read Command
42	/CSEXP	Chip Select Expansion RAM
43	/EXPACK	Expansion RAM Acknowledge
44	/WR	Write Command
45	/EXPERR	Expansion RAM Parity Error
46	/BHE	Branch High Enable

MASTER BOARD

P6 -- RAM EXPANSION CONNECTOR

Pin	Signal	Purpose
47	+5 V	
48	+5 V	
49	Ground	
50	Ground	

EXPANSION RAM BOARD

Pin	Signal	Purpose
1	Ground	
2	Ground	
3	+5 V	
4	+5 V	
5	D1	Data Line
6	D0	" "
7	D3	" "
8	D2	" "
9	D5	" "
10	D4	" "
11	D7	" "
12	D6	" "
13	D9	" "
14	D8	" "
15	D11	" "
16	D10	" "
17	D13	" "
18	D12	" "
19	D15	" "
20	D14	" "
21	A1	Address Line
22	A0	" "
23	A3	" "
24	A2	" "
25	A5	" "
26	A4	" "
27	A7	" "
28	A6	" "
29	A9	" "

MASTER BOARD

EXPANSION RAM BOARD

Pin	Signal	Purpose
30	A8	Address Line
31	A11	" "
32	A10	" "
33	A13	" "
34	A12	" "
35	A15	" "
36	A14	" "
37	A17	" "
38	A16	" "
39	Ground	
41	/RD	Read Command
42	/CSEXP	Chip Select Expansion
43	/EXPACK	Expansion Board Acknowledge
44	/WR	Write Command
45	/EXPERR	Expansion RAM Error
46	/BHE	Branch High Enable
47	+5 V	
48	+5 V	
49	Ground	
50	Ground	

HARD DISK CONTROLLER

J1 -- CONTROLLER TO WINCHESTER DRIVE CONTROL INTERFACE

Pin	Signal Name
All Odd	Ground
2	/Reduced write current (ST506 Only)
4	/Head Select 2^2
6	/Write Gate
8	/Seek Complete
10	/Track 000
12	/Write Fault
14	/Head Select 2^0
16	Reserved
18	/Head Select 2^1
20	/Index
22	/Ready
24	/Step
26	/Drive Select 1
28	/Drive Select 2
30	/Drive Select 3
32	/Drive Select 4
34	/Direction In

J2 AND J3 -- CONTROLLER TO WINCHESTER DRIVE DATA INTERFACE

Pin	Signal Name
1	/Drive Selected
13	/+MFM Write Data
14	/-MFM Write Data
17	/+MFM Read Data
18	/-MFM Read Data
All Others	Ground

HARD DISK CONTROLLER

J6 -- CONTROLLER TO SCSI INTERFACE

Pin	Signal	Purpose
All Odd	Ground	
2	D0	Data Line
4	D1	" "
6	D2	" "
8	D3	" "
10	D4	" "
12	D5	" "
14	D6	" "
16	D7	" "
18	/PARITY	Parity Bit
36	/BSY	Hard Disk Busy
38	/ACK	Acknowledge
40	/RST	Reset
42	/MSG	Message -- Command completed
44	/SEL	Hard Disk Select
46	/CD	Command, message, or status (low); or data
48	/REQ	Request from Hard Disk
50	/IO	Input (low) or Output

J10 -- POWER CABLE CONNECTIONS

Pin	Signal
1	+12 V
2	Ground
3	Ground
4	+5 V

Table A-2. Expansion Box

MOTHER BOARD

P1, J1-J6 -- MULTIBUS SLOTS

Pin	Signal	Purpose
1	Ground	
2	Ground	
3	+5 V	
4	+5 V	
5	+5 V	
6	+5 V	
7	+12 V	
8	+12 V	
11	Ground	
12	Ground	
13	BCLK	Bus clock
14	/INIT	Initialize = system reset
15(P1)	/P1	Select P1
15(J1)	/J1	Select J1
15(J2)	/J2	Select J2
15(J3)	/J3	Select J3
15(J4)	/J4	Select J4
15(J5)	/J5	Select J5
15(J6)	/J6	Select J6
17	/BUSY	MULTIBUS not available
18(P1)	/P1	P1 select request
18(J1)	/J2	J1 select request
18(J2)	/J2	J2 select request
18(J3)	/J3	J3 select request
18(J4)	/J4	J4 select request
18(J5)	/J5	J5 select request
18(J6)	/J6	J6 select request
19	/MRDC	Memory read command
20	/MWTC	Memory write command
21	/IORC	I/O read command
22	/IOWC	I/O write command
23	/XACK	Transfer of data acknowledged
24	/INHI	Inhibit line (not used)
25	/LOCK	Locks out other bus masters
26	/INHL	Inhibit line (not used)
27	/BHEN	Bus high enable
28	/AD10	Address Line
29	/CBRQ	Common bus request
30	/AD11	Address Line
31	/CCLK	Inverted 8 MHz clock
32	/AD12	Address Line
33	/INTA	Interrupt acknowledge

MOTHER BOARD

Pin	Signal	Purpose
34	/AD13	Address Line
35	/INT6	Interrupt Line
36	/INT7	" "
37	/INT4	" "
38	/INT5	" "
39	/INT2	" "
40	/INT3	" "
41	/INT0	" "
42	/INT1	" "
43	/ADRE	Address Line
44	/ADRF	" "
45	/ADRC	" "
46	/ADRD	" "
47	/ADRA	" "
48	/ADRB	" "
49	/ADR8	" "
50	/ADR9	" "
51	/ADR6	" "
52	/ADR7	" "
53	/ADR4	" "
54	/ADR5	" "
55	/ADR2	" "
56	/ADR3	" "
57	/ADR0	" "
58	/ADR1	" "
60	/DATF	Data Line
61	/DATC	" "
62	/DATD	" "
63	/DATA	" "
64	/DATB	" "
65	/DAT8	" "
66	/DAT9	" "
67	/DAT6	" "
68	/DAT7	" "
69	/DAT4	" "
70	/DAT5	" "
71	/DAT2	" "
72	/DAT3	" "
73	/DAT0	" "
74	/DAT1	" "
75	Ground	
76	Ground	
79	-12 V	
80	-12 V	
81	+5 V	
82	+5 V	

MOTHER BOARD

Pin	Signal	Purpose
83	+5 V	
84	+5 V	
85	Ground	
86	Ground	

P2 AND P3 -- POWER SUPPLY

Pin	Signal
1	+5 V
2	Ground
3	Ground
4	Ground
5	+5 V
8	-12 V

P4 -- POWER SUPPLY

Pin	Signal
1	+5 V
2	Ground
3	Ground
4	Ground
5	+5 V

P5 AND P6 -- POWER SUPPLY

Pin	Signal
1	+5 V
2	Ground
3	Ground
4	Ground
5	+5 V
6	+12 V

Table A-3. Slave Board

MOTHER BOARD

P6 TO OPTIONAL RAM

Pin	Signal	Purpose
1	Ground	
2	Ground	
3	+5 V	
4	+5 V	
5	D1	Data Line
6	D0	" "
7	D3	" "
8	D2	" "
9	D5	" "
10	D4	" "
11	D7	" "
12	D6	" "
13	D9	" "
14	D8	" "
15	D11	" "
16	D10	" "
17	D13	" "
18	D12	" "
19	D15	" "
20	D14	" "
21	A1	Address Line
22	A0	" "
23	A3	" "
24	A2	" "
25	A5	" "
26	A4	" "
27	A7	" "
28	A6	" "
29	A9	" "
30	A8	" "
31	A11	" "
32	A10	" "
33	A13	" "
34	A12	" "
35	A15	" "
36	A14	" "
37	A17	" "
38	A16	" "
39	Ground	
41	/RD	Read Command
42	/CSEXP	Chip Select Expansion Ram

MOTHER BOARD

Pin	Signal	Purpose
43	/EXPACK	Expansion RAM Acknowledge
44	Not Used	
45	/EXPERR	Expansion RAM Parity Error
46	/BHE	Branch High Enable
47	+5 V	
48	+5 V	
49	Ground	
50	Ground	

MULTIBUS INTERFACE

Pin	Signal	Purpose
1	Ground	
2	Ground	
11	Ground	
12	Ground	
13	/BCLK	Bus clock
14	/INIT	Initialize = system reset
15	/BPRN	Bus priority in, signals MULTIBUS available
17	/BUSY	MULTIBUS is in use
18	/BREQ	MULTIBUS request
19	/MRDC	Memory read command
20	/MWTC	Memory write command
21	/IORC	I/O read command
22	/IOWC	I/O write command
23	/XACK	Transfer of data acknowledged
27	/BHEN	Bus high enable
28	/AD10	Address Line
29	/CBRQ	Common bus request
30	/AD11	Address Line
31	/CCLK	Inverted 8 MHz clock
32	/AD12	Address Line
34	/AD13	Address Line
37	/INT4	Interrupt Line
38	/INT5	" "
39	/INT2	" "
40	/INT3	" "
41	/INT0	" "
42	/INT1	" "
43	/ADRE	Address Line
44	/ADRF	" "
45	/ADRC	" "
46	/ADRD	" "

MULTIBUS INTERFACE

Pin	Signal	Purpose
47	/ADRA	Address Line
48	/ADRB	" "
49	/ADR8	" "
50	/ADR9	" "
51	/ADR6	" "
52	/ADR7	" "
53	/ADR4	" "
54	/ADR5	" "
55	/ADR2	" "
56	/ADR3	" "
57	/ADR0	" "
58	/ADR1	" "
59	/DATE	Data Line
60	/DATF	" "
61	/DATC	" "
62	/DATD	" "
63	/DATA	" "
64	/DATB	" "
65	/DAT8	" "
66	/DAT9	" "
67	/DAT6	" "
68	/DAT7	" "
69	/DAT4	" "
70	/DAT5	" "
71	/DAT2	" "
72	/DAT3	" "
73	/DAT0	" "
74	/DAT1	" "
75	Ground	
76	Ground	
79	Ground	
80	Ground	

DBS 16 HARDWARE DESCRIPTION AND MAINTENANCE MANUAL

APPENDIX B
PROGRAMMER'S HARDWARE REFERENCE

B.1 MASTER BOARD

The Master Board implements processing and peripheral control capability for up to four users of the DBS 16 System, as well as several system peripheral functions. The major hardware features include:

- 80186 CPU running at 8 MHz
- 256K bytes of dynamic RAM with parity checking
- 256K bytes of additional RAM optional via plug-in card
- 8K bytes of EPROM for Booting
- Four asynchronous serial I/O ports
- One synchronous/asynchronous serial I/O port
- One parallel printer interface port
- Control of up to two floppy disk drives
- Control of Winchester disk drive via an SCSI interface
- Two interrupt controllers
- MULTIBUS interface to expansion chassis

Address Summary

LMCS = Lower Memory Chip Select
UMCS = Upper Memory Chip Select
MMCS = Middle Memory Chip Select
PCS = Peripheral Chip Select

LMCS	Dynamic RAM		00000 - 3FFFF
MMCS	Dynamic RAM		40000 - 7FFFF (optional)
	MULTIBUS Shared RAM Mailbox		80000 - FD000 jumper-selectable on Mother Board -- normally set for BF000 - BFFFF
UMCS	Boot PROM		FE000 - FFFFF
PCS0	SIO #1	00 - 0C even	INT 2
	SIO #2	10 - 1C even	INT 3
	SIO #3	20 - 2C even	INT 4
	SIO #4	30 - 3C even	INT 5
	FDC	40 - 46 even	INT 13 DRQ0
	PPI	50 - 56 even	INT 12
	S/A I/O	60 - 62 even	INT 2 (Rx) INT 6 (Tx)
	BRG	70	Baud Rate Generator
PCS2	PIC #1	100 - 102 even	Programmable Interrupt Controller
PCS3	PIC #2	180 - 182 even	Programmable Interrupt Controller
PCS4	SCSI	200 - 201	INT 14 DRQ0

B.1.1 Memory

The Boot PROM resides at the top of physical memory. It occupies addresses FE000 through FFFFF (8K bytes using two 4K x 8 2732 EPROMs). The shared memory Mailbox RAM is located on the backplane card, and is electrically connected to the MULTIBUS. This RAM occupies addresses BF000 through FFFFF (using two 2K x 8 static RAMs). This is jumper-selectable on the Mother Board.

The working RAM for the Master Board CPU is 256K bytes of dynamic RAM, consisting of thirty-six 64K bit RAMs, including parity checking circuitry, located at addresses 00000 through 3FFFF. This RAM is controlled by a dynamic RAM controller chip which allows operation with two wait states. An optional expansion capability adds another 256K bytes of RAM, located at addresses 40000 through 7FFFF.

The memory locations not on this board (i.e., 80000 through FDFFF) are accessible via the MULTIBUS.

Parity errors in main memory or expansion memory generate interrupt INT0. This interrupt can only be cleared by a hard reset (not by software).

NOTE: The presence or absence of an Expansion RAM card can be determined by reading port 3C. Bit D6 will be true if the Expansion card is installed. This port is the Modem Status port for SIO #4.

B.1.2 Peripherals

The following peripheral control chips are included on the Master Board:

- Four 8250 Async Serial I/O ports for connecting user terminals
- One 8251A Sync/async Serial I/O port for use with a serial printer or for host communication (i.e., 2780, 3270, and others)
- Baud Rate Generator for 8251A
- Two 8259A Interrupt Controllers
- One 8255A Parallel Interface for parallel printer, floppy disk drive and side select, and configuration switch
- One 1793 Floppy Disk Controller
- SCSI interface to Winchester disk controller

You will find in this appendix detailed address and interface information for these peripheral controllers, as well as detailed setup information regarding the internal memory and peripheral control registers on the 80186 CPU.

B.1.3 Asynchronous Serial I/O Ports -- 8250

The 8250 Asynchronous Communication Controller performs serial/parallel and parallel/serial conversion on data received and transmitted by the terminal. It includes an internal baud rate generator driven at 2 MHz, modem control and status interface, and interrupt-control logic, which allows interrupts to be generated to the CPU on several conditions.

Peripheral Chip Select 0 (PCS0) selects the 8250s. The interrupts are set up as follows:

8250 #1	00 - 0C even	connected	to	Interrupt	INT 2
8250 #2	10 - 1C even	"	"	"	INT 3
8250 #3	20 - 2C even	"	"	"	INT 4
8250 #4	30 - 3C even	"	"	"	INT 5

The 8250 contains 10 CPU-accessible registers. Two pairs of registers share the same address; which register is accessed depends on the setting of the DLAB bit in the Line Control Register. The registers and addresses are as follows:

X0	R	Receive Buffer Register	(DLAB = 0)
		Divisor Latch LS byte (divisor bits 0-7)	(DLAB = 1)
	W	Transmit Buffer Register	(DLAB = 0)
		Divisor Latch LS byte (divisor bits 0-7)	(DLAB = 1)
X2	R/W	Interrupt Enable Register	(DLAB = 0)
		Divisor Latch MS byte (divisor bits 8-15)	(DLAB = 1)
X4	R	Interrupt ID Register	
X6	R/W	Line Control Register	(Word length, parity, etc.)
X8	R/W	Modem Control Register	(DTR RTS Loop, 2 other outputs)
XA	R	Line Status Register	(RxRdy TxRdy PE FE OE Break)
XC	R	Modem Status Register	(CTS RI DSR, etc.)

The bits in each register are as follows:

X0 R (DLAB = 0) RECEIVE BUFFER REGISTER
Contains the last received character.

X0 W (DLAB = 0) TRANSMIT BUFFER REGISTER
Characters to be transmitted are written to this register.

X2 R/W (DLAB = 0) INTERRUPT ENABLE REGISTER
(all bits = 0, following reset)

D0	ERBFI	Enable Receive Data Available Interrupt
D1	ETBEI	Enable Transmit Buffer Empty Interrupt
D2	ELSI	Enable Line Status Interrupt
D3	EDSSI	Enable Modem Status Interrupt

D4-D7 = 0

X4 R INTERRUPT ID REGISTER

Contains identification of interrupt.

D0 = 0 if interrupt pending (set to 1 after reset)
D1,D2 Interrupt ID (set to 00 after reset)
D3-D7 = 0

D2	D1	Source
0	0	Modem status (Lowest priority)
0	1	Xmit buffer empty
1	0	Received character available
1	1	Break or PE or FE or OE (Highest priority)

X6 R/W LINE CONTROL REGISTER (set to all 0's after reset)

Controls the bit format of received and transmitted data.

D0	WLS0	Word Length Select LSB 00,01,10,11 = 5,6,7,8 bits
D1	WLS1	Word Length Select MSB
D2	STB	Number of stop bits 0 = 1 stop bit, 1 = 2 stop bits
D3	PEN	Parity Enable
D4	EPS	Even Parity Select
D5		Stick Parity
D6		Set Break
D7	DLAB	Divisor Latch Access bit 0 = access Rx Tx data register, 1 = access divisor latch register

X8 R/W MODEM CONTROL REGISTER (set to all 0's after reset)

Controls the Modem control lines.

D0 DTR Data Terminal Ready
D1 RTS Request to Send
D2 Spare Output 1
D3 Spare Output 2
D4 Loopback
D5-D7 = 000

XA R LINE STATUS REGISTER (set to 0's after reset except D5,6 which is set to 11)

Contains the receiver status.

D0	DR	Data Ready in receiver
D1	OR	Overrun Error on receive
D2	PE	Parity Error
D3	FE	Framing Error
D4	BI	Break Interrupt (set if Rx is spacing for greater than one character time)
D5	THRE	Transmit Holding Register Empty
D6	TSRE	Transmit Shift Register Empty
D7	= 0	

XC R MODEM STATUS REGISTER (D0-D3 set to 0 after reset)

Contains the status of the modem.

D0	DCTS	Delta Clear to Send (CTS has changed)
D1	DDSR	Delta Data Set Ready (DSR has changed)
D2	TERI	Trailing Edge Ring Indicator (RI has turned off)
D3	DRLSD	Delta Carrier Detect (RLSD has changed)
D4	CTS	
D5	DSR	
D6	RI	
D7	RLSD	(Carrier Detect)

X0 R,W (DLAB = 1) BAUD RATE DIVISOR LATCH LS byte
X2 R,W (DLAB = 1) BAUD RATE DIVISOR LATCH MS byte

The Baud Rate Divisor Latch must be loaded by the CPU with a binary number which, when used to divide the input frequency, provides an output which is 16 times the desired baud rate. The Baud Rate Divisor Latch is accessed by setting the DLAB bit to 1. The input frequency is 2 MHz.

B.1.4 Floppy Disk Controller -- 1793

The 1793 Floppy Disk Controller handles the interface between the floppy disks and the system CPU/memory. It performs seek operations, controls loading of the R/W heads, and handles the serial/parallel and parallel/serial conversion of data from/to the disks/memory, including recognition of address marks. It also performs disk formatting.

Data is transferred to/from memory via the DMA controller, which handles memory addressing and generates the R/W strobes. It uses even port addressing. The CPU controls the FDC via five internal registers, while the FDC can notify the CPU of completion of a command via an interrupt.

In the following list, IOA = I/O Address.

PCS0	Command/Status	IOA = 40
	Track	IOA = 42
	Sector	IOA = 44
	Data	IOA = 46

DRQ is connected to DMA request channel 0 (OR-ed with SCSI); INT is connected to interrupt INT 13.

The FDC contains five internal registers which can be read/written to by the CPU. The register names, functions and addresses are:

X0	W	Command	CPU writes command words
X0	R	Status	CPU reads status
X2	R/W	Track	Maintains current track number
X4	R/W	Sector	Holds desired sector number
X6	R/W	Data	Used for data transfers, and track number for seeks

The 1793 recognizes four types of commands: I, II, III, and IV. A Type I command moves the head. A Type II command reads and writes variable data. A Type III command reads or writes an entire track. A Type IV command terminates an operation in process and generates an interrupt.

The following table summarizes the available commands.

Table B-1. 1793-Recognizable Commands

TYPE	COMMAND	7 6 5 4 3 2 1 0	
I	Restore	0 0 0 0 h V r1 r0	0C for 6 ms step
I	Seek	0 0 0 1 h V r1 r0	1C for 6 ms step track number in data register
I	Step	0 0 1 u h V r1 r0	3C for 6 ms step with track update
I	Step In	0 1 0 u h V r1 r0	5C for 6 ms step with track update
I	Step Out	0 1 1 u h V r1 r0	7C for 6 ms step with track update
II	Read	1 0 0 m X E 0 0	84/94 single/multiple sectors (sector number in sector register)
II	Write	1 0 1 m X E X a0	A4/B4 single/multiple sectors
II	Read Address	1 1 0 0 0 1 0 0	C4
III	Read Track	1 1 1 0 0 1 0 X	E4
III	Write Track	1 1 1 1 0 1 0 0	F4
IV	Force Int.	1 1 0 1 I3 I2 I1 I0	D8 Immediate Interrupt

NOTE: In the table, X = Don't Care

Type I Commands

h = 1 Load head at beginning
h = 0 Unload head at beginning

V = 1 Verify on last track
V = 0 No verify

u = 1 Update track register
u = 0 No update

Stepping Rates

r1	r0	
0	0	6 ms
0	1	12 ms
1	0	20 ms
1	1	30 ms

Type II Commands

m = 0 Single sector
m = 1 Multiple sectors

a0 = 0 Address mark = FB (data mark)
a0 = 1 Address mark = F8 (deleted data)

E = 1 Wait 15 ms after head load
E = 0 Wait 0 ms after head load

Type IV Commands

I0 = 1 Not-ready to ready
I1 = 1 Ready to not-ready
I2 = 1 Index Pulse
I3 = 1 Immediate Interrupt

NOTE: With I0, I1, I2, and I3 all set to 0, no interrupt is generated, but the current operation is terminated.

B.1.4.1 Status

The form of the status word varies depending on the type of the last command issued. The status words are as follows:

Type I Commands	Type II & III Commands
D0 Busy	D0 Busy
D1 Index	D1 Data Request
D2 Track 00	D2 Lost Data
D3 CRC Error	D3 CRC Error
D4 Seek Error	D4 Record not Found
D5 Head Loaded	D5 Wrong Record Type in data address mark
D6 Write Protect	D6 Write Protect (write command only)
D7 Drive Not Ready	D7 Drive Not Ready

B.1.5 Parallel Peripheral Interface -- 8255A

PSC0 Configuration Switch Port IOA = 50 - read-only

D0-D6 = 0 functions to be determined
D7 = 0 boot from floppy
= 1 boot from hard disk

Printer Data Port IOA = 52 - read/write
8 bits

Printer Status Port IOA = 54 - read-only

D0 Printer Ready (= Interrupt)
D1 OBF - low true
D2 ACK - low true pulse
D3 Printer Fault - low true

D2 INTE (write - 0 = disable 1 = enable)

Printer Interrupt connected to INT 12

Floppy Disk Select Port IOA = 54 - read/write

(must use bit set/reset commands to write -- refer to Bit Set/Reset Commands in the following)

D4 Drive Select (0 = drv 0 1 = drv 1)
D5 No Connection
D6 Side Select (0 = normal 1 = back side)
D7 Ext Clock Select - 8251 (0 = internal 1 = external)

Configuration control port IOA = 56

(MUST be set to 95H following reset, then SHOULD be set to 05 to enable printer INT)

Bit Set/Reset Commands are written to port 56, and are in the following form:

0000BBBD where BBB is bit number to set
D is 1 or 0 to set the bit

B.1.6 Synchronous/Asynchronous Serial I/O -- 8251A

PCS0 Data Port Read Serial Received Data IOA = 60
Write Serial Transmit Data

Command/Status Port Read Status IOA = 62

D0	TxRdy	Transmitter Ready for next character
D1	RxRdy	Receiver has next character available
D2	TxE	Transmitter Empty
D3	PE	Parity Error
D4	OE	Overrun Error
D5	FE	Framing Error
D6	SYNDET	Sync Detect (sync mode only)
D7	DSR	Data Set Ready

RxRdy connected to INT 1
TxRdy connected to INT 6
Clock Select - refer to PCS0 Parallel Peripheral Interface in preceding text

NOTE: Carrier Detect from the Sync/Async port is connected to SIO #4, Modem status register, port 3C, bit D7.

Control Port Write Mode and Command words

The Mode word is the first word written to this port following a hard or soft reset.

Mode Format - Asynchronous Mode

D0 Baud rate factor (LSB)	00 = Sync Mode	01 = 1x
	10 = 16x	11 = 64x
D1 Baud rate factor (MSB)		
D2 Character Length (LSB)	00 = 5 bits	01 = 6 bits
	10 = 7 bits	11 = 8 bits
D3 Character Length (MSB)		
D4 Parity Enable	Enable = 1	Disable = 0
D5 Type Parity	Even = 1	Odd = 0
D6 Number of Stop Bits (LSB)	00 = invalid	01 = 1 stop bit
	10 = 1-1/2	11 = 2 bits
D7 Number of Stop Bits (MSB)		

Mode Format - Synchronous Mode

D0 = 0	
D1 = 0	
D2 Character Length (LSB)	(same as preceding)
D3 Character Length (MSB)	
D4 Parity Enable	Enable = 1 Disable = 0
D5 Type Parity	Even = 1 Odd = 0
D6 External Sync Detect	1 = SYNDET is input
	0 = output Set to 0

D7 Sync 0 = double character sync 1 = single char sync

The Command word can be written any time after a Mode word is written.

Command Word Format

D0	TxEn	Transmit Enable
D1	DTR	Data Terminal Ready
D2	RxEn	Receive Enable
D3	SBRK	Send Break - Sets TxData line low
D4	ER	Error Status Reset
D5	RTS	Request to Send
D6	IR	8251 Reset
D7	EH	Enter Hunt Mode (search for Sync)

NOTE: The 8251 should be programmed for 16x clocks when using asynchronous mode.

Baud Rate Generator -- 8116

PCS0 Data Port IOA = 70

D0(LSB) - D3(MSB) Receive Baud Rate
D4(LSB) - D7(MSB) Transmit Baud Rate

Baud Rate	Hex Value	Baud Rate	Hex Value
50	0	1800	8
75	1	2000	9
110	2	2400	A
134.5	3	3600	B
150	4	4800	C
300	5	7200	D
600	6	9600	E
1200	7	19,200	F

B.1.7 Programmable Interrupt Controllers -- 8259A

PCS2 8259A #1 100 - 102 even connected to INT0/INTA0
PCS3 8259A #2 180 - 182 even connected to INT1/INTA1

INT0 - highest priority on PIC #1
INT7 - lowest priority on PIC #1
INT8 - highest priority on PIC #2
INT15 - lowest priority on PIC #2

Interrupts (total 16):

INT0 RAM Parity Error
INT1 8251A Rx
INT2 8250 #1
INT3 8250 #2
INT4 8250 #3
INT5 8250 #4
INT6 8251A Tx
INT7 Bus Int #0
INT8 Bus Int #1
INT9 Bus Int #2
INT10 Bus Int #3
INT11 Bus Int #4
INT12 8255 (Printer)
INT13 1793
INT14 SCSI
INT15 Bus Int #5

B.1.8 SCSI Interfacing

SCSI Interface for Winchester Disk Drive:

PCS4 Data Port IOA = 200 read/write
Control/Status Port IOA = 201

These ports may be accessed as bytes or words:

RFS connected to Interrupt INT 14
DRQ connected to DMA request channel 0 (OR-ed with floppy)

SCSI - Hard Disk Controller Interface

Data Port - Read/Write 8 bits

Status Port 8 bits NOTE: All status bits are LOW true

D0	RFDO	Ready for Data Out to controller
D1	RFDI	Ready for Data In from controller
D2	BUSY	Controller is BUSY
D3	RFC	Ready for Command out to controller
D4	RFS	Ready for Status in from controller - connected to Interrupt
D5	RFM	Ready for Message in from controller
D6	DRQ	DMA Request - connected to DMA channel
D7	always 0	

Control Port 8 bits

D0	SEL	Selects controller designated by bit on data port
D1		Reset controller
D2-D7		Not Connected

The RFS (Ready for Status) bit in the interface will generate an interrupt.

DMA Request is generated by RFDI or RFDO.

The data port is connected to the LS byte of the CPU Data Bus; the Control/Status port is connected to the MS byte of the Data Bus. Both ports can be accessed as bytes or words.

B.1.9 80186 Internal Register Setup

B.1.9.1 Relocation Register at FFFE

This register controls the location of the Peripheral Control Block (PCB). The value should not be changed from the default, which is 20FF. This setting puts the PCB at FF00 in I/O space, sets normal Interrupt mode, and disables ESC Traps. The only bit which might be changed is the ESC trap bit.

B.1.9.2 Upper Memory Chip Select UMCS at FFA0 = FE3B

This register selects the amount of address space assigned to Upper Memory. UMCS is connected to the Boot PROM. The default value sets the Upper Memory for a 1K byte block, located at FFC00 through FFFFF, with three wait states, and external Ready used. This register must be changed to FE3B before PROM below address FFC00 is accessed. This sets Upper Memory for 8K bytes, with 3 wait states and external Ready used.

B.1.9.3 Lower Memory Chip Select LMCS at FFA2 = 3FFA

This register selects the address space assigned to Lower Memory, the built-in working RAM for this processor. This memory space consists of 256K bytes of dynamic RAM, starting at address 0, and requires two wait states for operation. This register must be programmed to 3FFA before this memory space is accessed.

B.1.9.4 Mid Memory Chip Select MMCS at FFA6 = 41FA

This register selects the base address assigned to the expansion memory for this processor. This memory space consists of 256K bytes of dynamic RAM with characteristics identical to those for Lower Memory, with addresses from 40000 through 7FFFF. This register must be programmed to 41FA before this memory space is accessed.

B.1.9.5 Peripheral Chip Select PACS at FFA4 = 003E

This register controls the chip select logic for PCS0-PCS3. It must be set up before these I/O devices are used. The register should be set to 003E. This sets the Programmable Base Address (PBA) of the peripheral chip select block to 0000, with two wait states and external Ready ignored.

B.1.9.6 Memory and Peripheral Chip Select MPCS at FFA8 = A0BC

This register controls the size of the mid-range memory block, which is used to select the expansion memory. It also controls the wait states for PCS4 to PCS6. This register should be set to A0BC before any peripherals or the expansion memory are accessed. This selects the peripherals to be in I/O address space, and PCS5 and PCS6 to be active, with 0 wait states for peripherals PCS4-PCS6.

B.2 SLAVE CARD

The DBSI Slave Card implements processing capability for up to four user terminals in the DBS 16 System. The major functional features of this board include:

- 80186 CPU running at 8 MHz
- 256K bytes of dynamic RAM with parity checking
- 256K bytes of additional RAM optional
- 8K bytes of EPROM for boot and test programs
- Two 2681 dual UARTs for user terminal interfaces
- Interface to the system MULTIBUS for communication with other processors in the DBS 16 System

This appendix defines the address ports and bits necessary for the system programmer to design and write the operating software for the system.

Address Summary

LMCS	Dynamic RAM	00000 - 3FFFF	
MMCS	Dynamic RAM	40000 - 7FFFF (optional)	
	MULTIBUS Memory	80000 - BFFFF	
UMCS	Boot ROM	FE000 - FFFFF	
PCS0	DUART #1	0000 - 001F even I/O addresses only	INT1
PCS1	DUART #2	0080 - 009F " " " "	INT2
PCS4	Board ID/Master Intpt	I/O 0200	
	MULTIBUS I/O	8000 - BFFF	

B.2.1 Interrupts

Memory Parity Errors generate INT0.

DUART 1 generates INT1. DUART 2 generates INT2.

Any device on the MULTIBUS can generate INT3 (see Master/Slave interrupts).

Slave Card generates one bus interrupt to signal Master.

NMI is not used.

DMA and Timers:

Both DMA channels and all Timers are available for system use. None have any dedicated hardware function.

B.2.2 Memory

The Boot PROM resides at the top of physical memory. It occupies addresses FE000 through FFFFF (8K bytes using two 4K x 8 2732 EPROMs). The boot PROM is always enabled.

The working RAM for the Slave CPU consists of 256K bytes of dynamic RAM, located at addresses 00000 through 3FFFF. Working RAM may be expanded by an additional (optional) 256K bytes located at addresses 40000 through 7FFFF, using a plug-in card. Operation of this RAM depends on the setup of several registers in the 80186, which must be set up before this RAM is accessed. These setup conditions are detailed further on in this appendix.

The Mailbox RAM resides on the system MULTIBUS board, and is accessible from the Master and all Slave cards via the MULTIBUS. The address of this RAM is selectable by jumpers on the MULTIBUS board, and is normally set to BF000 through BFFFF.

B.2.3 Peripherals

The peripheral chips on this board are two 2681 dual UARTs, each of which can be connected to two user terminals. Additionally, there is a switch, readable by the CPU, used for setting a board address; also, there is hardware to allow the Slave CPU to generate an interrupt to the Master CPU, and to allow the Master to interrupt the Slave.

The rest of this appendix details the aforementioned hardware, to allow the system programmer to implement the system software.

B.2.4 Asynchronous Serial I/O Ports -- 2681-24

PCS0	DUART #1	0000 - 001F even	connected to INT1
PCS1	DUART #2	0080 - 009F even	" " INT2

2681-24 Dual UART (even port numbers)

The internal baud rate generators are driven at 3.6864 MHz.

The 2681-24 is a Dual Universal Asynchronous Receiver/Transmitter (DUART) in a 24-pin DIP package. It fully implements two channels of communications, including baud rate generators, but without modem controls. This paragraph describes the way it is connected in the DBSI Slave Board.

NOTE: Port numbers assume the first port is at address 00. Add the base address to the value shown for the actual address.

SLAVE CARD (cont'd)

Port 00	R/W	A Mode (MR1A,MR2A)
" 02	R	A Status (SRA)
	W	A Clock Select (CSRA)
Port 04	R	RESERVED - Do not access
	W	A Command (CRA)
Port 06	R	A Rx Holding Reg (RHRA) - Received Data A
	W	A Tx Holding Reg (THRA) - Transmit Data A
Port 08	R	(Input Port Change Reg (IPCR) - N.C.)
	W	Aux Control Reg (ACR)
Port 0A	R	Interrupt Status (ISR)
	W	Interrupt Mask (IMR)
Port 0C	R/W	Counter/Timer Upper (CTU)
" 0E	R/W	Counter/Timer Lower (CTL)
" 10	R/W	B Mode (MR1B,MR2B)
" 12	R	B Status (SRB)
	W	B Clock Select (CSRB)
Port 14	R	RESERVED - Do not access
	W	B Command (CRB)
Port 16	R	B Rx Holding Reg (RHRB) - Received Data B
	W	B Tx Holding Reg (THRB) - Transmit Data B
Port 18	R/W	RESERVED - Do not access
" 1A	R	(Input Port - N.C.)
	W	(Output Port Configuration (OPCR) - N.C.)
Port 1C	R	Start Counter Command
	W	(Set Output Port Bits Command - N.C.)
Port 1E	R	Stop Counter Command
	W	(Reset Output Port Bits Command - N.C.)

The following information summarizes the bit functions in the various registers. Refer to the "Signetics SCN2681 Data Sheet" for detailed information on the operation of this chip.

00 A Mode Register (MR1A,MR2A) Read/Write
10 B Mode Register (MR1B,MR2B) Read/Write

The mode register consists of two registers, both accessed via the same port number. MR1A/MR2A are selected following RESET, or by a set pointer command via the command register (CRA/CRB). After this register is accessed, MR2A/MR2B are selected.

MR1A/MR1B

D1,0	bits per char 00 = 5 01 = 6 10 = 7 11 = 8
D2	parity 0 = even 1 = odd
D4,3	parity 00 = with parity 01 = force parity 10 = no parity 11 = multidrop mode(NA)
D5	error mode 0 = each character in FIFO has own error bits 1 = error bits are OR of all characters in FIFO
D6	Rx Interrupt Select 0 = RxRdy 1 = FIFO full
D7	Rx RTS control - set to 0

MR2A/MR2B

D3,2, 1,0	Stop bit length	0111 = 1.0 1111 = 2.0 (add 0.5 for 5 bits/char); other values available
D4	CTS enable Tx -	set to 0
D5	TX RTS control -	set to 0
D7,6	Mode	00 = normal 01 = auto echo 10 = local loop 11 = remote loop

02 A Status (SRA) Read Only
12 B Status (SRB) Read Only

D0	RxRdy
D1	FIFO Full
D2	TxRdy
D3	Tx Empty
D4	Overrun Error
D5	Parity Error
D6	Framing Error
D7	Received Break

NOTE: D5,6,7 bits in character error mode follow the characters through the FIFO. In block error mode, these bits are set by the given error on any character since the last "Reset Error Status" command.

02 A Clock Select (CSRA) Write Only
12 B Clock Select (CSRB) Write Only

D3,2, 1,0	Tx Clock Select
D7,6, 5,4	Rx Clock Select

Auxiliary Control Register

bit D7 = 0

Word	Baud	Word	Baud
0000	50	1000	2400
0001	110	1001	4800
0010	134.5	1010	7200
0011	200	1011	9600
0100	300	1100	38,400
0101	600	1101	timer
0110	1200	1110	NA
0111	1050	1111	NA

bit D7 = 1

Word	Baud	Word	Baud
0000	75	1000	2400
0001	110	1001	4800
0010	134.5	1010	1800
0011	150	1011	9600
0100	300	1100	19,200
0101	600	1101	timer
0110	1200	1110	NA
0111	2000	1111	NA

NOTE: When using timer, the actual baud rate is timer output divided by 16.

04 A Command Register (CRA) Write Only
14 B Command Register (CRB) Write Only

D0	Enable Receive	0 = no 1 = yes
D1	Disable Receive	0 = no 1 = yes
D2	Enable Transmit	0 = no 1 = yes
D3	Disable Transmit	0 = no 1 = yes
D6,5,4	Miscellaneous Commands -- details follow	
D7	must be 0	

Commands		
	000	None
	001	Reset MR pointer - points to MR1
	010	Reset receiver - disable Rx and clear FIFO
	011	Reset transmitter
	100	Reset error status
	101	Reset ch A break change interrupt
	110	Start break (Tx)
	111	Stop break (Tx)

06 A Receive Holding Register (RHRA) Read Only
16 B Receive Holding Register (RHRB) Read Only
D0-D7 Receive Data

06 A Transmit Holding Register (THRA) Write Only
16 B Transmit Holding Register (THRB) Write Only
D0-D7 Transmit Data

08 Input Port Change Register (IPCR) Read Only
Because there is no input port on the 24-pin part, this register is useless.

08 Auxiliary Control Register (ACR) Write Only

D3,2, 1,0	Input pin delta - N.C.
D6,5, 4	Counter/timer mode - refer to following list
D7	Baud Rate Generator Select (refer to preceding text)

Counter/Timer Mode D6,5,4

000	Do not use (counter external input)
001	Counter - TXCA - 1X clock from A Tx
010	Counter - TXCB - 1X clock from B Tx
011	Counter - crystal oscillator / 16
100	Do not use (timer external input)
101	Do not use (timer external input / 16)
110	Timer - crystal oscillator
111	Timer - crystal oscillator / 16

Interrupt Status (ISR) Read Only

D0	TxRdy A
D1	RxRdy/FIFO Full A *
D2	Delta Break A
D3	Counter Ready
D4	TxRdy B
D5	RxRdy/FIFO Full B *
D6	Delta Break B
D7	0 (In/Out port change)

(* Selected by mode register)

0A Interrupt Mask (IMR) Write Only
Refer to ISR. 0 = disable 1 = enable interrupt

0C Counter/Timer Upper (CTU) Read/Write
Most significant byte of the counter/timer register

0E Counter/Timer Lower (CTL) Read/Write
Least significant byte of the counter/timer register

1A Input Port - Read Only
There is no input port so this register is useless.

1A Output Port Configuration (OPCR) Write Only
There is no output port so this register is useless.

1C Start Counter Command - Read Only
Reading from this port will start (enable) the counter/timer.

1C Set Output Port Bits Command - Write Only
There is no output port so this register is useless.

1E Stop Counter Command - Read Only
Reading from this port will stop (disable) the counter/timer.

1E Reset Output Port Bits Command - Write Only
There is no output port so this register is useless.

04,14,18 Reserved
DO NOT ACCESS THESE PORTS. These ports are RESERVED internal to the chip. Any access to these ports may cause unspecified and undesirable events.

B.2.5 Master/Slave Interrupts and Identity

The Slave Board has several switches which are set to identify a particular Slave Card in the system. These switches are also connected into the Master/Slave interrupt structure. The functions of these switches are described in this paragraph.

There are six switches related to Slave ID. These switches can be read by an input from I/O port 0200. All but one switch on a given Slave Card will normally be ON. An ON switch reads as logic '0', while an OFF switch reads as logic '1'. The six possible values which might be read from port 0200 are therefore:

Slave ID	S1	S2	S3	S4	S5	S6	BUS INT	READ ID	INT ADDR
1	OFF	ON	ON	ON	ON	ON	0	41	BFFC
2	ON	OFF	ON	ON	ON	ON	1	21	BFFA
3	ON	ON	OFF	ON	ON	ON	2	11	BFF6
4	ON	ON	ON	OFF	ON	ON	3	09	BFEE
5	ON	ON	ON	ON	OFF	ON	4	05	BFDE
6	ON	ON	ON	ON	ON	OFF	5	03	BFDE

The MULTIBUS architecture defines 8 bussed interrupt lines. Six of these lines are connected to generate interrupts on the Master Board in the DBS 16 System. Each Slave is configured by the preceding jumpers to generate one of these six interrupts, as shown previously. Any output from the Slave to I/O Port 0200 with DO = 1/0 generates/clears the selected interrupt to the Master.

The DBS 16 System also defines a method by which the Master can interrupt each Slave Card. The actual implementation of this feature allows any device on the MULTIBUS to generate these interrupts. This feature is implemented via a flip-flop on each Slave Card which can be set or cleared by any device on the MULTIBUS. Setting the flop (writing DO to '1') generates INT3 on the Slave Card; clearing the flop (writing DO to '0') clears the interrupt. All Slave interrupt flops are cleared to '0' by power-up or hard reset. The bus I/O addresses for accessing the flops on the various Slave Cards are listed in the preceding table.

B.2.6 80186 Internal Register Setup

B.2.6.1 Relocation Register at FFFE

This register controls the location of the Peripheral Control Block (PCB). The value should not be changed from the default (20FF). This setting puts the PCB at FF00 in I/O space, sets normal Interrupt mode, and disables ESC Traps. The only bit which might be changed is the ESC trap bit.

B.2.6.2 Upper Memory Chip Select UMCS at FFA0 = FE3B

This register selects the amount of address space assigned to Upper Memory. UMCS is connected to the Boot PROM. The default value sets the Upper Memory for a 1K byte block, located at FFC00 through FFFFF, with three wait states, and external Ready used. This register must be changed to FE3B before PROM below address FFC00 is accessed. This sets Upper Memory for 8K bytes, with three wait states and external Ready used.

B.2.6.3 Lower Memory Chip Select LMCS at FFA2 = 3FFA

This register selects the address space assigned to Lower Memory, the built-in working RAM for this processor. This memory space consists of 256K bytes of dynamic RAM, starting at address 0, and requires two wait states for operation. This register must be programmed to 3FFA before this memory space is accessed.

B.2.6.4 Mid Memory Chip Select MMCS at FFA6 = 41FA

This register selects the base address assigned to the expansion memory for this processor. This memory space consists of 256K bytes of dynamic RAM with characteristics identical to those for Lower Memory, with addresses from 40000 through 7FFFF. This register must be programmed to 41FA before this memory space is accessed.

B.2.6.5 Peripheral Chip Select PACS at FFA4 = 003E

This register controls the chip select logic for PCS0-PCS3. It must be set up before these I/O devices are used. The register should be set to 003E. This sets the Programmable Base Address (PBA) of the peripheral chip select block to 0000, with two wait states and external Ready ignored.

B.2.6.6 Memory and Peripheral Chip Select MPCS at FFA8 = A0BC

This register controls the size of the mid-range memory block, which is used to select the expansion memory. It also controls the wait states for PCS4 through PCS6. This register should be set to A0BC before the expansion memory or peripherals are accessed. This selects the peripherals to be in I/O address space, and PCS5 and PCS6 to be active, with 0 wait states for peripherals PCS4-PCS6.

B.3 MULTIBUS USAGE

This paragraph describes the usage of the MULTIBUS in the DBS 16 System, concentrating on the specific implementation characteristics. It is assumed that the reader is familiar with the MULTIBUS specification, and the general characteristics of that bus standard.

The Expansion Box contains six slots for MULTIBUS cards, a Power Supply, and a connection to the Master Board in the Desktop Unit. The Expansion Box card cage Mother Board contains logic for parallel priority resolution. Signals defined in the MULTIBUS specification for serial priority resolution are not implemented in the Mother Board.

Both BCLK and CCLK are driven by the Master Board at 8 MHz.

B.3.1 Bus Master Priority and Interrupts

In this system, there are seven possible bus masters: the Master Board in the Desktop Unit, and up to six cards in the card cage. The parallel priority resolution circuitry on the Mother Board prioritizes the bus requests from these seven devices, and issues a bus acknowledge to the highest priority requestor. The Master Board in the Desktop Unit has the highest bus priority, followed by the slots in the Expansion Box, from top (second highest) to bottom (lowest priority).

The MULTIBUS specification defines eight bus interrupts, which occupy eight lines in the bus. In this system, six of these lines are implemented, and all are connected to generate interrupts to the processor on the Master Board. These interrupts are implemented as "Non Bus Vectored" interrupts. The two unused interrupt lines are bussed to all connectors, but are not connected on either the Master Board or the Slave Cards.

B.3.2 Bus Addressing: Memory

The processor on the Master Board in the Desktop Unit addresses onboard RAM in the range of 00000 through 7FFFF (hex), and onboard PROM from FE000 through FFFFF. Addresses in the range of 80000 through FDFFF (hex) attempt to access locations on the MULTIBUS.

The Slave Card processors address onboard RAM at 00000 through 7FFFF, and PROM at FE000 through FFFFF. Addresses in the range of 80000 through BFFFF (hex) access locations on the MULTIBUS. Addresses in the range of C0000 through FDFFF access non-existent memory.

The Mother Board contains circuitry implementing 4K bytes of static RAM. This RAM is used as a system mailbox in systems utilizing DBSI Slave Cards. This RAM is accessible to all processor cards on the bus. This RAM occupies 4K byte locations in the MULTIBUS address space, somewhere in the range of 80000 (hex) to BFFFF (hex).

The specific address location is determined by a set of switches on the Mother Board. In systems running MP/M-86, this RAM normally resides at addresses BF000 through BFFFF (hex).

The MULTIBUS memory address range within which this memory will respond is determined as follows. Switch 1 is used to enable (switch ON) or disable (switch OFF) the shared RAM. Switches 2 through 9 are used to determine the most significant eight bits of the address range to which the memory will respond, if enabled.

A given switch, when ON, sets its corresponding address bit to logic ONE (1), and when OFF, sets its corresponding address bit to logic ZERO (0). Switch 2 controls the least significant bit of the address range, and switch 9 sets the most significant bit of the address range. Therefore, the address range to which the shared memory will respond is determined as follows:

S9 S8 S7 S6 S5 S4 S3 S2 XXXX XXXX XXXX

With switch 1 ON, and all others OFF, the address range would read:

0 0 0 0 0 0 0 0 XXXX XXXX XXXX

The memory would respond to an address in the range of 00000 through 00FFF (hex). Note that no processor in the system can generate a bus address in this range.

To set the memory to respond to addresses BF000 through BFFFF (hex), as normally set in the system, the switches would be set as follows:

S9 S8 S7 S6 S5 S4 S3 S2 S1 ON to enable memory

ON OFF ON ON ON ON ON ON

1 0 1 1 1 1 1 1 XXXX XXXX XXXX

B.3.3 Bus Addressing: I/O

The processors on both the Master and Slave Boards can access MULTIBUS I/O ports in the range of 8000 through BFFF (hex). All other I/O accesses will be either to onboard devices, or non-existent ports. Both BCLK and CCLK are driven by the Master Board at 8 MHz. In systems with Master Board CPUs running at 6 MHz, the bus clocks also run at 6 MHz.

B.3.4 Slave Addressing

Each DBSI Slave Card contains circuitry to generate interrupts to the Master, and to receive interrupts from any device on the MULTIBUS. This circuitry also enables each Slave Card to have its own unique identity, required for proper communication between the Master and each of up to six Slave Cards.

Each Slave Card contains several switches which set the ID of that card. Six switches are used for this purpose. The following list gives the possible settings of these switches, the resulting addresses to be used by the Master to generate interrupts to that Slave, and the corresponding interrupts to the Master generated by that card:

S1	S2	S3	S4	S5	S6	BUS INT	READ ID	INT ADDR
OFF	ON	ON	ON	ON	ON	0	41	BFFC
ON	OFF	ON	ON	ON	ON	1	21	BFFA
ON	ON	OFF	ON	ON	ON	2	11	BFF6
ON	ON	ON	OFF	ON	ON	3	09	BFEE
ON	ON	ON	ON	OFF	ON	4	05	BFDE
ON	ON	ON	ON	ON	OFF	5	03	BFBE

BUS INT is the MULTIBUS interrupt generated by the Slave Card with the switches set to the position shown.

READ ID is the value which a given Slave Card reads from its ID port with the switches on that card set to the position shown.

INT ADDR is the MULTIBUS I/O address which the Master uses to generate an interrupt to the Slave Card with the switches set to the position shown.

B.4 MEMORY AND I/O MAPS

The following charts illustrate the locations of the various types of memory within the DBS 16 20-bit addressing range, and the location of various I/O devices within its 16-bit addressing range.

B.4.1 Memory Addresses

The total memory addressing range of the 80186 is divided into five blocks, assigned as follows:

```
00000 -- 3FFFF  Onboard RAM - 256K bytes
40000 -- 7FFFF  Optional onboard RAM - 256K bytes
80000 -- BFFFF  MULTIBUS Memory Access including
                shared RAM
C0000 -- FDFFF  MULTIBUS Memory Access
FE000 -- FFFFF  Boot PROM (8K bytes)
```

B.4.1.1 Processor/Memory Organization

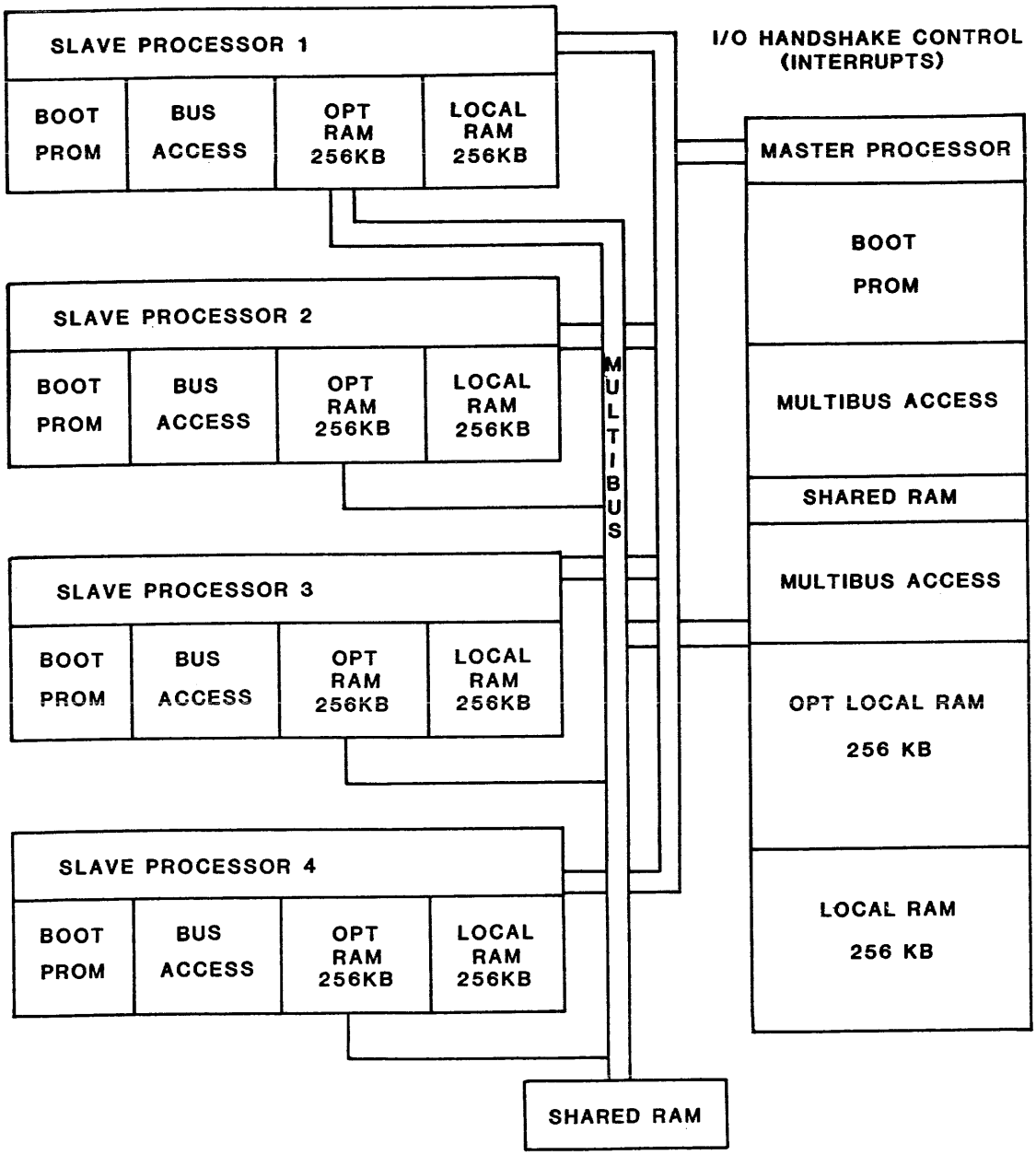


Figure B-1. DBS 16 System Processor/Memory Organization

B.4.1.2 Memory Map: Master and Slaves

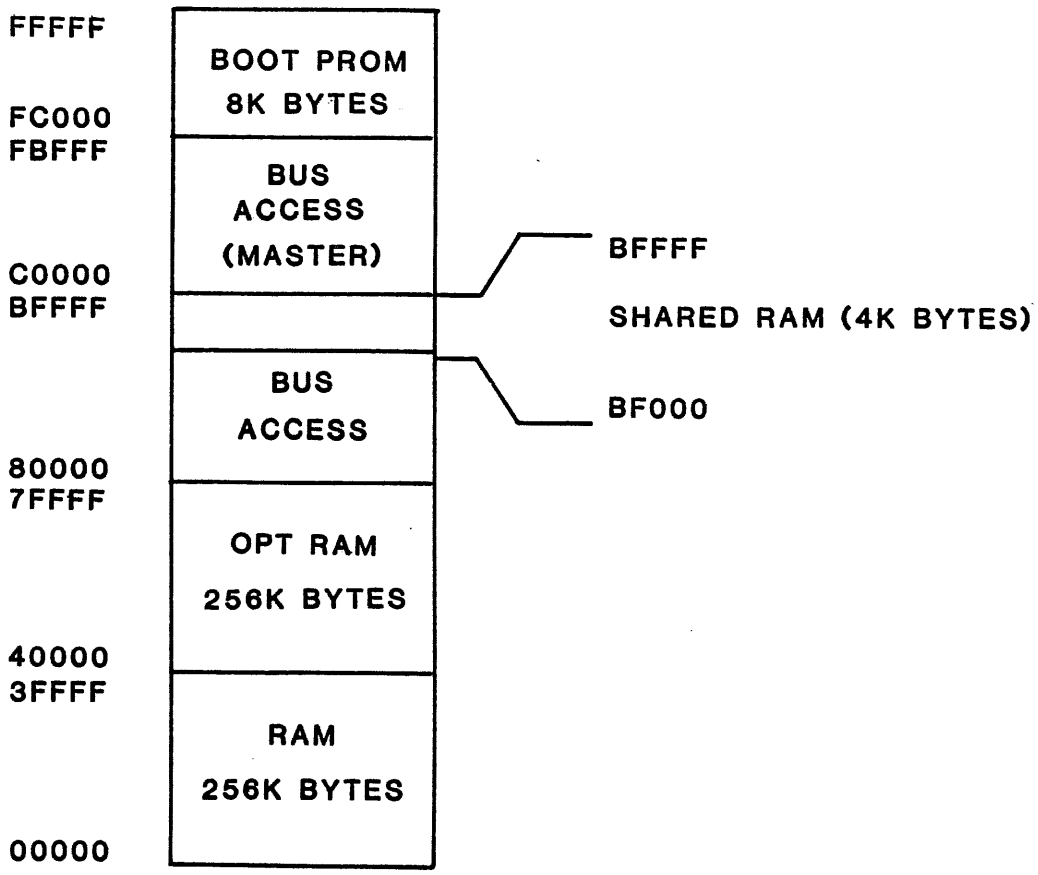


Figure B-2. Memory Map of Master and Slave Boards

B.4.2 Input/Output Addresses

The total I/O port addressing range of the 80186 is assigned as follows in this system: 0000-037F, onboard I/O ports; 8000-BFFF, Multibus I/O access.

B.4.2.1 Input/Output Map: Master Board

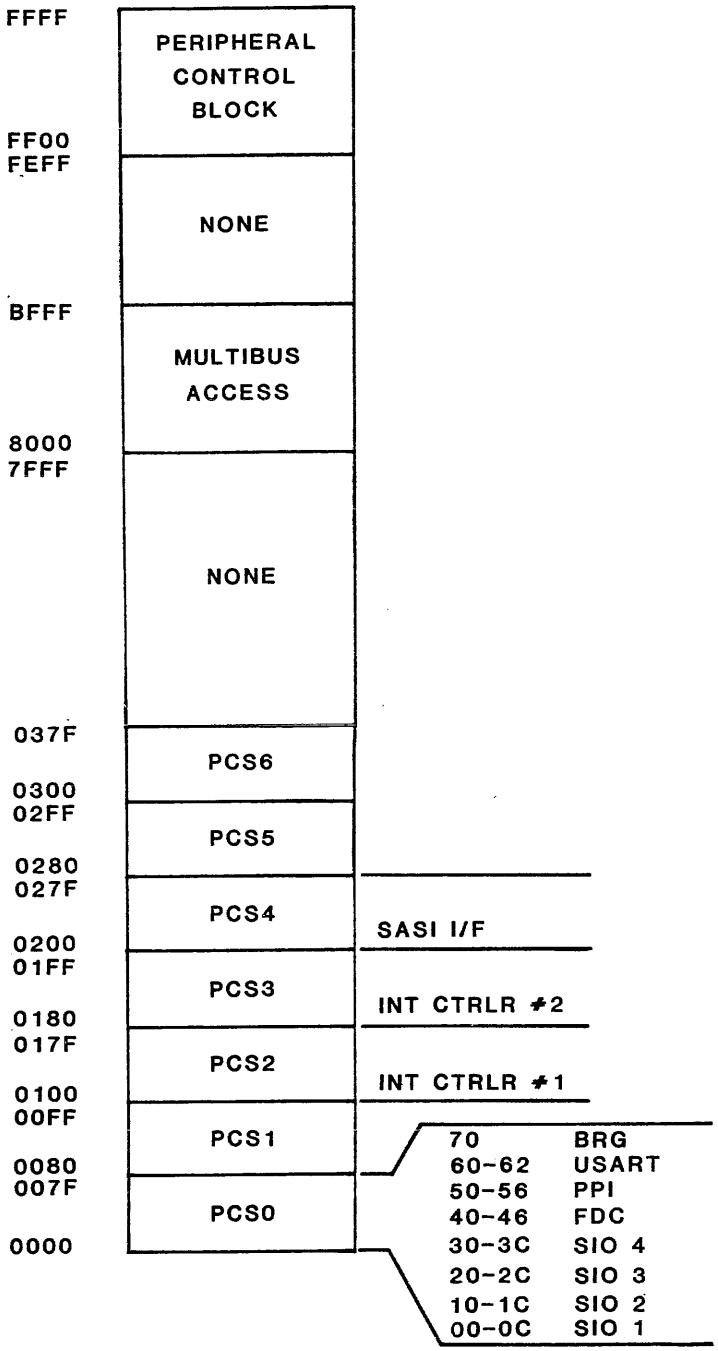


Figure B-3. I/O Map of Master Board

B.4.2.2 Input/Output Map: Slave Cards

MEMORY AND I/O MAPS (cont'd)

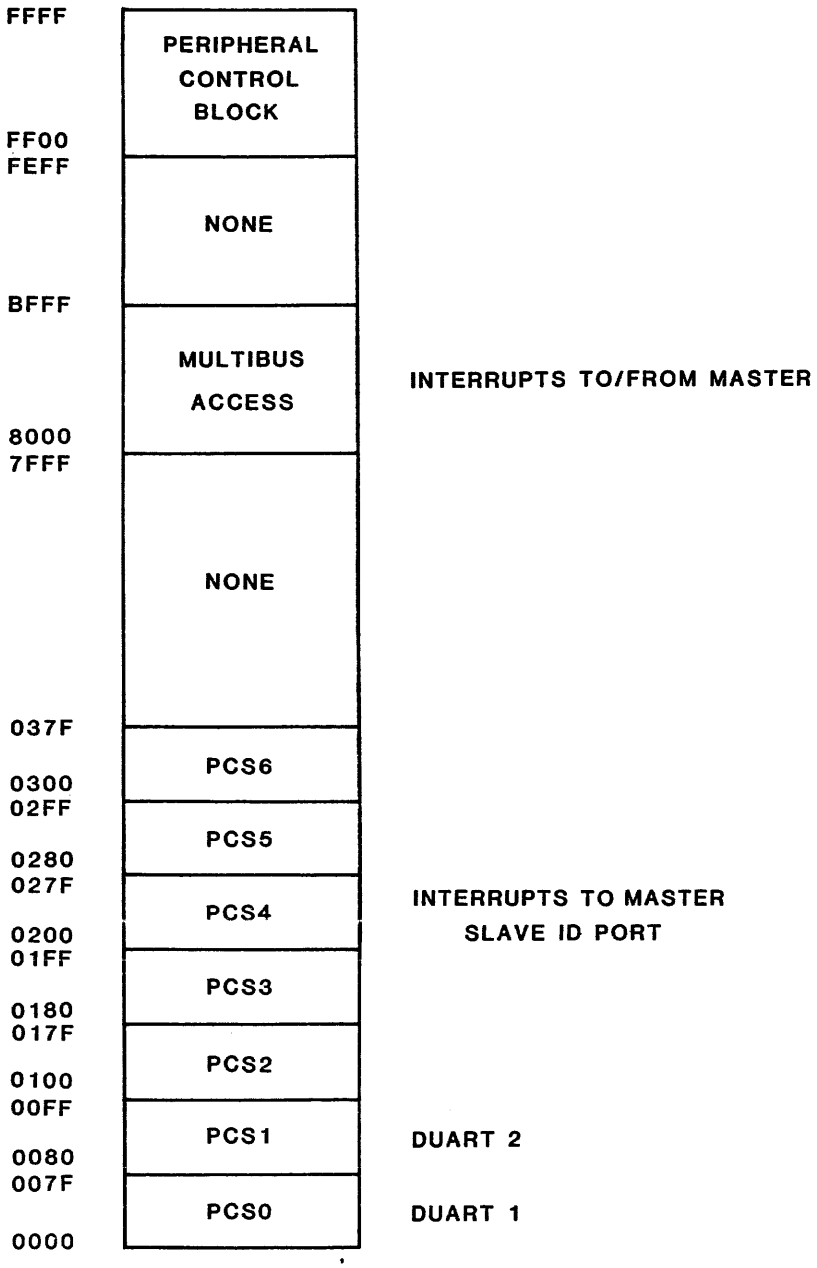


Figure B-4. I/O Map of Slave Cards

DBS 16 HARDWARE DESCRIPTION AND MAINTENANCE MANUAL

APPENDIX C
DBS 16 DIAGNOSTICS PROGRAM

C.1 GENERAL

There are two diagnostic packages available from DBSI. They are: MDP, the Master Diagnostic Package and SDP, the Slave Diagnostic package. MDP is used only on the DBS 16 Master desktop computers. SDP is a subset of MDP, consisting of the serial I/O tests and memory tests used in MDP.

> **CAUTION**
>
> NO WINCHESTER OR FLOPPY DISK TESTING IS ALLOWED FROM SLAVE UNITS.
>
> TEST THE DISKS FROM THE MASTER UNIT ONLY WHEN NO OTHER USERS ARE ON THE SYSTEM.

The main menu of the DBS 16 Diagnostics Program appears, as shown here:

Digilog DBS-16 Master Diagnostic Package V6.0

A. Winchester Diagnostics
B. Floppy-Disk Diagnostics
C. Character I/O Port Diagnostics
D. Memory Diagnostics

Test Category: (cursor is here)

NOTE: If expansion memory is present, another option will display as **E. Test Main & Expansion Memory.**

You then enter the letter (A,B,C,D (or E)) of the area you want to test and press the Return key. Each area of testing, the menus, and error messages are described in the following paragraphs.

C.2 WINCHESTER DIAGNOSTICS

If you select Test Category A, the following menu appears on your screen.

WINCHESTER DISK DIAGNOSTICS

1. **Format & Verify**
2. **Random Seek**
3. **Read/Write All Sectors**
4. **Read-Sector-Zero's** (Done by controller)
5. **Display a Sector**
6. **Re-set Disk Size**

Enter Test Selection: (cursor is here)

The functions performed by these tests are as follows:

1. Format/Verify

   This test properly formats your Winchester drive for operation in the DBS 16 System by producing a pattern of tracks and sectors. All data space is filled with the hexadecimal character "E5". After the Winchester is completely formatted, the program then goes back and verifies each sector.

> CAUTION
>
> THIS TEST WILL ERASE ALL PREVIOUSLY GENERATED FILES ON THE DRIVE.

   In normal operation, after formatting and verification, a message appears onscreen that the test was successfully completed. If a sector did not format properly, the program will attempt to reformat that particular track. If unsuccessful on a retry, it reallocates the track to the two percent reserve that is held on the disk, and displays the type of error found. In both cases, the offending head, cylinder, track, and sector are listed onscreen.

   If the two percent reserve is exceeded, a message appears, informing you that the disk is unusable and the drive should be replaced.

2. Random Seek

   When you select Test 2, this test causes the Winchester drive heads to randomly move and stop over 100 cylinders of the 306 in 10M and 15M drives, and 152 in a 5M drive.

   In normal operation, the screen displays the following:

   Enter number of passes: (Number of sets of 100)

   Beginning 100 Random Seeks of Hard Disk

   PASS 00: Head over Track XX
   PASS 01: Head over Track XX
   .
   .
   .
   PASS 99: Head over Track XX

   Should a problem be encountered, an error message appears onscreen informing you, for example, of **Seek error on Winchester.**

   If you want to stop the display as it scrolls onscreen, press CTRL-S. To resume the display, press CTRL-Q.

3. Read/Write All Sectors

If you select Test 3, this test writes the contents of a track into RAM memory, then writes it back into the same location on the Winchester, and then writes from the hard disk into another location on the Winchester and compares the contents of the two locations.

Should the data in the two hard disk locations differ, an error message appears onscreen. Otherwise, the message that the test was passed appears. This test takes between 12 and 15 minutes per 5M bytes of hard disk memory to complete.

4. Read-Sector-Zero's

This test is onboard the hard disk controller. It reads every sector 0 on every track, and then randomly selects 256 track 0's to reread. Again, an error message or a message that the test was successfully completed appears.

5. Display a Sector

If you select Test 5, this test displays the contents of a sector both as hexadecimal and ASCII data. The Winchester disk sectors are 256 bytes long; each sector can be displayed as 16 lines of 16 bytes. Additionally, the ASCII equivalent of each byte on a line is included at the end of each line.

After each sector is displayed, the prompt **continue?** appears. Pressing the Return key dumps the next sector. Pressing any other key displays the prompt, **Enter hex sector:.** You can the examine another range of sectors. Press Return in response to this prompt to exit this part of the diagnostics.

6. Re-set Disk Size

An intelligent controller is used to interface to the various size Winchesters used in DBS 16 computers. Normally, the operating system tells the controller what size Winchester is in the unit. There are also tests that request the size of the Winchester. However, there may be times when you want to tell the controller that the Winchester is a different size. This function does that.

When you have completed this function, you must either reset the disk size to the correct value, or simply reboot MP/M (or CP/M), to avoid confusion in the operating system.

C.3 FLOPPY DISK DIAGNOSTICS

If you select Test Category B, the following menu appears:

FLOPPY DISK DIAGNOSTICS

1. **Format & Verify**
2. **Random Seek**
3. **Read/Write All Sectors**
4. **Dump a Sector**
5. **Track Test**
6. **Dump a Track**

Enter Test Selection: (cursor is here)

These tests perform the following functions:

1. Format/Verify

This test formats and verifies, individually, each track of the floppy disk. If a track fails to format properly, the program stops and displays that failure as well as the type of error encountered and the contents of the track, sector, data, and select registers.

If you then change floppy disks, you must go back to the main menu and then return to this test.

In normal operation, after you select Test 1, the screen sequentially displays the following messages:

Formatting on 48 (or 96) tpi drive.
Enter 'F' to continue: (cursor is here)
Enter number of passes: (cursor is here)

Format/verify side 0:
fff ... (a total of 35 f's)
Format/verify side 1:
fff ... (a total of 35 f's)

Pass X of X complete!

Floppy Tests Complete? (Y/N):
(Y returns you to main menu
N returns you to this test menu)

2. Random Seek

When you select Test 2, this test causes the floppy disk drive head to randomly move and stop over 100 tracks. Each pass of 100 seeks takes about 15 seconds.

In normal operation, the screen displays the following:

Enter number of passes: (cursor is here)

Beginning 100 Random Seeks of Floppy Disk

PASS 00: Head over Track XX
PASS 01: Head over Track XX
•
•
•
PASS 99: Head over Track XX

If you want to stop the scroll, press CTRL-S; to resume, press CTRL-Q. Again, if there are any problems, a message appears onscreen.

3. Read/Write All Sectors

If you select Test 3, the program reads the contents of a sector into RAM, writes them back over the same location on the floppy disk, then writes them from the floppy into another location in RAM and compares the two to see if the data was stored intact.

In normal operation, the following appears sequentially onscreen:

Beginning read/write/read/compare of ALL sectors.
Enter number of passes: (cursor is here)

Checking side 0
ccc ... (35 c's)
Checking side 1
ccc ... (35 c's)

Pass X of X complete!
Floppy Tests Complete? (Y/N): (cursor is here)

4. Display a Sector

If you select Test 4, this test displays the contents of a sector as hexadecimal and ASCII data. The floppy disk sectors are 1024 bytes long; each sector can be displayed as 64 lines of 16 bytes. Additionally, the ASCII equivalent of each byte on a line is included at the end of each line.

After each sector is displayed, the prompt **continue?** appears. Pressing the Return key dumps the next sector. Pressing any other key displays the prompt, **Enter hex sector:.** You can the examine another range of sectors. Press Return in response to this prompt to exit this part of the diagnostics.

5. Track Test

This test allows you to select a physical track (0 through 34 on DBSI 48 TPI disks, 0 through 79 on 96 TPI disks), and the side of the disk to test.

After you make these selections, the utility moves the disk head to the selected track, and performs the chosen operation (Read or Write), until you press CTRL and X simultaneously. Both tests use a full track read or write. The pattern written during a write test is a standard disk format pattern. This test must be performed correctly, and only with the proper equipment.

The Read track test merely positions the disk head at the desired track, selects the side, and performs full track read until CTRL-X is pressed.

6. Track Dump

This test is similar to sector display (dump). Here, however, the entire track is displayed, including certain "internal" information of interest only to the qualified technician.

C.4 CHARACTER I/O PORT DIAGNOSTICS

If you selected Test Category C, the following menu appears:

Character I/O Port Diagnostics

1. Workstation Ports
2. RS-232 Port
3. Printer Port

Enter Test Selection: (cursor is here)

These tests perform the following functions:

1. Workstation Ports

When you select Test 1, you can verify the performance of the chip handling the workstation ports, including the interrupt mechanism. Elements involved in a workstation test are the Test port with loopback connector installed, and a Control port with a standard video terminal attached.

NOTE: The loopback connection is made at the Test port by shorting pins 2 and 3 of an RS-232 connector (DB-25) together on a four-wire cable with an SDL connector on the other end.

The Test port is then configured via the following dialogue:

Enter TEST port (1,2,3,4)
(Supply the number of the port with loopback connector attached.)

Enter CONTROL port (1,2,3,4)
(Supply the number of the port with video terminal attached.)

Enter the Baud-rate:
(Enter any standard baud rates from 110 to 9600.)

Number of Stop-bits (1 or 2):

Number of Bits-per-character (5 - 8):

Parity Enable (Y/N):
(If you select yes (Y), you must also select the following:)

Odd or Even (0, 1):
(0 = even parity; 1 = odd parity)

Attach loopback connector, Hit return when ready:

When the test is in progress, you can abort data transmission by pressing the space bar on the control terminal. This gives you the option of continuing with the current port, configuring another port, or exiting this part of the diagnostics.

2. RS-232 Port

When you select Test 2, by attaching a loopback connector, data is sent out and the system checks to see if the identical data is returned. Here, the loopback is achieved by shorting together pins 2 and 3 of the port connector.

In normal operation, the following messages appear sequentially onscreen:

Enter the Baud-rate:
(Enter any standard baud rate from 110 to 9600.)

Number of Stop-bits (1 or 2):

Number of Bits-per-character (5 - 8):

Parity Enable? (Y/N):
(If you select Y, also select from the following:)

Odd, or Even (0, 1):
(0 = even parity; 1 = odd parity)

Attach Loopback connector, Hit return when ready:

When the test is in progress, you can abort data transmission by pressing the space bar on the control terminal. This gives you the option of continuing with the current port, configuring another port, or exiting this part of the diagnostics.

If the port is working properly, the loop continues until you press CTRL-Z. If there is a problem, an error message appears.

3. Printer Port

If you select Test 3, this test exercises the parallel printer output port when the printer is attached.

In normal operation, the following message appears on your screen:

Attach printer, Hit return when ready (cursor is here)

C.5 MEMORY DIAGNOSTICS

The memory test handles the optional 256K expansion memory. If the software detects the additional memory, the user-prompts are adjusted to indicate a "512kb" memory test, and the test is performed on the larger size memory.

The actual test writes a word of all ones, complements the value just written, and tests for a zero value after a "not" operation. If an error is detected, you are notified of the segment and offset of the error. The test pauses and holds the displayed error location until you acknowledge the display by pressing the Return key.

As each 8K bit section is tested successfully, an "m" is displayed. When total memory has been tested, the program relocates to the tested memory, and then tests the memory in which it resided.

If there is an error in memory, the test stops and displays the faulty location. To continue the test, press the Return key. Press CTRL-C at any time to abort this test.

DBS 16
HARDWARE DESCRIPTION AND MAINTENANCE MANUAL

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