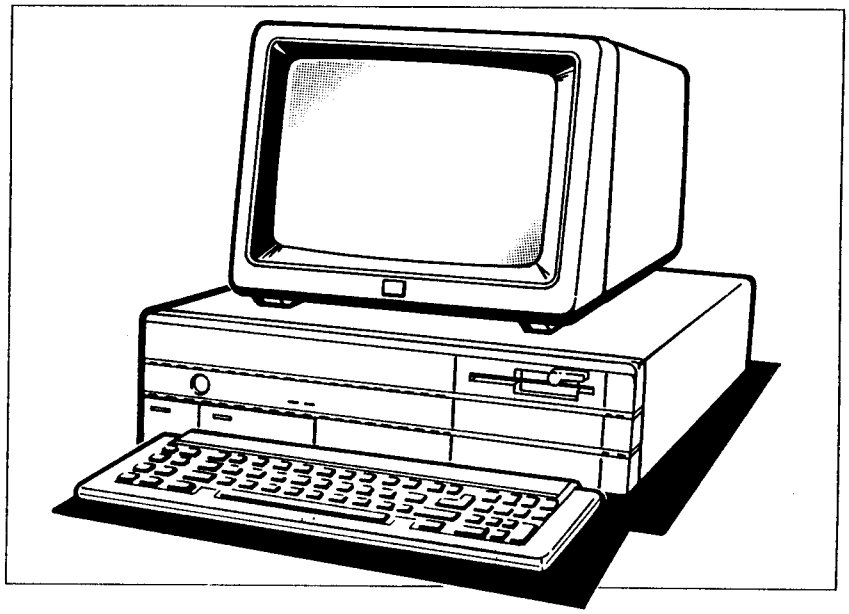
EPSON PC AX

TECHNICAL MANUAL



Seiko Epson Corporation
Nagano, Japan

Y12699900201

FCC COMPLIANCE STATEMENT

This equipment uses and generates radio frequency energy and it not installed and used properly, that is in strict accordance with the manufacture's instructions, may cause interference to radio and television reception.

It has been type tested and found to comply with limits for a Class B computing device in accordance with Sub-part J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment dose cause interference to radio or television reception, which can be determined by turning the equipment on and off, the user is encouraged to try to correct the interference by one or more of the following measures:

- reorient the receiving antenna
- relocate the computer with respect to the receiver
- move the computer away from the receiver
- plug the computer into a different outlet so that the computer and receiver are on different branch circuits

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet, prepared by the Federal Communications Commission, helpful:
"How to Identify and Resolve Radio-TV interference Problems. "This booklet is available from the U.S. Government Printing Office, Washington. D.C., 20402, Stock No. 044-000-00345-4.

You can determine whether your computer is causing interference by turning it off. If the interference stops, it was probably caused by the computer or its peripheral devices. To further isolate the problem, disconnect either the peripheral device or its I/O cable.

These devices usually require shielded cable. For Epson peripheral devices, you can obtain the proper shielded cable from your dealer. For non-Epson devices, contact the manufacturer or dealer for assistance.

Seiko Epson Corporation, Nagano, Japan

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PRECAUTIONS

Precautionary notations throughout the text are categorized relative to 1) personal injury and 2) damage to equipment.

DANGER — Signals a precaution which, if ignored, could result in serious or fatal personal injury. Great caution should be exercised in performing procedures preceded by DANGER Headings.

WARNING — Signals a precaution which, if ignored, could result in damage to equipment.

The precautionary measures itemized below should always be observed when performing repair/ maintenance procedures.

DANGER

1. ALWAYS DISCONNECT THE PRODUCT FROM BOTH THE POWER SOURCE AND PERIPHERAL DEVICES PERFORMING ANY MAINTENANCE OR REPAIR PROCEDURE.

2. NO WORD SHOULD BE PERFORMED ON THE UNIT BY PERSONS UNFAMILIAR WITH BASIC SAFETY MEASURES AS DICTATED FOR ALL ELECTRONICS TECHNICIANS IN THEIR LINE OF WORK.

3. WHEN PERFORMING TESTING AS DICTATED WITHIN THIS MANUAL, DO NOT CONNECT THE UNIT TO A POWER SOURCE UNTIL INSTRUCTED TO DO SO. WHEN THE POWER SUPPLY CABLE MUST BE CONNECTED, USE EXTREME CAUTION IN WORKING ON POWER SUPPLY AND OTHER ELECTRONIC COM-PONENTS.

WARNING

1. Repairs on Epson product should be performed only by an Epson certified repair technician.

2. Make certain that the source voltage is the same as the rated voltage, listed on the serial number/rating plate. If the Epson product has a primary AC rating different from available power source, do not connect it to the power source.

3. Always verify that the Epson product has been disconnected from the power source before removing or replacing printed circuit boards and/or individual chips.

4. In order to protect sensitive microprocessors and circuitry, use static discharge equipment, such as anti-static wrist straps, when accessing internal components.

5. Replace malfunctioning components only with those components by the manufacture; introduction of second-source ICs or other non-approved components may damage the product and void any applicable Epson warranty.

REVISION	ISSUE DATE	REVISION PAGE
REV.A	December 1986	-
REV.B	September 1988	1-7, 2-2, 2-6, 2-7, 2-10, 2-15, 2-25, 2-33, 2-36, 2-39, 2-40, 2-42, 2-51, 2-73 Chapter 8 added

PREFACE

This manual describes the theory of operation of the EPSON PC AX microcomputer system, and includes troubleshooting, repair, and maintenance procedures for serving system subassemblies. This text is divided into eight chapters:

CHAPTER 1. PRODUCT DESCRIPTION . . . Describes the features and specifications of the computer, illustrates system components, and lists the logic configuration of the primary circuit board.

CHAPTER 2. PRINCIPLES OF OPERATION . . . Details the functional organization of the logic circuitry. This chapter also illustrates the gate array pin configurations.

CHAPTER 3. OPTIONS . . . Describes option card specifications and the operating principles of the options.

CHAPTER 4. TROUBLESHOOTING . . . Provides instructions for isolating computer malfunctions.

CHAPTER 5. DISASSEMBLY AND ASSEMBLY . . . Describes system disassembly for replacement of malfunctioning subassemblies.

CHAPTER 6. ADJUSTMENT AND MAINTENANCE . . . Lists the necessary adjustments for unit assembly and servicing.

CHAPTER 7. DIAGRAMS AND REFERENCE MATERIALS . . . Describes jumper settings and connector pin assignments. This chapter also provides exploded circuit board layout and schematic diagrams for use in conjunction with the text.

CHAPTER 8. DIFFERENCES BETWEEN 10MHz AND 12 MHz . . . Describes between the EPSON PC AX 10MHz and the 12MHz, and includes the schematics for use in conjunction with the the 12MHz.

Subsequent product modifications will be brought to your attention via Service Bulletins; please revise the text as bulletins are received.

This document is subject to change without notice.

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1

PRODUCT DESCRIPTION

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1.1 FEATURES

The EQUITY III+ / EPSON PC AX computer system includes two major elements; a main system unit and a keyboard.

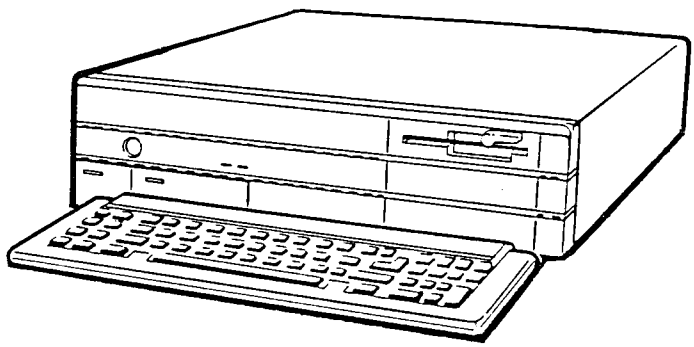

FIGURE 1-1-1. MAJOR COMPONENTS

The EQUITY III+ / EPSON PC AX hardware configuration has a high degree of compatibility with the IBM AT and the new AT.

System Performance

EQUITY III+ / EPSON PC AX has three CPU execution speeds, these are the IBM AT speed (6 MHz), the new AT speed (8 MHz) and a faster speed (10 MHz). Speed is selected by setting a three-position switch easily accessed from the front. The user can see the selected execution speed by the color of a LED.

Wait Cycles

EQUITY III+ / EPSON PC AX uses several types of internal devices, such as RAM, ROM, 16-bit extension memory, 16-bit I/O device, 8-bit extension memory and 8-bit I/O device at every CPU speed. In the case of 6 MHz or 8 MHz, the number of wait cycles is the same as the AT or the new AT.

NPX Clock

The clock input to the numerical processor extension (NPX) may be changed according to the NPX version. The standard clock input is 8 MHz (AT uses 4 MHz and the new AT uses 5.33 MHz). Other clock-inputs, 20, 16, or 12 MHz (divided by three in the NPX) may be selected by setting jumper connectors on the system board.

Mass Memory

EQUITY III+ / EPSON PC AX supports 4 types of built-in mass memory.

Mass Memory Slots

EQUITY III+ / EPSON PC AX has 5 half-height slots for FDD's and HDD's. There are several ways to install the drives in these slots: (1) 4 half-height drives, (2) 3 half-height drives and a full-height drive, (3) a half-height drive and 2 full-height drives. A maximum of four drives can be installed.

Power Supply

EQUITY III+ / EPSON PC AX has an IBM AT compatible power unit. Its specification is world wide, using 115 V /220 V, switch selected, UL/CSA and TUV standard, and FCC/FTZ standard. The number of power cables is 4.

Multi-function Card

The multi-function card in the EPSON proprietary slot provides the serial communication port, parallel printer port and floppy disk controller.

Hard Disk Controller

The hard disk controller contained in the prorietary slot will control two hard disks.

Packaging

All switches and controls are easily accessible. Switches control the processor execution speed, and the type of the display, color or monochrome. It is easy to connect the keyboard, control the volume, push the reset button, turn the power on or off, and lock or unlock the main unit. When the unit is locked, the system does not accept key input and ignores the reset button.

Exterior

The unit is designed in line with the EQUITY / EPSON PC series, which visually distinguishes it from the numerous compatibles.

1.2 SPECIFICATION

The following sections describe detail specifications by major subassembly.

POWER SUPPLY

Input	115 VAC	Min. 92 V Max. 132 V	Max. 4 A
	230 VAC	Min. 196 V Max. 265 V	Max. 2.5 A
Frequency	49 - 61Hz		
Power Consumption	115 VAC:		230 VAC approx. 60W
Surge Current	42 A O-P (0.5 sec. more)		

INSULATION STRENGTH ..... 115 VAC: AC 1.25 kV (1 min.) (AC-FG, AC-Secondary)
230 VAC: AC 1.25 kV (1 min.) (AC-FG)
AC 3.75 kV (1 min.) (AC-Secondary)

INSULATION RESISTANCE ..... 25 MOhm more (500 VDC) (AC-FG,AC-Secondary)
1 MOhm more (250 VDC) (SG-FG) (DIC short jumper not installed)

ENVIRONMENT CONDITIONS .....

	OPERATING	**NON-OPERATING**	**STORAGE**
Temperature	5°C to 35°C	-20°C to 60°C	-40°C to 60°C
Humidity (non-condensing)	20% to 80%	10% to 90%	5% to 95%
Maximum wet bulb	29 deg.	40 deg.	45 deg.
Vibration	0.2 G	1 G (non-HDD) 0.5 G (HDD)	3 G (non-HDD) 0.5 G (HDD)
Shock (non-HDD)	1 G (less than 10ms)	3 G (less than 10ms)	30 G (less than (10ms)
Shock (HDD)	1 G (less than 25mm 0-60Hz)	3 G (less than 25mm 0-60Hz)	20 G (less than 25mm 0-60Hz)
Altitude (HDD)	0 to 3000 m. ASL	-300 to 3600 m. ASL	-300 to 3600 m. ASL

1.2.1 Main System Unit Specifications

PROCESSOR	80286-10
CO-PROCESSOR	80287-8
ROM	64KB (27256 x 2)
RAM	640KB is standard
MASS MEMORY	5 1/4" 1.2MB FDD is standard
MASS MEMORY SLOTS	6 16-bit I/O expansion slots 3 8-bit I/O expansion slots
CPU CLOCK	6 MHz, 8 MHz, 10 MHz (Switch selectable)
WAIT CYCLES	Selectable
DIMENSIONS (W x D x H)	498.5 x 442 x 169 mm
WEIGHT	14.5 Kg (Standard model - 1FDD)

1.2.2 Keyboard Specifications

LAYOUT	New AT compatible
CORD	Approx. 2 meters
DIMENSIONS (W x D x H)	490 x 197.5 x 47.7 mm
WEIGHT	1.8 Kg

1.2.3 FD1155C Floppy Disk Drive Specification

High Density Mode		
Capacity (KBytes)		(MFM / FM)
	Unformatted	1670 / 830
	Formatted	1065 / 532 (256 byte x 26 sector)
		1229 / 614 (512 byte x 15 sector)
		1311 / 655 (1024 byte x 8 sector)
Transfer Rate (K-bits/sec)		500 / 250
Number of Tracks		160 (80 tracks x 2 sides)
Recording Density (BPI max.)		9870

Normal Density Mode	
Capacity (KBytes)	(MFM / FM)
Unformatted	1000 / 500
Formatted	655 / 328 (256 byte x 16 sector)
Transfer Rate	300 / 150
Number of Tracks	160 (80 tracks x 2 sides)
Recording Density (BPI max.)	5922
Seek Speed (1 track)	3 ms
Seek Settling Time	15 ms
Head Loading Time	35 ms
Disk Speed	360 RPM
Track Density	96 TPI
Recording Method	MFM/FM
Power Consumption x 2	4.8 w

1.2.4 MD5501-61 Floppy Disk Drive Specification

	Normal Density Mode		High Density Mode
Capacity (KBytes)	48 TPI	96 TPI	96 TPI
Unformatted	500	1000	1667
Formatted (IBM format)	327.7 (8 sector)	655.4 (16 sector)	1065 (26 sector)
Transfer Rate (Kbits/sec.)	300	300	500
Access Time (track-track)(ms)	10	5	3
Recording Density (BPI)	5876	5922	9870
Number of Tracks (per side)	40	80	80
Seek Settling Time	15 ms		
Disk Speed	360 RPM		
Recording Mode	MFM		
Power Consumption	3.0 w		

1.2.5 D5146H Hard Disk Drive Specification

Capacity		
Unformatted	51.24	MBytes
per Cylinder	83,328	bytes
per Track	10,416	bytes
Formatted	40.30	MBytes
per Cylinder	65,536	bytes
per Track	8,192	bytes
per Sector	256	bytes
Number of Cylinders	615	
Sectors per Track	32	
Bytes per Sector	256	
Number of Disks	4	
Number of Heads	8	
Transfer Rate	625	KB/sec
Access Time		
Track-Track	8	ms
Average Seek	40	ms
Max. Seek	75	ms
Disk Speed	3600	RPM
Start Time	25	sec.
Stop Time	30	sec.
Recording Method	MFM	
Recording Density	9000	BPI
Track Density	700	TPI

Environment Conditions	Operating	Storage
Temperature	5°C - 45°C	-40°C - 60°C
Humidity	8% - 80% (29°C)	
Vibration	0.2 G	0.5 G (0-60Hz, less than 25 mm)
Shock	2.0 G	20.0 G
Altitude	0 - 3000 m	-300 - 3600 m

Power Consumption	3.0 w

1.2.6 HMD-720 Hard Disk Drive Specification

Capacity	
Unformatted	25.5 MBytes
per Track	10,416 bytes
Formatted	20.0 MBytes
per Track	8,192 bytes
per Sector	256 bytes
Number of Cylinders	615
Number of Tracks	2460
Sectors per Track	32
Bytes per Sector	256
Number of Disks	2
Number of Heads	4
Transfer Rate	5 Mbits/sec
Access Time	
Track-Track	18 ms
Average Seek	69 ms
Max. Seek	150 ms
Disk Speed	3528 RPM +/-1%
Recording Method	MFM
Recording Density	12900 BPI
Track Density	910 TPI
Interface	ST-506/412

Environment Conditions	Operating	Storage
Temperature	5°C - 50°C	-40°C - 65°C
Humidity	8% - 80% (26C)	8% - 85% (30C)
Altitude	3000 m	10000 m

Shock-Vibration		
No Soft Errors		
Vibration	0.4 G, 36-500 Hz	
Shock	8 G, 10 ms	
No Hard Errors		
Vibration	2 G, 14-500 Hz	3 G, 12-500 Hz
Shock	20 G, 10 ms	40 G, 10 ms

Power Consumption	8.0 w

1.3 HARDWARE CONFIGURATION

1.3.1 Main System Unit Components

TABLE 1-3-1. ANTA BOARD COMPONENT DESCRIPTION

NAME	MODEL	Qty	FUNCTION
CPU	80286-10	1	16 bit CPU
NPX	80287-8	1	Co-processor (socket only)
DMAC	8237A-5	2	DMA control
INTC	8259A	2	Interrupt control
TIMER	8254-2	1	Support 3 clock channels
REAL TIME	146818	1	System clock, calender and CMOS RAM
KEYBOARD I/F	8042	1	Interface between 80286 and keyboard
GAATAB	E01085CB	1	Controls CPU address bus (A16-0), system address bus (SA16-0) and internal address bus (XA16-0). Generates refresh address.
GAATCB	E01086CA	1	Control bus (I/O write pulse, I/O read pulse, memory write pulse, memory read pulse) and 7 MSB of address bus (A23-17) and bus high enable signal.
GAATDB	E01068CA	1	Control CPU bus (D15-0), system data bus (SD15-0) and memory data bus (MD15-0)
GAATCK	E01068CA	1	Clock generator, bus controller and shut down circuit.
GAATRF	E01069BB	1	Controls D-RAM refresh, DMA transfer, 16-8 data bit conversion, and wait state insertion.
GAATIO	E01092EA	1	Address decoder for I/O space and I/O registers.

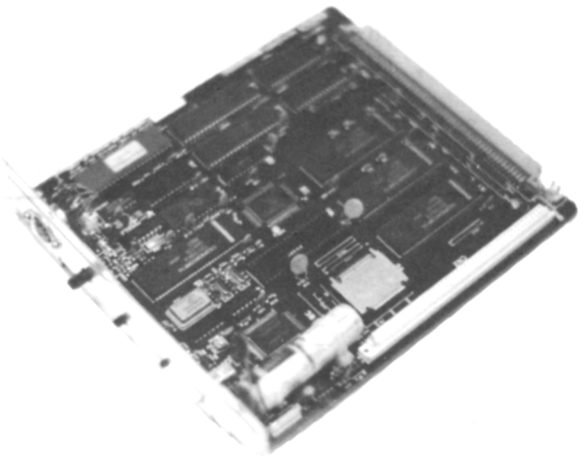

FIGURE 1-3-1. ANTA BOARD

TABLE 1-3-2. ANT-RM BOARD COMPONENT DESCRIPTION

NAME	MODEL	Qty	FUNCTION
RAM	MB81256-10Z	18	256Kbit dynamic RAM (Parity check RAM)
	MB81464-12P	4	64KB x 4 dynamic RAM
	uPD4164-12	2	Parity check RAM
ROM	27256	2	BIOS ROM
GAATM1	E01090BA	1	Address decoder for memory space and parity checker / generator for system D-RAM.
GAATM2	E01091EA	1	Generates D-RAM address (MA8-0) and D-RAM access signals (RAS, CAS and WE)

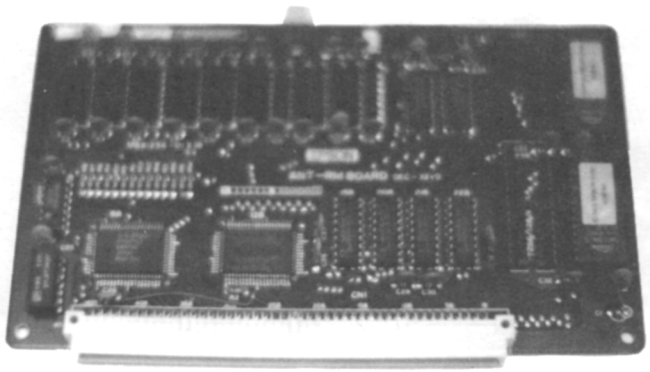

FIGURE 1-3-2. ANT-RM BOARD

TABLE 1-3-3. SPFG BOARD COMPONENT DESCRIPTION

NAME	MODEL	Q'ty	FUNCTION
FDC	uPD765A	1	Controls FDD's.
GAATSP	E01093BA	1	Parallel port and address decoder for serial port.
GAATFD	E01094BA	Q	Controls 360KB and 1.2MB diskette drives. Includes FDOR (Floppy digital output register), FCR (Floppy control register) and write precompensation circuit.
SERIAL CONTROLLER	16450	1	Controls serial data transfer.

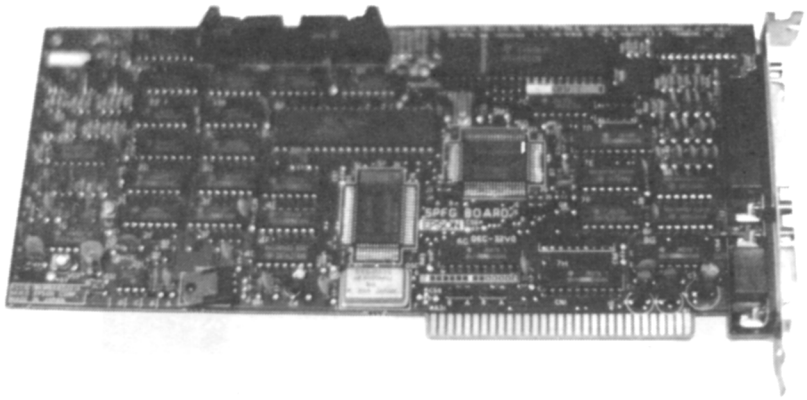

FIGURE 1-3-3. SPFG BOARD

TABLE 1-3-4. ATRPS UNIT OUTPUTS

NOMINAL OUTPUT [VDC]	LOAD CURRENT MIN.[A]	LOAD CURRENT MAX.[A]	REGULATION TOLERANCE	OVERLOAD PROTECTION [A]
+5	2.5	20	+- 4%	35
-5	0	0.3	* +-10%	3
+12	0	4.8 (7.0)	+- 5%	16
-12	0	0.3	+-10%	3

* 10 sec.

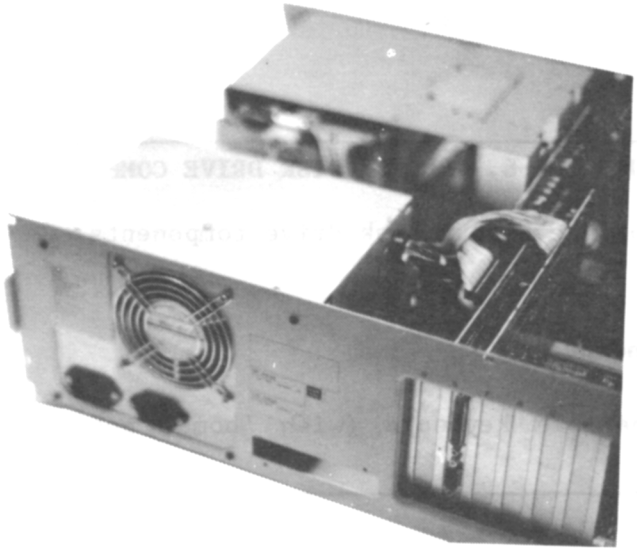

FIGURE 1-3-4. ATRPS UNIT

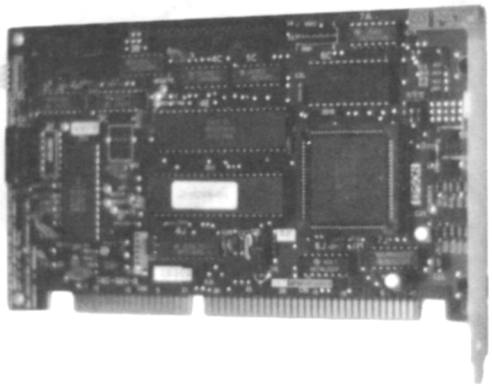

FIGURE 1-3-5. WHDC BOARD

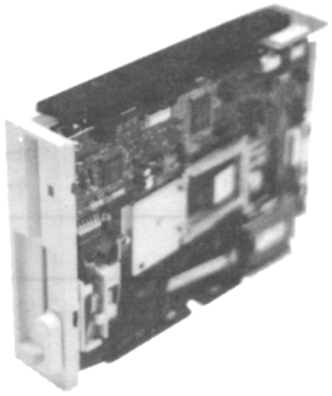

FIGURE 1-3-6. FLOPPY DISK DRIVE COMPONENTS

Refer to Chapter 3 for the Floppy disk drive components.

1.3.2 Keyboard Components

The new IBM AT compatible keyboard (with 'home' position keys F, J and 5 marked).

FIGURE 1-3-7. KEYBOARD COMPONENT

CHAPTER

2

PRINCIPLES OF OPERATION

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2.1 MAIN SYSTEM UNIT COMPONENTS

The following diagram shows a functional block diagram of the EQUITY III+ / EPSON PC AX.

All interface circuit except key board interface should be installed on a option slot.

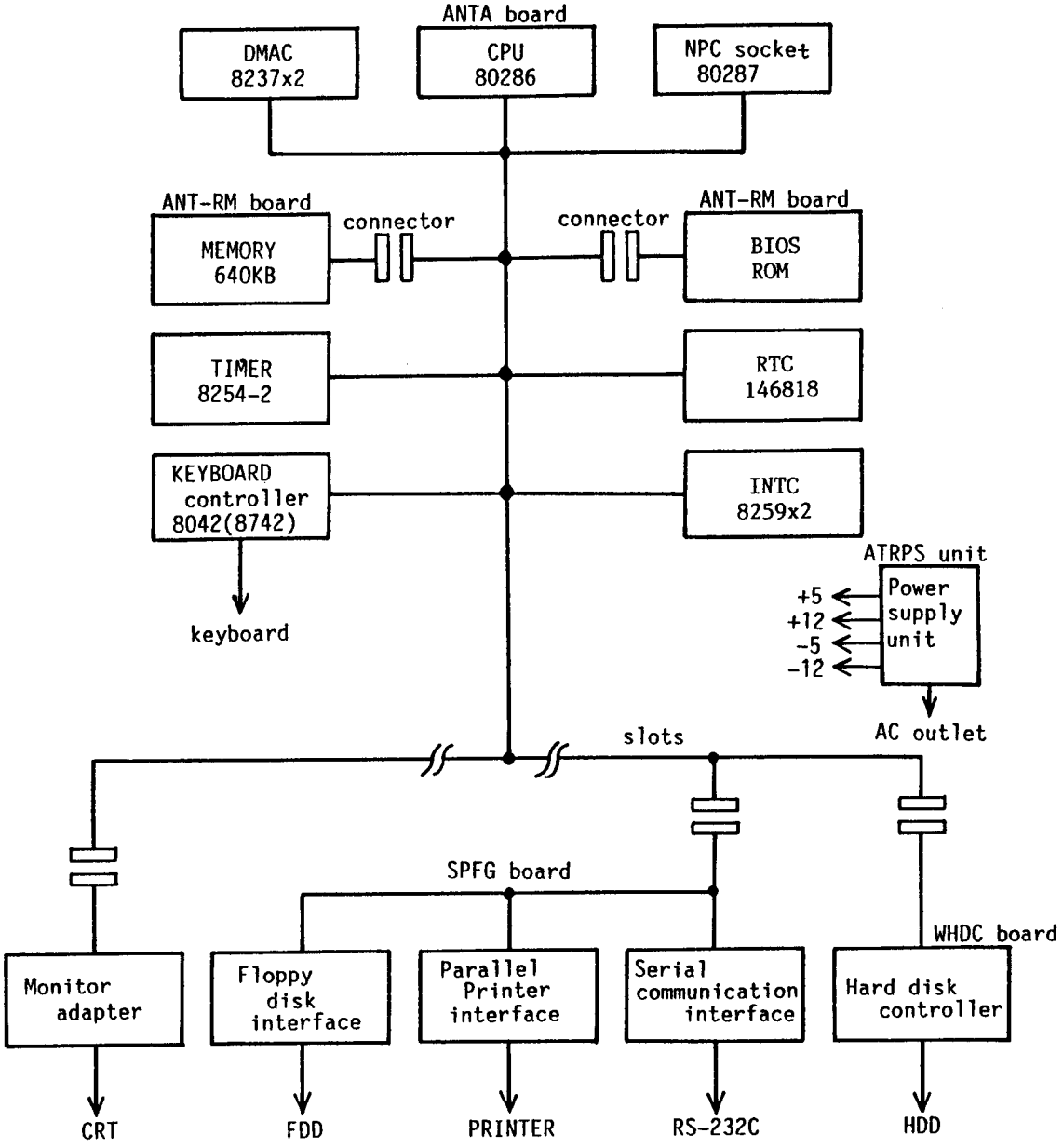


FIGURE 2-1-1. LOGIC BLOCK DIAGRAM

2.2 ATRPS POWER SUPPLY UNIT

ATRPS Unit is available in both 115-volt supply and 230-volt supply. Switch S1 selects either 115-volt supply or 230-volt supply, and simultaneously switches a fuse.

Basic Operation

ATRPS Unit uses the Forward Converter Switching Regulation way.

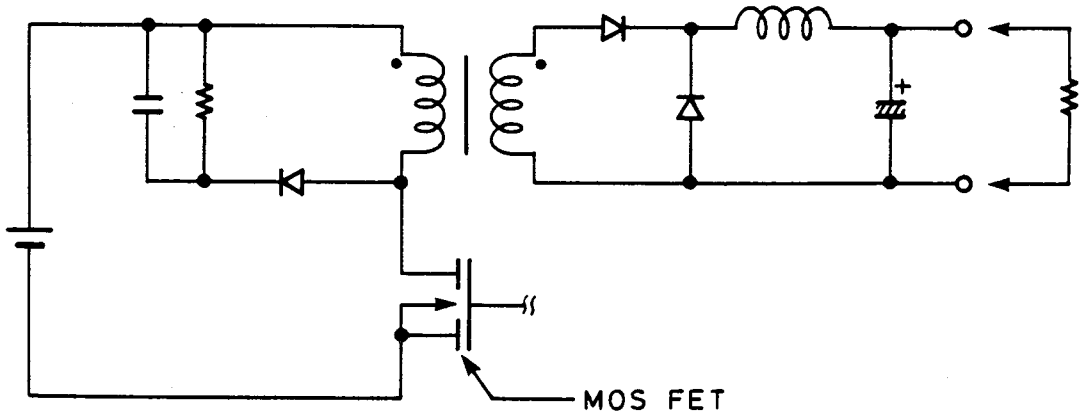


FIGURE 2-2-1. BASIC OPERATION CIRCUIT

2.2.1 Primary Oscillation Circuit

The HA16654 controls the MOS-FET. By supplying power to the HA16654, current flows in the MOS-FET.

2.2.1.1 Power supply circuit

Power supply circuit for the HA16654 is explained by the following 2 steps:

1. From power on till the transformer for switching oscillates correctly.
2. After the transformer for switching has oscillated correctly.

1. From POWER ON till the transformer for switching oscillates correctly.

The power supply circuit is shown in Figure 2-2-2.
Zenor Diode D10 and D11 works so as not to supply the HA16654 with a voltage until the input voltage V reaches the fixed-level voltage.

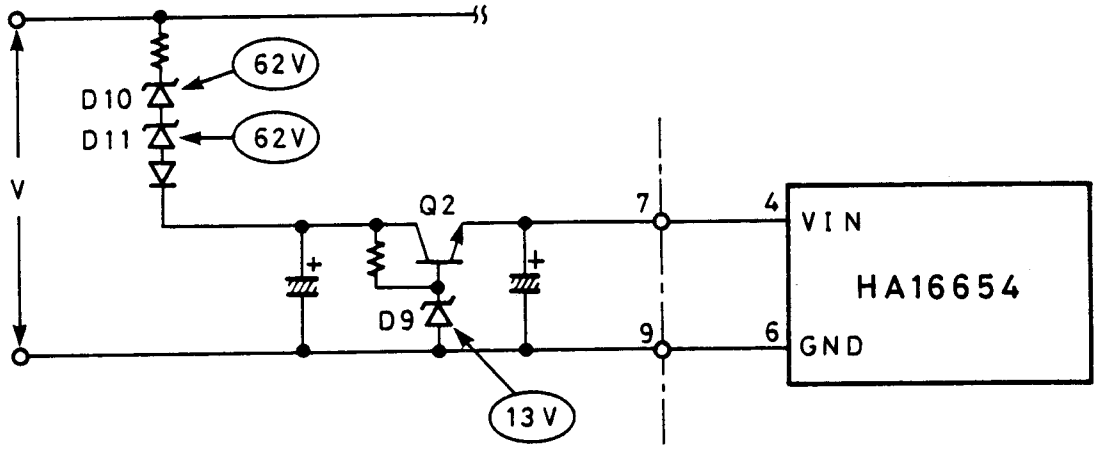


FIGURE 2-2-2. SWITCHING OSCILLATION CIRCUIT I

2. After the transformer for switching has oscillated correctly.

No current is present in R11, D10, D11, and D19 because the voltage supplied from D12 and R15 is higher than the voltage supplied from R11, D10, D11 and D19. This causes the increase of efficiency of the ATRPS Unit.

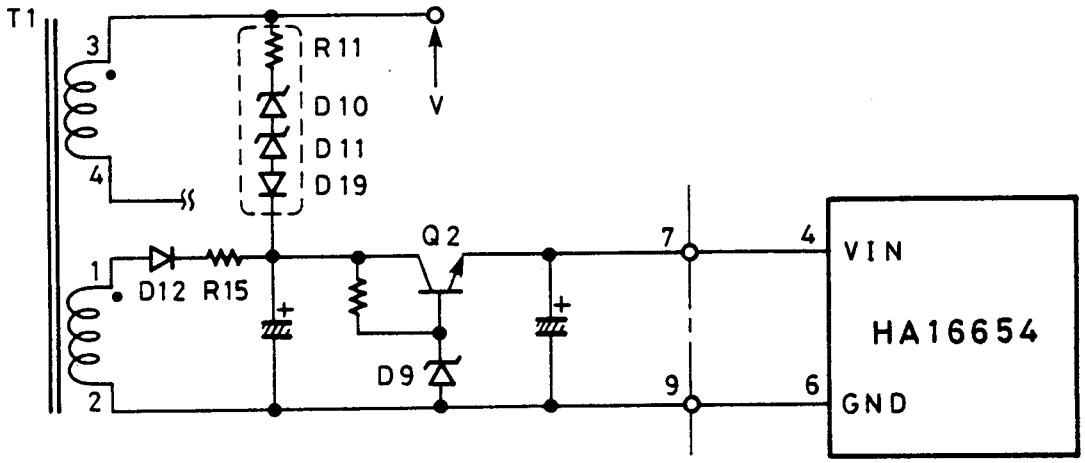


FIGURE 2-2-3. SWITCHING OSCILLATION CIRCUIT II

2.2.1.2 Overcurrent Prevention Circuit of the MOS-FET On-Off Control Circuit

The circuit which consists of the transistor Q4 and Q5 works as follows:

* If the input voltage is higher than the standard voltage, the Q5 collector current flows instead of the Q4 collector current.

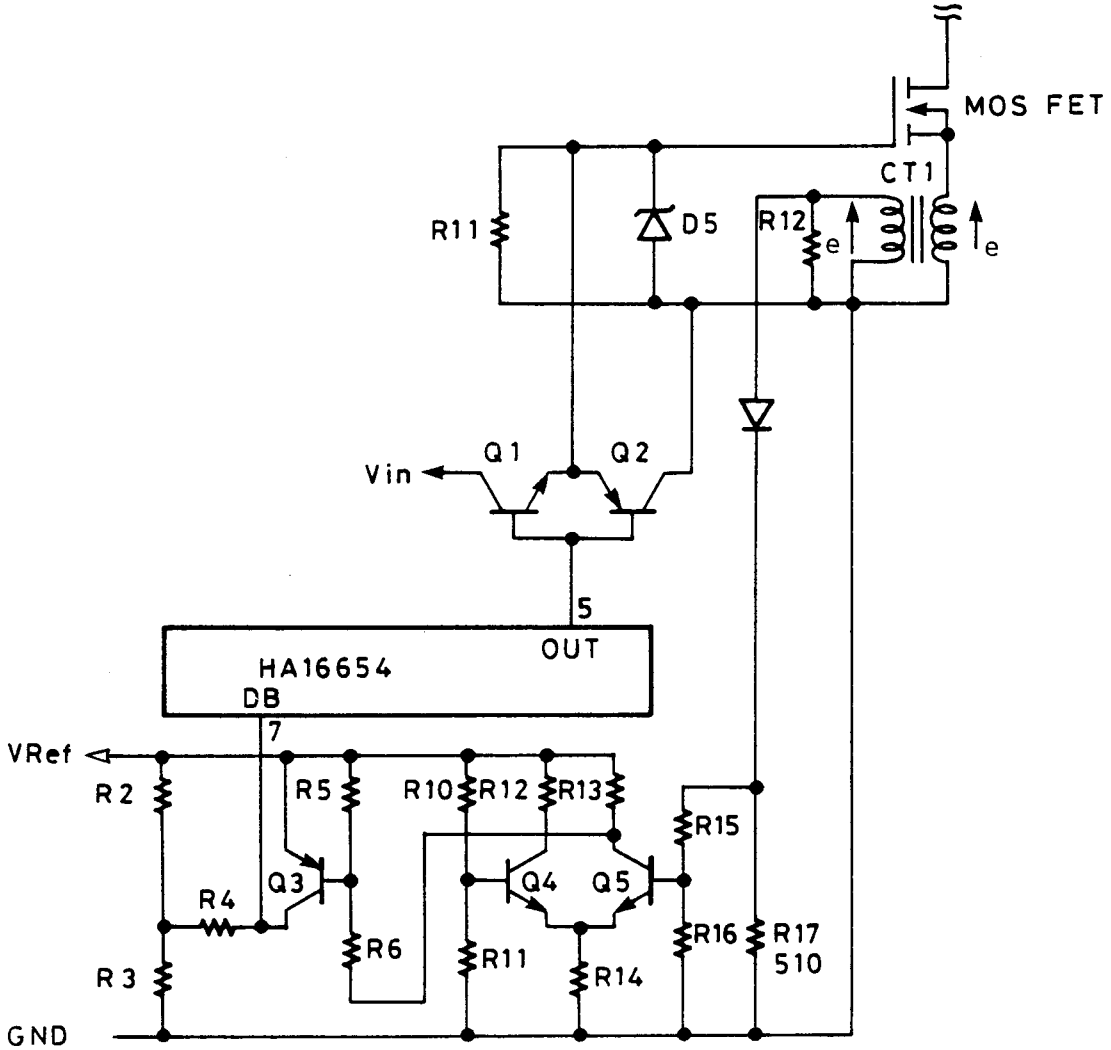


FIGURE 2-2-4. OVERCURRENT PREVENTION CIRCUIT I

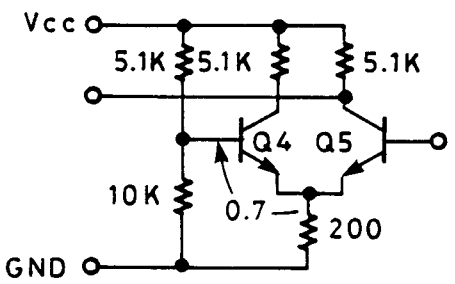


FIGURE 2-2-5. OVERCURRENT PREVENTION CIRCUIT II

1) If the current flowing in the MOS-FET increases, the induced voltage (e2) increases.

2) If the voltage which is distributed at R15 and R16 is higher than the standard voltage at R10 and R11, the Q5 collector current flows.

3) If positive voltage is applied between base and emitter of transistor Q3, then the collector current flows.

4) If the voltage at the DB terminal in the HA16654 increases, and the pulse width is reduced, then the current decreases.

2.2.1.3 Inrush Current Prevention Circuit

The inrush prevention circuit protects diode bridge DB1 and subsequent components from being damaged by excessive current flow in C12 and C13 at power-up. R3 limits the current to RC1 when power is applied; when the switching oscillator operates normally, voltage from T1 activates TRIAC CR1, permitting current flow to RC1.

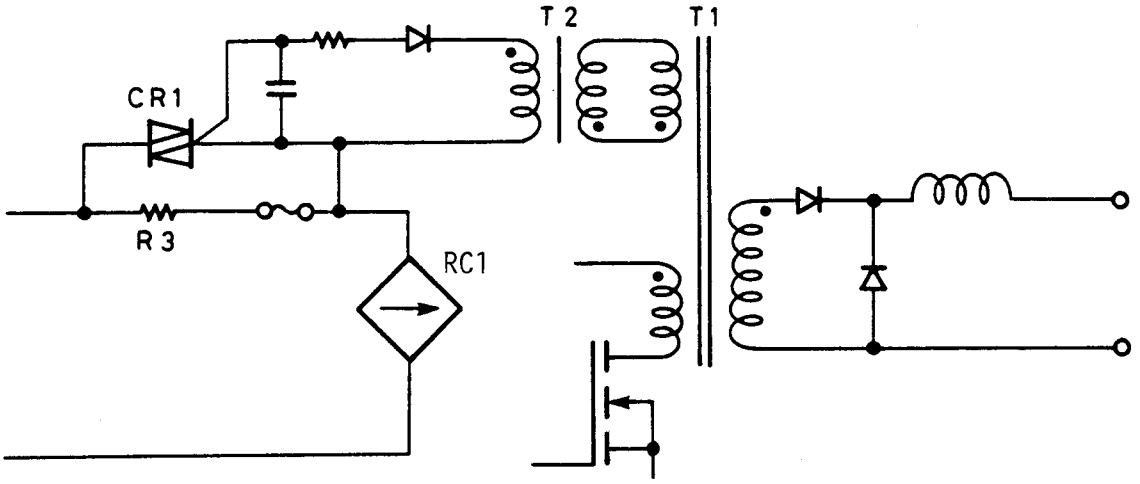


FIGURE 2-2-6. INRUSH CURRENT PREVENTION CIRCUIT

(Reference)

Resistor R5 and R6 have two following functions :

1) To be equal the voltage of the resistor R5 in C12 to that of the resistor R6 in C13.
2) To use up the electric charge as soon as the switch is turned off.

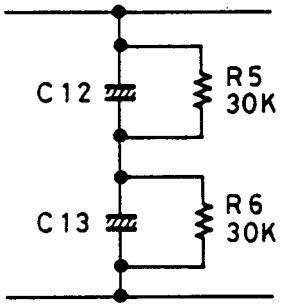


FIGURE 2-2-7. FUNCTIONS OF RESISTOR R5 AND R6

2.2.2 Secondary circuit

2.2.2.1 -5V and -12V Circuit

When an electromotive force which is in the direction of 1 is produced in the transformer T1, the series voltage regulator Z1 and Z2 are supplied with the power reference through RC2 and L4.

When an electromotive force which is in the direction of 2 was produced at the transformer T1, the power reference is supplied from L4.

* R17 is for capacitor discharge.
* D14 and D13 is for series voltage regulator protection.

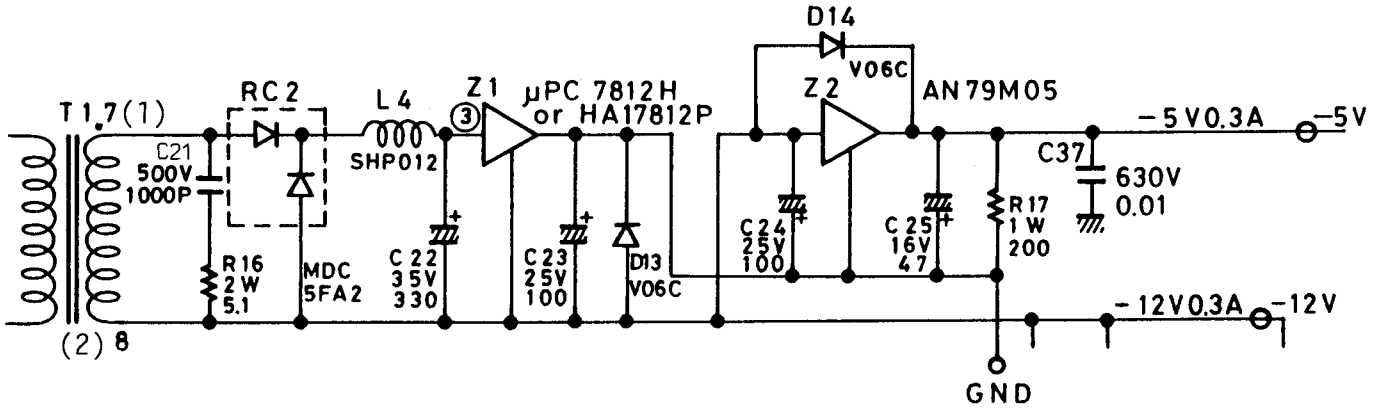


FIGURE 2-2-8. -5V AND -12V SUPPLY CIRCUIT

2.2.2.2 +12V Supply Circuit

a) Basic Circuit

+12V supply circuit is shown in Figure 2-2-9. The function of the +12V supply circuit is same as the -5V supply circuit and -12V supply circuit.

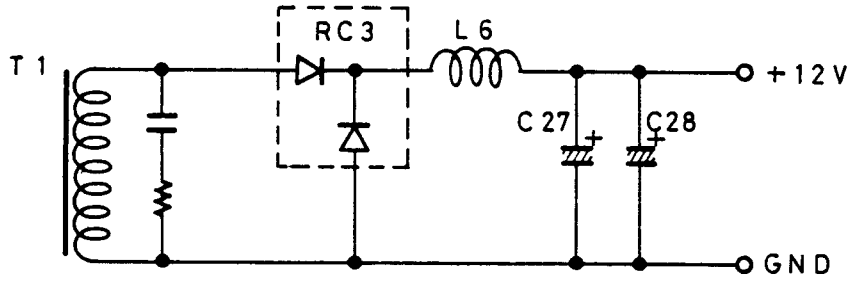


FIGURE 2-2-9. +12V SUPPLY CIRCUIT

b) Voltage stabilization circuit

b)-1. Basic Function

When a control signal is high level, an electric power through the transformer L5 is decreased. This function control the 12 volts voltage.

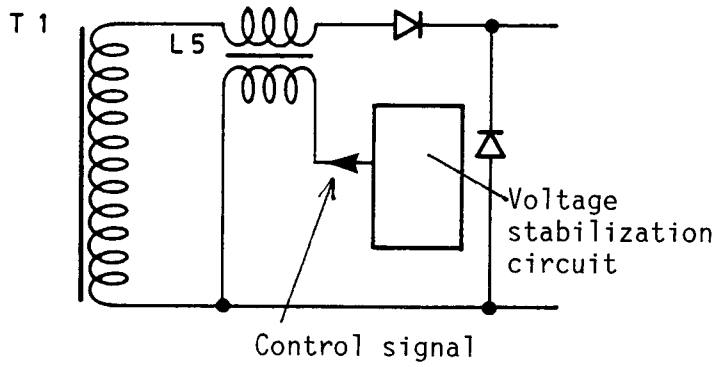


FIGURE 2-2-10. +12V STABILIZATION CIRCUIT

b)-2. Voltage Stabilization Circuit

The Z3 is designed so that when the voltage of reference terminal reaches fixed level, a current flows from cathode to anode.
This function is described in figure 2-2-11.

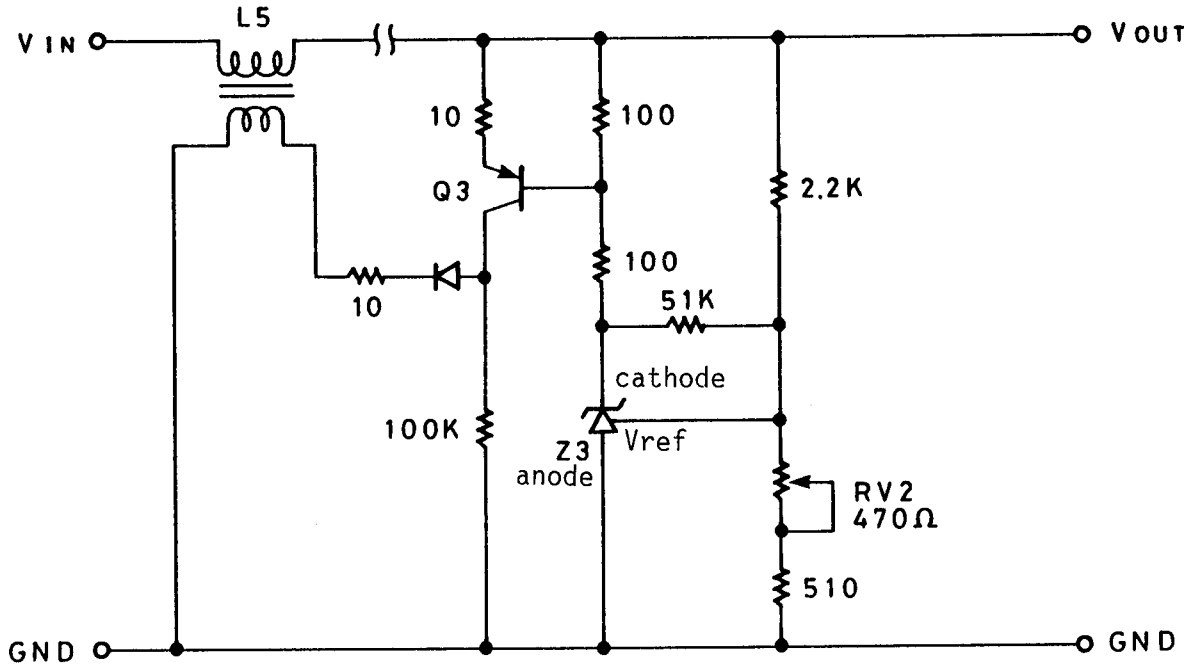


FIGURE 2-2-11. VOLTAGE STABILIZATION CIRCUIT II

If the Vout voltage rises, the Vref voltage rises and then the cathode current increases. After that the Q3 collector current increases, and the Vout voltage decreases ---- Function 1
If the Vout voltage decrease, the Vref voltage decreases and the cathode current decreases. After that the Q3 collector current decreases and the Vout voltage rises ---- Function 2

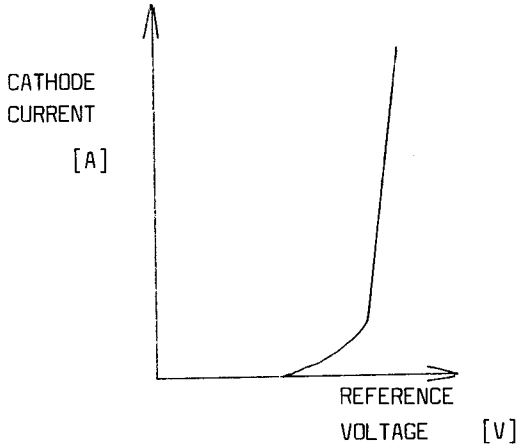


FIGURE 2-2-12. CHARACTERIZE OF Z3

A voltage stabilization circuit repeats the above functions and stabilizes the 12V line.

If a stable Vout voltage is lower than +12 volts, let down a RV2 resistor value. If let down a resistor value, the Vref voltage decreases and the cathode current decreases. After that, the Q3 collector current decreases and the Vout voltage rises.

In the same way, if a stable Vout voltage is higher than +12 volts, let up the resistor value of volume RV2.

c) Fan Revolution Speed Control Circuit

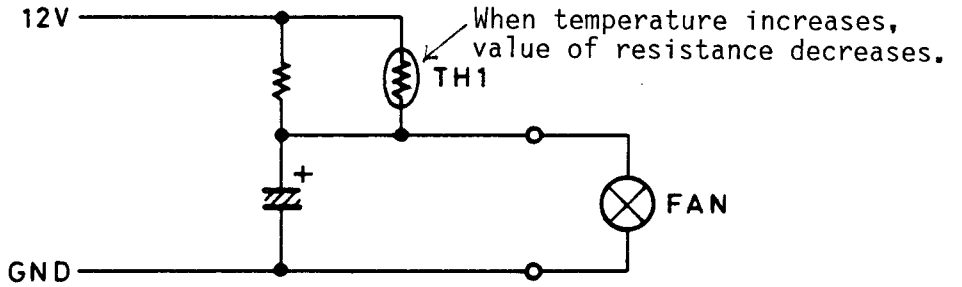


FIGURE 2-2-13. FAN REVOLUTION SPEED CONTROL CIRCUIT

d) Overcurrent Prevention Circuit

If a current is supplied more than a fixed current to +12V circuit, operational amplifier outputs high level signal and a transistor is turned on. Next, the DB terminal voltage rises, and it causes the voltage of the output terminal of the HA16654 not to output a pulse. When the overcurrent prevention comes to such a condition, SCR of PC1 keeps working. To return to the former condition, turn ON the power switch, then OFF after thirty seconds.

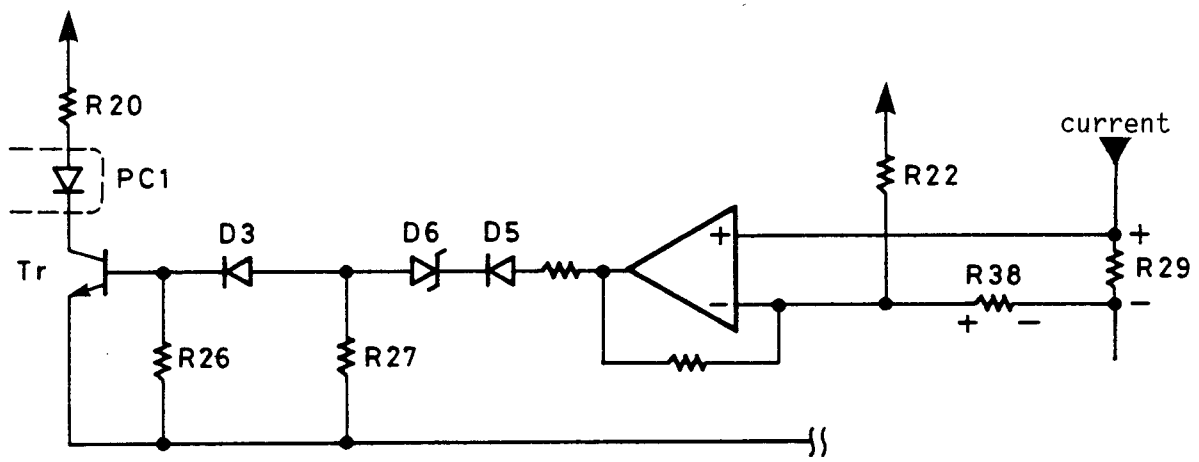


FIGURE 2-2-14. OVERCURRENT PREVENTION CIRCUIT

2.2.2.3 +5V Supply Circuit

a) Basic Circuit

The +5V circuit is shown in Figure 2-2-15.
The function of the +5 volts circuit is same as -5V circuit and -12V circuit.

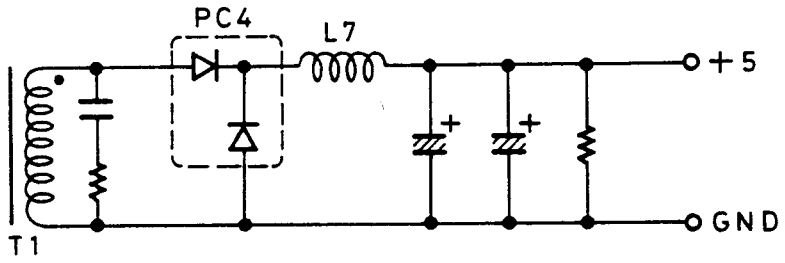


FIGURE 2-2-15. +5V SUPPLY CIRCUIT

b) Voltage Stability Circuit

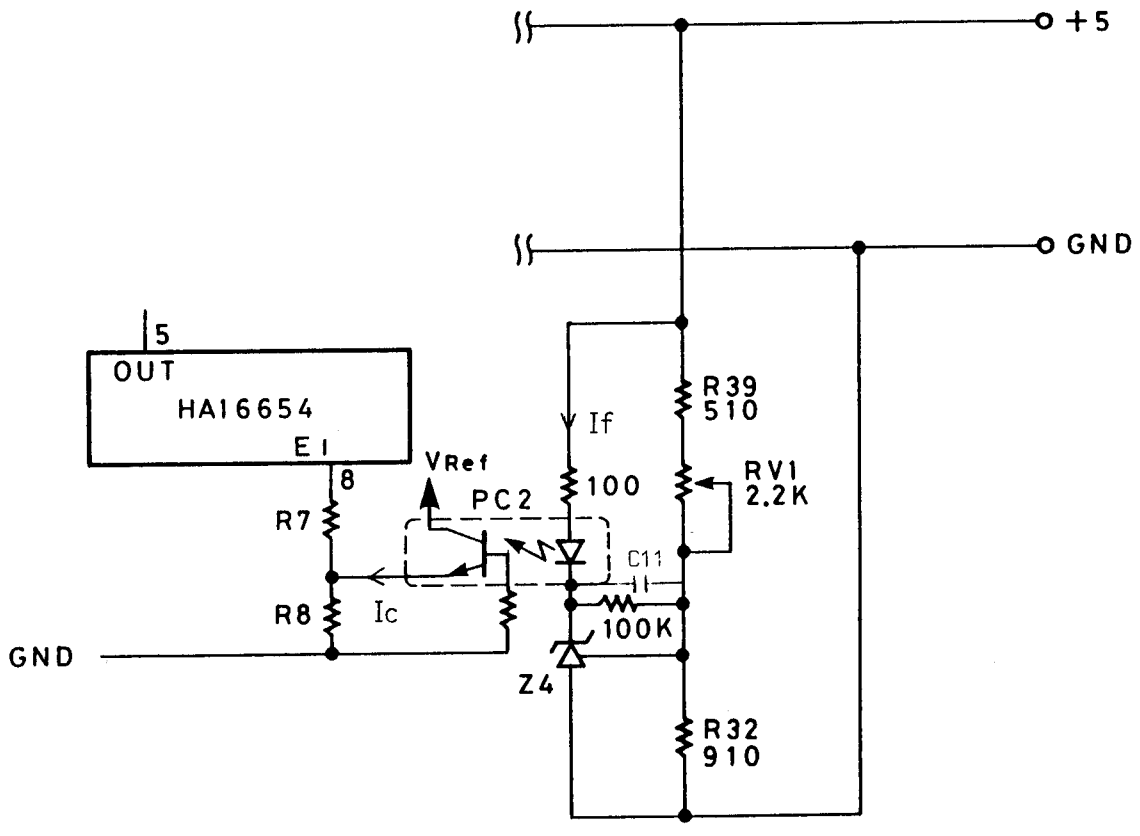


FIGURE 2-2-16. +5V VOLTAGE STABILITY CIRCUIT

Characteristics of Photo Coupler PC2

In the photo coupler, the output current (IC) increases in proportion to the current flowing in the LED (IF).

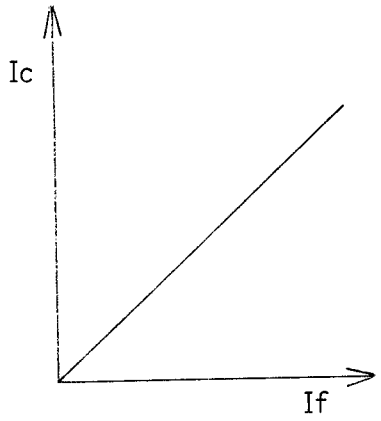


FIGURE 2-2-17. OUTPUT CURRENT OF PHOTOCOUPLER

Characteristics of HA16654

The 8th-pin error input terminal and the 5th-pin output terminal of the HA16654 have the following relation.

* If the voltage of ERROR INPUT terminal rise, the pulse width of the output terminal is reduced.

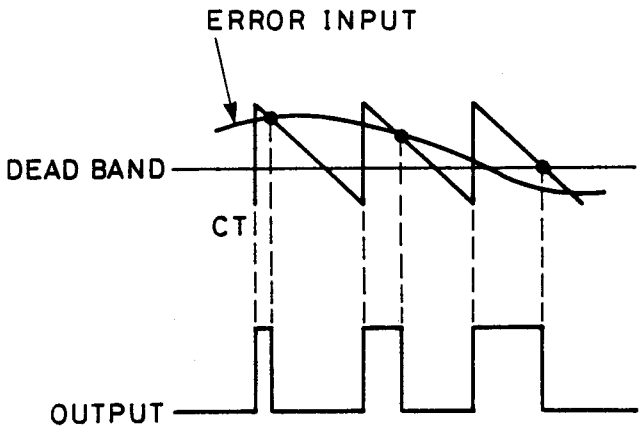


FIGURE 2-2-18. OUTPUT SIGNAL WAVEFORM

Characteristics of Z4

When the reference voltage of the ICZ4 reaches a fixed voltage, current flows from cathode to anode shown in Figure 2-2-17.

Description of circuit

The voltage stabilization circuit of the +5V supply circuit utilizes above three elements.
The vicinity of fixed voltage is applied to the reference terminal. As the voltage of +5V line increases, current flows in Z4 increases, and then the 8th-pin terminal voltage of the HA16654 increases. Then a pulse width of the output terminal is reduced and a output voltage of the secondary oscillation circuit decreases.
If the voltage of +5V line decrease, the voltage of the error input terminal of the HA16654 decreases and a pulse width of the output terminal widen. Therefore the output voltage of the secondary oscillation circuit increases.

If the voltage of the stable +5 volts line is lower than +5 volts, enlarge the resistor value of volume RV1. Then the terminal voltage of R32 decreases and the current flowing in Z4 decreases. The voltage of the ERROR INPUT terminal of the HA16654 decreases and it causes the pulse width of the output terminal to widen and the +5V line voltage to increase.

When a voltage of the stable +5 volts line is higher than +5 volts, let down the resistor value of the volumn RV1 because of the same reason as above.

* The base resistor of the photo coupler is for gaining the switching speed.

c) Overcurrent Prevention Circuit

Function of the overcurrent prevention circuit is same as +12V supply circuit.

d) Overvoltage Prevention Circuit

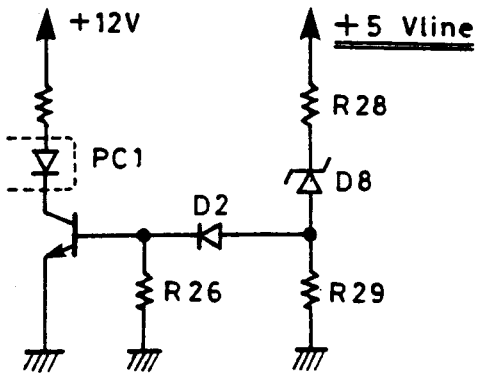


FIGURE 2-2-19. OVERVOLTAGE PREVENTION CIRCUIT

2.2.2.4 Overheating Prevention Circuit

When the temperature rises to a fixed level, switch TH2 is turned on. With switch TH2 turned on switch TH2, a comparator generates a high level signal and it results in no pulse output of the output terminal of the HA166654.

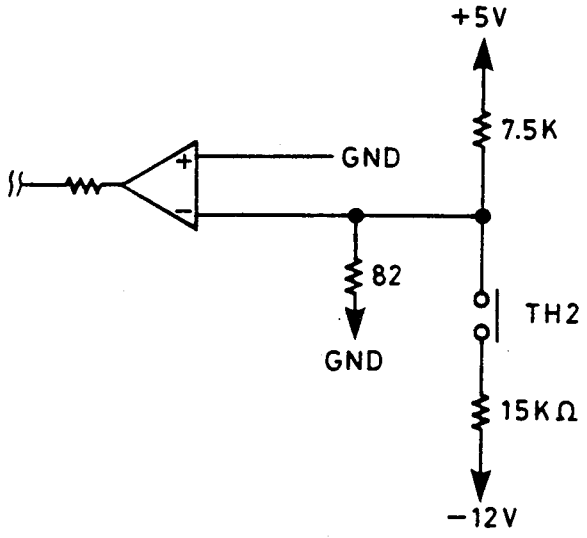


FIGURE 2-2-20. OVERHEATING PREVENTION CIRCUIT

2.2.2.5 Power Good Signal Generation Circuit

The power good signal generation circuit monitors the +5V line, +12V line,-12V line and -5V line of the secondary oscillation circuit.
If there is an abnormality (low voltage) in these lines, the power good signal changes to low level signal.
Also, it monitors a primary voltage proportion circuit. If there is an abnormality (low voltage) in the input AC adapter, power good signal changes to low level signal.

The primary voltage proportion circuit is equipped with the CR circuit. The CR circuit controls timing of the power good signal.

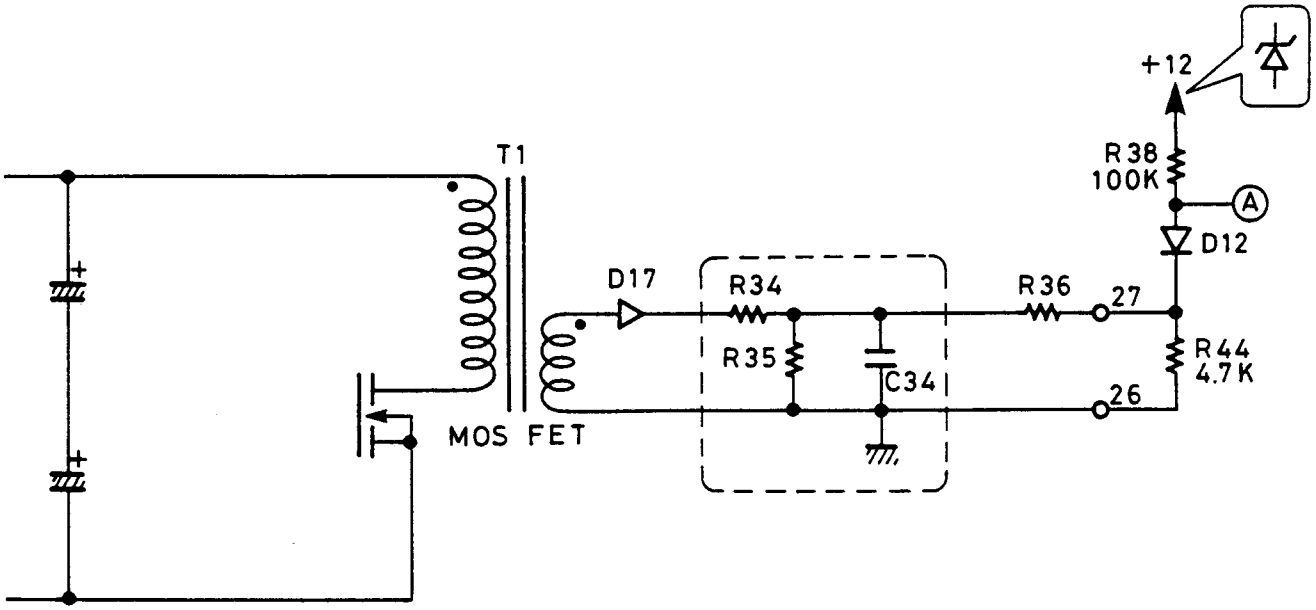


FIGURE 2-2-21. POWER GOOD SIGNAL GENERATION CIRCUIT I
(Primary voltage proportion circuit)

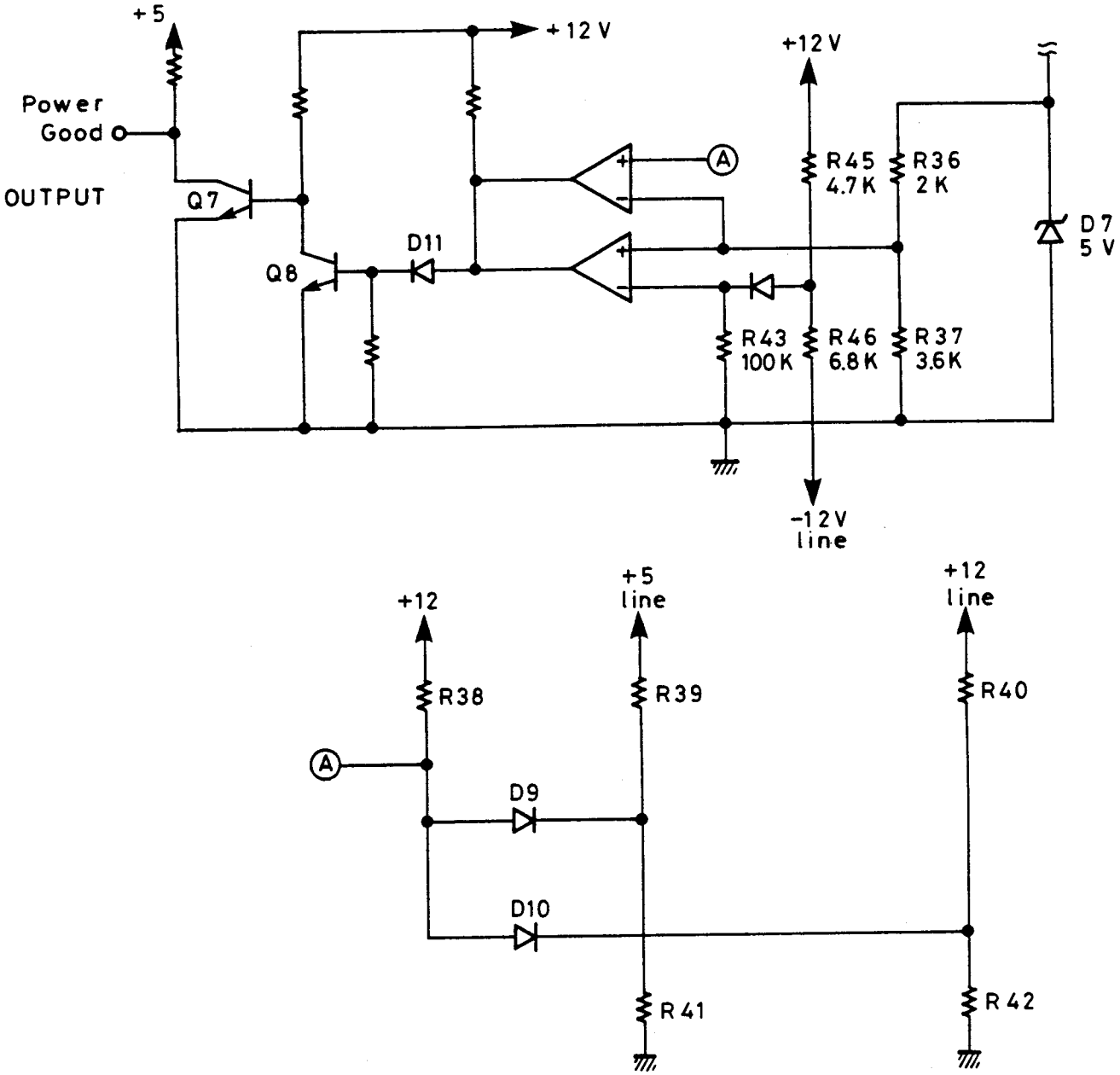


FIGURE 2-2-22. POWER GOOD SIGNAL GENERATION CIRCUIT II

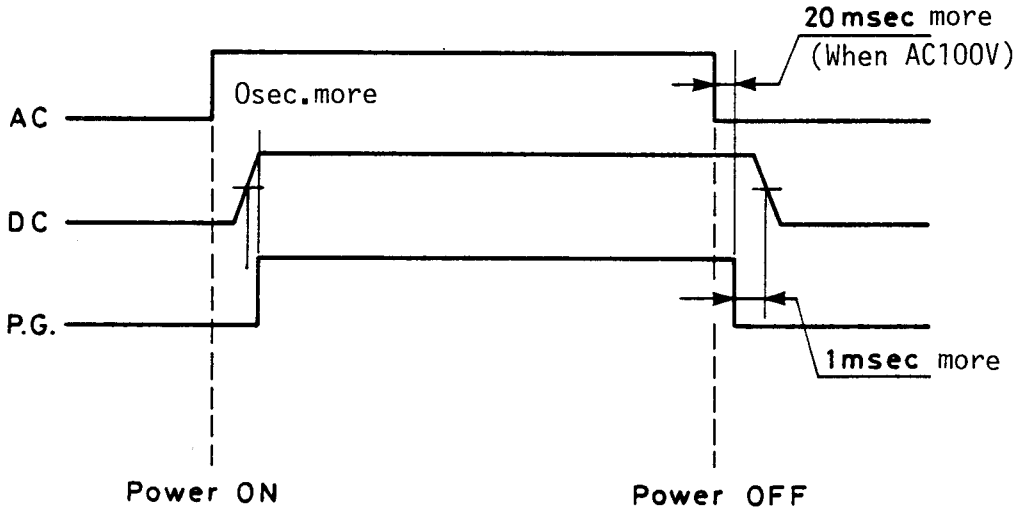


FIGURE 2-2-23. TIMING CHART OF POWER GOOD SIGNAL

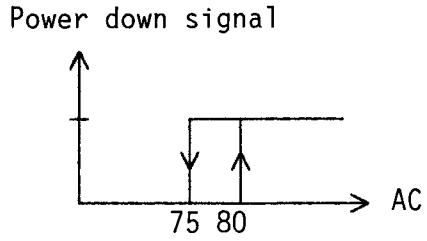
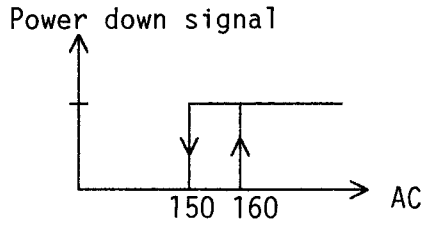
TABLE 2-2-1. FUNCTION OF PREVENTION CIRCUIT

		Detecting voltage or Detecting current	Condition after detecting
Overvoltage detector	+ 5V +12V -12V - 5V	5.5 volts - 7.0 volts	Cut all output off. To recuperate condition, turn off AC, then on after 30 seconds.
Overcurrent prevention circuit	+ 5V +12V -12V - 5V	35A 16A 3A 3A	Cut all output off. To recuperate condition, turn off AC, then on after 30 seconds.

TABLE 2-2-2 SPECIFICATION OF DC MAX CURRENT

	+5V	+12V	-12V	-5V
Output current Max (Min)	20A (2.5A)	4.8A * (0A) * 7A within 10 seconds after power on.	0.3A (0A)	0.3A (0A)
Current consumption				
ANTA BOARD	1.23A (effective value)	0A		
ANT-RM BOARD	0.50A (effective value)	0A		
SPFG BOARD	0.54A (effective value)	0A		
WHDC BOARD	0.53A (effective value)	0A		
MRS-MO BOARD	0.27A (effective value)	0A		
MRS-CR BOARD	0.50A (effective value)	-		
FD1155C	0.46A	0.21A (TYP) 0.39A (power on)		
MD5501	0.11A (TYP)	0.24A (TYP) 1.66A (peak)		
HMD-720	0.2A (TYP)	2.0A (power on) 0.58A (TYP)		
D5146 (40M HDD)	1.0A (MAX)	3.0A (power on) 2.0A (seek) 1.2A (read/write)		

TABLE 2-2-3. POWER DOWN SIGNAL SPECIFICATION

115V MODE	75V	
230V MODE	150V	

2.3 ANTA MAIN CONTROL BOARD OPERATIONS

This section describes the principles of the ANTA board operation by using the diagrams which shows an internal circuit of the EQUITY III+/ EPSON PC AX computer system. There are several blocks in the diagram for each circuit operations.

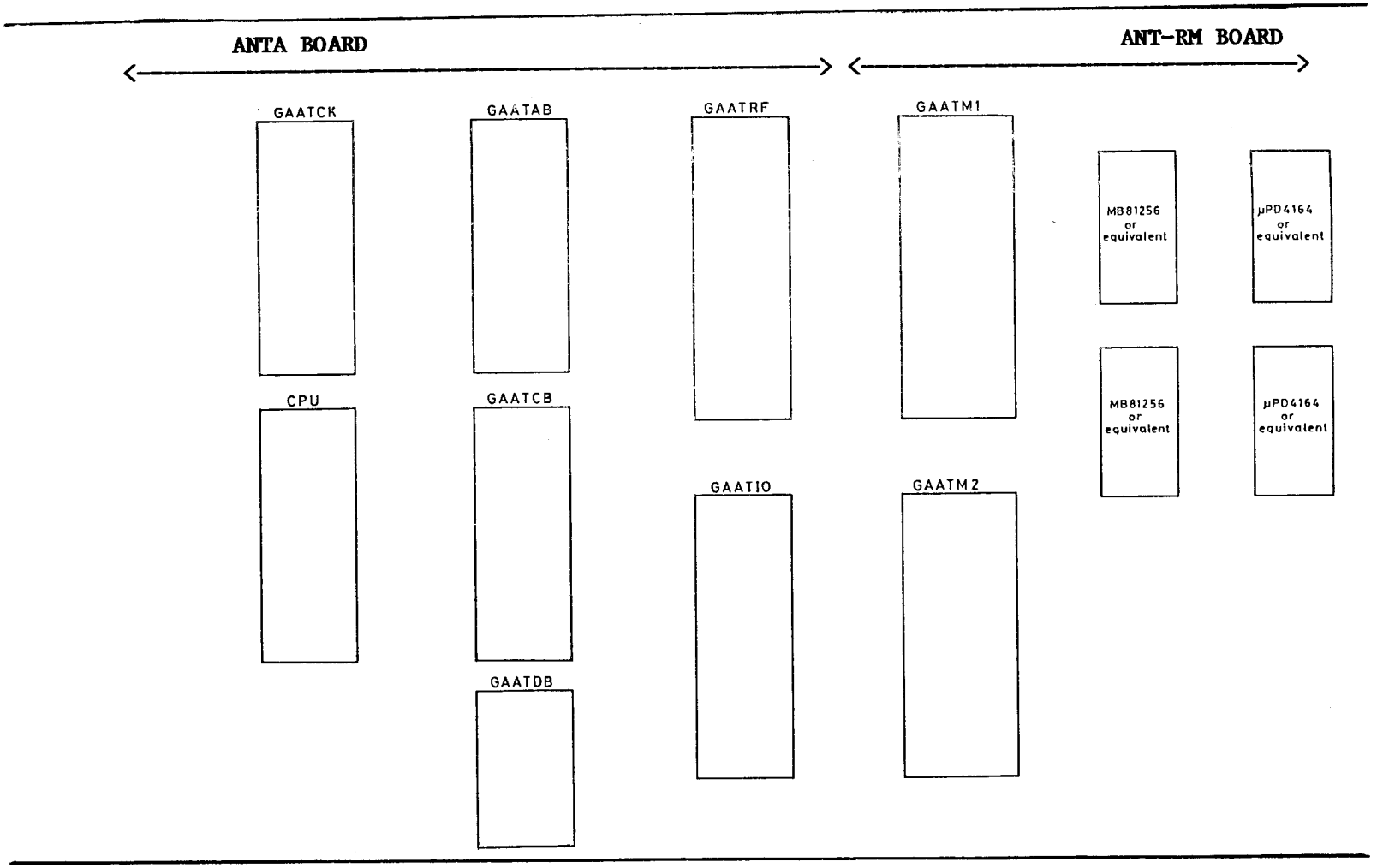


FIGURE 2-3-1. INTERNAL CIRCUIT CONFIGURATION

Table 2-3-1 shows the memory map for the EQUITY III+/EPSON PC AX computer system.

TABLE 2-3-1. MEMORY MAP

ADDRESS	NAME	FUNCTION
000000 to 09FFFF	640 KB system memory	System memory
0A0000 to 0BFFFF	128 KB video RAM	Reserved for graphics display buffer.
0C0000 to 0DFFFF	128 KB I/O EXPANSION ROM	Reserved for ROM on I/O adapters.
0E0000 to 0EFFFF	64 KB reserved on system	Duplicated code assignment at address FE0000.
0F0000 to 0FFFFF	64 KB ROM on system board	Duplicated code assignment at address FF0000.
100000 to FDFFFF	Maximum memory 15 MB	I/O channel memory - memory expansion option.
FE0000 to FEFFFF	64 KB reserved on system	Duplicated code assignment at address 0E0000.
FF0000 to FFFFFF	64 KB ROM on system board	Duplicated code assignment at address 0F0000.

2.3.1 System Clock Generation Circuit

All clock signals are supplied from the gate array (GAATCK) except the RTC (146818) clock signal. The GAATCK generates the following clocks.

1) CPU clock (12 MHz, 16MHz, 20MHz)
2) NPX clock (8MHz)
3) DMA clock (3MHz, 4MHz, 5MHz)
4) Timer counter clock (1.19MHz)
5) Keyboard controller clock (6MHz)
6) OSC clock (for option slot: 14.31818MHz)
7) SCLK signal (System clock for option slot: 6MHz, 8MHz, 10MHz)

< REMARK >

Please be careful with difference between 'clock speed' and 'operation speed'. The CPU and the NPX divide an input clock signal by one's internal circuit. (NPX does not divide the input clock signal in 8MHz mode. Please refer to Section 2-2-3.) This means there are some cases that the input clock speed is not identical with the operation speed. This manual defines these words as below.

Clock speed -------- Input or output clock signal speed
Operation speed ---- Internal clock speed

2.3.1.1 Select CPU Operation Speed

The EQUITY III+/EPSON PC AX has three kinds of CPU operation speeds. One is 6MHz, the same as IBM AT, 8MHz is the same as IBM NEW AT, and 10MHz is faster operation speed than IBM AT or NEW AT.
We can select these CPU operation speeds by slide switch (SW2). Also, the GAATCK includes clock speed select circuit.

2.3.1.2 LED Indications

There are two LEDs on the clock speed change circuit. These LEDs indicate the CPU

operation speed.

TABLE 2-3-2. LED INDICATIONS

LED INDICATIONS	CPU OPERATION SPEED
RED	6MHz
ORANGE	8MHz
GREEN	10MHz

< REMARK >

Jumper connector J1 is inhibitted to change setting. (Always connect between A to C)

2.3.1.3 Select NPX (80287) Operation Speed

The EQUITY III+/ EPSON PC AX has two kinds of NPX operation speed modes.

TABLE 2-3-3. NPX OPERATION SPEED

NPX OPERATION SPEED MODES		OPERATION SPEED
	(CPU OPERATION SPEED)	
1) CPU CLOCK MODE	(6MHz)	4MHz
	(8MHz)	5.3MHz
	(10MHz)	6.7MHz
2) 8MHz MODE	(6MHz,8MHz,10MHz)	8MHz

A selection is performed by setting of jumper connector J1 and J2 on the ANTA board (Main circuit board). Jumper connector setting of J1 and J2 are listed in CHAPTER 7.

< REMARK >

NPX divides the CPU clock into three in the CPU clock mode.
In CPU CLOCK MODE, the NPX divides the CPU clock into three. But 8MHz mode, the NPX does not divide 8MHz clock.

2.3.1.4 Oscillator

There are three oscillators on the ANTA board. The GAATCK inputs these signals and produces the following clock signals.

TABLE 2-3-4. OSCILLATOR CLOCK SIGNAL FLOW

OSC CLOCK SPEED	GAATCK DIVIDE THE CLOCK INTO;	GAATCK OUTPUTS;	CONNECT TO; (MAJOR CHIP)
48MHz	1/3	16MHz	CPU
	1/4	12MHz	CPU
	1/6	8MHz	NPX
	1/8	6MHz	KEYBOARD CONTROLLER
20MHz	1/1	20MHz	CPU
14.31818MHz	1/1	14.31818MHz	OPTION SLOT
	1/12	1.19MHz	TIMER COUNTER

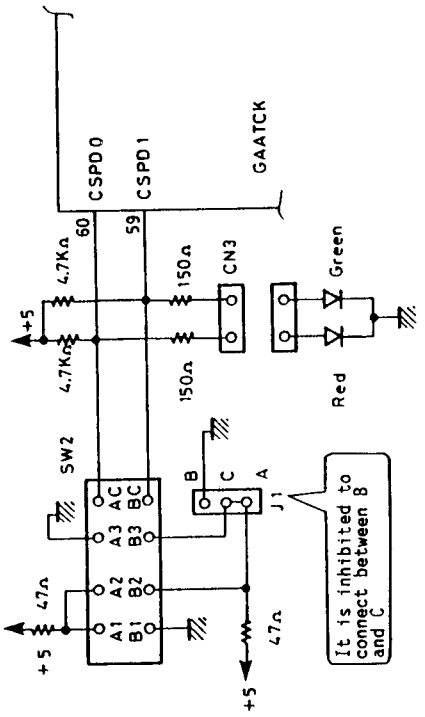


FIGURE 2-3-3. CLOCK SPEED CHANGE CIRCUIT

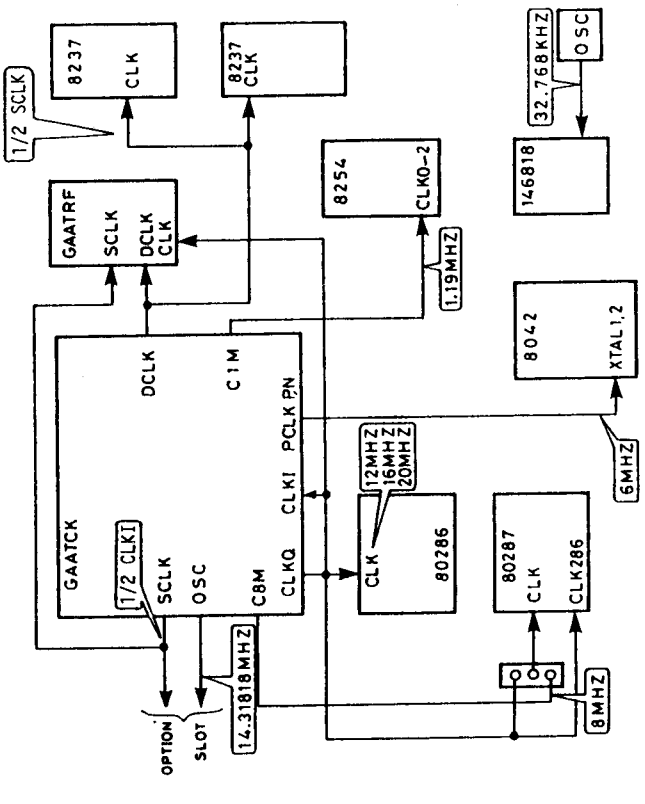


FIGURE 2-3-2. SYSTEM CLOCK SUPPLY CIRCUIT

2.3.2 System Reset Signal Generator Circuit

There are three kinds of reset signal on the EQUITY III+/EPSON PC AX computer system below. The gate array GAATCK generates these signals.

1) CPU RESET SIGNAL
2) INTERNAL CIRCUIT RESET SIGNAL
3) OPTION SLOT RESET SIGNAL

To generate the above reset signals, there are the following methods.

TABLE 2-3-5. RESET SIGNAL GENERATION METHODS

RESET SIGNAL	METHODS
CPU RESET SIGNAL	1) PWGD signal goes low. 2) Reset switch is pushed. 3) RC signal goes active.(Software reset) 4) Shut down cycle is executed.
INTERNAL CIRCUIT RESET SIGNAL	Reset switch is pushed.
OPTION SLOT REST SIGNAL	Reset switch is pushed.

< REMARK >

The software reset command (RC goes active) resets only the CPU.
When gate array GAATCK receives the RC signal, it generates the RSCPU signal.

2.3.2.1 System Reset Circuit

1) PWGD signal
The power supply unit (ATRPS unit) generates a signal. When the power supply unit has some problems, the PWGD signal becomes low. Normally, this signal keeps high level.
When the gate array GAATCK receives the PWGD signal, it generates a RSN signal, a RSDN signal and a RSCPU signal.

2) Reset switch (SW3)
When the reset switch SW3 is pushed, the GAATCK generates a RSN signal, a RSDN signal and a RSCPU signal. This computer system can disable the reset switch signal by locking the key cylinder on the front panel. When the key cylinder is locked, the key cylinder switch becomes on. When the key cylinder switch is on, the GAATCK does not output any reset signals.

3) RC signal
A RC signal is sent from P20 pin of the keyboard controller (8042) which can be controlled by software.
A RSCPU signal becomes active by the active RC signal.
(Refer to the remark in section 2-4.)

4) Shut down cycle
A Shut down cycle is a kind of CPU execution cycle. When the CPU executes this cycle, it means that the CPU detects a fatal software error with which the CPU can not continue its current operation. CPU indicates this cycle with SO, S1, M/IO, COD/INTA signals.
The shut down circuit of the GAATCK is searching for the shut down cycle whenever power is on and if it detects the shut down cycle, it generates an active RSCPU signal.

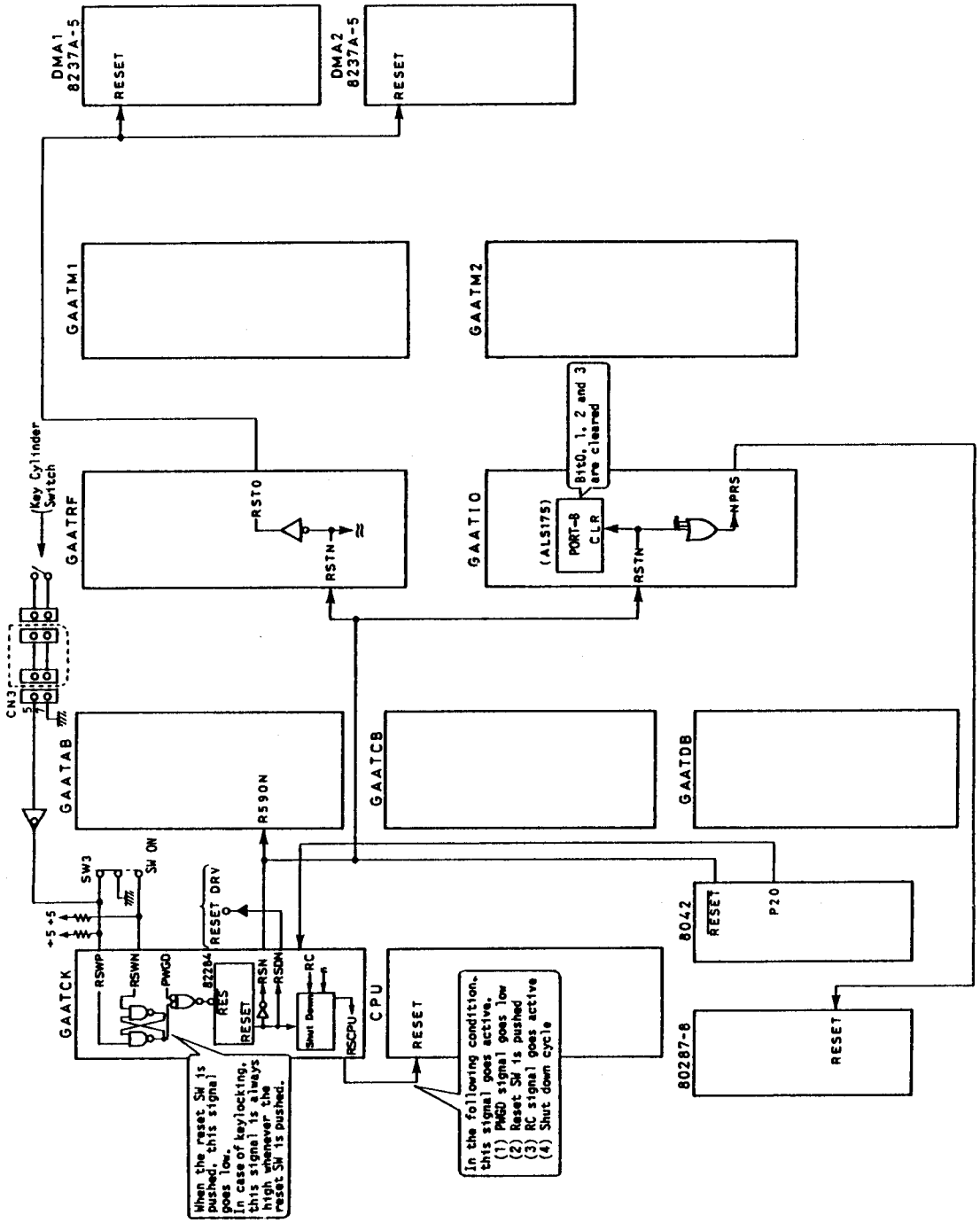


FIGURE 2-3-4. SYSTEM RESET CIRCUIT

2.3.3 Internal Memory Control Circuit

All system memory chips are integrated on the ANT-RM board. If the EQUITY III+/EPSON PC AX computer system has problem that system does not boot up, you should better to replace the ANT-RM board first because you can determine if the problem is caused by RAM chips or the other circuit.

2.3.3.1 RAM Chip type

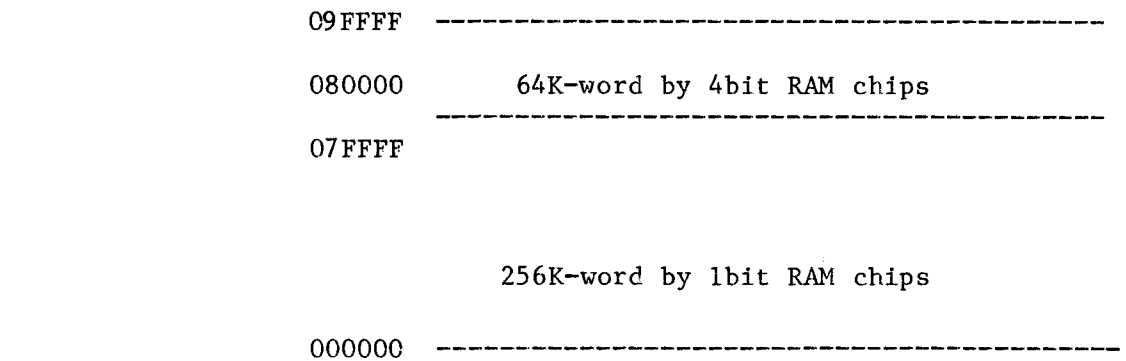
On the ANT-RM board, there are three kinds of RAM chips. (Refer to Table 2-3-6)

TABLE 2-3-6. FUNCTION OF RAM CHIPS

RAM CHIP TYPE	Q'TY	FUNCTION
256K-word by 1bit	16	System memory (512KB)
64K-word by 4bit	4	System memory (128KB)
256K-word by 1bit	2	Parity check
64K-word by 1bit	2	Parity check

2.3.3.2. RAM Chip addresses

The system memory RAM chips are located in the following address.



RAM CHIP ADDRESSES OF SYSTEM MEMORY

2.3.3.3 Jumper Connector Function

We can disable the system memory by setting of the jumper connectors J1,J2 and J3.

TABLE 2-3-7. JUMPER CONNECTOR FUNCTION

J3	J1	J2	DESCRIPTION
A-C	A-C	A-C	AVAILABLE AREA : 09FFFF TO 000000 (640KB)
	B-C	A-C	AVAILABLE AREA : 07FFFF TO 000000 (512KB)
	B-C	B-C	AVAILABLE AREA : 03FFFF TO 000000 (256KB)
B-C	---	---	AVAILABLE AREA : NONE (0KB)

2.3.3.4 Operations of Memory Control Circuit

1) ADDRESS SIGNAL

The CPU outputs address signal (A0 to A23). Next, the GAATM2 (Memory control gate array 2) receives from A1 signal to A18 signal to make RAM chip address signal. Also, the GAATM1 (Memory control gate array 1) receives from A17 signal to A23 signal and A0 signal to make a RAS signal, a CAS signal and etc.

< REMARK 1 >

The GAATRF controls A20 signal.

< REMARK 2 >

SA0 signal on the GAATAB is not used by memory control circuit in RAM read/ write mode. But it will used in the D-RAM refresh mode.

2) DATA SIGNAL
GAATDB controls data bus by its internal data bus buffer.

3) READ/WRITE CONTROL SIGNAL
CPU outputs S0, S1, M/IO signals. GAATCK receives these signals and makes MEMRN and MEMWN signals. GAATM2 receives MEMR and MEMW signals to control RAS and CAS signals. Also, GAATM2 receives XMWN (MEMWN) signal which has flowed through GAATCB to make WE signal of the RAM chips. GAATM1 receives XMRN (MEMRN) signal which has flowed through GAATCB to make RAS, CAS signals.

4) RAM CHIP CONTROL SIGNALS
All D-RAM control signals are sent from GAATM2.

5) D-RAM REFRESH CONTROL CIRCUIT
Refer to Section 2.3.11.

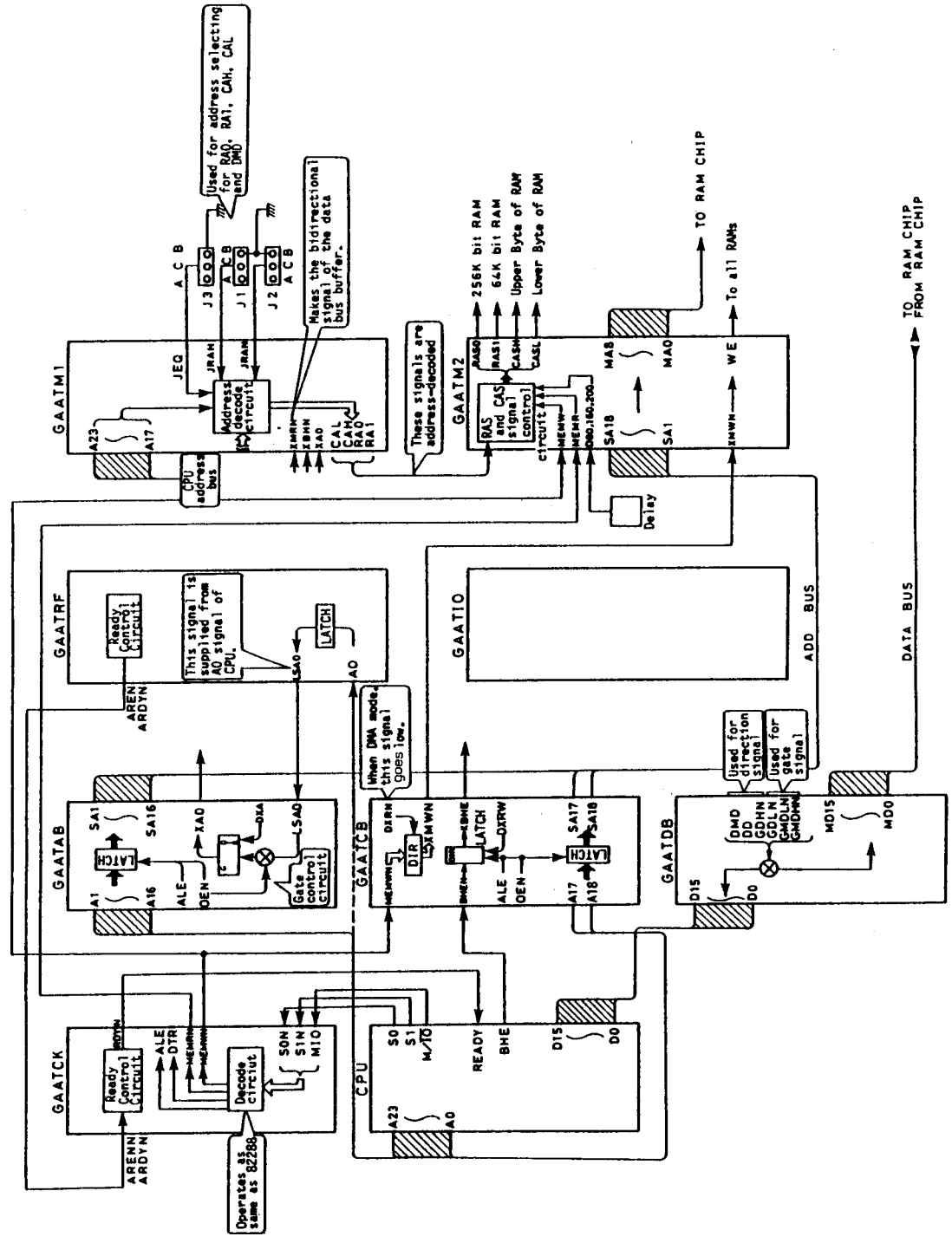


FIGURE 2-3-5. INTERNAL MEMORY CONTROL CIRCUIT

2.3.4 Byte/Word Access & 16-8 Bit Data Conversion

The CPU has the following data access modes.
16-8 bit data conversion means word transmission of even address (8 bit device).

TABLE 2-3-8. CPU DATA ACCESS MODES

NO.	MODE	DATA TRANSMISSION TO;	REFERENCE
1)	BYTE TRANSMISSION OF EVEN ADDRESS	16-BIT DEVICE	Figure 2-3-7
2)	BYTE TRANSMISSION OF ODD ADDRESS	16-BIT DEVICE	Figure 2-3-8
3)	WORD TRANSMISSION OF EVEN ADDRESS	16-BIT DEVICE	Figure 2-3-9
4)	WORD TRANSMISSION OF ODD ADDRESS	16-BIT DEVICE	---
5)	BYTE TRANSMISSION OF EVEN ADDRESS	8-BIT DEVICE	Figure 2-3-10
6)	BYTE TRANSMISSION OF ODD ADDRESS	8-BIT DEVICE	Figure 2-3-11
7)	WORD TRANSMISSION OF EVEN ADDRESS	8-BIT DEVICE	16-8 BIT DATA CONVERSION
8)	WORD TRANSMISSION OF ODD ADDRESS	8-BIT DEVICE	Figure 2-3-12

2.3.4.1 Data Bus Control Signal on GAATDB

The GAATDB includes five 8-bit buffers. This buffer needs a gate control signal and a direction control signal. The following table describes gate control signals and direction signals.

TABLE 2-3-9. FUNCTIONS OF CONTROL SIGNAL ON GAATDB.

SIGNAL NAME	DESCRIPTION
D245, G245	Controls data bus conversion (High byte --> low byte) (Low byte --> High byte)
GMDHN, GMDLN, DMD	Controls Memory data (Disabling, Direction control)
GDHN, GDLN, DD	Controls CPU data (Disabling, Direction control)
CBA, SBA	Controls data latching (With 16-8 bit data conversion)

2.3.4.2 Circuit Operation of Data Conversion

1) BYTE TRANSMISSION OF EVEN ADDRESS (16-BIT DEVICE)
   Figure 2-3-7 shows the GAATDB internal circuit operation.

2) BYTE TRANSMISSION OF ODD ADDRESS (16-BIT DEVICE)
   Figure 2-3-8 shows the GAATDB internal circuit operation.

3) WORD TRANSMISSION OF EVEN ADDRESS (16-BIT DEVICE)
   Figure 2-3-9 shows the GAATDB internal circuit operation.

4) WORD TRANSMISSION OF ODD ADDRESS (16-BIT DEVICE)

   The CPU operatrs as follows. First, the CPU executes the BYTE TRANSMISSION OF ODD ADDRESS (16-BIT DEVICE). Next, the CPU executes the BYTE TRANSMISSION OF EVEN ADDRESS (16-BIT DEVICE). When a software programmer instructs the CPU to do the WORD TRANSMISSION OF ODD ADDRESS (16-BIT DEVICE), the CPU executes the instruction with the above steps automatically.

5) BYTE TRANSMISSION OF EVEN ADDRESS (8-BIT DEVICE)
   Figure 2-3-10 shows the GAATDB internal circuit operation.

6) BYTE TRANSMISSION OF ODD ADDRESS (8-BIT DEVICE)
   Figure 2-3-11 and Figure 2-3-12 show the GAATDB internal circuit operations.
   (Read mode --- Figure 2-3-11, Write mode --- Figure 2-3-12)

7) WORD TRANSMISSION OF EVEN ADDRESS (8-BIT DEVICE) : 16-8 bit data conversion
   Figure 2-3-13 and Figure 2-3-14 show the GAATDB internal circuit operations.
   (Read mode --- Figure 2-3-13, Write mode --- Figure 2-3-14).
   In this section, there are two important signals. One is a COFF signal, the other is a XA0 signal.

COFF SIGNAL
   The GAATRF outputs this signal. The GAATCK receives this signal to make two 8-bit device read/write signals. Also, the GAATDB receives this signal to catch a low byte data by the internal buffer LS646.
   * While the GAATCK receives an active COFF signal, a read/write signal of the GAATCK will be inactive.

LSA0 SIGNAL (XA0 SIGNAL)

The GAATRF outputs this signal. In the 16-8 bit data conversion mode, the GAATRF does not use a CPU A0 signal to make a LSA0 signal. (This means, the internal circuit of the GAATRF generates the LSA0 signal but not in the conversion mode, the GAATRF uses the CPU A0 signal to make LSA0 signal.) The internal buffer LS646 of the GAATDB inputs this signal (XA0 signal) to send the catched data to the CPU. Also, the 8-bit device receive this signal to determine address. While a 16-8 bit data conversion, this signal changes status as low to high.

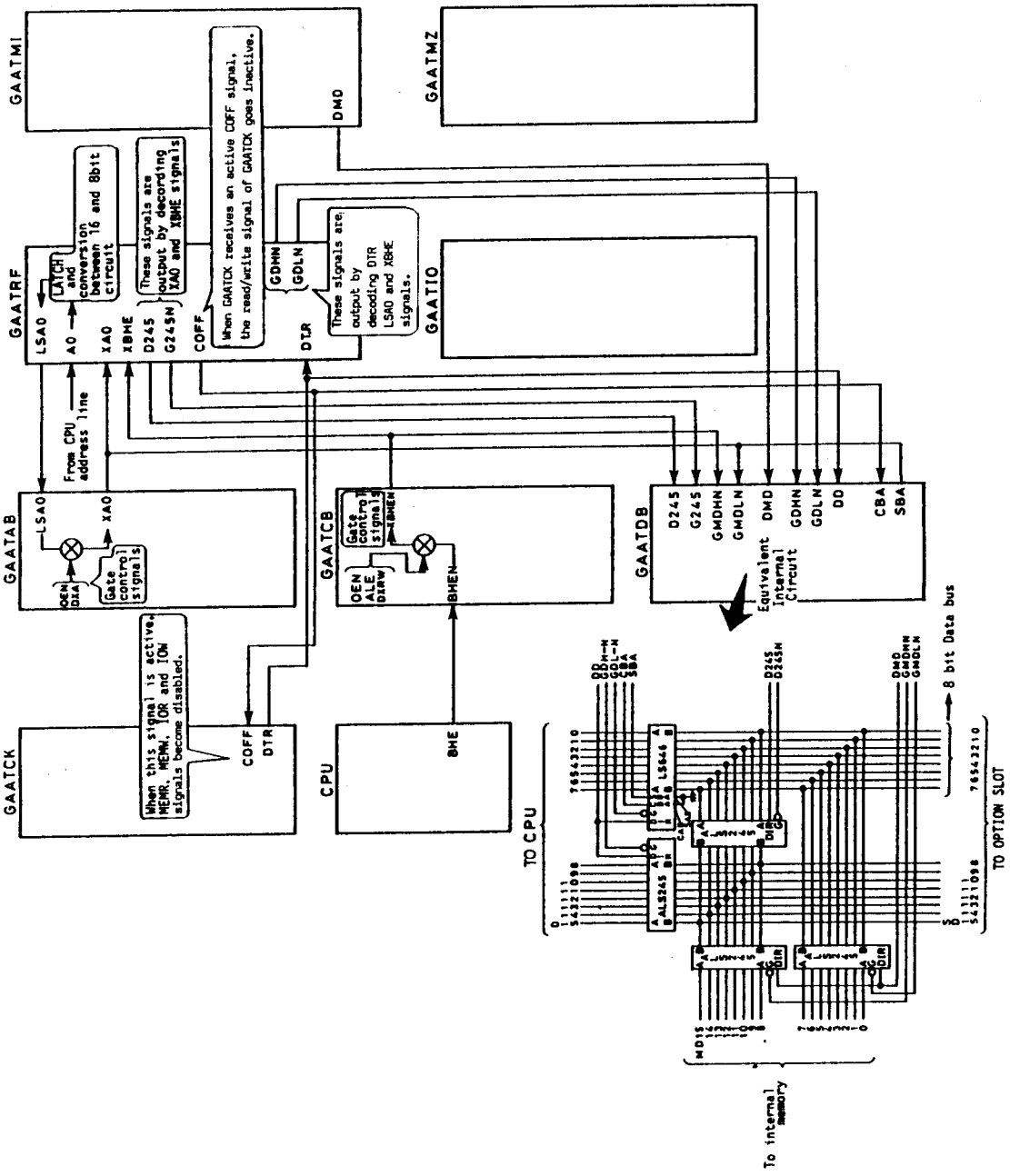


FIGURE 2-3-6. BYTE/WORD ACCESS & 16-8 BIT DATA CONVERSION

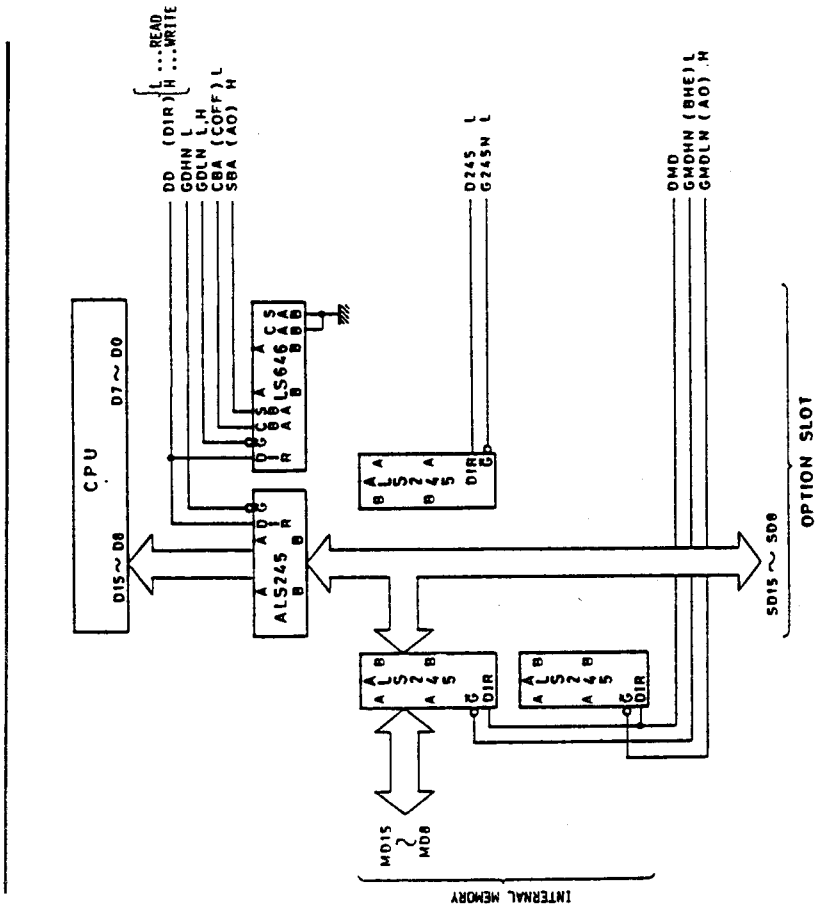


FIGURE 2-3-8. DATA TRANAMISSION TO 16 BIT DEVICE (BYTE TRANSMISSION OF ODD ADDRESS)

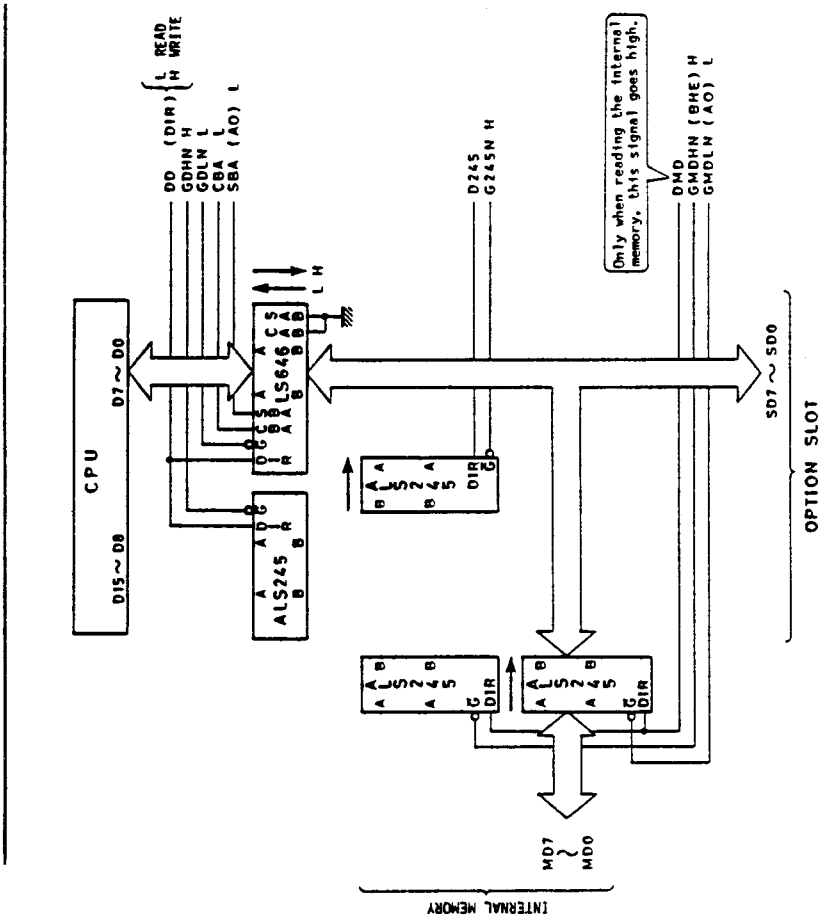


FIGURE 2-3-7. DATA TRANSMISSION TO 16 BIT DEVICE (BYTE TRANSMISSION OF EVEN ADDRESS)

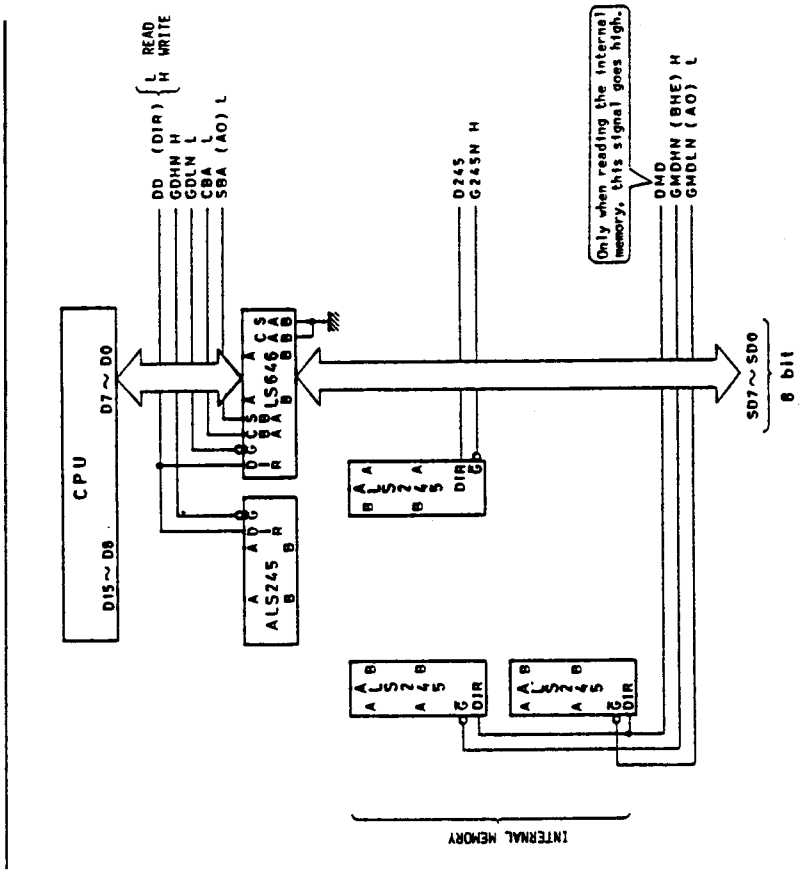


FIGURE 2-3-10. DATA TRANSMISSION TO 8 BIT DEVICE (BYTE TRANSMISSION OF EVEN ADDRESS)

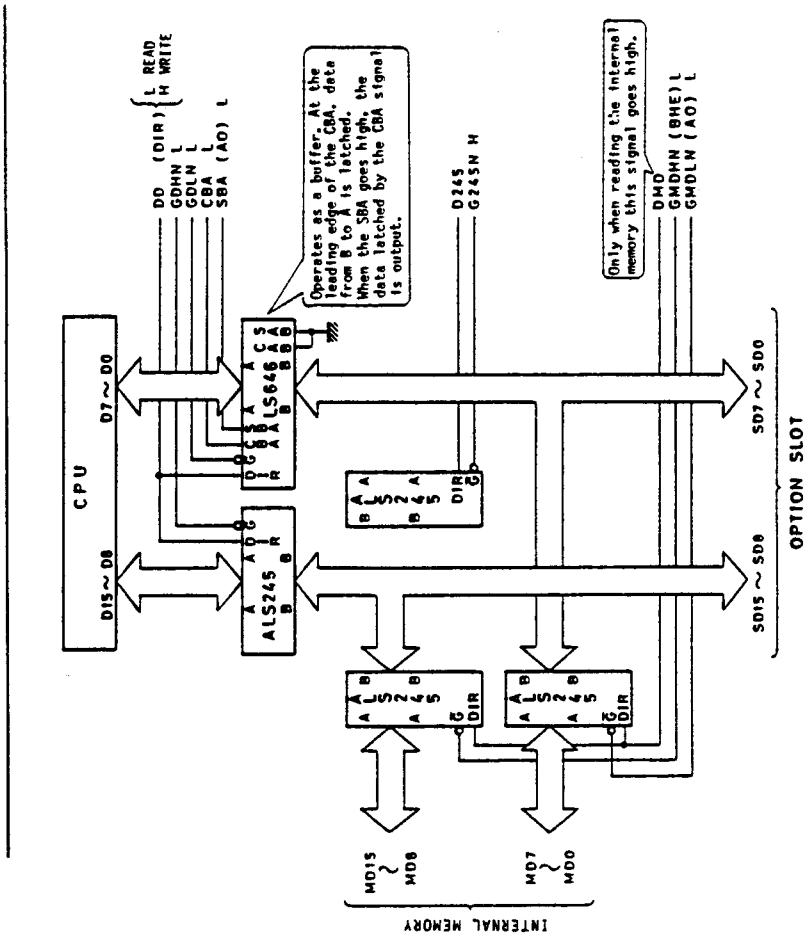


FIGURE 2-3-9. DATA TRANSMISSION TO 16 BIT DEVICE (WORD TRANSMISSION OF EVEN ADDRESS)

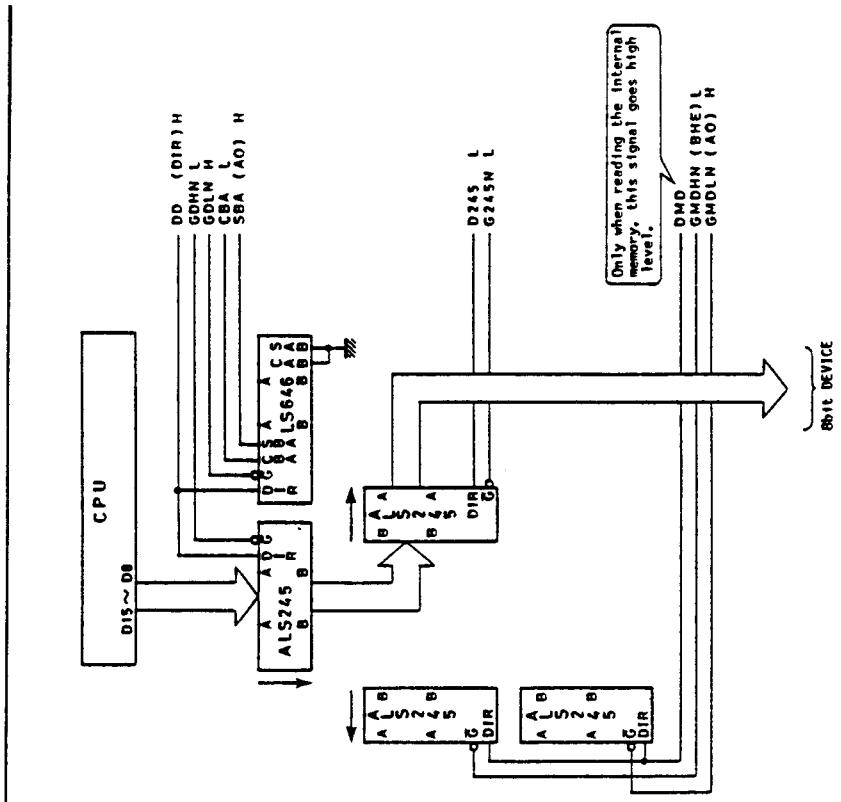


FIGURE 2-3-12. DATA TRANSMISSION TO 8 BIT DEVICE
—— WRITE MODE
(BYTE TRANSMISSION OF ODD ADDRESS)

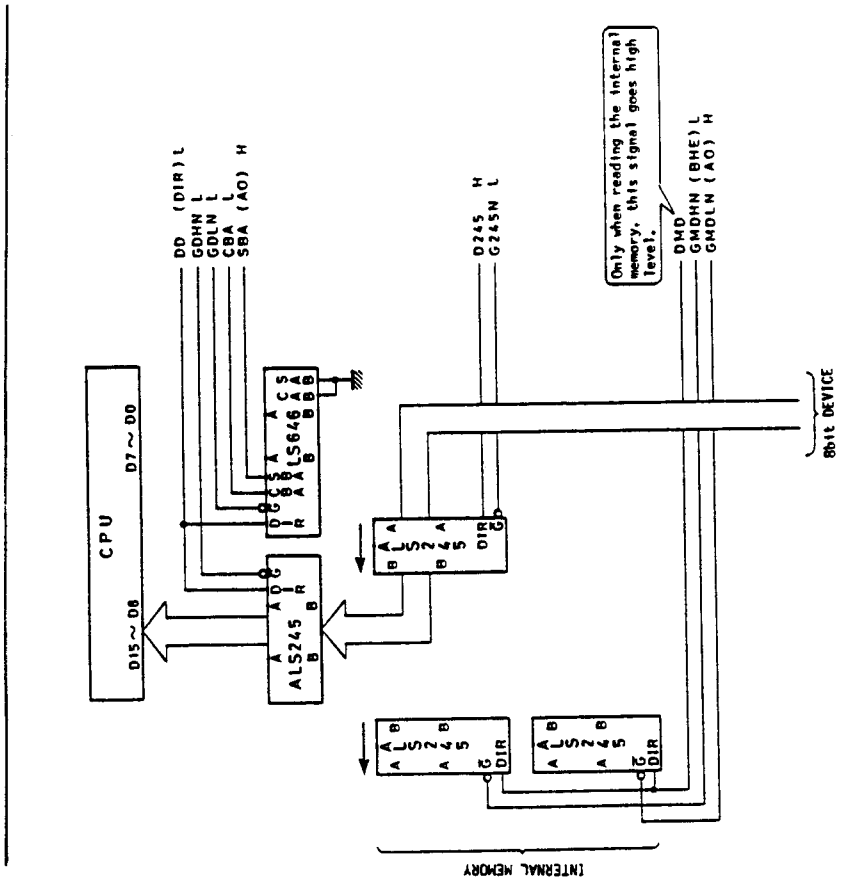


FIGURE 2-3-11. DATA TRANSMISSION TO 8 BIT DEVICE
—— READ MODE
(BYTE TRANSMISSION OF ODD ADDRESS)

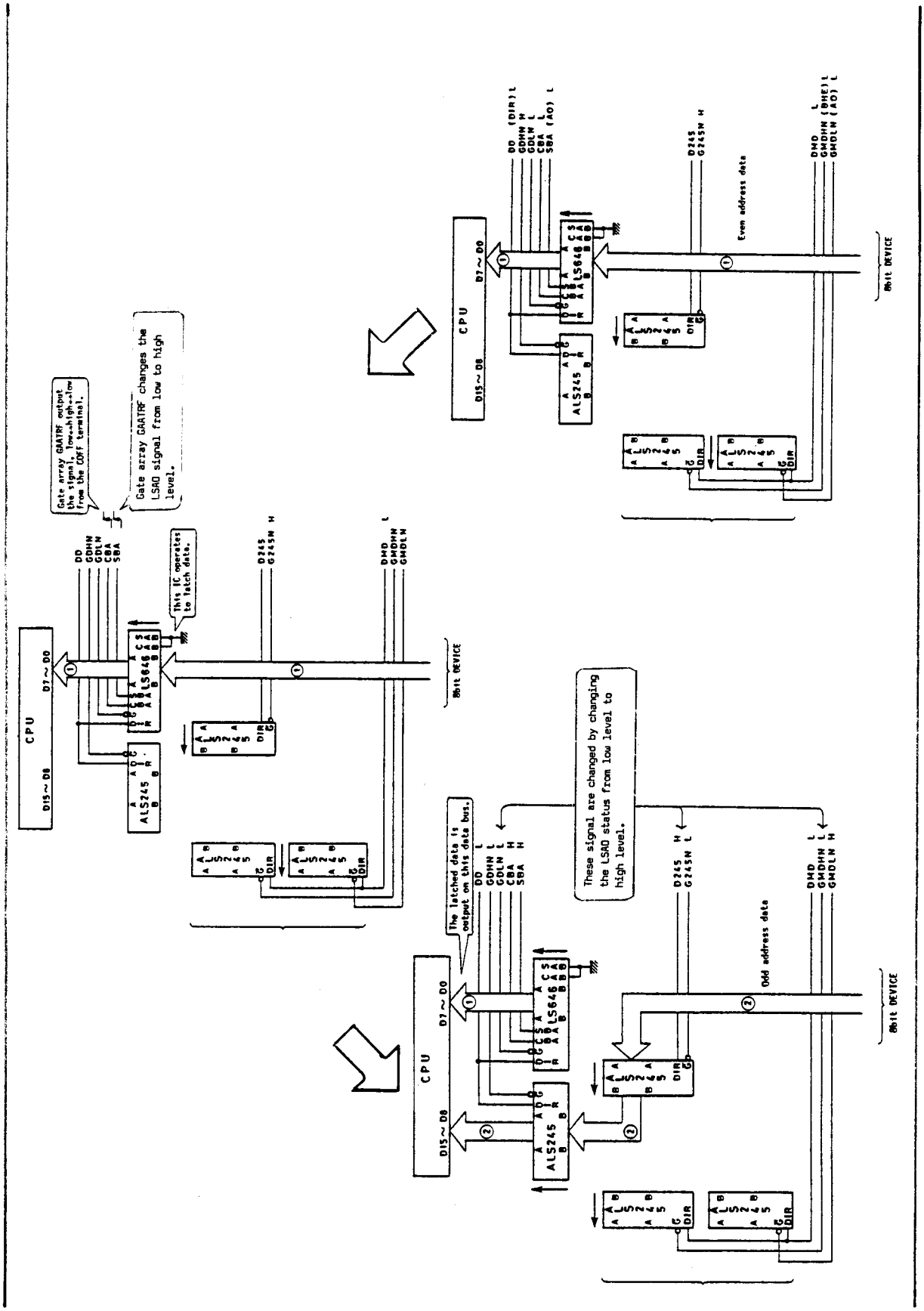


FIGURE 2-3-13. DATA TRANSMISSION TO 8 BIT DEVICE (WORD TRANSMISSION OF EVEN ADDRESS) — 16-8 BIT DATA CONVERSION — —— READ MODE

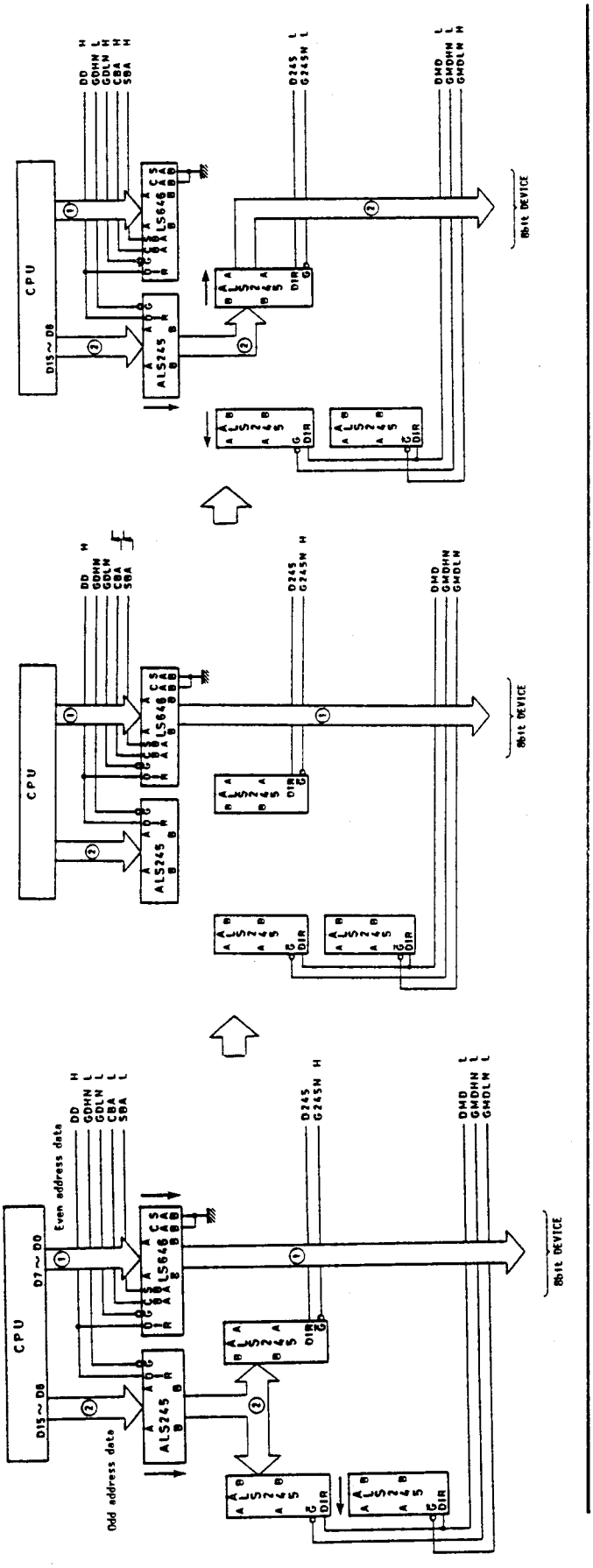


FIGURE 2-3-14. DATA TRANSMISSION TO 8 BIT DEVICE (WORD TRANSMISSION OF EVEN ADDRESS) —— 16-8 BIT DATA CONVERSION —— —— WRITE MODE

2.3.5 I/O Device Access Circuit

The GAATIO makes I/O device chip select signals by decording address signal. An ALS245 is used in the data transmission between the CPU and the I/O device.

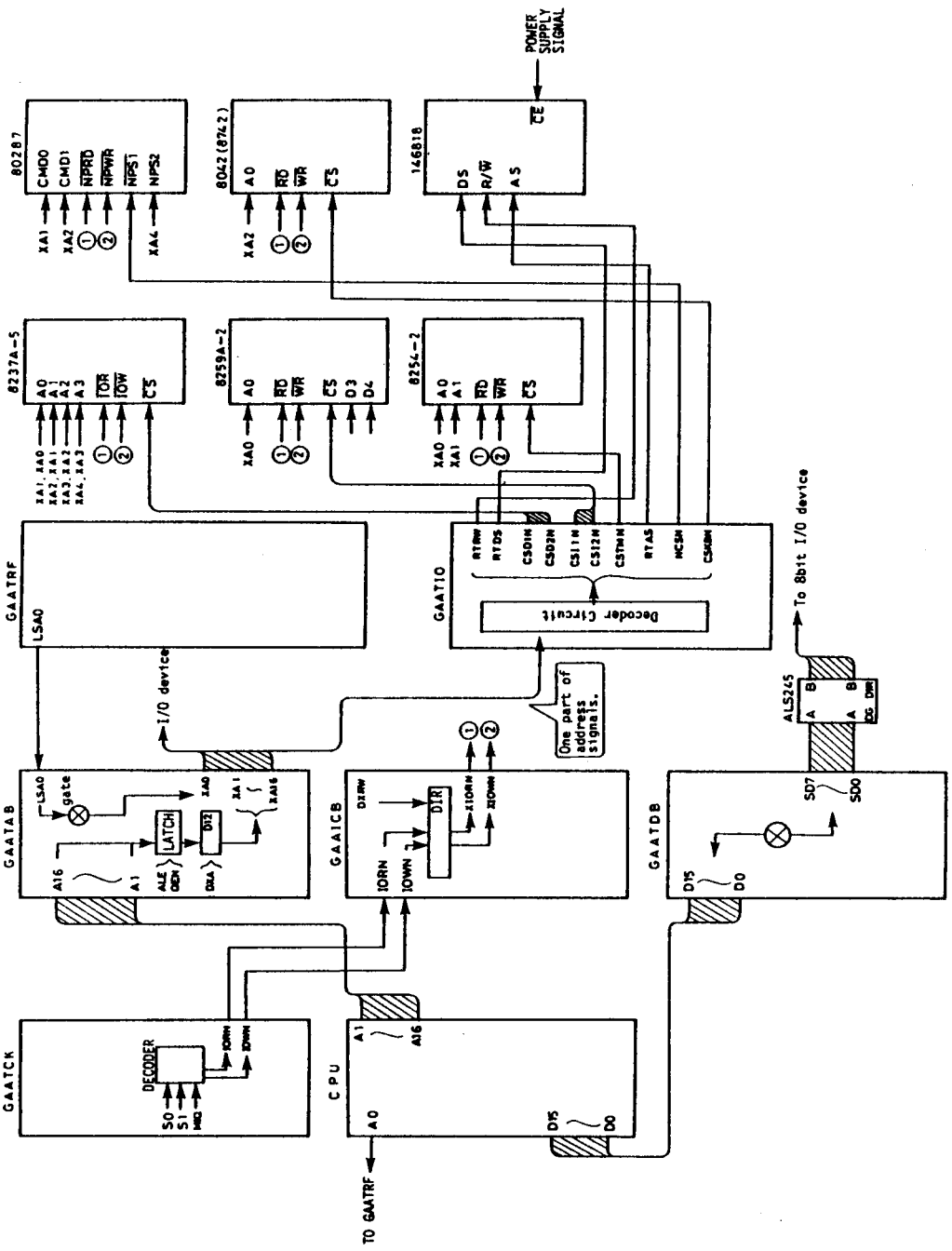


FIGURE 2-3-15. I/O DEVICE ACCESS CIRCUIT

2.3.6 DMA Control Circuit

There are two DMA controller on the main board (ANTA BOARD). A DMA1 (location: 2F) controls an 8-bit data transmission. A DMA2 (location: 2E) controls a 16-bit data transmission. It requires a page register to output address signal from A16 to A23. The page register is included in the GAATIO.
This section describes the following items.

1) Page register setting circuit
2) 8-bit DMA (Internal memory -- I/O)
3) 8-bit DMA (Internal memory -- Internal memory)
4) 16-bit DMA (Internal memory -- I/O)

2.3.6.1 Page Register Setting Circuit

The GAATIO includes a page register. The function of the page register is identical with TTL IC LS612. Table 2-3-10 describes about the function of LS612.

TABLE 2-3-10. EXPLANATION OF LS612

PIN NAME	FUNCTIONAL DESCRIPTION
D0 thru D11	I/O connections to data and control bus used for reading from and writing to the map register selected by RS0-RS3 when -CS is low. Mode controlled by R/-W.
RS0 thru RS3	Register select inputs for I/O operations.
R/-W	Read or write control used in I/O operations to select the condition of the data bus. When high, the data bus outputs are active for reading the register. When low, the data bus is used to write into the register.
-STROBE	Strobe input used to enter data into the selected map register during I/O operations.
-CS	Chip select input. A low input level selects the memory mapper (assuming more than on used) for an I/O operation.
MA0 thru MA3	Map address inputs to select one of 16 map registers when in map mode.
MA0 thru MO11	Map outputs. Present the map register contents to the system memeory address bus in the map mode. In the pass mode, these outputs provide the map address data on MO8-MO11 and low levels on MO0-MO7.
-ME	Map enable for the map outputs. A low level allows the outputs to be active while a high input level puts the outputs at high impedance.

The LS612 has sixteen 12-bit registers. The R/W signal and the STB signal is used as a read/write signal with pair. The RS0 to the RS3 is used as a select signal of registers when data setting. The MA0 to the MA3 is used as a select signal of registers when output data written. When setting mode, data is sent or received from "D0 TO D7" pin. When output mode, data is sent from "MD0 to MD7" pin.
When the ME signal is active, data written will be sent from "MD0 to MD7" pin.

2.3.6.2 8-bit DMA (Internal Memory — I/O)

Figure 2-3-17 shows the 8-bit DMA (Internal memory -- I/O) operation.
In the DMA mode, a MEMRN, a MEMWN, a IORN and an IOWN signal are output signals. (When CPU control mode, these signals are input signals.)

2.3.6.3 8-bit DMA (Internal Memory — Internal Memory)

Figure 2-3-18 shows the 8-bit DMA (Internal memory -- Internal memory) operation. First, the DMA controller stores memory data. Next, the DMA controller changes address signal and writes the stored data to the memory.

2.3.6.4 16-bit DMA (Internal Memory — I/O)

Figure 2-3-19 shows the 16-bit DMA (Internal memory -- I/O) operation.
A DMA2 controls the 16-bit DMA. In this mode, the GAATRF outputs A0 signal and BHE signal. Both A0 and BHE signal statuses are always low.
The DMA2's A0 signal is not connected to address bus bit 0. Because the A0 signal is output from the GAATRF.

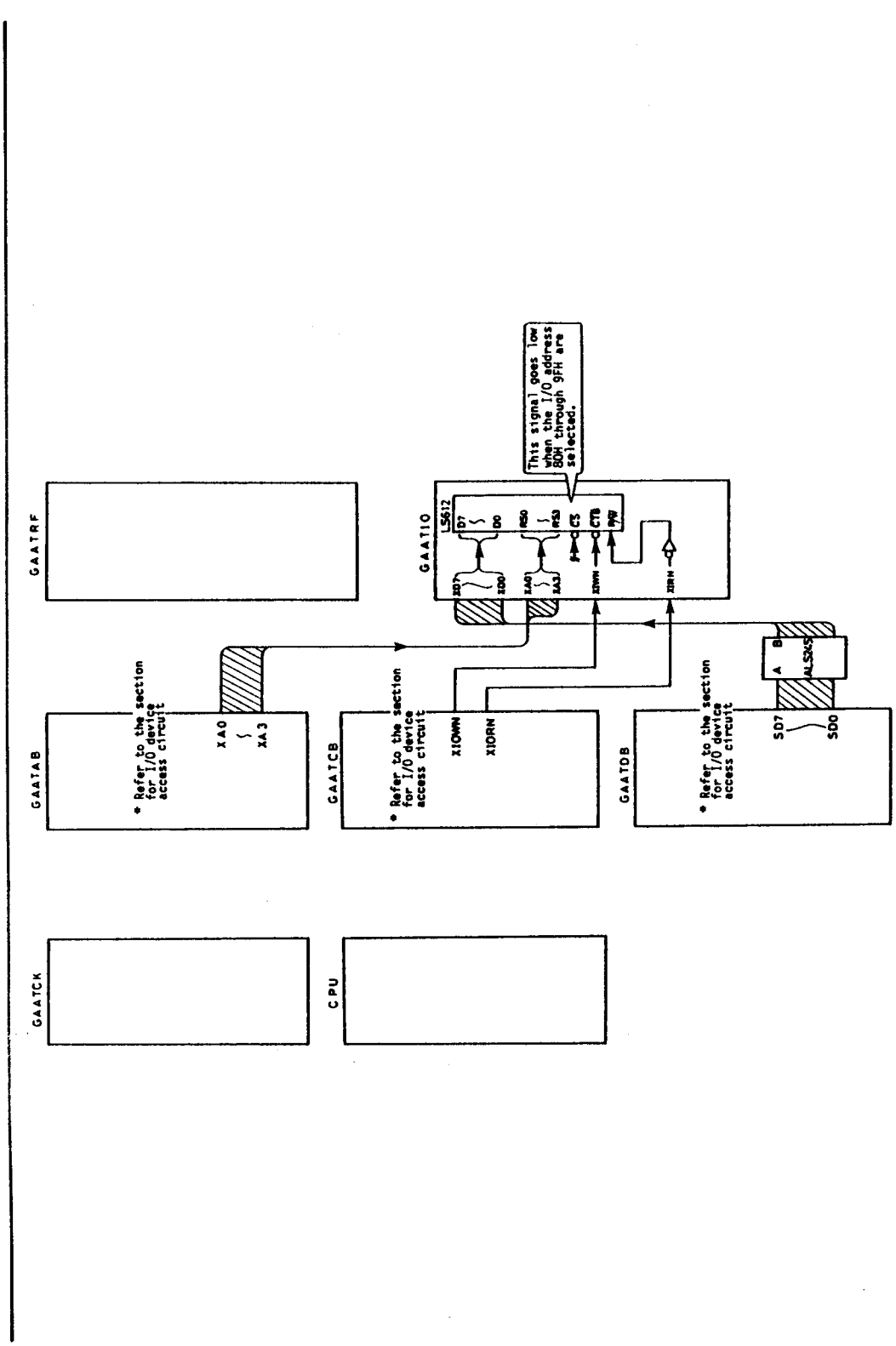


FIGURE 2-3-16. DMA CONTROL CIRCUIT I
(SETTING OF PAGE REGISTER)

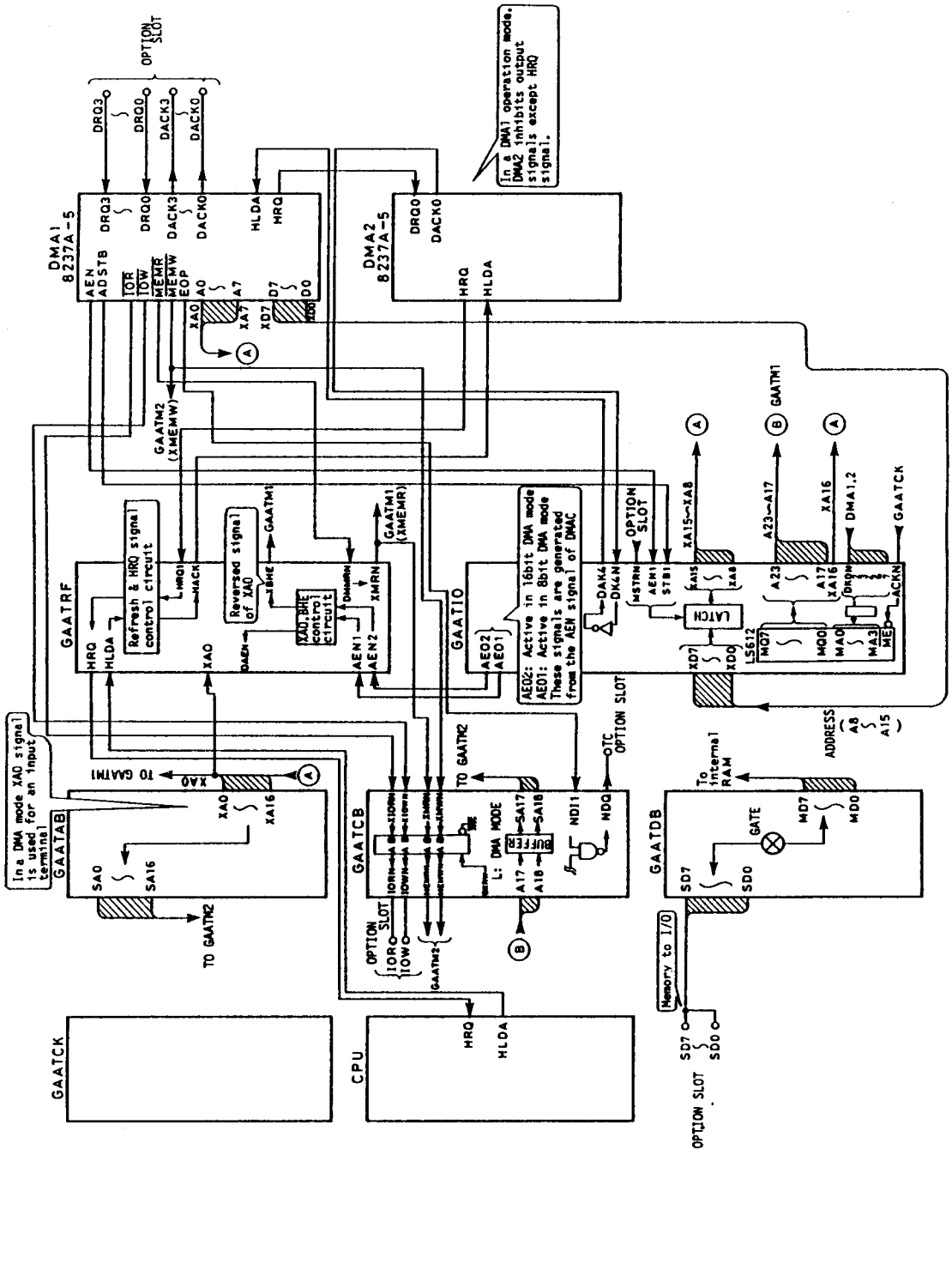


FIGURE 2-3-17. DMA CONTROL CIRCUIT II
(INTERNAL MEMORY <—> I/O)
—— 8 BIT DMA

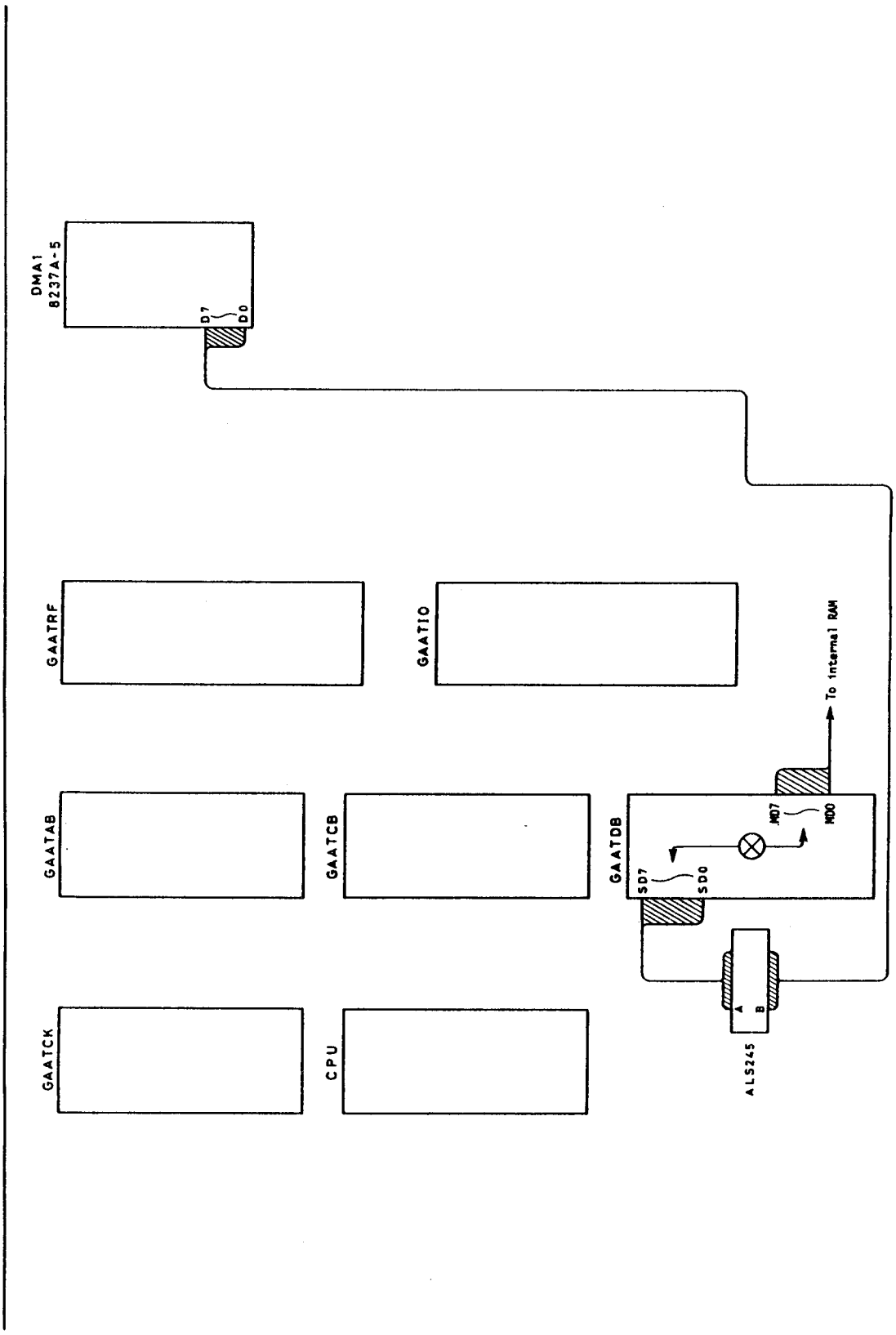


FIGURE 2-3-18. DMA CONTROL CIRCUIT III
(INTERNAL MEMORY <—> INTERNAL MEMORY)
— 8 BIT DMA

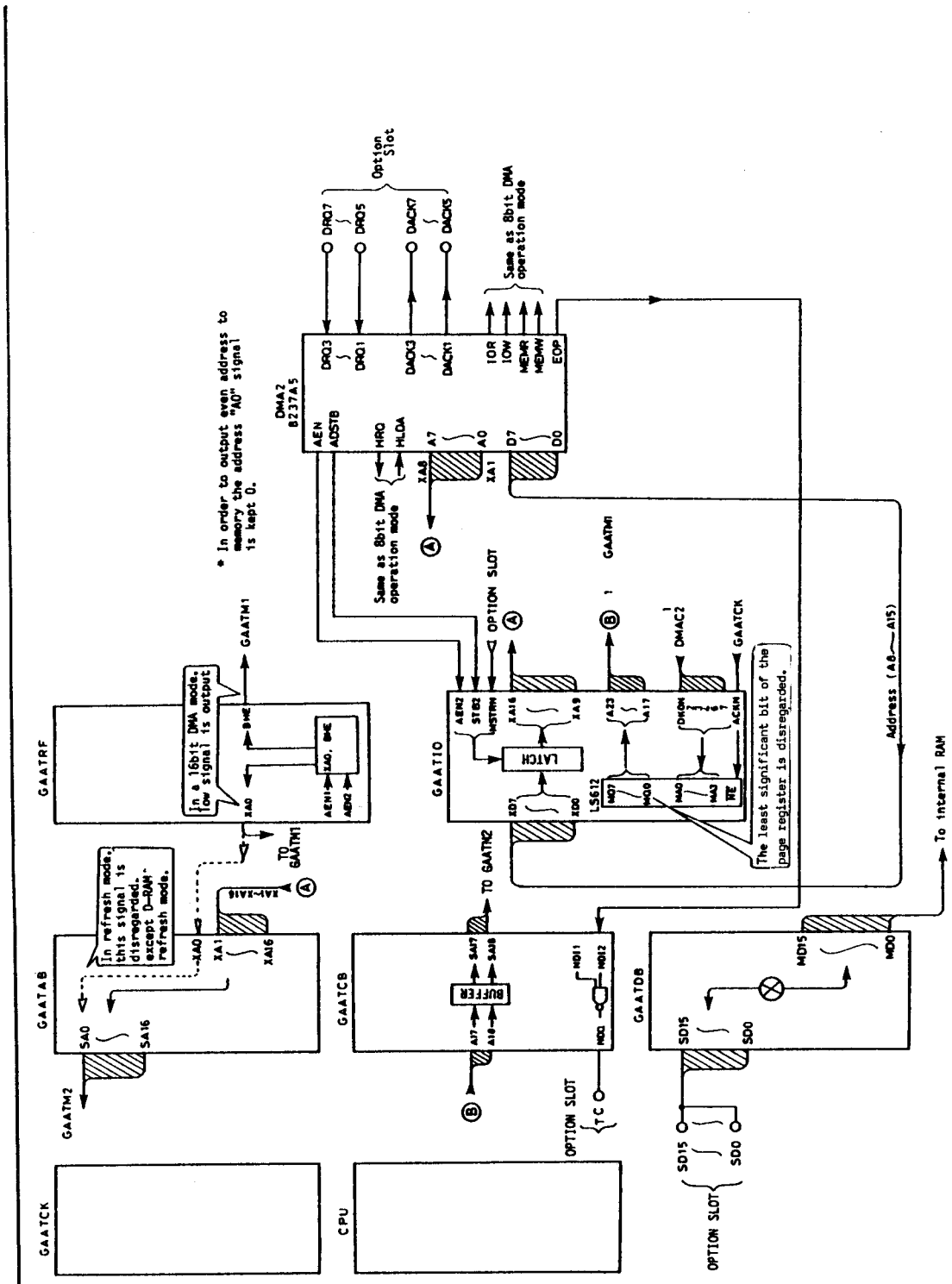


FIGURE 2-3-19. DMA CONTROL CIRCUIT IV
(INTERNAL MEMORY <—> I/O)
—— 16 BIT DMA

2.3.7 Ready Signal Control Circuit

The GAATRF controls a wait cycle insertion. The wait cycle is executed to allow adequate timing margin for internal chips and external chips. To request wait cycle, the GAATRF sends an ARDYN (Ready) signal and an ARENN (Ready enable) signal. The number of wait cycles is fixed except for a 16-bit ROM and a 16-bit I/O channel device. You can select wait cycles for the 16-bit ROM and the 16-bit I/O channel device by using jumper connectors J4, J5 and J6. But the selection is available only for 10MHz use.

TABLE 2-3-11. WAIT CYCLES

DEVICE TO BE ACCESSED	WAIT CYCLES [TOTAL CYCLES] 6MHz/ 8MHz	10MHz
16-bit memory (16-bit bus operation)		
DRAM (System memory) (00000 to 9FFFF)	1 [3]	1 [3]
ROM (0E0000 to 0FFFFF & FE0000 to FFFFFF)	1 [3]	1 or 2 [3 or 4] * NOTE 1
I/O channel (Other range)	1 [3]	1, 2, 3 or 4 [3, 4, 5 or 6] * NOTE 1
8-bit memory on I/O channel (8-bit bus operation)	4 [6]	8 [10]
8-bit memory on I/O channel (16-bit bus operation)	10 [12]	18 [20]
16-bit I/O on I/O channel (16-bit bus operation)	1 [3]	3 [5]
8-bit I/O on I/O channel (8-bit bus operation)	4 [6]	8 [10]
8-bit I/O on I/O channel	10 [12]	18 [20]

(16-bit bus operation)

* NOTE 1 : A jumper connector can select wait cycles. Please refer to Table 2-3-12.

TABLE 2-3-12. WAIT CYCLE SELECTION

JUMPER NUMBER			NUMBER OF WAIT CYCLES	
6	5	4	EPROM	16-BIT EXTERNAL DEVICE
*	*	B-C	1	*
*	*	A-C	2	*
B-C	B-C	*	*	1
B-C	A-C	*	*	2
A-C	B-C	*	*	3
A-C	A-C	*	*	4

* --- Ignored

2.3.7.1 Insertion More Wait Cycle

When you want to insert more wait cycles, Please control the IOCHRDY (I/O channel Ready) signal. When the IOCHRDY signal is high, a wait cycle will be inserted.

2.3.7.2 Zero Wait Cycle Request

To insert no wait cycle, a OWS signal is provided on the option slot. This signal is low when active.

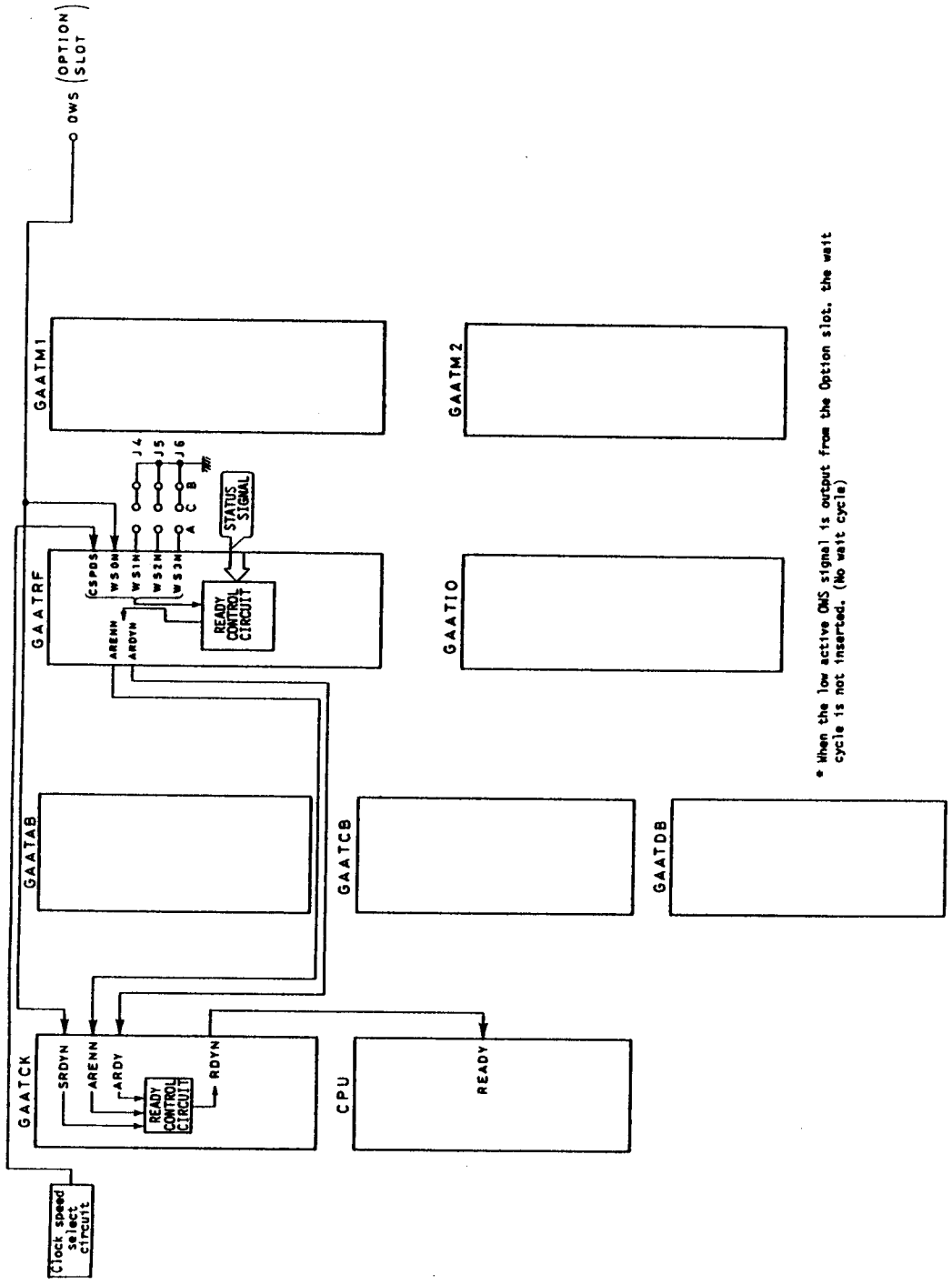


FIGURE 2-3-20. READY SIGNAL CONTROL CIRCUIT

2.3.8 Command Delay Signal Control Circuit

Some devices can not allow the standard following time (T) because it is too short. The command delay signal control circuit makes adequate timing margin for these devices.
To execute command delay function, it is necessary to send a CDLY (Command delay) signal to the GAATCK. The GAATRF outputs a CDLY signal when it detects the following mode listed in Table 2-3-13 automaticaly.

FIGURE 2-3-21. TIMING BETWEEN ADDRESS SIGNAL AND READ/WRITE SIGNAL

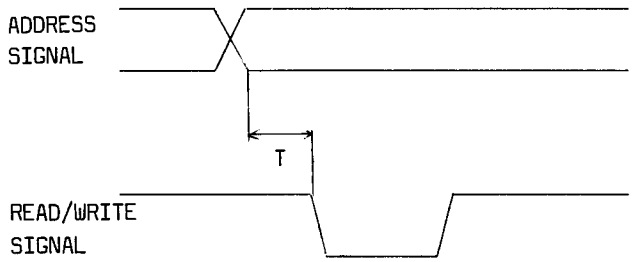


TABLE 2-3-13. CONDITION OF THE CDLY SIGNAL OUTPUT

NO.	CONDITION OF THE CDLY SIGNAL OUTPUT
1	INTA mode
2	I/O read /write mode
3	8-bit memory read/write

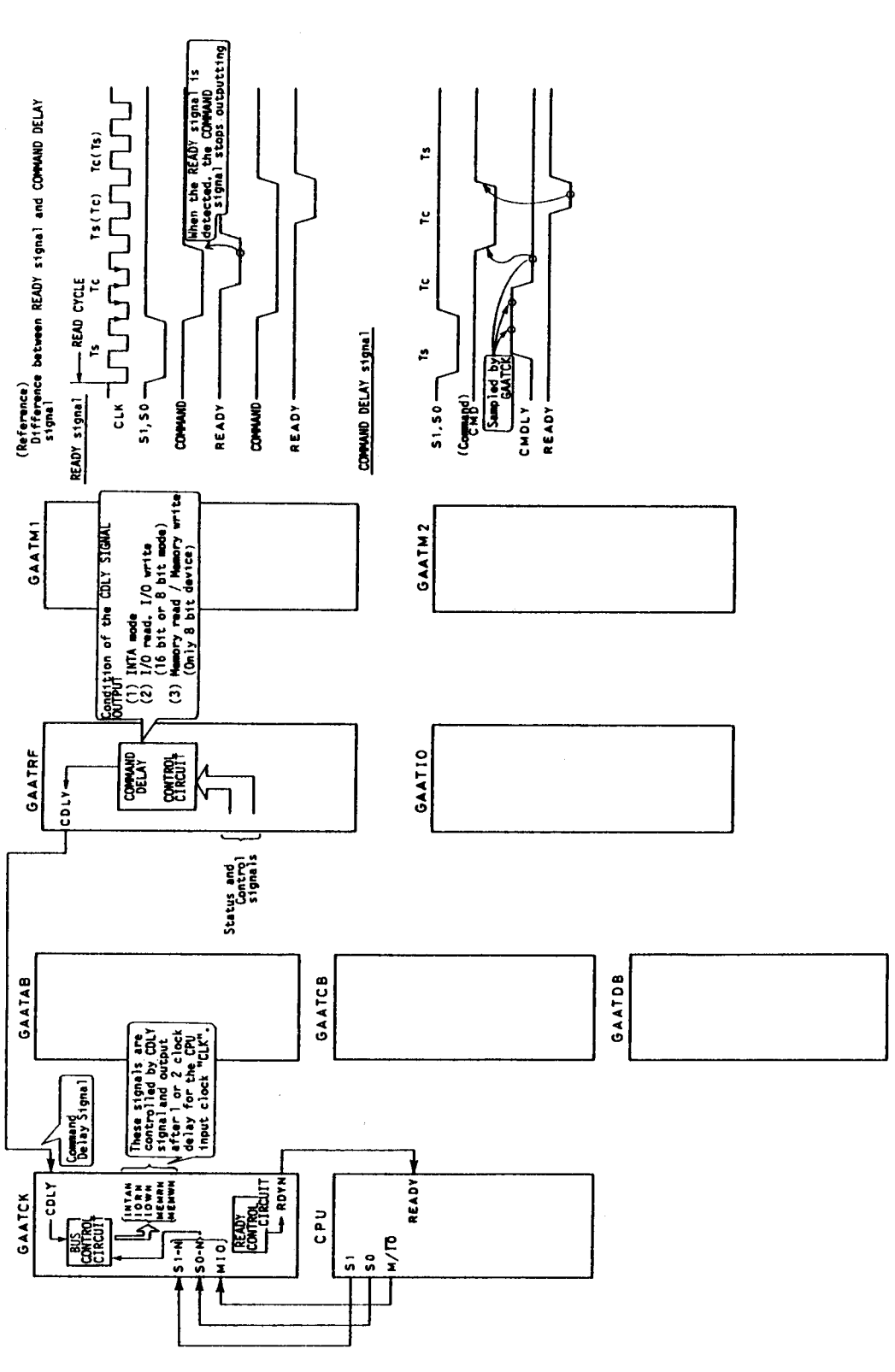


FIGURE 2-3-22. COMMAND DELAY SIGNAL CONTROL CIRCUIT

2.3.9 Interrupt Control Circuit

This circuit includes two interrupt controllers to support 15 level interrupts.
Two INTCs are connected by a cascade mode.
Figure 2-3-23 shows interrupt control circuit operation.

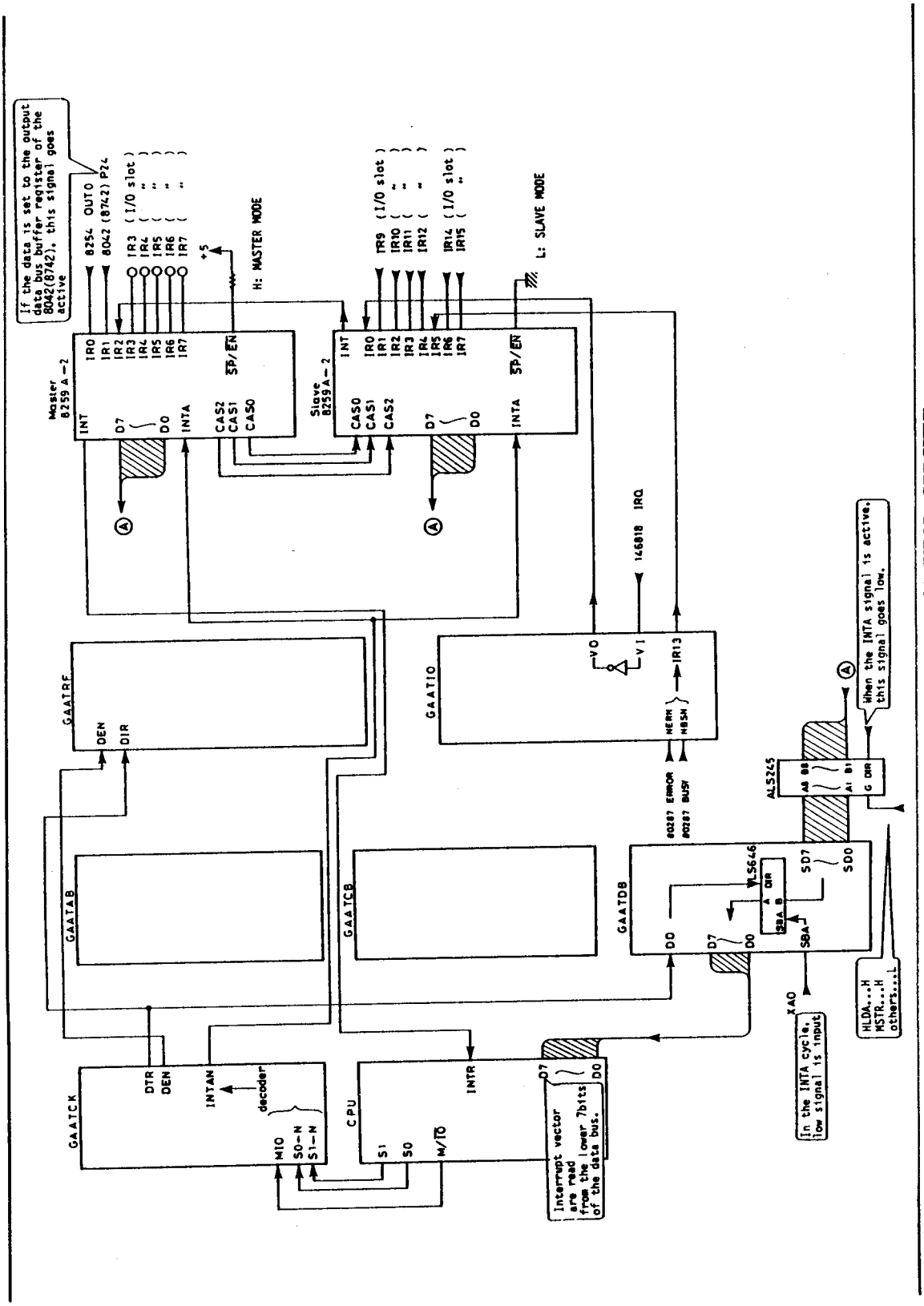


FIGURE 2-3-23. INTERRUPT CONTROL CIRCUIT

2.3.10 ROM Access Circuit

There are two pairs of ROM sockets. One is used by BIOS ROM. The others are free sockets for user. We can select ROM socket and ROM size by setting of the jumper connectors J4, J5, J6 and J7. Functional description of each jumper connector is explained in CHAPTER 7.

2.3.10.1 Available ROM Types

You can install the following type of ROM chips.

TABLE 2-3-14. AVAILABLE ROM TYPES

ROM TYPE	RECOMMENDED ACCESS SPEED	JUMPER SETTINGS	
		J4	J5
27128, 2764	200ns or more higher	A-C	A-C
27256	200ns or more higher	B-C	B-C

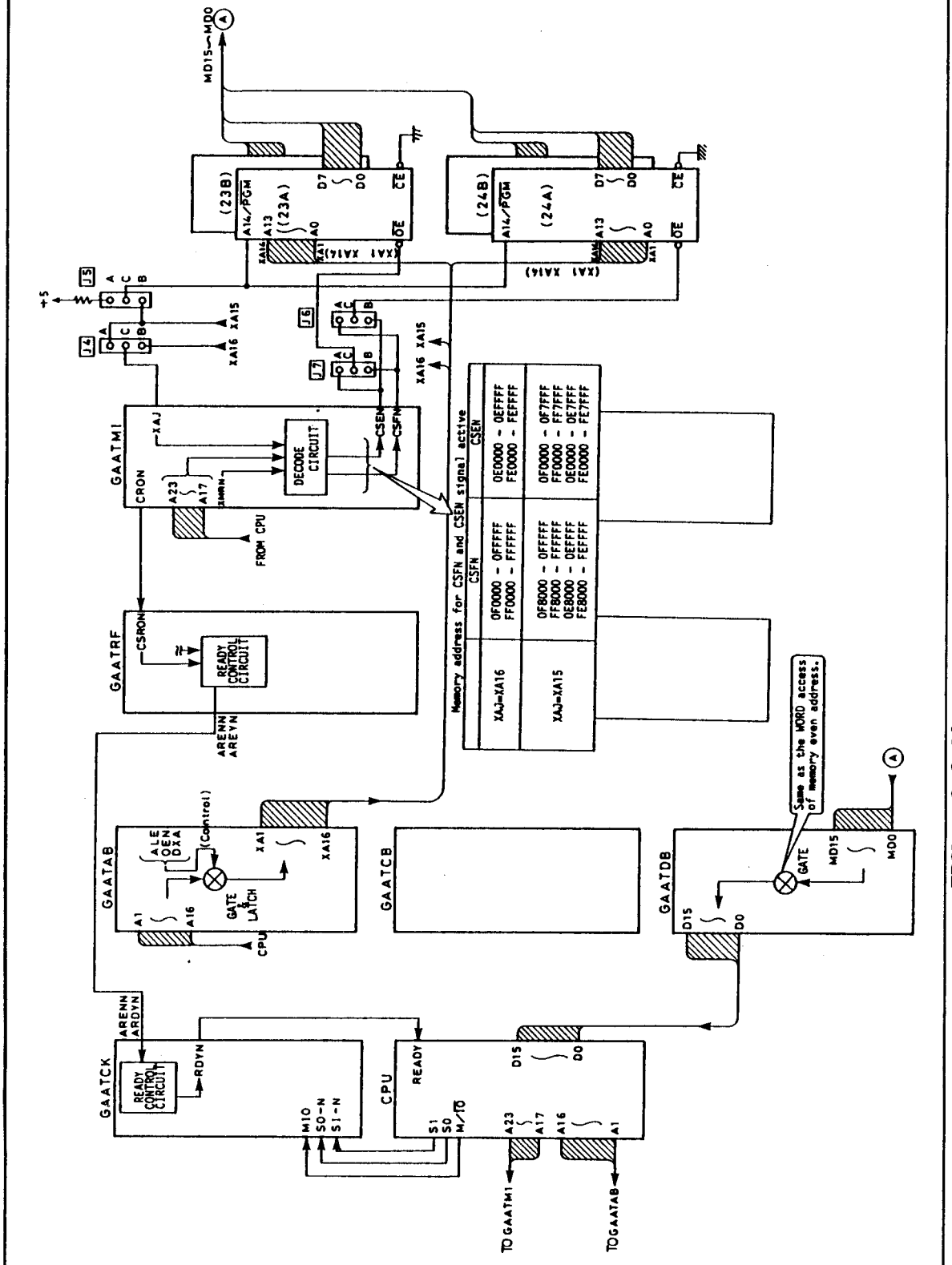


FIGURE 2-3-24. ROM ACCESS CIRCUIT

2.3.11 D-RAM Refresh Circuit

A timer counter (8254-2) controls refresh interval time. The refresh address is sent from a 8-bit binary counter in GAATAB. During D-RAM refresh, the CPU executes a bus hold cycle.
The RFNO (Refresh output) signal is an important signal. From this signal, the GAATM1 makes a RA0 and a RA1 signal (RAS signal). The GAATM2 controls the refresh address by using this RFNO signal. And more, this signal is used by the 8-bit binary counten as a count-up signal.
Figure 2-3-25 shows the D-RAM refresh control circuit operation.

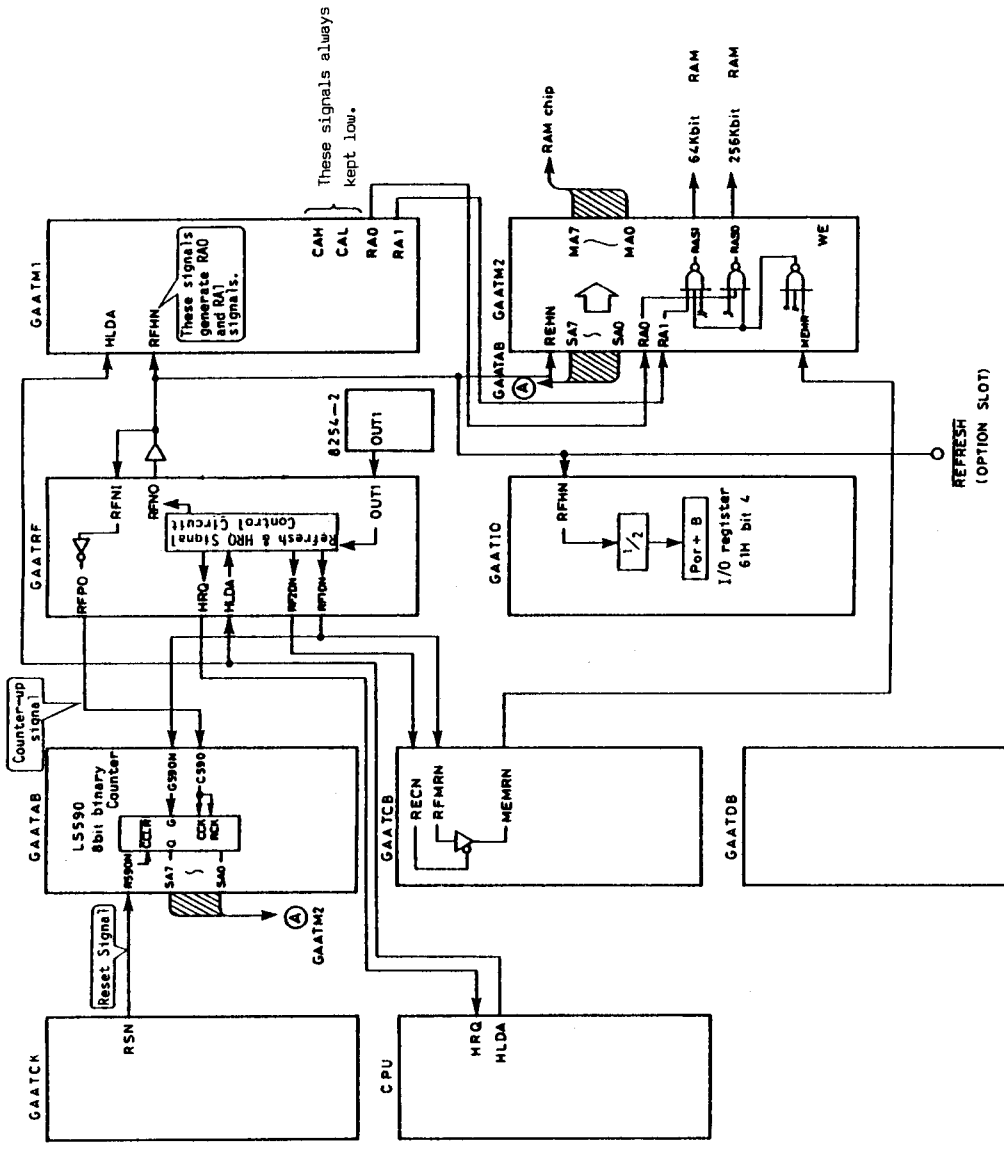


FIGURE 2-3-25. D-RAM REFRESH CIRCUIT

2.3.12 RAM Parity Check Circuit

In a D-RAM write mode, the GAATM1 generates a parity data. When in D-RAM read mode, the GAATM1 calculates the memory read data and the parity read data. If a parity error has occurred, the GAATM1 outputs a PCKN signal. The GAATIO receives a PCKN signal and makes a NMI (Non maskable interrupt) signal.
Figure 2-3-26 and Figure 2-3-27 show the RAM parity check circuit operation.

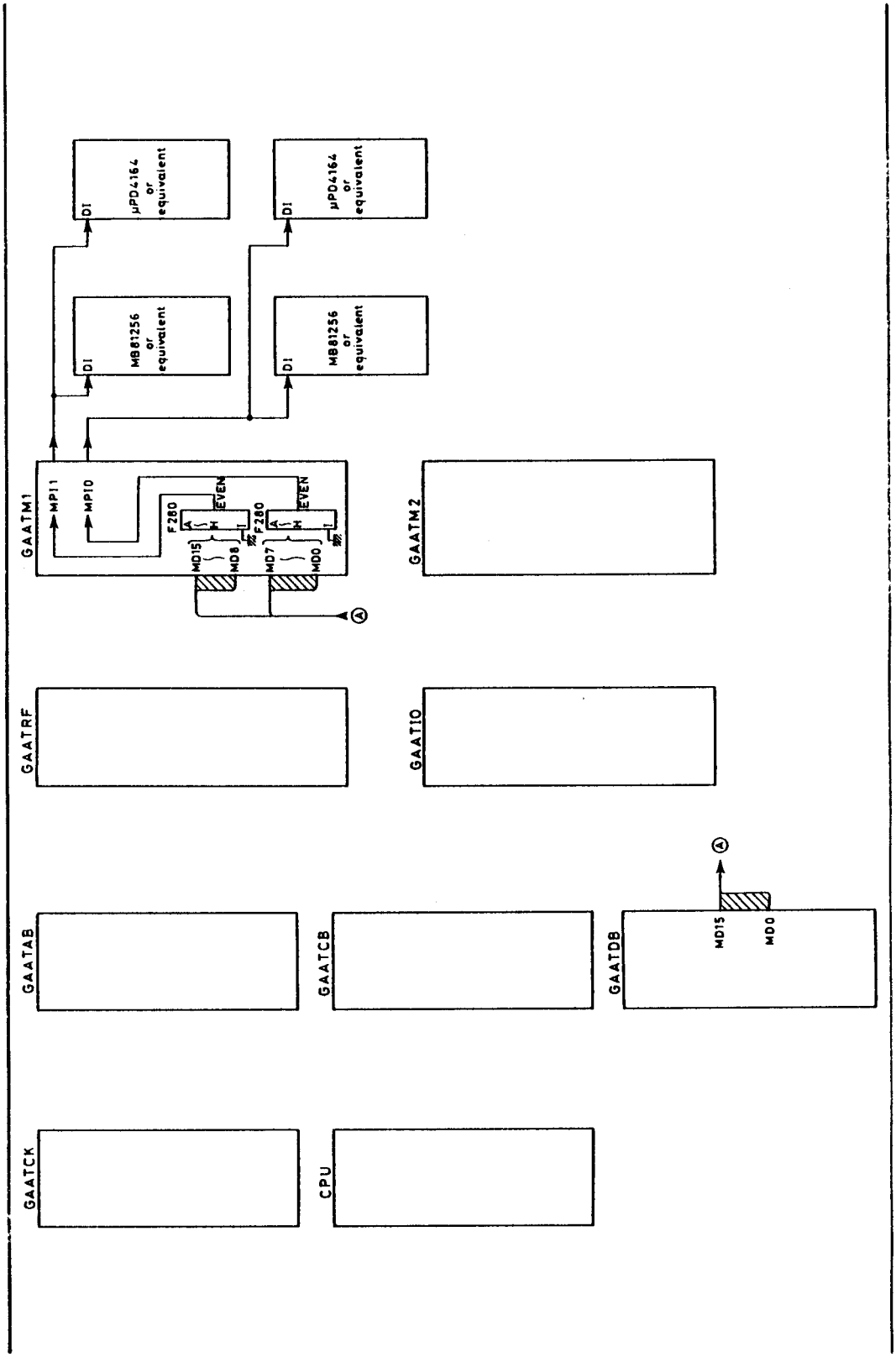


FIGURE 2-3-26. RAM PARITY CHECK CIRCUIT (DATA WRITE MODE)

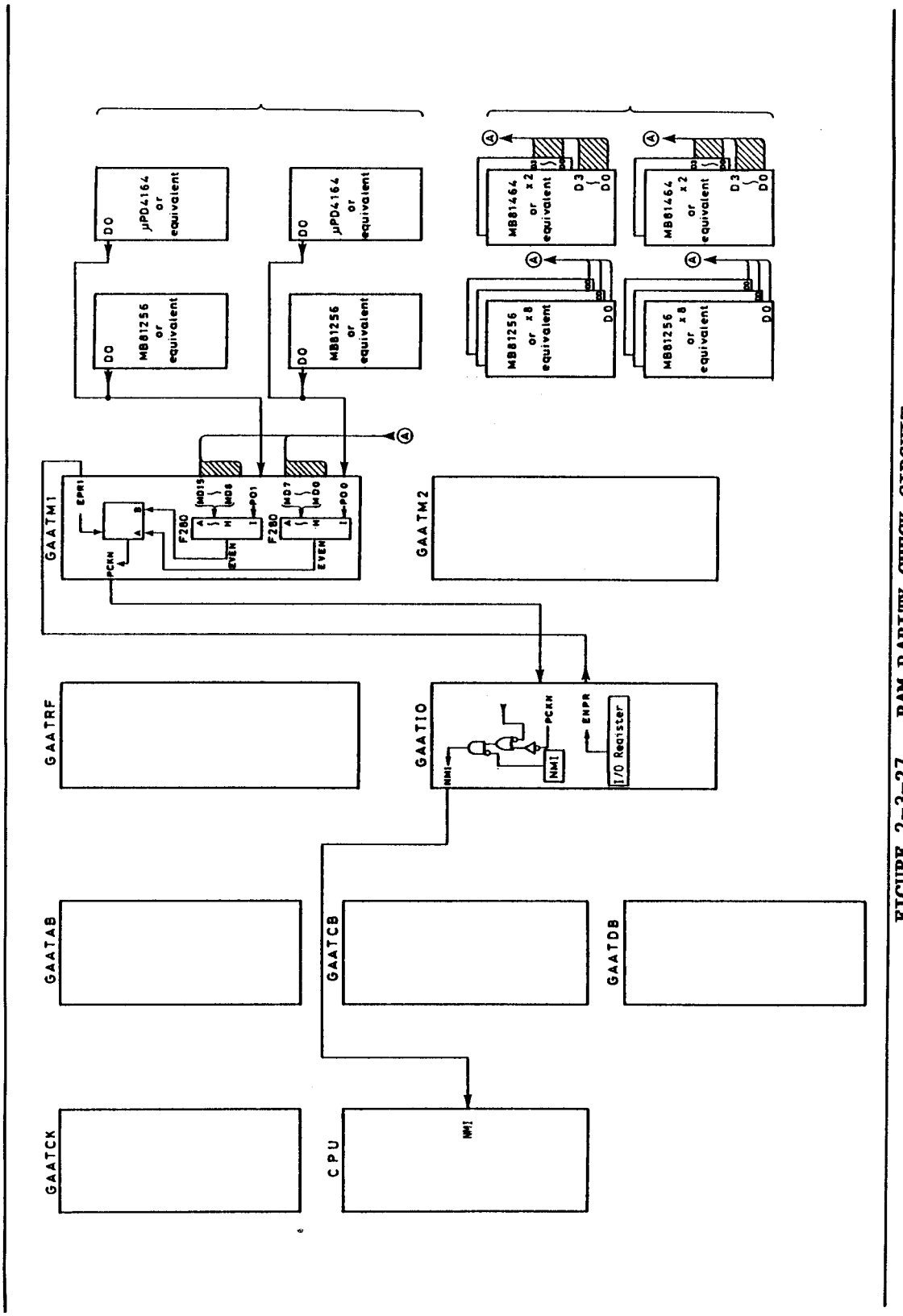


FIGURE 2-3-27. RAM PARITY CHECK CIRCUIT (DATA READ MODE)

2.3.13 Speaker Control Circuit

The timer counter controls the speaker. Figure 2-3-28 shows the speaker control circuit operaton.

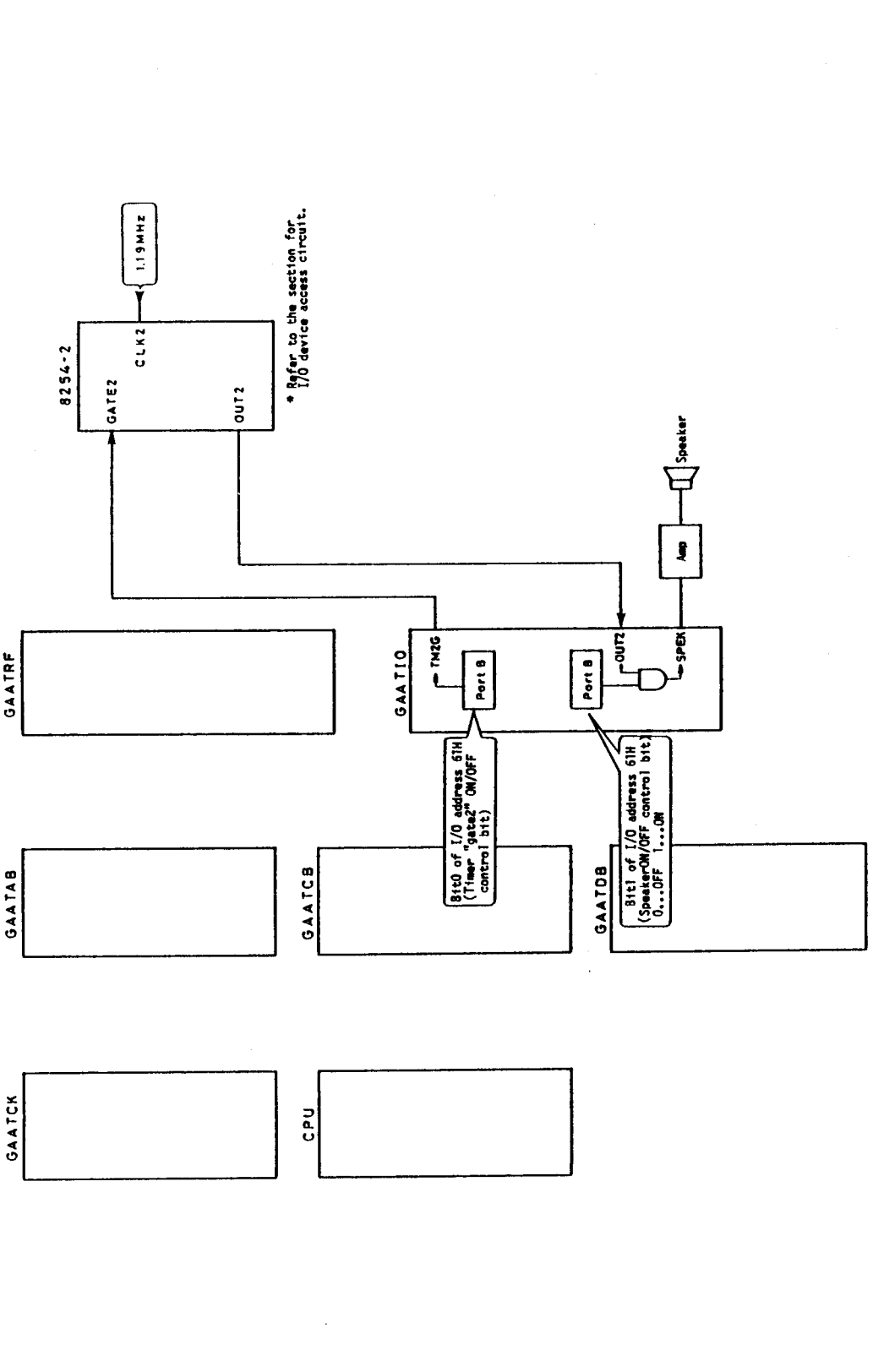


FIGURE 2-3-28. SPEAKER CONTROL CIRCUIT

2.3.14 Keyboard Interface Circuit & Other Circuit

A Keyboard controller (8042 or 8742) includes the following functions.

1) Keyboard interface
2) RAM size reading
3) Monitor setting reading
4) Disabling keyboard scan codes
5) Software reset signal generation
6) Address A20 signal control

2.3.14.1 Keyboard Interface

When receiving keyboard data, the 8042 receives keyboard data from test 1 pin.
When sending a keyboard control command, the 8042 sends command data from P27 pin.
When the 8042 receives keyboard data, it sends an interrupt request signal from P24 pin. P26 pin of 8042 outputs control signal of keyboard data transmission.
In detail, (Refer to section 2.2)

2.3.14.2 RAM Size Reading

The 8042 reads the condition of jumper connector J2 on the ANT-RM board.

2.3.14.3 Monitor Setting Reading

The 8042 reads the condition of slide switch SW1 on the ANTA board.

2.3.14.4 Disabling Keyboard Scan Codes

The P17 pin of 8042 inputs the condition of the key cylinder switch. When P17 pin is low, keyboard scan code will be disabled by the 8042 internal circuit.

2.3.14.5 Software Reset Signal Generation

The 8042 outputs software reset signal from P20 pin.

2.3.14.6 Address A20 Signal Control

The 8042 outputs A20 control signal (gate) signal to GAATRF. GAATRF controls A20 signal as below.

TABLE 2-3-15. A20 SIGNAL CONTROL BY GAATRF

CA20	A20G	A20
0	1	0
1	1	1
*	0	0

* ---- DON'T CARE

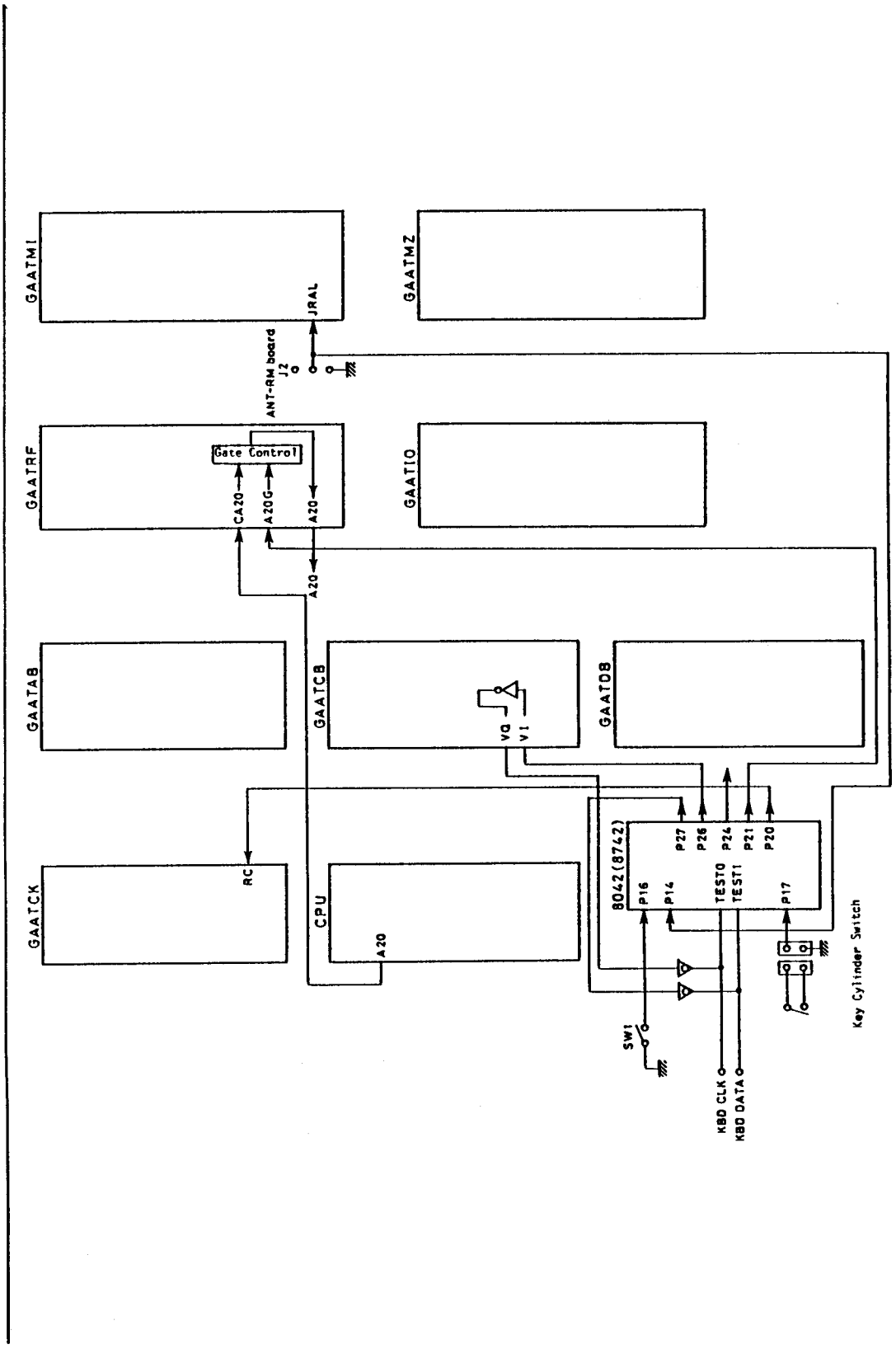


FIGURE 2-3-29. KEYBOARD INTERFACE AND OTHER FUNCTION CIRCUIT

2.3.15 I/O Slot Access Signal

Figure 2-3-30 shows the I/O slot access signals.

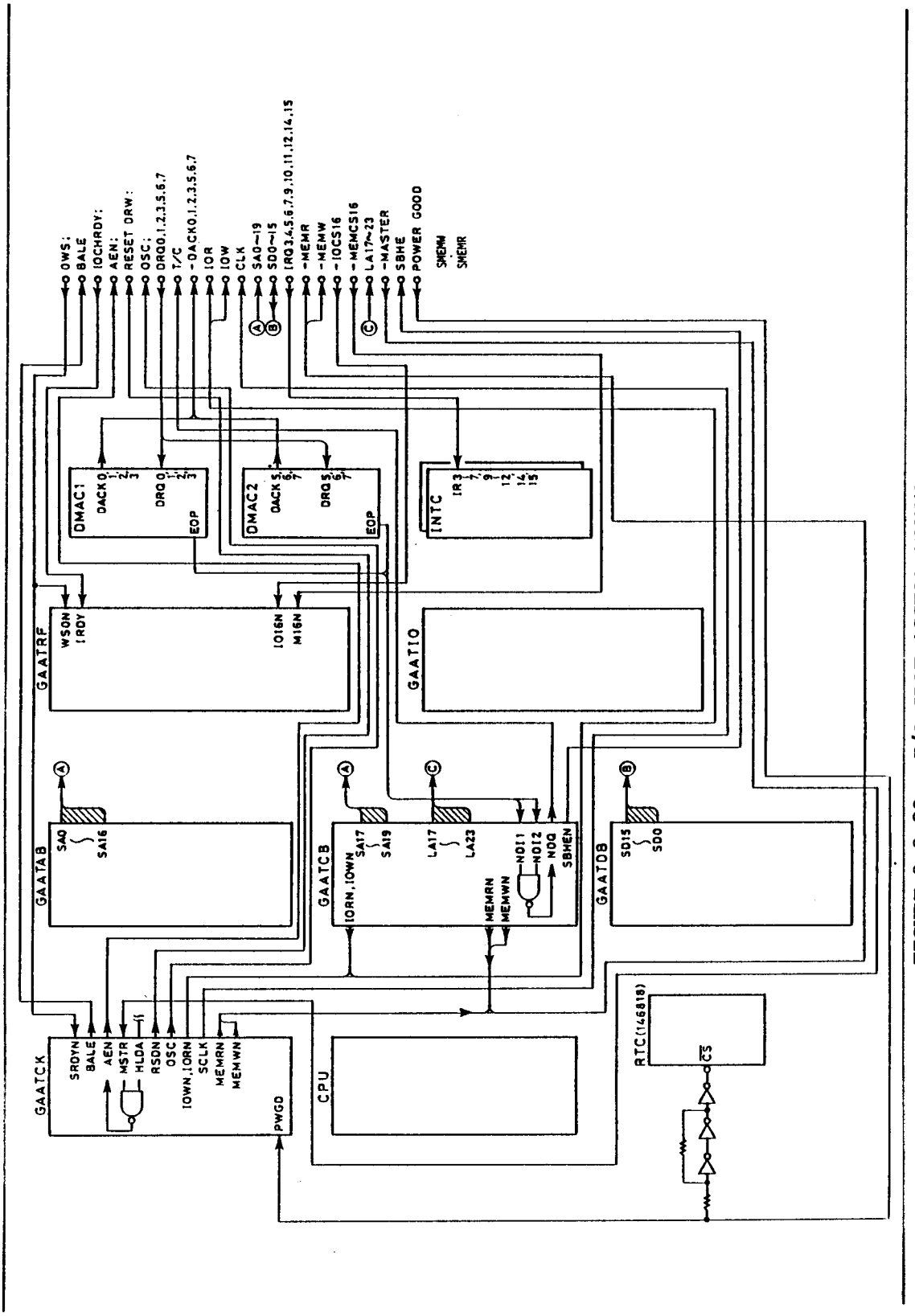


FIGURE 2-3-30. I/O SLOT ACCESS SIGNAL

2.4 MULTI-FUNCTION ADAPTER (SPFG BOARD) OPERATION

2.4.1 Serial Interface

A 16450 is used as a serial data controller. The XTAL1 terminal receives 1.8432 MHz clock generated by the OSC terminal in the gate array GAATSP.

2.4.1.1 16450 Chip Select Circuit

Chip select signal CS2 for activating the 16450 is applied from the gate array GAATSP (SCSN signal). There are two kinds of I/O addresses which SCSN signal activates. They are selected by jumper pin J5 and J6. Setting of J5 and J6 are listed in CHAPTER 7.

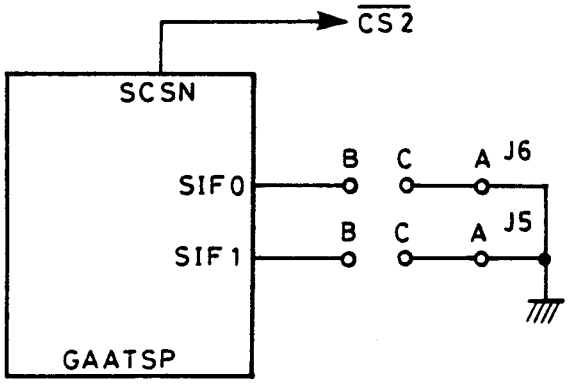


FIGURE 2-4-1. 16450 CHIP SELECT CIRCUIT

BPS can be set DC to 56000 bps.
The 8250 and the 16450 are indentical in their functions, however handling speed of the 16450 is higher than that of the 8250.

2.4.1.2 Interrupt Signal

Interrupt signal goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER.

1. Receiver Error Flag
2. Receiver Data Available
3. Transmitter Holding Register Empty
4. Modem Status Interrupt

Output of INTRPT signal can be applied to either IRQ3 or IRQ4. Either IRQ3 or IRQ4 is selected by jumper J9.

TABLE 2-4-1. JUMPER J9 SETTING

J9	INTERRUPT SIGNAL
A-C	IRQ4
B-C	IRQ3

2.4.1.3 Data Buffer Direction Control Signal

While the serial or parallel port is read, the DDIR signal generated by the gate array GAATSP DDIR terminal is kept low.

2.4.2 Parallel Data Control Circuit

The gate array GAATSP controls parallel data.

2.4.2.1 I/O Address Selection

There are two kinds of I/O addresses on the parallel Data control circuit. They are selected by jumper pin J3 and J4. Setting of J3 and J4 are listed in CHAPTER 7.

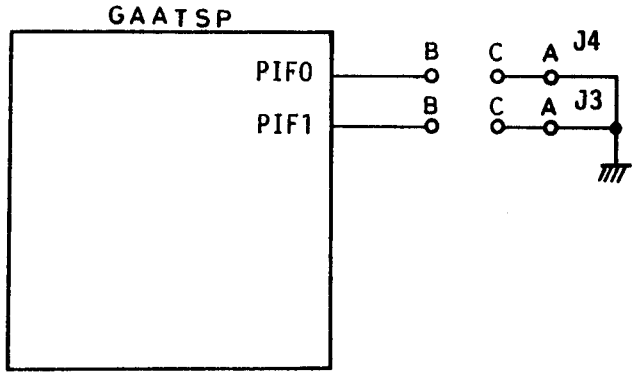


FIGURE 2-4-2. I/O ADDRESS SELECTION

2.4.2.2 Parallel Data Control Circuit Functions

Parallel Data control circuit has the following six functions.

1. Data output circuit
2. Output data read circuit
3. Printer control signal output circuit
4. Printer control signal read circuit
5. Printer status read circuit
6. Interrupt signal control circuit

Data Output Circuit

Direction of data is only from CPU to Printer because the DIR of ALS245 is fixed at low level.

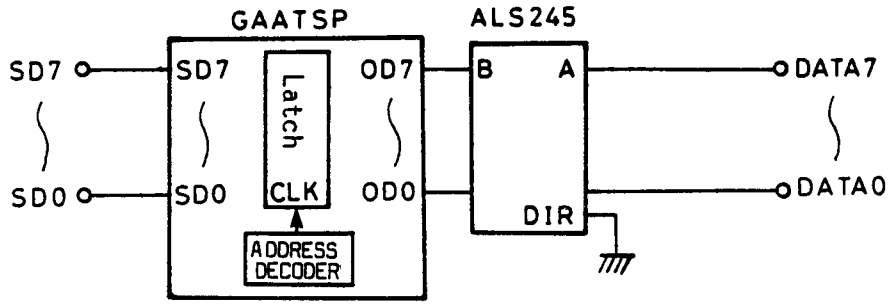


FIGURE 2-4-3. DATA OUTPUT (PRINTER DATA REGISTER WRITE)

Output Data Read Circuit

The output data for printer can be read via LS244 located in the GAATSP.

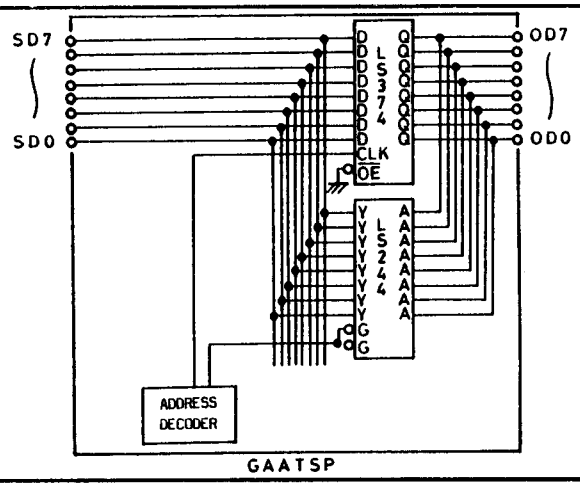


FIGURE 2-4-4. OUTPUT DATA READ CIRCUIT

Printer Control Signal Output Circuit

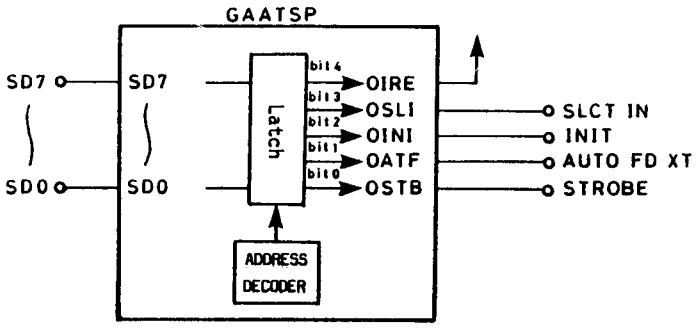


FIGURE 2-4-5. PRINTER CONTROL SIGNAL OUTPUT CIRCUIT

Printer Control Signal Read Circuit

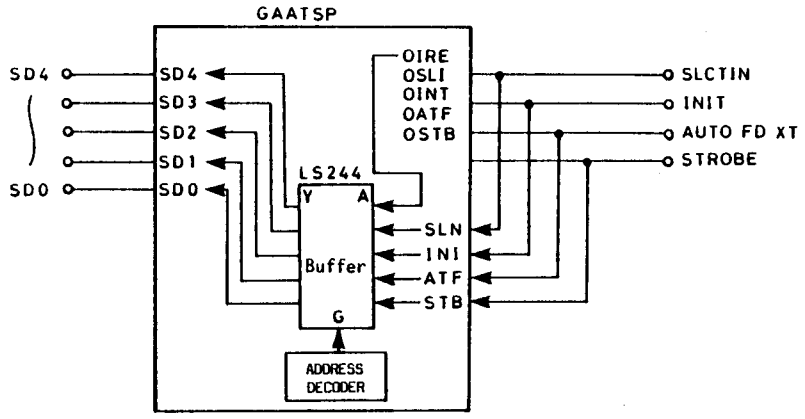


FIGURE 2-4-6. PRINTER CONTROL SIGNAL READ CIRCUIT

Printer Status Read Circuit

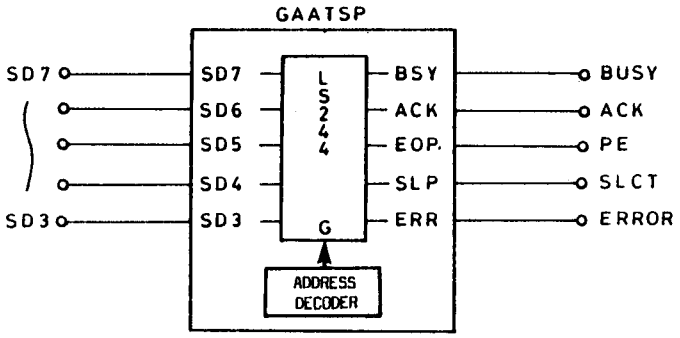


FIGURE 2-4-7. PRINTER STATUS READ CIRCUIT

Interrupt Signal Control Circuit

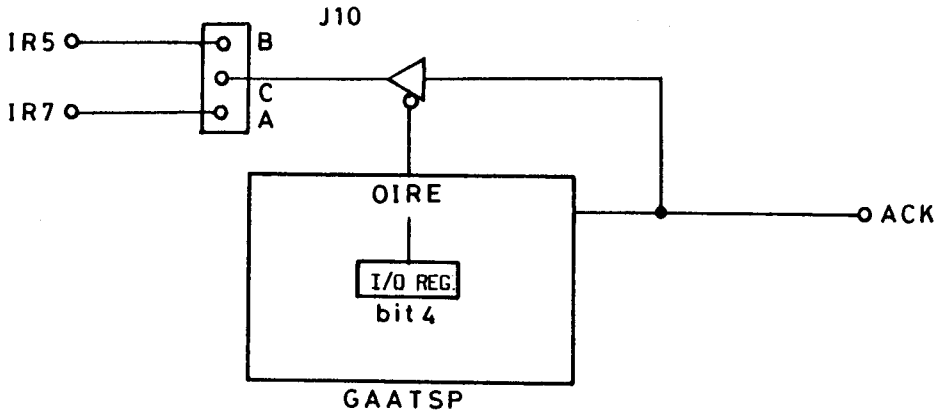


FIGURE 2-4-8. INTERRUPT SIGNAL CONTROL CIRCUIT

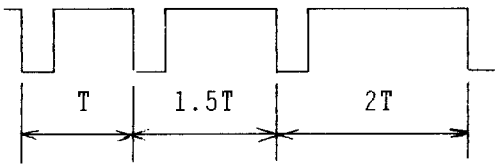
1.2 MB FDD

EQUITY II / EPSON PC+'s 1.2MB FDD (SD-581L) can not be installed on EQUITY III+ / EPSON PC AX. Because FDD control signals are different between EQUITY II / EPSON PC+'s 1.2MB FDD and EQUITY III+ / EPSON PC AX's 1.2MB FDD. (Refer to Table 2-4-2)

TABLE 2-4-2. DIFFERENCE BETWEEN 1.2MB FDD OF SD-581L AND FD1155C/MD5501

PIN NO.	SD-581L(*1)	FD1155C/MD5501(*2)
2	MODE SELECT	MODE SELECT
4	DISK CHANGE	(NOT USED)
6	DRIVE SELECT 3	DRIVE SELECT 3
8	INDEX	INDEX
10	DRIVE SELECT 0	DRIVE SELECT 0
12	DRIVE SELECT 1	DRIVE SELECT 1
14	DRIVE SELECT 2	DRIVE SELECT 2
16	MOTOR ON	MOTOR ON
18	DIRECTION	DIRECTION
20	STEP	STEP
22 (*3)	WRITE DATA	WRITE DATA
24	WRITE GATE	WRITE GATE
26	TRACK 00	TRACK 00
28	WRITE PROTECT	WRITE PROTECT
30 (*3)	READ DATA	READ DATA
32	SIDE SELECT	SIDE SELECT
34	READY	DISK CHANGE
OTHER PIN	GND	GND

NOTE : (*1) ; SD-581L is used in the EQUITY II/EPSON PC+.
(*2) ; FD1155C and MD5501 are used in the EQUITY III+/EPSON PC AX.
(*3) ; The difference of read/write data between SD-581L and FD1155C/MD5501 are shown in below.



(NORMAL DENSITY MODE)
SD-581L ..... T = 4 us
FD1155C/MD5501 ... T = 3.33 us

(HIGH DENSITY MODE)
SD-581L ..... T = 2 us
FD1155C/MD5501 ... T = 2 us

2.4.3 FDD Control Circuit

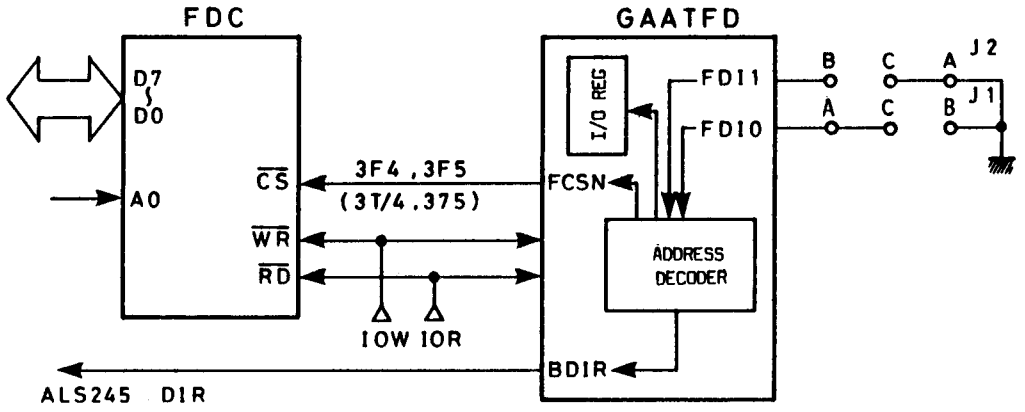


FIGURE 2-4-9. FDD CONTROL CIRCUIT I (FDD <-> CPU)

2.4.3.1 FDD Control Register Access Circuit

There are three kinds of I/O addresses on the FDD control register access circuit. They are selected by jumper pins J2 and J1. Setting of J2 and J1 are listed in CHAPTER 7.

2.4.3.2 Interrupt Signal and DMA Request Signal from FDC

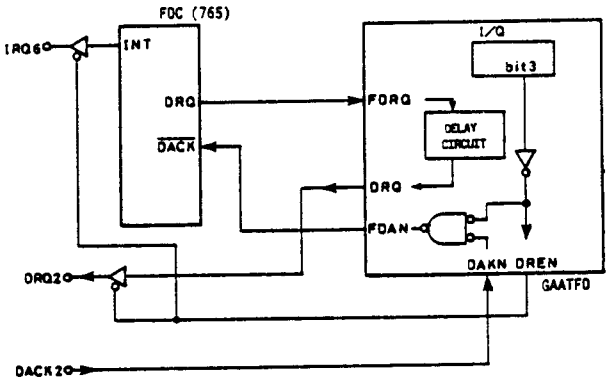


FIGURE 2-4-10. INTERRUPT SIGNAL AND DMA REQUEST SIGNAL FROM FDC

2.4.3.3 FDD Control Signals

MFM/FM signal of FDC is not used. MFM/FM is selected by a software command.

Disk Change Signal

When I/O address 3F7H or 377H is accessed, low level signal output is generated from the 3X7N terminal in the gate array GAATFD, and the disk change signal from FDD is applied to SD7 signal.

2.4.3.4 Read/Write Circuit

Write circuit

Figure 2-4-11 shows the FDD data write circuit.

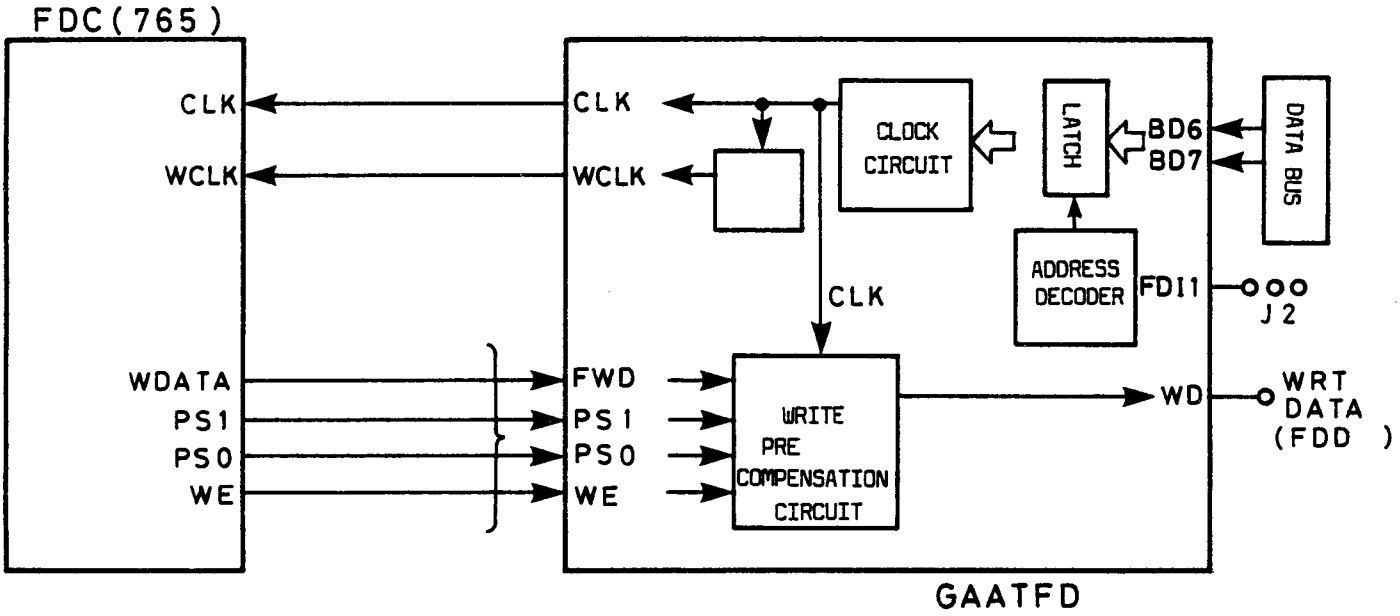


FIGURE 2-4-11. FDD DATA WRITE CIRCUIT

* FDD register of the SPFG board can select PC/AX mode and PC/AT mode by jumper switch (J2).
In case of the PC/XT mode, CLK and WCLK output generated in the gate array GAATFD is fixed.

Note: When jumper connectors J1 and J2 are set to 0,0, it is impossible to access the FDD register.

Read circuit

The VFO circuit has the following modes.

Data transmission speed

1. 500K bps mode
2. 300K bps mode
3. 250K bps mode

These modes are selected by A0, D0, D1, WR and 3XVN signals.

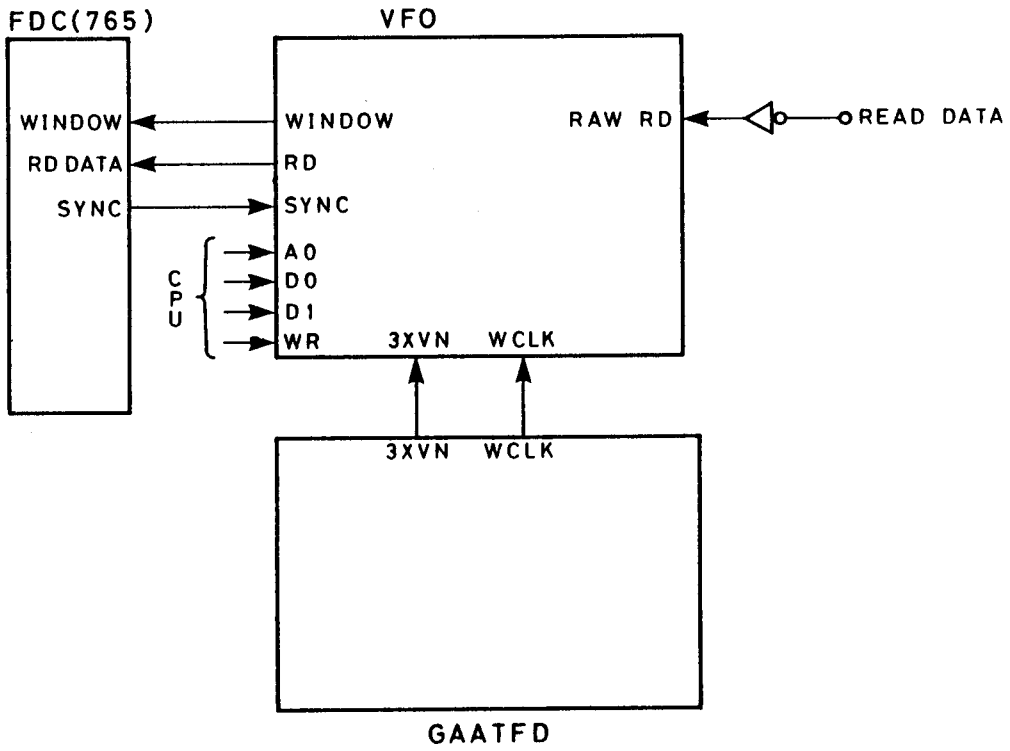


FIGURE 2-4-12. FDD DATA READ CIRCUIT

VFO circuit

The VFO circuit inputs a RAWRD signal and generates a WINDOW signal which synchronizes a REWRD signal.
When FDD is not in read operation, VFO circuit synchronizes a WCLK signal. The VFO circuit will synchronize, whether a WCLK signal or RAWRD signal is selected by SYNC signal.
(Whether the VFO circuit is synchronized with WCLK signal or RAWTD signal is selected by SYNC signal.)

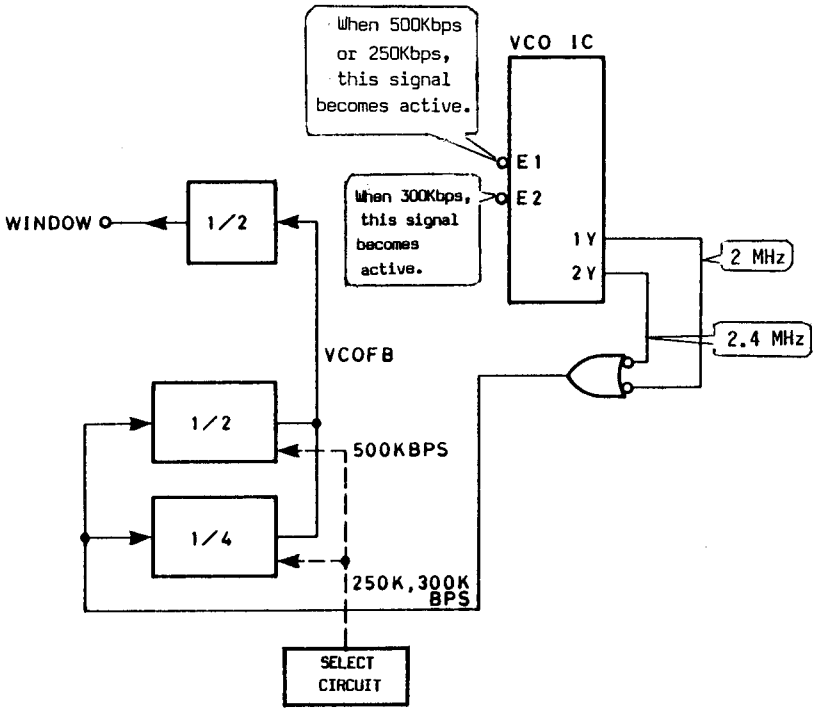


FIGURE 2-4-13. VFO WINDOW CIRCUIT

2.4.3.5 Other Functions

Terminator is attached for all FDDs. There is no need to disassemble a terminator. Because EPSON FDD uses 1K ohm terminator.

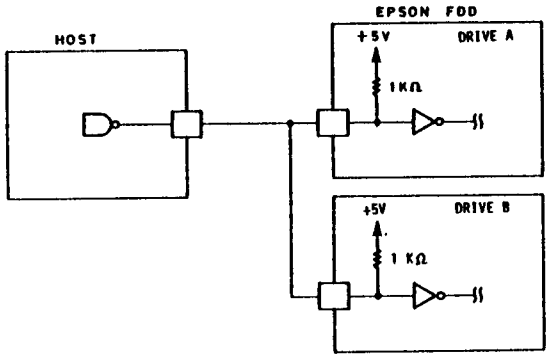


FIGURE 2-4-14. FDD TERMINATOR FUNCTION

FDD Special Signal Cable

When changing setting of floppy disk drive number (A or B), it is not necessary to change floppy disk drive jumper setting.
You can change the setting of floppy disk drive number by modification of the connections on the floppy disk drive signal cable.

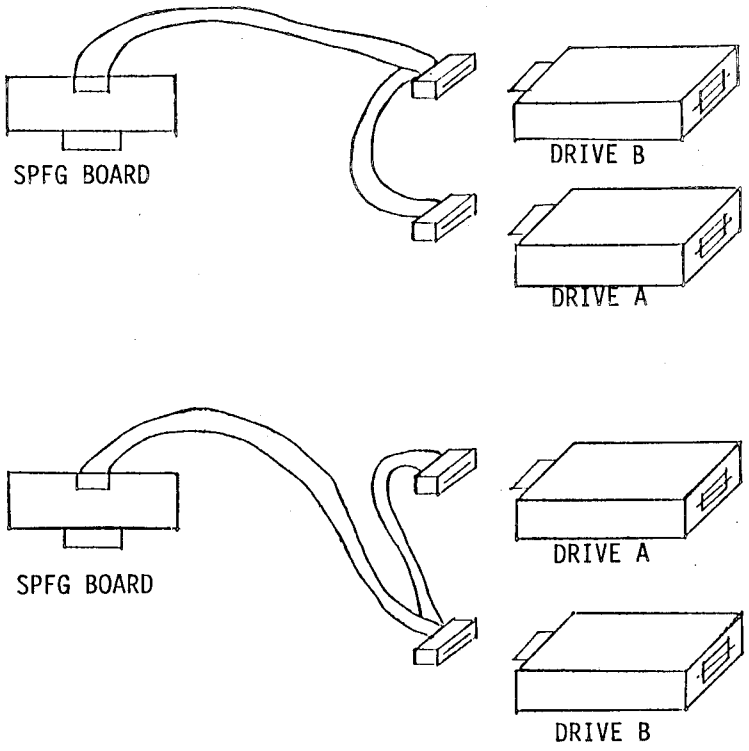


FIGURE 2-4-15. FDD CABLE SETTING

If DS1 signal output is generated at the host side, drive A is selected. If MT1 signal output is generated, motor in drive A is turned on.
If DS2 signal output is generated at the host side, drive B is selected. If MT2 signal output is generated, motor in drive B is turned on.

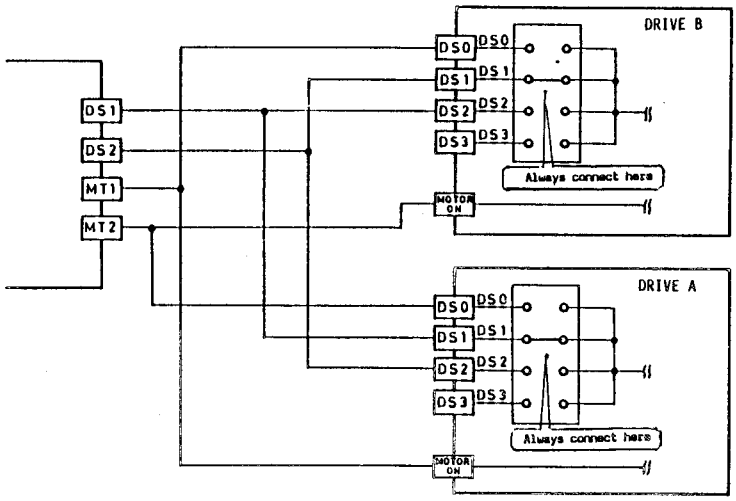


FIGURE 2-4-16. DRIVE SELECT AND MOTOR ON SIGNAL SUPPLY CIRCUIT

* Always set the drive select jumper switch to DS1 (Drive Select 1).

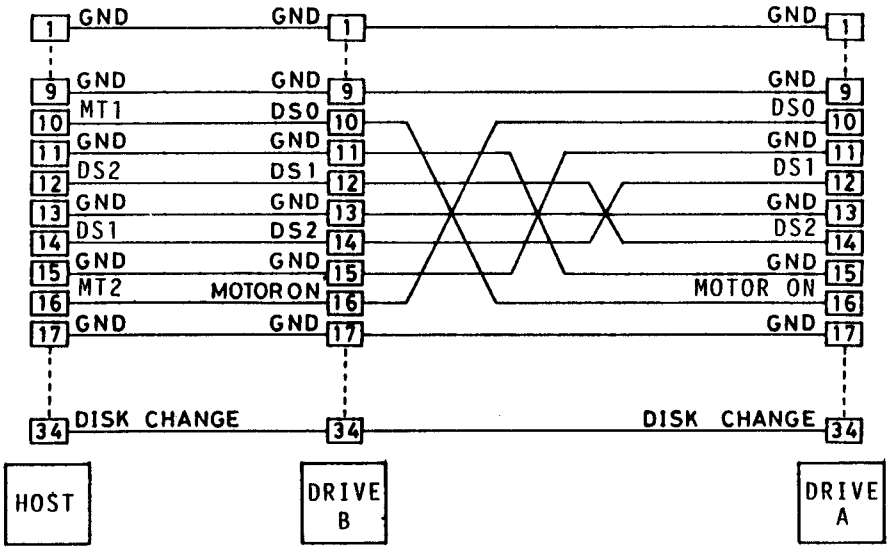


FIGURE 2-4-17. FDD SPECIAL SIGNAL CABLE

Hard Disk Drive Signal Cable

Hard disk drive signal cable is identical to the floppy disk drive signal cable. So, when changing the setting of the hard disk drive number (C or D), it is not necessary to change the hard disk drive jumper setting.
You can change the setting of the hard disk drive number by modifying the connections of the hard disk drive signal cable.

Remark

Concerning hard disk drive's terminator, they are not identical to the floppy disk drive. When you install the second hard disk drive, you must remove one terminator from drive number D.

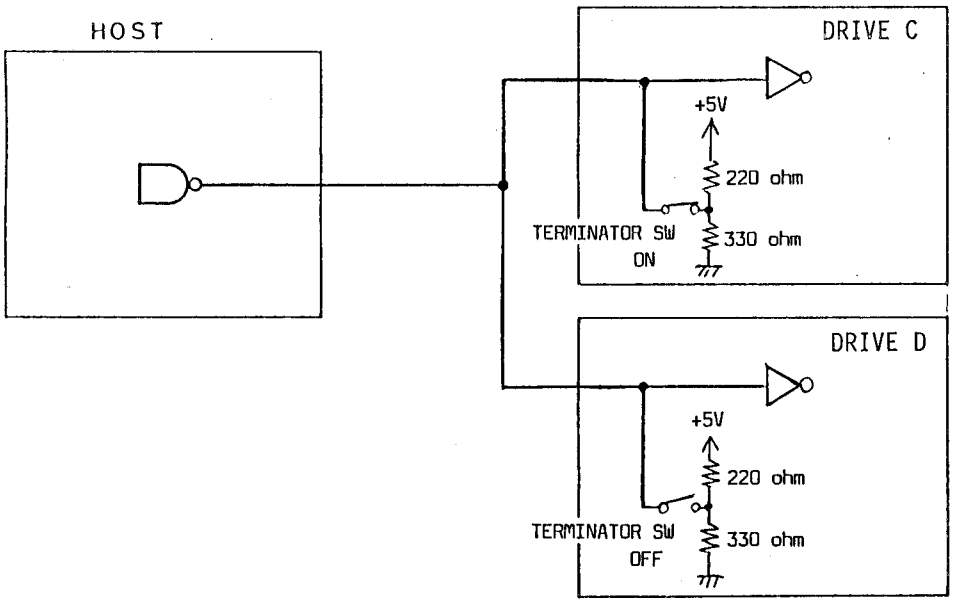
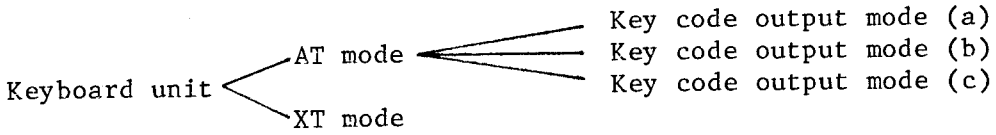


FIGURE 2-4-18. HARD DISK DRIVE SIGNAL CABLE

2.5 KEYBOARD

The keyboard unit has two operation modes. One is AT mode, the other is XT mode.
In the AT mode, there are three kinds of key code output mode.
Mode selection is performed by software.



The EQUITY III+ / EPSON PC AX system uses the key code output mode of the AT mode.

2.5.1 Block Diagram

The following diagram shows keyboard unit block diagram.

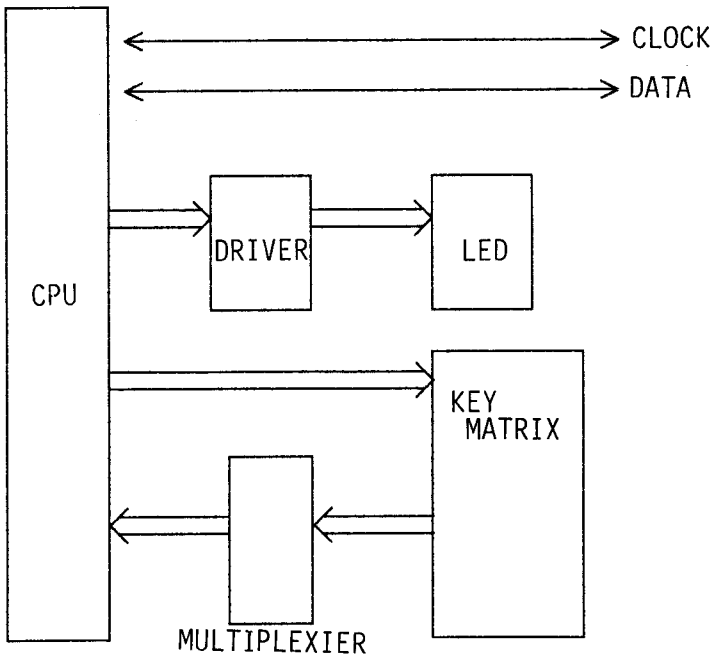


FIGURE 2-5-1. KEYBOARD UNIT BLOCK DIAGRAM

2.5.2. Interface Signal

2.5.2.1 AT mode

The Keyboard data (sent from keyboard) or the keyboard control data (sent from Host side) are communicated by using the clock pin and the data signal.

There are two modes in the keyboard interface circuit. One is interface control mode, the other is data communication mode.
In the interface control mode, the host controls operation mode of the keyboard to the host or from the host to the keyboard. At this mode, the keyboard sends clock signal to synchronize between the keyboard operation and the host side operation.

TABLE 2-5-1. INTERFACE CONTROL MODE

CLOCK	DATA	FUNCTION
H	H	Keyboard can send Data to Host side
L	H	Keyboard can't send Data to Host side
L	L	Keyboard prepares receiving Data
H	L	Keyboard starts inputting Data

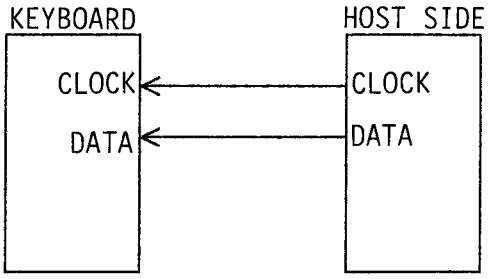
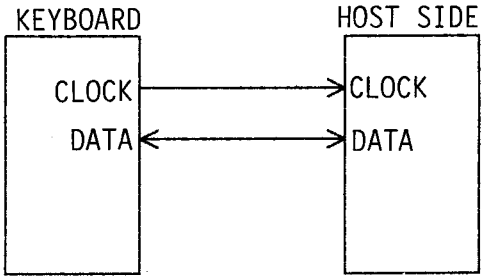


TABLE 2-5-2. DATA COMMUNICATION MODE (AT MODE)

CLOCK	Keyboard sends clock signal to synchronize between keyboard operation and Host side operation.
DATA	(1) Keyboard sends Data. (2) Host sends Data.



2.5.2.2 XT mode

TABLE 2-5-3. DATA COMMUNICATION MODE (XT MODE)

XT	CLOCK	←	Keyboard initializing signal (low active)
		→	Clock signal
	DATA	←	Keyboard Data wait signal (low active)
		→	Data signal from keyboard.

2.5.3 Description of Interface Signals (AT mode)

2.5.3.1 Clock

* Synchronous clock for transmitting and receiving keyboard data.

* The clock is generated from the keyboard.

* The transmission of data cannot take place even if the keyboard is ready to transmit when there is a low level signal (data wait) in the clock line. (data will be saved in the keyboard buffer)
  The keyboard checks the clock line during transmission of data and will stop transmission when it detects there is a low level signal.

2.5.3.2 Data

* Keyboard transmission (keyboard scan code, command code), reception code (command code) data.

* This is also the transmission request signal from the host. Once a low level signal is detected in the data line, the keyboard is ready for reception.

2.5.3.3 Keyboard Data Output (AT mode)

When the keyboard is ready to transmit data, it checks the clock and data lines for data wait or transmission request. If there are high level signals in both the clock and data lines, the keyboard determines that transmission is possible and starts transmitting. It checks the clock line during transmission and stops data transmission as soon as it detects a low level signal.

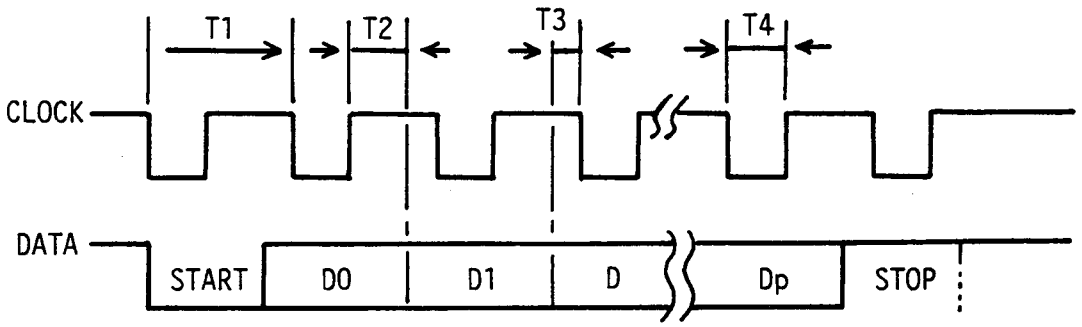
2.5.3.4 Keyboard Data Input (AT mode)

When the keyboard detects a low level signal in the data line it becomes ready to receive.
Then the signal in the host clock line drops to a low level below 60 us, which will stop keyboard transmission.
When the keyboard detects a high level in the clock line, data reception is performed (counts off each group of 11 bits). After receiving the 10th bit, the keyboard changes the signal in the data line to low level and receives one more bit (the stop bit). The low level signal of the 11th bit tells the host that the data has been received.

2.5.3.5 Data Transmission Method and Data Format

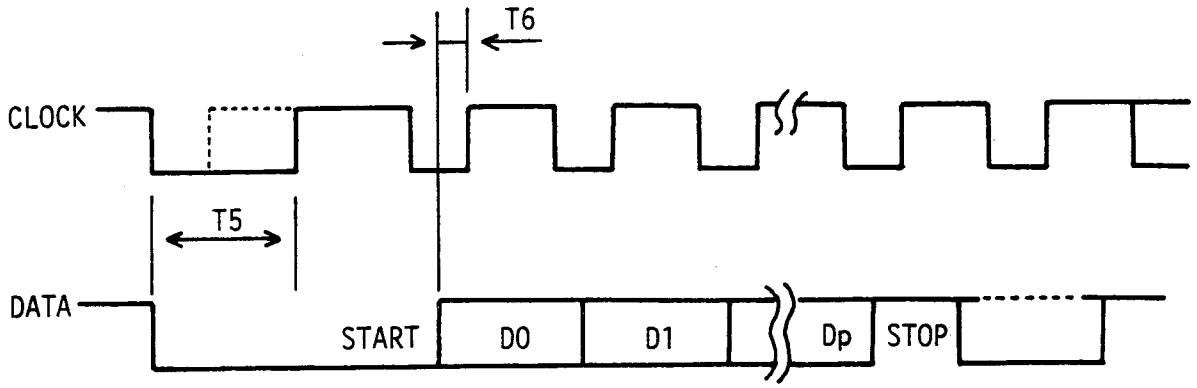
TABLE 2-5-4. DATA TRANSMISSION METHOD AND DATA FORMAT

(1) Transmission method	Synchronous serial transmission	Synchronous serial transmission
(2) Transmission rate	≒ 9600 BPS	≒ 9600 BPS
(3) Start bit	1	1
(4) Stop bit	1	1
(5) Data length	8 bit	8 bit
(6) Parity	Odd parity	None



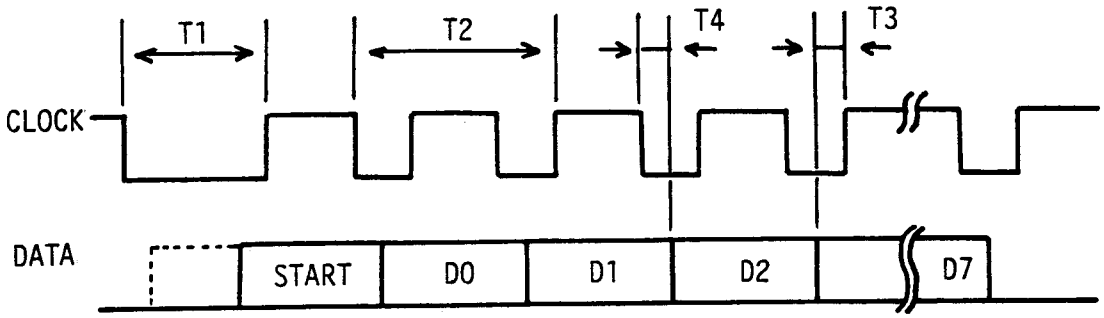
T1 ; 104 us ±20%
T2 ; 20 us Min
T3 ; 20 us Min
T4 ; 35 us ±20%

FIGURE 2-5-2. KEYBOARD DATA OUTPUT - AT MODE



T5 ; 60 us Min (Host data output ready time)
T6 ; 5 us Min

FIGURE 2-5-3. KEYBOARD DATA INPUT - AT MODE



T1 ; 100 - 250 us (Data output possibility
T2 ; 104 us ±20% check time)
T3 ; 10 us Min
T4 ; 10 us Min

FIGURE 2-5-4. KEYBOARD DATA OUTPUT - XT MODE

2.5.4 Interface Circuit Specification

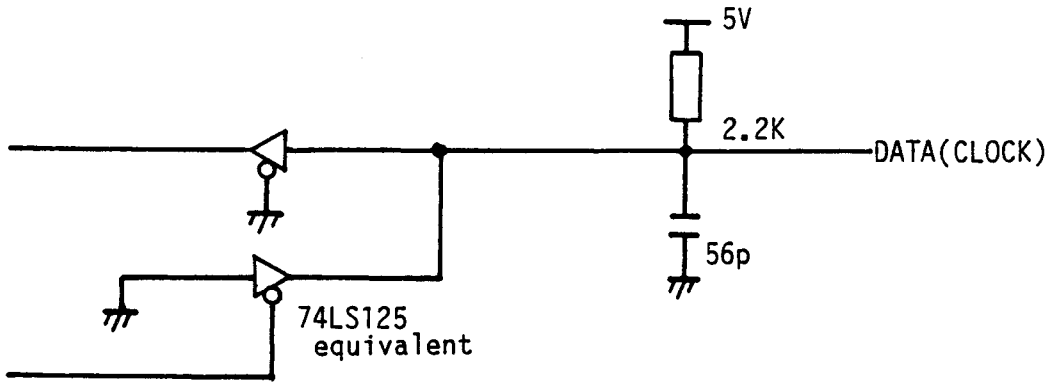


FIGURE 2-5-5. INTERFACE CIRCUIT

2.5.5 Connector Pin Explanation

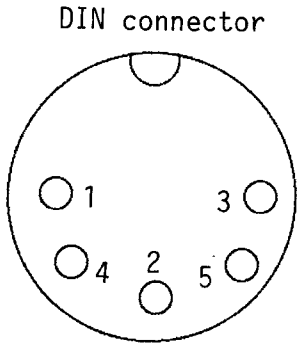


FIGURE 2-5-6. KEYBORAD CONNECTOR PIN LOCATIONS

TABLE 2-5-5. KEYBOARD CONNECTOR PIN FUNCTION

PIN NUMBER	SIGNAL NAME
1	Clock
2	Data
3	N.C.
4	Ground
5	+5V DC
-	Ground

2.5.6 Function Specifications

2.5.6.1 Stroke Characteristics

At N key roll over (with diode)

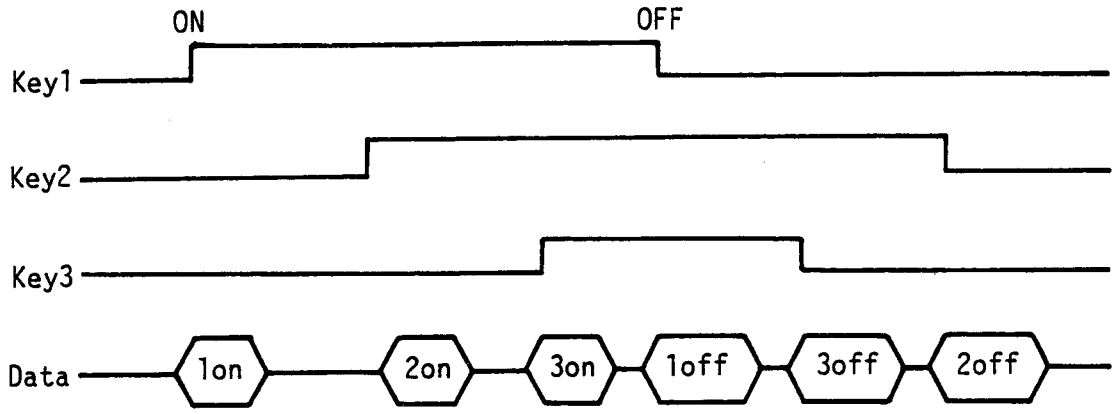


FIGURE 2-5-7. STROKE CHARACTERISTICS

2.5.6.2 Typematic Function

A key scan code is transmitted as long as a key is depressed. (Transmission intervals for all keys except the F16 (Pause) key depend on the typematic rate/delay (command assignment). When any of the other keys are pressed, it enters a new typematic cycle.

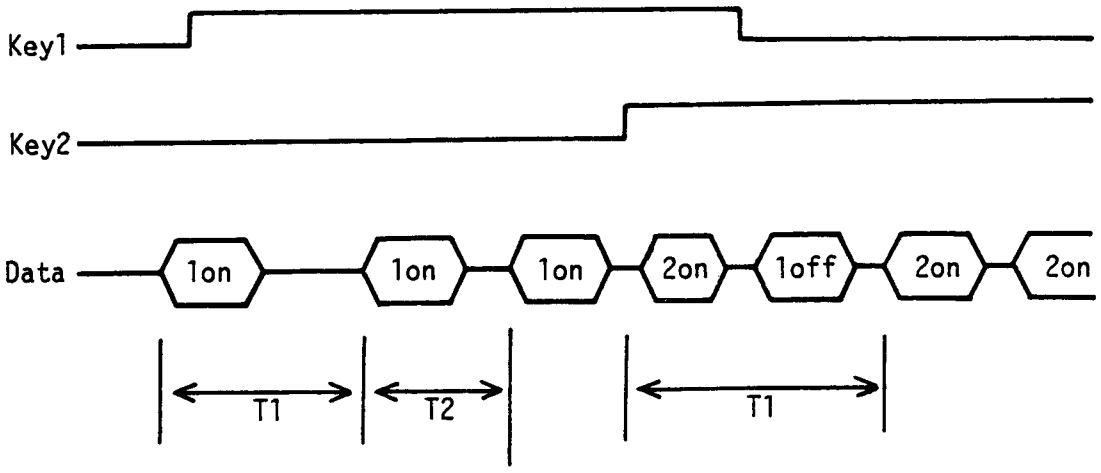


FIGURE 2-5-8. TYPEMATIC FUNCTION

TABLE 2-5-6. TRANSMISSION INTERVALS

	AT MODE	XT MODE
T1	250 - 1000 ms (default)	500 ms
T2	1/2 - 1/3 sec (default)	92 ms

The typematic function will be disabled when a clock line is low level.

2.5.6.3 Keyboard Buffer

When a key is pressed (released) before the code of a key pressed earlier has been transmitted during the key data out phase, the code of the no transmitted key is saved in this buffer until it is transmitted.
The buffer can save codes for 16 keys (16 make or break data).
The 17th code will be substituted by an overrun code.
However, no substitution will take place if there is an overrun code in the buffer.
Break codes and make codes when a key is depressed will not be lost even during an overrun.
However, they will be cancelled by a buffer clear command.
The overrun code is different between mode and mode below.

TABLE 2-5-7. OVERRUN CODES

KEY CODE OUTPUT MODE	(a)	(b)	(c)
AT mode	FF	00	00
XT mode		FF	

2.5.6.4 Power On Reset (AT mode)

When the power is turned on the keyboard logic performs a power on reset.

(1) Following the power on reset, a self-test program is performed.

- ROM check sum self-test program
- RAM check self-test program

(2) After the test, the keyboard turns off the mode indicator display (3 LED's) and transmits the end code of the self-test program.

- "AAH" : operated correctly
- "FCH" : operated abnormally (scanning is stopped after transmission of the end code.)

(3) When the operation normal end code (AAH) has been transmitted and the keyboard detects a low level signal longer than 10 us in the data line 5 us after from following edge of the stop bit, the keyboard enters the XT mode.

(4) In AT mode, the typematic rate/delay time and key code output mode will be set according to mode (b).

. Rate : 10.9 CPS (92 ms) Default
. Delay : 500 ms Default

2.5.6.5. Initializing (XT mode)

The clock line is checked in 10 ms cycles by keyboard and initializing is performed as soon as a low level signal is detected.

(1) Key scan memory clear

(2) Buffer (FIFO) clear

(3) Self-test program performed

. ROM sum check self-test program
. RAM check self-test program

(4) Transmission of self-test program end code

. "AAH" : Operated correctly
. "FCH" : Operated abnormally (scanning is stopped after transmission of the end code.)

2.5.6.6 Data Wait Function (XT mode)

When the start bit is set, the data line is checked by the keyboard and if a low level signal (longer than 250 us) is detected in the data line, data transmission will not take place.

2.5.6.7 Mode Indicator (3 LED's) Display (XT mode)

Basic Operation

(1) By pressing the Scroll Lock, Numeric Lock and Caps Lock keys each indicator are displayed alternatively (performed after the end of key code transmission).

(2) All displays are turned off during power on reset and initializing.

(3) The alternative operation does not take place when the control (Ctrl) key is pressed.

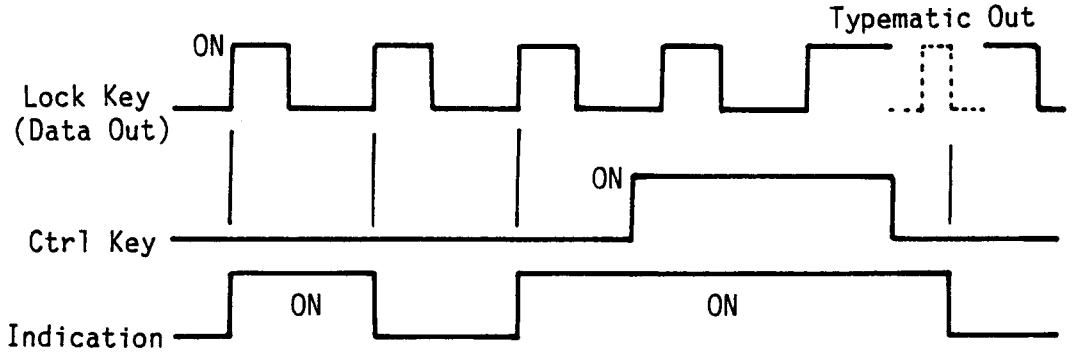


FIGURE 2-5-9. BASIC OPERATION OF MODE INDICATOR DISPLAY

Special Operations (For Germany and French)

By pressing the Caps key, Caps Lock indicator becomes on (light). By pressing the shift key, Caps Lock indicator becomes off (Not light).

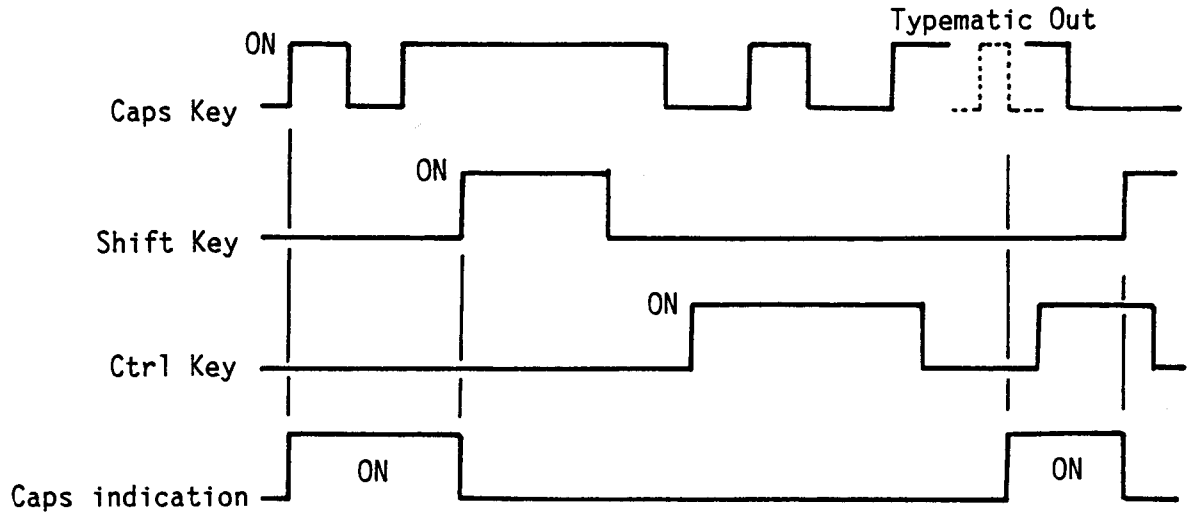


FIGURE 2-5-10. SPECIAL FUNCTIONS OF MODE INDICATOR DISPLAY

2.5.7 Key Scan Code

2.5.7.1 key Code Output (AT Mode)

In AT mode, there are three output modes : (a),(b) and (c)

Key code output in mode (a) and (b)

(1) Key code make up
The table below shows the codes allocatted to each key.

TABLE 2-5-8. KEY CODE MAKE UP

TITLE	KEY POSITION	MAKE CODE (*1) MODE (b)	MAKE CODE (*1) MODE (a)	BREAK CODE (*2) MODE (b)	BREAK CODE (*2) MODE (a)
General Keys	Other	x	x		
	A09,B20,A12	E0 + x	E0 + x		
Extension Key -1	A,D,E14 - E16 B15	E0 + x	E0 + x	Make code is substituted by "F0 + x"	"80" is added to make code "x" (OR)
Extension Key -2	E18	E0 + x	E0 + x		
Extension Key -3	F14	E0 + x	E0 + x		
Shift Key	B00,B11	x	x		
Special Key	F16(Pause)	8 bytes	6 bytes	No key code output	

NOTE : (*1) ; Make code (When key is depressed)
(*2) ; Break code (When key is released)

Note 1 : The "x" code indicates scan code data. (Refer to Table 2-5-22)

Note 2 : The F14 and 16 keys can generate other codes if used in combination with other keys. (Refer to section 2.5.7.1)

(2) Shift function

a) Numeric lock
The table below shows the conditions for setting and releasing the numeric lock.

TABLE 2-5-9. CONDITION FOR SETTING AND RELEASING NUMERIC LOCK

Setting	When the E17 (Num lock) is pressed and the make code has been transmitted or when the Num Lock LED been lit by a host command while the numeric lock is in released status.
Released	When the E17 key (Num lock) is pressed and the make code has been transmitted or when the Num Lock LED has been turned off by a host command while the numeric lock is in set status.

Note 1 : When the A00 or the A12 key (Ctrl) are pressed, it is not possible to perform setting or releasing with the Numlock key. (Setting and releasing cannot be performed even if the Ctrl key is released first.)

b) Extension Left and Right shift key code transmission

i) The table below shows the key stroke conditions for transmission of extension left and right shift codes.

TABLE 2-5-10. KEY STROKE CONDITION

N-LOCK	EXTENSION SHIFT SETTING	EXTENSION SHIFT RELEASE
NOT N.LOCK	Extension shift off code is transmitted when extension key-1 (or extension key-2) is pressed after the shift key has been pressed. In case of pressing extension key-2, same operation is performed even though N.LOCK mode.	(1) Extension shift on code is transmited when extension key-1 (or extension key-2) is released. (2) Extension shift on code is transmitted when other keys are pressed.
N.LOCK	Extension Left shift on code is transmitted when extension key-1 (or extension key-3) is pressed after the shift key has been pressed. In case of pressing extension key-3, same operation is performed even though NOT N.LOCK mode.	(1) Extension Left shift off code is transmitted when extension key-1 (or extension key-3) is released (2) Extension Left shift off code is transmitted when other keys are pressed.

ii) Extension left and right shift codes are as follows.

TABLE 2-5-11. EXTENSION LEFT AND RIGHT SHIFT CODES

TYPE	MODE (b)	MODE (a)
Extension Left Shift on code	E0 + 12	E0 + 2A
Extension Left Shift off code	E0 + F0 + 12	E0 + AA
Extension Right Shift on code	E0 + 59	E0 + 36
Extension Right Shift off code	E0 + F0 + 59	E0 + B6

iii) Transmission sequence of left and right codes are as follows.

TABLE 2-5-12. TRANSMISSION SEQUENCE OF LEFT AND RIGHT CODES KEY

CONDITION		TRANSMISSION SEQUENCE
Extension Shift Setting		EXS ----> x
Extension Shift Release	When extension Shift setting key is OFF	x ----> EXS
	When other keys are ON	EXS ----> x

Note : "x" : Key data
"EXS": Extension Left and right shift codes

(3) Special operations generated by a combination of keys

a) The codes shown in the table below are transmitted when the F16 (Break) key is pressed while either the A00 (left Ctrl) or the A12 (right Ctrl) key is also pressed.

TABLE 2-5-13. TRANSMITTED CODE OF F16(BREAK) KEY

MODE (b)	E0 + 7E + E0 + F0 + 7E
MODE (a)	E0 + 46 + E0 + C6

Note : No code below are transmitted when the F14 (Sys Rq) key is pressed while the [A01 (left Alt), the A09 (right Alt)] and the [A00 (left Ctrl), A12 (right Ctrl)] key or the B00 (Left shift) and B11 (right shift) keys.

(4) Key code output during typematic operation
All keys except the F16 (pause) key are typematic keys whose make codes are transmitted at specified intervals.

TABLE 2-5-14. TRANSMITTED CODE OF F14(Sys Rq) KEY

MODE	WHEN A00, A12 KEY OR B00, B11 KEYS ARE DEPRESSED		WHEN A01, A09 KEYS ARE DEPRESSES	
	MAKE	BREAK	MAKE	BREAK
(b)	E0 + 7C	E0 + F0 + 7C	84	F0 + 84
(a)	E0 + 37	E0 + B7	54	D4

Key Code Output in Mode (c)

(1) Transmission of make codes (when keys are pressed)
A one byte make code is transmitted when a key is pressed (refer to scan code table).

(2) Transmission of break codes (when keys are released)
The A00 (left Ctrl), the A01 (left Alt), the B00 (left shift), the B11 (right shift) and the C00 (Caps) keys transmit break codes when a key is released. The break code is "F0 + make code".

(3) Key code output during typematic operation
The A04, A14-A16, B01-B10, B15, C01-C12, D00-D14, E00-E13, D20,E13', C12', B11', B00' and D20' keys are typematic keys whose make codes are transmitted at specified intervals when pressed repeatedly.

(4) The break code transmission keys in (2) and the typematic keys in (3) above are set during default and all keys can be set with the commands described below.

2.5.7.2 Key Code Output (XT Mode)

The Key code outputs are performed according to the same conditions that prevail in key code mode (a) during AT mode (including shift function).

2.5.8 COMMANDS (AT mode)

2.5.8.1 Commands From the Host Side

These are commands received by the keyboard which it responds to within 20 ms.

TABLE 2-5-15. KEYBOARD COMMANDS (AT MODE)

COMMAND	DATA (HEX)	BUFFER CLR	LED SET
RESET	FF	O	O
RESEND	FE	-	-
TYPEMATIC KEY RESET 1,2	FC,FD	O	-
TYPEMATIC KEY SET	FB	O	-
ALL KEY TYPEMATIC CONTROL	FA-F7	O	-
SET DEFAULT	F6	O	-
DEFAULT DISABLE	F5	O	-
ENABLE	F4	O	-
SET TYPEMATIC RATE/DELAY	F3	-	-
READ KEYBOARD ID	F2	-	-
SET/READ KEY CODE MODE	F0	O	-
ECHO	EE	-	-
SET/RESET MODE INDICATORS	ED	-	O

(1) Reset
The keyboard recognizes this command with the acknowledge (ACK) command. When reception of the ACK command has been confirmed (confirmation is mode when both the clock and data line signals exceed 500 us high) a reeset operation indentical with the power on reset is performed. (Except for XT mode switching operation)

(2) Resend
The keyboard repeats the transmission of end data transmitted when recives a resend command.

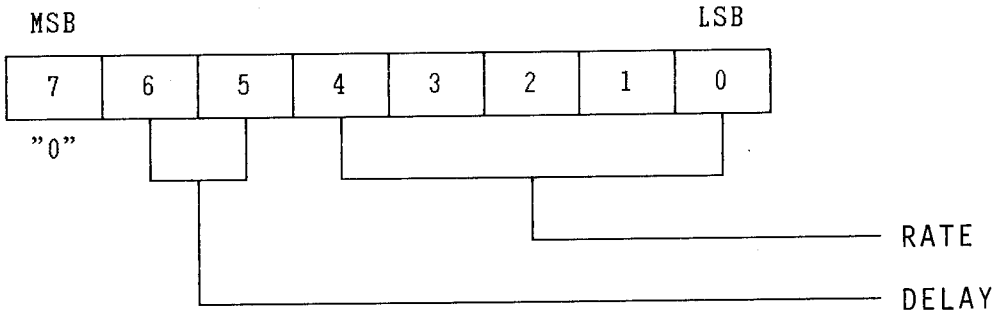
(3) Set default
The keyboard responds with an ACK command and continues scanning after the output buffer has been cleared and the default condition has been set.

(4) Default disable
The keyboaed stops scanning and except that it waits for a command it behaves as during a set default command.

(5) Enable
The keyboard acknowledges to the host side with and ACK command and clears the output buffer. Then starts scanning.

(6) Set typematic Rate/Delay
This command is made up of a 2-byte command and parameter.
The keyboard responds to the ACK command, stops scanning and waits for the parameter. Then the keyboard responds to the parameter with an ACK command, sets the rate and delay shown in the figure below and starts scanning (when proceeded as an Enable). If a command is received instead of a parameter, the current rate remains unchanged and keyboard stops this command operation, then the new command is performed and scanning starts.

TABLE 2-5-16. TYPEMATIC RATE/DELAY



1) DELAY

BIT 6	BIT 5	DELAY (ms)
0	0	250
0	1	500
1	0	750
1	1	1000

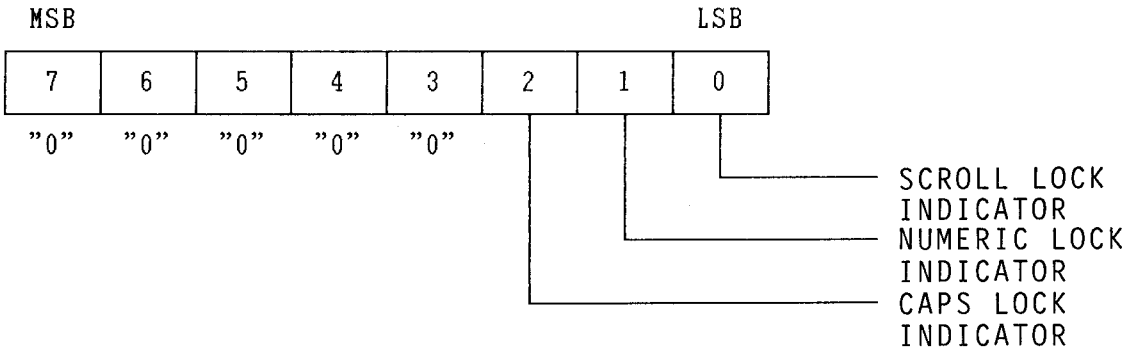
2) RATE

BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RATE (cps)
0	0	0	0	0	30.0
0	0	0	0	1	26.7
0	0	0	1	0	24.0
0	0	0	1	1	21.8
0	0	1	0	0	20.0
0	0	1	0	1	18.5
0	0	1	1	0	17.1
0	0	1	1	1	16.0
0	1	0	0	0	15.0
0	1	0	0	1	13.3
0	1	0	1	0	12.0
0	1	0	1	1	10.9
0	1	1	0	0	10.0
0	1	1	0	1	9.2
0	1	1	1	0	8.6
0	1	1	1	1	8.0
1	0	0	0	0	7.5
1	0	0	0	1	6.7
1	0	0	1	0	6.0
1	0	0	1	1	5.5
1	0	1	0	0	5.0
1	0	1	0	1	4.6
1	0	1	1	0	4.3
1	0	1	1	1	4.0
1	1	0	0	0	3.7
1	1	0	0	1	3.3
1	1	0	1	0	3.0
1	1	0	1	1	2.7
1	1	1	0	0	2.5
1	1	1	0	1	2.3
1	1	1	1	0	2.1
1	1	1	1	1	2.0

(7) Echo
The keyboard transmits a code "EE" response and continues scanning (when preceeded as an Enable).

(8) Set/Reset mode indicators
This command is made up of a 2-byte command and an option. The keyboard responds to the host side with and ACK command and waits for sending of the option. Then keyboard responds to the option, sets the indicator and starts scanning (when proceeded as an Enable). If it receives another command instead of the option, the indicator condition remains unchanged and the keyboard stops, this command operation. Then proceeds the new command and starts scanning.

TABLE 2-5-17. OPTION REGISTER FOR KEYBOARD



(9) Read Keyboard ID
The keyboard responds with the ACK command, transmits a 2-byte data ; "AB" + "83"

(10) Set/Read key code mode
This command is made up of a 2-byte command an option. The keyboard responds to the host side with an ACK command stops scanning and waits for the option. When keyboard inputs option, it responds to the host side with an ACK command, starts scanning after setting key code mode or transmission status. (When proceeded as an Enable.) If it receives another command instead of the option, processing of this command is cancelled, the new command is proceeded and scanning starts.

i) Read key code mode starts (option data "00")
The keyboard transmits the current keycode mode status. (1 byte)

TABLE 2-5-18. KEY CODE MODE STATUS

KEY CODE MODE	TRANSMITTING DATA
(a)	01
(b)	02
(c)	03

ii) Set key code mode (option data : "01"-"03")
The keyboard is set to specified key code mode depending on the option data.

TABLE 2-5-19. KEY CODE MODE ON OPTION DATA

OPTION DATA	KEY CODE MODE
01	(a)
02	(b)
03	(c)

(11) Typematic key set
This command is made up of a command and an option (Max 4 or 5 bytes). The keyboard responds to this command with an ACK command, stops scanning and responds to the option with an ACK command. In the key code mode (c), this command sets the typematic function and cancels break code transmission for keys waiting for the key scan codes that correspond to the option data. When the command has been proceeded, scanning stops and remains in that condition.

(12) Typematic key reset 1 ("FC")
This command releases the typematic function and sets transmission of the break code for keys waiting for key scan codes corresponding to option data. Other details are the same as described in the case of typematic key set above.

(13) Typematic key reset 2 ("FD")
This command releases the typematic function and cancels transmission of the break code for keys waiting for key scan codes corresponding to the option data. Other details are the same as described in the case of Typematic key set above.

(14) All key typematic control
The keyboard responds to this command with an ACK command cancels or sets the typematic function and break code transmission and continues scanning (when proceeded as an Enable.)

TABLE 2-5-20. ALL KEY TYPEMATIC CONTROL

COMMAND DATA	TYPEMATIC FUNCTION	BREAK CODE TRANSMISSION	REMARKS
FA	Setting	Setting	Applied for
F9	Cancel	Cancel	only key
F8	Cancel	Setting	code mode
F7	Setting	Cancel	(c).

2.5.8.2 Commands To Host Side

These are commands transmitted to the host side by the keyboard.

TABLE 2-5-21. COMMANDS TO THE HOST SIDE

COMMAND	DATA (HEX)
Resend	FE
ACK	FA
Overrun	**
Break Code Prefix	F0
BAT Completion	AA
Echo Response	EE
Read Keyboard ID	AB + 83
Read Key Code Mode	Mode (a) + 01
	Mode (b) + 02
	Mode (c) + 03

** : Key Code Mode (a) ..... FF
Key Code Mode (b),(c) .. 00

(1) Resend
The keyboard generates a resend command when it receives an invalid input or invalid parity input.

(2) ACK
The keyboard outputs an ACK response for valid inputs that do not generate echo or resend commands. If an interrupt is issued to the keyboard when an ACK command is being transmitted, transmission is terminated and the new command is responded to.

(3) Break code prefix
This command announces that a key has been released and sends the first byte of a 2-byte message. (Corresponds to key code mode (b) and (c).)

(4) Overrun
The overrun character is in the 17th position of the keyboard buffer and when the buffer becomes full, the character is stacked on the last code. When this code comes first in the buffer it is output as an overrun error.

(5) Bat completion code
When BAT is completed normally, the keyboard outputs an "AA" response. "FC" or other code indicates that the keyboard microprocessor is malfunctioning.

(6) Echo response
This command is transmitted in response to an echo command from the host side.

(7) Read keyboard ID
This command is transmitted in response to an equipment ID data read command from the host side.

(8) Read key code mode
This command transmits current keycode mode status in response to a key code mode read command from the host side.

TABLE 2-5-22. KEY SCAN CODE LIST

KEY NO.	MODE(a)	MODE(b)	MODE(c)	KEY NO.	MODE(a)	MODE(b)	MODE(c)
F00	01	76	08	E13(*2)	7D	6A	5D
F02	3B	05	07	E14	E0,52	E0,70	67
F03	34	06	0F	E15	E0,47	E0,6C	6E
F04	3D	04	17	E16	E0,49	E0,7D	6F
F05	3E	0C	1F	E17	45	77	76
F06	3F	03	27	E18	E0,35	E0,4A	77
F07	40	0B	2F	E19	37	7C	7E
F08	41	83	37	E20	4A	7B	84
F09	42	0A	3F	D00	0F	0D	0D
F10	43	01	47	D01	10	15	15
F11	44	09	4F	D02	11	1D	1D
F12	57	78	56	D03	12	24	24
F13	58	07	5E	D04	13	2D	2D
F14	E0,37	E0,7C	57	D05	14	2C	2C
F15	46	7E	5F	D06	15	35	35
F16	**	**	62	D07	16	3C	3C
E00	29	0E	0E	D08	17	43	43
E01	02	16	16	D09	18	44	44
E02	03	1E	1E	D10	19	4D	4D
E03	04	26	26	D11	1A	54	54
E04	05	25	25	D12	1B	5B	5B

E05	06	2E	2E	D13(*3)	2B	5D	5C
E06	07	36	36	D14	E0,53	E0,71	64
E07	08	3D	3D	D15	E0,4F	E0,69	65
E08	09	3E	3E	D16	E0,51	E0,7A	6D
E09	0A	46	46	D17	47	6C	6C
E10	0B	45	45	D18	48	75	75
E11	0C	4E	4E	D19	49	7D	7D
E12	0D	55	55	D20	4E	79	7C
E13	0E	66	66	D20'	7E	6D	7B
C00	3A	58	14	B06	31	31	31
C01	1E	1C	1C	B07	32	3A	3A
C02	1F	1B	1B	B08	33	41	41
C03	20	23	23	B09	34	49	49
C04	21	2B	2B	B10	35	4A	4A
C05	22	34	34	B11	36	59	59
C06	23	33	33	B11'(*2)	73	51	51
C07	24	3B	3B	B15	E0,48	E0,75	63
C08	25	42	42	B17	4F	69	69
C09	26	4B	4B	B18	50	72	72
C10	27	4C	4C	B19	51	7A	7A
C11	28	52	52	B20	E0,1C	E0,5A	79
C12	1C	5A	5A	B20'(*2)	78	63	78
C12'(*1)	2B	5D	53	A00	1D	14	11
C17	4B	6B	6B	A01	38	11	19
C18	4C	73	73	A05	39	29	29
C19	4D	74	74	A09	E0,38	E0,11	39
B00	2A	12	12	A12	E0,1D	E0,14	58
B00'(*1)	56	61	13	A14	E0,4B	E0,6B	61
B01	2C	1A	1A	A15	E0,50	E0,72	60
B02	2D	22	22	A16	E0,4D	E0,74	6A
B03	2E	21	21	A17	52	70	70
B04	2F	2A	2A	A17'(*2)	7C	68	68
B05	30	32	32	A19	53	71	71

** F16key code mode (a) ; E1,1D,45,E1,9D,C5
mode (b) ; E1,14,77,E1,F0,14,F0,77

For U.S.A. (*1) keys and (*2) keys are not installled.
For Europe (*2) keys and (*3) key are not installed.

CHAPTER

3

OPTIONS

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4

TROUBLESHOOTING

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4.1 Service Tools

Recommended service tools are listed in Table 4-1-1 with corresponding EPSON part numbers; these are also commercially available.

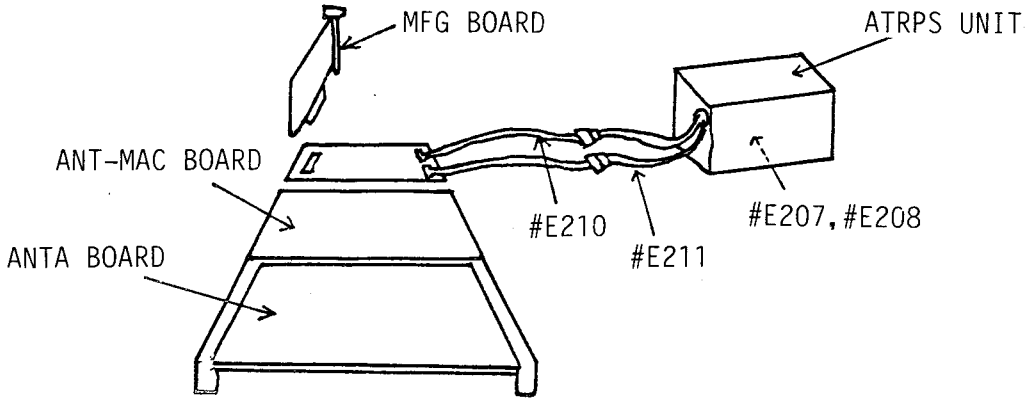


FIGURE 4-1-1. CONNECTION OF SERVICE TOOLS

TABLE 4-1-1. SERVICE TOOL LISTING

TOOLS NO.	PART NO.	DESCRIPTION
ANT-MAC BOARD	B778601601	Expansion board for the main control board.
MFG BOARD	B778601701	Bus status check board.
CABLE #E207	B778601801	Expansion for CN3 of the ATRPS unit.
CABLE #E208	B778602001	Expansion for CN4 of the ATRPS unit.
CABLE #E210	B778602001	Expansion for DC1 of the ATRPS unit.
CABLE #E211	B778602101	Expansion for DC2 of the ATRPS unit.
CABLE #E212	B778602201	Expansion for CN3 of the ANTA board.

4.2 TROUBLESHOOTING

The BIOS ROMs in the EQUITY III+ / EPSON PC AX computer system are including a diagnostic program which will perform the check for internal computer system automatically.
We call the test program "POD" (Power On Diagnostics).
The POD will output ERROR MESSAGE to the CRT screen or eight LEDs on the MFG Board if error is occurred in the EQUITY III+ / EPSON PC AX computer system.

The error message will be useful at repair because we can determine the probable cause by using this error message.

4.2.1 How to Use the POD (Power on diagnostics)

1. Connect a monitor and a MFG Board to the EQUITY III+ / EPSON PC AX computer system.
2. Turn the power switch of the EQUITY III+ / EPSON PC AX. The POD will start automatically and check internal circuits step by step automatically.
3. When error is occurred, the error message will appair on the monitor screen or LEDs of the MFG board.
   (The POD does not show good message when no error)
4. Search the 'RESPONSE AND INFORMATION FOR ERRORS' and find the corresponding probable cause yourself.

4.2.2 How to Use the MFG Board

1. Function of the MFG board.
   The MFG board is a service tool which can display data status (data bus bit 0 to bit 7) on the eight LEDs.
   This board can display data status of I/O address 000(H) to FFF(H).
   We can select the I/O address by using DIP switch.

2. How to set the DIP switch
   Each switches of the DIP switch are corresponding to address bus A0 to A11 as follows.

DIP SWITCH	SW2 8	7	6	5	4	3	2	1	SW1 4	3	2	1
CORRESPONDING ADDRESS	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

* When setting the DIP switch, please use following instance.

INSTANCE 1 : In case of setting the DIP switch to I/O address 80H.

DIP SWITCH	SW2 8	7	6	5	4	3	2	1	SW1 4	3	2	1	
CORRESPONDING ADDRESS	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
SETTING OF THE DIP SW	ON	ON	ON	ON	OFF	ON	ON	ON	ON	ON	ON	ON	
VALUE OF ADDRESS BUS	0	0	0	0	1	0	0	0	0	0	0	0	
		(0)				(8)				(0)			=080H

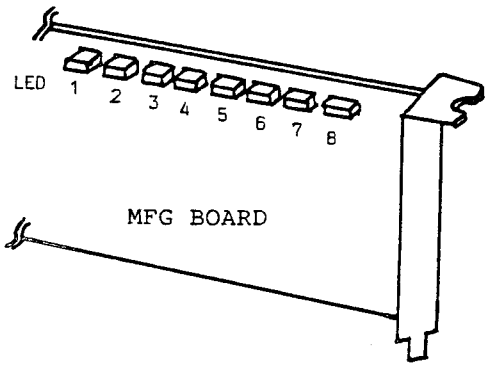
INSTANCE 2 : In case of setting the DIP switch to I/O address 177H.

DIP SWITCH	SW2 8	7	6	5	4	3	2	1	SW1 4	3	2	1	
CORRESPONDING ADDRESS	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
SETTING OF THE DIP SW	ON	ON	ON	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	
VALUE OF ADDRESS BUS	0	0	0	1	0	1	1	1	0	1	1	1	
		(1)				(7)				(7)			=177H

3. How to use the MFG board
   Install the MFG board to an option slot connector of the computer system.

4. Meaning of the LEDs

   * When the LED light, corresponding data bus is high status.



LED NO.	MEANING
LED 1	DATA BUS BIT 7
LED 2	DATA BUS BIT 6
LED 3	DATA BUS BIT 5
LED 4	DATA BUS BIT 4
LED 5	DATA BUS BIT 3
LED 6	DATA BUS BIT 2
LED 7	DATA BUS BIT 1
LED 8	DATA BUS BIT 0

4.3 RESPONSE AND INFORMATION FOR ERRORS

4.3.1 Outline

The power on diagnostics (called POD) of EQUITY III+ / EPSON PC AX ROM BIOS diagnoses the system status held when EQUITY III+ / EPSON PC AX is initiated and takes action according to the status.

4.3.2 POD Functions

POD has the following four functions:

1; POD halts the system to disable initiation if POD detects a serious error while checking system hardware.

2; If POD detects an error that is not fatal to the system, POD displays the error message on the CRT screen and I/O address 80H. Then makes the system wait for initiation until a specific key is pressed.

3; If a serious error occurs (refer to function 1), POD displays an error message on the CRT screen in addition to I/O address 80H.

4; In reference to a non fatal error (function 2), POD skips the specific key input wait status.

4.3.3 Explanation of the POD Functions

1; Checking system hardware (serious error)

See the table 4-2. (Responses and information for errors)

2; Checking system hardware (not fatal)

See the table 4-2. (Responses and information for errors)
The specific key is the F1 key.

3; Displaying an error message on the CRT screen and I/O address 80H.

See the table 4-2. (Responses and information for errors)

4; Skipping specific key input wait status

The key input wait request for an error specified in CMOS RAM 3EH and 3FH is skipped if a specific pattern is defined in CMOS RAM 34H to 3DH.

4.3.4 Specific Pattern in 34H to 3DH

Pattern

Specification in 3EH and 3FH

Each bit has the meaning listed below. Input-wait operation is skipped if a bit is 0. Input-wait operation is allowed if a bit is 1.

- Meaning of each bit

Bit 0 : RAM check error
Bit 1 : CPU VIRTUAL test error (not occur in BIOS ROM Ver.1.02)
Bit 2 : RTC error (corresponds to an error other than '163-time and date not set')
Bit 3 : RTC time error (corresponds to '163-time and date not set')
Bit 4 : CRT DIP switch setting error or controller error
Bit 5 : Keyboard error
Bit 6 : FDD error
Bit 7 : HDD error

- CMOS 3FH

Bit 0 : X287 setting error (corresponds to '162-time system options not set')
Bit 1 : Key locked status
Others : Reserved (set to 1)

4.3.4 Response and Information of Errors

The table shows response and information related to errors detected by POD. An unfixed value is stored at I/O address 80H if continue is indicated for operation.

TABLE 4-3-1. RESPONSE AND INFORMATION FOR ERRORS

PORT 80	PROBABLE CAUSE	SOLUTION	EXPLANATION	ERROR MESSAGE OUTPUT TO CRT	NEXT OPERATION
01H	CPU	Remove then re-insert or replace CPU	* CPU CHECK The protection enable (PF) bit in the CPU machine status ward (MSW) was 1 instead of 0. (MSW should be 0)	None	HALT
04H	BIOS ROM	Remove then re-insert or replace BIOS ROM	* BIOS ROM CHECK An error occurred in BIOS ROM check sum	None	HALT
05H	GAATIO	Replace GAATIO	* DMA PAGE REGISTER CHECK An error occurred during DMA page register check operation.	None	HALT
06H	146818 (RTC)	Replace RTC	* RTC REGISTER CHECK (Changing from protect mode to real mode check) An error occurred during RTC C-MOS RAM area 0FH check operation. Checking is performed by setting and verifying each bit sequentially. * RTC C-MOS RAM 0F(H): Shut down status byte	None	HALT
07H or 08H	8254 (Timer counter)	Replace 8254	* TIMER COUNTER CHECK (Refresh function) An error occurred during timer counter 1. -For 07H (1 is written in each bit for of the count register and counting is started) An error occurred when checking that the all upper four bits of the down counter become zero.	None	HALT

			-For 08H (0 is written in each bit of the count register and counting is started) An error occurred when checking that the upper four bits of the down counter become 1.		
09H or 0AH	GAATIO	Replace GAATIO	* REFRESH DEFECT BIT (I/O PORT) CHECK -For 09H I/O port 61H bit4 could not be set to 0. -For 0AH I/O port 61H bit4 could not be set to 1. * I/O port 61H: Refresh detect bit (Half of the refresh signal frequency is indicated by this bit)	None	HALT
0BH or 0CH	8237A5 (DMAC)	Replace 8237A5	* DMA REGISTER CHECK -For 0BH An error occurred during checking the DMA controller 1 register. -For 0CH An error occurred during checking the DMA controller 2 register.	None	HALT
11H and error bit pattern	RAM	Replace RAM	* RAM (Base 64KB) CHECK An error occurred during checking the base 64K-byte RAM. LED indicates the following data repeatedly. (1) 11h(1 second) (2) Error bit pattern (1 second) (Upper byte)	000000 xxxx 201 Error bit pattern	HALT

(3) Error bit pattern (1 second)
(lower byte)

* DETEMING THE FAULTY RAM LOCATION.
The RAM corresponding to the bit of which LED is on is faulty.

(Example)
When Upper byte 00000000
Lower byte 00001000,
RAM corresponding to bit3 at location 15A is faulty (When ANT-RM circuit board unit number Y12620300000 is used.)
If no error is detected during RAM check but an error is detected during parity check, LED indicated error message as follows:

(1) 11H (1 second)

(2) 00H (1 second)

(3) 00H (1 second)

In this case, the error bit pattern is not indicated.
(Note)
An error message is also displayed on the CRT screen. The faulty RAM is detemined as follows:

000000 xxxx 201

Error bit pattern

			(Example) When the error bit pattern is ADCE: A B C D 1010 1101 1100 1110 RAMs corresponding to bits 1, 2, 3, 6, 7, 8, 10, 11, 13 and 15 are faulty.		
16H	8042 (8742)	Replace 8042 (8742)*	KEYBOARD CONTROLLER REGISTER CHECK The IBF bit in the 8042 (8742) status register was not cleared even after a fixed time elapsed. * If the IBF bit is on, the 8042 (8742) data bus buffer contains data. This IBF bit is automatically cleared by the 8042 (8742) internal probram.	None	HALT
17H	8042 (8742)	Replace8042 (8742)*	KEYBOARD CONTROLLER SELF-CHECK The normal termination code (55H) was not returned when the keyboard controller selftest program was executed. (Note) The keyboard controller selftest differs from the keyboard unit selftest.	None	HALT
18H	8042 (8742)	Replace 8042 (8742)	* DATA TRANSMISSION CHECK BETWEEN KEYBOARD CONOROLLER AND CPU The IBF bit in the 8042 (8742) status register was not cleared even though a fixed time elapsed after a command was sent to the 8042 (8742) data bus buffer. * The IBF bit in the 8042 (8742) status register is on when the	None	HALT

			data bus buffer contains command or data. The IBF bit is automatically cleared by the 8042 (8742) internal program.		
22H	GAATIO	Replace GAATIO	* DMA PAGE REGISTOR CHECK An error was detected while checking the access to DMA page register (83, 84H) Folling two check operations are performed: (1) 55AAH is written as data in above port.(83,84H) The data is read by and the written data with read data. (2) 55AAH is written in avobe (83,84H) port byte mode. Then written data is read, and the written data is compared with the read data. This error is indicated if the written data was not equal to the read data.	106-System board error	HALT
23H - 25H	8259	Replace 8259	* INTERRUP CONTROLLER AND INTERRUPT MASKING CHECK For 23H: An error was detected in the interrupt mask register of the master interrupt controller. Checking is done writing and verifying 00 and FF in the interrupt mask register. For 24H: An error was detected in the interrupt mask register of the slave interrupt controller. Checking is the same as the explained for 23H.	101-System board error	HALT

			For 25H: An interrupt occurred even though all bits in the interupt mask register were on. Checking is done in the following order: -FFH is set in the interrupt mask registers of the master and slave interrupt controllers. -Whether an interrupt is ckecked by software ST1 command.		
26H or 27H	8254-2 8259A-2	Replace 8254-2 or 8259A-2	* TIMER SPEED CHECK An error was detected in timer controller counter 0. For 26H: It is set so that interrupt occurs after 60usec from the start of counter. This error is indicated if an interrupt does not occur during the 90usec from the start of counter. For 27H: It is set so that an interrupt occurs after 200usec from the start of counter. This error is indicated if an interrupt occurs during the 150 usec from the start of counter.	102-System board error	HALT
28H	8254-2 8259A-2	Replace 8254-2 or 8259A-2	* TIMER COUNTER INTERRUPT CHECK This error is indicated if a counter 0 interrupt set by the operation explained for 27H does not occur at 200usec or after 200usec.	103-System board error	HALT

2AH	8254-2	Replace 8254	* TIMER COUNTER 2 CHECK 55AAH is written in timer controller counter 2, the counter is read, and the written data is compared with the read data. This error is indicated if the written data is not equal to the read data.	108-System board error	HALT
2BH	RAM, GAATIO option board	Replace the RAM, GAATIO, or option board	* NMI CIRCUIT CHECK This error is indicated if an NMI occurs during the next 400us after NMI is allowed. During the 400usec, CPU does not access to RAM. So, if this error is occured NMI circuit has problem. (Ref) NMI occurs under one of the following conditions: (1) A RAM parity check error occurs. (2) An I/O channel error occurs.	105-System board error	HALT
2CH	8042 (8742)	Replace 8042 (8742)	* KEYBOARD CONTOLLER STATUS REGISTER CHECK The IBF bit in the 8042 (8742) status register was not cleared even after a fixed time elapsed. * Checking is done in the same way as 16H.	105-System board error	HALT
2EH, 36H, OR 3BH	CPU	Remove them re-insert or replace CPU	* ADDRESS LINE (A19 TO A23) CHECK The protection enable (PE) bit in THE CPU MACHINE STATUS WARD (MSW) REGISTER WAS TURNED ON BUT THE BIT WAS OFF WHEN VERIFIED.	None	HALT

31H or 32H	GAATM1 GAATM2	REPLACE GAATM1 OR GAATM2	* ADDRESS LINE (A19 TO A23) CHECK An error occurred while checking address lines 19 to 23. *Checking address lines method. (1) FFFFH is written in address 000000 (2) 0000H is written in the following addresses: 080000 100000 200000 400000 800000 (3) When the data stored in address 000000 is FFFFH, address lines A19 to A23 are detemined as normal. If value of address 000000 is not FFFFH, address line (A19 to A20) has problem.	None	HALT
(38H) Unfixed value	RAM	Replace RAM	* RAM SIZE CHECK One of the following errors was detected during the checking of the RAM size: (1) Bad RAM (2) A parity error * An error address and error bit pattern are displayed on the CRT screen. (1) If a bad RAM is detected: An error address and an error bit pattern are displayed on the CRT screen as follows: xxxxxx **** 202-Memory address error xxxxxx Error address	202-Momory address error	CONTINUE

(Address)
If an address from 000000H to 07FFFFH is indicated, there is an error in the 256K-bit RAM on the ANT-RM circuit board.
If an address from 080000H to 09FFFFH is indicated, there is an error in the 64K-bit RAM on the ANT-RM circuit board.
If an address from 100000H to FDFFFFH is indicated, there is an error in the RAM on the option slot.
(Pattern)
This is same as the one explained for 11H.
Please see "Note" in the item 11H.
(2) For a parity error
Data is indicated on the CRT screen as follows:

```
xxxxxx  0000 202-Memory address error

           --- Parity check  1 or 2
         1: RAM parity error (Internal circuit)
         2: I/O channel parity error
            (Extension Memory card)
xxxxxx ---- Error address
 0000  ---- All zeros are displayed
```

(3AH) Unfixed value	* ADDRESS LINE (A16 TO A23) CHECK One of the folowing errors was detected during checking the address line: (1) Address line (A16 to A23) error (2) Parity error	203-Memory address error	CONTINUE

* Checking address lines

a) Check data is written in the RAM specified at the start address of block (64K bytes) as shown in the above figure.
b) The written data is verified after the data is written in all of the blocks.
c) This error is indicated if an error is detected during verfication explained in b.

* An error address and read data are displayed on the CRT screen.
* Error message explantion
  (1) Address line error
      xxxxxx **** 203-Memory address error
      xxxxxx ---- Error address
       **** ---- Read data (Not accordant data)
      xxxxxx **** 203-Memory address error
         -- Parity check 1 or 2
          1: RAM parity error (Internal circuit)
          2: I/O channel parity error (Extension Memory card)

(3EH) Unfixed value	Keyboard unit or 8042 (8742)	Replace the keyboard unit or 8042 (8742)	* KEYBOARD CLOCK CHECK The T0 bit (indicating the clock sent from the keyboard) of the test input port in 8042 (8742) was not turned low.	304-keyboard or System Unit error	CONTINUE
(3FH)	Keyboard unit, 8042(8742), or ANTA circuit board	Replace the Keyboard, 8042(8742), or ANTA circuit board	* KEYBOARD INTERFACE CIRCUIT CHECK Before this check, the POD execute keyboard unit self-test. Next, the POD execute keyboard interface circuit check. When keyboard interface circuit has no error, this error will indicate.	301-KEYBOARD error	CONTINUE

		So, when this error message is indicated. In this case, the code output repeatedly is displayed on the CRT screen. This error is also indicated if a code is output repeatedly from the keyboard.		
(3FH) 8042 Unfixed (8742) value	Replace 8042 (8742)	* KEYBOARD INTERFACE CIRCUIT CHECK This error is indicated if a response to the interface line test command output during keyboard interface circuit check (explained in the previous section) is not returned or the response indicates an error.	303-CRT error or System unit error	CONTINUE
(42H) DIP Unfixed switch value setting	Set the DIP switch correctly.	* CRT SLIDE SWITCH SETTING CHECK The slide for setting the monitor did not match with the mounted video card. If 401-CRT error is displayed on the CRT screen, the monochrome monitor was set by the switch but the video card indicated the color monitor. If 501-CRT error is displayed on the CRT screen, the color monitor was set by the switch but the video card indicated the monochrome monitor.	401-CRT error or 501-CRT error	CONTINUE

(42H) Unfixed value	Lithium battery	Replace the lithium battery and perform 'set-up'	* RTC POWER FAILURE CHECK RTC power failure was detected. This error is indicated if the VRT bit in RTC (146818) control register D is 0.	101-System options not set 161-System options not set	CONTINUE CONTINUE
(42H) Unfixed value	RTC (146818) setting error	Replace or correctly set RTC (146818) and perform 'set-up'	* RTC SETTING CHECK AND RTC CHECK-SUM CHECK An error occurred in RTC check sum or the RTC contents did not match with the mounted hardware.	162-System options not set	CONTINUE
(42H) Unfixed value	Setting error	Preform setting correctly	* RAM SIZE CHECK This error is indicated if the value in the mounted RAM differs from RTC setting.	164-Memory size error	CONTINUE
(42H) Unfixed value	RTC (146818)	Replace RTC (146818)	* TIME AND DATE CHECK This error is indicated if the RTC control register was read but processing did not enter update in progress status, or update in progress status could not be cleared.	163-Time & Data not set	CONTINUE
(43H) Unfixed value	FDD, SPFG circuit board, or WHDC circuit board	1) Replace FDD 2) Mount one or both of the SPFG and WHDC circuit boards if it was not mounted. 3) Replace the SPFG or WHDC circuit board and perform 'set-up'	* FDD CHECK (1) An error was returned when FDC was reset (INT 13H reset function). (2) FDD was normally reset (as a result of the above checking) but an error was returned during head seek test (only drive A was checked). (3) A card equivalent to IBM COMBO card did not install(the error occurs if SPFG or WHDC circuit board is missing).	601-Diskette error	CONTINUE

		This error is indicated under one of the above conditions.		
(45H) WHDC Unfixed circuit value board	Replace the WHDC circuit board	* HDC SELF TEST CHECK An abnormal code was returned during hard disk controller selftest.	1782-disk controller failure	CONRINUE
(45H) HDD or Unfixed WHDC value circuit board	Replace the HDD or WHDC circuit board	* HDD CHECK The hard disk could not be recalibated. * If 1780-disk 0 failure is displayed on the CRT screen, the CMOS data in RTC is rewritten and IPL from HDD is disabled.45H	1780-Disk 0 failure 1781-Disk 1 failure	CONTINUE
(45H) Setting Unfixed error value	Perform setting correctly	* MAX CYLINDER, MAX HEAD, MAX SECTOR READ CHECK This error is indicated if the POD can not read the Max. sector of the Max.track which is determined by CMOS.	1790-Disk 0 error 1791-Disk 1 error	CONTINUE
(48H) ROM CHIP Unfixed on I/O value slot	Replace ROM chip	* I/O ROM CHECK When the POD detect a I/O ROM ID, the POD execute check-sum for the I/O ROM. This error message will be indicated on the screen of the CRT. <REMARK> In case of address if the I/O ROM ID is assighed to 7FFFH < I/O ROM ID < C800H, this error message will not be indicated on the screen of the CRT, but following error message will sound from spealer. BEEP First ; long beep Second ; short beep	xxxx0 ROM error	CONTINUE

(49H) RTC Unfixed value	(146818)	Replace RTC (146818)	* TIME AND DATE CHECK A range over error occurred when hour, minutes, and seconds are read even though RTC was normal: 1) Power failure was not detected 2) No error in RTC check sum. 3) RTC could enter update in progress status. 4) RTC could be cleared from update in progress status This error is indicated if a range over error occurs in hours, minutes, or seconds as follows: Hours > 23 Minutes > 59 seconds > 59		
(4CH) Unfixed value	The lock was in locked status	Unlock the key	* LOCK STATUS CHECK The lock was in locked status.	302-System unit keylock is locked	CONTINUE
None			* PARITY ERROR CHECK When a parity error was detedted, Entire memory is parity-checked again. The address of memory where the parity error was detected is indicated with a 5-digit hexadecimal number. At this time, a parity error cannot be found, ????? is indicated. All error message will be indicated on screen of CRT. (Example) If a parity error occurs in addresses 512 to 576KB, the following data is displayed on the CRT screen:	Parity check 1 or Parity check 2	HALT

```
Parity check 1
   80000   (S)
     (S) Segment
     A parity error occurred in the
     segment placed at address 80000
     or later.
```

CHAPTER

5

DISASSEMBLY AND ASSEMBLY

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5.1 MAIN UNIT DISASSEMBLY AND ASSEMBLY

5.1.1 Upper Case Removal

1. Unlock the key (B) to remove the upper case (A).
2. Remove the four screws (C) from the rear.
3. Slide the upper case forward.
4. Remove the upper case by opening the side section (1) in the direction indicated by the arrows.

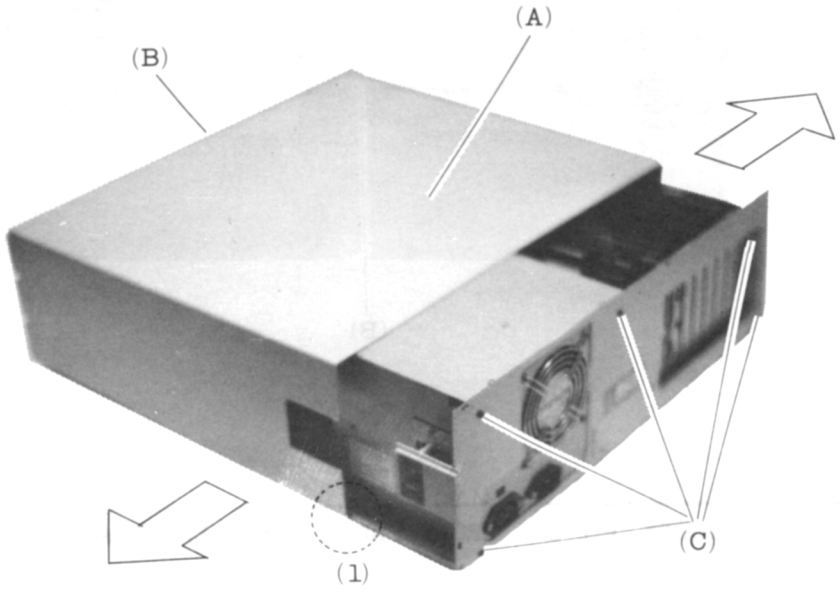

FIGURE 5-1-1. UPPER CASE REMOVAL/REPLACEMENT

5.1.2 Upper Case Replacement

1. Fit the upper case over the lower case.
2. Slide the upper case to the rear.
3. Replace the four screws (C) at the back.
5. Lock the upper case if required.

5.1.3 Front Panel Removal

1. Remove the upper case.
2. Remove the four screws (A) to remove the front panel.

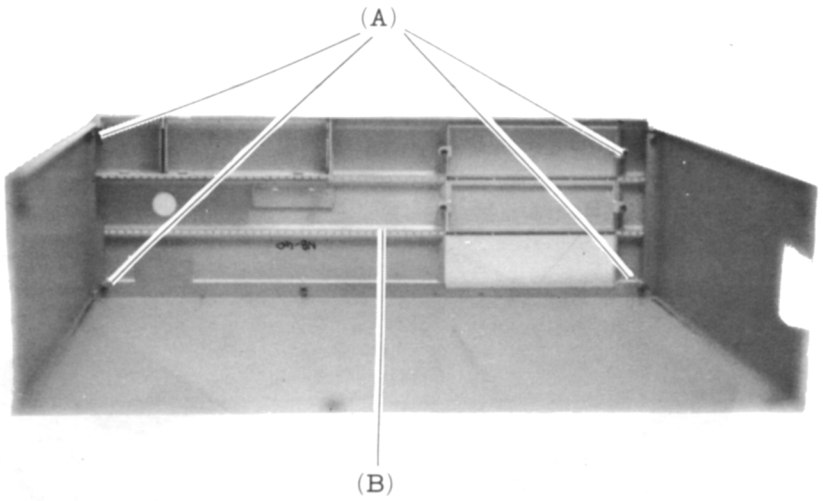

FIGURE 5-1-2. FRONT PANEL REMOVAL/REPLACEMENT

5.1.4 Front Panel Replacement

1. Replace the front panel by attaching the four screws (A).
2. Replace the upper case.

5.1.5 Power Supply Unit (ATRPS UNIT) Removal

1. Remove the upper case.
2. Remove the two ANT-MT Board connectors (B), and the FDD and HDD power supply connectors.
4. Remove the four screws (C) from the rear.
5. Slide the power supply unit (D) about 6 cm towards the front to clear the hold-down tabs and remove the unit.

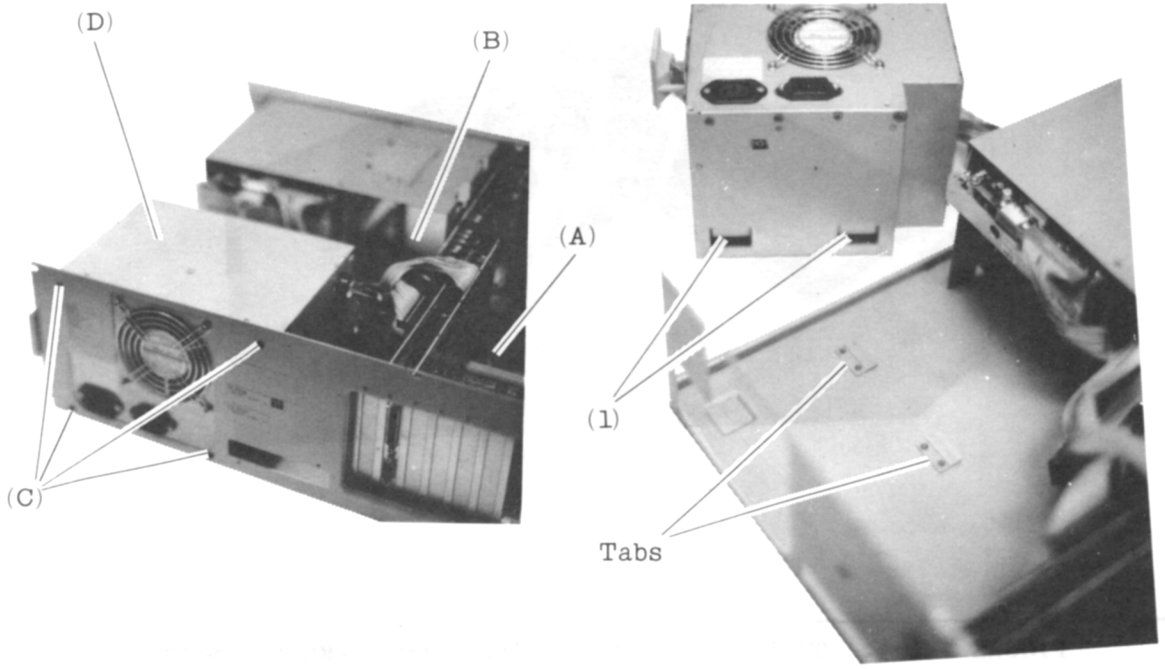

FIGURE 5-1-3. POWER SUPPLY UNIT REMOVAL/REPLACEMENT

5.1.6 Power Supply Unit (ATRPS UNIT) Replacement

1. Replace the power supply unit by sliding it toward the rear over the hold-down tabs on the lower case.
2. Fasten the power supply unit with the four screws (C).
3. Replace the two ANT-MT Board connectors (B), and the FDD and HDD power supply connectors.
4. Replace the upper case.

5.1.7 Optional Circuit Board Removal

1. Remove the upper case.
2. Disconnect the cables attached to the optional circuit board, if required.
3. Remove screw (A) which holds the board to the lower case.
4. Remove the board by firmly grasping the edge at both ends and pulling directly upwards.

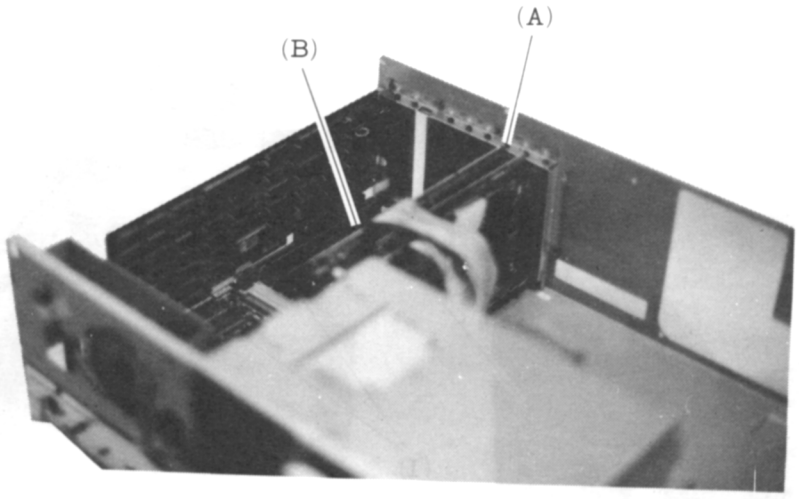

FIGURE 5-1-4. OPTIONAL CIRCUIT BOARD REMOVAL/REPLACEMENT

5.1.8 Optional Circuit Board Replacement

1. Insert the optional circuit board into the ANT-MT Board connector slot (B).
2. Fasten the board with screw (A).
3. Replace the cable connections.
4. Replace the upper case.

5.1.9 Disk Drive (HDD or FDD) Removal

1. Remove the upper case.
2. Disconnect the signal and power supply cables on the rear of the unit.
3. Remove the two side screws (A) fastening the drive.
4. Remove the drive unit by sliding it carefully out the front of the lower case.

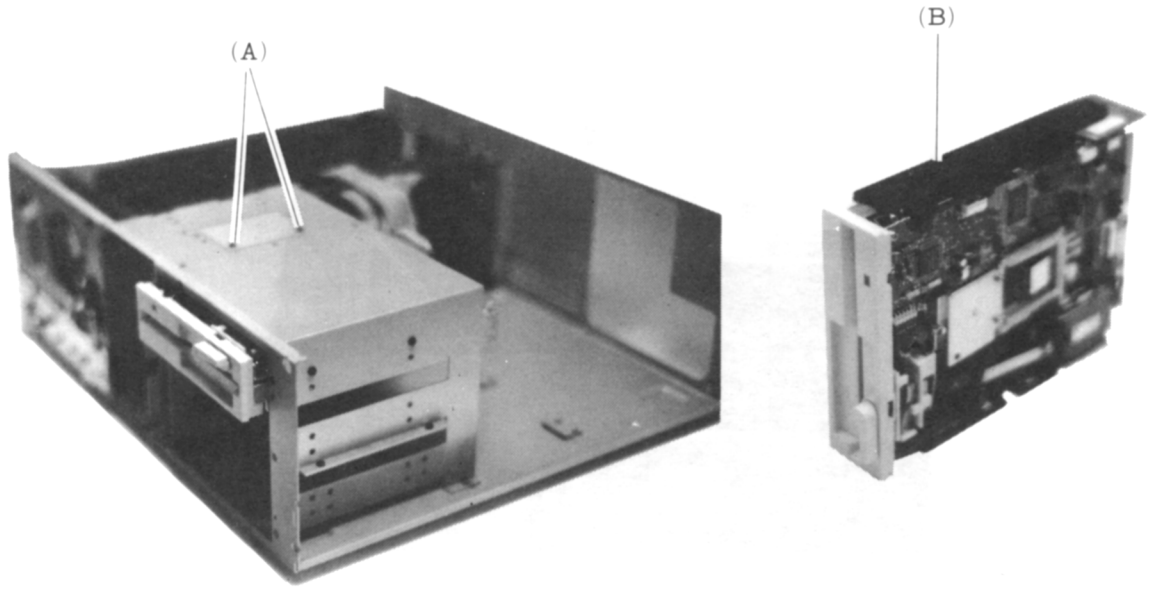

FIGURE 5-1-5. DISK DRIVE REMOVAL/REPLACEMENT

5.1.10 DISK DRIVE (HDD or FDD) Replacement

1. Place the slider (B) at the left (to mount the drive horizontally) or at the bottom (to mount the drive vertically) and attach the drive to the lower case.
2. Fasten the drive with the two screws (A).
3. Connect the signal and power supply cables to the drive.
4. Replace the upper case.

(Note 1) Arrange the signal and power supply cables, then fasten the cables with the clamp attached to the power supply unit.

5.1.11 ANT-RM Circuit Board Removal

1. Remove the upper case.
2. Remove the screw (B) fastening the ANT-RM board (A) to the lower case.
3. Remove the ANT-RM board by grasping the edge at both sides and pulling directly upwards.

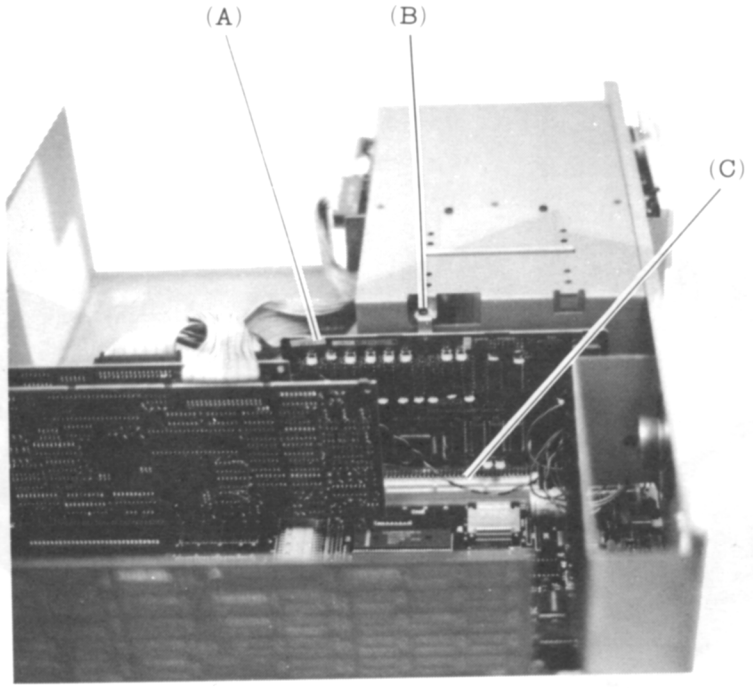

FIGURE 5-1-6. ANT-RM CIRCUIT BOARD REMOVAL/REPLACEMENT

5.1.12 ANT-RM Circuit Board Replacement

1. Insert the ANT-RM board in the ANTA board connector slot (C).
2. Fasten the ANT-RM board to the lower case with the screw (B).
3. Replace the upper case.

5.1.13 Main (ANTA) Circuit Board Removal

1. Remove the upper case.
2. Remove the ANT-RM circuit board.
3. Remove the four screws (D) fastening the ANTA board (C) to the lower case.
4. Disconnect the ANTA board connector (F).
5. Open the tabs (E) of the ANTA board towards the sides and slide the ANTA board out 7 or 8 cm towards the front.
6. Disconnectg the ANTA board connector (G).
7. Pull the ANTA board out all the way to remove it.

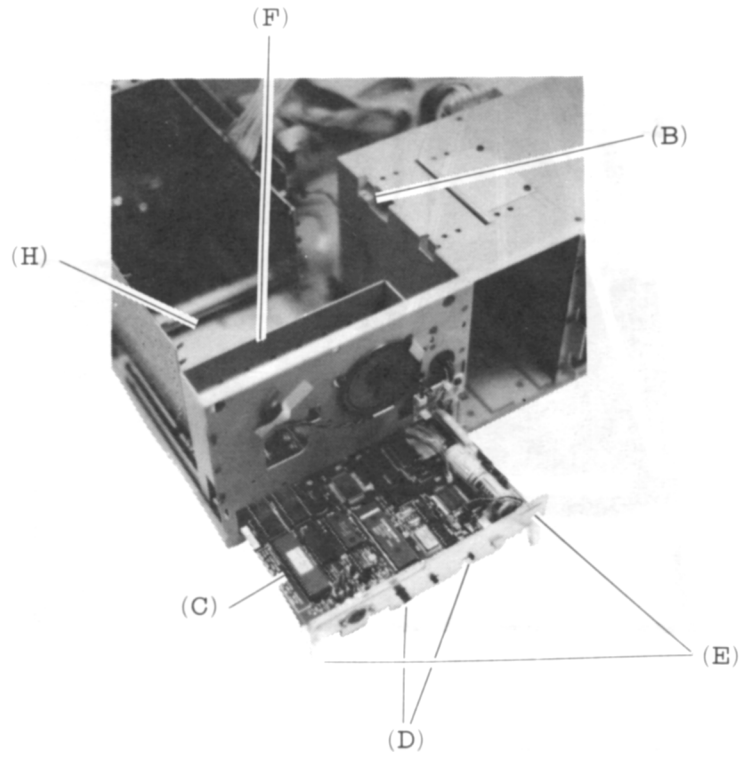

FIGURE 5-1-7. ANTA CIRCUIT BOARD REMOVAL/REPLACEMENT

5.1.14 Main (ANTA) Circuit Board Replacement

1. Hold the ANTA circuit board (C) level and slide it horizontally toward the rear until about 8 cm of clearance remains.
2. Replace the connector (G) on the ANTA board.
3. Slide the ANTA board horizontally to firmly seat it into the ANT-MT board connector (H).
   Note: Make sure that no cables are held between the ANTA and ANT-MT boards.
4. Replace the ANTA board connector (F).
5. Replace the ANT-RM board.
7. Replace the upper case.

5.1.15 ANT-MT Circuit Board Removal

1. Remove the upper case.
2. Remove all optional circuit boards.
3. Remove the ANT-RM board.
4. Remove the ANTA board.
5. Disconnect the two connectors (A).
6. Remove the five screws (C) fastening the ANT-MT board (B) to the lower case and remove the ANT-MT board.

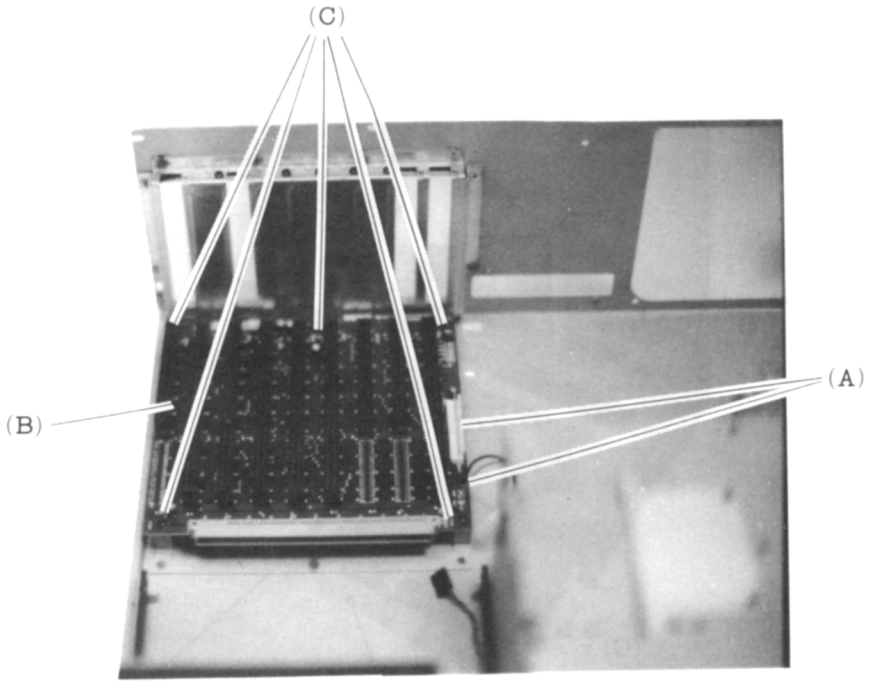

FIGURE 5-1-8. ANT-MT CIRCUIT BOARD REMOVAL/REPLACEMENT

5.1.16 ANT-MT Circuit Board Replacement

1. Replace the ANT-MT board and fasten with the five screws (C).
2. Connect the two connectors (A).
3. Replace the ANTA board.
4. Replace the ANT-RM board.
5. Replace the optional circuit boards.
6. Replace the upper case.

5.1.17 ANT-LS (LED) Circuit Board Removal

1. Remove the upper case.
2. Disconnect connector CN6 on the WHDC circuit board.
3. Remove the ANT-RM board and disconnect the connector (A) from the ANTA circuit board.
4. Disconnect the connector (B) from the speaker cable.
5. Disconnect the connector (D) from the case lock switch cable (C).
6. Remove the screws (F) fastening the ANT-LS circuit board (E).
7. Remove the ANT-LS board.

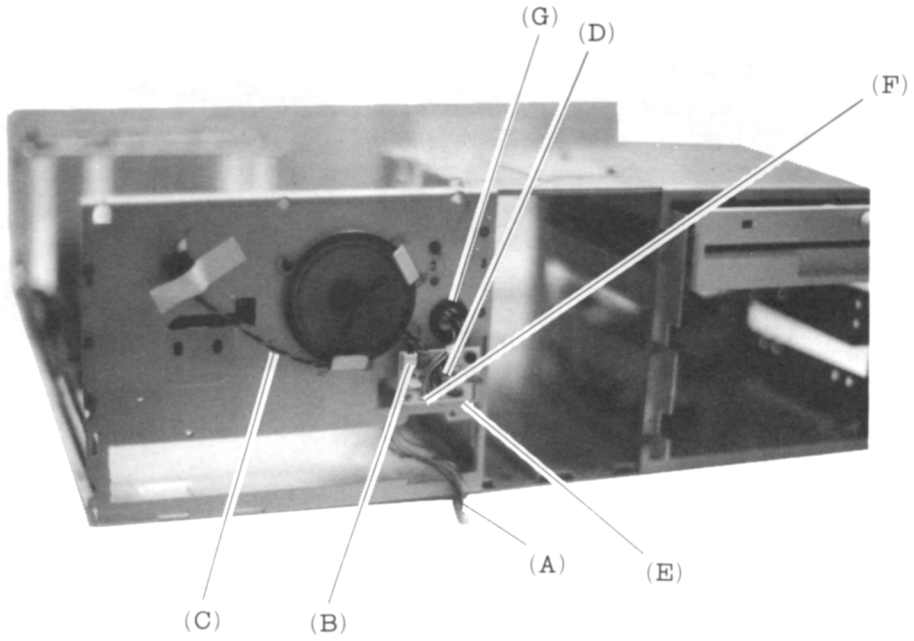

FIGURE 5-1-9. ANT-LS CIRCUIT BOARD REMOVAL/REPLACEMENT

5.1.18 ANT-LS Circuit Board Replacement

1. Replace the ANT-LS board (E) and fasten with the screws (F).
2. Pass the cable for the connector (A) through the hole (G) toward the main circuit board.
3. Connect the connector (A).
4. Connect the connectors (B) and (D).
5. Replace the ANTA and ANT-RM boards.
6. Connect connector CN6 of the WHDC circuit board.
7. Replace the upper case.

5.1.19 Speaker Removal

1. Remove the upper case.
2. Remove the speaker connector (A) from the ANT-LS board.
3. Remove the screw (C) fastening the speaker to the mounting board.
4. Remove the speaker.

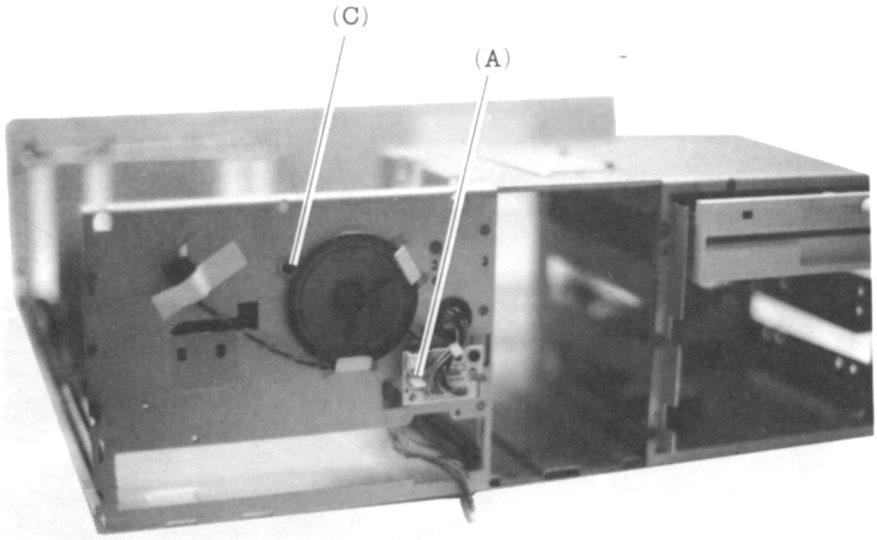

FIGURE 5-1-10. SPEAKER REMOVAL/REPLACEMENT

5.1.20 Speaker Replacement

1. Replace the speaker on the mounting board with the screw (C).
2. Connect the speaker cable to the connector (A) on the ANT-LS board.
3. Replace the upper case.

5.2 KEYBOARD UNIT DISASSEMBLY AND ASSEMBLY

5.2.1 Key Cylinder Unit Removal

1. Remove the upper case.
2. Disconnect the connector (B) from the case lock switch cable (A).
3. Remove the screws fastening the key cylinder unit mounting plate.
4. Remove the key cylinder unit mounting plate.

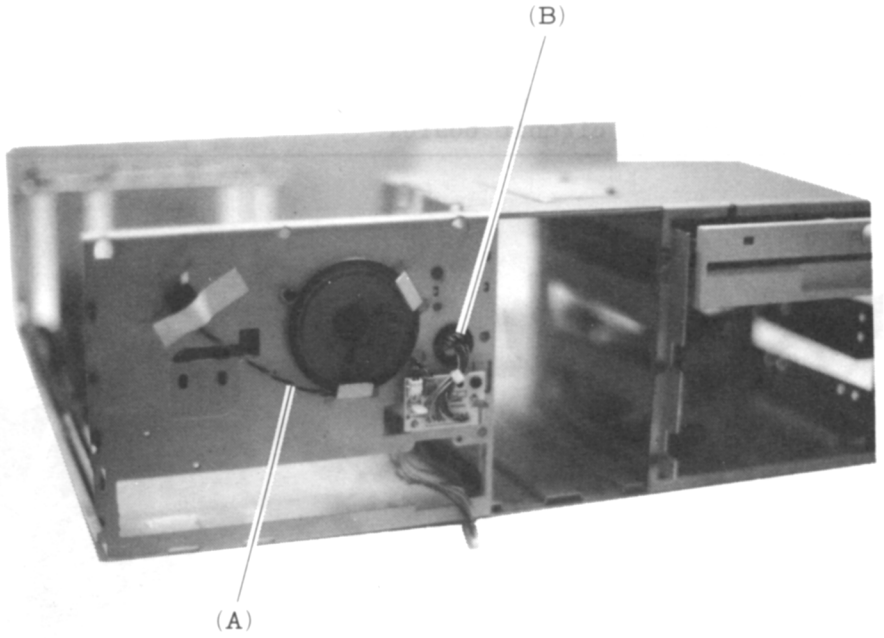

FIGURE 5-2-1. KEY CYLINDER UNIT REMOVAL/REPLACEMENT

5.2.2 Key Cylinder Unit Replacement

1. Fasten the key cylinder mounting plate with the screws.
4. Connect the connector (B) to the ANT-LS board.
5. Replace the upper case.

5.3 POWER SUPPLY UNIT (ATRPS) DISASSEMBLY AND ASSEMBLY

5.3.1. Secondary-side Circuit Board Removal

1. Remove the five screws (A) to remove the cover (B).
2. Remove the four screws (C).
3. Pull up the secondary-side circuit board (D) 5 cm and disconnect the fan connector (E).
4. Remove the cable clamp (F) in the following order:
   (1) Hold the cable clamp (F) and rotate the clamp so that the cut section of clamp is mated with the cut section of the power supply case.
   (2) Remove the cut section of the cable clamp.
   (3) Remove the cable clamp.
5. Remove the cables (G) along the cut section of the power supply case to remove the secondary-side circuit board.

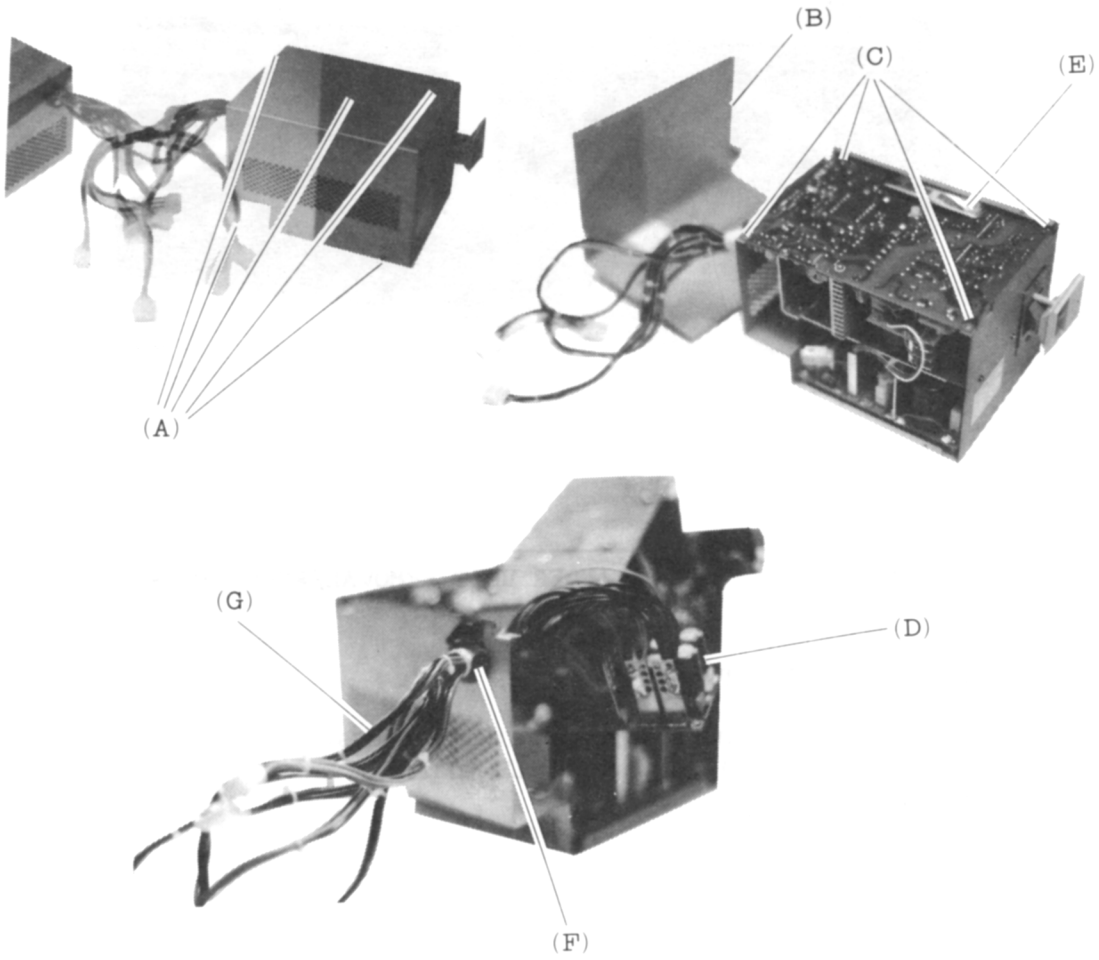

FIGURE 5-3-1. SECONDARY SIDE CIRCUIT BOARD REMOVAL/REPLACEMENT

5.3.2 Secondary-side Circuit Board Replacement

1. Replace the cable clamp (F) on the cable (G).
   Hold the cut section of the cable clamp so that it will not come off.
2. Insert the thinner section of the cable clamp in the hole on the power supply case.
3. Connect the connector (E) to the secondary-side circuit board (D).
4. Fasten the secondary-side circuit board with the four screws (C).
5. Fasten the cover (B) with five screws (A).

5.3.3 Fan Unit Removal

1. Remove the secondary-side circuit board.
2. Remove the four screws (A) to remove the fan unit.

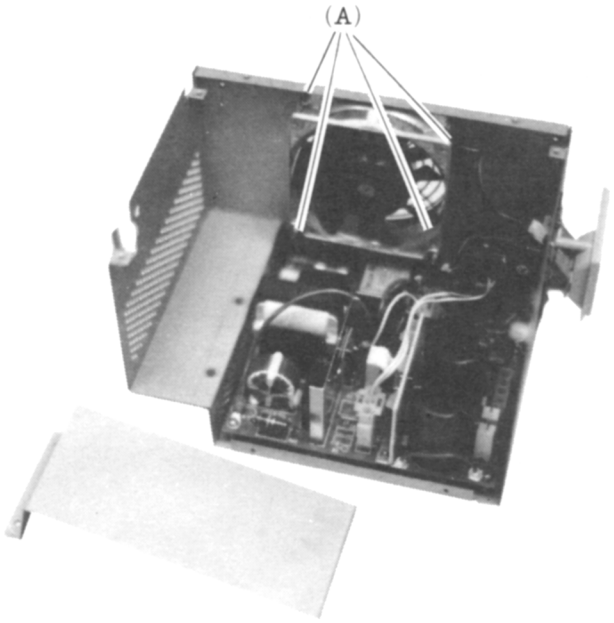

FIGURE 5-3-2. FAN UNIT REMOVAL/REPLACEMENT

5.3.4 Fan Unit Replacement

1. Fasten the fan unit (B) with the four screws (A).
2. Replace the secondary-side circuit board.

5.3.5 Primary-side Circuit Board Removal

1. Remove the secondary-side circuit board.
2. Remove the fan unit.
3. Remove the two connectors (D).
4. Remove the five screws (C) fastening the primary-side circuit board and remove the screws (E) fastening the two cables connecting the AC outlet.
5. Slide the primary-side board horizontally to remove the board.

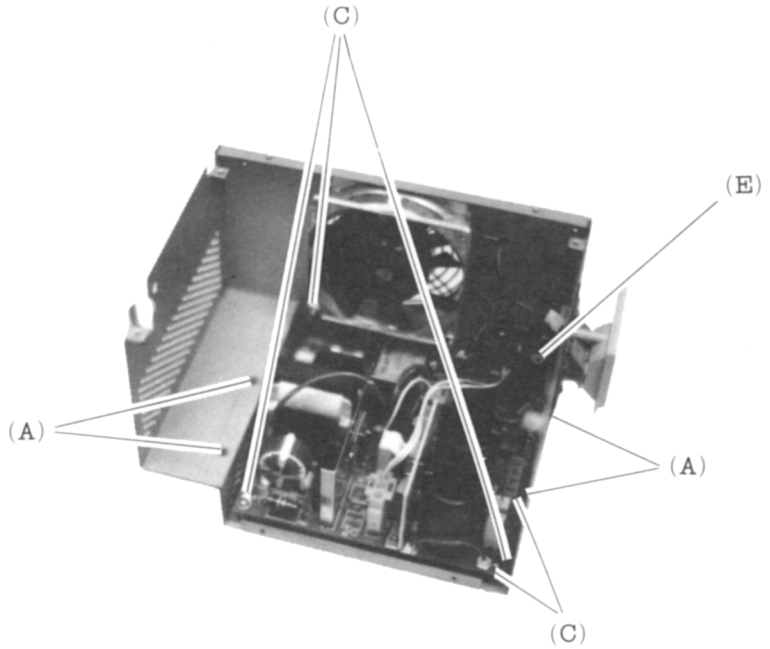

FIGURE 5-3-3. PRIMARY-SIDE CIRCUIT BOARD REMOVAL/REPLACEMENT

5.3.6 Primary-side Circuit Board Replacement

1. Replace the primary-side circuit board by sliding in horizontally.
2. Fasten the primary-side board with the five screws (C).
3. Fasten the two cables connecting the AC outlet to the primary-side board with the screws (E).
4. Connect the two connectors (D).
5. Replace the fan unit.
6. Replace the secondary-side circuit board.

CHAPTER

6

ADJUSTMENT AND MAINTENANCE

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7

DIAGRAMS AND REFERENCE MATERIALS

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7.1 SLIDE SWITCH & JUMPER CONNECTOR SETTINGS

7.1.1 Slide Switch Settings

Monitor Select Switch
MONO : Monochrome Monitor (Factory setting)
COLOR: Color Monitor

CPU Speed Select Switch
6 : 6 MHz
8 : 8 MHz (Factory setting)
10 : 10 MHz

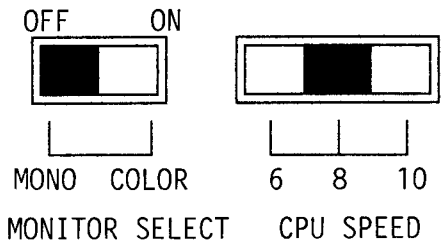


FIGURE 7-1-1. SLIDE SWITCH SETTINGS

Volume Adjustment
Turn clockwise to increase the volume.
Turn counter-clockwise to decrease the volume.

FIGURE 7-1-2. VOLUME ADJUSTMENT

7.1.2 JUMPER CONNECTOR SETTINGS

Jumper Connectors

Jumper connectors provide a means to make a semi-permanent selection of a particular operational function, for instance, the 'A' or 'B' function in Fig. 7-1-3 (1), where 'C' is the common terminal. If a jumper connection is called 'A-C', the jumper is connected as in configuration '2' in Fig. 7-1-3. If a jumper connection is called 'B-C', the jumper is connected as in configuration '3' in Fig. 7-1-3.

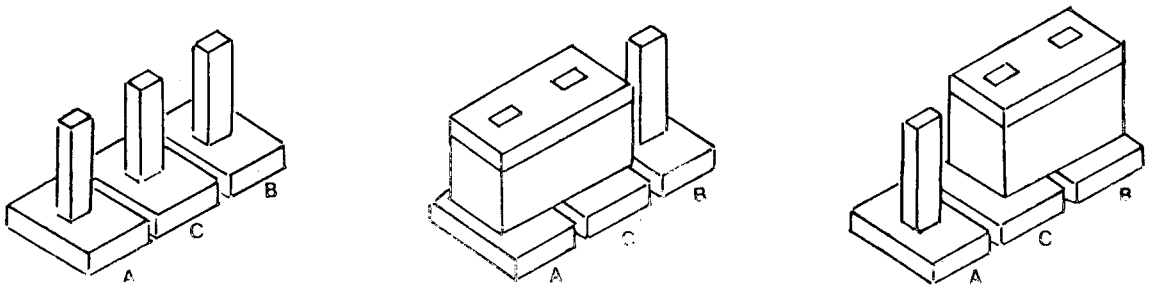


FIGURE 7-1-3. JUMPER CONNECTORS

Main (ANTA) Board Jumper Connections

TABLE 7-1-1. MAIN (ANTA) BOARD JUMPER CONNECTIONS

Jumper Number						Function
J6	J5	J4	J3	J2	J1	
*	*	*	*	*	A-C	Set CPU clock mode 6/8/10
*	*	*	*	*	B-C	Inhibit
*	*	*	A-C	A-C	*	Inhibit
*	*	*	A-C	B-C	*	Input CPU clock as NPX clock (1/3)
*	*	*	B-C	A-C	*	Input 8 MHz as NPX clock
*	*	*	B-C	B-C	*	Inhibit
*	*	A-C	*	*	*	2 wait cycles for EPROM access **
*	*	B-C	*	*	*	1 wait cycle for EPROM access **
A-C	A-C	*	*	*	*	4 wait cycles for ext. 16-bit device access **
A-C	B-C	*	*	*	*	3 wait cycles for ext. 16-bit device access **
B-C	A-C	*	*	*	*	2 wait cycles for ext. 16-bit device access **
B-C	B-C	*	*	*	*	1 wait cycle for ext. 16-bit device access **

Legend: * = Not Applicable
** = Wait cycles available at 10 MHz operation

Factory Settings (Main ANTA Board)

TABLE 7-1-2. FACTORY SETTINGS (MAIN ANTA BOARD)

Jumper Number	Factory Setting	Function
J1	A-C	-
J2	A-C	> Input CPU clock as
J3	B-C	> NPX clock
J4	A-C	2 wait cycles for EPROM access
J5	A-C	> 4 wait cycles for external
J6	A-C	> 16-bit device access

System Memory (ANT-RM)

TABLE 7-1-3. SYSTEM MEMORY (ANT-RM) BOARD JUMPER CONNECTIONS

Jumper Number							
J7	J6	J5	J4	J3	J2	J1	Function
*	*	*	*	A-C	A-C	A-C	640KB Memory
*	*	*	*	A-C	A-C	B-C	512KB Memory
*	*	*	*	A-C	B-C	A-C	-
*	*	*	*	A-C	B-C	B-C	256KB Memory
*	*	*	*	B-C	A-C	A-C	-
*	*	*	*	B-C	A-C	B-C	-
*	*	*	*	B-C	B-C	A-C	-
*	*	*	*	B-C	B-C	B-C	000KB (disable all RAM)
*	*	A-C	A-C	*	*	*	27128
*	*	A-C	B-C	*	*	*	-
*	*	B-C	A-C	*	*	*	-
*	*	B-C	B-C	*	*	*	27256 EPROM size
A-C	A-C	*	*	*	*	*	Select ROM pair 24A and 24B
A-C	B-C	*	*	*	*	*	-
B-C	A-C	*	*	*	*	*	-
B-C	B-C	*	*	*	*	*	Select ROM pair 23A and 23B

Legend: + = Not Applicable
- = Inhibited

Factory Settings (ANT-RM Board)

TABLE 7-1-4. FACTORY SETTINGS (ANT-RM BOARD)

Jumper Number	Factory Setting	Function
J1	A-C	> 640KB
J2	A-C	> Memory
J3	A-C	> Size
J4	B-C	> 27256 EPROM
J5	B-C	> Memory Size
J6	A-C	> Select ROM socket
J7	A-C	> pair 24A and 24B

Hard Disk Controller (WHDC)

TABLE 7-1-5. HDD CONTROLLER (WHDC) BOARD JUMPER CONNECTIONS

Jumper Number			
J3	J2	J1	Function
*	*	B-C	Select primary address sets
*	*	A-C	Select secondary address sets
*	B-C	*	Non-latched status (LED)
*	A-C	*	Latched status (LED)
B-C	*	*	WAH mode
A-C	*	*	WA2 mode

Factory Settings (WHDC Board)

TABLE 7-1-6. FACTORY SETTINGS (WHDC BOARD)

Jumper Number	Factory Setting	Function
J1	A-C	Secondary address sets
J2	B-C	Non-latched status
J3	B-C	WAH mode

Multi-function Adapter (SPFG)

TABLE 7-1-7. MULTI-FUNCTION ADAPTER (SPFG) BOARD JUMPER CONNECTIONS

Jumper Number										
J8	J7	J6	J5	J4	J3	J2	J1	J10	J9	Function
*	*	*	*	*	*	A-C	A-C	*	*	Primary register set (3F0-3F7) AT:FDC
*	*	*	*	*	*	A-C	B-C	*	*	Secondary regis. set (370-377) AT:FDC
*	*	*	*	*	*	B-C	A-C	*	*	PC register set (3F0-3F7) : FDC
*	*	*	*	*	*	B-C	B-C	*	*	Disable FDC register set
*	*	*	*	A-C	A-C	*	*	A-C	*	Primary parallel I/F (378-37F):IRQ 7
*	*	*	*	B-C	A-C	*	*	B-C	*	Secondary paral. I/F (278-27F):IRQ 5
*	*	*	*	A-C	B-C	*	*	A-C	*	Parallel I/F on video adapter (3BC-3BF) : IRQ 7
*	*	*	*	B-C	B-C	*	*	*	*	Disable parallel I/F
*	*	A-C	A-C	*	*	*	*	*	A-C	Primary serial I/F (3F8-3FF) : IRQ 4
*	*	B-C	A-C	*	*	*	*	*	B-C	Secondary serial I/F (2F8-2FF):IRQ 3
*	*	A-C	B-C	*	*	*	*	*	*	Disable serial I/F
*	*	B-C	B-C	*	*	*	*	*	*	Disable serial I/F
*	A-C	*	*	*	*	*	*	*	*	AT drive I/F
*	B-C	*	*	*	*	*	*	*	*	EQUITY-3 drive I/F
A-C	*	*	*	*	*	*	*	*	*	Standard configuration
B-C	*	*	*	*	*	*	*	*	*	Test mode of VCO

Factory Settings (SPFG Board)

TABLE 7-1-8. FACTORY SETTINGS (SPFG BOARD)

Jumper Number	Factory Setting	Function
J1	A-C	> Primary register
J2	A-C	> set of AT
J3	A-C	> Primary
J4	A-C	> parallel
J10	A-C	> I/F : IRQ 7
J5	A-C	> Primary
J6	A-C	> serial
J9	A-C	> I/F : IRQ 4
J7	A-C	AT drive I/F
J8	A-C	Standard configuration

7.2 GATE ARRAY DESCRIPTION

7.2.1 GAATAB

GAATAB controls the CPU address bus, system address bus and the internal address bus. It has an 8-bit refresh counter.

TABLE 7-2-1. GAATAB PIN ARRANGEMENT

SIGNAL NAME	I/O*	PIN NO.	PIN NO.	I/O*	SIGNAL NAME
TESTN	I	1	64		Vcc
ALE	I	2	63	I	A16
A1	I	3	62	I	A15
A2	I	4	61	I	A14
A3	I	5	60	I	A13
XA0	Tri	6	59	Tri	XA16
XA1	Tri	7	58	Tri	XA15
LSA0	I	8	57	I	DXA
XA2	Tri	9	56	Tri	XA14
XA3	Tri	10	55	Tri	XA13
SA0	Tri	11	54	Tri	XA12
SA1	Tri	12	53	Tri	SA16
SA2	Tri	13	52	Tri	SA15
SA3	Tri	14	51	Tri	SA14
SA4	Tri	15	50	Tri	SA13
GNDA		16	49		GNDB
GNDB		17	48		GNDA
SA5	Tri	18	47	Tri	SA12
SA6	Tri	19	46	Tri	SA11
SA7	Tri	20	45	Tri	SA10
SA8	Tri	21	44	Tri	SA9
XA4	Tri	22	43	Tri	XA11
XA5	Tri	23	42	Tri	XA10
XA6	Tri	24	41	Tri	XA9
OE-N	I	25	40	I	R590N
XA7	Tri	26	39	Tri	XA8
A4	I	27	38	I	A12
A5	I	28	37	I	A11
A6	I	29	36	I	A10
A7	I	30	35	I	A9
A8	I	31	34	I	G590N
Vcc		32	33	I	C590

* Legend: I = Input Pin
O = Output Pin
Tri = Tri-state Pin (Input, Output, High-impedance)

TABLE 7-2-2. GAATAB PIN DESCRIPTION

SYMBOL	I/O*	PIN NO.	NAME AND FUNCTION
A16-1	I	63-60,38-35, 31-27,5-3	CPU address bus.
LSA0	I	8	Converted address 0. It is identical to CPU address 0 (A0), except when word to byte conversion is being performed.
SA16-0	Tri	53-50,47-44 21-18, 15-11	System address bus.
XA16-0	Tri	59,58,56-54, 43-41,39,26, 24-22,10,9, 7,6	Internal address bus.
ALE	I	2	Address latch enable. A16-1 are latched by ALE.
OEN	I	25	Enable control of latched address (A16-1). When low, LSA0 and latched A16-1 are enabled.
DXA	I	57	Direction control of internal address bus(XA16-0) buffer. When high XA16-0 are driven by SA16-0, and when low SA16-0 are driven by XA16-0.
C590	I	33	Clock of refresh counter. Refresh counter increments at C590 rising edge.
G590N	I	34	Output enable of refresh counter. When low, refresh address is placed on SA7-0.
R590N	I	40	Reset on refresh counter. When low, refresh counter is cleared.
TESTN	I	1	Test input. Should be pulled up.

* Legend: I = Input Pin
O = Output Pin
Tri = Tri-state Pin (Input, Output, High Impedance)

7.2.2 GAATCB

GAATCB controls the CPU control bus and the most significant 7 bits of the address bus. Contains one inverter, one NOR gate and one NAND gate.

TABLE 7-2-3. GAATCB PIN ARRANGEMENT

SIGNAL NAME	I/O*	PIN NO.	PIN NO.	I/O*	SIGNAL NAME
GSA-N	I	1	64		Vcc
DLA	I	2	63	I	Vi
ALE	I	3	62	O	VO
OE-N	I	4	61	I	NRI2
RFMRN	I	5	60	I	NDI1
RFC-N	I	6	59	O	NRO
BHE	I	7	58	I	NDI2
MIO	I	8	57	I	NDI1
SBHE	Tri	9	56	O	NDO
SMIO	O&H-Z	10	55	I	DXRW
XBHE	Tri	11	54	I	GSRWN
(NC)		12	53	Tri	IOW-N
LA17	Tri	13	52	Tri	IOR-N
LA18	Tri	14	51	Tri	MEMRN
LA19	Tri	15	50	Tri	MEMWN
GNDA		16	49		GNDB
GNDB		17	48		GNDA
LA20	Tri	18	47	O&H-Z	SA17
LA21	Tri	19	46	O&H-Z	SA18
LA22	Tri	20	45	O&H-Z	SA19
LA23	Tri	21	44	O&H-Z	SMR-N
A17	Tri	22	43	O&H-Z	SMW-N
A18	Tri	23	42		(NC)
A19	Tri	24	41		(NC)
(NC)		25	40		(NC)
A20	Tri	26	39		(NC)
A21	Tri	27	38	Tri	XIOWN
(NC)		28	37		(NC)
A22	Tri	29	36	Tri	XIORN
A23	Tri	30	35	Tri	XMW-N
(NC)		31	34	Tri	XMR-N
Vcc		32	33		(NC)

* Legend:
I = Input Pin
O = Output Pin
Tri = Tri-state Pin (Input, Output, High-impedance)
O&H-Z = Output & High-impedance Pin

TABLE 7-2-4. GAATCB PIN DESCRIPTION

SYMBOL	I/O*	PIN NO.	NAME AND FUNCTION
A23-17	Tri	30,29,27,26, 24-22	CPU address bus.
SA19-17	O&H-Z	45-47	System address bus. (8-bit connector).
LA23-17	I	21-18,15-13	Unlatched system address bus. (16-bit connector).
BHE	I	7	CPU bus high enable signal.
SBHE	Tri	9	System bus high enable signal. (16-bit connector).
XBHE	Tri	11	Internal bus high enable signal.
MIO	I	8	CPU memory / I/O signal.
SMIO	O&H-Z	10	Buffered memory / I/O signal.
IOWN	Tri	53	System I/O write signal. (8-bit connector).
IORN	Tri	52	System I/O read signal. (8-bit connector).
MEMWN	Tri	50	System memory write signal (16-bit connector).
MEMRN	Tri	51	System memory read signal (16-bit connector).
XIOWN	Tri	38	Internal I/O write signal.
XIORN	Tri	36	Internal I/O read signal.
XMWN	Tri	35	Internal memory write signal.
XMRN	Tri	34	Internal memory read signal.
SMWN	O&H-Z	43	System memory write signal (8-bit connector).
SMRN	O&H-Z	44	System memory read signal (8-bit connector).
DLA	I	2	Direction control of CPU address bus (A23-17) buffer. When high, LA23-17 are driven by A23-17. And when low A23-17 are driven by LA23-17.
GSAN	I	1	Enable control of address bus (SA19-17) buffer. When low, SA19-17 are driven by A19-17.
ALE	I	3	Address latch enable. A19-17 and MIO and BHE are latched by ALE.
OEN	I	4	Enable control of latched address (A19-17), MIO and BHE. When low, SA19-17 are driven by latched A19-17. When low, SMIO and SBHE are driven by latched MIO and BHE, respectively.
DXRW	I	55	Direction control of CPU control bus. When high, XIOWN, XIORN, XNWN and XNRN are driven by IOWN, IORN, MEMWN, and MEMRN respectively. When low, IOWN, IORN, MEMWN and MEMRN are driven by XIOWN, XIORN, XMWN, and XMRN respectively.
GSRWN	I	54	Enable control of SMWN and SMRN. When low, SMWN and SMRN are enabled.
RFMRN	I	5	Memory read pulse of refresh cycle. RFMRN is used in conjunction with RFCN signal.
RFCN	I	6	Refresh enable. When low, MEMRN, XMRN and SMRN are driven by RFMRN.
VI	I	63	Input of inverter.
VO	T	62	Output of inverter.
NDI1	I	57	Input of NAND gate.
NDI2	I	58	Input of NAND gate.
NDO	O	56	Output of NAND gate.
NDI1	I	60	Input of NOR gate.

NDI2	I	61	Input of NOR gate.
NOR	O	59	Output of NOR gate.

* Legend: I = Input Pin
O = Ouput Pin
Tri = Tri-state Pin (Input, Output, High-impedance)
O&H-Z = Output and High-impedance Pin

7.2.3 GAATDB

GAATDB has two data bus buffers (system data bus buffer and memory data bus buffer) and a low to high byte conversion buffer.

TABLE 7-2-5. GAATDB PIN ARRANGEMENT

SIGNAL NAME	I/O*	PIN NO.	PIN NO.	I/O*	SIGNAL NAME
D0	Tri	1	64		Vcc
D1	Tri	2	63	Tri	D15
D2	Tri	3	62	Tri	D14
D3	Tri	4	61	Tri	D13
MD0	Tri	5	60	Tri	D12
MD1	Tri	6	59	Tri	MD15
DMD	I	7	58	I	CBA
GMDHN	I	8	57	I	SBA
GMDLN	I	9	56	Tri	MD14
MD2	Tri	10	55	Tri	MD13
MD3	Tri	11	54	Tri	MD12
SD0	Tri	12	53	Tri	SD15
SD1	Tri	13	52	Tri	SD14
SD2	Tri	14	51	Tri	SD13
SD3	Tri	15	50	Tri	SD12
GNDA		16	49		GNDB
GNDB		17	48		GNDA
SD4	Tri	18	47	Tri	SD11
SD5	Tri	19	46	Tri	SD10
SD6	Tri	20	45	Tri	SD9
SD7	Tri	21	44	Tri	SD8
MD4	Tri	22	43	Tri	MD11
MD5	Tri	23	42	Tri	MD10
MD6	Tri	24	41	I	DD
D245	I	25	40	I	GDH-N
G245N	I	26	39	I	GDL-N
MD7	Tri	27	38	Tri	MD9
D4	Tri	28	37	Tri	MD8
D5	Tri	29	36	Tri	D11
D6	Tri	30	35	Tri	D10
D7	Tri	31	34	Tri	D9
Vcc		32	33	Tri	D8

* Legend: I = Input Pin
O = Output Pin
Tri = Tri-state Pin (Input, Output, High-impedance)

TABLE 7-2-6. GAATDB PIN DESCRIPTION

SYMBOL	I/O*	PIN NO.	NAME AND FUNCTION
D15-0	Tri	63-60,31-28 4-1,33-36	CPU data bus.
MD15-0	Tri	59,56-54,43, 42,38,37,27, 24,23,22,11, 10,6,5	Memory data bus.
SD15-0	Tri	53-50,47-44 21-18,15-12	System data bus.
DD	I	41	Direction control of CPU data bus(D15-0) buffer. When low, CPU reads data from MD15-0 or SD15-0.
GDHN	I	40	Enable control of CPU data bus high byte (D15-8) buffer. When low, it enables high byte.
GDLN	I	39	Enable control of CPU data bus low byte (D7-0) buffer. When low, it enables low byte.
CBA	I	58	Read data latch. SD7-0 are latched at CBA rising edge.
SBA	I	57	SBA selects latched or un-latched data. When high, latched data are selected. SBA is used in conjunction with CBA signal.
DMD	I	7	Direction control of Memory data bus (MD15-0) buffer. When high Memory data is read.
GMDHN	I	8	Enable control of Memory data high byte (MD15-8) buffer. When low, it enables high byte. GMDHN is used in conjunction with DMD signal.
GMDLN	I	9	Enable control of Memory data low byte (MD7-0) buffer. When low, it enables low byte. GMDLN is used in conjunction with DMD signal.
D245	I	25	Direction control of low to high byte conversion buffer. When low, it indicates high to low byte conversion during data transfers to 8-bit peripherals (write). When high, it indicates low to high byte conversion during data transfers from 8-bit peripherals (read).
G245N	I	26	Enable control of low to high byte conversion buffer. It is active low signal and is used in conjunction with D245 signal.

* Legend: I = Input Pin
O = Output Pin
Tri = Tri-state Pin (Input, Output, High-impedance)

7.2.4 GAATCK

GAATCK includes following functional blocks.
(1) Clock generator
--- CPU clock, 80287 clock, System clock,
DMA clock, 8042 clock, 8254 clock,
NTSC clock (14.31818 MHz)
(2) Ready circuit
(3) Reset circuit
(4) Bus controller
--- MEMR, MEMW, IOR, IOW, INTA, ALE, DTR, DEN
(5) Shut down circuit

TABLE 7-2-7. GAATCK PIN ARRANGEMENT

SIGNAL NAME	I/O*	PIN NO.	PIN NO.	I/O*	SIGNAL NAME
C14M	I	1	64		Vcc
HLDA	I	2	63	I	C48M
A1	I	3	62	I	COFF
RSWN	I	4	61	I	CDLY
RSWP	I	5	60	I	CSPD0
PWGD	I	6	59	I	CSPD1
(NC)		7	58		(NC)
(NC)		8	57		(NC)
(NC)		9	56	O	RSN
ENAS	O	10	55	O	C1M
DTR	O	11	54	O	EMEMR
ACKN	O	12	53	O	DEN
EALE	O	13	52	O	BALE
RSDV	O	14	51	O	AEN
CLKO	O	15	50	O	SCLK
GNDA		16	49		GNDB
GNDB		17	48		GNDA
MEMR	O&H-Z	18	47	O	OSC
MEMW	O&H-Z	19	46	O&H-Z	IOR
ALE	O	20	45	O&H-Z	IOW
INTA	O&H-Z	21	44	O	PCLKP
DCLK	O	22	43	O	PCLKN
RDY	O	23	42	O	RSCPU
(NC)		24	41	O	C8M
(NC)		25	40		(NC)
RC	I	26	39		(NC)
MSTR	I	27	38		(NC)
M1O	I	28	37	I	SRDY
S1	I	29	36	I	ARDY
S0	I	30	35	I	AREN
C20M	I	31	34	I	TEST
Vcc		32	33	I	CLKI

* Legend: I = Input Pin
O = Output Pin
O&H-Z = Output & High-impedance Pin

TABLE 7-2-8. GAATCK PIN DESCRIPTION

SYMBOL	I/O*	PIN NO.	NAME AND FUNCTION
C48M	I	63	Clock input. 48 MHz.
C20M	I	31	Clock input. 20 MHz.
C14M	I	1	Clock input. 14.31818 MHz.
PCLKP	O	44	(+) KB controller (8042) clock. 6 MHz.
PCLKN	O	43	(-) KB controller (8042) clock. 6 MHz.
OSC	O	47	Clock output. 14.31818 MHz. (for option slot)
C1M	O	55	Clock output. 1.19 MHz. (for 8254)
C8M	O	41	Clock output. 8 MHz, duty 33%. (for 80287)
DCLK	O	22	DMA CLOCK
SCLK	O	50	System clock.
CLKO	O	15	CPU clock output.
CLKI	I	33	CPU clock input. CLKI should be connected to CLKO externally.
CSPD1	I	59	CPU clock select.
CSPD0	I	60	CPU clock select.

CSPD1	CSPD0	SCLK	CLKO	CLKI	DCLK
0	1	6 MHz	12 MHz	12 MHz	3 MHz
1	1	8 MHz	16 MHz	16 MHz	4 MHz
1	0	10 MHz	20 MHz	20 MHz	5 MHz
0	0	12 MHz	24 MHz	24 MHz	6 MHz

PWGD	I	6	Power good. When low, it indidates that power is not good and reset signals (RSN, RSDV, RSCPU) are activated.
RSWN	I	4	(-) Reset switch activation signal. RSWN becomes low.
RSWP	I	5	(+) Reset switch activation signal. RSWP becomes low.
RSN	O	56	(-) Reset signal. (for internal circuit)
RSDV	O	14	(+) Reset signal. (for option slot)
AREN	I	35	(-) Asynchronous ready and synchronous ready enable.
ARDY	I	36	(-) Asynchronous ready input. It is used in conjunction with AREN signal.
SRDY	I	37	(-) Synchronous ready input. It is used in conjunction with AREN signal.
RDY	O	23	(-) Ready output.
MIO	I	28	Memory or I/O select. When low, the current bus cycle is in the I/O space.
S1	I	29	Bus cycle status.
S0	I	30	Bus cycle status.

MIO	S1	S0	Type of bus cycle
0	0	0	INTA
0	0	1	IO READ
0	1	0	IO WRITE
0	1	1	NONE, IDLE
1	0	0	HALT OR SHUT DOWN

1	0	1	MEMORY READ
1	1	0	MEMORY WRITE
1	1	1	NONE, IDLE

COFF	I	62	(+) Control off. When high, command and DEN signal are forced inactive.
CDLY	I	61	Command delay. When high, the start of command output is delayed.
HLDA	I	2	Hold acknowledge. When high, command output becomes 3-state off.
ALE	O	20	Address latch enable.
DEN	O	53	Data bus enable.
DTR	O	11	Data transmit/receive. When high, this control output indicates that a write bus cycle is being performed.
MEMR	O&H-Z	18	(-) Memory read command.
MEMW	O&H-Z	19	(-) Memory write command.
IOR	O&H-Z	46	(-) I/O read command.
IOW	O&H-Z	45	(-) I/O write command.
INTA	O&H-Z	21	(-) Interrrupt acknowledge.
EMEMR	O	54	(-) Early memory read signal.
EALE	O	13	Early address latch enable.
BALE	O	52	Buffered address latch enable.
MSTR	I	27	(-) Master. A processor or DMA controller on the I/O channel may pull this signal low.
ACKN	O	12	(-) Acknowledge. When low, DMA controller (or refresh controller) has control of the address bus, data bus and control bus.
AEN	O	51	(+) Address enable.
A1	I	3	Address 1.
RC	I	26	(-) Reset CPU input from 8042.
RSCPU	O	42	(+) Reset CPU output. When high, CPU is reset. RSCPU becomes active when: (1) PWGD is low. (2) Reset switch is activated. (3) 8042 pulls RC signal low. (4) CPU executes shutdown cycle.
ENAS	O	10	(-) Enable control of RTCAS (RTC address strobe) signal.
TEST	I	34	(-) Test input. TEST should be pulled high.

* Legend: O = Output
I = Input
O&H-Z = Output & High-impedance Pin

7.2.5 GAATM2

GAATM2 generates memory address and RAS, CAS, WE signals used with GAATM1 and the delay line to control DRAM.

TABLE 7-2-9. GAATM2 PIN DESCRIPTION

SYMBOL	I/O*	PIN NO.	NAME AND FUNCTION
SA18-0	I	3,5,6,13-16, 18,20-24, 27-32	System address bus.
MA8-0	O	44,43,41,40, 9-7,12,11	DRAM address bus.
MEMR	I	61	(-) System memory read signal.
MEMW	I	62	(-) System memory write signal.
EMRN	I	46	(-) Early memory read signal.
XMWN	I	63	(-) Internal memory write signal.
RFHN	I	64	(-) Refresh signal.
D40	I	52	40 ns delayed signal from RAS.
D80	I	50	80 ns delayed signal from RAS.
D160	I	48	160 ns delayed signal from RAS.
D200	I	47	200 ns delayed signal from RAS.
RA1	I	35	(+) RA1 signal is used to generate RAS1 signal.
RA0	I	37	(+) RA0 signal is used to generate RAS0 signal.
CAH	I	38	(+) CAH signal is used to generate CASH signal.
CAL	I	39	(+) CAL signal is used to generate CASL signal.
RAS1	O	59	(-) Row address strobe for DRAM (80000H-9FFFFH).
RAS0	O	60	(-) Row address strobe for DRAM (0H-7FFFFH)
CASH	O	56	(-) Column address strobe for DRAM (0H-9FFFFH, odd byte).
CASL	O	55	(-) Column address strobe for DRAM (0H-9FFFFH, even byte).
WE	O	45	(-) Write enable signal for DRAM.
RAS	O	53	(+) RAS is generated from logical OR of MEMR and MEMW. This output is used to generate delay signals (D40, D80, D160, D200)
TEST	I	54	(-) Test input. TEST should be pulled up.

* Legend: I = Input Pin
O = Ouput Pin

7.2.6 GAATIO

GAATIO includes following functional blocks.

(1) Address decoder of I/O space.
(2) DMA page register (74LS612 compatible)
(3) Port B.
(4) NMI enable register.
(5) Address latch for DMA.
(6) Interface circuit between NP (80287) and CPU (80286).
(7) General purpose gates.
--- 1 inverter, 1 NAND gate, two 3-state buffers.

TABLE 7-2-10. GAATIO PIN DESCRIPTION

SYMBOL	I/O*	PIN NO.	NAME AND FUNCTION
XD7-0	Tri	38-31	Internal data bus.
A23-17	O&H-Z	66,68,70,72, 74,76,80	CPU address bus.
XA16-10	O&H-Z	77,75,73,71, 69,67,64	>
XA9-8	Tri	62,63	> Internal address bus.
XA7-1	I	61-55	>
XA0	I	52	>
XIWN	I	12	(-) Internal I/O write signal. (= -XIOW)
XIRN	I	11	(-) Internal I/O read signal. (= -XIOR)
RSTN	I	30	(-) Reset.
DK7N	I	21	-DACK7. DMA acknowledge 7.
DK6N	I	20	-DACK6. DMA acknowledge 6.
DK4N	I	19	-DACK4. DMA acknowledge 4.
DK3N	I	18	-DACK3, DMA acknowledge 3.
DK2N	I	17	-DACK2. DMA acknowledge 2.
DK0N	I	16	-DACK0. DMA acknowledge 0.
DAK4	I	14	+DACK4. This signal is output.
RFHN	I	85	(-) Refresh signal.
ACKN	I	86	(-) DMA acknowledge. ACKN is active when DMA or refresh cycle is being performed.
STB2	I	26	(+) DMAC-NO2 (16-bit DMA controller) address strobe signal.
STB1	I	27	(+) DMAC-NO1 (8-bit DMA controller) address strobe signal.
AEN2	I	22	(+) Address enable signal of DMAC-NO2.
AEN1	I	23	(+) Address enable signal of DMAC-NO1.
AE02	0	96	(-) AE02 is active when DMAC-NO2 has control of the system.
AE01	0	97	(-) AE01 is active when DMAC-NO1 has control of the system.
MSTN	I	87	-MASTER. When low, it indicates that the master on the option slot (DMAC or CPU on the slot) has the control of the system.

ITAN	I	100	-INTA. Interrupt acknowledge.
SMIO	I	88	Memory or I/O select.
NERN	I	8	(-) NP (80287) error.
NBSN	I	7	(-) NP (80287) busy.
Q1	I	89	Q1 is a timing signal to generate RTAS signal.
ENAS	I	98	(-) Enable control ot RTAS signal.
CD2N	O	24	(-) Chip select of DMAC2 (8237).
CD1N	O	25	(-) Chip select of DMAC1 (8237).
CI2N	O	42	(-) Chip select of INTC2 (8259).
CI1N	O	41	(-) Chip select of INTC1 (8259).
CTMN	O	47	(-) Chip select of system TIMER (8254).
CKBN	O	99	(-) Chip select of keyboard controller (8042).
RTRW	O	44	(-) Write signal of real time clock (HD146818).
RTDS	O	45	(-) Read signal of RTC (HD146818)
RTAS	O	46	(+) ALE signal of RTC (HD146818).
NPRS	O	6	(+) NP (80287) reset signal.
NCSN	O	5	(-) Chip select NP (80287).
CBSN	O	9	(-) CPU (80286) busy signal.
IR13	O	43	(+) Interrupt request 13.
DXD	O	39	Direction control of 8 bit internal data bus (XD7-0) buffer.
NMI	O	10	(+) Non-maskable interrupt request.
SPEK	O	51	Output signal for speaker.
TM2G	O	48	Timer CH2 gate. This signal is connected to channel 2 gate input of timer LSI (8254).
ENPR	O	81	(+) Enable RAM parity check.
IOEN	O	92	I/O channel error (option slot).
OUT2	I	49	Timer CH2 output. This signal is connected to channel 2 output of timer LSI (8254).
PCKN	I	82	(-) Parity check error.
VI	I	84	Input of inverter.
VO	O	83	Output of inverter.
NA1I	I	95	Input of NAND gate.
NA2I	I	94	Input of NAND gate.
NADO	O	93	Output of NAND gate.
TS2O	O&H-Z	91	Output of 3-state buffer.
TSI	I	1	Enable control (active low) of 3-state buffer.
TSO	O&H-Z	2	Output of 3-state buffer.
TSVI	I	13	Enable control (active low) of 3-state buffer.
TSVO	O&H-Z	50	Output of 3-state buffer.

* Legend:
I = Input Pin
O = Ouput Pin
Tri = Tri-state Pin (Input, Output, High-impedance)
O&H-Z = Output & High-impedance Pin

7.2.7 GAATM1

GAATM1 includes the following functional blocks.

1. Address decoder for ROM and DRAM
2. Parity checker / generator
3. Additional circuitry for the memory expansion card
   (This circuit is not used in EQUITY III+ / EPSON PC AX.)

TABLE 7-2-11. GAATM1 PIN DESCRIPTION

SYMBOL	I/O*	PIN NO.	NAME AND FUNCTION
A23-17	I	3-9	CPU address bus.
RFHN	I	17	(-) Refresh signal.
XAJ	I	2	ROM address select. XA16 or XA15 should be connected to XAJ. ROM address range: CSFN / CSEN XAJ = XA16: 0F0000-0FFFFF / 0E0000-0EFFFF; FF0000-FFFFFF / FE0000-FEFFFF XAJ = XA15: 0F8000-0FFFFF / 0F0000-0F7FFF; FF8000-FFFFFF / FF0000-FF7FFF; (0E8000-0EFFFF) / (0E0000-0E7FFF); (FE8000-FEFFFF) / (FE0000-FE7FFF)
ALE	I	15	(+) Address latch enable.
HLDA	I	16	(+) Hold acknowledge.
XMRN	I	14	(-) Internal memory read signal.
XBHE	I	18	Internal bus high enable signal.
XA0	I	19	Internal address bus 0.
JRAH	I	60	(+) Enable control of RAM from 080000H to 09FFFFH.
JRAL	I	59	(+) Enable control of RAM from 040000H to 07FFFFH.
JEFN	I	56	(-) RAM address select. When low, RAM address is assigned from F00000H to F9FFFFH. This input should be high or open in EQUITY III+ / EPSON PC AX.
JE0	I	57	(+) RAM address select. When high, RAM address is assigned from 000000H to 09FFFFH. This input should be high or open in EQUITY III+ / EPSON PC AX.
JROM	I	55	(+) Enable control of ROM. When high, ROM is enabled. This input should be high or open in EQUITY III+ / EPSON PC AX.
J1MN	I	28	(-) Chip select input for memory expansion card which uses 1Mbit RAM chips. This input should be high or open in EQUITY III+ / EPSON PC AX.

JKN	I	25	(-) Chip select input for memory expansion card which uses 256Kbit RAM chips. This signal should be high or open in EQUITY III+ / EPSON PC AX.
RA23	I	23	(+) Timing input for RS3N and RS2N. (When GAATM1 is used in memory expansion card.) This signal is not used in EQUITY III+ / EPSON PC AX, and should be high or open.
D40	I	24	40 ns delayed signal from RAS. (When GAATM1 is used in memory expansion card.) This signal is not used in EQUITY III+ / EPSON PC AX, and should be high or open.
LMGN	O	10	(-) Chip select of low order 1Mbyte memory space. LMGN is active when memory space from 000000H to 0FFFFFH is accessed.
CRON	O	12	(-) ROM chip select.
CRAN	O	11	RAM chip select.
CSFN	O	53	(-) Read signal of BIOS ROM.
CSEN	O	54	(-) Read signal of reserved ROM.
RA1	O	64	(+) RA1 signal is used to generate RAS1 signal in GAATM2.
RA0	O	63	(+) RA0 signal is used to generate RAS0 signal in GAATM2.
CAH	O	62	(+) CAH signal is used to generate CASH signal in GAATM2.
CAL	O	61	(+) CAL signal is used to generate CASL signal in GAATM2.
RS3N	O	31	(-) Row address strobe for DRAM. (When GAATM1 is used in memory expansion card.) This signal is not used in EQUITY III+ / EPSON PC AX.
RS2N	O	30	(-RAS2) Row address strobe for DRAM. (When GAATM1 is used in memory expansion card.) This signal is not used in EQUITY III+ / EPSON PC AX.
DMD	O	13	Direction control of memory data bus buffer.
MA9	O	29	Dynamic RAM address 9. (When GAATM1 is used in memory expansion card.) This signal is not used in EQUITY III+ / EPSON PC AX.
DM15-0	I	48-33	Memory data bus.
MP01	I	50	Parity bit of odd address byte. MP01 is parity-checked with MD15-8 in memory read cycle.
MP00	I	52	Parity bit of even address byte. MP00 is parity-checked with MD7-0 in memory read cycle.
MPI1	O	49	Parity bit of odd address byte. MPI1 is generated from MD15-8 in memory write cycle.
MPI0	O	51	Parity bit of even address byte. MPI0 is generated from MD7-0 in memory write cycle.
EPR1	I	21	(+) Enable RAM parity check. When high, parity check circuit is enabled. And when low, parity check circuit is cleared.
EPR2	I	22	(-) Enable RAM parity check. This signal is not used in EQUITY III+ / EPSON PC AX, and should be pulled down.
PCKN	O	20	(-) Parity error signal. When low, it indicates that parity error has occurred.
ERON	O&H-Z	32	(-) Parity error signal. 3-state output. This signal is not used in EQUITY III+ / EPSON PC AX.

* Legend: I = Input Pin
O = Output Pin
O&H-Z = Output & High-impedance Pin

In EQUITY III+ / EPSON PC AX the following signals are not used.

INPUT

JEFN JEO JROM J1MN JKN RA23 D40 : high or open

EPR2 : low

OUTPUT

RS3N RS2N MA9 ERON : no connection

7.2.8 GAATRF

GAATRF includes the following functional blocks.

1. DRAM refresh control circuit.
2. DMA control circuit.
3. 16 <--> 8 data conversion circuit.
4. Wait states insertion circuit.
5. Command delay control circuit.
6. XA0, XBHE control circuit.

TABLE 7-2-12. GAATRF PIN DESCRIPTION

SYMBOL	I/O*	PIN NO.	NAME AND FUNCTION
WS0	I	15	Zero wait insertion. When low, wait state is not inserted. -0WS signal of option slot is connected to this pin.
WS1	I	40	Wait states control of BIOS-ROM access. The number of wait states of BIOS-ROM (0E0000-0FFFFF, FE0000-FFFFFF) is controlled by WS1.
WS2	I	39	Wait states control of 16-bit memory devices on the option card which activates -MEMCS16 signal.
WS3	I	38	
A0	I	44	CPU address bus 0.
ALE	I	11	(+) Address latch enables.
MEMR	I	7	(-) System memory read signal.
MEMW	I	8	(-) System memory write signal.
IOR	I	9	(-) System I/O read signal.
IOW	I	10	(-) System I/O write signal.
INTA	I	12	(-) Interrupt acknowledge.
CSRA	I	48	(-) Chip select signal of internal DRAM (0-09FFFF).
CSR0	I	47	(-) Chip select signal of internal ROM (0E0000---0FFFFF, FE0000-FFFFFF).
M16	I	17	(-) Chip select signal of 16-bit memory devices on the option slot. (-MEMCS16 signal of option slot is connected to this pin.)

CSPD	WS1	Wait states
0 (10 MHz)	0	2
0 (10 MHz)	1	1
1 (6 or 8 MHz)	*	1

(* : don't care)

CSPD	WS3	WS2	Wait states
0 (10 MHz)	0	0	4
0 (10 MHz)	0	1	3
0 (10 MHz)	1	0	2
0 (10 MHz)	1	1	1
1 (6 or 8 MHz)	*	*	1

(* : don't care)

IO16	I	18	(-) Chip select signal of 16-bit I/O devices on the option slot. (-IOCS16 signal of option slot is connected to this pin.)
IRDY	I	61	(+) I/O channel ready signal. (+IOCHRDY signal of option slot is connected to this pin.)
NPCS	I	45	(-) Chip select signal of numerical processor (80287).
CSPD	I	52	CPU speed select.

CSPD	CPU speed
0	10 MHz
1	6 or 8 MHz

Q1	O	2	(+) Q1 signal is active from phase 2 of first Tc cycle to phase 1 of last Tc cycle.
ARFY	O	25	(-) Asynchronous ready.
AREN	O	16	(-) Asynchronous ready enable.
COFF	O	60	(+) Control off. This signal becomes active during 16 <--> 8 conversion. While COFF is active, control signals (-MEMR, -MEMW, -IOR,-IOW) are disabled.
LSA0	O	23	Latched and converted address 0.
AEN1	I	43	(-) DMA channel 1 (8-bit DMA) address enable.
AEN2	I	42	(-) DMA channel 2 (16-bit DMA) adress enable.
DAEN	O	32	(-) DMA enable. (channel 1 and channel 2)
XA0	Tri	49	Internal address bus 0.
XBHE	Tri	35	Bus high enable.

-AEN1	-AEN2	XA0	XBHE
1	1	input	input
0	1	input	-XA0 (output)
1	0	0 (output)	0 (output)

DEN	I	5	(+) Data bus enable.
DTR	I	4	Data transmit ot receive. When high, data is transmitted from CPU to memory or I/O.
GDL	O	57	(-) Enable control of CPU data bus low byte buffer (in GAATDB).
GDH	O	56	(-) Enable control of CPU data bus high byte buffer (in GAATDB).
G245	O	54	(-) Enable control of 16 <--> 8 conversion buffer (in GAATDB).
D245	O	55	Direction control of 16 <--> 8 conversion buffer (in GAATDB).
MIO	I	14	Memory or I/O select. CPU M/-IO signal is connected to this pin. When high, memory cycle is being executed.
CDLY	O	59	(+) Command delay. While active, the start of commands (-MEMR, -MEMW, -IOR, -IOW) are delayed.

CSPD	AREA	Command delay
0 (10 MHz)	16-bit memory	0
0 (10 MHz)	other	1
1 (6,8 MHz)	16-bit memory	0
1 (6,8 MHz)	other	0.5

OUT1	I	21	OUT1 signal of 8254 (Timer LSI)
HRQ1	I	22	(+) Hold request input from 8237 (DMAC LSI).
XMW	I	46	(-) Internal memory write signal.
HRQ	O	30	(+) Hold request output to CPU.
HLDA	I	3	(+) Hold acknowledge input from CPU.
HAK1	O	31	(+) Hold acknowledge output to 8237 (DMAC LSI).
RFNO	O	28	(-) Refresh signal. This signal is generated in GAATRF.
RFNI	I	63	(-) Refresh signal input.
RFPO	O	24	(+) Refresh signal.
RF1D	O	37	(-) Refresh signal which is delayed by one DMA clock cycle from RFNI signal.
RF2D	O	36	(-) Refresh signal which is delayed by two DMA clock cycles from RFNI signal.
DMMR	I	41	(-) DMA memory read signal.
XIOR	I	50	(-) Internal I/O read signal.
DRDY	O	29	(+) DMA ready signal.
XMR	O&H-Z	64	(-) Internal memory read signal.
CA20	I	34	CPU address bus 20. A20 signal of CPU is connected to this pin.
A20G	I	33	(+) Gate signal of A20. P21 signal of 8042 (one chip CPU) is connected to this pin.
A20	O&H-Z	62	System address bus 20.

CA20	A20G	A20
0	1	0
1	1	1
*	0	0 (* : don't care)

CLK	I	51	Processor clock.
SCLK	I	6	System clock.
DCLK	I	13	DMA clock.

CPU speed	CLK	SCLK	DCLK
6 MHz	12 MHz	6 MHz	3 MHz
8 MHz	16 MHz	8 MHz	4 MHz
10 MHz	20 MHz	10 MHz	5 MHz

RST	I	20	(-) Reset input.
RSTO	O	19	(+) Reset output.
TEST	I	53	(-) Test input.

* Legend:
I = Input Pin
O = Output Pin
Tri = Tri-state Pin (Input, Output, High-impedance)
O&H-Z = Output & High-impedance Pin

7.2.9 GAATSP

GAATSP includes the following functional blocks.

1. Address decoder for serial port (UART, 16450 or 8250)
2. Parallel port. (PTDR: printer data register,
   PTSR: printer status register,
   PTCR: printer control register)
3. Oscillator for UART. (1.8432 MHz output)
4. General purpose 3-state gate.

TABLE 7-2-13. GAATSP PIN DESCRIPTION

SYMBOL	I/O*	PIN NO.	NAME AND FUNCTION
SA9-0	I	13-4	Address bus
SD7-0	Tri	22,24,29,31 54,56,61,63	Data bus
IOWN	I	17	(-) I/O write pulse.
IORN	I	16	(-) I/O read pulse.
AEN	I	14	(+) Address enable. This signal becomes high, when DMA cycle is being executed.
RES	IS	32	(+) Reset.
PIF1	I	20	Address select pin for parallel port.
PIF0	I	21	Address select pin for parallel port.
			PIF1 PIF0 parallel port address 1 1 378, 379, 37A 1 0 278, 279, 27A 0 1 3BC, 3BD, 3BE 0 0 disable
SIF1	I	18	Address select pin for serial port.
SIF0	I	19	Address select pin for serial port.
			SIF1 SIF0 serial port address 1 1 3F8 --- 3FF 1 0 2F8 --- 2FF 0 1 disable 0 0 disable
XT1		51	Crystal input. (3.6864 MHz)
XT2		50	Crystal input. (3.6864 MHZ)
OSC	O	52	1.8432 MHz clock output.
TSA	I	48	Data input of 3-state buffer.
TSC	I	49	Control input of 3-state buffer.
TSY	O&H-Z	47	Output of 3-state buffer.
OD7-0	O	23,25,28,30 55,57,60,62	Printer data bit 7-0.
OSLI	O		(-) Printer select.
OINI	O	41	(-) Printer initialize.
OATF	O	43	(-) Auto feed.

OSTB	O	45	(-) Printer data strobe pulse.
SLN	I	38	(-) Printer select.
INI	I	40	(-) Printer initialize.
ATF	I	44	(-) Auto feed.
STB	I	46	(-) Printer data strobe pulse.
BSY	I	34	(+) Printer busy.
ACK	I	33	(-) Acknowledge.
EOP	I	35	(+) End of paper.
SLP	I	36	(+) Printer select.
ERR	I	37	(-) Printer error.
IRQ	O&H-Z	15	(+) Interrupt request. IRQ becomes active, when -ACK signal becomes low and interrupt request is enabled.
OIRE	O	3	(-) Interrupt request enable.
ACKP	O	2	(+) Acknowledge.
SCSN	O	53	(-) Chip select signal of serial port.
DDIR	O	64	(-) Direction control of data buffer. This signal is active while serial port or parallel port are being read.

* Legend:
I = Input Pin
O = Output Pin
Tri = Tri-state Pin (Input, Output, High-impedance)
O&H-Z = Output & High-impedance Pin

7.2.10 GAATFD

GAATFD includes the following functional blocks.

1. Address decoder for FDC(765) and I/O registers.
2. I/O register.
   FDOR : Floppy digital output register.
   FCR : Floppy control register.
3. Write precompensation circuit.
4. Clock circuit
5. DMA request circuit.

TABLE 7-2-14. GAATFD PIN DESCRIPTION

SYMBOL	I/O*	PIN NO.	NAME AND FUNCTION
BA9-0	I	8-2,64-62	Address bus.
BD5-0	I	14-19	Data bus.
IOWN	I	11	(-) I/O write pulse.
IORN	I	10	(-) I/O read pulse.
AEN	I	9	(+) Address enable. This signal becomes high, when DMA cycle is being executed.
RSE	I	52	(+) Reset.
FDI1	I	46	Address select pin for FDC.
FDI0	I	45	Address select pin for FDC. FDI1 FDI0 FDC address AT/XT 1 1 3F0 --- 3F7 AT port1 1 0 370 --- 377 AT port2 0 1 3F0 --- 3F7 XT 0 0 disable (When FDI1, FDI0 = 0, 1 Floppy control register can not be accessed.)
MOT2	O	30	(+) Motor enable 2. (DRIVE B)
MOT1	O	29	(+) Motor enable 1. (DRIVE A)
DS2	O	25	(+) Drive select 2. (DRIVE B)
DS1	O	24	(+) Drive select 1. (DRIVE A)
FRES	O	49	(+) FDC (765) reset signal.
RWC	O	23	(+) Reduced write current.
3X7N	O	32	(-) Read 3X7 signal. This signal becomes active while I/O address 3X7 is read. X means F (when FDI0=1) or 7 (when FDI0=0)
3XVN	O	47	(-) Chip select of 3X6 and 3X7. This signal becomes active while I/O address 3X6 or 3X7 are accessed.
FCSN	O	44	(-) Chip select of FDC (765).
BDIR	O	59	(-) Direction control of data buffer. This signal is active while FDC (765) is being read. (CPU access or DMA transfer)

DREN	O	60	(-) Enable DMA and interrupt.
DAKN	I	12	(-) DMA acknowledge. (input from 8237)
FDAN	O	50	(-) DMA acknowledge. (output to 765)
BTC	I	13	(+) Terminal count. (input from 8237)
FTC	O	42	(+) Terminal count. (output to 765)
FDRQ	I	40	(+) DMA request. (input from 765)
DRQ	O	61	(+) DMA request. (output to 8237)
FWD	I	35	(+) Write data. (input from 765)
WE	I	36	(+) Write enable. (input from 765)
PS1	I	33	Peak shift. (input from 765)
PS0	I	34	Peak shift. (input from 765)
WD	O	28	(+) Write data. (output to FDD)
C48	I	55	48 MHz clock input.
TEST	I	38	(-) Test pin.
MIN	O	48	Mini/Standard. (for SED9420)
OSC	O	57	16/9.6 MHz clock output. (for SED9420)
CLK	O	54	FDC clock. (8/4.8/4 MHz)
WCLK	O	56	FDC write clock. (1M/600K/500K Hz)
FINT	I	41	(+) Interrupt request of FDC. (input from 765)
SYNC	I	43	VFO synchronize. (input from 765)
VDRQ	O	53	(+) VFO DREQ. (for SED9420)
SIDE	I	51	(+) Side select. (Head select, input from 765)
HS	O	22	(+) Head select. (output to FDD)
INV	I	20	Input of inverter.
INVN	O	21	Output of inverter.
SEEK	I	37	(+) Seek. (input from 765)
DTK0	I	31	(+) Track 0. (input from FDD)
TRK0	O	39	(+) Track 0. (output to 765)

* Legend: I = Input Pin
O = Output Pin

DIAGNOSTICS PROGRAM

CONTENTS

1. System Board Check

This module checks the operation of each IC contained in the systemboard. The checking operation is performed in the following order, and the program displays an error message when some error is detected. If no error is detected, the program displays no error message.

1. 80286 Processor check
2. 146818 CMOS shutdown byte check
3. 27256 ROM checksum check
4. 8254 Timer Counter check
5. 8237 DMA Controller check
6. SN74LS612 DMA Page resister check
7. 8237 Memory reflesh check
8. 8042 Keyboard Controller check
9. 80286 instruction check
10. 146818 CMOS checksum and battery check
11. 8259 Interrupt Controller check
12. 8254 Timer Counter speed check
13. 80286 protect mode check

When the system board check is started, the program displays following message.

```
+-------------------------------------------------------------+
|                                                             |
|    SYSTEM BOARD CHECK                                       |
|                                                             |
+-------------------------------------------------------------+
```

The remainder of this section describes the procedures for each checking operation.

1) 80286 Processor Check

The 80286 Processor check performs writing and reading checks on the 80286 flags and segment registers.

a. "0ffh" is stored (safh) into the 8080 flag, then re-loaded (lahf). The flags are checked and it is considered an error if any of the below flags are not set (if the flag = 0):

   CF (Carry Flag)
   ZF (Zero Flag)
   PF (Parity Flag)
   SF (Sign Flag)
   AF (Auxiliary Carry-BCD)

The error message is as follows:

```
+-----------------------------------------------------------------+
|                                                                 |
|   Error code = 101                                              |
|   80286 CPU ERROR                                               |
|                                                                 |
+-----------------------------------------------------------------+
```

b. "00h" is stored (safh) into the 8080 flag, then re-loaded (lahf). The flags are checked and the program displays an error message if any of the flags listed in Item a. above are not reset (if the flag = 1).
The error message is identical to that of Item a.

c. "0aa55h" is sequentially written to and read from Registers es, ds, and ss, then their values are checked. The program displays an error message if the results do not match the initial values.
The error message is identical to that of Item a.

d. Using "055aah" as the test data, a check identical to that described in Item c. is conducted.
The error message is identical to that of Item a.

2) 146818 CMOS Shutdown Byte Check

The 146818 CMOS shutdown byte check performs a WRITE/READ check on the shutdown byte of the 146818 CMOS.

a. The shutdown byte of offset 8fh of the CMOS is selected, "01" is written and read, and the value is checked. The program displays an error message if the result does not match the initial value.

```
+-----------------------------------------------------------------+
|                                                                 |
|   Error code = 110                                              |
|   146818 CMOS SHUTDOWN BYTE ERROR                               |
|                                                                 |
+-----------------------------------------------------------------+
```

b. The test data of Item a. above is shifted to the left, then a check identical to that described in Item a. is performed for all eight bits.
The error message is identical to that of Item a.

c. Using "0aah" as the test data, a check identical to that described in Item a. is performed.
The error message is identical to that of Item a.

d. Using "055h" as the test data, a check identical to that described in Item a. is performed.
The error message is identical to that of Item a.

e. "00h" is written to the shutdown byte, then this operation is terminated.

3) 27256 ROM Checksum Check

The 27256 ROM checksum check performs a check on the sum total of all 27256 ROM data in byte units, then confirms whether or not that sum equals "00h". The program displays an error message if the sum does notequal "00h".

```
+-----------------------------------------------------------------+
|                                                                 |
|    Error code = 102                                             |
|    27256 ROM CHECKSUM ERROR                                     |
|                                                                 |
+-----------------------------------------------------------------+
```

4) 8254 Timer Counter Check

The 8254 Timer Counter check performs a check of the setting and reading operation of the counter register of the 8254 Timer Counter.

Count "0" of the 8254 Timer Counter is latched and the count value is checked. Next, a check is repeatedly performed to confirm that all 16 bits have the value of "1". The program displays an error message ifany bit of the count value of "1" cannot be read.

```
+-----------------------------------------------------------------+
|                                                                 |
|    Error code = 103                                             |
|    8254 TIMER COUNTER REGISTER ERROR                            |
|                                                                 |
+-----------------------------------------------------------------+
```

5) 8237 DMA Controller Check

The 8237 DMA Controller check performs a WRITE/READ check on the eight registers (Port Nos. 00h to 07h) of the first 8237 DMA Controller and on the eight registers (Port Nos. C0h, C2h to CEh) of the second 8237 DMA Controller.

The test data is used in the sequence of "0000h", "5555h", "0aaaah", and "0ffffh". If an error is detected, the following message will be displayed:

```
+-----------------------------------------------------------------+
|                                                                 |
|    Error code = 105                                             |
|    8237 DMA CONTROLLER REGISTER ERROR                           |
|                                                                 |
+-----------------------------------------------------------------+
```

6) SN74LS612 DMA Page Register Check

The SN74LS612 DMA Page register check performs a WRITE/READ check on the 15 registers (Port Nos. 81h to 8Fh) of the SN74LS612 Page Register.

The test data is used in the sequence of "00h", "55h", "0aah", and "0ffh". If an error is detected, the following message will be displayed:

```
+------------------------------------------------------------------+
|                                                                  |
|    Error code = 106                                              |
|    612 DMA PAGE REGISTER ERROR                                   |
|                                                                  |
+------------------------------------------------------------------+
```

7) 8237 Memory Refresh Check

The 8237 Memory refresh check performs a repeated check on the refresh detect bit of Port No. 61h, and checks if its status makes a change.

The program displyas an error message if the status does not change.

```
+------------------------------------------------------------------+
|                                                                  |
|    Error code = 105                                              |
|    8237 DMA REFRESH ERROR                                        |
|                                                                  |
+------------------------------------------------------------------+
```

8) 8042 Keyboard Controller Check

The 8042 Keyboard Controller check performs a check on the operating status of the Keyboard Controller.

a. The status of the Keyboard Controller is repeatedly checked, and the program displays an error message if its input buffer is not empty.

```
+------------------------------------------------------------------+
|                                                                  |
|    Error code = 107                                              |
|    8042 TIME OUT ERROR                                           |
|                                                                  |
+------------------------------------------------------------------+
```

b. The Self-test command is output to the Keyboard Controller so that it will execute a self-diagnostic test. If an error is detected, the following message will be displayed:

```
+-----------------------------------------------------------+
|                                                           |
|   Error code = 108                                        |
|   8042 SELF DIAGNOSTIC ERROR                              |
|                                                           |
+-----------------------------------------------------------+
```

c. The Read Input Code command is output to the Keyboard Controller, and the program displays an error message if it does not assume the "Input buffer empty" status.
The error message is identical to that of Item a. above.

d. The Write Keyboard Controller's Command Byte command is output tothe Keyboard Controller, and the program displays an error messageif it does not assume the "Input buffer empty status.
The error message is as follows:

```
+-----------------------------------------------------------+
|                                                           |
|   Error code = 108                                        |
|   8042 WRITE COMMAND ERROR                                |
|                                                           |
+-----------------------------------------------------------+
```

e. The mode of the Keyboard Controller is reset to the following modes and this operation is terminated.

PC Compatible Mode
Disable Keyboard
Inhibit Override
System flag
Enable Output-Buffer-Full Interrupt

9) 80826 Instruction Check

The 80826 Instruction check performs a WRITE/READ test on the System Table Registers IDTR and GDTR as well as a SET/RESET test on the direction flag and interrupt enable flag of the CPU flags.

a. The test data "0aaaah" is written to and read from IDTR and GDTR, then their values are checked. The program displays an error message if the results do not match the initial values.

```
+-----------------------------------------------------------+
|                                                           |
|   Error code = 113                                        |
|   80286 INSTRUCTION ERROR                                 |
|                                                           |
+-----------------------------------------------------------+
```

b. Using the test data "5555h" and "0000h", an identical check is performed.
The error message is identical to that of Item a. above.

c. "0ffffh" is set at IDTR.

d. The direction flag and interrupt enable flag are set using the STD and STI instructions, and the status of the CPU flags is checked. It is considered an error if the direction flag and interrupt enable flag are not set.
The error message is identical to that of Item a.

e. Similarly, the direction flag and interrupt enable flag are reset using the CLD and CLI instructions, and the status of the CPU flags is checked.
The error message is identical to that of Item a.

10) 146818 CMOS Checksum and Battery Check

The 146818 CMOS checksum and battery check performs a check on the battery status of the CMOS and the checksum.

a. The CMOS battery status is read to check if the battery is all right. If not, the program displys following error message.

```
+-----------------------------------------------------------------+
|                                                                 |
|   Error code = 111                                              |
|   146818 CMOS BATTERY ERROR                                     |
|                                                                 |
+-----------------------------------------------------------------+
```

b. The CMOS shutdown byte is read to check if it is in "Shutdown OK" status. If so, this operation is terminated here; if not, execution proceeds to the checking of the checksum.

c. The total sum of the data from CMOS offset 90h to 0adh is calculated, and the program displys an error message if the resulting value equals zero.

```
+-----------------------------------------------------------------+
|                                                                 |
|   Error code = 112                                              |
|   146818 CMOS CHECKSUM ERROR                                    |
|                                                                 |
+-----------------------------------------------------------------+
```

d. The total sum of the data from CMOS offset 90h to 0adh is compared with the checksum value (CMOS offset 0aeh and 0afh), and the program displys an error message if they do not match.
The error message is identical to that of Item c.

11) 8259 Interrupt Controller Check

The 8259 Interrupt Controller check performs the following checks on 8259.

a. The masking of all interrupts is reset, then a READ check is performed on the mask register.

b. The masking of all interrupts is set, then a READ check is performed on the mask register.

c. Interrupt state of the CPU is enabled in a status where all interrupts are masked, and the program displays an error message if an interrupt occurs.

If an error is detected during the above checks, the program displays following error message:

```
+-----------------------------------------------------------------+
|                                                                 |
|    Error code = 109                                             |
|    8259 INTERRUPT CONTROLLER ERROR                              |
|                                                                 |
+-----------------------------------------------------------------+
```

12) 8254 Timer Counter Speed Check

The 8254 Timer Counter speed check confirms if the timer is interrupted within the proper interval.

The interrupt processing routine of 8259A is set to the special setting, only the Count "0" output of the timer is placed into the interrupt enable status, and the Count "0" value is checked.

a. Starting with a Count value of 50, it is checked whether an interrupt occurs during 3memoryrefresh intervals. The program displays an error message if no interrupt occurs.

```
+-----------------------------------------------------------------+
|                                                                 |
|    Error code = 104                                             |
|    8254 TIMER COUNTER ERROR                                     |
|                                                                 |
+-----------------------------------------------------------------+
```

b. Starting with a Count value of 250, it is checked whether an interrupt does not occur during 4 memory refresh intervals, then it is checked whether an interrupt occurs during 6 intervals. If an error detected, the program displays an error message identical to that of Item a.

13) 80286 Protect Mode Check

The 80286 protect mode check performs a WRITE/READ check on the 80286 protect mode register as well as a check on the execution status of the instructions during protect mode.

a. The transition into protect mode is checked. The Global Descriptor table and Interrupt Descriptor table are prepared, then execution shifts from real mode to protect mode. At this point, the program displays an error message if the PE bit of the Machine Status Word does not become "1".

```
+-----------------------------------------------------------------+
|                                                                 |
|   Error code = 115                                              |
|   80286 PROTECT MODE ERROR 2                                    |
|                                                                 |
+-----------------------------------------------------------------+
```

b. The interruption of protect mode is checked. The program displays an error message if the interrupt processing routine set at the Interrupt Descriptor table in protect mode is not executed within the prescribed time.
The error message is identical to that of Item a.

c. A WRITE/READ check is performed on LDTR (Local Descriptor table register), and the program displays an error message if the values do not match.
The error message is identical to that of Item a.

d. A WRITE/READ check is performed on TR (Task register), and the program displays an error message if the values do not match.
The error message is identical to that of Item a.

e. A SET/RESET check is performed on DF (Direction flag), and the program displays an error message if the set status and the DF flag of the CPU do not match.
The error message is identical to that of Item a.

f. A boundary check is performed using the BOUND instruction, then the absence of an out-of-boundary interrupt (INT 5) is confirmed by checking the data within boundaries and the occurrence of an out-of-boundary interrupt is confirmed by checking the out-of-boundary data.
The error message is identical to that of Item a.

g. The operation of the PUSHA and POPA instructions is checked. The register values are changed after execution of PUSH A, POPA is executed, then it is checked whether the register values prior to PUSHA execution match the respective register values.
The error message is identical to that of Item a.

h. The operation of the VERR and VERW instructions is checked. The setting of the Writable bit of the access right byte to the Descriptor table is checked using the VERR and VERW instructions, then it is checked whether testing of the reading access right byte and writing access right byte of the segments can be properly performed.
The error message is identical to that of Item a.

i. The operation of the ARPL instruction is checked. Using the ARPL instruction, the operation is checked for the case where the requested privilege level is adjustable and the case where it is not adjustable.
The error message is identical to that of Item a.

j. The operation of the LAR instruction is checked. The access right byte is loaded using the LAR instruction and is checked for being the prescribed value. The program displays an error message if the access right bytecannot be read or if it is not the prescribed value.
The error message is identical to that of Item a.

k. The operation of the LSL instruction is checked. The segment limit is loaded using the LSL instruction and is checked for being the prescribed value. The program displays an error message if the segment limit cannot be read or if it is not the prescribed value.
The error message is identical to that of Item a.

l. A WRITE check is performed on the test data while changing the segment selector. The program displays an error message if the segment selector has not properly changed.

```
+-----------------------------------------------------------------+
|                                                                 |
|   Error code = 114                                              |
|   80286 PROTECT MODE ERROR 1                                    |
|                                                                 |
+-----------------------------------------------------------------+
```

m. The system is returned to real mode by system reset. The stack segment and stack pointer are reset, then this checking operation is terminated.

2. Memory Check

This module performs a WRITE/READ check on the Ramdom Access Memory (RAM) in block units (1 block = 64 KB). The remainder of this section describes the procedures for each checking operation.

1) 64 KB Check of "00000h" - "0FFFFh"

a. The contents of "00000h" - "0FFFFh" are evacuated to "20000h" - "2FFFFh".

b. The test data, "55aah", is written to the entire 64KB area, the I/O check and RAM Parity check are enabled, then a VERIFY check and parity check are performed.
If an error is detected, the program displays following error message:

```
+-----------------------------------------------------------------+
|                                                                 |
|    Error code = 201                                             |
|    xxxxx yyyy zzzzzz ERROR                                      |
|                                                                 |
+-----------------------------------------------------------------+
```

(xxxxx represents the absolute address where the error detected, yyyy represents the error data [any bit that is not "1"], and zzzzzz is either "PARITY" in case of a parity error or "MEMORY" in case ofa VERIFY error.)

c. Using "0aa55h" as the test data, a check identical to that of Item b. is performed.

d. Using "0101h" as the test data, a check identical to that of Item b. is performed.

e. The test data, "5555h" and "0aaaah", is written sequentially to the entire 64 KB area, then a parity check is performed. Next, the test data is read and a VERIFY check is performed. The test data "0000h" is written and a parity check is concurrently performed.

f. The test data "0FFFFh" is written to the leading and trailing words of the 64 KB block and test data "0000h" is written to the other words. Next, the test data is read, then a VERIFY check and parity check are performed.

g. If the check of the 64 KB block is normally terminated, the contents of "20000h" - "2FFFFh" are re-written to "00000h" - "0FFFFh".

h. Next, a message indicating the completion of the first 64 KB block check is displayed on the screen.

```
+-------------------------------------------------------------+
|                                                             |
|    000064 KB OK                                             |
|                                                             |
+-------------------------------------------------------------+
```

2) 64 KB Check of "10000h" - "1FFFFh"

a. The contents of "10000h" - "1FFFFh" are evacuated to "30000h" - "3FFFFh".

b. to f. A RAM check identical to that of Item 1) is performed.

g. If the check of the 64 KB block is normally terminated, the contents of "30000h" - "3FFFFh" are re-written to "10000h" - "1FFFFh".

h. Next, a message indicating the completion of the second 64 KB block check is displayed on the screen.

```
+-------------------------------------------------------------+
|                                                             |
|    000128 KB OK                                             |
|                                                             |
+-------------------------------------------------------------+
```

3) 64 KB Check of "20000h" - "2FFFFh"

a. The contents of "20000h" - "2FFFFh" are evacuated to "30000h" - "3FFFFh".

b. to f. A RAM check identical to that of Item 1) is performed.

g. If the check of the 64 KB block is normally terminated, the contents of "30000h" - "3FFFFh" are re-written to "20000h" - "2FFFFh".

h. Next, a message indicating the completion of the third 64 KB block check is displayed on the screen.

```
+-------------------------------------------------------------+
|                                                             |
|    000192 KB OK                                             |
|                                                             |
+-------------------------------------------------------------+
```

4) 64 KB Block Check of Address "30000h" and Onward

The CMOS settings are read, the highest RAM address is calculated, then a RAM check identical to Item 1) is performed in 64 KB units up to that highest address.

Each time a 64 KB check is completed, the program displays following message.

```
+-------------------------------------------------------------+
|                                                             |
|    XXXXXX KB OK                                             |
|                                                             |
+-------------------------------------------------------------+
```

(The XXXXXX represents the total size of the checked memory block.)

5) Lastly, a parity check is performed by word unit. Each time a 64 KB check is completed, the program displays following message.

```
+-------------------------------------------------------------+
|                                                             |
|    XXXXXX KB OK                                             |
|                                                             |
+-------------------------------------------------------------+
```

(The XXXXXX represents the total size of the checked memory block.)

NOTE: The base memorysize is checkedusing int 12h.The expansion memory size is checked by reading CMOS offset 30h and 31h. In case an expanded memory is installed, the memory check is performed in protect mode of 80286.

3. Keyboard Check

This module checks the operating status of the keyboard as well as the input of each key. The remainder of this section describes the checking procedures.

(In case of test multiple times, only keyboard function check is performed.)

1) Keyboard Function Check

a. The keyboard is read without pressing any keys, and the program displays an error message if the input status is not empty.

```
+------------------------------------------------------------------+
|                                                                  |
|    Error code = 301                                              |
|    8042 ERROR                                                    |
|                                                                  |
+------------------------------------------------------------------+
```

b. The self-test command is output to the keyboard. The program displays an error message if the Normal Termination code is not returned.

```
+------------------------------------------------------------------+
|                                                                  |
|    Error code = 301                                              |
|    8042 ERROR                                                    |
|                                                                  |
+------------------------------------------------------------------+
```

c. The interface test command is output to the keyboard. The program displays an error message if the Normal Termination code is not returned.

```
+------------------------------------------------------------------+
|                                                                  |
|    Error code = 301                                              |
|    KEYBOARD ERROR                                                |
|                                                                  |
+------------------------------------------------------------------+
```

d. The keyboard functions are disabled, then the response from the keyboard is checked. The program displays an error message if the keyboard is in data ON status with the keyboard clock in OFF status. The error message is identical to that of Item c.

e. The keyboard functions are enabled, then the reset command is output to the keyboard. The program displays an error message in case there is no ACK response or in case the resetting generates a BAT Completion code. The error message is identical to that of Item c.

2) Keyboard Lock Check

a. First, determine whether or not to check the keyboard lock.

```
+-----------------------------------------------------------------+
|                                                                 |
|   Do you wish to check the keyboard lock (Y/N)?                 |
|                                                                 |
+-----------------------------------------------------------------+
```

When "Y" is input after the prompt, the keyboard lock check is executed. When "N" is input, the keyboard lock check is not performed.

b. When the keyboard lock check is begun, the following message is displayed, so insert the key into the front panel and turn it to lock the keyboard.

```
+-----------------------------------------------------------------+
|                                                                 |
|   Lock the keyboard using the front-panel key                   |
|                                                                 |
+-----------------------------------------------------------------+
```

The program displays an error message if the keyboard is not locked within the prescribed time.

```
+-----------------------------------------------------------------+
|                                                                 |
|   Error code = 303                                              |
|   KEYBOARD LOCKING ERROR                                        |
|                                                                 |
+-----------------------------------------------------------------+
```

c. When the keyboard becomes locked, the following message is displayed, so turn the front-panel key to unlock the keyboard.

```
+-----------------------------------------------------------------+
|                                                                 |
|   Unlock the keyboard                                           |
|                                                                 |
+-----------------------------------------------------------------+
```

The program displays an error message if the keyboard is not unlocked within the prescribed time. The error message is identical to that of Item b.

3) Keyboard Input Check

First of all, select the keyboard type according to country.

```
+-------------------------------------------------------------+
|                                                             |
|    KEYBOARD SELECT MENU                                     |
|                                                             |
|    1 - US ASCII                                             |
|    2 - United Kingdom                                       |
|    3 - French                                               |
|    4 - German                                               |
|    5 - Italian                                              |
|    6 - Spanish                                              |
|                                                             |
|    0 - Exit                                                 |
|                                                             |
|    Enter selection number:                                  |
|                                                             |
+-------------------------------------------------------------+
```

When the keyboard type is selected, the 0F2h command code is output to the connected keyboard, and the keyboard is judged as being of old type (89 keys) or new type (101 or 102 keys) by its response.

Response	Keyboard Type
only ACK	Old type (89 keys)
ACK, ABh, 41h	New type (101 or 102 keys)

The keyboard layout corresponding to the judged keyboard type is displayed. By pressing an arbitrary key, the character corresponding to the pressed key top will be displayed on the screen.

When "Y" and ENTER is input, the check is normally terminated. If "N" and ENTER is input in the case that the pressed key top and the displayed character are different, the program displays following message:

```
+-------------------------------------------------------------+
|                                                             |
|    KEYBOARD CHECK                                           |
|                                                             |
|    Error code = 302                                         |
|    KEYBOARD IS NON-STANDARD, OR                             |
|    KEYBOARD IS DEFECTIVE.                                   |
|                                                             |
+-------------------------------------------------------------+
```

REMARK: During the keyboard input check, the interrupt vector of keyboard input is rewritten, the scan code of the keyboard is directly read, then the corresponding character is displayed.

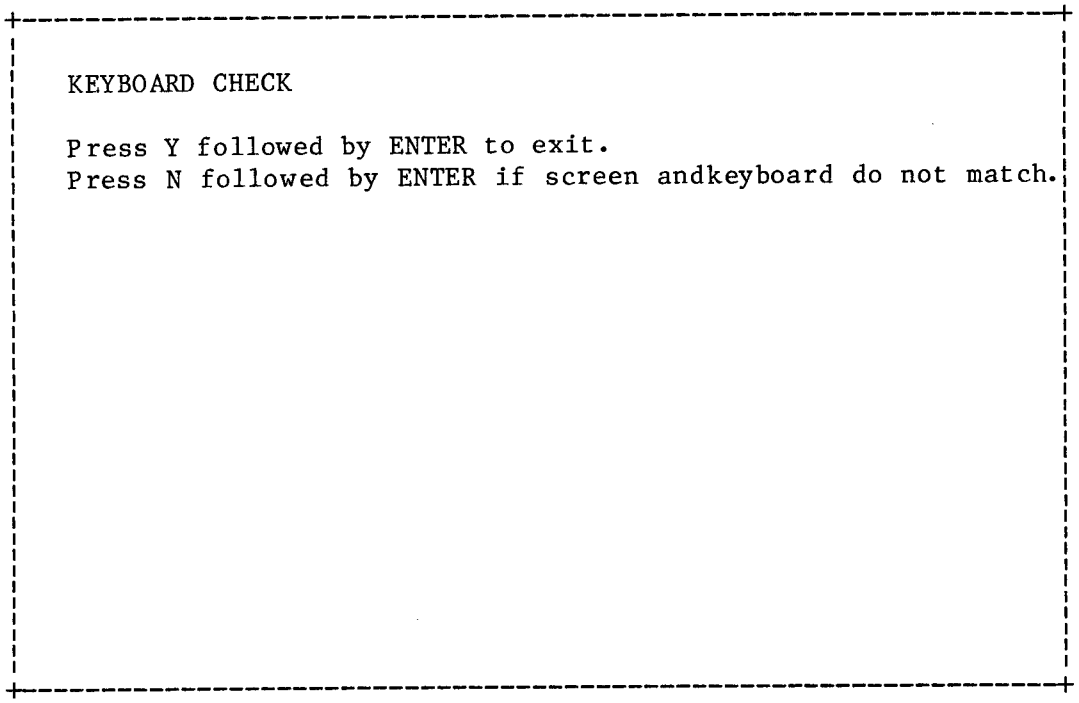
a. Layout of old-type keyboard

```
+-------------------------------------------------------------+
|                                                             |
|   KEYBOARD CHECK                                            |
|                                                             |
|   Press Y followed by ENTER to exit.                        |
|   Press N followed by ENTER if screen andkeyboard do not match.|
|                                                             |
|                                                             |
|                                                             |
|                                                             |
|                                                             |
|                                                             |
|                                                             |
|                                                             |
|                                                             |
|                                                             |
|                                                             |
+-------------------------------------------------------------+
```

b. Layout of new-type (101-key) keyboard

```
+-------------------------------------------------------------+
|                                                             |
|   KEYBOARD CHECK                                            |
|                                                             |
|   Press Y followed by ENTER to exit.                        |
|   Press N followed by ENTER if screen andkeyboard do not match.|
|                                                             |
|                                                             |
|                                                             |
|                                                             |
|                                                             |
|                                                             |
|                                                             |
|                                                             |
|                                                             |
|                                                             |
|                                                             |
+-------------------------------------------------------------+
```

c. Layout of new-type (102-key) keyboard



4. Monochrome Display Adapter and CRT Check

This module checks the monochrome display and its adapter. First, select which check to perform from the menu.

```
+-------------------------------------------------------------+
|                                                             |
|    MONOCHROME ADAPTER AND CRT CHECK MENU                    |
|                                                             |
|    1 - Monochrome adapter check                             |
|    2 - Attribute check                                      |
|    3 - Character set check                                  |
|    4 - Video check                                          |
|    5 - Sync check                                           |
|    6 - Run all above checks                                 |
|                                                             |
|    0 - Exit                                                 |
|                                                             |
|    Enter selection number:                                  |
|                                                             |
+-------------------------------------------------------------+
```

(In case of test multiple times, only the monochrome adapter check is performed.)

The remainder of this section describes each of the checking procedures.

1) Monochrome Adapter Check

When the monochrome adapter check is selected, the program displays following message:

```
+-------------------------------------------------------------+
|                                                             |
|    MONOCHROME ADAPTER CHECK                                 |
|                                                             |
+-------------------------------------------------------------+
```

a. A WRITE/READ check is performed on the VRAM area used for the monochrome display.

i) The Video Enable signal of the monochrome monitor is set to OFF. Next, the test data "00h" is written to and read from the entire VRAM area ("B0000H" - "B0FA0H"), and a comparison check is performed.

If the compared data do not match, the program displays the address generating the mismatch, the written data, and the read data.

```
+-----------------------------------------------------------+
|                                                           |
|   Error code = 401                                        |
|   V-RAM ERROR address   B000H:XXXX                        |
|   write data YY         read data ZZ                      |
|                                                           |
+-----------------------------------------------------------+
```

(XXXX represents the VRAM offset address that generated the mismatch, YY represents the written data, and ZZ represents the read data.)

ii) Next, using the test data "55h", an identical check is performed.

iii) Next, using the test data "0aah", an identical check is performed.

iv) Next, using the test data "0ffh", an identical check is performed.

Lastly, "00h" is written to the entire VRAM area.

b. Black/White mode check of CRT status port
The Video Enable signal of the monochrome monitor is set to ON status, then the program displays following message:

```
+-----------------------------------------------------------+
|                                                           |
|   MONOCHROME ADAPTER CHECK                                |
|                                                           |
+-----------------------------------------------------------+
```

Next, "0ffh" is written to the latter half of the VRAM area ("B07D0H" - "B0FA0H") for the monochrome display, and the CRT status port of 6845 is checked.
A Black/White Video signal that changes to "1" from "0" is normal. The program displays following error message if the Black/White Video signal remains "0" (LOW) or "1" (HIGH):

```
+-----------------------------------------------------------+
|                                                           |
|   Error code = 402                                        |
|   VIDEO SIGNAL ALWAYS LOW                                 |
|                                                           |
+-----------------------------------------------------------+
```

or

```
+-----------------------------------------------------------+
|                                                           |
|   Error code = 402                                        |
|   VIDEO SIGNAL ALWAYS HIGH                                |
|                                                           |
+-----------------------------------------------------------+
```

Lastly, "00h" is written to the latter half ("B07D0H" - "B0FA0H") of the VRAM area and this check is terminated.

2) Attribute Check

When the attribute check is selected, the various types of attributes that can be displayed are shown on the monochrome display using characters.

```
+-----------------------------------------------------------------+
|                                                                 |
|    ATTRIBUTE CHECK                                              |
|                                                                 |
|    NORMAL INTENSITY                                             |
|    HIGH INTENSITY                                               |
|    BLINKING                                                     |
|    REVERSE                                                      |
|    UNDERLINED                                                   |
|                                                                 |
|    Is the display correct (Y/N)?                                |
|                                                                 |
+-----------------------------------------------------------------+
```

Confirm whether each attribute is accurately displayed, then input the answer.

If "N" is input, the program displays an error message.

```
+-----------------------------------------------------------------+
|                                                                 |
|    Error code = 403                                             |
|    ATTRIBUTE ERROR                                              |
|                                                                 |
+-----------------------------------------------------------------+
```

3) Character Set Check

When the character set check is selected, the entire character set from "00h" to "0ffh" is displayed on the screen.

Confirm whether the character set is accurately displayed, then input the answer.

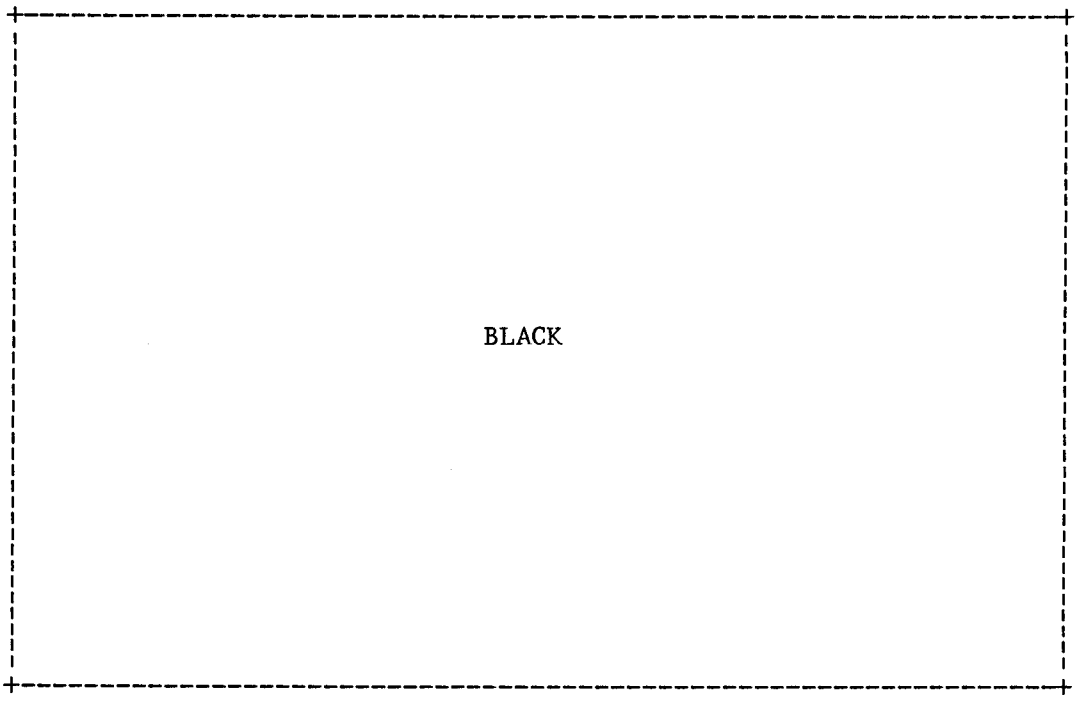
```
+-------------------------------------------------------------+
|                                                             |
|    CHARACTER SET CHECK                                      |
|                                                             |
|                                                             |
|                                                             |
|                                                             |
|                                                             |
|                    ( All character set )                    |
|                                                             |
|                                                             |
|                                                             |
|                                                             |
|    Is the display correct (Y/N)?                            |
|                                                             |
+-------------------------------------------------------------+
```

If "N" is input, an error message is displayed.

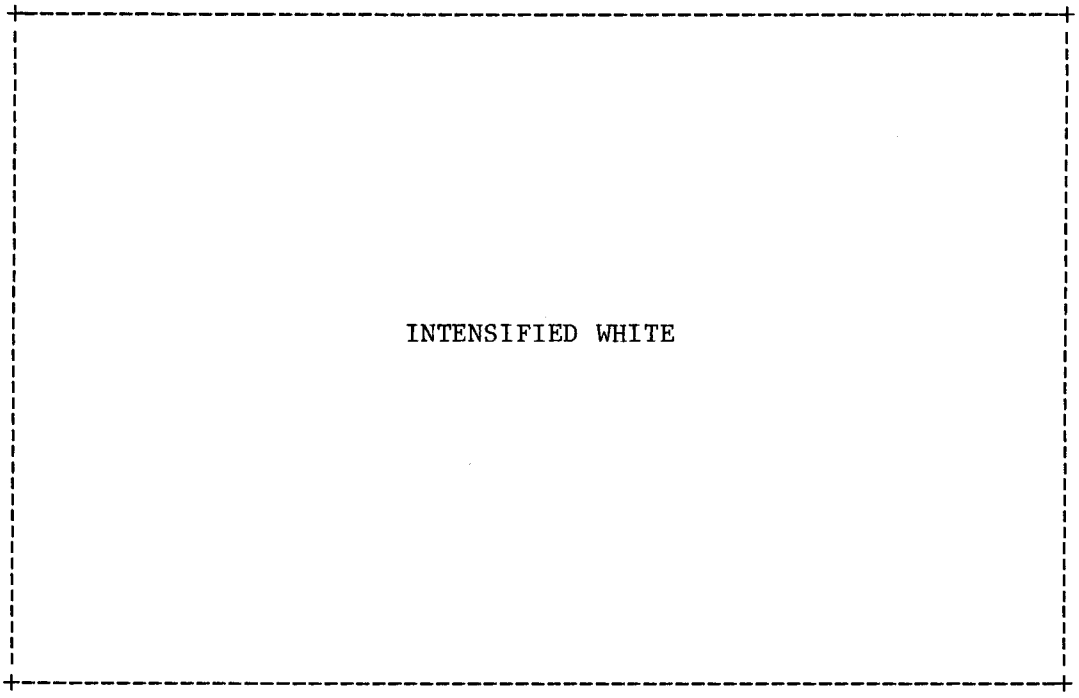
```
+-------------------------------------------------------------+
|                                                             |
|    Error code = 404                                         |
|    CHARACTER SET ERROR                                      |
|                                                             |
+-------------------------------------------------------------+
```

4) Video Check

When the video check is selected, the following screen is initially displayed with a high-intensity foreground color and a black background color:



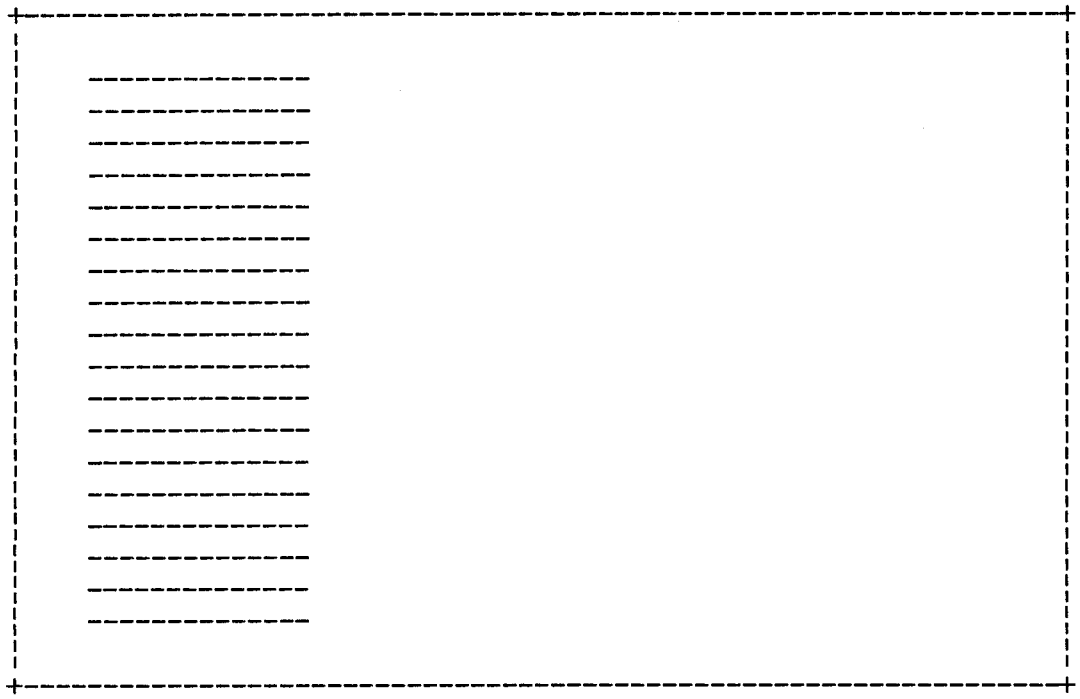
When any key is pressed, the following screen is displayed with a black foreground color and a high-intensity background color:



Pressing any key terminates this operation.

5) Sync Check

When the sync check is selected, the following screen is displayed. Check this screen for any discrepancies in the synchronization of all lines.



6) Run All Above Checks

When "Run all above checks" is selected, the checks described in Items 1) to 5) are consecutively executed.

5. Color Graphics Adapter and CRT Check

This module checks the color display and its adapter. First, select which check to perform from the menu.

```
+-------------------------------------------------------------+
|                                                             |
|    COLOR GRAPHICS ADAPTER AND CRT CHECK MENU                |
|                                                             |
|     1 - Color graphics adapter check                        |
|     2 - Attribute check                                     |
|     3 - Character set check                                 |
|     4 - 40-column character set check                       |
|     5 - 320X200 graphics mode check                         |
|     6 - 640X200 graphics mode check                         |
|     7 - Screen paging check                                 |
|     8 - Light pen check                                     |
|     9 - Color video check                                   |
|    10 - Sync check                                          |
|    11 - Run all above checks                                |
|                                                             |
|     0 - Exit                                                |
|                                                             |
|    Enter selection number:                                  |
|                                                             |
+-------------------------------------------------------------+
```

(In case of test multiple times, only the color graphics adapter check is performed.)

The remainder of this section describes each of the checking procedures.

1) Color Graphics Adapter Check

When the color graphics adapter check is selected, the program displays following message:

```
+-------------------------------------------------------------+
|                                                             |
|    COLOR ADAPTER CHECK                                      |
|                                                             |
+-------------------------------------------------------------+
```

At this point, a WRITE/READ check is performed on the VRAM area used for color graphics.

a. The Video Enable signal of color graphics is set to OFF. Next, the test data "00h" is written to and read from the entire VRAM area ("B8000H" - "B9F3FH" and "BA000H" - "BBF3FH") used for color graphics, and a comparison check is performed. If the compared data does not match, the program displays the address generating the mismatch, the written data, and read

data.

```
+-----------------------------------------------------------------+
|                                                                 |
|    Error code = 501                                             |
|    V-RAM ERROR address  B800H:XXXX                              |
|    write data YY        read data ZZ                            |
|                                                                 |
+-----------------------------------------------------------------+
```

(XXXX represents the address generating the mismatch, YY represents the written data, and ZZ represents the read data.)

b. Next, using the test data "55h", an identical check is performed.

c. Next, using the test data "0aah", an identical check is performed.

d. Next, using the test data "0ffh", an identical check is performed.

Lastly, "00h" is written to the entire VRAM area, the Video Enable signal is set to ON, and this check is terminated.

2) Attribute Check

When the attribute check is selected, the various types of attributes that can be displayed using color graphics are shown using characters. (40 x 25 character mode)

```
+-----------------------------------------------------------------+
|                                                                 |
|    ATTRIBUTE CHECK                                              |
|                                                                 |
|    NORMAL INTENSITY                                             |
|    BLINKING                                                     |
|    BLACK                                                        |
|    BLUE                                                         |
|    GREEN                                                        |
|    CYAN                                                         |
|    RED                                                          |
|    MAGENTA                                                      |
|    BROWN                                                        |
|    WHITE                                                        |
|    GRAY                                                         |
|    LIGHT BLUE                                                   |
|    LIGHT GREEN                                                  |
|    LIGHT CYAN                                                   |
|    LIGHT RED                                                    |
|    LIGHT MAGENTA                                                |
|    YELLOW                                                       |
|    WHITE  (High intensity)                                      |
|                                                                 |
|    Is the display correct (Y/N)?                                |
|                                                                 |
+-----------------------------------------------------------------+
```

Confirm whether each attribute is accurately displayed, then input the result. (The display has returned to the 80 x 25 character mode.)

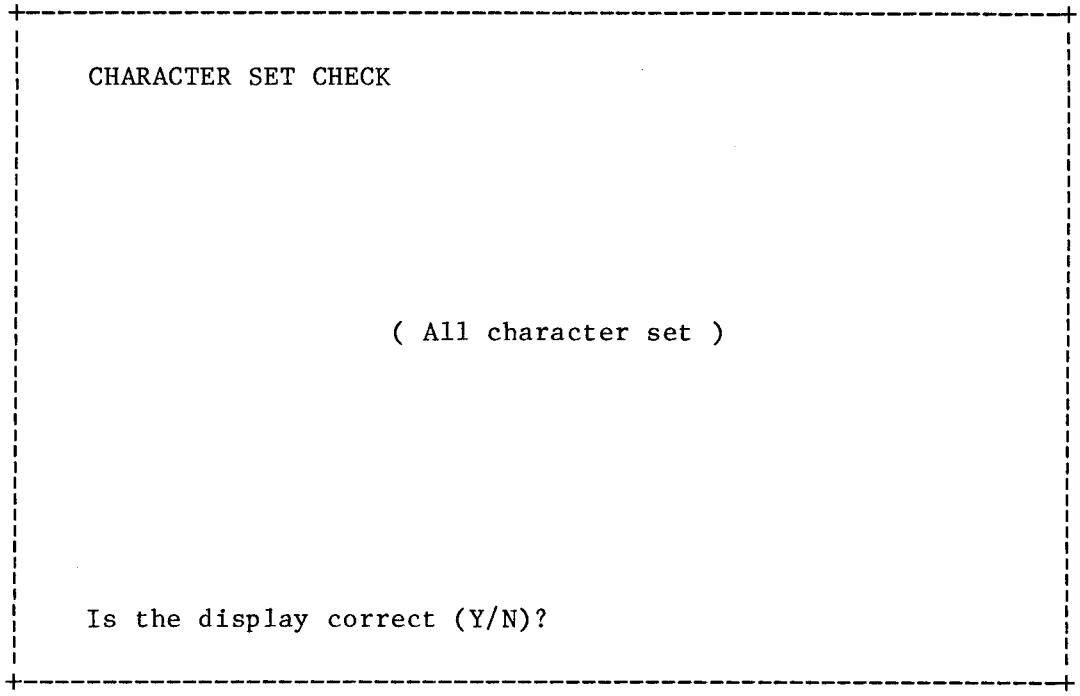
If "N" is input, the program displays an error message.

```
+-----------------------------------------------------------------+
|                                                                 |
|    Error code = 503                                             |
|    ATTRIBUTE ERROR                                              |
|                                                                 |
+-----------------------------------------------------------------+
```

3) Character Set Check

When the character set check is selected, the entire character set from "00h" to "0ffh" is displayed on the screen.

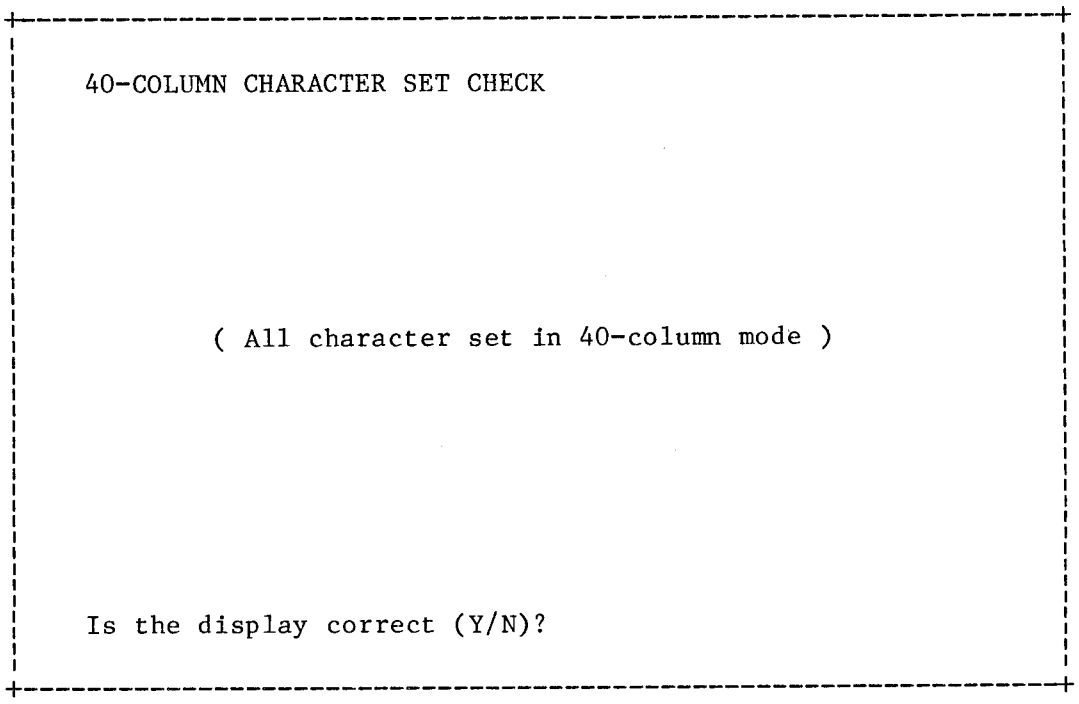
Confirm whether the character set is accurately displayed, then input the answer.



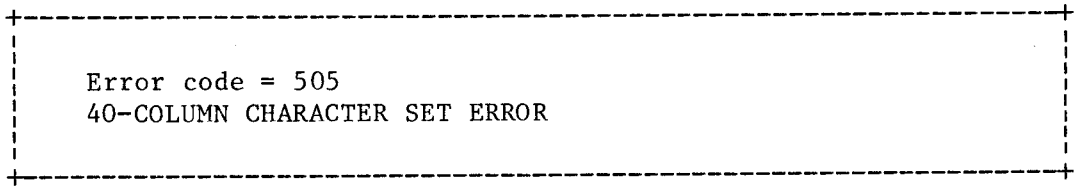
If "N" is input, the program displays an error message.

4) 40-Column Character Set Check

When the 40-column character set check is selected, the entire character set from "00h" to "0ffh" is displayed on the screen in 40-column mode.

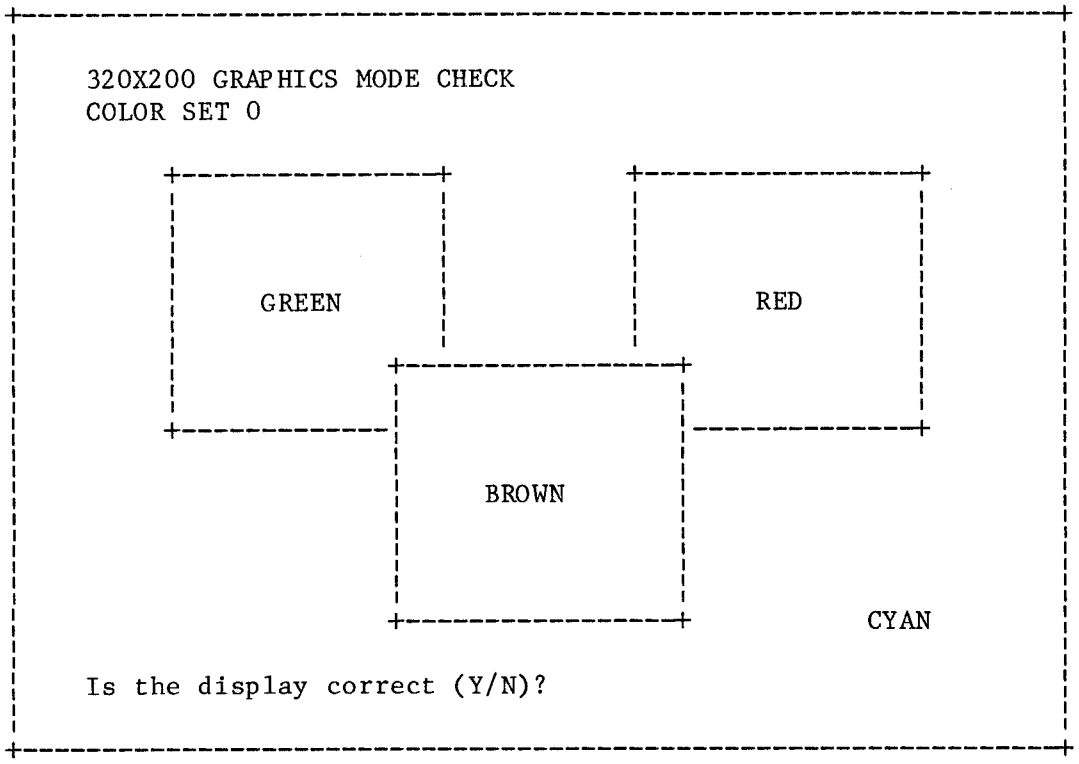


If "N" is input, the program displays an error message.

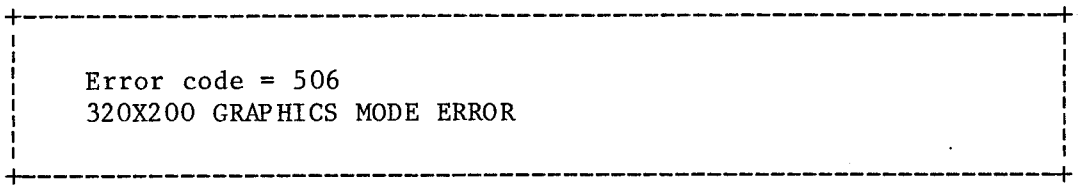


5) 320 x 200 Graphics Mode Check

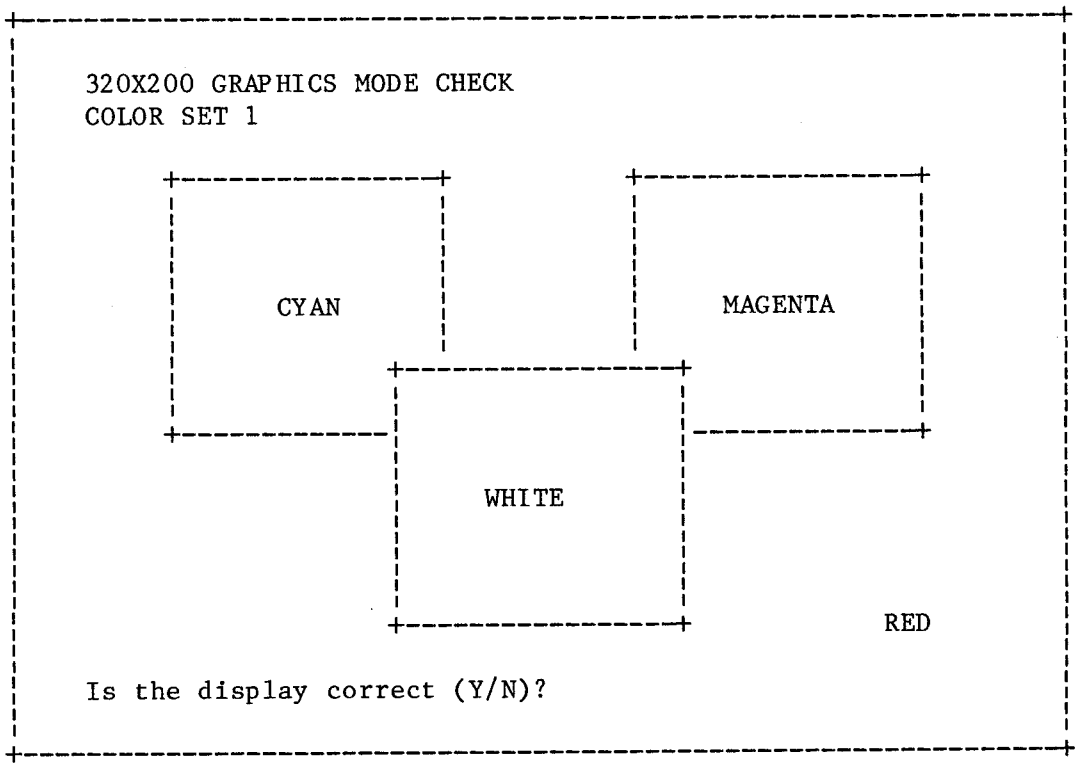
When the 320 x 200 graphics mode check is selected, the following image pattern is displayed on the screen.This screen has been created by writing directly to VRAM. (Color setting = "0")



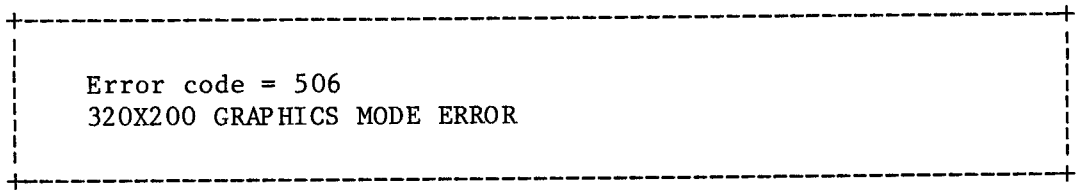
Confirm whether the pattern is accurately displayed, then input the answer.
If "N" is input, the program displays an error message.



Next, change the color setting to "1" to display the same image pattern on the screen.

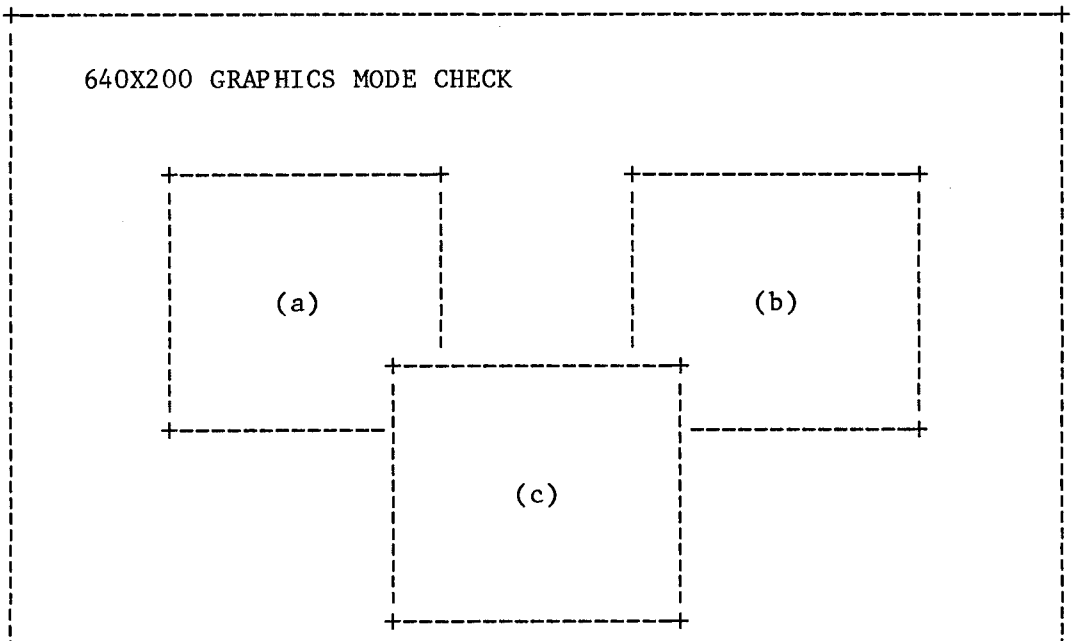


Confirm whether the pattern is accurately displayed, then input the answer.
If "N" is input, the program displays an error message.



6) 640 x 200 Graphics Mode Check

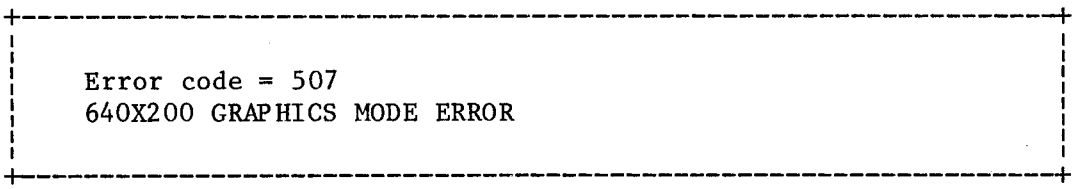
When the 640 x 200 graphics mode check is selected, the following image pattern is displayed on the screen. This screen has been created by writing directly to VRAM. (High-resolution mode)



(a) Coarse stripes (b) Fine stripes (c) Completely filled

Confirm whether the pattern is accurately displayed, then input the answer.

If "N" is input, the program displays an error message.



7) Screen Page Check

When the screen page check is selected, the characters "0" - "7" are respectively written to Pages 0 - 7, then the screen paging according to the changing of pages is checked.

```
SCREEN PAGING CHECK

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXX                XXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXX                XXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXX      (a)       XXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXX                XXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXX                XXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

Press any key for next page
```

(a) The numeral corresponding to each page no. is displayed.

After completing the check up to Page 7, confirm whether the screen paging was accurately displayed, then input the answer.

```
SCREEN PAGING CHECK

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXX                XXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXX                XXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXX      (a)       XXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXX                XXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXX                XXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

Is the display correct (Y/N)?
```

If "N" is input, the program displays an error message.

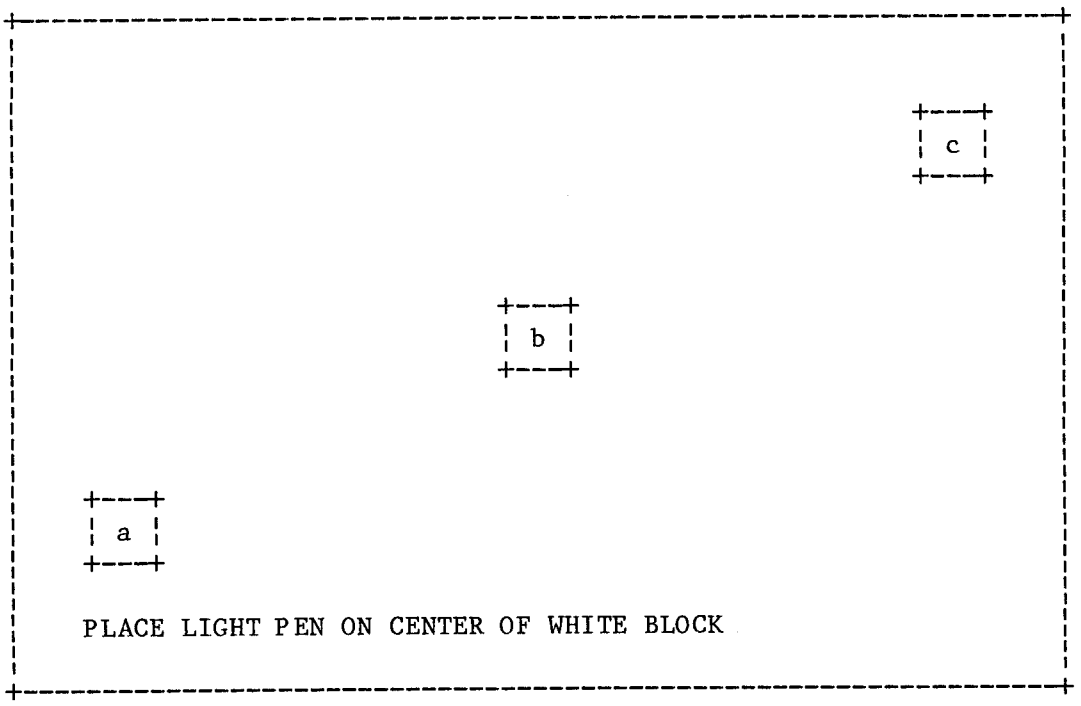
```
+-------------------------------------------------------------+
|                                                             |
|    Error code = 508                                         |
|    SCREEN PAGING ERROR                                      |
|                                                             |
+-------------------------------------------------------------+
```

8) Light Pen Check

When the light pen check is selected, you must next specify whether or not to actually perform the check.

```
+-------------------------------------------------------------+
|                                                             |
|    LIGHT PEN CHECK                                          |
|    Enter Y to start light pen check.                        |
|    Enter N to return to the menu.                           |
|                                                             |
+-------------------------------------------------------------+
```

Next, a white block is displayed on the the screen, so press the light pen on the center of each block. The address that is read from light pen is checked.



Check the three blocks in the order of a - b - c.

The program displays an error message if the position where the block is displayed and the light pen position do not match.

```
+-----------------------------------------------------------------+
|                                                                 |
|    Error code = 509                                             |
|    LIGHT PEN ERROR                                              |
|                                                                 |
+-----------------------------------------------------------------+
```

9) Color Video Check

When the color video check is selected, the display of the background color is changed in the sequence below:

1. Black
2. Blue
3. Green
4. Cyan
5. Red
6. Magenta
7. Brown
8. White
9. Gray
10. Light blue
11. Light green
12. Light cyan
13. Light red
14. Light magenta
15. Yellow
16. White (high intensity)

After all of the background colors are displayed, confirm whether they have been accurately displayed then input the answer.

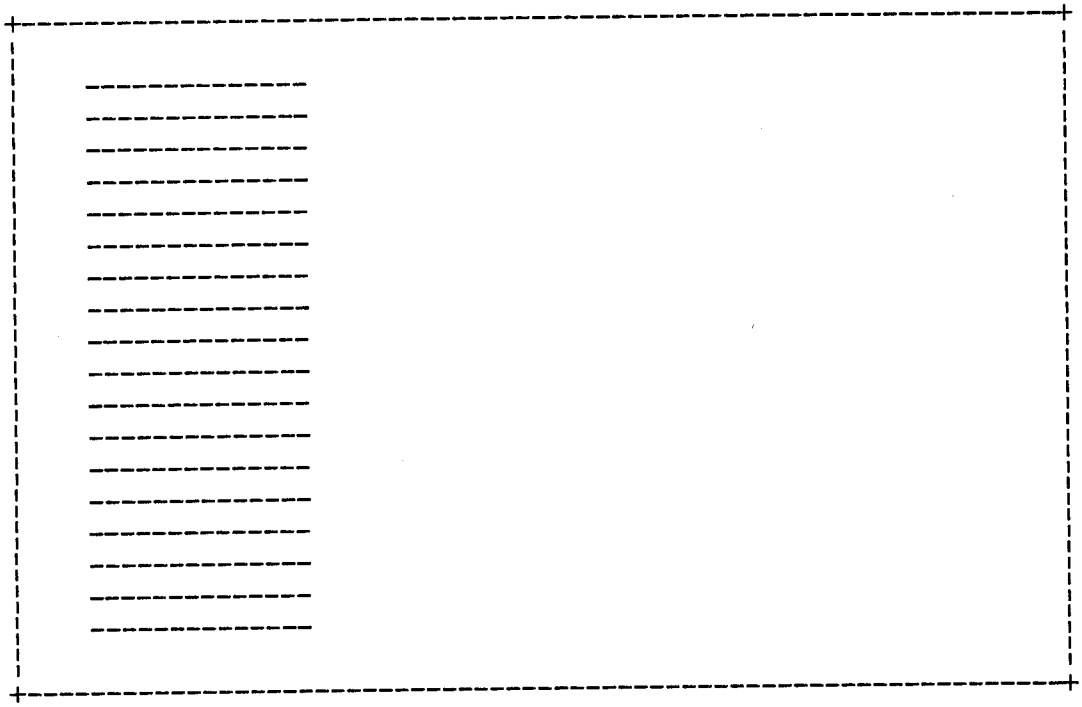
```
+-----------------------------------------------------------------+
|                                                                 |
|    Is the display correct (Y/N)?                                |
|                                                                 |
+-----------------------------------------------------------------+
```

If "N" is input, the program displays an error message.

```
+-----------------------------------------------------------------+
|                                                                 |
|    Error code = 510                                             |
|    COLOR VIDEO ERROR                                            |
|                                                                 |
+-----------------------------------------------------------------+
```

10) Sync Check

When the sync check is selected, the following screen is displayed. Check this screen for any discrepancies in the synchronization of all lines.



11) Run All Above Checks

When "Run all above checks" is selected, the checks described in Items 1) to 10) are consecutively executed.

6. Floppy Disk Drives and Controller Check

This module checks the floppy disks and floppy disk drives. First, select which check to perform from the menu.

```
+-------------------------------------------------------------+
|                                                             |
|    FLOPPY DISK DRIVE(S) AND CONTROLLER CHECK MENU           |
|                                                             |
|    1 - Sequential seek check                                |
|    2 - Random seek check                                    |
|    3 - Write, read check                                    |
|    4 - Speed check                                          |
|    5 - Disk change check                                    |
|    6 - Run all above checks                                 |
|                                                             |
|    0 - Exit                                                 |
|                                                             |
|    Enter selection number:                                  |
|                                                             |
+-------------------------------------------------------------+
```

(In case of test multiple times, the following checks are consecutively performed.)

```
+-------------------------------------------------------------+
|                                                             |
|    1 - Sequencial seek check                                |
|    2 - Random seek check                                    |
|    3 - Write, read check                                    |
|                                                             |
+-------------------------------------------------------------+
```

The remainder of this section describes each of the checking procedures.

1) Sequential Seek Check

Initially, the number of floppy disk drives installedis checked by using Equipment Determination (int 11h). The program displays following message if two drives are installed, so input the name of the drive to be checked:

```
+-------------------------------------------------------------+
|                                                             |
|    Check which drive (A/B)?                                 |
|                                                             |
+-------------------------------------------------------------+
```

The sequential seek check sequentially searches from the cylinder position of the innermost periphery to that of the outermost periphery for the head, then checks the seek operation. This check is performed with respect to Head "0" and "1".

```
SEQUENTIAL SEEK CHECK

Current track is xxxx
```

(The xxxx represents the number of the sought cylinder.)

The program displays an error message if the Floppy Disk Controller (FDC) assumes one of the following statuses:

1. The FDC main status remains BUSY.
2. The FDC is not in Output Ready status when the program going to output a command.
3. The FDC is not in Input Ready status when the program going to input status.

```
FLOPPY DISK DRIVE(S) AND CONTROLLER CHECK
Error code = 601
FLOPPY DISK CONTROLLER ERROR
```

The program displays an error message also when the seek operation of the FDC after performing head seek is not normally terminated.

```
FLOPPY DISK DRIVE(S) AND CONTROLLER CHECK
Error code = 602
SEQUENTIAL SEEK ERROR
TRACK -- xx
SIDE ---  y
```

(xx represents the error cylinder number and y representsthe error head number.)

2) Random Seek Check

The random seek checking procedure is identical to that of Item 1), except for the procedure that the seek operation is performed in randominstead of sequentially.

The messages are also identical except that "SEQUENTIAL SEEK" is replaced by "RANDOM SEEK". (Error code = 603)

3) WRITE/READ Check

The drive is selected as in Item 1). When a drive is selected, precautions pertaining to the start of the check operation are displayed.

```
+-------------------------------------------------------------+
|                                                             |
|    Use only a formatted blank diskette for this test.       |
|    Any data present may be erased.                          |
|                                                             |
|    If using drive A, remove your Diagnostic Disk.           |
|                                                             |
|    Enter Y to start this check.                             |
|    Enter N to return to the menu.                           |
|                                                             |
+-------------------------------------------------------------+
```

The WRITE/READ check is performed by writing and reading Head Nos. "0" and "1", alternately, to and from for all sectors of each cylinder, from the innermost cylinder to the outermost cylinder [0].
The check data is "6db6h".

```
+-------------------------------------------------------------+
|                                                             |
|    WRITE, READ CHECK                                        |
|                                                             |
|    Current track is xx                                      |
|                                                             |
+-------------------------------------------------------------+
```

(The xx represents the number of the checked cylinder.)

If an error is detected during the writing or reading of data, the program displays following message:

```
+-------------------------------------------------------------+
|                                                             |
|    FLOPPY DISK DRIVE(S) AND CONTROLLER CHECK                |
|    Error code = 604                                         |
|                                                             |
|    WRITE ERROR                                              |
|    TRACK -- xx                                              |
|    SECTOR -  y                                              |
|    SIDE ---  z                                              |
|                                                             |
+-------------------------------------------------------------+
```

(xx represents the error cylinder number, y represents the error sector number, and z represents the error head number.)

```
+-------------------------------------------------------------+
|                                                             |
|    FLOPPY DISK DRIVE(S) AND CONTROLLER CHECK                |
|    Error code = 605                                         |
|                                                             |
|    READ ERROR                                               |
|    TRACK -- xx                                              |
|    SECTOR -  y                                              |
|    SIDE ---  z                                              |
|                                                             |
+-------------------------------------------------------------+
```

(xx represents the error cylinder number, y represents the error sector number, and z represents the error head number.)

4) Speed Check

The drive is selected as in Item 1). The speed check performs 60 times one-sector reading operationsof Sector 1 of Cylinder No.32, Head No. 0, and the program measuresthe time for this operation using the Channel 0 of 8254.

Measurement is performed by counting the 8254 interrupt, which occurs every 1/18 second, and correcting by adding the number of the final Timer Count value. Finally the program displays the revolution speed in rpm (revolution per minutes).

expression:

(60 [times])/(interrupt count)*(18 [sec/times])*(60 [sec])

```
+-------------------------------------------------------------+
|                                                             |
|    The disk rotation speed should be more than xxx.x rpm and|
|                                          less than yyy.y rpm|
|                                                             |
|    The disk rotation speed is now zzz.z rpm                 |
|                                                             |
|                                                             |
|    Press any key to return to the menu                      |
|                                                             |
+-------------------------------------------------------------+
```

(xxx.x represents the lower-limit revolution value, yyy.y represents the upper-limit revolution value, and zzz.z represents the current revolution value.)

The lower-limit revolution value is 294.0 for 360 KB drive and 720 KB (3.5"), 352.8 for 1.2 MB. (Normal revolution value - 2%.) And the upper-limit revolution value is 306.0 for 360 KB drive and 720 KB (3.5"), 367.2 for 1.2 MB. (Normal revolution value + 2%.)

If a floppy disk is not installed or a read error is detected, the program displays following message:

```
+-------------------------------------------------------------+
|                                                             |
|    Disk is defective or not installed properly.             |
|    Press ENTER to return to the menu.                       |
|                                                             |
+-------------------------------------------------------------+
```

5) Disk Change Check

The drive selection is identical to that of Item 1). The disk change check can only be performed for 1.2 MB and 720 KB drives. The program performs read DASD type command of int 13h to confirm whether the specified drive is change line available or not.

If the drive is no change line available, the program displays following message, allowing you to return to the menu.

```
+-------------------------------------------------------------+
|                                                             |
|    Drive X is no change line available.                     |
|    DISK CHANGE is not allowed with this drive.              |
|                                                             |
|    Press ENTER to return to the menu.                       |
|                                                             |
+-------------------------------------------------------------+
```

(The X represents the drive name of the specified floppy disk.)

If the drive is change line available, the program displays following message, then remove the disk from the drive:

```
+-------------------------------------------------------------+
|                                                             |
|    Remove the disk from drive X.                            |
|                                                             |
+-------------------------------------------------------------+
```

(The X represents the drive name of the specified floppy disk.)

If the floppy disk is not removed within the prescribed time, the program displays following error message:

```
+-------------------------------------------------------------+
|                                                             |
|    Error code = 606                                         |
|    DISK CHANGE CHECK                                        |
|    REMOVE ERROR                                             |
|                                                             |
+-------------------------------------------------------------+
```

When the floppy disk is removed, the program displays following message, then re-insert the disk into the drive:

```
+-------------------------------------------------------------+
|                                                             |
|    Re-insert the disk into drive X.                         |
|                                                             |
+-------------------------------------------------------------+
```

(The X represents the drive name of the specified floppy disk.)

If the floppy disk is not re-inserted within the prescribed time, the program displays following error message:

```
+-------------------------------------------------------------+
|                                                             |
|    Error code = 607                                         |
|    DISK CHANGE CHECK                                        |
|    INSERT ERROR                                             |
|                                                             |
+-------------------------------------------------------------+
```

REMARKS: The disk change check reads the Digital Input Register of the FDC, then checks the disk change flag of Bit 7.

6) Run All Above Checks

When "Run all above checks" is selected, the checks described in Items 1) through 5) are consecutively executed.

7. Math Coprocessor Check (80287)

This module checks the mathematic coprocessor (80287). When this module is called, the following message is displayed:

```
+-----------------------------------------------------------+
|                                                           |
|    80287 COPROCESSOR TEST                                 |
|                                                           |
+-----------------------------------------------------------+
```

1) Coprocessor Installation Check

a. CMOS RAM Setting Check
First, Equipment Determination of int 11h is called to check whether or not the coprocessor is installed.
If the the coprocessor not installed, the program displays following error message:

```
+-----------------------------------------------------------+
|                                                           |
|    Error code = 701                                       |
|    COPROCESSOR NOT INSTALLED                              |
|                                                           |
+-----------------------------------------------------------+
```

b. Check by Initialization
The Initialize instruction (finit) is output to the coprocessor, then the status word of the coprocessor is read (fstsw) to check the installation status.
If all error bits are not read as "0", the program displays following error message:

```
+-----------------------------------------------------------+
|                                                           |
|    Error code = 701                                       |
|    COPROCESSOR NOT INSTALLED                              |
|                                                           |
+-----------------------------------------------------------+
```

2) Initialization Check of Coprocessor

The Initialize instruction (finit) is output to the coprocessor, then the status word of the coprocessor is read (fstsw) to check the initialization status.

If the all error bits are not read as "0" with BUSY = "0" and ST = "0", the program displays following error message:

```
+-----------------------------------------------------------------+
|                                                                 |
|    Error code = 702                                             |
|    COPROCESSOR INITIALIZE ERROR                                 |
|                                                                 |
+-----------------------------------------------------------------+
```

3) Invalid Operation Mask Check (1)

All exceptional interrupts of the coprocessor are masked, then operation is performed with an empty register to generate a stack underflow.

At this time, if the IR (Interrupt Request) bit of the status word of the coprocessor is "1", the program displays following error message:

```
+-----------------------------------------------------------------+
|                                                                 |
|    Error code = 703                                             |
|    COPROCESSOR INVALID OPERATION MASK ERROR                     |
|                                                                 |
+-----------------------------------------------------------------+
```

4) Invalid Operation Mask Check after Clearing of Exceptional Bits

All exceptional bits are cleared (fclex), then processing identical to that of Item 3) is performed.

At this time, if the IR bit of the status word of the coprocessor is "1", the program displays following error message:

```
+-----------------------------------------------------------------+
|                                                                 |
|    Error code = 703                                             |
|    COPROCESSOR INVALID OPERATION MASK ERROR                     |
|                                                                 |
+-----------------------------------------------------------------+
```

5) ST Field Check

Two items of integer data are loaded (fild) and added (fadd).

At this time, if the ST field value of the status word of the coprocessor is "6", the program displays following error message:

```
+-----------------------------------------------------------------+
|                                                                 |
|    Error code = 704                                             |
|    COPROCESSOR ST FIELD ERROR                                   |
|                                                                 |
+-----------------------------------------------------------------+
```

6) Exceptional Data Comparison Check (1)

The data from the stack underflow status of Item 3) is compared with"1"(fcom),iftheydo notmatch,theprogramdisplays following error message:

```
+-------------------------------------------------------------+
|                                                             |
|    Error code = 705                                         |
|    COPROCESSOR COMPARISON ERROR                             |
|                                                             |
+-------------------------------------------------------------+
```

7) Zero Division Mask Check

All exceptional interrupts of the coprocessor are masked, then "1" is divided by "0" to generate a zero divide exception.

At this time, if the IR (Interrupt Request) bit of the status word of the coprocessor is "1", the program displays following error message:

```
+-------------------------------------------------------------+
|                                                             |
|    Error code = 706                                         |
|    COPROCESSOR ZERO DIVIDE MASK ERROR                       |
|                                                             |
+-------------------------------------------------------------+
```

8) Exceptional Data Addition Check

The data items from Item 7) that resulted in zero division are added together.

At this time, if the IR (Interrupt Request) bit of the status word of the coprocessor is "1", the program displays following error message:

```
+-------------------------------------------------------------+
|                                                             |
|    Error code = 707                                         |
|    COPROCESSOR ADDITION ERROR                               |
|                                                             |
+-------------------------------------------------------------+
```

9) Exceptional Data Subtraction Check

The data items from Item 7) that resulted in zero division are subtracted from each other.

At this time, if the IR (Interrupt Request) bit of the status word of the coprocessor is "1", the program displays following error message:

```
+-------------------------------------------------------------+
|                                                             |
|    Error code = 708                                         |
|    COPROCESSOR SUBTRACTION ERROR                            |
|                                                             |
+-------------------------------------------------------------+
```

10) Exceptional Data Multiplication Check

The data from Item 7) that resulted in zero division is multiplied by "0".

At this time, if the IR (Interrupt Request) bit of the status word of the coprocessor is "1", the program displays following error message:

```
+-------------------------------------------------------------+
|                                                             |
|    Error code = 709                                         |
|    COPROCESSOR MULTIPLICATION ERROR                         |
|                                                             |
+-------------------------------------------------------------+
```

11) Invalid Operation Mask Check (2)

All exceptional interrupts of the coprocessor are masked, then "0" is divided by "0" to generate an invalid operation exception.

At this time, if the IR (Interrupt Request) bit of the status word of the coprocessor is "1", the program displays following error message:

```
+-------------------------------------------------------------+
|                                                             |
|    Error code = 703                                         |
|    COPROCESSOR INVALID OPERATION MASK ERROR                 |
|                                                             |
+-------------------------------------------------------------+
```

12) Exceptional Data Comparison Check (2)

The data from Item 7) that resulted in zero division is compared with "0" (fcom), and the program displays an error message if they do not match:

```
+-------------------------------------------------------------+
|                                                             |
|    Error code = 705                                         |
|    COPROCESSOR COMPARISON ERROR                             |
|                                                             |
+-------------------------------------------------------------+
```

13) Mathematic Function Check

Addition, subtraction, multiplication, division, and the square root operation are performed, then the precision is checked.

The program displays an error message if the mathematic result is incorrect.

```
+-----------------------------------------------------------------+
|                                                                 |
|    Error code = 710                                             |
|    COPROCESSOR PRECISION ERROR                                  |
|                                                                 |
+-----------------------------------------------------------------+
```

9. Parallel Port (Printer Interface) Check

This module performs a loop-back check on the parallel port (printer interface).

Before starting this check, attach the loop-back connector to the parallel port. The pin connection of the loop-back connection shoud be as follows:

Signal Name	PIN Number		PIN Number	Signal Name
Strobe	1	<----->	13	Select
Data Bit 0	2	<----->	15	Error
Auto Feed	14	<----->	12	P.END (out of paper)
Init. Printer	16	<----->	10	Acknowledge
Select Input	17	<----->	11	Busy
(Output signal)				(Input signal)

After attaching the loop-back connector to the parallel port, issue the instruction to start the check.

```
PARALLEL PORT CHECK
Attach loop-back connector to parallel port.
Enter Y to start this check when connector is attached, or
Enter N to return to the menu.
```

The procedures for checking the parallel port are as follows:

1) WRITE/READ Check of Data Output Port

a. The test data "0aah" is output to the data output port (378), then compared with the input from the same port. The configuration of the data output port is as follows:

Bit no.	PIN no.	Signal Name
0	2	Data Bit 0
1	3	" 1
2	4	" 2
3	5	" 3
4	6	" 4
5	7	" 5
6	8	" 6
7	9	" 7

If an unmatching bit is detected after performing the comparison, the corresponding pin number is displayed in an error message.

```
+-------------------------------------------------------------+
|                                                             |
|   PARALLEL PORT CHECK                                       |
|   Error code = 901                                          |
|   ERROR PIN xx                                              |
|                                                             |
+-------------------------------------------------------------+
```

(The xx represents the pin number corresponding to the unmatching bit.)

b. Next, using the test data "55h", an identical check is performed.

2) WRITE/READ Check of Control Port

a. The test data "0ah" is output to the control port (37A), then compared with the input from the same port. The configuration of the control port is as follows:

Bit no.	PIN no.	Signal Name
0	1	Strobe
1	14	Auto Feed
2	16	Ietialize Printer
3	17	Select Input
4	IRQ Enable	
5	not use	
6	not use	
7	not use	

If an unmatching bit is detected after performing the comparison, the corresponding pin number is displayed in an error message. The error message is identical to that of Item 1).

b. Next, using the test data "05h", an identical check is performed.

3) Loop-back Check of Control Signal

a. The test data "0ah" is output to the control port (37A) and the test data "01h" is output to the data output port (378). Next, input from the status port (379); the result is OK if Bits 7, 4, and 3 are "1" and Bits 6 and 5 are "0". The configuration of the status port is as follows:

Bit no.	PIN no.	Signal Name
0	not use	
1	not use	
2	not use	
3	15	Error
4	13	Select
5	12	P.END (out of paper)
6	10	Acknowledge
7	11	Busy

If an error is detected, the error message that identical to that of Item 1) is displayed.

b. The test data "05h" is output to the control port (37A) and the test data "00h" is output to the data output port (378). Next, input from the status port (379); the result is OK if Bits 7, 4, and 3 are "0" and Bits 6 and 5 are "1".
If an error is detected, the error message that identical to that of Item 1) is diaplayed.

c. Test data is output to the control port and data output port so that each signal of the status port goes ON, then the results are checked.
If an error is detected, the error message that identical to that of Item 1) is displayed.

11. Serial Port (RS-232C) Check

This module performs a loop-back check of the serial port (RS-232C port).

Before starting this check, attach the loop-back connector to the serial port.

The pin connection of the 9 pins loop-back connector is as follows:

Signal Name	PIN Number	PIN Number	Signal Name
Transmit Data	3 <------>	2	Receive Data
Request To Send	7 <------>	8	Clear To Send
Data Terminal Ready	4 <------>	6	Data Set Ready
(Output Signal)			(Input Signal)

After attaching the loop-back connector to the serial port, issue the instruction to start this check.

```
SERIAL PORT CHECK
Attach loop-back connector to serial port.
Enter Y to start this check when connector is attached, or
Enter N to return to the menu.
```

The procedures for checking the serial port are as follows:

1) Input/Output Check of MODEL Control Signal

a. Data Terminal Ready (DTR) = 0 and Request to Send (RTS) = 0 are output, then the Data Set Ready (DSR) and Clear to Send (CTS) signals are input.
The results are OK if both DSR and CTS equal "0". An error message is displayed if either signal equals "1".

When DSR = 1:

```
Error code = 1101
ERROR DTR DSR, DSR ALWAYS HIGH
```

When CTS = 1:

```
+-----------------------------------------------------------------+
|                                                                 |
|    Error code = 1101                                            |
|    ERROR RTS CTS, CTS ALWAYS HIGH                               |
|                                                                 |
+-----------------------------------------------------------------+
```

b. DTR = 1 and RTS = 1 are output, then DSR and CTS are input. The results are OK if both DSR and CTS equal "1". An error message is displayed if either signal equals "0".

When DSR = 0:

```
+-----------------------------------------------------------------+
|                                                                 |
|    Error code = 1101                                            |
|    ERROR DTR DSR, DSR ALWAYS LOW                                |
|                                                                 |
+-----------------------------------------------------------------+
```

When CTS = 0:

```
+-----------------------------------------------------------------+
|                                                                 |
|    Error code = 1101                                            |
|    ERROR RTS CTS, CTS ALWAYS LOW                                |
|                                                                 |
+-----------------------------------------------------------------+
```

2) Data Transfer Check using Various Baud Rates

The setting is fixed to even parity, two stop bits, and an eight-bit data length. The check data is "00" - "FFh".

A timeout check during data transmission and reception and a comparison check of the sent data and received data is performed.

The baud rates for performing the checks are used in the order below:

75 bps
110 bps
150 bps
300 bps
600 bps
1200 bps
2400 bps
4800 bps
9600 bps

When the check is started, the following message appears:

```
SERIAL PORT CHECK
RS232C echo back check -- at various baud rates
Current baud rate is xxxx
Current test data is yy
```

(xxxx represents the baud rate used for the current check, and yy represents the test data.)

The program displays an error message if either the TX Shift Register Empty status is not assumed during data transmission or the Data Ready status is not assumed during data reception.

```
Error code = 1102
TIME OUT ERROR
```

Thesent data and received data is compared,and theprogram displays an error message if they do not match.

```
Error code = 1103
VERIFY ERROR
Sent data     --- xx
Redeived data --- yy
```

(xx represents the sent data and yy representes the received data.)

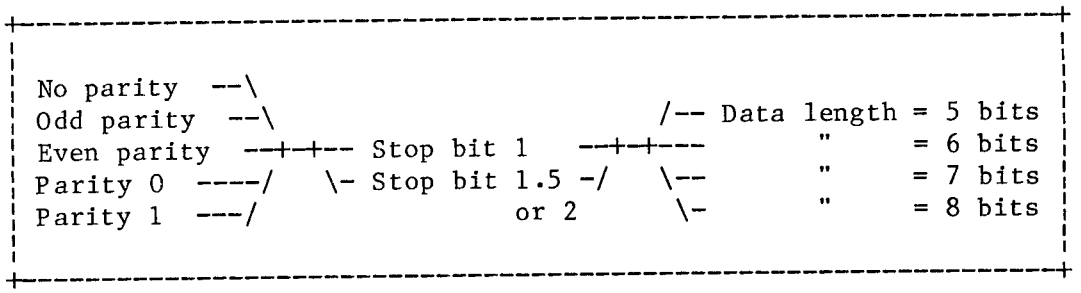
3) Data Transfer Check using Various Data Lengths, Stop Bits, and Parity

The baud rate is fixed to 9600 bps. The scope of the check data varies according to the data length.

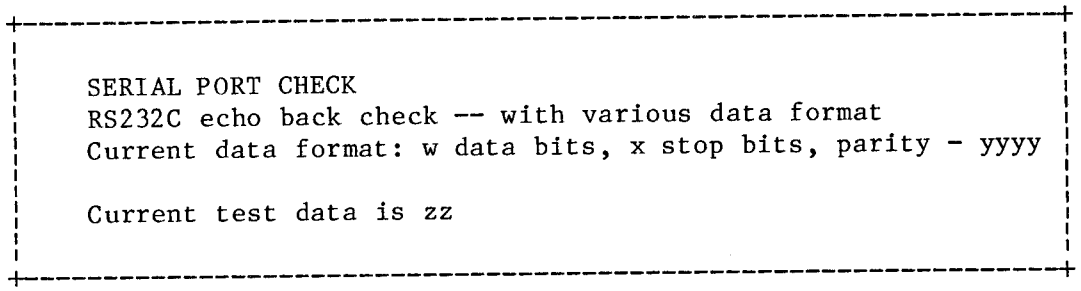
data length	check data
8 bits	00 - FFh
7 bits	00 - 7Fh
6 bits	00 - 3Fh
5 bits	00 - 1Fh

A timeout check during data transmission and reception and a comparison check of the sent data and received data is performed.

The data transfer conditions to be checked consist of the following combinations:



When the check is started, the following message appreas:



(w represents the data length of the current check, x represents the stop bits, yyyy represents the parity bit setting of NONE, ODD, EVEN, SPACED or MARKED, and zz represents the test data.)

In case of a timeout error detected during data transfer or mismatching of sent data and received data, the error message identical to that of Item 2) is displayed.

12. Alternate Serial Port Check

This module performs a loop-back check of the alternate serial port (alternate RS-232C port).

Before starting this check, attach the loop-back connector to the alternate serial port, then issue the instruction to start the check.

```
+-------------------------------------------------------------+
|                                                             |
|    ALTERNATE SERIAL PORT CHECK                              |
|    Attach loop-back connector to alternate serial port.     |
|    Enter Y to start this check when connector is attachd, or|
|    Enter N to return to the menu.                           |
|                                                             |
+-------------------------------------------------------------+
```

Since the checking procedure for the alternate serial port is identical to that for the serial port, its checking procedure is omitted here.

Only the differences are in port numbers and in the message titles:

```
+-------------------------------------------------------------+
|                                                             |
|    Error code = 1201                                        |
|    ERROR DTR DSR, DSR ALWAYS HIGH (or LOW)                  |
|    ERROR RTS CTS, CTS ALWAYS HIGH (or LOW)                  |
|                                                             |
+-------------------------------------------------------------+
```

```
+-------------------------------------------------------------+
|                                                             |
|    Error code = 1202                                        |
|    TIME OUT ERROR                                           |
|                                                             |
+-------------------------------------------------------------+
```

```
+-------------------------------------------------------------+
|                                                             |
|    Error code = 1203                                        |
|    VERIFY ERROR                                             |
|    Sent data     --- xx                                     |
|    Received data --- yy                                     |
|                                                             |
+-------------------------------------------------------------+
```

(xx represents the sent data and yy represents the received data.)

14. Dot-Matrix Printer Check

This module performs a printing check of the printer's with ASCII characters and bit images data.

Before starting this check, connect the printer to the parallel port, then issue the instruction to start.

```
+-------------------------------------------------------------+
|                                                             |
|    DOT-MATRIX PRINTER CHECK                                 |
|                                                             |
|    Is dot-matrix printer on-line (Y/N)?                     |
|                                                             |
+-------------------------------------------------------------+
```

The procedures for checking the printer are as follows:

(In case of test multiple times, only the printer connection check is performed.)

1) Printer Connection Status Check

A NULL code is output to the printer and the printer status is checked. If an error is detected, the corresponding error message is displayed.

```
+-------------------------------------------------------------+
|                                                             |
|    DOT-MATRIX PRINTER CHECK                                 |
|    Error code = 1401                                        |
|    Status : Time out error                                  |
|    Status : I/O error                                       |
|    Status : Not on-line                                     |
|    Status : Acknowledge error                               |
|    Status : Busy                                            |
|    Status : Out of paper                                    |
|                                                             |
+-------------------------------------------------------------+
```

2) Printing Check of Printer

ASCII characters and bit images are printed repeatedly by the printer, then you can check the printing results:

```
+-------------------------------------------------------------+
|                                                             |
|    Print test data                                          |
|    Text data       (20H-7FH,A0H-FFH)                        |
|    Bit-image data (00H-FFH)                                 |
|                                                             |
|    Press any key to return to the menu.                     |
|                                                             |
+-------------------------------------------------------------+
```

a. Printing Check of ASCII Characters
The ASCII characters "20H"-"7FH" and "A0H"-"FFH" are printed by the printer. The data is printed after printing the following title:

```
+-------------------------------------------------------------+
|                                                             |
|    Text data (20H-7FH,A0H-FFH)                              |
|                                                             |
+-------------------------------------------------------------+
```

Printing is performed at 80 columns per line. If an error is detected during printing, an error message is displayed that is identical to that of Item 1).

b. Printing Check of Bit Images data
The bit images data of "00H"-"FFH" are printed by the printer. The data is printed after printing the following message:

```
+-------------------------------------------------------------+
|                                                             |
|    Bit-image data (00H-FFH)                                 |
|                                                             |
+-------------------------------------------------------------+
```

The control code for bit-image printing is "ESC K n1 n2" (specification of single-density bit images). If an error is detected during printing, an error message is displayed that is identical to that of Item 1).

17. Hard Disk Drives and Controller Check

This module checks the hard disks and the hard disk drives. First of all, select which check is to be performed from the menu.

```
+-------------------------------------------------------------+
|                                                             |
|    HARD DISK DRIVE(S) AND CONTROLLER CHECK MENU             |
|                                                             |
|    1 - Seek check                                           |
|    2 - Write, read check                                    |
|    3 - Head select check                                    |
|    4 - Error detection and correction check                 |
|    5 - Read, verify check                                   |
|    6 - Run all above checks                                 |
|                                                             |
|    0 - Exit                                                 |
|                                                             |
|    Enter selection number:                                  |
|                                                             |
+-------------------------------------------------------------+
```

(In case of test multiple times, the following checks are consecutively executed in the order listed.)

```
+-------------------------------------------------------------+
|                                                             |
|    1 - Seek check                                           |
|    2 - Write, read check                                    |
|    3 - Head select check                                    |
|    4 - Error detection and correction check                 |
|                                                             |
+-------------------------------------------------------------+
```

Each of the checking procedures are described as follows:

1) Seek Check

The quantity of installed hard disk drives is first set using function 8 of int 13. The following message is displayed in case two hard disk drives are installed, so input the name of the drive you wish to check.

```
+-------------------------------------------------------------+
|                                                             |
|    Check which drive (C/D)?                                 |
|                                                             |
+-------------------------------------------------------------+
```

The seek check performs a sequential check on all heads simultaneously from the innermost cylinder position to the outermost cylinder position, then checks the seek operation.

```
+-----------------------------------------------------------------+
|                                                                 |
|    SEEK CHECK                                                   |
|                                                                 |
|    Current cylinder is xxx                                      |
|                                                                 |
+-----------------------------------------------------------------+
```

(The xxx represents the number of the cylinder being sought.)

If an error is detected in the seek operation, the following message is displayed:

```
+-----------------------------------------------------------------+
|                                                                 |
|    HARD DISK DRIVE(S) AND CONTROLLER CHECK                      |
|    Error code = 1701                                            |
|    SEEK ERROR                                                   |
|    CYLINDER --- xxx                                             |
|    HEAD     --- y                                               |
|                                                                 |
+-----------------------------------------------------------------+
```

(xxx represents the number of the cylinder detected the error and y represents the head number.)

2) WRITE/READ Check

Drive selection is identical to that of Item 1). Next, a precaution is displayed when this check is started.

```
+-----------------------------------------------------------------+
|                                                                 |
|    The data on the highest physical cylinder may be destroyed   |
|                                                    by this check.|
|    Enter Y to start this check.                                 |
|    Enter N to return to the menu.                               |
|                                                                 |
+-----------------------------------------------------------------+
```

The WRITE/READ check performs a WRITE/READ check for all sectors of all heads of the innermost cylinder (highest cylinder). The check data is "6db6h".

```
+-----------------------------------------------------------------+
|                                                                 |
|    WRITE, READ CHECK                                            |
|                                                                 |
+-----------------------------------------------------------------+
```

If an error is deteced during the writing or reading of data, the following message is displayed.

In case of write error:

```
HARD DISK DRIVE(S) AND CONTROLLER CHECK
Error code = 1702
WRITE ERROR
CYLINDER --- xxx
HEAD     --- y
SECTOR   --- zz
```

(xxx represents the number of the cylinder detected the error, y represents the head number, and zz represents the sector number.)

In case of read error:

```
HARD DISK DRIVE(S) AND CONTROLLER CHECK
Error code = 1703
READ ERROR
CYLINDER --- xxx
HEAD     --- y
SECTOR   --- zz
```

(xxx represents the number of the cylinder detected the error, y represents the head number, and zz represents the sector number.)

3) Head Selection Check

Drive selection is identical to Item 1). The head selection check makes each head seek the maximum cylinder position, then checks the head selection status.

```
HEAD SELECT CHECK
```

If the head is not properly selected, the following message is displayed:

```
HARD DISK DRIVE(S) AND CONTROLLER CHECK
Error code = 1704
HEAD ERROR
HEAD     --- x
```

(The x represents the number of the head detected the error.)

4) Error Detection/Correction Check

The procedure is identical to that of Item 2) up to the display of the precaution.

```
+-----------------------------------------------------------------+
|                                                                 |
|    ERROR DETECTION AND CORRECTION CHECK                         |
|                                                                 |
+-----------------------------------------------------------------+
```

a. In the error detection check, the test data "6db6h" is prepared in the buffer then is written to the hard disk using the normal "write" instruction. Writing and reading are performed at Sector number 1 of the highest head of the highest cylinder.
Next, the data is read using "read long", its leading byte is destroyed (= "2ah"), then re-written it using write long".
If a READ or WRITE error occurs up to this point, an error message identical to that of Item 2) is displayed.
The data is then read using the normal "read" instrucion, and the the following message is displayed if no error has been detected:

```
+-----------------------------------------------------------------+
|                                                                 |
|    HARD DISK DRIVE(S) AND CONTROLLER CHECK                      |
|    Error code = 1705                                            |
|    ERROR DETECTION ERROR                                        |
|                                                                 |
+-----------------------------------------------------------------+
```

b. In the error correction check, the test data "6db6h" is prepared in the buffer then is written to the hard disk using the normal write instrucion. Writing and reading are performed at Sector number 1 of the highest head of the highest cylinder.
Next the data is read using "read long", its leading byte is destroyed (= "6eh"), then re-written using "write long". (5 bits error.)
If a READ or WRITE error occurs up to this point, a error message identical to that of Item 2) is displayed.
The data is then read using the normal "read" instruction, and the read data and the test data are compared. An error message is displayed if the read data and test data do not match. Concurrently, detection of ERROR CORRECTION is also checked.

```
+-------------------------------------------------------------+
|                                                             |
|    HARD DISK DRIVE(S) AND CONTROLLER CHECK                  |
|    Error code = 1706                                        |
|    ERROR CORRECTION ERROR                                   |
|                                                             |
+-------------------------------------------------------------+
```

5) READ/VERIFY Check

Drive selection is identical to Item 1). In the READ/VERIFY check, all heads from the highest cylinder to Cylinder No. 0 are read in track units, and the read statuses that detected bad sector or any other READ error are preserved.

```
+-------------------------------------------------------------+
|                                                             |
|    READ, VERIFY CHECK                                       |
|                                                             |
|    Current cylinder is xxx                                  |
|                                                             |
+-------------------------------------------------------------+
```

(The xxx represents the number of the cylinder being read.)

When the reading of all cylinders up to Cylinder No. 0 is completed, the results are displayed:

```
+-------------------------------------------------------------+
|                                                             |
|    READ, VERIFY CHECK                                       |
|                                                             |
|    BAD TRACKS ..................... xxxx                    |
|    READ ERROR TRACKS ............. yyyy                    |
|    GOOD TRACKS ................... zzzz                    |
|                                                             |
|    Press ENTER to return to the menu                        |
|                                                             |
+-------------------------------------------------------------+
```

(xxxx represents the total number of bad tracks, yyyy represents the total number of tracks detecting a READ error, zzzz represents total number of normal tracks.)

6) Run All Above Checks

When "Run all above checks" is selected, the preceding checks described in Items 1) to 5) are consecutively executed.

21. Alternate Parallel Port Check

This module performs a loop-back check of the alternate parallel port.

Before starting this check, attach the loop-back connector to the alternate parallel port, then issue the instruction to start the check.

```
+-------------------------------------------------------------+
|                                                             |
|   ALTERNATE PARALLEL PORT CHECK                             |
|   Attach loop-back connector to alternate parallel port.    |
|   Enter Y to start this check when connector is attached, or|
|   Enter N to return to the menu.                            |
|                                                             |
+-------------------------------------------------------------+
```

Since the checking procedure for the alternate parallel port is identical to that for the parallel port, its checking procedure is omitted here.

Only the differences are port numbers and the error message titles.

Data output port	278h
Status port	279h
Controll port	27ah

```
+-------------------------------------------------------------+
|                                                             |
|   ALTERNATE PARALLEL PORT CHECK                             |
|   Error code = 2101                                         |
|   ERROR   PIN xx                                            |
|                                                             |
+-------------------------------------------------------------+
```

(The xx represents the pin number corresponding to bit number which is detected as an error.)

CHAPTER

8

DIFFERENCE BETWEEN 10MHz AND 12MHz

TABLE OF CONTENTS

8.1 MAJOR PARTS

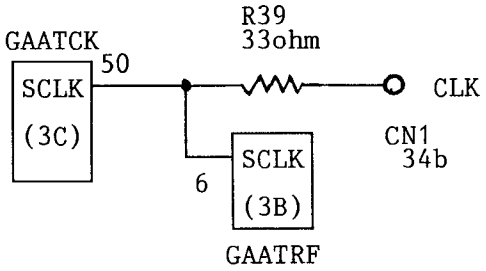
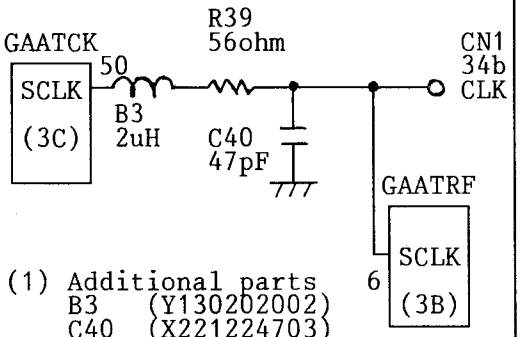
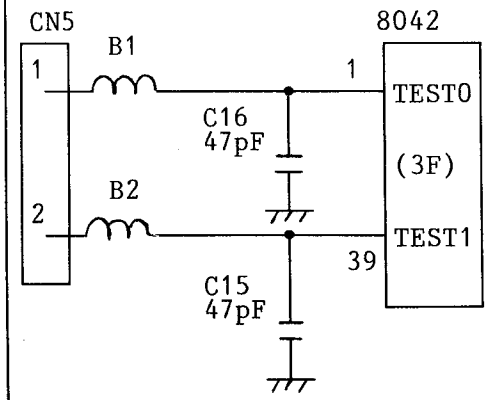
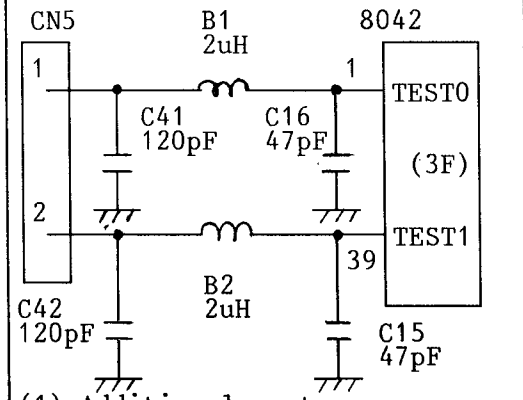
8.1.1 Excluding P.C.B. Units

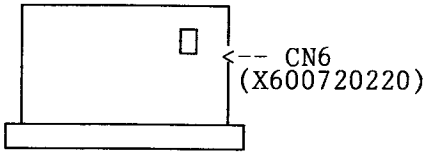
Unit Name	Description	Modification		Reason for Modification	Substitution Possible
		10MHz	12MHz		
Switch Panel Label	Modification the description of the clock speed	Switch Panel Label 01 (Y126027051) or Switch Panel Label 02 (Y126027151)	Switch Panel Label B01 (Y126042051)	Because the CPU clock speed is increased from 10MHz to 12MHz.	No
Earth Plate C	Addition of the Earth Plate C	No Earth Plate C is installed.	Earth Plate C is installed (Y126039251)	Countermeasure for FCC	NA
Hard Disk Cable	Modification of the Hard Disk Cables	Cable set #5BX (Y126306000) Cable set #5BY (Y126310000)	Cable set #5DY (Y127300300) Cable set #5DZ (Y127300400)	Hard Disk Cables for 12 MHz version should be longer than the 10MHz's because the location of the option slot connector is changed.	No
Serial Number Plate	Modification of the Serial Number Plate	Serial Number Plate 03 (Y126025251)	Serial Number Plate B06 (Y126041651)	Alphabet "A" is prefixed to the serial number. [Old] 010001 --- [New] A010001 --	No
Code Label	Modification of the Code Label	(abbreviated)	(abbreviated)	(abbreviated)	No
SPFG Board	Circuit design modification	SPFG board unit (Y12720100001)	SPFG board unit (Y12720110000)	To solve the format error with the 360KB or 720KB FDD at 12MHz.	No
ROM BIOS	(1) New Ver. (2) Modification of the ROM type	Version 1.02 ATR-B3 (Y126814002) ATR-C3 (Y126815002) ROM type: 27256-15	Version 2.00 ATR-B5 (Y126814004) ATR-C5 (Y126815004) ROM type: 27128-15	(1) New version (2) Cost reduction (ROM type: 27256 -> 27128)	No
Monitor Connector Cable	Addition of the Monitor Connector Cable	No Monitor Connector Cable is used.	Cable set #5EM (Y126311000)	Countermeasure for FCC	NA

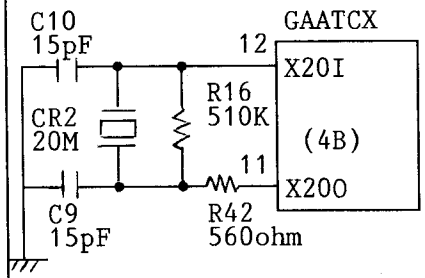
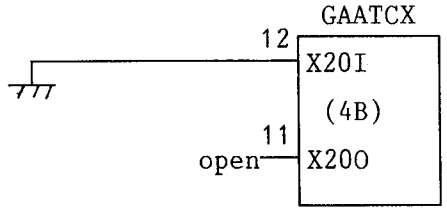
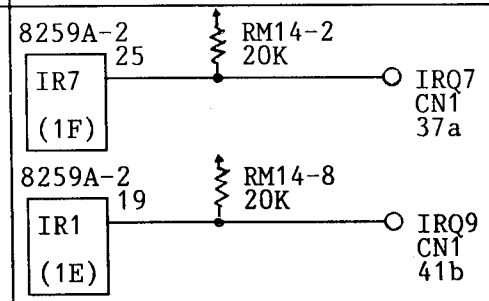
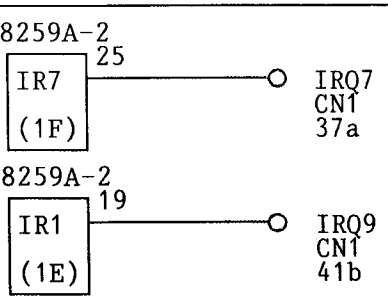
Unit Name	Description	Modification		Reason for Modification	Substitution Possible
		10MHz	12MHz		
ANT-RM Board	Circuit design modification	ANT-RM board unit (Y12620300000)	ANT-RM board unit (Y12620700000)	(1) To improve RAM access speed (2) To adjust signal timing	No
ANT-MT Board	(1) Cable set #5BT addition (2) Modification of the location of the option slot connector	ANT-MT board unit (Y12620200000)	ANT-MT board unit (Y12620800000)	(1) Countermeasure for FCC (2) To allow to use a full length Hard Disk Controller	No
ANT-RMA Board	ANT-RMA board unit newly authorized	No ANT-RMA board unit is used.	ANT-RMA board unit (Y12620900000) * This is an alternative unit for the ANT-RM board unit.	To keep constant parts supply	No
ANTA Board	Circuit design modification	ANTA board unit (Y12620500000)	ANTA board unit (Y12620600000)	(1) To increase CPU speed (2) Countermeasure for FCC (3) Cost reduction (4) Countermeasure for the genius problem (5) To improve the execution speed of the keyboard controller	No

8.2 COMPONENT PARTS

8.2.1 ANTA Board Unit

Unit	Description	Modification		Reason for Modification
		10MHz	12MHz	
ANTA Board Y12620500000 --> Y12620600000	(1) Addition of a filter circuit		 (1) Additional parts B3 (Y130202002) C40 (X221224703) (2) Parts modification R39 : 33ohm ----> 56ohm (X154413302) (X154415602)	Countermeasure for FCC
	(2) Improvement of the filter circuit		 (1) Additional parts C41 (X221221213) C42 (") (2) Parts modification B1 (X506000029)->(Y130202002) B2 (")->(")	Countermeasure for FCC

Unit	Description	Modification		Reason for Modification
		10MHz	12MHz	
ANTA Board	(3) Connector addition	No connector CN6 is installed.	Connector CN6 is installed. ANTA board unit  	Countermeasure for FCC
	(4) Modification of the DMA controller	Location : 2E and 2F Part : NEC uPD8237AC-5 (X400082374) or NEC uPD8237AC-2 (X400082371)	Location : 2E and 2F Part : FUJITSU MB89237A-P (X400892370) * 6MHz version	To improve DMAC clock speed capability.
	(5) Modification of the timer/counter	Location : 3E Part : INTEL 8254-2 (X400082541)	Location : 3E Part : INTEL 8254 (X400082540) or INTEL 8254-2 (X400082541) or AMD P82C54 (X400825400) or AMD P82C54-2 (X400825401)	Cost reduction

Unit	Description	Modification		Reason for Modification
		10MHz	12MHz	
ANTA Board	(6) Modification of the CPU	Location : 2A Part : SAB80286-1-R *LCC type (X400802861) or INTEL 80286-10 (X401802861) or AMD R80L286-10/C2H (X402802868)	Location : 2A Part : AMD *PLCC type N80L286-12/C2H (X402802868) or INTEL N80286-12 (X402802868)	(1) To improve CPU clock speed. (2) Cost reduction (LCC -> PLCC)
	(7) Modification of the CPU socket	Location : 2A Part : LCC type (X630116802)	Location : 2A Part : PLCC type (X630116820)	Cost reduction
	(8) Deletion of the 20MHz OSC circuit			This circuit is not necessary because the computer system does not use 10MHz.
	(9) Deletion of the resistors			Countermeasure for genius problem.
	(10) New Keyboard controller version	Location : 3F Part : C42051KA (Y126813000)	Location : 3F Part : C42051KB (Y126813001)	To improve the execution speed of the keyboard controller.

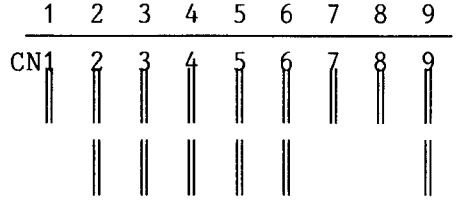
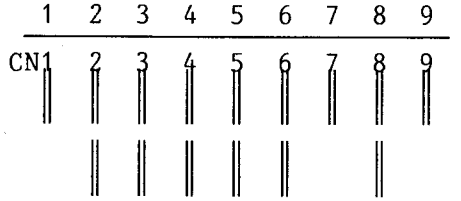
8.2.2 ANT-RM Board Unit

Unit	Description	Modification		Reason for Modification
		10MHz	12MHz	
ANT-RM Board Y12620300000 ---> Y12620700000	(1) Modification of the D-RAM chips	Location : 19B to 22B Part : FUJITSU MB81464-12P (X400584641) or NEC uPD41464C-12 (X400414642) or HITACHI HM50464-12 (X400504641)	Location : 19B to 22B FUJITSU MB81464-10P (X400584643) or NEC uPD41464C-10 (X400414641)	To improve RAM access speed.
		Location : 21A and 22A Part : NEC uPD4164C-12 (X400141645) or MATSUSHITA MN4164P-12 (X400041643)	Location : 21A and 22A Part : NEC uPD4164C-10 (X400141646)	
	(2) Modification of the delay line chip	Location : RL1 Part : 200ns type (X510000220)	Location : RL1 Part : 150ns type (X510000290)	To adjust signal timing
	(3) Modification of the P-ROM	Location : 24A and 24B Part : ATR-B3 (Y126814002) ATR-C3 (Y126815002) 27256-15 type Version 1.02	Location : 24A and 24B Part : ATR-B5 (Y126814004) ATR-C5 (Y126815004) 27128-15 type Version 2.00	(1) Cost reduction (2) New version

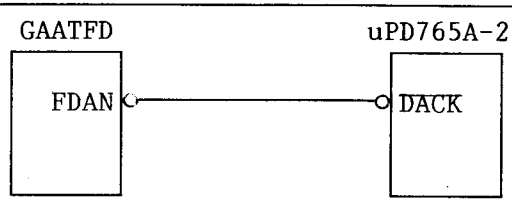
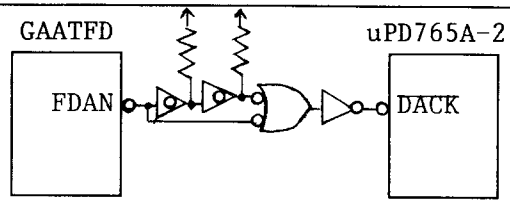
8.2.3 ANT-RMA Board Unit

Unit	Description	Modification		Reason for Modification
		10MHz	12MHz	
ANT-RMA Board	ANT-RMA board unit newly authorized	Not installed	Installed (Alternative unit for ANT-RM board)	To keep constant parts supply.

8.2.4 ANT-MT Board Unit

Unit	Description	Modification		Reason for Modification
		10MHz	12MHz	
ANT-MT Board Y12620200000 ---> Y12620800000	(1) Addition of the cable set #5BT	Not installed	Installed Part: Cable set #5BT (Y126303000)	Countermeasure for FCC
	(2) Modification of the slot location			To allow a full length Hard Disk Controller to be installed in connector CN8.

8.2.5 SPFG Board Unit

Unit	Description	Modification		Reason for Modification
		10MHz	12MHz	
SPFG Board Y12720100001 --->Y12720110000	(1) Addition of a delay circuit		 Additional Parts: R57 (X154414720) R58 (")	To solve the format error with the 360KB or 720KB FDD at 12MHz.

8.3 JUMPER SETTINGS

8.3.1 ANTA Board Jumper Settings

Unit	Jumper									Function		Factory Settings	
			J6	J5	J4	J3	J2	J1			10MHz	12MHz	
ANTA Board			-	-	-	-	-	A		Set CPU clock (6/8/10MHz)	Prohibited	J1: A	J1: B
			-	-	-	-	-	B		Prohibited	Set CPU clock (6/8/12MHz)		
			-	-	-	A	A	-		Prohibited	<---	J2: A	<---
			-	-	-	A	B	-		Use CPU clock for NPX clock	<---		
			-	-	-	B	A	-		Use 8MHz clock for NPX clock	<---	J3: B	
			-	-	-	B	B	-		Prohibited	<---		
			-	-	A	-	-	-		2 wait cycles for EPROM (note 1)	<--- (note 2)	J4: A	<---
			-	-	B	-	-	-		1 wait cycle for EPROM (note 1)	<--- (note 2)		
			A	A	-	-	-	-		4 wait cycles (note 3)	<--- (note 4)	J5: A	<---
			A	B	-	-	-	-		3 wait cycles (note 3)	<--- (note 4)		
			B	A	-	-	-	-		2 wait cycles (note 3)	<--- (note 4)	J6: A	
			B	B	-	-	-	-		1 wait cycle (note 3)	<--- (note 4)		

Slide switch settings

Slide Switch	10MHz	12MHz
Monitor select switch	(factory setting : MONO) MONO COLOR	(factory setting : MONO) MONO COLOR
CPU speed select switch	(factory setting : 8MHz) 6MHz 8MHz 10MHz	(factory setting : 8MHz) 6MHz 8MHz 12MHz

note 1 : These selectable wait cycles are available during 10MHz.
note 2 : These selectable wait cycles are available during 12MHz.
note 3 : Wait cycles for external. 16-bit devices.
These selectable wait cycles are available during 10MHz.
note 4 : Wait cycles for external. 16-bit devices.
These selectable wait cycles are available during 12MHz.

\- : Not applicable
<--- : Same as 10MHz

8.3.2 ANT-RM/RMA Board Jumper Settings

Unit	Jumper									Function		Factory Settings	
		J7	J6	J5	J4	J3	J2	J1			10MHz	12MHz	10MHz	12MHz
ANT-RM / ANT-RMA Board		-	-	-	-	A	A	A			RAM size 640KB	<---	J1: A	
		-	-	-	-	A	A	B			512KB (Disable upper 128KB)	<---		
		-	-	-	-	A	B	A			Prohibited	<---	J2: A	<---
		-	-	-	-	A	B	B			256KB (Disable upper 384KB)	<---		
		-	-	-	-	B	A	A			Prohibited	<---	J3: A	
		-	-	-	-	B	A	B			Prohibited	<---		
		-	-	-	-	B	B	A			Prohibited	<---		
		-	-	-	-	B	B	B			0KB (Disable upper 640KB)	<---		
		-	-	A	A	-	-	-			128KB ROM size (27128)	<---	J4: B	J4: A
		-	-	A	B	-	-	-			Prohibited	<---		
		-	-	B	A	-	-	-			Prohibited	<---	J5: B	J5: A
		-	-	B	B	-	-	-			256KB ROM size (27256)	<---		
		A	A	-	-	-	-	-			Select ROM sockets 24A & 24B	<---	J6: A	
		A	B	-	-	-	-	-			Prohibited	<---		<---
		B	A	-	-	-	-	-			Prohibited	<---	J7: A	
		B	B	-	-	-	-	-			Select ROM sockets 23A & 23B	<---		

- : Not applicable

<- : Same as 10MHz

8.3.3 SPFG Board Jumper Settings

Unit	Jumper										Function		Factory Settings	
	J8	J7	J6	J5	J4	J3	J2	J1	J10	J9	10MHz	12MHz	10MHz	12MHz
SPFG Board	-	-	-	-	-	-	A	A	-	-	Primary register set (AT FDC)	<---	J1 : A	<----
	-	-	-	-	-	-	A	B	-	-	Secondary register set (")	<---		
	-	-	-	-	-	-	B	A	-	-	PC register set (FDC)	<---	J2 : A	
	-	-	-	-	-	-	B	B	-	-	Disable FDC register set	<---		
	-	-	-	-	A	A	-	-	A	-	Primary parallel I/F: IRQ7	<---	J3 : A	<----
	-	-	-	-	B	A	-	-	B	-	Secondary parallel I/F: IRQ5	<---	J4 : A	
	-	-	-	-	A	B	-	-	A	-	Parallel I/F on video adapter:	IRQ7 <---	J10: A	
	-	-	-	-	B	B	-	-	-	-	Disable parallel I/F	<---		
	-	-	A	A	-	-	-	-	-	A	Primary serial I/F: IRQ4	<---	J5 : A	<----
	-	-	B	A	-	-	-	-	-	B	Secondary serial I/F: IRQ3	<---	J6 : A	
	-	-	A	B	-	-	-	-	-	-	Disable serial I/F	<---	J9 : A	
	-	-	B	B	-	-	-	-	-	-	Disable serial I/F	<---		
	-	A	-	-	-	-	-	-	-	-	AT compatible FDD I/F	<---	J7 : A	<----
	-	B	-	-	-	-	-	-	-	-	EPSON PC AX FDD I/F	<---		
	A	-	-	-	-	-	-	-	-	-	Standard setting	<---	J8 : A	<----
	B	-	-	-	-	-	-	-	-	-	Test mode of VCO	<---		

- : Not applicable

<- : Same as 10MHz

8.3.4 WHDC Board Jumper Settings

Unit	Jumper										Function		Factory Settings	
						J3	J2	J1			10MHz	12MHz	10MHz	12MHz
WHDC Board						– –	– –	B A			Select primary address sets Select secondary address sets	<--- <---	J1: A	<---
						– –	B A	– –			Non-latched status Latched status	<--- <---	J2: B	<---
						B A	– –	– –			WAH mode WA2 mode	<--- <---	J3: B	<---

– : Not applicable

<- : Same as 10MHz

8.4 COMPATIBILITY LIST

8.4.1 Major Unit

Unit			10MHz	12MHz
Main Unit	Power Supply	ATRPS ANPS	OK OK	OK OK
K.B. Unit	-----	--------	OK	OK
FDD Unit	360KB	MD5201-57 -58	OK OK	OK OK
	1.2MB	FD1155C FD1157C MD5501-61	OK OK OK	OK OK OK
Display Adapter	Mono	MRS-MO Board	OK (See *1)	OK (See *1)
	Color	MRS- CR Board MGA Board EGA Board	OK OK OK (See *2)	OK OK OK (See *2)

Descriptions:

*1 : Unit code Y14420620000 should be used.

*2 : Unit code Y12720400001 ---- Code view problem may occur.
Unit code Y12720400002 ---- Code view problem is solved on this version.

8.4.2 P.C.B Unit

Board		10MHz	12MHz
ANTA Board	Y12620100000	(See *d)	NG
	Y12620100001	(See *d)	NG
	Y12620100002	(See *d)	NG
	Y12620100003	OK	NG
	Y12620100004	OK	NG
	Y12620500000	OK	NG
	Y12620600000	NG	OK
ANT-RM Board	Y12620300000	OK	NG
	Y12620700000	(See *a)	OK
ANT-RMA Board	Y12620900000	(See *a)	OK
ANT-MT Board	Y12620200000	OK	(See *b)
	Y12620200001	OK	(See *b)
	Y12620800000	(See *b)	OK
SPFG Board	Y12720100000	OK	NG
	Y12720100001	OK	NG
	Y12720110000	(See *a)	OK
WHDC Board	Y12720300000	(See *c & *d)	(See *c & *d)
	Y12720310000	(See *c)	(See *c)
	Y12720300001	(See *d)	(See *d)
	Y12720310001	OK	OK

Descriptions:

*a : Should be "OK" but an additional compatibility check is required.
*b : The location of the option-slot connectors are different.
*c : XENIX problem may occur.
*d : This board may not satisfy FCC standard.

LIST OF DIAGRAMS

EQUITY III+/ EPSON PC AX
ANTA BOARD
UNIT NO. Y12620100000

A-1

CN1 TO CN12 ON ANT-MT BOARD

CN2 TO CN1 ON ANT-RM BOARD

CN3 TO J1 ON ANT-LS BOARD

CN6 TO J1 ON ANT-MT BOARD

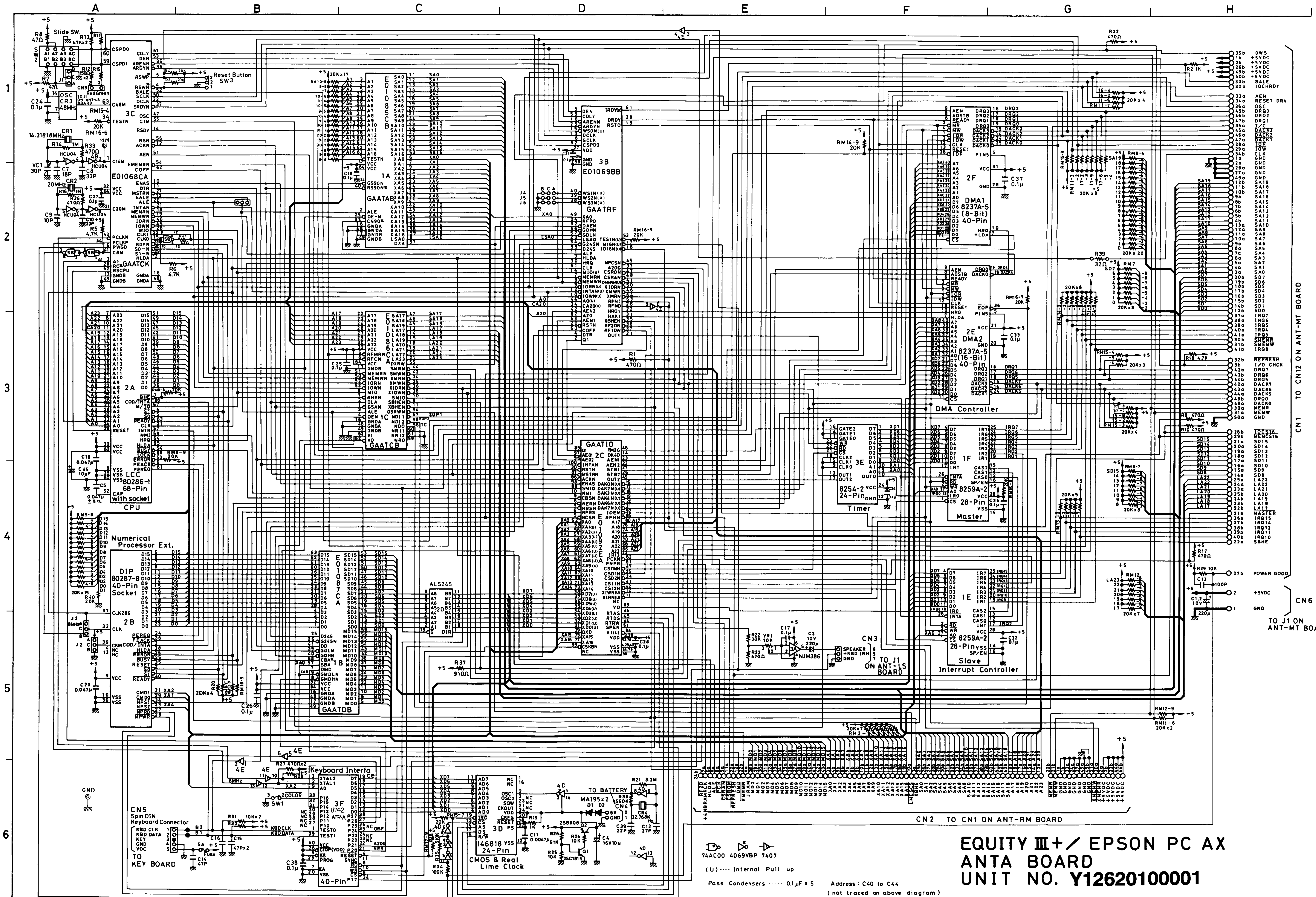
CN5 Spin DIN Keyboard Connector — TO KEY BOARD

74AC00 4069VBP 7407

(U)---- Internal Pull up

Pass Condensers ----- 0.1μF x 5

Address : C40 to C44 (not traced on above diagram)



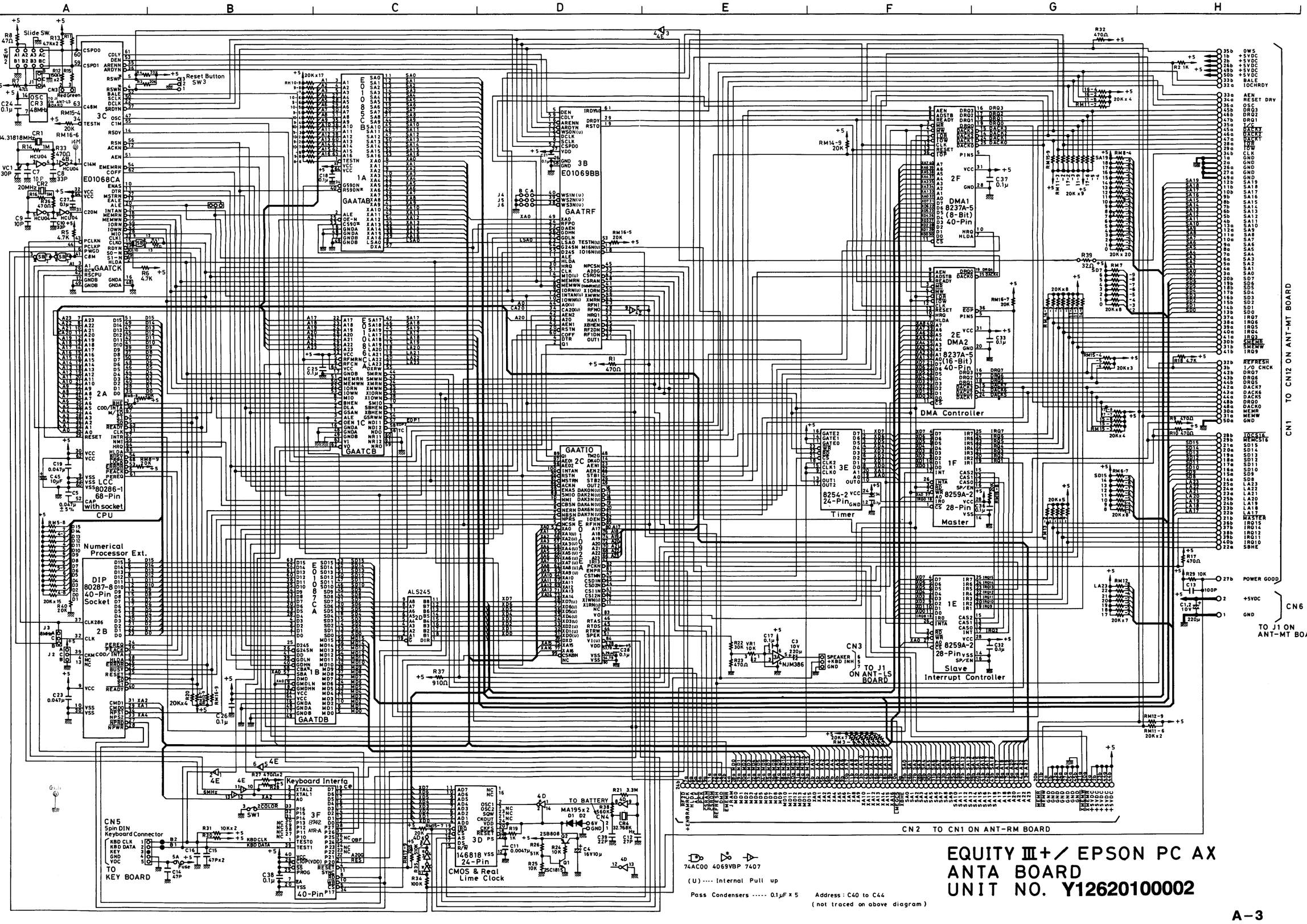
CPU
80286-1 68-Pin LCC with socket
Numerical Processor Ext.
DIP 80287-8 40-Pin Socket
E01068CA
GAATCK
E01069BB
GAATRF
GAATAB
GAATCB
GAATDB
GAATIO
DMA1 8237A-5 (8-Bit) 40-Pin
DMA2 8237A-5 (16-Bit) 40-Pin
DMA Controller
8254-2 24-Pin
Timer
8259A-2 28-Pin
Master
Slave
Interrupt Controller
ALS245
Keyboard Interface
8742 40-Pin
146818 24-Pin
CMOS & Real Lime Clock
CN1 TO CN12 ON ANT-MT BOARD
CN2 TO CN1 ON ANT-RM BOARD
CN3 TO J1 ON ANT-LS BOARD
CN5 5pin DIN Keyboard Connector
TO KEY BOARD
CN6 TO J1 ON ANT-MT BOARD
TO BATTERY
Reset Button SW3
Slide SW

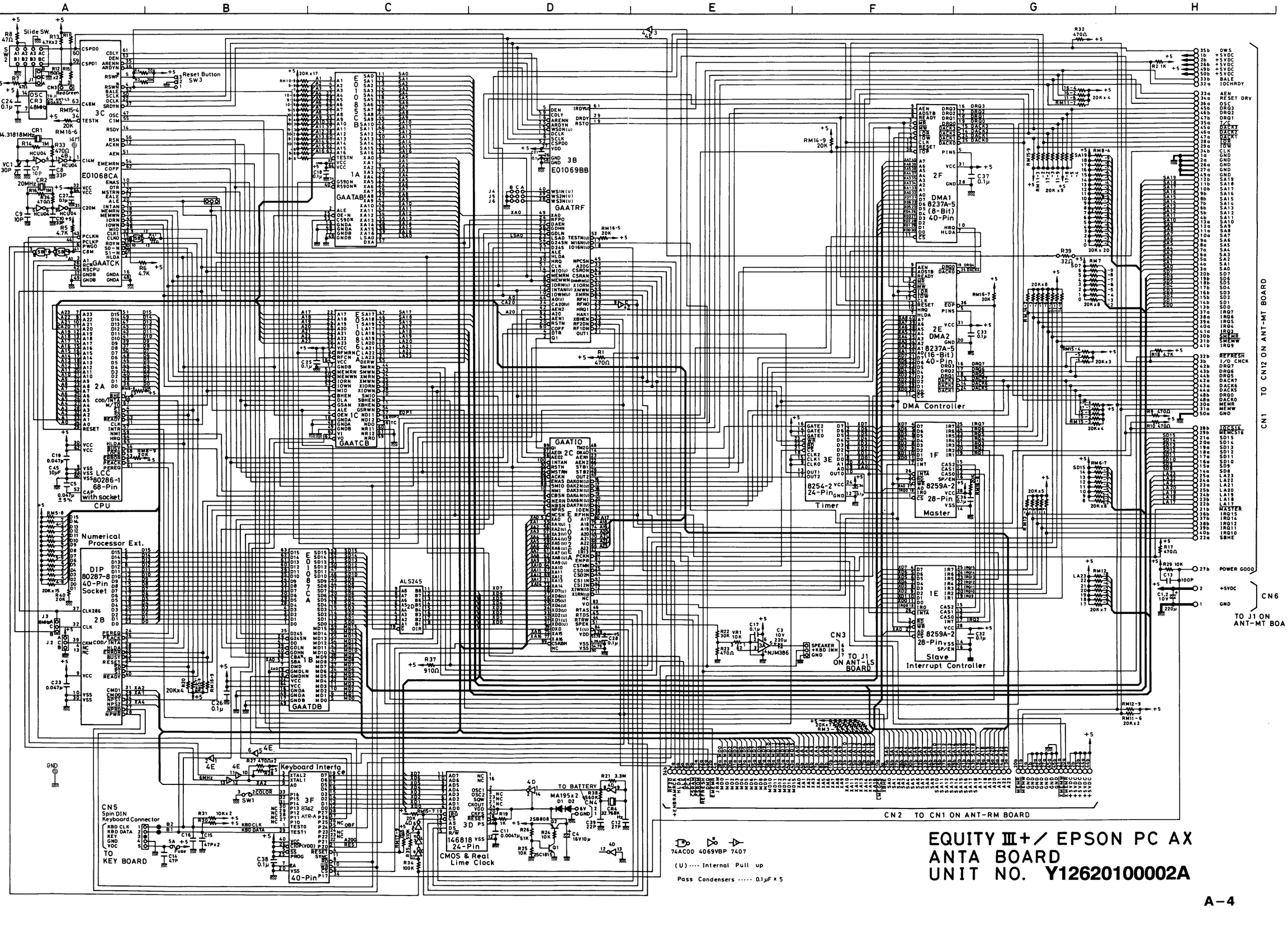
74AC00 4069VBP 7407

(U) ---- Internal Pull up

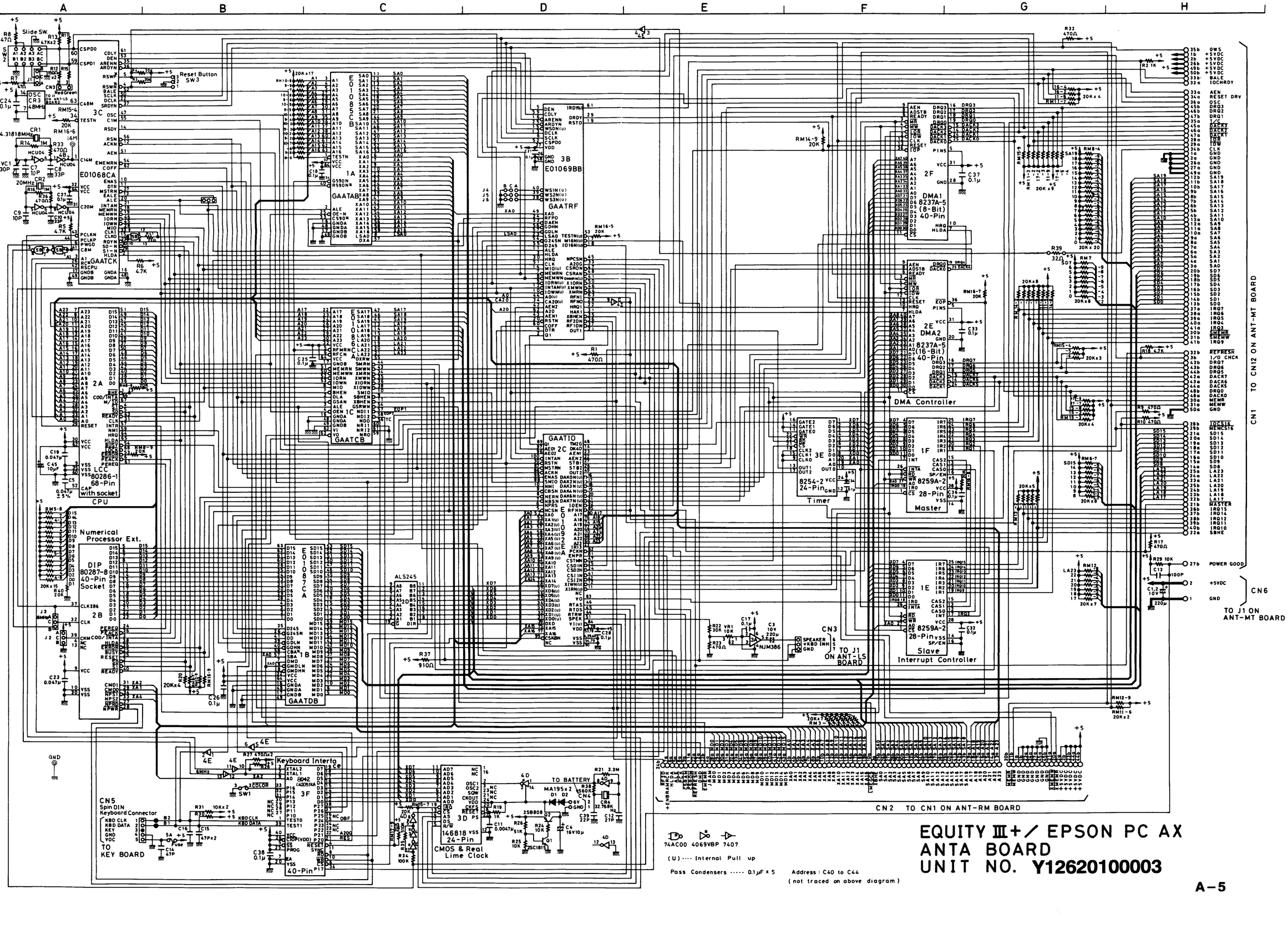
Pass Condensers ----- 0.1μF x 5   Address : C40 to C44 (not traced on above diagram)

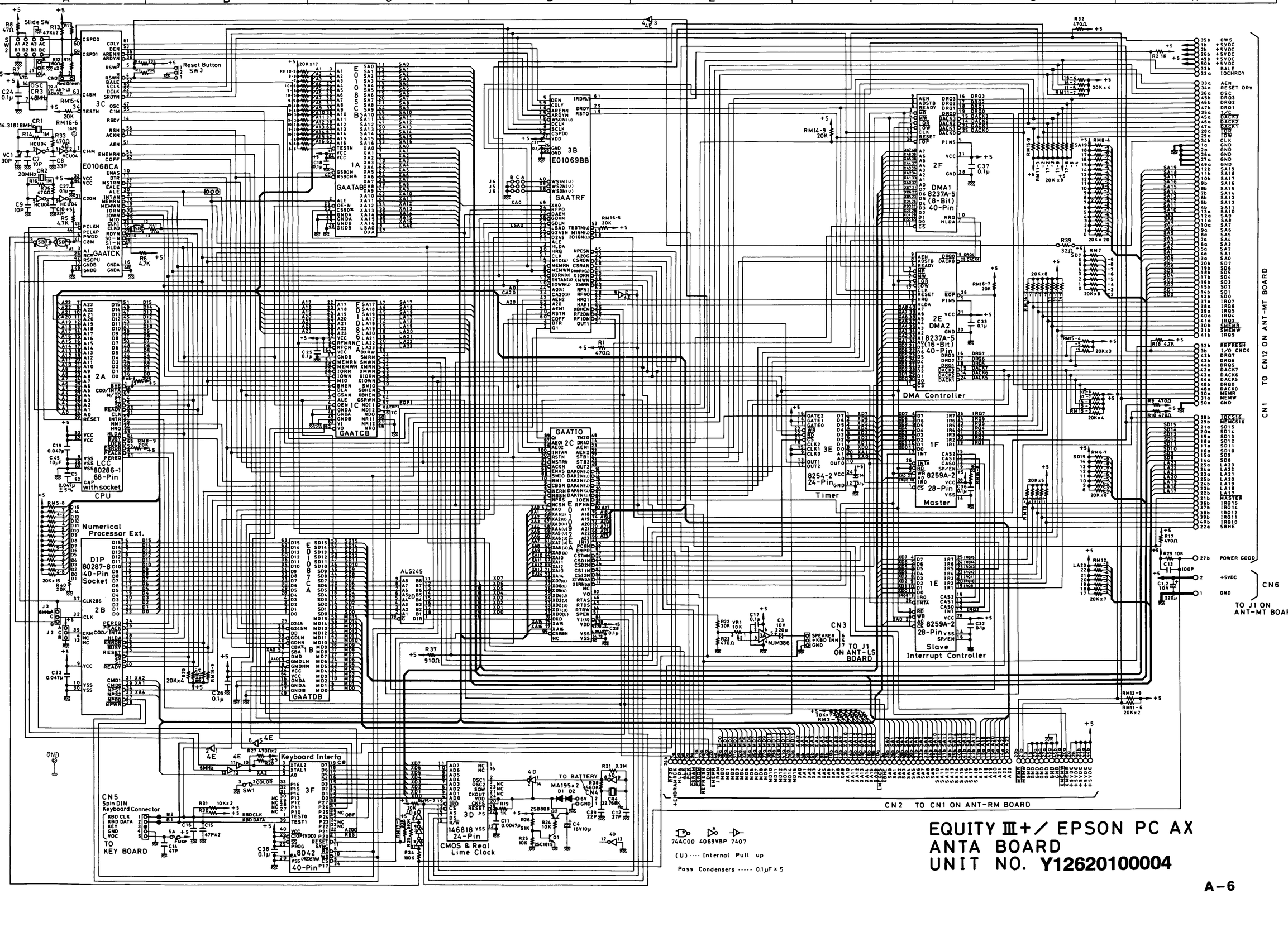
EQUITY Ⅲ+ / EPSON PC AX
ANTA BOARD
UNIT NO. Y12620100001


A
B
C
D
E
F
G
H
1
2
3
4
5
6
Slide SW.
Reset Button SW3
OSC
48MHz
CR1
14.31818MHz
CR2
20MHz
E01068CA
GAATCK
2A
LCC
80286-1
68-Pin
with socket
CPU
Numerical Processor Ext.
DIP
80287-8
40-Pin
Socket
2B
CLK286
1A
GAATAB
1B
GAATDB
1C
GAATCB
2C
GAATIO
2D
ALS245
3A
E01069BB
3B
GAATRF
3C
3D PS
146818 VSS
24-Pin
CMOS & Real
Lime Clock
Keyboard Interface
3F
8742
ATR-A
40-Pin
CN5
Spin DIN
Keyboard Connector
TO
KEY BOARD
2COLOR
SW1
MA195x2
2SB808
2SC1815
TO BATTERY
CR4
32.768K
74AC00 4069VBP 7407
(U)---- Internal Pull up
Pass Condensers ----- 0.1μF x 5
Address : C40 to C44
(not traced on above diagram)
DMA1
8237A-5
(8-Bit)
40-Pin
2F
DMA2
8237A-5
(16-Bit)
40-Pin
2E
DMA Controller
8254-2
24-Pin
Timer
3E
8259A-2
28-Pin
Master
1F
8259A-2
28-Pin
Slave
Interrupt Controller
1E
CN3
TO J1
ON ANT-LS
BOARD
CN2 TO CN1 ON ANT-RM BOARD
CN1 TO CN12 ON ANT-MT BOARD
CN6
TO J1 ON
ANT-MT BOARD
EQUITY Ⅲ+／EPSON PC AX
ANTA BOARD
UNIT NO. Y12620100002

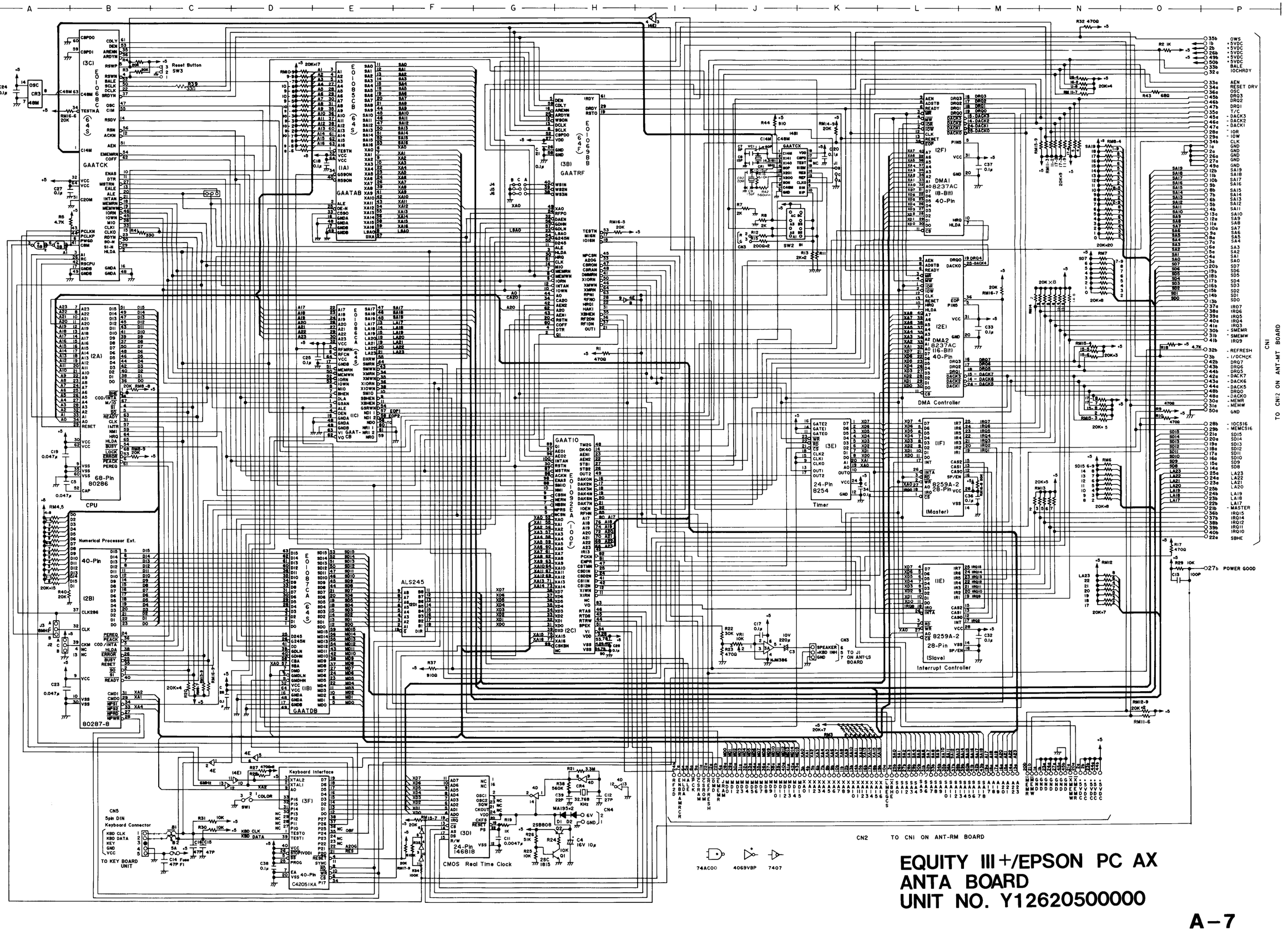


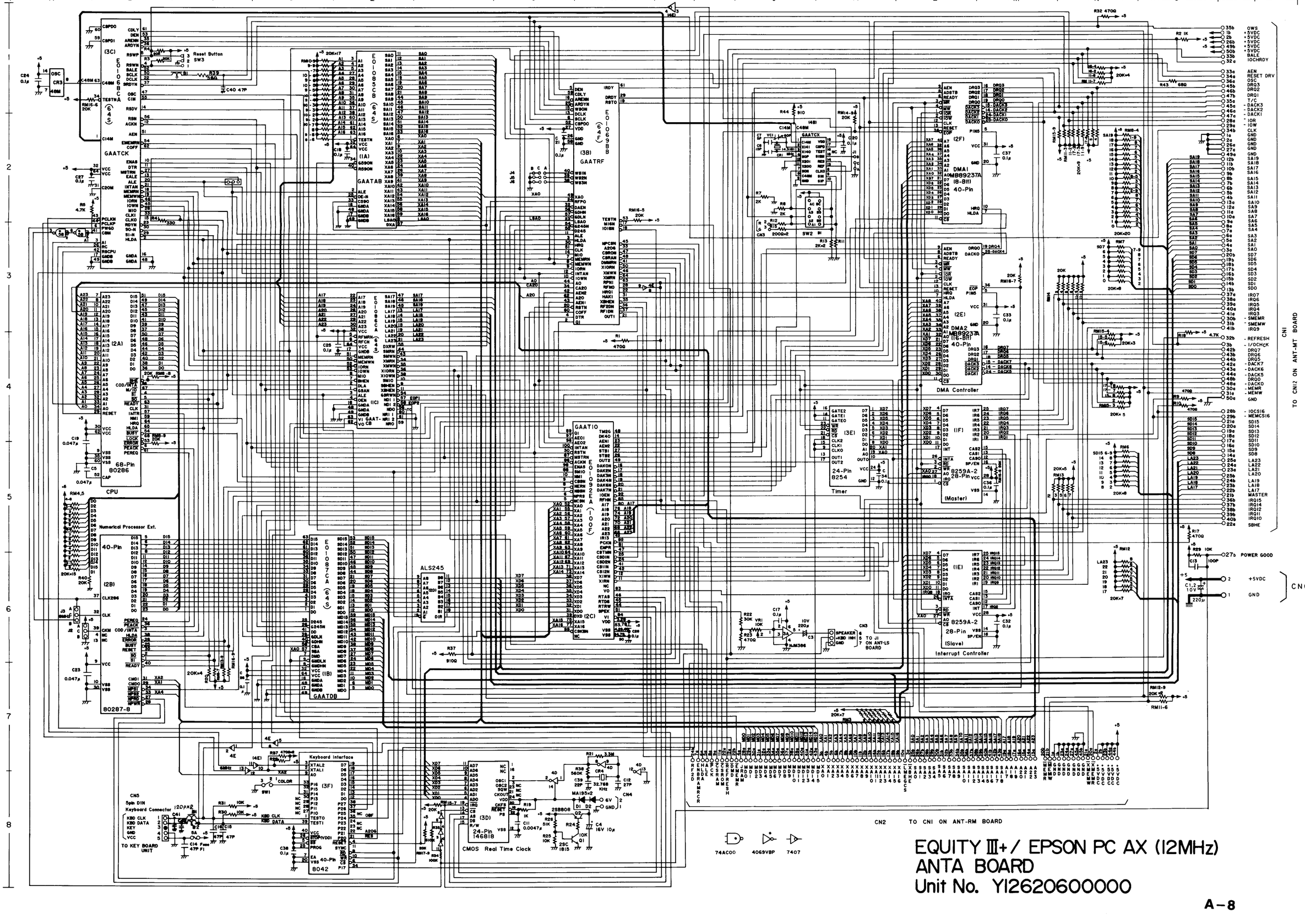
EQUITY III+/ EPSON PC AX
ANTA BOARD
UNIT NO. Y12620100002A


Slide SW
Reset Button SW3
14.31818MHz
20MHz
48MHz
E01068CA
GAATCK
GAATAB
GAATRF
GAATIO
GAATCB
GAATDB
E01069BB
E01087A
E01089CB
ALS245
3C
1A
2C
1C
2A
2B
1B
3B
2D
3D
1D
3F
CPU
80286-1
68-Pin
CAP
with socket
LCC
Numerical
Processor Ext.
DIP
80287-8
40-Pin
Socket
Keyboard Interface
8042
AH-0051NA
40-Pin
CN5
5pin DIN
Keyboard Connector
KBD CLK
KBD DATA
KEY
GND
VCC
TO
KEY BOARD
CMOS & Real
Time Clock
146818 VSS
24-Pin
TO BATTERY
MA195x2
2SB808
2SC1815
NJM386
SPEAKER
TO J1
ON ANT-LS
BOARD
DMA Controller
DMA1
8237A-5
(8-Bit)
40-Pin
DMA2
8237A-5
(16-Bit)
40-Pin
Timer
8254-2
24-Pin
Master
Interrupt Controller
Slave
8259A-2
28-Pin
1F
1E
2F
2E
3E
CN1
TO CN12 ON ANT-MT BOARD
CN6
TO J1 ON
ANT-MT BOARD
CN2 TO CN1 ON ANT-RM BOARD
74AC00 4069VBP 7407
(U)···· Internal Pull up
Pass Condensers ····· 0.1μF x 5
Address : C40 to C44
(not traced on above diagram)
EQUITY Ⅲ+／ EPSON PC AX
ANTA BOARD
UNIT NO. Y12620100003
A-5

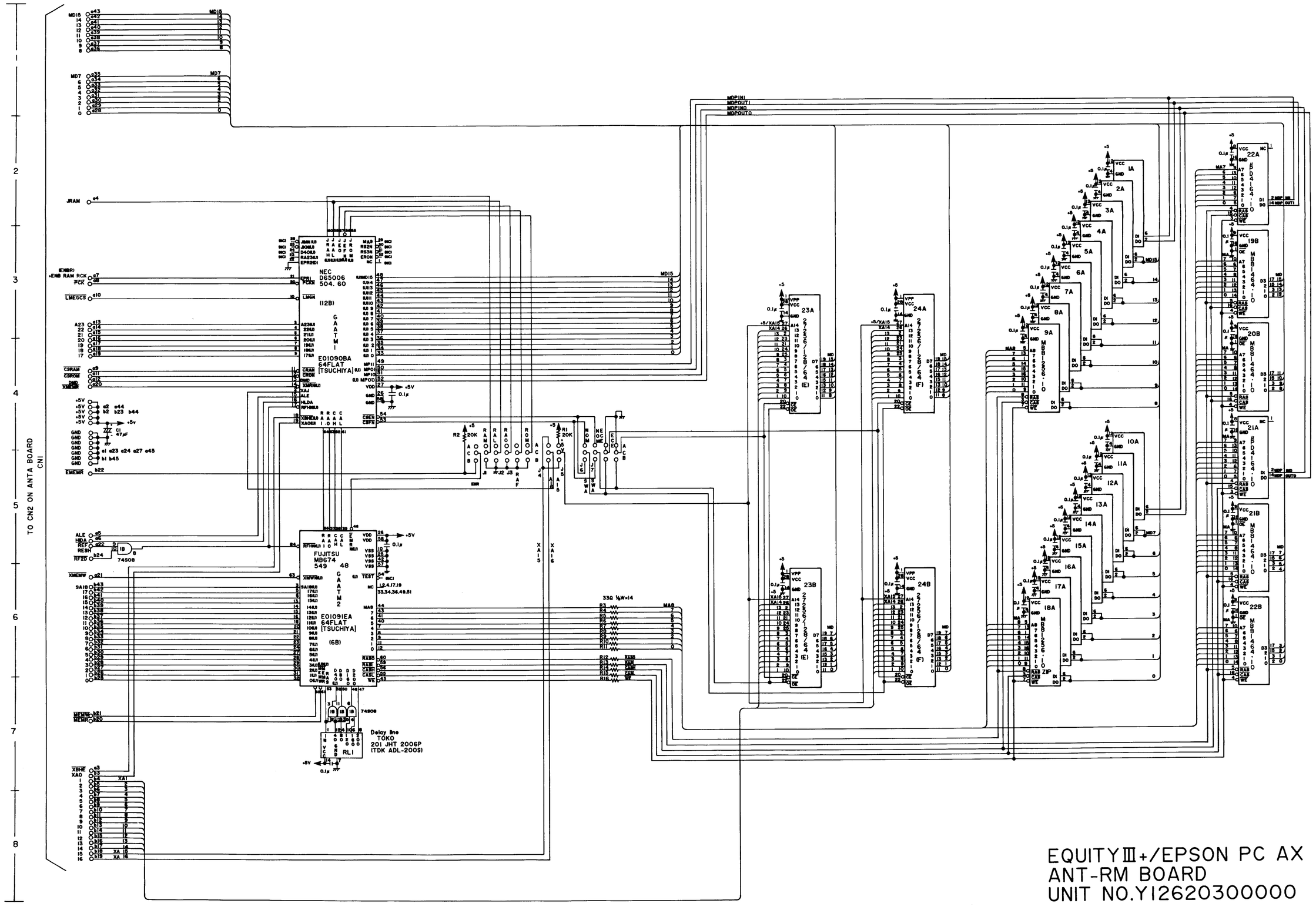


EQUITY III+/ EPSON PC AX
ANTA BOARD
UNIT NO. Y12620100004

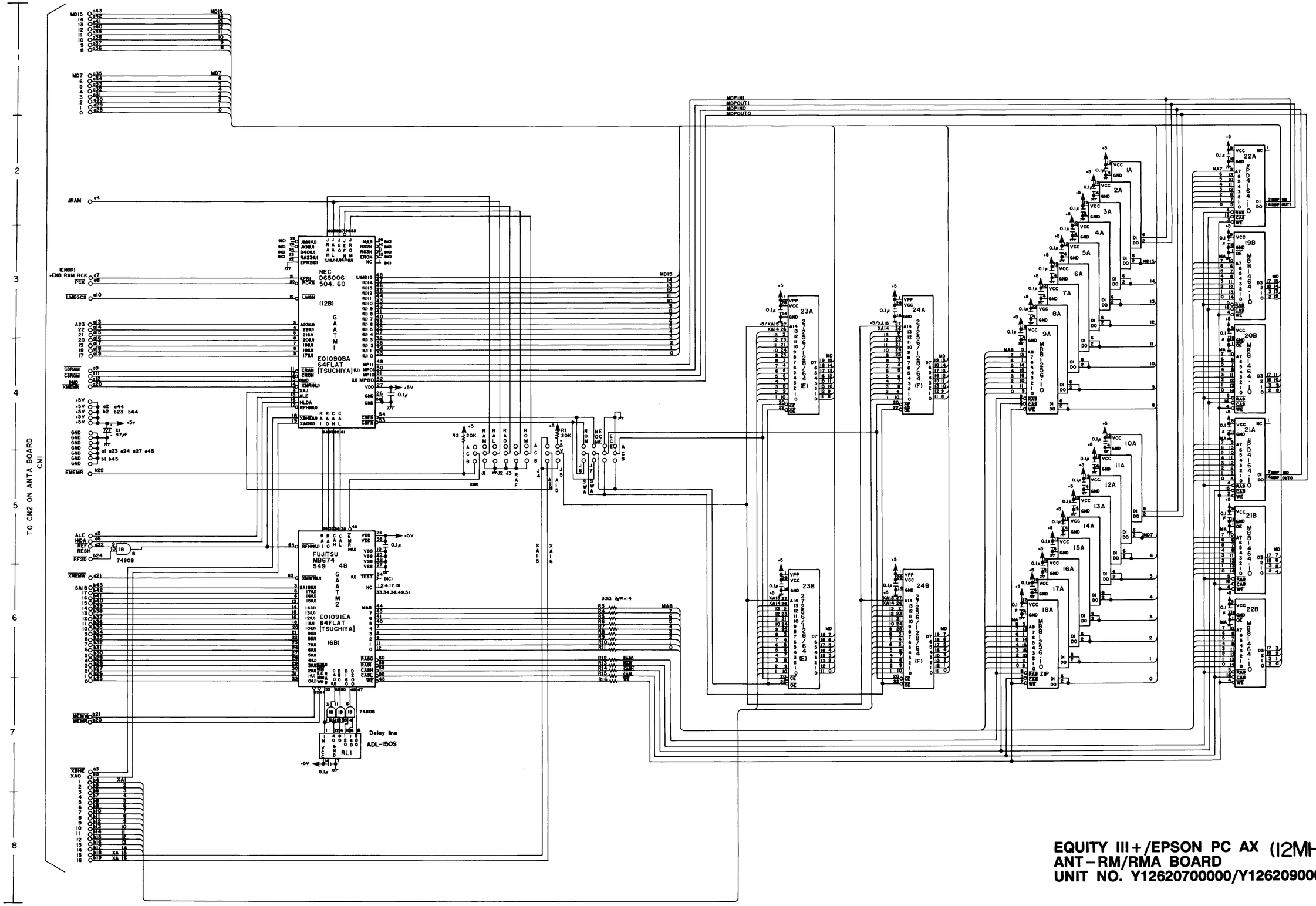

CPU
68-Pin
80286
80287-8
Numerical Processor Ext.
40-Pin
GAATCK
GAATAB
GAATRF
GAATDB
GAATIO
DMA Controller
8237AC
(8-Bit)
40-Pin
DMA1
DMA2
(16-Bit)
Timer
8254
24-Pin
8259A-2
28-Pin
Master
Slave
Interrupt Controller
Keyboard Interface
C42051KA P17
CMOS Real Time Clock
146818
Reset Button SW3
TO KEY BOARD UNIT
5pin DIN
Keyboard Connector
TO CN12 ON ANT-MT BOARD
CN2 TO CN1 ON ANT-RM BOARD
74ACOO
4069VBP
7407
EQUITY III+/EPSON PC AX
ANTA BOARD
UNIT NO. Y12620500000
A-7



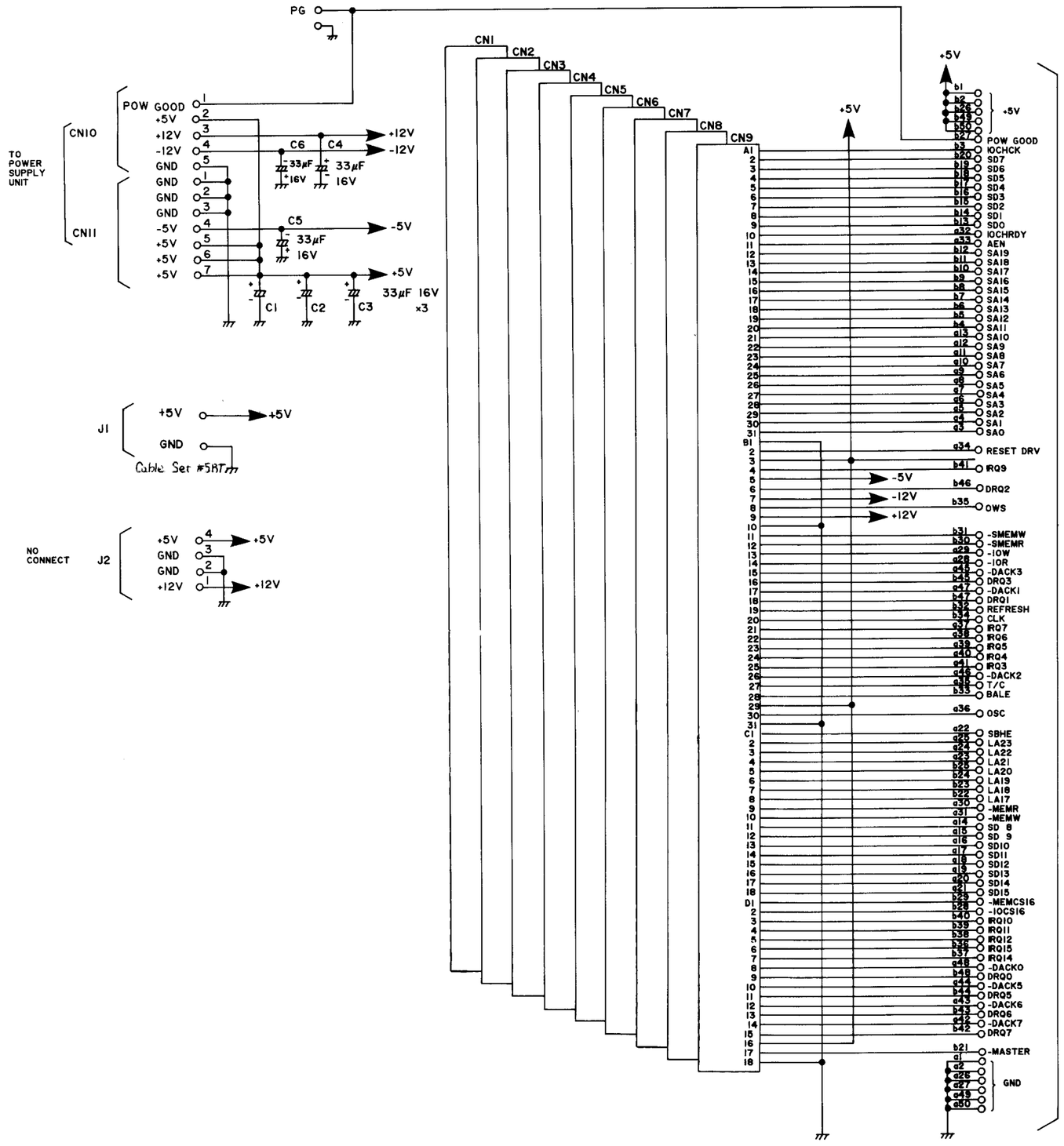
EQUITY III+ / EPSON PC AX (12MHz)
ANTA BOARD
Unit No. Y12620600000



EQUITY Ⅲ+/EPSON PC AX
ANT-RM BOARD
UNIT NO.Y1262030000



EQUITY III+/EPSON PC AX (12MHz)
ANT-RM/RMA BOARD
UNIT NO. Y12620700000/Y12620900000



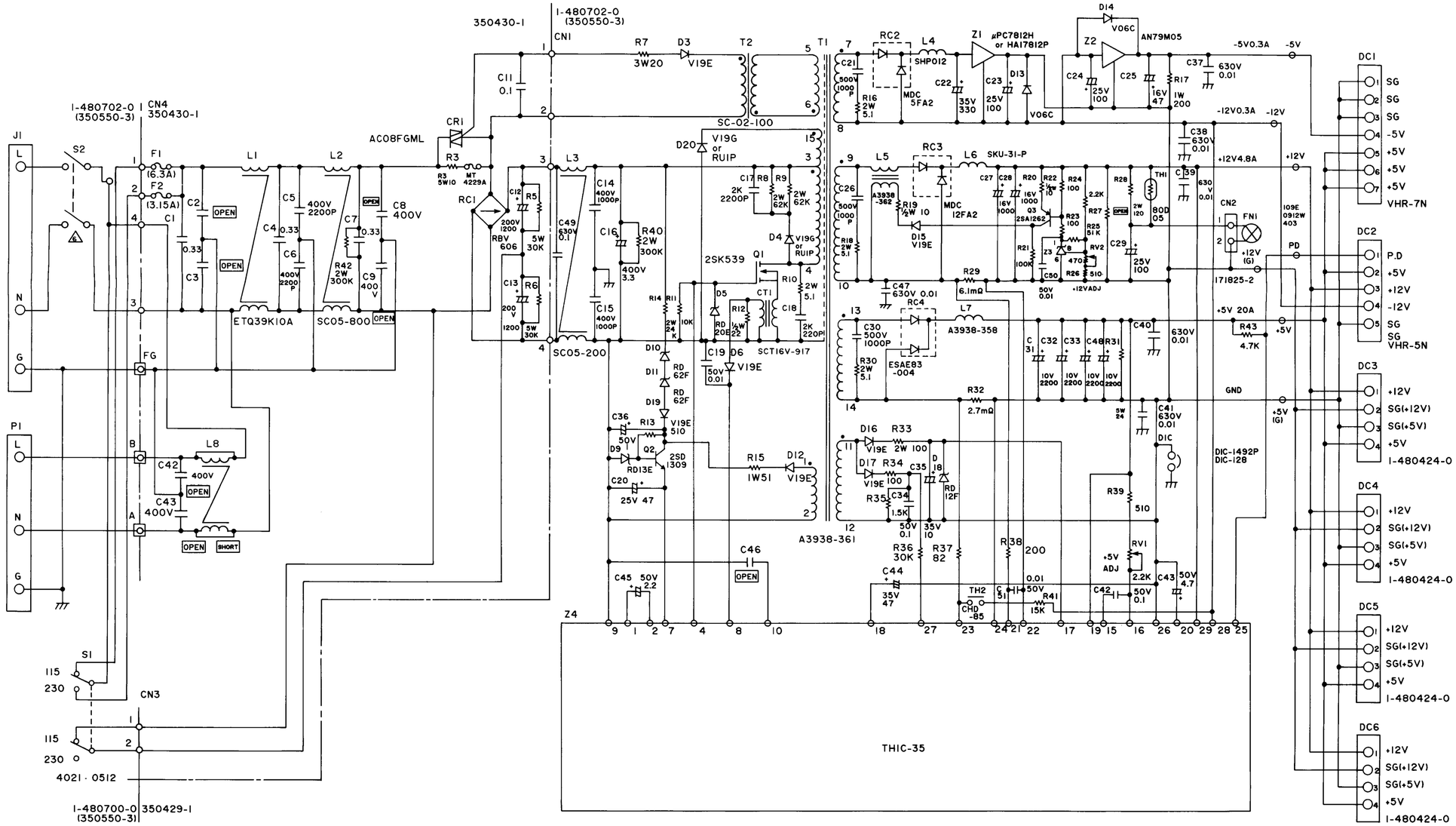
DESCRIPTIONS

Cable set #5BT is not installed on the Y12620200001.

Option slot locations

Unit Code	8 bit-bus connector	16 bit-bus connector
Y12620200000	CN1, CN7, CN8	CN2, CN3, CN4, CN5, CN6, CN9
Y12620200001	CN1, CN7, CN8	CN2, CN3, CN4, CN5, CN6, CN9
Y12620800000	CN1, CN7, CN9	CN2, CN3, CN4, CN5, CN6, CN8

EQUITY III+/EPSON PC AX
ANT-MT BOARD
UNIT NO. Y12620200000/Y12620200001/ Y12620800000



(CATHODE)
(Vref)
(ANODE)

(TH2)

(TH1)

(DIC)

OPEN

PRECISION ADJUSTABLE SHUNT REGULATOR

※When voltage of Vref pin becomes higher than fixed Voltage by external circuit, current will flow from CATHODE to ANODE. And flowing current becomes big in proportion to the Vref voltage.

※When temperature becomes higher than a fixed temperature, TH2 will be on.

※Value of resistor becomes low when temperature goes high proportionally.

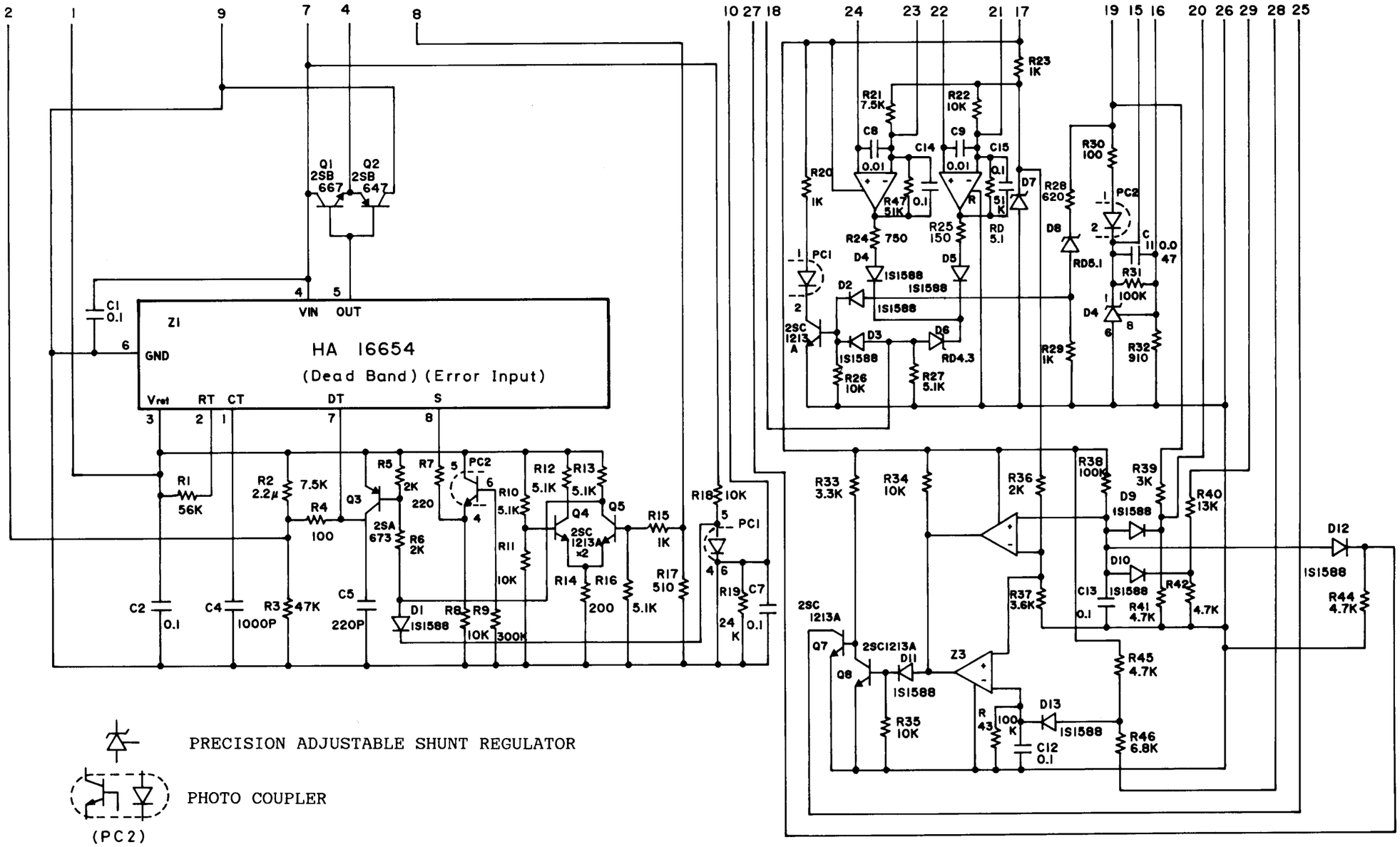
JUMPER CONNECTOR

※ In case of EQUITY Ⅲ+／EPSON PC AX, The DIC should be connected.

※"OPEN" means not installed.

EQUIY Ⅲ+/EPSON PC AX
ATRPS UNIT (Major Circuit)
UNIT NO. Y126501000/Y12650100001

NOTE : Y126501000 may not satisfy "TUV".

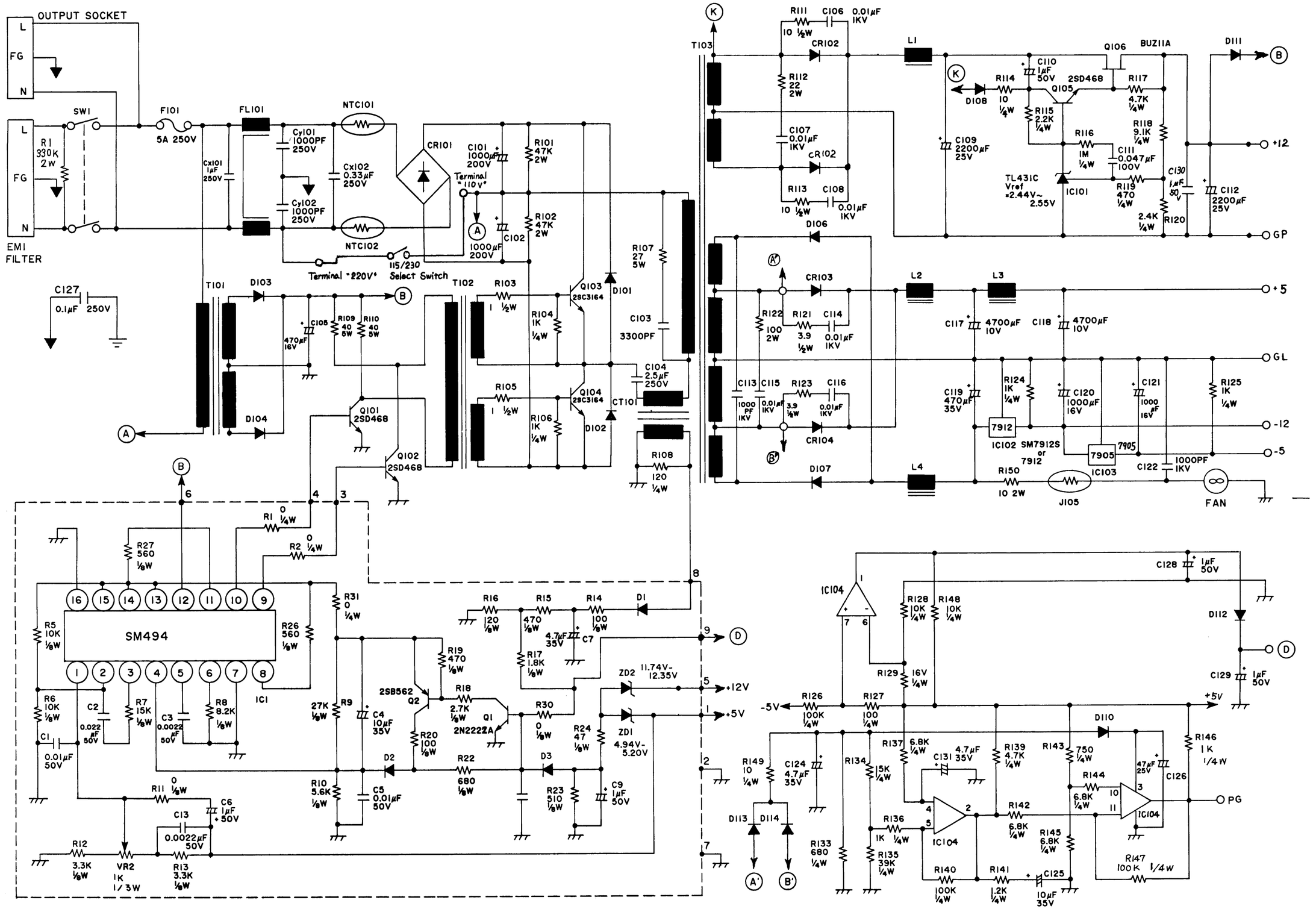


PRECISION ADJUSTABLE SHUNT REGULATOR

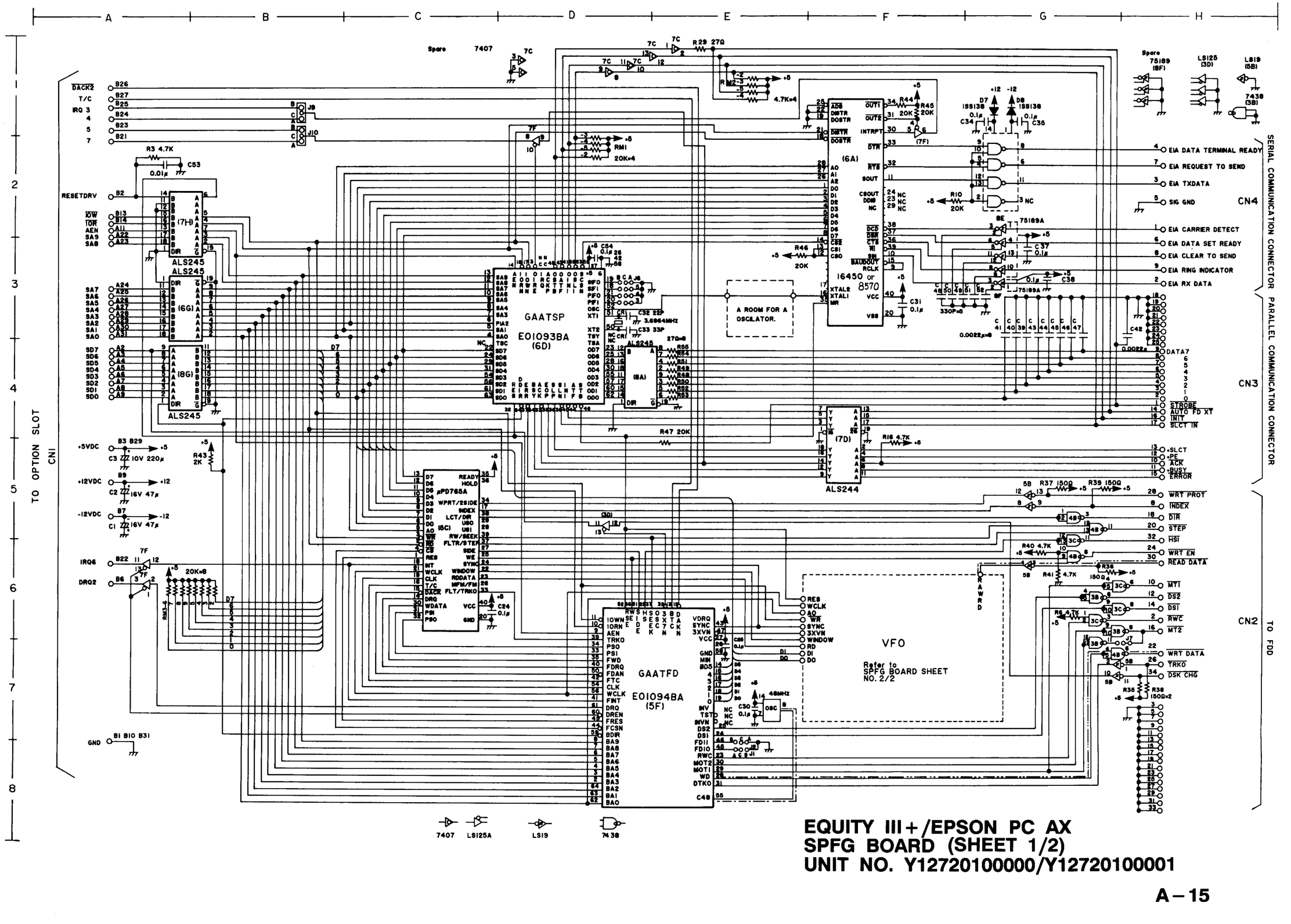
PHOTO COUPLER (PC2)

PHOTO SCR COUPLER (PC1)

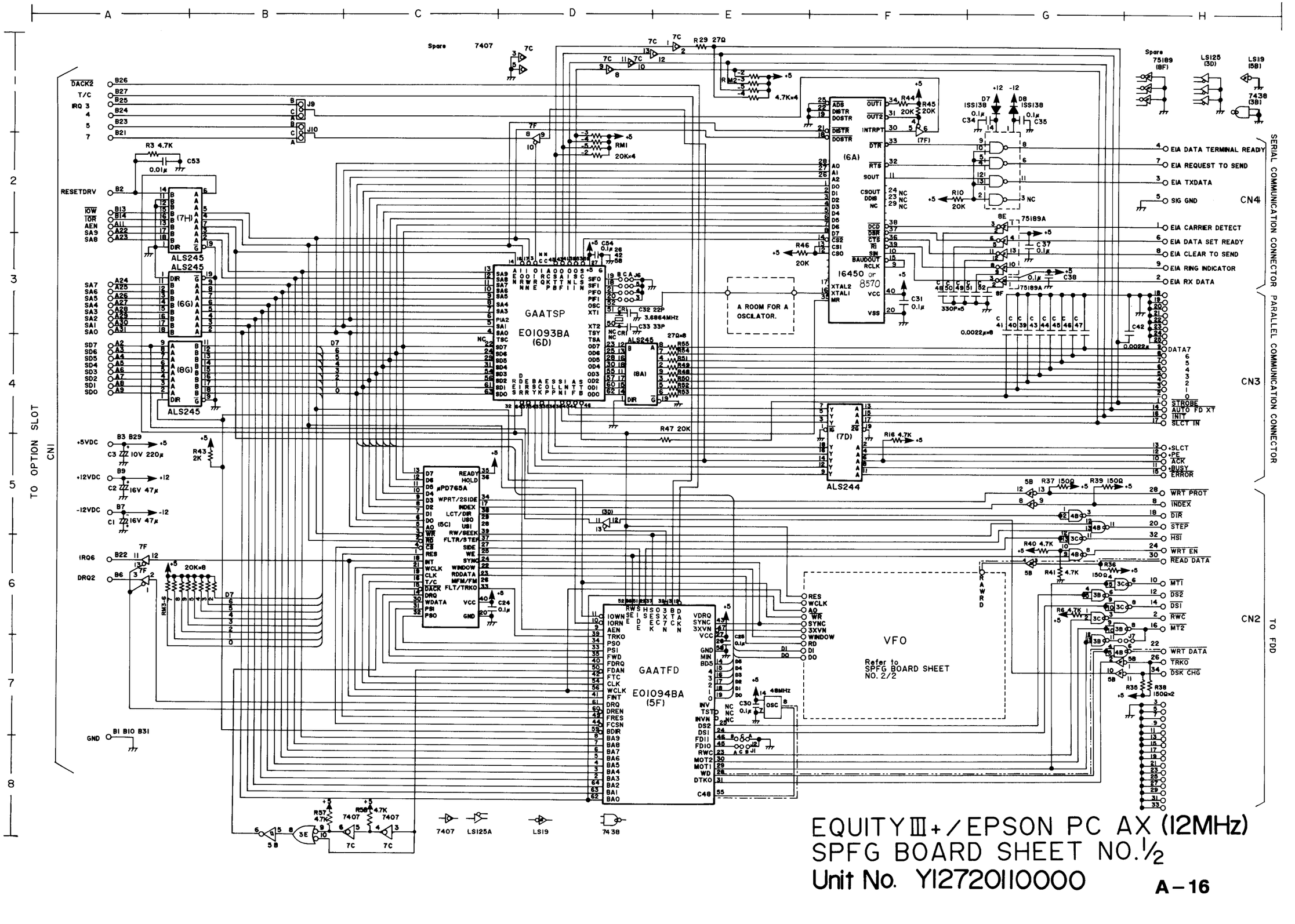
EQUIY III+/EPSON PC AX
ATRPS UNIT (THIC-35 BOARD)
UNIT NO. Y126501000/Y12650100001



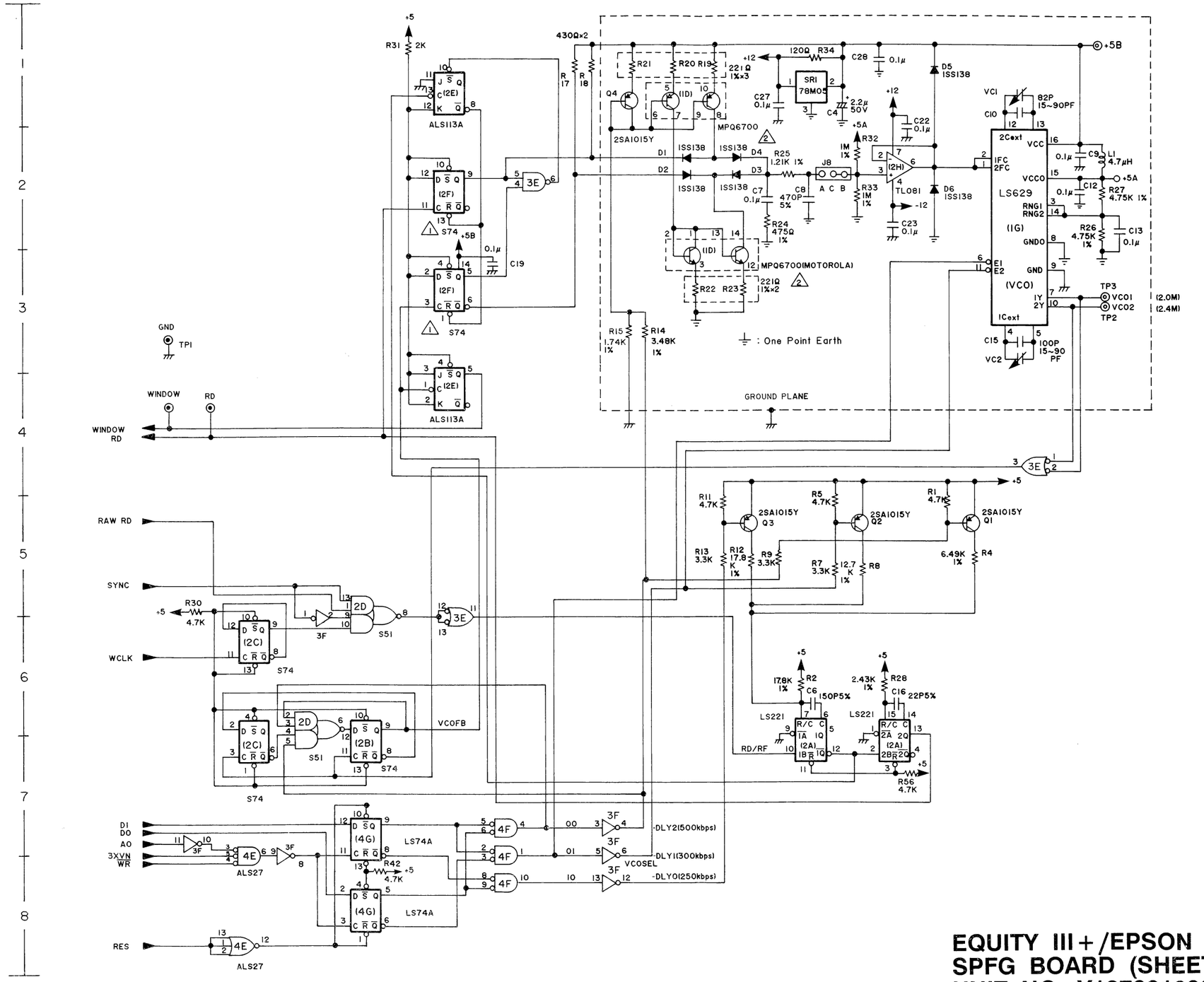
EQUITY III+/EPSON PC AX
ANPS UNIT (ALTERNATE POWER SUPPLY)
UNIT NO. Y126509000



EQUITY III+/EPSON PC AX
SPFG BOARD (SHEET 1/2)
UNIT NO. Y12720100000/Y12720100001



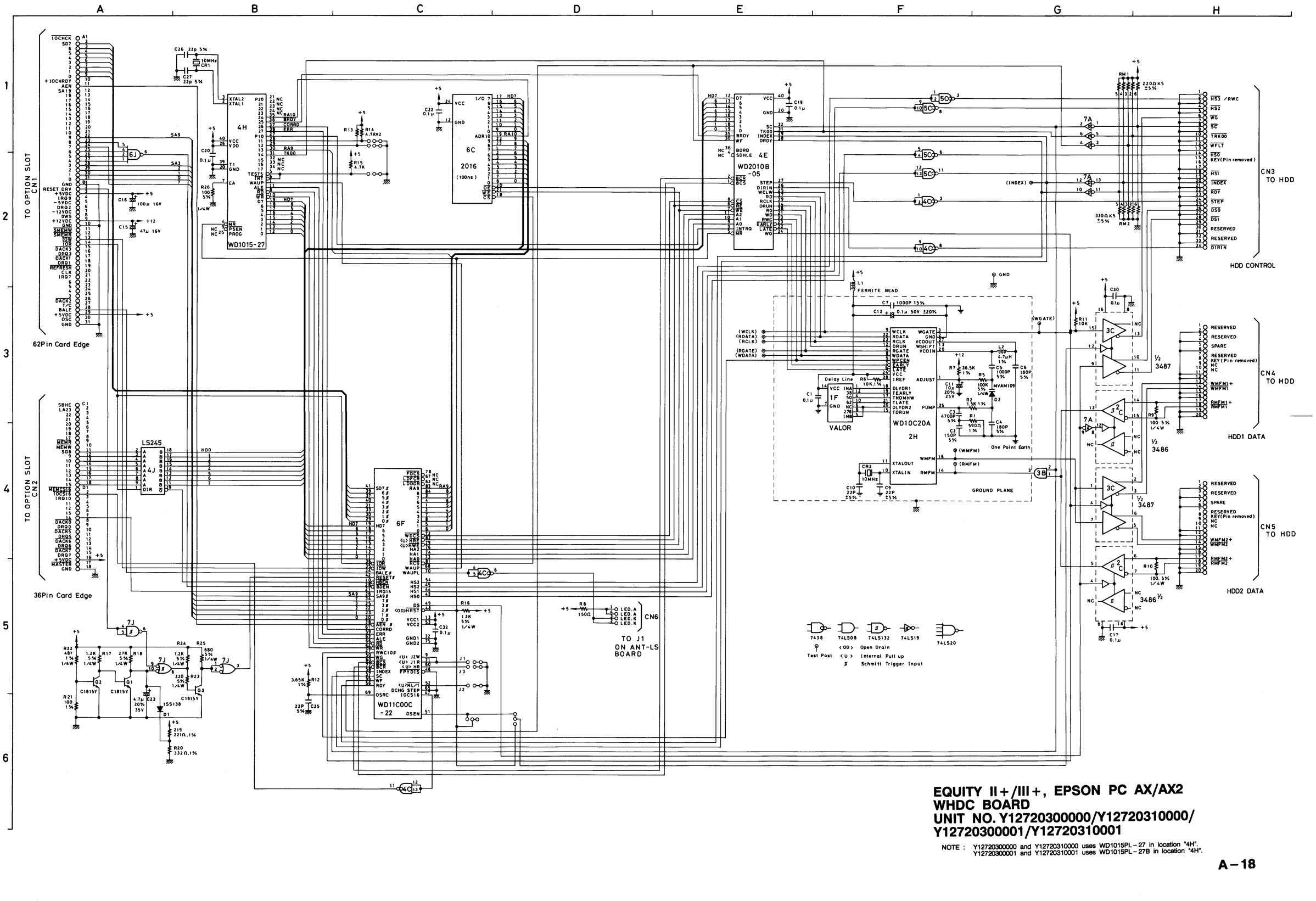
EQUITY III+ / EPSON PC AX (12MHz)
SPFG BOARD SHEET NO. 1/2
Unit No. Y12720110000



1 Both 74S74s are in the same package.

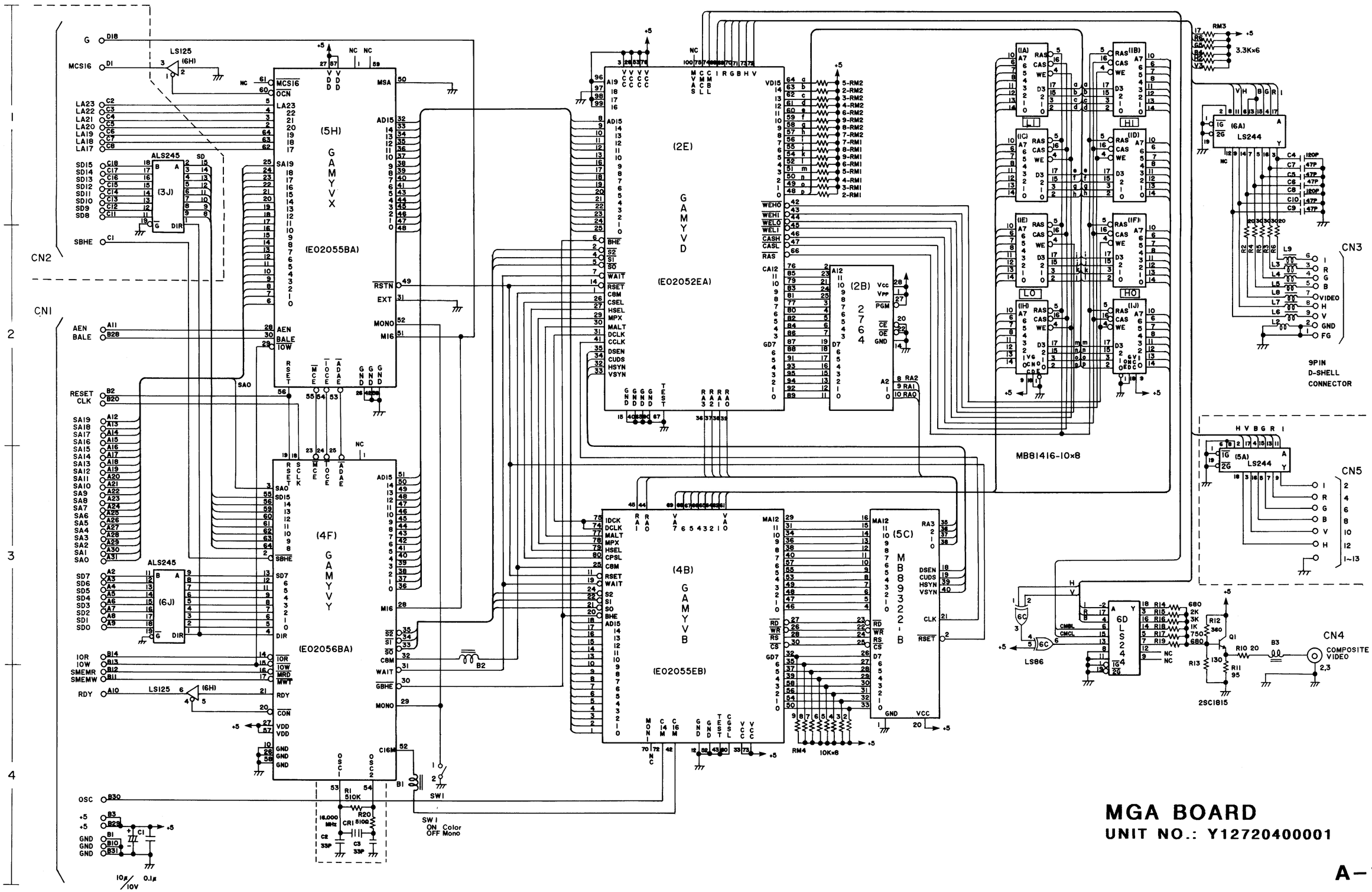
2 The MPQ6700 is a quad PNP/NPN complementary pair transistor.

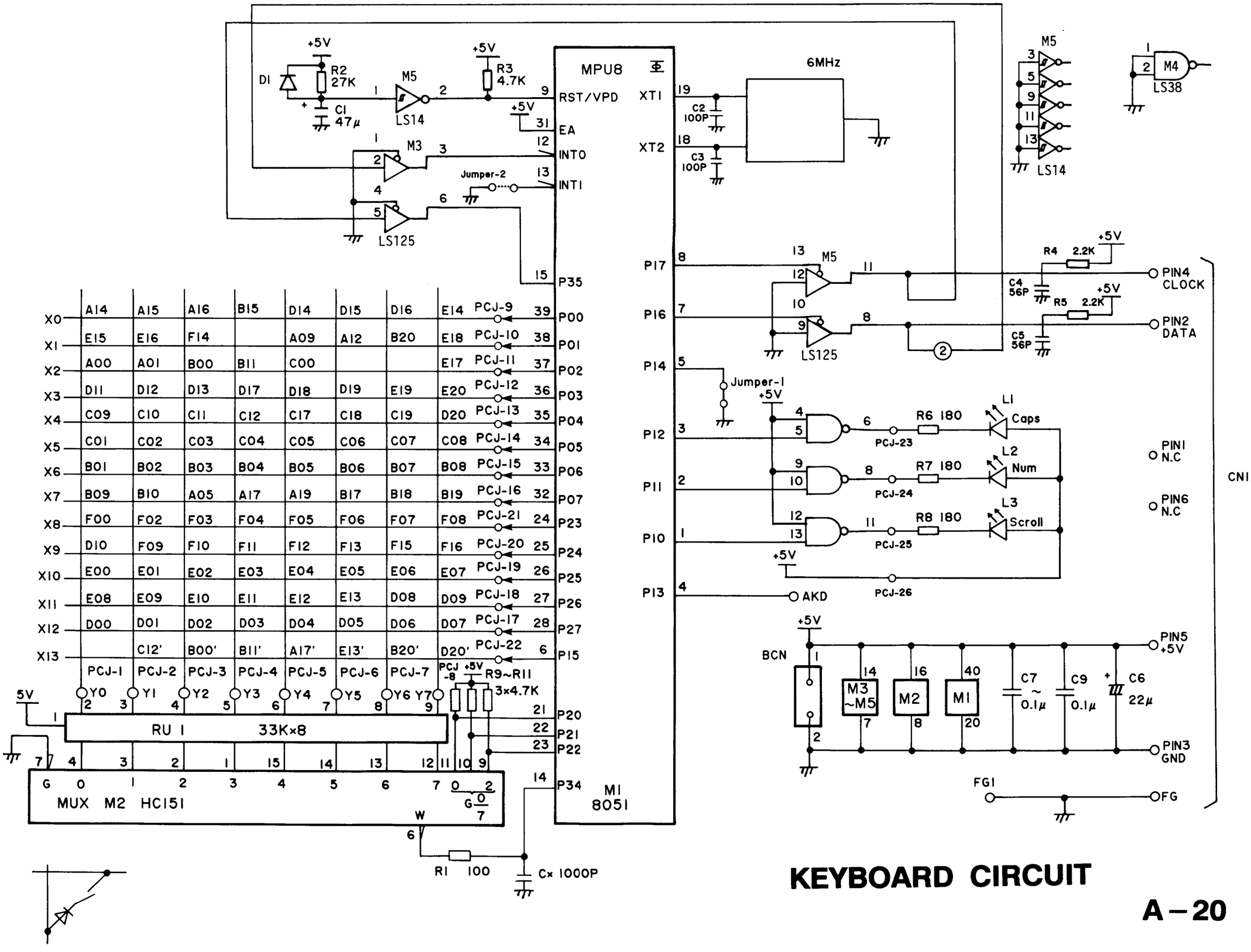
EQUITY III+/EPSON PC AX
SPFG BOARD (SHEET 2/2)
UNIT NO. Y12720100000/Y12720100001/ Y12720110000



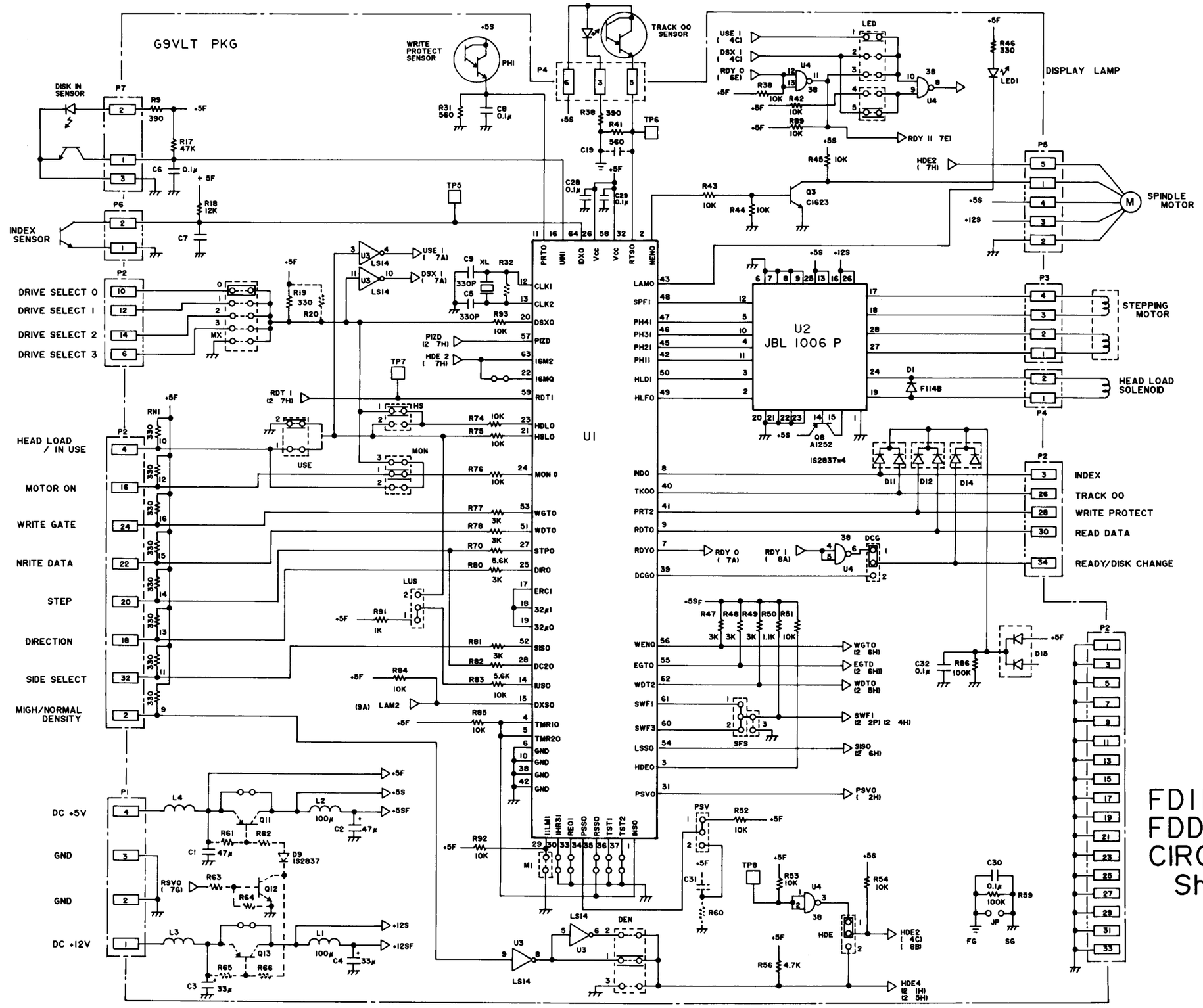
EQUITY II+/III+, EPSON PC AX/AX2
WHDC BOARD
UNIT NO. Y12720300000/Y12720310000/
Y12720300001/Y12720310001

NOTE : Y12720300000 and Y12720310000 uses WD1015PL-27 in location "4H".
Y12720300001 and Y12720310001 uses WD1015PL-27B in location "4H".

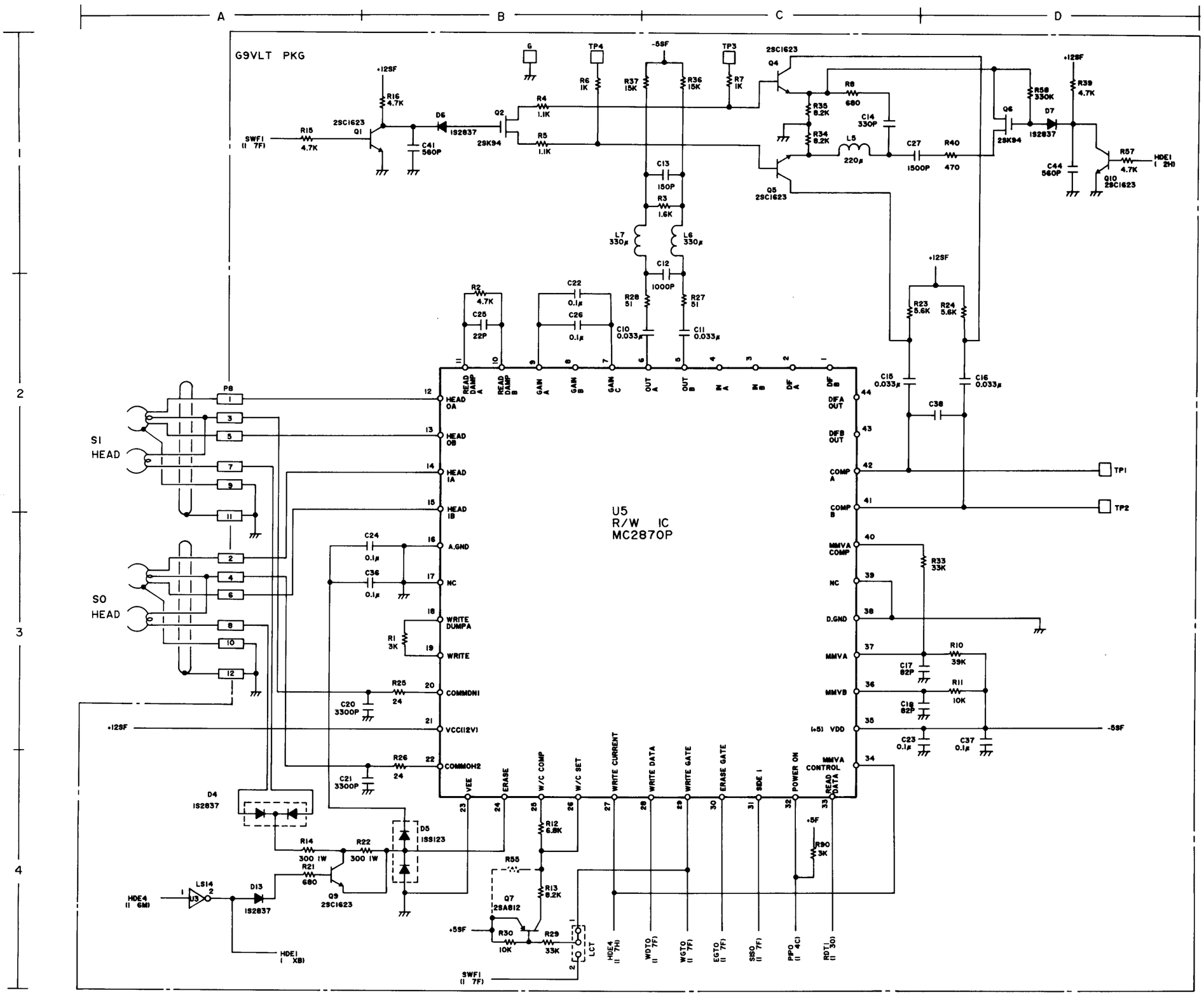

A
B
C
D
2
3
4
CN1
CN2
CN3
CN4
CN5
(5H)
GAMYVX
(E02055BA)
(2E)
GAMYD
(E02052EA)
(4F)
GAMYVY
(E02056BA)
(4B)
GAMYVB
(E02055EB)
(2B)
2764
(5C)
MB89322-B
(3J)
ALS245
(6J)
ALS245
(6H)
LS125
(6H)
LS125
(6A)
LS244
(5A)
LS244
6C
LS86
6D
LS244
MB81416-10x8
RM3
3.3K×6
RM4
10K×8
9PIN
D-SHELL
CONNECTOR
COMPOSITE
VIDEO
2SC1815
Q1
SW1
ON Color
OFF Mono
16.000
MHz
MGA BOARD
UNIT NO.: Y12720400001
A-19



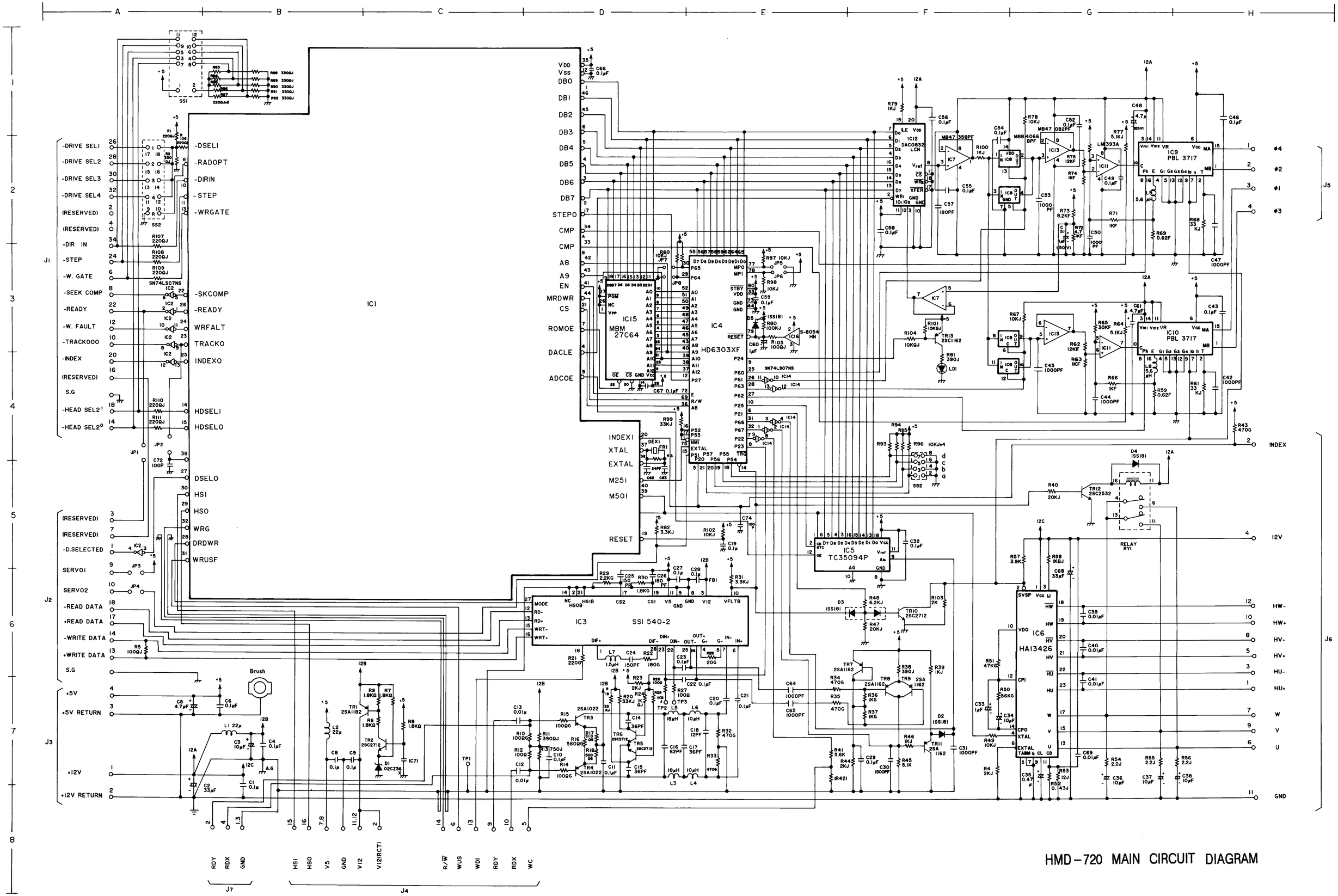
KEYBOARD CIRCUIT



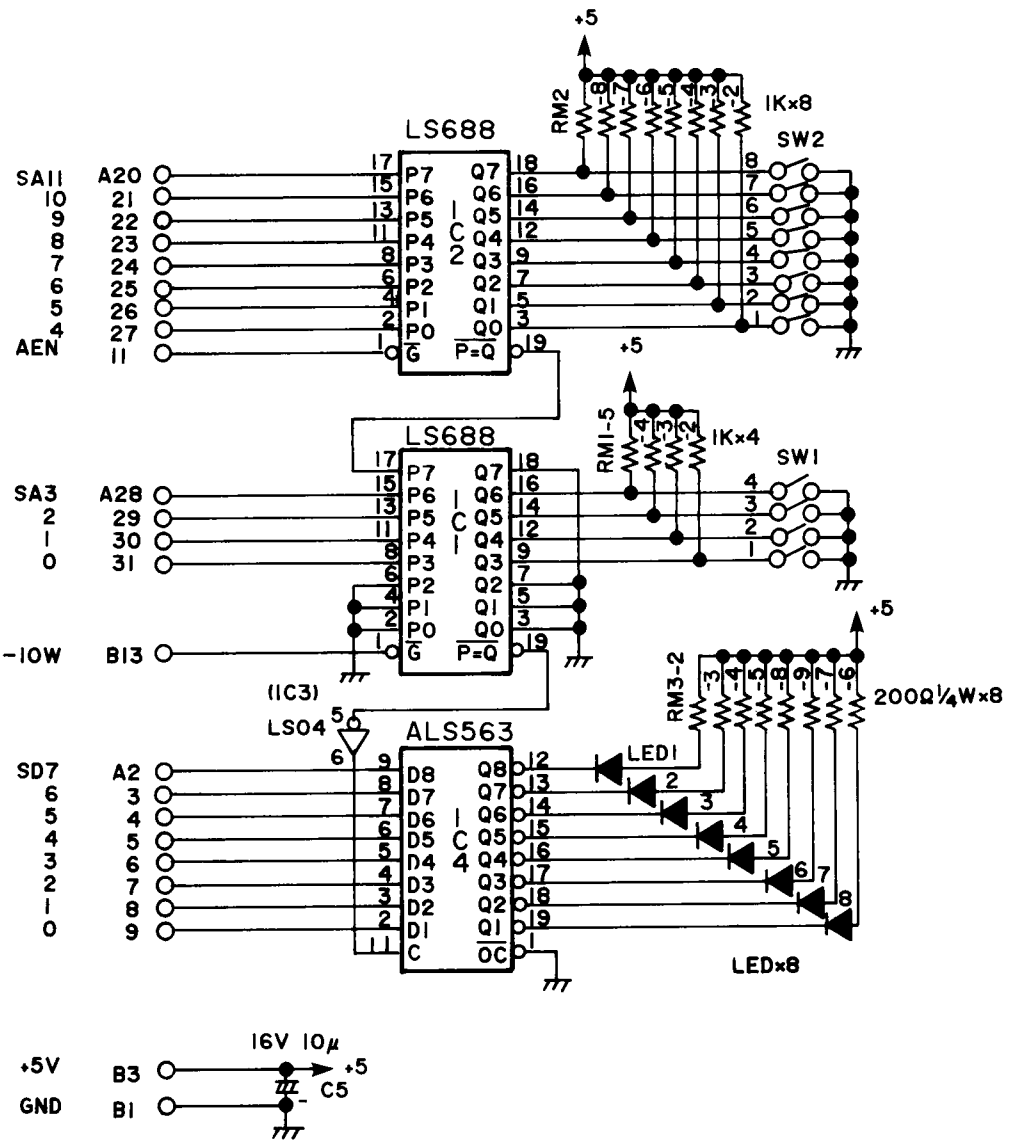
FD1155C (1.2MB FDD UNIT) CIRCUIT DIAGRAM Sheet 1/2



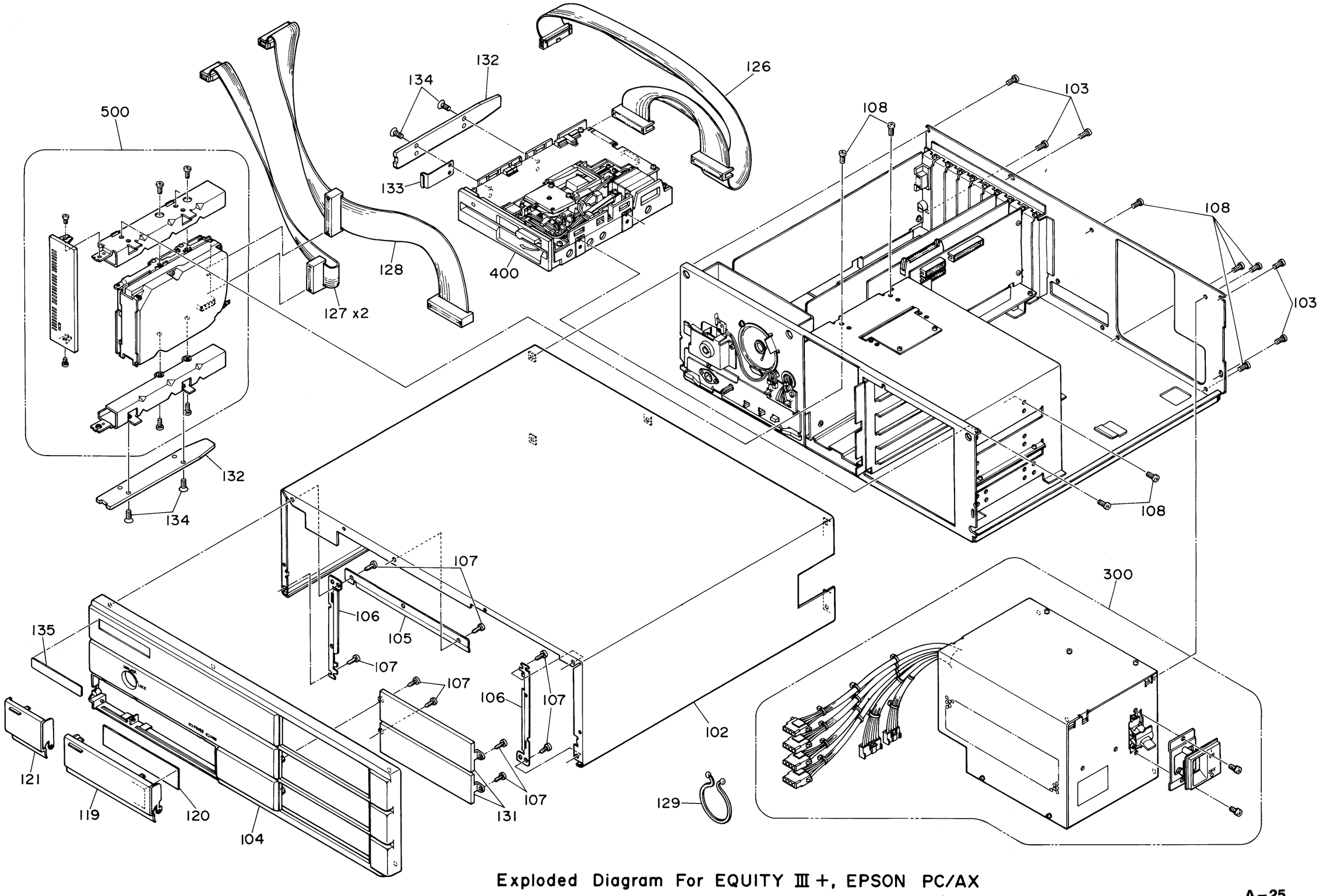
FD1155C
(1.2MB FDD UNIT)
CIRCUIT DIAGRAM
Sheet 2/2



HMD-720 MAIN CIRCUIT DIAGRAM

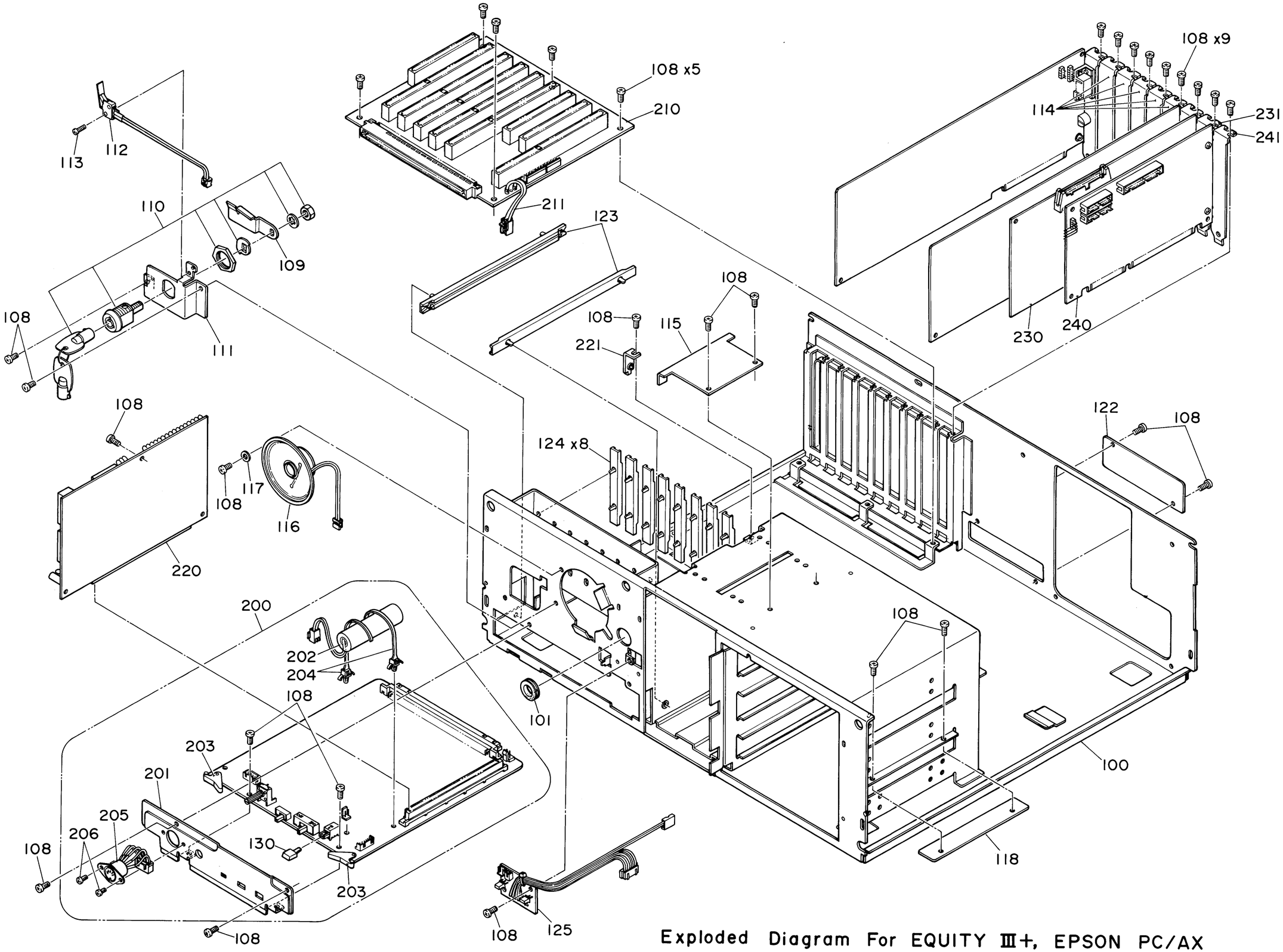

+5
RM2
IK×8
SW2
LS688
IC2
SA11 A20
10 21
9 22
8 23
7 24
6 25
5 26
4 27
AEN 11
P7 P6 P5 P4 P3 P2 P1 P0 G
Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0 P=Q
+5
RM1-5
IK×4
SW1
LS688
IC1
SA3 A28
2 29
1 30
0 31
-IOW B13
(IC3)
LS04
ALS563
IC4
SD7 A2
6 3
5 4
4 5
3 6
2 7
1 8
0 9
D8 D7 D6 D5 D4 D3 D2 D1 C
Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 OC
+5
RM3-2
200Ω1/4W×8
LED1
LED×8
16V 10μ
+5V B3
GND B1
+5
C5

MFG BOARD



Exploded Diagram For EQUITY III+, EPSON PC/AX

(2/2)



Exploded Diagram For EQUITY III+, EPSON PC/AX

(1/2)

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