

TC11  
(TM11/TU10 COMPATIBLE)  
TAPE CONTROLLER  
TECHNICAL MANUAL



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TC1151002 Rev F  
October, 1982

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Printed in U.S.A.

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## 1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the TC11 tape controller. In addition, this manual provides diagnostics and application information.

## 1.2 OVERVIEW

The TC11 Magnetic Tape Controller emulates the Digital Equipment Corporation TM11 tape controller and interfaces all tape transports having the industry standard (Pertec) interface. It is intended to be used with the PDP-11 and VAX-11/750/780 computers. The controller is software compatible with the TM11 and will read and write DEC or IBM compatible 9-track PE (1600 bpi), and 9-track NRZI (800 bpi) formats at industry standard tape drive speeds from 12.5 to 125 ips. A maximum of four tape transports may be attached to the controller with any mix of 9-track NRZI, PE or dual density. The controller accommodates two different transport speeds.

## 1.3 PHYSICAL CHARACTERISTICS

The basic TC11 is constructed on a single hex-size board which plugs directly into any PDP-11 or VAX-11 SPC slot. This single hex board provides for NRZI tape operations. For phase encoded operation, a quad size PE Read Board is added. This board converts the phase encoded read data into NRZI data for the controller. Two 40-wire flat cables, one for control and one for data, connect the controller and PE Read Board to the first tape transport. Both boards draw power from the CPU backplane.

## 1.4 FEATURES

### 1.4.1 Microprocessor Architecture

The TC11 design incorporates a high-speed 16-bit microprocessor to perform most of the functions of the controller. The controller's microprogramming provides the software compatibility and emulation of the TM11. In addition, the microprocessor design approach allows for extensive self-test of the controller and PE Read Board.

### 1.4.2 Phase Encoded Operation

The DEC TM11 tape controller does not handle 1600 bpi PE operation. The TC11 controller provides for PE operation in a manner which is compatible with the TM11 and all DEC software including diagnostics. The controller even generates CRC and LRC, which are not used in the PE format, so as to satisfy the NRZI diagnostics. The bad track information is placed in the MTRD at the end of each record rather than the LRC error. PE operation is normally enabled

by the high density switch at the tape transport. The controller will conform to the mode of the transport. The controller can also be programmed for 1600 bpi. Since standard software will select 800 bpi, the selection of 1600 bpi at the transport will force PE operation.

#### 1.4.3 Self-Test

The controller incorporates an extensive self-test capability for itself and the PE Read Board. The self-test is executed every time the controller is powered on. It does not execute self-test with a bus INIT. The LED on the top of the board is turned on when the controller is cleared and is turned off if the controller gets past the self-test. If the controller does not properly execute the self-test, the LED remains on and the controller cannot be addressed from the CPU. The controller also executes an extensive self-test of the PE Read Board consisting of the generation of short PE records with various data patterns and dead tracks. The controller checks the response from the PE Read Board and leaves the LED on if an error is detected. The PE self-test can be initiated with various options by writing into the Maintenance Register. (See Sections 3.1.7 and 3.3)

#### 1.4.4 Efficient DMA

The controller incorporates eight bytes of data buffering and it transfers data to or from memory on a word basis, except for odd bytes at the start or end of the record.

### 1.5 OPERATING SYSTEMS

#### 1.5.1 PDP-11 Operating Systems

The PDP-11 operating system supports the TM11 and consequently, also supports the TC11. The TC11 emulates the TM11 with no modification to the software.

#### 1.5.2 VAX Operating Systems

The VAX VMS Operating System does not support the TM11 and therefore it does not support the TC11. Emulex provides a VMS software driver, however, to allow the TC11 to be used on both the VAX-11 750 and 780. The Emulex part numbers are VD9960401 (750) and VD9960501 (780). The software is supplied with its own operation and installation manual.

### 1.6 DIAGNOSTICS

#### 1.6.1 VAX Diagnostics

DEC does not support the TM11 on the VAX line of computers and consequently there are no DEC diagnostics. Emulex provides diagnostics for the support of the TC11. The part numbers for the



Emulex diagnostics are VX9960401 (750) and VX9960501 (780). See the literature supplied with the diagnostic for installation and operation instructions.

### 1.6.2 PDP-11 Diagnostics

Because the PDP-11 supports the TM11, the DEC diagnostics will run on the TM11 with only minor patches. The TC11 controller executes the following DEC TM11/TU10 diagnostics in both NRZI and PE modes:

ZTMA	-	Instruction Test *
ZTMH	-	Multidrive Data Reliability Exercise
ZTME	-	Drive Function Timer *
ZTMG	-	Utility Driver
ZTMD	-	Data Reliability 9 Track

\*Requires minor patch

Table 1-1  
General Specifications

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<b>FUNCTIONAL</b>		
Recording Standards	IBM, ANSI, and DEC	
Number of Tracks	9	
Recording Method and Density	9-track NRZI, 800 bpi 9-track PE, 1600 bpi	
Number of Tape Units	4	
Number of Tape speeds	2	
Tape Speeds	125, 75, 45, 37.5, 18.75, 25, 15, 12.5 inches/second (ips)	
Controller Commands	Off-Line, Read, Write, Write EOF, Space Forward, Space Reverse, Write with Extended IRG and Rewind	
 <b>UNIBUS INTERFACE</b>		
Register Address		
-01 (Standard)	Status (MTS)	772520
	Command (MTC)	772522
	Byte/Record Count	772524
	Current Memory Address	772526
	Data Buffer (MTD)	772530
	Read Lines (MTRD)	772532
	Maintenance (MTM)	772534
-02 (Alternate)	Status (MTS)	772460
	Command (MTC)	772462
	Byte/Record Count	772464
	Current Memory Address	772466
	Data Buffer (MTD)	772470
	Read Lines (MTRD)	772472
	Maintenance (MTM)	772474
Interrupt Vector Address		
Standard	224	
Alternates	330, 370, 374	
Interrupt Priority Level	BR5	
Data Transfer	Direct Memory Access (DMA) with word (16-bit) transfer, except for odd byte at beginning or at end of record.	

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Table 1-1 (Cont'd)

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 PHYSICAL

Number of Boards	NRZI - one hex size board PE - one hex size board and one quad size board
Mounting	Any two SPC slots in standard DEC system unit.
Cables	One 40-wire flat cable for control and one 40-wire flat cable for data.

ELECTRICAL

Power	NRZI: +5V, 6 amps. (one board) PE: +5V, 8 amps. (two boards)
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ENVIRONMENTAL

Operating Temperature	0oC to +55oC
Storage Temperature	-10oC to +70oC
Humidity	10 to 90% without condensation

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**BLANK**

## 2.1 PHYSICAL DESCRIPTION

The TC11 Tape Controller is constructed on a single hex-size printed circuit board. This board contains all circuitry required for handling tape transports using NRZI formats up to 800 bits per inch. For transports using 1600 bpi (phase encoded) formats, an additional quad size board is required to decode the PE read signals from the tape and convert them to NRZI signals which can be handled by the controller board. The controller board and PE Read Board are interconnected by means of a 40-conductor flat ribbon cable when used together in a system.

### 2.1.1 TC11 Controller Board

The TC11 Tape Controller board is designated Part No. TC1110401. This board contains the interface circuitry to both the CPU, via the Unibus, and to the tape drives attached to the controller, plus all other circuitry required for tape control and data transfer operations, except for reading phase encoded signals from the tape.

The TC11 controller board is shown in Figure 2-1. The board is a 4-layer PCB with power and ground planes on the inner layers and etch interconnects on the outer layers. The board dimensions are 8.7 inches high by 15.69 inches wide, corresponding to the DEC hex height board. The board contains extractors which interface mechanically with the board insertion/extraction facilities contained in DEC standard Unibus chassis and expansion boxes. These handles are used for convenience in inserting and extracting the controller and also act as a card retention mechanism when the controller is installed.

Although overall hex height, the board interfaces only to connector rows C, D, E, and F. The 18 pins of each connector row are designated A through V - excluding the letters G, I, O, and Q - from right to left; the top side pins are designated "1" and the bottom side pins are designated "2".

#### 2.1.1.1 Connectors

The tape transport interface is made via two 40-pin connectors J1 and J2 at the top edge of the board. For NRZI only, cables are routed directly to the tape transport. For PE operation, the connector J1 cable is connected to the PE Read Board.

There are two additional male connectors located on the board, designated J3 and J4. These are used for connecting a special test panel used for factory test and repair operations and are not intended for use in normal controller operations.

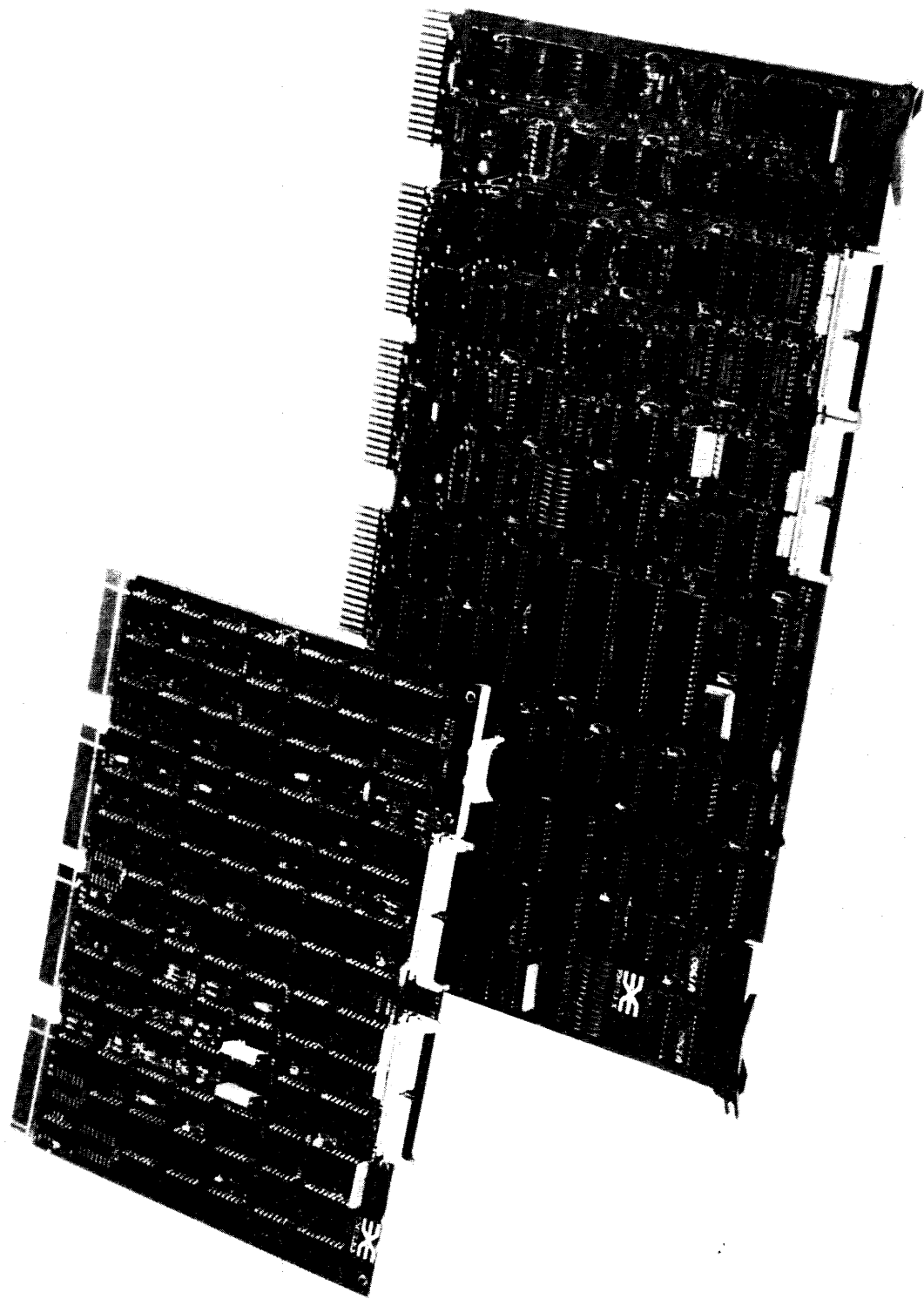


Figure 2-1 TC11 Controller and PE Read Board

### 2.1.1.2 Switches

The two DIP switches, SW1 and SW2 are for tape speed selection and controller options respectively.

### 2.1.1.3 Wire-Wrap Jumpers

There is a group of wire wrap jumper pins that are used to ground certain return lines when the PE Read Board is not present. These same data cable wires are used to pass certain control to the PE Read Board when it is in use.

### 2.1.1.4 Indicators

The LED located to the right of the two connectors is both a controller fault and an activity indicator. It will flash during data transfer operations.

## 2.1.2 PE Read Board

The PE Read board is designated Part No. TU1110402 or TU1110406. The TU1110402 design sets speed by changing capacitors and adjusting pots. The TU1110406 design sets speed by switch selection. See 4.4.2 and 4.4.3 for information on speed selection. The PE Read board contains the phase decode circuitry required for read back of PE signals from the tapes. The board is also used with the TC01 Tape Controller for the LSI-11.

The PE Read Board is shown in Figure 2-1. The board is a 4-layer PCB with power and ground planes on the inner layers and etch interconnects on the outer layers. The board dimensions are 8.7 inches wide by 10.44 inches high, corresponding to the DEC quad size board.

The board plugs into the four backplane connectors corresponding to connector rows C, D, E, and F. The 18 pins of each connector row are designated A through V - excluding the letters G, I, O, and Q - from right to left; the top side pins are designated "1" and the bottom side pins are designated "2". This board uses only the standard power and ground pins defined for these connectors, and no functional interface is made to the Unibus except for the bus grant signals which are jumpered.

Although the PE Read Board does not interface to the Unibus, it does occupy an SPC slot, and therefore, provision is made to jumper through the four bus grant signals to insure continuity to succeeding devices. These jumpers are made via Bus Grant Jumpers M-N, O-P, Q-R, and S-T. Jumpers I-J, K-L, U-V, and W-X are used for bus grant continuity when installed in an LSI-11 backplane. These connections are installed at the factory.

### 2.1.2.1 Connectors

The board has two 40-pin connectors located for interfaces to the TC11 Controller and to the tape transport. The board interfaces to the controller board via connector J1 and to the tape transport via connector J2; both are located at the top of the board. The board is equipped with handles for easy insertion and removal, as well as for maintaining spacing between adjacent boards.

### 2.1.2.2 Switches

The PE Read Board contains two rotary selector switches for setting the primary and secondary speeds. Section 4.4.1 describes the settings.

### 2.1.2.3 Indicators

The LED on the board indicates that the PE Read Board is in self-test, or that there is a fault in the board detected by the self-test.

## 2.2 ORGANIZATION

### 2.2.1 Controller Board

A block diagram showing the major functional elements of the TC11 controller is shown in Figure 2-2. The controller is organized around a 16-bit high-speed bipolar microprocessor. The ALU and register file portion of the microprocessor are implemented with four 2901 bit slice components. The microinstruction is 48 bits in length and the control memory of 1K words is implemented with twelve 1K x 4 PROMs.

All the device registers of the TC11 controller, the 4-word data buffer and working storage are contained in the microprocessor's registers.

The Write Data Register (WDR) holds the nine bits of data to the transport and the Read Data Register (RDR) receives the nine data bits from the transport. The Control Register holds internal control signals and the control signals to the transport via the control cable. The status signals from the transport via the control cable are testable signals to the microprocessor.

The Unibus interface consists of a 16-bit bi-directional set of data lines and an 18-bit set of address lines. The Unibus interface is used for programmed I/O, CPU interrupts, and NPR data transfers. The microprocessor responds to all programmed I/O and carries out the I/O functions required for the addressed controller register. The microprocessor also controls all NPR operations and transfers data between the Unibus data lines and the transport via its own internal buffer.



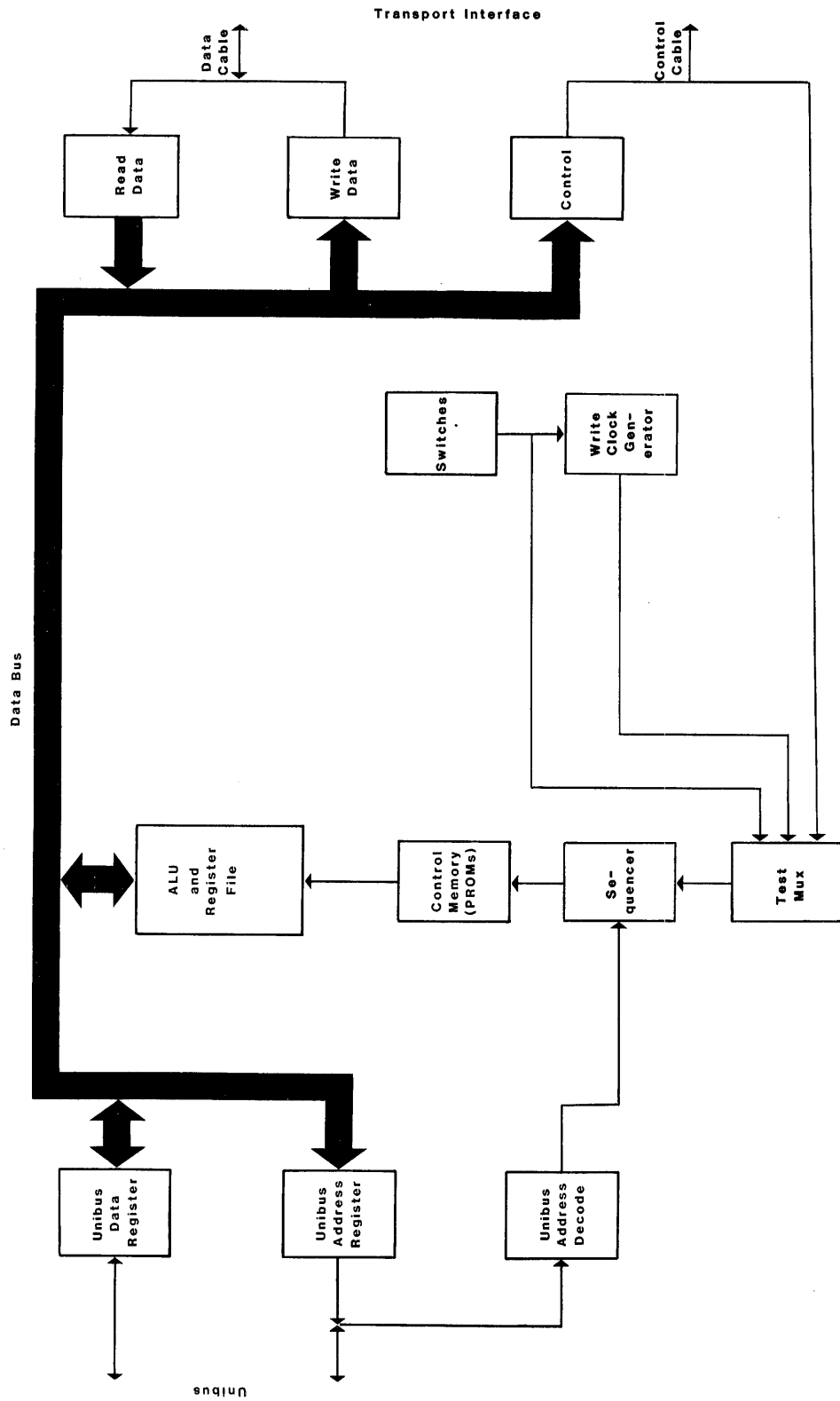


Figure 2-2 TC11 Block Diagram

### 2.2.2 PE Read Board

The PE Read Board intercepts the read data signals from the transport and converts the phase encoded waveform to NRZI data for the controller. The write data signals pass through the board from J1 to J2, but they can also be the input to the PE decode logic so that controller may simulate data from the transport when doing self-test.

The decode circuitry consists of a phase-locked loop and a three stage deskew buffer for each of the nine channels. The transistion detector and the high frequency part of the phase-locked loop are mechanized for each channel. The remainder of the loop, the deskew buffers and the bad track detection logic are done on a time-division multiplexed basis. The two VCO's (for two speeds) track either channel 6 or channel P.

## 2.3 TAPE TRANSPORT INTERFACE

### 2.3.1 Connectors and Cable

The tape controller uses two 40-conductor flat cables to interface to the transports. The cable should be a twisted pair with a maximum daisy-chained length of not over 50 feet. All wires should be 24 AWG minimum, and each pair should have not less than one twist per inch. Connectors are standard 40-pin flat cable connectors.

### 2.3.2 Input Circuits

The input lines from the tape transport are terminated with a 220 ohm, 5%, resistor to plus five volts, and a 330 ohm, 5%, resistor to ground. All input circuits have low-level input voltage of 0.8 volt maximum and a high level input voltage of 2.0 volt minimum. The input receivers are all 74LS type circuits.

### 2.3.3 Output Circuits

All output lines must be terminated at the far end of the daisy-chained cable with a 220 ohm, 5%, resistor to plus five volts and a 330 ohm, 5%, resistor to ground. Output driver circuits are 74LS374 TTL registers, except for some 7438 open collector gates.

### 2.3.4 Control Cable

The control cable has 11 signals from the controller to the transports, and seven responses from the tape transport to the controller. All signals are active-low logic level.

### 2.3.4.1 Control Signals to Tape Transport

#### Unit Select Lines: SLT0-SLT3

A low level on one of the four (4) unit select lines selects a tape transport. The select lines are a decoding of bits 09 and 08 of the MTC register.

#### Synchronous Forward Command: SFC

A low level causes the selected tape transport to move in the forward direction during read, write and space operations.

#### Synchronous Reverse Command: SRC

A low level causes the selected tape transport to move in the reverse direction during space reverse operation. The line becomes high upon reaching the load point.

#### Rewind Command: RWC

A low level pulse of approximately one usec commands the selected transport to rewind to the load point.

#### Rewind and Unload: RWU

A low level pulse of approximately one usec causes the on-line tape transport to be taken off-line.

#### Set Write Status: SWS

This line is at a low level for all write operations. The state of this line is interrogated in the tape transport approximately 20 usec after the leading edge of a SFC or SRC.

#### Overwrite Command: OVW

This line is low when an edit operation is taking place. The state of this line is interrogated in the tape transport approximately 20 usec after the leading edge of a SFC or SRC.

#### Data Density Select: DDS

A low level indicates that phase encoded operation is commanded. See 1.4.2 for information on forced PE operation.

### 2.3.4.2 Control Signals From Tape Transport

#### On-Line: OL

A low level indicates that the selected tape transport is on-line and under control of the tape controller.

Ready: RDY

A low level indicates that the selected tape transport has loaded the tape and not rewinding.

Rewinding: RWD

A low level indicates that the selected tape transport is engaged in a rewind operation or the load sequence following a rewind operation.

End of Tape: EOT

A low level indicates that the EOT tab on the tape is being sensed.

Load Point: LDP

A low level indicates that the selected tape transport is sensing the BOT tab on the tape, has completed its initial load sequence, and the tape transport is not rewinding.

File Protect: FPT

A low level indicates that a reel of tape without a write enable ring installed is mounted on the transport.

Data Density Indicator: DDI

A low level indicates that the high density PE mode of operation is selected. A high level indicates that the low density NRZI mode is selected.

NOTE - The controller uses this line to determine its own mode of operation.

2.3.5 Data Cable

The data cable plugs into connector J1 on the controller board or J2 on the PE Read Board. The data cable has 11 signals from the controller to the transport and 10 signals from the tape transports to the controller. All signals are active-low logic level.

2.3.5.1 Data Signals to Tape Transport

Write Data Lines: WDO-WD7, WDP

For NRZI operation, a low-level at the time of the trailing edge of WDS, will result in a flux transition being recorded on the tape if the transport is in the write mode. For phase encoded operation, the data lines are copied into the transport flip-flops on the trailing edge of WDS.

### Write Data Strobe: WDS

A low level pulse of approximately 1.2 usec occurs for each flux transition to be written on the tape. The frequency of the WDS is equal to the character rate in NRZI mode and twice the character rate in PE mode.

### Write Amplifier Reset: WARS

A low pulse of approximately 1.2 usec resets the write amplifier circuits on the leading edge. This signal is used to write the LRC character at the end of each record when recording NRZI data, and is used to turn off the write current doing an edit operation in both NRZI and PE modes.

### 2.3.5.2 Data Signals From Tape Transport

#### Read Data: RD0-RD7, RDP

For NRZI operation, the nine read data bits are clocked into the controller on the trailing edge of the read data strobe (RDS), and a low level indicates a binary 1 data bit. For PE operation, the signals on these lines are a replica of the wave form used to drive the write amplifiers when writing. The direction of the transition at the data transition time in the middle of the bit cell determines the state of the data. A transition from a high level to a low level on the read data lines indicates a binary 0 data, and a transition from a low level to a high level indicates a binary 1 data.

#### Read Data Strobe: RDS

A low level pulse of approximately one microsecond occurs for each data character read from the tape. The trailing edge of this pulse is used to clock the read data into the controller in NRZI mode.

## 2.4 UNIBUS INTERFACE

The controller interfaces to the PDP-11 or VAX-11 Unibus via a Small Peripheral Controller (SPC) connector. The Unibus consists of 18 address lines and 16 bi-directional data lines, plus control signals for data and interrupt vector address transfer and for becoming bus master. The signal connections of the SPC connector are shown in Table 2-3.

### 2.4.1 BR (Interrupt) Priority Level

The controller is hardwired for BR5. The other three Bus Grant signals are jumpered through.

### 2.4.2 Register Address

The controller register addresses are fixed and consist of seven registers starting at the standard TM11 address of 772520. An

alternate set of addresses may be used with Version -02 of the TC01. This set begins with the address 772460.

#### 2.4.3 Interrupt Vector Addresses

The standard controller interrupt vector address for a TM11 is 224. Three alternate addresses are available. Table 4-3 contains the interrupt vector switch settings.

#### 2.4.4 DCLO and INIT Signals

The DCLO and INIT signals both perform a controller clear. The self-test is performed only if DCLO has been asserted.

#### 2.4.5 NPR Operations

All DMA data transfers are carried out under microprocessor control. A check is made for memory parity errors when doing a tape write operation. If an error is detected the non-existent memory (NXM) error is set.

Table 2-1  
Control Cable Interface

Controller J2		Transport J101		Function
Signal	Ground	Signal	Ground	
17	18	J	8	Select 0 (SLT0)
19	20	A	8	Select 1 (SLT1)
7	8	18	8	Select 2 (SLT2)
9	10	V	8	Select 3 (SLT3)
15	16	C	3	Synchronous Forward Command (SFC)
3	4	E	5	Synchronous Reverse Command (SRC)
11	12	H	7	Rewind Command (RWC)
1	2	L	10	Rewind and Unload Command (RWU)
5	6	K	9	Set Write Status (SWS)
13	14	B	2	Overwrite (OVW)
21	22	D	4	Data Density Select (DDS)
27	28	T	16	Ready (RDY)
35	36	M	11	On-Line (ONL)
33	34	N	12	Rewinding (RWD)
31	32	U	17	End of Tape (EOT)
37	38	R	14	Load Point (LDP)
39	40	P	13	File Protect (FPT)
23	24	F	6	Data Density Indicator (DDI)

Table 2-2  
Data Cable Interface

Controller J1		Transport J102		Function
Signal	Ground	Signal	Ground	
21	22	C	3	Write Amplifier Reset (WARS)
23	24	A	1	Write Data Strobe (WDS)
25	26	L	10	Write Data Parity (WDP)
35	36	M	11	Write Data 0 (WD0)
27	28	N	12	Write Data 1 (WD1)
29	30	P	13	Write Data 2 (WD2)
33	34	R	14	Write Data 3 (WD3)
32	-	S	-	Write Data 4 (WD4)
31	-	T	-	Write Data 5 (WD5)
39	40	U	17	Write Data 6 (WD6)
37	38	V	18	Write Data 7 (WD7)

Controller J1		Transport J103		Function
Signal	Ground	Signal	Ground	
3	4	2	B	Read Data Strobe (RDS)
1	2	1	A	Read Data Parity (RDP)
9	10	3	C	Read Data 0 (RD0)
11	12	4	D	Read Data 1 (RD1)
17	18	8	J	Read Data 2 (RD2)
19	20	9	K	Read Data 3 (RD3)
13	14	14	R	Read Data 4 (RD4)
7	8	15	S	Read Data 5 (RD5)
5	6	17	U	Read Data 6 (RD6)
15	16	18	V	Read Data 7 (RD7)



Table 2-3  
SPC Unibus Connections

Column	C		D		E		F		
	Pin	1	2	1	2	1	2	1	2
A	NPGIN	+5V		+5V		+5V		+5V	
B	NPGOUT					-15V		-15V	
C	PA	GND		GND	A12	GND		GND	
D		D15		BR7	A17	A15	BBSY		
E		D14		BR6	MSYN	A16			
F		D13		BR5	A02	C1			
H	D11	D12		BR4	A01	A00			
J		D10			SSYN	C0	NPR		
K		D09		BG7IN	A14	A13			
L		D08	INIT	BG7OUT	A11				
M		D07		BG6IN			INTR		
N	DCLO	D04		BG6OUT	A08				
P		D05		BG5IN	A10	A07			
R		D01		BG5OUT	A09				
S	PB	D00		BG4IN					
T	GND	D03	GND	BG4OUT	GND		GND	SACK	
U		D02			A06	A04			
V	ACLO	D06			A05	A03			

**BLANK**

### 3.1 CONTROLLER REGISTERS

Device register usage is compatible with DEC TM11 register definitions. Some additions have been provided for extended functions. A Maintenance Register was added for PE Read Board diagnostics. Register functions and bit assignments are described in the following sections.

Registers and their mnemonic codes are the following:

<u>Location</u>	<u>Mnemonic</u>	<u>Name</u>
772520	MTS	Status Register
772522	MTC	Command Register
772524	MTBRC	Byte Record Counter
772526	MTCMA	Current Memory Address Register
772530	MTD	Data Buffer Register
772532	MTRD	Read Lines
772534	MTM	Maintenance Register

#### 3.1.1 Status Register (MTS) 772520

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ILC	EOF	CRE	PAE	BGL	EOT	RLE	BTE	NXM	SELR	BOT	7CH	SDN	WRL	RWS	TUR
		PEE													

#### Illegal Command (ILC) - Bit 15

This bit indicates an illegal command is received by the controller. It is set by the following illegal conditions:

- Any write to the MTC register during a tape operation. RDY in the MTC register indicates a controller tape operation is not in progress.
- Any write, write-end-of-file, or write-with-extended-inter-record gap (functions 5, 7, and 15) operation to a file-protected tape unit.
- Any command to a tape unit that is not on-line. SELR in the MTS indicates a tape unit which is on-line.
- Any time a tape unit goes off-line during any operation except off-line.

The ILC in MTS and ERR in MTC are set simultaneously. This is a read-only bit which is cleared by INIT, PWR CLR, or setting GO.

#### End of File (EOF) - Bit 14

This bit indicates that the tape has reached the end of the file. The EOF bit is set during a read, write or space operation when a file mark (PE mode) or a LRC character (NRZI mode) is detected. The ERR in the MTC is set at the same time. This is a read-only bit which is cleared by INIT, PWR CLR, or the initiation of a tape operation.

A pair of EOF characters (238) are written into the memory when an EOF character (NRZI mode) or a tape mark (PE mode) is detected during a read operation and the byte count has not yet reached zero.

#### Cyclic Redundancy Error (CRE) - Bit 13

This bit indicates a cyclic redundancy error has been detected during a NRZI read operation. This check compares the CRC character written on a 9-track NRZI tape during a write or write-with-extended-IRG operation with the CRC character generated in the controller during a read operation. If the two CRC characters are not the same, the CRE bit is set. The ERR bit in MTC is set at the same time. This is a read-only bit which is cleared by INIT, PWR CLR, or setting GO.

#### PE Error (PEE) - Bit 13

In PE mode this bit indicates that one or more bad tracks were detected during a write, write-with-extended-IRG or write EOF operation, or that more than one bad track was detected during a read or space operation. A single bad track can be tolerated when reading, since the missing data is reconstructed from the parity information, in which case CPE in MTRD is set to a 1-bit. PEE is also set when excessive track-to-track skew is detected. This is a read-only bit which is cleared by INIT, PWR CLR or setting GO.

#### Parity Error (PAE) - Bit 12

In NRZI operation, this bit indicates the detection of:

- Vertical parity error on any character other than the CRC or LRC character. Odd or even parity is defined by the even parity bit (PEVN in the MTC). Detection of a vertical parity error does not affect the transfer of data.
- Longitudinal Parity Error. This error is defined as an odd number of ones in any channel in the record.

In PE operation, this bit indicates the detection of:

- Vertical parity error on any character other than the preamble and postamble. This check is disabled for single track errors on read operation. Vertical parity errors do not affect the transfer of data.

The PAE bit is set when the parity error is detected, and the ERR bit in the MTC is set at the end of the record. This is a read-only bit which is cleared by INIT, PWR CLR, or setting GO.

#### Bus Grant Late (BGL) - Bit 11

This error occurs if Unibus NPR data transfers do not occur in sufficient time to insure valid data transfer through the controller data buffer. During write or write-with-extended-IRG, this error will occur if a write strobe is issued to the transport when there is no data to transfer. During read, this error occurs when a data character is read from the tape and the data buffer is full. A check is also performed to insure all data is transferred via NPR requests prior to completing a read operation.

The BGL in the MTS and ERR in the MTC are set simultaneously. This is a read-only bit which is cleared by INIT, PWR CLR, or setting GO.

#### End of Tape (EOT) - Bit 10

The EOT bit is set when the EOT marker is detected when the tape is moving in the forward direction. It is cleared by the trailing edge of the EOT marker when the tape is moving in the reverse direction.

The EOT is an error condition when the tape is moving in the forward direction and ERR in the MTC is set at the end of the record. This is a read-only bit.

#### Record Length Error (RLE) - Bit 09

This bit is set during read operations and occurs when a byte is read after the byte counter has incremented to zero and data transfers have stopped. The controller continues to read the entire record and sets ERR in the MTC when the end of the record is detected.

The RDY in the MTC remains cleared until the end of the record is detected, at which time RDY is set. This is a read-only bit which is cleared by INIT, PWR CLR, or setting GO.

#### Bad Tape Error (BTE) - Bit 08

A bad tape error occurs when a tape character is detected during the inter-record gap, or data can not be found within 16 feet after initiating a read or space operation.

ERR in the MTC is set simultaneously with BTE. See Bit 13 of the MTRD register for diagnostic simulation of this error bit. This is a read-only bit, which is cleared by INIT, PWR CLR, or setting GO.

### Non Existent Memory (NXM) - Bit 07

This error occurs when the controller is bus master during NPR transfer and does not receive a SSYN response within 3 us. after asserting MSYN. NXM in MTS and ERR in MTC are set simultaneously. This is a read-only bit which is cleared by INIT, PWR CLR, or setting GO.

### Select Remote (SELR) - Bit 06

This bit is set when the tape unit has been properly selected. The SELR bit is zero if the tape unit addressed does not exist, if the selected tape unit is off-line, or if the tape unit power is OFF. This is a read-only bit.

### 7 Channel (7CH) - Bit 04

This bit is always zero to indicate 9-track tape units. This is a read-only bit.

### Settle Down (SDWN) - Bit 03

This bit is set whenever the tape unit has completed an operation and the tape is slowing down. When the tape unit stops, SDWN is reset and the tape unit ready (TUR) is set.

The tape controller will accept any new command during the SDWN period, except if the new command is directed to the same tape unit which issued SDWN and the new command is not the same as the previous one. This is a read-only bit.

### Write Lock (WRL) - Bit 02

This bit is controlled by the presence or absence of a write protect ring on the selected tape unit. Absence of the write ring sets WRL and prevents the controller from writing on the tape. Presence of the write ring clears WRL and enables the writing of information on tape. This is a read-only bit.

### Rewind Status (RWS) - Bit 01

This bit is set at the start of a rewind operation and is reset as soon as the BOT marker is detected while the tape is moving in the forward direction. This is a read-only bit.

### Tape Unit Ready (TUR) - Bit 00

This bit is set when the tape unit is selected, the tape is loaded and stopped, and the SELR bit is set. This indicates the tape unit is ready to receive a new command. The bit is cleared when the selected tape is in motion. This is a read-only bit.

### 3.1.2 Command Register (MTC) 772522

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ERR	DEN	DEN	PWR	PEVN	SEL	SEL	SEL	RDY	IE	A17	A16	F2	F1	F0	GO
	8	5	CLR		2	1	0								

#### Error (ERR) - Bit 15

This bit indicates an error condition and is a function of bits <07:15> in the status register. It is cleared by INIT, PWR CLR, or by the next GO command. This is a read-only bit.

#### Density Bits (DEN8, DEN5) - Bits <14:13>

Bit 14 (DEN 8)	Bit 13 (DEN 5)	Density (BPI)	No. of Tracks
1	1	800 NRZI	9
0	0	1600 PE	9

Note that the controller will conform to the mode of the transport. Since standard software will select 800 bpi, the selection of 1600 bpi at the transport will force PE operation. To prevent errors, the software must be compatible with the mode of operation (PE or NRZI).

#### Power Clear (PWR CLR) - Bit 12

When a 1 is loaded into this bit position, it clears the controller registers and stops any tape operation except a rewind. The PWR CLR bit is always read back by a 0.

#### Parity Even (PEVN) - Bit 11

This bit is set if even vertical parity is to be used for a read or write operation. The bit is cleared if odd vertical parity is to be used. Vertical parity is checked for all tape motion operations except space forward, space reverse, and rewind. This is a read/write bit which is cleared by INIT, PWR CLR, or by loading a 0.

#### Unit Select (SEL) - Bits <10:08>

These three bits are the address of the tape unit being selected. All operations defined in the MTC and all status conditions defined in the MTS pertain to the selected tape unit. Units 0-3 select speed 1, while units 4-7 select speed 2. Only four physical tape units may be selected. These are read/write bits which are cleared by INIT, PWR CLR, or by loading zeros.

Controller Ready (RDY) - Bit 07

This bit, when set, indicates the controller is ready to receive a new command. It is cleared by setting the GO bit and is set at the completion of a tape operation, by INIT, PWR CLR, or when an error condition exists. This is a read-only bit.

Interrupt Enable (IE) - Bit 06

When set this bit allows an interrupt to occur whenever RDY changes from 0 to 1, or whenever a tape unit that was set into rewind has arrived at BOT. In addition, an interrupt is generated on an instruction that sets IE and does not set the GO bit. This is a read/write bit which is cleared by INIT, PWR CLR, or by loading a 0.

Extended Address Bits (A17, A16) - Bits <05:04>

These bits are bus address bits A17 and A16 and are used with the MTCMA register to specify an 18-bit address. These bits function with the MTCMA register and are incremented by one when MTMCA overflows. These are read/write bits which are cleared by INIT, PWR CLR, or by loading a 0.

Function Bits (F2-F0) - Bits <03:01>

These bits specify a command to be performed by the selected tape unit. These functions are:

Code	Function
0 (1)	Off-line
1 (3)	Read
2 (5)	Write
3 (7)	Write End of File
4 (11)	Space Forward
5 (13)	Space Reverse
6 (15)	Write with Extended IRG
7 (17)	Rewind

Function bits are read/write and are cleared by INIT, PWR CLR, or by loading a zero. Section 3.2 describes each controller function.

GO Bits (GO) - Bit 00

This bit is loaded with a 1 to initiate the function selected. When set, this bit clears RDY, ERR and the error flag. GO is cleared when the command is initiated by the controller. The time required to initiate may vary when issued to a rewinding drive.



### 3.1.3 Byte/Record Counter (MTBRC) 772524

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

Two's Complement of Number of Bytes or Records

The byte/record counter is loaded with the two's complement of the number of bytes to be transferred or the number of records to be spaced over. The MTBRC is cleared by INIT, PWR CLR, or by loading zeros.

This is a 16-bit binary counter used to count bytes in a read or write operation, and records in a space forward or reverse operation. When used in a write or write-with-extended-IRG operation, this register is set by the program to the two's complement of the number of bytes to be written on the tape. After the last byte of the record has been read from memory the register becomes 0. In NRZI, the controller then writes the CRC character and instructs the tape unit to write the LRC character. In PE (phase encoded) operation, the controller writes the postamble sync and 0s.

When used in a read operation, this register is set to a number equal to or greater than the two's complement of the number of words to be loaded into the memory. A record length error occurs whenever a character is received after the register has been incremented to zero. Neither the CRC or LRC character in NRZI mode or the preamble or postamble characters in PE mode are loaded into the memory.

When used in a space forward or space reverse operation, the byte record counter register is loaded with the two's complement of the number of records to be spaced over. The counter is incremented by 1 at the end of each record regardless of the tape direction. The space operation terminates when an EOF or file mark is read.

### 3.1.4 Current Memory Address Register (MTCMA) 772526

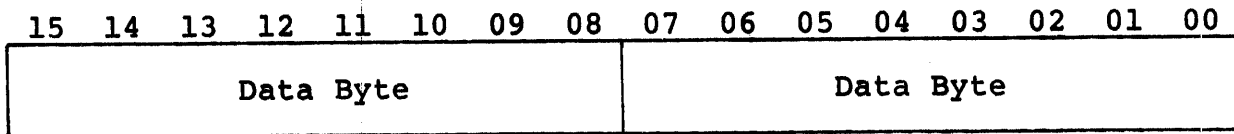
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

Memory Address

The MTCMA contains 16 of the 18 memory address bits. It is used in NPR operations to provide the memory address for data transfers in read, write, and write-with-extended-IRG operations. Prior to issuing a command, the MTCMA is set to the memory address into which the first byte is loaded in a read operation, or from which the first byte is read in a write or write-with-extended-IRG operation. If the initial or final memory address is not on a word boundary (Bit 00 is a one), that NPR operation will transfer one byte of data. NPR transfers, when the memory address falls on word boundaries (bit 00 is a zero), will be on a word basis (two bytes).

The MTCMA is incremented by one for each byte and two for each word of data transferred. Therefore, at any instance of time it points to the next higher address than the one which had most recently been accessed. In the error condition, memory parity error and non-existent memory (NXM), the MTCMA contains the word address of the location in which the failure occurred, plus two.

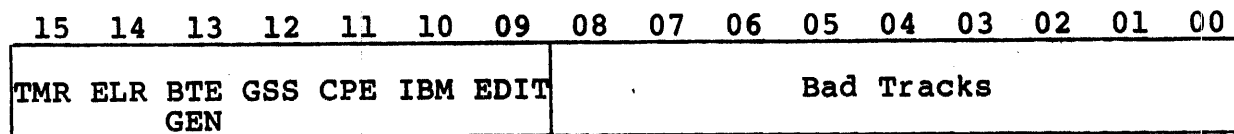
### 3.1.5 Data Buffer Register (MTD) 772530



The data buffer is a 16-bit register which is used during read, write, or write-with-extended-IRG operations. In a read operation, the data buffer is a temporary storage register for characters read from the tape before being stored into the memory. As the tape characters are read from the tape, they are assembled into a 16-bit word prior to transferring into the memory. During a write or write-with-extended-IRG operation, the data buffer is a temporary storage register for words read from the memory before they are written on tape. Each word from the memory is disassembled into two tape characters.

In a read operation, the LRC character (simulated LRC for PE operation) is placed in the Data Buffer register when ELR (bit 14 in MTRD) is a one, and is inhibited from doing so when ELR is a zero. Thus, after reading a nine channel tape, the data buffer contains the LRC character when ELR is a one, and the CRC character when ELR is a zero. After reading a seven channel tape, the data buffer contains the LRC when ELR is a one, and the last data character when ELR is a zero. INIT or PWR CLR clears all bits of the MTD.

### 3.1.6 Read Lines (MTRD) 772532



#### Timer (TMR) - Bit 15

The timer is a 10 KHz signal with a 50% duty cycle. The signal can be used for diagnostic purposes in measuring the time duration of tape operations. This is a read-only bit.

#### Enable LRC (ELR) - Bit 14

This bit is used to enable the LRC character to be placed in the MTD register rather than the CRC or last data character. This is a read/write bit which is cleared by INIT or PWR CLR. (See Section 3.1.5)

### Bad Tape Generator (BTE GEN) - Bit 13

This bit is used during diagnostics to check the bad tape error logic. When loaded with a 1, RDY is set and the tape is stopped, causing a premature gap shutdown while characters are still being read. This in turn, causes a bad tape error indication since one or more characters will be received in what the controller assumes to be the IRG. This is a write-only bit which is cleared by INIT, PWR CLR, or the completion of a tape operation.

### Gap Shutdown Status (GSS) - Bit 12

When set, this bit indicates the tape controller is in a gap shutdown interval, which is the time between reading or writing the last and then stopping the tape.

### Correctable Parity Error Status (CPE) - Bit 11

This bit indicates the controller detected and corrected a parity error in PE read operation. The data transferred into memory is the corrected data. This bit is read-only and is cleared by INIT, PWR CLR, or by the initiation of a tape operation.

### IBM Mode (IBM) - Bit 10

This bit controls the assembling and disassembling of the 16-bit data word transferred to or from the processor on a read, write or write-with-extended-IRG operation. When cleared, the even byte (bits <07:00>) corresponds to the first tape character on tape, and the odd byte (bits <15:08>) corresponds to the second character on tape. This is the normal DEC mode of operations.

When this bit is set the order of bytes is reversed. The odd byte (bits <15:08>) corresponds to the first character on the tape and the even byte (bits <07:00>) corresponds to the second character on tape. This is compatible with the IBM method of addressing bytes. This is a read/write bit which is cleared by INIT, PWR CLR, or by writing a 0.

### Edit Mode Control (EDIT) - Bit 09

This bit allows the controller to operate in edit mode. In this mode of operation, the processor can selectively replace any record of a previously recorded tape with an updated record. This bit is a write-only bit which is cleared by INIT, PWR CLR, or by writing a 0.

### Bad Tracks - Bits <08:00>

When a bad track is detected the corresponding BT bit is set after the record is read. In NRZI operation, these bits are an exclusive-OR of the generated LRC character and the one read from the tape. These bits indicate the channels with a longitudinal

parity error. In PE operation, these bits indicate the channels which are dead at the end of the record. A track is detected bad and becomes dead for the remainder of the record, when incorrect, missing or misplaced transitions are detected during read, space, or write operations. The order of channel numbers is reversed from the order of bit numbers. Bit 00 is for Channel 7, bit 01 is for Channel 6, etc. Bit 08 is for channel P. These are read-only bits which are cleared by INIT, PWR CLR, or the initiation of a tape operation.

### 3.1.7 Maintenance Register (MTM) 772534

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	Command							

This register is a read/write register which is used to command the built-in diagnostics of the PE Read Board. The following commands can be used:

- 05X - Perform single pass test
- 15X - Perform continuous test
- 250 - Stop test

Where X = 1 - Freeze bad track selection  
 = 2 - Freeze data pattern  
 = 4 - Stop on errors

## 3.2 FUNCTION COMMANDS

Command and their corresponding function codes (always odd since the GO bit is included) are described below:

### 3.2.1 Off-Line (1)

This function causes the tape transport to go off-line. With some transports, it also rewinds and/or unloads the tape.

### 3.2.2 Read (3)

This function causes a single record to be read from the tape. All data characters up to the number of bytes specified by MTBRC are transferred to the CPU memory at the address specified by MTCMA. Data transfer is aborted by non-existent memory timeout and data late.

### 3.2.3 Write (5)

This function causes a single record to be written on the tape with the number of characters specified by MTBRC transferred from the CPU memory at the address specified by MTCMA. Data transfer is aborted by non-existent memory timeout, memory parity error, data late.

#### 3.2.4 Write EOF (7)

This function causes three inches of tape to be erased and a tape mark (PE mode) or EOF character and associated LRC (NRZI mode) to be written on the tape. The PE tape mark and the NRZI EOF character and its associated LRC character are considered one record.

#### 3.2.5 Space Forward (11)

This function causes the tape to space over the number of records specified by MTBRC. The space operation stops when a tape mark or EOF is read. Space forward does not transfer any data to the CPU memory.

#### 3.2.6 Space Reverse (13)

This function is identical to the space forward function except the tape moves in the reverse direction.

#### 3.2.7 Write-With-Extended-IRG (15)

This function is the same as write except that a 3-inch segment of tape is erased before writing the first character or the preamble.

#### 3.2.8 Rewind (17)

This function initiates a rewinding of the tape. The controller becomes ready immediately after sending the rewind pulse to the transport. This function sets the RWS status bit, which is reset when the tape reaches the beginning-of-tape (BOT) marker and the tape motion is stopped.

### 3.3 INTERNAL SELF-TEST

#### 3.3.1 Controller Test

The TC11 Tape Controller has a built-in self-test for verifying the proper operation of the controller. This test is initiated when the CPU and controller are powered-up, and by the front panel INIT button when option switch SW2-5 is closed and the LED's are not on. The LED on the controller board is turned on at the beginning of the self-test and is turned off after successful completion of the test. If any fault is detected during the test, the controller's microprocessor stops at the step where the error is detected and leaves the LED on. The controller cannot be addressed from the CPU while the LED is indicating a controller fault. The self-test exercises the microprocessor, the byte swap register, the 10 KHz. timer, the write time base, and the Unibus DMA and programmed I/O logic. The Unibus test can be disabled by closing option switch SW2-6. The write data and read data interfaces are also checked if a PE Read Board is present.

### 3.3.2 PE Read Board Test

The controller can exercise an extensive self-test on the PE Read Board. This test consists of a simulated phase encoded record consisting of a preamble, 20 identical data characters and shortened postamble. The test can be operated with various data patterns, bad track configurations, and operating modes as described below.

#### 3.3.2.1 Test Initiation

The PE Read Board test is automatically executed following the successful execution of the controller self-test when the PE Read Board is connected to the controller. Therefore, the test is initiated upon power-up and by depressing the front panel INIT button when option switch SW2-5 is closed if the LED is not on. The closing of this option switch also provides for continuous run of the PE Read Board self-test without stopping on errors so as to facilitate observing the operation by means of an oscilloscope. An alternative method of initiating the self-test is to enter 05X or 15X into the Maintenance Register (MTM). (See Section 3.1.7.) The LED located between the connectors on the PE Read Board is turned on when the controller or PE Read Board self-test is initiated and will be on as long as the controller is in the PE Read Board self-test.

#### 3.3.2.2 Self-Test Registers

The PE Read Board self-test makes use of the TC11 registers for set-up and communicating error information. These registers are used as described in Table 3-1.

#### 3.3.2.3 Data Patterns

The self-test makes use of 10 data patterns consisting of a single bit in each of the channels (starting with the Channel P and proceeding through Channel 7) and an all 1s pattern. Each data pattern is run without any bad tracks and then with a single bad track in each of the channels (starting with Channel P and proceeding through Channel 7). The test starts over when all patterns have been run. If an error is detected during a record, the pattern is repeated with the same bad track. Other data patterns and bad track configurations can be run by entering these into the appropriate register and running the test with data and bad track freeze.

It should be noted that tape Channel P corresponds to bit position 8; Channel 0 corresponds to bit position 7; Channel 7 corresponds to bit position 0.

#### 3.3.2.4 Error Codes

The self-test monitors the data status being received from the PE Read Board during the simulated record. When an error is detected,

an error code is placed in bits <14:12> of the MTS register. These error codes are given in Table 3-2.

Table 3-1  
PE Read Board Self-Test Registers

Address	Register	Use
772520	MTS	Error code in bits <14:12>. See Table 3-2.
772522	MTC	Speed 2 can be selected by setting bit 10 (2000).
772524	MTBRC	Count of characters in record, starting with 2 <sup>4</sup> <sub>8</sub> and counting to 0.
772526	MTCMA	Write Data
772530	MTDB	Read Data or status
772532	MTRD	Bad Track configuration
772534	MTM	Maintenance Register used to initiate test and select options.

Table 3-2  
PE Read Board Self-Test Error Codes

<u>Code</u>	<u>Error</u>
0	No Error
1	No data received
2	Read data not equal to write data
3	Postamble detect flag not present
4	Bad track status not equal to expected bad track
5	Status Error



This section describes the step-by-step procedure for installation of the TC11 Tape Controller in a Unibus environment. The following list is an outline of the procedure. Each step corresponds to a second level heading in this section (i.e., item one, Inspect the TC11, is covered in paragraph 4.1).

Emulex recommends that Section 4 be read in its entirety before installation is begun.

1. Inspect the TC11.
2. Prepare the tape drives.
3. Prepare the CPU.
4. Configure the TC11.
5. Install the TC11.
6. Route the drive I/O cables.
7. Run the diagnostics.

#### 4.1 INSPECTION

A visual inspection of the board is recommended after unpacking. Specific checks should be made for such items as bent or broken connector pins, damaged components or any other visual evidence of physical damage. The PROMs should be examined carefully to insure that they are firmly and completely seated in the sockets.

#### 4.2 TRANSPORT CONFIGURATION AND MODIFICATION

##### 4.2.1 Transport Configuration

The transport manual should be checked to insure that the transport is configured for the desired modes of operation. PE (1600 bpi) operation is normally enabled by the high density switch at the tape transport. The controller will conform to the mode of the transport. The controller can also be programmed for 1600 bpi. Since standard software will select 800 bpi, the selection of 1600 bpi at the transport will force PE operation. In particular, the configuring of the DDI signal should be checked since some transports configure this signal differently from that required by the TC11 controller. This signal determines how the mode (PE or NRZI) of the controller is sensed. Check the interface section of your transport manual for specification of the characteristics of this signal. After the levels for the transport have been

determined, see 4.3.6.1 for information on setting the dual density level on the TC11.

#### 4.2.2 Transport Addressing

It is possible to use up to four tape drives with the TC11. When using more than one tape drive, it is necessary to assign unique unit numbers to each tape drive. The unit numbers must be within the range 0-3 or 4-7. In assigning unit numbers it is important to be aware of tape speeds. The units assigned in the 0-3 range will run at a different speed than those assigned to the 4-7 range. The corresponding device names are MT0-MT7, respectively. See 4.3.3 for information pertaining to the programming of tape speed. The standard address 772520 or the alternate address 772460 must be used for all units.

#### 4.2.3 Transport Modifications

In some cases it may be necessary to make a minor modification to the transport for it to work properly with the TC11.

##### 4.2.3.1 Cipher Units

The Cipher transports require a modification if they are to operate at 125 ips in PE mode. This modification causes the write strobe to write off the trailing edge rather than a delay of the leading edge. The 900X transport is modified as follows:

- 1) Cut ground etch to pin 9 of the 74LS123 at U115.
- 2) Cut the etch between pin 10 of U115 and top of R259, which is available immediately to the right of R259.
- 3) Jumper U115 pin 9 to U112 pin 6 (or lower end of R259).
- 4) Jumper U115 pin 10 to U115 pin 16.

##### 4.2.3.2 Pertec Units

The DDI status output from Pertec tape transports is the OR of phase encoded mode and 9 track mode. Since the DDI must be a function of the transports PE mode only, it is necessary to cut the etch to the OR gate where 9-track mode is OR-ed in.

### 4.3 CONTROLLER SET-UP

The TC11 controller assembly is shown in Figure 4-1.

#### 4.3.1 Controller Address Selection

Unibus addressing for the TC11 is not selectable. The controller board designated TC1110401-01 has a base address beginning at 772520. The TC1110401-02 version has a base address which begins with 772460. See Section 3 for a description of the registers.

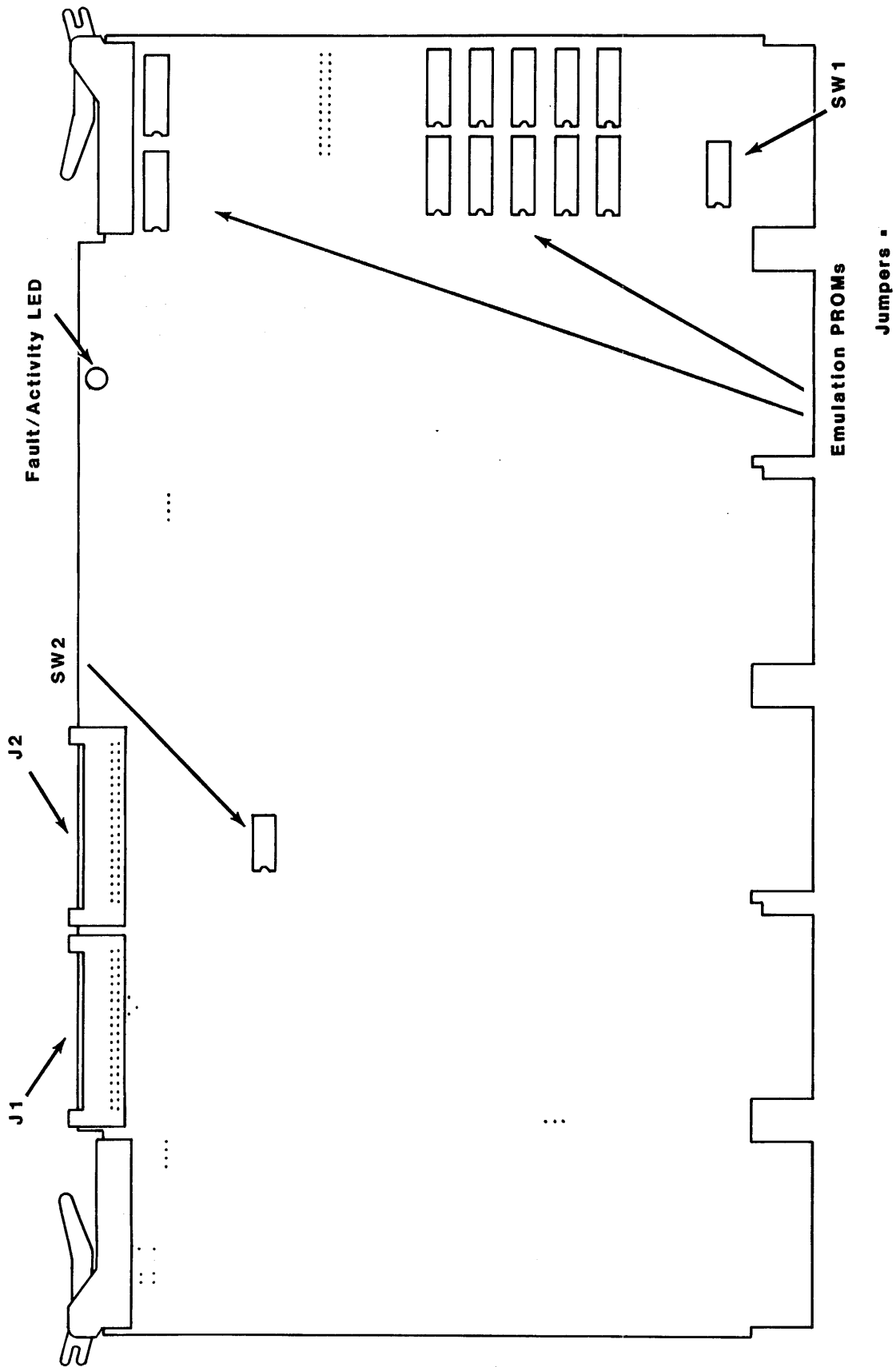


Figure 4-1 TC11 Controller Assembly

### 4.3.2 Interrupt Vector Address Selection

The interrupt vector addresses are set by SW2-2 and SW2-3. See Table 4-3 for those addresses.

### 4.3.3 Tape Speed Switches

The tape speed is programmed into the controller by the DIP switch SW1 located on the lower right hand corner of the controller board. There are two speeds which can be set up. Speed 1 is programmed by switches SW1-1, SW1-2, and SW1-3. Speed 2 is programmed by switches SW1-4, SW1-5, and SW1-6. The controller uses speed 1 when the unit number is in the range 0-3 and uses speed 2 when the unit number is in the range 4-7. Table 4-1 lists the switch settings for the eight tape speeds.

Table 4-1  
Tape Speed Switch Settings

Speed 1:	SW1-1	SW1-2	SW1-3
Speed 2:	SW1-4	SW1-5	SW1-6
125 ips	ON	ON	ON
75 ips	OFF	ON	ON
45 ips	ON	OFF	ON
37.5 ips	OFF	OFF	ON
25 ips	ON	ON	OFF
18.75 ips	OFF	ON	OFF
15 ips	ON	OFF	OFF
12.5 ips	OFF	OFF	OFF

### 4.3.4 NRZI Only Configuration

When the controller board is to be used without the PE Read Board, certain lines in the Data Cable should be grounded by jumpers near J1 on the board. These lines are used to carry control signals when used with the PE Read Board, but are ground returns of read data lines when the Data Cable is plugged directly into the controller. The jumpers which must be installed are B-C, D-E, F-G, H-J, K-L, and M-N. In addition, the jumper A-B must be removed.

NOTE - It is not mandatory to change over from PE configuration to run without the PE Read Board. It only provides some better grounding which may be necessary with long cables.

#### 4.3.5 PE Reverse Consideration

When reading PE data in reverse the data must be complemented for proper operation. The PE Read Board has this capability. Some tape transports (notably Kennedy) have an option which performs this function - in which case the function must be defeated on the controller board. This is done by installing a jumper between pins K and L on the upper left hand corner of the controller board. If it is not known whether the option is installed in the tape transport, the diagnostics should be run with the jumper removed and then with it installed to see which gives proper operation.

#### 4.3.6 Option Switches

The TC11 has several optional features which allow the user to optimize the controller for a particular application. Dip switch SW2 selects these options. The options are described below.

##### 4.3.6.1 Dual Density Polarity Inversion

SW2-4 inverts the polarity of the DDI line. When the switch is OFF and the line is low, the high density (PE) mode of operation is indicated. When the switch is ON and the line is low, the low density (NRZI) mode is specified. See 2.3.4.2 for more information on level indications.

##### 4.3.6.2 Continuous Running of Self-Test

SW2-5 is used primarily for trouble-shooting. It allows the PE Read Board self-test to run continuously without stopping on errors.

##### 4.3.6.3 Unibus Check

SW2-6 puts data on the bus and checks the Unibus interface to ensure its operability.

#### 4.4 PE BOARD SET-UP

The PE Read board assembly is shown in Figure 4-2.

##### 4.4.1 PE Read Board Speed Selection

There are two different PE Read board designs. The TU1110406 sets speed by switch selection; the TU1110402 sets speed by changing capacitors and adjusting pots.

##### 4.4.2 TU1110406 Speed Selection

The PE Read Board with assembly number TU1110406 incorporates two rotary selector switches, SW1 and SW2 located on the right side of the board, for establishing the primary and secondary speed settings respectively. The switches allow selection of four speeds as follows:

Code	Speed
1	125 ips
2	75 ips
3	45 ips
4	37.5/25 ips

To provide 25 ips, it is necessary to insert the 25 ips jumper located below the switches and to adjust the 37.5/25 ips pot (R24) in accordance with Table 4-2. There is a pot for each of the four speeds provided on the board. They are adjusted as described in Section 4.4.3, and set as indicated in Table 4-2. There is no need to adjust for speed 2 as it uses the same VCO's as does speed 1.

#### 4.4.3 TU1110402 Speed Selection

The PE Read Board has two VCO's, each of which has two capacitors whose value must be selected based on the speed of the tape. Capacitors C20 and C27 are used with speed 1, and with C21 and C28, speed 2. The capacitors are soldered onto terminals on the board. In addition, there is a trimpot for adjusting the frequency at each VCO to the nominal frequency. R8 is used with speed 1 and R9 is used with speed 2.

Normally the proper capacitors are mounted and the VCO frequency adjusted at the factory in response to the purchase order. If it should be necessary to initially set up the VCO frequency or to change it in the field, the following procedure should be carried out.

The appropriate capacitors are installed in accordance with Table 4-2. The PE Read Board is then plugged into the CPU using an extender board or a slot where the trimpots can be reached with a screwdriver. While monitoring the timing generator output on TP1 (U1, pin 2), the period is adjusted by the trimpot in accordance with Table 4-2. By shorting terminal A-B, the same procedure can be carried out for speed 2.

### 4.5 PHYSICAL INSTALLATION

#### 4.5.1 Slot Selection

The controller may be placed in any SPC slot along the Unibus without regard to NPR priority. The controller contains adequate buffering to prevent data lates and will automatically get off the bus if any other device requests the Unibus. If the system contains a Unibus repeater, the controller will not give priority to devices which are on the CPU side of the repeater when the controller is on the far side of the repeater. This may require that the controller be placed on the CPU side of the repeater or that all DMA devices be on the far side of the repeater.

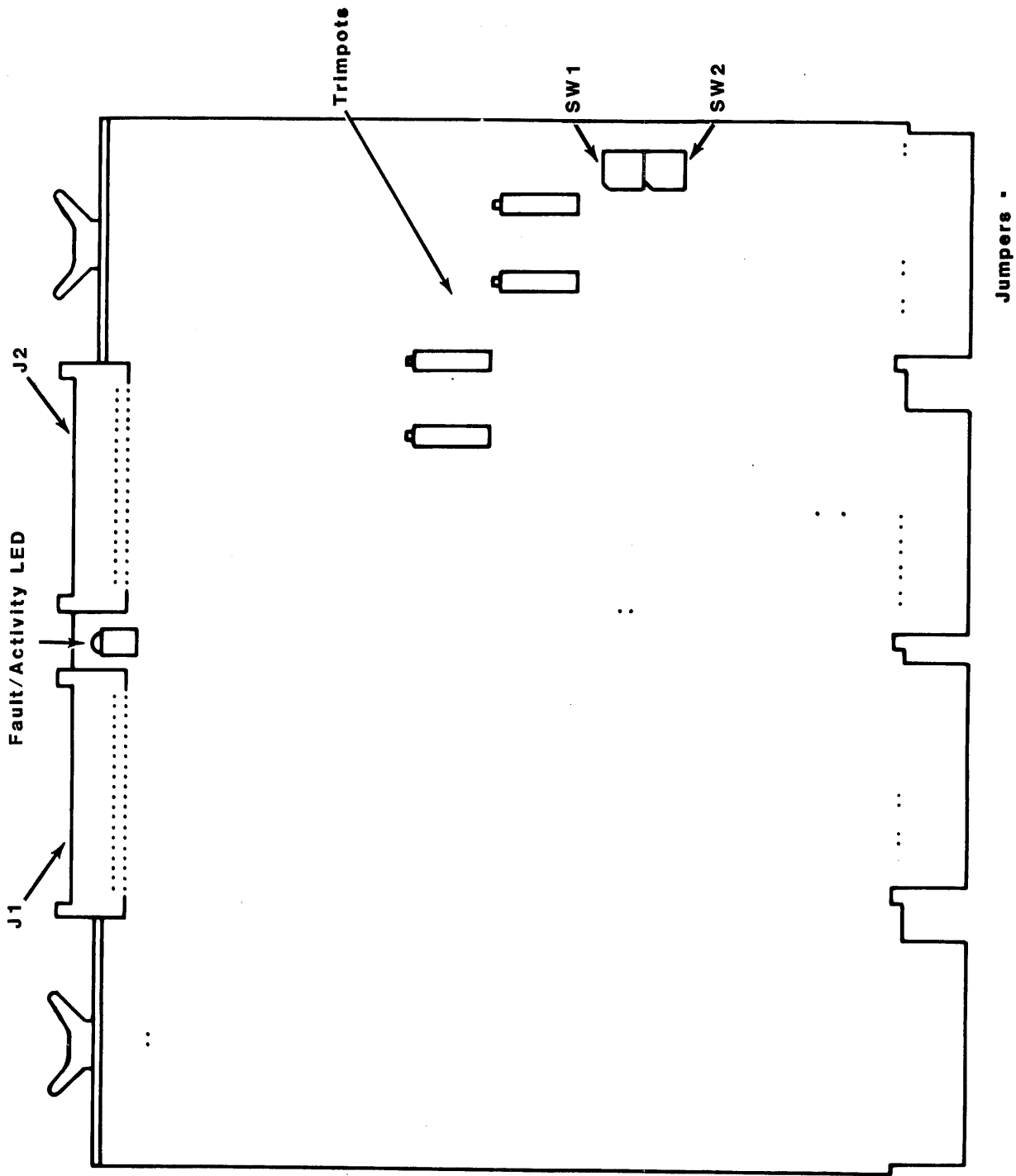


Figure 4-2 PE Read Board Assembly

Table 4-2  
PE VCO Capacitor Values and Periods

Speed 1: Speed 2:		Clock Period	C20 C21	C27 * C28
125	ips	1.0 us	33 pf	0.18 uf
75	ips	1.7 us	68 pf	0.33 uf
45	ips	2.9 us	100 pf	0.33 uf
37.5	ips	3.5 us	150 pf	0.68 uf
25	ips	5.2 us	220 pf	0.68 uf
18.75	ips	6.9 us	270 pf	1.0 uf
15	ips	8.6 us	330 pf	1.8 uf
12.5	ips	10.0 us	430 pf	1.8 uf

\* Capacitor locations for TU1110402 board.

Table 4-3  
Interrupt Vector Addresses

Interrupt Vector	SW2	SW3
224*	OFF	OFF
330	ON	OFF
370	ON	ON
374	OFF	ON

\* Standard vector

#### 4.5.2 Mounting

The controller board should be plugged into the Unibus backplane with components oriented in the same direction as the CPU and other modules. Always insert and remove the boards with the computer power OFF to avoid possible damage to the circuitry. Be sure that the board is properly seated in the throat of the connector before attempting to secure the board by means of the extractor handles.



#### 4.5.2.1 NPG Signal Jumper

The NPG signal jumper between pins CA1 and CB1 on the backplane must be removed so that the NPG signal passes through the controller.

### 4.6 CABLING

The controller board has two 40-pin connectors, one for control (J2) and one for read/write data (J1). Pin one of each cable connector is identified by an arrow. The control cable is connected to connector J101 of the tape transport. The data cable supplied by Emulex connects to both J102 and J103 of the tape transport. For NRZI operation without the PE formatter board, the data cable plugs directly into J1 of the controller. For dual density operation, the data cable plugs into J2 of the PE Read Board and J1 of the controller is connected to J1 of the PE Read Board by a short jumper cable which is supplied with the board. This jumper cable connects certain control signals to the PE Read Board in addition to the read and write data lines. Cabling is shown in Figures 4-3 and 4-4.

#### 4.6.1 Grounding

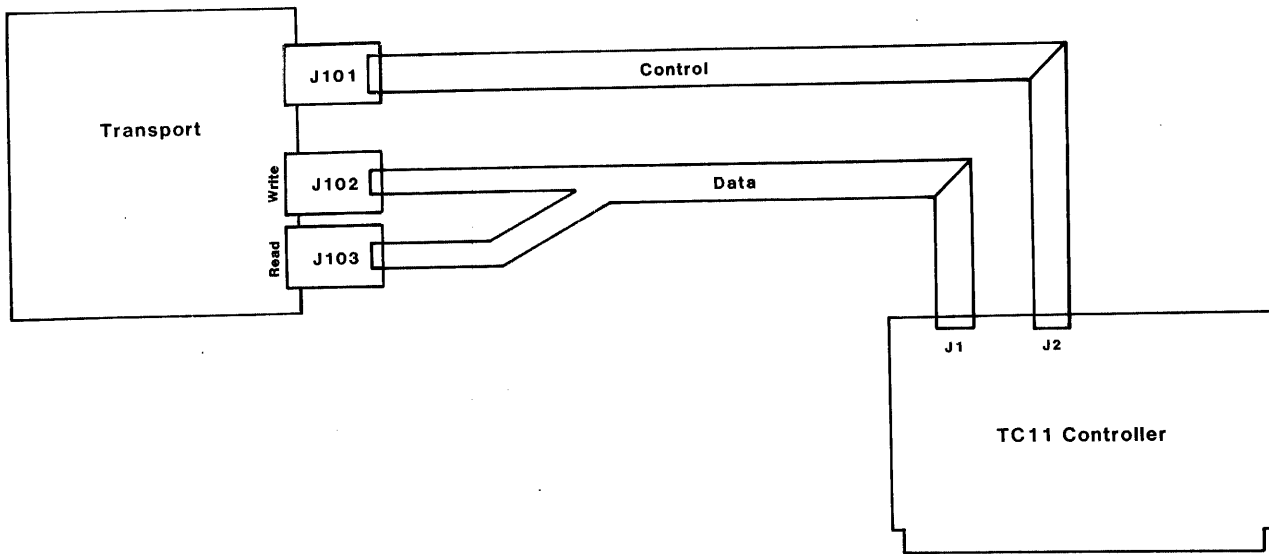
For proper operation of the tape subsystem, it is very important that the tape drives have a good ground connection to the logic ground of the computer. The ground connection should be a 1/4 inch braid (preferably insulated) or AWG No. 10 wire or larger. The grounding wire may daisy-chain between drives. If the drive has a switch or jumper which connects the logical signal ground to the cabinet ground (DC ground to AC ground), this connection should be removed once the drive is put on-line with the controller. It can be connected for performing local off-line maintenance on the drive.

**NOTE:** Failure to observe proper grounding methods will generally result in marginal operation with random error conditions.

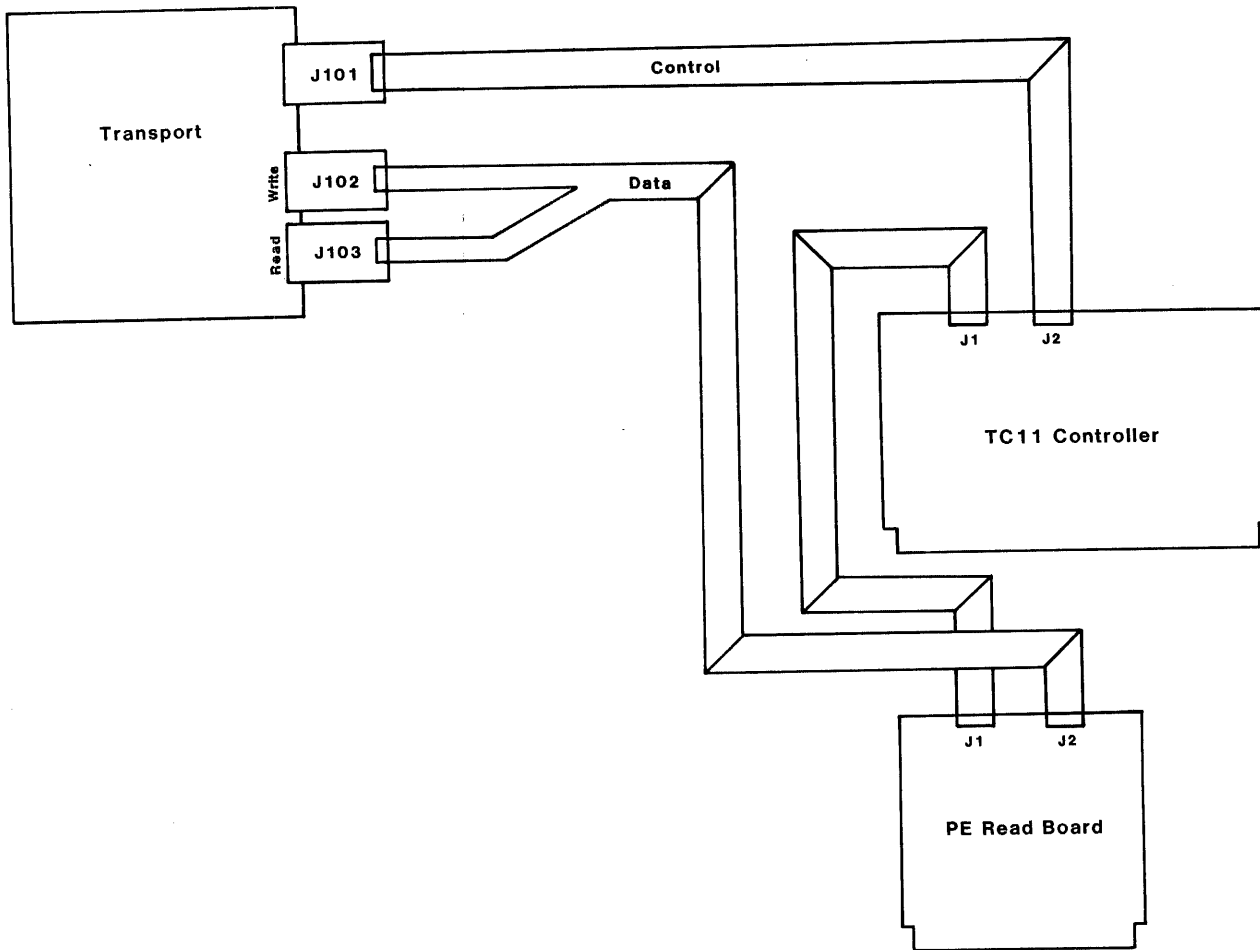
### 4.7 TESTING

#### 4.7.1 Self-Test

When power is applied to the CPU, the controller will automatically execute a built-in self-test. This self-test is not executed with every bus INIT but only on powering-up. If the self-test has been executed successfully, the Fault LED on the front edge of the controller board will be OFF or flashing. The Fault LED flashes when the controller cannot properly address at least one drive after successfully executing its self-test. This will occur if the cables are not properly plugged in, a drive is not powered-up with a proper address, or two drives have an identical address. If the Fault LED is ON steadily the controller did not pass its self-test and the controller cannot be addressed from the CPU.



**Figure 4-3 NRZI Cabling Diagram**



**Figure 4-4 PE Cabling Diagram**

#### 4.7.2 Register Examination

After powering-up the CPU and noting that the Fault LED indicator is not ON, a quick check should be made to ensure that the controller registers can be read. The MTS register will contain 000141 if the tape transport is on-line and the tape is loaded at the BOT.

#### 4.7.3 Diagnostics

DEC does not support the TM11 on the VAX line of computers and consequently there are no DEC diagnostics. Emulex provides diagnostics for the support of the TC11. The part numbers for the Emulex diagnostics are VX9960401 (11-750) and VX9960501 (11-780). See the literature supplied with the diagnostic for installation and operation instructions. The TC11 controller executes the following DEC TM11/TU10 diagnostics in both NRZI and PE modes:

ZTMA	-	Instruction Test *
ZTMH	-	Multidrive Data Reliability Exercise
ZTME	-	Drive Function Timer *
ZTMG	-	Utility Driver
ZTMD	-	Data Reliability 9 Track

\*Requires minor patch

Only the Instruction Test (ZTMA) and the Data Reliability Exerciser (ZTMD) need be run. The diagnostics can be loaded from an XXDP media. If loaded from tape, it will be necessary to zero location 40g to allow execution of the diagnostics.

#### 4.8 SOFTWARE DRIVER INSTALLATION

The VAX/VMS Operating System does not support the TM11, and consequently, it does not support the TC11. Emulex provides a VMS software driver however, to allow the TC11 to be used on both the VAX-11/750 and- 11/780. The Emulex part numbers are VD9960401 (11-750) and VD9960501 (11-780). Both drivers are fully compatible with VMS. The software is supplied with its own operation and installation manual.

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## Appendix A

### TC11 SWITCH SETTINGS

#### A.1 Tape Speed Switch

Switch SW1 sets the tape speed. See Table 4-1 for the settings.

#### A.2 Option switch

Optional features on the TC11 are set by SW2. Table A-1 lists the options enabled by this switch.

Table A-1  
Option Switch Settings

Option Switch	Function
SW2-1	Not used.
SW2-2	Interrupt Vector Address <sup>1</sup>
SW2-3	Interrupt Vector Address <sup>1</sup>
SW2-4	Invert DDI sense line polarity. <sup>2</sup>
SW2-5	Allows PE Read Board self-test to run continuously and not stop on errors. (Diagnostic use).
SW2-6	Disables Unibus activity portion of self-test on power-up.

<sup>1</sup>See Table 4-3.

<sup>2</sup>See paragraph 4.3.6.1

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## Appendix B

### DIAGNOSTICS

#### B.1 RUNNING THE DIAGNOSTICS

DEC does not support the TM11 on the VAX line of computers and consequently there are no DEC diagnostics. Emulex provides diagnostics for the support of the TC11. The part numbers for the Emulex diagnostics are VX9960401 (750) and VX9960501 (780). See the literature supplied with the diagnostic for installation and operation instructions. The TC11 controller executes the following DEC TM11/TU10 diagnostics in both NRZI and PE modes:

ZTMA	-	Instruction Test *
ZTMH	-	Multidrive Data Reliability Exercise
ZTME	-	Drive Function Timer *
ZTMG	-	Utility Driver
ZTMD	-	Data Reliability 9 Track

\*Requires minor patch

#### B.2 DIAGNOSTIC PATCHES

##### B.2.1 ZTMAH - Instruction Test

<u>Location</u>	<u>From</u>	<u>To</u>	
11000	13	60013	DEC patch
12164	100	177701	DEC patch
06322	177774	177400	Account for prefetch at BTE test
05456	22737	122737	Program bug in 7-track mode
14132	5077	5777	Bug with some CRT interfaces

##### B.2.2 ZTMEE - Function Timer

02056	1374	240	No write-erase time
06412	1403	3403	Change to mag. test for word trn.

Subtract  $16_8$  for addresses in ZTMED version.

##### B.2.3 ZTMHF - Data Reliability Test

20314	215	15	Possible parity problem with CRT
20336	260	60	(No problem, no patch!)
20352	270	70	

Subtract 6 for addresses in ZTMHE version.

### B.3 TM11 INSTRUCTION TEST ERROR HALTS

The following addresses are applicable when using Emulex diagnostics. The addresses for DEC diagnostics differ. See your DEC manual for addresses and test error halts for DEC products.

<u>Address</u>	<u>Reason</u>
1262, 1300, 1314, 1330	INIT didn't clear a register
1344, 1360, 1376	INIT didn't clear a register
1420, 1442, 1462, 1502	Power clear didn't clear a register
1522, 1542, 1564	Power clear didn't clear a register
1606	RDY and function bits not set
1636	Function bits not cleared
1660, 1702, 1724, 1736	Function bits not correct
1746, 1770, 2012, 2032	Function bits not correct
2056	RDY and Addr bits in MTC not set
2106	Address bits not cleared
2366, 2406, 2432	Address bits not set properly
2454	RDY and Unit Sel not set in MTC
2504	Unit Select bits not cleared
2526, 2550, 2572, 2614	Unit Select not proper
2636, 2660, 2702	Unit Select not proper
2724	Even parity not set
2754	Even parity not cleared
2776	RDY and Density bits not set in MTC
3026	Density bits not cleared
3050, 3072, 3114	Density bits not proper
3146	MTBC not holding proper value
3206	MTCMA not holding proper value



3246 MTDB not holding proper value  
3276 Bit 14 of MTRD not equal to 0  
3316 Bit 14 of MTRD not equal to 1  
3340 Tape not ready in MTS  
3354 RWS is set in MTS  
3320 Write lock is set in MTS  
3404 Settle down is set in MTS  
3430 Channel 7 selected in MTS  
3446 Channel 7 not selected in MTS  
3470 Tape not at BOT  
3504 Tape not on-line  
3566 Tape not at BOT  
3640 BOT not cleared in MTS on 1 byte write  
3650 RDY not set in MTC on 1 byte write  
3660 MTBC didn't increment to 0 on 1 byte write  
3672 MTCMA didn't increment on 1 byte write  
3756 RDY not set in MTC after 3 byte write  
3770 MTCMA didn't increment after 3 byte write  
4000 MTBC didn't increment to 0 after 3 byte write  
4010 ERR bit in MTC set after 3 byte write  
4104 RWS not set in MTS on rewind  
4114 TUR not reset in MTS on rewind  
4146 BOT not set when SDWN set after rewind  
4166 TUR not set after SDWN cleared on rewind  
4222 BOT set after rewind  
4274 BOT not reset after read from BOT  
4304 RDY not set in MTC after read

4314 MTBC didn't increment to 0 on read  
4326 MTCMA didn't increment on 1 byte read  
4412 RDY not set in MTC on 3 byte read  
4424 MTCMA didn't increment on 3 byte read  
4434 MTBC didn't increment to 0 on 3 byte read  
4444 ERR bit set in MTC on 3 byte read  
4530 MTBC shouldn't increment on write EOF  
4542 MTCMA shouldn't increment on write EOF  
4612 EOF in MTS not set on space into EOF  
4622 ERR in MTC not set on space into EOF  
4634 MTBC should have incremented from -2 to -1  
4646 MTCMA should not have incremented  
4666 Power clear didn't clear EOF  
4730 EOF not set in MTS after backplane into EOF  
4742 BOT should not be set on backplane into EOF  
4756 MTBC should have incremented from -2 to -1  
4766 MTCMA should not have incremented  
5156 EOF should not be set; spaced too far  
5204 EOF should be set on space into EOF  
5216 MTBC should = 1 on space into EOF  
5260 EOF should be set after backspace into EOF  
5304 MTBC should = 0 on backspace  
5310 MTCMA shouldn't increment on backspace  
5322 Backspace should not have reached BOT  
5430 EOF not set during read  
5452 EOF didn't transfer 23, 23 during 9T read  
5466 EOF didn't transfer 17, 17 during 7T read

5636 RLE not set on read  
5646 ERR not set on read  
5660 First two bytes not correct on RLE test  
5672 Third byte not proper or something fourth byte  
5712 Power clear didn't clear RLE  
6004 ILC not set on write to MTC while busy  
6014 ERR didn't set  
6060 Unit 7 should not indicate on-line  
6104 ILC should have set on rewind to Unit 7  
6122 ERR should have set  
6210 ILC should have set on backspace at BOT  
6222 Not at BOT after backspace at BOT  
6302 ILC should have set on rewind at BOT  
6314 Not at BOT after backspace to BOT  
6402 BTE not set in MTS after simulate bad tape  
6412 ERR not set  
6432 Power clear didn't clear BTE in MTS  
6504 NXM didn't set in MTS on read  
6514 ERR didn't set in MTS on read  
6534 Power clear didn't clear NXM  
6600 Interrupt enable didn't cause interrupt  
6634 Shouldn't have interrupt at this priority  
6720 No interrupt when controller became ready  
7030 No interrupt when controller became ready  
7042 Shouldn't be at BOT after RDY set  
7100 No interrupt on rewind complete  
7124 Write buffer contaminated on write

7300 ERR set during read of patterns; 20. byte record  
7314 Data pattern read not correct  
7420 Data read not equal to data written on long record  
7734 Parity Error not set in MTS read even parity  
10204 Parity Error not set in MTS on write even parity  
10234 LPC not proper  
10246 LPC not equal to 77 in 7T  
10266 Power clear didn't clear PAE  
10306 10KC timer bit in MTRD never 0  
10326 10KC timer bit in MTRD never 1  
10720 Data read not equal data written  
10732 Data read not equal data written  
10756 LPC not = 0 on write CRC test  
10766 CRC written on = CRC calculated  
10766 LPC not equal to CRC on read  
11360 CRC not zero



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