SC12/C SC12/V1

(RK06/RK07 COMPATIBLE)

DISK CONTROLLER

TECHNICAL MANUAL

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Section 1
INTRODUCTION

1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the SC12/C SC12/V1 Disk Controller. In addition, this manual provides diagnostics and application information.

1.2 OVERVIEW

1.2.1 General Description

The SC12 Disk Controller is a one board imbedded controller for PDP-11 and VAX-11 computers manufactured by Digital Equipment Corporation. The controller can be used to interface any large disk having a Storage Module Drive (SMD) interface. The SC12 controller emulates the RK611 disk controller manufactured by Digital Equipment Corporation for use with RK06 and RK07 disk drives.

General Specifications of the controller may be found in Table 1-2.

1.2.2 Controller Models

The SC12/C model is the basic RK06/RK07 emulation for the PDP-11 computers. The SC12/V1 model is functionally similar to the SC12/C, except that it performs four word NPR bursts optimized for the Unibus Adaptor (UBA) of the VAX family computers.

NOTE: The SC12/V1 Controller is supported by VMS Version 3.0 or above.

1.2.3 SC12/C Emulation of RK06 and RK07

The RK611 provides a convenient controller architecture for a wide variety of modern technology type disks. It is supported by all DEC operating systems and is easy to program. Disk subsystem characteristics of the RK611/RK06/RK07 are given in Table 1-1.

The SC12 controller can handle two disk drives of the same or different sizes. The controller configures each drive from the information in a configuration PROM. This technique permits up to 64 different switch selectable combinations of disk drive configurations on the two controller ports.

1.3 FEATURES

1.3.1 Microprocessor Design

The SC12 design incorporates a unique 8-bit bipolar microprocessor to perform all controller functions. The microprocessor approach provides for a reduced component count, high reliability, easy maintainability, and most importantly, the ability to adapt a single set of hardware to a wide range of emulation capabilities through the use of microprogramming. The Emulex controllers achieve functional capability beyond that of the DEC controllers which they emulate, by providing enhancement features such as built-in self-test during power-up, built-in disk formatting and the ability to work with disk drives of various sizes.

1.3.2 Packaging

The SC12 is constructed on a single, quad-size, multi-layer PC board which plugs directly into the CPU chassis or an expansion chassis. No cabling is required between the computer and the disk controller. The controller obtains its power from the chassis in which it is mounted.

1.3.3 Self-Test

The controller incorporates an internal self-test routine which is executed upon power-up. This test exercises all parts of the microprocessor, buffer and disk data logic. Although this test does not completely test all controller circuitry, successful execution indicates a very high probability that the controller is operational. If the controller fails the self-test, it leaves the LED on and the controller cannot be addressed from the CPU.

1.3.4 Buffering

The controller contains a 1K x 8 high-speed RAM buffer. It is used to store the device registers of the controller plus a full 512 byte data sector. This buffering permits multiple sector reads with a 3-to-1 sector interlace format. Buffer operations eliminate the possibility of a data late condition and permit the controller to be operated at low bus priorities.

1.3.5 Error Correction

The controller incorporates a 32-bit error correcting code (ECC) capable of correcting single error bursts of up to 11 bits in length and detecting bursts of longer length. The controller determines the location of the error and the pattern so that the software may correct the data after it is transferred to memory. Two 16-bit check characters are employed with the header of every sector.

1.3.6 Option and Configuration Switches

DIP switches are used to configure the controller for various disk sizes, Unibus addresses and options. It is possible to select one of 64 possible combinations of disk characteristics for the two drives which can be handled by the controller, including mixtures of disk sizes and drive type codes.

1.3.7 Dual-Port Capability

The SC12 controller does not support programmable dual-port capability. Those disk drives that have dual-port hardware may be used in a dual-port configuration if the port select switch is in the Channel I only or Channel II only position. The middle (programmable) position creates errors if two controllers access the drive at the same time.

1.4 FUNCTIONAL COMPATIBILITY

1.4.1 Media Compatibility

In all cases, the headers written on the drives are not standard RK06/RK07 headers. In addition a 3-to-1 (or an optional 2-to-1) sector interleave is generated by the hardware formatter. Packs may be formatted using software commands, or by utilizing the hardware formatting capability of the extended command set. Disk packs formatted with an SC12 controller are media compatible with Emulex SC02/C controllers but not with RK06/RK07 packs or Emulex SC11 and SC21/C packs.

1.4.2 Disk Mapping

Depending upon the type and size of the disk drive, one to eight logical units may be mapped on it. Various mapping organizations are used; most of which do not leave direct 1:1 correlation between the logical and physical addresses. Section 3.3.2 contains more information on disk drive configurations.

1.4.3 Diagnostics

1.4.3.1 SC12/C Diagnostics

Emulex recommends running its SC12/C diagnostics program. The part number for the mag tape is PX9960301, and instructions for running the program may be found in Appendix C. Modifications to DEC diagnostics for the SC12/C may be found in Appendix D.

1.4.3.2 SC12/V1 Diagnostics

The SC12/V1 controller executes the following standard DEC RK06/RK07 diagnostics:

EVREA - Vax RK611 Diagnostic. Emulex supports tests 1-11 and 16-55.
EVRAC - VAX Disk Formatter
EVRAA - VAX Disk and TU58 Reliability Tests

1.4.4 Operating Systems

The SC12 controllers are compatible with DEC operating systems without modifications.

Table 1-1
RK611/RK06/RK07 Disk Subsystem Characteristics

	Specifications	
Characteristics	RK06	RK07
Platters/Drive	2	2
MBytes/Logical Unit	13.8	27.4
Blocks/Drive	27,126	53,790
Tracks/Cylinder	3	3
Cylinders/Drive	411	815
Sectors/Track	22	22
Data Bytes/Sector	512	512
Drives/Controller, Max	8	8
Speed,RPM	2400	2400
Bit Density, (BPI)	4040	4040
Data Rate, (KBYTES/SEC)	204.8	204.8

Table 1-2
General Specification

Functional	
Emulation	DEC RK06 and RK07
Media Format	3-to-1 or optional 2-to-1 sector interlace
Drive Interface	SMD
Drive Ports	2
Error Control	32-bit ECC for data and two 16-bit check characters for headers. Correction of single data error burst of up to 11 bits.
Sector Size	256 words (512 bytes)
Sectors/Track	Selectable for each physical drive
Tracks/Cylinder	Selectable for each physical drive
Cylinders/Drive	Selectable for each physical drive
Drive Type Code	Selectable RK06 or RK07 for each physical drive
Computer Interface	Unibus
Vector Address	
Standard	210
Alternate	150
Priority Level	BR5
Data Buffering	1 Sector (256 words)
Data Transfer	High speed DMA operation
Self-Test	Extensive internal self-test on powering up

Table 1-2 (Cont.)
General Specification

Functional	
Indicator	Activity/Fault LED
Unibus Addresses	
SC12/C (PDP-11)	
Standard	777440
Alternates	776700
	776300
	772040
SC12/V1	
VAX-11/730/750	
Standard	FFFF20
Alternates	FFFDC0
	FFFCC0
	FFF420
VAX-11/780	
Standard	2013FF20
Alternates	2013FDC0
	2013FCC0
	2013F420
Design	High-speed bipolar microprocessor using 2901 bit-slice components
Physical	
Packaging	One Quad-sized board
Mounting	Any SPC slot in CPU or expansion box
Connectors	One 60-pin A cable flat connector and two 26-pin B cable connectors. (Flat cable type.)
Electrical	
Unibus Interface	DEC approved line drivers and receivers
Drive Interface	Differential line drivers and receivers. A cable accumulative length to 35 feet. B cable length to 25 feet.
Power	+5V, 5%, 5 Amp. max.

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Section 2
GENERAL DESCRIPTION

2.1 CONTROLLER ORGANIZATION

A block diagram showing the major functional elements of the SC12 controller is shown in Figure 2-1. The controller is organized around an 8-bit high-speed bipolar microprocessor. The ALU and register file portion of the microprocessor are implemented with two 2901 bit slice components. The microinstruction is 48 bits in length and the control memory of 1K words is implemented with twelve 1K x 4 PROMs.

The controller incorporates a 1K x 8 high-speed RAM buffer which is used to store the controller's device registers and one sector (512 bytes) of data buffering.

The A Cable Register (ACR) provides the storage of all A cable signals going to the disk drives. The inputs from the selected drive are testable by the microprocessor.

Serial data from the drive is converted into 8-bit parallel data and transferred to the buffer via the microprocessor. Likewise, the data access from the buffer by the microprocessor is serialized and sent to the drive under the control of the servo clock received from the drive. A 32-bit ECC Shift Register is used to generate and check the ECC for the data field. The same register is also used to employ two 16-bit check characters for the headers. The actual ECC polynomial operation is done independent of the microprocessor, but the determination of the error position and error pattern is done under the control of the microprocessor.

The Unibus interface consists of 18 address lines and 16 bi-directional data lines. The Unibus also carries interrupt vector address data, data control signals, and control signals for granting and receiving bus mastership. The Unibus interface is used for programmed I/O, CPU interrupts, and data transfers. The microprocessor responds to all programmed I/O and carries out the I/O functions required for the addressed controller register. The microprocessor also controls all DMA operations and transfers data between the Unibus data lines and the buffer.

2.2 PHYSICAL DESCRIPTION

The SC12 controller consists of a single quad-size board which plugs directly into a PDP-11 chassis or a VAX Unibus Adapter. A photograph of the SC12 board is shown in Figure 2-2.

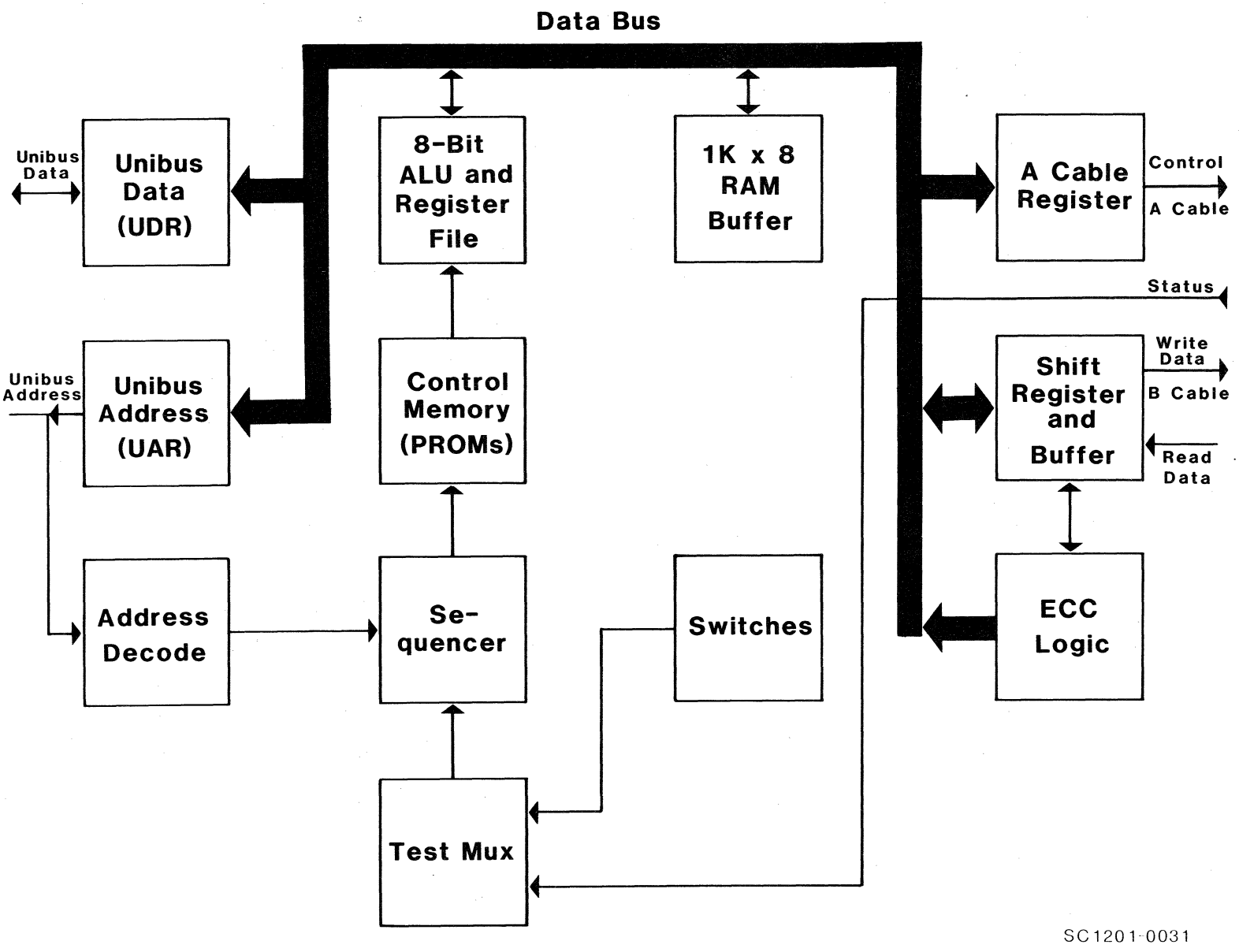
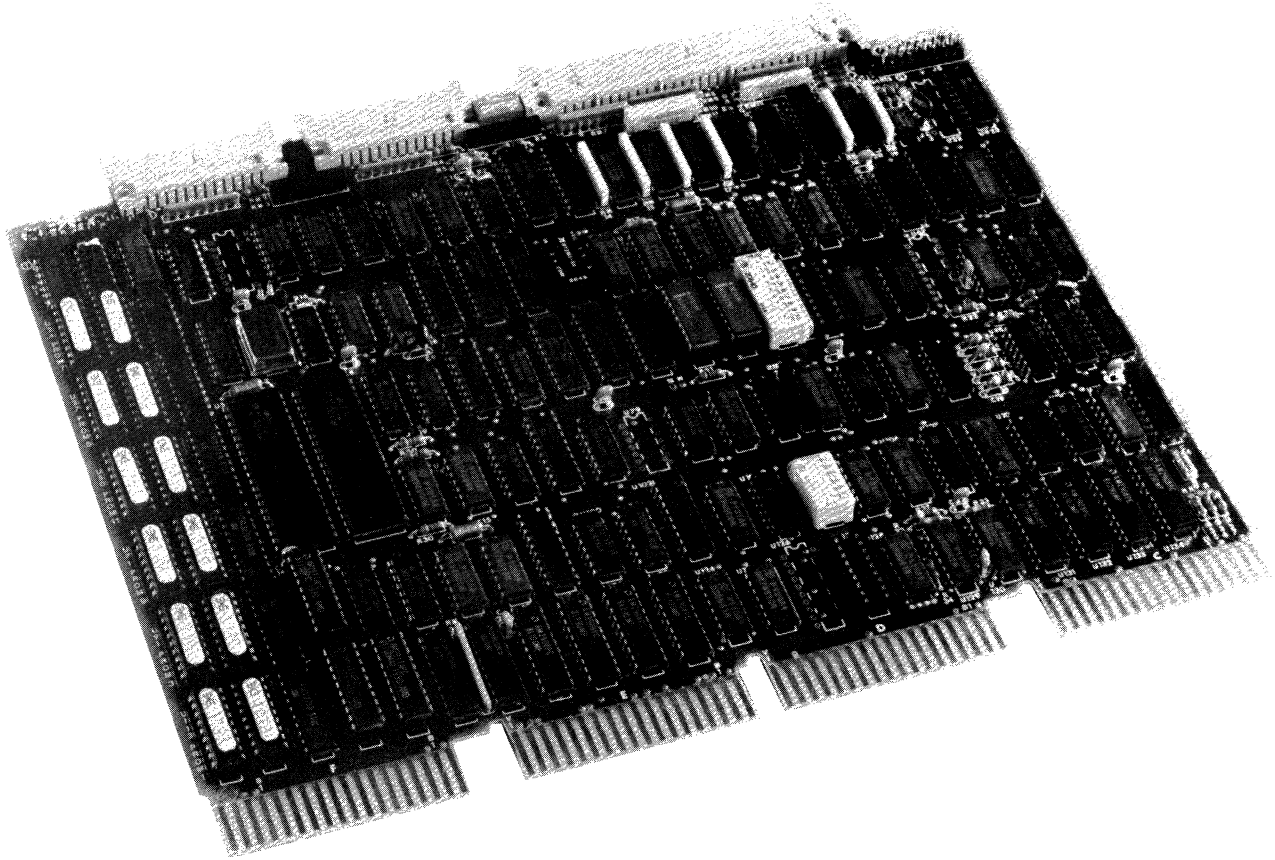


Figure 2-1 SC12 Block Diagram



SC1201-0032

Figure 2-2. SCl2 Controller Board

2.2.1 Connectors

2.2.1.1 A Cable Connector

The 60-pin flat cable connector labeled J3 at the top edge of the board is for the A cable which daisy-chains to all the drives for control and status. Pin 1 is located on the left side of the connector.

2.2.1.2 B Cable Connector

The two 26-pin flat cable connectors labeled J1 and J2 are for the radial B cables to each of two physical drives which may be attached to the controller. Pin 1 is located on the left side of the connector. The two B cable ports are all identical and any drive may be plugged into any connector.

2.2.1.3 Test Connectors

Connectors J4 and J5 are used with the Emulex test panel during manufacturing test and factory repair. They have no use in normal operation.

2.2.2 Switches

There are three sets of switches labeled SW1-SW3. SW1 is a four pole DIP 'piano-type' switch accessible from the PC board edge. The location of SW1 is such that it is accessible to the operator while the controller is imbedded in a Unibus type chassis, making the selection of common options such as hardware format simpler to perform.

The other two sets of switches SW2 and SW3 provide controller address decoding selection, option selection and drive configuration selection. (See Appendixes A and B for complete descriptions of the switch functions.)

2.2.3 LED Indicator

There is an LED indicator mounted between the connectors at the top of the board. The controller executes an extensive self-test when powering up. The microprogrammed organization of the controller permits most logic other than the interface circuitry to the disk to be validated before the controller becomes ready. The LED lamp is turned on as the controller starts its self-test and is turned off only when the controller successfully completes the test. If a malfunction is detected by the built-in diagnostics, the LED remains on and the controller will not respond to program I/O. The LED blinks at approximately a one second rate if the self-test is successful but no drive is seen on-line. The LED also functions as an activity indicator during read and write operations.

2.2.4 Firmware PROMs

There are twelve PROM sockets, used for the control memory, located along the left edge of the board. The sockets are labeled PROM 0 through PROM 11 in a discontinuous physical order. The numbers on the top of the PROM ICs are Emulex part numbers, which identify the unique pattern of the PROM. When inserting PROMs in the board, the ID numbers are placed in the same sequence as the PROM numbers on the board beside each socket.

2.3 INTERFACES

2.3.1 Disk Interface

The controller's disk interface conforms to the Flat Cable Interface Specification for the SMD, MMD, and CMD (CDC Document No. 64712400). The controller has been tested with most drives using the SMD interface and is compatible with these drives electrically and in timing.

The following defines the electrical interface and the recommended cables.

2.3.1.1 A Cable

The 60-conductor A cable is daisy-chained to all drives and terminated at the last drive. The signals in this cable are listed in Table 2-1 along with their function when the control tag (Tag 3) is asserted. The A cable should be 30 twisted pair flat cable with an impedance of 100 ohms and an accumulative length of no greater than 35 feet.

Spectra-Strip P/N 455-248-60 flat cable or its equivalent is recommended. It is possible to order A-Cable assemblies from Emulex that are made up in one of four lengths:

EMULEX P/N	LENGTH (FT.)
SU1111201	8.0
SU1111203	15.0
SU1111205	25.0
SU1111207	35.0

2.3.1.2 B Cable

The 26-conductor B cable is radial to all drives and contains the data and clock signals. The signals and grounds in this cable are listed in Table 2-1. The B cable should be 26 conductor flat cable with ground plane and drain wire. The impedance should be 130 ohms and the length must not be greater than 25 feet.

3M-P/N 3476/26 flat cable or its equivalent is recommended. It is possible to order B-cable assemblies from Emulex that are made up in one of three lengths:

EMULEX P/N	LENGTH (FT.)
SU1111202	8.0
SU1111204	15.0
SU1111206	25.0

2.3.2 Unibus Interface

The controller interfaces to the PDP-11 or VAX-11 Unibus via a Small Peripheral Controller (SPC) connector. The Unibus consists of 18 address lines and 16 bi-directional data lines, plus control signals for data and interrupt vector address transfer and for becoming bus master. The signal connections of the controller to the Unibus are shown in Table 2-2.

2.3.2.1 BR (Interrupt) Priority Level

The controller is hardwired for BR5. The other three Bus Grant signals are jumpered through.

2.3.2.2 Register Address

The register address and the number of registers assigned to the controller are decoded by a PROM at U104. The selections available are determined by configuration switch SW1 as discussed in Appendix A.

2.3.2.3 DCLO and INIT Signals

The DCLO and INIT signals both perform a controller clear. The self-test is performed only if DCLO has been asserted.

2.4 DISK FORMAT

2.4.1 Disk Organization

The formatting of a disk and the mapping of one or more logical drives onto a physical drive varies with the drive size. Some of this information is supplied by the configuration PROM. The rest is computed based upon configuration PROM information. In all cases, the headers actually written on the drives are not standard RK06/RK07 headers. In addition, a 3-to-1 (or an optional 2-to-1) sector interleave is generated by the hardware formatter. Disk packs formatted with an SC12 controller are media compatible with Emulex SC02/C controllers but not with RK06/RK07 packs or Emulex SC11 and SC21/C packs.

Table 2-1
Disk Drive Connections

Pins Lo/Hi	Signal	(Tag 3 Function)	From/To
A Cable:			
22,52	Unit Select Tag		To
23,53	Unit Select bit 0		To
24,54	Unit Select bit 1		To
26,56	Unit Select bit 2		To
27,57	Unit Select bit 3		To
1,31	Tag 1		
2,32	Tag 2		
3,33	Tag 3		
4,34	Bit 0	(Write Gate)	To
5,35	Bit 1	(Read Gate)	To
6,36	Bit 2	(Servo Offset Plus)	To
7,37	Bit 3	(Servo Offset Minus)	To
8,38	Bit 4	(Fault Clear)	To
9,39	Bit 5	(AM Enable)	To
10,40	Bit 6	(Return to Zero)	To
11,41	Bit 7	(Data Strobe Early)	To
12,42	Bit 8	(Data Strobe Late)	To
13,43	Bit 9	(Release)	To
30,60	Bit 10		To
14,44	Open Cable Detect		To
15,45	Fault		From
16,46	Seek Error		From
17,47	On Cylinder		From
18,48	Index		From
19,49	Unit Ready		From
20,50	Not Used		From
21,51	Busy (dual-port only)		From
25,55	Sector		From
28,58	Write Protected		From
29	Power Sequence Hold		To
59	Power Sequence Pick		To
B Cable:			
8,20	Write Data		To
6,19	Write Clock		To
2,14	Servo Clock		From
3,16	Read Data		From
5,17	Read Clock		From
10,23	Not Used		From
22,9	Unit Selected		From
12,24	Not Used		From
13,26	Not Used		From

Table 2-2
SPC Unibus Connections

Column	C		D		E		F	
Pin	1	2	1	2	1	2	1	2
A	NPGIN	+5V		+5V		+5V		+5V
B	NPGOUT					-15V		-15V
C	PA	GND		GND	A12	GND		GND
D		D15		BR7	A17	A15	BBSY	
E		D14		BR6	MSYN	A16		
F		D13		BR5	A02	C1		
H	D11	D12		BR4	A01	A00		
J		D10			SSYN	C0	NPR	
K		D09		BG7IN	A14	A13		
L		D08	INIT	BG7OUT	A11			
M		D07		BG6IN			INTR	
N	DCLO	D04		BG6OUT		A08		
P		D05		BG5IN	A10	A07		
R		D01		BG5OUT	A09			
S	PB	D00		BG4IN				
T	GND	D03	GND	BG4OUT	GND		GND	SACK
U		D02			A06	A04		
V	ACLO	D06			A05	A03		

2.4.2 Mapping

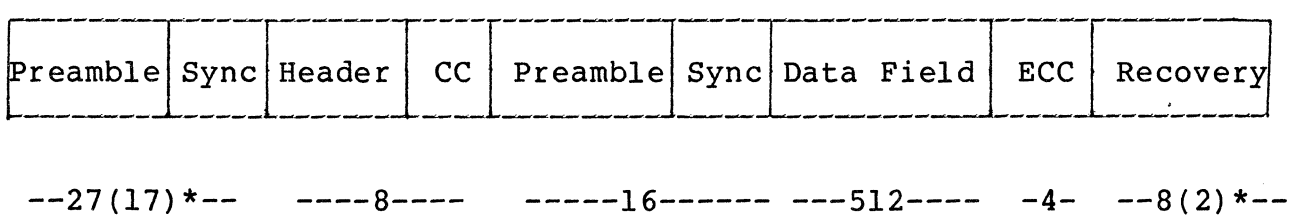
Depending upon the type and size of the disk drive, one to eight logical units may be mapped on it. The controller can handle a maximum of eight logical units distributed across a maximum of two physical disk drives. A logical drive may not be mapped across a physical unit boundary.

The controller firmware multiplies the logical address out to obtain a block address which is then divided by the physical drive configuration constants to provide an address for the physical drive. For this reason a 1:1 correspondence between logical and physical addresses will most likely not exist.

2.4.3 Sector Format

Each sector contains a detached two-word header and a 256 word data field. The header field is terminated with two vertical check characters and the data field is terminated with a 32-bit ECC. The controller attempts corrections only on the data field, never on the header. Each field is preceeded by at least 11 bytes of zeros and an 8-bit SYNC byte. The second header check character is not visible to the software which allows the header to be compatible with existing RK06/RK07 software.

In detail, each sector is organized as shown in Figure 2-3.



*When different than removable media format configuration, numbers for fixed media format configuration are shown in parenthesis.

Figure 2-3 Sector Format

2.4.3.1 Header Field

The header preamble is used to synchronize the Phase Locked Oscillator (PLO) in the drive to the data on the pack. The SYNC byte is used by the controller to synchronize to the data bytes and their boundaries, and by the drive to synchronize to the phase of the data stream. The two header data words are organized as follows:

Word #1 - Logical cylinder address, right justified.

Word #2 - Logical track and sector addresses, in low byte, sector in bits <04:00>, track in bits <07:05>. Flags in high byte, bits 15 and 14 are good sector flags, bit 09 is the 20 sector format flag, and bits 13, 12, and 10 are used to flag a replaced track.

To insure compatibility with RK611 controller software, only one of the check character words, which are identical, is available to the user. The other is written and checked entirely under firmware control to add to header integrity.

The header format is shown in Figure 2-4.

Header Word 1:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	Cylinder Address									

Header Word 2:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
GS Flags		0	0	0	0	FMT	0	Track Addr			Sector Address				

Header Check Character(s):

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Exclusive-OR of Words 1 and 2															

Figure 2-4 Header Format

2.4.3.2 Data Field

The data field preamble and SYNC bytes have the same functions as the header preamble and SYNC bytes. The data field itself is always 256 words long. Any unused portion of the sector will be zero filled during a write operation. The 32-bit ECC is generated during a write, and is used during a read to check the validity of the data. Any single error burst anywhere in the data field of 11 bits or less can be corrected. The error pattern and position are located by the controller, the software may then perform the correction of the data after it is transferred to memory.

2.4.3.3 Postambles

The postambles provide areas for turning off the write amplifiers, for turning on read amplifiers, and for switching from read-to-write. Write splices will exist within all of these areas. The sector pulse postamble will also include a head scatter area on removable media drives.

2.4.3.4 Recovery Area

The recovery area along with the preceeding postamble is required for head scatter tolerances on removable media drives.

2.5 GENERAL PROGRAMMING INFORMATION

2.5.1 Deleted Commands

The SC12 emulates the RK611 controller in its responses to all normal commands and register modifications except the diagnostic mode commands. The diagnostic mode commands (DMD bit in RKMR1 set) will cause the controller to go busy for approximately 40 microseconds after which the controller will become ready and will request an interrupt if interrupts enabled as in other commands; however, the command function will be ignored and not executed.

2.5.2 Extended Commands

The SC12 will execute an extended set of commands not found on the RK611 controller. To execute any of the extended commands, an enable flag must be set prior to issuing the command. To set the enable flag (flag exists only in firmware register), the Spare Register must contain a 1 in bit 15 and a 0 in bit 14 as the RKMR3 register is written (normally a read-only register) with all ones. The enable flag is cleared by a controller reset, subsystem clear, bus INIT, or by executing any command. The following commands are effective only if the enable flag is set. Attempting any extended command except "27" without the enable flag set will result in the illegal function (ILF) bit of RKDS being set along with the controller error (CERR) bit of RKCS1.

1. Hardware Format

   The hardware format command (code 27 in RKCS1) will cause the entire logical drive to be formatted. All headers are written and the data fields are written with the bad sector file format which includes the pack ID number. The number entered into the Spare Register (177462) will be used for the pack ID. The word count, Disk Address Registers and Bus Address Registers are not used in this command. The controller will become ready and will interrupt the processor (if enabled) when finished.

2. Logical Write Protect

This command serves many functions, one of which is to logically write protect a logical drive. This command is executed by writing a "33" command into RKCS1 after which bits <07:00> of the Spare Register will be copied and used as the write protect switches for drives 7-0 respectively. A set bit will cause a drive to be write protected; a reset bit will cause the drive to be not write protected only if the physical disk unit which the drive is mapped onto is also not write protected.

A second function of this command is to load a firmware Switch Register. When the command is executed, bits <13:08> of the Spare Register (177462) are copied to an internal firmware Switch Register. The Switch Register bits are cleared by writing into them with this command or whenever a power-up sequence occurs on the controller. Only one switch (bit 09) is used presently. Its function when set, is to limit the number of disk revolutions before a header search may abort to one revolution. Normally the search is continued for four revolutions except for write check commands, for which it is limited to one revolution also.

A third function of this command is to fill the data silo (177464) with the first 255 words of the Firmware Register block which contains the Controller Registers and configuration constants. Successive reads of the silo may then enable software to read this information for diagnostic purposes.

As with other commands, the controller will become ready and interrupt the processor (if enabled) when its function is completed.

3. Read Unit Headers

This command is used primarily to verify tracks of headers written to implement the track replacement function. It is executed by writing a "35" command in RKCS1. It differs from a standard read header command in that an entire track of headers (physical unit track) is read to the silo with one command. The headers are in order starting with the one after the index pulse and following the three to one interlace pattern until the last header is read. The RKDC and RKDA Registers must be loaded prior to this command with the desired physical cylinder and track to be read, as in the special write header command.

4. Write Unit Headers

This command is executed by writing a "37" command into RKCS1. Its primary function is to write headers to implement the track replacement function. It is similar to a normal write header command except that physical unit addresses are used instead of logical drive addresses. Before issuing the command, the RKDC Register must contain the physical cylinder address, the RKDA Register must contain the physical track address (no sector data - just 10 bits of right justified track address), and the RKWC and RKBA Registers must point to a memory block with the data to be written in the headers and with enough data for an entire physical disk track of headers.

To implement the track replacement function, the track to be replaced must be filled with headers of the following pattern:

1st Word - new physical cylinder address

2nd Word - new physical track address with bits 13, 12, and 10 additionally set to flag the track replace mode

3rd Word - exclusive "OR" of words one and two

The replacement track must then be written using this command with the normal header format as would be found on the replaced track.

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Section 3
INSTALLATION

This section describes the step-by-step procedure for installation of the SC12 Disk Controller in a PDP-11 or a VAX-11 system. The following list is an outline of the procedure. Each step corresponds to a second level heading in this section (i.e., item one, Inspect the SC12, is covered in paragraph 3.1).

Emulex recommends that Section 3 be read in its entirety before installation is begun.

1. Inspect the SC12.
2. Prepare the disk drives.
3. Configure the SC12.
4. Install the SC12.
5. Route the drive I/O cables.
6. Test the controller.

3.1 INSPECTION

Before unpacking the SC12, examine the packaging for any signs of damage. Notify the carrier if any damage is noted.

A visual inspection of the board is recommended after unpacking. Specific checks should be made for such items as bent or broken connector pins, damaged components or any other visual evidence of physical damage. The PROMs should be examined carefully to insure that they are firmly and completely seated in the sockets.

3.2 DISK DRIVE PREPARATION

3.2.1 Drive Placement

Uncrate and install the disk drives according to the manufacturer's instructions. Position and level the disk drives in their final places before beginning the installation of the SC12. This allows the I/O cable routing and length to be accurately judged. Place the drives side by side to make installation of the daisy-chained A Cable simpler.

3.2.2 Local/Remote

The LOCAL/REMOTE switch controls whether the drive can be powered up from the drive (local) or the controller (remote). Place the switch in the REMOTE position. With the controller powered down, press the START switch on the front panel of each of the drives

(the Start LED will light, but the drive will not spin up and become ready). When the controller is powered up, the drives will spin up sequentially. This prevents the heavy current draw that would be caused if all of the drives were powered up at once. When in the REMOTE mode the drives will power down when the controller is powered down. While the controller is powered on, the drives may be powered up and down sequentially (to change disk media, for example) using the START switch.

3.2.3 Sectoring

See Appendixes A and B, Configuration Selection, for the correct sector count settings for the disk drives in use. The exact method of entering the sector count differs from one drive manufacturer to another and the particular drive manual should be consulted for the exact procedure.

3.2.4 Unit Addressing

An address of 0 or 1 must be selected for each drive. Be careful not to give both drives the same number. CDC drive addresses are selected by means of an ID plug. Drives by other manufacturers have their addresses selected by switches on one of the logic cards. Consult the particular drive manual for the exact procedure.

3.3 CONTROLLER SETUP

Several configuration setups must be made on the controller before inserting it into the chassis. These are made by SW1,SW2 and SW3. An assembly drawing of the SC12 is shown in Figure 3-1.

3.3.1 Address Selection

The controller register address selection is accomplished by setting SW3-2, SW3-3, SW3-4 and SW3-5. The standard address for the PDP-11 is 777440. The standard address for the VAX-11/730 and 750 is FFFF20, and for the VAX-11/780 it is 2013FF20. Addresses for each register are contained in Section 4. They are listed after each register title and also contained in Table 4-1. A table of switch settings for the standard and alternate addresses may be found below and in Appendix A for the PDP-11 and Appendix B for the VAX-11.

Table 3-1
SC12 Address Selection

Switch	SC12/C		SC12/V1	
SW3-2	777440	(Standard)	FFFF20	(Standard)
SW3-3	776700	(Alternate)	FFFDC0	(Alternate)
SW3-4	776300	(Alternate)	FFFCC0	(Alternate)
SW3-5	772040	(Alternate)	FFF420	(Alternate)

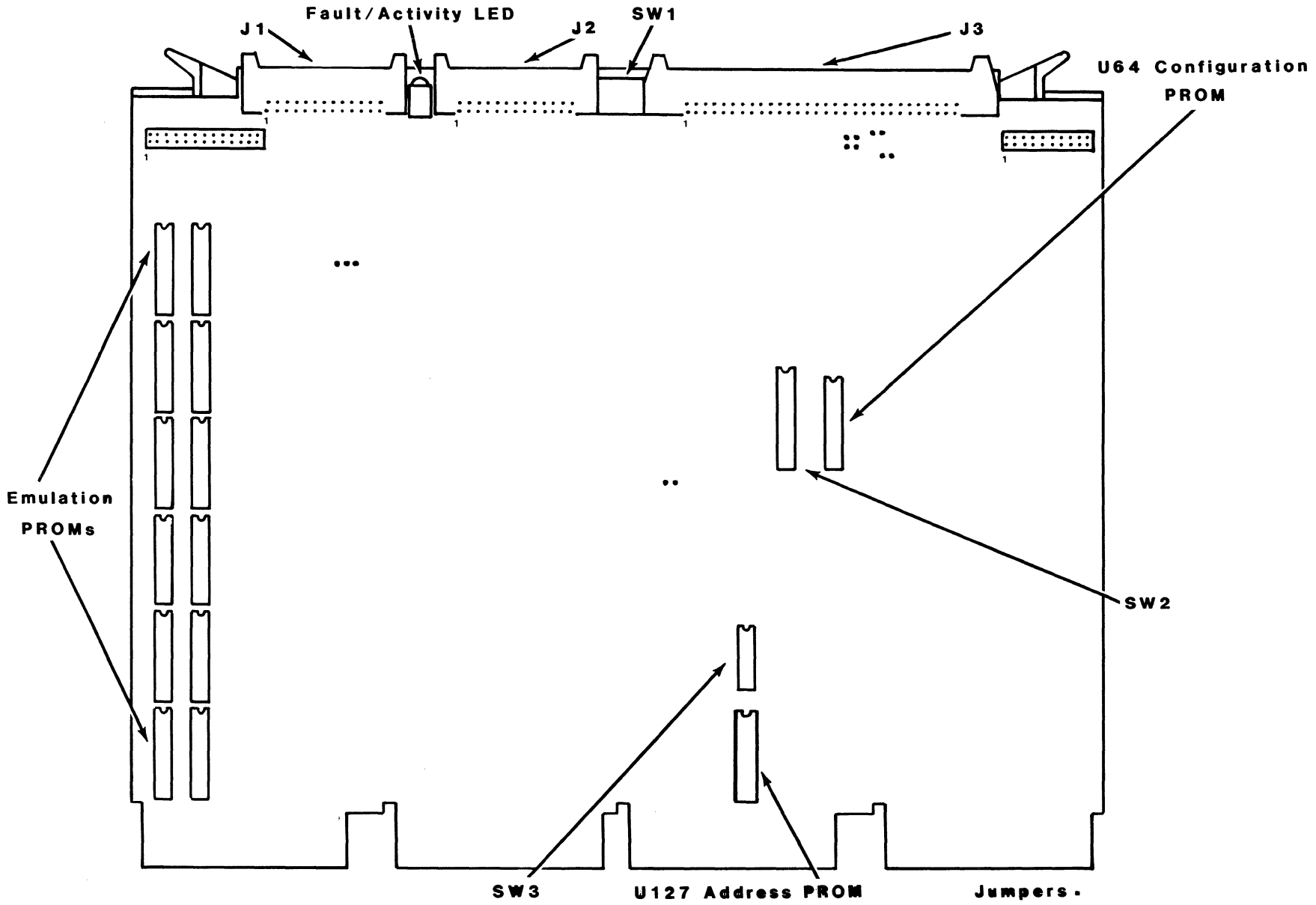

Figure 3-1 SC12 Controller Assembly

3.3.2 Interrupt Vector Address

The interrupt vector address is selected by means of SW2-7. Setting the switch to the open position (OFF) sets the interrupt vector to the standard address of 210. Setting the switch to the closed (ON) position enables the alternate address of 150.

3.3.3 Index and Sector Pulse Selection

The SC12 controller is designed to have the Index and Sector signals on the daisy chained A cable. The presence of the signals on the B cable is not required.

3.3.4 Drive Configuration Selection

The phrase "drive configuration selection" describes the process that is used to select the logical disk drives that will be emulated by the SC12 controllers using a given set of physical disk drives. That is, you have a particular set of physical disk drives. Using those disk drives and the SC12, you wish to emulate a specific type and arrangement of DEC subsystems. (The emulated subsystem is referred to as a logical disk drive.) Setting SW2-1 through SW2-6, SW2-9 and SW2-10 on the controller allows you to select the logical disk drive configuration (limited, of course, by the physical disk drives available). Information on switch settings for configurations is contained in Appendixes A and B.

3.3.5 User Selectable Options

There are a number of SC12 options that can be selected by the user. These features are selected using switches SW1, SW2 and SW3. SW1 is a four pole 'piano type' DIP switch mounted on the outer card edge between connectors J2 and J3. It is accessible while the controller is imbedded in the host computer. SW2 is a ten pole DIP switch, located between U63 and U64. SW3 is a six pole DIP switch, located between U104 and U105.

3.3.5.1 Media Compatibility to Read SC21/C Packs

Option switch SW1-2 allows the SC12/C (but not the SC12/V1) to read SC21/C packs. Setting SW1-2 ON (closed) disables the compare of the second header check character so that the SC21/C packs may be read. To assure maximum header integrity, this function should be used only when needed.

3.3.5.2 Header Check Error Reported as Bad Sector

Setting option switch SW1-3 ON (closed) causes a header check error to be reported as a header with good sector flags reset. The error is thus reported as a bad sector rather than a bad header. This feature should be used for diagnostic purposes only.

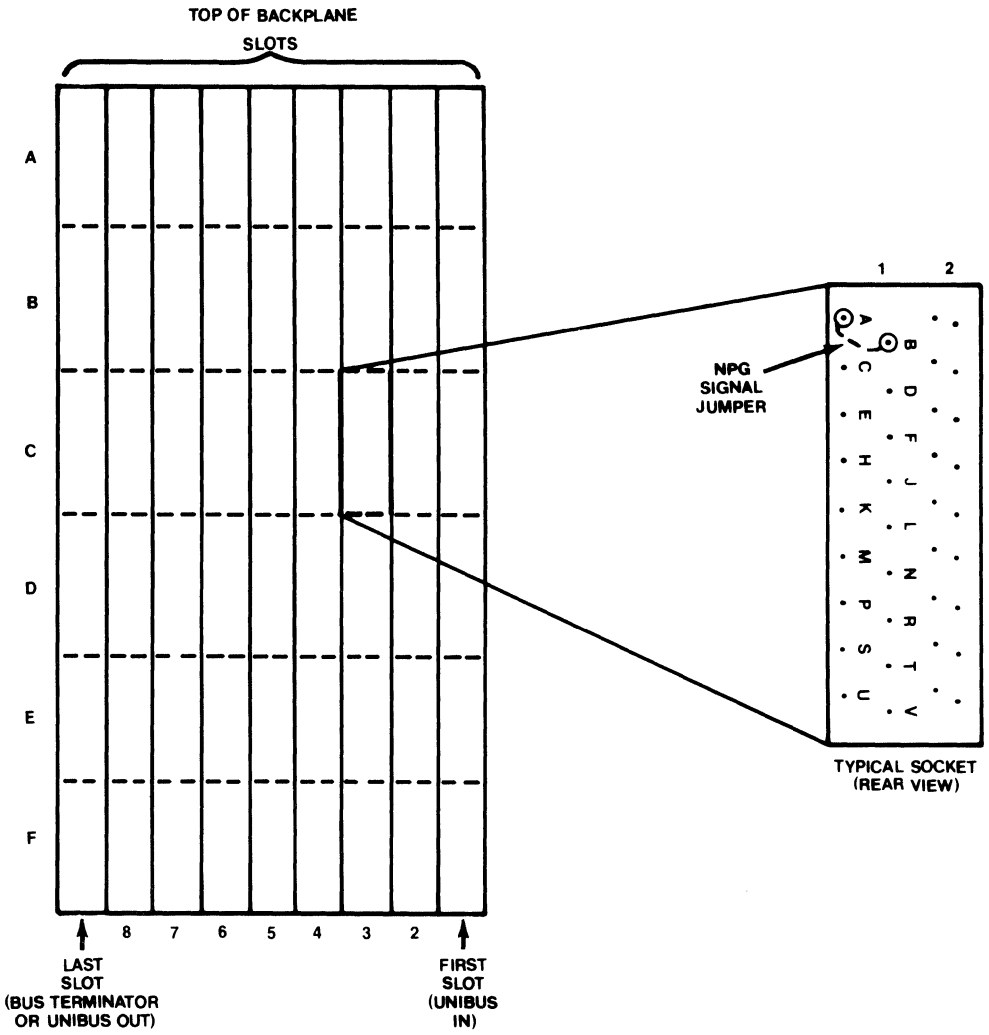

Figure 3-2 NPG Signal Jumper Location

3.3.5.3 All Drives Write-Locked at Power-Up

Enabling SW1-4 causes all the drives to be logically write-locked at power-up, so that data will not be accidentally corrupted. This feature may be used in conjunction with the Write Protect (extended) command (see paragraph 5.4.2). This command provides protection by allowing the user to write lock or unlock each drive separately.

3.3.5.4 Head Offset Capability

Enabling option switch SW2-8 allows head offset commands to be carried out. This feature allows the head carriage in the unit to be offset so that marginal data may be recovered, and should be used only with drives which have offset capability.

3.4 PHYSICAL INSTALLATION

3.4.1 SPC Slot Selection

The controller may be placed in any SPC slot along the Unibus without regard to NPR priority. The controller contains adequate buffering to prevent data lates and will automatically get off the bus if any other device is waiting for the Unibus. If the system contains a Unibus repeater, the controller will not give priority to devices which are on the CPU side of the repeater when the controller is on the far side of the repeater. This may require that the controller be placed on the CPU side of the repeater or that all DMA devices be on the far side of the repeater.

3.4.2 NPG Signal Jumper

The NPG signal jumper between pins CA1 and CB1 on the backplane must be removed so that the NPG signal passes through the controller. See Figure 3-2.

3.4.3 Mounting

The controller board should be plugged into the PDP backplane or VAX-11 Unibus with components oriented in the same direction as the CPU and other modules. Always insert and remove the board with the computer power OFF to avoid possible damage to the circuitry. Be sure that the board is properly positioned in the throat of the connector before attempting to seat the board by means of the extractor handles.

3.5 CABLING

The subsystem cabling of the drives and controller is shown in Figure 3-3.

3.5.1 A Cable

The 60-wire A cable should be plugged into the connector on the A board of the controller and wired to the first drive. If a second drive is used, it is then daisy-chained to it. The last drive on the A cable must have a terminator installed. This part is available from the drive manufacturer. The terminator is generally plugged into one of two A cable connectors on the drive. In some cases, a ground wire emerging from the terminator assembly will have to be connected to the drive to provide a ground return for the resistors in the terminator. Pin 1 of the board connector is on the left. Pin 1 of the cable connector has a notch on the connector body to identify it. Twist and flat cable will have brown-brown twist followed by red-brown twist on the pin 1 edge of the cable. The recommended cable part numbers is discussed in Section 2.3.1.1.

NOTE: The connector is not keyed and can be physically reversed in the header. No damage should result, but the system will not operate.

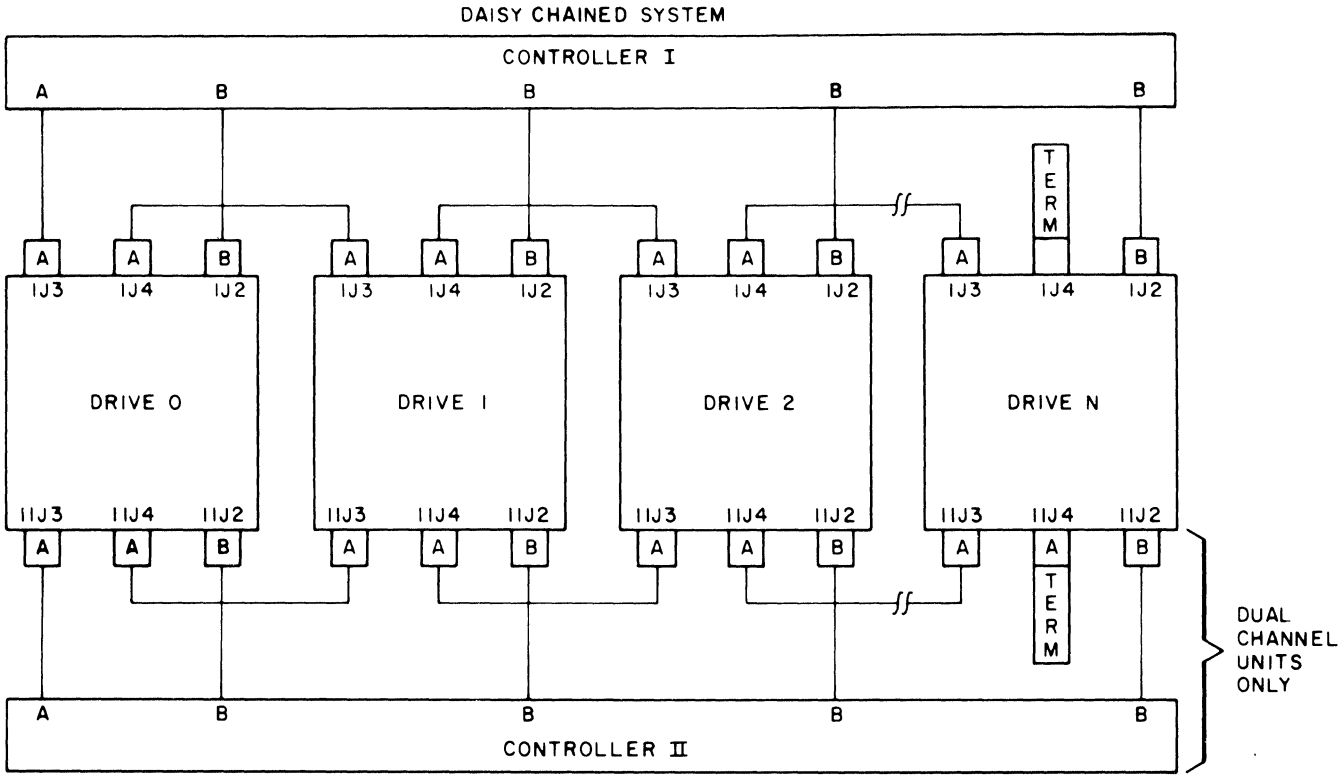

Figure 3-3 SC12 Cabling Diagram

3.5.2 B Cable

Each drive must have a 26-wire B cable wired from the drive to one of the B ports of the controller. It makes no difference which B port connection is used by a drive. No external terminators are used with the B cable. Pin 1 of the cable connector has a notch on the connector body to identify it. The pin 1 edge of the cable has a black stripe. The recommended cable part number is discussed in section 2.3.1.2.

NOTE: Observe the same caution on connector reversal given in paragraph 3.5.1.

3.5.3 Grounding

For proper operation of the disk subsystem, it is important that the disk drives have a good ground connection to the logic ground of the computer. The ground connection should be a 1/4 inch braid (preferably insulated) or AWG No. 10 wire or larger. The grounding wire may daisy-chain between drives. If the drive has a switch or jumper which connects the logical signal ground to the cabinet ground (DC ground to AC ground), this connection should be removed once the drive is put on-line with the controller. It can be connected for performing local off-line maintenance on the drive.

NOTE: Failure to observe proper grounding methods will generally result in marginal operation with random error conditions.

3.6 TESTING

3.6.1 Self-Test

When power is applied to the CPU, the controller automatically executes a built-in self test. This self test is not executed with every bus INIT but only on powering up. If the self test has been executed successfully, the LED on the top edge of the controller board will be OFF or flashing. The LED flashes when the controller cannot properly address at least one drive after successfully executing its self test. This will occur if the A and B cables are not properly plugged in, a drive is not powered up with a code plug, or two drives have an identical code plug. If the LED is ON steadily the controller did not pass its self test and the controller cannot be addressed from the CPU.

3.6.2 Register Examination

After powering up the CPU and noting that the LED indicator is not ON steadily, a quick check should be made to ensure that the controller registers can be read from the computer console. The Control Status Register (RKCS1) will contain 000200 if the controller is ready. To determine the on line status of the selected drive check the Drive Status Register (RKDS) (see Section 4). If the CPU has a console emulator all the registers of the controller should be examined.

3.6.3 Hardware Formatting the Disk

The controller has the means to format the disk by writing headers and bad sector file data in all sectors of the disk. This command does not verify the data or headers. See Table 4-1 for the register addresses.

If the drive is on line, the formatting is carried out as follows:

1. Perform a subsystem clear by depositing 000040 into RKCS2 (17777450).

2. Select the drive to be formatted by depositing the drive number in the least significant bits of RKCS2 (17777450).

3. Deposit a pack acknowledge command (3_8 for RK06 or 2003_8 for RK07) in RKCS1 (17777440).

4. Deposit a number to be used as a pack ID in the Spare Register (17777462); bit 15 of this number must be set, and bit 14 must be reset or the command will not execute.

5. Deposit all ones in RKMR3 (17777476) which is a "read-only" register, to enable extended command set.

6. Deposit the hardware format command (27_8 for RK06 or 2027_8 for RK07) in RKCS1 (17777440) to start formatting. The operation will finish in a couple of minutes with the RDY bit set in RKCS1. The controller LED will flash as data is being transferred to the disk during the formatting operation.

3.6.3.1 Hardware Format Examples

Three sample hardware formats for an SC12/X RK06/RK07 are listed below. The first two are for use with the PDP, and the third is for use with the VAX. The prompt for the M9301 console emulator is "$", and the prompt for the M9312 console emulator is "@". The VAX prompt is ">>>". All underlined text (or space) is information that must be input by the user. For configurations with more than two logical drives, repeat the procedure inserting the next logical drive number in RKCS2. Keep in mind that the sample below is only an example and the user must enter the addresses appropriate to his particular system.

Logical Drives 0-7 on a M9312 Console Emulator

Function	Entries and Displays	Description
1. DEP (RKCS2)	@17777450/000100 40	Subsystem clear
2. DEP (RKCS2)	@/000100 X	Select next logical drive
3. DEP (RKCS1)	@17777440/000200 XXXX	Pack acknowledge (RK06=0003, RK07=2003)
EXAM (RKCS1)	@/00XXXX	RK06=0202, RK07=2202
4. DEP (SP REG)	@17777462/000000 10000X	Pack I.D. next logical drive
5. DEP (RKMR3)	@17777476/000000 177777	Enable extended Op Code*
6. DEP (RKCS1)	@17777440/00X202 XXXX	Format command (RK06=0027, RK07=2027)
EXAM (RKCS1)	@/00X027	Format in progress (RK06=0, RK07=2)
EXAM (RKCS1)	@17777440/00X226	Format complete (RK06=0, RK07=2)

*Do not EXAM 17777476 after DEPOSITing all ones, as this will disable extended Op Code function.

Logical Drives 0-7 on a M9301 Console Emulator

Function	Entries and Displays	Description
1. DEP (RKCS2)	$L 17777450/<CR> 000100 D 40	Subsystem clear
2. DEP (RKCS2)	$L /000100<CR> D X	Select next logical drive
3. DEP (RKCS1)	$L 17777440/<CR> 000200 D XXXX	Pack acknowledge (RK06=0003, RK07=2003)
EXAM (RKCS1)	$E /00XXXX	RK06=0202, RK07=2202
4. DEP (SP REG)	$L 17777462/<CR> 000000 D 10000X	Pack I.D. next logical drive
5. DEP (RKMR3)	$L 17777476/<CR> 000000 D 177777	Enable extended Op Code*
6. DEP (RKCS1)	$L 17777440/<CR> 00X202 D XXXX	Format command (RK06=0027, RK07=2027)
EXAM (RKCS1)	$E /00X027	Format in progress (RK06=0, RK07=2)
EXAM (RKCS1)	$E 17777440/00X226	Format complete (RK06=0, RK07=2)

*Do not EXAM 17777476 after DEPOSITing all ones, as this will disable extended Op Code function.

Logical Drives 0-7 on a VAX

Function	Entries and Displays	Description
1. DEP (RKCS2)	>>>D 17777450/ 000100 40	Subsystem clear
2. DEP (RKCS2)	>>>D /000100 X	Select next logical drive
3. DEP (RKCS1)	>>>D 17777440/000200 XXXX	Pack acknowledge (RK06=0003, RK07=2003)
EXAM (RKCS1)	>>>E /00XXXX	RK06=0202, RK07=2202
4. DEP (SP REG)	>>>D 17777462/000000 10000X	Pack I.D. next logical drive
5. DEP (RKMR3)	>>>D 17777476/000000 177777	Enable extended Op Code*
6. DEP (RKCS1)	>>>D 17777440/00X202 XXXX	Format command (RK06=0027, RK07=2027)
EXAM (RKCS1)	>>>E /00X027	Format in progress (RK06=0, RK07=2)
EXAM (RKCS1)	>>>E 17777440/00X226	Format complete (RK06=0, RK07=2)

*Do not EXAM 17777476 after DEPOSITing all ones, as this will disable extended Op Code function.

3.6.4 Diagnostics

3.6.4.1 SC12/C Diagnostics

Emulex recommends running its SC12/C diagnostics program. The part number for the mag tape is PX9960301, and instructions for running the program may be found in Appendix C. Modifications to DEC diagnostics may be found in Appendix D.

3.6.4.2 SC12/V1 Diagnostics

The SC12/V1 executes the following standard DEC RK06/RK07 diagnostics in the Vax family computers:

EVREA - Vax RK611 Diagnostic. Emulex supports tests 1-11 and tests 16-55.
EVRAC - Vax Disk Formatter
EVRAA - Vax Disk and TU58 Reliability Tests

BLANK

There are 16 device registers in the controller. These are used to interface the controller to the computer. The registers are loaded and/or read under program control in order to initiate selected disk commands, and monitor status and error conditions.

NOTES - The registers must be written with word operations. All register addresses are listed in the order of PDP-11, VAX-11/730, 750 and VAX-11/780. Table 4-1 contains a more complete listing of the register addresses.

4.1 CONTROL/STATUS REGISTER 1 (RKCS1) 777440, FFFF20, 2013FF20

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CERR CCLR	DI	DTC	CFMT	CTO	CDT	A17	A16	RDY	IE	0	F3	F2	F1	F0	GO
		PAR													

The RKCS1 register can be read or written via program control and is used to store the current disk command code and operational status of the controller. In addition, the register can initiate command execution and controller clear operation.

Combined Error/Controller Clear (CERR/CCLR) - Bit 15

As a Combined Error (CERR) indicator, bit 15 is set by the controller to indicate that a subsystem error has occurred. However, when the bit is set via program control, a controller initialize (CCLR) operation is enabled which clears the controller, and results in the clearing of bit 15 itself. Thus, if the bit is internally set (CERR) by an error that is followed by an external set (CCLR) to initialize the controller, bit 15 will be cleared. However, since only controller errors will be initialized by CCLR, any error originating in a drive will remain set in the drive.

NOTE: When using a BIC instruction on the RKCS1 register, ensure that a 1 is set in bit 15 of the mask. If this is not done, and CERR is set, a CCLR will occur, and the RK611 will be cleared. For example, to clear the Interrupt Enable (IE) bit (bit 06 in RKCS1), the following instruction format is recommended:

```
BIC #100100, @RKCS1
```

Drive Interrupt (DI) - Bit 14

Drive Interrupt is a read-only bit which is set to differentiate between a drive-initiated interrupt and a controller-initiated interrupt.

The DI bit is set when any drive sets its Attention (ATN0-ATN7) bit (<08:15> in RKAS/OF). Thus, if the Interrupt Enable (IE) bit is set, the setting of the DI bit in conjunction with Controller Ready (RDY), bit 07 in RKCS1, indicates a drive-initiated interrupt. The DI bit is reset by Unibus Initialize (INIT), Subsystem Clear (SCLR), or by the execution of Drive Clear commands to all drives asserting Attention.

Drive-To-Controller Parity Error (DTC PAR) - Bit 13

The DTC Parity Error is a read-only bit that is set on the termination of a command if Parity Test (bit 04 of RKMR1) is set. This bit is for diagnostic compatibility only.

Controller Format (CFMT) - Bit 12

This bit must alway be reset to indicate 22 sector format, which is all the controller emulates of the RK06.

Controller Time-Out (CTO) - Bit 11

Controller Time-Out is a read-only error bit that is set to indicate that GO, bit 00 in RKCS1, has been set for approximately 800 ms. Since this interval exceeds the time required to execute the longest possible drive operation (i.e., a Seek from cylinder 410 to cylinder 0 followed by a 65K word data transfer), the set condition of this bit indicates that the last command has not been completed due to a malfunction.

Controller Drive Type (CDT) - Bit 10

This bit specifies the type of drive that will be selected by the controller. To specify RK06 Disk Drives, the bit must be reset.

Extended Bus Address (A16, A17) - Bits <08:09>

The Extended Bus Address bits reflect Unibus upper address bits <16:17>, and as such are an extension of the 16-bit RKBA register which contains the memory address required for the current data transfer.

Controller Ready (RDY) - Bit 07

Controller Ready (RDY) is a read-only bit. The bit can be externally set via conventional initialization (INIT, CCLR, SCLR), or internally set upon completion of a command. The RDY bit is reset when GO, bit 00 in RKCS1, is set.

Interrupt Enable (IE) - Bit 06

When the Interrupt Enable (IE) bit is set, the controller will be allowed to interrupt the processor at the end of a command execution or by any ATN being asserted. An interrupt is generated by writing 1's into IE and RDY at the same time.

Function Code (F3-F0) - Bits <04:01>

The configuration of the Function Code bits (F3-F0), in conjunction with the setting of the GO bit, allows the selected drive to respond to the following command control configuration.

01	Select Drive	21	Read Data
03	Pack Acknowledge	23	Write Data
05	Drive Clear	25	Read Header
07	Unload	27	Write Header
11	Start Spindle	31	Write Check
13	Recalibrate	33	*Set Logical Write Protect
15	Offset	35	*Reset Logical Write Protect
17	Seek	37	*Set Logical Write Protect

Go (GO) - Bit 00

When the GO bit is set, the disk command Function Code (F4-F0) is executed. With the GO bit set, only two other device register bits can be set (Diagnostic Mode excepted), as follows:

- Controller Clear (CCLR), bit 15 in RKCS1, may be set via program control in order to initialize (general clear and preset) certain device registers within the controller. However, any status and/or error conditions set in the drives are not effected.

- Subsystem Clear (SCLR), bit 05 in RKCS2, may be set via program control in order to initialize both the controller and all of the drives.

When command execution is completed, the GO bit is reset and the controller is ready to accept a new command. However, the GO bit cannot be set if the Combined Error (CERR) bit is set. When CERR is set, the execution of a command can only occur following the initiation of a CCLR.

These commands are illegal and will set the ILF bit in the RKER register unless an enabling procedure is performed before each issuance of the command. To enable these commands the spare register must contain a one in bit 15 and a zero in bit 14 while RKMR3 is written with all ones.

4.2 WORD COUNT REGISTER (RKWC) 777442, FFFF21, 2013FF21

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Two's Complement Word Count															

The RKWC is loaded with the two's complement of the number of data words to be transferred to or from main memory. The register is incremented by 1 after each word transferred, and accommodates a

maximum transfer of 65,356 words. The data transfer stops when the RKWC reaches zero. The RKWC is not cleared by INIT or controller clear.

4.3 BUS ADDRESS REGISTER (RKBA) 777444, FFFF22, 2013FF22

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Bus (Memory) Address															

The RKBA register is initially loaded with the low-order 16 bits of the Unibus address of the main memory starting location for a data transfer. The low-order bit 00 is always forced to a 0. The RKBA register is incremented by 2 after transfer of a word to or from memory,if BAI (bit 04, RKCS2) is not set. Overflow of this counter increments A16 and A17 in RKCS1.

4.4 DISK ADDRESS REGISTER (RKDA) 777446, FFFF23, 2013FF23

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	Track Address			0	0	0	Sector Address				

The RKDA is used to address the sector and track on the drive to or from which the data transfer is desired. It contains a 5-bit sector address counter which is incremented by one at the end of every sector transferred. After reaching a maximum count of 21, it resets to 0 and increments the track address by one. The register also contains a 3-bit track address counter which is incremented every time the sector address counter reaches maximum count. When this counter reaches maximum count of 2, it resets to 0 and causes the RKDC register to be incremented by one.

4.5 CONTROL/STATUS REGISTER 2 (RKCS2) 777450, FFFF24, 2013FF24

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	WCE	UPE	NED	NEM	PGE	MDS	0	OR	IR	SCLR	BAI	0	U2	U1	U0

The RKCS2 register can be read or written via program control and is used to store the current drive select code, subsystem operational status, and Silo control information. In addition, the register can initiate a Subsystem Clear (SCLR) operation.

Data Late Error (DLT) - Bit 15

This bit is not set during data transfers because of the full sector buffering used in the controller. It can only be set by accessing RKDB without the OR bit in RKCS2 set.

Write Check Error (WCE) - Bit 14

Write Check Error is a read-only error bit that is set to indicate that a data word read from the disk during the execution of a Write Check command did not compare with the corresponding data word contained in main memory. If a write check error is detected and the BAI bit is not set, the RKBA register will contain the memory address of the next data word location (mismatched word address plus two).

Unibus Parity Error (UPE) - Bit 13

Unibus Parity error is a read only bit that is set if a parity error occurs in the Unibus memory while the controller is performing a Write or Write Check command. When the error occurs, the RKBA register contains the address of the word following the word with the parity error (if BAI is not set).

Non-Existent Drive (NED) - Bit 12

Non-existent Drive is a read-only bit that is set when the program issues a command with the GO bit in RKCS1 set to a drive which is not emulated or is located on a physical unit which is not currently available at one of the controller ports.

Non-Existent Memory (NEM) - Bit 11

Non-existent Memory is a read-only bit that is set when the controller is performing an NPR transfer and the memory does not respond within 10 microseconds. The memory address displayed in RKBA is the address of the word following the memory location causing the error.

Programming Error (PGE) - Bit 10

Programming Error is a read-only error bit that is set if any controller register is written (bits for CCLR and SCLR excepted) while the GO bit in RKCS1 is set.

Multiple Drive Select (MDS) - Bit 09

Multiple Drive Select is a read-only error bit that is set when the controller detects two or more physical disk units responding to the same address.

Output Ready (OR) - Bit 07

Output Ready is a read-only bit that is set to indicate that a word is in the Silo output buffer. The bit is cleared by conventional initialization (INIT, CCLR, SCLR), or by the setting of the GO (bit 00 in RKCS1).

Input Ready (IR) - Bit 06

Input Ready is a read-only bit that is set to indicate that the Silo input buffer is ready to accept a word. Conversely, the bit is reset to indicate that the Silo is full and cannot accept a word. The IR bit is also set by conventional initialization (INIT, CCLR, SCLR), or by the setting of the GO (bit 00 in RKCS1).

Subsystem Clear (SCLR) - Bit 05

When the SCLR bit is set via program control, the controller is cleared and all status for the connected drives is initialized.

Bus Address Increment Inhibit (BAI) - Bit 04

When the BAI bit is set, the RKBA register is prevented from incrementing during data transfers. This is primarily a diagnostic aid.

Unit Select (U2-U0) - Bits <02:00>

The Unit Select bits select one of eight logical drives. These are read/write bits.

4.6 DRIVE STATUS REGISTER (RKDS) 777452, FFFF25, 2013FF25

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SVAL	CDA	PIP	0	WRL	0	0	DDT	DRY	VV	0	SL	ACLO	OFS	0	DRA

The RKDS register is a read-only register that is used to store the operational status of the selected drive. However, information obtained from the drive is not necessarily current or correct unless bit 15 (SVAL) is set.

Status information bits set in the RKDS register can be cleared by conventional initialization (INIT, CCLR, SCLR). However, a Controller Clear (CCLR) operation does not affect status or error condition bits that are currently set in the drives. In addition, a Unibus Initialize (INIT) or Subsystem Clear (SCLR) operation can only reset status or error bits in a drive if the associated status or error condition no longer exists.

Status Valid (SVAL) - Bit 15

Status Valid is a read-only bit that is set to indicate that the bits in both the Drive Status (RKDS) and Error (RKER) registers have been updated for the selected drive. The bit is cleared by conventional initialization (INIT, CCLR, SCLR), initiating a new command (writing into RKCS1), selecting a new drive (writing into RKCS2), or whenever at Attention signal is asserted by the selected drive for a drive status change.

Current Drive Attention (CDA) - Bit 14

Current Drive Attention is a read-only bit that is the logical equivalent of the Drive Status-Change (DSC) bit in the drive defined by the unit select in RKCS1. The assertion of attention indicates that the selected drive has completed a Seek, Offset, Recalibrate, Start Spindle, or Unload command, that the drive has been taken off-line or put on-line by the operator, or that a fault condition exists in the drive.

Positioning-in-Progress (PIP) - Bit 13

Positioning-in-Progress is a read only bit that is set to indicate that the head carriage on the logical drive is in motion.

Write Lock (WRL) - Bit 11

Write Lock is a read-only bit that is set if the selected drive is write protected. A drive may be physically or logically write protected.

Disk Drive Type (DDT) - Bit 08

Disk Drive Type is a read-only bit that is internally conditioned to indicate the type of drive selected. This bit is set to indicate an RK07 drive or reset to indicate an RK06 drive. This bit must compare with the condition of Controller Drive Type, bit 10 in RKCS1, before any command may be executed.

Drive Ready (DRY) - Bit 07

Drive Ready is a read-only bit that is set to indicate that the selected drive is up to speed and the heads are properly positioned over a valid cylinder. Under these conditions, the drive is prepared to receive a command.

Volume Valid (VV) - Bit 06

Volume Valid is a read-only bit that is set to indicate that the Volume Valid flip-flop has been set in the selected drive by a Pack Acknowledge command. The set condition of the bit ensures the program that the cartridge and the unit number plug have not been changed since the last command was issued to the drive, and power has not been removed. The bit is reset when the cartridge, the unit number plug, or ac power is removed from the physical disk unit.

Speed Loss (SL) - Bit 04

This bit is a read-only bit which is always reset for the SC12/C emulation.

Drive AC Low (ACLO) - Bit 03

Drive AC Low is a read-only bit that is always reset.

Offset (OFS) - Bit 02

Offset is a read-only bit that is set to indicate that the selected drive is in Offset mode.

Drive Available (DRA) - Bit 00

Drive Available is a read-only bit that is always set in single port configurations.

4.7 DRIVE ERROR REGISTER (RKER) 777454, FFFF26, 2013FF26

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCK	UNS	OPI	DTE	WLE	IDAE	COE	0	BSE	ECH	DT	FMTE	DPE	NXF	SKI	ILF

The RKER register is a read-only register that is used to store the error status of the selected drive. However, error information obtained from the drive is not immediately available to program control until the information is validated by the setting of SVAL (bit 15 in the RKDS register), which indicates that a complete status message frame has been received.

Error bits set in the RKER register can be cleared by conventional initialization (INIT, CCLR, SCLR). However, a Controller Clear (CCLR) operation does not affect error bits that are currently set in the drive. In addition, a Unibus Initialize (INIT) or Subsystem Clear (SCLR) operation can only reset error bits in a drive if the associated error condition no longer exists.

Data Check (DCK) - Bit 15

Data Check is a read-only bit that is set to indicate that a data error was detected when the current sector was read.

Drive Unsafe (UNS) - Bit 14

Drive unsafe is a read-only bit that is set to indicate a fault has occurred in the physical unit. This bit is also set if more than one unit responds to a unit address.

Operation Incomplete (OPI) - Bit 13

Operation Incomplete is a read-only bit which is set when a command involving header search cannot find the header.

Drive Timing Error (DTE) - Bit 12

Drive Timing Error is a read-only bit which is set when either the header or data sync pattern is not found. It is also set if a sector or index pulse is found in the sector's data field, or if there are not enough sectors on a physical unit during a firmware format operation.

Write Lock Error (WLE) - Bit 11

Write Lock Error is a read-only bit that is set to indicate that an attempt was made to write on a write protected drive.

Invalid Disk Address Error (IDAE) - Bit 10

Invalid Disk Address Error is a read-only bit that indicates that the address in RKDA or RKDC was invalid at the beginning of a command which used one or both of these registers.

Cylinder Overflow Error (COE) - Bit 09

Cylinder Overflow Error is a read-only bit that is set to indicate that a data transfer attempted to go beyond the last cylinder on a logical disk drive.

Bad Sector Error (BSE) - Bit 07

Bad Sector Error is a read-only bit that is set to indicate that a data transfer has been attempted to or from a sector that has at least one of the two Good Sector Flags (Header Word 2, bits 14 and 15) reset, indicating a bad sector.

Error Correction Hard (ECH) - Bit 06

Error Correction Hard is a read-only bit that is set to indicate that a data error detected by the Error Correction Code (ECC) logic in the controller cannot be corrected using ECC.

Drive Type Error (DT) - Bit 05

Drive Type Error is a read-only bit that is set when the drive type status bit returned from the selected drive does not compare with the CDT bit (bit 10) in RKCS1.

Format Error (FMTE) - Bit 04

Format Error is a read-only bit that is always zero for the SC12.

Control-to-Drive Parity Error (DPE) - Bit 03

Controller-to-Drive Parity Error is a read-only bit that is set when a command is issued to the controller with the PAT bit (bit 04) in RKMR1 set.

Non-Executable Function (NXF) - Bit 02

Non-Executable Function is a read-only bit that is set to indicate that a Seek or a Write command has been received by the selected drive while Volume Valid was reset.

Seek Incomplete (SKI) - Bit 01

Seek Incomplete is a read-only bit that is set whenever a seek error occurs in the physical disk unit, or a seek (explicit or implied) to track 3 or 7 is received by a logical unit.

Illegal Function (ILF) - Bit 00

Illegal Function is a read-only bit that is set to indicate that an illegal command (33_8, 35_8, 37_8) has been loaded into RKCS1.

4.8 ATTENTION SUMMARY/OFFSET REGISTER (RKAS/OF) 777456, FFFF27, 2013FF27

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATN 7	ATN 6	ATN 5	ATN 4	ATN 3	ATN 2	ATN 1	ATN 0	OF 7	OF 6	OF 5	OF 4	OF 3	OF 2	OF 1	OF 0

The RKAS/OF register can be read or written via program control and as such is used to store the head offset value required by an Offset command, and the current condition of the Attention signal line that is monitored for each drive.

Attention (ATN7-ATN0) - Bits <15:08>

The eight attention bits correspond to the eight drives. Each bit is the equivalent of the Drive Status-Change bit associated with each drive. Thus the clearing of this flip-flop clears the ATN bit in the register. The condition of the Drive Status-Change flip-flop for the selected drive is also shown in DSC (bit 14 in A0 Status).

4.9 DESIRED CYLINDER REGISTER (RKDC) 777460,FFFF28, 2013FF28

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	Cylinder Address									

The RKDC register can be read or written via program control, and is used to store the address of the desired cylinder. Following an initial load, the value in the RKDC register will be incremented by one whenever the track address value in the RKDA register overflows during a data transfer.

4.10 SPARE REGISTER (SPARE) 777462, FFFF29, 2013FF29

The spare register may be written and read back. In the SC12/C emulation the spare register is used for the Pack ID number for firmware format operations, and to setup extended commands.

4.11 DATA BUFFER REGISTER (RKDB) 77746A, FFFF24, 2013FF2A

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Data Buffer															

The RKDB register can be read or written via program control. Reading from the register empties the Silo, while writing into the register fills the Silo. Both the RKDB register and the Silo are cleared by conventional initialization (INIT, CCLR, SCLR).

4.12 MAINTENANCE REGISTER 1 (RKMR1) 777466, FFFF2B, 2013FF2B

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	1	0	0	1	0	0	0	0	DMD	PAT	0	0	MS1	MS0

The RKMR1 register can be read or written via program control, and is primarily used to select the particular A and B status messages.

Diagnostic Mode (DMD) - Bit 05

When Diagnostic Mode bit is set, the controller is effectively disconnected from all of the drives. This mode is not supported by the SC12 emulation.

Parity Test (PAT) - Bit 04

When the Parity Test bit is set, the controller will simulate even parity on status and control messages from and to the drives for diagnostic compatibility.

Message Select (MS1, MS0) - Bits <01:00>

These bits define one of the four pairs of 16-bit status messages (A0-A3 and B0-B3) that can be displayed in RKMR2 and RKMR3. The select bits are cleared by initialization or by loading a command (other than Select Drive) into RKCS1.

4.13 ECC POSITION REGISTER (RKECPS) 777470, FFFF2C, 2013FF2C

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	ECC Position												

The Error Correction Code (ECC) Position register is a read-only register that contains the position of the error pattern as determined by the ECC correction procedure. The error position is the number of bit positions from the beginning of the sector to the right most bit position of the error pattern stored in RKECPT. If the detected error is not correctable using ECC, the ECH error bit in RKER will be set.

4.14 ECC PATTERN REGISTER (RKECPT) 777472, FFFF2D, 2013FF2D

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	ECC Pattern										

The Error Correction Code (ECC) Pattern register is a read-only register that contains the 11-bit error correction pattern obtained from the ECC correction procedure. A 1 in the error pattern indicates a bit of the data in memory from the last read sector which is in error. The error pattern may straddle two 16-bit words in memory. The bit displacement to the right most bit of the pattern is determined by the bit count in RKECPS.

4.15 MAINTENANCE REGISTER 2 (RKMR2) 777474, FFFF2E, 2013FF2E

RKMR2 is a read-only register that displays the "A" status messages for the selected drive. The particular A status is selected by MS1 and MS0 in RKMR1.

Each status message has an odd parity bit in Bit 15 (for diagnostic compatability only) and the Unit No. of the drive in the low-order three bits.

4.15.1 A0 Status

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PAR	DSC	PIP	SO	WL	OFO	FMT	DT	DRY	VV	DRA	0	0	Unit No.		

Drive Status-Change (DSC) - Bit 14

The bit is the OR of any status change due to: completion of a position command, loading or unloading of the heads or any fault condition. The bit is cleared by a Drive Clear command as well as a subsystem clear.

Positioning in Progress (PIP) - Bit 13

This bit is set when a command is being executed that involves head movement.

Spindle On (SO) - Bit 12

This bit is set when the drive is cycled up.

Write Lock (WL) - Bit 11

This bit is set when the drive is in a write lock condition.

Offset On (OFST) - Bit 10

This bit is set to indicate that the logical drive's heads are in an offset condition.

Format (FMT) - Bit 09

This bit is 0 to indicate 22 sector (16 bit per word) format.

Drive Type (DDT) - Bit 08

This bit is a 0 for an RK06 drive, a 1 for an RK07 drive.

Drive Ready (DRDY) - Bit 07

This bit is set when the drive is cycled up, the heads are loaded and positioned over a cylinder, no unsafe condition exists, and the physical disk unit is on-line and ready.

Volume Valid (VV) - Bit 06

This bit is set by the Pack Acknowledge command. It is reset by taking the disk unit off-line.

Drive Available (DRAV) - Bit 05

This bit is always set in single port configurations.

4.15.2 Al Status

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PAR	HU	RTZ	HL	REV	FWD	SOK	CP	DL	BH	HH	SSP	0	Unit No.		

Heads Unloading (UNLD) - Bit 14

This bit is set during an Unload command to indicate that the heads are unloading.

Return-to-Zero (RCAL) - Bit 13

This bit is set while a recalibrate operation is underway.

Heads Loading (LOAD) - Bit 12

This bit is set during a Load command and is cleared when the unit is cycled up.

Reverse (REV) - Bit 11

This bit indicates that the head carriage is moving toward the spindle.

Forward (FWD) - Bit 10

This bit indicates that the head carriage is moving away from the spindle.

Speed O.K. (SPOK) - Bit 09

This bit is set as long as the drive is cycled up.

Cartridge Present (CRTG) - Bit 08

This bit is always set in an existing drive.

Door Latched (DLTCH) - Bit 07

This bit is always set in an existing drive.

Brushes Home (BHOME) - Bit 06

This bit is always set in an existing drive.

Heads Home (HHOME) - Bit 05

This bit is set whenever R/W UNSAFE condition (bit 14 of message B0) is set, or the drive is cycled down.

Servo Signal Present (SRVSG) - Bit 04

This bit is asserted as long as the drive is cycled up.

4.15.3 A2 Status

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PAR	0	0	Cylinder Difference/Offset Position										Unit No.		

This status message contains the difference between the current cylinder position the that specified by the RKDS; or the complement of the offset magnitude, if in offset mode.

4.15.4 A3 Status

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PAR	Firmware Rev Number MSD							LSD	Drive No.				Unit No.		

This status message contains the "drive serial number" which consists of the logical drive number for the LSB and the firmware revision number for the most significant two bits.

4.16 MAINTENANCE REGISTER 3 (RKMR3) 777476, FFFF2F, 2013FF2F

RKMR3 is a read-only register that displays the "B" status messages for the selected drive. The particular A status is selected by MS1 and MS0 in RKMR1.

Each status message has an odd parity bit in bit 15 (for diagnostic compatability only) and the status I.D. in the low-order two bits.

4.16.1 B0 Status

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PAR	RWU	0	SPL	WLE	SKI	PE	NXF	FLT	ACU	IAE	0	0	0	0	0

Read/Write Unsafe (UNS) - Bit 14

This bit is set when a Fault is detected in the disk unit or when more than one disk unit responds to a given address.

Drive-off-Track (DROT) - Bit 13

Always zero for SC12/C emulations.

Speed Loss Error (SPLS) - Bit 12

This bit is never set in the SC12 emulation.

Write Lock Error (WLE) - Bit 11

This bit is set if an attempt is made to write on the disk when the logical drive or physical disk unit is write protected.

Seek Incomplete Error (SEKI) - Bit 10

This bit is set whenever a Seek Error is set in the disk unit, or a seek (implied or explicit) is issued to track 3 or 7 on a logical drive.

Controller-to-Drive Parity Error (CDPE) - Bit 09

This bit is set when a command is issued with the Parity Test (bit 04 of RKMR1) set.

Non-Executable Function (NEXF) - Bit 08

This bit is set when a Seek or write command is attempted with the Volume Valid not set. It is reset with Drive Clear or a subsystem clear operation.

Fault (FALT) - Bit 07

This bit is the OR of all the error conditions in this register.

AC Low (ACLOW) - Bit 06

This bit is never asserted for the SC12 emulation.

Invalid Address Error (IDA) - Bit 05

This bit is set when the address in RKDC or RKDA is not valid (too large).

4.16.2 B1 Status

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PAR	SU	0	0	SSE	0	IE	0	0	0	0	SE	0	0	0	1

Servo Unsafe (UNSF) - Bit 14

Always reset in SC12 emulation.

Seek Limit (SKLIM) - Bit 13

Always reset in SC12 emulation.

Seek No-Motion (SKNOM) - Bit 12

Set when seek incomplete error occurs (see RKER bit 02).

Servo-Signal Error (SSE) - Bit 11

Set when drive unsafe condition detected (see RKER bit 14).

Tribit Error (TBE) - Bit 10

Never set in SC12 emulation.

Index Error (INDXE) - Bit 09

Never set in SC12 emulation.

Multiple Head Select (MHS) - Bit 08

Never set in SC12 emulation.

Head Fault (HFLT) - Bit 07

Set when unsafe condition exists (see RKER bit 14).

Write Gate - No Transitions (WGNT) - Bit 06

Never set for SC12 emulation.

No Write Gate (NWGT) - Bit 05

Never set for SC12 emulation.

Sector Error (SERR) - Bit 04

Never set for SC12 emulation.

4.16.3 B2 Status

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PAR	0	0	Cylinder Address									0	0	1	0

This status message contains the current logical cylinder address of the positioner.

4.16.4 B3 Status

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PAR	0	0	0	Track Addr				Sector Addr				0	0	1	1

This status message contains the track and sector address of the drive after last data transfer command to the drive.

Table 4-1
PDP-11 and VAX-11/730, 750 and 780 Register Addresses

Register	PDP-11	730/750	780/UBA0	780/UBA1
RKCS1	777440	FFFF20	2013FF20	2017FF20
RKWC	777442	FFFF22	2013FF22	2017FF22
RKBA	777444	FFFF24	2013FF24	2017FF24
RKDA	777446	FFFF26	2013FF26	2017FF26
RKCS2	777450	FFFF28	2013FF28	2017FF28
RKDS	777452	FFFF2A	2013FF2A	2017FF2A
RKER	777454	FFFF2C	2013FF2C	2017FF2C
RKAS/OF	777456	FFFF2E	2013FF2E	2017FF2E
RKDC	777460	FFFF30	2013FF30	2017FF30
SPARE	777462	FFFF32	2013FF32	2017FF32
RKDB	777464	FFFF34	2013FF34	2017FF34
RKMR1	777466	FFFF36	2013FF36	2017FF36
RKECPS	777470	FFFF38	2013FF38	2017FF38
RKECPT	777472	FFFF3A	2013FF3A	2017FF3A
RKMR2	777474	FFFF3C	2013FF3C	2017FF3C
RKMR3	777476	FFFF3E	2013FF3E	2017FF3E

Note: If VAX-11/780 has a UBA2 or UBA3, then the register block will start at 201BFF20 or 201FFF20, respectively.

Operations are initiated on the drive selected by the unit select bits in RKCS2 by loading the function code and GO bit into RKCS1. The function code specifies a specific command. The commands can be divided into three categories: data transfer commands, positioning commands, and housekeeping commands. Commands and their corresponding function codes (which are in octal and are always odd since the bit must be asserted to execute the command) are described below:

5.1 DATA TRANSFER COMMANDS

These commands involve data transfers to or from the disk and are designated by function codes 21 through 31.

All data transfer commands have seek and sector search functions implied. When the desired cylinder does not equal the current cylinder during the execution of the data transfer, a seek will be issued to the desired cylinder. The controller will then search the desired track for the desired sector and, when found, will start the data transfer. On all commands except the Write Header command (which is the format operation) and Read Header command, a match of the sector header must be made before the data transfer is started.

The desired sector, track and cylinder addresses are updated after the transfer of a sector. Therefore, at the end of a transfer, the disk is set up to transfer the next sequential sector. This allows multiple sector transfers and spiral transfers across tracks and cylinders. When the desired cylinder address changes during a transfer, the implied seek is performed and is termed a mid-transfer seek.

The data transfer commands are described below:

5.1.1 Read Data (21)

This command reads the 256-word data field from the selected sector and transfers the data to memory. When the sector data transfer is complete, the ECC is checked to Insure that the data read from the disk was error free. If a data error occurred, the ECC correction procedure is initiated to determine whether the error is correctable. When finished, the command is terminated to allow software to apply the correction procedure. Assuming no data errors, the word count in RKWC is checked; if not zero, the data transfer operation is repeated with the next sector.

5.1.2 Write Data (23)

This command writes the 256-word data field of the selected sector with words obtained from memory. A two word ECC is appended to

each sector. If the word count in RKWC goes to zero during the sector, the rest of the sector is 0 filled. After a sector transfer the word count in RKWC is checked, and if not zero, the data transfer operation is continued to the next sector; otherwise the command is terminated by setting the RDY bit.

5.1.3 Read Header (25)

This command transfers the three words of the first header encountered into the Silo and then sets RDY. The three words may be read by examining RKDB three times.

5.1.4 Write Header (Format Operation) (27)

This command writes one logical track with headers. Data for the three word headers are obtained from memory. The data field and the ECC are zeroed. (Actual header is four words, the fourth being an extra check character; however, this is performed entirely by firmware and is not apparent to the software.)

5.1.5 Write Check Data (31)

This command reads data from the selected drive and compares it on a word by word basis with that obtained from memory. If the data fails to compare, the WCE status bit is set and the command is terminated immediately.

5.2 POSITIONING COMMANDS

Positioning commands are mechanical movement commands used to position the heads over the disk pack and take milliseconds to complete. Upon initiating the positioning commands, the controller will set the PIP bit. Upon completion of the positioning operation, the controller resets the PIP bit. The positioning commands are described below:

5.2.1 Recalibrate (13)

This command causes the drive positioner to position the heads over cylinder 0. A Return-to-Zero is automatically performed whenever a Seek Error is detected.

5.2.2 Offset (15)

This command directs the selected drive to offset its heads a specific distance from the track center-line. The direction of the offset is determined by OS7 in RKAS/OF register and sets the OF0 mode bit for the drive. The actual offset is done when the data transfer takes place.

5.2.3 Seek Command (17)

This command causes the heads to be moved to the cylinder address specified by the contents of RKDC. When the controller sees the Seek command with the GO bit set, it sends the cylinder address to the corresponding drive. Upon completion of the seek operation, the ATN is set.

5.3 HOUSEKEEPING COMMANDS

Housekeeping commands are used to place drive logic into a known or initialized state and usually takes only a few microseconds to execute. The housekeeping commands are listed below:

5.3.1 Select Drive (1)

This command selects a drive and obtains the status information defined by MS1 and MS0 in RKMR1. This command sets status for the drive selected and sets the SVAL (Status Valid) bit in RMDS.

5.3.2 Pack Acknowledge (3)

This command sets the VV bit for the command controller. This command must be issued before any data transfer or positioning command can be given if the pack has gone off-line and then on-line. It is primarily intended to avoid unknown pack changes on a dual controller drive.

5.3.3 Drive Clear (5)

This command is used to clear all error flags in the selected drive, provided that the error(s) are no longer present. In addition, the command resets the Status-Change flip-flop for the drive.

5.3.4 Unload (7)

This command simulates the unloading of the heads if they are presently loaded in the selected drive. This operation can only be completed when the operator manually unloads the physical unit.

5.3.5 Start Spindle (11)

This command simulates the starting of the spindle and the loading of the heads on the selected drive if the drive is presently in the unloaded state. This operation will be complete when the operator causes the drive to cycle up.

5.4 EXTENDED COMMANDS

These commands are special to the SC12 emulation and are not found on the RK611 controller. The special commands are enabled by writing key word(s) in the spare register and RKMR1. The commands

may then be executed as other commands by writing to RKCS1 with the GO bit set. The extended command enable sequence must be executed before each extended command given. See paragraph 2.5.2 for more information.

To enable the extended command set, the spare register must contain a one in bit 15 and a zero in bit 14 as the RKMR3 register is written with all ones. The enable is removed with the execution of any command, a bus INIT, subsystem clear, or controller clear.

The following special commands may be executed, after performing extended command enable operation. If the commands are issued without performing the enable operation, the "27" command will result in the execution of the standard track format operation, while the "33", "35", or "37" commands will cause the ILF (Illegal function) bit to set in RKER.

5.4.1 Format Drive (27)

This command, normally a write header, when enabled to be an extended command will cause the entire drive to be hardware formatted. The data which was written in the Spare Register prior to the command will be used for the pack ID number and all blocks will be written with the bad sector block format.

5.4.2 Write Protect (33)

This command has multiple functions. The first is to logically write lock or unlock the logical drives. When the command is issued, the bits <07:00> of the Spare Register are used as the write lock switches for drives 7-0 respectively. A set bit will cause the drive to be write protected. A reset bit will remove the protect state, providing the physical unit on which the drive is mapped is not write protected.

The command also fills the data buffer (silo) with the first 255 words of the hardware buffer (see symbol table) which contains the controller registers, configuration constants, and firmware registers. Successive reads of the silo will then enable software to read the drive size and configuration information, etc. for diagnostic purposes.

The command also loads a firmware switch register when executed. Bits <13:08> of the Spare Register are copied and saved as the Switch Register. Presently only one switch is used (bit 09) which limits the number of disk revolutions to one during a header search before the search is aborted. Normally, search is attempted for four revolutions, except for write check commands, for which it's also limited to one revolution.

5.4.3 Read Unit Headers (35)

This read header command differs from the normal read header command in that an entire track of headers (physical unit track) is

read to the silo in one command. The headers are in order starting with one after the index pulse. (The interlace pattern is followed such that consecutive headers are not physically adjacent.)

The RKDC and RKDA registers must be loaded prior to this command with the desired physical cylinder and track to be read, as in the write unit headers command.

5.4.4 Write Unit Headers (37)

This write header command is used to write headers in conjunction with the track replacement function. It is similar to the normal write header command except that physical unit addresses are used instead of logical drive addresses. Before issuing the command, the RKDC Register must contain the physical cylinder address; the RKDA Register must contain the physical unit track address (no sector, just ten bits of track address) and the Bus Address and Word Count Registers must point to a memory block with the correct amount of data for the number of headers-per-track on the physical unit.

To write over a bad track, the header data should be as follows:

1st Word - New physical cylinder address.

2nd Word - New physical track address plus bits 13, 12, and 10 set to indicate track replace mode.

3rd Word - Exclusive "OR" of words one and two.

BLANK

APPENDIX A

SC12/C CONFIGURATION AND OPTION SELECTION

A.1 INTRODUCTION

To allow the SC12/C user maximum flexibility in disk drive selection, the SC12/C supports a wide variety of disk types. This appendix provides the switch settings which make possible this flexibility.

A.2 CONTROLLER CONFIGURATION

The SC12/C unit is capable of supporting a wide variety of disk drives. Switches SW2-1 through SW2-6, SW2-9 and SW2-10 define the various drives which are supported, and a list of these drive types and sizes may be found in Table A-1. Table A-2 gives the proper switch settings for each of the various configurations.

A.2.1 Physical vs Logical Disk Numbering

A primary feature of the SC12/C is its ability to emulate eight DEC disk subsystems using only two physical disk drives. This is accomplished by mapping more than one logical disk subsystem onto one physical disk drive.

The physical/logical assignments for specific disk configurations can be found by comparing the Physical drive column to the Logical drive column in Table A-2.

A.2.2 Drive Configuration Selection

To find the configuration switch settings which are compatible with your system use the following process. Note that some configurations require 19 sectors, while others require 23, 33, or 35. See the manufacturer's installation manual for instructions.

1. Locate your drive type and size in Table A-1. Note the KEY assigned to each type of drive you intend to use. Make sure your drive is properly sectored.

2. Scan down the KEY column of Table A-2 until you find your drive's number. Check the corresponding emulation in the Logical Drive column. If the emulation is not one that you require, continue to scan the KEY column in search of the required emulation.

3. After finding a suitable match for Drive 0, check the drive key and type for Drive 1 for that configuration row. It is not necessary to use both drive ports. The Logical Drive column is set up such that if logical units 0 and 1 are a drive of type RK06 and 4 and 5 are of drive type RK07 the line will be listed as: 1,2/4,5 = RK06/RK07.

4. When you have found an entire configuration which is suitable, set the configuration switches as indicated.

TABLE A-1
DRIVES SUPPORTED

MFG.	MODEL	KEY	CYL	TRK	SEC	CONFIGURATIONS
Amcodyne	7110	644-04	644	04	32	56,56A
Ampex	165	823-10	823	10	35	12,12A,17,23
Ampex	165-210	1024-10	1024	10	35	20,20A
Ampex	9160	1645-05	1645	5	35	21,21A
Ampex	DFR-932,964 996	823-02	823	2	35	0B,1,1B,2,2B,17,20, 21
Ball	BD160	1645-05	1645	5	35	21,21A
BASF	6172	614-03	614	3	23	7,7B
BASF	6173	614-05	614	5	23	7,7A
Century	T82	815-05	815	5	35	12,12B
Century	T82RM	823-05	823	5	35	44,51
Century	T302RM	823-19	823	19	33	31
CDC	9412	722-05	722	05	32	54A, 55A
CDC	9448-32	823-02	823	2	35	0B,1,1B,2,2B,17,20, 21
CDC	9448-64	823-04	823	4	35	0,3,3B,24,24B
CDC	9448-96	823-06	823	6	35	0B,1,1A,2,3,3A,12A, 15,23,25,25B,
CDC	9448-32	823-02	823	2	33	4,4A
CDC	9448-64	823-04	823	4	33	16,16A,24,24A,43, 43A,44,51,60,60B
CDC	9448-96	823-06	823	6	33	4,4A,25,25A
CDC	9455	206-04	206	4	32	30,30A
CDC	9457	624-04	624	4	32	41,41A,42,42A
CDC	9730-80,9762	823-05	823	5	35	12,12B,44,44B,51
CDC	9730-160	823-10	823	10	35	12,12A,17,23
CDC	9766	823-19	823	19	33	31
Fujitsu	2294	1024-16	1024	16	32	52
Fujitsu	2311	589-04	589	4	35	10,10B,11,11B,32
Fujitsu	2312	589-07	589	7	35	11,11A,32,32A,53,53B
Kennedy	5300-70	700-05	700	5	35	5,5B,15
Kennedy	7300	411-05	411	5	35	35,35A,35B,36,46A, 47A
Memorex	612-56	350-08	350	8	35	22,22B
Memorex	612-84	350-12	350	12	35	22,22A
Mitsu.	2860-25	548-07	548	7	23	45,45A,45B
NEC	2246	692-06	692	6	35	57
NEC	2257	1024-08	1024	8	33	61A
Nissei	NP30-120	568-11	568	11	35	50A

TABLE A-1, cont.

MFG.	MODEL	KEY	CYL	TRK	SEC	CONFIGURATIONS
Okidata	3305	339-10	339	10	32	43,43B
Priam	3350	561-03	561	3	32	5,5A
Priam	3350	561-03	561	3	35	6,6A,6B,27
Priam	2050	526-03	526	3	23	7,7B
Priam	3450	526-05	526	5	23	7,7A,10,10A
Priam	6650	1122-03	1122	3	35	33,33B
Priam	7050	1049-05	1049	5	23	37B
Priam	15450	1122-07	1122	7	35	33,33A,34,60
SLI	Sheyenne 3	656-05	656	5	19	13,13A,13B
SLI	Sheyenne 4	656-07	656	7	19	14,14A,14B,26
SLI	MV116	823-07	823	7	35	37A,40,40A,40B

TABLE A-2
DRIVE CONFIGURATIONS PROM 194

CONF. NO.	SW2- 10 9 6 5 4 3 2 1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s) = Dr Type	Rev
0	O O O O O O O O	823-04	0	35	0,1,2,3 = RK06	A
		823-04	1	35	4,5,6,7 = RK06	A
0A	O C O O O O O O	(Same as configuration no. 0)				
0B	C C O O O O O O	823-06	0	35	0,1,2,3,4,5 = RK06	A
		823-02	1	35	6,7 = RK06	A
1	O O O O O O O C	823-06	0	35	0,1/2,3 = RK06/RK07	A
		823-02	1	35	4,5 = RK06	A
1A	O C O O O O O C	823-06	0	35	0,1/2,3 = RK06/RK07	A
		823-06	1	35	4,5/6,7 = RK06/RK07	A
1B	C C O O O O O C	823-02	0	35	0,1 = RK06	A
		823-02	1	35	2,3 = RK06	A
2	O O O O O O C O	823-06	0	35	1,0,2,3,4,5 = RK06	A
		823-02	1	35	6,7 = RK06	A
2A	O C O O O O C O	(Same as configuration no. 2)				
2B	C C O O O O C O	823-02	0	35	1,0 = RK06	A
		823-02	1	35	2,3 = RK06	A
3	O O O O O O C C	823-06	0	35	1,0/2,3 = RK06/RK07	A
		823-04	1	35	4,5,6,7 = RK06	A
3A	O C O O O O C C	823-06	0	35	1,0/2,3 = RK06/RK07	A
		823-06	1	35	4,5/6,7 = RK06/RK07	A
3B	C C O O O O C C	823-04	0	35	1,0,2,3 = RK06	A
		823-04	1	35	4,5,6,7 = RK06	A
4	O O O O O C O O	823-06	0	33	1,0,2,3,4,5 = RK06	A
		823-02	1	33	6,7 = RK06	A
4A	O C O O O C O O	823-06	0	33	0,1,2,3,4,5 = RK06	A
		823-02	1	33	6,7 = RK06	A
4B	C C O O O C O O	(Same as configuration no. 4)				

TABLE A-2, cont.

CONF. NO.	SW2- 10	9	6	5	4	3	2	1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s) = Dr Type	Rev
5	O	O	O	O	O	C	O	C	561-03	0	32	0 = RK07	A
									700-05	1	35	1,2 = RK07	A
5A	O	C	O	O	O	C	O	C	561-03	0	32	0 = RK07	A
									561-03	1	32	1 = RK07	A
5B	C	C	O	O	O	C	O	C	700-05	0	35	0,1 = RK07	A
									700-05	1	35	2,3 = RK07	A
6	O	O	O	O	O	C	C	O	561-03	0	35	0 = RK07	A
									561-03	1	35	1,2 = RK06	A
6A	O	C	O	O	O	C	C	O	561-03	0	35	0 = RK07	A
									561-03	1	35	1 = RK07	A
6B	C	C	O	O	O	C	C	O	561-03	0	35	0,1 = RK06	A
									561-03	1	35	2,3 = RK06	A
7	O	O	O	O	O	C	C	C	526-05	0	23	0 = RK07	A
									526-03	1	23	1 = RK06	A
7A	O	C	O	O	O	C	C	C	526-05	0	23	0 = RK07	A
									526-05	1	23	1 = RK07	A
7B	C	C	O	O	O	C	C	C	526-03	0	23	0 = RK06	A
									526-03	1	23	1 = RK06	A
10	O	O	O	O	C	O	O	O	526-05	0	23	0,1 = RK06	A
									589-04	1	35	2/3 = RK07/RK06	A
10A	O	C	O	O	C	O	O	O	526-05	0	23	0,1 = RK06	A
									526-05	1	23	2,3 = RK06	A
10B	C	C	O	O	C	O	O	O	589-04	0	35	0/1 = RK07/RK06	A
									589-04	1	35	2/3 = RK07/RK06	A
11	O	O	O	O	C	O	O	C	589-07	0	35	0,1/2 = RK07/RK06	A
									589-04	1	35	3,4,5 = RK06	A
11A	O	C	O	O	C	O	O	C	589-07	0	35	0,1/2 = RK07/RK06	A
									589-07	1	35	3,4/5 = RK07/RK06	A
11B	C	C	O	O	C	O	O	C	589-04	0	35	0,1,2 = RK06	A
									589-04	1	35	3,4,5 = RK06	A
12	O	O	O	O	C	O	C	O	823-10	0	35	0,1,2,3,4 = RK07	A
									815-05	1	35	5,6/7 = RK07/RK06	A
12A	O	C	O	O	C	O	C	O	823-10	0	35	0,1,2,3,4 = RK07	A
									823-06	1	35	5,6,7 = RK07	A
12B	C	C	O	O	C	O	C	O	815-05	0	35	0,1/2 = RK07/RK06	A
									815-05	1	35	3,4/5 = RK07/RK06	A
13	O	O	O	O	C	O	C	C	656-05	0	19	0 = RK07	A
									656-05	1	19	1,2 = RK06	A
13A	O	C	O	O	C	O	C	C	656-05	0	19	0 = RK07	A
									656-05	1	19	1 = RK07	A
13B	C	C	O	O	C	O	C	C	656-05	0	19	0,1 = RK06	A
									656-05	1	19	2,3 = RK06	A
14	O	O	O	O	C	C	O	O	656-07	0	19	0/1 = RK07/RK06	A
									656-07	1	19	2,3,4 = RK06	A
14A	O	C	O	O	C	C	O	O	656-07	0	19	0/1 = RK07/RK06	A
									656-07	1	19	2/3 = RK07/RK06	A
14B	C	C	O	O	C	C	O	O	656-07	0	19	0,1,2 = RK06	A
									656-07	1	19	3,4,5 = RK06	A

TABLE A-2, cont.

CONF. NO.	SW2- 10 9 6 5 4 3 2 1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s) = Dr Type	Rev
15	O O O O C C O C	700-05	0	35	0,1 = RK07	A
		823-06	1	35	2,3/4,5 = RK06/RK07	B
15A	O C O O C C O C	(Same as configuration no. 5B)				
15B	C C O O C C O C	(Same as configuration no. 1A)				
16	O O O O C C C O	823-04	0	33	1,0,2,3 = RK06	B
		823-04	1	33	4,5,6,7 = RK06	B
16A	O C O O C C C O	823-04	0	33	0,1,2,3 = RK06	B
		823-04	1	33	4,5,6,7 = RK06	B
16B	C C O O C C C O	(Same as configuration no. 16)				
17	O O O O C C C C	823-10	0	35	0,1,2,3,4 = RK07	B
		823-02	1	35	5,6 = RK06	B
17A	O C O O C C C C	(Same as configuration no. 12A)				
17B	C C O O C C C C	(Same as configuration no. 1B)				
20	O O O C O O O O	1024-10	0	35	0,1,2,3,4,5 = RK07	B
		823-02	1	35	6,7 = RK06	B
20A	O C O C O O O O	1024-10	0	35	0,1,2,3,4,5 = RK07	B
		1024-04	1	35	6,7 = RK07	B
20B	C C O C O O O O	(Same as configuration no. 1B)				
21	O O O C O O O C	1645-05	0	35	0,1,2,3,4 = RK07	B
		823-02	1	35	5,6 = RK06	B
21A	O C O C O O O C	1645-05	0	35	0,1,2,3,4 = RK07	B
		1645-03	1	35	5,6,7 = RK07	B
21B	C C O C O O O C	(Same as configuration no. 1B)				
22	O O O C O O C O	350-12	0	35	0,1/2 = RK07/RK06	B
		350-08	1	35	3/4 = RK07/RK06	B
22A	O C O C O O C O	350-12	0	35	0,1/2 = RK07/RK06	B
		350-12	1	35	3,4/5 = RK07/RK06	B
22B	C C O C O O C O	350-08	0	35	0/1 = RK07/RK06	B
		350-08	1	35	2/3 = RK07/RK06	B
23	O O O C O O C C	823-10	0	35	0,1,2,3,4 = RK07	B
		823-06	1	35	5/6,7 = RK06/RK07	B
23A	O C O C O O C C	(Same as configuration no. 12A)				
23B	C C O C O O C C	(Same as configuration no. 3A)				
24	O O O C O C O O	823-04	0	33	1,0,2,3 = RK06	D*
		823-04	1	35	5,4,6,7 = RK06	D*
24A	O C O C O C O O	823-04	0	33	1,0,2,3 = RK06	D*
		823-04	1	33	5,4,6,7 = RK06	D*

TABLE A-2, cont.

CONF. NO.	SW2- 10 9 6 5 4 3 2 1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s) = Dr Type	Rev
24B	C C O C O C O O	823-04	0	35	1,0,2,3 = RK06	D*
		823-04	1	35	5,4,6,7 = RK06	D*
25	O O O C O C O C	823-06	0	33	1,0/2,3 = RK06/RK07	D*
		823-06	1	35	5,4/6,7 = RK06/RK07	D*
25A	O C O C O C O C	823-06	0	33	1,0/2,3 = RK06/RK07	D*
		823-06	1	33	5,4/6,7 = RK06/RK07	D*
25B	C C O C O C O C	823-06	0	35	1,0/2,3 = RK06/RK07	D*
		823-06	1	35	5,4/6,7 = RK06/RK07	D*
26	O O O C O C C O	656-07	0	19	0 = RK07[1]	E**
		656-07	1	19	1 = RK07[1]	E**
26A	O C O C O C C O	(Do not select)				
26B	C C O C O C C O	(Do not select)				
27	O O O C O C C C	561-03	0	35	0 = RK07[2]	E**
		561-03	1	35	1 = RK07[2]	E**
27A	O C O C O C C C	(Do not select)				
27B	C C O C O C C C	(Do not select)				
30	O O O C C O O O	206-04	0	32	1,0 = RK06[3]	E*
		206-04	1	32	3,2 = RK06[3]	E*
30A	O C O C C O O O	206-04	0	32	0,1 = RK06[3]	E*
		206-04	1	32	2,3 = RK06[3]	E*
30B	C C O C C O O O	(Do not select)				
31	O O O C C O O C	823-19	0	33	0,1,2,3,4,5,6,7 = RK07	E
		(No physical drive 1)				
31A	O C O C C O O C	(Do not select)				
31B	C C O C C O O C	(Do not select)				
32	O O O C C O C O	589-07	0	35	0,1,2,3,4 = RK06	E
		589-04	1	35	5,6,7 = RK06	E
32A	O C O C C O C O	589-07	0	35	0,1,2,3,4 = RK06	E
		589-07	1	35	5,6,7 = RK06	E
32B	C C O C C O C O	(Same as configuration no. 11B)				
33	O O O C C O C C	1122-07	0	35	0,1,2,3,4 = RK07	F
		1122-03	1	35	5,6 = RK07	F
33A	O C O C C O C C	1122-07	0	35	0,1,2,3,4 = RK07	F
		1122-07	1	35	5,6,7 = RK07	F
33B	C C O C C O C C	1122-03	0	35	0,1 = RK07	F
		1122-03	1	35	2,3 = RK07	F
34	O O O C C C O O	1122-07	0	35	0 = RK07[4]	F**
		1122-07	1	35	1 = RK07[4]	F**
34A	O C O C C C O O	(Do not select)				

TABLE A-2, cont.

CONF. NO.	SW2- 10	9	6	5	4	3	2	1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s) = Dr Type	Rev
34B	C	C	O	C	C	C	O	O	(Do not select)				
35	O	O	O	C	C	C	O	C	411-05	0	35	0 = RK07	F
									411-05	1	35	1,2 = RK06	F
35A	O	C	O	C	C	C	O	C	411-05	0	35	0 = RK07	F
									411-05	1	35	1 = RK07	F
35B	C	C	O	C	C	C	O	C	411-05	0	35	0,1 = RK06	F
									411-05	1	35	2,3 = RK06	F
36	O	O	O	C	C	C	C	O	411-05	0	35	0 = RK07[5]	F
									411-05	1	35	1 = RK07[5]	F
36A	O	C	O	C	C	C	C	O	(Do not select)				
36B	C	C	O	C	C	C	C	O	(Do not select)				
37	O	O	O	C	C	C	C	C	(Do not select)				
37A	O	C	O	C	C	C	C	C	823-07	0	35	0,1,2/3 = RK07/RK06	F
									823-07	1	35	4,5,6/7 = RK07/RK06	F
37B	C	C	O	C	C	C	C	C	1049-05	0	23	0,1 = RK07	F
									1049-05	1	23	2,3 = RK07	F
40	O	O	C	O	O	O	O	O	823-07	0	35	0 = RK07[6]	F*
									823-07	1	35	1,2 = RK06[7]	F*
40A	O	C	C	O	O	O	O	O	823-07	0	35	0 = RK07[6]	F*
									823-07	1	35	1 = RK07[6]	F*
40B	C	C	C	O	O	O	O	O	823-07	0	35	0,1 = RK06[7]	F*
									823-07	1	35	2,3 = RK06[7]	F*
41	O	O	C	O	O	O	O	C	624-04	0	32	1,0 = RK06	K
									624-04	1	32	3,2 = RK06	K
41A	O	C	C	O	O	O	O	C	624-04	0	32	0,1 = RK06	K
									624-04	1	32	2,3 = RK06	K*
41B	C	C	C	O	O	O	O	C	(Do not select)				
42	O	O	C	O	O	O	C	O	624-04	0	32	1,0 = RK06[8]	K**
									624-04	1	32	3,2 = RK06[8]	K**
42A	O	C	C	O	O	O	C	O	624-04	0	32	0,1 = RK06[8]	K**
									624-04	1	32	2,3 = RK06[8]	K**
42B	C	C	C	O	O	O	C	O	(Do not select)				
43	O	O	C	O	O	O	C	C	823-04	0	33	0,1/2 = RK06/RK07	G
									339-10	1	32	3,4 = RK07	G
43A	O	C	C	O	O	O	C	C	823-04	0	33	1,0/2 = RK06/RK07	G
									823-04	1	33	3,4/5 = RK06/RK07	G
43B	C	C	C	O	O	O	C	C	339-10	0	32	0,1 = RK07	G
									339-10	1	32	2,3 = RK07	G
44	O	O	C	O	O	C	O	O	823-04	0	33	1,0,2,3 = RK06	G
									823-05	1	35	4/5,6 = RK06/RK07	G
44A	O	C	C	O	O	C	O	O	(Do not select)				

TABLE A-2, cont.

CONF. NO.	SW2 10 9 6 5 4 3 2 1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s) = Dr Type	Rev
44B	C C O C C C O O	(Do not select)				
45	O O O C C C O C	411-05	0	35	0 = RK07	F
		411-05	1	35	1,2 = RK06	F
45A	O C O C C C O C	411-05	0	35	0 = RK07	F
		411-05	1	35	1 = RK07	F
45B	C C C O O C O C	548-07	0	23	0,1,2 = RK06	G
		548-07	1	23	3,4,5 = RK06	G
46	O O C O O C C O	(Do not select)				
46A	O C C O O C C O	411-05	0	35	0,1,2 = RK06[9]	G
		411-05	1	35	3,4,5 = RK06[9]	G
46B	C C C O O C C O	(Do not select)				
47	O O C O O C C C	(Do not select)				
47A	O C C O O C C C	411-05	0	35	0,1 = RK06[10]	G**
		411-05	1	35	2,3 = RK06[10]	G**
47B	C C C O O C C C	(Do not select)				
50	O O C O C O O O	(Do not select)				
50A	O C C O C O O O	568-11	0	35	0,1,2,3 = RK07	G
		568-11	1	35	4,5,6,7 = RK07	G
50B	C C C O C O O O	(Do not select)				
51	O O C O C O O C	823-05	0	35	0/1,2 = RK06/RK07	G
		823-04	1	33	3,4,5,6 = RK06	G
51A	O C C O C O O C	(Do not select)				
51B	C C C O C O O C	(Do not select)				
52	O O C O C O C O	1024-16	0	32	0,1,2,3,4,5,6,7 = RK07	H
		(No physical drive 1)				
52A	O C C O C O C O	(Do not select)				
52B	C C C O C O C O	(Do not select)				
53	O O C O C O C C	823-06	0	35	0,1/2,3 = RK06/RK07	H
		589-07	1	35	4,5/6 = RK07/RK06	H
53A	O O C O C O C C	823-06	0	35	0,1/2,3 = RK06/RK07	H
		823-06	1	35	4,5/6,7 = RK06/RK07	H
53B	C C C O C O C C	589-07	0	35	0,1/2 = RK07/RK06	H
		589-07	1	35	3,4/5 = RK07/RK06	H
54	O O C O C C O O	(Do not select)				

TABLE A-2, cont.

CONF. NO.	SW2- 10 9 6 5 4 3 2 1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s) = Dr Type	Rev
54A	O C C O C C O O	722-05	0	32	0,1 = RK07[11]	J
		722-05	1	32	2,3 = RK07[11]	J
54B	C C C O C C O O	(Do not select)				
55	O O C O C C O C	(Do not select)				
55A	O C C O C C O C	722-05	0	32	0,1 = RK07	J
		722-05	1	32	2,3 = RK07	J
55B	C C C O C C O C	(Do not select)				
56	O O C O C C C O	644-04	0	32	1,0 = RK06[12]	K
		644-04	1	32	3,2 = RK06[12]	K
56A	O C C O C C C O	644-04	0	32	0,1 = RK06[12]	K
		644-04	1	32	2,3 = RK06[12]	K
56B	C C C O C C C O	(Do not select)				
57	O O C O C C C C	692-06	0	35	0,1,2,3,4 = RK06	L,M
		(No physical drive 1)				
57A	O C C O C C C C	(Do not select)				
57B	O C C O C C C C	(Do not select)				
60	O O C C O O O O	1122-07	0	35	0,1,2,3,4 = RK07	M
		823-04	1	33	5,6/7 = RK06/RK07	M
60A	O C C C O O O O	(Do not select)				
60B	C O C C O O O O	823-04	0	33	0,1/2 = RK06/RK07	M
		823-04	1	33	3,4/5 = RK06/RK07	M
61A	O C C C O O O C	1024-08	0	33	0,1,2,3,4 = RK07	N
		(No physical drive 1)				
61B	C C C C O O O C	(Do not select)				
62	O O C C O O C O	589-07	0	35	0/1,2 = RK06/RK07	P
		823-10	1	35	3,4,5,6,7 = RK07	P
62A	O C C C O O C O	(Do not select)				
62B	C C C C O O C O	(Do not select)				
63	O O C C O O C C	823-05	0	35	0,1,2,3,4 = RK06	S
		823-05	1	35	5/6,7 = RK06/RK07	S
63A	O C C C O O C C	823-05	0	35	0,1,2,3,4 = RK06	S
		823-05	1	35	5,6,7 = RK06	S
63B	C C C C O O C C	823-05	0	35	0/1,2 = RK06/RK07	S
		823-05	1	35	3/4,5 = RK06/RK07	S

CONF. NO.	SW2- 10 9 6 5 4 3 2 1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s) = Dr Type	Rev
64	O O C C O C O O	1122-03	0	35	0,1 = RK07	S
		561-03	1	35	2 = RK07	S
64A	O C C C O C O O	1122-03	0	35	0,1 = RK07	S
		1122-03	1	35	2,3 = RK07	S
64B	C C C C O C O O	561-03	0	35	0 = RK07	S
		561-03	1	35	1 = RK07	S

NOTES: C = Closed (ON), O = Open (OFF)
*Rev D and above configurations require SC12/C Rev B or above emulation PROMs.

**Rev E and above configurations require SC12/C Rev C or above emulation PROMs.

The following notes refer to configurations which result in a non-standard drive size, i.e. an RK06 or RK07 with a non-standard number of cylinders. Emulex will not supply diagnostic or operating system patches for non-standard RK06/RK07 emulations. Diagnostic support is available in the Emulex Diagnostics for the SC12.

[1]This RK07 has 1312 cylinders.

[2]This RK07 has 888 cylinders.

[3]This RK06 has 198 cylinders.

[4]This RK07 has 4160 cylinders.

[5]This RK07 has 1088 cylinders.

[6]This RK07 has 3040 cylinders.

[7]This RK06 has 1520 cylinders.

[8]This RK06 has 592 cylinders.

[9]This RK06 has 360 cylinders.

[10]This RK06 has 544 cylinders.

[11]This RK07 has 870 cylinders.

[12]This RK06 has 624 cylinders.

TABLE A-3
SC12/C FACTORY SWITCH SETTINGS

Switch	Setting	Switch	Setting	Switch	Setting
SW1-1	OFF	SW2-1	OFF	SW3-1	OFF
SW1-2	OFF	SW2-2	OFF	SW3-2	ON
SW1-3	OFF	SW2-3	OFF	SW3-3	OFF
SW1-4	OFF	SW2-4	OFF	SW3-4	OFF
		SW2-5	OFF	SW3-5	OFF
		SW2-6	OFF	SW3-6	OFF
		SW2-7	OFF		
		SW2-8	OFF		
		SW2-9	ON		
		SW2-10	ON		

The factory switch settings enable a standard register address of 777440 and an interrupt vector address of 210.

A.3 USER SELECTABLE OPTIONS

Several other options including the register starting address for the SC12/C can be user selected. The functions of the switches that select those options are defined in Tables A-3, A-4 and A-5, below.

TABLE A-4
OPTION SWITCH SETTINGS

Option Sw	Open	Closed	Function
SW1-1	Run	Halt-Reset	Controller Run/Halt-Reset
SW1-2			Disables check of last header word to read packs written by SC21/Cs[1]
SW1-3	Disable	Enable	Header check error to be bad sector (diagnostic use only)[2]
SW1-4	Disable	Enable	Drives to be write-locked on power-up[3]

[1]See paragraph 3.3.4.1.

[2]See paragraph 3.3.4.2.

[3]See paragraph 3.3.4.3.

TABLE A-5
CONFIGURATION SWITCH SETTINGS

Config Sw	Open	Closed	Function
SW2-1			Drive Configuration[2]
SW2-2			Drive Configuration[2]
SW2-3			Drive Configuration[2]
SW2-4			Drive Configuration[2]
SW2-5			Drive Configuration[2]
SW2-6			Drive Configuration[2]
SW2-7	210	150	Interrupt vector address
SW2-8	Disable	Enable	Head offset capability[1]
SW2-9			Drive Configuration[2]
SW2-10			Drive Configuration[2]

[1]See paragraph 3.3.4.4.

[2]See TABLE A-2 for settings.

TABLE A-6
ADDRESS SWITCH SETTINGS

Switch	Open	Closed	Function
SW3-1	3:1	2:1	Sector Interlace
SW3-2		777440	Standard Address[1]
SW3-3		776700	Alternate Address #1[1]
SW3-4		776300	Alternate Address #2[1]
SW3-5		772040	Alternate Address #3[1]
SW3-6	Enable	Disable	2K Microcode Address[2]

[1]Only one address at a time may be selected. All other address switches must be OFF.

[2]This switch must be OFF.

APPENDIX B
SC12/V1 CONFIGURATION AND OPTION SELECTION

B.1 INTRODUCTION

To allow the SC12/V1 user maximum flexibility in disk drive selection, the SC12/V1 supports a wide variety of disk types. This appendix provides the switch settings which make possible this flexibility.

B.2 CONTROLLER CONFIGURATION

The SC12/V1 unit is capable of supporting a wide variety of disk drives. Switches SW2-1 through SW2-6, SW2-9 and SW2-10 define the various drives which are supported, and a list of these drive types and sizes may be found in Table B-1. Table B-2 gives the proper switch settings for each of the various configurations.

B.2.1 Physical vs Logical Disk Numbering

A primary feature of the SC12/V1 is its ability to emulate eight DEC disk subsystems using only two physical disk drives. This is accomplished by mapping two logical disk subsystems onto one disk drive which contains twice as much capacity as the standard DEC subsystem.

The physical/logical assignments for specific disk configurations can be found by comparing the Physical drive column to the Logical drive column in Table B-2.

B.2.2 Drive Configuration Selection

To find the configuration switch settings which are compatible with your system use the following process. Note that some configurations require 35 sectors, while others require 33 or 23. See the manufacturer's installation manual for instructions.

1. Locate your drive type and size in Table B-1. Note the KEY assigned to each type of drive you intend to use. Make sure your drive is properly sectored.

2. Scan down the KEY column of Table B-2 until you find your drive's number. Check the corresponding emulation in the Logical Drive column. If the emulation is not one that you require, continue to scan the KEY column in search of the required emulation.

3. After finding a suitable match for Drive 0, check the drive key and type for Drive 1 for that configuration row. It is not necessary to use both drive ports.

4. When you have found an entire configuration which is suitable, set the configuration switches as indicated.

TABLE B-1
DRIVES SUPPORTED

Model Numbers	KEY Cyl-Trk	Sects
Ampex/165	823-10	35
Ampex/165-210	1024-10	35
Ampex/9160	1645-05	35
Century/T82	815-05	35
Century/T82RM	823-05	35
Century/T302RM	823-19	33
CDC/9448-32	823-02	33/35
CDC/9448-64	823-04	33/35
CDC/9448-96	823-06	33/35
CDC/9730-80	823-05	35
CDC/9730-160	823-10	35
CDC/9762	823-05	35
CDC/9766	823-19	33
Fujitsu/2311	589-04	35
Fujitsu/2312	589-07	35
Kennedy/5300-70	700-05	35
Priam/6650	1122-03	35
Priam/7050	1049-05	23
Priam/15450	1122-07	35
SLI/MV116	823-07	35

TABLE B-2
DRIVE CONFIGURATIONS, PROM #598

CONF. NO.	SW2- 10 9 6 5 4 3 2 1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s) = Dr Type	Rev
0	O O O O O O O O	823-04	0	35	0,1,2,3 = RK06	A
		823-04	1	35	4,5,6,7 = RK06	A
0A	O C O O O O O O	(Same as configuration no. 0)				
0B	C C O O O O O O	823-06	0	35	0,1,2,3,4,5= RK06	A
		823-02	1	35	6,7 = RK06	A
1	O O O O O O O C	823-06	0	35	0,1/2,3 = RK06/RK07	A
		823-02	1	35	4,5 = RK06	A
1A	O C O O O O O C	823-06	0	35	0,1/2,3 = RK06/RK07	A
		823-06	1	35	4,5/6,7 = RK06/RK07	A
1B	C C O O O O O C	823-02	0	35	0,1 = RK06	A
		823-02	1	35	2,3 = RK06	A
2	O O O O O O C O	823-06	0	35	1,0,2,3,4,5 = RK06	A
		823-02	1	35	6,7 = RK06	A
2A	O C O O O O C O	(Same as configuration no. 2)				
2B	C C O O O O C O	823-02	0	35	1,0 = RK06	A
		823-02	1	35	2,3 = RK06	A

TABLE B-2 (con't)

CONF. NO.	SW2- 10	9	6	5	4	3	2	1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s) = Dr Type	Rev
3	O	O	O	O	O	O	C	C	823-06	0	35	1,0/2,3 = RK06/RK07	A
									823-04	1	35	4,5,6,7 = RK06	A
3A	O	C	O	O	O	O	C	C	823-06	0	35	1,0/2,3 = RK06/RK07	A
									823-06	1	35	4,5/6,7 = RK06/RK07	A
3B	C	C	O	O	O	O	C	C	823-04	0	35	1,0,2,3 = RK06	A
									823-04	1	35	4,5,6,7 = RK06	A
4	O	O	O	O	O	C	O	O	823-06	0	33	1,0,2,3,4,5 = RK06	A
									823-02	1	33	6,7 = RK06	A
4A	O	C	O	O	O	C	O	O	823-06	0	33	0,1,2,3,4,5 = RK06	A
									823-02	1	33	6,7 = RK06	A
4B	C	C	O	O	O	C	O	O	(Same as configuration no. 4)				
5	O	O	O	O	O	C	O	C	561-03	0	32	0 = RK07	A
									700-05	1	35	1,2 = RK07	A
5A	O	C	O	O	O	C	O	C	561-03	0	32	0 = RK07	A
									561-03	1	32	1 = RK07	A
5B	C	C	O	O	O	C	O	C	700-05	0	35	0,1 = RK07	A
									700-05	1	35	2,3 = RK07	A
6	O	O	O	O	O	C	C	O	526-05	0	23	0,1 = RK06	A
									589-04	1	35	2/3 = RK07/RK06	A
6A	O	C	O	O	O	C	C	O	526-05	0	23	0,1 = RK06	A
									526-05	1	23	2,3 = RK06	A
6B	C	C	O	O	O	C	C	O	589-04	0	35	0/1 = RK07/RK06	A
									589-04	1	35	2/3 = RK07/RK06	A
7	O	O	O	O	O	C	C	C	589-07	0	35	0,1/2 = RK07/RK06	A
									589-04	1	35	3,4,5 = RK06	A
7A	O	C	O	O	O	C	C	C	589-07	0	35	0,1/2 = RK07/RK06	A
									589-07	1	35	3,4/5 = RK07/RK06	A
7B	C	C	O	O	O	C	C	C	589-04	0	35	0,1,2 = RK06	A
									589-04	1	35	3,4,5 = RK06	A
10	O	O	O	O	C	O	O	O	823-10	0	35	0,1,2,3,4 = RK07	A
									815-05	1	35	5,6/7 = RK07/RK06	A
10A	O	C	O	O	C	O	O	O	823-10	0	35	0,1,2,3,4 = RK07	A
									823-06	1	35	5,6,7 = RK07	A
10B	C	C	O	O	C	O	O	O	815-05	0	35	0,1/2 = RK07/RK06	A
									815-05	1	35	3,4/5 = RK07/RK07	A
11	O	O	O	O	C	O	O	C	700-05	0	35	0,1 = RK07	A
									823-06	1	35	2,3/4,5 = RK06/RK07	A
11A	O	C	O	O	C	O	O	C	(Same as configuration no. 5B)				
11B	C	C	O	O	C	O	O	C	(Same as configuration no. 1A)				
12	O	O	O	O	C	O	C	O	823-04	0	33	1,0,2,3 = RK06	A
									823-04	1	33	4,5,6,7 = RK06	A
12A	O	C	O	O	C	O	C	O	823-04	0	33	0,1,2,3 = RK06	A
									823-04	1	33	4,5,6,7 = RK06	A
12B	C	C	O	O	C	O	C	O	823-10	0	35	0,1,2,3,4 = RK07	A
									823-06	1	35	5/6,7 = RK06/RK07	A

TABLE B-2 (con't)

CONF. NO.	SW2- 10	9	6	5	4	3	2	1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s) = Dr Type	Rev
13	O	O	O	O	C	O	C	C	823-10	0	35	0,1,2,3,4 = RK07	A
									823-02	1	35	5,6 = RK06	A
13A	O	C	O	O	C	O	C	C	(Same as configuration no. 12A)				
13B	C	C	O	O	C	O	C	C	(Same as configuration no. 1B)				
14	O	O	O	O	C	C	O	O	1024-10	0	35	0,1,2,3,4,5 = RK07	A
									823-02	1	35	6,7 = RK06	A
14A	O	C	O	O	C	C	O	O	1024-10	0	35	0,1,2,3,4,5 = RK07	A
									1024-04	1	35	6,7 = RK07	A
14B	C	C	O	O	C	C	O	O	(Same as configuration no. 1B)				
15	O	O	O	O	C	C	O	C	1645-05	0	35	0,1,2,3,4 = RK07	A
									823-02	1	35	5,6 = RK06	A
15A	O	C	O	O	C	C	O	C	1645-05	0	35	0,1,2,3,4 = RK07	A
									1645-03	1	35	5,6,7 = RK07	A
15B	C	C	O	O	C	C	O	C	(Same as configuration no. 1B)				
16	O	O	O	O	C	C	C	O	(Same as configuration no. 12B)				
16A	O	C	O	O	C	C	C	O	(Same as configuration no. 12A)				
16B	C	C	O	O	C	C	C	O	(Same as configuration no. 3A)				
17	O	O	O	O	C	C	C	C	823-04	0	33	1,0,2,3 = RK06	A
									823-04	1	35	5,4,6,7 = RK06	A
17A	O	C	O	O	C	C	C	C	823-04	0	33	1,0,2,3 = RK06	A
									823-04	1	33	5,4,6,7 = RK06	A
17B	C	C	O	O	C	C	C	C	823-04	0	35	1,0,2,3 = RK06	A
									823-04	1	35	5,4,6,7 = RK06	A
20	O	O	O	C	O	O	O	O	823-06	0	33	1,0/2,3 = RK06/RK07	A
									823-06	1	35	5,4/6,7 = RK06/RK07	A
20A	O	C	O	C	O	O	O	O	823-06	0	33	1,0/2,3 = RK06/RK07	A
									823-06	1	33	5,4/6,7 = RK06/RK07	A
20B	C	C	O	C	O	O	O	O	823-06	0	35	1,0/2,3 = RK06/RK07	A
									823-06	1	35	5,4/6,7 = RK06/RL07	A
21	O	O	O	C	O	O	O	C	823-19	0	33	0,1,2,3,4,5,6,7 = RK07	A
									(No physical drive 1)				
21A	O	C	O	C	O	O	O	C	(Do not select)				
21B	C	C	O	C	O	O	O	C	(Do not select)				
22	O	O	O	C	O	O	C	O	589-07	0	35	0,1,2,3,4 = RK06	A
									589-04	1	35	5,6,7 = RK06	A
22A	O	C	O	C	O	O	C	O	589-07	0	35	0,1,2,3,4 = RK06	A
									589-07	1	35	5,6,7 = RK06	A
22B	C	C	O	C	O	O	C	O	(Same as configuration 11B)				

TABLE B-2 (con't)

CONF. NO.	SW2- 10	9	6	5	4	3	2	1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s) = Dr Type	Rev
23	O	O	O	C	O	O	C	C	1122-07	0	35	0,1,2,3,4 = RK07	A
									1122-03	1	35	5,6 = RK07	A
23A	O	C	O	C	O	O	C	C	1122-07	0	35	0,1,2,3,4 = RK07	A
									1122-07	1	35	5,6,7 = RK07	A
23B	C	C	O	C	O	O	C	C	1122-03	0	35	0,1 = RK07	A
									1122-03	1	35	2,3 = RK07	A
24	O	O	O	C	O	C	O	O	1122-07	0	35	0 = RK07[1]	A
									1122-07	1	35	1 = RK07[1]	A
24A	O	C	O	C	O	C	O	O	(Do not select)				
24B	C	C	O	C	O	C	O	O	(Do not select)				
25	O	O	O	C	O	C	O	C	(Do not select)				
25A	O	C	O	C	O	C	O	C	823-07	0	35	0,1,2/3 = RK07/RK06	A
									823-07	1	35	4,5,6/7 = RK07/RK06	A
25B	C	C	O	C	O	C	O	C	1049-05	0	23	0,1 = RK07	A
									1049-05	1	23	2,3 = RK07	A
26	O	O	O	C	O	C	C	O	823-04	0	33	0,1/2 = RK06/RK07	A
									339-10	1	32	3,4 = RK07	A
26A	O	C	O	C	O	C	C	O	823-04	0	33	1,0/2 = RK06/RK07	A
									823-04	1	33	3,4/5 = RK06/RK07	A
26B	C	C	O	C	O	C	C	O	339-10	0	32	0,1 = RK07	A
									339-10	1	32	2,3 = RK07	A
27	O	O	O	C	O	C	C	C	823-04	0	33	1,0,2,3 = RK06	A
									823-05	1	35	4/5,6 = RK06/RK07	A
27A	O	C	O	C	O	C	C	C	(Do not select)				
27B	C	C	O	C	O	C	C	C	(Do not select)				
30	O	O	O	C	C	O	O	O	823-07	0	35	0 = RK07[2]	A
									823-07	1	35	1,2 = RK06[3]	A
30A	O	C	O	C	C	O	O	O	823-07	0	35	0 = RK07[2]	A
									823-07	1	35	1 = RK07[2]	A
30B	C	C	O	C	C	O	O	O	823-07	0	35	0,1 = RK06[3]	A
									823-07	1	35	2,3 = RK06[3]	A

The following notes refer to configurations which result in a non-standard drive size, i.e. an RK06 or RK07 with a non-standard number of cylinders. Emulex will not supply diagnostic or operating system patches for non-standard RK06/RK07 emulations. Diagnostic support is available in the Emulex Diagnostics for the SC12.

[1]This RK07 has 4160 cylinders.

[2]This RK07 has 3040 cylinders.

[3]This RK06 has 1520 cylinders.

C = Closed (ON), O = Open (OFF).

TABLE B-3
SC12/V1 FACTORY SWITCH SETTINGS

Switch	Setting	Switch	Setting	Switch	Setting
SW1-1	OFF	SW2-1	OFF	SW3-1	OFF
SW1-2	OFF	SW2-2	OFF	SW3-2	ON
SW1-3	OFF	SW2-3	OFF	SW3-3	OFF
SW1-4	OFF	SW2-4	OFF	SW3-4	OFF
		SW2-5	OFF	SW3-5	OFF
		SW2-6	OFF	SW3-6	OFF
		SW2-7	OFF		
		SW2-8	OFF		
		SW2-9	ON		
		SW2-10	ON		

The factory switch settings enable an interrupt vector address of 210, a standard register address of FFFF20 for the VAX-11/730 and /750, and an address of 2013FF20 for the VAX-11/780.

B.3 USER SELECTABLE OPTIONS

Several other options including the register starting address for the SC12/V1 can be user selected. The functions of the switches that select those options are defined in Tables B-3, B-4 and B-5, below.

TABLE B-4
OPTION SWITCH SETTINGS

Switch	Open	Closed	Function
SW1-1	Run	Halt-Reset	Controller Run/Halt-Reset
SW1-2			Not used[1]
SW1-3	Disable	Enable	Header check error to be bad sector[2]
SW1-4	Disable	Enable	Drives to be write-locked on power-up[3]

[1]All unused switches MUST BE OFF.
[2]See paragraph 3.3.4.2.
[3]See paragraph 3.3.4.3.

TABLE B-5
CONFIGURATION SWITCH SETTINGS

Switch	Open	Closed	Function
SW2-1			Drive configuration[2]
SW2-2			Drive configuration[2]
SW2-3			Drive configuration[2]
SW2-4			Drive configuration[2]
SW2-5			Drive configuration[2]
SW2-6			Drive configuration[2]
SW2-7	210	150	Interrupt vector address
SW2-8	Disable	Enable	Head offset capability[1]
SW2-9			Drive configuration[2]
SW2-10			Drive configuration[2]

[1]See paragraph 3.3.4.4.
[2]See Table B-2 for settings

TABLE B-6
ADDRESS SWITCH SETTINGS FOR VAX-11/730 AND VAX-11/750

Switch	Open	Closed	Function
SW3-1	3-to-1	2-to-1	Sector interlace
SW3-2		FFFF20	Standard Address[2]
SW3-3		FFFDC0	Alternate Address #1[2]
SW3-4		FFFCC0	Alternate Address #2[2]
SW3-5		FFF420	Alternate Address #3[2]
SW3-6	Enable	Disable	2K Microcode Address[3]

[1]All unused switches must be OFF.
[2]Only one address at a time may be selected. All other address switches must be OFF.
[3]This switch must be OFF.

TABLE B-7
ADDRESS SWITCH SETTINGS FOR VAX-11/780

Switch	Open	Closed	Function
SW3-1	3-to-1	2-to-1	Sector interlace
SW3-2		2013FF20	Standard Address[2]
SW3-3		2013FDC0	Alternate Address #1[2]
SW3-4		2013FCC0	Alternate Address #2[2]
SW3-5		2013F420	Alternate Address #3[2]
SW3-6	Enable	Disable	2K Microcode Address[3]

[1]All unused switches must be OFF.
[2]Only one address at a time may be selected. All other address switches must be OFF.
[3]This switch must be OFF.

BLANK

Appendix C
INSTRUCTIONS FOR THE EMULEX SC12/C DIAGNOSTICS

C.1 INTRODUCTION

This appendix provides instructions for use of the Emulex SC02/C Diagnostic program. The part number for the listing is PX9960001, and the part number for the mag tape is PX9960301.

C.1.1 Purpose

This program is intended to serve as an extremely useful hardware debugging tool, subsystem reliability test, and pack formatter for the SC12/C Disk Controller.

C.1.2 Program Description

This test program is controlled by a diagnostic supervisor which communicates to the operator via the TTY or CRT. The operator may specify, via the supervisor, any of the supervisor requests. The diagnostic supervisor provides some varied services to the individual diagnostic program. These include routines to interface to the terminal, octal conversion, error handler, operator options, looping facilities and test selection. For more information see the diagnostic supervisor description. Information which must be input by the user is underlined, although not all underlined text in this appendix is information which needs to be input by the user.

C.1.3 Program Format

The diagnostic supervisor locates in memory 1100 - 7776, and the diagnostic program begins at location 10000. It organizes as follows.

a. Supervisor control table

b. Disk controller register definitions

c. Additional command table

e. Command subroutines

f. Support subroutines

g. Test routines

h. Error message tables

C.2 SYSTEM REQUIREMENTS

The hardware necessary to run this program is a PDP-11 processor with 28K minimum words of memory, an operator communication terminal and an SC12/C disk subsystem.

C.3 OPERATING PROCEDURE

To start the program, boot the distribution tape. If you are running XXDP+ all of the following will print. If you are running XXDP only the last line of the following will print.

```
CLEARING MEMORY

CHM MTA0 XXDP+ MT MONITOR 28K

BOOTED VIA UNIT n

ENTER DATE: (DD-MMM-YR)  (The user must enter the date)

RESTART ADDRESS: 153726

50 HZ? N

LSI? N

THIS IS XXDP+

TYPE H OR H/L FOR DETAILS

$RUN SXCX0B
```

The controller will print:

```
EMULEX CORPORATION MODEL SC02/C DISK CONTROLLER
FUNCTIONAL LOGIC TEST, PACK FORMATTER, AND RELIABILITY TEST
REVISION B    MAY 17, 1982

DRIVE STATUS
```

	SECTOR	TRACK	CYLINDER	PHY.UNIT
DRIVE # 0 = RK06	22	3	411	0
DRIVE # 1 = RK06	22	3	411	0
DRIVE # 2 = RK07	22	3	815	0
DRIVE # 3 = RK07	22	3	815	0
DRIVE # 4 = OFF LINE	-	-	-	-
DRIVE # 5 = OFF LINE	-	-	-	-
DRIVE # 6 = OFF LINE	-	-	-	-
DRIVE # 7 = OFF LINE	-	-	-	-

```
ATP  Y OR N ? (Answer N to this)
```

A series of prompts will be printed which request the user to make certain selections. The following underlined answers (which denote user response) are only examples of certain answers.

The first prompt requests the user to select the drives to be tested.

```
EXC> DS 0,2
```

Should the user fail to respond to this command, all on line drives will be tested.

Next a prompt will be printed which requests the user to select the tests to be run:

```
EXC> ST 1,2,3,7
```

Should the user fail to respond to this command, all tests will be run.

A final prompt will be given which allows the user to start the program:

```
EXC> SP
```

After the program has started, it may be interrupted and the control returned to the diagnostic supervisor at any time by typing:

```
CNTL C
```

At the end of each pass, the program will print the following message and begin the next pass.

```
ALL DRIVES TESTED

END OF PASS XXX   ERROR TOTAL XXX
```

C.4 DIAGNOSTIC SUPERVISOR

The purpose of the diagnostic supervisor is to give the operator maximum flexibility in running the program and in using the program as a trouble-shooting aid.

The program is in supervisor command monitor when the following prompt is displayed:

```
EXC>
```

In this mode, the operator may input any of the supervisor command codes described below. A command is always terminated by a carriage return. If parameters are required they must be separated from the command by a space and separated from each other by commas. An example is:

ST 1,2,3 (Select test 1, test 2 and test 3)

C.4.1 Standard Supervisor Commands

Command codes are as follows:

DM (Dump Memory): Display the content of the specified memory locations.

Call:

DM SSSSSS,EEEEEE

Here, SSSSSS is the starting memory location and EEEEEE is the ending memory location.

PM (Patch Memory): Examine and/or modify specified memory location content. Should the user desire to modify the content of the open location, type in the new data in octal/hex, followed by a terminator. If there is no new data input, the content will remain unchanged.

Valid terminators are as follows:

CR - end patching, return to command monitor

LF - examine next sequential location

^ - examine previous sequential location

@ - examine location addressed by data

Call:

PM SSSSSS

Here, SSSSSS is the memory location.

DR (Dump Registers): Display all the PDP-11 general register contents at the trap or halt condition.

Call:

DR

SB (Set Breakpoint): Allows the user to stop execution of the program at a specific location, and return to command monitor.

Call:

SB SSSSSS

Here, SSSSSS is the specific trap location.

CB (Clear Breakpoint): Clears the previous breakpoint trap and restores the program code at the trap location.

Call:

```
CB
```

LB (Loop address on Breakpoint): Sets the breakpoint loop address and also sets SR8 on.

Call:

```
LB SSSSSS
```

Here, SSSSSS is the loop address.

SP (Start Program): Starts to execute the diagnostic test sequence. This is the normal procedure to start the test.

Call:

```
SP
```

LP (Line Printer): Enables the line printer as an output device.

Call:

```
LP
```

ST (Select Sequence Tests): Enters any particular test sequence for the diagnostic test.

Call:

```
ST 1,2,3,5
```

Here, 1,2,3,5 are the selected test numbers.

NT (Select NO Tests): Enters any tests which will not be included in the test sequence.

Call:

```
NT 1,2,3,5
```

Here 1,2,3,5 are bypass test numbers.

AT (Select All Tests): Initializes the test sequence to include all test routines.

Call:

```
AT
```

SS (Select Switch Options): Allows the user to enter any of the displayed switch options in the case that there are no front panel switches.

Call:

```
SS
```

DS (Display Switch Options): Displays all the selected switch options.

Call:

```
DS
```

GT (Go To Specific Address): Goes to a particular address which is specified by the user.

Call:

```
GT SSSSSS
```

Here, SSSSSS is a specific address.

IP (Initialize Program): Restarts the diagnostic program and initializes all the common variables.

Call

```
IP
```

SD (Select Test Drives): Allows the user to specify which drives are to be tested. The user may choose from drives 0 through 7.

Call:

```
SD 1,2
```

Here, 1,2 are selected drive numbers.

KB (Enable CRT/TTY): Enables CRT/TTY as output device, and disables the line printer.

Call:

```
KB
```

C.4.2 Extended Supervisor Commands

DP (Select Data Pattern): Allows the user to select any data pattern to be tested. Each bit in the word pattern corresponds to the pattern number.

Call:

```
DP 0,3,5
```

Here 0,3,5 are data pattern numbers.

TS (Test Summary): Displays the test result summary.

Call:

```
TS
```

FM (Pack Format): Causes all the online logical drives or any particular selected drives to be formatted. All headers are written and the data fields are written with the bad sector file format.

Call:

```
FM                  (for all on-line drives)
FM 0,2,4            (for selected drive 0,2,4 only)
```

DC (Drive Configurations): Displays all the drive configurations.

Call:

```
DC
```

QT (Quick Test): Performs selected tests one iteration, and does the data transfer function from cylinder 0 to cylinder 10 only.

Call:

```
QT
```

C.5 TEST DESCRIPTION

There will be only one iteration of all tests for the first pass for each drive. Otherwise it will perform the test as many iterations as was assigned to the test.

TEST 01 - Reset and Verify Registers

Resets the controller and reads all the controller registers except the data buffer and verifies that they are correct.

Re-examine RKCS1 to make sure controller error did not set.

Re-examine RKCS2 to make sure data late did not set.

TEST 02 - Controller Clear and Verify Registers

Initializes the controller with a controller clear, reads all the controller registers except the data buffer, and verifies that they are correct.

Re-examine RKCS1 to make sure controller error did not set.

Re-examine RKCS2 to make sure data late did not set.

TEST 03 - Test Bits in Controller Status Register 1

Verifies the loading and unloading of all possible read/write bits in the Controller Status Register 1 with both a floating zeros and a floating ones pattern.

TEST 04 - Test Bits in Word Count Register

Verifies the loading and reading of all possible read/write bits in the register with both a floating zeros and a floating ones pattern.

TEST 05 - Test Bits in Bus Address Register

Verifies the loading and reading of all possible read/write bits in the register with both a floating zeros and a floating ones pattern.

TEST 06 - Test Bits in Disk Address Register

Verifies the loading and reading of all possible read/write bits in the register with both a floating zeros and a floating ones pattern.

TEST 07 - Test Bits in Desired Cylinder Register

Verifies the loading and reading of all possible read/write bits in the register with both a floating zeros and a floating ones pattern.

TEST 10 - Interrupt Priority

There are two subtests in this test as follows:

a) Set up priority to one less than controller interrupt priority. Write ready with interrupt enable, make sure there is an interrupt.

b) Now set up priority equal to controller interrupt priority. Write interrupt enable with ready, make sure interrupt does not occur.

Note: In subtest A, for LSI 11/02 processor interrupt priority will be set to zero.

TEST 11 - SILO Read/Write Test

There are four subtests in this test as follows:

a) Read SILO when empty. Check for data late and controller error. Issue controller clear and check if error reset.

b) SILO loading and unloading of one word, using a floating zeros and floating ones pattern. Issue a controller clear to initialize controller. Clear word count register. Write a test word into silo. Check all other registers for interaction problems. Check that output ready is set in RKCS2. If not, wait for a reasonable time, read back content and make sure it is correct. Check for no controller error, no data late, input ready set, output ready reset. Then read another word from the SILO to make sure data late and controller error set. Repeat the test until it uses all the data patterns.

c) This subtest writes the SILO with 66 different data patterns, checks input ready, output ready, and data late for each word written. It then reads all 66 words back, checks contents, input ready, output ready, and data late for each word. An extra read is then done to make sure the SILO is empty.

d) Writes 67 words in the SILO and makes sure data late only occurs on the 67th word. Clears the controller with controller clear and checks input ready and output ready for initialize state.

TEST 12 - Drive Type Error

Creates a drive type error make sure drive type error sets and status valid sets.

TEST 13 - Status Valid and Parity Error

Issues a select to a test drive with bad parity. Makes sure DTCPAR, controller error, current drive attention, DPE, drive interrupt, and status valid set. Issues a controller clear. Makes sure drive interrupt and attention are still set. Selects drive again with good parity. Makes sure attention, current drive attention, drive interrupt, and status valid are set and DTCPAR is reset. Issues a controller clear to clear CERR bit. Issues a drive clear to make sure attention clears.

TEST 14 - Double Interrupt for Recalibrate

Issues a subsystem clear. Issues a recalibrate. Makes sure status valid is set after first interrupt. After second interrupt checks that status valid is reset. Issues drive select and makes sure status valid is set. Clears drive and checks that current drive attention is reset.

TEST 15 - Single Interrupt from Attention

Issues a subsystem clear. Does a seek to cylinder zero. Waits for interrupt from drive attention, and makes sure another interrupt does not occur. Clears drive.

TEST 16 - Illegal Disk Address

Issues a recalibrate, makes sure it is on legal disk address. Then performs the two subtests as follows:

a) Issues a seek to cylinder 0, and head 3. Makes sure illegal address error and seek incomplete set. Clears controller and drive. Repeats for heads 4-7. Checks that both IDAE and seek incomplete set for head 7, and IDAR sets for head 4, 5, and 6.

b) Issues a seek to maximum cylinder plus one, head 0, and makes sure illegal disk address error sets. Clears controller and drive.

TEST 17 - Write/Read One Sector

Issues a write data of one sector on cylinder 312, head 0, and sector 0. Reads it back to make sure it agrees with what is written. Repeats the test with all selected data patterns.

TEST 20 - Partial Write/Read Test

This test will perform the following 3 subtests:

a) Issues a write data of 103 words to cylinder 312, head 0, and sector 0. Issues a read data of 256 words on cylinder 312, head 0, and sector 0. Makes sure only 103 words agree with what is written, with the rest of sector words zero filled.

b) This subtest will be the same as subtest A, except it uses 255 words.

c) This subtest will also be the same as subtest A, except it uses 1 word.

Repeat this test with all selected data patterns.

TEST 21 - Write Check One Sector

This test consists of four subtests as follows:

a) Issues a write data to cylinder 312, head 0, and sector 0 with selected data pattern. Issues a write check to cylinder 312, head 0, sector 0, makes sure no error occurs.

b) Issues a write data to cylinder 312, head 0, and sector 0 with selected data pattern. Issues a write check to cylinder 312, head 0, and sector 0 with same data except word 110 has its complement. Makes sure write check error sets, and bus address and word count are correct.

c) Same as subtest b, except using word 0 for testing.

d) Same as subtest b, except using word 255 for testing.

Repeat this test with all selected data patterns.

TEST 22 - Partial Write Check

Writes data to cylinder 312, head 0, sector 0, with 256 words of known data. Issues a write check command of 110 words making sure that 111th word is different than data on the disk. Makes sure write check error does not set.

TEST 23 - Write/Write Check/Read Two Sectors

This test performs four subtests as follows:

a) Issues a write data of 512 words to cylinder 312, head 0, sector 0. Issues a write check of 512 words and makes sure no error. Issues a read data of 512 words and makes sure no error.

b) Issues a write data of 257 words to cylinder 312, head 0, sector 0. Issues a write check of 512 words and makes sure second sector fills with zero after the first word. Issues a read data of 512 words and makes sure no error.

c) Issues a write data of 512 words to cylinder 312, head 0, sector 21. Issues a write check of 512 words and make sure no error. Issues a read data of 512 words and makes sure no error.

d) Issues a write data of 512 words to cylinder 312, head 2, sector 21. Issues a write check of 512 words and

makes sure no error. Issues a read data of 512 words and makes sure no error.

Repeat this test with all selected data patterns.

TEST 24 - End of Pack

This test performs three subtests as follows:

a) Issues a write data with 512 words to last cylinder, last head, last sector, making sure the cylinder overflow error (COE) sets.

b) Issues a write check with 512 words to last cylinder, last head, last sector, making sure the cylinder overflow error (COE) sets.

c) Issues a read data with 512 words to last cylinder, last head, last sector, making sure the cylinder overflow error (COE) sets, and verifies the data in last cylinder, last head, last sector is correct.

TEST 25 - Programming Error

Issues a subsystem clear. Issues a read data of 512 words on cylinder 312, head 0, sector 0. During read, issues a write to the spare register. Makes sure programming error sets.

TEST 26 - ECC Hard Error

Issues a subsystem clear. Issues a write data of 512 words to cylinder 0, head 0, and sector 0. Again, issues a write data of 512 words, while writing the sector the second time and issues a controller clear. Now issues a read data of 512 words to cylinder 0, head 0, and sector 0, making sure ECC hard error sets.

TEST 27 - Non-Existing Memory

This test consists of two parts:

a) Issues a write data of 1 word using address 776000, making sure non-existing memory sets.

b) Issues a read data of 1 word using address 776000, making sure non-existing memory sets.

This test will not be run if the CPU is LSI 11/23 with 128K words of memory.

TEST 30 - Extended Memory Address Test

This test checks the operation of the extended memory address bits. If the system does not have memory management or has memory management and only 32K this test will not be performed. If switch 0 is set, 22-bit addressing will be tested, otherwise 18-bit addressing will be tested. Appropriate address bits will be verified.

a) The program writes 2 words on test sector of all zeros, except for the second word which is all ones.

b) Extended address bit "A16" is tested by clearing location 200000 and reading the test sector into location 177776. Location 200000 is checked to verify that data is all ones.

c) Location 400000 is cleared and the test sector is read into location 377776. Location 400000 is checked for the proper content (ones).

d) Location 1000000 is cleared and the test sector is read into location 777776. Location 1000000 is checked for the proper content (ones).

e) Location 2000000 is cleared and the test sector is read into location 1777776. Location 2000000 is checked for the proper content (ones).

f) Location 4000000 is cleared and the test sector is read into location 3777776. Location 4000000 is checked for the proper content (ones).

g) Location 10000000 is cleared and the test sector is read into location 7777776. Location 10000000 is checked for the proper content (ones).

TEST 31 - Generate Bad Sector File for Formatted Drive

This test includes two parts as follows:

a) It writes with data pattern 11 on every sector except all the sectors in the last cylinder, last head. The cylinder address and disk address will be saved in bad sector file wherever an error occurred.

b) Issues a write check to every sector except all sectors in the last cylinder, last head, because this command never does an ECC correction and it is necessary to have all read errors in the file. All cylinders, heads, sectors having error will be saved in bad sector file.

TEST 32 - Bad Sector File Manipulation

This test reads the current bad sector file and allows the operator to zero it, add to it, list it, and rewrite it. If switch 02 is set this is test will be bypassed.

TEST 33 - Operator Intervention Test

This test consists of three subtests as follows:

a) This subtest checks the status of 'WRL' bit in the RKDS; when write protected/read-write enabled.

b) This subtest checks the LTC interrupt. The following conditions have to be satisfied so that the test will run successfully.

1. For LSI 02 - W3 jumper must be removed.
2. For LSI 23 - W4 jumper must be removed.
3. In SC02 controller - SW3-5 should be on.

c) This subtest will read the bootstrap PROM and calculate the check sum and compare with the check sum in PROM to verify the PROM is correct.

TEST 34 - Seek Test

This test consists of the following three subtests:

a) Seek command is issued from cylinder 0 to the last cylinder with increment of one cylinder at a time.

b) Seek command is issued from the last cylinder to cylinder 0 with decrement of one cylinder at a time.

c) This subtest will initialize two cylinder address words, one to cylinder 0 and the other to the last valid cylinder (ADD0, and ADD1 resp.) Seek command sequences will be executed taking the cylinder address from ADD0 and ADD1, alternately. ADD0 and ADD1 will have its cylinder address incremented (ADD0) and decremented (ADD1) by one each time the appropriate word is used for a seek address. The subtest will be ended when the seek function has been completed for the zero cylinder address when taken from ADD1.

TEST 35 - Addressing Test

This test writes three words (cylinder address, head/sector address, and drive number) in all sectors. Then it reads them back and checks data to verify the proper sector is selected.

TEST 36 - Write/Write Check/Read Whole Pack

This test writes data to all sectors with selected data pattern, write checks all the sectors and reads all sectors and verifies the data is correct. Repeats the test with all selected data patterns.

TEST 37 - Multi-Drive Interference Test

This test performs multi-drive positioning operations, while the test drive performs a large data transfer, for the purpose of detecting problems of concurrent drive operation. This test will not be run if there is only one drive on the subsystem.

C.6 ERROR INFORMATION

The supervisor provides complete error handling capability, including the ability to loop back to a specified point from the error, suppress error typeout, etc. The supervisor error handler is called via the EMT call in the computer, which allows for up to 255 different error messages, as the low order byte can pass 8 bits of data to the handler. The handler will type three lines of information concerning the error. The first line will be a description of error, and the second line will be the heading for the data on the third line. For example:

```
ERROR OCCURRED IN WRITE OPERATION
TEST      PC     RKCS1   RKCS2    RKDS    RKER
000017  030722  100222  002000  100300  000000
```

The program passes the pertinent data to the error handler in $PARA0, $PARA1, $PARA2, etc. $PARA0 contains the number of data words passed in $PARA1, $PARA2, etc. For example:

```
        MOV     #2,$PARA0

        MOV     RKCS1(R4),$PARA1

        MOV     RKCS2(R4),$PARA2
```

The error message is specified by the number address to the basic error call (which is the EMT instruction). For example:

```
        ERROR+41
```

will tell the handler to output error message 41. The error message is placed at the end of the program. The error handler will search the error table to pick the address of error message and the error data heading address.

Physical and logical addresses of the current test drive will also be displayed in front of any error message. It provides some of

the information concerning the location of the error in the physical drive. The format is as follows:

-------PHYSICAL-------				--------LOGICAL--------			
DR	CYL	TRK	SEC	DR	CYL	TRK	SEC
0	1234	3	0	0	400	2	22

C.7 NON-STANDARD CONTROLLER ADDRESS AND INTERRUPT VECTOR

If the test controller is not using standard address (177440) and standard interrupt vector (210), the operator must patch the program before he starts to run the program.

Patch location 010240 for controller address.

Patch location 010242 for interrupt vector and location 010244 for interrupt status.

Patch location 010246 for interrupt priority, default is level 5.

C.8 TERMINAL REQUIREMENT

This program is written for a terminal using 9600 baud. If the terminal uses below 9600 baud, the operator must patch the program to provide appropriate filler characters. The filler character is located in 001263. Be careful as it is in the higher byte of a word. Enter the number in the high byte of word, for example:

001262 002000 enters the filler character number 4.

If the terminal is VT100, the operator must turn off the auto X-ON X-OFF mode. The diagnostic supervisor will not support auto X-ON, X-OFF mode.

C.9 CONTROL CHARACTERS

There are three control characters in this program as follows:

CONTROL C - Aborts the program and returns to the supervisor command monitor.

CONTROL S - Stops the display of output at your terminal.

CONTROL Q - Resumes the display of output at your terminal.

APPENDIX D
MODIFICATIONS TO DEC DIAGNOSTICS

D.1 ZR6A-CO RK611 DISKLESS DIAGNOSTIC - PART 1 - (Aug 77) - S1C20A

Location	From	To
12542	1404	404
13432	1404	404
14316	1404	404
15202	1404	404

D.2 ZR6K-EO RK06 FUNCTIONAL CONTROLLER DIAGNOSTIC (Feb 78)-S1C11A

Location	From	To
6304-6306	12737,62	137,6540
20606-20610	12737,12	137,22050
25612-25614	12737,5	137,26312
26372-26374	12737,12	137,30212
11346-11350	12737,12	137,11710
12042-12044	12737,12	137,12352
35110	42777	2
10630	104431	104435
10710	104423	104435
11272	104424	104435
12022	104425	104435
12432	104431	104435
12540	104431	104435
12570	104424	104435
22202	104424	104435
22374	104424	104435
22474	104424	104435
22656	104431	104435
24326	104431	104435
22132	104431	104435
30332	104426	104435
32162	104427	104435
11230	104431	104435
11772	104431	104435
37040	000020	000400

D.3 ZR6M-DO RK611/06 SUBSYSTEM VERIFY-PART 1 (Feb 78)-S1C22A

Location	From	To
55730-55732	5737,177572	137,56060
26044-26046	5037,5532	240,240

D.4 ZR6N-DO RK611/06 SUBSYSTEM VERIFY-PART 2 (Feb 78)-S1C23A

Location	From	To
23252	177145	177400
23262-23264	1002,5260	62760,100
57744-57746	5737,177572	137,60074
30602-30604	5037,5532	240,240

D.5 ZR6L-CO RK06 FORMATTER (Feb 78) - S1C18A

Location	From	To
20734	3670	4670
22030	3670	4670
31672	6	5
31676	12	0
31726	3660	4660
23576	104411	207
22056	10114	10124
22060-22062	104412,207	137,27536
27534	1457	457
27536-27540	52737,4	12714,17777
27542-27544	6364,105737	104412,207
2032-2034	44004,46413	46050,45563
2036-2040	47712,50310	0,0
27734-27736	104104,42737	104055,4737
27740-27742	2,6364	22024,240