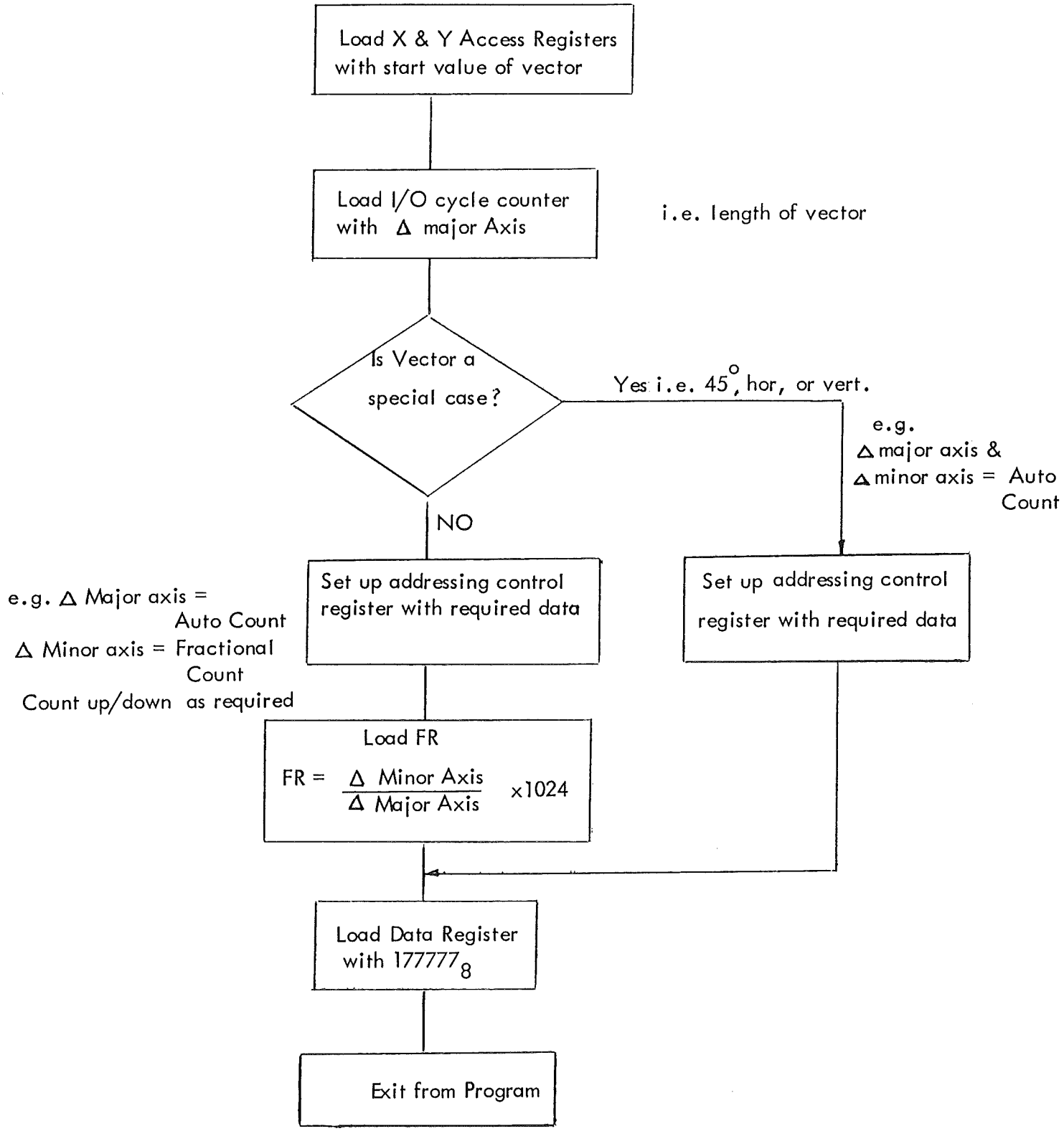

FIG. M5

Flowchart of Hardware Vector Generator Initialisation

M3 Circuit Description

The Address Computation PCB is situated in position no. 4 of the control backplane and the circuit arrangements are shown on Drg. 02-575. Connections with other PCBs are made via edge connector sockets (EC).

The board contains the X and Y access registers for the X and Y co-ordinates for Access cycles, the Y offset register for the starting address for Scan cycles, and the addressing control register which sets up these registers for the required mode of operation.

The computer accesses the registers by register address lines A0- and A1- on EC pins BF1, BF2. These are enabled into decoder A7 by the AC WRITE signal, input from the Control PCB on EC pin AB1, in order to set up the selected register. They are also applied to selector A5 to ensure the computed addresses are multiplexed onto the memory address highway. The computed address is divided into row and column components to drive the 16K or 64K RAMs on the Memory PCBs. Links are provided to allow compatibility with the memory capacity.

M3.1 Addressing Control Register

During the addressing sequence, the computer sets the required parameters for the selected mode on highway bits as defined in M2.2.

Signals A0, A1 are set low to clock data into the Addressing Control Register, D6, if bit 15 of the data is low.

M3.2 Access Cycle Addressing

An Access cycle allows the computer to randomly address the Memory PCBs.

The relevant bits in the addressing control register (D0 - D3) which set the required access mode are clocked through D6 by signal XYTFR- from the Control PCB and set up the X and Y access registers.

The computer sets the X or Y co-ordinates on the data highway and they are converted by the address computation logic into the bit, row and column addresses. The co-ordinates are clocked into the buffer registers (D7, E7 for the Y co-ordinates, C11, C13 for the X co-ordinates) by decoder A7 pin 5 or 4 as selected by programmable flags A0, A1:

A0	A1	
H	H	X access register
L	H	Y access register

The physical memory address is calculated from the X and Y co-ordinates according to the formula :

Y (HRES) + X.

The Y co-ordinates from the Y access buffer register (D7, E7) are loaded into Y access counter D8, E8, D9, D10 by the trailing edge of the XYTFR- pulse which also provides a clock pulse via monostable B2 to clock the co-ordinates through the counter. If automatic counting is required, the XYTFR- pulse clocks highway bits D0 and D1 through D6 to set counter pins 7 and 10 low for automatic count, and counter pin 1 high or low to increment or decrement the count. The counter is consequently clocked by a XYCNT+ signal from the Sync and Timing PCB (EC pin AC1) at the end of each cycle.

The counter outputs are applied to multiplexers E9, E13, D12, D11. The select pins on these units are controlled by the repeat field signal R.FIELD on EC pin BR2 such that the A inputs are selected for a repeat field system and the B inputs for a non-repeat field system. The A and B inputs are arranged so that for a non-repeat field system, the LSB from the counter becomes the MSB for the memory, and the remaining Y value bits are shifted down one place. This causes even lines to be stored in the lower half, and odd lines in the upper half of memory (see Fig. 4.1).

The 13 bit output from E9, E13, D12, D11 is applied to multiplexers E10, E14, D13, D15 and E12, E15, D14, D16. The multiplication factor signals MF0, MF1, MF2 on EC pins CJ1, CJ2, CK1 determine the horizontal resolution value (HRES) which may be used as follows :

256	(128 x 2)
384	(128 x 3)
512	(128 x 4)
768	(128 x 6)
1024	(128 x 8)

With MF2 set low, multiplexers E10, E14, D13, D15 select 1Y or 4Y as determined by signal MF0, and E12, E15, D14, D16 select 2Y or 4Y as determined by MF1. With MF0 set high, E10, E14, D13, D15 are inhibited. The selected outputs are then input to adders E11, E16, C14, C16, to provide the required Y(HRES) value.

The X co-ordinates from the X access register (C13, C11) are loaded into X access counter C15, C12, B11 as described for the Y access counter above, and the counter is set up for automatic counting if required by address control register bits D2, D3.

The outputs from counter B11 pins 14, 13, 12, 11 and C12 pin 14 provide the memory address bits M0 - M4. The outputs on C12 pins 13 and 12 provide the access row signals AR1, AR0. The remaining outputs from the X access counter are input to adders A10, D1, B14, B15 for summing with the Y(HRES) value from E11, E16, C14, C16 to give the single physical address.

The output from A10 pin 6 (for 64K memory) D1 pin 15 (for 16K memory) is input to E9 pin 5 to provide the MSB for a repeat field system. The remaining outputs from A10, D1 B14, B15 provide the access column (AC0 - AC5) and access row (AR2 - AR6) addresses which are applied to multiplexers A16, A15, B13, B12 for selection onto the memory address highway by multiplexer A5.

The computed access column and row addresses are input to multiplexers A16, A15, B13, B12. The actual address to be multiplexed onto the internal and memory address highways is selected via multiplexer A5. The select input on A5 pin 1 is set low for Access cycles so that the outputs follow the A inputs, and signal RCS1 on EC pin BB1 is set high. Row or column is selected by signal RCS0- on EC pin BA1 which is set low for row, high for column.

The selected address is multiplexed onto the memory address highway via buffers A11, A12, A14.

M3.3 Scan Cycle Addressing

For Scan cycles, register address line A0 is set high and A1 low so that signal AC WRITE, via A7 pin 6, clocks the Y offset value (data bits D0 - D13) into the Y offset register, C4, C7, C10. This register sets the actual address at which scanning of the visible picture begins, and the address provides the input to the scan counter.

The scan counter comprises C8, B8, B9, B10 and is controlled by multiplexer B6. The strobe, pin 15, is tied low and the select input, pin 1, is set low by the maintenance bit (D5) from the addressing control register.

For Scan cycles, the outputs on B6 follow the A inputs when the field is unblanked. Flip-flop B4 is clocked b on EC by FUNBNK+ at the start of the unblanked period which enables the next LINE SYNC pulse to load the start address into the scan counter. During the remainder of the field, the scan counter is clocked by SCAN UP.

The six least significant bits of the scan counter are not affected by the mode of operation and are connected directly to the multiplexers B12, B13, A15. Higher order bits are dependant upon whether 16K or 64K RAMs are in use and upon scrolling techniques. Patch panel SCØ - SC6 links the counter outputs to the multiplexers to suit the size of RAM, and selector C6 routes the counter outputs according to the mode of scrolling (See Fig. 4.2)

For a repeat field system, C6 pin 2 is set low so that SC6 and/or SC7 follow the scan counter outputs. Vertical scroll is controlled by the Y offset value from the computer (see sub-section 2.3.1).

For interlaced systems where vertical scrolling is not required or is required by an even number of lines, the exchange input on C6 pin 14 is set low. The outputs SC6 and/or SC7 follow the ODDEVE field input on C6 pins 4 and 12. If vertical scrolling is required by an odd number of lines, the computer sets the exchange bit in the addressing control register so that C6 pin 14 is high. The outputs now follow the inverted ODDEVE field input on C6 pins 3 and 13 to alternate the memory partition selection.

The scan column and row addresses from the scan counter, are input to multiplexers A16, A15, B13, B12. The actual address to be multiplexed onto the memory address highway is selected via multiplexer A5. The select input on A5 pin 1 is set low so that the outputs follow the A inputs, i.e. Scan cycles are selected by signal RCS1 on EC pin BB1 which is set low for scan. Row or column is selected by signal RCS0- on EC pin BA1 which is set low for row, high for column.

The selected address is multiplexed onto the memory address highway via buffers A14, A12, A11.

M3.4 Maintenance Mode

The purpose of maintenance mode is to allow the computer to verify the physical memory addresses generated from the X and Y access registers, the Y offset register and the scan counter.

For maintenance mode, bit D5 in the addressing control logic is set high and is clocked through D6. It is input to the scan counter multiplexer B6 and the address selection multiplexer A5 to inhibit the normal clocking of the scan counter and selection of the memory address.

A diagnostic program loads the X and Y access registers and the Y offset register with a range of values, and the resultant access or scan addresses are read by the computer to check the accuracy of the address computation circuits.

The diagnostic values for the Y offset register are loaded in the scan counter by the XYTFR- signal. This signal also provides the clock pulse via monostable B2 which causes B5 pin 8 to pulse high.

For address selection, the maintenance bit from D6 pin 12 sets A5 pin 1 high so that the A5 outputs follow the B inputs which are derived from the register address lines A0, A1 as follows :

A0	A1	Decoder A7	Selector A5
H	H	X access register	Access row address
L	H	Y access register	Access column address
H	L	Y offset register	Scan row address
L	L	Address control register	Scan column address

To verify the address computation, the AC.READ+ signal (EC pin AA1) from the Control PCB is set and enables transceivers A1, A2, A3. This allows the memory address to be placed onto the highway for transmission to the computer.

M3.5 Hardware Vector Generation

The Fractional Register (C3, E6 and D5) and Accumulator (C1, E4 and D3) are added together (via C2, E5, E3, and D4). The O/P of the adder feeding the accumulator. Thus, on every XYCNT the Accumulator is incremented by the value of the Fractional Register. X or Y Auto bits will be set depending on the angle of the vector to be drawn. Whichever is set, this enables either E2/3 or E2/6, allowing every XYCNT to clock the respective Access Counter. When the adder overflows C2/15 goes high and enables the fractional axis to increment. XYCNT stops when the I/O cycle counter (on the Control card) reaches zero.

The fractional register and addressing control register are loaded via a shortened write pulse, via monostable (B1). This is because some computers (e.g. PDP11-34) remove the data before cancelling the write signal. This will corrupt whichever of the 2 registers has not been written to, as Data bit D15 decodes the register that is to be accessed. The shortened write pulse will prevent this, by ensuring data is present throughout the duration of the write pulse.

SUPERVISOR 214 SB12 SLOT

Dimensions + Max. Weight:

Height: 221.5 overall
Width: 482.5 overall (436.5 to chassis sides)
Length: 361 overall, 343 without front panel
Max Weight: 15 - 20 Kg (Dependent on No. of Cards)
Colour: Choice of Ivory or Mist Grey Front Panel
Chassis Black, (Other colours to order)

Operating Environment:

Temperature: 10 - 40°C (Ambient)
Humidity: 20 - 80% R.H. Non condensing
Attitude: Any (Fan fail type ± 30° of horizontal)

Power Requirements:

Voltage Range: 110 or 240V 50 - 60 Hz
Tolerence: Voltage - 10% to + 6% Freq. ± 10%
Switch on Surge: 10A
Nominal Current: 110V 2A, 240V 1A

For Mech. details see 07 - 03 - 15

SUPERVISOR 214 SB16 SLOT

Dimensions + Max Weight:

Height: 267 Overall
Width: 482.5 Overall, 436.5 at chassis sides
Length: 391 Overall, 373 without front panel
Max Weight: 18 - 28 Kg (Dependent on No. of Cards)
Colour: Choice of Ivory or Mist Grey Front Panel
Chassis Black (Other colours to order)

Operating Environment:

Temperature: 10 - 40°C
Humidity: 20 - 80% Non condensing
Attitude: Any (Fan fail type ± 30° of horizontal)

Power Requirements:

Voltage range: 110 or 240v 50 - 60 HZ.
Tolerance: Voltage - 10% to + 6% Freq. + 10%
Switch on Surge: 10A
Nominal Current: 110V 3A, 240V 1.5A

For Mech. Details See 07 - 03 - 17

SUPERVISOR 214 COMPACT

Dimensions + Max Weight:

Height: 263.5
Width: 482.5 Overall 426.5 at Rack Slide Mounts.
Length: 595 Overall
Max Weight: 35 Kg
Colour: Ivory B.S. 4800, Black Trimite 401, Mist Grey or other Colours to order.

Operating Environment:

Temperature: 10°C - 30°C (Ambient)
Dependent on configuration.
Humidity: 20% - 80% Non Condensing
Attitude: Does not matter. (Fan fail type, ± 90° of horizontal).

Power Requirements:

Voltage Range: 110 or 240v 50 - 60 Hz.
Tolerance: Voltage - 10% to + 6% Freq. ± 10%
Switch on Surge: Internal PSU 10A Ext 35
Nominal Current: 6A 110V, 3A 240V

For Mech. details see: 07 - 03 - 14

APPENDIX N

MULTIBUS/S214 INTERFACE

CONTENTS

TABLES

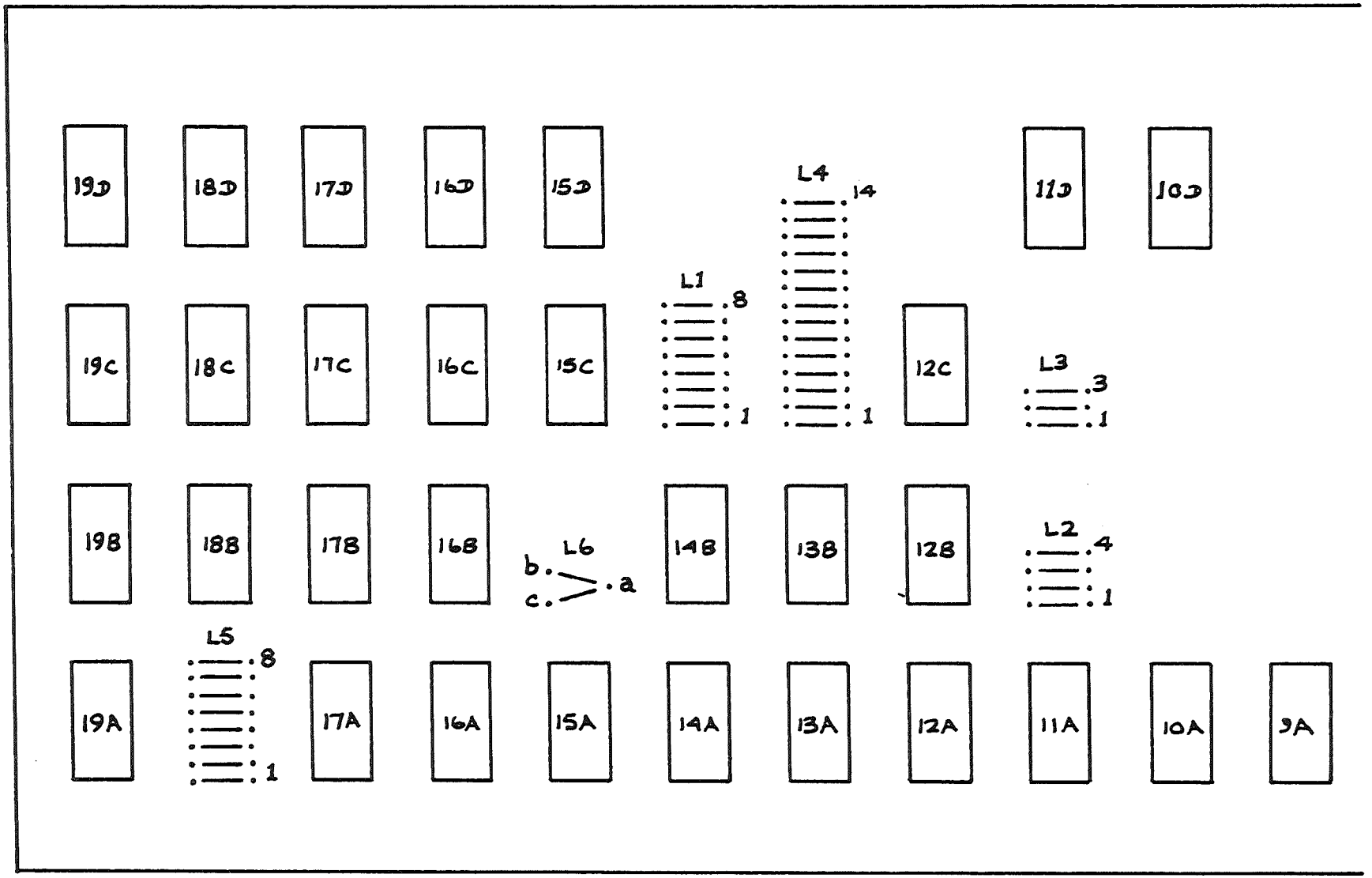

FIGURE N1

POSITION OF LINK FIELDS ON WIRE WRAP CARD

NI General Description

The supervisor 214 is controlled by reference to a set of 64 x 16 bit registers which appear in the I/O area of the Multibus address space. One exception to this is when the 214 is in the Data Page Mode. This mode is used for DMA transfers between the computer and the 214. Here the address space may be located anywhere in the main memory area and can be configured to utilise from 512 words to 4096 words.

The address allocation is determined by wire links on the card. The main constraint for allocating address space is that the lowest register address (ie the Data register) must be on a 64 word boundary.

There are 2 variants of the interface card.

a) 20 bit addressing from Computer.
b) 24 bit addressing from Computer.

Interupts from the 214 can be patched on to any of the 8 multi-bus interupt lines via wire links.

For full linking details see Table N.1

The Multi-bus Compliance for the interface is

SLAVE D16 M24/M20 116 VOL

TABLE N.1. LINKING ARRANGEMENTS

LOWEST REGISTER ADDRESS. (I/O MAPPED - L1 & L6)
0 = link closed, 1 = link open.

Standard Factory Setting = 100_H

Link	L6					L1			
		8	7	6	5	4	3	2	1
ADDRESS WEIGHT	ADR F	ADR E	ADR D	ADR C	ADR B	ADR A	ADR 9	ADR 8	ADR 7
FACTORY SET LINKS	0	0	0	0	0	0	0	1	0

NOTE: for ADDRESS BIT ADR F = 0 Link L6 a-b
ADR F = 1 Link L6 a-c

24 bit ADDRESSING LINKS (L2)

With 20 bit Addressing leave all unlinked
With 24 bit Addressing connect all 4 links.

LOWEST DATA PAGE ADDRESS (Memory Mapped - L4)

STANDARD FACTORY SETTING - Data Page Disabled.

Link	L4													
	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Address Weight	ADR 17	ADR 16	ADR 15	ADR 14	ADR 13	ADR 12	ADR 11	ADR 10	ADR F	ADR E	ADR D	ADR C	ADR B	ADR A
Factory Set Links	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTES: The Data Page Address Must be a multiple of the Data Page Size.

2. L4/1,2 & 3 are also affected by Data Page Size.

TABLE N1 Contd.

Data Page Size (L3)

NOTE. Data page size patching sometimes modifies the lowest page address patching as shown in table below.

Block Size Words	L3 Links			L4 Links		
	3	2	1	3	2	1
512	0	0	0	X	X	X
1024	0	0	0	X	X	1
2048	0	1	1	X	1	1
4096	1	1	1	1	1	1

X = don't care - These will be patched according to the address allocated.

Standard Factory Setting = Data Page Disabled.
L4/1 link made.
L3/1 link open.

Interupts - L5.

L5/1 --- L5/8 link to INT0 --- INT7 respectively.

Figure N1 shows locations of link fields as w/w card.

IMPORTANT NOTE. At no stage must the 214 Register Addresses co-incide with any of the Data page addresses.

N.2 Circuit Description - Circuit Diagram Number 02-586

N.2.1 214 Addressing

Address recognition is achieved via 2 sets of Comparitors.
a) 14B for Register Addressing - I/O mapped.
b) 12B and 13B for Data page addressing - Memory mapped.

The addresses are set by wire links which feed to one side of the comparitors.

N.2.1.1. Register Addressing

The output of 14B is "ORed" with the output of 12B. It is also gated with the multibus I/O control signals IORC and IOWC (11D). This ensures that when the same address is O/P by the computer in the main memory area, the 214 does not respond.

N.2.1.2. Data page addressing

The gating of 12B is similar to that of 14B except that it is gated with multibus memory control signals MRDC and MWTC.

N.2.2. Write Sequence

The multibus write signals MWTC and IOWC are gated together (IOD) to produce a single write signal for the 214. The write signal is gated with address recognition. This signal is then delayed via an RC network to satisfy the timing requirements of the 214 bus. Write is then O/P on to the 214 Bus. Because it is a write transfer 19B/8 and 19B/2 are low thus setting up the Data path transfer from multibus to 214 Bus.

The 214 acknowledges receipt of the data with signal REPLY. This is gated with address recognition and the Multibus control signals and O/P's as multibus signal XACK. The multibus write signal will then be removed which in turn will remove the 214 reply thus terminating the write sequence.

N.2.3. Read Sequence.

The gating for the Read path is identical to that of the write path except that 19B/2 and 19B/8 go "high" thus setting up the data transfer from 214 bus to Multibus.

N.3. Interupts.

The 214 can produce interupts which are fed straight through the 214 interface and can be linked to any of the 8 multibus interupt lines.