To verify the address computation, The AC.READ+ signal (EC pin AA1) from the Control PCB is set and enables transceivers a4, a5, a6. This allows the memory address to be placed onto the hgihway for transmission to the computer.

5.4 Syncs and Timing

The Syncs and Timing PCB generates the required timing waveforms to ensure synchronisation of the picture memory and television signals. The timing waveforms may be derived from either a crystal oscillator arrangement on the PCB or an external clock. The board is mounted in postion no. 3 of the control backplane, and the circuit arrangements are shown on Drg. 02-514.

Connections with other PCBs in the control backplane are made via edge connector sockets (EC).

5.4.1 Video Monitor Synchronisation

A variable range of video monitor synchronisation signals is provided in order to accommodate standard or non-standard monitors. These signals are derived from the 15MHz or 20MHz SYSTEM CLOCK. The basic timing signals required by a monitor for non-interlaced display are shown on Fig. 5.5. A block diagram of the monitor synchronisation signal generation is shown on Fig. 5.6.

5.4.2 Line Timing Signals

The HALF LINE counter comprises binary counters 13B, 12B. It counts down to zero from the number preset by inputs HL0 - HL5, and is clocked by memory cycle pulses out of the divide-by-16 counter, 12D. The ripple carry output on 12B pin 15 goes low at the end of every half line, and this causes the LINE flip-flop 11C pin 15 to change state for each half line. It is set high for a first half line, low for a second half line. Nand gate 6D ensures that the LINE flip-flop is correctly oriented after power-up.

The line unblank period starts when the output of the LINE UNBLANK DELAY comparator, on 11B pin 6, goes high. This clocks the LINE UNBLANK flip-flop (11C pin 6) which in turn loads the LINE UNBLANK DURATION COUNTER 12C, 13C. This counts down from the number preset by inputs VP0 - VP2 and is clocked by memory cycle pulses. The line unblank period is terminated when the ripple carry output 13C pin 15 goes low to reset the LINE UNBLANK flip-flop. The output of this flip-flop is used to gate Scan cycles (7C pin 5), and is inverted by 6B pin 8 to provide the line unblank waveform (LUNBNK).

At the start of each half line, the HALF LINE sequence generator (3D, 1D) produces three pulses, each of 2.4us wide, which after further gating generate the half line datum pulse, the line sync pulse and the equalising pulse. These pulses are used to generate the field synchronisation waveforms (see Fig. 5.1). 3D is a down-counter which is clocked by the divide-by-4 output of counter 12D and is preset with the appropriate number, depending upon the required resolution, to cause the ripple carry output on pin 15 to go low every 2.4us. This pulse clocks the shift register (1D) providing the sequence of three pulses.

The FIELD DURATION COUNTER comprises 9B, 10Band 12Aand is clocked by the half-line datum pulses. It counts down to zero from a number preset on inputs FD0 - FD10 and sets the ripple carry output low which drives the J-K inputs of flip-flop 1A pin 6. This flip-flop switches to define odd and even fields in an interlaced system but is held reset by 1B pin 3 in a non-interlaced system. The field unblank period starts when the FIELD UNBLANK DELAY comparator 9A, 10A & 11A recognises the count preset on inputs FUD1 - FUD10. Note that the least significant bit, FUD0 on 9A pin 10, is driven from the ODD/EVEN flip-flop in interlaced systems because in this case the odd field unblanking is delayed by half a line on the even field.

The output of the comparator (11A pin 6) clocks the FIELD UNBLANK flip-flop 1A pin 1which starts the FIELD UNBLANK DURATION counter (8C, 9C, 10C). This counter is clocked by the half line datum pulse and counts down from the number preset on the inputs VL0 - VL10. When the ripple carry output (10Cpin 15) goes to zero, the FIELD UNBLANK flip-flop is clocked into the alternative state.

The INTERFIELD SEQUENCE generator (4D, 4E) generates the three periods containing equalisation or seration pulses in the field synchronisation waveform (see Fig. 5.1). The counter 4D is clocked by half line datum pulses and counts down from preset number four to zero, at which pointthe ripply carry output on pin 15 goes low. this pulse clocks the shift register 4E which is loaded by a pulse from the FIELD DURATION counter to produce a sequence of three periods at the end of every field. These periods gate the signals from the half line sequence generator in gates 6Eand 6D to provide the field synchronisation waveform.

5.4.3 Memory Cycle Timing

Memory cycle timing waveforms are derived from the SYSTEM CLOCK which may be set at 15 or 20 MHz, depending on the resolution of the display (see Table 5.3). The period of a memory cycle is determined by the divide-by-16 counter 12D. Thus the memory cycle duration (12D pin 11) is 0.8us (20MHz clock) or 1.066us (15 MHz clock). The outputs of 12Dare decoded into 1 of 16 by decoders 9D & 9D which in turn drive flip-flops 8B, 4B, 4C and 3B to determine the memory cycle waveforms (see Fig. 5.8).

RAS and CAS are row and column address strobes respectively. They are gated by Scan and Access cycles to reduce power dissipation in the RAMs on the Memory PCB.

SYNWRI is the memory write synchronisation pulse.

END CYCLE is fed to the Control PCB to signal the completion of a memory cycle.

XY CNT clocks the X and Y access counters on the Address computation PCB when operating in the auto increment mode.

RCS0 is used to select row or column addresses on the Address Computation PCB.

RCS1 selects Scan or Access addresses on the Address Computation PCB.

SCAN UP clocks the scan counter on the Address Computation PCB.

ELCK is the pixel (or ELEMENT) clock (7A pins 12 and 13) which determines the width of pixels and is equal in duration to an integral number system clock pulse depending upon the display resolution (see Table 5.3). Part of 11D is a selector for pixel clock pulses.

5.4.4 Scan or Access Cycle Selection

The repetition rate of Scan cycles required to refresh the video monitor is dependent upon the resolution (see Table 5.3). Memory cycles occuring between Scan cycles in a TV line are available for memory access, as are all cycles during the line blanking period. Memory cycles that are required to be Scan cycles are selected by part of selector 11D. The least significant outputs of the line unblank duration counter are selected, according to resolution, to enable the Scan and access flip-flops (5B) and these are clocked by an output from the memory cycle decoder (4D pin 12).

When the data register holds data to be written into memory, the cycle request flip-flop 3B pin 3 is clocked by the CYC REQ signal on EC pin BE1. The request is then gated through 4A pin 6 during the next Access cycle and the Access cycle flip-flop (part of 5B is clocked by 4Dpin 12. The logic gates at the outputs of the Scan and Access flip-flops enable the SYN WRI pulse and generate the WRD WRI signal for 32-bit word writing. Note that the signal ERS WRI enables 32-bit word writing during Scan cycles for memory erasure. The 32ENB input is set for 32-bit word writing during Access cycles.

TABLE 5.3 DISPLAY RESOLUTION PARAMETERS

Display Resolution	System Clock MHz	Clock Pulses per Pixel	Ratio Scan/Access **	32-Bit Words per TV Line
1024 x 512	20	1	1/1	32
786 x 586	15	1	1/1	24
512 x 512 square	15	1	1/1	16
512 x 512 rect	20	2	1/3	16
512 x 256	20	2	1/3	16
384 x 293	15	2	1/3	12
256 square	15	2	1/3	8
256 rect	20	4	1/7	8

** Cycles during line unblank.

5.5 Memory Planes

Up to 24 Memory PCBs may be included in the Supervisor 214.

Each Memory PCB contains 32 random access memories (RAMs) of either 4k, 16k or 64k capacity, and is capable of storing a picture with one intensity bit. For the graphics (1 bit) mode, up to 16 bits are serialised from the data register and input to all memory PCBs. They are written only into those PCBs which have their access flag set. For the image (6, 8 or 12 bit) modes, the PCBs are divided into groups determined by the required intensity resolution, and the computer word is placed on the internal highway in one or two bytes. The first PCB in each group receives the first bit of each byte, the second PCB receives the second bit, and so on.

For a Scan cycle, data is read from the RAMs to refresh the TV monitors, and for an Access cycle the RAMs are available to the computer for read or write sequences.

The circuit arrangements for each Memory PCB are shown on Drg. 02-479.

5.5.1 RAM Operation

The 32 RAMs on each Memory PCB are arranged in four groups of eight, and the group address is determined by bits M3, M4 from the Address Computation PCB. The actual location within an individual RAM is set by address pins M5 - M12. Note that for 16k RAMs, the chip enable pin, 13, becomes an address line, otherwise the operation of the 4k and 16k RAMs is the same, 64k RAMs, however, have different pin-outs, see circuit diagram 02-588.

Each 4k RAM incorporates 64 internal rows and 64 columns. For addressing purposes two strobe signals are used, the row address strobe RAS and the column address strobe CAS. A RAM is selected when the RAS, CAS and chip enable (CE) pins are set low, and is arranged for read/modify/write operation.

In order to maintain valid data in the RAMs, all rows must be strobed with a RAS signal once every 2 mS. This is automatically provided by Scan cycles.

At the beginning of a read/modify/write memory cycle, signal RAS+, input from the Sync and Timing PCB on EC pin CJ2, is inverted and strobes the row address into the RAM address pins. The row address is derived from bits M5 - M10 (4k RAMs), M5 - M11 (16k RAMs) or M5 - M12 (64k RAMs). from the Address Computation PCB, and selects one of 64 rows. After a predetermined period, the row address bits are removed and the column address is placed on the address pins. This is strobed in by signal CAS- derived from EC pin CJ1. The write input, W, on pin 3 is set high during the column address set-up time, and the data from the selected RAM is output on pin 14. When the write signal is set low, the data on input pin 2 of the selected RAM is written in.

The input data is derived from data selector IC45 pin 5 in the bit loader logic circuit.

5.5.2 Mode Selection

The operating flags for each Memory PCB are contained in addressable latch IC57. At power up or when a new program is loaded, the INIT- signal on EC pin AV2 clears IC57.

When the computer wishes to access a Memory PCB, the memory flag clock is input on EC pin BT2 and enables B3 so that the output of the addressed latch follows the inverted memory flag input, MSK.DATA, (EC pin AP1). Address bits A0, A1 determine which flag is selected:

A0	A1	Flag	
H	H	Output Inhibit	B3 Pin 4
L	H	Input	B3 Pin 5
H	L	Foreground	B3 Pin 6
L	L	Background	B3 Pin 7

5.5.3 Scan Cycle

During the memory cycle read sequence, data from 32 RAM locations, as selected by memory bits M5 - M10 (M11), is output to a 32-bit shift register comprising A6, A8, A10 & A12. These are set up for parallel-in/serial-out operation and are clocked at pixel rate by the element clock signals EL.CLK+ and EL.CLK-, input from the Sync and Timing PCB on EC pins CF2 and CF1, via receiver A7 pin 13. The shift/load inputs on pins 3 of the shift register are controlled from flip-flop C3 pin 8. This flip-flop is clocked at pixel rate, and the data input is derived from the LOAD- and LOAD+ signals (EC pins CH2, CH1) via receiver A7 pin 11. When the shift/load inputs are set low, the 32-bit data from the RAMs is input in parallel to the shift register. It is clocked out in serial format from A6 pin 13 and applied to the data input of flip-flop C3 pin 2 which is also clocked at pixel rate.

For graphics applications video data is fed through the 75-ohm output to a display monitor, and for imaging applications, where further processing of the video signal is required, data is fed through a balanced line driver E4. These outputs are controlled by the OUTPUT flag and the REMOTE and OVERLAY inputs (see Para. 4.2.6). Composite syncs are also mixed with video data in the 75-ohm output .

5.5.4 Access Cycle

For Access cycles, available between Scan cycles for random access by the computer, the input flag from B3 pin 5 is used to enable read and write decoders B4 which select one group of eight RAMs for the read/modify/write sequence. The input flag also gates the block write signal, WRD.WRI on EC pin BV2, into the write PROM address lines. The foreground and background flags provide the select signals, along with the additive mode signal ADD- on EC pin BP1, for the write data decoder D3.

The group address decoder B4 pin 1 is enabled when the input flag is set high. During the read sequence of the memory cycle, the data from the selected RAM locations is output to data multiplexers is enabled, as determined by memory bits M3, M4, and selects one of the eight RAM data inputs, as determined by memory bits M0, M1, M2. The data bit is input to decoder D2 which selects one of eight outputs according to signals MODE0, MODE1 and BYTE which indicate the required data mode. The selected output is placed on the internal highway via transceiver A1 or A2 which is enabled by the inverted DAT.WRI+ signal on EC pin BP2 and the signal from B3 pin 5.

During the write sequence of the memory cycle, the input flag from B3 pin 5 is gated with the SYN.WRI+ signal on EC pin BV1 to enable decoder B4 pin 15. This decodes bits M3, M4 to identify the required RAM group address and enable the associated PROM (B5, B7, B9 or B11). The PROM decodes address M0, M1, M2 and sets the write signal, W- on pin 3, on the addressed RAM. Simultaneously, a data bit is read out from the RAMs as described above but is not enabled onto the internal highway. Instead it is input to the bit loader logic with the write data from the micro-computer. The bit loader logic processes the memory data and the computer data according to the setting of the additive, background and foreground flags and generates the data bit to be written into memory.

5.5.5 Bit Loader Logic

The additive flag, ADD- on EC pin BP1, is common to all Memory PCBs and determines whether the data from the computer replaces or is added to the existing data in the RAMs. The foreground and background flags are derived from addressable latch B3 pins 6 and 7, and are individual to each Memory PCB. In combination with the additive flag, they determine the logic of loading. The flags are input to the select pins of data selector D3 (pins 9, 11, 10) and the resulting data output is derived from a combination of the RAM data bit and/or the new computer data bit as shown in the Table below:

BG	FG		
Replacement Mode : ADD flag set high (IC45 pin 9 low)			
0	0	D3 pin 4	(Data bit 0)
0	1	D3 pin 3	(True Computer bit)
1	0	D3 pin 2	(Inverted computer bit)
1	1	D3 pin 1	(Data bit 1)
Additive Mode:		ADD flag set low (IC45 pin 9 high)	
0	0	D3 pin 15	(RAM bit and inverted computer bit)
1	0	D3 pin 13	
0	1	D3 pin 14	(RAM bit or true computer bit)
1	1	D3 pin 12	

As can be seen above, in replacement mode when neither the foreground nor the background flag is set, the data is ignored and logic 0 is loaded into the selected RAM. Similarly, if both flags are set, logic 1 is loaded.

5.5.6 Data Distribution Modes

1. One Bit Mode: Up to 16 bits are selected in turn from the computer word and written to pixel locations in the Memory PCBs. In each write cycle, all PCBs receive the same data bit, but it is written only into those which have their access flag set.

The data is serialised onto the one bit highway (1 BITHW- on EC pin BN2) in the Control PCB. It is input to each Memory PCB via transceiver A1 and applied to selector D1 pins 4 and 15. For one bit mode, the BYTE- signal is ineffective, and the MODE0 and MODE1 signals are both low.

2. 6 Bit Mode : 6 bits from the lower and upper bytes of the computer word are selected alternately and written to the Memory PCBs. The lower byte comprises bits 0 - 5 and the upper byte bits 8 - 13. All PCBs do not receive the same data bit. They are divided into groups of sic (PCBs 0 - 5, 6 - 11, 12 - 17, etc.) and the first PCB in each group receives bits 0 and 8, the second bits 1 and 9, and so on. The lower byte bit is input to the Memory PCB on EC pin AL2 as signal 6LB, and the upper byte bit on EC pin AM1 as 6UB. They are input to D1 pin 3 and 14 respectively.

   For 6 bit mode, signal MODE0 is high and MODE1 low, and the BYTE input is low for lower byte, high for upper byte.

3. 8 Bit Mode : This is similar to the 6 bit mode. 8 bits from the lower and upper bytes of the computer word are selected alternately and written to the Memory PCBs. In this case, the lower byte comprises bits 0 - 7, and the upper byte bits 8 - 15. The memory PCBs are divided into groups of eight, and the first PCB in each group receives bits 0 and 8, etc. The lower byte bit is input to the Memory PCB on EC pin AM2 as signal 8LB, and upper byte bit on EC pin AN1 as 8UB. They are input to D1 pin 2 and 13 respectively.

4. 12 Bit Mode : Bits 0 - 11 of the computer word are written into the Memory PCBs. The PCBs are divided into two groups of 12, and the first in each group receives bit 0, the second bit 1, and so on. Each bit is input to the Memory PCB on EC pin AN2 as signal 12 BIT.

5. 32 Bit Mode : This mode is used if the computer wishes to write a solid block of picture data, 32 pixels wide, into the Memory PCBs simultaneously in one write cycle. The word write signal, WRD.WRI- is set on EC pin BV2 and is gated with the input signal from B3 pin 5. It is then further gated with the SYN.WRI signal to set the address D input on the PROMs (B5, B7, B9 and B11 pins 13) so that all 32 RAMs are enabled for the write mode.

   This mode is also used for automatic erase when selected during a Scan cycle. In this way the complete visible image is erased in one frame period.

Fig. 5.8 shows the 32 bit word patterns generated by the least significant bits of the X address when the 32ENB or ERS.WRI bit is set.

5.5.7 Real Time Frame Capture

Without frame capture the data selectors (E5 - E12) are not fitted. Links are fitted to enable writing of data to the RAMS via D3. With frame capture E5 - E12 along with shift registers F6, F8, F10, F12 and latches F5, F7, F9, F11 are all fitted.

The method in which frame capture is achieved is to set the additive flag and the erase flag in the command and status register. At the start of the next complete frame the 214 hardware will set WRD.WRI and ADD. These two are gated and set the data selectors E5 - E12 to transmit the video source data to the RAMs. as for 32 bit Mode (see 5.5.6 for description).

The video data is fed from the image input card through data receiver E2 to a 32 bit shift register (F6, F8, F10, F12). When 32 bits have been shifted in SYNCWRI clocks the data into a 32 bit latch (F5, F7, F9, F11) which is clocked into RAMs via the data selectors.

When the whole frame is captured the data selectors (E5 - E12) are switched back to transmit computer data.

5.5.8 Hardware Area Fill

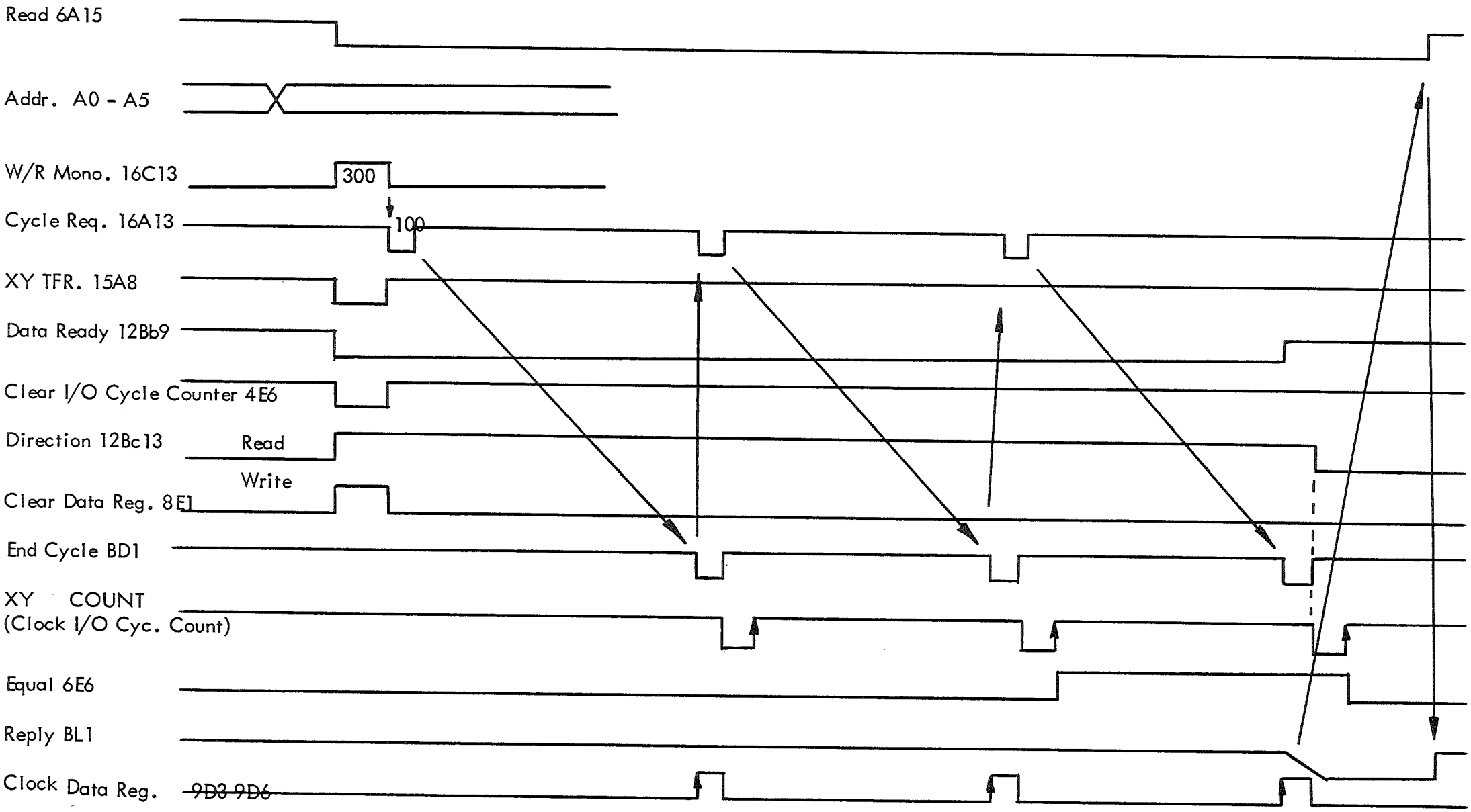
Hardware area fill is controlled by flip-flop F2a. When B3 pin 9 is low, F2a is held reset via F3 pin 4 and F3 pin 1, and area fill is disabled. When B3 pin 9 is high, flip-flop F2a is clocked on or off by a pixel or a group of contiguous pixels out of C3 pin 6. Flip-flop F2a is cleared by line sync, so that the first pixel or group of contiguous pixels turns area fill on and the next pixel or group of contiguous pixels turns it off. Thus in any TV line, odd numbered pixels or groups of contiguous pixels turns fill on, and even numbered ones turn it off. The output of flip-flop F2a (pin 7) is ored with the pixel stream from C3 pin 6 and overlay pixels at F1 pin 12 before being clocked out at F2b pin 6.

5.6 Display Formatting

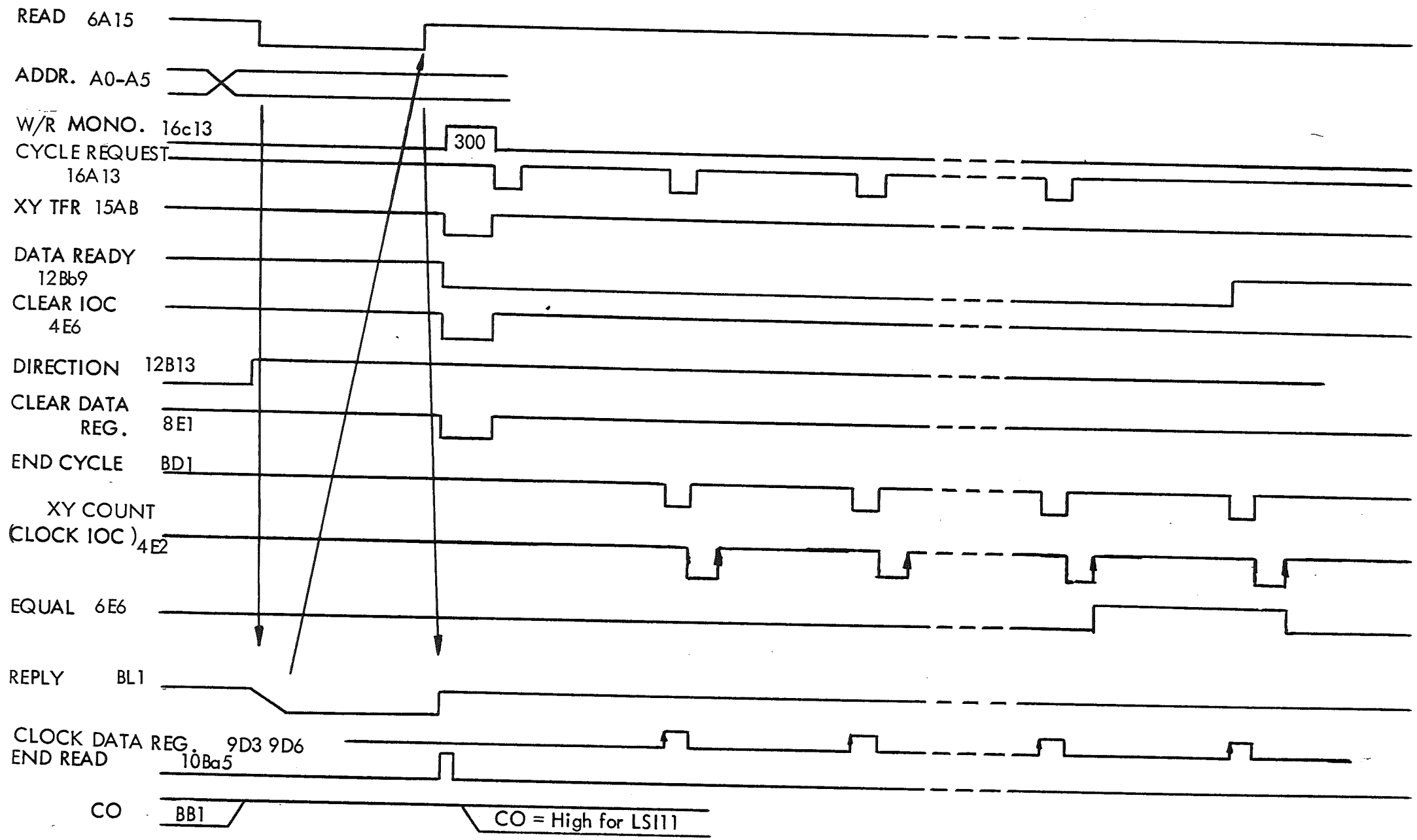
The Format PCB is situated in position no. 2 in the control backplane. Connections with other PCBs in the Supervisor 214 are made via edge connector sockets (EC).

The formatting PCB selects timing signals and picture parameter codes. Standard Format PCBs set up for the commonly used resolution settings are available, or a PCB may be supplied which has been hard-wired to a predetermined specification. In addition, a programmable format PCB is available. The board comprises four registers which must be correctly set up and addressed to provide the required signals for the Sync and Timing PCB or for the Address Computation PCB. See Appendix C.

FIG. 5.1 DATA REGISTER LOW COUNT READ



DATA REGISTER HIGH COUNT READ FIG . 5.2



DATA REGISTER LOW COUNT WRITE FIG. 5.3

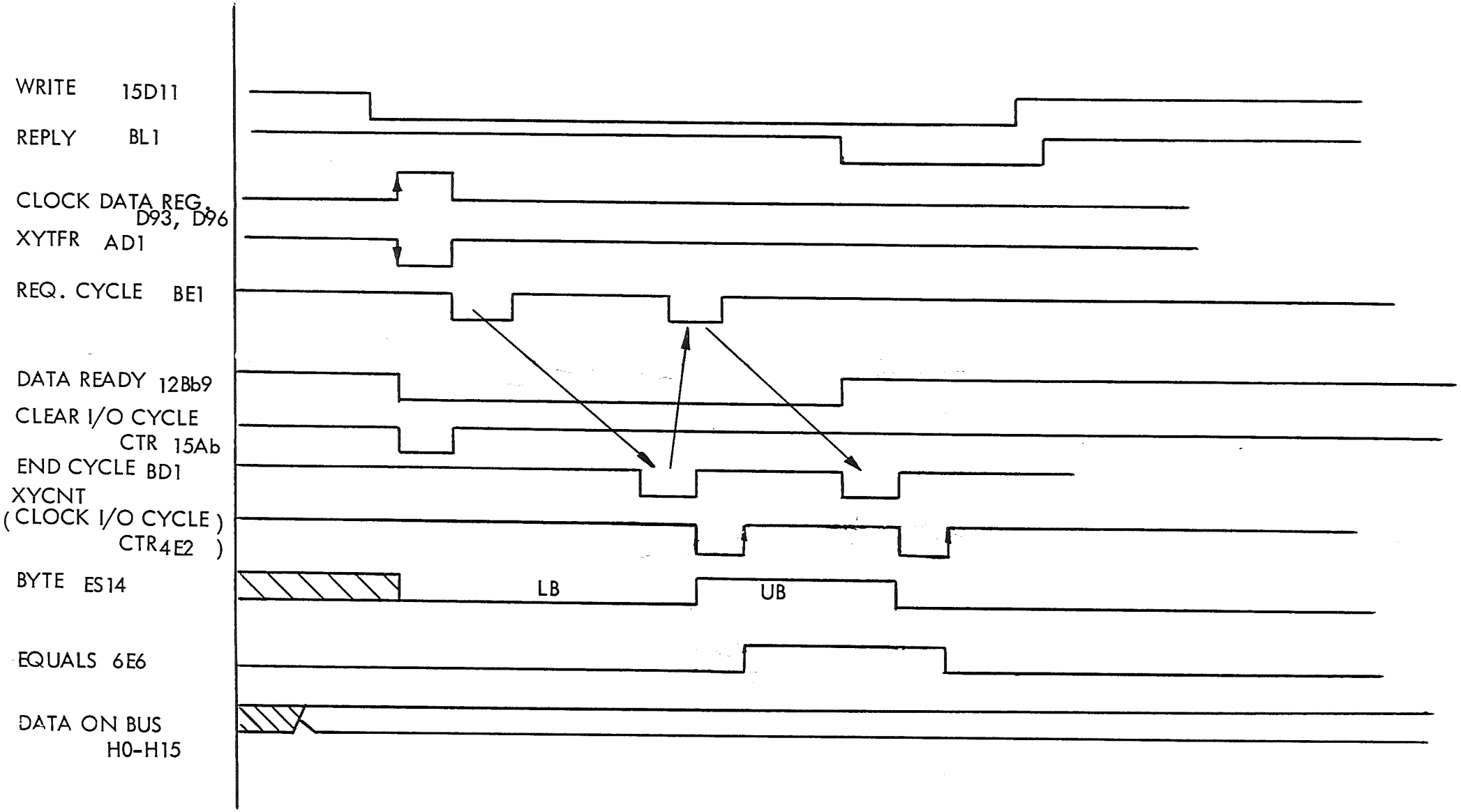


FIGURE 5.4 DATA REGISTER HIGH COUNT WRITE

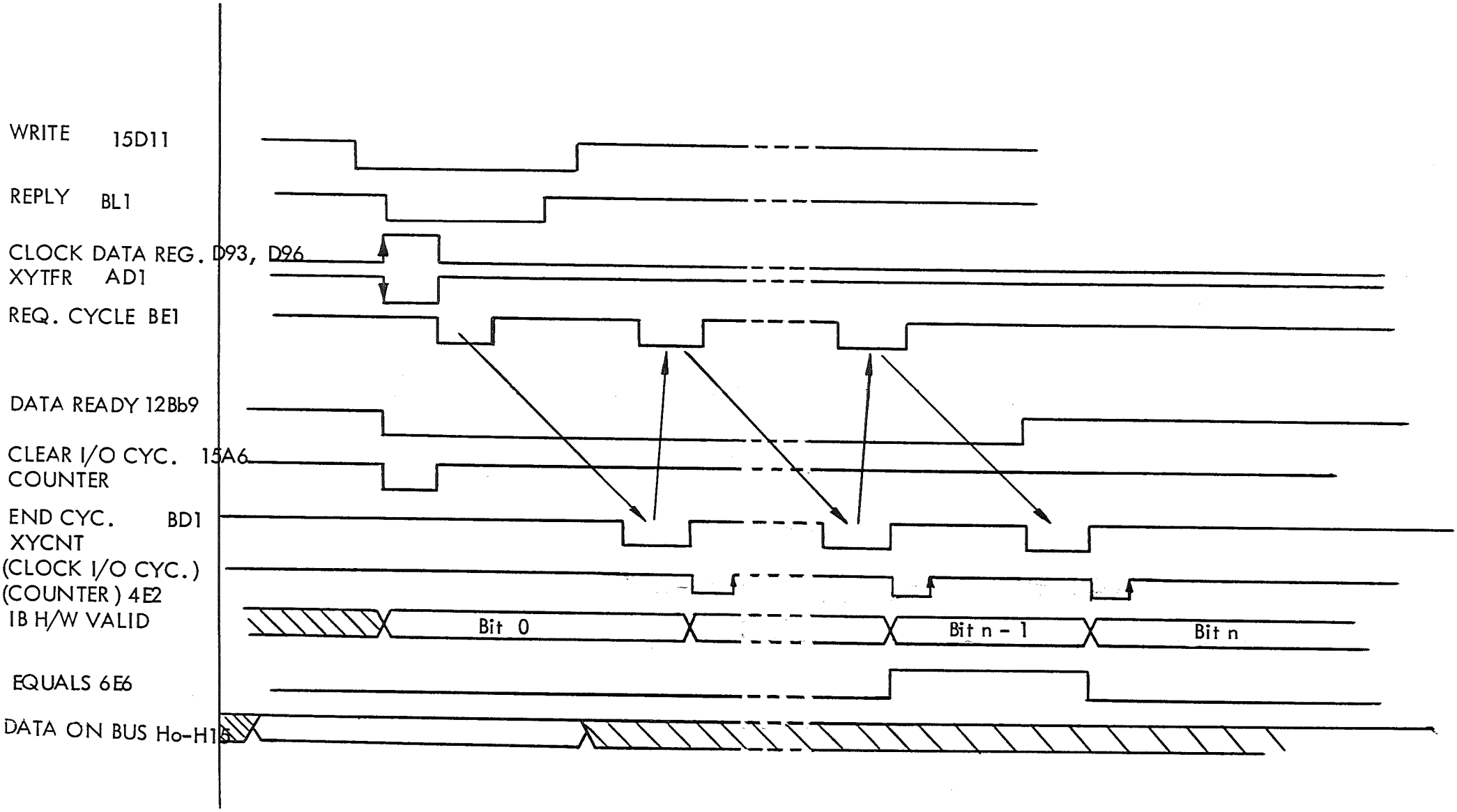


FIGURE 5.5 BASIC VIDEO MONITOR TIMING SIGNALS (NON-INTERLACED DISPLAY)

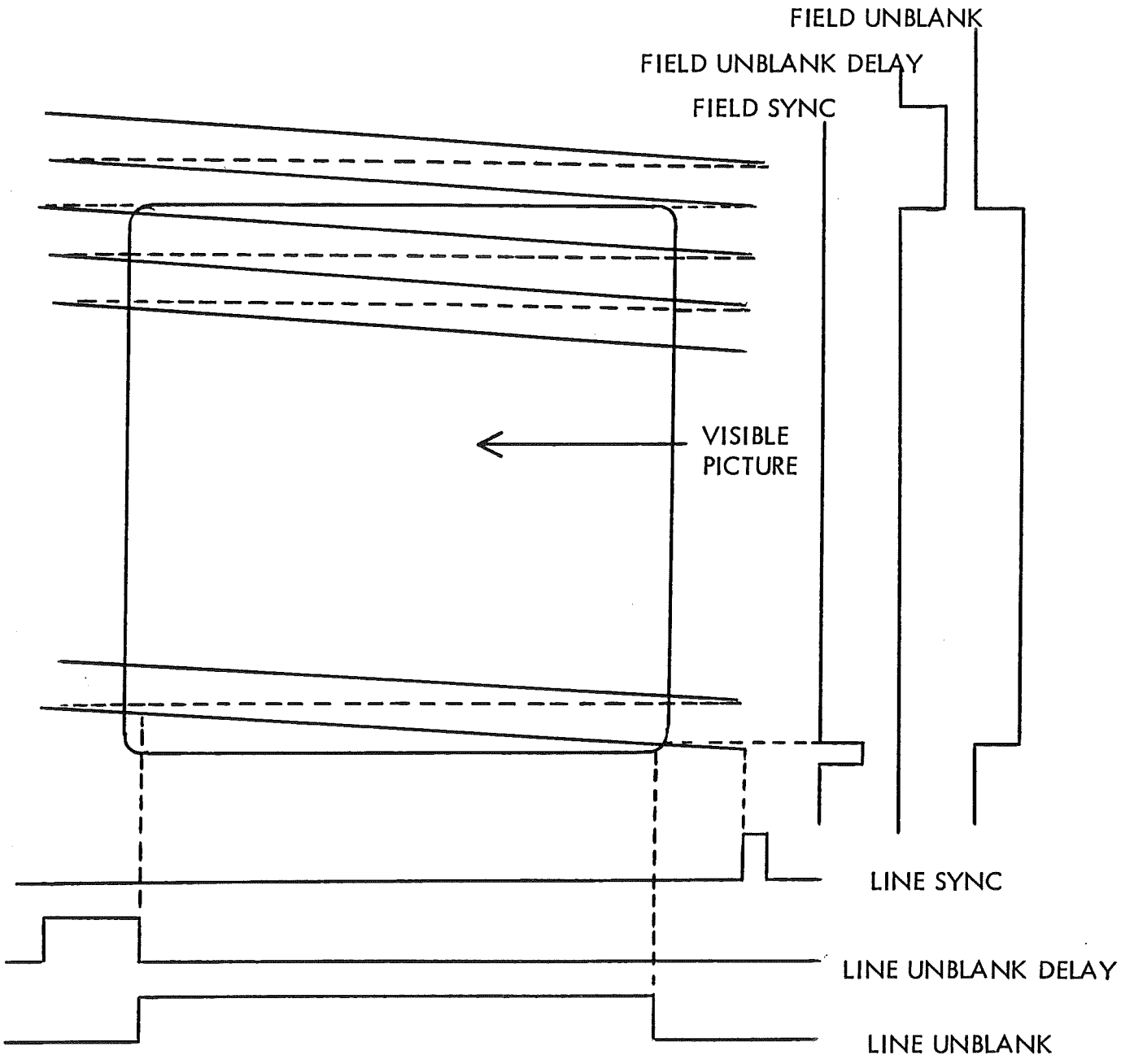
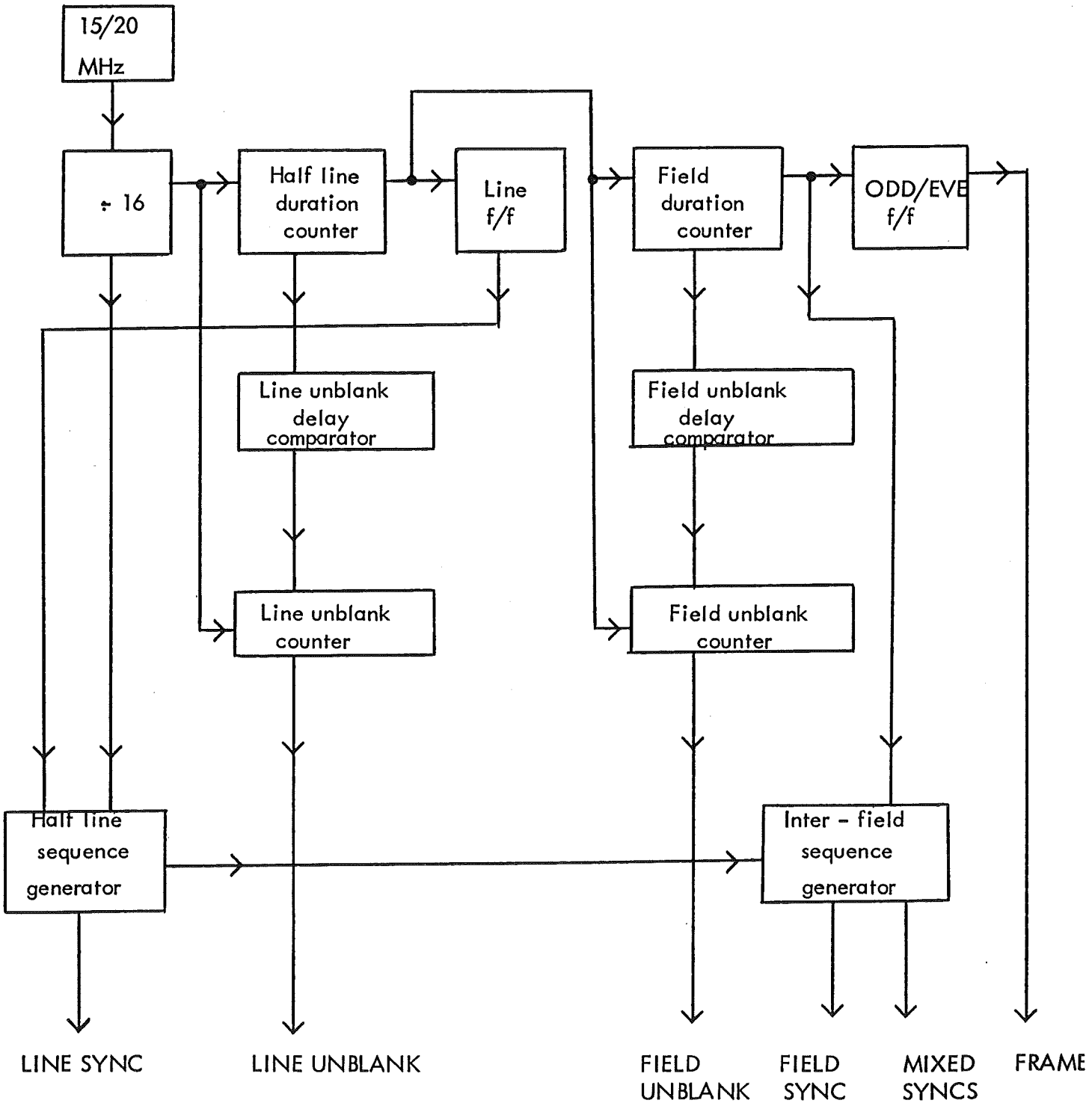
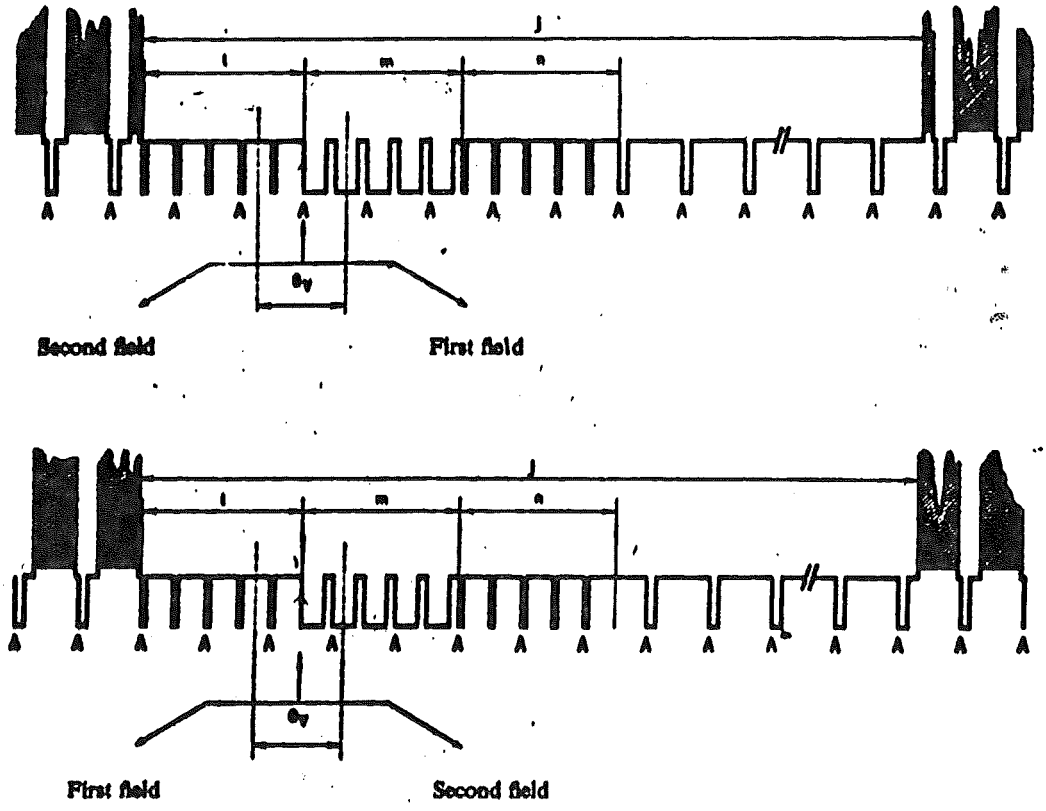


FIGURE 5.6 MONITOR TIMING GENERATION BLOCK DIAGRAM

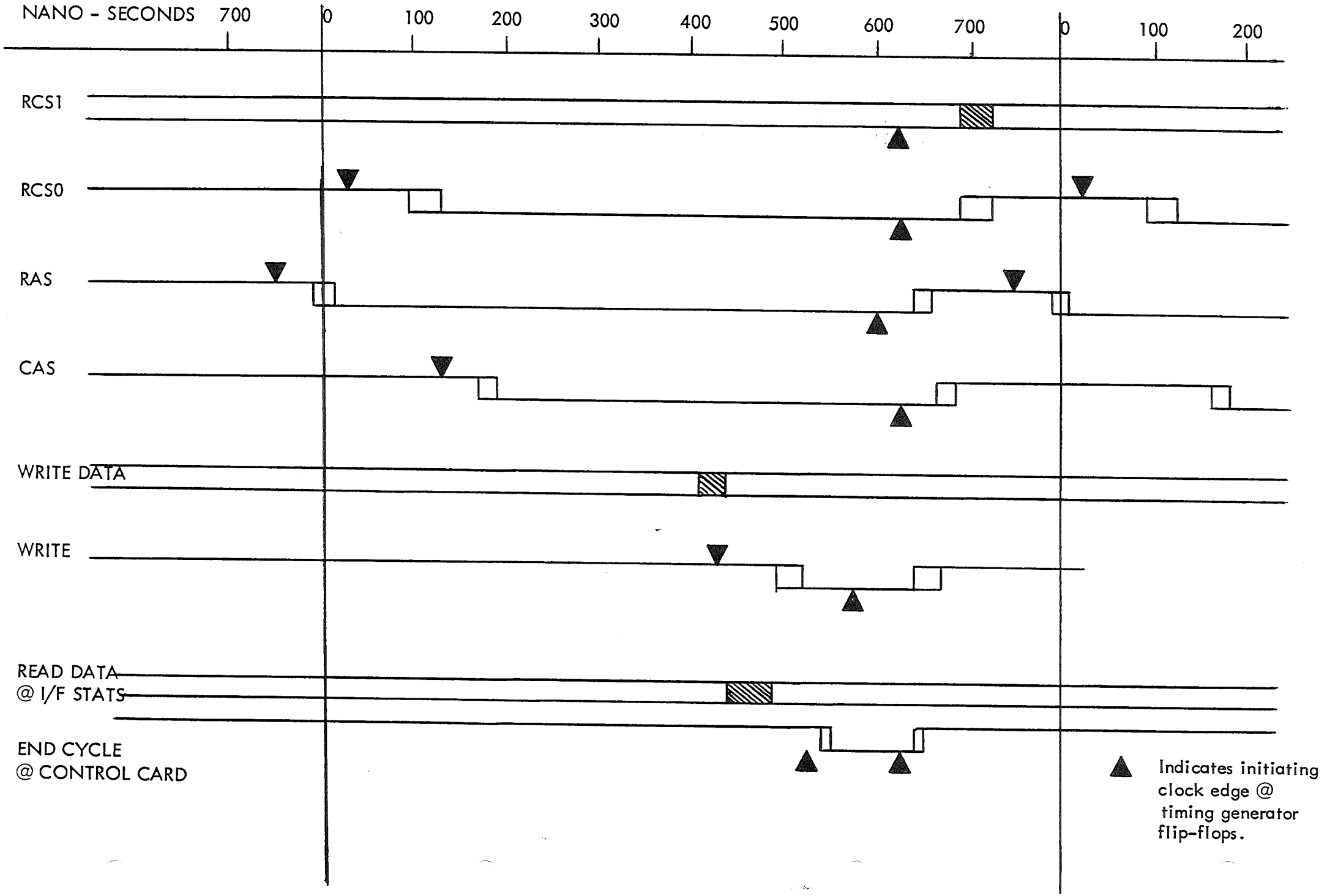




Note: l represents equalising pulses
m represents seration pulses
n represents equalising pulse
from the end of n to the end of j are line sync pulses

FIGURE 5.7 FIELD SYNCHRONISING WAVEFORMS

FIGURE 5.8 MEMORY CYCLE TIMING FLIP FLOPS - 20 MHz CLOCK



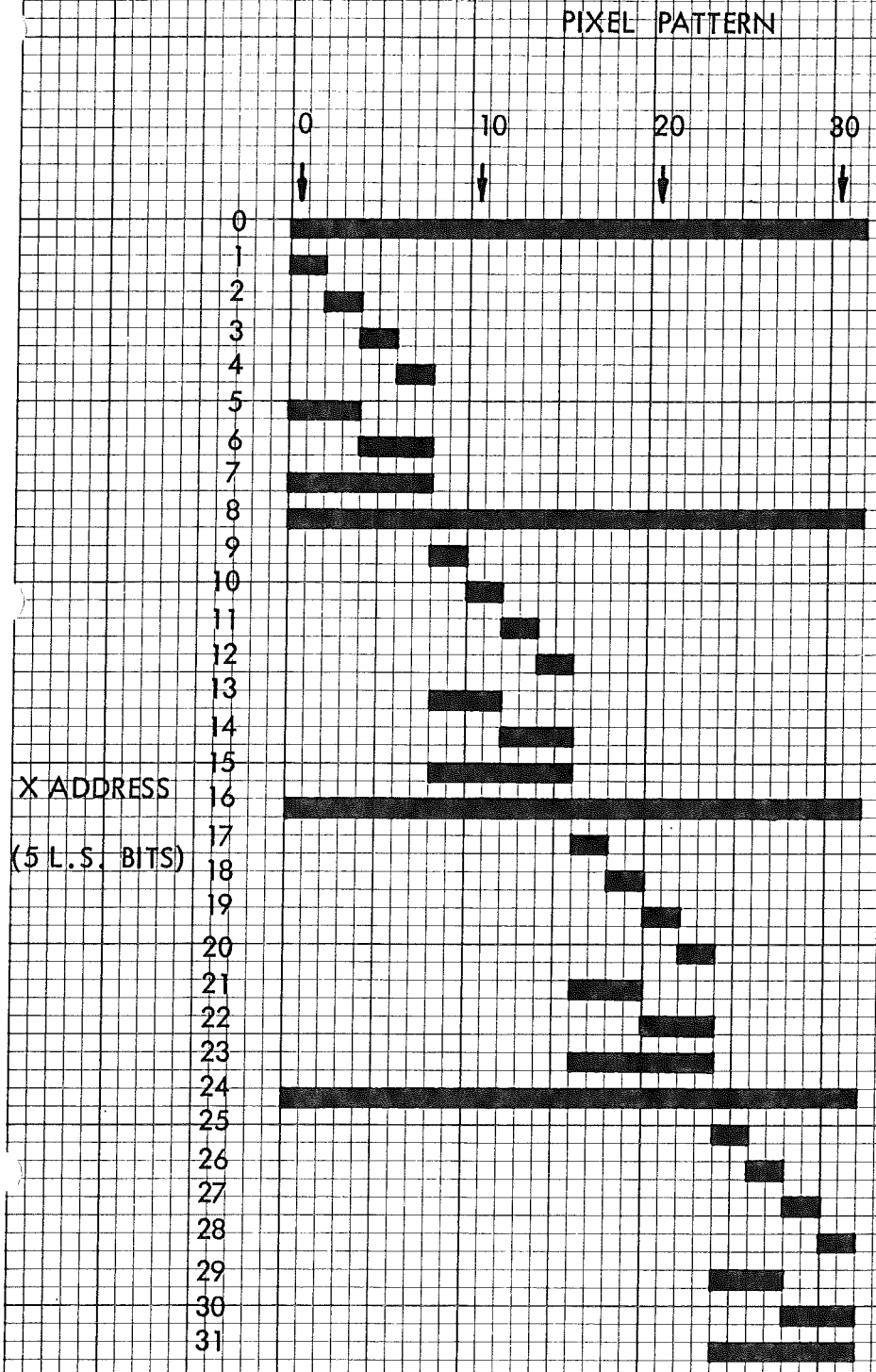


FIGURE 5.9 32 BIT WORD WRITING

SECTION 6

ROUTINE MAINTENANCE AND SERVICING

6. ROUTINE MAINTENANCE AND SERVICING

6.1 Access

Access to the Supervisor 214 may be gained by extending it along the telescopic runners. Ensure other equipment in the cabinet is secured in the rearmost position to prevent the cabinet from toppling forward.

Press the buttons by the front panel handles simultaneously, and carefully pull the chassis out along the runners.

6.2 Filter Servicing S214SB See Appendix J8.1

IT IS RECOMMENDED THAT AIR FLOW FILTERS ARE CLEANED REGULARLY (depending on the environmen

The filters are situated on the right hand side of the chassis and may be cleaned with a vacuum cleaner in situ. If degreasing is necessary, they may be removed and washed in a weak solution of warm water and detergent. Unclip the two retaining fasteners & remove the front panel. Pull out the framed filter assy.

DO NOT replace the filters until they are perfectly dry. Carefully slide the filter assembly back in position . Replace the front panel.

6.3 Power Supply Removal S214SB See Appendix J8.2

1. Ensure that the S214 is disconnected from the mains supply.
2. Remove the bottom cover plate.
3. Remove the two grey mains connector plugs.
4. Disconnect the +12v, +5v, -5v, 0v leads at the bus bars.
5. In order to gain access to any of the power supplies the complete power supply module must be removed from the S214. Remove the screws at the four corners of the module and withdraw it from the S214.
6. The -5v supply is integral with the power supply module. To gain access to the -5v supply, remove the four screws securing the back panel of the module.
7. The +5v and +12v supplies are modular and either may be removed as follows.

8. Remove all connections to the power supply in question.

9. Remove four screws in the corners of the grill at the side of the power supply. Withdraw the power supply.

6.4 Cooling Fans (S214 SB See Appendix J8.2)

Access to the fans is achieved as follows :

1. Unclip the two retaining fasteners and remove the front panel.

2. Slide the filter assembly forwards and remove.

3. Each of the four fans is retained by four screws and electrical connection is made by soldered joints.

SECTION 7

BACKPLANE CUSTOMISATION

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Drawings

7. BACKPLANE CUSTOMISATION

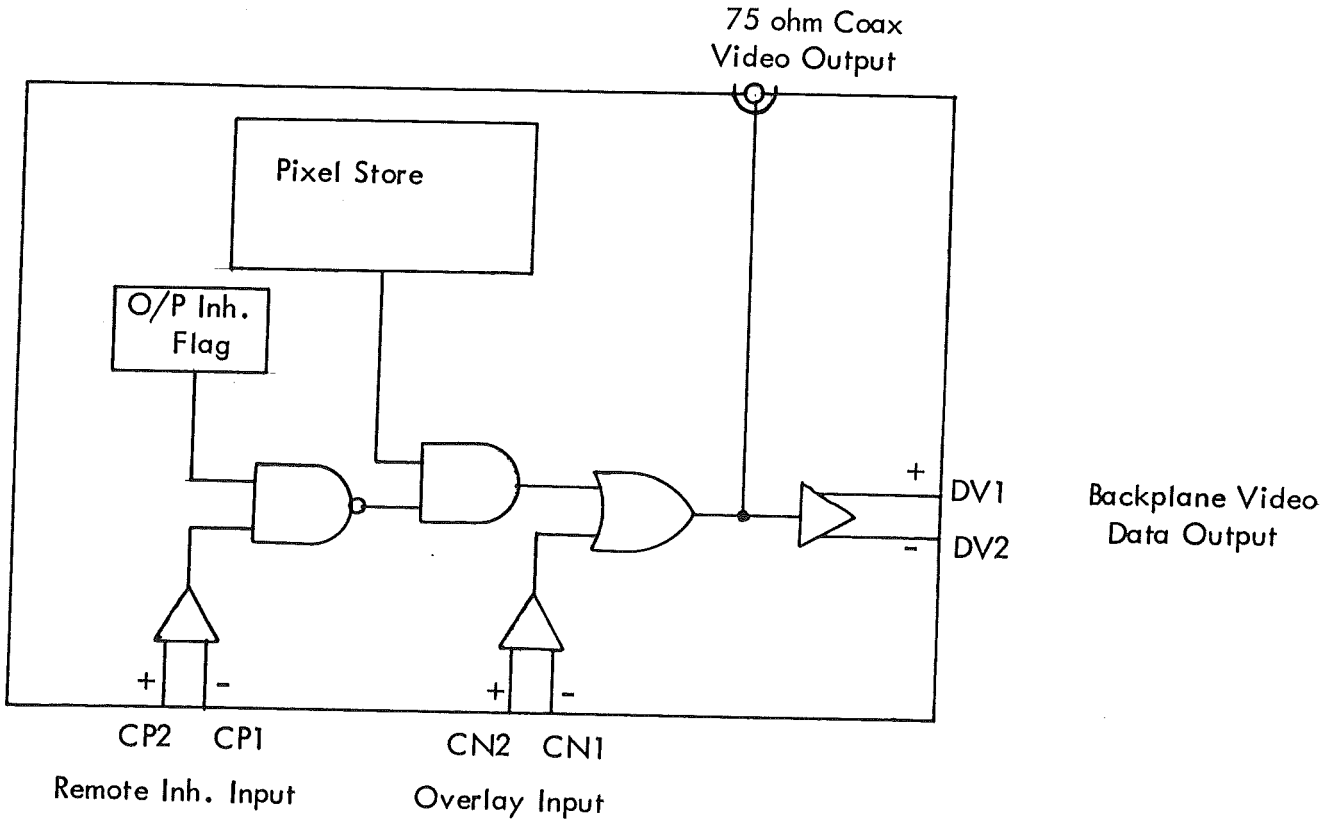
Backplane custom wiring determines the manner in which binary video signals from memory planes, cursors, ascii generators etc. are controlled and routed to meet the requirements of particular systems. There are two distinct ways of achieving this.

a. For simple graphics systems, customisation may be achieved by the interconnections of memory planes, cursor boards, ascii generator boards etc. taking the final video output directly from memory planes, and not utilising output boards.

b. For more complex graphics systems and imaging systems, the outputs of these boards are connected to an output board where signal selection and look-up table processing takes place.

7.1 THE MEMORY PLANE

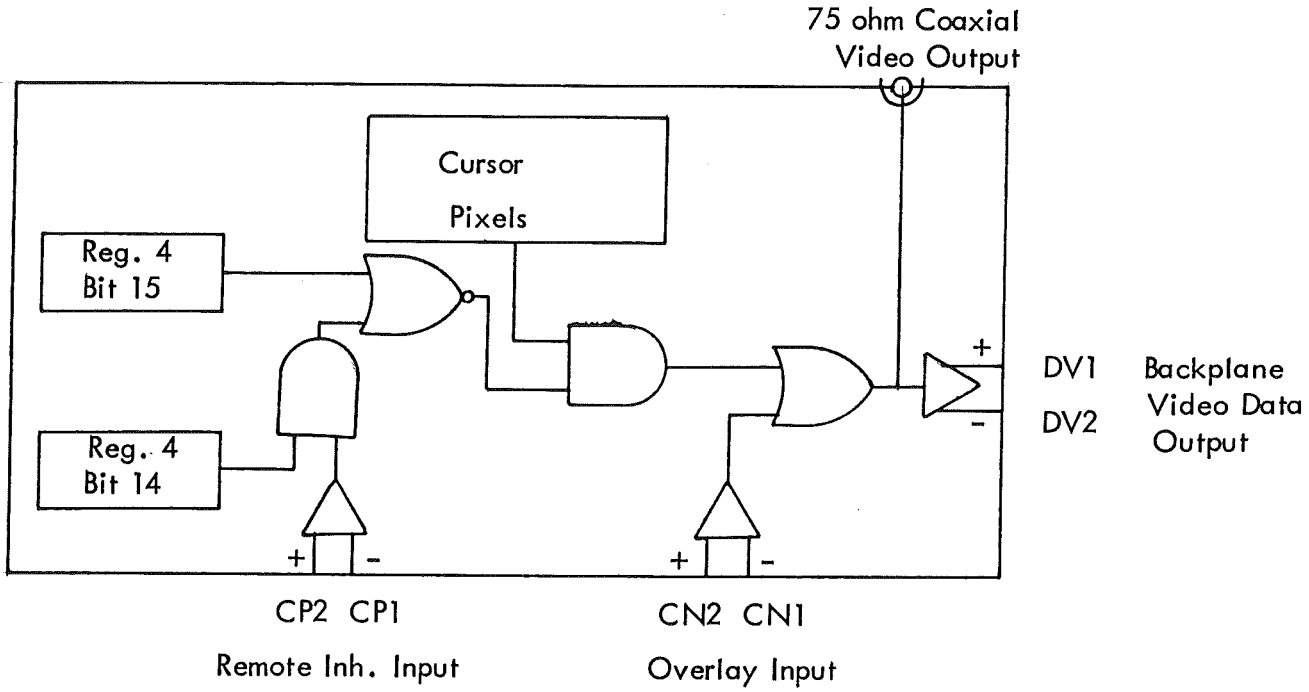
The logic and circuit board connections of the memory plane, concerned with customisation are shown below.



Both the REMOTE INHIBIT INPUT and the OUTPUT INHIBIT FLAG must be asserted to inhibit pixels from the on-board pixel store. Pixels introduced at the OVERLAY INPUT are ORED into both outputs. Overlay pixels are independant of both inhibits. The + and - signs indicate polarities when the respective signals are asserted.

The output inhibit flag is a bit in register number 8 or 12 (see table 4.1) and the remote inhibit input and overlay input are backplane connections.

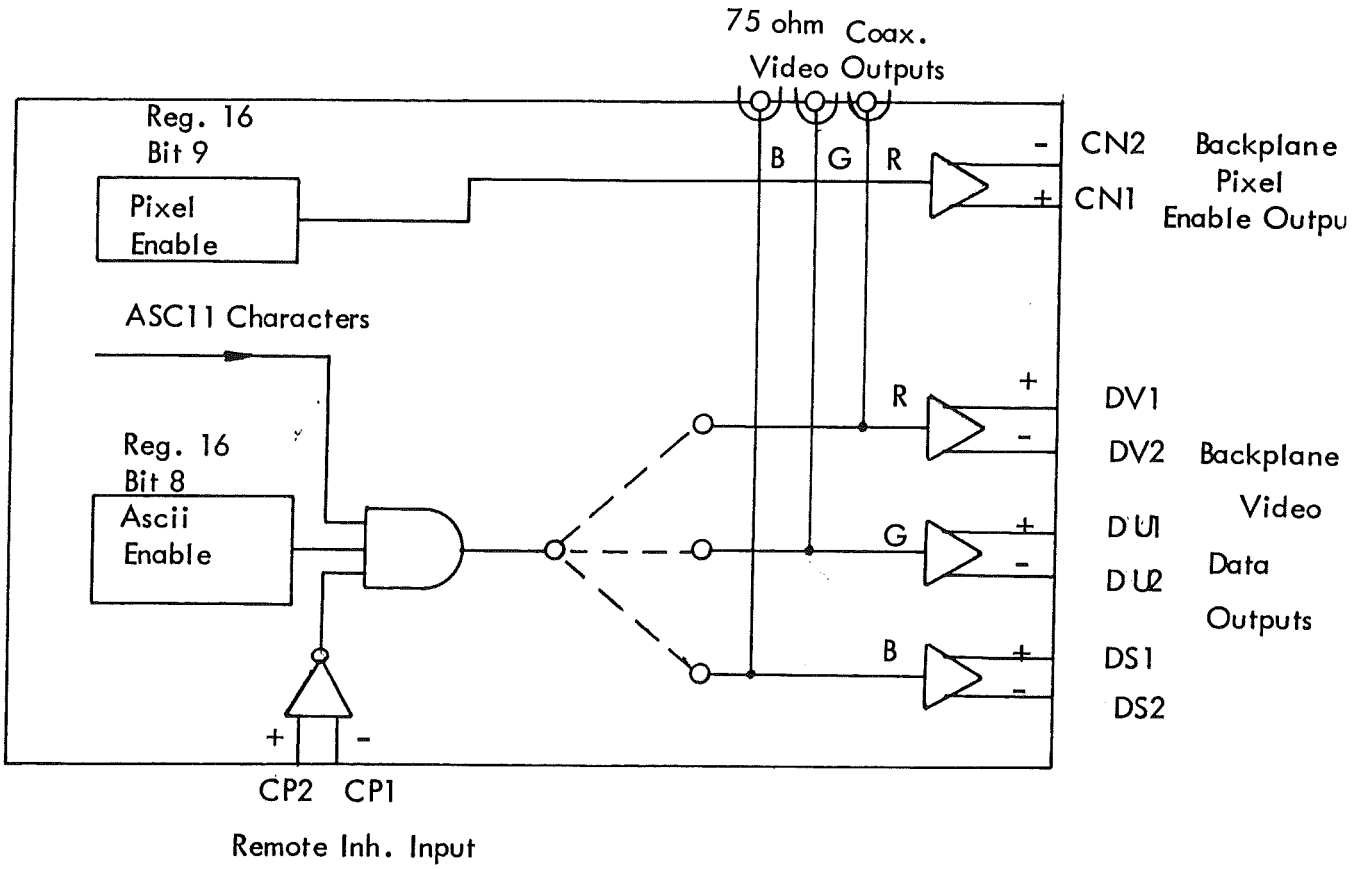
7.2 THE HARDWARE CURSOR



Customisation circuit board connections of the hardware cursor are identical with those of the memory plane. The logic is similar except that the cursor has an additional inhibit flag (REG4, BIT15, See Appendix D.3), which is independant of the REMOTE INHIBIT INPUT, and may be used to facilitate a flashing cursor as follows. The flashing waveform on a backplane pins CK1, CK2 is connected to cursor board pins CP1 and CP2 respectively. Register 4, bit 14 is set for a flashing cursor and cleared for a steady cursor. Register 4 bit 15 is set to inhibit the cursor and cleared to enable it. The + and - signs indicate polarities when the respective signals are asserted.

7.3 THE ASCII CHARACTER GENERATOR

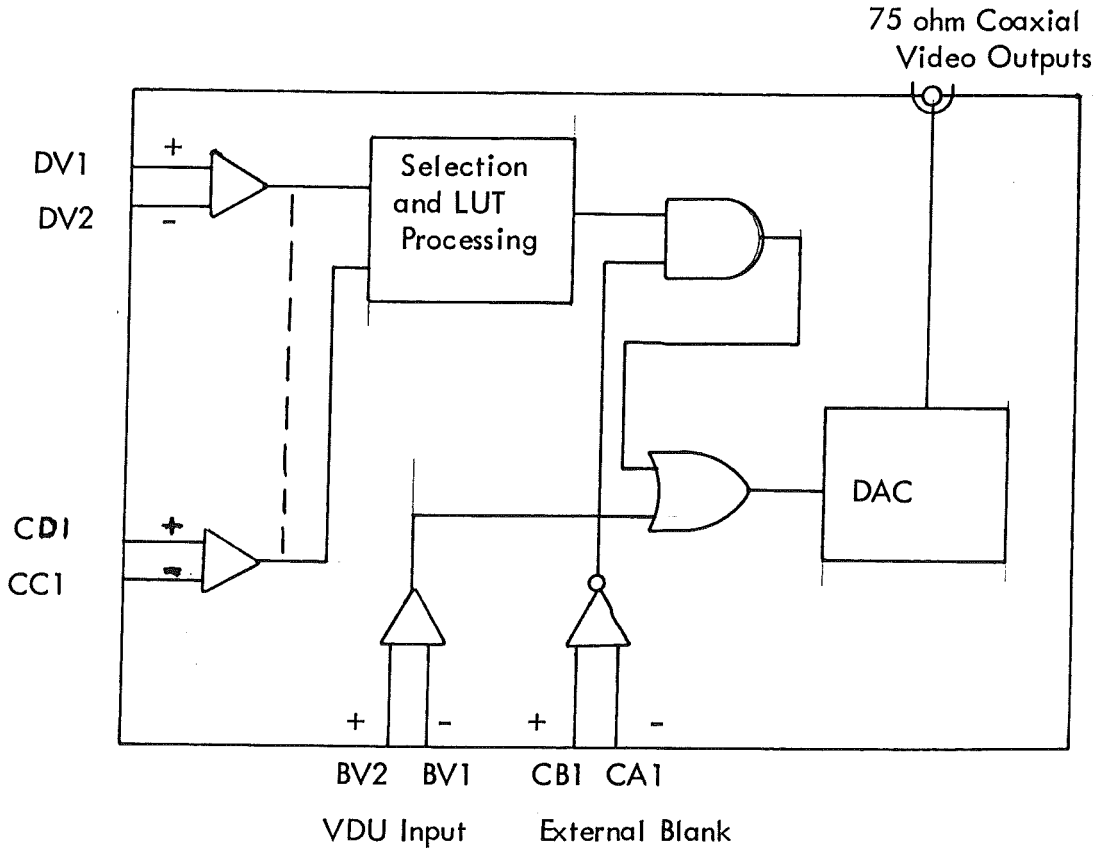
Customisation facilities of the character generator board are different from the memory and cursor boards.



The ASCII character generator board has no overlay input. It has two enable flags, one to control ASCII characters generated on board (REG16, BIT8) and another to control external pixels (REG16, BIT9, See Appendix E2.2). The REMOTE INHIBIT INPUT is asserted to inhibit ASCII characters. The + and - signs indicate polarities when the respective signals are asserted.

7.4 IMAGE AND GRAPHICS OUTPUT CARDS

The logic and circuit board connections of output cards concerned with customisation are shown as follows:



The + and - signs indicate polarities when the respective signals are asserted.

Memory plane signals and VDU signals may be output at the same time. The external blanking is overidden by the VDU input.

7.5 HIGH - LOW, FLASH AND WATCHDOG BACKPLANE SIGNALS

High and Low are TTL logic levels. High (CM1) = +3.4v, Low (CM2) = 0v, provided for the termination of unused inputs.

The flashing waveform is a two wire differential square wave carried on pins CK1 and CK2. The flash frequency is programmed by links on the CONTROL BOARD (See Para. 7.6) and it is normally used to control an area flash memory plane (See Para. 1.6.5).

The Watchdog is a two wire differential signal carried on pins CL1 and CL2 which is asserted if the interval between successive writing to either of the two addresses containing access flags (Registers No. 9 and No. 13, See Table 4.1) exceeds a predetermined time limit. The time limit is programmed by links on the CONTROL BOARD (See Para. 7.7).

It is normally used to blank the display, in the event of a computer error or failure. The watchdog is reset by writing the same words. Thus the effect of late writing to these addresses will be to cause the display to flicker or flash, and the effect of a complete lack of writing will cause the display to remain blank.

7.6 PROGRAMMING THE FLASH TIMER (SEE DRG. NO. 02-500)

The repetition rate of the flash timer is programmed by means of wire-wrap links on the CONTROL BOARD as follows :

LINK		FLASH CYCLE TIME
'a' to 'f'	-	0.64 secs.
'a' to 'e'	-	1.28 secs.
'a' to 'd'	-	2.56 secs.
'a' to 'c'	-	5.12 secs.

If the flash signal is to operate independantly of the Watchdog LINK pin 'X' to 'Z.

7.7 PROGRAMMING THE WATCHDOG TIME LIMIT (SEE DRG. NO. 02-500)

The Watchdog signal will be asserted if the computer fails to an access flag address before the preset time limit. The rate at which the watchdog timer increments is determined by linking pin 'b' to one of the flash timer output pins 'c' 'd' 'e' or 'f'. The watchdog output pin 'g' is linked to pins 'k' 'j' 'k' or 'l' to establish a time limit of 1, 2, 4 or 8 increments respectively.

In addition to driving the watchdog signal lines CL1 and CL2 the watchdog can inhibit the flashing waveform if pin 'X' is linked to pin 'Y'.

7.8 WIRING NOTES

Customisation wiring involves the interconnection of signal pairs. Consequently it is necessary to ensure that correct signal polarity is maintained. An output pin is normally connected to an input pin of like polarity. The only exception occurs when an enable output is connected to an inhibit or blanking input, or vice versa.

UNUSED INPUTS

Unused inputs are connected, opposite polarity to the HIGH(+) and LOW(-) busses on the backplane, with the exception of the REMOTE INHIBIT inputs on the MEMORY PLANES and HARDWARE CURSOR, which must be connected like polarity.

Unused VIDEO DATA INPUTS on OUTPUT BOARDS may be left unconnected.

7.9 SPECIMEN SIMPLE GRAPHICS SYSTEM

Drg. No. 013-379 is a schematic diagram showing the interconnection of circuit boards for a typical system not utilising an output board. It comprises three memory planes, one for each primary colour (R, G, B), a cursor board and an ascii character generator, which both overlay all three memory planes thus producing a white cursor and white ascii characters.

An area flash memory plane is connected to selectively inhibit the three RGB memory planes. The 75 ohm coaxial outputs of the RGB memory planes are connected directly to the RGB inputs of the monitor.

The pixel output of the Ascii Generator Board is connected to the overlay input of the cursor board, and the output of the cursor board is connected to the overlay input of the RGB memory planes. Thus ascii characters and cursor pixels are mixed on the cursor board before being overlaid on the RGB memory planes. Where a cursor board is used in a cascaded sequence of boards such as this, it is important that the cursor board is nearest the RGB planes in order to achieve the best alignment of cursor pixels with RGB pixels.

The area flash memory board is a standard memory board, written with a pattern that is required to flash on the display. The output of the area flash memory plane is connected to the remote inhibit input of the RGB memory planes, and the flashing cycle time is determined by the backplane flashing waveform which is connected to the remote inhibit input of the area flash memory plane. The output inhibit flag of this plane must be set high for flashing. The overlay input of the area flash plane is driven from the pixel enable flag output of the ascii generator board. Thus both this flag and the flash plane can inhibit the output of the RGB memory planes when the output inhibit flag on the RGB planes is set high.

The pixel enable flag output of the ascii generator board is also connected to the remote inhibit input of the cursor board. Hence when this flag is set low both RGB pixels and cursor pixels are inhibited and only ascii pixels will be seen on the monitor.

Cursor board register No. 4 bit 14 is set high to enable the remote inhibit input and bit 15 of the same register can also inhibit the cursor when set high. The wiring diagram for this system is shown on Drg. No. 013-380.

7.10 SPECIMEN IMAGING SYSTEM

The wiring diagram for a typical monochrome imaging system is shown on Drg. No. 013- 380. All outputs of the memory planes, cursor board, and ascii generator board are connected independantly to inputs on the output board. Remote inhibit inputs and overlay inputs on the memory planes are not used and are wired to the High and Low backplane signals.

The pixel enable output of the ascii generator board is connected to the external blanking inputs of the output board.

APPENDIX A

SUPERVISOR 214 SIGNAL BUS

TABLES

A1 Introduction

The S214 signal bus consists of a number of individual four-card backplanes, some of which have wire-wrap connections, other have printed circuit connections, all with wire-wrap interconnections. Signals are carried on single wire lines terminated in 120 ohms to +3.4v. The lines are terminated in dual in-line resistor packs mounted on a terminator board at the far end of the bus, and must be similarly terminated on the computer interface board(Fig.A4).

Connection is made to the S214 signal bus via a 40 way Berg connector, mounted on the control board. All pins on this connector, are joined directly to the S214 bus, through the control board edge connectors, with the exception of the INT- signal and some 0v pins, all of which connect to the control board only. (See Drg. No. 02-500). Signal lines in the bus are treated as transmission lines, and any connection to the bus should be designed to minimise stubs and mismatches.

A2 Computer Communication

The Supervisor 214 operates as a 'slave' device only, i.e. it cannot initiate a transaction with the computer. Communication commences when the computer puts an S214 register address on the bus, followed by a Read or Write signal. If it is a Write signal data must be stable on the bus before the Write is asserted.

When the Supervisor 214 receives a Read or Write signal from the computer, it always responds with a Reply signal. The computer must maintain the Read or Write signal until it receives the Reply, and the S214 will maintain the Reply until after the Read or Write is removed by the computer. If the operation requested by the computer will be completed within approximately eight microseconds, the S214 sends Reply to the computer when the operation is done, otherwise Reply is sent immediately and the computer must re-access the S214 when the operation is complete.

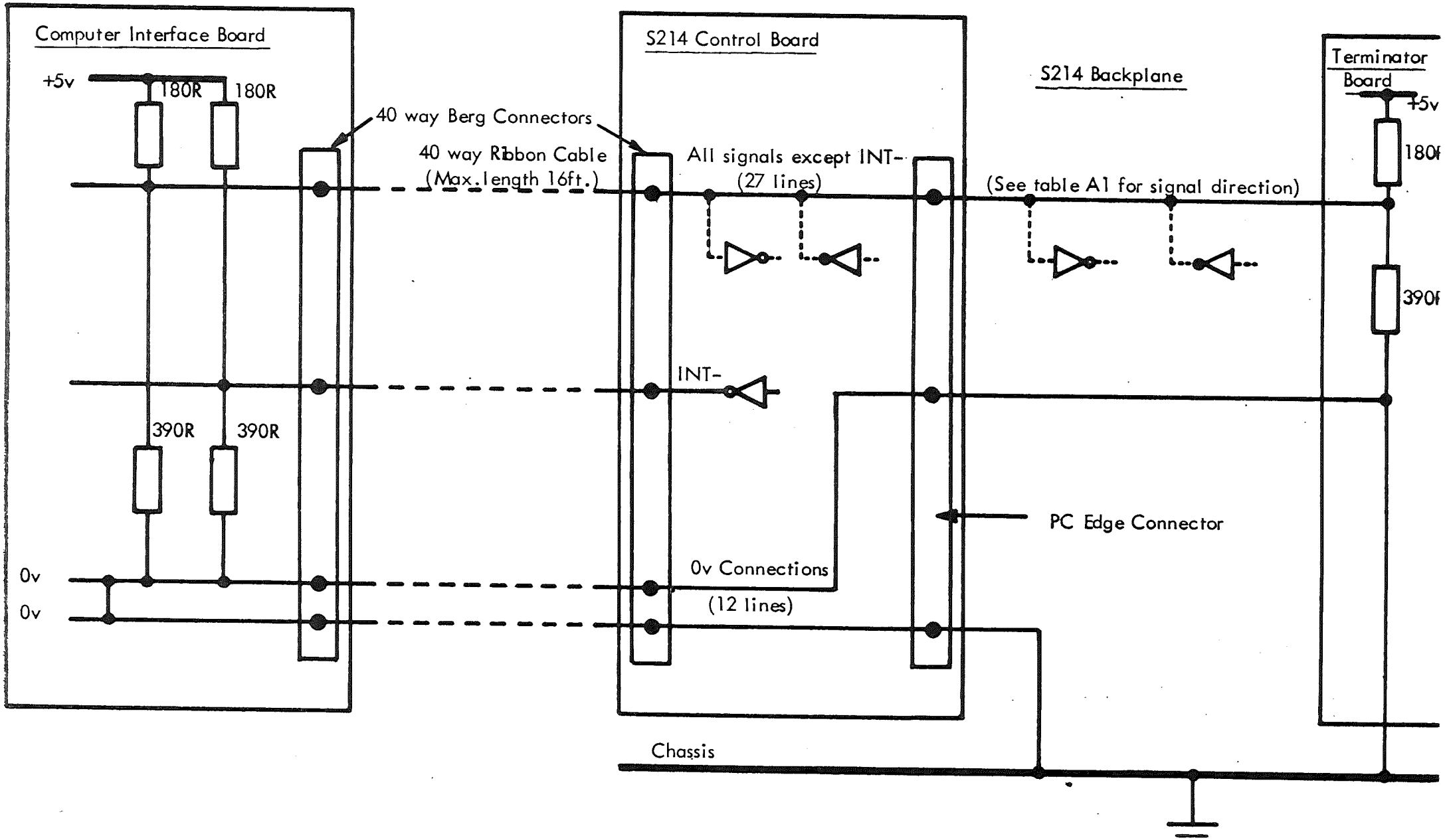
All registers in the S214 except the Data Register send Reply within 8 microseconds, when the operation is done, but the data register may require from 1 uS to 35uS, when operating in one bit mode. (see para. A4.2).

A3 Registers other than the Data Register

Fig. A.1 shows timing waveforms for all registers except the Data Register. Register address must be stable on the bus 100 nS before Read or Write is asserted, and for a Write, data must also be stable on the bus when Write is asserted. For a read, data is put on the bus by the S214 not more than 100 nS after Read. Reply is asserted not later than 2 uS after Read or Write.

S214 BUS SCHEMATIC DIAGRAM

FIG. A4



40 way Berg. Pin No.	Backplane Pin No.	Signal Direction	Signal Ident		
J1/1	AV2	T	INIT-		INITIALISE
J1/2	BE2		0V		
J1/3	*	R	INT-		INTERRUPT
J1/4	BE2		0V		
J1/5	BL1	R	REPLY-		
J1/6	*		0V		
J1/7	BK2	T	WRITE-		
J1/8	BE2		0V		
J1/9	BK1	T	READ-		
J1/10	*		0V		
J1/11	BF1	T	A0-	LSB	REGISTER ADDRESS
J1/12	BF2	T	A1-		
J1/13	*		0V		
J1/14	BH1	T	A2-		
J1/15	BH2	T	A3-		
J1/16	*		0V		
J1/17	BJ1	T	A4-		
J1/18	BJ2	T	A5-	MSB	
J1/19	BB1	T	C0-		REDUNDANT READ
J1/20	AF1	B	H0-	LSB	CONTROL
J1/21	AF2	B	H1-		
J1/22	AH1	B	H2-		
J1/23	AE2		0V		
J1/24	AH2	B	H3-		
J1/25	AJ1	B	H4-		
J1/26	AJ2	B	H5-		
J1/27	AL1		0V		
J1/28	AK1	B	H6-		
J1/29	AK2	B	H7-		
J1/30	AR1	B	H8-		DATA HIGHWAY
J1/31	AP2		0V		
J1/32	AR2	B	H9-		
J1/33	AS1	B	H10 -		
J1/34	AS2	B	H11 -		
J1/35	AT1		0V		
J1/36	AT2	B	H12 -		
J1/37	AU1	B	H13 -		
J1/38	AU2	B	H14 -		
J1/39	AT1		0V		
J1/40	AV1	B	H15 -	MSB	

* Indicates no backplane connection. These lines terminate on the CONTROL BOARD.
T = Transmit from computer
R = Receive at computer
B = Bidirectional

BUS LOGIC LEVEL CONVENTION

0V = Signal asserted +3.4V = Signal unasserted

TABLE 2

Bus Receiver Gate Specification

Bus receivers are signetics type 8T37 or 8T38 or equivalent.

	MIN.	MAX.	
Input High Threshold Voltage	1.8	2.5	V
Input Low Threshold Voltage	1.05	1.55	V
Input High Current		100	uA
Input Low Current		-0.05	mA

TABLE 3

Bus Driver Gate Specification

Bus drivers are signetics type 8T38 or equivalent.

	MIN.	MAX.	
Output Low Voltage (O/P current = 50 mA)		0.5	V
Output High Voltage (O/P current=-5.2 mA)	2.4		V
Output High Current		100	uA
Output Short Circuit Current		-55	mA

A4 The Data Register

The Data Register differs from all other registers in the S214 because it is normally involved in serial transactions, either by bit or byte, with the S214 memory planes, under the control of the I/O cycle counter. Hence, the longer time interval between Read or Write and Reply. There are two ways in which the Data Register responds to Read or Write, namely Late Reply, and Immediate Reply.

A4.1 Late Reply

This mode is similar to all other registers in the S214, in that Reply is sent to the computer when the operation is completed. The data register operates in this mode when the I/O cycle is less than five, and the time delay between Read or Write and Reply is not more than 8 uS.

N.B. The I/O cycle counter is loaded with a number one less than the required number of cycles.

A4.2 Immediate Reply

If the I/O cycle count is greater than four, then more than 8 uS may elapse before the operation is complete, so in this case, Reply is sent to the computer immediately a Read or Write is asserted, which permits the computer to access other registers in the S214 during the Data Register operation. The computer must not access the data register again until the operation is complete, which may be determined by the Data Ready Flag in the Control and Status Register.

I/O CYCLE COUNTS GREATER THAN FOUR ARE VALID IN ONE-BIT MODE ONLY, BECAUSE ALL OTHER MODES UTILISE THE DATA HIGHWAY DURING THE DATA REGISTER OPERATION, AND CONSEQUENTLY IT IS NOT AVAILABLE TO THE COMPUTER.

Figs. A2 and A3 show the Read and Write timing waveforms for the data register. The register address must be stable at least 100 nS before the Read or Write pulse, and Reply will be asserted either approximately 100 nano-seconds after Read or Write, or after several micro-seconds, depending upon the magnitude of the I/O cycle count. Data Ready is asserted when the I/O cycle count is exhausted, indicating that a Read or Write sequence is completed. After a Read sequence the data ready signal may be asserted up to 50 nS before data is stable on the bus.

A4.3 Co Redundant Read Control

When the Reply is immediate (1 bit mode, I/O cycle count $>$ 4), an instruction which caused a read-write cycle to the Data Register, would fail, because the S214 would immediately Reply to the Read, which would then cause the computer to assert a Write while the Read sequence was in operation. Also, in the auto increment mode, the X and Y registers would receive a double increment.

However, if the Co signal is asserted during the Read time of the Read-Write cycle, the Read sequence is inhibited, a Reply is issued in response to the Read, and only the Write sequence is effected.

Co must be asserted at least 100 nS before the Read and must be negated after the Read, but 100 nS before the Write of the Read-Write cycle. This facility is provided for older PDP11 computers which do a read and write for the last cycle of a MOV instruction.

A5 Initialise

An initialise signal is required at power-up. It clears various registers, counters and bistables in the S214. If a programmable format board is fitted, it presets the resolution of the display to 384 pixels by 293 lines.

A6 Interrupt

The S214 can assert Interrupt at the end of every display field. It is enabled by the Erase or Field Interrupt enable bits in the Control and Status Register.

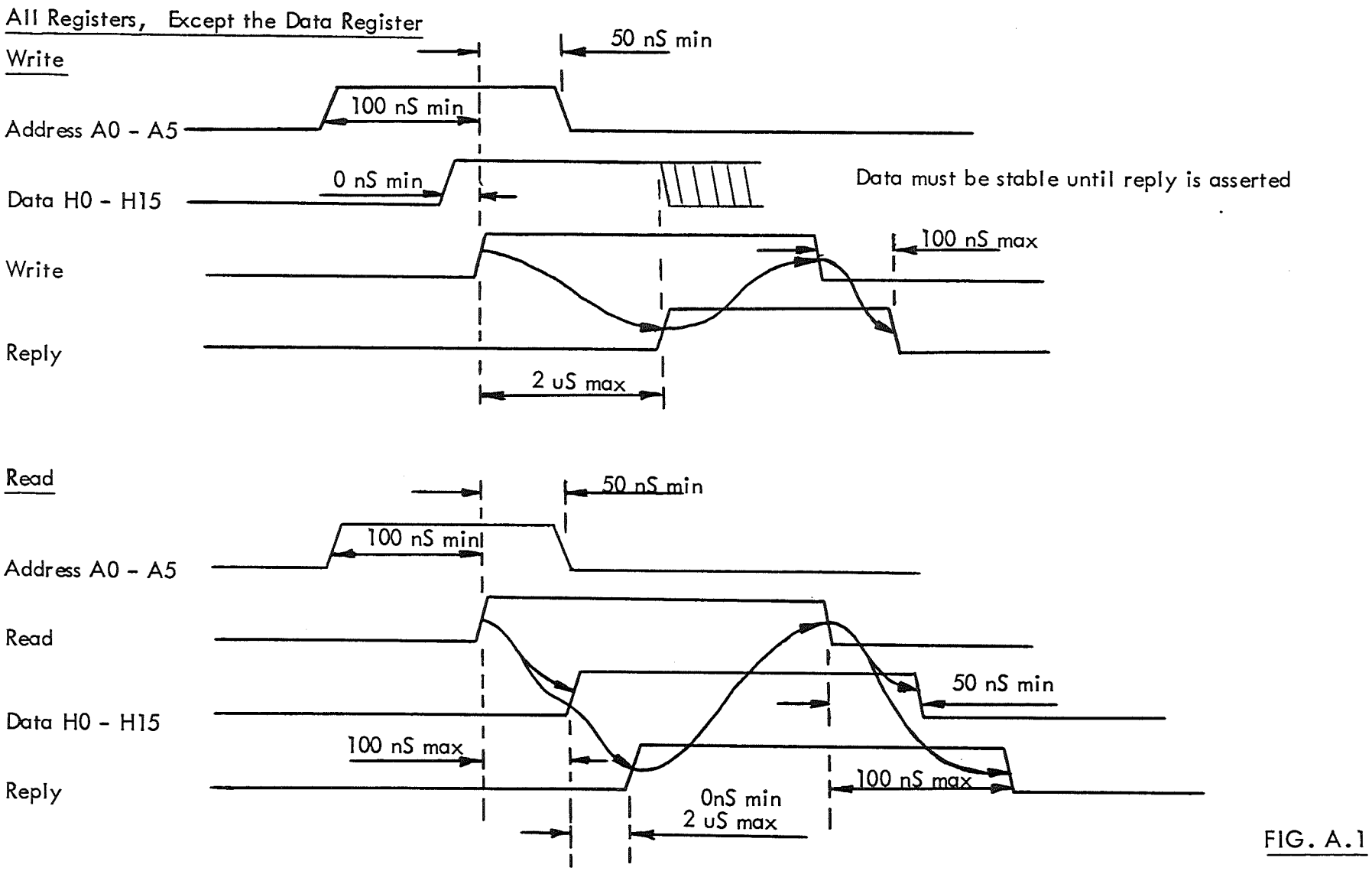

All Registers, Except the Data Register
Write
50 nS min
100 nS min
Address A0 - A5
0 nS min
Data H0 - H15
Data must be stable until reply is asserted
100 nS max
Write
Reply
2 uS max
Read
50 nS min
100 nS min
Address A0 - A5
Read
50 nS min
Data H0 - H15
100 nS max
100 nS max
Reply
0nS min
2 uS max

FIG. A.1

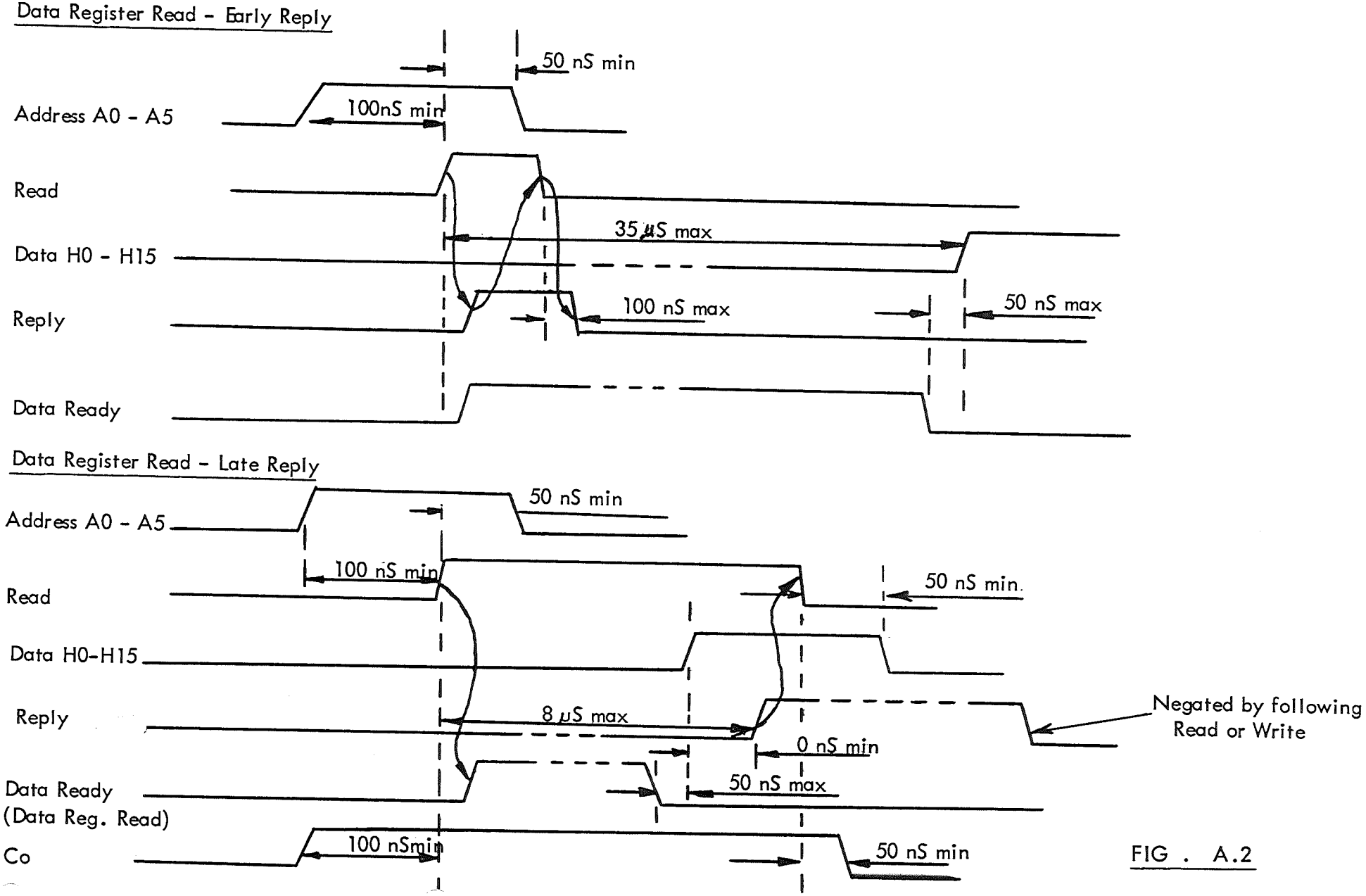
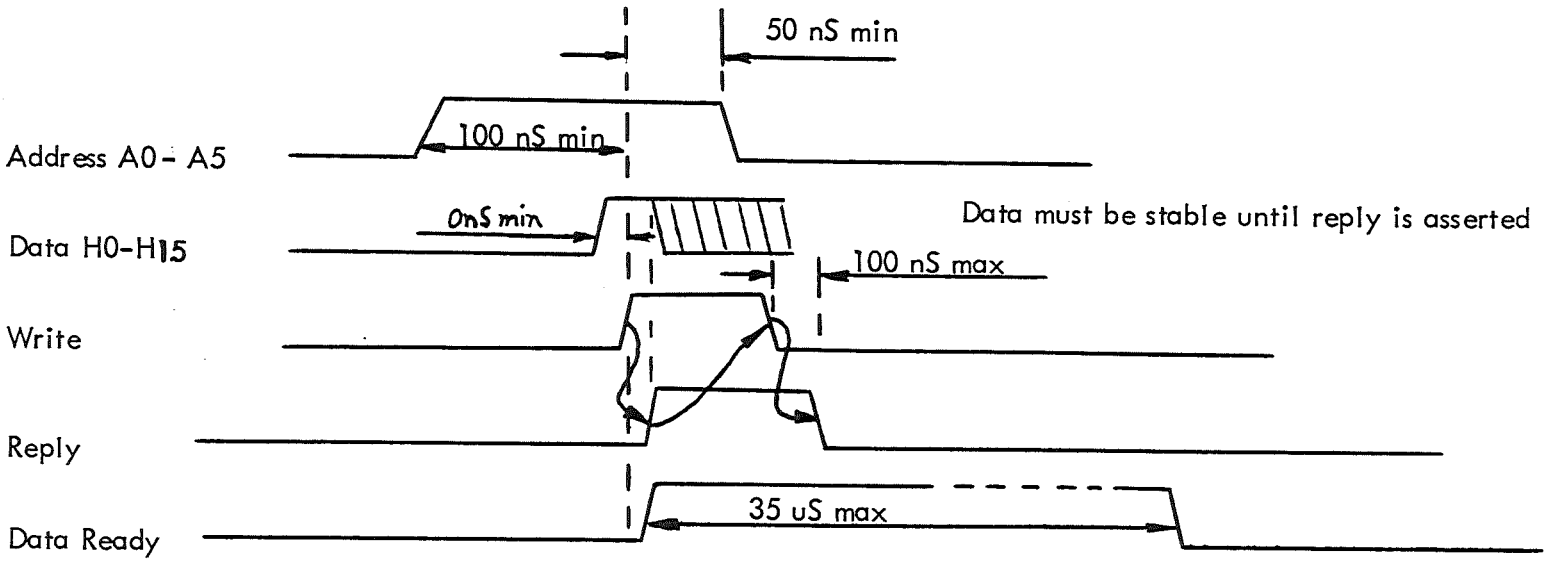

Data Register Read - Early Reply
50 nS min
Address A0 - A5
100nS min
Read
35 µS max
Data H0 - H15
Reply
100 nS max
50 nS max
Data Ready
Data Register Read - Late Reply
Address A0 - A5
50 nS min
100 nS min
Read
50 nS min.
Data H0-H15
Reply
8 µS max
Negated by following Read or Write
0 nS min
Data Ready
(Data Reg. Read)
50 nS max
Co
100 nSmin
50 nS min

FIG . A.2

Data Register Write-Early Reply



Data Register Write - Late Reply

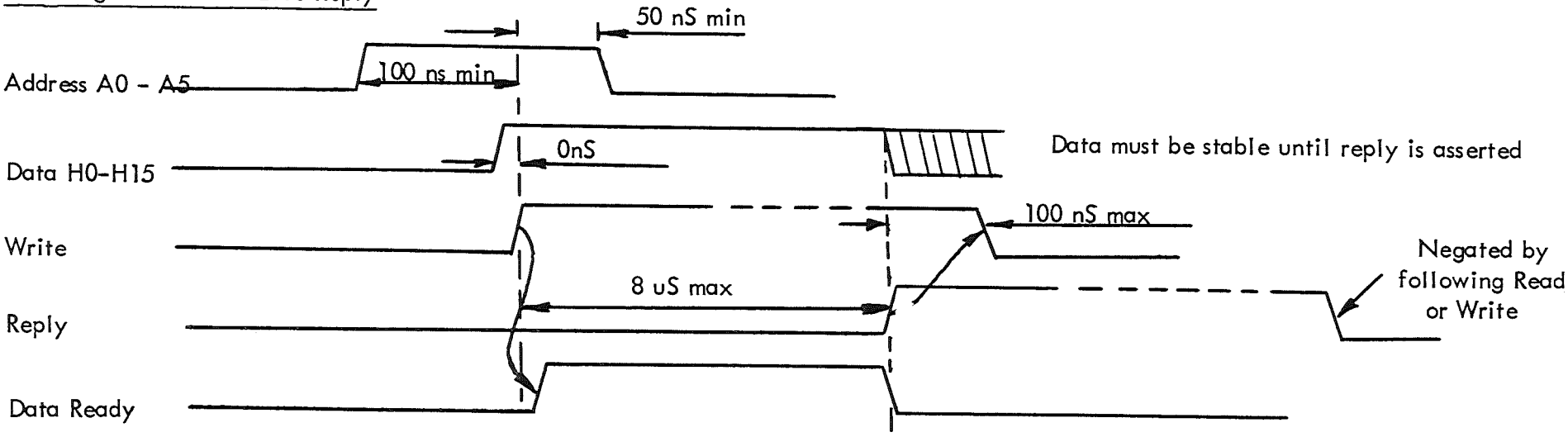


FIG. A.3

APPENDIX B

PDP11/S214 INTERFACE

TABLES

APPENDIX B PDP11/S214 INTERFACE

The PDP-11 Unibus address, control and data signals are transmitted via bus transceivers with open collector drivers.

The Supervisor 214 is allocated priority level 4, and therefore interrupt bus request lines BR7 - BR5 are not connected, and the associated bus grant lines are looped through via links on 7a.

The address, control and data information is output to the Supervisor 214 Control PCB via further transceivers with open collector drivers. The signals are terminated in resistor networks to ensure a matched transmission line in the Supervisor 214.

The 16 data lines, D0 - D15, are formatted in two bytes. The low order byte contains bits D0 - D7, and the high order byte bits D8 - D15. Of the 18 address lines, bits A1 - A6 specify the mode of operation, and A7 - A17 the location.

The interface arrangements allow for DAT0 and DAT1 data transactions to be carried out, initiated from the PDP-11 CPU. The type of transaction is identified by control signal C1 which is set low for a DATIO (write) sequence, high for a DATI (read) sequence. The Supervisor 214 may request bus control via the interrupt signal.

The circuit arrangements for the PDP-11 Interface PCB are shown on Drg. 02-505. The Interface PCB is mounted in the PDP-11 computer and connects to the Supervisor 214 Control PCB via a cable ribbon. The computer signals and connections are shown on Table B.1.

The initialise signal, INITL, is generated at power up and resets the bus request flip-flops. It is output to the Supervisor 214 as the INIT- signal.

B.1 Supervisor 214 Addresses

The Supervisor 214 is controlled by reference to a set of sixty four 16 bit registers which appear in the input/output page of the PDP-11 address space.

The register page address for the Supervisor 214 is set by the links (R7 - R14) on 6c which provide the A inputs to comparators 10b, 12b, 11b. With the link open, the input is set high, closed it is set low. The B inputs are derived from address bits A7L - A17L. The data register, as well as appearing at a single address in the PDP-11 input/output page, also appears as a block of addresses. The start of this block may be set anywhere in the PDP-11 address space on 512 word boundaries, and may be adjusted in steps of 512 words up to 4096 words. The required word block (page size) and start address are set up by switches D10-D17 and W10 - W12 on 9c as shown on Table B.2. Switches D10 - D17 provide the B inputs to comparators 8b, 9b, and set the appropriate inputs high if they are open, low if they are closed. The A inputs are derived from data highway bits A10L - A17L, the most significant bits of which are switched in from the data lines (switches W10 - W12 closed) or tied to +5V (1).

B.2 Write Sequence

The write sequence is a DATIO data transaction in which the PDP-11 writes data into the registers or memory planes of the Supervisor 214.

The PDP-11 initiates the sequence by asserting MSYNL and CIL, and by setting the register page address for the Supervisor 214 on address lines A7L - A17L, and the individual address lines A1L - A6L. The page address is recognised by comparators 11b, 12b, 10b and 10b pin 6 is set high. It is gated with the inverted MSYNL signal to set 7c pin 3 low. This enables the register address bits through transceivers 6a, 14b, and they are output to the Control PCB as signals A0 - A5.

The high output on 10b pin 6 sets 7c pin 6 high. This is gated with the inverted MSYNL and CIL signals and sets 7b pin 12 low. This signal is used to generate the WRITE- signal via transceiver 5c pin 4, and to enable transceivers 1b, 2b, 3b, 4b to allow data to be transmitted from Unibus lines D0L - D15L to Supervisor 214 bus lines H0 - H15.

The Supervisor 214 acknowledges receipt of the data with a REPLY- signal. It is gated through to 13a pin 14 and output as Unibus signal SSYNL. The PDP-11 CPU responds by negating signal MSYNL which in turn negates the WRITE- signal. The Supervisor 214 then drops the REPLY- signal which terminates the sequence by negating the SSYNL signal.

B.3 Read Sequence

The read sequence is a DATI data transaction in which the PDP-11 reads data from the Supervisor 214 registers or memory planes.

The sequence is similar to the write sequence except that signal CIL is set high. It is gated with the inverted MSYNL signal and the high output from 7c pin 6 to set 7b pin 6 low. This causes the READ- signal to be generated via transceiver 5c pin 1, and enables transceivers 1a, 2a, 3a, 4a to allow data to be transmitted from the Supervisor 214 bus (H0 - H15) to the PDP-11 Unibus (D0L - D15L). The Supervisor 214 acknowledges availability of data with the REPLY- signal, and the handshake continues as for a write sequence.

B.4 Interrupt Sequence

The Supervisor 214 can interrupt the PDP-11 CPU only if it has gained bus control by asserting signal BR4L.

It initiates an interrupt sequence by setting INT-. This clocks request flip-flop 14c and sets pin 5 high so that BR4L is asserted on the Unibus.

When the request is implemented (in accordance with priority), the PDP-11 CPU asserts the bus grant signal BG4INH. The clocks grant flip-flop 14c so that 11c pins 4 and 5 are enabled, and the request flip-flop 14c is cleared to negate signal BR4L. Pins 1 and 2 on 11c are also enabled because Unibus signals SSYNL and BBSYL are not asserted, and therefore 11c pin 6 is set low. This presets the interrupt flip-flop so that the interrupt request and bus busy signals, INTRL and BBSYL, are asserted on the Unibus. The low output on 12c pin 6 resets the grant flip-flop and enables the interrupt vector on to Unibus D2L - D8L. The CPU acknowledges acceptance of the interrupt vector by asserting SSYNL so that signals INTRL and BBSYL are negated. The CPU re-assumes control of the Unibus and enters the interrupt handling sequence.

TABLE B.1 PDP-11 INTERFACE SIGNALS

Control Signals

DD2	BR7L	Not used
DE2	BR6L	Not used
DF2	BR5L	Not used
DH2	BR4L	Bus request
DK2	BG7INH	Not used
DL1	INITL	Initialise signal
DL2	BG7OUTH	Not used
DM2	BG6INH	Not used
DN2	BG6OUTH	Not used
DP2	BG5INH	Not used
DR2	BG5OUTH	Not used
DS2	BG4INH	Bus grant input
DT2	BG4OUTH	Bus grant output
EE1	MSYNL	Master synchronise signal
EF2	CIL	Data transaction control
EJ1	SSYNL	Slave synchronise signal
FD1	BBSYL	Bus busy
FM1	INTRL	Interrupt

Data Lines

CS2	D0L	CL2	D8L
DR2	D1L	CK2	D9L
CU2	D2L	CJ2	D10L
CT2	D3L	CH1	D11L
CN2	D4L	CH2	D12L
CP2	D5L	CF2	D13L
CV2	D6L	CE2	D14L
CM2	D7L	CD2	D15L

Address Lines

EH2	A0L	ER1	A9L
EH1	A1L	EP1	A10L
EF1	A2L	EL1	A11L
EV2	A3L	EC1	A12L
EU2	A4L	EK2	A13L
EV1	A5L	EK1	A14L
EU1	A6L	ED2	A15L
EP2	A7L	EE2	A16L
EN2	A8L	ED1	A17L

TABLE B.2 LINK ARRANGEMENTS

Data Register Addresses

1 = link open 0 = link closed

DATA PAGE	D12	DR12	D11	DR11	D10	DR10	SET START ADDRESS LINK
4096 words	1	1	1	1	1	1	D17 - D13
2048 words		0	1	1	1	1	D17 - D12
1024 words		0		0	1	1	D17 - D11
512 words		0		0		0	D17 - D10
0 words	0	1	0	1	0	1	Data Page Disable

Vector Addresses

	Circuit Ref.	Ident.	Standard Factory Setting	
Switch	5a/7	V8	0	
	5a/6	V7	1	
	5a/5	V6	1	0 = link open
	5a/4	V5	0	1 = link closed
	5a/3	V4	0	
	5a/2	V3	0	FactorySetting = 300
	5a/1	V2	0	

Register Page Address

Link	6c/11	R12	1	
	6c/12	R11	0	
	6c/13	R10	0	0 = link closed
	6c/14	R9	0	1 = link open
	6c/15	R8	0	
	6c/16	R7	0	Factory Setting = 770000

Lowest Data Page Address

Link	9c/8	D17	1	
	9c/7	D16	1	
	9c/6	D15	1	0 = link closed
	9c/5	D14	1	1 = link open
	9c/4	D13	1	
	9c/3	D12	0	Factory Setting
	9c/2	D11	0	= 762000
	9c/1	D10	1	

Data Page Size

Link	9c/14	DR12	1	0 = link closed
	9c/15	DR11	1	1 = link open
	9c/16	DR10	1	Factory Setting = Data Page Disabled