Wildcat Board 1/Prototype Design

*** IMPORTANT NOTICE ***

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Information described within is subject to change without notice.

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DIGITAL INTERNAL USE ONLY

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REVISIONS

CHK	CHANGE NO.	REV

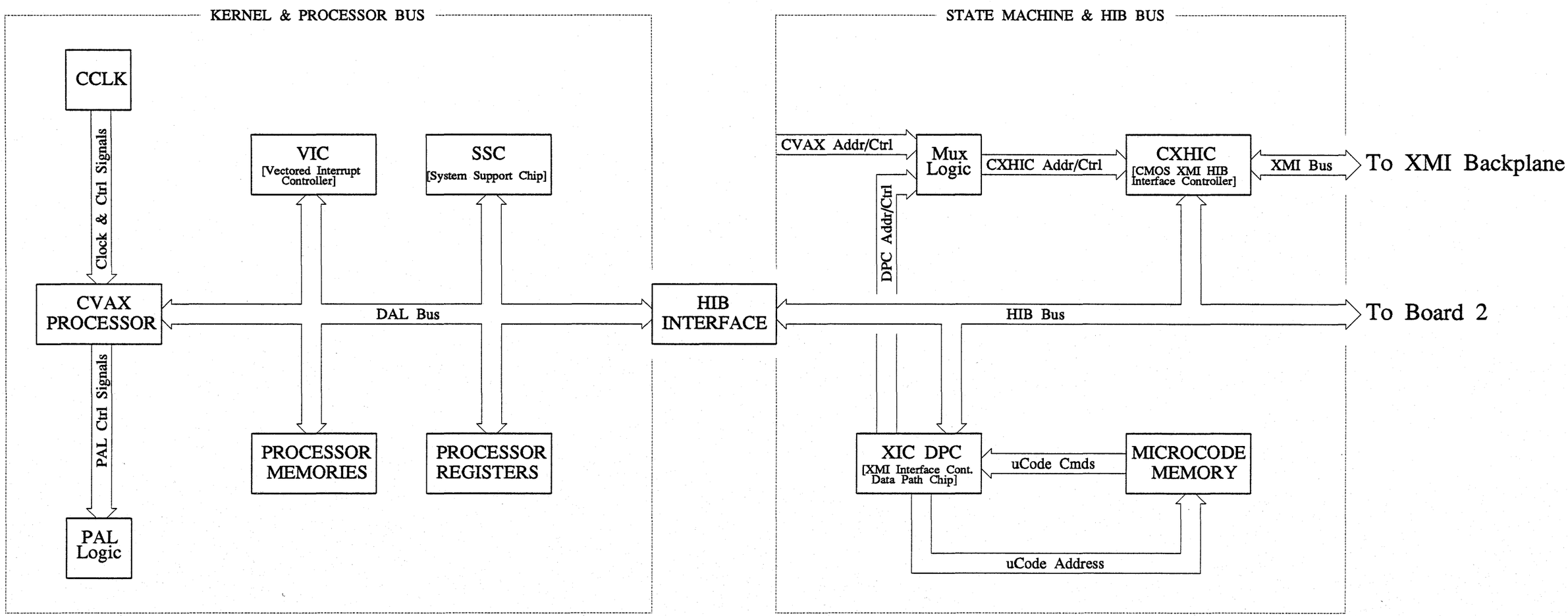
digital

LOGIC_NAME = LOGIC SHEET NAME — Thu Oct 20 17:21:42 1988
FIRST USED ON OPTION/MODEL: NUMBER

DRN: Taskmaster	DATE 10/20/88	ENG: D. Versace	DATE 10/20/88
CHK'D: K. Yesse	DATE 10/20/88	BOARD LOCATION: CXO	
		SHEET 1 OF Many	
		NEXT HIGHER ASSEMBLY: NAME	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	T2022	A1_12



WILDCAT BOARD 1: Basic Elements of KERNEL And STATE MACHINE

Local Drawing Library

REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]
Basic Board 1
Top-Level Block Diagram

digital

Thu Oct 20 16:45:20 1988

FIRST USED ON OPTION/MODEL: -

DRN: K. Yesse	-	DATE	ENG: D. Versace	-	DATE
CHK'D: -		DATE -	BOARD LOCATION: CXO		
			SHEET 2		
			NEXT HIGHER ASSEMBLY: -		

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

Manual/Powerup Reset

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Terminal

Ethernet

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HIB Address Parity

DATA CTRL LOGIC p.11

KERNEL BLOCK DIAGRAM

XISM (XI State Machine) BLOCK DIAGRAM

Local Drawing Library

REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]

Kernel & XI State Machine Block Diagrams

digital

Thu Oct 20 17:04:34 1988

FIRST USED ON OPTION/MODEL: -

DRN: K. Yesse	DATE -	ENG: D. Versace	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
		SHEET 3	
		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

Local Drawing Library

REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]

Detailed Kernel Diagram (TBD)

digital

- Thu Oct 20 17:05:42 1988

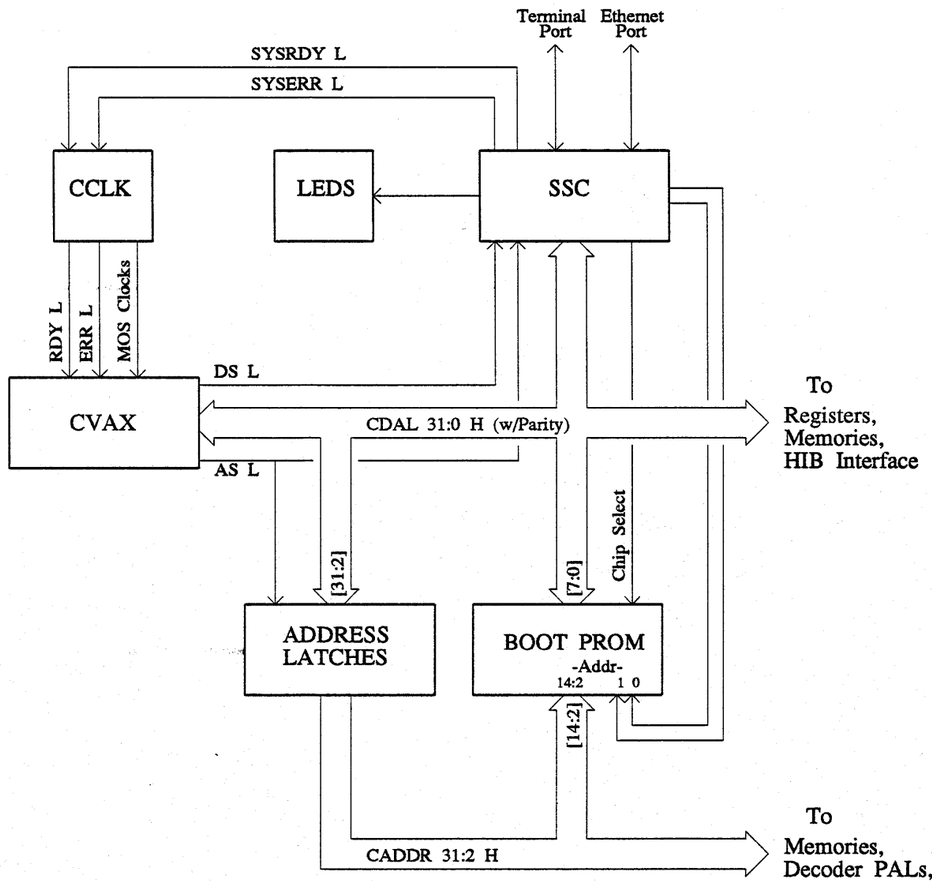
FIRST USED ON OPTION/MODEL: -

DRN: K. Yesse	-	DATE	ENG: D. Versace	-	DATE
CHK'D: -	-	DATE	BOARD LOCATION: CXO		
			SHEET 4		
			NEXT HIGHER ASSEMBLY: -		

TITLE: WILDCAT BOARD 1

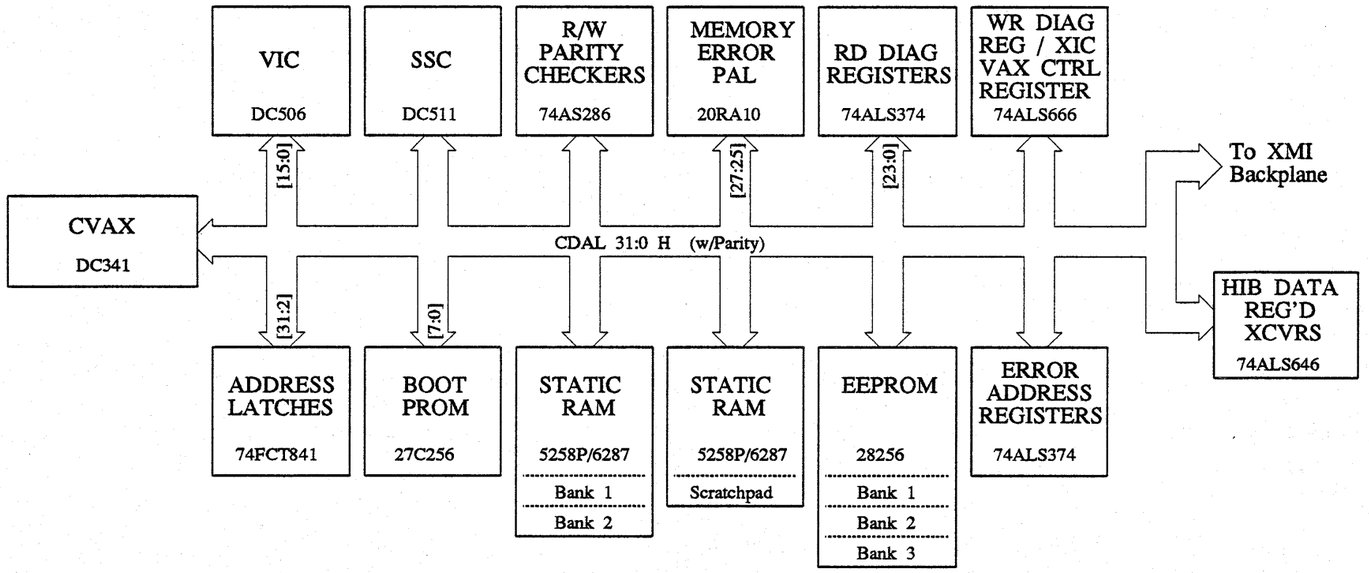
SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

SIZE	CODE	NUMBER	REV
K	CS	-	-



BOOT LOGIC

This diagram shows the minimum logic required to boot the CVAX processor.



DAL BUS DETAIL

Local Drawing Library

REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]
Boot Logic &
DAL Bus Detail Diagrams

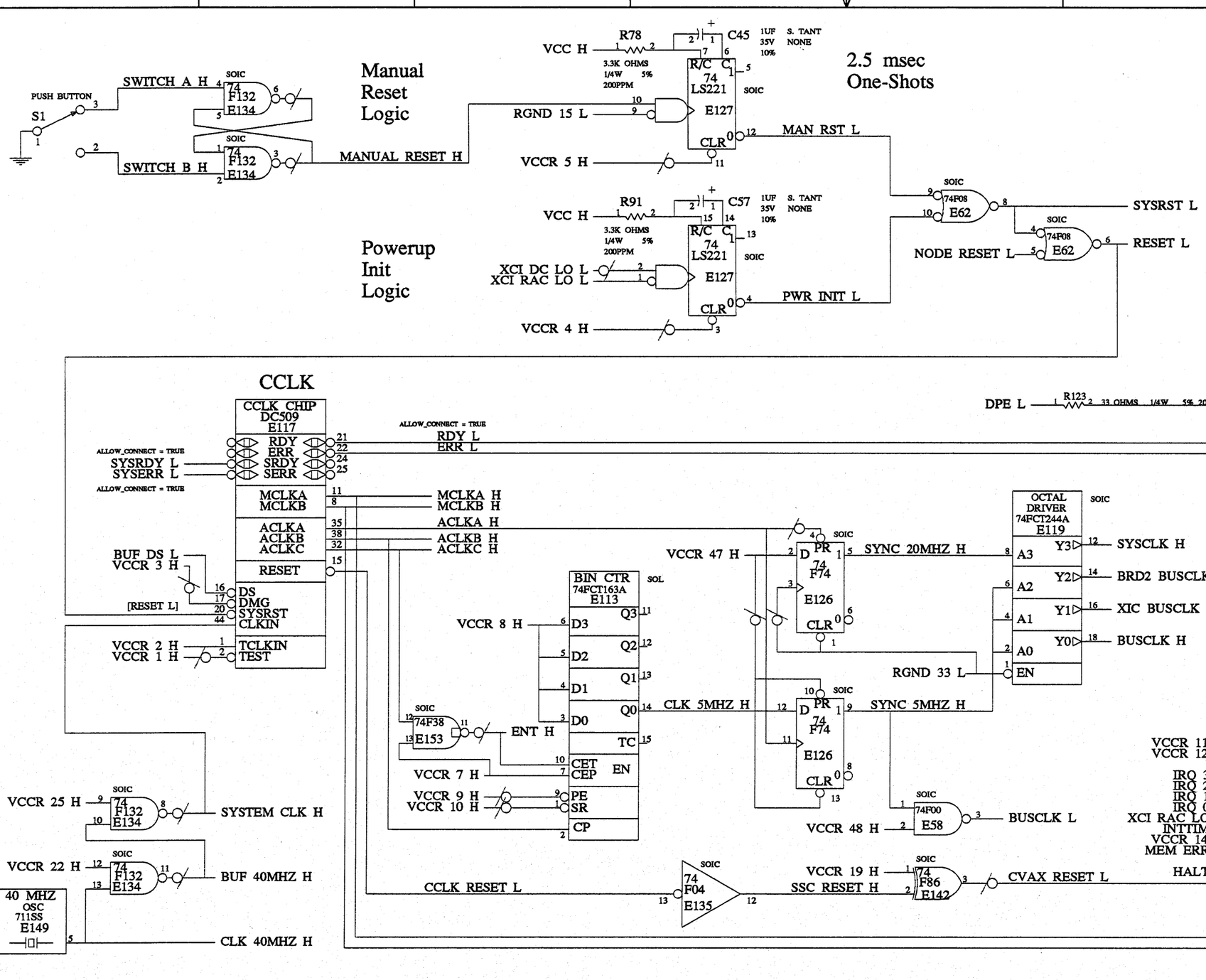
digital

Thu Oct 20 17:06:32 1988

DRN: K. Yesse	-	DATE	ENG: D. Versace	-	DATE
CHK'D: -		DATE	BOARD LOCATION: CXO		
			SHEET 5		
FIRST USED ON OPTION/MODEL: -			NEXT HIGHER ASSEMBLY: -		

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88



CVAX

CVAX CPU DC341 E91

90NS-13

NOTE: Series resistors should be placed as close to CVAX chip as possible.

DAL			CDAL
31	84	R184	CDAL 31 H
30	83	R183	CDAL 30 H
29	82	R182	CDAL 29 H
28	81	R181	CDAL 28 H
27	80	R180	CDAL 27 H
26	79	R186	CDAL 26 H
25	78	R194	CDAL 25 H
24	74	R175	CDAL 24 H
23	73	R192	CDAL 23 H
22	72	R188	CDAL 22 H
21	71	R173	CDAL 21 H
20	70	R170	CDAL 20 H
19	69	R165	CDAL 19 H
18	68	R185	CDAL 18 H
17	67	R174	CDAL 17 H
16	66	R172	CDAL 16 H
15	65	R157	CDAL 15 H
14	64	R169	CDAL 14 H
13	63	R161	CDAL 13 H
12	62	R155	CDAL 12 H
11	61	R153	CDAL 11 H
10	60	R147	CDAL 10 H
9	59	R151	CDAL 09 H
8	58	R140	CDAL 08 H
7	57	R133	CDAL 07 H
6	56	R131	CDAL 06 H
5	55	R121	CDAL 05 H
4	54	R119	CDAL 04 H
3	50	R138	CDAL 03 H
2	49	R141	CDAL 02 H
1	48	R142	CDAL 01 H
0	47	R143	CDAL 00 H

CP			CSDP
DAT5	3		
DAT4	4		
DAT3	5		
DAT2	6		
DAT1	7		
DAT0	8		
STA1	9		
STA0	10		
DPE	38		
CSDP3	39	R122	CSDP 3 H
CSDP2	40	R146	CSDP 2 H
CSDP1	41	R145	CSDP 1 H
CSDP0	42	R144	CSDP 0 H

AS	30	R148	AS L
DS	29	R154	DS L
WR	32	R132	WR L
DBE	31	R139	DBE L
BM3	43		BM 3 L
BM2	44		BM 2 L
BM1	45		BM 1 L
BM0	46		BM 0 L

All R: 33 OHMS 1/4W 5% 200PPM

RDY0	27
ERR	28
DMC	25
DMR	26
CCTL	24
IRQ3	14
IRQ2	13
IRQ1	12
IRQ0	11
PWRFL	18
IN'TTIM	15
CRD	16
MEMERR	17
HALT	19
RESET	35
CWE	23
TST	20
CLKA	34
CLKB	33

REVISIONS		
CHK	CHANGE NO.	REV

[Kernel]

CVAX, CCLK, CLOCK & RESET LOGIC

digital

DRN: K. Yesse	DATE -	ENG: T. Kinlaw	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
		SHEET 6	
- Thu Oct 20 17:11:49 1988		NEXT HIGHER ASSEMBLY: -	
FIRST USED ON OPTION/MODEL: -			

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

SSC

VIC

'ASSERTION POLARITY OF PIRQ SIGNALS ARE PROGRAMMABLE'
'ASSERTION SHOWN IS APPLICATION SPECIFIC'

uVAX VIC-II DC506 E63 — CIRQUAD

15	9	
14	8	
13	7	
12	6	
11	5	
10	4	
9	3	
8	2	
7	1	
6	68	
5	67	
4	66	
3	65	
2	64	
1	63	
0	62	

DIAG PIRQ L	28	PIRQ15
VCCR 30 H	27	PIRQ14
	26	PIRQ13
	25	PIRQ12
	24	PIRQ11
	23	PIRQ10
	22	PIRQ9
	21	PIRQ8
	20	PIRQ7
MASK ACT REG L	19	PIRQ6
HIB BUS ERR L	18	PIRQ5
SIB INTRPT L	17	PIRQ4
SIA INTRPT L	16	PIRQ3
XISM INTR L	15	PIRQ2
XBE ERR SUM L	14	PIRQ1
MASK ERR SUM L	13	PIRQ0
	50	RDY — SYSRDY L
BUF AS L	47	AS
BUF DS L	41	DS
REG WR L	40	WR
	56	IAKEOP
	57	IAKEON — SYSERR L
LET VIC IACK L	42	IAKEI
	55	IACK
	51	IRQ3
	52	IRQ2 — IRQ 2 L
	53	IRQ1 — IRQ 1 L
	54	IRQ0 — IRQ 0 L
REG CS 2 H	43	CS2
REG CS 1 H	45	CS1
REG CS 0 H	46	CS0
VIC RESET L	31	RESET
VIC CS L	39	CSEL
	61	XVEC
ACLKA H	30	CLK

∧ Notes, not
∨ signal names

uVAX SSC DC511 E92 — CIRQUAD

DAL31	4	CDAL 31 H
DAL30	5	CDAL 30 H
DAL29	6	CDAL 29 H
DAL28	7	CDAL 28 H
DAL27	8	CDAL 27 H
DAL26	9	CDAL 26 H
DAL25	10	CDAL 25 H
DAL24	13	CDAL 24 H
DAL23	14	CDAL 23 H
DAL22	15	CDAL 22 H
DAL21	16	CDAL 21 H
DAL20	17	CDAL 20 H
DAL19	18	CDAL 19 H
DAL18	19	CDAL 18 H
DAL17	20	CDAL 17 H
DAL16	21	CDAL 16 H
DAL15	22	CDAL 15 H
DAL14	23	CDAL 14 H
DAL13	24	CDAL 13 H
DAL12	25	CDAL 12 H
DAL11	26	CDAL 11 H
DAL10	27	CDAL 10 H
DAL09	28	CDAL 09 H
DAL08	29	CDAL 08 H
DAL07	30	
DAL06	31	
DAL05	34	
DAL04	35	
DAL03	36	
DAL02	37	
DAL01	38	
DAL00	39	

REG BM 3 L	54	BM3
REG BM 2 L	55	BM2
REG BM 1 L	56	BM1
REG BM 0 L	57	BM0
AS L	1	AS
DS L	84	DS
WR L	79	WR
	68	IRQ — IRQ 3 L
	80	EPS
	67	IAKEO — LET VIC IACK L
CSDP 2 H	81	CS2
CSDP 1 H	82	CS1
CSDP 0 H	83	CS0
	78	RDY — SYSRDY L
	77	ERR — SYSERR L
	65	INTCLKO — INTTIM L
	66	IORESET
	71	ROMAD1 — SSC ADDR 1 H
	70	AD0 — SSC ADDR 0 H
RGND 9 L	52	WID1
VCCR 15 H	53	WID0
	72	EN — BOOT ROM CS L
TD IN H	44	DI CT
	43	DO — TERM DATA OUT H
ED IN H	46	DI CS
	45	DO — ETHER DATA OUT H
VCCR 16 H	59	HALTI
	60	HALTO — SSC HLT L
VCCR 17 H	40	SECCON
	58	RUN
	62	ADS1 — ANAL TRIG L
	61	ADS0 — ERR ADDR CS L
	50	OPT3
	49	OPT2
	48	OPT1
	47	OPT0
SSC BLO L	51	BLO
SYSTEM CLK H	73	TB40
RGND 2 L	69	TB25
	74	CLKI
SSC RESET H	76	RESET
VCC H	3	VDDI
	41	VDDI

NOTES ON BOOT PROM:

Prototype uses DIP PROM (27C256) socketed using mark eyelets (Qty 28, p/n 12-23208-03).

FRS design uses PLCC PROM (27C256SL) permanently fastened to board.

Boot PROM

32K X 8 CMOS ROM 27C256 E158 — *IDEFAULT
250NS
000E6

O7	19	CDAL 07 H
O6	18	CDAL 06 H
O5	17	CDAL 05 H
O4	16	CDAL 04 H
O3	15	CDAL 03 H
O2	13	CDAL 02 H
O1	12	CDAL 01 H
O0	11	CDAL 00 H

CADDR 14 H	27	A14
CADDR 13 H	26	A13
CADDR 12 H	2	A12
CADDR 11 H	23	A11
CADDR 10 H	21	A10
CADDR 09 H	24	A09
CADDR 08 H	25	A08
CADDR 07 H	3	A07
CADDR 06 H	4	A06
CADDR 05 H	5	A05
CADDR 04 H	6	A04
CADDR 03 H	7	A03
CADDR 02 H	8	A02
	9	A01
	10	A00
	20	CE
PROM READ L	22	OE
VCC H	1	VPP

OCTAL DRIVER 74F240 E120 — SOIC

	2	D3
SSC OPT 3 L		Y3 — 18 — SSC LED 3 L — 7
	4	D2
SSC OPT 2 L		Y2 — 16 — SSC LED 2 L — 5
SSC OPT 1 L	6	D1
		Y1 — 14 — SSC LED 1 L — 3
SSC OPT 0 L	8	D0
		Y0 — 12 — SSC LED 0 L — 1
RGND 10 L	1	EN

LEDx4 PAK 555 4003 E88 — SOIC RED .008A .6MCD

7	8
5	6
3	4
1	2

VCC H

74 F04 E135 — SOIC: HLT H (11 → 10)
74F38 E153 — SOIC: HALT L (1, 2 → 3)

LINE DRIVER 9636 E139

	2	7 — TD OUT L
VCCR 18 H	3	6 — TERM DTR L
	1	WS
PWR 12V H	8	+12
PWR NEG 12V H	5	-12

R67 24K OHMS 1/4W 5% 200PPM (1, 2)
TERM SIG GND L
R75 220 OHMS 1/4W 5% 200PPM (1, 2)
TERM RCV DATA L
R69 220 OHMS 1/4W 5% 200PPM (1, 2)

Terminal Serial Port

R70 4.7K OHMS 1/4W 5% 200PPM (1, 2)
C46 56PF 50V 5% 1206 NPO (1, 2)
R73 24K OHMS 1/4W 5% 200PPM (1, 2)

9639 E140: 8 — 2 — TD IN H; 7

LINE DRIVER 9636 E141

	2	7 — ED OUT L
	3	6 — ETHER DTR L
	1	WS
	8	+12
	5	-12

R58 24K OHMS 1/4W 5% 200PPM (1, 2)
ETHER SIG GND L
R74 220 OHMS 1/4W 5% 200PPM (1, 2)
ETHER RCV DATA L
R63 220 OHMS 1/4W 5% 200PPM (1, 2)

Ethernet Serial Port

R68 4.7K OHMS 1/4W 5% 200PPM (1, 2)
C42 56PF 50V 5% 1206 NPO (1, 2)
R76 24K OHMS 1/4W 5% 200PPM (1, 2)

9639 E140: 6 — 3 — ED IN H; 5

XCVR Ports included for prototype build only (not for FRS design)

REVISIONS

CHK	CHANGE NO.	REV

[Kernel]

VIC, SSC, BOOT PROM [SERIAL PORTS/protos only]

digital

DRN: K. Yesse	DATE -	ENG: M. Dutaxus	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
- Thu Oct 20 17:12:58 1988		SHEET 7	
FIRST USED ON OPTION/MODEL: -		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

Bad Address Detector

8 BIT COMP 74F521 E152 SOIC

A=B 19 → NXM H

B7 18, A7 17, B6 16, A6 15, B5 14, A5 13, B4 12, A4 11, B3 9, A3 8, B2 7, A2 6, B1 5, A1 4, B0 3, A0 2, EN 1

RGND 13 L

Processor Memory Decoder PAL

LOGIC ARRAY 20L8B E122 PLCC

*DEFAULT

PRMDE

IO6 25 SRAM BANK 1 CS L
IO5 24 SRAM BANK 2 CS L
IO4 23 SCRATCH PAD CS L
IO3 22 CODE STR 1 CS L
IO2 21 CODE STR 2 CS L
IO1 20 CODE STR 3 CS L

O2 26 FAST MEM ACT L
O1 18 SLOW MEM ACT L

I14 27, I13 17, I12 16, I11 14, I10 13, I9 12, I8 10, I7 9, I6 7, I5 6, I4 4, I3 3, I2 2, I1 1

CADDR 29 H, CADDR 21 H, CADDR 20 H, CADDR 19 H, CADDR 18 H, CADDR 17 H

VCCR 42 H
DESELECT L

NOTE: Series resistors should be placed as close to 841 chips as possible.

CMOS BUS INTERFACE 74FCT841 E89 SOIC

CDAL 31 H	11 D10	Q10 14	R162 33 OHMS 1/4W 5% 200PPM — CADDR 31 H
CDAL 30 H	10 D9	Q9 15	R177 33 OHMS 1/4W 5% 200PPM — CADDR 30 H
CDAL 29 H	9 D8	Q8 16	R163 33 OHMS 1/4W 5% 200PPM — CADDR 29 H
CDAL 28 H	8 D7	Q7 17	R178 33 OHMS 1/4W 5% 200PPM — CADDR 28 H
CDAL 27 H	7 D6	Q6 18	R189 33 OHMS 1/4W 5% 200PPM — CADDR 27 H
CDAL 26 H	6 D5	Q5 19	R190 33 OHMS 1/4W 5% 200PPM — CADDR 26 H
CDAL 25 H	5 D4	Q4 20	R179 33 OHMS 1/4W 5% 200PPM — CADDR 25 H
CDAL 24 H	4 D3	Q3 21	R191 33 OHMS 1/4W 5% 200PPM — CADDR 24 H
CDAL 23 H	3 D2	Q2 22	R164 33 OHMS 1/4W 5% 200PPM — CADDR 23 H
CDAL 22 H	2 D1	Q1 23	R187 33 OHMS 1/4W 5% 200PPM — CADDR 22 H
	1 OE		
	13 LE		

CMOS BUS INTERFACE 74FCT841 E76 SOIC

CDAL 21 H	11 D10	Q10 14	R200 33 OHMS 1/4W 5% 200PPM — CADDR 21 H
CDAL 20 H	10 D9	Q9 15	R209 33 OHMS 1/4W 5% 200PPM — CADDR 20 H
CDAL 19 H	9 D8	Q8 16	R195 33 OHMS 1/4W 5% 200PPM — CADDR 19 H
CDAL 18 H	8 D7	Q7 17	R202 33 OHMS 1/4W 5% 200PPM — CADDR 18 H
CDAL 17 H	7 D6	Q6 18	R203 33 OHMS 1/4W 5% 200PPM — CADDR 17 H
CDAL 16 H	6 D5	Q5 19	R211 33 OHMS 1/4W 5% 200PPM — CADDR 16 H
CDAL 15 H	5 D4	Q4 20	R196 33 OHMS 1/4W 5% 200PPM — CADDR 15 H
CDAL 14 H	4 D3	Q3 21	R204 33 OHMS 1/4W 5% 200PPM — CADDR 14 H
CDAL 13 H	3 D2	Q2 22	R197 33 OHMS 1/4W 5% 200PPM — CADDR 13 H
CDAL 12 H	2 D1	Q1 23	R207 33 OHMS 1/4W 5% 200PPM — CADDR 12 H
	1 OE		
	13 LE		

CMOS BUS INTERFACE 74FCT841 E107 SOIC

CDAL 11 H	11 D10	Q10 14	R112 33 OHMS 1/4W 5% 200PPM — CADDR 11 H
CDAL 10 H	10 D9	Q9 15	R135 33 OHMS 1/4W 5% 200PPM — CADDR 10 H
CDAL 09 H	9 D8	Q8 16	R126 33 OHMS 1/4W 5% 200PPM — CADDR 09 H
CDAL 08 H	8 D7	Q7 17	R136 33 OHMS 1/4W 5% 200PPM — CADDR 08 H
CDAL 07 H	7 D6	Q6 18	R113 33 OHMS 1/4W 5% 200PPM — CADDR 07 H
CDAL 06 H	6 D5	Q5 19	R137 33 OHMS 1/4W 5% 200PPM — CADDR 06 H
CDAL 05 H	5 D4	Q4 20	R127 33 OHMS 1/4W 5% 200PPM — CADDR 05 H
CDAL 04 H	4 D3	Q3 21	R128 33 OHMS 1/4W 5% 200PPM — CADDR 04 H
CDAL 03 H	3 D2	Q2 22	R114 33 OHMS 1/4W 5% 200PPM — CADDR 03 H
CDAL 02 H	2 D1	Q1 23	R150 33 OHMS 1/4W 5% 200PPM — CADDR 02 H
RGND 4 L	1 OE		
AS L	13 LE		

CVAX Address Latches

REG CS 2 H
BUF AS L

Board 2 Decoder PAL

LOGIC ARRAY 20L8B E137 PLCC

*DEFAULT

HIBSD

IO6 25 CSICB CS L
IO5 24 DATA BUF CS L
IO4 23 BRD2 CS L
IO3 22 SISM CS L
IO2 21 HIB REG CS L
IO1 20

O2 26 CSICA CS L
O1 18 BRD2 ACT L

I14 27 REG CS 2 H, I13 17 BUF AS L, I12 16 CADDR 29 H, I11 14 CADDR 20 H, I10 13 CADDR 19 H, I9 12 CADDR 18 H, I8 10 CADDR 17 H, I7 9 CADDR 16 H, I6 7 CADDR 15 H, I5 6 CADDR 14 H, I4 4 CADDR 13 H, I3 3 CADDR 12 H, I2 2 CADDR 11 H, I1 1 CADDR 10 H

XIC/Processor Register Decoder PAL

LOGIC ARRAY 20L8B E118 PLCC

*DEFAULT

XICSD

IO6 25 DPC CS L
IO5 24 CXHIC CS L
IO4 23 XISM CS L
IO3 22 WR DIAG CS L
IO2 21 RD DIAG CS L
IO1 20

O2 26 VIC CS L
O1 18 XIC ACT L

I14 27, I13 17, I12 16, I11 14, I10 13, I9 12, I8 10, I7 9, I6 7, I5 6, I4 4, I3 3, I2 2, I1 1

^ for reference only; these are Notes, not signal names

REVISIONS

CHK	CHANGE NO.	REV

[Kernel]

ADDRESS LATCHES & DECODER PALS, II ADDRESS PAL

digital

DRN: Rev. Jackson — DATE: -

CHK'D: - — DATE: -

ENG: Rev. Calvert — DATE: -

BOARD LOCATION: CXO

SHEET 8

Thu Oct 20 17:13:48 1988

FIRST USED ON OPTION/MODEL: -

NEXT HIGHER ASSEMBLY: -

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

Registered Control Signals

CMOS BUS INTERFACE 74FCT843 E112 — SOIC

VCCR 20 H	10	D9	
		Q9	15
CSDP 2 H	9	D8	
		Q8	16 — REG CS 2 H
CSDP 1 H	8	D7	
		Q7	17 — REG CS 1 H
CSDP 0 H	7	D6	
		Q6	18 — REG CS 0 H
BM 3 L	6	D5	
		Q5	19 — REG BM 3 L
BM 2 L	5	D4	
		Q4	20 — REG BM 2 L
BM 1 L	4	D3	
		Q3	21 — REG BM 1 L
BM 0 L	3	D2	
		Q2	22 — REG BM 0 L
WR L	2	D1	
		Q1	23 — REG WR L
RGND 6 L	1	OE	
VCCR 21 H	14	PRE	
AS L	11	CLR	
	13	LE	

OCTAL DRIVER 74FCT244A E119 — SOIC

		Y3	3 — BUF AS L
	17	A3	
		Y2	5 — BUF DS L
DS L	15	A2	
		Y1	7 — BUF DBE L
DBE L	13	A1	
		Y0	9 — CLK 10MHZ H
~~ACLKC H~~	~~11~~	~~A0~~	
RGND 7 L	19	EN	

Buffered Control Signals

Memory Control PAL

LOGIC ARRAY 20R4B E150 — PLCC

*DEFAULT
MCTRL

		IO26	26 — DESELECT L
		IO25	25 — DEASSERT L
		IO20	20
		IO18	18
		RO24	24 — INV ADDR H
		RO23	23
		RO22	22
		RO21	21
VCCR 44 H	27	I27	
	17	I17	
	14	I14	
	13	I13	
CADDR 31 H	12	I12	
CADDR 30 H	10	I10	
SYSRST L	9	I9	
READY H	7	I7	
	6	I6	REG WR L
	4	I4	BUF AS L
	3	I3	BUF DS L
ACLKB H	2	I2	ACLKB H
ACLKC H	1	RCLK1	
RGND 5 L	16	OE16	

Notes for reference only ^

SOIC: 74F86 E142

	12	
CADDR 02 H	13	
	11	MEM ADDR 02 H

Register Control PAL

LOGIC ARRAY 20L8B E151 — PLCC

*DEFAULT
RGCTL

		IO6	25 — RD DIAG CLK H
		IO5	24 — RD DIAG ENA L
		IO4	23 — ERR ADDR RDBK L
		IO3	22 — ERR ADDR CLK H
		IO2	21 — PERR CLK H
		IO1	20 — PAR CLK H
		O2	26 — WR DIAG CLK H
		O1	18 — WR DIAG RDBK L
VCCR 43 H	27	I14	
	17	I13	
DCLK DIS L	16	I12	
	14	I11	
RD DIAG CS L	13	I10	
WR DIAG CS L	12	I9	
ERR ADDR CS L	10	I8	
REG CS 2 H	9	I7	
REG WR L	7	I6	
BUF AS L	6	I5	
BUF DS L	4	I4	
ACLKB H	3	I3	
	2	I2	
ACLKC H	1	I1	

Notes for reference only ^

Ready PAL

LOGIC ARRAY 20R4B E146 — PLCC

READY

		IO26	26 — READY H
BRD2 ACT L		IO25	25
		IO20	20
		IO18	18 — READY L *
ALLOW_CONNECT = TRUE		RO24	24
		RO23	23 — HE 3 L *
		RO22	22 — HE 2 L *
		RO21	21 — HE 1 L *
BUSCLK H	27	I27	
HIB DIR H	17	I17	
LOCK L	14	I14	
NXM H	13	I13	
RD DIAG CS L	12	I12	
WR DIAG CS L	10	I10	
FAST MEM ACT L	9	I9	
SLOW MEM ACT L	7	I7	
REG WR L	6	I6	
BUF AS L	4	I4	
BUF DS L	3	I3	
XIC ACT L	2	I2	
ACLKC H	1	RCLK1	
RGND 1 L	16	OE16	

SOIC: 74F38 E153

SYSRST L	10	
	9	
	8	RDY L

Error Address Registers

D-TYPE FLIP-FLOP 74ALS374 E154 — PLCC

CADDR 31 H	18	D7	
		Q7	19 — CDAL 31 H
CADDR 30 H	17	D6	
		Q6	16 — CDAL 30 H
CADDR 29 H	14	D5	
		Q5	15 — CDAL 29 H
CADDR 28 H	13	D4	
		Q4	12 — CDAL 28 H
CADDR 27 H	8	D3	
		Q3	9 — CDAL 27 H
CADDR 26 H	7	D2	
		Q2	6 — CDAL 26 H
CADDR 25 H	4	D1	
		Q1	5 — CDAL 25 H
CADDR 24 H	3	D0	
		Q0	2 — CDAL 24 H
ERR ADDR CLK H	11	CLK	
ERR ADDR RDBK L	1	EN	

D-TYPE FLIP-FLOP 74ALS374 E136 — PLCC

CADDR 23 H	18	D7	
		Q7	19 — CDAL 23 H
CADDR 22 H	17	D6	
		Q6	16 — CDAL 22 H
CADDR 21 H	14	D5	
		Q5	15 — CDAL 21 H
CADDR 20 H	13	D4	
		Q4	12 — CDAL 20 H
CADDR 19 H	8	D3	
		Q3	9 — CDAL 19 H
CADDR 18 H	7	D2	
		Q2	6 — CDAL 18 H
CADDR 17 H	4	D1	
		Q1	5 — CDAL 17 H
CADDR 16 H	3	D0	
		Q0	2 — CDAL 16 H
	11	CLK	
	1	EN	

D-TYPE FLIP-FLOP 74ALS374 E138 — PLCC

CADDR 15 H	18	D7	
		Q7	19 — CDAL 15 H
CADDR 14 H	17	D6	
		Q6	16 — CDAL 14 H
CADDR 13 H	14	D5	
		Q5	15 — CDAL 13 H
CADDR 12 H	13	D4	
		Q4	12 — CDAL 12 H
CADDR 11 H	8	D3	
		Q3	9 — CDAL 11 H
CADDR 10 H	7	D2	
		Q2	6 — CDAL 10 H
CADDR 09 H	4	D1	
		Q1	5 — CDAL 09 H
CADDR 08 H	3	D0	
		Q0	2 — CDAL 08 H
	11	CLK	
	1	EN	

D-TYPE FLIP-FLOP 74ALS374 E121 — PLCC

CADDR 07 H	18	D7	
		Q7	19 — CDAL 07 H
CADDR 06 H	17	D6	
		Q6	16 — CDAL 06 H
CADDR 05 H	14	D5	
		Q5	15 — CDAL 05 H
CADDR 04 H	13	D4	
		Q4	12 — CDAL 04 H
CADDR 03 H	8	D3	
		Q3	9 — CDAL 03 H
CADDR 02 H	7	D2	
		Q2	6 — CDAL 02 H
RGND 19 L	4	D1	
		Q1	5 — CDAL 01 H
	3	D0	
		Q0	2 — CDAL 00 H
	11	CLK	
	1	EN	

* Output used for feedback within PAL

REVISIONS		
CHK	CHANGE NO.	REV

[Kernel]
CVAX BUFFER/REGISTERS, CTRL PALS, ERROR ADDR REGS

digital

Thu Oct 20 17:14:21 1988

FIRST USED ON OPTION/MODEL: -

DRN: K. Yesse	-	ENG: R. Reagan	-
CHK'D: -	DATE -	BOARD LOCATION: CXO	DATE
		SHEET 9	
		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

XIC VCR Register

8D LATCH 74ALS666 E94 (SOIC)
- Q7/D7 — DPC TEST L
- Q6/D6 — PREEMPT H
- Q5/D5 — CRAM TST DIS H
- Q4/D4
- Q3/D3
- Q2/D2
- Q1/D1
- Q0/D0 — LED ENA H

8D LATCH 74ALS666 E106 (SOIC)
- Q7/D7
- Q6/D6
- Q5/D5
- Q4/D4
- Q3/D3
- Q2/D2
- Q1/D1
- Q0/D0

WR DIAG RDBK L
RGND 11 L
→ OERB, OE2, OE1

VCCR 26 H
SYSRST L
WR DIAG CLK H
→ PRE, CLR, C

CDAL 31 H
CDAL 30 H
CDAL 29 H
CDAL 28 H
CDAL 27 H [CVAX PERR]
CDAL 26 H [DPC PERR]
CDAL 25 H [VIC ERROR]
CDAL 24 H

CDAL 23 H
CDAL 22 H
CDAL 21 H
CDAL 20 H
CDAL 19 H
CDAL 18 H
CDAL 17 H
CDAL 16 H

Write Diagnostics Registers

8D LATCH 74ALS666 E80 (SOIC)
- Q7/D7 — CVAX PAR FEC H
- Q6/D6 — ERR DISABLE L
- Q5/D5 — CVAX DPE DIS L
- Q4/D4 — XIC ERR RESET L
- Q3/D3 — DIAG PIRQ L
- Q2/D2 — MIST DONE H [not a signal name]
- Q1/D1 — MIST FAIL H
- Q0/D0 — WREN H

8D LATCH 74ALS666 E69 (SOIC)
- Q7/D7 — DPC RESET L
- Q6/D6 — VIC RESET L
- Q5/D5 — BRD2 RESET L
- Q4/D4 — CXHIC RESET L
- Q3/D3 — XIC DATA FEC H
- Q2/D2 — HIB CTRL FEC H
- Q1/D1 — HIB ADDR FEC H
- Q0/D0 — CVAX DATA FEC H

→ OERB, OE2, OE1

→ PRE, CLR, C

CDAL 15 H
CDAL 14 H
CDAL 13 H
CDAL 12 H
CDAL 11 H
CDAL 10 H
CDAL 09 H
CDAL 08 H

CDAL 07 H
CDAL 06 H
CDAL 05 H
CDAL 04 H
CDAL 03 H
CDAL 02 H
CDAL 01 H
CDAL 00 H

Memory Error PAL

PAL REGISTERED 20RA10 E104 (PLCC)
*!DEFAULT
MEMER

- IO9 — VIC ERROR L *
- IO8 — MEM ERR L
- IO7 — DCLK DIS L
- IO6 — BUS TIMEOUT L *
- IO5 — PAL RESET L
- IO4
- IO3
- IO2
- IO1
- IO0 — XIC ERR RESET L
- I9 — BUF DS L
- I8 — ACLKC H
- I7 — CVAX PAR ERR H
- I6 — SYSRST L
- I5 — REG CS 2 H
- I4 — HIB PERR L
- I3 — ERR DISABLE L
- I2 — RD DIAG ENA L
- I1 — SYSERR L
- I0
- PL — VCCR 28 H
- OE — RGND 12 L

SOIC 74F32 E130
- RD DIAG CS L
- PROM READ L
- → REG OEN L

D-TYPE FLIP-FLOP 74ALS374 E72 (PLCC)
- VCCR 27 H → D7
- D6
- D5
- D4
- CSDP 3 H → D3
- CSDP 2 H → D2
- CSDP 1 H → D1
- CSDP 0 H → D0
- PAR CLK H
- RD DIAG ENA L → EN
- Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0 → CLK

D-TYPE FLIP-FLOP 74ALS374 E84 (PLCC)
- CXHIC CS L → D7
- DPC CS L → D6
- SRAM BANK 2 CS L → D5
- SRAM BANK 1 CS L → D4
- SCRATCH PAD CS L → D3
- CSICB CS L → D2
- CSICA CS L → D1
- DATA BUF CS L → D0
- RD DIAG CLK H → EN
- Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0 → CLK

D-TYPE FLIP-FLOP 74ALS374 E95 (PLCC)
- VCCR 27 H → D7
- D6
- BRD2 CS L → D5
- NXM H → D4
- REG WR L → D3
- DPC IDLE L → D2
- J2 H → D1
- J1 H → D0
- Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0 → CLK
- EN

Read Diagnostics Registers

* Output used for feedback within PAL

REVISIONS

CHK	CHANGE NO.	REV

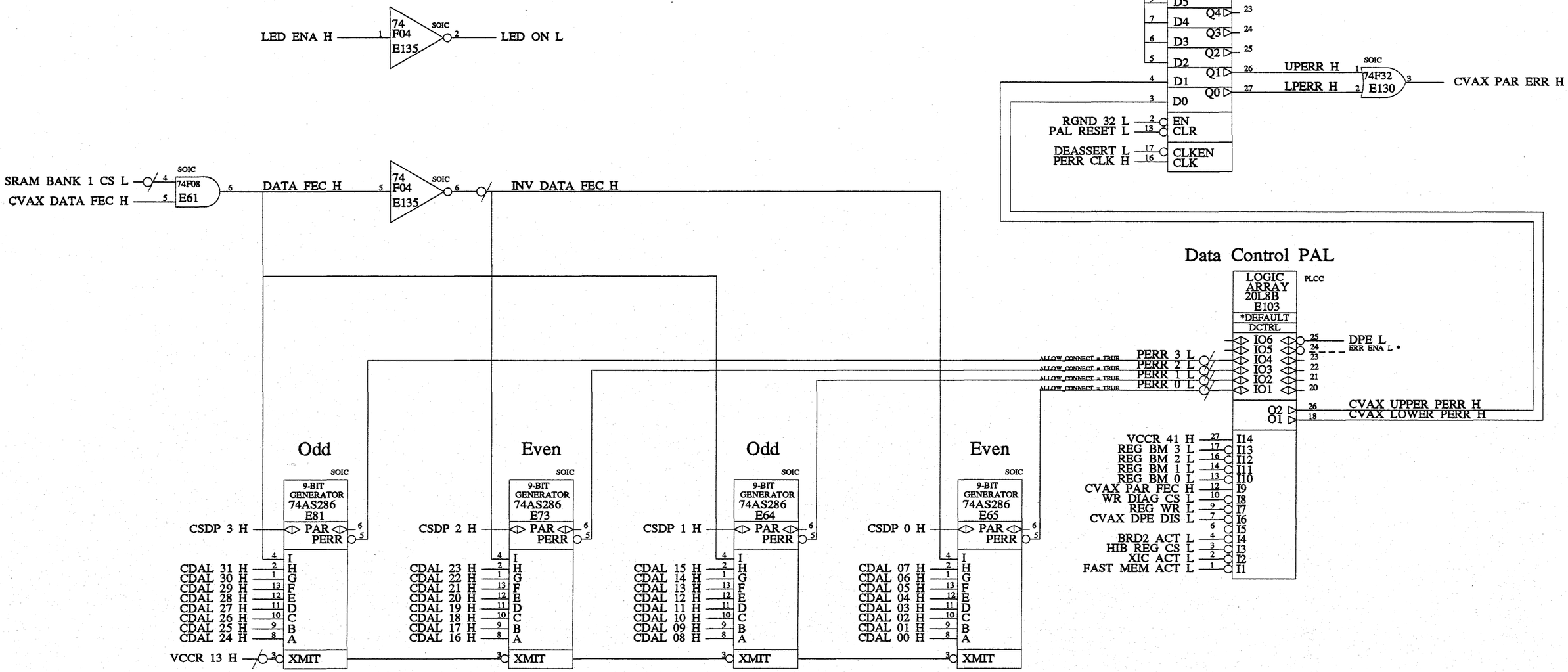
[Kernel]
PROCESSOR REGISTERS [R-W DIAG/XIC VCR], MEM ERR PAL

digital

DRN: K. Yesse	DATE -	ENG: Col. North	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
- Thu Oct 20 16:39:03 1988		SHEET 10	
FIRST USED ON OPTION/MODEL: -		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88



REVISIONS		
CHK	CHANGE NO.	REV

[Kernel]

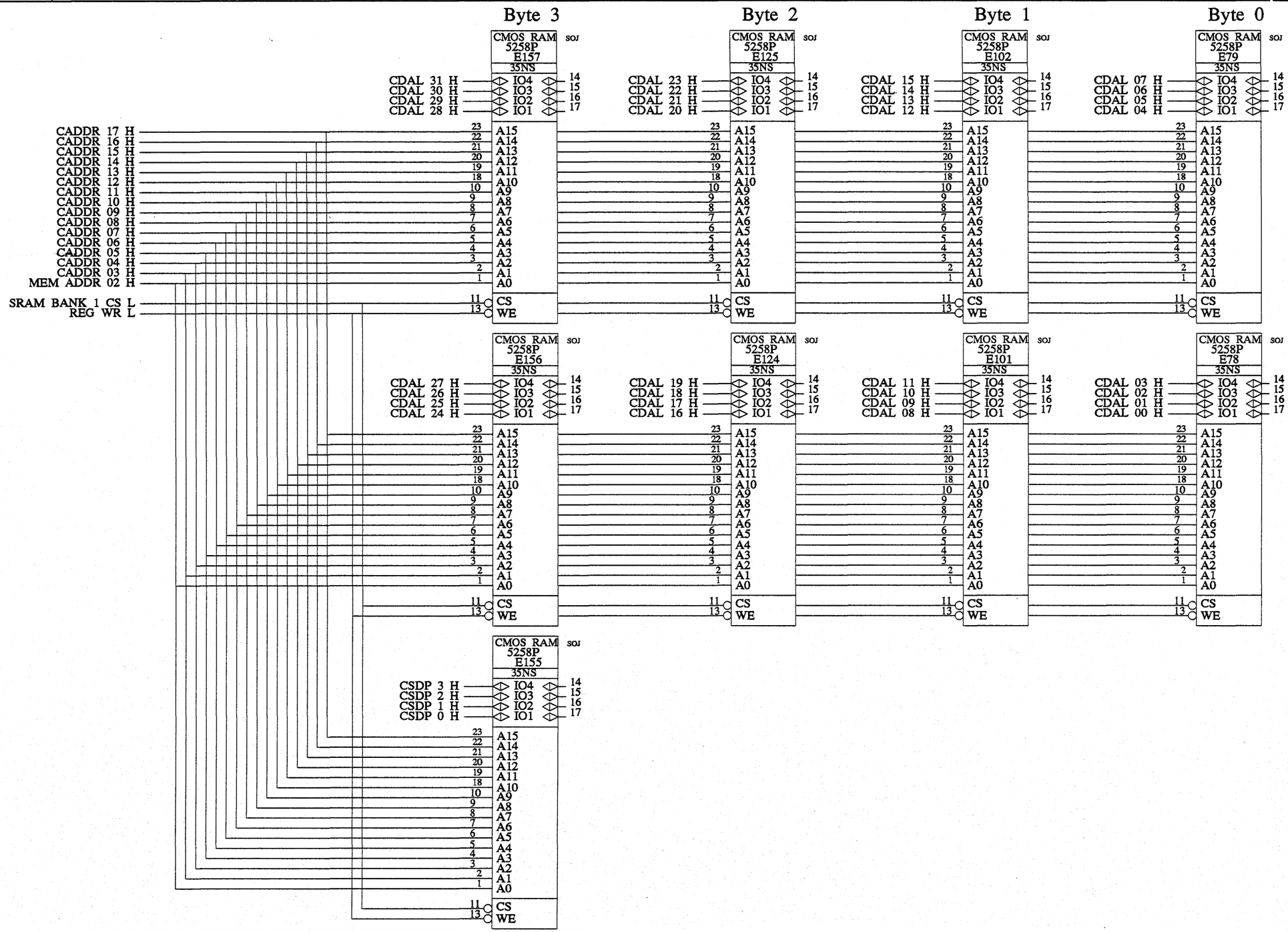
READ/WRITE PARITY CHECKERS, DATA CONTROL PAL

digital

DRN: K. Yesse	DATE -	ENG: H. Kinlaw	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
- Thu Oct 20 16:39:24 1988		SHEET 11	
FIRST USED ON OPTION/MODEL: -		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88



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REVISIONS		
CHK	CHANGE NO.	REV

[Kernel]

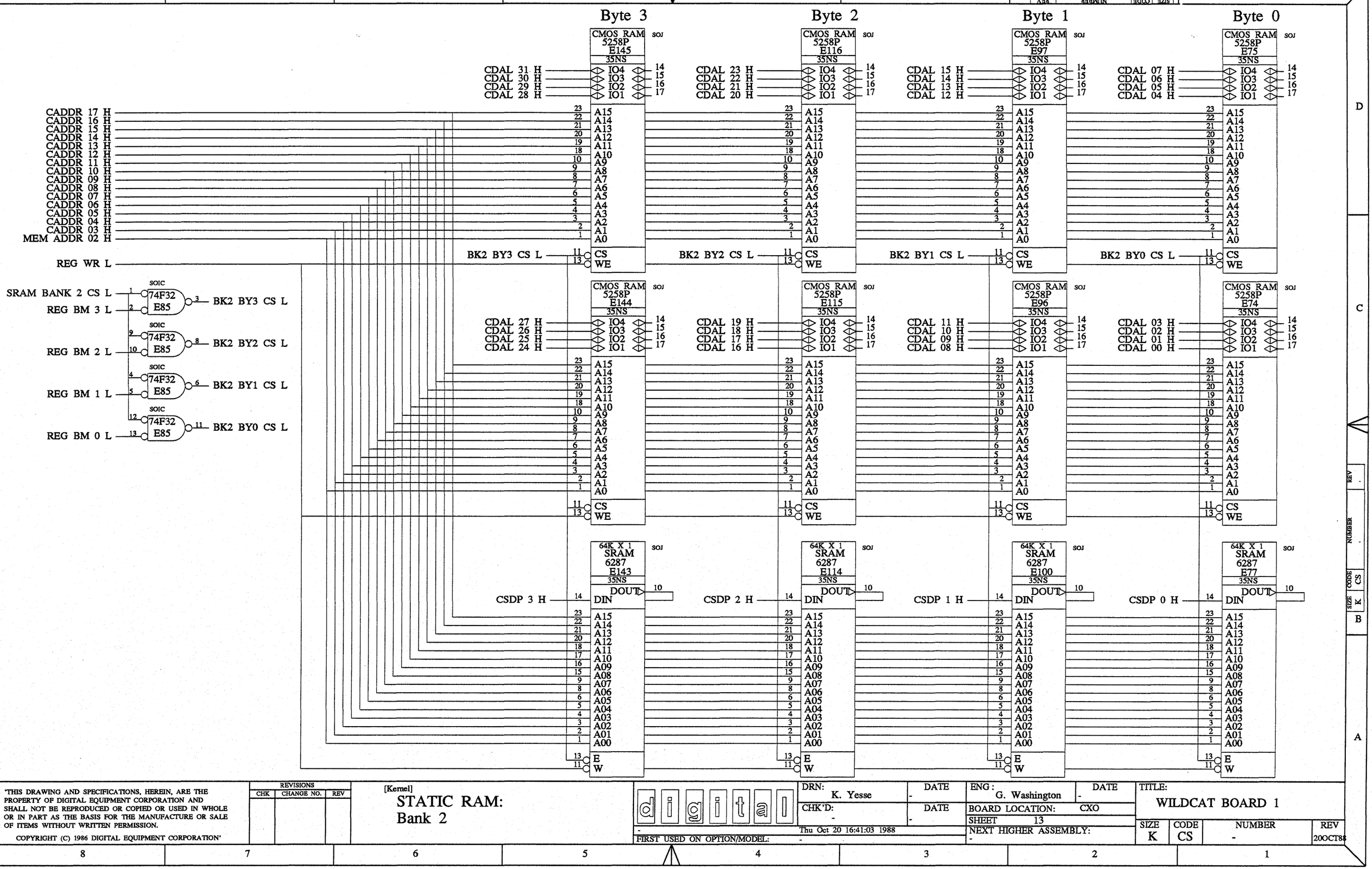
STATIC RAM: Bank 1

digital

DRN: K. Yesse	DATE -	ENG: G. Bush	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
- Thu Oct 20 16:40:03 1988		SHEET 12	
FIRST USED ON OPTION/MODEL: -		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88



REVISIONS		
CHK	CHANGE NO.	REV

[Kernel]

STATIC RAM: Bank 2

digital

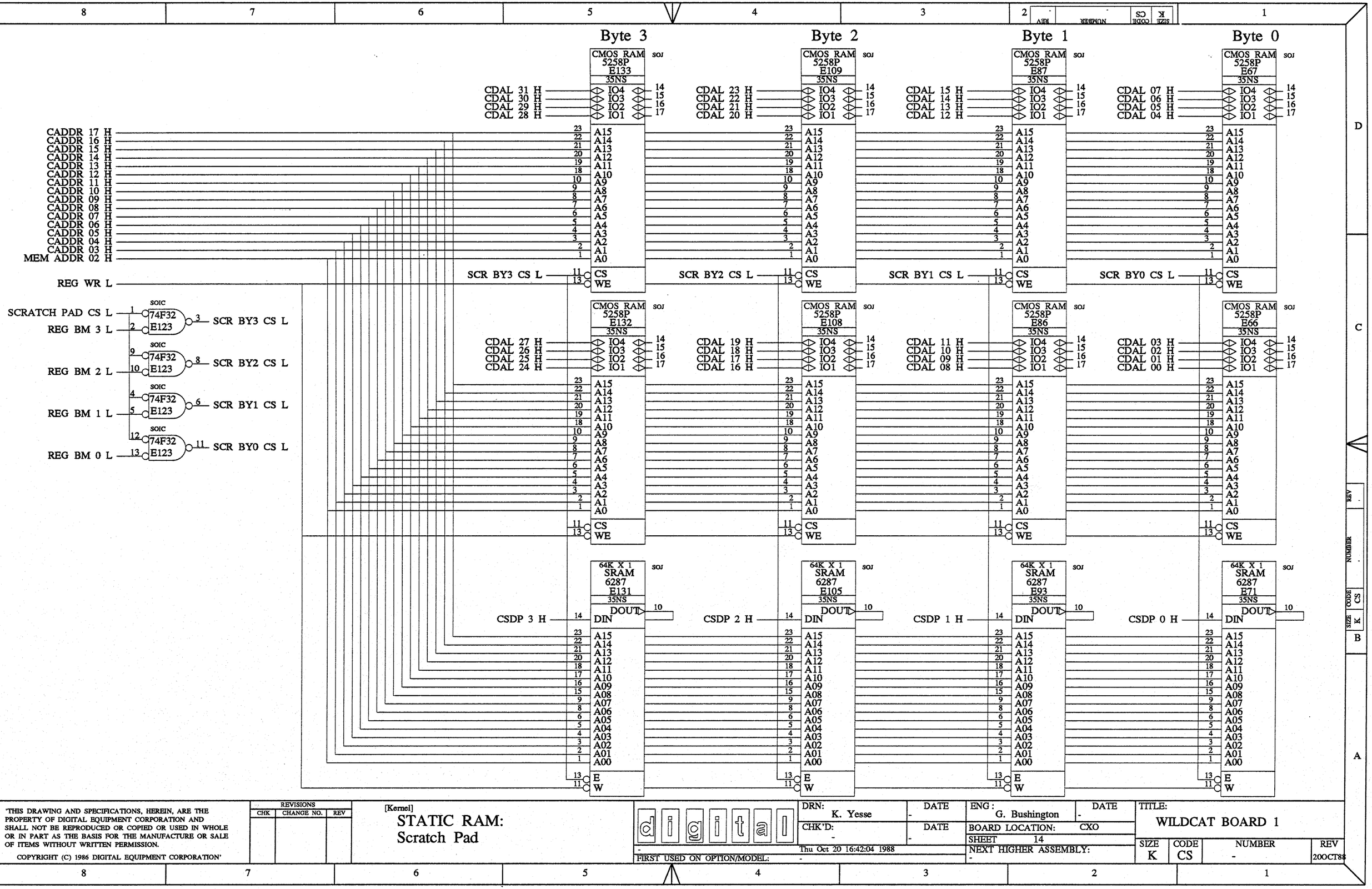
Thu Oct 20 16:41:03 1988

FIRST USED ON OPTION/MODEL: -

DRN: K. Yesse	DATE -	ENG: G. Washington	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
		SHEET 13	
		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88



REVISIONS		
CHK	CHANGE NO.	REV

[Kernel]

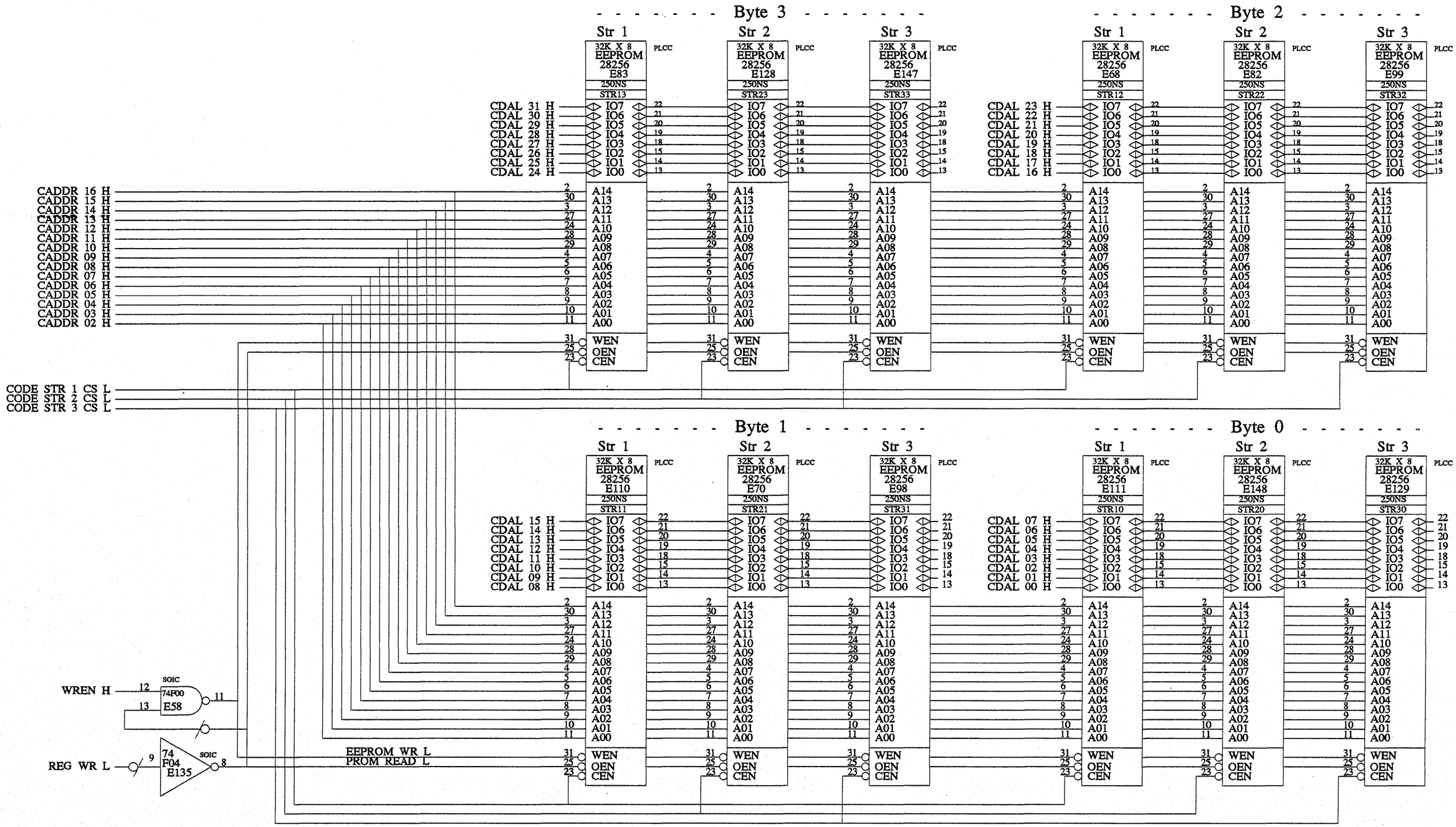
STATIC RAM: Scratch Pad

digital

DRN: K. Yesse	DATE -	ENG: G. Bushington	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
- Thu Oct 20 16:42:04 1988		SHEET 14	
FIRST USED ON OPTION/MODEL: -		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88



REVISIONS		
CHK	CHANGE NO.	REV

[Kernel]

EEPROMS:
Banks 1, 2, 3

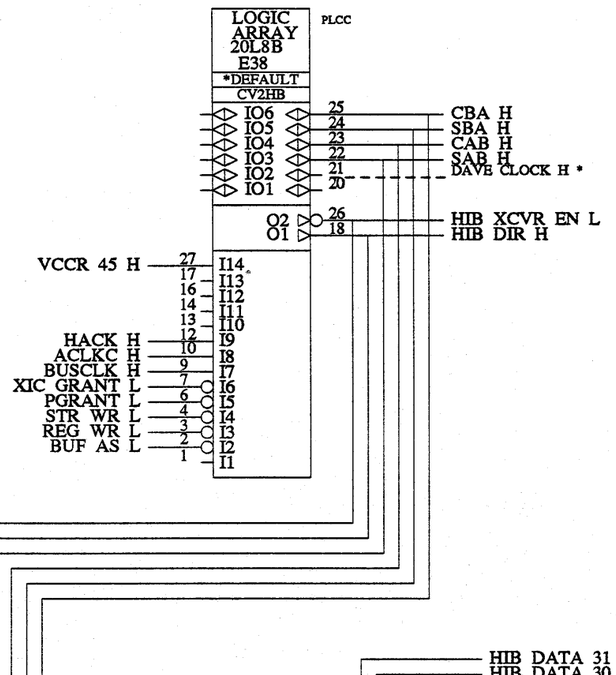
digital

DRN: K. Yesse	DATE -	ENG: A. E. Newman	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
- Thu Oct 20 16:43:28 1988		SHEET 15	
FIRST USED ON OPTION/MODEL: -		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

CVAX/HIB Data Control PAL



CVAX/HIB Data Registered XCVRs

* Output used for feedback within PAL

REVISIONS		
CHK	CHANGE NO.	REV

[HIB]

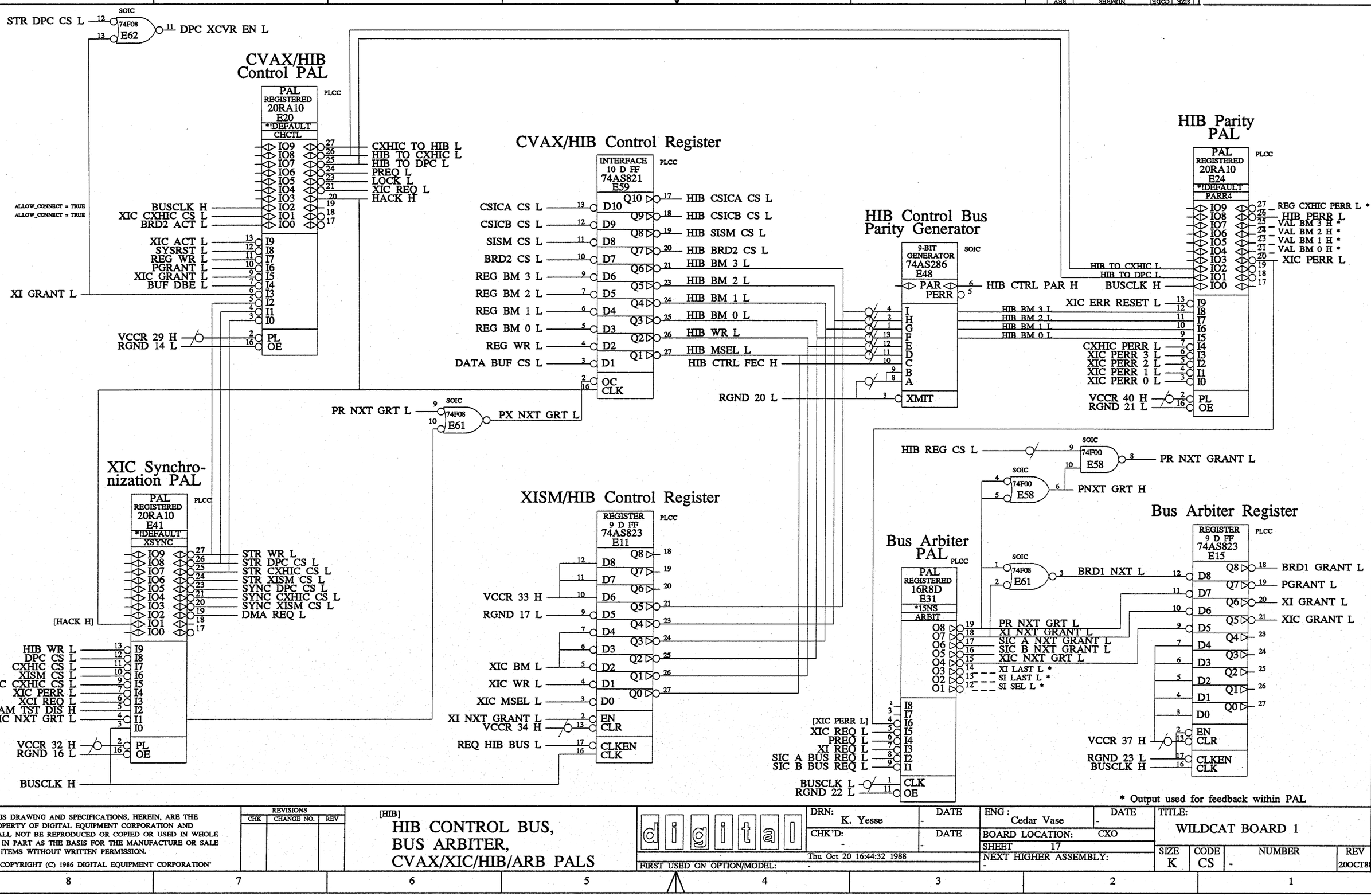
CVAX <-> HIB DATA XCVR/REGS & DATA CTRL PAL

digital

DRN: K. Yesse	DATE -	ENG: V. Dersace	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
- Thu Oct 20 16:44:00 1988		SHEET 16	
FIRST USED ON OPTION/MODEL: -		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88


STR DPC CS L
74F08 E62
DPC XCVR EN L
CVAX/HIB Control PAL
PAL REGISTERED 20RA10 E20 PLCC
*!DEFAULT
CHCTL
CXHIC TO HIB L
HIB TO CXHIC L
HIB TO DPC L
PREQ L
LOCK L
XIC REQ L
HACK H
ALLOW_CONNECT = TRUE
ALLOW_CONNECT = TRUE
BUSCLK H
XIC CXHIC CS L
BRD2 ACT L
XIC ACT L
SYSRST L
REG WR L
PGRANT L
XIC GRANT L
BUF DBE L
XI GRANT L
VCCR 29 H
RGND 14 L
PL
OE
CVAX/HIB Control Register
INTERFACE 10 D FF 74AS821 E59 PLCC
CSICA CS L
CSICB CS L
SISM CS L
BRD2 CS L
REG BM 3 L
REG BM 2 L
REG BM 1 L
REG BM 0 L
REG WR L
DATA BUF CS L
HIB CSICA CS L
HIB CSICB CS L
HIB SISM CS L
HIB BRD2 CS L
HIB BM 3 L
HIB BM 2 L
HIB BM 1 L
HIB BM 0 L
HIB WR L
HIB MSEL L
HIB CTRL FEC H
OC
CLK
HIB Control Bus Parity Generator
9-BIT GENERATOR 74AS286 E48 SOIC
PAR
PERR
HIB CTRL PAR H
RGND 20 L
XMIT
HIB Parity PAL
PAL REGISTERED 20RA10 E24 PLCC
*!DEFAULT
PARR4
HIB TO CXHIC L
HIB TO DPC L
BUSCLK H
XIC ERR RESET L
HIB BM 3 L
HIB BM 2 L
HIB BM 1 L
HIB BM 0 L
CXHIC PERR L
XIC PERR 3 L
XIC PERR 2 L
XIC PERR 1 L
XIC PERR 0 L
REG CXHIC PERR L *
HIB PERR L
VAL BM 3 H *
VAL BM 2 H *
VAL BM 1 H *
VAL BM 0 H *
XIC PERR L
VCCR 40 H
RGND 21 L
PR NXT GRT L
74F08 E61
PX NXT GRT L
XIC Synchro-nization PAL
PAL REGISTERED 20RA10 E41 PLCC
*!DEFAULT
XSYNC
STR WR L
STR DPC CS L
STR CXHIC CS L
STR XISM CS L
SYNC DPC CS L
SYNC CXHIC CS L
SYNC XISM CS L
DMA REQ L
[HACK H]
HIB WR L
DPC CS L
CXHIC CS L
XISM CS L
XIC CXHIC CS L
XIC PERR L
XCI REQ L
CRAM TST DIS H
XIC NXT GRT L
VCCR 32 H
RGND 16 L
BUSCLK H
XISM/HIB Control Register
REGISTER 9 D FF 74AS823 E11 PLCC
VCCR 33 H
RGND 17 L
XIC BM L
XIC WR L
XIC MSEL L
XI NXT GRANT L
VCCR 34 H
REQ HIB BUS L
EN
CLR
CLKEN
CLK
HIB REG CS L
74F00 E58
PR NXT GRANT L
PNXT GRT H
Bus Arbiter PAL
PAL REGISTERED 16R8D E31 PLCC
*15NS
ARBIT
PR NXT GRT L
XI NXT GRANT L
SIC A NXT GRANT L
SIC B NXT GRANT L
XIC NXT GRT L
XI LAST L *
SI LAST L *
SI SEL L *
[XIC PERR L]
XIC REQ L
PREQ L
XI REQ L
SIC A BUS REQ L
SIC B BUS REQ L
BUSCLK L
RGND 22 L
CLK
OE
Bus Arbiter Register
REGISTER 9 D FF 74AS823 E15 PLCC
74F08 E61
BRD1 NXT L
BRD1 GRANT L
PGRANT L
XI GRANT L
XIC GRANT L
VCCR 37 H
RGND 23 L
BUSCLK H
* Output used for feedback within PAL
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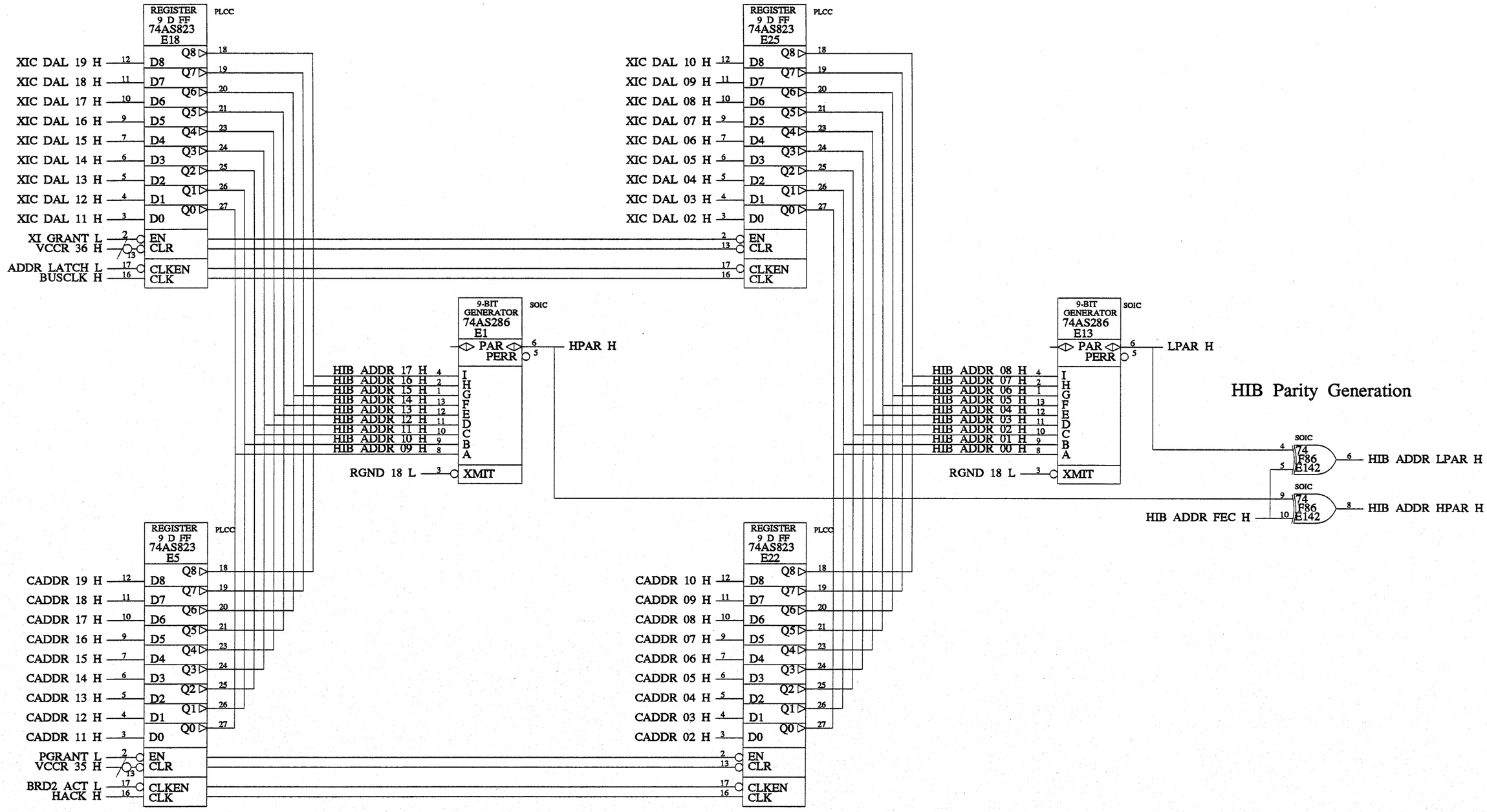
REVISIONS
CHK
CHANGE NO.
REV
[HIB]
HIB CONTROL BUS, BUS ARBITER, CVAX/XIC/HIB/ARB PALS
digital
DRN: K. Yesse
DATE -
CHK'D: -
DATE -
Thu Oct 20 16:44:32 1988
FIRST USED ON OPTION/MODEL: -
ENG: Cedar Vase
DATE -
BOARD LOCATION: CXO
SHEET 17
NEXT HIGHER ASSEMBLY: -
TITLE: WILDCAT BOARD 1
SIZE K
CODE CS
NUMBER -
REV 20OCT88

DPC/HIB Address Latches



CVAX/HIB Address Latches

REVISIONS		
CHK	CHANGE NO.	REV

[HIB]

CVAX/HIB & DPC/HIB ADDRESS LATCHES, PARITY GEN

digital

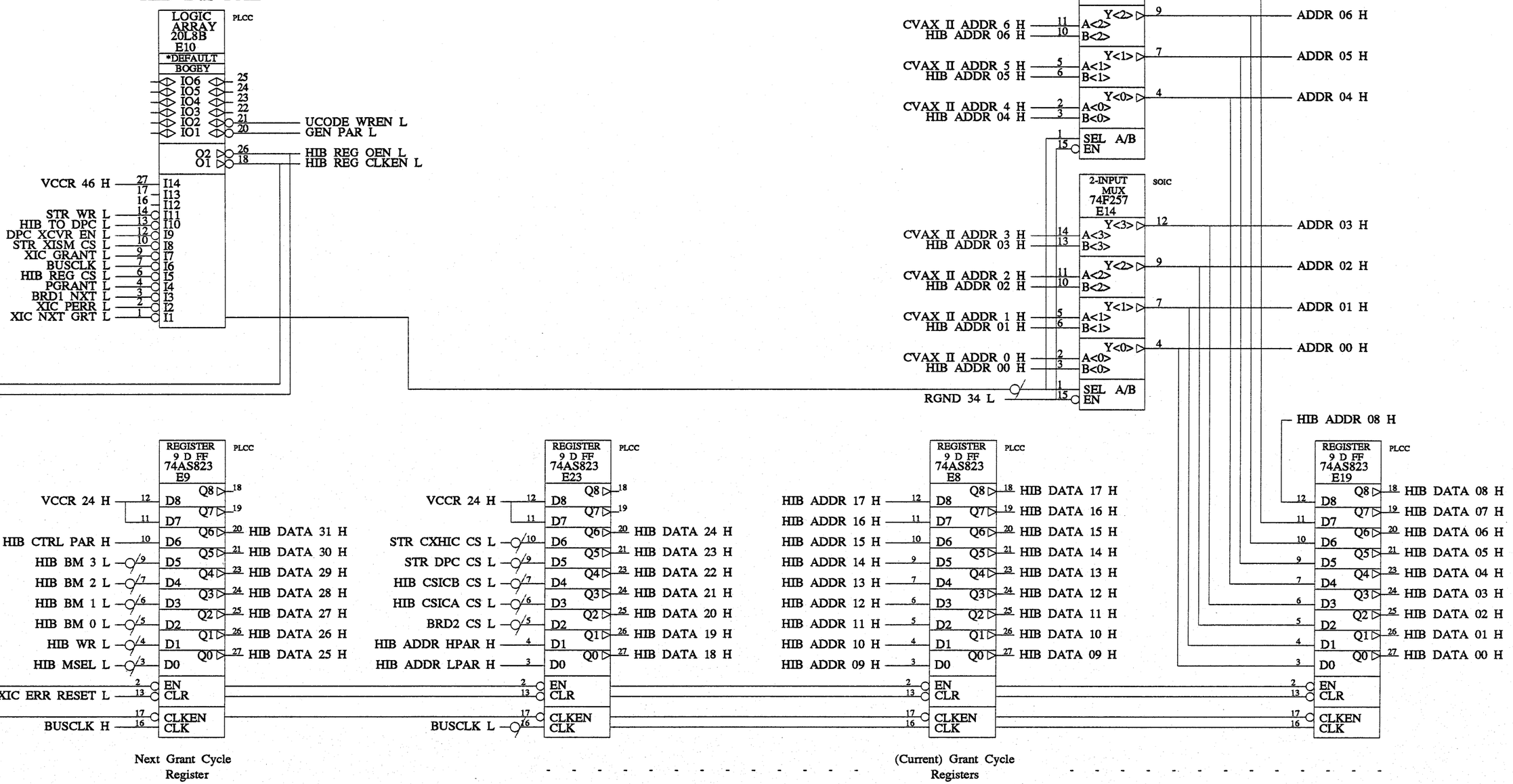
- Thu Oct 20 16:44:49 1988

FIRST USED ON OPTION/MODEL: -

DRN: K. Yesse	DATE -	ENG: B. Hoffman	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
		SHEET 18	
		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88



HIB Bus Registers

REVISIONS		
CHK	CHANGE NO.	REV

[HIB]

HIB BUS REGISTERS, MUXES

digital

FIRST USED ON OPTION/MODEL: -

DRN: K. Yesse	DATE -	ENG: R. Rabbit	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
		SHEET 19	
Thu Oct 20 16:45:09 1988		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

NOTE ON XIC DPC:

Prototype is socketed using mark eyelets (Qty 144, p/n 12-23208-03).

XIC DATA FEC H → 74 F04 E135 SOIC → INV X DATA FEC H

XIC DPC

E40

STATE MACHINE UCODE

UCODE PAR H — N7 — 31 PARITY
XIC MSEL L — R6 — 30 MEM L IO H
COUNT CTRL H — R7 — 29 CNG CNT
CLR TIMEOUT H — P7 — 28 XCI REQ
XCI REQ L — R9 — 27
MUX CTRL 4 H — R8 — 26
MUX CTRL 3 H — N9 — 25
MUX CTRL 2 H — P9 — 24 MUX CTL
MUX CTRL 1 H — P10 — 23
MUX CTRL 0 H — R10 — 22
XIC BM L — R11 — 21 WR ENA
XIC WR L — N10 — 20 WR L RD H
REQ HIB BUS L — N6 — 19 REQ BUS
REG SEL 3 H — P11 — 18
REG SEL 2 H — P12 — 17
REG SEL 1 H — R12 — 16 REG SEL
REG SEL 0 H — R13 — 15
ADDR SRC 1 H — P13 — 14
ADDR SRC 0 H — P14 — 13 ADDR SRC
ADDR INCR H — N14 — 12 ADDR INC
INIT REG 1 H — N15 — 11
INIT REG 0 H — P15 — 10 INIT REG
NEXT STATE 9 H — M14 — 09
NEXT STATE 8 H — M13 — 08
NEXT STATE 7 H — L13 — 07
NEXT STATE 6 H — M15 — 06
NEXT STATE 5 H — L15 — 05
NEXT STATE 4 H — L14 — 04
NEXT STATE 3 H — K14 — 03 NEXT ADDR
NEXT STATE 2 H — K13 — 02
NEXT STATE 1 H — J15 — 01
NEXT STATE 0 H — K15 — 00

UCODE ADDR 10 H — B14 — 10
UCODE ADDR 9 H — C14 — 9
UCODE ADDR 8 H — C15 — 8
UCODE ADDR 7 H — E14 — 7
UCODE ADDR 6 H — E13 — 6
UCODE ADDR 5 H — D15 — 5
UCODE ADDR 4 H — E15 — 4
UCODE ADDR 3 H — F15 — 3
UCODE ADDR 2 H — F14 — 2
UCODE ADDR 1 H — G14 — 1
UCODE ADDR 0 H — G15 — 0 PROM OUT

XMI CONTROLLER DATA PATH CHIP — XIC DPC

INTERNAL BUS SIGNALS

DPC D/A 31 — N4 — XIC DAL 31 H
30 — P4 — XIC DAL 30 H
29 — R2 — XIC DAL 29 H
28 — R3 — XIC DAL 28 H
27 — P3 — XIC DAL 27 H
26 — R1 — XIC DAL 26 H
25 — P1 — XIC DAL 25 H
24 — P2 — XIC DAL 24 H
23 — N2 — XIC DAL 23 H
22 — N1 — XIC DAL 22 H
21 — M1 — XIC DAL 21 H
20 — L3 — XIC DAL 20 H
19 — K3 — XIC DAL 19 H
18 — L1 — XIC DAL 18 H
17 — K1 — XIC DAL 17 H
16 — K2 — XIC DAL 16 H
15 — J2 — XIC DAL 15 H
14 — J1 — XIC DAL 14 H
13 — G2 — XIC DAL 13 H
12 — H1 — XIC DAL 12 H
11 — F1 — XIC DAL 11 H
10 — G1 — XIC DAL 10 H
09 — F3 — XIC DAL 09 H
08 — F2 — XIC DAL 08 H
07 — E2 — XIC DAL 07 H
06 — E3 — XIC DAL 06 H
05 — D3 — XIC DAL 05 H
04 — D2 — XIC DAL 04 H
03 — B1 — XIC DAL 03 H
02 — C1 — XIC DAL 02 H
01 — C2 — XIC DAL 01 H
00 — A1 — XIC DAL 00 H

BUS CLK — A7 — XIC BUSCLK H
NXT GRANT — N11 — XI NXT GRANT L
II ERROR — A13 — DXFER BAD L
BUS REQ OUT — N5 — XI REQ L
LATCH ADR — B4 — ADDR LATCH L

SHARED CVAX AND CXHIC SIGNALS

II A 6 — A6 — DPC II ADDR 6 H
5 — C7 — DPC II ADDR 5 H
4 — B7 — DPC II ADDR 4 H
3 — A5 — DPC II ADDR 3 H
2 — A8 — DPC II ADDR 2 H
1 — B9 — DPC II ADDR 1 H
0 — B8 — DPC II ADDR 0 H

CVAX SIGNALS

DPC RESET L — J14 — RESET
VCCR 23 H — B6 — 1 TESTMODE
DPC TEST L — H15 — 0 TESTMODE

DPC IDLE L — C11 — IDLE
XISM INTR L — C12 — INTERRUPT
B12 — CXHIC WRITTEN
PAGE XING H — B13 — PAGE XING
PREEMPT H — B15 — PREEMPT
A12 — IDLE STROBE
SYNC DPC CS L — P6 — CS
HIB WR L — P5 — RD

CXHIC SIGNALS

EVENT 4 — A2 — VCCR 38 H
3 — B2
2 — B3
1 — C5
0 — B5 — DXFER OK L

II WR MSK 3 — A10 — XIC II BM 3 L
2 — A9 — XIC II BM 2 L
1 — C10 — XIC II BM 1 L
0 — B10 — XIC II BM 0 L

CXHIC SEL IIRD — A14 — XIC CXHIC CS L
A4 — XIC II RD H

Byte 3 [Odd]

HIB DATA P3 H
XIC PERR 3 L

9-BIT GENERATOR 74AS286 E37 SOIC — PAR / PERR — I H G F E D C B A — XMIT

GEN PAR L

OCTAL BUS TRNCVR 74F245 E4 SOIC — B7 A7 … B0 A0 — B→A OE

INV X DATA FEC H

B7 A7 — 11 9 — HIB DATA 31 H
B6 A6 — 12 8 — HIB DATA 30 H
B5 A5 — 13 7 — HIB DATA 29 H
B4 A4 — 14 6 — HIB DATA 28 H
B3 A3 — 15 5 — HIB DATA 27 H
B2 A2 — 16 4 — HIB DATA 26 H
B1 A1 — 17 3 — HIB DATA 25 H
B0 A0 — 18 2 — HIB DATA 24 H

Byte 2 [Even]

HIB DATA P2 H
XIC PERR 2 L

9-BIT GENERATOR 74AS286 E36 SOIC — PAR / PERR — I H G F E D C B A — XMIT

GEN PAR L

OCTAL BUS TRNCVR 74F245 E16 SOIC — B7 A7 … B0 A0 — B→A OE

B7 A7 — 11 9 — HIB DATA 23 H
B6 A6 — 12 8 — HIB DATA 22 H
B5 A5 — 13 7 — HIB DATA 21 H
B4 A4 — 14 6 — HIB DATA 20 H
B3 A3 — 15 5 — HIB DATA 19 H
B2 A2 — 16 4 — HIB DATA 18 H
B1 A1 — 17 3 — HIB DATA 17 H
B0 A0 — 18 2 — HIB DATA 16 H

Byte 1 [Odd]

HIB DATA P1 H
XIC PERR 1 L

9-BIT GENERATOR 74AS286 E35 SOIC — PAR / PERR — I H G F E D C B A — XMIT

XIC DATA FEC H
GEN PAR L

OCTAL BUS TRNCVR 74F245 E26 SOIC — B7 A7 … B0 A0 — B→A OE

HIB TO DPC L
DPC XCVR EN L

B7 A7 — 11 9 — HIB DATA 15 H
B6 A6 — 12 8 — HIB DATA 14 H
B5 A5 — 13 7 — HIB DATA 13 H
B4 A4 — 14 6 — HIB DATA 12 H
B3 A3 — 15 5 — HIB DATA 11 H
B2 A2 — 16 4 — HIB DATA 10 H
B1 A1 — 17 3 — HIB DATA 09 H
B0 A0 — 18 2 — HIB DATA 08 H

Byte 0 [Even]

HIB DATA P0 H
XIC PERR 0 L

9-BIT GENERATOR 74AS286 E34 SOIC — PAR / PERR — I H G F E D C B A — XMIT

GEN PAR L

INV X DATA FEC H

OCTAL BUS TRNCVR 74F245 E27 SOIC — B7 A7 … B0 A0 — B→A OE

B7 A7 — 11 9 — HIB DATA 07 H
B6 A6 — 12 8 — HIB DATA 06 H
B5 A5 — 13 7 — HIB DATA 05 H
B4 A4 — 14 6 — HIB DATA 04 H
B3 A3 — 15 5 — HIB DATA 03 H
B2 A2 — 16 4 — HIB DATA 02 H
B1 A1 — 17 3 — HIB DATA 01 H
B0 A0 — 18 2 — HIB DATA 00 H

DPC/HIB Data XCVRs &
XIC Parity Generator/Checkers

REVISIONS

CHK	CHANGE NO.	REV

[HIB]

XIC DPC,
DPC <-> HIB XCVRS,
XIC PARITY GEN/CHECKERS

digital

Thu Oct 20 16:46:00 1988

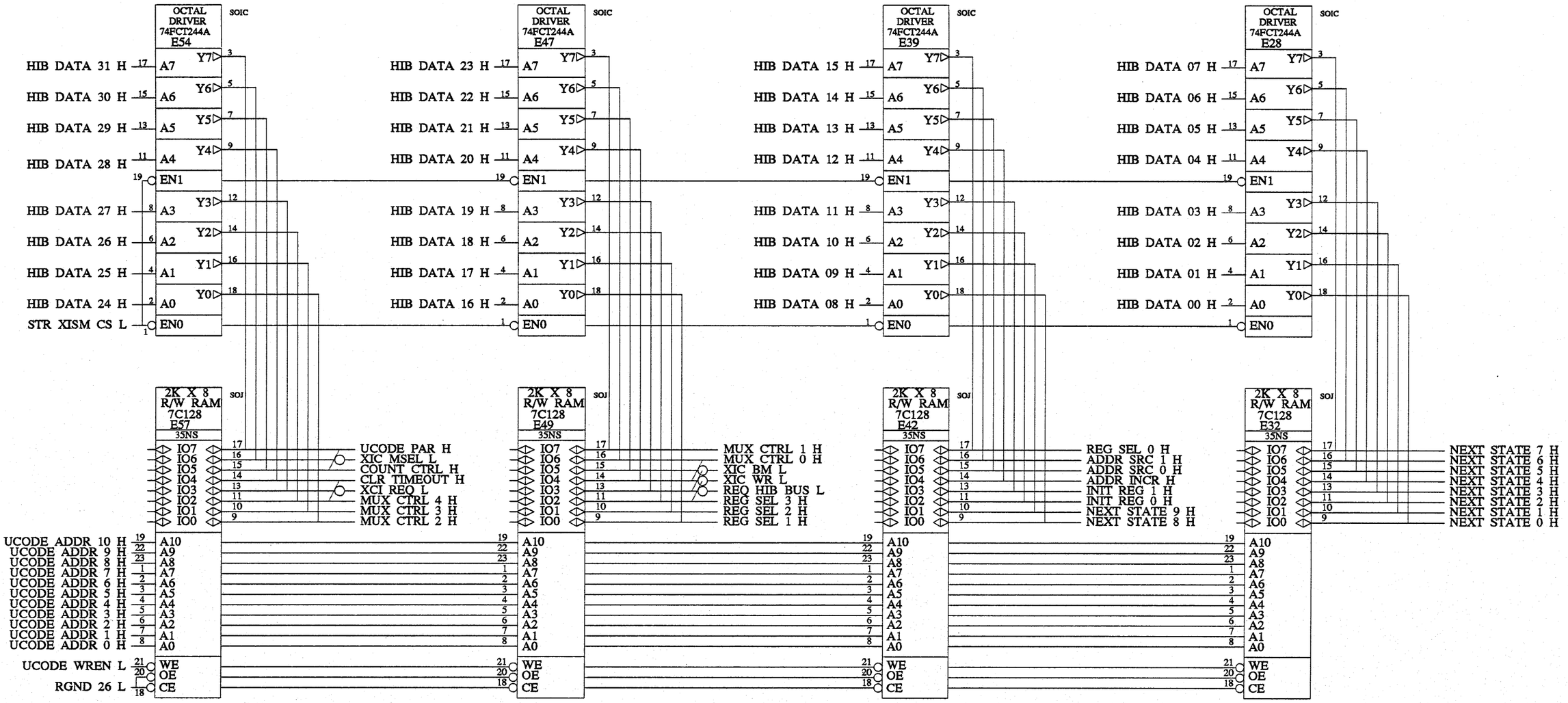
FIRST USED ON OPTION/MODEL: -

DRN: K. Yesse	DATE -	ENG: D. Versace	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
		SHEET 20	
		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

HIB Data Buffers



XIC DPC Microcode Memory

REVISIONS		
CHK	CHANGE NO.	REV

[HIB]

XIC DPC MICROCODE STATIC RAM & BUFFERS

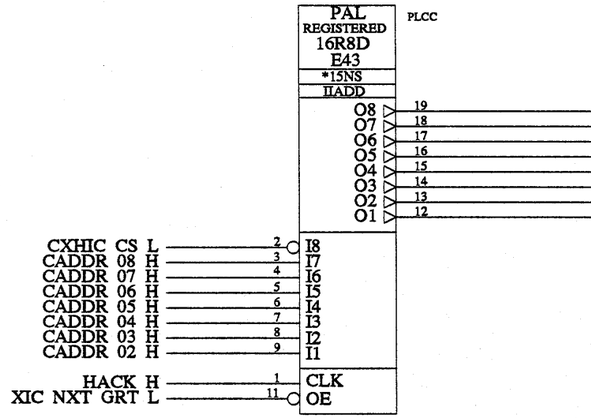
digital

- Thu Oct 20 16:46:36 1988

FIRST USED ON OPTION/MODEL: -

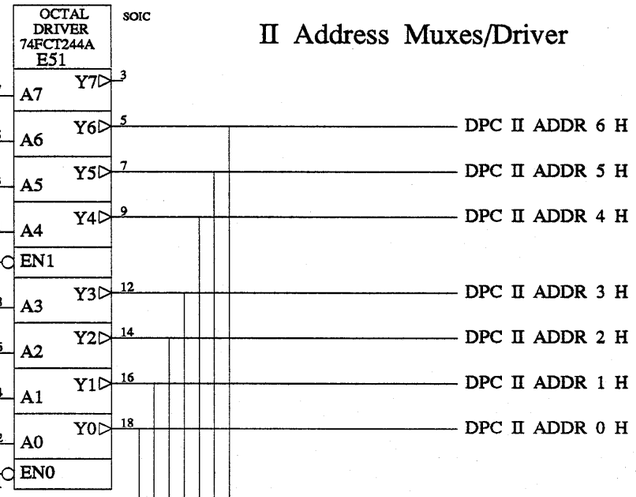
DRN: K. Yesse	- DATE	ENG: M. Gorbachev	- DATE	TITLE: WILDCAT BOARD 1	
CHK'D: -	- DATE	BOARD LOCATION: CXO			
		SHEET 21		SIZE K / CODE CS / NUMBER - / REV 20OCT88	
		NEXT HIGHER ASSEMBLY: -			

II Address Translation PAL

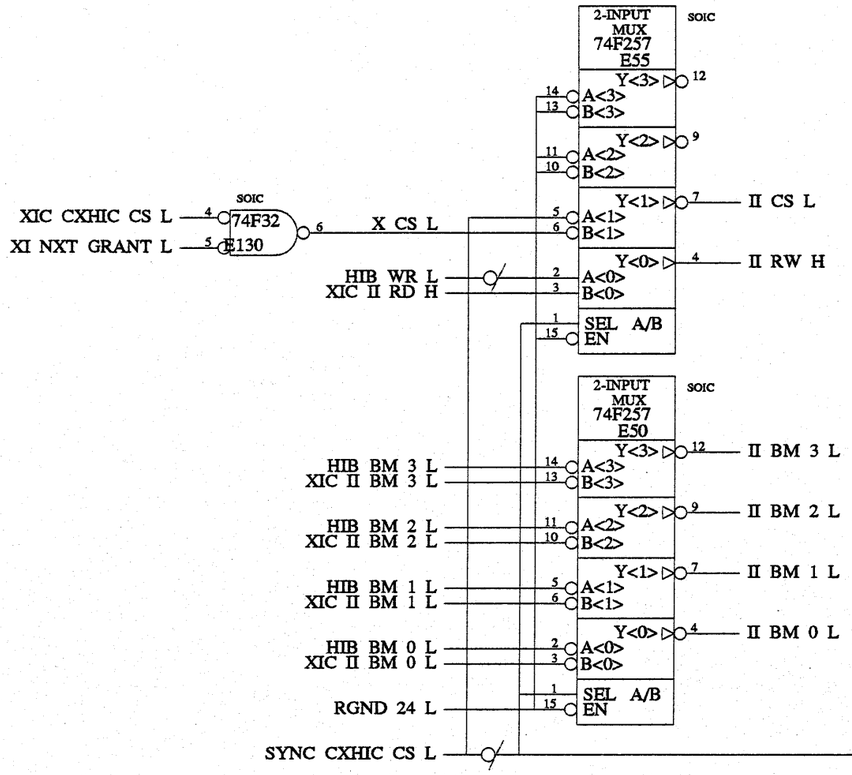


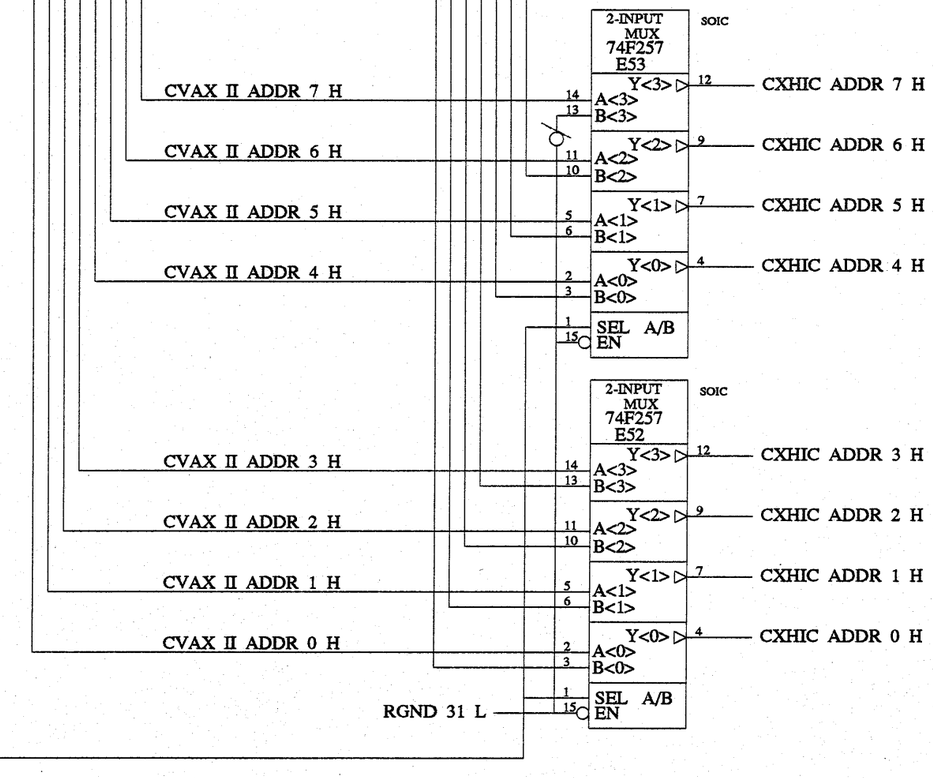
SYNC DPC CS L

II Address Muxes/Driver



II Control Mux





REVISIONS		
CHK	CHANGE NO.	REV

[HIB]

CXHIC MUX LOGIC, II ADDRESS PAL

digital

DRN: K. Yesse	DATE -	ENG: B. Hoffman	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
		SHEET 22	
-	Thu Oct 20 16:46:52 1988	NEXT HIGHER ASSEMBLY: -	
FIRST USED ON OPTION/MODEL: -			

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

CXHIC

DC7157
E30

LDCC

XCI HOLD EN H — 84 — XHOLD
XCI GC12 EN H — 85 — XGC12
XCI TBAD L — 83 — XTBAD
XCI RBAD L — 92 — XREAD
XCI DC LO L — 90 — XRDC

XCI ID5 H — 108 — 5
XCI ID4 H — 107 — 4
XCI ID3 H — 106 — 3
XCI ID2 H — 105 — 2
XCI ID1 H — 104 — 1
XCI ID0 H — 103 — 0
▽ XCIID

XCI F3 H — 112 — 3
XCI F2 H — 111 — 2
XCI F1 H — 110 — 1
XCI F0 H — 109 — 0
▽ XCIF

XCI P2 H — 102 — 2
XCI P1 H — 101 — 1
XCI P0 H — 95 — 0
▽ XCIP

XCI D63 H — 191 — 63
XCI D62 H — 190 — 62
XCI D61 H — 189 — 61
XCI D60 H — 188 — 60
XCI D59 H — 187 — 59
XCI D58 H — 186 — 58
XCI D57 H — 185 — 57
XCI D56 H — 184 — 56
XCI D55 H — 183 — 55
XCI D54 H — 182 — 54
XCI D53 H — 181 — 53
XCI D52 H — 180 — 52
XCI D51 H — 179 — 51
XCI D50 H — 178 — 50
XCI D49 H — 177 — 49
XCI D48 H — 176 — 48
XCI D47 H — 175 — 47
XCI D46 H — 174 — 46
XCI D45 H — 173 — 45
XCI D44 H — 170 — 44
XCI D43 H — 169 — 43
XCI D42 H — 168 — 42
XCI D41 H — 167 — 41
XCI D40 H — 166 — 40
XCI D39 H — 165 — 39
XCI D38 H — 164 — 38
XCI D37 H — 163 — 37
XCI D36 H — 162 — 36
XCI D35 H — 161 — 35
XCI D34 H — 160 — 34
XCI D33 H — 159 — 33
XCI D32 H — 158 — 32
XCI D31 H — 157 — 31
XCI D30 H — 156 — 30
XCI D29 H — 155 — 29
XCI D28 H — 154 — 28
XCI D27 H — 153 — 27
XCI D26 H — 152 — 26
XCI D25 H — 150 — 25
XCI D24 H — 139 — 24
XCI D23 H — 138 — 23
XCI D22 H — 137 — 22
XCI D21 H — 136 — 21
XCI D20 H — 135 — 20
XCI D19 H — 134 — 19
XCI D18 H — 133 — 18
XCI D17 H — 132 — 17
XCI D16 H — 131 — 16
XCI D15 H — 130 — 15
XCI D14 H — 129 — 14
XCI D13 H — 128 — 13
XCI D12 H — 127 — 12
XCI D11 H — 126 — 11
XCI D10 H — 125 — 10
XCI D9 H — 122 — 09
XCI D8 H — 121 — 08
XCI D7 H — 120 — 07
XCI D6 H — 119 — 06
XCI D5 H — 118 — 05
XCI D4 H — 117 — 04
XCI D3 H — 116 — 03
XCI D2 H — 115 — 02
XCI D1 H — 114 — 01
XCI D0 H — 113 — 00
▽ XCID

XCI TCNF1 L
XCI TCNF0 L

TESTEN — 65 — ADAMS PULLUP H
IVIN — 66 — RGND 29 L
IVOUT — 67
XCNER — 94 — XCI CNF ERR L
▽ XTCNF — 82
XRCNF — 91 — XCI RCNF L
XCIC34 — 140 — XCI C34 H
XCIC45 — 141 — XCI C45 H
XCIC56 — 142 — XCI C56 H
XCIC61 — 143 — XCI C61 H
XGRANT — 93 — XCI GRANT L
XCMDR — 81 — XMI CMD REQ L
XRESRQ — 80 — XMI RES REQ L

XID 3 — 89 — XMI NODEID3 H
XID 2 — 88 — XMI NODEID2 H
XID 1 — 87 — XMI NODEID1 H
XID 0 — 86 — XMI NODEID0 H

XRESET — 76 — NODE RESET L
HDTOK — 69 — DXFER OK L
HDTNOK — 78 — DXFER BAD L
HRESET — 63 — CXHIC RESET L
HXHLT — 73 — HALT L

HDMARQ — 79 — DMA REQ L
HPERR — 77 — CXHIC PERR L
HMAR — 71 — MASK ACT REG L
HMES — 72 — MASK ERR SUM L
HWCLK — 52 — CLK 10MHZ H
HDCROS — 64 — PAGE XING H
HCLKSM — 68 — XIC BUSCLK H

HIBA 7 — 38 — CXHIC ADDR 7 H
HIBA 6 — 39 — CXHIC ADDR 6 H
HIBA 5 — 40 — CXHIC ADDR 5 H
HIBA 4 — 41 — CXHIC ADDR 4 H
HIBA 3 — 42 — CXHIC ADDR 3 H
HIBA 2 — 43 — CXHIC ADDR 2 H
HIBA 1 — 44 — CXHIC ADDR 1 H
HIBA 0 — 45 — CXHIC ADDR 0 H

HCS — 46 — II CS L
ES — 70 — XBE ERR SUM L
HRWEN — 54 — II RW H

HBM 3 — 55 — II BM 3 L
HBM 2 — 56 — II BM 2 L
HBM 1 — 57 — II BM 1 L
HBM 0 — 58 — II BM 0 L

HIBP 3 — 59 — II PAR 03 H
HIBP 2 — 60 — II PAR 02 H
HIBP 1 — 61 — II PAR 01 H
HIBP 0 — 62 — II PAR 00 H

HIBD 31 — 4 — II DATA 31 H
HIBD 30 — 5 — II DATA 30 H
HIBD 29 — 6 — II DATA 29 H
HIBD 28 — 7 — II DATA 28 H
HIBD 27 — 8 — II DATA 27 H
HIBD 26 — 9 — II DATA 26 H
HIBD 25 — 10 — II DATA 25 H
HIBD 24 — 11 — II DATA 24 H
HIBD 23 — 12 — II DATA 23 H
HIBD 22 — 13 — II DATA 22 H
HIBD 21 — 14 — II DATA 21 H
HIBD 20 — 15 — II DATA 20 H
HIBD 19 — 16 — II DATA 19 H
HIBD 18 — 17 — II DATA 18 H
HIBD 17 — 18 — II DATA 17 H
HIBD 16 — 19 — II DATA 16 H
HIBD 15 — 20 — II DATA 15 H
HIBD 14 — 21 — II DATA 14 H
HIBD 13 — 22 — II DATA 13 H
HIBD 12 — 23 — II DATA 12 H
HIBD 11 — 26 — II DATA 11 H
HIBD 10 — 27 — II DATA 10 H
HIBD 09 — 28 — II DATA 09 H
HIBD 08 — 29 — II DATA 08 H
HIBD 07 — 30 — II DATA 07 H
HIBD 06 — 31 — II DATA 06 H
HIBD 05 — 32 — II DATA 05 H
HIBD 04 — 33 — II DATA 04 H
HIBD 03 — 34 — II DATA 03 H
HIBD 02 — 35 — II DATA 02 H
HIBD 01 — 36 — II DATA 01 H
HIBD 00 — 37 — II DATA 00 H

CXHIC TO HIB L
HIB TO CXHIC L
RGND 27 L

CXHIC/HIB Data XCVRs

Byte 3

9-BIT TRNSCVR 29863 E6 PLCC

T8 — 18 — HIB DATA P3 H
R8 — 12
T7 — 19 — HIB DATA 31 H
R7 — 11
T6 — 20 — HIB DATA 30 H
R6 — 10
T5 — 21 — HIB DATA 29 H
R5 — 9
T4 — 23 — HIB DATA 28 H
R4 — 7
T3 — 24 — HIB DATA 27 H
R3 — 6
T2 — 25 — HIB DATA 26 H
R2 — 5
T1 — 26 — HIB DATA 25 H
R1 — 4
T0 — 27 — HIB DATA 24 H
R0 — 3

OET1 — 16 — R>T
OET2 — 17
OER1 — 2 — T>R
OER2 — 13

Byte 2

9-BIT TRNSCVR 29863 E7 PLCC

T8 — 18 — HIB DATA P2 H
R8 — 12
T7 — 19 — HIB DATA 23 H
R7 — 11
T6 — 20 — HIB DATA 22 H
R6 — 10
T5 — 21 — HIB DATA 21 H
R5 — 9
T4 — 23 — HIB DATA 20 H
R4 — 7
T3 — 24 — HIB DATA 19 H
R3 — 6
T2 — 25 — HIB DATA 18 H
R2 — 5
T1 — 26 — HIB DATA 17 H
R1 — 4
T0 — 27 — HIB DATA 16 H
R0 — 3

OET1 — 16 — R>T
OET2 — 17
OER1 — 2 — T>R
OER2 — 13

Byte 1

9-BIT TRNSCVR 29863 E3 PLCC

T8 — 18 — HIB DATA P1 H
R8 — 12
T7 — 19 — HIB DATA 15 H
R7 — 11
T6 — 20 — HIB DATA 14 H
R6 — 10
T5 — 21 — HIB DATA 13 H
R5 — 9
T4 — 23 — HIB DATA 12 H
R4 — 7
T3 — 24 — HIB DATA 11 H
R3 — 6
T2 — 25 — HIB DATA 10 H
R2 — 5
T1 — 26 — HIB DATA 09 H
R1 — 4
T0 — 27 — HIB DATA 08 H
R0 — 3

OET1 — 16 — R>T
OET2 — 17
OER1 — 2 — T>R
OER2 — 13

Byte 0

9-BIT TRNSCVR 29863 E17 PLCC

T8 — 18 — HIB DATA P0 H
R8 — 12
T7 — 19 — HIB DATA 07 H
R7 — 11
T6 — 20 — HIB DATA 06 H
R6 — 10
T5 — 21 — HIB DATA 05 H
R5 — 9
T4 — 23 — HIB DATA 04 H
R4 — 7
T3 — 24 — HIB DATA 03 H
R3 — 6
T2 — 25 — HIB DATA 02 H
R2 — 5
T1 — 26 — HIB DATA 01 H
R1 — 4
T0 — 27 — HIB DATA 00 H
R0 — 3

OET1 — 16 — R>T
OET2 — 17
OER1 — 2 — T>R
OER2 — 13

REVISIONS		
CHK	CHANGE NO.	REV

[HIB]

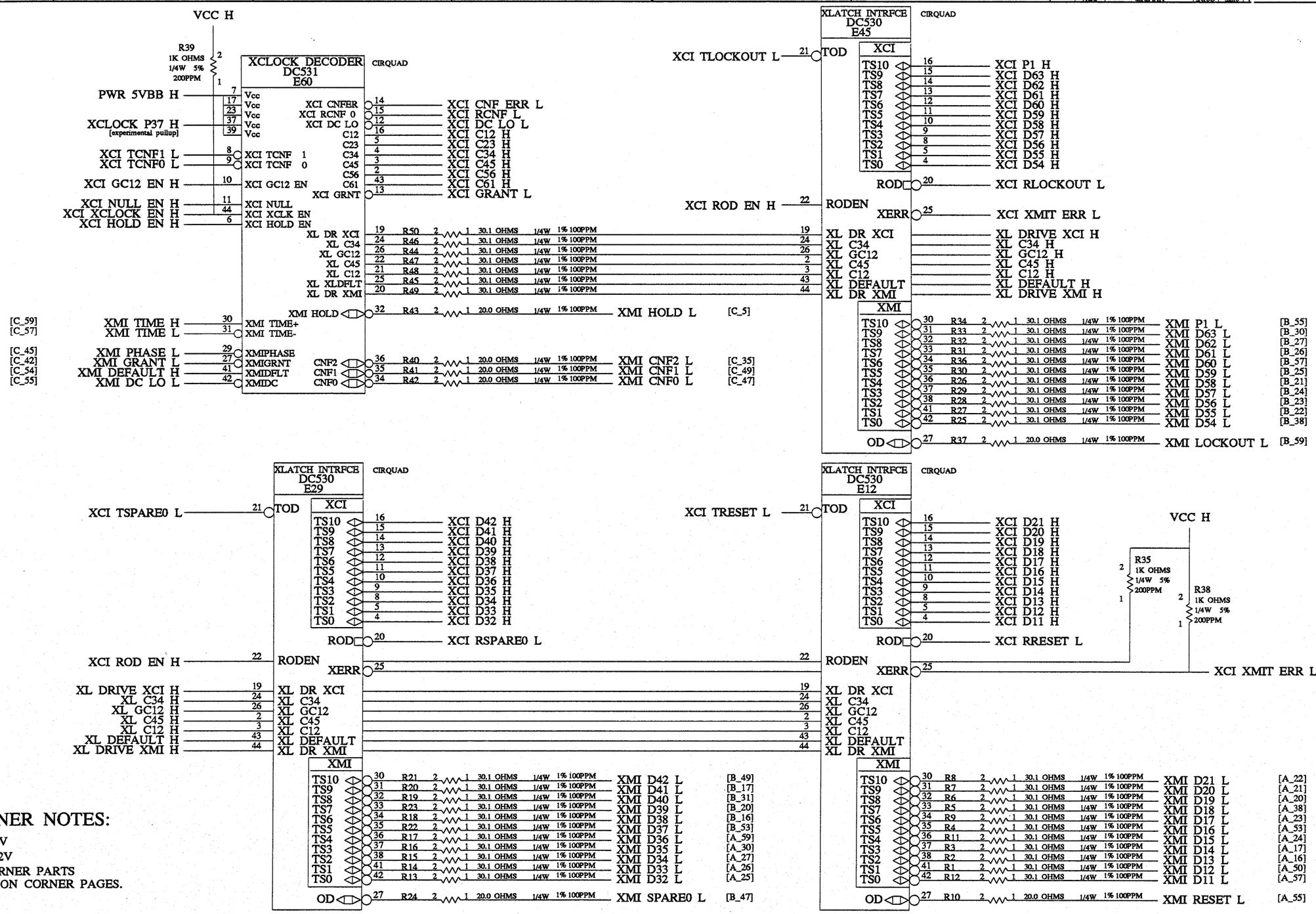
CXHIC,
CXHIC <-> HIB
DATA XCVRS

digital

DRN: K. Yesse	DATE -	ENG: T. Cxhic Adams	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
- Thu Oct 20 16:47:38 1988		SHEET 23	
FIRST USED ON OPTION/MODEL: -		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88



XMI CORNER NOTES:

1) VCC H = +5V
2) VEE H = -5.2V
3) NO NON-CORNER PARTS ALLOWED ON CORNER PAGES.

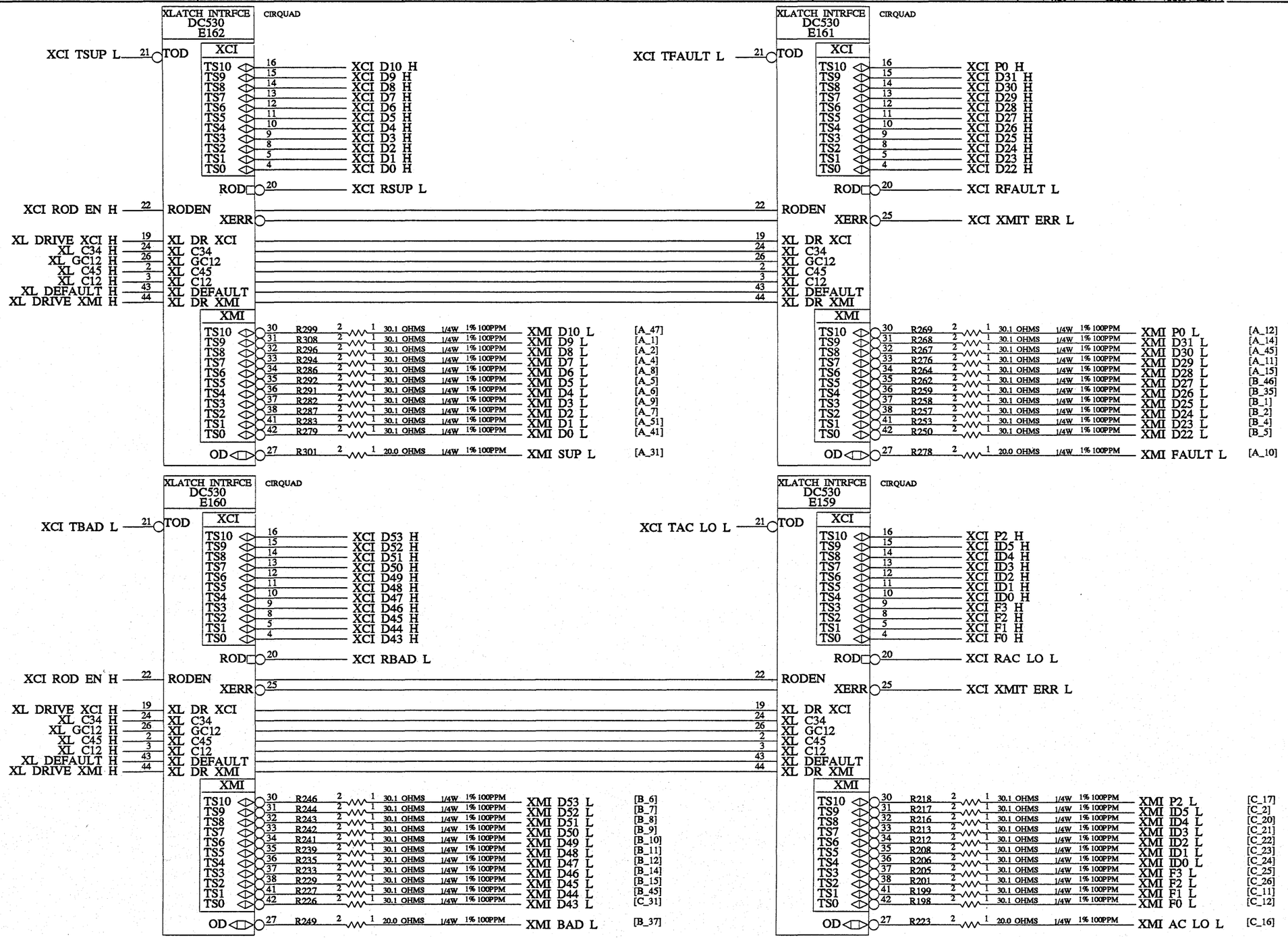
REVISIONS		
CHK	CHANGE NO.	REV

[XMI]
XMI CORNER

DRN: K. Yesse - DATE
CHK'D: - DATE
ENG: M. I. Real - DATE
BOARD LOCATION: CXO
SHEET 24
NEXT HIGHER ASSEMBLY: -
FIRST USED ON OPTION/MODEL: -
Thu Oct 20 16:48:48 1988

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88



REVISIONS		
CHK	CHANGE NO.	REV

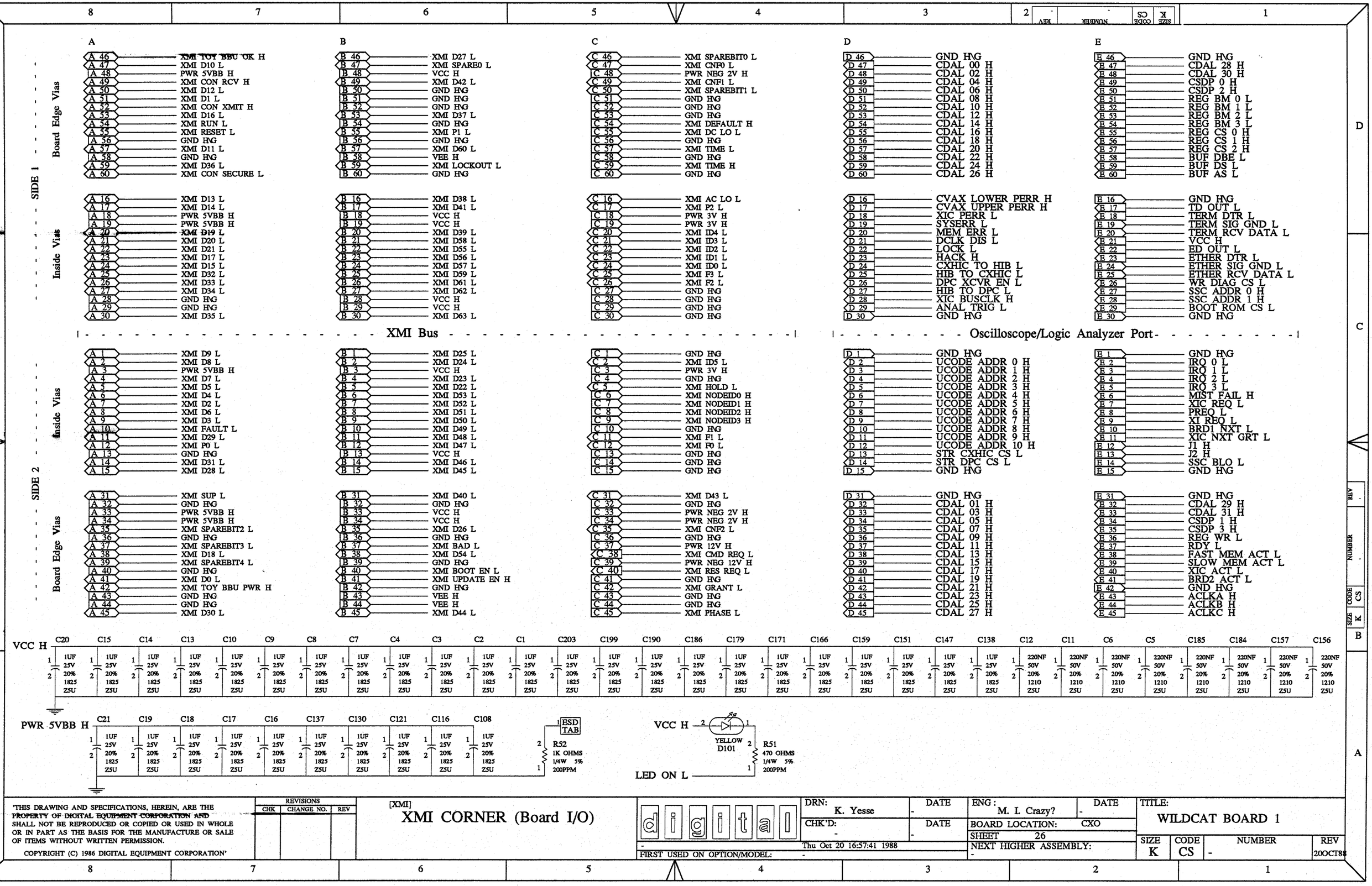
[XMI]

XMI CORNER

DRN: K. Yesse	DATE -	ENG: M. I. Memorex	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
- Thu Oct 20 16:49:46 1988		SHEET 25	
FIRST USED ON OPTION/MODEL: -		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88



REVISIONS		
CHK	CHANGE NO.	REV

[XMI]

XMI CORNER (Board I/O)

DRN: K. Yesse	DATE -	ENG: M. I. Crazy?	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
- Thu Oct 20 16:57:41 1988		SHEET 26	
FIRST USED ON OPTION/MODEL: -		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

SPACING = .100CC
MOUNT = 90D
HOUSING = SHROUD W/O LTCH
KEYING = NONE
CONFIG = STD
PINS = .022X.100G

BOARD COMPONENTS		J3 1	J3 2		BOARD EDGE
	GND HNG	1	2	SYSCLK H	/B_OUT
	GND HNG	3	4	BRD2 BUSCLK H	/B_OUT
	GND HNG	5	6	GND HNG	
/B_OUT	BRD2 EE CLK H	7	8	HIB DATA 00 H	/B_BI
/B_BI	HIB DATA 16 H	9	10	HIB DATA 01 H	/B_BI
/B_BI	HIB DATA 17 H	11	12	HIB DATA 02 H	/B_BI
/B_BI	HIB DATA 18 H	13	14	GND HNG	
/B_BI	HIB DATA 19 H	15	16	HIB DATA 03 H	/B_BI
/B_BI	HIB DATA 20 H	17	18	HIB DATA 04 H	/B_BI
/B_BI	HIB DATA 21 H	19	20	HIB DATA 05 H	/B_BI
/B_BI	HIB DATA 22 H	21	22	HIB DATA 06 H	/B_BI
/B_BI	HIB DATA 23 H	23	24	GND HNG	
/B_BI	HIB DATA 24 H	25	26	HIB DATA 07 H	/B_BI
/B_BI	HIB DATA 25 H	27	28	HIB DATA 08 H	/B_BI
/B_BI	HIB DATA 26 H	29	30	HIB DATA 09 H	/B_BI
/B_BI	HIB DATA 27 H	31	32	HIB DATA 10 H	/B_BI
/B_BI	HIB DATA 28 H	33	34	GND HNG	
/B_BI	HIB DATA 29 H	35	36	HIB DATA 11 H	/B_BI
/B_BI	HIB DATA 30 H	37	38	HIB DATA 12 H	/B_BI
/B_BI	HIB DATA 31 H	39	40	HIB DATA 13 H	/B_BI
/B_BI	HIB DATA P0 H	41	42	HIB DATA 14 H	/B_BI
/B_BI	HIB DATA P1 H	43	44	GND HNG	
/B_BI	HIB DATA P2 H	45	46	HIB DATA 15 H	/B_BI
/B_BI	HIB DATA P3 H	47	48	HIB ADDR 00 H	/B_OUT
/B_OUT	BRD2 EE DATA H	49	50	GND HNG	
/B_OUT	HIB ADDR 09 H	51	52	HIB ADDR 01 H	
/B_OUT	HIB ADDR 10 H	53	54	HIB ADDR 02 H	/B_OUT
/B_OUT	HIB ADDR 11 H	55	56	HIB ADDR 03 H	/B_OUT
/B_OUT	HIB ADDR 12 H	57	58	HIB ADDR 04 H	/B_OUT
/B_OUT	HIB ADDR 13 H	59	60	HIB ADDR 05 H	/B_OUT
/B_OUT	HIB ADDR 14 H	61	62	HIB ADDR 06 H	/B_OUT
/B_OUT	HIB ADDR 15 H	63	64	GND HNG	
/B_OUT	HIB ADDR 16 H	65	66	HIB ADDR 07 H	/B_OUT
/B_OUT	HIB ADDR 17 H	67	68	HIB ADDR 08 H	/B_OUT
/B_OUT	HIB ADDR HPAR H	69	70	HIB BM 0 L	/B_OUT
/B_OUT	HIB ADDR LPAR H	71	72	GND HNG	
/B_OUT	HIB SPARE 73 H	73	74	HIB BM 1 L	/B_OUT
/B_OUT	HIB SPARE 75 H	75	76	HIB BM 2 L	/B_OUT
/B_IN	HIB BUS ERR L	77	78	HIB BM 3 L	/B_OUT
/B_OUT	BRD2 EE WR H	79	80	HIB BRD2 CS L	/B_OUT
/B_OUT	HIB WR L	81	82	HIB CSICB CS L	/B_OUT
/B_OUT	HIB CSICA CS L	83	84	GND HNG	
/B_IN	BRD2 EE RD DATA H	85	86	HIB MSEL L	/B_OUT
/B_OUT	HIB CTRL PAR H	87	88	SIA INTRPT L	/B_IN
/B_IN	SIB INTRPT L	89	90	BRD2 RESET L	/B_OUT
/B_OUT	SIC B NXT GRANT L	91	92	SIC B BUS REQ L	/B_IN
/B_OUT	SIC A NXT GRANT L	93	94	GND HNG	
/B_OUT	XI NXT GRANT L	95	96	SIC A BUS REQ L	/B_IN
/B_OUT	PR NXT GRANT L	97	98	HIB SISM CS L	/B_OUT
	HIB SPARE 99 H	99	100	GND HNG	
		99	100		

NOTE: Connector pins have the property IO_DIRECTION set according to input/output/bidirectional status.

/B_OUT = from Board 1 to Board 2
/B_IN = from Board 2 to Board 1
/B_BI = Bidirectional signal

REVISIONS		
CHK	CHANGE NO.	REV

[HIB]
BOARD 1 <-> BOARD 2
HIB BUS CONNECTOR

digital

Thu Oct 20 16:58:11 1988

DRN: K. Yesse	DATE -	ENG: C. D. Light	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
FIRST USED ON OPTION/MODEL: -		SHEET 27	
		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

NOTE: Spare components shown here should generate a null Excess Spares List as shown in the PART LIST INFO section of the schematic.

Pullup Resistors

VCC H

R116	1K OHMS 1/4W 5% 200PPM	VCCR 1 H
R115	1K OHMS 1/4W 5% 200PPM	VCCR 2 H
R99	1K OHMS 1/4W 5% 200PPM	VCCR 3 H
R79	1K OHMS 1/4W 5% 200PPM	VCCR 4 H
R90	1K OHMS 1/4W 5% 200PPM	VCCR 5 H
R313	1K OHMS 1/4W 5% 200PPM	VCCR 6 H
R103	1K OHMS 1/4W 5% 200PPM	VCCR 7 H
R104	1K OHMS 1/4W 5% 200PPM	VCCR 8 H
R110	1K OHMS 1/4W 5% 200PPM	VCCR 9 H
R105	1K OHMS 1/4W 5% 200PPM	VCCR 10 H
R158	1K OHMS 1/4W 5% 200PPM	VCCR 11 H
R166	1K OHMS 1/4W 5% 200PPM	VCCR 12 H
R193	1K OHMS 1/4W 5% 200PPM	VCCR 13 H
R176	1K OHMS 1/4W 5% 200PPM	VCCR 14 H
R152	1K OHMS 1/4W 5% 200PPM	VCCR 15 H
R125	1K OHMS 1/4W 5% 200PPM	VCCR 16 H
R168	1K OHMS 1/4W 5% 200PPM	VCCR 17 H
R66	1K OHMS 1/4W 5% 200PPM	VCCR 18 H
R62	1K OHMS 1/4W 5% 200PPM	VCCR 19 H
R109	1K OHMS 1/4W 5% 200PPM	VCCR 20 H
R101	1K OHMS 1/4W 5% 200PPM	VCCR 21 H
R94	1K OHMS 1/4W 5% 200PPM	VCCR 22 H
R254	1K OHMS 1/4W 5% 200PPM	VCCR 23 H
R281	1K OHMS 1/4W 5% 200PPM	VCCR 24 H
R77	1K OHMS 1/4W 5% 200PPM	VCCR 25 H
R129	1K OHMS 1/4W 5% 200PPM	VCCR 26 H
R159	1K OHMS 1/4W 5% 200PPM	VCCR 27 H
R118	1K OHMS 1/4W 5% 200PPM	VCCR 28 H
R275	1K OHMS 1/4W 5% 200PPM	VCCR 29 H
R215	1K OHMS 1/4W 5% 200PPM	VCCR 30 H
R312	1K OHMS 1/4W 5% 200PPM	VCCR 31 H
R247	1K OHMS 1/4W 5% 200PPM	VCCR 32 H
R295	1K OHMS 1/4W 5% 200PPM	VCCR 33 H
R300	1K OHMS 1/4W 5% 200PPM	VCCR 34 H
R280	1K OHMS 1/4W 5% 200PPM	VCCR 35 H
R271	1K OHMS 1/4W 5% 200PPM	VCCR 36 H
R289	1K OHMS 1/4W 5% 200PPM	VCCR 37 H
R255	1K OHMS 1/4W 5% 200PPM	VCCR 38 H
R167	1K OHMS 1/4W 5% 200PPM	VCCR 39 H
R272	1K OHMS 1/4W 5% 200PPM	VCCR 40 H
R117	1K OHMS 1/4W 5% 200PPM	VCCR 41 H
R87	1K OHMS 1/4W 5% 200PPM	VCCR 42 H
R55	1K OHMS 1/4W 5% 200PPM	VCCR 43 H
R56	1K OHMS 1/4W 5% 200PPM	VCCR 44 H
R256	1K OHMS 1/4W 5% 200PPM	VCCR 45 H
R297	1K OHMS 1/4W 5% 200PPM	VCCR 46 H
R86	1K OHMS 1/4W 5% 200PPM	VCCR 47 H
R222	1K OHMS 1/4W 5% 200PPM	VCCR 48 H

R220	1K OHMS 1/4W 5% 200PPM	XCI TAC LO L
R274	1K OHMS 1/4W 5% 200PPM	XCI TFAULT L
R285	1K OHMS 1/4W 5% 200PPM	XCI TRESET L
R245	1K OHMS 1/4W 5% 200PPM	XCI TSPARE0 L
R302	1K OHMS 1/4W 5% 200PPM	XCI TSUP L
R54	1K OHMS 1/4W 5% 200PPM	SSC BLO L
R84	1K OHMS 1/4W 5% 200PPM	SYSRDY L
R88	1K OHMS 1/4W 5% 200PPM	SYSERR L
R72	1K OHMS 1/4W 5% 200PPM	RDY L
R85	1K OHMS 1/4W 5% 200PPM	ERR L
R120	1K OHMS 1/4W 5% 200PPM	DPE L
R80	1K OHMS 1/4W 5% 200PPM	IRQ 3 L
R83	1K OHMS 1/4W 5% 200PPM	IRQ 2 L
R93	1K OHMS 1/4W 5% 200PPM	IRQ 1 L
R95	1K OHMS 1/4W 5% 200PPM	IRQ 0 L
R171	1K OHMS 1/4W 5% 200PPM	HALT L
R228	1K OHMS 1/4W 5% 200PPM	SYNC DPC CS L
R230	1K OHMS 1/4W 5% 200PPM	SYNC CXHIC CS L
R248	1K OHMS 1/4W 5% 200PPM	SYNC XISM CS L
R71	1K OHMS 1/4W 5% 200PPM	SWITCH A H
R64	1K OHMS 1/4W 5% 200PPM	SWITCH B H
R100	1K OHMS 1/4W 5% 200PPM	CSDP 3 H
R97	1K OHMS 1/4W 5% 200PPM	CSDP 2 H
R89	1K OHMS 1/4W 5% 200PPM	CSDP 1 H
R82	1K OHMS 1/4W 5% 200PPM	CSDP 0 H

R252	1K OHMS 1/4W 5% 200PPM	HIB CSICA CS L
R240	1K OHMS 1/4W 5% 200PPM	HIB CSICB CS L
R261	1K OHMS 1/4W 5% 200PPM	HIB SISM CS L
R273	1K OHMS 1/4W 5% 200PPM	HIB BRD2 CS L
R238	1K OHMS 1/4W 5% 200PPM	HIB BM 3 L
R237	1K OHMS 1/4W 5% 200PPM	HIB BM 2 L
R231	1K OHMS 1/4W 5% 200PPM	HIB BM 1 L
R232	1K OHMS 1/4W 5% 200PPM	HIB BM 0 L
R219	1K OHMS 1/4W 5% 200PPM	HIB WR L
R263	1K OHMS 1/4W 5% 200PPM	HIB MSEL L
R57	1K OHMS 1/4W 5% 200PPM	ENT H
R149	1K OHMS 1/4W 5% 200PPM	J1 H
R160	1K OHMS 1/4W 5% 200PPM	J2 H
R221	1K OHMS 1/4W 5% 200PPM	XCLOCK P37 H
R270	1K OHMS 1/4W 5% 200PPM	ADAMS PULLUP H

TP6
TP5
TP4
TP3
TP2
TP1
TP0 — GND HG

GROUNDING POSTS
[Prototype build only]

Spare Components

R106 VCCR SP1 H
1K OHMS 1/4W 5% 200PPM

OCTAL DRIVER 74F240 E120 SOIC
D3 (11) Y3 (9)
D2 (13) Y2 (7)
D1 (15) Y1 (5)
D0 (17) Y0 (3)
EN (19)

R65 VCCR SP2 H
1K OHMS 1/4W 5% 200PPM

74F38 E153 SOIC (4, 5 → 6)
74F32 E130 SOIC (12, 13 → 11)

R210 VCCR SP3 H
1K OHMS 1/4W 200PPM

74F08 E62 SOIC (1, 2 → 3)
74F08 E61 SOIC (12, 13 → 11)

XE1 14 PIN SOIC SPARE
1+ 2+ 3+ 4+ 5+ 6+ 7+ | +14 +13 +12 +11 +10 +9 +8

Pulldown Resistors

GND HG

R306	100 OHMS 1/4W 5% 200PPM	RGND 8 L
R107	100 OHMS 1/4W 5% 200PPM	RGND 7 L
R102	100 OHMS 1/4W 5% 200PPM	RGND 6 L
R60	100 OHMS 1/4W 5% 200PPM	RGND 5 L
R108	100 OHMS 1/4W 5% 200PPM	RGND 4 L
R304	100 OHMS 1/4W 5% 200PPM	RGND 3 L
R124	100 OHMS 1/4W 5% 200PPM	RGND 2 L
R61	100 OHMS 1/4W 5% 200PPM	RGND 1 L
R251	100 OHMS 1/4W 5% 200PPM	RGND 16 L
R96	100 OHMS 1/4W 5% 200PPM	RGND 15 L
R284	100 OHMS 1/4W 5% 200PPM	RGND 14 L
R59	100 OHMS 1/4W 5% 200PPM	RGND 13 L
R130	100 OHMS 1/4W 5% 200PPM	RGND 12 L
R111	100 OHMS 1/4W 5% 200PPM	RGND 11 L
R92	100 OHMS 1/4W 5% 200PPM	RGND 10 L
R134	100 OHMS 1/4W 5% 200PPM	RGND 9 L
R224	100 OHMS 1/4W 5% 200PPM	RGND 24 L
R290	100 OHMS 1/4W 5% 200PPM	RGND 23 L
R265	100 OHMS 1/4W 5% 200PPM	RGND 22 L
R277	100 OHMS 1/4W 5% 200PPM	RGND 21 L
R234	100 OHMS 1/4W 5% 200PPM	RGND 20 L
R98	100 OHMS 1/4W 5% 200PPM	RGND 19 L
R293	100 OHMS 1/4W 5% 200PPM	RGND 18 L
R298	100 OHMS 1/4W 5% 200PPM	RGND 17 L
R156	100 OHMS 1/4W 5% 200PPM	RGND 32 L
R236	100 OHMS 1/4W 5% 200PPM	RGND 31 L
R260	100 OHMS 1/4W 5% 200PPM	RGND 30 L
R266	100 OHMS 1/4W 5% 200PPM	RGND 29 L
R309	100 OHMS 1/4W 5% 200PPM	RGND 28 L
R303	100 OHMS 1/4W 5% 200PPM	RGND 27 L
R225	100 OHMS 1/4W 5% 200PPM	RGND 26 L
R307	100 OHMS 1/4W 5% 200PPM	RGND 25 L
R214	100 OHMS 1/4W 5% 200PPM	XCI NULL EN H
R311	100 OHMS 1/4W 5% 200PPM	RGND 38 L
R53	100 OHMS 1/4W 5% 200PPM	RGND 37 L
R310	100 OHMS 1/4W 5% 200PPM	RGND 36 L
R305	100 OHMS 1/4W 5% 200PPM	RGND 35 L
R288	100 OHMS 1/4W 5% 200PPM	RGND 34 L
R81	100 OHMS 1/4W 5% 200PPM	RGND 33 L

NOTE: GND H (Global) is used by all ground symbols, and implicitly by ICs in their ground connections. RGND x L pulldowns employ the opposite assertion sense.

REVISIONS

CHK	CHANGE NO.	REV

[Common Logic]

PULLUP & PULLDOWN RESISTORS, SPARE COMPONENTS

digital

DRN: K. Yesse	DATE -	ENG: K. Olsen	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
		SHEET 28	
- Thu Oct 20 17:00:57 1988		NEXT HIGHER ASSEMBLY: -	
FIRST USED ON OPTION/MODEL: -			

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

VCC H

C198	C189	C183	C169	C164	C163	C161	C176	C197	C140	C155	C95	C24	C86	C162	C204	C175	C196	C154	C153	C94	C25	C124	C114	C191
C182	C170	C143	C81	C33	C110	C135	C89	C200	C172	C136	C139	C80	C43	C101	C126	C53	C40	C152	C144	C131	C61	C35	C195	C118
C72	C23	C92	C111	C44	C54	C106	C105	C60	C71	C48	C99	C109	C26	C64	C123	C104	C79	C59	C32	C47	C31	C39	C127	C115
C93	C22	C63	C141	C122	C78	C75	C133	C85	C27	C100	C77	C34	C128	C91	C66	C70	C52	C41	C202	C83	C107	C149	C145	C192
C37	C55	C88	C117	C62	C132	C65	C148	C38	C51	C56	C87	C112	C173	C150	C187	C98	C30	C50	C74	C90	C113	C177	C158	C125
C29	C49	C73	C96	C119	C188	C142	C193	C58	C28	C69	C76	C97	C120	C165	C160	C167	C168	C36	C68	C84	C103	C129	C194	C180
C201	C174	C67	C82	C102	C146	C134	C178	C181	C205															

All capacitors: .01UF 20% 50V CERAMIC Z5U

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REVISIONS

CHK	CHANGE NO.	REV

[Common Logic]

DECOUPLING CAPACITORS

digital

FIRST USED ON OPTION/MODEL: -

DRN: K. Yesse	DATE -	ENG: Your Name Here	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
Thu Oct 20 17:04:03 1988		SHEET 29	
		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

File: 16R8DSL_ARBIT.PLD
Source: DISK$HSBSIM_B:[SIMULATION.CMS]

```
Name          ARBIT;
Partno        xxxxx;
Date          8/25/88;
Revision      A3;
Designer      Richie;
Company       DEC;
Assembly      Wildass;
Location      e96;
Device        P16R8;
|
/*************************************************************/
/*                                                           */
/*          BUS ARBITER                                      */
/*                                                           */
/*************************************************************/
/*  Allowable Target Device Types:     16R8D                 */
/*************************************************************/
|
/* 8/25/88 -  added xic perr l to inputs for disabling xi nxt grant
              when a parity error occurs */
|
/**  Inputs  **/
|
Pin  1 = bus_clk;                  /* inverted > mid phase transition*/
Pin  4 = !xic_perr_l;              /* xic parity error              */
Pin  5 = !xic_req_l;               /* proc to xic bus request       */
Pin  6 = !preq_l;                  /* processor bus request         */
Pin  7 = !xi_req_l;                /* xic bus request               */
Pin  8 = !sic_a_bus_req_l;         /*                               */
Pin  9 = !sic_b_bus_req_l;         /*                               */
Pin 11 = !oe;                      /*                               */
|
/**  Outputs  **/
Pin 15 = !xic_nxt_grant_l;
Pin 16 = !sic_b_nxt_bus_grant_l;/* bus grants - all active low     */
Pin 17 = !sic_a_nxt_bus_grant_l;/*                                 */
Pin 18 = !xi_nxt_bus_grant_l;  /*                                  */
Pin 19 = !proc_nxt_grant_l;    /*                                  */
                               /* the following are used for      */
                               /* state information (active hi) */
Pin 12 = !sisel_l;             /* si selector - shows which SI    */
                               /* will get the bus next if both   */
                               /* SI channels request it          */
Pin 13 = !silast_l;            /* set if one of the SI's got the */
                               /* bus on the last cycle           */
Pin 14 = !xilast_l;            /* set if xiC got the bus on the   */
                               /* last cycle                      */
|
|
/**  Logic Equations  **/
|
|
/* IF ! sys_clock_H THEN BEGIN
|
/*++
/*
/* Equations:
/*
/*   Give the xi the bus if he wants it and the CVAX doesn't and:
/*      a)    Neither SI wants it and the xi didn't have it last cycle, or
/*      b)    Only one of the SI's wants it but he got it last cycle.
/*
/*--                                                          */
|
xic_nxt_grant_l.d = xic_req_l;          /* always let cvax have board1 bus, si
                                           sisms can't get here so no conflict */
|
xi_nxt_bus_grant_l.d =
       xi_req_l & !sic_a_bus_req_l & !sic_b_bus_req_l &
       !preq_l & !xilast_l & !xic_req_l & !xic_perr_l
     # xi_req_l & !sic_a_bus_req_l & sic_b_bus_req_l &
       silast_l & !sisel_l & !preq_l & !xic_req_l & !xic_perr_l
     # xi_req_l & sic_a_bus_req_l & !sic_b_bus_req_l &
       silast_l & sisel_l & !preq_l & !xic_req_l & !xic_perr_l;
|
/*++
/*      Give the uVAX the bus if he wants it and:
/*      a)    Neither SI wants it, or
/*      b)    Only one of the SI's wants it but he got it last cycle.
/*
/*--                                                          */
|
proc_nxt_grant_l.d =
```

16R8DSL_ARBIT.PLD continued..

```
       preq_l & !sic_a_bus_req_l & !sic_b_bus_req_l & !xic_req_l
     # preq_l & !sic_a_bus_req_l & sic_b_bus_req_l & silast_l & !sisel_l & !xic_req_l
     # preq_l & sic_a_bus_req_l & !sic_b_bus_req_l & silast_l & sisel_l & !xic_req_l;
|
/*++
/* Give the bus to SI A if he wants it and didn't get it last cycle and:
/*      a)    SI B doesn't want it, or
/*      b)    SI B wants it too but its SI A's turn due to fairness
/*
/*      The long form of the following equation is:
/*      (! sic_a_bus_req_l & sic_b_bus_req_l & ! (silast_l & sisel_l))
/*   #  (! sic_a_bus_req_l & ! sic_b_bus_req_l & ! sisel_l)
/*--                                                          */
|
sic_a_nxt_bus_grant_l.d =
       sic_a_bus_req_l & !sic_b_bus_req_l & !silast_l
     # sic_a_bus_req_l & !sisel_l;
|
/*++
/* Give the bus to SI B if he wants it and didn't get it last cycle and:
/*      a)    SI A doesn't want it, or
/*      b)    SI A wants it too but its SI B's turn due to fairness
/*
/*      The long form of the following equation is:
/*      (! sic_a_bus_req_l & sic_b_bus_req_l & ! (silast_l & ! sisel_l))
/*    # (! sic_a_bus_req_l & ! sic_b_bus_req_l & sisel_l)
/*--                                                          */
|
|
sic_b_nxt_bus_grant_l.d =
       sic_b_bus_req_l & !sic_a_bus_req_l & !silast_l
     # sic_b_bus_req_l & sisel_l;
|
|
/*++
/*      Set SILAST and xiLAST;
/*--                                                          */
|
silast_l.d = sic_a_bus_req_l & !sic_b_bus_req_l & !silast_l
           # sic_b_bus_req_l & !sic_a_bus_req_l & !silast_l
           # sic_a_bus_req_l & !sisel_l
           # sic_b_bus_req_l & sisel_l;
|
|
xilast_l.d = xi_req_l & !sic_a_bus_req_l & !sic_b_bus_req_l & !preq_l & !xilast_l & !xic_req_l
           # xi_req_l & !sic_a_bus_req_l & sic_b_bus_req_l & silast_l
                & !sisel_l & !preq_l & !xic_req_l
           # xi_req_l & sic_a_bus_req_l & !sic_b_bus_req_l & silast_l
                & sisel_l & !preq_l & !xic_req_l;
|
|
/*++
/*      If neither SI wanted the bus don't change SISEL, otherwise
/*      set SISEL to the index of the SI who deserves the bus next.
/*      This means that if an SI got the bus set SISEL to the other SI,
/*      and if an SI was denied the bus set SISEL to that SI.
/*
/*      The long form of the next equation is:
/*      ! sic_b_bus_req_l & ! sic_a_bus_req_l & ! sisel_l
/*    # ! sic_b_bus_req_l & sic_a_bus_req_l & (silast_l & ! sisel_l)
/*    # sic_b_bus_req_l & ! sic_a_bus_req_l & ! (silast_l & sisel_l)
/*    # sic_b_bus_req_l & sic_a_bus_req_l & sisel_l
/*--                                                          */
|
sisel_l.d = !sic_b_bus_req_l & sic_a_bus_req_l & !silast_l
          # sic_b_bus_req_l & silast_l & !sisel_l
          # sic_a_bus_req_l & !sisel_l
          # !sic_a_bus_req_l & !sic_b_bus_req_l & sisel_l;
```


REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]
PAL EQN FILES:
16R8DSL_ARBIT.PLD

digital

DRN: K. Yesse	-	DATE	-
CHK'D: -	-	DATE	-
-	Thu Oct 20 17:04:42 1988		
FIRST USED ON OPTION/MODEL:	-		

ENG: W. Chewbacca	-	DATE	-
BOARD LOCATION:	CXO		
SHEET	30		
NEXT HIGHER ASSEMBLY:	-		

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

File: 16R8DSL_IIADD.PLD
Source: DISK$HSBSIM_B:[SIMULATION.CMS]

```
NAME          IIADD;
PARTNO        16R8D;
REVISION      03;
DATE          8/22/88;
DESIGNER      Versace;
COMPANY       DEC;
ASSEMBLY      HSX50 BOARD 1;
LOCATION      E115;
DEVICE        P16R8;

/*************************************************************************/
/*                                                                       */
/*  HSX50 BOARD 1 PAL: Cvax XIC Address Translation                      */
/*                                                                       */
/*  REVISION HISTORY:                                                    */
/*    4/28/87   KY/DV   Verified correct pinout & functionality          */
/*    5/12/87   KY      Horrors! Took gen. 4, added comments             */
/*                        (threw away gen. 5, bad I/O)                   */
/*    7/19/88   DV      Added caddr07 to an output pin.                  */
/*    8/22/88   DV/MW   make signal names and pal names compatable       */
/*************************************************************************/

/**  INPUTS  **/

pin 1  = HACK_H;
pin 2  = !CXHIC_CS_L;
pin 3  = CADDR_08_H;
pin 4  = CADDR_07_H;
pin 5  = CADDR_06_H;
pin 6  = CADDR_05_H;
pin 7  = CADDR_04_H;
pin 8  = CADDR_03_H;
pin 9  = CADDR_02_H;
pin 11 = !XIC_NXT_GRT_L;

/**  OUTPUTS  **/

pin 12 = CVAX_II_ADDR_0_H;
pin 13 = CVAX_II_ADDR_1_H;
pin 14 = CVAX_II_ADDR_2_H;
pin 15 = CVAX_II_ADDR_3_H;
pin 16 = CVAX_II_ADDR_4_H;
pin 17 = CVAX_II_ADDR_5_H;
pin 18 = CVAX_II_ADDR_6_H;
pin 19 = CVAX_II_ADDR_7_H;

/*  The cxhic is longword addressable. The dpc is byte addressable. */
/*  This pal zero fills the lower 2 iiaddr lines for cvax to cxhic operations */
/*  and right shifts 2 bits for cvax to dpc operations.  */

/**  LOGIC EQUATIONS  **/

CVAX_II_ADDR_0_H.D = !CXHIC_CS_L &      /*  not assd  */
                     CADDR_02_H;        /*  asserted  */

CVAX_II_ADDR_1_H.D = !CXHIC_CS_L &      /*  not assd  */
                     CADDR_03_H;        /*  asserted  */

CVAX_II_ADDR_2_H.D = !CXHIC_CS_L &      /*  not assd  */
                     CADDR_04_H         /*  asserted  */
                   # CXHIC_CS_L &       /*  asserted  */
                     CADDR_02_H;        /*  asserted  */

CVAX_II_ADDR_3_H.D = !CXHIC_CS_L &      /*  not assd  */
                     CADDR_05_H         /*  asserted  */
                   # CXHIC_CS_L &       /*  asserted  */
                     CADDR_03_H;        /*  asserted  */

CVAX_II_ADDR_4_H.D = !CXHIC_CS_L &      /*  not assd  */
                     CADDR_06_H         /*  asserted  */
                   # CXHIC_CS_L &       /*  asserted  */
                     CADDR_04_H;        /*  asserted  */

CVAX_II_ADDR_5_H.D = !CXHIC_CS_L &      /*  not assd  */
                     CADDR_07_H         /*  asserted  */
                   # CXHIC_CS_L &       /*  asserted  */
                     CADDR_05_H;        /*  asserted  */

CVAX_II_ADDR_6_H.D = !CXHIC_CS_L &      /*  not assd  */
                     CADDR_08_H         /*  asserted  */
                   # CXHIC_CS_L &       /*  asserted  */
                     CADDR_06_H;        /*  asserted  */
```

16R8DSL_IIADD.PLD continued..

```
CVAX_II_ADDR_7_H.D = CADDR_07_H;        /*  asserted  */
```


REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]
PAL EQN FILES:
16R8DSL_IIADD.PLD

digital

DRN: K. Yesse	DATE -	ENG: W. Chewbacca	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
- Thu Oct 20 17:04:49 1988		SHEET 31	
FIRST USED ON OPTION/MODEL: -		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

File: 20L8BSL_BOGEY.PLD
Source: DISK$HSBSIM_B:[SIMULATION.CMS]

```
NAME          BOGEY
PARTNO        xxxxx;
REVISION      01;
DATE          9/07/88;
DESIGNER      Versace;
COMPANY       DEC;
ASSEMBLY      Wildcat;
LOCATION      E119;
DEVICE        P20L8;
FORMAT        -jf;

/*************************************************************/
/*      This is the HIB Bus pal.                             */
/*************************************************************/

/* 9/7/88 - modified hib reg clk ena to include processor to xism transfers */


/**  INPUTS  **/

pin 1  = XIC_NXT_GRT_L;          /* plcc pin1   */
pin 2  = XIC_PERR_L;             /* plcc pin2   */
pin 3  = BRD1_NXT_L;             /* plcc pin3   */
pin 4  = PGRANT_L;               /* plcc pin4   */
pin 5  = HIB_REG_CS_L;           /* plcc pin6   */
pin 6  = BUSCLK_L;               /* plcc pin7   */
pin 7  = XIC_GRANT_L;            /* plcc pin9   */
pin 8  = STR_XISM_CS_L;          /* plcc pin10  */
pin 9  = DPC_XCVR_EN_L;          /* plcc pin12  */
pin 10 = HIB_TO_DPC_L;           /* plcc pin13  */
pin 11 = STR_WR_L;               /* plcc pin14  */
pin 13 = SPARE16;                /* plcc pin16  */
pin 14 = SPARE17;                /* plcc pin17  */
pin 23 = VCCR_46;                /* plcc pin27  */

/**  OUTPUTS  **/

pin 15 = !HIB_REG_CLKEN_L;       /* plcc pin18  */
pin 16 = !GEN_PAR_L;             /* plcc pin20  */
pin 17 = !UCODE_WREN_L;          /* plcc pin21  */
pin 18 = SPARE18;                /* plcc pin22  */
pin 19 = SPARE19;                /* plcc pin23  */
pin 20 = SPARE20;                /* plcc pin24  */
pin 21 = SPARE21;                /* plcc pin25  */
pin 22 = !HIB_REG_OEN_L;         /* plcc pin26  */


/**  LOGIC EQUATIONS  **/

HIB_REG_OEN_L    = !HIB_REG_CS_L &       /* Asserted - during reads maintained */
                                         /* until cycle completion  */
                    STR_WR_L &           /* NOT Asserted - performing read */
                   !PGRANT_L;            /* Asserted - avoid bus contention */
                                         /* with XISM       */

HIB_REG_OEN_L.OE = VCCR_46;              /* For ICT: if = high then TTL    */
                                         /*          if = low then tristate */


HIB_REG_CLKEN_L = !BRD1_NXT_L &          /* Asst - either Proc. or XISM bus cycle */
                   HIB_REG_CS_L &        /* not asst. - therefore not reading reg */
                   XIC_PERR_L            /* not asst. - this error will disable   */
                                         /* further updating of reg until cleared */
                    #
                   !XIC_NXT_GRT_L &      /* Asst - processor to xism bus cycle */
                   HIB_REG_CS_L &        /* not asst. - therefore not reading reg */
                   XIC_PERR_L;           /* not asst. - this error will disable   */
                                         /* further updating of reg until cleared */

HIB_REG_CLKEN_L.OE  = VCCR_46;


GEN_PAR_L        = HIB_TO_DPC_L &        /* not asst. thus DPC Write to HIB */
                  !DPC_XCVR_EN_L;        /* Asst. -- some kind of DPC activity */

GEN_PAR_L.OE     = VCCR_46;


UCODE_WREN_L     = !STR_XISM_CS_L &      /* Asst.- accessing ucode SRAMs */
                  !XIC_GRANT_L &         /* asst.- CVAX granted the HIB Bus */
                  !STR_WR_L &            /* performing write operation */
                   BUSCLK_L;             /* when Buscik L is high -- 2nd half */
                                         /* of bus grant cycle    */
```

20L8BSL_BOGEY.PLD continued..

```
UCODE_WREN_L.OE = VCCR_46;
```


REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]
PAL EQN FILES:
20L8BSL_BOGEY.PLD

digital

DRN: K. Yesse	DATE -	ENG: W. Chewbacca	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
- Thu Oct 20 17:04:56 1988		SHEET 32	
FIRST USED ON OPTION/MODEL: -		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

File: 20L8BSL_CV2HB.PLD
Source: DISK$HSBSIM_B:[SIMULATION.CMS]

```
NAME          CV2HB;
PARTNO        xxxxx;
REVISION      01;
DATE          8/22/88;
DESIGNER      Versace;
COMPANY       DEC;
ASSEMBLY      Wildcat;
LOCATION      E107;
DEVICE        P20L8;
FORMAT        -jf;

/*****************************************************************/
/*  CVAX-HIB DATA CONTROL PAL                                    */
/*****************************************************************/

/*************  REVISION HISTORY **************/

/* 8-22-88 added vcer 45 h to provide in ckt test w/tri-state capability */

/**  INPUTS  **/

pin 1  = spare1;              /* plcc pin1   */
pin 2  = BUF_AS_L;            /* plcc pin2   */
pin 3  = REG_WR_L;            /* plcc pin3   */
pin 4  = STR_WR_L;            /* plcc pin4   */
pin 5  = PGRANT_L;            /* plcc pin6   */
pin 6  = XIC_GRANT_L;         /* plcc pin7   */
pin 7  = BUSCLK;              /* plcc pin9   */
pin 8  = ACLKC;               /* plcc pin10  */
pin 9  = HACK;                /* plcc pin12  */
pin 10 = SPARE10;             /* plcc pin13  */
pin 11 = SPARE11;             /* plcc pin14  */
pin 13 = SPARE13;             /* plcc pin16  */
pin 14 = SPARE14;             /* plcc pin17  */
pin 23 = VCCR_45;             /* plcc pin27  */

/**  OUTPUTS  **/

pin 15 = HIB_DIR;             /* plcc pin18  */
pin 16 = spare16;             /* plcc pin20  */
pin 17 = dave_clock;          /* plcc pin21  */
pin 18 = SAB;                 /* plcc pin22  */
pin 19 = CAB;                 /* plcc pin23  */
pin 20 = SBA;                 /* plcc pin24  */
pin 21 = CBA;                 /* plcc pin25  */
pin 22 = !HIB_XCVR_EN_L;      /* plcc pin26  */

/** LOGIC VARIABLES **/

/**  LOGIC EQUATIONS  **/

        /* CVAX read of HIB or XIC */

SBA         = HACK &                  /* HIB or XIC operation w/o lock */
              REG_WR_L &              /* CVAX read */
              CBA;                    /* data is latched in 646 from HIB */
                                      /* ready to output */

SBA.OE      = VCCR_45;                /* if vccr 45 = high then TTL */
                                      /* if vccr 45 = low then tristate */

dave_clock  = !BUSCLK &               /* when low - last 100ns of cycle */
              !ACLKC;                 /* when low - last 50ns of cycle */

dave_clock.OE = VCCR_45;

/* clocks in HIB data then feedback keeps asserted until end  */
/* so as to help maintain asserted HIB DIR signal for READY pal */

CBA         = STR_WR_L &              /* this read goes away after grant */
                                      /* and REG_WR doesn't */
              !PGRANT_L &             /* asserted */
              dave_clock              /* 0 -> 1 asserted CBA */
                #
              STR_WR_L &              /* maintained during HIB data cycle only */
              !XIC_GRANT_L &          /* asserted */
              dave_clock              /* 0 -> 1 asserted CBA */
                #
              CBA & !BUF_AS_L;        /* latched until BUF AS deasserts */

CBA.OE      = VCCR_45;

/* NOTE: If HACK occurs prior to 150, may have to qualify or possibly */
```

20L8BSL_CV2HB.PLD continued..

```
/* use WR DIAG CLK instead */

CAB         = !REG_WR_L &             /* asserted - doing CVAX write */
              HACK &                  /* asserted - bd2 or XICACT w/o lock */
              ACLKC;                  /* occures @200 - so plenty of set up */
                                      /* for parity */
CAB.OE      = VCCR_45;


SAB         = !PGRANT_L & !STR_WR_L   /* transfer stored CVAX data to HIB */
                #
              !XIC_GRANT_L & !STR_WR_L;

SAB.OE      = VCCR_45;


HIB_DIR     = !SBA;                   /* inverted SBA */

HIB_DIR.OE  = VCCR_45;                /* for ict */

/* If SBA deasserted low and SAB deasserted low then HIB XCVR ENA L = high */
/* else HIB XCVR EN L = low  -- nor functionality */

HIB_XCVR_EN_L =  SBA # SAB;

HIB_XCVR_EN_L.OE = VCCR_45;           /* for ict */
```


REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]
PAL EQN FILES:
20L8BSL_CV2HB.PLD

digital

DRN: K. Yesse	DATE -	ENG: W. Chewbacca	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
- Thu Oct 20 17:05:02 1988		SHEET 33	
FIRST USED ON OPTION/MODEL: -		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

File: 20L8BSL_DCTRL.PLD
Source: DISK$HSBSIM_B:[SIMULATION.CMS]

```
NAME            dctrl;
PARTNO          xxxxx;
REVISION        03;
DATE            9/26/88;
DESIGNER        Versace;
COMPANY         DEC;
ASSEMBLY        Wildcat;
LOCATION        E57;
DEVICE          P20L8;
FORMAT          -jf;
|
/*************************************************/
/* Wildcat Board 1 pal:  CVAX Data Control pal    */
/*                                                */
/* REVISION HISTORY:                              */
/*                                                */
/* 4/25/88 add two pins, wr diag csl & cvax par fec H,
   to allow the DPEL signal to be asserted when the WR
   DIAG reg is read and the cvax par fec line is asserted.
                        - mr. rick */
|
/* 5/2/88 add byte mask lines and perr lines from 286s to
          generate cvax perr H  - mr rick */
|
/* 6/24/88 created word wide cvax parity errors. */
|
/* 8/22/88  check parity for all board2 reads */
|
/* 9/21/88 removed HIB REG CS from pal since it's not  */
/*          parity protected                          */
|
/* 9/26/88 duh -- added HIB REG CS back in cause it was */
/*          supposed to be used as a qualifier for DPE  */
/*          and ERR ENA during BRD2 ACT assertions      */
|
/*************************************************/
|
/**  INPUTS  **/
|
pin 1  = FAST_MEM_ACT_L;        /* plcc pin1   */
pin 2  = XIC_ACT_L;             /* plcc pin2   */
pin 3  = HIB_REG_CS_L;          /* plcc pin3   */
pin 4  = BRD2_ACT_L;            /* plcc pin4   */
pin 5  = spare5;                /* plcc pin6   */
pin 6  = CVAX_DPE_DIS_L;        /* plcc pin7   */
pin 7  = REG_WR_L;              /* plcc pin9   */
pin 8  = WR_DIAG_CS_L;          /* plcc pin10  */
pin 9  = CVAX_PAR_FEC_H;        /* plcc pin12  */
pin 10 = REG_BM0_L;             /* plcc pin13  */
pin 11 = REG_BM1_L;             /* plcc pin14  */
pin 13 = REG_BM2_L;             /* plcc pin16  */
pin 14 = REG_BM3_L;             /* plcc pin17  */
pin 16 = PERR_0_L;              /* plcc pin20  */
pin 17 = PERR_1_L;              /* plcc pin21  */
pin 18 = PERR_2_L;              /* plcc pin22  */
pin 19 = PERR_3_L;              /* plcc pin23  */
pin 23 = VCCR_41;               /* plcc pin27  */
|
/**  OUTPUTS  **/
|
pin 15 = CVAX_LOWER_PERR;       /* plcc pin18  */
pin 20 = !ERR_ENA_L;            /* plcc pin24  */
pin 21 = !DPE_L;                /* plcc pin25  */
pin 22 = CVAX_UPPER_PERR;       /* plcc pin26  */
|
/** LOGIC VARIABLES **/
|
/**  LOGIC EQUATIONS  **/
|
/* allow cvax parity error detection */
|
DPE_L = !FAST_MEM_ACT_L &  CVAX_DPE_DIS_L & REG_WR_L
        #
        !XIC_ACT_L  &  CVAX_DPE_DIS_L & REG_WR_L
        #
        !BRD2_ACT_L &  CVAX_DPE_DIS_L & REG_WR_L & HIB_REG_CS_L
        #
        !WR_DIAG_CS_L &  CVAX_DPE_DIS_L & CVAX_PAR_FEC_H & REG_WR_L;
|
DPE_L.OE = REG_WR_L;    /* only drive dpel when a read occurs */
|
/* The next two circuits will assert cvax perr whenever a byte has */
/* bad parity and the corresponding byte mask is asserted, and we */
```

20L8BSL_DCTRL.PLD continued..

```
/* are error enabled. */
|
CVAX_LOWER_PERR = !REG_BM0_L & !PERR_0_L & ERR_ENA_L
                  #
                  !REG_BM1_L & !PERR_1_L & ERR_ENA_L;
|
CVAX_LOWER_PERR.OE = VCCR_41;
|
CVAX_UPPER_PERR = !REG_BM2_L & !PERR_2_L & ERR_ENA_L
                  #
                  !REG_BM3_L & !PERR_3_L & ERR_ENA_L;
|
CVAX_UPPER_PERR.OE = VCCR_41;
|
/* Error Enable was created for Diagnostic test purposes. It allows for */
/* CVAX parity error detection by the hardware w/o the CVAX internally */
/* seeing the parity error.  */
|
ERR_ENA_L       = !FAST_MEM_ACT_L &  REG_WR_L       /* reads from any parity */
                    #                               /* protected medium */
                  !XIC_ACT_L  &  REG_WR_L
                    #
                  !BRD2_ACT_L &  REG_WR_L & HIB_REG_CS_L
                    #
                  !WR_DIAG_CS_L &  CVAX_PAR_FEC_H & REG_WR_L /* special diag */
                    #                               /* test case */
                  !REG_WR_L;                        /* any write operation. */
|
ERR_ENA_L.OE = VCCR_41;
```


REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]
PAL EQN FILES:
20L8BSL_DCTRL.PLD

digital

DRN: K. Yesse	-	DATE	
CHK'D: -	-	DATE	
-	Thu Oct 20 17:05:08 1988		
FIRST USED ON OPTION/MODEL: -			

ENG: W. Chewbacca	-	DATE	
BOARD LOCATION: CXO			
SHEET 34			
NEXT HIGHER ASSEMBLY: -			

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

File: 20L8BSL_HIBSD.PLD
Source: DISK$HSBSIM_B:[SIMULATION.CMS]

```
NAME            hibsd;
PARTNO          xxxxx;
REVISION        02;
DATE            8/18/88;
DESIGNER        Versace;
COMPANY         DEC;
ASSEMBLY        Wildcat;
LOCATION        E94;
DEVICE          P20L8;
FORMAT          -jf;

/* 4/12/88 checked pins for new net list. removed novram csl output, added
   caddr21 input, added brd2 act output  - mr. rick */

/* 5/4/88 added deselect pin and move output pins  */

/* 7/1/88 temporarily eliminated the error log from brd2csl since
   it conflicts with exhicesl */

/* 7/5/88 fixed brd2cs decode and got rid of deselectl from brd2act */

/* 8/18/88 added hib reg cs decode and removed deselect from all eqns */


/*****************************************************************/
/*  This is the HIB space address decode pal.                    */
/*****************************************************************/

/**  INPUTS  **/

pin 1  = CADDR10;               /* plcc pin1   */
pin 2  = CADDR11;               /* plcc pin2   */
pin 3  = CADDR12;               /* plcc pin3   */
pin 4  = CADDR13;               /* plcc pin4   */
pin 5  = CADDR14;               /* plcc pin6   */
pin 6  = CADDR15;               /* plcc pin7   */
pin 7  = CADDR16;               /* plcc pin9   */
pin 8  = CADDR17;               /* plcc pin10  */
pin 9  = CADDR18;               /* plcc pin12  */
pin 10 = CADDR19;               /* plcc pin13  */
pin 11 = CADDR20;               /* plcc pin14  */
pin 13 = CADDR29;               /* plcc pin16  */
pin 14 = BUF_AS_L;              /* plcc pin17  */
pin 16 = CADDR21;               /* plcc pin20  */
pin 23 = REG_CS2;               /* plcc pin27  */

/**  OUTPUTS  **/

pin 15 = !BRD2_ACT_L;           /* plcc pin18  */
pin 17 = !HIB_REG_CS_L;         /* plcc pin21  */
pin 18 = !SISM_CS_L;            /* plcc pin22  */
pin 19 = !BRD2_CS_L;            /* plcc pin23  */
pin 20 = !DATA_BUF_CS_L;        /* plcc pin24  */
pin 21 = !CSIC_B_CS_L;          /* plcc pin25  */
pin 22 = !CSIC_A_CS_L;          /* plcc pin26  */

/** LOGIC VARIABLES **/

/**  LOGIC EQUATIONS  **/

DATA_BUF_CS_L   = !CADDR29 & !CADDR21 & !CADDR20 & !BUF_AS_L & REG_CS2;
            /* Addr bit 21 necc. to distinguish from proc mem decode */

SISM_CS_L       = CADDR29 & !CADDR21 & !CADDR20 & !CADDR19 & !CADDR18 &
                  !CADDR17 & !CADDR16 & !CADDR15 & !BUF_AS_L & REG_CS2;

CSIC_A_CS_L     =  CADDR29 & !CADDR21 & !CADDR20 & !CADDR19 & !CADDR18 &
                   !CADDR17 & !CADDR16 &  CADDR15 & !CADDR14 & !CADDR13 &
                   !CADDR12 & !CADDR11 & !CADDR10 & !BUF_AS_L & REG_CS2;

CSIC_B_CS_L     =  CADDR29 & !CADDR21 & !CADDR20 & !CADDR19 & !CADDR18 &
                   !CADDR17 & !CADDR16 &  CADDR15 & !CADDR14 & !CADDR13 &
                   !CADDR12 & !CADDR11 &  CADDR10 & !BUF_AS_L & REG_CS2;

BRD2_CS_L       =  CADDR29 & !CADDR21 & !CADDR20 & !CADDR19 & !CADDR18 &
                   !CADDR17 & !CADDR16 &  CADDR15 & !CADDR14 & !CADDR13 &
                   !CADDR12 &  CADDR11 &
                   !BUF_AS_L & REG_CS2;

HIB_REG_CS_L    =  CADDR29 & !CADDR21 & !CADDR20 & !CADDR19 & !CADDR18 &
                   !CADDR17 & !CADDR16 & CADDR15 & CADDR14 & CADDR13 &
                   !CADDR12 & !CADDR11 & !CADDR10 &
```

20L8BSL_HIBSD.PLD continued..

```
                   !BUF_AS_L & REG_CS2;

BRD2_ACT_L =    !CADDR29 & !CADDR21 & !CADDR20 & !BUF_AS_L & REG_CS2
                     /* DATA_BUF_CS_L  */
                  #
                CADDR29 & !CADDR21 & !CADDR20 & !CADDR19 & !CADDR18 &
                !CADDR17 & !CADDR16 & !CADDR15 & !BUF_AS_L & REG_CS2
                     /* SISM_CS_L     */
                  #
                CADDR29 & !CADDR21 & !CADDR20 & !CADDR19 & !CADDR18 &
                !CADDR17 & !CADDR16 &  CADDR15 & !CADDR14 & !CADDR13 &
                !CADDR12 & !CADDR11 & !CADDR10 & !BUF_AS_L & REG_CS2
                     /* CSIC_A_CS_L */
                  #
                CADDR29 & !CADDR21 & !CADDR20 & !CADDR19 & !CADDR18 &
                !CADDR17 & !CADDR16 &  CADDR15 & !CADDR14 & !CADDR13 &
                !CADDR12 & !CADDR11 &  CADDR10 & !BUF_AS_L & REG_CS2
                     /* CSIC_B_CS_L  */
                  #
                CADDR29 & !CADDR21 & !CADDR20 & !CADDR19 & !CADDR18 &
                !CADDR17 & !CADDR16 &  CADDR15 & !CADDR14 & !CADDR13 &
                !CADDR12 &  CADDR11 &
                !BUF_AS_L & REG_CS2
                     /* BRD2_CS_L */
                  #
                CADDR29 & !CADDR21 & !CADDR20 & !CADDR19 & !CADDR18 &
                !CADDR17 & !CADDR16 &  CADDR15 & CADDR14 & CADDR13 &
                !CADDR12 & !CADDR11 & !CADDR10 & !BUF_AS_L & REG_CS2;
                     /* HIB_REG_CS_L*/
```


REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]
PAL EQN FILES:
20L8BSL_HIBSD.PLD

digital

DRN: K. Yesse	-	DATE	ENG: W. Chewbacca	-	DATE
CHK'D: -	-	DATE	BOARD LOCATION: CXO		
- Thu Oct 20 17:05:14 1988			SHEET 35		
FIRST USED ON OPTION/MODEL: -			NEXT HIGHER ASSEMBLY: -		

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

File: 20L8BSL_PRMDE.PLD
Source: DISK$HSBSIM_B:[SIMULATION.CMS]

```
NAME          prmde;
PARTNO        xxxxx;
REVISION      03;
DATE          8/22/88;
DESIGNER      Versace;
COMPANY       DEC;
ASSEMBLY      Wildcat;
LOCATION      E61;
DEVICE        P20L8;
FORMAT        -jf;

/* 4-12-88  checked pinout for new netlist, rewired and added new equations
            and names for all outputs except scratchpadcs. added caddr21 input
              - mr. rick */

/* 6-3-88   buf_as_l was wrong sense in slowmemactl signal, added ! to each
            buf_as_l term in that equation.  rick */

/* 8-22-88  modified for In Ckt Test (ICT) Engineering to provide tri state
            capability */

/*************************************************************/
/*  This is the processor memory address decode pal.         */
/*************************************************************/

/**  INPUTS  **/

pin 1  = DESELECT_L;          /* plcc pin1   */
pin 2  = VCCR_42_H;           /* plcc pin2        8-22-88 for ICT */
pin 3  = SPARE_3;             /* plcc pin3   */
pin 4  = SPARE_4;             /* plcc pin4   */
pin 5  = SPARE_5;             /* plcc pin6   */
pin 6  = SPARE_6;             /* plcc pin7   */
pin 7  = CADDR17;             /* plcc pin9   */
pin 8  = CADDR18;             /* plcc pin10  */
pin 9  = CADDR19;             /* plcc pin12  */
pin 10 = CADDR20;             /* plcc pin13  */
pin 11 = CADDR21;             /* plcc pin14  */
pin 13 = CADDR29;             /* plcc pin16  */
pin 14 = BUF_AS_L;            /* plcc pin17  */
pin 23 = REG_CS2_H;           /* plcc pin27  */

/**  OUTPUTS  **/

pin 15 = !SLOW_MEM_ACT_L;     /* plcc pin18  */
pin 16 = !CODE_STR3_CS_L;     /* plcc pin20  */
pin 17 = !CODE_STR2_CS_L;     /* plcc pin21  */
pin 18 = !CODE_STR1_CS_L;     /* plcc pin22  */
pin 19 = !SCRATCH_PAD_CS_L;   /* plcc pin23  */
pin 20 = !SRAM_BANK2_CS_L;    /* plcc pin24  */
pin 21 = !SRAM_BANK1_CS_L;    /* plcc pin25  */
pin 22 = !FAST_MEM_ACT_L;     /* plcc pin26  */

/**  LOGIC EQUATIONS  **/

/* If vccr 42 h = high then ttl output else vccr 42 = low then tri state */

CS_CTRL = !BUF_AS_L & REG_CS2_H & DESELECT_L;

CODE_STR3_CS_L   = !CADDR29 &  CADDR21 & !CADDR20 & !CADDR19 & !CADDR18 &
                   !CADDR17 & CS_CTRL;

CODE_STR3_CS_L.OE = VCCR_42_H;

CODE_STR2_CS_L   = !CADDR29 & !CADDR21 &  CADDR20 &  CADDR19 &  CADDR18 &
                   CADDR17 & CS_CTRL;

CODE_STR2_CS_L.OE = VCCR_42_H;

CODE_STR1_CS_L   = !CADDR29 & !CADDR21 &  CADDR20 &  CADDR19 &  CADDR18 &
                   !CADDR17 & CS_CTRL;

CODE_STR1_CS_L.OE = VCCR_42_H;

SCRATCH_PAD_CS_L = !CADDR29 & !CADDR21 &  CADDR20 &  CADDR19 & !CADDR18 &
                   CS_CTRL;

SCRATCH_PAD_CS_L.OE = VCCR_42_H;

SRAM_BANK2_CS_L  = !CADDR29 & !CADDR21 &  CADDR20 & !CADDR19 &  CADDR18 &
                   CS_CTRL;
```

20L8BSL_PRMDE.PLD continued..

```
SRAM_BANK2_CS_L.OE = VCCR_42_H;

SRAM_BANK1_CS_L  = !CADDR29 & !CADDR21 &  CADDR20 & !CADDR19 & !CADDR18 &
                   CS_CTRL;

SRAM_BANK1_CS_L.OE = VCCR_42_H;

FAST_MEM_ACT_L   = !CADDR29 & !CADDR21 &  CADDR20 &  CADDR19 & !CADDR18 &
                   !BUF_AS_L & REG_CS2_H /* SCRATCH_PAD_CS_L */
                   #
                   !CADDR29 & !CADDR21 &  CADDR20 & !CADDR19 &  CADDR18 &
                   !BUF_AS_L & REG_CS2_H /* SRAM_BANK2_CS_L  */
                   #
                   !CADDR29 & !CADDR21 &  CADDR20 & !CADDR19 & !CADDR18 &
                   !BUF_AS_L & REG_CS2_H; /* SRAM_BANK1_CS_L  */

FAST_MEM_ACT_L.OE = VCCR_42_H;

SLOW_MEM_ACT_L   = !CADDR29 &  CADDR21 & !CADDR20 & !CADDR19 & !CADDR18 &
                   !CADDR17 & !BUF_AS_L & REG_CS2_H  /* CODE_STR3_CS_L   */
                   #
                   !CADDR29 & !CADDR21 &  CADDR20 &  CADDR19 &  CADDR18 &
                    CADDR17 & !BUF_AS_L & REG_CS2_H  /* CODE_STR2_CS_L */
                   #
                   !CADDR29 & !CADDR21 &  CADDR20 &  CADDR19 &  CADDR18 &
                   !CADDR17 & !BUF_AS_L & REG_CS2_H; /* CODE_STR1_CS_L   */

SLOW_MEM_ACT_L.OE = VCCR_42_H;
```


REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]
PAL EQN FILES:
20L8BSL_PRMDE.PLD

digital

FIRST USED ON OPTION/MODEL: -
Thu Oct 20 17:05:20 1988

DRN: K. Yesse	DATE -	ENG: W. Chewbacca	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
		SHEET 36	
		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

File: 20L8BSL_RGCTL.PLD
Source: DISK$HSBSIM_B:[SIMULATION.CMS]

```
NAME          RGCTL;
PARTNO        xxxxx;
REVISION      01;
DATE          8/22/88;
DESIGNER      Versace;
COMPANY       DEC;
ASSEMBLY      Wildcat;
LOCATION      E80;
DEVICE        P20L8;
FORMAT        -jf;

/* 4-22-88  added equation for err addr clk h and moved some pins
            - mr. rick */

/* 6-24-88  replaced delayed as with perr clk */

/* 8-22-88 modified for in ckt test engr. -- provide z capability */

/*****************************************************************/
/*  This is the REGISTER CONTROL pal.                            */
/*****************************************************************/


/**  INPUTS  **/

pin 1  = BUF_DBE_L;              /* plcc pin1   */
pin 2  = ACLKC;                  /* plcc pin2   */
pin 3  = ACLKB;                  /* plcc pin3   */
pin 4  = BUF_DS_L;               /* plcc pin4   */
pin 5  = BUF_AS_L;               /* plcc pin6   */
pin 6  = REG_WR_L;               /* plcc pin7   */
pin 7  = REG_CS2_H;              /* plcc pin9   */
pin 8  = ERR_ADDR_CS_L;          /* plcc pin10  */
pin 9  = WR_DIAG_CS_L;           /* plcc pin12  */
pin 10 = RD_DIAG_CS_L;           /* plcc pin13  */
pin 11 = DEASSERT_L;             /* plcc pin14  */
pin 13 = DCLK_DIS_L;             /* plcc pin16  */
pin 14 = SPARE_14;               /* plcc pin17  */
pin 23 = VCCR_43;                /* plcc pin27  */

/**  OUTPUTS  **/

pin 15 = !WR_DIAG_RDBK_L;        /* plcc pin18  */
pin 16 = PAR_CLK_H;              /* plcc pin20  */
pin 17 = PERR_CLK_H;             /* plcc pin21  */
pin 18 = ERR_ADDR_CLK_H;         /* plcc pin22  */
pin 19 = !ERR_ADDR_RDBK_L;       /* plcc pin23  */
pin 20 = !RD_DIAG_ENA_L;         /* plcc pin24  */
pin 21 = RD_DIAG_CLK;            /* plcc pin25  */
pin 22 = WR_DIAG_CLK;            /* plcc pin26  */


/**  LOGIC EQUATIONS  **/

PERR_CLK_H  =  ACLKC & DCLK_DIS_L;      /* Clock parity error reg when */
                                        /* aclkc 0->1 and dclk dis not asserted */

PERR_CLK_H.OE  =  VCCR_43;


/* Clock the err add reg when it is not being selected. The assertion of
   buf dsl will assert the clock high, and dclk dis will not allow the
   register to be clocked after and error has occured. */

ERR_ADDR_CLK_H = ERR_ADDR_CS_L & !BUF_DS_L & DCLK_DIS_L;

ERR_ADDR_CLK_H.OE =  VCCR_43;

ERR_ADDR_RDBK_L = !ERR_ADDR_CS_L & REG_WR_L;

ERR_ADDR_RDBK_L.OE  =  VCCR_43;

 WR_DIAG_CLK    = !REG_WR_L & !BUF_DS_L & !WR_DIAG_CS_L & ACLKB;

WR_DIAG_CLK.OE  =  VCCR_43;

WR_DIAG_RDBK_L  = !WR_DIAG_CS_L & REG_WR_L;

WR_DIAG_RDBK_L.OE  =  VCCR_43;

/* assert rd diag clk every cycle except when an error occurs (dclk_dis_L)
   or we are trying to read the register (rd_diag_cs_l)     */
```

20L8BSL_RGCTL.PLD continued..

```
RD_DIAG_CLK     = !ACLKC & !BUF_DBE_L & DCLK_DIS_L & DEASSERT_L & RD_DIAG_CS_L;

RD_DIAG_CLK.OE  =  VCCR_43;

RD_DIAG_ENA_L   = !RD_DIAG_CS_L & REG_WR_L;

RD_DIAG_ENA_L.OE  =  VCCR_43;

/* there might be a problem with the parity capture. Parity is valid at 180
   until 205. This clk edge should occur near 200.  */

PAR_CLK_H       =  !DEASSERT_L & DCLK_DIS_L & !BUF_AS_L;

PAR_CLK_H.OE  =  VCCR_43;
```


REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]
PAL EQN FILES:
20L8BSL_RGCTL.PLD

digital

DRN: K. Yesse	DATE -	ENG: W. Chewbacca	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
- Thu Oct 20 17:05:25 1988		SHEET 37	
FIRST USED ON OPTION/MODEL: -		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

File: 20L8BSL_XICSD.PLD
Source: DISK$HSBSIM_B:[SIMULATION.CMS]

```
NAME          XICSD;
PARTNO        xxxxx;
REVISION      02;
DATE          8/22/88;
DESIGNER      Versace;
COMPANY       DEC;
ASSEMBLY      Wildcat;
LOCATION      E62;
DEVICE        P20L8;
FORMAT        -jf;

/* 4-12-88  rewired pins for new netlist - mr. rick */

/* 5/4/88  added deselectl to xic act 1 term  */

/* 8/22/88 removed deselect term from xic act eqn -- */
/*            dave did this solely on his own volition */

/*************************************************************/
/*  This is the XIC and special address decode pal.          */
/*************************************************************/

/**  INPUTS  **/

pin 1  = CADDR10;              /* plcc pin1   */
pin 2  = CADDR11;              /* plcc pin2   */
pin 3  = CADDR12;              /* plcc pin3   */
pin 4  = CADDR13;              /* plcc pin4   */
pin 5  = CADDR14;              /* plcc pin6   */
pin 6  = CADDR15;              /* plcc pin7   */
pin 7  = CADDR16;              /* plcc pin9   */
pin 8  = CADDR17;              /* plcc pin10  */
pin 9  = CADDR18;              /* plcc pin12  */
pin 10 = CADDR19;              /* plcc pin13  */
pin 11 = CADDR20;              /* plcc pin14  */
pin 13 = CADDR29;              /* plcc pin16  */
pin 14 = BUF_AS_L;             /* plcc pin17  */
pin 16 = DESELECT_L;           /* plcc pin20  */
pin 23 = REG_CS2;              /* plcc pin27  */

/**  OUTPUTS  **/

pin 15 = !XIC_ACT_L;           /* plcc pin18  */
pin 17 = !RD_DIAG_CS_L;        /* plcc pin21  */
pin 18 = !WR_DIAG_CS_L;        /* plcc pin22  */
pin 19 = !XISM_CS_L;           /* plcc pin23  */
pin 20 = !CXHIC_CS_L;          /* plcc pin24  */
pin 21 = !DPC_CS_L;            /* plcc pin25  */
pin 22 = !VIC_CS_L;            /* plcc pin26  */

/**  LOGIC EQUATIONS  **/

XISM_CS_L      =  CADDR29 & !CADDR20 & !CADDR19 & !CADDR18 & !CADDR17 &
                  !CADDR16 &  CADDR15 & !CADDR14 &  CADDR13 &
                  !BUF_AS_L & REG_CS2;

CS_CTRL  =  !BUF_AS_L & REG_CS2 & DESELECT_L;

RD_DIAG_CS_L   =  CADDR29 & !CADDR20 & !CADDR19 & !CADDR18 & !CADDR17 &
                  !CADDR16 &  CADDR15 &  CADDR14 & !CADDR13 & !CADDR12 &
                  !CADDR11 &  CADDR10 & CS_CTRL;

WR_DIAG_CS_L   =  CADDR29 & !CADDR20 & !CADDR19 & !CADDR18 & !CADDR17 &
                  !CADDR16 &  CADDR15 &  CADDR14 & !CADDR13 & !CADDR12 &
                  !CADDR11 & !CADDR10 & CS_CTRL;

VIC_CS_L       =  CADDR29 & !CADDR20 & !CADDR19 & !CADDR18 &
                  !CADDR17 & !CADDR16 &  CADDR15 &  CADDR14 &
                  !CADDR13 &  CADDR12 & !CADDR11 & !CADDR10 &
                  !BUF_AS_L & REG_CS2;

CXHIC_CS_L     =  CADDR29 & !CADDR20 & !CADDR19 & !CADDR18 &
                  !CADDR17 & !CADDR16 &  CADDR15 & !CADDR14 &
                  !CADDR13 &  CADDR12 &  CADDR11 & !CADDR10 &
                  !BUF_AS_L & REG_CS2;

DPC_CS_L       =  CADDR29 & !CADDR20 & !CADDR19 & !CADDR18 &
                  !CADDR17 & !CADDR16 &  CADDR15 & !CADDR14 &
                  !CADDR13 &  CADDR12 &  CADDR11 &  CADDR10 &
                  !BUF_AS_L & REG_CS2;

XIC_ACT_L      =  CADDR29 & !CADDR20 & !CADDR19 & !CADDR18 & !CADDR17 &
```

20L8BSL_XICSD.PLD continued..

```
                  !CADDR16 & CADDR15 & !CADDR14 & CADDR13 &
                  !BUF_AS_L & REG_CS2
                       #
                   CADDR29 & !CADDR20 & !CADDR19 & !CADDR18 &
                  !CADDR17 & !CADDR16 &  CADDR15 & !CADDR14 &
                  !CADDR13 &  CADDR12 &  CADDR11 & !CADDR10 &
                  !BUF_AS_L & REG_CS2
                       #
                   CADDR29 & !CADDR20 & !CADDR19 & !CADDR18 &
                  !CADDR17 & !CADDR16 &  CADDR15 & !CADDR14 &
                  !CADDR13 &  CADDR12 &  CADDR11 &  CADDR10 &
                  !BUF_AS_L & REG_CS2;
```


REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]
PAL EQN FILES:
20L8BSL_XICSD.PLD

digital

DRN: K. Yesse	-	DATE	ENG: W. Chewbacca	-	DATE
CHK'D: -		DATE -	BOARD LOCATION: CXO		
			SHEET 38		
- Thu Oct 20 17:05:31 1988			NEXT HIGHER ASSEMBLY: -		
FIRST USED ON OPTION/MODEL: -					

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

File: 20R4BSL_MCTRL.PLD
Source: DISK$HSBSIM_B:[SIMULATION.CMS]

```
NAME            MCTRL;
PARTNO          NONE;
REVISION        03;
DATE            8/22/88;
DESIGNER        Versace;
COMPANY         DEC;
ASSEMBLY        WILDASS;
LOCATION        E86;
DEVICE          P20R4;
|
/* 4-12-88   moved pins around for new netlist - mr. rick */
/* 4-13-88   READYL has been changed to READYH, so we simply changed
          the polarity of the input (added !) to make the equations
          right - mr.rick */
/* 5-25-88   Added resetl term to invaddr logic so invaddr will clear during
             sysrst time since aclkc will be running */
/* 8-22-88   modified for ICT engr. to provide tri state capabilities
             also changed ready_l to ready_h and the associated !s */
|
/*************************************************************************/
/*  MEMORY CONTROL PAL                                                   */
/*************************************************************************/
|
/**  INPUTS  **/
|
pin 1  = ACLKC;                 /* plcc pin1  */
pin 2  = ACLKB;                 /* plcc pin2  */
pin 3  = BUF_DS_L;              /* plcc pin3  */
pin 4  = BUF_AS_L;              /* plcc pin4  */
pin 5  = REG_WR_L;              /* plcc pin6  */
pin 6  = READY_H;               /* plcc pin7  */
pin 7  = SYSRST_L;              /* plcc pin9  */
pin 8  = CADDR30;               /* plcc pin10 */
pin 9  = CADDR31;               /* plcc pin12 */
pin 10 = SPARE10;               /* plcc pin13 */
pin 11 = SPARE11;               /* plcc pin14 */
/*pin 13 = rgnd 5 1             /* plcc pin16 - OE16 */
pin 14 = SPARE14;               /* plcc pin17 */
pin 23 = VCCR_44;               /* plcc pin27 */
|
/** OUTPUTS  **/
|
pin 15 = SPARE15;               /* plcc pin18 */
pin 16 = SPARE16;               /* plcc pin20 */
pin 17 = SPARE17;               /* plcc pin21 */
pin 18 = SPARE18;               /* plcc pin22 */
pin 19 = SPARE19;               /* plcc pin23 */
pin 20 = !INV_ADDR;             /* plcc pin24 */
pin 21 = !DEASSERT_L;           /* plcc pin25 */
pin 22 = !DESELECT_L;           /* plcc pin26 */
|
/**  LOGIC EQUATIONS  **/
|
/* wr_enable is fed to eerproms and srams. Will deassert 2 pal delays after the
start of phi4. This should be before DSL deasserts so valid data will still be
on the cdal */
|
WR_ENABLE_L     = !REG_WR_L & !DEASSERT_L;  /* single cycles */
|
WR_ENABLE_L.OE  = VCCR_44;
|
INV_ADDR.D      = !CADDR31 & CADDR30     /* Multiple read cycle -- only */
                  #                      /* one address given so must   */
                  !READY_H & INV_ADDR    /* invert CADDR 2 for second   */
                  #                      /* lonword fetch -- ready      */
                  READY_H & !INV_ADDR    /* indicates how far we've     */
                  #                      /*  progressed in cycle        */
                  !SYSRST_L;             /* added 5-25-88 */
|
/* bufdsl added */
DEASSERT_L      =  !INV_ADDR & READY_H & ACLKB & !BUF_DS_L & !BUF_AS_L & SYSRST_L  /* multiple reads */
                   #
                  !CADDR31 & CADDR30 & READY_H & ACLKB & !BUF_AS_L & SYSRST_L  /* single cycles */
                   #
                  !BUF_AS_L & SYSRST_L & DEASSERT_L;   /* System Reset prevents initial latch up */
                                                       /* feedback latch up until end of cycle   */
DEASSERT_L.OE   = VCCR_44;
|
DESELECT_L      =   DEASSERT_L & !BUF_AS_L;  /* REG_WR_L  removed */
|
DESELECT_L.OE   = VCCR_44;
```


REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]
PAL EQN FILES:
20R4BSL_MCTRL.PLD

digital

Thu Oct 20 17:05:37 1988

FIRST USED ON OPTION/MODEL: -

DRN: K. Yesse	- DATE	ENG: W. Chewbacca	- DATE	TITLE: WILDCAT BOARD 1	
CHK'D: -	DATE	BOARD LOCATION: CXO			
		SHEET 39		SIZE K / CODE CS / NUMBER - / REV 20OCT88	
		NEXT HIGHER ASSEMBLY: -			

File: 20R4BSL_READY.PLD
Source: DISK$HSBSIM_B:[SIMULATION.CMS]

```
NAME            READY;
PARTNO          NONE;
REVISION        02;
DATE            8/22/88;
DESIGNER        Versace;
COMPANY         DEC;
ASSEMBLY        WILDASS;
LOCATION        E83;
DEVICE          P20R4;

/* 4-12-88   moved pins around for new netlist - mr. rick */

/* 6-7-88    added one more flip flop delay to slow mem activity */

/* 6-8-88    changed the ready_h deassertion for the eeprom slip cycle */
/*           conditions - mr. mike and mr. dave */

/* 6-17-88   added all hib logic to pal - mr. dave */

/* 6-24-88   replaced delayed as with buf as */

/* 7-6-88    changed cba to hib dir and changed its polarity to provide */
/*           adequate delay for hib reads */

/* 7-11-88   sync fix for any arbitor related activity on writes */

/* 8-22-88   rearranged signals for dave's aesthetically pleasing schematics */

/*************************************************************************/
/*  READY GENERATION PAL                                                 */
/*************************************************************************/

/** INPUTS **/

pin 1  = CLKC;                          /* plcc pin1  */
pin 2  = XIC_ACT_L;                     /* plcc pin2  */
pin 3  = BUF_DS_L;                      /* plcc pin3  */
pin 4  = BUF_AS_L;                      /* plcc pin4  */
pin 5  = REG_WR_L;                      /* plcc pin6  */
pin 6  = SLOW_MEM_ACT_L;                /* plcc pin7  */
pin 7  = FAST_MEM_ACT_L;                /* plcc pin9  */
pin 8  = WR_DIAG_CS_L;                  /* plcc pin10 */
pin 9  = RD_DIAG_CS_L;                  /* plcc pin12 */
pin 10 = NXM;                           /* plcc pin13 */
pin 11 = LOCK_L;                        /* plcc pin14 */
pin 13 = RGND1_L;                       /* plcc pin16 */
pin 14 = HIB_DIR;                       /* plcc pin17 */
pin 16 = ACLKC;                         /* plcc pin20 */
pin 21 = BRD2_ACT_L;                    /* plcc pin25 - added 6-8-88 for deassertion */
pin 23 = BUSCLK;                        /* plcc pin27 */

/** OUTPUTS **/

pin 15 = !READY_L;                      /* plcc pin18 */
pin 17 = !EE_1_L;                       /* plcc pin21 */
pin 18 = !EE_2_L;                       /* plcc pin22 */
pin 19 = !EE_3_L;                       /* plcc pin23 */
pin 20 = SPARE_REG20;                   /* plcc pin24 */
pin 22 = READY_H;                       /* plcc pin26 */

        /* YOU WILL NOTE THAT READY IS ACTIVE HIGH!!!!! */

/**  LOGIC EQUATIONS  **/

READY_H  = READY_L & !ACLKC                     /* syncs with CVAX during */
                                                /* last 50ns of data cycle */
         #
           EE_3_L & !BUF_DS_L & !ACLKC;         /* EEPROM feedback */
                                                /* BUF DS is used for */
                                                /* deassertion during */
                                                /* slipped cycles */
                                                /* 6-8-88 */

READY_L  = !FAST_MEM_ACT_L & !NXM               /* Any SRAM select */
         #
           !WR_DIAG_CS_L & !NXM                 /* Write Diagnostic */
         #
           !RD_DIAG_CS_L & !NXM                 /* Read Diagnostic */
         #
           !BRD2_ACT_L &                        /* Write to board 2 */
           !REG_WR_L &                          /* Write */
           LOCK_L &                             /* Nothing pending */
           !BUSCLK &
```

20R4BSL_READY.PLD continued..

```
           !NXM
         #
           !XIC_ACT_L & !REG_WR_L &             /* Write to XIC */
           !BUSCLK &
           LOCK_L & !NXM
         #
           !BRD2_ACT_L & REG_WR_L & LOCK_L &    /* Read from BD2 */
           !HIB_DIR &                           /* Processor grant completed */
           !NXM                                 /* and data latched in 646 */
         #
           !XIC_ACT_L & REG_WR_L & LOCK_L &     /* Read from XIC */
           !HIB_DIR &                           /* Processor grant completed */
           !NXM;                                /* and data latched in 646 */

EE_1_L.D  = !SLOW_MEM_ACT_L & !BUF_AS_L &       /* must delay ready gen. */
            !NXM;                               /* to account for 250ns */
EE_2_L.D  = EE_1_L & !BUF_AS_L;                 /* EEPROM access times  */

EE_3_L.D  = EE_2_L & !BUF_AS_L;
```


REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]
PAL EQN FILES:
20R4BSL_READY.PLD

digital

DRN: K. Yesse	DATE -	ENG: W. Chewbacca	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
- Thu Oct 20 17:05:48 1988		SHEET 40	
FIRST USED ON OPTION/MODEL: -		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

File: 20RA10SL_CHCTL.PLD
Source: DISK$HSBSIM_B:[SIMULATION.CMS]

```
NAME          CHCTL;
PARTNO        23-000J8-01;
REVISION      01;
DATE          8/23/88;
DESIGNER      Versace;
COMPANY       DEC;
ASSEMBLY      Wildcat board 1;
LOCATION      E134;
DEVICE        P20RA10;
|
|
/*************************************************************************/
/*                                                                       */
/*  Wildcat BOARD 1 PAL: CVAX to HIB Control pal                         */
/*                                                                       */
/*  REVISION HISTORY:                                                    */
/*                                                                       */
/*************************************************************************/
/*                                                                       */
/*      CUPL Rules of Thumb used herein:                                 */
/*        2) Noninverted outputs (without '!') indicate state            */
/*           at latch Q output, or from polarity XOR if pass-thru.       */
/*        3) Inverting an entire expression should blow polarity fuse.   */
/*        4) Due to output lines being declared with '!' (by             */
/*           definition), feedback lines will have opposite polarity     */
/*           than inputs when used in logic equations.                   */
/*                                                                       */
/*************************************************************************/
|
/* 7-19-88  add ! to xi_grant_L in 2nd term of hibto dpcl     */
/* 8/11/88  add ! to xic_cxhic_cs_l in 3rd term of hibtodpc. Without
            this, the hibtodpcl asserts when the xism tries to write
            the byte status to the workblock. - mr rick */
/* 8-23-88  BUSCLK incorrectly listed as output is really input -- dmv */
|
|
/**  INPUTS  **/
|
pin 2  = STR_CXHIC_CS_L;          /* plcc pin 3   */
pin 3  = STR_DPC_CS_L;            /* plcc pin 4   */
pin 4  = STR_WR_L;                /* plcc pin 5   */
pin 5  = XI_GRANT_L;              /* plcc pin 6   */
pin 6  = BUF_DBE_L;               /* plcc pin 7   */
pin 7  = XIC_GRANT_L;             /* plcc pin 9   */
pin 8  = PGRANT_L;                /* plcc pin 10  */
pin 9  = REG_WR_L;                /* plcc pin 11  */
pin 10 = SYSRST_L;                /* plcc pin 12  */
pin 11 = XIC_ACT_L;               /* plcc pin 13  */
pin 14 = BRD2_ACT_L;              /* plcc pin 17  */
pin 15 = XIC_CXHIC_CS_L;          /* plcc pin 18  */
pin 16 = BUSCLK;                  /* plcc pin 19  */
|
/* pin 1  = Vccr 29 H                plcc pin 2        preload default    */
/* pin 13 = Rgnd 14 L                plcc pin 16       output enable def. */
|
|
/**  OUTPUTS  **/
|
pin 17 = HACK;                    /* plcc pin 20  */
pin 18 = !XIC_REQ_L;              /* plcc pin 21  */
pin 19 = !LOCK_L;                 /* plcc pin 23  */
pin 20 = !PREQ_L;                 /* plcc pin 24  */
pin 21 = !HIB_TO_DPC_L;           /* plcc pin 25  */
pin 22 = !HIB_TO_CXHIC_L;         /* plcc pin 26  */
pin 23 = !CXHIC_TO_HIB_L;         /* plcc pin 27  */
|
|
|
/**  LOGIC EQUATIONS  **/
|
CXHIC_TO_HIB_L  = !STR_CXHIC_CS_L &     /* PROC read of CXHIC */
                  STR_WR_L
                  #
                  !XIC_CXHIC_CS_L &     /* XISM write to data buffer */
                  !STR_WR_L &
                  !XI_GRANT_L;
|
HIB_TO_CXHIC_L  = !STR_CXHIC_CS_L &     /* PROC write to CXHIC */
                  !STR_WR_L
                  #
                  !XIC_CXHIC_CS_L &     /* XISM read of data buffer */
                   STR_WR_L &
```

20RA10SL_CHCTL.PLD continued..

```
                  !XI_GRANT_L;
|
HIB_TO_DPC_L    = !STR_DPC_CS_L &       /* PROC write to DPC */
                  !STR_WR_L
                   #
                  !XI_GRANT_L &         /* XISM read of data buffer */
                   STR_WR_L             /* or workblock polling by DPC */
                   #
                  !XI_GRANT_L &         /* XMI write to data buffer  */
                  !STR_WR_L &           /* EDC calculation by DPC */
                  !XIC_CXHIC_CS_L;
|
 /* LOCK L inhibits a current new CVAX HIB cycle from overwriting pending */
 /* old HIB cycle data which has not received a bus grant and thus */
 /* is still waiting to complete */
 /* LOCK is asserted on the rising edge of BUSCLK and remains asserted */
 /* until the end of a bus grant cycle  */
|
LOCK_L.D        = !BRD2_ACT_L &         /* HIB write initially sets LOCK L */
                  !REG_WR_L &
                  !LOCK_L               /* LOCK not currently asserted */
                     #
                  !XIC_ACT_L &          /* or CVAX write to XISM */
                  !REG_WR_L &
                  !LOCK_L               /* LOCK not currently asserted */
                     #
                  XIC_GRANT_L &         /* upon receiving either GRANT */
                  PGRANT_L &            /* deassert LOCK at end of cycle */
                  LOCK_L;               /* on rising edge of BUSCLK */
|
LOCK_L.CK       = BUSCLK;
|
LOCK_L.AR       = !SYSRST_L;            /* Initial clear at power up */
|
|
PREQ_L.D        = !BRD2_ACT_L &         /* If no XIC REQUEST is pending */
                  !XIC_REQ_L &          /* post PROC REQUEST on rising edge */
                   SYSRST_L             /* of Busclk H if BRD2 Activity asst */
                     #
                   SYSRST_L &           /* Continue to assert request until */
                   PREQ_L;              /* receipt of GRANT  */
|
PREQ_L.CK       = BUSCLK;
|
PREQ_L.AR       = !PGRANT_L;            /* remove Processor Request */
|
|
XIC_REQ_L.D     = !PREQ_L &             /* if no Processor Request pending */
                  !XIC_ACT_L &          /* assert XI Controller Request */
                   SYSRST_L
                     #
                   SYSRST_L &
                   XIC_REQ_L;
|
XIC_REQ_L.CK    = BUSCLK;
|
XIC_REQ_L.AR    = !XIC_GRANT_L;         /* remove XI Controller Request */
|
|
HACK            = !BRD2_ACT_L &         /* Provide clock to capture CVAX */
                  !LOCK_L &             /* HIB addr and control */
                  !BUF_DBE_L            /* assures CVAX addr and ctrl stable */
                     #
                  !XIC_ACT_L &          /* allow assertion of synchronized */
                  !LOCK_L &             /* XIC chip selects  */
                  !BUF_DBE_L;           /* assures CVAX CS stable  */
|
```


REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]
PAL EQN FILES:
20RA10SL_CHCTL.PLD

digital

DRN: K. Yesse	DATE -	ENG: W. Chewbacca	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
		SHEET 41	
-	Thu Oct 20 17:05:55 1988	NEXT HIGHER ASSEMBLY: -	
FIRST USED ON OPTION/MODEL: -			

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

File: 20RA10SL_MEMER.PLD
Source: DISK$HSBSIM_B:[SIMULATION.CMS]

```
NAME          MEMER;
PARTNO        23-000J8-01;
REVISION      04;
DATE          8/26/88;
DESIGNER      Versace;
COMPANY       DEC;
ASSEMBLY      Wildcat board 1;
LOCATION      E142;
DEVICE        P20RA10;

/*************************************************************************/
/*                                                                       */
/*  Wildcat BOARD 1 PAL: Memory Error Generator                          */
/*                                                                       */
/*  REVISION HISTORY:                                                    */
/*                                                                       */
/*************************************************************************/
/*                                                                       */
/*      CUPL Rules of Thumb used herein:                                 */
/*        2) Noninverted outputs (without '!') indicate state            */
/*           at latch Q output, or from polarity XOR if pass-thru.       */
/*        3) Inverting an entire expression should blow polarity fuse.   */
/*        4) Due to output lines being declared with '!' (by             */
/*           definition), feedback lines will have opposite polarity     */
/*           than inputs when used in logic equations.                   */
/*                                                                       */
/*************************************************************************/

/* 5/26/88 remove dpe from all equations since cvaxperrl is now qualified
   in the dctrl pal with dpe and deassertl */

/* 5/26/88 remove deselect from the .ck input on the rd diag reg cvax perrl
   bit since cvaxperrl is now qualified with deassert in the dctrl pal */

/* 6/14/88 total redesign of the memory error pal - 20ra10 changed to new
   pinouts, but the kernal board will use the old... thus this pld file
   was renamed to k20ra10sl_memer.pld */

/* 6/16/88 changed polarity err_disable */

/* 6/23/88 to please dave's schematics - switched buf ds and reg oen */

/* 7/5/88 wrong sense of err_disable in mem err equation */

/* 8/22/88 modify dclk dis equation - removing xic perr
           -- changed reset to the xic perr latch to xic_err_reset */
/* 8/26/88 modified mem err eqn so that if cvax perr and hib perr occur
           simulatanceously the pal will regenerate mem err after servicing
           of the first of the two error indications */

/**  INPUTS  **/

pin 2  = REG_OEN_L;              /* plcc pin 3   */
pin 3  = SYSERR_L;               /* plcc pin 4   */
pin 4  = RD_DIAG_ENA_L;          /* plcc pin 5   */
pin 5  = ERR_DISABLE_L;          /* plcc pin 6   */
pin 6  = HIB_PERR_L;             /* plcc pin 7   */
pin 7  = REG_CS2_H;              /* plcc pin 9   */
pin 8  = SYSRST_L;               /* plcc pin 10  */
pin 9  = CVAX_PAR_ERR;           /* plcc pin 11  */
pin 10 = ACLKC;                  /* plcc pin 12  */
pin 11 = BUF_DS_L;               /* plcc pin 13  */
pin 14 = XIC_ERR_RESET_L;        /* plcc pin 17    added 8/22/88 */

/* pin 1  = Vccr 28 H            plcc pin 2       preload default    */
/* pin 13 = Rgnd 12 L            plcc pin 16      output enable def. */

/**  OUTPUTS  **/

pin 15 = !CDAL_25_H;             /* plcc pin 18  - VIC ERROR L */
pin 16 = !CDAL_26_H;             /* plcc pin 19  - DPC PERR L  */
pin 17 = !CDAL_27_H;             /* plcc pin 20  - CVAX PERR L */
pin 18 = spare_18;               /* plcc pin 21  - SPARE PIN   */
pin 19 = !PAL_RESET_L;           /* plcc pin 23 */
pin 20 = !BUS_TIMEOUT_L;         /* plcc pin 24 */ /* local output */
pin 21 = !DCLK_DIS_L;            /* plcc pin 25 */
pin 22 = !MEM_ERR_L;             /* plcc pin 26 */
pin 23 = !VIC_ERROR_L;           /* plcc pin 27 */ /* local output */
```

20RA10SL_MEMER.PLD continued..

```
/**  LOGIC EQUATIONS  **/

MEM_ERR_L      = VIC_ERROR_L          /* VIC_ERROR_L asserted */
                 #
                 ERR_DISABLE_L &      /* ERR_DISABLE deasserted */
                 !HIB_PERR_L &        /* DPC parity error asserted */
                 !PAL_RESET_L         /* deasst. -If clearing CVAX PERR */
                                      /* asserted MEM ERR will toggle */
                 #
                 ERR_DISABLE_L &      /* ERR_DISABLE deasserted */
                 CVAX_PAR_ERR &       /* CVAX_PAR_ERR asserted */
                 XIC_ERR_RESET_L;     /* deasst. -If clearing HIB PERR */
                                      /* asserted MEM ERR will toggle */

DCLK_DIS_L     = CVAX_PAR_ERR         /* CVAX_PAR_ERR asserted  */
                 #
                 BUS_TIMEOUT_L        /* or BUS_TIMEOUT asserted */
                 #
                 VIC_ERROR_L;         /* or VIC_ERROR_L asserted */

PAL_RESET_L.D  = !RD_DIAG_ENA_L;      /* RD_DIAG_ENA_L asserted  */

PAL_RESET_L.CK = ACLKC;               /* Clocks on: CLKC 0->1  */

PAL_RESET_L.AP = !SYSRST_L;           /* ASSERTED - assert pal_reset_L
                                         on power up */

PAL_RESET_L.AR = SYSRST_L &           /* SYSRST_L deasserted */
                 !DCLK_DIS_L;         /* DCLK_DIS_L deasserted */


        /* CVAX_PERR_L part of read diag register */
CDAL_27_H.D    = 'b'1;                /* Latch data always 1   */

        /* CLOCKS ON ERROR ASSERTION 1 -> 0 */
CDAL_27_H.CK   = CVAX_PAR_ERR;        /* CVAX_PAR_ERR asserted  */

CDAL_27_H.AR   = PAL_RESET_L;         /* Resets on !PAL_RESET_L asserted  */

CDAL_27_H.OE   = !REG_OEN_L;          /* Enables on REG_OEN_L asserted */


        /* DPC_PERR_L part of read diag register */
CDAL_26_H.D    = 'b'1;                /* Latch data always 1  */

        /* CLOCKS ON ERROR ASSERTION 1 -> 0 */
CDAL_26_H.CK   = !HIB_PERR_L;         /* HIB_PERR_L asserts  */

CDAL_26_H.AR   = !XIC_ERR_RESET_L;    /* Resets by sftw toggle of write */
                                      /* diagnostic register bit       */

CDAL_26_H.OE   = !REG_OEN_L;          /* Enables on REG_OEN_L asserted */


        /* VIC ERROR part of read diag register */
CDAL_25_H.D    = 'b'1;                /* Latch data always 1  */

CDAL_25_H.CK   = !REG_CS2_H &         /* Clocks on:   BUV_CS2_H 1->0  */
                 !SYSERR_L;           /*                ERR_L asserted  */

CDAL_25_H.AR   = PAL_RESET_L;         /* Resets on PAL_RESET_L asserted  */

CDAL_25_H.OE   = !REG_OEN_L;          /* Enables on REG_OEN_L asserted */


/* WHEN CS2 IS LOW AND SYSERR IS ASSERTED, THEN WE ARE PROBABLY IN AN INT ACK
   CYCLE AND MUST POST MEM_ERR TO GET OUT OF AN INFINITE LOOP.
   This signal does not need to be cleared since syserr will deassert on the
   next cycle. This circuit is required since the CDAL 25 H ckt is tristated
   until read and thus can not provide feedback. */

VIC_ERROR_L.D  = !REG_CS2_H &         /* REG_CS2_H deasserted  */
                 !SYSERR_L;           /* ERR_L asserted  */

/* Clocks at the end of the cycle when BUF_DS_L goes high (deasserts)
   and DCLK_DIS_L is deasserted */

VIC_ERROR_L.CK = BUF_DS_L &           /* BUF_DS_L deasserts */
```


REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]
PAL EQN FILES:
20RA10SL_MEMER.PLD

DRN: K. Yesse	DATE -	ENG: W. Chewbacca	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
- Thu Oct 20 17:06:02 1988		SHEET 42	
FIRST USED ON OPTION/MODEL: -		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

20RA10SL_MEMER.PLD continued..
Source: DISK$HSBSIM_B:[SIMULATION.CMS]

```
                    !DCLK_DIS_L;            /* DCLK_DIS_L deasserted */
|
VIC_ERROR_L.AR  = PAL_RESET_L;              /* Resets on PAL_RESET_L asserted  */
|
/* Any NXM will result in the SSC asserting SYSERR due to a CVAX */
/* bus timeout -- this error will only disable error reporting regs. */
|
BUS_TIMEOUT_L.D = REG_CS2_H &               /* REG_CS2_H asserted */
                  !SYSERR_L;                /* ERR_L asserted */
|
/* Clocks at the end of the cycle when BUF_DS_L goes high (deasserts)
   and DCLK_DIS_L is deasserted */
|
BUS_TIMEOUT_L.CK = !DCLK_DIS_L &            /* DCLK_DIS_L deasserted */
                   BUF_DS_L;                /* BUF_DS_L deasserts */
|
BUS_TIMEOUT_L.AR = PAL_RESET_L;             /* reset on PAL_RESET_L asserted */
```


REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]
PAL EQN FILES:
20RA10SL_MEMER.PLD

digital

- Thu Oct 20 17:06:07 1988
FIRST USED ON OPTION/MODEL: -

DRN: K. Yesse	- DATE	ENG: W. Chewbacca	- DATE	TITLE: WILDCAT BOARD 1	
CHK'D: -	- DATE	BOARD LOCATION: CXO			
		SHEET 43			
		NEXT HIGHER ASSEMBLY: -		SIZE K / CODE CS / NUMBER - / REV 20OCT88	

File: 20RA10SL_PARR4.PLD
Source: DISK$HSBSIM_B:[SIMULATION.CMS]

```
NAME          PARR4;
PARTNO        23-000J8-01;
REVISION      02;
DATE          9/9/88;
DESIGNER      Versace;
COMPANY       DEC;
ASSEMBLY      Wildcat board 1;
LOCATION      E136;
DEVICE        P20RA10;

/*************************************************************************/
/*                                                                       */
/*  Wildcat BOARD 1 PAL: HIB PARITY PAL                                  */
/*                                                                       */
/*  REVISION HISTORY:                                                    */
/*       never was one never will be one... I has spokin                 */
/*                                                                       */
/*  Rev 1 -- 9/7/88 - modified clock equation in HIB PERR clk thus       */
/*                    changing HIB PERR from pulse to a level so we      */
/*                    don't drop this error inside the MEMERR pal        */
/*                    under simultaneous error assertions                */
/*                                                                       */
/*  Rev 2 -- 9/9/88 - reversed dip pinning between VAL BM1 & XIC PERR    */
/*                                                                       */
/*  Rev 3 -- 9/20/88 - correct VAL BM equation so DeMorgan doesn't       */
/*                     blow polarity fuse thus inverting VAL BM output   */
/*************************************************************************/
/*                                                                       */
/*       CUPL Rules of Thumb used herein:                                */
/*         2) Noninverted outputs (without '!') indicate state           */
/*            at latch Q output, or from polarity XOR if pass-thru.      */
/*         3) Inverting an entire expression should blow polarity fuse.  */
/*         4) Due to output lines being declared with '!' (by            */
/*            definition), feedback lines will have opposite polarity    */
/*            than inputs when used in logic equations.                  */
/*                                                                       */
/*************************************************************************/


/**  INPUTS  **/

pin 2  = XIC_PERR0_L;              /* plcc pin 3   */
pin 3  = XIC_PERR1_L;              /* plcc pin 4   */
pin 4  = XIC_PERR2_L;              /* plcc pin 5   */
pin 5  = XIC_PERR3_L;              /* plcc pin 6   */
pin 6  = CXHIC_PERR_L;             /* plcc pin 7   */
pin 7  = HIB_BM0_L;                /* plcc pin 9   */
pin 8  = HIB_BM1_L;                /* plcc pin 10  */
pin 9  = HIB_BM2_L;                /* plcc pin 11  */
pin 10 = HIB_BM3_L;                /* plcc pin 12  */
pin 11 = XIC_ERR_RESET_L;          /* plcc pin 13  */
pin 14 = BUSCLK;                   /* plcc pin 17  */
pin 15 = HIB_TO_DPC_L;             /* plcc pin 18  */
pin 16 = HIB_TO_CXHIC_L;           /* plcc pin 19  */


/* pin 1  = Vccr 40 H                 plcc pin 2        preload default     */
/* pin 13 = Rgnd 21 L                 plcc pin 16       output enable def.  */


/**  OUTPUTS  **/


pin 23 = !REG_CXHIC_PERR_L;        /* plcc pin 27  */
pin 22 = !HIB_PERR_L;              /* plcc pin 26  */
pin 21 = VAL_BM3;                  /* plcc pin 25  */
pin 20 = VAL_BM2;                  /* plcc pin 24  */
pin 19 = VAL_BM1;                  /* plcc pin 23  */
pin 18 = VAL_BM0;                  /* plcc pin 21  */
pin 17 = !XIC_PERR_L;              /* plcc pin 20  */


/**  LOGIC EQUATIONS  **/

     /* THE DPC's AS286 PARITY GENERATOR/CHECKERS PERFORM AS FOLLOWS:  */
      /* DPC XISM OPERATIONS: Writes - parity generation no checking */
      /*                      Reads - parity checking and error detection */
      /* CVAX OPERATIONS: Writes -parity checking and error detection */
      /*                  Reads - parity generation no checking */
```

20RA10SL_PARR4.PLD continued..

```
/* Since the HIB BMs are only valid during next grant cycles they are */
/* registered to provide correct info during error detection portion  */
/* the grant cycle    */

VAL_BM0.D       = !HIB_BM0_L;    /* If HIB BM = 0, then assert VAL BM = 1 */
VAL_BM0.CK      = BUSCLK;         /* Clocked on rising edge (0->1) of Busclk */
                                  /* at the beginning of the grant cycle  */
VAL_BM1.D       = !HIB_BM1_L;
VAL_BM1.CK      = BUSCLK;

VAL_BM2.D       = !HIB_BM2_L;
VAL_BM2.CK      = BUSCLK;

VAL_BM3.D       = !HIB_BM3_L;
VAL_BM3.CK      = BUSCLK;

        /* This error will be generated by: */
        /* 1) CXHIC write to data buffer mem -- DPC calc EDC */
        /* 2) CXHIC read of data buffer mem -- DPC chk EDC */
        /* 3) XISM work block polling    */
        /* 4) CXHIC determination of HIB DATA Parity Error */
        /* 5) CVAX write to XIC    */

XIC_PERR_L      = HIB_PERR_L              /* Assert if Hib Perr asserted */
                  #
                  REG_CXHIC_PERR_L       /* or if CXHIC Perr is asserted */
                  #
                  XIC_PERR_L &           /* or if Feedback latch up asserted */
                  XIC_ERR_RESET_L;       /* and error reset not asserted  */
                                         /* Maintains the error assertion */
                                         /* until cleared by sftwr servicing */

/* The CXHIC provides an async. parity error signal so it is  */
/* sampled and registered inside of this pal  */

REG_CXHIC_PERR_L.D  =(CXHIC_PERR_L &     /* CXHIC detected parity error */
                      !HIB_TO_CXHIC_L;   /* and operation involving CXHIC */

REG_CXHIC_PERR_L.CK = BUSCLK;             /* Clocked on rising edge (0->1) */
                                          /* of Busclk at end of grant cycle */

REG_CXHIC_PERR_L.AR = !XIC_ERR_RESET_L;   /* asserted by WR Diag Reg after */
                                          /* error serviced by software  */

/* Every time data is read into the DPC the 74AS286 are checking byte */
/* parity.  These devices provide most of the HIB BUS error detection */

HIB_PERR_L.D    = !HIB_TO_DPC_L &         /* Hib to DPC asserted - DPC xcvr ena*/
                  !XIC_PERR0_L &          /* and XIC Perr 0 is asserted by 286 */
                   VAL_BM0                /* and the byte mask is valid */
                   #
                  !HIB_TO_DPC_L &
                  !XIC_PERR1_L &
                   VAL_BM1
                   #
                  !HIB_TO_DPC_L &
                  !XIC_PERR2_L &
                   VAL_BM2
                   #
                  !HIB_TO_DPC_L &
                  !XIC_PERR3_L &
                   VAL_BM3;

HIB_PERR_L.CK   = BUSCLK &                /* clock the register at the end of */
                  !HIB_PERR_L;            /* grant cycle when Busclk goes 0->1 */
                                          /* and we aren't in an error state   */

HIB_PERR_L.AR   = !XIC_ERR_RESET_L;       /* Cleared by bit clr then bit set in */
                                          /* Wrt Diag by sftw servicing routine */
```


REVISIONS: CHK | CHANGE NO. | REV

[Documentation]
PAL EQN FILES:
20RA10SL_PARR4.PLD

digital

Thu Oct 20 17:06:13 1988

FIRST USED ON OPTION/MODEL: -

DRN: K. Yesse	DATE -	ENG: W. Chewbacca	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
		SHEET 44	
		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

File: 20RA10SL_XSYNC.PLD
Source: DISK$HSBSIM_B:[SIMULATION.CMS]

```
NAME          XSYNC;
PARTNO        23-000J8-01;
REVISION      00;
DATE          6/21/88;
DESIGNER      Versace;
COMPANY       DEC;
ASSEMBLY      Wildcat board 1;
LOCATION      E39;
DEVICE        P20RA10;

/*************************************************************************/
/*                                                                       */
/*  Wildcat BOARD 1 PAL: XIC Synchronization PAL                         */
/*                                                                       */
/*  REVISION HISTORY:                                                    */
/*                                                                       */
/*************************************************************************/
/*                                                                       */
/*      CUPL Rules of Thumb used herein:                                 */
/*        2) Noninverted outputs (without '!') indicate state            */
/*           at latch Q output, or from polarity XOR if pass-thru.       */
/*        3) Inverting an entire expression should blow polarity fuse.   */
/*        4) Due to output lines being declared with '!' (by             */
/*           definition), feedback lines will have opposite polarity     */
/*           than inputs when used in logic equations.                   */
/*                                                                       */
/*************************************************************************/

/* 8/17/88 - registered dma_req so glitches on prom address lines do not
             assert dma req to cxhic                                     */

/**  INPUTS  **/

pin 2  = BUSCLK;                /* plcc pin 3  */
pin 3  = XIC_NXT_GRT_L;         /* plcc pin 4  */
pin 4  = CRAM_TST_DIS;          /* plcc pin 5  */
pin 5  = XCI_REQ_L;             /* plcc pin 6  */
pin 6  = XIC_PERR_L;            /* plcc pin 7  */
pin 7  = XIC_CXHIC_CS_L;        /* plcc pin 9  */
pin 8  = XISM_CS_L;             /* plcc pin 10 */
pin 9  = CXHIC_CS_L;            /* plcc pin 11 */
pin 10 = DPC_CS_L;              /* plcc pin 12 */
pin 11 = HIB_WR_L;              /* plcc pin 13 */
pin 15 = HACK;                  /* plcc pin 18 */

/* pin 1  = Vccr 32 H             plcc pin 2     preload default     */
/* pin 13 = Rgnd 16 L             plcc pin 16    output enable def.  */

/**  OUTPUTS  **/

pin 14 = SPARE14;               /* plcc pin 17 */
pin 16 = !DMA_REQ_L;            /* plcc pin 19 */
pin 17 = !SYNC_XISM_CS_L;       /* plcc pin 20 */
pin 18 = !SYNC_CXHIC_CS_L;      /* plcc pin 21 */
pin 19 = !SYNC_DPC_CS_L;        /* plcc pin 23 */
pin 20 = !STR_XISM_CS_L;        /* plcc pin 24 */
pin 21 = !STR_CXHIC_CS_L;       /* plcc pin 25 */
pin 22 = !STR_DPC_CS_L;         /* plcc pin 26 */
pin 23 = !STR_WR_L;             /* plcc pin 27 */


/**  LOGIC EQUATIONS  **/

/* SYNC_DPC_CS is alway = 1 by means of an external pullup resisitor, */
/* until next grant asserts then it = 0.  When next grant deasserts   */
/* so does SYNC_DPC_CS_L */

SYNC_DPC_CS_L.D    =  !DPC_CS_L;            /* DPC CS asserted */

SYNC_DPC_CS_L.OE   =  !XIC_NXT_GRT_L;       /* output enabled when asserted */

SYNC_DPC_CS_L.CK   =  BUSCLK & HACK;        /* clocked 0 -> 1 */

STR_DPC_CS_L.D     =  SYNC_DPC_CS_L;        /* SYNC DPC CS asserted */

STR_DPC_CS_L.CK    =  BUSCLK;               /* clocked 0 -> 1 */
```

20RA10SL_XSYNC.PLD continued..

```
/* Like sync dpc cs, SYNC_XISM_CS is alway = 1 until next grant */
/* asserts then it = 0. When next grant deasserts, CS deasserts */

SYNC_XISM_CS_L.D    =  !XISM_CS_L;          /* XISM CS asserted */

SYNC_XISM_CS_L.OE   =  !XIC_NXT_GRT_L;      /* output enabled when asserted */

SYNC_XISM_CS_L.CK   =  BUSCLK & HACK;       /* clocked 0 -> 1 */

STR_XISM_CS_L.D     =  SYNC_XISM_CS_L;      /* SYNC XISM CS asserted */

STR_XISM_CS_L.CK    =  BUSCLK;              /* clocked 0 -> 1 */

/* NOTE: SYNC_CXHIC_CS is alway = 1 until next grant asserts then = 0 */
/* until next grant deasserts */

SYNC_CXHIC_CS_L.D   =  !CXHIC_CS_L;         /* CXHIC CS asserted */

SYNC_CXHIC_CS_L.OE  =  !XIC_NXT_GRT_L;      /* output enabled when asserted */

SYNC_CXHIC_CS_L.CK  =  BUSCLK & HACK;       /* clocked 0 -> 1 */

STR_CXHIC_CS_L.D    =  SYNC_CXHIC_CS_L;     /* SYNC CXHIC CS asserted */

STR_CXHIC_CS_L.CK   =  BUSCLK;              /* clocked 0 -> 1 */

STR_WR_L.D          =  !HIB_WR_L;           /* HIB WR asserted */

STR_WR_L.CK         =  BUSCLK;              /* clocked 0 -> 1 */

/* this signal tells the CXHIC to kick off an XMI transfer */

DMA_REQ_L.D         =  !XCI_REQ_L &         /* Asserted */
                       !CRAM_TST_DIS &      /* deasserted */
                       XIC_PERR_L;          /* deasserted */

DMA_REQ_L.CK        =  BUSCLK;              /* clocked 0 -> 1 */
```


REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]
PAL EQN FILES:
20RA10SL_XSYNC.PLD

digital

DRN: K. Yesse	DATE -	ENG: W. Chewbacca	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
- Thu Oct 20 17:06:19 1988		SHEET 45	
FIRST USED ON OPTION/MODEL: -		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

Output Sources for nets listed in cross-reference available upon request

Output Source Key: o> general output t> tristate output b> bidirectional output

ACLKA H:
E63-30 p.7
o>E117-35 p.6
E126-4 p.6
E126-11 p.6
E_43-1 p.26
ACLKB H:
E113-2 p.6
o>E117-38 p.6
E150-2 p.9
E151-3 p.9
E_44-1 p.26
ACLKC H:
E38-10 p.16
E104-12 p.10
o>E117-32 p.6
E119-11 p.9
E146-1 p.9
b>E146-20 p.9
E150-1 p.9
E151-2 p.9
E153-12 p.6
E_45-1 p.26
ADAMS PULLUP H:
E30-65 p.23
R270-2 p.28
ADDR 00 H:
t>E14-4 p.19
E19-3 p.19
ADDR 01 H:
t>E14-7 p.19
E19-4 p.19
ADDR 02 H:
t>E14-9 p.19
E19-5 p.19
ADDR 03 H:
t>E14-12 p.19
E19-6 p.19
ADDR 04 H:
t>E2-4 p.19
E19-7 p.19
ADDR 05 H:
t>E2-7 p.19
E19-9 p.19
ADDR 06 H:
t>E2-9 p.19
E19-10 p.19
ADDR 07 H:
t>E2-12 p.19
E19-11 p.19
ADDR INCR H:
t>E39-9 p.21
E40-N14 p.20
b>E42-14 p.21
ADDR LATCH L:
E18-17 p.18
E25-17 p.18
o>E40-B4 p.20
ADDR SRC 0 H:
t>E39-7 p.21
E40-P14 p.20
b>E42-15 p.21
ADDR SRC 1 H:
t>E39-5 p.21
E40-P13 p.20
E42-16 p.21
ANAL TRIG L:
D_29-1 p.26
o>E92-62 p.7
AS L:
E76-13 p.8
E89-13 p.8
E92-1 p.7
E107-13 p.8
E112-13 p.9
E119-17 p.9
R148-2 p.6
AS ST L:
b>E91-30 p.6
R148-1 p.6
BK2 BY0 CS L:
E74-11 p.13
E75-11 p.13
E77-13 p.13
o>E85-11 p.13
BK2 BY1 CS L:
o>E85-6 p.13
E96-11 p.13
E97-11 p.13
E100-13 p.13
BK2 BY2 CS L:
o>E85-8 p.13
E114-13 p.13
E115-11 p.13
E116-11 p.13
BK2 BY3 CS L:
o>E85-3 p.13
E143-13 p.13
E144-11 p.13
E145-11 p.13
BM 0 L:
o>E91-46 p.6
E112-3 p.9
BM 1 L:
o>E91-45 p.6
E112-4 p.9
BM 2 L:
o>E91-44 p.6
E112-5 p.9
BM 3 L:
o>E91-43 p.6
E112-6 p.9
BOOT ROM CS L:
o>E92-72 p.7
E158-20 p.7
E_29-1 p.26
BRD1 GRANT L:
t>E15-18 p.17
BRD1 NXT L:
E10-3 p.19
E15-12 p.17
E61-3 p.17
E_10-1 p.26
BRD2 ACT L:
E5-17 p.18
b>E20-17 p.17
E22-17 p.18
E103-4 p.11
t>E137-18 p.8
E146-25 p.9
E_41-1 p.26
BRD2 BUSCLK H:
t>E119-14 p.6
J3-4 p.27
BRD2 CS L:
E23-5 p.19
E59-10 p.17
E95-14 p.10
b>E137-23 p.8
BRD2 EE CLK H:
J3-7 p.27
BRD2 EE DATA H:
J3-49 p.27
BRD2 EE RD DATA H:
J3-85 p.27
BRD2 EE WR H:
J3-79 p.27
BRD2 RESET L:
t>E69-17 p.10
J3-90 p.27
BUF 40MHZ H:
E134-10 p.6
o>E134-11 p.6
BUF AS L:
E38-2 p.16
E63-47 p.7
E118-17 p.8
t>E119-3 p.9
E122-17 p.8
E137-17 p.8
E146-4 p.9
E150-4 p.9
E151-6 p.9
E152-1 p.8
E_60-1 p.26
BUF DBE L:
E20-7 p.17
t>E119-7 p.9
E151-1 p.9
E_58-1 p.26
BUF DS L:
E63-41 p.7
E104-13 p.10
E117-16 p.6
t>E119-5 p.9
E146-3 p.9
E150-3 p.9
E151-4 p.9
E_59-1 p.26
BUSCLK H:
E9-16 p.19
E11-16 p.17
E15-16 p.17
E18-16 p.18
b>E20-19 p.17
b>E24-17 p.17
E25-16 p.18
E38-9 p.16
E41-3 p.17
t>E119-18 p.6
E146-27 p.9
BUSCLK L:
E8-16 p.19
E10-7 p.19
E19-16 p.19
E23-16 p.19
E31-1 p.17
o>E58-3 p.6
CAB H:
E21-2 p.16
E33-2 p.16
b>E38-23 p.16
E44-2 p.16
E46-2 p.16
E56-2 p.16
CADDR 02 H:
E22-3 p.18
E43-9 p.22
E68-11 p.15
E70-11 p.15
E82-11 p.15
E83-11 p.15
E98-11 p.15
E99-11 p.15
E110-11 p.15
E111-11 p.15
E121-7 p.9
E128-11 p.15
E129-11 p.15
E142-13 p.9
E147-11 p.15
E148-11 p.15
E158-8 p.7
R150-2 p.8
CADDR 02 ST H:
t>E107-23 p.8
R150-1 p.8
CADDR 03 H:
E22-4 p.18
E43-8 p.22
E66-2 p.14
E67-2 p.14
E68-10 p.15
E70-10 p.15
E71-2 p.14
E74-2 p.13
E75-2 p.13
E77-2 p.13
E78-2 p.12
E79-2 p.12
E82-10 p.15
E83-10 p.15
E86-2 p.14
E87-2 p.14
E93-2 p.14
E96-2 p.13
E97-2 p.13
E98-10 p.15
E99-10 p.15
E100-2 p.13
E101-2 p.12
E102-2 p.12
E105-2 p.14
E108-2 p.14
E109-2 p.14
E110-10 p.15
E111-10 p.15
E114-2 p.13
E115-2 p.13
E116-2 p.13
E121-8 p.9
E124-2 p.12
E125-2 p.12
E128-10 p.15
E129-10 p.15
E131-2 p.14
E132-2 p.14
E133-2 p.14
E143-2 p.13
E144-2 p.13
E145-2 p.13
E147-10 p.15
E148-10 p.15
E155-2 p.12
E156-2 p.12
E157-2 p.12
E158-7 p.7
R114-2 p.8
CADDR 03 ST H:
t>E107-22 p.8
R114-1 p.8
CADDR 04 H:
E22-5 p.18
E43-7 p.22
E66-3 p.14
E67-3 p.14
E68-9 p.15
E70-9 p.15
E71-3 p.14
E74-3 p.13
E75-3 p.13
E77-3 p.13
E78-3 p.12
E79-3 p.12
E82-9 p.15
E83-9 p.15
E86-3 p.14
E87-3 p.14
E93-3 p.14
E96-3 p.13
E97-3 p.13
E98-9 p.15
E99-9 p.15
E100-3 p.13
E101-3 p.12
E102-3 p.12
E105-3 p.14
E108-3 p.14
E109-3 p.14
E110-9 p.15
E111-9 p.15
E114-3 p.13
E115-3 p.13
E116-3 p.13
E121-13 p.9
E124-3 p.12
E125-3 p.12
E128-9 p.15
E129-9 p.15
E131-3 p.14
E132-3 p.14
E133-3 p.14
E143-3 p.13
E144-3 p.13
E145-3 p.13
E147-9 p.15
E148-9 p.15
E155-3 p.12
E156-3 p.12
E157-3 p.12
E158-6 p.7
R128-2 p.8
CADDR 04 ST H:
t>E107-21 p.8
R128-1 p.8
CADDR 05 H:
E22-6 p.18
E43-6 p.22
E66-4 p.14
E67-4 p.14
E68-8 p.15
E70-8 p.15
E71-4 p.14
E74-4 p.13
E75-4 p.13
E77-4 p.13
E78-4 p.12
E79-4 p.12
E82-8 p.15
E83-8 p.15
E86-4 p.14
E87-4 p.14
E93-4 p.14
E96-4 p.13
E97-4 p.13
E98-8 p.15
E99-8 p.15
E100-4 p.13
E101-4 p.12
E102-4 p.12
E105-4 p.14
E108-4 p.14
E109-4 p.14
E110-8 p.15
E111-8 p.15
E114-4 p.13
E115-4 p.13
E116-4 p.13
E121-14 p.9
E124-4 p.12
E125-4 p.12
E128-8 p.15
E129-8 p.15
E131-4 p.14
E132-4 p.14
E133-4 p.14
E143-4 p.13
E144-4 p.13
E145-4 p.13
E147-8 p.15
E148-8 p.15
E155-4 p.12
E156-4 p.12
E157-4 p.12
E158-5 p.7
R127-2 p.8
CADDR 05 ST H:
t>E107-20 p.8
R127-1 p.8
CADDR 06 H:
E22-7 p.18
E43-5 p.22
E66-5 p.14
E67-5 p.14
E68-7 p.15
E70-7 p.15
E71-5 p.14
E74-5 p.13
E75-5 p.13
E77-5 p.13
E78-5 p.12
E79-5 p.12
E82-7 p.15
E83-7 p.15
E86-5 p.14
E87-5 p.14
E93-5 p.14
E96-5 p.13
E97-5 p.13
E98-7 p.15
E99-7 p.15
E100-5 p.13
E101-5 p.12
E102-5 p.12
E105-5 p.14
E108-5 p.14
E109-5 p.14
E110-7 p.15
E111-7 p.15
E114-5 p.13
E115-5 p.13
E116-5 p.13
E121-17 p.9
E124-5 p.12
E125-5 p.12
E128-7 p.15
E129-7 p.15
E131-5 p.14
E132-5 p.14
E133-5 p.14
E143-5 p.13
E144-5 p.13
E145-5 p.13
E147-7 p.15
E148-7 p.15
E155-5 p.12
E156-5 p.12
E157-5 p.12
E158-4 p.7
R137-2 p.8
CADDR 06 ST H:
t>E107-19 p.8
R137-1 p.8
CADDR 07 H:
E22-9 p.18
E43-4 p.22
E66-6 p.14
E67-6 p.14
E68-6 p.15
E70-6 p.15
E71-6 p.14
E74-6 p.13
E75-6 p.13
E77-6 p.13
E78-6 p.12
E79-6 p.12
E82-6 p.15
E83-6 p.15
E86-6 p.14
E87-6 p.14
E93-6 p.14
E96-6 p.13
E97-6 p.13
E98-6 p.15
E99-6 p.15
E100-6 p.13
E101-6 p.12
E102-6 p.12
E105-6 p.14
E108-6 p.14
E109-6 p.14
E110-6 p.15
E111-6 p.15
E114-6 p.13
E115-6 p.13
E116-6 p.13
E121-18 p.9
E124-6 p.12
E125-6 p.12
E128-6 p.15
E129-6 p.15
E131-6 p.14
E132-6 p.14
E133-6 p.14
E143-6 p.13
E144-6 p.13
E145-6 p.13
E147-6 p.15
E148-6 p.15
E155-6 p.12
E156-6 p.12
E157-6 p.12
E158-3 p.7
R113-2 p.8
CADDR 07 ST H:
t>E107-18 p.8
R113-1 p.8
CADDR 08 H:
E22-10 p.18
E43-3 p.22
E66-7 p.14
E67-7 p.14
E68-5 p.15
E70-5 p.15
E71-8 p.14
E74-7 p.13
E75-7 p.13
E77-8 p.13
E78-7 p.12
E79-7 p.12
E82-5 p.15
E83-5 p.15
E86-7 p.14
E87-7 p.14
E93-8 p.14
E96-7 p.13
E97-7 p.13
E98-5 p.15
E99-5 p.15
E100-8 p.13
E101-7 p.12
E102-7 p.12
E105-8 p.14
E108-7 p.14
E109-7 p.14
E110-5 p.15
E111-5 p.15
E114-8 p.13
E115-7 p.13
E116-7 p.13
E124-7 p.12
E125-7 p.12
E128-5 p.15
E129-5 p.15
E131-8 p.14
E132-7 p.14
E133-7 p.14
E138-3 p.9
E143-8 p.13
E144-7 p.13
E145-7 p.13
E147-5 p.15
E148-5 p.15
E155-7 p.12
E156-7 p.12
E157-7 p.12
E158-25 p.7
R136-2 p.8
CADDR 08 ST H:
t>E107-17 p.8
R136-1 p.8
CADDR 09 H:
E22-11 p.18
E66-8 p.14
E67-8 p.14
E68-4 p.15
E70-4 p.15
E71-9 p.14
E74-8 p.13
E75-8 p.13
E77-9 p.13
E78-8 p.12
E79-8 p.12
E82-4 p.15
E83-4 p.15
E86-8 p.14
E87-8 p.14
E93-9 p.14
E96-8 p.13
E97-8 p.13
E98-4 p.15
E99-4 p.15
E100-9 p.13
E101-8 p.12
E102-8 p.12
E105-9 p.14
E108-8 p.14
E109-8 p.14
E110-4 p.15
E111-4 p.15
E114-9 p.13
E115-8 p.13
E116-8 p.13
E124-8 p.12
E125-8 p.12
E128-4 p.15
E129-4 p.15
E131-9 p.14
E132-8 p.14
E133-8 p.14
E138-4 p.9
E143-9 p.13
E144-8 p.13
E145-8 p.13
E147-4 p.15
E148-4 p.15
E155-8 p.12
E156-8 p.12
E157-8 p.12
E158-24 p.7
R126-2 p.8
CADDR 09 ST H:
t>E107-16 p.8
R126-1 p.8
CADDR 10 H:
E22-12 p.18
E66-9 p.14
E67-9 p.14
E68-29 p.15
E70-29 p.15
E71-15 p.14
E74-9 p.13
E75-9 p.13
E77-15 p.13
E78-9 p.12
E79-9 p.12
E82-29 p.15
E83-29 p.15
E86-9 p.14
E87-9 p.14
E93-15 p.14
E96-9 p.13
E97-9 p.13
E98-29 p.15
E99-29 p.15
E100-15 p.13
E101-9 p.12
E102-9 p.12
E105-15 p.14
E108-9 p.14
E109-9 p.14
E110-29 p.15
E111-29 p.15
E114-15 p.13
E115-9 p.13
E116-9 p.13
E118-1 p.8
E124-9 p.12
E125-9 p.12
E128-29 p.15
E129-29 p.15
E131-15 p.14
E132-9 p.14
E133-9 p.14
E137-1 p.8
E138-7 p.9
E143-15 p.13
E144-9 p.13
E145-9 p.13
E147-29 p.15
E148-29 p.15
E155-9 p.12
E156-9 p.12
E157-9 p.12
E158-21 p.7
R135-2 p.8
CADDR 10 ST H:
t>E107-15 p.8
R135-1 p.8
CADDR 11 H:
E5-3 p.18
E66-10 p.14
E67-10 p.14
E68-28 p.15
E70-28 p.15
E71-16 p.14
E74-10 p.13
E75-10 p.13
E77-16 p.13
E78-10 p.12
E79-10 p.12
E82-28 p.15
E83-28 p.15
E86-10 p.14
E87-10 p.14
E93-16 p.14
E96-10 p.13
E97-10 p.13
E98-28 p.15
E99-28 p.15
E100-16 p.13
E101-10 p.12
E102-10 p.12
E105-16 p.14
E108-10 p.14
E109-10 p.14
E110-28 p.15
E111-28 p.15
E114-16 p.13
E115-10 p.13
E116-10 p.13
E118-2 p.8
E124-10 p.12
E125-10 p.12
E128-28 p.15
E129-28 p.15
E131-16 p.14
E132-10 p.14
E133-10 p.14
E137-2 p.8
E138-8 p.9
E143-16 p.13
E144-10 p.13
E145-10 p.13
E147-28 p.15
E148-28 p.15
E155-10 p.12
E156-10 p.12
E157-10 p.12
E158-23 p.7
R112-2 p.8
CADDR 11 ST H:
t>E107-14 p.8
R112-1 p.8
CADDR 12 H:
E5-4 p.18
E66-18 p.14
E67-18 p.14
E68-24 p.15
E70-24 p.15
E71-17 p.14
E74-18 p.13
E75-18 p.13
E77-17 p.13
E78-18 p.12
E79-18 p.12
E82-24 p.15
E83-24 p.15
E86-18 p.14
E87-18 p.14
E93-17 p.14
E96-18 p.13
E97-18 p.13
E98-24 p.15
E99-24 p.15
E100-17 p.13
E101-18 p.12
E102-18 p.12
E105-17 p.14
E108-18 p.14
E109-18 p.14
E110-24 p.15
E111-24 p.15
E114-17 p.13
E115-18 p.13
E116-18 p.13
E118-3 p.8
E124-18 p.12
E125-18 p.12
E128-24 p.15
E129-24 p.15
E131-17 p.14
E132-18 p.14
E133-18 p.14
E137-3 p.8
E138-13 p.9
E143-17 p.13
E144-18 p.13
E145-18 p.13
E147-24 p.15
E148-24 p.15
E155-18 p.12
E156-18 p.12
E157-18 p.12
E158-2 p.7
R207-2 p.8
CADDR 12 ST H:
t>E76-23 p.8
R207-1 p.8
CADDR 13 H:
E5-5 p.18
E66-19 p.14
E67-19 p.14
E68-27 p.15
E70-27 p.15
E71-18 p.14
E74-19 p.13
E75-19 p.13
E77-18 p.13
E78-19 p.12
E79-19 p.12
E82-27 p.15
E83-27 p.15
E86-19 p.14
E87-19 p.14
E93-18 p.14
E96-19 p.13
E97-19 p.13
E98-27 p.15
E99-27 p.15
E100-18 p.13
E101-19 p.12
E102-19 p.12
E105-18 p.14
E108-19 p.14
E109-19 p.14
E110-27 p.15
E111-27 p.15
E114-18 p.13
E115-19 p.13
E116-19 p.13
E118-4 p.8
E124-19 p.12
E125-19 p.12
E128-27 p.15
E129-27 p.15
E131-18 p.14
E132-19 p.14
E133-19 p.14
E137-4 p.8
E138-14 p.9
E143-18 p.13
E144-19 p.13
E145-19 p.13
E147-27 p.15
E148-27 p.15
E155-19 p.12
E156-19 p.12
E157-19 p.12
E158-26 p.7
R197-2 p.8
CADDR 13 ST H:
t>E76-22 p.8
R197-1 p.8
CADDR 14 H:
E5-6 p.18
E66-20 p.14
E67-20 p.14
E68-3 p.15
E70-3 p.15
E71-20 p.14
E74-20 p.13
E75-20 p.13
E77-20 p.13
E78-20 p.12
E79-20 p.12
E82-3 p.15
E83-3 p.15
E86-20 p.14
E87-20 p.14
E93-20 p.14
E96-20 p.13
E97-20 p.13
E98-3 p.15
E99-3 p.15
E100-20 p.13
E101-20 p.12
E102-20 p.12
E105-20 p.14
E108-20 p.14
E109-20 p.14
E110-3 p.15
E111-3 p.15
E114-20 p.13
E115-20 p.13
E116-20 p.13
E118-6 p.8
E124-20 p.12
E125-20 p.12
E128-3 p.15

REVISIONS

CHK	CHANGE NO.	REV

[Documentation]

CROSS REFERENCE:
Signal Names

DRN: K. Yesse - DATE -
CHK'D: - DATE -
ENG: C. Threepio - DATE -
BOARD LOCATION: CXO
SHEET 50
NEXT HIGHER ASSEMBLY: -
- Thu Oct 20 17:07:03 1988
FIRST USED ON OPTION/MODEL: -

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

Output Sources for nets listed in cross-reference available upon request

Output Source Key: o> general output t> tristate output b> bidirectional output

E129-3 p.15
E131-20 p.14
E132-20 p.14
E133-20 p.14
E137-6 p.8
E138-17 p.9
E143-20 p.13
E144-20 p.13
E145-20 p.13
E147-3 p.15
E148-3 p.15
E155-20 p.12
E156-20 p.12
E157-20 p.12
E158-27 p.7
R204-2 p.8
CADDR 14 ST H:
▷E76-21 p.8
R204-1 p.8
CADDR 15 H:
E5-7 p.18
E66-21 p.14
E67-21 p.14
E68-30 p.15
E70-30 p.15
E71-21 p.14
E74-21 p.13
E75-21 p.13
E77-21 p.13
E78-21 p.12
E79-21 p.12
E82-30 p.15
E83-30 p.15
E86-21 p.14
E87-21 p.14
E93-21 p.14
E96-21 p.13
E97-21 p.13
E98-30 p.15
E99-30 p.15
E100-21 p.13
E101-21 p.12
E102-21 p.12
E105-21 p.14
E108-21 p.14
E109-21 p.14
E110-30 p.15
E111-30 p.15
E114-21 p.13
E115-21 p.13
E116-21 p.13
E118-7 p.8
E124-21 p.12
E125-21 p.12
E128-30 p.15
E129-30 p.15
E131-21 p.14
E132-21 p.14
E133-21 p.14
E137-7 p.8
E138-18 p.9
E143-21 p.13
E144-21 p.13
E145-21 p.13
E147-30 p.15
E148-30 p.15
E155-21 p.12
E156-21 p.12
E157-21 p.12
R196-2 p.8
CADDR 15 ST H:
▷E76-20 p.8
R196-1 p.8
CADDR 16 H:
E5-9 p.18
E66-22 p.14
E67-22 p.14
E68-2 p.15
E70-2 p.15
E71-22 p.14
E74-22 p.13
E75-22 p.13
E77-22 p.13
E78-22 p.12
E79-22 p.12
E82-2 p.15

E83-2 p.15
E86-22 p.14
E87-22 p.14
E93-22 p.14
E96-22 p.13
E97-22 p.13
E98-2 p.15
E99-2 p.15
E100-22 p.13
E101-22 p.12
E102-22 p.12
E105-22 p.14
E108-22 p.14
E109-22 p.14
E110-2 p.15
E111-2 p.15
E114-22 p.13
E115-22 p.13
E116-22 p.13
E118-9 p.8
E124-22 p.12
E125-22 p.12
E128-2 p.15
E129-2 p.15
E131-22 p.14
E132-22 p.14
E133-22 p.14
E136-3 p.9
E137-9 p.8
E143-22 p.13
E144-22 p.13
E145-22 p.13
E147-2 p.15
E148-2 p.15
E155-22 p.12
E156-22 p.12
E157-22 p.12
R211-2 p.8
CADDR 16 ST H:
▷E76-19 p.8
R211-1 p.8
CADDR 17 H:
E5-10 p.18
E66-23 p.14
E67-23 p.14
E71-23 p.14
E74-23 p.13
E75-23 p.13
E77-23 p.13
E78-23 p.12
E79-23 p.12
E86-23 p.14
E87-23 p.14
E93-23 p.14
E96-23 p.13
E97-23 p.13
E100-23 p.13
E101-23 p.12
E102-23 p.12
E105-23 p.14
E108-23 p.14
E109-23 p.14
E115-23 p.13
E116-23 p.13
E118-10 p.8
E122-9 p.8
E124-23 p.12
E125-23 p.12
E131-23 p.14
E132-23 p.14
E133-23 p.14
E136-4 p.9
E137-10 p.8
E143-23 p.13
E144-23 p.13
E145-23 p.13
E155-23 p.12
E156-23 p.12
E157-23 p.12
R203-2 p.8
CADDR 17 ST H:
▷E76-18 p.8
R203-1 p.8
CADDR 18 H:
E5-11 p.18

E118-12 p.8
E122-10 p.8
E136-7 p.9
E137-12 p.8
R202-2 p.8
CADDR 18 ST H:
▷E76-17 p.8
R202-1 p.8
CADDR 19 H:
E5-12 p.18
E118-13 p.8
E122-12 p.8
E136-8 p.9
E137-13 p.8
R195-2 p.8
CADDR 19 ST H:
▷E76-16 p.8
R195-1 p.8
CADDR 20 H:
E118-14 p.8
E122-13 p.8
E136-13 p.9
E137-14 p.8
R209-2 p.8
CADDR 20 ST H:
▷E76-15 p.8
R209-1 p.8
CADDR 21 H:
E122-14 p.8
E136-14 p.9
▷E137-20 p.8
R200-2 p.8
CADDR 21 ST H:
▷E76-14 p.8
R200-1 p.8
CADDR 22 H:
E136-17 p.9
E152-3 p.8
R187-2 p.8
CADDR 22 ST H:
▷E89-23 p.8
R187-1 p.8
CADDR 23 H:
E136-18 p.9
E152-5 p.8
R164-2 p.8
CADDR 23 ST H:
▷E89-22 p.8
R164-1 p.8
CADDR 24 H:
E152-7 p.8
E154-3 p.9
R191-2 p.8
CADDR 24 ST H:
▷E89-21 p.8
R191-1 p.8
CADDR 25 H:
E152-9 p.8
E154-4 p.9
R179-2 p.8
CADDR 25 ST H:
▷E89-20 p.8
R179-1 p.8
CADDR 26 H:
E152-12 p.8
E154-7 p.9
R190-2 p.8
CADDR 26 ST H:
▷E89-19 p.8
R190-1 p.8
CADDR 27 H:
E152-14 p.8
E154-8 p.9
R189-2 p.8
CADDR 27 ST H:
▷E89-18 p.8
R189-1 p.8
CADDR 28 H:
E152-16 p.8
E154-13 p.9
R178-2 p.8
CADDR 28 ST H:
▷E89-17 p.8
R178-1 p.8
CADDR 29 H:
E118-16 p.8

E122-16 p.8
E137-16 p.8
E154-14 p.9
R163-2 p.8
CADDR 29 ST H:
▷E89-16 p.8
R163-1 p.8
CADDR 30 H:
E150-10 p.9
E154-17 p.9
R177-2 p.8
CADDR 30 ST H:
▷E89-15 p.8
R177-1 p.8
CADDR 31 H:
E150-12 p.9
E154-18 p.9
R162-2 p.8
CADDR 31 ST H:
▷E89-14 p.8
R162-1 p.8
CBA H:
E21-27 p.16
E33-27 p.16
▷E38-25 p.16
E44-27 p.16
E46-27 p.16
E56-27 p.16
CCLK RESET L:
o>E117-15 p.6
E135-13 p.6
CDAL 00 H:
D_47-1 p.26
▷E21-5 p.16
▷E63-62 p.7
E65-8 p.11
▷E66-17 p.14
▷E69-3 p.10
▷E74-17 p.13
▷E78-17 p.12
▷E92-39 p.7
▷E95-2 p.10
▷E111-13 p.15
▷E121-2 p.9
▷E129-13 p.15
▷E148-13 p.15
▷E158-11 p.7
R143-2 p.6
CDAL 00 ST H:
▷E91-47 p.6
R143-1 p.6
CDAL 01 H:
D_32-1 p.26
▷E21-6 p.16
▷E63-63 p.7
E65-9 p.11
▷E66-16 p.14
▷E69-4 p.10
▷E74-16 p.13
▷E78-16 p.12
▷E92-38 p.7
▷E95-5 p.10
▷E111-14 p.15
▷E121-5 p.9
▷E129-14 p.15
▷E148-14 p.15
▷E158-12 p.7
R142-2 p.6
CDAL 01 ST H:
▷E91-48 p.6
R142-1 p.6
CDAL 02 H:
D_48-1 p.26
▷E21-7 p.16
▷E63-64 p.7
E65-10 p.11
▷E66-15 p.14
▷E69-5 p.10
▷E74-15 p.13
▷E78-15 p.12
▷E92-37 p.7
▷E95-6 p.10
E107-2 p.8
▷E111-15 p.15
▷E121-6 p.9
▷E129-15 p.15

▷E148-15 p.15
▷E158-13 p.7
R141-2 p.6
CDAL 02 ST H:
▷E91-49 p.6
R141-1 p.6
CDAL 03 H:
D_33-1 p.26
▷E21-9 p.16
▷E63-65 p.7
E65-11 p.11
▷E66-14 p.14
▷E69-6 p.10
▷E74-14 p.13
▷E78-14 p.12
▷E92-36 p.7
▷E95-9 p.10
E107-3 p.8
▷E111-18 p.15
▷E121-9 p.9
▷E129-18 p.15
▷E148-18 p.15
▷E158-15 p.7
R138-2 p.6
CDAL 03 ST H:
▷E91-50 p.6
R138-1 p.6
CDAL 04 H:
D_49-1 p.26
▷E21-10 p.16
▷E63-66 p.7
E65-12 p.11
▷E67-17 p.14
▷E69-7 p.10
▷E75-17 p.13
▷E79-17 p.12
▷E92-35 p.7
▷E95-12 p.10
E107-4 p.8
▷E111-19 p.15
▷E121-12 p.9
▷E129-19 p.15
▷E148-19 p.15
▷E158-16 p.7
R119-2 p.6
CDAL 04 ST H:
▷E91-54 p.6
R119-1 p.6
CDAL 05 H:
D_34-1 p.26
▷E21-11 p.16
▷E63-67 p.7
E65-13 p.11
▷E67-16 p.14
▷E69-8 p.10
▷E75-16 p.13
▷E79-16 p.12
▷E92-34 p.7
▷E95-15 p.10
E107-5 p.8
▷E111-20 p.15
▷E121-15 p.9
▷E129-20 p.15
▷E148-20 p.15
▷E158-17 p.7
R121-2 p.6
CDAL 05 ST H:
▷E91-55 p.6
R121-1 p.6
CDAL 06 H:
D_50-1 p.26
▷E21-12 p.16
▷E63-68 p.7
E65-1 p.11
▷E67-15 p.14
▷E69-9 p.10
▷E75-15 p.13
▷E79-15 p.12
▷E92-31 p.7
▷E95-16 p.10
E107-6 p.8
▷E111-21 p.15
▷E121-16 p.9
▷E129-21 p.15
▷E148-21 p.15
▷E158-18 p.7

R131-2 p.6
CDAL 06 ST H:
▷E91-56 p.6
R131-1 p.6
CDAL 07 H:
D_35-1 p.26
▷E21-13 p.16
▷E63-1 p.7
E65-2 p.11
▷E67-14 p.14
▷E69-10 p.10
▷E75-14 p.13
▷E79-14 p.12
▷E92-30 p.7
▷E95-19 p.10
E107-7 p.8
▷E111-22 p.15
▷E121-19 p.9
▷E129-22 p.15
▷E148-22 p.15
▷E158-19 p.7
R133-2 p.6
CDAL 07 ST H:
▷E91-57 p.6
R133-1 p.6
CDAL 08 H:
D_51-1 p.26
▷E46-5 p.16
▷E63-2 p.7
E64-8 p.11
▷E70-13 p.15
▷E80-3 p.10
▷E84-2 p.10
▷E86-17 p.14
▷E92-29 p.7
▷E96-17 p.13
▷E98-13 p.15
▷E101-17 p.12
E107-8 p.8
▷E110-13 p.15
▷E138-2 p.9
R140-2 p.6
CDAL 08 ST H:
▷E91-58 p.6
R140-1 p.6
CDAL 09 H:
D_36-1 p.26
▷E46-6 p.16
▷E63-3 p.7
E64-9 p.11
▷E70-14 p.15
▷E80-4 p.10
▷E84-5 p.10
▷E86-16 p.14
▷E92-28 p.7
▷E96-16 p.13
▷E98-14 p.15
▷E101-16 p.12
E107-9 p.8
▷E110-14 p.15
▷E138-5 p.9
R151-2 p.6
CDAL 09 ST H:
▷E91-59 p.6
R151-1 p.6
CDAL 10 H:
D_52-1 p.26
▷E46-7 p.16
▷E63-4 p.7
E64-10 p.11
▷E70-15 p.15
▷E80-5 p.10
▷E84-6 p.10
▷E86-15 p.14
▷E92-27 p.7
▷E96-15 p.13
▷E98-15 p.15
▷E101-15 p.12
E107-10 p.8
▷E110-15 p.15
▷E138-6 p.9
R147-2 p.6
CDAL 10 ST H:
▷E91-60 p.6
R147-1 p.6
CDAL 11 H:

D_37-1 p.26
▷E46-9 p.16
▷E63-5 p.7
E64-11 p.11
▷E70-18 p.15
▷E80-6 p.10
▷E84-9 p.10
▷E86-14 p.14
▷E92-26 p.7
▷E96-14 p.13
▷E98-18 p.15
▷E101-14 p.12
E107-11 p.8
▷E110-18 p.15
▷E138-9 p.9
R153-2 p.6
CDAL 11 ST H:
▷E91-61 p.6
R153-1 p.6
CDAL 12 H:
D_53-1 p.26
▷E46-10 p.16
▷E63-6 p.7
E64-12 p.11
▷E70-19 p.15
▷E80-7 p.10
▷E84-12 p.10
▷E87-17 p.14
▷E92-25 p.7
▷E97-17 p.13
▷E98-19 p.15
▷E102-17 p.12
▷E110-19 p.15
▷E138-12 p.9
R155-2 p.6
CDAL 12 ST H:
▷E91-62 p.6
R155-1 p.6
CDAL 13 H:
D_38-1 p.26
▷E46-11 p.16
▷E63-7 p.7
E64-13 p.11
▷E70-20 p.15
▷E80-8 p.10
▷E84-15 p.10
▷E87-16 p.14
▷E92-24 p.7
▷E97-16 p.13
▷E98-20 p.15
▷E102-16 p.12
▷E110-20 p.15
▷E138-15 p.9
R161-2 p.6
CDAL 13 ST H:
▷E91-63 p.6
R161-1 p.6
CDAL 14 H:
D_54-1 p.26
▷E46-12 p.16
▷E63-8 p.7
E64-1 p.11
▷E70-21 p.15
E76-4 p.8
▷E80-9 p.10
▷E84-16 p.10
▷E87-15 p.14
▷E92-23 p.7
▷E97-15 p.13
▷E98-21 p.15
▷E102-15 p.12
▷E110-21 p.15
▷E138-16 p.9
R169-2 p.6
CDAL 14 ST H:
▷E91-64 p.6
R169-1 p.6
CDAL 15 H:
D_39-1 p.26
▷E46-13 p.16
▷E63-9 p.7
E64-2 p.11
▷E70-22 p.15
E76-5 p.8

▷E80-10 p.10
▷E84-19 p.10
▷E87-14 p.14
▷E92-22 p.7
▷E97-14 p.13
▷E98-22 p.15
▷E102-14 p.12
▷E110-22 p.15
▷E138-19 p.9
R157-2 p.6
CDAL 15 ST H:
▷E91-65 p.6
R157-1 p.6
CDAL 16 H:
D_55-1 p.26
▷E56-5 p.16
▷E68-13 p.15
▷E72-2 p.10
E73-8 p.11
E76-6 p.8
▷E82-13 p.15
▷E92-21 p.7
▷E99-13 p.15
▷E106-3 p.10
▷E108-17 p.14
▷E115-17 p.13
▷E124-17 p.12
▷E136-2 p.9
R172-2 p.6
CDAL 16 ST H:
▷E91-66 p.6
R172-1 p.6
CDAL 17 H:
D_40-1 p.26
▷E56-6 p.16
▷E68-14 p.15
▷E72-5 p.10
E73-9 p.11
E76-7 p.8
▷E82-14 p.15
▷E92-20 p.7
▷E99-14 p.15
▷E106-4 p.10
▷E108-16 p.14
▷E115-16 p.13
▷E124-16 p.12
▷E136-5 p.9
R174-2 p.6
CDAL 17 ST H:
▷E91-67 p.6
R174-1 p.6
CDAL 18 H:
D_56-1 p.26
▷E56-7 p.16
▷E68-15 p.15
▷E72-6 p.10
E73-10 p.11
E76-8 p.8
▷E82-15 p.15
▷E92-19 p.7
▷E99-15 p.15
▷E106-5 p.10
▷E108-15 p.14
▷E115-15 p.13
▷E124-15 p.12
▷E136-6 p.9
R185-2 p.6
CDAL 18 ST H:
▷E91-68 p.6
R185-1 p.6
CDAL 19 H:
D_41-1 p.26
▷E56-9 p.16
▷E68-18 p.15
▷E72-9 p.10
E73-11 p.11
E76-9 p.8
▷E82-18 p.15
▷E92-18 p.7
▷E99-18 p.15
▷E106-6 p.10
▷E108-14 p.14
▷E115-14 p.13
▷E124-14 p.12
▷E136-9 p.9
R165-2 p.6

CDAL 19 ST H:
▷E91-69 p.6
R165-1 p.6
CDAL 20 H:
D_57-1 p.26
▷E56-10 p.16
▷E68-19 p.15
▷E72-12 p.10
E73-12 p.11
E76-10 p.8
▷E82-19 p.15
▷E92-17 p.7
▷E99-19 p.15
▷E106-7 p.10
▷E109-17 p.14
▷E116-17 p.13
▷E125-17 p.12
▷E136-12 p.9
R170-2 p.6
CDAL 20 ST H:
▷E91-70 p.6
R170-1 p.6
CDAL 21 H:
D_42-1 p.26
▷E56-11 p.16
▷E68-20 p.15
▷E72-15 p.10
E73-13 p.11
E76-11 p.8
▷E82-20 p.15
▷E92-16 p.7
▷E99-20 p.15
▷E106-8 p.10
▷E109-16 p.14
▷E116-16 p.13
▷E125-16 p.12
▷E136-15 p.9
R173-2 p.6
CDAL 21 ST H:
▷E91-71 p.6
R173-1 p.6
CDAL 22 H:
D_58-1 p.26
▷E56-12 p.16
▷E68-21 p.15
▷E72-16 p.10
E73-1 p.11
▷E82-21 p.15
E89-2 p.8
▷E92-15 p.7
▷E99-21 p.15
▷E106-9 p.10
▷E109-15 p.14
▷E116-15 p.13
▷E125-15 p.12
▷E136-16 p.9
R188-2 p.6
CDAL 22 ST H:
▷E91-72 p.6
R188-1 p.6
CDAL 23 H:
D_43-1 p.26
▷E56-13 p.16
▷E68-22 p.15
▷E72-19 p.10
E73-2 p.11
▷E82-22 p.15
E89-3 p.8
▷E92-14 p.7
▷E99-22 p.15
▷E106-10 p.10
▷E109-14 p.14
▷E116-14 p.13
▷E125-14 p.12
▷E136-19 p.9
R192-2 p.6
CDAL 23 ST H:
▷E91-73 p.6
R192-1 p.6
CDAL 24 H:
D_59-1 p.26
▷E33-5 p.16
E81-8 p.11
▷E83-13 p.15
E89-4 p.8
▷E92-13 p.7

▷E94-3 p.10
▷E128-13 p.15
▷E132-17 p.14
▷E144-17 p.13
▷E147-13 p.15
▷E154-2 p.9
▷E156-17 p.12
R175-2 p.6
CDAL 24 ST H:
▷E91-74 p.6
R175-1 p.6
CDAL 25 H:
D_44-1 p.26
▷E33-6 p.16
E81-9 p.11
▷E83-14 p.15
E89-5 p.8
▷E92-10 p.7
▷E94-4 p.10
▷E104-18 p.10
▷E128-14 p.15
▷E132-16 p.14
▷E144-16 p.13
▷E147-14 p.15
▷E154-5 p.9
▷E156-16 p.12
R194-2 p.6
CDAL 25 ST H:
▷E91-78 p.6
R194-1 p.6
CDAL 26 H:
D_60-1 p.26
▷E33-7 p.16
E81-10 p.11
▷E83-15 p.15
E89-6 p.8
▷E92-9 p.7
▷E94-5 p.10
▷E104-19 p.10
▷E128-15 p.15
▷E132-15 p.14
▷E144-15 p.13
▷E147-15 p.15
▷E154-6 p.9
▷E156-15 p.12
R186-2 p.6
CDAL 26 ST H:
▷E91-79 p.6
R186-1 p.6
CDAL 27 H:
D_45-1 p.26
▷E33-9 p.16
E81-11 p.11
▷E83-18 p.15
E89-7 p.8
▷E92-8 p.7
▷E94-6 p.10
▷E104-20 p.10
▷E128-18 p.15
▷E132-14 p.14
▷E144-14 p.13
▷E147-18 p.15
▷E154-9 p.9
▷E156-14 p.12
R180-2 p.6
CDAL 27 ST H:
▷E91-80 p.6
R180-1 p.6
CDAL 28 H:
▷E33-10 p.16
E81-12 p.11
▷E83-19 p.15
E89-8 p.8
▷E92-7 p.7
▷E94-7 p.10
▷E128-19 p.15
▷E133-17 p.14
▷E145-17 p.13
▷E147-19 p.15
▷E154-12 p.9
E157-17 p.12
E_47-1 p.26
R181-2 p.6
CDAL 28 ST H:
▷E91-81 p.6
R181-1 p.6

REVISIONS

CHK	CHANGE NO.	REV

[Documentation]

CROSS REFERENCE:
Signal Names

digital

DRN: K. Yesse	DATE -	ENG: C. Threepio	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
- Thu Oct 20 17:07:35 1988		SHEET 51	
FIRST USED ON OPTION/MODEL: -		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

Output Sources for nets listed in cross-reference available upon request

Output Source Key: o> general output t> tristate output b> bidirectional output

CDAL 29 H:
b>B33-11 p.16
E81-13 p.11
b>E83-20 p.15
E89-9 p.8
b>E92-6 p.7
b>E94-8 p.10
b>E128-20 p.15
b>E133-16 p.14
b>E145-16 p.13
b>E147-20 p.15
t>E154-15 p.9
E157-16 p.12
E_32-1 p.26
R182-2 p.6
CDAL 29 ST H:
b>E91-82 p.6
R182-1 p.6
CDAL 30 H:
b>E33-12 p.16
E81-1 p.11
b>E83-21 p.15
E89-10 p.8
b>E92-5 p.7
b>E94-9 p.10
b>E128-21 p.15
b>E133-15 p.14
b>E145-15 p.13
b>E147-21 p.15
t>E154-16 p.9
E157-15 p.12
E_48-1 p.26
R183-2 p.6
CDAL 30 ST H:
b>E91-83 p.6
R183-1 p.6
CDAL 31 H:
b>E33-13 p.16
E81-2 p.11
b>E83-22 p.15
E89-11 p.8
b>E92-4 p.7
b>E94-10 p.10
b>E128-22 p.15
b>E133-14 p.14
b>E145-14 p.13
b>E147-22 p.15
t>E154-19 p.9
E157-14 p.12
E_33-1 p.26
R184-2 p.6
CDAL 31 ST H:
b>E91-84 p.6
R184-1 p.6
CLK 10MHZ H:
E30-52 p.23
b>E119-9 p.9
CLK 40MHZ H:
E134-13 p.6
E149-5 p.6
CLK 5MHZ H:
o>E113-14 p.6
E126-12 p.6
CLR TIMEOUT H:
E40-P7 p.20
t>E54-9 p.21
b>E57-14 p.21
CODE STR 1 CS L:
B98-25 p.15
E83-23 p.15
E110-23 p.15
E111-23 p.15
b>E122-22 p.8
CODE STR 2 CS L:
E70-23 p.15
E82-23 p.15
b>E122-21 p.8
E128-23 p.15
E148-23 p.15
CODE STR 3 CS L:
E98-23 p.15
E99-23 p.15
b>E122-20 p.8
E129-23 p.15
E147-23 p.15
COUNT CTRL H:
E40-R7 p.20
t>E54-7 p.21
b>E57-15 p.21
CRAM TST DIS H:
E41-5 p.17
t>E94-17 p.10
CSDP 0 H:
b>E44-5 p.16
b>E65-6 p.11
t>E71-10 p.14
E71-14 p.14
E72-3 p.10
t>E77-10 p.13
E77-14 p.13
E92-83 p.7
E112-7 p.9
E155-17 p.12
E_49-1 p.26
R82-2 p.28
R144-2 p.6
CSDP0 ST L:
b>E91-42 p.6
R144-1 p.6
CSDP 1 H:
b>E44-6 p.16
b>E64-6 p.11
E72-4 p.10
E92-82 p.7
t>E93-10 p.14
E93-14 p.14
t>E100-10 p.13
E100-14 p.13
E112-8 p.9
E155-16 p.12
E_34-1 p.26
R89-2 p.28
R145-2 p.6
CSDP1 ST L:
b>E91-41 p.6
R145-1 p.6
CSDP 2 H:
b>E44-7 p.16
E72-7 p.10
b>E73-6 p.11
E92-81 p.7
t>E105-10 p.14
E105-14 p.14
E112-9 p.9
t>E114-10 p.13
E114-14 p.13
E155-15 p.12
E_50-1 p.26
R97-2 p.28
R146-2 p.6
CSDP2 ST L:
b>E91-40 p.6
R146-1 p.6
CSDP 3 H:
b>E44-9 p.16
E72-8 p.10
b>E81-6 p.11
t>E131-10 p.14
E131-14 p.14
t>E143-10 p.13
E143-14 p.13
E155-14 p.12
E_35-1 p.26
R100-2 p.28
R122-2 p.6
CSDP3 ST L:
b>E91-39 p.6
R122-1 p.6
CSICA CS L:
E59-13 p.17
E84-4 p.10
t>E137-26 p.8
CSICB CS L:
E59-12 p.17
E84-7 p.10
b>E137-25 p.8
CVAX DATA FEC H:
E61-5 p.11
t>E69-22 p.10
CVAX DPE DIS L:
t>E80-17 p.10
E103-7 p.11
CVAX II ADDR 0 H:
E14-2 p.19
t>E43-12 p.22
E51-2 p.22
E52-2 p.22
CVAX II ADDR 1 H:
E14-5 p.19
t>E43-13 p.22
E51-4 p.22
E52-5 p.22
CVAX II ADDR 2 H:
E14-11 p.19
t>E43-14 p.22
E51-6 p.22
E52-11 p.22
CVAX II ADDR 3 H:
E14-14 p.19
t>E43-15 p.22
E51-8 p.22
E52-14 p.22
CVAX II ADDR 4 H:
E2-2 p.19
t>E43-16 p.22
E51-11 p.22
E53-2 p.22
CVAX II ADDR 5 H:
E2-5 p.19
t>E43-17 p.22
E51-13 p.22
E53-5 p.22
CVAX II ADDR 6 H:
E2-11 p.19
t>E43-18 p.22
E51-15 p.22
E53-11 p.22
CVAX II ADDR 7 H:
E2-14 p.19
t>E43-19 p.22
E51-17 p.22
E53-14 p.22
CVAX LOWER PERR H:
D_16-1 p.26
E90-3 p.11
CVAX PAR ERR H:
E104-11 p.10
o>E130-3 p.11
CVAX PAR FEC H:
t>E80-15 p.10
E103-12 p.11
CVAX RESET L:
E91-35 p.6
E142-3 p.6
CVAX UPPER PERR H:
D_17-1 p.26
E90-4 p.11
t>E103-26 p.11
CXHIC ADDR 0 H:
E30-45 p.23
t>E52-4 p.22
CXHIC ADDR 1 H:
E30-44 p.23
t>E52-7 p.22
CXHIC ADDR 2 H:
E30-43 p.23
t>E52-9 p.22
CXHIC ADDR 3 H:
E30-42 p.23
t>E52-12 p.22
CXHIC ADDR 4 H:
E30-41 p.23
t>E53-4 p.22
CXHIC ADDR 5 H:
E30-40 p.23
t>E53-7 p.22
CXHIC ADDR 6 H:
E30-39 p.23
t>E53-9 p.22
CXHIC ADDR 7 H:
E30-38 p.23
t>E53-12 p.22
CXHIC CS L:
E41-11 p.17
E43-2 p.22
E84-18 p.10
b>E118-24 p.8
CXHIC PERR L:
E24-7 p.17
E30-77 p.23
CXHIC RESET L:
E30-63 p.23
E69-18 p.10
CXHIC TO HIB L:
D_24-1 p.26
E3-16 p.23
E6-16 p.23
E7-16 p.23
E17-16 p.23
b>E20-27 p.17
DATA BUF CS L:
E59-3 p.17
E84-3 p.10
b>E137-24 p.8
DATA FEC H:
o>E61-6 p.11
E64-4 p.11
E81-4 p.11
E135-5 p.11
DBE L:
E119-13 p.9
R139-2 p.6
DBE ST L:
o>E91-31 p.6
R139-1 p.6
DCLK DIS L:
D_21-1 p.26
b>E104-25 p.10
E151-16 p.9
DEASSERT L:
E90-17 p.11
b>E150-25 p.9
E151-14 p.9
DESELECT L:
b>E118-20 p.8
E122-1 p.8
b>E150-26 p.9
DIAG PIRQ L:
E63-28 p.7
t>E80-19 p.10
DMA REQ L:
E30-79 p.23
b>E41-19 p.17
DPC CS L:
E41-12 p.17
E84-17 p.10
b>E118-25 p.8
DPC IDLE L:
o>E40-C11 p.20
E95-7 p.10
DPC II ADDR 0 H:
b>E40-B8 p.20
t>E51-18 p.22
E52-3 p.22
DPC II ADDR 1 H:
b>E40-B9 p.20
t>E51-16 p.22
E52-6 p.22
DPC II ADDR 2 H:
b>E40-A8 p.20
t>E51-14 p.22
E52-10 p.22
DPC II ADDR 3 H:
b>E40-A5 p.20
t>E51-12 p.22
E52-13 p.22
DPC II ADDR 4 H:
b>E40-B7 p.20
t>E51-9 p.22
E53-3 p.22
DPC II ADDR 5 H:
b>E40-C7 p.20
t>E51-7 p.22
E53-6 p.22
DPC II ADDR 6 H:
b>E40-A6 p.20
t>E51-5 p.22
E53-10 p.22
DPC RESET L:
E40-J14 p.20
t>E69-15 p.10
DPC TEST L:
E40-H15 p.20
E94-15 p.10
DPC XCVR EN L:
D_26-1 p.26
E4-19 p.20
E10-12 p.19
E16-19 p.20
E26-19 p.20
E27-19 p.20
o>E62-11 p.17
DPE L:
b>E103-25 p.11
R120-2 p.28
R123-1 p.6
DPE ST L:
b>E91-38 p.6
R123-2 p.6
DS L:
E92-84 p.7
E119-15 p.9
R154-2 p.6
DS ST L:
o>E91-29 p.6
R154-1 p.6
DXFER BAD L:
E30-78 p.23
E40-A13 p.20
DXFER OK L:
E30-69 p.23
E40-B5 p.20
ED IN H:
E92-46 p.7
o>E140-3 p.7
ED OUT L:
E141-7 p.7
E_22-1 p.26
EEPROM WR L:
o>E58-11 p.15
E68-31 p.15
E70-31 p.15
E82-31 p.15
E83-31 p.15
E98-31 p.15
E99-31 p.15
E110-31 p.15
E111-31 p.15
E128-31 p.15
E129-31 p.15
E147-31 p.15
E148-31 p.15
ENT H:
E113-10 p.6
o>E153-11 p.6
R57-2 p.28
ERR ADDR CLK H:
E121-11 p.9
E136-11 p.9
E138-11 p.9
b>E151-22 p.9
E154-11 p.9
ERR ADDR CS L:
o>E92-61 p.7
E151-10 p.9
ERR ADDR RDBK L:
E121-1 p.9
E136-1 p.9
E138-1 p.9
b>E151-23 p.9
E154-1 p.9
ERR DISABLE L:
t>E80-16 p.10
E104-6 p.10
ERR L:
E91-28 p.6
b>E117-22 p.6
R85-2 p.28
ETHER DATA OUT H:
o>E92-45 p.7
E141-2 p.7
ETHER DTR L:
E141-6 p.7
E_23-1 p.26
ETHER RCV DATA L:
E_25-1 p.26
R63-1 p.7
ETHER SIG GND L:
E_24-1 p.26
R74-1 p.7
FAST MEM ACT L:
B103-1 p.11
t>E122-26 p.8
E146-9 p.9
E_38-1 p.26
GEN PAR L:
b>E10-20 p.19
E34-3 p.20
E35-3 p.20
E36-3 p.20
E37-3 p.20
GND H:
A_13-1 p.26
A_28-1 p.26
A_29-1 p.26
A_32-1 p.26
A_36-1 p.26
A_40-1 p.26
A_43-1 p.26
A_44-1 p.26
A_56-1 p.26
A_58-1 p.26
B_32-1 p.26
B_36-1 p.26
B_39-1 p.26
B_42-1 p.26
B_50-1 p.26
B_51-1 p.26
B_52-1 p.26
B_54-1 p.26
B_56-1 p.26
B_60-1 p.26
C1-2 p.26
C2-2 p.26
C3-2 p.26
C4-2 p.26
C5-2 p.26
C6-2 p.26
C7-2 p.26
C8-2 p.26
C9-2 p.26
C10-2 p.26
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C39-2 p.29
C40-2 p.29
C41-2 p.29
C43-2 p.29
C44-2 p.29
C47-2 p.29
C48-2 p.29
C49-2 p.29
C50-2 p.29
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C85-2 p.29
C86-2 p.29
C87-2 p.29
C88-2 p.29
C89-2 p.29
C90-2 p.29
C91-2 p.29
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C93-2 p.29
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C96-2 p.29
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C100-2 p.29
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C102-2 p.29
C103-2 p.29
C104-2 p.29
C105-2 p.29
C106-2 p.29
C107-2 p.29
C108-2 p.26
C109-2 p.29
C110-2 p.29
C111-2 p.29
C112-2 p.29
C113-2 p.29
C114-2 p.29
C115-2 p.29
C116-2 p.26
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C120-2 p.29
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C131-2 p.29
C132-2 p.29
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C171-2 p.26
C172-2 p.29
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C199-2 p.26
C200-2 p.29
C201-2 p.29
C202-2 p.29
C203-2 p.26
C204-2 p.29
C205-2 p.29
C_1-1 p.26
C_4-1 p.26
C_10-1 p.26
C_13-1 p.26
C_14-1 p.26
C_15-1 p.26
C_27-1 p.26
C_28-1 p.26
C_29-1 p.26
C_30-1 p.26
C_32-1 p.26
C_36-1 p.26
C_41-1 p.26
C_43-1 p.26
C_44-1 p.26
C_51-1 p.26
C_52-1 p.26
C_53-1 p.26
C_56-1 p.26
C_58-1 p.26
C_60-1 p.26
D_1-1 p.26
D_15-1 p.26
D_30-1 p.26
D_31-1 p.26
D_46-1 p.26
E91-20 p.6
E_1-1 p.26
E_15-1 p.26
E_16-1 p.26
E_30-1 p.26
E_31-1 p.26
E_42-1 p.26
E_46-1 p.26
J3-1 p.27
J3-3 p.27
J3-5 p.27
J3-6 p.27
J3-14 p.27
J3-24 p.27
J3-34 p.27
J3-44 p.27
J3-50 p.27
J3-64 p.27
J3-72 p.27
J3-84 p.27
J3-94 p.27
J3-100 p.27
R52-1 p.26
R53-1 p.28
R58-2 p.7
R59-1 p.28
R60-1 p.28
R61-1 p.28
R67-2 p.7
R68-1 p.7
R70-1 p.7
R81-1 p.28
R92-1 p.28
R96-1 p.28
R98-1 p.28
R102-1 p.28
R107-1 p.28
R108-1 p.28
R111-1 p.28
R124-1 p.28
R130-1 p.28
R134-1 p.28
R156-1 p.28
R214-1 p.28
R224-1 p.28
R225-1 p.28
R234-1 p.28
R236-1 p.28
R251-1 p.28
R260-1 p.28
R265-1 p.28
R266-1 p.28
R277-1 p.28
R284-1 p.28
R288-1 p.28
R290-1 p.28
R293-1 p.28
R298-1 p.28
R303-1 p.28
R304-1 p.28
R305-1 p.28
R306-1 p.28
R307-1 p.28
R309-1 p.28
R310-1 p.28
R311-1 p.28
S1-1 p.6
TP0-1 p.28
TP1-1 p.28
TP2-1 p.28
TP3-1 p.28
TP4-1 p.28
TP5-1 p.28
TP6-1 p.28
HACK H:
D_23-1 p.26
E5-16 p.18
b>E20-20 p.17
E22-16 p.18
E38-12 p.16
b>E41-18 p.17
E43-1 p.22
E59-16 p.17
HALT L:
E30-73 p.23
E91-19 p.6
o>E153-3 p.7
R171-2 p.28
HIB ADDR 00 H:
E13-8 p.18
E14-3 p.19
t>E22-27 p.18
t>E25-27 p.18
J3-48 p.27
HIB ADDR 01 H:
E13-9 p.18
E14-6 p.19
t>E22-26 p.18
t>E25-26 p.18
J3-52 p.27
HIB ADDR 02 H:
E13-10 p.18
E14-10 p.19
t>E22-25 p.18
t>E25-25 p.18
J3-54 p.27
HIB ADDR 03 H:
E13-11 p.18
E14-13 p.19
t>E22-24 p.18
t>E25-24 p.18
J3-56 p.27
HIB ADDR 04 H:
E2-3 p.19
E13-12 p.18
t>E22-23 p.18
t>E25-23 p.18
J3-58 p.27
HIB ADDR 05 H:
E2-6 p.19
E13-13 p.18
t>E22-21 p.18
t>E25-21 p.18
J3-60 p.27
HIB ADDR 06 H:
E2-10 p.19
E13-1 p.18
t>E22-20 p.18
t>E25-20 p.18
J3-62 p.27
HIB ADDR 07 H:
E2-13 p.19
E13-2 p.18
t>E22-19 p.18
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REVISIONS

CHK	CHANGE NO.	REV

[Documentation]

CROSS REFERENCE: Signal Names

digital

DRN: K. Yesse	DATE: -
CHK'D: -	DATE: -
-	Thu Oct 20 17:08:08 1988
FIRST USED ON OPTION/MODEL: -	

ENG: C. Threepio	DATE: -
BOARD LOCATION: CXO	
SHEET 52	
NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

Output Sources for nets listed in cross-reference available upon request

Output Source Key: o> general output t> tristate output b> bidirectional output

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E50-11 p.22
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HIB DATA 02 H:
b>E17-25 p.23
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HIB DATA 03 H:
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HIB DATA 04 H:
b>E17-23 p.23
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HIB DATA 05 H:
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HIB DATA 06 H:
b>E17-20 p.23
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HIB DATA 07 H:
b>E17-19 p.23
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HIB DATA 11 H:
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HIB DATA 13 H:
b>E3-21 p.23
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HIB DATA 14 H:
b>E3-20 p.23
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HIB DATA 15 H:
b>E3-19 p.23
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HIB DATA 16 H:
b>E7-27 p.23
▷E8-19 p.19
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b>E56-25 p.16
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HIB DATA 17 H:
b>E7-26 p.23
▷E8-18 p.19
b>E16-17 p.20
E47-4 p.21
b>E56-23 p.16
J3-11 p.27
HIB DATA 18 H:
b>E7-25 p.23
b>E16-16 p.20
▷E23-27 p.19
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b>E56-21 p.16
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HIB DATA 19 H:
b>E7-24 p.23
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HIB DATA 20 H:
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▷E23-25 p.19
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b>E56-19 p.16
J3-17 p.27
HIB DATA 21 H:
b>E7-21 p.23
b>E16-13 p.20
▷E23-24 p.19
E47-13 p.21
b>E56-18 p.16
J3-19 p.27
HIB DATA 22 H:
b>E7-20 p.23
b>E16-12 p.20
▷E23-23 p.19
E47-15 p.21
b>E56-17 p.16

J3-21 p.27
HIB DATA 23 H:
b>E7-19 p.23
b>E16-11 p.20
▷E23-21 p.19
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b>E56-16 p.16
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HIB DATA 24 H:
b>E4-18 p.20
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b>E33-24 p.16
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HIB DATA 25 H:
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b>E33-23 p.16
E54-4 p.21
J3-27 p.27
HIB DATA 26 H:
b>E4-16 p.20
b>E6-25 p.23
▷E9-26 p.19
b>E33-21 p.16
E54-6 p.21
J3-29 p.27
HIB DATA 27 H:
b>E4-15 p.20
b>E6-24 p.23
▷E9-25 p.19
b>E33-20 p.16
E54-8 p.21
J3-31 p.27
HIB DATA 28 H:
b>E4-14 p.20
b>E6-23 p.23
▷E9-24 p.19
b>E33-19 p.16
E54-11 p.21
J3-33 p.27
HIB DATA 29 H:
b>E4-13 p.20
b>E6-21 p.23
▷E9-23 p.19
b>E33-18 p.16
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J3-35 p.27
HIB DATA 30 H:
b>E4-12 p.20
b>E6-20 p.23
▷E9-21 p.19
b>E33-17 p.16
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J3-37 p.27
HIB DATA 31 H:
b>E4-11 p.20
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HIB DATA P2 H:
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b>E24-26 p.17
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b>E137-21 p.8
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▷E59-26 p.17
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E33-25 p.16
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E44-25 p.16
E46-25 p.16
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E100-1 p.13
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E109-1 p.14
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b>E24-21 p.17
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b>E104-27 p.10
o>E130-11 p.28
▷E80-20 p.10
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▷E106-22 p.10
▷E106-21 p.10
▷E106-20 p.10
▷E106-19 p.10
▷E106-18 p.10
▷E106-17 p.10
▷E106-16 p.10
▷E106-15 p.10
b>E146-18 p.9
▷E146-21 p.9
▷E146-22 p.9
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b>E150-18 p.9
b>E150-20 p.9
▷E150-21 p.9
▷E150-22 p.9
▷E150-23 p.9
E150-13 p.9
E150-14 p.9
E150-17 p.9
▷E112-15 p.9
b>E10-22 p.19
b>E10-23 p.19
b>E10-24 p.19
b>E10-25 p.19
E10-16 p.19
E10-17 p.19
b>E38-20 p.16
b>E38-21 p.16
E38-1 p.16
E38-13 p.16
E38-14 p.16
E38-16 p.16
E38-17 p.16
b>E103-24 p.11
E103-6 p.11
E151-17 p.9
E122-3 p.8
E122-4 p.8
E122-6 p.8
E122-7 p.8
o>B63-55 p.7
o>B63-51 p.7
E63-61 p.7
o>B63-56 p.7
o>B92-66 p.7
o>B92-58 p.7
▷E120-3 p.28
▷E120-5 p.28
▷E120-7 p.28
▷E120-9 p.28
o>E126-6 p.6
o>E126-8 p.6
o>E153-6 p.28
o>B62-3 p.28
o>B61-11 p.28
o>E113-13 p.6
o>E113-12 p.6
o>E113-11 p.6
o>E113-15 p.6
o>E127-5 p.6
o>E127-13 p.6
o>E91-23 p.6
o>E91-25 p.6
b>E91-8 p.6
b>E91-7 p.6
b>E91-6 p.6
b>E91-5 p.6
b>E91-4 p.6
b>E91-3 p.6
b>E91-10 p.6
b>E91-9 p.6
NEXT STATE 0 H:
▷E28-18 p.21
b>E32-9 p.21
E40-K13 p.20
NEXT STATE 1 H:
▷E28-16 p.21
b>E32-10 p.21
E40-J15 p.20
NEXT STATE 2 H:
▷E28-14 p.21
b>E32-11 p.21
E40-K13 p.20

REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]

CROSS REFERENCE:
Signal Names

digital

FIRST USED ON OPTION/MODEL: -

Thu Oct 20 17:08:40 1988

DRN: K. Yesse	DATE -	ENG: C. Threepio	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
		SHEET 53	
		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

Output Sources for nets listed in cross-reference available upon request

Output Source Key: o> general output t> tristate output b> bidirectional output

NEXT STATE 3 H:
▷E28-12 p.21
b>E32-13 p.21
E40-K14 p.20
NEXT STATE 4 H:
▷E28-9 p.21
b>E32-14 p.21
E40-L14 p.20
NEXT STATE 5 H:
▷E28-7 p.21
b>E32-15 p.21
E40-L15 p.20
NEXT STATE 6 H:
▷E28-5 p.21
b>E32-16 p.21
E40-M15 p.20
NEXT STATE 7 H:
▷E28-3 p.21
b>E32-17 p.21
E40-L13 p.20
NEXT STATE 8 H:
▷E39-18 p.21
E40-M13 p.20
b>E42-9 p.21
NEXT STATE 9 H:
▷E39-16 p.21
E40-M14 p.20
b>E42-10 p.21
NODE RESET L:
E30-76 p.23
E62-5 p.6
NXM H:
E95-13 p.10
E146-13 p.9
o>E152-19 p.8
1 H:
PAGE XING H:
E30-64 p.23
E40-B13 p.20
PAL RESET L:
E90-13 p.11
b>E104-23 p.10
PAR CLK H:
E72-11 p.10
b>E151-20 p.9
PERR 0 L:
o>E65-5 p.11
b>E103-20 p.11
PERR 1 L:
o>E64-5 p.11
b>E103-21 p.11
PERR 2 L:
o>E73-5 p.11
b>E103-22 p.11
PERR 3 L:
o>E81-5 p.11
b>E103-23 p.11
PERR CLK H:
E90-16 p.11
b>E151-21 p.9
PGRANT L:
E5-2 p.18
E10-4 p.19
▷E15-19 p.17
E20-10 p.17
E22-2 p.18
E38-6 p.16
PNXT GRT H:
o>E58-6 p.17
E58-10 p.17
PREEMPT H:
E40-B15 p.20
▷E94-16 p.10
PREQ L:
b>E20-24 p.17
E31-6 p.17
E_8-1 p.26
PR NXT GRANT L:
o>E58-8 p.17
J3-97 p.27
PR NXT GRT L:
E15-11 p.17
▷E31-19 p.17
E58-4 p.17
E58-5 p.17
E61-1 p.17

E61-9 p.17
PROM READ L:
E58-13 p.15
E68-25 p.15
E70-25 p.15
E82-25 p.15
E83-25 p.15
E98-25 p.15
E99-25 p.15
E110-25 p.15
E111-25 p.15
E128-25 p.15
E129-25 p.15
E130-10 p.10
o>E135-8 p.15
E147-25 p.15
E148-25 p.15
E158-22 p.7
PWR 12V H:
C_37-1 p.26
E139-8 p.7
E141-8 p.7
PWR 5VBB H:
A_3-1 p.26
A_18-1 p.26
A_19-1 p.26
A_33-1 p.26
A_34-1 p.26
A_48-1 p.26
C16-1 p.26
C17-1 p.26
C18-1 p.26
C19-1 p.26
C21-1 p.26
C108-1 p.26
C116-1 p.26
C121-1 p.26
C130-1 p.26
C137-1 p.26
E60-7 p.24
E60-17 p.24
E60-23 p.24
E60-39 p.24
PWR INIT L:
E62-10 p.6
o>E127-4 p.6
PWR NEG 12V H:
C_39-1 p.26
E139-5 p.7
E141-5 p.7
R73-2 p.7
R76-2 p.7
PWR NEG 2V H:
C_33-1 p.26
C_34-1 p.26
C_48-1 p.26
PX NXT GRT L:
E59-2 p.17
o>E61-8 p.17
RD DIAG CLK H:
E84-11 p.10
E95-11 p.10
b>E151-25 p.9
RD DIAG CS L:
b>E118-21 p.8
E130-9 p.10
E146-12 p.9
E151-13 p.9
RD DIAG ENA L:
E72-1 p.10
E84-1 p.10
E95-1 p.10
E104-5 p.10
b>E151-24 p.9
RDY L:
E91-27 p.6
b>E117-21 p.6
E153-8 p.9
E_37-1 p.26
R72-2 p.28
READY H:
b>E146-26 p.9

E150-7 p.9
E153-9 p.9
REG BM 0 L:
E59-5 p.17
E85-13 p.13
E92-57 p.7
E103-13 p.11
▷E112-22 p.9
E123-13 p.14
E_51-1 p.26
REG BM 1 L:
E59-6 p.17
E85-5 p.13
E92-56 p.7
E103-14 p.11
▷E112-21 p.9
E123-5 p.14
E_52-1 p.26
REG BM 2 L:
E59-7 p.17
E85-10 p.13
E92-55 p.7
E103-16 p.11
▷E112-20 p.9
E123-10 p.14
E_53-1 p.26
REG BM 3 L:
E59-9 p.17
E85-2 p.13
E92-54 p.7
E103-17 p.11
▷E112-19 p.9
E123-2 p.14
E_54-1 p.26
REG CS 0 H:
E63-46 p.7
E112-18 p.9
E_55-1 p.26
REG CS 1 H:
E63-45 p.7
E112-17 p.9
E_56-1 p.26
REG CS 2 H:
E63-43 p.7
E104-9 p.10
▷E112-16 p.9
E118-27 p.8
E122-27 p.8
E137-27 p.8
E151-9 p.9
E_57-1 p.26
REG OEN L:
E104-3 p.10
o>E130-8 p.10
REG SEL 0 H:
▷E39-3 p.21
E40-R13 p.20
b>E42-17 p.21
REG SEL 1 H:
E40-R12 p.20
▷E47-18 p.21
b>E49-9 p.21
REG SEL 2 H:
E40-P12 p.20
▷E47-16 p.21
b>E49-10 p.21
REG SEL 3 H:
E40-P11 p.20
▷E47-14 p.21
b>E49-11 p.21
REG WR L:
E20-11 p.17
E38-3 p.16
E59-4 p.17
E63-40 p.7
E66-13 p.14
E67-13 p.14
E71-11 p.14
E74-13 p.13
E75-13 p.13
E77-11 p.13
E78-13 p.12
E79-13 p.12
E86-13 p.14
E87-13 p.14
E93-11 p.14

E95-8 p.10
E96-13 p.13
E97-13 p.13
E100-11 p.13
E101-13 p.12
E102-13 p.12
E103-9 p.11
E105-11 p.14
E108-13 p.14
E109-13 p.14
▷E112-23 p.9
E114-11 p.13
E115-13 p.13
E116-13 p.13
E124-13 p.12
E125-13 p.12
E131-11 p.14
E132-13 p.14
E133-13 p.14
E135-9 p.15
E143-11 p.13
E144-13 p.13
E145-13 p.13
E146-6 p.9
E150-6 p.9
E151-7 p.9
E155-13 p.12
E156-13 p.12
E157-13 p.12
E_36-1 p.26
REQ HIB BUS L:
E11-17 p.17
E40-N6 p.20
▷E47-12 p.21
b>E49-13 p.21
RESET L:
o>E62-6 p.6
E117-20 p.6
RGND 10 L:
E120-1 p.7
R92-2 p.28
RGND 11 L:
E69-2 p.10
E69-23 p.10
E80-2 p.10
E80-23 p.10
E94-2 p.10
E94-23 p.10
E106-2 p.10
E106-23 p.10
R111-2 p.28
RGND 12 L:
E104-16 p.10
R130-2 p.28
RGND 13 L:
E152-2 p.8
E152-4 p.8
E152-6 p.8
E152-8 p.8
E152-11 p.8
E152-13 p.8
E152-15 p.8
E152-17 p.8
E152-18 p.8
R59-2 p.28
RGND 14 L:
E20-16 p.17
R284-2 p.28
RGND 15 L:
E127-9 p.6
R96-2 p.28
RGND 16 L:
E41-16 p.17
R251-2 p.28
RGND 17 L:
E11-9 p.17
R298-2 p.28
RGND 18 L:
E1-3 p.18
E13-3 p.18
R293-2 p.28
RGND 19 L:
E121-3 p.9
E121-4 p.9
R98-2 p.28
RGND 1 L:

E146-16 p.9
R61-2 p.28
RGND 20 L:
E48-3 p.17
E48-8 p.17
E48-9 p.17
R234-2 p.28
RGND 21 L:
E24-16 p.17
R277-2 p.28
RGND 22 L:
E31-11 p.17
R265-2 p.28
RGND 23 L:
E15-2 p.17
E15-17 p.17
R290-2 p.28
RGND 24 L:
E50-15 p.22
E55-10 p.22
E55-11 p.22
E55-13 p.22
E55-14 p.22
E55-15 p.22
R224-2 p.28
RGND 25 L:
R307-2 p.28
RGND 26 L:
E32-18 p.21
E32-20 p.21
E42-18 p.21
E42-20 p.21
E49-18 p.21
E49-20 p.21
E57-18 p.21
E57-20 p.21
R225-2 p.28
RGND 27 L:
E3-13 p.23
E3-17 p.23
E6-13 p.23
E6-17 p.23
E7-13 p.23
E7-17 p.23
E17-13 p.23
E17-17 p.23
R303-2 p.28
RGND 28 L:
R309-2 p.28
RGND 29 L:
E30-66 p.23
R266-2 p.28
RGND 2 L:
E92-69 p.7
R124-2 p.28
RGND 30 L:
R260-2 p.28
RGND 31 L:
E52-15 p.22
E53-13 p.22
E53-15 p.22
R236-2 p.28
RGND 32 L:
E90-2 p.11
R156-2 p.28
RGND 33 L:
E119-1 p.6
E126-1 p.6
E126-3 p.6
R81-2 p.28
RGND 34 L:
E2-15 p.19
E14-15 p.19
R288-2 p.28
RGND 35 L:
R305-2 p.28
RGND 36 L:
R310-2 p.28
RGND 37 L:
R53-2 p.28
RGND 38 L:
R311-2 p.28
RGND 3 L:
R304-2 p.28
RGND 4 L:
E76-1 p.8

E89-1 p.8
E107-1 p.8
R108-2 p.28
RGND 5 L:
E150-16 p.9
R60-2 p.28
RGND 6 L:
E112-1 p.9
R102-2 p.28
RGND 7 L:
E119-19 p.9
R107-2 p.28
RGND 8 L:
R306-2 p.28
RGND 9 L:
E92-52 p.7
R134-2 p.28
SAB H:
E21-3 p.16
E33-3 p.16
b>E38-22 p.16
E44-3 p.16
E46-3 p.16
E56-3 p.16
SBA H:
E21-26 p.16
E33-26 p.16
b>E38-24 p.16
E44-26 p.16
E46-26 p.16
E56-26 p.16
SCRATCH PAD CS L:
E84-8 p.10
b>E122-23 p.8
E123-1 p.14
E123-4 p.14
E123-9 p.14
E123-12 p.14
SCR BY0 CS L:
E66-11 p.14
E67-11 p.14
E71-13 p.14
o>E123-11 p.14
SCR BY1 CS L:
E86-11 p.14
E87-11 p.14
E93-13 p.14
o>E123-6 p.14
SCR BY2 CS L:
E105-13 p.14
E108-11 p.14
E109-11 p.14
o>E123-8 p.14
SCR BY3 CS L:
o>E123-3 p.14
E131-13 p.14
E132-11 p.14
E133-11 p.14
SIA INTRPT L:
E63-16 p.7
J3-88 p.27
SIB INTRPT L:
E63-17 p.7
J3-89 p.27
SIC A BUS REQ L:
E31-8 p.17
J3-96 p.27
SIC A NXT GRANT L:
▷E31-17 p.17
J3-93 p.27
SIC B BUS REQ L:
E31-9 p.17
J3-92 p.27
SIC B NXT GRANT L:
▷E31-16 p.17
J3-91 p.27
SISM CS L:
E59-11 p.17
b>E137-22 p.8
SLOW MEM ACT L:
▷E122-18 p.8
E146-7 p.9
E_39-1 p.26
SRAM BANK 1 CS L:
E61-4 p.11
E78-11 p.12

E79-11 p.12
E84-13 p.10
E101-11 p.12
E102-11 p.12
b>E122-25 p.8
E124-11 p.12
E125-11 p.12
E155-11 p.12
E156-11 p.12
E157-11 p.12
SRAM BANK 2 CS L:
E84-14 p.10
E85-1 p.13
E85-4 p.13
E85-9 p.13
E85-12 p.13
b>E122-24 p.8
SSC ADDR 0 H:
o>E92-70 p.7
E158-10 p.7
E_27-1 p.26
SSC ADDR 1 H:
o>E92-71 p.7
E158-9 p.7
E_28-1 p.26
SSC BLO L:
E92-51 p.7
E_14-1 p.26
R54-2 p.28
SSC HLT L:
o>E92-60 p.7
E135-11 p.7
SSC LED 0 L:
E88-1 p.7
▷E120-12 p.7
SSC LED 1 L:
E88-3 p.7
▷E120-14 p.7
SSC LED 2 L:
E88-5 p.7
▷E120-16 p.7
SSC LED 3 L:
E88-7 p.7
▷E120-18 p.7
SSC OPT 0 L:
o>E92-47 p.7
E120-8 p.7
SSC OPT 1 L:
o>E92-48 p.7
E120-6 p.7
SSC OPT 2 L:
o>E92-49 p.7
E120-4 p.7
SSC OPT 3 L:
o>E92-50 p.7
E120-2 p.7
SSC RESET H:
E92-76 p.7
o>E135-12 p.6
E142-2 p.6
STR CXHIC CS L:
D_13-1 p.26
E20-3 p.17
E23-10 p.19
E41-25 p.17
STR DPC CS L:
D_14-1 p.26
E20-4 p.17
E23-9 p.19
b>E41-26 p.17
E62-12 p.17
STR WR L:
E10-14 p.19
E20-5 p.17
E38-4 p.16
b>E41-27 p.17
STR XISM CS L:
E10-10 p.19
E28-1 p.21
E28-19 p.21
E39-1 p.21
E39-19 p.21
b>E41-24 p.17
E47-1 p.21
E47-19 p.21
E54-1 p.21

E54-19 p.21
SWITCH A H:
E134-4 p.6
R71-2 p.28
S1-3 p.6
SWITCH B H:
E134-2 p.6
R64-2 p.28
S1-2 p.6
SYNC 20MHZ H:
E119-8 p.6
o>E126-5 p.6
SYNC 5MHZ H:
E58-1 p.6
E119-2 p.6
E119-4 p.6
E119-6 p.6
o>E126-9 p.6
SYNC CXHIC CS L:
b>E41-21 p.17
E50-1 p.22
E52-1 p.22
E53-1 p.22
E55-1 p.22
E55-5 p.22
R230-2 p.28
SYNC DPC CS L:
E40-P6 p.20
b>E41-23 p.17
E51-1 p.22
E51-19 p.22
R228-2 p.28
SYNC XISM CS L:
b>E41-20 p.17
R248-2 p.28
SYSCLK H:
▷E119-12 p.6
J3-2 p.27
SYSERR L:
D_19-1 p.26
o>E63-57 p.7
o>E92-77 p.7
E104-4 p.10
b>E117-25 p.6
R88-2 p.28
SYSRDY L:
o>E63-50 p.7
o>E92-78 p.7
b>E117-24 p.6
R84-2 p.28
SYSRST L:
E20-12 p.17
E62-4 p.6
o>E62-8 p.6
E69-11 p.10
E80-11 p.10
E94-11 p.10
E104-10 p.10
E106-11 p.10
E150-9 p.9
E153-10 p.9
SYSTEM CLK H:
E92-73 p.7
E92-74 p.7
E117-44 p.6
o>E134-8 p.6
TD IN H:
E92-44 p.7
o>E140-2 p.7
TD OUT L:
E139-7 p.7
E_17-1 p.26
TERM DATA OUT H:
o>E92-43 p.7
E139-2 p.7
TERM DTR L:
E139-6 p.7
E_18-1 p.26
TERM RCV DATA L:
E_20-1 p.26
R69-1 p.7
TERM SIG GND L:
E_19-1 p.26
R75-1 p.7
UCODE ADDR 0 H:
D_2-1 p.26

E32-8 p.21
o>E40-G15 p.20
E42-8 p.21
E49-8 p.21
E57-8 p.21
UCODE ADDR 1 H:
D_3-1 p.26
E32-7 p.21
o>E40-G14 p.20
E42-7 p.21
E49-7 p.21
E57-7 p.21
UCODE ADDR 10 H:
D_12-1 p.26
E32-19 p.21
o>E40-B14 p.20
E42-19 p.21
E49-19 p.21
E57-19 p.21
UCODE ADDR 2 H:
D_4-1 p.26
E32-6 p.21
o>E40-F14 p.20
E42-6 p.21
E49-6 p.21
E57-6 p.21
UCODE ADDR 3 H:
D_5-1 p.26
E32-5 p.21
o>E40-F15 p.20
E42-5 p.21
E49-5 p.21
E57-5 p.21
UCODE ADDR 4 H:
D_6-1 p.26
E32-4 p.21
o>E40-E15 p.20
E42-4 p.21
E49-4 p.21
E57-4 p.21
UCODE ADDR 5 H:
D_7-1 p.26
E32-3 p.21
o>E40-D15 p.20
E42-3 p.21
E49-3 p.21
E57-3 p.21
UCODE ADDR 6 H:
D_8-1 p.26
E32-2 p.21
o>E40-E13 p.20
E42-2 p.21
E49-2 p.21
E57-2 p.21
UCODE ADDR 7 H:
D_9-1 p.26
E32-1 p.21
o>E40-E14 p.20
E42-1 p.21
E49-1 p.21
E57-1 p.21
UCODE ADDR 8 H:
D_10-1 p.26
E32-23 p.21
o>E40-C15 p.20
E42-23 p.21
E49-23 p.21
E57-23 p.21
UCODE ADDR 9 H:
D_11-1 p.26
E32-22 p.21
o>E40-C14 p.20
E42-22 p.21
E49-22 p.21
E57-22 p.21
UCODE PAR H:
E40-N7 p.20
▷E54-3 p.21
b>E57-17 p.21
UCODE WREN L:
b>E10-21 p.19
E32-21 p.21
E42-21 p.21
E49-21 p.21
E57-21 p.21
UPERR H:

▷E90-26 p.11
E130-1 p.11
VCC H:
B_3-1 p.26
B_13-1 p.26
B_18-1 p.26
B_19-1 p.26
B_28-1 p.26
B_29-1 p.26
B_33-1 p.26
B_34-1 p.26
B_48-1 p.26
C1-1 p.26
C2-1 p.26
C3-1 p.26
C4-1 p.26
C5-1 p.26
C6-1 p.26
C7-1 p.26
C8-1 p.26
C9-1 p.26
C10-1 p.26
C11-1 p.26
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REVISIONS

CHK	CHANGE NO.	REV

[Documentation]

CROSS REFERENCE:
Signal Names

digital

DRN: K. Yesse	DATE -	ENG: C. Threepio	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
- Thu Oct 20 17:09:12 1988		SHEET 54	
FIRST USED ON OPTION/MODEL: -		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

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▷▷E40-C2 p.20
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▷▷E27-6 p.20
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▷▷E40-D2 p.20

Output Source Key: o> general output t> tristate output b> bidirectional output

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REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]

CROSS REFERENCE: Signal Names

digital

FIRST USED ON OPTION/MODEL: -

DRN: K. Yesse	DATE -	ENG: C. Threepio	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
Thu Oct 20 17:09:45 1988		SHEET 55	
		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

Output Sources for nets listed in cross-reference available upon request

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b>E27-7 p.20
E34-1 p.20
b>E40-D3 p.20
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XMI D62 L:
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R216-2 p.25
XMI ID5 L:
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R217-1 p.25
XMI ID5 ST L:
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R217-2 p.25
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B_59-1 p.26
R37-1 p.24
XMI LOCKOUT ST L:
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R37-2 p.24
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XMI NODEID1 H:
C_7-1 p.26
E30-87 p.23
XMI NODEID2 H:
C_8-1 p.26
E30-88 p.23
XMI NODEID3 H:
C_9-1 p.26
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XMI P0 L:
A_12-1 p.26
R269-1 p.25
XMI P0 ST L:
E161-30 p.25
R269-2 p.25
XMI P1 L:
B_55-1 p.26
R34-1 p.24
XMI P1 ST L:
E45-30 p.24
R34-2 p.24
XMI P2 L:
C_17-1 p.26
R218-1 p.25
XMI P2 ST L:
E159-30 p.25
R218-2 p.25
XMI PHASE L:
C_45-1 p.26
E60-29 p.24
XMI RESET L:
A_55-1 p.26
R10-1 p.24
XMI RESET ST L:
E12-27 p.24
R10-2 p.24
XMI RES REQ L:
C_40-1 p.26
E30-80 p.23

Output Source Key: o> general output t> tristate output b> bidirectional output

REVISIONS

CHK	CHANGE NO.	REV

[Documentation]

CROSS REFERENCE: Signal Names

digital

FIRST USED ON OPTION/MODEL: -

Thu Oct 20 17:10:17 1988

DRN: K. Yesse	DATE -	ENG: C. Threepio	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
		SHEET 56	
		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

Output Sources for nets listed in cross-reference available upon request

Output Source Key: o> general output t> tristate output b> bidirectional output

XMI RUN L:
A_54-1 p.26
XMI SPARE0 L:
B_47-1 p.26
R24-1 p.24
XMI SPARE0 ST L:
E29-27 p.24
R24-2 p.24
XMI SPAREBIT0 L:
C_46-1 p.26
XMI SPAREBIT1 L:
C_50-1 p.26
XMI SPAREBIT2 L:
A_35-1 p.26
XMI SPAREBIT3 L:
A_37-1 p.26
XMI SPAREBIT4 L:
A_39-1 p.26
XMI SUP L:
A_31-1 p.26
R301-1 p.25
XMI SUP ST L:
E162-27 p.25
R301-2 p.25
XMI TIME H:
C_59-1 p.26
t>E60-30 p.24
XMI TIME L:
C_57-1 p.26
E60-31 p.24

REVISIONS

CHK	CHANGE NO.	REV

[Documentation]
CROSS REFERENCE:
Signal Names

digital

Thu Oct 20 17:10:24 1988
FIRST USED ON OPTION/MODEL: -

DRN: K. Yesse	- DATE	ENG: C. Threepio	- DATE
CHK'D: -	- DATE	BOARD LOCATION: CXO	
		SHEET 57	
		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

KEY: C = Capacitor D = Diode E = Logic Part F = Fuse J = Jumper/Connector R = Resistor S = Switch U = Board Etch

C 1....p.26
C 2....p.26
C 3....p.26
C 4....p.26
C 5....p.26
C 6....p.26
C 7....p.26
C 8....p.26
C 9....p.26
C 10....p.26
C 11....p.26
C 12....p.26
C 13....p.26
C 14....p.26
C 15....p.26
C 16....p.26
C 17....p.26
C 18....p.26
C 19....p.26
C 20....p.26
C 21....p.26
C 22....p.29
C 23....p.29
C 24....p.29
C 25....p.29
C 26....p.29
C 27....p.29
C 28....p.29
C 29....p.29
C 30....p.29
C 31....p.29
C 32....p.29
C 33....p.29
C 34....p.29
C 35....p.29
C 36....p.29
C 37....p.29
C 38....p.29
C 39....p.29
C 40....p.29
C 41....p.29
C 42....p.7
C 43....p.29
C 44....p.29
C 45....p.6
C 46....p.7
C 47....p.29
C 48....p.29
C 49....p.29
C 50....p.29
C 51....p.29
C 52....p.29
C 53....p.29
C 54....p.29
C 55....p.29
C 56....p.29
C 57....p.6
C 58....p.29
C 59....p.29
C 60....p.29
C 61....p.29
C 62....p.29
C 63....p.29
C 64....p.29
C 65....p.29
C 66....p.29
C 67....p.29
C 68....p.29
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C 71....p.29
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C 73....p.29
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C 84....p.29
C 85....p.29
C 86....p.29
C 87....p.29
C 88....p.29
C 89....p.29
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C168....p.29
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C171....p.26
C172....p.29
C173....p.29
C174....p.29
C175....p.29
C176....p.29
C177....p.29
C178....p.29
C179....p.26
C180....p.29
C181....p.29
C182....p.29
C183....p.29
C184....p.26
C185....p.26
C186....p.26
C187....p.29
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C189....p.29
C190....p.26
C191....p.29
C192....p.29
C193....p.29
C194....p.29
C195....p.29
C196....p.29
C197....p.29
C198....p.29
C199....p.26
C200....p.29
C201....p.29
C202....p.29
C203....p.26
C204....p.29
C205....p.29
D101....p.26
E 1....p.18
E 2....p.19
E 3....p.23
E 4....p.20
E 5....p.18
E 6....p.23
E 7....p.23
E 8....p.19
E 9....p.19
E 10....p.19
E 11....p.17
E 12....p.24
E 13....p.18
E 14....p.19
E 15....p.17
E 16....p.20
E 17....p.23
E 18....p.18
E 19....p.19
E 20....p.17
E 21....p.16
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E 38....p.16
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E 46....p.16
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E 49....p.21
E 50....p.22
E 51....p.22
E 52....p.22
E 53....p.22
E 54....p.21
E 55....p.22
E 56....p.16
E 57....p.21
E 58....p.6
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E 59....p.17
E 60....p.24
E 61....p.11
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E 62....p.6
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E 63....p.7
E 64....p.11
E 65....p.11
E 66....p.14
E 67....p.14
E 68....p.15
E 69....p.10
E 70....p.15
E 71....p.14
E 72....p.10
E 73....p.11
E 74....p.13
E 75....p.13
E 76....p.8
E 77....p.13
E 78....p.12
E 79....p.12
E 80....p.10
E 81....p.11
E 82....p.15
E 83....p.15
E 84....p.10
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E 90....p.11
E 91....p.6
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E106....p.10
E107....p.8
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E148....p.15
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E152....p.8
E153....p.6
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E154....p.9
E155....p.12
E156....p.12
E157....p.12
E158....p.7
E159....p.25
E160....p.25
E161....p.25
E162....p.25
J 3....p.27
R 1....p.24
R 2....p.24
R 3....p.24
R 4....p.24
R 5....p.24
R 6....p.24
R 7....p.24
R 8....p.24
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R196....p.8
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R244....p.25
R245....p.28
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R305....p.28
R306....p.28
R307....p.28
R308....p.25
R309....p.28
R310....p.28
R311....p.28
R312....p.28
R313....p.28
S 1....p.6
TP 4...p.28
TP 3...p.28
TP 1...p.28
TP 5...p.28
TP 2...p.28
TP 6...p.28
TP 0...p.28
U 1....p.26
XE 1...p.28

REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]

CROSS REFERENCE:
Part Reference Designators

digital

DRN: K. Yesse	DATE -	ENG: C. Threepio	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
		SHEET 58	
- Thu Oct 20 17:10:31 1988		NEXT HIGHER ASSEMBLY: -	
FIRST USED ON OPTION/MODEL: -			

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

PART I: PARTS COUNT SUMMARY

Generic Parts Summary for WC_BRD1/REVA1_12 - Generated 20-OCT-1988 16:34:46

PROTO QTY	FRS QTY	Generic Part Name
2	2	16R8DSL
7	7	20L8BSL
2	2	20R4BSL
4	4	20RA10SL
1	0	27C256
12	12	28256SL
4	4	29863SL
25	25	5258PSOJ
8	8	6287SOJ
7	7	74ALS374SL
5	5	74ALS646SL
4	4	74ALS666SO
11	11	74AS286SO
1	1	74AS821SL
11	11	74AS823SL
1	1	74F00SO
1	1	74F04SO
2	2	74F08SO
1	1	74F132SO
1	1	74F240SO
4	4	74F245DSO
6	6	74F257SO
3	3	74F32SO
1	1	74F38SO
1	1	74F521SO
1	1	74F74SO
1	1	74F86SO
1	1	74FCT163ASOL
6	6	74FCT244ASO
3	3	74FCT841BSO
1	1	74FCT843BSO
1	1	74LS221SO
2	0	9636
1	0	9639
1	1	BICDPC
203	201	CAP,C
2	2	CPCAP
4	4	CY7C128SOJ
1	1	DC341A
1	1	DC506
1	1	DC509
1	1	DC511
7	7	DC530
1	1	DC531P
1	1	DC7157
1	0	ESDTAB
300	0	FINGER
1	1	LEDA
1	1	LEDX4
1	1	PC2CONN100A
7	7	POST
313	305	RES,C
1	0	SPSOIC14
1	1	SW,SPDT
1	1	TCO711SS
0	1	27C256SL
172	0	[Mark Eyelets]

PART II: EXCESS SPARES LIST

Excess Spare Parts/Gates Summary for WC_BRD1/REVA1_12 - Generated 20-OCT-1988 16:34:45

-- NO EXCESS SPARES FOUND --

PART III: PACKAGE-SPECIFIC LOGIC PART SUMMARIES

== PLCC-Packaged Parts ==

PROTO QTY	FRS QTY	Generic Part Name
2	2	16R8DSL
7	7	20L8BSL
2	2	20R4BSL
4	4	20RA10SL
12	12	28256SL
4	4	29863SL
7	7	74ALS374SL
5	5	74ALS646SL
1	1	74AS821SL
11	11	74AS823SL
0	1	27C256SL

== SOIC-Packaged Parts ==

PROTO QTY	FRS QTY	Generic Part Name
4	4	74ALS666SO
11	11	74AS286SO
1	1	74F00SO
1	1	74F04SO
2	2	74F08SO
1	1	74F132SO
1	1	74F240SO
4	4	74F245DSO
6	6	74F257SO
3	3	74F32SO
1	1	74F38SO
1	1	74F521SO
1	1	74F74SO
1	1	74F86SO
1	1	74FCT163ASOL
6	6	74FCT244ASO
3	3	74FCT841BSO
1	1	74FCT843BSO
1	1	74LS221SO

== SOJ-Packaged Parts ==

PROTO QTY	FRS QTY	Generic Part Name
25	25	5258PSOJ
8	8	6287SOJ
4	4	CY7C128SOJ

REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]
PART LIST INFO:
Part Summaries &
Excess Spares List

digital

DRN: K. Yesse — DATE: -
CHK'D: - — DATE: -
- Thu Oct 20 17:12:04 1988
FIRST USED ON OPTION/MODEL: -

ENG: C. Threepio — DATE: -
BOARD LOCATION: CXO
SHEET 60
NEXT HIGHER ASSEMBLY: -

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88

PART IV: DETAILED PART LIST

Detailed Parts List (w/Ref. Des.) for WC_BRD1/REVA1_I2 - Generated 20-OCT-1988 16:35:09
[Sorted by Generic Part Number]

Prototype Quantity	Generic Name	DEC Part No.	Part Reference Designators
QTY: 1	16R8DSL	ID-ARBIT-P1	E31
QTY: 1	16R8DSL	ID-IIADD-P1	E43
QTY: 1	20L8BSL	ID-BOGEY-P1	E10
QTY: 1	20L8BSL	ID-CV2HB-P1	E38
QTY: 1	20L8BSL	ID-DCTRL-P1	E103
QTY: 1	20L8BSL	ID-HIBSD-P1	E137
QTY: 1	20L8BSL	ID-PRMDE-P1	E122
QTY: 1	20L8BSL	ID-RGCTL-P1	E151
QTY: 1	20L8BSL	ID-XICSD-P1	E118
QTY: 1	20R4BSL	ID-MCTRL-P1	E150
QTY: 1	20R4BSL	ID-READY-P1	E146
QTY: 1	20RA10SL	ID-CHCTL-P1N	E20
QTY: 1	20RA10SL	ID-MEMER-P1N	E104
QTY: 1	20RA10SL	ID-PARR4-P1N	E24
QTY: 1	20RA10SL	ID-XSYNC-P1N	E41
QTY: 1	27C256	23-000E6-07	E158
QTY: 1	28256SL	ID-STR10-P2	E111
QTY: 1	28256SL	ID-STR11-P2	E110
QTY: 1	28256SL	ID-STR12-P2	E68
QTY: 1	28256SL	ID-STR13-P2	E83
QTY: 1	28256SL	ID-STR20-P2	E148
QTY: 1	28256SL	ID-STR21-P2	E70
QTY: 1	28256SL	ID-STR22-P2	E82
QTY: 1	28256SL	ID-STR23-P2	E128
QTY: 1	28256SL	ID-STR30-P2	E129
QTY: 1	28256SL	ID-STR31-P2	E98
QTY: 1	28256SL	ID-STR32-P2	E99
QTY: 1	28256SL	ID-STR33-P2	E147
QTY: 4	29863SL	19-26845-01	E17,E3,E6,E7
QTY: 25	5258PSOJ	21-26937-05	E101,E102,E108,E109,E115,E116,E124,E125,E132,E133,E144,E145,E155,E156,E157,E66 ,E67,E74,E75,E78,E79,E86,E87,E96,E97
QTY: 8	6287SOJ	21-24781-04	E100,E105,E114,E131,E143,E71,E77,E93
QTY: 7	74ALS374SL	19-23441-01	E121,E136,E138,E154,E72,E84,E95
QTY: 5	74ALS646SL	19-26843-01	E21,E33,E44,E46,E56
QTY: 4	74ALS666SO	19-28730-01	E106,E69,E80,E94
QTY: 11	74AS286SO	19-26848-01	E1,E13,E34,E35,E36,E37,E48,E64,E65,E73,E81
QTY: 1	74AS821SL	19-26837-01	E59
QTY: 11	74AS823SL	19-23453-02	E11,E15,E18,E19,E22,E23,E25,E5,E8,E9,E90
QTY: 1	74F00SO	19-21305-02	E58
QTY: 1	74F04SO	19-21307-02	E135
QTY: 2	74F08SO	19-21308-02	E61,E62
QTY: 1	74F132SO	19-26844-01	E134
QTY: 1	74F240SO	19-21008-02	E120
QTY: 4	74F245DSO	19-20441-02	E16,E26,E27,E4
QTY: 6	74F257SO	19-21330-02	E14,E2,E50,E52,E53,E55
QTY: 3	74F32SO	19-21312-02	E123,E130,E85
QTY: 1	74F38SO	19-26139-01	E153
QTY: 1	74F521SO	19-21417-02	E152
QTY: 1	74F74SO	19-21314-02	E126
QTY: 1	74F86SO	19-21315-02	E142
QTY: 1	74FCT163ASOL	21-30158-01	E113
QTY: 6	74FCT244ASO	21-30486-01	E119,E28,E39,E47,E51,E54
QTY: 3	74FCT841BSO	21-30289-01	E107,E76,E89
QTY: 1	74FCT843BSO	21-30474-01	E112
QTY: 1	74LS221SO	19-12858-02	E127
QTY: 2	9636	19-15415-00	E139,E141
QTY: 1	9639	19-19542-01	E140
QTY: 1	BICDPC	21-27781-01	E40
QTY: 2	CAP,C	10-24051-10	C42,C46
QTY: 160	CAP,C	10-24053-01	C100,C101,C102,C103,C104,C105,C106,C107,C109,C110,C111,C112,C113,C114,C115,C117 ,C118,C119,C120,C122,C123,C124,C125,C126,C127,C128,C129,C131,C132,C133,C134,C135 ,C136,C139,C140,C141,C142,C143,C144,C145,C146,C148,C149,C150,C152,C153,C154,C155 ,C158,C160,C161,C162,C163,C164,C165,C167,C168,C169,C170,C172,C173,C174,C175,C176 ,C177,C178,C180,C181,C182,C183,C187,C188,C189,C191,C192,C193,C194,C195,C196,C197 ,C198,C200,C201,C202,C204,C205,C22,C23,C24,C25,C26,C27,C28,C29,C30,C31,C32,C33,C34 ,C35,C36,C37,C38,C39,C40,C41,C43,C44,C47,C48,C49,C50,C51,C52,C53,C54,C55,C56,C58 ,C59,C60,C61,C62,C63,C64,C65,C66,C67,C68,C69,C70,C71,C72,C73,C74,C75,C76,C77,C78 ,C79,C80,C81,C82,C83,C84,C85,C86,C87,C88,C89,C90,C91,C92,C93,C94,C95,C96,C97,C98,C99
QTY: 8	CAP,C	10-24053-12	C11,C12,C156,C157,C184,C185,C5,C6
QTY: 33	CAP,C	10-24053-18	C1,C10,C108,C116,C121,C13,C130,C137,C138,C14,C147,C15,C151,C159,C16,C166,C17,C171 ,C179,C18,C186,C19,C190,C199,C2,C20,C203,C21,C3,C4,C7,C8,C9
QTY: 2	CPCAP	10-24455-08	C45,C57
QTY: 4	CY7C128SOJ	21-17872-13	E32,E42,E49,E57
QTY: 1	DC341A	21-24674-13	E91
QTY: 1	DC506	21-24330-02	E63
QTY: 1	DC509	21-24673-01	E117
QTY: 1	DC511	21-24942-03	E92
QTY: 7	DC530	21-26702-02	E12,E159,E160,E161,E162,E29,E45
QTY: 1	DC531P	21-26703-01	E60
QTY: 1	DC7157	ID-X7157-01	E30

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QTY: 1	ESDTAB	99-99999-96	U1
QTY: 1	LEDA	11-17373-02	D101
QTY: 1	LEDX4	11-20964-01	E88
QTY: 1	PC2CONN100A	ID-40697-01	J3
QTY: 7	POST	90-07791-00	TP0,TP1,TP2,TP3,TP4,TP5,TP6
QTY: 71	RES,C	13-23825-13	R112,R113,R114,R119,R121,R122,R123,R126,R127,R128,R131,R132,R133,R135,R136,R137 ,R138,R139,R140,R141,R142,R143,R144,R145,R146,R147,R148,R150,R151,R153,R154,R155 ,R157,R161,R162,R163,R164,R165,R169,R170,R172,R173,R174,R175,R177,R178,R179,R180 ,R181,R182,R183,R184,R185,R186,R187,R188,R189,R190,R191,R192,R194,R195,R196,R197 ,R200,R202,R203,R204,R207,R209,R211
QTY: 39	RES,C	13-23825-25	R102,R107,R108,R111,R124,R130,R134,R156,R214,R224,R225,R234,R236,R251,R260,R265 ,R266,R277,R284,R288,R290,R293,R298,R303,R304,R305,R306,R307,R309,R310,R311,R53,R59 ,R60,R61,R81,R92,R96,R98
QTY: 4	RES,C	13-23825-33	R63,R69,R74,R75
QTY: 1	RES,C	13-23825-41	R51
QTY: 95	RES,C	13-23825-49	R100,R101,R103,R104,R105,R106,R109,R110,R115,R116,R117,R118,R120,R125,R129,R149 ,R152,R158,R159,R160,R166,R167,R168,R171,R176,R193,R210,R215,R219,R220,R221,R222 ,R228,R230,R231,R232,R237,R238,R240,R245,R247,R248,R252,R254,R255,R256,R261,R263 ,R270,R271,R272,R273,R274,R275,R280,R281,R285,R289,R295,R297,R300,R302,R312,R313 ,R35,R38,R39,R52,R54,R55,R56,R57,R62,R64,R65,R66,R71,R72,R77,R79,R80,R82,R83,R84 ,R85,R86,R87,R88,R89,R90,R93,R94,R95,R97,R99
QTY: 2	RES,C	13-23825-61	R78,R91
QTY: 2	RES,C	13-23825-65	R68,R70
QTY: 4	RES,C	13-23826-10	R58,R67,R73,R76
QTY: 11	RES,C	13-23827-30	R10,R223,R24,R249,R278,R301,R37,R40,R41,R42,R43
QTY: 84	RES,C	13-23827-47	R1,R11,R12,R13,R14,R15,R16,R17,R18,R19,R198,R199,R2,R20,R201,R205,R206,R208,R21 ,R212,R213,R216,R217,R218,R22,R226,R227,R229,R23,R233,R235,R239,R241,R242,R243,R244 ,R246,R25,R250,R253,R257,R258,R259,R26,R262,R264,R267,R268,R269,R27,R276,R279,R28 ,R282,R283,R286,R287,R29,R291,R292,R294,R296,R299,R3,R30,R308,R31,R32,R33,R34,R36 ,R4,R44,R45,R46,R47,R48,R49,R5,R50,R6,R7,R8,R9
QTY: 1	SPSOIC14	ID-0SOIC-14	XE1
QTY: 1	SW,SPDT	12-16523-00	S1
QTY: 1	TCO711SS	18-29889-01	E149
QTY: 172	[Mark Eyelet]	12-23208-03	

REVISIONS		
CHK	CHANGE NO.	REV

[Documentation]
PART LIST INFO:
Detailed Part List

digital

DRN: K. Yesse	DATE -	ENG: C. Threepio	DATE -
CHK'D: -	DATE -	BOARD LOCATION: CXO	
- Thu Oct 20 17:12:11 1988		SHEET 61	
FIRST USED ON OPTION/MODEL: -		NEXT HIGHER ASSEMBLY: -	

TITLE: WILDCAT BOARD 1

SIZE	CODE	NUMBER	REV
K	CS	-	20OCT88