FIELD MAINTENANCE PRINT SET

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UNIT VARIATIONS COVERED BY THIS PRINT SET
6300B-A2
6300B-A3
6300B-B2
6300B-B3
6300B-C2
6300B-C3
6300B-D2
6300B-D3

6300B
FIELD MAINTENANCE PRINT SET

DIGITAL EQUIPMENT CORPORATION

PRINT SET PART NUMBER MP-02071-01 REV A1

FILE NAME: TC-6300B-0-DBUA

REVISION HISTORY		
REV.	A	
ECO NUMBER	INITIAL	
DATE		

DRN. D. HEALY	DATE 25FEB85	TITLE digital 6300B MICRO VAX II WORLD BOX
CHK'D D. HEALY	DATE 19MAR85	
DES. ENG. J. NICHOLS	DATE 19MAR85	
RESP. ENG. K. WORTMAN	DATE 19MAR85	
FIELD SERVICE	DATE	SIZE B / CODE TC / NUMBER 6300B-0-DBU / REV. A
TOP DOC. B-DD-6300B-0-DBU		SHEET 1 OF 1

SIZE B CODE TC NUMBER 6300B-0-DBU REV. A

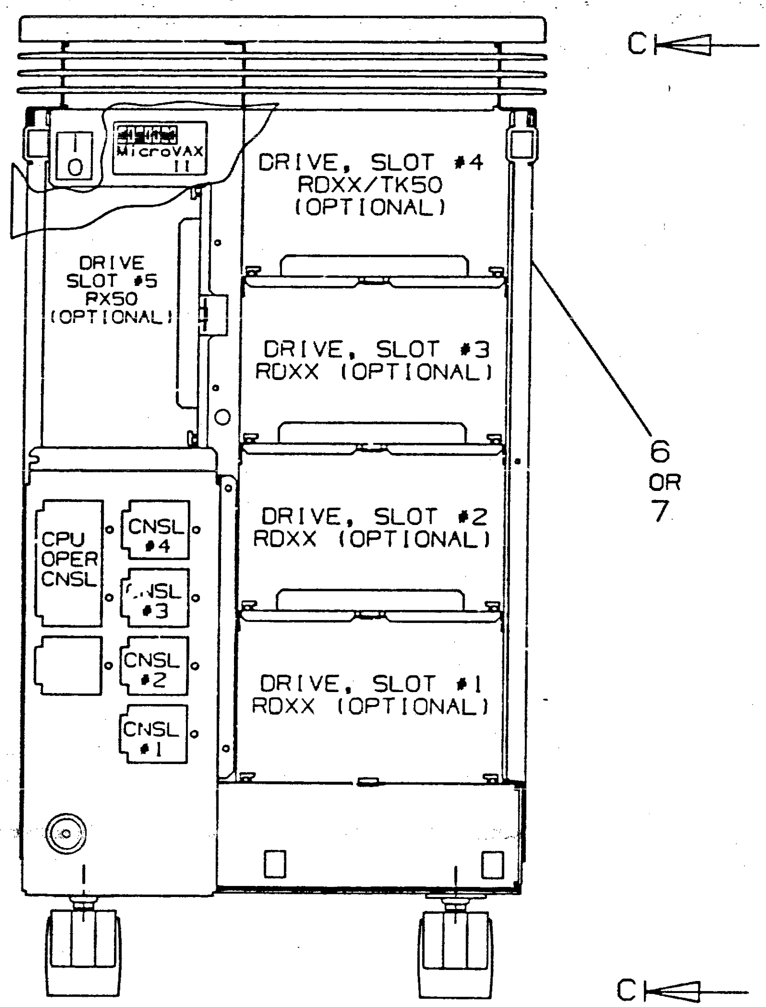
ML01

LEGEND

PART NO.	REV	VARIATION
63008-A2	A2	1 MB FP 120V
63008-A3	A2	1 MB FP 240V
63008-B2	A2	1 MB NO FP 120V
63008-B3	A2	1 MB NO FP 240V
63008-C2	A2	256 KB FP 120V
63008-C3	A2	256 KB FP 240V
63008-D2	A2	256 KB NO FP 120V
63008-D3	A2	256 KB NO FP 240V

NOTES:

1. BACK PANEL CONFIGURATION RULES & MASS STORAGE CONFIGURATION RULES: REF D-AR-7022380-0-DBU
2. ITEM #5 NOT SHOWN ON THIS ASSY.



(SEE SHEET 2)

VIEW A-A
(FRONT)
(SEE SHEET 2)
SHOWN WITHOUT FRONT
OR SIDE PANELS

LAYER #6: WORK LAYER (SHT 4)
LAYER #5: WORK LAYER (SHT 3)
LAYER #4: FORMAT LAYER (SHT 2,3 & 4)
LAYER #3: WORK LAYER (SHT 2)
LAYER #2: FORMAT LAYER (SHT 1)
LAYER #1: WORK LAYER (SHT 1)
PLOT SCALE: .50
SYSTEM #: 20
PROGRAM VERSION: UGRAF D4.1
FILE NAME: 63008-0-DBUB
TITLE: 63008 MICRO VAX II WORLD BOX

PLOT AT .50

CAUTION: OFF SHEET PARTS LIST EXISTS
REFER TO K-PL-63008-0-DBP
(ML 863)

QUANTITY & VARIATION	DESCRIPTION	DRAWING NO.	PART NO.	ITEM NO.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND THE FOLLOWING TOLERANCES APPLY (PER DEC STD 114)

INCHES TOLERANCES: .X: ± .1, .XX: ± .02, .XXX: ± .005 — ANGLES ±0° 30' — SURFACE QUALITY (MICROINCHES)

APPLICABLE DIMENSION RANGE (CHECK ONE)	OVER 0 TO 0.2	OVER 0.2 TO 1.2	OVER 1.2 TO 4.0	OVER 4.0 TO 12.0	OVER 12.0 TO 40.0	OVER 40.0 TO 80.0
☐	±.02		±.03	±.06	±.10	
☐	±.004	±.008	±.012	±.016	±.024	±.04
☐						

FIRST HIGHER ASS'Y

THIRD ANGLE PROJECTION

DO NOT SCALE DRAWING

REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL: SEE PARTS LIST

FINISH: NONE

		DATE
DRN	PAUL GAGNE	22 JAN 85
CHK'D	D. HEALY	19 MAR 85
DES. ENG.	J. NICHOLS	19 MAR 85
RESP. ENG.	J. NICHOLS	19 MAR 85
MFG. ENG.	K. WORTMAN	19 MAR 85

TOP DOC. B-DD-63008-0-DBU

digital

TITLE: 63008 MICRO VAX II WORLD BOX

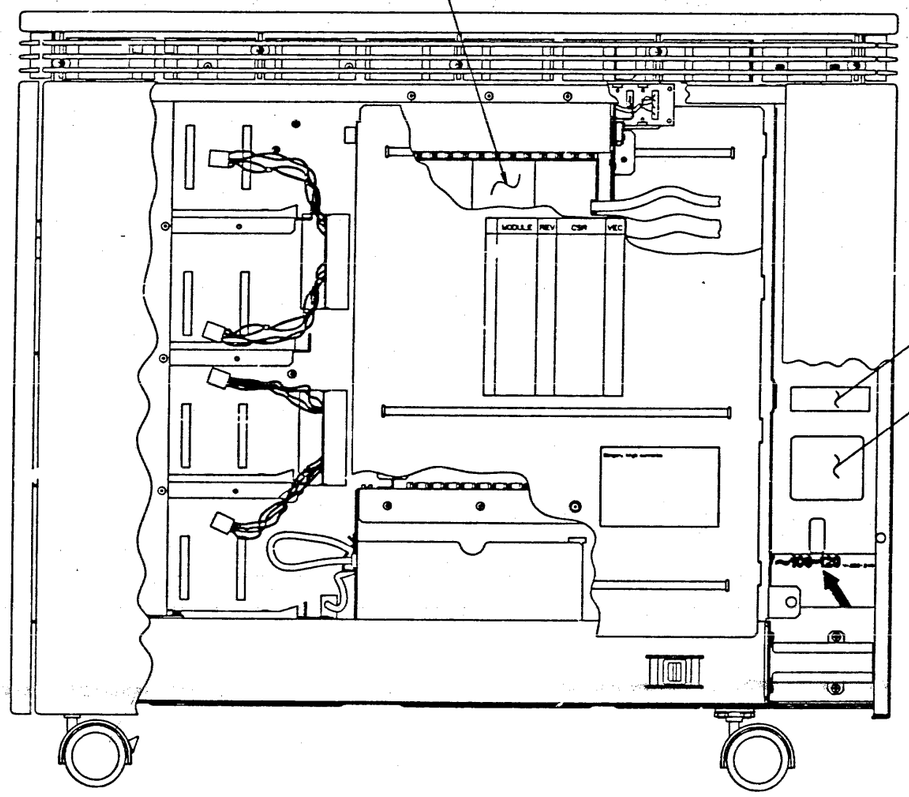
DOCUMENT NUMBER

SIZE	CODE	NUMBER	REV.
D	UA	63008-0-DBU	B

SCALE 1/2 — SHEET 1 OF 4

REVISIONS

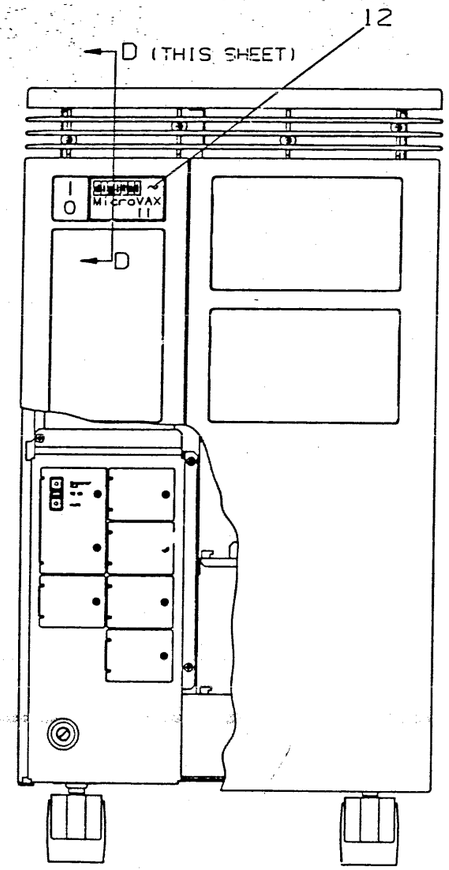
CHG.	CHANGE NO.	REV.
O.H.	INITIAL 63008-ML001 CHRIS DAVID 8 MAY 85	A
	JAY NICHOLS 8 MAY 85	B



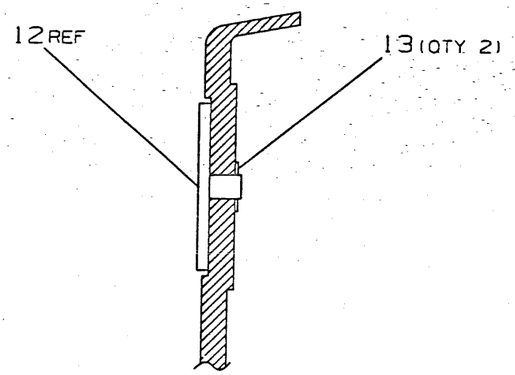
PLOT AT .50

REVISIONS		
CHK	CHANGE NO	REV

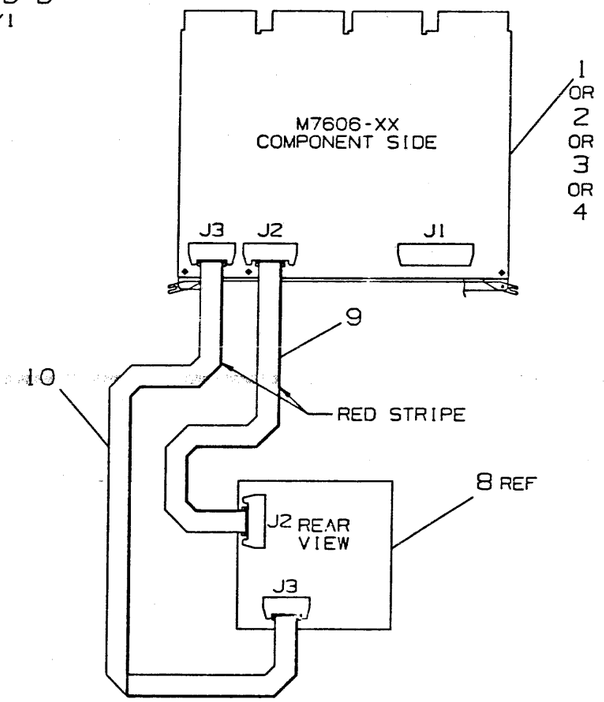
TITLE	SIZE	CODE	NUMBER	REV
63008 MICRO VAX II WORLD BOX	D	UA	63008-0-DBU	B
SCALE 1/2 SHEET 2 OF 4	DIST			



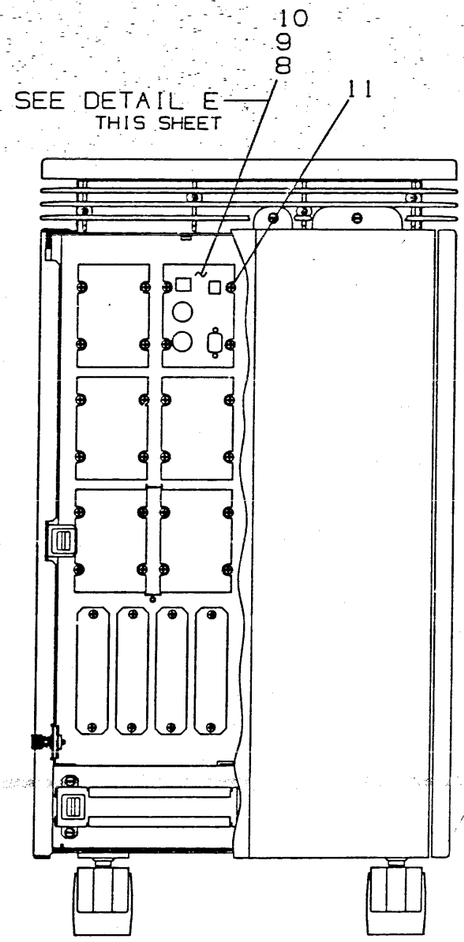
VIEW A-A
SEE SHT 2



SECTION D-D
SCALE 2/1



DETAIL "E"



VIEW B-B
SEE SHT 2

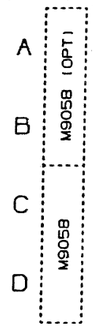
REVISIONS		
CHK	CHANGE NO	REV

PLOT AT .5000

TITLE	SIZE	CODE	NUMBER	REV
63008 MICRO VAX II WORLD BOX	D	UA	63008-0-DBU	B
SCALE 1/2 SHEET 3 OF 4			DIST	

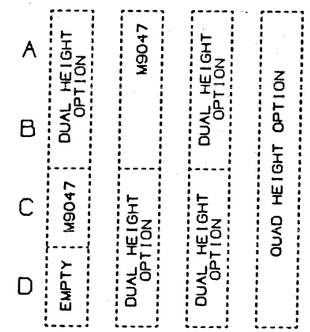
ML01

THE MODULE UTILIZATION FOR 13TH SLOT SEE NOTE 9



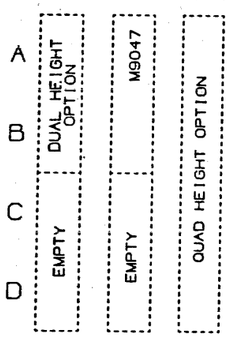
13

POSSIBLE MODULE UTILIZATIONS FOR SLOT 5-12 ARE AS FOLLOWS (SEE NOTES 7 AND 8 THIS SHT):



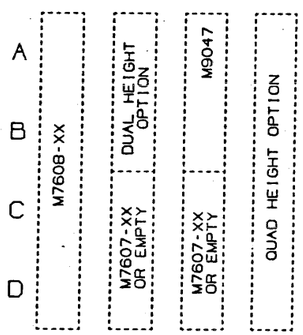
5-12

POSSIBLE MODULE UTILIZATIONS FOR SLOT 4 ARE AS FOLLOWS



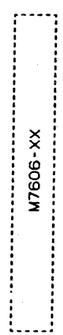
4

POSSIBLE MODULE UTILIZATIONS FOR SLOT 2 AND 3 ARE AS FOLLOWS (SEE NOTES 5,6,7 AND 8 THIS SHT):

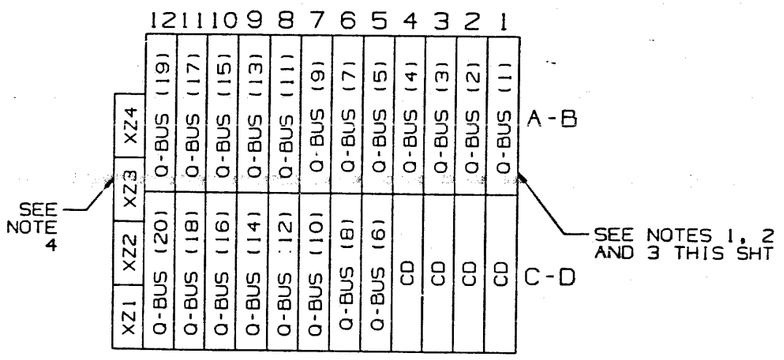


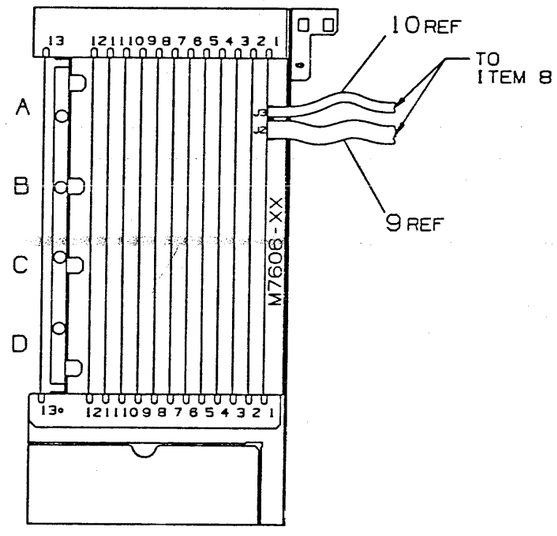
2-3

THE MODULE UTILIZATION FOR THE FIRST SLOT IS AS FOLLOWS:



1





MODULE UTILIZATION

NOTES:

1. BACKPLANE VIEWS ARE FROM THE MODULE SIDE
2. THE AB ROWS OF SLOTS 1-12 AND THE CD ROWS OF SLOTS 5-12 ARE EACH LABELED "Q-BUS" BECAUSE THEY ARE INTERCONNECTED PER THE Q-BUS SPECIFICATION. THE NUMBER IN PARENTHESIS SHOWS THE PATH OF INTERRUPT AND DMA GRANT CONTINUITY; INCREASING VALUE DENOTES DECREASING PRIORITY.
3. THE CD ROWS OF SLOTS 1-4 ARE LABELED "CD" BECAUSE THEY ARE CONNECTED PER THE "CD INTERCONNECT" SPECIFICATION. THIS INTERCONNECT CONNECTS SELECTED SIDE TWO PINS OF A GIVEN SLOT TO SIDE ONE PINS OF THE NEXT SLOT.
4. THE BACKPLANE INCLUDES FOUR RESISTOR PACKS IN LOCATIONS XZ1, XZ2, XZ3 AND XZ4. THESE RESISTOR PACKS PROVIDE AN ADDITIONAL 120 OHMS OF TERMINATION TO THE Q-BUS LINES.
5. THE SYSTEM MAY CONTAIN UP TO TWO MS630 MEMORY MODULES, LOCATED IN SLOTS 2 AND 3 (A SINGLE MS630 MODULE MUST BE LOCATEDIN SLOT 2). A QUAD HEIGHT MS630 (M7608-A(X) OR M7608-B(X)) FILLS THE ENTIRE SLOT. A DUAL HEIGHT MS630 (M7607-A(X)) OCCUPIES THE CD ROWS ONLY.
6. IF SLOTS 2 AND 3 (OR SLOT 3) ARE NOT USED FOR MS630 MEMORY MODULE(S), AND ARE NOT REQUIRED FOR Q-BUS OPTIONS, THEN RESERVE THEM (IT) FOR FUTURE MEMORY MODULE EXPANSION WITH M9047 GRANT CONTINUITY CARD(S) IN ROW AB.
7. QUAD HEIGHT Q-BUS OPTIONS MAY BE ADDED TO ANY OPEN SLOTS, AND DUAL HEIGHT Q-BUS OPTIONS MAY BE ADDED TO ANY OPEN "Q-BUS" HALF SLOTS. ALL UNUSED "Q-BUS" HALF SLOTS WHICH PRECEED THE LAST OPTION MUST CONTAIN GRANT CONTINUITY MODULES (M9047) TO PASS GRANTS TO MODULES OF A LOWER PRIORITY. UNUSED "CD" HALF SLOTS ARE LEFT VACANT. (NOTES 2 AND 3 IDENTIFY THE "Q-BUS" AND "CD" HALF SLOTS).
8. FOR MORE INFORMATION ON BACKPLANE SLOT ASSIGNMENTS, REFER TO THE SYSTEM TECHNICAL MANUAL.
9. REF D-AR-7022380-0-DBU FOR MODULE UTILIZATION REQUIREMENTS.

REVISIONS

CHK	CHANGE NO	REV

PLOT AT .50

TITLE	SIZE	CODE	NUMBER	REV
6300B MICRO VAX II WORLD BOX	D	UA	6300B-0-DBU	B
SCALE 1/2	SHEET 4 OF 4	DIST		

AUTOMATED BY PRTLST.5R(55) — P A R T S L I S T —

LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION A2 A2	A3 A2	B2 A2	B3 A2	C2 A2	C3 A2	D2 A2	D3 A2
					VARIATION REVISION LEVEL:	A2	A2	A2	A2	A2	A2	A2	A2
1	1	B-DD-M7606-0-0	M7606-AA		MICROVAX II W/1MB,FP,INCLUDES TI	1	1	-	-	-	-	-	-
2	2	B-DD-M7606-0-0	M7606-BA		M7606-AA W/NO FP (CPU,1MB) = M76	-	-	1	1	-	-	-	-
3	3	B-DD-M7606-0-0	M7606-CA		M7606-AA W/256KB MEM (CPU,256KB,	-	-	-	-	1	1	-	-
4	4	B-DD-M7606-0-0	M7606-DA		M7606-AA W/256KB MEM,NO FP = M76	-	-	-	-	-	-	1	1
5	5	K-PL-7022382-0-DBP	7022382-02		BA123-A ACCESSORY KIT	1	1	1	1	1	1	1	1
6	6	B-DD-7022380-0-DBU	7022380-01		BA123-A BASIC ENCLOSURE (120V)	1	-	1	-	1	-	1	-
7	7	B-DD-7022380-0-DBU	7022380-02		BA123-A BASIC ENCLOSURE (240V)	-	1	-	1	-	1	-	1
8	8	B-DD-5416744-0-0	5416744-01		FUNCTION SEL/SLU CONSOLE CONNECT	1	1	1	1	1	1	1	1
9	9	A-PS-1700712-0-0	1700712-02	A	WIRE HARN ASSY 20COND 30AWG 20SK	1	1	1	1	1	1	1	1
10	10	A-PS-1700624-0-0	1700624-01	A	CABLE ASSY,10COND,FLAT,10(2X05)I	1	1	1	1	1	1	1	1
11	11	A-PS-9010174-0-0	9010174-00	C	SCREW,SEMS PAN PHIL 6-	4	4	4	4	4	4	4	4
12	12	D-MD-7431480-0-0	7431480-03	A	MEDALLIAN SYSTEM LOGO (630QB)	1	1	1	1	1	1	1	1
13	13	A-PS-9009257-0-0	9009257-02	D	RING,RETAINER EXTERNAL FOR .188	2	2	2	2	2	2	2	2
14	14	A-PS-3617880-0-0	3617880-02		LABEL,FCC,CLASS A,PROCESSOR	1	1	1	1	1	1	1	1
15	15	A-PS-3624471-0-0	3624471-01	A	LABEL,BUSINESS COMP BA123-A2	1	-	1	-	1	-	1	-
16	16	A-PS-3624471-0-0	3624471-02	A	LABEL,BUSINESS COMP BA123-A3	-	1	-	1	-	1	-	1
17	17	A-PS-1700198-0-0	1700198-00	B	PWR CORD,TERM 3-18 250	-	REF	-	REF	-	REF	-	REF
18	18	A-PS-1700199-0-0	1700199-00	A	PWR CORD,TERM 3 250	-	REF	-	REF	-	REF	-	REF
19	19	A-PS-1700209-0-0	1700209-00	A	PWR CORD,TERM 3- .75MM 5A 250	-	REF	-	REF	-	REF	-	REF
20	20	A-PS-1700210-0-0	1700210-01	A	PWR CORD,TERM 3- .75MM 250V 6	-	REF	-	REF	-	REF	-	REF
21	21	A-PS-1700310-0-0	1700310-01	A	PWR CORD,TERM 3- .75MM 250	-	REF	-	REF	-	REF	-	REF
22	22	A-PS-1700364-0-0	1700364-01	A	PWR CORD,TERM 3- .75MM 250V	-	REF	-	REF	-	REF	-	REF
23	23	D-AR-7022380-0-DBU			BA123-A SYSTEM ARRANGEMENT	REF	REF	REF	REF	REF	REF	REF	REF
24	24	B-DD-M9047-0-0	M9047-00		QBUS GRANT CONTINUITY,1ST USED I	A/R	A/R	A/R	A/R	A/R	A/R	A/R	A/R
25	25	A-PS-3617674-0-0	3617674-22		LABEL,SERIAL/POWER,W/UL & CSA MA	A/R	A/R	A/R	A/R	A/R	A/R	A/R	A/R

REVISION HISTORY			BASIC PART NO: 630QB			
ENG	ECO NUMBER	REV	SECTION A OF A			
JN	630QB-ML001	B	SECTION.VARIATION INDEX [A]A2,A3,B2,B3,C2,C3, D2,D3	DRN: D. RICHARD	DATE: 19-FEB-85	D I G I T A L
			[B]	CHK'D: D. HEALY	DATE: 19-MAR-85	TITLE PARTS LIST 630QB MICRO VAX II WORLD BOX
			[C]	DES.ENG: J. NICHOLS	DATE: 19-MAR-85	DOCUMENT NUMBER: SIZE K, CODE PL, NUMBER 630QB-0-DBP, REV B
			[D]	RESP.ENG.: J. NICHOLS	DATE: 19-MAR-85	
			[E]	MFG.ENG.: K. WORTMAN	DATE: 19-MAR-85	RELEASE DATE: 07-MAY-85
			[F]	ASSEMBLY NUMBER: D-UA-630QB-0-DBU	TOP DOCUMENT NUMBER: B-DD-630QB-0-DBU	FILE NAME: ML863B.PLS / EDIT # 14

LINE ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION A2	A3	B2	B3	C2	C3	D2	D3
				VARIATION REVISION LEVEL:	A2	A2	A2	A2	A2	A2	A2	A2

26 NOTE: DEPENDING ON RAM VENDOR, MODULE MAY BE STAMPED AD/AH,BC/BH, CC/CH, DC/DH

D I G I T A L	TITLE 630QB MICRO VAX II WORLD BOX	SECTION A OF A	SIZE K	CODE PL	DOCUMENT NUMBER 630QB-0-DBP	REV B

DRAWING DIRECTORY

UNIT VARIATIONS

VAR	TITLE
63008-A2	MICRO VAX II WORLD BOX 1 MB FP 120V
63008-A3	MICRO VAX II WORLD BOX 1 MB FP 240V
63008-B2	MICRO VAX II WORLD BOX 1 MB NO FP 120V
63008-B3	MICRO VAX II WORLD BOX 1 MB NO FP 240V
63008-C2	MICRO VAX II WORLD BOX 256 KB FP 120V
63008-C3	MICRO VAX II WORLD BOX 256 KB FP 240V
63008-D2	MICRO VAX II WORLD BOX 256 KB NO FP 120V
63008-D3	MICRO VAX II WORLD BOX 256 KB NO FP 240V

FILE NAME: DD-6300B-0-DBUA

REVISIONS		
REV.	CHANGE NO.	CHK
A	INITIAL	

USED ON OPTION/MODEL

SHEET 1 OF 3

DRN. D. HEALY	DATE 25FEB85	
CHK'D D. HEALY	DATE 19MAR85	
PROJ. ENG. J. NICHOLS	DATE 19MAR85	
PROD. K. WORTMAN	DATE 19MAR85	
TOP DOC. B-DD-6300B-0-DBU		

TITLE

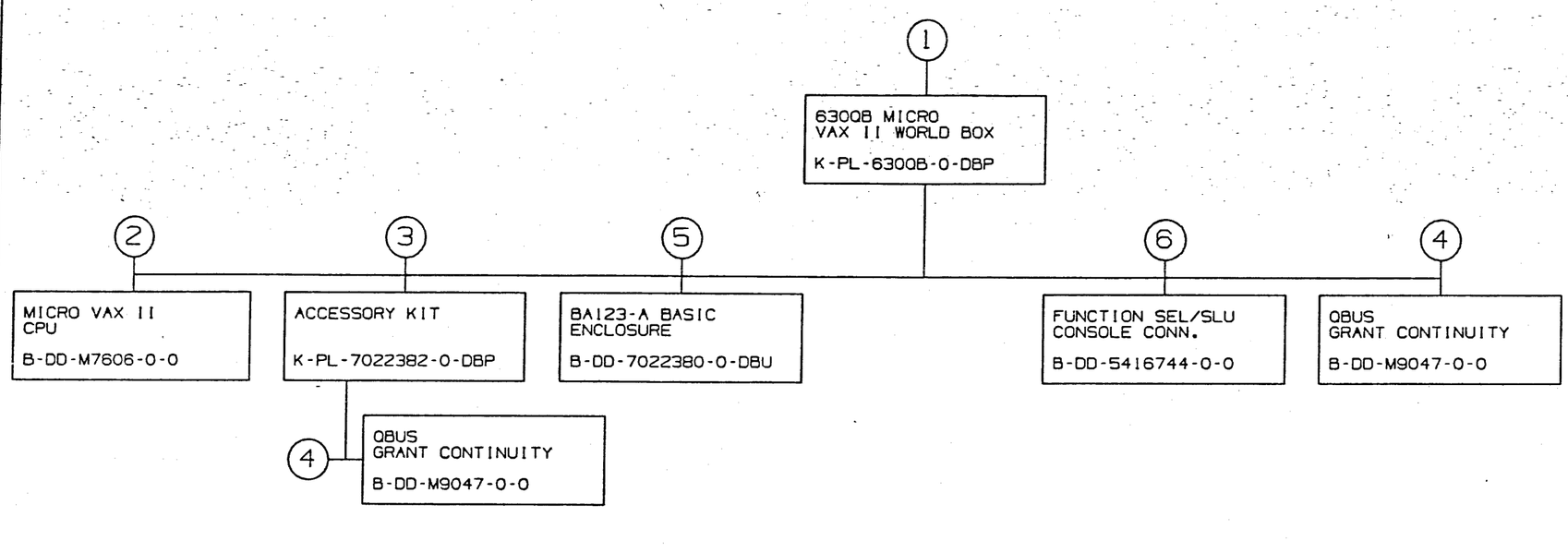
digital

6300B MICRO VAX II WORLD BOX

SIZE	CODE	NUMBER	REV.
B	DD	6300B-0-DBU	A

DIST.

MLOI



TITLE: 6300B MICRO VAX II WORLD BOX	SHEET 2 OF 3	SIZE	CODE	NUMBER	REV.
		B	DD	6300B-0-DBU	A

FIND NO.	DRAWING NO.	DESCRIPTION	TYPE
1	MP-02071-01	6300B MICRO VAX II WORLD BOX (MP)	-
	B-TC-6300B-0-DBU	6300B MICRO VAX II WORLD BOX (TC)	-
	D-UA-6300B-0-DBU	6300B MICRO VAX II WORLD BOX	E/M
	K-PL-6300B-0-DBP	6300B MICRO VAX II WORLD BOX (PL)	E/M
	A-PS-1700712-0-0	CABLE ASSY, 20 PIN	E/M
	A-PS-1700624-0-0	CABLE CONSOLE BACKPLANE	E/M
	D-MD-7431480-0-DBU	MEDALLIAN SYSTEM LOGO (6300B)	E/M
	A-PS-3617880-0-0	LABEL, FCC CLASS A PROCCESSOR	M
	A-PS-3624471-0-0	LABEL, BUSINESS COMPUTER	M
2	B-DD-M7606-0-0	MICRO VAX II CPU	E/M
3	K-PL-7022382-0-DBP	ACCESSORY KIT	E/M
	A-PS-1700301-0-0	CABLE ASSY, 7 COND	E/M
	A-PS-3622092-0-0	LABEL, LCPS CONFIGURATION	M
	A-PS-3624251-0-0	LABEL, MULTI LINGUAL F. PANEL	M
4	B-DD-M9047-0-0	O BUS GRANT CONTINUITY CARD	E/M
5	B-DD-7022380-0-DBU	BA123-A BASIC ENCLOSURE	E/M
6	B-DD-5416744-0-0	FUNCTION SEL/SLU CONSOLE CONN.	E/M

FIND NO.	DRAWING NO.	DESCRIPTION	TYPE

TYPE: E ELECTRICAL
M MECHANICAL
E/M ELECTRO/MECHANICAL

digital

TITLE: 6300B MICRO VAX II WORLD BOX

SHEET 3 OF 3 | SIZE B | CODE DD | NUMBER 6300B-0-DBU | REV. A

DRB 108A

SIZE	CODE	NUMBER	REV
B	DD	M7606-0-0	H

DRAWING NO.	NO. OF SHTS.	PART NO.	DESCRIPTION	REVISIONS																	
		M7606	KA630	B1	C1	D1	E1	F1	H2	H2											
D-UA-M7606-0-0	1		KA630 UNIT ASSEMBLY	A	A	B	B	B	B	B											
K-PL-M7606-0-DBP	2		KA630 PARTS LIST	A	B	C	D	E	F	H											
K-PC-M7606-0-DBJ	1		P.C. DESIGN DATA BASE	E	E	E	E	E	E	E											
		5016523-01	ETCHED CIRCUIT BOARD	E1	E1	E1	E1	E1	E1	E1											
B-DD-5016523-0-0	1		DRAWING DIRECTORY	A	A	A	A	A	A	A											
B-CS-M7606-0-1	1		M7606 DRAWING DIRECTORY	-	B	B	B	B	B	B											
B-CS-M7606-0-2	1		MICROVAX II SYSTEM	-	B	B	B	B	B	B											
B-CS-M7606-0-3	1		KA630-UVAX ON Q22 BUS	-	B	B	B	B	B	B											
B-CS-M7606-0-4	1		UVAX & FPU	-	B	B	B	B	B	B											
B-CS-M7606-0-5	1		UVAX & FPU PINOUTS	-	-	-	-		A	A											
B-CS-M7606-0-6	1		ADDRESS LATCH/LOCAL MEMORY DECODE	-	B	B	B	B	B	B											
B-CS-M7606-0-7	1		MEMORY SUBSYSTEM	-	B	B	B	B	B	B											
B-CS-M7606-0-8	1		Q22 BUS INTERFACE GATE ARRAY	-	B	B	B	B	B	B											
B-CS-M7606-0-9	1		Q22 BUS INTERFACE GATE ARRAY	-	B	B	B	B	B	B											
B-CS-M7606-0-10	1		DC380 PAD ASSIGNMENT TOP VIEW LL5320 IN 144 PIN GRID ARRAY	-	B	B	B	B	B	B											
B-CS-M7606-0-11	1		REFRESH LOGIC/COUNTER	-	B	B	B	B	B	B											
B-CS-M7606-0-12	1		DIVIDE BY 12	-	B	B	B	B	B	B											
B-CS-M7606-0-13	1		SYNCHRONOUS 3 BIT COUNTER	-	B	B	B	B	B	B											

NOTES:

NOTE: MODULE PART REV H' WAS USED FOR VAXSTATION FIELD UPGRADE KIT ONLY.
M7606 ECO-00006 REWORKED VARIATION M7606 AH TO EITHER M7606-ZS (NEW NEC) M7606-ZP (MITSUBIRSHI) M7606 OR M7606-ZF (HITACHI). THERE WAS NO PART REV CHANGE.

REVISION HISTORY																					
REV.	A	B	C	D	E	F	H														
ECO NO.	INIT	ML001	ML002	ML003	ML004	ML005	ML006														
DATE	5/84	5/85	6/85	7/85	8/85	1/86	3/86														

digital

DRN. D.DROZD	DATE 5/17/84	TITLE KA630
CHK'D E.LANDRY	DATE 5/17/84	DOCUMENT NUMBER
DES. ENG. B.MASKAS	DATE 5/17/84	SIZE B / CODE DD / NUMBER M7606-0-0 / REV H
RESP. ENG. B.MASKAS	DATE 5/17/84	— / SHEET 1 OF 4
MFG. ENG. B.SCHULTE	DATE 9/24/84	

DRB 126C
EN-01242-16-REVA(396)

DRAWING NO.	NO. OF SHTS.	PART NO.	DESCRIPTION	REVISIONS
B-CS-M7606-0-14	1		VECTOR HACK	- B B B B B B
B-CS-M7606-0-15	1		INVERTING MUX LOGIC	- B B B B B B
B-CS-M7606-0-16	1		4 to 1 MUX	- B B B B B B
B-CS-M7606-0-17	1		Q-BUS SUPPORT LOGIC	- B B B B B B
B-CS-M7606-0-18	1		BLK MD CTR LOGIC	- B B B B B B
B-CS-M7606-0-19	1		TOGGLE FLOP	- B B B B B B
B-CS-M7606-0-20	1		Q-BUS SUPPORT LOGIC	- B B B B B B
B-CS-M7606-0-21	1		Q-BUS SUPPORT LOGIC	- B B B B B B
B-CS-M7606-0-22	1		Q-BUS SUPPORT LOGIC	- B B B B B B
B-CS-M7606-0-23	1		Q-BUS SUPPORT LOGIC	- B B B B B B
B-CS-M7606-0-24	1		POWER BUFFER MACRO	- B B B B B B
B-CS-M7606-0-25	1		BIDIRECT BUFFER	- B B B B B B
B-CS-M7606-0-26	1		MUX LOGIC	- B B B B B B
B-CS-M7606-0-27	1		TRANSLATION MAP GROUP	- B B B B B B
B-CS-M7606-0-28	1		KA630 Q-BUS INTERFACE	- B B B B B B
B-CS-M7606-0-29	1		UVAX INTERFACE GATE ARRAY	- B B B B B B
B-CS-M7606-0-30	1		DC379 PAD ASSIGNMENT TOP VIEW LL5320 IN 144 PIN GRIP ARRAY	- B B B B B B
B-CS-M7606-0-31	1		UVAX INTERFACE GATE ARRAY DATA PATH	B B B B B B
B-CS-M7606-0-32	1		UVDAL I/O BUFFERS, ADDR LATCHES	- B B B B B B

NOTES:

REVISION HISTORY	A	B	C	D	E	F	H
ECO NO.	INIT	ML001	ML002	ML003	ML004	ML005	ML006
DATE	5/84	5/85	6/85	7/85	8/85	1/86	3/86

digital

DRN. D.DROZD	DATE 5/17/84	TITLE KA630
CHK'D E.LANDRY	DATE 5/17/84	DOCUMENT NUMBER
DES. ENG. B.MASKAS	DATE 5/17/84	SIZE B / CODE DD / NUMBER M7606-0-0 / REV. H
RESP. ENG. B.MASKAS	DATE 5/17/84	SHEET 2 OF 4
MFG. ENG. B.SCHULTE	DATE 9/24/84	

DRB 126C
EN-01242-16-REVA(396)

SIZE	CODE	NUMBER	REV
B	DD	M7606-0-0	H

DRAWING NO.	NO. OF SHTS.	PART NO.	DESCRIPTION	REVISIONS
B-CS-M7606-0-33	1		ADDRESS DECODER	- B B B B B B
B-CS-M7606-0-34	1		EXCEPTIONS AND INTERRUPTS	- B B B B B B
B-CS-M7606-0-35	1		UVAX INPUTS AND I/O PINS	- B B B B B B
B-CS-M7606-0-36	1		BOOT/DIAG REG., MEM ERR ADDR REG.	- B B B B B B
B-CS-M7606-0-37	1		EPR BUS, X DAL BUS	- B B B B B B
B-CS-M7606-0-38	1		INTERNAL DATA BUSES	- B B B B B B
B-CS-M7606-0-39	1		MISC. CONTROL STROBES	- B B B B B B
B-CS-M7606-0-40	1		RESET COUNTER, POWER UP/DOWN CNTRL	- B B B B B B
B-CS-M7606-0-41	1		MEMORY SYSTEM ERROR REGISTER	- B B B B B B
B-CS-M7606-0-42	1		TIME OF YEAR (TOY) CLOCK	- B B B B B B
B-CS-M7606-0-43	1		CONSOLE SERIAL LINE INTERFACE	- B B B B B B
B-CS-M7606-0-44	1		LEDS AND CONFIGURATION CONNECTOR	- B B B B B B
B-CS-M7606-0-45	1		DECOUPLING CAPACITORS	- B B B B B B
B-CS-M7606-0-46	1		KA630 STATE MACHINES	- B B B B B B
B-CS-M7606-0-47	1		UVAX CYCLE CONTROLLER	- B B B B B B
B-CS-M7606-0-48	1		MEMORY SEQUENCER	- B B B B B B
B-CS-M7606-0-49	1		MEMORY SEQUENCER SUPPORT	- B B B B B B
B-CS-M7606-0-50	1		Q22 BUS STATE MACHINES	- B B B B B B
D-CS-M7606-0-51	1		KA630 MEMORY ARBITER LISTING	- - - - - A A

NOTES:

REVISION HISTORY								
REV.	A	B	C	D	E	F	H	
ECO NO.	INIT	ML001	ML002	ML003	ML004	ML005	ML006	
DATE	5/84	5/85	6/85	7/85	8/85	1/86	3/86	

digital

DRN.	D.DROZD	DATE	5/17/84
CHK'D	E.LANDRY	DATE	5/17/84
DES. ENG.	B.MASKAS	DATE	5/17/84
RESP. ENG.	B.MASKAS	DATE	5/17/84
MFG. ENG.	B.SCHULTE	DATE	9/24/84

TITLE: KA630

DOCUMENT NUMBER

SIZE	CODE	NUMBER	REV
B	DD	M7606-0-0	H

SHEET 3 OF 4

SIZE	CODE	NUMBER	REV
B	DD	M7606-0-0	H

DRAWING NO.	NO. OF SHTS.	PART NO.	DESCRIPTION	REVISIONS																	
B-CS-M7606-0-52	1		KA630 MEMORY SYSTEM ARBITER STATE FLOW DIAGRAMS	-	B	B	B	B	B	B											
B-CS-M7606-0-53	1		KA630 MEMORY SYSTEM ARBITER STATE FLOW DIAGRAMS	-	B	B	B	B	B	B											
D-CS-M7606-0-54	1		KA630 LOCAL I/O CONTROL MACHINE	—	—	—	—	—	A	A											
.			UL TESTING	-	-	-	-	—													
B-CS-M7606-0-55	1		KA630 LOCAL I/O BUS CONTROL	-	B	B	B	B	B	B											
D-CS-M7606-0-56	1		KA630 Q-BUS ARBITRATION CONTROL MACHINE LISTING	-	-	-	-	—	A	A											
B-CS-M7606-0-57	1		Q-BUS ARBITRATION CONTROLLER DETAILED CONTROL PLOW DIAGRAM	-	B	B	B	B	B	B											
D-CS-M7606-0-58	1		Q22 BUS MASTER CONTROL MACHINE LISTING	-	-	-	-	—	A	A											
B-CS-M7606-0-59	1		Q22 BUS MASTER CONTROL MACHINE PLOW DIAGRAM	-	B	B	B	B	B	B											
D-CS-M7606-0-60	1		Q22 BUS SLAVE CONTROL MACHINE LISTING	-	-	-	-	—	A	A											
B-CS-M7606-0-61	1		Q22 BUS SLAVE CONTROL MACHINE PLOW DIAGRAM	-	B	B	B	B	B	B											
B-CS-M7606-0-62	1		Q22 BUS SLAVE CONTROL MACHINE PLOW DIAGRAM	-	B	B	B	B	B	B											
D-CS-M7606-0-63	1		IKKL RAS DECODE FROM (ETS) LISTING	-	-	-	-	—	A	A											
D-CS-M7606-0-64	1		PALASM LISTING FOR PALISLSA DEVICES	-	-	-	-	—	A	A											
D-CS-M7606-0-65	1		MNEMONIC DICTORY	-	-	-	-	-	A	A											
K-DO-M7606-0-0	24		M7606 CROSS REF LIST	-	A	A	A	A	A	A											

NOTES:

REVISION HISTORY									
REV.	A	B	C	D	E	F	H		
ECO NO.	INIT	ML001	ML002	ML003	ML004	ML005	ML006		
DATE	5/84	5/85	6/85	7/85	8/85	1/86	3/86		

digital

DRN. D.DROZD	DATE 5/17/84	TITLE: KA630
CHK'D E.LANDRY	DATE 5/17/84	DOCUMENT NUMBER
DES. ENG. B.MASKAS	DATE 5/17/84	SIZE B / CODE DD / NUMBER M7606-0-0 / REV H
RESP. ENG. B.MASKAS	DATE 5/17/84	SHEET 4 OF 4
MFG. ENG. B.SCHULTE	DATE 9/24/84	

REWORK INSTRUCTIONS

1. COMPONENT DELETES
   - 2-1 DELETE E21 P/N 23035E6-00
   - 2-2 DELETE E22 P/N 23034E6-00
2. COMPONENT ADDS.
   - 2-3 DELETE E21 P/N 23063E6-00
   - 2-4 DELETE E22 P/N 23062E6-00

16

94 (QTY. 4)

C-3 REF

COMPONENT SIDE VIEW

J10 J11 J12 J13 J14 J2 J3

E45 E44 E43 E42 Y1 Y2 Y3

2-1 2-2 2-3 2-4

NOTES: 1. N1 NOT INSTALLED

STEP E	↑ Y AXIS ____ STEP ___ TIMES
REPEAT	→ X AXIS ____ STEP ___ TIMES

CHK	CHANGE NO	REV
	M7606 MOD	B

ETCH REV. F1

SIGNATURES	DATE
DRN.	
CHK'D.	
MECH. ENG.	
PROJ. ENG.	
PROD.	
SCALE	
SHT. OF	
NEXT HIGHER ASSY.	

digital

TITLE [illegible] A-B-C-D

SIZE	CODE	NUMBER	REV
D	UA	M7606	B

1 MS# [illegible]

KA630-AA,-AB,-AC,-AD (M7606) DRAWING DIRECTORY

DATA PATH

0	MICROVAX II SYSTEM
1	KA630 - uVAX on Q22 Bus
1.1	uVAX & FPU
1.1.1	uVAX & FPU PINOUTS
1.2	ADDRESS LATCH/LOCAL MEMORY DECODE
1.3	Memory Subsystem
1.4	Q22 Bus Interface Gate Array
	1.4.1-1.4.2, 1.4.1.1-1.4.1.9
1.5	Translation Map Group
1.6	KA630 QBUS INTERFACE
1.7	uVAX Interface Gate Array
	1.7.1-1.7.2, 1.7.2.1-1.7.2.10
1.8	TOY CLOCK
1.9	Console Serial Line Interface
1.10	LEDS and Configuration Connector
1.11	Decoupling Capacitors

CONTROL

2	KA630 State Machines
2.1	uVAX Cycle Controller
2.1.1	MEMORY SEQUENCER
2.1.2	MEMORY SEQUENCER SUPPORT
2.2	Q22 BUS STATE MACHINES

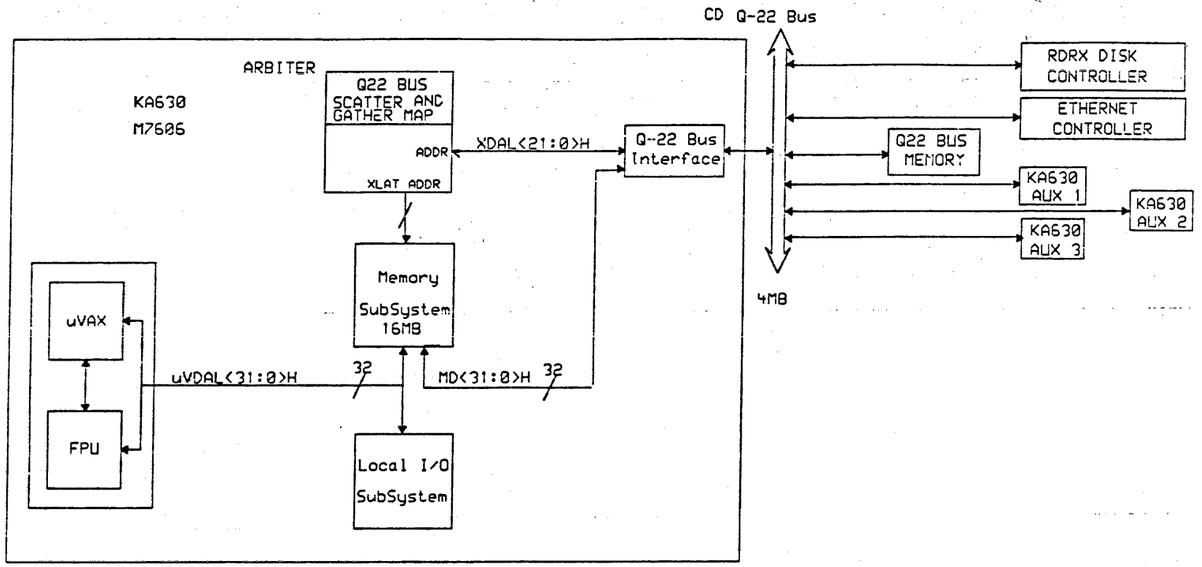
MISC.

3	KA630 MEMORY ARBITER LISTING
3.1-3.2	KA630 MEMORY ARBITER FLOW DIAGRAM
4	KA630 LOCAL I/O CONTROL MACHINE LISTING
4.1	KA630 LOCAL I/O CONTROL MACHINE FLOW DIAGRAM
5	Q22 BUS ARBITRATION CONTROL MACHINE LISTING
5.1	Q22 BUS ARBITRATION CONTROL MACHINE FLOW DIAGRAM
6	Q22 BUS MASTER CONTROL MACHINE LISTING
6.1	Q22 BUS MASTER CONTROL MACHINE FLOW DIAGRAM
7	Q22 BUS SLAVE CONTROL MACHINE LISTING
7.1-7.2	Q22 BUS SLAVE CONTROL MACHINE FLOW DIAGRAM
8	1KX4 RAS DECODE PROM (E79) LISTING
9	PALASM LISTINGS FOR PAL16L8A DEVICES
10	MNEMONIC DICTIONARY

DRAWING
TITLE=DIRECTORY
ABBREV=DIRECT
CIRCUIT←TYPE=DOCUMENTATION
LAST←MODIFIED=Sun Dec 9 16:50:34 1984

DEFINE
X←FIRST=0
X←STEP=SIZE

REVISION | CHK | CHANGE NO | REV
M7606 | JOE McMULLIN
digital
DRN. MASKAS & McNamara DATE 8-DEC-83 | ENG. MASKAS & McNamara DATE 8-DEC-83
CHK'D. MASKAS & McNamara DATE 8-DEC-83 | BOARD LOCATION: | SHEET OF
USRA: | FIRST USED ON OPTION/MODEL: | TOP DOCUMENT NUMBER:
TITLE: M7606 DRAWING DIRECTORY
SIZE D | CODE CS | NUMBER M7606-0-1 | REV



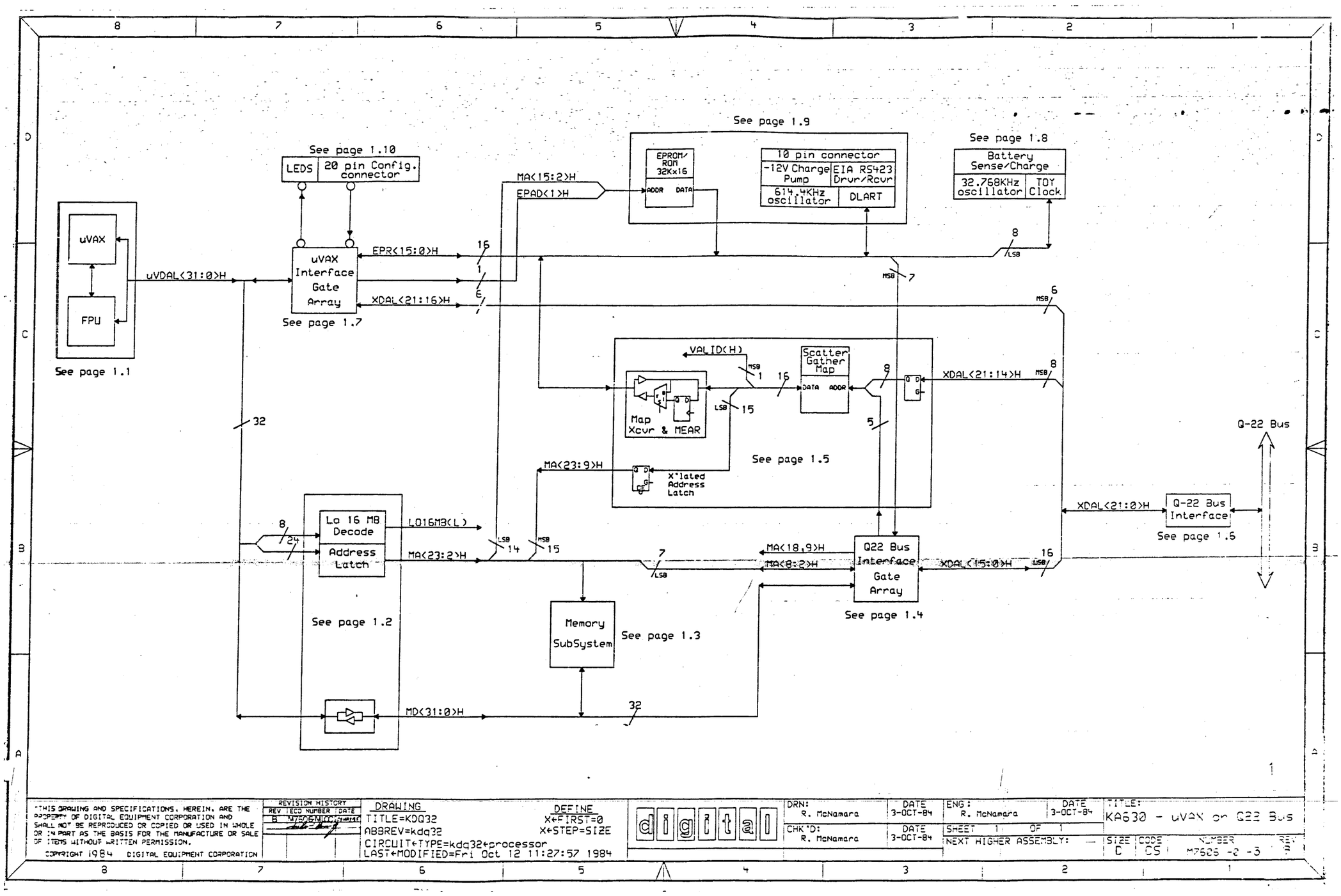
REVISION HISTORY		
REV	ECO NUMBER	DATE
B	INCREMENTAL RELEASE	26-MAR-84

DRAWING
TITLE=KASYSTEM
ABBREV=kasystem
CIRCUIT=TYPE=kaq32=processor
LAST=MODIFIED=Sun Oct 7 18:10:51 1984

DEFINE
X=FIRST=0
X=STEP=SIZE

digital

DRN: BARRY MASKAS	DATE 27-APR-84	ENG: BARRY MASKAS	DATE 27-APR-84	TITLE: MICROVAX II SYSTEM	
CHK'D: BARRY MASKAS	DATE 27-APR-84	SHEET 1 OF 1		SIZE C	CODE 05
		NEXT HIGHER ASSEMBLY:		NUMBER M7606-0-2	REV B



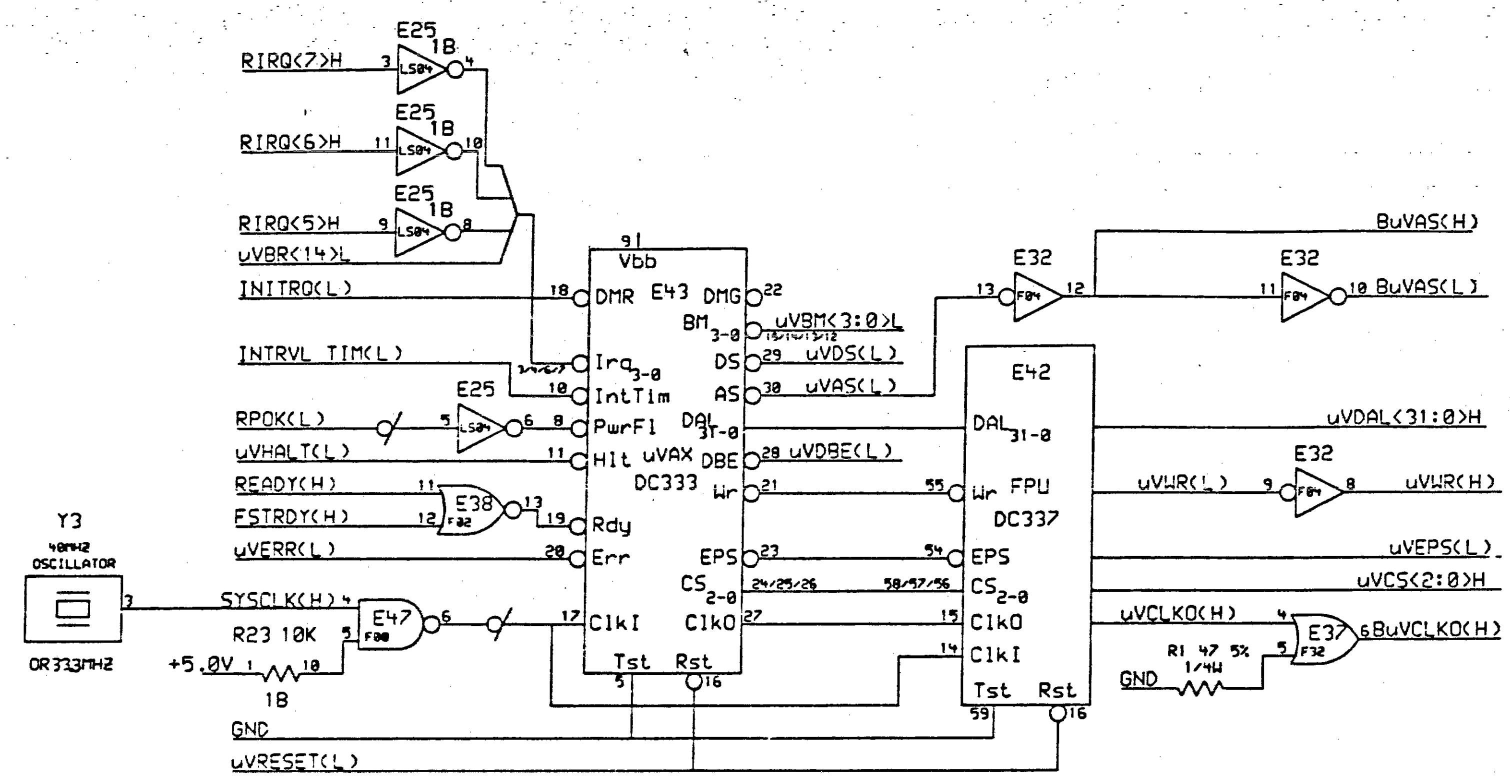
REVISION HISTORY

REV	ECO NUMBER	DATE
B	MYA0MIC	[illegible]

DRAWING
TITLE=KDQ32
ABSREV=kdq32
CIRCUIT+TYPE=kdq32+processor
LAST+MODIFIED=Fri Oct 12 11:27:57 1984

DEFINE
X+FIRST=0
X+STEP=SIZE

DRN: R. McNamara	DATE 3-OCT-84	ENG: R. McNamara	DATE 3-OCT-84	TITLE: KA630 - uVAX or Q22 Bus	
CHK'D: R. McNamara	DATE 3-OCT-84	SHEET 1 OF 1			
		NEXT HIGHER ASSEMBLY: —		SIZE C	CODE CS
				NUMBER M7606 -2 -3	REV B



uVAS(L) CYCLES

uVCS<2:0>H uVWR(L)

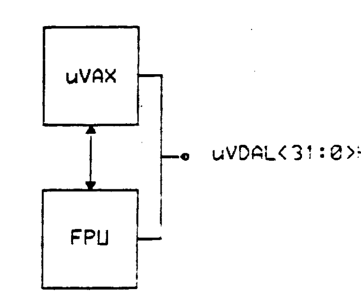
LHH	H	interrupt acknowledge (IAK)
HLL	H	read (I - stream)
HLH	H	read (lock)
HHx	H	read (D - stream)
HLH	L	write (unlock)
HHH	L	write (D - stream)

x => don't care

uVEPS(L) CYCLES

uVCS<2:0>H uVWR(L)

HLH	H	read data
HHH	H	read response (uVCS<2> pulled low by responder)
HLL	L	write command (fpu)
HLH	L	write data
HHL	L	write command (non-fpu)



REVISION HISTORY — REV | ECO NUMBER | DATE — B

DRAWING
TITLE=UVAX
ABBREV=UVAX+FPU
CIRCUIT+TYPE=uVAX/FPU
LAST+MODIFIED=Fri Nov 9 18:39:57 1984

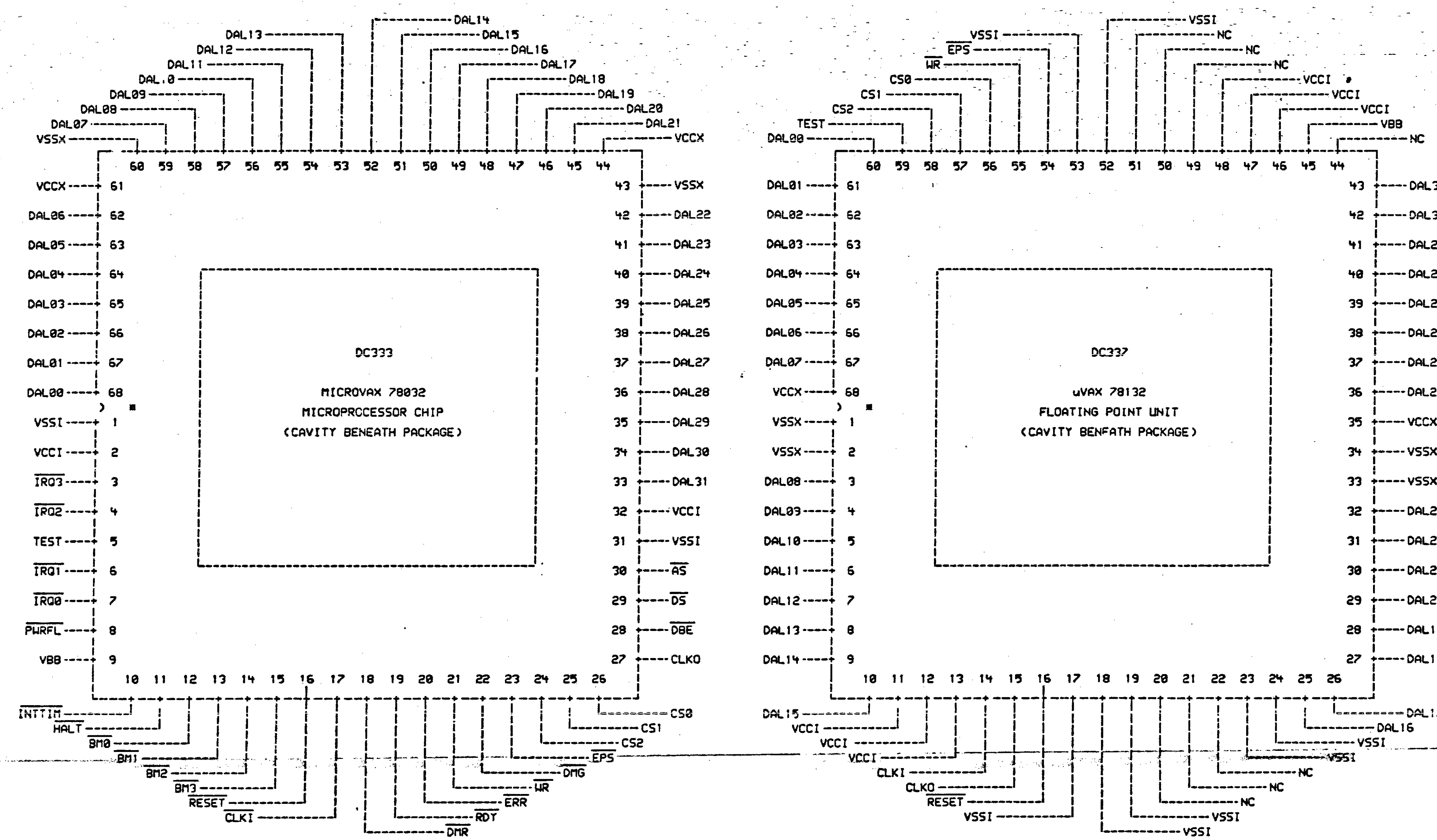
DEFINE
X+FIRST=0
X+STEP=SIZE

digital

DRN: BARRY MASKAS — DATE 3-OCT-84
CHK'D: BARRY MASKAS — DATE 3-OCT-84
ENG: BARRY MASKAS — DATE 3-OCT-84
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:

TITLE: uVAX & FPU

SIZE D | CODE CS | NUMBER M7606-2-1 | REV. B



1.1.1

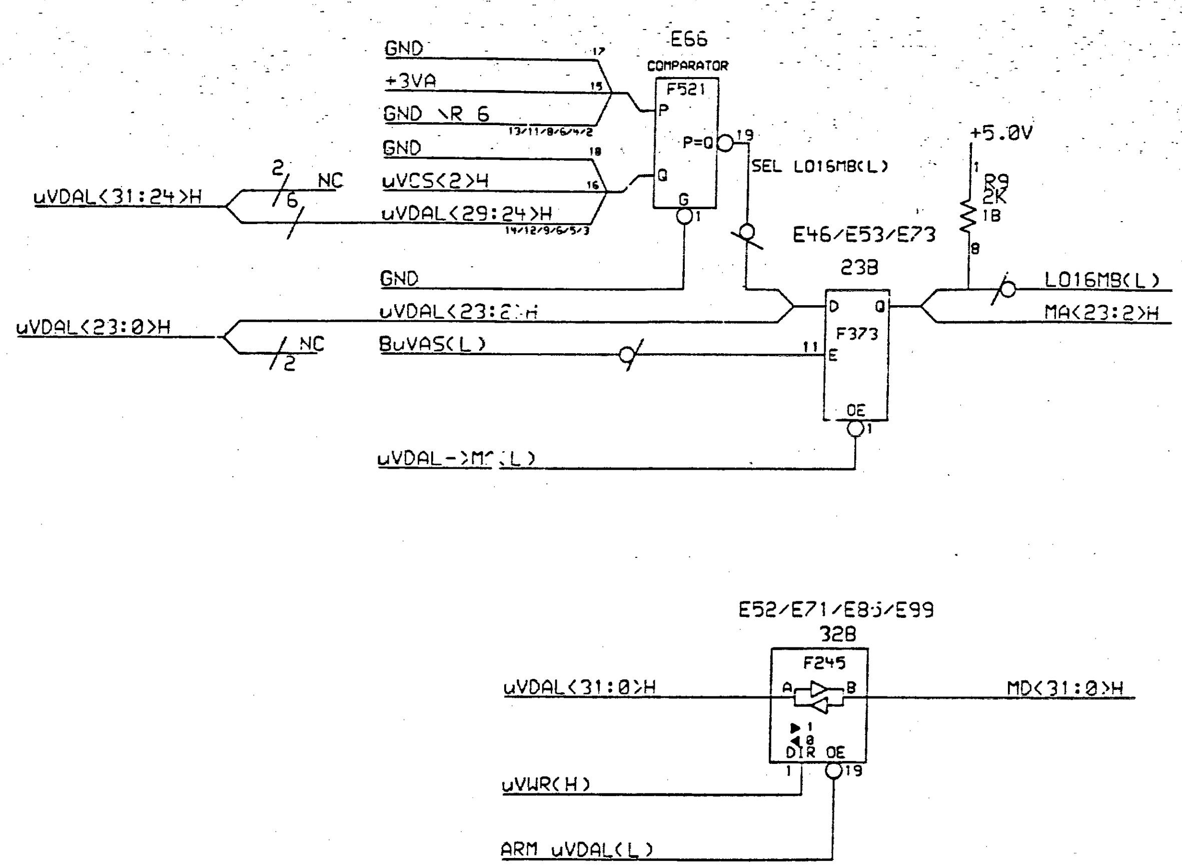
REVISIONS		
CHK	CHANGE NO.	REV

digital

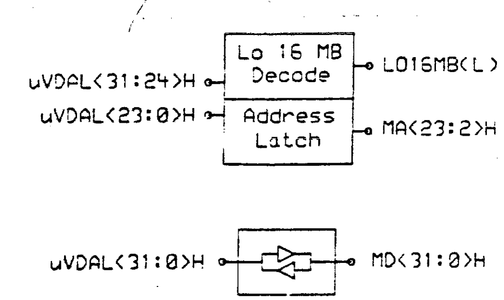
DRN.	DATE 12-AUG-85	ENG. R. MCNAMARA, DATE 12-AUG-85
CHK'D. R. MCNAMARA	DATE 12-AUG-85	BOARD LOCATION:
SUDCOM:(BOWEN)DC333.DRW 31-JUL-85 12:55	SHEET 1 OF 1	NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL:		

TITLE: UVAX & FPU PINOUTS

SIZE	CODE	NUMBER	REV.
D	CS	M7606-0-5	A



1.2



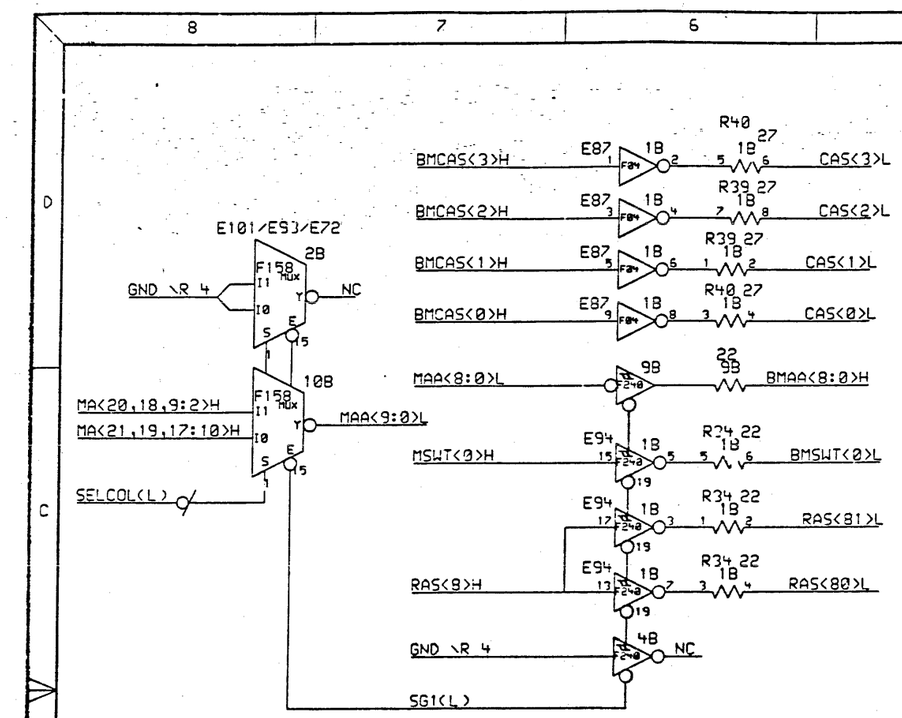
REVISION HISTORY

DRAWING
TITLE=ADDR LATCH
ABBREV=ADLATCH
CIRCUIT-TYPE=ADDR-LATCH
LAST-MODIFIED=Sat Oct 20 18:19:02 1984

DEFINE
X-FIRST=0
X-STEP=SIZE

digital

DRN: BARRY MASKAS DATE 3-OCT-84
ENG: BARRY MASKAS DATE 3-OCT-84
CHKD: BARRY MASKAS DATE 3-OCT-84
TITLE: ADDRESS LATCH/ LOCAL MEMORY DECODE
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:
SIZE D CODE CS NUMBER M7626 -0 -6 REV B



MODULE CD CONNECTORS

GND	CT1	GND	DT1
RAS<0>H	CU2	RAS<6>H	DU2
MSID<4>L	CT2		
MAA<8>L	CS2		
MAA<0>L	CR2	BMCAS<3>H	DR2
MAA<2>L	CP2	BMCAS<2>H	DP2
MAA<1>L	CN2	RAS<2>H	DN2
MSID<1>L	CM2	MSID<3>L	DM2
RAS<4>H	CL2	RAS<7>H	DL2
MSWT<1>H	CK2	RAS<3>H	DK2
MSID<0>L	CJ2	MSID<2>L	DJ2
BMCAS<1>H	CH2	MAA<6>L	DH2
RAS<1>H	CF2	MAA<3>L	DF2
BMCAS<0>H	CE2	MAA<4>L	DE2
RAS<5>H	CD2	MAA<5>L	DD2
GND	CC2	GND	DC2
MAA<9>L	CB2	MAA<7>L	DB2
+5.0V	CA2	+5.0V	DA2

E48/E54/E60/E67/E74/E81/E88/E95/E102

E49/E55/E61/E68/E75/E82/E89/E96/E103

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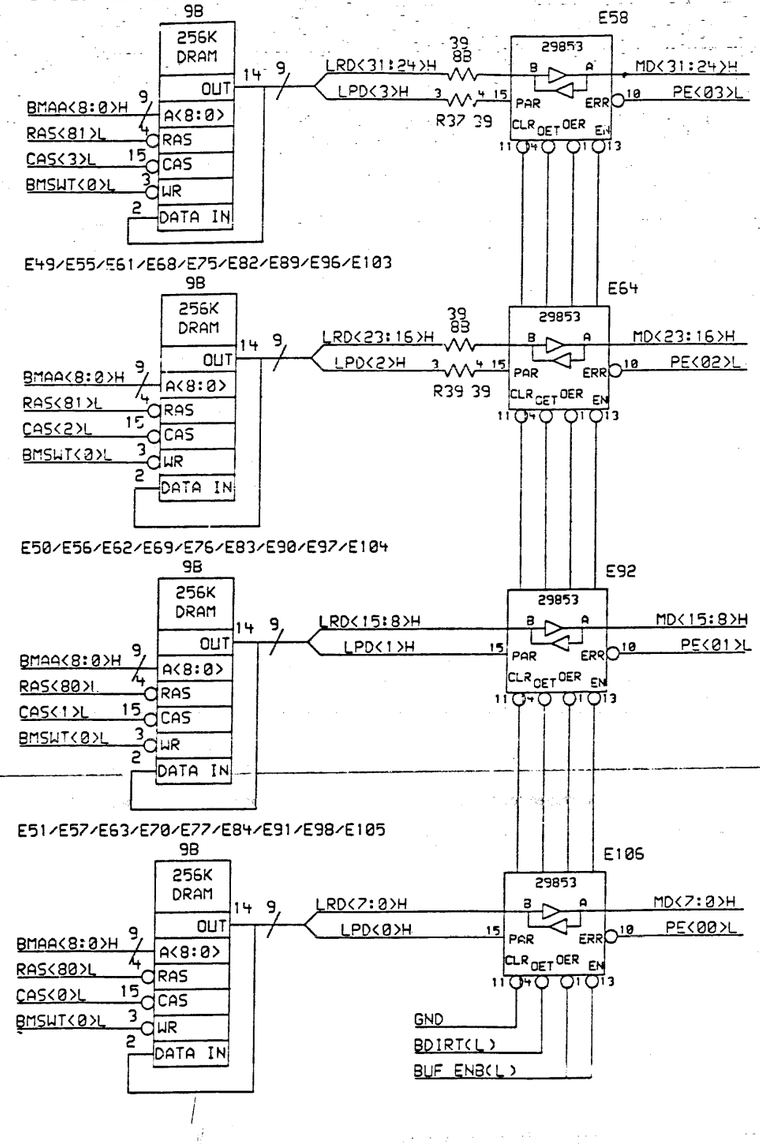
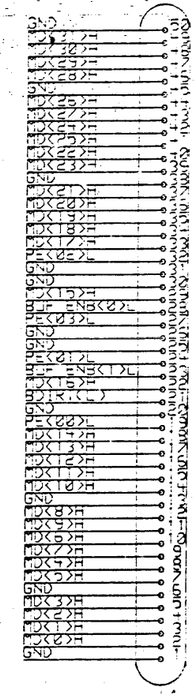


50 PIN MEMORY DATA CONNECTOR



1.3

MA<23:2>H

Memory SubSystem

MD<31:0>H

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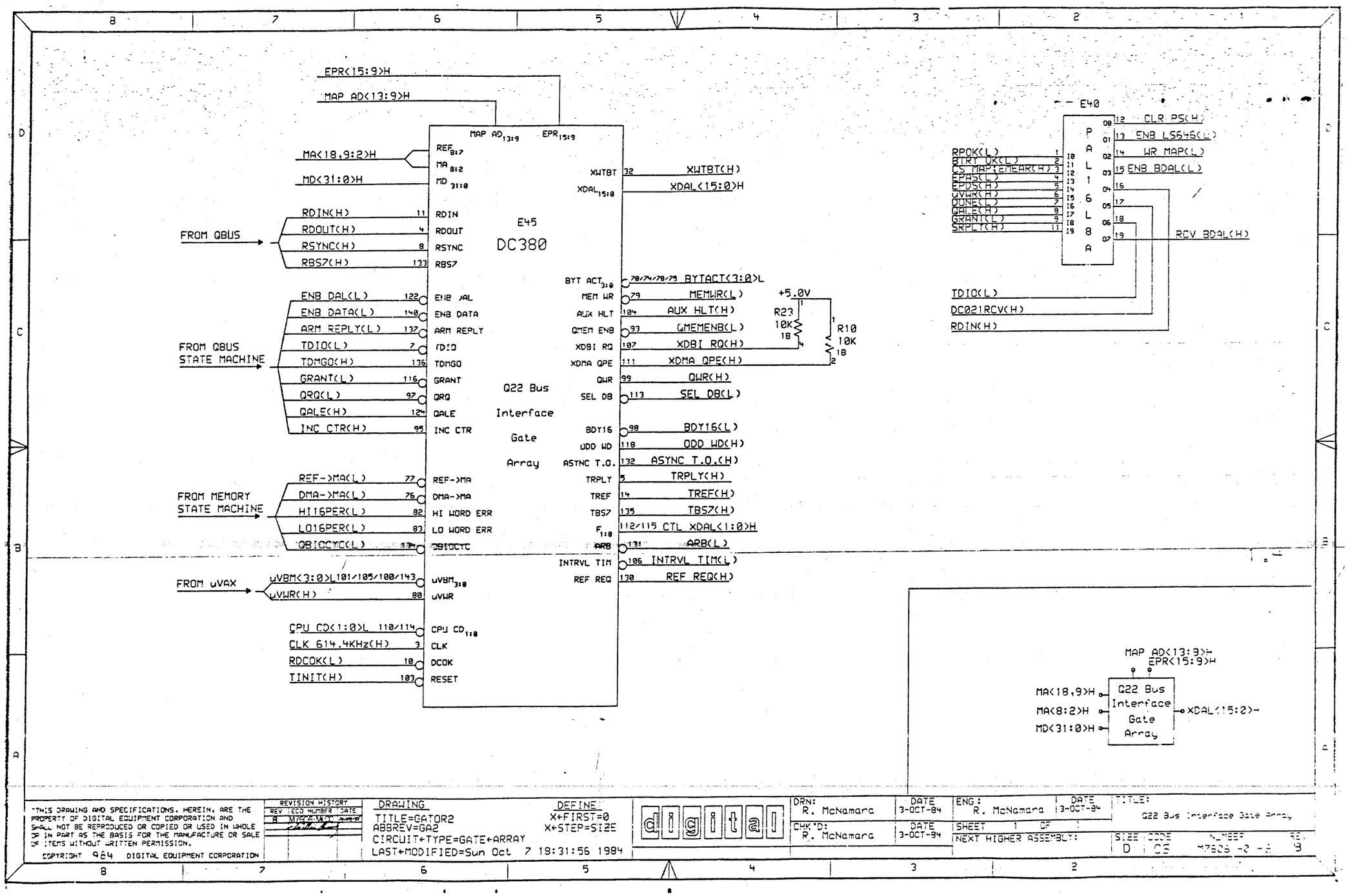
REVISION HISTORY		
REV	ECO NUMBER	DATE
H	M7606 MILCO	

DRAWING
TITLE←MEM
ABBREV←MEM
CIRCUIT←TYPE←MEMEORY
LAST←MODIFIED←Mon Oct 29 09:26:41 1984

DEFINE
X←FIRST←0
X←STEP←SIZE

DRN: BARRY MASKAS	DATE 3-OCT-84	ENG: BARRY MASKAS	DATE 3-OCT-84	TITLE: Memory SubSystem	
CHK'D: BARRY MASKAS	DATE 3-OCT-84	SHEET 1 OF 1		SIZE D	CODE 05
		NEXT HIGHER ASSEMBLY:		NUMBER M7606-0-0-7	REV 0



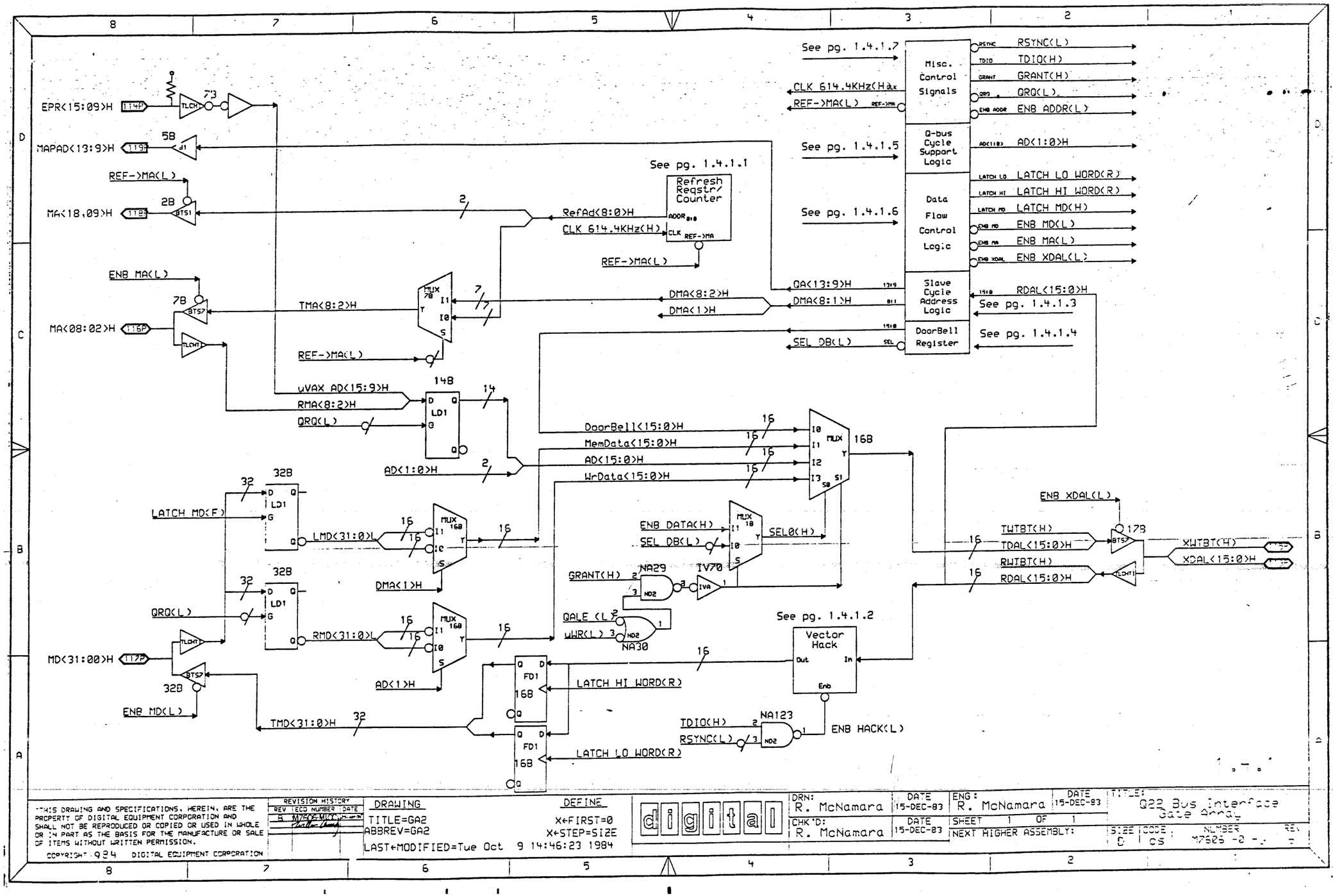
REVISION HISTORY
REV | ECO NUMBER | DATE
B | MACC-MAC | [illegible]

DRAWING
TITLE=GATOR2
ABBREV=GA2
CIRCUIT=TYPE=GATE=ARRAY
LAST=MODIFIED=Sun Oct 7 18:31:56 1984

DEFINE
X=FIRST=0
X=STEP=SIZE

DRN: R. McNamara	DATE 3-OCT-84	ENG: R. McNamara	DATE 3-OCT-84
CHK'D: R. McNamara	DATE 3-OCT-84	SHEET 1 OF 1	
NEXT HIGHER ASSEMBLY:			

TITLE: Q22 Bus Interface Gate Array
SIZE D | CODE 05 | NUMBER M7505-2-B | REV B



REVISION HISTORY

REV	ECO NUMBER	DATE
B	M7605 MUC	

DRAWING
TITLE=GA2
ABBREV=GA2
LAST←MODIFIED=Tue Oct 9 14:46:23 1984

DEFINE
X←FIRST=0
X←STEP=SIZE

DRN: R. McNamara	DATE 15-DEC-83	ENG: R. McNamara	DATE 15-DEC-83	TITLE: Q22 Bus Interface Gate Array	
CHK'D: R. McNamara	DATE 15-DEC-83	SHEET 1 OF 1			
		NEXT HIGHER ASSEMBLY:		SIZE C	CODE 05	NUMBER M7605 -2 -..	REV -

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
Q	72 VSS	68 MD25	64 MD21	63 MD15	61 MD11	57 MD5	56 MD1	53 MD29	51 MD26	50 MD22	47 MD16	44 MD12	42 MD6	39 MD0	36 VSS	Q
P	75 BYT,ACT0	71 MD27	67 MD23	65 MD17	62 MD13	59 MD7	58 MD3	52 MD31	48 MD28	46 MD24	43 MD18	40 MD14	38 MD8	35 MD2	32 XWTBT	P
N	78 BYT ACT1	74 BYT ACT2	70 BYT ACT3	69 MD19	66 VSS	60 MD9	55 VSS	54 VDD	49 MD30	45 VSS	41 MD20	37 VDD	34 MD10	31 MD4	28 XDAL15	N
M	80 UVWR	76 DMA->MA	73 VDD										33 XDAL12	29 XDAL13	27 XDAL14	M
L	83 LO WORD ERR	79 MEM WR	77 REF->MA		stand off						stand off		30 VSS	26 XDAL10	25 XDAL11	L
K	86 REF8	82 HI WORD ERR	81 VSS										24 XDAL7	23 XDAL8	21 XDAL9	K
J	87 MA7	84 MA8	85 REF7										19 VSS	22 XDAL5	20 XDAL6	J
H	89 MA5	88 MA6	90 VDD										18 VDD	16 XDAL3	17 XDAL4	H
G	92 MA3	94 MA4	91 VSS										13 XDAL0	12 XDAL1	15 XDAL2	G
F	93 QMEM ENB	95 INC CTR	96 MA2		stand off								9 VSS	10 DCOK	14 TREF	F
E	97 QRQ	98 BDY16	102 VSS								stand off		5 DOREPLY	7 TDIO	11 RDIN	E
D	99 QWR	101 UVBM3	105 UVBM2										extra pin	1 VDD	4 RDOUT	8 RSTNC	D
C	100 UVBM1	103 RESET	106 INTRVL TIM	109 VDD	113 SEL D8	117 VSS	121 EPR13	126 VDD	127 VSS	132 ASNYC T.O	138 VSS	141 MAP AD10	142 MAP AD13	2 MAP AD12	6 MAP AD11	C
B	104 AUX HLT	107 XDBI RQ	110 CPU CD1	112 F1	115 F0	118 ODD WD	120 EPR9	124 QALE	130 REF REQ	131 ARB	134 QBIOCYC	137 TRPLY	139 MAP AD9	143 UVBM0	3 CLK 614.4KHZ	B
A	108 VSS	111 XDMA QPE	114 CPU CD0	116 GRANT	119 EPR10	122 ENB ADDR	123 EPR11	125 EPR12	128 EPR14	129 EPR15	133 RBS7	135 TBS7	136 TDMGO	140 ENB DATA	144 VSS	A
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Footprint
Side 1 View
LSI5320
144 pin grid

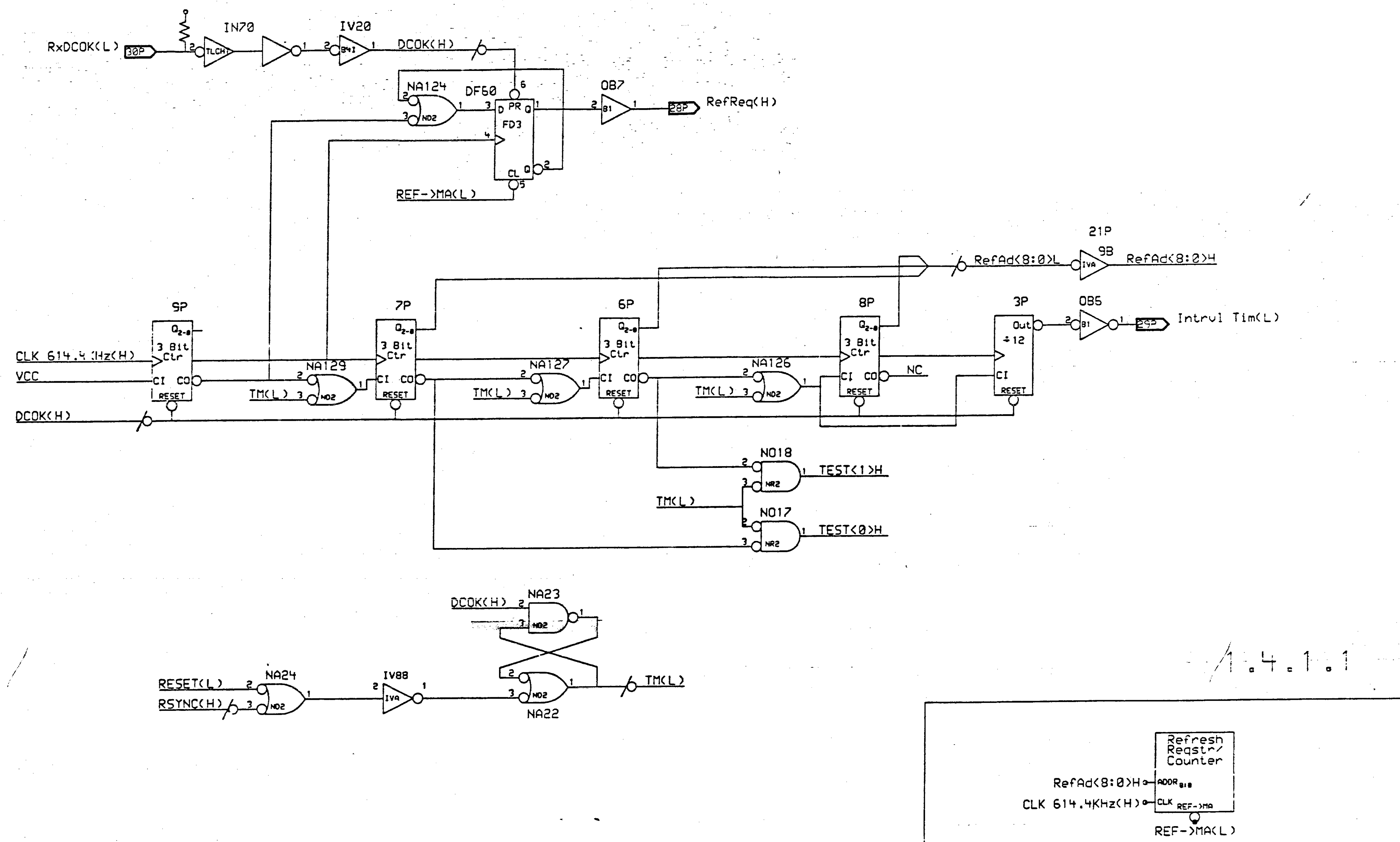
DC380

Q22 BUS
Interface
Gate Array

REVISION HISTORY		
REV	ECO NUMBER	DATE
B	M7605 V1.00	4-MAY-84

digital

DRN: R. McNamara	DATE 18-MAY-84	ENG: R. McNamara	DATE 18-MAY-84	TITLE: DC380 PAD ASSIGNMENT TOP VIEW LL5320 IN 144 PIN GRID ARRAY	
CHK'D: R. McNamara	DATE 18-MAY-84	SHEET 1 OF 1		SIZE D	CODE 05	NUMBER M7605 -2 -0	REV B
		NEXT HIGHER ASSEMBLY:			



1.4.1.1

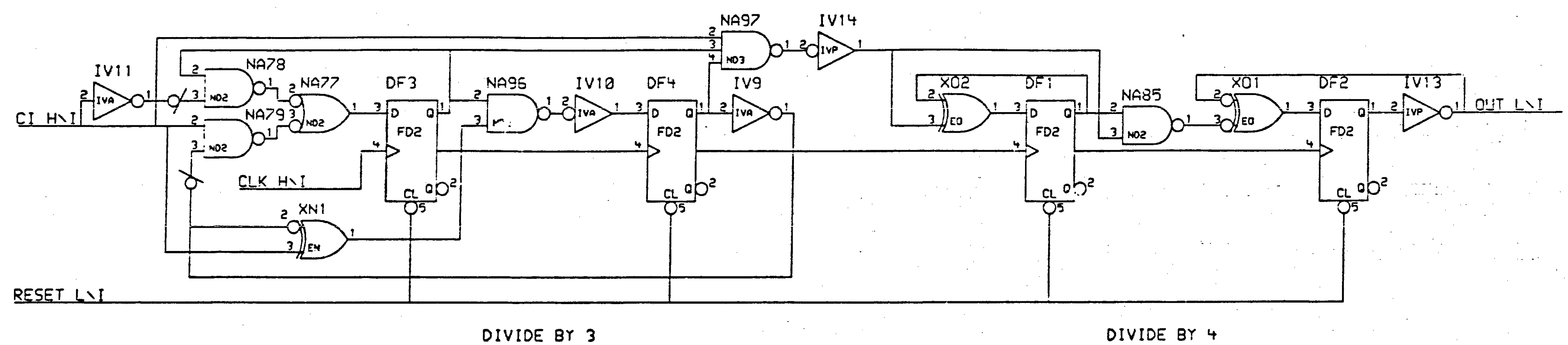
REVISION HISTORY

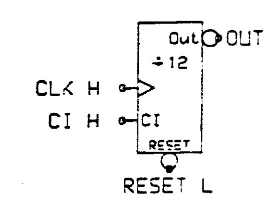
REV	ECO NUMBER	DATE
B	M7626-MCC	

DRAWING
LAST-MODIFIED=Wed Oct 10 19:06:07 1984

digital

DRN: R. McNamara	DATE 13-NOV-83	ENG: R. McNamara	DATE 13-NOV-83	TITLE: REFRESH LOGIC/COUNTER
CHK'D: R. McNamara	DATE 13-NOV-83	SHEET 1 OF 1		SIZE D CODE CS NUMBER M7626-0-11 REV B
		NEXT HIGHER ASSEMBLY:		





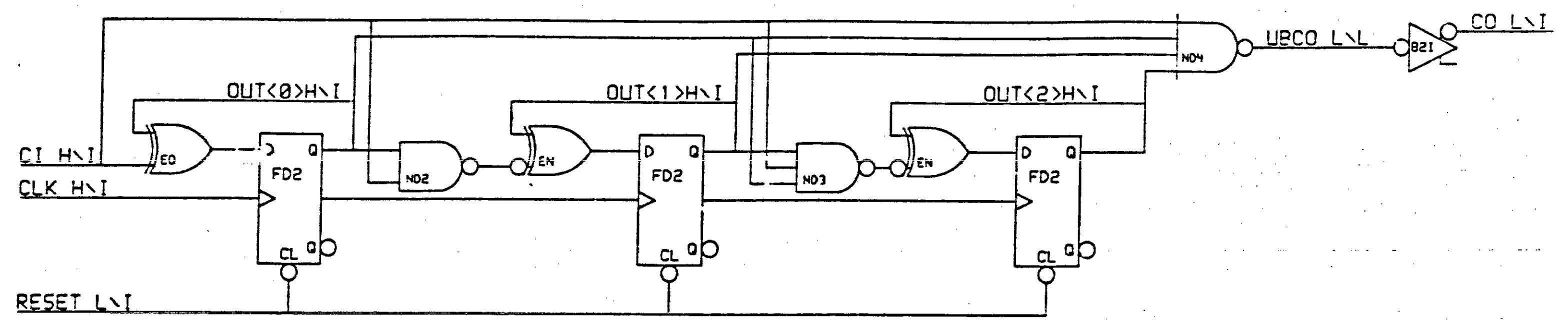
REVISION HISTORY — REV | ECO NUMBER | DATE

DRAWING
TITLE=DIV BY 12
ABBREV=DIV12
LAST←MODIFIED=NOT WRITTEN

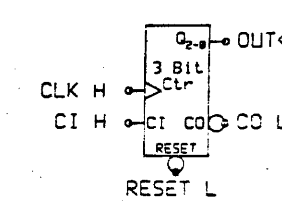
DEFINE
X←FIRST=0
X←STEP=SIZE

digital

DRN: R. McNamara	DATE 13-NOV-83	ENG: R. McNamara	DATE 13-NOV-83	TITLE: Divide by 12
CHK'D: R. McNamara	DATE 13-NOV-83	SHEET 1 OF 1		
		NEXT HIGHER ASSEMBLY:		SIZE C · CODE CS · NUMBER · REV. B



1.4.1.1.2



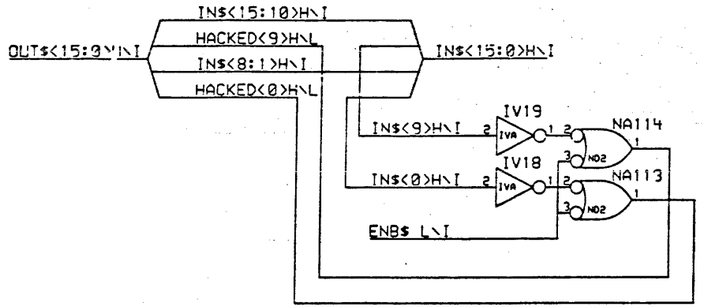
REVISION HISTORY		
REV	ECO NUMBER	DATE
B	M7606 M.CO	

DRAWING
TITLE=3 BIT CTR
ABBREV=3BCTR
CIRCUIT←TYPE=3BITCTR
LAST←MODIFIED=Sat Oct 20 18:47:47 1984

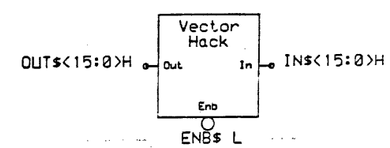
DEFINE
X←FIRST=0
X←STEP=SIZE

digital

DRN: R. McNamara	DATE 6-NOV-83	ENG: R. McNamara	DATE 6-NOV-83	TITLE: Synchronous 3 Bit Counter
CHK'D: R. McNamara	DATE 6-NOV-83	SHEET 1 OF 1	NEXT HIGHER ASSEMBLY:	SIZE D CODE CS NUMBER M7606 -0 -13 REV B



1.4.1.2



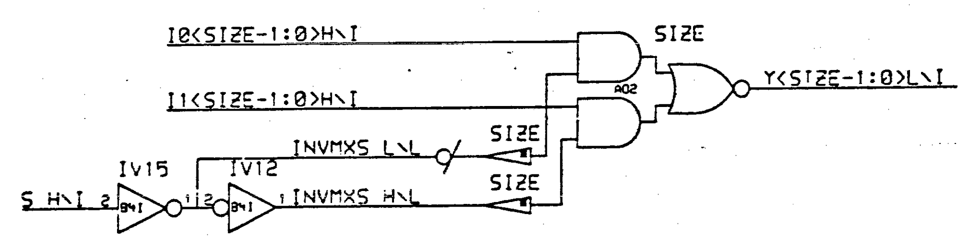
REVISION HISTORY		
REV	ECO NUMBER	DATE
B	MAC-0100	

DRAWING
TITLE=VECTOR HACK
ABBREV=VCTRHCK
LAST←MODIFIED=Wed Oct 10 19:16:55 1984

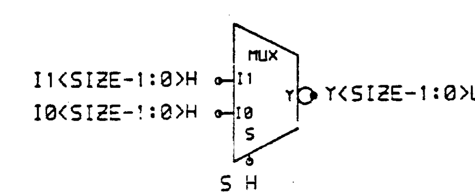
DEFINE
X←FIRST=0
X←STEP=SIZE

digital

DRN: R. McNamara	DATE 9-NOV-83	ENG: R. McNamara	DATE 9-NOV-83	TITLE: Vector Hack	
CHK'D: R. McNamara	DATE 9-NOV-83	SHEET 1 OF 1			
		NEXT HIGHER ASSEMBLY:		SIZE D	CODE 05	NUMBER M7525 -0 -4	REV B



1.4.1.2A



REVISION HISTORY		
REV	ECO NUMBER	DATE
B	M7606M001	

DRAWING
TITLE=INV MUX
ABBREV=INVMX
LAST←MODIFIED=Wed Oct 10 19:20:46 1984

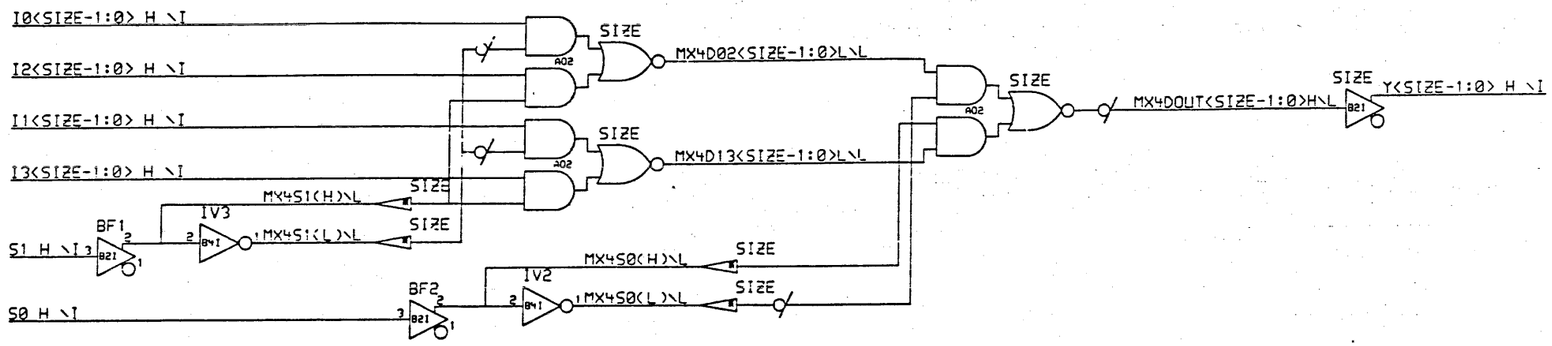
DEFINE
X←FIRST=0
X←STEP=SIZE

digital

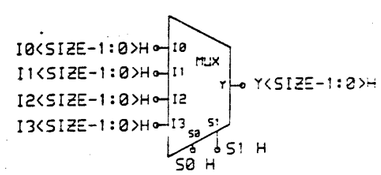
DRN: R. McNamara	DATE 23-Jan-84	ENG: R. McNamara	DATE 23-Jan-84
CHK'D: R. McNamara	DATE 23-Jan-84	SHEET 1 OF 1	
		NEXT HIGHER ASSEMBLY:	

TITLE: Inverting MUX Logic

SIZE	CODE	NUMBER	REV
D	CS	M7606 -0 -15	B



1.4.1.2B

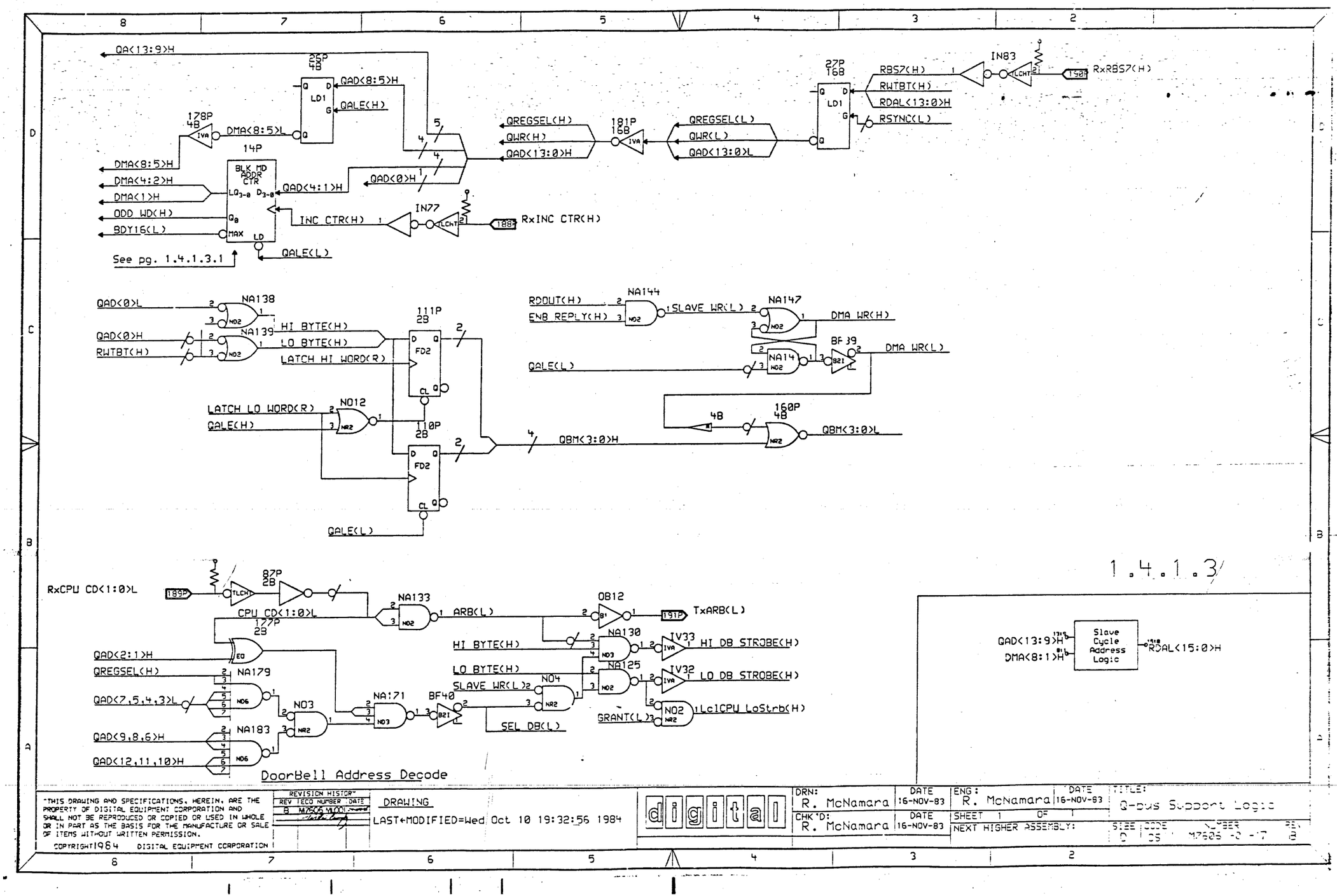


REVISION HISTORY
REV ECO NUMBER DATE
B M76CGM 10-JAN-84

DRAWING
TITLE=4MUX
ABBREV=4MX
LAST←MODIFIED=Wed Oct 10 19:23:47 1984

DEFINE
X←FIRST=0
X←STEP=SIZE

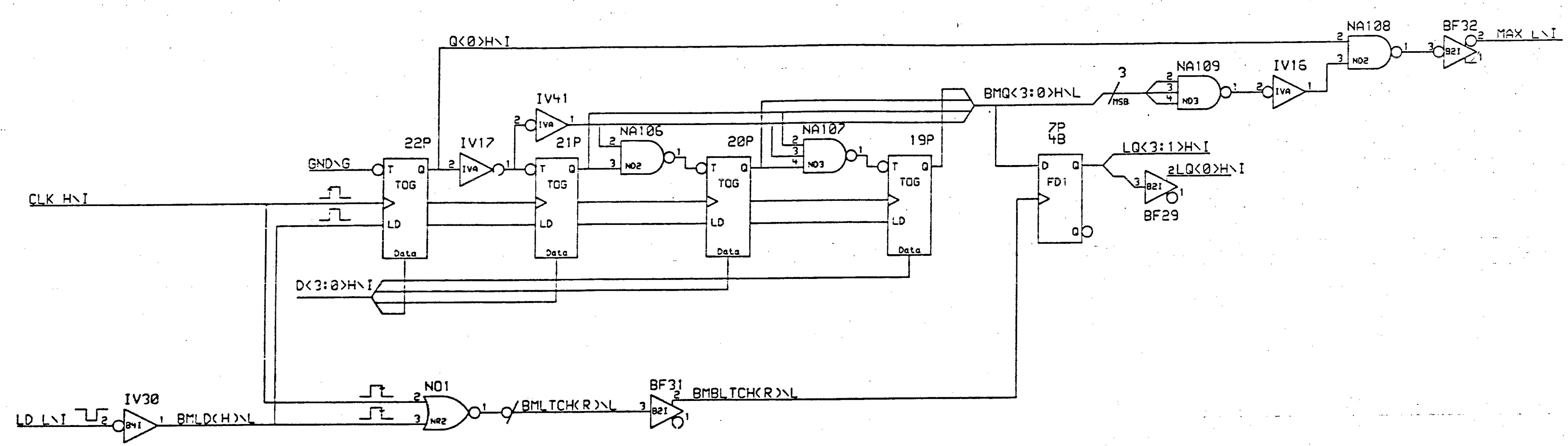
DRN: R. McNamara DATE 10-JAN-84
CHK'D: R. McNamara DATE 10-JAN-84
ENG: R. McNamara DATE 10-JAN-84
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY: —
TITLE: 4 to 1 MUX
SIZE CODE NUMBER REV
D CS M7605-0-16 B



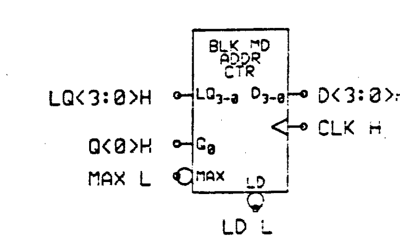
REVISION HISTORY
REV | ECO NUMBER | DATE
B | M7606 MODIFIED

DRAWING
LAST←MODIFIED=Wed Oct 10 19:32:56 1984

DRN: R. McNamara	DATE 16-NOV-83	ENG: R. McNamara	DATE 16-NOV-83	TITLE: Q-bus Support Logic	
CHK'D: R. McNamara	DATE 16-NOV-83	SHEET 1 OF 1			
		NEXT HIGHER ASSEMBLY:		SIZE D	CODE 05	NUMBER M7606 -0 -17	REV B



1.4.1.3.1



REVISION HISTORY		
REV	ECO NUMBER	DATE
B	M7606-M1001	

DRAWING
TITLE=BLK MD CTR
ABBREV=BMCTR
CIRCUIT←TYPE=BLKMDCTR
LAST←MODIFIED=Wed Oct 10 19:28:01 1984

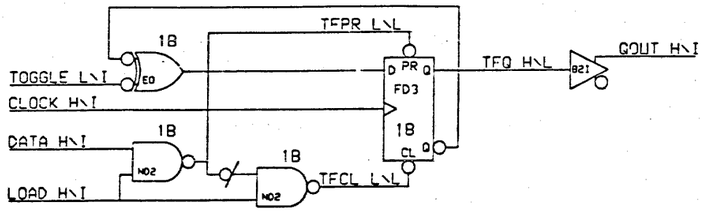
DEFINE
X←FIRST=0
X←STEP=SIZE

digital

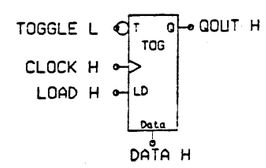
DRN:	DATE	ENG:	DATE
R. McNamara	6-NOV-83	R. McNamara	6-NOV-83
CHK'D: R. McNamara	6-NOV-83	SHEET 1 OF 1	
		NEXT HIGHER ASSEMBLY:	

TITLE: BLK MD CTR LOGIC

SIZE	CODE	NUMBER	REV.
D	CS	M7606-0-8	F



1.4.1.3.1.1



REVISION HISTORY		
REV	ECO NUMBER	DATE
3	M7626-ML001	[illegible]

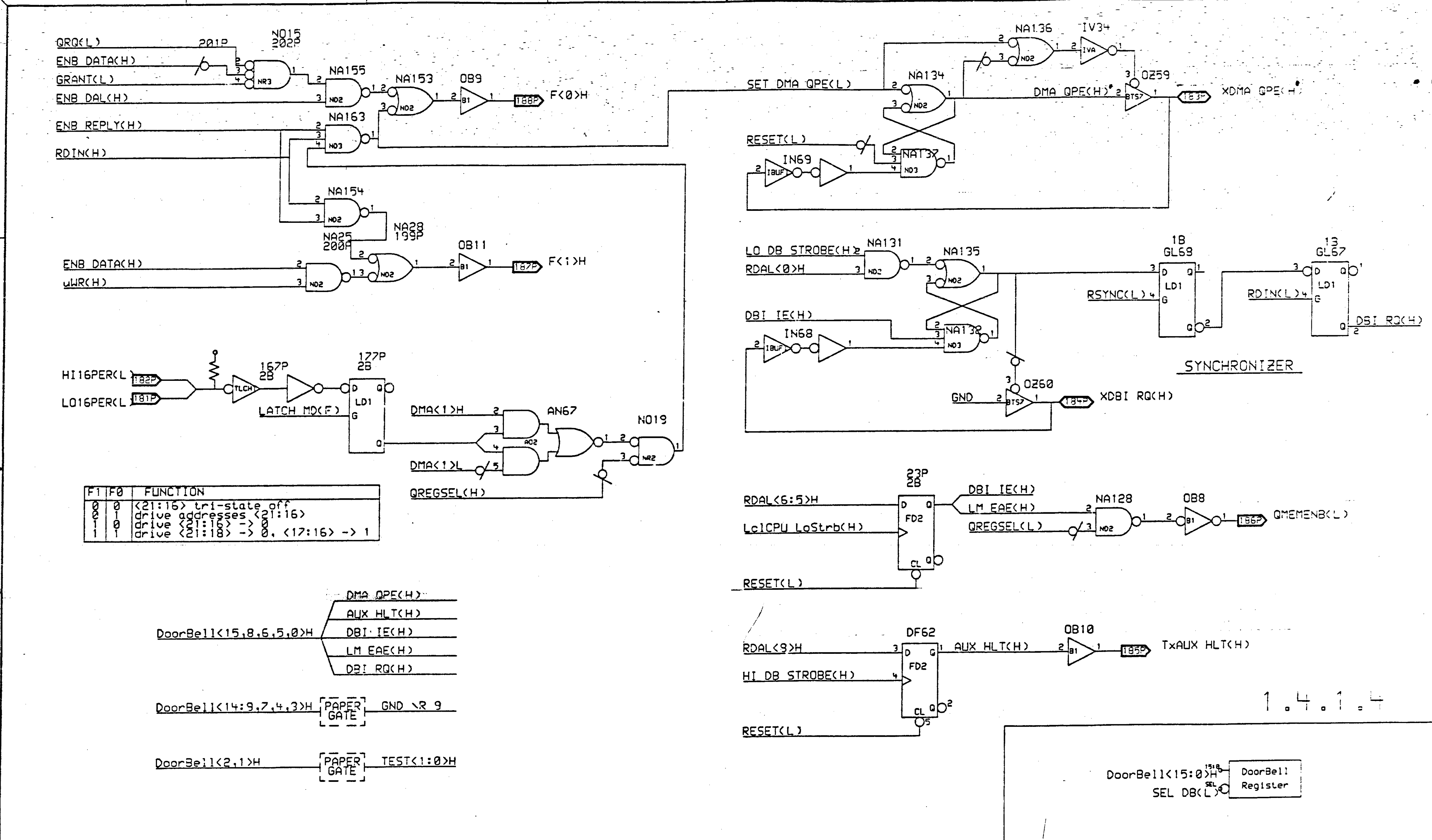
DRAWING
TITLE=TOG
ABBREV=TOG
LAST←MODIFIED=Wed Oct 10 19:57:28 1984

DEFINE
X←FIRST=0
X←STEP=SIZE

digital

DRN:	DATE	ENG:	DATE	TITLE:
R. McNamara	6-NOV-83	R. McNamara	6-NOV-83	TOGGLE FLOP
CHK'D:	DATE	SHEET 1 OF 1		
R. McNamara	6-NOV-83	NEXT HIGHER ASSEMBLY:		

SIZE D | CODE 05 | [illegible] | REV 6


QRQ(L)
ENB DATA(H)
GRANT(L)
ENB DAL(H)
ENB REPLY(H)
RDIN(H)
NA155
NA153
NA163
NA154
0B9
F(0)H
ENB DATA(H)
uWR(H)
0B11
F(1)H
HI16PER(L)
LO16PER(L)
LATCH MD(F)
DMA(1)H
DMA(1)L
QREGSEL(H)
AN67
NO19
DoorBell<15,8,6,5,0>H
DMA QPE(H)
AUX HLT(H)
DBI IE(H)
LM EAE(H)
DBI RQ(H)
DoorBell<14:9,7,4,3>H
PAPER GATE
GND \R 9
DoorBell<2,1>H
TEST<1:0>H
SET DMA QPE(L)
NA136
IV34
NA134
DMA QPE(H)
XDMA QPE(H)
RESET(L)
IN69
NA137
LO DB STROBE(H)
RDAL<0>H
NA131
NA135
DBI IE(H)
IN68
NA132
GL69
GL67
RSYNC(L)
RDIN(L)
DBI RQ(H)
SYNCHRONIZER
GND
0Z60
XDBI RQ(H)
RDAL<6:5>H
LclCPU LoStrb(H)
DBI IE(H)
LM EAE(H)
QREGSEL(L)
NA128
0B8
QMEMENB(L)
RESET(L)
RDAL<9>H
HI DB STROBE(H)
DF62
AUX HLT(H)
0B10
TxAUX HLT(H)
RESET(L)
1.4.1.4
DoorBell<15:0>H
SEL DB(L)
DoorBell Register

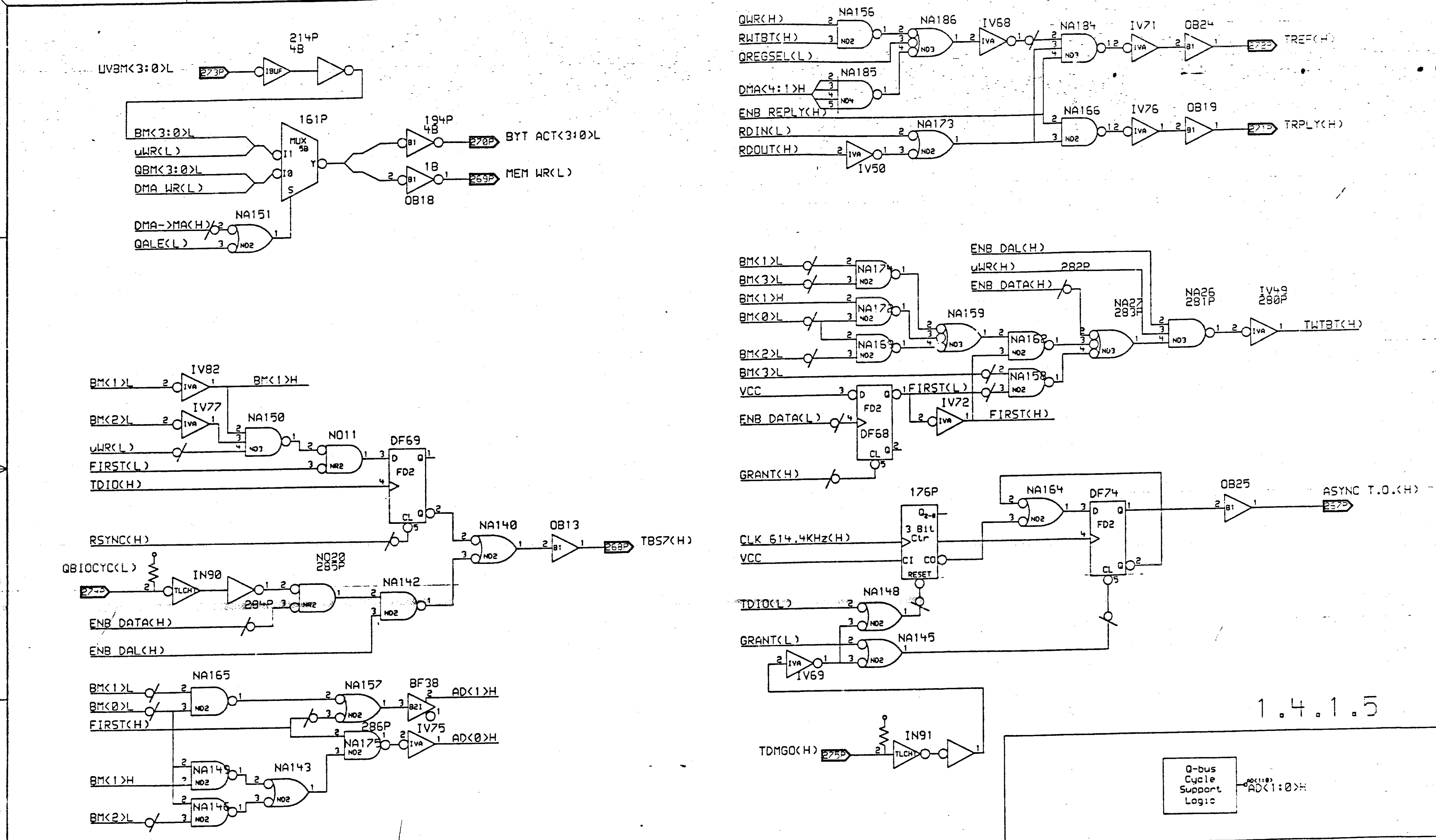
F1	F0	FUNCTION
0	0	<21:16> tri-state off
0	1	drive addresses <21:16>
1	0	drive <21:16> -> 0
1	1	drive <21:18> -> 0, <17:16> -> 1

REVISION HISTORY — REV B, ECO NUMBER M7606-MU001

DRAWING
LAST-MODIFIED=Wed Oct 10 19:36:34 1984

digital

DRN: R. McNamara — DATE 1-NOV-83
CHK'D: R. McNamara — DATE 1-NOV-83
ENG: R. McNamara — DATE 1-NOV-83
SHEET 1 OF
NEXT HIGHER ASSEMBLY:
TITLE: Q-bus Support Logic
SIZE C — CODE DS — NUMBER M7606-0-0-20 — REV A



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REVISION HISTORY

DRAWING

LAST-MODIFIED=Wed Oct 10 19:53:46 1984

digital

DRN: R. McNamara DATE 21-OCT-83

CHK'D: R. McNamara DATE 21-OCT-83

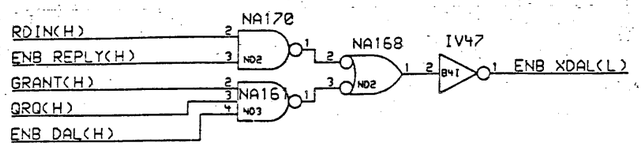
ENG: R. McNamara DATE 21-OCT-83

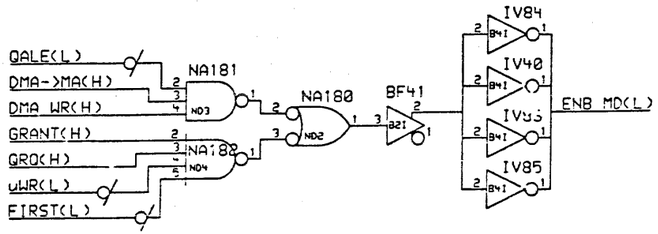
TITLE: Q-bus Support Logic

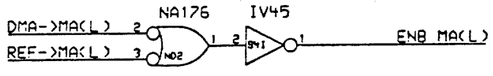
SHEET 1 OF

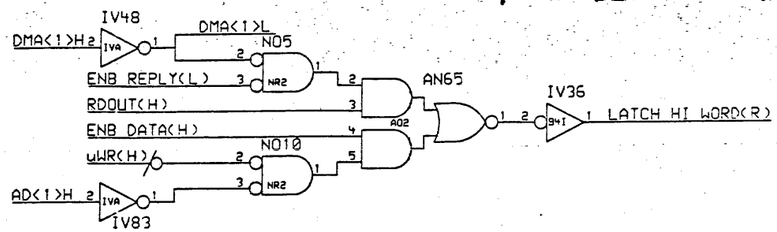
NEXT HIGHER ASSEMBLY:

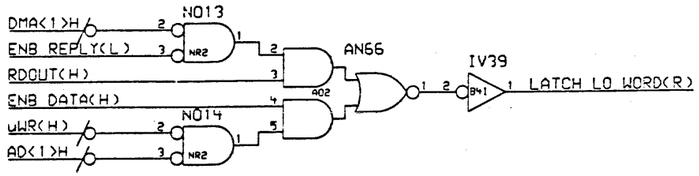
SIZE D -21



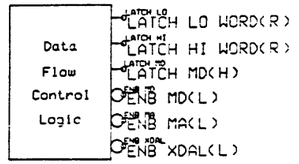








1.4.1.6



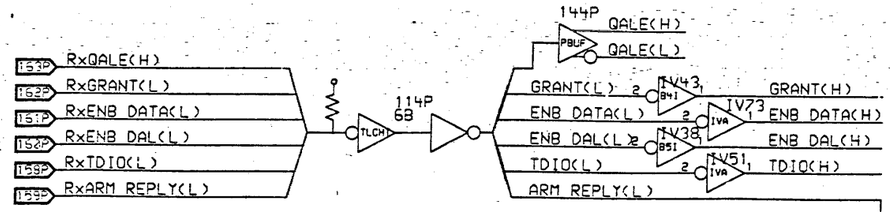
REVISION HISTORY

REV	ECO NUMBER	DATE
B	MODIFIED	

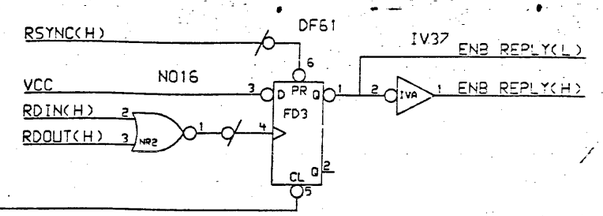
DRAWING

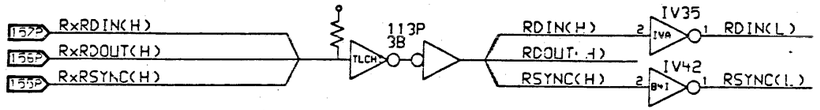
LAST-MODIFIED=Wed Oct 10 19:45:31 1984

DRN: R. McNamara	DATE 09-NOV-83	ENG: R. McNamara	DATE 09-NOV-83	TITLE: Q-Bus Support Logic	
CHK'D: R. McNamara	DATE 09-NOV-83	SHEET 1 OF		SIZE D	CODE 25
		NEXT HIGHER ASSEMBLY:		MODS	

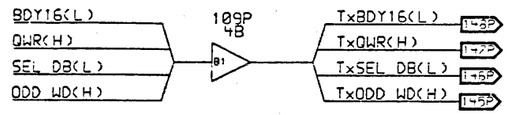


Inputs from Q-bus State Machines

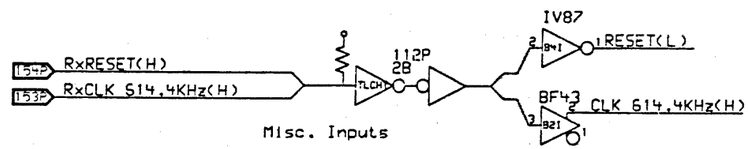




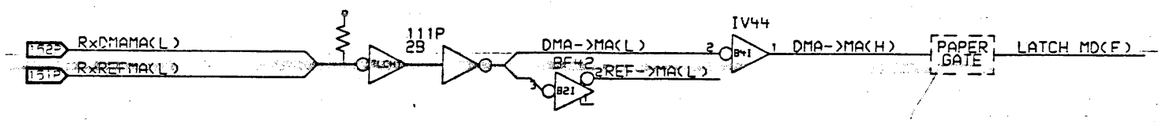
Q-bus Control Signal Inputs



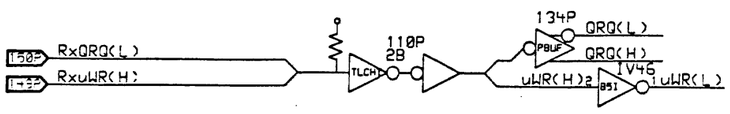
Outputs to Q-bus State Machines



Misc. Inputs

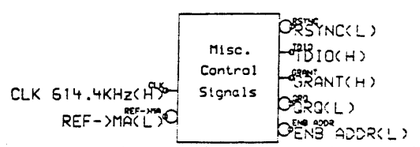


Inputs from Main Memory Controller



Inputs from uVAX cycle machine

1.4.1.7

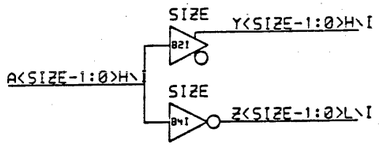


REVISION HISTORY		
REV	ECO NUMBER	DATE
B	MCO-5400	

DRAWING
LAST←MODIFIED=Wed Oct 10 19:49:4' 1984

digital

DRN: R. McNamara	DATE 11-NOV-83	ENG: R. McNamara	DATE 11-NOV-83	TITLE: Q-bus Support Logic	
CHK'D: R. McNamara	DATE 11-NOV-83	SHEET 1 OF 1		SIZE D	CODE 25
		NEXT HIGHER ASSEMBLY:		NUMBER M7620-YD-13	REV B



1.4.1.7.1

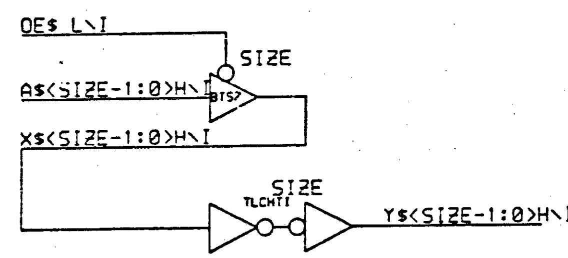
REVISION HISTORY		
REV	ECO NUMBER	DATE
B	WSG100	

DRAWING
TITLE=PBUF
ABBREV=PBUF
LAST←MODIFIED=Wed Oct 10 20:01:17 1984

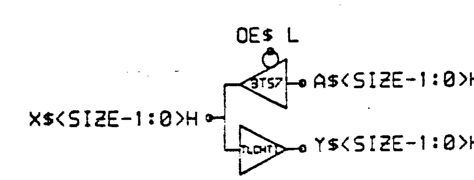
DEFINE
X←FIRST=0
X←STEP=SIZE

digital

DRN: R. McNamara	DATE 11-JAN-84	ENG: R. McNamara	DATE 11-JAN-84	TITLE: Power Buffer Macro	
CHK'D: R. McNamara	DATE 11-JAN-84	SHEET 1 OF 1			
		NEXT HIGHER ASSEMBLY:		SIZE D	CODE CS



1.4.1.8



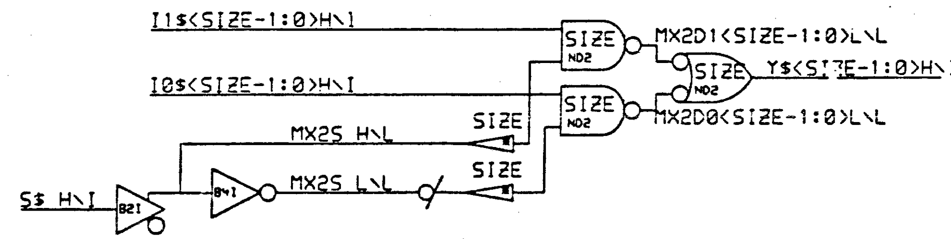
REVISION HISTORY		
REV	ECO NUMBER	DATE
B	M7526M100	

DRAWING
TITLE=BIDIRECT
ABBREV=BI
LAST←MODIFIED=Wed Oct 10 20:05:46 1984

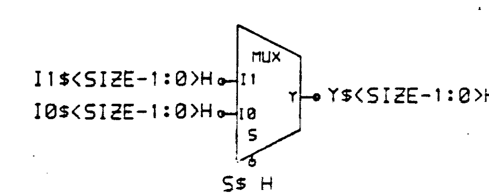
DEFINE
X←FIRST=0
X←STEP=SIZE

digital

DRN: R. McNamara	DATE 11-NOV-83	ENG: R. McNamara	DATE 11-NOV-83	TITLE: BIDIRECT BUFFER
CHK'D: R. McNamara	DATE 11-NOV-83	SHEET OF 1		
		NEXT HIGHER ASSEMBLY:		SIZE D · CODE CS · NUMBER M7526 -0 -25 · REV B



1.4.1.9



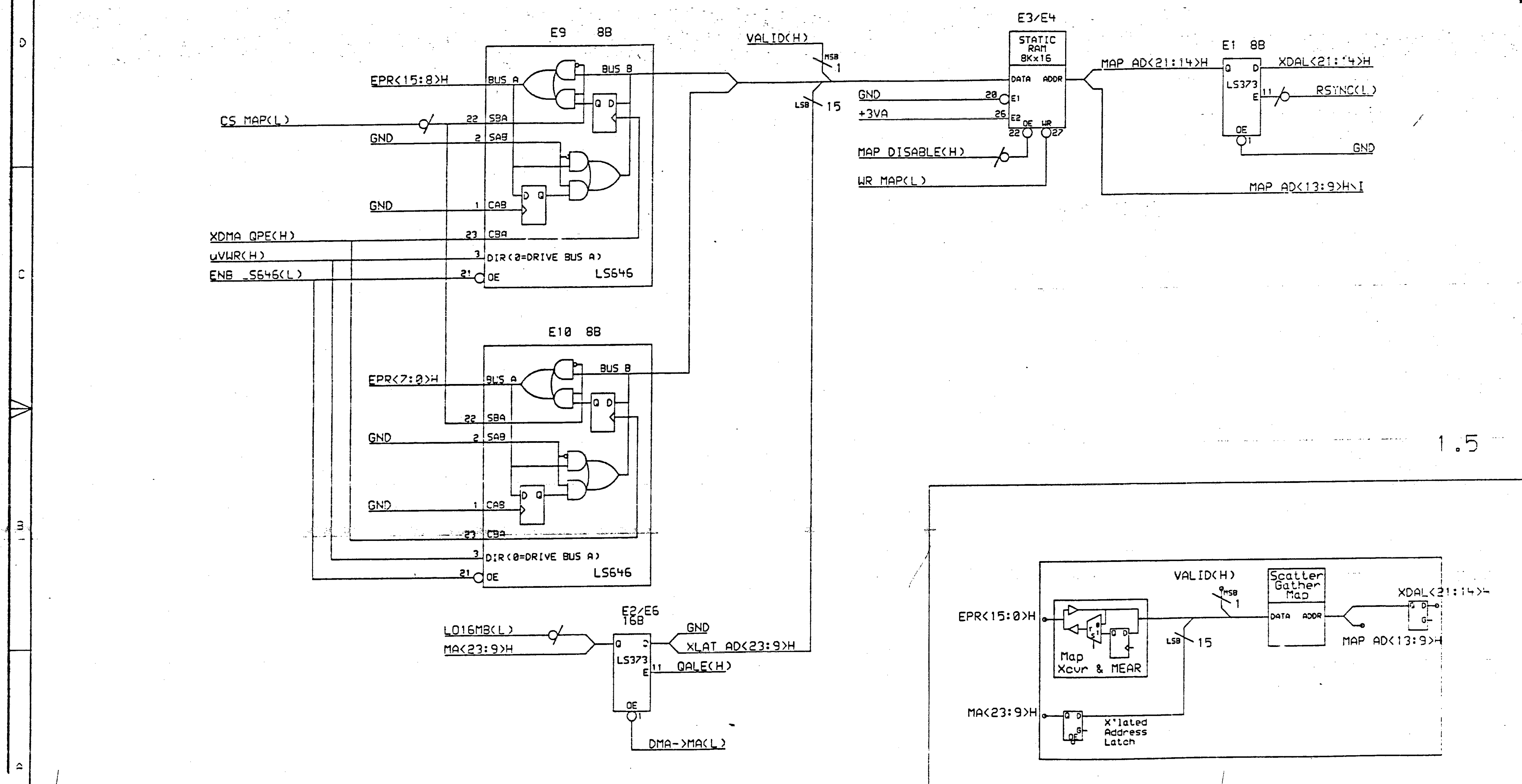
REVISION HISTORY — REV | ECO NUMBER | DATE

DRAWING
TITLE=MUX16
ABBREV=MX16
LAST←MODIFIED=Wed Oct 10 20:09:42 1984

DEFINE
X←FIRST=0
X←STEP=SIZE

digital

DRN: R. McNamara — DATE 8-NOV-83
CHK'D: R. McNamara — DATE 8-NOV-83
ENG: R. McNamara — DATE 8-NOV-83
TITLE: MUX LOGIC
SHEET OF
NEXT HIGHER ASSEMBLY:
SIZE C



REVISION HISTORY: REV | ECO NUMBER | DATE

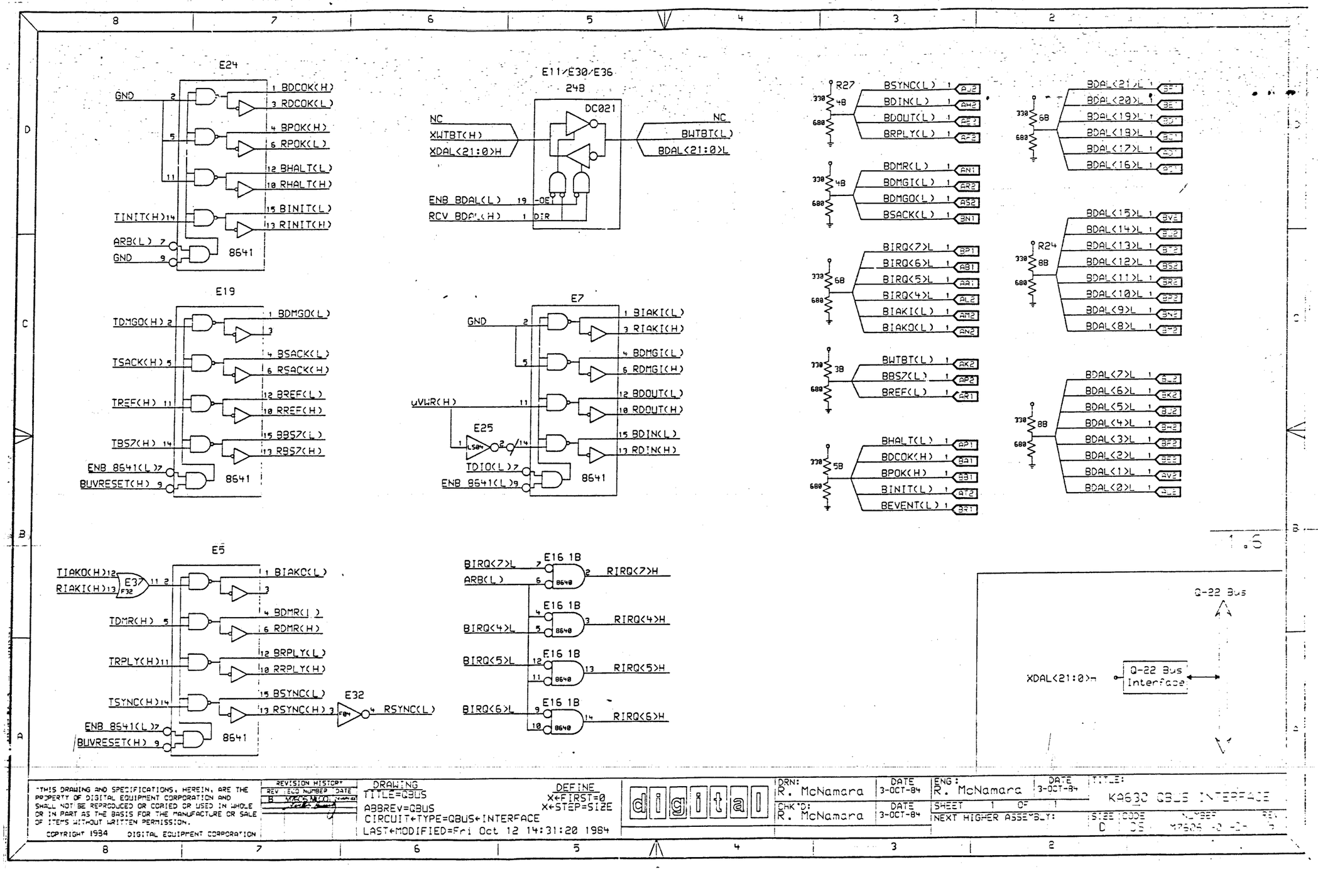
DRAWING
TITLE=MAP GROUP
ABBREV=MAP
CIRCUIT+TYPE=TRANS+MAP
LAST+MODIFIED=Sun Oct 7 18:33:49 1984

DEFINE
X+FIRST=0
X+STEP=SIZE

digital

DRN: R. McNamara — DATE 3-OCT-84
CHK'D: R. McNamara — DATE 3-OCT-84
ENG: R. McNamara — DATE 3-OCT-84
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:

TITLE: Translation Map Group
SIZE: D | CODE: CS | NUMBER: M7606-2-27



1.6

REVISION HISTORY
REV | ECO NUMBER | DATE
B | MSCO-M101 |

DRAWING
TITLE=QBUS
ABBREV=QBUS
CIRCUIT=TYPE=QBUS=INTERFACE
LAST=MODIFIED=Fri Oct 12 14:31:20 1984

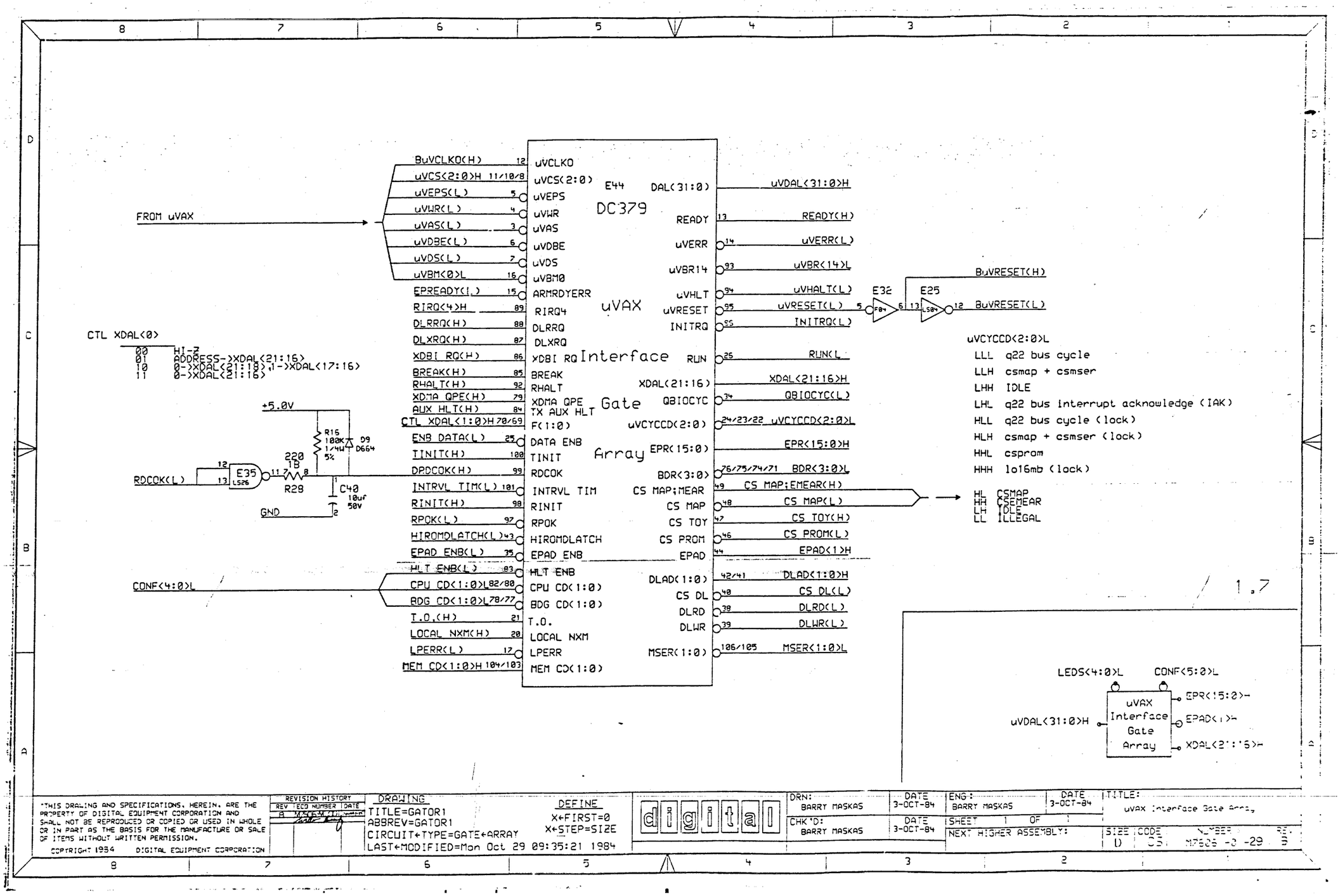
DEFINE
X=FIRST=0
X=STEP=SIZE

digital

DRN: R. McNamara	DATE 3-OCT-84	ENG: R. McNamara	DATE 3-OCT-84
CHK'D: R. McNamara	DATE 3-OCT-84	SHEET 1 OF 1	
		NEXT HIGHER ASSEMBLY:	

TITLE: KA630 QBUS INTERFACE

SIZE	CODE	NUMBER	REV
D	05	M7606-0-01	B

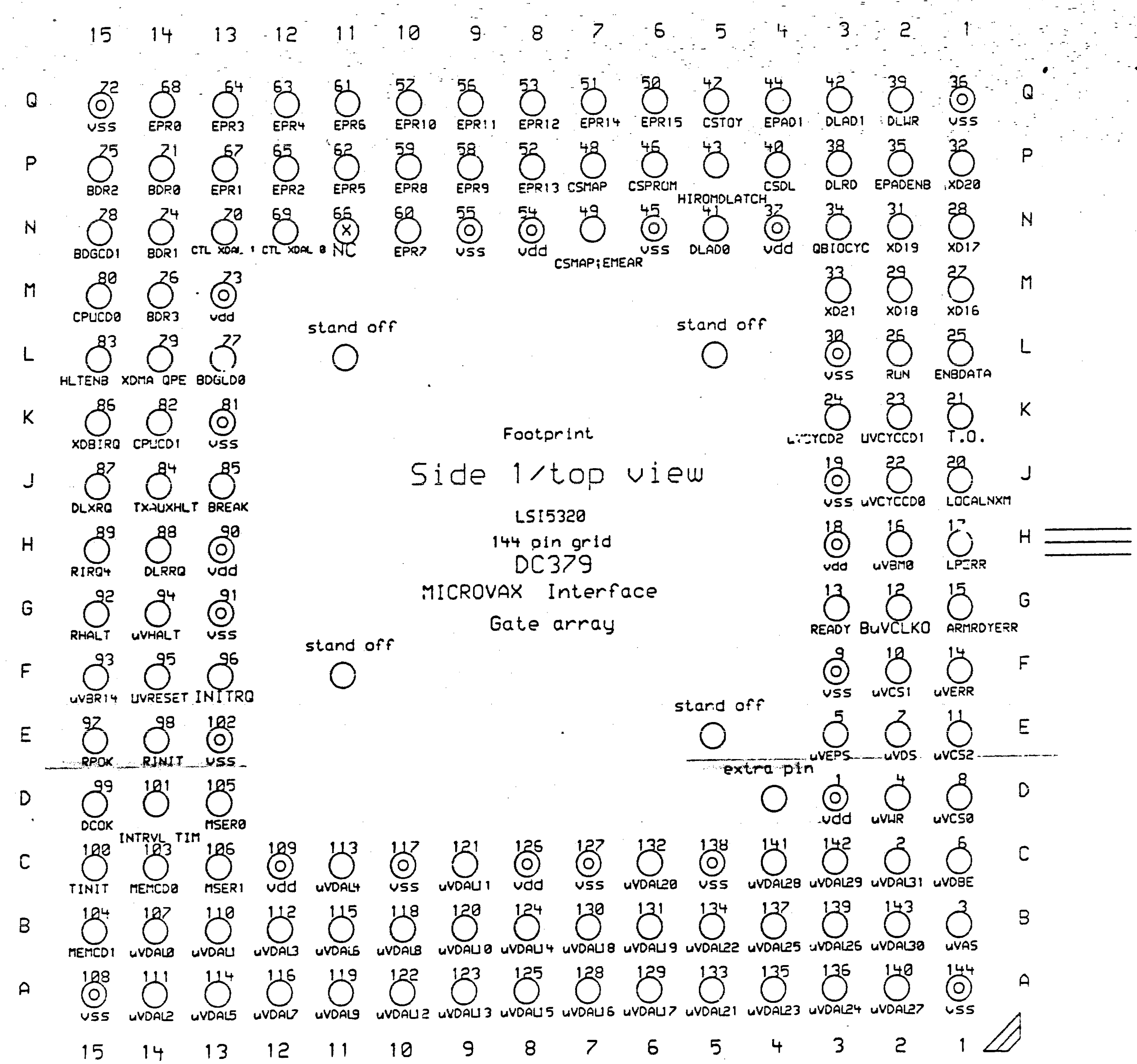


REVISION HISTORY
REV | ECO NUMBER | DATE
B | MSCM-[illegible]

DRAWING
TITLE=GATOR1
ABBREV=GATOR1
CIRCUIT=TYPE=GATE=ARRAY
LAST=MODIFIED=Mon Oct 29 09:35:21 1984

DEFINE
X=FIRST=0
X=STEP=SIZE

DRN: BARRY MASKAS | DATE 3-OCT-84
CHK'D: BARRY MASKAS | DATE 3-OCT-84
ENG: BARRY MASKAS | DATE 3-OCT-84
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:
TITLE: uVAX Interface Gate Array
SIZE D | CODE 03 | NUMBER M7525 -0 -29 | REV B



15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Q: 72 VSS, 68 EPR0, 64 EPR3, 63 EPR4, 61 EPR6, 57 EPR10, 56 EPR11, 53 EPR12, 51 EPR14, 50 EPR15, 47 CSTOY, 44 EPAD1, 42 DLAD1, 39 DLWR, 36 VSS
P: 75 BDR2, 71 BDR0, 67 EPR1, 65 EPR2, 62 EPR5, 59 EPR8, 58 EPR9, 52 EPR13, 48 CSMAP, 46 CSPROM, 43 HIROMDLATCH, 40 CSDL, 38 DLRD, 35 EPADENB, 32 XD20
N: 78 BDGCD1, 74 BDR1, 70 CTL XDAL 1, 69 CTL XDAL 0, 66 NC, 60 EPR7, 55 vss, 54 vdd, 49 CSMAP;EMEAR, 45 vss, 41 DLAD0, 37 vdd, 34 QBIOCYC, 31 XD19, 28 XD17
M: 80 CPUCD0, 76 BDR3, 73 vdd, 33 XD21, 29 XD18, 27 XD16
L: 83 HLTENB, 79 XDMA QPE, 77 BDGLD0, 30 vss, 26 RUN, 25 ENBDATA
K: 86 XDBIRQ, 82 CPUCD1, 81 vss, 24 uVCYCD2, 23 UVCYCCD1, 21 T.O.
J: 87 DLXRQ, 84 TXAUXHLT, 85 BREAK, 19 vss, 22 uVCYCCD0, 20 LOCALNXM
H: 89 RIRQ4, 88 DLRRQ, 90 vdd, 18 vdd, 16 uVBM0, 17 LPERR
G: 92 RHALT, 94 uVHALT, 91 vss, 13 READY, 12 BuVCLKO, 15 ARMRDYERR
F: 93 uVBR14, 95 UVRESET, 96 INITRQ, 9 vss, 10 uVCS1, 14 uVERR
E: 97 RPOK, 98 RINIT, 102 vss, 5 uVEPS, 7 uVDS, 11 uVCS2
D: 99 DCOK, 101 INTRVL TIM, 105 MSER0, 1 vdd, 4 uVWR, 8 uVCS0
C: 100 TINIT, 103 MEMCD0, 106 MSER1, 109 vdd, 113 uVDAL4, 117 vss, 121 uVDAL11, 126 vdd, 127 vss, 132 uVDAL20, 138 vss, 141 uVDAL28, 142 uVDAL29, 2 uVDAL31, 6 uVDBE
B: 104 MEMCD1, 107 uVDAL0, 110 uVDAL1, 112 uVDAL3, 115 uVDAL6, 118 uVDAL8, 120 uVDAL10, 124 uVDAL14, 130 uVDAL18, 131 uVDAL19, 134 uVDAL22, 137 uVDAL25, 139 uVDAL26, 143 uVDAL30, 3 uVAS
A: 108 vss, 111 uVDAL2, 114 uVDAL5, 116 uVDAL7, 119 uVDAL9, 122 uVDAL12, 123 uVDAL13, 125 uVDAL15, 128 uVDAL16, 129 uVDAL17, 133 uVDAL21, 135 uVDAL23, 136 uVDAL24, 140 uVDAL27, 144 vss
stand off
stand off
stand off
stand off
extra pin
Footprint
Side 1/top view
LS15320
144 pin grid
DC379
MICROVAX Interface
Gate array

REVISION HISTORY — REV | ECO NUMBER | DATE

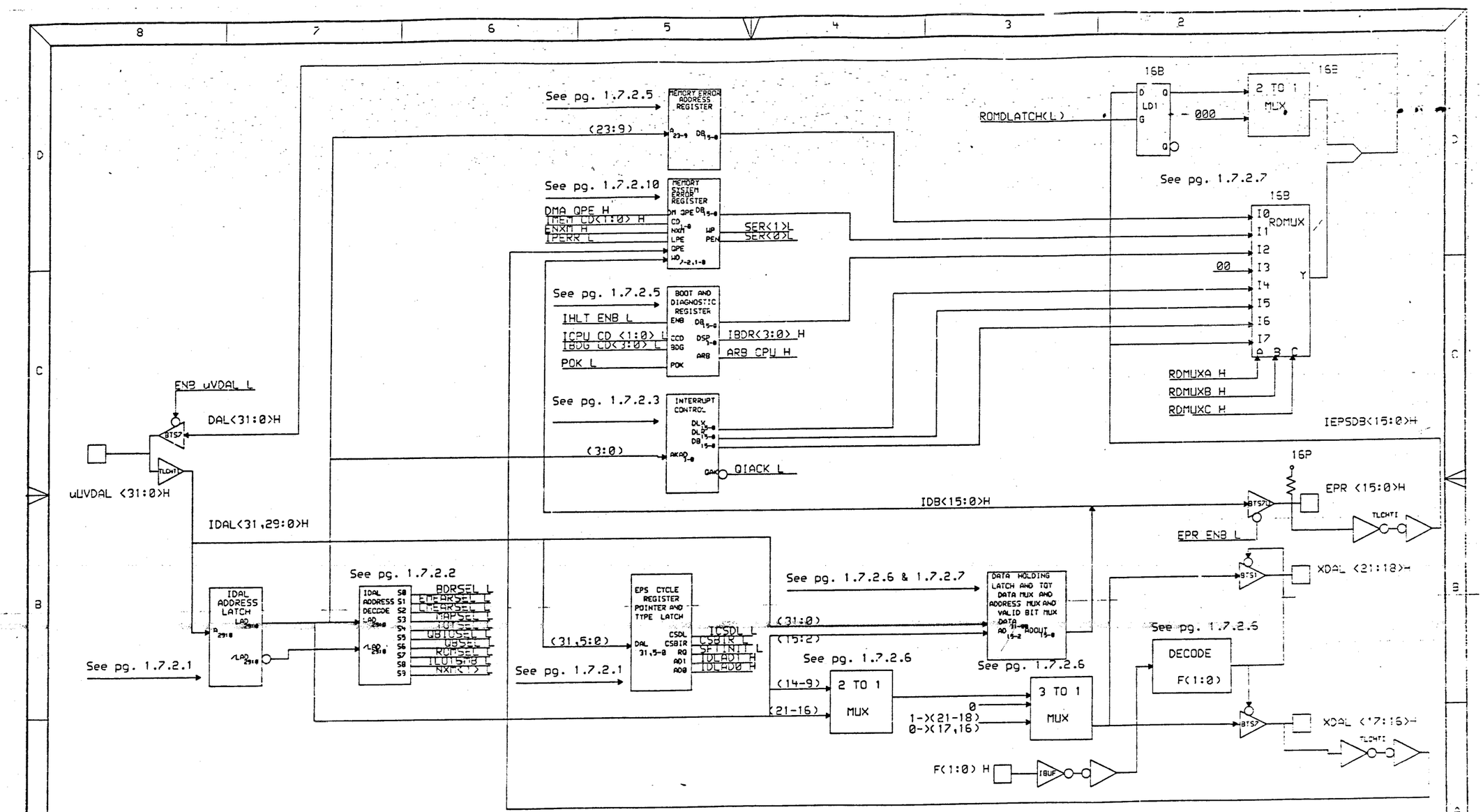
DRAWING
TITLE=galpads
LAST+MODIFIED=Mon Oct 29 11:47:47 1984

DEFINE
X+FIRST=0
X+STEP=SIZE

digital

DRN: BARRY MASKAS — DATE
CHK'D: BARRY MASKAS — DATE
ENG: BARRY MASKAS — DATE 15-DEC-83
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:

TITLE: DC379 PAD ASSIGNMENT TOP VIEW LL5320 IN 144 PIN GRID ARRAY
SIZE D | CODE CS | NUMBER [illegible]-30 | REV A



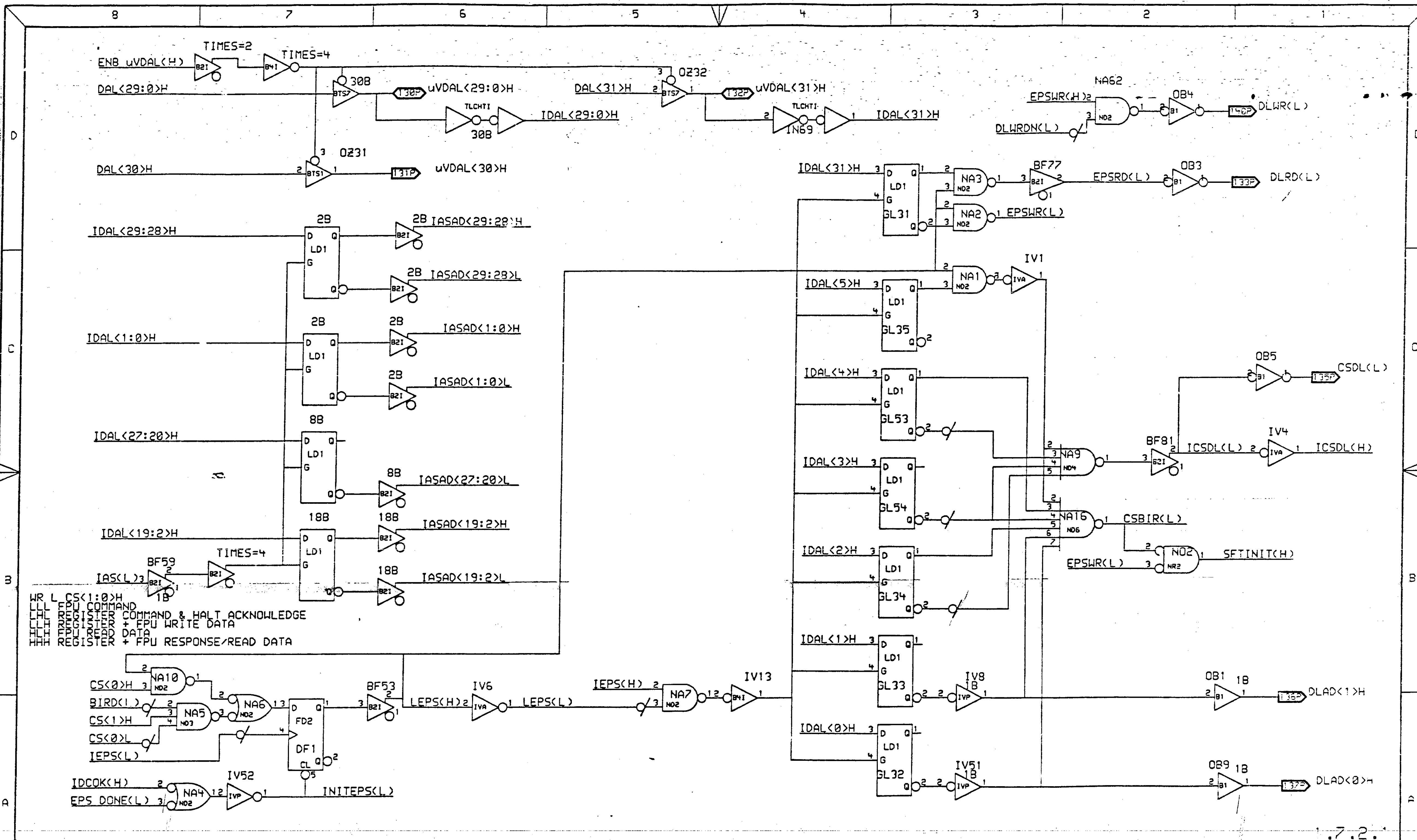
REVISION HISTORY

REV	ECO NUMBER	DATE
H	M7500MOD	[illegible]

DRAWING

TITLE=GA1BLOCK
ABBREV=GA1BLOCK
CIRCUIT-TYPE=GATE-ARRAY
LAST-MODIFIED=Sun Oct 7 20:17:53 1984

DRN: BARRY MASKAS	DATE 15-DEC-83	ENG: BARRY MASKAS	DATE 15-DEC-83	TITLE: uVax Interface Gate Array, Data Path	
CHK'D: BARRY MASKAS	DATE 15-DEC-83	SHEET 1 OF 1			
		NEXT HIGHER ASSEMBLY:		SIZE C	CODE 08



REVISION HISTORY

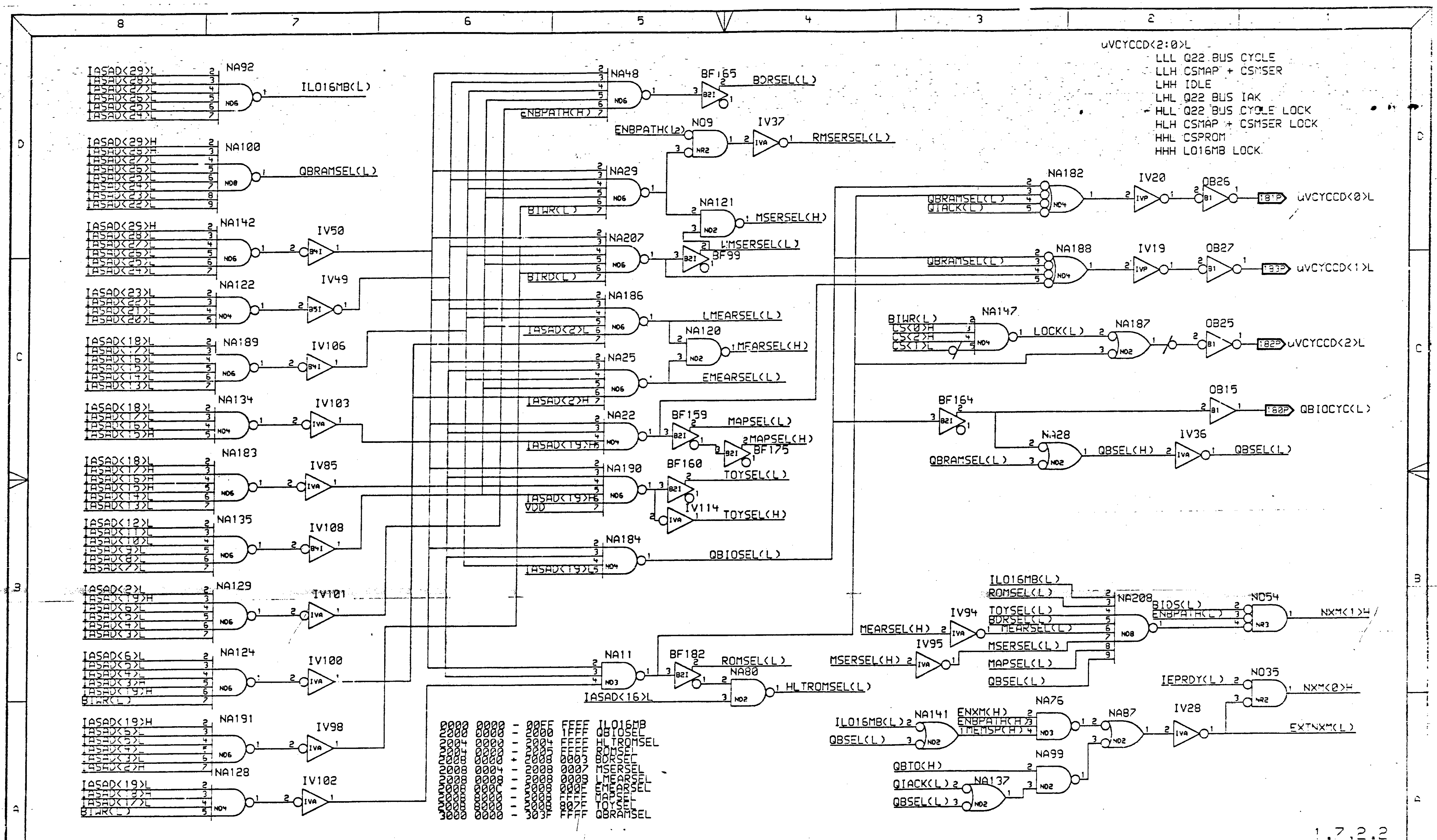
REV	ECO NUMBER	DATE

DRAWING
TITLE=GA1
ABBREV=GA1
CIRCUIT+TYPE=GATE+ARRAY
LAST+MODIFIED=Sun Oct 7 20:20:28 1984

DEFINE
X+FIRST=0
X+STEP=SIZE

digital

DRN: BARRY MASKAS	DATE 19-DEC-83	ENG: BARRY MASKAS	DATE 19-DEC-83	TITLE: uVDAL I/O BUFFERS, ADDR LATCHES
CHK'D: BARRY MASKAS	DATE 19-DEC-83	SHEET 1 OF 1		SIZE D · CODE CS · NUMBER M7626 -0 -2 · REV H
		NEXT HIGHER ASSEMBLY:		

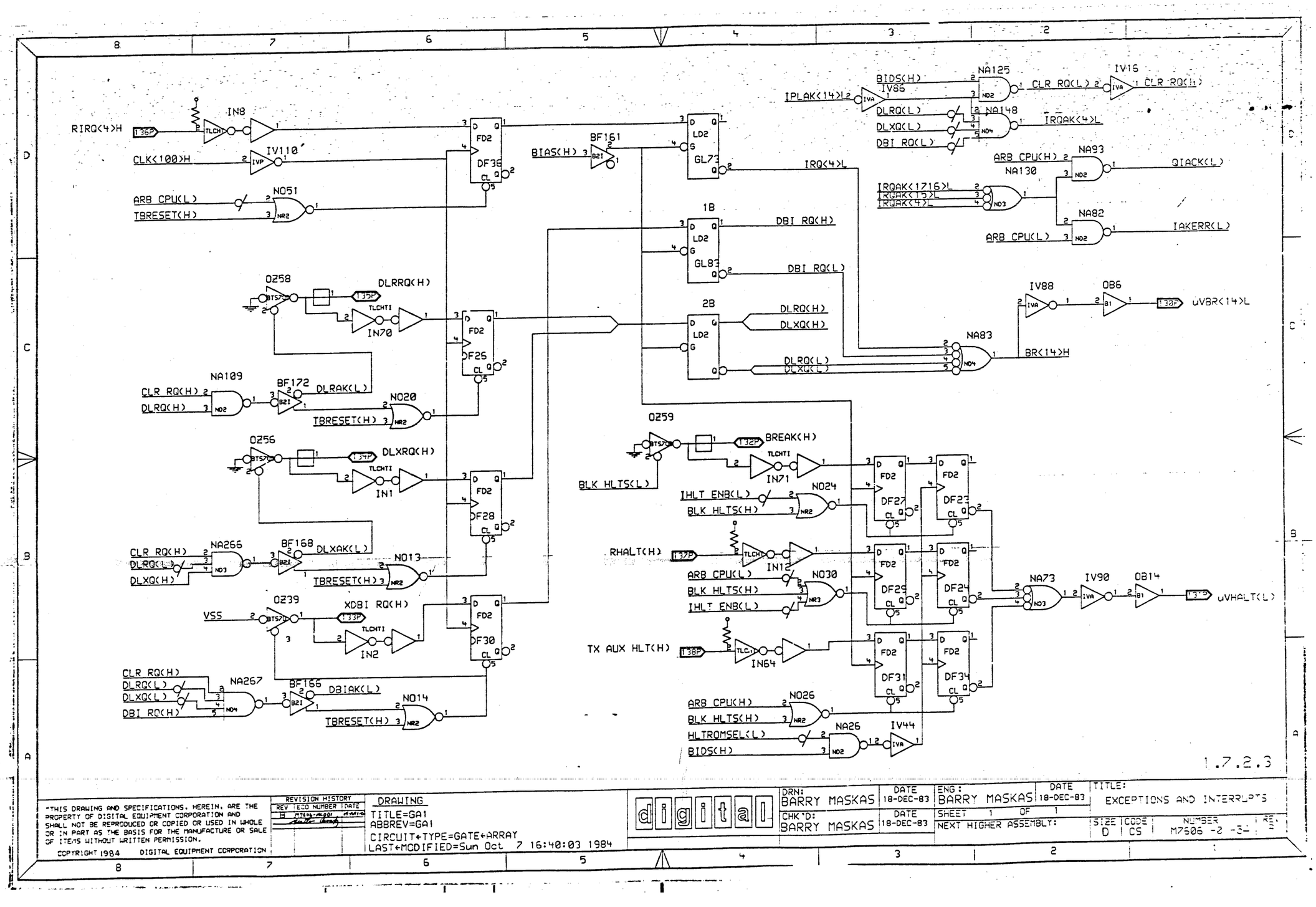


REVISION HISTORY		
REV	ECO NUMBER	DATE
B	M7606-MI00	

DRAWING
TITLE=GA1
ABBREV=GA1
CIRCUIT←TYPE=GATE←ARRAY
LAST←MODIFIED=Sun Oct 7 16:34:28 1984

digital

DRN: BARRY MASKAS	DATE 19-DEC-83	ENG: BARRY MASKAS	DATE 19-DEC-83	TITLE: ADDRESS DECODER
CHK'D: BARRY MASKAS	DATE 19-DEC-83	SHEET 1 OF 1	NEXT HIGHER ASSEMBLY:	SIZE D, CODE CS, NUMBER M7606-0-F3, REV

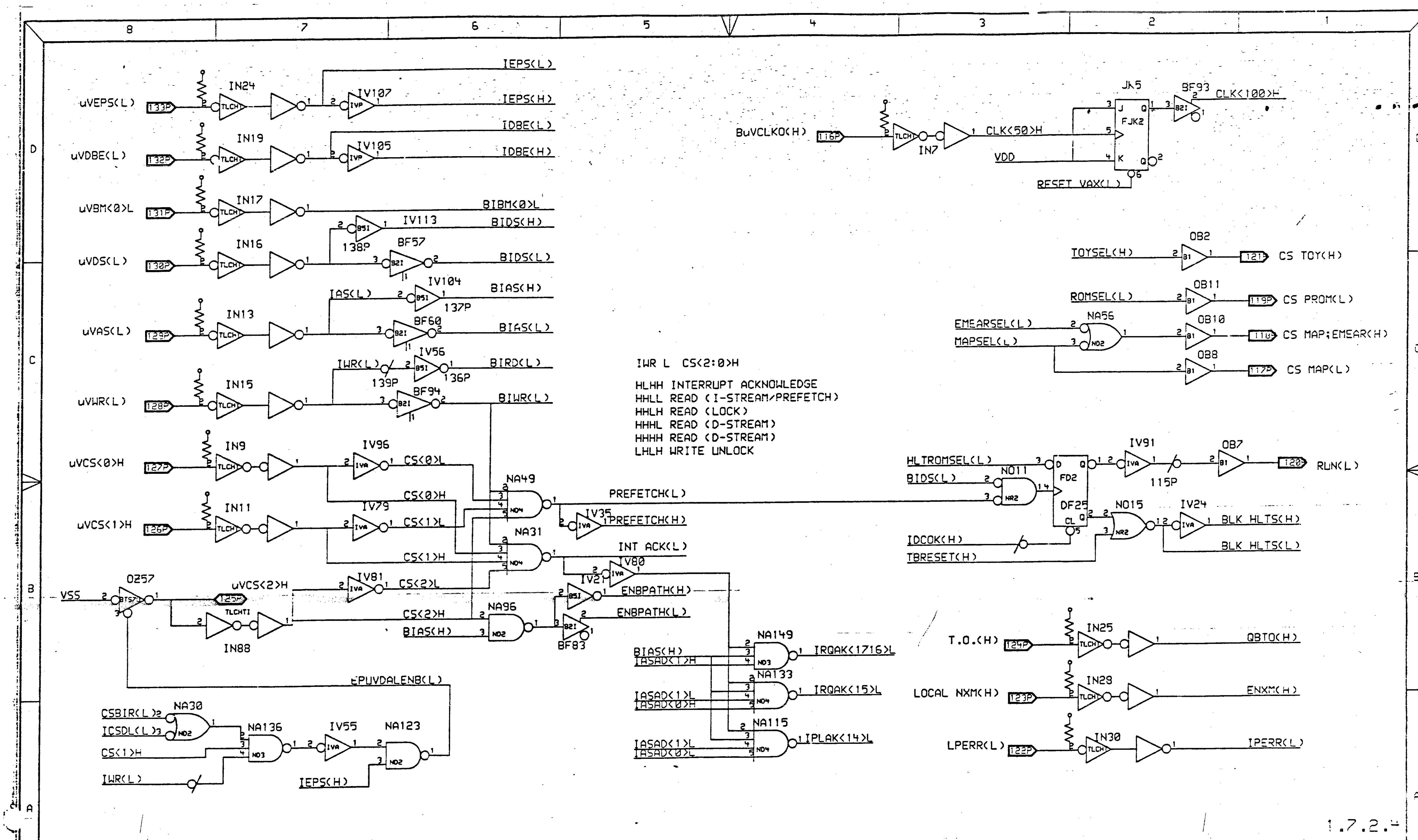


REVISION HISTORY		
REV	ECO NUMBER	DATE
B	M7506-00001	19-MAY-84

DRAWING
TITLE=GA1
ABBREV=GA1
CIRCUIT=TYPE=GATE=ARRAY
LAST=MODIFIED=Sun Oct 7 16:40:03 1984

digital

DRN: BARRY MASKAS	DATE 18-DEC-83	ENG: BARRY MASKAS	DATE 18-DEC-83	TITLE: EXCEPTIONS AND INTERRUPTS	
CHK'D: BARRY MASKAS	DATE 18-DEC-83	SHEET 1 OF 1			
		NEXT HIGHER ASSEMBLY:		SIZE D / CODE CS / NUMBER M7506 -2 -3-	REV



REVISION HISTORY
REV | ECO NUMBER | DATE

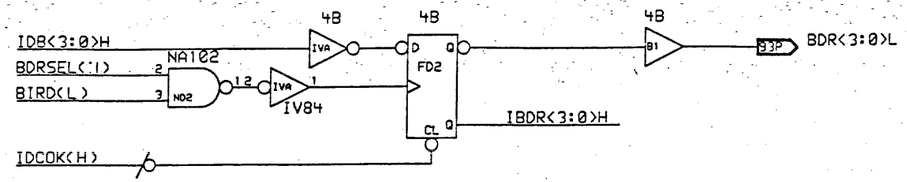
DRAWING
TITLE=GA1
ABBREV=GA1
CIRCUIT+TYPE=GATE+ARRAY
LAST+MODIFIED=Sat Oct 20 18:44:09 1984

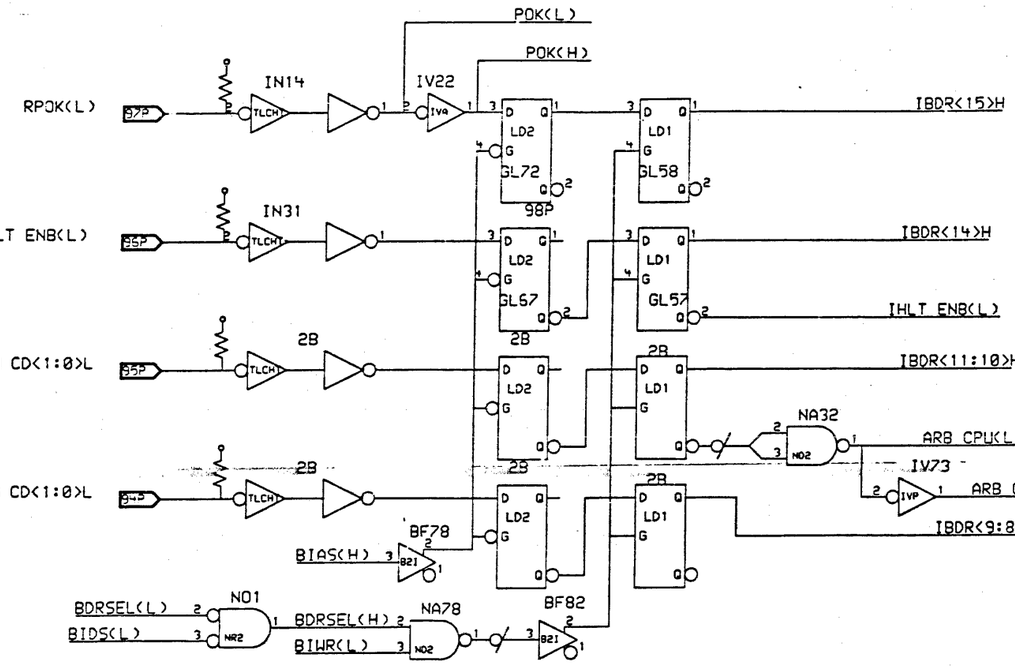
digital

DRN: BARRY MASKAS DATE 19-DEC-83
CHK'D: BARRY MASKAS DATE 19-DEC-83
ENG: BARRY MASKAS DATE 19-DEC-83
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:

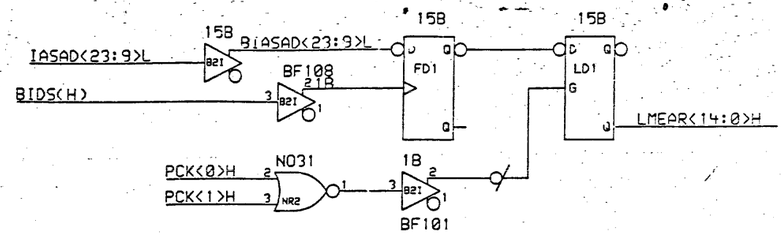
TITLE: uVAX INPUTS AND I/O PINS
SIZE D | CODE CS | NUMBER M7606 -0 -35 | REV 3

BOOT AND DIAGNOSTIC REGISTER





MEMORY ERROR ADDRESS REGISTER



1.7.2.5

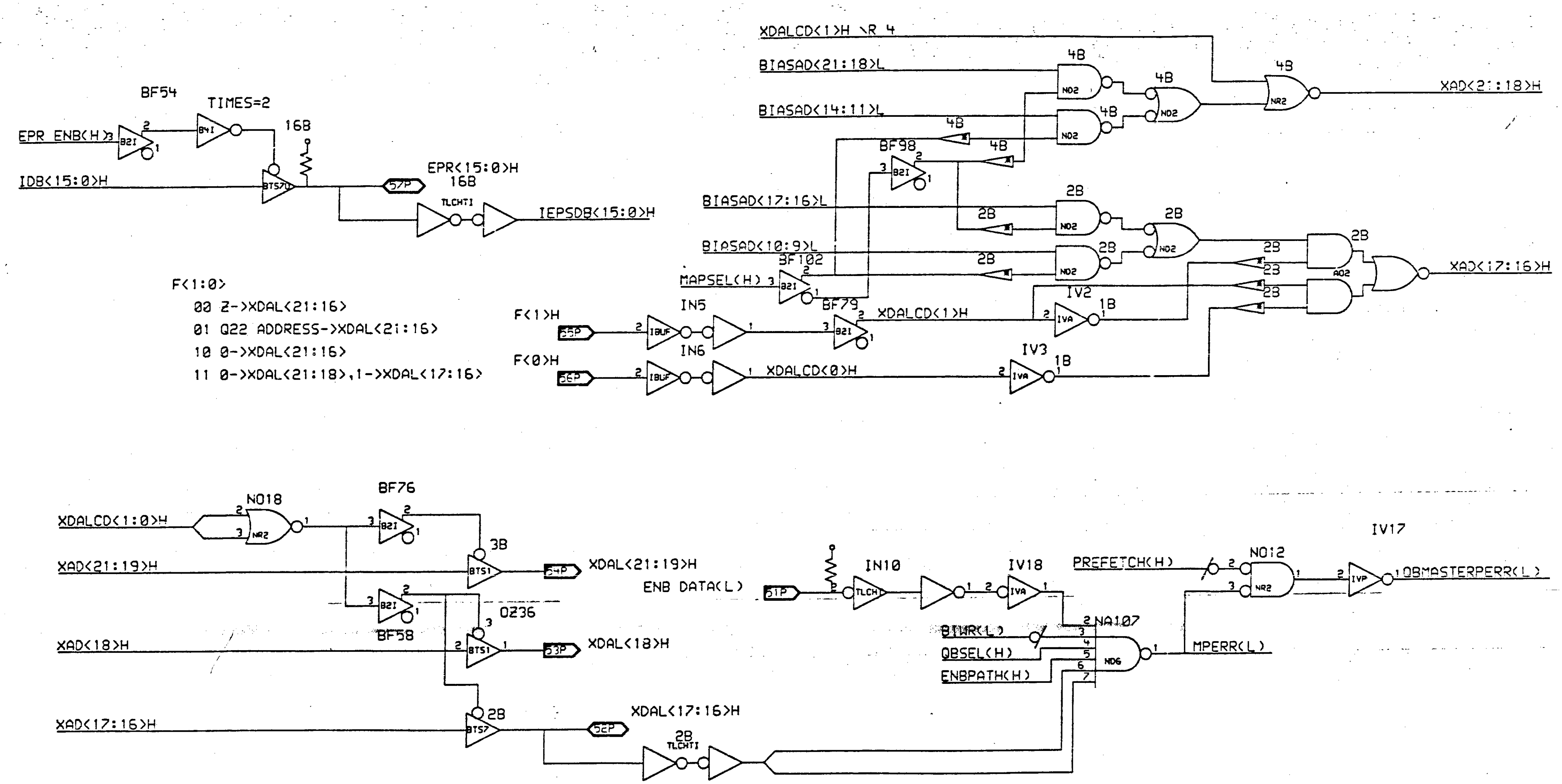
REVISION HISTORY

REV	ECO NUMBER	DATE
A		

DRAWING
TITLE=GA1
ABBREV=GA1
CIRCUIT←TYPE=GATE←ARRAY
LAST←MODIFIED=Sun Oct 7 16:53:31 1984

digital

DRN: BARRY MASKAS	DATE 18-DEC-83	ENG: BARRY MASKAS	DATE 18-DEC-83	TITLE: BOOT/DIAG REG., MEM ERR ADDR REG.	
CHK'D: BARRY MASKAS	DATE 18-DEC-83	SHEET 1 OF 1			
		NEXT HIGHER ASSEMBLY:		SIZE D / CODE CS / NUMBER M7606 -0 -36	REV A



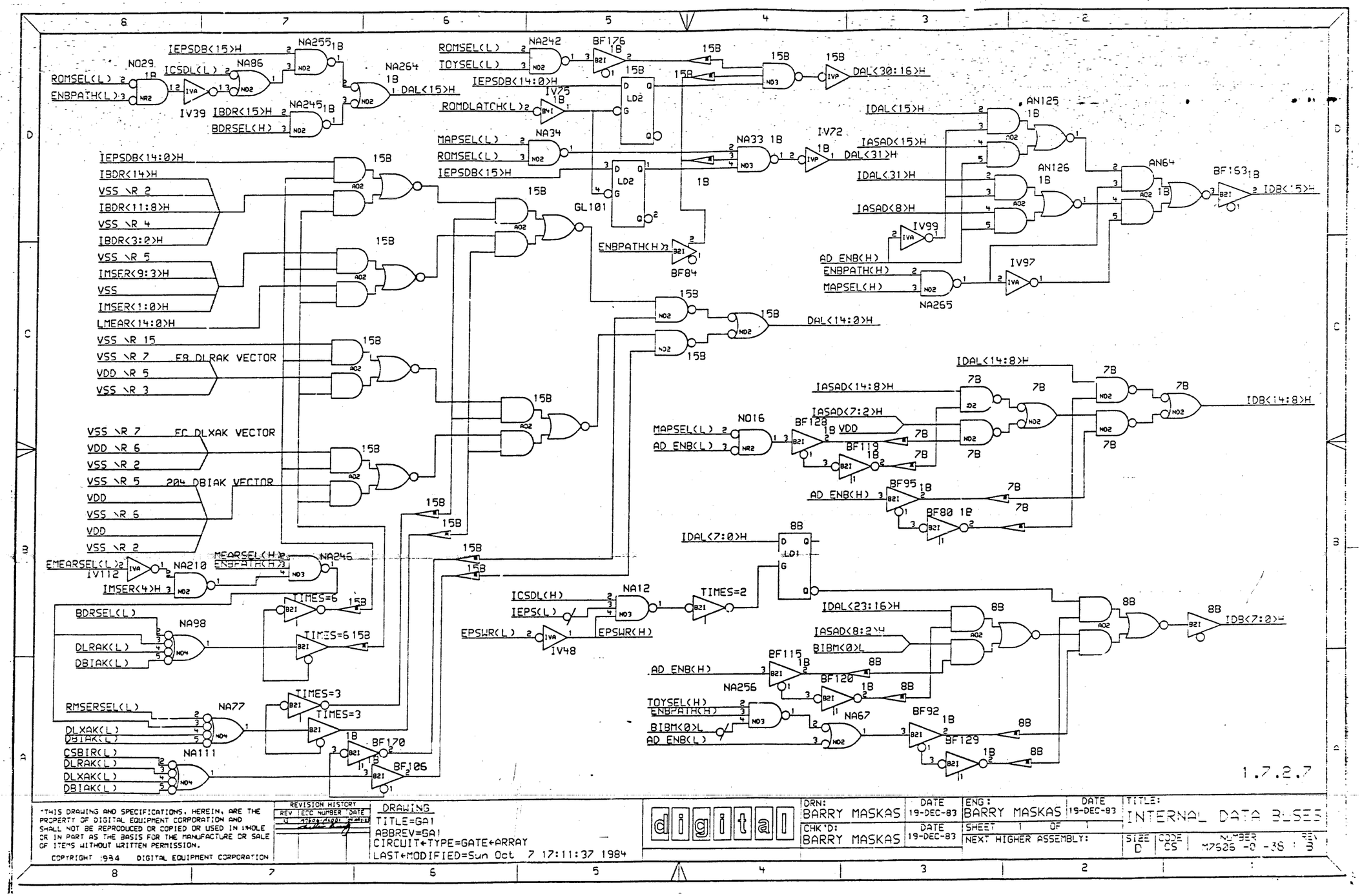
1.7.2.5

REVISION HISTORY
REV | ECO NUMBER | DATE

DRAWING
TITLE=GA1
ABBREV=GA1
CIRCUIT←TYPE=GATE←ARRAY
LAST←MODIFIED=NOT WRITTEN

digital

DRN: BARRY MASKAS	DATE 19-DEC-83	ENG: BARRY MASKAS	DATE 19-DEC-83	TITLE: EPR BUS,XDAL BUS
CHK'D: BARRY MASKAS	DATE 19-DEC-83	SHEET 1 OF 1		
		NEXT HIGHER ASSEMBLY:		SIZE D · CODE CS · NUMBER M7606-0-37 · REV 3



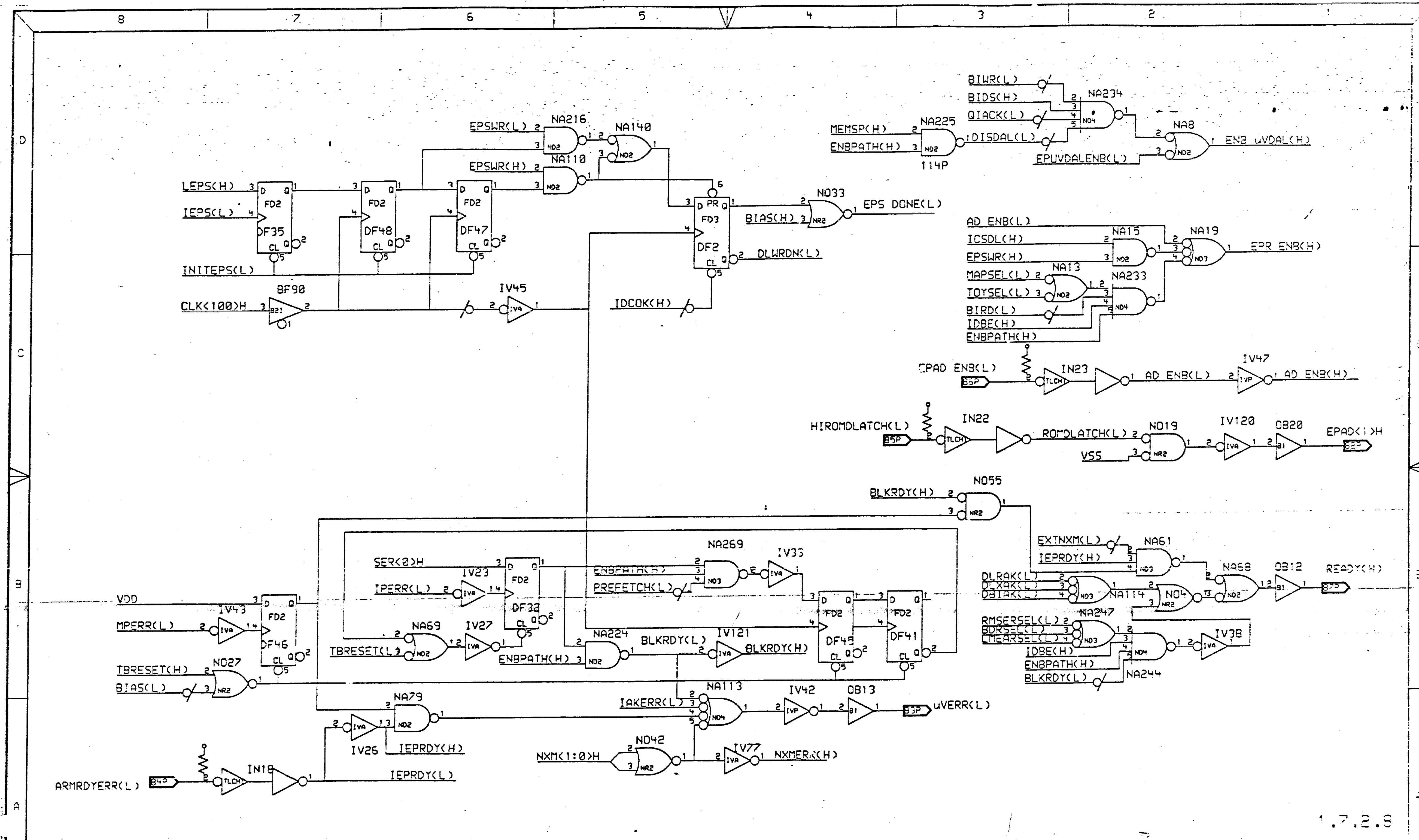
REVISION HISTORY

REV	ECO NUMBER	DATE

DRAWING
TITLE=GA1
ABBREV=GA1
CIRCUIT-TYPE=GATE-ARRAY
LAST-MODIFIED=Sun Oct 7 17:11:37 1984

digital

DRN: BARRY MASKAS	DATE 19-DEC-83	ENG: BARRY MASKAS	DATE 19-DEC-83	TITLE: INTERNAL DATA BUSES	
CHK'D: BARRY MASKAS	DATE 19-DEC-83	SHEET 1 OF 1			
		NEXT HIGHER ASSEMBLY:		SIZE D / CODE CS / NUMBER M7525-0-38 / REV B	



REVISION HISTORY

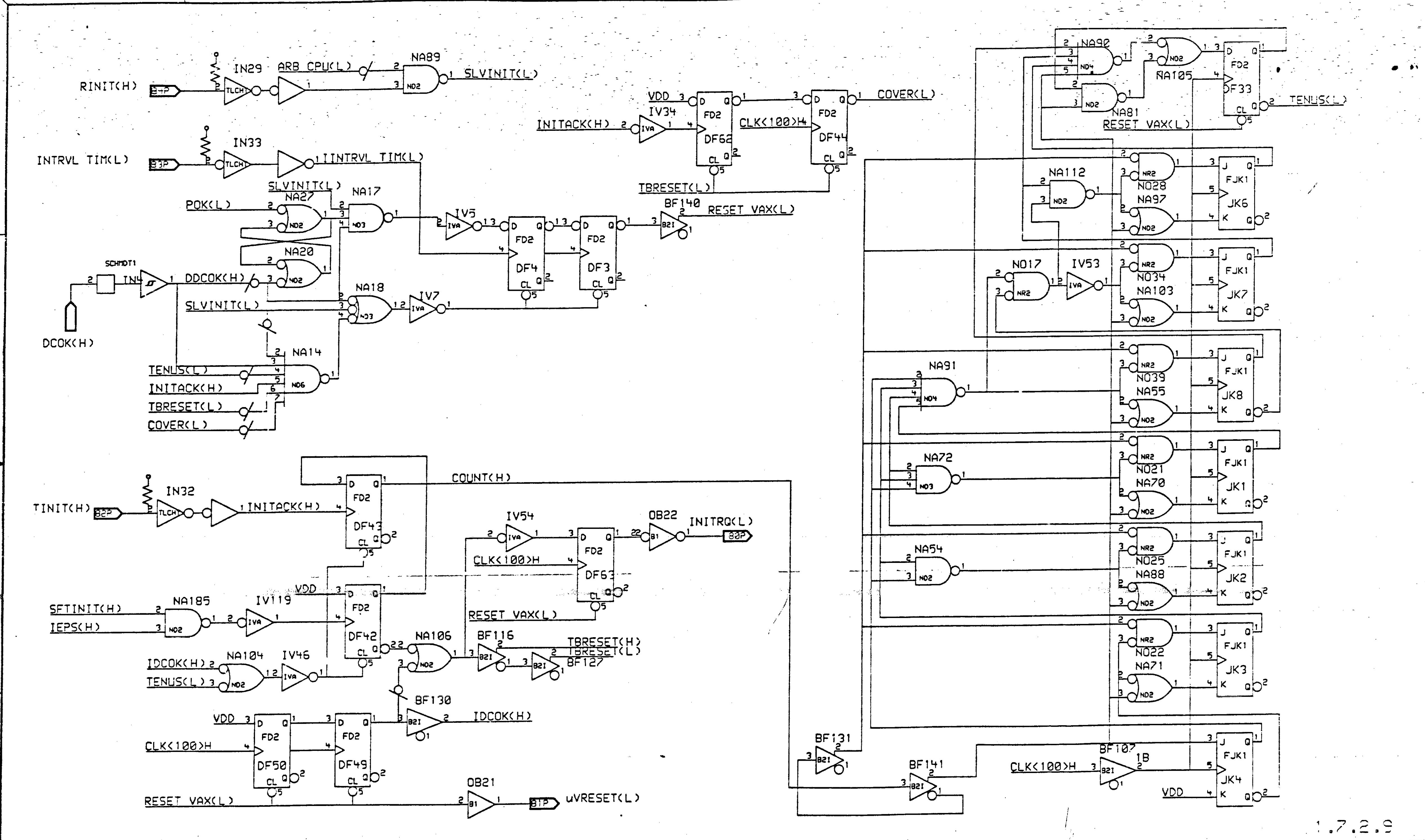
REV	ECO NUMBER	DATE

DRAWING

TITLE=GA1
ABBREV=GA1
CIRCUIT+TYPE=GATE+ARRAY
LAST+MODIFIED=Sun Oct 7 17:15:18 1984

digital

DRN: BARRY MASKAS	DATE 19-DEC-83	ENG: BARRY MASKAS	DATE 19-DEC-83	TITLE: MISC. CONTROL STROBES
CHK'D: BARRY MASKAS	DATE 19-DEC-83	SHEET OF		SIZE D, CODE CS, NUMBER M7606-?-?9, REV 6
		NEXT HIGHER ASSEMBLY:		



1.7.2.9

REVISION HISTORY
REV | ECO NUMBER | DATE

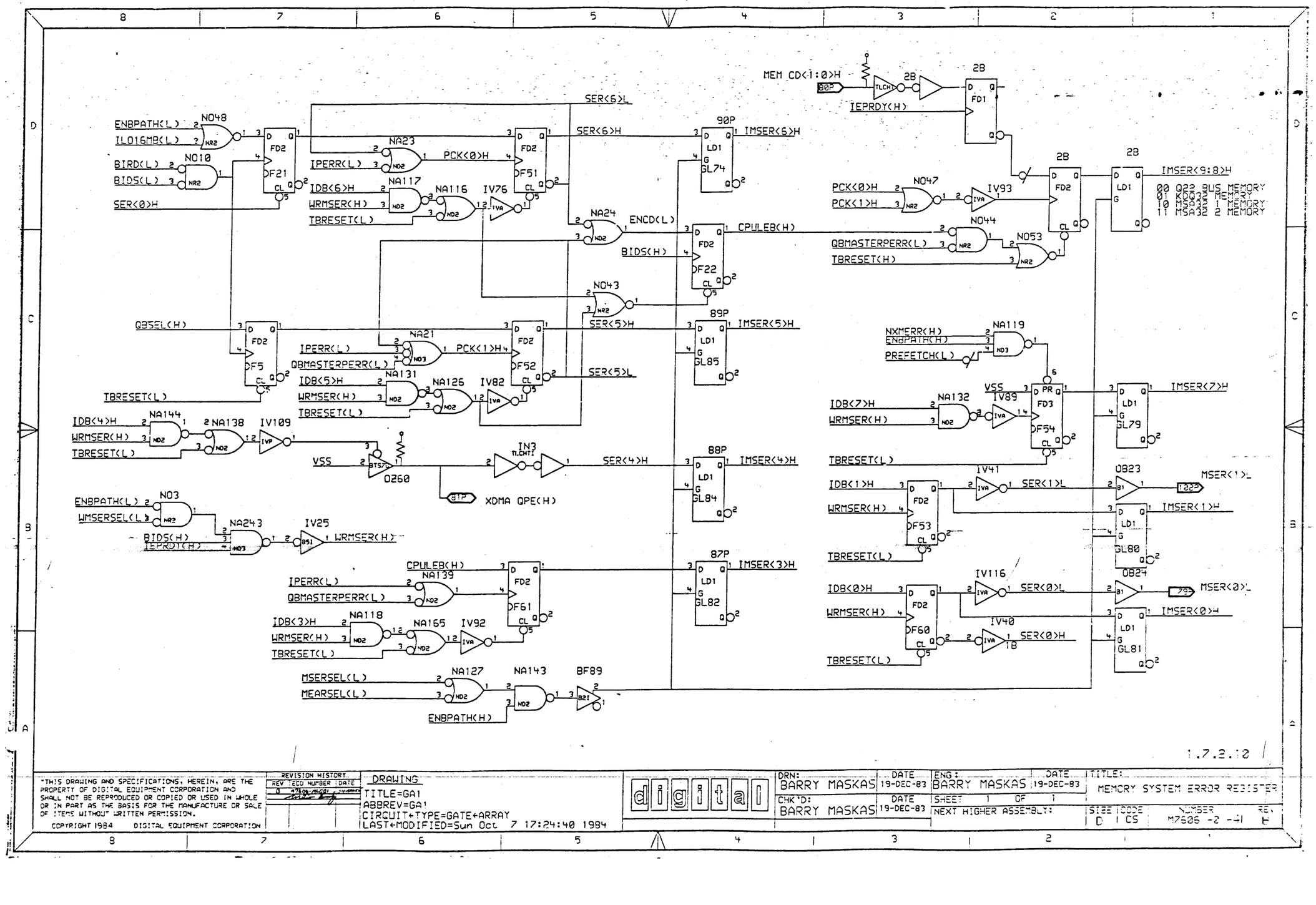
DRAWING
TITLE=GA1
ABBREV=GA1
CIRCUIT+TYPE=GATE+ARRAY
LAST+MODIFIED=Sun Oct 7 17:19:49 1984

digital

DRN: BARRY MASKAS	DATE 19-DEC-83	ENG: BARRY MASKAS	DATE 19-DEC-83
CHK'D: BARRY MASKAS	DATE 19-DEC-83	SHEET 1 OF 1	NEXT HIGHER ASSEMBLY:-

TITLE: RESET COUNTER, POWER UP/DOWN CNTRL

SIZE D | CODE CS | NUMBER M7626 -0 -40 | REV. B



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REVISION HISTORY

REV	ECO NUMBER	DATE
A	[illegible]	

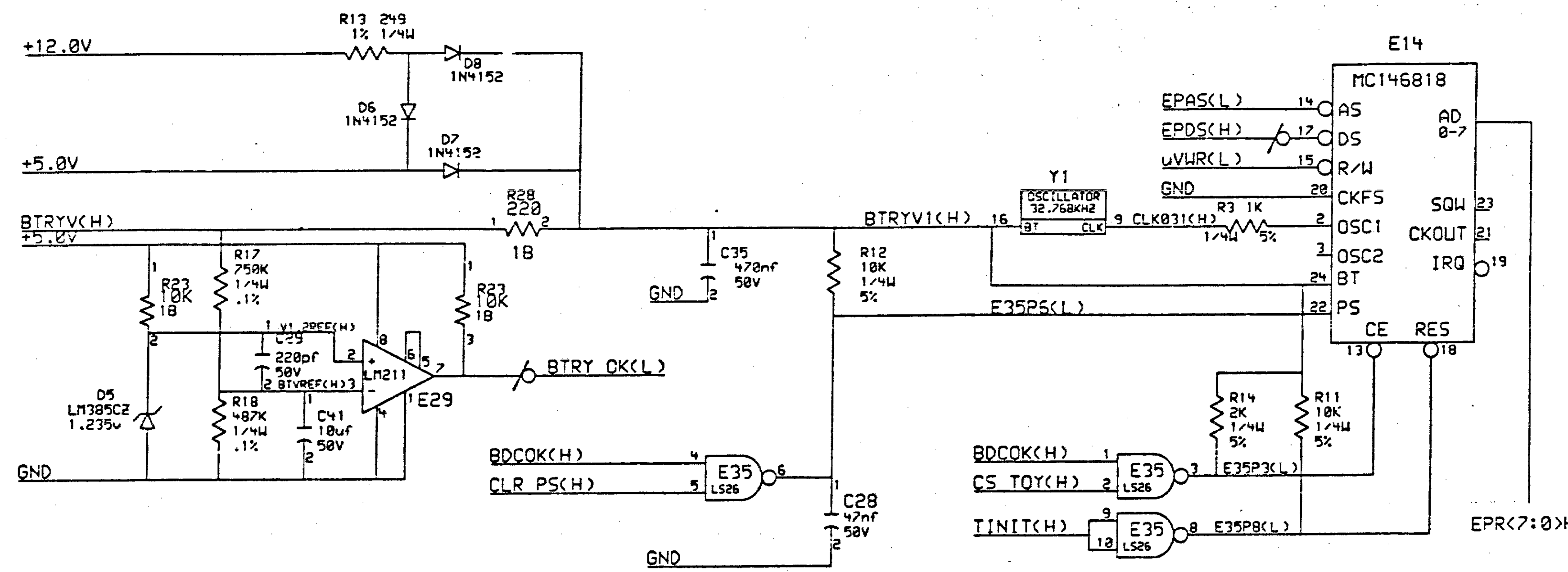
DRAWING

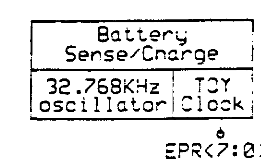
TITLE=GA1
ABBREV=GA1
CIRCUIT-TYPE=GATE-ARRAY
LAST-MODIFIED=Sun Oct 7 17:24:40 1984

DRN: BARRY MASKAS	DATE 19-DEC-83	ENG: BARRY MASKAS	DATE 19-DEC-83
CHK'D: BARRY MASKAS	DATE 19-DEC-83	SHEET 1 OF 1	
		NEXT HIGHER ASSEMBLY:	

TITLE: MEMORY SYSTEM ERROR REGISTER

SIZE	CODE	NUMBER	REV.
D	CS	M7605 -2 -41	E





REVISION HISTORY
REV | ECO NUMBER | DATE

DRAWING
TITLE=TOY
ABBREV=TOY
CIRCUIT←TYPE=TOY/CLOCK
LAST←MODIFIED=Fri Oct 12 11:59:59 1984

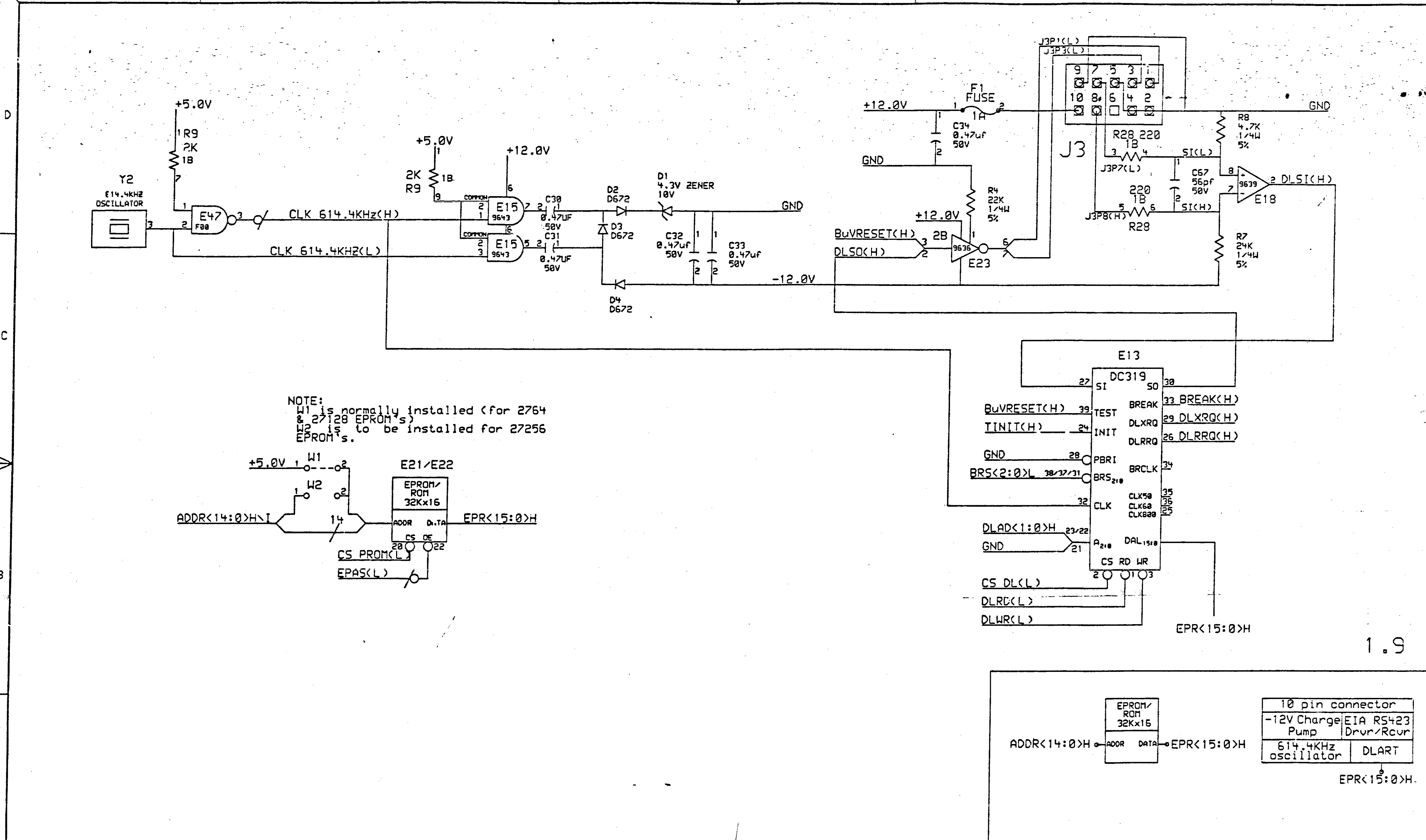
DEFINE
X←FIRST=0
X←STEP=SIZE

digital

DRN: BARRY MASKAS	DATE 3-OCT-84	ENG: BARRY MASKAS	DATE 3-OCT-84
CHK'D: BARRY MASKAS	DATE 3-OCT-84	SHEET 1 OF 1	
		NEXT HIGHER ASSEMBLY:	

TITLE: TIME OF YEAR (TOY) Clock

SIZE D | CODE CS | NUMBER M7625 -?- 12 | REV. B



REVISION HISTORY — REV | ECO NUMBER | DATE

DRAWING
TITLE=COMM
ABBREV=COMM
CIRCUIT+TYPE=SERIAL+I/O
LAST+MODIFIED=Fri Oct 12 14:27:55 1984

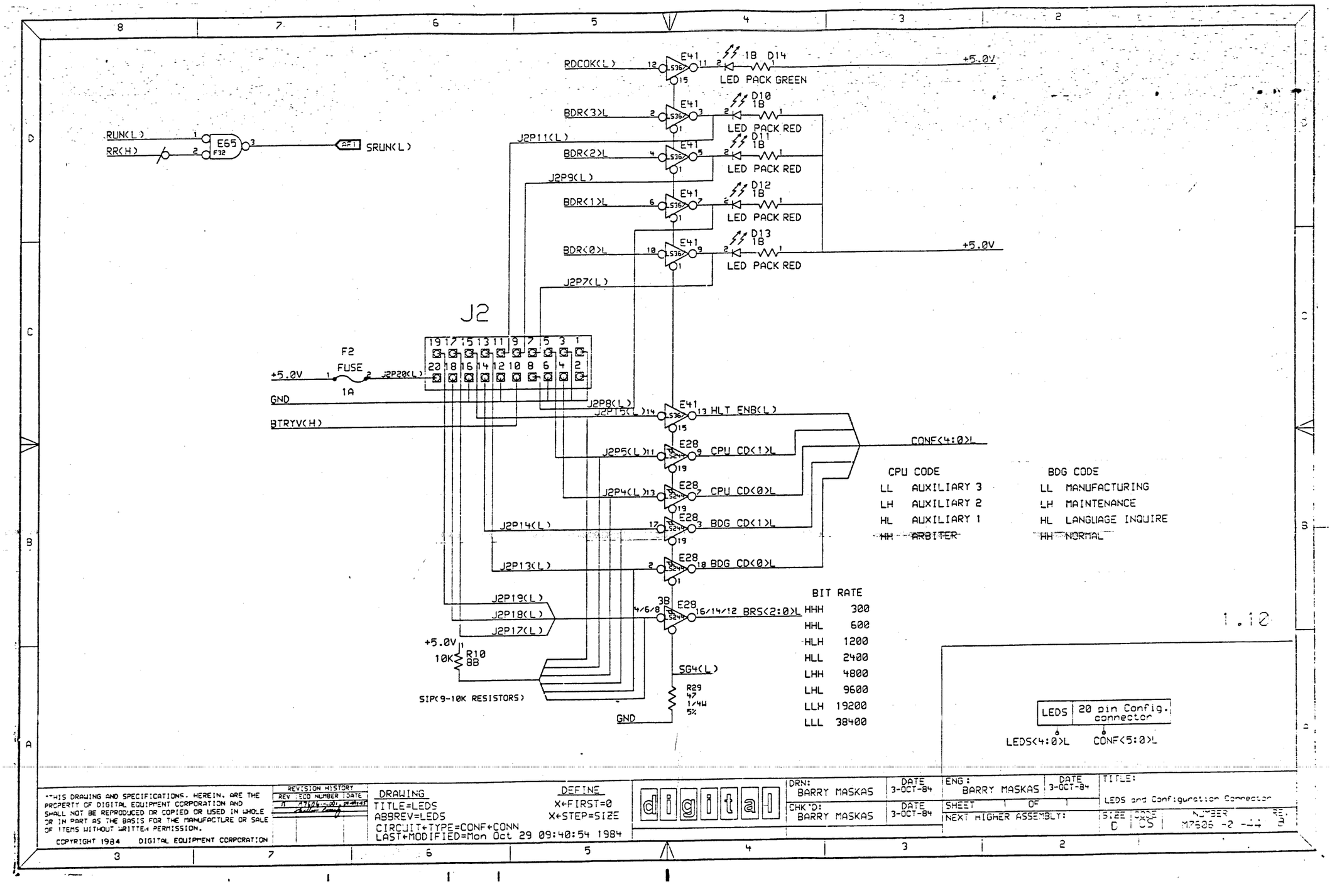
DEFINE
X+FIRST=0
X+STEP=SIZE

digital

DRN: BARRY MASKAS	DATE 3-OCT-84	ENG: BARRY MASKAS	DATE 3-OCT-84
CHK'D: BARRY MASKAS	DATE 3-OCT-84	SHEET 1 OF 1	
		NEXT HIGHER ASSEMBLY:	

TITLE: Console Serial Line Interface

SIZE	CODE	NUMBER	REV
D	CS	M7606 -0 -43	3



REVISION HISTORY

REV	ECO NUMBER	DATE
A	[illegible]	[illegible]

DRAWING
TITLE=LEDS
ABBREV=LEDS
CIRCUIT=TYPE=CONF=CONN
LAST=MODIFIED=Mon Oct 29 09:40:54 1984

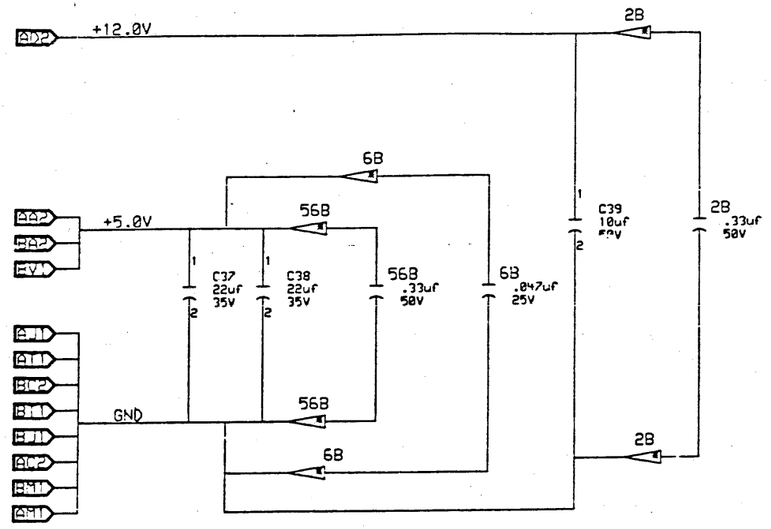
DEFINE
X=FIRST=0
X=STEP=SIZE

digital

DRN: BARRY MASKAS	DATE 3-OCT-84	ENG: BARRY MASKAS	DATE 3-OCT-84
CHK'D: BARRY MASKAS	DATE 3-OCT-84	SHEET 1 OF 1	
		NEXT HIGHER ASSEMBLY:	

TITLE: LEDS and Configuration Connector

SIZE D | CODE 05 | NUMBER M7505 -2 -A- | REV A



REVISION HISTORY

REV	ECO NUMBER	DATE
A	47826-74001	[illegible]

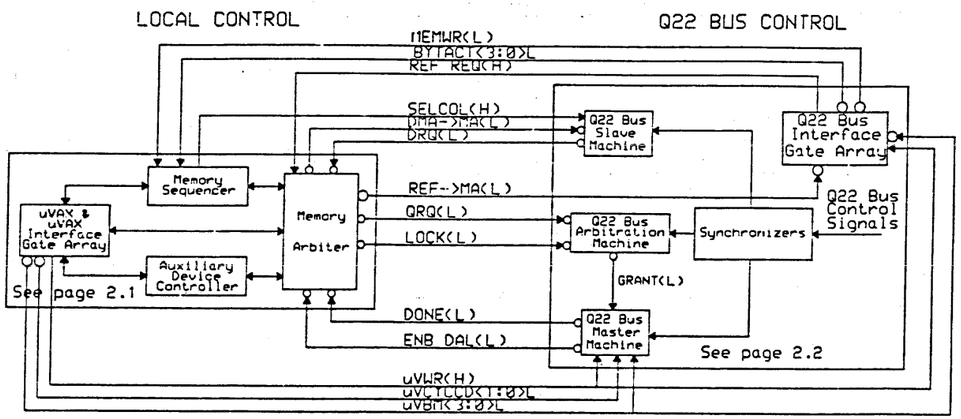
DRAWING

TITLE=KDQ32

LAST-MODIFIED=Sun Oct 7 20:49:41 1984

digital

DRN: BARRY MASKAS	DATE 3-OCT-84	ENG: BARRY MASKAS	DATE 3-OCT-84	TITLE: Decoupling Capacitors	
CHK'D: BARRY MASKAS	DATE 3-OCT-84	SHEET 1 OF 1			
		NEXT HIGHER ASSEMBLY:		SIZE D	CODE CS
				NUMBER M7505 -0 -5	REV B



REVISION HISTORY

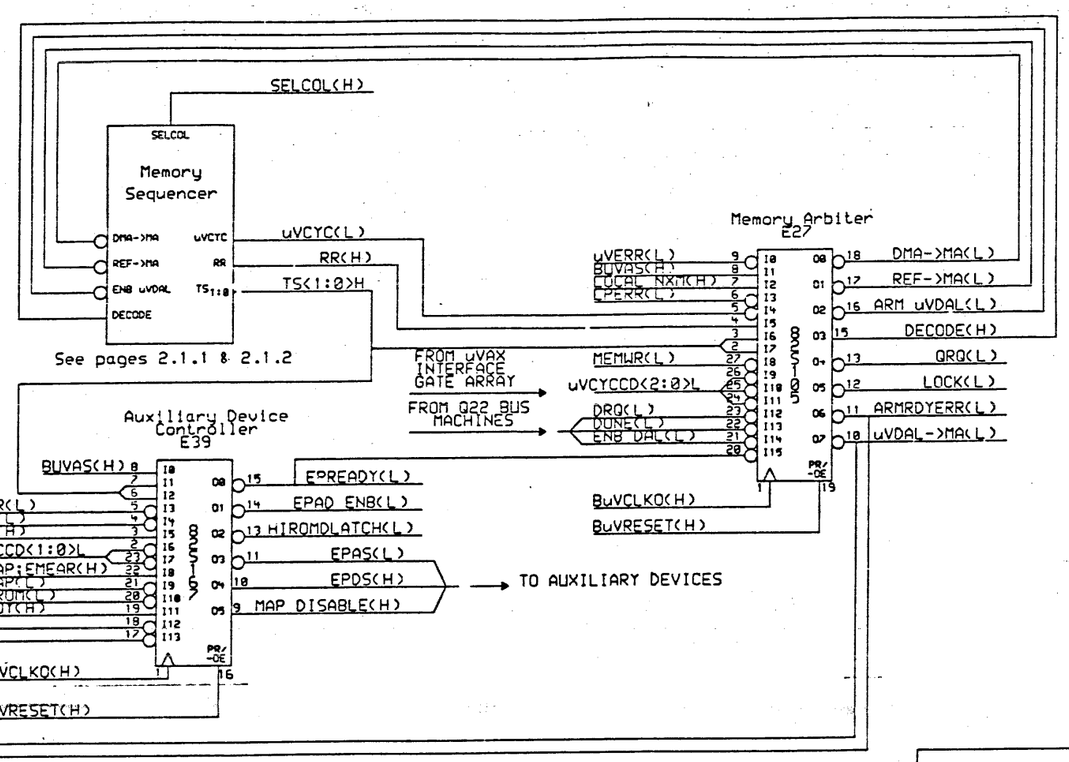
REV	ECO NUMBER	DATE
A	[illegible]	[illegible]

DRAWING

TITLE=CTLBLOCK
ABBREV=ctl
CIRCUIT-TYPE=CONTROL
LAST-MODIFIED=Mon Oct 29 09:44:18 1984

digital

DRN: BARRY MASKAS	DATE 8-DEC-83	ENG: BARRY MASKAS	DATE 8-DEC-83	TITLE: KA630 State Machines	
CHK'D: R. MCNAMARA	DATE 8-DEC-83	SHEET 1 OF			
		NEXT HIGHER ASSEMBLY:		SIZE C	CODE 09	NUMBER M7505-0 -46	REV B



REVISION HISTORY

REV	ECO NUMBER	DATE
J	ATM-0109	[illegible]

DRAWING
TITLE=UVAX MACHINE
ABBREV=uVMach
CIRCUIT+TYPE=control
LAST+MODIFIED=Sun Oct 7 18:51:31 1984

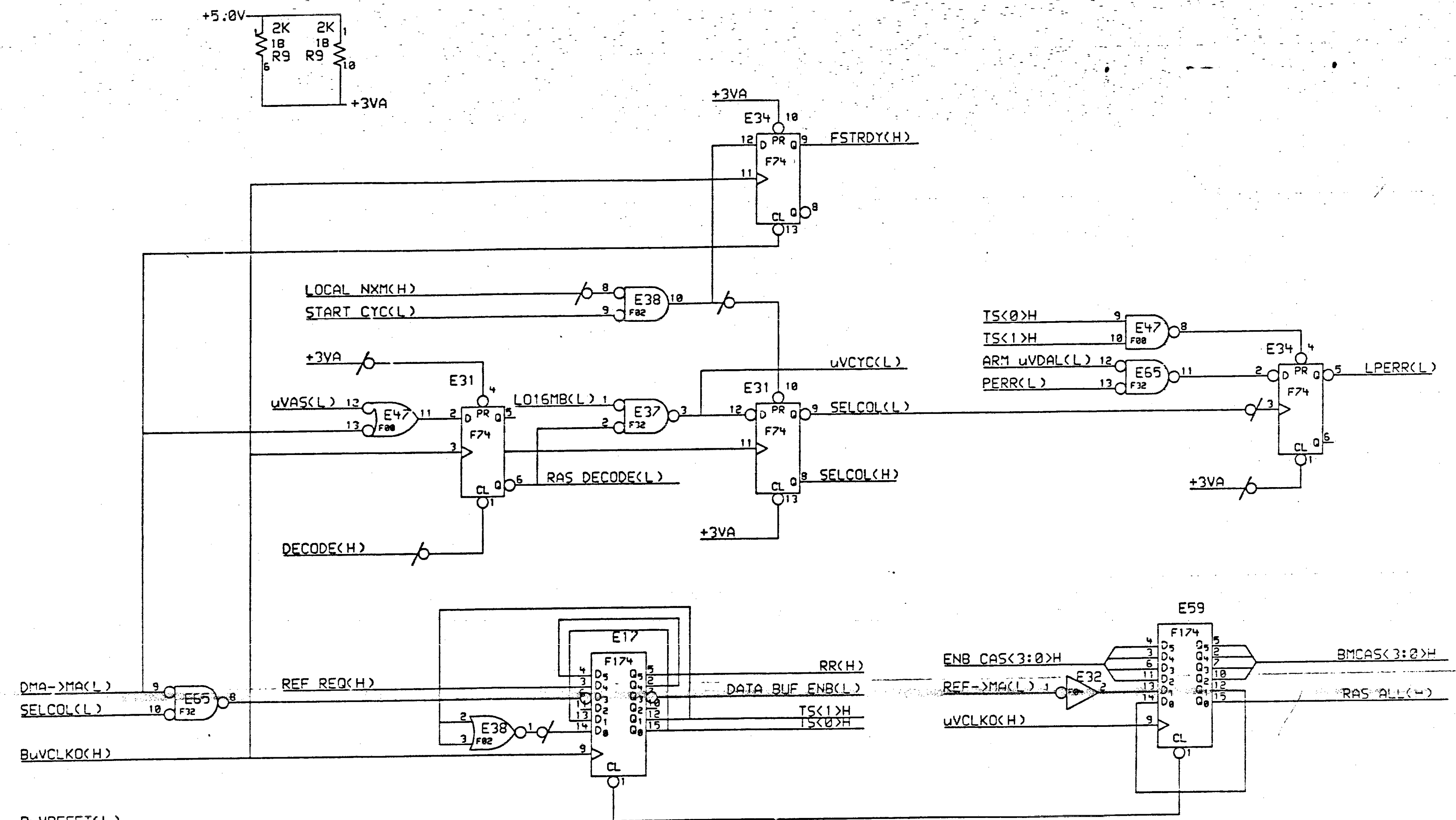
DEFINE
X+FIRST=0
X+STEP=SIZE

digital

DRN: BARRY MASKAS	DATE 3-OCT-84	ENG: BARRY MASKAS	DATE 3-OCT-84
CHK'D: BARRY MASKAS	DATE 3-OCT-84	SHEET 1 OF 1	
		NEXT HIGHER ASSEMBLY:	

TITLE: uVAX Cycle Controller

SIZE	CODE	NUMBER	REV
D	CS	M7505 -0 -47	E



TS(1:0) STATE TABLE (uVAX Microcycle Counter)

	s	ns	
T4	00	01	first uVAX CLKO after /BuVRESET
T1	01	11	
T2	11	10	
T3	10	00	

2.1.

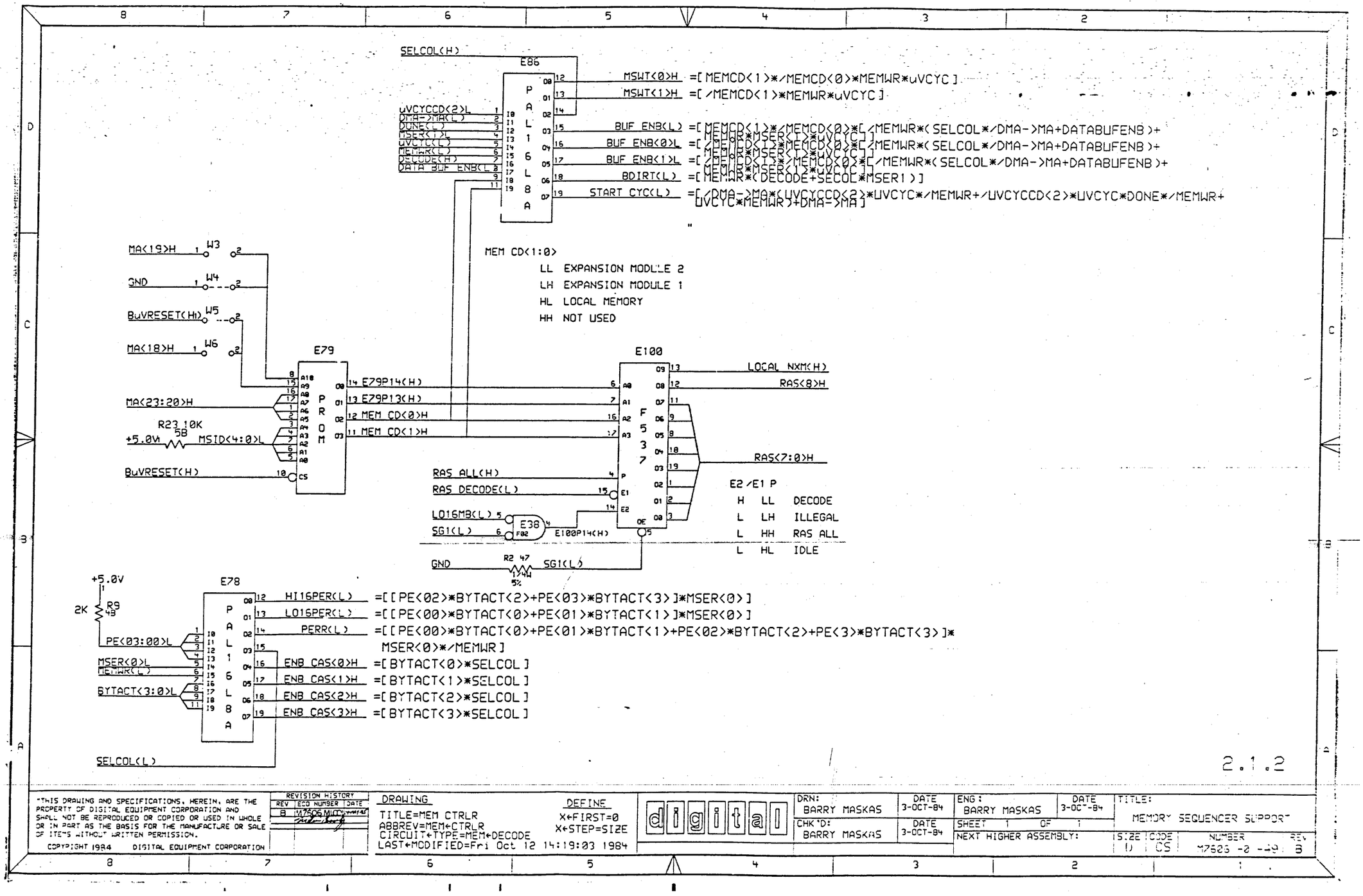
REVISION HISTORY
REV | ECO NUMBER | DATE
B | M7605-MC001 |

DRAWING
TITLE=MEM CTRLR
ABBREV=MEMCTRL
CIRCUIT+TYPE=MEM+CTRL
LAST+MODIFIED=Fri Oct 12 14:23:21 1984

digital

DRN: BARRY MASKAS — DATE 18-DEC-83
CHK'D: BARRY MASKAS — DATE 18-DEC-83
ENG: BARRY MASKAS — DATE 18-DEC-83
SHEET OF
NEXT HIGHER ASSEMBLY:

TITLE: MEMORY SEQUENCER
SIZE D | CODE CS | NUMBER M7605-2-43 | REV B



2.1.2

REVISION HISTORY

REV	ECO NUMBER	DATE
B	M7505 MICO	

DRAWING
TITLE=MEM CTRLR
ABBREV=MEM+CTRLR
CIRCUIT+TYPE=MEM+DECODE
LAST+MODIFIED=Fri Oct 12 14:19:03 1984

DEFINE
X+FIRST=0
X+STEP=SIZE

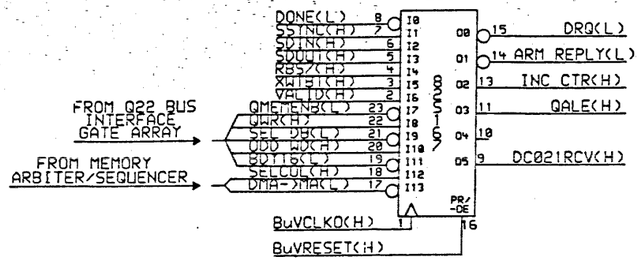
digital

DRN: BARRY MASKAS	DATE 3-OCT-84	ENG: BARRY MASKAS	DATE 3-OCT-84
CHK'D: BARRY MASKAS	DATE 3-OCT-84	SHEET 1 OF 1	
NEXT HIGHER ASSEMBLY:			

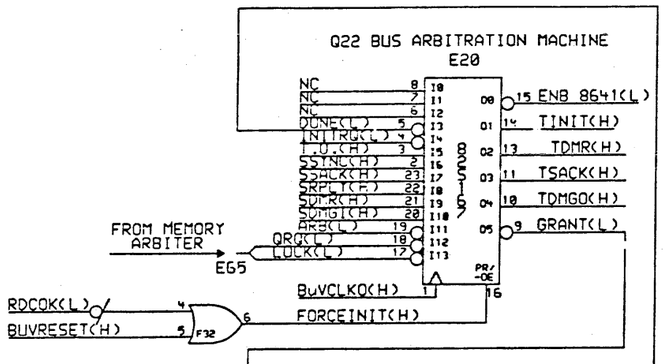
TITLE: MEMORY SEQUENCER SUPPORT

SIZE	CODE	NUMBER	REV
D	CS	M7583 -0 -49	B

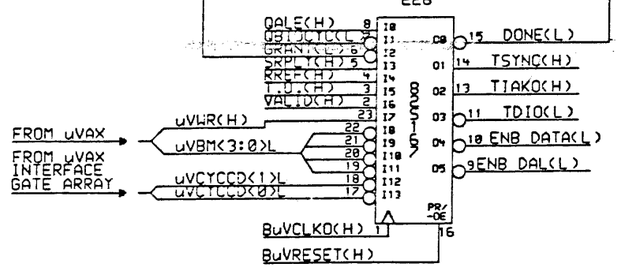
Q22 BUS SLAVE MACHINE
E33

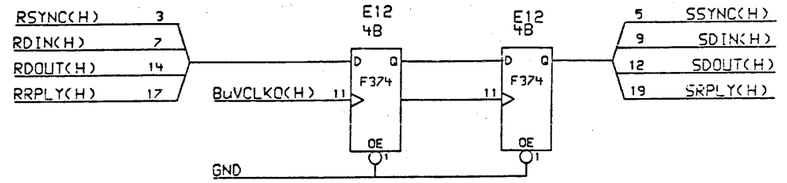


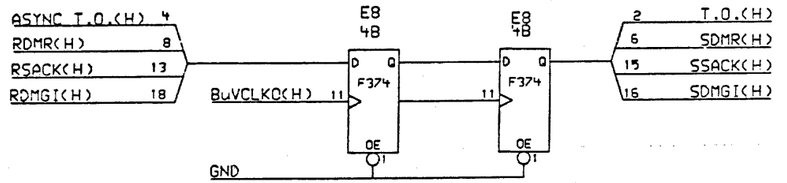
Q22 BUS ARBITRATION MACHINE
E20



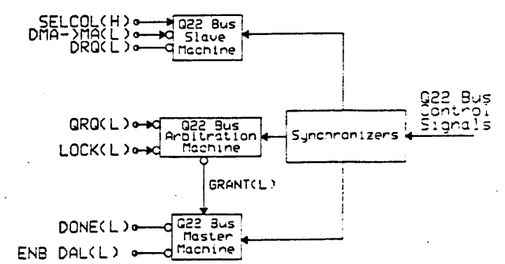
Q22 BUS MASTER MACHINE
E26







2.2



REVISION HISTORY		
REV	ECO NUMBER	DATE
A	[illegible]	[illegible]

DRAWING
TITLE=QBUS MACHINE
ABBREV=QCTRL
CIRCUIT+TYPE=QBUS+CNTRL
LAST+MODIFIED=Fri Oct 12 12:21:22 1984

DEFINE
~~X+EXIST=0~~
X+STEP=512E

digital

DRN: R. McNamara	DATE 3-OCT-84	ENG: R. McNamara	DATE 3-OCT-84	TITLE: Q22 BUS STATE MACHINES	
CHK'D: R. McNamara	DATE 3-OCT-84	SHEET 1 OF 1			
		NEXT HIGHER ASSEMBLY:		SIZE D	CODE 05
				NUMBER MT526 -0 -50	REV B

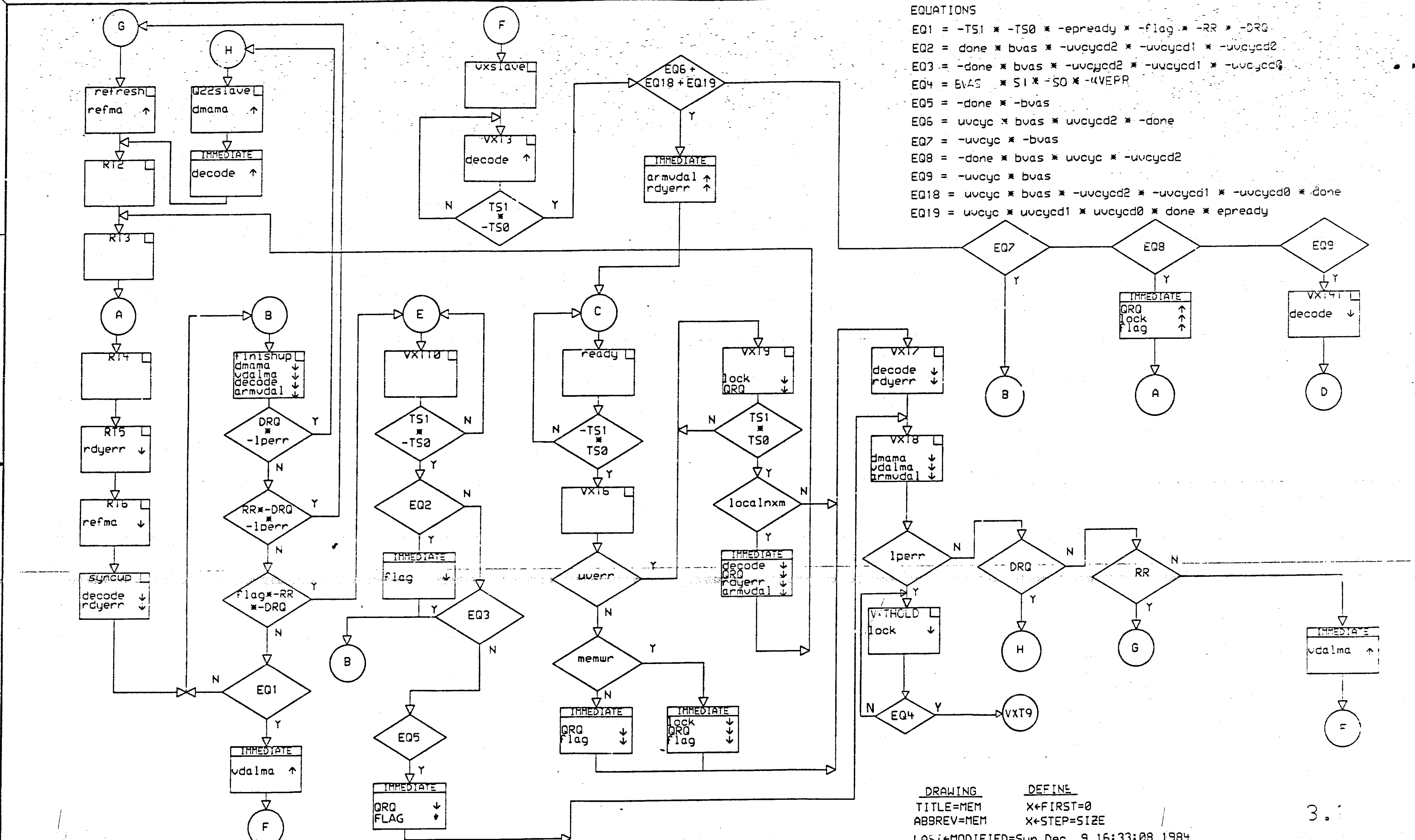
```
NAME 23_053L1_00__E27 ;MEMORY ARBITER MACHINE
OPTION PRESET
INPUT -EPRDY, -ENBADR, -DONE, -DRQ, -CYCD0, -CYCD1, -CYCD2,
INPUT -MEMWR, S0, S1, RR, -VCYC, -LPERR, LOCALNXM, BVAS, -VERR
OUTPUT -DALMA, -RDYERR, -LOCK, -QRQ, DECODE, -ARMDAL, -REFMA, -DMAMA

LOCAL FLAG ;LOCK FLAG PREVENTS VAX FROM CHANGING MEMORY UNTIL Q22 BUS
           ;MASTERSHIP, Q22 BUS AND REFRESH CYCLES ARE ALLOWED.
MACHINE 23_053L1_00__E27

STATE POWERUP ;LET REFRESH OR Q22 SLAVE THROUGH UNTIL Q22 BUS OWNED.
IF [ -DONE * S1 * -S0 * RR ] THEN FINISHUP [ -DMAMA, -DALMA, -DECODE,&
-ARMDAL, -FLAG ]
IF [ -DONE * DRQ ] THEN FINISHUP [ -DMAMA, -DALMA, -DECODE,&
-ARMDAL, -FLAG ]
IF [ DONE * -ENBADR * CYCD0 ] THEN VXT12 [ RDYERR, ARMDAL ] ;LOCAL MISS.
IF [ DONE * ENBADR * CYCD0 ] THEN Q22MT3 [ -DALMA ] ;LOCAL MISS AND GLOBAL HIT
IF [ DONE * CYCD1 * -CYCD0 ] THEN VXT12 [ RDYERR ] ;FINISH UP THE MAP CYCLE.

STATE SYNCUP, NUMBER -LLLLH
GOTO FINISHUP [ -DMAMA, -DALMA, -DECODE, -ARMDAL ]

STATE FINISHUP, NUMBER -HLLLH ;Q22 SLAVE CYCLES HAVE TOP PRIORITY, REFRESH
IF [ -LPERR  * DRQ ] THEN Q22SLAVE [ DMAMA ]
IF [ -LPERR * RR * -DRQ ] THEN REFRESH [ REFMA ] ;LPERR IS FOR OPTIMIZATION.
IF [ FLAG * -RR * -DRQ ] THEN VXT10 ;IF FLAGWAIT FOR DONE.
IF [ -S1 * -S0 * -EPRDY * -FLAG * -RR * -DRQ ] THEN VXSLAVE [ DALMA ]

STATE REFRESH, NUMBER -HHHLH
GOTO RT2

STATE RT2, NUMBER -LLLLL
GOTO RT3

STATE RT3  ;WHEN REFRESH, RAS<8:0>H AND LOCALNXM(H) ASSERT.
GOTO RT4

STATE RT4
GOTO RT5        [ -RDYERR ]

STATE RT5
GOTO RT6        [ -REFMA ]

STATE RT6
GOTO SYNCUP     [ -DECODE, -RDYERR ]

STATE Q22SLAVE, NUMBER -HLLLL  ;LOCAL MEMORY IS SLAVE TO Q22 BUS MASTER.
GOTO RT2 [ DECODE ]

STATE VXSLAVE, NUMBER -HHLLL  ;LOCAL MEMORY IS SLAVE TO VAX.
GOTO VXT3 [ DECODE ]

STATE VXT3, NUMBER -LHLLL
IF [ S1 * -S0 * VCYC * BVAS * CYCD2 * -DONE ] THEN READY [ ARMDAL, RDYERR ]
IF [ S1 * -S0 * VCYC * BVAS * -CYCD2 * -CYCD1 * -CYCD0 * DONE ] THEN READY &
[ ARMDAL, RDYERR ]
IF [ S1 * -S0 * VCYC * CYCD1 * CYCD0 * DONE * EPRDY ] THEN READY [ ARMDAL,&
RDYERR ]
IF [ S1 * -S0 * -BVAS * -VCYC ] THEN FINISHUP [ -DMAMA, -DALMA,&
-DECODE, -ARMDAL ]  ;IF NOTHING TO DO GO LOOK FOR REFRESH OR Q22 SLAVE.
IF [ S1 * -S0 * VCYC * BVAS * -CYCD2 * -DONE ] THEN RT4 [ QRQ, LOCK, FLAG ]
IF [ S1 * -S0 * -VCYC * BVAS ] THEN VXT41 [ -DECODE ]  ;WHAT CYCLE TO DO?

STATE VXT41 ;FIND OUT WHAT KIND OF CYCLE TO RUN?
IF [ -VCYC * CYCD2 * -CYCD1 * CYCD0 ] THEN Q22CYC [ QRQ, -DALMA, ARMDAL ]
IF [ -VCYC * -CYCD2 * -CYCD1 * CYCD0 ] THEN PROMCYC [ RDYERR ]
IF [ -VCYC * -CYCD1 * -CYCD0 ] THEN RT4
IF [ -VCYC * CYCD2 * CYCD1 * -CYCD0 ] THEN Q22CYC
IF [ -VCYC * -CYCD2 * CYCD1 * -CYCD0 ] THEN Q22CYC [ LOCK ]
IF [ -VCYC * CYCD2 * CYCD1 * CYCD0 ] THEN Q22CYC [ ARMDAL ]
IF [ -VCYC * -CYCD2 * CYCD1 * CYCD0 ] THEN Q22CYC [ LOCK, ARMDAL ]

STATE READY ;CYCLE IS RUNNING AND EPR MACHINE ASSERTS EPRDY
IF [ -S1 * S0 ] THEN VXT6 ;TO STROBE MEMCD<1:0> OR MSER WRITE DATA.

STATE VXT6 ;IF VAX ERROR PIN IS ASSERTED, EXTRA uCYCLE OCCURS.
IF [ VERR ] THEN VXT9 [ -LOCK, -QRQ ] ;FREE Q22 BUS ON ERRORS OR MEMORY WRITES.
IF [ -VERR * -MEMWR ] THEN VXT7 [ -QRQ, -DECODE, -RDYERR, -FLAG ]
IF [ -VERR * MEMWR ] THEN VXT7 [ -LOCK, -DECODE, -RDYERR, -FLAG, -QRQ ]

STATE VXT7, NUMBER -LLLHH
GOTO VXT8  [ -DMAMA, -DECODE, -DALMA, -ARMDAL ]

STATE VXT8, NUMBER -HLLHH ;IF LOCAL PARITY ERROR THEN PROTECT MEMORY AND WAIT
IF [ LPERR ] THEN VXTHOLD [ -LOCK ]
IF [ -LPERR * -RR * -DRQ ] THEN VXSLAVE [ DALMA ]  ;ALLOW Q22 IAKS.
IF [ -LPERR * RR * -DRQ ] THEN REFRESH [ REFMA ]  ;ALLOW REFRESH.
IF [ -LPERR * DRQ ] THEN Q22SLAVE [ DMAMA ]  ;ALLOW Q22 SLAVE.

STATE VXTHOLD ;FORCE VAX MACHINE CHECK, THEN ALLOW MEMORY CYCLES
IF [ BVAS * S1 * -S0 * -VERR ] THEN VXT9

STATE VXT9  ;STALL ONE MICROCYCLE IF VAX SAW AN ERROR.
IF [ S1 * S0 * -LOCALNXM ] THEN VXT7 [ -DECODE, -RDYERR ]
IF [ S1 * S0 * LOCALNXM ] THEN RT3 [ -DECODE, -QRQ, -RDYERR, -ARMDAL ]

STATE VXT10 ;STALL UNTIL Q22 BUS MASTERSHIP THEN RUN READ LOCK CYCLE.
IF [ S1 * -S0 * DONE * BVAS * -CYCD2 * -CYCD1 * -CYCD0 ] THEN FINISHUP&
[-FLAG ]
IF [ S1 * -S0 * -DONE * BVAS * -CYCD2 * -CYCD1 * -CYCD0 ] THEN FINISHUP
IF [ S1 * -S0 * -DONE * -BVAS ] THEN VXT8 [  -FLAG, -DMAMA, -QRQ, -DALMA,&
-ARMDAL ]

STATE PROMCYC  ;EPR MACHINE RUNS A PROM CYCLE WHEN RDYERR IS ASSERTED.
IF [ EPRDY ] THEN RT4  ;EPR MACHINE ASSERTS EPRDY WHEN PROM CYCLE IS DONE.

STATE VXT12  ;EPR MACHINE IS DOING THE SYNCING.
IF [ EPRDY ] THEN READY [ RDYERR ]  ;EPR MACHINE IS DONE AND VAX
                                    ;IS FINISHING.
STATE Q22CYC ;Q22 BUS DATA CYCLE OR IAK.
IF [ S1 * S0 ] THEN POWERUP [ QRQ ]

STATE Q22MT3  ;GET IN STEP AND GO RUN THE MISS-HIT CYCLE, TELL EPR MACHINE.
IF [ S1 * -S0 ] THEN Q22MT4 [ DMAMA, RDYERR ]

STATE Q22MT4, NUMBER -HHLLH
GOTO VXSLAVE

END
```


REVISIONS		
CHK	CHANGE NO.	REV

digital	DRN. [signature]	DATE 09-AUG-85	ENG. R. MCNAMARA	DATE 09-AUG-85
	CHK'D. R. MCNAMARA	DATE 09-AUG-85	BOARD LOCATION:	
DSK:9.T2P[4,550]	09-AUG-85 07:40		SHEET 1 OF 1	
FIRST USED ON OPTION/MODEL:			NEXT HIGHER ASSEMBLY:	

TITLE: MEMORY ARBITER LISTING

SIZE	CODE	NUMBER	REV.
D	CS	M7606-0-51 —	A



EQUATIONS

EQ1 = -TS1 * -TS0 * -epready * -flag * -RR * -DRQ

EQ2 = done * bvas * -uvcycd2 * -uvcycd1 * -uvcycd2

EQ3 = -done * bvas * -uvcycd2 * -uvcycd1 * -uvcycd0

EQ4 = BVAS * S1 * -S0 * -UVEPR

EQ5 = -done * -bvas

EQ6 = uvcyc * bvas * uvcycd2 * -done

EQ7 = -uvcyc * -bvas

EQ8 = -done * bvas * uvcyc * -uvcycd2

EQ9 = -uvcyc * bvas

EQ18 = uvcyc * bvas * -uvcycd2 * -uvcycd1 * -uvcycd0 * done

EQ19 = uvcyc * uvcycd1 * uvcycd0 * done * epready

DRAWING

TITLE=MEM

ABBREV=MEM

DEFINE

X←FIRST=0

X←STEP=SIZE

LAST←MODIFIED=Sun Dec 9 16:33:08 1984

3.

digital

DRN. BARRY MASKAS DATE 29-AUG-1984 ENG. BARRY MASKAS DATE 29-AUG-1984

CHK'D. BARRY MASKAS DATE 29-AUG-1984

BOARD LOCATION:

SHEET C- 2

TOP DOCUMENT NUMBER:

USRA:

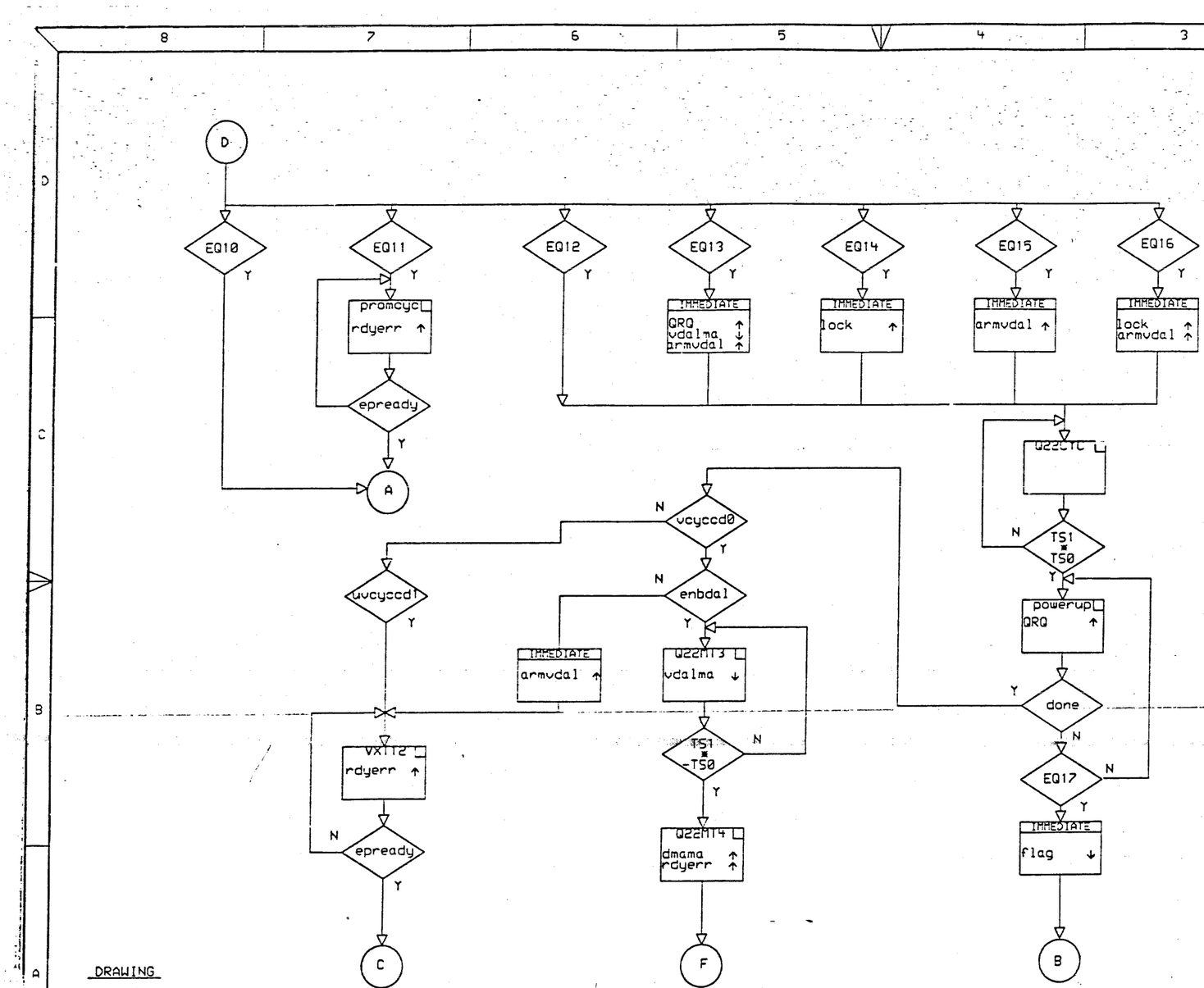
FIRST USED ON OPTION/MODEL:

TITLE: KA630 MEMORY SYSTEM ARBITER STATE FLOW DIAGRAMS

SIZE D CODE CS NUMBER M7606-0-52 REV.

REVISION CHK CHANGE NO REV

M7606-0-52



EQUATIONS

EQ10 = -uvcyc * -uvcycd1 * -uvcycd0

EQ11 = -uvcyc * -uvcycd2 * -uvcycd1 * uvcycd0

EQ12 = -uvcyc * uvcycd2 * uvcycd1 * -uvcycd0

EQ13 = -uvcyc * uvcycd2 * -uvcycd1 * uvcycd0

EQ14 = -uvcyc * -uvcycd2 * uvcycd1 * -uvcycd0

EQ15 = -uvcyc * uvcycd2 * uvcycd1 * uvcycd0

EQ16 = -uvcyc * -uvcycd2 * uvcycd1 * uvcycd0

EQ17 = DRQ + TS1 * -TS0 * RR

DRAWING

NAME=MEM
ABBREV=MEM
LAST-MODIFIED=Sun Dec 9 16:40:59 1984

3.2

REVISION		
CHK	CHANGE NO.	REV
	147606-M001	B

DRN: BARRY MASKAS
CHK'D: BARRY MASKAS
ENG: BARRY MASKAS
BOARD LOCATION:
USED:
FIRST USED ON OPTION/MODEL:
TOP DOCUMENT NUMBER:

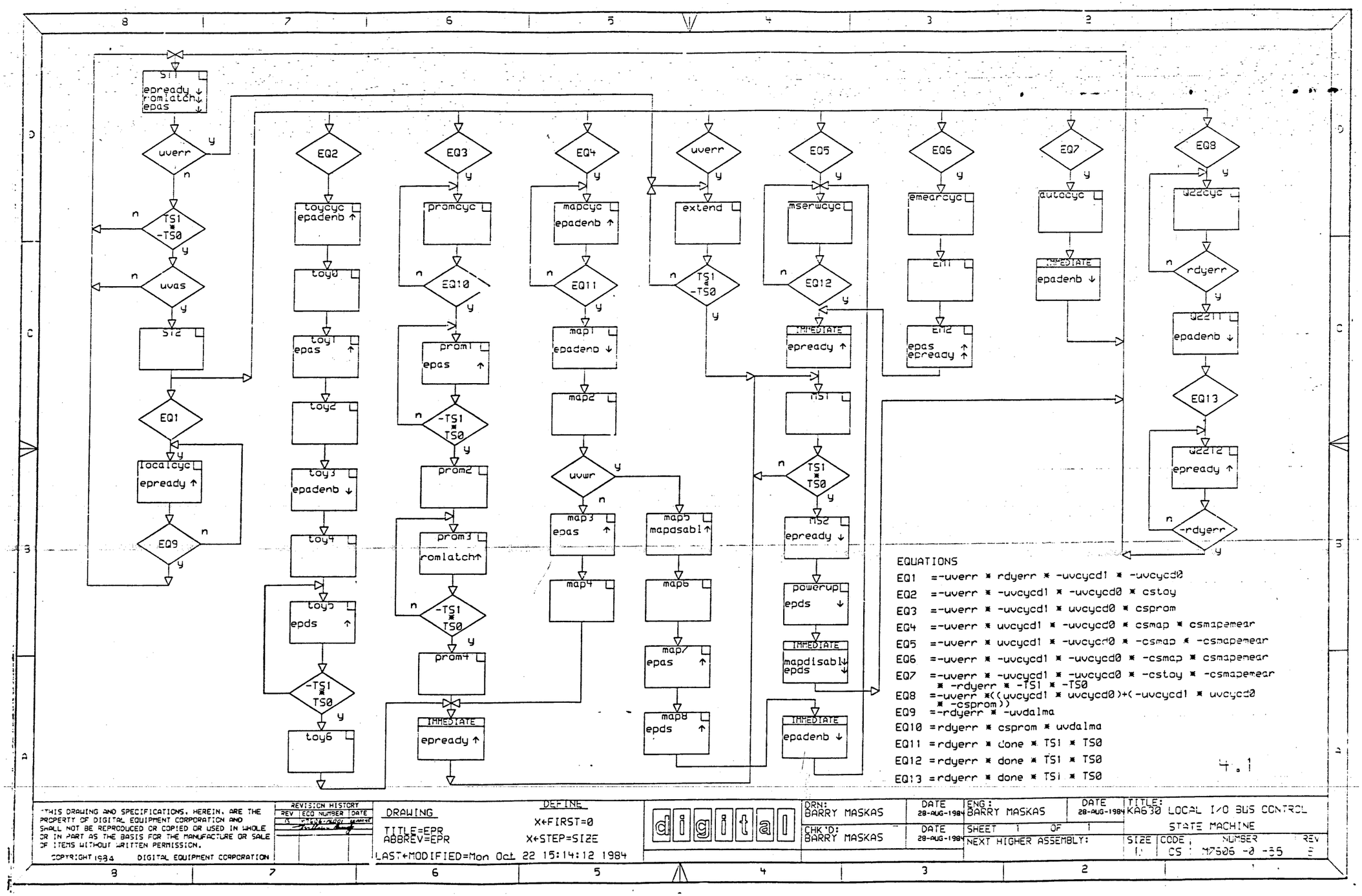
TITLE: KA630 MEMORY SYSTEM ARBITER STATE FLOW DIAGRAM

SIZE: D | CODE: 05 | NUMBER: 47606-0-03 | REV: B

```
NAME 23_014L3_00 ;KA630 LOCAL I/O CONTROL MACHINE revision 2
OPTION PRESET
INPUT NC1, -UVDALMA, -RDYERR, CSTOY, -CSPROM, -CSMAP, CSMAPEMEAR,
INPUT -UVCYCD0, -UVCYCD1, NC0, UVWR, -DONE, -UVERR, TS0, TS1, BUVAS
OUTPUT NC3, MAPDISABLE, EPDS, -EPAS, NC2, -HIROMDLATCH, -EPADENB, -EPREADY

MACHINE 23_014L3_00

STATE POWERUP
GOTO ST1 [ -MAPDISABLE, -EPDS, -EPREADY, -EPAS, -HIROMDLATCH ]

STATE ST1, NUMBER LLHHLL
IF [ TS1 * -TS0 * BUVAS * -UVERR ] THEN ST2
IF [ TS1 * -TS0 * UVERR ] THEN EXTEND

STATE ST2, NUMBER LLLHLL ;WHAT SHOULD RUN? IF Q22 BUS PUT ADDRESS ON EPR.
IF [ -UVERR * RDYERR * -UVCYCD1 * -UVCYCD0 ] THEN LOCALCYC [ EPREADY ]
IF [ -UVERR * -UVCYCD1 * -UVCYCD0 * CSTOY ] THEN TOYCYC [ EPADENB ]
IF [ -UVERR * -UVCYCD1 * UVCYCD0 * CSPROM ] THEN PROMCYC
IF [-UVERR * UVCYCD1 * -UVCYCD0 * CSMAP * CSMAPEMEAR ] THEN MAPCYC [ EPADENB ]
IF [ -UVERR * UVCYCD1 * -UVCYCD0 * -CSMAP * -CSMAPEMEAR ] THEN MSERWCYC
IF [ -UVERR * -UVCYCD1 * -UVCYCD0 * -CSMAP * CSMAPEMEAR ] THEN EMEARCYC
IF [ -UVERR * -UVCYCD1 * -UVCYCD0 * -CSTOY * -CSMAPEMEAR * -RDYERR * -TS1 *&
-TS0 ] THEN AUTOCYC
IF [ -UVERR *((UVCYCD1 * UVCYCD0) + (-UVCYCD1 * UVCYCD0 * -CSPROM))] THEN&
Q22CYC [ EPADENB ]
IF [ UVERR ] THEN EXTEND

STATE EXTEND, NUMBER LLHLLL
IF [ TS1 * -TS0 ] THEN MS1

STATE LOCALCYC  ;FAST READY FLEW BY BUT EPREADY ASSERTS TO STROBE ERRORS.
IF [ -RDYERR * -UVDALMA ] THEN ST1 [ -EPREADY, -HIROMDLATCH, -EPAS ]

STATE TOYCYC, NUMBER HLLHHH  ;TOY CLOCK CYCLE
GOTO TOYT0

STATE TOYT0, NUMBER HLLHHL  ;ADDRESS SETUP TIME
GOTO TOYT1          [ EPAS ]  ;CHIP SELECT AND ADDRESS ARE STABLE SO GO TO IT.

STATE TOYT1, NUMBER HLLHLL
GOTO TOYT2  ;ADDRESS HOLD TIME.

STATE TOYT2, NUMBER HLLHLH
GOTO TOYT3          [ -EPADENB ]

STATE TOYT3, NUMBER HLLLLH
GOTO TOYT4  ;PREVENT TRISTATE OVERLAP.

STATE TOYT4, NUMBER HLHLLH
GOTO TOYT5          [ EPDS ] ;GET OR PUT THE DATA.

STATE TOYT5, NUMBER LLHLLH  ;DELAY FOR DATA ACCESS TIME.
IF [ -TS1 * TS0 ] THEN TOYT6

STATE TOYT6, NUMBER LHLLLL  ;TELL UVAX THAT CYCLE CAN FINISH.
GOTO MS1 [ EPREADY ]

STATE PROMCYC  ;PROM CYCLE
IF [ UVDALMA * CSPROM * RDYERR ] THEN PROMT1 [ EPAS ]  ;ADDRESS OK?

STATE PROMT1  ;DELAY FOR ACCESS TIME.
IF [ -TS1 * TS0 ] THEN PROMT2

STATE PROMT2  ;DELAY FOR ACCESS TIME, STROBE HI 16 BITS INTO LATCH.
GOTO PROMT3 [ HIROMDLATCH ]  ;CHANGE ADDRESS TO LO 16 BITS.

STATE PROMT3  ;DELAY FOR ACCESS TIME.
IF [ -TS1 * TS0 ] THEN PROMT4

STATE PROMT4, NUMBER HLLLLL  ;TELL MEMORY MACHINE AND UVAX TO FINISH.
GOTO MS1 [ EPREADY ]

STATE MAPCYC  ;MAP CYCLE
IF [ RDYERR * DONE * TS1 * TS0 ] THEN MAPT1 [ -EPADENB ]  ;HAVE THE Q22 BUS?

STATE MAPT1, NUMBER LLLHHH
GOTO MAPT2  ;PREVENT TRISTATE OVERLAP.

STATE MAPT2, NUMBER LLLHLH  ;READ OR WRITE CYCLE?
IF [ UVWR ] THEN MAPT5 [ MAPDISABLE ]  ;IF WRITE THEN Z THE MAP OUTPUTS.
IF [ -UVWR ] THEN MAPT3 [ EPAS ]  ;IF READ THEN GET DATA ON EPR BUS.

STATE MAPT3, NUMBER HHLLLH
GOTO MAPT4  ;DELAY ONE TICK TO SYNC UP.

STATE MAPT4, NUMBER HHLLLL  ;TELL UVAX AND MEMORY MACHINE TO FINISH.
GOTO MS1 [ EPREADY ]

STATE MAPT5
GOTO MAPT6  ;PREVENT TRISTATE OVERLAP.

STATE MAPT6  ;ENABLE THE WRITE DATA.
GOTO MAPT7     [ EPAS ]

STATE MAPT7  ;ASSERT THE WRITE STROBE.
GOTO MAPT8    [ EPDS ]

STATE MAPT8  ;SYNC UP WITH UVAX AND MEMORY MACHINE.
GOTO MSERWCYC [ -EPADENB ]

STATE MSERWCYC  ;MSER WRITE CYCLE, GET THE Q22 BUS, STROBE THE DATA.
IF [ RDYERR * DONE * TS1 * TS0 ] THEN MS1 [ EPREADY ]

STATE MS1, NUMBER LLLLLL  ;STROBE THE MSER DATA WITH EPREADY.
IF [ TS1 * TS0 ] THEN MS2 [ -EPREADY ]

STATE MS2
GOTO POWERUP [ -EPDS ]

STATE EMEARCYC, NUMBER HHHHLH ;EXTERNAL MEAR CYCLE.
GOTO EM1

STATE EM1, NUMBER HHHLLH ;ENABLE THE EPR DATA AND TELL UVAX TO FINISH.
GOTO EM2 [ EPAS, EPREADY ]

STATE EM2, NUMBER HHHLLL
GOTO MS1 [ EPREADY ]

STATE AUTOCYC  ;NOTHING TO DO SO BACK FOR ANOTHER LOOK.
GOTO ST1 [ -EPREADY, -HIROMDLATCH, -EPAS, -EPADENB ]

STATE Q22CYC  ;Q22 BUS IAK OR Q22 BUS READ OR WRITE.
IF [ RDYERR ] THEN Q22T1 [ -EPADENB ]

STATE Q22T1
IF [ RDYERR * DONE * TS1 * TS0 ] THEN Q22T2 [ EPREADY ]

STATE Q22T2  ;WAIT UNTIL MEMORY MACHINE IS DONE.
IF [ -RDYERR ] THEN ST1 [ -EPREADY, -HIROMDLATCH, -EPAS ]

END
```


REVISIONS		
CHK	CHANGE NO.	REV

digital | DRN. [signature] | DATE 09-AUG-85 | ENG. R. MCNAMARA | DATE 09-AUG-85
CHK'D. R. MCNAMARA | DATE 09-AUG-85 | BOARD LOCATION: | SHEET 1 OF 1
DSK:8.T2P(4,550) 09-AUG-85 07:40 | NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL:
TITLE: LOCAL I/O CONTROL MACHINE LISTING
SIZE D | CODE CS | NUMBER M7606-0-54 | REV. A



EQUATIONS

EQ1 =-uverr * rdyerr * -uvcycd1 * -uvcycd0

EQ2 =-uverr * -uvcycd1 * -uvcycd0 * cstoy

EQ3 =-uverr * -uvcycd1 * uvcycd0 * csprom

EQ4 =-uverr * uvcycd1 * -uvcycd0 * csmap * csmapemear

EQ5 =-uverr * uvcycd1 * -uvcycd0 * -csmap * -csmapemear

EQ6 =-uverr * -uvcycd1 * -uvcycd0 * -csmap * csmapemear

EQ7 =-uverr * -uvcycd1 * -uvcycd0 * -cstoy * -csmapemear * -rdyerr * -TS1 * -TS0

EQ8 =-uverr *((uvcycd1 * uvcycd0)+(-uvcycd1 * uvcycd0 * -csprom))

EQ9 =-rdyerr * -uvdalma

EQ10 =rdyerr * csprom * uvdalma

EQ11 =rdyerr * done * TS1 * TS0

EQ12 =rdyerr * done * TS1 * TS0

EQ13 =rdyerr * done * TS1 * TS0

4.1

REVISION HISTORY		
REV	ECO NUMBER	DATE
A	WORKING DRAWING	

DRAWING
TITLE=EPR
ABBREV=EPR

DEFINE
X←FIRST=0
X←STEP=SIZE

LAST←MODIFIED=Mon Oct 22 15:14:12 1984

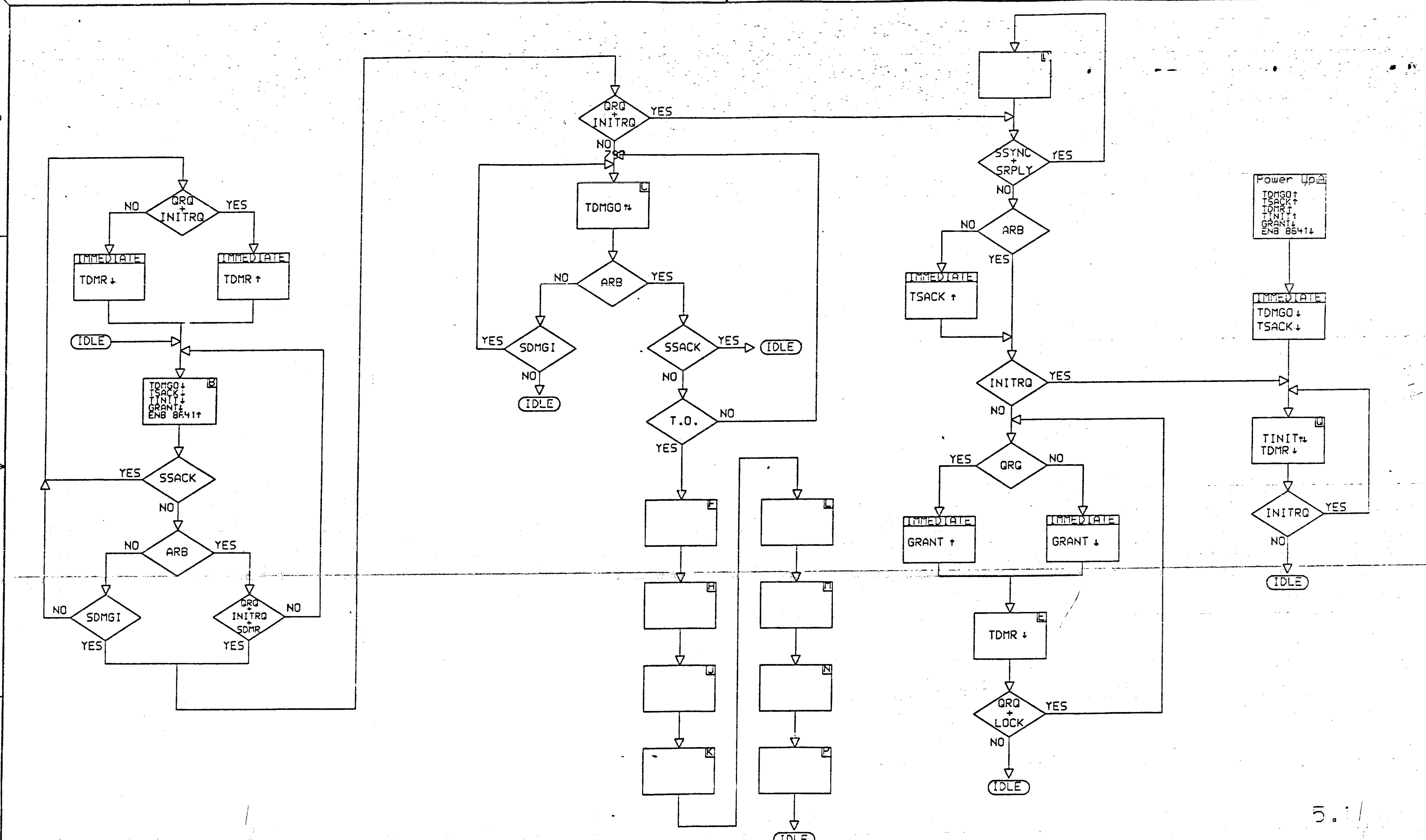
digital

DRN: BARRY MASKAS	DATE 28-AUG-1984	ENG: BARRY MASKAS	DATE 28-AUG-1984	TITLE: KA630 LOCAL I/O BUS CONTROL STATE MACHINE
CHK'D: BARRY MASKAS	DATE 28-AUG-1984	SHEET 1 OF 1		
		NEXT HIGHER ASSEMBLY:	SIZE C	CODE: CS NUMBER M7506 -0 -35 REV E

```
name 23_008L3_00_E20    ;Q22 bus arbitration control machine

input   nci15, -lock, -qrq, -arb, sdmgi, sdmr, srply, ssack,
input   ssync, nci6, t_o, -initrq, -done, nci2, nci1, nci0

output  nco7, -grant, tdmgo, tsack, nci3, tdmr, tinit, -enb8641

machine q_bus_arb

state A
goto Q [-grant, -tdmgo, -tsack, -tdmr, tinit, -enb8641]

state B
if [-ssack * (arb + (-arb * sdmgi)) * (qrq + initrq) * (ssync + srply)] then D
if [-ssack * arb * qrq * -initrq * -ssync * -srply] then E [grant, -tdmr]
if [-ssack * arb *        initrq * -ssync * -srply] then Q [tinit, -tdmr]
if [-ssack * ((arb * sdmr) + (-arb * sdmgi)) * -qrq * -initrq] then C [tdmgo]
if [-ssack * -arb * sdmgi * qrq * -initrq * -ssync * -srply] then E &
      [grant, -tdmr, tsack]
if [-ssack * -arb * sdmgi *        initrq * -ssync * -srply] then Q &
      [tinit, -tdmr, tsack]
if [ssack * (qrq + initrq) + -arb * -sdmgi * (qrq + initrq)] then [ tdmr]
if [ssack * -qrq * -initrq + -arb * -sdmgi * -qrq * -initrq + &
      arb * -qrq * -initrq * -sdmr] then [-tdmr]

state C
if [arb * ssack] then B [-tdmgo, -tsack, -tinit, -grant, enb8641]
if [arb * -ssack * t_o] then F [-tdmgo]
if [-arb * -sdmgi] then B [-tdmgo, -tsack, -tinit, -grant, enb8641]

state D
if [-ssync * -srply * arb * qrq * -initrq] then E [grant, -tdmr]
if [-ssync * -srply * arb * -qrq * -initrq] then E [-grant, -tdmr]
if [-ssync * -srply * arb *  initrq] then Q [tinit, -tdmr]
if [-ssync * -srply * -arb * qrq * -initrq] then E [grant, tsack, -tdmr]
if [-ssync * -srply * -arb * -qrq * -initrq] then E [-grant, tsack, -tdmr]
if [-ssync * -srply * -arb * initrq] then Q [tinit, tsack, -tdmr]

state E
if [-qrq * -lock] then B [-tdmgo, -tsack, -tinit, -grant, enb8641]
if [-qrq] then [-grant]
if [qrq] then [grant]

state F
goto H

state H
goto J

state J
goto K

state K
goto L

state L
goto M

state M
goto N

state N
goto P

state P
goto B [-tdmgo, -tsack, -tinit, -grant, enb8641]

state Q
if [-initrq] then B [-tdmgo, -tsack, -tinit, -grant, enb8641]

END
```


REVISIONS		
CHK	CHANGE NO.	REV

DRN.	DATE	ENG.	DATE	TITLE:	Q22 BUS ARB. CTL MACHINE LISTING
CHK D. R. MCNAMARA	09-AUG-85	R. MCNAMARA	09-AUG-85		
	09-AUG-85	BOARD LOCATION:			
DSK:S.T2P[4,550]	09-AUG-85 07:39	SHEET 1 OF 1			
FIRST USED ON OPTION/MODEL:		NEXT HIGHER ASSEMBLY:		SIZE D / CODE CS / NUMBER M7606-0-56 / REV. A	



"THIS DRAWING AND SPECIFICATIONS, HEREIN, ARE THE PROPERTY OF DIGITAL EQUIPMENT CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION. COPYRIGHT 1984 DIGITAL EQUIPMENT CORPORATION	REVISION HISTORY: REV / ECO NUMBER / DATE	DRAWING TITLE=ARB ABBREV=arb LAST←MODIFIED=Mon Oct 22 15:04:38 1984	DEFINE X←FIRST=0 X←STEP=SIZE	digital	DRN: R. McNamara DATE 6-Jul-84; CHK'D: R. McNamara DATE 6-Jul-84	ENG: R. McNamara DATE 6-Jul-84; SHEET 1 OF 1; NEXT HIGHER ASSEMBLY:	TITLE: QBUS ARBITRATION CONTROLLER DETAILED CONTROL FLOW DIAGRAM; SIZE D; CODE CS; NUMBER M7505 -?-57; REV B

```
name 23_009L3_00_E26    ;Q22 bus master cycle control machine

input   nci15, -cd0, -cd1, -bm0, -bm1, -bm2, -bm3, uVWR
input   valid, nci6, t_o, rref, srply, -grant, -qbiocyc, qale

output  nco7, -EnbDal, -EnbData, -tdio, nco3, tiako, tsync, -done

local   first

machine q_bus_master

state A, number -hhhhh
if [-grant] then B [first, -EnbDal, -EnbData, -done, -tdio, -tiako, -tsync]

state B, number -hhlhl
if [grant * qale * -(-cd1)] then P [EnbDal]
if [grant * qale * (-cd1 * -cd0)]  then T
if [grant * qale * (-cd1 * cd0)] then C [tdio, -first]

state C, number -hllhl
goto D

state D, number -lllhl
gotc E

state E, number -hllhh
goto F

state F, number -lllhh
goto H

state H, number -lhlhh
goto J  [tiako]

state J, number -lhhll
goto V

state K, number -lhllh
goto L

state L, number -hhlll
goto M

state M, number -lhlhl
goto N  [-EnbData, -tdio, -first]

state N, number -lhlll
if      [-srply] then P [EnbDal, -tsync]

state P, number -hlhhl
goto R

state R, number -llhhl
goto S

state S, number -hlhhh
goto T

state T, number -llhhh
if      [qale * (-cd0 + (valid * qbiocyc))] &
    then AP     [done]
if      [qale *  cd0 * (-valid + qbiocyc)] &
    then U      [tsync]
if      [qale * cd0 * valid * -qbiocyc * -first] then [-tsync]
if      [qale * cd0 * valid * -qbiocyc *  first] then [ tsync, -first]

state U, number -hlhll
goto V

state V, number -llhll
if      [uVWR] then AB [EnbData]
if      [-uVWR] then AJ [tdio, -EnbDal]

state AJ, number -hhllh
if      [t_o + srply] then AK

state AK, number -hlllh
goto AL

state AL, number -llllh
goto AM
if [-t_o] then [EnbData]

state AM, number -hllll
if      [-t_o * -uVWR * (bm2*bm1) * first * -rref] then N &
                        [-EnbData, -tdio, -tiako, -first]
if      [t_o + uVWR + -(bm2*bm1) + -first + rref] then AN &
                        [-EnbData, -tdio, -tiako]

state AN, number -lllll
if      [-srply * -t_o * first * (bm2*bm1) * -uVWR] &
    then V [-first]
if      [-srply * -t_o * first * (Lm2*bm1) * uVWR] &
    then AB [-first, EnbData]
if      [-srply * (t_o + -(bm2*bm1) + -first)] &
    then AP [-tsync, done, -EnbDal]

state AP, number -hhlhh
if      [grant * -qbiocyc * -qale] then S
if      [-grant + qbiocyc + qale] then A

state AB, number -hhhll
goto AC

state AC, number -lhhhl
goto AD

state AD, number -hhhhl
goto AE [tdio]

state AE, number -hhhlh
if      [t_o + srply] then AF

state AF, number -hlhlh
if &
[-t_o * first * (bm2*bm1) * -((-uVWR + bm0 * bm3) * rref)] &
    then K      [-tdio]
if &
[t_o + -first + -(bm2*bm1) + rref * (-uVWR + bm0 * bm7)] &
    then AH     [-tdio]

state AH, number -llhlh
goto AL

END
```

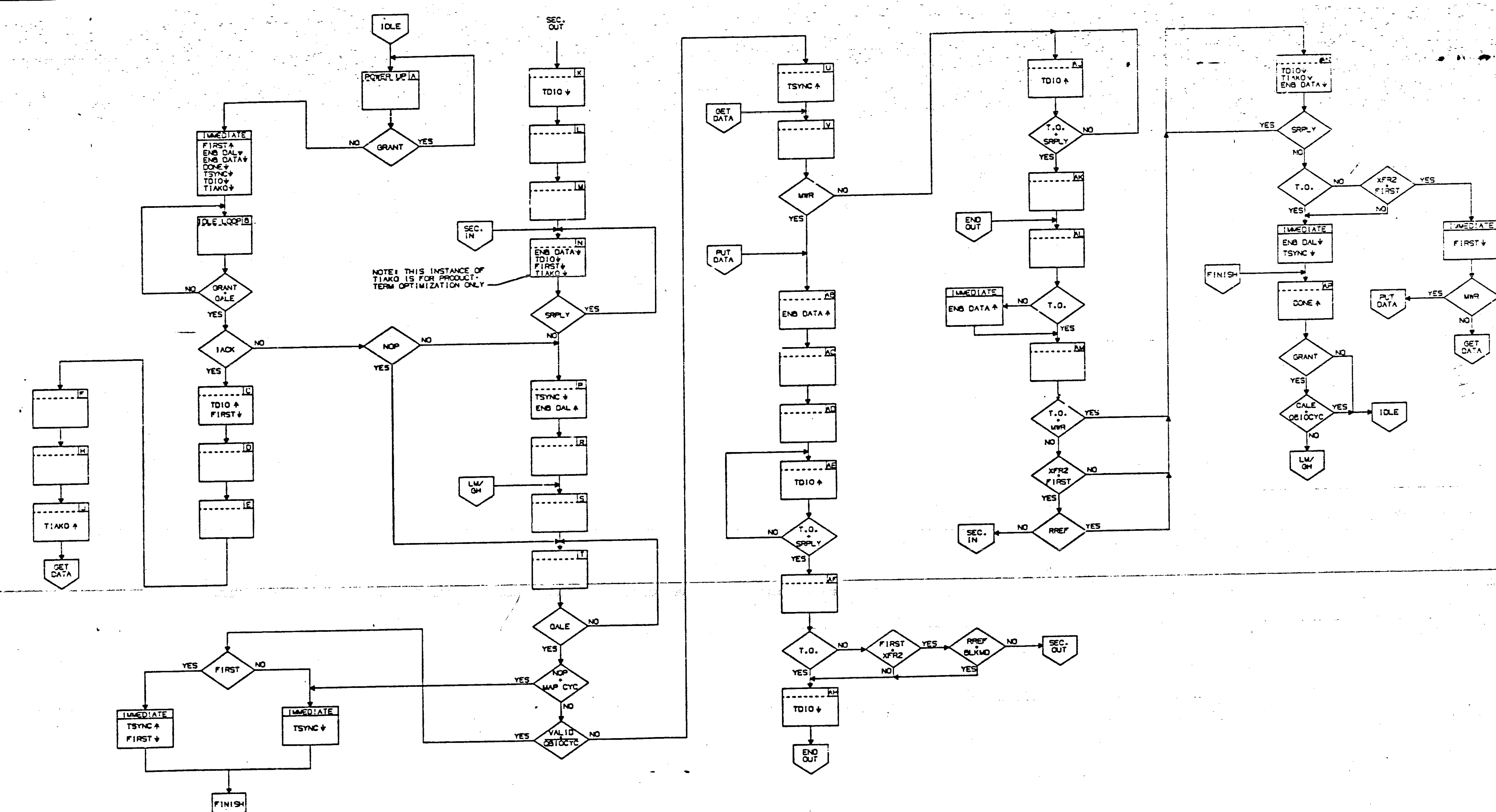

REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN.	DATE 09-AUG-85	ENG. R. MCNAMARA	DATE 09-AUG-85
CHK'D. R. MCNAMARA	DATE 09-AUG-85	BOARD LOCATION:	
		SHEET 1 OF 1	
DSK:6.T2P[4,550]	09-AUG-85 07:39	NEXT HIGHER ASSEMBLY:	
FIRST USED ON OPTION/MODEL:			

TITLE: Q22 BUS MASTER CTL MACHINE LISTING

SIZE	CODE	NUMBER	REV.
D	CS	M7606-0-58	A



Q22 BUS MASTER CONTROL MACHINE FLOW DIAGRAM

SIZE	CODE	NUMBER	REV
D	CS	M7606-0-59	B

SCALE 1/1 SHEET 1 OF 1

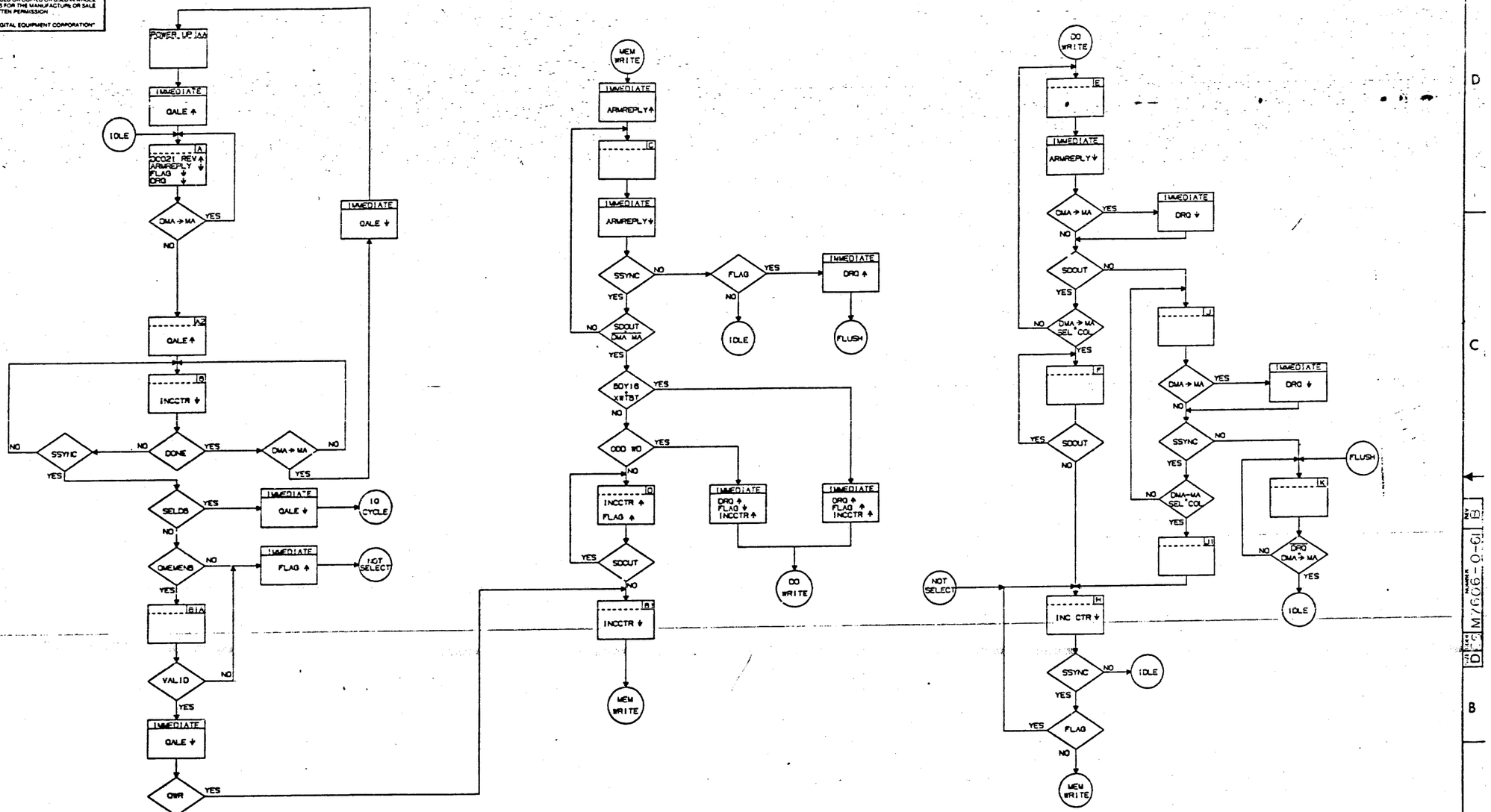
```
name 2?_010L3_00_E33    ;Q22 bus slave cycle control machine

input   -drq, -dmaMA, selcol, -bdy16, oddwd, -sel_db, qwr, -QMemEnb
input   valid, nci6, xwtbt, rbs7, sdout, sdin, ssync, -done

output  nco7, DC021rcv, nco5, qale, nco3, incctr, -armreply, -drq

local flag

machine q_bus_slave

state AA, number -hhhhh
goto A [DC021rcv, -drq, qale, -armreply, -flag]

state A, number -11111
if [-dmaMA] then A2 [qale]


state A2, number -lh111
goto B [-incctr]


state B1, number -lhh11
goto C [armreply]

state C, number -11h11
always [-armreply]
if [-ssync * flag] then K [drq]
if [-ssync * -flag] then A &
        [DC021rcv, -armreply, -flag, -drq]
if [ssync * sdout * -dmaMA * -xwtbt * -bdy16 * -oddwd] then D [incctr, flag]
if [ssync * sdout * -dmaMA * (xwtbt + bdy16)] then E [drq, flag, incctr]
if [ssync * sdout * -dmaMA * -xwtbt * -bdy16 * oddwd] then E &
        [drq, -flag, incctr]

state D
if [-sdout] then B1 [-incctr]

state E, number -11h1h
always [-armreply]
if [dmaMA] then [-drq]
if [-sdout] then J
if [sdout * dmaMA * selcol] then F

state F
if [-sdout] then H [-incctr]

state H, number -h1hh1
if [-ssync] then A [DC021rcv, -armreply, -flag, -drq]
if [ssync * -flag] then C [armreply]

state J, number -h111h
if [dmaMA] then [-drq]
if [-ssync] then K
if [ssync * dmaMA * selcol] then J1

state J1, number -hh11h
goto H [-incctr]

state K, number -1111h
if [dmaMA + -drq] then A [DC021rcv, -armreply, -flag, -drq]

state L1, number -1hhhh
got? M [armreply]

state M, number -11hhh
always [-armreply]
if [-sdin * -sdout] then N [DC021rcv]

state N, number -111h1
if [-ssync] then A [DC021rcv, -armreply, -flag, -drq]
if [ssync * sdin * -flag] then L1 [-DC021rcv, flag]
if [ssync * -(sdin * -flag) * sdout] then M [armreply, flag]

state P, number -h1111
if [dmaMA] then [-drq]
if [-ssync] then K
if [ssync * dmaMA * selcol] then R

state R, number -hh111
goto R1 [-incctr]

state R1, number -hh1h1
goto R2 [-DC021rcv]

state R2, number -1hhh1
goto S [armreply]

state S, number -11hh1
always [-armreply]
if [-ssync] then A [DC021rcv, -armreply, -flag, -drq]
if [ssync * sdin * bdy16] then U
if [ssync * sdin * -bdy16] then T [incctr]

state T
if [-sdin * -rbs7] then V &
        [-incctr, DC021rcv, qale]
if [-sdin * rbs7 * oddwd] then  S &
        [-incctr, armreply]
if [-sdin * rbs7 * -oddwd] then P &
        [-incctr, DC021rcv, drq]

state U
if [-sdin] then V [DC021rcv, qale]

state V, number -h11h1
if [-ssync] then A [DC021rcv, -armreply, -flag, -drq]
if [ssync * sdout] then V1 [-qale]

state V1, number -1hh1h
goto E [armreply, flag, drq]

state B, number -1h1h1
if [-done * ssync * -sel_db *  QMemEnb] then B1A
if [-done * ssync * -sel_db * -QMemEnb] then H [flag, -incctr]
if [-done * ssync * sel_db] then N [-qale, DC021rcv]
if [done * dmaMa] then AA [-qale]

state B1A
if [-valid] then H [flag, -incctr]
if [valid *  -qwr] then P  [ -qale, drq]
if [valid *   qwr] then B1 [ -qale, -incctr]

END
```


REVISIONS		
CHK	CHANGE NO.	REV

digital	DRN. [signature]	DATE 09-AUG-85	ENG. R. MCNAMARA	DATE 09-AUG-85
	CHK'D. R. MCNAMARA	DATE 09-AUG-85	BOARD LOCATION:	
			SHEET 1 OF 1	
DSK:7.T2?[4,550]	09-AUG-85 07:39		NEXT HIGHER ASSEMBLY:	
FIRST USED ON OPTION/MODEL:				

TITLE: Q22 BUS SLAVE CTL MACHINE LISTING

SIZE	CODE	NUMBER	REV.
D	CS	M7606-0-60	A



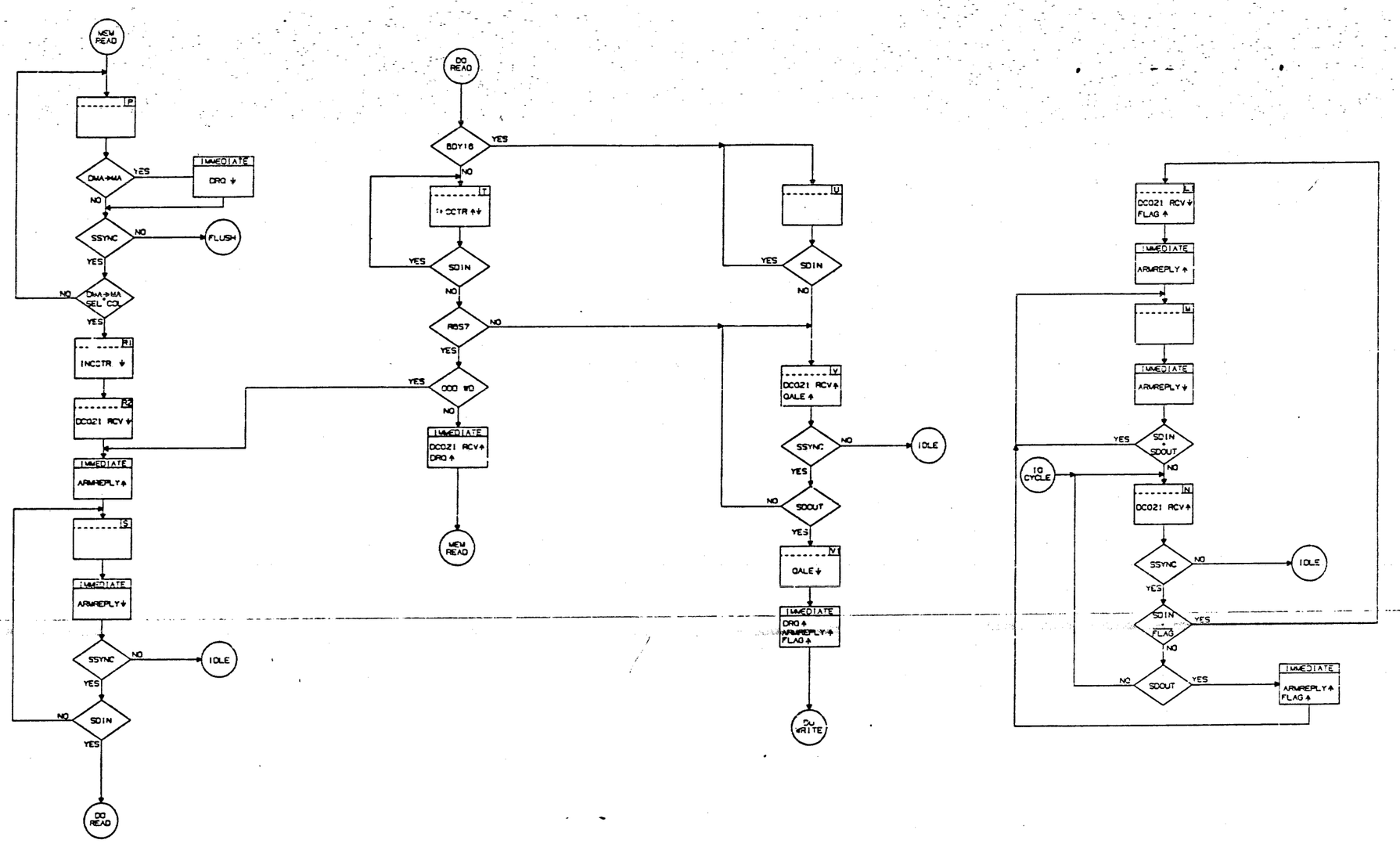
REVISION HISTORY		
DATE	ECO NUMBER	REV
[illegible]	[illegible]	B

TITLE: Q22 BUS SLAVE CONTROL MACHINE FLOW DIAGRAM

DOCUMENT NUMBER: DCS M7606-0-01 REV B

SIZE: D CODE: DCS NUMBER: M7606-0-01 REV: B

SCALE: 1:1 SHEET 1 OF 1



REVISION HISTORY		
DATE	ECO NUMBER	REV

TITLE	Q22 BUS SLAVE CONTROL MACHINE FLOW DIAGRAM
SIZE	D
CODE	DCS
NUMBER	M7606-0-52
REV	B
SCALE	1
SHEET	1 OF 1

M7606-0-52 REV B

DEC PART NUMBER: 23-E42F1-00 KA630 -A, -B 1MB RAS DECODE PROM (E79)
DATE ORIGINATED: 10-September-1984

HEX LOC	HEX DATA	HEX LOC	HEX DATA	HEX LOC	HEX DATA	HEX LOC	HEX DATA	HEX LOC	HEX DATA	HEX LOC	HEX DATA	HEX LOC	HEX DATA	HEX LOC	HEX DATA	HEX LOC	HEX DATA	HEX LOC	HEX DATA	HEX LOC	HEX DATA	HEX LOC	HEX DATA	HEX LOC	HEX DATA	HEX LOC	HEX DATA	HEX LOC	HEX DATA	HEX LOC	HEX DATA	HEX LOC	HEX DATA
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001	9	03E	8	07B	9	0B8	8	0F5	9	132	9	16F	9	1AC	9	1E9	9	226	9	263	9	2A0	9	2DD	9	31A	9	357	9	394	9	3D1	9
002	9	03F	9	07C	7	0B9	9	0F6	9	133	9	170	9	1AD	9	1EA	1	227	9	264	9	2A1	9	2DE	9	31B	9	358	9	395	9	3D2	9
003	4	040	9	07D	9	0BA	9	0F7	9	134	9	171	9	1AE	9	1EB	9	228	9	265	9	2A2	9	2DF	9	31C	9	359	9	396	9	3D3	9
004	9	041	9	07E	9	0BB	9	0F8	9	135	9	172	9	1AF	9	1EC	9	229	9	266	9	2A3	9	2E0	9	31D	9	35A	9	397	9	3D4	9
005	9	042	9	07F	9	0BC	9	0F9	9	136	9	173	9	1B0	9	1ED	9	22A	9	267	9	2A4	9	2E1	9	31E	9	35B	9	398	9	3D5	9
006	9	043	4	080	9	0BD	9	0FA	9	137	9	174	9	1B1	9	1EE	9	22B	9	268	9	2A5	9	2E2	9	31F	9	35C	9	399	9	3D6	9
007	4	044	9	081	9	0BE	9	0FB	9	138	9	175	9	1B2	9	1EF	9	22C	9	269	9	2A6	9	2E3	9	320	9	35D	9	39A	9	3D7	9
008	9	045	9	082	9	0BF	9	0FC	9	139	9	176	9	1B3	9	1F0	9	22D	9	26A	9	2A7	9	2E4	9	321	9	35E	9	39B	9	3D8	9
009	9	046	9	083	5	0C0	9	0FD	9	13A	9	177	9	1B4	9	1F1	9	22E	9	26B	9	2A8	9	2E5	9	322	9	35F	9	39C	9	3D9	9
00A	4	047	4	084	9	0C1	9	0FE	9	13B	9	178	9	1B5	9	1F2	9	22F	9	26C	9	2A9	9	2E6	9	323	9	360	9	39D	9	3DA	9
00B	4	048	9	085	9	0C2	9	0FF	9	13C	9	179	9	1B6	9	1F3	9	230	9	26D	9	2AA	9	2E7	9	324	9	361	9	39E	9	3DB	9
00C	4	049	9	086	9	0C3	5	100	9	13D	9	17A	9	1B7	9	1F4	9	231	9	26E	9	2AB	9	2E8	9	325	9	362	9	39F	9	3DC	9
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00F	4	04C	6	089	9	0C6	9	103	0	140	9	17D	9	1BA	9	1F7	9	234	9	271	9	2AE	9	2EB	9	328	9	365	9	3A2	9	3DF	9
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013	9	050	6	08D	0	0CA	5	107	0	144	9	181	9	1BE	9	1FB	9	238	9	275	9	2B2	9	2EF	9	32C	9	369	9	3A6	9	3E3	9
014	4	051	0	08E	0	0CB	5	108	9	145	9	182	9	1BF	9	1FC	9	239	9	276	9	2B3	9	2F0	9	32D	9	36A	9	3A7	9	3E4	9
015	4	052	1	08F	5	0CC	0	109	9	146	9	183	8	1C0	9	1FD	9	23A	9	277	9	2B4	9	2F1	9	32E	9	36B	9	3A8	9	3E5	9
016	4	053	9	090	0	0CD	1	10A	0	147	8	184	9	1C1	9	1FE	9	23B	9	278	9	2B5	9	2F2	9	32F	9	36C	9	3A9	9	3E6	9
017	9	054	6	091	2	0CE	1	10B	0	148	9	185	9	1C2	9	1FF	9	23C	9	279	9	2B6	9	2F3	9	330	9	36D	9	3AA	9	3E7	9
018	4	055	0	092	3	0CF	5	10C	1	149	9	186	9	1C3	9	200	9	23D	9	27A	9	2B7	9	2F4	9	331	9	36E	9	3AB	9	3E8	9
019	4	056	1	093	9	0D0	2	10D	1	14A	0	187	9	1C4	9	201	9	23E	9	27B	9	2B8	9	2F5	9	332	9	36F	9	3AC	9	3E9	9
01A	4	057	9	094	0	0D1	8	10E	1	14B	9	188	9	1C5	9	202	9	23F	9	27C	9	2B9	9	2F6	9	333	9	370	9	3AD	9	3EA	9
01B	9	058	6	095	8	0D2	9	10F	8	14C	1	189	9	1C6	9	203	9	240	9	27D	9	2BA	9	2F7	9	334	9	371	9	3AE	9	3EB	9
01C	4	059	0	096	9	0D3	9	110	8	14D	8	18A	1	1C7	9	204	9	241	9	27E	9	2BB	9	2F8	9	335	9	372	9	3AF	9	3EC	9
01D	4	05A	8	097	9	0D4	8	111	9	14E	9	18B	9	1C8	9	205	9	242	9	27F	9	2BC	9	2F9	9	336	9	373	9	3B0	9	3ED	9
01E	4	05B	9	098	0	0D5	9	112	9	14F	9	18C	8	1C9	9	206	9	243	9	280	9	2BD	9	2FA	9	337	9	374	9	3B1	9	3EE	9
01F	8	05C	6	099	9	0D6	9	113	9	150	9	18D	9	1CA	1	207	9	244	9	281	9	2BE	9	2FB	9	338	9	375	9	3B2	9	3EF	9
020	9	05D	8	09A	9	0D7	9	114	9	151	9	18E	9	1CB	9	208	9	245	9	282	9	2BF	9	2FC	9	339	9	376	9	3B3	9	3F0	9
021	9	05E	9	09B	9	0D8	9	115	9	152	9	18F	9	1CC	9	209	9	246	9	283	9	2C0	9	2FD	9	33A	9	377	9	3B4	9	3F1	9
022	9	05F	9	09C	8	0D9	9	116	9	153	9	190	9	1CD	9	20A	9	247	9	284	9	2C1	9	2FE	9	33B	9	378	9	3B5	9	3F2	9
023	4	060	9	09D	9	0DA	9	117	9	154	9	191	9	1CE	9	20B	9	248	9	285	9	2C2	9	2FF	9	33C	9	379	9	3B6	9	3F3	9
024	9	061	9	09E	9	0DB	9	118	9	155	9	192	9	1CF	9	20C	9	249	9	286	9	2C3	9	300	9	33D	9	37A	9	3B7	9	3F4	9
025	9	062	9	09F	9	0DC	9	119	9	156	9	193	9	1D0	9	20D	9	24A	9	287	9	2C4	9	301	9	33E	9	37B	9	3B8	9	3F5	9
025	9	063	4	0A0	9	0DD	9	11A	9	157	9	194	9	1D1	9	20E	9	24B	9	288	9	2C5	9	302	9	33F	9	37C	9	3B9	9	3F6	9
027	4	064	9	0A1	9	0DE	9	11B	9	158	9	195	9	1D2	9	20F	9	24C	9	289	9	2C6	9	303	9	340	9	37D	9	3BA	9	3F7	9
028	9	065	9	0A2	9	0DF	9	11C	9	159	9	196	9	1D3	9	210	9	24D	9	28A	9	2C7	9	304	9	341	9	37E	9	3BB	9	3F8	9
029	9	066	9	0A3	5	0E0	9	11D	9	15A	9	197	9	1D4	9	211	9	24E	9	28B	9	2C8	9	305	9	342	9	37F	9	3BC	9	3F9	9
02A	4	067	4	0A4	9	0E1	9	11E	9	15B	9	198	9	1D5	9	212	9	24F	9	28C	9	2C9	9	306	9	343	9	380	9	3BD	9	3FA	9
02B	4	068	9	0A5	9	0E2	9	11F	9	15C	9	199	9	1D6	9	213	9	250	9	28D	9	2CA	9	307	9	344	9	381	9	3BE	9	3FB	9
02C	5	069	9	0A6	9	0E3	5	120	9	15D	9	19A	9	1D7	9	214	9	251	9	28E	9	2CB	9	308	9	345	9	382	9	3BF	9	3FC	9
02D	5	06A	4	0A7	5	0E4	9	121	9	15E	9	19B	9	1D8	9	215	9	252	9	28F	9	2CC	9	309	9	346	9	383	9	3C0	9	3FD	9
02E	0	06B	4	0A8	9	0E5	9	122	9	15F	9	19C	9	1D9	9	216	9	253	9	290	9	2CD	9	30A	9	347	9	384	9	3C1	9	3FE	9
02F	4	06C	7	0A9	9	0E6	9	123	1	160	9	19D	9	1DA	9	217	9	254	9	291	9	2CE	9	30B	9	348	9	385	9	3C2	9	3FF	9
030	5	06D	0	0AA	5	0E7	5	124	9	161	9	19E	9	1DB	9	218	9	255	9	292	9	2CF	9	30C	9	349	9	386	9	3C3	9		
031	5	06E	0	0AB	5	0E8	9	125	9	162	9	19F	9	1DC	9	219	9	256	9	293	9	2D0	9	30D	9	34A	9	387	9	3C4	9		
032	0	06F	4	0AC	0	0E9	9	126	9	163	3	1A0	9	1DD	9	21A	9	257	9	294	9	2D1	9	30E	9	34B	9	388	9	3C5	9		
033	9	070	7	0AD	0	0EA	5	127	1	164	9	1A1	9	1DE	9	21B	9	258	9	295	9	2D2	9	30F	9	34C	9	389	9	3C6	9		
034	5	071	1	0AE	1	0EB	5	128	9	165	9	1A2	9	1DF	9	21C	9	259	9	296	9	2D3	9	310	9	34D	9	38A	9	3C7	9		
035	5	072	2	0AF	5	0EC	0	129	9	166	9	1A3	9	1E0	9	21D	9	25A	9	297	9	2D4	9	311	9	34E	9	38B	9	3C8	9		
036	0	073	9	0B0	1	0ED	1	12A	0	167	9	1A4	9	1E1	9	21E	9	25B	9	298	9	2D5	9	312	9	34F	9	38C	9	3C9	9		
037	9	074	7	0B1	3	0EE	1	12B	8	168	9	1A5	9	1E2	9	21F	9	25C	9	299	9	2D6	9	313	9	350	9	38D	9	3CA	9		
038	5	075	1	0B2	8	0EF	5	12C	1	169	9	1A6	9	1E3	9	220	9	25D	9	29A	9	2D7	9	314	9	351	9	38E	9	3CB	9		
039	5	076	8	0B3	9	0F0	3	12D	1	16A	0	1A7	9	1E4	9	221	9	25E	9	29B	9	2D8	9	315	9	352	9	38F	9	3CC	9		
03A	0	077	9	0B4	1	0F1	9	12E	8	16B	9	1A8	9	1E5	9	222	9	25F	9	29C	9	2D9	9	316	9	353	9	390	9	3CD	9		
03B	9	078	7	0B5	9	0F2	9	12F	9	16C	1	1A9	9	1E6	9	223	9	260	9	29D	9	2DA	9	317	9	354	9	391	9	3CE	9		
03C	5	079	8	0B6	9	0F3	9	130	9	16D	9	1AA	1	1E7	9	224	9	261	9	29E	9	2DB	9	318	9	355	9	392	9	3CF	9		

REVISIONS: CHK | CHANGE NO. | REV

digital | DRN. | CHK'D. R. MCNAMARA | DATE 09-AUG-85 | ENG. R. MCNAMARA | DATE 09-AUG-85 | BOARD LOCATION: | SHEET 1 OF 1 | NEXT HIGHER ASSEMBLY:

DSK:4.T2P(4,550] 09-AUG-85 07:39

FIRST USED ON OPTION/MODEL:

TITLE: 1KX4 RAS DECODE PROM (E79) LISTING

SIZE D | CODE CS | NUMBER M7606-0-63 | REV. A

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T:      PAL16L8A
P:      23-169J5-00  E40
N:      BARRY MASKAS
D:      25 OCT 1984
S:      /RPOK /BTRYOK CSMAPEMEAR /EPAS EPDS UVWR /DONE QALE /GRANT
        GND SRPLY /CLRPSH /ENBLS646 /WRMAP /ENBBDAL RDIN DC021RCV /TDIO
        /RCVBDALH VCC
B:      IF [VCC] CLRPSH = RPOK + BTRYOK
        IF [VCC] ENBLS646 = CSMAPEMEAR * EPAS
        IF [VCC] WRMAP = CSMAPEMEAR * UVWR * EPDS
        IF [VCC] ENBBDAL  = /GRANT * /RDIN * /DONE +
        GRANT * /DONE * QALE + /DC021RCV * /GRANT * /DONE
        IF [VCC] RCVBDALH = /TDIO * /DC021RCV + /TDIO * GRANT +
        /SRPLY * /DC021RCV + /SRPLY * GRANT + UVWR * /DC021RCV +
        UVWR * GRANT
E:      KA630-A, -B, -C, -D (M7606) MISC. CONTROL STROBES

T:      PAL16L8A
P:      23-170J5-00  E78
N:      BARRY MASKAS
D:      25 OCT 1984
S:      /PE3 /PE2 /PE1 /PE0 /MSER0 /MEMWR /BYTACT3 /BYTACT2 /BYTACT1
        GND /BYTACT0 /HI16PER /LO16PER /PERR /SELCOL /ENBCAS0H /ENBCAS1H
        /ENBCAS2H /ENBCAS3H VCC
B:      IF [VCC] HI16PER = MSER0 * PE2 * BYTACT2 + MSER0 * PE3 * BYTACT3
        IF [VCC] LO16PER = MSER0 * PE0 * BYTACT0 + MSER0 * PE1 * BYTACT1
        IF [VCC] PERR = MSER0 * /MEMWR * PE0 * BYTACT0 + MSER0 * /MEMWR *
        PE1 * BYTACT1 + MSER0 * /MEMWR * PE2 * BYTACT2 + MSER0 * /MEMWR *
        PE3 * BYTACT3
        IF [VCC] ENBCAS0H = /SELCOL + /BYTACT0
        IF [VCC] ENBCAS1H = /SELCOL + /BYTACT1
        IF [VCC] ENBCAS2H = /SELCOL + /BYTACT2
        IF [VCC] ENBCAS3H = /SELCOL + /BYTACT3
E:      KA630-A, -B, -C, -D (M7606) MEMORY SYSTEM CAS CONTROL STROBES AND
E:      PARITY ERROR DETECTION STROBES

T:      PAL16L8A
P:      23-171J5-00  E86
N:      BARRY MASKAS
D:      25 OCT 1984
S:      /UVCYCCD2 /DMAMA /DONE /MSER1 /UVCYC /MEMWR DECODE /DATABUFENB
        MEMCD0 GND MEMCD1 /MSWT0H /MSWT1H SELCOL /BUFENB /BUFENB0 /BUFENB1
        /BDIRT /STARTCYC VCC
B:      IF [VCC] MSWT0H = /MEMCD1 + MEMCD0 + /MEMWR + /UVCYC
        IF [VCC] MSWT1H = MEMCD1 + /MEMWR + /UVCYC
        IF [VCC] BUFENB = MEMCD1 * /MEMCD0 * /MEMWR * SELCOL * /DMAMA +
        MEMCD1 * /MEMCD0 * /MEMWR * DATABUFENB + MEMCD1 * /MEMCD0 * MEMWR *
        UVCYC * MSER1
        IF [VCC] BUFENB0 = /MEMCD1 * MEMCD0 * /MEMWR * SELCOL * /DMAMA +
        /MEMCD1 * MEMCD0 * /MEMWR * DATABUFENB + /MEMCD1 *
        MEMCD0 * MEMWR * UVCYC * MSER1
        IF [VCC] BUFENB1 = /MEMCD1 * /MEMCD0 * /MEMWR * SELCOL * /DMAMA +
        /MEMCD1 * /MEMCD0 * /MEMWR * DATABUFENB + /MEMCD1 *
        /MEMCD0 * MEMWR * UVCYC * MSER1
        IF [VCC] BDIRT = MEMWR * DECODE + MEMWR * SELCOL * MSER1
        IF [VCC] STARTCYC = /DMAMA * UVCYCCD2 * UVCYC * /MEMWR +
        /DMAMA * DECODE * /UVCYCCD2 * UVCYC * /MEMWR * DONE + /DMAMA * UVCYC *
        MEMWR + DMAMA * DECODE + DMAMA * SELCOL
E:      KA630-A, -B, -C, -D (M7606) MEMORY SUBSYSTEM BUFFER CONTROL STROBES
E:      AND MEMORY CYCLE ENABLE STROBE
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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. [signature]	DATE 09-AUG-85	ENG. R. MCNAMARA	DATE 09-AUG-85	TITLE: PALASM LISTINGS FOR PAL16L8A DEVICES	
CHK'D. R. MCNAMARA	DATE 09-AUG-85	BOARD LOCATION:			
		SHEET 1 OF 1			
DSK:3.T2P(4,550)	09-AUG-85 07:39	NEXT HIGHER ASSEMBLY:		SIZE D / CODE CS / NUMBER M7606-0-64	REV. A
FIRST USED ON OPTION/MODEL:					

+12.0V	raw +12 volts
+3VA	logic "high" voltage
+5.0V	raw +5 volts
-12.0V	charge pump generated -12 volts
ARB(L)	asserted if module is bus arbiter
ARM REPLY(L)	sets ENBREPLY (inside Qbus gate array)
ARM UVDAL(L)	asserted to enable the uVDAL (-> MD transceivers
ARMRDYERR(L)	indicates that memory arbiter is READY to finish a cycle
ASYNC T.O.(H)	Q-bus timeout
AUX HLT(H)	auxiliary processor halt
BBS7(L)	Qbus BS7 (selects I/O page, used in block mode handshake)
BDAL(21:0)L	Qbus data/address lines
BDCOK(H)	Qbus DCOK signal (indicates DC power at proper level)
BDG CD(1:0)L	firmware mode select from configuration connector to BDR
BDIN(L)	Qbus DIN control signal
BDIRT(L)	dram buffer direction transmit enable
BDMGI(L)	Qbus DMGI (DMA grant in)
BDMGO(L)	Qbus DMGO (DMA grant out)
BDMR(L)	Qbus DMR (DMA request)
BDOUT(L)	Qbus DOUT control signal
BDR(3:0)L	boot and diagnostic register LED controls
BDY16(L)	indicates address is at a 16 word boundary
BEVENT(L)	Qbus EVENT signal (terminated but not used)
BHALT(L)	Qbus HALT signal
BIAKI(L)	Qbus IAKI (interrupt acknowledge in)
BIAKO(L)	Qbus IAKO (interrupt acknowledge out)
BINIT(L)	Qbus INIT signal (clobbers/inits everybody on bus)
BIRQ(7:4)L	Qbus IRQ lines (interrupt requests)
BMAA(8:0)H	buffered and damped local dram array address signals
BMCAS(3:0)H	byte active controlled unbuffered column address strobes
BMSWT(0)L	buffered and damped local dram array write signal
BPOK(H)	Qbus POK signal (indicates sufficient power for operation)
BREAK(H)	serial line break indication from DLART
BREF(L)	Qbus REF signal (used in block mode handshake)
BRPLY(L)	Qbus RPLY control signal (reply)
BRS(2:0)L	bit rate selection (from back panel into DLART)
BSACK(L)	Qbus SACK control signal (bus acknowledge)
BSYNC(L)	Qbus SYNC control signal (strobes address, frames transactions)
BTRY OK(L)	indicates battery voltage above minimum threshold
BTRYV(H)	raw battery voltage from back panel
BTRYV1(H)	battery or system voltage supply to watch/ram (TOY) chip
BTVREF(H)	battery supplied reference voltage (used to detect the battery)
BUF ENB(L)	local dram array data transceiver receive direction enable
BUF ENB(1:0)L	expansion dram array data transceiver receive direction enable
BUVAS(H)	buffered uVAX address strobe
BUVAS(L)	buffered uVAX address strobe
BUVCLK0(H)	buffered uVAX clock out
BUVRESET(H)	buffered uVAX reset
BUVRESET(L)	buffered uVAX reset
BWTBT(L)	Qbus WTBT signal (indicates write cycle, and byte write)
BYTACT(3:0)L	byte active bits to mem sequencer
CAS(3:0)L	buffered and damped local dram array column address strobes
CLK 614.4KHZ(H)	clock from 614.4KHz oscillator
CLK 614.4KHZ(L)	clock from 614.4KHz oscillator
CLK031(H)	clock from 32KHz oscillator (31us period)
CLK25(H)	clock from 40MHz oscillator (25ns period)
CLR PS(H)	clear power sense in TOY clock
CONF(3:2)L	configuration connector buffered inputs (see table on 1.10)
CS DL(L)	chip select for DLART
CS MAP(L)	chip select for MAP

CS MAP;EMEAR(H)	chip select for MAP or EMEAR (external mem. err. addr. reg.)
CS PROM(L)	chip select for PROM
CS TOY(H)	chip select for TOY
CTL XDAL(1:0)H	address function bits (see table on 1.7)
DATA BUF ENB(L)	qbus slave memory cycle
DC021RCV(H)	controls direction of DC021 during slave mode transactions
DECODE(H)	allows memory sequencer to decode and RAS memory
DLAD(1:0)H	the two lo-order address lines for the DLART
DLRD(L)	read signal for DLART
DLRRQ(H)	receiver interrupt from DLART
DLSI(H)	serial data in (to DLART)
DLSO(H)	serial data out (from DLART)
DLWR(L)	write signal for DLART
DLXRQ(H)	transmitter interrupt from DLART
DMA->MA(L)	"DMA acknowledge" from main memory state machine
DOK(H)	delayed indication of DC power at proper level
DONE(L)	indicates that requested transaction is completed
DRDCOK(H)	delayed indication of DC power at proper level
DRQ(L)	DMA request to main memory state machine
ENB 8641(L)	enable for Qbus drivers (for disabling drivers at power up)
ENB BDAL(L)	output enable for DC021 xcvr's
ENB CAS(3:0)H	select column and byte active controlled column address strobe enables
ENB DAL(L)	enable data/address onto Q-bus
ENB DATA(L)	mux'd output; enables data onto Q-bus (write), or strobes data in from Q-bus (read)
ENB LS646(L)	output enable control strobe for EPR (-> XLAT AD transceivers
EPAD ENB(L)	external processor bus (local I/O bus) address enable
EPAC(1)H	firmware proms LSB address control
EPAS(L)	external processor bus (local I/O bus) address strobe
EPDS(H)	external processor bus (local I/O bus) data strobe
EPR(15:0)H	external processor bus (local I/O bus) address/data bus
EPREADY(L)	auxiliary machine arm for DC379 READY or uVERR logic
FORCEINIT(H)	assertion forces arbitration machine to reset and assert TINIT
FSTRDY(H)	low 16 mega-byte normal (fast) uVAX ready strobe
GRANT(L)	Q-bus grant sent to Q-bus Master state machine
HI16PER(L)	high word parity error from memory sequencer
HIROMDLATCH(L)	signals uVAX intfce gate array to latch hi-order rom data
HLT ENB(L)	configuration connector buffered halt enable mask and BDR flag
INC CTR(H)	increments block mode address counter
INITRQ(L)	init request from uVAX's bus init register
INTRVL TIM(L)	interval timer 10mS
IRQ(7:5)L	uVAX interrupt request inputs for processor levels 17, 16, 15
LO16MB(L)	indicates address is in low 16 MB of 30 bit address space
LO16PER(L)	low word parity error from memory sequencer
LOCAL NXM(H)	low 16 meag-byte non-existent physical memory flag
LOCK(L)	asserted if uVAX is doing "read lock/write unlock"
LPD(3:0)H	local dram array transceiver generated byte parity data bits
LRD(31:0)H	local dram array transceiver data bits
LPERR(L)	local low 16 mega-byte dram parity error strobe
MA(23:2)H	memory address bus
MAA(9:0)L	row/column multiplexed memory address bus
MAP AD(21:9)H	RDAL bits 21:9 latched for translation map
MAP DISABLE(H)	scatter/gather map ram output enable control
MBMAA(8:0)H	local dram array buffered address signals
MBMSWT(0)L	local dram array buffered write strobe
MCAS(3:0)L	local dram array buffered column address strobes
MD(31:0)H	32 bit memory data bus
MEM CD(1:0)H	memory array selection codes (see 2.1.2)
MEMWR(L)	indicates a write to memory

REVISIONS		
CHK	CHANGE NO.	REV

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DRN. [signature] DATE 09-AUG-85 | ENG. R. MCNAMARA DATE 09-AUG-85
CHK'D R. MCNAMARA DATE 09-AUG-85 | BOARD LOCATION:
DSK:1.T2P(4,550) 09-AUG-85 07:38 | SHEET 1 OF 2
FIRST USED ON OPTION/MODEL: | NEXT HIGHER ASSEMBLY:

TITLE: MNEMONIC DICTIONARY

SIZE	CODE	NUMBER	REV.
D	CS	M7606-0-65	A

SIZE	CODE	NUMBER	REV.
D	CS	M7606-0-65	A

MRAS<81:80>L	local dram array buffered row address strobes
MSER<1:0>L	memory system error register write wrong parity and parity trap enable controls
MSID<4:0>L	expansion memory identification codes
MSWT<1:0>H	expansion memory write control strobes
ODD WD<H)	indicates an odd word address
OSC031<H)	watch/ram (TOY chip) clock input (31us)
PD<3:2>H	local dram array parity data
LPD<3:0>H	local dram array dampened parity data
PE<3:0>L	dram array transceiver (wire-ored) byte parity error strobes
PERR<L)	local dram array byte active and select column controlled parity error strobe
PF<L)	power failure strobe
QALE<H)	Q-bus address latch enable (also indicates "slave idle")
QBIOCYC<L)	uVAX is addressing Q-bus I/O space (not memory)
QMEMENB<L)	enables Q-bus access to local memory
QRQ<L)	Q-bus request from uVAX
QWR<H)	WTBT input from Q-bus (latched at assertion of SYNC)
RAS ALL<H)	generates RAS for all memory banks during refresh
RAS DECODE<L)	row address strobe decoder enable
RAS<81:80>L	buffered and damped local dram array row address strobes
RAS<8:0>h	nine row address strobes for the nine possible banks of dram
RBS7<H)	BS7 input from Q-bus
RCV BDAL<H)	controls the direction of the DC021 xcvr's
RD<31:16>h	undampened local dram array data transceiver data lines
RDCOK<L)	indicates DC power at proper level
RDIN<H)	DIN from the Q-bus
RDMGI<H)	DMGI from the Q-bus
RDMR<H)	DMR from the Q-bus
RDOUT<H)	DOUT from the Q-bus
READY<H)	DC379 generated uVAX ready strobe, armed by EPREADY
REF REQ<H)	indicates a refresh cycle needed
REF->MA<L)	clears a refresh request & enables ref adrs onto MA
RHALT<H)	HALT from the Q-bus
RIAK<H)	IAKI from the Q-bus
RINIT<H)	INIT from the Q-bus
RIRQ<7:4>H	IRQ's from the Q-bus
RPOK<L)	POK from the Q-bus
RR<H)	sync'd refresh request (to memory arbiter)
RREF<H)	REF from the Q-bus
RRPLY<H)	RPLY from the Q-bus
RSACK<H)	SACK from the Q-bus
RSYNC<H)	SYNC input from Q-bus
RSYNC<L)	inverted SYNC for latching XDAL's for scatter/gather map
RUN<L)	exited halt protected prom and prefetching and dram refreshing status flag
SDIN<H)	sync'd DIN from the Q-bus
SDMGI<H)	sync'd DMGI from the Q-bus
SDMR<H)	sync'd DMR from the Q-bus
SDOUT<H)	sync'd DOUT from the Q-bus
SEL DB<L)	Q-bus doorbell select
SEL LO16MB<L)	dynamic low 16 mega-byte address comparitor output
SELCOL<H)	RAM timing signal (indicates existing memory)
SELCOL<L)	RAM timing signal (indicates existing memory)
SG1<L)	soft ground (for use by board testers)
SG4<L)	soft ground (for use by board testers)
SI<H)	terminated eia serial in +
SI<L)	terminated eia serial in -
SRPLY<H)	sync'd RPLY input from Q-bus
SRUN<L)	goes to "RUN" light on front panel

SSACK<H)	sync'd SACK input from Q-bus
SSYNC<H)	sync'd SYNC input from Q-bus
START CYC<L)	select column control for lock or non-existent memory cycles
SYSCLK<H)	unbuffered system clock used to drive uVAX and FPU
T.O.<H)	sync'd 10 usec. timeout
TBS7<H)	BS7 output to Q-bus
TDIO<L)	TDIN or TDOUT control from Q-bus master state machine
TDMGO<H)	DMGO output to Q-bus
TDMR<H)	DMR output to Q-bus
TIAK0<H)	IAKO output to Q-bus
TINIT<H)	INIT output to Q-bus (externally gated by ARB)
TREF<H)	REF output to Q-bus
TRPLY<H)	TRPLY output to Q-bus
TS<1:0>H	"t-state" counter outputs (sync'd to uVAX ucycle at power up)
TS<1>L	"t-state" grey code counter inverted feedback next state control
TSACK<H)	SACK output to Q-bus
TSYNC<H)	SYNC output to Q-bus
UVAS<L)	uVAX address strobe
UVBM<3:0>L	byte mask bits from uvax
UVBR<14>L	bus interrupt request input for processor level 14
UVCLKO<H)	unbuffered uVAX clock out
UVCS<2:0>H	uVAX cycle status strobes (see table on 1.1)
UVCYC<L)	low 16 mega-byte dram cycle started flag (enables select column strobe)
UVCYCCD<2:0>L	uVAX cycle codes (see table on 1.7)
UVDAL->MA<L)	enables uVAX latched addresses onto MA bus
UVDAL<31:0>H	uVAX data/address lines
UVDBE<L)	uVAX data buffer enable strobe
UVDS<L)	uVAX data strobe
UVEPS<L)	uVAX external processor strobe
UVERR<L)	uVAX error (forces abnormal termination of cycle)
UVHALT<L)	uVAX halt
UVRDY<L)	uVAX ready control input
UVRESET<L)	uVAX reset control signal
UVWR<H)	buffered uVAX write signal
UVWR<L)	uVAX write signal
V1.2REF<H)	1.2 volt reference in battery sense circuit
V4.3REF<H)	4.3 volt regulator in charge pump circuit
VALID<H)	valid bit from "scatter-gather" map
WR MAP<L)	write control signal for map
XDAL<21:0>H	address/data in/out from Q-bus
XDBI RQ<H)	doorbell interrupt request
XDMA QPE<H)	Q-bus parity error on a Q-bus read cycle
XLAT AD<23:9>H	translated addresses out of scatter/gather map
XWTBT<H)	WTBT input from Q-bus

REVISIONS		
CHK	CHANGE NO.	REV

DRN. [signature] DATE 09-AUG-85 | ENG. R. MCNAMARA DATE 09-AUG-85 | CHK'D. R. MCNAMARA DATE 09-AUG-85 | BOARD LOCATION: | SHEET 2 OF 2

DSK:I2.T2P(4,550) 09-AUG-85 07:38 | NEXT HIGHER ASSEMBLY: | FIRST USED ON OPTION/MODEL:

TITLE: MNEMONIC DICTIONARY

SIZE	CODE	NUMBER	REV.
D	CS	M7606-0-65	A

SIZE	CODE	NUMBER	REV
B	DD	5416744-0-0	B

DRAWING NO.	NO OF SHTS.	PART NO.	DESCRIPTION	REVISIONS																	
		5416744-01	FUNCTION SEL/SLU BOARD	A1	A1																
D-UA-5416744-0-0	1		FUNCTION SEL/SLU UNIT ASSEMBLY	A	B																
K-CS-5416744-0-1	1		FUNCTION SEL/SLU CIRCUIT SCHEMATIC	A	A																
K-PL-5416744-0-DBP	1		FUNCTION SEL/SLU PARTS LIST	A	A																
K-PC-5416744-0-DBJ			P.C. DESIGN DATA BASE	A	A																
		5016743-01	ETCHED CIRCUIT BOARD	A1	A1																
B-DD-5016743-0-0	1		DRAWING DIRECTORY	A	A																
K-CS-5416744-0-DBV			VALID DATA BASE	A	A																

NOTES:

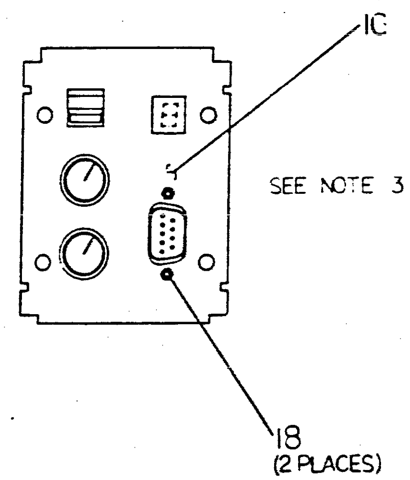
REVISION HISTORY																					
REV.	A	B																			
ECO NO.	INIT	TW0001																			
DATE	1/85	5-85																			

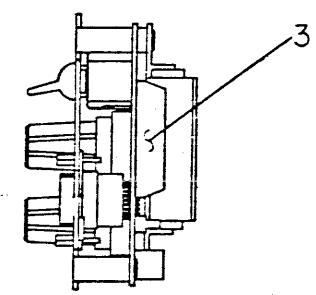
digital

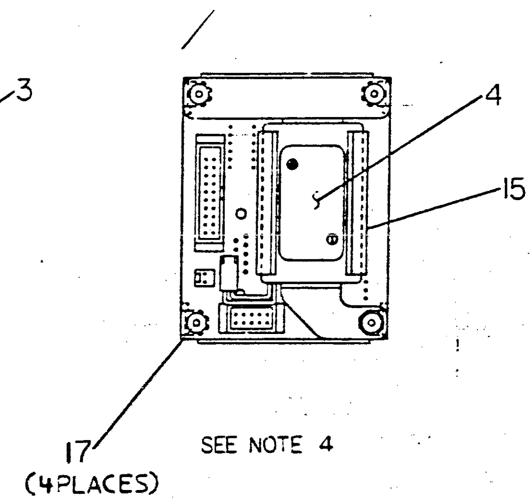
DRN. D.DROZD	DATE 1/31/85	TITLE FUNCTION SEL/SLU	
CHK'D J.CUNNINGHAM	DATE 1/31/85		
DES. ENG. M. deMARE	DATE 1/31/85	DOCUMENT NUMBER	
RESP. ENG M. deMARE	DATE 1/31/85	SIZE B / CODE DD / NUMBER 5416744-0-0	REV. B
MFG. ENG. S. [illegible]	DATE 1/31/85		SHEET 1 OF 1

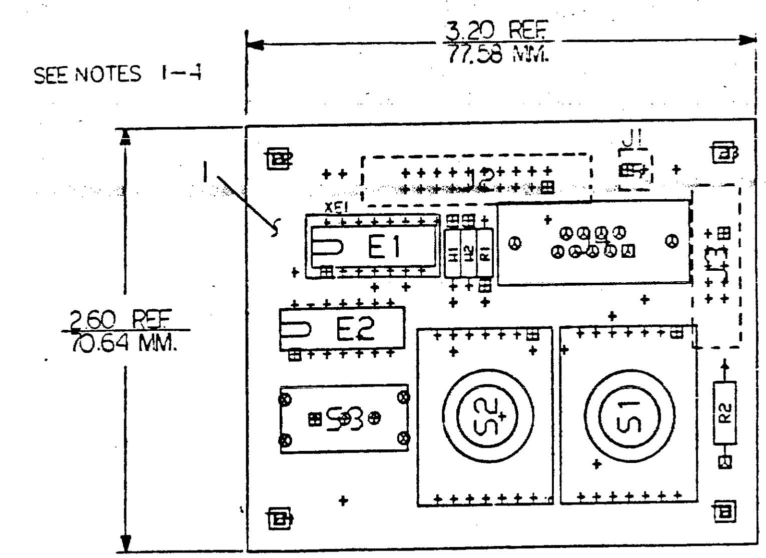
DRB 126C
EN-01242-16-REVA(396)

TW









NOTES:
1. W1 W2 ARE NOT INSTALLED.
2. J1 J2 AND J3 ARE MOUNTED ON SIDE 2
3. MOUNT J4 TO ITEM 16 WITH ITEM 13 BEFORE SOLDERING INTO ITEM 1
4. TEST PANEL IN TESTER AFTER COMPLETING NOTE 3 AND BEFORE ASSEMBLY OF ITEMS 1,15,&16 WITH ITEM 17.

STEP &	↑ Y AXIS ______ STEP ___ TIMES
REPEAT	→ X AXIS ______ STEP ___ TIMES

REV	CHANGE NO	CHK	D.
B	5416744-TW1		D. JERRY 24-MAY-85 M.DEMARE

ETCH REV. A1

SIGNATURES	DATE
DRN. DAVID DROZD	
CHK'D.	
MECH.ENG.	
PROJ.ENG.	
PROD.	
SCALE 2/1	
SHT. OF	
NEXT HIGHER ASSY. B-DD-5416744-0-0	

digital

TITLE FUNCTION SEL / SLU

SIZE	CODE	NUMBER	REV
D	UA	5416744-0-0	B

1 MS# 275

AUTOMATED BY PRTLST.5R(55) — P A R T S L I S T — SHEET A1 -OF A1

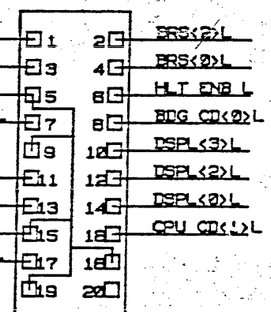
LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION 01	REFERENCE DESIGNATOR
					VARIATION REVISION LEVEL:	A1	
1	1	D-MD-5016743-0-0	5016743-01		CIRCUIT DRILL AND ETCH	1	
2	2		1216565-02		SKT,IC 14PIN DIP TIN ELEV	1	XE1
3	3		1217727-00		PCB,HEADER 20POS(1X20).100CC STR	1	J2
4	4		1219245-01		BATTERY,3CELL 3.75V .18MA NICAD	1	
5	5		1219251-00		PCB HEADER 02PIN(1X02).100CC STR	1	J1
6	6		1219573-05		CONN,D SUB 9PIN ASSY STR	1	J4
7	7		1219952-08		PCB HEADER 09PIN(2X05).100CC STR	1	J3
8	8		1223262-01		SW,ROT 1P08POS	1	S1
9	9		1223263-02		SW,ROT 2P03POS	1	S2
10	10		1223646-01		SW,RKR SPDT ON-OFF-ON	1	S3
11	11		1300229-00		100.0 .25 W 5.0 % CF	1	R1
12	12		1300354-00		750.0 .50 W 5.0 % CF	1	R2
13	13		1912803-00		LS04 INVERTER GATE,HEX	1	E2
14	14		1916921-00		HEXADECIMAL DISPLAY W/DECODER	1	E1
15	15		7430801-01		HOLDER,BATTERY	1	
16	16		7431737-01		PLATE,CONNECTOR	1	
17	17		9008181-01		SCREW,TAP PAN PHIL 6-	4	
18	18		9008451-01		SCREW LOCK,STANDOFF ONLY .060TH	2	

REVISION HISTORY			BASIC PART NO: 5416744				
ENG	ECO NUMBER	REV	SECTION A OF A				
---	INITIAL	A	SECTION.VARIATION INDEX [A] 01 [B] [C] [D] [E] [F] [H] [J] [K] [L] [M] [N]	DRN: E. LANDRY	DATE: 01-JUN-84	D I G I T A L	
				CHK'D: D. DROZD	DATE: 01-JUN-84	TITLE PARTS LIST FUNCTION SEL/SLU MODULE	
				DES.ENG: M. DEMARE	DATE: 12-OCT-84	DOCUMENT NUMBER	
				RESP.ENG.: M. DEMARE	DATE: 12-OCT-84	SIZE: K / CODE: PL / NUMBER: 5416744-0-DBP	REV: A
				MFG.ENG.: S. WASH	DATE: 12 NOV 84	RELEASE DATE: 27-FEB-85	
				ASSEMBLY NUMBER: D-UA-5416744-0-0	TOP DOCUMENT NUMBER: D-UA-5416744-0-0P	FILE NAME: ML769A.PLS	EDIT #: 34

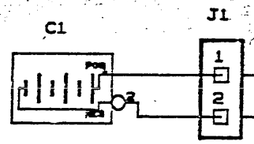
FROM M7608 J2 PIN	TO FS&SLU J2 PIN		FROM M7608 J2 PIN	TO FS&SLU J2 PIN	
1	20	GND	11	10	DSPL<3>L
2	19	GND	12	9	GND
3	18	GND	13	8	BDG CD<0>L
4	17	CPU CD<0>L	14	7	BDG CD<1>L
5	16	CPU CD<1>L	15	6	HLT ENB L
6	15	GND	16	5	GND
7	14	DSPL<0>L	17	4	BRS<0>L
8	13	DSPL<1>L	18	3	BRS<1>L
9	12	DSPL<2>L	19	2	BRS<2>L
10	11	BTRYU H	20	1	+5.0VF = VCC

FROM M7608

J2



C1



J1

BTRYU H

DSPL<1>L

GND

CPU CD<0>L

DSPL<3>L

DSPL<2>L

DSPL<1>L

DSPL<0>L

E2 BDSPL<3>H

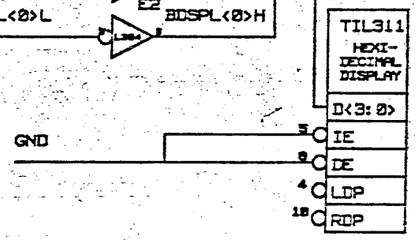
E2 BDSPL<2>H

E2 BDSPL<1>H

E2 BDSPL<0>H

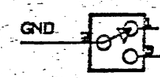
XE1

TIL311 HEXI-DECIMAL DISPLAY



GND

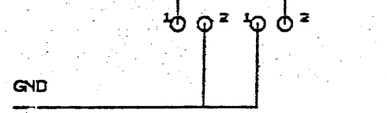
S3 Halt Enable



CPU CD<1>L

CPU CD<0>L

W2 W1



GND

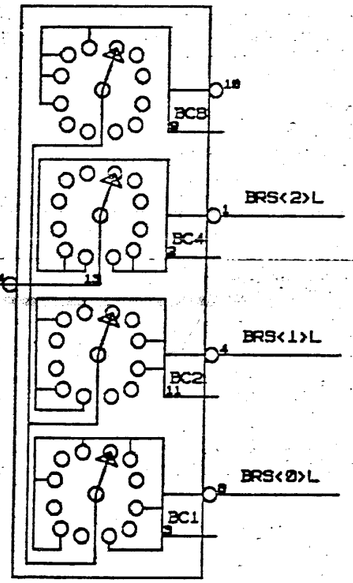
CPU CD<1:0>L

W2	W1	FUNCTION
R	R	NORMAL
R	I	AUXILIARY 1
I	R	AUXILIARY 2
I	I	AUXILIARY 3

I=INSERTED

R=REMOVED

S1



Baud Switch

BRS<2:0>L

0	HHH	300 BAUD
1	HHL	600
2	HLH	1200
3	HLL	2400
4	LHH	4800
5	LHL	9600
6	LLH	19200
7	LLL	38400

to Console terminal

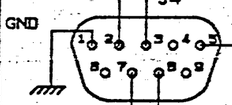
SLU OUT L

SLU INP L

GND

CHASSIS GND

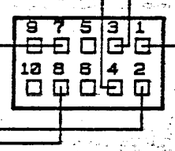
J4



SLU IN L

R1 100 1/4W

J3



R2 750 ohms 1/2W

+12.0VF

S2

BDG CD<0>L

BDG CD<1>L

SLU INP L

SLU OUT L

Mode Switch

BDG CD<1:0>L

0	HH	NORMAL
1	HL	LANGUAGE INQUIRY
2	LH	SLU LOOPBACK TEST

FROM M7608 J3 PIN	TO FS&SLU J3 PIN	
1	10	BUVRESET<L>
2	9	GND
3	8	SLU OUT L
4	7	GND
5	6	KEY
3	5	KEY
7	4	SLU IN H
8	3	SLU IN L
9	2	GND
10	1	+12.0VF

REVISION HISTORY		
REV	ECO NUMBER	DATE

DRAWING

TITLE=FUNCT SEL/SLU

ABBREV=FSSLU

LAST_MODIFIED=Thu Jan 31 17:20:33 1985

DEFINE

X_FIRST=0

X_STEP=SIZE

digital

DRN: Malcolm de Mars	DATE 28-SEP-84	ENG: Malcolm de Mars	DATE 28-SEP-84	TITLE: Function Selection & SLU Module (FS&SLU) for M7608(KA630)	
CHK'D: DAVE DROZD	DATE 28-SEP-84	SHEET 1 OF 1			
		NEXT HIGHER ASSEMBLY: B-DD-5416744-0-0		SIZE K / CODE CS / NUMBER 5416744-0-1	REV A

SIZE	CODE	NUMBER	REV
B	DD	M9047-0-0	B

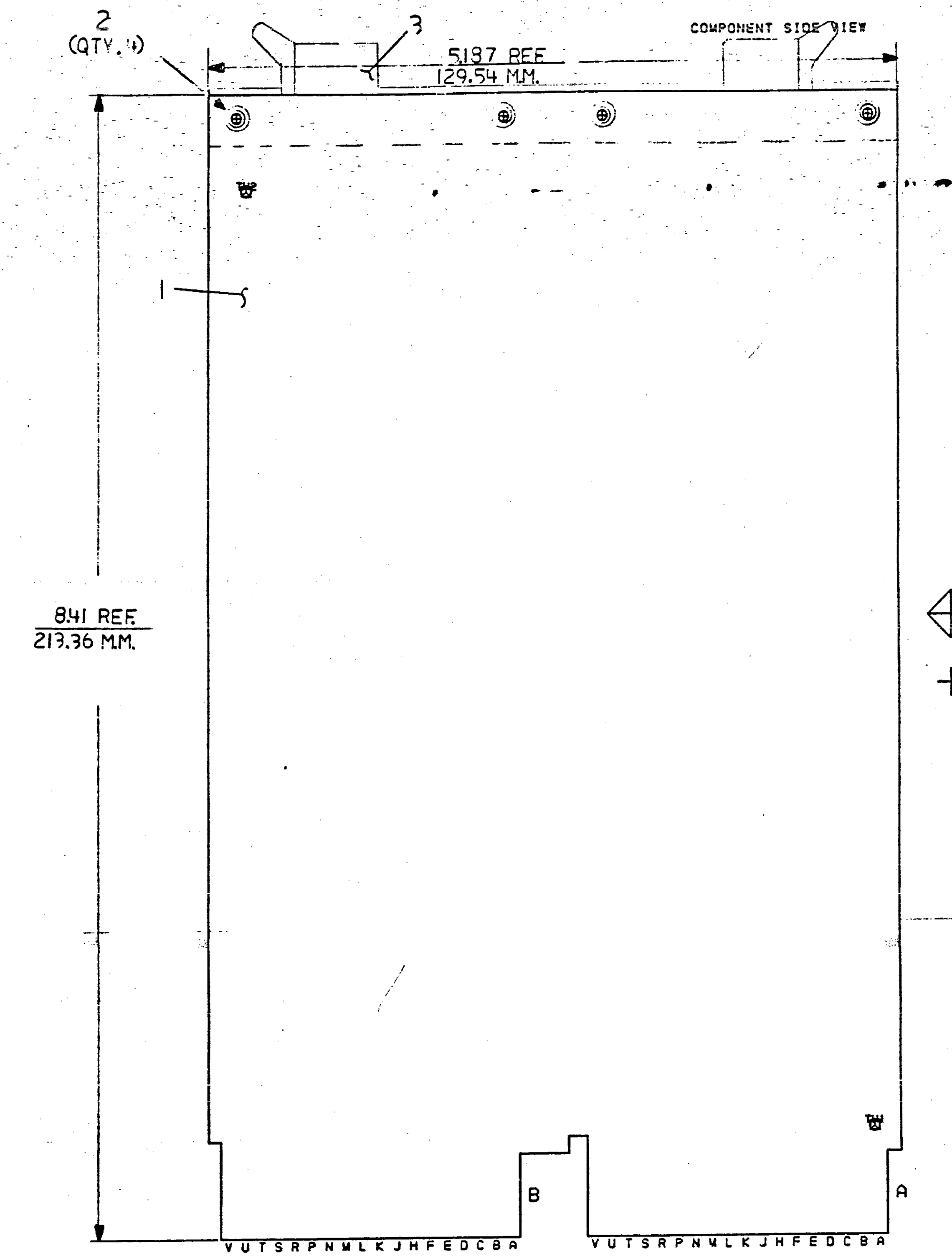
DRAWING NO.	NO. OF SHTS.	PART NO.	DESCRIPTION	REVISIONS
		M9047-00	GRANT CONTINUITY	A1 B1
D-UA-M9047-0-0	1		GRANT CONTINUITY UNIT ASSEMBLY	A B
D-CS-M9047-0-1	1		GRANT CONTINUITY SCHEMATIC	A A
K-PL-M9047-0-DBP	1		GRANT CONTINUITY PARTS LIST	A B
K-PC-M9047-0-DBP			P.C. DESIGN DATA BASE	A B
		5016679-01	ETCHED CIRCUIT BOARD	A1 B1
B-DD-5016679-0-0			DRAWING DIRECTORY	A B

NOTES:

REVISION HISTORY		
REV.	A	B
ECO NO.	11/84 INIT	5/85 ML001
DATE		

digital

DRN. BARRY CORMIER	DATE 11/9/84	TITLE: GRANT CONTINUITY
CHK'D J.CUNNINGHAM	DATE 11/9/84	DOCUMENT NUMBER
DES. ENG. R.LEAZER	DATE 11/14/84	SIZE B / CODE DD / NUMBER M9047-0-0 / REV. B
RESP. ENG. R.LEAZER	DATE 11/14/84	SHEET 1 OF 1
MFG. ENG. A. BROOKS	DATE 11/14/84	



NOTES:

STEP & REPEAT ↑ Y AXIS ____ STEP ____ TIMES
→ X AXIS ____ STEP ____ TIMES

REV	CHANGE NO	CHK
B	M9047-M-001	

ETCH REV. B1-P2

SIGNATURES	DATE
DRN. E. LANDRY	4-9-85
CHK'D.	4-9-85
MECH. ENG.	5-10-85
PROJ. ENG.	5-10-85
PROD. (EB)	5-10-85
SCALE 2/1	
SHT. 1 OF 1	

digital

TITLE GRANT CONTINUITY

SIZE	CODE	NUMBER	REV
D	UA	M9047-0-0	B

NEXT HIGHER ASSY. B-DD-M9047-0-0

MS# 275466

SIZE D | CODE CS | NUMBER M9047-0 -1 | REV A

AM2

AN2

AR2

AS2

REVISION HISTORY		
REV.	ECO NUMBER	DATE

DRN David Doty	DATE 2-26-85	TITLE digital
CHK Ed Cantey	DATE 2-27-85	GRANT CONTINUITY
DES. ENGR. Barry Markin	DATE 2-27-85	
REL. ENGR. Barry Markin	DATE 2-27-85	DOCUMENT NUMBER
PROJ. ENGR.	DATE 2-27-85	SIZE D | CODE CS | NUMBER M9047-0-1 | REV A
NEXT HIGHER DOC. B-00-M9047-0 -0		SCALE | SHEET 1 OF 1

DRD 102E

AUTOMATED BY PRTLST.5R(55)

P A R T S L I S T

LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION 01	02
					VARIATION REVISION LEVEL:	A1	A1
1	1	A-PS-1700313-0-0	1700313-01	A	CABLE ASSY,06 COND,MOLD,SHLD 2	1	-
2	2	A-PS-4700042-0-0	4700042-01		SCREWDRIVER,FLAT BLADE 0.12 X 2.	1	1
3	3	A-PS-3622092-0-0	3622092-01	A	LABEL,LCP5 CONFIGURATION	1	1
4	4	A-PS-9907349-0-0	9907349-01	A	CARTON,DIECUT,C,200PSI,W/GRAPHIC	1	1
5	5	B-DD-M9047-0	M9047-00		QBUS GRANT CONTINUITY,1ST USED I	1	1
6	6	A-PS-1700301-0-0	1700301-00	A	CABLE ASSY,07 COND,MOLD,SHLD 2	-	1
7	7	A-PS-3624251-0-0	3624251-01	A	LABEL,FRONT CONTROL PANEL BA123	1	1

REVISION HISTORY			BASIC PART NO: 7022382			
ENG	ECO NUMBER	REV	SECTION A OF A			
---	INITIAL	A	SECTION.VARIATION INDEX [A]01,02	DRN: D. HEALY	DATE: 05-DEC-84	D I G I T A L
			[B]	CHK'D: D. HEALY	DATE: 08-MAR-85	TITLE PARTS LIST BA123-A ACCESSORY KIT
			[C]	DES.ENG: J. KWONG	DATE: 08-MAR-85	DOCUMENT NUMBER: SIZE K, CODE PL, NUMBER 7022382-0-DBP, REV A
			[D]	RESP.ENG.: J. KWONG	DATE: 08-MAR-85	
			[E]	MFG.ENG.: J. EDWARDS	DATE: 08-MAR-85	RELEASE DATE: 26-MAR-85
			[F]	ASSEMBLY NUMBER:	TOP DOCUMENT NUMBER:	FILE NAME: ML755A.PLS, EDIT # 4

FIELD MAINTENANCE PRINT SET

TABLE OF CONTENTS

UNIT VARIATIONS COVERED BY THIS PRINT SET
7022380-A2
7022380-A3

7022380
FIELD MAINTENANCE PRINT SET

DIGITAL EQUIPMENT CORPORATION

PRINT SET PART NUMBER MP-02049-01 REV A1

FILE NAME: TC7022380-0-DBUA

REVISION HISTORY		
REV.	ECO NUMBER	DATE
A	INITIAL	

DRN. D. HEALY	DATE 29 NOV 84	TITLE digital BA123-A BASIC ENCLOSURE
CHK'D D. HEALY	DATE 08 MAR 85	
DES. ENG. J. KWONG	DATE 08 MAR 85	
RESP. ENG. J. KWONG	DATE 08 MAR 85	
FIELD SERVICE J. EVANS	DATE 08 MAR 85	
TOP DOC. B-DD-7022380-0-DBU		SIZE B · CODE TC · NUMBER 7022380-0-DBU · REV. A · SHEET 1 OF 1

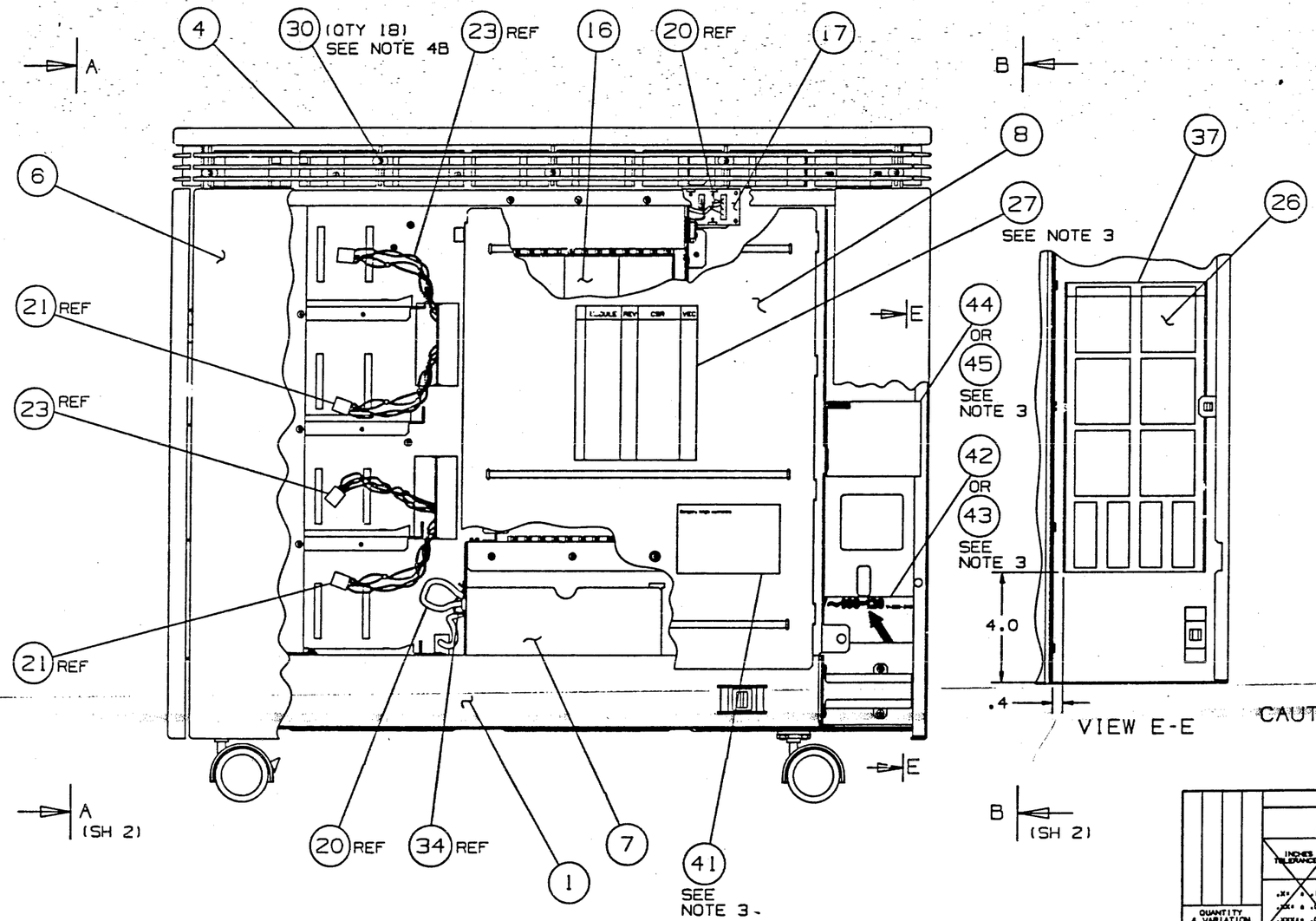
SIZE B · CODE TC · NUMBER 7022380-0-DBU · REV. A

ML01

LEGEND		
PART NO.	REV	V. RIATION
7022380-01	A1	120V
7022380-02	A1	240V

NOTES:

1. ITEM #12 (LOUVRE,SHORT) TO BE ORIENTATED BY ITS MARKING LOCATED ON THAT ITEM.
2. ITEMS #34 (CABLE CLAMP) TO BE LOCATED APPROX WHERE SHOWN.
3. LOCATE ITEMS 27,41, 42 OR 43, 44 OR 45 APPROX WHERE SHOWN NEAR SIDE.
4. TORQUE REQUIREMENTS ARE AS FOLLOWS:
   A. ITEMS #31,32 & 36 SHALL BE 8 TO 11 INCH-LBS
   B. ITEM #30 TO BE 6 TO 8 INCH-LBS
   C. ITEM #29 TO BE 18 TO 24 INCH-LBS.
5. WORKMANSHIP TO BE PER DEC STD 187



CAUTION: OFF SHEET PARTS LIST EXISTS REFER TO K-PL-7022380-0-DBP (ML 752)

REVISIONS			
CHK	CHANGE NO.	RELEASE	REV.
			B

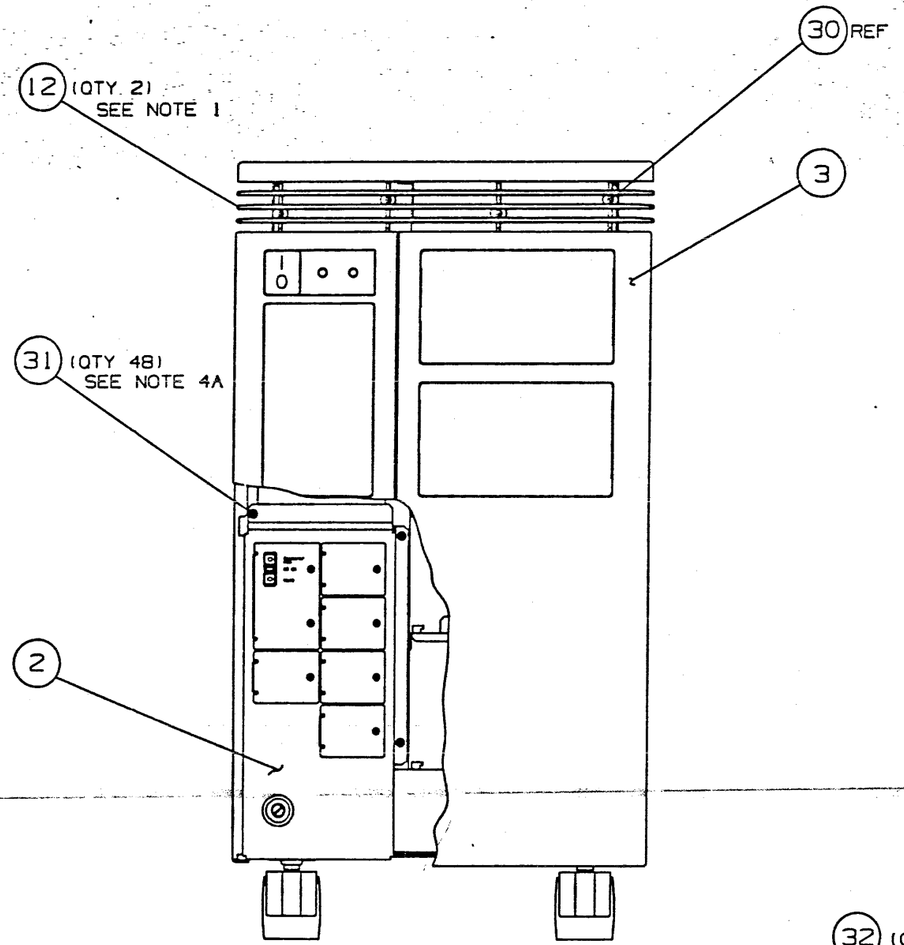
DESCRIPTION	DRAWING NO.	PART NO.	ITEM NO.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND THE FOLLOWING TOLERANCES APPLY (PER DEC STD 114)

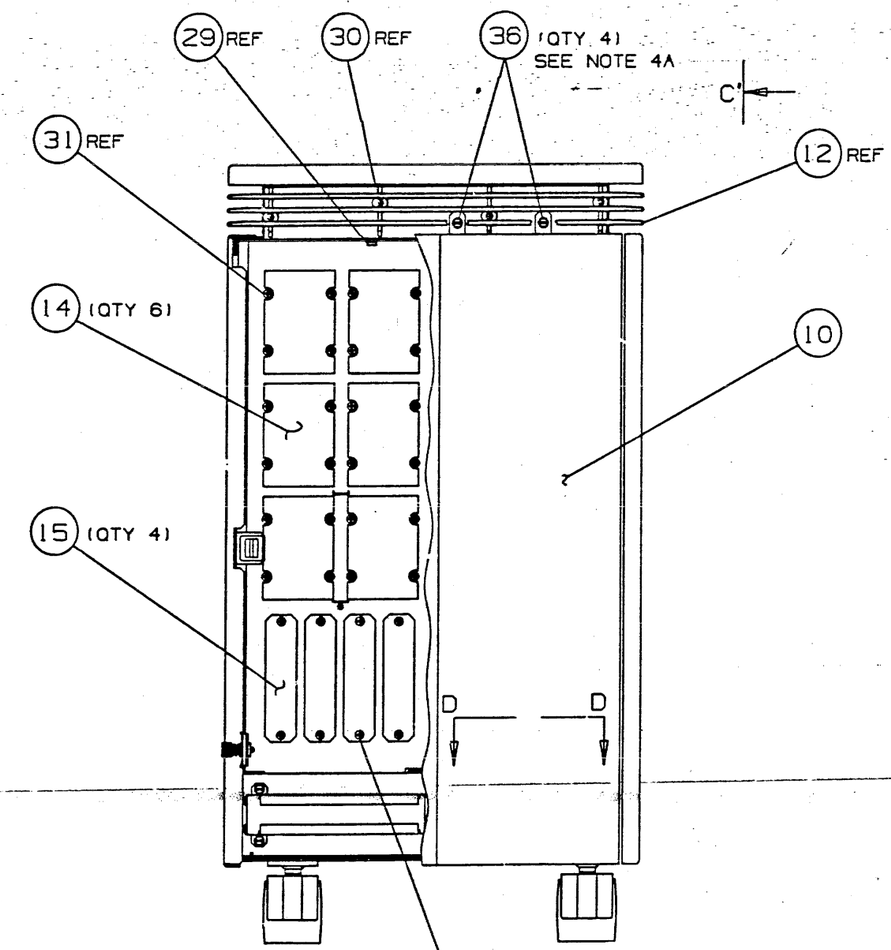
QUANTITY & VARIATION	INCHES TOLERANCES	ANGLES ±0° 30'	SURFACE QUALITY MICROINCHES	APPLICABLE DIMENSION RANGE (CHECK ONE)	DIMENSION RANGE IN INCHES: OVER 0 TO 3.0	OVER 3.0 TO 6.0	OVER 6.0 TO 12.0	OVER 12.0 TO 30.0	OVER 30.0 TO 80.0
	.X ± .1				±.02	±.03	±.05	±.10	
	.XX ± .02				±.004	±.008	±.012	±.016	±.024	±.04
	.XXX ± .005								

THIRD ANGLE PROJECTION	DRN D. PELLEGRINO	DATE 17-DEC-84	TITLE digital BA123-A BASIC ENCLOSURE
DO NOT SCALE DRAWING	CHK'D J. KUSHAGIN	DATE 14-FEB-85	
REMOVE BURRS AND BREAK SHARP CORNERS	DES. ENG. J. KWONG	DATE 17-DEC-84	
MATERIAL SEE PARTS LIST	PROJ. ENG. J. KWONG	DATE 17-DEC-84	DOCUMENT NUMBER: SIZE D, CODE AD, NUMBER 7022380-0-DBU, REV B
FINISH NONE	MFG. ENG. J. EDWARDS	DATE 17-DEC-84	SCALE 1/2, SHEET 1 OF 3
	TOP DOC. D-AD-7022380-0-DBU		

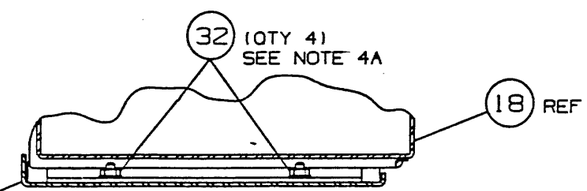
7022380-0-DBU REV B
D AD



VIEW A-A



VIEW B-B

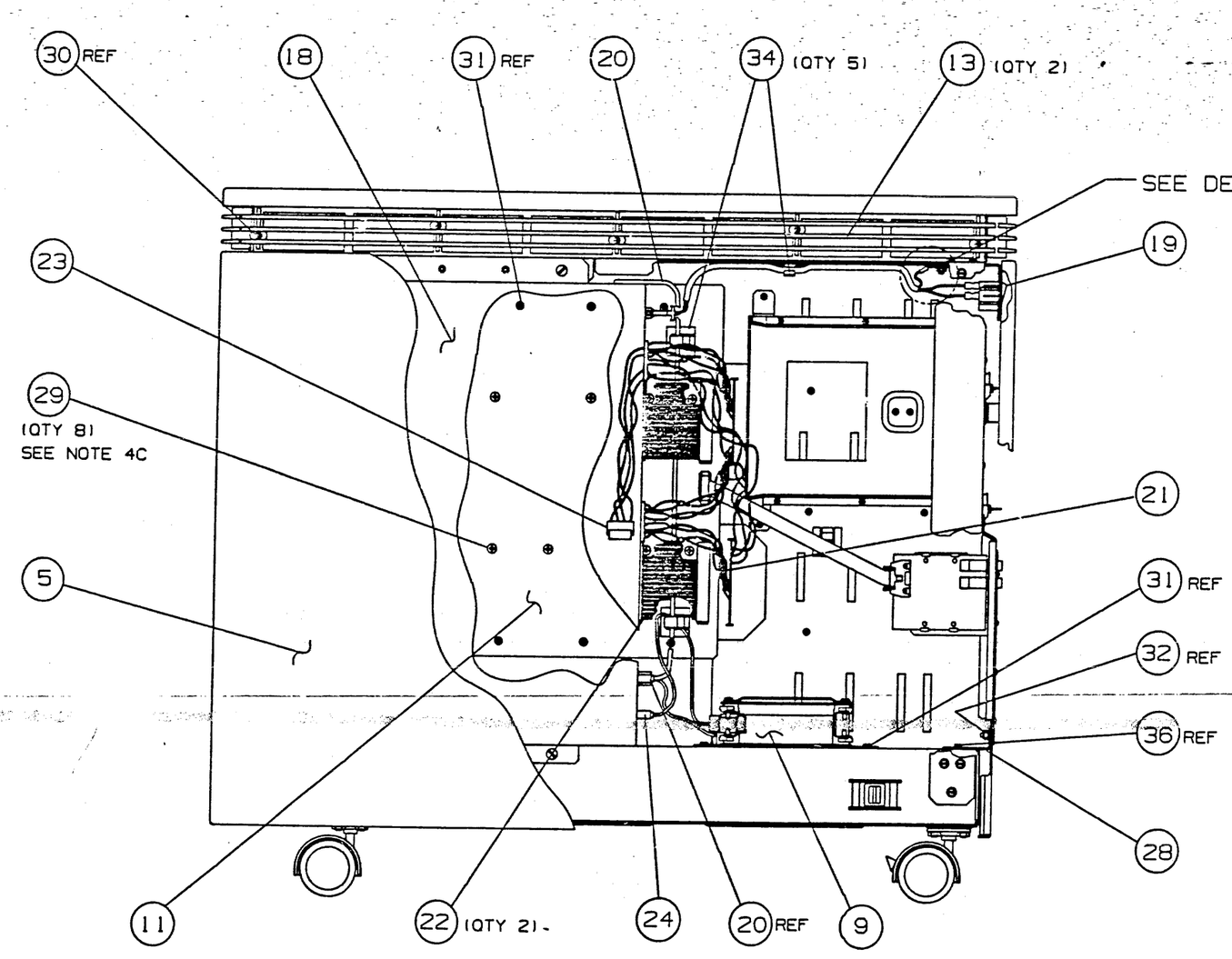


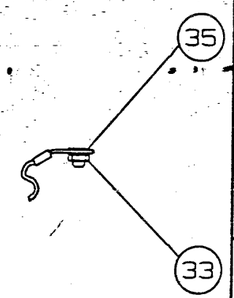
SECTION D-D
SCALE: 1/1

C (SH 3)

REVISIONS		
CHK	CHANGE NO	REV
	RELEASE	B

TITLE	SIZE	CODE	NUMBER	REV
BA123-A BASIC ENCLOSURE	D	AD	7022380-0-DBU	B
SCALE 1/2	SHEET 2 OF 3		DIST	





DETAIL E
SCALE 1/1

VIEW C-C

REVISIONS		
CHK	CHANGE NO	REV
	RELEASE	B

TITLE	BA123-A BASIC ENCLOSURE			
SIZE	CODE	NUMBER	REV	
D	AD	7022380-0-DBU	B	
SCALE 1/2	SHEET 3 OF 3	DIST		

AUTOMATED BY PRTLST.5R(55)

P A R T S L I S T

LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION 01	02
					VARIATION REVISION LEVEL:	A1	A1
1	1	D-AD-7021991-0-DBU	7021991-01		FRAME ASSEMBLY	1	1
2	2	C-AD-7021996-0-DBU	7021996-01		CONTROL PANEL ASSY.	1	1
3	3	D-AD-7021997-0-DBU	7021997-01		PANEL COVER FRONT DISK ASSY	1	1
4	4	D-AD-7021999-0-DBU	7021999-01		TOP COVER ASSY.	1	1
5	5	D-AD-7022000-0-DBU	7022000-01		SIDE PANEL ASSY L/H	1	1
6	6	D-AD-7022001-0-DBU	7022001-01		SIDE PANEL ASSY R/H	1	1
7	7	D-AD-7022003-0-DBU	7022003-01		FAN MOUNT CARD CAGE ASSY.	1	1
8	8	D-IA-7022006-0-DBU	7022006-01		COVER FRONT CARD CAGE ASSY.	1	1
9	9	D-AD-7022296-0-DBU	7022296-01		FAN MOUNT MASS STORAGE ASSY	1	1
10	10	D-AD-7022339-0-DBU	7022339-01		DOOR, REAR ASSY.	1	1
11	11	D-IA-7430692-0-DBU	7430692-01		COVER,REAR,CARD CAGE	1	1
12	12	D-MD-7430709-0-DBU	7430709-01		LOUVRE,SHORT	2	2
13	13	D-MD-7430710-0-DBU	7430710-01		LOUVRE,LONG	2	2
14	14	C-IA-7427574-0-0	7427574-01		PLATE,COVER	6	6
15	15	B-MD-7428683-0-DBU	7428683-01		PLATE,CONNECTOR BLANK	4	4
16	16	E-UA-5417507-0-DBU	5417507-01		QBUS BACKPLANE,13 SLOTS,QUAD	1	1
17	17	D-UA-5416665-0-DBU	5416665-01		REMOTE SENSE OF TEMPERATURE FOR	1	1
18	18	D-PS-3023616-0-DBU	3023616-01		P.S. 460W 2DC REGULATOR BDS,FAN	1	1
19	19	A-PS-1700859-0-0	1700859-01		CABLE ASSY,AC,ON/OFF POWER	1	1
20	20	A-PS-1700863-0-0	1700863-01		CABLE ASSY,FAN	1	1
21	21	A-PS-1700870-0-0	1700870-01		CABLE ASSY,DC POWER DRIVE	1	1
22	22	A-PS-1700865-0-0	1700865-01		CABLE ASSY,18COND	2	2
23	23	A-PS-1700911-0-0	1700911-01		CABLE ASSY,9POS POWER DRIVE	1	1
24	24	A-PS-1700864-0-0	1700864-01		CABLE ASSY,FAN	1	1
25	25	A-PA-3700821-0-0	3700821-01		PKG COMPUTER, BA123 CUSTOMER	1	1
26	26	A-PS-3624253-0-0	3624253-01		LABEL,I/O,BULKHEAD	1	1
27	27	A-PS-3624254-0-0	3624254-01		LABEL,MU BUSINESS COMPUTER	1	1
28	28	C-MD-7431225-0-DBU	7431225-01		BRACKET,CONTROL PANEL	1	1
29	29		9010174-01		SCREW,SEMS PAN PHIL 8-	8	8
30	30		9000055-01		SCREW,THD RL,PAN POZI F/METL 4	18	18

REVISION HISTORY

ENG	ECO NUMBER	REV
---	INITIAL	B

BASIC PART NO: 7022380

SECTION A OF A

SECTION.VARIATION INDEX
[A]01,02
[B]
[C]
[D]
[E]
[F]

DRN: S. STEFANICK DATE: 18-DEC-84

CHK'D: J. KUSHAGIN DATE: 13-FEB-85

DES.ENG: J. KWONG DATE: 18-DEC-84

RESP.ENG.: J.KWONG DATE: 18-DEC-84

MFG.ENG.: J. EDWARDS DATE: 18-DEC-84

ASSEMBLY NUMBER: B-DD-7022380-0-DBU

TOP DOCUMENT NUMBER: B-DD-7022380-0-DBU

D I G I T A L

TITLE PARTS LIST
BA123-A BASIC ENCLOSURE

DOCUMENT NUMBER

SIZE	CODE	NUMBER	REV
K	PL	7022380-0-DBP	B

RELEASE DATE: 06-MAR-85

FILE NAME: ML752B.PLS

EDIT # 23

LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION 01	02
					VARIATION REVISION LEVEL:	A1	A1
31	31		9009701-00		SCREW,SEMS PAN PHIL 6-	48	48
32	32		9006560-00		NUT,HEX EXT TOOTH LCKWSHR 6-32	4	4
33	33		9007651-00		WASHER,LOCK EXTERNAL STEEL	1	1
34	34		9010016-00		CLAMP, CABLE, ADH BACK	5	5
35	35		9006565-00		NUT,HEX EXT TOOTH LCKWSHR 10-32	1	1
36	36		9010075-03		SCREW,TAP HEXWW THD RL 6-	4	4
37	37		9907588-01		ENVELOPE,CLEAR ADH BACK	1	1
38	38	D-AR-7022380-0-DBU			BA123-A SYSTEM ARRANGEMENT	REF	REF
39	39	K-SP-BA123-A-DBF			ENG. SPEC BA123-A	REF	REF
40	40		1700083-00		PWR CORD,TERM 3-14 SJT 125	1	-
41	41		3615087-04		LABEL,"DANGER-HIGH CURRENT"	1	1
42	42		3617905-16		LABEL,WARNING EQUIP. RATING,100-	1	-
43	43		3617905-17		LABEL,WARNING EQUIP. RATING,220-	-	1
44	44	A-PS-3624471-0-0	3624471-01		LABEL,BUSINESS COMP BA123-A2	1	-
45	45	A-PS-3624471-0-0	3624471-02		LABEL,BUSINESS COMP BA123-A3	-	1

46 NOTE: ITEMS #25 AND #40 NOT SHOWN ON FIELD OF DWG.

D I G I T A L	TITLE BA123-A BASIC ENCLOSURE	SECTION A OF A	SIZE: K / CODE: PL / DOCUMENT NUMBER: 7022380-0-DBP	REV: B

DRAWING DIRECTORY

UNIT VARIATIONS

VAR	TITLE
7022380-01	BA123-A BASIC ENCLOSURE (120 V)
7022380-02	BA123-A BASIC ENCLOSURE (240 V)

FILE NAME: DD7022380-0-DBUA

REVISIONS		
REV.		A
CHANGE NO.		INITIAL
CHK		

USED ON OPTION/MODEL
17308-C2
17308-C3

SHEET 1 OF 6

DRN.	D. HEALY	DATE 29 NOV 84
CHK'D	D. HEALY	DATE 08MAR85
PROJ. ENG.	J. KWONG	DATE 08MAR85
PROD.	J. EDWARDS	DATE 08MAR85
TOP DOC.	B-DD-7022380-0-DBU	

TITLE

digital

BA123-A BASIC ENCLOSURE

SIZE	CODE	NUMBER	REV.
B	DD	7022380-0-DBU	A

DIST.

ML01

1 — BA123-A BASIC ENCLOSURE
D-AD-7022380-0-DBU
K-PL-7022380-0-DBP

2 — FRAME ASSEMBLY
D-AD-7021991-0-DBU
K-PL-7021991-0-DBP

3 — BOTTOM PLENUM ASSY
E-AD-7021992-0-DBU
K-PL-7021992-0-DBP

4 — SPRING RETAINER ASSY
D-IA-7021147-0-DBU
K-PL-7021147-0-DBP

5 — MASS STORAGE/TAPE DRIVE ASSY
D-IA-7022320-0-DBU
K-PL-7022320-0-DBP

6 — SHELF MASS STORAGE ASSEMBLY
D-IA-7021993-0-DBU
K-PL-7021993-0-DBP

4 — SPRING RETAINER ASSY
D-IA-7021147-0-DBU
K-PL-7021147-0-DBP

7 — SHELF TAPE DRIVE ASSEMBLY
D-IA-7021994-0-DBU
K-PL-7021994-0-DBP

4 — SPRING RETAINER ASSY
D-IA-7021147-0-DBU
K-PL-7021147-0-DBP

8 — CARD CAGE ASSEMBLY
D-IA-7021995-0-DBU
K-PL-7021995-0-DBP

9 — QBUS BACKPLANE 13 SLOTS QUAD
B-DD-5417507-0-0

10 — CONTROL PANEL ASSY
C-AD-7021996-0-DBU
K-PL-7021996-0-DBP

11 — BEZEL SYSTEM CONSOLE ASSEMBLY
D-AD-7022305-0-DBU
K-PL-7022305-0-DBP

12 — WELDMENT BEZEL SYSTEM CONSOLE
D-IA-7022048-0-DBU
K-PL-7022048-0-DBP

13 — CONSOLE BOARD FOR BA123-A
B-DD-5416596-0-0

14 — POWER SUPPLY ASSY (H7260)
A-PS-3023616-0-0

SEE SHEET 3

TITLE: BA123-A BASIC ENCLOSURE	SHEET 2 OF 6	SIZE	CODE	NUMBER	REV.
		B	DD	7022380-0-DBU	A

ML01

CONT FROM
SHEET 2

(15) PANEL, COVER FRONT DISK ASSEMBLY
D-AD-7021997-0-DBU
K-PL-7021997-0-DBP

(16) COVER FRONT CARD CAGE ASSEMBLY
D-IA-7022006-0-DBU
K-PL-7022006-0-DBP

(17) TOP COVER ASSEMBLY
D-AD-7021999-0-DBU
K-PL-7021999-0-DBP

(18) SIDE PANEL ASSEMBLY L/H
D-AD-7022000-0-DBU
K-PL-7022000-0-DBP

(19) PANEL SIDE L/H WELDMENT
D-IA-7022302-0-DBU
K-PL-7022302-0-DBP

(20) SIDE PANEL ASSEMBLY R/H
D-AD-7022001-0-DBU
K-PL-7022001-0-DBP

(21) PANEL SIDE R/H WELDMENT
D-IA-7022303-0-DBU
K-PL-7022303-0-DBP

(22) FAN MOUNT MASS STORAGE ASSEMBLY
D-AD-7022296-0-DBU
K-PL-7022296-0-DBP

(23) FAN MOUNT CARD CAGE ASSEMBLY
D-AD-7022003-0-DBU
K-PL-7022003-0-DBP

(24) PACKAGING ASSY
A-PA-3700821-0-0
K-PL-3700821-0-DBP

(25) DOOR, REAR ASSY
D-AD-7022339-0-DBU
K-PL-7022339-0-DBP

(26) REMOTE OF SENSE TEMPERATURE
B-DD-5416665-0-0

TITLE: BA123-A BASIC ENCLOSURE	SHEET 3 OF 6	SIZE B	CODE DD	NUMBER 7022380-0-DBU	REV. A

ML01

FIND NO.	DRAWING NO.	DESCRIPTION	TYPE
1	MP-02049-01	BA123-A BASIC ENCLOSURE (MP)	-
	B-TC-7022380-0-DBU	BA123-A BASIC ENCLOSURE (TC)	-
	D-AD-7022380-0-DBU	BA123-A BASIC ENCLOSURE	E/M
	K-PL-7022380-0-DBP	BA123-A BASIC ENCLOSURE (PL)	E/M
	D-AR-7022380-0-DBU	BA123-A SYSTEM ARRANGEMENT	REF
	A-SP-BA123-A-DBF	BA123-A MICRO SYS. ENCL. FUNC. SPEC.	E/M
	D-IA-7430692-0-DBU	COVER, REAR CARD CAGE	M
	K-PL-7420692-0-DBP	COVER, REAR CARD CAGE (PL)	M
	D-MD-7430709-0-DBU	LOUVER, SHORT	M
	D-MD-7430710-0-DBU	LOUVER, LONG	M
	C-IA-7427574-0-DBU	PLATE, COVER	M
	K-PL-7427574-0-DBP	PLATE, COVER (PL)	M
	B-MD-7428683-0-DBU	PLATE, CONN. BLANK	M
	A-PS-1700859-0-0	CABLE ASSY AC ON/OFF PWR	E/M
	A-PS-1700865-0-0	CABLE, 18 COND P.S. TO BACK PANEL	E/M
	A-PS-1700863-0-0	CABLE, P.S. TO CC FAN & SENSOR	E/M
	A-PS-1700911-0-0	CABLE, P.S. TO 3 DRIVES	E/M
	A-PS-1700870-0-0	CABLE, P.S. TO 2 DRIVES	E/M
	A-PS-1700083-0-0	US LINE CORD	E/M
	C-MD-7431225-0-DBU	BRACKET, CONTROL PANEL	M
	A-PS-3624253-0-0	LABEL, I/O BULKHEAD	M
	A-PS-3624254-0-0	LABEL, MU BUSINESS COMPUTER	M
	A-PS-3615087-0-0	LABEL, DANGER, HIGH CURRENT	M
	A-PS-3617905-0-0	LABEL, EQUIP RATING	M
	A-PS-3624471-0-0	LABEL, BUSINESS COMPUTER	M
2	D-AD-7021991-0-DBU	FRAME ASSEMBLY	M
	K-PL-7021991-0-DBP	FRAME ASSEMBLY (PL)	M
	D-IA-7430684-0-DBU	SUPPORT VERT	M
	K-PL-7420684-0-DBP	SUPPORT VERT (PL)	M
	D-MD-7430699-0-DBU	SUPPORT, REAR CENTER	M
	C-IA-7421109-0-DBU	BRACKET, BULKHEAD	M
	K-PL-7431109-0-DBP	BRACKET, BULKHEAD (PL)	M
	E-IA-7430687-0-DBU	BULKHEAD, I/O	M
	K-PL-7430687-0-DBP	BULKHEAD, I/O (PL)	M
	E-MD-7420688-0-DBU	PANEL, TOP	M
	D-MD-7420701-0-DBU	BAFFLE	M
	E-IA-7430744-0-DBU	BAFFLE, HORIZ. MASS STORAGE	M
	K-PL-7430744-0-DBP	BAFFLE, HORIZ. MASS STORAGE (PL)	M

FIND NO.	DRAWING NO.	DESCRIPTION	TYPE
	D-MD-7430827-0-DBU	BRACKET, MTG	M
	D-MD-7431188-0-DBU	HINGE, REAR DOOR LIVING	M
	B-IA-7431605-0-DBU	BRKT, DOOR INTERLOCK SWITCH	M
	K-PL-7431605-0-DBP	BRKT, DOOR INTERLOCK SWITCH (PL)	M
	A-PS-1700942-0-0	CABLE ASSY FAN DOOR INTERLOCK	E/M
	D-MD-7431189-0-DBU	RESTRAINT, CABLE	M
3	E-AD-7021992-0-DBU	BOTTOM PLENUM ASSEMBLY	M
	K-PL-7021992-0-DBP	BOTTOM PLENUM ASSEMBLY (PL)	M
	E-IA-7431044-0-DBU	PLENUM, BOTTOM	M
	K-PL-7431044-0-DBP	PLENUM, BOTTOM (PL)	M
	E-IA-7430689-0-DBU	PANEL BOTTOM	M
	K-PL-7430689-0-DBP	PANEL BOTTOM (PL)	M
	C-MD-7430743-0-DBU	BRACKET, GND	M
	D-MD-7427554-0-DBU	HALF SLIDE	M
	C-MD-7431175-0-DBU	BRACKET, SUPPORT(REAR PANEL)	M
	D-MD-7431108-0-DBU	GUIDE, CARD CAGE FAN TRAY	M
	E-IA-7430700-0-DBU	PLENUM, CARD CAGE	M
	K-PL-7430700-0-DBP	PLENUM, CARD CAGE (PL)	M
4	D-IA-7021147-0DBU	SPRING RETAINER ASSY	M
	K-PL-7021147-0-DBP	SPRING RETAINER ASSY (PL)	M
	B-MD-7429413-0-DBU	BRACKET, SPRING	M
	B-MD-7427217-0-DBU	TAB, SPRING	M
5	D-IA-7022320-0-DBU	MASS STORAGE/TAPE DRIVE ASSY	M
	K-PL-7022320-0-DBP	MASS STORAGE/TAPE DRIVE ASSY (PL)	M
	E-IA-7430697-0-DBU	SUPPORT, INNER VERTICAL	M
	K-PL-7430697-0-DBP	SUPPORT, INNER VERTICAL (PL)	M
	D-MD-7430698-0-DBU	SUPPORT, OUTER VERTICAL	M
6	D-IA-7021993-0-DBU	SHELF MASS STORGAE ASSEMBLY	M
	K-PL-7021993-0-DBP	SHELF MASS STORAGE ASSEMBLY (PL)	M
	D-MD-7430696-0-DBU	SHELF MASS STORAGE	M
	D-MD-7427554-0-DBU	HALF SLIDE	M

TYPE: E ELECTRICAL
M MECHANICAL
E/M ELECTRO/MECHANICAL

digital

TITLE: BA123-A BASIC ENCLOSURE

SHEET 4 OF 6

SIZE	CODE	NUMBER	REV.
B	DD	7022380-0-DBU	A

DRB 108A

ML01

FIND NO.	DRAWING NO.	DESCRIPTION	TYPE
7	D-IA-7021994-0-DBU	SHELF TAPE DRIVE ASSEMBLY	M
	K-PL-7021994-0-DBP	SHELF TAPE DRIVE ASSEMBLY (PL)	M
	D-MD-7430746-0-DBU	SHELF TAPE DRIVE	M
	D-MD-7427554-0-DBU	HALF SLIDE	M
8	D-IA-7021995-0-DBU	CARD CAGE ASSEMBLY	M
	K-PL-7021995-0-DBP	CARD CAGE ASSEMBLY (PL)	M
	E-IA-7430690-0-DBU	FRAME CARD CAGE	M
	K-PL-7430690-0-DBP	FRAME CARD CAGE (PL)	M
	D-MD-7429632-0-DBU	CARD GUIDE 12 SLOT	M
	D-IA-7430693-0-DBU	BAFFLE, FCC	M
	K-PL-7430693-0-DBP	BAFFLE, FCC (PL)	M
9	B-DD-5417507-0-0	QBUS BACKPLANE 13 SLOTS QUAD	E/M
10	C-AD-7021996-0-DBU	CONTROL PANEL ASSEMBLY	M
	K-PL-7021996-0-DBP	CONTROL PANEL ASSEMBLY (PL)	M
	E-IA-7430705-0-DBU	PANEL CONTROL	M
	K-PL-7420705-0-DBP	PANEL CONTROL (PL)	M
	C-MD-7431171-0-DBU	BEZEL, BLANK	M
11	D-AD-7022305-0-DBU	BEZEL, SYSTEM CONSOLE ASSY	E/M
	K-PL-7022305-0-DBP	BEZEL, SYSTEM CONSOLE ASSY (PL)	E/M
	A-PS-1700860-0-0	CABLE ASSY, CONSOLE BACKPLANE	E/M
12	D-IA-7022048-0-DBU	WELDMENT, BEZEL SYS CONSOLE	M
	K-PL-7022048-0-DBP	WELDMENT, BEZEL SYS CONSOLE (PL)	M
	D-MD-7431169-0-DBU	BRACKET, SUPPORT SYSTEM CONSOLE	M
	D-MD-7431173-0-DBU	BEZEL, SYSTEM CONSOLE	M

FIND NO.	DRAWING NO.	DESCRIPTION	TYPE
	A-SS-7022048-0-1	SILK SCREEN	M
13	B-DD-5416596-0-0	CONSOLE BOARD FOR BA123-A	E/M
14	A-PS-3023616-0-0	POWER SUPPLY ASSEMBLY (H7260)	E/M
15	D-AD-7021997-0-DBU	PANEL COVER FRONT DISK ASSY	M
	K-PL-7021997-0-DBP	PANEL COVER FRONT DISK ASSY (PL)	M
	E-MD-7430704-0-DBJ	PANEL, FRONT	M
	C-MD-7431191-0-DBU	BRACKET, STUD	M
	E-MD-7430708-0-DBU	DOOR, FRONT	M
	C-MD-7431178-0-DBU	BRACKET, DOOR HINGE	M
	D-MD-7431477-0-DBU	PANEL, FILLER	M
16	D-IA-7022006-0-DBU	CARD CAGE FRONT COVER ASSY	M
	K-PL-7022006-0-DBP	CARD CAGE FRONT COVER ASSY (PL)	M
	E-IA-7430691-0-DBU	COVER FRONT CARD CAGE	M
	K-PL-7430691-0-DBP	COVER FRONT CARD CAGE (PL)	M
	D-MD-7430828-0-DBU	SUPPORT MODULES	M
	D-MD-7431479-0-DBU	SUPPORT, MODULE REMOVEABLE	M
17	D-AD-7021999-0-DBU	TOP COVER ASSEMBLY	M
	K-PL-7021999-0-DBP	TOP COVER ASSEMBLY (PL)	M
	D-IA-7430707-0-DBU	COVER, TOP	M
	K-PL-7420707-0-DBP	COVER, TOP (PL)	M
	C-MD-7423357-0-DBU	KEY BUTTON	M
	D-IA-7431045-0-DBU	BRACKET, COVER	M
	K-PL-7431045-0-DBP	BRACKET, COVER (PL)	M
18	D-AD-7022000-0-DBU	SIDE PANEL ASSEMBLY L/H	M
	K-PL-7022000-0-DBP	SIDE PANEL ASSEMBLY L/H (PL)	M

TYPE: E ELECTRICAL
M MECHANICAL
E/M ELECTRO/MECHANICAL

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TITLE: BA123-A BASIC ENCLOSURE

SHEET 5 OF 6 | SIZE B | CODE DD | NUMBER 7022380-0-DBU | REV. A

DRB 108A

ML01

FIND NO.	DRAWING NO.	DESCRIPTION	TYPE
19	D-IA-7022302-0-DBU	PANEL, SIDE L/H WELDMENT	M
	K-PL-7022302-0-DBP	PANEL, SIDE L/H WELDMENT (PL)	M
	E-MD-7431042-0-DBU	PANEL, LEFT	M
	B-MD-7431190-0-DBU	BRACKET STUD SIDE PANEL	M
20	D-AD-7022001-0-DBU	SIDE PANEL ASSEMBLY R/H	M
	K-PL-7022001-0-DBP	SIDE PANEL ASSEMBLY R/H (PL)	M
21	D-IA-7022303-0-DBU	PANEL, SIDE R/H WELDMENT	M
	K-PL-7022303-0-DBP	PANEL, SIDE R/H WELDMENT (PL)	M
	D-MD-7430702-0-DBU	PANEL SIDE	M
	B-MD-7431190-0-0	BRACKET, STUD SIDE PANEL	M
22	D-AD-7022296-0-DBU	FAN MOUNT MASS STORAGE ASSY	M
	K-PL-7022296-0-DBP	FAN MOUNT MASS STORAGE ASSY (PL)	M
	D-MD-7430711-0-DBU	BRACKET, FAN MOUNT MASS STORAGE	M
23	D-AD-7022003-0-DBU	FAN MOUNT CARD CAGE ASSY	M
	K-PL-7022003-0-DBP	FAN MOUNT CARD CAGE ASSY (PL)	M
	D-MD-7430694-0-DBU	BRACKET, FAN MOUNT CARD CAGE	M
24	A-PA-3700821-0-0	PACKAGING ASSY	M
	K-PL-3700821-0-DBP	PACKAGING ASSY (PL)	M

FIND NO.	DRAWING NO.	DESCRIPTION	TYPE
25	D-AD-7022339-0-DBU	DOOR, REAR ASSY	M
	K-PL-7022339-0-DBP	DOOR, REAR ASSY (PL)	M
	E-IA-7431043-0-DBU	DOOR, REAR	M
	K-PL-7431043-0-DBP	DOOR, REAR (PL)	M
	E-IA-7430703-0-DBU	PANEL, REAR	M
	K-PL-7430703-0-DBP	PANEL, REAR (PL)	M
	D-MD-7431188-0-DBU	HINGE, REAR DOOR LINING	M
26	B-DD-5416665-0-0	REMOTE OF SENSE TEMPERATURE	E/M

TYPE: E ELECTRICAL
M MECHANICAL
E/M ELECTRO/MECHANICAL

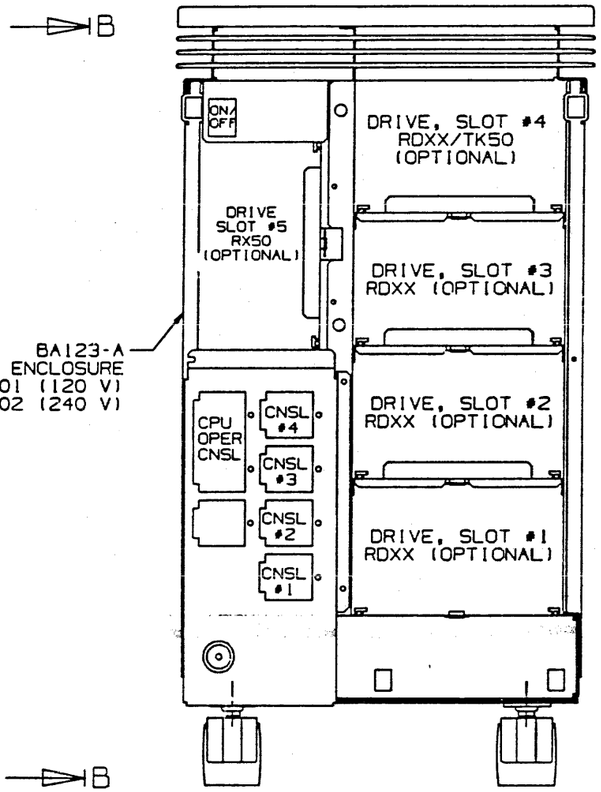
digital

TITLE: BA123-A BASIC ENCLOSURE

SHEET	SIZE	CODE	NUMBER	REV.
SHEET 6 OF 6	B	DD	7022380-0-DBU	A

DRB 108A

ML01



VIEW A-A
(SEE SHEET 2)
SHOWN WITHOUT FRONT
OR SIDE PANELS

NOTES:

1. RQDX SIGNAL DISTRIBUTION (M9058) IS SHOWN FOR REF ONLY AND NOT PART OF BA123-A. (SEE SHEET 5)
2. FOR REAR PANEL RULES AND CONFIGURATION SEE SHEET 3.
3. FOR POWER HARNESS WIRING DIAGRAM SEE SHEET 6.
4. FOR MODULE RULES SEE SHEET 6.
5. MASS STORAGE CONFIGURATION RULES:
   THE POWER SUPPLY IN THE BA123-A ENCLOSURE CAN POWER UP TO FOUR OF THE FIVE DRIVE SLOTS ONLY.
   THE FOLLOWING ARE SOME OF THE COMBINATIONS:
   - (4) RD52'S
   - RX50, TK50, (2) RD52'S
   - TK50, (3) RD52'S

FILE NAME: AR7022380-0-DBUA

PLOT AT .5000

REVISIONS		
CHK	CHANGE NO.	REV.
	INITIAL	A

FIRST HIGHER ASS'Y: D-AD-BA123-A-D8P

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND THE FOLLOWING TOLERANCES APPLY (PER DEC STD 114)

QUANTITY & VARIATION

THIRD ANGLE PROJECTION

DO NOT SCALE DRAWING

REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL //

FINISH //

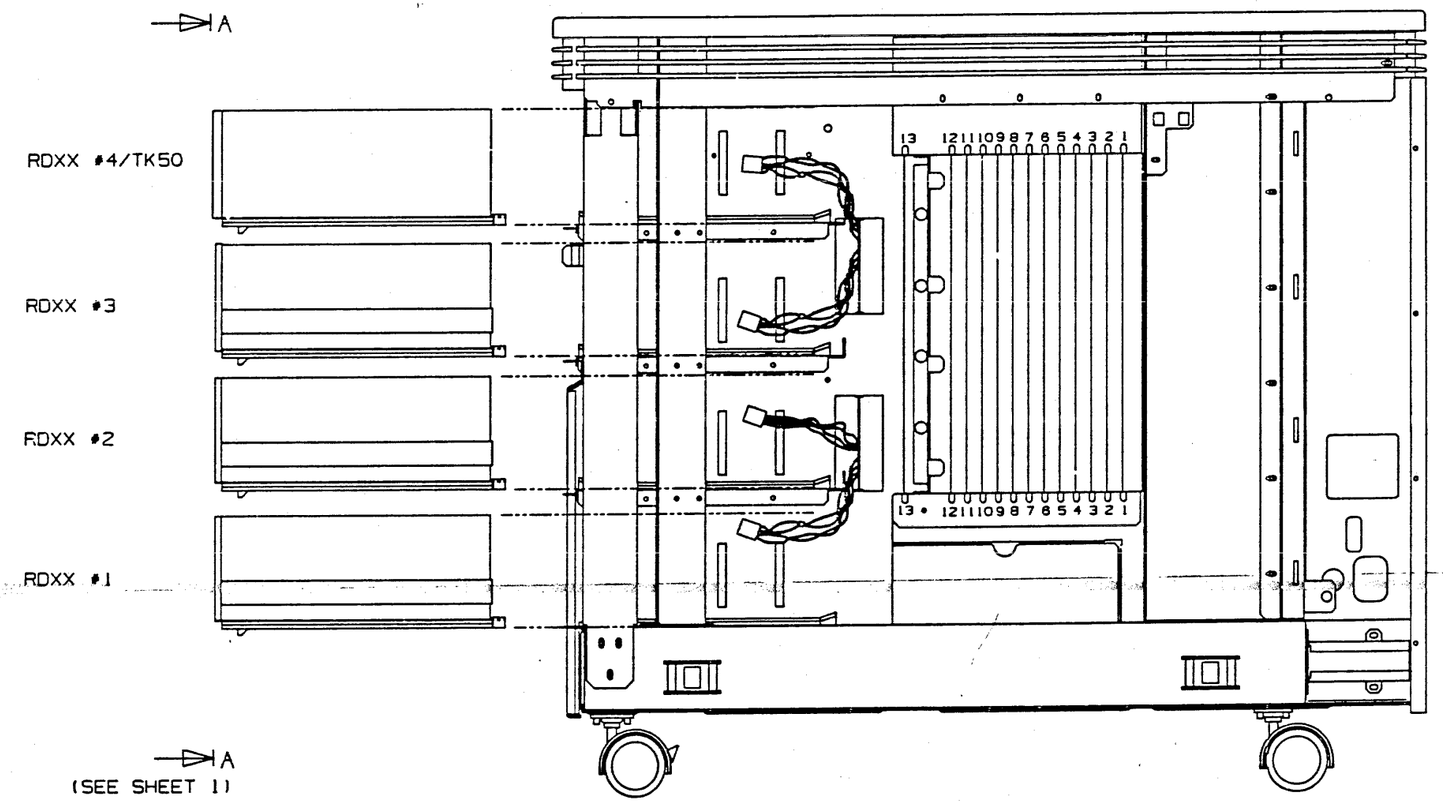
DRN	B. LAPOCHE	08-JAN-85
CHK'D	D. HEALY	08-MAR-85
DES. ENG.	J. KWONG	08-MAR-85
RESP. ENG.	J. KWONG	08-MAR-85
MFG. ENG.	J. EDWAROS	08-MAR-85
TOP DOC.	D-AR-7022380-0-DBU	

TITLE: BA123-A SYSTEM ARRANGEMENT

DOCUMENT NUMBER: SIZE D | CODE AR | NUMBER 7022380-0-DBU | REV. A

SCALE 1/2 | SHEET 1 OF 6

ML01



VIEW C-C
(SEE SHEET 1)
SHOWN WITHOUT FRONT
OR REAR PANELS

PLOT AT .5000

REVISIONS		
CHK	CHANGE NO	REV

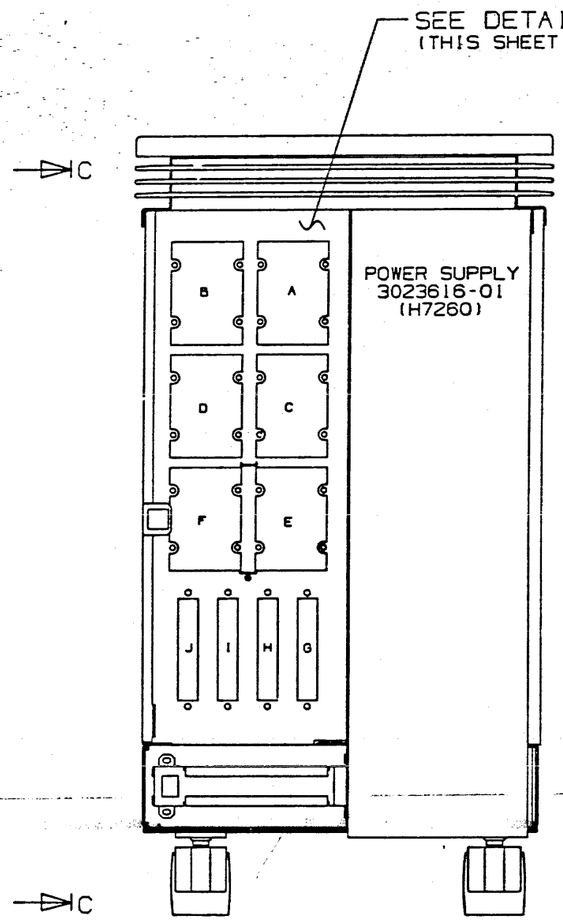
TITLE	BA123-A SYSTEM ARRANGEMENT		
SCALE 1/2	SHEET 2 OF 6	DIST	
SIZE	CODE	NUMBER	REV
D	AR	7022380-0-DBU	A

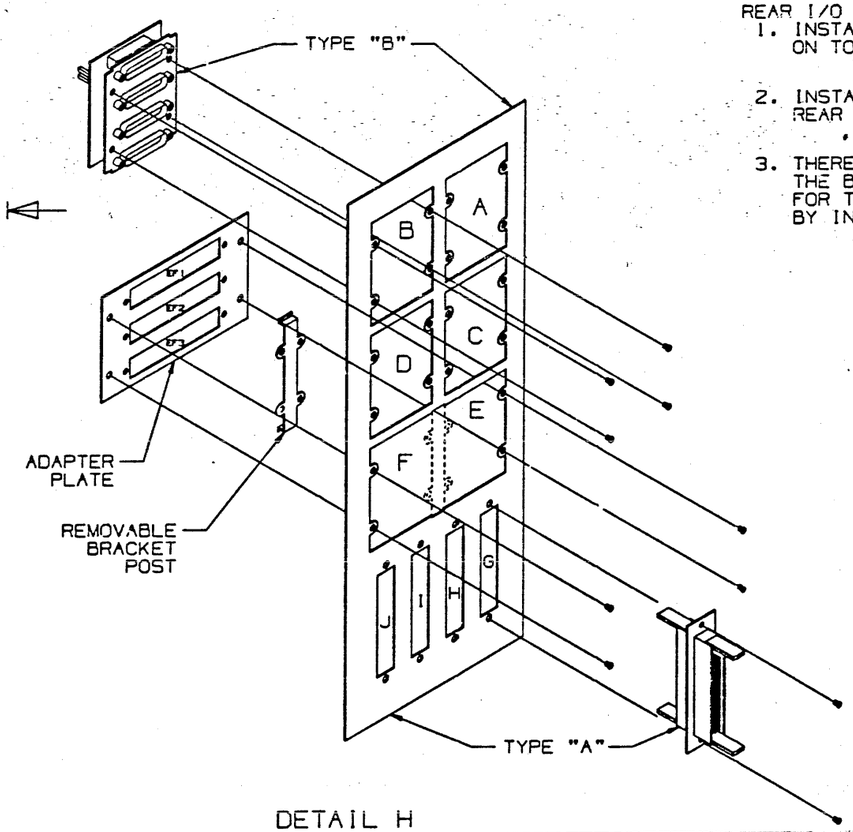
ML01

NOTES:

REAR I/O PANEL CONNECTION RULES:

1. INSTALL TYPE "B" (2.5" X 3.2") FILTER PANEL ON TO THE REAR I/O PANEL IN THIS SEQUENCE:
   A→C→E→B→D→F
2. INSTALL TYPE "A" (1 X 4) FILTER PANEL ON TO REAR I/O PANEL IN THIS SEQUENCE:
   G→H→I→J
3. THERE IS A REMOVABLE BRACKET POST BETWEEN THE BOTTOM 2 TYPE "B" CUTOUTS. THIS ALLOWS FOR THE ADDITION OF 3 MORE TYPE "A" CUTOUTS BY INSTALLING AN ADAPTER PLATE (7427720-01)





DETAIL H

SEE NOTES THIS SHEET FOR REAR I/O PANEL RULES

C (SEE SHEET 2)

B (SEE SHEET 4)

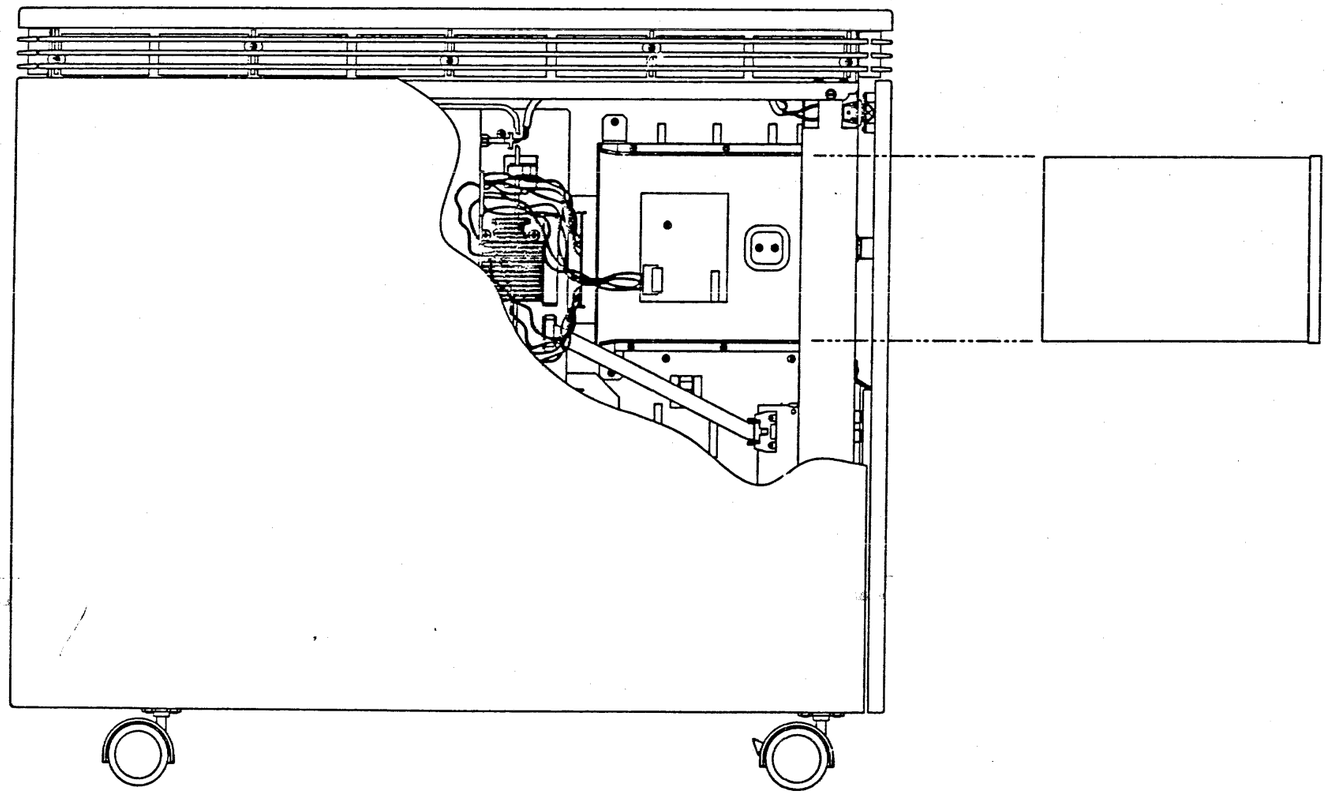
VIEW D-D
(SEE SHEET 2)
SHOWN WITHOUT REAR OR SIDE PANELS

PLOT AT .5000

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
BA123-A SYSTEM ARRANGEMENT	D	AR	7022380-0-DBU	A
SCALE 1/2	SHEET 3 OF 8		DIST	

MLG1



VIEW B-B
(SEE SHEET 1)
(TK50 INSTALLATION)

REVISIONS		
CHK	CHANGE NO	REV

PLOT AT .5000

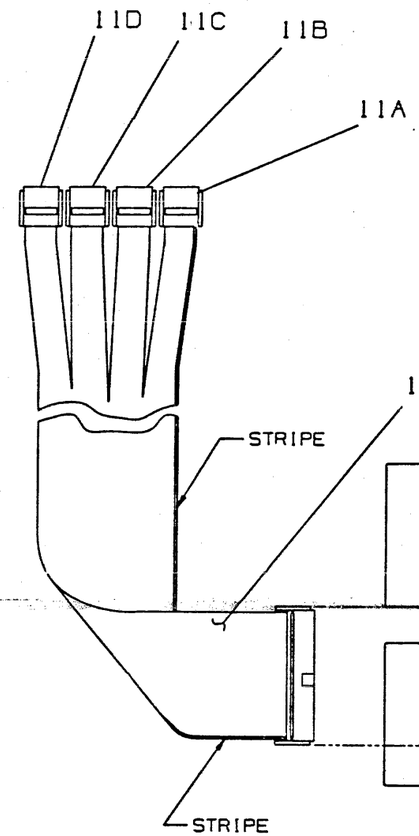
TITLE	SIZE	CODE	NUMBER	REV
BA123-A SYSTEM ARRANGEMENT	D	AR	7022380-0-DBU	A
SCALE 1/2	SHEET 4 OF 6	DIST		

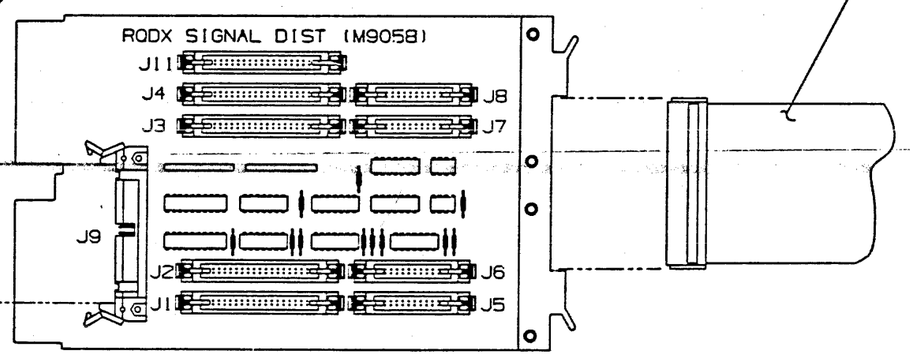
ML01

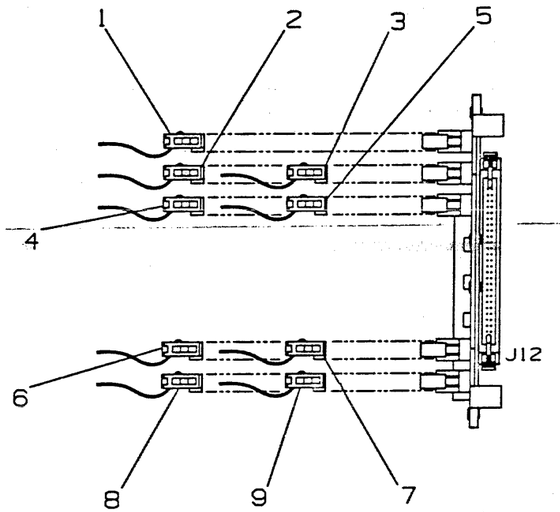
CABLE LEGEND			
ITEM	PART NO.	FROM	TO
1	1700867-01	M9058-J11	RX50
2	1700286-01	M9058-J4	RDXX#4
3	1700282-01	M9058-J8	RDXX#4
4	1700286-01	M9058-J3	RDXX#3
5	1700282-01	M9058-J7	RDXX#3
6	1700286-01	M9058-J2	RDXX#2
7	1700282-01	M9058-J6	RDXX#2
8	1700286-01	M9058-J1	RDXX#1
9	1700282-01	M9058-J5	RDXX#1
10	1700861-01	M9058-J12	RODX2 MODULE
11	1700862-01	M9058-J9	SEE BELOW
11A	↕	↕	RDXX#1 CONSOLE
11B	↕	↕	RDXX#2 CONSOLE
11C	↕	↕	RDXX#3 CONSOLE
11D	1700862-01	M9058-J9	RDXX#4 CONSOLE

NOTES:

1. ITEM #S SHOWN ARE FOR REF ONLY (FOR CABLE HOOK UP ONLY).





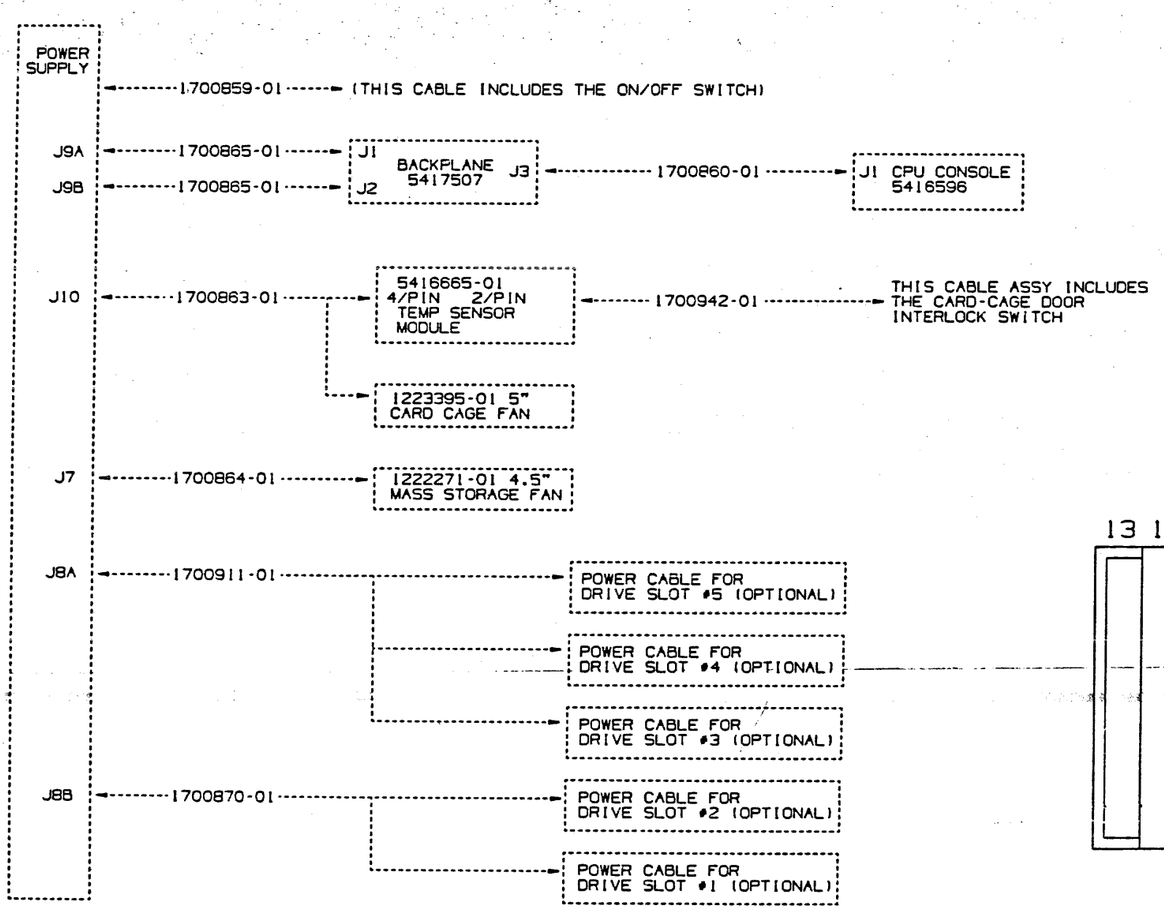


REVISIONS		
CHK	CHANGE NO	REV

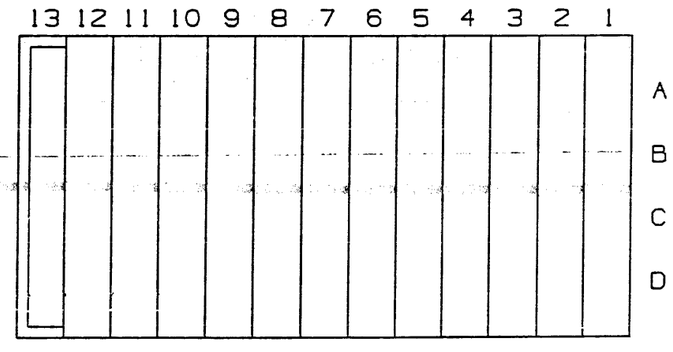
PLOT AT 1.000

TITLE	SIZE	CODE	NUMBER	REV
BA123-A SYSTEM ARRANGEMENT	D	AR	7022380-0-DBU	A
SCALE 1/1	SHEET 5 OF 8		DIST	

ML01



BA123-A BASIC ENCLOSURE
POWER HARNESS WIRING DIAGRAM



BACKPLANE MODULE
UTILIZATION- SEE RULES
THIS SHEET

NOTES:

BACKPLANE CONFIGURATION RULES

WHEN CONFIGURING THE BACKPLANE, THE FOLLOWING RULES MUST BE REFERENCED:

1. ALL Q-BUS OPTIONS ARE INSTALLED BELOW THE CPU MODULE.
2. QUAD OPTIONS MAY BE INSTALLED ANYWHERE BELOW THE CPU MODULE.
3. DUAL OPTIONS CAN BE INSTALLED ANYWHERE BETWEEN SLOT 5-12 (i.e. AB OR CD ROWS) AND BETWEEN SLOT 1-4 ON THE AB ROWS BELOW THE CPU. NO DUAL OPTIONS MAY BE INSTALLED IN SLOTS 2 THROUGH 4 ON THE CD ROWS.
4. DUAL OPTIONS ALONE IN A SLOT REQUIRE A M9047 GRANT CARD ADJACENT TO THEM (A OR C ROWS).
5. SLOT 13 RESERVED FOR DIGITAL USE ONLY.

REVISIONS		
CHK	CHANGE NO	REV

PLOT AT 1.000

TITLE	SIZE	CODE	NUMBER	REV
BA123-A SYSTEM ARRANGEMENT	D	AR	7022380-0-DBU	A
SCALE 1/1	SHEET 6 OF 6		DIST	

ML01

SIZE	CODE	NUMBER	REV
B	DD	5417507-0-0	A

DRAWING NO.	NO. OF SHTS.	PART NO.	DESCRIPTION	REVISIONS
		5417507-01	BACKPLANE BA123-A	A1
E-UA-5417507-0-0	1		BACKPLANE BA123-A	A
K-PL-5417507-0-DBP	1		BACKPLANE BA123-A	A
B-DD-5017506-0-0	1		DRAWING DIRECTORY	A

NOTES:

REVISION HISTORY

REV.	ECO NO.	DATE
A	INIT	2/85

digital

USED ON OPTION/MODEL

DRN. [illegible]	DATE 26 SEP 84	TITLE BACKPLANE BA123-A
CHK'D [illegible]	DATE 9-26-84	
DES. ENG. [illegible]	DATE [illegible]	DOCUMENT NUMBER
RESP. ENG. [illegible]	DATE [illegible]	SIZE B CODE DD NUMBER 5417507-0-0 REV A
MFG. ENG. R. BELIVEAU	DATE 3/1/85	SHEET 1 OF 1

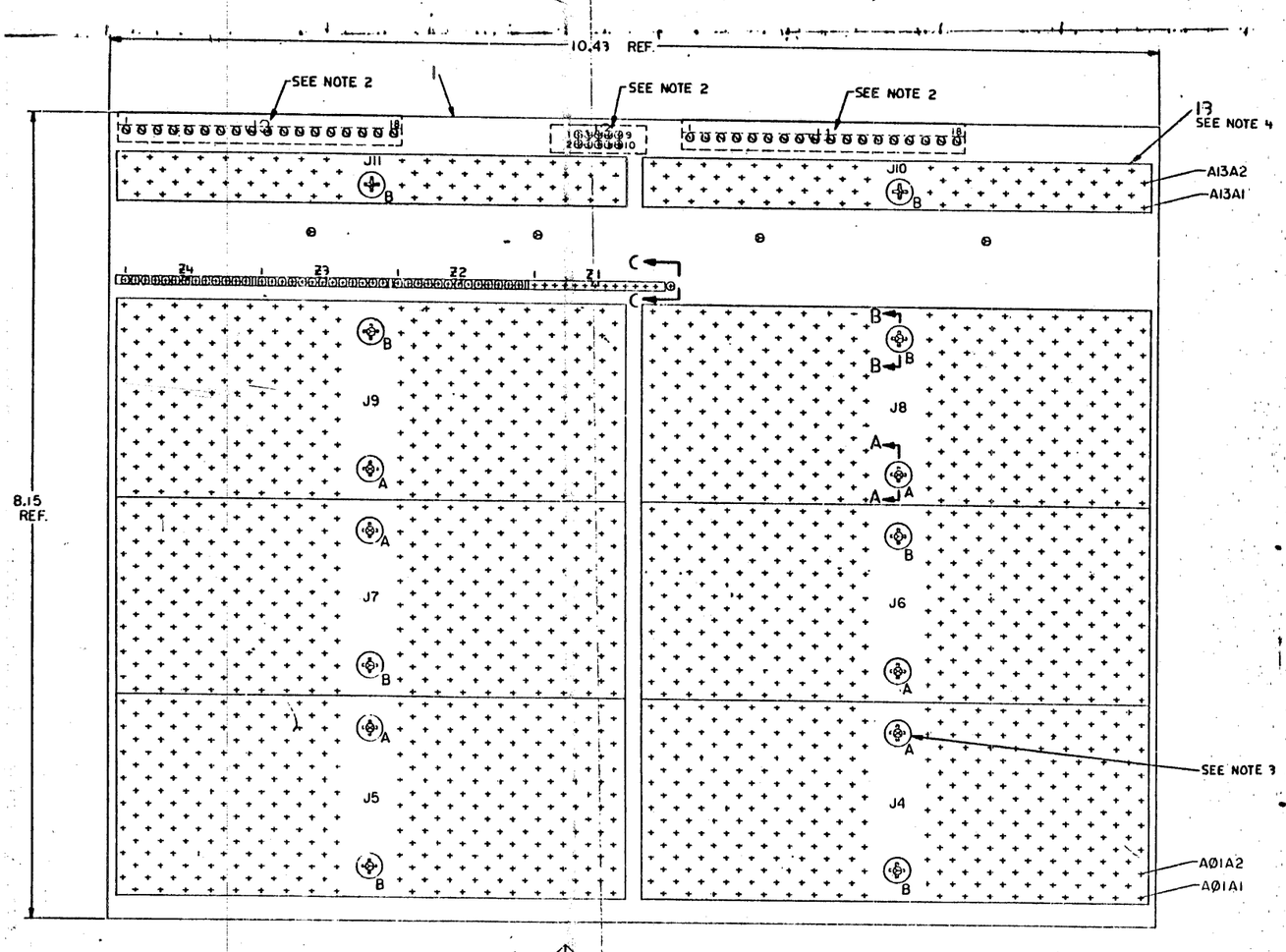
DRB 126A

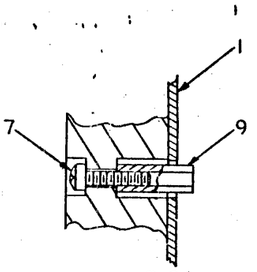
AUTOMATED BY PRTLST.5R(55)

P A R T S L I S T

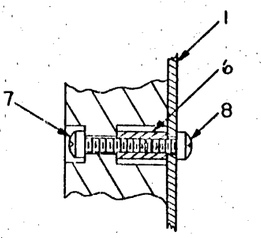
LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION 01	REFERENCE DESIGNATOR
					VARIATION REVISION LEVEL:	A1	
1	1	D-MD-5017506-0-0	5017506-01		ETCHED BOARD	1	
2	2		1214886-05		PCB HEADER 10POS(2X 5).100CC	1	J2
3	3		1215699-07		PCB,HEADER 18POS(1X18).156CC STR	2	J1,J3
4	4		1217535-05		SKT,IC 13PIN SIP TIN SOLD	4	XZ1-XZ4
5	5		7417041-00		288 PIN CONNECTOR	6	J4-J9
6	6		9000033-12		SPACER,THREADED HEX ALUM 8-3	6	
7	7		9006120-06		SCREW, FILL POZI 8-	14	
8	8		9006035-01		SCREW,MACH PAN PHIL 8-	6	
9	9		9009246-00		SPACER,THREADED HEX ALUM 8-3	8	
10	10		7411881-01		DECAL	1	
11	11		1323505-01		R NETWORK 180/390 2.0 % 13PIN	4	Z1-Z4
12	12		7417042-00		72 PIN CONNECTOR	2	J10-J11
13	13		3623593-01		LABEL,BLANK,PAPER,PIN FEED	1	
14	14		9905016-03		CARTON,DIE CUT,SELF LOCK W/FOAM	1	

REVISION HISTORY			BASIC PART NO: 5417507			
ENG	ECO NUMBER	REV	SECTION A OF A			
---	INITIAL	A	SECTION.VARIATION INDEX [A] 01 [B] [C] [D] [E] [F] [H] [J] [K] [L] [M] [N]	DRN: S.MANSOR	DATE: 07-JUN-84	D I G I T A L
				CHK'D: F.GAROFALO	DATE: 1-MAR-85	TITLE PARTS LIST 13 SLOT BACKPLANE
				DES.ENG: T.ORR	DATE: 1-MAR-85	DOCUMENT NUMBER
				RESP.ENG.: T.ORR	DATE: 1-MAR-85	SIZE K / CODE PL / NUMBER 5417507-0-DBP / REV A
				MFG.ENG.: R.BELIVEAU	DATE: 1-MAR-85	RELEASE DATE: 04-MAR-85
				ASSEMBLY NUMBER: E-UA-5417507-0-0	TOP DOCUMENT NUMBER: B-DD-5417507-0-0	FILE NAME: TW261A.PLS / EDIT # 4

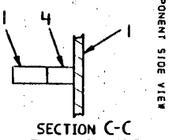




SECTION B-B
TYP. 8 PLACES (MARKED "B")
SCALE 2/1



SECTION A-A
TYP. 6 PLACES (MARKED "A")
SCALE 2/1



SECTION C-C
TYP 4 PLACES
NOT TO SCALE

COMPONENT SIDE VIEW

NOTES:
UL RATING IS HPWR.
INSTALL J1, J2, J3 ON SIDE 2.
REMOVE ITEM 8 (SCREW LABELED "A") AFTER WAVE SOLDER.
STICK LABLE ON "J10"

P E	+ Y AXIS	STEP	LINES
CRT	± X AXIS	STEP	LINES

CHG/CHANGE NO. REV.

ETCH REV. D

SIGNATURES	DATE
DRN.	7-5-84
CHK. D.	7-5-84
MECH. ENG.	8/15/84
PROJ. ENG.	8/15/84
PROD. R. DELIVEAU	9/1/84

SCALE 1/1
SHT. 1 OF 1
NEXT HIGHER ASSY. B-DD-5417507-0-0

digital

TITLE BACKPLANE BA123-A

SIZE	CODE	NUMBER	REV
E	UA	54,7507-0-0	A

SIZE	CODE	NUMBER	REV
B	DD	5416596-0-0	B

DRAWING NO.	NO. OF SHTS.	PART NO.	DESCRIPTION	REVISIONS																	
		5416596-01	BA123-A FRONT PANEL	A1	A2																
D-UA-5416596-0-0	1		BA123-A FRONT PANEL	A	A																
D-CS-5416596-0-1	1		BA123-A FRONT PANEL	A	A																
K-PL-5416596-0-DBP	1		BA123-A FRONT PANEL	A	B																
K-PC-5416596-0-DBC			P.C. DESIGN DATA BASE	A	A																
		5016595-01	ETCHED CIRCUIT BOARD	B1	B1																
B-DD-5016595-0-0	1		DRAWING DIRECTORY	A	A																
K-SP-5416596-0-DBF	6		BA123-A FRONT PANEL	A	A																

NOTES:

REVISION HISTORY																					
REV.	A	B																			
ECO NO.	INIT	ML001																			
DATE	6-84	5-85																			

digital

DRN. B.LENNON	DATE 27JUN84	TITLE: BA123-A FRONT PANEL
CHK'D R.BARRIERE	DATE 27JUN84	
DES. ENG. J.PADGETT	DATE 27JUN84	DOCUMENT NUMBER
RESP. ENG. J.PADGETT	DATE 27JUN84	SIZE B / CODE DD / NUMBER 5416596-0-0 / REV B
MFG. ENG. R.BELLIVEAU	DATE 27JUN84	SHEET 1 OF 1

DRB 126C
EN-01242-16-REVA(396)

AUTOMATED BY PRTLST.5R(55)

P A R T S L I S T

LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION 01	REFERENCE DESIGNATOR
					VARIATION REVISION LEVEL:	A2	
1	1	D-MD-5016595-0-0	5016595-01		CIRCUIT DRILL AND ETCH	1	
2	2		1000021-00		220.0 MMF 100V 5%200PPM MICA	1	C1
3	3		1005636-00		22 MFD 6V 10% S.TANT	1	C2
4	4		1012784-00		.047 MFD 50V +80-20% CER	2	C3,C4
5	5		1012312-01		.47 MFD 50V +80-20% CER	1	C5
6	6		1017472-00		10 MFD 35V +75-10% AL EL	1	C6
7	7		1100114-00		PIV= 25 IO=135 MA	1	D1
8	8		1119827-01		LED,SUPERBRIGHT,RED T1 PKG	1	D2
9	9		1116622-02		LED 2.0MCD@25M	1	D3
10	10		1121248-01		GREEN LED T1 4MCD 1"LEADS	1	D4
11	11		1110864-00		LED 2MCD@10MA	2	D5,D6
12	12		1218945-03		SW,PB,LT 1PST NO-MOMENTARY .25A	1	S1
13	13		1218945-01		SW,PB,LT 1PST NO-MAINTAIN .25A	1	S2
14	14		1217310-07		SW,DIP 2POS/1PST 5VDC100MA S	1	S3
15	15		1216832-07		*** THIS ITEM IS NOT USED ***	-	
16	16		1219918-01		SKT,SWITCH 4PIN RT ANGLE	2	XS1,XS2
17	17		1300250-00		150.0 .25 W 5.0 % CF	1	R1
18	18		1311523-00		110.0 .25 W 5.0 % CF	1	R2
19	19		1300271-00		220.0 .25 W 5.0 % CF	1	R3
20	20		1302388-00		2.0 K .25 W 5.0 % CF	4	R4,R5,R6,R7
21	21		1300479-00		10.0 K .25 W 5.0 % CF	4	R10-R13
22	22		1302514-00		39.0 K .25 W 5.0 % CF	2	R14,R15
23	23		1302466-00		100.0 K .25 W 5.0 % CF	1	R16
24	24		1300391-00		1.50 K .25 W 5.0 % CF	2	R8,R9
25	25		1914987-00		8641-2 TRANSCEIVER,UNIBUS,QU	1	E1
26	26		1912858-00		LS221 ONE SHOT-DUAL,SCHMIT	1	E2
27	27		1914156-01		LM 393AN VOLT COMPARATOR,DUA	1	E3
28	28	D-MD-7430089-0-DBU	7430089-01		HOLDER,L.E.D.,SINGLE	1	
29	29		1209941-05		PCB,HEADER 10PIN(2X10).100CC 90D	1	J1
30	30		1209941-04		PCB,HEADER LATCH	1	

REVISION HISTORY		
ENG	ECO NUMBER	REV
JP	INITIAL	A
JP	5416596-ML001	B

BASIC PART NO: 5416596

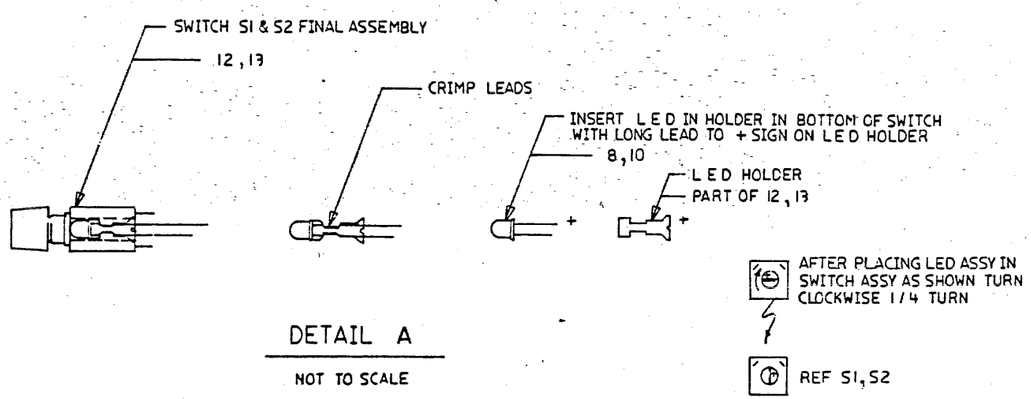
SECTION A OF A

SECTION.VARIATION INDEX
[A] 01
[B]
[C]
[D]
[E]
[F]
[H]
[J]
[K]
[L]
[M]
[N]

DRN: M. FUNARO	DATE: 16-MAR-84	D I G I T A L
CHK'D: D. BARRIERE	DATE: 16-MAR-84	TITLE PARTS LIST BA123-A FRONT PANEL
DES.ENG: J. PADGETT	DATE: 16-MAR-84	DOCUMENT NUMBER
RESP.ENG.: J. PADGETT	DATE: 16-MAR-84	SIZE: K / CODE: PL / NUMBER: 5416596-0-DBP / REV: B
MFG.ENG.: R. BELIVEAU	DATE: 18-MAY-84	RELEASE DATE: 01-MAY-85
ASSEMBLY NUMBER: D-UA-5416596-0-0	TOP DOCUMENT NUMBER: B-DD-5416596-0-0	FILE NAME: Z9241B.PLS / EDIT #: 15

LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION 01	REFERENCE DESIGNATOR
					VARIATION REVISION LEVEL:	A2	
31	31		1209941-03		PCB,HEADER LATCH	1	

D I G I T A L	TITLE BA123-A FRONT PANEL	SECTION A OF A	SIZE K	CODE PL	DOCUMENT NUMBER 5416596-0-DBP	REV B

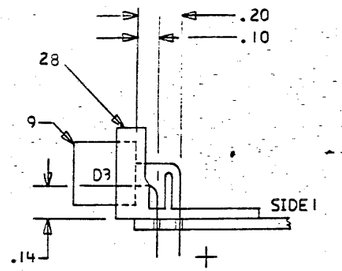


DETAIL A

NOT TO SCALE

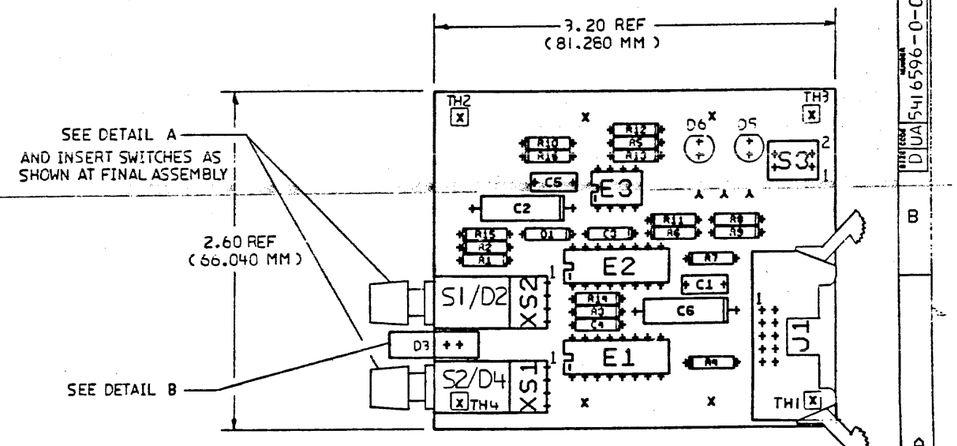
AFTER PLACING LED ASSY IN SWITCH ASSY AS SHOWN TURN CLOCKWISE 1/4 TURN

REF S1,S2



DETAIL B

NOT TO SCALE



NOTES: 1. THIS BOARD MEETS UL REQUIREMENT FOR LPMA.
2. COMPONENTS MOUNT ON SIDE 1.

CHK	CHANGE NO	REV

STEP E	↑ Y AXIS	STEP	TIMES
REPEAT	→ X AXIS	STEP	TIMES

ETCH REV. B1

SIGNATURES	DATE
DRN.	4/11/84
CHK'D.	4/16/84
MECH.ENG.	7/3/84
PROJ.ENG.	7/3/84
PROG	7/3/84

digital

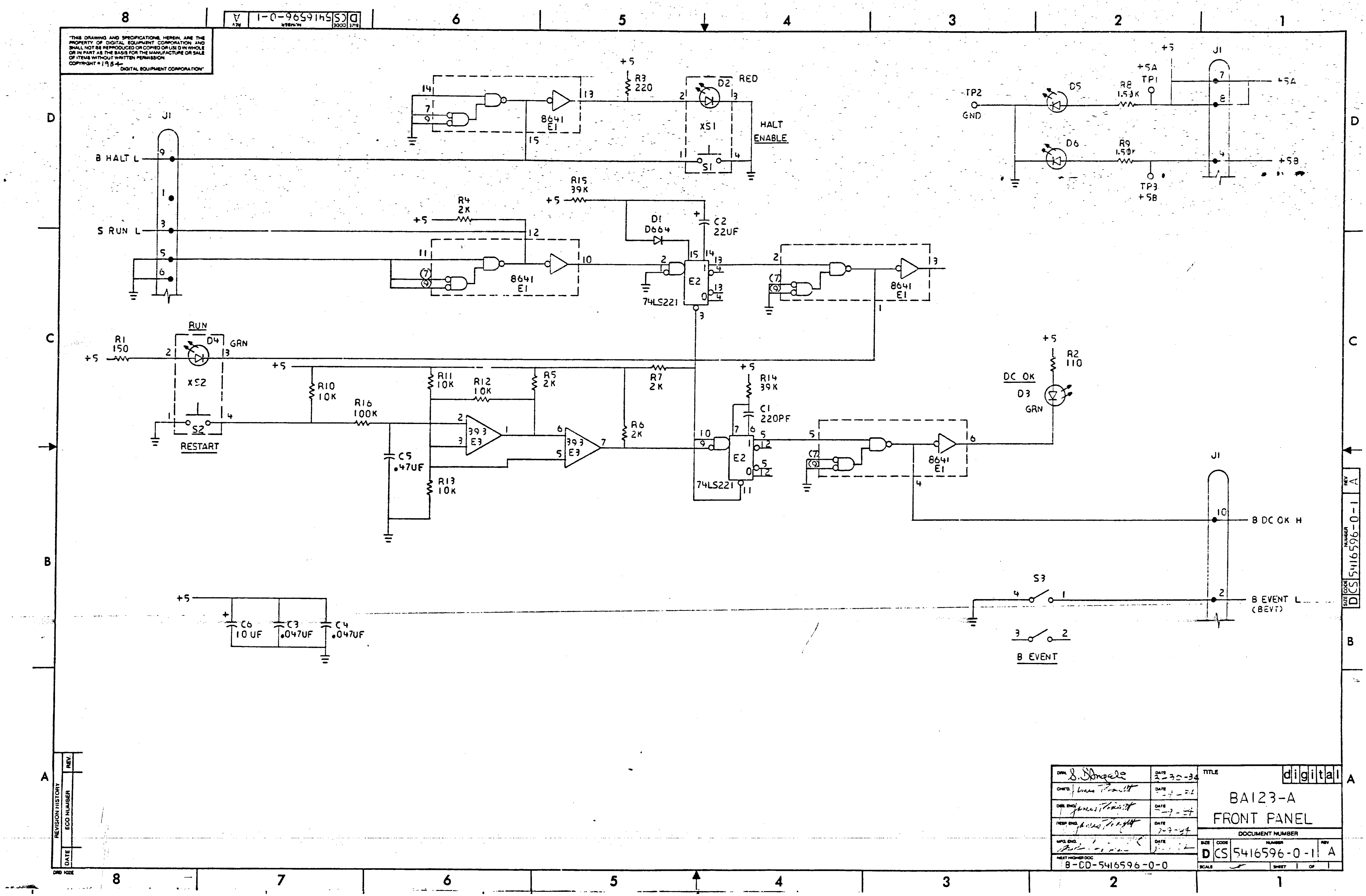
TITLE BA123-A FRONT PANEL

SCALE 2:1 | SIZE D | CODE UA | NUMBER 5416596-0-0 | REV A

SHT. 1 OF 1

TOP DOC NO. B-DD-5416596-0-0

MS#



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D CS 5416596-0-1 A
J1
B HALT L
S RUN L
8641 E1
R3 220
D2 RED
XS1
S1
HALT ENABLE
TP2 GND
D5
D6
R8 1.5K
R9 1.5K
TP1 +5A
TP3 +5B
+5A
+5B
R15 39K
R4 2K
D1 D664
C2 22UF
E2
74LS221
R1 150
RUN
D4 GRN
XS2
S2
RESTART
R10 10K
R11 10K
R12 10K
R5 2K
R7 2K
R16 100K
393 E3
C5 .47UF
R13 10K
R6 2K
R14 39K
C1 220PF
R2 110
DC OK
D3 GRN
B DC OK H
S3
B EVENT L (BEVT)
B EVENT
C6 10 UF
C3 .047UF
C4 .047UF
REVISION HISTORY
ECO NUMBER
DATE
REV.
BA123-A
FRONT PANEL
digital
DOCUMENT NUMBER
D CS 5416596-0-1 A
NEXT HIGHER DOC
B-CD-5416596-0-0
SHEET 1 OF 1

DRAWING DIRECTORY

ITEM	DRAWING NO.	NO. OF SHTS	PART NO.	DESCRIPTION	TYPE	REVISIONS
1			5416665-01	TEMP SENSOR BD.		A1 A1 A2
2	D-UA-5416665-0-0	1		TEMP SENSOR BD.		A B C
3	D-CS-5416665-0-1	1		TEMP SENSOR BD.		A A A
4	K-PL-5416665-0-DBP	1		TEMP SENSOR BD.		A A B
5	K-PC-5416665-0-DBC			P.C. DESIGN DATA BASE		A A A
6			5016664-01	ETCHED CIRCUIT BOARD		B1 B1 B1
7	B-DD-5016664-0-0	1		DRAWING DIRECTORY		A A A

NOTES:

DD REV A B C

REVISION HISTORY

ENG	ECO NUMBER	REV
	INITIAL	A
TO	5416665-ML001	B
RL	5416665-MK002	C

CONT. REVISION HISTORY

ENG	ECO NUMBER	REV

MADE BY: P.LENNON
DATE: 23-OCT-84

CHECKED BY: D. BARRIERE
DATE: 23-OCT-84

DESIGN ENGINEER: T. ORR
DATE: 23-OCT-84

RESPONSIBLE ENG: R. LIGENZA
DATE: 04-FEB-86

PRODUCTION ENG: NEMI HARRIS
DATE: 04-FEB-86

d i g i t a l

TITLE DRAWING DIRECTORY

TEMP SENSOR BD.

SIZE	CODE	DOCUMENT NUMBER	REV.
K	DD	K-DD-5416665-0	C

SHEET 1 OF 1 MKO

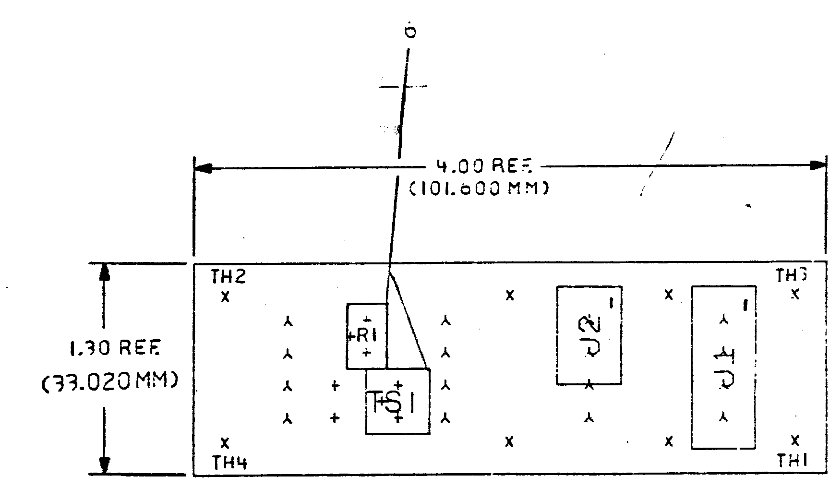
AUTOMATED BY VAXKPL (V1.0)

P A R T S L I S T

SHEET A1 OF A1

LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VAR/REV 01	QTY PER VAR/REV A2	REFERENCE DESIGNATORS
1	1	D-MD-5016664-0-0	50-16664-01		CIRCUIT DRILL & ETCH	1		
2	2		13-24146-01		*** THIS ITEM IS NOT USED ***	-		
3	3		12-23681-03		THERMOSTAT,NO C@ 50C	1		TS1
4	4		12-11342-04		MATE-N-LOK 04PIN(1X04).200CC HDR	1		J1
5	5		12-11342-02		MATE-N-LOK 02PIN(1X02).200CC HDR	1		J2
6	6		90-07254-00		TRANSIPADS #10146	2		
7	7		13-25634-01	A	THERMISTOR,EPOXY COATED,5000HM 5	1		R1

REVISION HISTORY			KPL MODULE FORMAT	SECTION A OF A	DRN: T. ORR	DIGITAL
ENG	ECO NUMBER	REV	SECTION/VARIATION INDEX		DATE: 25-OCT-84	
TO RL	INITIAL 5416665-MK002	A B	[A] 01 [M] [B] [N] [C] [P] [D] [Q] [E] [R] [F] [S] [H] [T] [J] [V] [K] [W] [L] [Y]		CHK'D: D. BARRIERE DATE: 25-OCT-84 DES.ENG: T. ORR DATE: 25-OCT-84 RESP.ENG.: T. ORR DATE: 25-OCT-84 MFG.ENG: B. LAIDMAN DATE: 25-OCT-84	TITLE PARTS LIST TEMP SENSOR BD DOCUMENT NUMBER SIZE: K CODE: PL NUMBER: 5416665-0-DBP REV: B RELEASE DATE: RELEASE STATUS: UNDER CHANGE
			BASIC PART NUMBER: 5416665	ASSEMBLY NUMBER: D-UA-5416665-0-0	TOP DOCUMENT NUMBER: B-DD-5416665-0-0	FILE NAME: MK1283.PLS EDIT #: 2



NOTES:
1: ON SIDE ONE, IDENTIFY POINT OF MANUFACTURE, DATE CODE AND REVISION

STEP & REPEAT		
STEP E	↑ Y AXIS ______ STEP ___ TIMES	
REPEAT	→ X AXIS ______ STEP ___ TIMES	

REV	CHANGE NO	CHK
A	INIT	10/84
B	54-16665-ML001 WEINBERG J PADGETT	6/85 6/88
C	5416665-MK003 A.KRAWIECKI R.LIGENZA	5-86

ETCH REV. B1

SIGNATURES	DATE
DRN.	
CHK'D	
MECH.ENG. J. Padgett	
PROJ.ENG. J. Padgett	
PROD.	
SCALE 2:1	
SHT. 1 OF 1	

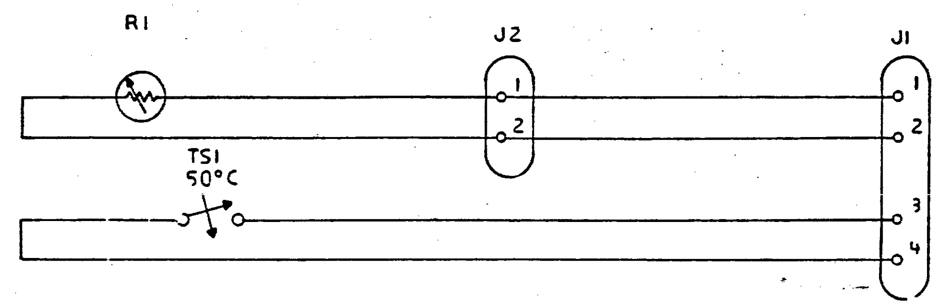
digital

TITLE TEMP SENSOR BD.

SIZE	CODE	NUMBER	REV
D	JA	5416665-0-0	C

TOP DWG.NO. B-DD-5416665-0-0

MS#1F2692B



DRN. S. D'Angelo	DATE 24 OCT 84	TITLE	digital
CHK'D. R. Bassine	DATE 24 OCT 84	TEMP SENSOR BD	
DES. ENG. J. Pruitt	DATE 13 OCT 84		
RESP. ENG. J. Pruitt	DATE 13 OCT 84	DOCUMENT NUMBER	
MFG. ENG.	DATE	SIZE D · CODE CS · NUMBER 5416665-0-1	REV. A
TOP DOC NO. B-DD-5416665-0		SCALE · SHEET · OF	

REVISION HISTORY | REV. | ECO NUMBER | DATE

D CS 5416665-0-1 A