EK-IEUQ1-UG-003

IEU11-A/IEQ11-A

User's Guide

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EK-IEUQ1-UG-003

IEU11-A/IEQ11-A

User's Guide

Prepared by
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Digital Equipment Corporation • Nashua, NH 03062

3rd Edition, November 1985

Printed in U.S.A.

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FIGURES

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TABLES (Cont)

INTENDED AUDIENCE

The IEU11-A/IEQ11-A User's Guide is for either the field service engineer or the user who must install, program, or maintain either the IEUII-A option or the IEQII-A option down to the Field Replaceable Unit (FRU) level.

DOCUMENT DESIGN

Chapter 1 provides general information about the IEU11-A option and the IEQ11-A option. This chapter contains a physical description, application examples, functional description, and general specifications.

Chapter 2 contains the installation procedure for both the IEU11-A option and the IEQ11-A option. There are two separate installation procedures: one for the IEU11-A option, which is installed in UNIBUS systems (VAX-11 and PDP-11), and another for the IEQ11-A option which is installed in Q-Bus systems (LSI-11, MICRO/PDP-11 and MICRO/VAX).

Chapter 3 provides programming information for both the IEU11-A option and the IEQ11-A option. This chapter defines the register bits for both the IEU11-A option and IEQ11-A option. Much of this chapter is taken from the TMS 9914A General Purpose Interface Bus (GPIB) Controller manual (published by Texas Instruments).

Chapter 4 contains guidelines in troubleshooting the IEU11-A option and the IEQ11-A option. There is a troubleshooting flowchart and references to the required diagnostics for both options.

RELATED DOCUMENTATION

The following documents contain information that is relevant to both the IEU11-A option and the IEQ11-A option.

Title	Document Number	Source
PDP-11 Bus Handbook	EB-17525-20	Available in hardcopy
IEU11-A Print Set	MP-01179	Shipped with the IEU11-A option
IEQ11-A Print Set	MP-01180	Shipped with the IEQ11-A option
PDP-11 Diagnostic Listing	AC-T064C-MC	Distributed by SDC
IEX11-A IEC/IEEE Bus Interfaces (A Service Information Guide)	EY-1064E-SG-001	Available in hardcopy

Title	Document Number	Source
*TMS 9914A General Purpose Interface Bus (GPIB) Controller		Published by Texas Instruments
DIN IEC625 Part 1		Published by DIN Deutsches Inst.fuer Normung E.V.
*IEEE Standard 488-1975-78		Published by The Institute of Electrical and Electronic Engineers

Additional copies of this document and printed copies of the documents listed above (except those documents marked with an {*}) may be obtained from:

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CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual describes two similar but distinct options: the IEU11-A option, and the IEQ11-A option. The IEU11-A option is a DMA controller that interfaces a UNIBUS system to two independent instrument buses (IEC/IEEE). The IEQ11-A option is a DMA controller that interfaces a Q-bus system to two independent instrument buses (IEC/IEEE). In both options the instrument buses conform to both the European Standard IEC 625-1 and the U.S. Standard IEEE 488-1978. Each instrument bus can have up to fifteen devices in a sequential configuration. The total of fifteen devices includes the option itself.

NOTE

The designation IEU11-A/IEQ11-A option is used to refer to both the IEU11-A option and IEQ11-A option simultaneously. This designation is used in this manual for convenience only, since the IEU11-A option and the IEQ11-A option are two distinct options.

Software drivers control and communicate with the IEU11-A/IEQ11-A option through programmed I/O transfers, DMA transfers, and interrupts. Programmed transfers are normally used for command bytes. DMA transfers are used for data bytes.

1.2 PHYSICAL DESCRIPTION

There are two kinds of options: the IEU11-A option, and the IEQ11-A option. The IEU11-A option is used in UNIBUS systems, such as the PDP-11 and VAX-11 systems. The IEQ11-A option is used in the Q-BUS systems, such as the LSI-11, MICRO/PDP-11 and MICRO/VAX systems.

NOTE

MICRO/PDP-11 systems and MICRO/VAX systems (both Q22-BUS and BA23 boxes) will, in the following document, be referred to as MICRO systems.

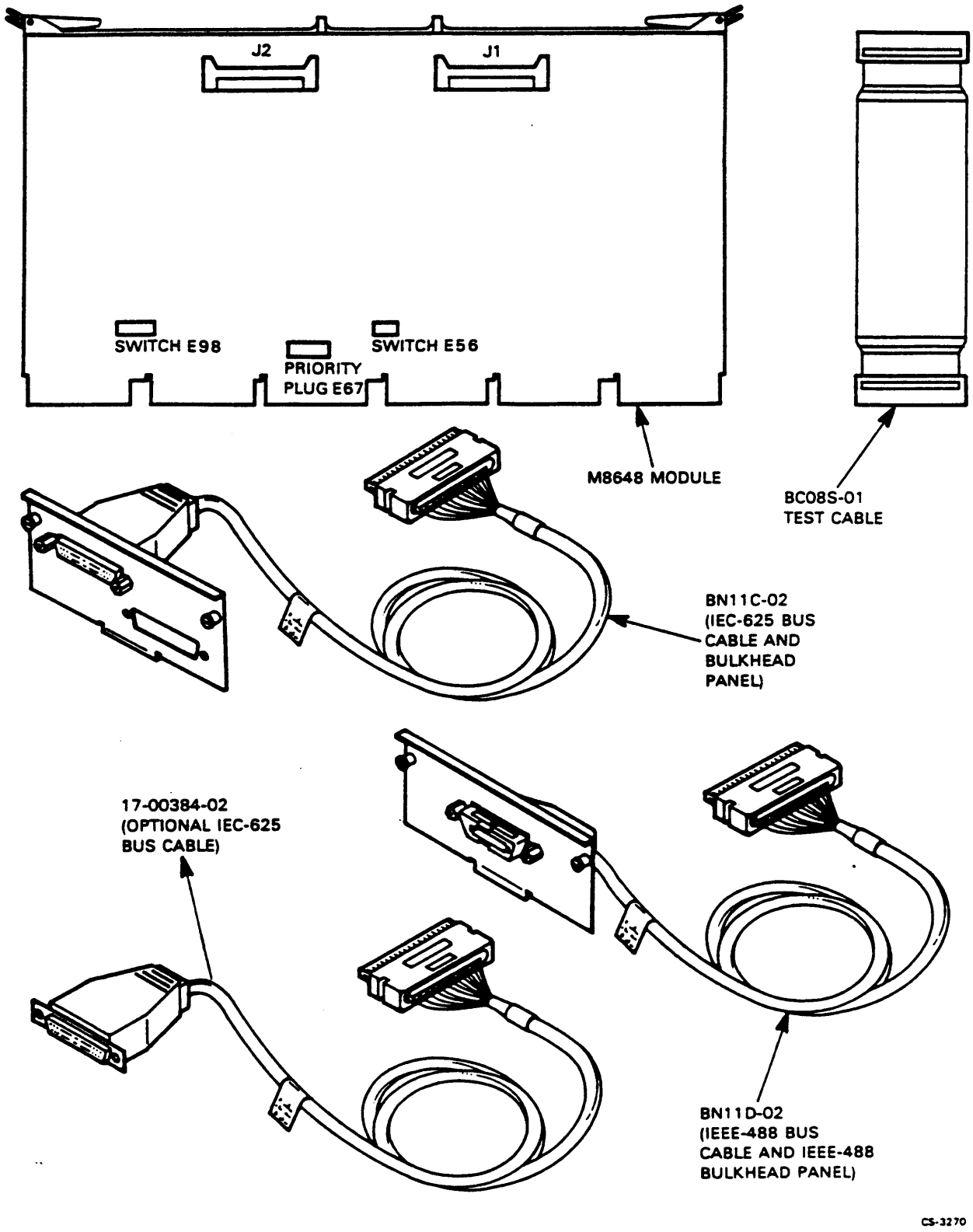


Figure 1-1A IEU11-A Option Components

1.2.1 IEU11-A Option Components

The IEU11-A option consists of one M8648 module and a BC08S-01 test cable. The type of cable and bulkhead panel depends on whether the option is used with an IEC bus or an IEEE bus. In an IEC bus installation, the IEC-625 bulkhead will hold an IEC bus cable (BN11C-02). Although it is shipped with only one cable, a second cable (17-00384-02) is optional. In an IEEE bus installation, the IEEE-488 bulkhead attaches to only one IEEE bus cable (BN11D-02). A second IEEE-488 bulkhead panel and IEEE bus cable combination (BN11D-02) is optional. The BC08S-01 test cable connects J1 and J2 connectors on the M8648 module when diagnostics are run to test the IEU11-A option. Refer to Figure 1-1A for the IEU11-A option components.

1.2.2 IEQ11-A Option Components

The IEQ11-A option consists of one M8634 module and a BC08S-01 test cable. The type of cable used with the bulkhead panel depends on whether the option is used with an IEC bus or IEEE bus. In an IEC bus installation, the C size IEC-625 bulkhead panel is used with one IEC bus cable (BN11E-01). The second bus cable (17-00384-01) is optional. In an IEEE bus installation, a C size IEEE-488 bulkhead panel is used with one IEEE-488 bus cable (BN11F-01). The second cable (70-20161-01) is optional. For the MICRO systems, a B-size IEEE-488 bulkhead panel is used with one IEEE-488 bus cable (BN11K-0C). The second cable (BN11L-0C) is optional. For IEC Bus applications, a B-size IEC 625-1 bulkhead panel is used with one IEC 625-1 bus cable (BN11J-0C). The second cable (BN11M-0C) is optional. The BC08S-01 test cable connects J1 and J2 connectors on the M8634 module when diagnostics are run to test the IEQ11-A option.

Refer to Figure 1-1B and Figure 2-13 for the IEQ11-A option components.

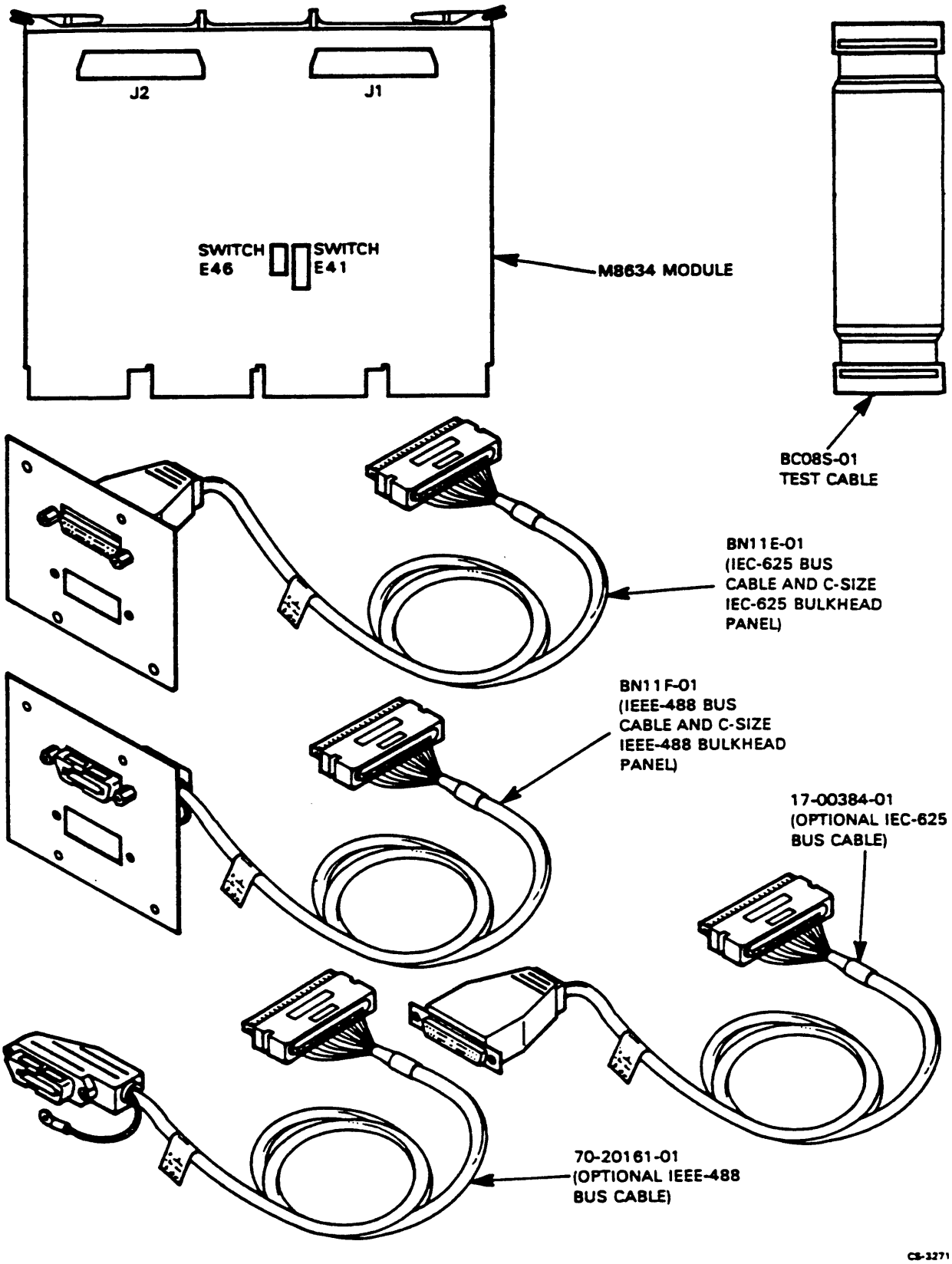


Figure 1-1B IEQ11-A Option Components

1.3 APPLICATION EXAMPLES

The IEU11-A/IEQ11-A option can be configured in numerous ways. Figure 1-2 shows an interprocessor link, while Figure 1-3 shows a multiple processor link.

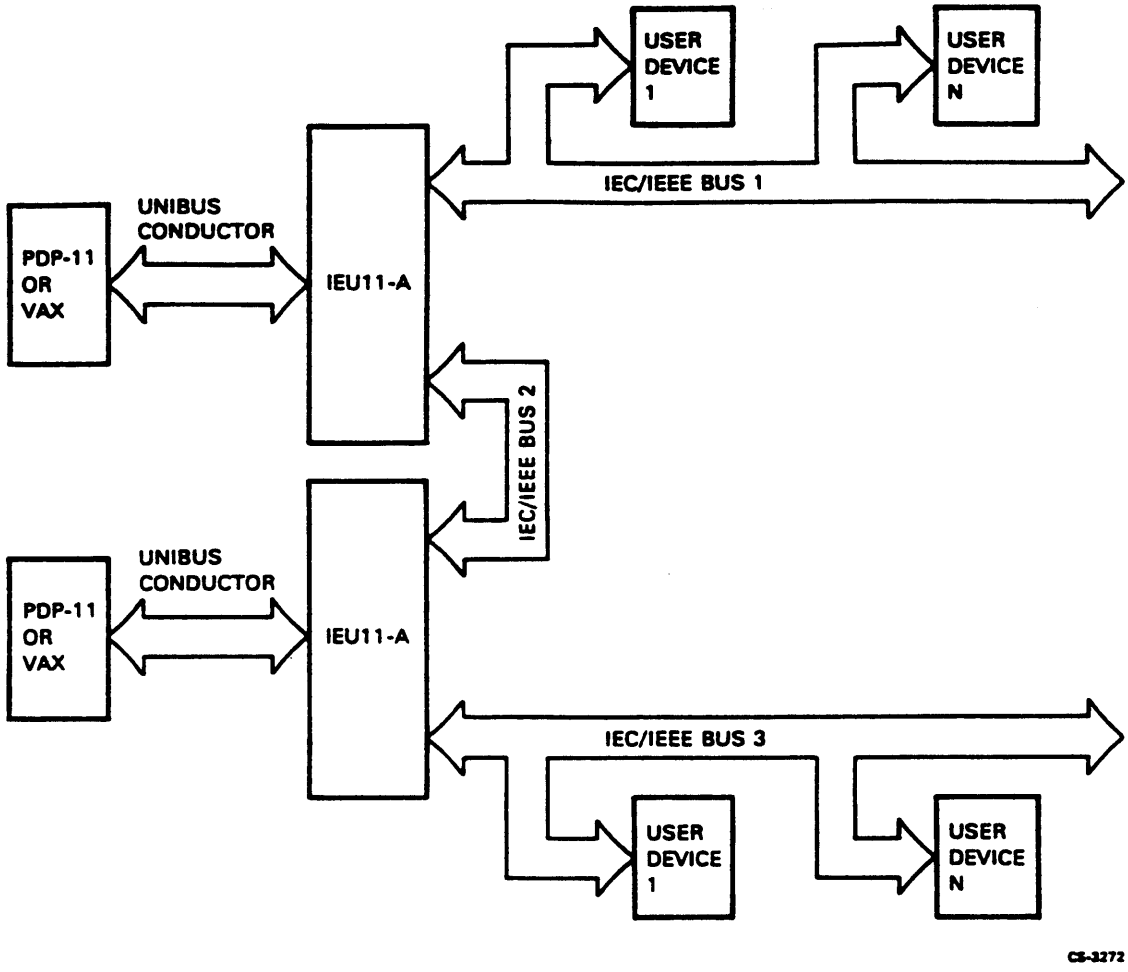


Figure 1-2 Interprocessor Link

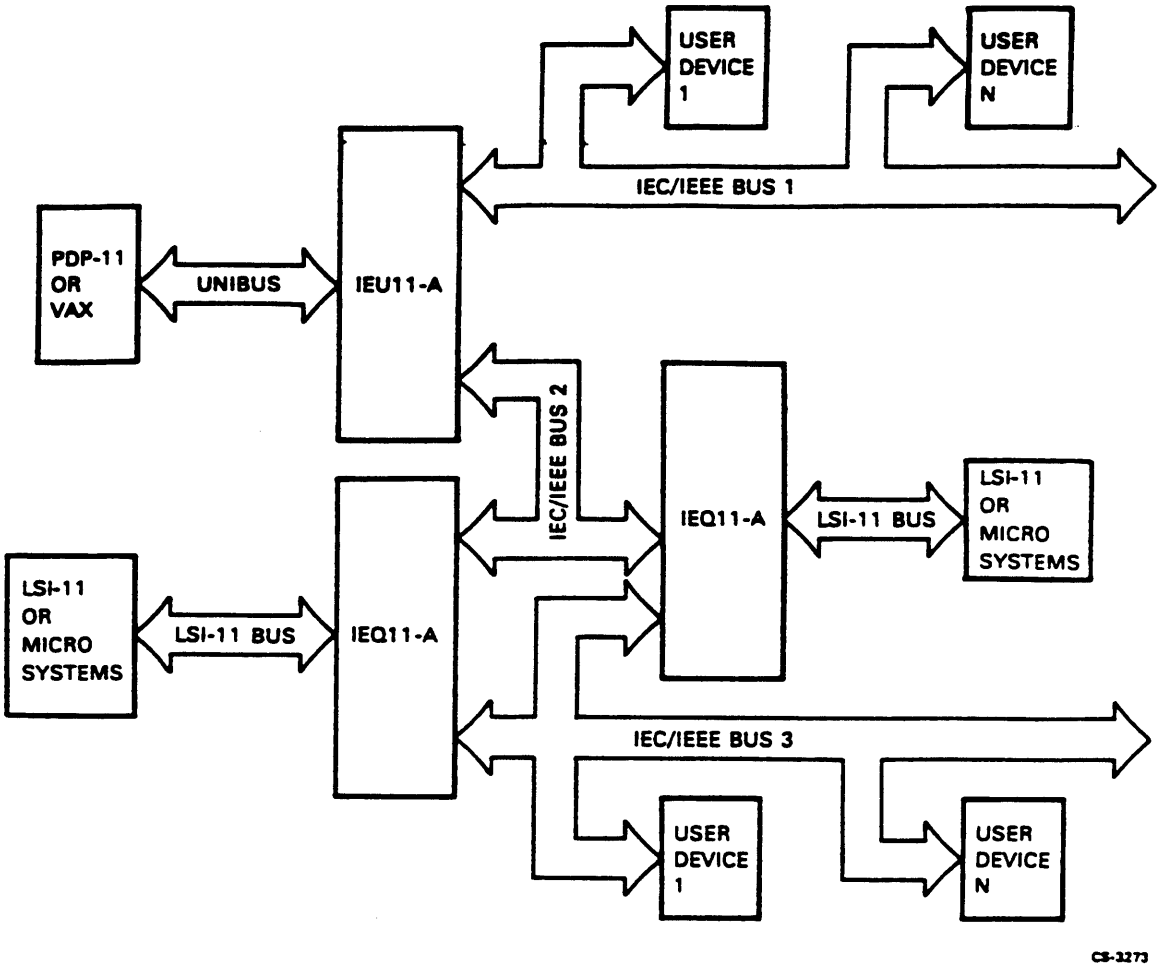


Figure 1-3 Multiple Processor Link

1.4 FUNCTIONAL DESCRIPTION

The IEC/IEEE bus, a standardized instrumentation bus, transfers digital data between a group of instruments and a computer system (see Figure 1-4). The data is transmitted in bit-parallel/byte-serial format. The data can consist of either interface messages or device dependent messages.

There are sixteen lines that are used to control and transmit messages between the devices. These lines are as follows: eight data lines, five interface management lines, and three handshaking lines. All data is transferred by means of the data lines (DIO <8:1>). Refer to Table 1-1 for data lines parameters. The interface management signal lines control the overall bus operations (Table 1-2 describes these signal lines). The three handshaking lines operate in a three-wire interlocked handshake process to transfer each data byte by means of the DIO data lines (Table 1-3 describes the function of these lines, while Appendix C describes the handshaking process itself).

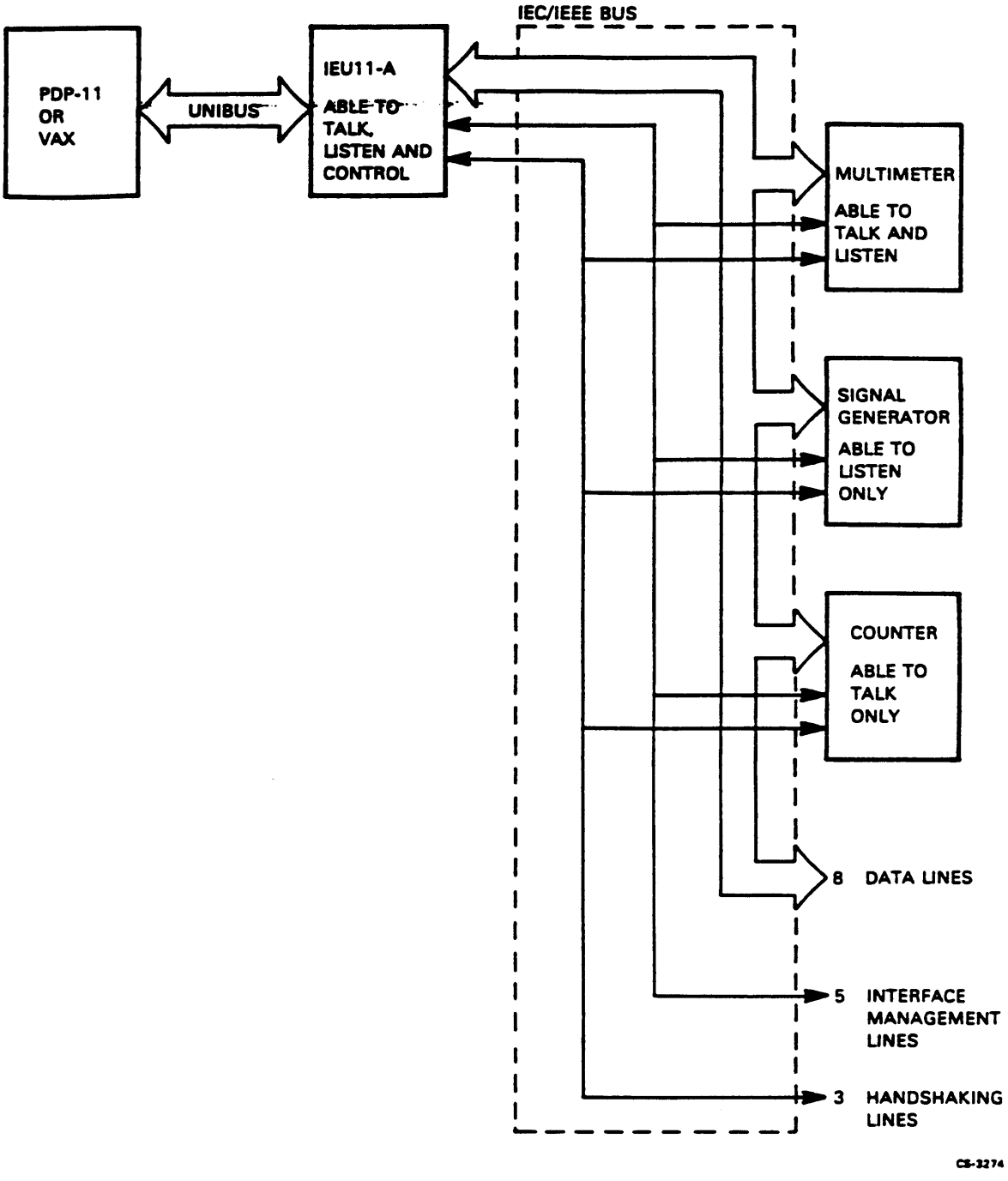


Figure 1-4 Example Devices on an IEC/IEEE Bus

Table 1-1 Data Line

Signal Name	Mnemonic	Function
Data Input/Output	DIO <8:1>	DIO <8:1> lines are the data input/output lines to the IEC/IEEE bus. These data lines are connected to the IEC/IEEE bus by means of non-inverting transceivers.

Table 1-2 Interface Management Signal Lines

Signal Name	Mnemonic	Function
Attention	ATN	Sent by the controller in charge. When true (low), interface commands are being sent over the DIO lines. When false (high), these lines carry data.
Interface Clear	IFC	Sent by the system controller to set the interface system into a known quiescent state. The system controller becomes the controller in charge.
Service Request	SRQ	Set true (low) by a device to indicate a need for service.
Remote Enable	REN	Sent by system controller to select control either from the front panel or from the IEC/IEEE bus.
End Or Identify	EOI	If ATN is false (high), this indicates the end of a message block. If ATN is true (low), the controller is requesting a parallel poll.

Table 1-3 Handshaking Lines

Signal Name	Mnemonic	Function
Data Valid	DAV	Controlled by source to show acceptors when valid data is presented to the bus.
Not Ready For Data	NRFD	Sent by acceptor to indicate readiness for next byte.
Not Data Accepted	NDAC	Acceptor sets this false (high) when it has latched the data from the I/O lines.

1.4.1 IEC/IEEE Interface Messages

This section describes the messages that may be sent by means of the IEC/IEEE Bus by a controller-in-charge. A controller-in-charge is an IEU11-A/IEQ11-A option that is active (CACS). The messages can be divided into five groups.

1. Address Command Group (ACG)
2. Universal Command Group (UCG)
3. Listener Address Group (LAG)
4. Talker Address Group (TAG)
5. Secondary Command Group (SCG)

1.4.1.1 Address Command Group (ACG) -- These commands are effective only in devices which have been addressed as a Listener or a Talker. Table 1-4 list the ACG commands.

Table 1-4 Address Command Group (ACG)

Mnemonic	Octal	ASCII	Function	Command	Description
GTL	001	SOH	Listener	Go To Local	Causes addressed listeners to go from Remote mode to Local mode. When local is true, a device is controlled by its front or back panel controls.
SDC	004	EOT	Listeners	Selected Device Clear	Causes the addressed listeners to be reset (initialization).
PPC	005	ENQ	Listener	Parallel Poll Configuration	Causes the addressed listeners to enter the Parallel Poll Configuration mode so that the addressed listeners are able to participate in a parallel poll. The next command must be PPE from the Secondary Command Group to allow the listener to respond to ATN or EOI becoming true.
GET	010	BS	Listener	Group Execute Trigger	Causes the addressed listeners to start basic operation of the device of which the listener is a part.
TCT	011	HT	Talker	Take Control	Causes a device which has been addressed as the talker to enable its controller to become the controller-in-charge after the current controller-in-charge unasserts ATN.

1.4.1.2 Universal Command Group (UCG) -- These commands affect all devices which are able to respond without having to be previously addressed. The UCG commands are listed in Table 1-5.

Table 1-5 Universal Command Group (UCG)

Mnemonic	Octal	ASCII	Command	Description
LLO	021	DC1	Local Lockout	Causes all devices to ignore their local message RTL (Return To Local).
DCL	024	DC4	Device Clear	Causes all devices to be reset (initialization).
PPU	025	NAK	Parallel Poll Unconfigure	Causes all parallel poll configurations to become unconfigured.
SPE	030	CAN	Serial Poll Enable	Causes all talkers to enter the serial poll mode to allow a talker to send a status byte after being addressed by the controller-in-charge.
SPD	031	EM	Serial Poll Disable	Causes all talkers to exit the serial poll mode and return to the normal data mode.

1.4.1.3 Listener Address Group (LAG) -- These commands may be used to address one or more listeners or to address all listeners at once. Addressed listeners become active when the controller-in-charge unasserts ATN. The LAG commands may be followed by a secondary address (MSA) to address an extended listener. Table 1-6 lists the LAG addresses.

Table 1-6 Listener Address Group (LAG)

Mnemonic	Octal	ASCII	Address	Description
MLA 00	040	SP	My Listen Address 0	Any listener that recognizes its own address becomes an addressed listener, and is able to receive data bytes from a talker as soon as the controller-in-charge unasserts ATN.
MLA 01	041	!	My Listen Address 1	" "
MLA 30	076	>	My Listen Address 30	" "
UNL	077	?	Unlisten	Causes all listeners to become unaddressed.

1.4.1.4 Talker Address Group (TAG) -- These commands are used to address or unaddress one talker. An addressed talker becomes active when the controller-in-charge unasserts ATN. The commands in the TAG may be followed by a secondary address (MSA) to address an extended talker.

Table 1-7 Talker Address Group

Mnemonic	Octal	ASCII	Address	Description
MTA 00	100	@	My Talk Address 0	A talker that recognizes its own address becomes an addressed talker, whereas all other talkers becomes unaddressed. Only one talker is able to send data via the IEC/IEEE Bus.
MTA 01	101	A	My Talk Address 1	" "
MTA 30	136	^	My Talk Address 30	" "
UNT	137	-	Untalk	Causes the addressed talker to become unaddressed.

1.4.2 Secondary Command Group (SCG)
The meaning of these commands is defined by the preceeding primary command of the Primary Command Group (PCG= ACG UCG LAG TAG). Table 1-8 list the SCG commands.

Table 1-8 Secondary Command Group

Mnemonic	Octal	ASCII	Command	Description
PPE #1	140		Parallel Poll Enable #1	Each PPE command must follow a PPC (Parallel Poll Configure) command which forces currently addressed listeners into their Parallel Poll Configuration state. The PPE command indicates to a device how to respond to a parallel poll request from the controller-in-charge. A device responds by sending one status bit on one of the eight DIO lines. The second digit of the PPE command mnemonic specifies that line, whereas the first digit specifies which state of the devices status bit should activate the DIO line. For example, PPE 12 instructs the device to activate the DIO line 2 when the device status bit is "1", and PPE #2 instructs the device to activate that line if the status bit is "0". A Parallel Poll Request is issued by the controller-in-charge by activating the EDI line together with the ATN line.
PPE #2	141	a	Parallel Poll Enable 2	" "
PPE #7	146	f	Parallel Poll Enable #7	" "
PPE #8	147	g	Parallel Poll Enable #8	" "
PPE 11	150	h	Parallel Poll Enable 11	" "
PPE 12	151	i	Parallel Poll Enable 12	" "
PPE 17	156	n	Parallel Poll Enable 17	" "
PPE 18	157	o	Parallel Poll Enable 18	" "
PPD	160	p	Parallel Poll Disable	This command must follow its associated PPC command and inhibits devices from responding to the Parallel Poll Request.
MSA #0	140		My Secondary Address 0	An MSA Command must follow a Talker or Listener Address. Devices that use extended addressing will not become addressed as long as the associated Secondary Address follows the Primary Address.
MSA #1	141	a	My Secondary Address 1	" "
MSA 29	175	}	My Secondary Address 29	" "
MSA 30	176	~	My Secondary Address 30	" "

1.4.3 Types of Functional Devices

There are four functional types of devices that can be used on the IEC/IEEE bus. These functional types are the following:

- Talk only devices
- Listen only devices
- Talk and listen devices
- Talk, listen, and control devices

Table 1-9 describes these functional types of devices.

Table 1-9 Functional Types of Devices

Device Type	Function	Example Device
Talk Only	When signaled, this device applies its output to the DIO lines in a fixed configuration. The configuration may be altered by a front panel control.	Counter
Listen Only	Responds to data from the DIO lines.	Printer, signal generator
Listens and Talks	This device is configured by signals from the controller, receives the requested reading, and returns the results to the IEC/IEEE bus.	Digital multimeter
Talks, Listens, and Controls	Not only can talk and listen, but also controls all operations on the IEC/IEEE bus.	IEU11-A or IEQ11-A

1.4.4 IEC/IEEE Bus System

Each IEC/IEEE Bus system must have three basic functional elements to be able to organize and manage the information exchanged between devices. The three functional devices are the following:

- Controller device
- Listener device
- Talker device

When acting as a controller, the IEU11-A/IEQ11-A option can be the controller-in-charge, as well as the system controller. An IEC/IEEE Bus System can have multiple devices which contain the controller interface function. However, only one device at a time can be the controller, and this device is known as the controller-in-charge. The system controller is the controller that is able to send IFC and REN messages (see Table 1-2 for the definition of IFC and REN). Only one device can be assigned as system controller.

An IEU11-A/IEQ11-A option becomes a listener when the controller-in-charge sends its listen address over the IEC/IEEE bus, or by loading its own Auxiliary Command Register with the Listen Only command (LON). When active, the listener receives data bytes from the IEC/IEEE bus to the IEU11-A/IEQ11-A option. Multiple listeners may be configured simultaneously.

An IEU11-A/IEQ11-A option becomes a talker when the controller-in-charge applies its talk address by means of the IEC/IEEE bus, or by loading its own Auxiliary Command Register with the Talk Only command (TON). When active, the talker sends data bytes from the IEU11-A/IEQ11-A option to the IEC/IEEE bus. Only one device at a time acts as a talker.

1.4.5 IEEE 488-1978 Interface Functions

The IEU11-A/IEQ11-A option provides the IEEE 488-1978 interface functions listed in Table 1-10.

Table 1-10 IEEE 488-1978 Interface Functions

Function Name	Mnemonic
Automatic Source Handshake	SH1
Automatic Acceptor Handshake	AH1
Talker and Extended Talker (includes serial poll capability)	T5, TE5
Listener and Extended Listener	L3, LE3
Service Request	SR1
Remote Local	RL1
Parallel Poll	PP1, PP2
Device Clear	DC1
Device Trigger	DT1
Controller	C1, 2, 3, 4, 5

1.5 GENERAL SPECIFICATIONS

This section contains information on environmental specifications, electrical specifications, performance parameters, and IEC/IEEE bus parameters. Refer to Table 1-11 through Table 1-14 for the information.

Table 1-11 Environment Specifications

Environmental Parameter	Specification
Operating Temperature	5° to 50° C
Relative Humidity	10% to 90% noncondensing

Table 1-12 Electrical Specifications

Electrical Parameter	Specification
Required Voltage(s)	+5 V dc (±5%)
Current Requirement(s)	3.5A @ +5 volts (IEU11-A Option) 3.0A @ +5 volts (IEQ11-A Option)
UNIBUS/LSI Bus Load	1
Logic Levels	TTL
IEC/IEEE Bus Load	1 on each bus

Table 1-13 Performance Parameters

Parameter	Specifications
Operating Mode(s)	1. Programmed I/O transfers with interrupt. 2. DMA data transfer, byte addressing, and interrupt.
Transfer Rate	Up to 150K bytes per second (DMA transfer). Transfer rates dependent on the hardware configuration and operating system being used.
Maximum Block Length	64K bytes
Addressable Memory Range	256 KB (4MB on Q-22)
Interrupt	Vector A (channel 1) is selectable, while Vector B (channel 2) depends on Vector A. Vector A is set at A+4.
Priority Level	BR6 (selectable). BR4 is used on Q-bus CPUs.

Table 1-14 IEC/IEEE Bus Parameters

Parameter	Specification
Communication Channel	Two independent IEC/IEEE buses
Number of Devices	Up to 15 devices on each bus (includes IEU11-A/IEQ11-A)
Maximum Cable Length	Two meters (6.56 ft) times the number of devices, or 20 meters (65.6 ft), whichever is less

NOTE

Individual cable length should not exceed four meters between devices.

CHAPTER 2
INSTALLATION

2.1 INTRODUCTION

The IEU11-A option can be installed in either a PDP-11 or a VAX-11 system, while the IEQ11-A option can be installed in either a LSI-11 or a MICRO system. The installation procedure for LSI-11 and MICRO systems is different from the PDP-11 and VAX-11 systems, since a different module is used.

An installation consists of the following six major steps.

1. Unpacking and inspection
2. Module configuration
3. Module installation
4. Verifying module operation
5. Field service and customer acceptance
6. IEC/IEEE bus interconnection

To do an IEU11-A/IEQ11-A option installation, perform the following:

- PDP-11 or VAX-11 system installation - Sections 2.2 through 2.8.
- LSI-11 or MICRO systems installation - Sections 2.9 through 2.15.

2.2 IEU11-A OPTION UNPACKING AND INSPECTION

The IEU11-A option is packed according to commercial packing practices. Remove all packing materials and check the equipment against the shipping list. Table 2-1 lists the items contained in the IEU11-AA option (IEC bus), while Table 2-2 lists the items contained in the IEU11-AB option (IEEE bus).

Table 2-1 IEU11-AA Option Shipping List (IEC Bus)

Qty.	Part Number	Description
1	M8648	Dual IEC/IEEE bus controller (UNIBUS)
I	BC08S-01	Test cable
1	BN11C-02	IEC 625-1 bus system cable with PDP-11 bulkhead panel assembly
1	BN01C-02	Instrument bus cable, dual IEEE-488 connectors on both ends (optional)

Table 2-2 IEU11-AB Option Shipping List (IEEE Bus)

Qty.	Part Number	Description
1	M8648	Dual IEC/IEEE bus controller (UNIBUS)
1	BC08S-01	Test cable
1	BN11D-02	IEEE 488 bus cable with PDP-11 bulkhead panel assembly
1	BN01A-02	Instrument bus cable, dual IEEE-488 connectors on both ends (optional)

Inspect all items and carefully check the module for cracks, loose components, and breaks in the etched paths. Report damages or missing items to the shipper immediately, and inform the DIGITAL representative.

2.3 IEU11-A SITE REQUIREMENTS

Table 2-3 lists the site requirements for the IEU11-A option.

Table 2-3 IEU11-A Site Requirements

Parameter	Requirements
Module Environment	DD11 backplane; one hex SPC-slot with NPR jumper removed
Voltage Requirements	5V dc @ 3.5 A
Bulkhead Panel Size	One 2-insert unit
Location of Bulkhead Panel	Anywhere in bulkhead frame

Table 2-3 IEU11-A Site Requirements (Cont)

Parameter	Requirements
Device Address	The factory installed address is 764100. The IEU11-A requires an assignment of eight consecutive device addresses in the UNIBUS I/O page. The factory installed address is assigned to the first register (ISR 1 and 2).
Interrupt Vector Address	The factory installed Interrupt Vector address is 270. The Interrupt Vector Address requires a block of two interrupt vectors (four words) at the beginning of an address where bits <2:0> must equal 0.
Interrupt Priority Level	BR6 (bus grant jumper plug).

2.4 M8648 MODULE CONFIGURATION

Two dip switchpacks and a replaceable bus grant jumper plug determine the M8648 module configurations. One dip switchpack (E98) is used for the device address, while the other dip switchpack (E56) is used for the interrupt vector address. A bus grant jumper plug is used to determine the BR level, normally BR6.

2.4.1 M8648 Module Configuration Procedure

Step	Procedure
1	Verify that the correct device address (764100) is set in dip switchpack E98 (refer to Figure 2-1). If a second IEU11-A option is used in the same system, another device address must be assigned to the second IEU11-A option. The device address must always be in increments of 20 (octal) starting from 0. Refer to Figure 2-1 for the dip switchpack address scheme.
2	Verify that the correct interrupt vector address (270) is set in the dip switchpack E56 (refer to Figure 2-1). If a second IEU11-A option is used in the same system, another interrupt vector address must be assigned to the second IEU11-A option. Refer to Figure 2-1 for the dip switchpack address scheme.
3	Verify that the correct bus grant jumper plug (E67) is installed and seated properly (refer to Figure 2-1). If the plug (E67) does not meet the required BR level, remove the plug and install one of desired level.

NOTE

Ensure that any changes from the standard configuration are noted and are considered during the software driver installation, because the default parameters expect a standard hardware configuration.

2.5 M8648 MODULE INSTALLATION

The IEU11-A option can be installed in any DD11 system unit or CPU backplane that accepts hex-height modules. The IEU11-A uses a SPC slot.

2.5.1 M8648 Module Installation Procedure

Step	Procedure
1	Turn off system power.
2	Locate the SPC slot in the DD11 backplane that the M8648 module is to be installed in. DO NOT insert the M8648 module into the backplane at this time.
3	Remove the NPG jumper between pins CA1 and CB1 from the designated M8648 slot on backplane.
4	Remove the Grant Continuity Card from the designated M8648 slot.
5	Connect the M8648 J1 connector to the M8648 J2 connector with a BC08S-01 cable (refer to Figure 2-2). Ensure that Pin A of connector J1 is connected to Pin A of connector J2. The BC08S-01 cable needs to be installed to run the diagnostics and DEC-X/11 System Exerciser.
6	Insert the M8648 module into the designated SPC slot.
7	Turn on the system power.
8	Measure the +5 Vdc (Pin A2, any slot) on the DD11 system backplane. The voltage should be between 4.75 V and 5.25 V.

2.6 VERIFYING M8648 MODULE OPERATION

Choosing which diagnostic to use to verify the operation of the M8648 module depends on whether the M8648 is installed in a PDP-11 system or a VAX-11 system. Therefore, if the M8648 module is installed in a PDP-11 system, proceed to Section 2.6.1. If it is installed in a VAX-11 system, proceed to Section 2.6.2.

NOTE

The diagnostics required to verify the operation of the M8648 module are not shipped with the IEU11-A option. The diagnostics are distributed to DIGITAL Field Service through the Software Distribution Center (SDC).

2.6.1 M8648 Module Operation Verified in a PDP-11 System

The operation of the M8648 module (PDP-11) is verified by running the CZIEA?? IEU/IEQ Static Diagnostic. The loading and operating procedures for the diagnostic are contained in the program listing. The BC08S-01 cable must be installed (Figure 2-2). Perform the following:

- Run the default series of tests for the unit.
- Run three error free passes of Tests 1 through 26 with the 'Quick Verify' flag selected.
- Run one error free pass without the 'Quick Verify' flag selected.

2.6.2 M8648 Module Operation Verified in a VAX-11 System

The operation of the M8648 module (VAX-11) is verified by running the IEU11-A M8648 Offline Test Diagnostic (EVCDC). The EVCDC diagnostic is a repair level (Level 3) diagnostic that exercises an M8648 module. This diagnostic requires a VAX-11 Diagnostic Supervisor of V6.11 or later. Instructions for running the Diagnostic Supervisor can be referenced in the Diagnostic System User's Guide for the respective type of VAX-11 processor. The BC08C-01 test cable must be installed to run the EVCDC diagnostic.

2.7 FIELD SERVICE AND CUSTOMER ACCEPTANCE

The procedure used for field service and customer acceptance depends on whether the M8648 module is installed in a PDP-11 system or a VAX-11 system. Therefore, proceed to Section 2.7.1 if the M8648 module is installed in a PDP-11 system, and if it is installed in a VAX-11 system, proceed to Section 2.7.2.

NOTE

The diagnostics required for field service and customer acceptance are not shipped with the IEU11-A option. The diagnostics are distributed to DIGITAL Field Service through the Software Distribution Center (SDC).

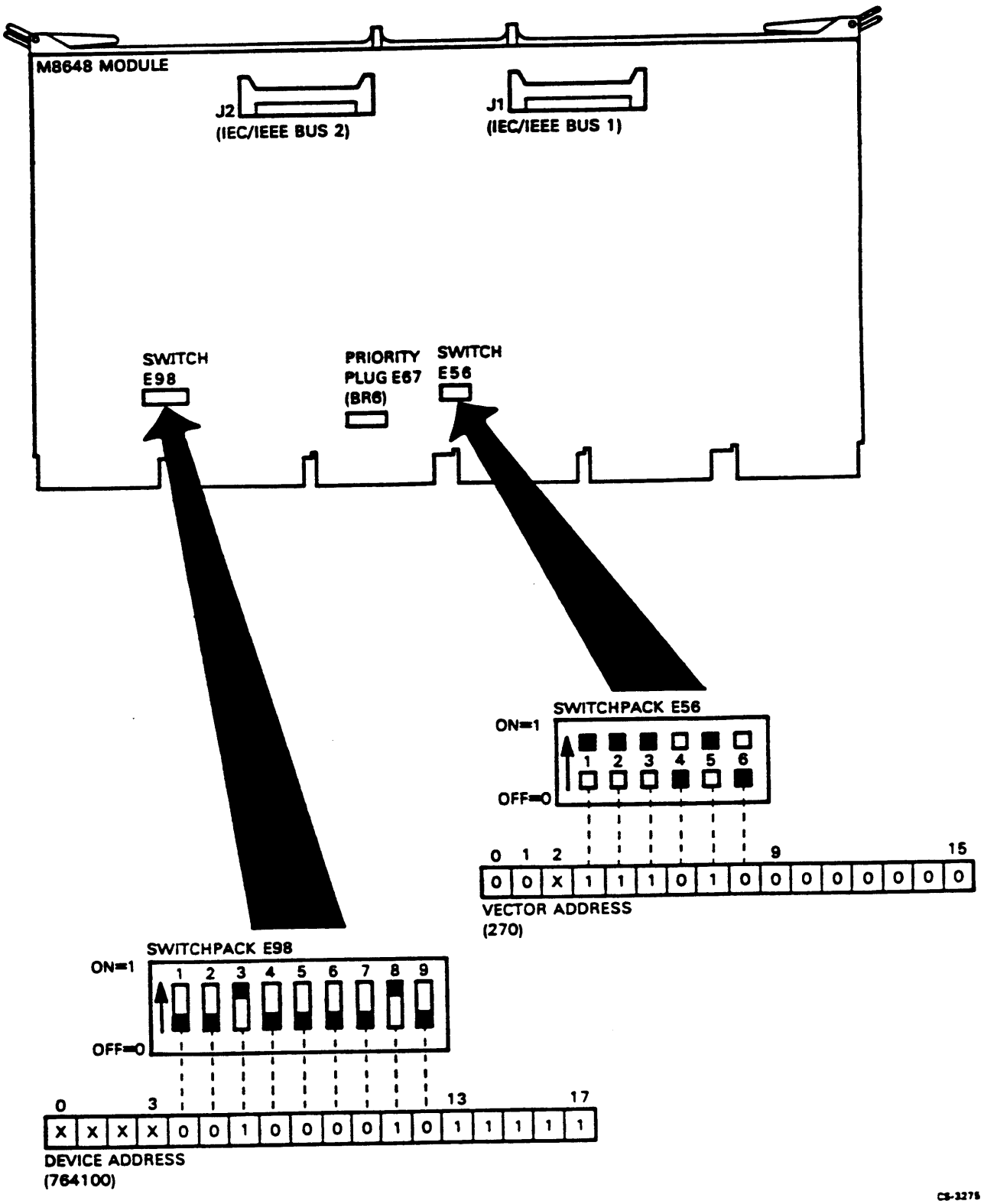


Figure 2-1 M8648 Module Configuration (UNIBUS)

2.7.1 Field Service and Customer Acceptance Procedure (PDP-11 System)

The following needs to be performed in order to demonstrate to the field engineer and to the customer that the IEU11-A option performs correctly. The BC08S-01 cable must be installed (Figure 2-2).

- Run the CZIEA?? IEU/IEQ static diagnostic as outlined in Section 2.6.1 (four error-free passes).
- Configure a DEC-X/11 System Exerciser to include all the devices in the PDP-11 system.
- Run the exerciser until a complete "relocation cycle" has been performed through the memory.

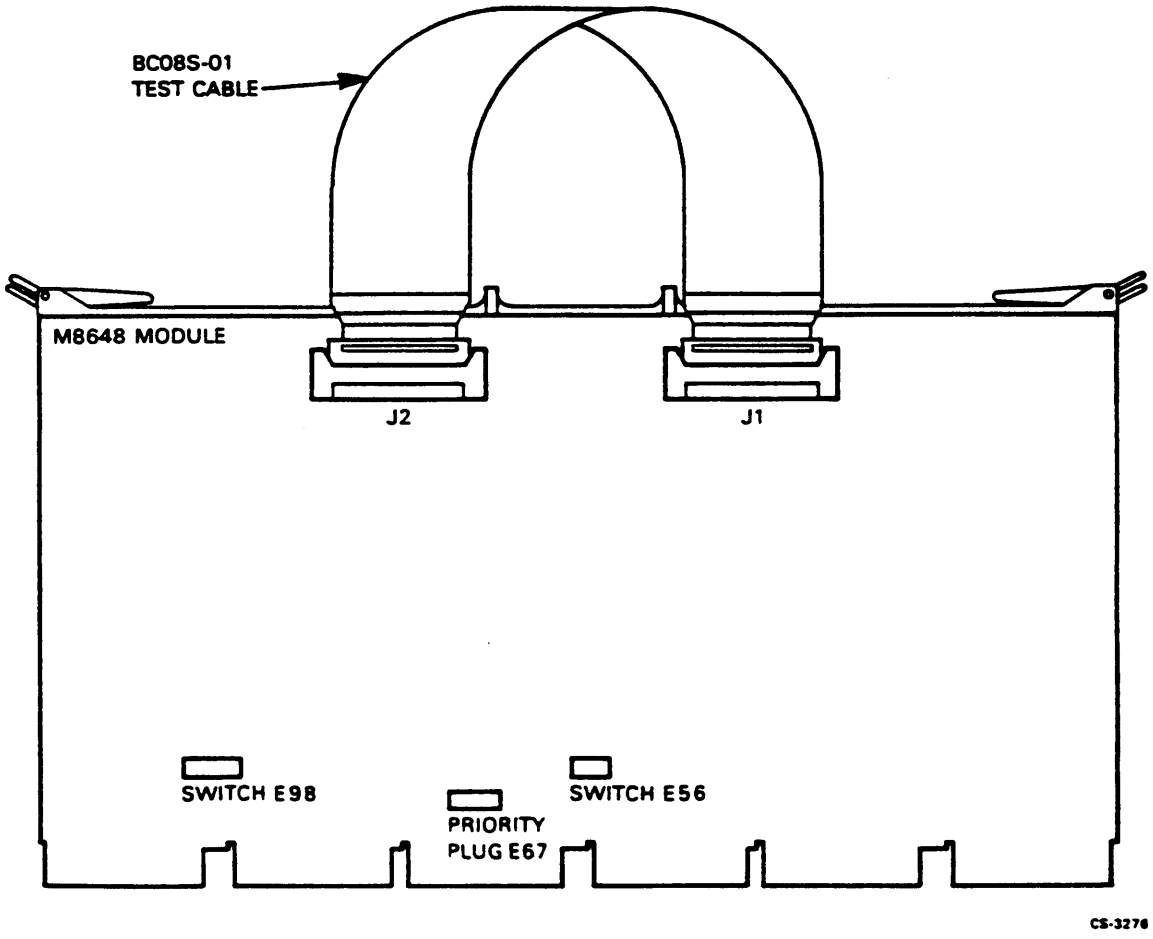


Figure 2-2 BC08S-01 Test Cable Installed (M8648 Module)

2.7.2 Field Service and Customer Acceptance Procedure (VAX-11 System)

After the EVCDC diagnostic (Section 2.6.2) is run, the EVCDB diagnostic needs to be run to demonstrate to both the field service engineer and the customer that the IEU11-A performs properly. The EVCDB diagnostic is a functional level (Level 2R) diagnostic that exercises an IEU11-A option. The program runs with the Diagnostic Supervisor under VMS Version 3.Ø or later. The BCØ8S-Ø1 test cable must be installed to run this diagnostic.

The VMS software driver (IXDRIVER) must be loaded and connected, using the SYSGEN utility. The VMS software driver (IXDRIVER) must be installed before the EVCDB diagnostic can be executed. Refer to the HELP file under the Diagnostic Supervisor (DS>HELP EVCDB).

2.8 IEC/IEEE BUS INTERCONNECTION

The IEU11-A can be a controller for either one or two IEC/IEEE bus systems. Therefore, there are four possible configurations:

1. IEU11-A acts as a controller for one IEC bus system.
2. IEU11-A acts as a controller for two IEC bus systems.
3. IEU11-A acts as a controller for one IEEE bus system.
4. IEU11-A acts as a controller for two IEEE bus systems.

2.8.1 IEEE/IEC Bus Interconnect Procedure

Step	Procedure
1	Remove the BC08S-01 test cable from the M8648 module.
2	Identify the 2-meter shielded cable with a Berg connector on one end and an Amphenol™ or a Cannon™ connector on the other end. The Amphenol or Cannon connector is connected to the I/O bulkhead panel. An IEC cable has part number BN11C-02, while an IEEE cable has part number BN11D-02.
3	Connect the Berg connector of the identified cable to the J1 connector on the M8648 module. Refer to Figure 2-3 for an IEC cable connection, or Figure 2-4 for an IEEE cable connection.
4	Determine if one of the following optional components are present: a 2-meter IEC-625 Bus cable (17-00384-02), or an IEEE-488 Bus cable with an I/O bulkhead panel (BN11D-02). If this second cable is present, connect the Berg connector to J2 on the M8648 module. On an IECBus installation, connect the Amphenol or Cannon connector of the cable (17-00384-02) to the I/O bulkhead panel. Refer to Figure 2-3 for an IEC bus cable connection, or Figure 2-4 for an IEEE bus connection.
5	Attach the I/O bulkhead panel(s) to an available bulkhead frame(s) with the four screws. If no bulkhead frame is available, the I/O panels can be attached to the cabinet frame wherever it is most convenient.

Berg™ is a trademark of Berg Electronics.

Amphenol™ is a trademark of Amphenol North America: Division of Bunker-Ramo.

Cannon™ is a trademark of ITT Cannon Electric.

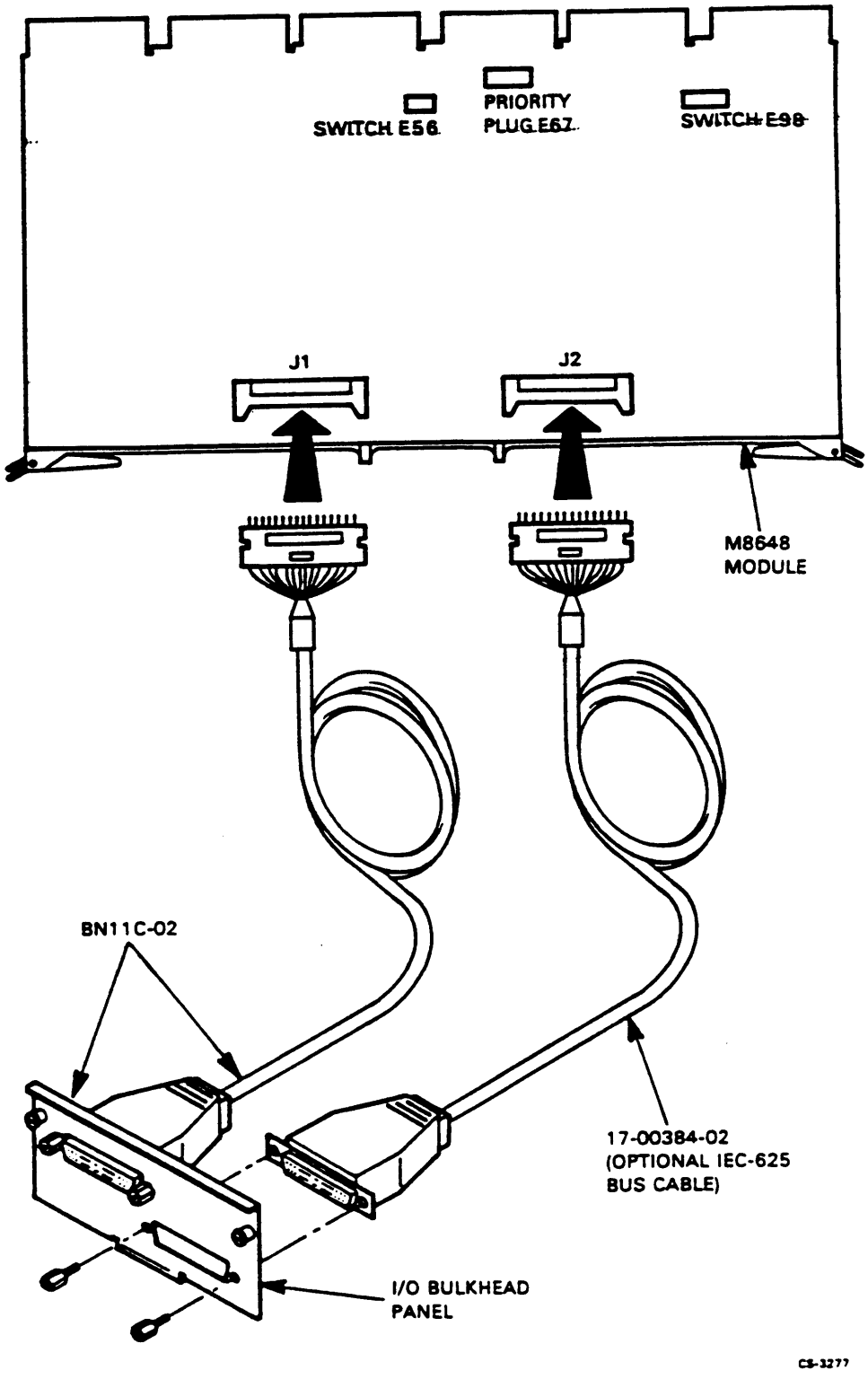


Figure 2-3 IEC Cable Connections (UNIBUS)

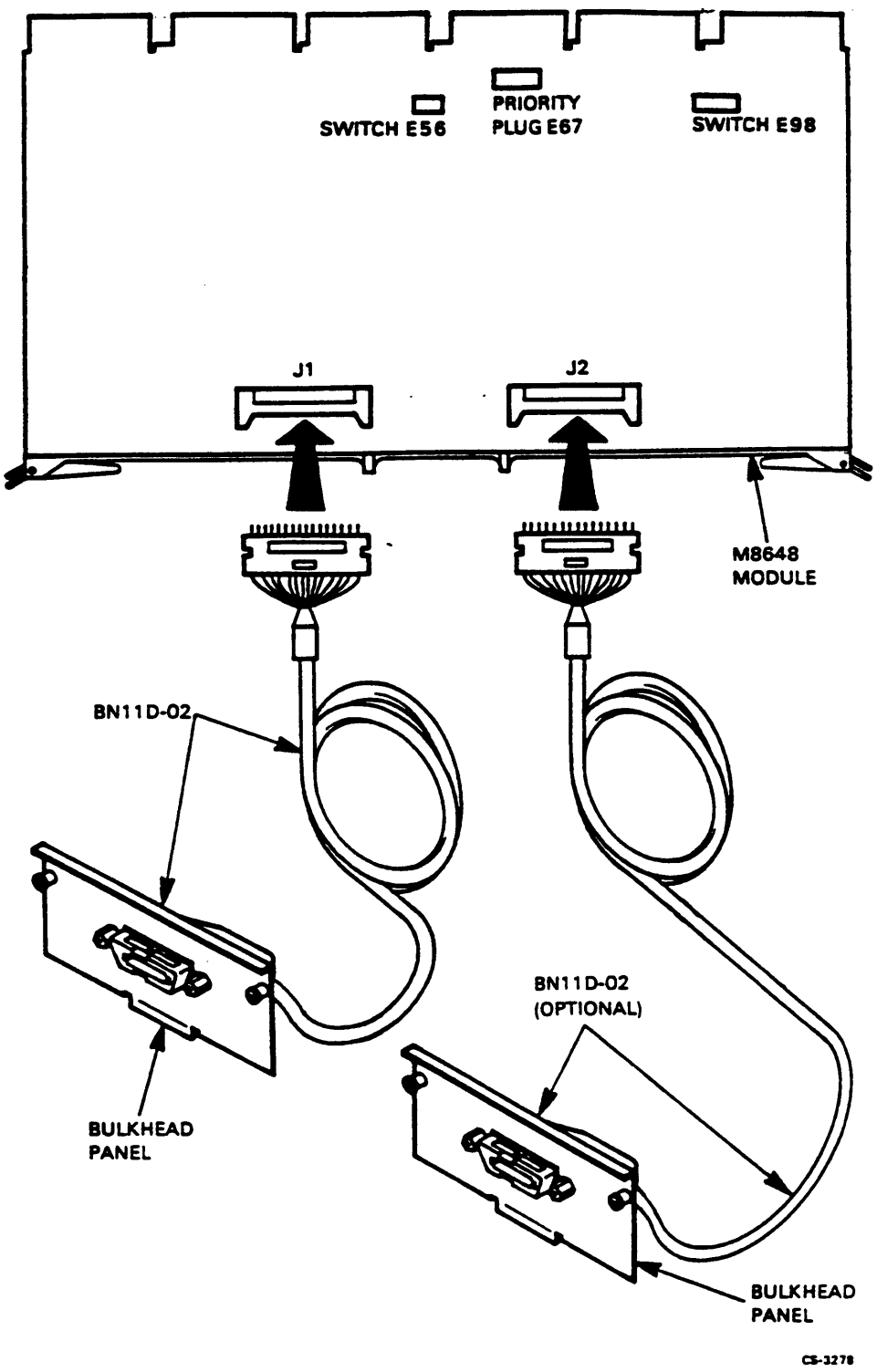


Figure 2-4 IEEE Cable Connections (UNIBUS)

2.8.2 Testing the IEC/IEEE Bus Cables

To test the IEC/IEEE bus cables that interconnect the M8648 module to the I/O bulkhead panel(s), the following procedure is performed.

Step	Procedure
1	Both channels on the IEU11-A option must be used; that is, the following must be installed: • IEC installation -- an IEC bus cable with I/O bulkhead panel (BN11C-Ø2) and an optional IEC bus cable (17-ØØ384-Ø2). Refer to Figure 2-3. • IEEE installation -- two IEEE bus cables with two I/O bulkhead panels (BN11D-Ø2). Refer to Figure 2-4.
2	Interconnect both channels by performing the following: • IEC installation -- connect the two channels by installing an instrument bus cable, dual IEC-625 connector on both ends (BNØ1C-Ø2) to the I/O bulkhead panel (refer to Figure 2-5).

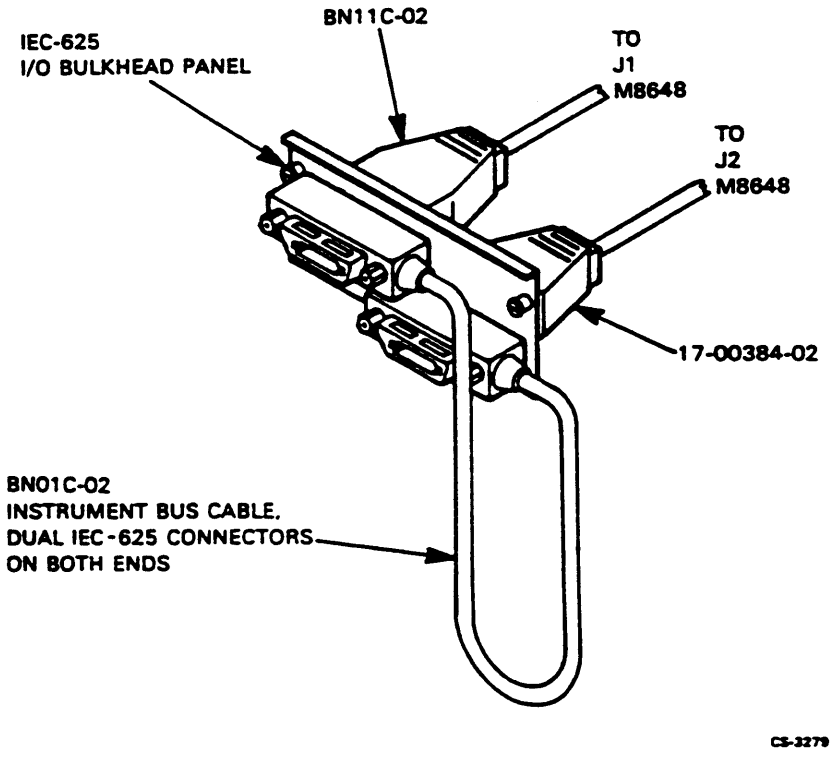


Figure 2-5 IEC Cable Test Configuration (UNIBUS)

Step	Procedure
	• IEEE installation -- connect the two channels by installing an instrument bus cable, dual IEEE-488 connector on both ends (BNØ1A-Ø2) to the two I/O bulkhead panels (refer to Figure 2-6).
3	Perform the module verification procedure in Section 2.6, ignoring the references in Section 2.6 to the BCØ8S-Ø1 test cable.

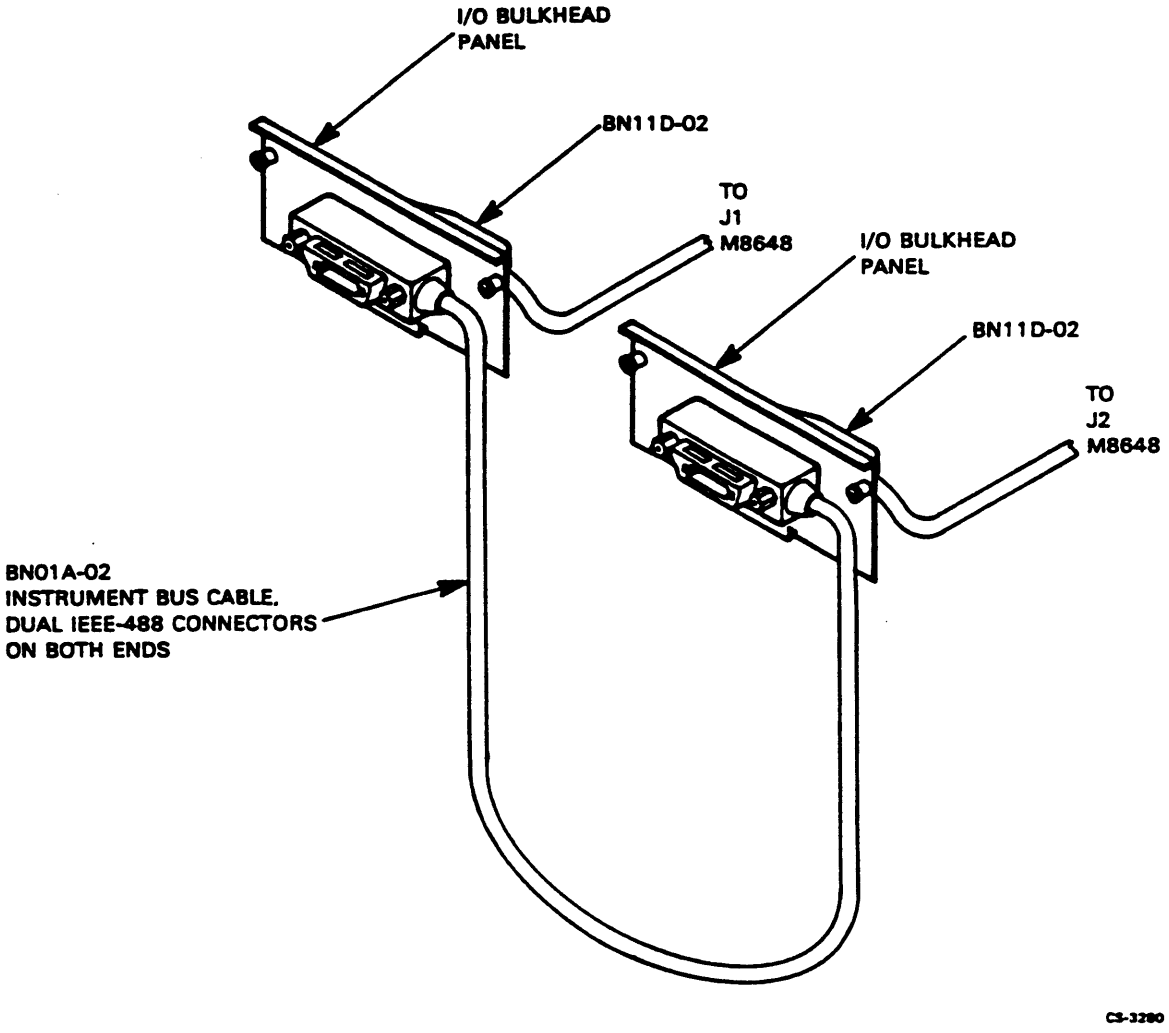


Figure 2-6 IEEE Cable Test Configuration (UNIBUS)

2.9 IEQ11-A OPTION UNPACKING AND INSTALLATION

The IEQ11-A option is packed according to commercial packing practices. Remove all packing materials and check the equipment against the shipping list. Table 2-4 lists the items contained in the IEQ11-AA option (IEC bus) while Table 2-5 lists IEQ11-AB option (IEEE bus).

Table 2-4 IEQ11-AA/AC Option Shipping List (IEC Bus)

Qty.	Part Number	Description
1	M8634	Dual IEC/IEEE bus controller (Q-Bus)
1	BC08S-01	Test cable
1	BN11E-01	IEC 625-1 bus cable with LSI bulkhead panel assembly. Used on IEQ11-AA.
	or	
1	BN11J-0C	IEC 625-1 bus interconnect cable with MICRO systems bulkhead panel assembly. Used on IEQ11-AC.
1	BN01C-02	Instrument Bus cable, dual IEC-625 connectors on both ends (optional)

Table 2-5 IEQ11-AB/AD Option Shipping List (IEEE Bus)

Qty.	Part Number	Description
1	M8634	Dual IEC/IEEE bus controller (Q-Bus)
1	BC08S-01	Test cable
1	BN11F-01	IEEE 488 bus cable with LSI bulkhead panel assembly. Used on IEQ11-AB.
	or	
1	BN11K-0C	IEEE 488 bus cable with MICRO systems bulkhead panel assembly. Used on IEQ11-AD.
1	BN01A-02	Instrument Bus cable, dual IEEE-488 connectors on both ends (optional)

Inspect all items and carefully check the module for cracks, loose components, and breaks in the etched paths. Report damages or missing items to the shipper immediately, and inform the DIGITAL representative.

2.10 IEQ11 SITE REQUIREMENTS

Table 2-6 lists the site requirements for the IEQ11-A option.

Table 2-6 IEQ11-A Option Site Requirements

Parameter	Requirement
Module Environment	LSI bus backplane 1 quad slot
Voltage Requirement	5 Vdc @ 3.0 A
Required I/O Panel	C size I/O bulkhead panel, B-size I/O bulkhead panel for MICRO system enclosures.
Location I/O Bulkhead Panel	Available bulkhead frame
Device Address	The factory installed address is 764100 (first register ISR 1 and 2). An assignment of eight consecutive device addresses in I/O page is required.
Interrupt Vector Address	The first interrupt vector has the assigned address 270. Requires a block of two interrupt vectors (four words) at the beginning address where bits <2:0> must equal zero.
Priority Interrupt Level	BR4

2.11 M8634 MODULE CONFIGURATION

Two dip switchpacks and eight jumpers determine the M8634 module configuration. One dip switchpack (E41) is used for the device address, while the other dip switchpack (E46) is used for the interrupt vector address. Jumpers W1 through W3 are configured according to the type of LSI-11 backplane that the M8634 is installed in. Jumpers W4 through W6 are used in conjunction with the multilevel interrupt integrated circuit which is not presently available. Jumpers W7 and W8 provide continuity for the interrupt acknowledge (BIAK) and direct memory access grant (BDMG) bus signals.

2.11.1 M8634 Module Configuration Procedure

Step	Procedure
1	Verify that the correct device address (764100) is set in dip switchpack E41 (refer to Figure 2-7). If a second IEQ11 option is used in the same system, another device address must be assigned to the second IEQ11 option. Refer to Figure 2-7 for the dip switchpack address scheme.
2	Verify that the correct interrupt vector address (270) is set in dip switchpack E46 (refer to Figure 2-7). If a second IEQ11 option is used in the same system, another interrupt vector address must be assigned to the second IEQ11 option. Refer to Figure 2-7 for the dip switchpack address scheme.
3	Verify that jumpers W6 through W4 are configured for the correct BR level. Refer to both Table 2-7 for the W6 through W4 jumper scheme and Figure 2-7 for the jumper locations on the M8634 module. The jumper scheme is used only when the multi-level interrupt integrated circuit is used; otherwise, jumpers W4 through W6 must not be installed.

Table 2-7 BR Level Jumpers

BR Level	Jumper W4	Jumper W5	Jumper W6
BR 4	Out	Out	Out
BR 5	In	Out	Out
BR 6	Out	Out	In
BR 7	Out	In	In

NOTE

The IEQ11-A option only supports BR level 4. Therefore, the multi-level interrupt function is not possible, and the jumpers W4 through W6 must be out.

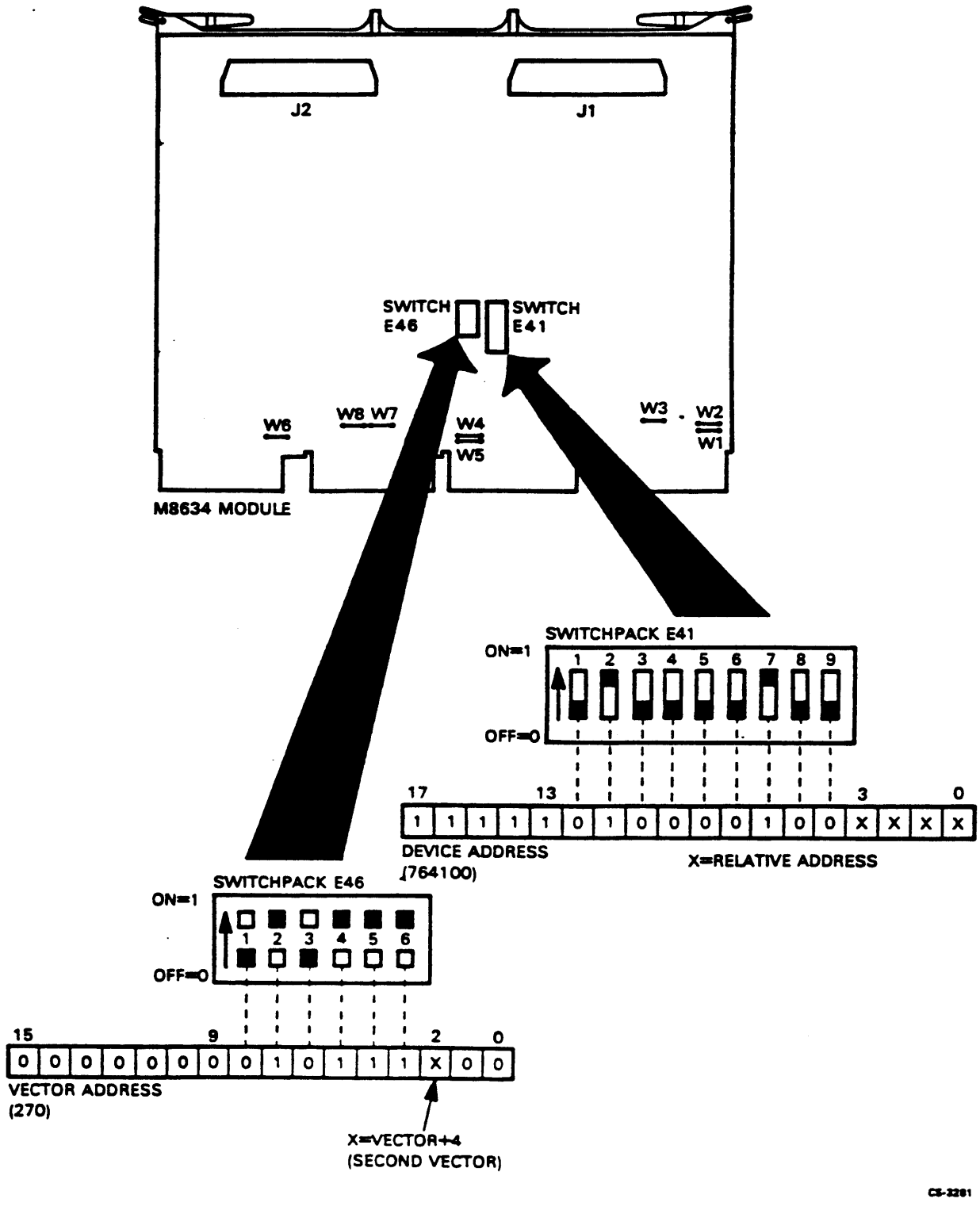


Figure 2-7 M8634 Module Configuration (Q-Bus)

2.12 M8634 MODULE INSTALLATION

The M8634 module can be installed in any LSI-11 and MICRO systems bus backplane that accepts quad-height modules. The M8634 module can support 18-bit addressing in backplanes that feature the traditional LSI-11 bus (Q-bus) or 22-bit addressing in backplanes that feature the extended Q22 Bus. Jumpers W1 through W3 must be configured to accommodate the specific backplane.

2.12.1 M8634 Module Installation Procedure

Step	Procedure
1	Turn system power off.
2	Locate a quad slot in the backplane in which the M8634 module is to be installed. DO NOT insert the M8634 module into the backplane at this time.
3	Determine the kind of backplane being used. Refer to backplane label for the kind of backplane.
4	Verify that jumpers W1 through W3 are installed according to Table 2-8. Refer to Figure 2-7 for the jumper locations.
5	Connect M8634 J1 connector to M8634 J2 connector with a BC08S-01 cable (refer to Figure 2-8). Ensure that Pin A of connector J1 is connected to Pin A of J2 connector. The BC08S-01 cable needs to be installed for both the CZIEA?? IEU/IEQ Static Diagnostic and CXIEA?? DEC-X/11 System Exerciser, and if the M8634 is running in a MICRO/VAX for NAIEA? MDM IEQ11-A Diagnostic.
6	Insert the M8634 module into the designated backplane quad slot.
7	Turn on the system power.
8	Measure the +5 Vdc (Pin A2, any slot) on the backplane. C2 and T1 (any slot) are ground. The voltage should be between 4.75 V and 5.25 Vdc.
9	Verify that the computer system bus is not hung by booting the system and/or running a normal program.

Table 2-8 System-dependent Jumper Scheme

Backplane	LSI-11 Bus Structure Slot A/B	Slot C/d	Module Jumper Setting IN	OUT	Bus Grant Jumper IN	OUT
H9276	Q22-Bus	C/D-Bus	W3,W2	W1		W7,W8 *
H9273	Q-Bus	C/D-Bus	W1	W3,W2		W7,W8 *
H9275	Q22-Bus	Q22-Bus	W3,W2	W1	W7,W8	
H9270	Q-Bus	Q-Bus	W1	W3,W2	W7,W8	
DDV11-B	Q-Bus	Q-Bus	W1	W3,W2	W7,W8	
H9278-A	Q22-Bus	C/D-Bus	W3,W2	W1		W7,W8 *

* See Note of Section 2.14

2.13 VERIFYING M8634 MODULE OPERATION

The operation of the M8634 is verified by running the CZIEA?? IEU/IEQ Static Diagnostic (LSI-11 and MICRO/PDP-11) and by running the NAIEA? MDM IEQ11-A Diagnostic (MICRO/VAX). The loading and operating procedures for the diagnostic are contained in the program listing. The BC08S-01 cable must be installed (Figure 2-8). Perform the following:

- Run the default series of tests for the unit.
- Run three passes of tests 1 through 26 without an error, if the M8634 is installed in a traditional LSI-11 system.
- Run Tests 27 and 28 to test the upper four address lines, if a Q22-bus system is used.
- Run the MDM system (MICRO/VAX Diagnostic Monitor) to verify the M8634, if it is installed in a MICRO/VAX.

NOTE

The diagnostics required to verify the M8634 module operation are not shipped with the IEQ11-A option. The diagnostics are distributed to DIGITAL Field Service through the Software Distribution Center (SDC).

2.14 FIELD SERVICE AND CUSTOMER ACCEPTANCE

The following needs to be performed in order to demonstrate to the field engineer and to the customer that the IEQ11-A option performs correctly. The BC08S-01 cable must be installed (Figure 2-8).

NOTE

The diagnostics required for field service and customer acceptance are not shipped with the IEQ11-A option.

- Run the CZIEA?? IEU/IEQ Static Diagnostic and perform all the steps listed in Section 2.13.
- Configure a DEC-X/11 System Exerciser to include all the devices in the LSI-11 system including CXIEA?? IEU/IEQ DEC-X module.
- Run the exerciser until a complete "relocation cycle" through the memory has been performed.
- Run the MDM system (MICRO/VAX Diagnostic Monitor) to verify the M8634, if it is installed in a MICRO/VAX.

NOTE

If the M8634 module is installed in a Q-BUS backplane (H9273 or H9276 or H9278-A) and the jumpers W7 and W8 are in, pin CM2 is shorted to CN2 and pin CR2 to CS2 on the adjacent higher numbered slot. These connections may be obstructive in some cases, and can be deleted by removing the jumpers.

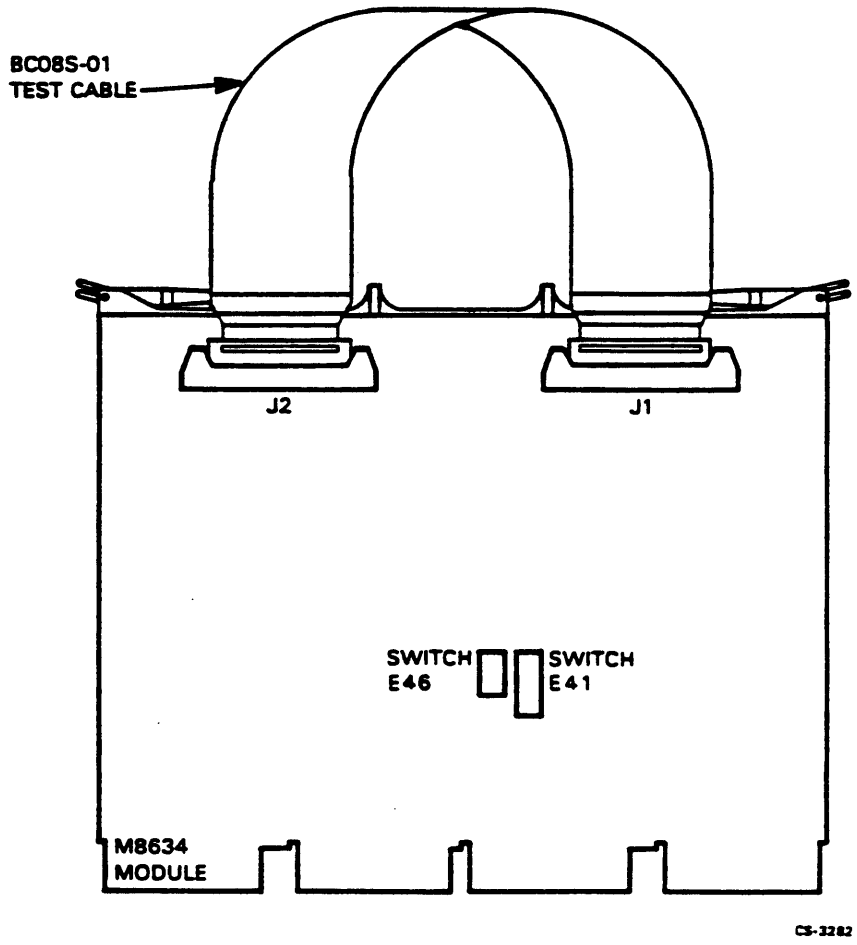


Figure 2-8 BC08S-01 Test Cable Installed (M8634)

2.15 IEEE/IEC BUS INTERCONNECTION

The IEQ11-A can be a controller for either one or two IEC/IEEE bus systems. Therefore, there are four possible configurations:

1. IEQ11 acts as controller for one IEC bus system.
2. IEQ11 acts as controller for two IEC bus systems.
3. IEQ11 acts as controller for one IEEE bus system.
4. IEQ11 acts as controller for two IEEE bus systems.

2.15.1 IEEE/IEC Bus Interconnection Procedure

Step	Procedure
1	Remove the BC08S-01 test cable from the M8634 module.
2	Identify the 1.0 m or .3 m shielded cable with a Berg connector on one end and an Amphenol or Cannon connector on the other end. An IEC cable has part number BN11E-01 and for the MICRO systems BN11J-0C, while an IEEE cable has part number BN11F-01 and for the MICRO systems BN11K-0C.
3	Connect the Berg connector of the identfied cable to the J1 connector on the M8634 module. Refer to Figure 2-9 or Figure 2-13 for an IEC cable connection, or Figure 2-10 and Figure 2-14 for an IEEE cable connection.
4	Determine if one of the following optional components are present: a 1.0 m or .3 m IEC-625 Bus cable (17-00384-01 or BN11M-0C), or an IEEE-488 Bus cable (70-20161-01 or BN11L-0C). If this second cable is present, connect the Berg connector to J2 on the M8634 module. Connect the Amphenol or Cannon connector to I/O bulkhead panel. Refer to Figure 2-9 or Figure 2-13 for an IEC bus cable connection, or Figure 2-10 and Figure 2-14 for an IEEE bus connection.
5	Attach the I/O bulkhead panel to an available bulkhead panel frame with the four screws. If no bulkhead frame is available, the I/O panel can be attached to the cabinet frame wherever it is most convenient.

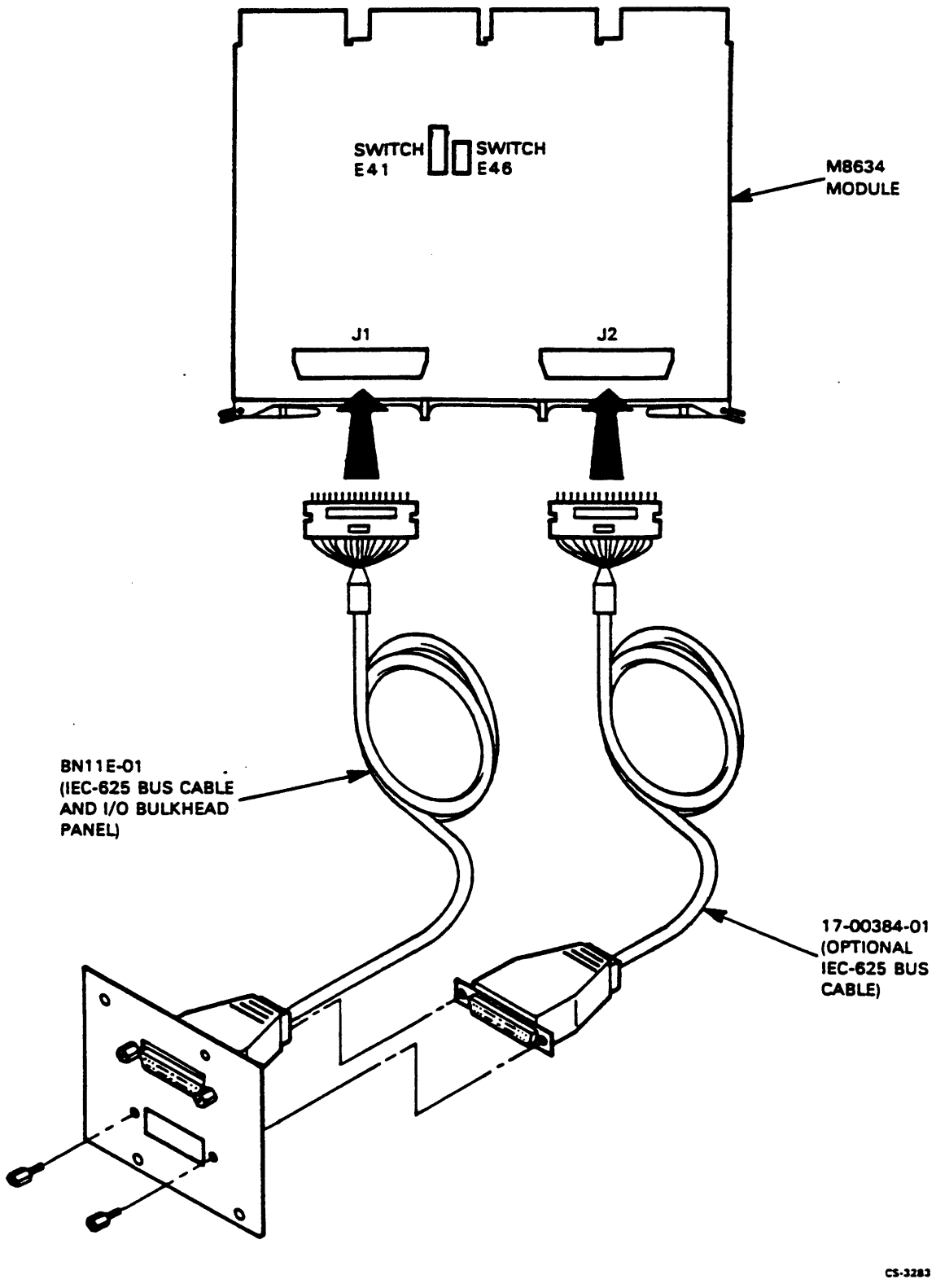


Figure 2-9 IEC Cable Connections, IEQ11-AA

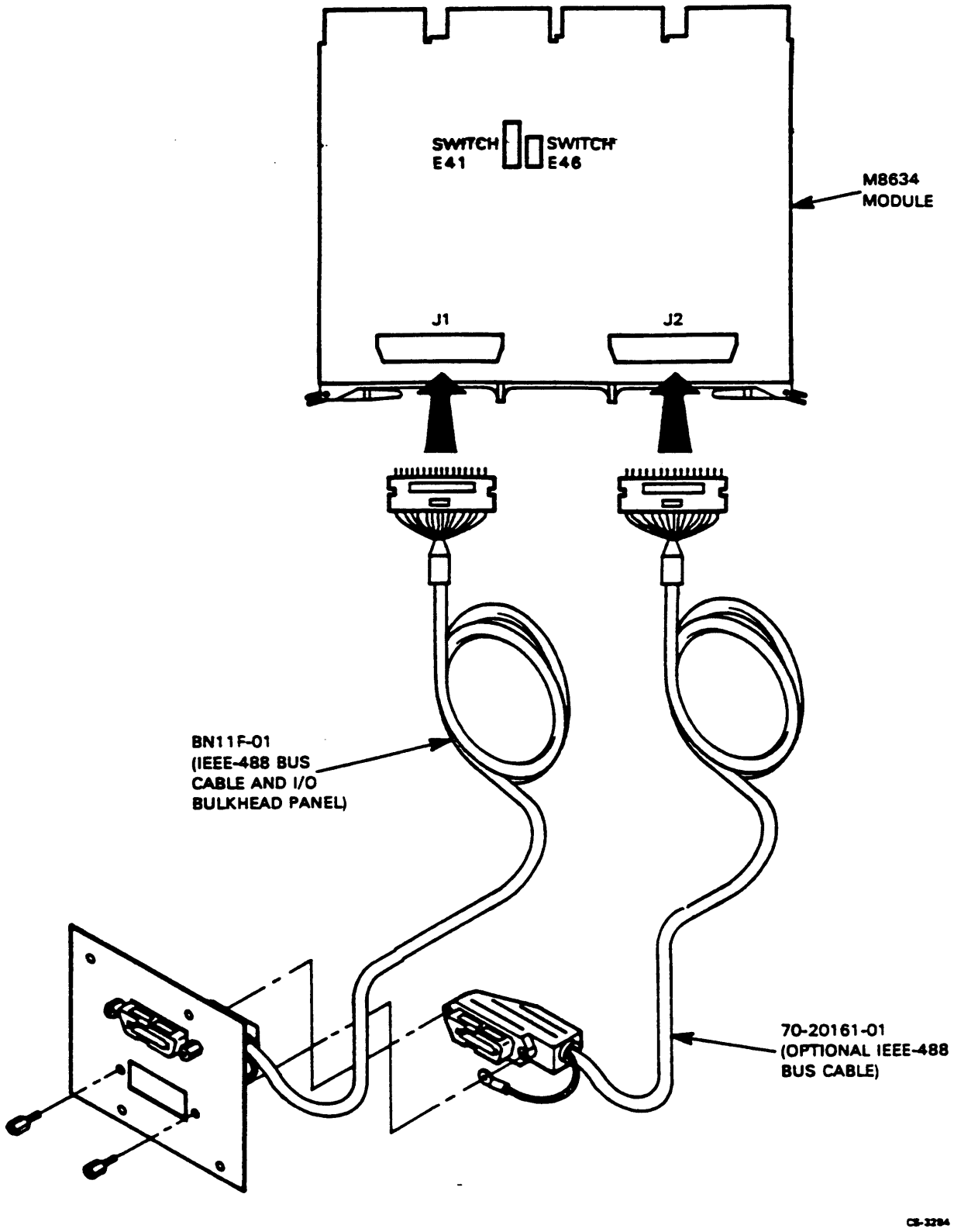


Figure 2-10 IEEE Cable Connections, IEQ11-AB

2.15.2 Testing the IEC/IEEE Bus Cables

To test the IEC/IEEE Bus cables that interconnect the M8634 module to the I/O bulkhead panel, the following procedure is performed.

Step	Procedure
1	Both channels on the IEQ11-A option must be used; that is, the following must be installed: • IEC installation -- an IEC bus cable with I/O bulkhead panel (BN11E-Ø1 or BN11J-ØC) and an optional IEC Bus cable (17-ØØ384-Ø1 or BN11M-ØC). Refer to Figure 2-11 or Figure 2-13. • IEEE installation -- an IEEE bus cable with an I/O bulkhead panel (BN11F-Ø1 or BN11K-ØC), and an optional IEEE bus cable (7Ø-2Ø161-Ø1 or BN11L-ØC). Refer to Figure 2-12 or Figure 2-14.
2	Interconnect both channels by performing the following: • IEC installation -- connect the two channels by installing an instrument bus cable, dual IEC-625 connectors on both ends (BNØ1C-Ø2) to the I/O bulkhead panel (refer to Figure 2-11 or Figure 2-13). • IEEE installation -- connect the two channels by installing an instrument bus cable, dual IEEE-488 connector on both ends (BNØ1A-Ø2) to the I/O bulkhead panel (refer to Figure 2-12).
3	Perform the module verification procedure in Section 2.13, ignoring the references in Section 2.13 to the BC08S-Ø1 test cable.

NOTE

The BN11K-ØC/BN11J-ØC is used on the MICRO systems. All cabling for testing applies, and test procedures do not change.

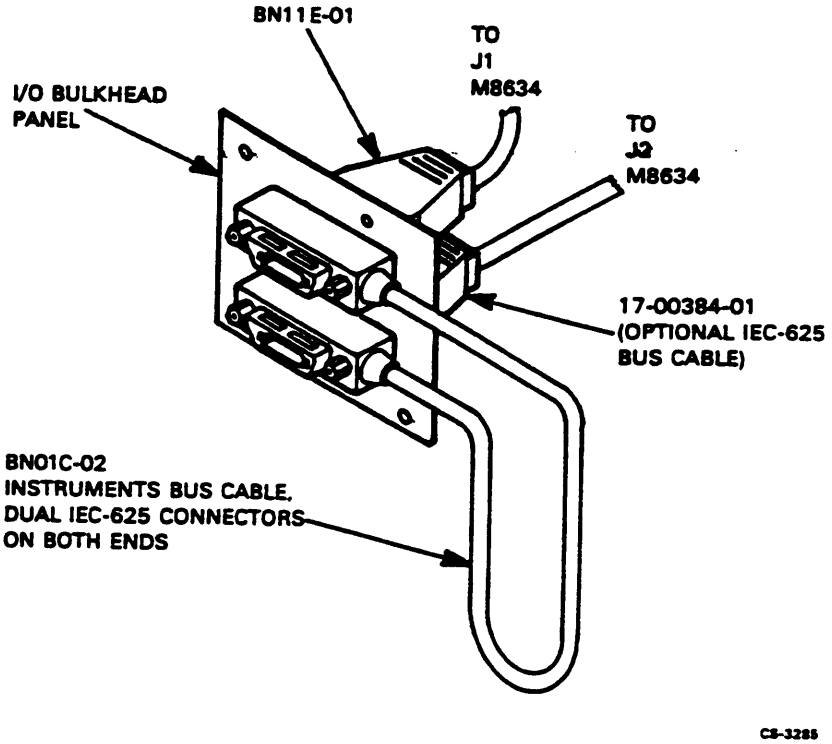


Figure 2-11 IEC Cable Test Configuration, IEQ11-AA

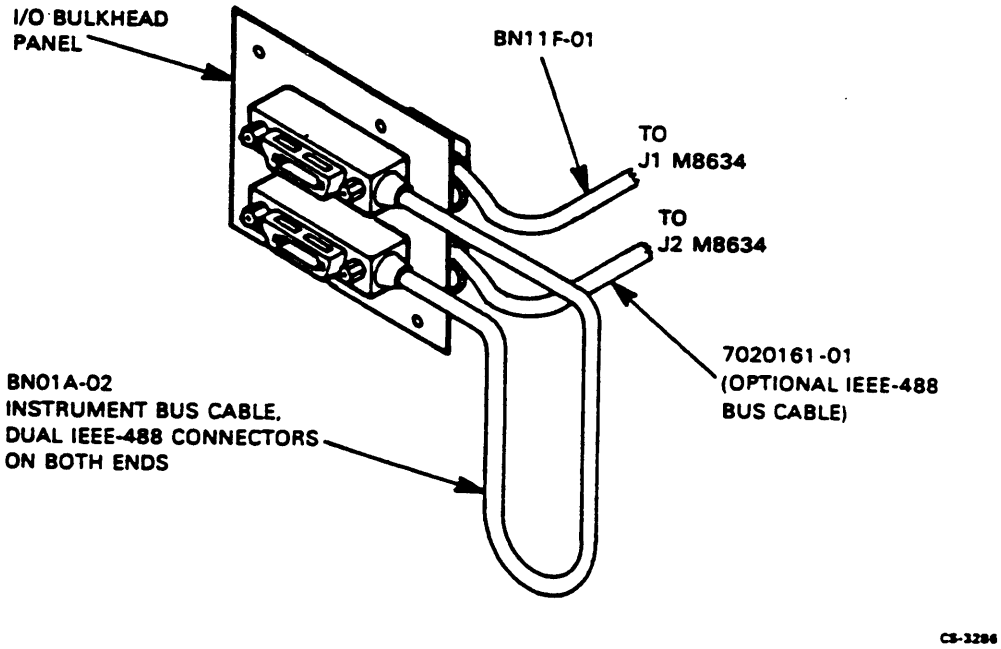


Figure 2-12 IEEE Cable Test Configuration, IEQ11-AB

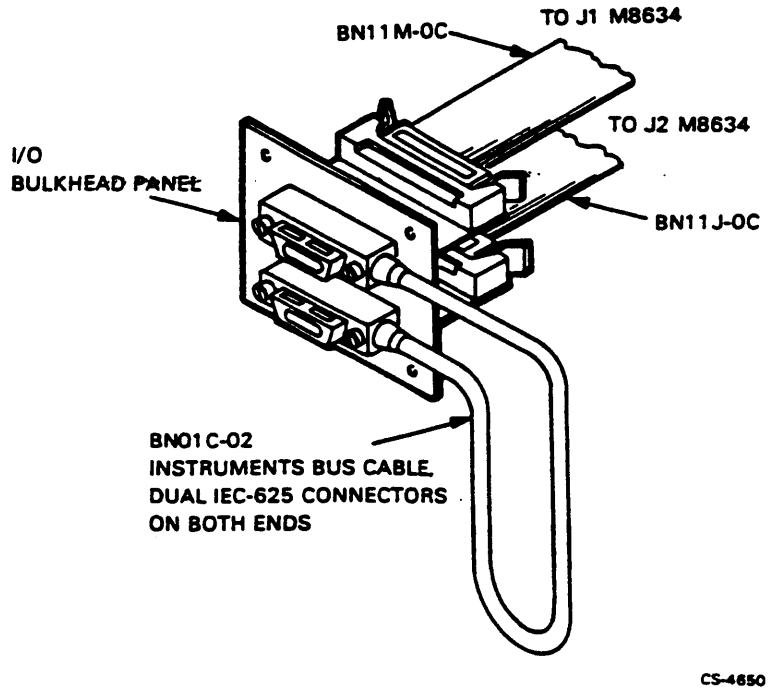


Figure 2-13 IEC Cable Test Configurations, IEQ11-AC

NOTE
Ensure that Pin A of connector J1 or J2 (M8634) is connected to Pin A of connector assembly.

Table 2-9 IEQ11-A Installation Cables

	IEQ11-AA	IEQ11-AB	IEQ11-AC	IEQ11-AD
Bulkhead Cable Assembly (included with option)	BN11E-01	BN11F-01	BN11J-0C	BN11K-0C
Optional Cable to Second Controller on M8634	17-00384-01	7020161-01	BN11M-0C	BN11L-0C

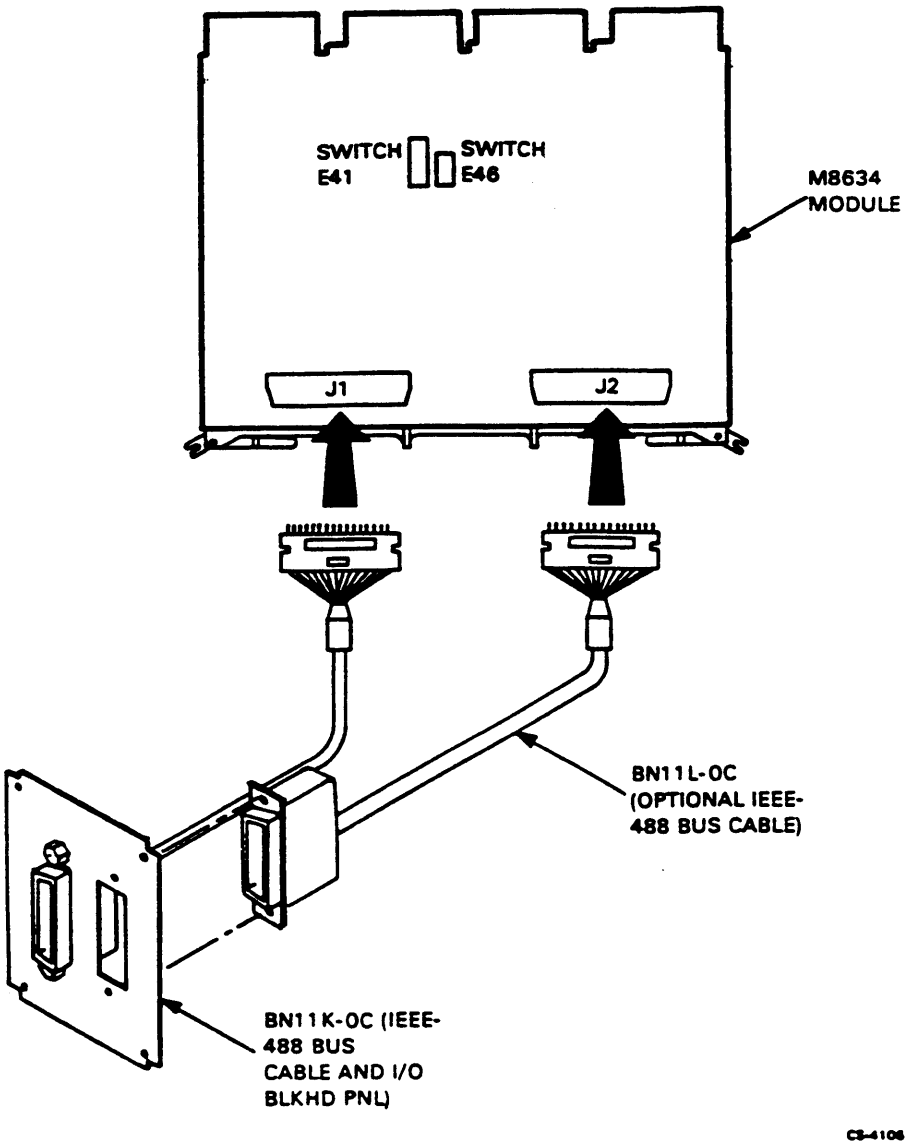


Figure 2-14 IEEE Cable Connections, IEQ11-AD

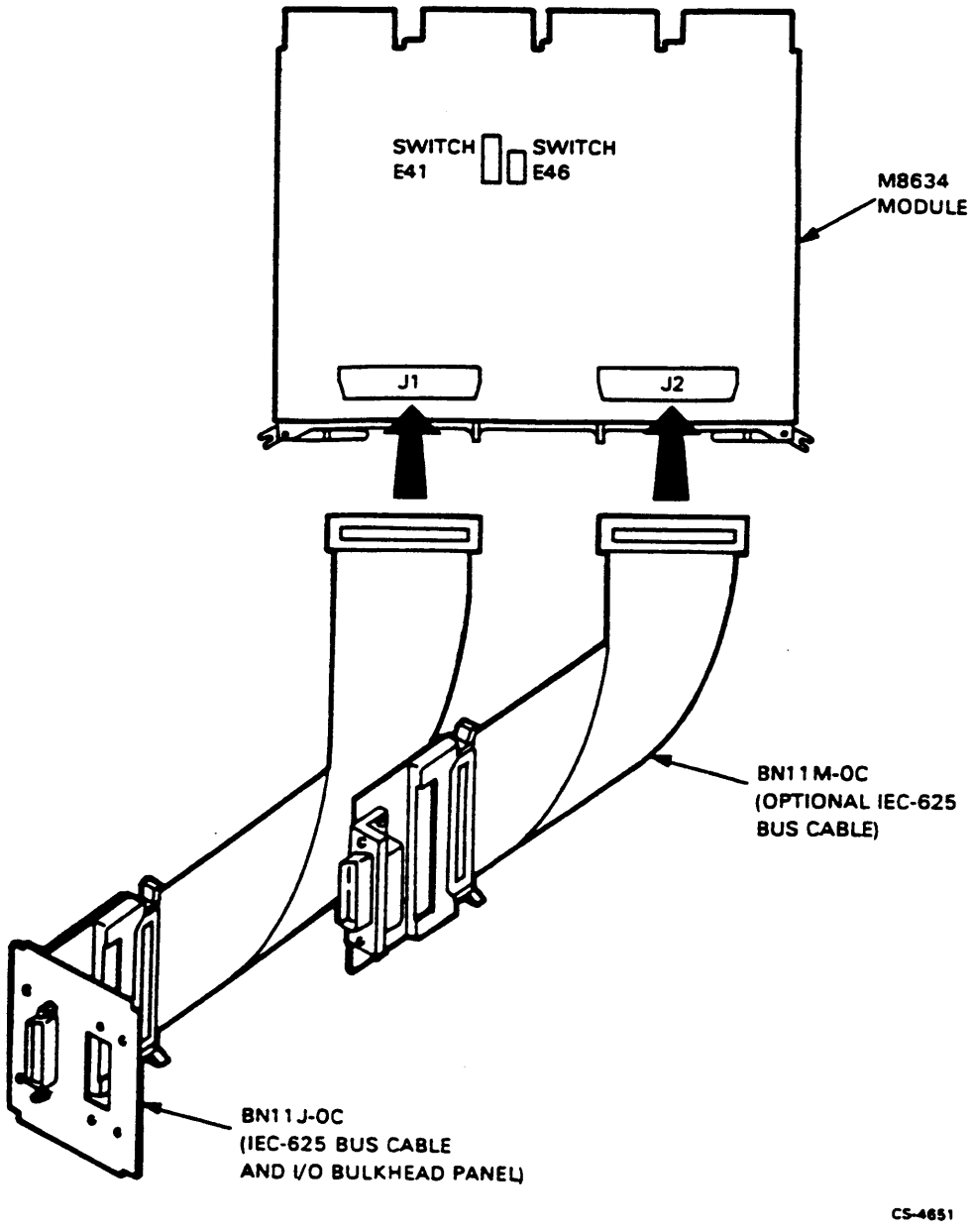


Figure 2-15 IEC Cable Connections, IEQ11-AC

3.1 INTRODUCTION

The following section describes the IEU11-A option operation on the UNIBUS. The description for the IEQII-A option operation on the Q-bus is identical to the IEU11-A option, except where it is noted. All software control of the IEU11-A is performed by means of device registers. These device registers are assigned eight UNIBUS addresses. PDP-11 or VAX-11 instructions can be used to read and write these registers through these assigned addresses.

The IEU11-A performs an interface function between a UNIBUS and two independent IEC/IEEE bus systems. Since the IEC/IEEE bus systems are independent of each other, the IEU11-A has two identical register sets. To reduce the number of UNIBUS addresses, the two UNIBUS register sets are multiplexed. A MUX bit, which can be controlled by either of the two control status registers, distinguishes between register sets 1 and 2. With the advantage of MUX bit, only eight UNIBUS addresses are needed to address the sixteen UNIBUS registers.

3.1.1 UNIBUS Addresses

The UNIBUS address assignments are changed by means of a DIP switchpack on the IEU11-A module. The other seven UNIBUS addresses are relative to this base address that is set in the switchpack. The switchpack has a range of 760000 to 777777. The factory set address (base address) is 764100 for both the IEU11-A option and the IEQ11-A option. Table 3-1 lists the registers and their addresses. Registers that are preceded with IEEE are resident in the TMS 9914A.

Table 3-1 UNIBUS Addresses

Register	Mnemonic	Address (Octal)
IEEE Status Register	ISR 1 and 2	764100 (see Note 1)
IEEE Interrupt Register	IIR 1 and 2	764102
IEEE Command Register	ICR 1 and 2	764104
IEEE Data Register	IDR 1 and 2	764106
Control and Status	CSR 1 and 2	764110
Bus Address Register	BAR 1 and 2	764112
Byte Count Register	BCR 1 and 2	764114
Match Character Register	MCR 1 and 2	764116

NOTE

This address is the standard hardware address. It is the only one that is freely-selectable via dip switch E98.

3.1.2 Register Bit Abbreviations

Table 3-2 lists abbreviations that describe what action can be done to a register bit. These abbreviations are used in the register bit format figures.

Table 3-2 Register Bit Abbreviations

Abbreviation	Action
R	Read only bit; cannot be set or cleared.
W	Write only bit; always read as zero.
R/W	Read/Write bit; may be set or reset.
R/C	Read/Clear bit; may be read and is cleared after reading the appropriate register.
R/WØ	Read/Write Zero bit; may be read and cleared, but cannot be set.
Not Used	Not used: reading of such bits results in receiving a zero or one - writing of such bits will have no effect on the appropriate register.

3.2 IEU11-A DEVICE REGISTERS

This section describes the device registers used in the IEU11-A option. The IEU11-A option has two identical register sets. One register set controls one IEC/IEEE bus channel, while the other register set controls the other IEC/IEEE bus channel. Since both register sets are identical, only one register set is described. The IEEE registers (those registers that reside in the TMS 9914A), are listed in Table 3-3 (read-only registers) and Table 3-4 (write-only registers).

Table 3-3 TMS 9914A Read Registers

UNIBUS Address Offset (octal) (Word Read Only)	Register Name	Bit Assignment							
		07	06	05	04	03	02	01	00
0	Address Status	REM	LLO	ATN	LPAS	TPAS	LADS	TADS	ulpa
1	Bus Status	ATN	DAV	NDAC	NRFD	EOI	SRQ	IFC	REN
2	Int Status 0	INT0	INT1	BI	BO	END	SPAS	RLC	MAC
3	Int Status 1	GET	ERR	UNC	APT	DCAS	MA	SRQ	IFC
4	Cmd Pass Thru	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1
5	*	xx	xx	xx	xx	xx	xx	xx	xx
6	*	xx	xx	xx	xx	xx	xx	xx	xx
7	Data In	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1

* Reserved to DIGITAL™

Table 3-4 TMS 9914A Write Registers

UNIBUS Address Offset (octal)	Register Name	Bit Assignment							
		07	06	05	04	03	02	01	00
0	Int Mask 0	xx	xx	BI	BO	END	SPAS	RLC	MAC
1	Int Mask 1	GET	ERR	UNC	APT	DCAS	MA	SRQ	IFC
2	*	xx	xx	xx	xx	xx	xx	xx	xx
3	Address	edpa	dal	dat	A5	A4	A3	A2	A1
4	Serial Poll	S8	rsv1	S6	S5	S4	S3	S2	S1
5	Auxiliary Cmd	cs	xx	xx	f4	f3	f2	f1	f0
6	Parallel Poll	PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1
7	Data Out	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1

* This address is not decoded by the TMS 9914A. A write to this location will have no effect on the device, as if a write had not occurred.

3.2.1 IEEE Status Register (ISR)

The IEEE status register consists of four TMS 9914A internal registers: Interrupt Mask Register Ø, Interrupt Mask Register 1, Address Status Register, and Bus Status Register. These four registers use the same UNIBUS address. Reading or writing to this UNIBUS address does not access the same TMS 9914A internal register, since two registers are read only and the other two are write only (refer to Figures 3-1 and 3-2).

To read the ISR requires an UNIBUS DATI cycle. Since the DATI cycle is a word (16 bits) data transfer, two read cycles to the TMS 9914A internal registers are automatically performed by the IEU11-A logic to execute one UNIBUS READ cycle.

To write to the ISR requires a UNIBUS DATOB cycle. Since the ISR is only byte-loadable, one UNIBUS WRITE cycle will load either the LOB (low order byte) or the HOB (high order byte) of the ISR. However, if a DATO cycle is performed, only the LOB of the ISR is loaded.

3.2.1.1 Interrupt Mask Register Ø and Interrupt Status Register Ø -- The Interrupt Mask and Interrupt Status registers operate independently of each other. The status bits will always be set when the appropriate events occur regardless of the state of the corresponding mask bit.

All interrupt bits, with the exception of INTØ and INT1 (which are not storage bits), are edge triggered and set when the appropriate condition becomes true. The storage bits are cleared immediately after the corresponding Interrupt Status Register is read by the host MPU. If an interrupt condition becomes true during this read operation, then the event is stored. The corresponding bit is set when the read operation ends; therefore, no interrupts are lost. In addition to being cleared by a read operation, the BO interrupt is also cleared by writing to the Data Out Register, and the BI interrupt is cleared by reading the Data In Register.

The interrupt status bits are cleared and held in the Ø condition while Software Reset (swrst) is set.

The corresponding bit of the Interrupt Mask register must be set to a 1 if an interrupt status bit is to cause an external interrupt ($\overline{INT}$ Low) when it is set. For example:

$$\overline{INT}=\overline{INT\ STATUS.INT\ MASK}$$

The mask register is not cleared by 'swrst' or the Hardware Reset pin ($\overline{RESET}$) and will power on in a random state. It must, therefore, be written to by the host MPU before 'swrst' is cleared to avoid extraneous interrupts (see Section 3.2.3.2 for operation of 'swrst').

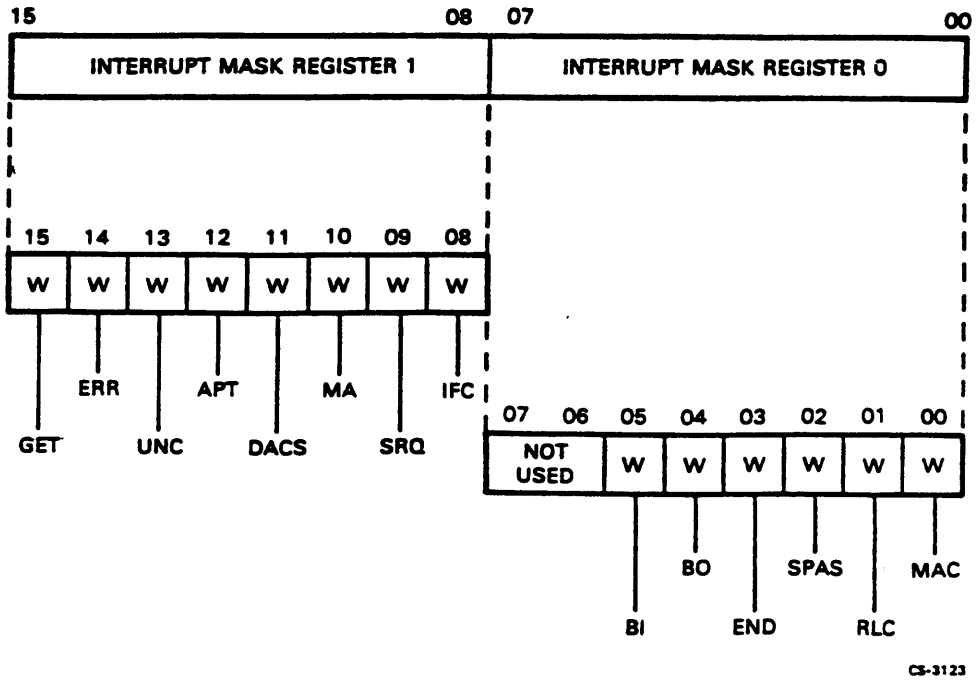


Figure 3-1 IEEE Status Register (Write Only)

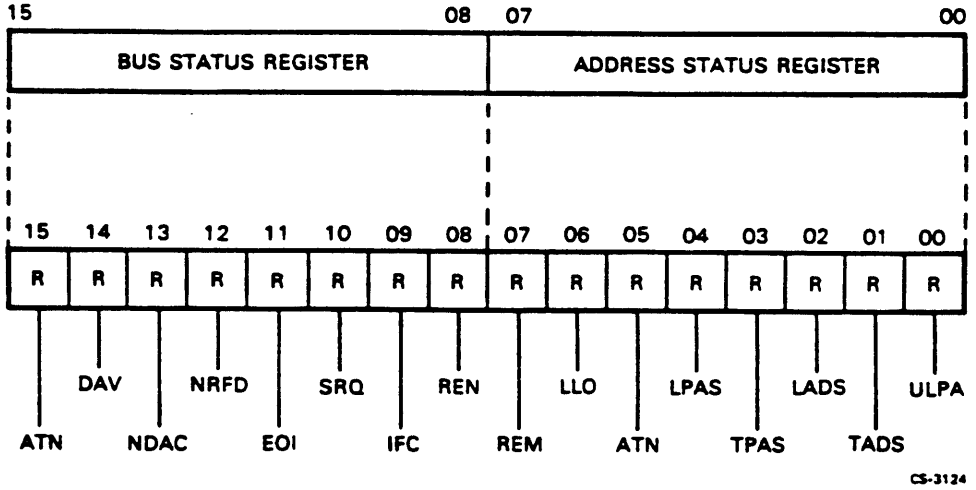


Figure 3-2 IEEE Status Register (Read Only)

The INTØ and INT1 bits of the Interrupt Status Register are not true status bits. INT1 will be true if there are any unmasked interrupt status bits set to a 1 in Interrupt Status Register 1. INTØ will be true if any of bits <Ø5:ØØ> of Interrupt Status Register Ø are unmasked and set to a 1. If either INT1 or INTØ is true, then the External Interrupt pin (INT) will be pulled low, provided that the Disable All Interrupts feature (dai) has not been set.

Figure 3-1 shows the bit format for the interrupt mask register Ø. Table 3-5 defines the interrupt mask register Ø bits. The conditions that set these bits (shown in parenthesis), are defined in terms of the state diagrams in Section 3.3. Each bit is set on the rising edge of the condition shown.

Table 3-5 Interrupt Mask Register Ø and Interrupt Status Register Ø Bit Description

Bit	Name (Mnemonic)	Function
7	Interrupt 1 (INT1)	This will be a 1 when an unmasked status bit in Interrupt Status Register 1 is set to a 1.
6	Interrupt Ø (INTØ)	This will be a 1 when any of bits <Ø5:ØØ> of Interrupt Status Register Ø is unmasked and set to a 1.
5	Byte In (BI)	A data byte has been received in the Data In Register. If the mask bit is not set, no interrupt is generated, but an RFD holdoff will still occur before the next data byte is accepted. If the Shadow Handshake feature is used, this status bit will not be set. This bit is cleared by reading the Data In Register as well as after Interrupt Status Register Ø has been read. (Set On: ACDS1.LACS)
4	Byte Out (BO)	This bit is set when the Data Out Register is available to send a byte over the IEC/IEEE bus. This byte may be either a command (if the device is a controller), or data (if the device is a talker). It is set when the device becomes an active talker or controller, but will not occur if the Data Out Register has been loaded with a byte that has not been sent. Subsequently, it will occur after each byte has been sent and the TMS 9914A register returns to SGNS. This bit is cleared by writing to

Table 3-5 Interrupt Mask Register Ø and Interrupt Status Register Ø Bit Description (Cont)

Bit	Name (Mnemonic)	Function
		the Data Out Register as well as by reading Interrupt Status Register Ø. (Set On: SGNS.CACS+SGNS. TACS.$\overline{SHFS}$)
		NOTE When a controller addresses itself as a talker and then goes to standby, there will be a momentary transition of the source handshake into SIDS before TACS becomes true and it re-enters SGNS. Under these circumstances, the TMS 9914A register is guaranteed to give a BO interrupt on re-entering 'SGNS'.
3	End (END)	This bit indicates that a byte just received by a listener was the last byte in a string (that is, it was received with the EOI line true). It is set at the same time as the BI interrupt. (Set On: (ACDS1.LACS.EOI))
2	Serial Poll/ Active (SPAs)	This bit indicates that the TMS 9914A register has requested service by means of rsv1 or rsv2 (in the Serial Poll Register or Poll Register or Auxiliary Command Register) and has been polled in a serial poll. It is set on the false transition of STRS when the serial poll status byte is sent. (Set On: STRS.SPAS.(APRS1+ APRS2))
1	Remote/Local Change (RLC)	This bit is set by any transition between local and remote states in the Remote/Local function. (Set On: (LOCS-REMS)+(REMS-LOCS)+ (LWLS-RWLS)+(RWLS-LWLS))
Ø	My Address Change (MAC)	This bit indicates that a command has been received from the IEC/IEEE bus which has resulted in the change of the addressed state of the TMS 9914A register. It will not occur if secondary addressing is being used, or indicate that the TMS 9914A register has been readdressed on its other primary address. (Set On: ACDS1. (MTA.TADSUNT+OTA.TADS+MLA.LADS+UN.LADS))

3.2.1.2 Interrupt Mask Register 1 and Interrupt Status Register 1 -- The operation of Interrupt Mask and Status Register 1 is similar to that of Interrupt Mask and Status Register Ø except that all bits are true storage bits. The status bits are cleared only following the register being read and by 'swrst'.

There is one distinct group of interrupts in this register: GET, UNC, APT, DCAS, MA. These interrupts are all set in response to commands received over the bus and, if unmasked, a Data Accepted (DAC) holdoff will occur when the interrupt in question is set. It may be released with a 'dacr' auxiliary command. This is further discussed in Section 3.3.2.

The mask bit of the APT interrupt is further used in the talker and listener functions. When the interrupt is unmasked, the talker and listener functions of the TMS 9914A register implement the extended talker and extended listener functions of IEEE-488. Otherwise, these functions implement the talker and listener functions of IEEE-488.

Figure 3-1 shows the bit format for the Interrupt Mask Register 1 bits. The conditions that set these bits (shown in parenthesis) are defined in terms of the state diagrams in Section 3.3.

Table 3-6 Interrupt Mask Register 1 and Interrupt Status Register 1 Bit Description

Bit	Name (Mnemonic)	Function
15	Group Execute Trigger (GET)	This bit is set if a Group Execute Trigger command is received. A DAC holdoff occurs if the interrupt is unmasked.
14	Error (ERR)	This bit is set if the source handshake becomes active and finds that the NDAC and NRFD lines are both high. This indicates that, for whatever reason, there are no acceptors on the bus. (Set On: SERS)
13	Unrecognized Command (UNC)	This bit is set if a command has been received that has no meaning to the TMS 9914A register. Unrecognized address commands will only cause this interrupt if the device is LADS (except for TCT, which will only interrupt in TADS). Secondary commands will cause this interrupt only if the 'pts' auxiliary command has been previously set. A DAC holdoff will occur if this interrupt is unmasked, which effectively enables the command pass through feature. Unrecognized commands may be inspected in

Table 3-6 Interrupt Mask Register 1 and Interrupt Status Register 1 Bit Description (Cont)

Bit	Name (Mnemonic)	Function
		the Command Pass Through Register before this holdoff is released. (Set On: ACDS1.(UCG.LLO.SPE.SPD.DCL+ACG.GET.GTL.SDC.TCT.LADS+TCT.TADS+SCG.pts))
12	Address Pass Through (APT)	Unmasking this interrupt enables secondary addressing. It is set if a secondary command is received provided that the last primary command received was a primary talk or listen address of the TMS9914A register. A DAC holdoff will occur and the secondary address may be read from the Command Pass Through Register. The holdoff may be released by a 'dacr' auxiliary command and the 'cs' bit of the Auxiliary Command Register is used to indicate that a valid (cs = 1) or an invalid (cs = Ø) secondary has been identified by the host MPU. (Set On: ACDS1.SCG.(LPAS+TPAS))
11	Device Clear Active State (DCAS)	This bit is set when a device clear command (DCL) is received or when a selected device clear (SDC) is received with the TMS 9914A register in LADS. This will cause a DAC holdoff if unmasked. (Set On: ACDS1.(DCL+SDC.LADS))
1Ø	Service Request (SRQ)	This bit is provided for the benefit of the controller, which should execute a serial poll in response to this interrupt. It is set when the SRQ line becomes true. (Set On: SRQ.($\overline{CIDS}$+$\overline{CADS}$))
9	My Address (MA)	This bit is set when the TMS 9914A register recognizes its primary talk or listen address. A DAC holdoff will occur if this is unmasked. (Set On: (MLA+MTA).$\overline{SPMS}$.aptmk))
8	Interface Clear (IFC)	This bit is provided for the benefit of devices that are not the System Controller. It is set when the IFC line becomes true and indicates that the TMS 9914A register has been returned to an idle state. If the device is the System Controller, then the IFC interrupt is not set. (Set On: IFCIN)

3.2.1.3 Address Status Register -- Figure 3-2 shows the bit format for the Address Status Register. Table 3-7 describes the Address Status Register bits.

Table 3-7 Address Status Register Bit Description

Bit	Mnemonic	Function
7	REM	The device is in the remote state
6	LLO	Local lockout is in operation
5	ATN	The attention line is low (true) on the bus
4	LPAS	Register TMS 9914A is in the listener primary addressed state
3	TPAS	Register TMS 9914A is the talker primary addressed state
2	LADS (or LACS)	The device is addressed to listen
1	TADS (or TACS)	The device is addressed to talk
Ø	ulpa	This bit shows the LSB of the last address recognized by the TMS 9914A register

3.2.1.4 Bus Status Register -- The host MPU may examine the status of IEC/IEEE bus management lines at the time of reading.

The IFC bit of this register does not indicate a true value if the device is a system controller using the 'sic' auxiliary command.

Figure 3-2 shows the bit format for the bus status register.

3.2.2 IEEE Interrupt Register (IIR)
The IEEE Interrupt Register consists of three TMS9914A internal registers: Interrupt Status Register Ø, Interrupt Status Register 1, and Address Register. These three registers use the same UNIBUS address. Reading or writing to this UNIBUS address does not access all three registers, since two are read only and the other register is write only. Reading requires a DATI cycle, while writing requires a DATOB cycle. The read and write cycles are performed the same as the IEEE status register (refer to Section 3.2.1 for a description).

3.2.2.1 Address Register -- Figure 3-3 shows the bit format for the address register. Table 3-8 describes the address register bits.

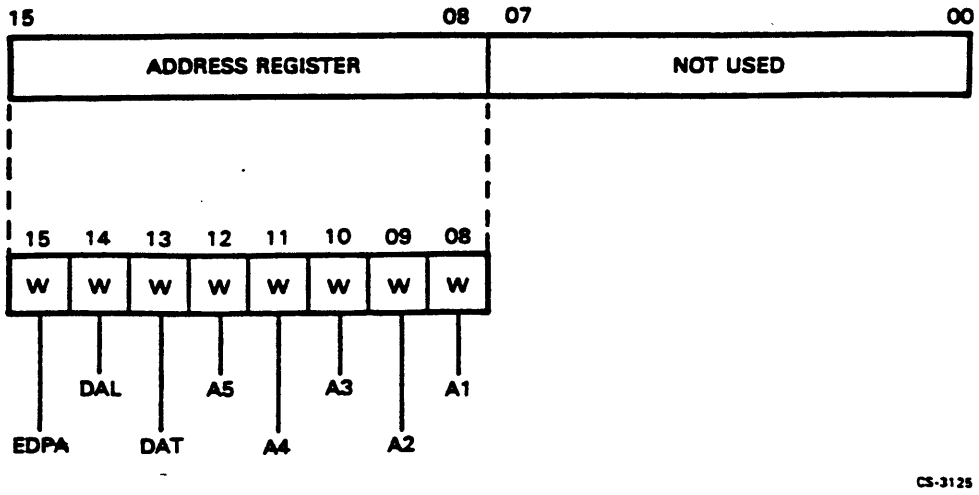


Figure 3-3 IEEE Interrupt Register (Write Only)

Table 3-8 Address Register Bit Description

Bit	Mnemonic	Function
15	edpa	Enable dual primary addressing mode
14	dal	Disable listener function
13	dat	Disable talker function
<12:08>	A5-A1	Primary address of the TMS 9914A register

Bits A5-A1 of this register contain the primary address of the device. IEEE-488 1975/78 does not allow a device to be assigned the value 11111 for bits A5-A1. When 'swrst' is true at power-up, or if set by the host MPU, the TMS 9914A register is held in an idle state. During this time the host MPU may load the primary address of the device into these bits. Often, this will be read from an Address Switch Register.

The 'edpa' bit is used to enable the dual addressing mode of the TMS 9914A register. It causes the LSB of the address to be ignored by the address comparator giving two consecutive primary addresses for the device. The address from which the TMS 9914A register was selected is indicated by the 'ulpa' bit of the Address Status Register.

The Address Register is not cleared by 'swrst' or hardware reset.

3.2.2.2 Interrupt Status Register Ø -- Figure 3-4 shows the bit format for the Interrupt Status Register Ø. Table 3-5 and Section 3.2.1.1 describes the Interrupt Status Register Ø bits.

3.2.2.3 Interrupt Status Register 1 -- Figure 3-4 shows the bit format for the Interrupt Status Register 1. Table 3-6 and Section 3.2.1.2 describes the Interrupt Status Register 1 bits.

3.2.3 IEEE Command Register (ICR)
The IEEE Command Register consists of three TMS 9914A internal registers: Auxiliary Command Register, Serial Poll Register, and Command Pass Through Register. These three registers use the same UNIBUS address. Reading or writing to this UNIBUS address does not access all three registers, since two are write only and the other register is read only. Reading requires a DATI cycle, while writing requires a DATOB cycle. The read and write cycles are performed the same as the IEEE status register (refer to Section 3.2.1 for a description).

3.2.3.1 Auxiliary Command Register -- Auxiliary commands are used to enable and disable most of the selectable features of the TMS 9914A register and to initiate many of the device actions. The desired feature is selected by writing a byte to this register with the appropriate value in bits f4-fØ. These values are given in Table 3-9. Figure 3-5 shows the bit format of the Auxiliary Command Register.

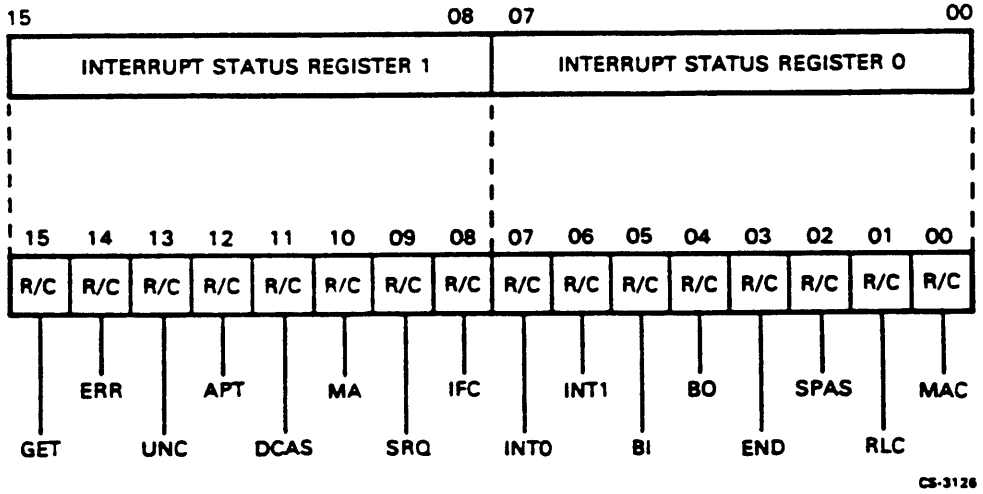


Figure 3-4 IEEE Interrupt Register (Read Only)

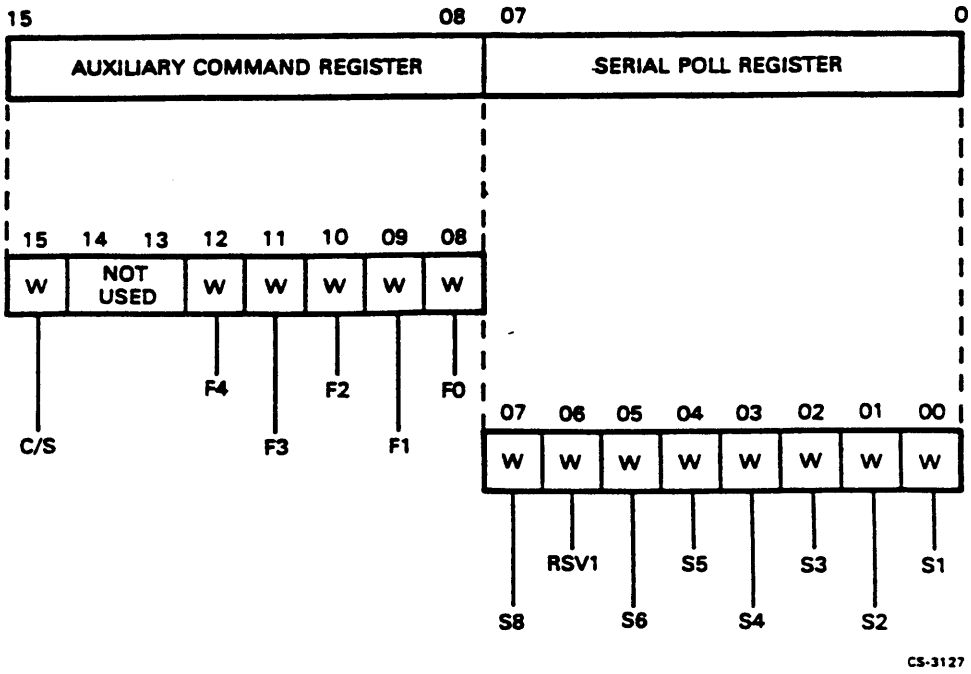


Figure 3-5 IEEE Command Register (Write Only)

The 'cs' bit is used in most cases when the feature selected by f4-fØ is of the clear/set type. The feature is enabled if 'cs' = '1' and disabled if 'cs' = 'Ø'. The holdoff on all data (hdfa) feature is an example of such a feature. Other auxiliary commands initiate an action of the TMS 9914A register, such as release RFD holdoff (rhdf). In most cases, the 'cs' bit is unused and ignored by these commands.

All the clear/set auxiliary commands are cleared by the hardware RESET pin except 'swrst,' which is set true by RESET.

The force group execute trigger (fget) and return to local (rtl) auxiliary commands have a clear/set mode of operation and a pulsed mode of operation. They behave as normal clear/set features, but if they are written with 'cs' = 'Ø' when they have not been previously set, then they will pulse true. Using the 'fget' command in this manner will produce a pulse of approximately 1 microsecond at the TR pin (with a 5 MHz clock). The 'rtl' command in this way will cause a return to one of the local states (assuming local lockout is not in force) but the TMS 9914A register may re-enter the remote state next time the listen address occurs.

NOTE

The TR pin signal is not available in the IEU11-A option.

Table 3-9 Auxiliary Commands

c/s	f4	f3	f2	f1	f0	Mnemonic	Features
0/1	0	0	0	0	0	swrst	Software reset
0/1	0	0	0	0	1	dacr	Release DAC holdoff
na	0	0	0	1	0	rhdf	Release RFD holdoff
0/1	0	0	0	1	1	hdfa	Holdoff on all data
0/1	0	0	1	0	0	hdfe	Holdoff on EOI only
na	0	0	1	0	1	nbaf	New byte available false
0/1	0	0	1	1	0	fget	Force group execute trigger
0/1	0	0	1	1	1	rtl	Return to local
na	0	1	0	0	0	feoi	Send EOI with next byte
0/1	0	1	0	0	1	lon	Listen only
0/1	0	1	0	1	0	ton	Talk only
na	0	1	0	1	1	gts	Go to standby
na	0	1	1	0	0	tca	Take control asynchronously
na	0	1	1	0	1	tcs	Take control synchronously
0/1	0	1	1	1	0	rpp	Request parallel poll
0/1	0	1	1	1	1	sic	Send interface clear
0/1	1	0	0	0	0	sre	Send remote enable
na	1	0	0	0	1	rqc	Request control
na	1	0	0	1	0	rlc	Release control
0/1	1	0	0	1	1	dai	Disable all interrupts
na	1	0	1	0	0	pts	Pass through next secondary
0/1	1	0	1	0	1	stdl	Short T1 settling time
0/1	1	0	1	1	0	shdw	Shadow handshake
0/1	1	0	1	1	1	vstdI	Very short T1 delay
0/1	1	1	0	0	0	rsv2	Request Service Bit 2

3.2.3.2 Auxiliary Commands --

Software Reset (swrst) 0/1xx00000

Setting this command causes the TMS 9914A register to be returned to a known idle state during which it will not take part in any activity on the IEC/IEEE. This auxiliary command is set by the power-on RESET and the chip should be configured while 'swrst' is set. Configuration should include writing the address of the device into the Address Register, writing mask values into the Interrupt Mask Registers, and selecting the desired features in the Auxiliary Command Register and Address Register. After this, 'swrst' may be cleared, at which point the device becomes logically existent on the IEC/IEEE. The Serial Poll Register and Parallel Poll Registers may also be written in this period, but this is not necessary if there is no status to report, as both of these are cleared by the power-on RESET pin. Table 3-10 lists the various states and other conditions forced by 'swrst'.

Table 3-10 Software Reset Conditions

Mnemonic	Description
SIDS	Source idle state
AIDS	Acceptor idle state
TIDS	Talker idle state
TPAS	Talker primary idle state
LIDS	Listener idle state
LPAS	Listener primary state
NPRS	Negative poll response state
LOCS	Local state
CIDS	Controller idle state
SPIS	Serial poll idle state
PPSS	Parallel poll standby state
ADHS	DAC holdoff state
ANHS	RFD holdoff state
AEHS	RFD holdoff on end state
SHFS	Source holdoff state
ENIS	END idle state

NOTE

1. See Section 3 for definition of above.

2. All interrupt status bits are held in a 0 state, but interrupt mask bits are not affected.

Release DAC Holdoff (dacr)0/1xx00001

The Data Accepted (DAC) holdoff allows time for the host microprocessor to respond to unrecognized commands, secondary addresses, and device trigger or device clear commands. The holdoff is released by the MPU when the required action has been taken. Normally the command is loaded with the clear/set bit at zero; however, when used with the address pass through feature, CS is set to one (if the secondary address was valid) or to zero (if invalid).

Release RFD Holdoff (rhdf)naxx00010

Any Ready For Data (RFD) holdoff caused by a 'hdfa' or 'hdfe' is released.

Holdoff on All Data (hdfa)0/1xx00011

A Ready For Data (RFD) holdoff is caused on every data byte until the command is loaded with CS set to zero. The handshake must be completed after each byte has been received by the MPU using the 'rhdf' command.

Holdoff on End (hdfe)0/1xx00100

An RFD holdoff will occur when an end of data string message (EOI true with ATN false) is received over the interface. This holdoff must be released using 'rhdf'.

Set New Byte Available False (nbaf)naxx00101

If a talker is interrupted before the byte just stored in the data out register is sent over the interface, this byte will normally be transmitted as soon as the ATN line returns to the false state. If, as a result of the interrupt, this byte is no longer required, its transmission may be suppressed using the 'nbaf' command.

Force Group Execute Trigger (fget)0/1xx00110

The state of the TR output from the TMS 9914A register is affected when this command is executed. If the CS bit is zero, the line is pulsed high for approximately 5 clock cycles (1 microsecond at 5 MHz). If CS is one, the TR line goes high until 'fget' is sent with CS equal to zero. No interrupts or handshakes are initiated.

NOTE
The TR signal is not available on the IEU11-A option.

Return to Local (rtl)0/1xx00111

Provided the local lockout (LLO) has not been enabled, the remote/local status bit is reset, and an interrupt is generated (if

enabled) to inform the host microprocessor that it should respond to the front panel controls. If the CS bit is set to one the 'rtl' command must be cleared (CS = Ø) before the device is able to return to remote control. If CS is set to zero, the device may return to remote without first clearing 'rtl'.

Force End or Identify (feoi)naxxØ1ØØØ

This command causes the EOI message to be sent with the next data byte. The EOI line is then reset.

Listen Only (lon)Ø/1xxØ1ØØ1

The listener state is activated until the command is sent with CS set to Ø or until deactivated by a bus command.

Talk Only (ton)Ø/1xxØ1Ø1Ø

The talker state is activated until the command is sent with CS set to Ø or until deactivated by a bus command.

NOTE

'ton' and 'lon' are included for use in systems without a controller. However, where the TMS 9914A register is being used as a controller, it utilizes the 'lon' and 'ton' functions to set itself up as a listener or talker, respectively. Care must therefore be taken to ensure these functions are reset if sending UNL or OTA.

Go to Standby (gts)naxxØ1Ø11

Issued by the controller in charge to set the ATN line false.

Take Control Synchronously (tcs)naxxØ11Ø1

Control is again taken by the controller in charge, and ATN is asserted. If the controller is not a true listener, the shadow handshake command must be used to monitor the handshake lines so that the TMS 9914A register is synchronous with the talker/listeners and only sends ATN true at the end of byte transfer. This ensures that no data is lost or corrupted.

Request Parallel Poll (rpp)Ø/1xxØ111Ø

This is executed by the controller in charge to send the parallel poll command over the interface (the TMS 9914A register must be in the Controller Active State so that the Attention line is asserted). The poll is completed by reading the Command Pass Through Register to obtain the status bits, then sending 'rpp' with the CS bit at zero.

Take Control Asynchronously (tca)naxx01100

This command is used by the controller in charge to set the attention line true and to gain control of the interface. The command is executed immediately and data corruption or loss may occur if a talker/listener is in the process of transferring a data byte.

Send Interface Clear (sic)0/1xx01111

The IFC line is set true when this command is sent with CS set to one. This must only be sent by the system controller and should be reset (CS = 0) after the IEEE minimum time for IFC has elapsed (100 microseconds). The system controller is put into the controller active state.

Send Remote Enable (sre)0/1xx10000

Issued by the system controller to set the REN line true and send the remote enable message over the interface, REN is set false by sending 'sre' with CS at zero.

Request Control (rqc)naxx10001

When the TCT command has been recognized by means of the unidentified command pass through, this command is sent by the MPU. The TMS 9914A register waits for the ATN line to go false and then enters the controller active state (CACS).

Release Control (rlc)naxx10010

This command is used after TCT has been sent and handshake completed to release the ATN line and pass control to another device.

Disable All Interrupts (dai)0/1xx10011

The INT line is disabled, but the interrupt registers and any holdoffs selected are not affected.

Pass Through Next Secondary (pts)naxx10100

This feature may be used to carry out a remote configuration of a parallel poll. The parallel poll configure command (PPC) is passed through the TMS 9914A register as an unrecognized addressed command and is identified by the MPU. The 'pts' command is loaded, and the next byte received by the TMS 9914A register is passed through by means of the Command Pass Through Register. This would be the parallel poll enable (PPE), which is read by the microprocessor.

Set T1 Delay (std1)1xx10101

The T1 delay time can be set to 6 clock cycles (1.2 us at 5 MHz) if this command is sent with the CS bit at one. The T1 delay time

is 11 clock cycles (2.2 microseconds at 5 MHz) following a power-on reset or if the command is sent with CS set to zero.

Shadow Handshake (shdw)0/1xx10110

This feature enables the controller in charge to carry out the listener handshake without participating in a data transfer. The Data Accepted line (DAC) is pulled true a maximum of 3 clock cycles after Data Valid (DAV) is received, and Not Ready For Data (NRFD) is allowed to go false as soon as DAV is removed.

The shadow handshake function allows the tcs' command to be synchronized with the Acceptor Not Read State (ANRS) so that ATN can be re asserted without causing the loss or corruption of data byte. The END interrupt can also be received and causes an RFD holdoff to be generated.

Very Short T1 Delay (vstd1)0/1xx10111

If this feature is enabled the GPIB settling time (T1) will be reduced to 3 clock cycles (600 ns at 5 MHz) on the second and subsequent data bytes when ATN is false. Otherwise the IEC/IEEE settling time is determined by the stdl feature.

Request Service Bit 2 (rsv2)0/1xx11000

The rsv2 bit performs the same function as the rsv1 bit (see Section 2.1.8) but provides a means of requesting service which is independent of the Serial Poll Register. This allows minor updates to be made to the Serial Poll Register without affecting the state of the request service.

In addition, rsv2 is cleared when the serial poll status byte is sent to the controller during a serial poll. It is therefore used in situations where a service request is simply a request from an instrument for the controller to poll its status. As soon as this happens rsv2 is cleared since the reason for requesting service has been satisfied. This eliminates the burden of clearing the bit from the host MPU, but also guarantees that rsv2 is cleared before another serial poll can occur If this were not so, there would be a possibility of a second status byte being sent with the RQS message true, which could result in confusion for the controller (rsv2 is cleared on. SPAS (APRS1+APRS2).STRS).

3.2.3.3 Serial Poll Register -- Figure 3-5 shows the bit format for the serial poll register.

Bits S8, S6 S1 of this register are sent out over the IEC/IEEE when the device is addressed during a serial poll. They are cleared by a hardware reset but not by 'swrst' and may therefore be set up during configuration of the chip. These bits are fully double buffered and if the register is written to while the device is addressed during a serial poll (serial poll active state,

SPAS), the value written is saved, and these bits are updated when SPAS is terminated.

The rsv1 bit provides an input to the service request function of the TMS 9914A register and is used to instruct this to request that the controller service the device. When rsv1 is set true, the SRQ line is pulled true on the IEC/IEEE bus, and the controller typically responds by setting up a serial poll to obtain the status of all instruments on the bus that may require service. When the TMS 9914A register is addressed to send its status byte, SRQ is set false, and the status byte is sent with the RQS message true on DIO7. The rsv1 bit must then be cleared and set true again if service is to be requested a second time. The SPAS interrupt is set immediately following the status byte being sent.

The rsv1 bit is also cleared by the hardware reset pin but not by 'swrst'. It is not double-buffered, but the service request function comprehends changes in the state of rsv1 while the device is in SPAS. The Serial Poll Register may therefore be written to any time.

3.2.3.4 Command Pass Through Register -- Figure 3-6 shows the bit format for the Command Pass Through Register.

This provides a means of directly inspecting the IEC/IEEE data lines (DIO(8-1)). It has no storage and should only be used when the data lines are known to be in a steady state such as will occur during a DAC holdoff or in CPWS during a parallel poll. It is used to read unrecognized commands and secondaries following a UNC interrupt or to read secondary addresses following an APT interrupt. In addition, an active controller uses this register to read the results of a parallel poll at least 2 microseconds after setting the 'rpp' auxiliary command.

3.2.4 IEEE Data Register (IDR)

The IEEE Data Register consists of three TMS 9914A internal registers: Data Out Register, Parallel Poll Register, and Data In Register. These three registers use the same UNIBUS address. Reading or writing to this UNIBUS address does not access all three registers, since two are write only and the other register is read only. Reading requires a DATI cycle, while writing requires a DATOB cycle. The read and write cycles are performed the same as the IEEE status register (refer to Section 3.2.1 for a description).

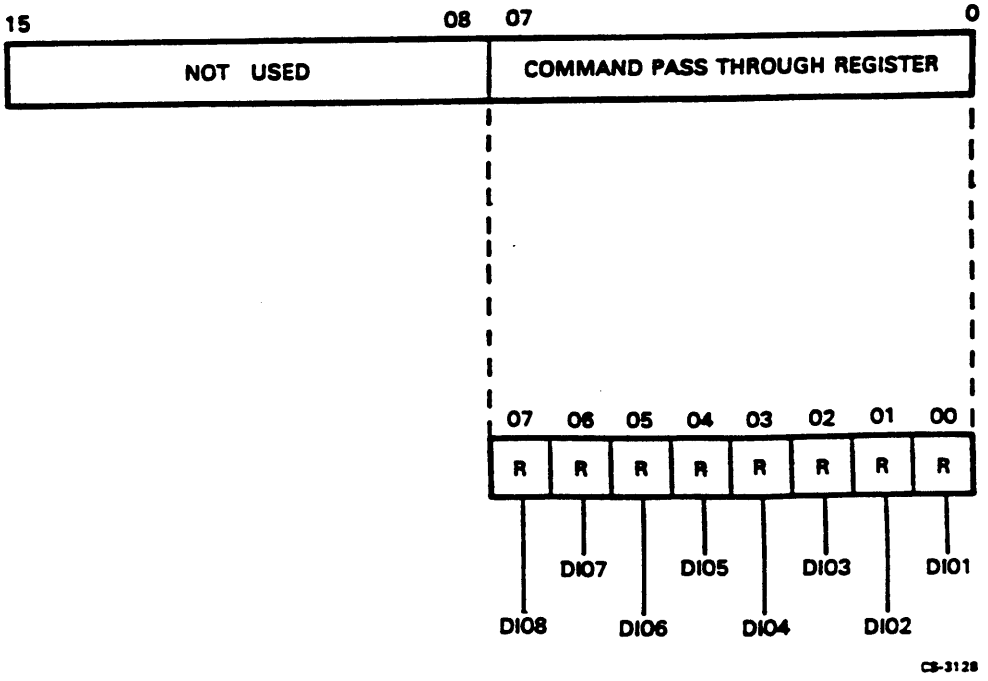


Figure 3-6 IEEE Command Register (Read Only)

3.2.4.1 Data Out Register -- Figure 3-7 shows the bit format for the Data Out Register.

The Data Out Register is used by a controller or talker for sending interface messages and device dependent messages. When the TMS 9914A register enters the Talker Active State (TACS) or the Controller Active State (CACS), the contents of the Data Out Register are presented to the IEC/IEEE data lines (DIO(8-1)), and the byte is set over the bus under the control of the Source Handshake. Each time a byte is written, the source handshake is bottom enabled, and the byte is sent. If the handshake is interrupted before the byte can be sent, then it will be sent the next time the Source Handshake becomes active unless a new byte available false (nbaf) auxiliary command is written. This has the effect of clearing an unsent byte from the Data Out Register, and although the register itself is not cleared, the TMS 9914A register behaves as if it had not been loaded.

Each time the source handshake becomes active and there is no unsent byte in the Data Out Register, a BO interrupt will occur, informing the host MPU that the Data Out Register is available for use.

The Data In Register and Data Out Register operate independently. The Data Out Register is not double buffered, and its contents are output directly to the data lines of the IEC/IEEE.

3.2.4.2 Parallel Poll Register -- Figure 3-7 shows the bit format for the Parallel Poll Register.

When a controller initiates a parallel poll, the contents of this register are presented to the IEC/IEEE data lines. If all bits of the register are cleared, then none of the lines DIO(8-1) will be pulled low during a parallel poll which corresponds to the Parallel Poll Idle State (PPIS) of IEEE-488. If it is desired to participate in a parallel poll, then the bit corresponding to the desired parallel poll response is set to a 1.

The Parallel Poll Register is fully double buffered. If it is written to during a parallel poll, the new value is held until the parallel poll ends, at which point the register is updated. This permits the host MPU to update the parallel poll response completely asynchronously to the IEC/IEEE.

If this register is cleared by the hardware RESET pin but not by 'swrst', it may be loaded while the chip is being configured with 'swrst' set.

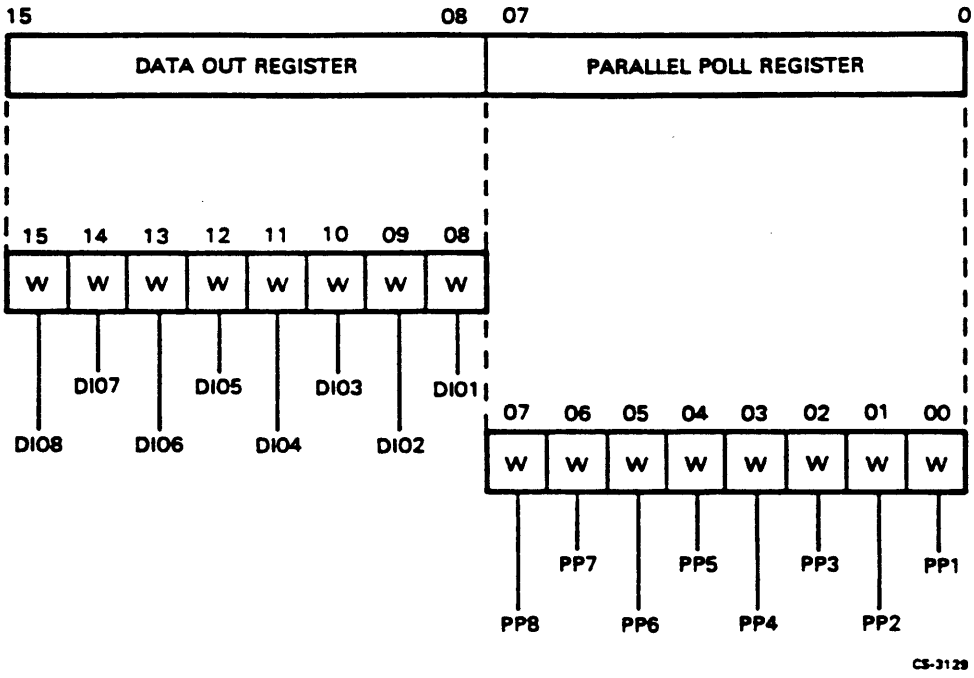


Figure 3-7 IEEE Data Register (Write Only)

3.2.4.3 Data In Register -- Figure 3-8 shows the bit format for the Data In Register.

This register is used to hold data received by the TMS 9914A register when it is a listener. It is loaded during Accept Data State (ACDS1) and, following this, an RFD holdoff will occur. This will normally be released when the byte is read by the host MPU, but if the Holdoff On All Data (hdfa) feature is selected, this holdoff must be released by the 'rhdf' auxiliary command.

If the Holdoff On End (HDFE) feature is selected, the RFD holdoff will be released by reading the Data In Register. But if the EOI line is true when the byte is received, reading the data byte will not release the holdoff and rhdf must be used.

As the Data In Register is loaded, the BI interrupt is set. The END interrupt is set simultaneously if the byte is accompanied by a true EOI line.

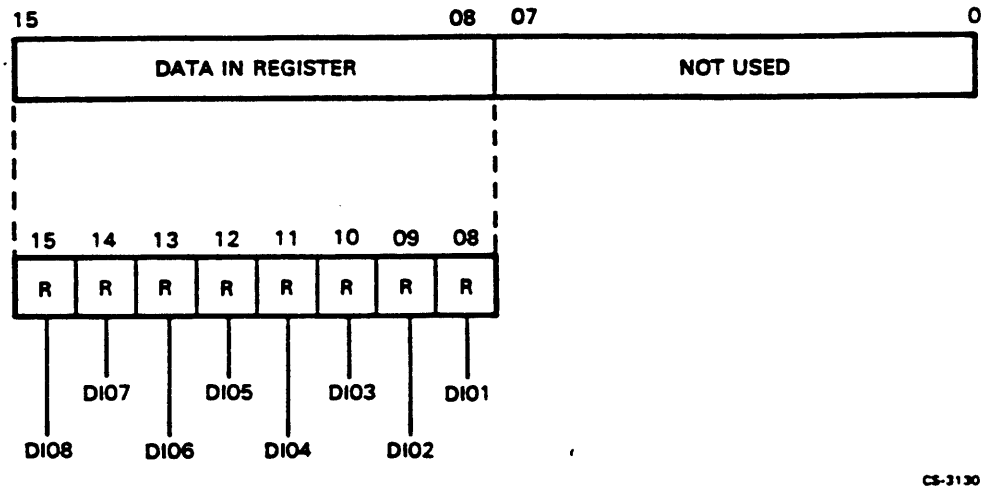


Figure 3-8 IEEE Data Register (Read Only)

3.2.5 Control and Status Register (CSR)

The control and status register enables interrupt logic and also controls data transfers, status conditions, and error conditions. It can be read and written at the assigned address. The CSR is both byte and word loadable.

Figure 3-9 shows the CSR bit format, while Table 3-11 defines the bits for the CSR.

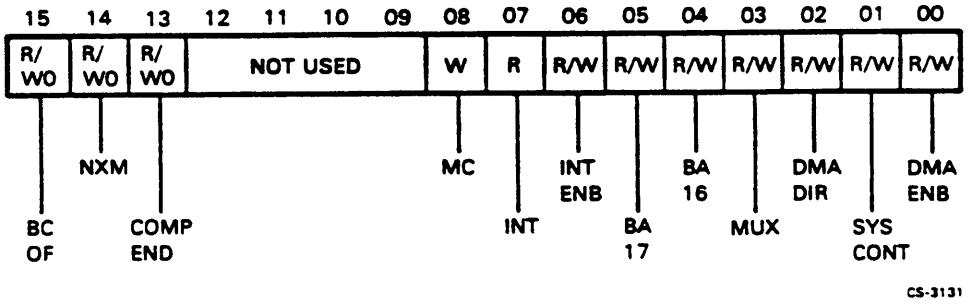


Figure 3-9A Control and Status Register (IEU11-A only)

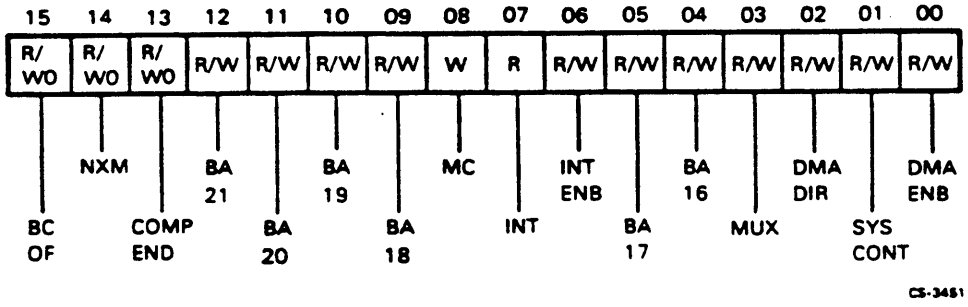


Figure 3-9B Control and Status Register (IEQ11-A Only)

Table 3-11 Control and Status Register Bit Format

Bit	Name (Mnemonic)	Function (When Set)	Cleared By
15	Byte Count Overflow (BC OF)	Indicates that the specified number of device dependent data bytes have been received or transmitted by the controller. The setting of this bit causes the ENB DMA bit to become false, which terminates the DMA data transfer. An interrupt is also generated, if the INT ENB bit (CSR Bit<6>) is set.	INIT, MC, or loading with "0"
14	Non-existent Memory (NXM)	Indicates that the controller is performing a DMA transfer and the memory address/specified in the BAR register is non-existent (does not respond to MSYN within 10 microseconds). The setting of this bit causes the ENB DMA bit to become false. An interrupt is also generated, if the INT ENB bit (CSR Bit <6>) is set.	INIT, MC, or loading
13	Comparison End (COMP END)	Indicates that a predefined number of successive EOS characters has been detected by the MCR register. To activate this comparison logic, the ENB Match bit (MCR Bit<15>) must be set. The setting of this bit causes the DMA ENB bit (CSR Bit<0>) to become false. An interrupt is also generated, if the INT ENB bit (CSR Bit<6>) is set.	INIT, MC, or loading with "0"
<12:09>		BA <21:18> used for the IEQ11-A only.	

Table 3-11 Control and Status Register Bit Format (Cont)

NOTE

The extended bus address bits can be loaded only by word instructions because the upper four extended bus address bits 18 to 21, which are resident in the high byte of the CSR, cannot be loaded byte-wise. Extended address bits are not used with the IEU11-A.

Bit	Name (Mnemonic)	Function (When Set)	Cleared By
8	Master Clear (MC)	Loading with "1" generates a reset pulse with the same effect for bits of the CSR and MCR registers as the INIT signal. Therefore, this bit allows selective resetting of the IEU11-A without affecting devices on the UNIBUS.	
7	Interrupt (INT)	Represents the logical NOR condition of the INT Ø + INT 1 bit (IIR Bits<7:6>). The setting of this bit causes the DMA ENB bit (CSR Bit<Ø>) to become false. An interrupt is also generated, if the INT ENB bit (CSR Bit <6>) is set.	INIT, software reset command (ACR) or reading the IIR
6	Interrupt Enable (INT ENB)	Enables the bits BC OF, NXM, COMP END, or INT to generate an interrupt request to the CPU. The assertion of the INT DONE signal is automatically generated by the hardware after each interrupt sequence. Therefore, it has to be set again to allow further interrupts.	INIT, MC or assertion of INT DONE signal

Table 3-11 Control and Status Register Bit Format (Cont)

Bit	Name (Mnemonic)	Function (When Set)	Cleared By
<5:4>	Bus Address <17:16> (BA <17:16>)	In conjunction with BAR bits <5:4> specify the starting memory address of a DMA transfer. These bits are incremented when BAR overflows.	
3	Multiplex (MUX)	Identifies which set of registers is active. When this bit is clear, it indicates that register set 1 is being used, whereas register set 2 is selected when it is set. Since this bit can be activated by both CSRs, CSR 1 must set the MUX bit to select register set 2. Clearing this bit by CSR 2 will select registr set 1. By changing the MUX bit, the CSR which is presently addressed, is activated. Both CSRs can read the state of the MUX bit.	
2	DMA Direction (DMA DIR)	Defines the data path during DMA transfers. It causes the IEU11 A to perform a DATI cycle (data from memory to IDR). The IEU11 A performs a DATOB cycle (data from IDR to memory) when this bit is cleared.	INIT, MC
1	System Control (SYS CONT)	Gives the IEU11 A the capabilities of a system controller. That is the IEU11-A is able to send the IFC and REN message by means of the IEC/IEEE bus, otherwise the appropriate bus transceivers are not enabled.	INIT MC

Table 3-11 Control and Status Register Bit Format (Cont)

Bit	Name (Mnemonic)	Function (When Set)	Cleared By
Ø	DMA Enable (DMA ENB)	Enables a DMA block transfer determined by the bus address in the BAR and the block length in the BCR. Clearing this bit terminates the DMA transfer, because this disables further DMA requests. Setting this bit again is only possible after canceling all the conditions used to reset the DMA ENB bit (CSR Bit<Ø>).	INIT, MC, BC OF, NXM, COMP END, or INIT

3.2.6 Bus Address Register (BAR)

The Bus Address Register points to the current data byte that is to be accessed during a DMA block transfer. The BAR can be read and written at the assigned UNIBUS address. It is byte and word loadable. The BAR is incremented by +1 after each DMA transfer of a data byte to or from memory.

The BAR is loaded prior to setting the DMA ENB bit (CSR Bit<Ø>). Along with BA <17:16> (CSR Bits<5:4>), the BAR contents specifies the starting memory address of a DMA transfer. Refer to Figure 3-1Ø for the bit format of the BAR.

The BAR can only be cleared by writing "Øs" to it.

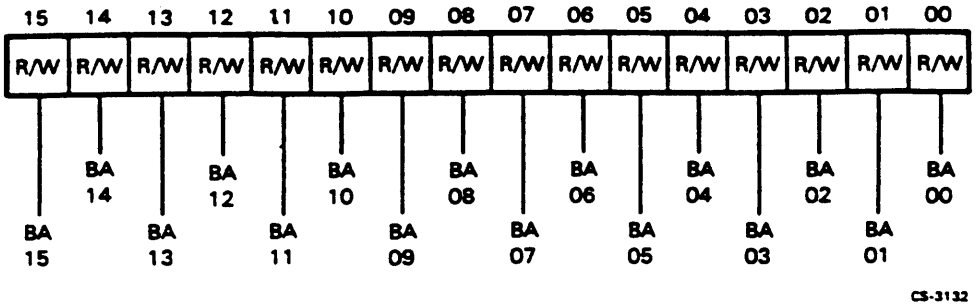


Figure 3-1Ø Bus Address Register

3.2.7 Byte Count Register

The byte count register (BCR) defines the length of the data block that is to be transferred in the DMA mode. Refer to Figure 3-11 for the bit format. The BAR can be read and written at the assigned UNIBUS address. It is both byte and word loadable.

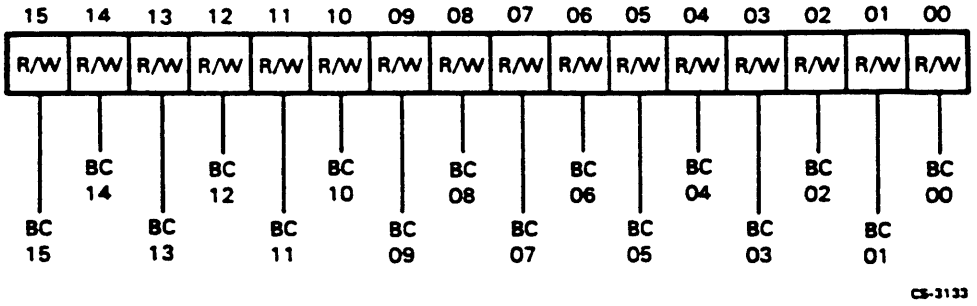


Figure 3-11 Byte Count Register

The BCR must be loaded initially by the 2's complement of the number of transfers to be made before setting the DMA ENB bit (CSR Bit<Ø>). The register's contents is incremented by +1 every time a DMA cycle is performed. When the register's contents equal zero, the BC OF bit is set to terminate the DMA transfer. However, the DMA transfer can be terminated sooner by resetting the DMA ENB bit (CSR Bit<Ø>). In this case, the BCR contains a remainder that can be used to calculate the real block length that has been transferred.

The BCR can only be cleared by writing "Øs" to it.

3.2.8 Match Character Register

The Match Character Register (MCR) provides the possibility to detect EOS characters while the IEU11-A is in the Listener Active State (LACS) and data is being transferred by means of a DMA. The MCR can be read and written at the assigned UNIBUS address. It is both byte and word loadable.

Figure 3-12 shows the bit format for the MCR, while Table 3-12 defines the bits.

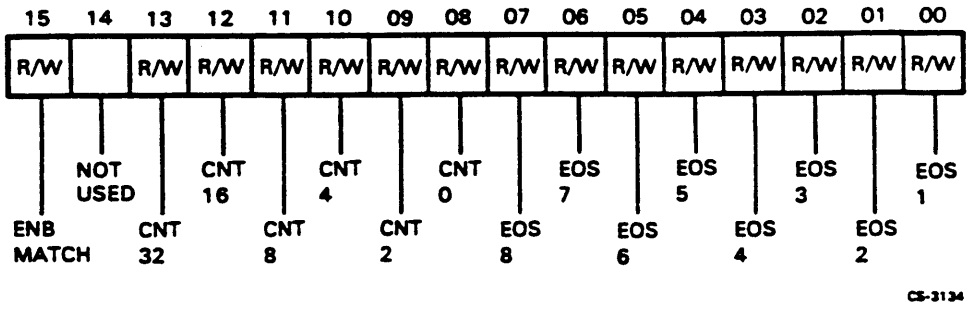


Figure 3-12 Match Character Register

Table 3-12 Match Character Register Bit Descriptions

Bit	Name (Mnemonic)	Function (When Set)	Cleared By
15	Enable Match Detection	Enables comparison logic to assert the COMP END bit (CSR Bit<13>) if a predefined number of consecutive characters equal to the low order byte of this register has been detected. The desired number of EOS characters may be defined by loading the MCR bits <13:Ø8> with the appropriate value.	
<13:Ø8>	Counter (CNT 32, 16, 8, 4, 2, Ø)	Can be loaded with a binary number from 1 to 63 to define how many consecutive EOS characters must be detected by the Listener before the COMP END bit (CSR Bit <13>) is asserted. Loading with zero is not allowed.	INIT or MC
<Ø7:ØØ>	End of String (EOS <8:Ø>)	Can be loaded with a character equal to EOS character used on the IEC/IEEE bus to detect end of string. The EOS character depends on the device that is currently the Talker and is freely selectable.	INIT or MC

3.3 STATE DIAGRAM IMPLEMENTATION

This section contains the state diagrams for the TMS 9914A.

Where equivalent, the names of TMS 9914A states are the same as those of IEEE-488. In some cases, IEEE-488 states have been divided, for example, ACDS of the IEEE-488 has been split into ACDS1 and ACDS2. The convention of lower case characters for local messages and upper case for remote messages and interface states is retained.

State diagrams with remote message outputs are supplemented with tables. T is used to represent a true output and F a false output. Parentheses denote a passive output; otherwise, it is active. The outputs shown are the values presented to the bus and

assume the use of the SN75160 and SN75161 or SN75162 transceivers or their logical equivalents. The symbol (NUL) associated with DIO(1-8) indicates that each of these lines is sent passive false by the function in question.

NOTE

An arrow into a state with no state as its origin represents a transition from every other state on the diagram. Note, however, that this does not imply that all exit conditions from the destination state are overridden. If such an entry condition is true and, simultaneously, an exit condition is true, then this represents an illegal situation and should be avoided. Such situations will not occur in normal operation of the device.

No maximum timings are discussed. The TMS 9914A register, with its recommended transceivers, meets all IEEE-488 maximum timing requirements. If the TMS 9914A register is used with other transceivers, then it must be ensured that these requirements are still met.

3.3.1 Auxiliary Commands

There are two basic types of commands implemented in the auxiliary command register: immediate execute and clear/set.

The clear/set commands are used to enable and disable the various features of the TMS 9914A register. The particular feature is selected by the code on f0-f4 and it is set or cleared according to the value on the cs bit. For the purposes of the state diagrams, the mnemonic of a clear/set command simply represents its current state.

The immediate execute auxiliary commands remain active for the duration of a strobe signal after the auxiliary command register has been written to. This is represented in the form of a state diagram in Figure 3-13. Note that writes to the auxiliary command register must be spaced by at least five clock cycles. For the purposes of the remaining state diagrams, the immediate execute commands are represented as the mnemonic gated by the auxiliary command strobe state (AXSS).

The clear/set bit of the auxiliary command register is used by several of the immediate execute commands, for example; 'dacr' uses it to differentiate between valid and not valid secondary addresses when releasing a DAC holdoff on a secondary address. The 'lon' and 'ton' auxiliary commands are also considered immediate execute, as described in Section 3.3.4.

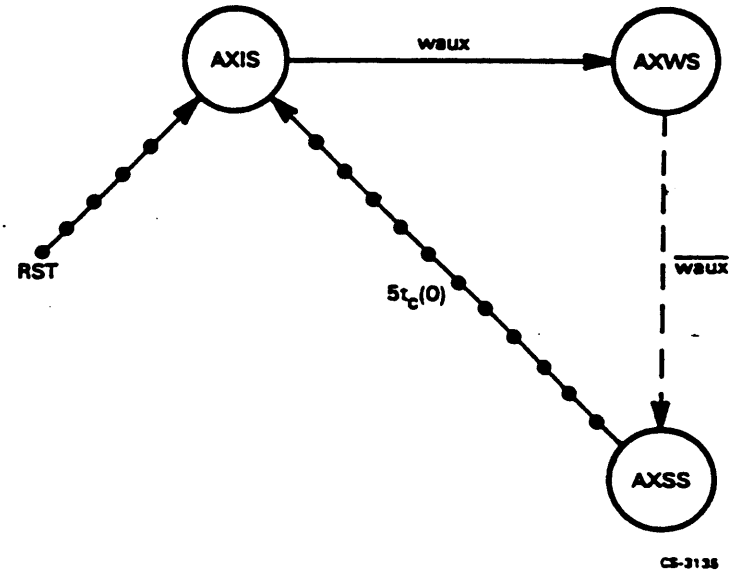


Figure 3-13 TMS 9914A Auxiliary Command State Diagram

The 'fget' and 'rtl' auxiliary commands are both immediate execute and clear/set. They may be cleared or set in the normal way, but if they are cleared when they are already in the false state, they will pulse true for the duration of AXSS. In the following state diagrams, however, these are simply included in their clear/set form.

Table 3-13 Auxiliary Command State Diagram Mnemonics

Mnemonics	Messages	Mnemonics	States
waux	- write to auxiliary command register	AXIS	- auxiliary command register idle state
$t_{c(0)}$	- clock cycle time	AXWS	- auxiliary command write state
		AXSS	- auxiliary command strobe state

3.3.2 Acceptor Handshake

The TMS 9914A acceptor handshake is shown in Figure 3-14. The main variation from IEEE-488 to note is that the device remains in AIDS while the controller function is in CACS. The TMS 9914A register, therefore, does not monitor the commands that it sends over the bus, and this places some restrictions on the user which are outlined in Section 3.7.

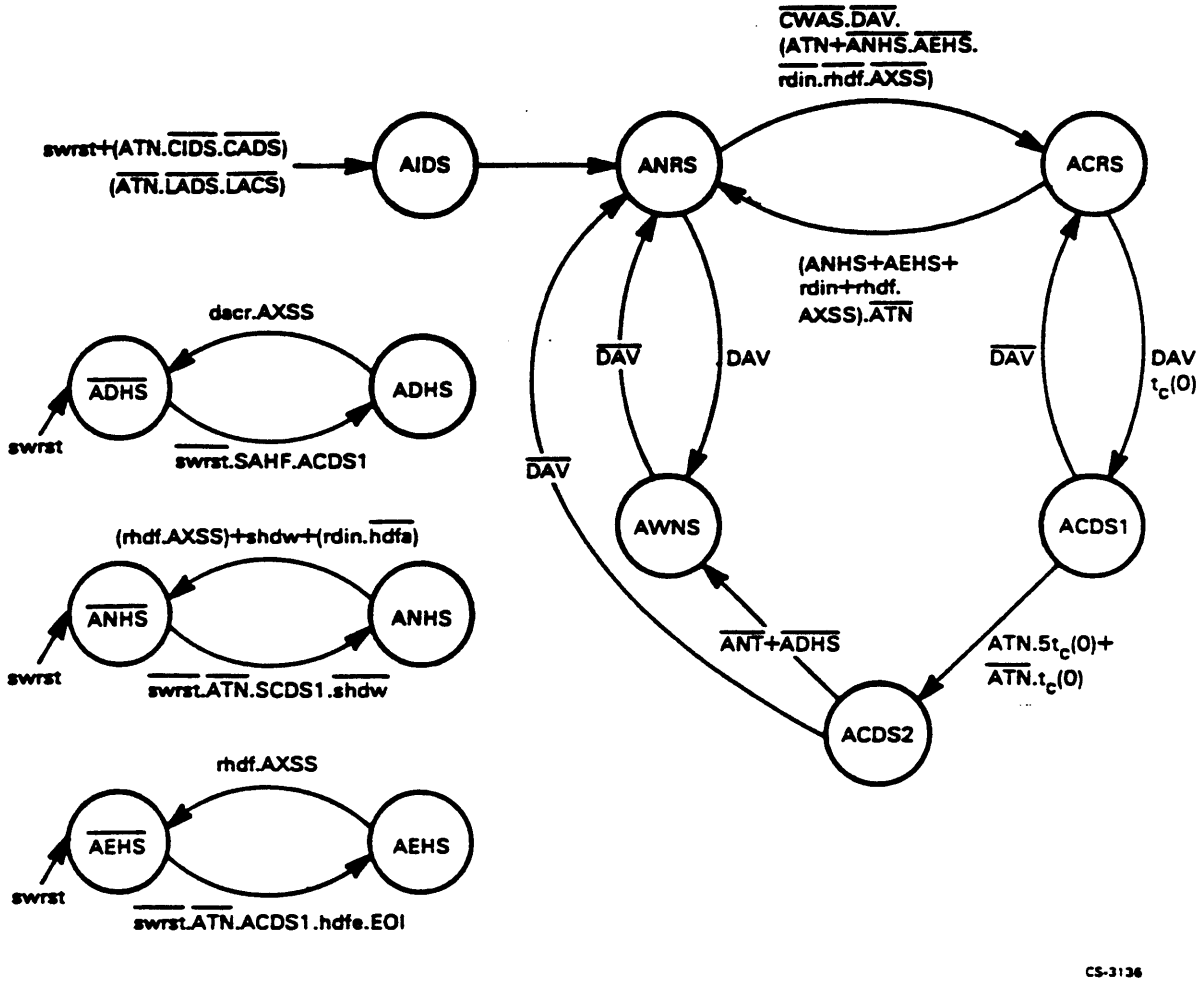


Figure 3-14 TMS 9914A Acceptor Handshake State Diagram

The accept data state of IEEE-488 (ACDS) is divided into two states. The first (ACDS1) is used to strobe data into the Data In Register, or to sequence the decoding of commands from the bus. All interrupts generated by the acceptor handshake (GET, MA, MAC, DCAS, APT, UCG, BI, and END) are generated by this state. The second (ACDS2) is used as a holding state where the device will remain in the event of a DAC holdoff.

Certain commands will cause interrupts in ACDS1 and, if the interrupts are unmasked, a DAC holdoff will occur. The interrupts concerned are GET, MA, DCAS, UCG, and APT. This is represented in the state diagram by the signal SAHF which becomes true when one of the above interrupts is set if it is unmasked. It persists for the duration of ACDS1. This event is stored by causing ADHS to become active, which inhibits the transition from ACDS2 to AWNS. ADHS is cleared by 'dacr'. Table 3-27 shows the response of the TMS 9914A register to the various bus commands.

Two additional state diagrams are included to record the type of data received in ACDS1 when ATN is false. ANHS indicates that a data byte has been received and that an RFD holdoff should be caused before the next data byte is accepted. The holdoff may be released by reading the Data In Register unless the 'hdfa' feature is enabled in which case 'rhdf' must be used. AEHS shows that the last data byte was accepted with the EOI message true and the 'hdfe' feature set. This will cause an RFD holdoff which can only be released by 'rhdf'.

Table 3-14 Acceptor Handshake Mnemonics

Mnemonics	Messages	Mnemonics	States
swrst	= software reset	AIDS	= acceptor idle state
dacr	= DAC release	ANRS	= acceptor not ready state
rhdf	= release RFD holdoff	ACRS	= acceptor ready state
shdw	= shadow handshake	ACDS1	= accept data state 1
rdin	= read data in register	ACDS2	= accept data state 2
hdfe	= enable RFD holdoff after END messages received	AWNS	= acceptor wait for new cycle state
hdfa	= enable RFD holdoff on all data	ADHS	= accept data holdoff state
ATN	= attention	ANHS	= acceptor not ready holdoff state
DAV	= data valid	AEHS	= acceptor not ready holdoff after 'END'
EOI	= end or identify state	CWAS	= controller wait for ANRS state (controller function)
RFD	= ready for data	AXSS	= auxiliary command strobe state (auxiliary command register)
DAC	= data accepted	LADS	= listener addressed state (listener function)
SAHF	= set accept data holdoff state	LACS	= listener active state (listener function)

Table 3-14 Acceptor Handshake Mnemonics (Cont)

Mnemonics	Messages	Mnemonics	States
$t_{c(\emptyset)}$	- clock cycle time	CIDS	- controller idle state (controller function)
		CADS	- controller addressed state (controller function)

Table 3-15 Acceptor Handshake Message Outputs

State	Remote Messages Sent RFD	DAC	Other Actions
AIDS	(T)	(T)	
ANRS	F	F	
ACRS	(T)	F	
ACDS1	F	F	ATN False: - data entered into Data In Register - BI interrupt generated - end interrupt generated if EOI is true ATN True: - commands decoded - command related interrupts set - sahf set if command requires a DAC holdoff - TR pin set true if GET message is received - pts feature cleared after UNC interrupt set
ACDS2	F	F	TR - pin set true if GET command was received in ACDS1
AWNS	F	(T)	

3.3.3 Source Handshake

The TMS 9914A source handshake state diagram is shown in Figure 3-15. IEEE-488 states SIWS and SWNS have been removed. These record the false then true transition of 'nba' (new byte available) as the old data byte is removed and a new data byte is made ready. Instead, the TMS 9914A register uses as a separate state

(SHFS) to record the availability of a data byte in the Data Out Register. This state is exited when a byte is written to the Data Out Register which enables the transition from SGNS to SDYS and the subsequent transmission of the byte. The SHFS is re-entered as the byte is sent in STRS, but if the handshake is interrupted before this, then the fact that the byte has not been sent is recorded until the source handshake again becomes active. If, however, the byte in the Data Out Register is to be disregarded, then 'nbaf' may be used to return the device to SHFS.

The status byte in the Serial Poll Register is continually available. The transition from SGNS to SDYS is not dependent on SHFS during a serial poll; that is, while SPAS is active. By separately recording the availability of a byte in the Data Out Register, a talker sending data may be interrupted for a serial poll without risk of a byte being lost.

The additional state SERS is included to detect an error condition on the bus. This will be entered when the source handshake tries to send a byte but finds both the NRFD and NDAC lines false at the same time. This condition will normally indicate for a controller that there are no devices powered up on the bus, or for a talker that there are no devices addressed to listen on the bus.

The state VSTS will be entered after the first data byte of a talker has been sent if the 'vstd1' feature is enabled. This enables a very short bus settling time ($4t_{c(g)}$) for all subsequent bytes until ATN next becomes true. The TMS 9914A register will not use the short bus settling time when it is an active controller.

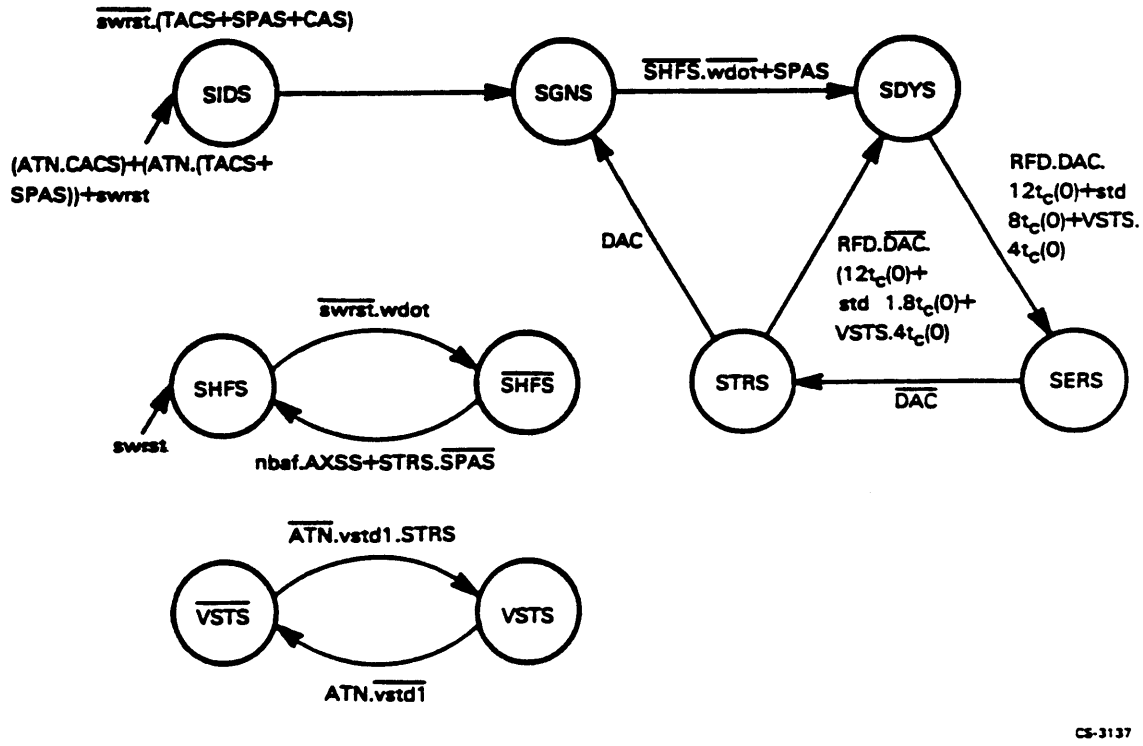


Figure 3-15 TMS 9914A Source Handshake State Diagram

Table 3-16 Source Handshake Mnemonics

Mnemonics		Messages	Mnemonics		States
swrst	=	software reset	SIDS	=	source idle state
nbaf	=	new byte available false	SGNS	=	source generate state
wdot	=	write to the data out register	SDYS	=	source delay state
stdl	=	enable short bus setting time	SERS	=	source error state
vstdl	=	enable very short bus setting time	STRS	=	source transfer state
ATN	=	attention	SHFS	=	source holdoff state
RFD	=	ready for data	VSTS	=	very short bus settling time state

Table 3-16 Source Handshake Mnemonics (Cont)

Mnemonics		Messages	Mnemonics		States
DAC	=	data accepted	TACS	=	talker active state (talker function)
$t_{c(\emptyset)}$	=	clock cycle time	CACS	=	controller active state (controller function)
			SPAS	=	serial poll active state (talker function)
			AXSS	=	auxiliary command strobe state (auxiliary command register)

Table 3-17 Source Handshake Message Outputs

State	Remote Messages Sent DAV	Other Actions
SIDS	(F)	BO interrupt and ACCRQ set true if
SGNS	F	SHFS is false and SPAS is not true
SDYS	F	
SERS	F	ERR interrupt set true
STRS	T	

3.3.4 Talker and Listener Functions

Figures 3-16 and 3-17 show the TMS 9914A listener and talker state diagrams, which serve the purpose of the listener and talker or extended listener and extended talker functions of IEEE-488, depending on the state of the APT interrupt mask bit.

The TMS 9914A register does not recognize secondary addresses on-chip and these must be passed through to the host MPU for verification. Secondary addressing is enabled by unmasking the APT interrupt. A secondary address will cause this interrupt if the last primary command received was a primary address of the device; that is, it is in TPAS or LPAS. A DAC holdoff will also occur. The host MPU must respond to the interrupt by reading the secondary from the Command Pass Through Register and identifying it as being valid or invalid. The holdoff may then be released with a 'dacr' auxiliary command, the sense of the 'cs' bit being used to indicate a valid (cs=1) or invalid (cs=Ø) secondary. If a valid secondary address is indicated, then the TMS 9914A register will enter TADS or LADS depending on whether it is in TPAS or LPAS.

The 'lon' and 'ton' auxiliary commands together with the clear/set bit (cs) have a direct influence on the appropriate state diagrams. Therefore, although they appear as ordinary clear/set auxiliary commands, they can be effectively cleared by other bus events. For example, if a TMS 9914A register addresses itself as a listener by means of the 'lon' command, it may be returned to LIDS by a UNL command from the bus at a later time.

The 'lon' and 'ton' auxiliary commands are used to implement two features of IEEE-488. First, talk only and listen only are used in situations where there is no active controller on the bus. Note that the 'lon' and 'ton' commands are linked with these features to indicate to the user that these commands are not enabled by CAS as are 'ltn' and 'lun' of IEEE-488.

Second, the 'lon' and 'ton' auxiliary commands are used by an active controller to address itself. IEEE-488 provides for a controller to address itself to listen by means of the 'ltn' and 'lun' message, but there is no corresponding message for the talker. Therefore, when a controller addresses itself to talk through 'ton', it must send its talk address over the bus and, similarly, if it sends another talk address over the bus, then it must unaddress itself by writing 'ton' false.

When the TMS 9914A register enters SPAS, the contents of the serial poll register are sampled and presented on DIO(8-1). These will remain unchanged until SPAS is exited. The source handshake will, however, send this status byte as many times as the controller will accept it.

The internal IFC signal of the TMS 9914A register (IFCIN) is suppressed when the device itself is sending IFC in order to simplify implementation of the controller function (see Section 3.7.3). Therefore, the send interface clear (sic) auxiliary command is included with IFCIN to return the talker and listener functions to their idle states and allow a system controller to clear its own interface.

A separate diagram is included to control the sending of the END message of IEEE-488. If the 'feoi' auxiliary command is written followed by loading a byte into the Data Out Register, the TMS 9914A register will enter ERAS, and the EOI line will be asserted as 'DIO(8-1)' and will begin to change. The function will enter ENAS as soon as the source handshake begins to send this byte, and EOI will be released when the Data Out Register is next loaded. If it is desired to send EOI true with the next byte as well, then 'feoi' may be written before the Data Out Register returns the device to ERAS.

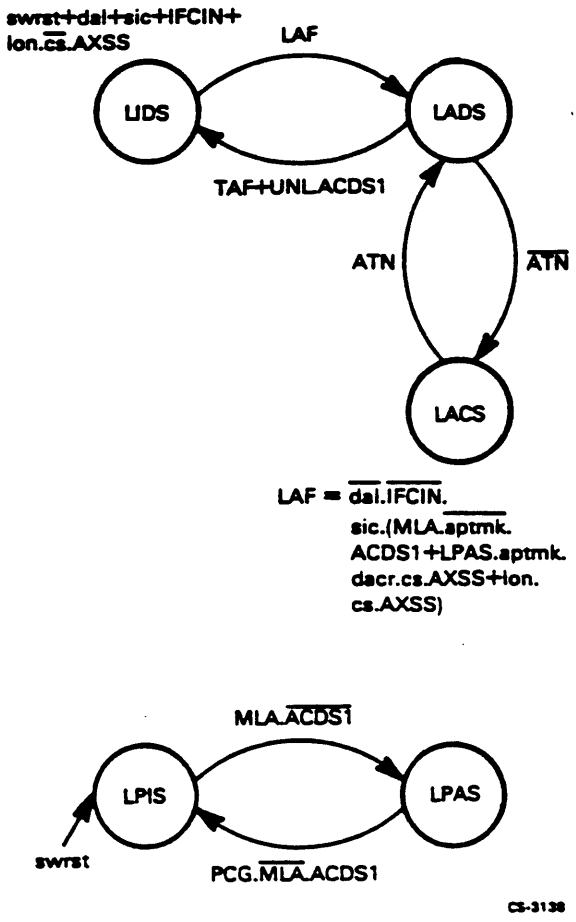


Figure 3-16 TMS 9914A Listener State Diagram

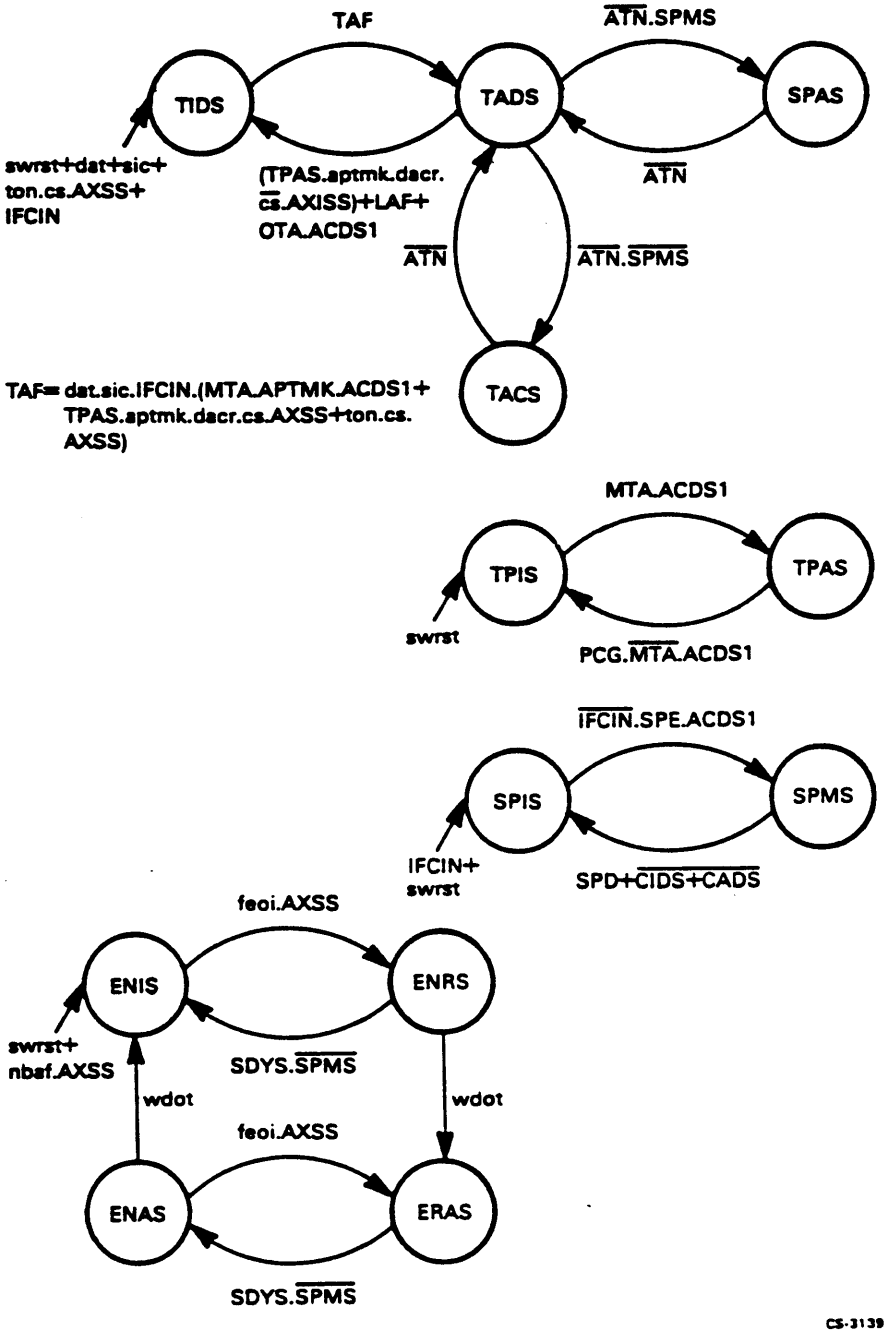


Figure 3-17 TMS 9914A Talker State Diagram

Table 3-18 Talker and Listener Mnemonics

Mnemonics	Messages	Mnemonics	States
swrst	= software reset	LIDS	= listener idle state
dal	= disable listener	LADS	= listener addressed state
dat	= disable talker	LACS	= listener active state
sic	= send interface clear	LPIS	= listener primary idle state
lon	= listen only	LPAS	= listener primary addressed state
ton	= talk only	TIDS	= talker idle state
cs	= clear/set bit of the auxiliary command register	TADS	= talker addressed state
dacr	= release 'DAC' holdoff	TACS	= talker active state
aptmk	= address pass through interrupt mask	SPAS	= serial poll active state
nbaf	= new byte available false	SPIS	= serial poll idle state
feoi	= force 'EOI'	SPMS	= serial poll mode state
wdot	= write to the Data Out Register	TPIS	= talker primary idle state
ATN	= attention	TPAS	= talker primary addressed state
IFCIN	= internal interface clear message (a debounced signal, suppressed by 'sic')	ENIS	= end idle state
EOI	= end or identify	ENRS	= end ready state
PCG	= primary command group	ERAS	= end ready and active state
MLA	= my listen address	ENAS	= end active state
MTA	= my talk address	SDYS	= source delay state (source handshake)

Table 3-18 Talker and Listener Mnemonics (Cont)

Mnemonics	Messages	Mnemonics	States
OTA	= other talk address	CIDS	= controller idle state (controller function)
SPE	= serial poll enable	CADS	= controller addressed state (controller function)
SPD	= serial poll disable	ACDS1	= accept data state 1 (acceptor handshake)
UNL	= unlisten	AXSS	= auxiliary command strobe state (auxiliary command register)
PCG	= primary command group		

Table 3-19 Talker Function Message Outputs

State	Qualifier	Remote Messages Sent RQS	EOI	Other Actions DIO(8-1)
TIDS		(F)	(F)	(NUL)
TADS		(F)	(F)	(NUL)
TACS	ENIS.ENRS	(F)	F	DATA OUT REG
TACS	ENAS.ERAS	(F)	T	DATA OUT REG
SPAS	NPRS.SRQS	F	F	SERIAL POLL REG
SPAS	APRS1.APRS2	T	F	SERIAL POLL REG

3.4 SERVICE REQUEST FUNCTION

Figure 3-18 shows the state diagram for the TMS 9914A service request function. The device has two means of implementing the request service (rsv) local message of IEEE-488: the first, 'rsv1', is bit 7 of the Serial Poll Register; the second is the auxiliary command 'rsv2'. These are simply ORed together to provide an input to the service request function and, in any particular application, only one would normally be used, the other being left in its hardware reset state.

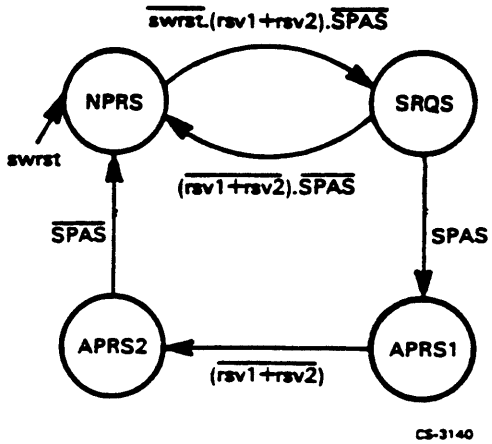


Figure 3-18 Service Request State Diagram

The affirmative poll response state (APRS) of IEEE-488 is split into two states on the TMS 9914A register for the following reason: consider the case where a device has requested service, has been serial polled, and then wishes to request service again. The host MPU must clear the 'rsv' message and then set it true again. Suppose this temporary false condition happens within one occurrence of SPAS. If the service request function has been implemented exactly as per IEEE-488, it will not be recognized, and SRQ will not be asserted a second time. Therefore, 'rsv' may only be cleared when the device is known not to be in SPAS, which can only happen if it is cleared as a consequence of some prearranged action of the controller. This action would normally be a part of the service routine executed by the controller as a response to the request for service. For example, if service was requested by an instrument which had some data to send for processing or to a printing device, then 'rsv' could be cleared when it is addressed to talk and send its data over the bus.

For many applications, the fact that the device has been serial polled after requesting service is considered sufficient response from the controller. The 'rsv' local message, therefore, simply becomes a request for the controller to read its serial poll status byte. It is then desirable to be able to clear and reassert 'rsv' at any time after the serial poll status byte has been polled and the SPAS interrupt set. The TMS 9914A register is able to record a false transition of 'rsv1' or 'rsv2' by moving from APRS1 to APRS2 even if the device is in SPAS. This makes the above approach to serial polling possible.

To further support this approach, the 'rsv2' auxiliary command is automatically cleared when the serial poll status byte is polled, ensuring that 'rsv2' is cleared before a second serial poll can occur. If this were not the case, the same status byte might be polled twice by the controller with the RQS bit true, which may indicate that two reasons for requiring service have arisen.

The TMS 9914A register will only send one serial poll status byte during each active period of SPAS. However, it will send this status byte as many times as the controller is prepared to accept it. Therefore, the controller should only read the status byte once per serial poll; otherwise, each time a status byte is sent with the RQS message true, the SPAS interrupt will be generated and 'rsv2' will be cleared.

Table 3-20 Service Request Mnemonics

Mnemonics	Messages	Mnemonics	States
swrst	= software reset	NPRS	= negative poll response state
rsv1	= request service 1 (bit 7 of serial poll register)	SRQS	= service request state
rsv2	= request service 2 (auxiliary command register)	APRS1	= affirmative poll state 1
		APRS2	= affirmative poll state 2
		SPAS	= serial poll active state (talker function)

Table 3-21 Service Request Message Outputs

State	Remote Messages Sent SRQ	Other Actions
NPRS	(F)	
SRQS	T	
APRS1	(F)	- rsv2 cleared if in SPAS and STRS
		- SPAS interrupt set if in SPAS when STRS is exited
APRS2	(F)	- same as APRS1

3.5 REMOTE/LOCAL FUNCTION

The TMS 9914A remote local state diagram is shown in Figure 3-19. It differs little from that of IEEE-488.

The complete listener function (LAF) is used to effect the transition from LOCS to REMS or from LWLS to RWLS. This means that if the APT interrupt is masked, the device will enter one of the remote states in response to its listen address, but if secondary addressing is enabled, this will not happen until 'dacr' is written with 'cs' true in response to a valid secondary address. In addition, the transition to one of the remote states will occur if 'lon' is used to address the device to listen.

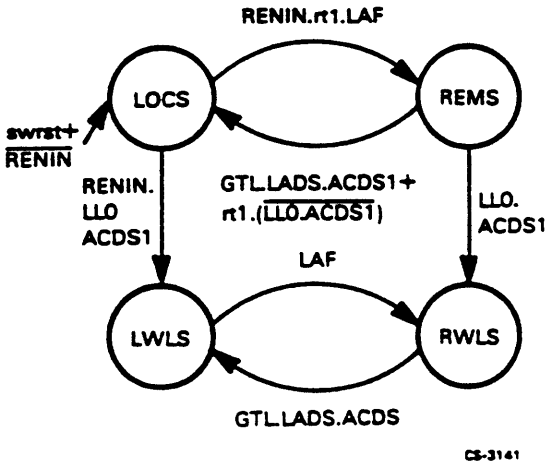


Figure 3-19 TMS 9914A Remote Local State Diagram

Table 3-22 Remote/Local Mnemonics

Mnemonics	Messages	Mnemonics	States
swrst	= software reset	LOCS	= local state
rtl	= return to local	REMS	= remote state
RENIN	= internal remote enable message (debounced)	RWLS	= remote with lockout state
GTL	= go to local	LWLS	= local with lockout state
LLO	= local lockout	LADS	= listener addressed state (listener function)
		ACDS1	= accept data state 1 (acceptor handshake)

3.6 PARALLEL POLL FUNCTION

The parallel poll function of the TMS 9914A register only nominally supports logically-configured parallel poll. With a suitable software package, remotely-configured parallel poll may also be easily implemented. The state diagram is shown in Figure 3-20.

When the EOI and ATN lines become true simultaneously (the Identify message), the contents of the Parallel Poll Register are output to DIO(8-1). If parallel poll is to be used in a particular bus environment, then the Pull-Up Enable (PE) input of the SN75160 must be held low so that the DIO(8-1) are driven by open collector buffers. Parallel Poll, occurring when the Parallel Poll Register is in the hardware reset condition of all zeros, will result in none of DIO(8-1) being pulled low. This corresponds to the Parallel Poll Idle State (PPIS). If it is desired to participate in a parallel poll, then the bit corresponding to the desired parallel poll response is set true. This implements the Parallel Poll Standby State (PPSS) and, when the Identify message becomes true, the appropriate line DIO(8-1) is pulled low. This is equivalent to the Parallel Poll Active State (PPAS). Only one bit of the Parallel Poll Register should be set true at once.

3.6.1 Remote Configured Parallel Poll

The Parallel Poll Configure command (PPC) is treated by the TMS 9914A register as an unrecognized addressed command. It is passed through when the TMS 9914A register is in LADS. If an instrument is to be remotely configured for parallel poll, then the pass through next secondary (pts) auxiliary command should be written before releasing the DAC holdoff. This will cause the next command received to also set a UNC interrupt if it is a secondary command. The secondary command will be either the Parallel Poll Enable command (PPE) or the Parallel Poll Disable command (PPD) and should be read from the Command Pass Through Register and identified. If it is the PPE command, then the attendant bits (S, P1, P2, P3) should be extracted and stored by the host MPU (see Section 2.9.2 of IEEE-488 1978). The S bit should then be matched against the individual status of the instrument (represented by 'ist'), and if they are the same, the bit corresponding to the parallel poll response, specified by P1, P2, P3, should be set true in the Parallel Poll Register. If this is not the case, the Parallel Poll Register should be cleared if it is not already clear. After this, each time the individual status of the device changes, the 'ist' should again be matched against the S bit and the Parallel Poll Register updated accordingly until PPD or PPU is received.

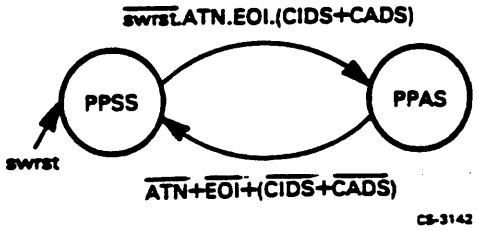


Figure 3-20 TMS 9914A Parallel Poll State Diagram

If a PPD command is passed through after the 'pts' feature has been written, the Parallel Poll Register should be cleared before the DAC holdoff is released. The PPC command that precedes PPD is an address command; it is a means of eliminating individual members of a parallel poll. The parallel unconfigure command is treated by the TMS 9914A register as an unrecognized universal command. When it is passed through, the host MPU should clear its Parallel Poll Register before releasing the DAC holdoff. This command will clear all members of a parallel poll.

Table 3-23 Parallel Poll Mnemonics

Messages		States	
swrst	= software reset	PPSS	= parallel poll standby state
ATN	= attention	PPAS	= parallel poll active state
EOI	= end or identify	CIDS	= controller idle state (controller function)
		CADS	= controller addressed state (controller function)

Table 3-24 Parallel Poll Message Outputs

State	Remote Messages Sent (DIO(8-1)	Other Actions
PPSS	(NUL)	none
PPSS	PARALLEL POLL REG*	none

* If there is a true bit in the Parallel Poll Register, it must be sent active; any false bit must be sent passive.

3.7 CONTROLLER FUNCTION

The controller function of the TMS 9914A register is greatly simplified compared with that of IEEE-488. It relies heavily on software support but, with suitable software, it enables all subsets of the controller function to be implemented. With this approach the controller logic is reduced to a small proportion of the chip area which means that the device may be economically used in situations where a talker/listener only is required.

Figure 3-21 shows the controller function state diagram. With suitable software, it will perform the full controller function as described in the IEEE-488A 1980 supplement to the IEEE-488 1978. It therefore includes the additional state CSHS, which allows time for DAV to be recognized false by all devices on the bus before ATN is asserted. The 'tcs' local message is implemented by an immediate execute auxiliary command. The state CWAS is therefore added to record the occurrence of this command until the acceptor handshake enters ANRS and the device can enter CSHS. The 'tca' auxiliary command also causes entry into CSHS although IEEE-488A 1980 allows it to move directly from CSBS to CSWS. This is done for convenience of implementation and results in the 'tca' auxiliary command taking an extra 1.6 microseconds to assert ATN.

The delay between CSWS and CAWS is slightly less than specified in IEEE-488A 1980 but the total time taken in moving form CSWS to CACS is still greater than the specified minimum.

The Controller Parallel Poll State (CPPS) is not included on the TMS 9914A register. To conduct a parallel poll, a TMS 9914A based controller must set the 'rpp' clear/set auxiliary command true when it is in CACS, moving it to CPWS which sends EOI true. The host MPU must then wait 2 microseconds before reading back the parallel poll responses by means of the Command Pass Through Register. The 'rpp' auxiliary command can then be cleared, EOI will go false, and the parallel poll is complete. The host MPU will receive a BO interrupt as soon as the TMS 9914A register reenters CACS and the source handshake becomes active.

3.7.1 Controller Self-Addressing

The acceptor handshake does not operate when the controller is active. This means that commands being sent are not monitored, and special precautions are required as a consequence of this when addressing devices and when passing control.

When the controller is active, it uses 'ton' or 'lon' to address and unaddress itself. IEEE-488 provides for the controller to locally address itself to listen, but there is no corresponding local message for the talker. The TMS 9914A register should always accompany a 'ton' auxiliary command with 'cs' true with its own talk address, or a UNT command sent over the bus. Similarly, if the TMS 9914A register sends the talk address of another device over the bus, it should ensure that it is in TIDS by writing the 'ton' auxiliary command false.

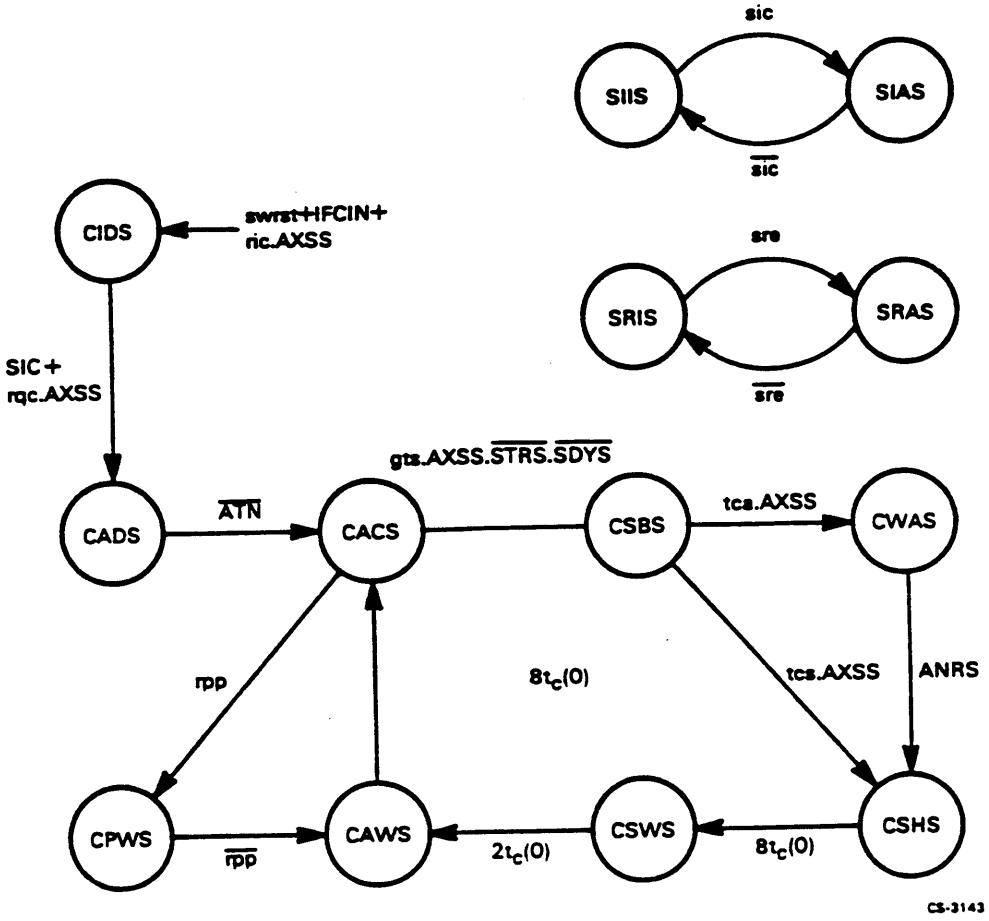


Figure 3-21 TMS 9914A Controller State Diagram

Table 3-25 Controller Function Mnemonics

Mnemonics	Messages	Mnemonics	States
swrst	= software reset	CIDS	= controller idle state
sic	= send interface clear	CADS	= controller addressed state
sre	= send remote enable	CACS	= controller active state
rqc	= request control	CSBS	= controller standby rate
rlc	= release control	CSHS	= controller standby hold state
	= go to standby	CSWS	= controller synchronous wait state
tcs	= take control synchronously	CAWS	= controller active wait state
tca	= take control asynchronously	CPWS	= controller parallel poll wait state
rpp	= request parallel poll	ANRS	= acceptor not ready state (acceptor handshake)
IFCIN	= internal interface clear message (a debounded signal which is suppressed if 'sic' is true)	SDYS	= source delay state (source handshake)
ATN	= attention	STRS	= source transfer state (source handshake)
$t_{c(0)}$	= clock cycle time	AXSS	= auxiliary command strobe state (auxiliary command register)
		LWAS	= controller wait for ANRS state

Table 3-26 Controller Function Message Outputs

State	Remote Message Sent ATN	EOI	DIO(8-1)	Other Actions
CIDS	(F)	(F)	(NUL)	
CADS	(F)	(F)	(NUL)	
CACS	T	F	DATA OUT REG	Data Out Reg. may contain any of the commands in Table 3-15
CSBS	F	(F)	(NUL)	
CWAS	F	(F)	(NUL)	
CSHS	F	(F)	(NUL)	
CSWS	T	F	(NUL)	
CAWS	T	F	(NUL)	
CPWS	T	T	(NUL)	DIO(8-1) may be read via the Command Pass Through Register

State	Remote Messages Sent IFC	Other Actions
SIIS*	(F)	Internal interface clear message IFCIN is held false
SIIS	F	
SIAS	T	

State	Remote Messages Sent REN	Other Actions
SRIS*	(F)	none
SRIS	F	none
SRAS	T	none

* Buffers not configured for a system controller; otherwise, buffers are configured for system controller.

3.7.2 Passing Control

As Figure 3-21 shows, the controller transfer state (CTRS) of IEEE-488 is not present, and all transitions associated with the TCT command have been removed. Instead, two immediate execute auxiliary commands are included. Request control (rqc) will cause a transition from CIDS to CADS, and the release control command (rlc) will return the function to CIDS. The TCT command is treated similarly to an unrecognized addressed command but will cause a UNC interrupt if the device is in TADS.

Figure 3-22 is a representation of the sequence of events involved in passing control from one TMS 9914A based device to another. The device passing control must initially ensure that it is not in TADS; then it should send out the talk address of the device to receive control. The receiving device will enter TADS, and after any DAC holdoff has been released, the host MPU of the device passing control will set a BO interrupt indicating that it may then send the TCT command. The TCT command will cause a UNC interrupt to the host MPU of the receiving device, and also a DAC holdoff will occur. The host MPU of the receiving device must examine its Command Pass Through Register, and upon identifying TCT, should write the auxiliary command 'rqc' to put its TMS 9914A register into CADS. The receiving device may then release DAC with a 'dacr' auxiliary command causing another BO interrupt at the device passing control. This indicates that the 'rlc' auxiliary command may then be used by the host MPU of the device passing control to return its TMS 9914A register to CIDS and allow ATN to go false. The receiving device then enters CACS, asserts ATN, and its host MPU gets a BO interrupt as the source handshake becomes active. The passing of control is complete.

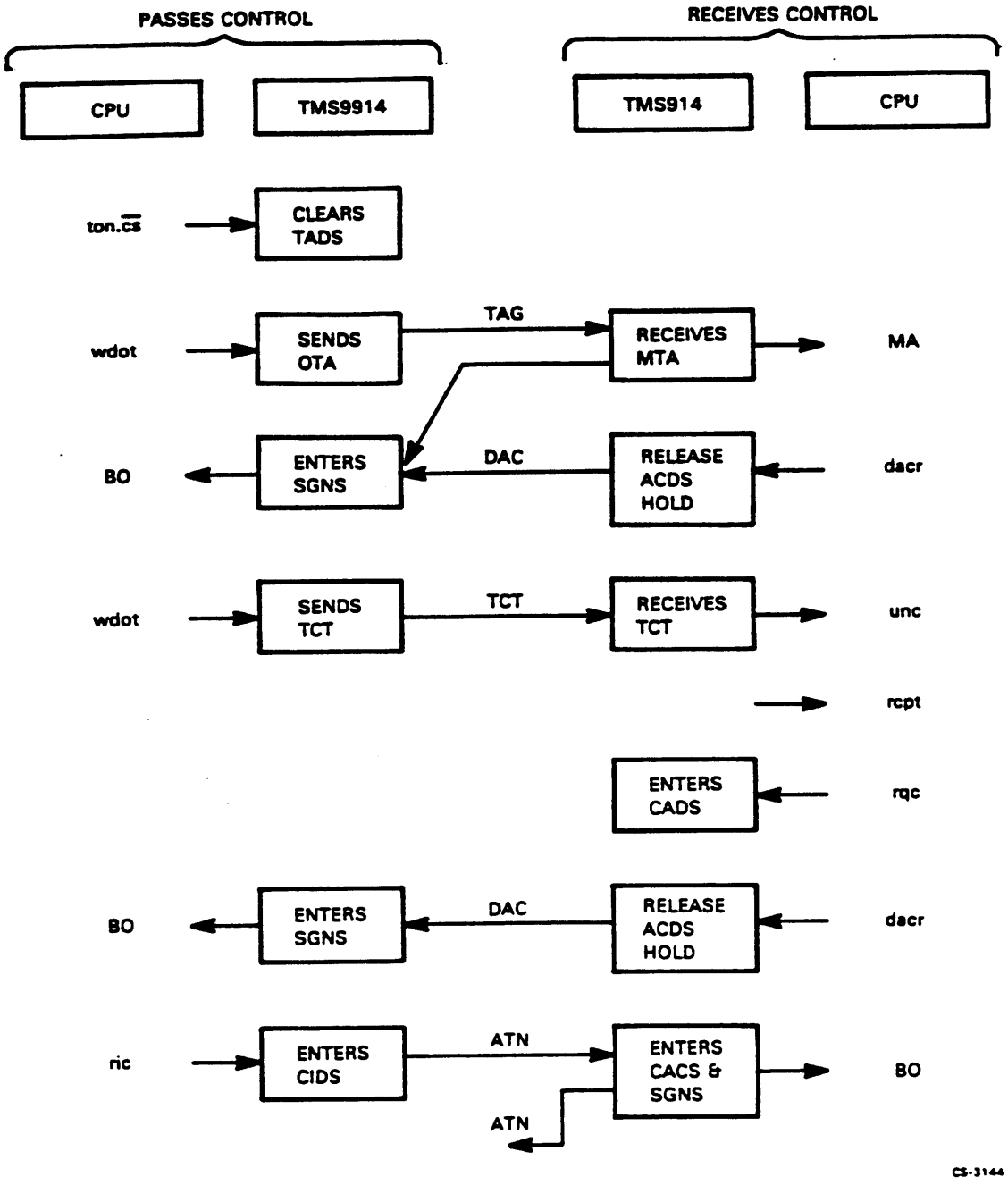


Figure 3-22 Passing Control Between TMS 9914s

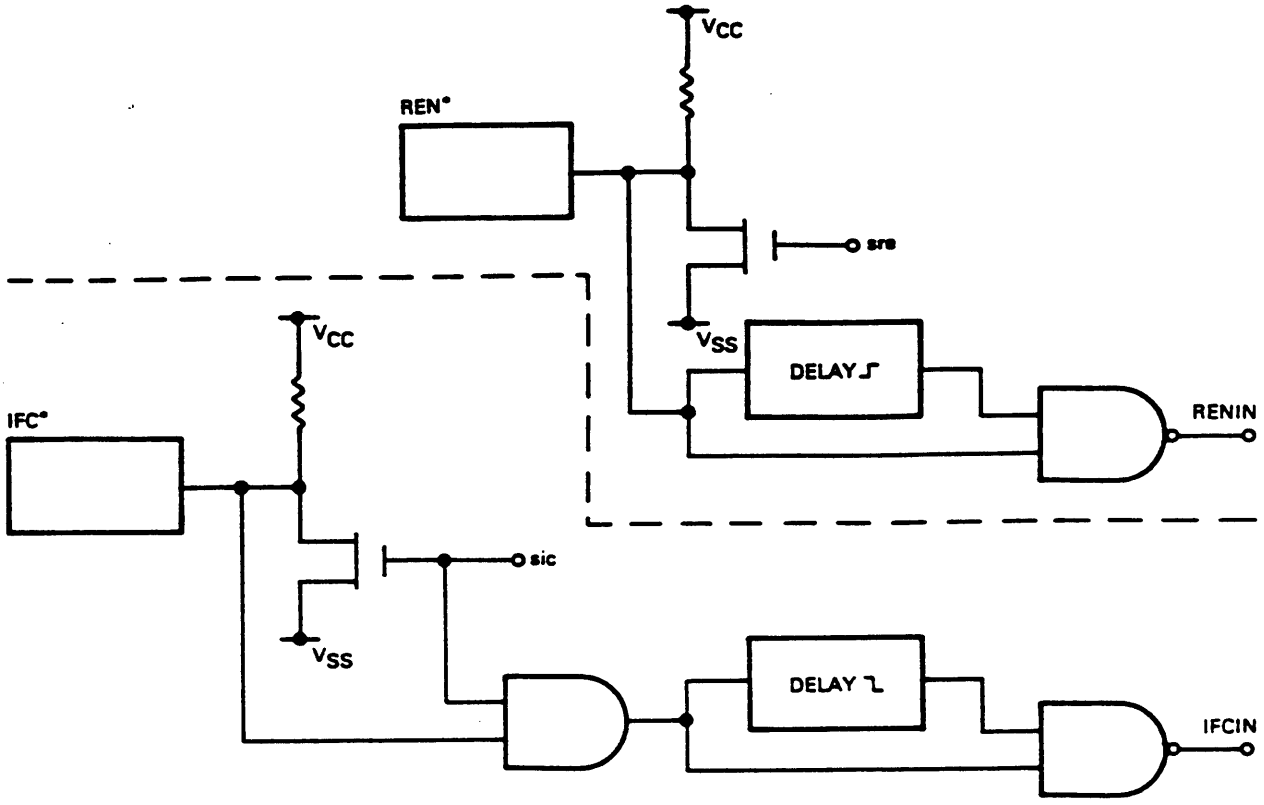
3.7.3 System Controller

The TMS 9914A register has no on-chip means of determining whether or not it is the system controller. Instead, this is determined by the software and by the configuration of the buffers to the IEEE-488 bus.

The REN and IFC outputs of the TMS 9914A register are controlled by the auxiliary commands 'sre' and 'sic'. These should never be used by the host MPU of a device unless it is the system controller. As may be seen from Figure 3-23, the REN and IFC outputs of the TMS 9914A registers are open drains with internal pull-ups. This means that the outputs are capable of driving the inputs of the buffers if the device is a system controller. If not, the buffers will drive into the REN and IFC pins and override the pull-ups. Hence, no direction control is required.

The false transition of REN and the true transition of IFC are both debounced to prevent noise on these lines from causing permanent state changes on the TMS 9914A register. In addition, the internal interface clear signal (IFCIN) is held false if the TMS 9914A register is sending IFC. Figure 3-21 shows the reason for this. If the device is not a system controller, then the occurrence of IFC will return the controller function to CIDS.

If, however, the device is a system controller, when it asserts IFC and is in CIDS, the 'sic' auxiliary command will cause it to enter CADS. As IFCIN is suppressed, it will not be forced back into CIDS, and there will be no conflict.



*THE "REN" AND "IFC" SIGNALS ARE AT THE PINS OF THE TMS9914A AND ARE THEREFORE NEGATVIE LOGIC SIGNALS. THE REMAINING SIGNALS ARE CONVENTIONAL POSITIVE LOGIC SIGNALS.

Figure 3-23 IFC and REN Pins

Table 3-27 Multiline Interface Messages

Command	Symbol	DIO 8 - 1	Class	Interrupt (1,2)	DAC (3) Holdoff	Note
ADDRESSED COMMAND GROUP	ACG	ØØØXXXX	AC	--	--	
DEVICE CLEAR	DCL	X0010100	UC	DCAS	YES	
GROUP EXECUTE TRIGGER	GET	X0001000	AC	GET	YES	
GO TO LOCAL	GTL	X0000001	AC	RLC	NO	14
LISTEN ADDRESS GROUP	LAG	X01XXXXX	AD	--	--	
LOCAL LOCKOUT	LLO	X0010001	UC	NONE	NO	
MY LISTEN ADDRESS	MLA	X01AAAAA	AD	MA,MAC,RLC	MA ONLY	4,14
MY TALK ADDRESS	MTA	X10AAAAA	AD	MA,MAC	MA ONLY	4
MY SECONDARY ADDRESS	MSA	X11SSSSS	SE	APT	YES	5,6
OTHER SECONDARY ADDRESS	OSA	SCG.MSA-	SE	APT	YES	6,7
OTHER TALK ADDRESS	OTA	TAG.MTA-	AD	MAC	NO	
PRIMARY COMMAND GROUP	PCG	ACG+UCG+ LAG+TAG	--	--		
PARALLEL POLL CONFIGURE	PPC	X0000101	AC	UNC	YES	8
PARALLEL POLL ENABLE	PPE	X110SPPP	SE	UNC	YES	9,10
PARALLEL POLL DISABLE	PPD	X111DDDD	SE	UNC	YES	9,11
PARALLEL POLL UNCONFIGURE	PPU	X0010101	UC	UNC	YES	12
SECONDARY COMMAND GROUP	SCG	X11XXXXX	SE	--	--	
SELECTED DEVICE CLEAR	SDC	X0000100	AC	DCAS	YES	
SERIAL POLL DISABLE	SPD	X0011001	UC	NONE	NO	
SERIAL POLL ENABLE	SPE	X0011000	UC	NONE	NO	
TAKE CONTROL	TCT	X0001001	AC	UNC	YES	13
TALK ADDRESS GROUP	TAG	X10XXXXX	AD	--	--	
UNLISTEN	UNL	X0111111	AD	MAC	NO	
UNTALK	UNT	X1011111	AD	--	--	
UNIVERSAL COMMAND GROUP	UCG	X001XXXX	UC	NONE	NO	

Classes:
- UC - universal command
- AC - addressed command
- AD - address
- SE - secondary command

Symbols:
- Ø - logical zero (high level on GPIB)
- 1 - logical one (low level on GPIB)
- x - don't care (received message)

NOTES:

1. Interrupts listed are as a direct consequence of the command received. They are set during ACDS1 (see Section 3.2) and will cause the INT pin to be pulled low if unmasked.

2. The addressed commands will only cause their corresponding interrupt if the device is in LADS with the exception of TCT.

3. A DAC holdoff will only be caused if the corresponding interrupt is unmasked.

4. AAAAA represents the primary address of a device.

5. SSSSS represents the secondary address of a device.

6. Secondary addresses are handled by means of address pass through (APT interrupt). The host MPU should respond by writing the 'dacr' auxiliary command with 'cs' false.

7. If OSA is passed through by means of the APT interrupt, the host MPU should respond by writing the 'dacr' auxiliary command with 'cs' false.

8. PPC is not recognized by the TMS 9914A register and is therefore treated as an unrecognized address command.

9. PPE and PPD are secondary commands. These may be passed through to the host MPU using the 'pts' auxiliary command. When the PPC command is received, the 'pts' auxiliary command should be written. PPE or PPD will then cause an APT interrupt.

10. SPPP specifies the sense bit, and the desired parallel poll response is a remotely configured parallel poll (see Section 3.7.1).

11. DDDD specifies don't care bits which must be sent as zeros but need not be decoded by the host MPU of the receiving devices.

12. PPU is not recognized by the TMS 9914A register and will cause a UNC interrupt.

13. TCT is not recognized directly by the TMS 9914A register. It will cause a UNC interrupt when the device is in TADS.

14. RLC is set if MLA or GTL causes an appropriate transition in the Remote/Local function.

3.8 GENERAL OPERATION

The following typical communication sequence is used to describe the operation of the IEU11-A in general terms when both channels are interconnected with a BC08S-01 cable. Channel 1 of the IEU11-A is one device on the IEC/IEEE Bus and channel 2 is the other. The selection of these channels is done by the MUX bit in the control status register. Channel 1 performs the controller and listener functions, while channel 2 is assigned the function of talker. The following sequence is almost identical with the programming example in Section 3.9.

1. The processor initializes both channels by asserting the INIT signal on the UNIBUS (usually power-up) or by setting MC (Master Clear) in each of the unit CSR registers.

2. The processor loads the interrupt mask registers of both channels with the appropriate bits to enable all required interrupts.

3. The processor loads the address registers of both channels with assigned device primary addresses.

4. The SYS CONT bit in the control and status register 1 is set to select channel 1 as the system controller. Either channel could be system controller.

5. The auxiliary command register 1 is loaded with the send interface clear command (SIC) bit to place the interface system in a known quiescent state. The interface clear message is sent by means of the IEC/IEEE bus. After 100 microseconds, the IFC message may be cleared by loading SIC and setting the C/S bit to zero in the auxiliary command register 1.

6. Step 5 automatically causes channel 1 to enter the controller active state (CACS) and therefore is the controller-in-charge. Consequently, the ATN line is in the true state.

7. The primary talk address of channel 2 is loaded into the data out register of channel 1 which transmits the primary talk address by means of the IEC/IEEE bus.

8. Step 7 causes the MA and MAC bits in the interrupt status register of channel 2 to become true. An interrupt is generated provided the appropriate mask bits and the INT ENB bit of the control status register 2 are set. Also, an ACDS holdoff is generated, which allows the processor to respond to the interrupt, to recognize the cause by reading the interrupt status registers, and therefore perform the appropriate action (for example, check if the Talker Addressed State (TADS) is in the true state) before the holdoff is released.

9. The controller-in-charge sets itself up as a listener by using the Listen Only command (LON) which has to be loaded into auxiliary command register 1 by the processor.

10. All parameters that are required to perform a DMA data transfer have to be loaded into the control and status, bus address, and byte count registers by the processor. In this example, channel 1 performs DATOB whereas channel 2 performs DATI cycles.

11. Loading the Go to Standby command (GTS) into the auxiliary command register 1 sets the ATN line false and thus the controller enters the controller standby state (CSBS).

12. Performing step 11 initiates a DMA data transfer (BOP) from the CPU main memory back to memory by means of the IEC/IEEE bus. This process is automatic and needs no further processor intervention.

13. In this example, the data transfer is terminated upon byte count overflow in both byte count registers 1 and 2, respectively (for example, the selected byte count is the same for both registers). The assertion of both these BC OF bits clears the DMA ENB bit in the control and status registers 1 and 2. To restart the DMA data transfer, a new setup is required.

3.9 PROGRAMMING EXAMPLE

The following program sequence provides an example of how the IEU11-A (IEQ11-A) option operates. This programming example provides a routine that enables every character that is typed to be echoed to the screen, which means that two identical characters appear on the screen.

To perform this program sequence, the program must establish the following IEC/IEEE bus configuration: Channel 1 is assigned the role of both controller and listener, while channel 2 is assigned the role of talker (refer to Section 3.8 for details of this setup and how to initiate the data transfer). In order for this program sequence to function, a BC08S-01 cable must connect both channels.

```
        START
10$:    TSB     @# RXCSR            ;Console routine
        BPL     10$                 ;Console routine
        MOV     @#RXBUF,@#TXBUF     ;Echo typed character
        MOV     @#RXBUF,@#2000      ;Get data from RX Data Buffer
        MOV     #10,@#CSR           ;Select channel 2
        MOVB    #200,@#ICRx         ;Initialize channel 2
        CLRB    @#ICRx              ;Clear auxiliary command SWRST
        CLRB    @#ISR               ;Load Interrupt Mask Register 0
        CLRB    @#ISRx              ;Load Interrupt Mask Register 1
        MOVB    #1,@#IIRx           ;Load device primary address "1"
        MOV     #2000,@#BAR         ;Load Bus Address Register
        MOV     #177777,@#BCR       ;Load Byte Count Register
        MOV     #5,@#CSR            ;Set DMA ENB and DMA DIR bit
                                    ;in CSR and select channel 1
        MOVB    #200,@#ICRx         ;Initialize channel 1
        CLRB    @#ICRx              ;Clear auxiliary command SWRST
        CLRB    @#ISR               ;Load Interrupt Mask Register 0
        CLRB    @#ISRx              ;Load Interrupt Mask Register 1
        CLRB    @#IIRx              ;Load device primary address "0"
        MOV     #3000,@#BAR         ;Load Bus Address Register
        MOV     #177777,@#BCR       ;Load Byte Count Register
        MOV     #3,@#CSR            ;Set DMA ENB and SYS CONT bit in CSR
        MOVB    #217,@#ICR#         ;Set IFC line true
        MOV     #500,R0             ;Delay for release of IFC line
                                    ;(100 microsec)
```

```
20$:  DEC    R0                ;
      BNE    20$               ;
      MOVB   #17,@#ICRx        ;Clear auxiliary command SIC
      MOVB   #101,@#IDRx       ;Select channel 2 as Talker
      MOVB   #211,@#ICRx       ;Select channel 1 as Listener
      MOVB   #13,@#ICRx        ;Release ATN line and start
                               ;DMA data transfer
30$:  TST    @#CSR             ;Wait for byte count overflow
      BPL    30$
      MOVB   #14,@#ICRx        ;Reassert ATN line
40$   TSTB   @#TXCSR           ;Console routine
      BPL    40$               ;Console routine
      MOV    @#3000,@3TXBUF    ;Send character to TX Data Buffer
                               ;and print it
      MOV    #410,@#CSR        ;Load MC and MUX bit in CSR
                               ;(clear channel 1)
      MOV    #400,@#CSR        ;Load MC bit in CSR (clear channel 2)
      JMP    10$               ;Go to start
      END
```

NOTE

The character "x", which appears in the above programming example in addition to the register designation, refers to the high order byte of the appropriate register.

4.1 INTRODUCTION

The corrective maintenance philosophy for both the IEU11-A and IEQ11-A option is to replace the failing unit only. This field replaceable unit (FRU) maintenance is used to ensure that the system can be restored to operating status in minimum time. Therefore, only units such as failing modules or defective cables are replaced.

Diagnostics are used to detect system failures and to verify the functionality of a module. A system exerciser is run to test the system, while a repair diagnostic is used to test the functionality of a module. The PDP-11 and LSI-11 systems use the same diagnostics.

Once the IEU11-A/IEQ11-A option is installed, no preventive maintenance procedures or periodic alignment/adjustment procedures are necessary.

4.2 REQUIRED TOOLS AND EQUIPMENT

The DIGITAL Field Service tool kit and the BC08S-01 test cable are required. The BC08S-01 test cable is used to interconnect the two IEC/IEEE ports (J1 and J2) on either the M8648 module (PDP-11 or VAX-11 systems) or the M8634 module (LSI-11/MICRO systems). This test cable allows testing of the module without using any external IEC/IEEE instruments. To test the IEC/IEEE bus cables that interconnect the module (M8648 or M8634) to the I/O bulkhead panel, an Instrument Bus cable with either dual IEC-625 or IEEE-488 connectors on both ends must be connected to the I/O bulkhead panel. For instructions on how to do this, refer to Section 2.8.2 for a PDP-11 or VAX-11 installation, or Section 2.15.2 for an LSI-11/MICRO system installation.

4.3 CORRECTIVE MAINTENANCE

The corrective maintenance procedure is an aid for the Field Service engineer to isolate and repair faults within the IEU11-A/IEQ11-A option. The diagnostic programs are the basic tool used to isolate failures, since the diagnostics test all six functional areas of the IEU11-A/IEQ11-A option. By using a BC08S-01 test cable, no external IEC/IEEE instruments are necessary to run the diagnostics. Figure 4-1 is a troubleshooting flowchart. This flowchart provides a logical approach to isolating a fault within the IEU11-A/IEQ11-A option.

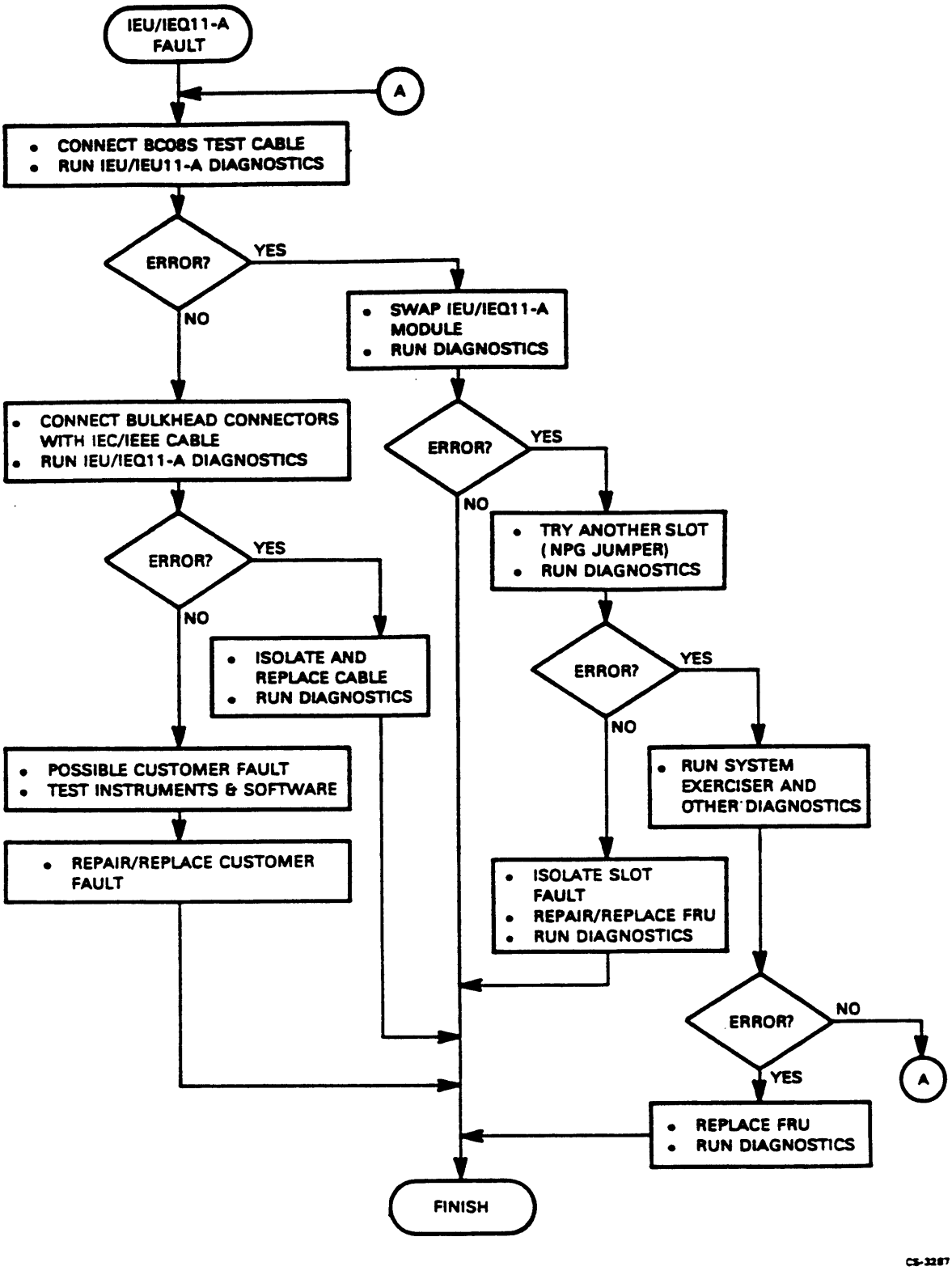


Figure 4-1 IEU11-A and IEQ11-A Troubleshooting Flowchart

The structure of the IEU11-A/IEQ11-A diagnostic programs allows the diagnostic to test one channel at a time. Therefore, most of the failures can be isolated to one of the channels. This feature, along with the fact that the TMS 9914A integrated circuits are plugged into sockets, facilitates troubleshooting. For example, the two TMS 9914A integrated circuits can be swapped, and if the failure moves to the other channel, one of the TMS 9914A integrated circuits must be defective. With the aid of the error printout, the defective integrated circuit should be easily located.

Because of the IEU11-A/IEQ11-A hardware structure, some of the logic sections are used for both channels. Therefore, the hardware structure limits the kinds of failures, but does help in isolating the failure. For example, in using the PDP-11 diagnostic CZIEA??, if an error occurs in Test 23, Test 24 should also be run, since both are DMA tests. If Test 24 runs correctly, it can be assumed that the DMA CONTROL and sections of the DMA logic are not defective, because both sections are used by both channels.

4.4 IEU11-A/IEQ11-A DIAGNOSTIC SOFTWARE

The same diagnostic software is used for both the PDP-11 and LSI-11 systems. Other diagnostic software is used for the VAX-11 and MICRO/VAX systems. Therefore, refer to the respective section in the following diagnostic software sections.

4.4.1 Diagnostic Software (PDP-11 and LSI-11 Systems)

There are two diagnostic programs used to test the IEU11-A/IEQ11-A option when installed in either a PDP-11 or LSI-11 system. The diagnostic programs are the CXIEA?? DEC-X/11 System Exerciser, and the CZIEA?? Static Diagnostic.

The DEC-X/11 System Exerciser aids in determining a failing option within a PDP-11 system or LSI-11 system, but it may not aid in the option repair. Option fault isolation requires using the CZIEA?? Static Diagnostic.

The CZIEA?? Static Diagnostic verifies the IEU11-A/IEQ11-A option operation according to specifications and within its actual environment. The diagnostic program consists of 28 tests. However, Tests 27 and 28 are not used to test the IEU11-A option. These two tests are used to test the IEQ11-A option in conjunction with a Q-22 bus.

Refer to the diagnostic listing for both details on loading and running these diagnostics, and for a description of each test.

4.4.2 Diagnostic Software (VAX-11 Systems)

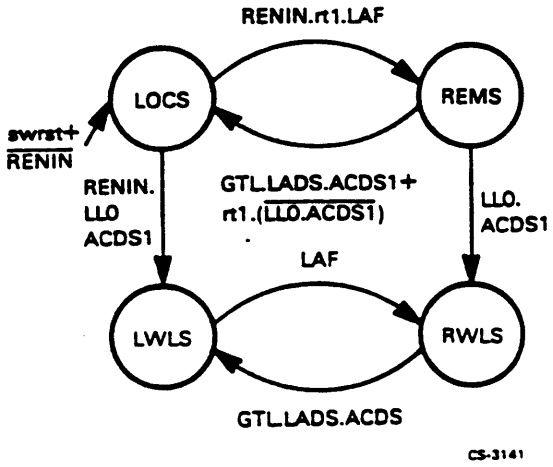
There are two diagnostic programs that are used to test the IEU11-A option when it is installed in a VAX-11 system. The two diagnostics are the IEU11-A M8648 On-line Test and the IEU11-A M8648 Off-line Test.

The IEU11-A M8648 On-line Test (EVCDB) is a functional level (Level 2R) diagnostic that exercises an IEU11-A option. This diagnostic aids in determining a failing option. Option fault isolation is accomplished by using the IEU11-A M8648 Off-line Test (EVCDC). The EVCDC diagnostic is used both to verify the IEU11-A option according to specifications, and for proper operation in an actual environment.

Both diagnostics are run under the Diagnostic Supervisor. Instructions for running the Diagnostic Supervisor can be referenced in the Diagnostic System User's Guide for the respective type of VAX-11 processor. Refer to the diagnostic listing for operating and loading procedures.

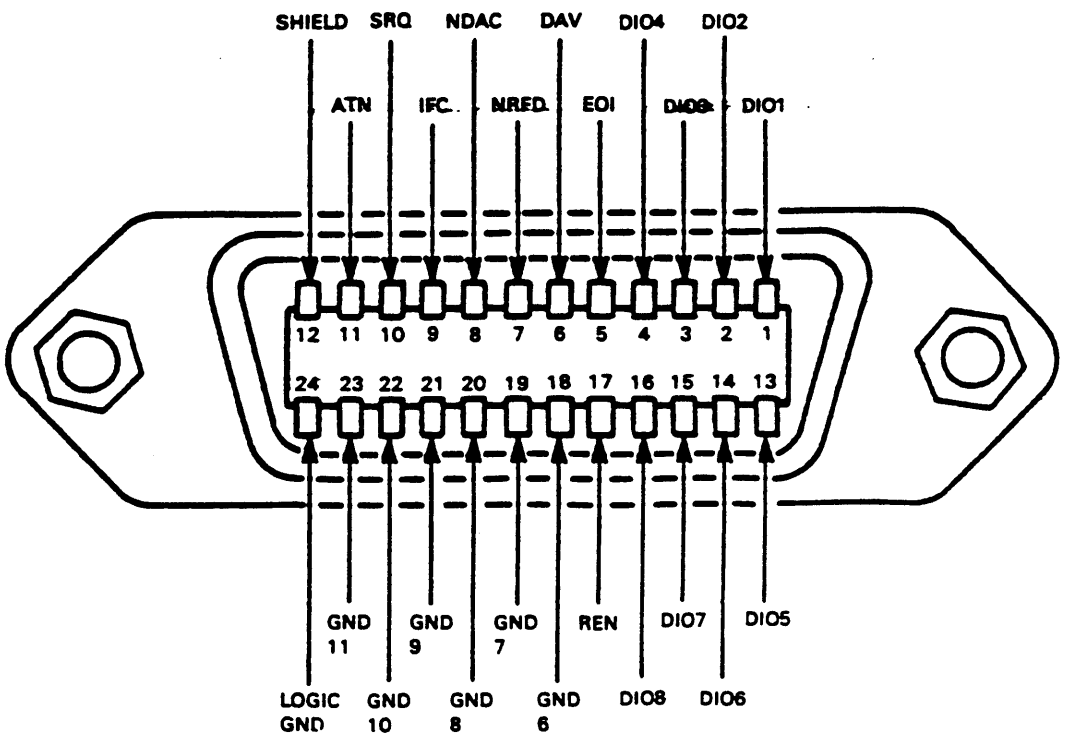
4.4.3 Diagnostic Software (MICRO/VAX Systems)

The MDM IEQ11-A Diagnostic NAIEA? is used to test the IEQ11-A option when it is installed in a MICRO/VAX system. This diagnostic aids in determining a faulty option and verifies the IEQ11-A operation.

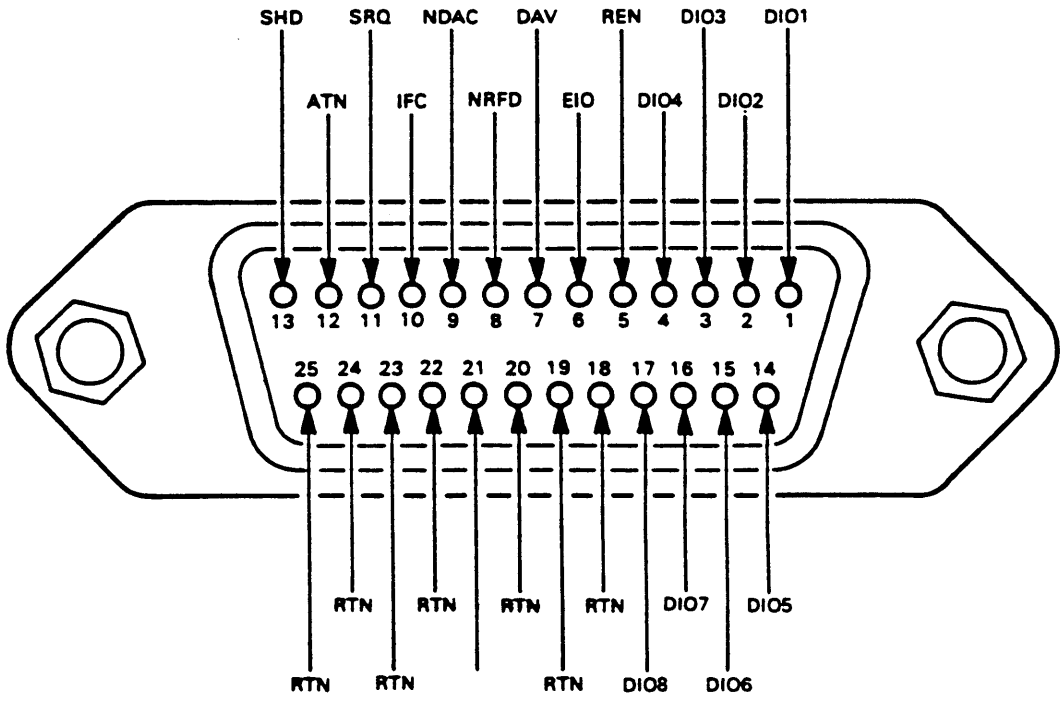


APPENDIX A
STANDARD CONNECTIONS

IEEE-488 STANDARD CONNECTOR



IEC-625 STANDARD CONNECTOR



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APPENDIX B
REMOTE MESSAGE CODING

MESSAGE NAME	MNEMONIC	TYPE CLASS	BUS SIGNAL LINES			
			DIO 87 654 321	DAV NRFD NDAC	ATN	EOI SRQ IFC REN
ADDRESSED COMMAND GROUP	ACG	M AC	XD 00X XXX	XXX	1	X X X X
ATTENTION	ATN	U UC	XX XXX XXX	XXX	1	X X X X
DATA BYTE	DAB	M DD	DD DDD DDD 87 654 321	XXX	0	X X X X
DATA ACCEPTED	DAC	U HS	XX XXX XXX	XXD	X	X X X X
DATA VALID	DAV	U HS	XX XXX XXX	1XX	X	X X X X
DEVICE CLEAR	DCL	M UC	XD 010 100	XXX	1	X X X X
END	END	U ST	XX XXX XXX	XXX	0	1 X X X
END OF STRING	EOS	M DD	EE EEE EEE 87 654 321	XXX	0	X X X X
GROUP EXECUTE TRIGGER	GET	M AC	XD 001 000	XXX	1	X X X X
GO TO LOCAL	GTL	M AC	XD 000 001	XXX	1	X X X X
IDENTIFY	IDY	U UC	XX XXX XXX	XXX	X	1 X X X
INTERFACE CLEAR	IFC	U UC	XX XXX XXX	XXX	X	X X 1 X
LISTEN ADDRESS GROUP	LAG	M AD	XD 1XX XXX	XXX	1	X X X X
LOCAL LOCKOUT	LLO	M UC	XD 010 001	XXX	1	X X X X
MY LISTEN ADDRESS	MLA	M AD	XD 1LL LLL 54 321	XXX	1	X X X X
MY TALK ADDRESS	MTA	M AD	1X 0TT TTT 54 321	XXX	1	X X X X
MY SECONDARY ADDRESS	MSA	M SE	X1 1SS SSS 54 321	XXX	1	X X X X
NULL BYTE	NUL	M DD	00 000 000	XXX	X	X X X X
OTHER SECONDARY ADDRESS	OSA	M SE	(OSA = SCG ^ $\overline{\text{MSA}}$)			
OTHER TALK ADDRESS	OTA	M AD	(OTA = TAG ^ $\overline{\text{MTA}}$)			
PRIMARY COMMAND GROUP	PCG	M —	(PCG = ACG v UCG v LAG v TAG)			
PARALLEL POLL CONFIGURE	PPC	M AC	XD 000 101	XXX	1	X X X X
PARALLEL POLL ENABLE	PPE	M SE	X1 10S PPP 321	XXX	1	X X X X
PARALLEL POLL DISABLE	PPD	M SE	X1 11D DDD 4 321	XXX	1	X X X X
PARALLEL POLL RESPONSE 1	PPR1	U ST	XX XXX XX1	XXX	1	1 X X X
PARALLEL POLL RESPONSE 2	PPR2	U ST	XX XXX X1X	XXX	1	1 X X X
PARALLEL POLL RESPONSE 3	PPR3	U ST	XX XXX 1XX	XXX	1	1 X X X
PARALLEL POLL RESPONSE 4	PPR4	U ST	XX XX1 XXX	XXX	1	1 X X X
PARALLEL POLL RESPONSE 5	PPR5	U ST	XX X1X XXX	XXX	1	1 X X X
PARALLEL POLL RESPONSE 6	PPR6	U ST	XX 1XX XXX	XXX	1	1 X X X
PARALLEL POLL RESPONSE 7	PPR7	U ST	X1 XXX XXX	XXX	1	1 X X X
PARALLEL POLL RESPONSE 8	PPR8	U ST	1X XXX XXX	XXX	1	1 X X X
PARALLEL POLL UNCONFIGURE	PPU	M UC	XD 010 101	XXX	1	X X X X
REMOTE ENABLE	REN	U UC	XX XXX XXX	XXX	X	X X X 1
READY FOR DATA	RFD	U HS	XX XXX XXX	XXX	X	X X X X
REQUEST SERVICE	RQS	U ST	X1 XXX XXX	XXX	0	X X X X
SECONDARY COMMAND GROUP	SCG	M SE	X1 1XX XXX	XXX	1	X X X X
SELECTED DEVICE CLEAR	SDC	M AC	XD 000 100	XXX	1	X X X X
SERIAL POLL DISABLE	SPD	M UC	XD 011 001	XXX	1	X X X X
SERIAL POLL ENABLE	SPE	M UC	XD 011 000	XXX	1	X X X X
SERVICE REQUEST	SRQ	U ST	XX XXX XXX	XXX	X	X 1 X X
STATUS BYTE	STB	M ST	SX SSS SSS 8 654 321	XXX	0	X X X X
TAKE CONTROL	TCT	M AC	XD 001 001	XXX	1	X X X X
TALK ADDRESS GROUP	TAG	M AD	X1 0XX XXX	XXX	1	X X X X
UNIVERSAL COMMAND GROUP	UCG	M UC	XD 01X XXX	XXX	1	X X X X
UNLISTEN	UNL	M AD	XD 111 111	XXX	1	X X X X

SYMBOLS: TYPE – U = UNILINE MESSAGE
M = MULTILINE MESSAGE
CLASS – AC = ADDRESSED COMMAND
AD = ADDRESS (TALK OR LISTEN)
DD = DEVICE DEPENDENT
HS = HANDSHAKE
UC = UNIVERSAL COMMAND
SE = SECONDARY
ST = STATUS

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APPENDIX C
HANDSHAKE PROCESS TIMING SEQUENCE

C.1 GENERAL COMMENTS

Each data byte transferred by the interface system uses the handshake process to exchange data between source and acceptor. Typically, the source is a Talker and the acceptor is a Listener.

Figure C-1 illustrates the handshake process by indicating the actual waveforms on the DAV, NRFD and NDAC signal lines. The NRFD and NDAC signals each represent composite waveforms resulting from two or more listeners accepting the same data byte at slightly different times due to variations in the transmission path length and different response rates (delays) to accept and process the data byte.

Figure C-2 represents the same sequence of events in flowchart form, to transfer a data byte between source and acceptor.

The annotation numbers on the flow chart and the timing sequence diagram refer to the same event on the list of events.

NOTE

The C-2 flow diagram is not intended to represent the only method of implementing and acceptor handshake.

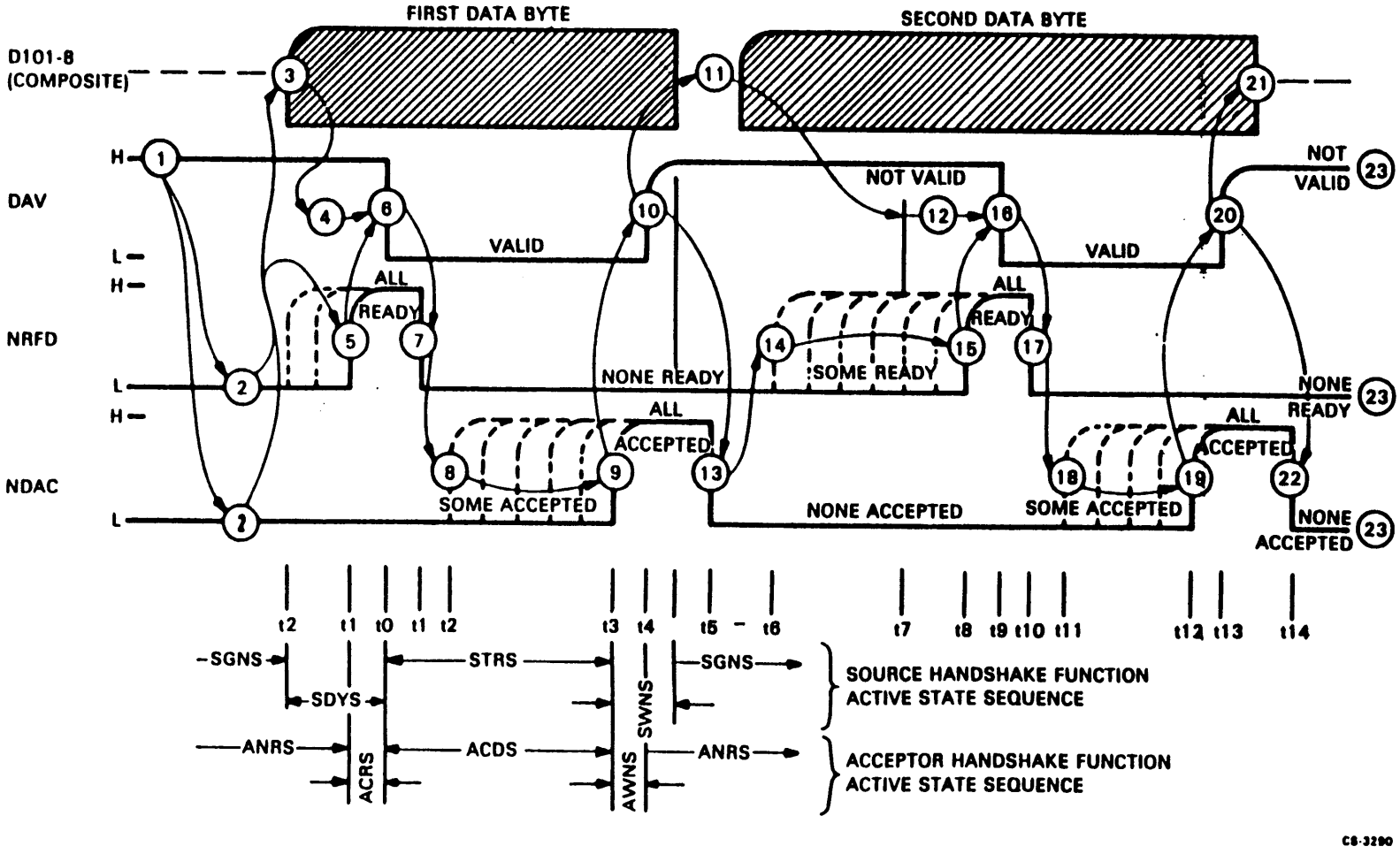

Figure C-1 Handshake Process Timing Diagram

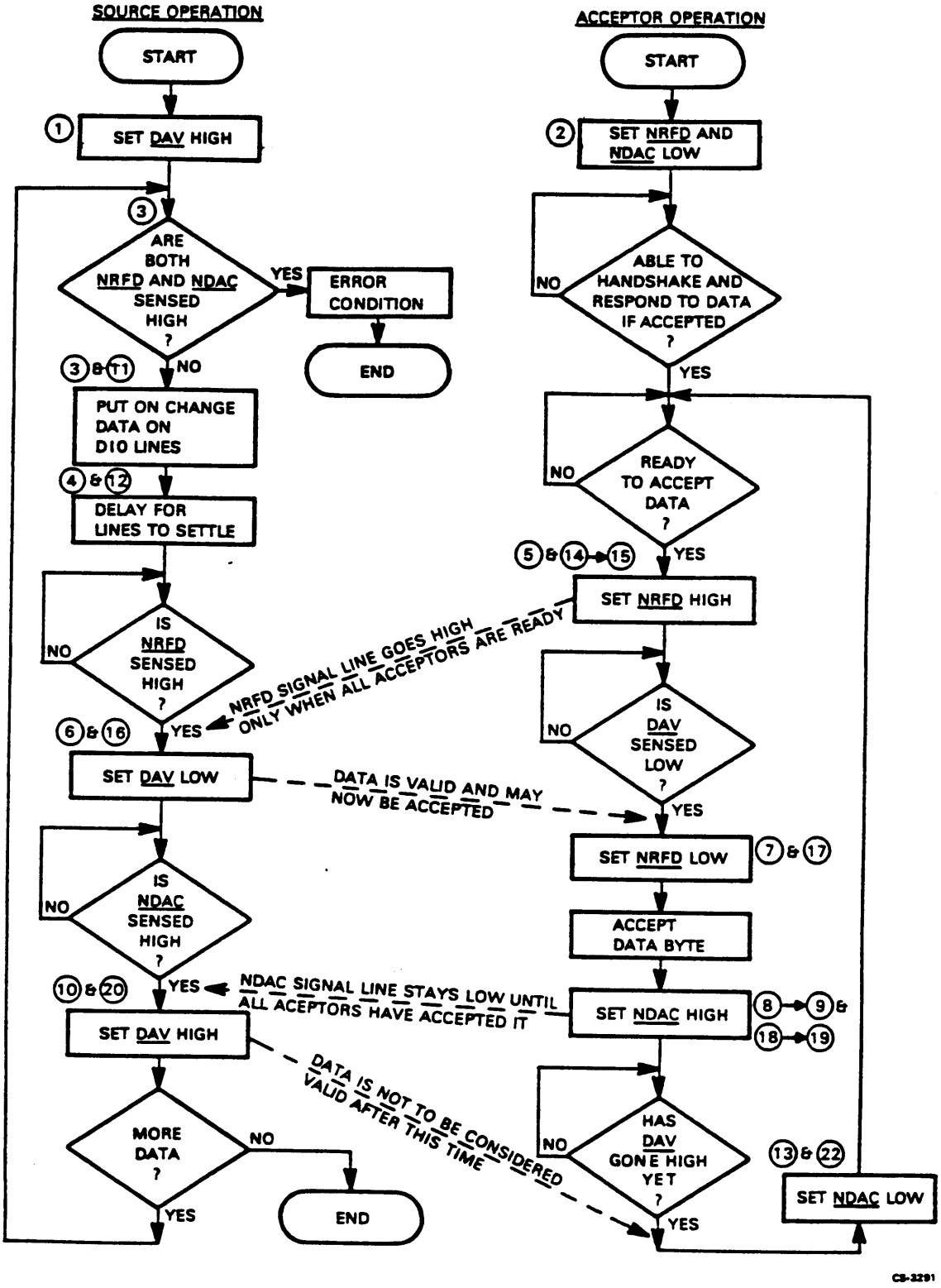

Figure C-2 Handshake Process Flow Diagram

C.2 LIST OF EVENTS FOR HANDSHAKE PROCESS

1. - Source initializes DAV to High (data not valid).

2. - Acceptors initialize NRFD to Low (none are ready for data), and set NDAC to low (none have accepted the data).

3. t_{-2} Source checks for error condition (both NRFD and NDAC High), then sets data byte on DIO lines.

4. t_{-2} $t_{\emptyset}$ Source delays to allow data to settle on DIO lines.

5. t_{-1} Acceptors have all indicated readiness to accept first data byte; NRFD line goes high.

6. $t_{\emptyset}$ Source, upon sensing NRFD High, sets DAV Low to indicate that the data on DIO lines is settled and valid.

7. t_1 First acceptor sets NRFD Low to indicate that it is no longer ready, then accepts the data. (NDAC remains Low due to other acceptors driving NDAC Low.)

8. t_2 First acceptor sets NDAC High to indicate that it has accepted the data. (NDAC remains Low due to other acceptors driving NDAC Low.)

9. t_3 Last acceptor sets NDAC High to indicate that it has accepted the data; all have now accepted and the NDAC line goes High.

10. t_4 Source, having sensed that NDAC is High, sets DAV High. This indicates to the acceptors that data on the DIO lines must now be considered not valid.

11. t_4-t_7 Source changes data on the DIO lines.

12. t_7-t_9 Source delays to allow data to settle on DIO lines.

13. t_5 Acceptors, upon sensing DAV high (at 10) set NDAC Low in preparation for next cycle. NDAC line goes Low as the first acceptor sets the line Low.

14. t_6 First acceptor indicates that it is ready for the next data byte by setting NRFD High. (NRFD remains Low due to other acceptors driving NRFD Low.)

15. t_8 Last acceptor indicates that it is ready for the next data byte by setting NRFD High; NRFD signal line goes High.

16. t_9 Source, upon sensing NRFD High, sets DAV Low to indicate that data on DIO lines is settled and valid.

17. t_{10} First acceptor sets NRFD Low to indicate that it is not longer ready, then accepts the data.

18. t_{11} First acceptor sets NDAC High to indicate that it has accepted the data (as in 8).

19. t_{12} Last acceptor sets NDAC High to indicate that it has accepted the data (as in 9).

20. t_{13} Source, having sensed that NDAC is High, sets DAV High (as in 10).

21. - Source removes data byte from DIO signal lines after setting DAV high.

22. t_{14} Acceptors, upon sensing DAV High, set NDAC Low in preparation for next cycle.

23. - Note that all three handshake lines are at their initialized states, as at 1 and 2.

(SENT AND RECEIVED WITH ATN=1)

b7 b6 b5 → / BITS ② b4 b3 b2 b1 / ROW ↓ COLUMN →	0 0 0	MSG ①	0 0 1	MSG	0 1 0	MSG	0 1 1	MSG	1 0 0	MSG	1 0 1	MSG	1 1 0	MSG	1 1 1	MSG
	0		1		2		3		4		5		6		7	
0 0 0 0 0	NUL		DLE		SP		0		@		P				p	
0 0 0 1 1	SOH	GTL	DC1	LLO	!		1		A		Q		a		q	
0 0 1 0 2	STX		DC2		"		2		B		R		b		r	
0 0 1 1 3	ETX		DC3		#		3		C		S		c		s	
0 1 0 0 4	EOT	SDC	DC4	DCL	$		4		D		T		d		t	
0 1 0 1 5	ENQ	PPC③	NAK	PPU	%		5		E		U		e		u	
0 1 1 0 6	ACK		SYN		&		6		F		V		f		v	
0 1 1 1 7	BEL		ETB		'		7		G		W		g		w	
1 0 0 0 8	BS	GET	CAN	SPE	(		8		H		X		h		x	
1 0 0 1 9	HT	TCT	EM	SPD	)		9		I		Y		i		y	
1 0 1 0 10	LF		SUB		*		:		J		Z		j		z	
1 0 1 1 11	VT		ESC		+		;		K		[		k		{	
1 1 0 0 12	FF		FS		,		<		L		\		l		|	
1 1 0 1 13	CR		GS		-		=		M		]		m		}	
1 1 1 0 14	SO		RS		.		>		N		^		n		~	
1 1 1 1 15	SI		US		/		?		O		_		o		DEL	

MLA ASSIGNED TO DEVICE (MSG column)
MTA ASSIGNED TO DEVICE (MSG column)
MEANING DEFINED BY PCG CODE (MSG column)

ADDRESSED COMMAND GROUP (ACG)
UNIVERSAL COMMAND GROUP (UCG)
④ LISTEN ADDRESS GROUP (LAG)
TALK ADDRESS GROUP (TAG)

PRIMARY COMMAND GROUP (PCG)

SECONDARY COMMAND GROUP (SCG)

NOTES:

① MSG = INTERFACE MESSAGE
② b1 = D101... b7 = D107
③ REQUIRES SECONDARY COMMAND
④ DENSE SUBSET (COLUMN 2 THROUGH 5)

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