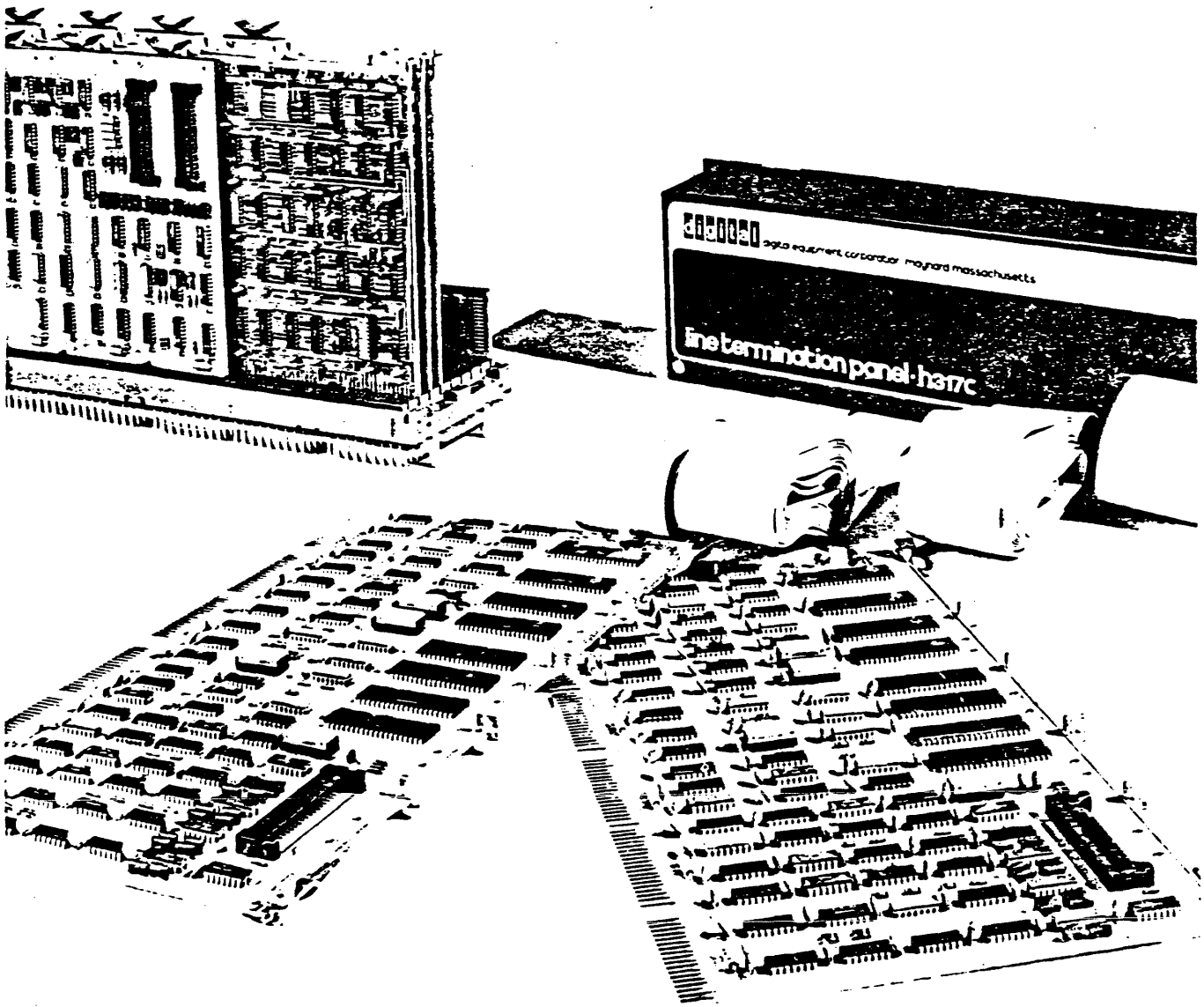
DIGITAL EQUIPMENT CORPORATION

OPTION BULLETIN

pdp11

JULY 1975

DV11 Synchronous Preprocessor



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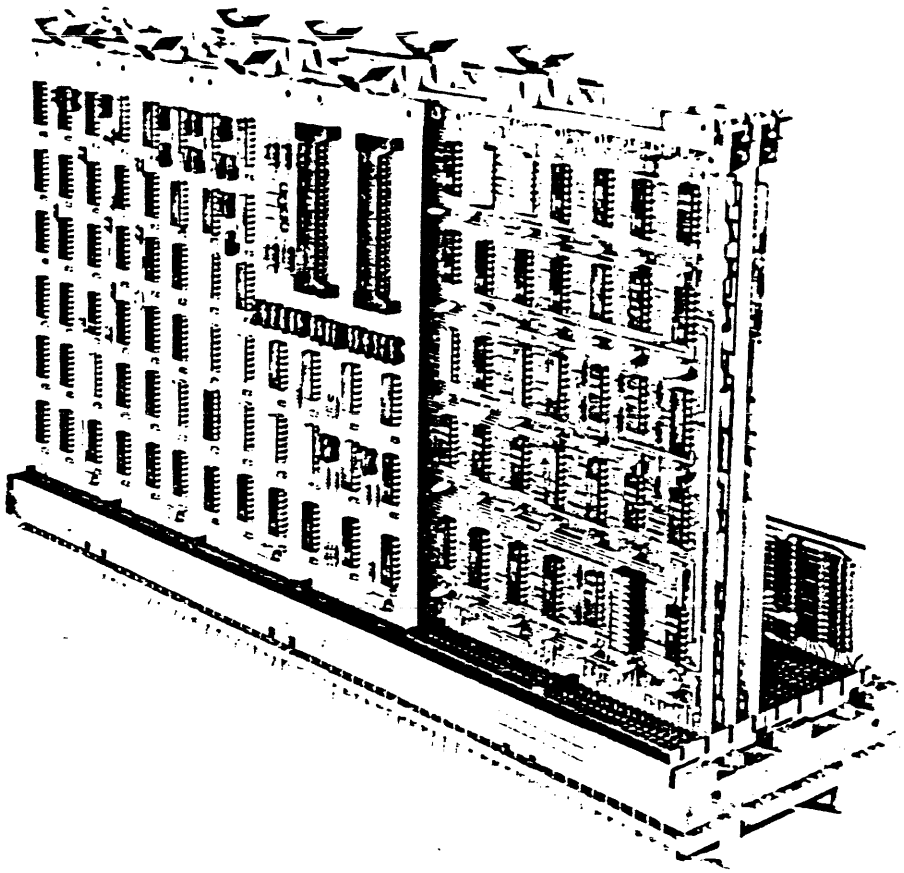
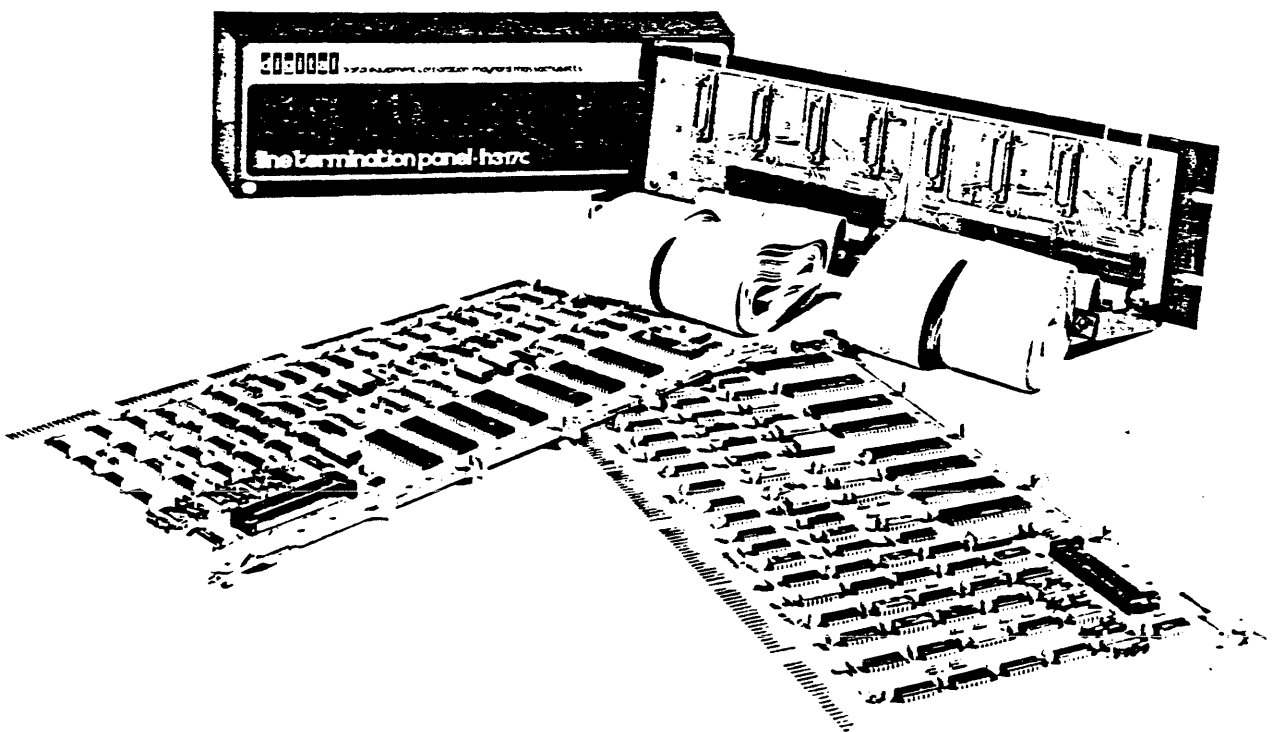


DV11-AA double system unit containing logic modules.



DV11-BA line cards and distribution panel for eight lines. Two DV11-BA's can be used with one DV11-AA.

HIGHLIGHTS

- 8- or 16-line synchronous multiplexer for use with PDP-11 family computers.
- NPR data transfers on transmission and reception.

  Total 16-line throughput of up to 38,400 characters per second (9600 baud full duplex for each line).
- Control table scheme provides programming flexibility, particularly for special character and protocol handling.
- Open-ended flexible design—hardware not committed to any specific protocol.
- 128-character first-in/first-out receiver buffer.
- Program-selectable block checks (LRC-8, CRC-16, CRC/CCITT) calculated by the hardware.
- Modem control.
- Choice of external or internal clock.
- Two program-selectable sync characters for each line.
- Switch-selectable character sizes.
- Up to 4 DV11's with total throughput of 76,800 characters per second can be connected to a PDP-11 depending on configuration and application.

GENERAL DESCRIPTION

The DV11 is a synchronous preprocessor which permits eight or sixteen synchronous lines to be interfaced to a PDP-11. It is designed to relieve the PDP-11 processor of almost the entire overhead associated with interrupt handling, character processing and CRC/LRC calculations.

It provides very high throughput (up to 38,400 characters per second total for all 16 lines) and extremely flexible handling of special data link characters. High throughput is achieved by use of direct memory (NPR) transfers on both transmission and reception. Flexibility is achieved, without committing hardware to any specific protocol, through the use of control bytes stored in core tables. The program can specify parameters in each control byte, thus providing flexibility for requirements within a specific application.

The DV11 contains provisions for up to eight reception modes for use with character-oriented protocols (for instance, there are modes for transparent data reception and for normal text reception). The action taken in each mode and the transition from one mode to another are controlled by control tables located in core memory. A control table for an individual reception state consists of 256 bytes—one for each of the possible characters that can be received during the reception.*

The DV11 hardware can perform block check calculations for longitudinal redundancy checks (LRC) and cyclic redundancy checks (CRC-16 and CRC/CCITT).

The character size (5, 6, 7 or 8 bits) and character format (no parity, even, or odd parity) are switch-selectable for each 4-line group (0-3, 4-7, 8-11, 12-15). The DV11 can calculate LRC's for all character sizes, and CRC's for 8-bit characters.

*Typically, control bytes are used to indicate how the character is to be handled, whether an interrupt is to be generated, and whether the character is to be included in the block check.

Two sync characters may be manually pre-selected for each 4-line group. Then the program can select from either of those two sync characters for each individual line. For transmission, the same sync character is used as the transmitter fill-character or an "all 1's" condition can be sent.

PHYSICAL DESCRIPTION

The DV11 consists of a 9-slot double system unit (DV11-AA) which contains the basic logic modules, a microprocessor and modem control modules, plus a distribution panel and line cards for eight lines (DV11-BA).

Two DV11-BA 8-line units can be used with a DV11-AA.

BASIC OPERATION (Figure 1)

Sixteen Synchronous Receivers assemble characters received from serial communications lines and assert a flag as each character is received. Sixteen Synchronous Transmitters disassemble characters and transmit them on serial communications lines and assert a flag whenever they can accept another character for transmission. The Master Scanner sequentially checks the synchronous receivers and transmitters for each line to see if a flag exists.

The microprocessor handles all characters received or transmitted by the DV11. It controls all non-UNIBUS data transfers and steps the Master Scanner. Except for those occasions where a UNIBUS instruction or NPR transfer involving the DV11 is taking place, the microprocessor never stops.

The microprocessor system includes a 128-character first-in/first-out storage buffer. While most characters received by the DV11 will propagate through this buffer and be directly transferred to PDP-11 core by means of an NPR transfer, the occasion may arise when the attention of the PDP-11 program is required before this is done. To prevent the synchronous receivers from experiencing data overruns during the interval that the DV11 is awaiting program attention, the microprocessor will continue to load the received characters into the first-in/first-out buffer, but the action of the microprocessor in withdrawing characters from the buffer will cease until the PDP-11 program responds to the interrupt caused by the special character at the bottom of the silo buffer. The character which requires PDP-11 program attention is copied into the Receive Interrupt Character Register at the time the interrupt is generated.

The Receiver Interrupt Character Register is a UNIBUS-addressable register used by the microprocessor to show the PDP-11 program any received character, along with line number and error flags for which the control logic requires assistance in processing.

The Receiver Control Byte Storage Register is a UNIBUS-addressable secondary register used to instruct the microprocessor how to process the character in the Receiver Interrupt Character Register.

The NPR control is the hardware which is used to gain control of the UNIBUS in order to store received char-

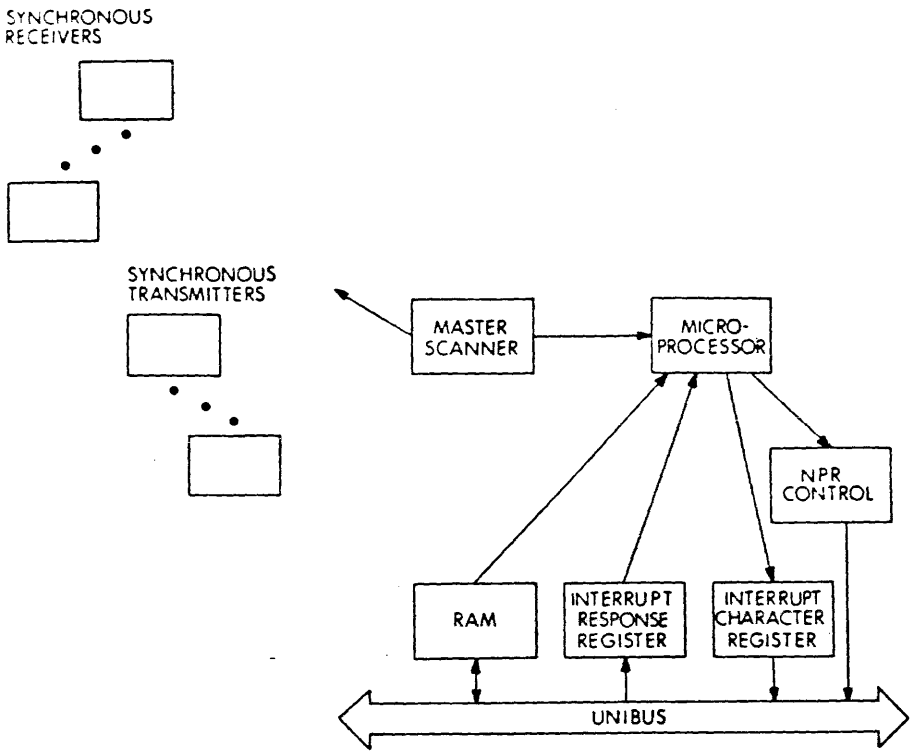


Figure 1. Basic Operation

acters, obtain characters for transmission, and to obtain control bytes that direct the character processing.

The microprocessor read/write random access memory (RAM) contains current addresses and two's complement byte counts used in NPR transfers. The initial values are loaded by the PDP-11 program via the UNIBUS, and these values are subsequently updated by the microprocessor. The RAM also contains a line protocol word for each line by which the PDP-11 program can specify what action is to be taken when the byte count reaches zero and what type of block check polynomial should be used. In addition, a line state word is stored for each line providing a snapshot of what microprocessor activity is in progress at a particular line.

RECEPTION OPERATION (Figure 2)

Line synchronization and character assembly are accomplished by LSI synchronous receivers which initially compare groups of eight bits received on each line with the preselected sync character to achieve line synchronization. When line synchronization has been achieved, subsequently-received characters are placed into a first-in/first-out, 128-character silo storage buffer. Each line receiver appends the line number (four bits) and any error flags (two bits—parity error, overrun error) to the character prior to placing it in the receiver storage buffer.

The DV11 microprocessor removes characters from the silo along with their line number and error flags. If there is an error flag (as a result of the parity error or overrun error detected by the receiver) the character placed in a UNIBUS-addressable register called the Receiver Interrupt Character Register and an interrupt request is generated.

If there is no error flag, the DV11 processing depends on whether a character-oriented protocol (example: BISYNC) or a byte-count-oriented protocol (example: DDCMP) is being used.

Character-Oriented Protocol Reception (Example: BISYNC)

If there is no error flag, the microprocessor affixes three mode bits at the high-order end of the received 8-bit character. This 11-bit character is then used as an offset in the PDP-11 control table to obtain a control byte that will indicate to the microprocessor what mode is to be used for subsequent reception on this line and any special handling information appropriate to this character (such as whether or not to generate an interrupt, whether or not to include the character in a block-check computation, whether or not to store the character in a PDP-11 core message buffer.)

If the generation of an interrupt is indicated, the character and the line number are moved to the Receiver Interrupt Character Register along with an error bit code. The error bit code indicates that this interrupt is being generated because a control table control byte has indicated that this is a special character.

If the control byte indicates that this character should be included in a block check, the DV11 microprocessor performs the appropriate calculation (LRC, CRC-16, or CRC/CCITT).

If the control byte directs that a received character be discarded, the character is discarded. If it indicates that the character be stored, the DV11 microprocessor

obtains the current address from a secondary register associated with this line and uses that address to store the received character in a message buffer. The DV11 microprocessor then increments the current address secondary register for that line. In addition, the DV11 microprocessor increments the byte count Secondary Register for that line. If the storage of the character caused the byte count to reach zero, the microprocessor checks to see whether a mode change has been requested. Such a change is indicated by the Byte Count Register being initially loaded with bit 15 cleared. The new mode is stored by the PDP-11 program in the high byte of the Line State Secondary Register in approximately the same format as a control byte. Having accomplished any actions requested in this pseudo control byte, a copy of the character is moved to the Receiver Interrupt Character Register along with the error bits that indicate that a new receive message buffer must be established for this line. In all cases where a character is moved to the Receive Interrupt Character Register, an interrupt is generated, and the DV11 microprocessor ceases to withdraw characters from the receiver silo storage buffer until the PDP-11 program indicates that such withdrawal can proceed again (by setting a bit in the DV11 System Control Register).

Byte-Count-Oriented Protocol Reception (Example: DDCMP)

If a byte-count-oriented protocol is used, Line Protocol Parameters bit 05 (DDCMP Receive) should be set by the PDP-11 program and the receiver mode should be set to 0. This will direct the DV11 microprocessor to skip the control byte process described above, include all characters in the Block Check Calculation, and store all characters (except BCC1 and BCC2). Details of character storage are the same as indicated above.

RECEIVER THROUGHPUT

The receiver throughput in the DV11 is dependent on the number of characters identified in the control bytes as being special (interrupt generating) and the size of the message buffers for received characters. It is intended that the ability of control bytes to accomplish reception mode changes relieves the necessity for received special characters generating an interrupt. When a receiver interrupt is generated, received characters are accumulated in a 128-character first-in/first-out (silo) storage buffer until the interrupt is handled. Assuming arrival of characters at a 19,200-character-per-second rate, it would take approximately 6.6 milliseconds for a silo overflow to occur. Thus, substantial worst-case interrupt latency can be accommodated.

In response to a receiver interrupt indication, the PDP-11 program should set the System Control Register (bit 08) indicating that the DV11 microprocessor may resume processing the character in the Receiver Interrupt Character Register and resume withdrawing characters from the receive silo storage buffer.

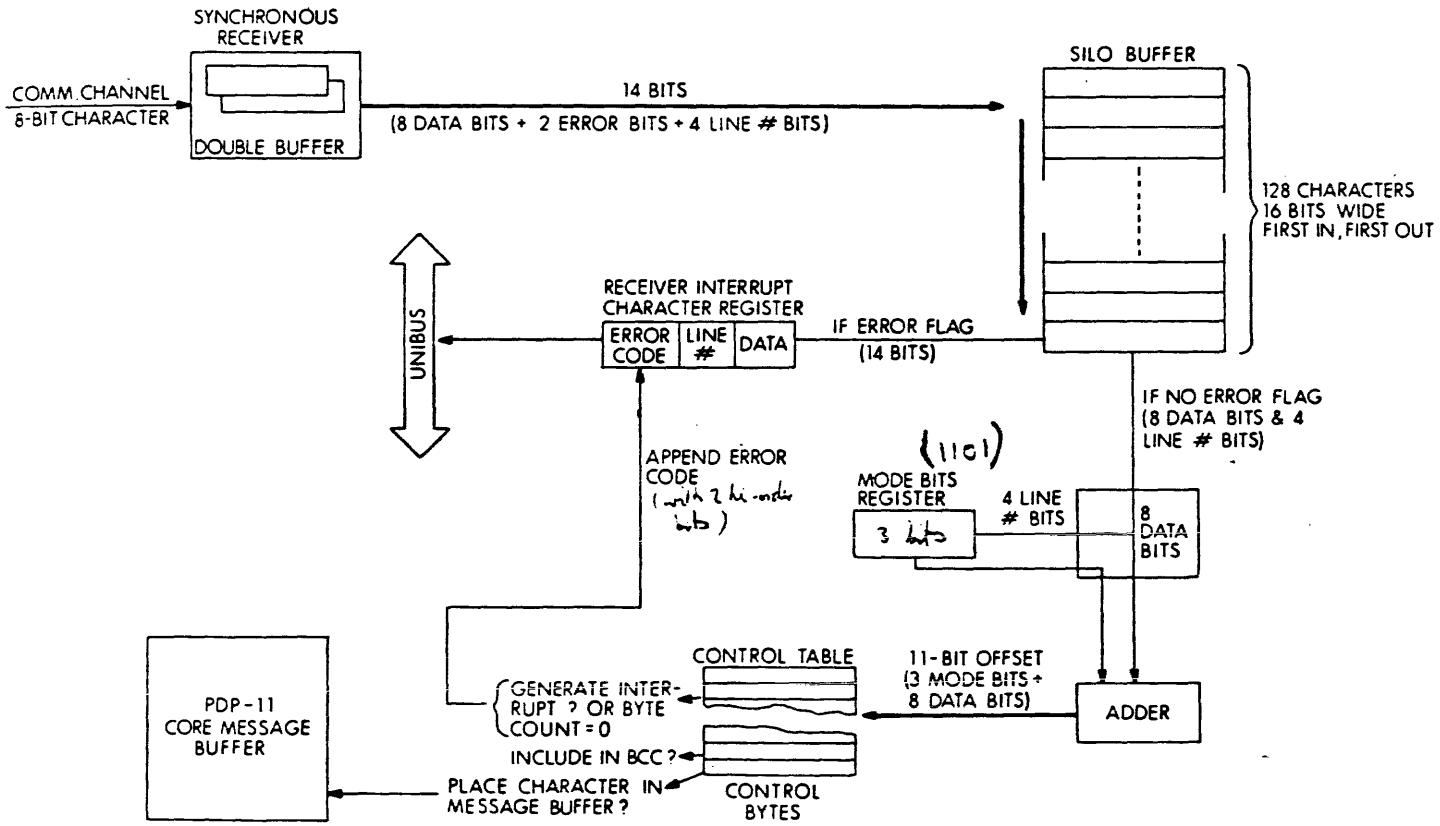


Figure 2. Reception

If the program so desires, it may alter the receiver control byte stored in the Receiver Control Byte Storage Register before setting bit 08 in the System Control Register.

TRANSMISSION OPERATION (Figure 3)

For each line there is a double-buffered serial transmitter. Whenever the transmitter buffer is empty, a flag is raised. The microprocessor scans for transmitter flags and when it finds one, it checks a "worksheet" to determine whether any special action must be taken (e.g., send a block check character). If no special action is required, the microprocessor checks to see if the transmitter "GO" bit for the line is set. If it is set, the microprocessor uses the transmitter current address register to perform an NPR transfer and obtain—from a core message buffer—a character to be transmitted. The DV11 processing of this character depends on whether a Character-Oriented Protocol (example: BISYNC) or a Byte-Count-Oriented Protocol (example: DDCMP) is being used.

Character-Oriented Protocol Transmission (Example: BISYNC)

Before transmitting the character, the microprocessor copies it, adds mode bits to the high-order end and performs an NPR to obtain a transmit control byte from a control table. This byte contains information indicating what new modes are to be used, whether to include the character in the block check, and whether to prefix the transmission of the character with a DLE (performed by microprocessor).

Byte-Count-Oriented Protocol Transmission (Example: DDCMP)

If a byte-count-oriented protocol is used, Line Protocol parameters bit 06 (DDCMP Transmit) should be set by the PDP-11 program and the transmitter mode should be set to 0. This will direct the DV11 microprocessor to skip the control byte process described above and include all characters in the Block Check Calculation. The characters are transmitted as described below.

Transmission of Characters

The microprocessor then loads the character to be transmitted into the appropriate line transmitter and increments the byte count. It then checks the byte count to determine whether it has reached zero. If it has, a check is made to determine whether a mode change has been requested. (Such a change is indicated by the byte count register being initially loaded with bit 15 cleared). The new mode is stored by the PDP-11 program in the high byte of the Line Progress Secondary Register in approximately the same format as the control byte. Having accomplished any actions requested in this pseudo control byte, the microprocessor will switch to the other set of tables (i.e., from principal to alternate or vice versa). If the byte count that is just exhausted did not request a mode change via bit 15 on the Byte Count Register, the microprocessor will switch from principal to alternate (or vice versa) without reference to the upper byte of the Line Progress Secondary Register.

If, after the switch in registers, the microprocessor finds the new byte count is also zero, it will clear "Transmit Go" in the Line State Register and idle sync (or ones), depending on the setting of the "Idle Mark" bit in the Line Protocol Parameters Register.

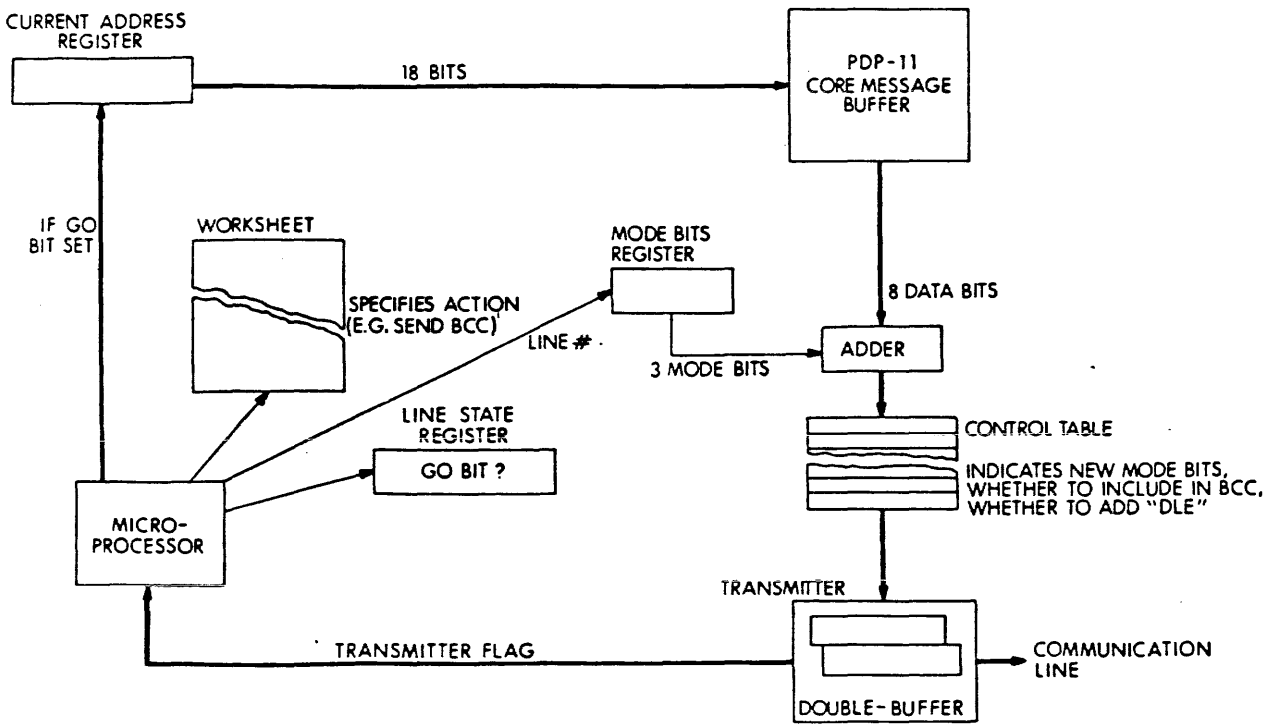
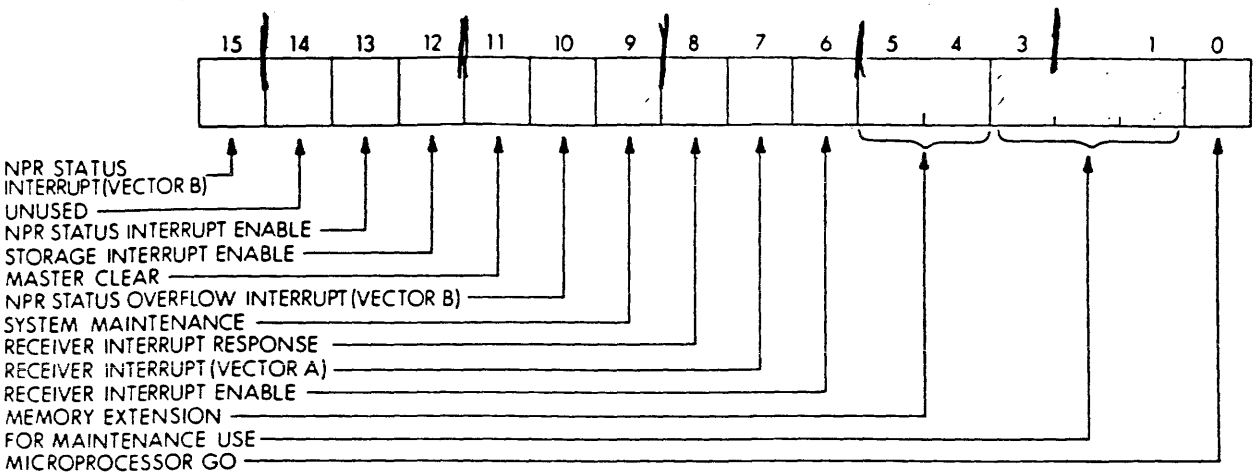


Figure 3. Transmission

SYSTEM CONTROL REGISTER (SCR)–ADDRESS 775000 (775040, 775100, 775140)

The System Control Register is a byte-addressable register. The bit assignment is as follows:



Bits	Description
00	Microprocessor Go

This bit when set, permits the DV11 to operate the microprocessor that controls the DV11. This is read/write, CLEARED by Initialize. System programs must set this bit for the DV11 to function.

01 (For Maintenance Use)

Do not write one's here

02 (For Maintenance Use)

Do not write one's here

03 (For Maintenance Use)

Do not write one's here

04-05 Memory Extension

For the line number entered in bits 00-03 of the Secondary Register Selection Register, the information stored in these bits becomes bits 16 and 17, respectively, of any current address or control table base address loaded by the program into the RAM. These bits are read/write (cleared by Initialize) but when read, represent only the status of bits 4 and 5 of the System Control Register, not the status of address bits 16 and 17 of the selected line. See the Line Control Register for further information. This arrangement permits interrupt service routines to save the contents of the System Control Register accurately.

06 Receiver Interrupt Enable

This bit, when set, permits the setting of bit 7 to generate an interrupt request. This bit is read/write, and is cleared by Initialize.

07 Receiver Interrupt (Vector A)

This bit, when set, indicates that the microprocessor has either (1) withdrawn a byte from a core control table indicating that an interrupt should be generated for the character presently being processed, or (2) the character presently being processed has one or more of its associated error flags set or (3) experienced a zero byte count, non-existent memory location, or memory parity error in processing this character. The program should respond to this interrupt by setting SCR08. (The program might wish to alter the control byte in the Receiver Control Byte Storage Register before setting SCR08.) This bit is read-only, except when SCR09 is set. It is cleared by Initialize.

08 Receiver Interrupt Response Completed

The setting of this bit clears SCR07 and allows the microprocessor to take action on the character in the RICR (according to the information stored in the Receiver Control Byte Storage Register) and to continue removing characters from the receive silo for processing.

09 For Maintenance Use

This bit, when set, permits the program to write bits 7 and 15 of this register. This bit is read/write and is cleared by Initialize. This register must be word-addressed when and while this bit is set.

10 NPR Status Overflow Interrupt (Vector B)

This bit, when set, indicates that the DV11 hardware checked the NPR Status Register (a 64-entry silo) and and found that there was no room for the entry due to insufficient program attention to servicing this register. All DV11 transmitter action in performing NPR transfers will cease until this condition is corrected. This bit is read/write and is cleared by Initialize.

11 Master Clear

This bit, when set, generates "Initialize" within the DV11 data handling sections. (It does not affect the modem control.) The silos (both received character and NPR status*) are cleared. The secondary registers are not cleared. This bit is write-only (reads as zero, as it is self-clearing).

12 Storage Interrupt Enable

This bit, when set, permits the setting of bit 10 to generate an interrupt request. This bit is read/write and is cleared by Initialize.

13 NPR Status Interrupt Enable

This bit, when set, permits the setting of bit 15 to generate an interrupt request. This bit is read/write and is cleared by Initialize.

14 Unused

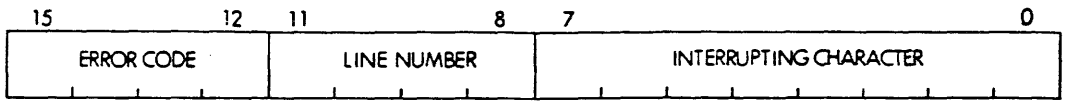
15 NPR Status Interrupt (Vector B)

This bit is set whenever there are one or more entries in the NPR Status Register, which is a silo-type register. The reading of that read-once register clears this bit, but it resets again if a new entry moves down into the register to replace the previously read entry. This bit is read-only except when SCR bit 09 is set, when it is read/write. This bit is cleared by Initialize.

*The NPR Status Register, bit 15 ("Entry Present"), is cleared by Initialize; the other bits are not.

RECEIVER INTERRUPT CHARACTER REGISTER (RICR)–ADDRESS 775002 (775042, 775102, 775142)

This register is read-only and is cleared by Initialize.



Bits Description

00-07 Interrupting character

These bits contain the interrupting character, right-justified. The least significant bit is bit 00. On parity-equipped characters, less than eight bits, the parity bit will appear immediately to the left of the highest-order bit in the character. See special note associated with Error Code 0101 below.

08-11 Line Number

These bits indicate the line number on which the interrupting character was received. Bit 8 is the least significant bit.

12-15 Error Code

These bits indicate the reason that the character shown in bits 00-07 generated an Interrupt request.

Error Code Bits				Meaning
15	14	13	12	
0	0	0	0	SPECIAL CHARACTER The receipt of this character caused the seizure of a control byte which had bit 00 (generate interrupt) set indicating that this is a special character.
0	0	0	1	PARITY ERROR This character was received with a parity sense opposite to that selected for this line by the parity sense switches on the line card.
0	0	1	0	OVERRUN The character(s) preceding this character on this line has (have) been lost due to failure of the DV11 receiver system to keep up with the incoming character rate on this line.
0	0	1	1	PARITY ERROR AND OVERRUN (see previous listings)
0	1	0	0	BYTE COUNT WARNING This character has been stored, but it is the last character that can be stored for this line as the byte count is now zero for reception on this line.
0	1	0	1	BLOCK CHECK COMPLETED A block of text or data and the associated block check characters have been received and the program should now check the accumulated receiver block check; the DV11 presents the OR of the high and low bytes of that register in bits 00-07 of this register.

Error Code Bits				Meaning
0	1	1	0	UNDEFINED
0	1	1	1	UNDEFINED
1	0	0	0	BYTE COUNT ZERO This character was not stored, as the byte count for reception on this line is zero and thus there is no place to store this character.
1	0	0	1	UNDEFINED
1	0	1	0	UNDEFINED
1	0	1	1	UNDEFINED
1	1	0	0	PROCESSING ERROR 00 A nonexistent memory time-out occurred when the DV11 attempted to store this character.
1	1	0	1	PROCESSING ERROR 01 A nonexistent memory time-out occurred when the DV11 attempted to obtain the control byte associated with this character.
1	1	1	0	PROCESSING ERROR 10 A memory parity error occurred when the DV11 attempted to store this character. (NOTE: this error should never occur, as the memory parity logic gives alarms only on DATO transfers).
1	1	1	1	PROCESSING ERROR 11 A memory parity error occurred when the DV11 attempted to obtain the control byte associated with this character.

In response to a receiver interrupt (SCR07), the PDP-11 Program should examine this register (Receiver Interrupt Character Register), make any desired changes in the Receiver Control Byte Storage Register, and then set SCR08.

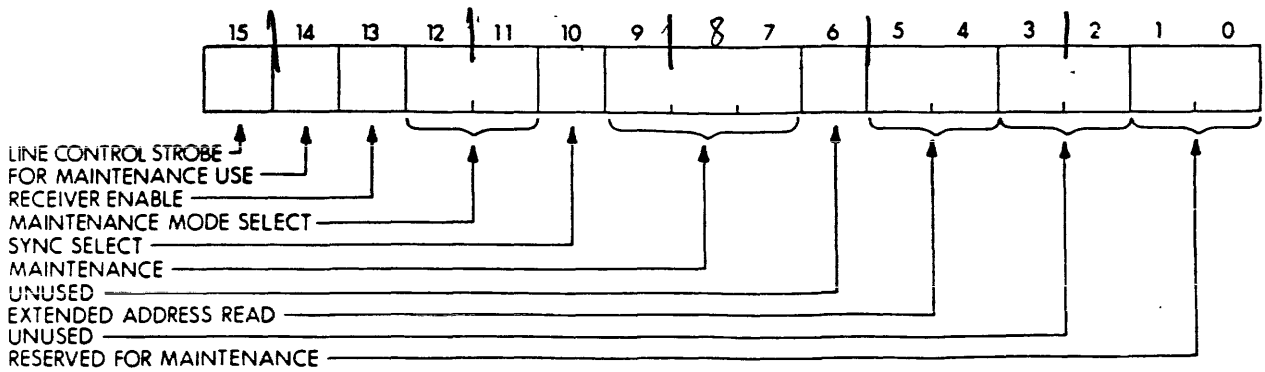
In the case of code 0000, Special Character, the Receiver Control Byte Storage Register will contain the control byte associated with the Special Character, but with its bit 00 (generate interrupt) cleared to zero. Thus, for those characters where an interrupt is desired merely to advise the program of reception of a particular character, the program will typically wish to set SCR08 without changing the contents of the Receiver Control Byte Storage Register. For all other error codes, the microprocessor creates a special "remain in mode specified by last control byte fetched for this line, do not include in BCC, do not expect BCC1 next, do not store, do not interrupt" control byte and stores that in the Receiver Control Byte Storage Register before initiating a receiver interrupt request. Thus, for those characters or conditions specifying occurrence of an error, the PDP-11 program can dispose of the character by merely setting SCR08. If desired, the Receiver Control Byte Storage Register may be changed before SCR08 is set.

LINE CONTROL REGISTER (LCR)–ADDRESS 775004 (775044, 775104, 775144)

This register controls the maintenance features associated with each line in the DV11 and provides an opportunity for the PDP-11 program to read the extended address bits for each line. This register is word-addressable only.

Bits indicated to be "write-only" will be read back in the state they were last set. Since this is not a presentation of the corresponding bit for the selected line, the bit is referred to as "write-only."

The bit functional assignments are as follows:



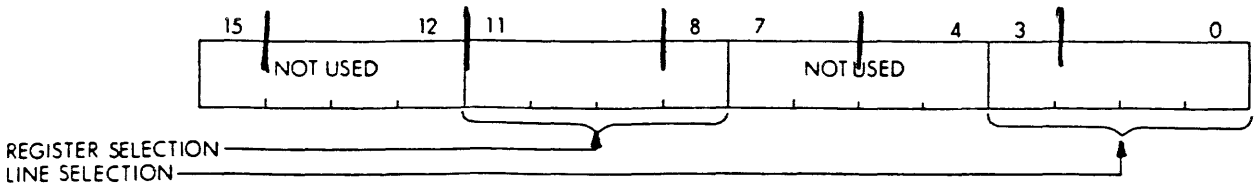
Bits	Description
00-01	Reserved for Maintenance (CAUTION: Various bits may appear here during normal DV11 operation.)
02-03	Unused
04-05	Extended Address Read (Read-Only) For the line number entered in bits 00-03 of the Secondary Register Selection Register, these bits represent the status of bits 16 and 17 of the secondary register specified by bits 08-11 of the Secondary Register Selection Register. This permits the PDP-11 program to read the Extended Address bits of the Current Address and Control Table Base Address entries in the RAM.
06	Unused
07	Maintenance (Read-Only) (CAUTION: Various bits may appear here during normal DV11 operation.)
08	Maintenance
09	Maintenance (See bit 15)
10	Sync Select (See bit 15) Each four-line group of the DV11 (0-3, 4-7, 8-11, 12-15) has associated with it two switch-selectable sync/fill characters referred to as Sync A and Sync B. For each individual line in that group (as entered in bits 00-03 of the Secondary Register Selection Register), the setting of this bit determines whether Sync A (bit=0) or Sync B (bit=1) is used. This bit is write-only and is cleared by initialize.
11-12	Maintenance Mode Select (Maintenance) (See bit 15) Bits 11 and 12 are write-only and are cleared by Initialize. Normal operating mode is 00.
13	Receiver Enable (See bit 15) When this bit is set by the program, a sync search is initiated on this line by the receiver logic. After an initialize, this bit must be set by the program before any reception can begin on this line (i.e., Receiver Active (See "Line State" secondary register) will not set unless this bit has been set). A switch for each line determines whether the receiver searches for one sync character or for two in a row. A successful sync search results in the setting of Receiver Active (Line State bit 00) for this line. This bit is write-only and is cleared by Initialize. NOTE Should it be desired to resynchronize during the course of reception, the program could accomplish this by setting "Receiver Resynchronize" (Line State 01). To shut down reception on a line, the program should clear Receiver Enable and then set Receiver Resynchronize.
14	Maintenance (See bit 15)
15	Line Control Strobe The setting of this bit records the status of bits 09, 10, 11, 12, 13, and 14 into the per-line status flip-flops associated with the line specified in bits 00-03 of the Secondary Register Selection Register. This bit is self-clearing, thus write-only. It may be set at the same time as the bits whose status it records, as its action is delayed until the conclusion of the instruction cycle which set it and the proper phasing of the DV11 internal clocks. This bit is necessary due to "reads" in the PDP-11/20 being "read/write" cycles and certain synchronization requirements associated with mode changes during clocking pulses. The bits marked "Maintenance" should be written to zero for normal DV11 use.

SECONDARY REGISTER SELECTION REGISTER–ADDRESS 775006 (775046, 775106, 775146)

The bits in this register provide a path for the program to access the various locations in the DV11 RAM. The PDP-11 program can read or write these locations. The various locations can be considered as indirectly addressable registers.

Interrupts must be inhibited or the contents of this register saved between the setting of bits in this register and the reading or writing of the Secondary Register Access Register–Address X10. This register is byte-addressable.

The bit assignments of the Secondary Register Selection Register are as follows:



Bits	Description
00-03	Line Selection

For each type of register selected by bits 08-11 below, there are 16 registers, one per line. The setting of the Line Selection Bits determines exactly which of these line registers is to be addressed. The Line Selection Bits are also used to select the line to which the bits in the Line Control Register (X04) apply.

04-07 Unused

08-11 Register Selection

These bits determine which type of register is addressed for the line number specified in bits 00-03.

Bits				Register
11	10	09	08	
0	0	0	0	Transmitter Principal Current Address Register
0	0	0	1	Transmitter Principal Byte Count Register
0	0	1	0	Transmitter Alternate Current Address Register
0	0	1	1	Transmitter Alternate Byte Count Register
0	1	0	0	Receiver Current Address Register
0	1	0	1	Receiver Byte Count Register
0	1	1	0	Transmitter Accumulated Block Check Register
0	1	1	1	Receiver Accumulated Block Check Register
1	0	0	0	Transmitter Control Table Base Address Register
1	0	0	1	Receiver Control Table Base Address Register
1	0	1	0	Line Protocol Parameters Register
1	0	1	1	Line State Register
1	1	0	0	Transmitter Mode Bits Register
1	1	0	1	Receiver Mode Bits Register
1	1	1	0	Line Progress Register
1	1	1	1	Receiver Control Byte Storage Register

SECONDARY REGISTER ACCESS REGISTER–ADDRESS 775010 (775050, 775110, 775150)

This register should be loaded or read only after the appropriate bits of the Secondary Register Selection Register have been conditioned to select the type of register and line number within that type. Since this register is essentially a "window" through which the program may access a large number of other registers, no specific bit assignment may be given. See the individual register bit assignment listings. A list of the registers accessible through this register follows. This register is word-addressable only.

These registers are not cleared by Initialize. The PDP-11 program must clear all of these registers before setting SCR00 (microprocessor go).

Code	Register
0000	Transmitter Principal Current Address Secondary Register

This register contains 18-bit entries that will indicate, for each line's transmitter hardware, where in a core memory message table to obtain the next character to load into the synchronous transmitter unit associated with that line. Two additional bits are initially loaded from bits 04 and 05 of the System Control Register (X00), permitting 18-bit addressing capability.

When the byte count associated with this current address reaches zero, an entry will be made in the NPR Status Silo and transmission will continue using the Transmitter Alternate Current Address, provided that the "Transmitter Go" bit in the Line State Secondary Register for this line is still set.

Code Register

0001 Transmitter Principal Byte Count Secondary Register

This register contains a 15-bit word that is the two's complement of the number of bytes (characters) remaining to be transmitted on this line. The 16th bit (bit 15) is used to indicate, when loaded clear, that the high byte of the Line Progress Register will control further action on this line when the principal byte count reaches zero. When a simple change to alternate byte count is desired, bit 15 should be set to one.

0010 Transmitter Alternate Current Address Secondary Register

This register has exactly the same function as the Transmitter Principal Current Address Secondary Register described above.

When the byte count associated with this current address reaches zero, an entry will be made in the NPR Status Silo and transmission will continue using the Transmitter Principal Current Address, provided the "Transmitter Go" bit in the Line State Secondary Register for this line is still set.

0011 Transmitter Alternate Byte Count Secondary Register

This register contains a 15-bit word that is the two's complement of the number of bytes (characters) remaining to be transmitted on this line. The 16th bit (bit 15) is used to indicate, when loaded clear, that the high byte of the Line Progress Register will control action on this line when the alternate byte count reaches zero. When a simple change to principal byte count is desired, bit 15 should be set to one.

NOTE

The program can tell the DV11 whether to start from principal or alternate tables by loading the appropriate bits in the Line State Secondary Register.

0100 Receiver Current Address Secondary Register

This register contains 18-bit entries that will indicate, for each line's receiver hardware, where in a core memory message table to store the next character received on this line. Two additional bits are initially loaded from bits 04 and 05 of the System Control Register (X00).

0101 Receiver Byte Count Secondary Register

This register contains a 15-bit word that is the two's complement of the number of bytes (characters) remaining to be received on this line. The 16th bit (bit 15) is used to indicate, when loaded clear, that the high byte of the Line State Register will control action on this line when the receiver byte count reaches zero.

When the in-core message table for reception on this line has been filled with received characters, the byte count will have been up-counted to zero. An entry will then be made in the Receiver Interrupt Character Register, a receiver interrupt request will be generated, and the action of the microprocessor in retrieving characters from the received character storage silo will stop. Refer to Receiver Interrupt Character Register error code 1000 for further details.

0110 Transmitter Accumulated Block Check Secondary Register

This register contains an up-to-date calculation of the block check character associated with transmission on each line. The type of polynomial used for each line is specified in the Line Protocol Parameters Secondary Register (1010). Characters to be included are specified by bit 03 of the control bytes obtained from the core transmission control tables during the NPR transmission of characters on this line if a character-oriented protocol such as BISYNC is being used. If a byte-count-oriented protocol such as DDCMP is being used and the transmitter mode is 0, all characters are included. The contents of this register may be checked at any time by the program. The program may also write into this register; this register can be cleared by writing zeroes into it. (The microprocessor will do this automatically when the BCC is transmitted). The contents of this register are sent out over the line as two 8-bit bytes (low order 8 bits first), except if LRC-8 is the selected protocol, in which case only one byte is sent.

NOTE

The DV11 calculates CRC-16 and CRC-CCITT on a byte-at-a-time basis (parallel); thus the character length must be eight bits if these block checks are to be used. LRC may be used for shorter characters.

Code Register

0111 Receiver Accumulated Block Check Secondary Register

This register contains an up-to-date calculation of the block check character associated with reception on each line. The type of polynomial used for each line is specified in the Line Protocol Parameters Secondary Register (1010). Characters to be included are specified by bit 03 of control bytes withdrawn from the receiver control byte tables if a character-oriented protocol, such as BISYNC, is being used. If a byte-count-oriented protocol, such as DDCMP, is being used and the receiver mode is 0, all characters (except leading syncs which can be stripped) are included. The contents of this register may be checked at any time by the program. The program may also write into this register; this register can be cleared by writing zeroes into it. The program must do this after it has checked the block check at the end of the message as the microprocessor does not do this. (This would only be necessary if the block check were not zero—an error condition in most protocols).

1000 Transmitter Control Table Base Address Secondary Register

This register contains an 18-bit word that indicates the starting address of the transmitter control table for this line. Extended address bits are initially loaded from bits 04 and 05 of the System Control Register (SCR). This address will have the character to be transmitted (with higher order mode bits appended) added to it by the transmitter hardware to obtain a byte address to which the NPR control hardware will go to obtain a control byte. The control byte will instruct the DV11 transmitter what to do with this particular character—whether to include it in the BCC, etc. If all lines in the DV11 are using the same protocol, the program could set all 16 Transmitter Control Table Base Addresses to the same value. In addition, if the protocol permits, the same base addresses could be used for both the transmit control table and for the receive control table.

1001 Receiver Control Table Base Address Secondary Register

1010 Line Protocol Parameters Register

This register contains information concerning the protocol to be executed on this line. This register must be initially loaded by the PDP-11 program before reception or transmission begins on this line. The bit assignments are as follows:

Bits	Function
00	Idle Mark on Both Byte Counts Zero

When this bit is set, the microprocessor will condition the synchronous transmitter on this line to idle MARK when both byte counts reach zero. If the bit is not set, SYNC will be idled. It is anticipated that this feature will be used in half-duplex systems wherein the PDP-11 program will set this bit immediately after loading the last byte count.

01 Strip Leading Sync

When this bit is set, all sync characters received between the time a line goes "active" and the time the first non-sync character arrives will be automatically stripped from the received message. Once a non-sync arrives, this feature is disabled until the line is resynchronized by the issuance of a Receiver Resynchronize command (see Line State Register, bit 01).

02 Reserved (1011)

03-04 Block Check Type

These bits are conditioned by the PDP-11 program to indicate what type of block check calculation is to be done for transmissions and receptions on this line.

04	03	
0	0	LRC-8 (XOR)
0	1	CRC-16 ($X^{16} + X^{15} + X^2 + 1$)
1	0	Unused-16
1	1	CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$)

05 DDCMP Receive

If this bit is set and reception is in mode 0, the received character will be processed without reference to a control byte. A control byte calling an inclusion of all characters in the BCC and storage of all characters (excluding syncs stripped by bit 01 above) will be assumed. This bit is intended for use with byte-count-oriented protocols.

06 DDCMP Transmit

If this bit is set and transmission is in mode 0, the transmitted character will be processed without reference to a control byte. A control byte calling for inclusion of all characters in the BCC will be assumed. This bit is intended for use with byte-count-oriented protocols.

07 Reserved

Code	Register
	Bits Function
	08-15 Data Link Escape Character

In the process of transmitting on a line, the microprocessor fetches control bytes from core indicating what special action, if any, is applicable to the transmission of that character on that line. One of the possibilities is the necessity of transmitting a Data Link Escape Character before transmitting the actual character. The Data Link Escape Character used is retrieved by the microprocessor from the high byte of this secondary register.

1011 Line State Register

This register is a scorecard with which the microprocessor keeps track of what it is doing with respect to the special actions required of it in executing various line protocols. The bit assignments are as follows:

Bits	Function
00	Receiver Active (set and cleared by microprocessor). This bit is set when an enabled line (LPR 12 set) has satisfied the synchronization conditions. This bit is cleared when the microprocessor finds Line State bit 01 "Receiver Resynchronize" set.
01	Receiver Resynchronize (set by PDP-11 program and cleared by microprocessor). This bit is set when the PDP-11 program desires to resynchronize a line or when it has cleared LPR 13 and is turning off reception on a line. The microprocessor upon finding this bit set will clear Receiver Active, clear this bit, send a resync pulse to the Synchronous Receiver for this line, and will insert a special flag character into the silo. It will also set bit 07 of the Line Progress Secondary Register to indicate that the special resynchronization character is in the silo. (sic)
02	Transmitter Go (set by PDP-11 program and cleared by microprocessor). The PDP-11 program will set this bit whenever it has prepared a message for transmission and desires that the DV11 transmit it. The microprocessor will clear this bit whenever Transmitter NXM sets, Transmitter MPE sets, or both byte counts associated with this line are zero. The PDP-11 program may clear this bit if it is desired that a transmission be aborted.
03	Transmitter Underrun (set by microprocessor and cleared by PDP-11 program). This bit is set if the microprocessor finds, upon loading a character for transmission, that a synchronous transmitter is exhibiting a "Data Not Available" flag. The setting of this bit does not generate an interrupt or clear any other bit; it is for the programmer's information only. When the bit has been read by the program, the program should clear it.
04	Transmitter NXM (set by microprocessor and cleared by PDP-11 program). This bit sets whenever a microprocessor transmitter service routine encounters an NXM condition. The PDP-11 program should empty the NPR Status Silo and then clear this bit. The setting of this bit clears Transmitter Go.
05	Transmitter MPE (same description as Transmitter NXM, but a Memory Parity Error occurred rather than an NXM).
06	Sync Strip On (set and cleared by microprocessor). This bit sets whenever Receiver Active sets on a line whose Line Protocol Parameters bit 01 (Strip Leading Sync) is set. This bit clears whenever the first non-SYNC character arrives on that line. This bit is for use by the microprocessor only.
07	Use Alternate Tables (set and cleared by microprocessor or by PDP-11 program). Before setting Transmitter Go, the PDP-11 program should condition this bit to indicate to the microprocessor whether to start the transmission from the principal or from the alternate tables. When a byte count runs out, the microprocessor will switch to the other current address and byte count. If the other byte count is also zero, this bit will remain in that second state and "go" will be cleared.
08-09	Unused.
10	Expect BCC1 Next on Byte Count Run-out. The PDP-11 program may load this bit to indicate to the DV11 that it should expect the first eight bits of the block check character when a "marked" reception byte count reaches zero. When the DV11 processes the last character and the "marked" byte count thus reaches zero, the microprocessor will set Line Progress Register bit 05 to tell the DV11 logic that the BCC is next. This information will be used when the DV11 services the next character that arrives on this line.
11-12	Unused.
13-15	Receiver Next Mode on Byte Count Run-out. The PDP-11 program may load these bits with the receiver mode to which it desires the DV11 hardware to go when a "marked" reception byte count reaches zero.

Code Register

1100 Transmitter Mode Bits Register

This register contains three bits (00-02) which indicate the "mode" of transmission on this line. These three bits determine which of the up to eight possible control tables will be used for transmission on this line. The transmitter logic appends these bits onto the high-order end of a copy of the character to be transmitted and uses the resulting 11-bit character as an offset from the transmitter control table base address to obtain a control byte from core. The control byte contains special instructions with regard to the character that is about to be transmitted.

1101 Receiver Mode Bits Register

This register contains three bits (00-02) which indicate the "mode" of reception on this line. Specifically, these bits determine which of the up to eight possible control tables will be used for reception on this line. Refer to the section entitled "Control Tables."

1110 Line Progress Register

The bit assignments for the Line Progress Secondary Register are as follows:

Bits	Function
00	Send BCC1 Next This bit is set by the microprocessor when it runs out a "marked" transmission byte count (bit 15 loaded as zero) (typical use: DDCMP) or encounters a transmitter control byte with bit 02 (send BCC next) set, typically ITB, ETB, or ETX in BISYNC. It is cleared by the microprocessor when LRC is the selected block check and has been loaded for transmission, or when the BCC1 has been loaded for transmission.
01	Send BCC2 Next This bit is set by the microprocessor when the BCC1 has been loaded for transmission. This bit is cleared by the microprocessor when the BCC2 is loaded for transmission.
02	DLE Sending In Progress (Data Link Escape Char.) This bit is set by the microprocessor when it has just loaded a DLE for transmission in response to seizure of a control byte that says to prefix a DLE. This bit is used by the microprocessor to prevent stuffing DLE characters continuously. This bit is cleared by the microprocessor when the DLE has been sent.
03-04	Unused.
05	Expect BCC1 Next This bit is set by the microprocessor when it runs out a "marked" reception byte count (bit 15 loaded as zero) (typical use: DDCMP) or encounters a receiver control byte with bit 02 (expect BCC next) set, typically ITB, ETB, or ETX in BISYNC. This bit is cleared by the microprocessor when LRC is the selected block check and has been received, or when the BCC1 has been received.
06	Expect BCC2 Next This bit is set by the microprocessor when the BCC1 has been received. This bit is cleared by the microprocessor when the BCC2 has been received.
07	Resynchronization Flag Character Not Found (set and cleared by microprocessor). This bit is set when the microprocessor processes a resynchronization request for this line. It is cleared when the microprocessor finds the flag character that it inserted in the silo at the time that resynchronization was requested. Characters retrieved from the silo for this line while this bit is set are discarded.
08-09	Unused.
10	Send BCC1 Next on Marked Byte Count Run-out The PDP-11 program may load this bit to indicate to the DV11 that it should send the first eight bits of the block check character when a "marked" transmitter byte count reaches zero. If this bit is set, the microprocessor in the DV11 will, upon reaching zero, set Line Progress Register bit 00 (see above).
11-12	Unused.
13-15	Transmitter Next Mode on Marked Byte Count Run-out The PDP-11 program may load these bits with the transmitter mode to which it desires the DV11 hardware to go when a "marked" transmitter byte count reaches zero.

Code	Register
1111	Receiver Control Byte Storage Register

This register contains a copy of the control byte fetched from the receiver control table by the DV11. When a control byte is fetched that has bit 00 (generate interrupt) set, a copy of that control byte (but with bit 00 cleared) is stored here; the interrupt causing character and its line number are moved to the Receiver Interrupt Character Register; and an interrupt request is generated. The PDP-11 program may merely take note of the arrival of this character and set System Control Register bit 08 to direct the microprocessor to resume processing the character. The microprocessor will use this copy of the control byte for that processing. The PDP-11 program can alter the contents of this register before setting SCR08 if it desires to change the character processing from that originally dictated by the control byte.

In the case of receiver interrupts generated by causes other than the fetching of a control byte with bit 00 (generate interrupt) set, a special control byte arranged for character discard, no BCC inclusion, no BCC expectation, and same mode as control byte last fetched for reception on this line, is placed in this register by the microprocessor before conditioning the Receiver Interrupt Character Register and generating the receiver interrupt request.

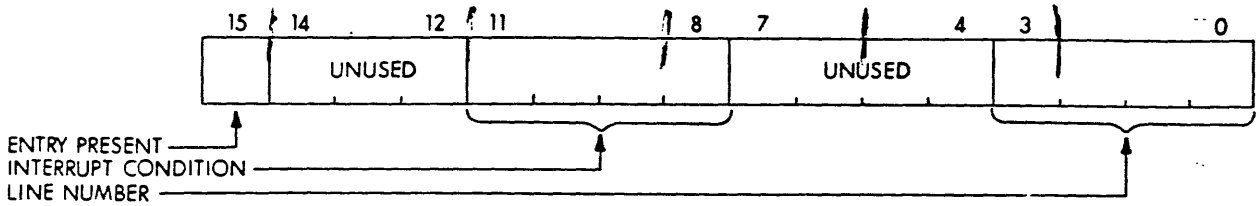
SPECIAL FUNCTIONS REGISTER–ADDRESS 775012 (775052, 775112, 775152)

Reserved for Maintenance. Various bits may appear here during normal operations. This register is word-addressable.

NPR STATUS REGISTER–ADDRESS 775014 (775054, 775114, 775154)

This register is a 64-entry silo-type register in that it is read once, and then a new entry "falls" into the register if additional "entries" exist at the time that the read of this register is completed.

This register reports various interrupt-causing conditions associated with the transmitter NPR hardware. Interrupt conditions related to various transmitter NPR operations are stacked in a first-in/first-out storage buffer along with the line number being serviced when this condition occurred. As soon as the program has finished reading this register once, a new entry is cycled into the register in place of the former entry. The interrupt is SCR 15 (NPR Status Interrupt). This register is read-only and is not cleared by Initialize, except for bit 15 which is cleared by Initialize.



Bits	Description
00-03	Line Number

These bits indicate which line was being serviced when the interrupt condition developed. The format of these bits is the same as bits 00-03 of the Secondary Register Selection Register (SRSR) so that the program can load these bits into the SRSR and read the appropriate current address or byte count.

04-07 Unused

08-11 Interrupt Condition

These bits indicate the type of interrupt condition which occurred. The hardware is designed so that simultaneous occurrences on the same line create separate entries (Example: nonexistent memory and byte count zero both occur).

Note that the condition codes are the addresses of the secondary registers which apply.

Code	Condition
0000	Transmitter Principal Current Address sent NPR hardware to a nonexistent memory location (NXM).
0001	Transmitter Principal Byte Count = 0.
0010	Transmitter Alternate Current Address sent NPR hardware to a nonexistent memory location.
0011	Transmitter Alternate Byte Count = 0.
1000	Transmitter Control Table Base Address–fetching control byte produced NXM or a memory parity error. The program should examine the Line State Secondary Register for further details.

12-14 Unused

15 Entry Present

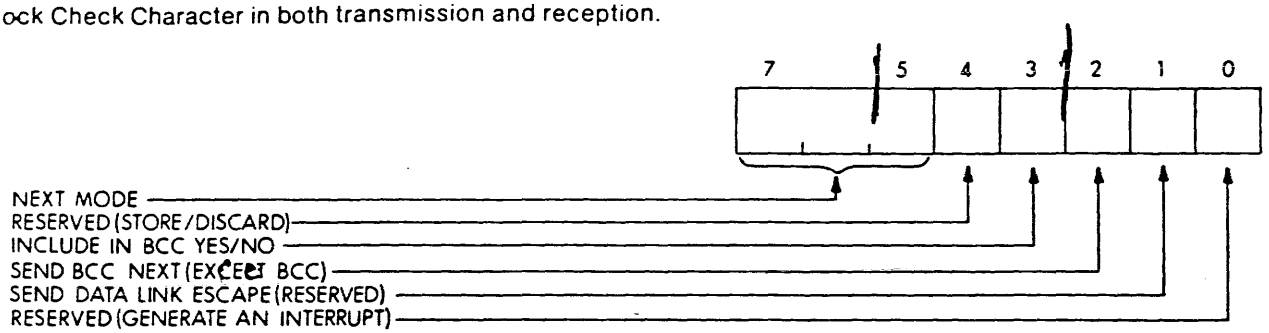
When set, this bit indicates that bits 00-11 contain a valid entry. Reading the register or generating Initialize clears this bit. It resets when another status report entry reaches the "bottom" of the silo and can be read in bits 00-11. Bits 00-11 are meaningless unless this bit (15) is set.

RESERVED REGISTER–ADDRESS 775016 (775056, 775116, 775156)

Bits	Function
00-15	Reserved; word-addressable

CONTROL BYTE FORMATS

The DV11 achieves its high throughput and generalized operating capabilities by having both the transmitter and the receiver character-handling apparatus perform NPR cycles. The NPR cycles access byte tables in PDP-11 core to determine the next step to take with regard to the particular character being processed. The bit assignments in the control bytes are arranged such that the same control bytes may be used for both transmission and reception if the communications protocol being used progresses from mode to mode in a symmetrical fashion on both transmit and receive and provided that the same characters would be included in the Block Check Character in both transmission and reception.

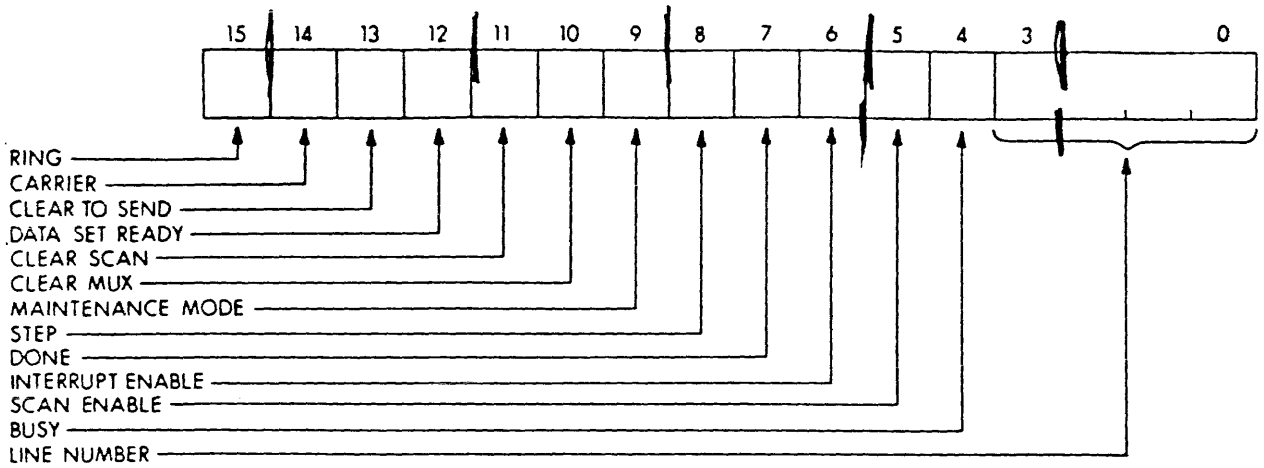


Bits	Transmitter Control Byte Function	Receiver Control Byte Function
05-07	Next Mode Determines next transmission mode used on this line.	Next Mode Determines next reception mode used on this line.
04	Reserved	Store/Discard Determines whether this character is stored in message table or is discarded.
03	Include in BCC Yes/No Determines whether or not this character will be included in the BCC being accumulated for this line.	Include in BCC Yes/No Determines whether or not this character will be included in the BCC being accumulated for this line.
02	Send BCC Next Tells transmitter logic to send the 16-bit BCC after the character presently being handled. (8-bit if LRC selected).	Expect BCC Next Tells receiver logic to expect the 16-bit BCC after the character presently being handled (8-bit if LRC selected).
01	Send Data Link Escape Next Tells transmitter logic to send Data Link Escape character from Secondary Register 1010 before sending the character presently being handled.	Reserved
00	Reserved	Generate an Interrupt The setting of this bit causes the character presently being processed to generate an interrupt. The microprocessor moves that character to the Receiver Interrupt Character Register and generates an interrupt request.

PROGRAMMABLE MODEM CONTROL DEVICE REGISTERS

The two programmable modem control device registers and their specific bit assignments are listed in the following paragraphs.

CONTROL STATUS REGISTER (CSR)–ADDRESS 775020 (775060, 775120, 775160)



Bits	Status	Description
00-03	LINE #	The LINE # bits are the binary addresses for the modem control's 16 lines (0-15) as follows:

Bit 3	2	1	0	Line
0	0	0	0	0
0	0	0	1	1
			•	•
			•	•
			•	•
1	1	1	1	15

If the Scan is cleared by INITIALIZE or CLR SCAN, the Line # Register will settle in 16μs ±10%. When settled, the Line # Register will be set to Line #0(0000).

NOTE

When the Scan is enabled (or STEP), the next line to be tested will always be Line # +1. These bits are Read/Write and are cleared by INITIALIZE and by CLR SCAN.

04 BUSY

BUSY provides a program indicator that is set to 1 when the Scan is cycling. This bit is particularly useful to determine when a CLR SCAN (bit 11) has completed the task of cycling 0's into the Scanner's memory elements.

In addition, this bit must be tested for 0 if SCAN ENABLE was turned off preparatory to changing the Line #.

In Interrupt Mode, this procedure guarantees that detected transitions are serviced before the Line # is changed. (If functioning with interrupts OFF, then DONE should be tested after BUSY is found to be 0.)

05 SCAN EN

The SCAN ENABLE flip-flop allows the scan to "free run," testing all lines sequentially if the DONE flip-flop is cleared.

When the SCAN EN flip-flop is set to 1 and DONE is 0, a ring counter is allowed to cycle in the following order (from Rest):

1. Increment line counter.
2. Store contents of memory (Line # Address) in the HOLD flip-flop.
3. Write current modem status into memory.
4. Compare HOLD and contents of memory for interrupt conditions.

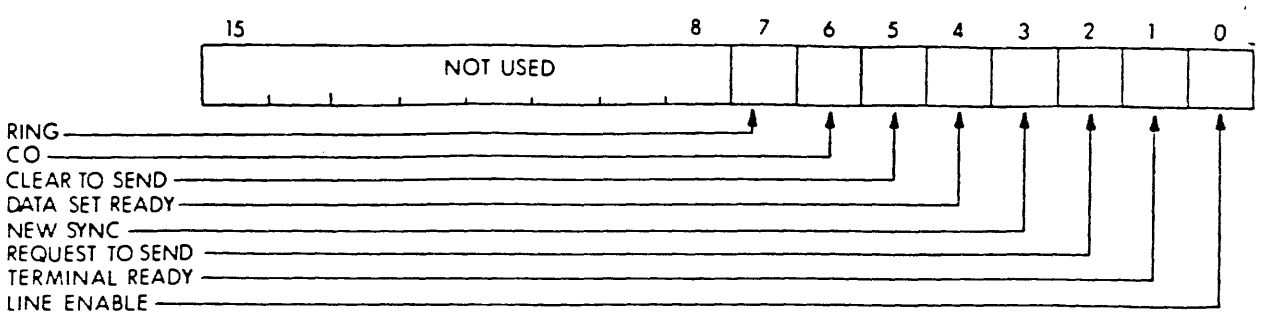
The ring counter continues to cycle (1 to 4) if DONE remains 0 and SCAN EN is set. If the SCAN EN flip-flop is negated while the ring counter is cycling (i.e., DONE not set) the ring counter will come to rest in 1.2μs ± 10%. The Line # Register must not be changed until BUSY (bit 04) is found to be 0. This bit is read/write and cleared by INITIALIZE and CLR SCAN.

INTER EN

If set to 1, Interrupt Enable allows DONE to cause an interrupt on priority four. This bit is read/write and cleared by INITIALIZE and CLR SCAN.

Bits	Status	Description
07	DONE	The DONE flag, when set to 1, indicates that the hardware Scan has detected a transition on CARRIER, SEC RX, CS, or the RING modem Status leads. Additionally, DONE freezes the SCAN which makes available to the programmer: 1. The Line # that caused the interrupt. 2. The state of the flags (four bits). 3. Modem Status (eight bits). This bit is read/write and cleared by INITIALIZE and CLR SCAN.
08	STEP	STEP, when set to 1, causes the Scan to increment the Line # and test that line for interrupts causing transitions. STEP can be used in place of SCAN EN, but care should be exercised that the Scan rate is great enough (milliseconds) so that double carrier transitions will be detected. Additionally, DONE does not inhibit STEP. A STEP requires 1.2μs $\pm$ 10% to execute. This bit is write 1's only.
09	MAINT MODE	When the MAINT MODE flip-flop is set to 1, it conditions the Scan Input (RING, CLEAR TO SEND, CARRIER, and SEC RX) to a 1 or ON state. Utilizing STEP or SCAN EN with MAINT MODE exercises 100 percent of the scan logic (not the data multiplexers). This includes the interrupt circuits and the address selector. This mode provides a diagnostic feature, as well as an on-line test facility for the modem control's interaction with the UNIBUS. This bit is read/write and is cleared by INITIALIZE and CLR SCAN.
10	CLEAR MUX	CLEAR MUX clears the REQUEST TO SEND, TERMINAL READY, SEC TX, and LINE EN flip-flops for all lines, when this bit is set to 1. This bit is write 1's only.
11	CLEAR SCAN	CLEAR SCAN clears all active functions (line #, SCAN EN, etc.) and the memory logic, when this bit is set to 1. The memory logic requires 18.8μs $\pm$ 10% to cycle a CLEAR through the memory locations. This function is especially useful if the programmer requires knowledge of the ON states of CARRIER, CLEAR TO SEND, RING and SEC RX. When the Scan is enabled (or STEP) following a CLR SCAN, an interrupt will occur for all ON states as they will appear (to the logic) as OFF-to-ON transitions.
12	DSR	The DATA SET READY flag is 1 if an ON-to-OFF or an OFF-to-ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is read-only and presents 0 when INITIALIZED or CLR SCAN.
13	CS	The CLEAR TO SEND flag is 1 if an ON-to-OFF or OFF-to-ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is read-only and presents 0 when INITIALIZED or CLR SCAN.
14	CO	The CARRIER flag is 1 if an ON-to-OFF or OFF-to-ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is read-only and presents 0 when INITIALIZED and CLR SCAN.
15	RING	The RING flag is 1 if an OFF-to-ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is read-only and presents 0 when INITIALIZED and CLR SCAN.

LINE STATUS REGISTER (LSR)–ADDRESS 775022 (775062, 775122, 775162)



Bits	Status	Description
00	LINE EN	The LINE ENABLE flip-flop, when asserted, enables RING, CO, CS, and SEC RX to be sampled (line status) by the program, and to be tested for transitions. This bit is read/write and is cleared by INITIALIZE and CLEAR MUX.
01	TERM RDY	Controls switching of the data communications equipment to the communication channel (via modem). Auto-Dial and Manual Call origination: Maintains the established call. Auto-Answer: Allows "handshaking" in response to a RING signal. This bit is read/write and is cleared by INITIALIZE and CLEAR MUX.
02	RS	When REQUEST TO SEND is set to 1, it conditions the modem for transmit if the communications channel has been established (switched network). This bit is read/write and is cleared by INITIALIZE and CLEAR MUX.
03	NS	The New Sync (201) flip-flop, when 1, presents a high to the New Sync lead. This bit is read/write and is cleared by INITIALIZE or CLEAR MUX.
04	DSR	When the state of the modem's Data Set Ready lead is a high, this bit is a 1. The DSR bit is inhibited when the LINE EN flip-flop is 0. This bit is read-only.
	CS	This bit reflects the current state of the modem CLEAR TO SEND lead. An ON indicates that the modem is ready to transmit data. This lead is most often the result of the REQUEST TO SEND lead. The CS bit is inhibited when the LINE EN flip-flop is 0. This bit is read-only.
06	CO	This bit reflects the current state of the modem carrier detect lead. An OFF indicates that the received signal is unsuitable for demodulation. The CO bit is inhibited when the LINE EN flip-flop is 0. This bit is read-only.
07	RING	Set to 1 whenever the ring line from the modem selected by bits 00-03 of the CSR is on, provided that the line enable bit for that modem has been set.

NOTE

The Line Status Register bits 04-07 are inhibited when LINE EN is 0.

SPECIFICATIONS

System Addresses

DV11 uses the same address space as the DM11-A. The first DV11 in a system would be at 775000; the next at 775040; then 775100; and finally, 775140. If there are DM11-A's in the system already, the first DV11 would be at 775040. The DV11 data handling and modem control use a total of ten registers.

Interrupt Vectors

Each DV11 requires three interrupt vectors—two for the data handling section and one for the modem control. The interrupt vectors are in the floating vector space that starts at 300. The DV11 modem control follows the DM11-BB which follows the DN11. The DV11 data handling section follows the DUP11 which in turn follows the DU11.

Timing Considerations

The modem control timing considerations consist of scan control and CLR SCAN operations. Scan control through the CSR allows the scan either to run free (SCAN EN) or to be sequentially stepped through the line counter line-by-line (STEP bit of CSR). The read/write cycles of the modem control scan logic force the program to wait, after issuing CLR SCAN, until it has cycled through the memories. Also, the scan's read/write cycles prevent halting the scan and changing the line number with one machine cycle.

Programs should not spin on flags in the DV11 secondary registers using loops less than 30 (octal) instructions; to do so may interfere with DV11 RAM processor/UNIBUS access interlocks.

Order Numbers

DV11-AA—Double System unit contains all DV11 logic except the line cards and distribution panels. No lines are implemented.

DV11-BA—Line cards and distribution panel for eight lines. Requires 5¼ inches of cabinet space. Two DV11-BA's can be used with one DV11-AA.

To configure an 8-line DV11, order one DV11-AA and one DV11-BA.

To configure a 16-line DV11, order one DV11-AA and two DV11-BA's.

Bus Loads

Two bus loads.

Power Consumption

15 amps @ +5 volts.
1 amp @ −15 volts.
0.5 amps @ +15 volts.

Environmental

+10° to +50°C. with a relative humidity of 20% to 95%.

Space Requirements

DV11-AA: two system units (SU's)
DV11-BA: 5¼ inches of cabinet space (SM PAN)

Cables

Order BC05D-25 modem cables. 7.6m 25-conductor cable terminated in cinch DB25S socket at one end and cinch DB25P plug at the other.

Internal Clock

The DV11 includes an internal clock which can be used when two PDP-11's are connected locally without modems. It is also useful for diagnostic purposes. The clock speed can be set at 1200, 2400, 4800, or 9600 baud, switch-selectable for each 4-line group 0-3, 4-7, 8-11, 12-15).