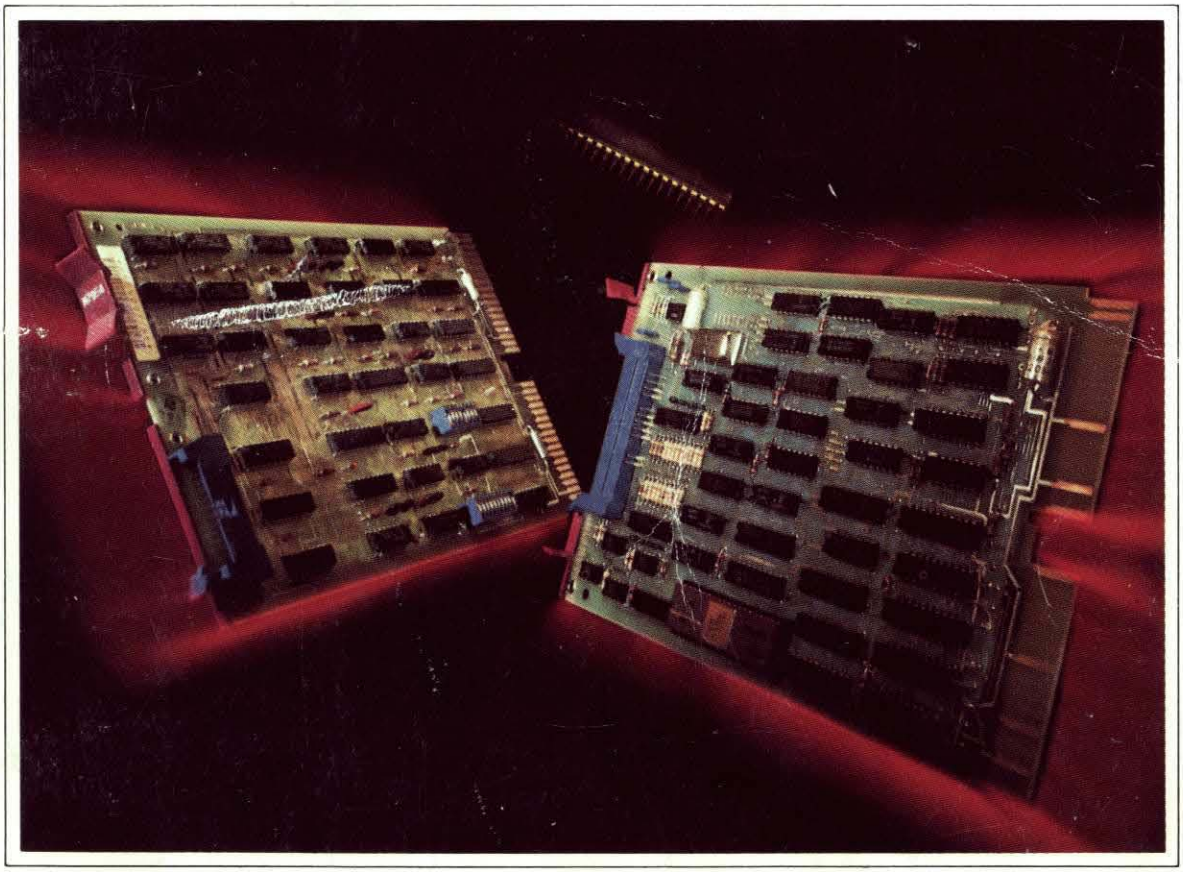
digital PDP-11 Microcomputer Interfaces Handbook 1983–84



PDP-11

Microcomputer Interfaces Handbook

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DIGITAL Facility, Hudson, Massachusetts

CORPORATE PROFILE

Digital Equipment Corporation designs, manufactures, sells and services computers and associated peripheral equipment, and related software and supplies. The Company's products are used world-wide in a wide variety of applications and programs, including scientific research, computation, communications, education, data analysis, industrial control, timesharing, commercial data processing, word processing, health care, instrumentation, engineering and simulation.

***Cover**— Flanked by two DIGITAL interface board modules— the IBV11-A instrument bus interface and the DPV11-DA serial synchronous line interface— is DIGITAL's first available serial line communications chip interface— the DC319-AA DLART. The DLART represents DIGITAL's latest advancement and commitment to an even lower level of integration than board-level components, while still providing proven PDP-11 architecture. System and hardware designers, as well as other customers will find this new level of integration an attractive alternative for application designs based on chip-level microcomputer-based products, including implementation of DIGITAL's new family of chip-level processors— the T-11, the F-11,and the J-11.*

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This handbook was designed, produced, and typeset
by DIGITAL's New Products Marketing Group
using an in-house text-processing system.

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PART 2 LSI-11 BUS INTERFACE DESCRIPTIONS

* This interface product appears out of the alphanumeric sequence in this handbook because it was included just prior to publication.

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PREFACE

The 1983-84 Microcomputer Interfaces Handbook is the companion publication to the 1982 Microcomputers and Memories Handbook.

Designed in the form of a catalog, the purpose of this handbook is to provide DIGITAL customers with quick and handy reference material on DIGITAL microcomputer interface options that connect to the LSI-11 bus. Though user applications may vary widely, the detailed logic, configuration, and installation information presented in this handbook should be sufficient to satisfy their needs. In most cases throughout this handbook, the interfaces have a detailed introductory section, a features section, specifications, configuration, and descriptive narrative— especially on the newer interface products. The major product sections in the handbook include: Interface Options, Communications Options, Peripherals, Backplanes, Enclosures (boxes), Cabinets, Power Supplies, Cables and Connectors, Intergrated Circuits, and miscellaneous options available for DIGITAL'S diverse family of both board-level and systems-based microcomputers.

A major goal of this handbook is to present the most recently introduced interface products and still provide needed but basic information on the older interface products. Detailed passages on 11 new interface products are currently found in this handbook, including a new family of analog I/O boards— the AAV11-C, the ADV11-C, and the AXV11-C; the KWV11-C programmable realtime clock; the H9275-A and H9276 backplanes; the BA11-S mounting/expander box; the DPV11-DA synchronous serial line interface; the DMV11 synchronous line controller; the RLV12 disk controller; and for the first time, we are including a section on the new serial line communications chip interface— the DC319-AA DLART. Passages on the DPV11-DA, the DMV11, and the RLV12 appear at the end of Part 2 of this handbook. These three interface products are out of alphanumeric sequence because they were included (immediately) prior to the time of publication.

Since this handbook was last published, many DIGITAL microcomputer interface products that were written about extensively then are currently not necessarily the most technically advanced or newest ones available. For example, in a case where a customer who still uses the AAV11-A four-channel 12-bit D/A converter, a DIGITAL interface introduced a few years back, information pertaining to this interface was found in the first few pages of the 1981 Microcomputer interfaces Handbook. In this handbook, however, an abbreviated version briefly introduces and describes its features and benefits, and lists its specifications. Appendix F in the back of this handbook lists all the documention and order numbers needed to supplement these older

products. For users requiring extensive information on some of these microcomputer interfaces, this appendix lists all the necessary reference material, at several levels of technicality, including user documents, configuration guides, and data sheets.

A section devoted to mass storage peripherals will be covered in a future handbook. For users desiring information on DIGITAL's memory offerings and detailed information on LSI-11 bus signals, please consult the 1982 Microcomputers and Memories Handbook. The order code for the Microcomputer and Memories Handbook is EB-20912-20.

part 1
introduction

INTRODUCTION

This handbook is a reference guide for interface and peripheral hardware options that can be installed on the LSI-11 bus. It includes descriptions, specifications, configuration information, programming information as applicable to the options, and functional theory. Because the hardware options described in this handbook are designed to interface with a processor via the LSI-11 bus, the user should be familiar with the contents of the 1982 Microcomputer and Memories Handbook.

The 1983-84 Microcomputer Interfaces Handbook is organized into two parts. Part 1 contains general information about microcomputer interfaces. Part 2 contains descriptions of the interface options in alphanumeric sequence.

Digital Equipment Corporation designs and manufacturers the options described in this handbook. Our general design criterion is to provide maximum system throughput for options when they are installed on the LSI-11 bus. LSI-11 bus-compatible processors, interfaces, and peripherals are designed to work together to provide a broad spectrum of system-compatible hardware options. Memory and peripheral devices can be used with various LSI-11 bus configurations and the system can later be expanded or modified to meet new system requirements. This hardware flexibility, when coupled with DIGITAL software and support, provides a single source for all present and future microcomputer processing needs.

LSI-11 FAMILY CHARACTERISTICS

LSI-11 bus systems include various processors, memory and peripheral device options, and software. Some of the characteristics of the LSI-11 bus systems are:

- Low-cost powerful components for integration into any small- or medium-sized computer system.
- Direct addressing of all memory locations and peripheral device registers.
- Efficient processing of 8-bit bytes (characters) without the need to rotate, swap, or mask.
- Asynchronous bus operation that allows system components to run at their highest possible speed; replacement with faster devices means faster operation without other hardware or software changes.
- A module component design that provides ease and flexibility in configuring systems.

- Inherent direct memory access capabilities for high data rate devices.
- A bus structure that provides position-dependent priority for peripheral device interfaces connected to the I/O bus.
- Vectored interrupts that allow service routine entry without device polling.

Processors

The processor is connected to the LSI-11 bus (backplane) as a subsystem that executes programs and arbitrates usage of the LSI-11 bus for peripherals. It contains multiple, high-speed, general-purpose registers that can be used as accumulators, address pointers, index registers, and other specialized functions. The processor can perform data transfers directly between peripheral input/output (I/O) devices and memory without disturbing the processor registers. Data transfers include both 16-bit word and 8-bit byte data.

LSI-11 Bus

System components, including the processor, memory, and peripherals, are interconnected and communicate with each other via the LSI-11 bus. The form of communication is the same for all devices on the bus; instructions that communicate with memory can communicate with peripheral devices. Each device, including memory locations and peripheral device registers, is assigned an individual byte or word address on the LSI-11 bus.

The LSI-11 bus supports 16-, 18-, and 22-bit addresses. However, processors and peripherals having a 22-bit addressing capability are completely PDP-11 hardware- and software-compatible within the 18-bit or 16-bit limitation. Simarily, 18-bit addressing devices are downward-compatible to 16-bit addressing. By PDP-11 convention, all peripheral device addresses are located within the upper 4K address space in the system, whether 16-bit or 18-bit addresses are used. This 4K address space is called the I/O page or "bank 7."

Whenever the I/O page is addressed, the processor must assert the BBS7 L bus signal. All peripheral devices use this signal line during addressing rather than decoding address bits<15:13>or<17:13>. An active (asserted) BBS7 L signal will always indicate an address in the I/O page, enabling peripheral device addressing.

Peripheral device addresses within the I/O page are decoded by each peripheral device. Each peripheral device will include one or more "device register(s)." These registers can be accessed under program con-

trol in exactly the same manner as memory locations. Unique addresses within the I/O page are encoded on address bits<15:00>.

NOTE

Address bits, for the purpose of this discussion, are logical states present on LSI-11 bus signal lines BDAL<17:00>L during the addressing portion of a bus cycle.

Refer to the appropriate processor handbook for a complete description of bus transactions, including bus cycles, addressing, etc.

Device Registers

All peripheral devices are defined by one or more device registers that are addressed as part of the main memory. These registers are generally designated control and status registers.

Control and status registers (CSRs) contain all the necessary information to establish communications with the device. Some devices will require fewer than 16 status bits, while other devices could require more than 16 bits and therefore will require additional registers. The bits of the CSR have predetermined assigned functions. Typical bit functions include interrupt enable, error, done or ready, and enabled.

Data buffer registers (DBRs) are for temporarily storing data to be transferred into and out of the processor. The number and type of data registers is a function of the individual peripheral device requirements.

Interrupts

Interrupts allow devices to obtain processor service when they are "ready" for service, or "done" with a specific operation. The interrupt structure allows the processor to execute other programs while one or more peripherals are "busy." When a peripheral requires service it requests an interrupt. The processor completes execution of the present instruction, saves PC and PS words on the stack, and acknowledges the interrupt. The highest priority peripheral device currently requesting interrupt service responds by inputting its interrupt vector address to the processor. The processor uses this vector address as a pointer to two memory locations containing the PC (starting address) and PS for the peripheral device interrupt service routine. Program control is transferred from the interrupted program to the routine associated with the requesting peripheral device. Note that no device polling is required, since the interrupt vector is unique for that device. Once the

device service routine execution has been completed, control is returned either to the previously interrupted program or to another peripheral device requesting interrupt service.

Memory Address

Memory addresses are generally limited to the address space other than the I/O page. However, the I/O page can contain read-only memory (ROM) for disk bootstraps, paper tape loaders, diagnostics, etc. or read/write memory for DMA buffers. The system designer must use care in assigning memory addresses within the I/O page to avoid conflicts with peripheral device addresses used for actual system hardware, or addresses that system software may attempt to access for peripheral devices not actually installed in the system. See Appendix A for the standard assignments of the addresses in the I/O page.

SPECIFICATIONS

All the LSI-11 bus modules will operate under the following conditions:

Temperature	5° to 60° C (41° to 140° F)
Humidity	10 to 95% (no condensation)

When operating at the maximum outlet temperature (60° C or 140° F), adequate air flow must be maintained to control the inlet to outlet temperature rise across the modules to 5° C (9° F) maximum. The air flow should be directed to flow across the modules.

All the individual module specifications are included in the detailed descriptions of the peripheral or option. A summary of the module characteristics is provided in Table 2; these characteristics are defined as follows:

1. The option designation is the alphanumerical code assigned to the option.
2. The module number is the number assigned to the interface modules that are connected to the LSI-11 bus. This number is printed on the module handle and can be used as a quick reference to determine what specific options are installed in any system. The module numbers are listed numerically in Table 3 so that the user can identify the options installed by using the module numbers.
3. The module description identifies the category of the option.
4. The power requirements specify the power by the option when connected to the bus backplane. These requirements are used to determine the total power supply loading within a single system.

5. The bus loads for ac and dc loading are provided so that the user can calculate the total ac and dc loading for any system.
6. The interface modules are standarized as either a double or a quad and all are extended length. The double size module is 13.2 cm (5.2 in.) high, 22.8 cm (8.9 in.) long, and 1.27 cm (0.5 in.) wide. The quad size module is 26.5 cm (10.5 in.) high, 22.8 cm (8.9 in.) long, and 1.27 cm (0.5 in.) wide (Figure 1).

DESCRIPTION OF OPTION CATEGORIES

The LSI-11 bus peripherals and options are classified into general categories that pertain to their performance and function. This listing indicates the wide span of equipment capability available to the user.

Interface Options

AAV11-A — The AAV11-A is a 4-channel, 12-bit digital-to-analog converter module that includes control and interfacing circuits. It has four D/A converters, a dc-dc converter that provides power to the analog circuits, and a precision voltage reference. Each channel has its own holding register that can be addressed separately and provides 12 bits of resolution. Bits 0, 1, 2, and 3 of the fourth holding register are brought out to the I/O connector so that they can be used as a 4-bit digital output register.

AAV11-C — The AAV11-C is a 4-channel, 12-bit digital-to-analog converter module that has four individually addressable, separately controlled digital-to-analog converters (DACs), each with 12 bits of resolution. Each DAC can be written or read in either word or byte format. One of the DACs also has four digital output bits for creating control signals to an analog instrument. The D/A converters accept data from a program controlled interface in either a binary notation for unipolar output, or offset binary for bipolar output.

ADV11-A — The ADV11-A is a 12-bit successive approximation analog-to-digital converter that samples analog data at specified rates and stores the digital equivalent value for processing. The mul-

tiplexer can accommodate up to 16 single-ended or 8 quasi-differential inputs. The converter uses a patented auto-zeroing design that measures the sampled data with respect to its own offset and therefore cancels out its own offset error.

External event inputs can originate at the user's equipment or from the Schmitt trigger output of the KWV11-A clock. Three reference signals are provided for self-testing any channel input. These signals consist of two dc levels and one bipolar triangular waveform. This output can be used with DIGITAL diagnostic software to produce a data base for extremely precise analog linearity testing.

ADV11-C

The ADV11-C is a dual-height LSI-11 bus module that performs analog-to-digital conversions. It may be configured to provide either 16 single-ended, 16 pseudo-differential, or eight true-differential analog input channels with input full scale ranges of either 0 to 10V or -10V to 10V. This board is designed to interface analog instrumentation to the LSI-11 bus, and is suitable for use in a wide variety of industrial and laboratory LSI-11 microcomputer applications such as data acquisition/display, process control, and signal analysis.

The ADV11's precision instrumentation amplifier, under software control, may be programmed to amplify input signals by factors of 1, 2, 4, or 8 before being digitized by the A/D converter. This programmable gain feature provides effective input signal full scale ranges of 10V, 5V, 2.5V, and 1.25V, respectively, especially useful for maintaining maximum resolution of input signals that fall below 50% of the 12-bit A/D converter's 10V range.

AXV11-C

The AXV11-C is a cost-effective analog I/O interface board that has 16 single-ended analog input channels. The AXV11-C offers all the features of the ADV11-C plus two analog output channels,

each with 12-bit D/A converters. Each D/A converter generates an output signal with full 12-bit accuracy and resolution. The D/A's accept data in either binary, offset binary, or two's complement notation.

DRV11

The DRV11 is a parallel interface module that is used to interconnect the LSI-11 bus with general-purpose, parallel line TTL or DTL devices. It allows program-controlled data transfers at rates up to 40K words per second and uses LSI-11 bus interface and control logic to generate interrupts and process vector handling. The data are handled by 16 diode-clamped input lines and 16 latched output lines. There are two 40-pin connectors on the module for user interface applications.

DRV11-B

The DRV11-B is an interface module that uses direct memory access (DMA) to transfer data directly between the system memory and an I/O device. The interface is programmed by the processor to move variable length blocks of 8- or 16-bit data words to or from specified locations in the system memory. Once programmed, there is no processor intervention required. The module can transfer up to 250K 16-bit words per second in the single-cycle mode and up to 500K 16-bit words per second in the burst mode. It also allows read-modify write operations.

DRV11-J

Sixty-four input/output data lines are now available on a double-height module for the LSI-11/2, LSI-11/23, PDP-11/03, and PDP-11/23. The DRV11-J also includes an advanced interrupt structure with bit interruptability up to 16 lines, programmable interrupt vectors, and program selection of fixed or rotating interrupt priority within the DRV11-J. The DRV11-J's bit interrupts for real-time response make it especially useful for sensor I/O applications. It can also be used as a general-purpose interface to custom devices, and two DRV11-Js can be connected back-to-back as a link between two LSI-11 buses.

INTRODUCTION

DRV11-P

The DRV11-P is a foundation wire-wrap interface module with a 40-pin I/O connector. Approximately 25 percent of the module is occupied by bus transceivers, interrupt vector generation logic, device comparator logic, protocol logic, and interrupt logic. The remaining 75 percent is for user applications; this portion has plated-through holes for securing ICs and wire-wrap pins for interconnecting the user's curcuits. The plated-through holes can accept 6-, 8-, 14-, 18-, 20-, 22-, 24-, and 40-pin dual-in-line integrated circuits or discrete components.

IBV11-A

The IBV11-A is an interface module that interconnects the LSI-11 bus with the instrument bus described in IEEE standard 488 1975, "Digital Interface for Programmable Instrumentation." The IBV11-A makes a processor-controlled programmable instrument system possible. The module can accommodate up to 15 IEEE-488 devices and is PDP-11 software-compatible.

KWV11-A

The KWV11-A is a programmable real-time clock/counter that provides a means of determining time intervals or counting events. It can be used to generate interrupts to the processor at predetermined intervals or establish timing between input and output events. It can also initialize the ADV11-A analog-to-digital converter by a clock counter overflow or by firing a Schmitt trigger. The clock counter has a resolution of 16 bits and can be driven by any one of five crystal-controlled frequencies (100 Hz to 1 MHz), from a line frequency input, or from a Schmitt trigger fired by an external input. The module can operate in any of four programmable modes: single interval, repeated interval, external event timing, and external event timing from zero base.

KWV11-C

The KWV11-C, like the KWV11-A, is a programmable real-time clock/counter that provides a variety of means for determining time intervals or counting events. It can generate interrupts to the

processor at predetermined intervals or establish timing between input and output events. It is used to start the ADV11-C analog-to-digital converter or the AXV11-C analog I/O module, either by clock counter overflow or by the firing of a Schmitt trigger. The KWV11-C's two Schmitt triggers each have integral slope and level controls. The Schmitt triggers permit the user to start the clock, initiate A/D conversions, or generate program interrupts in response to external events.

Communications Options

DLV11

The DLV11 is a serial line unit (SLU) that interfaces with asynchronous serial I/O devices. The module has jumper-selectable baud rates (50-9600) and serial word format that includes the number of stop bits, number of data bits, and even, odd, or no parity bit. The DLV11 can support 20 mA current loop interfaces or EIA "data leads only" interfaces.

DLV11-E

The DLV11-E is an asynchronous line interface module that interconnects the LSI-11 bus to standard serial communications lines. The module receives serial data, converts it to parallel data, and transfers it to the LSI-11 bus. Also, it accepts parallel data from the LSI-11 bus, converts it to serial data, and transmits it to the peripheral device. The module has jumper-selectable or software-selectable baud rates (50-19,200), and jumper-selectable data bit formats. The DLV11-E offers full modem control for EIA/CCITT interfaces.

DLV11-F

The DLV11-F is an asynchronous line interface module that interconnects the LSI-11 bus to several types of standard serial communications lines. The module receives serial data, converts it to parallel data, and transfers it to the LSI-11 bus. It also accepts parallel data from the LSI-11 bus, converts it to serial data, and transmits it to

the peripheral device. The module has jumper-selectable or software-selectable baud rates (50-19,200) and jumper-selectable data bits. The DLV11-F supports either 20 mA current loop or EIA standard lines, but does not include modem control.

DLV11-J

The DLV11-J contains four independent asynchronous serial line channels used to interface peripheral devices to the LSI-11 bus. Each channel transmits and receives data from the peripheral device over EIA data leads (lines that do not use a control line). The module can be used with 20 mA current loop devices if a DLV11-KA adapter is used. The DLV11-J has jumper-selectable baud rates from 150 to 38.4 K baud.

DUV11

The DUV11 synchronous line interface module establishes a data communication line between the LSI-11 bus and a Bell 201 synchronous modem or equivalent. The module is fully programmable with respect to sync characters, character length (to to 8 bits), and parity selection. The receiver logic accepts serial data for the LSI-11 bus. The transmitter logic converts the parallel LSI-11 bus data into serial data for the transmission line. The interface logic converts the TTL logic levels to the EIA voltage levels required by the Bell 201 modems and also controls the modem for half-duplex or full-duplex operation.

DZV11

The DZV11 is an asynchronous multiplexer interface module that interconnects the LSI-11 bus with up to four asynchronous serial data communications channels. The module provides EIA interface voltage levels and data set control to permit dial-up (auto-answer) options with full-duplex modems such as Bell models 103, 113, 212, or equivalent. The DZV11 does not support half-duplex operations or the secondary transmit and receive operations available in some modems such as Bell 202. The DZV11 has applications in

data concentration and collection systems where front-end systems interface to a host computer and for use in a cluster controller for terminal applications.

Peripherals

LPV11

The LPV11 printer option consists of an interface module, an interface cable, and either an LP05 or LA180 line printer. The interface module provides programmed control of data transfers and provides printer strobe signals appropriate for either printer. The LA180 DECprinter is a high-speed printer that prints 180 characters per second and the LP05 printer can print 240 or 300 lines per minute, depending on which model is selected.

RXV11

The RXV11 option consists of an interface module, cable assembly, and either a single or dual drive RX01 floppy disk. This option is a random access mass storage device that stores data in fixed-length blocks on a preformatted flexible diskette. Each diskette can store and retrieve up to 256K, 8-bit bytes of data. The RXV11 system is rack mountable in the standard 48.3 cm (19 in.) cabinet.

RXV21

The RXV21 floppy disk option is a random access mass memory device that stores data in fixed-length blocks on a preformatted, flexible diskette. Each diskette can store and retrieve up to 512K 8-bit bytes of data. The RXV21 system is rack-mountable and consists of an interface module, an interface cable, and either a single or dual RX02 floppy disk drive. The interface module converts the RX02 I/O bus to the LSI-11 bus structure. It controls the RX02 interrupts to the processor, decodes device addresses for register selection, and handles the data interchange between the RX02 and the processor via DMA transfers. Power for the interface module is supplied by the LSI-11 bus.

TU58	The TU58 is a low-cost intelligent mass memory device that offers random access to block-formatted data on pocket-size cartridge media. It is ideal as inexpensive archive mass storage or as a software update distribution medium. A dual drive TU58 offers 512 Kb of storage space, making it one of the lowest cost complete mass storage subsystems available. For mounting flexibility, the TU58 is offered both as a component level subsystem and as a fully powered 5½" rack-mount subsystem.
VK170-CA	The VK170 module forms an integral part of a terminal. The module accepts serial ASCII encoded data to be stored in a refresh memory to generate a display for a video monitor. The VK170 also accepts parallel data from a keyboard (on strobe demand) to generate serial ASCII output. The VK170 is an extended-length, double-height board. Mounting holes are provided for stand-off mounting via handle rivets and two holes located near the module fingers.

Backplanes

The following backplane options are available for the LSI-11 bus:

H9270	A 4 × 4 (four rows of four slots each) backplane with card guide assembly. LSI-11 bus in rows A-B and C-D. Accepts 8 double-height modules or 4 quad-height modules or combinations of both.
H9273-A	A 9 × 4 (nine rows of four slots each) backplane with card guide assembly. LSI-11 bus in rows A-B only. Special interconnect bus in rows C-D. Accepts double-height or quad-height modules.
H9275-A	A 9 × 4 (nine rows of four slots each) backplane with card guide assembly. LSI-11 bus in rows A-B and C-D. Accepts up to 18 dual-height modules or nine quad-height modules or a mixture of both. Supports 4 megabyte (22-bit) addressing capability.
H9276	A 9 × 4 (nine rows of four slots each) backplane. Extended LSI-11 bus in rows A-B. C-D rows are

	special interconnect bus rows. Accepts both double- and quad-height LSI-11 modules for use in a 22-bit addressing system. Can be used as a mounting box or as an expander box.
H9281	A 2-slot backplane available in 4-, 8-, or 12-slot options. Accepts double-height modules only.
DDV11-B	A 9 × 6 (nine rows of six slots each) backplane. LSI-11 bus in rows A-B and C-D. Rows E-F are unbussed except for +5V and ground. Accepts 18 double-height or 9 quad-height modules or combinations of both.

Enclosures

H909-C	A 13.3 cm (5.25 in) high, 48.3 cm (19 in) wide enclosure which can be mounted in a 48.3 cm (19 in) rack or as a stand-alone. Accommodates the DDV11-B backplane or a 9 × 6 system mounting unit or houses non-standard mounting arrangement. Includes cooling fan, cord guide, cable restraints, front bezel, and connector block.
BA11-M	A 8.9 cm (3.5 in) high, 48.3 cm (19 in) wide expansion box which can be mounted in 48.3 cm (19 in) rack. Includes H9270 backplane, H780 power supply, blank front panel or bezel, and cooling fan.
BA11-N	A 13.2 cm (5.19 in) high, 48.3 cm (19 in) wide mounting box which can be mounted in a 48.3 cm (19 in) rack. Includes H9273-A backplane, H786 power supply, H403-A ac input panel, blank front panel or bezel, and cooling fan.
BA11-S	A 13.2 cm (5.19 in) high, 48.3 cm (19 in) wide mounting or expander box. It can be installed in a standard 48.3 cm (19 in) rack. Includes H9276 backplane, H7861 power supply, H403-B ac input box, a blank front bezel or bezel assembly with switches and indicators, and two cooling fans.

BA11-VA

The BA11-VA is a small form-factor package providing mounting space and power for four LSI-11/2 or LSI-11/23 family modules. This package, plus the high functionality of DIGITAL's microcomputer products, allows LSI-11 microcomputer applications to be implemented within a space smaller than that required for many 8-bit systems.

Power Supplies

H780

Provides +5V ± 4%, 18 A (max) and +12V ± 3%, 3.5 A (max) at 110 Vac and features line-time clock, and power-fail/automatic restart. Available primary power of 115 or 230 Vac and with or without master and slave console.

Cables and Connectors

Various preassembled cables in different lengths are available for use with interface and communications options. See Appendix E for commonly used cables.

Wire-Wrappable Modules

W9500 Series: LSI-11 Bus-Compatible Wire-Wrappable Modules (W9511, W9512, W9514 AND W9515) — The LSI-11 bus-compatible wire-wrappable modules consist of quad-height and double-height modules. Two LSI-11 bus-compatible modules are available without DIP sockets.

W9511

Quad-height, extended-length, single-width module with extractor handle. No DIP sockets included. One 40-pin male cable connector premounted on board and space for additional 40-pin connector provided.

Power and ground connections are V_{CC} —
BA2, CA2, DA2
GND —AT1, BT1, CT1, DT1, AC2, BC2, CC2, DC2

W9514

Same as W9511 except with 58 pre-mounted DIP sockets.

	Power and ground connections are the same as W9511
W9512	Double-height, extended-length, single-width module with Flip-Chip handle. No DIP sockets included. One 40-pin male connector premounted on board.
	Power and ground connections are GND—AT1, BT1,AC2, BC2
W9515	Same as W9512 except with 25 pre-mounted DIP sockets.
	Power and ground connections are the same as W9512

Integrated Circuits

DC319-AA DLART	The DC319-AA DLART is a DL-compatible, asynchronous receiver/transmitter designed for data communications with Digital's microprocessor family. Programmed by the CPU to operate either in 8-bit or 16-bit mode with asynchronous baud rates ranging from 300 to 38.4K, the DLART accepts data characters from the CPU in parallel format and converts them into a continuous serial data stream for transmission. Simultaneously, the DLART can receive serial data streams and convert them into parallel data characters for the CPU.
DCK11-AA, -AC	The DCK11-AA and -AC CHIPKITs provide the logic necessary for a program transfer interface to the LSI-11 bus. The DCK11-AA kit contains one DC003 Interrupt Chip, one DC004 Protocol Chip, and four DC005 Transceiver/Address Decoder/Vector Select Chips. The DCK11-AC kit contains previous chips plus one W9512 double-height, extended length, high-density wire-wrappable module and one BC07D-10 ten-foot, 40-connector plug-in cable.
DCK11-AB, -AD	The DCK11-AB and -AD CHIPKITs provide the logic necessary for a Direct Memory Access (DMA) interface to the LSI-11 bus.

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The DCK11-AB kit contains one DC003 Interrupt Chip, one DC004 Protocol Chip, four DC005 Transceiver/Address Decoder/Vector Select Chips, two DC006 Word Count/Bus Address Chips, and one DC010 DMA Control Chip. The DCK11-AD kit contains the previous chips plus one W9512 double-height, extended-length, high-density wire-wrappable module and one BC07D-10 ten-foot, 40-connector plug-in cable. DMA applications use the same chips as program control interfaces, plus two DC006s for word or byte address counters and a DC010 DMA bus control IC.

Miscellaneous Options

BDV11

The BDV11 module has 2K words of read-only memory (ROM) that contains diagnostic and bootstrap programs. These programs are user-selectable by setting dip switches. The diagnostic programs will test the processor, the memory, and the user's console. The bootstrap programs can boot most LSI-11 peripheral devices. The module also has 120-ohm bus terminator circuits.

The user can add up to 16K of read-only memory (ROM) and up to 2K words of erasable programmable ROM (EPROM) on the module. This 18K words of additional memory can be used with no increase in the amount of I/O address space.

KPV11-A, -B, -C

The KPV11-A module generates power-up and power-down sequences, monitors for a power-fail condition, and generates the line-time clock (LTC) function. The KPV11-B is the same as the "A" except that it provides 120-ohm termination circuits. The KPV11-C is the same as the "A" except that it provides 220-ohm termination circuits. The module can be installed on any backplane or remotely installed via an optional cable.

INTRODUCTION

REV11-A, -C	The REV11-C module has a bootstrap ROM and direct memory access (DMA) refresh circuits. The REV11-A is identical to the REV11-C except it has additional 120-ohm termination circuits.
TEV11	The TEV11 is a bus terminator module that provides 120-ohm bus termination circuits.
DLV11	The DMV11 is a microprocessor- controlled communications interface that permits Direct Memory Access (DMA) data transfers. The controller converts parallel data from the LSI-11 bus to serial data for line transmission and serial data from the the line to parallel data for the LSI-11 bus. The serial data is transferred synchronously over private or leased telephone lines or through shielded cables for local operation. The controller performs the detailed protocol operations, including character and message synchronization, header and message formatting, error checking, and transmission control.
DPV11-DA	The DPV11-DA is an single-line, program-controlled, double-buffered communication device designed to interface the LSI-11 bus to high-speed serial synchronous lines for use in many commercial, industrial, and scientific applications, such as remote batch, remote data collection, remote concentration and communication networking. The self-contained DPV11-DA can handle a wide variety of protocols.
RLV12	The RLV12 disk controller interfaces RL01 and RL02 disk drives to any quad- or hex-size backplane that uses a 16-, 18-, or 22-bit LSI-11 bus. One RLV12 can control up to four RL01 and RL02 disk drives, in any combination. The RLV12 has LSI-11 bus transceivers and decoders, programmable registers, controller timing and sequence logic, and data formatting circuits to read and write on the disk.

Table 1 Module Specifications

Option Desig.	Module No(s).	Description	Power Requirements +5V ±5%	Power Requirements +12V ±3%	Bus Loads* AC(Max)	Bus Loads* DC	Size
AAV11-A	A6001	4-channel, 12-bit D/A converter	1.5 A	0.4 A	1.9	1	Quad
AAV11-C	A6006	4-channel, 12-bit D/A converter	2.0 A	—	0.9	1.0	Double
ADV11-A	A012	16-channel, 12-bit A/D converter	20. A	0.45 A	3.25	1	Quad
ADV11-C	A8000	16 single-ended or 8 differential A/D channels, 12-bit	1.5 A	—	1.3	1.0	Double
AXV11-C	A0026	Analog I/O board 16 single-ended analog input channels, 12-bits 2 D/A output, 12-bit channels	1.5 A	—	1.3	1.0	Double
BDV11	M8012	Bootstrap, terminator, diagnostic	1.6 A	0.07 A	2.0	1	Quad
DDV11-B		6 X 9 backplane			6.4	0	

* These ac load figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/ac load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

Table 1 Module Specifications (cont.)

Option Desig.	Module No(s).	Description	Power Requirements +5V ±5%	Power Requirements +12V ±3%	Bus Loads* AC(Max)	Bus Loads* DC	Size
DLV11	M7940	Asynchronous serial line interface	1.0 A	0.18 A	2.5	1	Double
DLV11-E	M8017	Asynchronous line interface	1.0 A	0.18 A	1.6	1	Double
DLV11-F	M8028	Asynchronous line interface	1.0 A	0.18 A	2.2	1	Double
DLV11-J	M8043	4 asynchronous serial interfaces	1.0 A	0.25 A	1	1	Double
DPV11	M8020	Synchronous serial line interface	1.2 A	0.30 A	1.0	1.0	Double
DMV11		Synchronous line controller	4.7 A	0.38 A	2.0	1.0	Quad
DRV11	M7941	Parallel line unit interface	0.9 A	—	1.4	1	Double
DRV11-B	M7950	DMA interface	1.9 A	—	3.3	1	Quad
DRV11-J	M8049	64-line parallel I/O	1.6 A	1.8 A	2.0	1	Double
DRV11-P	M7948	Foundation module	1.0 A + user logic	—	2.1	1	Quad

* These ac load figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/ac load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

Table 1 Module Specifications (cont.)

Option Desig.	Module No(s).	Description	Power Requirements +5V ±5%	Power Requirements +12V ±3%	Bus Loads* AC(Max)	Bus Loads* DC	Size
DUV11	M7951	Synchronous serial line interface	0.86 A	0.32	1.00	1	Quad
DZV11	M7957	Asynchronous line interface	1.15 A	0.39	3.95	1	Quad
H9270		4 X 4 backplane			5.1	0	
H9273		4 X 9 backplane			2.6	0	
H9275-A		4 X 9 backplane	—	—	10.0	0	
H9276		4 X 9 backplane			2.6	0	
H9281A		2 X 4 backplane			1.3	0	
H9281B		2 X 8 backplane			2.4	0	
H9281C		2 X 12 backplane			3.6	0	
IBV11-A	M7954	Instrument bus interface	0.8 A	—	1.9	1	Double
KD11-F	M7264	LSI-11 CPU 4K RAM	1.8 A	0.8 A	2.4	1	Quad

* These ac load figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/ac load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

Table 1 Module Specifications (cont.)

Option Desig.	Module No(s).	Description	Power Requirements +5V ±5%	Power Requirements +12V ±3%	Bus Loads* AC(Max)	Bus Loads* DC	Size
KD11-H	M7264-YA	LSI-11 CPU without RAM	1.6 A	0.25	2.4	1	Quad
KD11-HA	M7270	LSI-11/2 CPU	1.0 A	0.22 A	1.7	1	Double
KDF-11	M8186	LSI-11/23 CPU	2.0 A	0.2 A	2.0	1	Double
KPV11-A	M8016	Power-fail/line-time clock	0.56 A	—	1.63	1	Double
KPV11-B	M8016-YB	Power-fail/line-time clock/120 Ω bus terminator	0.56	—	1.63	1	Double
KPV11-C	M8016-YC	Power-fail/line-time clock/220 Ω bus terminator	0.56 A	—	1.63	1	Double
KUV-11	M8018	WCS module	3.0 A			1	Quad
KWV11-A	M7952	Programmable real-time clock	1.75 A	0.01 A	3.4	1	Quad
KWV11-C	A4002	Programmable real-time clock	1.75 A	0.1 A	1.0	1.0	Double

* These ac load figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/ac load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

Table 1 Module Specifications (cont.)

Option Desig.	Module No(s).	Description	Power Requirements +5V ±5%	Power Requirements +12V ±3%	Bus Loads* AC(Max)	Bus Loads* DC	Size
LPV11	M8027	LA180/LP05 printer interface	0.8 A	—	1.4	1	Double
MRV11-AA	M7942	4K X 16 read-only memory (less PROM intergrated circuits)	0.4 AA	—	1.8	1	Double
		(with 32 512 X 4 PROM integrated circuits) (MRV11-AC)	2.8 A				
MRV11-BA	M8021	UV PROM-RAM (less PROM integrated circuits	0.58 A	0.34 A	2.8	1	Double
		(with 8 1K X 8 PROM integrated circuits) (MRV11-BC)	0.62 A	0.5 A			

* These ac load figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/ac load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

Table 1 Module Specifications (cont.)

Option Desig.	Module No(s).	Description	Power Requirements +5V ±5%	Power Requirements +12V ±3%	Bus Loads* AC(Max)	Bus Loads* DC	Size
MRV11-C	M8048	PROM/ROM module	0.8 A		2.0	1	Double
MSV11-B	M7944	4K X 16 read/write MOS memory	0.6 A	0.54 A	1.9	1	Double
MSV11-CD	M7955-YD	16K X 16 read/write MOS memory	1.1 A	0.54 A	2.3	1	Quad
MSV11-D	M8044	4K/16K/32K MOS memory	1.7 A	0.34 A	2.0	1	Double
MSV11-E	M8045	4K/16/32K MOS memory	2.0 A	0.41 A	2.0	1	Double
MXV11-A	M8047	Multifunction module	1.2 A	0.1 A	2.0	2	Double
REV11-A	M9400-YA	120 Ω terminator, DMA refresh, bootstrap ROM	1.6 A	—	2.2	1	Double
REV11-C	M9400-YC	DMA refresh, bootstrap	1.6 A	—	2.2	1	Double

* These ac load figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/ac load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

Table 1 Module Specifications (cont.)

Option Desig.	Module No(s).	Description	Power Requirements +5V ±5%	Power Requirements +12V ±3%	Bus Loads* AC(Max)	Bus Loads* DC	Size
RLV12	M8061	Disk controller	5.0 A	0.1 A	3.0	1.0	Quad
RXV11	M7946	RX01 interface	1.5 A	—	1.8	1	Double
RXV21	N8029	Double density floppy interface	1.1 A		2.0	1	Double
TEV11	M9400-YB	120 Ω terminator	0.5 A	—	0	0	Double
TU58		Serial/cartridge cassette	0.75 Appr.	1.2 A max			
VK170	CAM7142	Serial video module	1.2 A	0.15			Double

* These ac load figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/ac load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

INTRODUCTION

CONFIGURATION

The LSI-11 bus permits a unified addressing structure in which control/status and data registers for peripheral devices are directly addressed as memory locations. All operations on these registers, such as transferring informaton to or from them or manipulating data within them, are performed by normal memory address instructions. The use of memory address instructions on peripheral device registers greatly increases the flexibility of input/output communications.

Addresses

All the options except memories have at least one control and status register and may have several data registers. Each register is assigned an address through which the option can communicate with the processor. The upper 4K of memory address space is reserved for the processor and external input/output (I/O) registers. The user can select any address (Appendix A) in the range of 160000 through 177776 and assign it to the option interface module. The modules are configured to the desired address by selecting dip switches, connecting or disconnecting wire-wrap pins, or installing or removing wired jumpers on the module.

part 2

the interfaces

AAV11-A

AAV11-A 4-CHANNEL 12-BIT D/A CONVERTER

INTRODUCTION

The AAV11-A is a four-channel, digital-to-analog converter module that includes control and interfacing circuits. It has four D/A converters, a dc-to-dc converter that provides power to the analog circuits, and a precision voltage reference. Each channel has its own holding register that can be addressed separately and provides 12 bits of resolution. These registers can be written and read, using either word or byte format. In addition, bits 0, 1, 2, and 3 of the fourth holding register are brought out to the I/O connector, so they can be used as a four-bit digital output register.

FEATURES

- Four 12-bit digital input channels, binary encoded for either unipolar mode or bipolar mode.
- Jumper-selected output ranges and modes:
  Bipolar mode ±2.56 V, ±5.12 V, ±10.24 V
  Unipolar mode 0 to +5.12 V, 0 to +10.24 V
- One part in 4,096 resolution
- 5 V/μs slew rate
- ±5 mA drive capability per converter

SPECIFICATIONS

Identification	A6001
Size	Quad
Power	+5.0 Vdc ±5% at 1.5 A +12.0 Vdc ±3% at 0.4 A
Bus loads	
ac	1.9
dc	1.0
Resolution	12 bits (1 part in 4,096)
Number of D/A converters	4
Digital input	12 bits (binary-encoded for unipolar mode; offset-binary-encoded for bipolar mode)
Digital storage	Read/write, word or byte operable, single-buffered

AAV11-A

Output voltage range (jumper selected)	±2.56 V, ±5.12 V, ±10.24 V bipolar, 0 V to +5.12 V, 0 V to +10.24 V unipolar
Gain accuracy	Adjustable (factory set for bipolar ±5.12 V)
Gain temperature coefficient	10 PPM per °C, max.
Offset temperature coefficient	20 PPM of full scale range per °C, max.
Linearity	±½ LSB max, nonlinearity
Differential linearity	±½ LSB, monotonic
Output impedance	1 ohm max.
Drive capability	±6 mA max. per converter
Slewing speed	5 V/μs
Rise and settling time (to 0.1% of final value)	4 μs (8 μs wth 5000 pF load in parallel with 1 kΩ

CONFIGURATION

This section describes how the user can configure the module to function within the system by setting dip switches (Figure 2) to obtain the desired device address. The voltage range for each D/A converter (DAC 0—DAC 3) can be configured independently by installing or removing the designated jumpers (Figure 2) associated with a specific D/A converter. This section also describes how to connect external devices to the module. The standard factory addresses for the registers are listed in Table 1.

AAV11-A

Table 1 Standard Addresses

Register	Mnemonic	Address
Holding 0	DAC 0	170440
Holding 1	DAC 1	170442
Holding 2	DAC 2	170444
Holding 3	DAC 3	170446

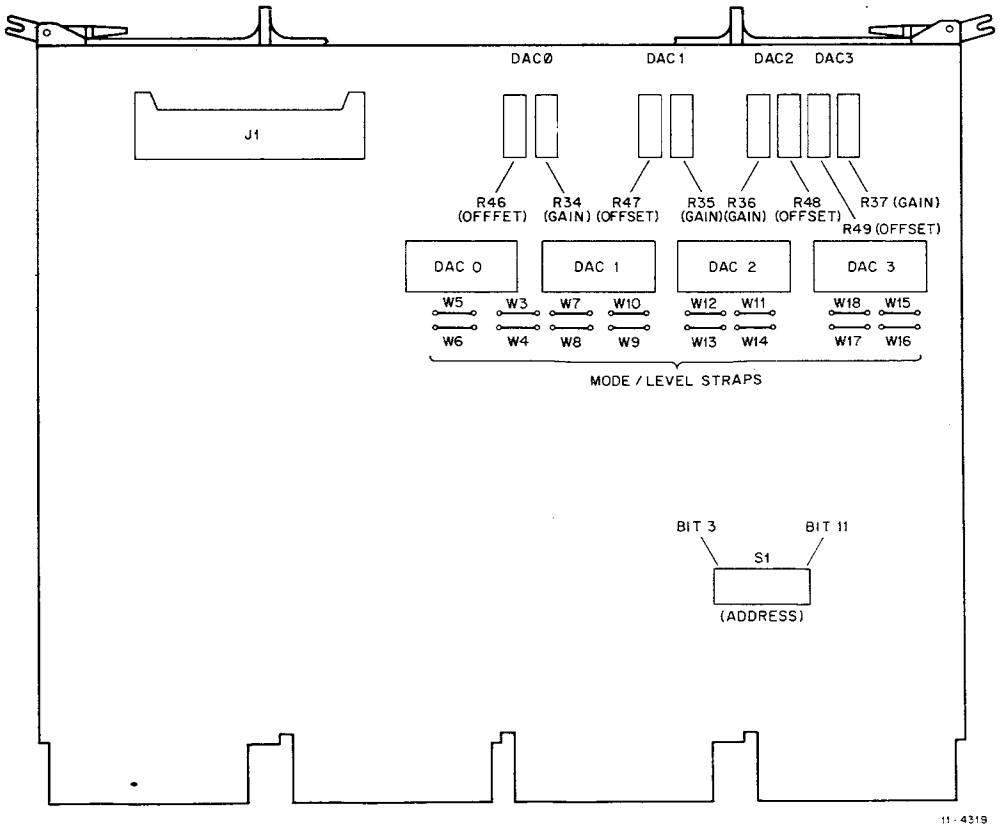


Figure 1 AAV11-A Connectors, Switches, and Jumpers

Device Registers

The device registers can be configured to respond to any address within the range 170000 to 177777. Each register address does not have to be individually set. The DAC 0 register address is selectable, and the last digit will be zero. The remaining registers will use addresses 17XXX2, 17XXX4, and 17XXX6 for DAC 1, DAC 2, and DAC 3 registers, respectively. The factory-configured device address is 170440 as shown in Figure 2. The word formats for the DAC registers are described in Table 2. Note that all device registers are always a sequence of four consecutive even locations. There is no vector used for this module.

D/A Converter Range and Mode

The range and mode (bipolar or unipolar) voltages can be selected by the user inserting or removing jumpers as shown in Figure 1. Four jumpers are associated with each D/A converter. The module is factory-configured for −5.12 to +5.12 V bipolar operation. The jumper configuations for the bipolar mode ranges are shown in Table 3; the unipolar ranges are shown in Table 4.

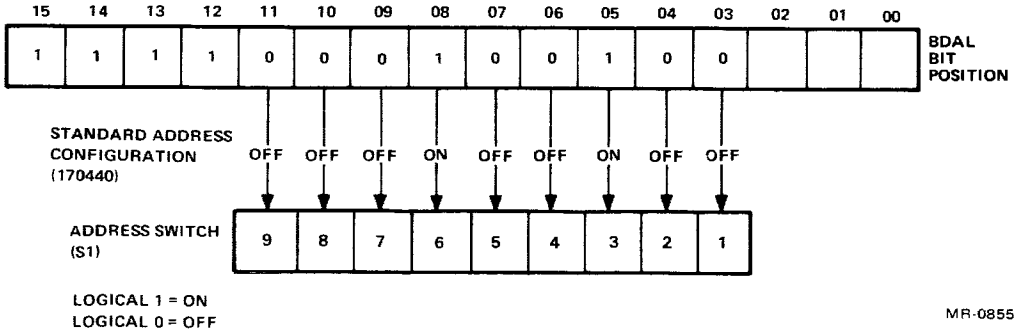


Figure 2 Address Selection

Table 2 DAC Word Formats

Bit	DAC 0, DAC 1, DAC 2	DAC 3
15-12	Not used	Not used
11	Binary 11	Binary 11
10	Binary 10	Binary 10
9	Binary 9	Binary 9
8	Binary 8	Binary 8
7	Binary 7	Binary 7
6	Binary 6	Binary 5
5	Binary 5	Binary 5
4	Binary 4	Binary 4
3	Binary 3	Binary 3/Control 3
2	Binary 2	Binary 2/Control 2
1	Binary 1	Binary 1/Control 1
0	Binary 0	Binary 0/Control 0

Table 3 Jumper Configurations for Bipolar Operation

	±2.56 V	±5.12 V	±10.24 V
DAC 1			
W3	IN	IN	OUT
W4	OUT	OUT	IN
W5	IN	OUT	OUT
W6	IN	IN	IN
DAC 2			
W7	IN	IN	OUT
W8	OUT	OUT	IN
W9	IN	OUT	OUT
W10	IN	IN	IN

Table 3 Jumper Configurations for Bipolar Operation (Cont)

	±2.56 V	±5.12 V	±10.24 V
DAC 3			
W11	IN	IN	OUT
W12	OUT	OUT	IN
W13	IN	OUT	OUT
W14	IN	IN	IN
DAC 4			
W15	IN	IN	OUT
W16	OUT	OUT	IN
W17	IN	OUT	OUT
W18	IN	IN	IN

Table 4 Jumper Configurations for Unipolar Operation

	0 V—+5.12 V	0 V—+10.24 V
DAC 1		
W3	IN	IN
W4	OUT	OUT
W5	IN	OUT
W6	OUT	OUT
DAC 2		
W7	IN	IN
W8	OUT	OUT
W9	IN	OUT
W10	OUT	OUT
DAC 3		
W11	IN	IN
W12	OUT	OUT
W13	IN	OUT
W14	OUT	OUT

Table 4 Jumper Configurations for Unipolar Operation (Cont)

	0 V—+5.12 V	0 V—+10.24 V
DAC 4		
W15	IN	IN
W16	OUT	OUT
W17	IN	OUT
W18	OUT	OUT

J1 Output Connections

Analog output devices such as oscilloscopes may be either grounded or floating. If the oscilloscope is grounded, either through its power plug or through contact between its chassis and a grounded cabinet, the oscilloscope ground should not be connected to any of the AAV11-A ground pins. Doing so may result in a ground loop which will adversely affect oscilloscope control results as well as ADV11-A operation (if used). If the oscilloscope is floating, its ground should be connected to the AAV11-A logic ground, J1 pins L, N, R, or T. Note that the foregoing assumes that the LSI-11 powersupply ground is connected to powerline (earth) ground. If continuity checks reveal no such connection, attach a length of 12-gauge wire between the powersupply ground and a convenient point associated with earth ground.

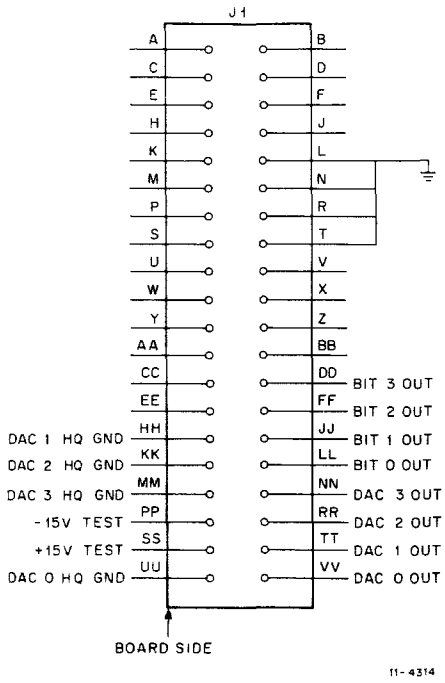


Figure 3 Connection to Oscilloscope with Differential Input

AAV11-C

AAV11-C ANALOG OUPUT BOARD

INTRODUCTION

The AAV11-C is a dual-height, multi-channel analog output board designed to interface analog instrumentation to the LSI-11 bus. It has four individually addressable digital-to-analog converters (DACs), each with 12 bits of input data resolution. Each DAC can be written or read in either word or byte format. Jumpers permit selection of the analog output voltage range for each register and its operating mode, either unipolar or bipolar. One of the registers, DAC D, also has four digital output bits for creating control signals to an analog device, such as a CRT.

FEATURES

- 4 D/A converter circuits, separately controlled
- 12-bit digital resolution
- Read/write, word or byte addressable registers
- Unipolar or bipolar output
- Output voltage range selection of ± 10 V or 0 to 10 V
- 4-bit digital output for CRT control signals intensity, blank, unblank, erase

SPECIFICATIONS

Identification	A6006
Size	Dual-height: 13.16 cm × 21.6 cm (5.18 in × 8.5 in)
Power	+5.0 V ±5% at 2.5 A
Bus loads	
AC	0.9
DC	1.0
D/A Resolution	12-bit
Number of D/A converters	4
Digital input	12-bits (binary encoded for unipolar output; offset binary for bipolar mode)

AAV11-C

Digital storage	Four separate Read/write DAC registers for word or byte storage
Analog Output Voltage	± 10 V @ 10 mA; 0 V to 10 V @ 10 mA
Gain accuracy	Adjustable to (-) full-scale value
Gain drift	± 30 PPM per °C, max.
Offset drift	± 15 PPM per °C, max.
Offset error	Adjustable to zero
Linearity (0-10 V)	± ½LSB; ± 1.2 mV at full-scale range
Differential linearity	± ½LSB
Output impedance	0.5 ohm
Output current	10 mA @ 10 V min.
Settling time	6μs to 0.1% for a 20 V p-p output change
I/O connector	20 pins; 3M no. 3421-7020

CONFIGURATION

The physical layout of the AAV11-C is shown in Figure 1. The AAV11-C has switches and two jumpers to set up the device address. The board also has jumpers to select the output voltage range for unipolar and bipolar operation. The following paragraph describes in detail the procedure for setting up the circuit board.

Device Select Addressing

The AAV11-C device address is the I/O address assigned to the first of four DAC registers. The user selects the device address via a switch pack for address bits DAL 3-10 and two jumpers for bits DAL 11 and DAL 12. The device address can range from 160000_8 to 177770_8 in increments of 10_8. The device address is usually set at 170440_8. This is shown in Figure 2. A switch in the ON position represents a 0; a switch in the OFF position represents a 1. Jumper A11 is installed to place a 0 at address bit DAL 11. Jumper A12 is removed to place a 1 at address bit DAL 12.

AAV11-C

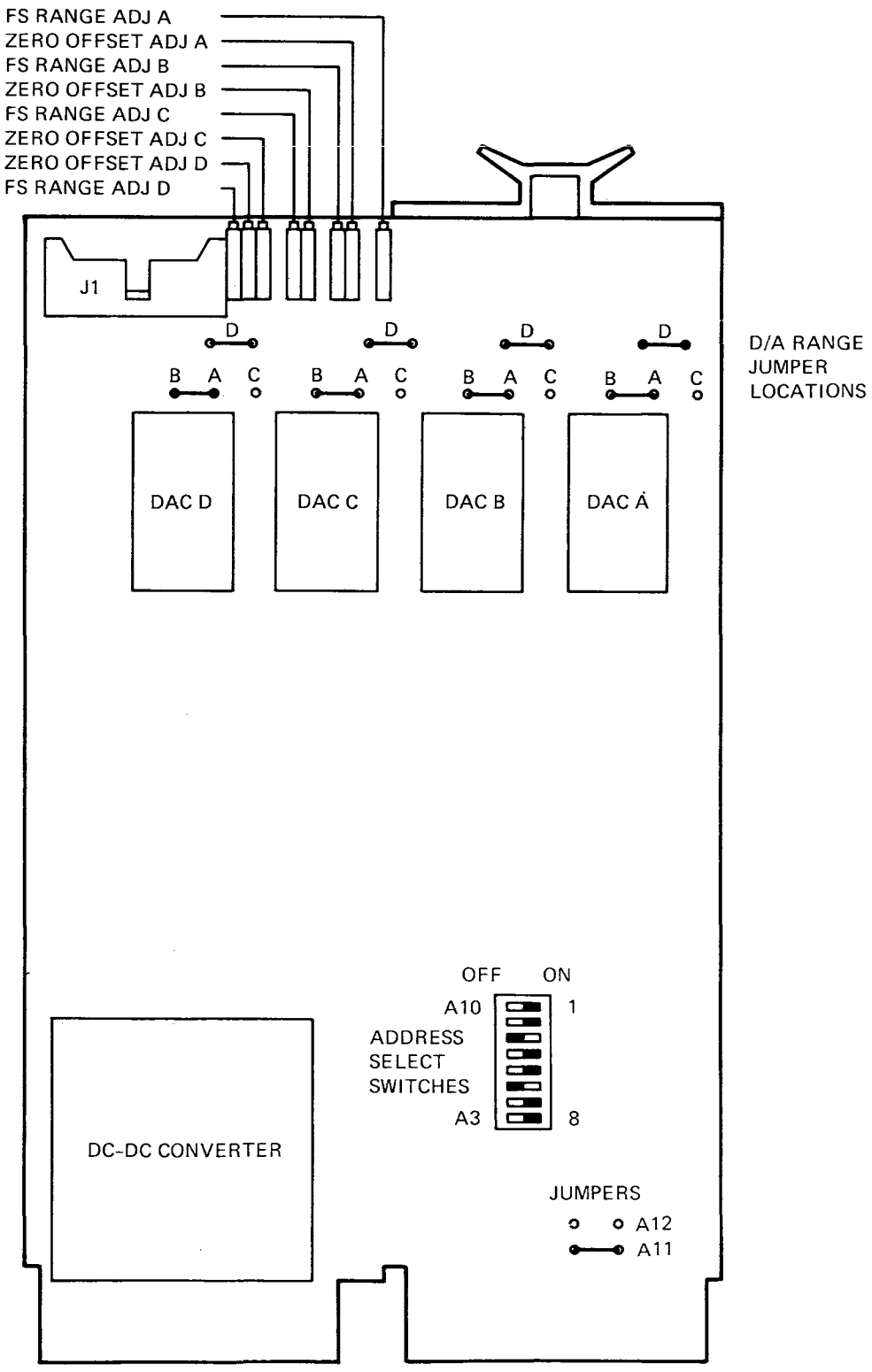


Figure 1 AAV11-C Physical Layout

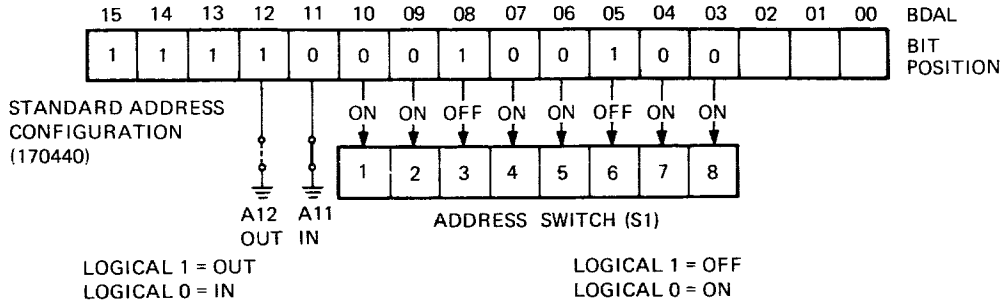


Figure 2 Selecting AAV11-C Device Address

Output Voltage Range Selection

Each DAC on the AAV11-C has separate voltage range jumpers. These jumpers are found above their corresponding D/A converter IC on the printed circuit board (See Figure 1). When sent from the factory, the AAV11-C has a voltage range selected for all four DACs of bipolar ± 10 V. Table 1 shows the jumpers to install to select the output voltage range. The output of the board can be configured for either straight binary notation for unipolar operation or offset binary notation for bipolar operation. The expected output values are shown in Table 1.

Table 1 AAV11-C Output Voltage Range Jumpers

Polarity	Output Voltage Range	Install Jumpers	Notation	Input Code (Octal)	Output Value
Unipolar	0 to + 10 V	A to C	Binary	000000	+ full scale
				007777	0 V
Bipolar	± 10 V	A to B: D	Offset binary	000000	+ full scale
				004000	0 V
				007777	− full scale

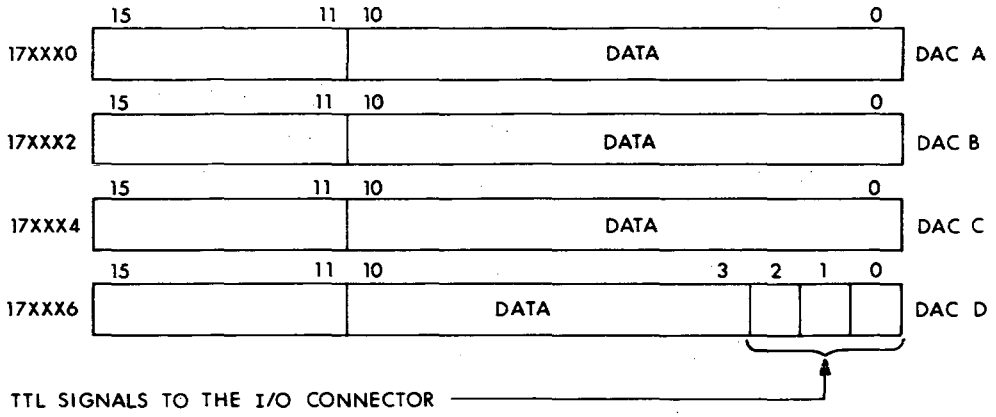


Figure 3 AAV11-C DACs

PROGRAMMING

The AAV11-C has four addressable read/write registers. Each register is used by one of four digital-to-analog converters and can be addressed as one word or two bytes, allowing complete use of the LSI-11 instruction set. The AAV11-C device address is the base address of the first register, usually 170440_8. The other registers are addressed in increments of 2_8 above the base address.

Interfacing to the AAV11-C

Figure 1 shows the location of the connectors on the AAV11-C. DAC inputs and control signal inputs enter the board via the LSI-11 bus connectors. Analog output voltages and digital control signals leave the board via the top edge connector J1. Table 2 shows the signal names on this connector. Each DAC has one output and a corresponding analog ground pin. The four least significant bits of DAC D (D00, D01, D02, and D03) are used for control signals to an analog device. These four bits are TTL-compatible.

Figure 4 shows how the AAV11-C is connected to a device that uses differential analog inputs and one control input. Both the AAV11-C and the analog device must be set up for electrical compatibility. The device manual should define which pins to attach to the AAV11-C control bits. The software enables or disables the control bits.

Table 2 AAV11-C Connector J1 Pin Assignments

Pin	Signal	Pin	Signal
1	D00 H	2	DGND
3	D01 H	4	DGND
5	D02 H	6	DGND
7	D03 H	8	DGND
9		10	
11	AGND	12	AGND
13	DAC D OUT	14	AGND
15	DAC C OUT	16	AGND
17	DAC B OUT	18	AGND
19	DAC A OUT	20	AGND

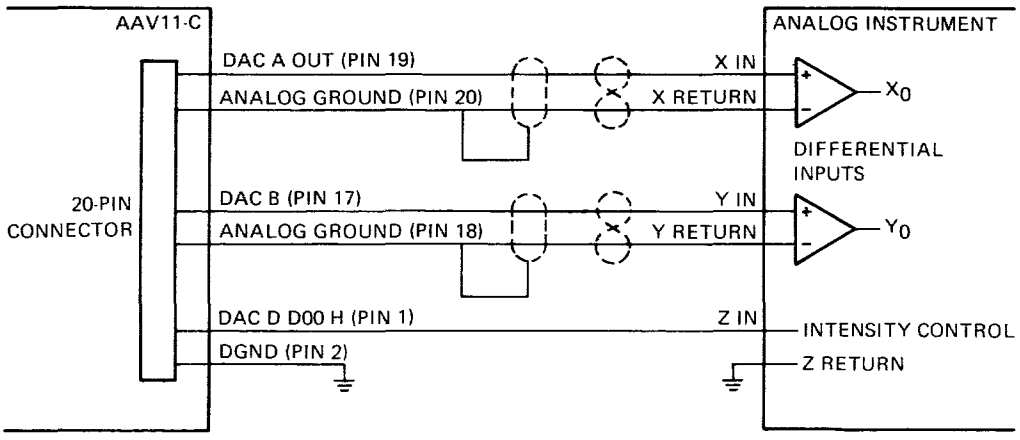


Figure 4 Connecting AAV11-C to a Differential Input Device

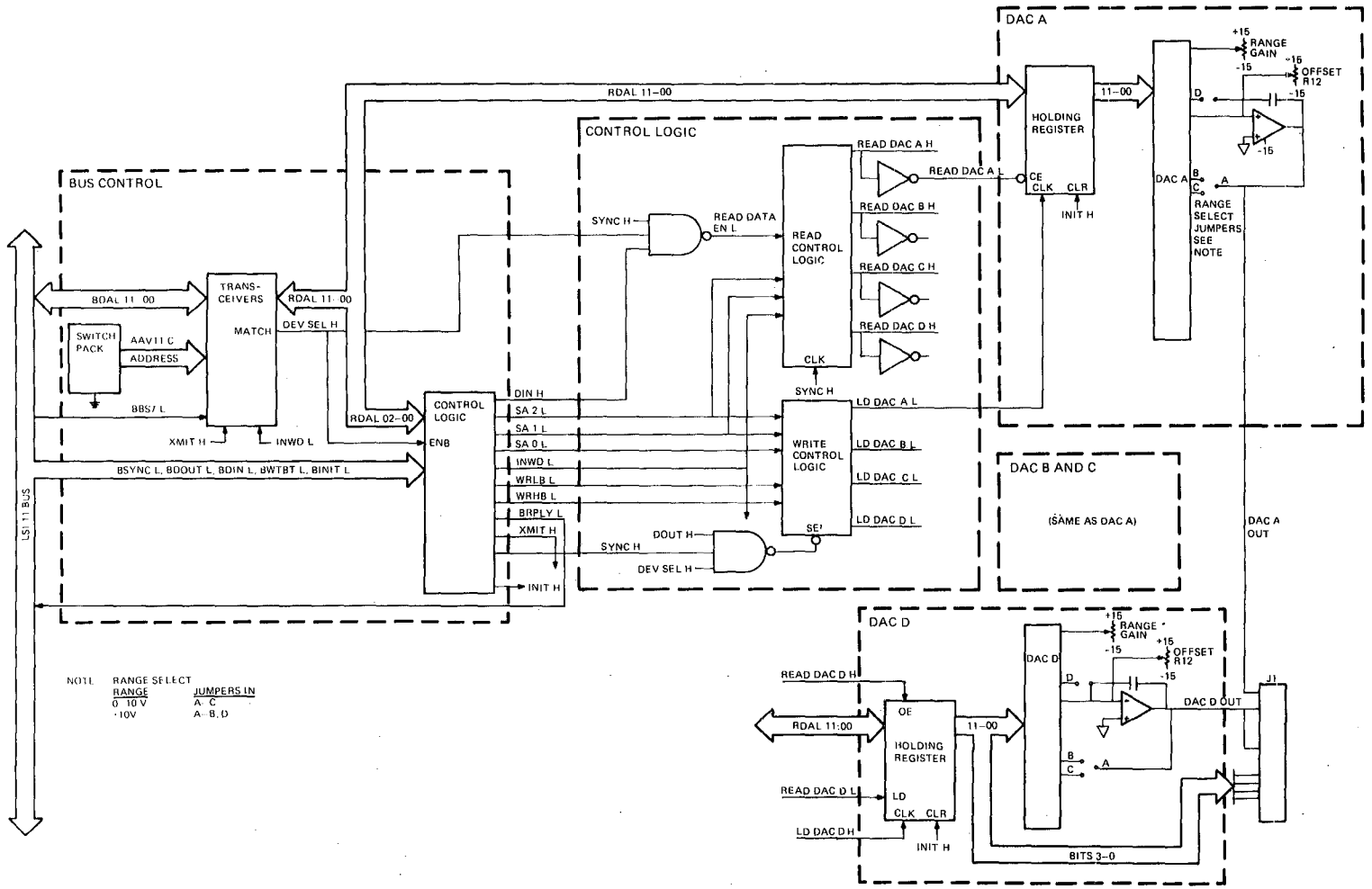


Figure 5 AAV11-C Block Diagram

AAV11-C

DESCRIPTION

Illustrated in Figure 5 is the block diagram of the AAV11-C. It is addressable from the LSI-11 bus at its interface transceivers. An address switch pack determines the device address of the board. Setting the address switch pack is described in the Configuration section of the discussion on this interface.

Binary data is written to these registers to be converted to an analog voltage. BDAL 000-11 becomes RDAL 00-11 within the AAV11-C. This is the input to the holding register of the DAC selected. LD DAC A, B, C, or D clocks the data into the DAC register.

DAC A, B, AND C

Digital-to-analog conversions are performed in each of three DACs by identical circuits. A fourth DAC is slightly different. The first three DACs have a holding register to store the digital input, a DAC IC that generates a current to the input of the amplifier (the current is a function of the value in the holding register and the range select jumpers), and an amplifier that changes its input current into a voltage proportional to its input. The fourth DAC performs a function similar to the other three DACs, but can also supply TTL-compatible signals for output to external logic.

Each DAC has an offset potentiometer to adjust the amplifier to negative full-scale range and a range gain potentiometer to adjust for positive and negative full-scale range.

DAC D

The DAC D is identical to the DAC A, B, and C except that bits 0-3 from its holding register go to the I/O connector and to the DAC IC. These bits can be used for external equipment that needs control signals at programmable times.

Control signals in these bits will affect any D/A conversions that occur at the same time using DAC D.

ADV11-A

ADV11-A ANALOG TO DIGITAL CONVERTER

INTRODUCTION

The ADV11-A is a 12-bit successive approximation analog-to-digital converter that samples analog data at specified rates and stores the digital equivalent value for processing. A multiplexer section can accommodate up to 16 single-ended or 8 quasi-differential inputs. The converter section uses a patented auto-zeroing design that measures the sample data with respect to its own circuitry offset and therefore cancels out its own offset error.

A/D conversions are initiated by program command, clock overflow, or external events. The program control is determined by the control and status register (CSR). The clock overflow command is supplied by the KWV11-A option. External event inputs can originate at the user's equipment or from the Schmitt trigger output on the KWV11-A clock. The digital data output is routed through a buffer register to the bus, from which it can be transferred into memory. This buffer optimizes the throughput rate of the converter.

Three reference signals are provided for selftesting on any channel input: two dc levels and one bipolar triangular waveform. This output can be used with DIGITAL diagnostic software to produce a database for extremely thorough and precise analog linearity testing.

FEATURES

- 16-channel multiplexer
- Sample-and-hold functions
- Autozeroing technique
- Buffered data output
- Selftesting features

SPECIFICATIONS

Identification	A012
Type	Quad
Power	+5 Vdc ±5% at 2.0 A +12 Vdc ±3% at 450 mA
Bus Loads	
ac	3.25
dc	1

ADV11-A

Inputs

Analog input protection	Fusible resistor guaranteed to open at ±85 V within 6.25 seconds. Guaranteed not to open from −25 V to +20 V at the input. Overload affects no components other than the fusible resistor on the overloaded channel; no other channels are affected.
Logic input protection	Fusible resistor guaranteed to open at ±25 V within 6.25 seconds. Guaranteed not to open from −4 V to +9 V at the input.
Analog input full scale range (FSR)	10.24 V bipolar (−5.12 V to +5.12 V)
Analog input dynamic resistance (Vin ≤ 5.12 V)	100 MΩ minimum
Analog input bias current (Vin ≤ 5.12 V)	50 nA, maximum
Logic input voltages	Low = 0.0 to +0.7 V High = +2 V to +5 V
Logic input currents	Low = −6.8 mA at 0 V High = +1.3 mA at +5 V
Logic input rise/fall time	400 ns maximum

Coding

A/D Converter	
Resolution	12 bits, binary-weighted (2.5 mV nominal)
Format	Parallel offset binary, right-justified
	Input Voltage
	+FS-1 LSB
	0
	−FS
	Output Code
	7777
	4000
	0

	(FS = 5.12 V; 1 LSB = 2.5 mV)
Vernier D/A Resolution	8 bits, binary weighted
Format	Offset binary encoded
	Input Code 377 200 0
	Approximate Offset Voltage +2.5 A/D LSB (+6.4 mV) 0 −2.5 A/D LSB (−6.4 mV)
Performance	
Gain error	Adjustable to zero
Offset error	Adjustable to zero
Differential linearity	No skipped states; no states wider than 2 LSB. 99% of state widths ±½ LSB
Integral linearity	±1 LSB, maximum non-linearity (referenced to end points)
Temperature coefficients	Gain = 6 PPM per °C Linearity = 2 PPM of full-scale range per °C Offset = 7.5 PPM of full-scale range per °C
Noise	Module = 0.4 LSB rms; 2 LSB peak System = 0.5 LSB rms; 2 LSB peak
Warm-up time	5 minutes, maximum
Timing	
External start	Low level pulse, 50 ns minimum to 10 μs maximum; conversion starts on leading edge

Synchronization	0 to T
Conversion time	16 T (T = Clock period = 2 μs)
Transition interval (reacquisition interval between end of conversion or channel change and start of new conversion)	9 μs

Test Signals

The ADV11-A provides three output voltages for test purposes:

1. Positive dc level, +4.4 V (±15%)
2. Negative dc level, −4.4 V (±15%)
3. Triangular wave, 15 Hz nominal (±15%)

CONFIGURATION

This section describes how the user can configure the module to function within the system by setting dip switches S1 and S2 (Figure 1) to obtain the desired device address and interrupt vector as described in Table 1. When a jumper wire is inserted between the lugs, the single-ended inputs (16 channels) are selected. When the wire is removed, quasidifferential inputs are selected.

ADV11-A

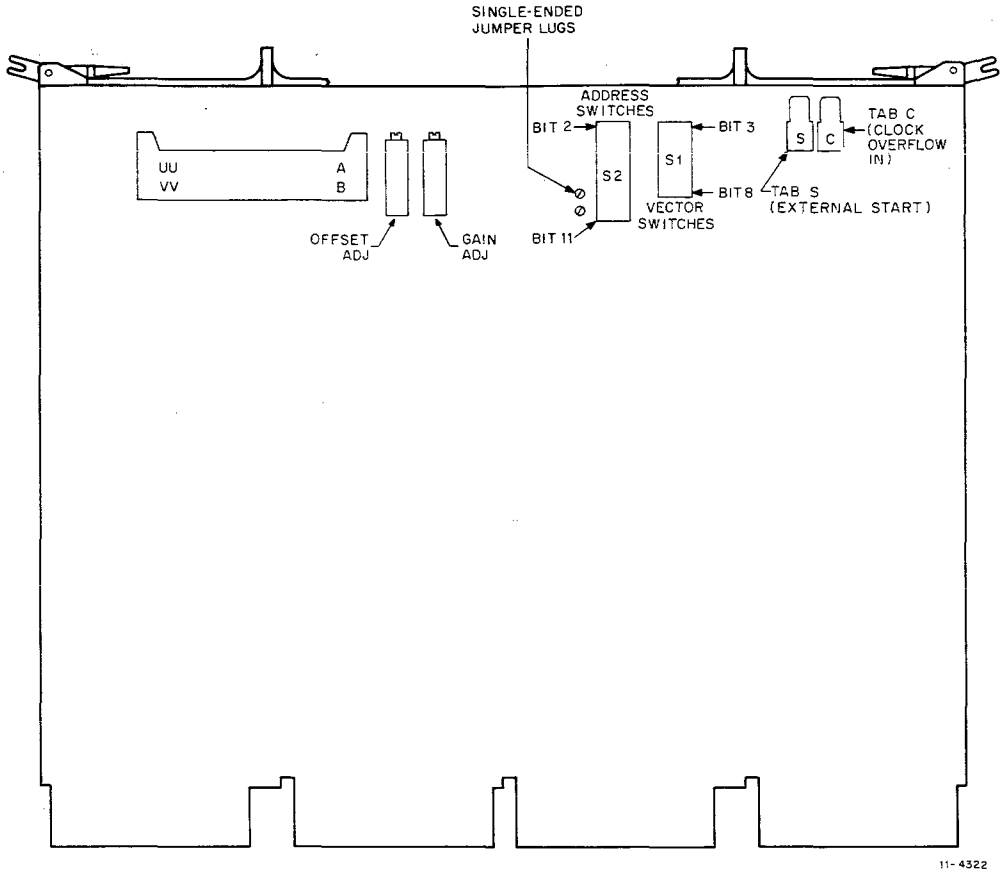


Figure 1 ADV11-A Connectors and Switches

Table 1 Standard Assignments

Description	Mnemonic	First Module Address	Second Module Address
Registers			
Control and Status	CSR	170400	170420
Data Buffer	DBR	170402	170422
Interrupt Vectors			
Conversion Complete		400	410
Error		404	414

Registers

The control and status register (CSR) address can be selected in the range of 170000 to 177774 by using the S2 dip switch as shown in Figure 2. Switch S2 is factory-set at 170400, which is the recommended address as illustrated in Figure 2. The functions of the CSR bits are shown in Figure 3 and detailed in Table 2.

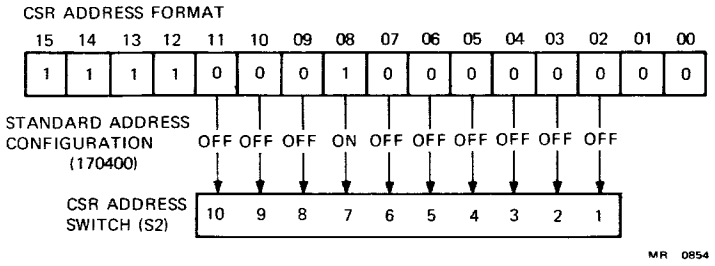


Figure 2 CSR Switch-Selectable Address

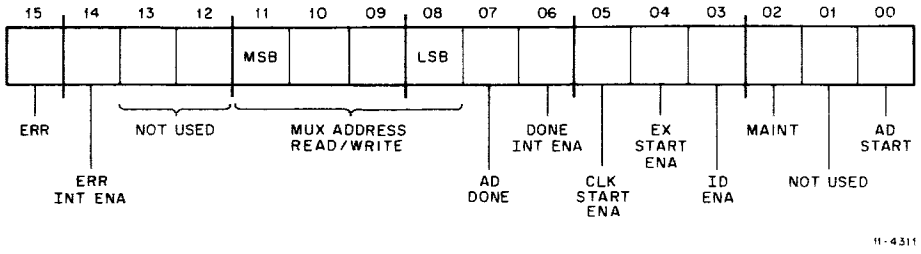


Figure 3 CSR Bit Format

Table 2 DBR Bit Functions

Bit	Function
Read-Only	
15-13	Not used. Should read as 0.
12	ID—When ID Enable (bit 3) of the CSR has been set, DBR bit 12 will be set to 1 at the end of the conversion.
11-0	Converted Data—These bits contain the results of the last A/D conversion.
Write-Only	
15-8	Not used.
7-0	Vernier D/A—These bits provide a programmed offset to the converted value (scaled 1 D/A LSB = 1/50 A/D LSB). The hardware initializes this value to 200_8 (midrange). Values greater than 200_8 make this input voltage appear more positive.

Vector Interrupt

The A/D conversion complete interrupt vector is set by dip switch S1 (Figure 1). Any address in the range of 000_8 to 777_8 can be selected by the user. The switch is factory-configured for 400_8, the recommended vector, as shown in Figure 4. The error interrupt vector will be four words higher than the A/D conversion complete interrupt vector.

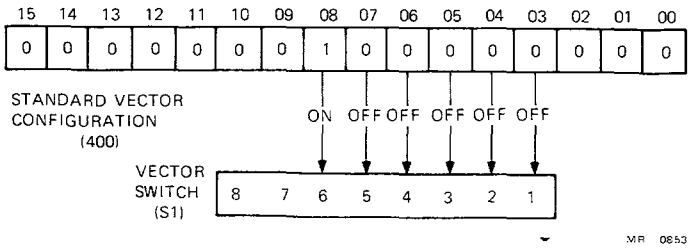


Figure 4 Interrupt Vector

Connections

Figure 5 illustrates the location of user connectors and switches on the component side of the ADV11-A board.

Analog input signals are input to the ADV11-A through the 40-pin connector. Pin assignments for the connector are shown in Figure 5. The proper H856-to-H856 cable is the BCO8R; The proper H856 to prepared open-ended cable is the BCO4Z.

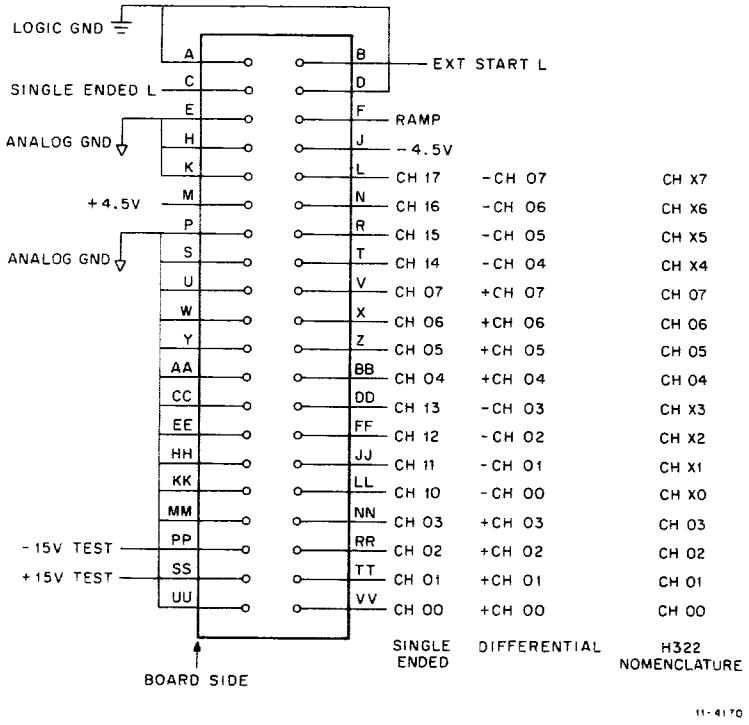


Figure 5 ADV11-A 40-Pin Connector Pin Assignments

ADV11-C

ADV11-C ANALOG-TO-DIGITAL CONVERTER

INTRODUCTION

The ADV11-C is an LSI-11 analog input printed circuit board that performs analog-to-digital conversions. A dual-height module, it can accept up to 16 single-ended inputs, or up to eight differential inputs, either unipolar or bipolar. A unipolar input can range from 0 Vdc to 10 Vdc. A bipolar input can range from – 10 Vdc to 10 Vdc. The ADV11-C also has a programmable gain on these inputs of 1, 2, 4, or 8 times the input voltage.

Analog-to-digital (A/D) conversions are started by a program command, an external trigger, or a realtime clock input. When the program command sets the A/D START bit in the control/status register, the ADV11-C will start the A/D conversion on the selected input channel. The ADV11-C changes the analog input into digital data. The digital data goes to the A/D data buffer register and waits for a programmed data transfer to the LSI-11 processor or memory, or the ADV11-C puts an interrupt request on the LSI-11 bus and waits for the interrupt request to be acknowledged.

FEATURES

- 16 single-ended analog input channels
- Eight differential analog input channels
- Software Programmable gain Amplifier with gains of 1, 2, 4, or 8
- 12-bit output data resolution
- Output data notation in binary, offset binary, or two's complement format
- A/D results can be received by a programmed I/O transfer or by servicing an interrupt request
- Interrupts can be enabled and automatically set by A/D DONE and/or ERROR flags

SPECIFICATIONS

Identification	A8000
Size	Dual-height: 13.16 cm × 21.6 cm (5.18 in × 8.5 in)
Power	+5.0 V ±5% at 2.0 A

ADV11-C

Bus loads	
AC	1.3
DC	1.0
I/O Connector	26 pins 3M no. 3399-7026

Inputs

Number of analog inputs	Eight channels using differential inputs, or 16 channels using single-ended inputs
Analog input range	0 V to +10 V −10 V to +10 V
Maximum input signal	±10.5 V (signal + common mode voltage)

Input impedance

Off channels	100 M ohm minimum in parallel with 10 pF maximum
On channels	100 M ohm minimum in parallel with 100 pF maximum
Power off	1 K ohm in series with a diode
Input protection	Inputs are current-limited and protected to ± 30 V overvoltage without damage
Input bias current	20 nA at 25° C (76° F), maximum

A/D Output

Data Buffer Register	16-bit read-only output register
Resolution	12-bit unipolar; 11-bit bipolar, plus sign
Data Notation	Binary, offset binary, or 2's complement
Sample and Hold Amplifier	
Aperture uncertainty	Less than 10 ns
Aperture delay	Less than 0.5μs from start of conversion to signal disconnect.

ADV11-C

Front end settling	Less than 15μs to ±0.01% of full-scale value for a 20 V p-p input.
Input noise	Less than 0.2 mV rms
A/D Converter Performance	
Linearity	±1/2 LSB
Stability (temperature coefficient)	±30 ppm/°C
Stability, long-term	±0.05% change per six months
System accuracy	Input voltage to digitized value ±0.03%
Conversion time	25μs from end of front end starting to setting the A/D DONE bit
System throughput	25K channel samples per second
Environment	
Temperature, operating	5°C to 60°C (41°F to 140°F)
Temperature, not operating	−40°C to 66°C (−40°F to 150°F)
Relative humidity, operating	10% to 95% with max. wet bulb of 32°C (90°F) and min. dew point of 2°C (35°F)not condensing

DESCRIPTION

Figure 1 shows a block diagram of the ADV11-C. It is addressed via the LSI-11 bus at its interface transceivers. The board has jumpers to select its device address. The ADV11-C has two programmable addressable registers: the Control/Status Register (CSR), which is a read/write, byte-addressable register, and the Data Buffer Register (DBR), a read-only, word-addressable register. The board also has jumpers to select the base interrupt vector. The ADV11-C has two interrupt vectors. One is enabled when A/D DONE is set in the CSR; the other may be enabled for an ERROR set in the CSR. The ERROR vector automatically receives the base interrupt vector address + 4. See the address and vector jumpers.

Once addressed, the transceivers send the bus data instruction to the CSR. The instruction selects one of 16 channels, determines the gain

selected (GS0, GS1), and determines how the board will start an analog conversion. An analog conversion can be started by a realtime clock input, by an external event trigger, or under program control by setting the A/D START bit in the CSR.

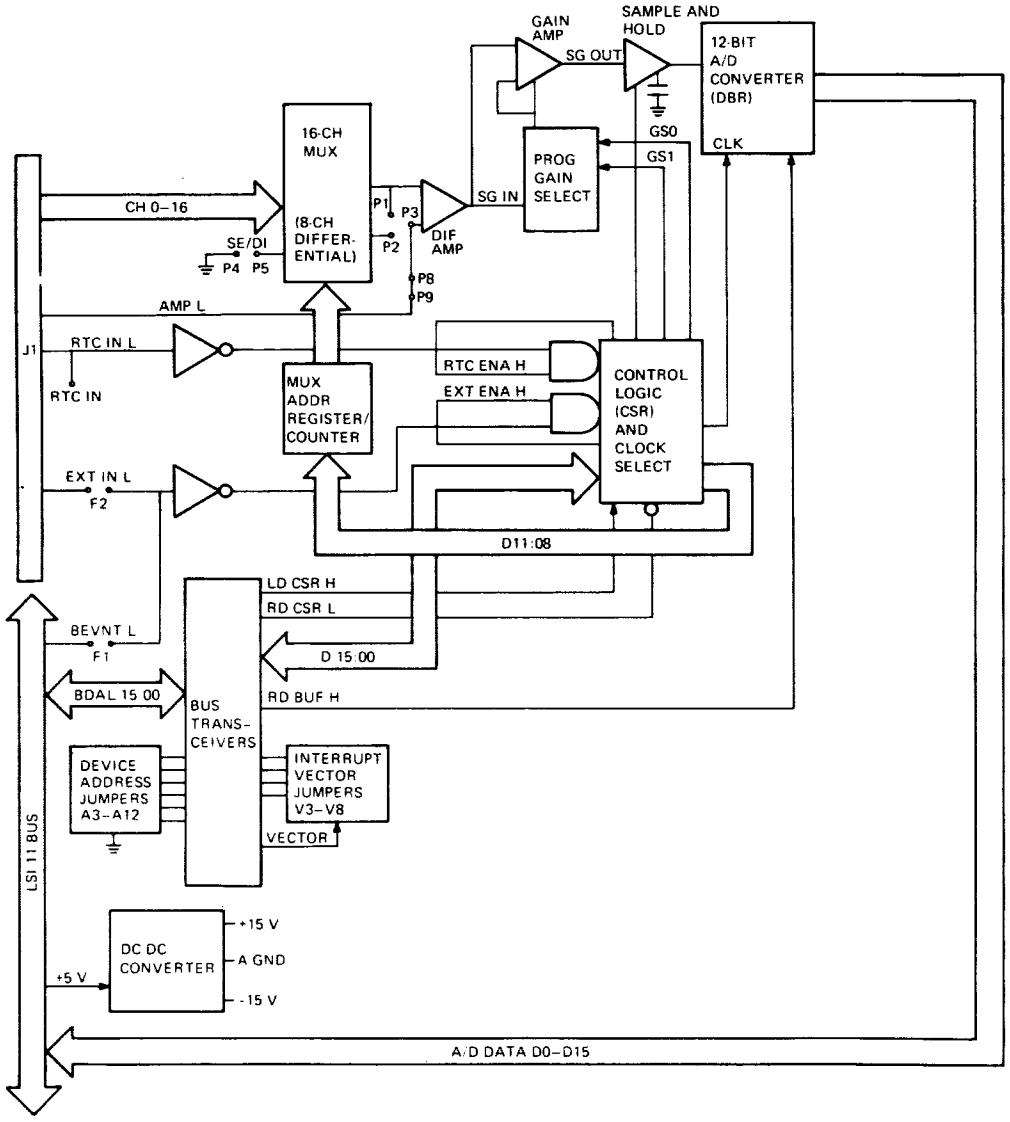


Figure 1 ADV11-C Block Diagram

One jumper (SE/DI) to the multiplexer determines whether the module uses single-ended or differential inputs. Two jumpers (F2, F1) determine whether the external trigger comes from the I/O connector (J1) or from the LSI-11 bus 50/60 Hz line input (BEVNT L).

The output of the multiplexer goes to a differential amplifier then to a programmable gain amplifier. Its gain is set by writing bits 2 and 3 in the CSR. The gain selected (GS0 and GS1) may be 1, 2, 4, or 8 times the input voltage.

The output of the programmable gain amplifier goes to a sample and hold amplifier, where the analog signal is continuously sampled until one of the following inputs is received.

- A/D START bit set in the CSR
- Realtime clock input at I/O connector or at pin RTC IN
- External event trigger input at I/O connector or at LSI-11 bus BEVNT line.

When one of these inputs has been received, the sample and hold amplifier switches to "hold," and the 12-bit A/D converter digitizes the held analog voltage.

When the A/D conversion is complete, the A/D DONE bit is set in the CSR, and the sample and hold amplifier returns to sampling. If the DONE INT ENABLE bit is also set, an interrupt occurs to the LSI-11 bus. When the interrupt is acknowledged, the data is read by reading the data buffer register (DBR).

PROGRAMMING THE ADV11-C REGISTERS

This section describes the mode of operation determined by setting bits in the CSR and defines the bits in both registers.

Selecting ADV11-C Mode of Operation

The user determines the mode of operation of the ADV11-C, and selects how the A/D conversions are to start and how the digital data is transferred to the LSI-11 processor.

Starting an A/D Conversion — An A/D conversion can be started in one of three ways.

1. Realtime clock input: Set bit 5 in CSR
2. External trigger enable: Set bit 4 in CSR
3. A/D START bit: Set bit 0 in CSR

Transferring Data to LSI-11 — The digital data can be transferred to the LSI-11 processor or memory by a programmed I/O transfer or by servicing an interrupt request.

Using LSI-11 instructions, a programmed I/O transfer can write the CSR in the ADV11-C, read the CSR, and wait for an A/D DONE bit (bit 7), then read the DBR to get the A/D data.

If interrupts are used, set interrupt enable bit (bit 6) of the CSR. When the A/D conversion is complete, the A/D DONE bit (bit 7) sets, and an interrupt occurs to the LSI-11 processor. The processor services the interrupt request and gets the A/D data. After receiving the data, the software clears the A/D DONE bit in the ADV11-C's CSR.

An interrupt may also be programmed to occur on an error condition by setting bit 14 in the CSR.

ADV11-C Standard Device Address

The ADV11-C permits assigning a device address between 160000_8 and 177770_8. The standard device address is 170400_8. This is the address for the control/status register. The data buffer register automatically receives the base address + 2, or 170402_8. Table 1 shows the standard address and interrupt vector address assignments.

ADV11-C Standard Interrupt Vector Address

The interrupt vector can be assigned between 0 and 770_8 in increments of 10_8. The standard base interrupt vector for the ADV11-C is 400_8. This vector is assigned to the A/D DONE interrupt request. If the DONE INT ENABLE bit (bit 6) is set in the CSR, the A/D DONE bit (bit 7) enables the interrupt request to the LSI-11 bus. When the interrupt request is acknowledged by the LSI-11 processor, the interrupt service routine is started at address 400_8.

The ADV11-C can also interrupt on an error. The error interrupt request is automatically assigned the base vector address + 4, or 404_8. If the ERROR INT ENABLE bit (bit 14) is set by the program, an interrupt request will occur at the occurrence of any error (bit 15 set).

The standard interrupt vector addresses are shown in Table 1.

Table 1 Standard Octal Address Assignments

Description	Mnemonic	First Module Address	Second Module Address
Registers			
Control /Status	CSR	170400	170420
Data Buffer	DBR	170402	170422
Interrupt Vectors			
A/D DONE		400	410
ERROR		404	414

Control/Status Register (CSR)

The control/status register is a read/write register, shown in Figure 2. A control instruction is written into the CSR; the A/D status is read from the CSR. The bit definitions are described in Table 2.

Data Buffer Register (DBR)

The data buffer register is a read-only register that holds the digital data after the A/D conversion is complete. The DBR can be read after the A/D DONE flag is set in the CSR register. The format for the DBR is shown in Figure 3. The bit definitions are described in Table 3. The A/D DONE flag is cleared after reading the register or on initializing the LSI-11 bus.

CONFIGURATION

The ADV11-C, shown in Figure 4, has jumpers to set up the device address, the interrupt vector address, and the analog configuration. The user may select the A/D input range, polarity, and the output data notation.

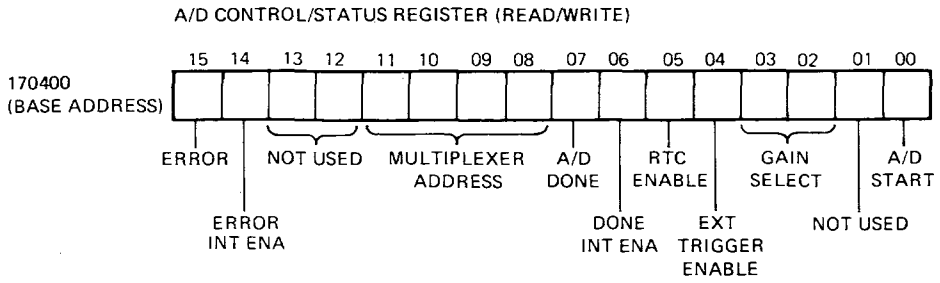


Figure 2 ADV11-C Control/Status Register (Read/Write)

Table 2 ADV11-C Control/Status Register Bit Assignments

Bit	Name	Description
0	A/D START	Write Only - When set, this bit starts an A/D conversion. This bit is cleared by internal logic after starting conversion. It always reads back 0.
1	Not used	
2, 3	GAIN SELECT	Read/Write - Set these bits to select the gain for the analog input as follows.
4	EXT TRIG ENABLE	Read/Write - When set, this bit allows an external trigger to start an A/D conversion.
5	RTC ENABLE	Read/Write - When set, this bit allows a realtime clock input to start an A/D conversion.
6	DONE INTERRUPT ENABLE	Read/Write - When set, this bit enables an interrupt on A/D DONE (bit 7). Both bits are cleared by INIT.
7	A/D DONE	Read Only - This bit is set at the end of an A/D conversion and is reset by reading the A/D data buffer register.
8-11	MULTIPLEXER ADDRESS	Read/Write - These bits select one of 16 analog input channels.

Gain	GS1 (bit 3)	GS0 (bit 2)
1	0	0
2	0	1
4	1	0
8	1	1

Bit	Name	Description
12-13	Not used	
14	ERROR	Read/Write - When set, this bit enables an interrupt on an ERROR (bit 15). Both bits are cleared by INIT.
15	ERROR INTERRUPT ENABLE	Read/Write - When set, this bit indicates that an error has occurred due to one of the following. • Trying an external start or clock start during multiplexer settling time. • Trying a start while an A/D conversion is in process. • Trying any start while the A/D DONE bit is set. This bit can be cleared by writing the CSR or by an INIT.

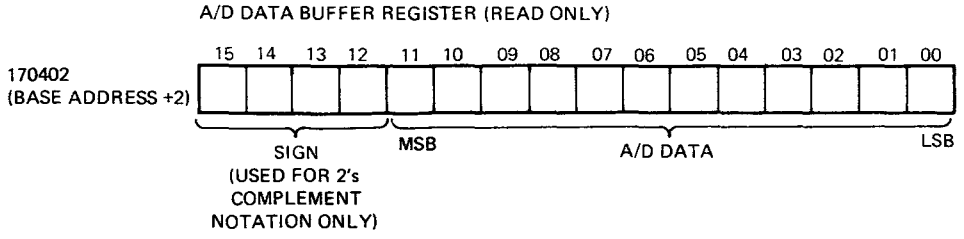


Figure 3 ADV11-C Data Buffer Register (Read Only)

There are two types of jumpers on the ADV11-C board. Some are point-to-point jumpers, in which each jumper pin has a unique number. A jumper is installed from one numbered pin to another. The other jumpers are pairs of pins. With each jumper type, a jumper wire is installed across a pair of pins.

This paragraph provides details on setting up the circuit board.

Table 3 ADV11-C Data Buffer Register Bit Assignments

Bit	Name	Description
0-11	A/D DATA	These bits hold the parallel digital output after completion of the A/D conversion in one of the following data notations. • binary • offset binary • 2's complement The user selects the data notation.
12-15	SIGN	These bits are the sign for the bipolar inputs when using 2's complement notation. These bits are not used for binary or offset binary notation.

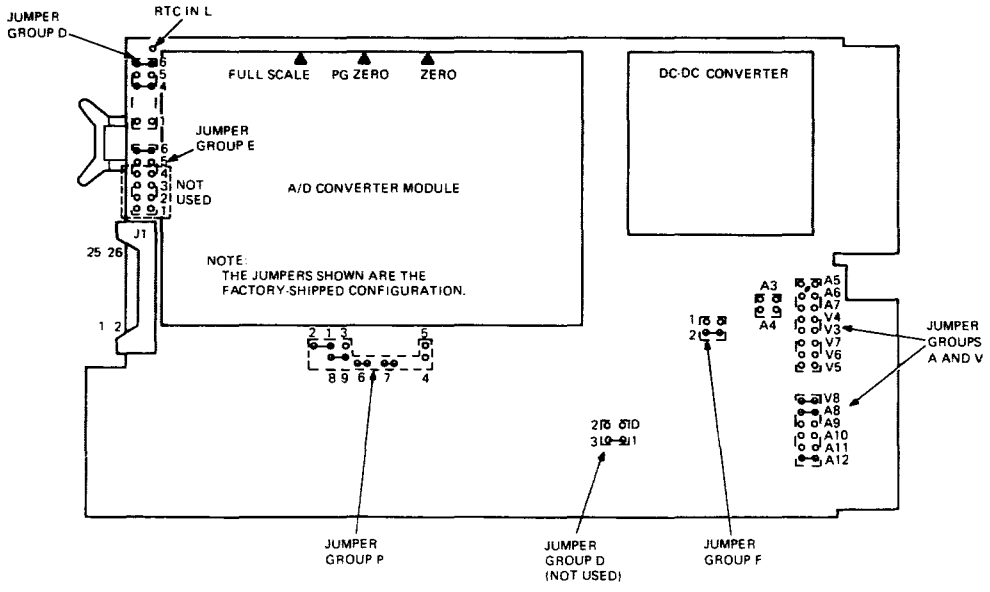


Figure 4 ADV11-C Physical Layout

Selecting ADV11-C Device Address

The ADV11-C device address is the I/O address assigned to the A/D control/status register. The device address is selected by means of jumpers A3 through A12. (See jumper groups A and V in Figure 4). The jumpers allow the user to set the device address within the range of 160000_8 to 177770_8 in increments of 10_8. The device address is usually set at 170400_8, as shown in Figure 5. A jumper installed decodes a 1 in the corresponding bit position; a jumper out decodes a 0.

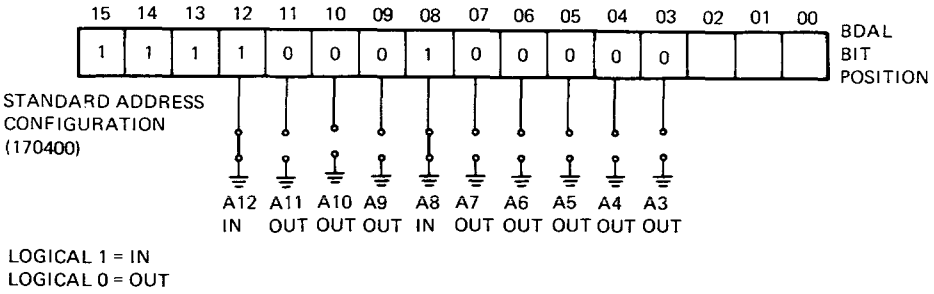


Figure 5 Selecting ADV11-C Device Address

Selecting ADV11-C Interrupt Vector Address

The ADV11-C is capable of generating two interrupt vectors to the LSI-11 processor. These interrupts, if enabled, occur when the A/D DONE bit or the ERROR bit is set in the CSR. The base interrupt vector address is assigned to A/D DONE. (The ERROR interrupt automatically is assigned the base interrupt vector address + 4.)

The base interrupt vector address can be set within the range of 0 to 770_8, in increments of 10_8. It is usually set to 400_8 by jumpers V3 through V8, as shown in Figure 6. (See jumper groups A and V in Figure 4).

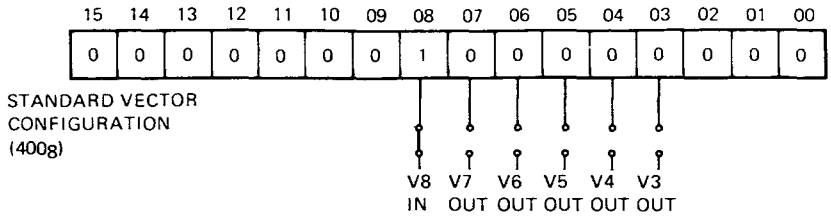


Figure 6 Selecting ADV11-C Interrupt Vector Address

Selecting ADV11-C Analog Input Range, Type, and Polarity

The ADV11-C allows software control over the full-scale range selection. The effective ranges provided by the programmable gain are as follows:

Gain	Unipolar	Bipolar
1	0 V to +10 V	±10 V
2	0 V to +5 V	±5 V
4	0 V to +2.5 V	±2.5 V
8	0 V to 1.25 V	±1.25 V

Table 4 shows the jumpers that must be installed to set up the analog input type. The board comes from the factory set for 16-channel single-ended, bipolar inputs. Refer to jumper group P in Figure 4.

Table 4 Selecting ADV11-C Analog Input Type

Input Type	Install Jumpers
Single-Ended Inputs*	P1 to P2; P8 to P9
Differential Inputs	P2 to P3; P4 to P5

* Factory configuration

NOTE

Jumpers P6 and P7 are factory installed for the programmable gain feature and should be left in.

Selecting ADV11-C A/D Output Data Notation

The ADV11-C allows the user to select the data notation to be used for the A/D output, as either binary, offset binary, or 2's complement notation. Table 5 shows the jumpers that must be installed to select the data notation. Refer to jumper groups D and E near the handle of the board, shown in Figure 4.

Table 5 Selecting A/D Output Data Notation

A/D Output Data Notation	Jumpers 1D	4D	5D	6D	5E	6E	Input Voltage	Output Code (Octal)
Binary	IN	OUT	OUT	IN	OUT	IN	+ full scale	007777
							0 V	000000
Offset binary*	OUT	IN	OUT	IN	OUT	IN	+ full scale	007777
							0 V	004000
							— full scale	000000
2's Complement	OUT	IN	IN	OUT	IN	OUT	+ full scale	003777
							0 V	000000
							— full scale	174000

* Factory configuration

Selecting Source of External Trigger

The A/D conversions within the ADV11-C can be started in one of the following three ways:

1. Under program control, using the A/D START bit in the CSR.
2. By a realtime clock input at J1 pin 21 or at pin RTC IN.
3. By an external trigger, either at J1 pin 19 or at the BEVNT line on the LSI-11 bus.

The user can select the source of the external trigger using two jumpers on the board. (See jumper group F in Figure 4.) Table 6 shows the jumpers to install to select the source of the external trigger.

Table 6 Selecting ADV11-C External Trigger

	Jumpers	
External Trigger Source	**F1**	**F2**
BEVNT line (LSI-11 bus)	IN	OUT
EXT TRIG IN (J1 pin 19)	OUT	IN

INTERFACING TO THE ADV11-C

Figure 4 shows the location of the I/O connector J1 on the ADV11-C. Analog input signals enter the board through this connector. Up to 16 single-ended analog inputs can be connected to J1 (CH 0-CH 15), or up to 8 differential analog inputs can be connected to J1 using CH 0-CH 7

and RETURN 0-7. A realtime clock input and an external trigger can also be connected to J1. Under program control, the clock or external trigger can be enabled to start an A/D conversion. The pin assignments for J1 are shown in Table 7.

The ADV11-C has two bus interface connectors that plug into the LSI-11 bus. These connectors have signals defined by LSI-11 bus specifications.

Single-Ended Inputs (16 Channels)

Single-ended analog inputs have one side of the user's analog source connected to the A/D converter amplifier and the other side connected to ground, as shown in Figure 7.

The benefit of single-ended inputs is that the user gets twice as many channels as in a differential input system. The disadvantage is the loss of the common mode rejection that is available with a differential system. Therefore, the recommended analog inputs are as follows:

- Input level: High, more than 1 V
- Input cable lengths: Short, less than 4.5 m (15 ft)

The user's source may be positioned some distance from the computer, and a voltage difference may occur between the user's source ground and the computer ground. This ground voltage difference (V_N) is included in the signal received by the A/D converter. To decrease this ground difference, plug the user's device into an ac receptacle as close as possible to the one providing power to the computer.

Table 7 ADV111-C Connector J1 Pin Assignments

Pin	Signal Name	Pin	Signal Name
1	CH 0	2	CH 8 or RETURN 0
3	CH 1	4	CH 9 or RETURN 1
5	CH 2	6	CH 10 or RETURN 2
7	CH 3	8	CH 11 or RETURN 3
9	CH 4	10	CH 12 or RETURN 4
11	CH 5	12	CH 13 or RETURN 5
13	CH 6	14	CH 14 or RETURN 6
15	CH 7	16	CH 15 or RETURN 7

Pin	Signal Name	Pin	Signal Name
17	A GND	18	AMP L
19	EXT TRIG IN L	20	D GND
21	RTC IN L	22	D GND
23	—	24	A/D REF
25	—	26	A/D REF

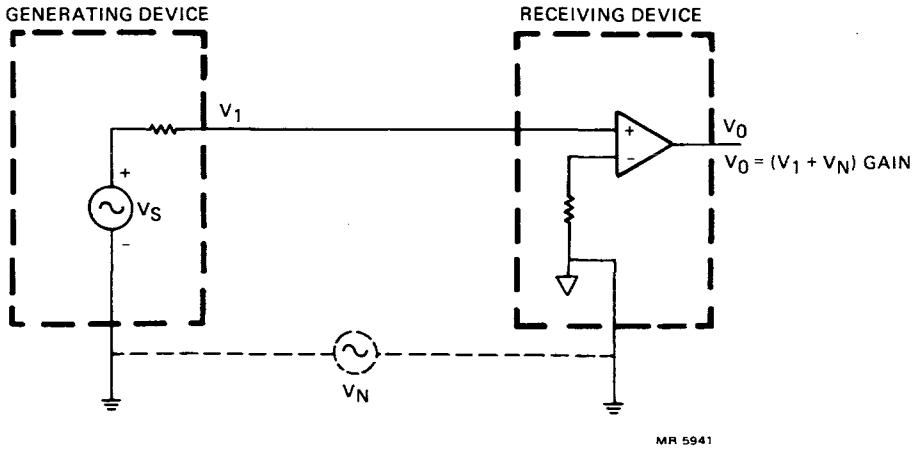


Figure 7 Single-Ended Analog Input

NOTE

Do not run a wire from the user's ground to the ADV11-C analog ground, since this wire forms a path for ground loop current that can affect the results on all input channels.

Floating input lines can be created by connecting the common side of the user's devices to the analog ground input on the ADV11-C (J1 pin 17). The ground point is shared among the channels. The signal return path from the A/D converter does not result in a current loop with the device ground.

Pseudo-Differential Inputs (16 Channels)

A pseudo-differential analog input system can be created by connecting all input sensors referenced to a common point, such as AMP L, as

shown in Figure 8. This is possible because AMP L is an input at connector J1 (pin 18) for user connection. The input amplifier rejects the common mode noise. The recommended analog inputs are as follows:

- Input range: 100 mV to 10 V
- Input cable lengths: Less than 7.5 m (25 ft)

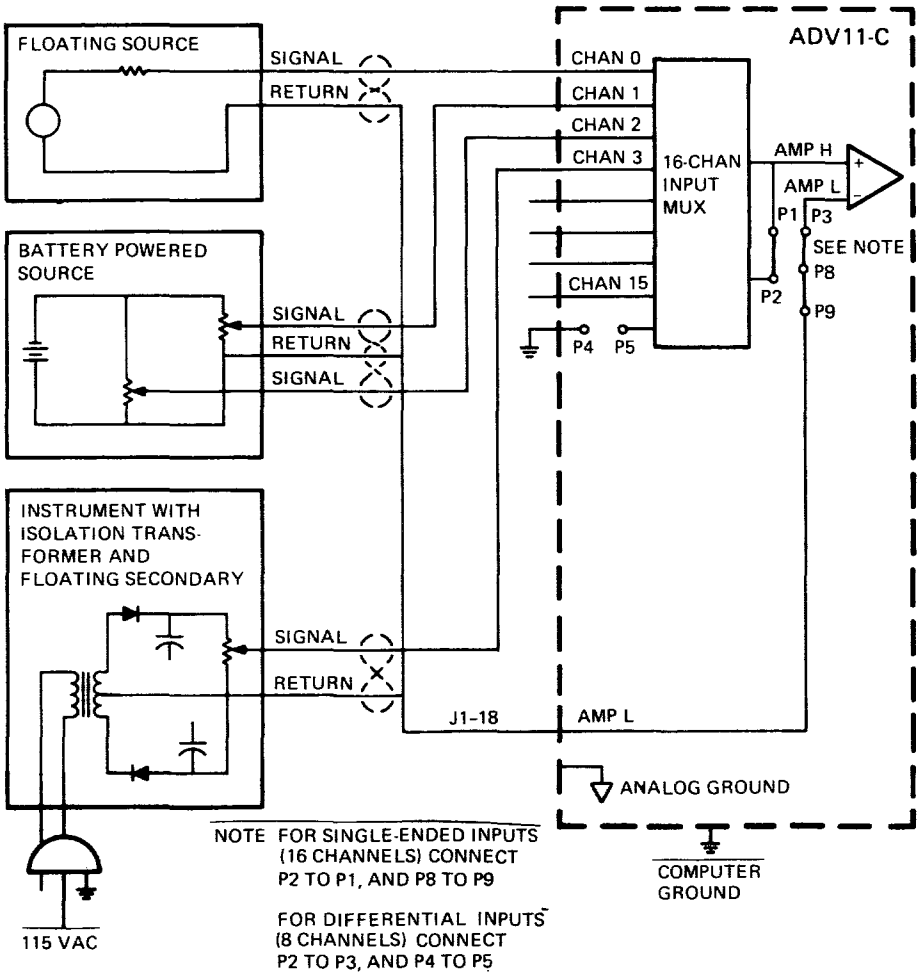


Figure 8 Pseudo-Differential Inputs

Differential Inputs (8 Channels)

Differential inputs have one side of the generating source connected to the positive (+) input of the A/D input amplifier and the other side of the source connected to the negative (−) input of the amplifier, as shown in Figure 9.

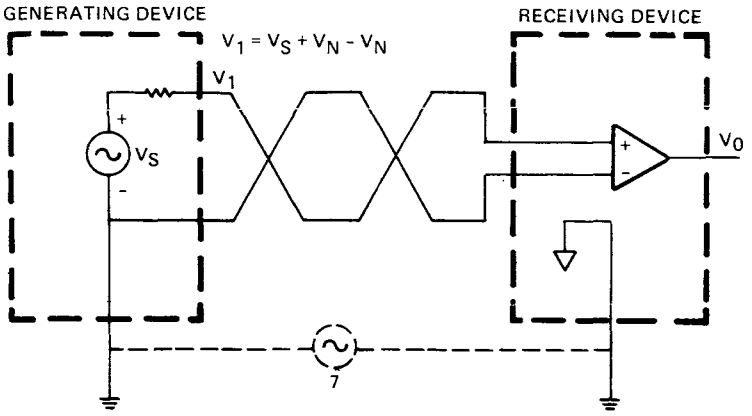


Figure 9 Differential Inputs

The benefit of differential inputs is that noise voltages appearing at the same time on both sides of the source are rejected by the A/D input amplifier. This is called common mode rejection, and provides a system with low noise. The amount of noise rejection is a ratio, the common mode rejection ratio (CMRR), given in decibels (dB). The CMRR for the ADV11-C is 80 dB at full-scale range.

The disadvantage of differential inputs is that the number of available input channels is lowered by half.

The recommended analog inputs are as follows:

- Input range: 10 mV to 10 V
- Input cable length: As needed by user
- Cable type: Twisted-pair, shielded lines with low impedance

AXV11-C ANALOG INPUT/OUTPUT BOARD

INTRODUCTION

The AXV11-C is an LSI-11 analog input/output printed circuit board, A0026. The board accepts up to 16 single-ended inputs, or up to 8 differential inputs, either unipolar or bipolar. A unipolar input can range from 0 V to + 10 V. A bipolar input can range from – 10 V to + 10 V. The AXV11-C has a programmable gain on these inputs of 1, 2, 4, or 8 times the input voltage.

A/D conversions can be started by a program command, an external trigger, or a realtime clock input. The AXV11-C changes the analog input into digital data at its output. The digital data waits for a programmed data transfer to the LSI-11 processor or memory, or the AXV11-C puts an interrupt request on the LSI-11 bus and waits for the request to be acknowledged.

The AXV11-C also has two separate digital-to-analog converters (DACs). Each DAC has a write-only register that provides 12-bit input data resolution. On receiving the data, the AXV11-C changes the data to an analog output voltage.

FEATURES

- 16 single-ended analog input channels or 8 differential analog input channels; SE/DI jumper is field-selectable.
- Programmable gain of 1, 2, 4, or 8.
- 12-bit output data resolution.
- Output data notation in binary, offset binary, or 2's complement format.
- A/D conversions can be started by a program, an external trigger, or a realtime clock.
- A/D results can be received by a programmed I/O transfer or by servicing an interrupt request.
- Common mode rejection ratio of 80 dB at maximum range.
- Two D/A converters (DACs).
- 12-bit digital input to each DAC.
- Each DAC has a unipolar or bipolar output.
- Output voltage range selection of ± 10 V or 0 V to 10 V.

AXV11-C

SPECIFICATIONS

Identification	A0026
Power Requirements	+5 V (±5%) @ 2.0 A
Bus Loads	
DC bus loads	1
AC bus loads	1.3
I/O Connector	26 pins; 3M no. 3399-7026
Analog Input	
No. of analog inputs	8 channels using differential inputs, or 16 channels using single-ended inputs
Input range	0 V to +10 V; −10 V to +10 V
Input gain (programmable)	**Gain (±0.05%) Range** 1 10 V 2 5 V 4 2.5 V 8 1.25 V
Maximum input signal	10.5 V (signal + common mode voltage)
Input impedance	
Off channels	100 MΩ in parallel with 10 pF max
On channels	100 MΩ in parallel with 100 pF max
Power off	1 kΩ in series with a diode
Input bias current	20 nA @ 25° C, max
Common mode rejection ratio	80 dB at 10 V full-scale range at 60 Hz
A/D Output	
Data buffer register	16-bit read-only output register
Resolution	12-bit unipolar; 11-bit bipolar plus sign

Data notation	Binary, offset binary, or 2's complement

Coding

Notation Used	Full-Scale Input Voltage	Output Coding Code (Octal)
Binary	+9.9976 V	007777
	0.0000 V	000000
Offset binary	+9.9951 V	007777
	0.0000	004000
	−10.0000 V	000000
2's complement	+9.9951 V	003777
	0.0000 V	000000
	−10.000 V	174000

Sample and Hold Amplifier

Aperture uncertainty	Less than 10 ns
Aperture delay	Less than 0.5μS from start of conversion to signal disconnect.
Front end settling	Less than 15μS to ±0.01% of full-scale value for a 20 V p-p input
Input noise	Less than 0.2mV rms

A/D Converter Performance

Linearity	±1/2 LSB
Stability (temperature coefficient)	±30 ppm/°C
Stability, long-term	±0.05% change per 6 months
Conversion time	25μS from end of front end starting to setting the A/D DONE bit
System throughput	25K channel samples per second
System accuracy	Input voltage to digitized value ±0.03%

AXV11-C

D/A Converter Specifications

No. of D/A converters	2
Digital input	12 bits (Binary code is used for unipolar output; offset binary or 2's complement code is used for biplar output)
Analog output	±10 V or 0 V to +10 V
Output current	±5 mA max
Output impedance	0.1 Ω
Differential linearity	±1/2 LSB
Non-linearity	0.02% of full-scale value
Offset error	Adjustable to zero
Offset drift	±30 ppm/°C max
Gain accuracy	Adjustable to full-scale value
Gain drift	±30 ppm/°C max
Settling time	65μS to 0.1% for a 20 V p-p output change
Noise	0.1% full-scale value
Capacitive load capability	0.5μF

Environment

Temperature, operating	5°C to 60°C (41°F to 140°F)
Temperature, not operating	−40°C to 66°C (−40°F to 150°F)
Relative humidity, operating	10% to 95% with max. wet bulb of 32°C (90°F) and min. dew point of 2°C (35°F)not condensing

DESCRIPTION

Figure 1 shows a block diagram of the AXV11-C. The board has jumpers to select its device address. It has four addressable registers: the control/status register (CSR), the data buffer register (DBR), DAC A

register, and DAC B register. The board also has jumpers to select the base interrupt vector address. The AXV11-C has two interrupt vectors. One is enabled when A/D DONE is set in the CSR; the other may be enabled for an ERROR set in the CSR.

A/D Conversion

When the AXV11-C is addressed, the transceivers send the instruction from the LSI-11 processor to the CSR. The instruction selects 1 of 16 channels, determines the gain selected, and determines how the board will start the analog conversion. A jumper (SE/DI) to the input multiplexer determines if singled-ended or differential inputs are to be used.

An analog conversion can be started by a realtime clock, by an external trigger, or under program control by setting the A/D START bit in the CSR. CSR bit 5 enables the realtime clock input; CSR bit 4 enables the external trigger input. Two jumpers (F2, F1) on the board determine whether the external trigger comes from the I/O connector (J1) or from the LSI-11 bus event line (BEVNT L).

The output of the multiplexer goes to a differential amplifier, then to a programmable gain amplifier. The gain is set in the CSR with bits 2 and 3 (GS0 and GS1). The gain may be selected as 1, 2, 4, or 8 times the input voltage.

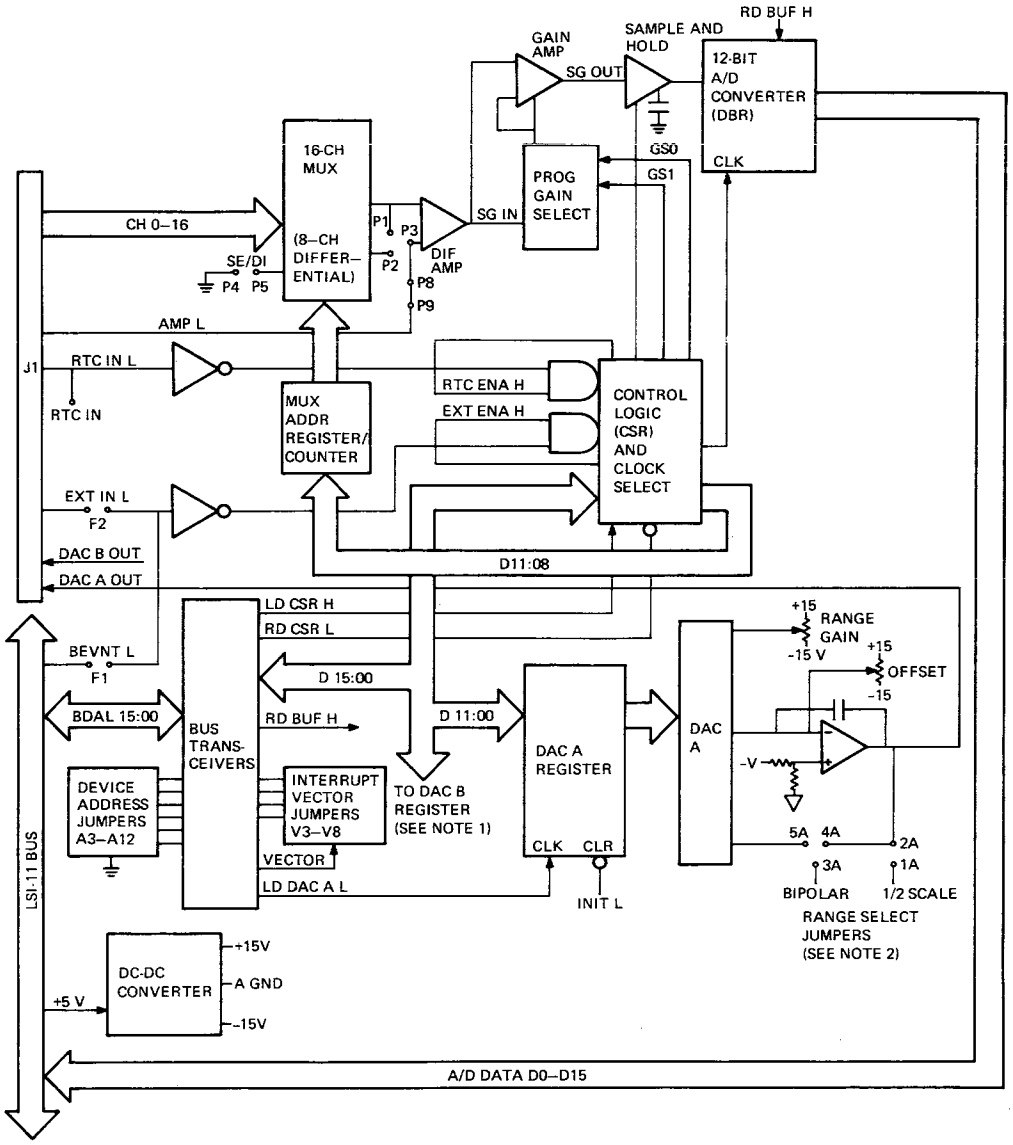
The output of the programmable gain amplifier goes to a sample and hold amplifier. The amplifier continuously samples the analog signal while waiting for the A/D START bit in the CSR, for a realtime clock input, or for an external trigger input. When one of these inputs has been received, the sample and hold amplifier changes to "hold" and the 12-bit A/D converter digitizes the "held" analog voltage.

When the A/D conversion is complete, the A/D DONE bit is set in the CSR and the sample and hold amplifier returns to sampling. If the DONE INT ENABLE bit is also set, an interrupt occurs to the LSI-11 bus. The contents of the 12-bit A/D converter is read by reading the A/D data buffer register (DBR).

D/A Conversion

The DAC register input data is addressed on the LSI-11 bus as follows.

AXV11-C



NOTE 1 DAC B CIRCUIT (NOT SHOWN) IS THE SAME AS DAC A CIRCUIT

NOTE 2 RANGE SELECT JUMPERS

RANGE	DAC A JUMPERS	DAC B JUMPERS
± 10 V	3A–5A	1B–5B
0–10 V	1A–2A	2B–3B

Figure 1 AXV11-C Functional Block Diagram

Register	Address	Signal Generated
DAC A	base address + 4	SEL 4 L
DAC B	base address + 6	SEL 6 L

The signals SEL 4 L and SEL 6 L create LD DAC A and LD DAC B, respectively, to load either DAC A or DAC B. The digital data from the LSI-11 bus goes to the bus transceivers, then into the selected DAC register. Once the register is loaded, the digital-to-analog conversion takes place. The DAC IC generates a current to the input of an amplifier. The current is a function of the value in the register. (A zero offset adjustment is made at the input to this amplifier.)

The amplifier converts the current to a voltage proportional to its input, with its maximum range selected by jumpers. (A trim pot provides adjustment to full-scale range.) The voltage is then amplified to become DAC A OUT or DAC B OUT at the I/O connector J1.

PROGRAMMING THE AXV11-C

The AXV11-C has four programmable registers.

Register	Read or Write	Standard Address
Control/status register	Read/write	170400_8
Data buffer register	Read only	170402_8
DAC A register	Write only	170404_8
DAC B register	Write only	170406_8

This paragraph describes setting the mode of operation, defines the standard device address and vector address, and defines the bits in each register.

Selecting AXV11-C Mode of Operation

The user determines the AXV11-C mode of operation. The user selects how the A/D conversions are to start and how the digital data is transferred to the LSI-11 processor.

Starting an A/D Conversion — An A/D conversion can be started in one of the following three ways.

1. Realtime clock input: set bit 5 in CSR.
2. External trigger enable: set bit 4 in CSR.
3. A/D START bit: set bit 0 in CSR.

Transferring A/D Data to LSI-11 Processor — The digital data can be transferred to he LSI-11 processor or memory by a programmed I/O transfer or by servicing an interrupt request. Using LSI-11 instructions, a programmed I/O transfer can write the CSR in the AXV11-C, read the CSR and wait for an A/D DONE bit (bit 7), then read the DBR to get the A/D data.

If interrupts are used, set the DONE INT ENABLE bit (bit 6) of the CSR. When the A/D conversion is complete, the A/D DONE bit (bit 7) sets, and an interrupt occurs to the LSI-11 processor. The processor services the interrupt request and gets the A/D data. After receiving the data, the software clears the A/D DONE bit in the AXV11-C's CSR.

An interrupt may also be programmed to occur on an error condition by setting bit 14 in the CSR.

AXV11-C Standard Device Address

The AXV11-C permits assigning a device address between 160000_8 and 177770_8. The standard device address is 170400_8. This is the starting address for the AXV11-C registers. The control/status register (CSR) receives this first address; the A/D data buffer register automatically receives the starting address + 2, or 170402_8. The DAC A register receives the starting address + 4, and the DAC B register receives the starting address + 6. Table 1 shows the AXV11-C standard address and vector address assignments. Please see section on selecting AXV11-C device address.

Table 1 AXV11-C Standard Address Assignments

Description	Mnemonic	First Module Address	Second Module Address
Registers			
Control/Status	CSR	170400	170420
Data Buffer	DBR	170402	170422
DAC A	DAA	170404	170424
DAC B	DAB	170406	170426
Interrupt Vectors			
A/D DONE		400	410
ERROR		404	414

AXV11-C Standard Interrupt Vector Address

The interrupt vector can be assigned between 0 and 770_8 in increments of 10_8. The standard base interrupt vector for the AXV11-C is 400_8. This vector is assigned to the A/D DONE interrupt request. If the DONE INT ENABLE bit (bit 6) is set in the CSR, the A/D DONE bit (bit 7) generates an interrupt request to the LSI-11 processor. When the request is ac-

knowledged by the LSI-11 processor, it starts the interrupt service routine at address 400.

The AXV11-C can also interrupt on an error. The error interrupt request is automatically assigned the base vector address + 4, or 404_8. If the ERROR INT ENABLE bit (bit 14) is set in the CSR by the program, an interrupt request will occur at the occurrence of any error (bit 15 set).

The standard interrupt vector addresses are shown in Table 1. See selecting AXV11-C interrupt vector address section to change the base interrupt vector address.

Control/Status Register (CSR)

The control/status register is a read/write register, shown in Figure 2. A control instruction is written into the CSR; the A/D status is read from the CSR. Table 2 defines the bits of the CSR.

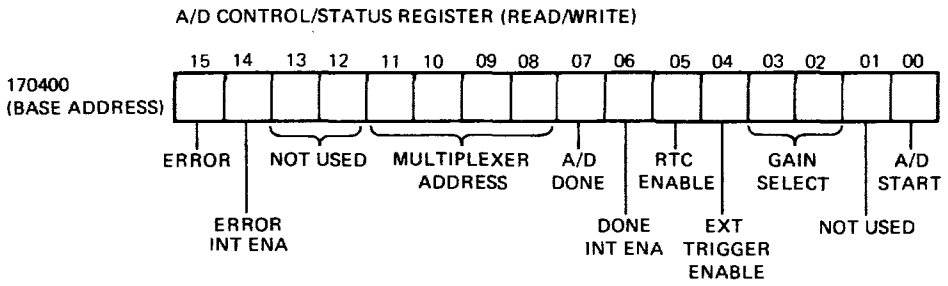


Figure 2 AXV11-C Control/Status Register (Read/Write)

Table 2 AXV11-C Control/Status Register Bit Assignments

Bit	Name	Description
0	A/D START	Write Only—When set this bit starts an A/D conversion. This bit is cleared by internal logic after starting conversion. It always reads back 0.
1	Not used	
2, 3	GAIN SELECT	Read/Write—Set these bits to select the gain for the analog input as follows.

Bit	Name	Description	
	Gain	**GS1 (bit 3)**	**GS0 (bit 2)**
	1	0	0
	2	0	1
	4	1	0
	8	1	1
4	EXT TRIG ENABLE	Read/Write—When set this bit allows an external trigger to start an A/D conversion.	
5	RTC ENABLE	Read/Write—When set this bit allows a realtime clock input to start an A/D conversion.	
6	DONE INTERRUPT ENABLE	Read/Write—When set this bit enables an interrupt on A/D DONE (bit 7). Both bits are cleared by INIT.	
7	A/D DONE	Read Only—This bit is set at the end of an A/D conversion and is reset by reading the A/D data buffer register.	
8-11	MULTIPLEXER ADDRESS	Read/Write—These bits select 1 of 16 analog input channels.	
12-13	Not used		
14	ERROR INTERRUPT ENABLE	Read/Write—When set this bit enables an interrupt on an ERROR (bit 15). Both bits are cleared by INIT.	
15	ERROR	Read/Write—When set this bit indicates that an error has occurred due to one of the following. • Trying an external start or clock start during multiplexer settling time. • Trying a start while an A/D conversion is in process.	

Bit	Name	Description
		• Trying any start while the A/D DONE bit is set. This bit can be cleared by writ ing the CSR or by an INIT.

Data Buffer Register (DBR)

The data buffer register is a read-only register that holds the digital data after the A/D conversion is complete. The DBR can be read after the A/D DONE bit is set in the CSR. Figure 3 shows the format for the DBR; Table 3 defines its bits.

The A/D DONE flag is cleared after reading the register or on initializ- ing the LSI-11 bus.

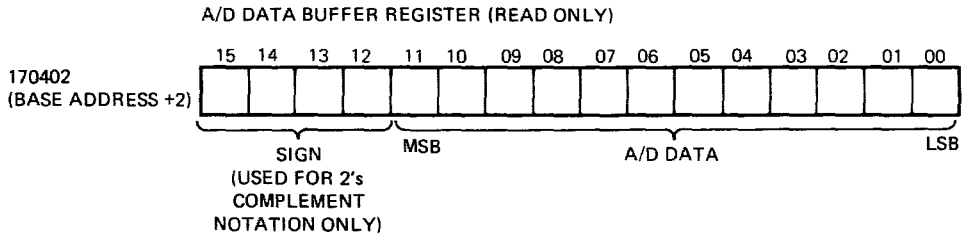


Figure 3 AXV11-C Data Buffer Register (Read Only)

Table 3 AXV11-C Data Buffer Register Bit Assignments

Bit	Name	Description
0-11	A/D DATA	These bits hold the parallel digital outputs after completion of the A/D conversion in one of the following data notations. • binary • offset binary • 2's complement The user selects the data nota- tion; see table 6.

Bit	Name	Description
12-15	SIGN	These bits are the sign for the bipolar inputs when using 2's complement notation. These bits are not used for binary or offset binary notation.

DAC A and DAC B Registers

DAC A register and DAC B register are 12-bit write-only registers. They are loaded from the LSI-11 bus with digital data to be changed to an analog voltage. Figure 4 shows the format for each register. Each DAC responds immediately to the data word placed in its register. Each register holds its last value until it is written again or power is turned off.

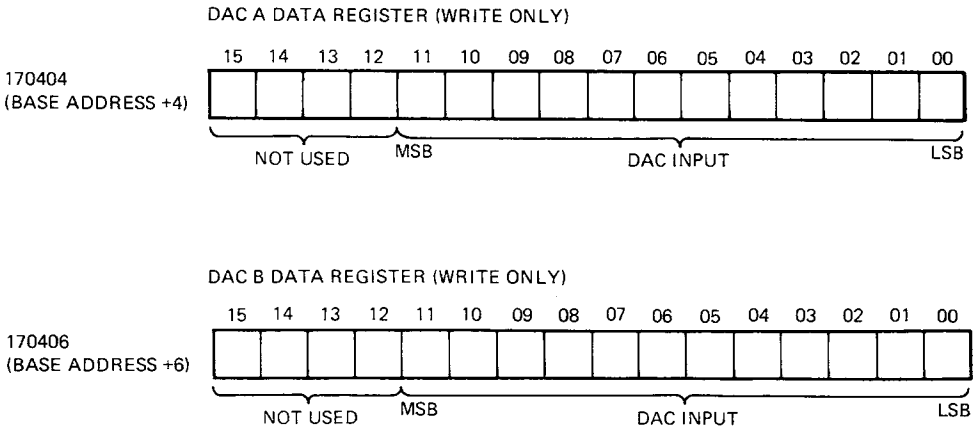


Figure 4 AXV11-C DAC A and DAC B Registers

Selecting AXV11-C Device Address

The AXV11-C device address is the I/O address assigned to the control/status register. The device address is selected by means of jumpers A3 through A12. (See jumper groups A and V in Figure 5.) The jumpers allow the user to set the device address within the range of 160000_8 to 177770_8. The device address is usually set at 170400_8, as shown in Figure 6. A jumper installed decodes a 1 in the corresponding bit position; a jumper out decodes a 0.

The user may select the format of the input data and output range and polarity. However, both registers must use the same input data notation - binary, offset binary, or 2's complement format. The output ranges can be ± 10 V or 0 V to + 10 V. The two registers must use the same polarity. Table 4 shows the expected output of the DAC for the selected input.

Table 4 AXV11-C DAC Input and Output Values

Polarity	Input Data Notation	Input Code (Octal)	Output Voltage
Unipolar	Binary	007777	+ full scale
		000000	0 V
Bipolar	Offset binary	007777	+ full scale
		004000	0 V
		000000	– full scale
Bipolar	2's complement	003777	+ full scale
		000000	0 V
		004000	– full scale

CONFIGURATION

The AXV11-C, shown in Figure 5, has jumpers to set up the device address, the interrupt vector address, the analog configuration, and the DAC configuration. The user may select the A/D input range, polarity, and the output data notation. The user may select the D/A input data notation, output range, and polarity of each DAC.

There are two types of jumpers on the board. Some are point-to-point jumpers, in which each jumper pin has a unique number. A jumper is installed from one numbered pin to another. The other jumpers are pairs of jumper pins. With each jumper type, a jumper wire is installed across a pair of pins.

This paragraph provides details on setting up the circuit board.

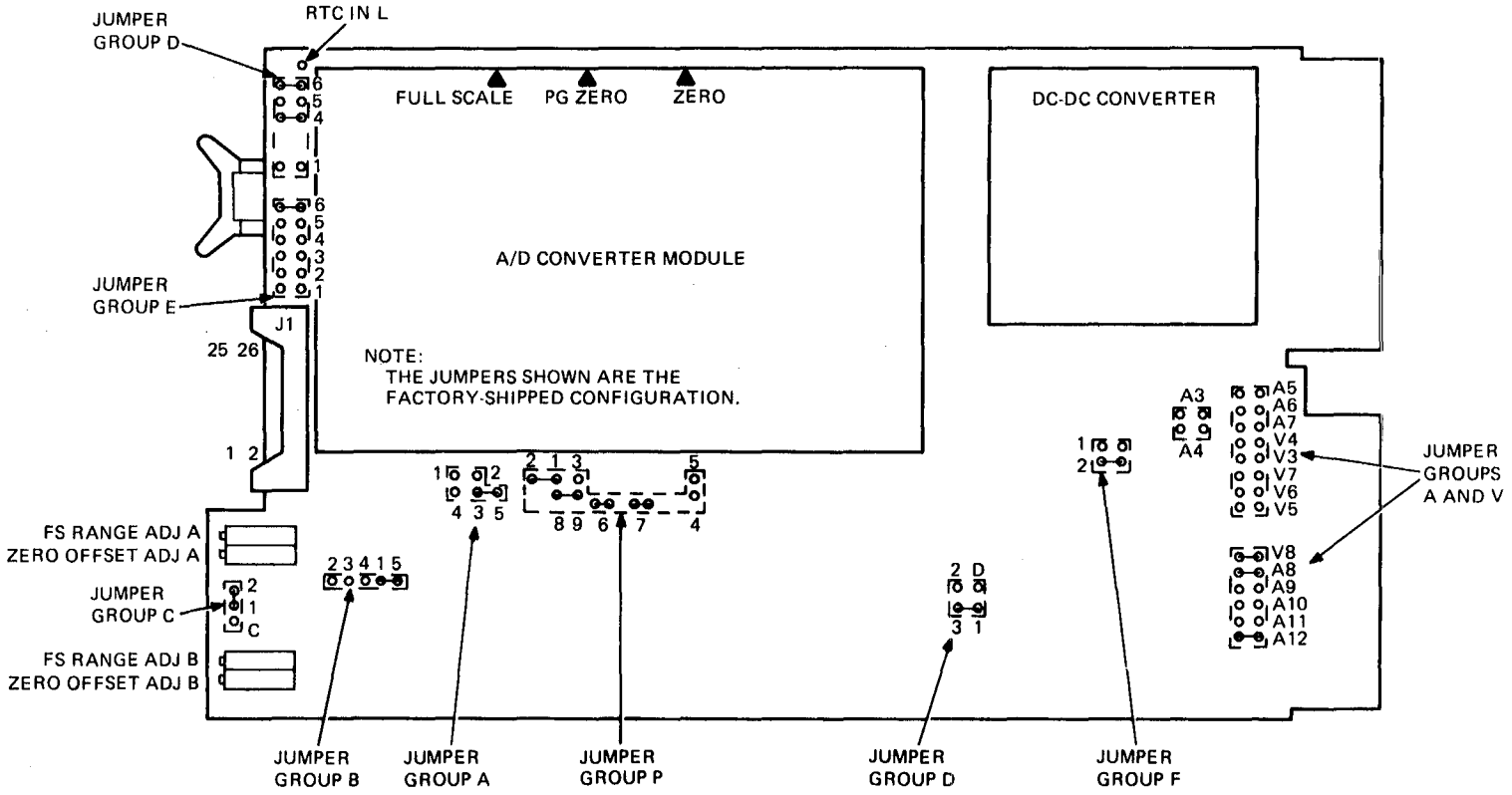


Figure 5 AXV11-C Physical Layout

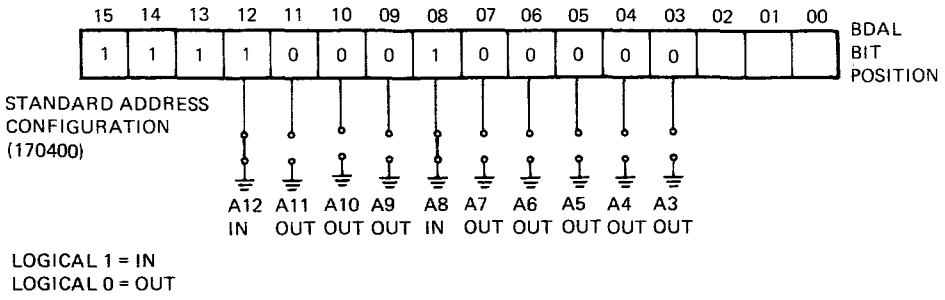


Figure 6 Selecting AXV11-C Device Address

Selecting AXV11-C Interrupt Vector Address

The AXV11-C is capable of generating two interrupt vectors to the LSI-11 processor. These interrupts, if enabled, occur when the A/D DONE bit or the ERROR bit is set in the CSR. The base interrupt vector address is assigned to A/D DONE. (The ERROR interrupt automatically is assigned the base interrupt vector address + 4.)

The base interrupt vector address can be set within the range of 0 to 770_8, in increments of 10_8. It is usually set to 400_8 by jumpers V3 through V8, as shown in Figure 7. (See jumper groups A and V in Figure 5.)

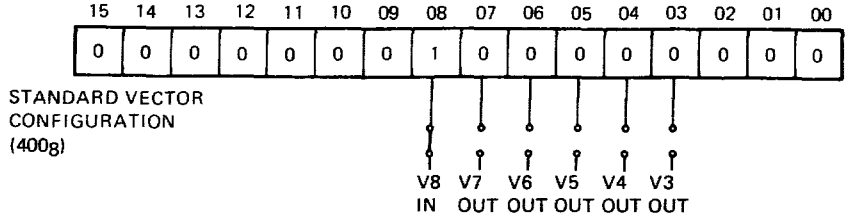


Figure 7 Selecting AXV11-C Interrupt Vector Address

Selecting AXV11-C Analog Input Range, Type, and Polarity

The AXV11-C allows software control over the full-scale range selection. The effective ranges provided by the programmable gain are as follows.

Gain	Effective Input Range Unipolar	Bipolar
1	0 V to +10 V	±10 V
2	0 V to +5 V	±5 V
4	0 V to +2.5 V	±2.5 V
8	0 V to ±1.25 V	±1.25 V

Table 5 shows the jumpers that must be installed to set up the analog input type. The board comes from the factory set for 16-channel single-ended, bipolar inputs. Refer to jumper group P in Figure 5.

Table 5 Selecting AXV11-C Analog Input Type

Input Type	Install Jumpers
Single-Ended Inputs*	P1 to P2; P8 to P9
Differential Inputs	P2 to P3; P4 to P5

* Factory configuration

NOTE

Jumpers P6 to P7 are factory installed for the programmable gain feature and should be left in.

Selecting AXV11-C A/D Output Data Notation

The AXV11-C allows the user to select the data notation to be used for the A/D output, as either binary, offset binary, or 2's complement notation. Table 6 shows the jumpers that must be installed to select the data notation. Refer to jumper groups D and E near the handle of the board, shown in Figure 5.

Selecting Source of External Trigger

The A/D conversions within the AXV11-C can be started in one of the following three ways.

1. Under program control using the A/D START bit in the CSR.
2. By a realtime clock input at J1 pin 21 or at pin RTC IN.
3. By an external trigger, either at J1 pin 19 or at the BEVNT line on the LSI-11 bus.

The user can select the source of external trigger using two jumpers on the board. (See jumper group F in Figure 5.) Table 7 shows the jumpers to install to select the source of the external trigger.

Table 6 Selecting A/D Output Data Notation

A/D Output Data Notation	Jumpers 1D	4D	5D	6D	5E	6E	Input Voltage	Output Code (Octal)
Binary	IN	OUT	OUT	IN	OUT	IN	+ full scale	007777
							0 V	000000
Offset binary*	OUT	IN	OUT	IN	OUT	IN	+ full scale	007777
							0 V	004000
							— full scale	000000
2's Complement	OUT	IN	IN	OUT	IN	OUT	+ full scale	003777
							0 V	000000
							— full scale	174000

* Factory configuration

Table 7 Selecting AXV11-C External Trigger

	Jumpers	
External Trigger Source	**F1**	**F2**
BEVNT line (LSI-11 bus)	IN	OUT
EXT TRIG IN (J1 pin 19)	OUT	IN

Selecting AXV11-C D/A Configuration

The user can select the input data notation and the output voltage range for the two D/A converters on the AXV11-C. DAC A and DAC B can be configured for different polarities; however, the input data notation selected and the output polarity selected must be the same for each DAC. Refer to Table 8 to set up DAC A; refer to Table 9 to set up DAC B. Jumper groups A, B, and D for the DACs are found below the A/D converter module, shown in Figure 5.

Table 8 Selecting DAC A Jumper Configuration

Range and Polarity	D/A Input Data Notation: Binary	Offset Binary	2's Complement
± 10 V	N/A	3A to 5A* D1 to D3	3A to 5A D to D2
0 to + 10 V	1A to 2A D1 to D3	N/A	N/A

*Factory configuration

Table 9 Selecting DAC B Jumper Configuration

Range and Polarity	D/A Input Data Notation: Binary	Offset Binary	2's Complement
± 10 V	N/A	1B to 5B* D1 to D3	1B to 5B D to D2
0 to + 10 V	2B to 3B D1 to D3	N/A	N/A

* Factory configuration

INTERFACING TO THE AXV11-C

Figure 5 shows the location of the I/O connector J1 on the AXV11-C. Analog input signals enter the board through this connector, and DAC output signals leave through this connector. Up to 16 single-ended analog inputs can be connected to J1 (CH 0-CH 15), or up to 8 differential analog inputs can be connected to J1 using CH 0-CH 7 and RETURN 0-7. A real-time clock input and an external trigger can also be connected to J1. Under program control, these two inputs can be enabled to start an A/D conversion.

RTC IN has a separate pin, found near the printed circuit board handle, for easy installation of a wire jumper from a clock board, such as the KWV11-C CLK OVFL tab.

BA11-M

BA11-M EXPANSION BOX

INTRODUCTION

The BA11-M expansion box provides a convenient means for expanding LSI-11 bus systems. Each box includes an H9270 LSI-11 bus-structured backplane and an H780 powersupply system mounted in an enclosure with a blank front panel.

The BA11-M is shown in Figure 1. Mechanical and mounting details are shown in Figures 2 and 3.

FEATURES

- Provides power and cooling for LSI-11 Bus options
- Accepts quad-or-double height modules
- Eight double-height (four quad) LSI-11 Bus slots available for options
- LSI-11 Bus power sequencing signals provided by the powersupply
- LSI-11 Bus line frequency clock signal provided by powersupply
- LSI-11 Bus backplane compatible with LSI-11, LSI-11/2, LSI-11/23, and SBC-11/21 processors, memories, and interface modules
- Rack-mountable in standard RETMA 19 inch-wide-rack
- UL listed; CSA certified

SPECIFICATIONS

Dimensions (including bezel)	
Width	48.3 cm (19 in)
Height	8.9 cm (3.5 in)
Depth	
Without mounting brackets	34.3 cm (13.5 in)
With mounting brackets	38.1 cm (15.0 in)
Shipping Weight	18.1 kg (40 lb)
Operating temperature*	5° to 60° C (41° to 140° F)
Operating humidity	10% to 95% with a maximum wet-bulb temperature of 32° C (90° F) and a minimum dew point of 2° C (36° F)

The maximum allowable operating temperature is based on operation at sea level, i.e., at 760 mmHg (29.92 inHg); maximum allowable operating temperature will be reduced by a factor of 1.8° C/1000 m (1.0° F/1000 ft) for operation at higher altitude sites.

BA11-M

AC input power	100-127 Vrms, 50 ±1 Hz or 60 ±1 Hz, 400 W maximum, or 200-254 Vrms, 50 ±1 Hz or 60 ±1 Hz, 400 W maximum
DC output power	+5 Vdc ±3%, 0-18 A load (static and dynamic) +12 Vdc ±3%, 0-3.5 A load (static and dynamic) Maximum output power: 120 W (total)
Recommended circuit breaker rating	15 A and 115 Vac or at 230 Vac

CONFIGURATION

The BA11-M is a rack-mounted enclosure that provides power and cooling for eight double (four quad) LSI-11 Bus module slots. It accepts either double-or-quad-size modules. Modules are accessible from the front of the box. A cable area is provided for routing I/O cables from the modules to the rear of the box where a cable clamp allows cables to be strain-relieved before leaving the box. An ac ON/OFF switch and linecord are located at the rear of the box. Two of the eight slots for double-size modules are normally used for cabling and termination, which leaves six bus slots available for options. Note that multiboard options that require the special backplane interconnection on connections card D (i.e., RLV11) are not accommodated by this expansion box. The BA11-M is available in two line voltage variations: 115V and 230V. Each version accommodates either 60 Hz or 50 Hz line frequency.

When installing an expansion box to expand from a single to a dual backplane system, the BCV1B bus expansion option and TEV11 bus terminator option (or equivalent) must be used. Install the BCV1B modules and cables as shown in Figure 4. The terminator must be installed in the option location in the last box. When installing the BCV1B cable set, disregard any "This side up" labels that may be on the BC05L cables. Ensure that the red line on each cable is toward the center of both modules and that J1 on each board is connected to J1 on the second board, and similarly, J2 on both boards. Ensure that the cables have no twists. Carefully fold excess cable as shown in

Figure 4. Figure 5 illustrates proper installation of the BCV1B and TEV11 options.

When expanding from a second to a third backplane, the BCV1A bus expansion option is required, in addition to the items required for expansion to the second backplane.

NOTE

BCV1A and BCV1B cables must differ in length by 121.92 cm (4 ft) (minimum).

The completed installation for a three-backplane system using the BCV1A option is shown in Figure 5. In addition to this option, the BCV1B option is required to connect the first backplane to the second backplane; a 120 bus termination is required in the last optionslot in the third backplane.

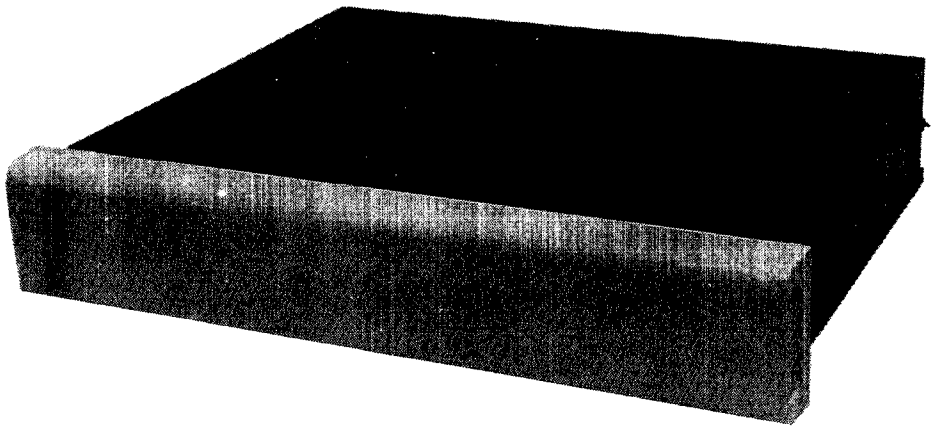


Figure 1 BA11-M Expansion Box

BA11-M

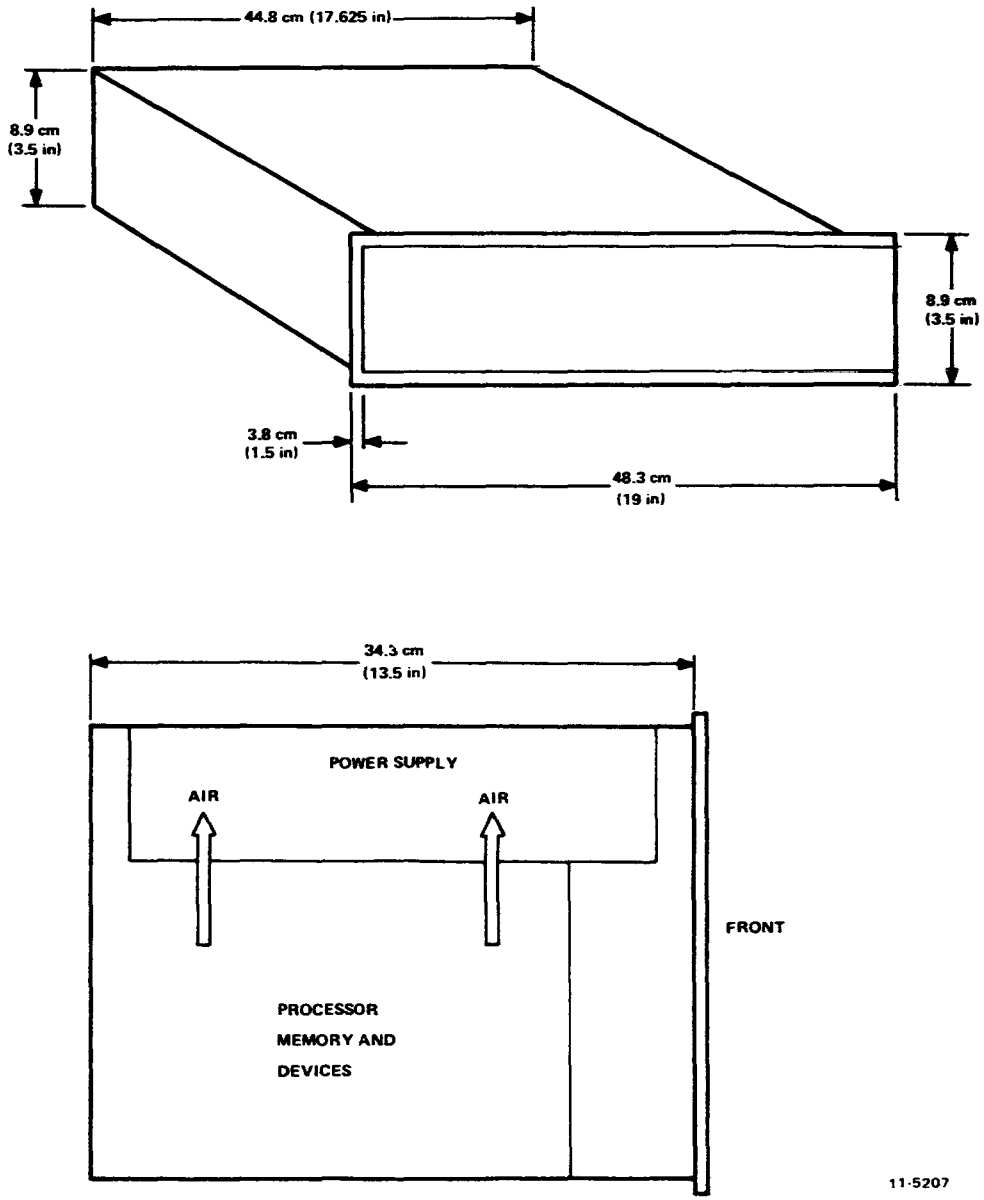


Figure 2 BA11-M Assembly Unit

BA11-M

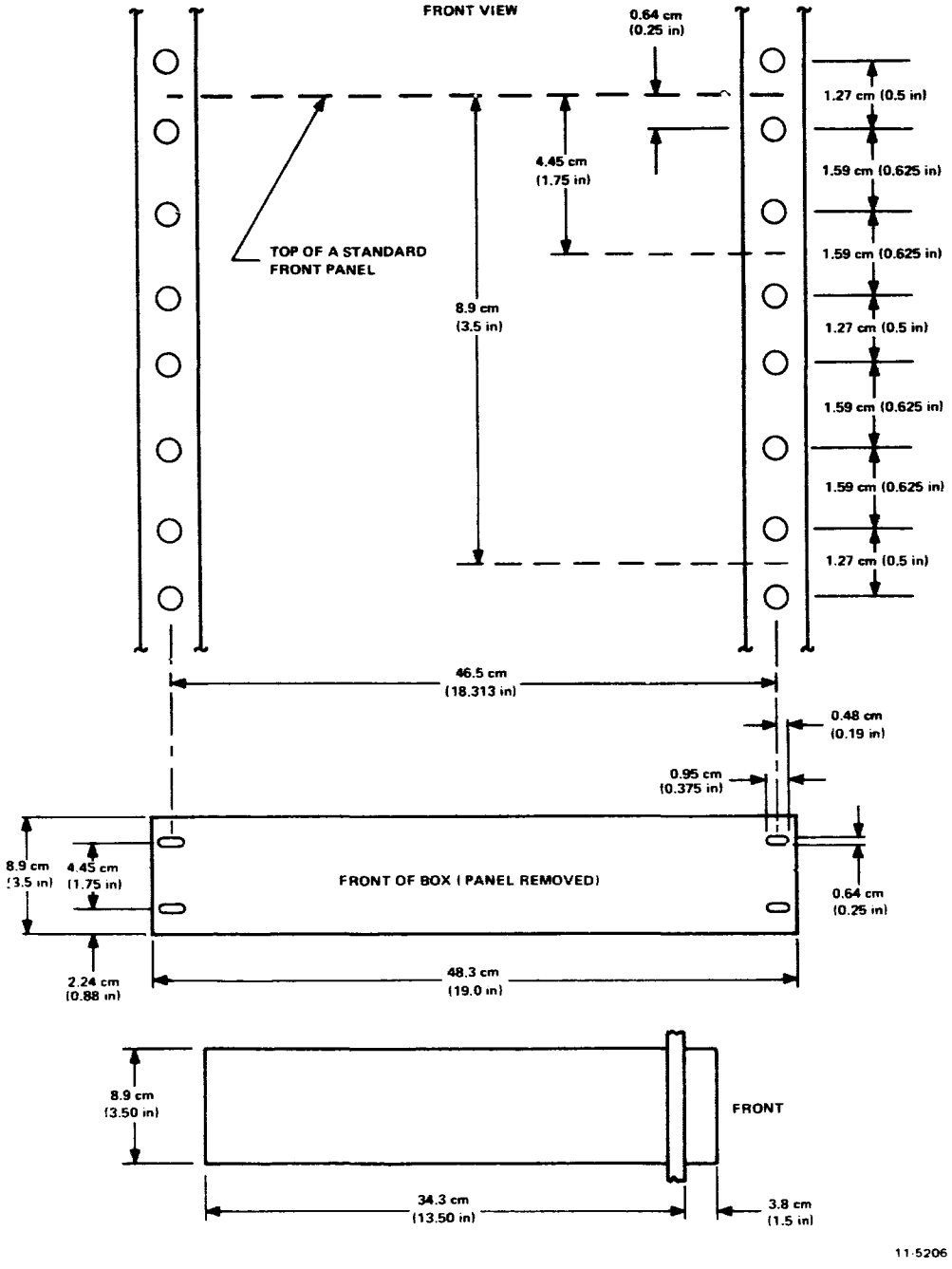


Figure 3 BA11-M Cabinet Mounting

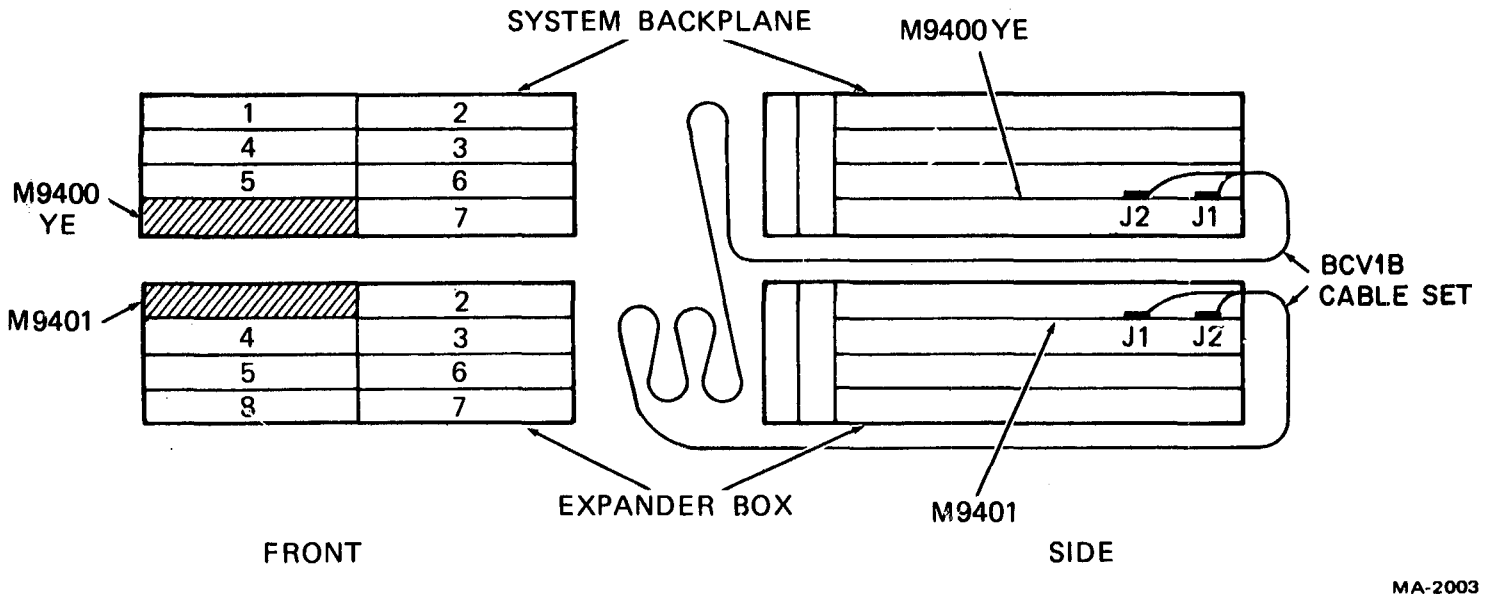
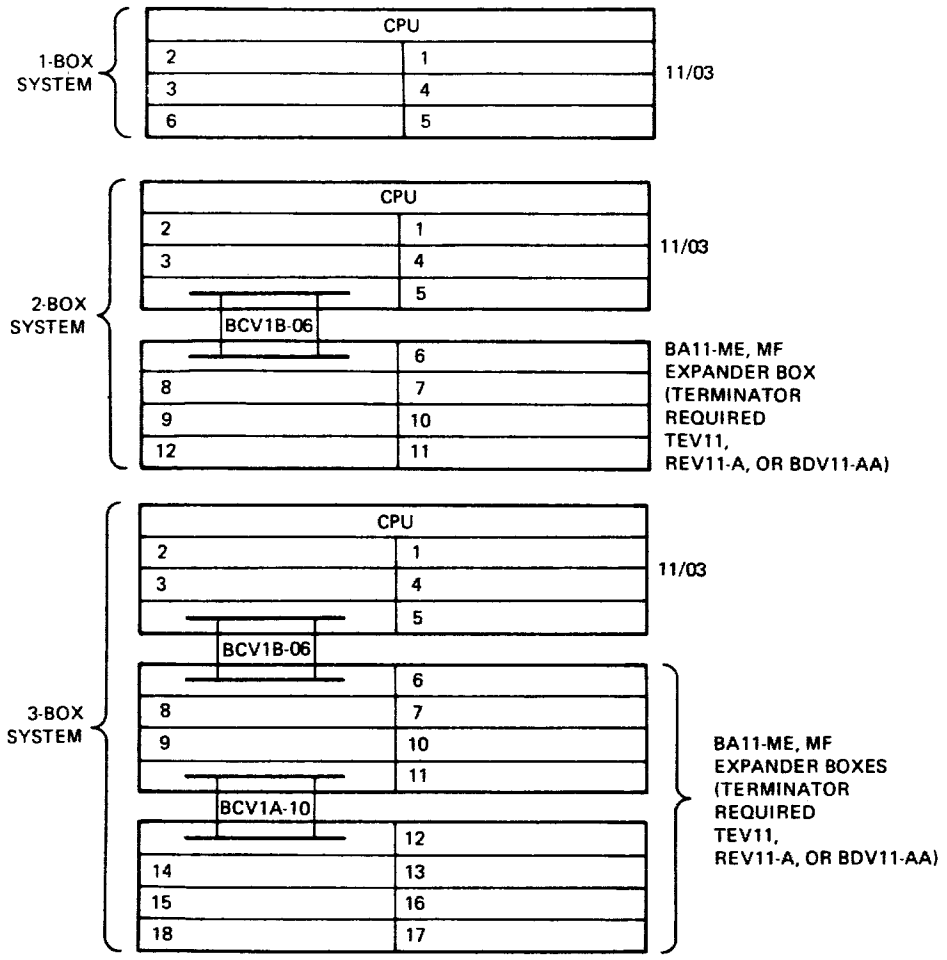


Figure 4 BA11-M Expansion Box Interconnections (two-backplane system)



NOTES

1. INCLUDED IN BCV1B BUS EXPANSION OPTION. (CABLES ARE AVAILABLE IN 2, 4, 6, OR 12 FT LENGTHS.)
2. INCLUDED IN BCV1A BUS EXPANSION OPTION. (CABLES ARE AVAILABLE IN 2, 4, 6, OR 12 FT LENGTHS.)
3. INCLUDED IN TEV11 BUS TERMINATOR OPTION.
4. THE LSI-11 BUS IN RESTRICTED TO 15 OPTIONS, MAXIMUM. THESE OPTION SLOTS WOULD ONLY BE USED WHEN PREVIOUS OPTION(S) OCCUPY MORE THAN 1 OPTION LOCATION.
5. BCV1A AND BCV1B EXPANSION CABLES MUST DIFFER IN LENGTH BY 4 FT (MIN).

MA-2000

Figure 5 BCV1A Installation

BA11-N

BA11-N MOUNTING BOX

INTRODUCTION

The BA11-N mounting box is designed to be used as a mounting box or as an expander box for an LSI-11-bus-based system. Each mounting box (Figure 1) includes an H9273 backplane assembly, an H786 power supply, and an H403-A ac input panel mounted in an enclosure with a blank front panel (BA11-NE, NF) or bezel assembly (PDP-11/03-LC, LD).

FEATURES

- Nine slots for double-or-quad-size modules
- Powerful and reliable 240-watt switching powersupply, which is both voltage- and frequency-independent
- Module cooling
- Designed to meet small-system applications
- Modular design for ease of servicing
- LSI-11 bus power-sequencing signals provided by power supply
- Line frequency signal provided by powersupply
- Unique backplane interconnection for custom multiboard options
- LSI-11 bus backplane-compatible with LSI-11, LSI-11/2 and LSI-11/23 processors, memories, and interface modules
- Rack-mountable in standard RETMA 19-inch-wide rack
- UL listed, CSA certified and complies with VDE and IEC requirements

SPECIFICATIONS

Tables 1 and 2 show BA11-NE and BA11-NF mounting box specifications, including the H786 powersupply.

Dimensions (including bezel)	
Width	48.3 cm (19 in)
Height	13.2 cm (5.19 in)
Depth	
Without mounting brackets	57.8 cm (22.7 in)
With mounting brackets	67.96 cm (26.75 in)
Weight (without modules)	20 kg (44 lb)

BA11-N

Operating temperature*	5° to 60° C (41° to 140° F)
Operating humidity	10% to 95%, with a maximum wet-bulb temperature of 32° C (90° F) and a minimum dew point of 2° C (36° F)
Input voltage	
BA11-NE	115 Vac
BA11-NF	230 Vac
Input current**	
BA11-NE	12 A max
BA11-NF	6 A max
Circuit breaker rating	15 A at 115 Vac or 230 Vac

* The maximum allowable operating temperature is based on operation at sea level, i.e., at 760 mmHg (29.92 inHg); maximum allowable operating temperature will be reduced by a factor of 1.8° C/1000 m (1.0° F/1000 ft) for operation at higher altitude sites.

** Input current consists of that used by the BA11-N, itself, plus whatever current is supplied via the convenience ac outlet (J3) to an expander box; the total current must be less than the maximum specified.

DESCRIPTION

The H9273 backplane assembly consists of a backplane, a card frame assembly, and two cooling fans. The H9273 9-slot backplane assembly will accept nine LSI-11 bus double-height or quad-height modules (except for MMV11-A 4K × 16 core memory modules). The PDP-11/03-LC and the BA11-NE operate on 115 V and the PDP-11/03-LD and the BA11-NF operate on 230 V. Mechanical and mounting details are shown in Figure 2.

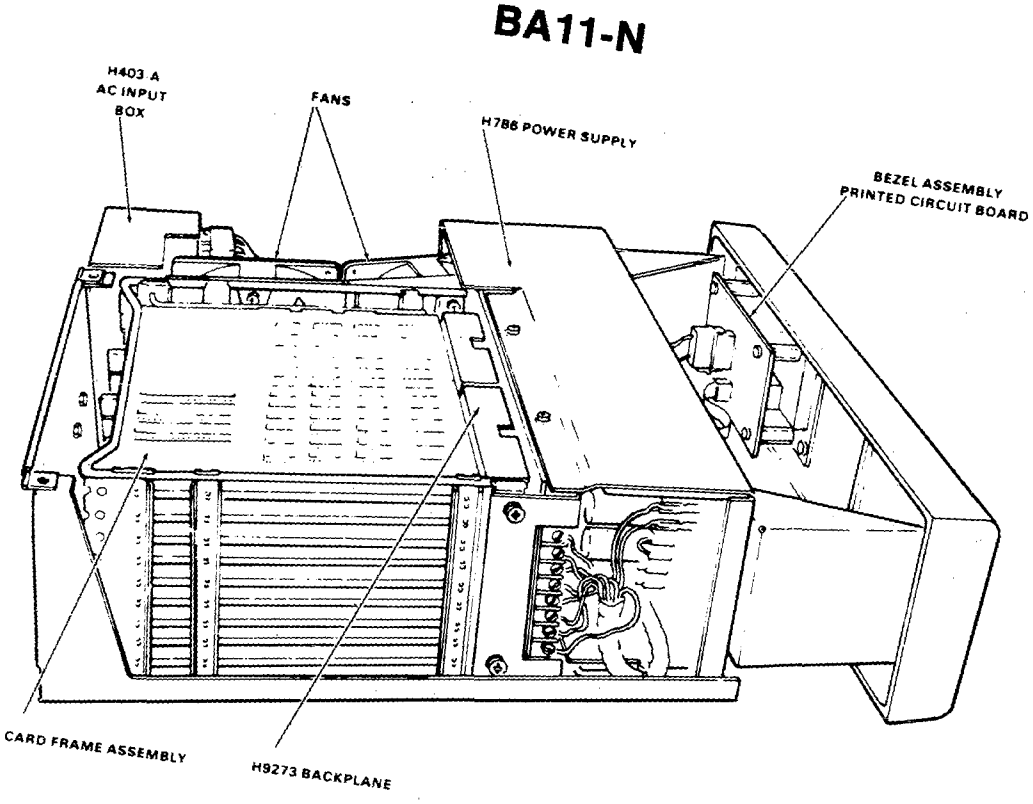


Figure 1 BA11-N Major Assemblies

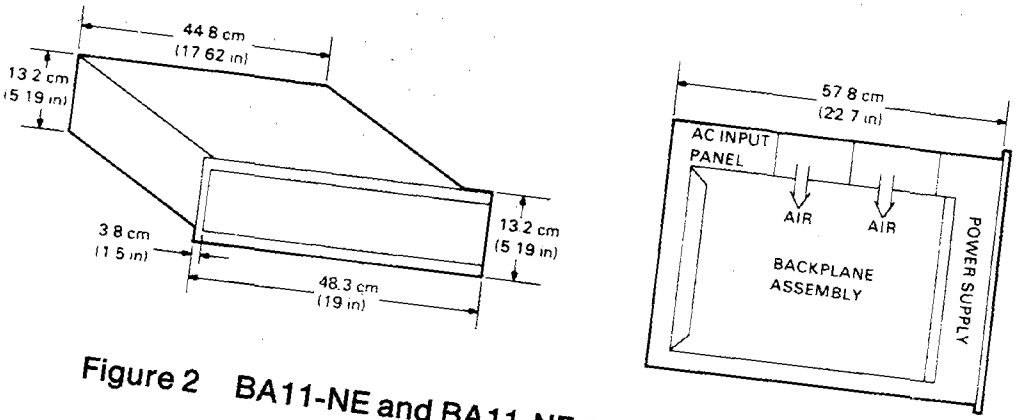


Figure 2 BA11-NE and BA11-NF Assembly Unit

The ac input box, powersupply, and H9273 logic assembly are attached to the logic-box base. The powersupply assembly is hinged to the base and can be swung open to expose the internal components; with little effort, the entire assembly can be removed from the base and replaced. LSI-11 bus modules are inserted in the backplane from the rear of the box through an access door that is equipped with strain reliefs for LSI-11 bus and communications cables.

When the unit is to be mounted in an equipment rack, the logic-box cover is attached to the rack with mounting hardware. The logic-box base slides into the mounted cover and a spring-button assembly engages to prevent the base from being accidentally pulled out of the cover.

Table 1

Item	Specification
Current rating	5.5 A at 115 Vrms 2.7 A at 230 Vrms
Inrush current	100 A peak, for ½ cycle at 128 Vrms or 256 Vrms
Apparent power	630 VA
Power factor	The ratio of input power to apparent power shall be greater than 0.6 at full load and low input voltage
Output power	+5 Vdc ±250 mV at 22 A (A minimum of 2 A of +5 Vdc power must be drawn to ensure that the +12 Vdc supply regulates properly) +12 Vdc ±600 mV at 11 A
Power-up/power-down characteristics	
Static performance	
Power-up	BDCOK H goes high; 75 Vac BPOK H goes high; 90 Vac
Power-down	BPOK H goes low; 80 Vac BDCOK H goes low; 75 Vac

Table 1 BA11-N Power Supply Specifications (Cont)

Item	Specification
Dynamic performance	
Power-up	3 msec (min) from dc power within specification or to BDCOK H asserted 70 msec (min) from BDCOK H asserted to BPOK H asserted
Power-down	4 msec (min) from ac power off to BPOK H negated 4 msec (min) from BPOK H negated to BDCOK H negated 5 μsec (min) from BDCOK H negated to dc power as of specifications

CONFIGURATION

The procedure for mounting the BA11-N mounting box in an equipment rack is presented below.

Installing the Logic Box Cover — The logic-box cover is mounted in the equipment rack as shown in Figure 3.

1. When the unit is shipped, the logic-box cover is held to the base by four screws (these are used only in non-rack-mounted applications) and a single shipping screw, which, for safety, must be in place whenever the unit is moved or shipped. First, remove the four screws that attach the cover to the base. Then open the rear door and remove the shipping screw.
2. A safety locking device is found on the right side of the unit (when looking at the front). This device, a spring-button assembly, is attached to the side of the ac input box. When the unit is closed, the button on this assembly fits into the rear hole of two holes in the right side of the cover. This mechanical interlock can be overridden by pushing the button in from the outside of the cover while, at the same time, pulling the logic-box base to get the button past the hole. The base can then be pulled out of the cover to its extended position; at this position, the button pops into the front of the two holes, preventing the base from being inadvertently pulled entirely out of the cover. Open the base to the extended position and then release the button from the front

hole. Slowly pull the base entirely out of the cover and set the base out of the way.

3. Attach the Tinnerman nuts to the cabinet uprights in eight places.
4. Mount the cover to the front cabinet uprights using four pan-head screws (10-32 × 0.62 lg) and four No. 8 lockwashers.
5. Attach the two support brackets to the cover using four Phillips pan-head screws (8.32 × 0.38 lg) and four No. 8 lockwashers.
6. Attach the support brackets to the rear cabinet uprights using four Phillips pan head screws (10-32 × 0.62 lg) and four No. 10 flat washers.
7. Slide the unit into the cover. It will be held in place by the spring-button assembly. To slide the unit forward again it will be necessary to release this spring button.
8. If the system is to be moved or shipped, the shipping screw must be replaced.

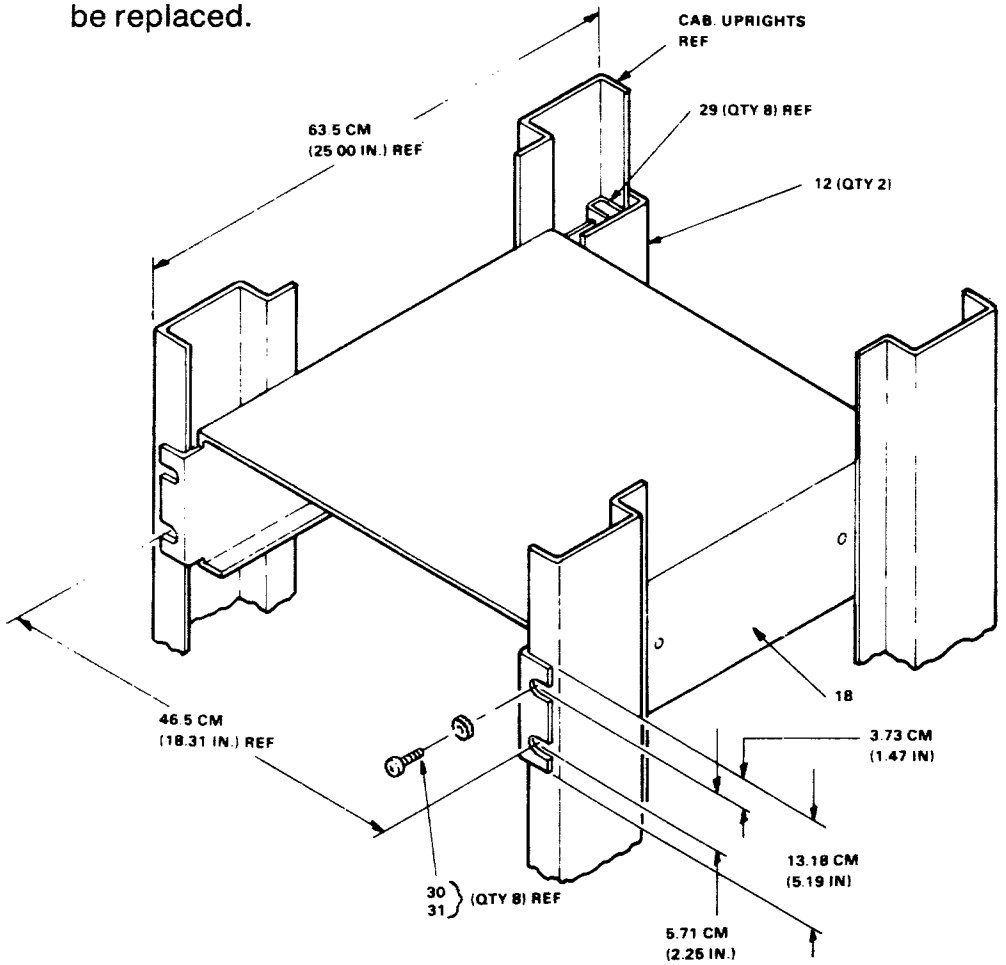


Figure 3 BA11-NE and BA11-NF Cover Mounting Dimensions

Installing the Logic-Box Base in the Cover — Set the rear of the logic-box base on the support flanges of the cover and slide the base in until the spring-button assembly engages in the extended position. Take care not to pinch the cables while sliding in the base. Release the spring-button and push the base all the way in until it engages in the closed position. Take the following steps to complete the installation.

NOTE

The base being installed is either the main base, i.e., the one containing the CPU, or an expander base (two expander boxes can be added). Modify the following instructions to suit the kind of base you are installing, e.g., if there is a blank front panel, skip the first half of step 1.

1. Put the AUX switch in the front panel in the OFF position; put the ON/OFF switch on the ac input box in the OFF position.
2. When the AUX switch on the front panel is in the ON position, the two wires of the powercontroller cable are common. Connect the free end of the cable to the input circuit of the powercontroller so that the AUX switch controls the application of primary power to the controller. Keep the AUX switch in the OFF position.
3. Loosen the cable strain reliefs and open the rear door of the box to install the LSI-11 bus expansion cable assemblies. Two cable assemblies are used. Table 2 describes the assemblies and tells where to insert the assembly modules. (Figure 4 illustrates module placement.) When inserting the modules, make sure the connectors are on top.
4. Close the rear door; bring the bus cables out under the left strain relief and the communcations cables out under the right strain relief. Adjust the strain reliefs so that the cables are held firmly, but are not pinched or crushed. Secure the strain reliefs and the rear door. Make sure the cables will not bind when the base is pulled out to the extended position.

Table 2 LSI-11 Bus Expansion Cable Assemblies

Assembly	Assembly Composition	Insert Modules In
BCV1B-XX	Two BC05L-XX cables	
	One M9400-YE module	Slots A and B of the first open row after all other LSI-11 bus options have been installed in the main box.
	One M9401 module	Slots A and B of row 1 of expander box 1
BCV1A-XX	Two BC05L-XX cables	
	One M9400-YD module	Slots A and B of the first open row after all other LSI-11 bus options have been installed in expander box 1
	One M9401 module	Slots A and B of row 1 of expander box 2

NOTE

"-X" in the cable assembly number denotes length, which can be 60.96, 121.92, 182.88, or 304.80 cm (2, 4, 6, or 10 ft). (Each cable of an assembly is the same length.) When both assemblies are used in a system (boxes), the lengths must differ by 121.92 cm (4 ft). To facilitate servicing, the BCV1B cables should be 182.88 cm (6 ft) in length, while the BCV1A cables should be 304.80 cm (10 ft) in length.

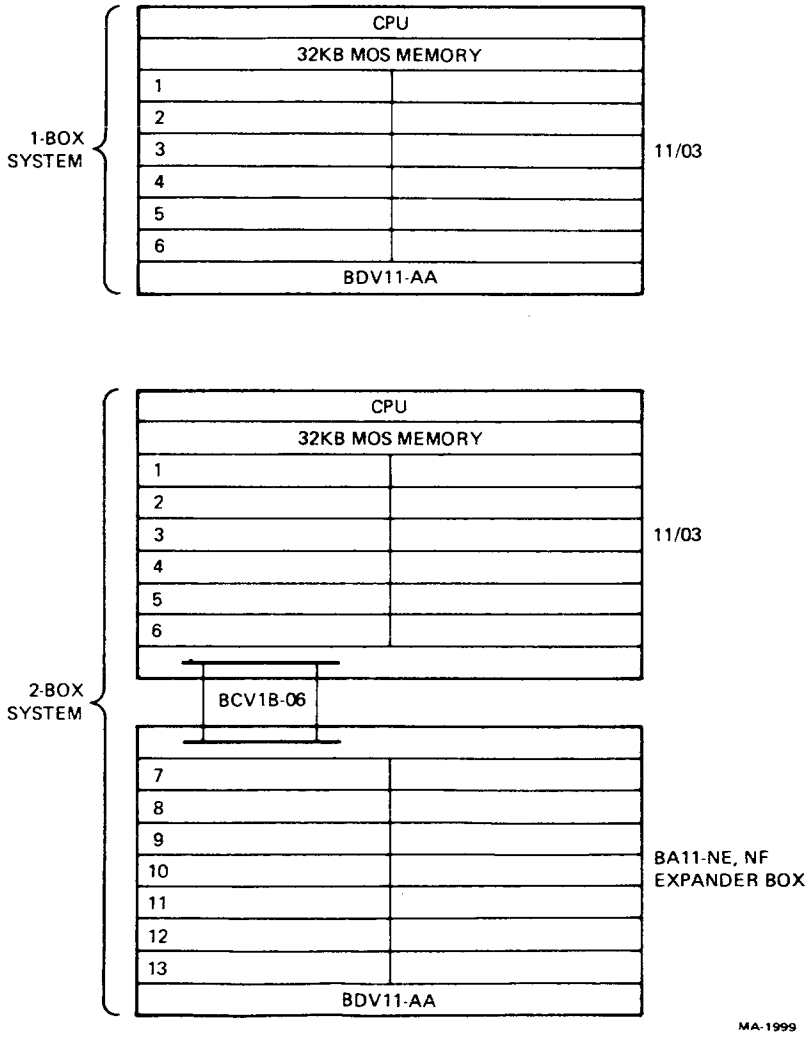


Figure 4 Configuring Large Box

BA11-S

BA11-S EXPANSION BOX

INTRODUCTION

The BA11-S is both a mounting box and an expander box designed for use with the PDP-11/23-PLUS computer system and LSI-11/23 modules. Each BA11-S box comes with an H9276 logic assembly, two cooling fans (a 70 cfm fan to cool the logic boards and a 100 cfm fan cools the power supply), and an H403-B AC input box. A layout of these components in the BA11-S box is illustrated in Figure 1.

The BA11-S mounting box is available for both 120 V and 240 V systems, and a choice of two front panel models can be selected. Listed below are the six models:

Model	Primary Power/Front Panel
BA11-SA	120 V/Control Panel
BA11-SB	240 V/Control Panel
BA11-SC	120 V/Blank Panel
BA11-SD	240 V/Blank Panel
BA11-SE	120 V/No Cable or Expansion Modules/Blank Bezel
BA11-SF	240 V/No Cable or Expansion Modules/Blank Bezel

FEATURES

- 9 slots for double-and quad-height LSI-11 modules
- Provides power and cooling for LSI-11 bus modules
- Modular design for easy servicing

SPECIFICATIONS

Dimensions (including bezel)	
Width	48.3 cm (19 in)
Height	13.2 cm (5.19 in)
Depth	
Without mounting brackets	57.8 cm (22.75 in)
Operating temperature*	5° to 60° C (41° to 140° F)

Operating humidity	10% to 95%, with a maximum wet bulb temperature of 32° C (90° F) and a minimum dew point of 2° C (36° F)
Input voltage	
BA11-SA, SC, SE	120 Vac
BA11-SB, SD, SF	240 Vac
Input current	
BA11-SA, SC, SE	6 A max
BA11-SB, SD, SF	3 A max
Output Voltage	+5 V at 2 A to 36 A +12 V at 0.0 A to 5 A

* The maximum allowable operating temperature is based on operation at sea level, i.e., at 760 mmHg (29.92 inHg); maximum allowable operating temperature will be reduced by a factor of 1.8° C/100 m (1.0° F/100 ft) for operation at higher altitude sites.

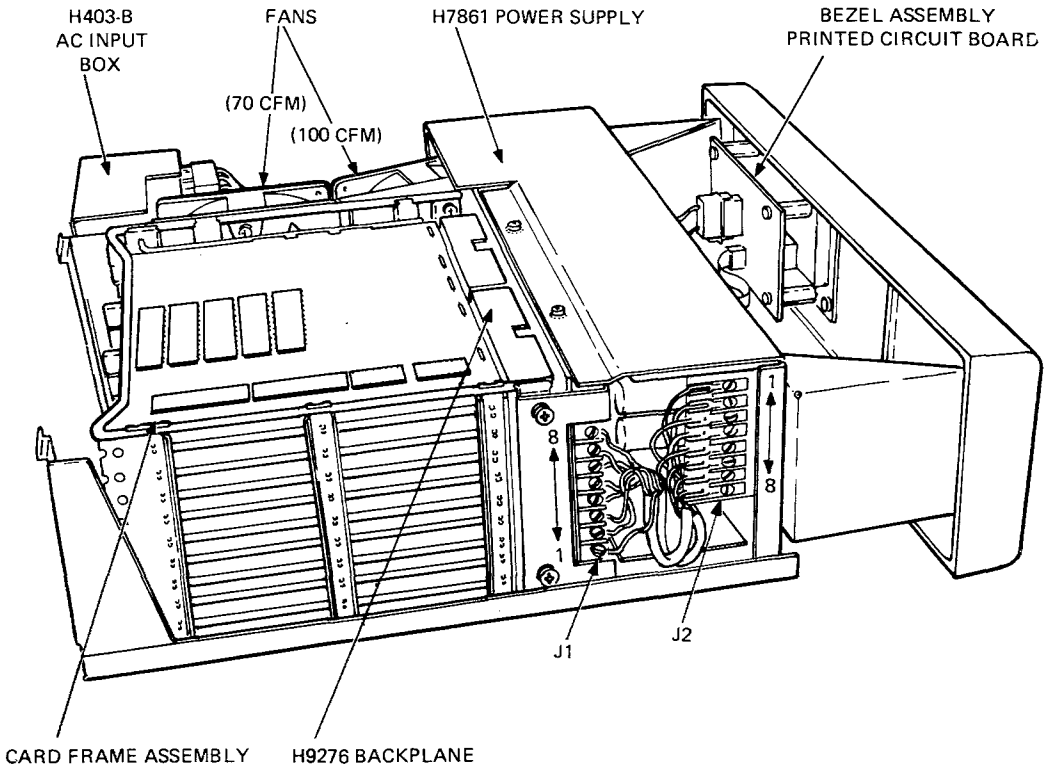


Figure 1 BA11-S Major Assemblies

When the equipment is being operated at the maximum allowable temperature, air flow must maintain air temperature rise to a maximum of 7°C (12.6° F)

DESCRIPTION

Figure 2 illustrates the BA11-S with its logic box cover removed. The ac input box, power supply, and the H9276-B logic assembly (which includes the fans and the backplanes) are attached to the logic box base. The bezel is attached to the power supply. The power supply assembly is hinged to the base and can be swung open to expose the internal components. The complete assembly can be easily removed

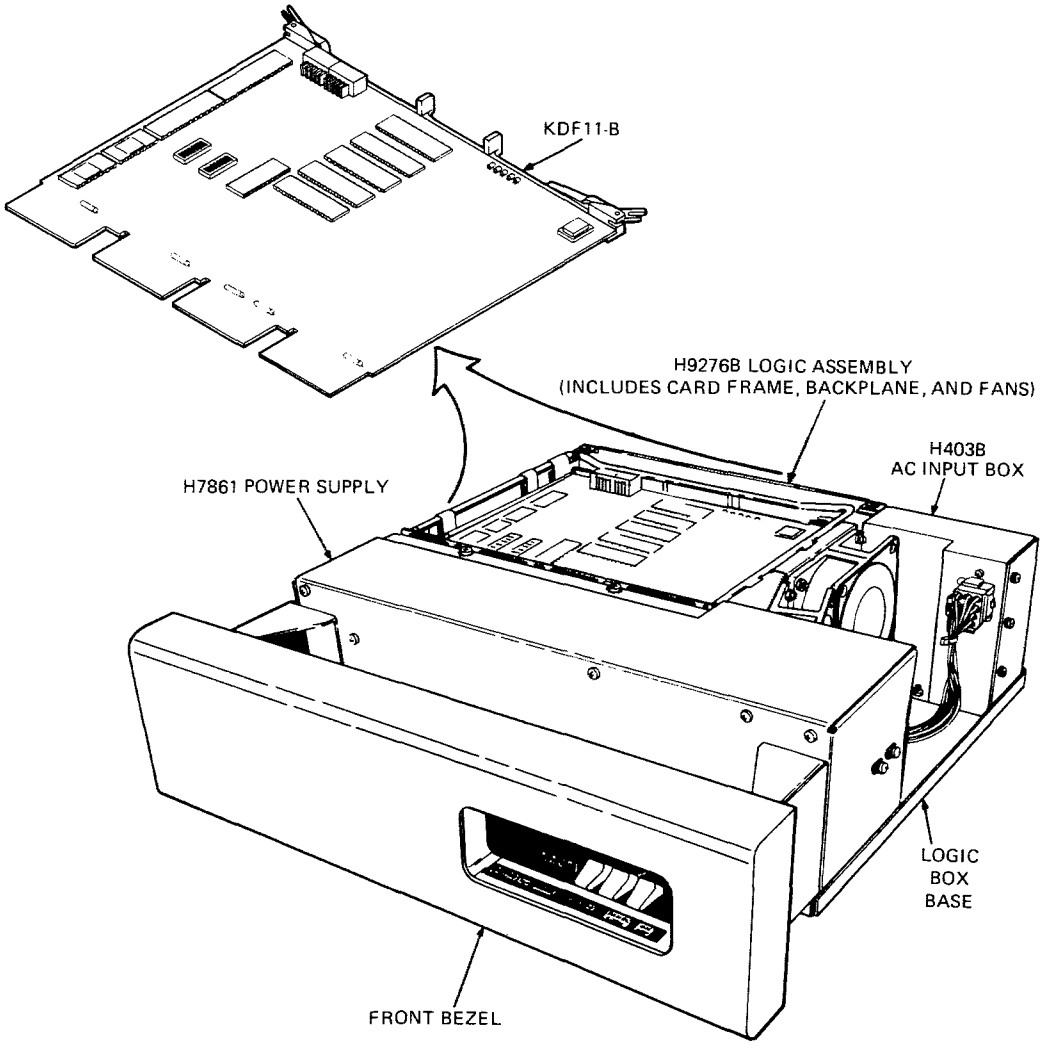


Figure 2 BA11-S Logic Box with Cover Removed

from the base and replaced. Extended LSI-11 bus modules are inserted in the backplane from the rear of the box through the rear access door.

When the unit is mounted in an equipment rack, the logic box cover is attached to the rack with mounting hardware. The logic box base slides into the rack-mounted cover. A restraint cable is attached between the H403-B ac input box and the rack frame to prevent the base from being pulled completely out of the cover by mistake.

AC Input Box (H403-B)

Power is provided to the H403-B box from the ac mains by either a 120 V line cord or a 240 V line cord. The box includes an ac input connector, a circuit breaker, a line filter, and a switch that makes the correct connections to the fans and the power supply for both the 120 VAC and 240 VAC line voltages. The output of the box is taken to the fans and the power supply by an AC power harness. Connectors P1 and P4 (see Figure 3) of the harness are Mate-N-Lok connectors (12-pin and 9-pin, respectively), while P2 and P3 are molded AC plugs that break out of the harness to plug into terminals on the fans.

H7861 Power Supply

The H7861 power supply is attached to the logic assembly with two screws and held to the logic base by two hinge assemblies. When the two screws are removed from the logic assembly, the complete power supply assembly can be tipped open on the hinges, allowing access to the printed circuit boards mounted within. The assembly can be easily removed by first removing the screws, unlatching the hinges, and disconnecting a maximum of four cables (three, if a blank front panel is used).

Three printed circuit boards contain all the power supply components. The control board and the power monitor board are inserted in connectors that are mounted on the master board. The regulated dc voltages generated on the master board are sent to the H9276 backplane by a dc harness that connects on both ends to screw terminals. The signals generated on the control board are applied to the backplane and to the front panel by two different signal cable assemblies.

H9276 Backplane

The H9276 is a 9 × 4 (nine slots of four rows each) backplane in which both double and quad modules can be inserted. Rows A and B of each slot supply the extended LSI-11 bus signals, and these signals, in turn, are bused to each of the nine slots. The pins of the C and D

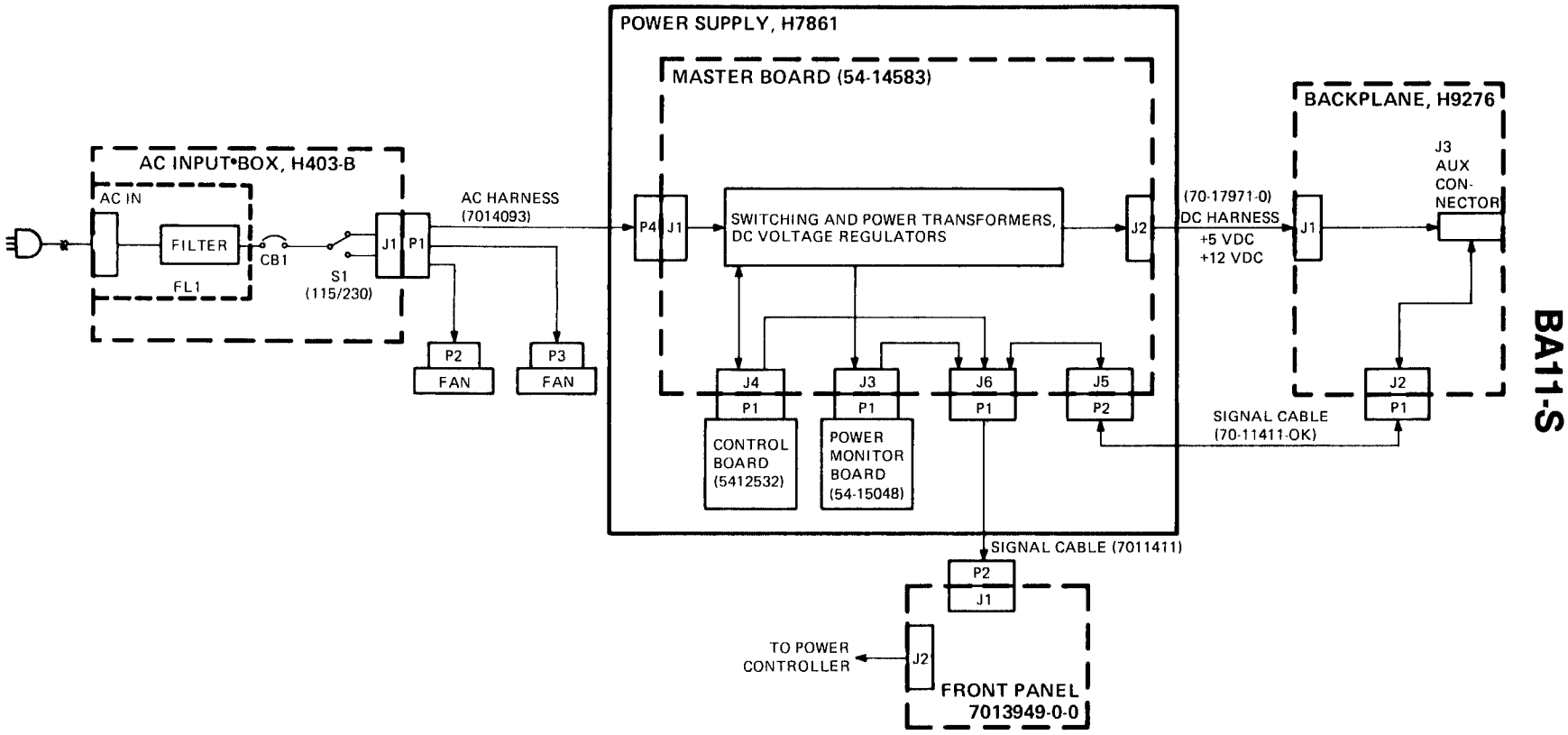


Figure 3 BA11-S Functional Block Diagram

rows are not bused; however, the pins of the adjacent slots are connected. This not only precludes the necessity of top connectors, but also provides the means for designing buses whose lengths are determined by the number of modules in a set. The C and D rows of the backplane are referred to collectively as the CD bus. More information on the H9276 backplane is detailed in the H9276 section which follows in this handbook.

BA11-S Expander Box

The BA11-S expander box for LSI-11 bus systems is physically identical to the BA11-S main box, with the exception of the front panel (usually only one box has a functional front panel). BA11-SE and BA11-SF expander boxes are identical to the BA11-S main box, except for the blank bezel. BA11-SE and BA11-SF boxes are identical to the BA11-SC and the BA11-SD, except that they have 9404 and 9405 modules and BC02D cables.

The BA11-S box with the H9276 backplane functionally differs only slightly from the BA11-N box (with H9275 backplane). The BA11-S box has four more address lines than the BA11-N box; these lines are needed for 22-bit operation.

INSTALLATION

The procedure for mounting the BA11-S mounting box in an equipment rack is described below.

Installing the Logic Box Cover

The logic box cover is mounted in the equipment rack as depicted in Figure 4. This illustration also shows the mounting dimensions and the cover mounted to the four cabinet uprights.

1. When the unit is shipped, the logic box cover is held to the base by four screws (these are used only in non-rack-mounted applications), and a single shipping screw, which, for safety, must be in place whenever the unit is moved or shipped. First, remove the four screws that attach the cover to the base; then open the rear door and remove the restraining screw.
2. Attach the Tinnerman nuts to the cabinet uprights in eight places.
3. Mount the cover to the front cabinet uprights using four 10-32 screws and four No. 10 flat washers.

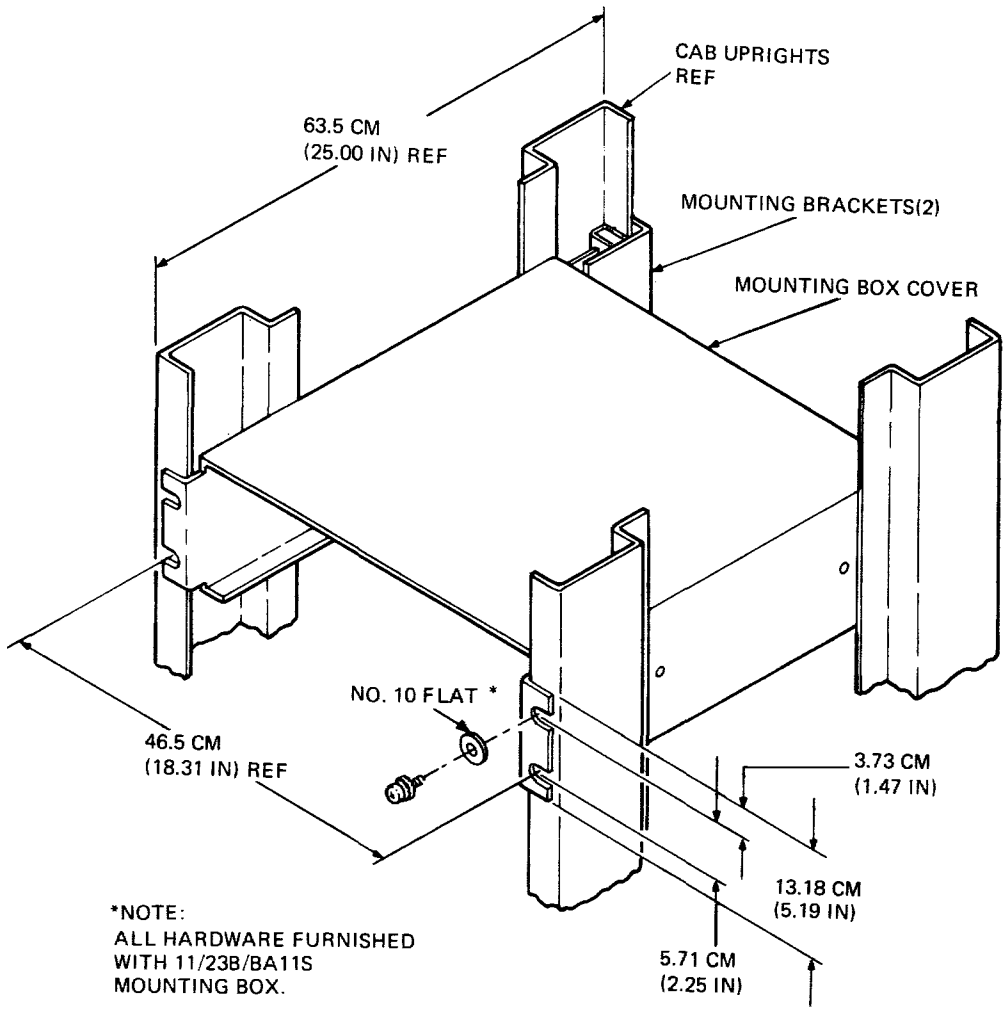


Figure 4 BA11-S Cover Mounting Dimensions

4. Attach the two mounting brackets to the cover using four 8-32 Phillips screws.
5. Attach the support brackets to the rear cabinet uprights using four Phillips 10-32 Phillips screws and four No. 10 flat washers.
6. Slide the unit into the cover. In the rear of the unit, attach a restraining cable to the stud on the H403-B ac input box with a No. 8 nut. Anchor the other end of the restraining cable the chassis or patch panel.
7. If the system is to be moved or shipped, the shipping screw must be replaced.

8. A safety restraining cable is located on the right rear side of the unit (when viewing from the front). This cable (DEC Part No. 12-15700-06), when attached to the rear of the AC input box, keeps the logic box base from being overextended. When the system unit is in the closed position, the restraining cable loops around at the rear of the unit inside the cover. When the base is pulled out from the cover to its extended position, the 44 cm (17-1/2-inch) restraining cable holds the box, preventing the base from accidentally being pulled completely out of the cover.

   To pull the base completely out of the cover, remove the nut on the H403-B ac input box stud, and then remove the restraining cable. Slide the base forward and set the base out of the way.

Installing the Logic Box Base in the Cover — Set the rear of the logic box base on the support flanges of the cover and slide the base in until it is in the closed position. Take care not to pinch the cables while sliding the base in.

NOTE

A stud extending from the H403-B ac input box is used to anchor a restraining cable (DEC Part No. 12-15700-06) to the patch panel, thereby preventing the logic box base from accidentally being pulled completely away from the cover assembly.

Perform the following steps to complete the installation

NOTE

The box being installed is either the main box, i.e., the one holding the CPU, or an expander base. Modify the following instructions to satisfy the type of box that is being installed; e.g., if there is a blank front panel, skip the first half of step 1.

1. Put the AUX switch in the front panel in the OFF position; put the ON/OFF switch on the ac input box in the OFF position.
2. When the AUX switch on the front panel is in the ON position, the two wires of the power controller cable are common. Connect the loose end of the cable to the input circuit of the power con-

troller so that the AUX switch controls the application of primary power to the controller. Keep the AUX switch in the OFF position.

3. To install the expanded LSI-11 bus expansion cable assemblies, open and remove the rear access door by turning the two quarter-turn screws in the lower corners of the door, then swing the door out and up to unhook it. Then put it aside. The BC02D cable and module configurations are listed in Table 1. When inserting the modules, make sure the connectors are on top.
4. After installing the correct module and cable, let the cable extend out of the rear opening, and replace the access door in the reverse of the way it was removed. Loosen the two Phillips screws on the correct cable strain relief to allow enough space for the cable to exit without binding when the box is extended. After installing the cables, retighten the two screws.

Table 1 Extended LSI-11 Bus Expansion Cable Assemblies

Assembly	Assembly Arrangement	Insert Modules In
BC02D	Two BC02D-03 cables	
	One M9404-00 module	Rows A and B of the first open slot after all other extended LSI-11 bus options have been installed in the main box.
	One M9405-YA module	Rows A and B of slot 1 of expander box 1

BA11-VA

BA11-VA MOUNTING CHASSIS/POWER SUPPLY

INTRODUCTION

The BA11-VA is a small form-factor package providing mounting space and power for four LSI-11/2 or LSI-11/23 family modules. This package, plus the high functionality of DIGITAL's microcomputer products, allows LSI-11 microcomputer applications to be implemented within a space smaller than that required for many eight-bit systems.

FEATURES

- Four slots for double 5.2 in × 8.9 in-(13.2cm × 22.8cm) high modules.
- LSI-11 bus backplane compatible with the LSI-11/2, LSI-11/23, and SBC-11/21 processors, memories, and interface modules.
- Power and cooling for modules.
- ac power indicator.
- Mounting hardware for tabletop or fixed-position usage.
- Off/On switch located at the rear of the unit.
- External connection to let users add a remote restart switch.
- UL listed, CSA certified, and complies with VDE and IEC requirements.

SPECIFICATIONS

Mechanical	
Capacity	4 dual LSI-11 bus modules
Size	11.7 in × 13.38 in × 3.62 in (29.71cm × 33.98cm × 9.19cm)
Weight	10 lb (4.5kg)
Mounting	4 rubber feet for table-top use and 4 metal brackets for fixed-position mounting (installed by user)
Environmental	
Operating Temperature	60°C (41°F) to 5°C (140°F)
Relative Humidity	10% to 95% (non-condensing)
Power	
Output	5.6 amps at +5V max 1.6 amps at +12V max

BA11-VA

Input Voltage	115Vac-50/60Hz or + 230V-50/ 60Hz (selectable by user)
Current	3.0 amps at 115V (maximum) 1.5 amps at 230V (maximum)
Power cord	6 ft 3 in (1.9m) for 115 Vac to be used with a NEMA 5-15P wall socket. User supplies cord for other power requirements.
External Connectors	
Optional Poweroutlet	Plug type (user-supplied) for use with the power outlet: 3-pin AMP™ plug—Part #1-480700-0 AMP contact pins—Part #350547-3
Remote Restart	Plug type (user-supplied) for use with the remote-restart outlet: 2-pin AMP plug—Part #1-480698-0. AMP contact pins—Part #350547-3
Model Number	BA11-VA—LSI-11 Bus mounting chassis and powersupply

DESCRIPTION

The BA11-VA is designed as a low-cost mounting enclosure for a wide range of mounting configurations. Two types of mounting hardware let the BA11-VA be used as a tabletop unit or be attached to a flat surface in any plane.

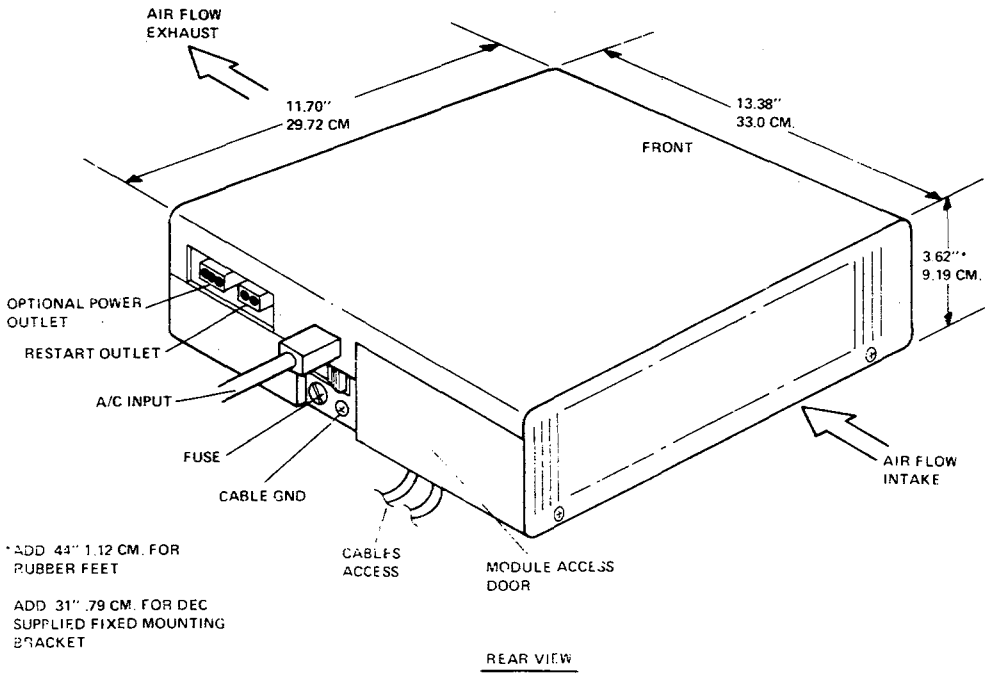
The BA11-VA does not generate a signal for use as a line-time clock in the processor module. If this function is required, the MXV11 multi-function module, which includes a 60Hz clock, should be used. If powerfail capability is needed, external hardware is required.

For applications where the mounting of the BA11-VA prevents easy user access to the chassis, the capability is provided for adding an external restart switch. A simple, single-pole/single-throw switch can be located up to ten feet from the box and connected using a standard connector. Momentary closure of this switch causes the processor to go to the user-selected powerup mode for the system.

The powersupply has more capacity than normally used by the four LSI-11 bus modules that can be mounted in the chassis. Therefore, a

connector is supplied to let this power be used for other electronic equipment located in the same area as the computer.

The BA11-VA powersupply can be configured through selector switches to operate throughout the world. The product is UL-listed, CSA- certified, and complies with VDE and IEC requirements.



BDV11

BDV11 DIAGNOSTIC, BOOTSTRAP, TERMINATOR

INTRODUCTION

The BDV11 module has 2K words of read-only memory (ROM) that contains both diagnostic programs and bootstrap programs. These programs are user-selectable by setting dip switches. The diagnostic programs test the processor, the memory, and the user's console. The bootstrap programs are used to boot a number of LSI-11-compatible peripherals. The module also contains 120-ohm bus terminator circuits.

Space is available on the module to allow the user to add up to 2K words of erasable programmable ROM (EPROM) and up to 16K words of ROM.

A HALT/ENABLE switch allows the user to start and stop the processor and a RESTART switch enables the user to reboot the system. The module also has four programmable light-emitting diodes (LEDs) that indicate a failure in a program and monitor the tests in progress. All the switches and indicators are edge-mounted on the module for easy access.

NOTE

There are two versions of the BDV11 module: revisions 0 and A. The revision 0 module was produced in limited quantities and does not incorporate all the characteristics of revision A. The differences between these modules are listed at the end of this section.

FEATURES

- Programmed ROMs with bootstraps for RXV11, RXV21, RLV11, and RKV11 disk options
- DECnet bootstraps for DLV11-E, DLV11-F, and DUV11 serial line units
- Capable of booting a system automatically with no operator intervention
- Can automatically load and start a 16K word program from ROM/EPROM to RAM
- 12-bit readable configuration register
- 16-bit read/write maintenance register

BDV11

- Software-controllable line-time clock (LTC)
- Power OK monitor, green LED
- 4-bit LED programmable display
- RESTART and HALT switches
- 120-ohm bus terminator

SPECIFICATIONS

Identification	M8012
Type	Quad
Power	+5 Vdc ±5% at 1.6 A +12 Vdc ±3% at 0.07 A
Bus Loads	
AC	2
DC	1

DESCRIPTION

The functions of the BDV11 are shown in Figure 1. The transceiver and control functions control the transfer of data between the bus and the BDV11. The ROM address function decodes the address data from the bus and uses the socket selection and ROM address functions to access the memory located on the BDV11. The ROM address function is also used to transfer data into the data selection function. Then data is placed on the LSI-11 bus by the control and transceiver functions. The data for the read/write registers are also transferred in and out by using the transceiver and control functions. The BDV11 uses power-up, BVENT, and display functions for monitoring program operations.

Transceiver

The transceiver logic monitors the LSI-11 bus BDAL lines for the address of a BDV11 register or the address of a ROM location. When a register or a ROM has been addressed, the transceiver logic gates the address onto the BDV11 DAL lines. If a register was addressed, the transceiver logic generates the address match signal that activates the control logic. If a ROM address was generated, then the DAL lines transfer the address to the ROM address selection logic. The transceiver logic is also used to transfer data from the DAL lines to the LSI-11 bus BDAL lines. When the transceiver receives XMIT H, the data can be from either a register or ROM address.

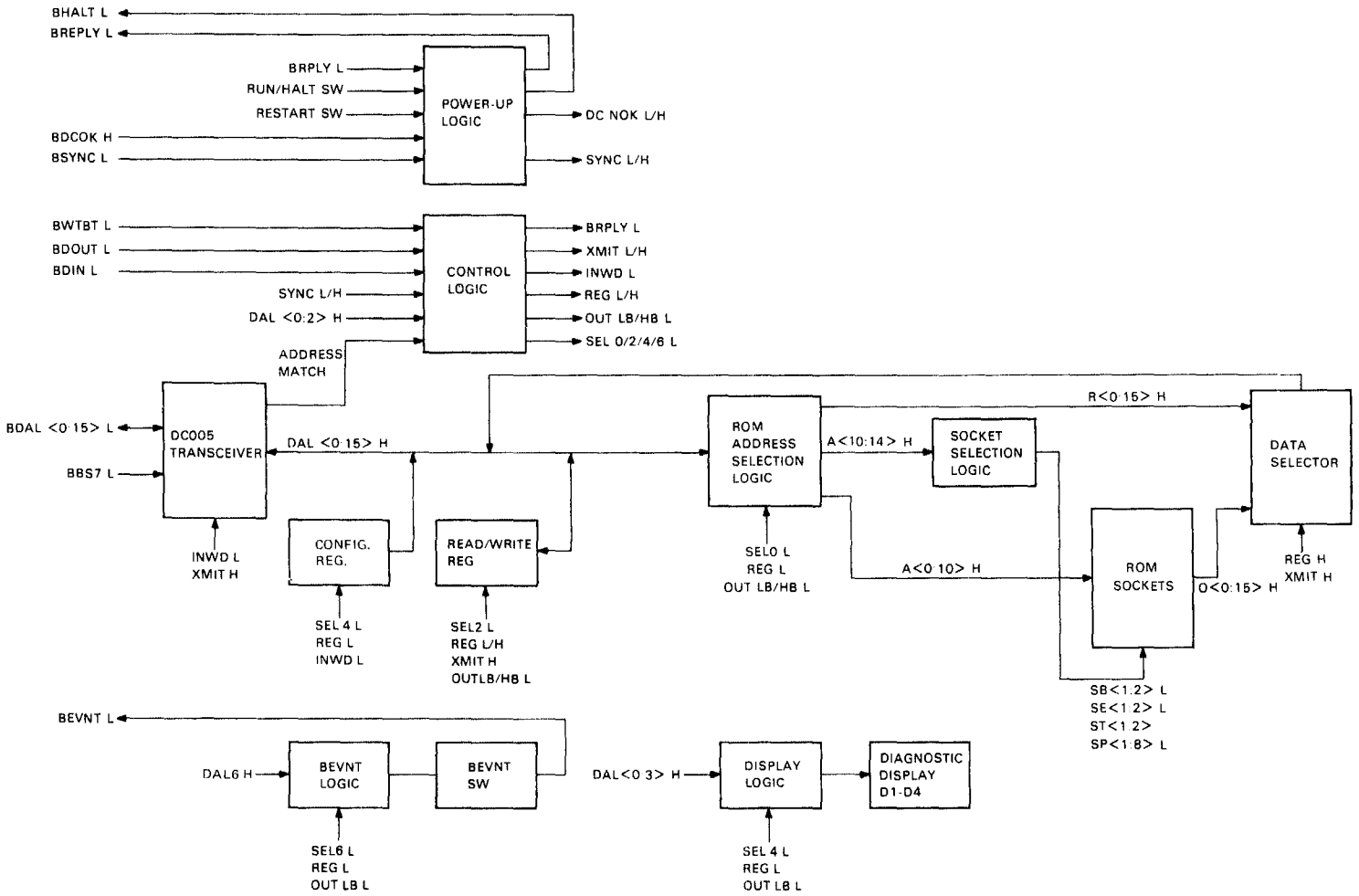


Figure 1 BDV11 Block Diagram

Control

The control logic consists of a DC004 protocol chip and an 82523 PROM. The control logic is enabled by the address match signal from the transceiver logic. The PROM monitors some of the DAL lines and the address match signal and generates an enable signal for the DC004 chip whenever any of the assigned bus addresses (173000 to 173777) is placed on the BDAL lines. The DC004 chip generates all the protocol signals used with the LSI-11 bus to allow data transfers. The control logic also generates the control signals for the read/write register's ROM address selection and the ROM socket selection logic. The bus control signals are defined in the appropriate processor handbook.

Read/Write Registers

The read/write register logic consists of two 8-bit universal shift registers. When the registers are being read, the control logic asserts XMIT H and the information on the DAL lines is the data within the shift registers. When the registers are to be written into, the XMIT signal is negated and the registers are placed into a load condition. The registers are clocked and the information on the DAL lines is loaded into the registers as data. The registers are cleared when power is turned on or when the system is booted.

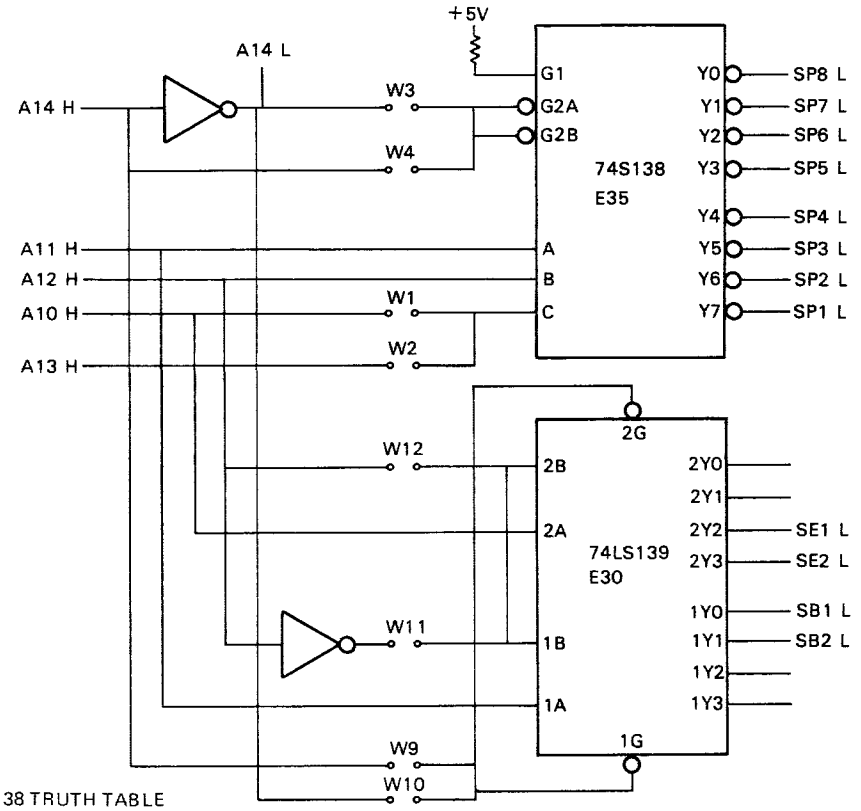
ROM Address Selection

The ROM address selection logic uses the contents of the PCR register and the LSI-11 bus address to determine the address of the BDV11 ROM locations. Each ROM has 2048_{10} addresses available. The logic selects the high byte of the PCR register if bit 8 of the LSI-11 bus is one and selects the low byte if bit 8 is a zero. The selected byte is shifted to the right one bit and used as the high byte of the BDV11 address. The low byte of the LSI-11 bus address is shifted one bit to the right and used as the low byte of the BDV11 address. The complete BDV11 ROM address is formatted by using a combination of the high and low bytes generated. Table 10 is a listing of how the PCR contents and the LSI-11 bus addresses are used to generate ROM addresses.

Socket Selection

The socket (or ROM) selection logic (Figure 2) consists of two decoders (E30 and E35) that provide the outputs used to select the high byte and low byte sockets. The user can program A10 H and A14 H inputs to these decoders by selecting jumper wires W1-W4 and W9-W12 to determine the configuration designation described in Table 2. The

SB1 L and SB2 L outputs are used to select the 4K of diagnostic/bootstrap DIGITAL programs. The SE1 L and SE2 L outputs are used to select the 2K words of user PROM. The SP1 L to SP8 L outputs are used to select the additional 16K words of user ROM.



74S138 TRUTH TABLE

G1	G2	C	B	A	OUT LOW
H	L	L	L	L	Y0 (SP8 L)
		L	L	H	Y1 (SP7 L)
		L	H	L	Y2 (SP6 L)
		L	H	H	Y3 (SP5 L)
		H	L	L	Y4 (SP4 L)
		H	L	H	Y5 (SP3 L)
		H	H	L	Y6 (SP2 L)
		H	H	H	Y7 (SP1 L)

74LS139 TRUTH TABLE (EACH HALF)

G	B	A	OUT LOW
L	L	L	YO(SB1 L)
	L	H	Y1 (SB2 L)
	H	L	Y2 (SE1 L)
	H	H	Y3 (SE2 L)

Figure 2 Socket Selection Logic

ROM Address

The ROM address logic uses the socket select logic outputs and address lines A0 to A10 to select the desired address. The diagnostic/bootstrap ROMs are enabled by SB1 L and SB2 L and are addressed by A0 to A10. The user EPROMs are enabled by SE1 L and SE2 L and are addressed by A0 to A9. The user ROM sockets are enabled by SP1 L to SP8 L and addressed by A0 to A9. The output data from the ROMs is sent to the data selector logic.

Data Selector

The data selector receives data from the ROMs and the registers of the BDV11. This data is stored until the outputs are enabled by XMIT. The data is then gated to the DAL0-15 bus lines where it is transferred to the LSI-11 bus by the transceiver and control logic.

Display

The display logic consists of four flip-flops and four LEDs. The contents of the display register (address 177524) are gated into the flip-flops and the outputs light the display LED indicators. The pattern of the display indicates to the user the type of program error when a failure occurs.

Power-up

The power-up logic includes the ENABLE/HALT switch and the RESTART switch. In normal operation, the ENABLE/HALT switch is in the ENABLE position. When the switch is placed in the HALT position, the bus signal BHALT L is asserted. The processor enters the halt mode and responds to the console ODT commands. To resume processor operation, the user must set the switch to ENABLE and enter a "P" command from the console.

The RESTART switch must be cycled to reboot the system. When the switch is cycled, a capacitor is charged to disable the bus BDCOK H signal and DCNOK L is asserted to initialize the BDV11 registers. When the capacitor discharges, the BDCOK H signal is enabled, the processor carries out a power-up sequence, and normal operation is resumed.

BVENT

The BVENT logic uses a switch located in E21 that lets the user control the LTC function. When the switch is open, the bus BVENT L signal can be controlled by the LTC signal generated in the LSI-11 bus power supply. When the switch is closed, the BVENT L signal can be controlled by the program.

CONFIGURATION

The BDV11 is factory-configured in Table 2 by DIGITAL to let the user expand the diagnostic and bootstrap programs by adding 2K words of EPROM and 16K words of ROM/EPROM memory. The user can modify the configuration for his own software requirements. Thirteen jumper wires are located on the module as shown in Figure 3 and identified in Table 1. Eight are used for selecting sockets, and five are used to accommodate various types of memory chips. The switches used to select programs are listed in the Programming section below.

Socket Selection

The socket selection logic is controlled by jumpers W1-W4 and W9-W12, which can be configured in seven different ways, as shown in Table 2. Group A assigns the PCR pages and socket selections. Groups B-G let the user choose where to begin program execution, such as having the processor execute instructions directly from a system ROM or EPROM when power is turned ON, rather than from the diagnostic/bootstrap ROM.

Table 1 Selectable Jumpers

Jumper	Function
W1	Socket selection
W2	Socket selection
W3	Socket selection
W4	Socket selection
W5	Chip selection
W6	Chip selection
W7	Chip selection
W8	Chip selection
W9	Socket selection
W10	Socket selection
W11	Socket selection
W12	Socket selection
W13	Chip selection

BDV11

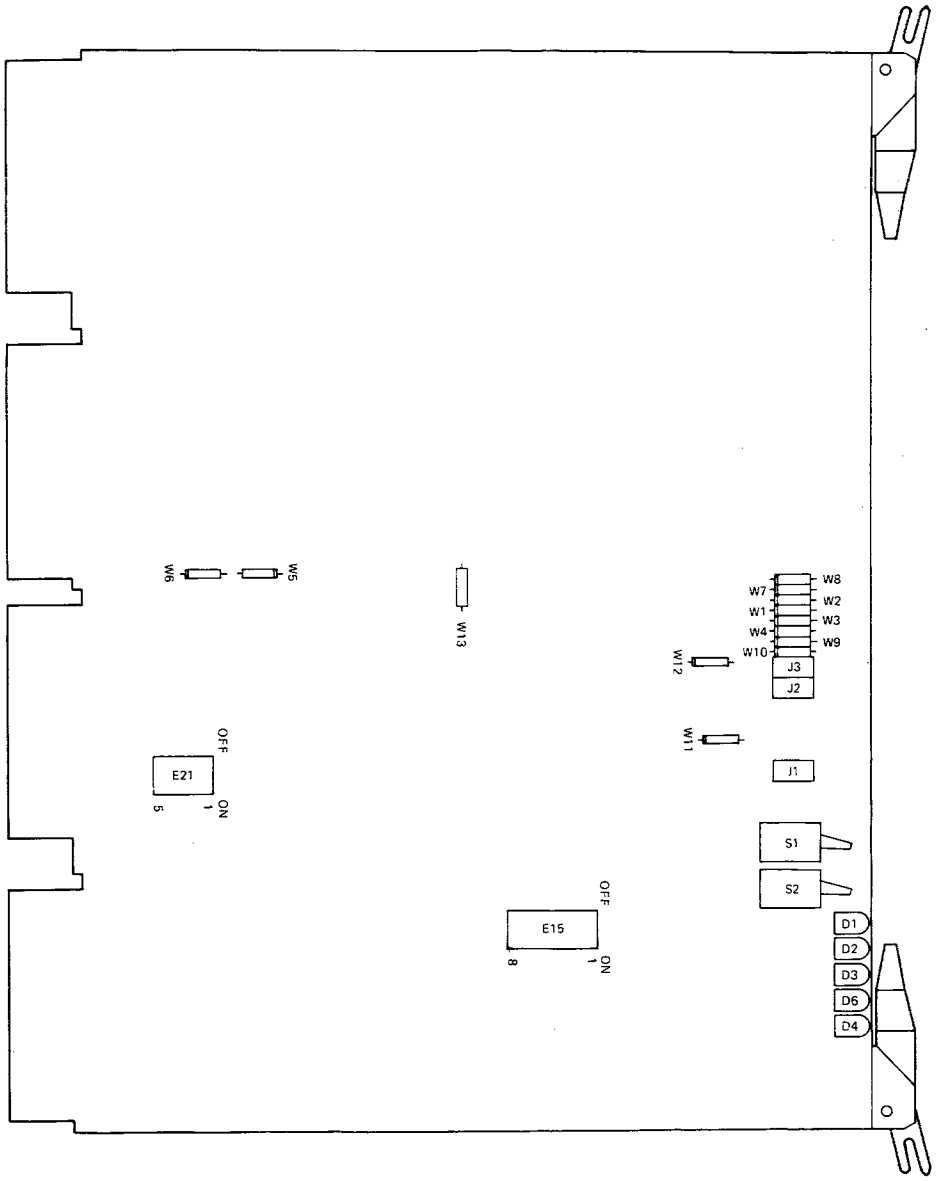


Figure 3 BDV11 Switch and Jumper Locations

Table 2 Memory Configuration

High Byte Socket	Low Byte Socket	Configuration Designation	ROM Address	PCR Page	Selection Signal
4K Diagnostic/Bootstrap (DIGITAL)					
E53	E48	A	0-2K	0-17	SB1 L
(2)	(1)	B	4K-6K	40-57	SB1 L
		C	16K-18K	200-217	SB1 L
		D	20K-22K	240-257	SB1 L
E58	E44	A	2K-4K	20-37	SB2 L
(4)	(3)	B	6K-8K	60-77	SB2 L
		C	18K-20K	220-237	SB2 L
		D	22K-24K	260-277	SB2 L
2K User EPROM					
E57	E40	A	4K-5K	40-47	SE1 L
(3)	(1)	B	0-1K	0-7	SE1 L
		C	20K-21K	240-247	SE1 L
		D	16K-17K	200-207	SE1 L
E52	E36	A	5K-6K	50-57	SE2 L
(4)	(2)	B	1K-2K	10-17	SE2 L
		C	21K-22K	250-257	SE2 L
		D	17K-18K	210-217	SE2 L

Table 2 Memory Configuration (Cont)

High Byte Socket	Low Byte Socket	Configuration Designation	ROM Address	PCR Page	Selection Signal
16K User ROM					
E54 (2)	E49 (1)	A	16K-18K	200-217	SP8 L
		E	16K-17K	200-207	SP8 L
		F	0-2K	0-17	SP8 L
		G	0-1K	0-7	SP8 L
E59 (4)	E45 (3)	A	18K-20K	220-237	SP7 L
		E	18K-19K	220-227	SP7 L
		F	2K-4K	20-37	SP7 L
		G	2K-3K	20-27	SP7 L
E60 (6)	E41 (5)	A	20K-22K	240-257	SP6 L
		E	18K-19K	240-247	SP6 L
		F	4K-6K	40-57	SP6 L
		G	4K-5K	40-47	SP6 L
E55 (8)	E37 (7)	A	22K-24K	260-277	SP5 L
		E	22K-23K	260-267	SP5 L
		F	6K-8K	60-77	SP5 L
		G	6K-7K	60-67	SP5 L

Table 2 Memory Configuration

High Byte Socket	Low Byte Socket	Configuration Designation	ROM Address	PCR Page	Selection Signal
16K User ROM (cont)					
E51	E38	A	24K-26K	300-317	SP4 L
(10)	(9)	E	17K-18K	210-217	SP4 L
		F	8K-10K	100-117	SP4 L
		G	1K-2K	10-17	SP4 L
E47	E42	A	26K-28K	320-337	SP3 L
(12)	(11)	E	19K-20K	230-237	SP3 L
		F	10K-12K	120-137	SP3 L
		G	3K-4K	30-37	SP3 L
E43	E46	A	28K-30K	340-357	SP2 L
(14)	(13)	E	21K-22K	250-257	SP2 L
		F	12K-14K	140-157	SP2 L
		G	5K-6K	50-57	SP2 L
E39	E50	A	30K-32K	360-377	SP1 L
(16)	(15)	E	23K-24K	270-277	SP1 L
		F	14K-16K	160-177	SP1 L
		G	7K-8K	70-77	SP1 L

BDV11

NOTE

The parenthetical numbers in the socket columns indicate the order for installing each ROM.

Memory Configuration

The user can change the configuration of the BDV11 memory structure by using socket selection jumpers W1-W4 and W9-W12; the standard configuration is in Table 2. This table also indicates the installation order for the PROM/ROM chips. The B, C, D, E, F, and G configurations show as alternate ways the user can map the ROM memory. Details about selecting a configuration using the socket selection jumpers are shown below.

Configuration	Socket Selection Jumpers*							
Designation	**W1**	**W2**	**W3**	**W4**	**W9**	**W10**	**W11**	**W12**
A	R	I	I	R	I	R	R	I
B	X	X	X	X	I	R	I	R
C	X	X	X	X	R	I	R	I
D	X	X	X	X	R	I	I	R
E	I	R	I	R	X	X	X	X
F	R	I	R	I	X	X	X	X
G	I	R	R	I	X	X	X	X

* I = Installed, R = Removed, X = Irrelevant

Chip Selection

The system ROM sockets can be occupied by either 2K ROMs or 1K ROMs. The ROM socket logic uses jumpers W5-W8 and W13 to select the type of ROM that can be used on the BDV11. Table 3 shows jumper configurations and the type of ROM or PROM used with these configurations.

Control Registers

The BDV11 module has five hardware registers that are software-addressable. These registers are assigned individual addresses that *cannot be changed or modified.* The registers are described in the following paragraphs; their designations and addresses are listed in Table 4.

Page Control Register (PCR) — This register is word- or byte-addressable and can be read or written. The PCR is a 16-bit register that consists of two 8-bit bytes. The low byte consists of bits 0-7 and the high byte consists of bits 8-15. When the low byte of the PCR is equal to page 6, then bus addresses 173000-173777 accesses the 128 ROM locations in the block 1400-1577. When a bus address falls in this range, the logic considers only the low byte of the PCR. However, if the bus address is in the range 173400-173777, only the high byte of the PCR is used to select the ROM location.

Table 3 Chip Selection Jumpers

	Jumpers Inserted[1]				
ROM Type	**W5**	**W6**	**W7**	**W8**	**W13**
2708[2]	R	I	R	I	R
2716[3]	R	R	I	R	I
8316E[4]	I	R	I	R	R
8316E[5]	R	R	I	R	I

NOTES

1. I = Inserted; R = Removed.
2. CB2 and DB2 must be supplied with external −5 V power.
3. Use only +5 Vdc type components.
4. Chip select signals must be programmed as follows:

CS1	CS2	CS3
LOW	LOW	LOW

5. Chip select signals must be programmed as follows:

CS1	CS2	CS3
LOW	LOW	HIGH

Table 4 Standard Assignments

Register	Read/ Write	Size	Address
Page Control	R/W	16 bits	177520
Read/Write	R/W	16 bits	177522
Configuration*	R	12 bits	177524
Display*	W	4 bits	177524
BEVNT*	W	1 bit	177546

* Dual-purpose register.

Table 5 relates the PCR contents to the PCR page for pages 0-17. If the PCR is loaded with data 000400, the PCR low byte contains data 000, while the high byte contains data 001. The PCR bytes can be loaded separately. To select ROM locations 1600-1777, for instance, one need only load the PCR high byte with page 7; thus, the high byte contains 007, while the low byte can contain anything. Table 6 lists the PCR contents for the remaining PCR pages.

Read/Write Register — This register is used as a maintenance register for the diagnostic programs. The register is cleared when power is turned on or when the RESTART switch is activated.

Configuration Register — This 12-bit read-only register is used to select for execution diagnostics or bootstrap programs for maintenance and system configuration. Bits 0-11 of the register are set by switches E15-1 through E15-8 and E21-1 through E21-4. These switches are associated with BDAL(0:11)L, when an individual switch is closed (on), the corresponding BDAL signal is low (1).

Display Register — This 4-bit register is used for program control of the diagnostic LED display. When bits 0-3 of the register are set, then the corresponding LEDs are off. The register is cleared by turning power ON or by activating the RESTART switch.

Table 5 PCR Contents/Page Relationship, Pages 0-17

PCR Page	PCR Contents	PCR High Byte (Bits 15-8)	PCR Low Byte (Bits 7-0)
0			
1	000400	001	000
2			
3	001402	003	002
4			
5	002404	005	004
6			
7	003406	007	006
10			
11	004410	011	010
12			
13	005412	013	012
14			
15	006414	015	014
16			
17	007416	017	016

Table 6 Pages 20-57, 200-377

Page	Contents	Page	Contents
20,21	010420	260,261	130660
22,23	011422	262,263	131662
24,25	012424	264,265	132664
26,27	013426	266,267	133666
30,31	014430	270,271	134670
32,33	015432	272,273	135672
34,35	016434	274,275	136674
36,37	017436	276,277	137676
40,41	020440	300,301	140700
42,43	021442	302,303	141702

Table 6 Pages 20-57, 200-377 (Cont)

Page	Contents	Page	Contents
44,45	022444	304,305	142704
46,47	023446	306,307	143706
50,51	024450	310,311	144710
52,53	025452	312,313	145712
54,55	026454	314,315	146714
56,57	027456	316,317	147716
200,201	100600	320,321	150720
202,203	101602	322,323	151722
204,205	102604	324,325	152724
206,207	103606	326,327	153726
210,211	104610	330,331	154730
212,213	105612	332,333	155732
214,215	106614	334,335	156734
216,217	107616	336,337	157736
220,221	110620	340,341	160740
222,223	111622	342,343	161742
224,225	112624	344,345	162744
226,227	113626	346,347	163746
230,231	114630	350,351	164750
232,233	115632	352,353	165752
234,235	116634	354,355	166754
236,237	117636	356,357	167756
240,241	120640	360,361	170760
242,243	121642	362,363	171762
244,245	122644	364,365	172764
246,247	123646	366,367	173766
250,251	124650	370,371	174770
252,253	125652	372,373	175772
254,255	126654	374,375	176774
256,257	127656	376,377	177776

BEVNT Register — Setting bit 6 (100_8) removes the clamp from BEVNT, thus enabling the line-time clock. Under program control, the user can clamp the BEVNT line low (thus stopping the line-time clock). Opening the BEVNT switch disconnects this function. The register is cleared (disabling the line-time clock) when the power is turned ON or when the RESTART switch is activated.

PROGRAMMING

The BDV11 contains dip switches that let the user select diagnostic and bootstrap programs for execution. Four LEDs indicate when a program fails. A green LED monitors the +12 Vdc and +5 Vdc and is lit when power is ON. A HALT/ENABLE switch and a RESTART switch let the user start and stop the processor. The switches and LEDs are shown in Figure 4.

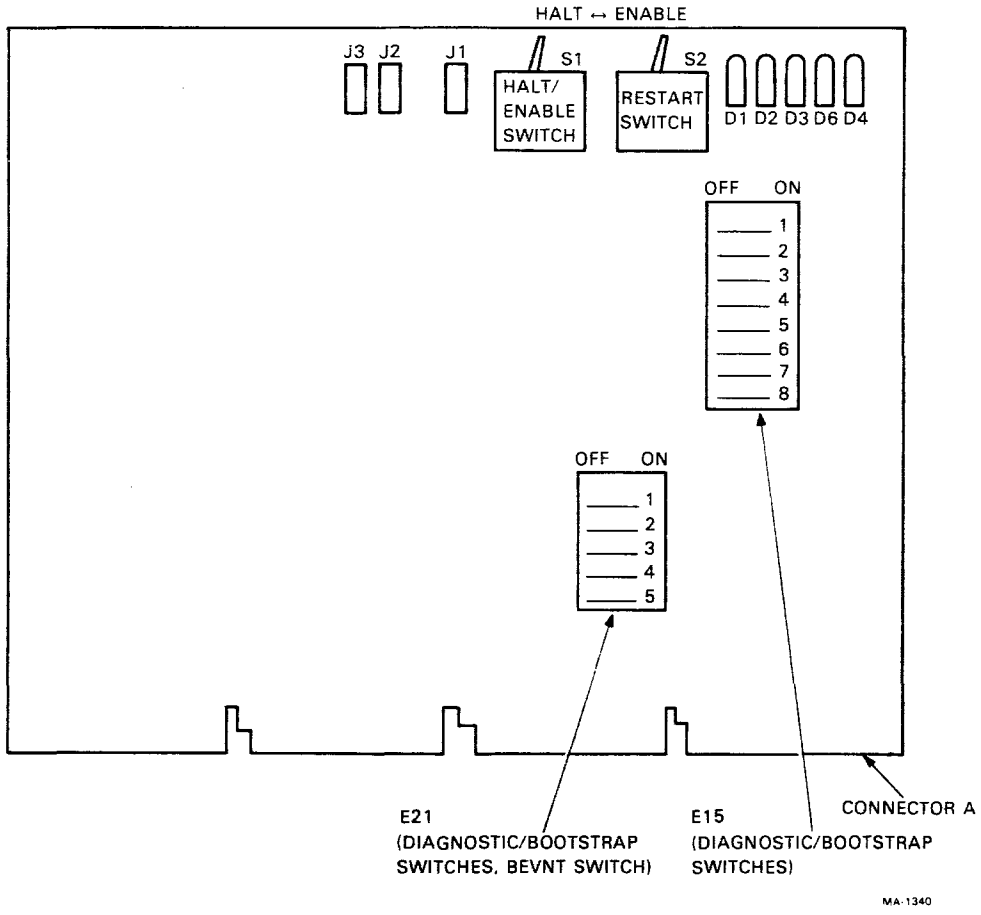


Figure 4 BDV11 Switches and Indicators

Diagnostic/Bootstrap Switches

Dip switch units E15 and E21 let the user select diagnostic programs and/or a bootstrap program. Switches A1-A8 represent switches 1-8

of E15, and switches B1-B4 represent switches 1-4 of E21. The programs selected by these switches are listed below. These 12 switches make up the configuration register that can be read at address 177524.

Switches A1-A4 are defined as follows:

A1	ON	Execute CPU test upon power-up or restart.
A2	ON	Execute memory test upon power-up or restart.
A3	ON	DECnet boot—A4, 5, 6, and 7 are arguments.
A4	ON	Console test and dialogue (A3 OFF).
A4	OFF	Turnkey boot dispatched by switch setting (A3 OFF).

DECnet boot arguments are:

Boot*	A4	A5	A6	A7
DUV11	ON	OFF	OFF	OFF
DLV11-E	OFF	ON	OFF	OFF
DLV11-F	OFF	ON	OFF	ON

All boots other than the DECnet boots above are controlled by the bit patterns in switches A5 through A8 and B1 (shown in Table 7) or, if the console test is selected, by mnemonic and unit number. The console test prompts with

```
xx
START?
```

where xx is the decimal multiple of 1024 words of RAM found in the system when sized from 0 up in 1024-word increments. The first word of each 1024-word segment is read and then written back into itself.

Allowed responses are a 2-character mnemonic with a 1-digit octal unit number or one of two special single-character mnemonics. The response must be followed by a RETURN. The special single-character mnemonics are:

Y	Use switch settings to determine boot device
N	Halt—enter microcode ODT

* DLV11-E CSR = 175610; DLV11-F CSR = 176500; DUV11 CSR = 160040 if no devices from 160010 to 160036.

Table 7 Diagnostic/Boostrap Switch Selection

Mnemonic	A5	A6	A7	A8	B1	Program Selected[1]
	0	0	0	0	0	
	0	0	0	0	1	Loop on test
DKn; n<8	0	0	0	1	0	RKV11 Boot
	0	0	0	1	1	
DLn; n<4	0	0	1	0	0	RLV11 Boot
	0	0	1	0	1	
	0	0	1	1	0	
	0	0	1	1	1	
DXn; n<2	0	1	0	0	0	RXV11 Boot
	0	1	0	0	1	
	0	1	0	1	0	
	0	1	0	1	1	
DYn; n<2	0	1	1	0	0	RXV21 Boot
	0	1	1	0	1	
	0	1	1	1	0	
	0	1	1	1	1	
	1	0	0	0	0	ROM Boot[2]
	1	0	0	0	1	
	1	0	0	1	0	
	1	0	0	1	1	
	1	0	1	0	0	
	1	0	1	0	1	
	1	0	1	1	0	
	1	0	1	1	1	
	1	1	0	0	0	
	1	1	0	0	1	
	1	1	0	1	0	
	1	1	0	1	1	
	1	1	1	0	0	
	1	1	1	0	1	
	1	1	1	1	0	
	1	1	1	1	1	

On = 1
Off = 0

1. All unused patterns or mnemonics will default to ROM boot if switch B2, B3, or B4 is on.
2. The ROM boot uses switches B2, B3, and B4 to dispatch as follows:

B2	B3	B4	ROM
1	X	X	Extended diagnostic
0	1	X	2708
0	0	1	Program ROM

where X = Irrevelant

If an unrecognized mnemonic or switch setting (A5 through B1) is encountered, B2, B3, and B4 are checked for the presence of additional ROM. If present, the ROM boot is invoked. The mnemonic's first character is placed in the high byte location of 2. Both characters are converted to uppercase with bit 7 cleared. Location 0 is loaded with the binary unit number. If an unrecognized switch setting is encountered instead, a copy of the switches is placed in location 2 with bit 15 set.

If no additional ROM exists, the switch-checking routine will halt or the mnemonic routine will reprompt.

The above features let the user implement additional features or boots in additional ROMs without changing to the base ROMs. If the additional ROM encounters an unrecognized mnemonic, it should load address 173000 into the PC, which will restart the BDV11 base ROM and reprompt.

Diagnostic Lights

When a failure occurs in a diagnostic test or in a bootstrap program, the diagnostic light display indicates the area of the failure as shown in Table 8. A failure causes the error to be indicated by the display and an error halt instruction is carried out by the processor. When entering the halt mode, the processor outputs the PC address at the time of the error on the console terminal. (The actual error address is one word less than the terminal printout.) In the halt mode, the processor responds to console ODT commands and the operator can troubleshoot the error. Table 9 lists the possible address and the cause of some errors.

BEVNT L Switch

Contact 5 of dip-socket switch E21 is the BEVNT L switch. When the switch is off (open), the LSI-11 bus BEVNT L signal can be controlled by the power supply-generated LTC signal. When the switch is on (closed), the LTC function is program-controlled, i.e., a single-bit, write-only register in the logic (address 177546, bit 6) clamps BEVNT L low when the register is cleared. (The register is automatically cleared when the power is turned on or when the RESTART switch is cycled.)

Power OK LED

This green LED is lit when the +12 Vdc supply voltage is greater than +10 V and the +5 Vdc supply voltage is greater than +4 V for normal operating conditions. The +12 Vdc voltage and the +5 Vdc voltage can be measured at the tip jacks as indicated below. (Both J2 and J3 have a 560-ohm resistor in series to prevent damage from a short circuit; use at least a 20,000 ohm/V meter to measure the voltage.)

Jack	Color	Voltage
J1	Black	Ground
J2	Red	+5 Vdc
J3	Purple	+12 Vdc

HALT/ENABLE Switch

When this switch is in the ENABLE position, the processor can operate program control. If the switch is placed in the HALT position, the processor enters the halt mode and responds to console ODT commands. While in the halt mode, the processor can execute single instructions for system maintenance. Program control is reestablished by returning the switch to the ENABLE position and entering a "P" command at the console terminal (providing the contents of register R7 were not changed). Refer to the appropriate processor handbook for a description of console ODT command usage.

Table 8 Diagnostic LED Error Display (D1-D4)*

D4 Bit 3	D3 Bit 2	D2 Bit 1	D1 Bit 0	Comments* (Type of Error)
On	On	On	On	System hung; halt switch on or power-up mode wrong.
Off	Off	Off	On	CPU, fault, or configuration error.
Off	Off	On	Off	Memory error; R1 points to bad location.
Off	Off	On	On	Console SLU will not transmit.
Off	On	Off	Off	Waiting for response from operator.
Off	On	Off	On	Load device fault.
Off	On	On	Off	Secondary boot incorrect (location 0 not a NOP).
Off	On	On	On	DECnet waiting for response from host.
On	Off	Off	Off	DECnet; received done flag set.
On	Off	Off	On	DECnet; message received.
On	Off	On	Off	ROM bootstrap error.

* The light pattern indicates the corresponding test is in progress or failed. Some tests retry (DECnet) and others will halt the CPU (CPU, memory, non-DECnet boots).

Table 9 List of Error Halts

Address of Error	Cause of Error
173 022	Memory error 1. Write address into itself.
173 040	SLU switch selection incorrect. Error in switches.
173 046	SLU error. CSR address for selected device. Check CSR for selected device in floating CSR address area.

Table 9 List of Error Halts (Cont)

Address of Error	Cause of Error
173 050	CP1 error. R0 contains address of error.
173 052	Memory error 2. Data test failed.
173 106	Memory error 3. Write and read bytes failed.
173 202	ROM loader error. Checksum on data block.
173 240	CP4 error. R0 contains address of error.
173 366	ROM loader error. Checksum on address block.
173 402	ROM loader error. Jump address is odd.
173 532	RL device error.
173 634	CPU error 3. R0 points to cause of error.
173 642	In console terminal test, a "no" typed.
173 656	RK device error.
173 656	Switch mode halt. Match was not made with switches.
173 670	Console terminal test. No done flag.
173 706	CPU error 2. R0 points to cause of error.
173 712	RX device error.

RESTART Switch

When the RESTART switch is cycled, i.e., moved from one side to the other and back, the CPU automatically carries out a power-up sequence. Thus, for maintenance purposes, the system can be rebooted at any time.

Addressing ROM on the BDV11 module

A block of 256 LSI-11 bus addresses is reserved to address the ROM locations on the BDV11 module. This block resides in the upper 4K address bank (28K-32K), which is normally used for peripheral-device addressing, and consists of byte addresses 173000-173776.

All 2048 locations in a selected 2K ROM (or 1024 locations in a 1K ROM) can be addressed by just these 256 bus addresses. The logic includes a page control register (PCR) at bus address 177520; the contents of this read/write register determine which specific ROM location is accessed when one of the 256 bus addresses is placed on the BDAL lines. The PCR is loaded with "page" information, i.e., the PCR contents point to 1 of 16 (or 1 of 8) 128-word pages in the selected ROM (16 pages × 128 words = 2048 words). For example, if the PCR contents represent pages 0 and 1, then bus addresses 173000-173776 access ROM locations 0000-0377; if the PCR contents represent pages 10 and 11, then bus addresses 173000-173776 access ROM locations 2000-2377. Table 10 relates bus addresses, PCR pages, and ROM locations.

At the top of each column of PCR pages in Table 10 appear two circuit component designations; column 1, for example, is headed by E53/E48. These designations represent the ROMs and EPROMs that one might find on a BDV11 module. For instance, the BDV11 is supplied with 2K words of diagnostic ROM. The ROM inserted in socket XE53 supplies the high byte (bits 8-15) of these 2K words, while the ROM inserted in socket XE48 supplies the low byte (bits 0-7). To access the BDV11 diagnostic ROM locations, the user must load the PCR with the pages in column 1; thus, when 12 and 13, for example, are loaded into the PCR, diagnostic ROM locations 2400-2777 can be addressed by the LSI-11 BDAL signals. Another variation of the BDV11 could have 1K-word EPROMs inserted in sockets XE57—XE40 (E57 supplies the high byte, while E40 supplies the low byte). To access these EPROM locations, the user would load the PCR with pages in column 3; thus, with 44 and 45 in the PCR, EPROM locations 1000-1377 are accessible.

Table 10 BDV11 Bus Address/PCR Pages

ROM Location Bus Address Accessed	PCR Pages E53/ E48	E58/ E44	E57/ E40	E52/ E36	E54/ E49	E59/ E45	E60/ E41	E55/ E37	E51/ E38	E47/ E42	E43/ E46	E39/ E50
173000-173376 0000-0177	0	20	40	50	200	220	240	260	300	320	340	360
173400-173777 0200-0377	1	21	41	51	201	221	241	261	301	321	341	361
173000-173376 0400-0577	2	22	42	52	202	222	242	262	302	322	342	362
173400-173777 0600-0777	3	23	43	53	203	223	243	263	303	323	343	363
173000-173376 1000-1177	4	24	44	54	204	224	244	264	304	324	344	364
173400-173777 1200-1377	5	25	45	55	205	225	245	265	305	325	345	365
173000-173376 1400-1577	6	26	46	56	206	226	246	266	306	326	346	366
173400-173777 1600-1777	7	27	47	57	207	227	247	267	307	327	347	367

Table 10 BDV11 Bus Address/PCR Pages (Cont)

ROM Location Bus Address Accessed	PCR Pages E53/ E48	E58/ E44	E57/ E40	E52/ E36	E54/ E49	E59/ E45	E60/ E41	E55/ E37	E51/ E38	E47/ E42	E43/ E46	E39/ E50
173000-173376 2000-2177	10	30			210	230	250	270	310	330	350	370
173400-173777 2200-2377	11	31			211	231	251	271	311	331	351	371
173000-173376 2400-2577	12	32			212	232	252	272	312	332	352	372
173400-173777 2600-2777	13	33			213	233	253	273	313	333	353	373
173000-173376 3000-3177	14	34			214	234	254	274	314	334	354	374
173400-173777 3200-3377	15	35			215	235	255	275	315	335	355	375
173000-173376 3400-3577	16	36			216	236	256	276	316	336	356	376
173400-173777 3600-3777	17	37			217	237	257	277	317	337	357	377

As Table 10 implies, the PCR pages are assigned to specific module ROM sockets. Furthermore, the sockets are assigned specific kinds of ROMs, as Table 11 indicates, e.g., the diagnostic/bootstrap ROM can occupy only sockets XE53 and XE48. Thus, a specific ROM can be addressed only when the PCR contains the page or pages assigned to the socket that the ROM occupies. For example, if 2K-word ROMs are inserted in sockets E39 and E50, they can be addressed only when the PCR contains pages 360-377. The page/socket assignments indicated in Table 10 apply to the BDV11 module shipped by DIGITAL. There are eight locations on the BDV11 printed circuit board in which jumpers are inserted selectively to achieve these assignments. The user can change the factory arrangement of these jumpers to cause the CPU to execute instructions directly from a ROM or EPROM of the user's choice when power is turned on, rather than from the diagnostic ROMs.

Table 11 Functions of ROM Sockets

Sockets	ROM Function	Sockets	ROM Function
XE53/XE48	2K Diagnostic/Bootstrap	XE47/XE42	2K System ROM
XE58/XE44	2K Diagnostic/ Bootstrap (reserved for DIGITAL)	XE51/XE38	2K System ROM
XE57/XE40	1K EPROM	XE55/XE37	2K System ROM
XE52/XE36	1K EPROM	XE60/XE41	2K System ROM
XE39/XE50	2K System ROM	XE59/XE45	2K System ROM
XE43/XE46	2K System ROM	XE54/XE49	2K System ROM

Loading ROM into RAM

A utility is provided in the BDV11 firmware which loads user programs from ROM to RAM at specified (and possibly scattered) addresses and transfers control to a specified address. This allows a programmer to write a program (to be stored in ROM) without knowing the BDV11 mapping hardware or having to "ROMize" the program. This utility loads the DIGITAL-reserved space, the 2K EPROM, or the 16K ROM/EPROM areas. The utility uses the four highest words of RAM (<30K) as scratch space.

The format is a modified version of absolute loader paper tape format. The standard format consists of sequential blocks, organized by byte, as follows:

1 BYTE	This indicates start of block.
0 BYTE	Required.
BCL	Low-order eight bits of byte count.
BCH	High-order eight bits of byte count.
ADL	Low-order eight bits of load address.
ADH	High-order eight bits of load address.
DATA	Sequential bytes of data.
CKB	Checksum byte.

These frames are repeated as required until a starting address block is encountered. This is indicated by a byte count of six, which is too short to allow a data field. The load address of this block is used as the starting address.

The format skips every 255th and 256th location in the ROM pattern. These locations are filled with checking information which allows DIGITAL diagnostics to determine whether the ROMs are good and inserted in the correct socket.

The ROMs should be inserted as indicated by the ROM address chart. The user program may be patched by changing only the last ROM of a set and by adding a new data block(s) before the starting address block. This block will overlay previously loaded data.

Executing ROMs in the I/O Page

ROMs may be executed in the I/O page provided their starting address is between 173016 and 173376.

DC319-AA DLART

INTRODUCTION

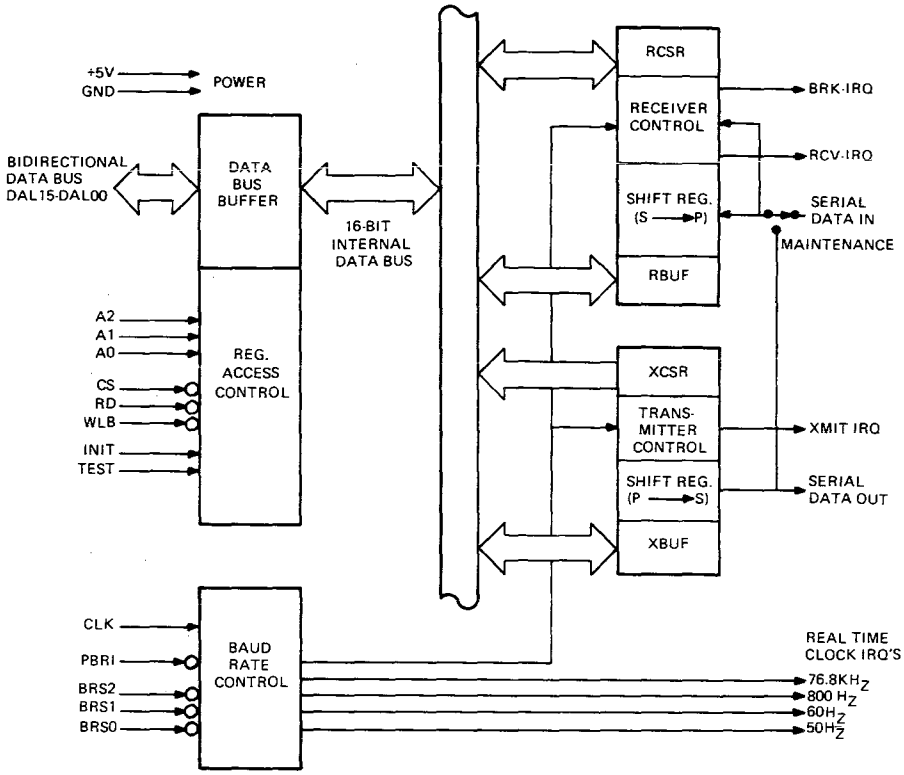
Digital's DC319-AA DLART is a DL-compatible, asynchronous receiver/transmitter designed for data communications with Digital's microprocessor family. The DLART is used as a peripheral device. It is programmed by the CPU to operate either in 8-bit or 16-bit mode with asynchronous baud rates varying from 300 to 38.4K. The DLART accepts data characters from the CPU in parallel format and converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The DLART will signal the CPU whenever it can accept new characters for transmission or whenever it has received a character from the CPU.

The DLART also has an internal baud rate control to reduce support logic and provides four realtime interrupt outputs to support dynamic memory refresh for realtime system applications. The CPU can read the complete status of the DLART at any time. The status includes data transmission errors and control signals such as BRK-IRQ and RCV-IRQ. The DLART does not handle device address detection, vector generation, and interrupt arbitration. These must be handled outside the DLART. The DLART provides the DL-defined internal registers: RCSR, RBUF, XCSR, XBUF. Thus, standard Digital software will work with the DLART. The chip is fabricated in N-channel MOS silicon technology.

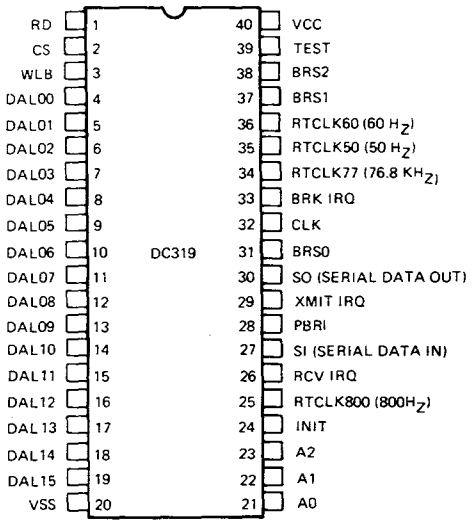
FEATURES

- Asynchronous operation
- Error detection-overrun, framing, and brake generation
- Compatible with both 8- and 16-bit modes of the micro T-11 microprocessor
- Internal baud rate generation from 300 baud to 38.4K baud
- Four realtime clock interrupt outputs to support dynamic memory refresh for realtime system applications
- One stop bit only
- Common baud rate for both transmitter and receiver
- 40-pin DIP package
- Single +5 V supply
- Single TTL clock

DC319-AA DLART



DLART Block Diagram



DLART Pin Locations

PIN DESCRIPTIONS

Pin Functions

Pin No.	Name	Asserted State	Description
1	RD	Low	Read When asserted while CS is asserted and WLB is unasserted, this control input causes the contents of the register selected by the A2, A1 and A0 lines to drive the DAL lines. This line has no effect if CS is unasserted or if WLB is asserted.
2	CS	Low	Chip Select This input is asserted to permit data transfers through the DAL lines to or from the internal registers under control of the RD or WLB lines. When this line goes from asserted to unasserted while WLB is asserted and A0 is unasserted, data on the low byte of the DAL lines is written into the writable bits of the register selected by the A2, A1 lines.
3	WLB	Low	Write Low Byte When this input goes from asserted to unasserted while CS is asserted and A0 is unasserted, data on the low byte of the DAL lines is written into the writable bits of

Pin No.	Name	Asserted State	Description
			the register selected by the A2, A1 lines. This line has no effect on internal registers if CS is unasserted or A0 is asserted.
4-19	DAL	High	Data I/O Lines The receivers are active at all times. The drivers are active only when CS and RD are asserted and WLB is unasserted. The drivers will go inactive (tristate) within 50 ns whenever one or more of the following occurs: (1) CS goes unasserted, (2) RD goes unasserted, or (3) WLB goes asserted.
21	A0	High	Register Byte Select When this input is asserted, the high byte of the register selected by A2, A1 is multiplexed to the low byte of the DAL lines. Reading is normal, but attempts to write have no effect.
22, 23	A2-1	High	Register Address Select These inputs determine which DLART internal register is accessible through the DAL lines when the ES line is asserted.

Pin No.	Name	Asserted State	Description
			AA21 Register 00 RCSR 01 RBUF 10 XCSR 11 XBUF
24	INIT	High	Init This input is used to reset only the RCV IE bit in the RCSR register, and the XMIT IE, MAINT, and XMIT BRK bits in the XCSR register.
25	RTCLK800	High	800 Hz Realtime clock Interrupt This output provides an 800 Hz, 50% duty cycle signal. After being high for a minimum of 500 ns, this output can be cleared externally by being forced low (clamped to ground) with an open collector transistor for a minimum of 100 ns.
26	RCV IRQ	High	Receiver Interrupt Request This interrupt output is asserted only when both the RCV DONE and RCV IE bits in the RCSR are set. This output can also be cleared externally by being forced low (clamped to ground) by an open collector transistor

Pin No.	Name	Asserted State	Description
			for a minimum of 100 ns after being high for a minimum of 500 ns.
27	SI	High	Serial Input This input accepts an asynchronous bit serial data stream. The input signal must remain in the high (marking) state for at least one half bit time before a high-to-low (mark-to-space) transition is recognized. A mark-to-space transition is required to determine the beginning of a start bit and initiate data reception.
28	PBRI	Low	Programmable Baud Rate Inhibit This input is optionally held low externally by a jumper to ground or held high internally. Holding this line low disbles software programmable baud rate selection (clears the PBR2-0 and PBRE bits) but makes the DLART DL-software compatible.
29	XMIT IRQ	High	Transmitter Interrupt Request This interrupt request output is asserted only when both the XMIT RDY and XMIT IE bits in the XCSR are set. This output

Pin No.	Name	Asserted State	Description
			can also be cleared externally by being forced low (clamped to ground) by an open collector transistor for a minimum of 100 ns after being high for a minimum of 500 ns.
30	SO	High	Serial Output This output provides an asynchronous bit serial data stream. This line remains high (marking) when no data is being transmitted. This line will remain low when the XMIT BRK bit in the XCSR register is set.
32	CLK	High	Clock In This input requires a 614.4 KHz ± 0.1% square wave. All baud rates and clocks are derived from this input.
33	BRK IRQ	High	Break Detected Interrupt Request This interrupt request output is asserted when the RCV BRK bit is set and is unasserted by TEST or when the RBUF is read. This output can also be cleared externally by being forced low (clamped to ground) by an open collector transistor for a minimum of 100 ns after being high for a minimum of 500 ns.

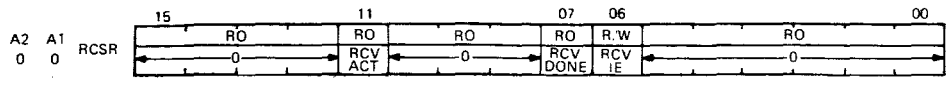
Pin No.	Name	Asserted State	Description
34	RTCLK77	High	76.8 KHz Realtime Clock Interrupt This output provides a 76.8 KHz, 50% duty cycle signal. After being high for a minimum of 500 ns, this output can be cleared externally by being forced low (clamped to ground) with an open collector transistor for a minimum of 500 ns.
35	RTCLK50	High	50 Hz Realtime Clock Interrupt This output provides a 50 Hz, 50% duty cycle signal. After being high for a minimum of 500 ns, this output can be cleared externally by being forced low (clamped to ground) with an open collector transistor for a minimum of 100 ns.
36	RTCLK60	High	60 Hz Realtime Clock Interrupt This output provides a 60 Hz, 50% duty cycle signal. After being high for a minimum of 500 ns, this output can be cleared externally by being forced low (clamped to ground) with an open collector transistor for a minimum of 100 ns.

Pin No.	Name	Asserted State	Description
38	BRS2-0	Low	Baud Rate Select These inputs provide for external baud rate selection. These inputs are optionally asserted low externally by a jumper to ground or held high internally. The receiver and transmitter baud rate is determined by these lines when the PBRE bit is clear.
39	TEST	High	Test This input is used during module assembly and test to disable all DLART outputs. It is also used in a system during powerup to reset all internal logic.

PBR 210	Baud Rate	BRS 210
000	300	HHH
001	600	HHL
010	1200	HLH
011	2400	HLL
100	4800	LHH
101	9600	LHL
110	19200	LLH
111	38400	LLL

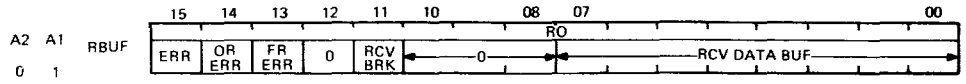
REGISTERS

Receiver Control/Status Register (RCSR)



Bit	Name	Description
15-12	0	Zero (Read-Only) These bits are always read as zeros.
11	RCV ACT	Receiver Active (Read-Only) When this bit is set, the receiver is active. Set at the center of the start bit which is the beginning of the input serial data and cleared one bit time prior to the leading edge of RCV DONE or TEST.
10-08	0	Zero (Read-Only) These bits are always read as zeros.
07	RCV DONE	Receiver Done (Read-Only) This bit is set when an entire byte has been received and transferred to the RCV DATA BUFFER. This bit is cleared by reading the RCV DATA BUFFER or by TEST.
06	RCV IE	Receiver Interrupt Enable (Read/Write) When this bit is set under program control, the RCV IRQ line follows the RCV DONE bit. This allows an interrupt request to be made when RCV DONE is set. This bit is cleared by INIT and by TEST.
05-00	0	Zero (Read-Only) These bits are always read as zeros.

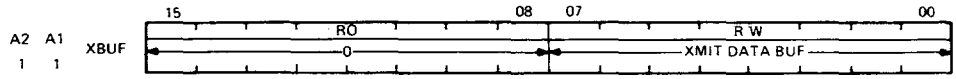
Receiver Buffer Register (RBUF)



Bit	Name	Description
15	ERR	Error (Read-Only) This bit is set when the overrun or the framing error bit is set and cleared by removing the error-producing condition.
14	OR ERR	Overrun Error (Read-Only) This bit is set when a received byte is transferred to the RCV DATA BUFFER before the RCV DONE bit is cleared. An overrun error indicates that reading of the previously received byte was not completed prior to receiving a new byte. This bit is updated when a byte is transferred to the RCV DATA BUFFER and is cleared by TEST.
13	FR ERR	Framing Error (Read-Only) This bit is set when a received byte without a valid stop bit is transferred to the RCV DATA BUFFER. This bit is cleared by TEST or when a received byte with a valid stop bit is transferred to the RCV DATA BUFFER.
12	0	Zero (Read-Only) This bit is always read as a zero.
11	RCV BRK	Received Break (Read-Only) This bit is set when the serial-in (SI) signal goes from a mark to a space and stays in the

Bit	Name	Description
		space condition for 11 bit times after serial reception starts. This bit is cleared when the SI signal returns to the mark condition or by TEST.
10-08	0	Zero (Read-Only) These bits are always read as zeros.
07-00	RCV DATA BUFFER	Received Data Buffer (Read-Only) These 8 bits hold the most recent byte received. When a new byte is transferred to the RCV DATA BUFFER, the RCV DONE bit in the RCSR is set. These bits are cleared by TEST.

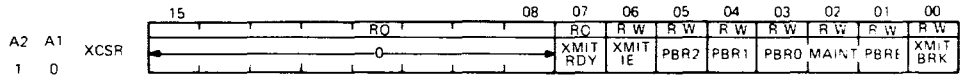
Transmitter Data Buffer (XBUF)



Bit	Name	Description
15-08	0	Zero (Read-Only) These bits are always read as zeros.
07-00	XMIT DATA BUFFER	Transmitter Data Buffer (Read/Write) This byte register holds a copy of the most recent byte written into it. When a byte is written into this register, the XMIT RDY bit in the XCSR register is cleared. This byte is copied into the transmitter serial output register whenever that register is empty and the XMIT RDY bit is clear. The XMIT RDY

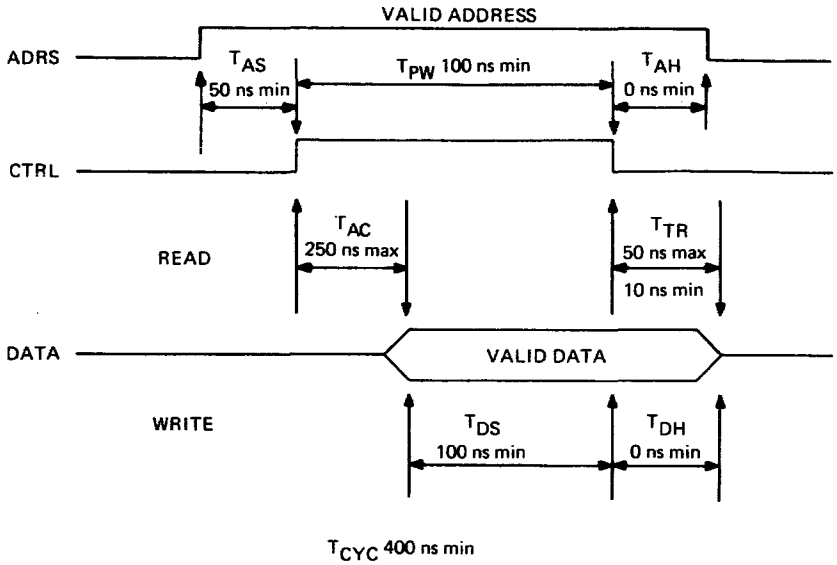
Bit	Name	Description
		bit is set when a byte is copied from the XMIT DATA BUFFER into the serial output register. Reading the contents of this register causes no other effect. This register is cleared by TEST.

Transmitter Control/Status Register (XCSR)



Bit	Name	Description
15-08	0	Zero (Read-Only) These bits are always read as zeros.
07	XMIT RDY	Transmitter Ready (Read-Only) This bit is set when the XMIT DATA BUFFER is ready to accept a byte. This bit is cleared by writing to the XMIT DATA BUFFER and is set by TEST.
06	XMIT IE	Transmitter Interrupt Enable (Read/Write) When this bit is set under program control, the XMIT IRQ line follows the XMIT RDY bit. This allows an interrupt request to be made when XMIT RDY is set. This bit is cleared by INIT and by TEST.
05-03	PBR2-0	Programmable Baud Rate Select* When the PBRE bit is set, these bits determine the baud rate as shown in the table under the BRS2-0 pins. These bits are

Bit	Name	Description
		cleared by TEST or PBRI (programmable baud rate inhibit).
02	MAINT	Maintenance (Read/Write) This bit is used to facilitate a maintenance self-test. When this bit is set, the transmitter serial output is connected to the receiver serial input while disconnecting the external serial input. This bit is cleared by INIT and by TEST.
01	PBRE	Programmable Baud Rate Enable* This bit selects between internal and external baud rate selection. When set, the baud rate is determined by the PBR2-0 bit in this register. When clear, the baud rate is determined by the BRS2-0 pins. This bit is cleared by TEST or PBRI (programmable baud rate inhibit).
00	XMIT BRK	Transmit Break (Read/Write) When this bit is set, the serial output (SO) line is forced to a space condition. This bit is cleared by INIT and by TEST.



NOTE: READ CONTROL EQUALS CS ASSERTED AND RD ASSERTED AND WLB UNASSERTED.

WRITE CONTROL EQUALS CS ASSERTED AND WLB ASSERTED AND AO UNASSERTED.

Write/Read Data and Control Cycle

NOTE

READ CONTROL EQUALS CS ASSERTED AND RD ASSERTED AND WLB UNASSERTED.

WRITE CONTROL EQUALS CS ASSERTED AND WLB ASSERTED AND AO UNASSERTED.

DC319-AA DLART

AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5.0 V ± 5%, GND = 0 V)

Symbol	Parameter	Min.	Max.
T_{cyc}	Cycle time	400ns	
T_{pw}	Controlling pulse width	100 ns	
T_{as}	Address set-up time	50 ns	
T_{ah}	Address hold time	0 ns	
T_{ac}	Access time	0 ns	250 ns
T_{tr}	Tristate time	10 ns	50 ns
T_{ds}	Data set-up time	100 ns	
T_{dh}	Data hold time	0 ns	

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias 0° to 70°C

Storage Temperature −65°C to −150°C

Voltage On Any Pin With Respect To Ground −0.5 V to *min7 V

Power Dissipation 1 W

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DCK11-AA, -AC PROGRAM TRANSFER INTERFACE

INTRODUCTION

The DCK11-AA and -AC CHIPKITs provide the logic necessary for a program transfer interface to the LSI-11 bus.

The DCK11-AA kit contains:

1-DC003 Interrupt Chip
1-DC004 Protocol Chip
4-DC005 Transceiver/Address Decoder/Vector Select Chips

The DCK11-AC kit contains the above chips plus:

1-W9512 double-height, extended-length, high-density wire-wrappable module
1-BC07D-10 ten-foot, 40-conductor plug-in cable

Figure 1 shows a schematic of the program control CHIPKIT part of a user's interface.

FEATURES

DC003 Interrupt Logic IC Features

- Two interrupts (A & B) per DC003
- Interrupt enable flip-flop on the IC
- Enable flip-flop outputs available to the user
- Interrupts initially disabled by BUS INIT
- VECTOR output to the DC005s to gate the Interrupt Vector address directly onto the LSI-11 bus
- Interrupt B generates the second LSB of vector address directly (VECRQST B H)
- BUS INIT buffered and made available to the user (INITO L)
- Contains logic for LSI-11 bus "daisy-chained" interrupts

DC004 Protocol Logic IC Features

- Device selection features
  - Four register select lines (SEL 6 L, SEL 4 L, SEL 2 L, SEL 0 L)
  - High and low byte output select lines (OUTHB L, OUTLB L)
  - Input select line (INWD L)
  - Enable input from higher level decode (ENB H)
- Bus functions
  - Bus reply generated for device addresses and for interrupts (BRPLY L)
  - Ability to vary bus reply response by adding an RC network provided (RXCX H)

DC005 Bus Transceiver IC Features

- Four bits per IC
- Three bits of address selection logic included on the chip
- LSI-11 bus drivers and receivers
  - Drivers—open collector with 70 mA sink capability
  - Receiver—65 μA input loading (BUS 0-3L)
- Internal 3-state bus drivers and receivers
  - Drivers—20 mA sink
  - Receivers—standard TTL (DAT 0-3 H)
- Address selection
  - Enable input for use with a higher level decoded input (MENB L)
  - Address bits may be excluded from comparison by tying them to VCC (JA(3:1)L)
- Interrupt Vector
  - Vector address bits "ORed" directly onto LSI-11 bus (JV(3:1)H)

SPECIFICATIONS

For complete Electrical Specifications refer to EJ 17475. A summary of the more important specifications follow the pin/signal descriptions for individual ICs.

DC003 Pin/Signal Descriptions

Pin	Signal	Description
1	VECTOR H	Interrupt Vector Gating. This signal should be used to gate the appropriate vector address onto the bus and to form the bus signal called BRPLY L. **Type:** TTL-OUTPUT
2	VECRQSTB H	Vector Request "B." When asserted, indicates RQST "B" service vector address is required. When unasserted, indicates RQST "A" service vector address is required. VECTOR H is the gating signal for the entire vector address; VECRQSTB H is normally bit 2 of the vector address. **Type:** TTL-OUTPUT

DC003 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
3	BDIN L	Bus Data In. This signal, generated by the processor BDIN, always precedes a BIAK signal. **Type:** BUS-INPUT
4	INITO L	Initialize Out. This is the buffered BINIT L signal used in the device interface for general initialization. **Type:** OPEN COLLECTOR WITH 1K PULL UP - OUTPUT
5	BINIT L	Bus Initialize. When asserted, this signal brings all driven lines to their unasserted state (except INITO L). **Type:** BUS-INPUT
6	BIAKO L	Bus Interrupt Acknowledge (Out). This signal is the daisy-chained signal that is passed by all devices not requesting interrupt service (see BIAKI L). Once passed by a device, it must remain passed until a new BIAKI L is generated. **Type:** BUS-OUTPUT
7	BIAKI L	Bus Interrupt Acknowledge (In). This signal is the processor's response to BIRQ L true. This signal is daisy-chained such that the first requesting device blocks the signal propagation while non-requesting devices pass the signal on as BIAKO L to the next device in the chain. The leading edge of BIAKI L causes BIRQ L to be unasserted by the requesting device. **Type:** BUS-INPUT
8	BIRQ L	Bus Interrupt Request. This signal is generated when this device needs to interrupt the processor. The request is generated by a false to true transition of the RQST signal along with the associated true interrupt enable signal. The request is removed after the acceptance of the BDIN L signal and on the leading edge of the BIAKI L signal or the removal of the associated request signal. **Type:** BUS-OUTPUT

DC003 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
10 17	RQSTB H RQSTA H	Device Interrupt Request. When asserted with the enable flip-flop set, will cause the assertion of BIRQ L on the bus. This signal line normally remains asserted until the request is serviced. **Type:** BUS-INPUT
11 16	ENBST H ENAST H	Interrupt Enable Status. This signal indicates the state of the interrupt enable internal flip-flop which is controlled by the signal ENX (where X is either A or B) DATA H, and the ENX (where X is either A or B) CLK H clock line. **Type:** TTL-OUTPUT
12 15	ENBDATA H ENADATA H	Interrupt Enable Data. The level on this line, in conjunction with the ENX (where X is either A or B) CLK H signal, determines the state of the internal interrupt enable flip-flop. The output of this flip-flop is monitored by the ENX (where X is either A or B) ST H signal.**Type:** TTL-INPUT
13 14	ENBCLK H ENACLK H	Interrupt Enable Clock. When asserted (on the positive edge), interrupt enable flip-flop assumes the state of the ENX (where X is either A or B) DATA H, signal line. **Type:** TTL-INPUT

Summary of Electrical Specifications for DC003

Ambient Temperatures	0°C to 70°C
TTL Input	
High-level input current	50 μA max. I_{IH}(V=2.7V)
Low-level input current I_{IL}(V_I=0.5V)	−.55 mA max.
Exceptions	Pins 12 & 15 ENX DATA H I_{IH} = 100 μA max. I_{IL} = −2.0 mA max.

TTL Outputs

High-level output voltage V_{OH} (I_O = −1 mA max.)	2.7V min.
Low-level output voltage V_{OL} (I_O = 20 mA max.)	0.5V max.

Bus (Hi Z) input and (open collector) outputs.

Bus Inputs

High-level input current I_{IH} (V_I = 3.8V)	40μA max.
Low-level input current I_{IL} (V_I = 0V)	−10μA max.

Bus Outputs

Low-level output voltage V_{LO} (I_{sink} = 70 mA max.)	0.8V max.

DC004 Pin/Signal Descriptions

Pin	Signal	Description
1	VECTOR H	Vector. This input causes BRPLY L to be generated through the delay circuit. Independent of BSYNC L and ENB H. **Type:** TTL-INPUT
2 3 4	BDAL2 L BDAL1 L BDAL0 L	Bus Data Address Lines. These signals are latched at the assert edge of BSYNC L. Lines 2 and 1 are decoded for the select outputs; line 0 is used for byte selection. **Type:** BUS-INPUTS
5	BWTBT L	Bus Write/Byte. While the BDOUT L input is asserted, this signal indicates a byte or word operation: asserted = byte, unasserted = word. Decoded with BDOUT L and latched BDAL0 L to form OUTLB L and OUTHB L. **Type:** BUS-INPUT

DCK11-AA, -AC

DC004 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
6	BSYNC L	Bus Synchronize. At the assert edge of this signal, address information is trapped in four latches. While unasserted, disables all outputs except the vector term of BRPLY L. **Type:** BUS-INPUT
7	BDIN L	Bus Data In. This is a strobing signal to effect a data input transaction. Generates INWD L and BRPLY L through the delay circuit and INWD L. **Type:** BUS-INPUT
8	BRPLY L	Bus Reply. This signal is generated through an RC delay by VECTOR H, or BDIN L, or BDOUT L and the AND of BSYNC L and latched ENB H. **Type:** BUS-OUTPUT
9	BDOUT L	Bus Data Out. This is a strobing signal to effect a data output transaction. Decoded with BWTBT L and BDAL0 to form OUTLB L and OUTHB L. Generates BRPLY L through the delay circuit. **Type:** BUS-INPUT
11	INWD L	In Word. Used to gate (read) data from a selected register onto the data bus. Enabled by BSYNC L and strobed by BDIN L. **Type:** TTL-OUTPUT
12 13	OUTLB L OUTHB L	Out Low Byte. Out High Byte. Used to load (write) data into the lower, higher, or both bytes of a selected register. Enabled by BSYNC L and decode of BWTBT L and latched BDAL0 L, and strobed by BDOUT L. **Type:** TTL-OUTPUT
14 15 16 17	SEL0 L SEL2 L SEL4 L SEL6 L	Select Lines. One of these four signals is true as a function of BDAL2 L and BDAL1 L if ENB H is asserted at the asserted edge of BSYNC L. They indicate that a word register has been selected for a data transaction. These signals never become asserted except at the assertion of BSYNC L (then only

DC004 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
		if ENB H is asserted at that time) and once asserted, are not unasserted until BSYNC L becomes unasserted. **Type:** TTL-OUTPUT
18	RXCX H	External Resistor Capacitor Node. This node is provided to vary the delay between the BDIN L, BDOUT L, or VECTOR H inputs and BRPLY L output. The external resistor should be tied to V_{CC} and the capacitor to ground. As an output, it is the logical inversion of BRPLY L. **Type:** OPEN-COLLECTOR OUTPUT
19	ENB H	Enable. This signal is latched at the asserted edge of BSYNC L and is used to enable the select outputs and the address term of BRPLY L. **Type:** TTL-INPUT WITH 850Ω PULL UP

Summary of Electrical Specifications for DC004

Ambient Temperatures	0°C to 70°C
TTL Inputs	
High level input current I_{IH} (V_I = 2.7V)	50 μA max.
Low level input current I_{IL} (V_I = 0.5V)	−.70 mA max.
Exceptions	Pin 19 ENB H I_{IH} = −3.85 mA max. I_{IL} = −8.0 mA max.
TTL Outputs	
High Level output voltage V_{OH} (I_O = −1 mA)	2.7V min.
Low level output voltage V_{OL} (I_O = 20 mA)	0.5V max.
Bus (Hi- Z) Inputs and (Open Collector) Outputs	
Bus inputs	

High level input current I_{IH} (V_I = 3.8V)	40 μA max.
Low level input current I_{IL} (V_I = 0V)	−10 μA max.
Bus Outputs Low level output voltage V_{LO} (I_{sink} = 70 mA)	0.8V max.

DC005 Pin/Signal Descriptions

Pin	Signal	Description
	BUS(3:0) L	
12	BUS0 L	Bus Data. This set of four lines constitutes
11	BUS1 L	the bus side of the transceiver. Open collec-
9	BUS2 L	tor outputs; high-impedance inputs. Low=
8	BUS3 L	1. **Type:** BUS-INPUT/OUTPUT
	DAT(3:0) H	
18	DAT0 H	Peripheral Device Data. These four tri-state
17	DAT1 H	lines carry the inverted received data from
7	DAT2 H	BUS (3:0) when the transceiver is in the re-
6	DAT3 H	ceive mode. When in transmit data mode, the data carried on these lines are passed inverted to BUS (3:0). When in the disabled mode, these lines go open (HI-Z). High = 1. **Type:** TTL-INPUTS
	JV(3:1) H	Vector Jumpers. These inputs, with internal
14	JV1 H	pull-down resistors, directly drive BUS
15	JV2 H	(3:1). A low or open on the jumper pin will
16	JV3 H	cause an open condition on the corres- ponding bus pin if XMIT H is low. A high will cause a one (low) to be transmitted on the bus pin. Note that BUS0 L is not controlled by any jumper input. **TYPE:** TTL-INPUT WITH PULL DOWN
13	MENB L	Match Enable. A low on this line will enable the Match output. A high will force MATCH low, overriding the MATCH circuit. **TYPE:** BUS-INPUT

DC005 Pin/Signal Descriptions (Cont)

Pin	Signal	Descriptions
3	MATCH H	Address Match. When BUS (3:1) match with the state of JA (3:1) and MENB L is low, this output is open; otherwise it is low. **TYPE:** BUS-OUTPUT
	JA(3:1) L	Address Jumpers. A strap to ground on these inputs will allow a match to occur with a 1 (low) on the corresponding BUS line; an open will allow a match with a 0 (high); a strap to V_{CC} will disconnect the corresponding address bit from the comparison. **TYPE:** TERNARY-INPUT (SEE TEXT)
1	JA1 L	
2	JA2 L	
19	JA3 L	
5	XMIT H	Control Inputs. These lines control the operation of the transceiver as follows:
4	REC H	

REC	XMIT	
0	0	DISABLE:BUS,DAT open
0	1	XMIT DATA:DAT→BUS
1	0	RECEIVE:BUS→DAT
1	1	RECEIVE:BUS→DAT

To avoid 3-state signal overlap conditions, an internal circuit delays the change of modes between XMIT DATA and RECEIVE mode and delays 3-state drivers on the DAT lines from enabling. This action is independent of the DISABLE mode.

Summary of Electrical Specifications for DC005

Ambient Temperatures	0°C to 70°C
TTL Inputs	
High level input current I_{IH} (V_I = 2.7V)	—
REC H Pin 4	100 μA max.
XMIT H Pin 5	50 μA max.
Low level input current I_{IL} (V_I = 0.5V)	—

REC H Pin 4	−2.2 mA max.
XMIT H Pin 5	−1.1 mA max.

TTL Outputs

High Level output voltage V_{OH} (I_O = −1 MA)	3.65V min.
Low level output voltage V_{OL} (I_O = 20 mA)	0.5V max.

Bus (Hi-Z) Inputs and (Open Collector) Outputs

Bus inputs	
High level input current I_{IH} (V_I = 3.8V)	65 μA max.
Low level input current I_{IL} (V_I = 0.5V)	−10 μA max.
Bus Outputs	
Low level output voltage V_{LO} (I_{sink} = 70 mA)	0.8V max.

DESCRIPTION

PROGRAM CONTROL CHIPKIT APPLICATION

In Figure 1, the transceivers (four DC005s) provide data lines D0 through D15 to reflect the state of the bus lines BDAL 0-15, when REC H is asserted, and to drive the BDAL lines when XMIT is asserted. Address and interrupt vector information for interrupt request and device selection is also provided by the DC005. The device address is set up using input lines A3 through A12, while the interrupt vector address is set up using input lines V3 through V8.

When the address lines (JA inputs on DC005s) match the state of the associated BDAL lines, the MATCH output will float high such that all DC005s will let ENB H on the DC004 be asserted, thus enabling the DC004 to look for proper synchronizing signals from the bus. Once these synchronizing signals (BDIN, BDOUT, BSYNC, and BWTBT) are present, the DC004 generates the control signals (INWD, OUTHB, OUTLB, and SEL 0, 2, 4, 6) for the user's device.

The protocol logic (DC004) functions as a register selector to provide

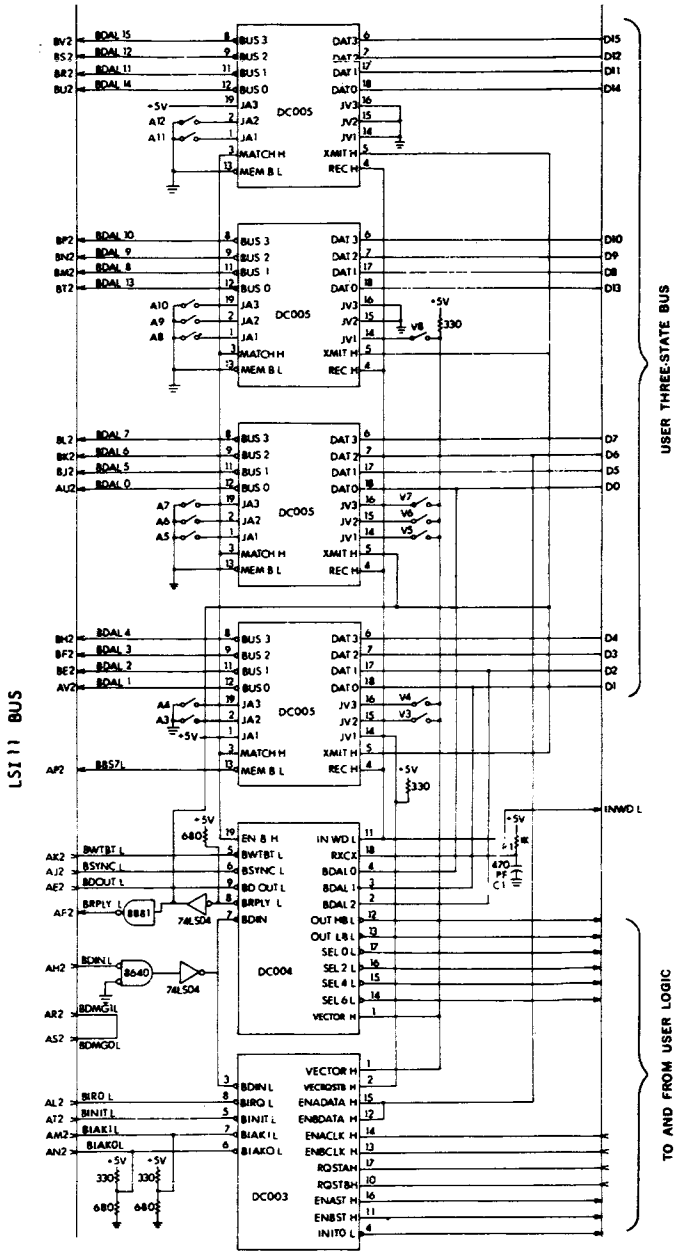
the signals necessary to control data flow into and out of the user's registers. When the proper device address has been decoded by the device address comparator (all DC005s), the MATCH outputs let the ENBH input go high, thus enabling the DC004 protocol logic. Address bits D01 H and D02 H are decoded by the protocol logic, producing one of the SEL outputs, while bit D0 and BWTBT are decoded for output word/byte selection (OUTHB L, OUTLB L). The device select line (SEL 0, 2, 4, 6) and word/byte select lines (INWD L, OUTHB L, OUTLB L) are used by the user's logic. Each SEL output is used to select one of four user's registers, and the word/byte lines are used to determine the type of transfer (word or byte) to or from these registers.

Either BDIN L or BDOUT L, depending on the type of bus cycle, will initiate a delay whose value is dependent on the time constant of the RC network connected to pin RXCX H of the DC004. The end of this delay will initiate a reply to the CPU indicating that the address has been received.

The interrupt logic (DC003) performs an interrupt transaction. Two channels (A and B) are provided for generating two interrupt requests, with channel A having the highest priority. The interrupt enable flip-flop within the interrupt logic must first be set when the user's device is to interrupt the LSI-11. This is accomplished by asserting (logic H) the ENX DATA* line and then clocking the enabled flip-flop by asserting the ENX CLK* line. With the interrupt enable flip-flop set, the user's device may then make an interrupt request by asserting (logic H) RQSTX*. When RQST is asserted and the interrupt enable flip-flop is set, the interrupt logic asserts BIRQ L to the bus which initiates the bus "handshake" operation. This operation terminates with the generation of the vector address by the DC005 under the control of the DC003, and it's signals VECTOR H and VECRQSTB H.

The interrupt logic available to the user indicates the status of the interrupt logic enable flip-flops. Each line is asserted (logic H) when the appropriate interrupt enable flip-flop is set. These status lines can function as part of the user's control status register (CSR). The VECRQSTB H line is asserted (logic H) when the device connected to channel B has been granted use of the bus for interrupt vector transfer operation. When VECRQSTB H is unasserted (logic L), the user's device connected to channel A of the interrupt logic has been granted use of the bus. The INITO L output from the interrupt logic can be used to initialize the user's logic.

* X may be either A or B depending on which half of the interrupt logic is being enabled.



NOTE:

CLOSE SWITCH FOR ONE
OPEN SWITCH FOR ZERO

Figure 1 DCK11 Bus Interface Typical Application

DC003 Interrupt Logic

The interrupt chip is an 18-pin, 0.762 cm center × 2.349 cm long (max) (0.3 in center × 0.925 in long) dual-in-line-package (DIP) device that provides the circuits to perform an interrupt transaction in a computer system that uses a daisy-chain type of arbitration scheme. The device is used in peripheral interfaces to provide two interrupt channels labeled "A" and "B," with the A section at a higher priority than the B section. Bus signals use high-impedance input circuits or high-current open collector outputs, which allow the device to directly attach to the computer system bus. Maximum current required from the V_{CC} supply is 140 mA.

Figure 2 is a simplified logic diagram of the DC003 IC.

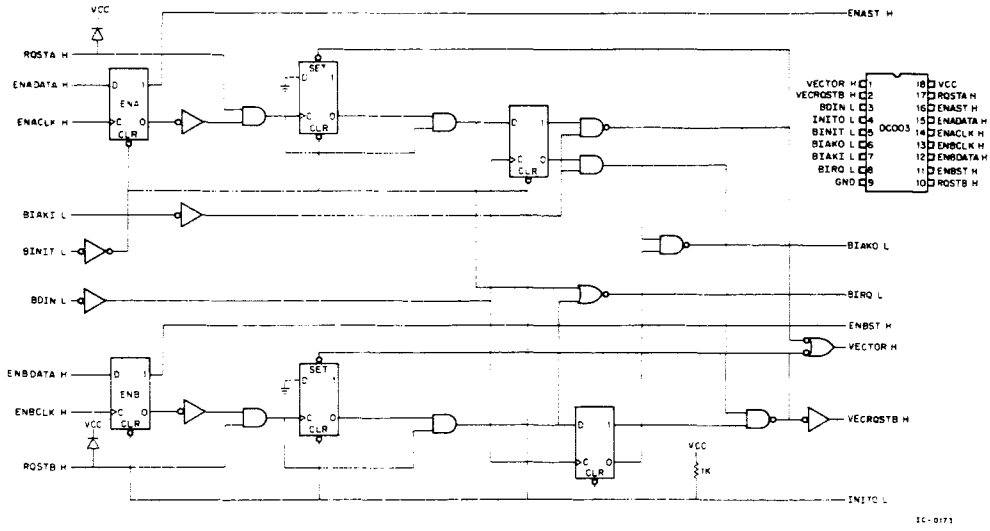


Figure 2 DC003 Simplified Logic Diagram

DC004 Protocol Logic

The protocol chip is in a 20-pin 0.762 cm center × 2.74 cm long (0.3 in. center × 1.08 in. long) DIP device that functions as a register selector, providing the signals to control the data flow into and out of up to four word registers (eight bytes). Bus signals can directly attach to the device because receivers and drivers are provided on the chip. However, the DC004 is now ordinarily used with the user's three-state bus to limit Bus loading. An RC delay circuit is provided to slow the response of the peripheral interface to data transfer requests. The circuit is designed such that if tight tolerance is not required, then only an external 1K ±20 percent resistor is necessary. External RCs can be added to vary the delay. Maximum current required from the V_{CC} supply is 120 mA.

Figure 3 is a simplified logic diagram of the DC004 IC.

NOTE

The pin names shown in this diagram are for the situation where the DC004 is connected to the internal 3-state bus of the DC005s, not connected directly to the LSI-11 bus.

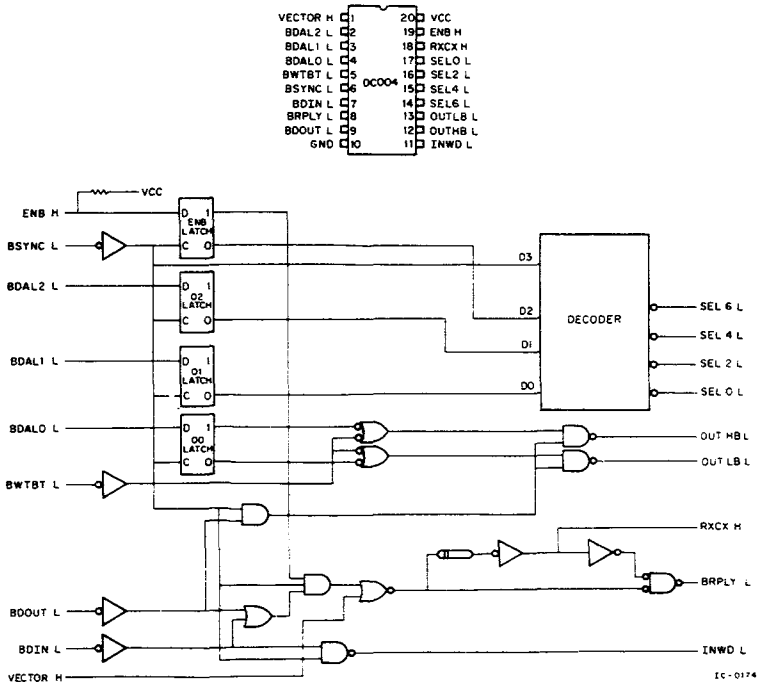


Figure 3 DC004 Simplified Logic Diagram

DC005 Transceiver Logic

The 4-bit transceiver is a 20-pin, 0.762 cm center × 2.74 cm long (0.3 in. center × 1.08 in. long) DIP, low-power Schottky device; its primary use is in peripheral device interfaces to function as a bidirectional buffer between a data bus and peripheral device logic bus. It also includes a comparison circuit for device address selection and a constant generator for interrupt vector address generation. The bus I/O port provides high-impedance inputs and high drive (70 mA) open collector outputs to allow direct connection to a computer data bus structure. On the peripheral device side, a bidirectional port is also provided, with standard TTL inputs and 20 mA, tri-state drivers. Data on this port are the logical inversion of the data on the bus side.

Three address "jumper" inputs are used to compare against three bus inputs to generate the signal MATCH. The MATCH output is open collector, which allows the output of several transceivers to be wire-ANDed to form a composite address match signal. The address jumpers can also be put into a third logical state that disables jumpers for "don't care" address bits. In addition to the three address jumper inputs, a fourth high-impedance input line is used to enable/disable the MATCH output.

Three vector jumper inputs are used to generate a constant that can be passed to the computer bus. The three inputs directly drive three of the bus lines, overriding the action of the control lines.

Two control signals are decoded to give three optional states: receive data, transmit data, and disable.

Maximum current required from the V_{CC} supply is 120 mA.

Figure 4 is a simplified logic diagram of the DC005 IC.

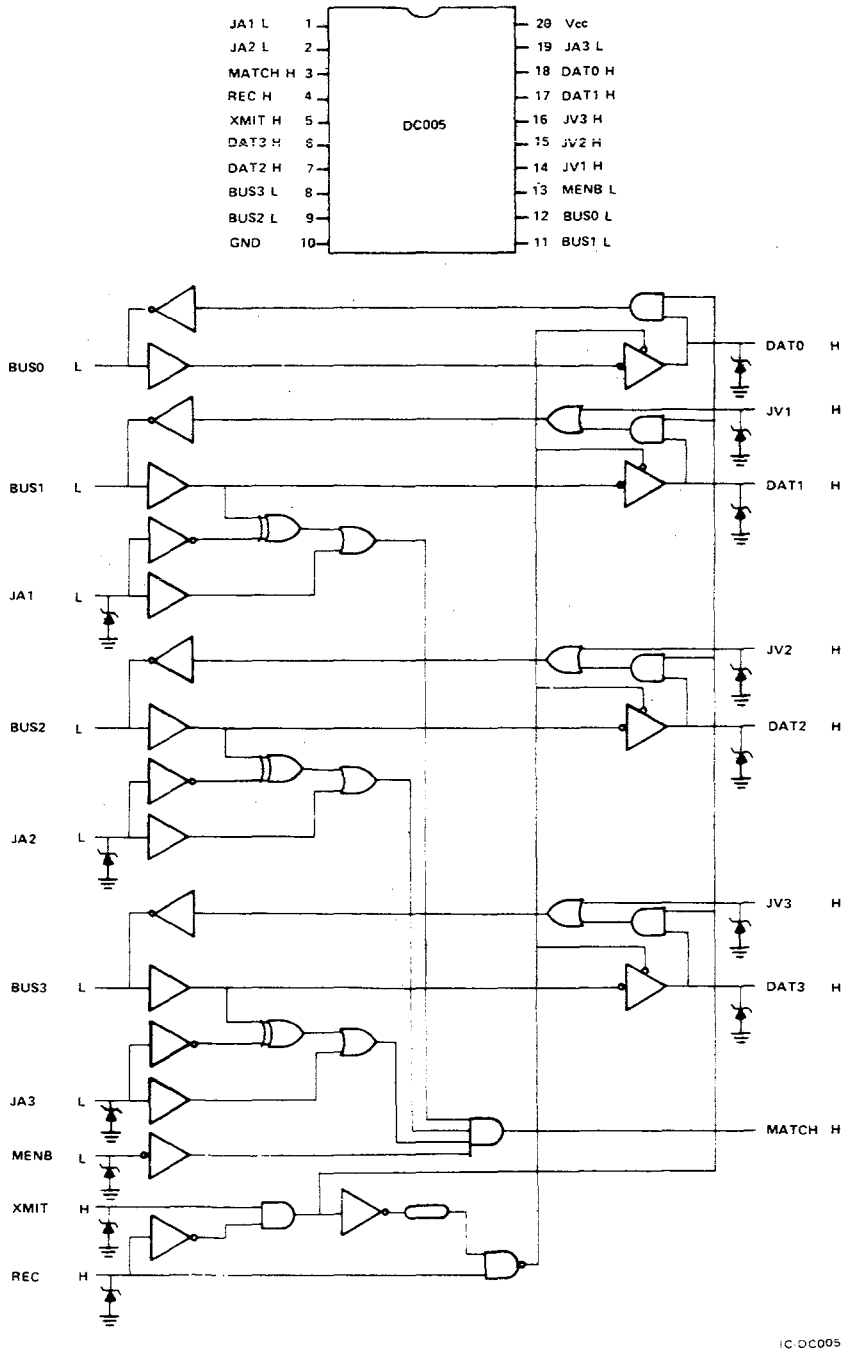


Figure 4 DC005 Simplified Logic Diagram

CONFIGURATION

The drawings on the following pages show sample circuits that may be helpful in applying the CHIPKITS.

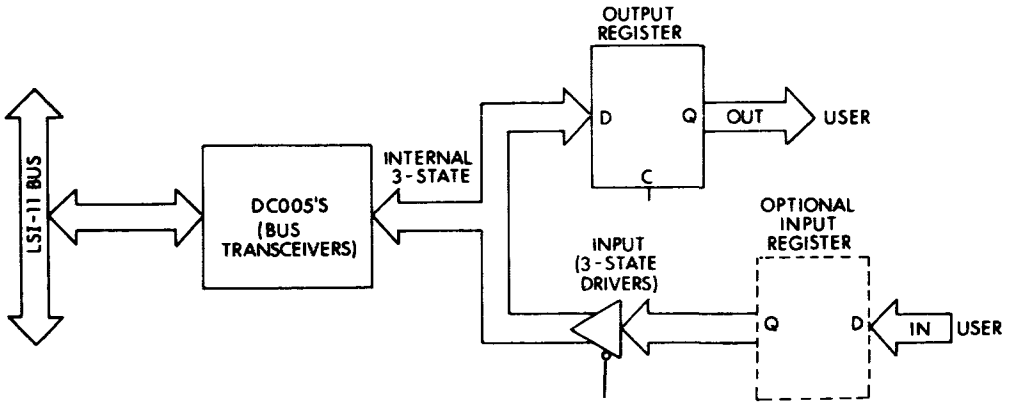


Figure 5 Data Path Flow Diagram

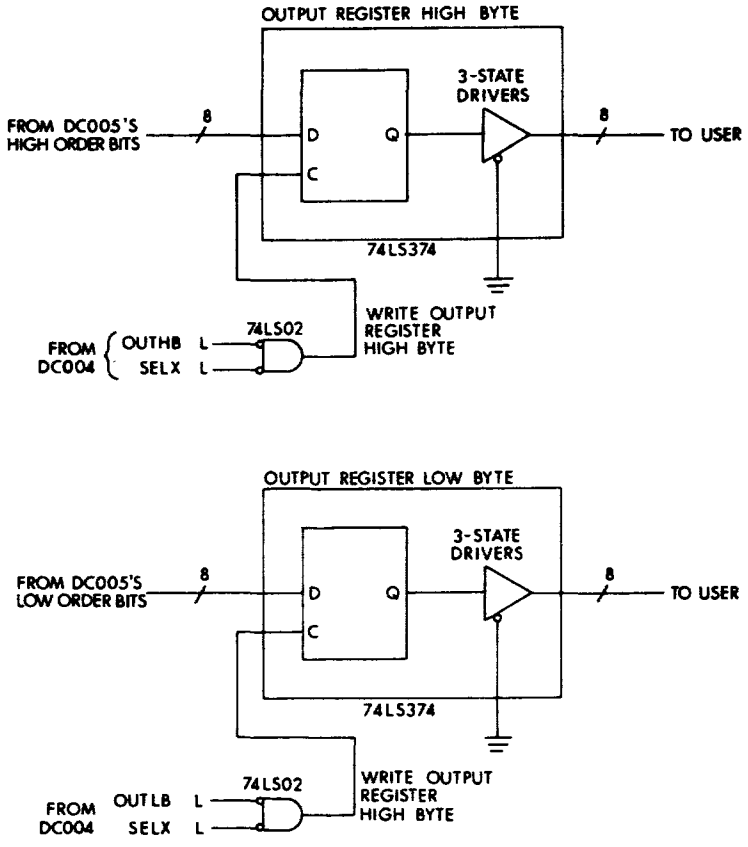


Figure 6 Example of Output Register

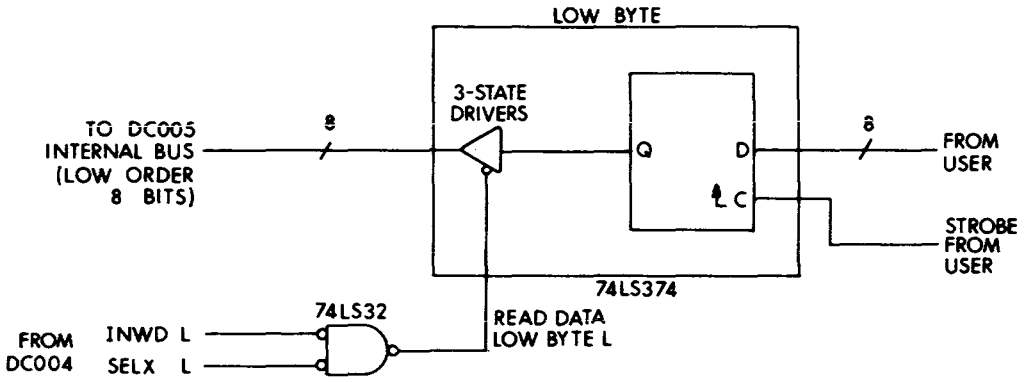


Figure 7 Example of Input Register (BYTE)

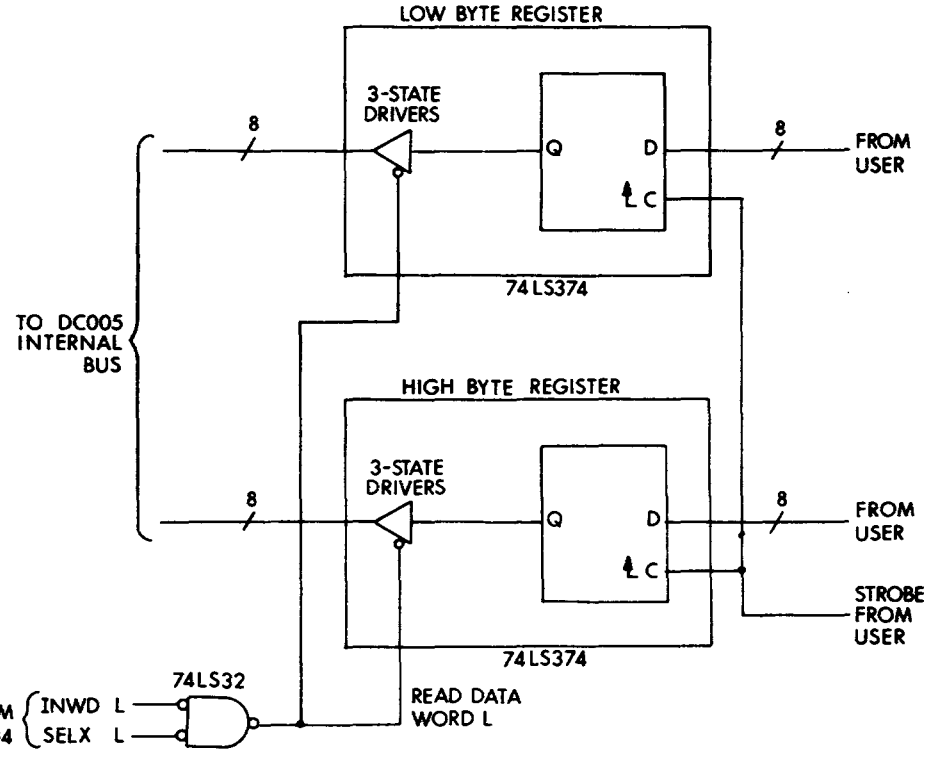


Figure 8 Example of Input Register (WORD)

This example is the interrupt enable bit for interrupt A which connects to bit 6 of the example CSR.

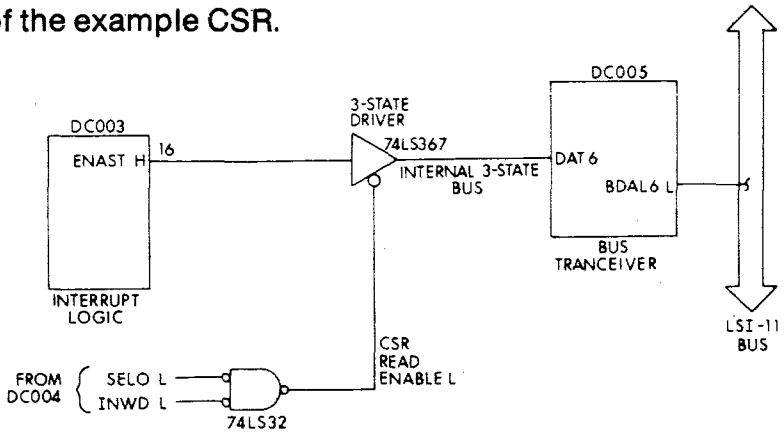
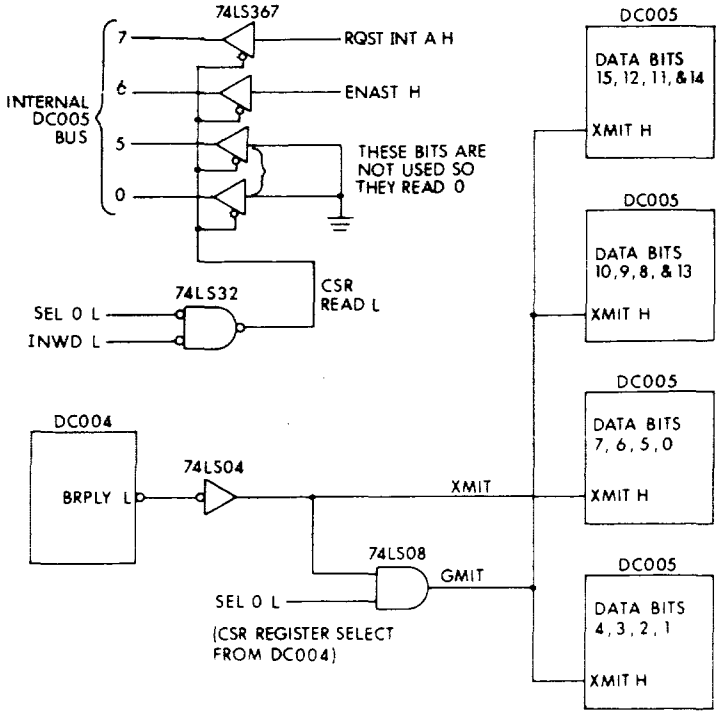


Figure 9 Typical CSR Bit



WHEN THE CSR IS READ (SEL 0 L = 0) THE SIGNAL GMIT WILL BE 0 CAUSING THE UNUSED DC005 BITS TO BE READ AS ZEROS. (HIGH ON BDAL LINES) FOR ANY OTHER REGISTER GMIT = XMIT.

Figure 10 Sample Circuit to Cause Unused CSR Bits to be Read as Zeros

This example is the A interrupt request and a DATA READY status bit (bit 7 of the CSR).

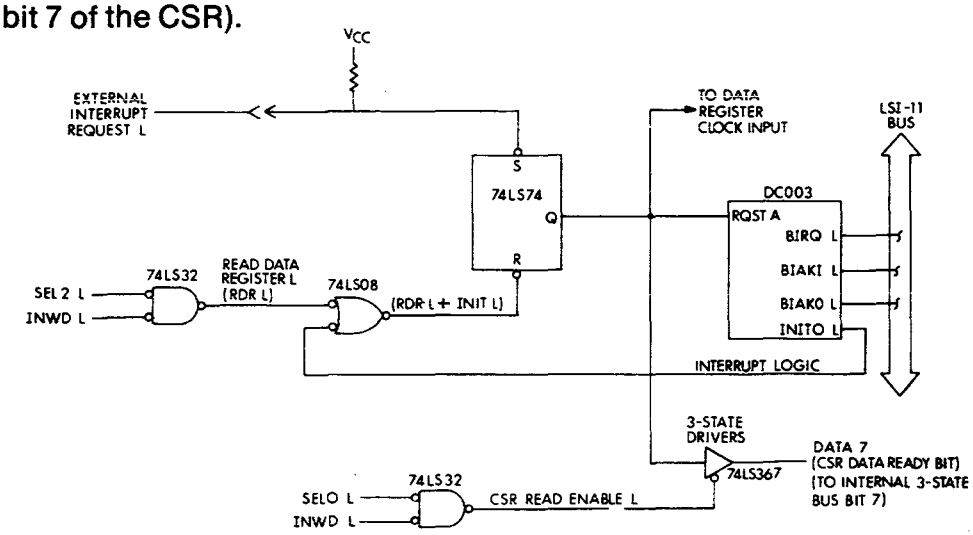


Figure 11 Typical Interrupt Request

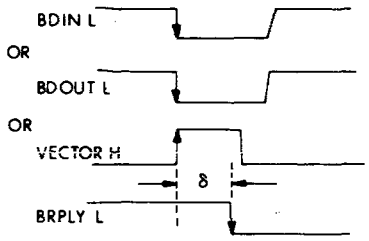
BUS REPLY DELAY TIMES

Bus Reply delays as a function of RC values connected to pin 18 (RXCX H) of the DC004.

k1. RX = 1KΩ 5%
CX = 0
Delay ~ 50 ns from falling edge of BDIN L, or BDOUT L, or rising edge of VECTOR H to BRPLY L falling edge.

2. RX = 1KΩ 5%
CX = 470 pf 5%
Delay as described in item 1 above ~ 200 ns.

3. RX = 10KΩ 5%
CX = 1000 pf 5%
Delay as described above ~ 3.2 μsec



WHERE δ = DELAY DESCRIBED IN ITEMS 1-3

Figure 12

DCK11-AB, -AD DIRECT MEMORY ACCESS INTERFACE

INTRODUCTION

The DCK11-AB and -AD CHIPKITs provide the logic necessary for a Direct Memory Access (DMA) interface to the LSI-11 bus.

The DCK11-AB kit contains:

1-DC003 Interrupt Chip
1-DC004 Protocol Chip
4-DC005 Transceiver/Address Decoder/Vector Select Chips
2-DC006 Word Count/Bus Address Chips
1-DC010 DMA Control Chip

The DCK11-AD kit contains the above chips plus:
1-W9512 double-height, extended-length, high-density wire-wrappable module
1-BC07D-10 ten-foot, 40-conductor plug-in cable

Figure 1 shows a typical interconnection of DMA CHIPKIT components, in block diagram form.

DMA applications use the same chips as program control interfaces, plus two DC006s for word or byte address counters and a DC010 DMA bus control IC.

DC006 Word and Address Counter IC Features

- Two 8-bit counters on each IC
- 16-bit address and word counters available in two ICs cascaded
- Input and output share pins on the 3-state bus
- Read and write control logic located on the IC
- Maximum count decoded and brought out for user

DC010 DMA Logic Features

- Uses an external 8 MHz clock to generate LSI-11 bus signals for DIN, DOUT, SYNC, and SACK
- Inputs allow selection of cycle type (DATI, DATO, DATIO)
- Interfaces with DMA daisy-chain signals
- Allows an external RC network to force a variable wait before the next bus request is made (TMOUT H)
- An input which allows a maximum of four transfers before the bus is released, when enabled (CNT4 H)

DCK11-AB, -AD

SPECIFICATIONS

This section contains a summary of the most important specifications for DC006 and DC010. See the previous section DCK11-AA, -AC for a summary of specifications for DC003, DC004, and DC005.

DC006 Pin/Signal Descriptions

Pin	Signal	Description
6	CNT1A	Count A Counter by 1 (TTL Input). This signal controls the least significant bit of the A counter. When CNT1A is low, the A counter increments by one. When high, the LSB is prevented from toggling, hence the counter increments by two. When two counters are cascaded, CNT1A on the high-order counter should be grounded.
3	CLK-A	Clock A Counter (TTL Input). This clock signal increments the A counter on its negative edge. The counter is incremented by one or two, depending on CNT1A. CNT1A and LD must be stable while CLK-A is high.
16	CLK-C	Clock C Counter (TTL Input). This clock signal increments the C counter by one on its negative edge. LD must be stable while CLK-C is high.
2	S-A	Select A Counter (TTL Input). This signal allows the selection of the A counter according to the truth tables.

DC006 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
19	S-C	Select C Counter (TTL Input). This signal allows the selection of the A counter according to the truth tables.
4	RD-A	Read A Counter (TTLInput). This signal allows the selection of the A counter according to the truth tables.
5	RD-	Read (TTL Input). This signal allows the read operation to take place according to the truth tables.
18	LD	Load (TTL Input). When this signal goes through a high-to-low transition, the load operation is allowed to take place according to the truth tables. No data changes permitted while LD is low.
7-9 11-15	D/F (7:0)	Data Bus (Bidirectional, 3-State Outputs/TTL Inputs). These eight bidirectional lines are used to carry data in and out of the selected counter.
1	MAX-A	Maximum A Count(TTL Output). This signal is generated by ANDing CLK-A and the maximum count condition of counter A (count 376 when counting by 2 or count 377 when counting by 1).
17	MAX-C	Maximum C Count (TTL Output). This signal is generated by ANDing CLK-C and the maximum count conditions of counter C (count 377).

Summary of Electrical Specifications for DC006

Ambient Temperatures	0° to 70°
TTL Inputs	
High level input current I_{IH} (V_I = 2.7V)	55 μA max.
Low level input current I_{IL} (V_I = 0.5V)	−1.7 mA max.
TTL Outputs	
High level output voltage V_{OH} (I_O = −1 mA)	2.7V min.
Low level output voltage V_{OL} (I_O = 20 mA)	0.5V max.

DC010 Pin/Signal Descriptions

Pin	Signal	Description
1	REQ H	Request (TTL Input). A high on this signal initiates the bus request transaction. A low allows the termination of bus mastership to take place.
13	BDMGI L	DMA Grant Input (Hi-Z Input). A low on this signal allows bus mastership to be established if a bus request was pending (REQ = high); otherwise, this signal is delayed and output as BDMGO L.
16	CNT4 H	Count Four Input (TTL Input). A high on this signal allows a maximum of four transfers to take place before giving up bus mastership. A low disables this feature and an unlimited transfer will take place as long as REQ is high. If left open, this pin will assume a high state.

DC010 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
14	TMOUT H	Time-Out (TTL Input/Open Collector Output). This I/O pin is low while MASTER ENA is high. It goes into high impedence when MASTER ENA is low. When driven low it prevents the assertion of BDMR; when driven high it allows the assertion of BDMR to take place if BDMR has been negated due to the 4-maximum transfer condition. An RC network may be used on this pin to delay the assertion of BDMR.
3	DATIN L	Data In (TTL Input). This signal allows the selection of the type of transfers to take place according to the truth table.
2	DATIO L	Data IN/Out (TTL Input). This signal allows the selection of the type of transfer to take place according to the truth table. During a DATIO transfer, this signal must be toggled in order to allow the completion of the output portion of the I/O transfer. If left open, this pin will assume a high state.
12	RSYNC H	Receive Synchronize (TTL Input). This signal allows the device to become master according to the following relationship:

DC010 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
		RSYNC L · RPLY H· MASTER ENA = MASTER
17	CLK L	Clock (TTL Input). This clock signal used to generate all transfer timing sequences.
15	RPLY H	Reply (TTL Input). This signal is used to enable or disable the clock signal. This signal also allows the device to become master according to the following relationship: RSYNC L · RPLY H · MASTER ENA = MASTER
19	INIT L	Initialize (TTL Input). This signal is used to initialize the chip to the state where REQ is needed to start a bus reqest transaction. When INIT is low, the following signals are negated: BDMR L, MASTER H, DATEN L, ADREN H, SYNC H, DIN H, DOUT H.
11	BDMR L	DMA Request (Open Collector Output). A low on this signal indicates that the device is requesting bus mastership. This output may be tied directly to the bus.
9	MASTER H	Master (TTL Output). A high on this signal indicates that the device has bus mastership and a transfer sequence is in progress.

DC010 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
8	BDMGO L	DMA Grant Output (Open Collector Output). This signal is the delayed version of BDMGI if no request is pending; otherwise, it is not asserted. This output may be tied directly to the bus.
7	TSYNC H	Transmit Synchronize (TTL Output). This signal is asserted by the device to indicate that a transfer is in progress.
18	DATEN L	Data Enable (TTL Output). This signal is asserted to indicate that data may be placed on the bus.
4	ADREN H	Address Enable (TTL Output). This signal is asserted to indicate that an address may be placed on the bus.
6	DIN H	Data In (TTL Output). This signal is asserted to indicate that the bus master device is ready to accept data.
5	DOUT H	Data Out (TTL Output). This signal is asserted to indicate that the bus master device has output valid data.

Summary of Electrical Specifications for DC010

Ambient Temperatures 0°C to 70°C

TTL Inputs

High level input current I_{IH} (V_I = 2.7V) 300 μA max.

Low level input current I_{IL} (V_I = 0.5V)	−2.0 mA max.

TTL Outputs

High Level output voltage V_{OH} (I_O = −1 mA)	2.7V min.
Low level output voltage V_{OL} (I_O = 8 mA)	0.5V max.

Bus (Hi - Z) Inputs and (Open Collector) Outputs

Bus inputs

High level input current I_{IH} (V_I = 3.8V)	65 μA max.
Low level input current I_{IL} (V_I = 0.5V)	−10 μA max.

Bus Outputs

Low level output voltage V_{LO} (I_{sink} = 70 mA)	0.8V max.

DESCRIPTION

DMA CHIPKIT Application

Figure 1 shows how four DC005 transceivers are used to handle the first 16 BDAL lines (BDAL 0-BDAL 15) from the LSI-11 bus and to provide the interface to the internal 3-state bus. The transceivers are enabled to receive data from the LSI-11 bus when the REC H line is driven high. Similarly, the transceivers transmit data to the LSI-11 bus when the XMIT H line is driven high. Normally, the DC005s are in the receive state (REC H line asserted) and allow the transceivers to monitor the LSI-11 bus for device addresses.

Device address and vector switch inputs to the transceivers provide convenient address and vector selection.

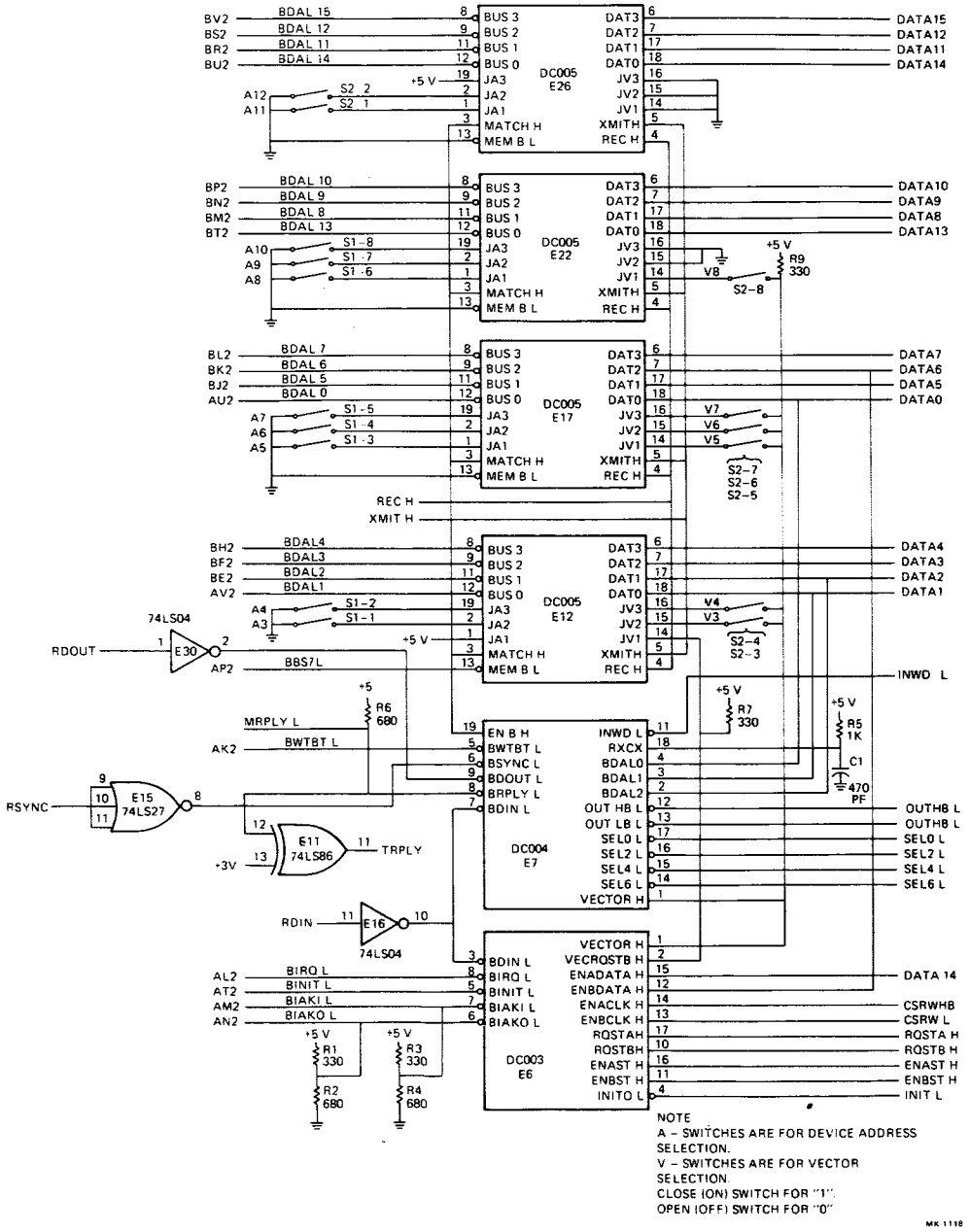


Figure 1 Typical DMA CHIPKIT Application

Switches A3 through A12 are the device address selection switches and switches V3 through V8 are for vector selection. Switches are ON

(closed) for a 1 bit and are OFF (open) for a 0 bit. The addressable registers are:

Register	Bank 7 Octal Address
Bus Address Register	1XXXX0
Word Count Register	1XXXX2
Control/Status Register	1XXXX4
Output Buffers	1XXXX6

The user selects a base address for the bus address register and sets the device address selection switches to decode this address. The remaining register addresses are then properly decoded as sequential addresses beyond the bus address register (Figures 2 and 3).

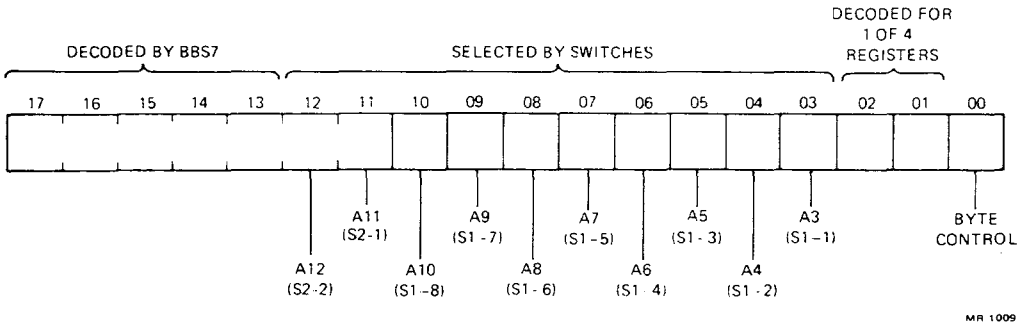


Figure 2 Device Address Select Format

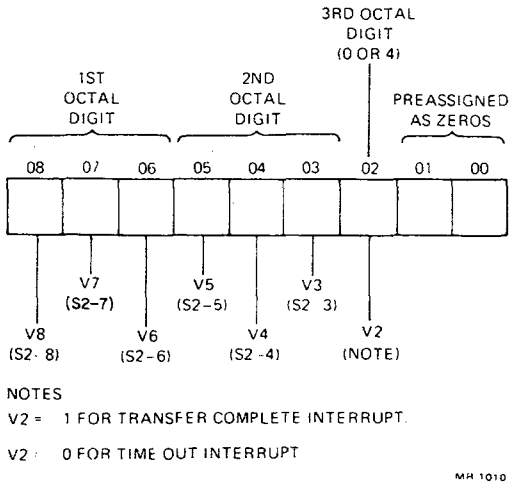


Figure 3 Interrupt Vector Select Format

The DC004 is the internal register selector. This integrated circuit monitors BDAL lines 0, 1, and 2 to determine which register address has been placed on the LSI-11 bus. The states of BDOUT and BDIN are also monitored to determine the type of transfer (DATO or DATI). When an address for an internal register is placed on the LSI-11 bus, one of the SEL outputs from the DC004 is driven low. This selects that particular register for the transfer (into or out of the master device) is determined by the state of the OUTHB L, OUTLB L, or INWD L lines. Internal register selection is summarized as follows:

Control Line	Select	Register
INWD L (Read)	SEL 0 L	Bus Address Register
INWD L (Read)	SEL 2 L	Word Count Register
OUTHB L (Write High Byte)	SEL 0 L	Bus Address Register
OUTHB L (Write High Byte)	SEL 2 L	Word Count Register
OUTLB L (Write Low Byte)	SEL 0 L	Bus Address Register
OUTLB L (Write Low Byte)	SEL 2 L	Word Count Register
INWD L (Read)	SEL 4 L	Control/Status Register
OUTHB L and MRPLY L (Write CSR High Byte)	SEL 4 L	Control/Status Register
OUTLB L and MRPLY L (Write CSR Low Byte)	SEL 4 L	Control/Status Register
OUTHB L and MRPLY L (Write High Byte)	SEL 6 L	Output Buffer
OUTLB L and MRPLY L (Write Low Byte)	SEL 6 L	Output Buffer

Note that MRPLY L is the BRPLY L output of the DC004 and is used along with OUTHB L and OUTLB L to write either the high or low byte in the control/status register or the output buffers. Write byte selection for the bus address register and the word count register is controlled only by the OUTHB L and OUTLB L lines. Words can be written to the control/status register or the output buffer registers by driving both OUTHB L and OUTLB L to the low state at the same time.

The DC004 integrated circuit was designed to operate directly from the LSI-11 bus. However, since the introduction of the DC005, the DC004 is usually interfaced to the LSI-11 bus through the DC005. Bus signals (BDAL lines) passing through the DC005 are inverted. Therefore, BDAL 0, 1, and 2 signals applied to the DC004 are inverted. Because of this inversion, it is necessary to change the nomenclature

on pins 12 through 17 on the DC004. The difference in nomenclature between DC004s operated directly from the LSI-11 bus and through a DC005 are as follows:

From Bus (Non-Inverted BDAL 0,1,2)		From DC005 (Inverted BDAL 0,1,2)	
Pin	**Signal**	**Pin**	**Signal**
12	OUTLB L	12	OUTHB L
13	OUTHB L	13	OUTLB L
14	SEL 0 L	14	SEL 6 L
15	SEL 2 L	15	SEL 4 L
16	SEL 4 L	16	SEL 2 L
17	SEL 6 L	17	SEL 0 L

It is recommended that when a DC005 is used, the DC004 be interfaced to the LSI-11 bus through the DC005 to avoid unnecessary bus loading.

The DC003 IC performs an interrupt transaction that uses the daisy-chain type arbitration scheme to assign priorities to peripheral devices. The DC003 has two channels (A and B) for generating two interrupt requests. Channel A has higher priority than channel B. If a user's device wants control of the LSI-11 bus, the interrupt enable flip-flop within the DC003 must be set. This is accomplished by asserting (logic 1) the ENX* DATA line to the DC003 (writing bit 14 or bit 6 to a one) and then clocking the enable flip-flop by asserting (logic 1) RQST. RQST must be held asserted until the interrupt is serviced. When the RQST is asserted and the interrupt enable flip-flop is set, the DC003 asserts (logic 0) BIRQ L, thus making a bus request. When the request is granted, the processor asserts (logic 0) BDIN L. This causes the DC003 to assert (logic 1) VECTOR H, which is applied to the DC005. VECTOR H at the DC005 causes the device vector to be placed on the BDAL lines to the processor. Interrupts are produced for bus time-outs (CSR bits 15 and 14) and at the completion of a block transfer (CSR bits 7 and 6).

* X may be either A or B.

DMA Application

Figure 4 shows the DMA control (DC010), the word count/bus address registers (both DC006), the output buffers (both 74LS273s), and the input drivers (74LS367s).

The DC010 performs handshaking operations required to request and gain control of the LSI-11 bus for DMA data transfers. After becoming bus master, the DC010 produces the signals necessary to perform a DIN or DOUT bus cycle as specified by the control lines. An 8-MHz free-running clock is provided by E21. This clock is used by the DC010 to generate all transfer timing sequences. The actual clock frequency is not critical and can be any frequency up to 8.3 MHz, provided it is symmetrical. An RC time constant provided by resistor R14 and capacitor C2 provides a delay for the reassertion of BDMR to the LSI-11 bus. This allows other direct memory access devices to obtain the bus during the time the CNT4 logic releases the bus and re-requests the bus.

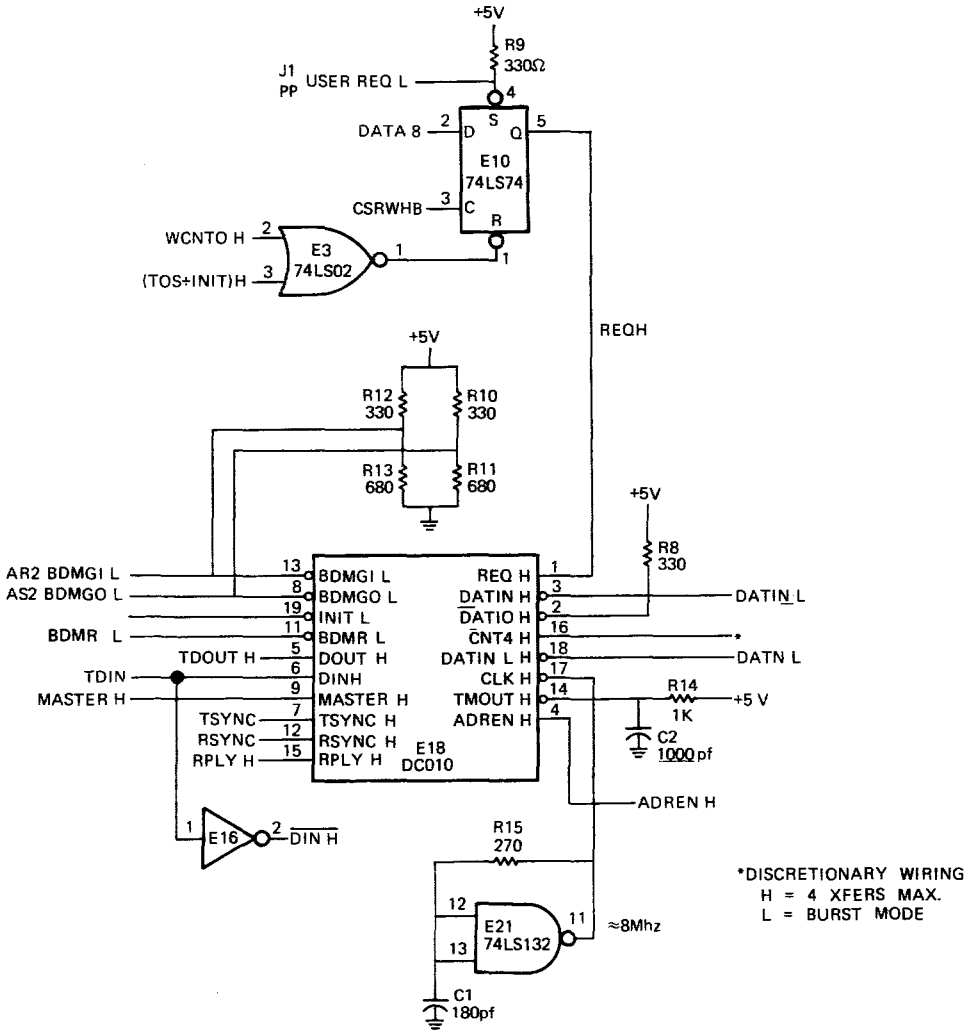


Figure 4 Typical Application (DC006, DC010, Output Delay, and Input Drives)
(Sheet 1 of 2)

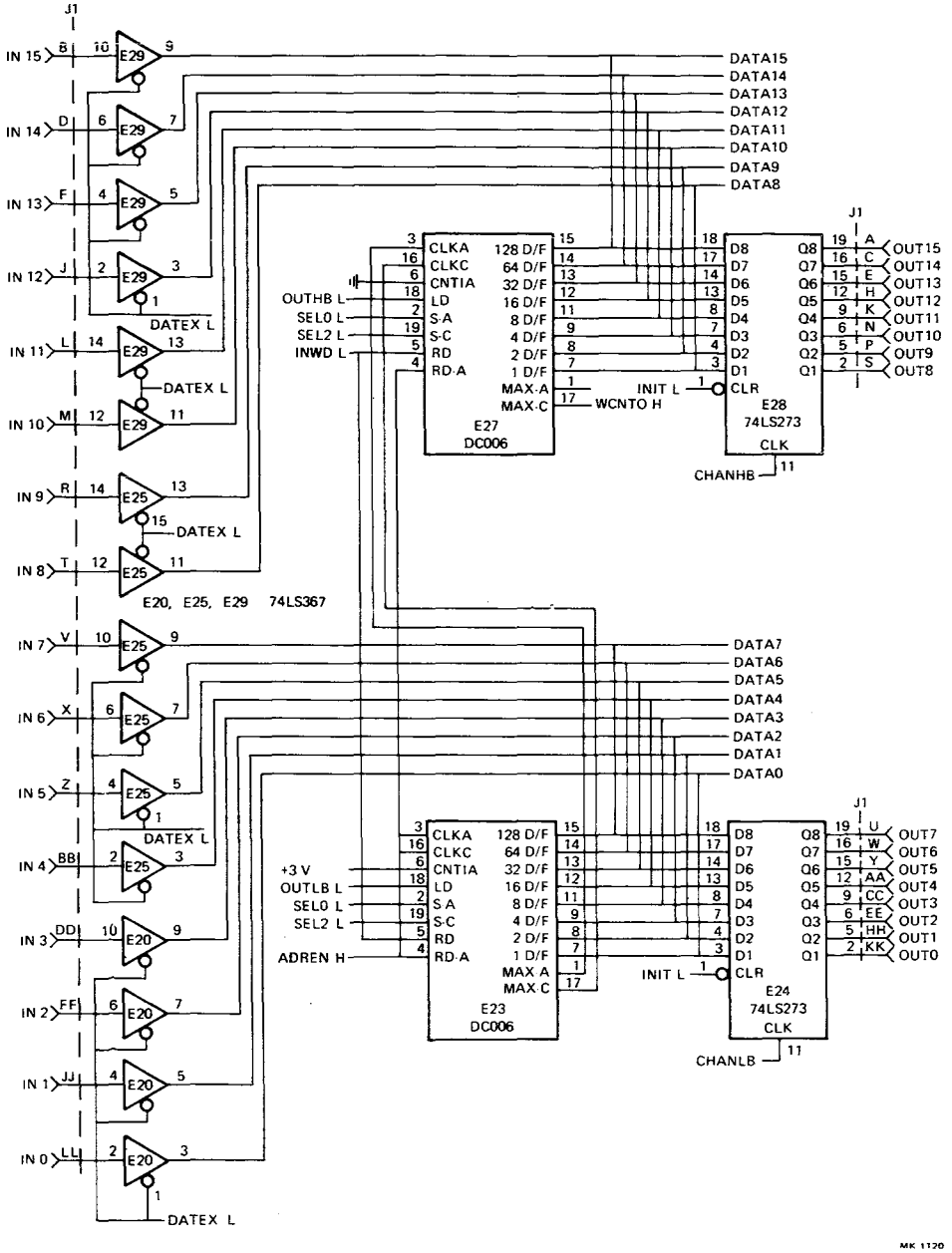


Figure 4 Typical Application (DC006, DC010, Output Delay, and Input Drives)
(Sheet 2 of 2)

User devices initiate bus requests by driving the set input of the request flip-flop (E10) low. This asserts REQ to the DC010 and generates BDMR L to the LSI-11 bus. When the DC010 becomes bus master, it asserts ADREN H to the DC006 bus address registers. ADREN H allows the bus address registers to place the address of the slave (memory) onto the internal bus and, via the DC005 transceivers, onto the LSI-11 bus. The request flip-flop (E10) remains set until the DC006 word count overfows to zero (WCNT0). WCNT0 then resets the request flip-flop.

Two DC006 word count/bus address register ICs are used to provide 16 bits each of word count and bus address. The least significant bits of the word count and bus address register and register C is the word count register. Both registers can be read or written under program control from the LSI-11 bus. Registers are selected by:

• Read bus address register	SEL 0 L INWD L
• Write high byte of bus address register	SEL 0 L OUTHB L
• Write low byte of bus address register	SEL 0 L OUTLB L
• Read word count register	SEL 2 L INWD L
• Write high byte of word count register	SEL 2 L OUTHB L
• Write low byte of word count register	SEL 2 L OUTLB L

The bus address register is incremented by two for word transfers. To accomplish the increment by two, the CNT1A input to the most significant DC006 (E23) must be high, and the CNT1A input to the most significant DC006 (E27) must be grounded. Clocking for DC006 E23 is provided by the transition of the ADREN H line from the DC010. When bus address register DC006 E23 overflows, MAX-A goes high, thus clocking the DC006 E27 bus address register.

The word count register is incremented by one each time a word is transferred. Initially, the word count register is loaded under program control, with the 2's complement of the number of words to be transferred. As words are transferred, the word count register is incremented toward zero. When DC006 E23 overflows, MAX-C goes high. MAX-C clocks the DC006 E27 word count register until DC006 E27 overflows. When E27 overflows, WCNT0 H is generated; WCNT0 H then resets the request flip-flop (E10), thus terminating data transfers.

During DMA data transactions input data from the DATI bus cycle is placed on the internal 3-state bus via the DC005 transceivers and is applied to he 74LS273 (E28 and E24) output buffers. These buffers are then clocked by CHANHB and CHANLB, thus placing the data on the 16 OUT lines to the user's device.

For output data transfers (DATO), the user's device places data on the 16 IN lines to the 74LS367 3-state drivers. The drivers are enabled by DATEX L, which is asserted during a DATO cycle. The data passes through the drivers, is applied to the internal 3-state bus and, via the DC005 transceivers, to the LSI-11 bus.

Miscellaneous Logic

Miscellaneous logic is shown in Figure 5. This logic includes CSR, output buffer and input driver control, non-existent address time-out, DC005 transceiver receive/transmit control, the control/status register (CSR), additional transceivers (8641s), and the "B" request flip-flop.

The CSR, output buffers, and input driver control receive INWD L, OUTHB L, OUTLB L, SEL 4 L, SEL 6 L, DATN H, and DIN H. These signals are gated to produce enable signals for the CSR, the output buffers, and the input drivers. CSR RD is produced by INWD L and SEL 4 L to enable the CSR data (DATA 5 through DATA 14) (Figure 5, sheet 1) to pass through the 74LS367 3-state drivers and onto the LSI-11 bus via the DC005 transceivers. OUTHB L, OUTLB L, SEL 4 L, and MRPLY L produce either CSRWHB L or CSRWLB L for writing bit 6 of the CSR (74LS74 E10 on Figure 3, sheet 1), or for clocking the "B" request flip-flop. DATEX L enables the 74LS367 3-state input drivers (Figure 5, sheet 1) during an "input" cycle. The CHANHB and CHANLB signals clock the 74LS273 output buffers during an "output" cycle. When bytes are transferred, OUTHB L, MRPLY L and SEL 6 L enable the high byte (CHANHB L asserted), while OUTLB L, MRPLY and SEL 6 L enable the low byte (CHANLB L). Both bytes are simultaneously transferred (word transfer) when DIN H is negated.

The non-existent address time-out provides a 10 μs time-out in the event that a non-existent address is requested on the LSI-11 bus during a DMA operation. This prevents hanging-up the LSI-11 bus for periods longer than 10 μs. When the DC010 becomes bus master, ADREN H is asserted and cocks the 10 μs one-shot (E8). Normally RPLY L from the LSI-11 bus goes low and the one-shot is cleared. However, if RPLY L is high (no response from slave), the one-shot times out and cocks the 74LS74 flip-flop (E9). The flip-flop is set, generating (TOS + INIT) L; this signal is applied to the DC010 (Figure 4, sheet 1) clearing the internal synchronization circuit and releasing the LSI-11 bus. The signal (TOS + INIT) H resets the request flip-flop (E10). The 74LS74 flip-flop (E9) can be set and reset with CSRW HB and DATA 15 (CSR bus time-out). This flip-flop is automatically reset during power-up.

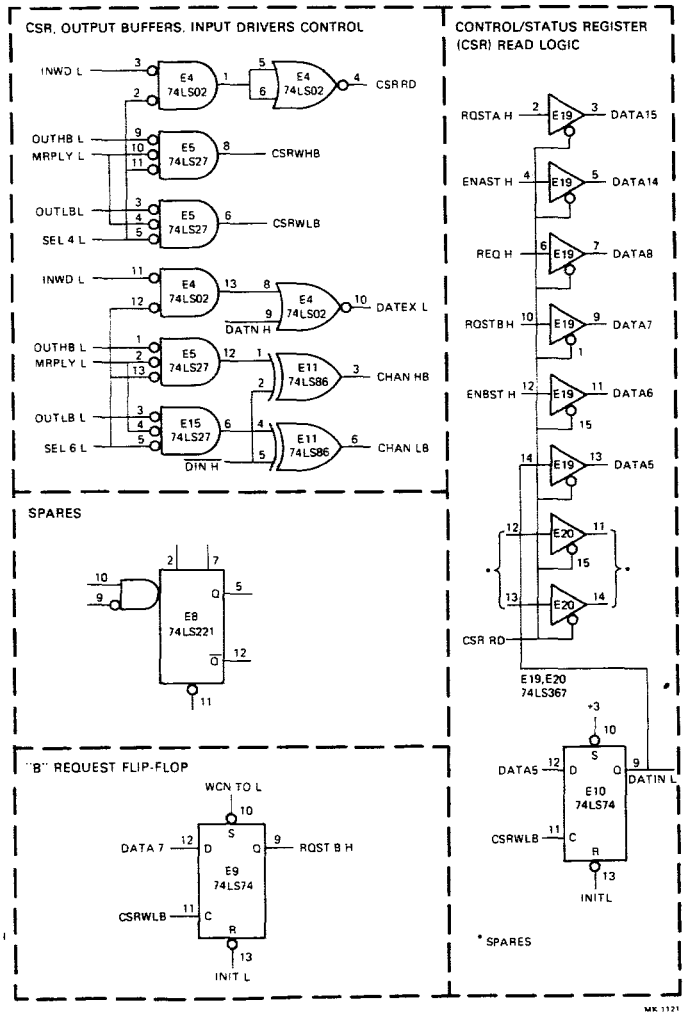


Figure 5 Typical Application (Miscellaneous Logic) (Sheet 1 of 3)

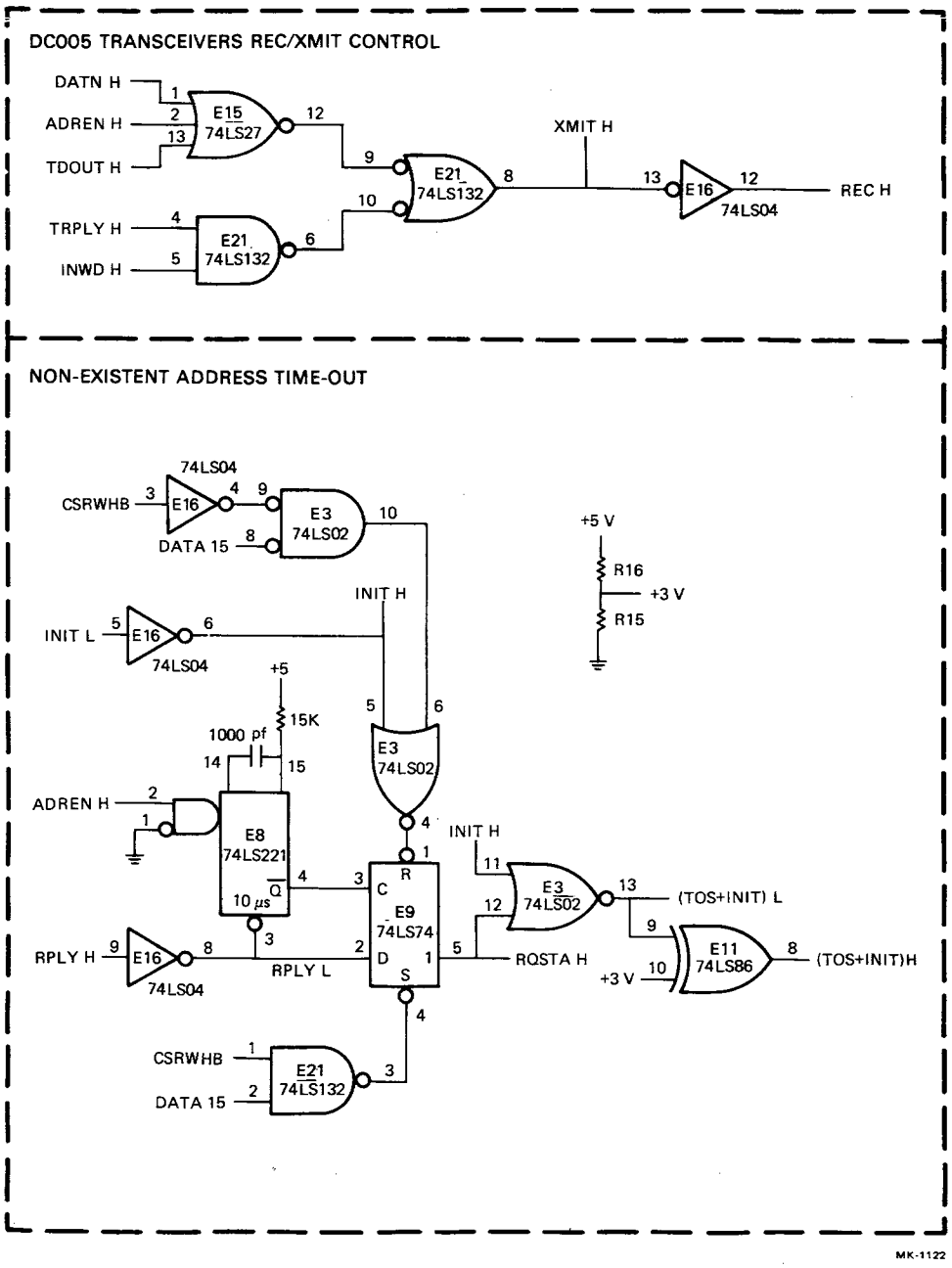


Figure 5 Typical Application (Miscellaneous Logic)
(Sheet 2 of 3)

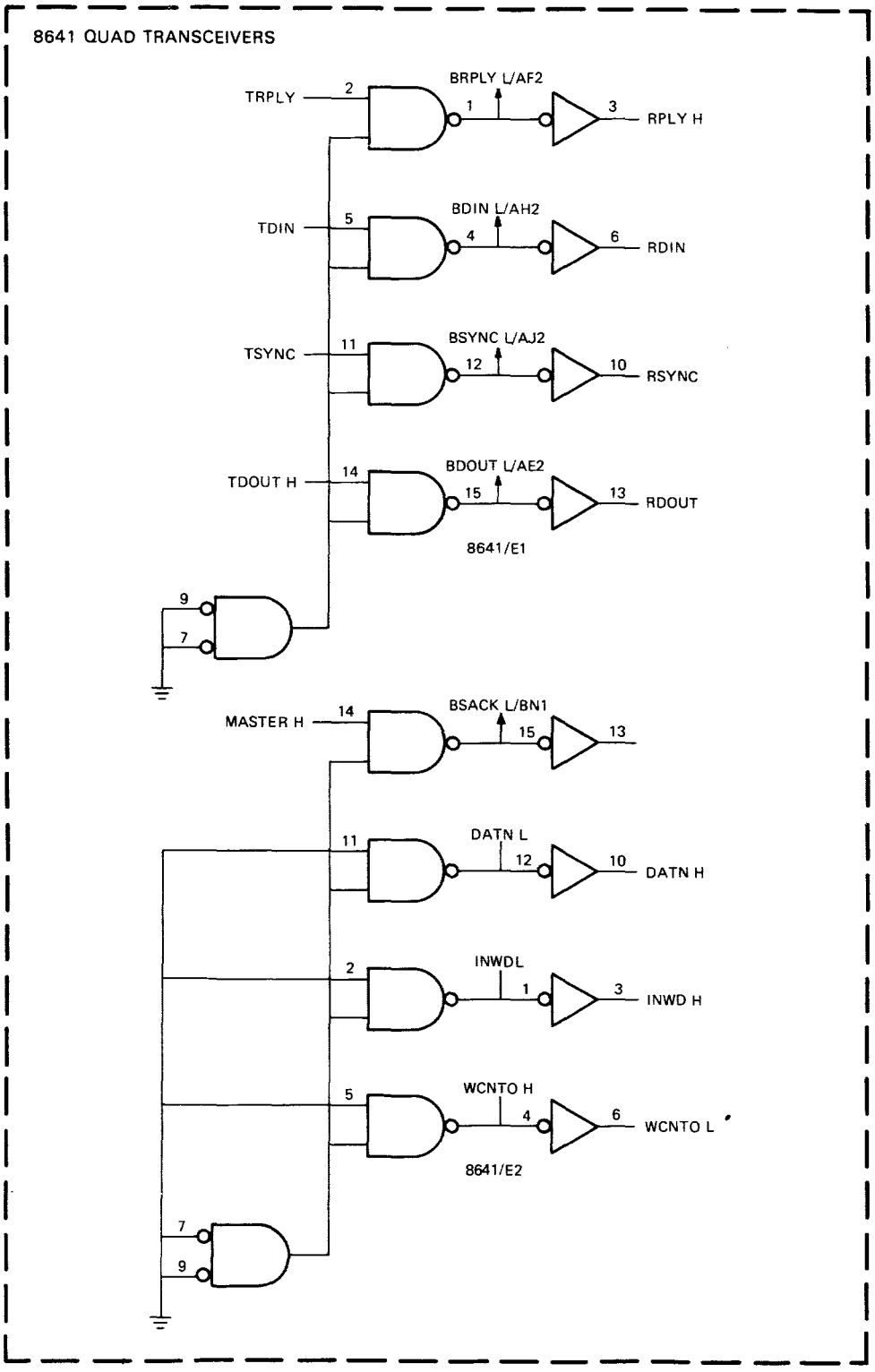


Figure 5 Typical Application (Miscellaneous Logic)
(Sheet 3 of 3)

The DC005 transceiver receive/transmit control determines the state of the DC005 transceivers. Normally, the transceivers are in the receive state to accept device addresses from the LSI-11 bus. When REC H is asserted (high), XMIT is negated (low). XMIT is asserted (high) when transferring data to the LSI-11 bus (TDOUT, DATEN, and ADREN are high; TRPLY, INWD are low). REC is asserted (high) when receiving data from the LSI-11 bus (TDOUT, DATEN, and ADREN are low; TRPLY, INWD are high).

The control/status register (CSR) (Figure 5, sheet 1) has six active bits and is a read/write register comprised of 74LS367 3-state drivers and flip-flops which are part of other logic circuits shown in Figure 3, sheet 1 and Figure 5, sheet 2. Figure 6 shows the CSR format.

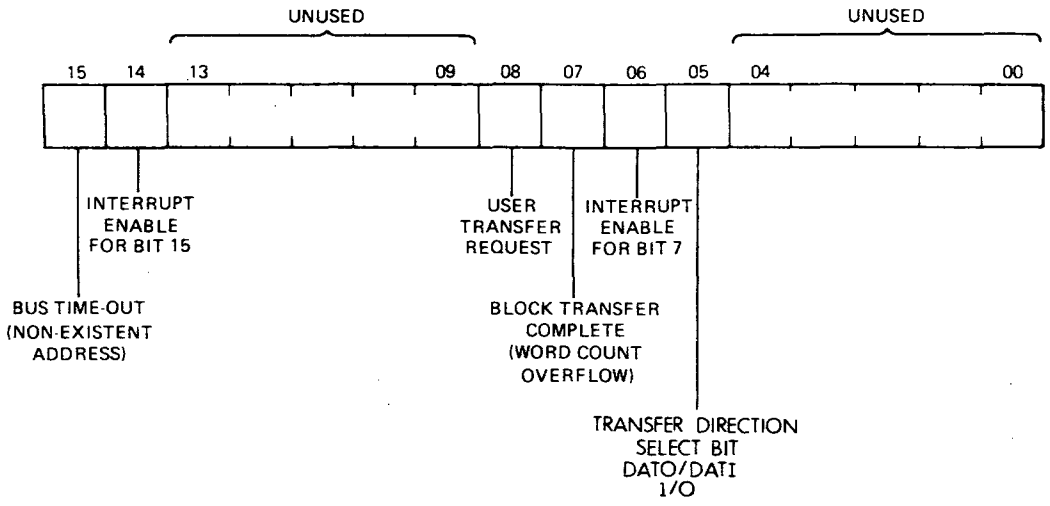


Figure 6 Control/Status Register (CSR) Format

The quad transceivers (8641) shown in Figure 3,sheet 3 supplement the DC005 transceivers for interfacing to the LSI-11 bus. In this particular application, the 8641s are permanently enabled by grounding pins 7 and 9.

CSR Bit Descriptions

Bit	Name	Description
00	Unused	
01		
02		
03		
04		
05	DATO/DATI	When set to a 1, indicates a DATO cycle; when set to a 0, indicates DATI bus cycle.
06	Interrupt enable for bit 7	This bit must be set (1) to enable the word count overflow interrupt at the end of a block transfer. When set to 0, the interrupt is inhibited.
07	Block transfer complete	This bit sets (1) when the word count register overflows, providing bit 06 is set.
08	User transfer request	The user's device must set (1) this bit to make a bus request and transfer data. User REQ L (J1-PP) must be driven low (0) to set bit 08. This bit is always read as a zero. This is an example for test purposes.
09	Unused	
10		
11		
12		
13		
14	Interrupt enable for bit 15	This bit must be set (1) to enable the bus time-out interrupt. When set to a 0, the interrupt is inhibited.
15	Bus time-out	This bit sets (1) when a slave on the LSI-11 bus does not respond with BRPLY within 10 μs after being addressed. Bit 14 must be set (1) to enable the bus time-out interrupt.

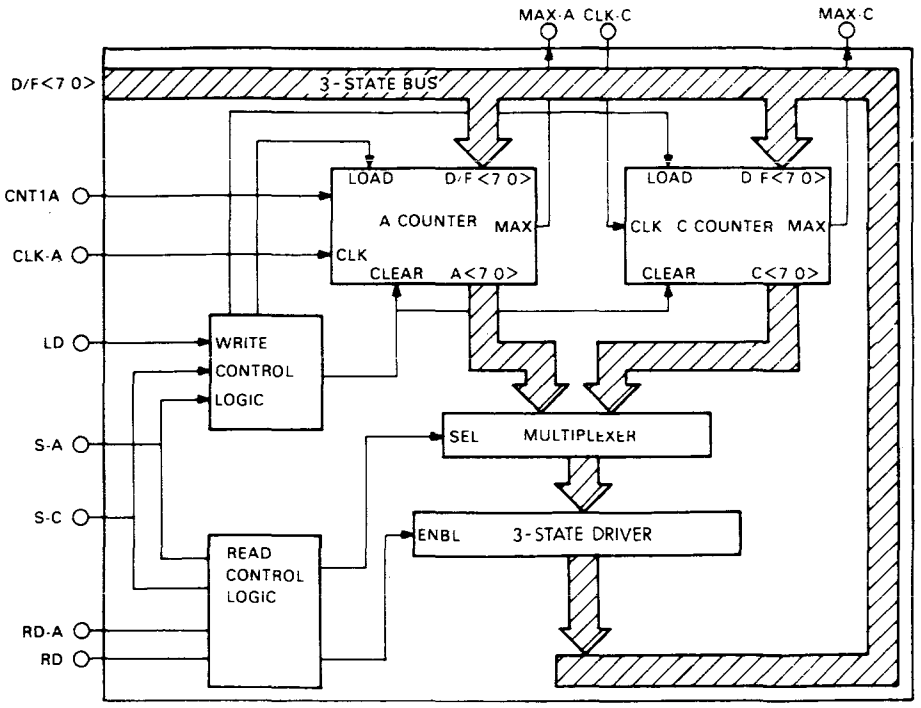


Figure 7 DC006 Simplified Block Diagram

DC006 WORD COUNT/BUS ADDRESS LOGIC

The word count/bus address (WC/BA) chip is a 20-pin, 0.762 cm center x 2.74 cm long (0.3 in center x 1.08 in long) DIP, low-power Schottky device. Its primary use is in DMA peripheral device interfaces. This IC is designed to connect to the 3-state side of the DC005 transceiver. The DC006 has two 8-bit binary up-counters, one for the word (byte) count and another for bus address. Two DC006 ICs may be cascaded to increase register implementation.

The chip is controlled by the address latch protocol chip (DC004), the DMA chip (DC010), and a minimum of ancillary logic. Both counters may be cleared simultaneously. Each counter is separately loaded by LD and the corresponding select line from the protocol chip. Each counter is incremented separately. The WC counter (word byte counter) is always incremented by one; the A counter (bus address) may be incremented by one or two for byte or word addressing, respectively.

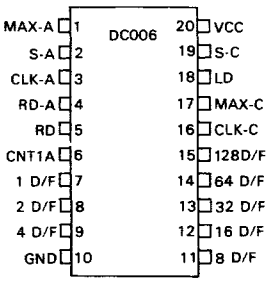
Data from the DC006 IC is placed on the 3-state bus via internal 3-state drivers. Each counter is separately read by RD and the corresponding select line.

Figure 7 is a block diagram of the DC006 IC while Figure 8 illustrates a simplified logic diagram. The DC006 pin/signal description is presented in Table 2.

TRUTH TABLES
WHERE L = TTL LOW
H = TTL HIGH
X = DON'T CARE
Z = HIGH IMPEDANCE
↓ = HIGH TO LOW TRANSITION

READ CONTROL

INPUTS				OUTPUTS
LD - H		S-A	S-C	D/F<7:0>
RD-A	RD			
L	L	L	L	CLEAR A&C AND READ C
L	L	L	H	A<7:0>
L	L	H	L	C<7:0>
L	L	H	H	Z
L	H	X	X	Z
H	L	L	L	CLEAR A&C AND READ A
H	L	L	H	A<7:0>
H	L	H	L	A<7:0>
H	L	H	H	A<7:0>
H	H	L	L	CLEAR A&C AND READ A
H	H	L	H	A<7:0>
H	H	H	L	A<7:0>
H	H	H	H	A<7:0>



WRITE CONTROL

INPUTS			FUNCTION
RD - A = L, RD = H	S-A	S-C	
LD			
↓	L	L	*ILLEGAL
↓	L	H	LOAD A<7:0>
↓	H	L	LOAD C<7:0>
X	H	H	WC/BA NOT SELECTED
H	L	L	CLEAR BOTH COUNTERS
H	L	H	LOADING DISABLED
H	H	L	LOADING DISABLED

*ILLEGAL CONDITION BECAUSE A LOAD OPERATION AND A CLEAR OPERATION IS ATTEMPTED SIMULTANEOUSLY. RESULT OF THIS OPERATION IS TO CLEAR BOTH COUNTERS.

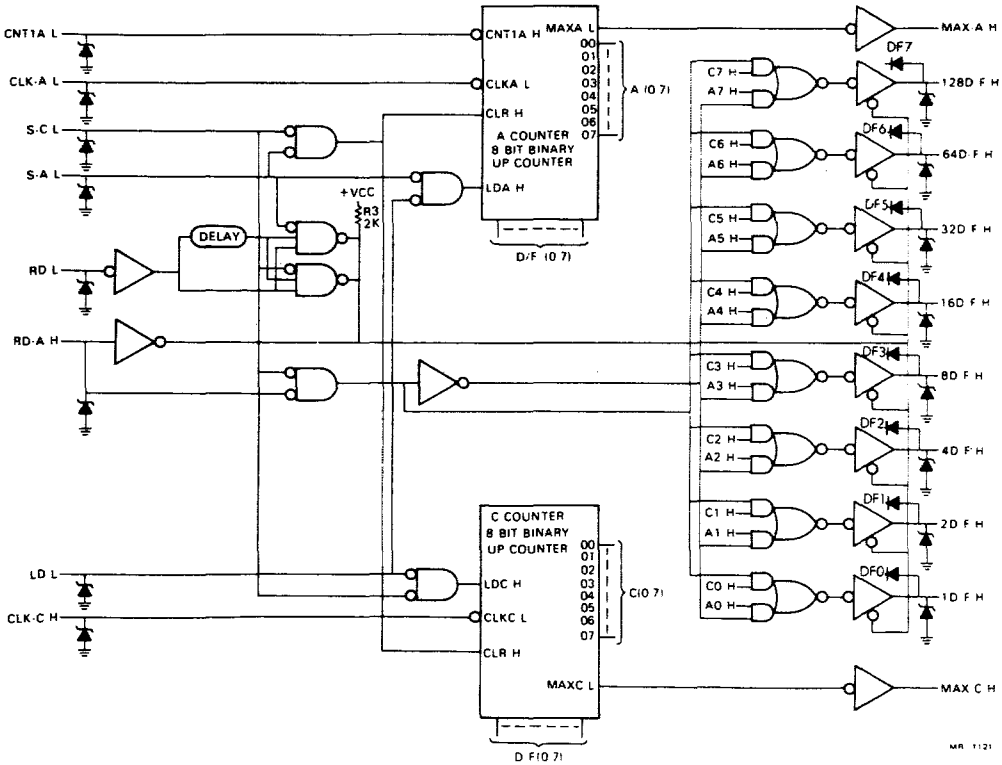


Figure 8 DC006 Simplified Logic Diagram

DC010 DIRECT MEMORY ACCESS LOGIC

The Direct Memory Access (DMA) chip is a 20-pin, 0.762 cm center × 2.74 cm long (0.3 in. center × 1.08 in. long) DIP, low-power Schottky device for primary use in DMA peripheral device interfaces using the LSI-11 bus.

This device provides the logic to perform the handshaking operations required to request and to gain control of the system bus. Once bus mastership has been established, the DC010 generates the required signals to perform a DATI, DATO, or DATIO transfer as specified by control lines to the chip. The DC010 IC has a control line that will allow multiple transfers or only four transfers to take place before giving up bus mastership.

Figure 9 is a simplified logic diagram of the DC010 IC. The logic symbols and truth table are presented in Figure 10.

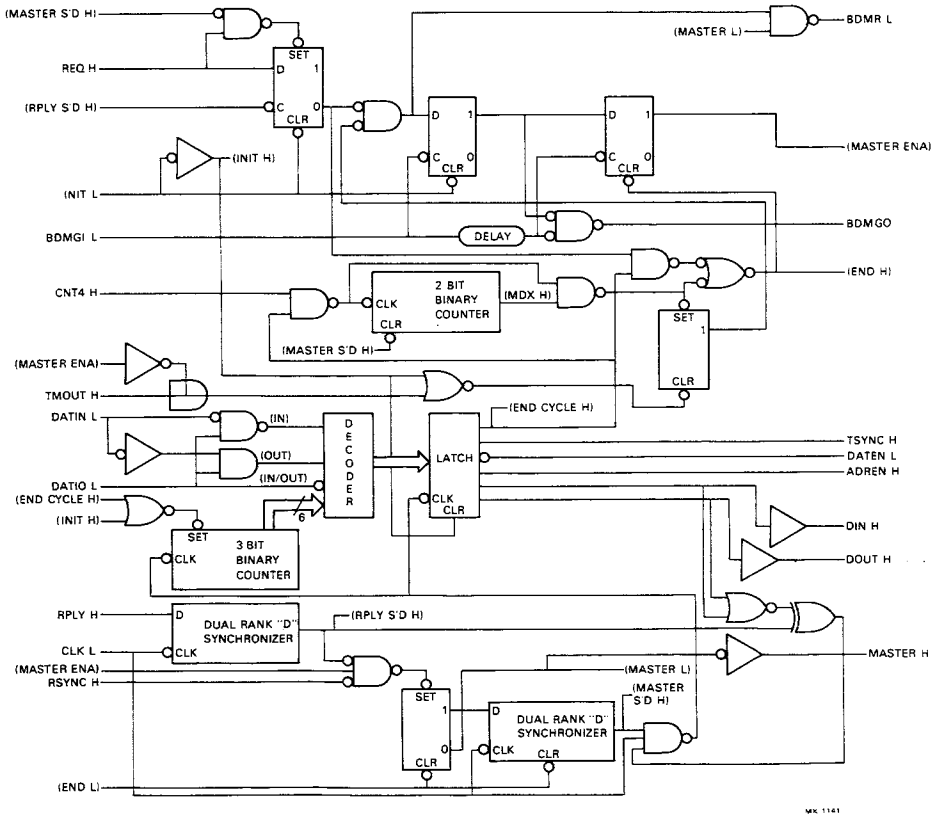
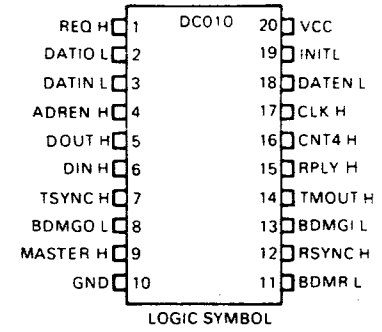


Figure 9 DC010 Simplified Logic Diagram



LOGIC SYMBOL

TRUTH TABLE

WHERE L = TTL LOW
H = TTL HIGH
X = DON'T CARE

INPUTS		TRANSFER TYPE
DATIN	DATIO	
X	L	DATIO
L	H	DAT I
H	H	DATO

Figure 10 DC010 Logic Symbol/Truth Table

DDV11-B

DDV11-B Backplane

INTRODUCTION

The DDV11-B is an optional LSI-11 bus expansion backplane for use when additional logic space is required. The DDV11-B is a 9 × 6, 54-slot backplane with a 9 × 4 slot section (18 individual double-height or nine quad-height module slots) prebused specifically for LSI-11 bus signal, power, and ground connections. The remaining 9 × 2 slot section is provided with +5 Vdc, GND, and −12 Vdc powerconnections only; this leaves the remaining pins free for use with any special double-height logic modules to be used in conjunction with the LSI-11 family of modules and bus requirements.

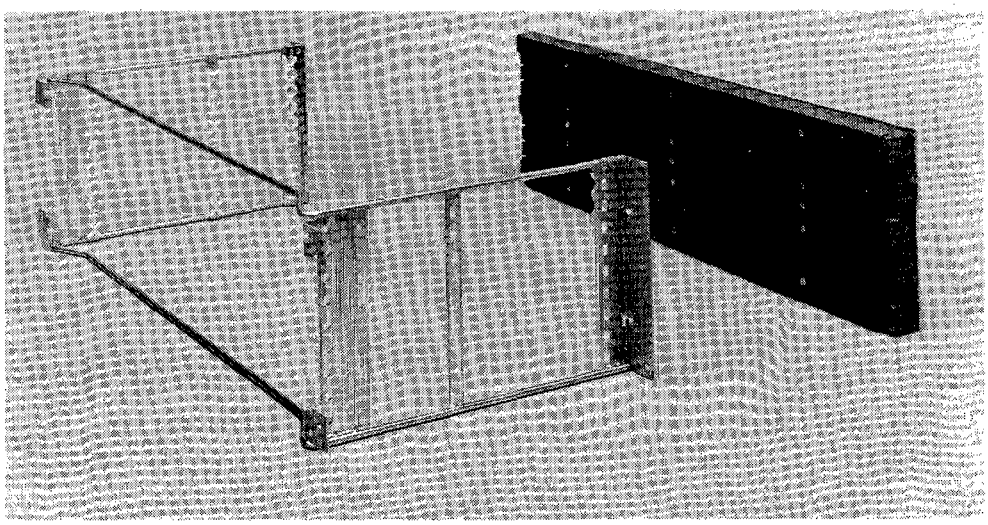
DESCRIPTION

The DDV11-B consists of an H034 system unit mounting-frame, six H863 and three H8030 connector blocks, and the etched- board bus structure necessary for signal routing. The etched board completely overlays the entire pin side of all connector blocks and is recessed sufficiently to allow wirewrapping on those same pins with 30-AWG wire.

An optional cardcage, type H0341, is also available to provide protection against physical damage to modules and to serve as a cardguide. The cardcage completely surrounds the slot side of the system unit and is shown in Figure 1. The DDV11-B can be mounted in the H909-C enclosure.

NOTE

The H909-C includes the H0341 cardguide.



7920 - 28W - A0169

Figure 1 DDV11-B with H0341 Card Assembly

DDV11-B

CONFIGURATION

Module Slot Assignments

Figure 2 shows the slot location assignments of the DDV11-B. Rows A, B, C, and D are dedicated to the LSI-11 bus. Any module which conforms to the LSI-11 bus specifications can be used in this portion of the DDV11-B. The position numbers indicate the bus-grant wiring scheme with respect to the processor module. The bus-grant signals propagate through the slot locations in the position order shown in Figure 2 until they reach the requesting device. Any unused slots must be jumpered to provide busgrant signal continuity, or it is recommended that unused locations occur only in the highest position-numbered locations.

Rows E and F contain the 18 user-defined slots with power and ground connections provided.

Equipment Supplied

The DDV11-B option consists of the following items:

Six H863 connector blocks
Three H8030 connector blocks
Etched-board bus structure

Installation

The DDV11-B can be mounted on panels or chassis using standard hardware. The overall dimensions of the unit are shown in Figure 3. The H034 mounting frame of the DDV11-B is provided with tapped holes and clearance holes to enable the attachment of the system unit.

H0341 Card Assembly Mounting

The card assembly provides nylon guides which help to guide and support the modules installed in the system unit. The H0341 card assembly is supplied with the hardware necessary to mount to the H034 mounting frame. Figure 4 shows the method of assembly. Two screws (item 2) and two washers (item 1) are inserted through the clearance holes of the PC board and H034 mounting frame and into the two threaded inserts on each bracket of the card assembly.

DDV11-B

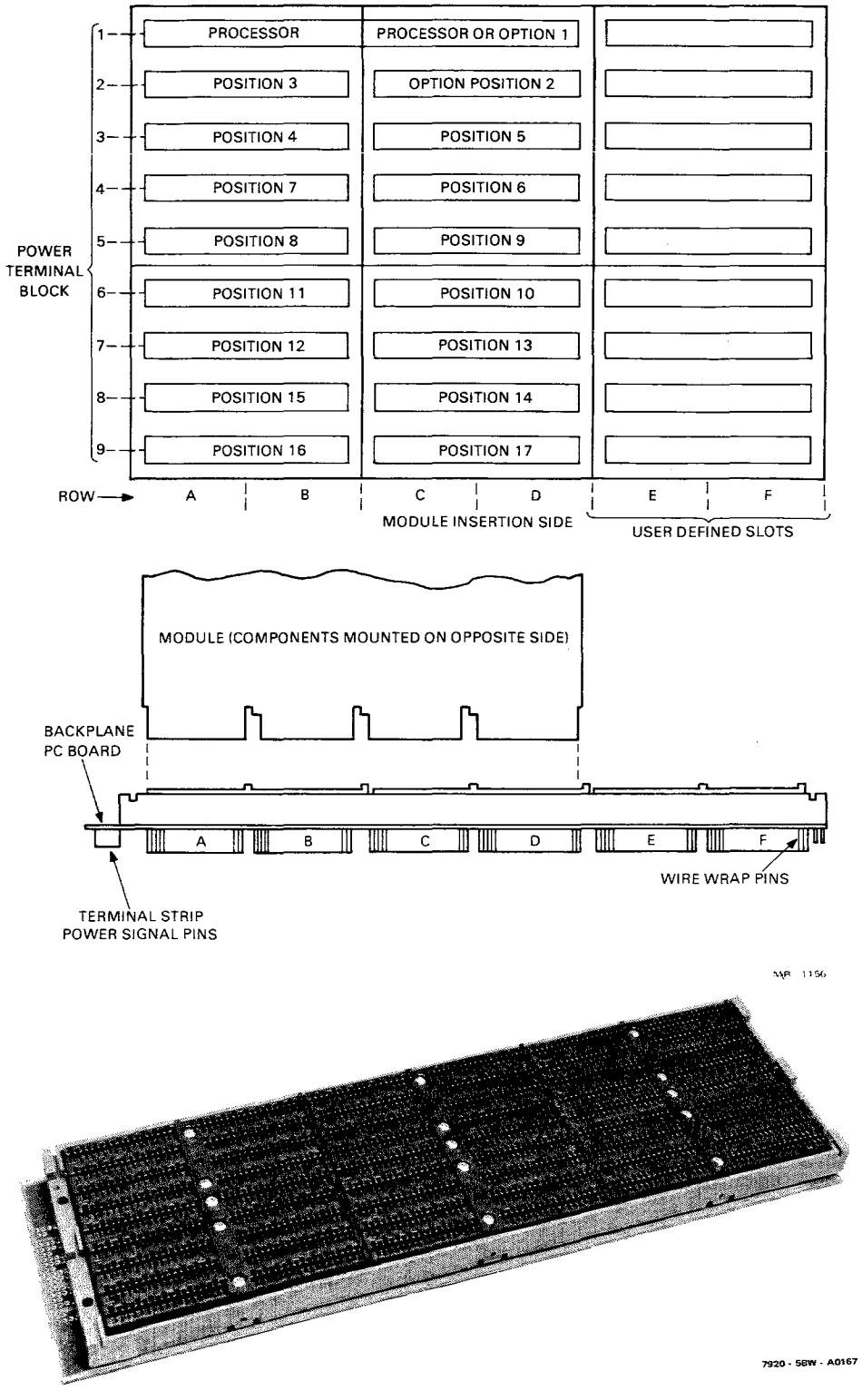
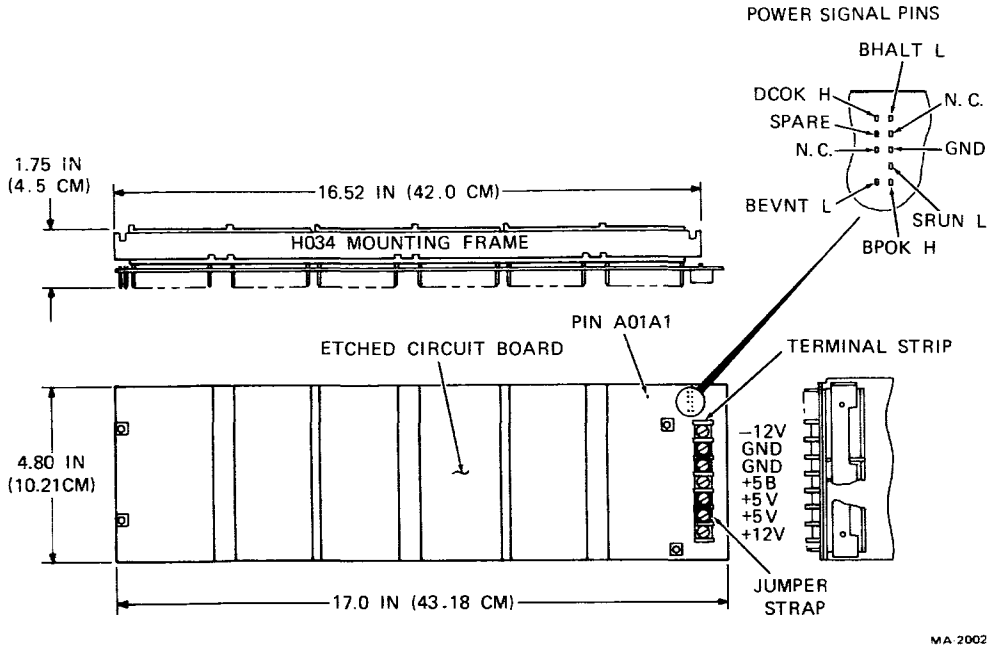


Figure 2 DDV11-B Module Installation and Slot Assignments



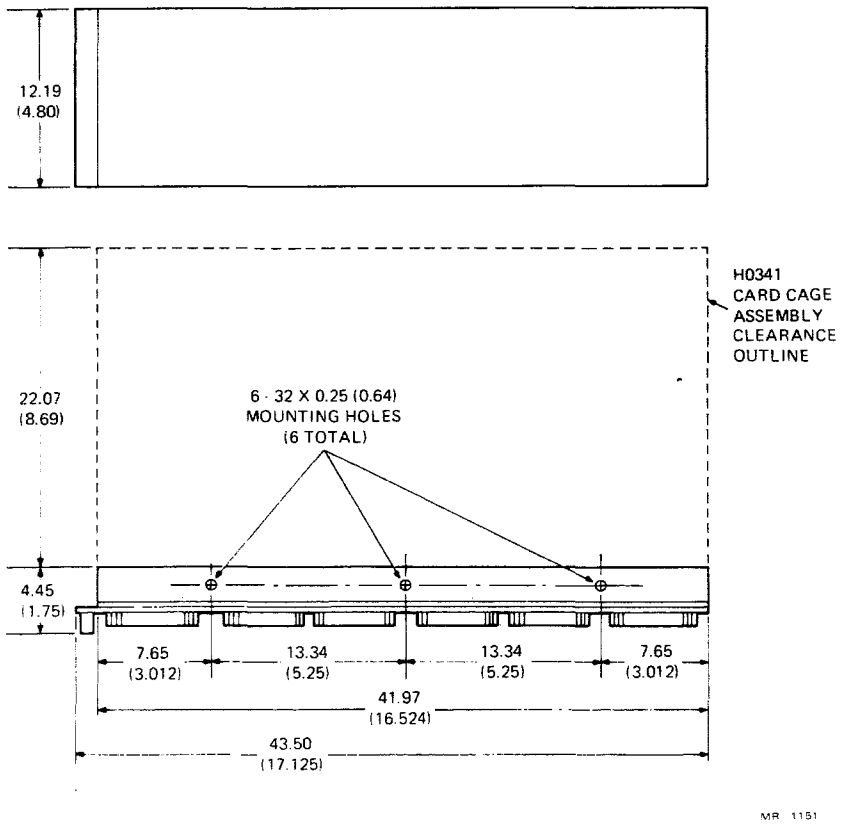


Figure 3 DDV11-B Power Wiring and Dimensions

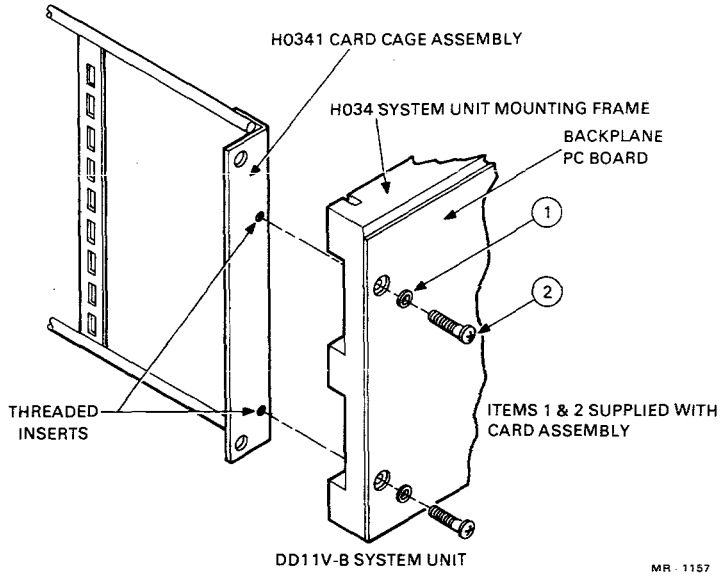


Figure 4 H0341 Card Assembly Installation

dc Power and PowerSignal Connections

dc power is supplied to the modules in the DDV11-B through the backplane PC board. The power and ground leads from the external source connect to the seven-position terminalboard mounted on the edge of the PC board as shown in Figure 3. Any suitable connector terminals, solder, or crimp style, can be attached to the powersupply leads and inserted under the terminal strip screws. A jumpertab is mounted between the two +5 V screws and between the two ground (GND) screws on the terminal board. The total current capability of the DDV11-B and the wire size required are as follows:

Terminal		Current (Max)	Wire Size (AWG)
+12 V		20 A	14
+5 V	Jumped	40 A	14
+5 V			
+5 B		20 A	
GND	Jumped	40 A	14
GND			
−12 V		20 A	

Figure 5 identifies the powersignal pins which are located at the opposite end of the backplane PC board from the power terminal strip. A mating female connector (DIGITAL P/N 12-11206-02 or 3M P/N 3473-3) can be inserted over the pins and used to connect the external signals to the backplane.

Backplane Pin Assignments

Table 1 lists the backplane pin assignments for the LSI-11 bus signals and dc power and ground connections on the DDV11-B backplane.

Table 1 DDV11-B Backplane Pin Assignments

Side	2	1	2	1	2	1	2	1
Row	A&C	A&C	B&D	B&D	E	E	F	F
A	+5V	BSPARE1	+5V	BDCOK H	+5V	BLANK	+5V	BLANK
B	−12V	BSPARE2	−12V	BPOK H	−12V	BLANK	−12V	BLANK
C	GND	BDAL 17 L	GND	SSPARE 4	GND	BLANK	GND	BLANK
D	+12V	BDAL 16 L	+12V	SSPARE 5	BLANK	BLANK	BLANK	BLANK
E	BDOUT L	SSPARE1	BDAL2 L	SSPARE 6	BLANK	BLANK	BLANK	BLANK
F	BRLPY L	SSPARE2	BDAL3 L	SSPARE 7	BLANK	BLANK	BLANK	BLANK
H	BDIN L	SSPARE3	BDAL4 L	SSPARE 8	BLANK	BLANK	BLANK	BLANK
J	BSYNC L	GND	BDAL5 L	GND	BLANK	BLANK	BLANK	BLANK
K	BWTBT L	MSPAREA	BDAL6 L	MSPARE B	BLANK	BLANK	BLANK	BLANK
L	BIRQ L	MSPAREA	BDAL7 L	MSPARE B	BLANK	BLANK	BLANK	BLANK
M	BIAK I L	GND	BDAL8 L	GND	BLANK	BLANK	BLANK	BLANK
N	BIAK O L	BDMR L	BDAL9 L	BSACK L	BLANK	BLANK	BLANK	BLANK
P	BBS 7 L	BHALT L	BDAL10 L	BSPARE 6	BLANK	BLANK	BLANK	BLANK
R	BDMG 1 L	BREF L	BDAL11 L	BEVNT L	BLANK	BLANK	BLANK	BLANK
S	BDMG 0 L	PSPARE3	BDAL12 L	PSPARE 4	BLANK	BLANK	BLANK	BLANK
T	BINIT L	GND	BDAL13 L	GND	BLANK	GND	BLANK	GND
U	BDAL 0 L	+12B	BDAL14 L	PSPARE 2	BLANK	BLANK	BLANK	BLANK
V	BDAL 1 L	+5B	BDAL15 L	+5	BLANK	BLANK	BLANK	BLANK

DLV11

DLV11 SERIAL LINE UNIT

SPECIFICATIONS

Identification	M7940
Size	Double
Power	+5.0 Vdc ± 5% at 1.0 A (1.6 A max) +12.0 Vdc ± 3% at 0.18 A (0.25 A max)
Bus loads	
ac	2.5
dc	1.0

CONFIGURATION

The user can select the register address, parity, number of data bits, number of stop bits, baud rate, and type of serial interface. The descriptions of the registers and their standard factory addresses are listed in Table 1. Available jumpers are shown in Figure 1 and their applications are listed in Table 2.

Table 1 Standard Addresses

Register	Mnemonic	Console	Second Module
Receiver control status	RCSR	177560	176500
Receiver data buffer	RBUF	177562	176502
Transmit control/status	XCSR	177564	176504
Transmit data buffer	XBUF	177566	176506
Standard vectors	RCSR	060	300
	XCSR	064	304

DLV11

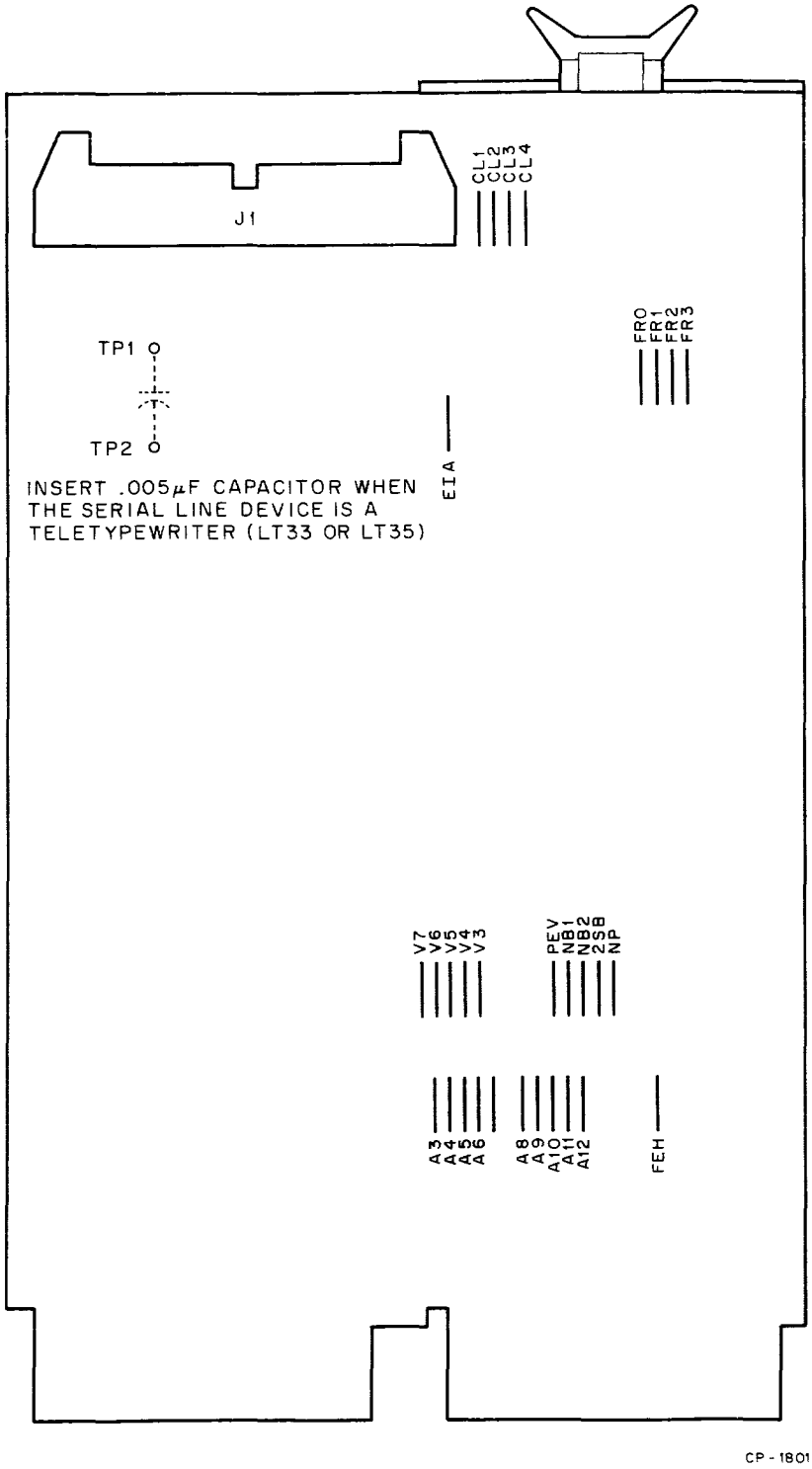


Figure 1 DLV11 Jumper Locations

Table 2 DLV11 SLU Factory Jumper Configuration

Jumper Designation	Jumper State*	Function Implemented
A3	I	This arrangement of jumpers A3 through A12 implements the octal device address 17756X, which is the assigned address for the console device SLU. The least significant digit is hardwired on the module to address the four SLU device registers as follows: X = 0, RCSR address X = 2, Receive data register address X = 4, XCSR address X = 6, Transmit data register address
A4	R	
A5	R	
A6	R	
A7	I	
A8	R	
A9	R	
A10	R	
A11	R	
A12	R	
V3	I	This jumper arrangement implements the interrupt vector: 60 for received data and 64 for transmitted data.
V4	R	
V5	R	
V6	I	
V7	I	
NP	R	No parity
2SB	R	Two stop bits
NB2	R	Eight data bits
NB1	R	
PEV	R	Even parity if NP installed
FEH	I	Halt on framing error
EIA	I	12 V EIA operation enabled
FR0	R	
FR1	R	110 baud rate selected
FR2	R	
FR3	R	
CL1	I	20 mA current loop active receiver and transmitter selected
CL2	I	
CL3	I	(jumpered with 180 ohm resistors)
CL4	I	

* R = removed, I = installed

Addresses

Addresses for the DLV11 can range from 160000_8 through $17777X_8$. The least-significant-three bits (only bits 1 and 2 are used; bit 0 is ignored) address the desired register in the DLV11, as described in Table 1.

Address bits 3 through 12 are jumper-selected, as shown in Figure 2.

Since each DLV11 module has four registers, each requires four addresses. Addresses 177560-177566 are reserved for the DLV11 used with the console peripheral device. Additional DLV11 modules should be assigned addresses from 176500 through 176670, allowing up to 30 additional DLV11 modules to be addressed.

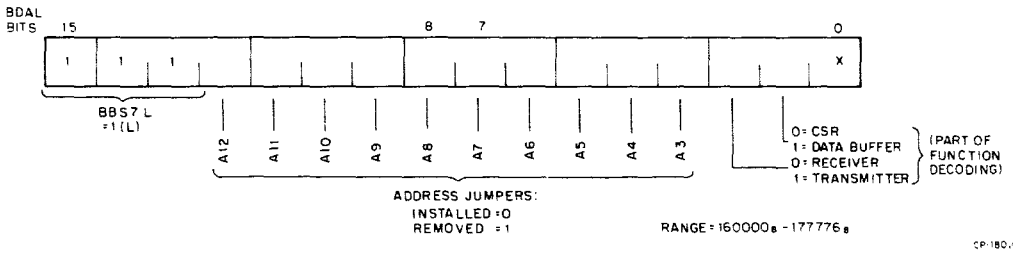


Figure 2 CSR Address Selection

UART Operation

The UART operation is programmed by using jumpers NP, 2SB, NB1, NB2, and PEV as shown below.

Number of Data Bits

	NB1	NB2
5	Installed	Installed
6	Removed	Installed
7	Installed	Removed
8	Removed	Removed

Number of Stop Bits Transmitted

2SB installed = One stop bit
2SB removed = Two stop bits

DLV11

Parity Transmitted
NP removed = No parity bit
NP and PEV installed = Odd parity
NP installed and PEV removed = Even parity

Baud Rate Selection
Baud rate is programmed via jumpers FR0 through FR3 as shown in Table 3.

EIA Interface
EIA drivers are enabled when jumper EIA is installed. It should be removed during 20 mA current loop operation.

20 mA Current Loop Interface
Jumpers CL1 through CL4 are associated with 20 mA current loop interface operation. CL2 and CL3 are 180 ohm resistors.

Active Current Loop

Transmit	CL4 Jumper installed CL3 Resistor installed
Receive	CL4 Jumper installed CL3 Resistor installed

Passive Current Loop

Transmit	CL4 Jumper removed CL3 Resistor removed
Receive	CL4 Jumper removed CL3 Resistor removed

Table 3 Baud Rate Selection

Baud Rate	FR3	FR2	FR1	FR0
50	I	I	R	I
75	I	I	R	R
110	R	R	R	R
134.5	I	R	I	I
150	R	R	R	I
200	I	R	I	R
300	R	R	I	R
600	I	R	R	I
1200	R	I	R	R
1800	R	I	R	I
2400	I	R	R	R
2400	R	R	I	I
4800	R	I	I	R
9600	R	I	I	I
External (via pin BH1)	I	I	I	X

NOTE:
I = Installed X = Irrelevant R = Removed

DLV11-E

DLV11-E ASYNCHRONOUS LINE INTERFACE

INTRODUCTION

The DLV11-E is an asynchronous line interface module that interfaces the LSI-11 bus to any of several types of serial communications lines. The module receives serial data from peripheral devices, assembles it into parallel data, and transfers it to the LSI-11 bus. It accepts data from the LSI-11 bus, converts it into serial data, and transmits it to the peripheral devices. The DLV11-E offers full modem control and EIA-type interface.

FEATURES

- Jumper- or program-selectable, crystal-controlled baud rates: 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, and 19,200. Split transmit and receive baud rates are possible.
- Provisions for user-supplied external clock inputs for baud rate control.
- Jumper-selectable data bit formats.
- LSI-11 bus interface and control logic for interrupt processing and vectored addressing of interrupt service routines.
- Full modem control (Bell 103, 113, 202C, 202D, and 212-compatible).

SPECIFICATIONS

Identification	M8017
Size	Double
Power	+5.0 Vdc ±5% at 1.0A +12.0 Vdc ±3% at 0.18 A
Bus loads	
AC	1.6
DC	1.0

DLV11-E

DESCRIPTION

Major functions contained on the DLV11-E are shown in Figure 1. Communications between the processor and the DLV11-E are executed via programmed I/O operations or interrupt-driven routines.

Bus Interface

The bus interface circuit signal lines consist of data moving between the LSI-11 bus and the module's internal tri-state bus. It decodes the device address and produces an address match (MATCH H) signal and it places interrupt vectors on the LSI-11 bus. The bus interface receives from the LSI-11 bus unless it is switched to transmit to the LSI-11 bus. The interrupt logic can cause the bus interface to transmit either a transmitter or receiver interrupt vector and the I/O control logic can cause the bus interface to transmit to or receive data from the LSI-11 bus.

The bus interface receives LSI-11 bus lines BDAL00 L through BDAL15 L and places them on the module's tri-state bus. If BBS7 L is asserted, the circuit decodes BDAL03 L through BDAL12 L and asserts MATCH H. Jumpers A3-A12 are configured to allow the option to respond to specific device register addresses. Jumpers V3-V8 select the options' interrupt vector.

I/O Control Logic

When the I/O control logic receives MATCH H from the bus interface, it decodes tri-state bus lines DAT00 H through DAT02 H and selects the addressed device register. The I/O control logic exchanges bus control signals with the processor to perform input and output data transfers.

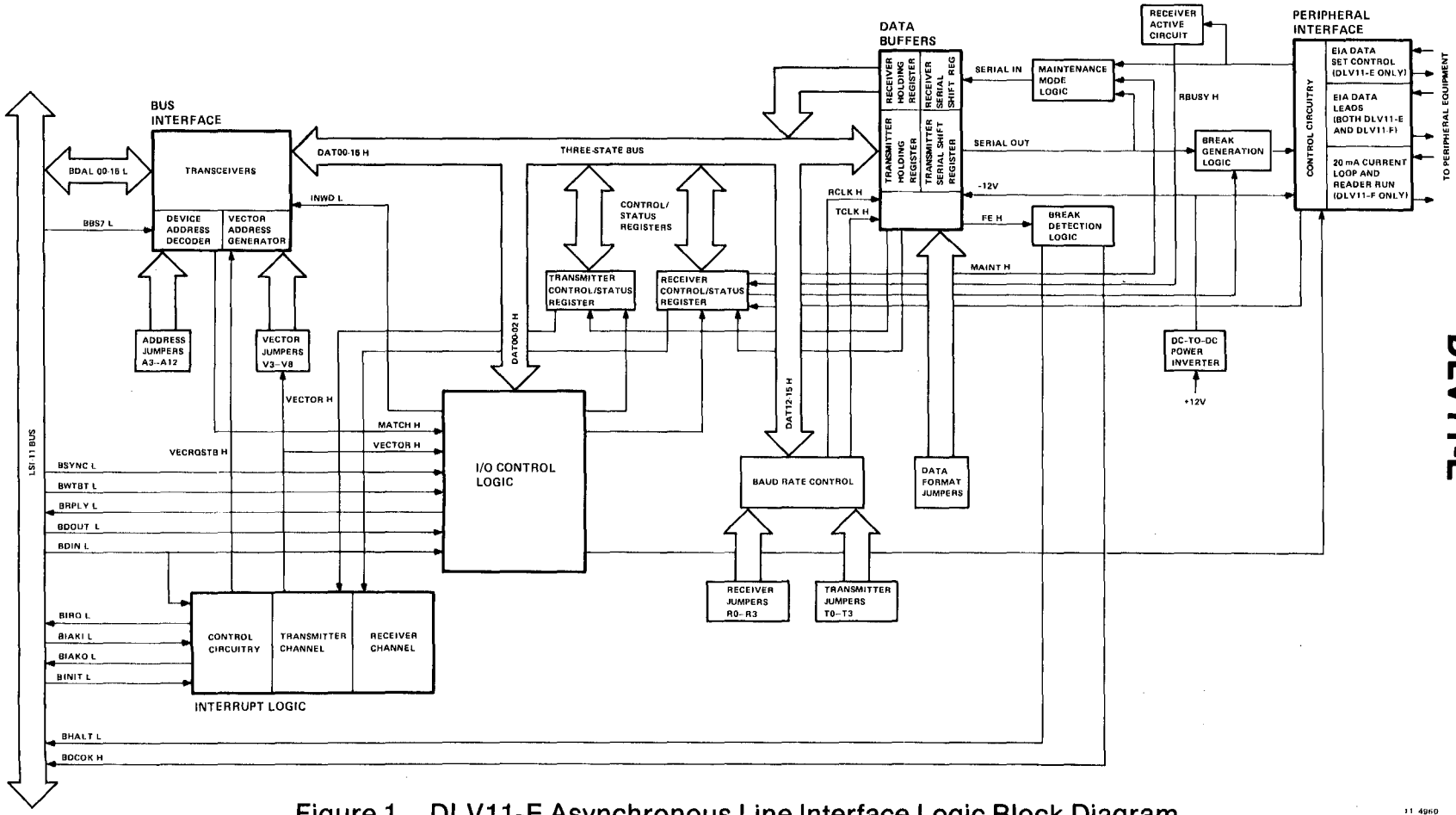


Figure 1 DLV11-E Asynchronous Line Interface Logic Block Diagram

11 4960

During an interrupt transaction, VECTOR H from the interrupt logic causes the circuit to assert BRPLY L in response to BDIN L. During data transactions, the I/O control logic asserts INWD L to switch the bus interface transceivers from receiving to transmitting.

Control/Status Registers

The receiver control/status register (RCSR) and the transmitter control/status register (XCSR) are enabled by selection signals from the I/O control logic. The CSRs are byte addressable for reading status bits or writing control bits.

Data Buffers

The receiver buffer (RBUF) and transmitter buffer (XBUF) provide double-buffering, in that one byte of data can be held while another byte is entering or exiting. This allows asynchronous, full-duplex operation. Data is handled in the low byte of the registers. The buffer control circuitry places receiver buffer error flag bits in the high byte of the RBUF. It also sends a status bit to the RCSR and a framing error bit (FE H) to the break logic.

Receiver Active Circuit

This circuit monitors the received serial data line and sets a status bit (RCVR ACT) as soon as the RBUF begins receiving data. It clears the bit when a character of data has been received.

Interrupt Logic

The DLV11-E can generate transmitter interrupts. If the XBUF is ready to serialize another character of data and the transmitter interrupt enable bit is set in the XCSR, the interrupt logic requests to interrupt the processor (by asserting BIRQ L.) If the processor acknowledges via the BIAKI/BIAKO daisy-chain, the interrupt logic asserts VECTOR H and VECRQSTB H. These signals cause the bus interface to place the transmitter function interrupt vector address on the LSI-11 bus.

The module also can request a receiver interrupt if the RBUF has received a character and the receiver interrupt bit is set in the RCSR. When the interrupt request is acknowledged, the interrupt logic asserts VECTOR H. VECTOR H causes the bus interface circuit to place the receiver function interrupt vector on the LSI-11 bus. (VECRQSTB H is used only for a transmitter interrupt.)

The DLV11-E also generates a receiver interrupt as a result of data set status. If the data set interrupt enable bit is set in the RCSR, a receiver interrupt will result from a change of state on any of the modem control lines (ring, clear to send, carrier, or secondary received data).

The interrupt acknowledge daisy-chain (BIAKI/BIAKO) passes through both the receiver and transmitter sections of the interrupt logic. It goes through the receiver section first, thereby giving the receiver channel priority over the transmitter channel.

Baud Rate Control

The baud rate control establishes the speed at which the data buffers handle serial data. It produces clock signals by dividing a crystal oscillator frequency by an amount selected by jumpers or the program. The circuit can be jumpered to generate either independent transmitter and receiver clocks (split speed operation) or a common clock (common speed operation).

When the programmable baud rate enable bit is set in the XCSR, the baud rate control decodes tri-state bus lines DAT12 H through DAT15 H. These bits control the receive baud rate in split speed operation and both transmit and receive baud rate in common speed operation. When programmable baud rate is not enabled, the baud rates are controlled by jumpers. In split speed operation, jumpers R0-R3 control the receive baud rate and jumpers T0-T3 control the transmit baud rate. In common speed operation, R0-R3 control both baud rates.

The circuit also has provisions for a user-supplied external clock.

Break Logic

A break signal is a continuous spacing condition on the serial data line. If the break bit is set in the XCSR, the module will transmit a break signal to the peripheral device (normally another processor). If the module receives a break signal from the peripheral device (normally a console device), the RBUF control circuitry interprets the absence of stop bits as a framing error. The circuit can be jumpered to ignore the framing error, to place the processor in the halt mode, or to cause the processor to reboot. The break logic asserts BHALT L to halt the processor. It negates BDCOK H to reboot.

Maintenance Mode Logic

The modules can check out their data paths up to (but not including) the peripheral interface circuit by looping the XBUF's serial output back to the RBUF's serial input. Data from the LSI-11 bus still goes to the peripheral device, but no data is received from the peripheral in this maintenance mode. The program can compare received (looped) data with transmitted data to check for errors. The maintenance mode is entered by setting the maintenance bit in the XCSR.

Signal Peripheral Interface

This circuit converts the module's TTL levels to EIA standard levels for modem control. It receives ring, carrier, clear to send, and secondary received data from the data set. It transmits data terminal ready, request to send, force busy, and secondary transmitted data to the data set. (Request to send and force busy are jumper-selectable.) If data set interrupts are enabled, a change in state on any of the received control lines initiates a receiver interrupt. Data is received on the received data line and transmitted on the transmitted data line. Handshake sequences are under program control.

DC-to-DC Power Inverter

The power inverter uses the + 12V from the backplane to produce – 12V for the peripheral interface and data buffer circuitry. It consists of an oscillator, rectifier, inductive charge pump, and a zener regulator.

CONFIGURATION

The following paragraphs describe how the user can configure the module to function within his system. The user can select the register addresses, interrupt vectors, data format, baud rate, and interface mode. The descriptions of the registers and their standard factory addresses are listed in Table 1. The jumpers used on this module consist of wire-wrap pins to which the connections are made; their locations are shown in Figure 2 . A complete listing of the jumpers and a description of their functions are contained in Table 2.

Addresses for the DLV11-E can range from 160000 through 177770_8. The least significant three bits (only bits 1 and 2 are used; bit 0 is ignored) address the desired registers in the module, as described in Table 1. Address bits 3 through 12 are jumper-selected as illustrated in Figure 3.

DLV11-E

Since each module has four registers, each requires four addresses. Addresses 177560—177566 are reserved for the module used with the console peripheral device. Additional modules should be assigned addresses from 175610 through 176176, allowing up to 30 additional DLV11-E modules to be addressed.

Table 1 Standard Assignments

Description	Mnemonic	Console Module	Second Module
Register			
Receiver Control/Status	RCSR	177560	175610
Receiver Data Buffer	RBUF	I77562	175612
Transmit Control/Status	XCSR	177564	175614
Transmit Data Buffer	XBUF	177566	175616
Interrupts			
Receiver		60	300
Transmitter		64	304

DLV11-E

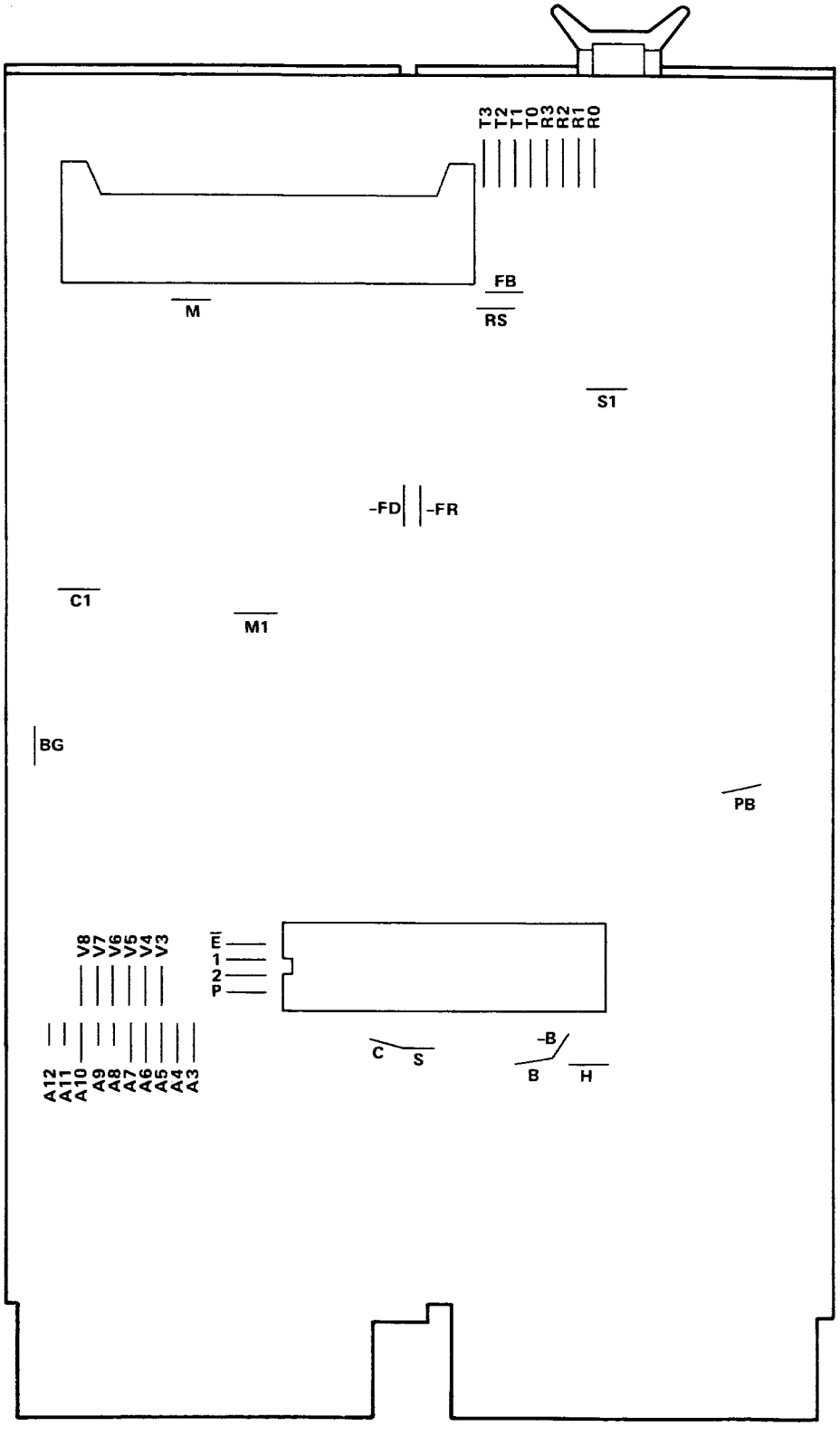


Figure 2 DLV11-E Jumper Locations

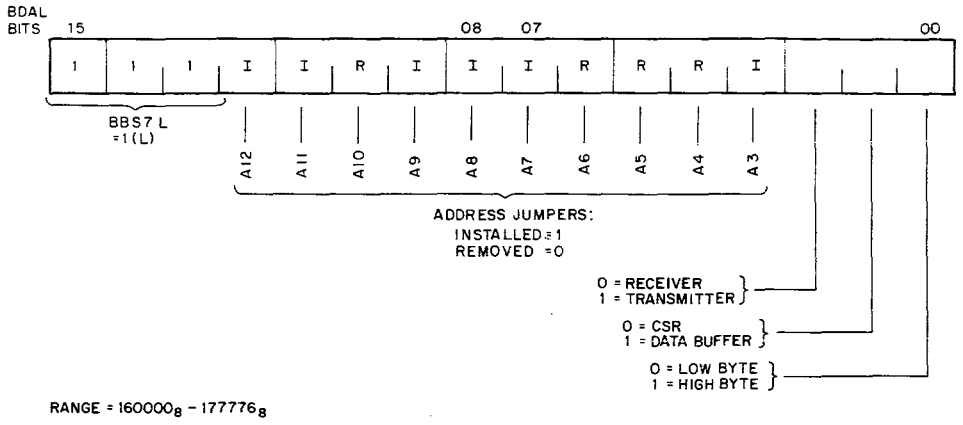


Figure 3 DLV11-E Addressing

Table 2 DLV11-E Jumper Definitions

NOTE

Jumpers are inserted to enable the function they control except for those jumpers which indicate negation (such as "−B" and "E"). Negated jumpers are removed to enable the functions they control.

Jumper	Function
A3-A12	These jumpers correspond to bits 3 through 12 of the address word. When inserted, they will cause the bus interface to check for a true condition on the corresponding address bit.
V3-V8	Used to generate the vector during an interrupt transaction. Each inserted jumper will assert the corresponding vector bit on the LSI-11 bus.
R0-R3	Receiver and transmitter baud rate select jumpers during common speed operation. Receiver-only baud rate select jumpers during split speed operation as defined in Table 3.
T0-T3	Transmitter baud rate select jumpers during split speed operation. Both receiver and transmitter baud rate if maintenance mode is entered during split speed operation as defined in Table 3.

BG	Jumper is inserted to enable break generation.
P	Jumper is inserted for operation with parity.
E	Removed for even parity; inserted for odd parity.
1, 2	These jumpers select the desired number of data bits, as defined in Table 4.
PB	Jumper is inserted to enable the programmable baud rate capability.
C, C1	These jumpers are inserted for common speed operation. (Note that S and S1 must be removed when C and C1 are inserted.)
S, S1	Inserted for split speed operation. (Note that C and C1 must be removed when S and S1 are inserted.)
H	This jumper is inserted to assert BHALT L when a framing error is received, except when the maintenance bit is set. This places the processor in the halt mode.
B, −B	Jumper B is inserted to negate BDCOK H when a break signal or framing error is received, except when the maintenance bit is set. This causes the processor to reboot. (Jumper −B must be removed when B is inserted.)
−FD	Jumper is removed to force data terminal ready signal on.
−FR	Jumper is removed to force request to send signal on.
RS	This jumper is inserted to enable normal transmission of the request to send signal.
FB	Inserted to enable transmission of the force busy signal (for Bell model 103E data sets).
M, M1	These are test jumpers used during the manufacture of the module. They are not defined for field use.

Interrupt Vectors

The interrupt vectors are selected by using jumpers V3 to V8. The standard configuration is shown in Figure 4 and Table 1. The vectors can range from 001 through 774. Note that vectors 60 and 64 are reserved for the console device. Additional DLV11-E modules should be assigned vectors following any DRV11 parallel interface modules installed in the system that start at address 300.

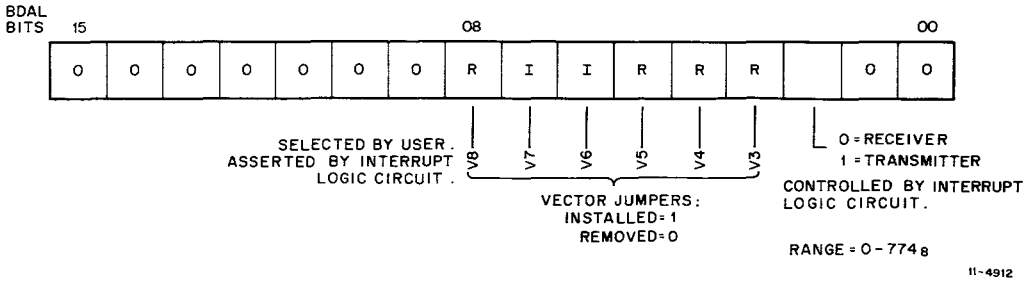


Figure 4 DLV11-E Interrupt Vector

Baud Rate Selection

The DLV11-E allows the user to configure jumpers T0-T3 and R0-R3 for the transmit baud rate and the receiver baud rate as shown in Table 3.

Data Bit Selection

The number of data bits being transmitted or received by the DLV11-E is user-selectable by installing or removing jumpers 1 and 2. The specific number of data bits as controlled by the configuration of jumpers 1 and 2 is shown in Table 4.

Factory Configuration

The user can reconfigure any of the jumpers to make the module meet his requirements. The factory configuration as shipped is shown in Table 5 to help the user determine if any changes are required.

Registers

The word format for the DLV11-E CSR is shown in Figure 5 and its functions are described in Table 6.

Table 3 DLV11-E Baud Rate Selection

Program Control / Receive Jumpers / Transmit Jumpers	Bit 15 / R3 / T3	Bit 14 / R2 / T2	Bit 13 / R1 / T1	Bit 12 / R0 / T0	Bit 11* / Baud Rate
	I	I	I	I	50
	I	I	I	R	75
	I	I	R	I	110
	I	I	R	R	134.5
	I	R	I	I	150
	I	R	I	R	300
	I	R	R	I	600
	I	R	R	R	1200
	R	I	I	I	1800
	R	I	I	R	2000
	R	I	R	I	2400
	R	I	R	R	3600
	R	R	I	I	4800
	R	R	I	R	7200
	R	R	R	I	9600
	R	R	R	R	19200

I = jumper inserted = program bit cleared.

R = jumper removed = program bit set.

* Bit 11 of the XCSR (write-only bit) must be set in order to select a new baud rate under program control. Also, jumper PB must be inserted to enable baud rate selection under program control.

Table 4 DLV11-E Data Bit Selection

Jumpers 2	Jumpers 1	Number of Data Bits
I	I	5
I	R	6
R	I	7
R	R	8

Table 5 DLV11-E Factory Jumper Configuration

Jumper Designation	Jumper State	Function Implemented
A3	I	Jumpers A3 through A12 implement device address 17561X. The least significant octal digit is hardwired on the module to address the four device registers as follows:
A4	R	
A5	R	
A6	R	
A7	I	
A8	I	X = 0 RCSR
A9	I	X = 2 RBUF
A10	R	X = 4 XCSR
A11	I	X = 6 XBUF
A12	I	
V3	R	This jumper selection implements interrupt vector address 300_8 for receiver interrupts and 304_8 for transmitter interrupts.
V4	R	
V5	R	
V6	I	
V7	I	
V8	R	
R0	I	This module is configured to receive at 110 baud.
R1	R	
R2	I	
R3	I	

T0	I	The transmitter is configured for 9600
T1	R	baud if split speed operation is used.
T2	R	
T3	R	
BG	I	Break generation is enabled
P	R	Parity bit is disabled.
E	R	Parity type is not applicable when P is removed
1	R	Operation with eight data bits per char-
2	R	acter
PB	R	Programmable baud rate function disabled.
C	I	Common speed operation enabled.
C1	I	
S	R	Split speed operation disabled.
S1	R	
H	R	Halt on framing error disabled.
B	R	Boot on framing error disabled.
−B	I	
FD	I	The data terminal ready signal is not forced continuously true.
RS	I	The circuitry controlling the request to send signal is enabled.
FB	R	The force busy signal is disabled.
EF	R	Error flags are enabled.
MT	R	Maintenance bit is disabled.
M	R	Factory test jumpers. Not defined for
M1	R	field use.

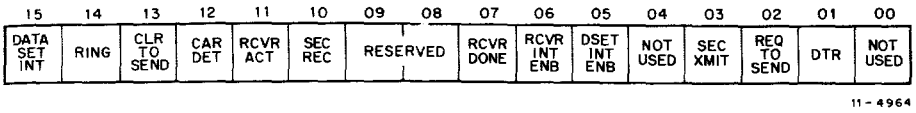


Figure 5 DLV11-E RCSR Register Word Format

Table 6 DLV11-E RCSR Bit Assignments

Bit: 15 **Name:** DATA SET INT
Description: (Data Set Interrupt)
This bit initiates an interrupt sequence provided the DSET INT ENB (bit 5) is also set.

This bit is set whenever CAR DET, CLR TO SEND, or SEC REC changes state, i.e., on a 0 to 1 or 1 to 0 transition of any one of these bits. It is also set when RING changes from 0 to 1.

Cleared by INIT or by reading the RCSR. Because reading the register clears the bit, it is, in effect, a "read-once" bit.

Bit: 14 **Name:** RING
Description: When set, indicates that a ringing signal is being received from the data set. Note that the ringing signal is not a level but an EIA control with a duty cycle of 2 seconds ON and 4 seconds OFF.

Read-only bit.

Bit: 13 **Name:** CLR TO SEND
Description: (Clear to Send)
This state of this bit is dependent on the state of the clear to send signal from the data set. When set, this bit indicates an ON condition; when clear, it indicates an OFF condition.

Read-only bit.

Bit: 12 **Name:** CAR DET
Description: (Carrier Detect)
This bit is set when the data carrier is received. When clear, it indicates either the end of the current transmission activity or an error condition.

Read-only bit.

Bit: 11 **Name:** RCVR ACT
Description: (Receiver Active)
When set, this bit indicates that the DLV11-E's receiver is active. The bit is set at the center of the start bit, which is the beginning of the input serial data from the device, and is cleared by the leading edge of RDONE H.

Read-only bit; cleared by INIT or by RDONE H (bit 7).

Bit: 10 **Name:** SEC REC
Description: (Secondary Received or Supervisory Received Data)
This bit provides a receive capability for the reverse channel of a remote station. A space (+6V) is read as a 1. (A transmit capability is provided by bit 3.)

Read-only bit.

Bit: 9-8 **Name:** Not Used
Description: Reserved for future use.

Bit: 7 **Name:** RCVR DONE
Description: (Receiver Done)
This bit is set when an entire character has been received and is ready for transfer to the processor. When set, initiates an interrupt sequence provided RCVR INT ENB (bit 6) is also set.

Cleared whenever the receiver buffer (RBUF) is addressed. Also cleared by INIT.

Read-only bit.

Bit: 6 **Name:** RCVR INT ENB
Description: (Receiver Interrupt Enable)
When set, allows an interrupt sequence to start when RCVR DONE (bit 7) sets.

Read/write bit; cleared by INIT.
(See Note 1.)

Bit: 5 **Name:** DSET INT ENB
Description: (Data Set Interrupt Enable)
When set, allows an interrupt sequence to start when DATA SET INT (bit 15) sets.

Read/write bit; cleared by INIT.
(See Note 1.)

Bit: 4 **Name:** Not Used
Description: Reserved for future use.

Bit: 3 **Name:** SEC XMIT
Description: (Secondary Transmitted or Supervisory Transmitted Data)
This bit provides a transmit capability for a reverse channel of a remote station. When set, transmits a space (approx. +11.5V). (A receive capability is provided by bit 10.)

Read/write bit; cleared by INIT.

Bit: 2 **Name:** REQ TO SEND
Description: (Request to Send)
A control lead to the data set which is required for transmission. A jumper on the DLV11-E ties this bit to REQ TO SEND or force busy in the data set.

Read/write bit; cleared by INIT.

Bit: 1 **Name:** DTR
Description: (Data Terminal Ready)
A control lead for the data set communication channel. When set, permits connection to the channel. When clear, disconnects the interface from the channel.

Read/write bit; must be cleared by the program; is not cleared by INIT. (See Note 2.)

NOTES

1. When clearing an interrupt enable bit, first set the appropriate processor status bit = 1. After the interrupt enable bit at the module is cleared, the processor may be returned to its normal priority.
2. The state of this bit is not defined after power-up.
3. INIT = LSI-11 bus BINIT signal assertion.

The word format for the DLV11-E RBUF register is shown in Figure 6 and its functions are described in Table 7.

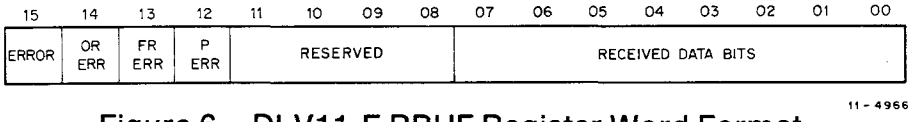


Figure 6 DLV11-E RBUF Register Word Format

Table 7 DLV11-E RBUF Bit Assignments

Bit: 15 **Name:** ERROR
Description: (Error)
Used to indicate that an error condition is present. This bit is the logical OR of OR ERR, FR ERR, and P ERR (bits 14, 13, and 12, respectively). Whenever one of these bits is set, it causes error to set. This bit is not connected to the interrupt logic.

Read-only bit; cleared by removing the error-producing condition.

NOTE

Error indications remain present until the next character is received, at which time the error bits are updated. INIT clears the error bits.

Bit: 14 **Name:** OR ERR
Description: (Overrun Error)
When set, indicates that reading of the previously received character was not completed (RCVR DONE not cleared) prior to receiving a new character.

Read-only bit. Cleared by INIT.

Bit: 13 **Name:** FR ERR
Description: (Framing Error)
When set, indicates that the character that was read had no valid stop bit.

Read-only bit. Cleared by INIT.

Bit: 12 **Name:** P ERR
Description: (Parity Error)
When set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no parity is selected.

Read-only bit. Cleared by INIT.

Bit: 11-8 **Name:** Not Used
Description: Reserved for future use.

Bit: 7-0 **Name:** RECEIVED DATA
Description: Holds the character just read. If less than eight bits are selected, then the buffer is right-justified into the least significant bit positions. In this case, the unused bits are read as 0s.

Read-only bits; not cleared by INIT.

NOTE

INIT = LSI-11 bus BINIT signal assertion.

The word format for the DLV11-E XCSR register is shown in Figure 7 and its functions are described in Table 8.

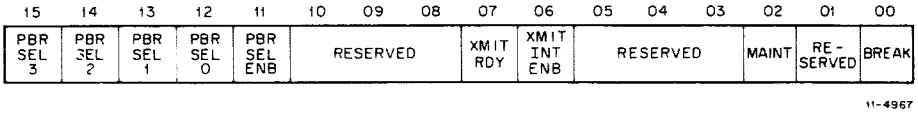


Figure 7 DLV11-E XCSR Register Word Format

Table 8 DLV11-E XCSR Bit Assignments

Bit: 15-12 **Name:** PBR SEL
Description: (Programmable Baud Rate Select)
When set, these bits choose a baud rate from 50-9600 baud.
See Table 3.

Write-only bits.

Bit: 11 **Name:** PBR ENB
Description: (Programmable Baud Rate Enable)
This bit must be set in order to select a new baud rate indicated by bits 12-15.

Write-only bits.

Bit: 10-8 **Name:** Not Used
Description: Reserved for future use.

Bit: 7 **Name:** XMIT RDY
Description: (Transmitter Ready)
This bit is set when the transmitter buffer (XBUF) can accept another character. When set, it initiates an interrupt sequence provided XMIT INT ENB (bit 6) is also set.

Bit: 6 **Name:** XMIT INT ENB
Description: (Transmitter Interrupt Enable)
When set, allows an interrupt sequence to start when XMIT RDY (bit 7) is set.

Read/write bits; cleared by INIT.
(See Note.)

Bit: 5-3 **Name:** Not Used
Description: Reserved for future use.

Bit: 2 **Name:** MAINT
Description: Used for maintenance function. When set, connects the transmitter serial output to the receiver serial input while disconnecting the external device from the receiver serial input. It also forces the receiver to run at transmitter baud rate speed when common speed operation is enabled.

Read/write bit; cleared by INIT.

Bit: 1 **Name:** Not Used.
Description: Reserved for future use.

Bit: 0 **Name:** BREAK
Description: When set, transmits a continuous space to the external device.

Read/write bit; cleared by INIT.

NOTE

When clearing an interrupt enable bit, first set the appropriate processor status word bit = 1. After the interrupt enable bit at the module is cleared, the processor may be returned its normal priority.

The word format for the DLV11-E XBUF register is shown in Figure 8 and its functions are described in Table 9.

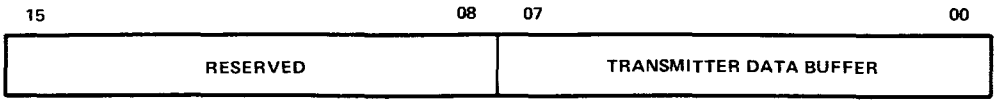


Figure 8 DLV11-E XBUF Register Word Format

Table 9 DLV11-E XBUF Bit Assignments

Bit: 15-8 **Name:** Not Used
Description: Not defined. Not necessarily read as 0s.

Bit: 7-0 **Name:** TRANSMITTER DATA BUFFER
Description: Holds the character to be transferred to the external device. If less than eight bits are used, the character must be loaded so that it is right-justified into the least significant bits.

Write-only bits. Not necessarily read as 0s.

Installation

Prior to installing the DLV11-E on the backplane, first establish the desired priority level to determine the backplane slot in which the module will be installed. Then, check that module configuration jumpers are configured as required for your application. Connection to the peripheral device is via an optional BC05C-X* modem cable for EIA interface applications.

The BC05C cable provides the correct connection to the 40-pin connector on the DLV11-E. The peripheral device end of the cable is terminated with a Cinch DB25P connector that is pin-compatible with Bell 103, 113, 202C, 202D, and 212 modems. Connector pinning and signal levels conform to EIA specification RS-232C. The EIA interface circuit is shown in Figure 9; jumpers are shown in Figure 2.

*X= Length in feet. Standard length is 25 feet.

DLV11-E

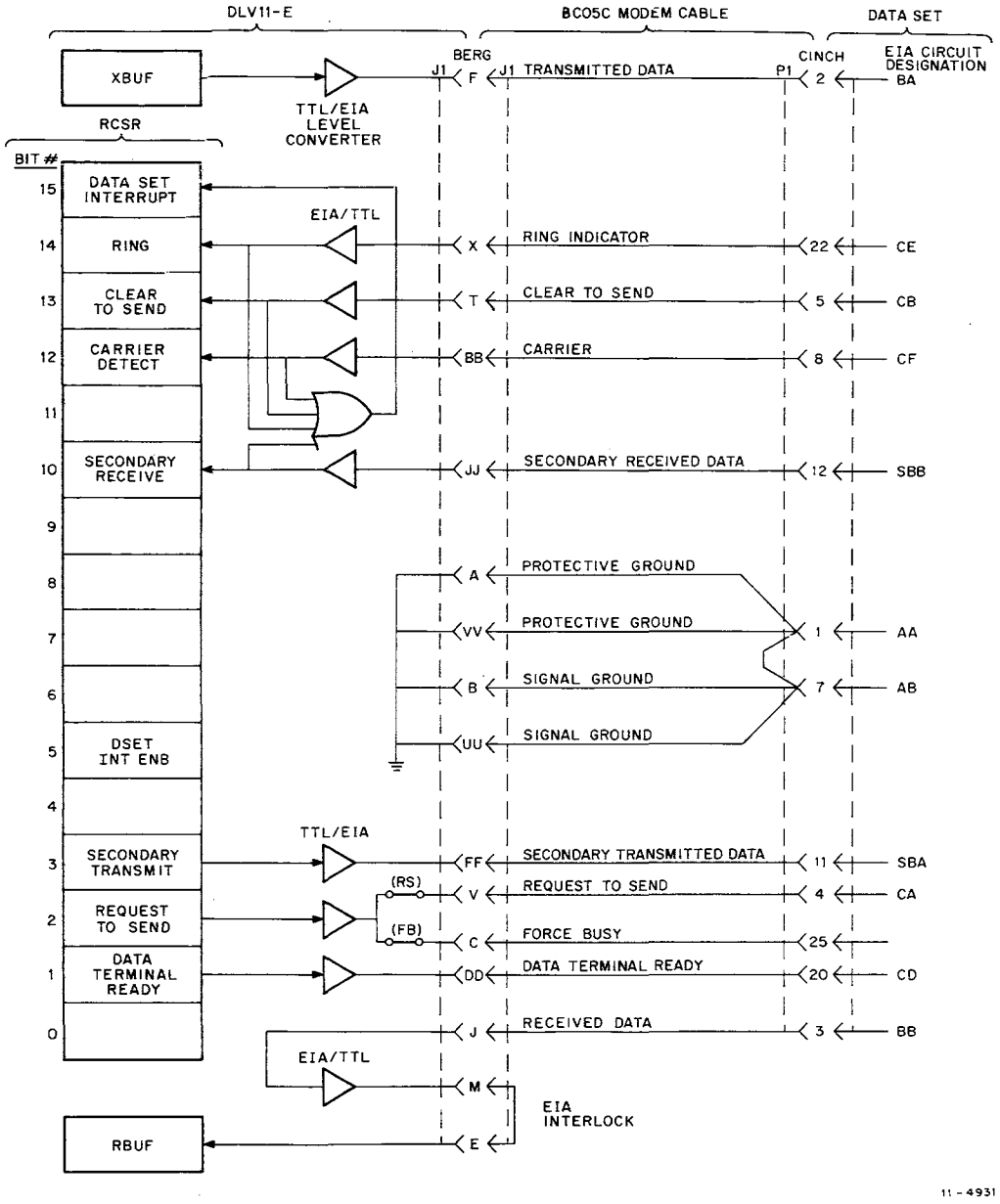


Figure 9 DLV11-E Peripheral Interface Signal Flow

DLV11-F

DLV11-F ASYNCHRONOUS LINE INTERFACE

INTRODUCTION

The DLV11-F asynchronous line interface module interfaces the LSI-11 bus to any of several standard types of serial communications lines. The module receives serial data from peripheral devices, assembles it into parallel data, and transfers it to the LSI-11 bus. It accepts data from the LSI-11 bus, converts it into serial data, and transmits it to the peripheral devices. The DLV11-F supports either 20 mA current loop or EIA-standard lines, but does not include modem control.

FEATURES

- Jumper- or program-selectable, crystal-controlled baud rates: 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, and 19,200. Split transmit and receive baud rates are possible.
- Provisions for user-supplied external clock inputs for baud rate control.
- Jumper-selectable data bit formats.
- LSI-11 bus interface and control logic for interrupt processing and vectored addressing of interrupt service routines.
- Control, status, and data buffer registers directly accessible via processor instructions.
- Support for "data leads only" modem (Bell type 103, 113).
- Generation of reader run signal for use with ASR-type terminals (when equipped with reader run relay).

SPECIFICATIONS

Identification	M8028
Size	Double
Power	+5.0 Vdc ±5% at 1.0 A +12.0 Vdc ±3% at 0.18 A
Bus loads	
AC	2.2
DC	1.0

DESCRIPTION

Major functions of the DLV11-F are shown in Figure 1. Communications between the processor and the DLV11 are executed via programmed I/O operations or interrupt-driven routines.

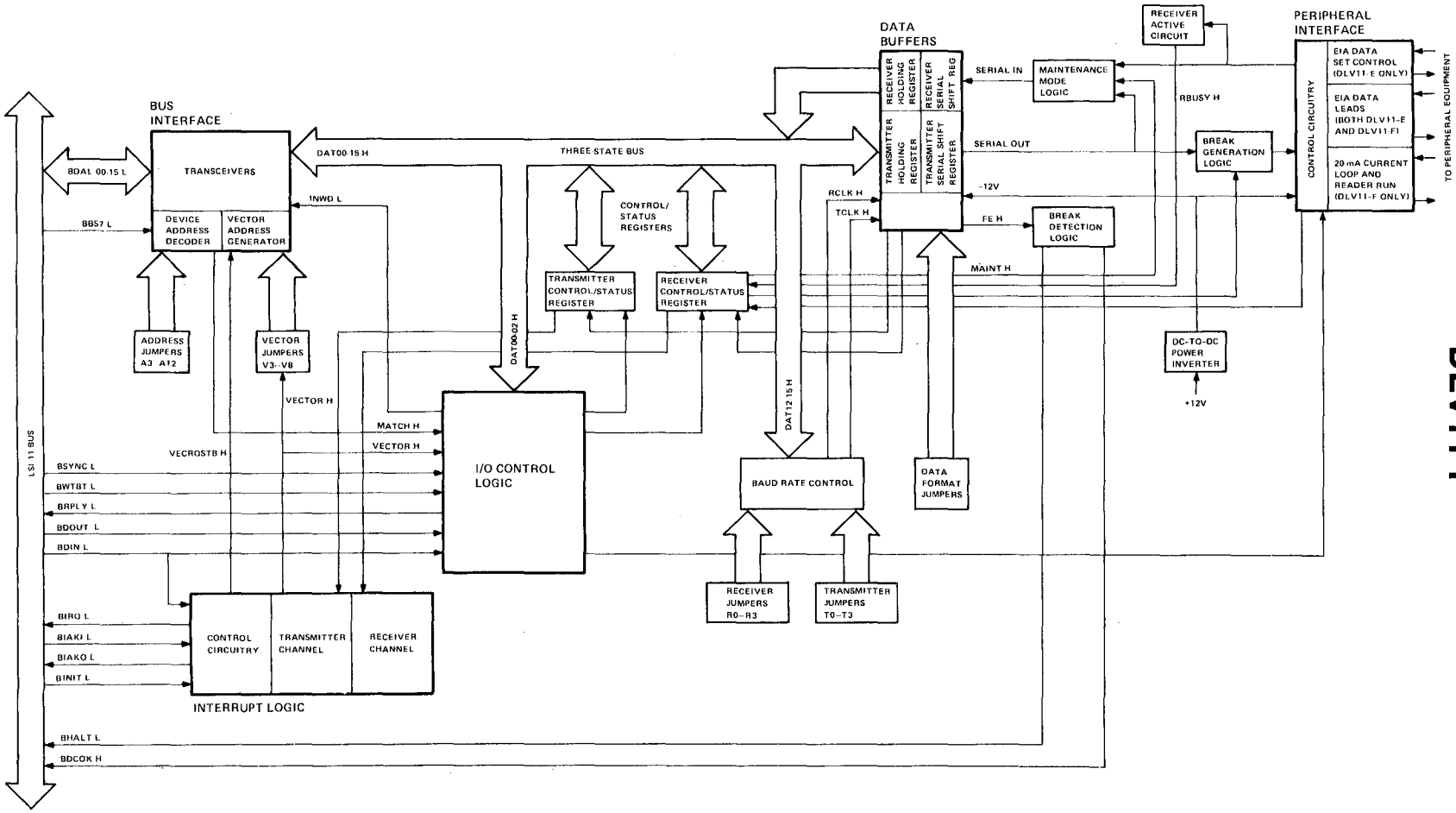


Figure 1 DLV11-F Asynchronous Line Interface Logic Block Diagram

Bus Interface

The bus interface circuit signal levels consist of data moving between the LSI-11 bus and the module's internal tri-state bus. The interface decodes the device address and produces an address match (MATCH H) signal, and places interrupt vectors on the LSI-11 bus. The interface receives from the LSI-11 bus unless it is switched to transmit to the LSI-11 bus. The interrupt logic can cause the bus interface to transmit either a transmitter or a receiver interrupt vector; the I/O control logic can cause the interface to transmit or receive data to or from the LSI-11 bus.

The interface receives LSI-11 bus lines BDAL00 L through BDAL15 L and places them on the module's tri-state bus. If BBS7 L is asserted, the circuit decodes BDAL03 L through BDAL12 L and asserts MATCH H. Jumpers A3-A12 are configured to let the option respond to specific device register addresses. Jumpers V3-V8 select the option's interrupt vector.

I/O Control Logic

When the I/O control logic receives MATCH H from the bus interface, it decodes tri-state bus lines DATO0 H through DATO2 H and selects the addressed device register. The I/O control logic exchanges bus control signals with the processor to perform input and output data transfers. During an interrupt transaction, VECTOR H from the interrupt logic causes the circuit to assert BRPLY L in response to BDIN L. During data transactions, the I/O control logic asserts INWD L to switch the bus interface transceivers from receiving to transmitting.

Control/Status Registers

The receiver control/status register (RCSR) and the transmitter control/status register (XCSR) are enabled by selection signals from the I/O control logic. The CSRs are byte-addressable for reading status bits or writing control bits.

Data Buffers

The receiver buffer (RBUF) and transmitter buffer (XBUF) provide double-buffering in that one byte of data can be held while another byte is entering or exiting. This allows asynchronous, full-duplex operation. Data is handled in the low byte of the registers. The buffer control circuitry places receiver buffer error flag bits in the high byte of the RBUF. If also sends a status bit to the RCSR and a framing error bit (FE H) to the break logic.

Receiver Active Circuit

This circuit monitors the received serial data line and sets a status bit (RCVR ACT) as soon as the RBUF begins receiving data. It clears the bit when a full character of data has been received.

Interrupt Logic

The DLV11-F can generate transmitter interrupts. If the XBUF is ready to serialize another character of data and the transmitter interrupt enable bit is set in the XCSR, the interrupt logic requests to interrupt the processor (by asserting BIRQ L). If the processor acknowledges via the BIAKI/BIAKO daisy-chain, the interrupt logic asserts VECTOR H and VECRQSTB H. These signals cause the bus interface to place the transmitter function interrupt vector address on the LSI-11 bus.

The module also can request a receiver interrupt if the RBUF has received a character and the receiver interrupt bit is set in the RCSR. When the interrupt request is acknowledged, the interrupt logic asserts VECTOR H. VECTOR H causes the bus interface circuit to place the receiver function interrupt vector address on the LSI-11 bus. (VECRQSTB H is used only for a transmitter interrupt.)

The interrupt acknowledge daisy-chain (BIAKI/BIAKO) passes through both the receiver and transmitter sections of the interrupt logic. It goes through the receiver section first, thereby giving the receiver channel priority over the transmitter channel.

Baud Rate Control

The baud rate control establishes the speed at which the data buffers handle serial data. It produces clock signals by dividing a crystal oscillator frequency by an amount selected by jumpers or by the program. The circuit can be jumpered to generate either independent transmitter and receiver clocks (split speed operation) or a common clock (common speed operation).

When the programmable baud rate enable bit is set in the XCSR, the baud rate control decodes tri-state bus lines DAT12 H through DAT15 H. These bits control the receive baud rate in split speed operation and both transmit and receive baud rate in common speed operation. When programmable baud rate is not enabled, the baud rates are controlled by jumpers. In split speed operation, jumpers R0-R3 control the receive baud rate and jumpers T0-T3 control the transmit baud rate. In common speed operation, R0-R3 control both baud rates.

The circuit has provisions for a user-supplied external clock.

Break Logic

A break signal is a continuous spacing condition on the serial data line. If the break bit is set in the XCSR, the module will transmit a break signal to the peripheral device (normally another processor). If the module receives a break signal from the peripheral device (normally a console device), the RBUF control circuitry interprets the absence of stop bits as a framing error. The circuit can be jumpered to ignore the framing error, to place the processor in the halt mode, or to cause the processor to reboot. The break logic asserts BHALT L to halt the processor. It negates BDCOK H to reboot.

Maintenance Mode Logic

The modules can check out their data paths up to (but not including) the peripheral interface circuit by looping the XBUF's serial output back to the RBUF's serial input. Data from the LSI-11 bus still goes to the peripheral device, but no data is received from the peripheral in this maintenance mode. The program can compare received (looped) data with transmitted data to check for errors. The maintenance mode is entered by setting the maintenance bit in the XCSR.

Peripheral Interface

This circuit can be jumpered to support either EIA-level data leads (no modem control) or 20 mA current loop modes. When interfacing EIA-level data leads ("data leads only" operation), request to send, force busy, and data terminal ready are continuously true by separate EIA drivers. No modem control signals are received.

In the current loop mode of operation, the circuit uses optical isolators to interface TTL to 20 mA current loops. This operation is jumper-selectable for either active or passive operation of the transmitter and receiver circuitry.

The peripheral interface also produces a reader run current to advance the paper tape reader on a peripheral equipped with a reader run relay. This is controlled by the reader enable bit in the DLV11-F's RCSR.

DC-to-DC Power Inverter

The power inverter uses the +12V from the backplane to produce −12V for the peripheral interface and data buffer circuitry. It consists of an oscillator, rectifier, inductive charge pump, and a zener regulator.

DLV11-F

CONFIGURATION

The following paragraphs describe how the user can configure the module to function within his system. The user can select the register addresses, interrupt vectors, data format, baud rate, and interface mode. The registers and their standard factory addresses are listed in Table 1. The jumpers used on this module consist of wire-wrap pins to which the connections are made; their locations are shown in Figure 2. A complete listing of the jumpers and a description of their functions are listed in Table 2.

Addresses

Addresses for the DLV11-F can range from 160000_8 through 177770_8. The least significant three bits (only bits 1 and 2 are used; bit 0 is ignored) address the desired registers in the module, as shown in Table 1. Address bits 3 through 12 are jumper-selected as shown in Figure 3.

Since each module has four registers, each requires four addresses. Addresses 177560—177566 are reserved for the module used with the console peripheral device. Additional modules should be assigned addresses from 176500 through 176670, allowing up to 30 additional DLV11-F modules to be addressed.

Interrupt Vectors

The interrupt vectors are selected by using jumpers V3 to V8. The standard configuration is shown in Figure 4 and Table 1. The vectors can range from 001 through 774_8. Note that vectors 60_8 and 64_8 are reserved for the console device. Additional DLV11-F modules should be assigned vectors following any DRV11 peripheral interface module installed in the system that starts at address 300_8.

Table 1 Standard Assignments

Description	Mnemonic	Console Module	Second Module
Register			
Receiver Control/Status	RCSR	177560	176500
Receiver Data Buffer	RBUF	177562	176502
Transmit Control/Status	XCSR	177564	176504
Transmit Data Buffer	XBUF	177566	176506
Interrupts			
Receiver		60	300
Transmitter		64	304

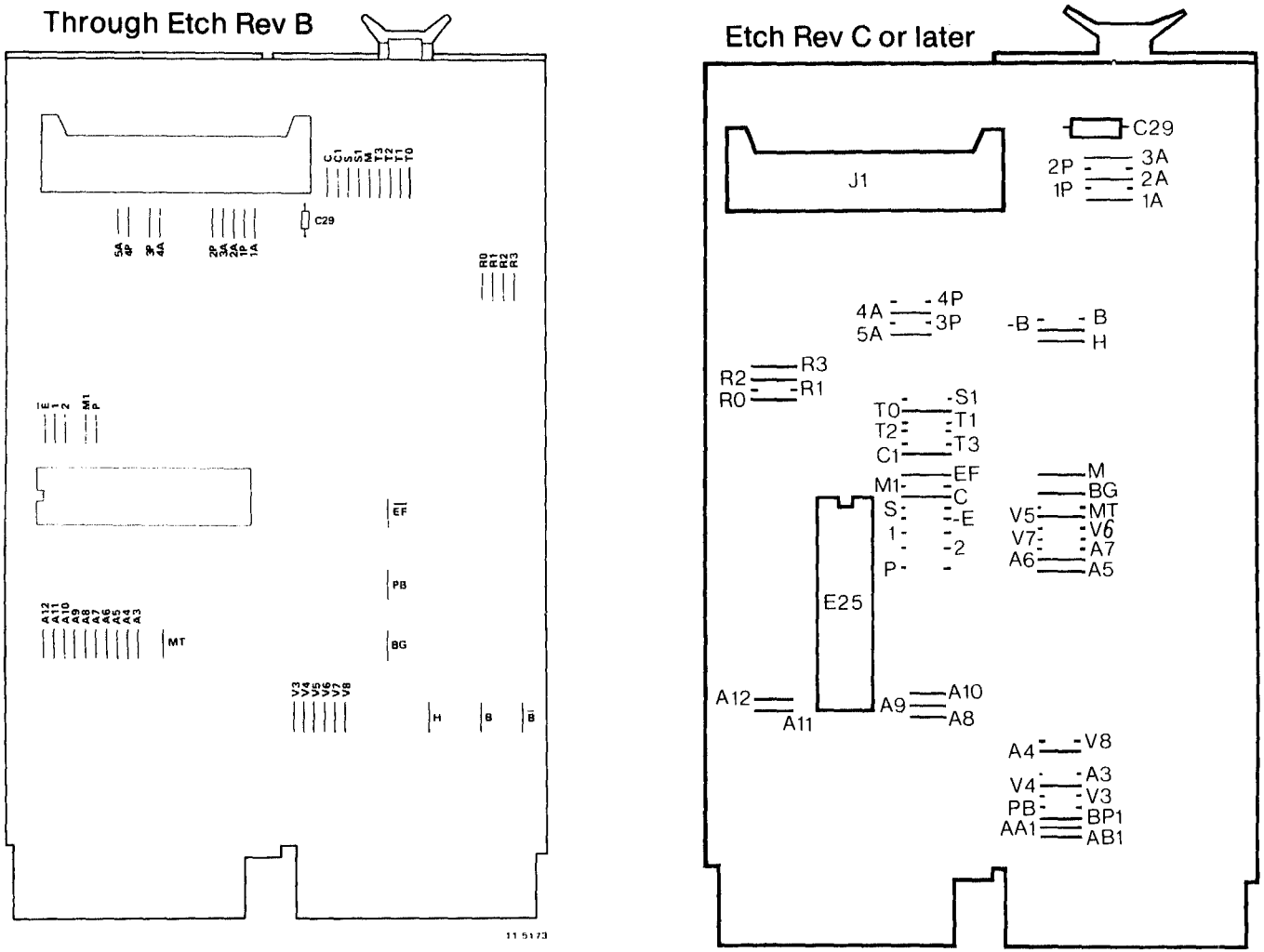


Figure 2 DLV11-F Jumper Locations

DLV11-F

Table 2 DLV11-F Jumper Definitions

NOTE

Jumpers are inserted to enable the function they control except for those jumpers which indicate negation (such as "−B" and "E"). Negated jumpers are removed to enable the functions they control.

Jumper	Function
A3-A12	These jumpers correspond to bits 3 through 12 of the address word. When inserted, they cause the bus interface to check for a true condition on the corresponding address bit.
V3-V8	Used to generate the vector during an interrupt transaction. Each inserted jumper asserts the corresponding vector bit on the LSI-11 bus.
R0-R3	Receiver and transmitter baud rate select jumpers during common speed operation. Receiver-only baud rate select jumpers during split speed operation, as defined in Table 3.
T0-T3	Transmitter baud rate select jumpers during split speed operation. Both receiver and transmitter baud rate if maintenance mode is entered during split speed operation, as defined in Table 3.
BG	Jumper is inserted to enable break generation.
P	Jumper is inserted for operation with parity.
E	Receiver checks for appropriate parity and transmitter inserts appropriate parity.
1, 2	These jumpers select the desired number of data bits, as defined in Table 4.
PB	Jumper is inserted to enable the programmable baud rate capability.
C, C1	These jumpers are inserted for common speed operation. (Note that S and S1 must be removed when C and C1 are inserted.)

S, S1	Inserted for split speed operation. (Note that C and C1 must be removed when S and S1 are inserted.)
H	This jumper is inserted to assert BHALT L when a framing error is received, except when the maintenance bit is set. This places the processor in the halt mode.
B, −B	Jumper B is inserted to negate BDCOK H when a break signal or framing error is received, except when the maintenance bit is set. This causes the processor to reboot. (Jumper −B must be removed when B is inserted.)
1A, 2A, 3A	These three jumpers are inserted to make the 20 mA current loop receiver active. (Jumpers 1P and 2P must be removed when 1A, 2A, and 3A are inserted.)
1P, 2P	These jumpers are inserted to make the 20 mA current loop receiver passive. (Jumpers 1A, 2A, and 3A must be removed when 1P and 2P are installed.)
4A, 5A	Inserted to make the 20 mA current loop transmitter active. (Jumpers 3P and 4P must be removed when 4A and 5A are inserted.)
3P, 4P	Inserted to make the 20 mA current loop transmitter passive. (Jumpers 4A and 5A must be removed when 3P and 4P are inserted.)
EF	Jumper is removed to enable the error flags to be read in the high byte of the receiver buffer.
M, M1	These are test jumpers used during the manufacture of the module. They are not defined for field use.

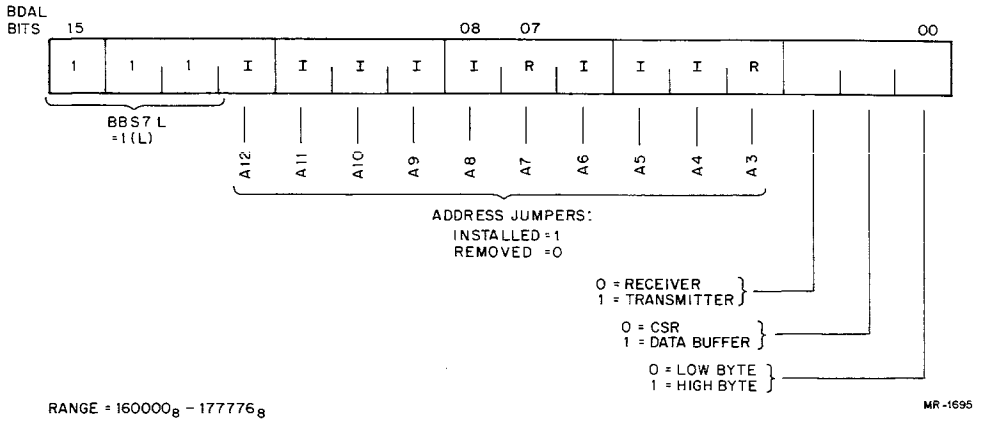


Figure 3 DLV11-F Addressing

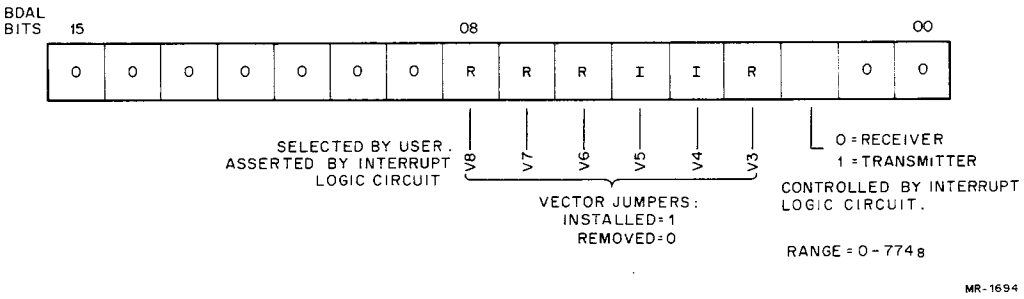


Figure 4 DLV11-F Interrupt Vectors

Baud Rate Selection

The DLV11-F allows the user to configure jumpers T0-T3 and R0-R3 for the transmit baud rate and the receiver baud rate as shown in Table 3.

Data Bit Selection

The number of data bits transmitted or received by the DLV11-F is user-selectable by installing or removing jumpers 1 and 2. The specific number of data bits as controlled by the configuration of jumpers 1 and 2 is shown in Table 4.

Table 3 DLV11-F Baud Rate Selection

Program Control Receive Jumpers Transmit Jumpers	Bit 15 R3 T3	Bit 14 R2 T2	Bit 13 R1 T1	Bit 12 R0 T0	Bit 11* Baud Rate
	I	I	I	I	50
	I	I	I	R	75
	I	I	R	I	110**
	I	I	R	R	134.5
	I	R	I	I	150
	I	R	I	R	300
	I	R	R	I	600
	I	R	R	R	1200
	R	I	I	I	1800
	R	I	I	R	2000
	R	I	R	I	2400
	R	I	R	R	3600
	R	R	I	I	4800
	R	R	I	R	7200
	R	R	R	I	9600
	R	R	R	R	19200

I = Jumper inserted = program bit cleared
R = Jumper removed = program bit set

* Bit 11 of the XCSR (write-only bit) must be set in order to select a new baud rate under program control. Also, jumper PB must be inserted to enable baud rate selection under program control.

** When configured for 110 baud, the UART is set for two stop bits.

Table 4 DLV11-F Data Bit Selection

Jumpers		Number of Data Bits
2	1	
I	I	5
I	R	6
R	I	7
R	R	8

Factory Configuration

The user can reconfigure any of the jumpers to make the module meet his requirements. The factory configuration, as shipped, is shown in Table 5 to assist the user in determining what changes are needed.

Table 5 DLV11-F Factory Jumper Configuration

Jumper Designation	Jumper State	Function Implemented
A3	R	Jumpers A3 through A12 implement device address 17756X. The least significant octal digit is hardwired on the module to address the four device registers as follows: X = 0 RCSR 0 X = 2 RBUF 2 X = 4 XCSR 4 X = 6 XBUF
A4	I	
A5	I	
A6	I	
A7	R	
A8	I	
A9	I	
A10	I	
A11	I	
A12	I	
V3	R	This jumper selection implements interrupt vector 60_8 for receiver interrupts and 64_8 for transmitter interrupts.
V4	I	
V5	I	
V6	R	
V7	R	
V8	R	
R0	I	The module is configured to receive at 110-baud.
R1	R	
R2	I	
R3	I	
T0	I	The transmitter is configured for 9600 baud if split speed operation is used.
T1	R	
T2	R	
T3	R	
BG	I	Break generation is enabled.

P	R	Parity bit is disabled.
E	R	Parity type is not applicable when P is removed.
1 2	R R	Operation with eight data bits per character.
PB	R	Programmable baud rate function disabled.
C C1	I I	Common speed operation enabled.
S S1	R R	Split speed operation disabled.
H	I	Halt on framing error enabled.
B −B	R I	Boot on framing error disabled.
1A 2A 3A 1P 2P	I I I R R	The 20 mA current loop receiver is configured as an active receiver.
4A 5A 3P 4P	I I R R	The 20 mA current loop transmitter is configured for active operation.
EF	I	Error flags are disabled.
MT	R	Maintenance bit disabled.
M M1	I I	Factory test jumpers. Not defined for field use.

Registers

The word format for the DLV11-F RCSR is shown in Figure 5 and functionally described in Table 6.

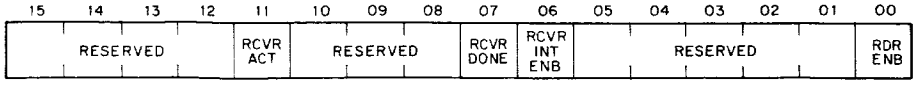


Figure 5 DLV11-F RCSR Word Format

Table 6 DLV11-F RCSR Bit Assignments

Bit: 15-12 **Name:** Not used
Description: Reserved for future use.

Bit: 11 **Name:** RCVR ACT
Description: (Receiver Active)
When set, this bit indicates that the DLV11-F interface receiver is active. The bit is set at the center of the start bit, which is the beginning of the input serial data from the device and is cleared by the leading edge of RDONE H.

Read-only bit; cleared by INIT or by RCVR DONE (bit 7).

Bit: 10-8 **Name:** Not used
Description: Reserved for future use.

Bit: 7 **Name:** RCVR DONE
Description: (Receiver Done)
This bit is set when an entire character has been received and is ready for transfer to the processor. When set, initiates an interrupt sequence provided RCVR INT ENB (bit 6) is also set.

Read-only bit.

Bit: 6 **Name:** RCVR INT ENB
Description: (Receiver Interrupt Enable)
When set, allows an interrupt sequence to start when RCVR DONE (bit 7) sets.

Read/write bit; cleared by INIT.

Bit: 5-1 **Name:** Not used
Description: Reserved for future use.

Bit: 0 **Name:** RDR ENB
Description: (Reader Enable)
When set, this bit advances the paper tape reader in DIGITAL-modified TTY units (LT33-C, LT35-A, C) and clears the RCVR DONE bit (bit 7).

This bit is cleared at the middle of the start bit, which is the beginning of the serial input from an external device. Also cleared by INIT.

Write-only bit.

NOTE

INIT = LSI-11 bus BINIT signal assertion.

The word format for the DLV11-F RBUF register is shown in Figure 6 and functionally described in Table 7.

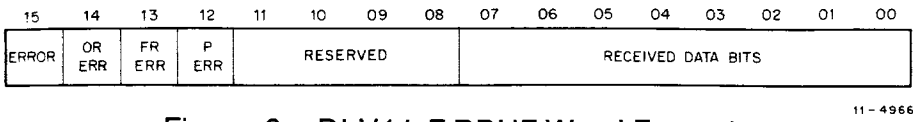


Figure 6 DLV11-F RBUF Word Format

Table 7 DLV11-F RBUF Bit Assignments

Bit: 15 **Name:** ERROR
Description: Used to indicate that an error condition is present. This bit is the logical OR of OR ERR, FR ERR, and P ERR (bits 14, 13, and 12, respectively). Whenever one of these bits is set, it causes bit 15 to set. This bit is not connected to the interrupt logic.

Read-only bit; cleared by removing the error-producing condition.

NOTE

Error indications remain present until the next character is received, at which time the error bits are updated. INIT clears the error bits.

Bit: 14 **Name:** OR ERR
Description: (Overrun Error)
When set, indicates that reading of the previously received character was not completed (RCVR DONE not cleared) prior to receiving a new character.

Read-only bit. Cleared by INIT.

Bit: 13 **Name:** FR ERR
Description: (Framing Error)
When set, indicates that the character that was read had no valid stop bit.

Read-only bit. Cleared by INIT.

Bit: 12 **Name:** P ERR
Description: (Parity Error)
When set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no parity is selected.

Read-only bit. Cleared by INIT.

Bit: 11-8 **Name:** Not used
Description: Reserved for future use.

Bit: 7-0 **Name:** RECEIVED DATA BITS
Description: Holds the character just read. If less than eight bits are

selected, then the buffer is right-justified into the least significant bit positions. In this case, the higher unused bit or bits are read as 0s.

Read-only bits; not cleared by INIT.

NOTE

INIT = LSI-11 bus BINIT signal assertion.

The word format for the DLV11-F XCSR register is shown in Figure 7 and functionally described in Table 8.

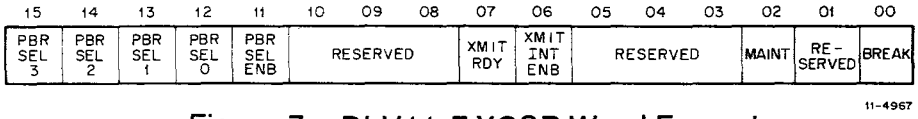


Figure 7 DLV11-F XCSR Word Format

Table 8 DLV11-F XCSR Bit Assignments

Bit: 15-12 **Name:** PBR SEL
Description: (Programmable Baud Rate Enable)
When set, these bits choose a baud rate from 50-9600 baud. See Table 3.

Write-only bits.

Bit: 11 **Name:** PBR ENB
Description: (Programmable Baud Rate Enable)
This bit must be set in order to select a new baud rate indicated by bits 12 to 15.

Write-only bits.

Bit: 10-8 **Name:** Not used
Description: Reserved for future use.

Bit: 7 **Name:** XMIT RDY
Description: (Transmitter Ready)
This bit is set when the transmitter buffer (XBUF) can accept another character. When set, it initiates an interrupt sequence provided XMIT INT ENB (bit 6) is also set.

Bit: 6 **Name:** XMIT INT ENB
Description: (Transmitter Interrupt Enable)
When set, allows an interrupt sequence to start when XMIT RDY (bit 7) is set.

Read/write bit; cleared by INIT. (See Note.)

Bit: 5-3 **Name:** Not used
Description: Reserved for future use.

Bit: 2 **Name:** MAINT
Description: Used for maintenance function. When set, connects the transmitter serial output to the receiver serial input while disconnecting the external device from the receiver serial input. It also forces the receiver to run at transmitter baud rate speed when common speed operation is enabled.

Read/write bit; cleared by INIT.

Bit: 1 **Name:** Not used
Description: Reserved for future use.

Bit: 0 **Name:** BREAK
Description: When set, transmits a continuous space to the external device.

Read/write bit; cleared by INIT.

NOTE

When clearing an interrupt enable bit, first set the appropriate processor status word bit = 1. After the interrupt enable bit at the module is cleared, the processor may be returned to its normal priority.

The word format for the DLV11-F XBUF register is shown in Figure 8 and functionally described in Table 9.

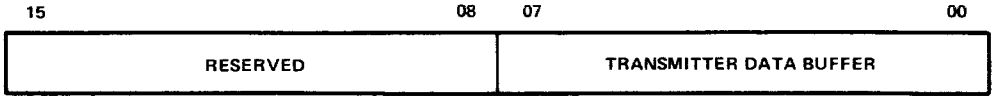


Figure 8 DLV11-F XBUF Word Format

Table 9 DLV11-F XBUF Bit Assignments

Bit: 15-8 **Name:** Not Used
Description: Not defined. Not necessarily read as 0s.

Bit: 7-0 **Name:** TRANSMITTER DATA BUFFER
Description: Holds the character to be transferred to the external device. If fewer than eight bits are used, the character must be loaded so it is right-justified into the least significant bits.

Write-only bits. Not necessarily read as 0s.

DLV11-F

Installation

Before installing the DLV11-F on the backplane, first establish the desired priority level to determine in which backplane slot to install the module. Then ensure that the module configuration jumpers are configured correctly for your application. Connection to the peripheral device is via an optional data interface cable. Cables are listed below.

Application	Cable Type*
EIA Interface	BC01V-X or BC05C-X Modem Cable
20 mA Current Loop	BC05M-X Cable Assembly

Interfacing EIA-Compatible Devices

The DLV11-F supports only the data leads of EIA-compatible devices. It uses a BC05C modem cable to interface devices such as the Teletype® Model 37 Teletypewriter and the Bell Data Set Model 103 (in auto mode). The DLV11-F's EIA "data leads only" interface circuit is shown in Figure 9 and the jumpers are shown in Table 5.

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* X = Length in feet. Standard length is 25 feet.

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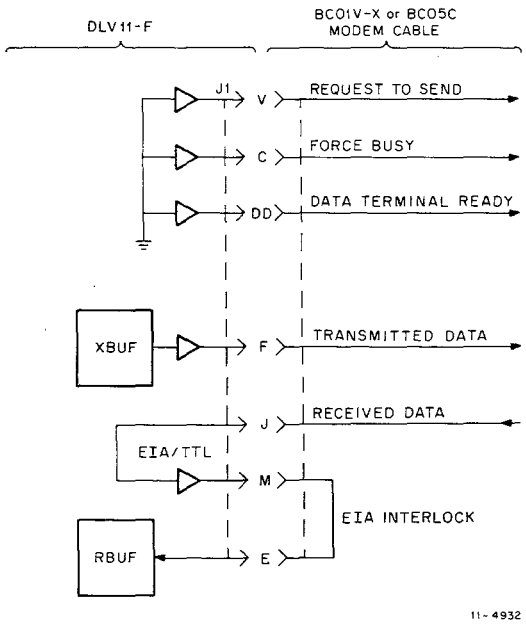


Figure 9 EIA Data Leads Only Interface

Interfacing 20 mA Current Loop Devices with the DLV11-F

When interfacing with 20 mA current loop devices, the BC05M cable assembly provides the correct connections to the 40-pin connector on the DLV11-F. The peripheral device end of the cable is terminated with

a Mate-N-Lok connector that is pin-compatible with all DIGITAL 20 mA serial interface terminals.

The interface circuits provided by the BC05M cable and the associated DLV11-F jumpers are shown in Figures 9, 10, 11, and 12.

NOTE

When the DLV11-F is used with teletypewriter devices, a 0.005μF capacitor must be installed (see Figure 1).

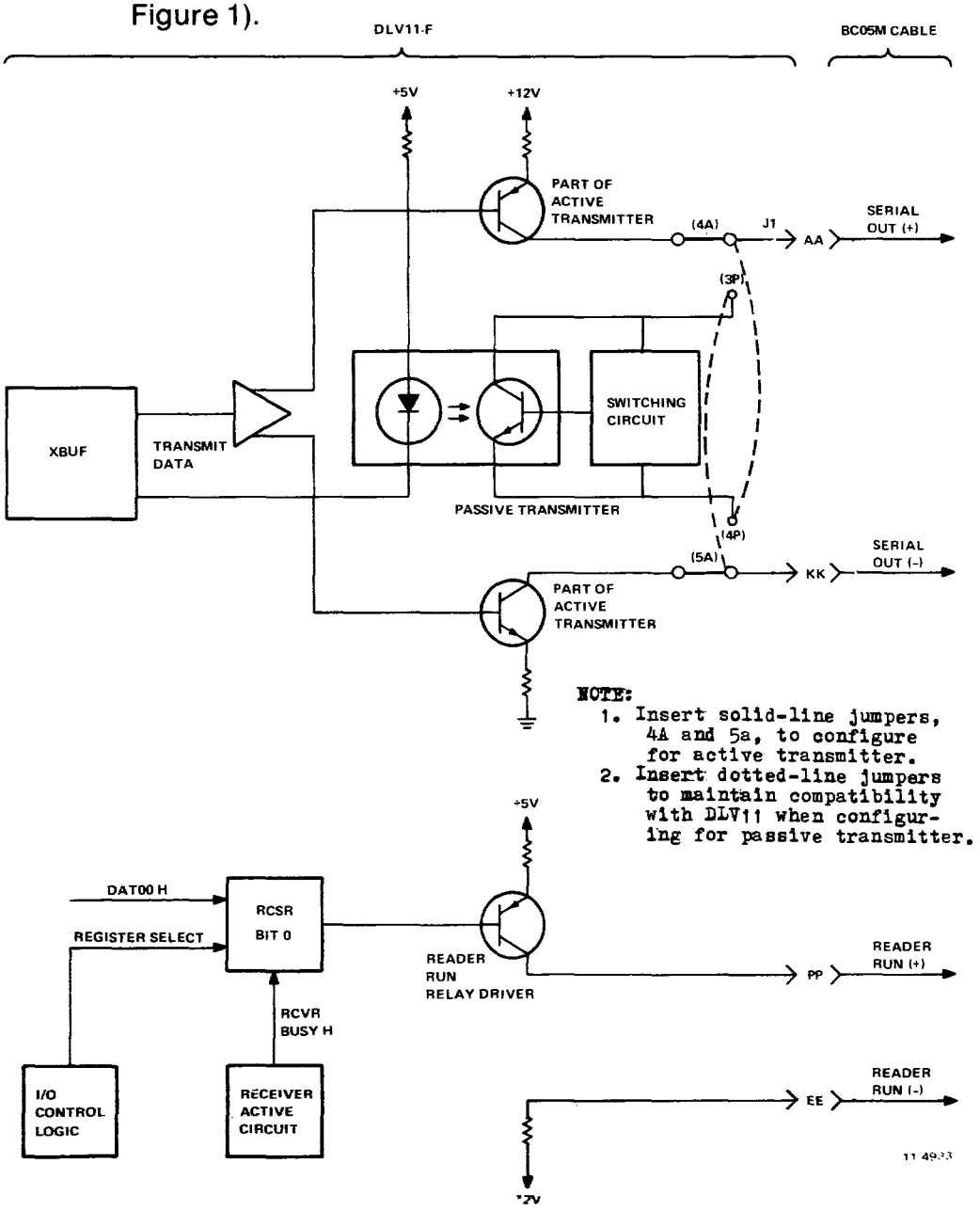


Figure 10 20 mA Transmitter and Reader Run Circuits

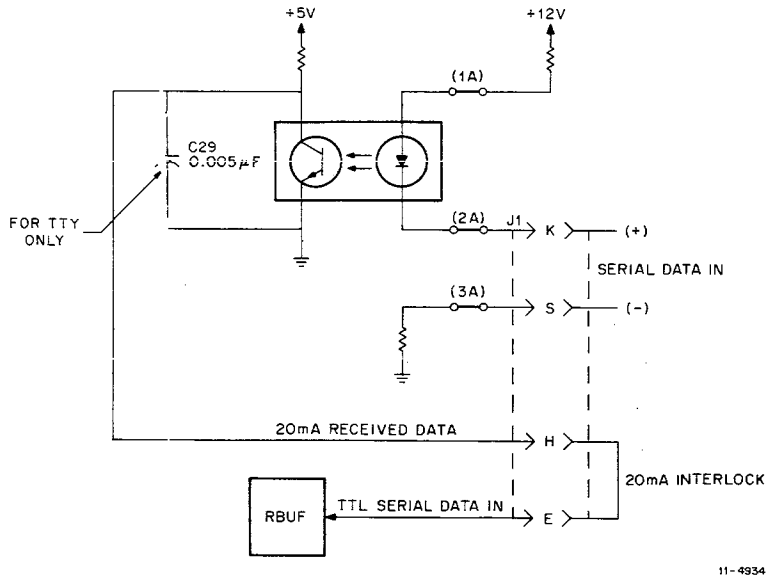


Figure 11 Active Receive 20 mA Current Loop

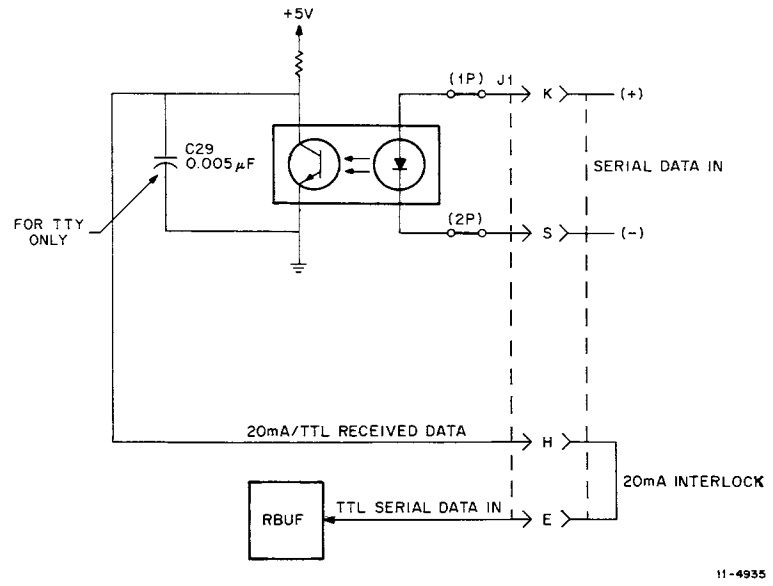


Figure 12 Passive Receive 20 mA Current Loop

DLV11-J FOUR-CHANNEL ASYNCHRONOUS SERIAL INTERFACE

INTRODUCTION

The DLV11-J is a 4-channel asynchronous serial line unit used to interface peripheral equipment to an LSI-11 bus. The interface transmits and receives data from the peripheral device over Electronics Industry Association (EIA) "data leads only" lines which do not use control lines. The module can be used with 20 mA current loop devices (with "reader-run" capabilities) when the DLV11-KA option is installed. With a DLV11-J interface, the processor can communicate with a local terminal such as a console teleprinter, a remote terminal via data sets and private line, or another local or remote processor.

FEATURES

- Four independent, full-duplex, asynchronous serial line interfaces to the LSI-11 bus on one double-height module.
- Each channel independently configured for:
  1. EIA RS-232C, RS-422, RS-423
  2. Baud Rates: 150, 300, 600, 1200, 2400, 4800, 9600, 19.2K, 38.4K and external
  3. Variable character format:
     7 or 8 data bits;
     1 or 2 stop bits;
     odd, even,or no parity
  4. Support for data leads only: MODEMS (Bell type: 103, 113)
- One channel configurable as computer console device interface, including halt or boot on received break.
- 8.9 in × 5.2 in (22.8cm × 13.2cm) module
- 20 mA current loop and 110 baud capability optionally added using the EIA to 20 mA converter (DLV11-KA).
- The DLV11-KA provides:
  1. Single line EIA to 20 mA converter unit and 3 ft. (.91m) cable for connection to DLV11-J.
  2. A program-controlled, reader advance function for DIGITAL-modified ASR33 teletypes.
  3. A 110 baud rate generator.
  4. Choice of active or passive operation.
  5. Operation up to 9600 baud.
  6. Cable drive capability up to 4000 feet.

DLV11-J

SPECIFICATIONS

Identification	M8043
Size	Double
Power	+5 V ±5% at 1.0 A +12 V ±3% at 0.25 A
Bus Loading	
AC	1
DC	1

DESCRIPTION

The DLV11-J module is designed to interface peripheral devices that transmit and receive asynchronous serial data over EIA-compatible data lines or 20 mA current loops to the parallel LSI-11 bus. When configured, the module transmits and receives the specified EIA signal levels on the receive and transmit data lines of the cable. Also, the module constantly asserts the data-terminal-ready signal.

When configured for 20 mA current loop operation (DLV11-KA option installed), the DLV11-J can support devices which contain program-controlled paper tape readers (such as DIGITAL's LT33 Teletypewriters or the ASR33 Teletypewriter with the LT33 modification kit.)

During operation, the module is required to convert data from parallel to serial and serial to parallel. To accomplish this, a universal asynchronous receiver/transmitter (UART) is employed. When performing this conversion, the UART must also alter the speed and character format for the data (to meet user-selected parameters). In addition, the UART creates error bits to allow the programmer to check data transmission for errors. A block diagram of the DLV11-J module is shown in Figure 1.

UART Operation

The DLV11-J module is equipped with four universal asynchronous receiver/transmitters, one for each channel. The UART chip is capable of parallel data transfers with the computer and serial data transfers with the peripheral device. User-selectable jumpers determine the character format used during transmission. The jumpers select:

7 or 8 data bits
1 or 2 stop bits
Parity or no parity
Even or odd parity

The receiver section performs serial-to-parallel conversion of data which will always appear right-justified in the receive data buffer. The start, stop, and parity bits are removed and error flags appended to the transmission as it enters the receive buffer. The error flags, when set, will not interrupt operation, but they are available to the programmer when reading the RBUF.

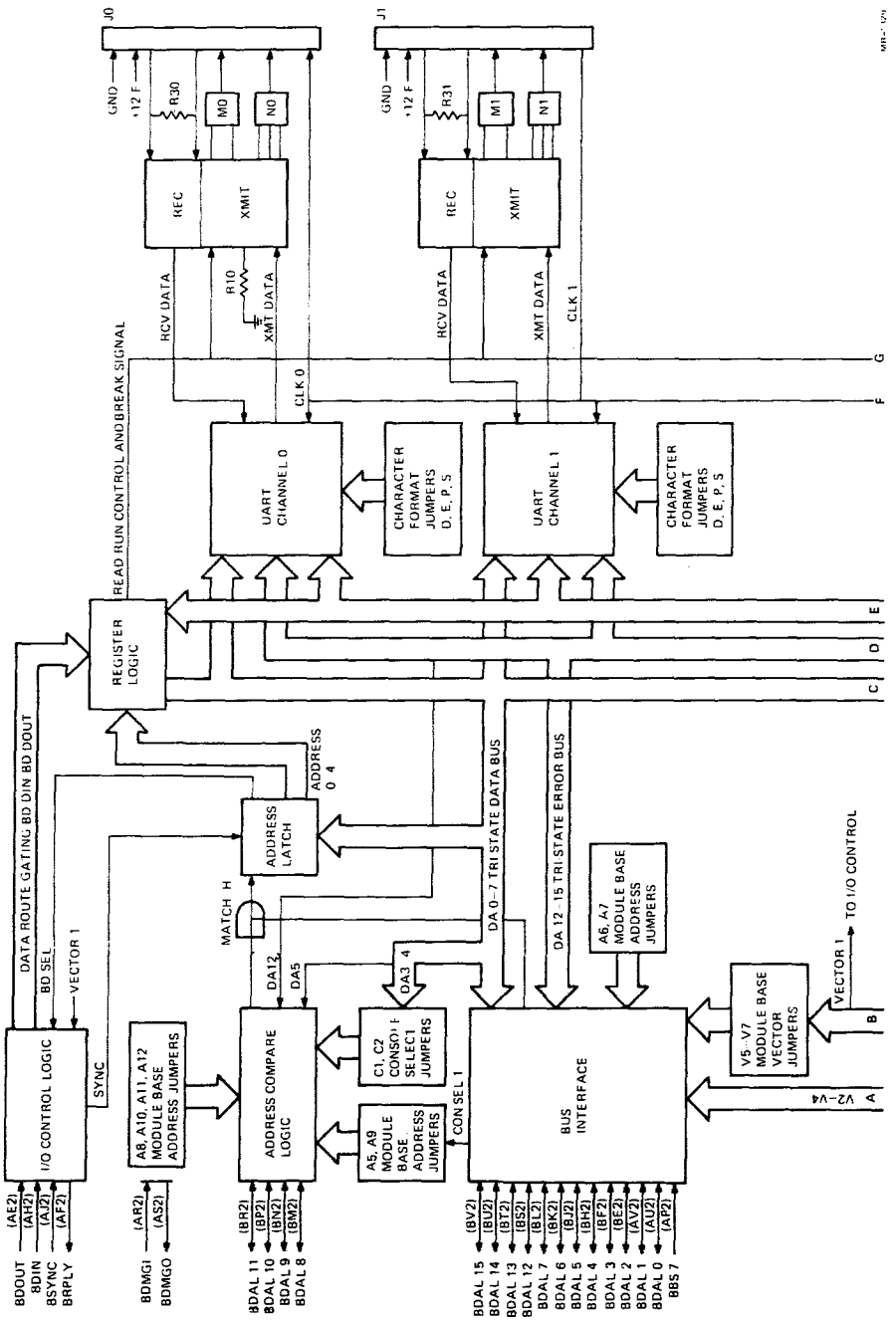


Figure 1 DLV11-J Block Diagram (Sheet 1 of 2)

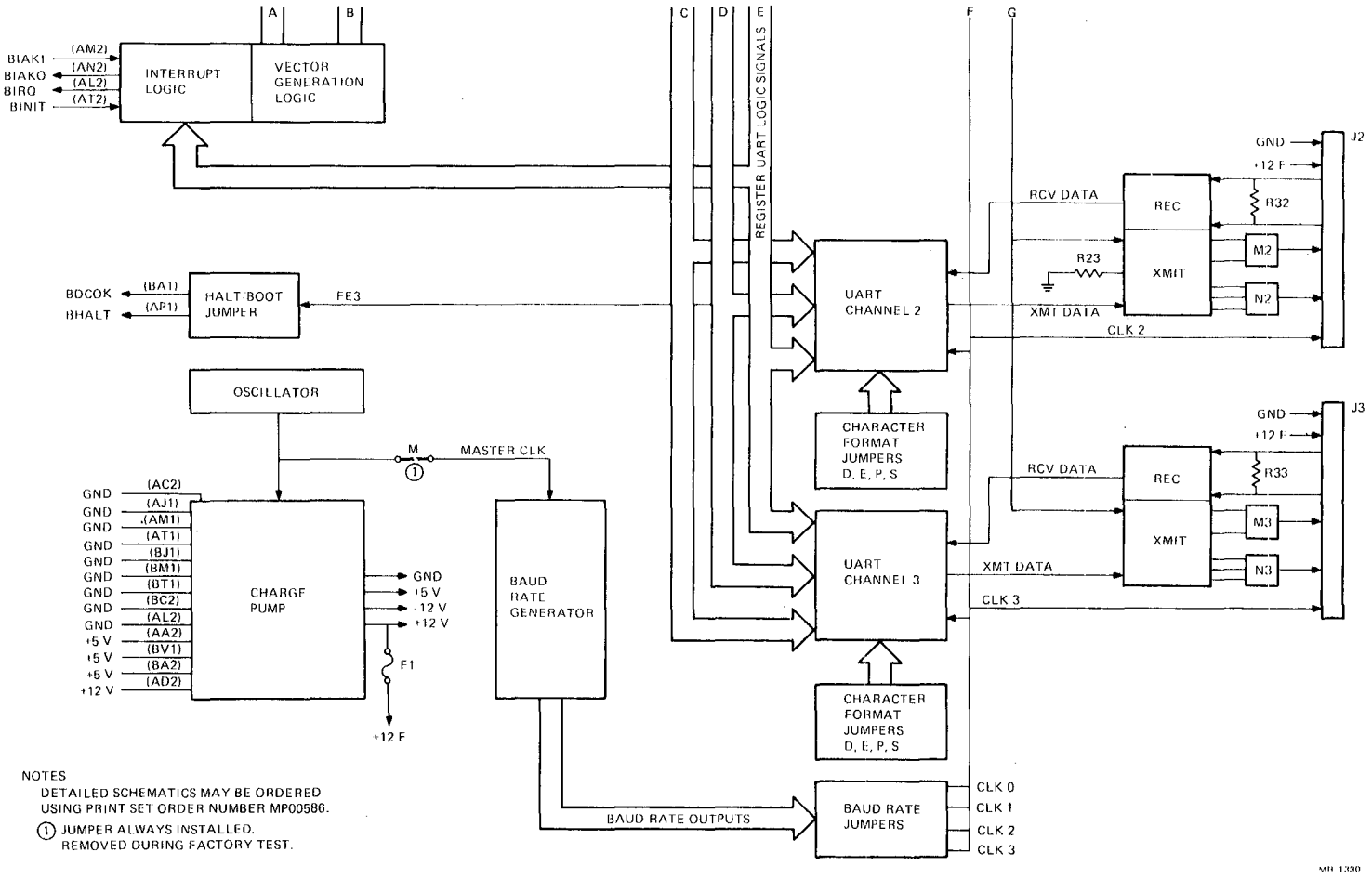


Figure 1 DLV11-J Block Diagram (Sheet 2 of 2)

The transmitter performs parallel to serial conversion of data provided by the LSI-11 bus. The character length, stop bit code, parity, and baud rate are identical to the receiver section of the SLU channel. The transmitter, however, appends the proper start, stop, and parity bits to the data before transmission.

Baud Rate Generator

The baud rate control circuit generates clock signals that control the speed at which the receive buffer (RBUF) and the transmit buffer (XBUF) move serial data. The circuit provides a command clock to both buffers of the channel.

The speed at which a channel will operate is configured by the selection of wire-wrap jumpers which supply the desired baud rate clock. The clock is developed by a crystal-controlled oscillator driving a frequency division chip. The outputs of the frequency division chip are connected to wire-wrap posts which may be selected when configuring the channel(s). If more than one channel is used for a particular baud rate, the clock may be daisy-chained between channels.

When 110 baud operation is desired, the DLV11-KA option must be used. This option provides the 110 clock to the channel via the peripheral device cable; no baud rate jumper may be configured on the module for the 110 baud channel.

I/O Control Logic

The I/O control logic directs data transfers between the computer and the DLV11-J module. The logic monitors the LSI-11 bus control lines to determine the type of data transfer to be executed (from the LSI-11 bus to the register logic for an output operation or from the register logic to the LSI-11 bus for an input operation). The following LSI-11 bus control lines are monitored by the I/O control logic during the operation:

BSYNC	Bus Synchronized. Set when valid address has been placed on LSI-11 bus.
BDIN	Bus Data Input. Set when processor is ready to receive input data.
BDOUT	Bus Data Output. Set when processor is ready to transmit output data.

The module asserts the BRPLY (reply from module) bus control line when the data transfer has been completed.

During operation, the module receives the BSYNC signal indicating an address has been placed onto the LSI-11 bus. The I/O control logic gates this address into the address latch of the module with a SYNC H gating signal. If the address received is a bus device address on the DLV11-J, the address latch sends a BD SEL signal to the I/O control logic (indicating a valid address has been received). The control logic may now develop the proper gating signals (BDOUT/BDIN) to move the data to its proper destination. When the data transfer is complete, the module signals the processor via the BRPLY control line.

Address Latch

The address latch is used to hold the channel address (0-3), the device register address (RCSR, RBUF, XCSR, or XBUF), and the high-low byte indicator of the pending operation. When the program addresses the DLV11-J module, address bits 0-4 are presented to the address latch by the bus interface circuit over the internal tri-state data bus. Simultaneously, the address compare circuit and the bus interface circuit supply the address latch with the MATCH H signal and are gated into the latch under the control of the I/O control logic circuit (SYNC H signal). The address latch now holds the address and a board select signal (BD SEL 1) to be used by the I/O control/register logic during the completion of the desired operation.

Address Compare Circuit

The address compare circuit tests the user-configured base address of the module (wire-wrap jumpers A5, A8-12) against the LSI-11 bus input (BDAL 5, 8-12 L). If the addresses are same, the address compare circuit generates a portion of the MATCH H signal. (The remainder of MATCH H is supplied by the bus interface.) The MATCH H signal is used by the address latch circuit when creating the BD SEL H signal required by the I/O control logic during data transfers.

When channel 3 is configured as a console device interface, the bus interface logic tests for a proper console device address on the LSI-11 bus. If the address received by the bus interface is a proper console address, the CON SEL 1 H signal is generated. This signal is transmitted from the bus interface to the address compare circuit to force console address recognition.

Bus Interface

The module contains bus drivers and receivers which interface directly with the LSI-11 bus. This allows data movement between the LSI-11 bus and the module's internal tri-state bus. These drivers also have

the ability to transmit vector addresses received from the interrupt vector generation logic onto the LSI-11 bus.

If the LSI-11 bus holds an address within the I/O page, the BBS7 L signal line is asserted. This will cause the bus interface circuit of the DLV11-J to test the BDAL 6-7 L lines against the user-configured wire-wrap pins (A6-7) when the addresses and the same MATCH H signal are allowed to be asserted to the address latch. Since this is a "wired-AND," the MATCH H signal from the address compare signal must also be asserted. The MATCH H signal is required by the address latch to allow I/O data transfers. If channel 3 has been selected as a console device interface (jumpers C1 and C2 installed between wire-wrap posts X and 1), the bus interface performs a match operation between the LSI-11 bus lines (BDAL 3-5) and an internal address which is enabled by console select jumper C1. If the addresses agree, a CON SEL 1 H signal is produced for the address compare circuit which will force a console address recognition.

Interrupt and Vector Generation Logic

When a peripheral device interfaced to a DLV11-J needs service, the module can, if enabled, interrupt the computer program and vector to a service routine. The interrupt logic can initiate two types of interrupts: a receiver interrupt and a transmitter interrupt. These interrupts are handled through separate receiver and transmitter channels.

For an interrupt transaction to occur, the program must set the interrupt enable bit (bit 6) in the control/status register (CSR). Next, the interrupt logic must recognize a condition requiring service (indicated by the setting of bit 7 within the CSR) and then assert the interrupt request line (BIRQ L) on the LSI-11 bus. When the interrupt is acknowledged by the processor, the interrupt logic creates an input to the module's vector generation circuit which reflects the channel needing service (0, 1, 2, or 3) and the type of service needed (receive or transmit). The vector generation logic creates a vector function address which may be modified by the user-configured "base vector" address jumpers (V5-7). This modified address is output to the LSI-11 bus by the bus interface circuit, thus causing the processor to jump to the proper peripheral device service routine.

A receiver interrupt request is initiated when the receive buffer (RBUF) has received and assembled a character of data and is ready to transfer it to the processor. A transmitter interrupt is initiated when the transmitter buffer holding register (XBUF) is empty and is ready for another data input from the processor. The interrupt logic is also used

to initialize the DLV11-J module. On a system power-up sequence, the processor creates BINIT L on the LSI-11 bus which is converted by the interrupt logic into INITO H. This signal is distributed on the module to initialize the four UARTs and the interrupt status registers (held within the interrupt logic).

Control/Status Registers

The control/status registers (CSRs) consist of a series of latches, data selectors, and gating circuitry. During data transactions, the I/O control logic enables the XCSR or RCSR to either latch in control bits or gate out status bits.

The RCSR uses only three bits during operation:

Receiver done (bit 7), set by RBUF
Receiver interrupt enable (bit 6), set by program
Reader enable (bit 0), set by program

All bits except the reader enable bit may be read by the program.

The XCSR uses three bits during operation:

Transmitter ready (bit 7), set by XBUF
Transmitter interrupt enable (bit 6), set by program
Break (bit 0), set by program and used only with the DLV11-KA option

All bits may be read by the program.

Break Logic

During normal operation, the UART checks each received character for the proper number of stop bits. It does this by testing for a marking condition at the appropriate bit time. If it finds a spacing condition instead, it sets the framing error (FE) flag. The BREAK signal is a continuous spacing condition, and is interpreted by the UART as a data character that is missing its stop bit(s). The UART, therefore, responds to the BREAK signal by asserting FE H. If the channel 3 break response jumper is installed from X to B, FE H will negate control line BDCOK H; BDCOK H indicates to the processor that dc power is "OK." When FE H negates this signal, it causes the computer to restart at the bootstrap (provided proper processor power-up mode is selected).

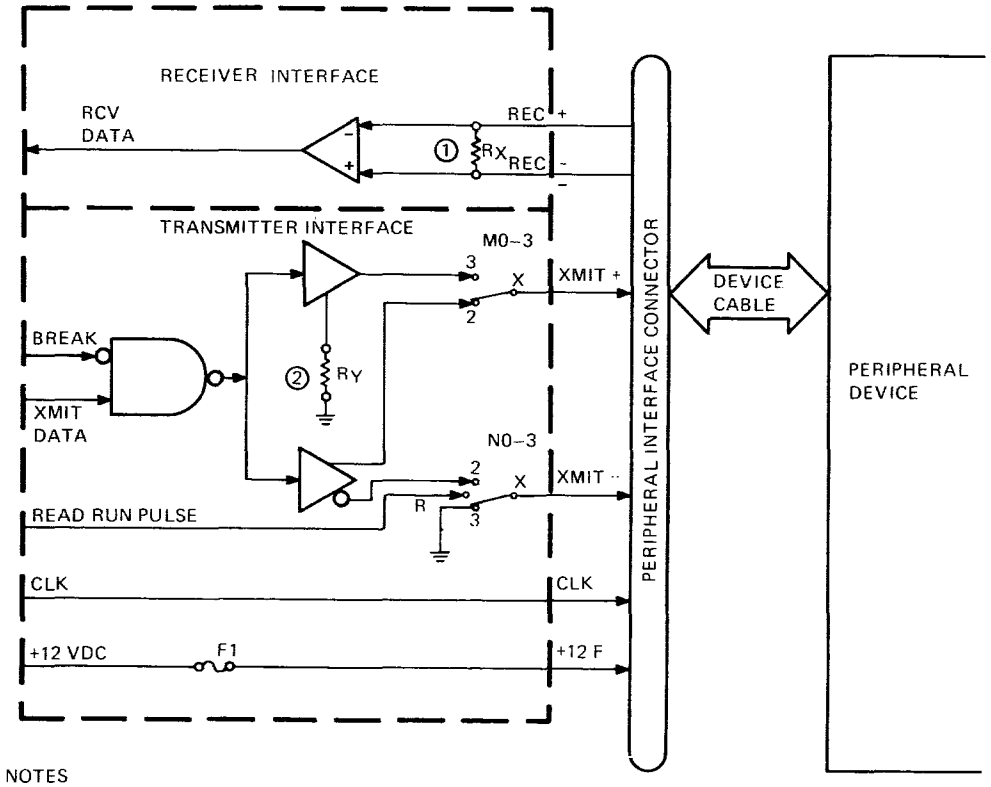
If the break jumper is installed from X to H, the computer will not "boot" on a framing error, but FE H will negate control line BHALT L. This causes the computer to halt when a framing error is received.

CAUTION

If the system is using MOS memory, data may be lost when BDCOK is negated because this action interrupts the memory refresh cycle. If the jumper is not installed, the module will not take action.

Peripheral Interface

Each SLU channel of the DLV11-J module can be independently configured for line signal compatibility with EIA RS-232C and RS-423, RS-422, or 20 mA current loop operation (Figure 2). Each of the four interfaces may be configured to support 20 mA current loop devices with the addition of the DLV11-KA option. When installed, the peripheral interface supplies all power supply voltages needed by this option. If the 20 mA device contains a paper tape reader that can be program-controlled (such as DIGITAL's LT33 or an ASR33 Teletypewriter with LT33 modification kit), the interface can be configured to advance the reader one character at a time.



NOTES

① RX IS INSTALLED WHEN CHANNEL IS CONFIGURED FOR EIA RS-422 OPERATION (100 Ω, 1/4 W NON-WIRE WOUND)
R30 - CHANNEL 0
R31 - CHANNEL 1
R32 - CHANNEL 2
R33 - CHANNEL 3

② RY IS CHOSEN FOR PROPER SLEW RATE WHEN CHANNEL IS CONFIGURED FOR EIA RS-232C/RS-423 OPERATION
R10 SETS SLEW RATE FOR CHANNELS 0 AND 1
R23 SETS SLEW RATE FOR CHANNELS 2 AND 3

MR-1297

Figure 2 Typical Peripheral Interface

DC-to-DC Power Converter

The power converter produces −12 Vdc and +5 Vdc from the LSI-11 power supply voltage of +12 Vdc. These voltages are produced to power all chips on the DLV11-J module and to supply the DLV11-KA 20 mA option. The power converter circuit consists of a crystal-controlled oscillator which drives a charge pump. The charge pump during operation supplies the desired power supply output voltage.

CONFIGURATION

The DLV11-J device and vector addressing, serial word formats, baud rates, interface, type, etc., are selected by installing and/or removing jumpers. Wire-wrap posts are provided on the module for this purpose. The module is factory-configured and ready to use in most user applications. However, if a system requires different device register addresses and interrupt vectors or operations, the module may be reconfigured. The DLV11-J module is factory-configured for the following operations:

- Base address = 176500
- Base vector address = 300
- Channel 3 enabled as the console device (device addresses 177560-177566 and vector addresses 60 and 64).
- Channel 3 halt on break enabled
- Baud rates (transmit and receive are identical):
  Channels 0,1 and 2 = 9.6K baud
  Channel 3 = 300 baud
- Data/parity/stop bit format (all channels):
  Eight data bits
  One stop bit
  No parity
- Serial line signal interface levels (all channels) compatible with both EIA RS-232C and RS-423, simultaneously (slew rate = 2 μs)

Figure 3 gives jumper and pad locations on the DLV11-J module and Table 1 gives a summary of the module's factory configuration.

DLV11-J

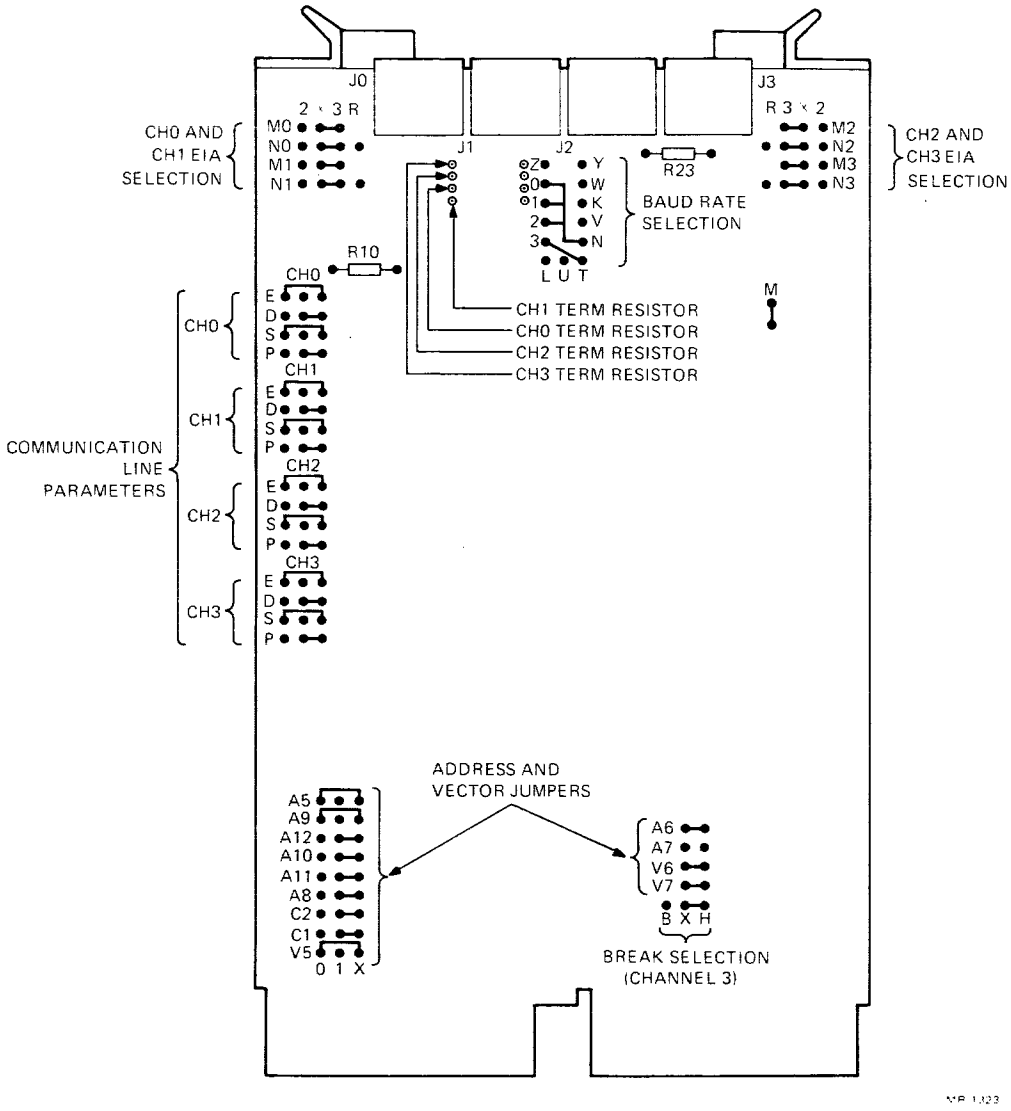


Figure 3 DLV11-J Jumper Locations

DLV11-J

Table 1 Factory Jumper Configuration

Label	Standard Configuration	Function Implemented
A12 A11 A10 A9 A8 A7 A6 A5	X to 1 X to 1 X to 1 X to 0 X to 1 R I X to 0	This arrangement of jumpers A5-A12 implements the octal base device address 1765XX, which is the assigned address for channel 0 RCSR. The least significant digit is decoded on the module during operation to address one of four SLU device registers as follows: X = 0, RCSR X = 2, RBUF X = 4, XCSR X = 6, XBUF
C1 C2	X to 1 X to 1	These jumpers are used to enable channel 3 for console operation. Base address must be 176500 (factory-configured), 176540, or 177500 for the console.
(Break response)	X to H	This jumper determines channel 3 break response. The board is configured for halt (console emulator mode) on break condition.
V7 V6 V5	I I X to 0*	This arrangement of jumpers V5-V7 implements the octal "base" vector of 300 with channel 3 at 60 and 64.
E D S P	X to 0 X to 1 X to 0 X to 1	Odd parity 8 data bits 1 stop bit Parity inhibited These jumpers determine the word format used by the channel. All channels are configured the same at the factory.

Table 1 Factory Jumper Configuration (Cont)

Label	Standard Configuration	Function Implemented
0	0 to N	9.6K baud
1	1 to N	9.6K baud
2	2 to N	9.6K baud
3	3 to T	300 baud These jumpers determine the baud rate of the serial line channel for same baud rate daisy-chain wire-wraps.
NO-3 MO-3	X to 3 X to 3	These jumpers determine the EIA standard compatibility of the channel. All channels are set at the factory to be compatible to both EIA RS-423 and RS-232C simultaneously.
R10	22KΩ	Channels 0 and 1, slew rate of 2 μs (used when configured for EIA RS-423/RS-232C).
R23	22KΩ	Channels 2 and 3, slew rate of 2 μs (used when configured for EIA RS-423/RS232C).

* See Interrupt Vector Format figure.

Device Registers— The DLV11-J contains 16 device registers that can be individually addressed by the program. The four device registers provided for each of the SLU channels (0 through 3) are:

Receive Control/Status Registers (RCSR)
Receive Buffer (RBUF)
Transmit Control/Status Register (XCSR)
Transmit Buffer (XBUF)

Wire-wrap jumpers are configured to establish the base address (BA) for the module. This base address is the channel 0 RCSR address. The device address format is shown in Figure 4. The remaining device addresses follow through 16 (total) contiguous word addresses; however, it is possible to independently dedicate the last four addresses (channel 3) to a console device. When configured for console device operation, the channel's device register addresses will be 177560-

177566. For console operation, the board's base address must be one of the following:

176500 (factory-configured)
176540
177500

The floating address configurations are listed in Table 2 and the factory or standard configuration addresses are listed in Table 3.

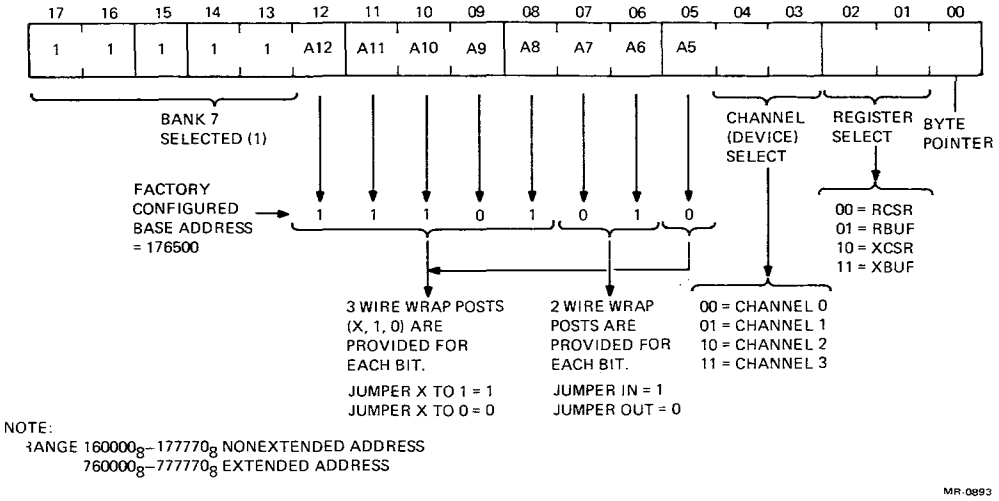


Figure 4 Channel 0 RCSR Address Format

Table 2 Address Assignments (with Console Selected)

Address	Device Register	Associated Vector
	Channel 0	
Module Base Address (BA)	RCSR	Module Base Vector (BV)
BA+2	RBUF	
BA+4	XCSR	BV+4
BA+6	XBUF	
	Channel 1	
BA+10	RCSR	BV+10
BA+12	RBUF	
BA+14	XCSR	BV+14
BA+16	XBUF	

Table 2 Address Assignments (with Console Selected) (Cont)

Address	Device Register	Associated Vector	
		Channel 2	
BA+20	RCSR	BV+20	
BA+22	RBUF		
BA+24	XCSR	BV+24	
BA+26	XBUF		
		Channel 3*	
177560	RCSR		
177562	RBUF	60	Console
177564	XCSR		Selected
177566	XBUF	64	

* Channel 3 is used as a console device.

Table 3 Factory or Standard Addresses

Address	Register	Vector	
176500	RCSR		
176502	RBUF	300	
176504	XCSR		Channel 0
176506	XBUF	304	
176510	RCSR		
176512	RBUF	310	
176514	XCSR		Channel 1
176516	XBUF	314	
176520	RCSR		
176522	RBUF	320	
176524	XCSR		Channel 2
176526	XBUF	324	
177560	RCSR		
177562	RBUF	60	
177564	XCSR		Channel 3
177566	XBUF	64	

Four word formats, one for each device register within a channel, are shown in Figure 5 and described in Table 4. These word formats are typical of all channels on the DLV11-J module.

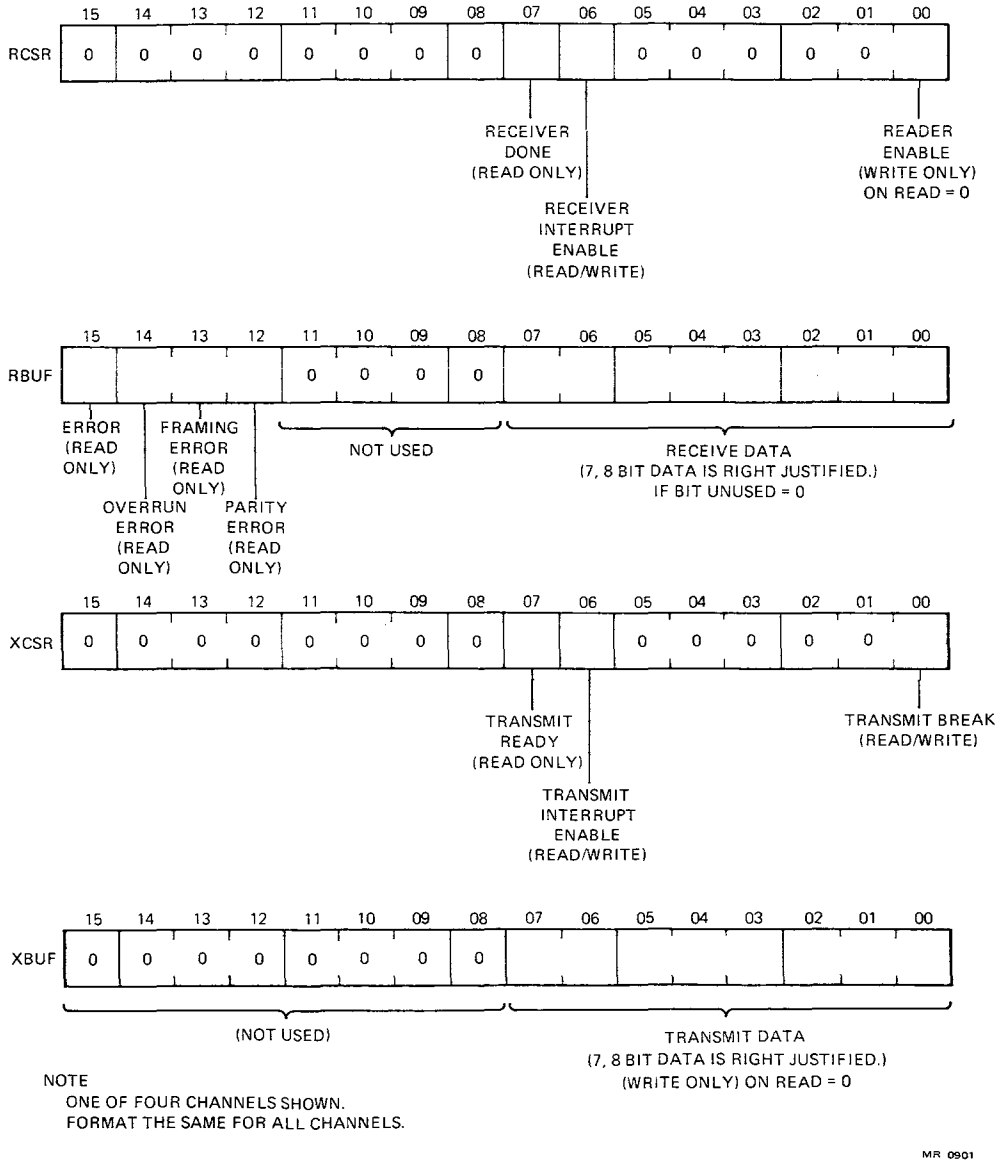


Figure 5 DLV11-J Device Register Formats

Table 4 DLV11-J Word Formats

Receiver Control/Status Register

Bit: 8-15
Description: Not used. Read as 0.

Bit: 7
Description: Receiver Done. Set when an entire character has been received and is ready for input to the processor. This bit is automatically cleared when RBUF is read, when BINIT L signal goes true (low), or when reader enable bit is set. Read-only bit.

If Receiver Interrupt (bit 6) is set, the setting of Receiver Done starts an interrupt sequence.

Bit: 6
Description: Receive Interrupt Enable. Set under program control when it is desired to generate a receiver interrupt request (when a character is ready for input to the processor signified by bit 7 being set). Cleared under program control or by the BINIT signal. Read/write bit.

Bit: 1-5
Description: Not used. Read as 0.

Bit: 0
Description: Reader Enable. Setting this bit advances the paper tape reader on an LT33 terminal one character at a time. Setting of this bit clears Receiver Done (bit 7). Write-only bit.

The DLV11-KA 20 mA current loop option is required for operation of this bit.

Receiver Buffer

Bit: 15
Description: Channel Error Status. Logical OR of bits 14, 13, and 12. Read-only bit.

Bit: 14
Description: Overrun Error. When set, indicates that the reading of the previously received character was not completed (Receiver Done not cleared) prior to receiving a new character.

Cleared by BINIT signal. Read-only bit.

NOTE

When "back-to-back" characters are received, one full character time is allowed from the time instant receiver done (bit 7) is set to the occurrence of an overrun error.

Bit: 13
Description: Framing Error. When set, indicates that the character read had no valid stop bit.

Cleared by BINIT signal. Read-only bit.

Bit: 12
Description: Parity Error. When set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no-parity operation is configured for the channel. Read-only bit.

NOTE

Error bits remain valid until the next character is received, at which time the error bits are updated.

Bit: 8-11
Description: Not used. Read as 0.

Bit: 0-7
Description: Data bits. Contains seven or eight data bits in a right-justified format. Bit 7 = 0 when 7 data bits are enabled. Read-only bits.

Transmitter Control/Status Register

Bit: 8-15
Description: Not used. Read as 0.

Bit: 7
Description: Transmit Ready. Set when XBUF is empty and can accept another character for transmission. It is also set by INIT during the power-up sequence or during a reset instruction. Read-only bit.

If Transmitter Interrupt Enable (bit 6) is set, the setting of Transmit Ready will start an interrupt sequence.

Bit: 6
Description: Transmit Interrupt Enable. Set under program control when it is desired to generate a transmitter interrupt request (when transmitter is ready to accept a character for transmission).

The bit is cleared under program control, during power-up sequence, or reset instruction. Read/write bit.

Bit: 1-5
Description: Not used. Read as 0.

Bit: 0
Description: Transmit Break. Set or reset under program control. When set, a continuous space level is transmitted. However,Transmit Done and Transmit interrupt can still operate, allowing software timing of break. When not set, normal character transmission can occur.

Cleared by BINIT. Read/write bit.

Transmit Buffer

Bit: 8-15
Description: Not used. Read as 0.

Bit: 0-7
Description: Data bits. Contains seven or eight right-justified data bits. Loaded under program control for serial transmission.

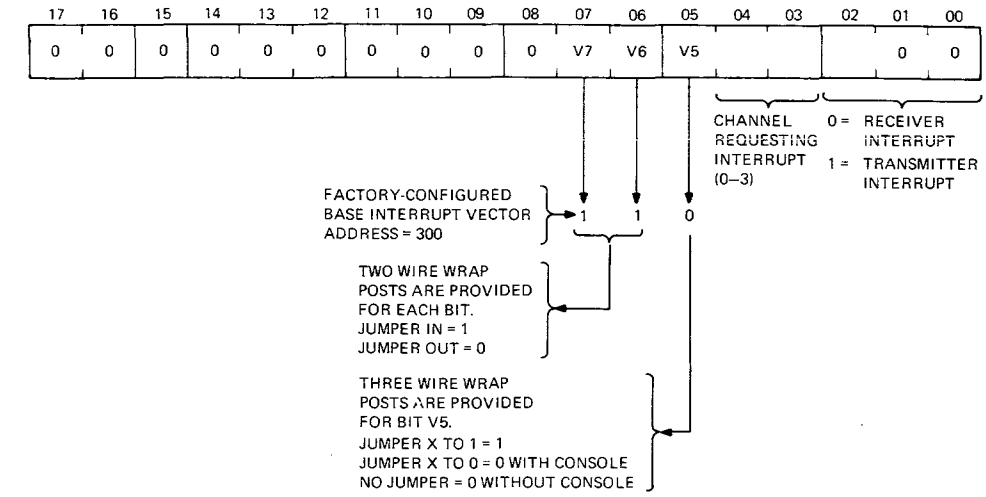
Interrupt Vectors

Two interrupt vectors are provided for each of the four SLU channels (eight vectors total). The procedure for configuring the vectors is similar to that used when configuring the base device register address; the configured base vector is the channel 0 receiver interrupt vector. Each interrupt vector references two word locations in memory (the Program Counter address and the Processor Status Word). Hence, sequential vectors appear in increments of four.

The module is factory-configured with an interrupt vector base of 300. However, it is also configured for channel 3 operation as the console device; thus, channel 3 will automatically have interrupt vectors of 60 and 64. The vector format is shown in Figure 6 and a summary of vector jumper configurations is provided in Table 5. Table 6 gives a list of the factory-configured vector assignments.

Interrupt priority within the DLV11-J module is structured as follows:

Interrupt Priority	Requesting Function
1 (highest)	Channel 0, receiver
2	Channel 1, receiver
3	Channel 2, receiver
4	Channel 3, receiver
5	Channel 0, transmitter
6	Channel 1, transmitter
7	Channel 2, transmitter
8 (lowest)	Channel 3, transmitter



NOTE:
RANGE $0–377_8$ (040_8 NOT ALLOWED IN CONSOLE MODE)

MR-0895

Figure 6 Interrupt Vector Format

Table 5 Summary of Vector Jumper Configurations

Label	Logical 1	Logical 0
V7	Jumper installed.	Jumper removed.
V6	Jumper installed.	Jumper removed.
V5	Jumper installed from wire-wrap post X to 1.	Console not selected: jumper removed. Console selected: jumper. installed from wire-wrap post X to 0.

Table 6 Vector Assignments (with Console Selected) (Factory Configured)

Standard Address	Interrupt Vector
300 [Module Base Vector (BV)]	Channel 0, Receiver
304 (BV+4)	Channel 0, Transmitter
310 (BV+10)	Channel 1, Receiver
314 (BV+14)	Channel 1, Transmitter
320 (BV+20)	Channel 2, Receiver
324 (BV+24)	Channel 2, Transmitter
60	Channel 3, Receiver
64 Console Selected	Channel 3, Transmitter

NOTES

1. Module is factory-configured for channel 3 as a console device.
2. All addresses are in octal notation.

Character Formats

Each of the four channels may be independently configured for various character formats. When a character format is configured (by wire-wrap jumpers) for a channel, both the transmitter and receiver will use the same format. The character may contain:

7 or 8 data bits
1 or 2 stop bits
Parity or no parity
Even or odd parity

Configuration instructions for determining the character formats of each channel are shown in Table 7.

Baud Rates

Each channel can be configured for baud rates ranging from 150 to 38,400 bits per second. One baud rate clock input wire-wrap pin is provided for each channel (0 through 3). Both the transmitter and receiver for a given channel must operate at the same baud rate; split baud rate operation cannot be configured. Configure baud rates by connecting a jumper from the appropriate baud rate generator output wire-wrap pin to the clock input pin of the channel. One jumper is

required for each channel. When configuring the same baud rate for more than one channel, the wire-wrap pins may be daisy-chained. Table 8 lists the possible baud rates for each channel and their associated labels.

Table 7 Character Format Jumpers

Label	Channel Parameter	Wire-wrap X to 0	Connection X to 1	Comments
D	No. of data bits	7 bits	8 bits	LSB transmitted first
S	No. of stop bits	1 bit	2 bits	
P	Parity inhibit	Parity generation and detection enabled	Parity bit deleted; parity error = 0	
E	Even parity enabled	Odd parity expected	Even parity expected	Only when P = 0

Table 8 Baud Rate Generator Outputs

Wire-Wrap Pin Label	Baud Rate (Bits/Second)
U	150
T	300
V	600
W	1,200
Y	2,400
L	4,800
N	9,600
K	19,200
Z	38,400

When using the DLV11-KA option, 110 bits/sec operation is possible. A 110 baud rate clock generator circuit on the option will supply the DLV11-J module with the proper clock; no baud rate jumper is configured on the module for the desired channel.

Console Device Selection

Channel 3 of the DLV11-J module may be independently dedicated for console device operation. To accomplish this, the console select jumpers must be properly configured. Table 9 gives channel 3 configuration instructions. When configured for console operation, the device addresses are 177560-177566 and the interrupt vectors are 60 and 64.

Table 9 Summary of Console Selection Jumper Configurations

Label	Console Selected	Console Not Selected
C1	Install jumper from wire-wrap pins X to 1.	Install jumper from wire-wrap pins X to 0.
C2	Install jumper from wire-wrap pins X to 1.	Install jumper from wire-wrap pins X to 0.

Break Response

Channel 3 may be configured to either bootstrap, halt (console emulator mode), or have no response to a receive break condition. A bootstrap operation upon a receive break condition will cause the processor to execute the bootstrap program starting at the memory location defined by the power-up mode jumpers of the processor. A halt operation upon a receive break condition will cause the processor to halt and the console octal debugging technique (ODT) microcode to be invoked. Configuration instructions are given in Table 10.

Table 10 Channel 3 Break Operation Jumper Summary

Break Operation Response	Jumper Connection
Boot*	Install jumper between wire-wraps X to B.
Halt	Install jumper between wire-wrap pins X to H.
No Response	No jumper installed.

* Do not send continual breaks to a system so configured, as it will cause continued reinitializing of any device on the bus.

Peripheral Interface Configuration

Each of the channels can be independently configured for serial line signal compatibility with EIA RS-423 (simultaneously RS-232C), RS-422, or 20 mA current loop devices. When using 20 mA current loop devices, the DLV11-KA option is required. Configuration instructions for each of the standards are listed in Table 11. Table 12 is used when configuring EIA RS-423 (RS-232C compatible) slew rates. Use this table in conjunction with Table 11.

Table 11 Summary of Serial Channel Signal Level Configurations

Serial Channel Signal Level Modifiers	EIA RS-422	EIA RS-232C and RS-423	20 mA Current Loop (Using DLV11-KA)
M0-3 Jumper	Connect wire-wrap pins X and 2.	Connect wire-wrap pins X and 3.	Connect wire-wrap pins X and 3.
N0-3 Jumper	Connect wire-wrap pins X and 2	Connect wire-wrap pins X and 3.	Connect wire-wrap pins X and R for program-controlled paper tape reader.
Termination Resistor (one per channel)	Install a 100Ω, 1/4 W, non-wire wound, fusible resistor.		
Wave-Shaping Resistor (one per channel pair; channel pair 0 and 1; 2 and 3)		Install resistor from Table 12 (1/4 W non-wire wound).	
Fuse F1			Install 2.0 A Pico fuse

Table 12 EIA RS-423 and RS-232C Slew Rate Resistor Values

Baud Rate	R10 or R23
38.4 K	22 KΩ
19.2 K	51 KΩ
9.6 K	120 KΩ
4.8 K	200 KΩ
2.4 K	430 KΩ
1.2 K	820 KΩ
600	1 MΩ
300	1 MΩ
150	1 MΩ
110	1 MΩ

Cabling

Following are listed cables currently available that will mate with the 2×5 pin Amp connector on the DLV11-J, as well as some pointers and part numbers for constructing a cable.

DIGITAL cables for the DLV11-J:

BC20N-05	5' EIA RS-232C null modem cable to directly interface with an EIA RS-232C terminal (2×5 pin Amp female to RS-232C female; see Figure 8).
BC21B-05	5' EIA RS-232C modem cable to interface with modems and acoustic couplers (2×5 pin Amp female to RS-232C male; see Figure 7).
BC20M-50	50' EIA RS-422 or RS-423 cable for high-speed transmission (19.2K baud) between two DLV11-Js (2×5 pin Amp female to 2×5 pin Amp female).
DLV11-KA	20 mA current loop converter option for the DLV11-J. Comes **with** an EIA cable (BC21A-03) which connects the DLV11-KB converter box to the DLV11-J. The option mates with standard DIGITAL 20 mA cabling using the 8-pin Mate-'N'-Lock connector.

DLV11-J

When designing a cable for the DLV11-J, here are several points to consider:

1. The receivers on the DLV11-J have differential inputs. Therefore, when designing an RS-232C or RS-423 cable, RECEIVE DATA (pin 7 on the 2×5 pin Amp connector) must be tied to signal ground (pins 2, 5, or 9) in order to maintain proper EIA levels. RS-422 is balanced and uses both RECEIVE DATA+ and RECEIVE DATA —.
2. To directly connect to a local EIA RS-232C terminal, it is necessary to use a null modem. To design the null modem into the cable, one must switch RECEIVE DATA (pin 2) with TRANSMITTED DATA (pin 3) on the RS-232C male connector as shown in Figure 8.
3. To mate to the 2×5 pin connector block, the following parts are needed:

Cable Receptacle	AMP PN 87133-5 DEC PN 12-14268-02
Locking Clip Contacts	AMP PN 87124-1 DEC PN 12-14267-00
Key Pin (pin 6)	AMP PN 87179-1 DEC PN 12-15418-00

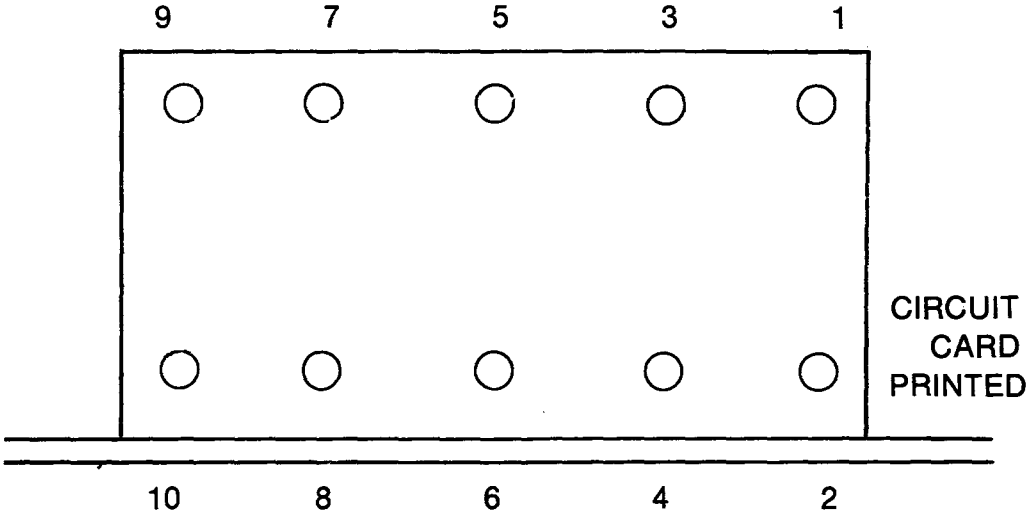
4. The pin out on the 2×5 pin connector block on the DLV11-J is as follows:

Pin #	**Signal**
1	UART clock in or out (16 × baud rate; CMOS)
2	Signal ground
3	TRANSMIT DATA+
4	TRANSMIT DATA−

Note: For EIA RS-423, this line is grounded. For DLV11-KA 20 mA option, this line is the reader enable pulse.

5	Signal ground
6	Indexing key—no pin
7	RECEIVE DATA−
8	RECEIVE DATA+
9	Signal ground
10	When F1 is installed for the DLV11-KA, +12V is supplied through a fuse to this pin

DLV11-J



2×5 PIN CONNECTOR
BLOCK (Viewed from
Edge of Card)

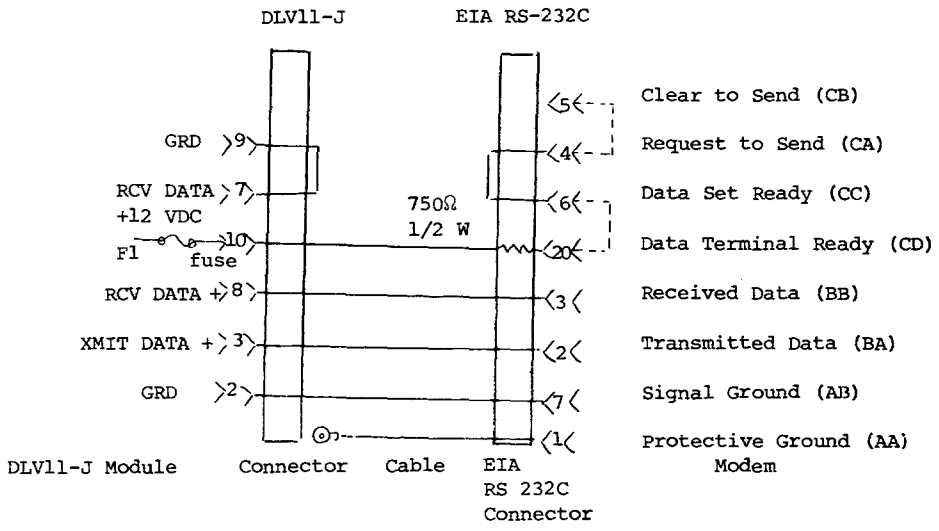


Figure 7 BC21B-05 Modem Cable

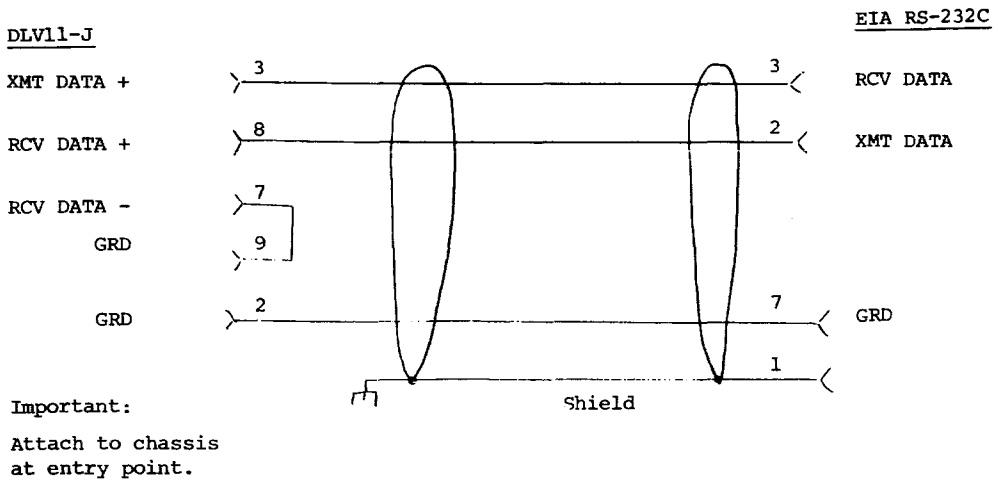


Figure 8 BC20N-05 "Null Modem" Cable

PROGRAMMING

The DLV11-J contains a bank of sixteen (16) contiguous registers that may be positioned from 160000_8 to 177777_8 in address space by wire wrap jumpers. Four registers are provided for each of the four SLU channels.

The format of these registers is shown in Figure 1.

Similarly, the DLV11-J has a bank of eight contiguous interrupt vectors that may be positioned in vector space from 000_8 to 377_8 by jumpers. Two vectors (receive and transmit) are provided for each of the four channels.

NOTE

One channel may be separately configured as the computer console device ($177560\text{-}6_8$, vectors 60 and 64) provided the module base address is 176500_8, 176540_8 or 177500_8.

To software, the DLV11-J appears to be four independent serial line units similar to four single-channel DLV11s.

DLV11-KA

DLV11-KA EIA TO 20 MA CONVERTER

INTRODUCTION

The DLV11-KA option consists of the DLV11-KB EIA-to-20 mA converter unit and a BC21A-03 EIA interface cable. This option is designed to allow 20 mA current loop capability to be added to a standard RS-232 EIA serial line unit interface module, such as the DLV11-J. The DLV11-KB is a small enclosed box with two connectors, one (2 × 5 pin Berg) for the EIA/TTL signals from the interface module and the other (standard DIGITAL 20 mA connector 8-pin Mate-N-Lok) for the 20 mA signals to 20 mA peripherals using standard DIGITAL 20 mA cabling.

FEATURES

- EIA RS-232 to 20 mA converter (XMT data)
- 20 mA to EIA RS-232 converter (RCVR data)
- A program-controlled, one character at a time reader advance function for DIGITAL-modified ASR-33 Teletypes*
- A 110 baud rate generator
- Optical isolation
- Choice of active or passive operation
- Operates up to 9600 baud rate
- Drive capability up to 4000 feet of cable

* Teletype is a registered trademark of Teletype Corporation.

SPECIFICATIONS

Size:	13.3cm (5.25 in.) long 11.4cm (4.5 in.) wide 2.64cm (1.04 in.) high
Power:	+12.0 Vdc ±5% at 0.275 A max

CONFIGURATION

The DLV11-KA requires the configuration of eleven jumper wire connections and one capacitor connection. The locations of these jumpers are shown in Figure 1 and their functions are listed in Table 1.

Current Loop Definition

In simplest terms, the current in a circuit loop which extends from the sender to the receiver is switched on and off to represent some particular format for serial transmission of binary data. Besides the actual current path (wire), the following other three functions are required in every current loop:

1. Current source 2. Switch 3. Current detector

The switch has to be located in the transmitter, and the current detector has to be located in the receiver. However, the current source may be located in either the sender or receiver. The function that includes the current source is designated active and the one without it passive. Only one passive and one active function are allowed in a current loop: never two active or two passive functions (Figure 2). In order to minimize ground differential noise coupling into data leads, the transmitter and receiver at one end of the line should be either both active or both passive, not mixed. Also, it is usually better to configure the computer (master computer) as active and the terminal (slave computer) as passive.

110 Baud Rate Generator

This circuit provides a 16 × 110 (1760 Hz), TTL level, crystal-controlled clock to be sent back to the serial line unit module in order to add 110 baud rate capability to the module. A solderable jumper (W11) is provided in order to select or deselect this function.

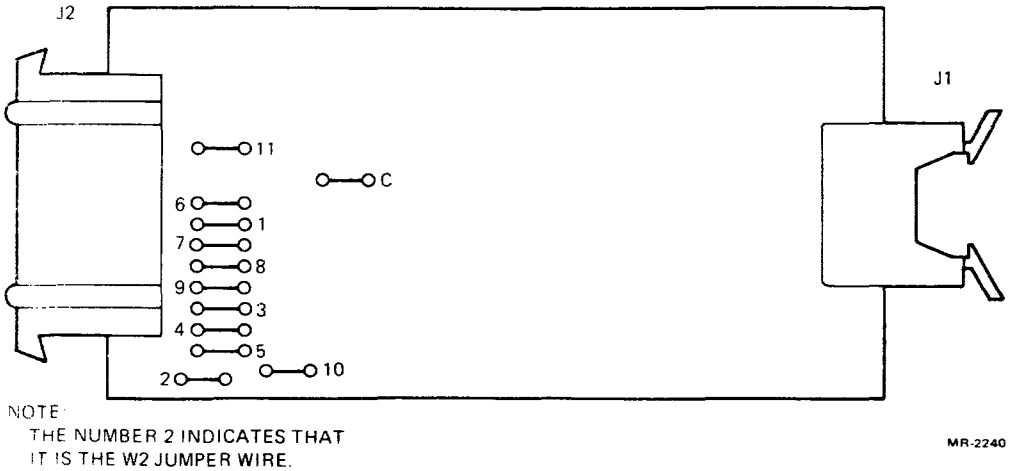


Figure 1 DLV11-KA Jumper Locations

DLV11-KA

Table 1 DLV11-K∆ Jumper Configurations

Function	Jumper In	Jumper Out
Passive 20 mA Receiver	W7, W9	W6, W8, W10
Active 20 mA Receiver*	W6, W8, W10	W7, W9
Passive 20 mA Transmitter	W2, W4	W1, W3, W5
Active 20 mA Transmitter*	W1, W3, W5	W2, W4
110 Baud Enabled*	W11	-
110 Baud Disabled	-	W11
Noise Suppression	-	-

* Factory configuration.

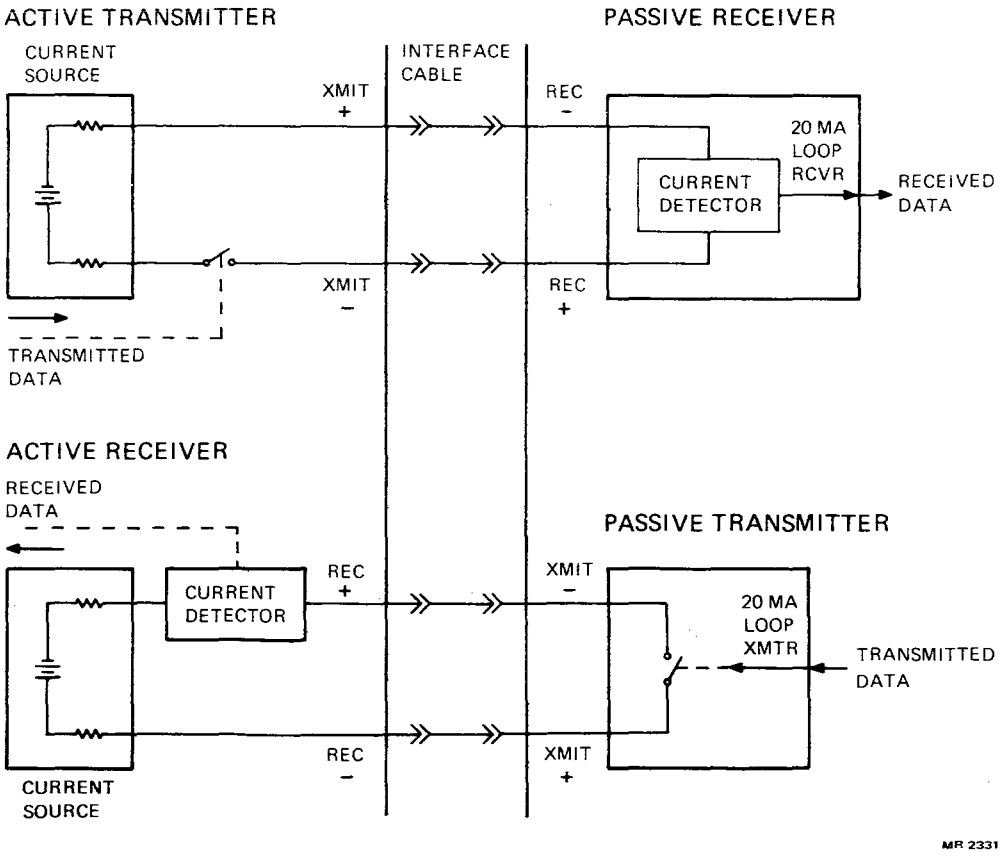


Figure 2 Standard Current Loop Interface

DLV11-KA

Installation

The DLV11-KA option can be installed in a system that requires conversion from EIA RS-232 standard to a 20 mA current loop. The DLV11-KA option consists of a DLV11-KB converter box and a BC21A-03 interface cable as shown in Figure 4. The BC21A-03 is a 0.9 m (3 ft.) cable that interconnects the DLV11-KB to a EIA SLU interface module. The smaller connector (2 × 5 pin) connects to the SLU module and the larger connector (2 × 7 pin) connects to the DLV11-KB box. Keying is provided on both connectors, and cable retention is provided by locking pins on the SLU connector. To disengage, pull back on the connector shell and the connector will slide free. However, if the cable is pulled, the locking pins will hold the connector firmly in place. A BC05F-XX cable can be used to connect the DLV11-KB converter box to DIGITAL 20 mA terminals including the DIGITAL-modified ASR-33 Teletype. External mounting dimensions for the DLV11-KB box are shown in Figure 4.

Cabling

Cables other than the DIGITAL BC05F-XX can be used when installing the DLV11-KA option. However, any other cable must conform to the following parameters in order to meet the baud rate versus cable length specification described in Table 2.

1. Resistance—not more than 30 ohms/1000 ft. (not less than 22 AWG)
2. Capacitance to ground—not more than 50 pF/ft.
3. Capacitance wire-to-wire—not more than 35 pF/ft.

The BC05F-XX cable meets the above requirements. If the user desires to use shielded cable, the shield should be grounded to the chassis at entry point and not to the DLV11-KB converter box. The user can fabricate custom cables for the 20 mA interface by using DIGITAL connectors and pins.

Baud Rate

The DLV11-KA option will operate up to a maximum of 9600 baud, provided that the interface module can accommodate these rates.

However, the maximum operational baud rate is also limited by the length of cable. Table 2 provides maximum recommended cable lengths for the specific baud rates. These recommendations are conservative and will yield satisfactory operation for almost all applications. Exceeding these guidelines should be done only after reviewing the DLV11-KA specifications, the severity of the operating environment, and the error rate that can be tolerated.

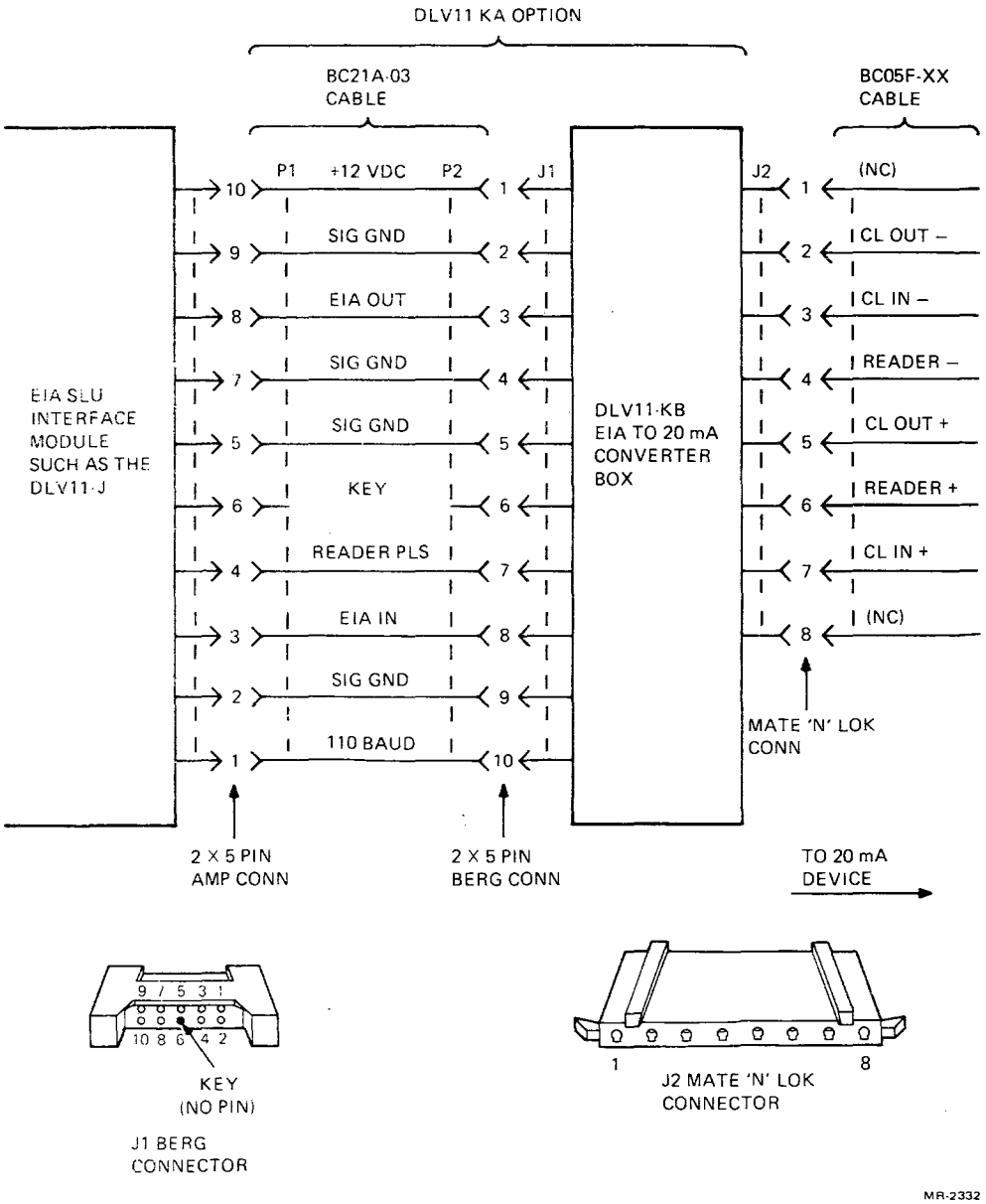


Figure 3 DLV11-KA Typical Installation

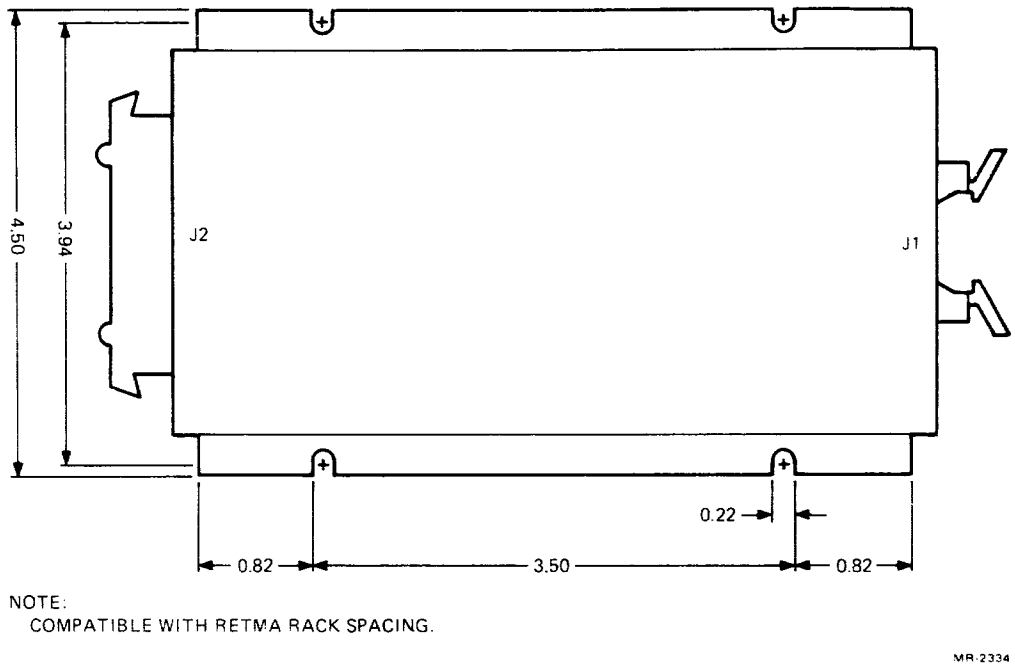


Figure 4 DLV11-KA Mounting Dimensions

Table 2 Baud Rate vs. Cable Length

Baud Rate	Max Cable Length
9600	30 m (100 ft.)
4800	76 m (250 ft.)
2400	152 m (500 ft.)
1200	305 m (1000 ft.)
600	610 m (2000 ft.)
300	1220 m (4000 ft.)
110	1220 m (4000 ft.)

DRV11

DRV11 PARALLEL LINE UNIT

INTRODUCTION

The DRV11 is a general purpose interface unit used for connecting parallel line TTL or DTL devices to the LSI-11 bus over up to 7.6 m (25 ft) of cable. It permits program-controlled data transfers at rates up to 40K words per second and provides LSI-11 bus interface and control logic for interrupt processing and vector generation. Data is handled by 16 diode-clamped input lines and 16 latched output lines. The device address is user-assigned and control/status registers (CSR) and data registers are compatible with PDP-11 software routines.

FEATURES

- 16 diode-clamped data input lines
- 16 latched output lines
- 16-bit word or 8-bit byte programmed data transfers
- User-assigned device address decoding
- LSI-11 bus interface and control logic for interrupt processing and vector generation
- Interrupt priority determined by electrical position along the LSI-11 bus
- Control/status registers (CSR) and data registers that are compatible with PDP-11 software routines
- Four control lines to the peripheral device for NEW DATA RDY, DATA TRANS, REQ A, and REQ B
- Logic-compatible with TTL and DTL devices
- Program-controlled data transfer rate of 40K words per second (maximum)

SPECIFICATIONS

Identification	M7941
Size	Double
Power	5.0 Vdc ±5% at 0.9 A
Bus Loads	
AC	1.4
DC	1.0

DESCRIPTION

Major functions contained on the DRV11 module are shown in Figure 1. Communications between the processor and the DRV11 are execut-

ed via programmed I/O operations or interrupt-driven routines.

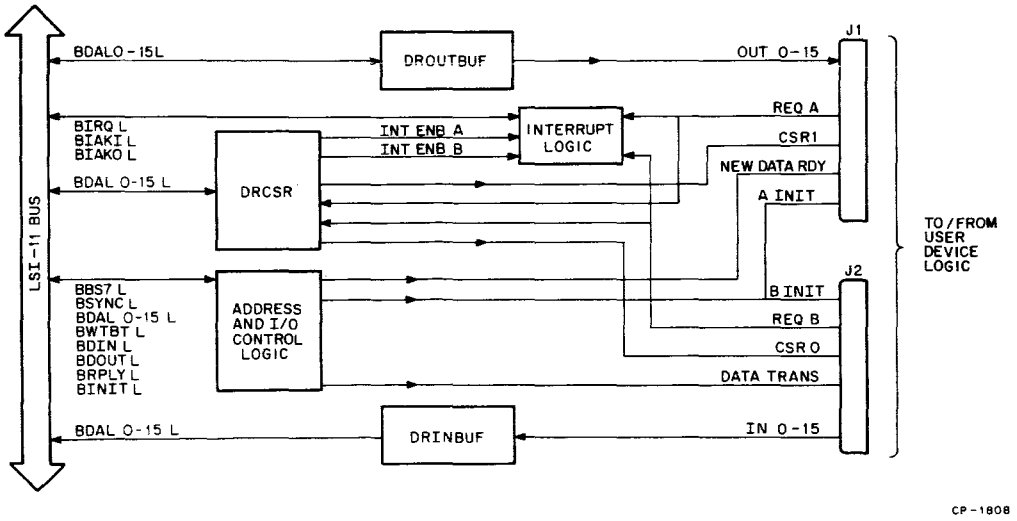


Figure 1 DRV11 Parallel Line Unit

The DRV11 is capable of storing one 16-bit output word or two 8-bit output bytes in DROUTBUF. The stored data (OUT0-15 H) is routed to the user's device via an optional I/O cable connected to J1. Any programmed operation that loads a byte or a word in DROUTBUF causes a NEW DATA RDY H signal to be generated, informing the user's device of the operation.

Input data (DRINBUF) is gated onto the BDAL bus during a DATI bus cycle. All 16 bits are placed on the bus simultaneously; however, when the processor is involved in an 8-bit byte operation, it uses only the high or low byte. When the data is taken by the processor, a DATA TRANS H pulse is sent to the user's device to inform the device of the transfer.

Addressing

When addressing a peripheral device interface such as the DRV11, the processor places an address on BDAL0-15 L, which is received and distributed as BRD0-15 H in the DRV11. The address is in the upper 4K (28-32K) address space. On the leading edge of BSYNC L, the address decoder decodes the address selected by jumpers A3-A12 and sets the device selected flip-flop (not shown); the active flip-flop output is the ME signal, which enables function selection and I/O control logic operation. At the same time, function selection logic stores address bits BRD0-2.

NOTE

When addressed, the DRV11 always responds to either BDIN L or BDOUT L by asserting BRPLY L (L = assertion).

Function Selection

Function selection and I/O control logic monitors the ME signal and bus signals BDIN L, BDOUT L, and BWTBT L. It responds by generating appropriate select signals which control internal data gating. NEW DATA RDY H or DATA TRANS H output signals for the user's device, and the BRPLY L bus signal which informs the processor that the DRV11 has responded to the programmed I/O operation. Since the DRV11 appears to the processor as three addressable registers (DRCSR, DROUTBUF, and DRINBUF) that can be involved in either word or byte transfers, the three low-order address bits stored during the addressing portion of the bus cycle are used for function selection. The select signals relative to I/O bus control signals and address bits 0-2 are listed in Table 1.

Function selection is performed by a ROM located at E15 on the DRV11. The inputs to this ROM consist of the address bits and other LSI-11 bus signals as shown at the top of Table 1. This table shows the functions performed by the ROM outputs for a specific input condition. For example, when the output buffer is addressed by the processor, the last octal digit is decoded by the ROM to provide the SEL2IN L and the RPLY L signals. The RPLY L signal is delayed and becomes the BRPLY L signal. The SEL2IN L signal is used by the DRV11 logic to enable the contents of the output buffer register to be placed on the data lines of the LSI-11 bus so that the processor can read the data.

NEW DATA READY H is active for the duration of BDOUT L when in a DROUTBUF write operation. This signal is normally active for 350 ns. However, by adding an optional capacitor in the BRPLY L portion of the circuit, the leading edge of BRPLY is delayed, effectively increasing the duration of the NEW DATA RDY H pulse; adding the capacitor also increases the DATA TRANS H pulse width by approximately the same amount.

DATA TRANS H is active for the duration of BDIN L when in a DRINBUF read operation. This signal is normally active for 1150 ns. The time, however, can be extended by adding the optional capacitor to the BRPLY L portion of the circuit as previously described.

Table 1 DRV11 Device Function Decoding

Programmed Operation	Stored Device Addr. Bits 0-2	BWTBT L During Data Transfer	BDIN L	BDOUT L	Bus Cycle Type	Select Signals
	0	0	H	L	DATO	
Write DRCSR	0	1	H	L	DATOB	SEL0OUT L
Read DRCSR	0	0	L	H	DATI or DATIO	SEL0IN L
Write DROUTBUF Word	2	0	H	L	DATO	SEL2OUT (W + HB) L, SEL2OUT (W + LB) L, and NEW DATA READY H
Low Byte	2	1	H	L	DATOB	SEL2OUT (W + LB) L and NEW DATA READY H
High Byte	3	1	H	L	DATOB	SEL2OUT (W + HB) L and NEW DATA READY H
Read DROUTBUF	2	0	L	H	DATI or DATIO	SEL2IN L
Read DRINBUF	4	0	L	H	DATI	SEL4IN L and DATA TRANS H

Read Data Multiplexer

The read data multiplexer selects the proper data and places them on the BDAL bus when the processor inputs DRCSR, DROUTBUF or interrupt vectors; DRINBUF contents are gated onto the bus separately. The select signals (previously described) and VECTOR H, produced by the interrupt logic, control read data selection.

DRCSR Functions

The control/status register (DRCSR) has separate functions. Four of the six significant DRCSR bits can be involved in either write or read operations. The remaining two bits, 7 and 15, are read-only bits that are controlled by the external device via the REQ A H and REQ B H signals, respectively. The four read/write bits are stored in the 4-bit CSR latch. They represent CSR0 and CSR1 (DRCSR bits 0 and 1, respectively), which can be used to simulate interrupt requests when used with an optional maintenance cable. INT ENB A and INT ENB B (bits 6 and 5, respectively) enable interrupt logic operation. Note that CSR0 and CSR1 are available to the user's device for any user application.

DRINBUF Input Data Transfer

DRINBUF is an addressable 16-bit read-only register that receives data from the user's device for transmission to the LSI-11 bus. Data to be read are provided by the user's device on the IN0-15 H signal lines. Since the input buffer consists of gating logic rather than a flip-flop register, the user's device must hold the data on the lines until the data input transaction has been completed.

The input data are read during a DATI sequence while bus drivers are enabled by the SEL4IN L signal. The DATA TRANS pulse that is sent to the user's device by the function select logic informs the device of the transaction. Input data can be removed on the trailing edge of this pulse.

DROUTBUF Output Data Transfer

DROUTBUF comprises two 8-bit latches, enabling either 16-bit word or 8-bit byte output transfers. Two SEL2 signals function as clock signals for the latches. When in a DATO bus cycle, both signals clock data from the internal BRD0-15 H bus into the latches. However, when in a DATOB cycle, only one signal clocks data into an 8-bit latch, as determined by address bit 0 previously stored during the addressing portion of the bus cycle.

The NEW DATA RDY H pulse generated by the function select logic is sent to the user's device to inform the device of the data transaction. The data can be input to the device on the trailing edge of this pulse.

Interrupts

The DRV11 contains LSI-11 bus-compatible interrupt logic that allows the user's device to generate interrupt requests. Two independent interrupt request signals (REQ A H and REQ B H) are capable of requesting processor service via separate interrupt vectors. In addition, DRCSR contains two interrupt enable bits (INT EN A and INT EN B, bits 6 and 5, respectively), which independently enable or disable interrupt requests. REQ A and REQ B status can be read by the processor in DRCSR bits 7 and 15, respectively. Since separate interrupt vectors are provided for each request, one of the requests could be used to imply that device data is ready for input and the remaining request could be used to imply that the device is ready to accept new data.

An interrupt sequence is generated when a DRCSR INT EN bit (A or B) is set and its respective REQ signal is asserted by the device. The processor responds (if its PS bit 7 is not set) by asserting BDIN L; this enables the device requesting the interrupt to place its vector on the BDAL bus when the interrupt request is acknowledged. The processor then asserts BIAKO L, acknowledging the interrupt request. The DRV11 receives BIAKI L and the interrupt logic generates VECTOR H, which gates the jumper-addressed vector information through the read data multiplexer and bus drivers and onto the LSI-11 bus. The processor then proceeds to service the interrupt request.

Maintenance Mode

The maintenance mode allows the user to check DRV11 operation by installing an optional BC08R cable between connectors J1 and J2. This maintenance cable allows the contents of the output buffer DROUTBUF to be read during a DRINBUF DATI bus cycle. In addition, interrupts can be simulated by using DRCSR bits CSR0 and CSR1. CSR1 is routed via the cable directly to the REQ B H input and CSR0 is routed to the REQ A H input. By setting or clearing INT EN A, INT EN B, and CSR0 and CSR1 bits in the DRCSR register, a maintenance program can test the interrupt facility.

Initialization

BINIT L is received by a bus driver, inverted, and distributed to DRV11 logic to initialize the device interface. The buffered initialize signal is

available to the user's device via the AINIT H and BINIT H signal lines. DRV11 logic functions cleared by the BINIT signal include DROUT-BUF, DRCSR (bits 0, 1, 5, and 6), and interrupt logic.

CONFIGURATION

The following paragraphs describe how the user can configure the module by inserting or removing jumpers (Figure 2) so that it will function within his system. The jumpers, listed in Table 2, indicate the factory configuration when shipped.

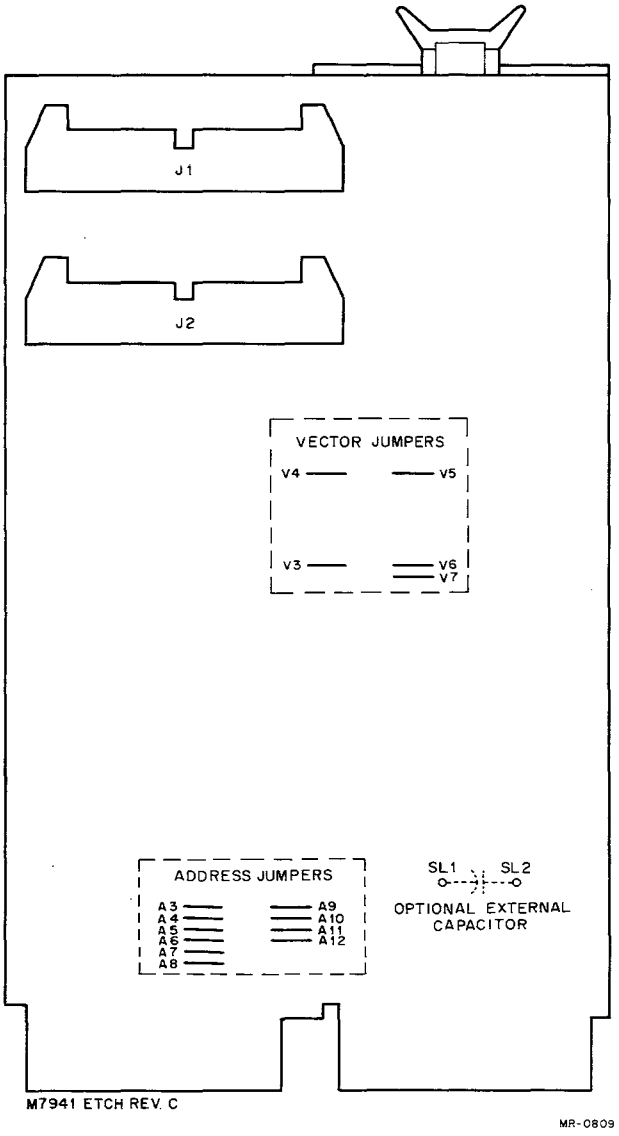


Figure 2 DRV11 Jumper Locations

Table 2 DRV11 PLU Factory Jumper Configuration

Jumper Designation	Jumper State	Function Implemented
A3	R	This arrangement of jumpers A3 through A12 assigns the device address 16777X to the PLU. This address is the starting address of a reserved block in memory bank 7 which is recommeded for user device address assignments. The least significant digit X is hardwired on the module to implement the three PLU device addresses as follows: X = 0 DRCSR address X = 2 Output buffer address X = 4 Input buffer address
A4	R	
A5	R	
A6	R	
A7	R	
A8	R	
A9	R	
A10	R	
A11	R	
A12	I	
V3	I	This factory-installed jumper configuration implements the two interrupt vector addresses 300 and 304 for use as defined by application requirements.
V4	I	
V5	I	
V6	R	
V7	R	

R = Removed, I = Installed

Device Address

Addresses for the DRV11 can range from 16000X through 17777X. The three least significant bits are predetermined for the other DRV11 registers as shown in Table 3 and Figure 3. Addresses within 177560 to 177566 are reserved for the console device and should not be used for the DRV11.

Table 3 Standard Assignments

Description	Mnemonic	Read/ Write	First Module Address	Second Module Address
Register				
Control and Status	DRCSR	R/W	167770	167760
Output Buffer	DROUTBUF	R/W	167772	167762
Input Buffer	DRINBUF	R	167774	167764
Interrupt				
Request A	REQ A	—	300	310
Request B	REQ B	—	304	314

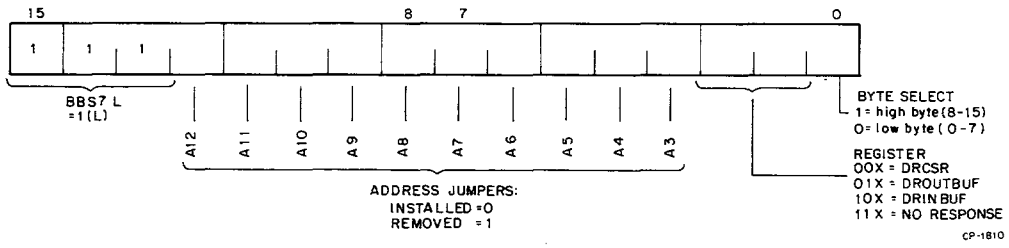


Figure 3 DRV11 Device Address Selection

Jumpers for bits 3 through 12 are installed or removed to produce the 16-bit address word shown in Figure 3. The appropriate jumpers are removed to produce logical 1 bits, and installed to produce logical 0 bits.

Vectors

The two vectors are selected within the range of 000 to 374 by using jumpers V3 to V7. Vector bits 3 through 7 are selected by the user to form the vector as described in Figure 4. The factory configuration sets the interrupt vector for 300 as shown in Table 3 and Figure 4.

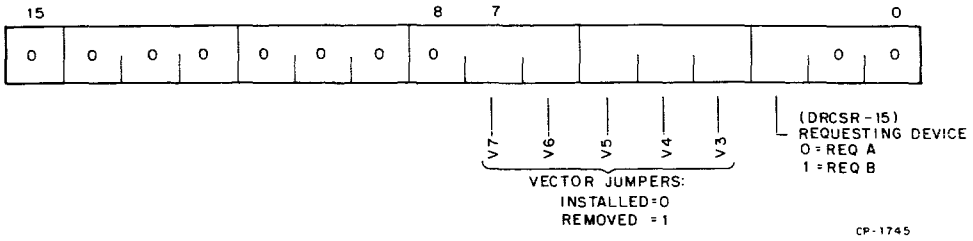


Figure 4 DRV11 Interrupt Vector

Registers

The word format for the control and status register (DRCSR) is shown in Figure 5 and described in Table 4.

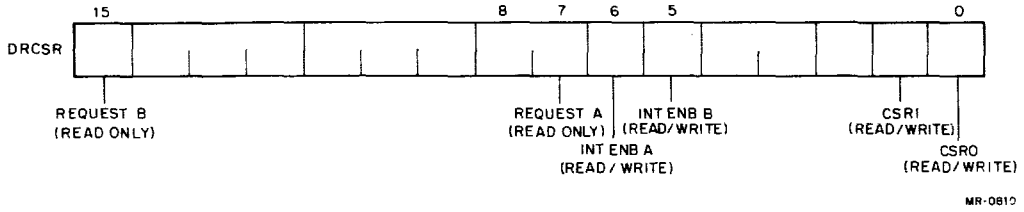


Figure 5 DRCSR Word Format

Table 4 DRCSR Word Formats

Bit: 15 **Name:** Request B.

Function: This bit is under control of the user's device and may be used to initiate an interrupt sequence or to generate a flag that may be tested by the program.

When used as an interrupt request, it is asserted by the external device and initiates an interrupt provided the INT ENB B bit (bit 5) is also set. When used as a flag, this bit can be read by the program to monitor external device status.

When the maintenance cable is used, the state of this bit is dependent on the state of CSR1 (bit 1). This permits checking interface operation by loading a 0 or 1 into CSR1 and then verifying that Request B is the same value.

Read-only bit. Cleared by INIT when in maintenance mode.

Bit: 14-8 **Name:** Not used.
Function: Read as 0.

Bit: 7 **Name:** Request A.
Function: Performs the same function as Request B (bit 15) except that an interrupt is generated only if INT ENB A (bit 6) is also set.

When the maintenance cable is used, the state of Request A is identical to that of CSR0 (bit 0).

Read-only bit. Cleared by INIT when in maintenance mode.

Bit: 6 **Name:** INT ENB A.
Function: Interrupt enable bit. When set, allows an interrupt request to be generated, provided Request A (bit 7) becomes set.

Bit: 5 **Name:** INT ENB B.
Function: Interrupt enable bit. When set, allows an interrupt sequence to be initiated, provided Request B (bit 15) becomes set.

Bit: 4-2 **Name:** Not used.
Function: Read as 0.

Bit: 1 **Name:** CSR1.
Function: This bit can be loaded or read (under program control) and can be used for a user-defined command to the device (appears only on connector number 1).

When the maintenance cable is used, setting or clearing this it causes an identical state in bit 15 (request B). This permits checking operation of bit 15 which cannot be loaded by the program.

Can be loaded or read by the program (read/write bit). Cleared by INIT.

Bit: 0 **Name:** CSR0.
Function: Performs the same functions as CSR1 (bit 1) but appears only on connector number 2.

When the maintenance cable is used, the state of this bit controls the state of bit 7 (Request A).

Read/write bit; cleared by INIT

The word format for the transmit output buffer (DROUTBUF) is shown in Figure 6 and defined in Table 5.

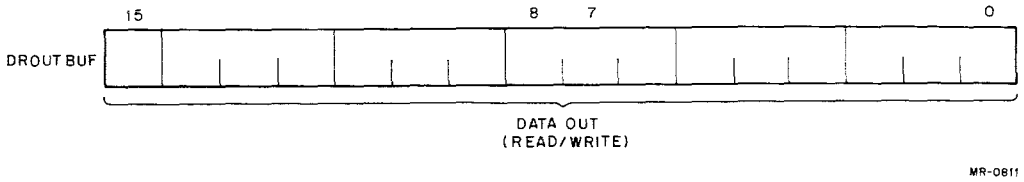


Figure 6 DROUTBUF Word Format

Table 5 DROUTBUF Word Format

Bit: 15-0 **Name:** Output Data Buffer.
Function: Contains a full 16-bit word or one or two 8-bit bytes; high byte = 15-8; low byte = 7-0.

Loading is accomplished under a program-controlled DATO or DATOB bus cycle. It can be read under a program-controlled DATI cycle.

The word format for the receiver input buffer (DRINBUF) is shown in Figure 7 and defined in Table 6.

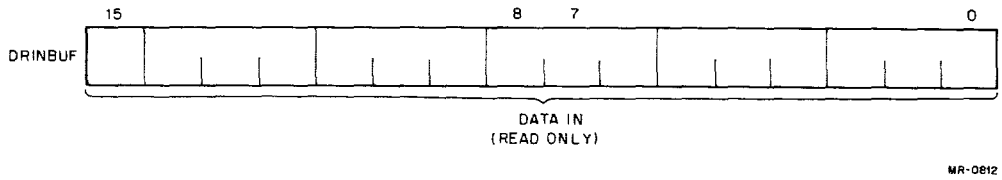


Figure 7 DRINBUF Word Format

Table 6 DRINBUF Word Format

Bit: 15-0 **Name:** Input Data Buffer.
Function: Contains a full 16-bit word or one or two 8-bit bytes. The entire 16-bit word is read under a program-controlled DATI bus cycle.

DRV11

Installation

Prior to installing the DRV11 on the backplane, first establish the desired priority level for the backplane slot installation. Check that proper device address vector jumpers are installed. The DRV11 can then be installed on the backplane. Connection to the user's device is via optional cables.

Interfacing to the User's Device

Interfacing the DRV11 to the user's device is via the two board-mounted H854 40-pin male connectors. Pins are located as shown in Figure 8. Signal pin assignments for input interface J2 (connector number 2) and output interface J1 (connector number 1) are listed in Table 7. Optional cables and connectors for use with the DRV11 include:

BC08R-01—Maintenance cable; 40-conductor flat with H856 connectors on each end.

*BC07D-X**—Signal cable; two 20-conductor ribbon cables with a single H856 connector on one end; remaining end is terminated by the user. Available in lengths of 3, 4.6, and 7.6 m (10, 15, and 25 ft).

* The -X in the cable number denotes length in feet, -10, -12, -20. For example, a 10-ft BC07D cable would be ordered as BC07D-10.

*BC04Z-X**—Flat 40-conductor signal cable with a single H856 connector on one end; remaining end is terminated by the user. Available in lengths of 3, 4.6, and 7.6 m (10, 15, and 25 ft).

*BCV11-X**—Flat, 40-conductor, twisted pair cable with a single H856 connector on one end. The remaining end is connected by the user. Available in lengths of 1.5, 3, 4.6, 6.1, and 7.6 m (5, 10, 15, 20, and 25 ft).

H856—Socket, 40-pin female, for user-fabricated cables.

When using the BC07D cable, connect the free end of the ribbon cables using the wiring data contained in Table 8.

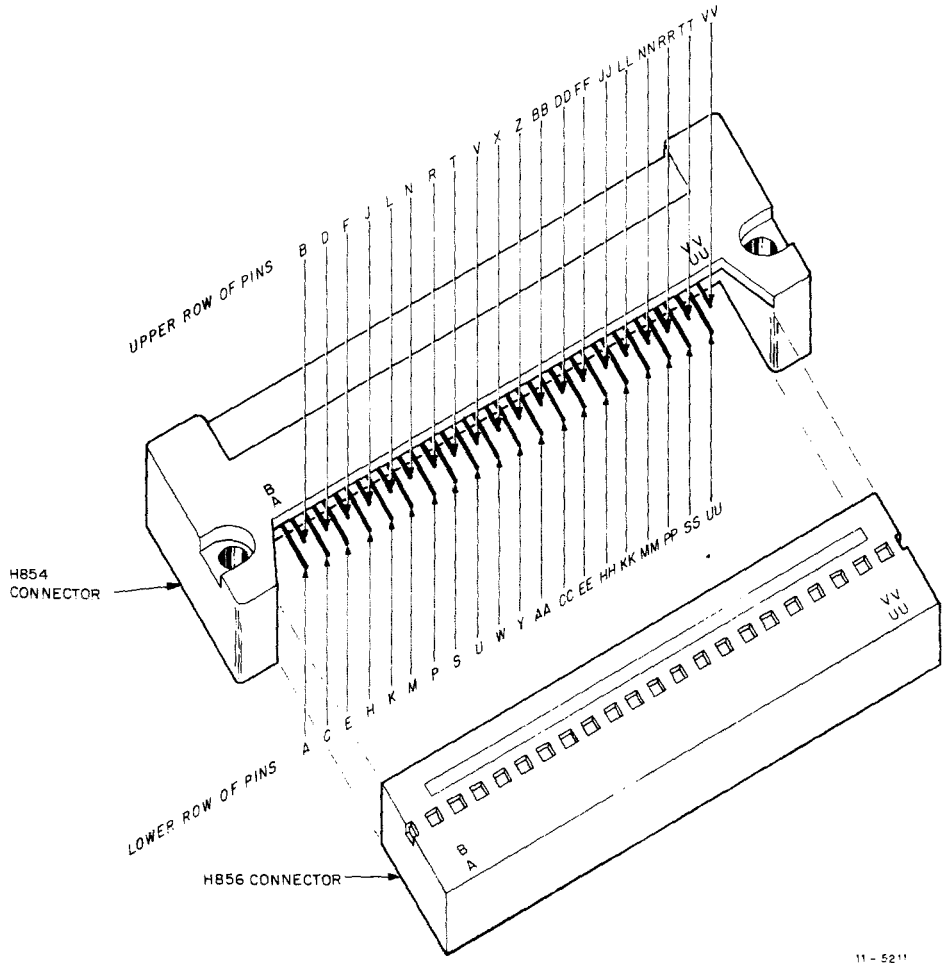


Figure 8 J1 or J2 Connector Pin Locations

DRV11

Table 7 DRV11 Input and Output Signal Pins

Inputs			Outputs		
Signal	**Connector**	**Pin**	**Signal**	**Connector**	**Pin**
IN00	J2	TT	OUT00	J1	C
IN01	J2	LL	OUT01	J1	K
IN02	J2	H, E	OUT02	J1	NN
IN03	J2	BB	OUT03	J1	U
IN04	J2	KK	OUT04	J1	L
IN05	J2	HH	OUT05	J1	N
IN06	J2	EE	OUT06	J1	R
IN07	J2	CC	OUT07	J1	T
IN08	J2	Z	OUT08	J1	W
IN09	J2	Y	OUT09	J1	X
IN10	J2	W	OUT10	J1	Z
IN11	J2	V	OUT11	J1	AA
IN12	J2	U	OUT12	J1	BB
IN13	J2	P	OUT13	J1	FF
IN14	J2	N	OUT14	J1	HH
IN15	J2	M	OUT15	J1	JJ
REQ B	J2	S	REQ A	J1	LL
DATA TRANS	J2	C	NEW DATA RDY	J1	VV
CSR0	J2	K	CSR1	J1	DD
INIT	J2	RR, NN	INIT	J1	P

Table 8 BC07D Signal Cable Connections

Cable 1 (connector pins B-VV)				Cable 2 (connector pins A-UU)		
Wire Color	**Pins**	**J1 Signal**	**J2 Signal**	**Pins**	**J1 Signal**	**J2 Signal**
blk	B	open	open	A	open	open
brn	D	open	open	C	OUT00	DATA TRANS
red	F	open	open	E	open	IN02

Table 8 BC07D Signal Cable Connections (Cont)

Cable 1 (connector pins B-VV)				Cable 2 (connector pins A-UU)		
Wire Color	Pins	J1 Signal	J2 Signal	Pins	J1 Signal	J2 Signal
orn	J	GND	GND	H	open	IN02
yel	L	OUT04	GND	K	OUT01	CSR0
grn	N	OUT05	IN14	M	GND	IN15
blu	R	OUT06	GND	P	INIT	IN13
vio	T	OUT07	GND	S	GND	REQ B
gry	V	GND	IN11	U	OUT03	IN12
wht	X	OUT09	GND	W	OUT08	IN10
blk	Z	OUT10	IN08	Y	GND	IN09
brn	BB	OUT12	IN03	AA	OUT11	GND
red	DD	CSR1	GND	CC	GND	IN07
orn	FF	OUT13	open	EE	GND	IN06
yel	JJ	OUT15	GND	HH	OUT14	IN05
grn	LL	REQ A	IN01	KK	GND	IN04
blu	NN	OUT02	INIT	MM	GND	GND
vio	RR	OUT02	INIT	PP	GND	GND
gry	TT	open	IN00	SS	GND	GND
wht	VV	NEW DATA RDY	open	UU	GND	GND

Table 9 BC08R Maintenance Cable Signal Connection

J2		J1	
Pin	**Name**	**Pin**	**Name**
VV	OPEN	A	OPEN
UU	GND	B	OPEN
TT	IN00	C	OUT00
SS	GND	D	OPEN
RR	INIT H	E	OPEN
PP	GND	F	OPEN
NN	INIT	HH	OPEN
MM	GND	J	GND
LL	IN01	K	OUT01
KK	IN04	L	OUT04
JJ	GND	M	GND
HH	IN05	N	OUT05
FF	OPEN	P	INIT H
EE	IN06	R	OUT06
DD	GND	S	GND
CC	IN07	T	OUT07
BB	IN03	U	OUT03
AA	GND	V	GND
Z	IN08	W	OUT08
Y	IN09	X	OUT09
X	GND	Y	GND
W	IN10	Z	OUT10
V	IN11	AA	OUT11
U	IN12	BB	OUT12
T	GND	CC	GND
S	REQ B	DD	CSR1
R	GND	EE	GND
P	IN13	FF	OUT13
N	IN14	HH	OUT14
M	IN15	JJ	OUT15
L	GND	KK	GND
K	CSR0	LL	REQ A
J	GND	MM	GND

Table 9 BC08R Maintenance Cable Signal Connection (Cont)

J2		J1	
Pin	**Name**	**Pin**	**Name**
H	IN02	NN	OUT02
F	OPEN	PP	GND
E	IN02	RR	OUT02
D	OPEN	SS	GND
C	DATA TRANS	TT	OPEN
B	OPEN	UU	GND
A	OPEN	VV	NEW DATA RDY

Output Data Interface

The output interface is the 16-bit buffer (DROUTBUF). It can be either loaded or read under program control. When loaded by a DATO or DATOB bus cycle, the NEW DATA RDY H pulse is generated to inform the user's device of the data transfer. The trailing edge of this positive-going pulse should be used to strobe the data into the user's device in order to allow data to settle on the interface cable. The system initialize signal (BINIT L) will clear DROUTBUF.

All output signals are TTL levels capable of driving eight unit loads except for the following:

New Data Ready = 10 unit loads
Data Transmitted = 30 unit loads
INIT (Initialize) = 10 units per connector

Input Data Interface

The input interface is the 16-bit DRINBUF read-only register, made up of gated bus drivers that transfer data from the user's device onto the LSI-11 bus under program control. DRINBUF is not capable of storing data; hence the user must keep input data on the IN lines until read by the processor. When read, the DRV11 generates a positive-going DATA TRANS H pulse which informs the user's device that the data has been accepted. The trailing edge of the pulse indicates that the input transfer has been completed.

All input signals are one standard TTL unit load; inputs are protected by diode clamps to ground and +5 V.

Request Flags

Two signal lines (REQ A H and REQ B H) can be asserted by the user's device as flags in the DRCSR word. REQ B is available via connector number 2, and it can be read in DRCSR bit 15. REQ A is available via connector number 1, and it can be read in DRCSR bit 7. Two DRCSR interrupt enable bits, INT ENB A (bit 6) and INT ENB B (bit 5), allow automatic generation of an interrupt request when their respective REQ A or REQ B signals are asserted. Interrupt enable bits can be set or reset under program control.

In a typical application, REQ A and REQ B are generated by request flip-flops in the user's device. The user's request flip-flop must be set when servicing is required and must be cleared by the trailing edge of NEW DATA RDY or DATA TRANS when the appropriate data transaction has been completed.

This timing is shown in Figure 9. The logic required by the user to implement this is shown in Figure 10. The logic consists of a flip-flop that is set by the User Request pulse, which indicates that the user's device is requesting a transfer. The flip-flop is reset by the trailing edge of the NEW DATA RDY signal or the DATA TRANS signal.

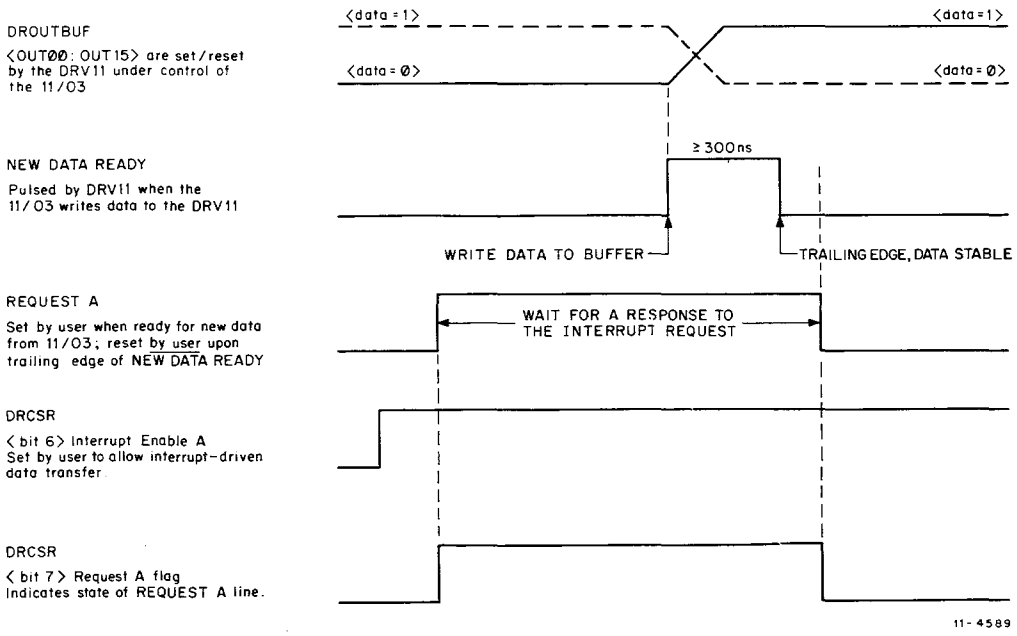


Figure 9 DRV11 Interface Signal Sequence

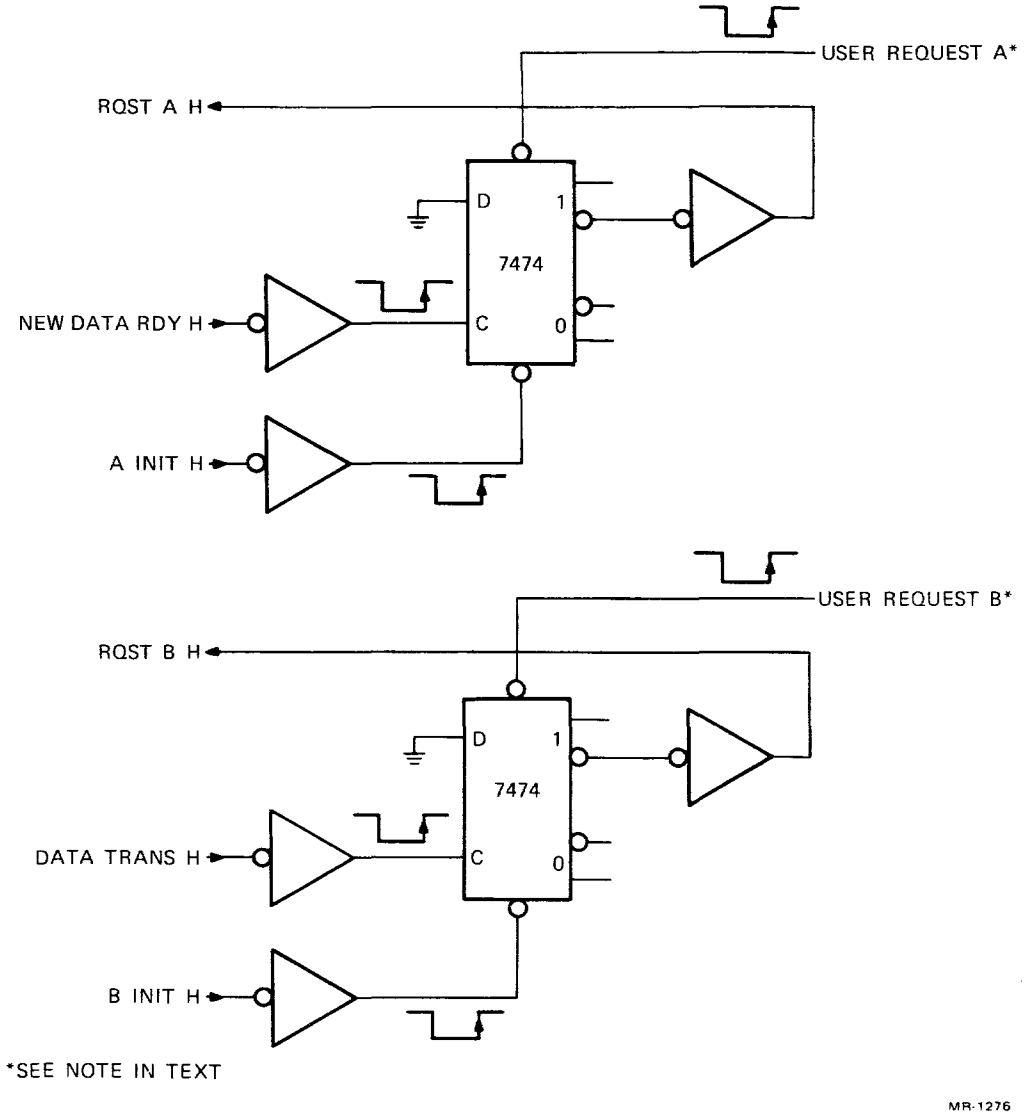


Figure 10 User Request Logic

NOTE

The User Request signal must return to the "high" state prior to the occurrence of the trailing edge of NEW DATA RDY or DATA TRANS. The leading edge of NEW DATA RDY or DATA TRANS can be used for this purpose. In most applications, a pulse on the User Request Line of less than 10 μs is adequate.

Initialization

The BINIT L processor-generated initialize signal is applied to DRV11 circuits for interface logic initialization. It is also available to the user's circuits via connectors J1 and J2 as follows:

Connector/Pin	Signal
J1/P	AINIT H
J2/RR	BINIT H
J2/NN	BINIT H

An active BINIT L signal will clear DROUTBUF data, DRCSR bits 6, 5, 1, 0, bits 16 and 7 (when the maintenance cable is connected), and interrupt request and interrupt acknowledge flip-flops.

NEW DATA RDY and DATA TRANS Pulse Width Modification

An optional capacitor can be added by the user to the DRV11 module to extend the pulse width of both the NEW DATA RDY and DATA TRANS pulse widths. The capacitor can be added in the location shown in Figure 2 to produce the approximate pulse widths listed below.

Optional External	Approximate Pulse Width (ns)	
Capacitance (F)	NEW DATA RDY	DATA TRANS
None	350	1150
0.0047	750	1550
0.01	1550	2400
0.02	2330	3200
0.03	3150	3900

BC08R Maintenance Cable

When using the optional BC08R maintenance cable, the connections listed in Table 9 are provided. Cable connectors P1 and P2 are connected to DRV11 connectors J1 and J2, respectively. Note that CSR0 (J2-K), which can be set or reset under program control, is routed to the REQ A input (J1-LL); similarly, CSR1 (J1-DD) is routed to REQ B (J2-S). Hence, a maintenance program can output data to DROUTBUF and read the same data via the cable and DRINBUF. DRCSR bits 0 (CSR0) and 1 (CSR1) can be used to simulate REQ A and REQ B signals, respectively. If the appropriate INT ENB bit (DRCSR bits 5 or 6) is set, the simulated signal will generate an interrupt request. Note that the BC08R cable must incorporate a half-twist when connected to J1 and J2.

DRV11-B

DRV11-B DMA INTERFACE

INTRODUCTION

The DRV11-B is a general purpose direct memory access (DMA) interface used to transfer data directly between the LSI-11 system memory and an I/O device. The interface is programmed by the processor to move variable length blocks of 8- or 16-bit data words to or from specified locations in memory by means of the LSI-11 bus. Once programmed, no processor intervention is required. The DRV11-B can transfer up to 250K 16-bit words per second in single cycle mode and up to 500K 16-bit words per second in burst mode. The control structure also allows read-modify-write operations.

FEATURES

- Buffered input/output data
- Data transfer rate of up to 500K 16-bit words per second
- Each Transfer of up to 32K 16-bit words
- Compatible with LSI-11 bus
- 16-bit CSR available for control and status functions
- Two 40-pin I/O connectors mounted on module for interface with user's hardware
- Switch-selectable device address and interrupt vector

SPECIFICATIONS

Identification	M7950
Size	Quad
Power	+5 Vdc ±5% at 1.9 A
Bus Loads	
AC	3.3
DC	1

DESCRIPTION

Basic functions that make up the DRV11-B are shown in Figure 1. The following paragraphs describe the DRV11-B registers, the bus operations required for DMA transfers and the DMA transfer timing.

DRV11-B Registers

The DRV11-B contains five registers:

Word Count Register (WCR)
Bus Address Register (BAR)
Control/Status Register (CSR)
Output Data Buffer Register (ODBR)
Input Data Buffer Register (IDBR)

Word Count Register (WCR) — The WCR is a 16-bit read/write register that controls the number of transfers. This register is loaded (under program control) with the 2's complement of the number of words to be transferred. At the end of each transfer, the word count register is incremented. When the contents of the WCR are incremented to zero, transfers are terminated. READY is set, and if enabled, an interrupt is requested. The WCR is word-addressable only.

Bus Address Register (BAR) — The BAR is a 15-bit read/write register. This register is loaded (under program control) with a bus address (not including the address bit 0) which specifies the location to or from which data is to be transferred. The BAR is incremented acros 32K memory boundaries via the extended address feature of the DRV11-B. Systems with only 16 address bits will "wrap-around" to location zero when the extended address bits are incremented. The BAR is word-addressable only.

Control/Status Register — The CSR is a 16-bit register used to control the function and monitor the status of the interface. Bit 0 is a write-only bit and always reads as zero. Bits 1-6 and bits 8 and 12 are read/write bits; bits 7, 9-11, and 13-15 are read-only bits. Bit 14 can be written to a zero. Bits 4 and 5 are the extended addressing bits. The CSR is both byte- and word-addressable.

Input and Output Data Buffer Registers (DBRs) — The two DBRs are 16-bit registers. The input DBR is a read-only register and the output DBR is a write-only register. Data is loaded into the input DBR by the user's device and subsequently transferred into memory under DMA control by the DRV11-A , or under program control by the processor. Conversely, data is written into the output DBR from memory under DMA control by the DRV11-B, or under program control by the processor, and read by the user's device. The input and output DBRs interface to the user's device by means of two separate 40-pin I/O connectors. These connectors may be cabled together (for maintenance purposes) to function as a read/write register. The input and output DBRs share the same bus address and are byte- and word-addressable.

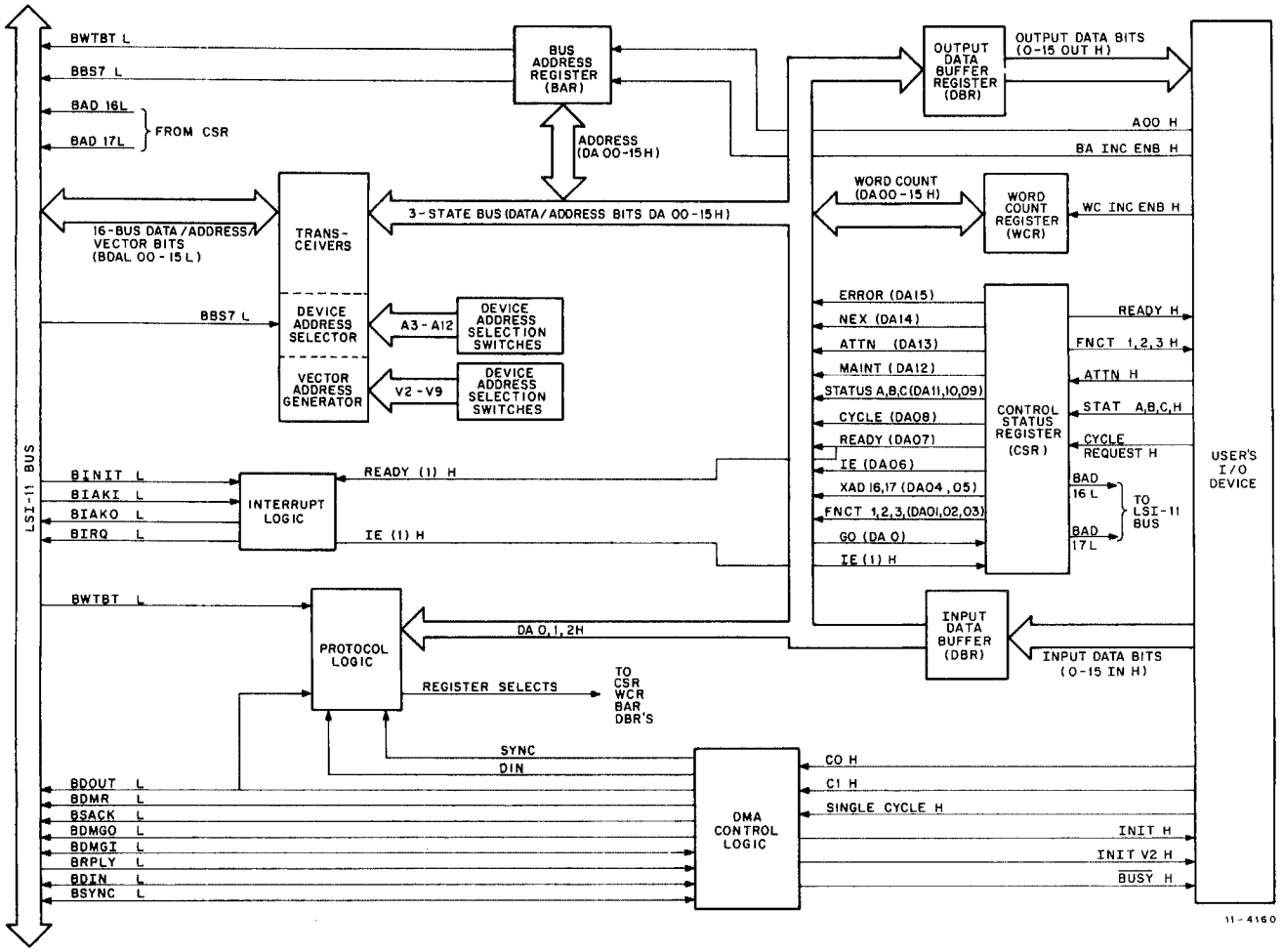


Figure 1 DRV11-B Logic Block Diagram

User's I/O Device to System Memory Transfer (DATO or DATOB)

Data transfers from the user's I/O device to the memory are DMA transfers. Figure 2 illustrates the data flow for a DMA DATO or DATOB cycle. Referring to Figure 1, DMA transfers are initialized under program control by loading the DRV11-B WCR (in 2's complement) with a count equal to the number of words to be transferred; loading the BAR with the starting memory address for word storage; and setting the CSR for transfers.

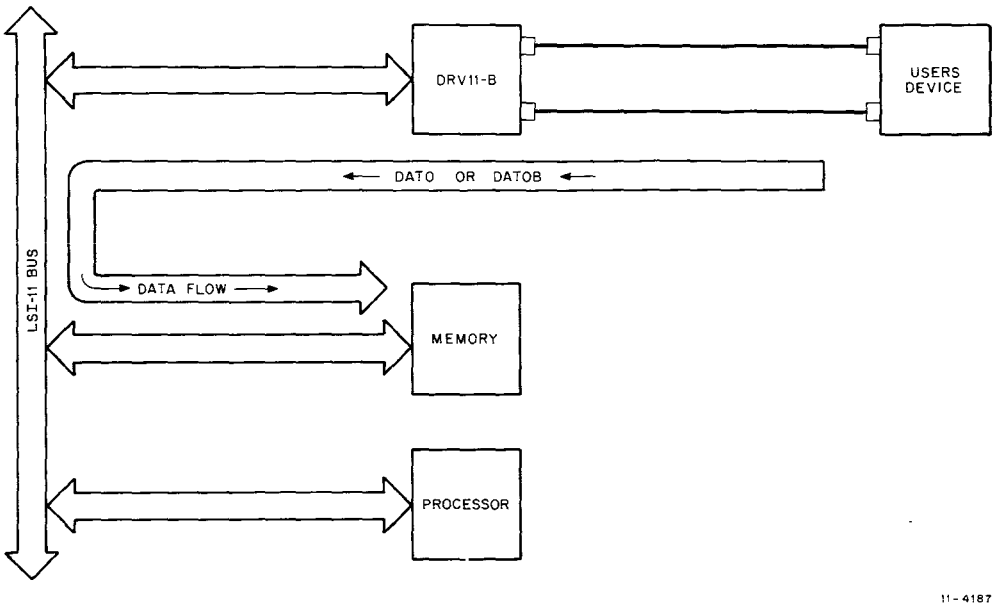


Figure 2 DMA DATO/DATOB Data Flow Diagram

When the GO bit of the CSR is written to a "one," READY goes low, the user's I/O device conditions the A00, BA INC ENB, WC INC ENB, ATTN, SINGLE CYCLE (high for normal DMA transfers), and the C0, C1 (Table 6) lines, and then asserts CYCLE REQUEST. The input data bits and the control bits (C0, C1, and SINGLE CYCLE) are latched into the respective DRV11-B registers. CYCLE REQUEST sets CYCLE and causes the DRV11-B to assert BDMR, which makes an LSI-11 bus request and causes BUSY to go low. In response to BDMR, the processor asserts BDMGO which is received as BDMGI. The DRV11-B becomes bus master and asserts BSACK and negates BDMR. The processor then terminates the bus grant sequence by negating BDMGO.

When the DRV11-B becomes bus master, a DATI or DATIO bus cycle is performed (a DATI is described). The DRV11-B places the address of the memory location from which the first word is taken on the BDAL

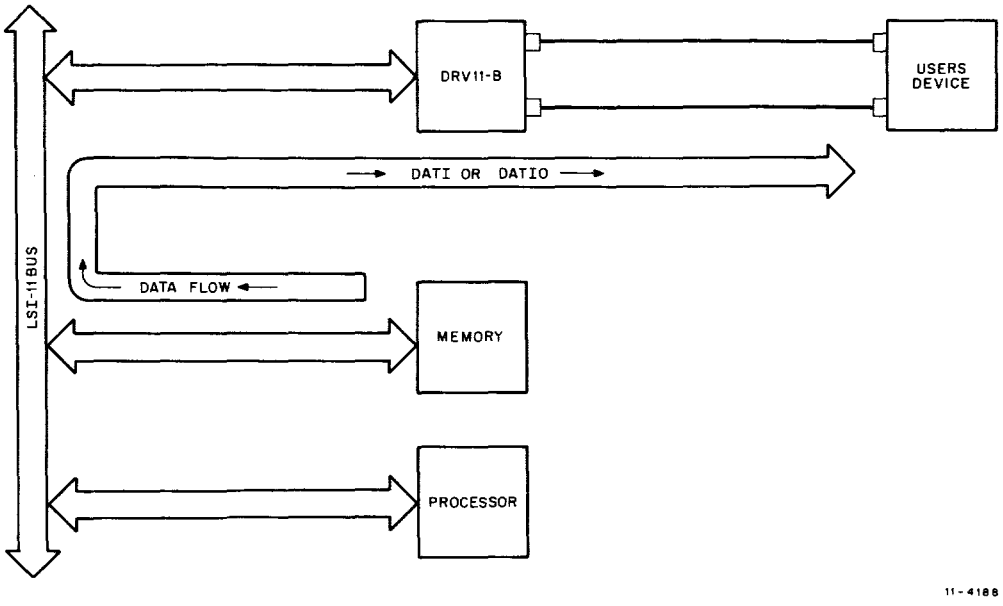


Figure 3 DMA DATIO/DATI Data Flow Diagram

lines and asserts BSYNC. Memory decodes and latches the address. The DRV11-B then removes the address from the BDAL lines and asserts BDIN. Input data is now placed on the BDAL lines by the memory and the memory asserts BRPLY. The input data is accepted by the DRV11-B and BDIN is negated. Memory negates BRPLY and the DRV11-B negates BSACK and BSYNC to terminate the bus cycle and release the bus. The output data bits for the user's I/O device are stored in the DRV11-B output data buffer register. These bits can be read by the user's device at the low-tc-high transition of BUSY.

At the end of the first transfer, the DRV11-B WCR and BAR are incremented, BUSY goes high and READY remains low. The user's device can initiate another DATI or DATIO cycle by again setting CYCLE REQUEST. DMA transfers to the user's device can continue until the WCR increments to zero and causes an interrupt request to be generated.

DMA Transfers

The DRV11-B interface is designed for DMA transfers which the user can accomplish in several ways. DMA transfers are always set up by the processor when it loads the BAR and WCR and sets the READY bit. The user then has the option of initiating transfers either by program control (setting the GO bit in the CSR) or by the user device asserting CYCLE REQUEST for 1 μs minimum.

Type of I/O to be Performed — The user has the option of selecting DATI, DATO, DATOB, or DATIO bus cycles by asserting C0 and C1 per Table 6. Note that if byte transfers are being performed, the byte address bit (A00) must be manipulated by the user. (Refer to the section entitled "Word or Byte Transfers.")

Burst Mode vs. Single Cycle DMA — Single cycle DMA allows the asynchronous transfer of data to or from the user's device. Each time the user's device is ready for a transfer, the user asserts CYCLE REQUEST for 1 μs. A DMA cycle is requested from the LSI-11 bus, and when the bus is granted to the DRV11-B, the BUSY line is asserted to inform the user that a data transfer is underway. The user must set up input data when CYCLE REQUEST is asserted, and hold it valid until the next assertion of CYCLE REQUEST. The user must strobe output data out of the DRV11-B on the rising edge of BUSY. The data will be valid 250 ns minimum before the rising edge of BUSY. (Figures 4 and 5 are detailed timing diagrams.)

Burst mode DMA allows synchronous transfer of data between a user's device and the DRV11-B. Once a DMA sequence is started (either by the user or by the processor), data will be transferred at a synchronous rate of 500K words per second. One data word will be transferred every 2 μs. The user must strobe data out of the DRV11-B into the user's device on the rising edge of BUSY. The data to be transferred to the DRV11-B must be set up when the READY line goes low (for the first data transfer) or on the rising edge of BUSY (for subsequent data transfers). (Figures 6 and 7 are detailed timing diagrams.)

Word or Byte Transfers — The DRV11-B can transfer words or bytes to memory. Transfers from memory are always on a word basis; if only one byte is required, the unused bytes are disregarded. To transfer data on a byte basis to memory, the following operations must be performed:

1. A00 must be manipulated by the user to address the proper byte in memory.
2. The byte to be transferred to memory must be input in its proper position in the input word, i.e., if A00 is 1, the byte to be input must be on the input lines IN 8 H through IN 15 H (high byte being transferred).
3. WC INC EN H and BA INC EN H must be asserted during the write cycle of the first byte of each word to inhibit the BAR and WCR from incrementing.

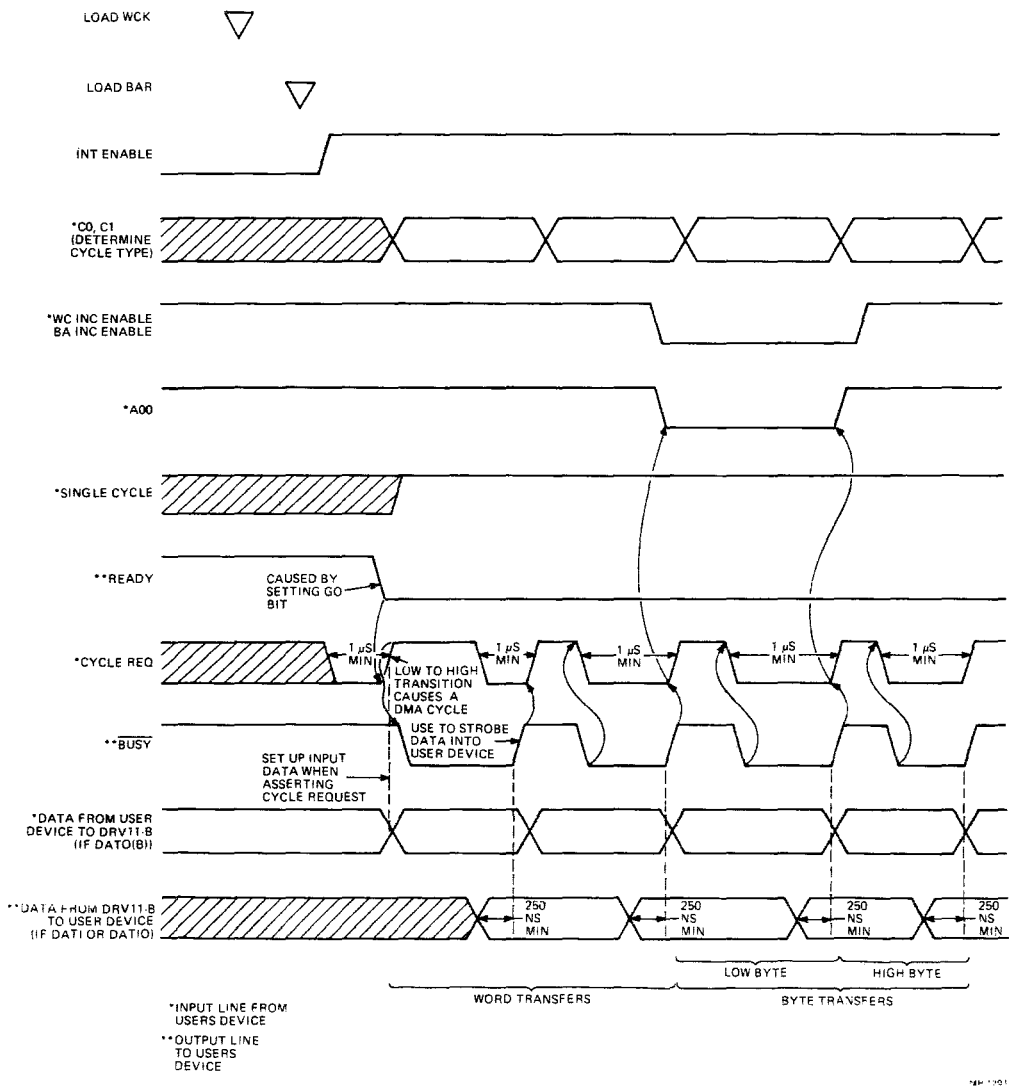


Figure 4 DRV11-B Timing: Single Cycle, Asynchronous, User-Initiated

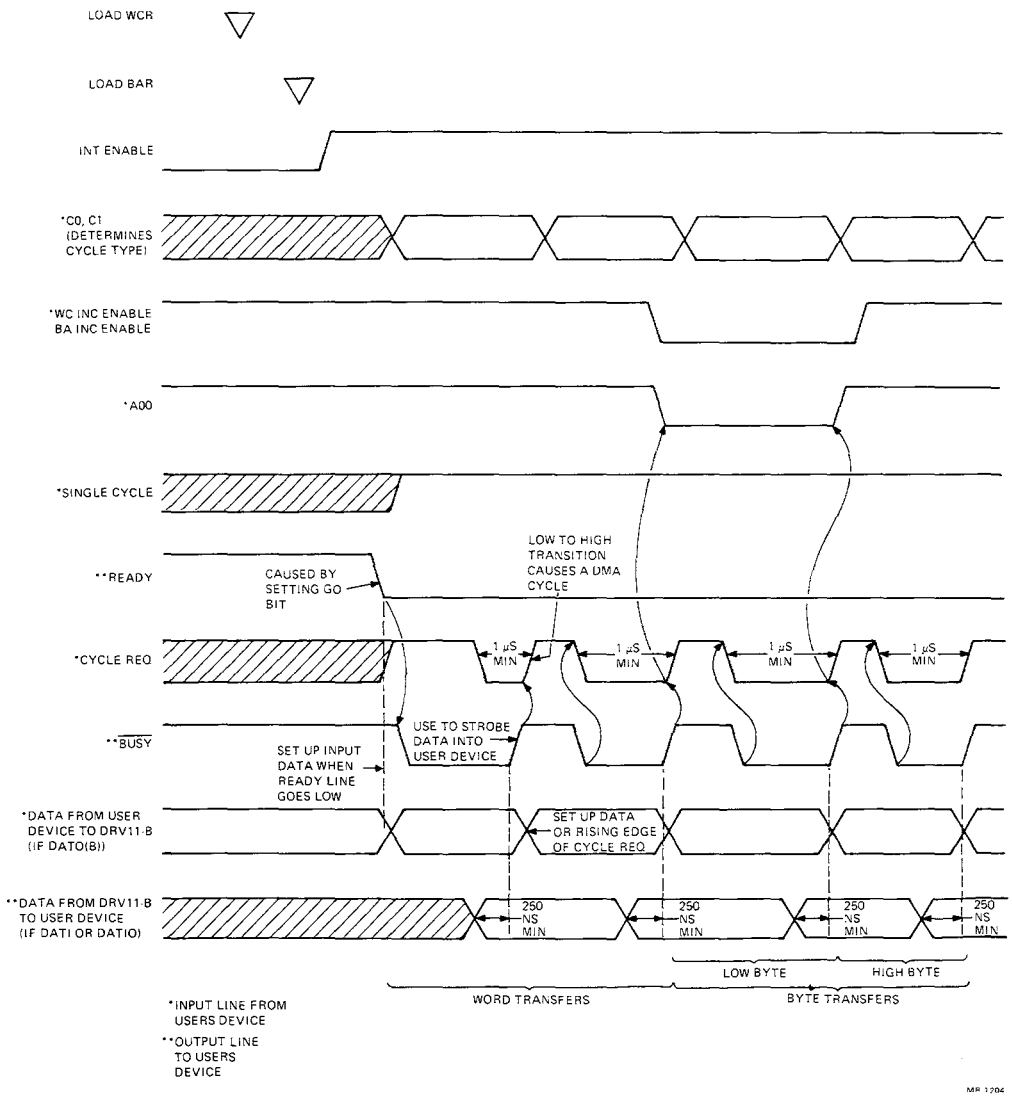


Figure 5 DRV11-B Timing: Single Cycle, Asynchronous, Program-Initiated

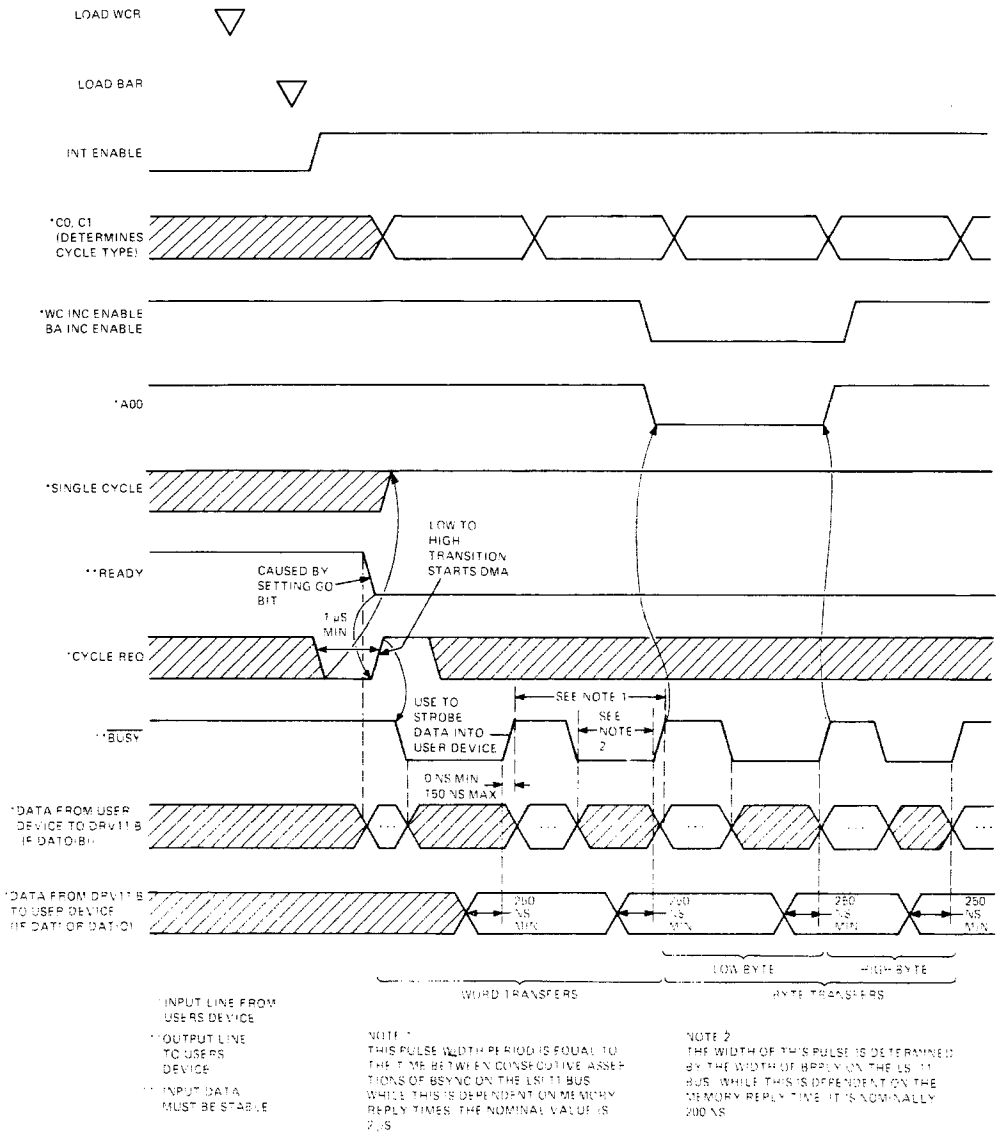


Figure 6 DRV11-B Timing: Burst Mode, User-Initiated

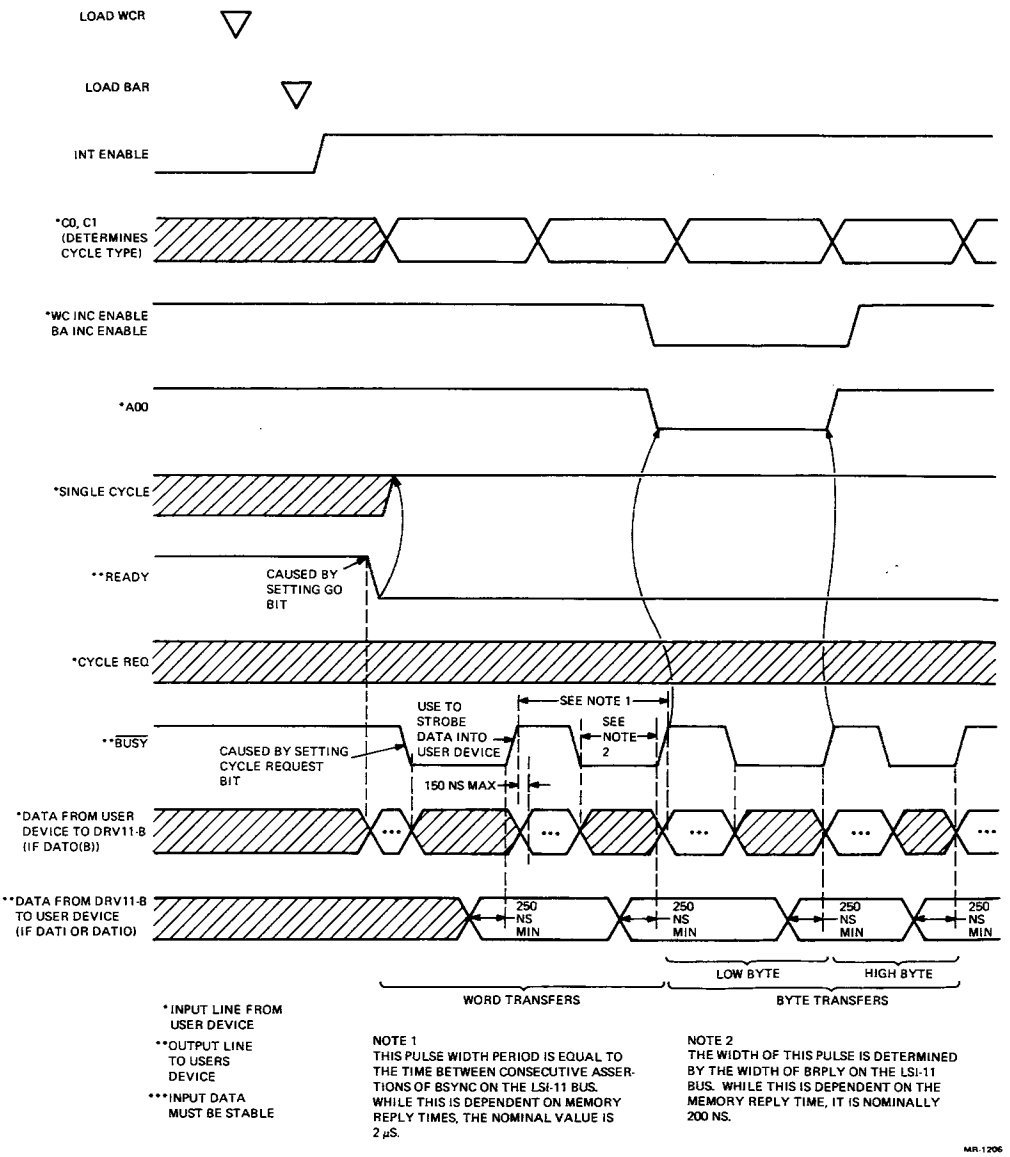


Figure 7 DRV11-B Timing: Burst Mode, Program Initiated

Miscellaneous Signals — Four sets of signals exist to perform handshaking and status exchange between the processor and the user's device. They are:

STATUS A, B, C—These three TTL lines are used to input status to the DRV11-B from the user's device.

FUNCT 1, 2, 3—These three TTL lines are used to output status from the DRV11-B to the user's device.

INIT, INIT V2—INIT is asserted when the LSI-11 bus INIT signal is asserted. INIT V2 is asserted either when the LSI-11 bus INIT is asserted or when FUNCT 2 is a 1.

ATTN—ATTN terminates a DMA transfer. This sets the READY bit and causes an interrupt (if the interrupt enable bit has been set).

DRV11-B

CONFIGURATION

The interface consists of five registers (Table 1): word count register (WCR), bus address register (BAR), control/status register (CSR), input data buffer register (IDBR), and output data buffer register (ODBR). The module also includes bus transceivers and logic for interrupt requests, address control and protocol, and DMA requests.

Table 1 Standard Addresses

Description	Mnemonic	Read/ Write	Address
Register			
Word Count	WCR	R/W	172410
Bus Address	BAR	R/W	172412
Control/Status	CSR	R/W	172414
Input Data Buffer	IDBR	R	172416
Output Data Buffer	ODBR	W	172416
Interrupt			
Interrupt Vector	—	—	124

The DRV11-B contains two switch packs, one to assign an appropriate device address to the DMA interface and one to select an interrupt vector.

The address of both the DRV11-B interface and the interrupt vector is selected by the position of the switches in switch pack S2 and S1, respectively. The location of the switches on the module is shown in Figure 8. The switches are set to the OFF position (open) to select a zero bit and the ON position (closed) to select a one.

Device Address Format

The DRV11-B decodes four addresses, one for each of the registers listed:

Register	Octal Address
WCR	1XXXX0
BAR	1XXXX2
CSR	1XXXX4
DBR	1XXXX6

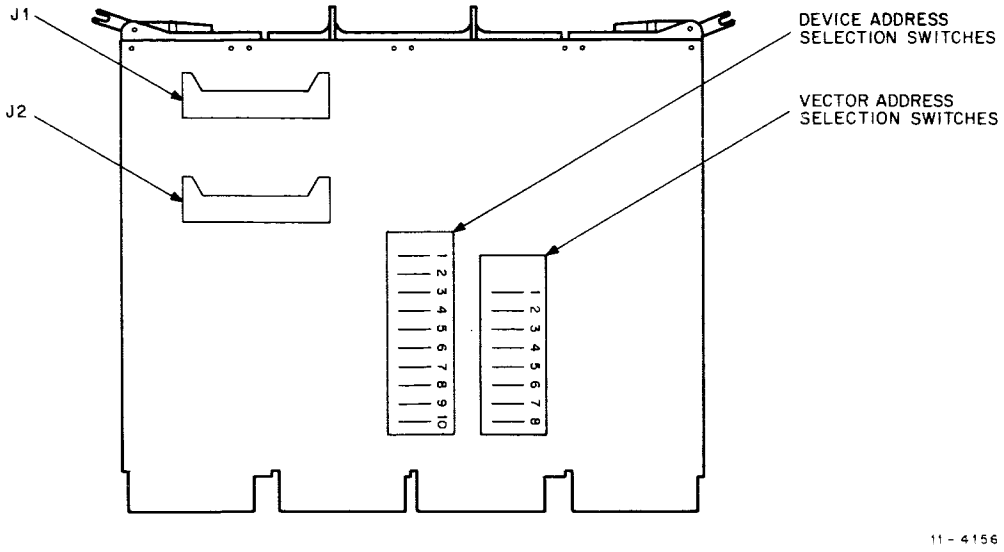


Figure 8 DRV11-B Connector and Switch Locations

Normally, the addresses assigned to the DMA start at 772410_8 and progress upward. Switches S2-1 through S2-10 select the base address as indicated by the X portion of the octal code; the individual registers are decoded by the DMA interface. The relationship between the address format and the switches is shown in Figure 9.

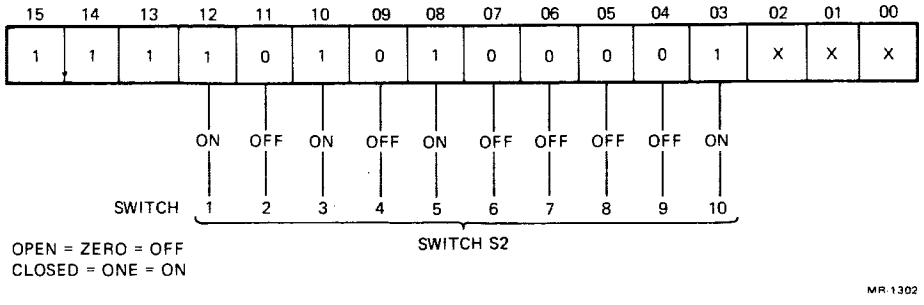


Figure 9 Device Address Switch S2 Selection

Interrupt Vector Selection

The interrupt vectors for the LSI-11 systems are allocated from $0\text{-}774_8$. The recommended vector assigned to the DRV11-B is 124_8. Switches S1-1 through S1-8 are used to select the vector. The relationship between the switches and the vector format is shown in Figure 10.

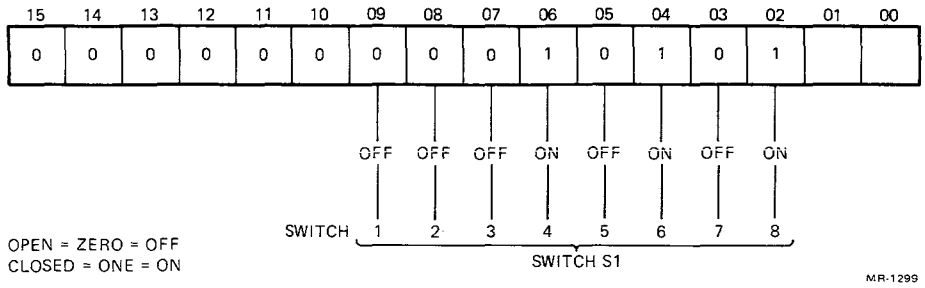


Figure 10 Interrupt Vector Switch S1 Selection

Registers

Each of the five registers can be addressed by the processor. The IDBR and ODBR are assigned the same address and are read-only and write-only, respectively.

Word Count Register (WCR) — The WCR (Figure 11) is a 16-bit read/write counter which is loaded by the program with the 2's complement of the number of words or bytes to be transferred at one time between memory and the I/O device. At the end of each transfer, the WCR is incremented. When the count becomes zero (all 16 bits = 0), the DMA generates an interrupt request. The contents of the WCR can be monitored by the processor program.

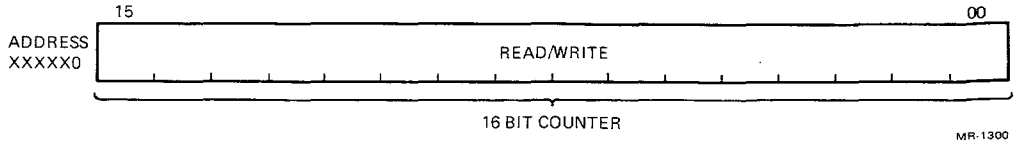


Figure 11 Word Count Register

Bus Address Register (BAR) — The BAR (Figure 12) is a 16-bit read/write register used to generate the bus address which specifies the location to or from which data is to be transferred. The register is incremented after each transfer. It will increment across 32K boundary lines via the extended address bits in the control/status register. Bus address bit 0 is driven by the user device.

Control and Status Register (CSR) — The CSR (Figure 13) contains 16 bits of information used to control the function and monitor the status of the DMA transfers. The information in the CSR can be modified or read by the processor program in either 8-bit bytes or 16-bit words. Table 2 lists and defines each of the 16 bits.

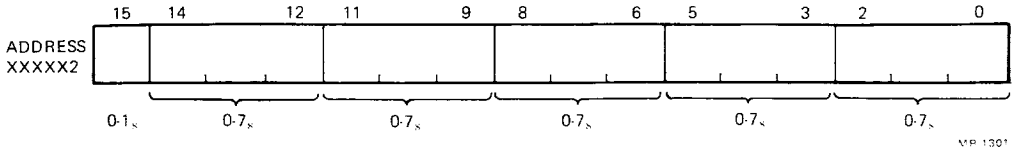


Figure 12 Bus Address Register

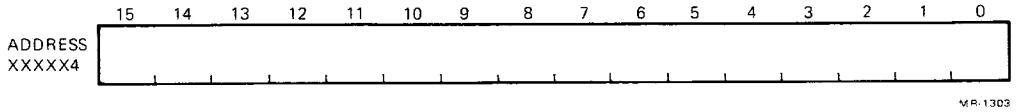


Figure 13 Control/Status Register

Table 2 DRV11-B Control/Status Register Bit Description

Bit: 15 **Name:** Error
Description: (Read-only)
Indicates a special condition
NEX (bit 14)
ATTN (bit 13)

Sets READY (bit 7) and causes interrupt if IE (bit 6) is set.

Cleared by removing the special condition.
NEX is cleared by writing to zero.
ATTN is cleared by the user device.

Bit: 14 **Name:** NEX
Description: (Read/Write zero)
Nonexistent memory indicates that as bus master, the DRV11-B did not receive BRPLY or that a DATIO cycle was not completed.

Sets error (bit 15).

Cleared by INIT or by writing to zero.

Bit: 13 **Name:** ATTN
Description: (Read-only)
Indicates the state of the ATTN user signal.

Sets error (bit 15).

Bit: 12 **Name:** MAINT
Description: (Read/Write)
Maintenance bit used with diagnostic program.

Bit: 11 **Name:** STAT A
Description: (Read-only)
Device status bit that indicates the state of the DSTAT A, B, and C, user signals.

Set and cleared by user control only.

Bit: 10 **Name:** STAT B
Description: (Read-only)
Device status bit that indicates the state of the DSTAT A, B, and C user signals.

Set and cleared by user control only.

Bit: 9 **Name:** STAT C
Description: (Read-only)
Device status bit that indicates the state of the DSTAT A, B, and C user signals.

Set and cleared by user control only.

Bit: 8 **Name:** CYCL
Description: (Read/Write)
Cycle is used to prime a DMA bus cycle.

Bit: 7 **Name:** READY
Description: (Read-only)
Indicates that the DRV11-B is able to accept a new command. Requests an interrupt if IE (bit 6) is set.

Set by INIT.

Bit: 6 **Name:** IE
Description: (Read/Write)
Enables interrupts to occur when READY (bit 7) is set.

Cleared by INIT.

Bit: 5 **Name:** XAD 17
Description: (Read/Write)
Extended access bit 17; cleared by INIT.

Bit: 4 **Name:** XAD 16
Description: (Read/Write)
Extended address bit 16; cleared by INIT.

Bit: 3 **Name:** FNCT 3
Description: (Read/Write)
One of three bits made available to the user device. User defined.
Cleared by INIT.

Bit: 2 **Name:** FNCT 2
Description: (Read/Write)
One of three bits made available to the user device. User defined.

Cleared by INIT.

Bit: 1 **Name:** FNCT 1
Description: (Read/Write)
One of three bits made available to the user device. User defined.

Cleared by INIT.

Bit: 0 **Name:** GO
Description: (Write-only)
Causes "NOT READY" to be sent to the user device indicating a command has been issued. Clears READY (bit 7). Enables DMA transfers.

Input Data Buffer Register (IDBR) — The IDBR (Figure 14) is used for read-only operations. Data is loaded into the register by the user's device. The data may be read from the IDBR as a 16-bit word, an 8-bit high byte or an 8-bit low byte. Transfers are usually via DATO or DATOB DMA bus cycles. The register input connects to J2 mounted on the module.

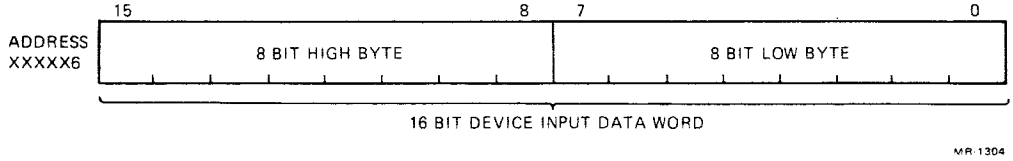


Figure 14 Input Data Buffer Register

Output Data Buffer Register (ODBR) — The ODBR (Figure 15) is used during write-only operations. Data from the LSI-11 bus is loaded into the register under program control and read from the register by the user's device. The register can be loaded with a 16-bit data word or with an 8-bit high byte or an 8-bit low byte. Transfers are usually via DATI or DATIO DMA bus cycles. The output of the register connects to J1 on the module.

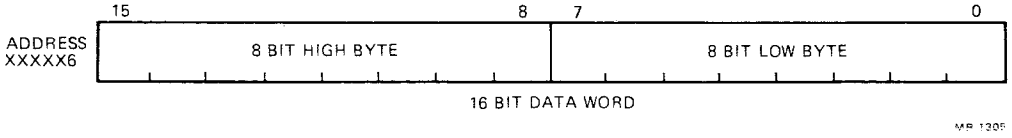


Figure 15 Ouput Data Buffer Register

PROGRAMMING

The DRV11-B interface operates as both a slave and a master device. Prior to becoming bus master, all data transfers out (DATO) or data transfers in (DATI) are in respect to the processor. Once the DRV11-B is granted bus mastership by the processor, all data transfers are in respect to the DRV11-B.

DMA operation is initialized under program control by loading the WCR with the 2's complement of the number of words to be transferred, loading the BAR with the first address to or from which data is to be transferred, or loading the CSR with the desired function bits. After the interface is initialized, data transfers are under control of the DMA logic.

Program Control Transfers

Data transfers may be performed under program control by addressing the IDBR or ODBR and reading or writing data.

DMA Control Transfers

DMA input (DATI) or output (DATO) data transfers occur when the processor clears READY. For a DATO cycle (DRV11-B to memory transfer), the user's I/O device presets the control bits [word count increment enable (WC INC ENB), bus address increment enable (BA INC ENB), C1, C0, A00, and ATTN], and asserts CYCLE REQUEST to gain use of the LSI-11 bus. When CYCLE REQUEST is asserted, input data is latched into the input DBR, the control bits are latched into the DRV11-B DMA control and BUS goes low. A DATI cycle—memory to DRV11-B transfer—is handled in a similar manner, except that the output data is latched into the output DBR at the end of the bus cycle.

When the DRV11-B becomes bus master, a DATO or DATI cycle is performed directly to or from the memory location specified by the BAR. At the end of each cycle, the WCR and BAR are incremented and BUSY goes high while READY remains low. A second DATO or DATI cycle is performed when the user's I/O device again asserts CYCLE REQUEST. DMA transfers will continue until the WCR increments to zero, at which time READY goes high and the DRV11-B generates an interrupt (if interrupt enable is set) to the processor.

If burst mode is selected (SINGLE CYCLE low), only one CYCLE REQUEST is required for the complete transfer of the specified number of data words.

Device Cables and Signals

Data, status, and control signals are transferred between the user's

I/O device and DMA by an input and an output cable assembly. The input cable attaches to connector J2 and the output cable attaches to connector J1. Tables 3 and 4 list the connector pin and designations for each signal. Table 5 lists several recommended cable assemblies that are available from DIGITAL in the lengths indicated. The H856 female connector mates with either J1 or J2 on the DRV11-B. To order cable assemblies in lengths not listed, contact a DIGITAL sales office. Cables up to 15.2 m (50 ft) maximum may be used.

Table 3 DRV11-B Input Connector Signals

J2* Connector Pin	Signal Name	Unit Loads
B	BUSY H	10 (drive)
D	ATTN H	1
F	A00 H	1
J	BA INC ENB H	1
K, L	FNCT 3 H	10 (drive)
N	C0 H	1
R	FNCT 2 H	10 (drive)
T	C1 H	1
V	FNCT 1 H	10 (drive)
DD	08 IN H	
FF	09 IN H	
JJ	10 IN H	
LL	11 IN H	
NN	12 IN H	
RR	13 IN H	
TT	14 IN H	
VV	15 IN H	
CC	07 IN H	
EE	06 IN H	
HH	05 IN H	1
KK	04 IN H	
MM	03 IN H	
PP	02 IN H	
SS	01 IN H	
UU	00 IN H	

* All remaining pins connect in common to logic ground by board etch.

Table 4 DRV11-B Output Connector Signals

J1* Connector Pin	Signal Name	Unit Loads
B	CYCLE REQUEST H	1
D	INIT V2 H	10 (drive)
F	READY H	10 (drive)
J	WC INC ENB H	1
K	SINGLE CYCLE H	1
L	STATUS A	1
N	INIT H	10 (drive)
R	STATUS B	1
T, V	STATUS C	1
DD	08 OUT H	
FF	09 OUT H	
JJ	10 OUT H	
LL	11 OUT H	
NN	12 OUT H	
RR	13 OUT H	
TT	14 OUT H	
VV	15 OUT H	
CC	07 OUT H	
EE	06 OUT H	10 (drive)
HH	05 OUT H	
KK	04 OUT H	
MM	03 OUT H	
PP	02 OUT H	
SS	01 OUT H	
UU	00 OUT H	

* All remaining pins connect in common to the logic ground by board etch.

Table 5 Recommended Cable Assemblies

Cable No.	Connectors	Type	Standard Lengths (ft)
BC07D-XX	H856 to open end	2,20 conductor ribbon	10, 15, 15
BC08R-XX	H856 to H856	Shielded flat	1, 6, 10, 12, 20, 25, 50
BC04Z-XX	H856 to open end	Shielded flat	6, 10, 15, 25, 50

Table 6 DRV11-B Interface Connector Signals

Mnemonic	Description
00 OUT — 15 OUT	16 TTL data output lines from the DRV11-B. One = high.
00IN — 15 IN	16 TTL data input lines from the user's device. One = high.
STATUS A, B, C	Three TTL status input lines from the user's device. The function of these lines is defined by the user.
FUNCT 1, 2, 3	Three TTL output lines to the user's device. The function of these lines is defined by the user.
INIT	One TTL output line; used to initialize the user's device.
INIT V2	One TTL output line; present when INIT is asserted or when FUNCT 2 is written to a one. Used for interprocessor buffer applications.
A00	One TTL input line from the user's device. This line is normally high for word transfers. During byte transfers this line controls address bit 00.

Table 6 DRV11-B Interface Connector Signals

Mnemonic	Description
BUSY	One TTL output line to the user's device. BUSY is low when the DRV11-B DMA control logic is requesting control of the LSI-11 bus or when a DMA cycle is in progress. A low-to-high transition indicates end of cycle.
READY	One TTL output line to the user's device. When the READY line goes low, DMA transfers may be initiated by the user's device.
C0, C1	Two TTL input lines from the user's device. These lines control the LSI-11 bus cycle for DMA transfers. C0, C1 codes for the four (4) possible bus cycles as listed below: **Bus Cycle C0 C1** DATI 0 0 DATIO 1 0 DATO 0 1 DATOB 1 1
SINGLE CYCLE	One TTL input line from the user's device. This line is internally pulled high for normal DMA transfers. For burst mode operation, SINGLE CYCLE is driven low by the user's device. **CAUTION:** When SINGLE CYCLE is driven low, total system operation is affected because the LSI-11 bus becomes dedicated to the DMA device and other devices cannot use the bus.
WC INC ENB	One TTL input line from the user's device. This line is normally high to enable incrementing the DRV11-B word counter. Low inhibits incrementing.
BA INC ENB	One TTL input line from the user's device. This line is normally high to enable incrementing the bus address counter. Low inhibits incrementing.

Table 6 DRV11-B Interface Connector Signals

Mnemonic	Description
CYCLE REQUEST	One TTL input line from the user's device. A low-to-high transition of this line initiates a DMA request.
ATTN	One TTL input line from the user's device. This line is driven high to terminate DMA transfers, to set READY, and to request an interrupt if the interrupt enable bit is set.

As bus master, the DRV11-B performs a DATO or DATOB bus cycle by placing the memory address on BDAL lines, asserting BWTBT, and then asserting BSYNC. The memory decodes the address, then the DRV11-B removes the address from the BDAL lines, negates BWTBT (BWTBT will remain active for a DATOB), places the user's input data on the BDAL lines and asserts BDOUT. Memory receives the data and asserts BRPLY. In response to BRPLY, the DRV11-B negates BDOUT and then removes the user's input data from the BDAL lines. Memory now negates BRPLY, the bus cycle is terminated, and the bus released when the DRV11-B negates BSACK and BSYNC.

At the end of the first transfer, the DRV11-B WCR and BAR are incremented, BUSY goes high, and READY remains low. With BUSY high and READY low, the user's I/O device can initiate another DATO or DATOB cycle by again asserting CYCLE REQUEST.If the interrupt enable is set, DMA transfers can continue until the WCR increments to zero and generates an interrupt request.When the WCR increments to zero, READY goes high, and the DRV11-B generates an interrupt request (if the interrupt circuits are enabled). The processor responds to the interrupt request (BIRQ) by asserting BDIN followed by BIAKI (interrupt acknowledge). BIAKI is received by the DRV11-B and in response places a vector address on the BDAL lines, asserts BRPLY, and negates BIRQ. The processor receives the vector address and negates BDIN and BIAKI. The DRV11-B now negates BRPLY, while the processor exits from the main program and enters a service program for the DRV11-B via the vector address.

Interrupt requests from the DRV11-B occur for the following conditions:

1. When the WCR increments to zero—this is a normal interrupt at the end of a designated number of transfers.

2. When the user's I/O device asserts ATTN—this is a special condition interrupt which may be defined by the user to override the WCR.
3. When a nonexistent memory location is addressed by the DRV11-B—this special condition interrupt is produced when no BRPLY is received from the memory.

System Memory to User's Device Transfers (DATIO or DATI)

DMA transfers from the memory to the user's I/O device occur in a manner similar to that described for user's I/O device to memory transfers. Figure 3 illustrates the data flow for a DMA DATIO or DATI cycle. Under program control, the DRV11-B WCR (Figure 11) is loaded with a count equal to the number of transfers, while the BAR is loaded with the starting address from which the first word will come; the CSR is set for transfers.

With the CSR set, READY goes low and the user's I/O device conditions the C0, C1 lines (Table 6) for a DATI or a DATIO, conditions the WC INC ENB, BA INC ENB, ATTN, SINGLE CYCLE (high for normal DMA transfers) signals, and asserts CYCLE REQUEST.

DRV11-J

HIGH DENSITY PARALLEL INTERFACE

INTRODUCTION

Sixty-four input/output data lines are now available on a double-height module for the LSI-11/2, LSI-11/23, PDP-11/03, and PDP-11/23. The DRV11-J also includes an advanced interrupt structure with bit interruptability up to 16 lines, programmable interrupt vectors, and program selection of fixed or rotating interrupt priority within the DRV11-J.

The DRV11-J's bit interrupts for realtime response make it especially useful for sensor I/O applications. It can also be used as a general purpose interface to custom devices, and two DRV11-Js can be connected back-to-back as a link between two LSI-11 buses.

FEATURES

- 64 tri-state bidirectional input/output lines organized as four 16-bit ports, A through D.
- Data line direction selectable under program control for each 16-bit port.
- Transitions on each of the 16 lines of Port A can generate unique interrupt vectors (bit interrupts). This means high-priority inputs get serviced by the CPU much faster.
- Transitions on the USER RPLY lines of each port can generate unique interrupt vectors (I/O interrupts). This means less processor overhead. By selecting this feature, bit interrupts are reduced to 12.
- Double-height module: 22.8cm × 13.2cm (8.9 in × 5.2 in)
- Drive up to 25 feet of shielded cable, 6 feet of unshielded flat or round cable.
- Four external control lines per port: USER RDY, USER RPLY, DRV11-J RDY, and DRV11-J RPLY.
- Interrupt vectors (fixed or rotating priority) are set under program control. This eliminates the need for jumper-defined vectors.
- Latched outputs, PNP-Schmitt-trigger inputs.

SPECIFICATIONS

Identification M8049

Power

+5V±5% 1.6A typical, 1.8A maximum

Bus Loading:

2 ac loads, 1 dc load

DRV11-J

Data Buffer Tri-State Outputs:
V_{OL} = 0.5V @ I_{OL} = 8 mA
V_{OL} = 0.4V @ I_{OL} = 4 mA
V_{OH} = 2.4V @ I_{OH} = −2.6 mA

Data Buffer Inputs:
I_{IL} = −0.2 mA @ V_{IL} = 0.4V
I_{IH} = 20 μA @ V_{IH} = 2.7V

Protocol Signal Tri-State Outputs:
V_{OL} = 0.55V @ I_{OL} = 64 mA
V_{OH} = 2.4V @ I_{OH} = −15 mA

Protocol Signal Inputs:
Termination: 120 ohms
I_{IL} = −27 mA @ V_{IL} = 0.5V
I_{IH} = 80 μA @ V_{IH} = 2.7V

Environmental:
Storage temperature: −40°C to +60°C
Operating temperature: +5°C to +60°C
Adequate airflow must limit the inlet to outlet temperature rise to 10°C (5°C if inlet air is 55°C).

NOTE

Derate maximum operating temperature by 1.8°C for each 1000 meters of altitude above sea level.

Humidity: 10% to 90%, non-condensing

Size
Double-height module:
13.2cm (5.2in) wide
22.8cm (8.9in) long

Cabling:
BC05W-xx—Shielded cable with 50-pin connectors at both ends. Available in 3.0 and 7.5 meter (10 and 25 foot) lengths.

DESCRIPTION
Detailed information about the DRV11-J is supplied with the module.

DRV11-J

PROGRAMMING

The DRV11-J is programmed through eight contiguous directly addressable registers, which may be positioned to start from 760000_8 through 777760_8 in address space by stake pin jumpers. There are four Control Status Registers and four Data Buffers.

The Registers are:

Control Status Register A	(CSRA)	$7XXXX0_8$
Data Buffer Register A	(DBRA)	$7XXXX2_8$
Control Status Register B	(CSRB)	$7XXXX4_8$
Data Buffer Register B	(DBRB)	$7XXXX6_8$
Control Status Register C	(CSRC)	$7XXX10_8$
Data Buffer Register C	(DBRC)	$7XXX12_8$
Control Status Register D	(CSRD)	$7XXX14_8$
Data Buffer Register D	(DBRD)	$7XXX16_8$

XXXX is jumper-selectable between 6000_8 to 7776_8 in a modulus of 16 and factory-set to 6416_8 (CSRA = 764160_8).

The format of these registers is shown in Figure 1.

Unlike other LSI-11 interface modules, the DRV11-J uses two sets of eight internal registers to control interrupts. The first set of registers is controlled through CSRA and CSRB and is responsible for interrupts generated in bits 0-7 of Port A. The second set of registers is controlled through CSRC and CSRD and is responsible for either bits 8-15 of Port A or, when I/O interrupts are selected, the four USER RPLY lines and bits 8-11 of Port A (see Figure 1).

IRR	Interrupt Request Register
ISR	Interrupt Service Register
IMR	Interrupt Mask Register
ACR	Auto Clear Register
—	Status Register
—	Mode Register
—	Command Register
—	Byte Count
—	Vector Address Memory

Interrupt vectors are stored in Vector Address Memory. Vector addresses can be set from 0 to 1774_8 and must be loaded on power-up. To provide for dynamic changing of interrupt subroutines, vectors are programmable. Four vectors are available for each of the sixteen interrupts.

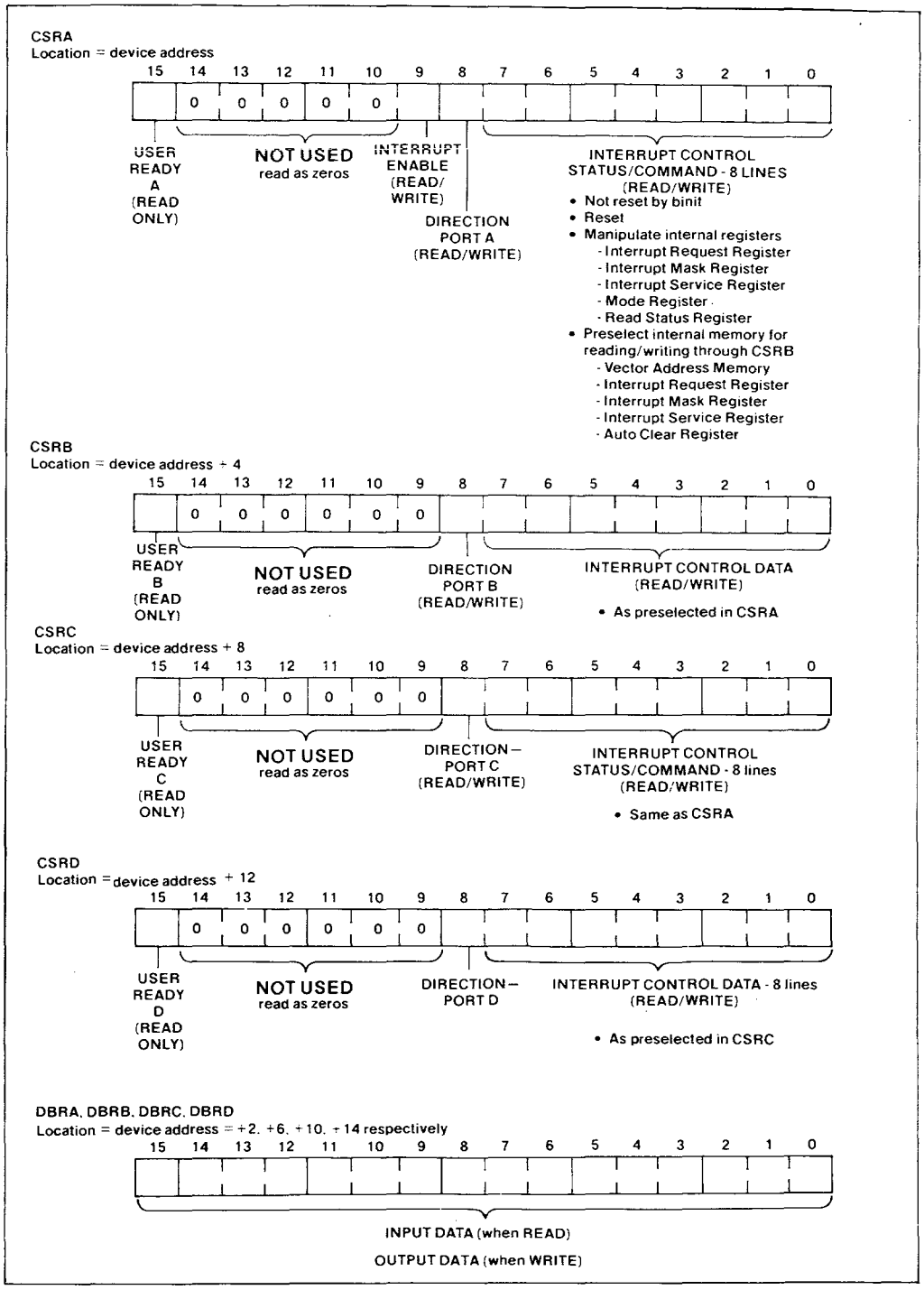


Figure 1 Register Format

DRV11-P

DRV11-P LSI-11 BUS FOUNDATION MODULE

INTRODUCTION

The DRV11-P is an LSI-11 bus-compatible foundation wire-wrap interface module. Approximately one-quarter of the module is occupied by bus transceivers, interrupt vector generator logic, and a 40-pin I/O connector. The remaining three-quarters of the module is for user application and has plated-through holes to accept ICs and wire-wrap pins (WP) for interconnecting the user's circuits. The plated-through holes can accept 6-, 8-, 14-, 16-, 18-, 20-, 22-, 24-, and 40-pin dual-in-line ICs or IC sockets in various mounting areas of the module, or discrete components can be inserted into the plated-though holes. The DRV11-P can be inserted into any one of the available interface option locations of any LSI-11 bus.

FEATURES

- An easy-to-use foundation module for custom interface applications.
- Factory-installed LSI-11 bus-compatible interface circuits.
- Device and interrupt vector that can be configured by the user.
- Compact—occupies only two device locations on the bus.
- Can accommodate up to 50 integrated circuits making up the user's device logic.
- Wire-wrap pins are provided for all signals.
- All user control signal lines are TTL-compatible.

SPECIFICATIONS

Identification	M7948
Size	Quad
Power	5.0 Vdc ±5% at 1.0 A
Bus Loads	
ac	2.1
dc	1 (plus user's logic)

CONFIGURATION

The DRV11-P (Figure 1) is a versatile wire-wrap module that contains interface logic for operation with the LSI-11 bus and provides adequate board area for mounting and connecting integrated circuits (ICs) or discrete components. Because the bus interface logic is in-

cluded, the module can be efficiently configured by the user to satisfy a variety of device interface logic applications.

A 40-pin connector mounted at the board edge connects to a device through several cable assembly types available from DIGITAL.

Except for the bus interface connections, all signals and voltages are terminated to wire-wrap pins for user connections. The bus control logic is provided with wire-wrap test points for monitoring the internal signals. The test points are spaced at 0.254 cm (0.1 in.) between pins to let the 40-pin connector be inserted over the wire-wrap pins for automated test functions.

Approximately two-thirds of the surface area on the module consists of plated-through holes, each connected to a wire-wrap pin. The user can mount three different types of dual-in-line ICs or a variety of discrete components into the holes and connect the proper voltages and signals by wire-wrapping leads on the board.

Device Address Selection

The DRV11-P will respond to up to four consecutive addresses in the bank 7 area (addresses between 160000_8 and 177776_8). The register addresses are sequential by even numbers and are as follows:

Register	BBS7	Octal Address
1	1	16XXX0
2	1	16XXX2
3	1	16XXX4
4	1	16XXX6

The user selects a base ending in zero for assignment to the first register by means of wire-wrap pins on the DRV11-P module. The module decodes this base address and the remaining register addresses are then properly decoded by the DRV11-P as they are received from the LSI-11 bus.

Figure 2 shows the address select format and presents the wire-wrap pin-to-bit relationship for device address selection. Bits to be decoded as 0 bits in the base address are wire-wrapped to ground wire-wrap pins (WP). Bits to be decoded as 1 bits are left unwrapped as these bits are pulled up to the 1 state.

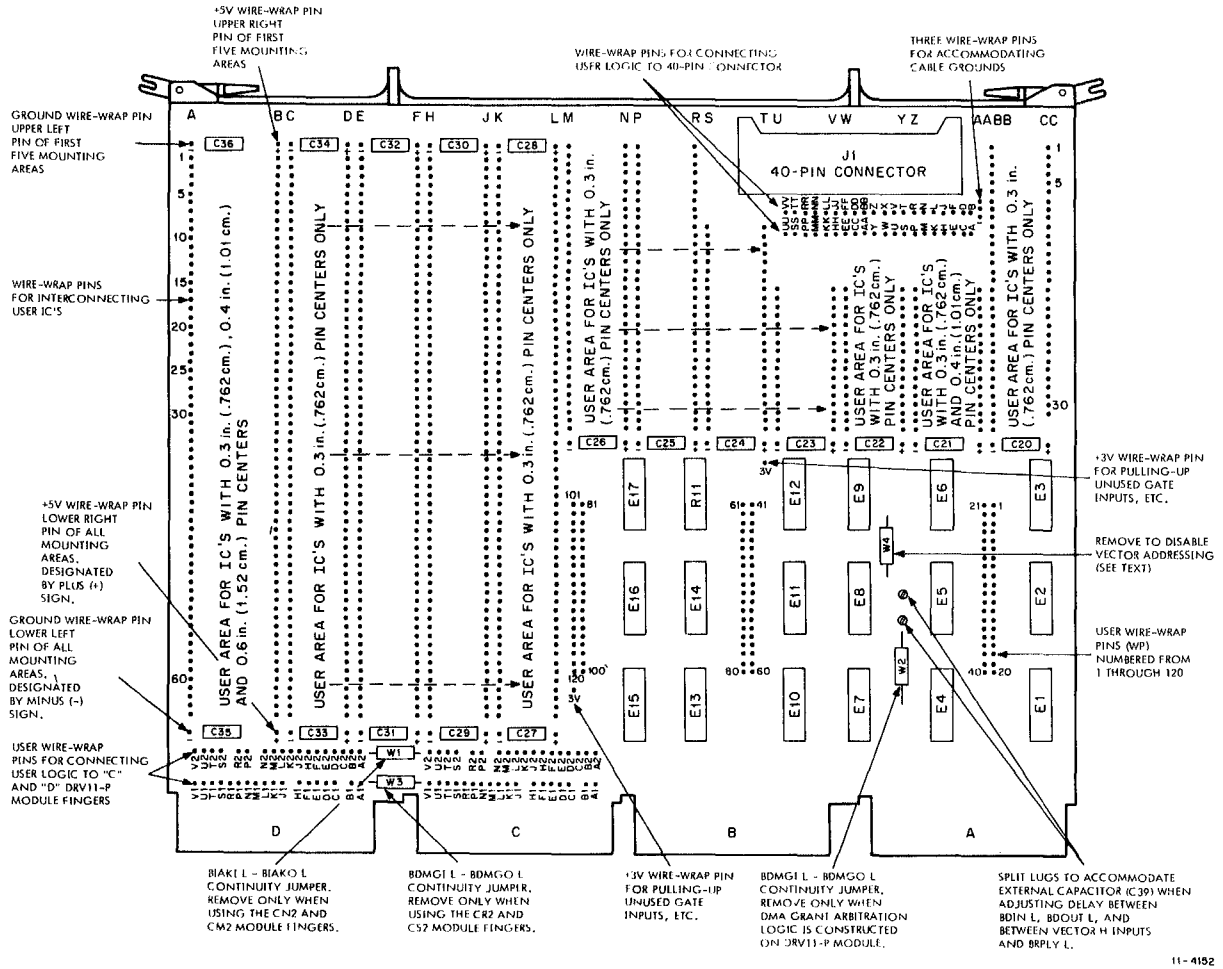


Figure 1 DRV11-P Component Mounting Locations

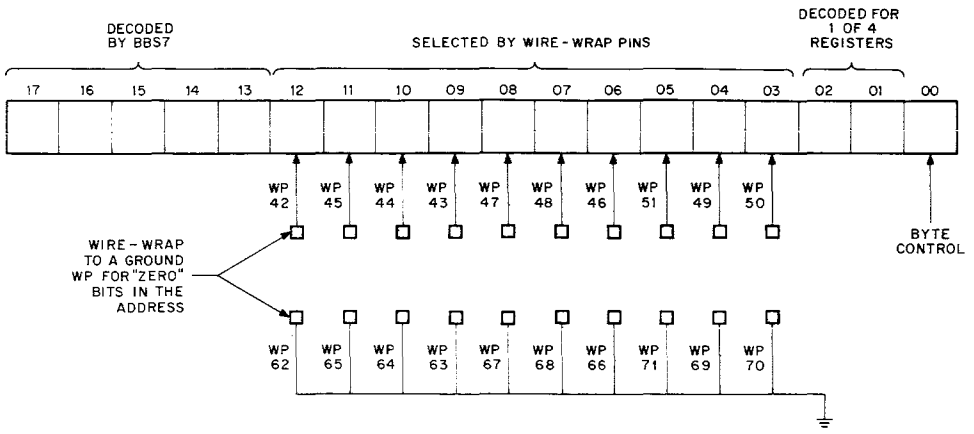


Figure 2 DRV11-P Device Address Select Format

Interrupt Vector Logic — The interrupt vector logic is used in conjunction with the interrupt control logic to generate a vector on bus lines BDAL 00 L-BDAL 07 L. The interrupt vector is specified by the user and selected by installing jumper leads between wire-wrap pins on the M7948 module. The vectors available are from 0 to 374_8. The vector range can be increased from 0 to 774_8 with additional logic and wiring.

When the VECTOR H signal is asserted as a result of a device interrupt request, the interrupt vector is placed on the bus lines.

Wire-wrap pins V3 through V7 are used to assign the vector bits. A jumper lead installed selects a logical 0 address bit for its associated line and no lead selects a logical 1 address bit according to the format in Figure 3.

Bit BDAL 02 L can be connected to the device interrupt request RQST A signal to specify a separate vector address for channel A and channel B.

Status and control information can be multiplexed through the same logic used to generate the vector address. Up to eight status and control bits can be assigned by the user and transferred to bus lines BDAL 00 L-BDAL 07 L. The information can be gated onto the bus lines using a select level generated by the address decoding logic.

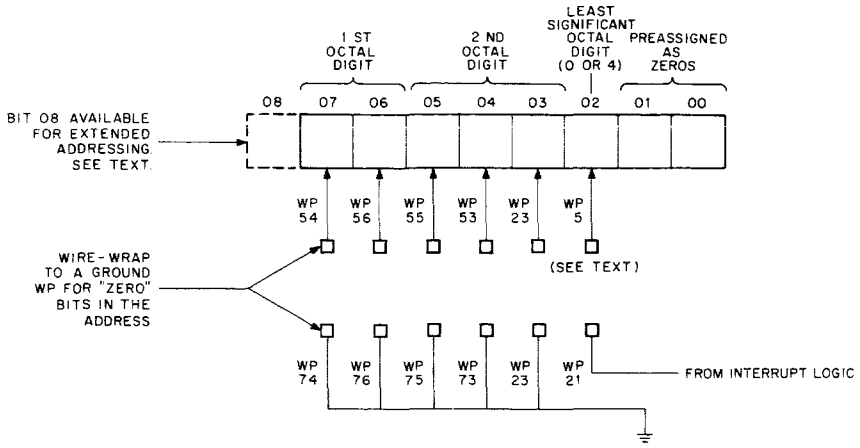


Figure 3 DRV11-P Vector Selection

DUV11

DUV11 LINE INTERFACE

INTRODUCTION

The DUV11 line interface is a buffered, program-controlled, single-line communications interface device which is used to establish a data communications line between any LSI-11 bus and a Bell 201 synchronous modem or the equivalent. The module is fully programmable with respect to sync characters, character length (5 to 8 bits), and parity selection. The DUV11 provides serial-to-parallel and parallel-to-serial data communications, buffers TTL-to-EIA voltage levels and EIA-to-TTL voltage levels, and controls the modem for half- or full-duplex operation.

FEATURES

- Interfaces synchronous and isochronous communications data
- Supports bisynchronous communications data
- Interface signals meet EIA RS-232C standard
- Operates in full-duplex or half-duplex modes
- Maximum baud rate is 19.2K baud
- Uses variable length characters (5, 6, 7, or 8 bits plus parity)
- Generates odd or even parity bits that are transmitted with the data character to the modem
- Verifies received character parity
- Inhibits transmitter output for maintenance purposes
- Provides control signals to the modem and monitors the modem status lines
- Establishes synchronization prior to receiving data
- Generates program interrupt requests

SPECIFICATIONS

Identification	M7951
Size	Quad
Power	+5 Vdc ±5% at 0.86A +12 Vdc ±3% at 0.32A
Bus Loads	
AC	1
DC	1

DUV11

CONFIGURATION

The following paragraphs describe how the user can configure the module for his own system. This module contains switches to select the device address, vector interrupt, and special control functions. The descriptions of the registers and their standard factory addresses are listed in Table 1 and described below.

Table 1 DUV11 Factory Address Assignments

Register	Mnemonic	Read/ Write	DUV11 Address
Receiver Status	RXCSR	R/W	160010
Receiver Data Buffer*	RXDBUF	R	160013
Parameter Status*	PARCSR	W	160012
Transmitter Status	TXCSR	R/W	160014
Transmitter Data Buffer	TXDBUF	W	160016
Interrupt Vector	DONE	—	440

* Dual-purpose read or write register.

Device Address

The LSI-11 bus address and interrupt vector addresses, which are selectable, must be determined prior to operating the DUV11. The bus address (also referred to as the device address) is controlled by switches contained in the two switch banks E38 and E39 (Figure 1), located in the address comparator logic. The position of these switches determines the required address state (1 or 0) of bus address bits 12-3. If a switch is set to ON, the switch contacts are closed and an address state of 1 is required on the related address bit to the address of the DUV11. Hence, electrically, the DUV11 can have any device address within the range of 160000 to 177777. However, DIGITAL software requires that the device address fall within the floating address range of 160010 to 163776. The device address is set to 160010 at the factory to facilitate manufacturing testing. The switch positions for address selection are described in Table 1 and Figure 2.

NOTE

If a device address is selected which falls outside the floating address range, the software must be modified accordingly.

DUV11

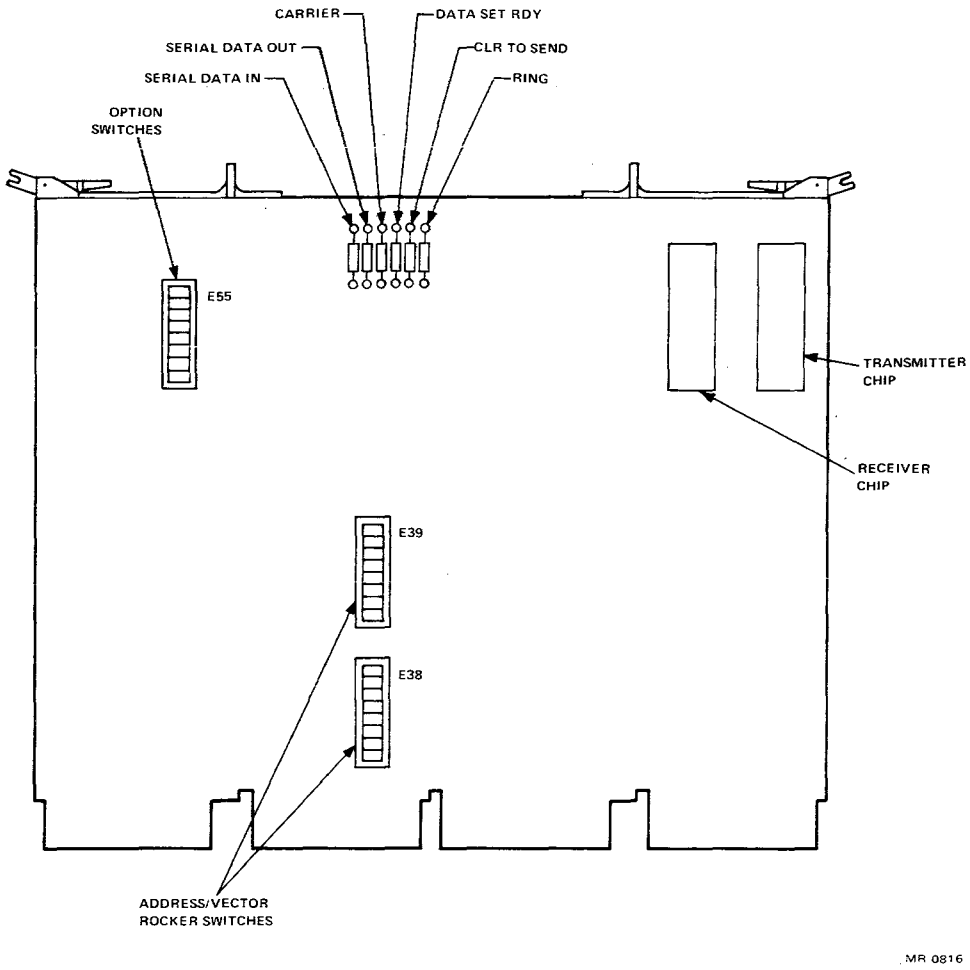


Figure 1 DUV11 (M7951) Major Components

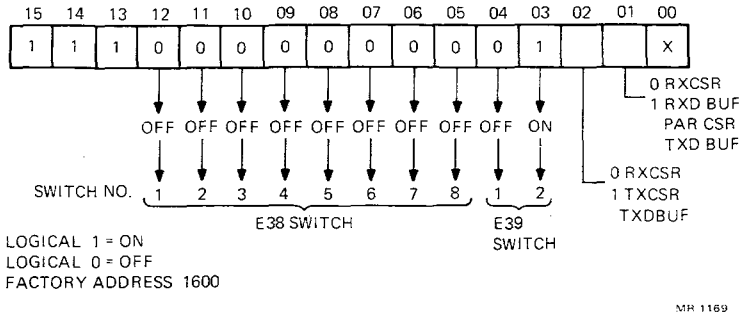


Figure 2 Device Address Selection

Interrupt Vector

The interrupt vector is also floating and is set to 440 at the factory to facilitate factory testing. If it is necessary to change the vector, simply change the six vector select switches contained in switch bank E39 (Figure 1) as required. These switches control vector bits 8-3; therefore, vectors can be generated in the range 000 to 774. However, the software requires that the vector fall within the floating range of 300 to 777. The switch settings for vector selection are shown in Figure 3.

NOTE

If a vector is selected which falls outside the floating address range, the software must be modified accordingly.

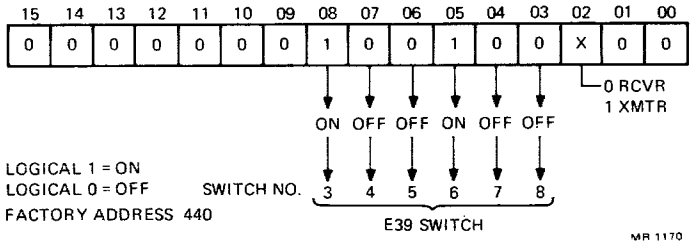


Figure 3 Interrupt Vector Selection

Option Switches

The DUV11 can select optional control functions that are used during operation by using switches S1 through S8 of E55. The detailed operation of these switches is listed in Table 2.

Table 2 Switch Assignments

Switch No.*	Function
SW1	Optional Clear—Switch ON enables CLR OPT, which is used to clear RXCSR bits 3, 2,and 1.
SW2	Secondary Transmit—Switch ON enables secondary data channel between the modem and DUV11.

*All switches are located on component reference designation E55.

Table 2 Switch Assignments (Cont)

Switch No.*	Function
SW3	Secondary Receive—Switch ON enables secondary data channel between the modem and DUV11.
SW4	Sync Characters—Switch ON enables the receiver to synchronize internally upon receiving one sync character. The normal condition of receiving two sync characters exists when SW4 is off.
SW5	Special Feature—Switch ON allows external clock to be internally generated; used when a modem is not being utilized.
SW6	Special Feature—Optional feature is switched ON for program control of data rate selection.
SW7	Maintenance Clock—Switch ON enables the clock that is used for maintenance purposes only.
SW8	Not used.

* All switches are located on component reference designation E55.

Optional Equipment

Mating Connector	H836
Cable	BC05C-XX

DZV11 ASYCHRONOUS MULTIPLEXER

INTRODUCTION

The DZV11 is an asynchronous multiplexer interface module that interconnects the LSI-11 bus with up to four asynchronous serial data communications channels. The module provides EIA interface levels and enough data set control to permit dial-up (auto-answer) operation with modems using full-duplex operations such as Bell models 103, 113, 212, or equivalent. The DZV11 does not support half-duplex operations such as remote operation over private lines for full-duplex point-to-point or full-duplex multipoint as a control (master) station. The DZV11-B includes a BC11U cable assembly for interconnection to the communication devices.

The DZV11-B interface consists of the M7957 module, a BC11U-25 interface cable, and two accessory test connectors (H329 and H325). The H329 connector permits a staggered loopback. The H325 connector is used with the BC11U cable to provide the single-line loopback.

FEATURES

- Selectable baud rates of 50 to 9600
- Character length of 5, 6, 7, or 8-bits
- Stop bits, 1 or 2, for 6-, 7-, and 8-bit characters
- Stop bits, 1 or 1.5, for 5-bit characters
- Parity generation and detection for odd, even, and no parity
- Transmitter and receiver interrupts
- Generates and detects break signals

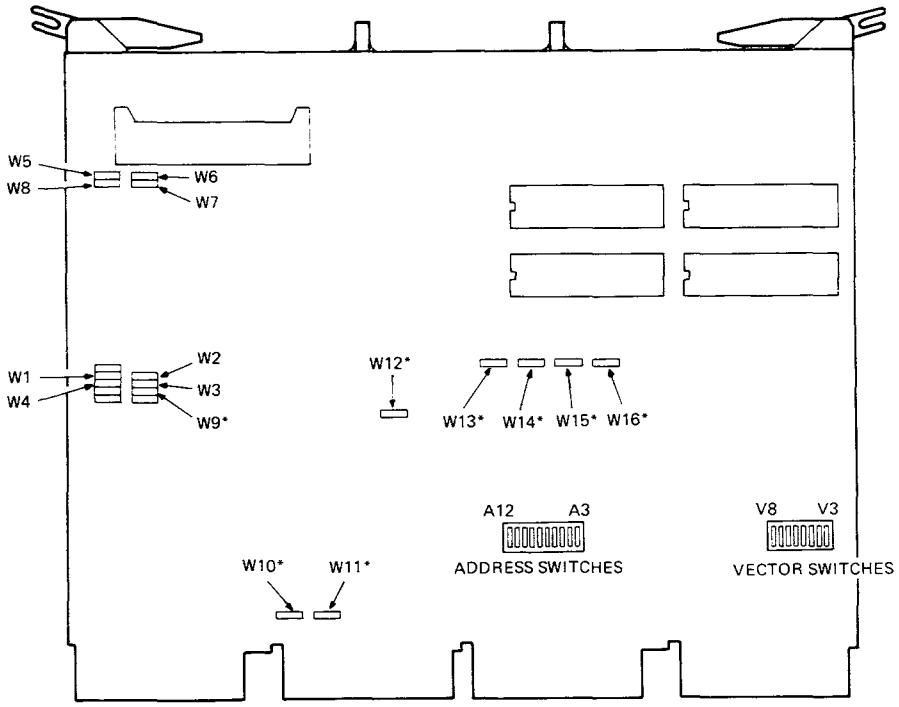
SPECIFICATIONS

Identification	M7957
Size	Quad
Power	+5 Vdc ±5% at 1.15 A +12 Vdc ±3% at 0.40 A
Bus loads	
ac	4.1
dc	1
Interface	EIA standard RS-232C

DZV11

CONFIGURATION

The software control of the DZV11 is performed by six device registers. These registers are assigned addresses and can be read or loaded by the program. DIGITAL software requires that the device addresses be within the range of 760000 to 777777. The M7957 module utilizes the floating address space that starts at 760010 and extends to 764000. The control and status register (CSR) is assigned the basic address by setting the rocker switches of E30 on the module, as shown in Figure 1. The correlation between the bit assignments and the switches is detailed in Figure 2. The remaining register addresses will sequentially follow the basic address, as shown in Table 1. A basic address is preset at the factory; if the user requires a different address, the switches allow him to change the addresses to comply with his system. The interrupt vector is also programmable and can be used with DIGITAL software, provided that the address is within 300 to 777. The switches of E2 on the module allow the user to select an interrupt vector to function within his system. The correlation between the bit assignments and the switches is detailed in Figure 3.



*NOTES:

JUMPERS W9, W12, W13, W14, W15, AND W16 ARE REMOVED ONLY FOR MANUFACTURING TESTS. THEY SHOULD NOT BE REMOVED IN THE FIELD.

JUMPERS W10 AND W11 MUST REMAIN INSTALLED WHEN THE MODULE IS USED IN A BACKPLANE THAT SUPPLIES LSI-11 BUS SIGNALS TO THE C AND D CONNECTORS OF THE DZV11 (SUCH AS THE H9270). WHEN THE MODULE IS USED IN A BACKPLANE THAT INTERCONNECTS THE C AND D SECTIONS TO AN ADJACENT MODULE, JUMPERS W10 AND W11 MUST BE REMOVED.

Figure 1 M7957 Module

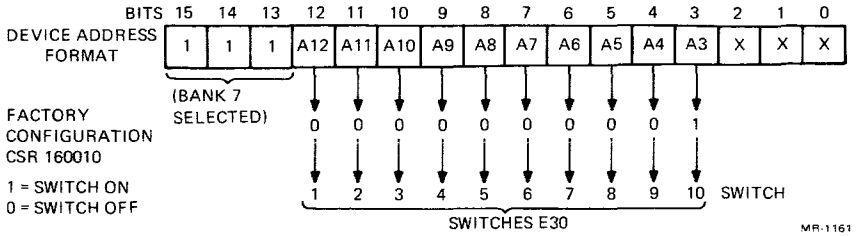


Figure 2 DZV11 CSR Address Bits

Table 1 DZV11 Register Address Assignments

Register	Mnemonic	Address*	Read/ Write
Control and Status	CSR	76XXX0	R/W
Receiver Buffer	RBUF	76XXX2	R
Line Parameter	LPR	76XXX2	W
Transmitter Control	TCR	76XXX4	R/W
Modem Status	MSR	76XXX6	R
Transmit Data	TDR	76XXX6	W

* XXX = Selected in accordance with floating device address scheme. Dual-purpose register.

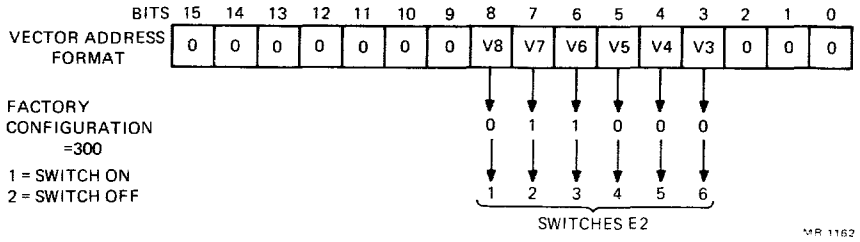


Figure 3 DZV11 Vector Bits

Jumpers

Modem Control — There are eight jumpers (W1-W8) used for modem control. Jumpers W1 and W4 connect data-terminal-ready (DTR) to request-to-send (RTS). This allows the DZV11 to assert both DTR and RTS when using a modem that requires the control of RTS. These

jumpers must be installed to run the external cable and test diagnostic programs. Jumpers W5 through W8 connect the forced-busy leads to the request-to-send leads. When these jumpers are installed, the assertion of an RTS signal places an ON or busy signal on the corresponding forced busy lead. Forced busy jumpers W5-W8 are normally removed unless they are required for the modem. These modem control jumpers are listed in Table 2.

Table 2 Modem Control Jumper Configuration

Jumper	Connection	Line
W1	DTR to RTS	3
W2	DTR to RTS	2
W3	DTR to RTS	1
W4	DTR to RTS	0
W5	RTS to FB	3
W6	RTS to FB	2
W7	RTS to FB	1
W8	RTS to FB	0

Bus Signals — Jumpers W10 and W11 must remain installed when the module is used in a backplane that supplies bus signals to C and D connectors such as the H9270. When the module is in a backplane that uses the C-D interconnect scheme (such as the H9273), the jumpers W10 and W11 must be removed.

Testing — Jumpers W9 and W12 through W16 are removed for manufacturing test purposes only. These jumpers should not be removed by the user.

Device Registers — All software control of the DZV11 is performed by six device registers. Each register is assigned a bus address that can be read or loaded.

Control and Status Register — The control and status register (CSR) is a byte- and word-addressable register. All bits in the CSR are cleared by an occurrence of BINIT or by setting device master clear (CSR 4).

H780 POWER SUPPLY

INTRODUCTION

Six H780 power supply options are available for use in system applicatons. The six models provide for a choice of input voltage (115 Vac or 230 Vac, nominal), and master console, slave console, or no console.

All models are used for supplying dc operating voltages to an LSI-11 bus backplane. In addition, each model generates a proper power-up/Power-down sequence of BDCOK H and BPOK H LSI-11 bus signals. Master console-equipped and slave console-equipped models can be interconnected to allow control of both supplies from the master console.

FEATURES

- +5V ±3%, 18 A (maximum) and +12V ±3%, 3.5 A (maximum); combined dc power must not exceed 110 W.
- Overcurrent/short-circuit protection—Output voltages return to normal after removal of overload or short; current is limited to approximately 1.2 times the required maximum rating.
- Overvoltage protection—+5V limited to +6.3V (approximately); +12V limited to +15V (approximately).
- Line-time clock—A bus-compatible signal is generated by the power supply for the event (line-time clock) interrupt input to the processor. This signal is either 50 or 60 Hz, depending on primary power line frequency input to the power supply.
- Power-fail/automatic restart—Fault detection and status circuits monitor ac and dc voltages and generate bus-compatible BPOK H and BDCOK H signals (respectively) to inform the LSI-11 bus modules of power supply status.
- Fans—Built-in fans provide cooling for the power supply and modules contained in the system backplane.

SPECIFICATIONS

Input voltage (Continuously—see Note 1)
100-127 Vac (H780-C, -H, -K)
200-254 Vac (H780-D, -J, -L)

Temporary Line Dips Allowed
100% of voltage, 20 msec max

H780

AC Inrush Current
70 A at 127V, 60 Hz (8.33 msec)
25 A at 254V, 50 Hz (10 msec)

Input Power (fans included)
340 W at full load max
290 W at full load typical

Input Protection
H780-C, -H, -K (100-127 Vac) fast blow, 5 A fuse
H780-D, -J, -L (200-254 Vac) fast blow, 2.5 A fuse

Hi-Pot
2 kV for 60 seconds from input to output, or input to chassis

Output Power (combinations not to exceed 110 W)
+5V, 1.5 A-18 A
+12V, 0.25 A-3.5 A

Maximum DC Current under Fault Conditions
+5V bus = 28 A
+12V bus = 9.5 A

+5V Output

Total Regulation	5V ±3%
Line Regulation	±0.5%
Load Regulation	±1.0%
Stability	0.1%/1000 hours
Thermal Drift	0.025%/°C (See Note 2)
Ripple	150 mV p-p (1% for f <3 kHz)
Dynamic Load Regulation	±1.2% di/dt = 0.5 A μs delta I = 5 A
Noise	1 % peak at f > 100 kHz (noise is super-imposed on ripple)
Interaction due to +12V	±0.05%

+12V Output

Total Regulation	12V ±3%
Line Regulation	±0.25%
Load Regulation	±0.5%
Stability	0.1%/1000 hours (See Thermal Drift Note 2) 0.025%/°C above 25°C

H780

Ripple	350 mVp-p (1% for f <3 kHz)
Dynamic Load Regulation	±0.8% di/dt = 0.5 A μsec f<500 Hz delta I = 3 A
Noise	1 % peak at f > 100 kHz (noise is super-imposed on ripple)
Interaction due to +5V	±0.02%
Overvoltage Protection	
+5V	6.3V nominal 5.65V min 6.8V max
+12V	15V nominal 13.6V min 16.5V max
Adjustments	
+5V Output	4.05V-6.8V Guarantee Range 4.55-5.65V
+12V Output	10.6V-16.5V Guarantee range 11.7-13.6V
Controls	
Rear Panel	AC ON/OFF switch
Front Console	DC ON/OFF switch HALT/ENABLE switch
(Master only)	LC ON/OFF switch
Console Indicators	DC ON RUN (Master) SPARE (Master only)

Backplane Signals

BPOK H	
BDCOK H	
BEVNT L	Transmitted
BHALT L	
SHRUN L	Received (Master only)

Mechanical

Cooling

Two self-contained fans provide 0.7140 m^3/min (30 ft^3/min) air flow.

H780

Size
13.97 cm w × 8.43 cm h × 37.15 cm l
(5-1/2 in w × 3-1/3 in h × 14-5/8 in l)

Weight
5.90 kg (13 lb)

Environmental

Temperature

Ambient	5° to 50° C (41° to 122° F)
Storage	−40° to +70° C (−40° to +158° F)

Humidity
90% maximum without condensation

NOTES

1. Operation from ac lines below 100V may cause the power supply to overheat because of decreased air flow from the cooling fans.
2. These parameters apply after 5 minutes of warmup and are measured with an averaging meter at the processor backplane terminal block under system loading.

DESCRIPTION

Six H780 power supply options are available for use in LSI-11 bus systems. Individual model numbers determine combinations of 115 or 230 Vac (nominal) primary power and selection of master console, slave console, or no console. Models are listed below.

H780 Model No.	Input Power	Console Description
H780-C	115V	None
H780-D	230V	None
H780-H	115V	Master
H780-J	230V	Master
H780-K	115V	Slave
H780-L	230V	Slave

The H780 master console contains RUN and DC ON indicators for monitoring the processor states, as well as DC ON/DC OFF, LTC ON/OFF, and ENABLE/HALT switches for controlling the processor. The slave console contains only a DC ON indicator for monitoring the status of the slave power supply.

Console Controls and Indicators — The H780-H or -J master console has three LED indicators and three 2-position toggle switches. One of the LED indicators is a spare indicator. Circuitry to drive this indicator is included on the console printed circuit board for user application. The console on the H780-K and -L slave supplies has only one LED indicator, DC ON. The H780 console controls and indicators are described in Table 1. Additionally, the rear panel of the H780 contains an AC ON/OFF toggle switch and an ac line fuse.

+12 V and +5 V Adjustment Procedure — The H780 power supply is factory-adjusted to produce +12 V and + 5 V outputs within the operating tolerance of the system. The adjustment procedures presented allow the user to trim the dc outputs of the H780 to meet his particular needs. One adjustment is provided for the +12 V output, while two adjustments (one for the output voltage and one for the switching regulator frequency) are provided for the +5 V. A DVM, an oscilloscope, and a small screwdriver are required. Power supply loading is provided by the LSI-11 bus or processor.

Table 1 H780 Controls and Indicators

Control/ Indicator	Type	Function
DC ON	LED indicator	Illuminates when the DC ON/OFF toggle switch is set to ON and proper dc output voltages are being produced by the H780. If either the +5 or +12 V output from the H780 is faulty, the DC ON indicator will not illuminate. This is the only indicator on the H780-K and -L slave supplies.
RUN	LED indicator	Illuminates when the processor is in the run state (see ENABLE/HALT).
SPARE	LED indicator	Not used by the H780 or processor. The H780 contains circuitry for driving this indicator for user applications.
DC ON/OFF	Two-position toggle switch	When set to ON, enables the dc outputs of the H780. The DC ON indicator will illuminate if the H780 dc output voltages are of proper values. If a slave supply is connected to a master, the slave DC ON indicator will light if the slave dc output voltages are of proper value. When set to OFF, the dc outputs from the H780 are disabled and the DC ON indicator is extinguished. If a slave supply is connected to a master, the slave DC ON indicator will also extinguish.

Table 1 H780 Controls and Indicators (Cont)

Control/ Indicator	Type	Function
ENABLE/HALT	Two-position toggle switch	When set to ENABLE, the B HALT L line from the H780 to the processor is not asserted and the processor is in the Run mode (RUN indicator illuminated). When set to HALT, the B HALT L line is asserted, allowing the processor to execute console ODT microcode (RUN indicator extinguished).
LTC ON/OFF	Two-position toggle switch	When set to ON, enables the generation of the line-time clock (LTC) BEVNT L signal by the H780. When set to OFF, disables the H780 line time clock.
AC ON/OFF (rear panel)	Two-position toggle switch	When set to ON, applies ac power to the H780. When set to OFF, removes ac power from the H780.
FUSE (rear panel)	5 A or 2.5 A fast-blow	Protects H780 from excessive current. H780-C, -H, and -K use a 5 A fuse, H780-D, -J, and -L use a 2.5 A fuse.

H909-C

H909-C GENERAL PURPOSE LOGIC ENCLOSURE

INTRODUCTION

The H909-C is an enclosure for use with the DDV11-B.

SPECIFICATIONS

Width	48.25 cm (19 in)
Height	13.33 cm (5.25 in)
Depth	62.86 cm (24.75 in) 70.48 cm (27.50 in) including bezel
Weight	27.21 kg (60 lb.)
Mounting Space for Power Supplies	12.7 cm × 15.8 cm × 50.8 cm (5 in × 6.25 in × 20 in)

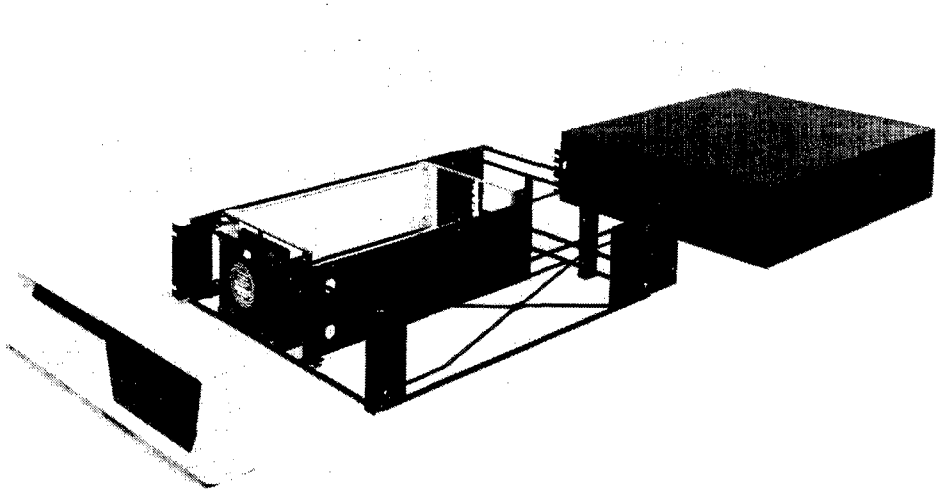


Figure 1 H909-C Enclosure

H909-C

DESCRIPTION

The H909-C is a general purpose logic box designed to accommodate the DDV11-B backplane for any one of several different standard logic subsystems. A photograph of the H909-C enclosure is shown on the opposite page. The H909-C features a distinctive front panel that can be drilled for lights and switches as required by the user. A fan is provided for cooling purposes, and ample room is reserved for power supply installation.

CONFIGURATION

A detailed description of each, including application and configuration information, is presented in the following table. The various options available are listed below.

Options	Voltage (V)	Bezel*	Includes	Mounting
H909-C	—	No	Fan and H0341 card guide	—

* Including switches

H9270 BACKPLANE

INTRODUCTION

The H9270 consists of an 8-slot backplane with a card guide assembly. This backplane is designed to accept up to eight double-height modules (including processor), four quad modules, or a combination of quad and double-height modules. When used for bus expansion in multiple backplane systems, the H9270 provides space for up to six option modules, plus the required expansion cable connector module(s) and/or terminator module.

DESCRIPTION

Mounting the Backplane

Mounting dimensions and possible methods of mounting the H9270 backplane (in any of three planes) are shown in Figure 1. Option positions are shown in Figure 2. Slot numbers indicate device interrupt and DMA priority in LSI-11 bus systems. The lowest numbered positions receive the highest priority.

DC Power Connections

Voltage and Current Requirements — A power supply for a single H9270 backplane LSI-11 system should have the following capacity:

+5V ±5% load; 0-18 A static/dynamic
+12V ±3% load; 1-2.5 A static/dynamic
+5 ripple; less than 1% of nominal voltage
+12 ripple; less than 150 mV p-p (frequency 5 kHz)

NOTE

Regulation at the H9270 backplane must be maintained to the specifications listed above.

The H780 power supply option provides sufficient dc power and generates the required bus signals. Installation details are included in the H780 power supply description.

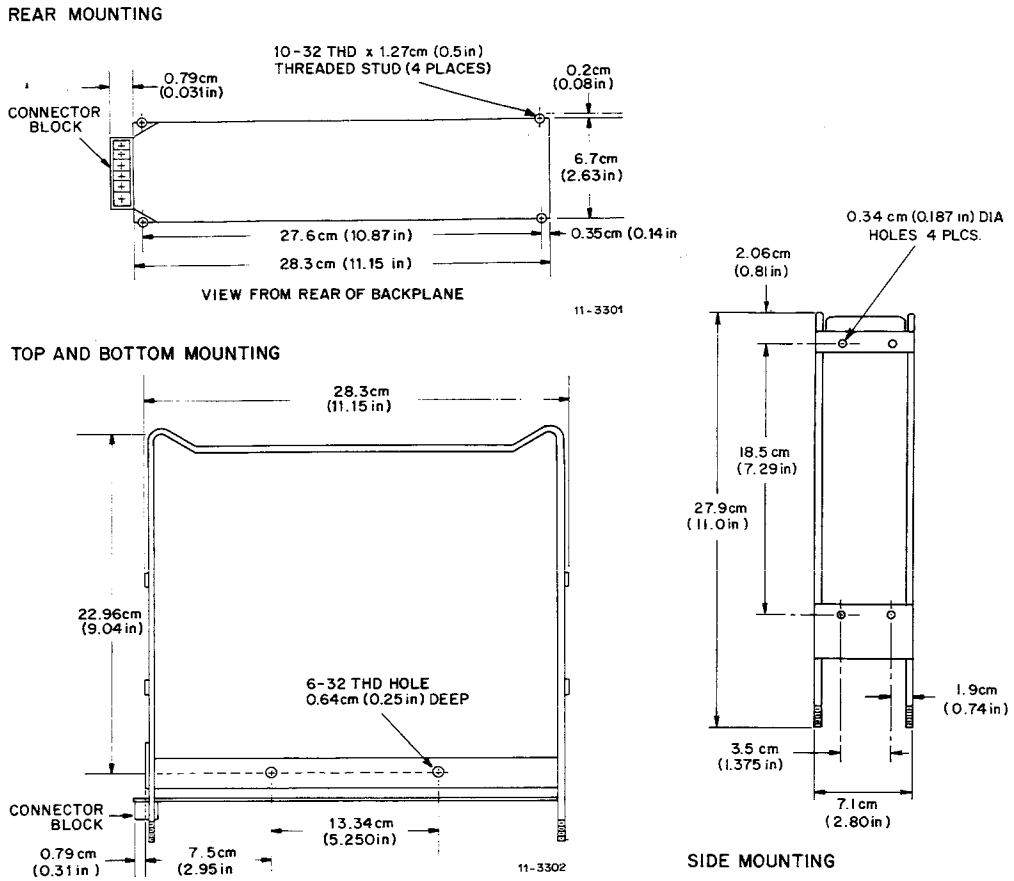


Figure 1 Backplane Mounting

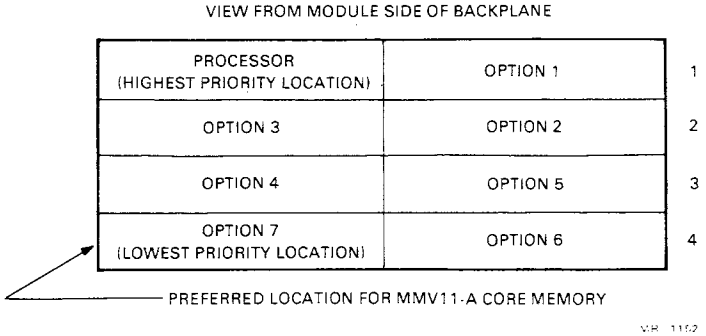


Figure 2 H9270 Option Positions

A multiple-backplane system using H9270 backplanes should have the same voltage regulation and ripple specification as listed for the single H9270 backplane. However, it will be necessary to calculate the actual power requirements, based on individual power requirements for modules used in the system.

Backplane Power Connections — If the H780 power supply option is not used, perform the following steps to connect power to the H9270 backplane (Figure 3).

1. Select wire size. (14 gauge is recommended.) Consider load current and distance between the power supply and backplane.
2. For a standard system, connect the applicable wires to the H9270 connector block per Table 1.

   For battery backup, remove the jumper between +5V and +5B and connect the applicable wires to the H9270 connector block.
3. Connect the ground terminals at the power source.
4. It is recommended that the backplane frame/casting be electrically connected to the system/power supply ground.

The signal connections to the H9270 backplane are shown in Figure 4.

Table 1 H9270 Backplane Standard Power Connections

Power Source (From)		H9270 Connector Block (To)
+12V	+12V	
+5V	+5V	Factory
	+5B	Connected
GND	GND	Factory
GND	GND	Connected
−12V	−12V	This voltage is not required. The connection is available for custom interfaces.

NOTE
H9270 has 5.1 AC loads.

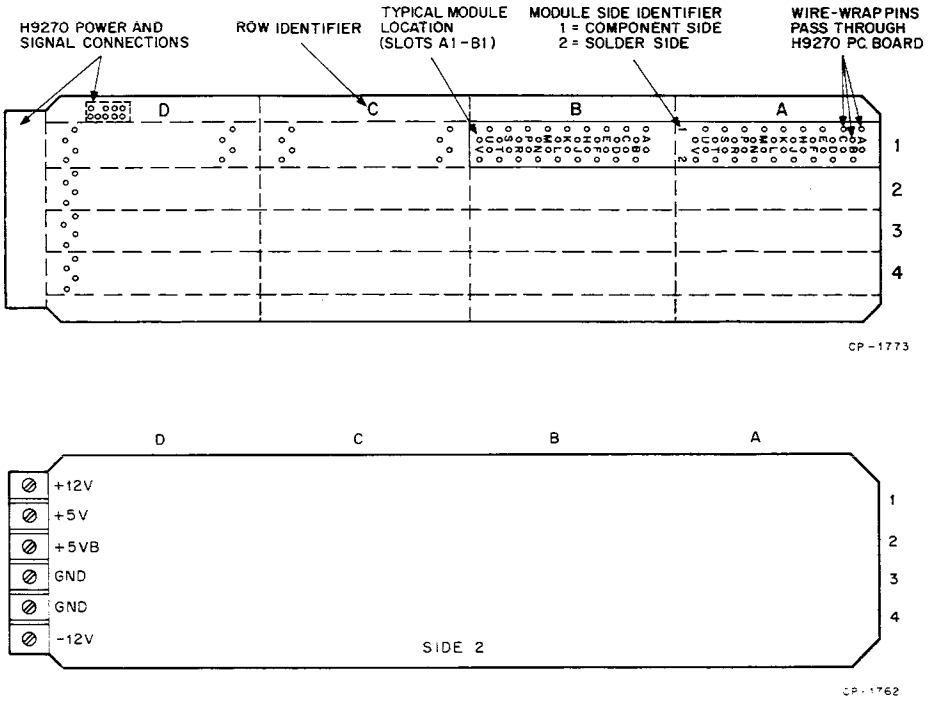


Figure 3 H9270 Backplane Terminal Block (Pin Side View Shown)

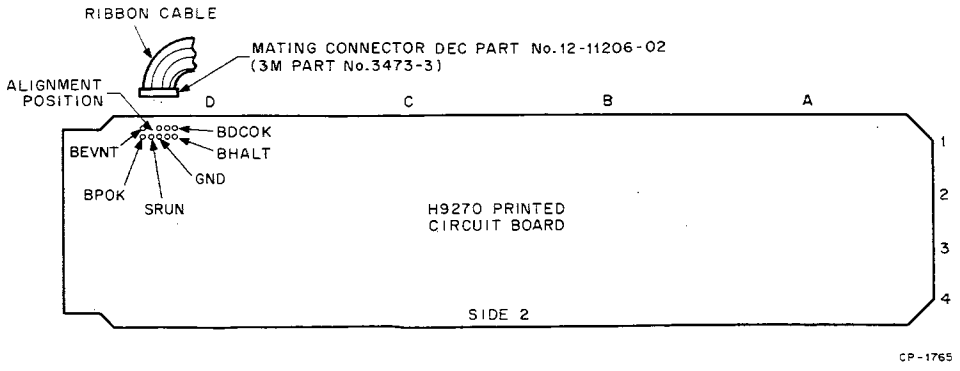


Figure 4 H9270 Backplane Signal Connections (Pin Side View Shown)

CONFIGURATION

Backplane and Module Configuration

LSI-11 bus systems can be classified as either single-backplane or multiple-backplane systems. The electrical characteristics of each system are different; hence, two sets of rules have been devised and must be observed. These rules have their basis in bus loading and power consumption.

Single-Backplane Configuration Rules

1. The LSI-11 bus can support up to 20 ac loads, if unterminated at the end.
2. The terminated bus can support up to 35 ac loads.
3. The bus can support up to 20 dc loads.
4. The amount of current drawn from each power supply should be 70 percent or less of the maximum rated output of the supply.

Multiple-Backplane Configuration Rules

1. No more than three backplanes can be connected together.
2. Each backplane can have no more than 20 ac loads.
3. The total number of dc loads cannot be more than 20.
4. Both ends of the termination line must be terminated with 120 ohms, i.e., the first backplane must have an impedance of 120 ohms, and the last backplane must have a termination of 120 ohms.
5. The cable connecting the first two backplanes (i.e., the main box and expander box 1) must be at least 60.96 cm (2 ft.) long. (A 182.88 cm (6 ft) cable is recommended for ease of installation.)
6. The cable connecting the backplane of expander box 1 to the backplane of expander box 2 must be at least 121.92 cm (4 ft) longer or shorter than the cable connecting the main box and expander box 1 (a 304.80 cm (10 ft) cable is recommended for ease of installation).
7. The combined length of both cables in a 3-backplane system cannot exceed 487.68 cm (16 ft).
8. The interbackplane cables must have a characteristic impedance of 120 ohms.
9. The amount of current drawn from each power supply should be 70 percent or less of the maximum output of the supply.

H9270

To configure an LSI-11 bus system, take the following steps:

1. Choose the type of memory (MOS, PROM, or combination) required for the specific application.
2. Select the CPU and memory combination most suited for the application.
3. Select additional memory, interface, and peripheral options.
4. Count the total number of module positions.
5. Count the total number of bus positions.
6. Choose a backplane configuration that satisfies both the module position requirement, the bus position requirement, and also provides sufficient expansion space.
7. Enter the option names in the backplane positions of the selected configuration.

H9273-A BACKPLANE

INTRODUCTION

The H9273-A backplane logic assembly consists of a 9 × 4 backplane (nine rows of four slots) and a card frame assembly.

DESCRIPTION

The H9273-A backplane logic assembly is shown in Figure 1. Power and signals are supplied to the backplane to conncectors J7 and J8. These connectors are shown in Figures 1, 2,and 3. Connectors J9 (GND) and J10 (−12V) are also shown in Figure 2.

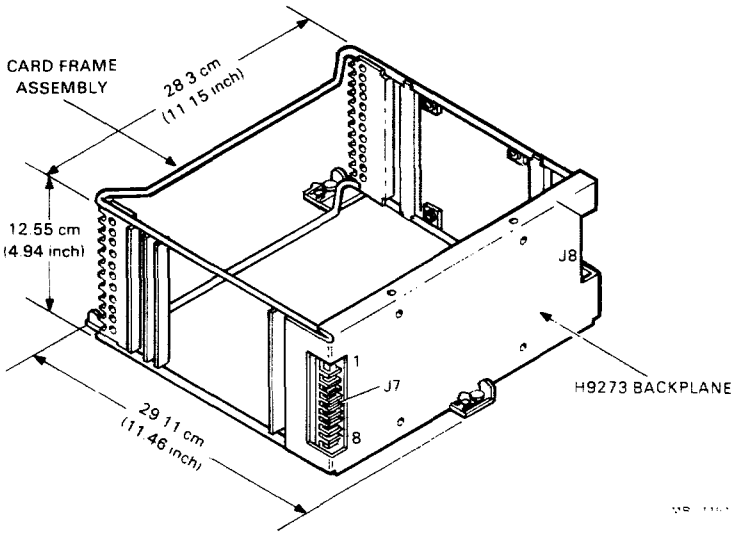


Figure 1 H9273-A Backplane Logic Assembly

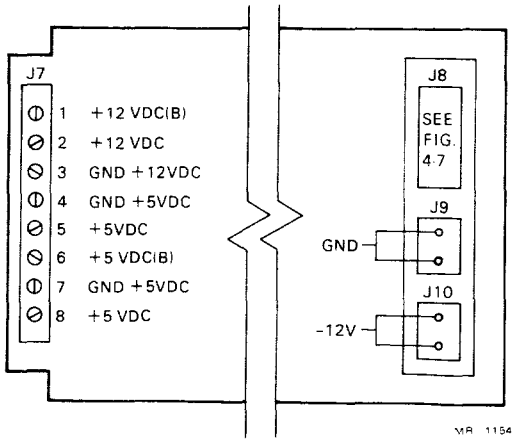


Figure 2 H9273-A Power Connections

H9273-A

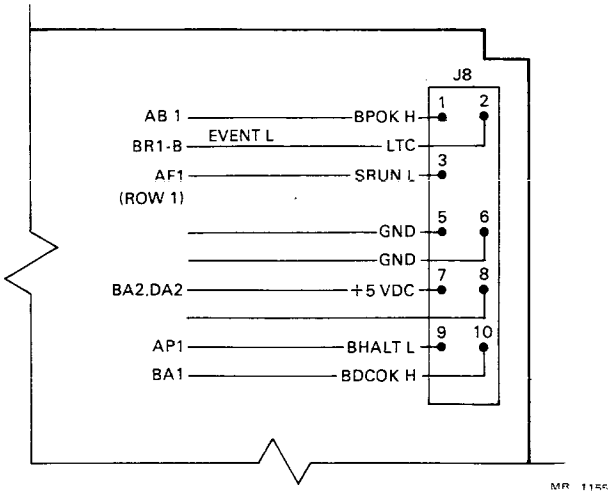


Figure 3 H9273-A Signal Connections

The H9273-A backplane is designed to accept both double-height and quad-height modules with the exception of the MMV11-A core memory module. The backplane structure is unique in that it provides two distinct buses: the LSI-11 bus signals (slots A and B) and the CD bus (slots C and D). The connectors that make up this backplane are arranged in nine rows (Figure 4). Each connector has two slots, each of which contains 36 pins, 18 on either side of the slot.

The connectors designated "Connector 1" in Figure 4 are wired according to the LSI-11 bus specifications. Slots A and B carry the LSI-11 bus signals and are termed the LSI-11 bus slots. The connectors designated "Connector 2" are wired for +5 V and ground, and have no connections to the LSI-11 bus; instead, C- and D-slot pins on side 2 of each row are connected to the C- and D-slot pins on side 1 in the next lower row. Details of the CD interconnection scheme are depicted in Figure 5.

CONFIGURATION

The H9273-A backplane logic assembly is designed to mount into a BA11-N mounting box or equivalent. Refer to the BA11-N mounting box description for more information.

NOTE

Connector block pins do not extend beyond the H9273-A printed circuit etch card, thus eliminating the possibility of backplane wire-wrapping.

H9273-A has 2.6 AC loads.

Three jumpers (W1, W2, and W3) are shown in Figure 4. Jumper W1 enables the line-time clock when inserted and disables it when removed.

NOTE

Only one BA11-N mounting box in any system may have the line-time clock enabled.

When inserted, jumpers W2 and W3 allow the LSI-11 quad-height CPU to run in row 1. Jumpers W2 and W3 are removed when the backplane is used as an expansion backplane in a system.

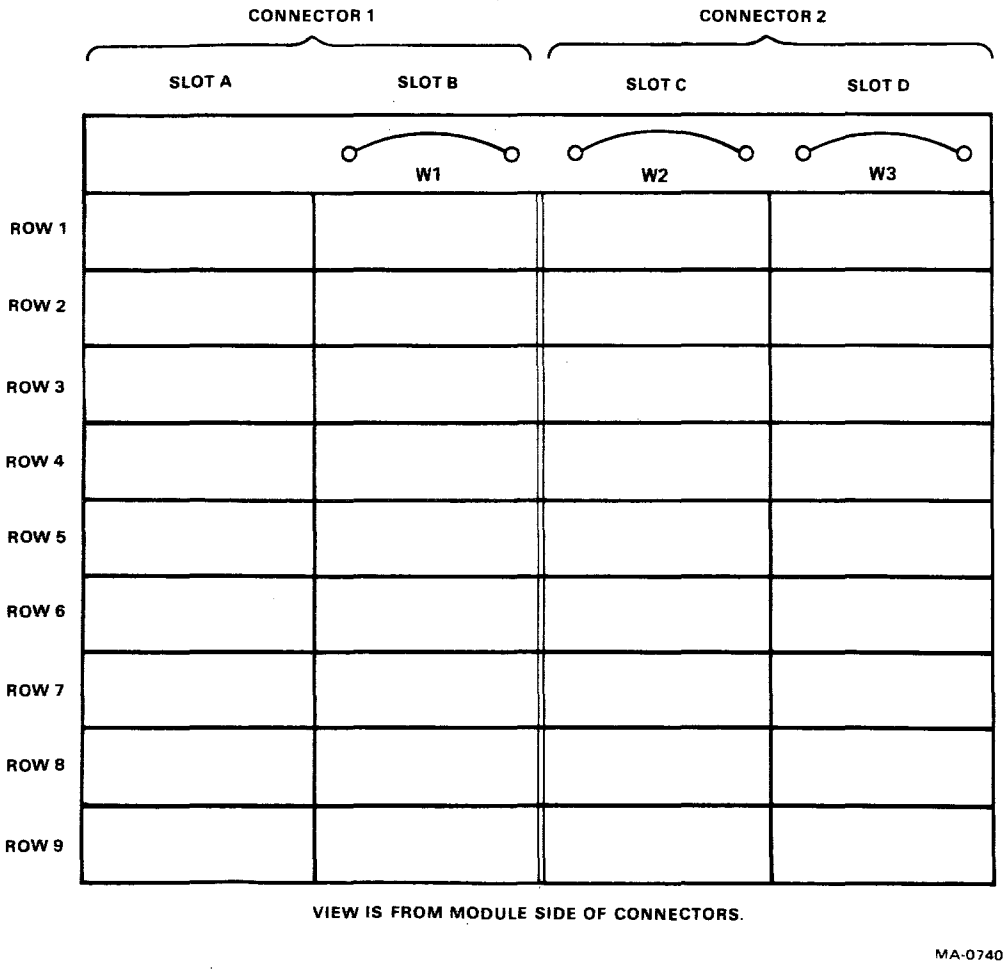
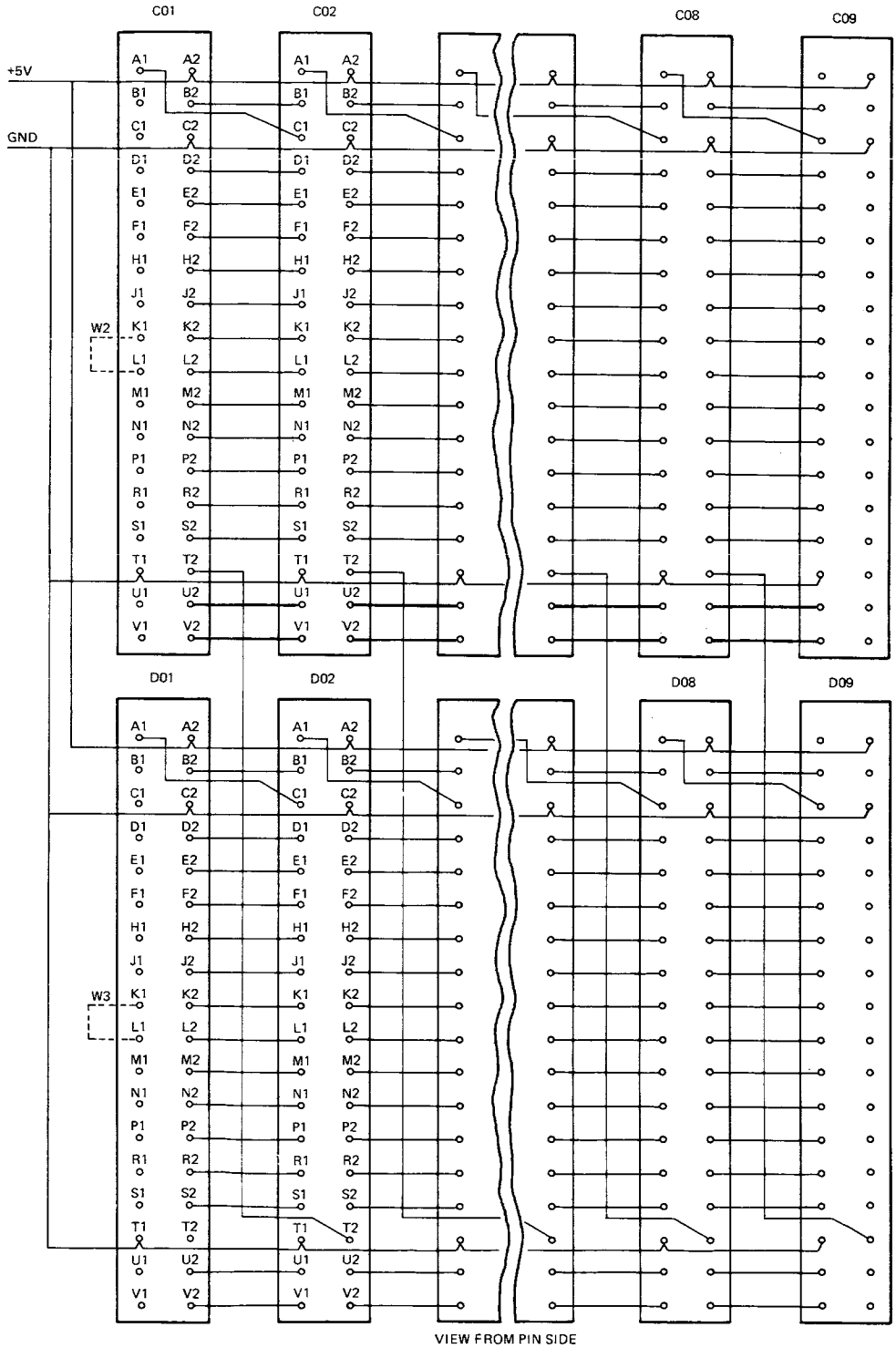


Figure 4 H9273-A Backplane Connectors

H9273-A



FEATURES:

- ALL PINS A1 CONNECT TO PINS C1 IN THE NEXT LOWEST SLOT.
- ALL PINS A2 CONNECT TO +5 VOLTS.
- ALL PINS T2 OF SLOT C ARE CONNECTED TO PIN T2 OF SLOT D IN THE NEXT LOWER SLOT.
- ALL PINS C2 AND PINS T1 ARE GROUND.
- JUMPER W2 IS CONNECTED ACROSS PINS K1 AND L1 IN SLOT C ONLY.
- JUMPER W3 IS CONNECTED ACROSS PINS K1 AND L1 IN SLOT D ONLY.

MR-1364

Figure 5 C-D Bus Interconnection Scheme

H9275-A BACKPLANE

INTRODUCTION

The H9275-A is an 18 position, LSI-11, terminated backplane that has been designed to accept LSI-11 processors, memories, and interface modules. The nine slot by four row backplane accepts up to 18 dual-height modules, or 9 quad-height modules, and uses a 22-bit address bus (see Figure 1). Both dual-height and quad-height modules can be mixed together in the H9275-A backplane because the LSI-11 bus is repeated on both of its sides.

The H9275-A includes a wire frame card cage with integral card guides. LSI-11 bus signals are terminated on the backplane with 120 ohm networks, eliminating the need for a terminator module.

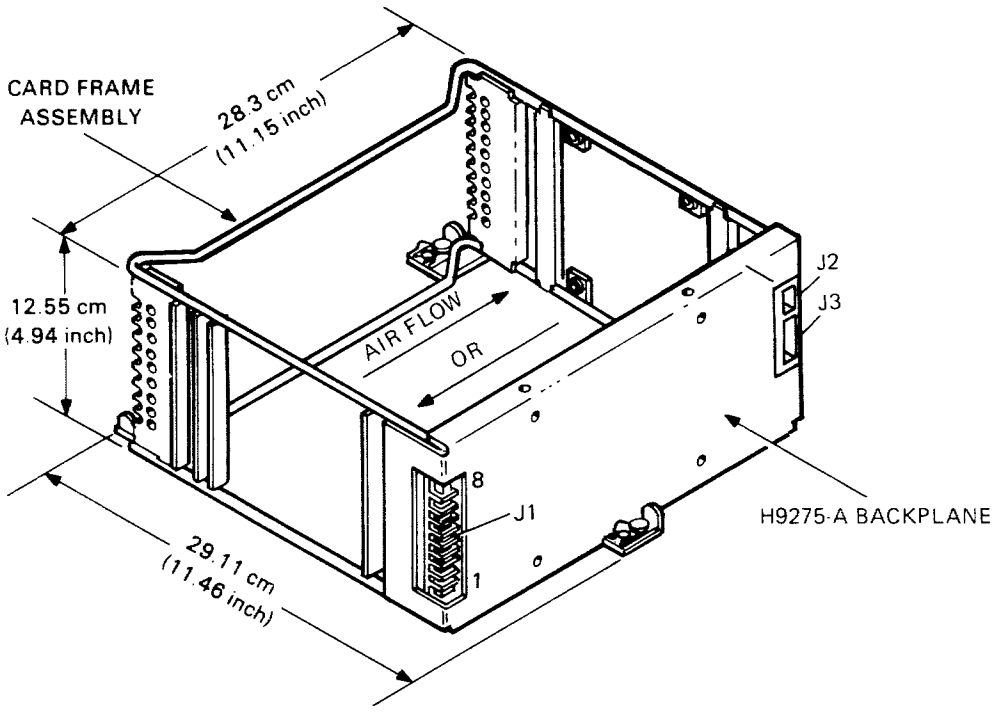


Figure 1 H9275-A Backplane Assembly

DESCRIPTION

The H9275-A backplane assembly has nine jumper wires, designated W1 through W9, which modify the bus configuration. The H9275-A also has connectors that are positioned in four rows, called the A, B, C, and D rows. (Please refer to Figure 2 for an illustration of the con-

nectors on the backplane). LSI-11 modules are plugged into these rows and connected to the bus. Position 1 uses the row A and row B connectors. Position 2 uses the row C and row D connectors. Therefore, row A is wired identically to row C, and row B is wired identically to row D.

The H9275-A backplane supports the LSI-11/23 processor modules four megabyte memory addressing capability. LSI-11 and LSI-11/2 processor modules can also be used with the H9275-A with slight variations. Table 1, below, illustrates the jumper wires that must be removed or installed, depending on which processor is used.

The LSI-11/2 processor can be connected to the H9275-A backplane after the W2, W3, W4, and W5 jumper wires have been removed. These wires connect BDAL 18 through BDAL 21 (the extended address lines that provide 22-bit addressing) address lines to position 1 (the processor position). If jumper wires W2-W5 are not removed, interference of bus operation will result because the LSI-11/2 processor connects signals to these lines' jumper wires, which are not used for addressing.

The LSI-11 processor can also be used in the H9275-A backplane, provided jumper wires W6, W7, W8, and W9 are removed. Since the LSI-11/2 processor is a quad-height module, it requires positions 1 and 2 on the backplane. Jumper wires W6 through W9 connect the BDAL 18 through BDAL 21 address lines to position 2, which is used by the processor. The W2-W5 jumpers can either be installed or removed, and will not interfere with the operation of the LSI-11 processor.

Table 1 Jumper Wire Status for Microprocessors

	LSI-11/23	FALCON AND LSI-11/2	LSI-11
W2-W5	INSTALLED	REMOVED	DON'T CARE
W6-W9	INSTALLED	INSTALLED	REMOVED

CONFIGURATION

The H9275-A backplane uses three medium snap slide fasteners to secure it to the mounting surface. The user provides three mounting

studs for the snap slide fasteners. These fasteners are available from Dimco Gray Company as part no. 25-1-075-093. These studs are positioned in a plane defined by the length and width of the backplane. The mounting stud locations within this backplane are defined in Figure 3.

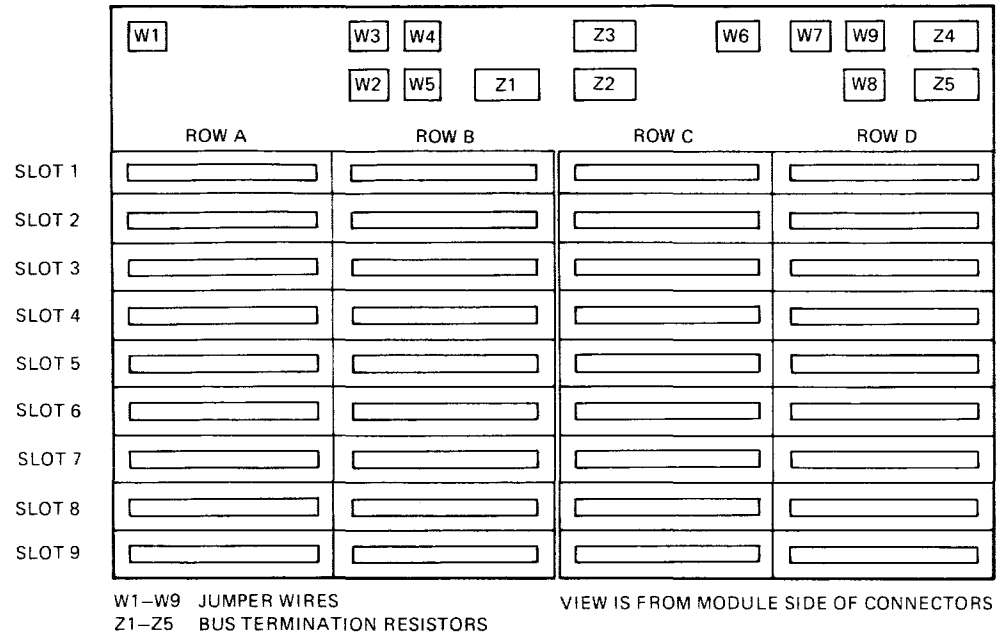


Figure 2 H9275-A Backplane Connectors

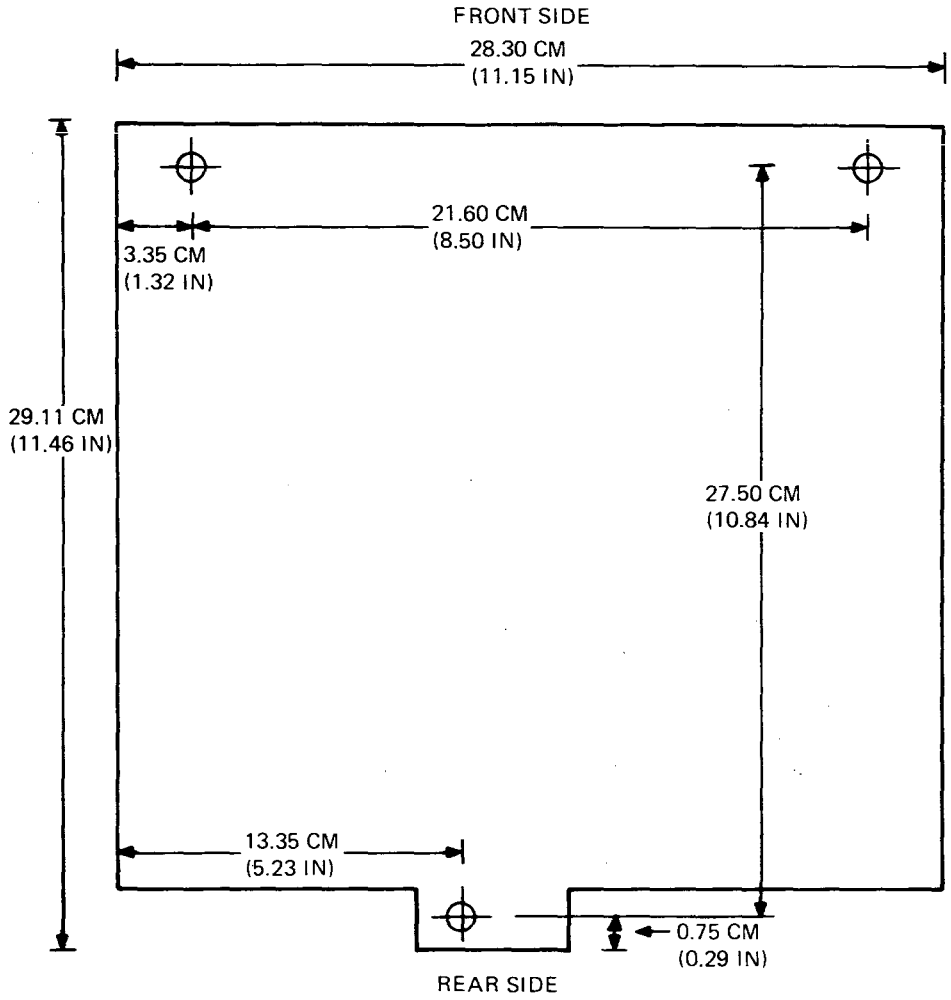


Figure 3 Mounting Stud Locations

Connecting System Power

The H9275-A backplane requires external +5 Vdc and +12 Vdc power sources. The current rating of these power sources is defined by the configuration of the user's system. The external power sources are connected to the standard power connector, J1. The J1 connector is a screw terminal strip located on the rear of the backplane, as shown in Figure 4.

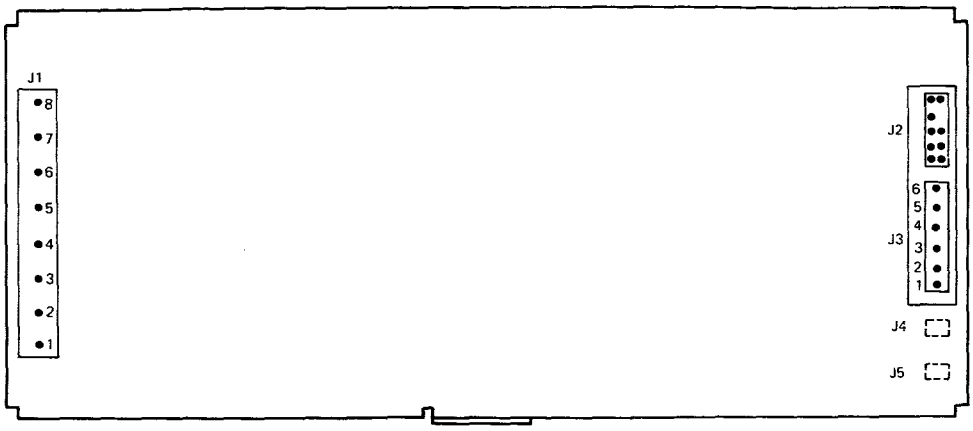


Figure 4 H9275-A Rear View

The J1 terminal strip connectors are rated for 15 amperes per terminal and accept up to a No. 12 wire. The backplane connector pins for the modules are rated at one ampere. Additional +5 Vdc power can be connected to the backplane by using two push-on power tabs designated as J4 and J5. J4 and J5 power tabs are used only when the system requires more than 45 amperes of +5 Vdc power. These power tabs are located on the rear of the backplane as shown in Figure 4.

NOTE

The J4 and J5 power tabs should never be used as a +5 Vdc power source from the bus to another device.

The J5 power tab is for the +5 Vdc connection and is rated for 15 amperes. The J4 power tab is for the ground connection and is rated for 15 amperes.

Connecting Control Bus Signals

Control bus signals are connected to the H9275-A backplane through the J2 connector on the rear of the backplane as shown in Figure 4. These signals include the power sequence signals BPOK H and BDCOK H, as well as the signals BHALT L and BEVNT L. The processor SRUN L signal is available to monitor the processor-run condition.

The signal connections to the J2 connector are detailed in Figure 5. The connector is keyed to accept the LSI-11 console/backplane cable No. 70-11411-0K. This cable must not exceed one meter in length.

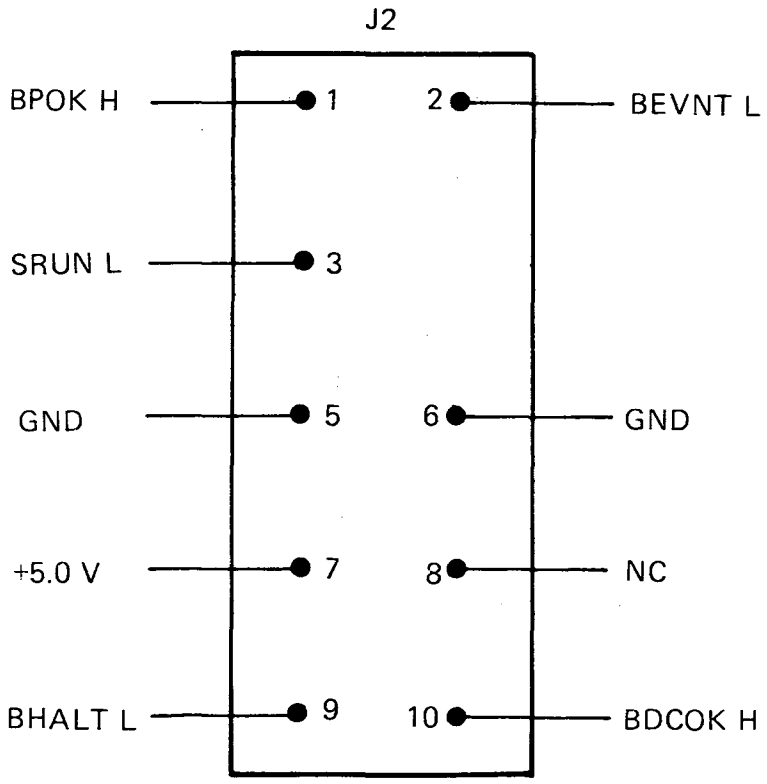


Figure 5 Control Bus Signals J2 Connector

Bus Priority

The modules in the system are serviced on a priority basis for bus interrupts and Direct Memory Access (DMA) requests. Bus interrupts function in either a position-dependent priority or a position-independent priority while DMA requests function only in the position-dependent priority. Position-independent priority is only implemented on the LSI-11/23 CPU.

The bus positions described in Figure 6 are numbered in order for the position-dependent priority structure. Priority is determined by the

physical placement of the module in the backplane. Position 1 is assigned the highest priority and position 18 is assigned the lowest priority. This priority structure operates with the condition that there are no open or empty positions in the backplane between the placement of the modules.

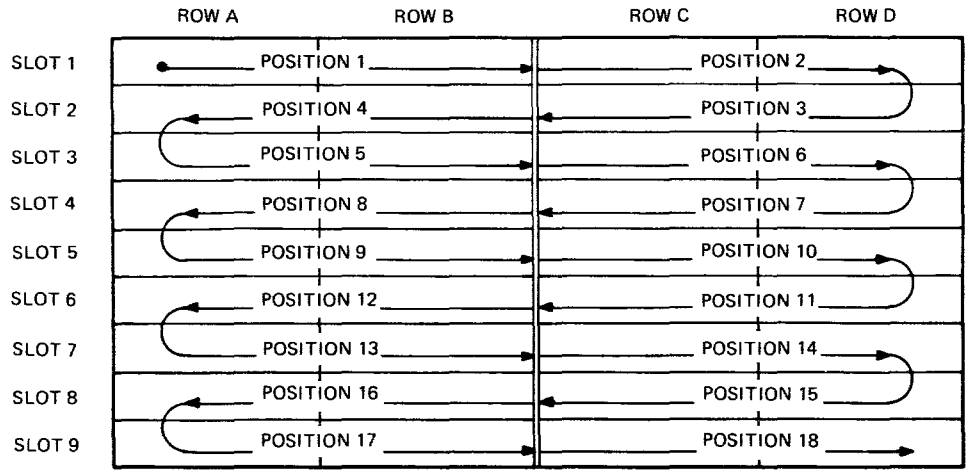


Figure 6 Horizontal Position Priority Structure

Bus Termination

The bused signals are terminated in the backplane with a characteristic impedance of 123 ohms connected to the 3.4 Vdc. The termination resistors are located by Z1 through Z5 in Figure 2.

Bus Restrictions

The H9275-A backplane is a maximum LSI-11 system configuration that will not support any external cabling of the bus. This limits any system to the backplane and is not expandable by using additional backplanes. The backplane contains 0.188 inch pins on the connector blocks and will not accept any wirewrap connections.

H9276

H9276 BACKPLANE

INTRODUCTION

The H9276 is a 9 x 4 (nine rows of four slots) backplane designed for use with the BA11-S mounting box. It can accommodate both dual- and quad-height extended LSI-11 bus modules used in the 22-bit addressing system.

SPECIFICATIONS

AC Loading: 3 Units

DESCRIPTION

The H9276 backplane provides two separate buses: the extended LSI-11 bus and the CD bus. (The C and D rows of the backplane collectively comprise the CD bus). Figure 1 depicts these two buses and illustrates the H9276 backplane, as well as power and signal connectors (J1-J3).

All modules are inserted in slots 1 through 9 of the H9276 backplane. Rows A and B of each slot supply the extended LSI-11 bus signals, while these signals, in turn, are bused to each of the nine slots. The pins of the C and D rows are not bused, but the pins of the adjacent slots are connected. This arrangement not only precludes the necessity of top connectors, but provides the means for designing buses whose lengths are determined by the number of modules in a set.

The connector labeled "connector 1" in Figure 2 has two connector slots wired in parallel (etch connections). When the PDP-11/23-PLUS CPU module is inserted into rows A, B, C, and D of slot 1, rows A and B carry the extended LSI-11 bus signals. Therefore, the A and B rows are called the extended LSI-11 bus rows.

The connector labeled "connector 2" in Figure 2 carries the CD signals. These connectors are not wired in parallel, except the +5 V and ground. These connectors have no connectors to the extended LSI-11 bus in rows A and B. The connectors that make up the H9276 backplane each have 36 pins. Four rows-- A-, B-, C-, and D-- each have nine slots. Each slot has two rows of connector pins, 18 on either side of the slot.

The extended LSI-11 bus signals are found on all 9 slots of rows A and B, and use rows CD connector slots for communications between any number of consecutive slots between slots 2 and 9. Figure 3 shows the C-D bus interconnection scheme. LSI-11 double-height modules are inserted into the extended LSI-11 bus slots, rows A and B on the H9276

H9276

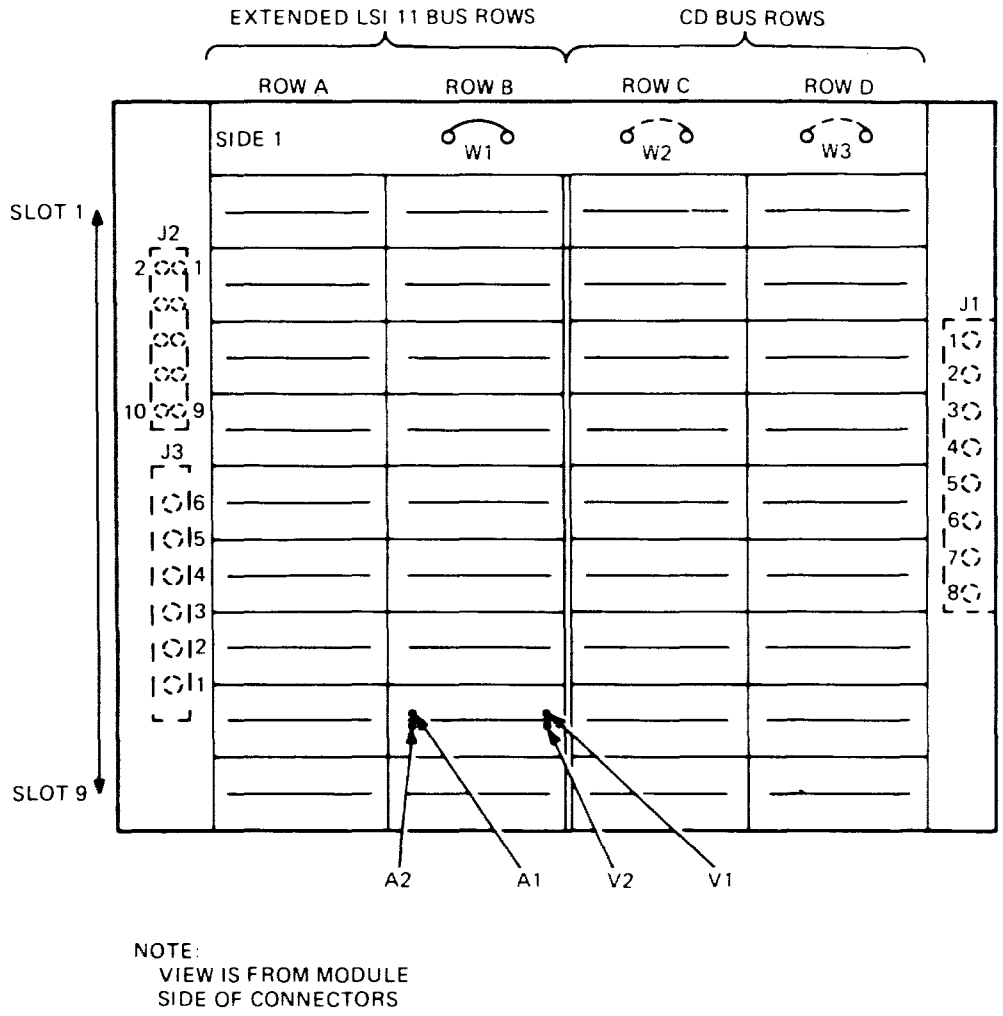


Figure 1 H9276 Backplane

backplane. If the extended LSI-11 bus is to be continued to a second backplane, a M9404 connector module is inserted into rows A and B of the next available slot, while an M9405 connector module is inserted into slot 1 (rows A and B) of the second backplane. A pair of BC02D cables is used with these modules to connect one H9276 backplane to another.

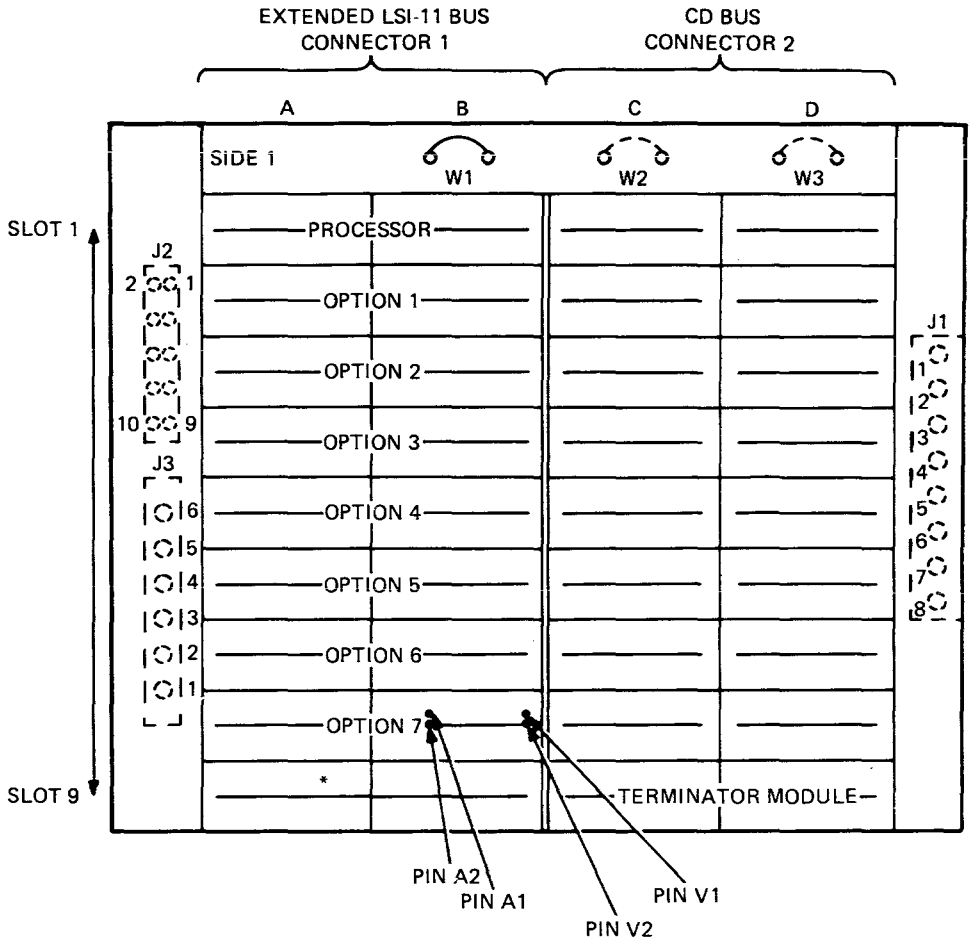
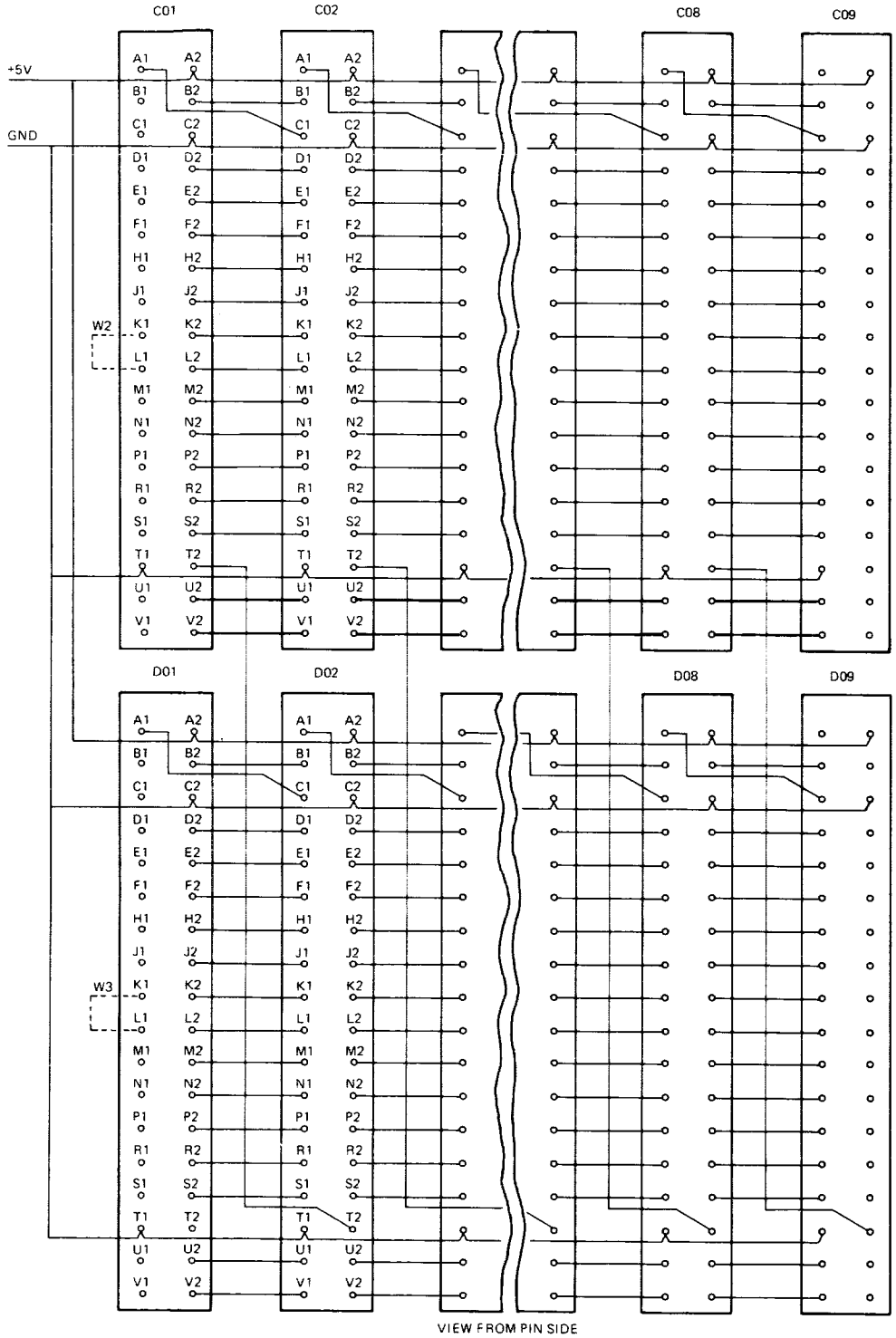


Figure 2 H9276 Backplane Connectors (Module Side)

H9276



FEATURES:

- ALL PINS A1 CONNECT TO PINS C1 IN THE NEXT LOWEST SLOT.
- ALL PINS A2 CONNECT TO +5 VOLTS.
- ALL PINS T2 OF SLOT C ARE CONNECTED TO PIN T2 OF SLOT D IN THE NEXT LOWER SLOT.
- ALL PINS C2 AND PINS T1 ARE GROUND.
- JUMPER W2 IS CONNECTED across PINS K1 AND L1 IN SLOT C ONLY.
- JUMPER W3 IS CONNECTED ACROSS PINS K1 AND L1 IN SLOT D ONLY.

MR-1364

Figure 3 C-D Bus Interconnection Scheme

H9281 BACKPLANE

INTRODUCTION

The H9281 backplane is designed to accept double-height modules only. Six options of the H9281 backplane let the user configure compact LSI-11 bus systems that most efficiently use available system space.

No quad-height modules can be installed in the H9281 backplane.

DESCRIPTION

The H9281 2-slot backplane is available in the following six options:

Backplane Option Designation	Description
H9281-AA	4-module backplane
H9281-AB	8-module backplane
H9281-AC	12-module backplane
H9281-BA	4-module backplane and card cage assembly
H9281-BB	8-module backplane and card cage assembly
H9281-BC	12-module backplane and card cage assembly

CONFIGURATION

Mounting dimensions for H9281 backplanes are shown in Figures 1 and 2. The H9281 backplanes can be mounted in any plane. The enclosure in which the backplane is mounted, available system space, and cooling air flow will determine an acceptable backplane position in a particular system.

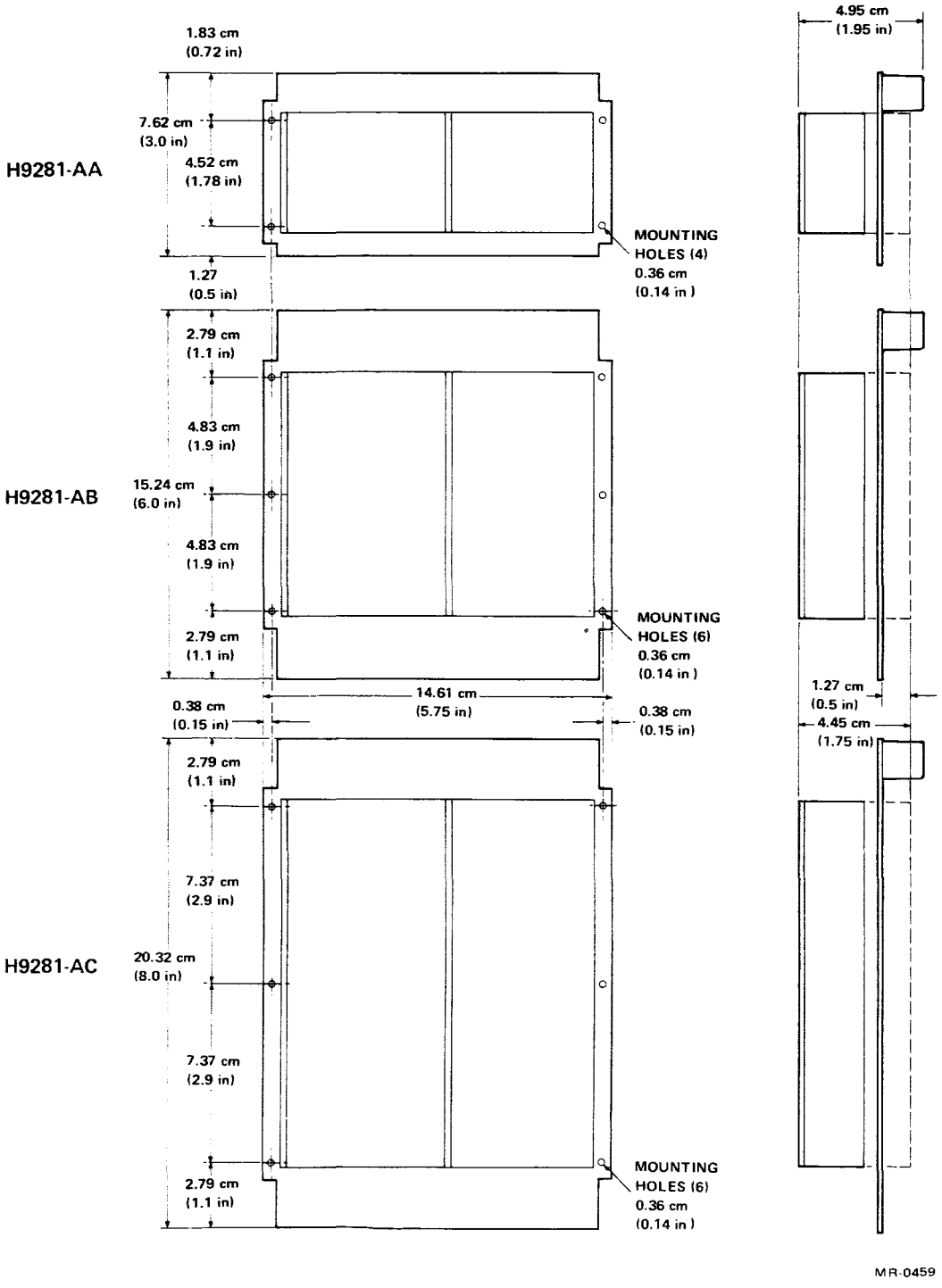


Figure 1 H9281-AA,-AB,-AC Mounting Dimensions

H9281

MODEL	MOUNTING DIMENSION A	ASSEMBLY LENGTH B
H9281-BA	6.86 cm (2.7 in)	7.62 cm (3.0 in)
H9281-BB	11.94 cm (4.7 in)	15.24 cm (6.0 in)
H9281-BC	17.02 cm (6.7 in)	20.32 cm (8.0 in)

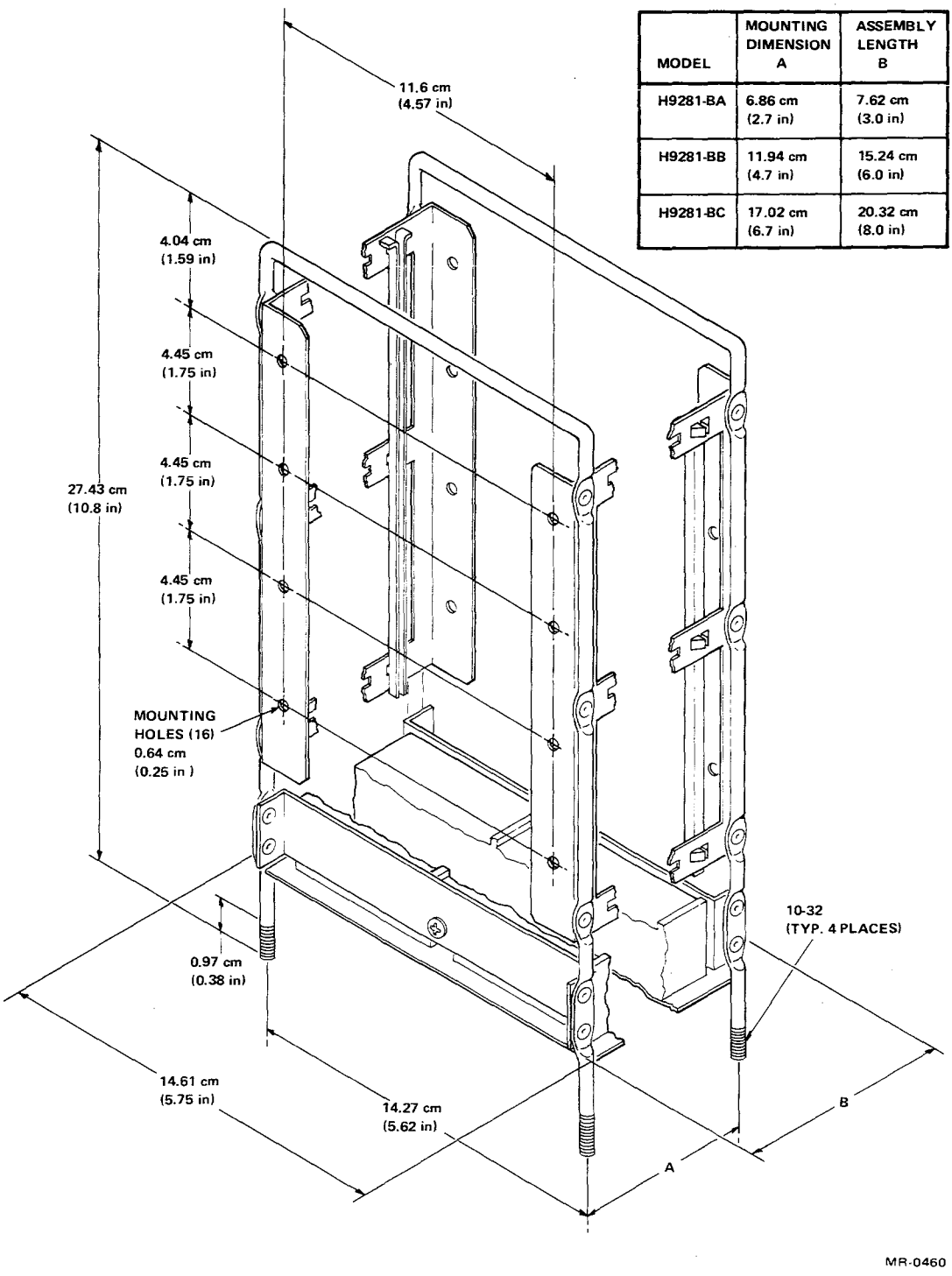


Figure 2 H9281-BA;-BB;-BC Mounting Dimensions

Connecting System Power

Seven screw terminals are provided on the slot 1 end of the backplane for power connections. Connect system power (and optional battery backup power) as shown in Figure 3. Power wiring should be done with a wire gauge appropriate for the total power requirements for options installed in the backplane. The recommended wire size for H9281-AC and -BC backplanes is 12 gauge. 14 gauge is sufficient for the other H9281 models.

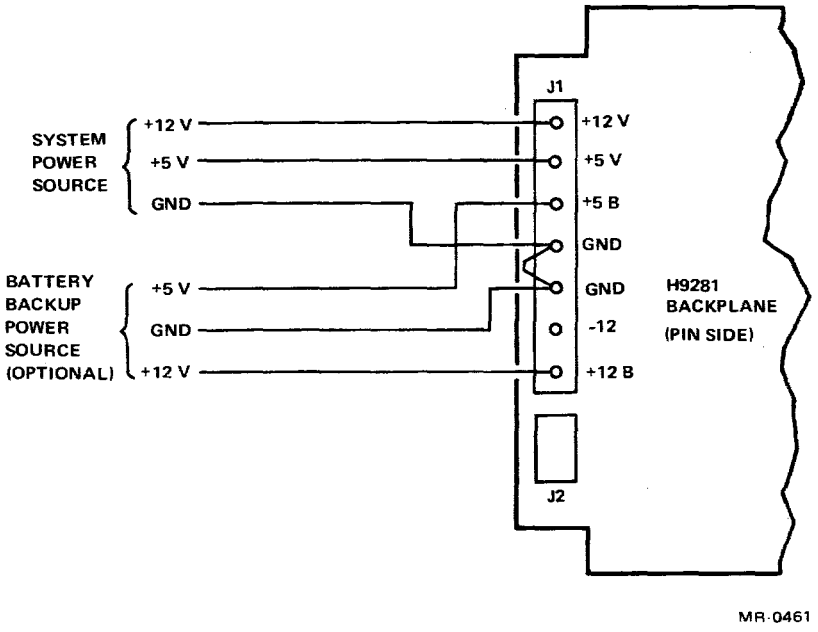


Figure 3 H9281 Power Connections

Select a power supply that will meet LSI-11 system power specifications and supply sufficient current for the options in the system. The H780 power supply is recommended.

Connecting Externally Generated Bus Signals

Externally generated bus signals can be connected to the H9281 backpanel via connector J2. These signals include power sequence signals BPOK H, BDCOK H, BHALT L and BEVNT L. In addition, the processor-generated SRUN L signal is available via J2 for driving a RUN indicator circuit. J2 connector pins are fully compatible with the H780 model series power supply or the KPV11-A power-fail/line-time clock. Signal connector J2 pinning and signal names are identified in Figure 4.

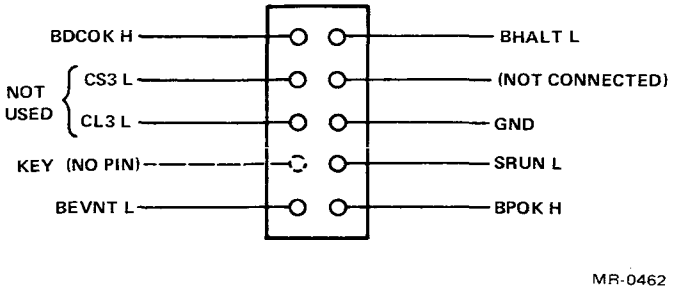


Figure 4 H9281 Signal Connections (J2)

Device Priority

All LSI-11 bus backplanes are priority structured. Daisy-chained grant signals for DMA and interrupt requests propagate away from the processor from the first (highest priority device) to successively lower priority devices. Processor module locations and device (option) priorities are shown in Figure 5.

Bus Terminations

Backplane models H9281-AB, -BB, -AC, and -BC include 120 Ω bus termination resistors at the electrical end of the bus; therefore, it is not necessary to install a separate 120 Ω bus terminator module in these backplanes.

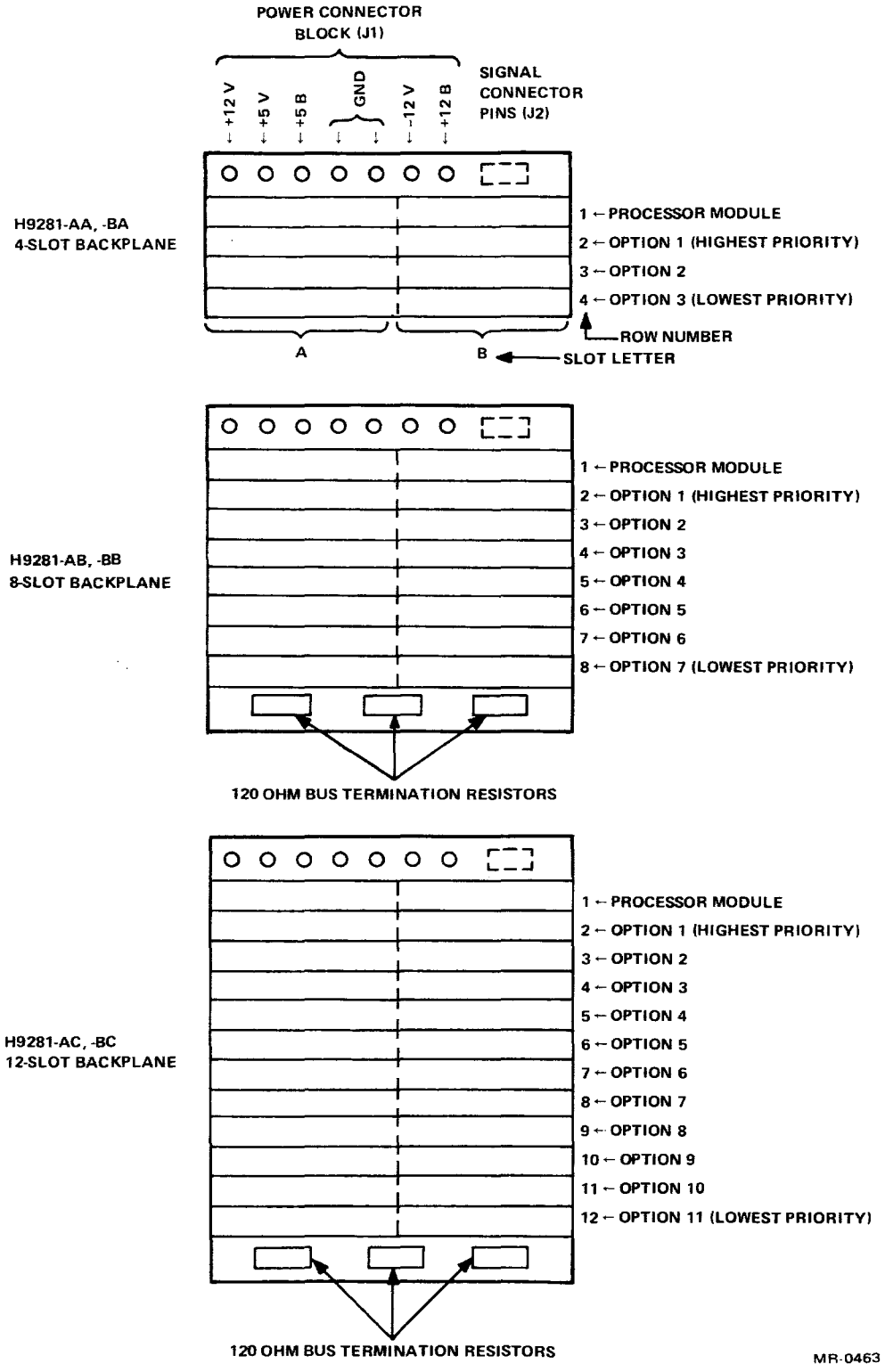


Figure 5 H9281 Option and Connector Locations (Module Side)

IBV11-A

IBV11-A INSTRUMENT BUS INTERFACE

INTRODUCTION

The IBV11-A is an option that interfaces the LSI-11 bus with the instrument bus as described in IEEE Standard 488-1975, "Digital Interface for Programmable Instrumentation." An IBV11-A can be installed in any LSI-11 system. The IBV11-A consists of an M7954 interface module and a BN11A-04 cable for connecting the first instrument. Additional instruments may be connected using a BN01A cable.

The IBV11-A makes an LSI-11 based programmable instrument system possible.

FEATURES

- PDP-11 software-compatible
- 40-Kbyte/sec maximum transfer capability of hardware
- Board-mounted, user-configured switches allow easy device (register address) and interrupt vector address selection
- Software support available under FORTRAN IV
- 5-Kbyte/sec transfer rate under FORTRAN
- System hardware-compatible with the LSI-11 component system
- Instrument bus compatible with the IEEE 488-1975 standard
- The module supports cable lengths up to 20 m (65.6 ft) total
- 15 devices (maximum) can connect to the bus

SPECIFICATIONS

Identification	M7954
Size	Double
Power	+5.0 Vdc ±5% at 0.8 A
Bus Loads	
AC	1.8
DC	1

The IBV11-A, *when connected to the LSI-11,* will meet the following subsets of IEEE Standard 488-1975:

SH1	SR1	C1
AH1	RL1	C2
TS	PP2	C3
TE5	DC1	C4
LE3		

IBV11-A

This module is designed to be the only controller on the IEEE bus. Therefore, it will not respond to another controller on the bus that issues either a parallel poll configure command or a parallel poll control signal.

DESCRIPTION

The functional logic blocks that make up the IBV11-A are shown in Figure 1. LSI-11 software controls and communicates with the IBV11-A via programmed I/O transfers and interrupts. Programmed I/O transfers are made possible by assigning unique device addresses (also called "bus addresses") to the IBS and IBD registers.

LSI-11 Bus Interface

LSI-11 bus address selection, interrupt vector address generation, and bus data driver/receiver (transceiver) functions are provided by transceiver integrated circuits (DC005). Each integrated circuit provides the interface for four BDAL bus lines; thus, four transceivers comprise the 16-line BDAL (0:15) L LSI-11 bus interface.

Bit 1 of the least significant octal digit (BDAL 0) selects the IBS or IBD register. This is a byte pointer and it is significant for DATOB and DATIOB bus cycles only. Register address selection is actually performed in the LSI-11 bus protocol and register selection circuit (DC004); the receiver integrated circuit (DC005) simply routes the received low-order three address bits [DA (2:0)] to that function.

All I/O transfers over the LSI-11 bus are done according to a strict protocol. One bus protocol integrated circuit (DC004) performs both this function and the register address selection previously discussed. When an active ADDRESS MATCH signal is present and BSYNC L signal is asserted, the bus protocol integrated circuit is enabled to complete its register selection function. BWTBT L, BDOUT L, and BDIN L bus signals are decoded in the integrated circuit, as appropriate, to produce the LOAD IBS LOW BYTE, SELECT IBS, LOAD IBD LOW BYTE, and RECEIVE internal control signals from the IBV11-A logic functions. The integrated circuit also asserts BRPLY L as required during the I/O sequence to complete the programmed transfer.

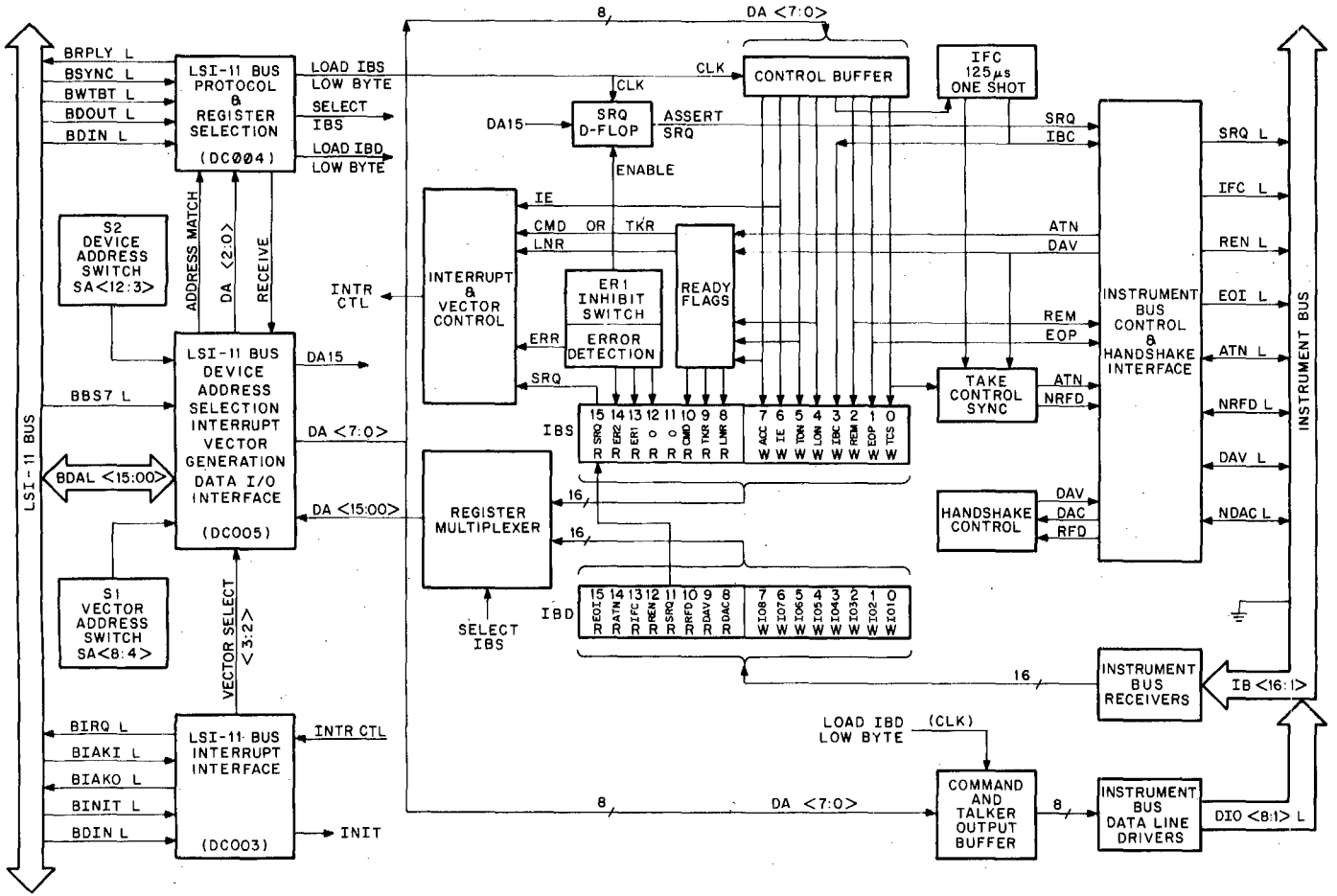


Figure 1 IBV11-A Functional Block Diagram

Interrupts are generated by one interrupt integrated circuit (DC003). Four interrupt vectors can be generated by this bus interrupt interface function. A 5-bit vector switch allows the user to select the interrupt vector for the IBV11-A module. The IBV11-A base interrupt vector is factory-configured for 420. The base interrupt vector can range from 300 to 760; however, the vector interrupt must not conflict with other bus devices, or with those interrupts reserved for system vectors.

Interrupt Vector	Interrupt Source
000420	Error
000424	Service request
000430	Command and talker
000434	Listener

These interrupt vectors allow the IBV11-A to generate interrupts that can most efficiently be serviced by four separate service routines.

Interrupt and vector control logic on the IBV11-A module generates the INTR CTL signals that initiate the interrupts. Inputs for this logic function include the interrupt enable (IE) bit (stored in the control buffer), command or talker (CMD or TKR) and listener (LNR) ready flags, error (ERR) status from the error detection logic, and the device service request (instrument bus control signal).

Instrument Bus Control

The control buffer is an 8-bit register that functions as the low byte of the IBS register. Bits stored in this register control generation of interrupts, instrument bus clear, and instrument bus control and status logic. Setting the IBC bit actually triggers a one-shot producing a 125 μs pulse that clears the instrument bus. Take control sync and handshake control logic function together with instrument bus control and handshake interface logic to communicate with instruments on the bus according to instrument bus protocol. Output transactions with the low byte of the IBD register result in data being stored in the 8-bit command and talker output buffer. Instrument bus line drivers gate this byte onto the instrument bus when the IBV11-A is an active talker, or when it is an active controller.

Instrument Bus Interface

The IBV11-A interfaces with the instrument bus via four integrated circuits, type MC3441. These integrated circuits are bus transceivers, each containing four bus drivers, four bus receivers, and bus terminations that comply with instrument bus specifications.

IBV11-A

CONFIGURATION

The IBV11-A option can be installed in any LSI-11 bus to interface various instruments via an "interrupt bus." The instrument bus is defined in the IEEE Standard 488-1975, "Digital Interface for Programmable Instrumentation." Any instruments designed to interface with the bus defined in that standard can be interfaced to the LSI-11 system via the IBV11-A.

The following paragraphs contain only the basic information necessary for configuring device register addresses and vector interrupts, general installation and interface to the instrument bus, and basic programming (e.g., device register functions).

Device Address

Device address switches provide a convenient means for the user to configure the IBV11-A's register addresses. Only switches corresponding to BDAL lines (3:12) are provided. By PDP-11 convention, the upper 4K address space (bank 7) is normally reserved for peripheral devices, such as the IBV11-A. The processor module asserts BBS7 L whenever a bank 7 address [BDAL (13:15) L is asserted] is placed on the bus. Thus, BBS7 L must be asserted to enable an "address match" output from the address selection function. Any address ranging from 16000X to 17777X can be configured that does not conflict with other device addresses within the system; the X in the address represents register and byte selection within the module.

Each IBV11-A module is factory-configured for a standard device register address (160150) and interrupt vector (420). Switches S1 (interrupt vector) and S2 (device register address) configure the module. A summary of register addressing and interrupt vectors is provided in Figures 2 and 3. Observe that the IBD register address is always the IBS address plus 2. Similarly, only the error interrupt vector is configured. The remaining three vectors are permanently assigned sequential addresses in address increments of four as shown in Table 1.

Table 1 Standard Assignments

Description	Mnemonic	Read/ Write	First Module Address
Registers			
Control/Status	IBS	R/W	160150
Data	IBD	R/W	160152
Vectors			
Error	ER2, ER1		420
Service	SRQ		424
Command and Talker	CMD, TKR		430
Listener	LNR		434

Switches S1 and S2 are located on the IBV11-A module as shown in Figure 4. S1 and S2 are switch assemblies, each containing several individual switches. The individual switches indicated in Figures 2 and 3 are clearly marked on the S1 and S2 assemblies. The ON and OFF positions are also clearly marked.

Interrupt Vectors

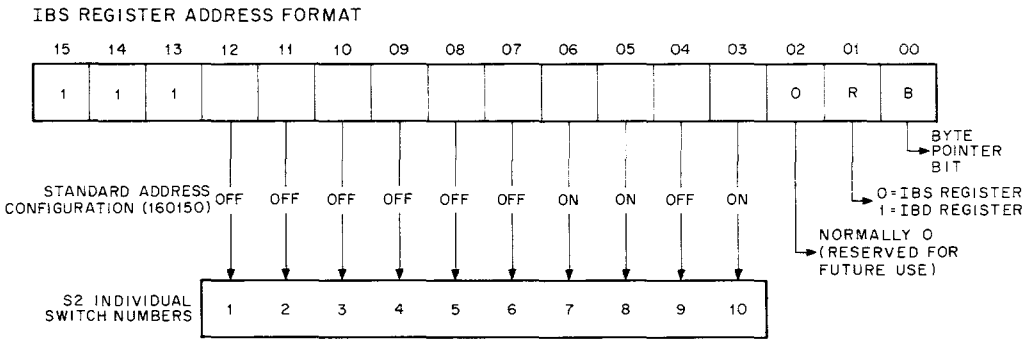
The IBV11-A is capable of generating four separate interrupt requests; each have separate interrupt vectors and normally would have separate service routines. Interrupts can be requested only when the IBS IE (interrupt enable) bit is set. Interrupt requests are priority structured in the IBV11-A. A summary of the four types is provided below.

Priority	Vector	Associated IBS Bit	Cause of Interrupt
Highest	000XNN00	ER2, ER1	Error condition.
Second highest	000XNN04	SRQ	A device connected to the instrument bus is requesting service.
Third highest	000XNN19	TKR, CMD	The IBV11-A is an active talker and is ready for the processor to output a byte to the low byte of the IBD register. (The IBV11-A will normally then transmit the

			byte over the installation bus to the active listener(s).)
Lowest	000XNN14	LNR	The IBV11-A is an active listener and has a data byte to be read by the processor.

NOTES

1. X = User-configured interrupt vector octal digit.
2. N = User-configured interrupt vector binary bits.
3. Associated IBS bits shown, when set, produce interrupt requests if the IE bit is set.

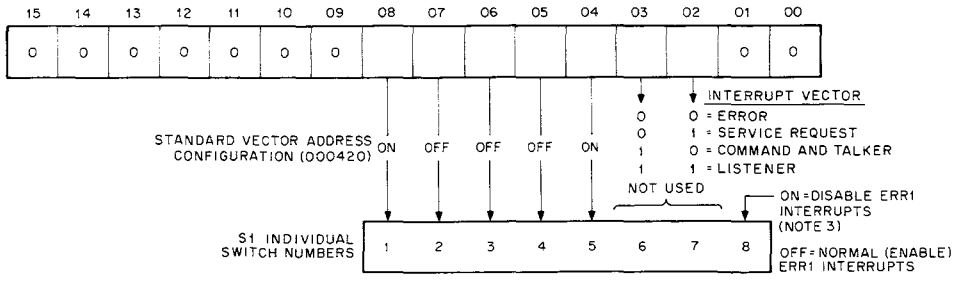


NOTES:

1. OFF = Logical 0; ON = Logical 1
2. Only the IBS REGISTER ADDRESS is configured via S2. The IBD REGISTER ADDRESS always equals the IBS REGISTER ADDRESS +2.

11-4887

Figure 2 Register Addresses



NOTES:

1. OFF = Logical 0; ON = Logical 1
2. Only the VECTOR ADDRESS bits (8:4) are configured via S1. Bits 3 and 2 are IBV11-A hardware-selected for the functions shown
3. S1-8 OFF = IBV11-A is the only system controller connected to the instrument bus.
   S1-8 ON = Another system controller is connected to the instrument bus.

11-4888

Figure 3 Interrupt Vector

IBV11-A

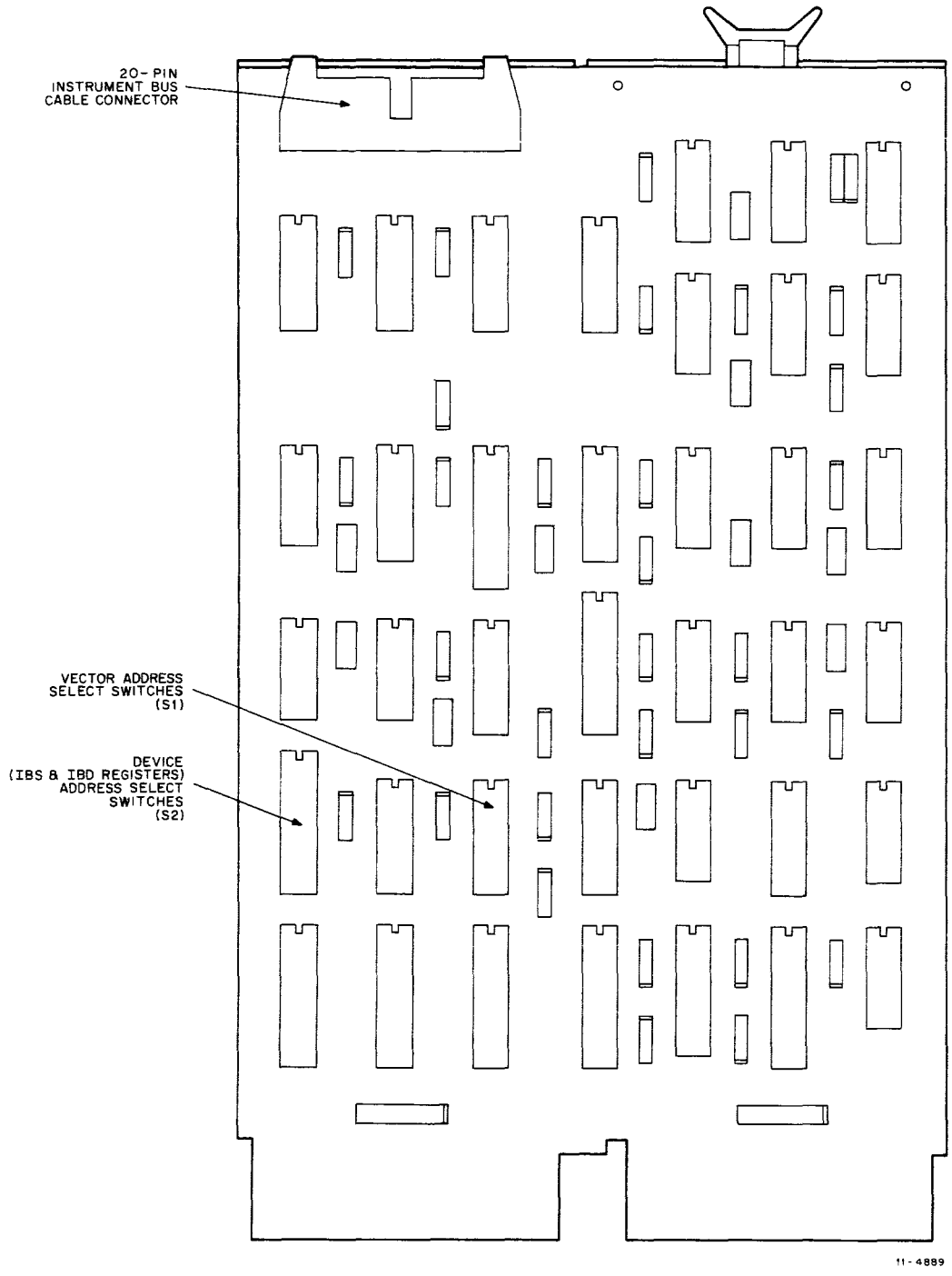


Figure 4 IBV11-A Module Switch Locations

IBV11-A

Interrupt	Interrupt Vector
Error	"n" (configured vector)
Service	n + 4
Command and Talker	$n + 10_8$
Listener	$n + 14_8$

Preferred value range for "n" = $300 \leq n \leq 760$

Registers

The IBV11-A communicates with devices connected to the instrument bus under the control of the program being executed. All communication between the processor and the IBV11-A is via the instrument bus status (IBS) and instrument bus data (IBD) registers. The programmer must be aware of the functional significance of each bit in both registers before any programs can be written that will control specific devices on the instrument bus. In addition, the programmer must establish instrument (device) addresses, and conform to the programming rules specified for each instrument connected to the instrument bus. See Figure 5 for a description of the IEEE bus.

The instrument bus status (IBS) register is similar in function to other device control/status register (CSRs). The instrument bus data (IBD) register is a 16-bit register that contains eight read/write data bits in the low byte and eight read-only bits in the high byte. The eight read-only bits allow the program to read the logical state of the control and management signals of the instrument bus.

The IBS register provides the means for controlling the instrument bus control and management signals, and IBV11-A functions relative to the LSI-11 bus. The low byte of the IBD register, on the other hand, is used for passing commands to devices connected to the bus, and for transmitting and receiving data between the processor and talker and listener devices. In addition, the high byte of the IBD register allows for processor monitoring of all instrument bus signal (control) lines. IBS and IBD registers are shown in Figure 6 and described in Tables 2 and 3.

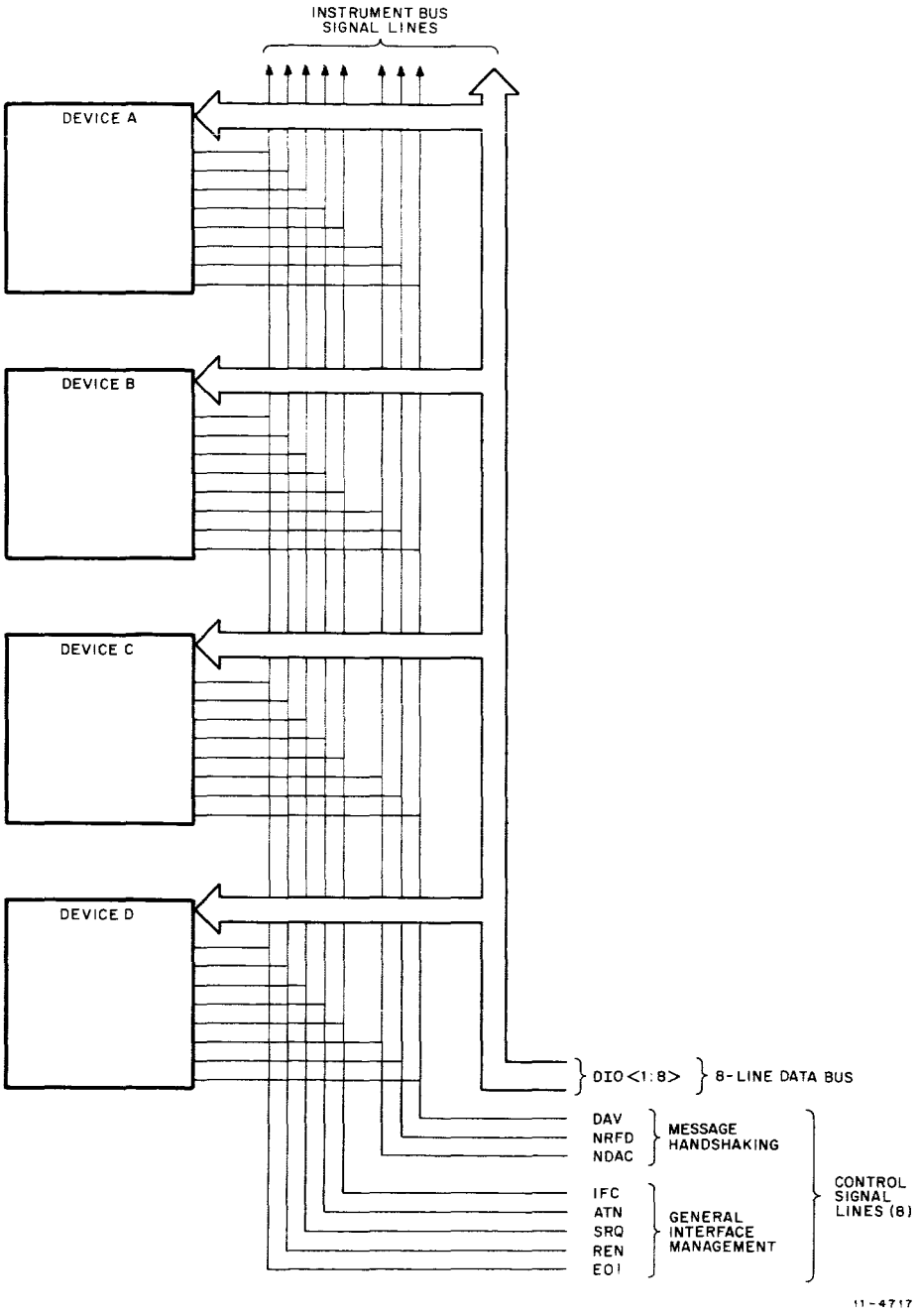


Figure 5 Instrument Bus Signal Lines

INSTRUMENT BUS STATUS (IBS)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SRQ	ER2	ER1	NOT USED	NOT USED	CMP	TKR	LNR	ACC	IE	TON	LON	IBC	REM	EOP	TCS

INSTRUMENT BUS DATA (IBD)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
EOI	ATN	IFC	REN	SRQ	RFD	DAV	DAC	I08	I07	I06	I05	I04	I03	I02	I01

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Figure 6 Register Word Format

Table 2 Instrument Bus Status Word Format

Bit: 15 **Name:** SRQ
Description: (Service Request)
Monitors the state of the instrument bus service request line at all times. Set when the IB SRQ line is low. Will cause an interrupt when both SRQ and the interrupt enable bits are set. When the ER1-inhibit switch is set, this bit will be written by any type of instruction that writes into the IBS. Read/write.

Bit: 14 **Name:** ER2
Description: (Error 2)
Asserted if the IB reports that DAC is true when the IBV11-A tries to send a data or command byte. This condition will exist when there is no active listener or command acceptor on the IB. An ERR interrupt occurs when both the ER2 and the interrupt enable bits are set. Cleared by clearing both TON the TCS. Read-only.

Bit: 13 **Name:** ER1
Description: (Error 1)
Unless inhibited by the ER1-inhibit switch, this bit is asserted whenever a conflict occurs between the IB ATN, IFC, or REN lines and their IBV11-A control hardware, i.e., if one or more of these control lines is asserted when it should not be asserted or not asserted when it should be asserted. When asserted, the IBV11-A will not assert the ATN line even though the TCS bit remains set. An ERR interrupt occurs when both the ER1 and the interrupt enable bits are set. This condition can be cleared only by clearing the cause. Read-only.

Bit: 12 **Name:** Not used
Description: Always read as a zero. Read-only.

Bit: 11 **Name:** Not used
Description: Always read as a zero. Read-only.

Bit: 10 **Name:** CMD
Description: (Command Done)
Set when the IBV11-A is ready to send a command byte; set by a successsful TCS to indicate that ATN was asserted and the first command byte may be issued. Also set by DAC when a command has been completely accepted. A CMD/TKR interrupt occurs when both the CMD and the interrupt enable bits are set. This bit is cleared by INIT, received IFC, writing a command into the IBD low byte, or by turning TCS off. Read-only.

Bit: 9 **Name:** TKR
Description: (Talker Ready)
Set when the IBV11-A is ready to send a data byte; set when TON is on while TCS is turned off, or by DAC when TON is on. A CMD/TKR interrupt occurs when both the TKR and the interrupt enable bits are set. Cleared by INIT, received IFC, writing a data byte into the IBD low byte, or by turning TON off or TCS on. Read-only.

Bit: 8 **Name:** LNR
Description: (Listener Ready)
Set when the IBV11-A has a data or command byte ready for reading from the IBD low byte; set by DAV when LON is on. An LNR interrupt occurs when both the LNR and the interrupt enable bits are set. Cleared by reading the IBD low byte if ACC is off or by clearing the IBD low byte if ACC is on. Also cleared when LON is turned off and by INIT or received IFC. Read-only.

Bit: 7 **Name:** ACC
Description: (Accept Data)
Set and cleared under program control. When clear, reading the IBD will automatically clear the LNR and assert DAC. When set, the programmer must write 0 to the IBD low byte in order to clear the LNR bit and assert DAC. When the TCS, LON, and TON bits are all off (clear), setting this bit will assert NRFD. Cleared by INIT or received IFC. Read/write.

Bit: 6 **Name:** IE
Description: (Interrupt Enable)
Set and cleared under program control to enable and disable all interrupts. Cleared by INIT. Read/write.

Bit: 5 **Name:** TON
Description: (Talker On)
Set and cleared under program control to enable and disable the talker function. Cleared by INIT or received IFC. Read/write.

Bit: 4 **Name:** LON
Description: (Listener On)
Set and cleared under program control to enable and disable the listener function. Cleared by INIT or received IFC. Read/write

Bit: 3 **Name:** IBC
Description: (Interface Bus Clear)
Set under program control to cause the IFC line to be asserted for about 125 μsec. TCS will automatically be asserted at the end of IBC (out-going IFC). Cleared by INIT. Read/write

Bit: 2 **Name:** REM
Description: (Remote On)
Set and cleared under program control to assert and unassert the REN line. Cleared by INIT or received IFC. Read/write

Bit: 1 **Name:** EOP
Description: (End of Poll)
Set and cleared under program control to assert and unassert the E01 line. Cleared by INIT or received IFC. Read/write

Bit: 0 **Name:** TCS
Description: (Take Control Synchronously)
Set and cleared under program control to take control synchronously, or to unassert ATN. Setting TCS will cause NRFD to be asserted for at least 500 ns before DAV is checked. ATN is then asserted when DAV is unasserted; NRFD is unasserted and CMD is set no sooner than 500 ns after ATN is asserted. Cleared by INIT or received IFC. Read/write

---

Table 3 Instrument Bus Data Word Format

Bit: 15 **Name:** EOI
Function: (End or Identify)
Monitors the IB EOI line at all times. Set when the IB EOI line is low. Read-only.

Bit: 14 **Name:** ATN
Function: (Attention)
Monitors the IB ATN line at all times. Set when the IB ATN line is low. Read-only.

Bit: 13 **Name:** IFC
Function: (Interface Clear)
Monitors the IB IFC line at all times. Set when the IB IFC line is low. Read-only.

Bit: 12 **Name:** REN
Function: (Remote Enable)
Monitors the IB REN line at all times. Set when the IB REN line is low. Read-only.

Bit: 11 **Name:** SRQ
Function: (Service Request)
Monitors the state of the instrument bus service request line at all times. Set when the IB SRQ line is low. Will cause an interrupt when both SRQ and the interrupt enable bits are set. Read-only.

Bit: 10 **Name:** RFD
Function: (Ready for Data)
Monitors the IB NRFD line at all times. Set when the IB NRFD line is high. Read-only.

Bit: 9 **Name:** DAV
Function: (Data Valid)
Monitors the IB DAV line at all times. Set when the IB DAV line is low. Read-only.

Bit: 8 **Name:** DAC
Function: (Data Accepted)
Monitors the IB NDAC line at all times. Set when the IB NDAC line is high. Read-only.

Bit: 7-0 **Name:** DIO8-DIO1
Function: IB Data I/O lines
Reading the IBD low byte picks up unlatched data directly from the IB DIO lines. Data on the IB DIO lines may change if the LNR bit is not set. Generally, the only reason to read the DIO lines when LNR is not set is when a parallel poll response is expected. Writing data to the IB DIO lines is permitted when TON is set and DAV is clear, or when TCS and ATN are set and DAV is clear. Otherwise, writing into the IBD low byte will have no effect on the DIO lines but will set DAC if both ACC and LNR are set. Read/write.

The data and command output buffer is cleared by INIT or received IFC.

Connecting the External Equipment
Connection from the IBV11-A to the first device on the instrument bus is via a type BN11A cable (supplied with the M7954 module), as shown in Figure 7. One end is terminated with a 20-pin connector that mates with the 20-pin connector on the IBV11-A module; the other end is terminated with a 24-pin "double-ended" connector that conforms to

the IEEE 488 1975 standard; the cable can be connected to any device conforming to that standard. The double-ended connector contains a male 24-pin and a female 24-pin connector in the same connector housing. This allows for "linear" and "star" connections to instruments connected to the instrument bus, as shown in Figure 8. One BN11A is included in the IBV11-A option.

The linear arrangement shown in the figure includes five devices (or instruments), A through E. There is no particular significance to the sequence shown, or the electrical position along the instrument bus. Unlike the LSI-11 bus, the position along the bus does not structure device priority in the system.

The star arrangement shown in the figure allows five devices to be connected by stacking instrument cable connectors on the BN11A's double-ended connector. Double-ended connectors on instrument bus cables will normally include captive locking screws on each connector assembly (two each), allowing stacked connectors to be secured together in a single assembly.

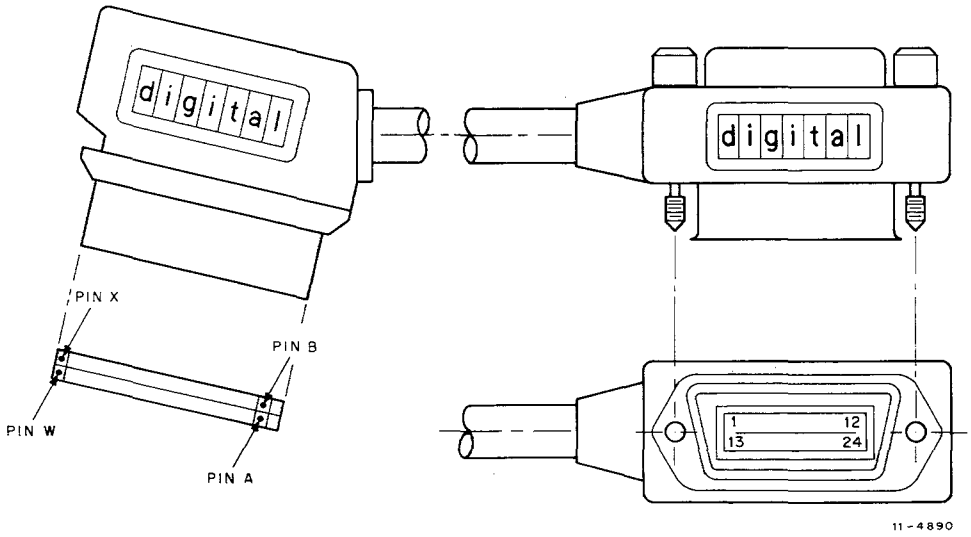


Figure 7 BN11A Instrument Bus Cable

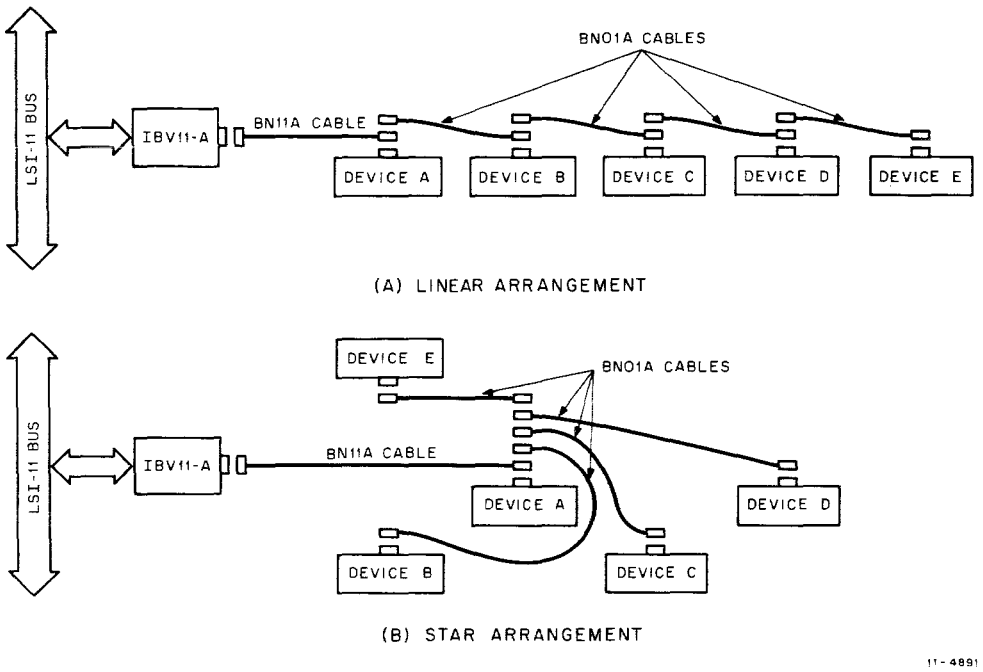


Figure 8 Linear and Star Configurations

The BN11A cable connector pin signal assignments are listed in Table 4 for each connector. One BN11A cable is required for each IBV11-A module in a system.

Optional Cables

1. Connect M7954 module to first instrument:

BN11A-02	2 m (78.7 in)
BN11A-04	4 m (157.5 in)

2. Connect instrument to instrument:

BN01A-01	1 m (39.4 in)
BN01A-02	2 m (78.7 in)
BN01A-04	4m (157.5 in)

Table 4 BN11A Connector Pin Assignments

IBV11-A Connector Pin	Signal Name	Instrument Bus Connector Pin
U	DIO1	1
S	DIO2	1
P	DIO3	3
M	DIO4	4
R	EOI	5
T	DAV	6
V	NRFD	7
X	NDAC	8
B	IFC	9
J	SRQ	10
F	ATN	11
W	(SHIELD)	12
K	DIO5	13
H	DIO6	14
E	DIO7	15
C	DIO8	16
D	REN	17
	GND (DAV GND)	18
N	GND (NRFD GND)	19
	GND (NDAC GND)	20
A	GND (IFC GND)	21
	GND (SRQ GND)	22
L	GND (ATN GND)	23
W	GND (LOGIC)	24

PROGRAMMING

Example 1—IBV11-A to Listener Device

This programming example illustrates how the IBV11-A communicates with a listener device. Standard device and vector addresses are used, as shown in Figures 2 and 3. Once the program is started, and after pointers have been initialized and the IBV11-A has taken control synchronously, it communicates with the IBV11-A via an interrupt-driven service routine. No "background" program is used; the program simply waits until another interrupt occurs.

Communication with the listener device includes the transmission of two command bytes (read as words from a message buffer), followed by 24 message bytes that program device functions. After all message bytes have been transmitted, the program halts (displays HALT PC address = 1066).

A program flowchart for this example is shown in Figure 9; a symbolic listing is shown in Figure 10.

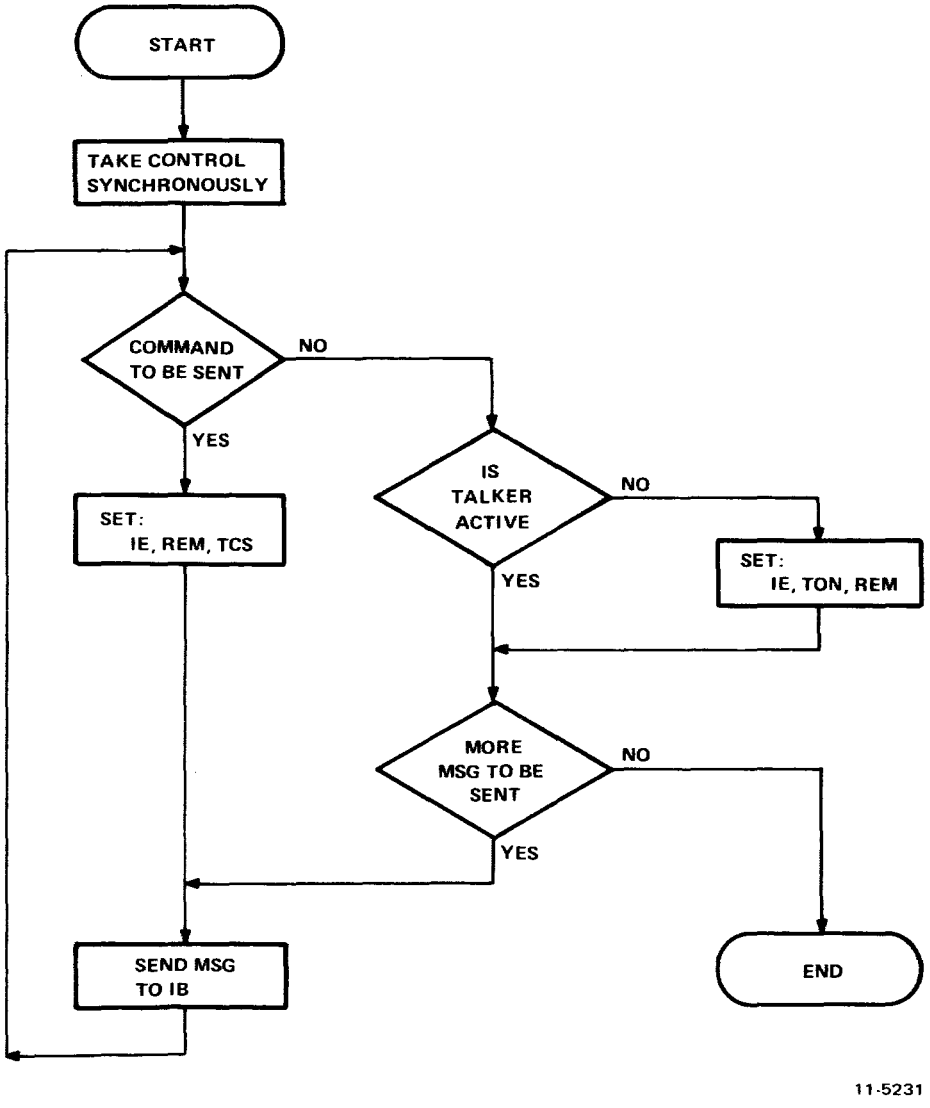


Figure 9 Communicating with a Listener Device (Program Flowchart)

```
ADDRESS   OCTAL CODE     ASSEMBLER SYNTAX          COMMENTS

000430    001020                                   ; INTR RETURN ADDRESS
000432    000200                                   ; PSW

001000    012706   START: MOV #500,R6               ; SET UP STACK POINTER
001002    000500
001004    012700         MOV #2000,R0              ; R0 IS MSG BUFFER ADDRESS
001006    002000
001010    012737         MOV #110,160150           ; TAKE CONTROL
001012    000110                                   ; SYNCHRONOUSLY TO BECOME
001014    160150                                   ; CONTROLLER-IN-CHARGE

001016    000777   WAIT:  BR .                      ; WAIT FOR INTERRUPT
001020    020027         CMP R0,#2004              ; MORE COMMANDS TO BE SENT?
001022    002004
001024    100006         BPL 20$                   ; IF NO,GO TO 20$
001026    012737         MOV #105,160150           ; IF YES,SET IE,REM,AND
001030    000105                                   ; TCS BITS OF IBS REG TO
001032    160150                                   ; ACTIVATE CONTROLLER
001034    012037   SEND:  MOV (R0)+,160152         ; SEND MSG TO IB
001036    160152
001040    000002         RTI                       ; RETURN TO WAIT---FOR
                                                   ; MSG TO BE ACCEPTED
001042    020027   20$:   CMP R0,#2004              ; IS TALKER ACTIVE?
001044    002004
001046    003003         BGT 30$                   ; IF YES,GO TO 30$
001050    012737         MOV #144,160150           ; OTHERWISE SET IE,TON
001052    000144                                   ; AND REM BITS OF IBS REG
001054    160150                                   ; TO ACTIVATE TALKER
001056    020027   30$:   CMP R0,#2064              ; HAD ALL MSG BEEN SENT?
001060    002064
001062    100364         BMI SEND                  ; IF NO,GO SEND ANOTHER MSG
001064    000000         HALT                      ; OTHERWISE STOP
```

11-5232

Figure 10 Communicating with a Listener Device (Program Listing)

Example 2—IBV11-A to Talker Device

This programming example illustrates how the IBV11-A communicates with a talker device. As in example 1, this programming example assumes standard IBV11-A device and interrupt vector addresses. Communication between the instrument and the LSI-11 system is via IBV11-A interrupt-driven service routines. No background program is used; the program simply waits until another interrupt occurs.

Communication with the instrument involves first transmitting the content of the command message buffer, in a manner similar to the program operation described for example 1, followed by accepting instrument output data and storing it in a received data buffer. The content of the command message buffer typically includes first activating the device via its listener address, followed by setting up range mode, operating parameters for the instrument, an execute command, and finally, activating the device as an active talker via its talker address. Once the device has received the command message buffer data, it performs the programmed measurements (or the function, depending on the instrument) and returns data to the LSI-11 system via the IBV11-A. Note that during this portion of program operation, the IBV11-A functions as an active listener on the instrument bus. Once all measurements have been stored by the program, the program halts with a displayed PC address = 1102.

A program flowchart for this example is shown in Figure 11 and a symbolic program listing is shown in Figure 12.

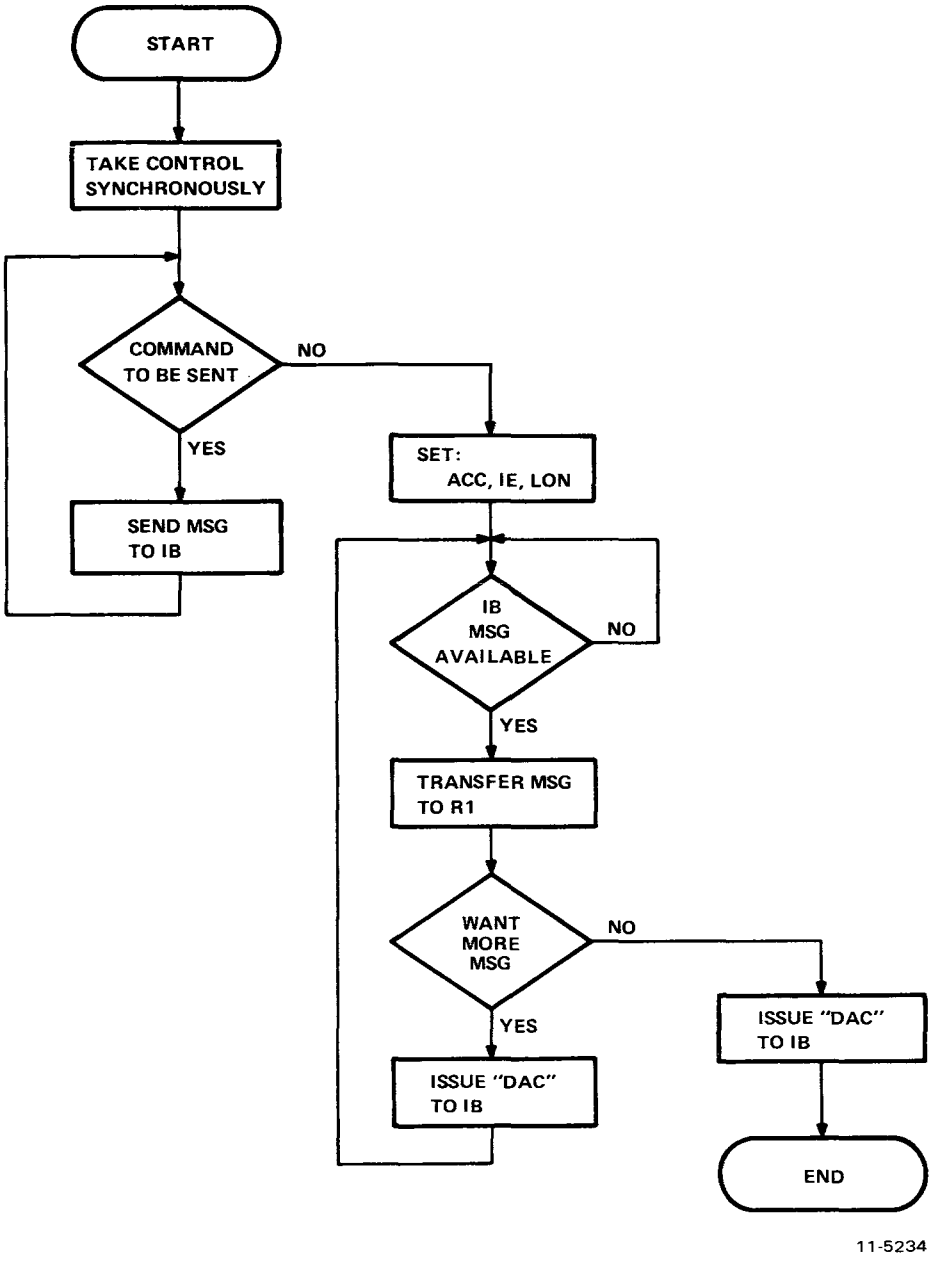


Figure 11 Communicating with a Talker Device (Program Flowchart)

```
ADDRESS  CODE    ASSEMBLER SYNTAX          COMMENTS

000430   001024                            ; COMMAND/TALKER INTR
                                           ; RETURN ADDRESS
000432   000200                            ; PSW
000434   001056                            ; LISTENER RETURN ADDRESS
000436   000200                            ; PSW

001000   012706  START:  MOV #500,R6        ; SET UP STACK
001002   000500
001004   012700         MOV #2000,R0       ; IBV11-A MSG BUFFER
001006   002000
001010   012701         MOV #2500,R1       ; BUFF FOR RECEIVED MSG
001012   002500
001014   012737         MOV #110,160150    ; TAKE CONTROL SYNCHRONOUSLY
001016   000110                            ; TO BECOME CONTROLLER-
001020   160150                            ; IN-CHARGE,C-I-C
001022   000777  WAIT:   BR .               ; WAIT--FOR INTERRUPT
001024   012737         MOV #105,160150    ; PREPARE TO SEND
001026   000105                            ; COMMAND MESSAGES
001030   160150
001032   022700         CMP #2024,R0       ; HAD ALL COMMANDS
001034   002024                            ; BEEN SENT?
001036   001404         BEQ 20$            ; IF YES,GO TO 20$
001040   012037         MOV (R0)+,160152   ; OTHERWISE SEND MSG
001042   160152
001044   000002         RTI                ; RETURN TO WAIT--FOR
                                           ; MSG TO BE ACCEPTED
001046   012737  20$:    MOV #320,160150    ; IBV11-A SWITCHES FROM
001050   000320                            ; CONTROLLER TO LISTENER
001052   160150
001054   000002         RTI                ; RETURN TO WAIT--
                                           ; FOR DMM MSG
001056   013721         MOV 160152,(R1)+   ; SAVE THE RECEIVED
001060   160152                            ; MSG IN R1
001062   022701         CMP #2540,R1       ; HAD 20 (OCTAL) MSG
001064   002540                            ; BEEN ACCEPTED?
001066   001403         BEQ 30$            ; IF YES,GO TO 30$
001070   005037         CLR 160152         ; OTHERWISE ISSUE DAC
001072   160152
001074   000002         RTI                ; RETURN TO WAIT--FOR
                                           ; ANOTHER DMM MSG
001076   005037  30$:    CLR 160152         ; ISSUE DAC TO IB
001100   000000         HALT               ; STOP,20 MSG RECEIVED
```

11-5235

Figure 12 Communicating with a Talker Device (Program Listing)

KPV11-A,-B,-C
POWERFAIL/LINETIME
CLOCK/TERMINATOR

The KPV11 is an LSI-11 powerfail/linetime clock (LTC) generator. Three versions of the KPV11 are available: KPV11-A, which has only powerfail and LTC functions; KPV11-B, which has 120Ω bus terminations in addition to the powerfail and LTC; and KPV11-C, which is similar to the KPV11-B, but has 220 bus terminations. The KPV11 is compatible with all LSI-11 component systems and LSI-11 backplane options. It is designed for installation into any LSI-11 bus-structured backplane or remote installation (not installed into a backplane) via an optional cable which connects the KPV11 to the LSI-11 backplane. In order to use the KPV11-B or KPV11-C as bus terminators, they must be installed in the LSI-11 backplane. An optional console panel and bezel are available for annual control of the LTC and the display of dc power on/off status and the processor run/halt state.

FEATURES

- Automatic generation of BPOK and BDCOK powerup/powerdown signal sequence
- Automatic program restoration and starting when used with non-volatile memory and appropriate software routines
- Linetime clock time reference provided by a signal source (user supplied) other than the powerline
- KPV11-B and KPV11-C provide bus termination when plugged into an LSI-11 backplane
- Can be installed into the LSI-11 backplane or mounted remotely. An optional cable (DIGITAL part no. 70-12754) connects the KPV11 to the LSI-11 backplane
- Expandable with the 54-11808 console panel option

KPV11-A, -B, -C

SPECIFICATIONS

Identification	M8016 (KPV11-A) M8016-YB (KPV11-B) M8016-YC (KPV11-C)
Size	Double
Power	+5 Vdc ±5% at 560 mA
System dc	
dc Sensing Inputs	+5 Vdc ±5% at 0.11 mA +12 Vdc ±3% at 0.82 mA
ac Line Monitor Input	24 Vac ±10% at 200 mA with grounded center tap (Figure 4)
Bus Loads	
ac	1.6
dc	1.0
Options	
54-11808	Console Panel (PC assembly)
70-11656	Console Bezel
70-12754	Remote Signal Cable (for remote mounting of KPV11)
70-086120	Console Signal/Power Cable (for connecting optional console panel to the KPV11)

CONFIGURATION

The KPV11 can be installed into any LSI-11 system backplane or into a remote installation (not installed in a backplane). All KPV11 installations require a user-supplied, 24 Vac, center-tapped transformer capable of supplying at least 0.2 A. Remote KPV11 installations also require the optional remote-signal cable (part no. 70-12754). Users requiring manual control of the LTC and desiring the display of dc power on/off status and processor run/halt status need the optional console panel, console bezel, and console signal/powercable. Mounting hardware for the console panel and remote installation must be provided by the user.

Configuring LTC Jumpers

LTC jumpers are located on the KPV11 module as shown in Figure 7 and are factory-configured for programmable operation with the LKS (line- clock status) register at address (177546) as shown in Figure 8. Normally, it will not be necessary to reconfigure LTC jumpers; however, it is possible to alter LTC operation as listed in Table 1 and the LKS device address as shown in Figure 8 and listed in Table 2.

KPV11-A, -B, -C

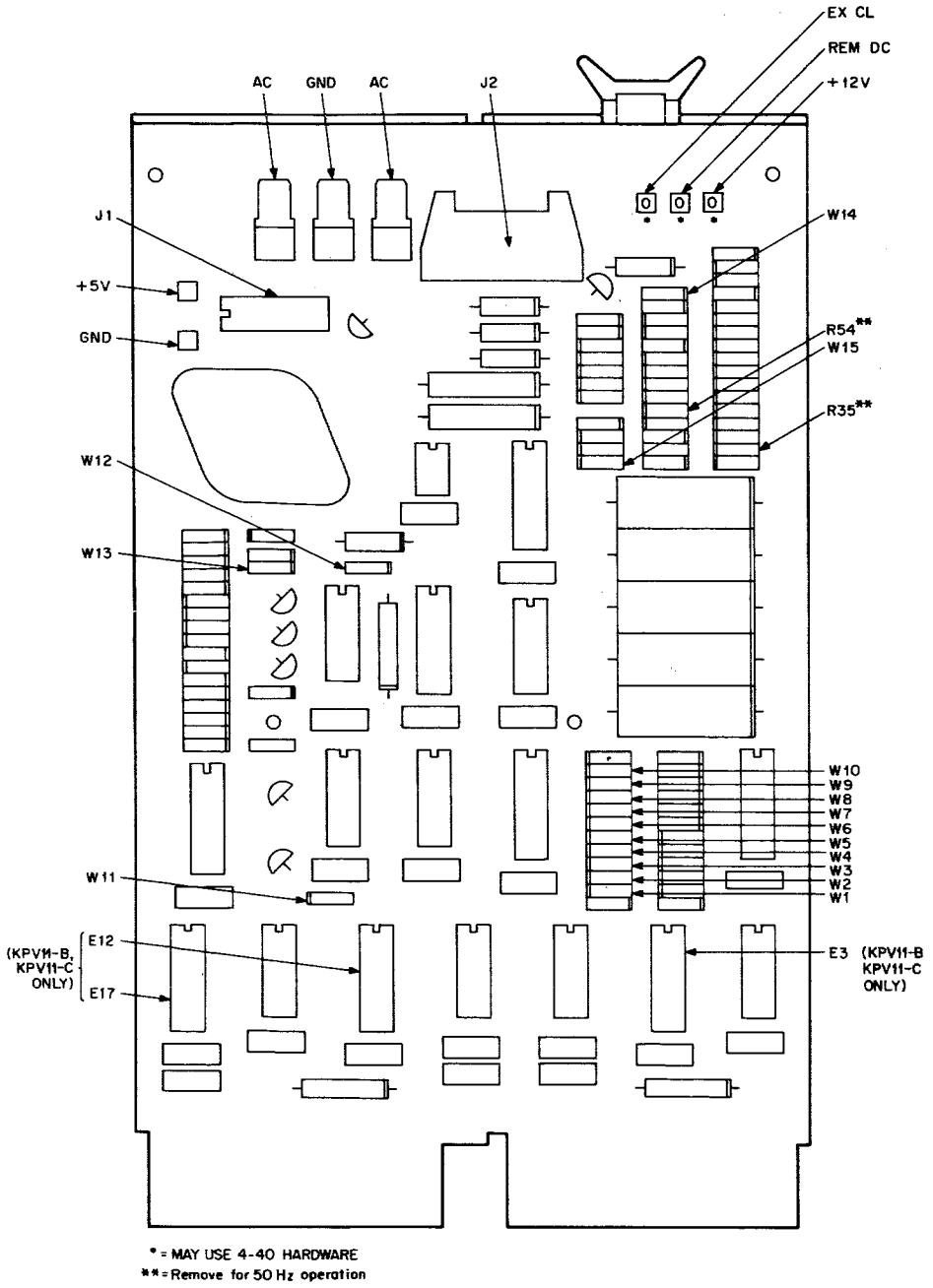


Figure 1 Jumper, Connector, Resistor, and Pad Locations

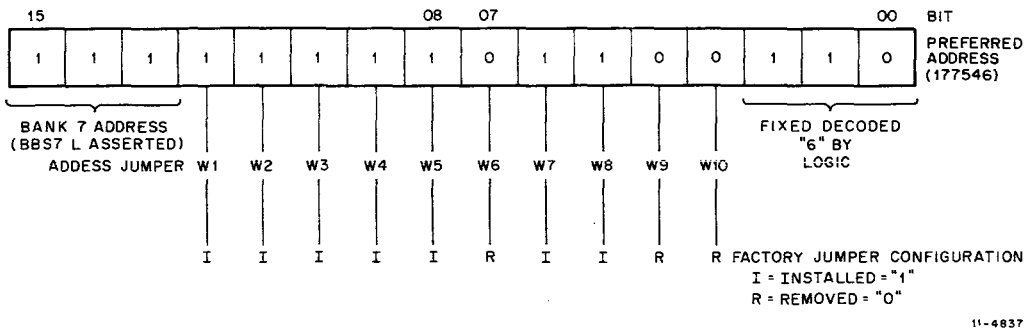


Figure 2 Device Address (LKS Register) Jumpers

Table 1 LTC Jumpers

Jumper	Installed	Removed
W12	Enable manual control or continuous LTC interrupt request operation. Do not install when W13 is installed.	*Disable continuous or manual operation.
W13	*LTC interrupt requests can be enabled and disabled by program. Do not install when W12 is installed.	LTC interrupt requests cannot be program controlled.
W14	*Console (optional) LTC ON/OFF switch enabled.	Console LTC ON/OFF switch disabled.
W15	*LTC signal occurs at the power line frequency.	LTC frequency is determined by an external source via EXT TIME REF etched pad on module.

* Factory-jumpered configuration

KWV11-A PROGRAMMABLE REAL-TIME CLOCK

INTRODUCTION

The KWV11-A is a programmable clock/counter that provides a variety of means for determining time intervals or counting events. It can be used to generate interrupts to the processor at predetermined intervals, or to synchronize the processor ratios between input and output events. It can also be used to start the ADV11-A analog-to-digital converter either by clock counter overflow or by the firing of a Schmitt trigger.

The clock counter has a resolution of 16 bits and can be driven from any of five internal crystal-controlled frequencies (100 Hz to 1 MHz), from a line frequency input or from a Schmitt trigger fired by an external input. The KWV11-A can be operated in any of four programmable modes: single interval, repeated interval, external event timing, and external event timing from zero base.

The KWV11-A includes two Schmitt triggers, each with integral slope and level controls. The Schmitt triggers permit the user to start the clock, initiate A/D conversions, or generate program interrupts in response to external events.

FEATURES

- Resolution of 16 bits
- Can be driven by an external input or from any of five internal frequencies
- Four programmable modes
- Slope and reference signal level selection switches
- Can be used to start the ADV11-A analog-to-digital converter.

SPECIFICATIONS

Identification	M7952
Size	Quad
Power	+5 Vdc ±5% at 1.75 A +12 Vdc ±3% at 0.01 A
Bus Loads	
ac	3.4
dc	1
Operational	
Clock	
Accuracy	0.01%
Range	Base frequency (10 MHz) divided into five selectable rates (1 MHz, 100 kHz, 10 kHz, 1 kHz, 100 Hz); line frequency; Schmitt trigger 1 input

KWV11-A

Input Signals	
ST1 IN (Schmitt Trigger 1 Input)	
Input Range m(maximum limits)	−3V to +30V
Assertion Level	Depends upon position of slope reference selector switch and level control; triggering range = −12 V to +12V
Origin	User device
Response Time	Depends on input waveform and amplitude; typically 600 ns with TTL logic input
Hysteresis	Approximately 0.5V, positive and negative
Characteristics	Single-ended input; 100 KΩ impedance to ground
ST2 IN (Schmitt Trigger 2 Input)	
Same description as ST1 IN	
Output Signals	
CLK OV (Clock Overflow)	Low
Asserted Level	User device or ADV11-A
Destination	Approximately 500 ns
Duration	TTL open-collector driver with 470 Ω pull-up to +5V
Characteristics	Maximum source current from output through load to ground when output is high (≥2.4V): 5 mA
	Maximum sink current from external source voltage through load to output when output is low (≤0.8V): 8 mA
ST1 Out (Schmitt Trigger 1 Output)	
Same description as CLK OV	
ST2 Out (Schmitt Trigger 2 Output)	
Same description as CLK OV	

CONFIGURATION

The following paragraphs describe the procedure for device and interrupt vector address selection, slope and reference level selection, user connections, and programming. (Refer to the ADV11-A when using the KWV11-A with that module.)

Device Address Selection

The KWV11-A contains two device registers that can be addressed by the processor. These registers are the control/status register (CSR) and buffer/preset register (BPR). The BPR's address is always equal to the CSR address plus two. Thus, only the CSR address is configured by the user, as shown in Table 1.

Table 1 Standard Assignments

Description	Mnemonic	Read/ Write	First Module Address
Register			
Control/Status	CSR	R/W	170420
Buffer/Preset	BPR	R/W	170422
Interrupts			
Clock Overflow	CLK OV	—	440
Schmitt Trigger 2	ST2	—	444

Switch pack S1 (Figure 2) contains 10 switches; each corresponds to an address bit as shown in Figure 3. The ON positions select a logical 1 bit address; similarly, the OFF positions select logical 0s. The CSR address can be configured for any address ranging from 17000 to 17777r, with the least significant octal digit configured for 0 or 4. The recommended KWV11-A CSR address is 170420; S1 is shown configured for this address in Figure 2. Note that the BPR address, based on the recommended CSR address, is 170422.

Interrupt Vector Selection

The KWV11-A can interrupt the processor for clock overflow and Schmitt trigger 2 (ST2) services. Thus, two interrupt vectors are produced by the KWV11-A. Switch pack S3 (Figure 4) selects the vector for the clock overflow interrupts; the ST2 interrupt vector is always

equal to the clock overflow interrupt vector plus four. S3 contains seven switches (one not used) that correspond to vector bits (03:08), as shown in Figure 4. Configure the desired clock overflow interrupt vector. The recommended address is 000440.

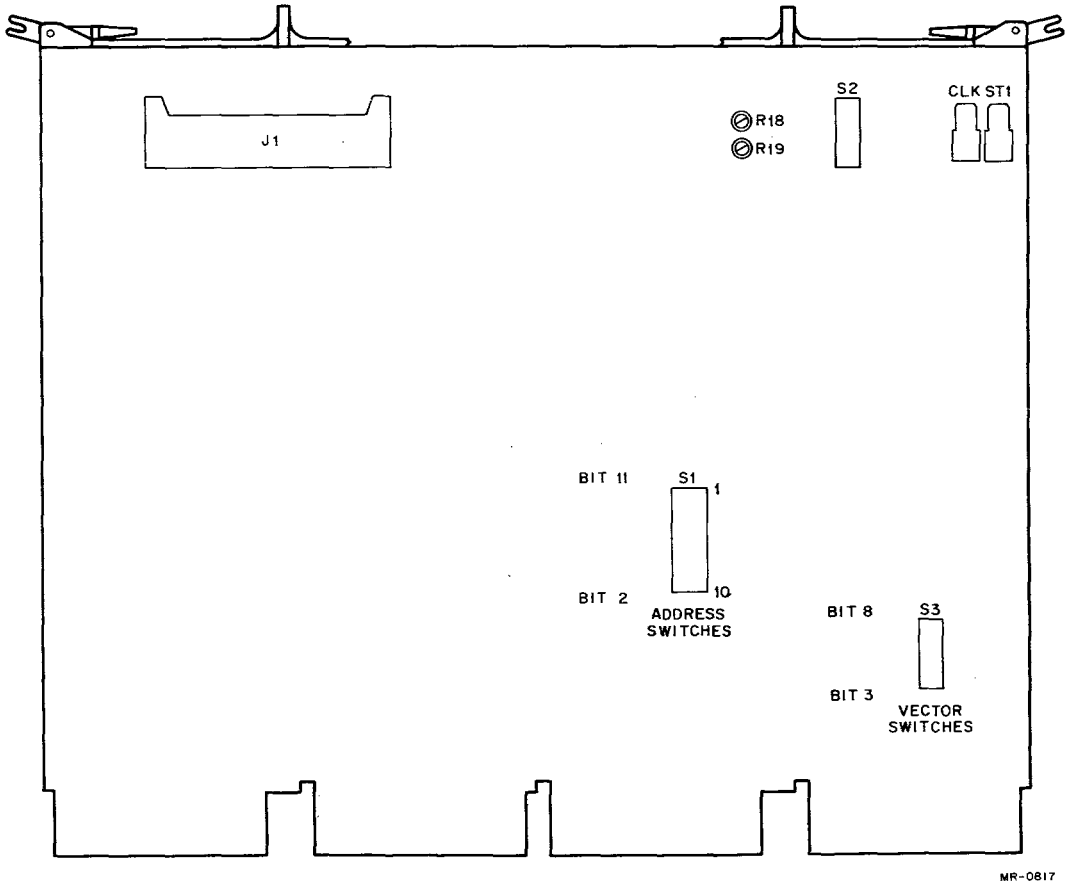


Figure 2 KWV11-A Connectors, Switches, and Controls

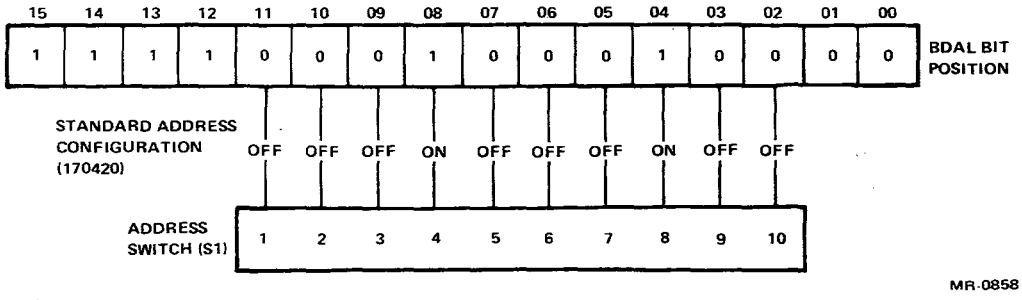


Figure 3 KWV11-A CSR Address Switches

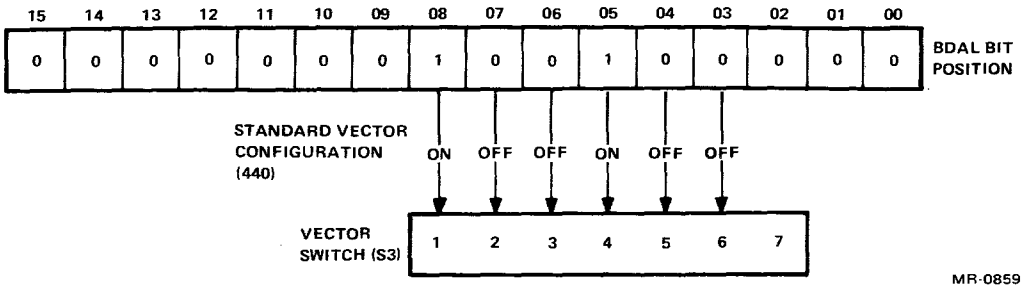


Figure 4 KWV11-A Vector Address Switches

Slope and Reference Level Selection

Slope and reference level switches and controls are shown in Figures 2 and 5. Two reference modes are selectable for each Schmitt trigger—one that picks a fixed level appropriate to TTL logic, and one that picks a variable level that permits setting the ST threshold to any point between −12V and +12V.

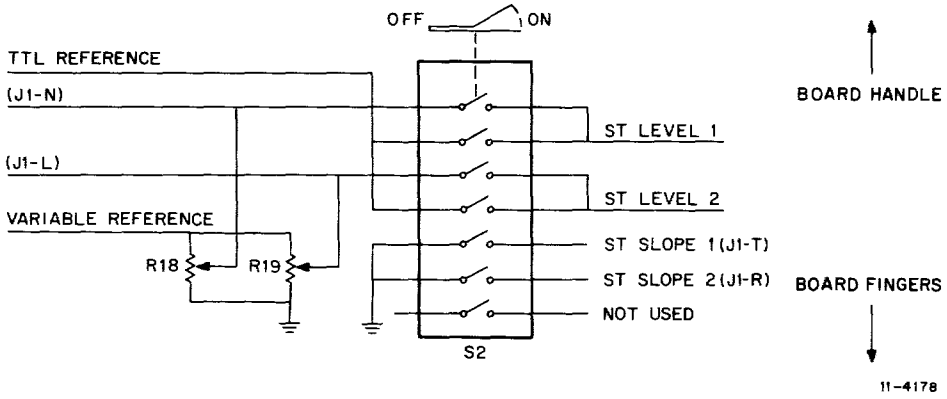


Figure 5 KWV11-A Slope/Reference Level Selector Switches and Controls

Slope selection is accomplished by separate switches for ST1 and ST2, respectively. When the related switch is on, the firing point effectively occurs on the positive slope of the input waveform. When the switch is off, the firing point occurs on the negative slope. R18 or R19 is used to set the level of the reference. Typical slope selection is shown in Figure 6.

NOTE

Users should take care that both TTL and variable switches for either Schmitt trigger are not on simultaneously. This condition will not damage components, but produces unpredictable reference levels. Note also that if no signal is connected to a Schmitt trigger input, both threshold switches for that ST should be open for noise immunity. Alternatively, ST1 IN and ST2 IN can be grounded externally.

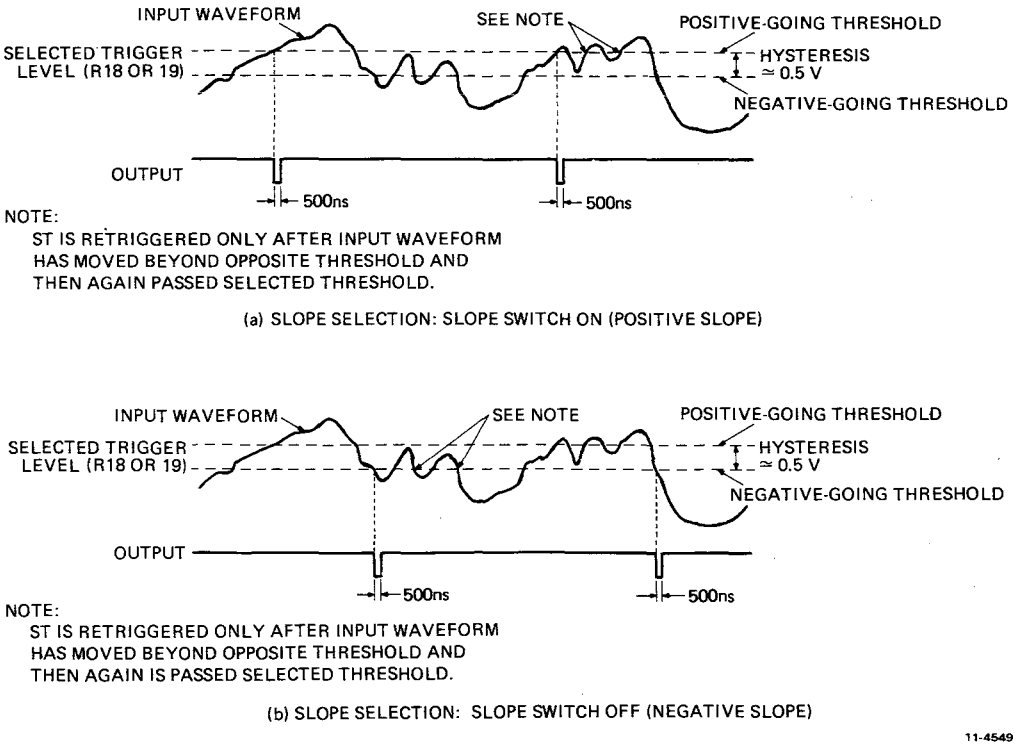


Figure 6 KWV11-A Slope Selection

KWV11-C PROGRAMMABLE REALTIME CLOCK

INTRODUCTION

The KWV11-C is a programmable realtime clock printed circuit board, M4002. It can be programmed to count from one of five crystal-controlled frequencies, from an external input frequency or event, or from the 50/60 Hz line frequency on the LSI-11 bus. The board can generate interrupts or can synchronize the processor to external events. The KWV11-C has a counter that can be programmed to operate in any one of the following modes.

Mode	Counter Operation
0	Single interval
1	Repeated interval
2	External event timing
3	External event timing from zero base

The KWV11-C has two Schmitt triggers that can be set to operate at any level between ± 12 V on either the positive or negative slope of the external input signal. In response to external events, the Schmitt triggers can start the clock, start A/D conversions in an A/D input board, or generate program interrupts to the processor.

- Resolution of 16 bits
- Five internal crystal frequencies—1 MHz, 100 kHz, 10 kHz, 1 kHz, and 100 Hz.
- Two Schmitt triggers, each with slope and level controls that can be used to start the clock or generate program interrupts.
- Line frequency input from BEVNT bus signal (50/60 Hz).
- Four programmable modes.

SPECIFICATIONS

Identification	Dual-height module, M4002
Power Requirement	+5 V ± 5% @ 2.2 A +12 V ± 3% @ 13 mA
Bus Loads	
DC bus loads	1
AC bus loads	1.0
Clock	
Crystal oscillator	10 MHz base frequency
Output ranges	1 MHz, 100 kHz, 10 kHz, 1 kHz, and 100 Hz

Oscillator accuracy	0.01%
Other sources	Line frequency or input at Schmitt trigger 1
I/O Connector	40 pins; 3M no. 3417-7040

Schmitt Trigger Input Signals

No. of inputs	2
Input range	±30 V (max limits)
Triggering range	−12 V to +12 V adjustable
Triggering slope	Positive or negative, switch selectable
Source	User device
Response Time	Depends on input waveform and amplitude; for TTL logic levels, typically 600 ns.
Hysteresis	Approximately 0.5 V, positive and negative
Characteristics	Single-ended input with 100 KΩ impedance to ground

Clock Output

Single	CLK OV L (clock overflow, asserted low)
Output pins	J1 pin RR and CLK OVFL tab
Function	Time base selection from an internal crystal-controlled frequency, an input at ST1, or a line frequency at BEVNT bus line.
Duration	Approximately 500 ns
Line driver	TTL compatible, open collector circuit with 470 Ω pull-up resistor to +5 V.
Max source current	5 mA when output is high (≥ 2.4 V), measuring from source through load to ground.
Max sink current	8 mA when output is low (≤ 0.8 V), measuring from external source voltage through load to output.

Schmitt Trigger 1 Output

Signal	ST1 OUT L (asserted low)
Output pins	J1 pin UU and ST1 OUT tab

Function	External time base input or counter of external events. Input frequency is a function of the input signal.
Other characteristics	Same as clock output.

Schmitt Trigger 2 Output

Signal	ST2 OUT L (asserted low)
Output pins	J1 pin SS
Function	Starts counter, sets ST2 flag, and generates an interrupt (if enabled); causes buffer preset register (BPR) to be loaded from counter.
Other characteristics	Same as clock output.

Environment

Temperature, operating	5°C to 60°C (41°F to 140°F)
Temperature, not operating	−40°C to 66°C (−40°F to 150°F)
Relative humidity, operating	10% to 95% with max. wet bulb of 32°C (90°F) and min. dew point of 2°C (35°F)not condensing

DESCRIPTION

Figure 1 shows a block diagram of the KWV11-C. It has two read/write registers that can be addressed by the processor— the control/status register (CSR) and the buffer/Preset register (BPR). Two switch packs on the board allow the user to select the starting device address for these registers and the starting interrupt vector address.

The DMA bus transceivers monitor and generate bus signals for interrupts, data transfers, and addressing and timing controls. The bus transceivers receive address and data information from the LSI-11 bus. When an address match occurs, the bus transceivers transfer data to or from the control/status register or the buffer/Preset register.

Control/Status Register

The control/status register (CSR) allows the processor to control the operation of the KWV11-C and to get status information on its current operating condition. The CSR has bits to enable interrupts, mode se-

lection, clock rate selection, and starting the counter (GO bit). The CSR monitors the counter overflow flag, flag overrun, and the Schmitt trigger flag (ST2). In addition, the CSR enables some maintenance operations.

Buffer/P reset Register and Counter

The buffer/P reset register (BPR) is a 16-bit, word-addressable, read/write register. This register has two functions, depending on the mode of operation selected. In mode 0 or 1, the BPR is loaded from the program with the clock count. The clock count is the 2's complement of the number of clock inputs the counter is to receive before it overflows. The clock overflow (CLK OV L) sets a flag in the CSR and generates an interrupt request (if enabled). CLK OV L can also be connected directly to an A/D input board to start an A/D conversion.

In mode 2 or 3, the BPR provides indirect reading of the clock counter. An input to Schmitt trigger 2 (ST2) causes the BPR to be loaded with the contents of the counter. The counter is an internal register that is accessible only by reading the BPR in these modes. The counter keeps track of the number of clock pulses from the clock selector or the number of input pulses at Schmitt trigger 1 (ST1).

Oscillator, Divider, and Clock Selector

The clock selector provides the clock input to the counter. The clock selector has eight inputs, five of which are derived from a 10 MHz crystal oscillator and frequency divider network. The other inputs are: STOP, BEVNT, and ST1. STOP halts the counter; BEVNT is a 50 or 60 Hz line clock input from the LSI-11 bus; ST1 (Schmitt trigger 1) can be used as an input for an external clock or as an input to count external events.

Mode Control

CSR bits 1 and 2 determine the mode of operation of the KWV11-C. These bits are decoded in the mode control logic as follows.

CSR Bit		
2	**1**	**Mode Selected**
0	0	Mode 0—Single interval
0	1	Mode 1—Repeated interval
1	0	Mode 2—External event timing
1	1	Mode 3—External event timing from zero base

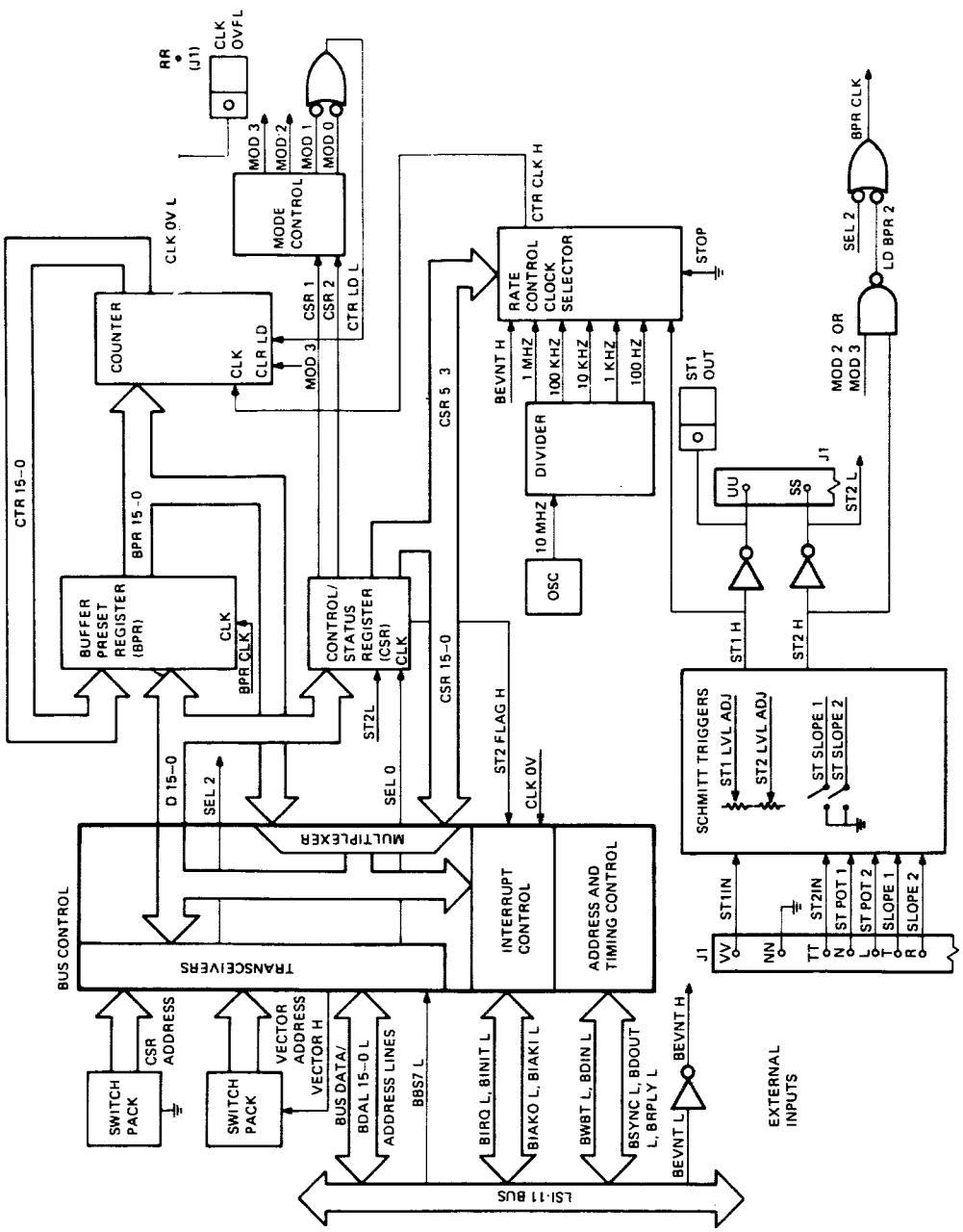


Figure 1 KWV11-C Functional Block Diagram

In either mode 0 or 1, the counter is loaded from the buffer/P reset register. In mode 0, the counter increments at the clock selected rate until it overflows, then it waits for another GO command. In mode 1, the counter continues to count even after an overflow and can cause an interrupt at repeated intervals.

In mode 2, the counter increments at the clock-selected rate (or at rate of external input). An input at ST2 causes the contents of the counter to be loaded into the BPR, where it can be read by the processor. In mode 3, the counter is reset to zero after loading its contents into the BPR.

In all modes, if a second overflow occurs before the processor services the first overflow, or if a second ST2 input tries to set a previously set ST2 FLAG, a flag overrun bit is set in the CSR.

Schmitt Triggers

The KWV11-C has two Schmitt triggers—ST1 and ST2. Both have switches to select the threshold level and the slope selection (positive or negative). Selecting a positive slope allows the Schmitt trigger to fire on a low-to-high transition of the input signal; selecting a negative slope allows the Schmitt trigger to fire on a high-to-low transition.

The Schmitt triggers are used in different ways.

ST1 — Schmitt trigger 1 can be an external time base input or an external input for signals to be counted. ST1 is one of the inputs to the clock selector and can be selected as the clock for the counter. ST1 also goes to connector J1 and to tab ST1 OUT. A jumper wire cna be connected from this tab to the RTC IN jumper pin on the A/D input printed circuit board.

ST2 — Schmitt trigger 2 can be used to start the counter, to set a flag in the CSR, or to generate an interrupt to the processor. When the ST2 GO ENABLE bit is set in the CSR, the ST2 input sets the GO bit, which starts the counter, sets the ST2 flag in the CSR, and generates an interrupt (if enabled).

PROGRAMMING THE KWV11-C

The KWV11-C has the following two programmable read/write registers.

Control/Status Register (CSR)
Buffer/P reset Register (BPR)

KWV11-C

The standard address and interrupt vectors for the KWV11-C are shown in Table 1. This paragraph describes these registers and defines their bits.

Table 1 KWV11-C Standard Address Assignments

Description	Mnemonic	Address
Registers		
Control/Status	CSR	170420_8
Buffer/P reset	BPR	170422_8
Interrupt Vectors		444_8
Clock Overflow	CLK OV	440_8
Schmitt Trigger 2	ST2	

KWV11-C Control/Status Register

Figure 2 shows the bit assignments in the control/status register. Each bit can be written or read under program control; however, the maintenance bits, the flags, and the go bits have special programming considerations.

- The maintenance bits (8, 9 and 10) always read 0.
- The flags (7, 12, and 15) cannot be set by the program.
- The go bits (0, 13) can be cleared by more than one method.

Table 2 defines each bit in the CSR.

KWV11-C Buffer/Preset Register

The address of the buffer/p reset register is the standard device address +2, or 170422_8. This register has two purposes. During mode 0 or 1 operation, this register is used to load the number of clock counts before the counter overflows. During mode 2 or 3 operations, this register is used to read the current count from the counter. Reading the BPR, indirectly reads the counter.

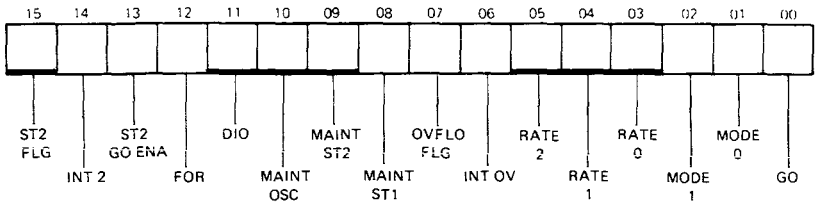


Figure 2 KWV11-C Control/Status Register

Table 2 KWV11-C Control/Status Register Bit Definitions

Bit	Name	Function	Set By/C leared By
0	GO	Read/Write — Setting this bit starts the counter at a rate determined by the rate bits 3-5.	The GO bit is set and cleared under program control. In modes 1, 2, and 3, this bit remains set until cleared by the program. In mode 0 this bit is cleared automatically when the counter overflows. Clearing bit 0 or a BUS INIT resets the counter and stops the counting.
1, 2	MODE	Read/Write **2 1 Mode** 0 0 Mode 0 0 1 Mode 1 1 0 Mode 2 1 1 Mode 3	The mode is set and cleared under program control and by BUS INIT. BUS INIT causes the board to go into mode 0.

Bit	Name	Function	Set By/C leared By
3-5	RATE	Read/Write — These bits select the clock rate or counting source for the counter. **5 4 3 Rate** 0 0 0 Stop 0 0 1 1 MHz 0 1 0 100 kHz 0 1 1 10 kHz 1 0 0 1 kHz 1 0 1 100 Hz 1 1 0 ST1 external input 1 1 1 Line (50/60 Hz)	The rate is set and cleared under program control and by BUS INIT.
6	INTOV (Interrupt on Overflow)	Read/Write — When this bit is set, the assertion of OVFLO FLAG generates an interrupt. Interrupt is also generated if bit 6 is set while OVFLO FLAG is set.	This bit is set and cleared under program control. If either bit 6 or 7 is cleared while an overflow interrupt request to the processor is pending, the request is cancelled.

Bit	Name	Function	Set By/C leared By
7	OVFLO FLAG	Read/Write to 0 — If bit 6 is set, setting bit 7 generates an interrupt. Bit 7 must be cleared after the interrupt has been serviced to enable further overflow interrupts. If two enabled interrupts are requested at the same time by bits 7 and 15, bit 7 has the higher priority.	This flag is set each time the counter overflows. It is cleared under program control, or at the low-to-high transition of the GO bit, or by BUS INIT.
8	MAINT ST1	Write Only — Setting this bit simulates the firing of ST1. All functions started by ST1 can be exercised under program control by using this bit.	This bit is set under program control. Clearing is not needed. It is always read as a 0.
9	MAINT ST2	Write Only — Setting this bit simulates the firing of Schmitt Trigger 2. All func-	This bit is set under program control. Clearing is not needed. It is always read as a 0.

Bit	Name	Function	Set By/C leared By
		tions started by ST2 can be exercised under program control by using this bit.	
10	MAINT OSC	Write Only — For maintenance purposes, setting this bit simulates one cycle of the internal crystal oscillator used to increment the clock counter. (Bit 11 must be set.)	This bit is set under program control. Clearing is not needed. It is always read as a 0.
11	DIO (Disable Internal Oscillator)	Read/Write — For maintenance purposes, this bit prevents the internal crystal oscillator from incrementing the clock counter. This bit is used with bit 10.	This bit is set and cleared under program control.
12	FOR (Flag Overrun)	Read/Write — Flag Overrun provides the programmer	This flag is set when an overflow occurs and the OVFLO

Bit	Name	Function	Set By/C leared By
		with an indication that the hardware is being asked to operate at a speed higher than is compatible with the software.	FLAG (bit 7) is still set from a previous occurrence, or when ST2 fires and the ST2 FLAG (bit 15) has been previously set. Bit 12 is cleared under program control, or at the low-to-high transition of the GO bit, or by BUS INIT.
13	ST2 GO ENABLE	Read/Write — When set, the assertion of ST2 FLAG sets the GO bit and clears the ST2 GO ENABLE bit.	The ST2 GO ENABLE bit is cleared under program control, or at the low-to-high transition of the GO bit, or by BUS INIT.
14	INT 2 (Interrupt on ST2)	Read/Write — When set, the assertion of ST2 FLAG (bit 15) causes an interrupt. If set while ST2 FLAG is set, an interrupt request is generated.	This bit is set and cleared under program control and by BUS INIT. When either bit 14 or 15 is cleared, any pending ST2 interrupt request is cancelled.
15	ST2 FLAG	Read/Write to 0 — Setting this flag	The ST2 FLAG is set by the firing of Schmitt Trig-

Bit	Name	Function	Set By/C leared By
		starts an interrupt request if bit 14 is set. Bit 15 must be cleared after servicing an ST2 interrupt to enable further interrupts. If two enabled interrupts are requested at the same time by bits 7 and 15, bit 7 has the higher priority.	ger 2 or the setting of the MAINT ST2 bit (in any mode) while the GO bit or the ST2 GO ENABLE bit is set. The ST2 FLAG is cleared under program control or at the low-to-high transition of the GO bit unless the ST2 GO ENABLE bit has previously been set. This bit is also cleared by BUS INIT.

Typical Program Sequences

This paragraph describes typical program sequences for operating the KWV11-C in each of the four modes of operation.

Single Interval (Mode 0)

This mode of operation is used to generate a fixed interval for such applications as known delays.

1. The program loads the BPR with the 2's complement of the number of clock pulses needed to generate the time delay at the user-selected clock rate. For example:

   Loading the BPR with – 100, at a clock frequency of 1 kHz, generates a 100 ms time delay.
2. The program loads the CSR with mode 0, the clock rate, and interrupt enable (INTOV) if needed.
3. The program sets the GO bit, or it sets the ST2 GO ENA bit and waits for an external event to set the GO bit.

4. When the GO bit is set, the counter is loaded with the contents of the BPR and starts counting. The counter increments until it overflows, at which time it clears the GO bit and stops counting.
5. The overflow causes the overflow flag (OVFLO) to be set in the CSR. If INTOV has been previously set, the OVFLO causes an interrupt to occur. If not, the KWV11-C waits for another program command.
6. The program either responds to the interrupt, or it responds as a result of checking the flags in the KWV11-C or in the A/D CSR. For example:

   The program can test the OVFLO flag in the CSR of the KWV11-C.

   If CLK OVL is used to start an A/D conversion, the program can check the A/D DONE flag in the A/D input board or allow the A/D DONE flag to generate an interrupt request.
7. The program reads the CSR, clears the OVFLO flag, and if no counting or mode changes are needed, sets the GO bit (or ST2 GO ENA bit) to start again at step 4 above.

Repeated Interval (Mode 1)

In this mode of operation, the user can generate a fixed frequency pulse train with any period within the range of the clock counter and the five crystal frequencies.

1. The program loads the BPR with the 2's complement of the number of clock pulses needed to generate the time delay at the user-selected clock rate. For example:

   Loading the BPR with -1 and selecting a 100 KHz clock rate generates a 1 MHz pulse train.

   In general, the overflow rate (pulse train) is equal to the clock rate divided by the absolute value that is loaded into the BPR.
2. The program loads the CSR with mode 1, the clock rate, and interrupt enable (INTOV) if needed.
3. The program sets the GO bit, or it sets the ST2 GO ENA bit and waits for an external event to set the GO bit.
4. When the GO bit is set, the counter is loaded with the contents of the BPR and starts counting. The counter increments until it overflows.

5. The overflow causes the counter to be loaded again with the count from the BPR and to start counting again. The overflow also sets the OVFLO flag in the CSR, which generates an interrupt if enabled.
6. If a second overflow occurs before the processor services the first overflow flag, then the flag overrun (FOR) bit is set in the CSR to inform the processor of a loss of data.
7. The program either responds to the interrupt, or it responds as a result of checking the flags in the KWV11-C CSR or in the A/D CSR. For example:

   The overflow (CLK OVL) can be used to start an A/D conversion in an A/D input board. When the A/D conversion is complete, A/D DONE in the A/D CSR can generate an interrupt request.
8. The program writes the KWV11-C CSR to clear the OVFLO flag, make necessary changes, and set the GO bit (or ST2 GO ENA bit). Then the program starts again at step 4 above.

External Event Timing (Mode 2)

In this mode of operation, the user can generate a pulse train while monitoring external events, can record the time of external events, or can count external events. Two external events can be monitored with respect to each other.

1. The program may load the BPR with the 2's complement of one of the following:

- The number of line inputs (BEVNT) that will generate a realtime reference to record the time of an external event at ST2.
- The number of clock pulses needed to generate the time delay at the user-selected clock frequency.
- The number of external events to be counted at ST1 before an overflow occurs.

2. The program loads the CSR with mode 2, the clock input (ST1, BEVNT, or one of five frequencies), and interrupt enable (INTOV or INT2) if needed.
3. The program sets the GO bit, or it sets the ST2 GO ENA bit and waits for an external event to set the GO bit.

4. When the GO bit is set, the counter is cleared and it starts counting at the selected clock rate or number of inputs at ST1.
5. An input at ST2 places the current contents of the counter in the BPR and sets the ST2 flag in the CSR. If INT2 has previously been set, an interrupt is generated to the processor. The program can then read the BPR and record the time of the event.
6. If ST2 does not occur, the counter continues to increment even after an overflow. The overflow sets the OVFLO flag and generates an inerrupt if INTOV is enabled.
7. The counter continues until the program clears the GO bit.

External Event Timing from Zero Base (Mode 3)
The program for this operation is the same as for mode 2, except the counter is automatically cleared after every ST2 pulse.

CONFIGURATION

The KWV11-C, shown in Figure 3, has two switch packs, SW1 and SW2, to set up its device address and interrupt vector address. It also has a switch pack, SW3, to select Schmitt trigger slope and level controls. For each of the two Schmitt triggers on the board, the user may select a fixed reference level for TTL logic or a variable reference level that permits setting the Schmitt trigger threshold to any point between −12 V and +12 V. The user may also select whether the Schmitt trigger fires on the positive or negative slope of the input waveform.

Two tabs on the board provide outputs from the clock counter (CLK OVL) and Schmitt trigger 1 (ST1 OUT). Either of these output tabs can be used to connect a short jumper wire to the A/D input board (pin RTC IN) to start an A/D conversion.

This paragraph provides details on setting up the KWV11-C.

Selecting the KWV11-C Device Address

The KWV11-C device address is the base I/O address assigned to the control/status register of the board. The device address is selected by means of two switch packs, SW1 and SW2. The switches allow the user to set the device address within the range of 170000_8 to 177774_8 in increments of 4_8. The device address is usually set at 170420_8, as shown in Figure 4. A switch in the ON position decodes a 1 in the corresponding bit position; a switch in the OFF position decodes a 0.

KWV11-C

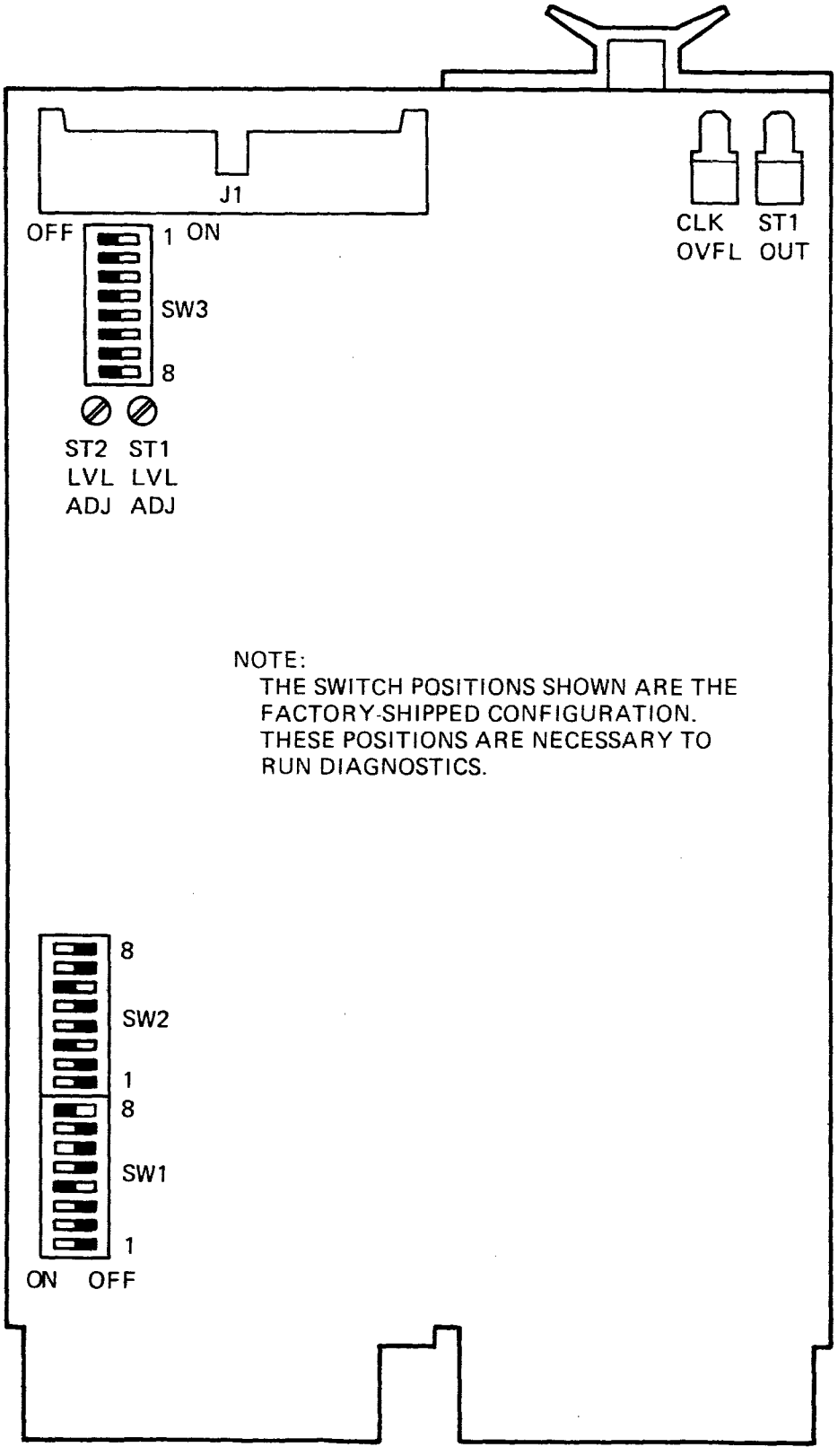


Figure 3 KWV11-C Physical Layout

Selecting the KWV11-C Interrupt Vector Address

The KWV11-C is capable of generating two interrupt vectors to the LSI-11 processor. These interrupts can occur when one of the following occurs:

- Clock counter overflows
- Schmit trigger 2 fires

The base interrupt vector is assigned to the clock overflow interrupt and can be assigned any address between 0 and 770_8 in increments of 10_8. It is usually set to 440_8 by SW2, as shown in Figure 5. A switch in the OFF position decodes a 0; a switch in the ON position decodes a 1.

The interrupt vector for ST2 is automatically 4 address locations higher than the selected base interrupt vector.

Selecting Schmitt Trigger Reference Levels and Slopes

The KWV11-C has two Schmitt triggers that condition the input waveforms to a form needed by the user. Both can be adjusted to trigger at any level in the ± 12 V range (or at TTL fixed levels) and on either the positive or negative slope of the input signal. Each Schmitt trigger has three switches and a potentiometer, shown in Figure 6. The use of these switches and potentiometers is given in Table 3.

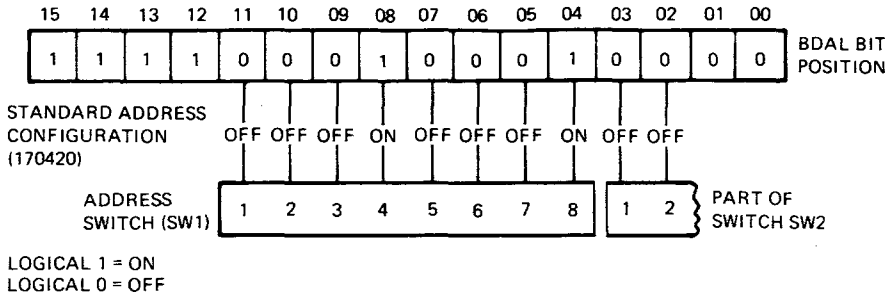


Figure 4 Selecting KWV11-C Device Address

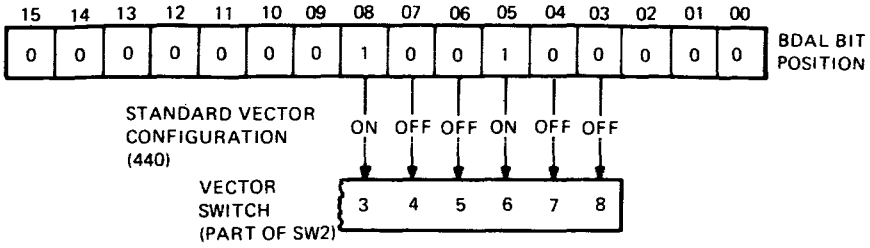


Figure 5 Selecting KWV11-C Interrupt Vector Address

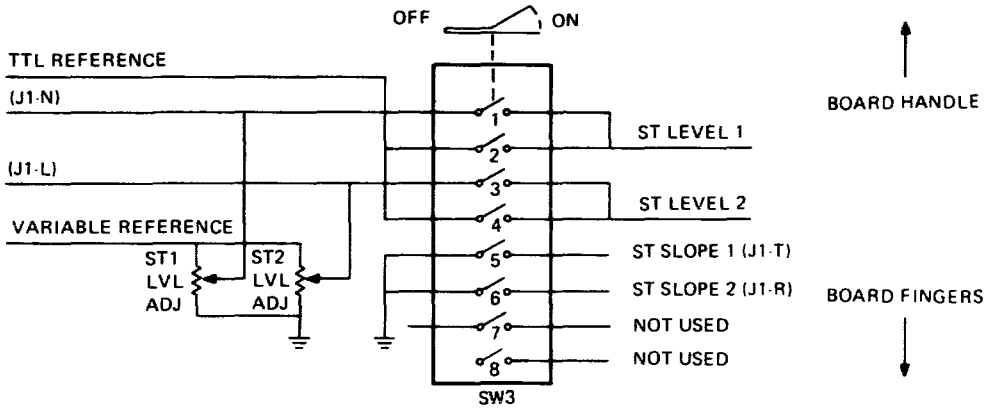


Figure 6 KWV11-C Slope and Reference-Level Switches

Table 3 Setting Schmitt Triggers on KWV11-C

SW3 Switch No.	Function
1	With this switch ON and switch 2 OFF, ST1 fires at a level determined by the ST1 LVL ADJ potentiometer within a range of ± 12 V.

NOTE

Switches 1 and 2 cannot be on together.

SW3 Switch No.	Function
2	With this switch ON and switch 1 OFF, ST1 fires at a fixed reference level for TTL logic. The potentiometer has no effect.
3	With this switch ON and switch 4 OFF, ST2 fires at a level determined by the ST2 LVL ADJ potentiometer within a range of ± 12 V.
	NOTE Switches 3 and 4 cannot be on together.
4	With this switch ON and switch 3 OFF, ST2 fires at a fixed reference level for TTL logic. The potentiometer has no effect.
5	When this switch is OFF, ST1 fires on the negative slope (high to low transition) of the input signal. When ON, ST1 fires on the positive slope (low to high transition).
6	When this switch is OFF, ST2 fires on the negative slope of the input signal. When ON, ST2 fires on the positive slope.
7,8	Not used.

Figure 7 shows the relationship of an analog input signal to the Schmitt trigger output. Note that once the Schmitt trigger fires, it fires again only after the input signal moves past the opposite threshold and then again passes the user-selected threshold.

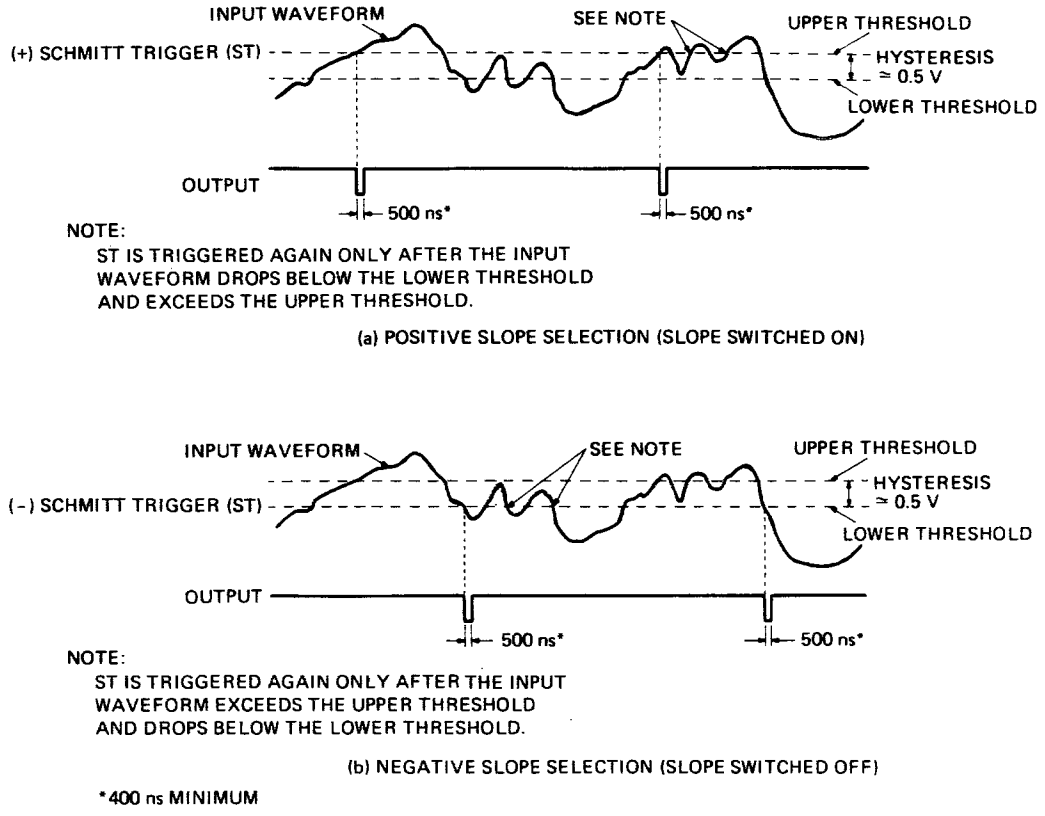
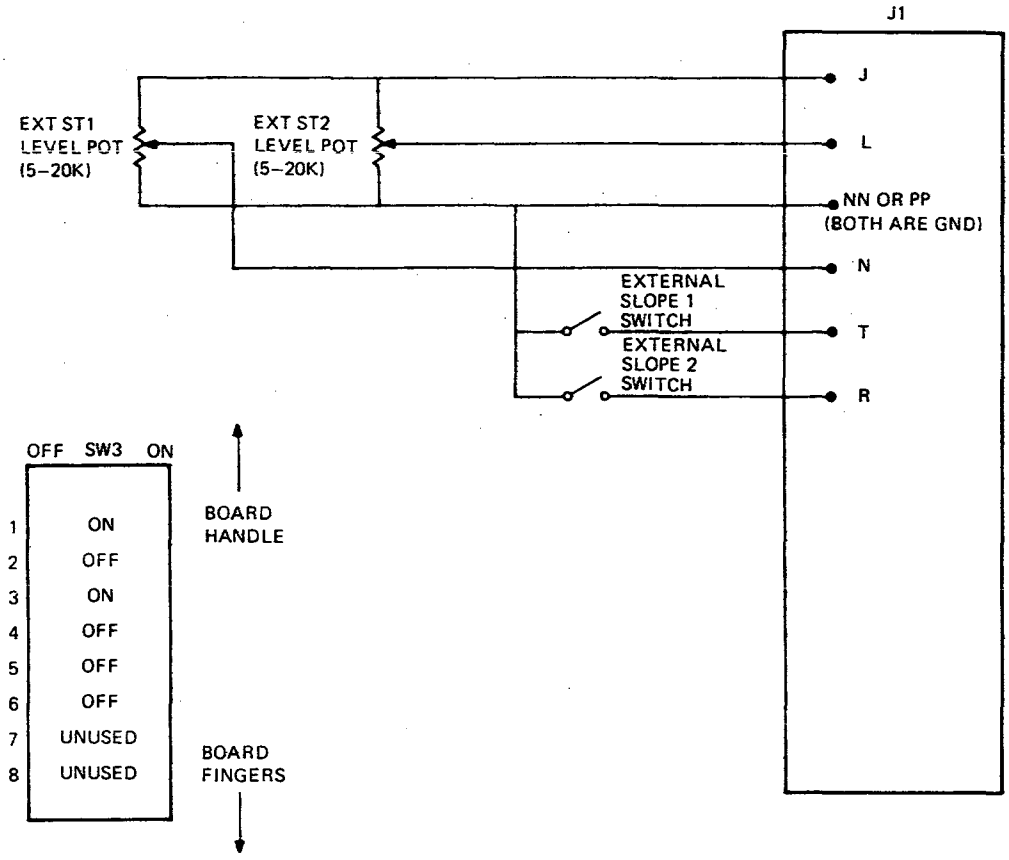


Figure 7 Input-to-Output Waveforms for Postive and Negative Slopes

External Control of Schmitt Triggers

The connector J1 on the board allows the user to connect external slope and level controls for each Schmitt trigger. Connect external potentiometers and switches as shown in Figure 8. The value of the potentiometers should be between 5 k Ω and 20 k Ω. Selecting a potentiometer with more turns provides for a finer adjustment over the ± 12 V range.

SW3 on the KWV11-C must be set as shown in Figure 8, and the potentiometers on the KWV11-C should be set to their center of rotation. At the center, the screwdriver, slot should be aligned with the notch at its edge.



NOTES:

1. FOR PROPER OPERATION OF EXTERNAL LEVEL CONTROLS, BOTH POTENTIOMETERS ON THE KWV11-C BOARD MUST BE SET TO APPROXIMATE CENTER OF ROTATION.
2. SW3 SWITCHES 1–4 MUST BE SET AS SHOWN; SWITCHES 5 AND 6 CAN BE EITHER OFF FOR NEGATIVE SLOPE TRIGGERING OR ON FOR POSITIVE SLOPE TRIGGERING.

Figure 8 Example Circuit for External Control of Schmitt Triggers

INTERFACING TO THE KWV11-C

Figure 9 shows the pin assignments of the 40-pin I/O connector J1 on the KWV11-C. This connector is provided for user inputs and outputs.

In addition, two tabs (shown in Figure 3) provide output signals CLK OVFL and ST1 OUT. These tabs are electrically in parallel with pins RR and UU of J1. These tabs make it easier for the user to connect an external start signal since an A/D conversion can be from Schmitt trigger 1 or from the clock counter overflow.

The KWV11-C has two bus interface connectors that plug into the LSI-11 bus. These connectors have signals defined by LSI-11 bus specifications.

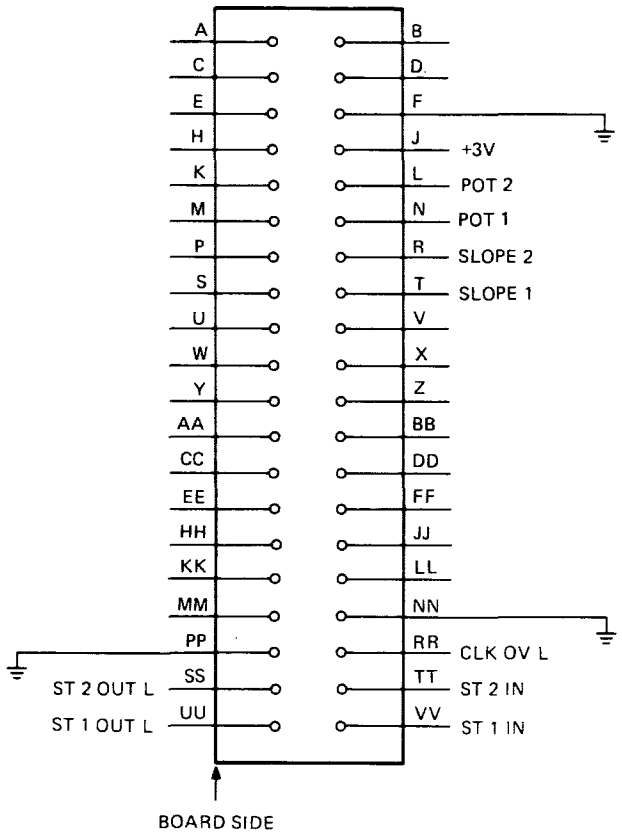


Figure 9 KWV11-C I/O Connector J1 Pin Assignments

LPV11 PRINTER OPTION

INTRODUCTION

The LPV11 printer option is a high-speed line printer system for use with an LSI-11 system. The system consists of an LPV11 interface module, an interface cable, and a line printer (either an LP05 or LA180). The LPV11 interface module functions that are used with an LP05 or LA180 line printer are similar; however, the printer strobe signals required for each printer are different. The specific interface cable allows the interface module to detect which printer it is interfacing to, and automatically supplies the correct timing signals for the specific type of printer. The interface module is program-controlled to transfer data from an LSI-11 bus to the line printer. There are 12 option numbers that define the type of printer and four primary power (line) voltages. Printer types include the LA180 DECprinter and two LP05 line printer models (uppercase letters only, and both uppercase and lowercase letters). These models and their interface cables are defined in Table 1.

Table 1 LPV11 Option Model Numbers

Option No. (Model)	Interface Cable*	Primary Power	Model	Printer Description
LPV11-PA	BC11S-25	115V, 60Hz	LA180-PA	180 char/sec printer, 132 column, upper- and lowercase letters
LPV11-PB	BC11S-25	230V, 60Hz	LA180-PB	
LPV11-PC	BC11S-25	115V, 50Hz	LA180-PC	
LPV11-PD	BC11S-25	230V, 50Hz	LA180-PD	
LPV11-VA	70-11212-25	115V, 60Hz	LP05-VA	300 line/min printer,132 column, uppercase letters only
LPV11-VB	70-11212-25	230V, 60Hz	LP05-VB	
LPV11-VC	70-11212-25	115V, 50Hz	LP05-VC	
LPV11-VD	70-11212-25	230V, 50Hz	LP05-VD	
LPV11-WA	70-11212-25	115V, 60Hz	LP05-WA	240 line/min printer, 132 column upper-and lower-case letters
LPV11-WB	70-11212-25	230V, 60Hz	LP05-WB	
LPV11-WC	70-11212-25	115V, 50Hz	LP05-WC	
LPV11-WD	70-11212-25	230V, 50Hz	LP05-WD	

* 7.62 m (25 ft) interface cable is supplied with each option.

LPV11

FEATURES

- Models available for 115 or 230 Vac operation at either 50 or 60Hz
- Line printers available with 132-column upper- and lowercase letters, or uppercase only
- Line printers available with speeds of 180 characters per second (LA180), or 300 or 240 lines per minute (LP05)
- Interface module and interface cable supplied.

SPECIFICATIONS

Module

Identification	M8027
Size	Double
Power	+5V ±5% at 0.8 A
Bus Loads	
AC	1.4
DC	1

Interface Cable

Type	BC11S-25 or 70-11212-25, depending on LPV11 model (see Table 1)
Length	7.62 m (25 ft) maximum

LP05 Line Printer

Power	115 Vac ±10% 50/60 Hz ±3 Hz or 230 Vac ±10% 50/60 Hz ±3 Hz 700 W
Printable Characters	
64-Character set	!"#$%&'()*+,->/0123456789:;<=>?@ ABCDEFGHIJKLMNOPQRS TUVWXYZ[\]↑_
96-Character set	All of the above plus a through z: ~
Type	Open Gothic print
Size	Typically 0.024 cm (0.095 in.) high; 0.065 cm (0.025 in.) wide

LPV11

Code Format	ASCII
Characters per line	132
Character drum speed	64-character drum: 1200 r/min 96-character drum: 800 r/min
Printer Characteristics	
Format	Top-of-form control; single line advance with automatic perforation step-over, and carriage return. Automatic vertical format control is optional.
Paper-Feed	One pair of pin-feed tractors for 1.27 cm (½ in) hole center, edge-punched paper.
Paper Slew Speed	50.8 cm (20 in) per second
Print Area	33.53 cm (13.2 in) wide, left justified
Character Spacing (horizontal)	0.254 ±0.0127 cm (0.1 ±0.005 in) between centers; maximum possible accumulative error for normal spacing is 0.0254 cm (0.-01 in) per 80- or 132-character line.
Line Spacing	0.424 ±0.025 cm (0.167 ±0.01 in) at 6 lines per inch; 0.3175 cm (0.125 in) at 8 lines per inch. Each character within ±0.254 cm (0.1 in) from mean line through character.
Line Advance Time	50 msec maximum
Character Synchronization	Variable reluctance pick-off senses drum position.
Physical Characteristics	
Height	1.14 m (45 in)
Width	0.81 m (32 in)
Depth	0.56 m (22 in)
Weight	150 kg (330 lb)

Ribbon Characteristics	
Type	Inked roll
Width	38.1 cm (15 in)
Length	18.288 m (20 yd)
Thickness	0.01 cm (0.004 in)
Paper Characteristics	
Type	Standard fanfold, edge punched, 27.94 cm (11 in) between folds
Width	10.16 cm to 42.55 cm (4 in to 16-3/4 in)
Weight	15-lb. bond minimum (single copy) 12-lb. bond with single-sheet carbon for up to six parts (multiple copy)
Environmental	
Operating Temperature	10° to 32° C (50° to 90° F)
Humidity	30 to 90% (no condensation)
Print Rates	
LP05-VA, -VB, -VC, -VD (64-character drum)	300 lines per minute
LP05-WA, -WB, -WC, -WD (96-character drum)	240 lines per minute

LA180 DECprinter

Power	90-132 Vac or 180-264 Vac 50 or 60 Hz ±1 Hz 400 W max (printing) 200 W max (idle)
Printable Characters	96 upper- and lowercase character set (7 × 7 dot matrix): +,-./0123456789 :;<=>?@ ABCDEFGHIJK LMNOPQRS TUVWXYZ [\]↑_abcdef ghijklmnopqr stuvwxyz {μ}~!"#$%&'()*

LPV11

Code Format	ASCII
Non-printable Characters	Six Commands: BEL, BS, LF, FF, CR, DEL
Number of Characters per Line	132 max
Type of Character Transfer	Parallel (7-bit plus parity)
Printer Characteristics	
Print Cycle Speed	Up to 180 characters per second
Line Printing Speeds	70 lines per minute on full line 300 lines per minute on short lines
Print Size	0.254 cm (10 characters per inch) horizontal 0.233 cm (6 lines per inch) vertical

DESCRIPTION

The M8027 interface module comprises functions that control the flow of data between the LSI-11 bus and the line printer (see Figure 1). The interface signals are different for the LP05 and the LA180 line printers, but the LPV11 detects a ground in the interface cable, and automatically configures itself for the proper printer. Each function of the interface is described in the following paragraphs. The LA180 and LP05 strobe timing diagrams are shown in Figures 2 and 3.

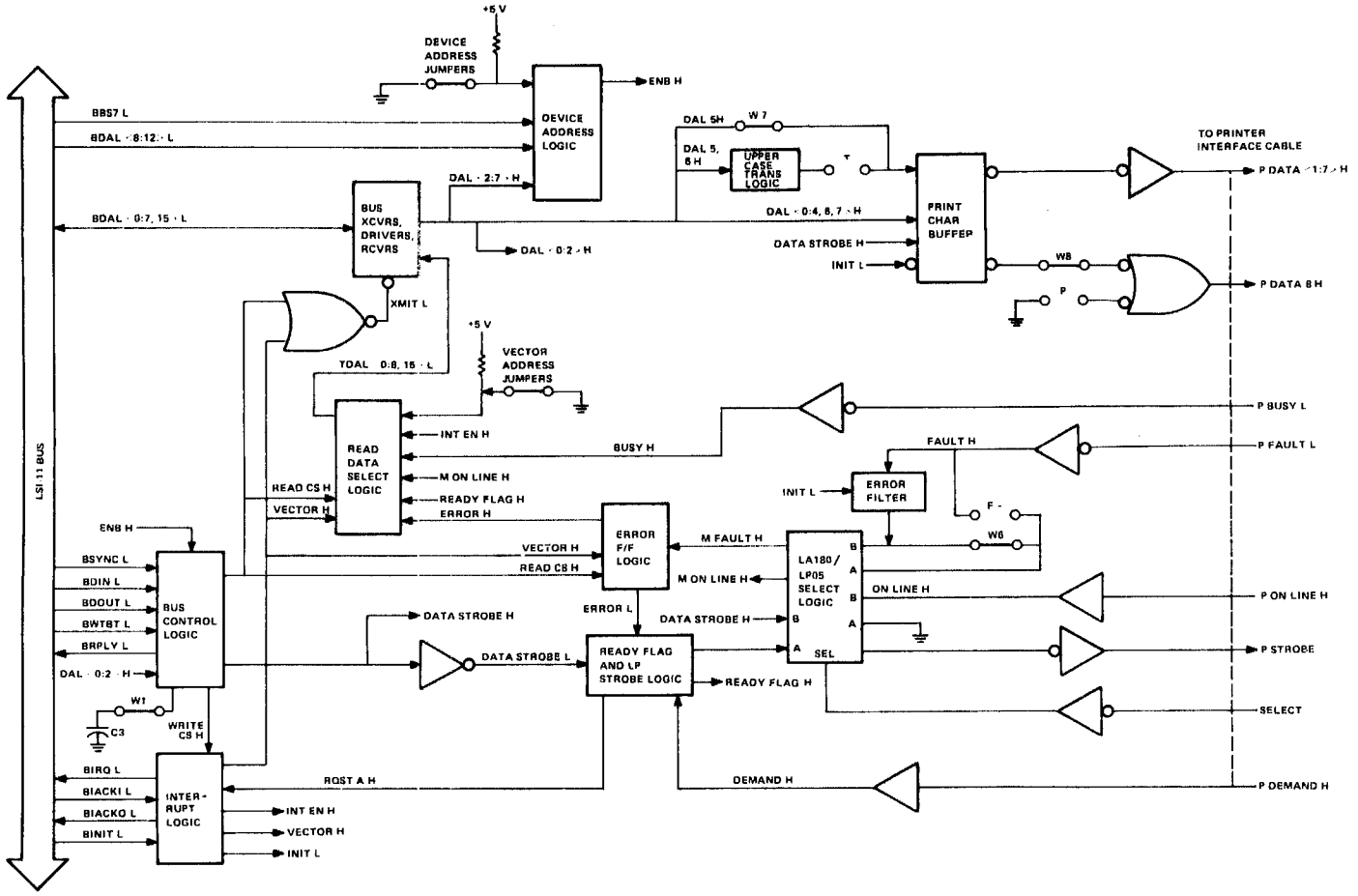
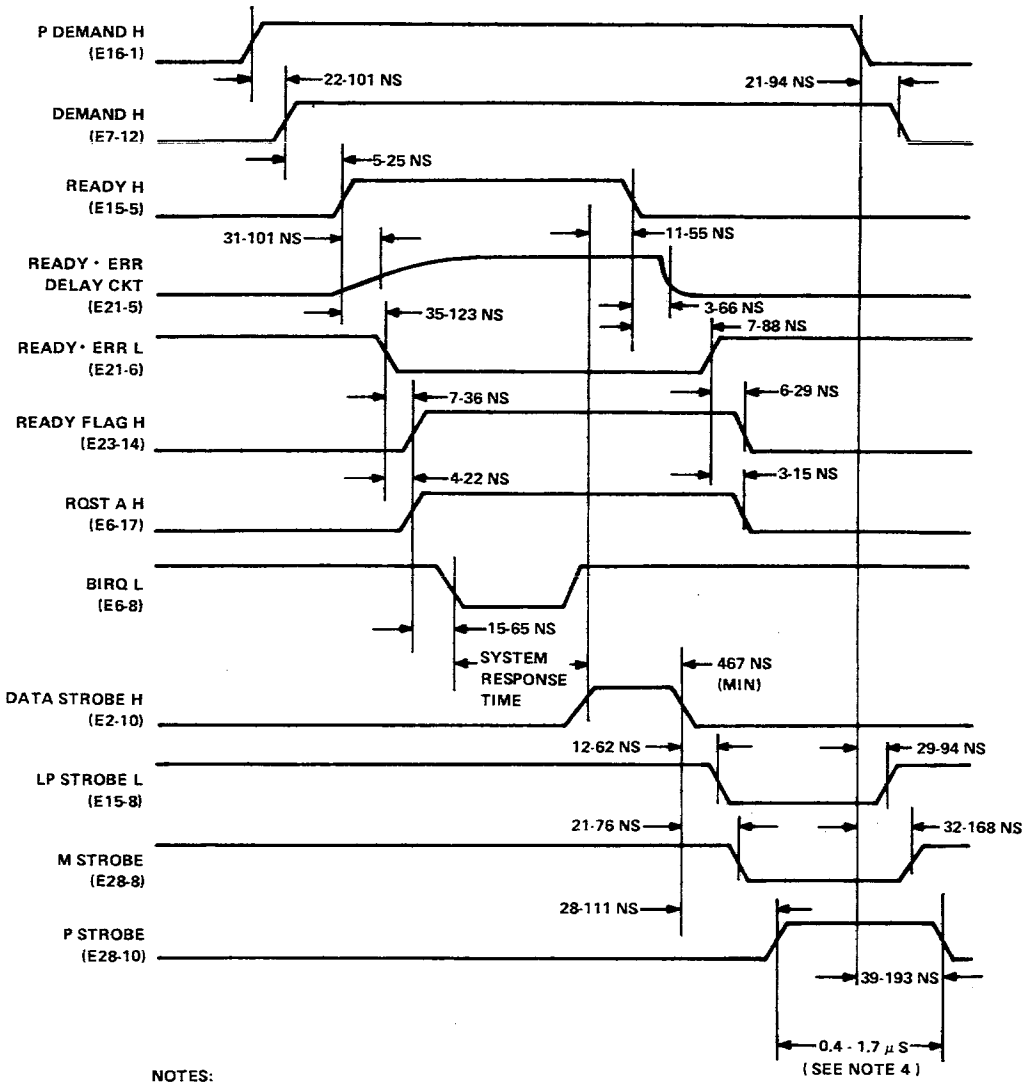


Figure 1 LPV11 Interface Logic Functions

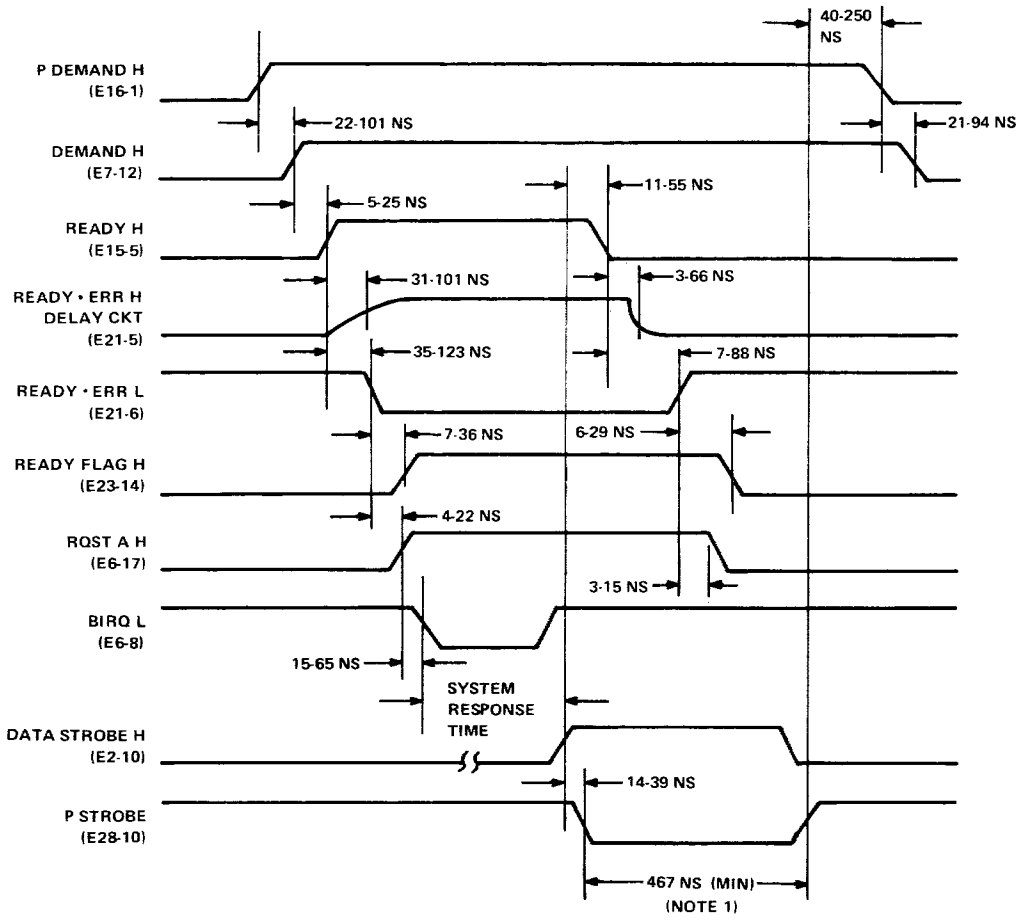


NOTES:

1. TIMING SHOWN IS TYPICAL, AND SHOWN FOR REFERENCE PURPOSES ONLY
2. TIMING SHOWN WITH JUMPER W1 INSTALLED
3. ( ) = INTEGRATED CIRCUIT PINS.
4. TIME IS DETERMINED BY LP05 PRINTER LOGIC.

11-5638

Figure 2 LP05 Internal Timing



NOTES:
1. JUMPER W1 INSTALLED (REQUIRED) FOR TIMING SHOWN.
2. TIMING IS TYPICAL, AND SHOWN FOR REFERENCE PURPOSES ONLY.
3. ( ) = INTEGRATED CIRCUIT PINS.

11-5637

Figure 3 LA180 Internal Timing

Bus Transceivers and Drivers

Bus transceivers (DEC 8641) receive the LSI-11 bus BDAL (0:7) L signals and distribute the bits on DAL (0:7) H lines. In addition, they transmit LPCS bits or interrupt vector address bits during a DATI bus cycle or interrupt sequence. Bus drivers (DEC 8881) transmit LPCS bits 8 and 15 during a DATI bus cycle in which the LPCS is addressed.

REV11-A, -C

REV11-A TERMINATOR, REV11-C DMA REFRESH, BOOTSTRAP

INTRODUCTION

The REV11-A DMA refresh, bootstrap/terminator module consists of DMA refresh circuits, a bootstrap ROM, and 120-ohm termination circuits. The REV11-C is similar to the REV11-A, but does not have the 120-ohm termination circuits.

FEATURES

- Dynamic MOS memory refresh
- ROM programs for booting paper tapes, RXV11 floppy disks, and RKV11 cartridge disks
- ROM diagnostics for CPU and memory
- 120-ohm LSI-11 bus terminations (REV11-A only)

SPECIFICATIONS

Identification	M9400-YA (REV11-A) M9400-YC (REV11-C)
Size	Double
Power	+5 V ±5% at 1.64 A (REV11-A) +5 V ±5% at 1.0 A (REV11-C)
Bus loads	
ac	2.2
dc	1

DESCRIPTION

Addressing – The module includes a 512 X 16-bit ROM array that is addressed in two 256-word segments. These address segments are reserved for REV11 options and reside in the upper 4K address bank, normally used for peripheral device addresses. The reserved addresses range from 165000–165776 and 173000–173776. A power-up mode, which will cause the processor to access ROM location 173000 upon power-up, is jumper-selectable on the processor module.

Initialization – The bootstrap ROM logic is initialized only when BDCOK H goes false. This condition occurs during a power failure and produces active BD INIT H and BD INIT L signals. These signals clear the 9-bit address latch and circuits contained in the DMA refresh logic. The option does not respond to the LSI-11 bus BINIT L signal.

Terminations (REV11-A Only)
Each bus signal line terminates with two resistors.
These termination resistors are generally contained in a 16-pin, dual-in-line package which is identical to an IC package. Each package contains 14 termination pairs. The values used are shown in the figure. Daisy-chained grant signals are terminated and jumpered. BIAKI L is jumpered (with etch) to BIAKO L, and BDMGI L is connected to BDMGO L via factory-installed jumper W1.

CONFIGURATION

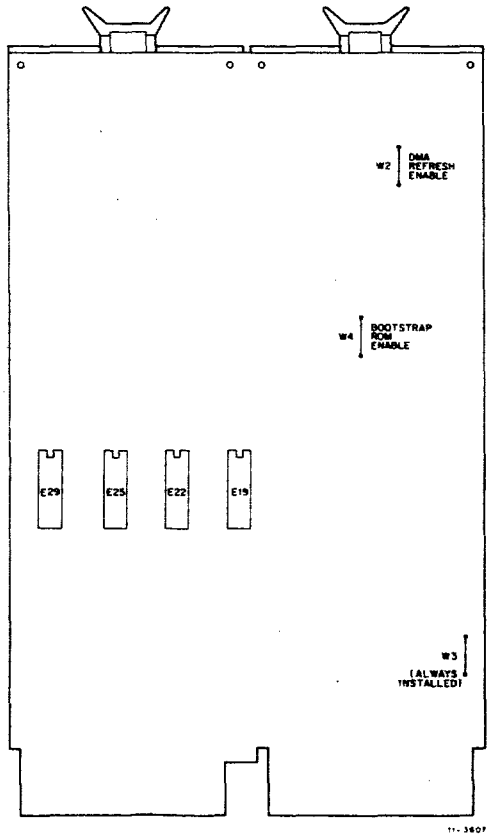


Figure 1 REV11-A, -C, Jumpers

W2	Insert to enable DMA refresh.
W4	Insert to enable bootstrap ROM.

RXV11 FLOPPY DISK OPTION

SPECIFICATIONS

Module	
Identification	M7946
Size	Double
Power	+5 V ±5% at 1.5 A
Bus Loads	
AC	1.8
DC	1
Drive	
Identification	RX01
Size	46.3 cm w × 28.7 cm h × 53.3 cmd (19 in w × 10.5 in h × 21 in d)
Recommmended Service Clearance (front and rear)	55 cm (22 in)
AC Power	4 A at 115 Vac; 2 A at 230 Vac (dual drive)
Cable Included	BC05L-15 (15 ft)
Drive Performance	
Capacity (8-bit bytes)	
Per diskette	262,144 bytes
Per track	3,328 bytes
Per sector	128 bytes
Data Transfer Rate	
Diskette to controller buffer	4 μsec/data bit (250K bits/sec)
Buffer to RXV11 interface	2 μsec/bit (500K bits/sec)
RXV11 interface to LSI-11 I/O bus	18 μsec/8-bit byte (<50K bytes/sec)
Track-to-track move	6 msec/track maximum
Head settle time	25 msec maximum
Rotational speed	360 rpm±2.5%; 166 msec/rev nominal

Recording surfaces per disk	1
Tracks per disk	77 (0-76) or ($0\text{-}114_8$)
Sectors per track	26 (1-26) or ($0\text{-}32_8$)
Sectors per disk	2002
Recording technique	Double frequency
Bit density	3200 bits/in at inner track
Track density	48 tracks/in
Average access	262 msec, computed as follows:

Seek	Settle	Rotate	Total

(77 tks/3) × 6 msec + 25 msec + (166 msec/2) = 262 msec

Environmental Characteristics

Temperature

RX01, operating	15° to 32° C (59° to 90° F) ambient; maximum temperature gradient = −6.7° C/hr (20° F/hr)
RX01, nonoperating	−35° to +60° C (−30° to +140° F)
Media, nonoperating	−35° to +52° C (−30° to +125° F)

NOTE

Media temperature must be within operating temperature range before use.

Relative Humidity

RX01, operating	25° C (77° F) maximum wet bulb 2° C (36° F) minimum dew point 20% to 80% relative humidity
RX01, nonoperating	5% to 98% relative humidity (no condensation)
Media, nonoperating	10% to 80% relative humidity
Magnetic field	Media exposed to a magnetic field strength of 50 oersteds or greater may lose data.

System Reliability	
Minimum number of revolutions/track	3 million/media (head-loaded)
Seek error rate	1 in 10^6 seeks
Soft read error rate	1 in 10^9 bits read
Hard read error rate	1 in 10^{12} bits read

NOTE

The above error rates apply only to media that are properly cared for. Seek error and soft read errors are usually attributable to random effects in the head/media interface, such as electrical noise, dirt, or dust. Both are called "soft" errors if the error is recoverable in ten additional tries or less. "Hard" errors cannot be recovered. Seek error retries should be preceded by an initialize.

CONFIGURATION

The factory jumper locations on the M7946 interface module are shown in Figure 1. Note that two styles of modules are used; one style (etch Rev B) has machine-inserted jumpers; the other (etch Rev C) has wire-wrap jumpers. All M7946 interface modules are configured and shipped with preselected register addresses and vectors as shown in Figure 2. The control/status register (RXCS) address is 177170, and the data buffer register (RXDB) address is 177172. The interrupt vector is 264_8. As supplied, the factory-configured jumpers are for the normal addresses used with DIGITAL software. However, in applications where more than one RXV11 system is required, appropriate register addresses and vectors may be configured by installing or removing jumpers. A second RXV11 system would normally be assigned register addresses 177174 (RXCS) and 177176 (RXDB), with an interrupt vector of 270_8 (Table 2).

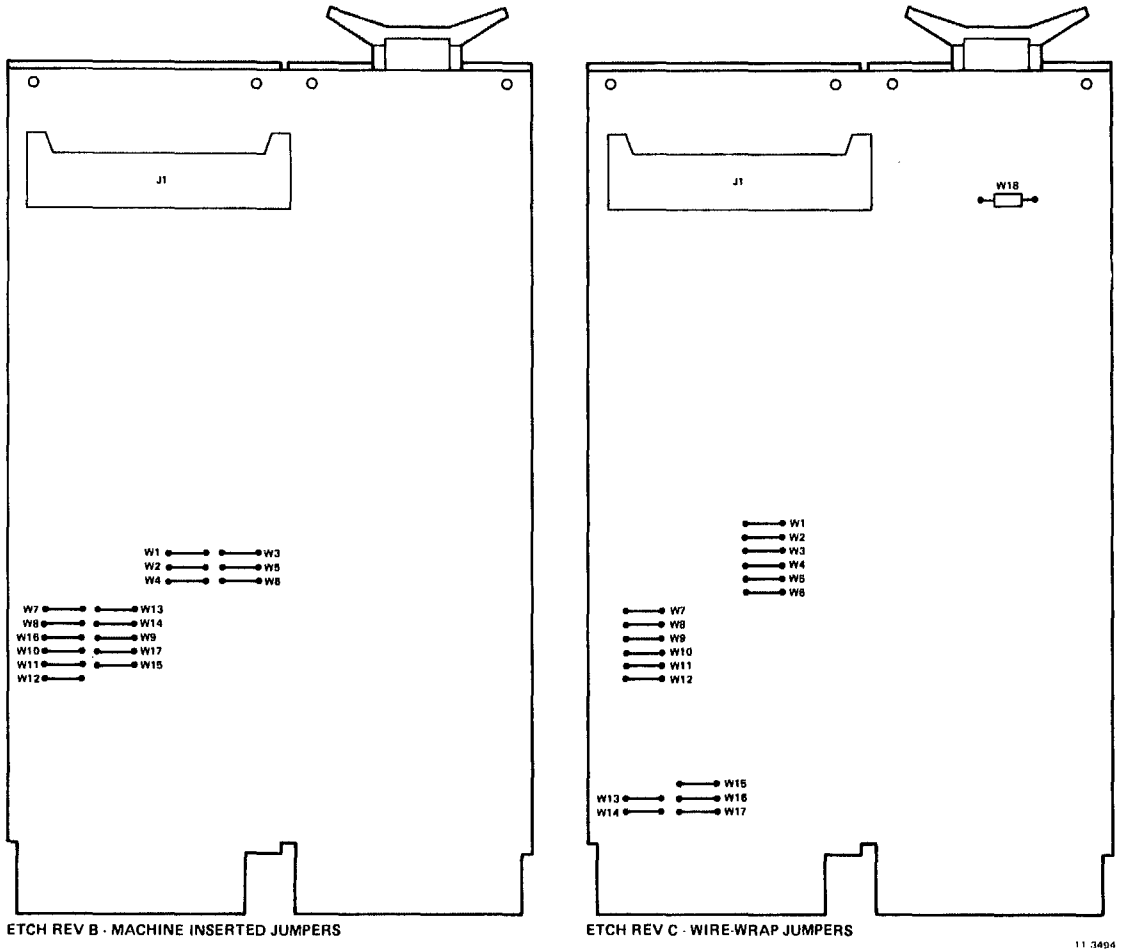


Figure 1 RXV11 Device Register and Interrupt Vector Jumper Locations

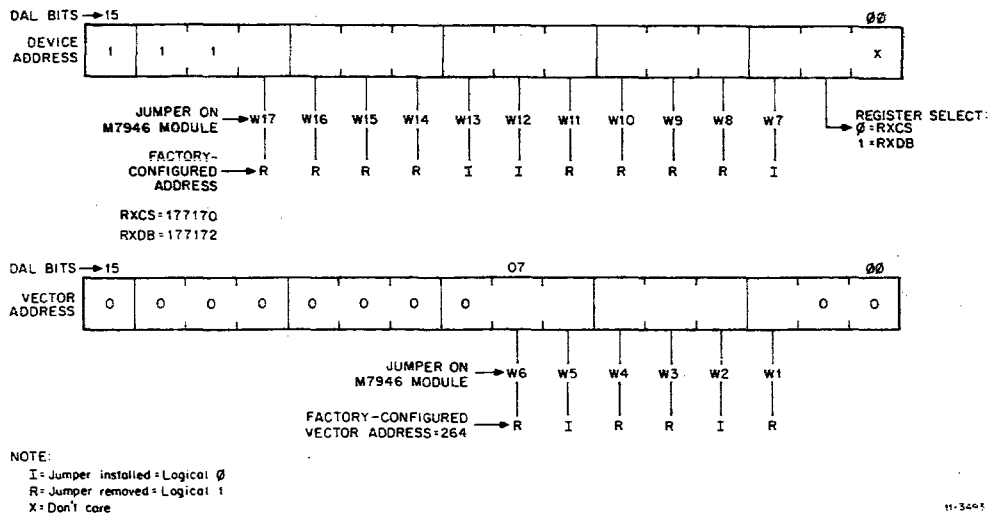


Figure 2 Device Register Address and Interrupt Vector

Table 1 RXV11 Configurations

System	Disk Drive	Line Voltage*
RXV11-AA	Single drive system	115V/60 Hz
RXV11-AC	Single drive system	115V/50 Hz
RXV11-AD	Single drive system	230V/50 Hz
RXV11-BA	Dual drive system	115V/60 Hz
RXV11-BC	Dual drive system	115V/50 Hz
RXV11-BD	Dual drive system	230V/50 Hz

* 50 Hz versions are available in voltages of 105, 115, 220, and 240 Vac by field-pluggable conversion.

Table 2 Standard Assignments

Description	Mnemonic	Read/ Write	First Module Address	Second Module Address
Registers				
Control/Status	RXCS	R/W	177170	177174
Data Buffer	RXDB	R/W	177172	177176
Interrupt				
Function Complete	Done	—	264	270

RXV21

RXV21 FLOPPY DISK OPTION

INTRODUCTION

The RXV21 floppy disk option is a random access mass memory device that stores data in fixed-length blocks on a preformatted, flexible diskette. Each diskette can store and retrieve up to 512K 8-bit bytes of data. The RXV21 system is rack-mountable and consists of an interface module, an interface cable, and either a single or dual RX02 floppy disk drive.

FEATURES

- Compact disk system
- Stores/retrieves 512K 8-bit bytes of data
- Rack mountable
- Available with either single or dual disk drive
- Available for 115 or 230 Vac, 50 or 60 Hz
- Can be converted (50 Hz version) for 105, 115, 220 or 240 Vac operation
- Direct Memory Access data tranfer
- Industry-compatible mode under software selection

SPECIFICATIONS

Module

Identification	M8029
Size	Double
Power	+5V ±5% at 1.8A typically
Bus Loads	
AC	3
DC	1

Drive

Identification	RX02
Size	46.3 cm w × 28.7 cm h × 53.3 cm d (19 in w × 10.5 in h × 21 in d)
Recommended Service Clearance (front and rear)	55 cm (22 in)

RXV21

AC Power	4A at 115 Vac; 2A at 230 Vac (dual drive)
Cable Included	BC05L-15 (15 ft)
Drive Performance	
Capacity (8-bit bytes)	
Per diskette	512,512 bytes
Per track	6,656 bytes
Per sector	256 bytes
Data Transfer Rate	
Diskette to controller buffer	2 μsec/data bit (500K bits/sec)
Buffer to RXV21 interface	1.2 μsec/bit (500K bits/sec)
RXV21 interface to LSI-11 I/O bus	23 μsec/16-bit word
Track-to-track move	6 msec/track maximum
Head settle time	25 msec maximum
Rotational speed	360 rpm ±2.5%; 166 msec/rev nominal
Recording surfaces per disk	1
Tracks per disk	77 (0-76) or ($0\text{-}114_8$)
Sectors per track	26 (1-26) or ($0\text{-}32_8$)
Sectors per disk	2002
Recording technique	Double frequency (FM) or modified (MFM)
Bit density	3200 bpi (FM); 6400 bpi (modified MFM)
Track density	48 tracks/in
Average access	262 msec, computed as follows:

Seek	Settle	Rotate	Total

(77 tks/3) × 6 msec + 25 msec + (166 msec/2) = 262 msec

RXV21

Environmental Characteristics	
Temperature	
RX02, operating	15° to 32° C (59° to 90° F) ambient; maximum temperature gradient = 11°C/hr (20°F/hr)
RX02, nonoperating	−35° to +60° C (−30° to +140° F)
Media, nonoperating	−35° to +52° C (−30° to +125° F)

NOTE

Media temperature must be within operating temperature range before use.

Relative Humidity	
RX02, operating	25° C (77° F) maximum wet bulb 2° C (36° F) minimum dew point 20% to 80% relative humidity
RX02, nonoperating	5% to 98% relative humidity (no condensation)
Media, nonoperating	10% to 80% relative humidity
Magnetic field	Media exposed to a magnetic field strength of 50 oersteds or greater may lose data.
System Reliability	
Minimum number of revolutions/track	3 million/media (head-loaded)
Seek error rate	1 in 10^6 seeks
Soft read error rate	1 in 10^9 bits read
Hard read error rate	1 in 10^{12} bits read

NOTE

The above error rates apply only to DIGITAL-approved media that is properly cared for. Seek error and soft read errors are usually attributable to random effects in the head/media interface, such as electrical noise, dirt, or dust. Both are called "soft"

errors in that the error is recoverable in ten additional tries or less. "Hard" errors cannot be recovered. Seek error retries should be preceded by an initialize.

DESCRIPTION

The interface module converts the RX02 I/O bus to the LSI-11 bus structure. It controls the RX02 interrupts to the processor, decodes device addresses for register selection, and handles the data interchange between the RX02 and the processor via DMA transfers. Power for the interface module is supplied by the LSI-11 bus.

The RXV21 floppy disk system is available in the configurations described in Table 1.

Table 1 RXV21 Configurations

System	Disk Drive	Line Voltage*
RXV21-AA	Single drive system	115V/60 Hz
RXV21-AC	Single drive system	115V/50 Hz
RXV21-AD	Single drive system	230V/50 Hz
RXV21-BA	Dual drive system	115V/60 Hz
RXV21-BC	Dual drive system	115V/50 Hz
RXV21-BD	Dual drive system	230V/50 Hz

* 50 Hz versions are available in voltages of 105, 115, 220, and 240 Vac by field-pluggable conversion.

CONFIGURATION

The factory jumper locations on the M8029 interface module are shown in Figure 1. All M8029 interface modules are configured and shipped with preselected register addresses and vectors as shown in Figure 2. The control/status register (RX2CS) address is 177170, and the data buffer register (RX2DB) address is 177172. The interrupt vector is 264_8. As supplied, the factory-configured jumpers are for the normal addresses used with DIGITAL software. However, in applications where more than one RXV21 system is required, appropriate register addresses and vectors may be configured by installing or removing jumpers. A second RXV21 system would normally be assigned register addresses 177200 (RX2CS) and 177202 (RX2DB), with an interrupt vector of 270_8 (Table 2).

Register Descriptions

Control/Status Register (RXCS)(177170) — The format for the RX2CS register is shown in Figure 3. Bit descriptions are presented in Table 3. Loading the RX2CS register while the RX01 is not busy and with bit 0 = 1 will initiate a function described in Table 3.

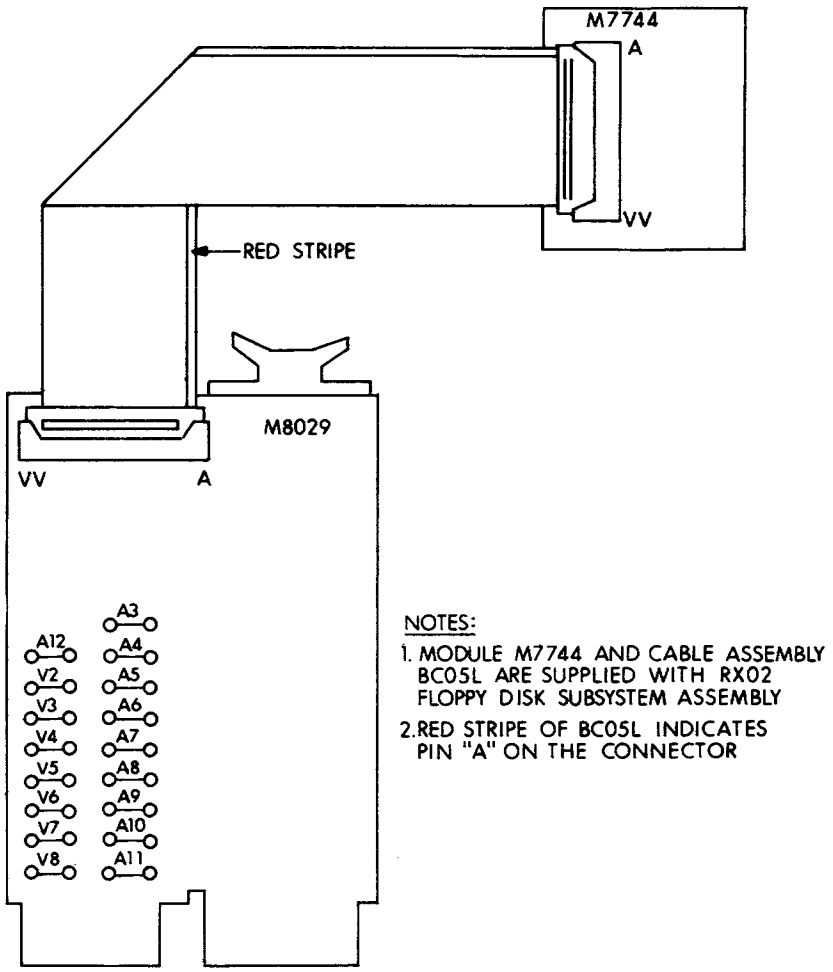


Figure 1 RXV21 Device Register and Interrupt Vector Jumper Locations

To select the standard address, the following jumpers are installed:

A12	Installed
A11	Installed
A10	Installed
A9	Installed
A8	Removed
A7	Removed
A6	Installed
A5	Installed
A4	Installed
A3	Installed

The standard Interrupt Vector is selected by installing the following jumpers:

V2	Installed
V3	Removed
V4	Installed
V5	Installed
V6	Removed
V7	Installed
V8	Removed

Figure 2 Device Register Address and Interrupt Vector

Table 2 Standard Assignments

Description	Mnemonic	Read/ Write	First Module Address	Second Module Address
Registers				
Control/ Status	RX2CS	See register description	177170	177150
Data Buffer	RX2DB		177172	177152
Interrupt				
Function Complete	Done	—	264	270

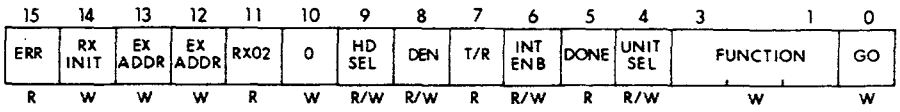


Figure 3 RXV21 Command and Status Register (RX2CS)

Table 3 RX2CS Bit Descriptions

Bit: 0 **Name:** GO
Function: Initiates a command to the RX02. Write-only.

Bit: 1-3 **Name:** Function Select
Function: These bits code one of the eight possible functions described in the Programming Specification. Write-only.

Bit: 4 **Name:** Unit Select
Function: This bit selects one of the two possible disks for execution of the desired function. This bit is readable only when DONE is set. At that time, it indicates the unit previously selected. At any other time it is not valid.

Bit: 5 **Name:** DONE
Function: Indicates the completion of a function. DONE will generate an interrupt upon being asserted if Interrupt Enable (RX2CS Bit 6) is set. Read-only.

Bit: 6 **Name:** Interrupt Enable
Function: This bit is set by the program to enable an interrupt when the RX02 has completed an operation (DONE). The condition of this bit is normally determined at the time a function is initiated. Cleared by initialize. Read/write.

Bit: 7 **Name:** Transfer Request
Function: This bit signifies that the RXV21 needs the next word in the register protocol sequence (see Programming Specification). Read-only.

Bit: 8 **Name:** Density
Function: This bit determines the density of the function to be executed. This bit is readable only when DONE is set. At that time, it indicates the density of the function previously executed. This bit is not valid at any other time.

Table 3 RX2CS Bit Descriptions (Cont)

Bit: 9 **Name:** Head Select
Function: This bit selects one of two heads for double-sided operation. This bit is readable only when DONE is set. At that time, it indicates the side that was previously selected. At any other time, it is not valid.

Bit: 10 **Name:**
Function: Reserved. Note: Must be written 0.

Bit: 11 **Name:** RX02
Function: This bit is set by the interface to inform the programmer that this is an RX02 system. Read-only.

Bit: 12-13 **Name:** Extended Address
Function: These bits are used to declare an extended bus address. Write-only.

Bit: 14 **Name:** RXV21 Initialize
Function: This bit is set by the program to initialize the RXV21 without initializing all of the devices on the UNIBUS.

CAUTION: Loading the lower byte of the RX2CS will also load the upper byte of the RX2CS. Upon setting this bit in the RX2CS, the RXV21 will drop DONE and move the head position mechanism of both drives (if two are available) to track zero. Upon completion of a successful initialize, the RX02 will zero error and status and set DONE. It will also read sector one of track one on drive 0. At termination, drive 0 head is at track one.

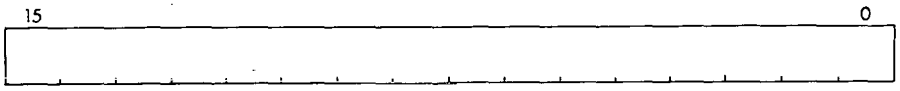
Bit: 15 **Name:** ERROR
Function: This bit is set by the RX02 to indicate that an error has occurred during an attempt to execute a command. Cleared by the initiation of a new command. Read-only.

RXV21 Data Buffer Register (RX2DB)
This register serves as a general purpose data path between the RX02 and the RXV21. It may represent one of six RX02 registers according to the protocol in progress. (See Programming Specification.) This register is read/write if the RX02 is not in the process of executing a command; it may be manipulated without affecting the RX02.

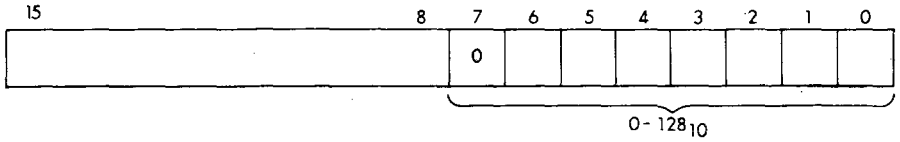
Caution

Violation of protocol in manipulation of this register may cause permanent data loss.

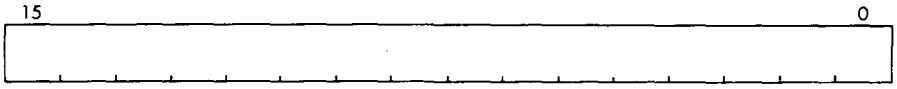
RX2DB—RXV21 Data Buffer Register



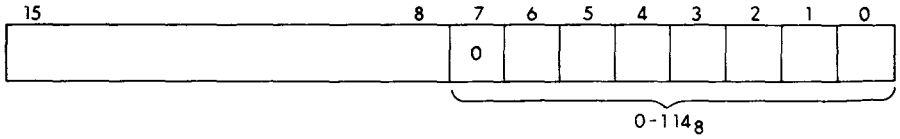
RX2WC—RXV21 Word Count Register — For a double-density sector the maximum word count is 128_{10}. For a single-density sector the maximum word count is 64_{10}. If a word count is beyond the limit for the density indicated, the control asserts Word Count Overflow (Bit 10 of RX2ES). Write-only register. The actual word count and *not* the 2's complement of the word count is loaded into the register.



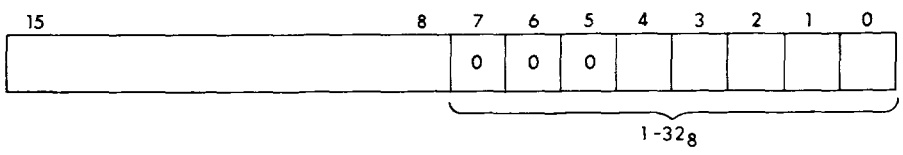
RX2BA—RXV21 Bus Address Register — This register specifies the bus address of data transferred during Fill Buffer, Empty Buffer, and Read Definitive Error operations. Incrementation takes place after a memory transaction has occurred. The RX2BA, therefore, is loaded with the address of the first data word to be transferred. This is a 16-bit write-only register (See Programming).



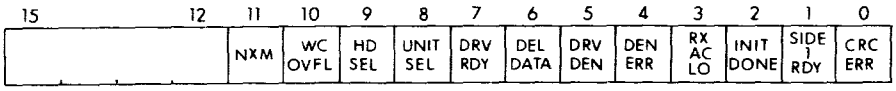
RX2CA—RXV21 Track Address Register — This is a write-only register which is loaded to indicate on which of the 77_{10} tracks a given function is to operate. It is addressed only under the protocol of the function in progress.



RX2SA—RXV21 Sector Address Register — This is a write-only register which is loaded to indicate on which of the 26_{10} sectors a given function is to operate. It can be addressed only under the protocol of the function in progress.



RX2ES—RXV21 Error and Status Register — The RX2ES is a read-only register available at the termination (DONE) of each function. The Drive Ready bit is only updated during an Initialize or Read Status function. At the termination of any other function, it reflects the drive status of the last Read Status or Initialize command.



Bit: 0 **Name:** CRC Error
Function: The cyclic redundancy check at the end of the data field has indicated an error. The data collected must be considered invalid. It is suggested that the data transfer be re-tried up to 10 times, as most data errors are recoverable (soft).

Bit: 1 **Name:** Side 1 Ready
Function: This bit, when set, indicates that a double-sided diskette is mounted in a double-sided drive and is ready to execute a function. This bit is only valid at the termination of an Initialize sequence or a Maintenance Read Status command.

Bit: 2 **Name:** Initialize Done
Function: Indicates completion of the initialize routine. Can be asserted due to: a) a RX02 power failure, B) system power failure, C) programmable or bus initialize.

Bit: 3 **Name:** RX AC LO
Function: RX power failure. Bit is set when the subsystem power is gone.

Bit: 4 **Name:** Density Error
Function: Indicates that the density of the function in progress does not match the Drive Density. Upon detection of this error, the control terminates the operation and asserts Error and Done.

Bit: 5 **Name:** Drive Density
Function: Indicates the density of the diskette mounted in the drive indicated by the Unit Select bit.

Bit: 6 **Name:** Deleted Data
Function: In the course of recovering data, the "deleted data" address mark was detected at the begining of the data field. The Drv Den bit(s) indicate whether the mark was an address mark. The data fol-

lowing the mark will be collected and transferred normally, as the deleted data mark has no further significance other than to establish drive density. Any alteration of files or actual deletion of data, due to this mark, must be accomplished by user software.

Bit: 7 **Name:** Drive Ready
Function: The selected drive is ready if Bit 7 = 1. All conditions for disk operation are satisfied, such as door closed, power OK, diskette up to speed, etc. The RX02 may be presumed to be ready to perform any operation. This bit is only valid when retrieved with a Read Status function or initialize.

Bit: 8 **Name:** Unit Select
Function: This bit indicates the drive on which the previous command was executed. This bit should agree with bit 4 of the RX2CSR for commands which require drive operation.

Bit: 9 **Name:**
Function: Reserved

Bit: 10 **Name:** Word Count Overflow
Function: The Word Count Register resides in the control. If the control senses that the word count is beyond sector size it will terminate the Fill or Empty Buffer operation and set Error and,Done.

Bit: 11 **Name:** Nonexistent Memory Error
Function: This bit is set when a DMA transfer is being performed and the memory address specified in RX2BA is nonexistent (does not respond to MSYN within 10 μsec).

PROGRAMMING

Data storage and recovery on the RXV21 occurs with careful manipulation of the two RXV21 registers (RX2CS, RX2DB) following the strict protocol of the individual function. Data may be permanently lost if the protocol is not followed. New functions given before the completion of a previous function are ignored.

Function Codes

The following is a detailed description of the programming protocol associated with each function encoded and written into bits 1-3 of RX2CS if DONE is set.

Function	Description
000	Fill Buffer

This function is used to fill the RX02 data buffer with the number of words of data specified by the RX2WC register. "Fill Buffer" is a complete function in itself. The function ends when RX2WC overflows and, if necessary, the control has zero-filled the remainder of the buffer. The contents of the buffer may be written on the disk, by means of a subsequent Write Sector command, or returned to the host processor by an "Empty Buffer" command. To initiate this function, the RX2CS is loaded with the function. Bit 4 of the RX2CS (Unit Select) does not affect this function, since no disk operation is involved. Bit 8 (Density) must be properly selected since this determines the Word Count limit. When the command has been loaded, the DONE bit (RX2CS Bit 5) goes false. When the TR bit is asserted, the RX2WC may be loaded into the data buffer register. When TR is again asserted, the RX2BA may be loaded into the RX2DB. The data words are transferred directly from memory and DONE goes true, ending the operation, when RX2WC overflows and the control has zero-filled the remainder of the sector buffer, if necessary. If bit 6 RX2CS (Interrrupt Enable) is set, an interrupt is initiated. Any read on the RX2DB during the data transfer is ignored by the RXV21. After DONE is true, the RX2ES is located in the RX2DB register.

001 Empty Buffer

This function is used to empty the contents of the internal buffer through the RXV21 for use by the host processor. This data is in the buffer as the result of a previous "Fill Buffer" or "Read Sector" command.

The programming protocol for this function is identical to that for the "Fill Buffer" command. The RX2CS

is loaded with the command to initiate the function. This function will ignore bit 4 RX2CS (Unit Select). RX2CS bit 8 (Density) must be selected to allow the proper word count limit. When the command has been loaded, the DONE bit (RX2CS bit 5) goes false. When the TR bit is asserted, the RX2WC may be loaded into the RX2DB. When TR is again asserted, the RX2BA may be loaded into the RX2DB. The RXV21 assembles one word of data at a time and transfers it directly to memory. Transfers occur until Word Count overflow, at which time the operation is complete and DONE goes true. If bit 6 RX2CS (Interrupt Enable) is set, an interrupt is initiated. After DONE is true the RX2ES is located in the data buffer register.

010 Write Sector

This function is used to locate a desired sector on the diskette and fill it with the contents of the internal buffer. The initiation of the function clears RX2ES, TR, and DONE.

A. When TR is asserted, the program must load the desired Sector Address into RX2DB, which will drop TR.

   TR will remain unasserted while the RX02 attempts to locate the desired sector. The diskette density is determined at this time and is compared to the function density. If the densities do not agree, the operation is terminated; bit 4 RX2ES is set, RX2ES is moved to the RX2DB, Error (bit 15 RX2CS) is set, DONE is asserted, and an interrupt is initiated if bit 6 RX2CS (Interrupt Enable) is set.

   If the densities agree but the RX02 is unable to locate the desired sector within two diskette revolutions, the RXV21 will abort the operation, move the contents of RX2ES to the RX2DB, set ERROR (bit 15 RX2CS), assert DONE, and initiate an interrupt if Bit 6 RX2CS (Interrupt Enable) is set.

B. If the desired sector has been reached and the densities agree, the RXV21 will write the 128_{10} or 64_{10} words stored in the internal buffer followed by a CRC character which is automatically calculated by the RX02. The RXV21 ends the function by asserting DONE and if bit 6 RX2CS (Interrupt Enable) is set, initiating an interrupt.

CAUTION:

The contents of the sector buffer are not valid data after a power loss has been detected by the RX02. "Write Sector" however, will be accepted as a valid instruction and the (random) contents of the buffer will be written, followed by a valid CRC.

NOTE:

The contents of the sector buffer are not destroyed during a write sector operation.

011 Read Sector

This function is used to locate the desired sector and transfer the contents of the data field to the internal buffer in the control. This function may also be used to rapidly retrieve (5 ms) the current status of the drive selected. The initiation of this function clears RX2ES, TR, and DONE.

A. When TR is asserted, the program must load the desired Sector Address into the RX2DB, which will drop TR. When TR is again asserted, the program must load the desired Cynlinder Address into the RX2DB, which will drop TR.

   TR and DONE will remain unasserted while the RX02 attempts to locate the desired sector. If the RX02 is unable to locate the desired sector within two diskette revolutions for any reason, the RXV21 will abort the operation, set DONE and ERROR (Bit 15 RX2CS), move the contents of the RX2ES to the RX2DB, and if Bit 6 RX2CS (Interrupt Enable) is set, initiate an interrupt.

B. If the desired sector is successfully located, the control reads the data address mark and determines the density of the diskette. If the diskette (drive) density does not agree with the function

density, the operation is terminated and DONE and ERROR (bit 15 RX2CS) are asserted. Bit 4 RX2ES is set (Density Error) and the RX2ES is moved to the RX2DB. If Bit 6 RX2CS (Interrupt Enable) is set, an interrupt is initiated.

D. If the desired sector is successfully located, the densities agree, and the data are transferred with no CRC error, DONE will be set and if Bit 6 RX2CS (Interrupt Enable) is set, the RXV21 initiates an interrupt.

100 Set Media Density

This function causes the entire diskette to be reassigned to a new density. Bit 8 RX2CS (Density) indicates the new density. The control reformats the diskette by writing new data address marks (double or single density) and zeroing out all of the data fields on the diskette.

The function is initiated by loading the RX2CS with the command. Initiation of the function clears RX2ES and DONE. When TR is set, an ASCII "I" (111) must be loaded into the RX2DB to complete the protocol. This extra character is a safeguard against an error in loading the command. When the control recognizes this character it begins executing the command.

The control starts at Sector 1, Track 0 and reads the header information, then starts a write operation. If the header information is damaged, the control will abort the operation.

If the operation is successfully completed, DONE is set and if Bit 6 RX2CS (Interrupt Enable) is set, an interrupt is initiated.

NOTE:

If double-sided media is mounted in a double-sided drive, both sides are set to the same density automatically.

CAUTION:

This operation takes about 15 seconds and should not be interrupted. If for any reason the operation is interrupted, an illegal diskette has been generated which may have data marks of both densities. This diskette should again be completely reformatted.

101 Maintenance Read Status

This function is initiated by loading the RX2CS with the command. DONE is cleared. The Drive Ready bit (Bit 7 RX2ES) is updated by counting index pulses in the control. The Drive Density is updated by loading the head of the selected drive and reading the first data mark. All other RX2ES bits reflect the conditions created by the last command. During this function, in addition to status, the control performs the wraparound mode in the device electronics. If an error occurs while wrapping the data from the Sector Buffer through the device electronics, the Error bit (Bit 15 RX2CS) is set. The RX2ES is moved into the RX2DB. The RX2CS may be sampled when DONE (Bit 5 RX2CS) is again asserted and if Bit RX2CS (Interrupt Enable) is set, an interrupt will occur. This operation requires approximately 250 msec to complete.

NOTE:

If double-sided media is mounted in a double-sided drive, the Side 1 Ready bit (RX2ES bit 1) is set.

110 Write Sector With Deleted Data

This operation is identical to function 011 (Write Sector) with the exception that a deleted data address mark is written preceding the data rather than the standard data address mark. The Density bit associated with the function indicates whether a single or double density deleted data address mark will be written.

111 Read Error Code

The Read Error Code function implies a read extended status. In addition to the specific Error code, a dump of the control's internal scratch pad registers

also occurs. This is the only way that the Word Count Register can be retrieved. This function is used to retrieve specific information as well as drive status information, depending on detection of the general ERROR BIT.

The transfer of the registers is a DMA transfer. The function is initiated by loading the RX2CS with the command. DONE goes false. When TR is true, the RX2BA may be loaded into the RX2DB and TR goes false. The registers are assembled one word at a time and transferred directly to memory.

Following is the Register Protocol.

NOTE:

The Density bit (bit 8 RX2CS) must be loaded with the function. If the wrong assumption was made, an error is returned.

Following is the Register Protocol.

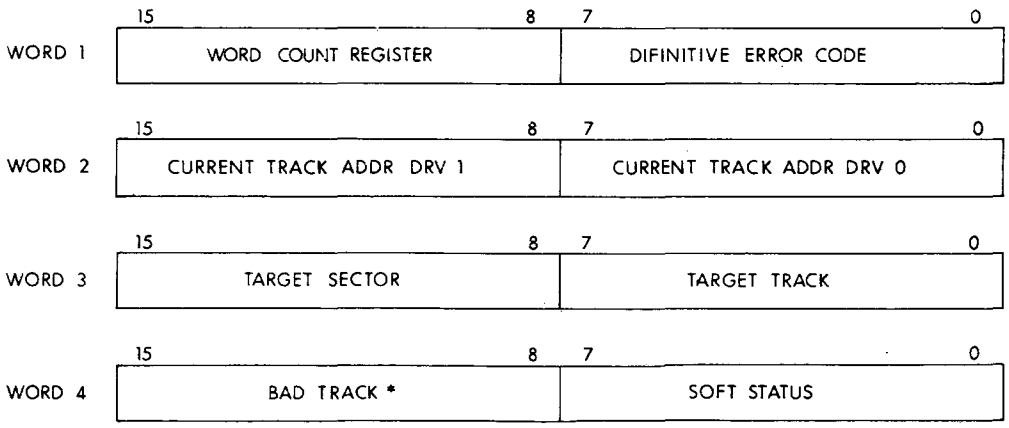


Table 4 Definitive Error Codes

10	DRIVE 0 FAILED TO SEE HOME ON INITIALIZE
20	DRIVE 1 FAILED TO SEE HOME ON INITIALIZE
40	TRIED TO ACCESS A TRACK GREATER THAN 76
50	HOME WAS FOUND BEFORE DESIRED TRACK WAS REACHED

Table 4 Definitive Error Codes (Cont)

70	DESIRED SECTOR COULD NOT BE FOUND AFTER 52 TRIES
110	MORE THAN 40 MICROSECONDS AND NO SEP CLOCK SEEN
120	A PREAMBLE COULD NOT BE FOUND
130	A PREAMBLE FOUND BUT NO ID MARK FOUND WITHIN ALLOWABLE TIME
150	THE TRACK ADDRESS OF A GOOD HEADER DOES NOT COMPARE WITH DESIRED TRACK
160	TOO MANY TRIES FOR IDAM
170	DATA ARE NOT FOUND IN ALLOTTED TIME
200	CRC ON READING THE SECTOR FROM THE DISK
220	FAILED MAINTENANCE WRAPAROUND CHECK
230	WORD COUNT OVERFLOW
240	DENSITY ERROR
250	INCORRECT KEY WORD ON SET DENSITY COMMAND

RX02 Power Fail or Initialize

When the RX02 control senses a loss of power within the RX02, it will unload the head and abort all controller action. The RXAC L line is asserted to indicate to the RXV21 that subsystem power is gone. The RXV21 asserts DONE and ERROR and sets the RXAC L bit in the RX2ES.

When the RX02 senses the return of power, it will remove DONE and begin a sequence to:

1. Move each drive head position mechanism to track 00
2. Clear any active error bits
3. Read sector 1 of track 1, on drive 0
4. Assert Initialize DONE in the RXES

Upon completion of the power-up sequence, DONE is again asserted. There is no guarantee that information being written at the time of a power failure will be retrievable; however, all other information on the diskette will remain unaltered.

LSI-11 Bus Power Fail

When the BPOK H line is negated by the LSI-11, the RXV21 asserts the Initialize line and holds it asserted. The RX02 control unloads the head and aborts controller action as detailed above. When LSI-11 power is restored, the above power-up sequence is started.

* This is the only valid bit in the RX2ES at this time.

Programming Examples for Typical Operation

Disk Write

A typical disk write sequence, which is initiated by the user program, would occur in two steps.

Fill Buffer—A command to fill the buffer is moved into the RX2CS. The GO bit must be set. The program tests for TR. When TR is detected, the program moves the desired word count into the RX2DB. TR goes false while the word count is moved to the RX02. The program retests TR and moves the Bus Address into the RX2DB. The device now requests bus mastership and DMA's one data word at a time into the RX2DB and shifts it across the RX02 data bus bit serially one 8-bit byte at a time into the sector buffer. When the Word Count Register overflows and, if necessary, the RX02 control zero fills the remainder of the sector buffer, the DONE bit is set and an interrupt will occur if the program has enabled interrupts.

Write Sector—A command to write the contents of the sector buffer onto the disk is moved into the RX2CS. The program tests TR and when TR is set, moves the desired sector address to the RX2DB. TR remains false while the sector address is shifted to the RX02 control. The control retests TR and when it is again set, moves the desired track address register to the RX2DB. Again TR is negated. The RX02 locates the desired track and sector and compares the diskette density against the assigned function density and writes the contents of the sector buffer onto the disk if the densities agree. When the write operation is completed, the DONE bit is set and an interrupt will occur if the program has enabled interrupts.

Disk Read

A typical disk read operation occurs in the reverse order. First, the desired track and sector are located and the contents of the sector are read into the sector buffer (Read Sector). Then, the contents of the sector buffer are unloaded into memory (Empty Buffer). In either case, the contents of the sector buffer are not valid if either a Power Fail or Initialize follows a Fill Buffer or Read Sector function.

BOOTSTRAPPING THE RXV21

The RXV11 bootstrap loader program loads the system monitor from disk into system memory. No system operation can occur until the monitor is contained in system memory. Bootstrapping ("booting") the system can be accomplished via a hardware-implemented bootstrap in the REV11-A, or the BDV11 option, or it can be entered and executed via the console device.

The following bootstraps are entered under microcode ODT. The bootable volume must be in drive zero. All devices are at standard addresses and vectors. Enter the code starting at location 1000. Inhibit all interrupts by entering RS/___340 <CR>. Initialize the program counter by entering R7/___1000 <CR>. After the code has been entered, type P.

LOCATION	RX02 DOUBLE DENSITY CODE	RX02 SINGLE DENSITY CODE
1000	12700	12700
1002	100240	100240
1004	12701	12701
1006	177170	177170
1010	5002	5002
1012	12705	12705
1014	200	100
1016	12704	12704
1020	401	401
1022	12703	12703
1024	177172	177172
1026	30011	30011
1030	1776	1776
1032	100445	100437
1034	12711	12711
1036	407	7
1040	30011	30011
1042	1776	1776
1044	100432	100432
1046	100437	110413

RXV21

LOCATION	RX02 DOUBLE DENSITY CODE	RX02 SINGLE DENSITY CODE
1050	304	304
1052	30011	30011
1054	1776	1776
1056	110413	110413
1060	304	304
1062	100431	30011
1064	1776	1776
1066	100421	100421
1070	12711	12711
1072	403	3
1074	30011	30011
1076	1776	1776
1100	10414	100414
1102	10513	10513
1104	30011	30011
1106	1776	1776
1110	100410	100410
1112	10213	10213
1114	60502	60502
1116	60502	60502
1120	122424	122424
1122	120427	120427
1124	3	7
1126	3735	3735
1130	12700	12700
1132	0	0
1134	5007	5007
1136	120427	000003

TEV11 TERMINATOR

INTRODUCTION

The TEV11 terminator module provides 120-ohm termination circuits as shown in Figure 1.

SPECIFICATIONS

Identification	M9400-YB
Size	Double
Power	+5 Vdc ± 5% at 0.54A
Bus Loads	
AC	0
DC	0

DESCRIPTION

Each bus signal line terminates with two resistors as shown in Figure 2. These termination resistors are generally contained in a 16-pin, dual-in-line package which is identical to an IC package. Each package contains 14 termination pairs. The values used are shown in the figure. Daisy-chained grant signals are terminated and jumpered. BIAKI L is jumpered to BIAKO L and BDMGI L is connected to BDMGO L via factory-installed jumper W1.

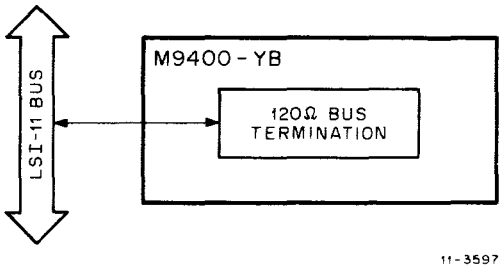


Figure 1 TEV11 Functions

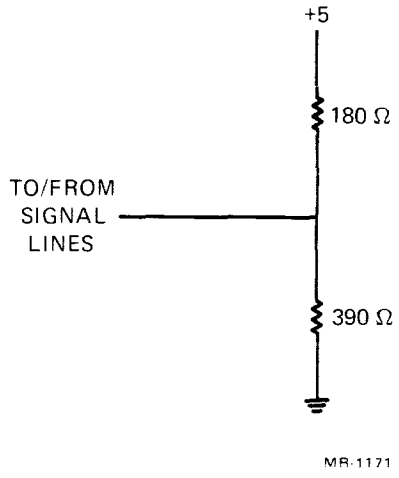


Figure 2 Typical 120-Ohm Bus Termination

TU58 CARTRIDGE TAPE DRIVE

INTRODUCTION

The TU58 is a low-cost intelligent mass memory device that offers random access to block-formatted data on pocket-size cartridge media. It is ideal as inexpensive archive mass storage, or as a software update distribution medium. A dual drive TU58 offers 512 Kb of storage space, making it one of the lowest cost complete mass storage subsystems available.

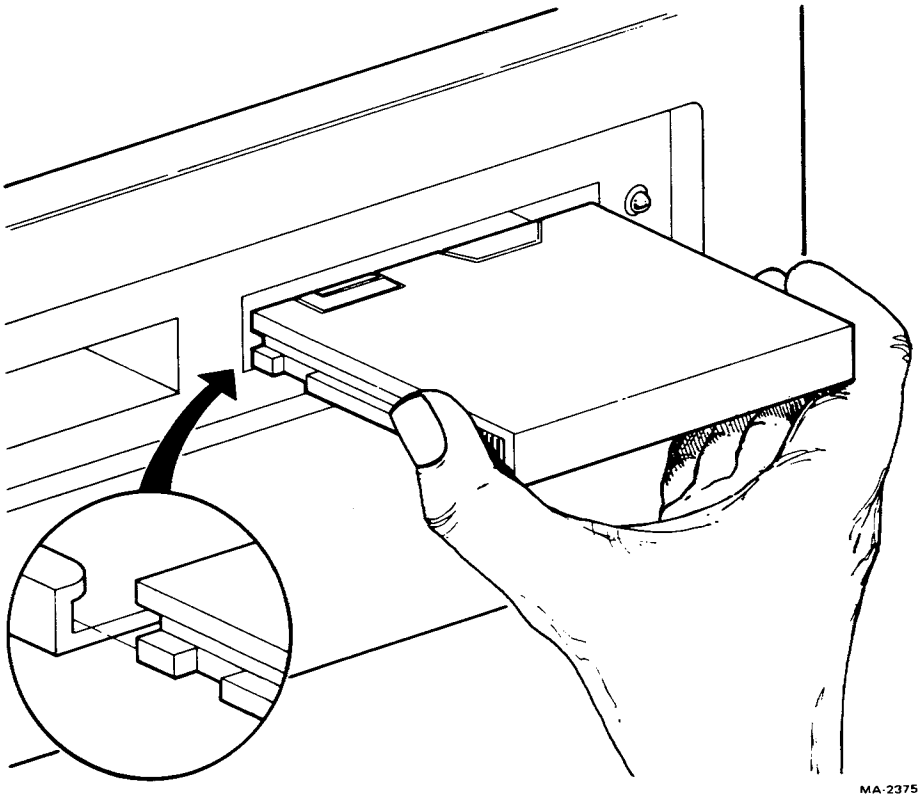


Figure 1 Loading a Cartridge

TU58

FEATURES

- 512 Kb per dual drive subsystem
- RS422, RS423, and RC232-C serial line I/O
- Reliable 30 inches per second read/write tape speed combined with 60 inches per second bidirectional search speed
- Flexible baud rates from 150 to 38,400
- Complete tape subsystem on one P.C. module for compact mounting
- Microprocessor-based subsystem with automatic soft-error recovery via rereads.

SPECIFICATIONS

Performance

Capacity per cartridge	262,144 bytes, formatted in 512 blocks of 512 bytes each
Data reliability	
Soft data error rate	1 in 10^7 bits read (before self-correction)
Hard error rate	1 in 10^9 bits read (unrecoverable within eight automatic retries)
Hard error rate with write verify and system correction	2 in 10^{11} bits read/written
Error checking	Checksum with rotation
Average access time	9.3 seconds
Maximum access time	28 seconds
Read/write tape speed	76 cm/s (30 ips)
Search tape speed	152 cm/s (60 ips)
Bit density	315 bits/cm (800 bits/in.)
Flux reversal density	945 fr/cm (2400 fr/in.)
Recording method	Ratio encoding
Medium	DECtape II cartridge with 42.7 m (140 ft.) of 3.81 mm (0.150 in.) tape Size: 6.1 × 8.1 × 1.3 cm (2.4 × 3.2 × 0.5 in.)

TU58

Track format	Two tracks, each containing 1024 individually numbered, firmware-interleaved "records." Firmware manipulates four records at each operation to form 512-byte blocks.
Drive	Single motor, head integrally cast into molded chassis.
Drives per controller	One or two. Only one may operate at a time.

Electrical

Power consumption	
Module and one or two drives	11 W, typical, drive running +5V ±5% at 0.75A, maximum +12V + 10% −5% at 1.2A, peak 0.6A average running 0.1A idle
Serial interface standards	In accordance with RS422 or RS423; compatible with RS232-C.

Mechanical

Drive	8.1 H × 8.3 D × 10.6 W cm (3.2 × 3.3 × 4.1 in.) with 19 cm (7.5 in.) cable 0.23 Kg (0.516 lbs.)
Board (Module)	13.2 H × 26.5 D × 3.5 W cm (5.19 × 10.44 × 1.4 in.) 0.24 Kg (0.5316 lbs.)
Power connector to module	AMP 87159-6 with 87027-3 contacts (DEC part nos. 12-12202-09, 12-12203-00)
Interface connector to module	AMP 87133-5 with 87124-1 locking clip contacts and 87179-1 index pin (DEC part nos. 12-14268-02, 12-14267-00, 12-15418-00)

Environmental

Maximum dissipation	
TU58-AB, TU58-BB	34 Btu/hour
Temperature	
TU58-AB,BB operating	15°C (59°F) to 4 °C (108°F)
TU58-AB,BB nonoperating	−34°C (−30°F) to 60°C (140°F)
Medium operating temperature	0°C (32°F) to 50°C (122°F)
Maximum temperature difference between system ambient and TU58 module	18°C (32.4°F)
Relative Humidity, noncondensing	
TU58 operating	
Maximum wet bulb	26°C (79°F)
Minimum dew point	2°C (36°F)
Relative humidity	20% to 98%
TU58 nonoperating	5% to 98%
Medium nonoperating	10% to 80%

DRIVE AND MODULE INSTALLATION

Figures 2 and 3 provide the mounting dimensions for the circuit board (module) and drive mechanism. The drive has a 19 cm (7.5 in.) cable which plugs into the module header with the wires coming out of the plug toward the center of the module. The plug is keyed to ensure proper orientation. The cartridge extends 1.60 cm (0.62 in.) from the front of the drive. If the drive is recessed in a panel, clearance must be provided around the opening for fingers to grip the cartridge. Ideally, the cartridge slot in a front panel will be somewhat larger than minimum, to allow easy insertion. The opening should be at least the dimensions of the cartridge, 1.3 cm (0.5 in.) × 8.1 cm (3.2 in.), located not more than 0.53 cm (0.17 in.) above the bottom mounting surface.

The module should be mounted on a flat surface with 3 mm (4-40) hardware and 1 cm (3/8 in.) standoffs. Both the module and the drive

may be mounted at any angle. For mounting to a surface above the drives, the 1.80 cm (0.71 in.) clearance is required; hole spacing is given in the outline drawings. For mounting to a surface below the drives, an 8.18 cm (3.22 in.) × 8.89 cm (3.50 in.) chassis cutout is required, with the same mounting hole spacing.

CAUTION

The mounting surface for the drives must be flat within 0.64 cm (0.025 in.).

INTERFACE STANDARDS SELECTION AND SETUP

The TU58 is shipped with factory-installed jumpers for a transmission rate of 38.4 kilobaud, and the RS-423 unbalanced line interface. A variety of standards and rates may be selected by changing the jumpers on the controller module. Table 1 provides a list of all the pins on the board and their functions, including the wire-wrap (WW) pins, interface, and power connectors.

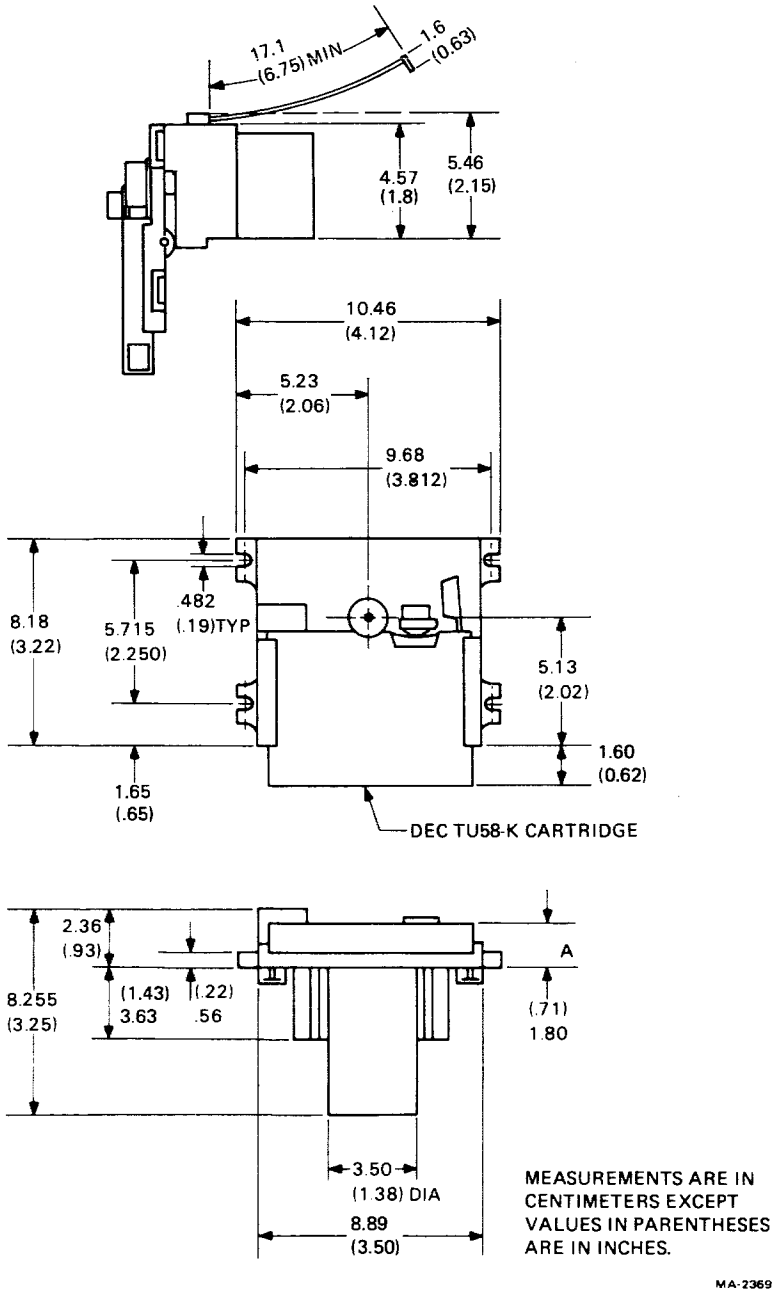


Figure 2 Drive Outline Drawings

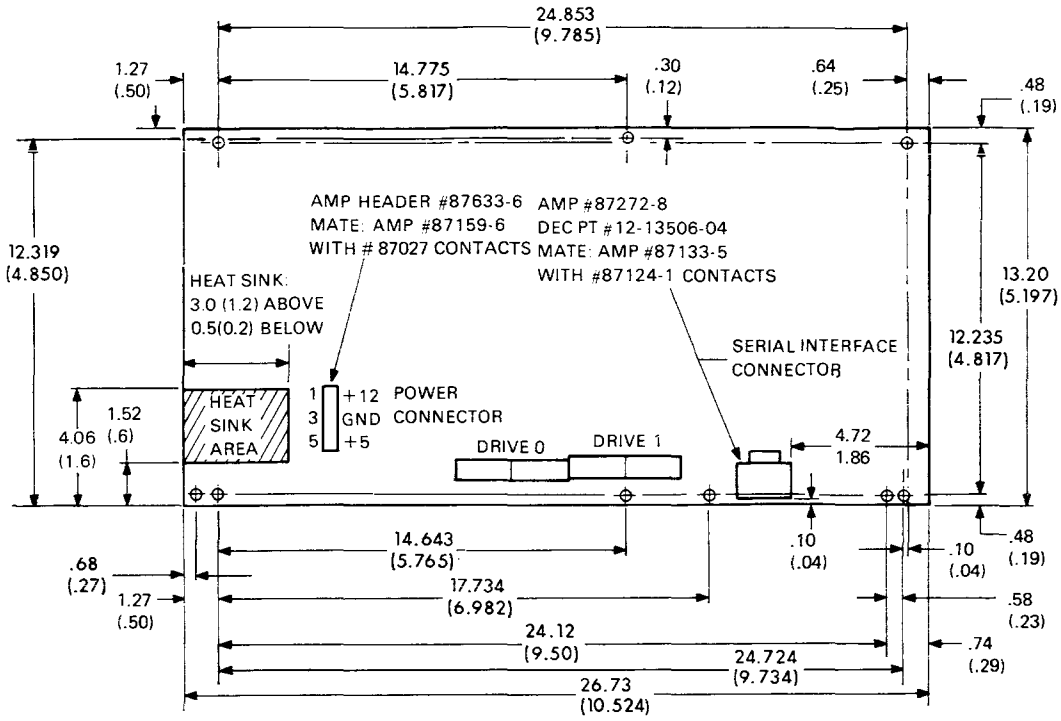


Figure 3 Module Outline Drawing

Table 1 TU58 Module Connections

Wire-Wrap Pins	
WW1	150 baud
WW2	300 baud
WW3	600 baud
WW4	1200 baud
WW5	2400 baud
WW6	4800 baud
WW7	9600 baud
WW8	19,200 baud
WW9	38,400 baud
WW10	UART Receive Clock
WW11	UART Transmit Clock
WW12	Auxiliary A (to interface connector pin L)
WW13	Auxiliary B (to interface connector pin A)

WW14	Factory Test Point
WW15	Ground
WW16	Boot Connect together for auto-boot on power-up
WW17	RS-423 Driver
WW18	RS-423 Common (Ground)
WW19	Transmit Line +
WW20	Transmit Line −
WW21	RS-422 Driver +
WW22	RS-422 Driver −
WW23	Receiver Series Resistor
WW24	(Jump for RS-422)

Serial Interface Connector

J2-10	Auxiliary B	J2-5	Ground
J2-9	Ground	J2-4	Transmit Line −
J2-8	Receive Line +	J2-3	Transmit Line +
J2-7	Receive Line −	J2-2	Ground
J2-6	Key (no connection)	J2-1	Auxiliary A

Power Input Connector

J1-1	+12V
J1-3	Ground
J1-5	+5V
J1-6	Ground

Drive Cable

J3,4-1	Cart L	J3,4-9	LED
J3,4-2	No Connection	J3,4-10	Head Shield Ground
J3,4-3	Permit L	J3,4-11	Erase Return
J3,4-4	Signal Ground	J3,4-12	Erase 1
J3,4-5	Motor +	J3,4-13	Erase 0
J3,4-6	Motor −	J3,4-14	Head Return
J3,4-7	+12V	J3,4-15	Head 0
J3,4-8	Tachometer	J3,4-16	Head 1

VK170-CA

SERIAL VIDEO MODULE

INTRODUCTION

The VK170 module forms an integral part of a terminal. The module accepts serial ASCII encoded data to be stored in a refresh memory to generate a display for a video monitor. The VK170 also accepts parallel data from a keyboard (on strobe demand) to generate serial ASCII output.

The VK170 is an extended-length, double-height, single-width board. Mounting holes are provided for stand-off mounting via handle rivets and two holes located near the module fingers.

FEATURES

- Complete video subassembly on a double-height module
- Displays 80 characters per line and 25 lines
- 7 × 7 characters displayed in 8 × 8 character cells using standard installed character ROM
- 8 × 8 character cell allows simple graphics with customer-defined character set
- Selectable attributes:
  - blink
  - half intensity
  - reverse video
  - characters, from customer-defined character set
- I.C. socket for two customer-defined character sets (2716 EPROM or equivalent)
- EIA RS-423 serial interface for direct interconnect to DLV11-J or MXV11
- Jumper-selectable baud rates: 150, 300, 600, 1200, 2400, 4800, 9600, 19,200, 38,400
- Smooth scrolling
- Drives standard video monitors over coaxial cable per EIA RS170, or jumper-selectable for direct drive monitor
- Interfaces to a standard keyboard (8-bit ASCII)
- Can be plugged into LSI-11 backplanes or mounted on stand-offs applying power via H807 edge connector

VK170-CA

SPECIFICATIONS

Height	13.2 cm (5.2 in.)
Length	22.3 cm (8.5 in.)
Width	1.27 cm (0.5 in.)
Power Requirements	+5V ±5%, 1.2A +12V (or −15V) ±3%, .15A

The VK170 module operates under the following conditions:

- Environment must conform to:
  Temperature 5°C to 60°C
  Humidity 10% to 95% (no condensation)
- Power dissipation is based on circuit requirements of 1.8 amps maximum. If only 5 Vdc is used, power dissipation does not exceed 9 watts. An additional 2 watts (nominal) is dissipated when the 12 volts is enabled.

CONFIGURATION

Interface

This section describes the sequences of signal exchanges that occur among the VK170 and other external devices. Figure 1 shows the pin number locations of the interfacing connectors.

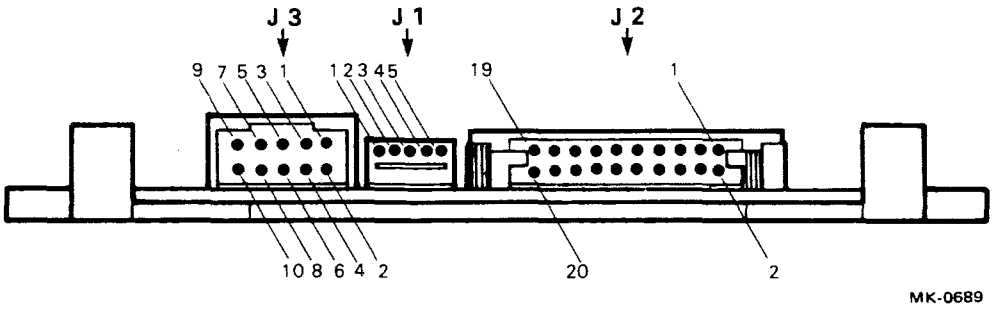


Figure 1 Connector Pin Number Location Diagram

Keyboard/VK170 Interface

The keyboard interfaces to the VK170 via a 20-pin connector (J2). The DIGITAL mating connector is the H8561. Table 1 presents the connector pin numbers and associated signal names.

Table 1 Keyboard/VK170 Connector (J2)

Pin No.	Signal Name	Pin No.	Signal Name
1	+5 Volts	11	KB4
2	−12 Volts	12	Not used
3	GND	13	KB3
4	KB8	14	BREAK (GND)
5	KB7	15	KB2
6	GND	16	GND
7	KB6	17	KB1 (LSB)
8	KBSTRB H	18	GND
9	KB5	19	Not Used
10	BREAK	20	Not Used

Edge Connector

VK170 edge connector pins and associated signals are presented in Table 2.

Table 2 VK170 Edge Connector

Pin No.	Signal Name
AA2,BA2	+5 Vdc
AC2,AT1,BC2,BT1	GND
AB2	−15 Volts
AD2	+12 Volts
Others	Not Connected

Video Output Connector

Video output is provided as RS170 compatible and as separate TTL output lines. A 5-pin MOLEX* connector (J1) is used with pin assignments as shown in Table 3. (Mating connector = H8562.)

Composite video output provides RS170 output generated by combining the video signal with a composite sync signal. The picture from the balancing level to reference white across 75 ohms is 1 volt. The synchronizing levels are imposed at 40% of the signal.

* Vendor Trademark

Table 3 Video Output Connector (J1)

Pin No.	Signal Name	Timing/Freq
1	HORIZONTAL DRIVE H	15.36 kHz/27 μs
2	VERTICAL DRIVE L	60 Hz/520 μs
3	VIDEO HI Z	
4	GND	
5	RS170 VIDEO	

0 volts = SYNC
0.4 volts = BLACK
1.4 volts = WHITE

For direct drive output, jumper W4 must be cut, providing a high impedance source at the MOLEX* connector, pin 3. The VK170 has been tested with the following direct drive monitors:

- ITOH
- Ball Brothers
- Elston

Communications Port Connector

The communications port is a 10-pin connector (J3), pinned for direct DLV11-J connection. The electrical interface may be wired for RS-423 or 20 mA communication (see Figure 2). The DIGITAL mating connector is H8560. Table 4 presents the pin assignments and associated signal names.

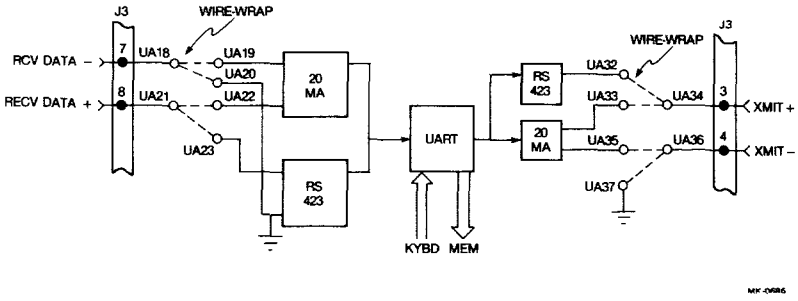


Figure 2 Select RS-423/20 mA Loop

* Vendor Trademark

Table 4 Communications Port Connector (J3)

Pin No.	Signal Name
1	CLOCK I/O
2	GND
3	XMIT DATA +
4	XMIT DATA –
5	GND
6	NOT USED/POLARIZING POINT
7	RCV DATA –
8	RCV DATA +
9	GND
10	20 mA SOURCE

Installation Procedures

The following sections describe the installation of the VK170 module.

Jumper Configurations

Figure 3 illustrates the location of the various jumpers and wire wrap posts of the VK170. Verify that the factory-installed jumpers are configured per Table 5. Any jumper configuration changes required for user applications should be made at this time.

Data Rate Selection

The data rates are generated via a 13.5168 MHz crystal and selected through a dual 4-bit decade and binary counter. The following data rates are selectable: 150, 300, 600, 1200, 2400, 4800, 9600, 19,200, and 38,400 bits per second.

The UART may be configured to transmit and receive at either the same data rate or at split data rates. Data rates are configured by connecting a jumper from the selected data rate wire-wrap pin to the clock input pin(s) of the UART. When configuring at the same data rate, the wire-wrap pins may be daisy-chained. Table 6 lists the data rates and their respective pin numbers.

The UART can be configured to operate from an external clock source via pin 1 of J3. Both UA26 and UA27 must be jumpered to the external clock. Do not select a data rate pin when using an external clock.

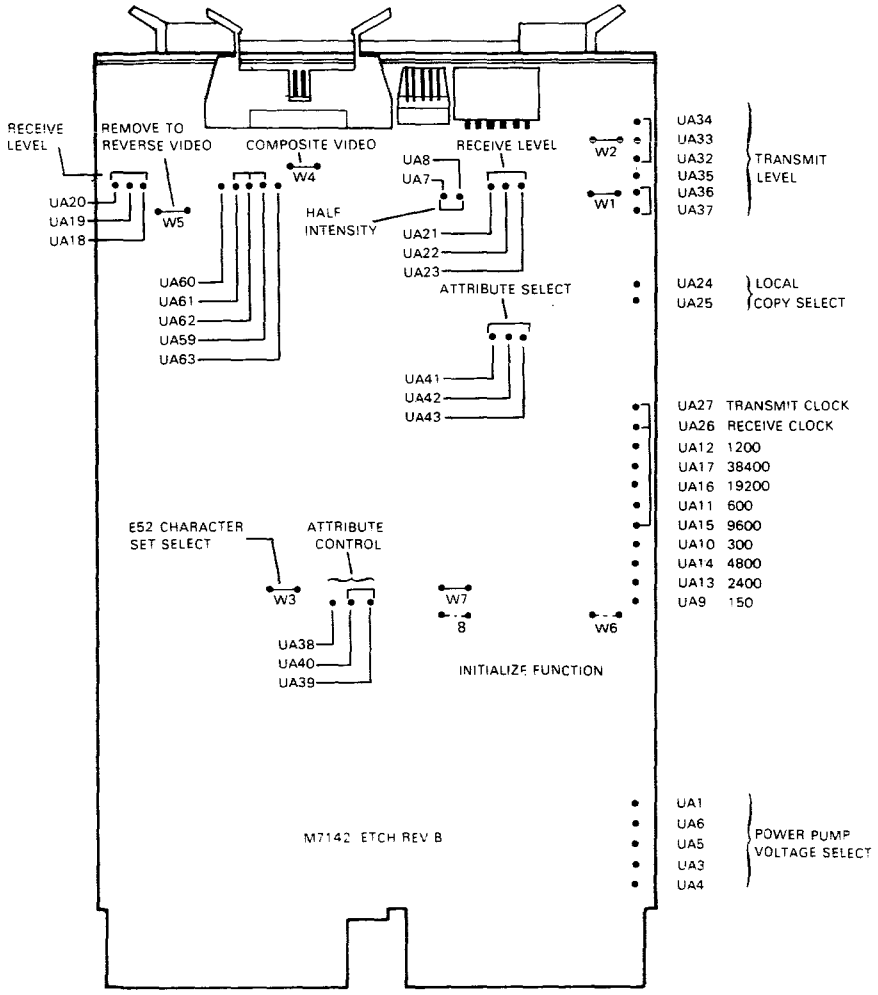


Figure 3 Jumper and Wire Wrap Post Locations

Table 5 Factory- Installed Jumper Configurations

Jumper	Function Implemented
W1 (or UA1 to UA5)	+ 12V operation
W2 (or UA4 to UA6)	
W4	RS170 operation
W7	Form feed receive enabled for remote initialization
UA59 to UA61 to UA62	8-bit—no parity

Jumper	Function Implemented
UA18 to UA20	
UA21 to UA23	EIA RS-423 operation
UA34 to UA32	
UA36 to UA37	
W3	E52 character set enabled
UA39 to UA40	SI/SO (Shift In/Shift Out) attribute control
W5	Forward video
UA41 to UA43	Blink attribute enabled
UA26 to UA27 to UA15	9600 data rate selected

Table 6 Data Rate Jumper Configurations

FROM	TO Pin	Data Rate
	UA9	150
	UA10	300
Transmit clock	UA11	600
pin UA27	UA12	1200
and/or	UA13	2400
Receiver clock	UA14	4800
pin UA26	UA15	9600
	UA16	19200
	UA17	38400

Attributes and Attribute Control Selection

Several jumpers are used for attribute and attribute control selection. Table 7 lists the various attribute and attribute control configurations.

Communications Selection

Four jumpers are used for communications selection. Table 8 lists the jumper configurations required for either EIA RS-423 or 20 mA current loop communications.

Table 7 Attribute Jumper Configurations

Jumper	Characteristic
W3	Install to enable character ROM E52 Remove to enable character ROM XE53
W5	Install for forward video Remove for reverse video
UA7 to UA8	Install to disable half intensity
UA41 to UA42	Install to select reverse attribute
UA41 to UA43	Install to select blink attribute
UA40* to UA38	Install to select character bit 8 for attribute control
UA40* to UA39	Install to select SI/SO for attribute control

* UA40 can either be jumpered to UA38 or UA39, but not both at the same time.

Table 8 Communications Jumper Configurations

	TO	
FROM	**RS423**	**20 mA**
UA18	UA20	UA19
UA21	UA23	UA22
UA34	UA32	UA33
UA36	UA37	UA35

Parity Selection

As many as three jumpers can be used to select ASCII serial data format. Table 9 lists the jumper configurations required to select either odd, even, or no parity.

Voltage Selection

As many as six jumpers (two are optional) can be used for voltage selection. Table 10 lists the jumper configurations required for either + 12 Volt or − 15 Volt operation.

Table 9 Parity Jumper Configuration

Characteristic	Jumper
No Parity (8 data bits)	UA59 to UA61 to UA62
Odd Parity (7 data bits)	UA60 to UA61 to UA62 to UA63
Even Parity (7 data bits)	UA60 to UA61 to UA62 and UA59 to UA60

Table 10 Voltage Jumper Configurations

Jumper	+12V	−15V
W1 (or UA1 to UA5)	In	Out
W2 (or UA4 to UA6)	In	Out
UA3 to UA5	Out	In
UA1 to UA6	Out	In

Remote Initialize Selection

As many as three jumpers are used for remote initialize selection. Table 11 lists the jumper configuration required for remote initialization.

Table 11 Remote Initialize Jumper Configurations

Characteristic	W6	W7	W8
Form Feed Receive	Out	In	Out
Break	In	Out	In
None	Out	Out	In
Form Feed or Break	In	In	Out

W9500 HIGH-DENSITY WIRE-WRAPPABLE MODULES

INTRODUCTION

The W9500 series of high-density wire-wrappable modules enables a user to easily configure special interface logic for the LSI-11 Microcomputer systems. These modules consist of DIGITAL's standard double-and quad-height sizes and are available with or without premounted Dual-In-Line Packages (DIP) low-profile sockets.

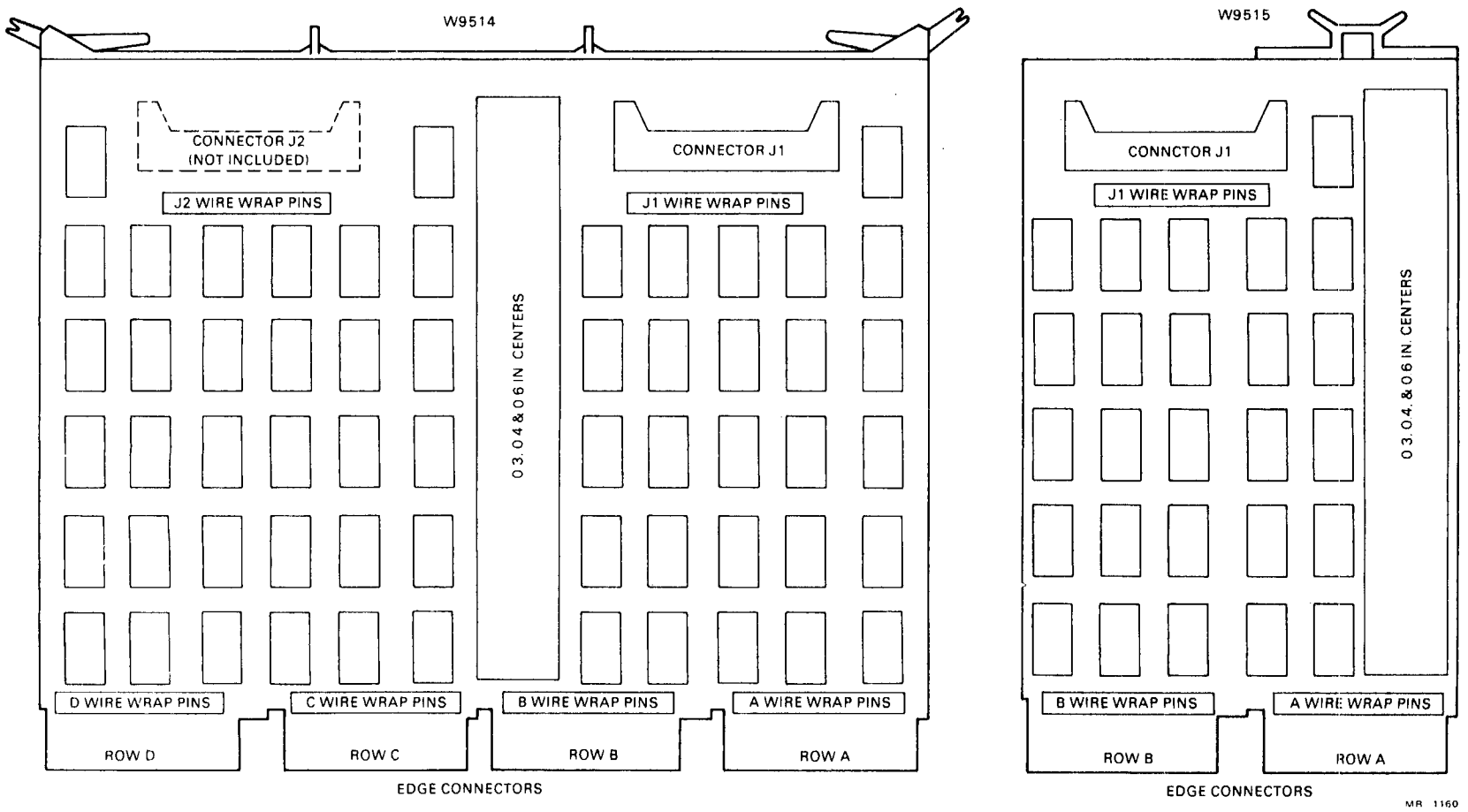
SPECIFICATIONS

W9511 Quad-Height Without Sockets

Height	Quad, 10.5 in (26.6 cm)
Length	Extended, 8.9 in (22.8 cm)
Width	Single, 0.5 in (1.27 cm)
Vcc Pins	AA2, BA2, CA2, DA2
GND Pins	AT1, BT1, CT1, DT1, AC2, BC2, CC2, DC2

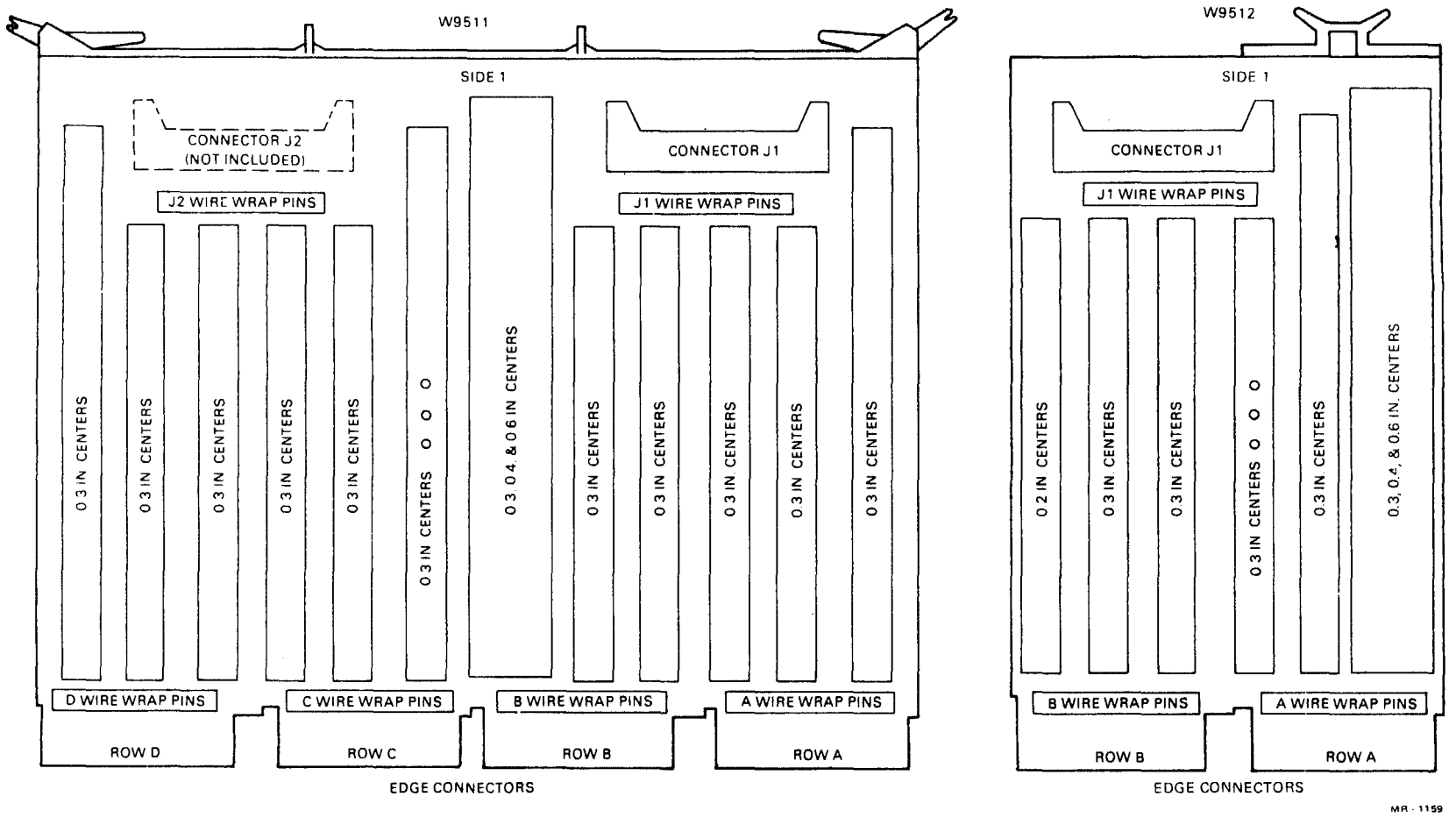
W9512 Double-Height Without Sockets

Height	Double, 5.2 in (13.2 cm)
Length	Extended, 8.9 in (22.8 cm)
Width	Single, 0.5 in (1.27 cm)
Vcc Pins	AA2, BA2
GND Pins	AT1, BT1, AC2, BC2



W9500

Figure 1 LSI-11 Bus-Compatible Modules (With DIP Sockets)



W9500

Figure 2 LSI-11 Bus-Compatible Modules (No DIP Sockets)

W9500

DESCRIPTION

The LSI-11 compatible series consists of four modules-- a quad-height with and without premounted sockets and a double-height with and without premounted sockets.

Table 1 provides a brief summary of each type. All modules are **single**-width; the height of each pin is 5/16 in

Each module without premounted sockets is configured to accept IC packages with pin centers on 0.3 in (7.62 cm); 0.4 in (10.16 cm); and 0.6 in (15.24 cm). Each module can be wrapped by standard automatic wrapping techniques as well as by hand.

Those modules with premounted sockets accept 16-pin ICs with 0.3 in centers. Space is provided between the sockets for decoupling capacitors or other discrete components as required by the user. In addition, these modules supplied with sockets also contain universal areas that will accept ICs with pin centers of 0.3 in (7.62 cm); 0.4 in (10.16 cm); and 0.6 in (15.24 cm). The accompanying drawings point out these universal areas and their capacities.

The printed circuit on each board connects the appropriate edge connector pins to the Vcc plane on side 2 of the board and the ground plane (GND) on side 1 (component side). The remaining edge connector pins terminate to a double row of wire-wrap pins for user designated functions. Each of the modules also includes a 40-pin male cable connector to allow an interface cable to be attached to the module logic. The pins of the cable connector are also terminated to a double row of wire-wrap pins. The quad-height modules are also provided with a space where an additional 40-pin cable connector (labeled J2) can be inserted by the user. When a connector is not required, additional IC packages with .3, .4, and .6 in centers can be installed in the space reserved for the connector. Each board contains insulated standoffs to maintain the required clearance between adjacent modules and prevent shorting of wire-wrap pins. A helpful alphanumeric X-Y grid pattern is also etched onto each board to facilitate ease in wire-wrap pin location and identification.

Table 1 W9500 Series Modules

Module No.	Description
W9511	Quad-height, extended-length, single-width module with extractor handle. No DIP sockets included. One 40-pin male cable connector premounted on board and space for additional 40-pin connector provided.
W9514	Same as W9511 except with 58 premounted DIP sockets.
W9512	Double-height, extended-length, single-width module with flip chip handle. No DIP sockets included. One 40-pin male cable connector premounted on board.
W9515	Same as W9512 except with 25 premounted DIP sockets.

DMV11

DMV11 SYNCHRONOUS CONTROLLER

INTRODUCTION

The multipoint DDCMP-DMV11 Intelligent Communications Synchronous Line Controller is an interface device which provides efficient high-speed synchronous communications for distributed networks. The DMV11 uses LSI-11 CPUs as control or tributary stations, while requiring a minimum of main CPU resources. The following provides detailed information on the installation and operation of the DMV11.

FEATURES

- Support of point-to-point and multipoint operation
- Support of remote or local, full duplex, or half-duplex configurations
- Support of 12 tributaries and one control station in multipoint operation
- Switch and program selectable operating mode and tributary address
- Support for multiple-addressed tributaries
- Down-line loading and remote load detect capabilities
- Go/No-Go diagnostic testing by the microcode
- Go/No-Go extensive error reporting
- Modem control

There are three available DMV11 options. These are the DMV11-AA, the DMV11-AB, and the DMV11-AC. The devices comprising each of these three options are described below.

The DMV11-AA

- An M8053-MA microcontroller/line unit (a quad-height module with multipoint microcode)
- An H3254 (V.35 or integral modem) module test connector
- H3255 (RS-423-A/232-C) module test connector
- A BC55H cable and an H3250 and H3251 cable turnaround test connector

DMV11

The DMV11-AB

- An M8053-MA microcontroller/line unit (a quad-height module with multipoint microcode)
- An H3254 (V.35 or integral modem) module test connector
- H3255 (RS-423-A/232-C) module test connector
- A BC05Z-25 cable and an H3250 and cable turnaround test connector

The DMV11-AC

- An M8064-MA microcontroller/line unit (a quad-height module with multipoint microcode)
- An H3254 (V.35 or integral modem) module test connector
- H3255 (RS-423-A/232-C) module test connector
- A BC55F cable and H3257 and H3258 terminators

Table 1 Interface and Line Speed

Option	Interface	Line Speed (DMV11 Limitations)
DMV11-AA	EIA RS-232-C EIA RS-423-A	Up to 19.2K b/s Up to 56K b/s
DMV11-AB	CCITT V.35	Up to 56K b/s
DMV11-AC	Integral modem	56K b/s only

System Requirements

- LSI-11 bus loading: The M8053-MA or the M8064-MA present two ac loads and one dc load to the LSI-11 bus.
- Power requirements: Check the power supply before and after installing the microcontroller/line unit to ensure against overloading. Power requirements are listed in Table 2.
- Interrupt priority: The interrupt priority is preset to level four.
- Device address assignments: The DMV11 address resides in the floating address space of the LSI-11 bus addresses. The selection of the device address is accomplished by switch packs on the microcontroller/line unit module. Refer to Figures 1 and 2, and Table 3.
- Device vector address assignment: The DMV11 vectors reside in the floating vector space of the LSI-11 bus addresses. The selection of the vector address is accomplished by a switchpack on the micro-

controller/line unit module. Refer to Figures 1 and 2, and Table 4.

- Device selectable feature: Please refer to Figures 1 and 2, and Table 5.

Table 2 DMV11 Voltage Chart

Module	Voltage Rating	Maximum Voltage	Minimum Voltage	Backplane Pin
M8053-MA	+5 V @ 3.4 A +12 V @ 0.380 A	+5.25 +12.60	+5.0 +11.40	AA2 AD2
M8064-MA	+5 V @ 3.35 A +12 V @ 0.260 A	+5.25 +12.60	+5.0 +11.40	AA2 AD2

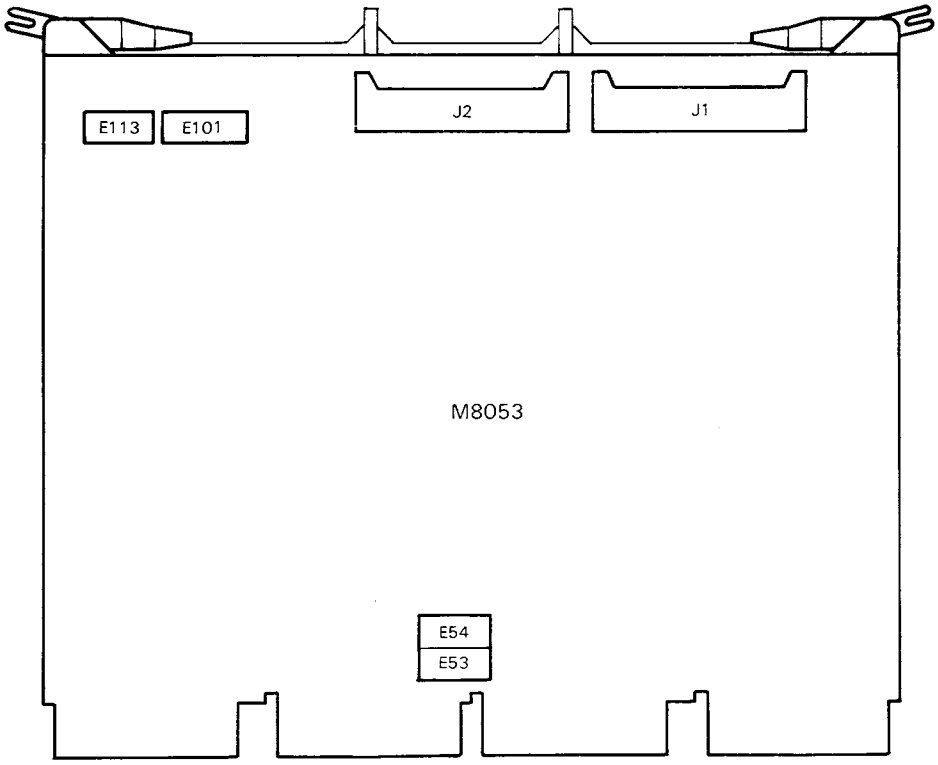


Figure 1 M8053 Switch Locations

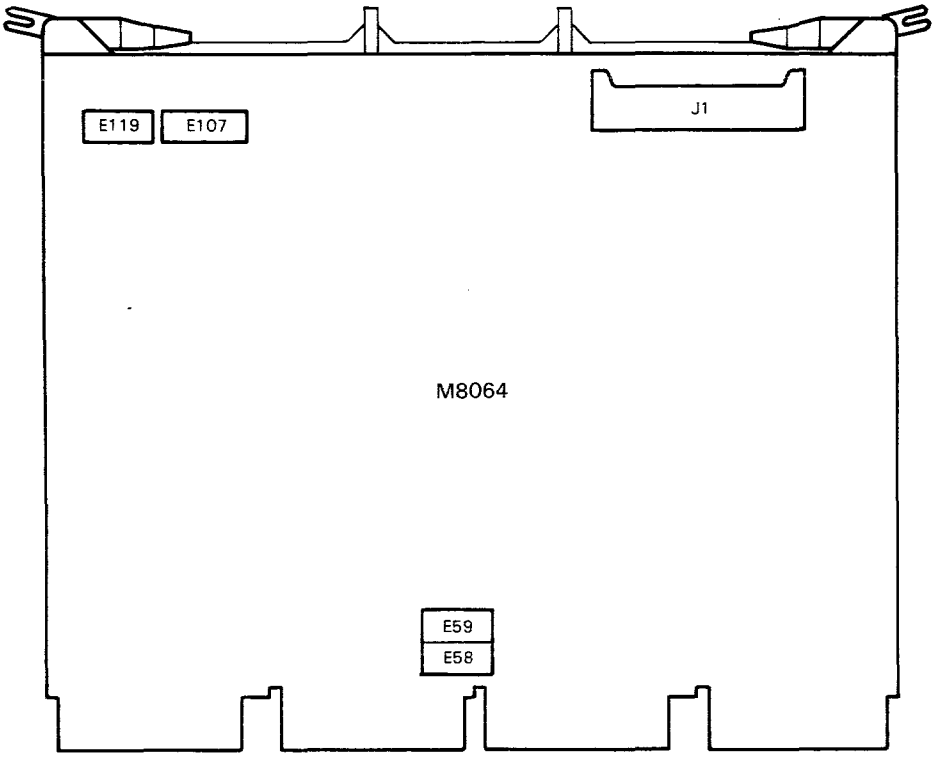


Figure 2 M8064 Switch Locations

PROGRAMMING

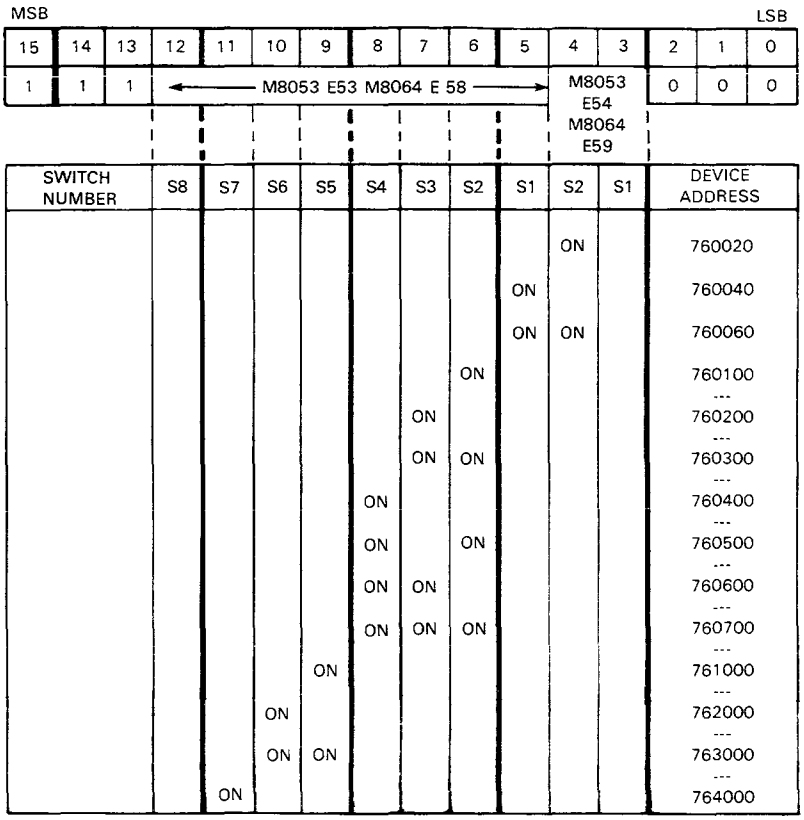
Presented in the following paragraphs is a brief overview of the programming sequences relevant to DMV11 operation in network environments. For further detailed information covering programming and installation, the DMV11 User Guide is available and can be ordered as supplementary material. The order number is EK-DMV11-UG-001.

Transfer of control and status information between the main CPU resident user program and the DMV11 is accomplished through four 16-bit control and status registers (CSRs). Input commands are issued to the DMV11 by the user program, and output responses are issued to the user program by the DMV11.

NOTE

Normally only four CSRs are used, but in 22-bit address mode, eight CSRs are available.

Table 3 Device Address Selection



NOTE: SWITCH ON RESPONDS TO LOGICAL ONE ON THE BUS

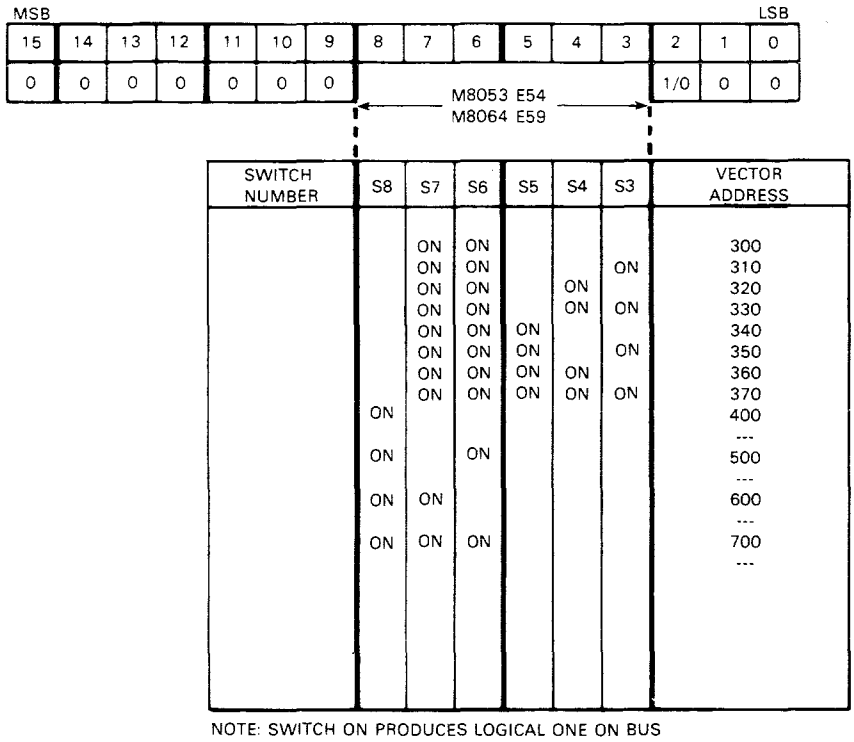
Control and Status Registers

Four 16-bit CSRs are used to transfer control and status information. These registers are both byte and word addressable. The eight bytes are assigned addresses in the floating address space in the I/O page as follows: 16XXX0, 16XXX1, 16XXX2, 16XXX3, 16XXX4, 16XXX5, 16XXX6, and 16XXX7.

For discussion, these byte addresses are designated byte select 0 through 7 (BSEL0 through BSEL07). BSEL10 and BSEL11 are only used in 22-bit address mode. BSEL12 through BSEL17 are not used bythe user/DMV11-command structure and are not referred to in this section.

The four word addresses are the even numbered locations and are designated select 0, 2, 4, and 6 (SEL0, SEL2. SEL4, and SEL6). The CSR addresses are assigned to the floating address space. The floating ad-

Table 4 Vector Address Selection



dress ranking for the DMV11 is 24. Detailed bit descriptions of SEL0 and BSEL2 are provided in Tables 6 and 7 respectively.

The four bytes comprising SEL4 and SEL6 contain the fields pertinent to each user-program command and DMV11 response.

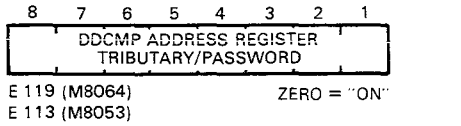
Input Commands Overview

Input commands, in general, provide the means for the user program to assign, receive, or transmit buffers to the DMV11.

There are four types of input commands that can be issued to the DMV11 for execution. These commands are the microprocessor control/maintenance command; the mode definition; control; and buffer address/character count.

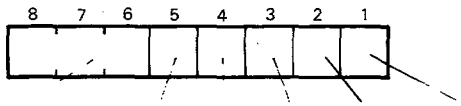
With the exception of the microprocessor control/maintenance command, input commands require an identifcation code in the first three bits of BSEL2. These codes, which define each command and variations of specific commands within the command set, are defined in Tables 7 and 8.

Table 5 Switch Selectable Features



E 119 (M8064)
E 113 (M8053)

ZERO = "ON"



MODE WHEN SWITCH ONE IS SET

REMOTE LOAD DETECT ENABLE

POWER ON BOOT ENABLE

AUTO ANSWER

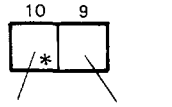
UNIT NUMBER FOR BOOTING

MODE ENABLE

E 107 (M8064)
E101 (M8053)

ZERO = "ON"

8	7	6	SWITCH SETTING FOR THE MODE OF OPERATION.
ON	ON	ON	HDX PT TO PT DMC COMPATIBLE
ON	ON	OFF	FDX PT TO PT DMC COMPATIBLE
ON	OFF	ON	HDX POINT TO POINT
ON	OFF	OFF	FDX POINT TO POINT
OFF	ON	ON	HDX CONTROL STATION
OFF	ON	OFF	FDX CONTROL STATION
OFF	OFF	ON	HDX TRIBUTARY STATION
OFF	OFF	OFF	FDX TRIBUTARY STATION



"ON" = V.35
"OFF" = EIA
M8053

HIGH SPEED

E 107 (M8064)
E 101 (M8053)
OFF = "LOGIC ONE"

HIGH SPEED SWITCH MUST BE SET FOR INTEGRAL MODEM OR WHEN RUNNING ABOVE 19.2KB

* UNUSED
ON
M8064

ZERO = "ON"

Table 6 SEL0 Bit Functions

Bits	Name	Description
BSEL0		
0	Interrupt Enable In (IEI)	When set, this bit enables the DMV11, upon asserting RDI (bit 4 of BSEL2), to generate an interrupt to vector address XX0.
1-3	Reserved	
4	Interrupt Enable Out (IEO)	When set, this bit enables the DMV11, upon asserting RDO (bit 7 of BSEL2), to generate an interrupt to vector address XX4.
5-6	Reserved	
7	Request In (RQI)	This bit is set by the user program to request access to the data port. It is cleared by the user program when the data port is not required for further issuing of commands. The user program may leave RQI set if successive requests for the data port are pending.
BSEL1		
8	Maintenance Request	When set, along with master clear (bit 14 of SEL4), this bit causes the DMV11 to enter the maintenance register emulation section of the microcode. **NOTE** **Detailed discussion of maintenance register emulation is presented in Section 4.8.**
9-10	Reserved	
11	Diagnostic Mode	When set, this bit allows diagnostic programs to change the mode of operation of the DMV11 using the mode definition command to override the mode switches.
12	Reserved	

Bits	Name	Description
13	Invoke P/MOP Boot	Invoke primary MOP mode. When set to one, this bit causes the DMV11 at this multipoint station to request that the control station initiate the primary MOP (maintenance operation protocol) boot procedure. In point-to-point networks, a DMV11 having this bit set requests the other station to initiate the primary MOP boot procedure. **NOTE** **The master clear bit (bit 14) must also be asserted to use invoke P/MOP.**
14	Master Clear	When set, this bit initializes the DMV11. The clock is enabled and the RUN flip-flop is set. Master clear is self-clearing.
15	Run	This bit controls running of the microprocessor. It is set by bus initialization or master clear. When run is cleared the microprocessor halts.

Table 7 BSEL2 Bit Functions

Bits	Name	Description
0-2	Control/Response Code	These bits define the type of input command or output response as follows.

Bits			Description
2	1	0	
0	0	0	Buffer address/character count (RCV) command or buffer disposition (RCV complete) response

Bits	Name	Description
		0 0 1 Control command or control response 0 1 0 Mode definition command or information response 0 1 1 Buffer disposition (RCV unused) response 1 0 0 Buffer address/character count (XMIT) command or buffer disposition (XMIT complete) response 1 0 1 Reserved 1 1 0 Buffer disposition (sent but not acknowledged) response 1 1 1 Buffer disposition (not sent) response
3	22-Bit Mode	This bit when set indicates to the DMV11 that the buffer address is in the 22-bit format.
4	Ready In (RDI)	RDI is the DMV11 response to RQI, indicating to the user program that it has control of the CSRs to issue a command. It is cleared by the user program when the data port contains the input command. Clearing RDI returns control back to the DMV11.
5-6	Reserved	
7	Ready Out (RDO)	RDO is asserted by the DMV11 to indicate that the data ports (SEL4 and SEL6) contain an output response for the user program. The user program must clear RDO after it has read this information. Clearing RDO returns the CSRs to the DMV11.

Table 8 Input Command Codes

Input Command Type	Binary Code(BSEL2)		
	Bit 2	Bit 1	Bit 0
Mode definition	0	1	0
Control	0	0	1
Buffer address/character count (receive)	0	0	0
Buffer address/character count (transmit)	1	0	0

NOTE
CSR addresses are expressed in octal.

Output Responses Overview

Ouput responses provide a means for the DMV11 to report various normal and abnormal (error) conditions concerning the data transfer operation. The three basic responses are buffer disposition, control, and information. The buffer disposition response is used to return both used and unused buffers to the user program.

The control response is used to report error conditions concerning the microcontroller/line unit hardware, data link, physical link, or remote station. It also passes protocol information to the user.

The information response provides information requested by a control command from the user program.

DPV11-DA

DPV11-DA SERIAL SYNCHRONOUS LINE INTERFACE

INTRODUCTION

The DPV11-DA is a serial synchronous line interface for connecting an LSI-11 bus to a serial synchronous modem that is compatible with EIA RS-232-C interface standards and EIA RS-423-A and EIA RS-422-A electrical standards. EIA compatibility is provided for use in local communications only (timing and data leads only). The DPV11-DA is intended for character-oriented protocols, such as BISYNC, byte count-oriented protocols, such as DDCMP, or bit-oriented data communications protocols, such as SDLC. The DPV11-DA does not provide automatic error generating and checking for BISYNC.

The DPV11-DA is a bus request device only and must rely on the system software for service. Interrupt control logic generates requests for the transfer of data between the DPV11-DA and the LSI-11 memory by means of the LSI-11 bus. (Figure 1 illustrates the jumper locations for the DPV11-DA.

The DPV11-DA consists of one double-height module and may be connected to an EIA RS-232-C modem by a BC26L-25 (RS-232-C) cable.

FEATURES

- Full-duplex or half-duplex operation
- Double-buffered transmitter and receiver
- EIA RS-232-C compatibility
- All EIA RS-449 Category 1 modem control
- Partial Category II modem control to include incoming call, test mode, remote loopback, and local loopback
- Program interrupt on transitions of modem control signals
- Operating speeds of up to 56Kb/s (may be limited by software or CPU memory)
- Software-selectable diagnostic loopback
- Operation with bit, byte count, or character-oriented protocols
- Internal cyclic redundancy check (CRC) character generation and checking (not usable with BISYNC)
- Internal bit-stuff and detection with bit-oriented protocols
- Programmable sych character, sync insertion, and sync stripping with byte count-oriented protocols

DPV11-DA

- Recognition of secondary station address with bit-oriented protocols

SPECIFICATIONS

Environment

Operating temperature	5°C to 60°C (41°F to 140°F)
Relative humidity	10% to 90% with max. wet bulb temperature of 28°C (82°F) and a min. dew point of 2°C (36°F)

Electrical specifications

The DPV11-DA requires these voltages from the LSI-11 bus for proper operation	12 V at 0.30 A max. (0.15 A typical) and 5 V at 1.2 A max. (0.92 A typical)

Performance

Operating mode	Full- or half-duplex
Data format	Synchronous BISYNC, DDCMP, and SDLC
Character size	Program-selectable (5-8 bits with character-oriented protocols and 1-8 bits with bit-oriented protocols)
Max. configuration	16 DPV11-DA modules per LSI-11 bus
Max. distance	15 m (50 ft) for RS-232-C 61 m (200 ft) for RS-423-A/RS-422-A (Distance is directly dependent on speed, and 200 ft is a suggested average. See RS-449 specifications for details.)
Max. serial data rates	56 Kb/s (May be less because of software and memory refresh limitations.)

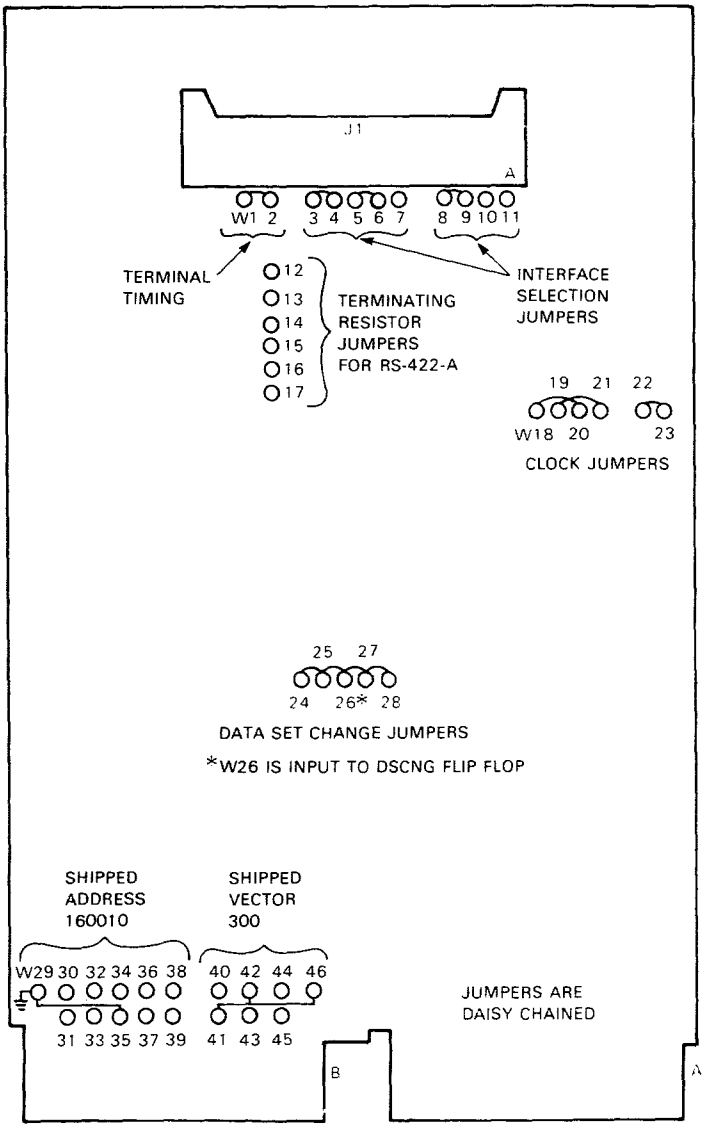


Figure 1 DPV11-DA Jumper Locations

Device Addresses

The five registers used in the DPV11 are shown in Table 4 (page 532). Note that two of the registers (PCSAR and RDSR) have the same address. This does not constitute a conflict, however, because the PCSAR is a write-only register and the RDSR is a read-only register. These five registers occupy eight contigious byte addresses which begin on a boundary where the low-order three bits are zero, and can be located anywhere between 160000_8 and 177776_8.

DPV11-DA

The DPV11-DA uses a universal-synchronous receiver/transmitter (USYNRT) chip which accounts for a large portion of the DPV11-DA's functionality. The USYNRT provides complete serialization, deserialization, and buffering of data to and from the modem.

Most of the DPV11-DA's registers are internal to the USYNRT. Only the receiver control and status register (RXCSR) and the low byte of the parameter control and character length register (PCSCR) are external.

NOTE

When using the special space sequence function, all registers internal to the USYNRT must be written in byte mode.

REGISTER BIT ASSIGNMENTS

Bit assignments for the five DPV11-DA registers are shown in Figure 2. In the paragraphs below a description of each register using a bit assignment illustration and an accompanying table with a detailed description of each bit is provided.

Receive Control and Status Register (RXCSR) (Address 16xxx0)

Figure 3 shows the format for the receive control and status register. Table 5, found on page 532, is a detailed description of the register. This register is external to the USYNRT.

NOTE

The RXCSR can read in either word or byte mode. However, reading either byte resets certain status bits in both bytes.

Receive Data and Status Register (RDSR) (Address 16xxx2)

Figure 4 shows the the format for the receive data and status register. It is a read-only register and shares its address with the parameter control sync/address register (PCSAR) which is write-only. Table 3 is a detailed description of the RDSR.

NOTE

The RDSR can read in either word or byte mode. However, reading either byte resets data and certain status bits in both bytes of this register as well as bits 7 and 10 of the RXCSR.

Parameter Control Sync/Address Register (PCSAR) (Address 16xxx2)

The PCSAR is a write-only register which can be written in either byte or word mode. Figure 5 shows the format and Table 7 is a detailed description of the PCSAR. This register shares its address with the RDSR.

NOTE

Bit set (BIS) and bit clear (BIC) instructions cannot be executed on the PCSCR, since they execute using a read-modify-write sequence.

Parameter Control and Character Length Register (PCSCR) (Address 16xxx4)

The parameter control and character length register can be read from or witten into in either word or byte mode. The low byte of this register is external to the USYNRT and the high byte is internal. Figure 6 shows the format and Table 8 is a detailed description of the PCSCR.

Transmit Data and Status Register (TDSR) (Address 16xxx6)

The format for the transmit data and status register is shown in Figure 7 and in Table 9 is a detailed description. The TDSR is a read/write register which can be accessed in either word or byte mode with no restrictions. All bits can be read from or written into and are reset by the Device Reset or Bus INIT except where noted.

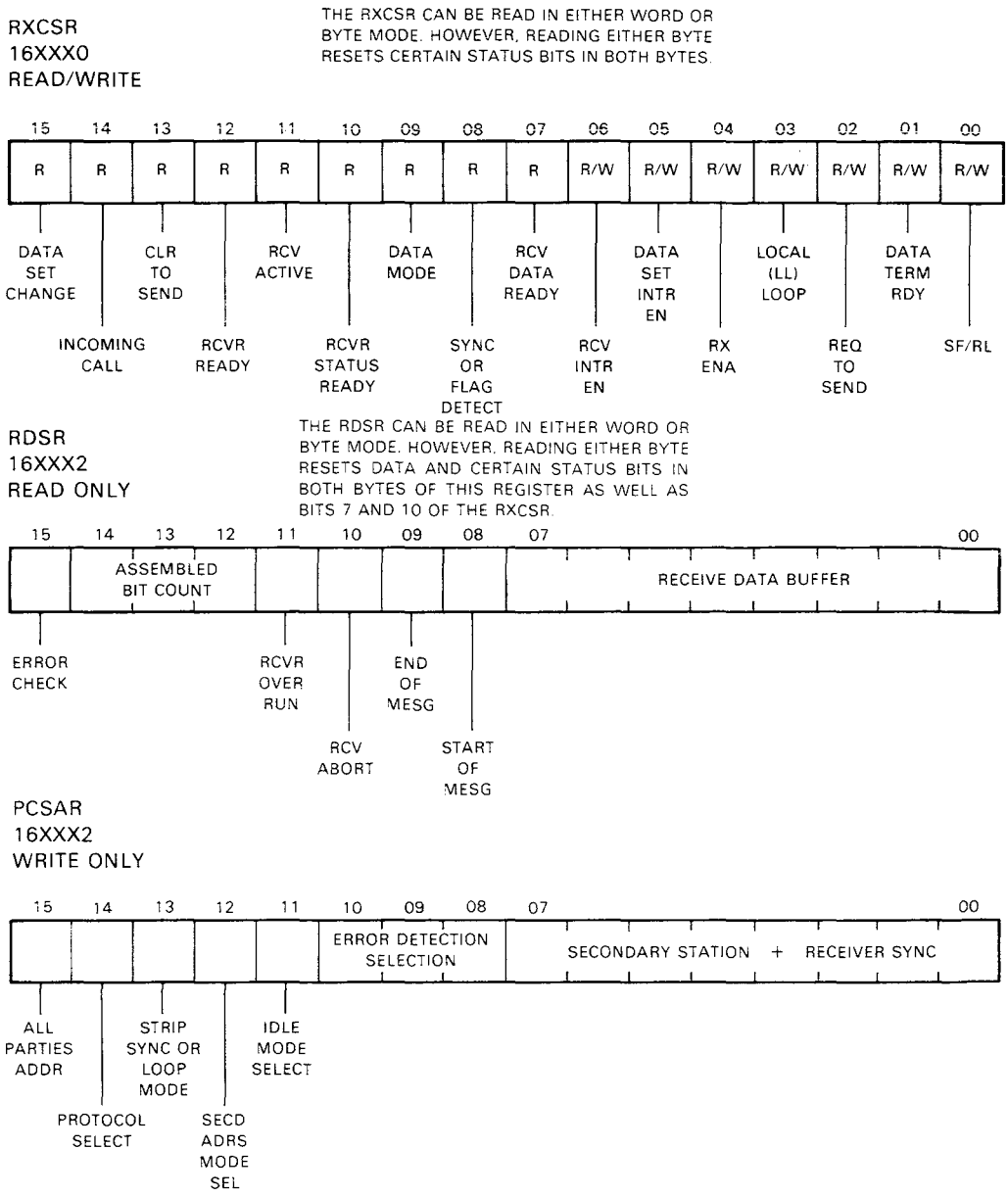
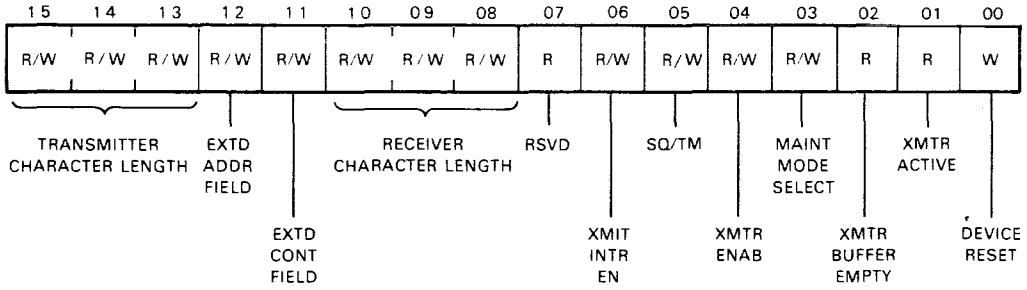


Figure 2 DPV11-DA Register Configurations and Bit Assignments (Sheet 1 of 2)

PCSCR
16XXX4
READ/WRITE



TDSR
16XXX6
READ/WRITE

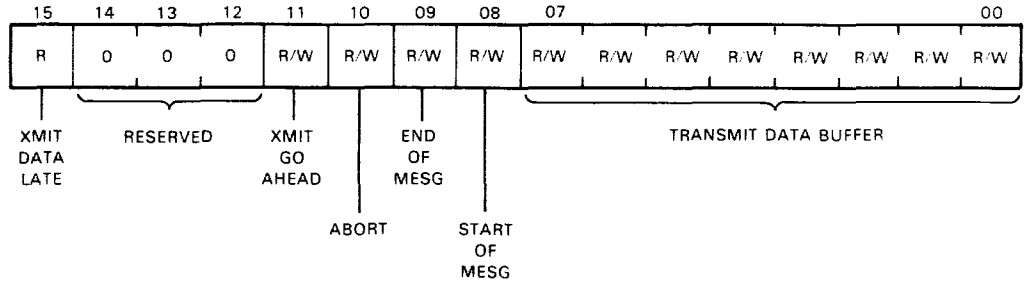
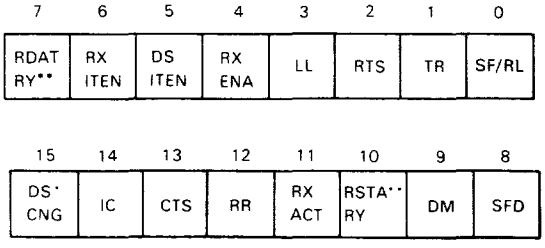


Figure 2 DPV11-DA Register Configurations and Bit Assignments (Sheet 2 of 2)



* THIS BIT IS RESET BY READING EITHER BYTE OF THIS REGISTER.
** THESE BITS ARE RESET BY READING EITHER BYTE OF RSDR.

Figure 3 Receive Control and Status Register (RXCSR) Format

DPV11-DA

Table 1 Jumper Configuration

(W1–W2) Driver Attenuation Jumper

Driver	Normal* Configuration	Alternate* Option	Description
Terminal Timing	W1 to W2	Not connected	Bypasses attenuation resistor. Jumper must be removed for certain modems to operate properly.

(W3–W11) Interface Selection Jumpers

Input Signals	Normal* Configuration	Alternate* Option	Description
SQ/TM (PCSCR-5)	W5 to W6		Signal quality
		W7 to W6	Test mode
DM (DSR) (RXCSR-9)	Not connected	W10 to W9	Data mode return for RS-422-A

(W3–W11) Interface Selection Jumpers (Cont.)

Output Signals	Normal* Configuration	Alternate* Option	Description
SF/RL (RXCSR-0)	W3 to W4		Select frequency
		W5 to W3	Remote loopback
Local Loopback	W8 to W9	Not connected	Local loopback
	Not connected	W8 to W11	Local loopback (alternate pin)

(W12–W17) Receiver Termination Jumpers

Receiver	Normal* Configuration	Alternate* Option	Description
Receive Data	Not connected	W12 to W13	Connects terminating resistor for RS-422-A compatibility

Receiver	Normal* Configuration	Alternate* Option	Description
Send Timing	Not connected	W14 to W15	
Receive Timing	Not connected	W16 to W17	

*Normal configuration is typically RS-423-A compatible. Alternate option is typically RS-422-A compatible.

(W18–W23) Clock Jumpers

Function	Normal* Configuration	Alternate* Option	Description
NULL MODEM CLK	W20 to W18		Sets NULL CLK MODEM CLK to 2 kHz.
		W21 to W18	Sets NULL MODEM CLK to 50 kHz.
Clock Enable	W19 to W21 W22 to W23	W19 to W21 W22 to W23	Always installed except for factory testing.

(W24–W28) Data Set Change Jumpers

Modem Signal Name	Normal* Configuration	Alternate* Option	Description
Data Mode (DSR)	W26 to W24	Not connected	Connects the DSCNG flip-flop to the respective modem status signal for transi-
Clear to Send	W26 to W25	Not connected	tion detection.
Incoming Call	W26 to W27	Not connected	Note: W26 is input to DSCNG flip-flop
Receiver Ready (Carrier Detect)	W26 to W28	Not connected	

*Normal configuration is typically RS-423-A compatible. Alternate option is typically RS-422-A compatible.

(W3–W11) Interface Selection Jumpers

Output Signals	Normal* Configuration	Alternate* Option	Description
SF/RL (RXCSR-0)	W3 to W4		Select frequency
		W5 to W3	Remote loopback
Local Loopback	W8 to W9	Not connected	Local loopback
	Not connected	W8 to W11	Local loopback (alternate pin)

(W12–W17) Receiver Termination Jumpers

Receiver	Normal* Configuration	Alternate* Option	Description
Receive Data	Not connected	W12 to W13	Connects terminating resistor for RS-422-A compatibility
Send Timing	Not connected	W14 to W15	
Receive Timing	Not connected	W16 to W17	

(W18–W23) Clock Jumpers

Function	Normal* Configuration	Alternate* Option	Description
NULL MODEM CLK	W20 to W18		Sets NULL CLK MODEM CLK to 2 kHz.
		W21 to W18	Sets NULL MODEM CLK to 50 kHz.
Clock Enable	W19 to W21 W22 to W23	W19 to W21 W22 to W23	Always installed except for factory testing.

(W24–W28) Data Set Change Jumpers

Modem Signal Name	Normal* Configuration	Alternate* Option	Description
Data Mode (DSR)	W26 to W24	Not connected	Connects the DSCNG flip-flop to the respective modem status signal for transition detection.
Clear to Send	W26 to W25	Not connected	
Incoming Call	W26 to W27	Not connected	Note: W26 is input to DSCNG flip-flop
Receiver Ready (Carrier Detect)	W26 to W28	Not connected	

*Normal configuration is typically RS-423-A compatible. Alternate option is typically RS-422-A compatible.

Table 2 Data Address Selection

DPV11-XX (M8020) DEVICE ADDRESSING

MSB LSB

15	14	13	12	11	10		8	7	6	5	4	3	2	1	0
1	1	1	←			JUMPERS						→	0	0	0

JUMPER NUMBER	W31	W30	W36	W33	W32	W39	W38	W37	W34	W35	DEVICE ADDRESS
										X	760010
									X		760020
									X	X	760030
								X			760040
								X		X	760050
								X	X		760060
								X	X	X	760070
							X				760100

						X					760200

						X	X				760300

					X						760400

					X		X				760500

					X	X					760600

					X	X	X				760700

				X							761000

			X								762000

			X	X							763000

		X									764000

"X" INDICATES A CONNECTION TO W29. W29 IS TIED TO GROUND. JUMPERS ARE DAISY CHAINED.

Table 3 Vector Address Selection

DPV11 (M8020) VECTOR ADDRESSING

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	JUMPERS						1/0	0	0

JUMPER NUMBER	W43	W42	W41	W40	W44	W45	VECTOR ADDRESS
		X	X				300
		X	X			X	310
		X	X		X		320
		X	X		X	X	330
		X	X	X			340
		X	X	X		X	350
		X	X	X	X		360
		X	X	X	X	X	370
	X						400

	X		X				500

	X	X					600

	X	X	X				700

"X" INDICATES A CONNECTION TO W46.
W46 IS THE SOURCE JUMPER FOR THE VECTOR ADDRESS
JUMPERS ARE DAISY CHAINED.

Table 4 DPV11-DA Registers

Register Name	Mnemonic	Address	Comments
Receive Control and Status	RXCSR	16xxx0	Word or byte* addressable. Read/write.
Receive Data and Status	RDSR**	16xxx2	Word or byte* addressable. Read-only.
Parameter Control Sync/Address	PCSAR**	16xxx2	Word or byte addressable. Write-only.†
Parameter Control and Character Length	PCSCR‡	16xxx4	Word or byte addressable. Read/write.
Transmit Data and Status	TDSR**	16xxx6	Word or byte addressable. Read/write.

*Reading either byte of these registers, clears data and certain status bits in other bytes. See Paragraphs 3.3.1 and 3.3.2.
**Registers contained within the USYNRT.
†It is not possible to do bit set or bit clear instructions on this register.
‡The high byte of this register is internal to the USYNRT.

Table 5 Receive Control and Status Register (RXCSR) Bit Assignments

Bit	Name	Description
15	Data Set Change (DSCNG)	This bit is set when a transition occurs on any of the following modem control lines: Clear to Send Data Mode Receiver Ready Incoming Call Transition detectors for each of these four lines can be disabled by removing the associated jumper. Data Set Change is cleared by reading either byte of the RXCSR or by Device Reset or Bus INIT.

Bit	Name	Description
		Data Set Change causes a receive interrupt if DSITEN (bit 5) and RXITEN (bit 6) are both set.
14	Incoming Call (IC)	This bit reflects the state of the modem Incoming Call line. Any transition of this bit causes Data Set Change bit (bit 15) to be asserted unless the Incoming Call line is disabled by removing its jumper. This bit is read-only and cannot be cleared by software.
13	Clear to Send (CTS)	This bit reflects the state of the Clear to Send line of the modem. Any transition of this line causes Data Set Change (bit 15) to be set unless the jumper enabling the Clear to Send signal is removed. Clear to Send is a program read-only bit and cannot be cleared by software.
12	Receiver Ready (RR)	This bit is a direct reflection of modem Receiver Ready lead. It indicates that the modem is receiving a carrier signal. For external maintenance loopback, this signal must be high. If the line is open, RR is pulled high by the circuitry. Any transition of this bit causes Data Set Change (bit 15) to be asserted unless the jumper enabling the Receiver Ready signal is removed. Receiver Ready is a read-only bit and cannot be cleared by software.
11	Receiver Active (RXACT)	This bit is set when the USYNRT presents the first character of a message to the DPV11. It remains set until the receive data path of the USYNRT becomes idle. Receiver Active is cleared by any of the following conditions: a terminating control character is received in bit-oriented protocol mode; an off transition of Receiver Enable (RXENA) occurs; or Device Reset or Bus INIT is issued.

Bit	Name	Description
		Receiver Active is a read-only bit which reflects the state of the USYNRT output pin 5.
10	Receiver Status Ready (RSTARY)	This bit indicates the availability of status information in the upper byte of the receive data and status register (RDSR). It is set when any of the following bits of the RDSR are set: Receiver End of Message (REOM); Receiver Overrun (RCV OVRUN); Receiver Abort or Go Ahead (RABORT); Error Check (ERRCHK) if VRC is selected. Receiver Status is cleared by any of the following conditions: reading either byte of the RDSR; clearing Receiver Enable (bit 4 of RXCSR); Device Reset, or Bus Init. When set, Receiver Status Ready causes a receive interrupt if Receive Interrupt Enable (bit 6) is also set. Receiver Status Ready is a read-only bit which reflects the state of USYNRT pin 7.
9	Data Mode (DM) (Data Set Ready)	This bit reflects the state of the Data Mode signal from the modem. When this bit is set it indicates that the modem is powered on and not in test, talk or dial mode. Any transition of this bit causes the Data Set Change bit (bit 15) to be asserted unless the Data Mode jumper has been removed. Data Mode is a read-only bit and cannot be cleared by software.
8	Sync or Flag Detect (SFD)	This bit is set for one clock time when a flag character is detected with bit-oriented protocols, or a sync character is detected with character-oriented protocols. SFD is a read-only bit which reflects the state of USYNRT pin 4.

Bit	Name	Description
7	Receive Data Ready (RDATRY)	This bit indicates that the USYNRT has assembled a data character and is ready to present it to the processor. If this bit becomes set while Receiver Interrupt Enable (bit 6) is set, a receive interrupt request will result. Receive Data Ready is reset when either byte of RDSR is read, Receiver Enable (bit 4) is cleared, or Device Reset or Bus INIT is issued. RDATRY is a read-only bit which reflects the state of USYNRT pin 6.
6	Receiver Interrupt Enable (RXITEN)	When set, this bit allows interrupt requests to be made to the receiver vector whenever RDATRY (bit 7) becomes set. The conditions which cause the interrupt request are the assertion of Receive Data Ready (bit 7), Receive Status Ready (bit 10), or Data Set Change (bit 15) if DSITEN (bit 5) is also set. RXITEN is a program read/write bit and is cleared by Device Reset or Bus INIT.
5	Data Set Interrupt Enable (DSITEN)	This bit, when set along with RXITEN, allows interrupt requests to be made to the receiver vector whenever Data Set Change (bit 15) becomes set. DSITEN is a program read/write bit and is cleared by Device Reset or Bus INIT.
4	Receiver Enable (RXENA)	This bit controls the operation of the receive section of the USYNRT. When this bit is set, the receive section of the USYNRT is enabled. When it is reset the receive section is disabled. In addition to disabling the receive section of the USYNRT, resetting bit 4 initializes all but two of the USYNRT receive registers. The two registers not reinitialized are the

Bit	Name	Description
		character length selection buffer and the parameter control register.
3	Local Loopback (LL)	Asserting this bit causes the modem connected to the DPV11 to establish a data loopback test condition. Clearing this bit restores normal modem operation. Local Loopback is program read/write and is cleared by Device Reset or Bus request to Send is program read/write and is cleared by Device Reset or Bus INIT.
2	Request to Send (RTS)	Setting this bit asserts the Request to Send signal at the modem interface. Request to Send is program read/write and is cleared by Device Reset or Bus INIT.
1	Terminal Ready (TR) (Data Terminal Ready)	When set, this bit asserts the Terminal Ready signal to the modem interface. For auto dial and manual call origination, it maintains the established call. For auto answer, it allows handshaking in response to a Ring signal.
0	Select Frequency or Remote Loopback (SF/RL)	This bit can be wire-wrap jumpered to function as either select frequency or remote loopback. When jumpered as select frequency (W3 to W4), setting this bit selects the modem's higher frequency band for transmission to the line and the lower frequency band for reception from the line. The clear condition selects the lower frequency for transmission and the higher frequency for reception. When jumpered for remote loopback (W5 to W3), this bit, when asserted, causes the modem connected to the DPV11 to signal when a remote loopback test condition has been established in the remote modem.

Bit	Name	Description
		SF/RL is program read/write and is cleared by Device Reset or Bus INIT.

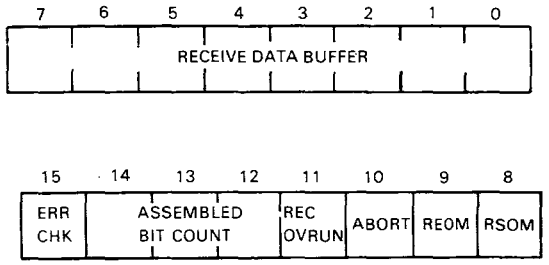


Figure 4 Receive Data and Status Register (RDSR) Format

Table 6 Receive Data and Status Register (RDSR) Bit Assignments

Bit	Name	Description
15	Error Check (ERR CHK)	This bit when set, indicates a possible error. It is used in conjunction with the error detection selection bits of the parameter control sync/address register (bits 8–10) to indicate either an error or an all zeros state of the CRC register. With bit-oriented protocols, ERR CHK indicates that a CRC error has occurred. It is set when the Receive End of Message bit (RDSR bit 9) is set. With character-oriented protocols ERR CHK is asserted with each data character if all zeros are in the CRC register. The processor must then determine if this indicates an error-free message or not. If VRC parity is selected, this bit is set for every character which has a parity error. ERR CHK is cleared by reading the RDSR, clearing RXENA (RXCSR bit 4), Device Reset or Bus INIT.

Bit	Name	Description
14–12	Assembled Bit Count (ABC)	Used only with bit-oriented protocols, these bits represent the number of valid bits in the last character of a message. They are all zeros unless the message ends on an unstated boundary. The bits are encoded to represent valid bits as shown below.

14	13	12	Number of Valid Bits
0	0	0	All bits are valid
0	0	1	One valid bit
0	1	0	Two valid bits
0	1	1	Three valid bits
1	0	0	Four valid bits
1	0	1	Five valid bits
1	1	0	Six valid bits
1	1	1	Seven valid bits

These bits are presented simultaneously with the last bits of data and are cleared by reading the RDSR or by resetting RXENA (bit 4 of RXCSR).

Bit	Name	Description
11	Receiver Overrun (RCV OVRUN)	This bit is used to indicate that an overrun situation has occurred. Overrun exists when the data buffer (bits 0–7 of RDSR) has not been serviced within one character time. As a general rule, the overrun is indicated when the last bit of the current character has been received into the shift register of the USYNRT and the data buffer is not yet available for a new character. Two factors exist which modify this general rule and apply only to bit-oriented protocols. The first factor is the number of bits inserted into the data stream for transparency. For each bit inserted during the formatting of the current character, the controller's maximum response time is increased by one clock cycle.

Bit	Name	Description
		The second factor is the result of termination of the current message. When this occurs, the data of the terminated message which is within the USYNRT is not overrunable. If an attempt is made to displace this data by the reception of a subsequent message, the data of the subsequent message is lost until the data of the prior message has been released.
10	Receiver Abort or Go Ahead (RABORT)	This bit is used only with bit-oriented protocols and indicate that either an abort character or a go-ahead character has been received. This is determined by the Loop Mode bit (PCSAR bit 13). If the Loop Mode bit is clear, RABORT indicates reception of an abort character. If the Loop Mode bit is set, RABORT indicates a go-ahead character has been received. The setting of RABORT causes Receiver Status Ready (bit 10 of RXCSR) to be set. RABORT is reset when the RDSR is read or when Receiver Enable (bit 4 of RXCSR) is reset. The abort character is defined to be seven or more contiguous one bits appearing in the data stream. Reception of this bit pattern when Loop Mode is clear causes the receive section of the USYNRT to stop receiving and set RSTARY (bit 10 of RXCSR). The abort character indicates abnormal termination of the current message. The go-ahead character is defined as a zero bit followed by seven consecutive one bits. This character is recognized as a normal terminating control character when the Loop Mode bit is set. If Loop Mode is cleared this character is interpreted as an abort character.
9	Receiver End of Message (REOM)	This bit is used only with bit-oriented protocols and is asserted if Receiver

Bit	Name	Description
		Active (bit 11 of RXCSR) is set and a message is terminated either normally or abnormally. When REOM becomes set, it sets RSTARY (bit 10 of RXCSR). REOM is cleared when RDSR is read or when Receive Enable (bit 4 of RXCSR) is reset.
8	Receiver Start of Message (RSOM)	Used only with bit-oriented protocols. This bit is presented to the processor along with the first data character of a message and is synchronized to the last received flag character. Setting of RSOM does not set RSTARY (RXCSR bit 10). RSOM is cleared by Device Reset, Bus INIT, resetting Receiver Enable (RXCSR bit 4), or the next transfer into the Receive Data buffer (low byte of RDSR).
7–0	Receive Data Buffer	The low byte of the RDSR is the Receive Data buffer. The serial data input to the USYNRT is assembled and transferred to the low byte of the RDSR for presentation to the processor. When the RDSR receives data, Receive Data Ready (bit 7 of RXCSR) becomes set to indicate that the RDSR has data to be picked up. If this data is not read within one character time, a data overrun occurs. The characters in the Receive Data buffer are right-justified with bit 0 being the least significant bit.

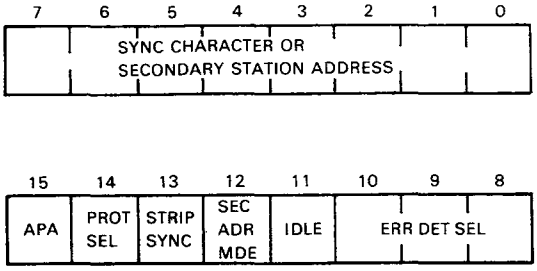


Figure 5 Parameter Control Sync/Address Register (PCSAR) Format

Table 7 Parameter Control Sync/Address Register (PCSAR) Bit Assignments

Bit	Name	Description
15	All Parties Addressed (APA)	This bit is set when automatic recognition of the All Parties Addressed character is desired. The All Parties Addressed character is eight bits of ones with necessary bit stuffing so as not to be confused with the abort character. Recognition of this character is done in the same way as the secondary station address (see bit 12 of this register) except that the broadcast address is essentially hardwired within the receive data path. The logic inspects the address character of each frame for the broadcast address. When the broadcast address is recognized, the USYNRT makes it available and sets Receiver Start of Message (bit 8 of RDSR). If the broadcast address is not recognized, one of two possible actions occurs. 1. If the Secondary Address Select mode bit (bit 12) is set, a test of the secondary station address is made. 2. If bit 12 is not set or the secondary station address is not recognized, the receive section of the USYNRT renews its search for synchronizing control characters.

Bit	Name	Description
14	Protocol Select (PROT SEL)	This bit is used to select between character- and byte count-oriented or bit-oriented protocols. It is set for character- and byte count-oriented protocols and reset for bit-oriented protocols.
13	Strip Sync or Loop Mode (STRIP SYNC)	This bit serves the following two functions. 1. Strip Sync (character-oriented protocols)—In character-oriented protocols, all sync characters after the initial synchronization are deleted from the message and not included in the CRC computation if this bit is set. If it is cleared, all sync characters remain in the message and are included in the CRC computation. 2. Loop Mode (bit-oriented protocols)—With bit-oriented protocols, this bit is used to control the method of termination. If it is set, either a flag or go-ahead character can cause a normal termination of a message. If it is cleared, only a flag character can cause a normal termination.
12	Secondary Address Mode (SEC ADR MDE)	This bit is used with bit-oriented protocols when automatic recognition of the secondary station address is desired. If it is set, the station address of the incoming message is compared with the address stored in the low byte of this register. Only messages prefixed with the correct secondary address are presented to the processor. If the addresses do not compare, the receive section of the USYNRT goes back to searching for flag or go-ahead characters. When SEC ADR MDE is cleared, the receive section of the USYNRT recognizes all incoming messages.
11	Idle Mode Select (IDLE)	This bit is used with both bit- and character-oriented protocols. With bit-oriented protocols, IDLE is used to select the type of control character

Bit	Name	Description
		issued when either Transmit Abort (bit 10 of TDSR) is set or a data underrun error occurs. If IDLE is set, flag characters are issued. If IDLE is clear, abort characters are issued. With character-oriented protocols, IDLE is used to control the method in which initial sync characters are transmitted and the action of the transmit section of the USYNRT when an underrun error occurs. IDLE is cleared to cause sync characters from the low byte of PCSAR to be transmitted. When IDLE is set, the transmit data output is held asserted during an underrun error and at the end of a message.
10–8	Error Detection Selection (ERR DEL SEL)	These bits are used to determine the type of error detection used on received and transmitted messages. In bit-oriented protocols, the selection is independent of character length. In character- and byte count-oriented protocols, CRC error detection is usable only with 8-bit character lengths. The maximum character length for VRC is seven. The bits are encoded as follows.

10	9	8	CRC Polynomial
0	0	0	$x^{16}+x^{12}+x^5+1$ (CRC CCITT) (Both CRC data registers in the transmit and receive sections are set to all ones prior to the computation.)
0	0	1	$x^{16}+x^{12}+x^5+1$ (CRC CCITT) (Both CRC data registers set to all zeros.)
0	1	0	Not used
0	1	1	$x^{16}+x^{15}+x^2+1$ (CRC 16) (Both CRC registers set to all zeros.)

Bit	Name	Description			
10–8	Error Detection Selection (ERR DEL SEL) (Cont)	**10**	**9**	**8**	**CRC Polynomial**
		1	0	0	Odd VRC Parity (A parity bit is attached to each transmitted character.) Should be used only in character-oriented protocols.
		1	0	1	Even VRC parity (Resembles odd VRC except that an even number of bits are generated.)
		1	1	0	Not used.
		1	1	1	All error detection is inhibited.
7–0	Sync Character or Secondary Address	The low byte of PCSAR is used as either the sync character for character-oriented protocols or as the secondary station address for bit-oriented protocols. The bits are right-justified with the least significant bit being bit 0.			

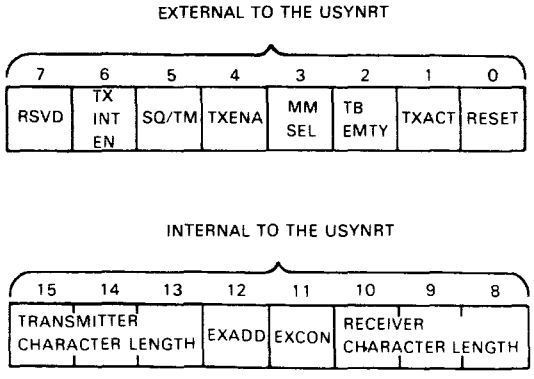


Figure 6 Parameter Control and Character Length Register (PCSCR) Format

Table 8 Parameter Control and Character Length Register (PCSCR) Bit Assignments

Bit	Name	Description
15–13	Transmitter Character Length	These bits can be read or written and are used to determine length of the characters to be transmitted. They are encoded to set up character lengths as follows.

15	14	13	Character Length
0	0	0	Eight bits per character
1	1	1	Seven bits per character
1	1	0	Six bits per character
1	0	1	Five bits per character (bit-oriented protocol only)
1	0	0	Four bits per character (bit-oriented protocol only)
0	1	1	Three bits per character (bit-oriented protocol only)
0	1	0	Two bits per character (bit-oriented protocol only)
0	0	1	One bit per character (bit-oriented protocol only)

These bits can be changed while the transmitter is active, in which case the new character length is assumed at the completion of the current character. This field is set to a character length of eight by Device Reset or Bus INIT. When VRC error detection is selected, the default character length is eight bits plus parity.

Bit	Name	Description
12	Extended Address Field (EXADD)	This bit is used with bit-oriented protocols and affects the address portion of a message in receiver operations. When it is set, each address byte is tested for a one in the least significant bit position. If the least significant bit is zero, the next character is an extension of the address field. If the least significant bit is one, the current character terminates the address field and the next character is a control character. EXADD is not used with Secondary Address Mode (bit 12 of PCSAR). EXADD is read/write and is reset by Device Reset or Bus INIT.
11	Extended Control Field (EXCON)	This bit is used with bit-oriented protocols and affects the control character of a message in receiver operations. When EXCON is set it extends the control field from one 8-bit byte to two 8-bit bytes. EXCON is not used with Secondary Address Mode (bit 12 of PCSAR). EXCON is read/write and is reset by Device Reset or Bus INIT.
10–8	Receiver Character Length	These bits are used to determine the length of the characters to be received. They are encoded to set up character lengths as follows.

10	9	8	Character Length
0	0	0	Eight bits per character
1	1	1	Seven bits per character
1	1	0	Six bits per character
1	0	1	Five bits per character
1	0	0	Four bits per character (bit-oriented protocols only)
0	1	1	Three bits per character (bit-oriented protocols only)

Bit	Name	Description
		10 9 8 Character Length 0 1 0 Two bits per character (bit-oriented protocols only) 0 0 1 One bit per character (bit-oriented protocols only)
7	Reserved	Not used by the DPV11.
6	Transmit Interrupt Enable (TXINTEN)	When set, this bit allows a transmitter interrupt request to be made to the transmitter vector when Transmit Buffer Empty (TBEMTY) is asserted. Transmit Interrupt Enable (TXINTEN) is read/write and is cleared by Device Reset or Bus INIT.
5	Signal Quality or Test Mode (SQ/TM)	This bit can be wire-wrap jumpered to function as either Signal Quality or Test Mode. When jumpered for signal quality (W5 to W6), this bit reflects the state of the signal quality line from the modem. When asserted, it indicates that there is a low probability of errors in the received data. When clear it indicates that there is a high probability of errors in the received data. When jumpered for the test mode (W6 to W7), this bit indicates that the modem has been placed in a test condition when asserted. The modem test condition could be established by asserting Local Loopback (bit 3 of RXCSR), Remote Loopback (bit 0 of RXCSR) or other means external to the DPV11. When SQ/TM is clear, it indicates that the modem is not in test mode and is available for normal operation. SQ/TM is program read-only and cannot be cleared by software.

Bit	Name	Description
4	Transmitter Enable (TXENA)	This bit must be set to initiate the transmission of data or control information. When this bit is cleared, the transmitter will revert back to the mark state once all indicated sequences have been completed. TXENA should be cleared after the last data character has been loaded into the transmit data and status register (TDSR). Transmit End of Message (bit 9 of TDSR) should be asserted when TXENA is reset (if it is to be asserted at all), and remain asserted until the transmitter enters the idle mode. TXENA is connected directly to USYNRT pin 37. It is a read/write bit and is reset by Device Reset or Bus INIT.
3	Maintenance Mode Select (MM SEL)	When this bit is asserted, it causes the USYNRT's serial output to be internally connected to the USYNRT's serial input. The serial send data output line from the interface is asserted and the receive data serial input is disabled. Send timing and receive timing to the USYNRT are disabled and replaced with a clock signal generated on the interface. The clock rate is either 49.152K b/s or 1.9661K b/s depending on the position of a jumper on the interface board. Maintenance mode allows diagnostics to run in loopback without disconnecting the modem cable. MM SEL is a read/write bit and is cleared by Device Reset or Bus INIT. When it is cleared, the interface is set for normal operation.
2	Transmitter Buffer Empty (TBEMTY)	This bit is asserted when the transmit data and status register (TDSR) is available for new data or control information. It is also set after a Device Reset or Bus INIT.

Bit	Name	Description
		The TDSR should be loaded only in response to TBEMTY being set. When the TDSR is written into, TBEMTY is cleared. If TBEMTY becomes set while Transmit Interrupt Enable (bit 6 of PCSCR) is set, a transmit interrupt request results. TBEMTY reflects the state of USYNRT pin 35.
1	Transmitter Active (TXACT)	This bit indicates the state of the transmit section of the USYNRT. It becomes set when the first character of data or control information is transmitted. TXACT is cleared when the transmitter has nothing to send or when Device Reset or Bus INIT is issued. TXACT reflects the state of USYNRT pin 34.
0	Device Reset (RESET)	When a one is written to this bit all components of the interface are initialized. It performs the same function as Bus INIT with respect to this interface. Modem Status (Data Mode, Clear to Send, Receiver Ready, Incoming Call, Signal Quality or Test Mode) is not affected. RESET is write-only; it cannot be read by software.

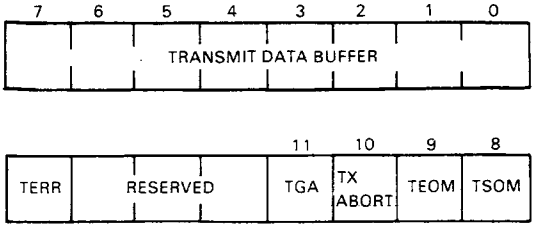


Figure 7 Transmit Data and Status Register (TDSR) Format

Table 9 Transmit Data and Status Register (TDSR) Bit Assignments

Bit	Name	Description
15	Transmitter Error (TERR)	This is a read-only bit which becomes asserted when the Transmitter Buffer Empty (TBEMTY) indication has not been serviced for more than one character time. When TERR occurs in bit-oriented protocols, the transmit section of the USYNRT generates an abort or flag character based on the state of the IDLE bit (PCSAR bit 11). If IDLE is set, a flag character is sent. If it is reset, an abort character is sent. When TERR occurs in character-oriented protocols, the state of the IDLE bit again determines the result. If IDLE is set, the transmit serial output is held in the MARK condition. If it is cleared, a sync character is transmitted. TERR is cleared when TSOM (TDSR bit 8) becomes set or by Device Reset or Bus INIT. Clearing Transmitter Enable (PCSCR bit 4) does not clear TERR and TERR is not set with Transmit End of Message.
14–12	Reserved	Not used by the DPV11.
11	Transmit Go Ahead (TGA)	This bit, when asserted, modifies the bit pattern of the control character initiated by either Transmit Start of Message (TSOM) or Transmit End of Message (TEOM). TSOM or TEOM normally causes a flag character to be sent. If TGA is set, a go-ahead character is sent in place of the flag character. TGA is only used with bit-oriented protocols.
10	Transmit Abort (TXABORT)	This bit is used only with bit-oriented protocols to abnormally terminate a message or to transmit filler information used to establish data link timing.

Table 9 Transmit Data and Status Register (TDSR) Bit Assignments (Cont)

Bit	Name	Description
		When TXABORT is asserted, the transmitter automatically transmits either flag or abort characters depending on the state of the IDLE mode bit. If IDLE is cleared, abort characters are sent. If IDLE is set, flag characters are sent.
9	Transmit End of Message (TEOM)	This control bit is used to normally terminate a message in bit-oriented protocol. It also terminates a message in character-oriented protocols when CRC error detection is used. As a secondary function, it is used in conjunction with the Transmit Start of Message (TSOM) bit to transmit a SPACE SEQUENCE. Refer to the TSOM bit description (bit 8 of this register) for information regarding this sequence. With bit-oriented protocols, asserting this bit causes the CRC information to be transmitted, if CRC is enabled, followed by flag or go-ahead characters depending on the state of the Transmit Go Ahead (TGA) bit. See bit 11 of this register. With character-oriented protocols, asserting this bit causes CRC information, if CRC is enabled, to be transmitted followed by either sync characters or a MARK condition depending on the state of the IDLE bit. If IDLE is cleared, sync characters are transmitted. The character following the CRC information is repeated until the transmitter is disabled or the TEOM bit is cleared. A subsequent message may be initiated while the transmit section of the USYNRT is active. This is accomplished by clearing the TEOM bit and supplying new message data without setting the Transmit Start of Message bit. However, the CRC character for the prior message must have completed transmission.

Bit	Name	Description
8	Transmit Start of Message (TSOM)	This bit is used with either bit- or character-oriented protocols. As long as it remains asserted, flag characters (bit-oriented protocols) or sync characters (character-oriented protocols) are transmitted. With bit-oriented protocols, a space sequence (byte mode only) of 16 zero bits can be transmitted by asserting TSOM and TEOM simultaneously provided the transmitter is in the idle state and Transmit Enable is cleared. This should not be done during the transfer of data, and must only be done in byte mode. **NOTE** **When using the special space sequence function, all registers internal to the USYNRT must be written in byte mode.** Normally at the completion of each sync, flag, go-ahead or Abort character, the TBEMTY indication is asserted. This allows the software to count the number of transmitted characters. In certain applications, the software may elect to ignore the service of the Transmitter Buffer Empty (TBEMTY) indication. Normally during data transfers, this would cause a transmit data late error. The TSOM bit asserted suppresses this error and provides the necessary synchronization to automatically transmit another flag, go-ahead or sync character.
7–0	Transmit Data Buffer	Data from the processor to be transmitted on the serial output line is loaded into this byte of the TDSR when Transmitter Buffer Empty (TBEMTY) is asserted. If the transmitter buffer is not loaded within one character time, an underrun error occurs. The characters are right-justified, with bit 0 being the least significant bit.

DATA TRANSFERS

A discussion on receive and transmit data transfers as they relate to system software is addressed below.

Receive Data

Serial data to be presented to the DPV11-DA from the modem enters the receiver circuit and is presented to the USYNRT. Recognition by the USYNRT of a control character initiates the transfer. When a transfer has been initiated, a character is assembled by the USYNRT and then placed in the low byte of the receive data and status register (RDSR) when it is available. If the RDSR is not available, the transfer is delayed until the previous character is serviced. This must take place before the next character is fully assembled or an overrun error exists. Refer to the description of bit 11 in Table 6 for more details on the Receiver Overrun.

Servicing the RDSR is the responsibility of the system software in response to the Receiver Data Ready (RDATRY) signal. This signal is asserted when a character has been transferred to the RDSR. The setting of the RDATRY would also create a receive interrupt request if Receive Interrupt Enable (RXITEN) is set. The software's response to RDATRY is to read the contents of the RDSR. At the completion of the operation, the new information is loaded into the RDSR and RDATRY is reasserted. This operation continues until terminated by some control character. The upper byte of the RDSR contains status and error indications which the software can also read.

The DPV11-DA will also handle data in bit-, byte-count- or character-oriented protocols.

With bit-oriented protocol, only flag characters are used to initiate the transfer of the message. Information inserted into the data stream for transparency or control is deleted before it is presented to the RDSR. This means that only data characters are available to the software. The first two characters of every message or frame are defined to be 8-bit characters and the USYNRT will handle them as such regardless of the programmed character length. All subsequent data is formatted in the selected character length. When CRC error detection is selected, the received CRC check characters are not presented to the software, but the error indication will be presented if an error has been detected.

If the secondary address mode is implemented, the first received data character must be the selected address. If this is not the case, the

USYNRT will renew its search for flag or go-ahead characters. Refer to the description of bit 12 of the PCSAR in Table 7.

With byte count or character-oriented protocols, two consecutive sync characters are required to synchronize the data transfer. The sync characters used in the message must be the same as the sync character loaded by the software into the low byte of the parameter control sync/address register. If leading sync characters subsequent to the initial two syncs are to be deleted from the data stream, the Strip Sync bit (bit 13) must alos be set in the upper byte of the PCSAR. The character length of the data to be received should also be set in bits 8, 9, and 10 of the parameter control and character length register (PCSCR). Sync characters and data must have the same character length and only characters of the selected length will be presented to the receive buffer. Sync characters following the initial two will be presented to the buffer and included in the CRC computation unless the Strip Sync bit is set. If vertical redundancy check (VRC) parity checking is selected, the parity bit itself is deleted from the character before it is presented to the buffer.

Transmit Data

System software loads information to be transmitted to the modem into the transmit data and status register. This does not ordinarily include error detection or control character information. Loading of the TDSR occurs in response to the Transmitter Buffer Empty signal from the USYNRT. The character length is of information to be transmitted is established by the software when it loads the transmit character length register (bits 13, 14, and 15 of the PCSCR). The default length of eight is assigned when the transmit character length register equals zero. The length of the characters presented to the TDSR should not exceed the assigned character length. When the information in the TDSR is transmitted, the TBEMTY signal is again asserted to request another character. The setting of TBEMTY also causes a transmit interrupt request if Transmit Interrupt Enable is set.

Byte count- or character-oriented protocols require the transmission of synchronizing information normally referrd to as sync characters. The sync characters can then be transmitted when Transmit Start of Message (TDSR bit 8) is set. This happens in one of two ways depending on the state of the IDLE bit (PCSAR bit 11). When the IDLE bit is cleared, the sync character is taken directly from the the common sync register (PCSAR bits 7-0). The sync register would have been previously loaded by the software. If the IDLE bit is set, the sync charac-

ter must be loaded into the TDSR by the software when it is to be transmitted. If multiple sync characters are to be transmitted, the TDSR must be loaded with only the first one in the sequence. This character will be transmitted until data information is loaded into the TDSR. The TBEMTY signal is asserted at the end of each sync character but the TSOM signal allows it to be ignored without causing a data late error. With byte-oriented protocols, the USYNRT automatically generates control characters as initiated by the software and inserts necessary information into the data stream to maintain transperency.

Interrupt Vectors

The DPV11-DA generates two vector addresses, one for receive data and modem control and the other for transmit data.

The receive and modem control interrupt has priority over the transmit interrupt and is enabled by seeting bit 6 (RXITEN) of the receiver control and status register (RXCSR).

If bit 6 of the RXCSR is set, a receiver interrupt may occur when any one of the following signals is asserted.

- Receive Data Ready (RDATRY)
- Receive Status Ready (RSTARY)
- Data Set Change (DAT SET CH)

The signal DAT SET CH causes an interrupt if bit 5 (DSITEN) of the RXCSR is also set. It is possible that a data set change interrupt could be pending while a receiver interrupt is being serviced, or the opposite could be true. In either case, the hardware ensures that both interrupt requests are recognized.

NOTE

The modem status change circuit interprets any pulse of two microseconds or greater duration as a data set change. This ensures that all legitimate transitions of modem status will be detected. However, on a poor line, noise may be defined as a data set change. Software written for the DPV11-DA must account for this possibility.

A transmitter interrupt request occurs if Transmit Interrupt Enable (TXINTEN) is set when Transmit Buffer Empty (TBEMTY) becomes asserted.

RLV12

RLV12 DISK CONTROLLER

INTRODUCTION

The RLV12 disk controller interfaces RL02 and RL01 disk drives to any quad-or hex-size backplane that uses 16-, 18-, or 22-bit LSI-11 bus. One RLV12 controls up to four disk drives. The RLV12 consists of one quad-size module, a BC80M cable, a drive terminator, and drive identification hardware.

The RL01 and the RL02 are random-access, mass storage subsystems that store data in fixed-length blocks on a preformatted disk cartridge. Each RL01 can store 5.24 million bytes, and each RL02 can store 10.48 million bytes. The drives are 26.67 cm (10.5 in) high, self-cooling rack-mountable units and come complete with a power supply. Option RLV12-AK includes one RL01 drive, and option RLV22-AK includes one RL02 drive.

The RLV12 transfers data to and from the LSI-11 bus using Direct Memory Access (DMA) transactions. This allows data transfers to occur without processor intervention.

FEATURES

- Single quad-size module; needs no C-D connections
- Supports DMA data transfers in 16-, 18-, or 22-bit addressing modes
- Software-compatible with RLV11 controller (16-, or 18-bit modes only)
- Supports 22-bit addressing on an LSI-11 bus
- Controls from one to four RL01 and RL02 disk drives
- Memory parity error abort feature for use with memories that have a parity option

SPECIFICATIONS

RLV12 Disk Controller

Identification	M8061
Size	Quad-height: 26.56 cm × 1.27 cm × 22.70 cm (10.45 in × 0.5 in × 8.94 in)
Power requirements	+5 Vdc ± 5% at 5.0 A and +12 Vdc ± 5% at 0.1 A

RLV12

Bus loads	
ac	3
dc	1
Addressing modes	16-, 18-, or 22-bit (determined by the user)
Max. config. for 22-bit address mode	H9275-A or similar backplane that supports 22-bit addressing, with memory capable of 22-bit addresses, such as the MSV11-L or the MSV11-P.
Limitations	The RLV12 will not fit in the dual-height LSI-11 mini-series H9281 backplane.
Drives per controller	Up to four RL01 and RL02 drives in any combination
LSI-11 addressable registers	8 (5 are used; 3 are not used)

Addressing Mode	**Base Device Address**
16-bit	17440_8
18-bit	774400_8
22-bit	17774400_8

Device interrupt vector	000160_8, jumper-selectable
Data transfer rates	4.9μs/word (avg) drive to controller, controller to memory 13.9μs/word (peak) drive to controller 2.0μs/word (peak) controller to memory
Error detection capability	Cyclic redundancy check (CRC) on data and headers. Memory parity error abort for use with memories that have parity checking.
Max. cable length (controller to last drive)	30 m(100ft)

RLV12

Environment

Temperature, operating	5°C to 60°C (41°F to 140°F)
Temperature, storage	−40°C to 66°C (−40°F to 150°F)
Relative humidity, operating and storage	10% to 95% noncondensing

RL01/RL02 Disk Drives

Medium	Magnetic disk cartridge
Recording surfaces	2 data surfaces
Magnetic heads	2 read/write heads

Recording Capacity (formatted)

	RL01	RL02
Cylinders per cartridge	256	512
Tracks per cylinder	2	2
Tracks per cartridge	512	1024
Sectors per track	40	40
Bytes per sector	256	256
Bytes per track	10,240	10,240
Bytes per cylinder	20,480	20,480
Bytes per cartridge	5.24 M	10.48 M
Recording method	Modified frequency modulation	

Performance

Transfer rate	40-sector (16-bit data words): 4.9μs/word (avg) drive to controller, controller to memory; 3.9μs/word (peak) drive to controller
Head positioning time	55 ms (avg); 17 ms (one track); 100 ms (max)
Revolution latency	12.5 ms (avg)

Operating Environment

Temperature range	10°C to 40°C (50oF to 114°F)at sea level
Relative humidity	10% to 90%, noncondensing
Wet-bulb temperature	28°C (82°F) max

RLV12

Altitude	Up to 2400 m (8000 ft) at max temperature of 36°C (96°F)
Heat dissipation	150 W (546 btu/hr)

Power

Drive	Single-phase

Starting current

5 A (rms) max, 120 V, 47/63 Hz;
2.5 A (rms) max, 240 V, Hz

Mechanical drive

Size	48 cm × 63.4 cm × 27 cm (19 in × 25 in × 10.5 in)
Weight	33.75 kg (75 lb)
Mounting	The drive mounts on slides in a standard 48.26 cm (19 in) cabinet (provided). Recommended max height from floor is 18.9 cm (48 in).
Cartridge	Embedded servo. Top loading cartridge with two data surfaces.

Standard length cables

Power cord	2.74 m (9ft)
Controller to first drive	1.83 m (6 ft)
Drive-to-drive	3.05 m (10 ft)

Optional drive cables

Cable	Part No.	Length
BC20J-20	7012122-20	6 m (20 ft)
BC20J-40	7012122-40	12 m (40 ft)
BC20J-60	7012122-60	18 m (60 ft)

NOTE

Total length of the cable(s) from controller to the last drive must not exceed 30 m (100 ft).

RLV12

Device Address Selection

Software control of the RLV12 is performed by four or five device registers: CSR, BAR, DAR, MPR, and BAE. Four registers are used for 16- or 18-bit addressing; five registers are used for 22-bit addressing. The bus address extension register (BAE) is added for upper address but selection for 22-bit addressing. The usual device starting address is as follows:

Addressing Modes	Starting Address (Octal)
16-bit	174400
18-bit	774400*
22-bit	17774400

* Factory configuration

NOTE

For 22-bit addressing, bit A3 is not decoded in the starting address.

The first register, the CSR, is assigned to the starting address, and the other registers are assigned to the next sequential address, as shown in Table 1.

The device starting address is selected by jumpers for bits 3-12. These jumpers are shown in Figure 1. A jumper from the selected bit to ground (M22) decodes a 1; no jumper decodes a 0; and a jumper to 5 V (M11) decodes an X (don't care) condition. Figure 2 shows the RLV12 device starting address format.

Bus Selection

The RLV12 module can be used on 16-, 18-, or 22-bit LSI-11 buses. When sent from the factory, the module operates on a 16-, 18-bit buses. To enable the module to operate on a 22-bit bus, install jumper M1 to M2, shown in Figure 1. When installed, the jumper enables bank select 7 (BBS7) to be determined by the upper address bits (13-21). When the jumper is removedthe RLV12 has an 18-bit mode bank select 7 and can replace an existing RLV11 or RLV21 as the disk controller for RL01 and RL02 disk drives.

Interrupt Vector

The interrupt vector has a range of 0 to 774. The interrupt vector is preset at the factory to 160. The user may select another vector by

changing the jumpers for bits V2-V8, as illustrated in Figure 3. A connection to VEC to BUS H (M3, shown in Figure 1) generates a 1 for that bit; no connection generates a 0.

Interrupt Request Level

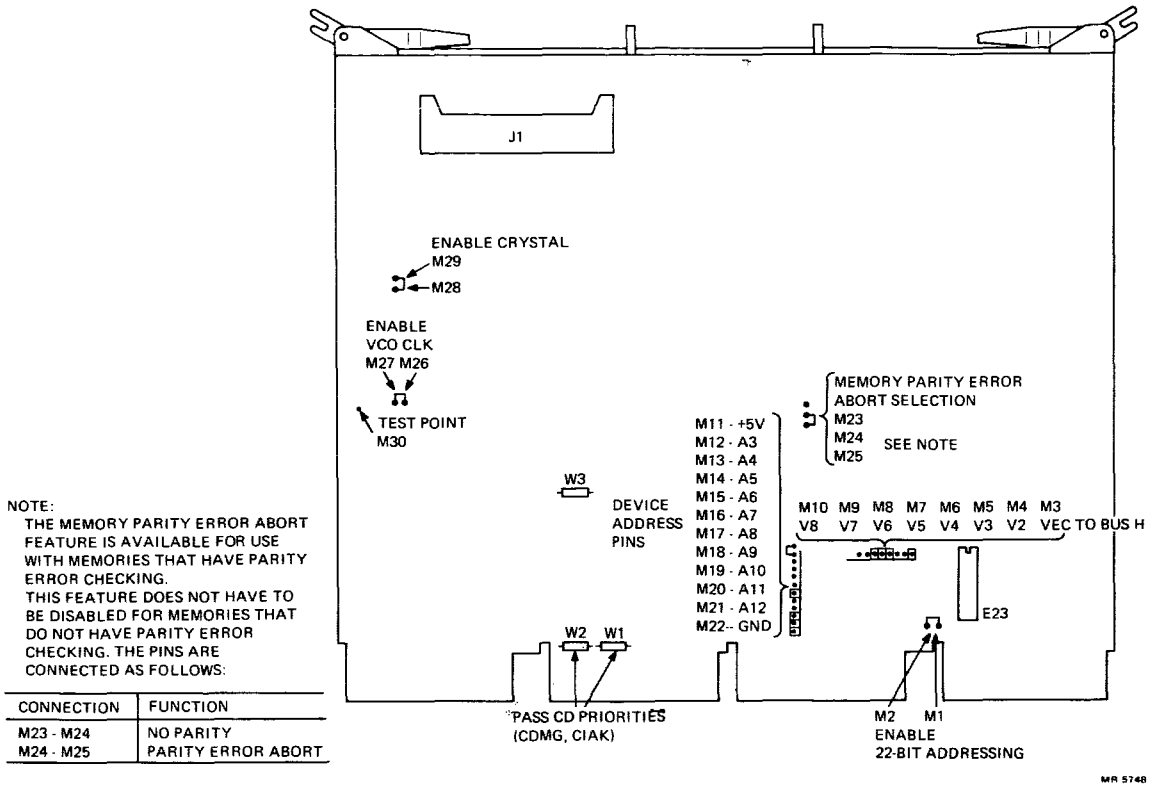
The RLV12 interrupts a priority level 4 determined by the interrupt chip E23, a DC003.

Table 1 Address Selection

Device Address	16-Bit Addressing	18-Bit Addressing*	22-Bit Addressing
Starting Address Range	160000–177770	760000–777770	17760000–17777760
Starting Address	174400	774400	17774400
No. of Registers	4	4	8 (5 are used; 3 are not)
Registers Used	CSR (174400) BAR (174402) DAR (174404) MPR (174406)	CSR (774400) BAR (774402) DAR (774404) MPR (774406)	CSR (17774400) BAR (17774402) DAR (17774404) MPR (17774406) BAE (17774410)
Jumpers Used	Tie M22 ("1") to M17, M20, and M21	Tie M22 ("1") to M17, M20, and M21	Tie M22 ("1") to M17, M20, and M21; Tie M11 ("X") to M12
Interrupt Vector			
Vector Range	0–774	0–774	0–774
Standard Vector	160	160	160
Jumpers Used	Tie M3 ("1") to M6, M7, and M8	Tie M3 ("1") to M6, M7, and M8	Tie M3 ("1") to M6, M7, and M8

*Factory Configuration

RLV12



NOTE:
THE MEMORY PARITY ERROR ABORT FEATURE IS AVAILABLE FOR USE WITH MEMORIES THAT HAVE PARITY ERROR CHECKING.
THIS FEATURE DOES NOT HAVE TO BE DISABLED FOR MEMORIES THAT DO NOT HAVE PARITY ERROR CHECKING. THE PINS ARE CONNECTED AS FOLLOWS:

CONNECTION	FUNCTION
M23 - M24	NO PARITY
M24 - M25	PARITY ERROR ABORT

Figure 1 RLV12 Jumper Locations

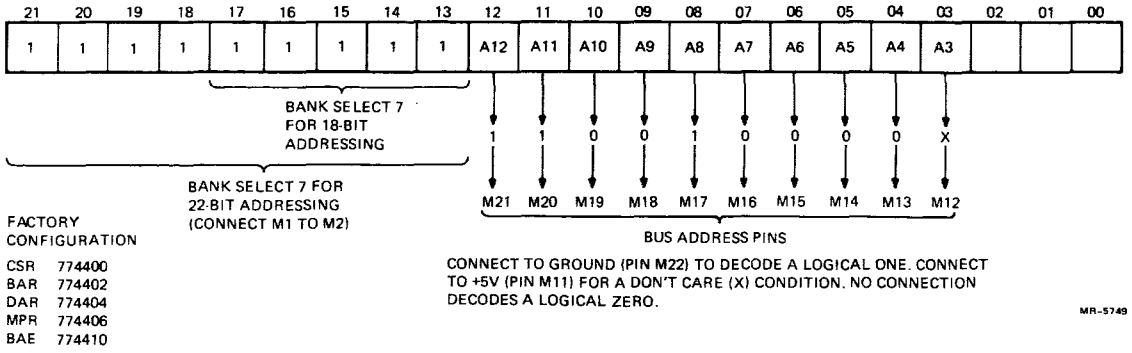


Figure 2 RLV12 Device Address Format

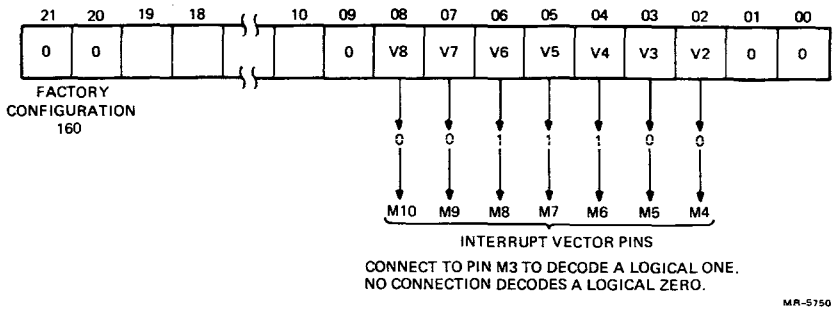


Figure 3 RLV12 Interrupt Vector Format

Memory Parity Error Abort Feature

When reading the system's optional memory with parity error detection, a parity error will set OPI and NXM of the CSR. This is a unique error condition that aborts the current command to the RLV12. This error abort feature is possible only with memories that have parity data bits.

The RLV12 is sent from the factory with the memory parity error abort feature enabled. To disable the parity error abort, remove the jumper between pins M24 and M25 and install a jumper between pins M23 and M24. (See Figure 1.) This feature does not have to be disabled for non-parity memories, as parity errors are not generated. Parity error abort uses data bits 16 and 17.

Jumpers That Remain Installed

The module has two jumpers, W1 and W2, that enable priority signals to pass through the module. The module has these jumpers installed, and they should be left in.

Jumper	Signal
W1	CIAKI to CIAKO
W2	CDMGI to CDMGO

One jumper, the W3, enables the word count register to automatically increment during a DMA operation. This jumper is used for factory testing and should be left in.

Two jumpers on the module disable the crystal oscillator and the voltage-controlled oscillator (VCO) during factory testing. These jumpers should be left in.

Jumper	Oscillator
M26-M27	VCO
M28-M29	Crystal

INSTALLATION

The RLV12 can be installed in any quad LSI-11 bus slot. The controller's priority level is based on its electrical distance from the processor module. Use the following procedure to install the module.

1. Examine the module to make sure that the base address jumpers and vector address jumpers are set correctly.
2. Check jumpers M1 and M2 for enabling the correct bank select 7 (BBS7) for the 18- or 22-bit LSI-11 bus.
3. If desired, disable the memory parity error abort feature. This feature can only be used with system memories that have parity options, but this feature does not have to be disabled for non-parity memories.
4. Insert the BC80M controller cable (or equivalent) into J1 on the M8061 as shown in Figure 4.
5. Insert the M8061 in the selected slot in the LSI-11 bus.
6. Attach the ground strap on the cable to the metal cabinet chassis.
7. Connect the other end to the BC80M cable to the back of the first disk drive.
8. Continue with the disk installation. Refer to the RL01/RL02 Disk Subsystem User Guide (EK-RL012-UG).

Acceptance Testing

The RLV12 controller is tested by running the RLV12 diskless diagnostic test, and, if a drive is attached, by running the diagnostics that exercise the RL01 and RL02 disk drive. The diskless diagnostic should be run first. The RLV12 diagnostics are available on different media. Contact your local DIGITAL sales office for the types of media available and their part numbers.

RLV12

Run the XXDP + diagnostics in the following order:

1. CVRLB RLV12 Diskless Diagnostic (16-, 18-, or 22-bit mode)

NOTE

When the RLV12 is configured for 16- or 18-bit addressing, the RLV11 diskless diagnostic (CVRLA) is compatable with the RLV12 diskless diagnostic and checks the same logic.

2. CZRLG Controller Test, Part 1
3. CZRLG Controller Test, Part 1
4. CZRLH Controller Test, Part 2
5. CZRLI Drive Test, Part 1
6. CZRLJ Drive Test, Part 2
7. CZRLN Drive Test, Part 3
8. CZRLK Performance Exerciser
9. CZRLL Compatibility Test
10. CZRLM Bad Sector File Utility

NOTE

The bad sector file Utility is not a diagnostic test. It is used by field service to examine the bad sector file on the disk and to write entries into that file.

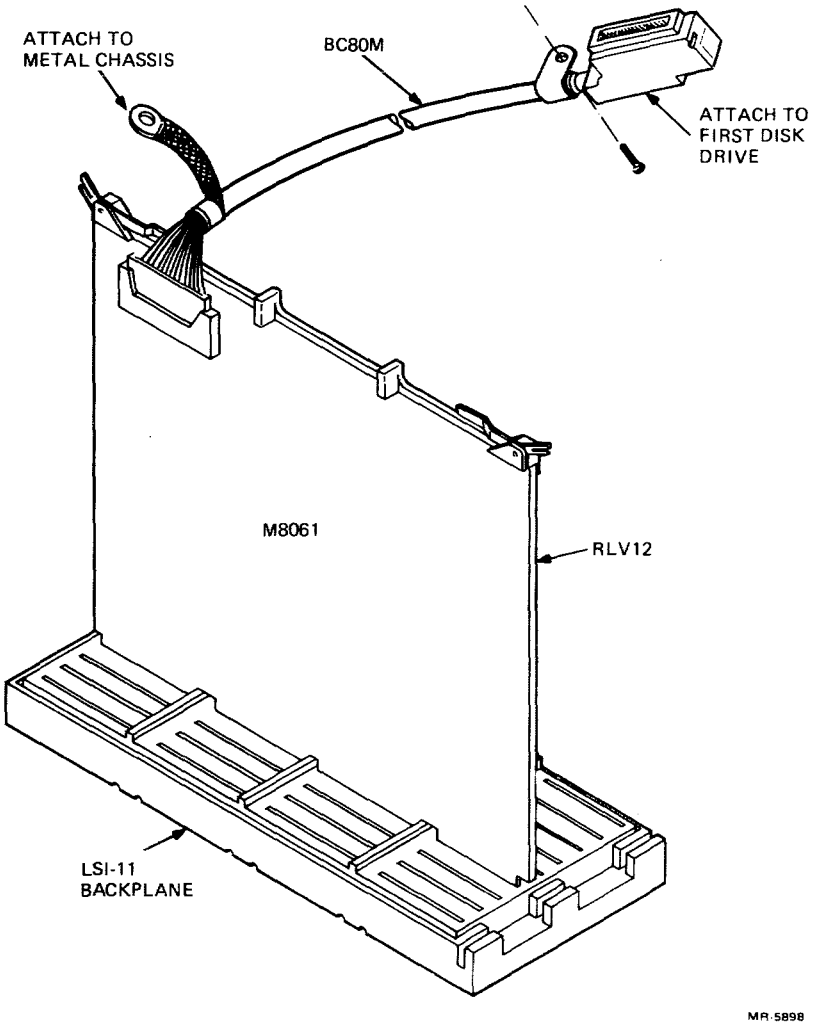
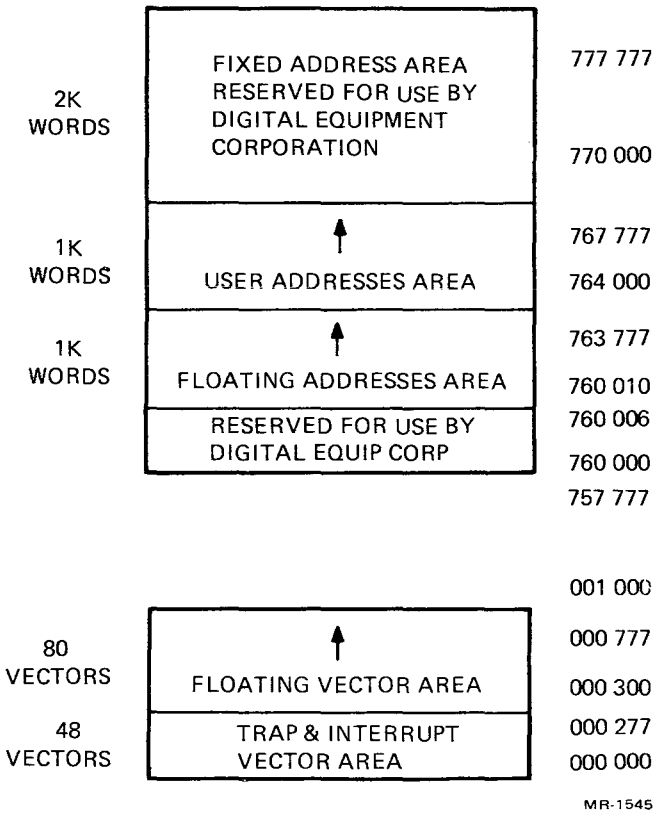


Figure 4 RLV12 Installation

APPENDIX A

ASSIGNMENT OF ADDRESSES AND VECTORS

ADDRESS MAP



FLOATING VECTORS

The conventions for the assignments of floating vectors for modules on the LSI-11 bus will adhere to those established for UNIBUS devices. UNIBUS devices are used to explain the priority ranking for floating vectors and are included in the subsequent table of trap and interrupt vectors as a guide to the user.

The floating vector convention used for communications and for devices that interface with the PDP-11 series of products assigns vectors sequentially starting at 300 and proceeding upward to 777. (Some LSI-11 bus modules, such as the DLV11 and DRV11, have an upper vector limit of 377). The following table shows the sequence for assigning vectors to modules. It can be seen that the first vector address, 300, is

assigned to the first DLV11 in the system. If another DLV11 is used, it would then be assigned vector address 310, etc. When the vector addresses have been assigned to all the DLV11s (up to a maximum of 32), addresses are then assigned consecutively to each unit of the next highest ranked device (DRV11 or DLV11-E, etc.), then to the other devices according to their rank.

Ranking for Floating Vectors
(Start at 300 and proceed upward.)

Rank	UNIBUS	LSI-11 Bus
1	DC11	
2	KL11, DL11-A, -B	DLV11, -F, -J
3	DP11	
4	DM11-A	
5	DN11	
6	DM11-BB	
7	DR11-A	DRV11-B
8	DR11-C	DRV11
9	PA611 Reader	
10	PA611 Punch	
11	DT11	
12	DX11	
13	DL11-C, -D, -E	DLV11-E
14	DJ11	
15	DH11	
16	GT40	
17	LPS11	
18	DQ11	
19	KW11-W	KWV11-A, C
20	DU11	DUV11

INTERRUPT AND TRAP VECTORS

Vector	UNIBUS	LSI-11 Bus
000	DEC reserved	DEC reserved
004	CPU errors	Bus time-out and illegal in-
.		structions (e.g., JMP R0)
.		(odd address and stack
.		overflow traps not

APPENDIX A

INTERRUPT AND TRAP VECTORS (Cont)

Vector	UNIBUS	LSI-11 Bus
.		implemented on LSI-11)
010	Illegal and reserved	Illegal and reserved
.	instructions	instructions
014	BPT, breakpoint trap	BPT instruction and T bit
020	IOT, input/output trap	IOT instruction
024	Power-fail	Power-fail
030	EMT, emulator trap	EMT instruction
034	TRAP instruction	TRAP instruction
040	System software	
044	System software	
050	System software	
054	System software	
060	Console terminal,	Console terminal, input
.	keyboard/reader	
064	Console terminal,	Console terminal, output
.	printer/punch	
070	PC11, paper tape reader	
074	PC11, paper tape punch	
100	KW11-L, line clock	External event line interrupt
104	KW11-P, programmable clock	
110		
114	Memory system errors	
120	XY plotter	
124	DR11-B DMA interface;	DRV11-B
.	(DA11-B)	
130	AD01, A/D subsystem	
134	AFC11, analog subsystem	
140	AA11, display	
144	AA11, light pen	
150		
154		
160	RL11	RLV11
164		
170	User reserved	
174	User reserved	
200	LP11/LS11, line printer;	LAV11, LPV11
.	LA180	
204	RS04/RF11, fixed head disk	

APPENDIX A

INTERRUPT AND TRAP VECTORS (Cont)

Vector	UNIBUS	LSI-11 Bus
210	RC11, disk	
214	TC11, DECtape	
220	RK11, disk	RKV11
224	TU16/TM11/TS03, magnetic tape	
230	CD11-CM11-CR11, card reader	
234	UDC11, digital control subsystem	
240	PIRQ, program interrupt request (11/45)	
244	Floating-point error	FIS (optional)
250	Memory management	
254	RP04/RP11 disk pack	
260	TA11, cassette	
264	RX11, floppy disk	RXV11, RXV21
270	User reserved	User reserved
274	User reserved	
300	(Start of floating vectors)	
374		
400		ADV11-A,C
404		
410		
414		
420		IBV11-A
424		
430		
434		
440		KWV11-A, C
444		
450		User reserved
777	(End of floating vectors)	

APPENDIX A

FLOATING ADDRESSES

The conventions for the assignment of floating addresses for modules on the LSI-11 bus are the same as UNIBUS devices. UNIBUS devices are used to explain the ranking sequence.

The floating address convention used for communications and for other devices that interface with the PDP-11 series of products assigns addresses sequentially starting at 760 010 (or 160 010) and proceeds upward to 763 776 (or 163 776). For compatiblity with UNIBUS convention, addresses are expressed as consisting of 18 bits (7XX XXX) rather than 16 bits (1XX XXX).

Floating addresses are assigned in the following sequence:

Rank	UNIBUS Device	LSI-11 Device
1	DJ11	
2	DH11	
3	DQ11	
4	DU11	DUV11
5	DUP11	
6	LK11A	
7	DMC11	
8	DZ11	DZV11
9	KMC11	
10	RL11 (extras)	RLV11 (extras)

DEVICE ADDRESSES

Address	UNIBUS	LSI-11 Bus
777 776	Processor status word (PS)	
777 774	Stack limit	
777 772	Program interrupt request (PIRQ)	
777 770		
.	DIGITAL reserved	
.		
.		
777 720		

APPENDIX A

DEVICE ADDRESSES (Cont.)

Address	UNIBUS	LSI-11 Bus
777 716		
.		
.	CPU Registers	
.		
777 710		
777 707	R7 (PC)	
777 706	R6 (SP)	
777 705	R5	
777 704	R4 — General Registers	
777 703	R3 — General Registers	
777 702	R2 — General Registers	
777 701	R1 — General Registers	
777 700	R0 — General Registers	
777 676		
.		
.	Memory management	
.		
777 600		
777 576		(SR2)
777 574	Memory mgt status register	(SR1)
777 572		(SR0)
777 570	Console switch and display register	
777 566	(XBUF) — Console Terminal	Console Terminal DLV11-A,C
777 564	(XCSR) — Console Terminal	Console Terminal DLV11-A,C
777 562	(RBUF) — Console Terminal	Console Terminal DLV11-A,C
777 560	(RCSR) — Console Terminal	Console Terminal DLV11-A,C
777 556		
777 554		
777 552	PC11/PR11	
777 550		
777 546	KW11-L, DL11-W	(LTC) KPV11 BDV11
777 544		
.		
.	XY11	
.		
777 530		
777 526	Unassigned	

APPENDIX A

DEVICE ADDRESSES (Cont.)

Address	UNIBUS		LSI-11 Bus
777 524			
777 522	Unassigned		BDV11
777 520			
777 516	LA180, LP11		
777 514	LS11, LV11		LAV11, LPV11
777 512			
777 510			
777 506			
.			
.	TA11		
.			
777 500			
777 476			
.			
.	RF11		
.			
777 460			
777 456			
.			
.	RC11		
.			
777 440			
777 436		#8	
777 434		#7	
777 432		#6	
777 430	DT07, bus switch	#5	
777 426		#4	
777 424		#3	
777 422		#2	
777 420		#1	
777 416			
.			
.	RK11		RKV11
.			
777 400			

APPENDIX A

DEVICE ADDRESSES (Cont.)

Address	UNIBUS		LSI-11 Bus
777 376	DC14-D		
.			
.			
.			
777 360			
777 356	TC11		
.			
.			
.			
777 340			
777 336	KE11-A, EAE #2		
.			
.			
.			
777 320			
777 316	KE11-A, EAE #1	arithmetic shift	
777 314		logical shift	
777 312		normalize	
777 310		step count/status register	
777 306		multiply	
777 304		multiplier quotient	
777 302		accumulator	
777 300		divide	
777 276	DIGITAL reserved		
.			
.			
.			
777 200			
777 176	RX11		RXV11
777 174			
777 172			
777 170	RX11		RXV11, RXV21
777 166	CR11, CM11, CD11		
777 164			
777 162			
777 160			

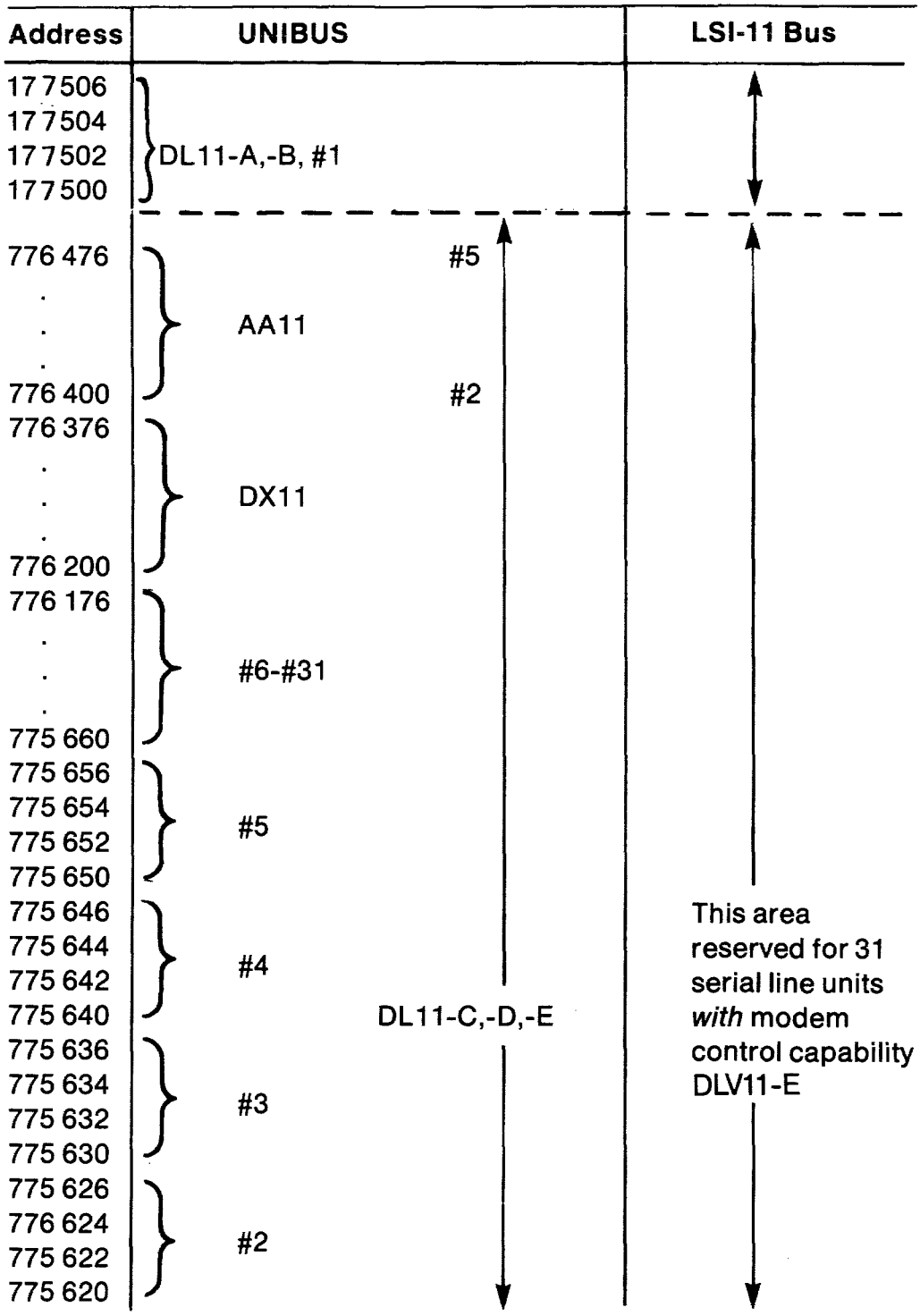
APPENDIX A

DEVICE ADDRESSES (Cont.)

Address	UNIBUS	LSI-11 Bus
777 156 ... 777 000	DIGITAL reserved	
776 776 ... 776 770	AD01	
776 766 ... 776 750	AA11 #1	
776 746 ... 776 740	Unassigned	
776 736 ... 776 700	RP11	
776 676 ... 177530	DL11-A, -B #4-#16	This area reserved for 16 serial line units *without* modem control capability DLV11-A, -B, -F, -J
177526 177524 177522 177520	DL11-A,-B, #3	
177516 177514 177512 177510	DL11-A,-B #2	

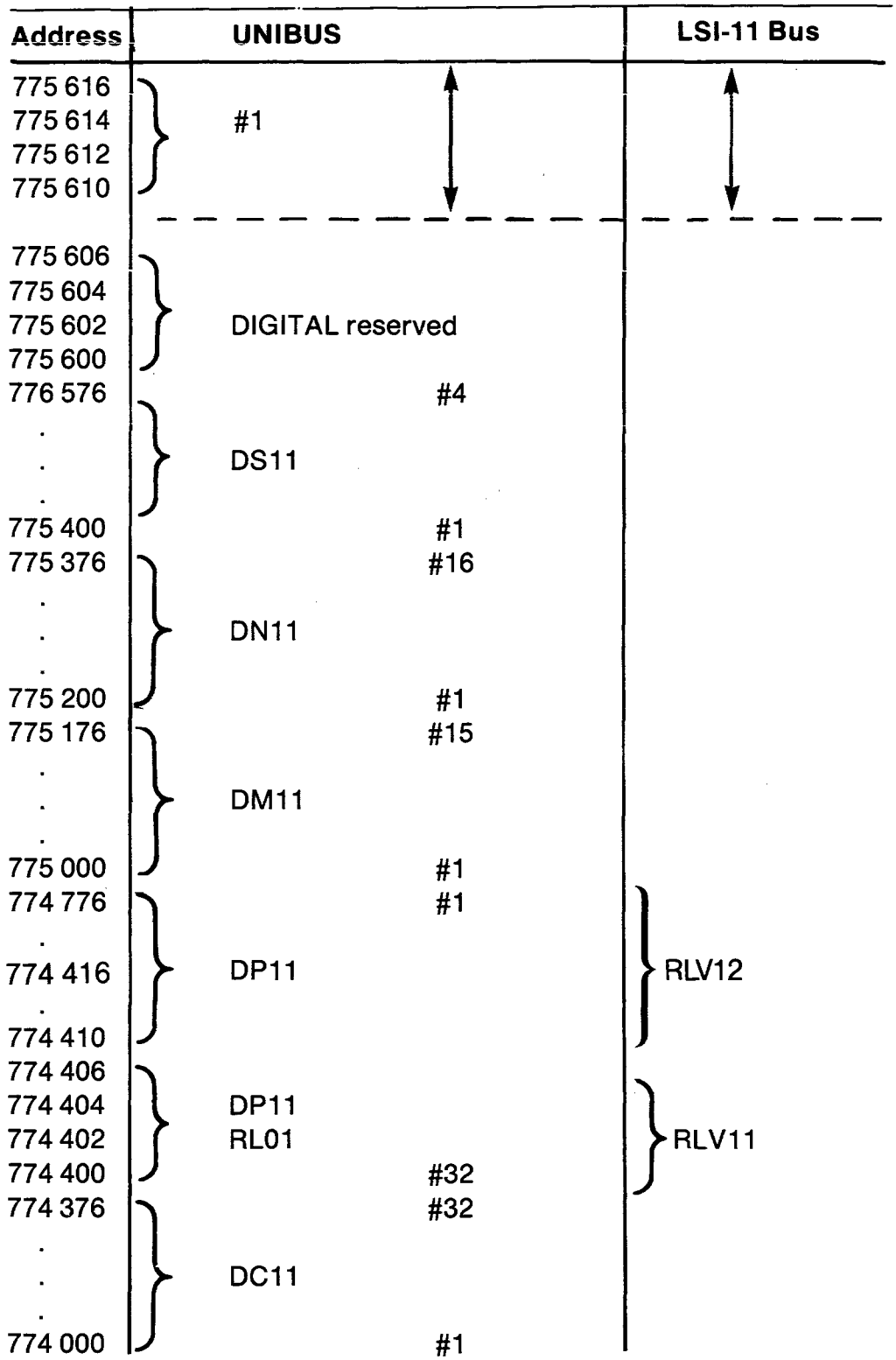
APPENDIX A

DEVICE ADDRESSES (Cont.)



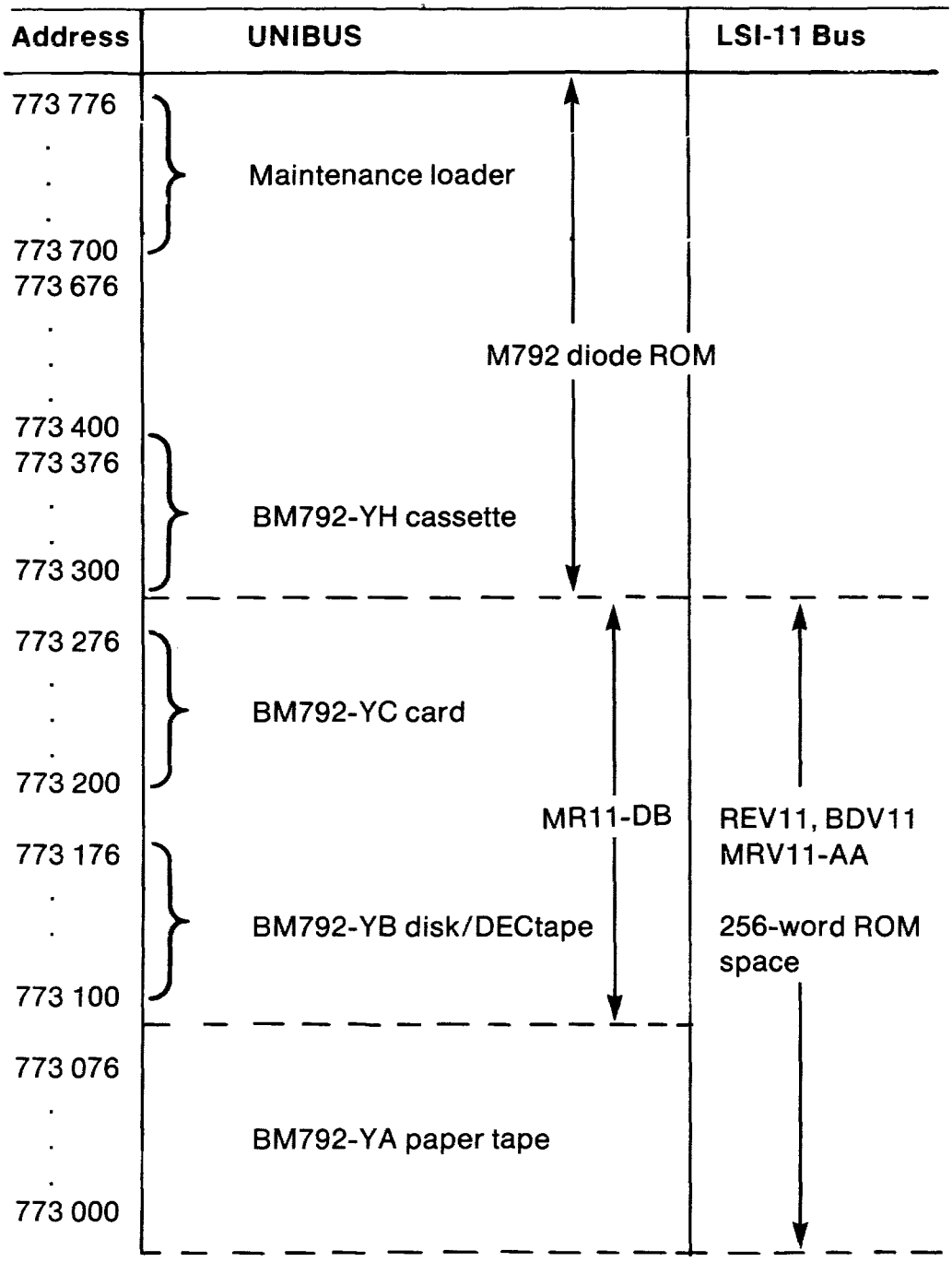
APPENDIX A

DEVICE ADDRESSES (Cont.)



APPENDIX A

DEVICE ADDRESSES (Cont.)



APPENDIX A

DEVICE ADDRESSES (Cont.)

Address	UNIBUS	LSI-11 Bus
772 776 . . . 772 700	PA611 typeset punch	
772 676 . . . 772 600	PA611 typeset reader	
772 576 772 574 772 572 772 570 772 566	AFC11	
. . . 772 560	DIGITAL reserved	
772 556 . . . 772 550	DIGITAL reserved	
772 546 772 544 772 542 772 540	KW11-P	
772 536 772 534 772 532 772 530 772 526 772 524 772 522 772 520	TM11	

APPENDIX A

DEVICE ADDRESSES (Cont.)

Address	UNIBUS	LSI-11 Bus
772 516	Memory mgt status register (SR3)	
772 514 . . . 772 500	OST	
772 456 . . . 772 450	DR11-B, #3	
772 446 . . . 772 440	TJU16	
772 436 772 434 772 432 772 430	DR11-B, #2	DRV11-B, #3
772 426 772 424 772 422 772 420	DIGITAL reserved	DRV11-B, #2
772 416 772 414 772 412 772 410	DR11-B,-C, #1	DRV11-B, #1
772 406 . . . 772 400	KW11-W	
772 376 . . . 772 200	Memory management	

APPENDIX A

DEVICE ADDRESSES (Cont.)

Address	UNIBUS	LSI-11 Bus
772 176 . . . 772 160	FP11	
772 156 . . . 772 140	Unassigned	
772 136 . . . 772 110	Memory parity	
772 106 . . . 772 102	Unassigned	
772 100	MS11-K, -LP, MM11-LP	
772 076 . . . 772 070	RL11	
772 066 . . . 772 040	RJS04	
772 036 . . . 772 020	DIGITAL reserved	

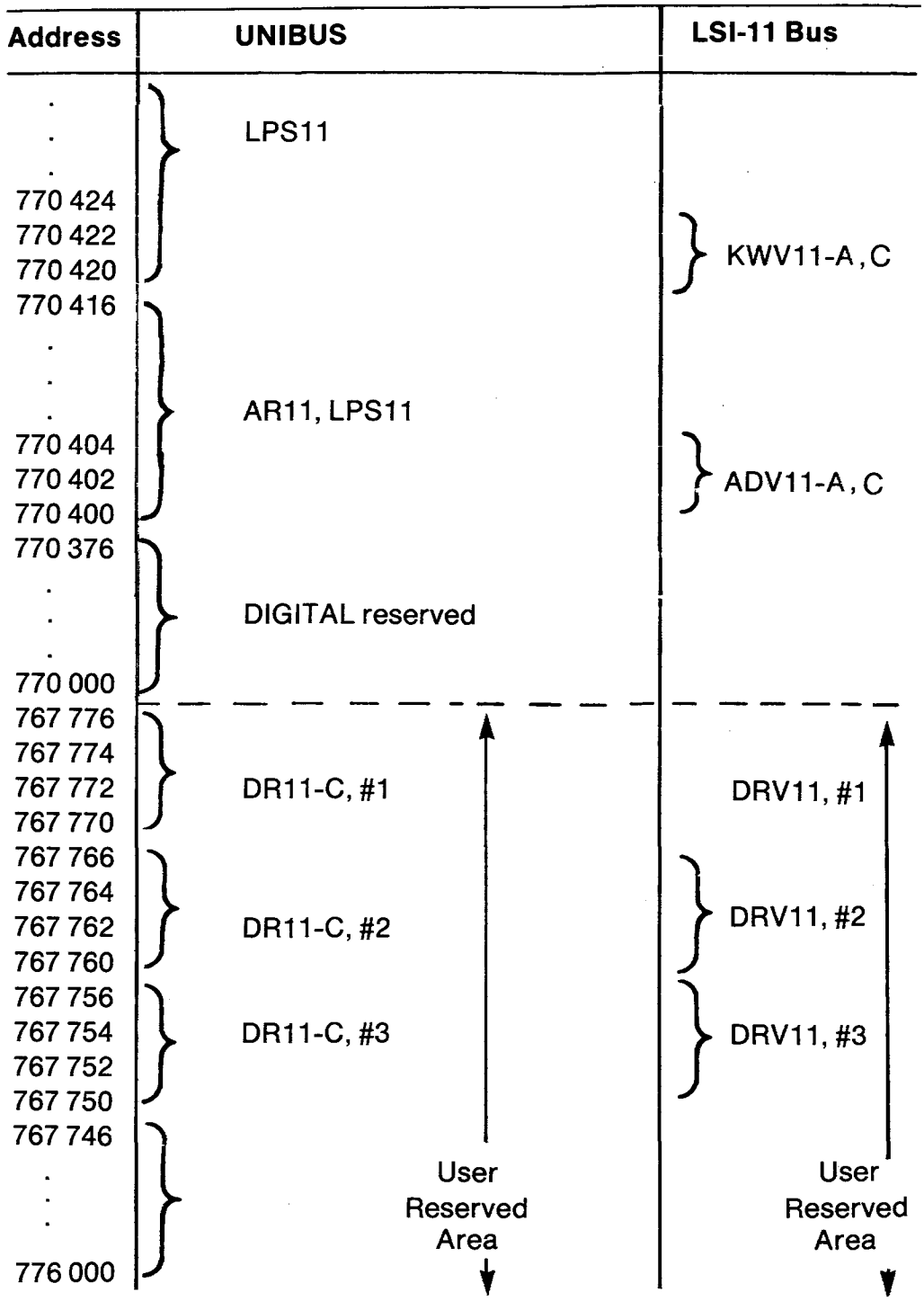
APPENDIX A

DEVICE ADDRESSES (Cont.)

Address	UNIBUS		LSI-11 Bus
772 016 ... 772 000	GT40, VT48		
771 776 ... 771 000	UDC functional I/O modules		
770 776 ... 770 700	KG11	#8 #1	
770 676 ... 770 500	DM11-BB	#16 #1	
770 476 ... 770 460	ADF11		
770 456 ... 770 450	Unassigned		
770 446 770 444 770 442 770 440 770 436	LPS11		AAV11-A , C

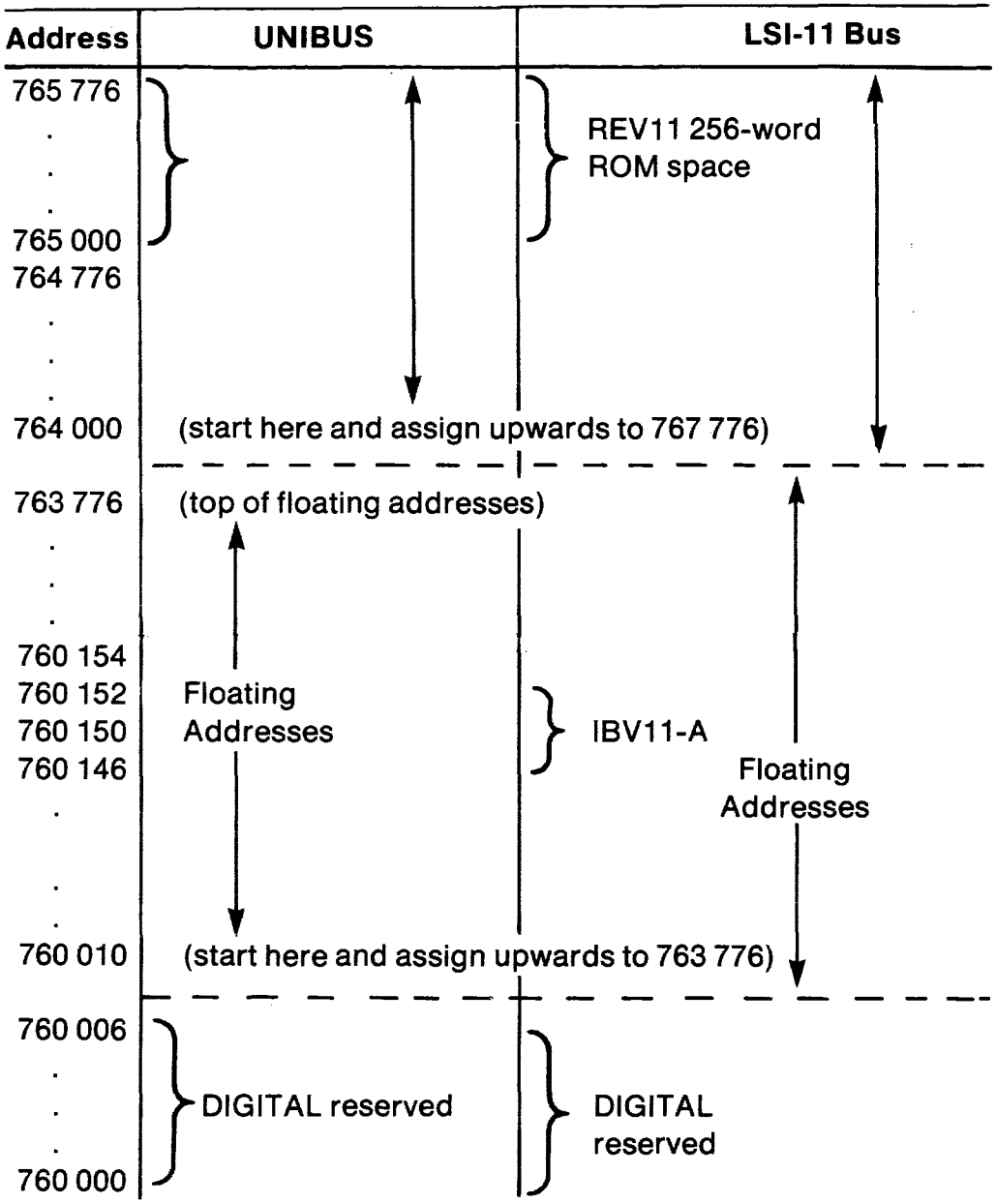
APPENDIX A

DEVICE ADDRESSES (Cont.)



APPENDIX A

DEVICE ADDRESSES (Cont.)



APPENDIX B

ASYNCHRONOUS SERIAL LINE UNIT (SLU) COMPARISONS

The characteristics listed in Tables 1, 2, and 3 compare the different members of the DLV11 (LSI-11 bus) and DL11 (UNIBUS) families of asynchronous serial line products. All modules of the DLV11 series are dual-height modules. The DLV11-E, -F, and -J modules detect overrun conditions which are reported in the receiver CSR. These modules will not generate phantom interrupts on overrun.

DLV11-J

Each of the four serial ports on this module are separate and independent from the others. This is *not* a multiplexed module. Each port has its own CSRs, data buffers, interrupt vectors, baud rates, UARTs, etc. The net effect of this module is to achieve a 4:1 compression ratio over the DLV11. The main functional difference between the ports of the DLV11-J and the DLV11 is that the DLV11-J provides an RS-232C-compatible interface (using RS-422 and RS-423) only and requires the DLV11-KA module (one per port) to accommodate the 110 baud, 20 mA current loop interface.

DLV11-E

This module is functionally equivalent to the DL11-E except that it has programmable baud rates. This module provides one serial port that has full modem control.

DLV11-F

This module is functionally equivalent to the DL11-F except that it has programmable baud rates. This module will eventually replace the DLV11.

DZV11-B

The DZV11-B is a multiplexer interface between four asynchronous serial data communication channels and the LSI-11 bus. The DZV11-B provides EIA level conversion and full modem control suitable for support of Bell series 103, 202, or equivalent modems. Program compatibility is maintained with the UNIBUS option, DZ11-A. The only compatibility exception is the number of serial channels supported. As a product enhancement feature, additional modem control leads are supported to allow half-duplex operation on switched-network-type lines.

MXV11-A

This multifunction module consists of two serial ports, RAM and ROM memory, and a 60 Hz clock. The two serial ports are RS-423 (RS-232-C-compatible, data leads only) The MXV11-A has two completely separate serial ports, where each port has its own CSRs, data buffers, baud rate generation, etc.

Table 1 Comparison of Hardware Features

	Unibus					LSI-11 bus						
	DL11-A	DL11-B	DL11-C	DL11-D	DL11-E	DLV11	DLV11-E	DLV11-F	DLV11-J	DLV11-KA	DZV11-B	MXV11-A
No. of ports per module	1	1	1	1	1	1	1	1	4	1	4	2
EIA RS-232C												
Full modem control					X		X				X	
Limited modem interface		X		X		X		X	X			X
EIA RS-423, RS-422												
Data leads only									X			**
20 mA current loop												
RCVR active or passive						X		X	*	X		
XMIT active or passive						X		X	*	X		
XMIT active only	X	X	X	X								

* The external 20 mA option (DLV11-KB) is required to implement this function.

† Optional feature.

‡ Applies only to the port assigned to the console Device.

§ The loop-back cable is required to implement this function.

| 110 baud only.

** RS-423 only

	Unibus					LSI-11 bus						
	DL11-A	DL11-B	DL11-C	DL11-D	DL11-E	DLV11	DLV11-E	DLV11-F	DLV11-J	DLV11-KA	DZV11-B	MXV11-A
CCITT		X		X	X						X	
Halt on framing error†						X	X	X	‡			‡
Boot on framing error†							X	X	‡			‡
Baud rates (Table 3)												
Programmable							X	X			X	
On-board clocks for split speed	X	X	X	X	X		X	X			X	
Reader run control	X		X			X		X	*			
Error flags	X	X	X	X	X		X	X			X	

* The external 20 mA option (DLV11-KB) is required to implement this function.

† Optional feature.

‡ Applies only to the port assigned to the console Device.

§ The loop-back cable is required to implement this function.

| 110 baud only.

	Unibus					LSI-11 bus						
	DL11-A	DL11-B	DL11-C	DL11-D	DL11-E	DLV11	DLV11-E	DLV11-F	DLV11-J	DLV11-KA	DZV11-B	MXV11-A
Break generation bit	X	X	X	X	X	X	X	X	X		X	X
Receiver active bit	X	X	X	X	X		X	X				
Maintenace bit	X	X	X	X	X	§	X	X	§		X	§
UART cleared by INIT	X	X	X	X	X		X	X	X			
UART cleared by DCOK						X			X			
No trap on write to input buffer	X	X	X	X	X		X	X				

* The external 20 mA option (DLV11-KB) is required to implement this function.

† Optional feature.

‡ Applies only to the port assigned to the console Device.

§ The loop-back cable is required to implement this function.

| 110 baud only.

	Unibus					LSI-11 bus						
	DL11-A	DL11-B	DL11-C	DL11-D	DL11-E	DLV11	DLV11-E	DLV11-F	DLV11-J	DLV11-KA	DZV11-B	MXV11-A
Easy configuration using wire-wrap jumpers							X	X	X			X
Stop bits												
1			X	X	X	X	X	X	X		X	X
1.5			X	X	X						X	
2	X	X	X	X	X	X	|	|	X		X	X

* The external 20 mA option (DLV11-KB) is required to implement this function.

† Optional feature.

‡ Applies only to the port assigned to the console Device.

§ The loop-back cable is required to implement this function.

| 110 baud only.

Table 2 Baud Rates

Baud Rate	Unibus					LSI-11 bus						
	DL11-A	DL11-B	DL11-C	DL11-D	DL11-E	DLV11	DLV11-E	DLV11-F	DLV11-J	DLV11-KA	DZV11-B	MXV11-A
50	X	X	X	X	X	X	X	X			X	
75	X	X	X	X	X	X	X	X			X	
110	X	X	X	X	X	X	X	X	*		X	
134.5			X	X	X	X	X	X			X	
150	X	X	X	X	X	X	X	X	X		X	X
200			X	X	X	X						
300	X	X	X	X	X	X	X	X	X		X	X
600	X	X	X	X	X	X	X	X	X		X	
1200	X	X	X	X	X	X	X	X	X		X	X
1800	X	X	X	X	X	X	X	X			X	
2000							X	X			X	
2400	X	X	X	X	X	X	X	X	X		X	X
3600							X	X			X	
4800			X	X	X	X	X	X	X		X	X
7200			X	X	X		X	X			X	
9600			X	X	X	X	X	X	X		X	X
19200							X	X	X			X
38,400									X			X
External						X		X	X	X		

* The external 20 mA option (DLV11-KB) is required to implement this function.

Table 3 Comparison of Software Features

			Unibus					LSI-11 bus				
			DL11-A	DL11-B	DL11-C	DL11-D	DL11-E	DLV11	DLV11-E	DLV11-F	DLV11-J	MXV11-A
Register	**Bit**	**Name**										
RCSR	15	Data Set Status/ Interrupt					X					
	14	Ring				X		X				
	13	CTS					X		X			
	12	CD					X		X			
	11	Receiver Active	X	X	X	X	X		X	X		
	10	2d Receive					X		X			
	9,8,4	Unused	X	X	X	X	X	X	X	X	X	X
	7	Receive Done	X	X	X	X	X	X	X	X	X	X
	6	Receive Int Enb	X	X	X	X	X	X	X	X	X	X
	5	Data Set Int Enb					X		X			
	3	2d XMT					X		X			
	2	RTS					X		X			
	1	PTR					X		X			
	0	Rdr Enable	X		X			X		X	*	

* The external 20 mA option (DLV11-KB) is required to implement this funtion.

Register			Unibus					LSI-11 bus				
			DL11-A	DL11-B	DL11-C	DL11-D	DL11-E	DLV11	DLV11-E	DLV11-F	DLV11-J	MXV11-A
RBUF	15	Error			X	X			X	X	X	X
	14	OE			X	X	X		X	X	X	X
	13	FE			X	X	X		X	X	X	X
	12	PE			X	X	X		X	X	X	X
	11-8	Unused	X	X	X	X	X	X	X	X	X	X
	7-0	Receive Data	X	X	X	X	X	X	X	X	X	X
XCSR	15-8	Unused	X	X	X	X	X	X	X	X	X	X
	7	XMT Ready	X	X	X	X	X	X	X	X	X	X
	6	XMT Int Enb	X	X	X	X	X	X	X	X	X	
	5-3,1	Unused	X	X	X	X	X	X	X	X	X	X
	2	Maintenance	X	X	X	X	X	*	X	X	*	*
	0	XMT Break			X	X	X	X	X	X	X	X
XBUF	15-8	Unused	X	X	X	X	X	X	X	X	X	X
	7-0	XMT BUF	X	X	X	X	X	X	X	X	X	X

* The external 20 mA option (DLV11-KB) is required to implement this funtion.

APPENDIX C

COMPARISON OF DATA TRANSMISSION TECHNIQUES

Frequently, the application arises where a data transmission path has to be established between two devices. Usually the distance between the device is known and also the rate of data transmission. The problem is deciding which is the best communication technique to use to interconnect the devices.

Figure 1 is a graph of data versus distance for the various standard transmission techniques. Parallel data transmission techniques (PLUs and DMA) give the highest data rate; however, they are good only for relatively short distances. The serial techniques (RS-232C, RS-422 and current loops) are good for longer distances but at limited data rates.

While analyzing Figure 1, remember that the axes are logarithmic and that the data in words per second rather than baud rate. The limits established for distance and data rate are a function of both the inherent limitations of the transmission technique and of the DIGITAL device used to do the interconnection. As an example, look at the 422 section of the graph. Maximum distance is 4000 feet as established by EIA standard RS-422, but the maximum data rate of 1920 words per second is based on the maximum baud rate of the DLV11-J which is 38.4K baud.

Table 1 is a summary of the LSI-11 bus and UNIBUS devices which can be used with each communication technique. Currently, there is no UNIBUS device for EIA RS-422.

APPENDIX C

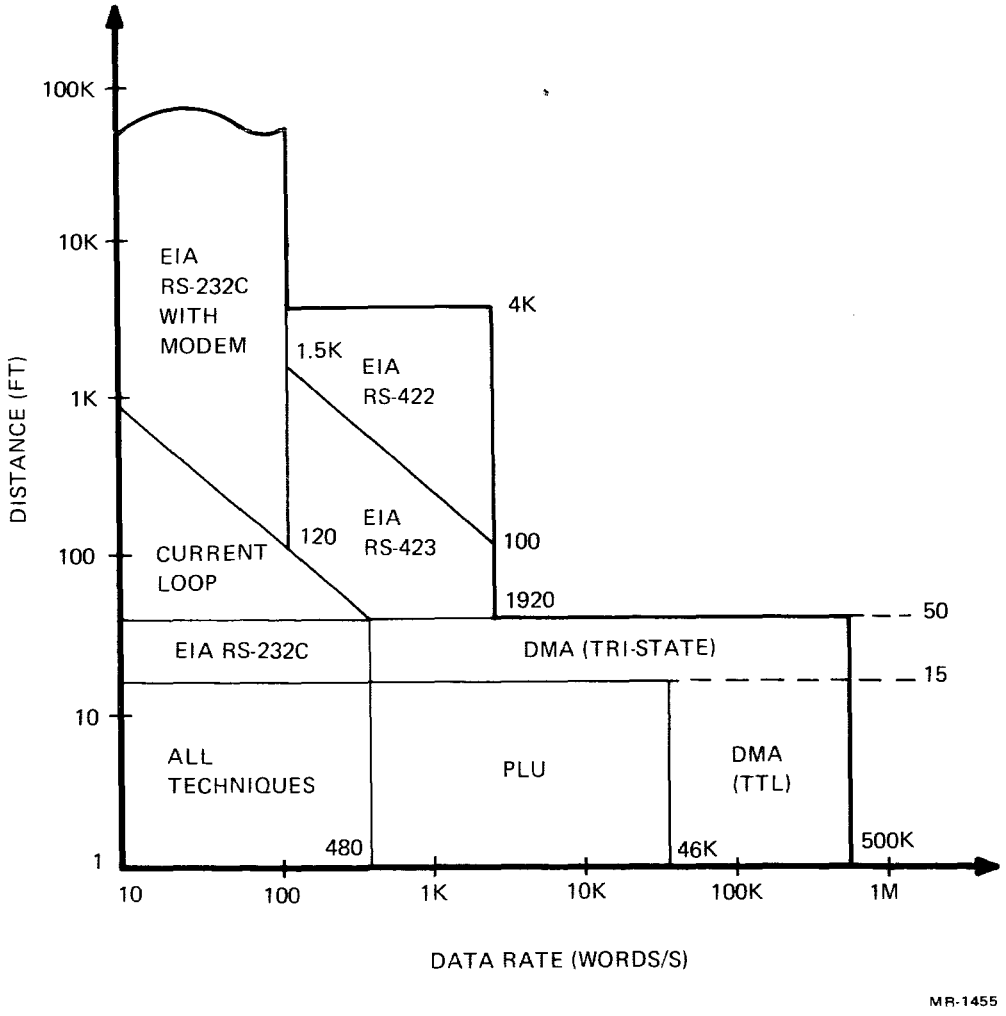


Figure 1 Data Rate vs Distance with DIGITAL Devices

Table 1 Communication Techniques

	LSI-11	UNIBUS
Loop	DLV11	DL11-C
EIA (RS-232C)	DLV11	DL11-D
EIA with Modem	DLV11-E	DL11-E
RS422, RS423	DLV11-J	—
PLU	DRV11	DR11-C
DMA	DRV11-B	DR11-B

APPENDIX C

NOTES AND ASSUMPTIONS FOR FIGURE 1

1. Data Rate Definition
   a. One word equals 16 bits.
   b. For serial techniques, one word equals two characters formatted with one start bit, eight data bits, and one stop bit. Asynchronous serial transmission is assumed.
2. Serial Line Maximum Data Rate
   a. Modems were limited to 120 words/sec (2400 baud) because modems with higher rates cost more than LSI-11 systems usually warrant. Higher data rate modems are generally synchronous rather than asynchronous.
   b. 480 words/sec is equal to 9600 baud, the limit of the DLV11 SLU.
   c. 1920 words/sec is equal to 38.4 baud, the limit of DLV11-J SLU.
3. PLU (Parallel Line Unit) Limits
   a. The TTL inputs/outputs of the DRV11 limit the distance to 15 feet.
   b. 46K words/sec assumes non-interrupt-driven program servicing with bit testing (TSTB, BMI, MOV and SOB). 97K words/sec is maximum rate with program servicing without bit testing (MOV and BR). With interrupt-driven servicing, the maximum limit is 20K words/sec assuming 50 μs for interrupt latency and software servicing of interrupt.
4. DMA (Direct Memory Access) Limits
   a. The DRV11-B can be used up to 50 feet because it has tri-state drivers and receivers. The distance is limited to 15 feet with TTL devices like the DR11-B.
   b. DMA transfer with the DRV11-B and the DR11-B are limited to 500K words/sec in burst mode operation; 250K words/sec is the limit for single-cycle mode operation with either device. These limits are device-dependent, not LSI-11 bus-dependent. Note that burst mode can disrupt memory refreshing if bus refreshing (DMA and microcode) is used. Self-refreshing memories (MSV11-CD or MSV11-D) eliminate this problem.

APPENDIX D

BUS RECEIVERS AND BUS DRIVERS

The equivalent circuits of LSI-11 bus-compatible drivers and receivers are shown in Figure 1. To perform the receiver and driver functions, Digital Equipment Corporation uses two monolithic integrated circuits with the characteristics listed in Table 1. A typical bus driver circuit is shown in Figure 2. Note that 8641 quad transceivers can be used, combining LSI-11 bus receiver and driver functions in a single package. Bus receiver (8640), bus driver (8881), and bus transceivers (8641) are shown in Figures 3, 4, and 5, respectively.

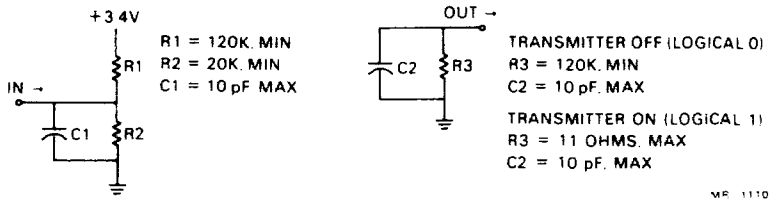


Figure 1 Bus Driver and Receiver Equivalent Circuits

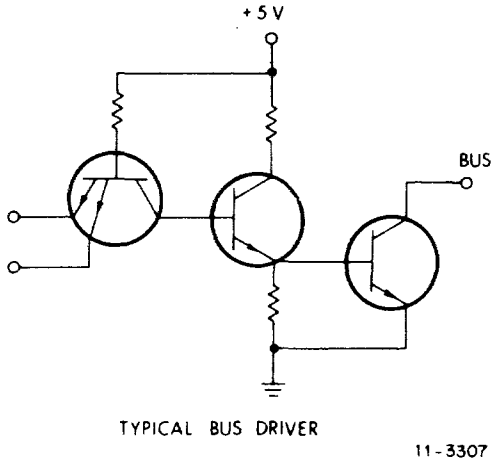


Figure 2 Typical Bus Driver Circuit

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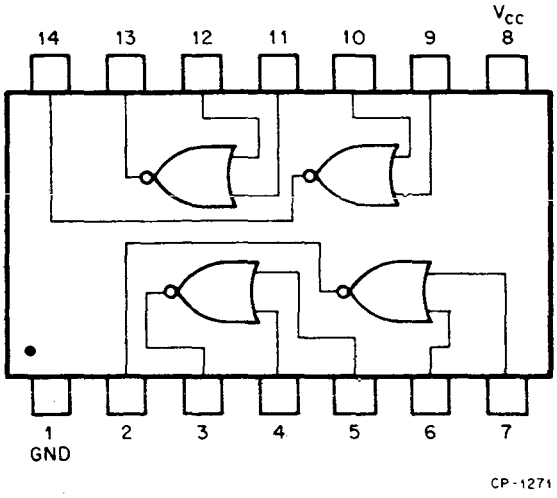

Figure 3 8640 Quad 2-Input NOR Gates (Bus Receiver)

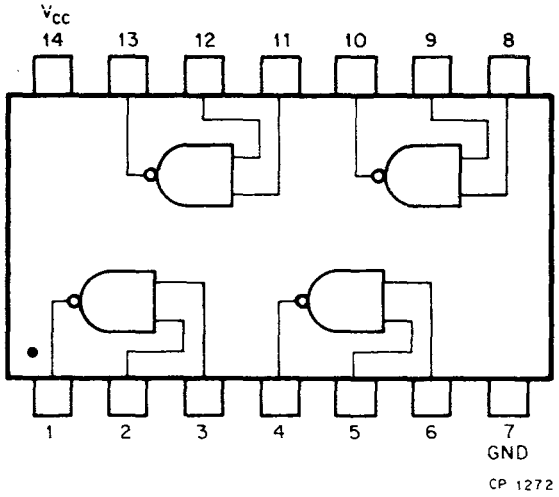

Figure 4 8881 Quad 2-Input NAND Gate (Bus Driver)

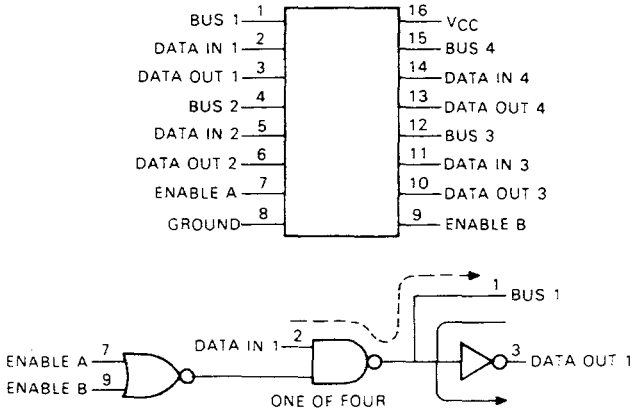

Figure 5 8641 Quad Unified Bus Transceiver (Bus Receiver/Driver)

APPENDIX D

Table 1 LSI-11 Bus Driver, Receiver, Transceiver Characteristics

Device	Characteristic	Sym	Specifications	Notes
Receiver	Input high voltage	V_{IH}	1.7 V min	1
(8640)	Input low voltage	V_{IL}	1.3 V max	1
(8641)	Input current at 3.8 V	I_{IH}	80 μA max	1, 3
	Input current at 0 V	I_{IL}	10 μA max	1, 3
	Output high voltage	V_{OH}	2.4 V min	2
	Output high current	V_{OH}	(16 TTL loads)	2, 3
	Output low voltage	V_{OL}	0.4 V max	2
	Output low current	I_{OL}	(16 TTL loads)	2, 3
	Propagation delay to high state	TPDH	10 ns min 35 ns max	4, 5
	Propagation delay to low state	TPDL	10 ns min 35 ns max	1, 5
Driver	Input high voltage	V_{IH}	2.0 V min	
(8881)	Input low voltage	V_{IL}	0.8 V max	
(8641)	Input high current	I_{IH}	60 μA max	6
	Input low current	I_{IL}	−2.0 mA max	6
	Output low voltage 70 mA sink	V_{OL}	0.8 V max	1
	Output high leakage current at 3.5 V	I_{OH}	25 μA max	1, 3
	Propagation delay to low state	TPDL	25 ns max	1, 5
	Propagation delay to high state	TPDH	35 ns max	1, 5

NOTES

1. This is a critical parameter for use on the I/O bus. All other parameters are shown for reference only.
2. This is equivalent to being capable of driving 16 unit loads of standard 7400 series TTL integrated circuits.
3. Current flow is defined as positive if into the terminal.
4. Conditions of load are 390 Ω to +5 V and 1.6 kΩ in parallel with 15 pF to ground for 10 ns min and 50 pF for 35 ns max.
5. Times are measured from 1.5 V level on input to 1.5 V level on output.
6. This is equivalent to 1.25 standard TTL unit loading of input.

Bus receivers and drivers should be well grounded and use V_{CC} to ground bypass capacitors. These gates should be located as close as practical to the module fingers which plug into the backplane and all etch runs to the bus should be kept as short as possible. Attention to these cautions should yield a module design with minimum bus loading (capacitance).

APPENDIX E

CABLING SUMMARY

Preassembled cables are available in a variety of lengths and types as listed in Table 1. The H854 and H856 connectors are shown in Figure 1.

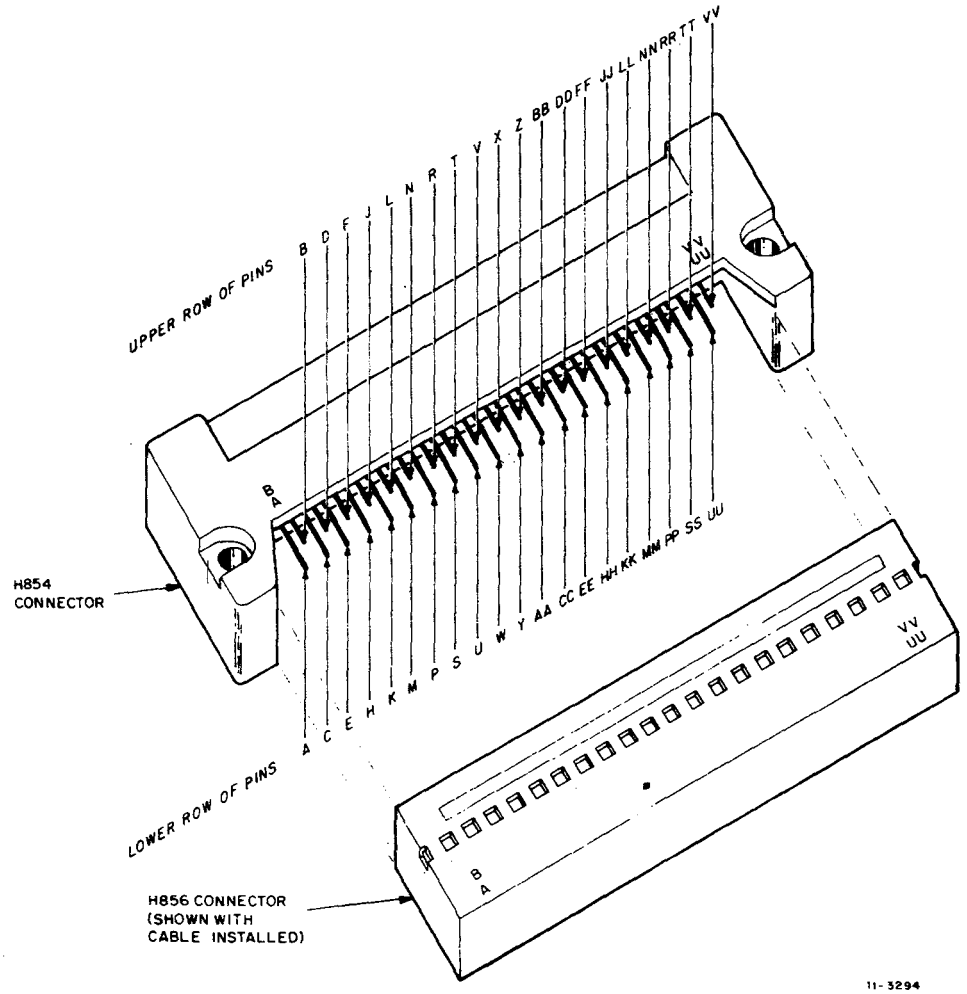

Figure 1 J1 or J2 Connector Pin Locations

APPENDIX E

Function	Module Type	Cable Recommendations
Serial I/O–Asynchronous		
20 MA	DLV11-F 1-Line DLV11-J 4-Line	BC05M-2C DLV11-KA (1 per line)
EIA RS-232C Data only (DLV11-J is also RS422/423)	DLV11-F 1-Line DLV11-J 4-Line MXV11-A	BC01V-25 (M) BC21B-05 (M) or 1 per line BC20N-05 (T)
EIA RS-232C with Modem Control	DLV11-E 1-Line DZV11-B 4-Line MUX	BC01V-25 (M) Cable included
Serial I/O–Synchronous		
EIA RS-232C with Modem Control	DUV11-DA 1-Line	BC05C-25 (M)
Digital I/O		
Programmed Transfer	DRV11 16 in/16 out	BC07D-15(U) 2 ea or
DMA Transfer	DRV11-B 16 in/16 out	BC08R-12(B)
Analog I/O		
A/D	ADV11-A 16 channel	BC07D-15(U)
D/A	AAV11-A 4 channel	BC08R-12(B)
Mass Storage		
Tape Cartridge	TU58-BB	BC20N-05 plus a Serial Modem (M) cable
Double Density Floppy Diskette	RXV21-BA	Includes cable
Hard Disk (H9273 Backplane Req'd)	RLV11-AK	Includes cable

Note: M–Connects to a Modem T–Connects to an EIA Terminal
U–User end unterminated B–User end terminated with 40 pin Berg Connector

APPENDIX F

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EK-BA11A-IP	BA11-A Unit Assembly IPB
EK-BA11A-TM	BA11-A Mounting Box & Power Tech
EK-BA11F-IP	BA11-F Mounting Box IPB
EK-BA11K-IP	BA11-K Mounting Box IPB
EK-BA11K-OP	BA11-K Mounting Box User Manual
EK-BA11K-TM	BA11-K Mounting Box Tech Manual
EK-BA11L-IP	BA11-L Mounting Box IPB
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EK-BA11M-IP	BA11-M Mounting Box IPB
EK-BA11N-IP	BA11-N Mounting Box IPB

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EK-BA11N-TM	BA11-N Mounting Box Configuration Guide
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EK-BA11N-TM	BA11-N Mounting Box Tech Manual
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EK-BA11U-IP	BA11-U Mounting Box IPB
EK-BA11V-IP	BA11-V Box Assembly IPB
EK-BA11V-RG	BA11-VA Configuration Guide
EK-BA1KP-IN	BA11-KP Installation Manual
EK-BAM11-TM	BAM11 Technical Manual
EK-BAM11-UG	BAM11 Status Alarm Monitor User Guide
EK-BDV11-TM	BDV11 Technical Manual
EK-BDV11N-TM	BDV11 Technical Manual
EB-19187-75	Cables Handbook
EK-01387-92	Chipkit User Guide
EK-DLV11J-UG	DLV11-J User Guide
EK-DLVKA-IN	DLV11-KA Installation Manual
EK-DLV11-OP	DLV11-E/F User Manual
EK-DPV11-CG	DPV11-DA Configuration Guide
EK-DPV11-UG	DPV-11 Synchronous Interface User Guide
EK-DPV11-TM	DPV-11 Technical Manual

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CATALOG NO.	PUBLICATION
EK-DRV1B-OP	DRV11-B Interface User Manual
EK-DRV1J-UG	DRV11-J Interface User Manual
EK-DRV11-OP	DRV11-P Foundation Module User Manual
EK-DUV11-TM	DUV-11 Line Interface Technical Manual
EK-DUV11-OP	DUV11 User Guide
EK-DZV11-TM	DZV11 Asynch Multi Technical Manual
EK-DZV11-TM	DZV11 Asynch Multi Technical Manual
EK-DZV11-UG	DZV11 Asynch Mtlpxr Guide & Addendum
EK-FPF11-TM	FPF11 Floating-Point Processor Technical Manual
EK-H927A-CG	H9275-A Configuration Guide
EK-IBV11-UG	IBV11-A User Manual
EK-KD1HA-CG	LSI-11/2 Processor Configuration Sheet
EK-KDF11-UG	KDF11-AA User Guide
EK-KDFAA-CG	LSI-11/23 Processor Configuration Sheet
EK-KUV11-TM	LSI-11 WCS User Guide
EK-AXV11-UG	KWV11-C User Guide
EK-KXT11-UG	KXT11-AA User Guide
EK-KXT11-CG	KXT11-AA Configuration Guide
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EK-LA120-UG	LA120-RA User Guide

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EK-LSI11-TM	LSI-11 PDP-11/03 User Manual
EK-LSIFS-SV	LSI-11 System Service Manual
EK-MCV1D-UG	MCV11-D User Guide
EB-20912-20	Microcomputer And Memories Handbook 1982
EB-20175-20	Microcomputer Interface Handbook 1981
EK-MSV1D-OP	MSV11-D/E User Manual
EK-MSVOL-UG	MSV11-L User Guide
EK-MSVOP-UG	MSV11-P User Guide
EB-19402-20	PDP-11 Processor Handbook
EK-T03LO-OP	PDP-11/T03-L System Manual
EK-V03LO-OP	PDP-11/V03-L System Manual
EK-1V03L-IP	PDP-11/V03-L Unit Assembly
EK-11V23-IP	PDP-11/V23 Unit Assembly IPB
EK-11V23-OP	PDP-11/V23 System Manual
EK-PWRPK-CL	Power And Packing Catalog
EK-RL012-PG	RKL01/02 Pocket Service Guide
EK-RL012-TM	RL01/02 Disk Drive Tech Manual
EK-RL012-UG	RL01/02 User Guide
EK-RL012-WS	RL01/02 P.M. Worksheet 25/P KG

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EK-RLV12-UG	IPB RLV12 User Guide
EK-ORX01-IP	RX01 Floppy Disk IPB
EK-ORX01-MM	RX01/08/11 Maintenance Manual
EK-ORX02-IP	RX02 Floppy Disk IPB
EK-ORX02-TM	RX02 Floppy Disk Systems Technical Manual
EK-ORX02-UG	RX02 Floppy Disk System User Guide
EK-OSB11-DG	SB11 Series OEM Sys Design Users Guide
EK-OSB11-IP	SB11 Microcomputer IPB
EK-TU58E-CG	TU58-EA Configuration Guide
EK-OTU58-EC	TU58 DECtape Customer Equip Care
EK-OTU58-IP	TU58 Cartridge Tape Drive Ipt
EK-OTU58-PS	TU58 DECtape II Pocket Service Guide
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EK-OTU58-WS	TU58 DECtape Installation Sheet

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EK-VT100-UG	VT100 User Guide
ED-VT103-CG	VT103 Configuration Guide
EK-VT103-UG	VT103 LSI-11 User Guide And Addendum
EK-VT103-IP	VT103 Unit Assembly IPB
EK-VT1X3-CG	VT1X3-MM Maintenance Module Configuration Sheet
EK-VT125-UG	VT125 User Guide

Option Bulletins/Postcards/Miscellaneous

EJ-21725-53	AAV11-C Analog I/O Board Postcard
EJ-21724-53	ADV11-C Analog I/O Board Postcard
EJ-21726-53	AXV11-C Analog I/O Board Postcard
ED-21049-53	AAV11-C, ADV11-C, AXV11-C Option Bulletin
ED-18321-53	Asynchronous Interface LSI-11 (DLV11-E)
AA-K724A-TC	Basic-11/RT-11 Installation Guide & Release Notes
ED-09371-53	Battery Backup-LSI-11 Eng. Note
EA-19971-18	Coming To Terms With IBM & Networking
GA-18195-75	Computer Maintenance Alternative Use
ED-06703-92	DDV11-B 9X6 Slot LSI-11 Backplane Bulletin
EJ-19822-53	DPV11-DA Synchronous Line Interface
ED-20086-53	DPV11-DA Option Bulletin

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ED-18511-53	.DRV11-J Option Bulletin
ED-18326-53	EPROM/P ROM/ROM Module LSI-11 (MRV11-C)
ED-17472-53	EPROM/P ROM/ROM Module March 79
ED-18322-53	Four-Channel LSI-11 Micro (DLV11-J)
EA-20360-53	.H9275-A Option Bulletin
ED-18762-53	High Density Parallel Interface DRV11-J
ED-07494-53	IBV11-A Interface Option For LSI-11
ED-18328-53	IEEE Interface OPT LSI-11 (IBV11-A)
EJ-21048-53	.KWV11-C Programmable RealTime Clock Postcard
EJ-21347-53	KXT11-AA (SBC-11/21) Processor Board Postcard
ED-21608-20	KXT11-AA Option Bulletin
ED-21394-53	KWV11-C Option Bulletin
ED-18967-18	LA38 DECwriter II Terminal
ED-18966-18	LA120 DECwriter III Data Sheet
ED-19211-56	LA120-RA DECprinter III Bulletin 4/80
ED-08193-18	LA180 DECprinter Data Sheet 06/78
ED-17474-53	LSI-11 Mounting Chassis/P Ower March 79
ED-18327-53	LSI-11 Multifunction ModulE (MXV11)
ED-18324-53	LSI-11 Option Memory Module (MSV11-DD)
ED-18323-53	LSI-11/2 Central Processor (KD11-HA)

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ED-18393-18	LSI-11/23 Data Sheet Oct 79
ED-18325-53	LSI-11/23 High Performance (KDF11-AA)
EH-17898-20	LSI-11/23 (PDP-11/23) Reference Card
EA-17057-18	LSI-11/23 Microcomputer
ED-18393-53	LSI-11/23 Option Bulletin
EE-19213-53	Micro Products Group Product Description
EJ-18382-53	Microcomputer Products Group U-note
EA-18334-53	Microcomputer Products Selection Guide
EA-20065-53	Microcomputer Software Brochure
EJ-22088-53	MCV11-D CMOS Read/Write Memory Postcard
ED-22045-53	MCV11-D Option Bulletin
ED-08012-53	MRV11-B Option Bulletin
ED-20881-53	MSV11-L Option Bulletin
ED-17470-53	MXV11 Multifunction Module March 79
EH-07043-53	PDP-11/03, LSI-11 Reference Card
EA-19442-18	RT-11 Single-User Realtime Systems
EJ-18922-28	RT-11 Technical Summary
ED-20997-53	RXO2 Option Bulletin
AE-3438C-TC	SPD 9.2.2 Papertape Support Package
AE-J514A-TC	SPD 10.16.0 RT-11

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CATALOG NO.	PUBLICATION
AE-D431F-TC	SPD 10.72.6 DECnet-RT
AE-3393M-TC	SPD 12.1.14 RT-11
AE-D007D-TC	SPD 12.4.3 RT2
AE-3394H-TC	SPD 12.5.8 BSC-11/RT-11
AE-3395L-TC	SPD 12.10.12 F IV/RT-11
AE-H257B-TC	SPD 12.14.1 Instrument Bus Sub
AE-3397F-TC	SPD 12.20.6 MU BSC-11/RT-11
AE-H585B-TC	SPD 12.21.1 PROM/RT-11
AE-H509C-TC	SPD 12.22.2 FMS-11/RT-11
AE-J673A-TC	SPD 12.29.0 Fortran/RT-11 Lab Extensions
AE-J698A-TC	SPD 14.42.0 APL-11/RT
AE-D607C-TC	SPD 15.44.2 LSP-11
AE-3413E-TC	SPD 15.45.6 SSP-11
AE-D370C-TC	SPD 15.90.2 LSI-11 Micro Tools
EA-18784-53	The Story Behind LSI-11 Microcomputer
EA-19973-53	TU-58 Option Bulletin October 1980
ED-17473-53	Universal Prom Programmer March 79
ED-19000-53	VT103/L SI-11 Video Terminal April 1980

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Brochures/Articles/Posters

CATALOG NO.	PUBLICATION
EJ-N0571-26	LSI-11 Trio Calls The Tune Article
EJ-N0994-53	Canadian Stock Exchange Article
EJ-N0995-53	Manufacturing Memory Tester Article
EJ-N0002-53	It's An Inside Job Article
EJ-N0017-53	Digital Controls Article
EJ-N1198-53	Low-cost 16-Bit Microcomputer Article
EJ-N1269-53	Airborne Data Acquisition System Article
EJ-N0076-53	If You Don't Have Millions In R&D Your Microcomputer Should Ad Reprint
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EJ-N0888-53	Our Microcomputers Are Faster Ad Reprint
EJ-20855-53	Mighty Micro Press Kit

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CATALOG NO.	PUBLICATION
EJ-21875-53	Falcon Press Kit
EJ-21317-53	Mighty Micro Poster
EJ-22251-53	Falcon Poster
EA-18097-18	Digital Family Of Terminals Brochure
EA-21333-18	LSI-11 Family Brochure
EA-23312-18	MICRO/PDP-11 Brochure
EJ-22333-18	Microcomputer Products Chips-Systems-Supplies Brochure
EA-21607-53	Micropower/Pascal Brochure
EA-18924-18	PDP-11 Microcomputer Members Brochure
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