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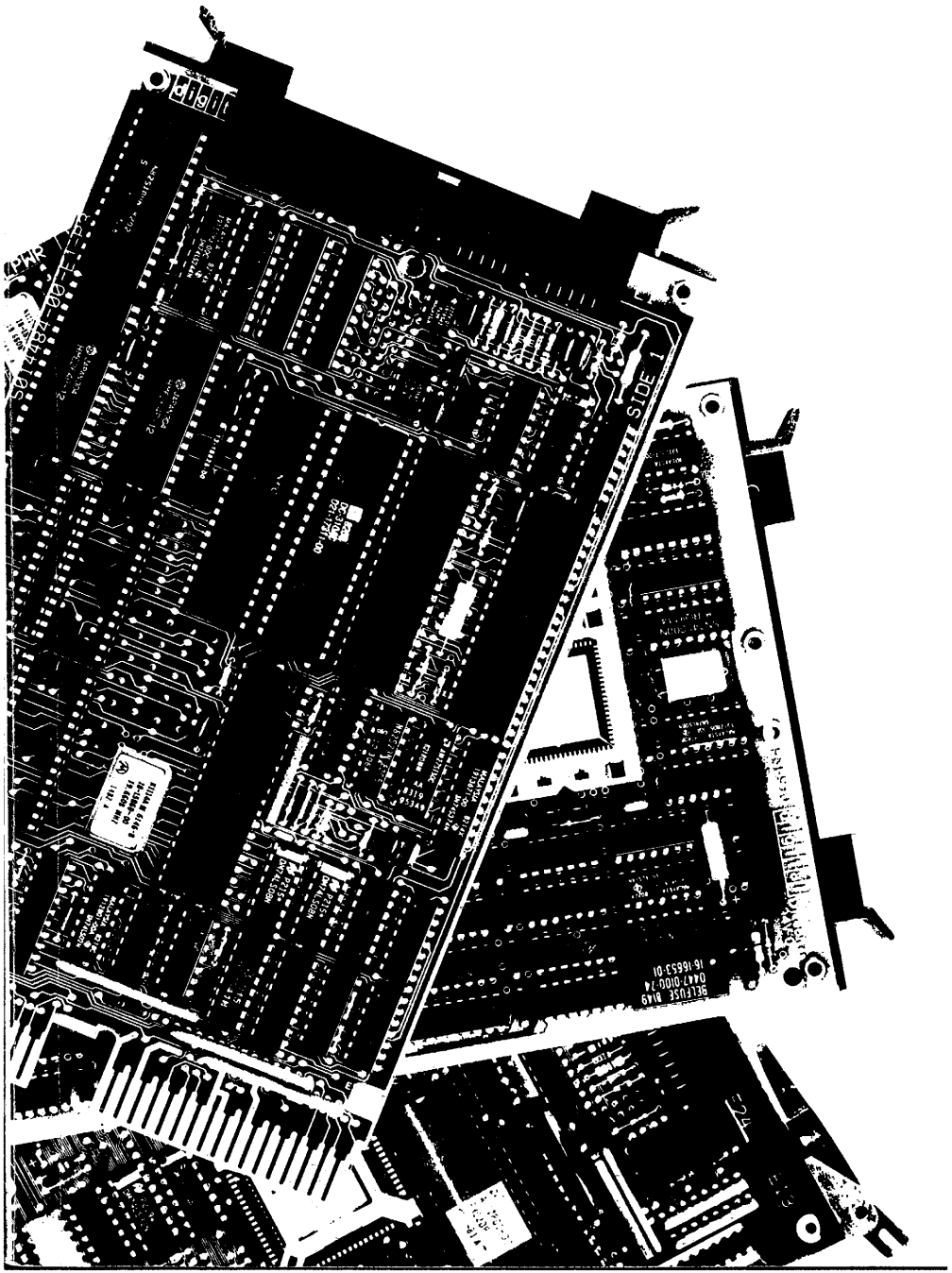
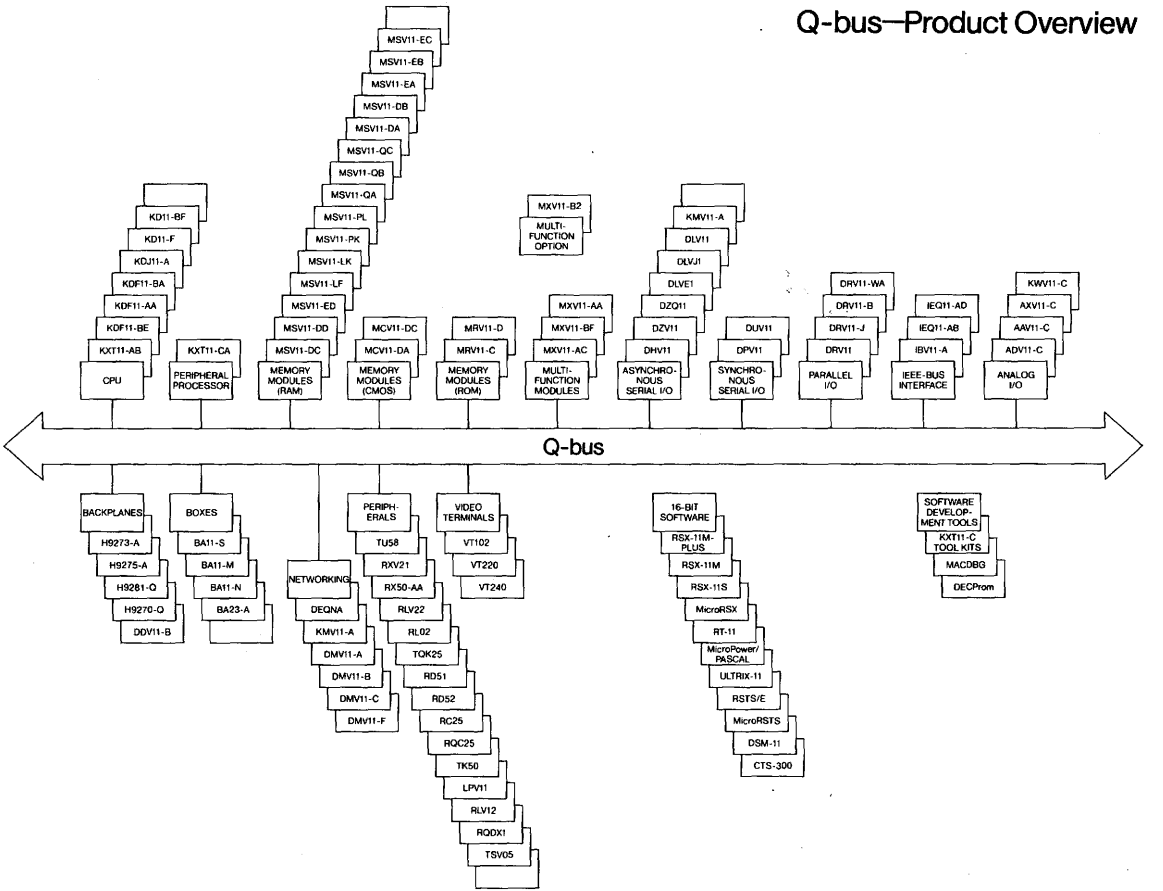


Q-bus—Product Overview



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Foreword

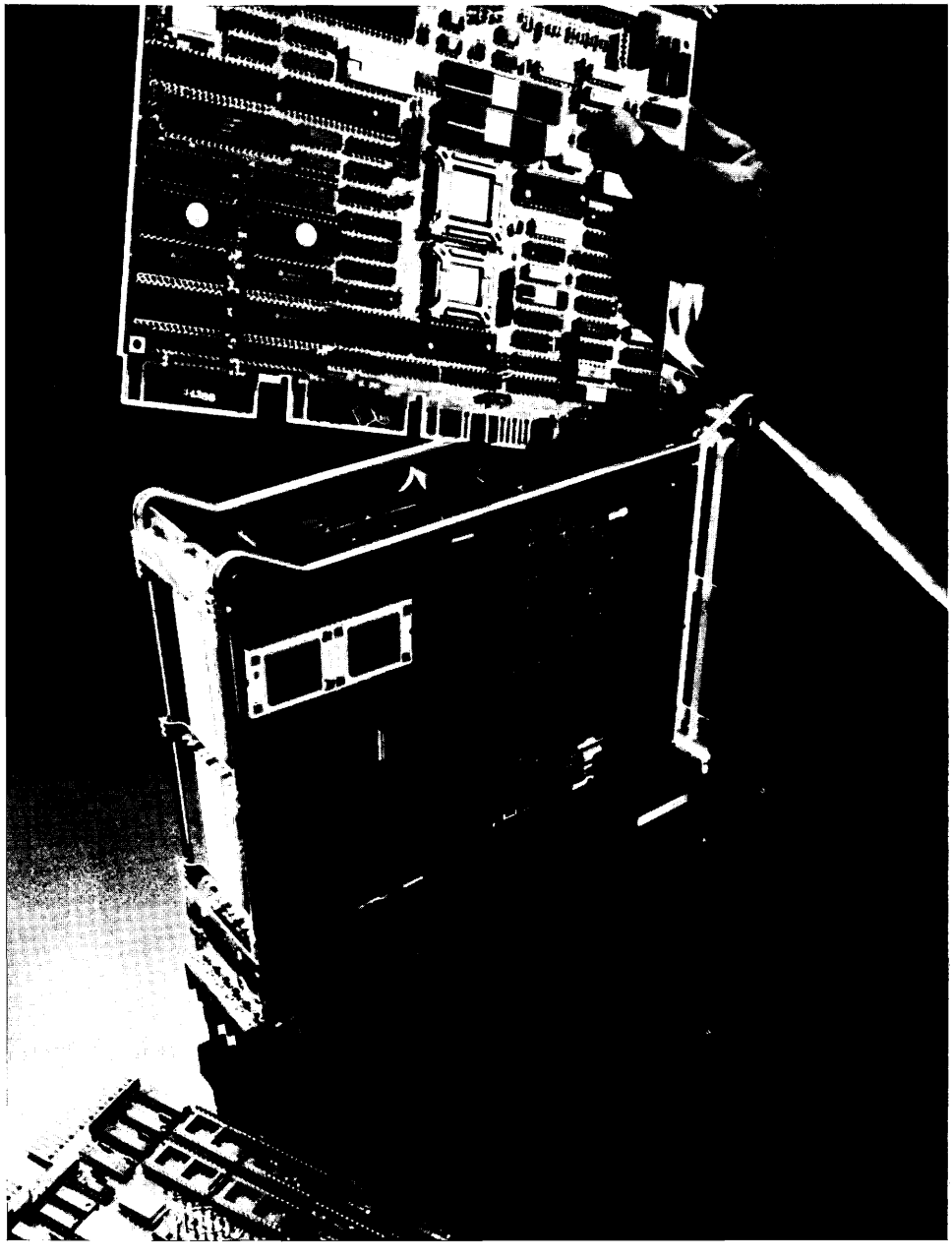
This handbook is a reference guide for board-level microcomputers, memories, interfaces, and peripheral options that can be installed on the Q-bus. The book is divided into ten parts (listed below) and three appendixes.

- Part I: Introduction
- Part II: Microcomputers
- Part III: Memories
- Part IV: Multifunction Modules
- Part V: Asynchronous Communications Interfaces
- Part VI: Synchronous Communications Interfaces
- Part VII: Analog Interfaces
- Part VIII: Parallel Interfaces
- Part IX: Peripheral Interfaces
- Part X: Backplanes, Enclosures, and Expansion Cables

Within Parts II through IX each module is discussed separately in an individual chapter. Following a brief description of the module, each chapter includes specification, configuration, and (where appropriate) cabling and cabinet kit information. The appendixes provide related information on configuration of a Q-bus system, on modules that are no longer marketed, and on chip kits.

For more information on configuring Q-bus systems including summary charts on all Q-bus module products and configuration rules, refer to the *Microcomputer Products Configuration Guide* (order number EB-27318-68).

Part I • Introduction



• The Q-bus

System components, including the processor, memory, and peripherals, are interconnected and communicate with each other via the Q-bus. The form of communication is the same for all devices on the bus; instructions that communicate with memory can communicate with peripheral devices. Each device, including memory locations and peripheral device registers, is assigned an individual byte or word address on the bus.

Master/Slave Relationship

Communication between devices on the bus is asynchronous. A master/slave relationship exists throughout each bus transaction. At any time, there is one device that has control of the bus. This controlling device is known as the bus master. The master device controls the bus while communicating with another device, known as the slave. The bus master (typically the processor or a direct memory access [DMA] device) initiates a bus transaction. The slave device responds by acknowledging the transaction in progress and by receiving data from, or transmitting data to, the bus master. Q-bus control signals transmitted or received by the bus master or slave device must complete the sequence according to bus protocol. Table 1-1 lists signals.

The processor controls bus arbitration, determining which device becomes bus master at any given time. A typical example of this relationship is the processor, as master, fetching an instruction from memory, which is always a slave. Communication on the Q-bus is interlocked so that for certain control signals issued by the master device, there must be a response from the slave in order to complete the transfer. It is this master/slave signal protocol that makes the Q-bus asynchronous. The asynchronous operation precludes the need for synchronizing with, and waiting for, clock pulses.

Device Registers and Addresses

The Q-bus reserves the top 4 Kwords of its address space for I/O and peripheral devices. This area is known as the I/O page. Digital implements some controllers at fixed addresses within this space; other controller addresses "float," based on a particular system's configuration.

Peripheral device addresses within the I/O page are decoded by each device itself. Each peripheral includes one or more device registers, accessible under program control in exactly the same manner as memory locations. These registers (generally known as control and status registers, or CSRs) contain all the necessary information to establish communications with the device. Additional data buffer registers (DBRs) are used for temporary storage of data to be transferred into and out of the processor.

Interrupts and Device Priority

The interrupt capability of the Q-bus allows any I/O device to temporarily suspend (or interrupt) current program execution and divert processor operation to service the requesting device. Interrupts can be caused by devices connected to the Q-bus or by actions within the CPU itself. Those interrupts that originate within the CPU are called traps and are caused by programming errors, hardware errors, special instructions, or maintenance features.

When an interrupt request is received from the bus, the processor completes execution of the present instruction, saves the program counter (PC) and processor status (PS) words on the stack and acknowledges the interrupt. The highest priority device requesting interrupt service responds by inputting its interrupt vector address to the processor. The processor uses this vector address as a pointer to two memory locations containing the starting address (PC) and processor status (PS) of the device's interrupt service routine. Program control is transferred to the service routine. Once the service routine has completed execution, control is either returned to the previously interrupted program or transferred to the service routine of the next device requesting interrupt service.

The Q-bus supports the following two methods of establishing device priority:

- Distributed arbitration — priority levels are implemented on the hardware. When devices of an equal priority level request an interrupt, priority is given to the device electrically closest to the processor.
- Position-defined arbitration — priority is determined solely by electrical position on the bus. The closer a device is to the processor, the higher its priority.

Q-bus Addressing

The Q-bus supports 16-, 18-, or 22-bit addresses. However, processors and peripherals having 22-bit addressing capabilities are completely PDP-11 software- and hardware-compatible within the 18-bit or 16-bit limitation. Similarly, 18-bit addressing devices are compatible within the 16-bit limitation. This is true because of the manner in which peripheral devices are addressed within a Q-bus system.

As mentioned above, all peripheral device addresses are located within the I/O page, regardless of the addressing mode of the bus. When the I/O page is addressed, the processor must assert the "bank 7 select" (BBS7) bus signal. All peripheral devices use this signal line during addressing rather than decoding the upper address bits. An asserted BBS7 signal always indicates an address in the I/O page, thereby enabling peripheral device addressing.

It should be noted, however, that memories or I/O devices that are not capable of 22-bit addressing can generate or decode erroneous addresses if they are used in systems that implement 22-bit addressing. Such devices can be used in a 22-bit system only if the size of the system is restricted to the address range of the device.

For more detailed information on the Q-bus, refer to the *PDP-11 Architecture Handbook.*

Q-bus Signal and Pin Identification

The Q-bus is based on the use of dual-height modules that plug into a 2-slot bus connector. Each slot contains 36 lines — 18 each on the component and solder sides of the circuit board — making a total of 72 contact pins carrying 72 individual signals. These contact pins are identified in the following fashion:

- The two slots are designated A or B — matching rows A and B on the module (as shown in Figure 1-1).
- The component side of the module is designated side 1 and the solder side is designated side 2.
- The 18 pins on each side of each slot (or row) are identified using letters A through V (excluding G, I, O, and Q).

An actual pin identifier has the format "slot/pin/side." For example, pin AA1 is the first pin of slot A, side 1; pin BE2 is the fifth pin of slot B, side 2; and pin BV1 is the eighteenth pin of slot B, side 1.

Table 1-1 lists the bus pins, along with the mnemonic and description of their associated signals.

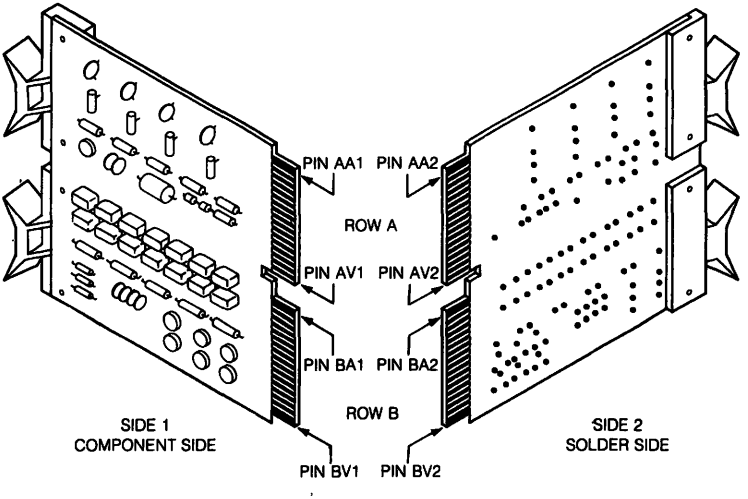


Figure 1-1 ▪ Dual-Height Module Contact Pin Identification

Table 1-1 ▪ Q-bus Signal and Pin Identifiers

Pin	Mnemonic	Description
AA1	BIRQ5	Interrupt Request Priority Level 5
AB1	BIRQ6	Interrupt Request Priority Level 6
AC1	BDAL16	Extended address bit during addressing protocol; memory error data line during data transfer protocol
AD1	BDAL17	Extended address bit during addressing protocol; memory error logic enable during data transfer protocol

(continued on next page)

Table 1-1 ▪ Q-bus Signal and Pin Identifiers (Cont.)

Pin	Mnemonic	Description
AE1	SSPARE1 (Alternate +5B)	Special Spare—not assigned or bused in Digital cable or backplane assemblies; available for user connection. Optionally, this pin can be used for +5 V battery (+5B) backup power to keep critical circuits alive during power failures. A jumper is required on Q-bus options to open (disconnect) the +5B circuit in systems that use this line as SSPARE1.
AF1	SSPARE2	Special Spare—not assigned or bused in Digital cable or backplane assemblies; available for user connection. In the highest-priority device slot, the processor can use this pin for a signal to indicate its RUN state.
AH1	SSPARE3 and SRUN (simultaneously)	Special Spare—not assigned or bused in Digital cable or backplane assemblies; available for user connection. An alternate SRUN signal can be connected in the highest-priority slot.
AJ1	GND	Ground—System signal ground and dc return
AK1 AL1	MSPAREA MSPAREB	Maintenance Spares—normally connected together on the backplane at each option location (not a bused connection)
AM1	GND	Ground—System signal ground and dc return

(continued on next page)

Table 1-1 ▪ Q-bus Signal and Pin Identifiers (Cont.)

Pin	Mnemonic	Description
AN1	BDMR	Direct Memory Access (DMA) Request — A device asserts this signal to request bus mastership. The processor arbitrates bus mastership between itself and all DMA devices on the bus. If the processor is not bus master (it has completed a bus cycle and BSYNC is not being asserted by the processor), it grants bus mastership to the requesting device by asserting BDMGO. The device responds by negating BDMR and asserting BSACK.
AP1	BHALT	Processor Halt — When BHALT is asserted for at least 25 microseconds, the processor services the halt interrupt and responds by halting normal program execution. External interrupts are ignored but memory refresh interrupts in the LSI-11 are enabled if W4 on the M7264 and M7264-YA processor modules is removed and DMA request/grant sequences are enabled. The processor executes the ODT microcode and the console device operation is invoked.
AR1	BREF	Memory Refresh — Asserted by a DMA device. This signal forces all dynamic MOS memory units requiring bus refresh signals to be activated for each BSYNC/BDIN bus transaction. It is also used as a control signal for block mode DMA.

Note

The user must avoid multiple DMA data transfers (burst or "hog" mode) that could delay refresh operation if using DMA refresh. Complete refresh cycles must occur once every 1.6 milliseconds if required.

(continued on next page)

Table 1-1 ▪ Q-bus Signal and Pin Identifiers (Cont.)

Pin	Mnemonic	Description
AS1	+12B or +5B	+12 Vdc or +5 V Battery Backup Power to keep critical circuits alive during power failures. This signal is not bused to BS1 in all Digital backplanes. A jumper is required on all Q-bus options to open (disconnect) the backup circuit from the bus in systems that use this line at the alternate voltage.
AT1	GND	Ground—System signal ground and dc return
AU1	PSPARE1	Spare—not assigned; customer usage not recommended. Prevents damage when modules are inserted upside down.
AV1	+5B	+5 V Battery Power—Secondary +5 V power connection. Battery power can be used with certain devices.
BA1	BDCOK	dc Power OK—Power supply-generated signal that is asserted when there is sufficient dc voltage available to sustain reliable system operation.
BB1	BPOK	Power OK—Asserted by the power supply 70 milliseconds after BDCOK is negated when ac power drops below the value required to sustain power (approximately 75 percent of nominal). When BPOK is negated during processor operation, a powerfail trap sequence is initiated.
BC1 BD1 BE1 BF1	SSPARE4/BDAL18 SSPARE5/BDAL19 SSPARE6/BDAL20 SSPARE7/BDAL21	Special Spares (in 18-bit Q-bus)—Not assigned. Bused in 22-bit cable and backplane assemblies; available for user connection. (Caution: These pins may be used as test points by Digital in some options.) Address Lines <21:18> (in 22-bit Q-bus). Currently not used during data transfers.

(continued on next page)

Table 1-1 ▪ Q-bus Signal and Pin Identifiers (Cont.)

Pin	Mnemonic	Description
BH1	SSPARE8	Special Spare—Not assigned or bused in Digital cable and backplane assemblies; available for user connection.
BJ1	GND	Ground—System signal ground and dc return
BK1 BL1	MSPAREB MSPAREB	Maintenance Spares—Normally connected together on the backplane at each option location (not a bused connection).
BM1	GND	Ground—System signal ground and dc return
BN1	BSACK	This signal is asserted by a DMA device in response to the processor's BDMGO signal, indicating that the DMA is bus master.
BP1	BIRQ7	Interrupt Request Priority Level 7
BR1	BEVNT	External Event Interrupt Request—When this signal is asserted, the processor responds by entering a service routine via vector address 100. A typical use of this signal is a linetime clock interrupt.
BS1	+12B	+12 Vdc Battery Backup Power—not bused to AS1 in all Digital backplanes
BT1	GND	Ground—System signal ground and dc return
BU1	PSPARE2	Spare—Not assigned; customer usage is not recommended. If a module is using −12 V (on pin AB2) and if the module is accidentally inserted upside down in the backplane, −12 Vdc appears on this pin.
BV1	+5V	+5 V Power—Normal +5 Vdc system power
AA2	+5V	+5 V Power—Normal +5 Vdc system power

(continued on next page)

Table 1-1 ▪ Q-bus Signal and Pin Identifiers (Cont.)

Pin	Mnemonic	Description
AB2	−12V	−12 V Power—Optional −12 Vdc power for devices requiring this voltage

Note

LSI-11 modules that require negative voltages contain an inverter circuit (on the module) which generates the required voltages. Hence, −12 V power is not required with Digital-supplied options.

AC2	GND	Ground—System signal ground and dc return
AD2	+12V	+12 V Power—12 Vdc system power
AE2	BDOUT	Data Output—When asserted, BDOUT implies that valid data is available on BDAL <0:15> and that an output transfer, from the bus master device, is taking place. BDOUT is deskewed with respect to data on the bus. The slave device responding to the BDOUT signal must assert BRPLY to complete the transfer.
AF2	BRPLY	Reply—BRPLY is asserted in response to BDIN or BDOUT and during IAK transactions. It is generated by a slave device to indicate that it has placed its data on the BDAL bus or that it has accepted output data from the bus.
AH2	BDIN	Data Input—Used for two types of bus operations. When asserted at the same time as BSYNC, BDIN signals an input transfer to the current bus master and requires a response (BRPLY). The master device must deskew input data from BRPLY. When asserted without BSYNC, BDIN signals an interrupt operation.

(continued on next page)

Table 1-1 ▪ Q-bus Signal and Pin Identifiers (Cont.)

Pin	Mnemonic	Description
AJ2	BSYNC	Synchronize—BSYNC is asserted by the bus master device to indicate that it has placed an address on BDAL<0: 17>. The transfer continues until BSYNC is negated.
AK2	BWTBT	Write/Byte—BWTBT is used in two ways to control a bus cycle: It is asserted at the leading edge of BSYNC to indicate that an output sequence (rather than an input sequence) is to follow. It is asserted during BDOUT (in a DATOB bus cycle) for byte addressing.
AL2	BIRQ4	Interrupt Request Priority Level 4—A level 4 device asserts this signal when its interrupt enable and interrupt request flip-flops are set. If PS<7> is 0, the processor acknowledges the request by asserting BDIN and BIAKO.
AM2 AN2	BIAKI BIAKO	Interrupt Acknowledge—In accordance with interrupt protocol, the processor asserts BIAKO to acknowledge receipt of an interrupt. The bus transmits this to BIAKI of the device electrically closest to the processor. This device accepts the interrupt acknowledge under two conditions: (1) The device requested the bus by asserting BIRQ*x*, and (2) the device has the highest-priority interrupt request on the bus at that time. If these conditions are not met, the device asserts BIAKO to the next device on the bus. This process continues in a daisychain fashion until the device with the highest interrupt priority receives the interrupt acknowledge signal.

(continued on next page)

Table 1-1 ▪ Q-bus Signal and Pin Identifiers (Cont.)

Pin	Mnemonic	Description
AP2	BBS7	Bank 7 Select—The bus master asserts this signal to reference the I/O page (including that portion of the I/O page reserved for nonexistent memory). The address in BDAL <0:12> is the address within the I/O page.
AR2 AS2	BDMGI BDMGO	Direct Memory Access Grant—The bus arbitrator asserts this signal to grant bus mastership to a requesting device, according to bus mastership protocol. The signal is passed from the arbitrator (as BDMGO), through the bus, to BDMGI of the device electrically closest to the processor. This device accepts the grant only if it requested the bus by asserting BDMR. If not, the device passes the grant to the next device on the bus. The process continues until the requesting device acknowledges the grant.
AT2	BINIT	Initialize—This signal is used for system reset. When BINIT is asserted, all devices on the bus are required to return to a known, initial state (i.e., all registers and logic are set to zero). Any exceptions should be completely documented in programming and engineering specifications for the device.
AU2 AV2	BDAL0 BDAL1	Data/Address Lines—These two lines are part of the 16-line data/address bus over which address and data information are passed. (See BDAL2 through BDAL15.)
BA2	+5V	+5 V Power—Normal +5 Vdc system power
BB2	−12V	−12 V Power—Optional −12 Vdc power for devices requiring this voltage.

(continued on next page)

Table 1-1 ▪ Q-bus Signal and Pin Identifiers (Cont.)

Pin	Mnemonic	Description
BC2	GND	Ground—System signal ground and dc return
BD2	+12V	+12 V Power—12 Vdc system power
BE2	BDAL2	Data/Address Lines—These 14 lines are part of the 16-line data/address bus over which address and data information are passed. Address information is first placed on the bus by the bus master device. The same bus lines are then used for the actual data transfer.
BF2	BDAL3	
BH2	BDAL4	
BJ2	BDAL5	
BK2	BDAL6	
BL2	BDAL7	
BM2	BDAL8	
BN2	BDAL9	
BP2	BDAL10	
BR2	BDAL11	
BS2	BDAL12	
BT2	BDAL13	
BU2	BDAL14	
BV2	BDAL15	

Note

All of the above signals are asserted LOW, with the exception of BDCOK and BPOK that are asserted HIGH.

▪ Specifications

Individual module specifications are included in each module chapter. These specifications include (at least) the following characteristics:

- Identification

  The module identification is the number assigned to each module. This number is printed on the module handle and can be used as a quick reference to determine what specific options are installed in a given system.

- Size

  Q-bus-compatible modules are standardized as either dual- or quad-height modules. The standard dimensions for each size module (shown in Figure 1-2) are as follows:

Dual:	13.2 cm (5.2 in) high
	22.8 cm (8.9 in) long
	1.27 cm (0.5 in) thick
Quad:	26.5 cm (10.5 in) high
	22.8 cm (8.9 in) long
	1.27 cm (0.5 in) thick

- Power Requirements

  The power requirements specify the power used by the option when connected to the Q-bus backplane. These requirements are used to determine the total power supply loading within a single system.

- Bus Loads

  The bus loads for ac and dc loading are provided so that the user can calculate the total loading for the system. The dc load is a measure of the leakage current a module's bus signal lines draw when high (undriven). One dc load is nominally 210 μA. The ac load is a measure of the capacitance a module adds to the bus signal lines. One ac load is 9.35 pF.

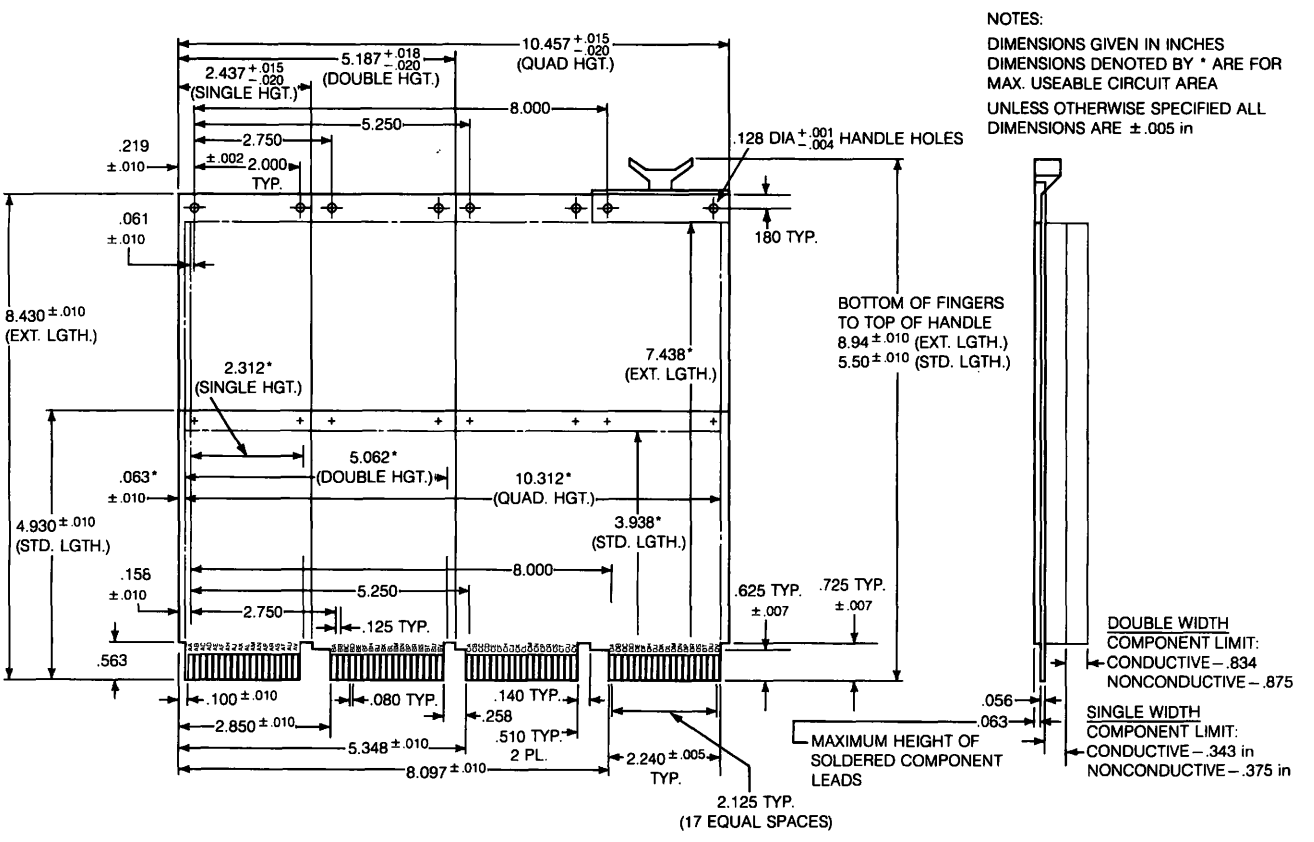


Figure 1-2 ■ Q-bus Module Dimensions

Most Q-bus modules are designed to operate within the environmental specifications listed in Table 1-2. Any module characteristics that do not meet or that exceed this set of specifications are listed in the individual module chapters.

Table 1-2 ▪ Q-bus Environmental Specifications

Temperature	
Storage	-40°C to 66°C (-40°F to 150°F)
Operating	5°C to 60°C (41°F to 140°F)

Note

The module must be brought into the operating environment and be allowed to stabilize at the operating temperature for a minimum of 5 minutes before operating.

Relative Humidity	
Storage	10% to 90%, noncondensing
Operating	10% to 90%, noncondensing
Wet bulb temperature	28°C (82°F) maximum
Dew point	2°C (36°F) minimum
Altitude	
Storage	Up to 15 km (50,000 ft)
Operating	Up to 15 km (50,000 ft) (90 mm mercury minimum)

Note

Lower the maximum operating temperature by one Celsius degree (1.8 Fahrenheit degrees) for each 305 m (1,000 ft) of altitude above 2.4 km (8,000 ft).

Air Quality	Air must be noncaustic.

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Table 1-2 ▪ Q-bus Environmental Specifications (Cont.)

Airflow (operating)	There must be enough airflow to limit the input to output temperature rise across the module to five Celsius degrees (nine Fahrenheit degrees) when the input temperature is 60°C (140°F). For operation below 55°C (131°F), there must be enough airflow to limit the input to output temperature rise across the module to 10 Celsius degrees (18 Fahrenheit degrees) maximum.

Note

These are design limits. Lower temperature limits will help increase the life of the module.

▪ Cabling and Cabinet Kits

Digital has implemented a design for shielding cabinets and cabling to reduce the potential of electromagnetic interference from computer devices. This new system is made up of three parts:

- A shielded CPU enclosure and an internal cable that originates at the option module or controller.
- A shielded I/O connection panel that joins the internal and external cables and provides the transition between option modules and externally connected devices.
- An external cable that attaches to the peripherals.

The I/O connection panel completes the shielding envelope and provides the filtering necessary to contain potential radio frequency interference within the cabinet. All cables entering or exiting the cabinet must do so via the I/O connection panel. (See Figure 1-3.)

Where appropriate, each module chapter contains information concerning available cabinet kits and external cables for use with the module.

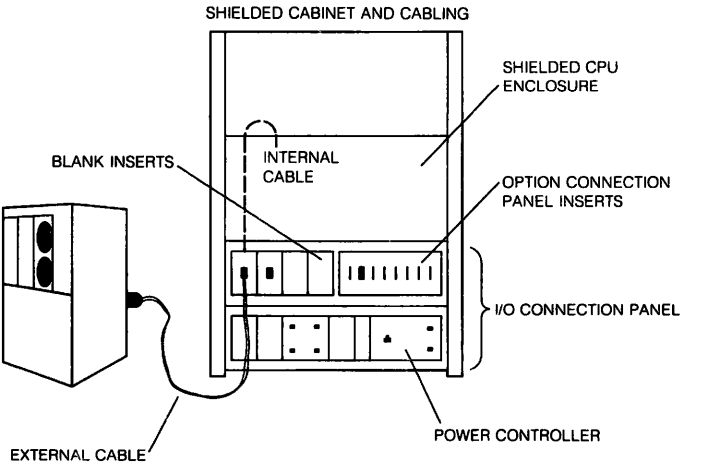
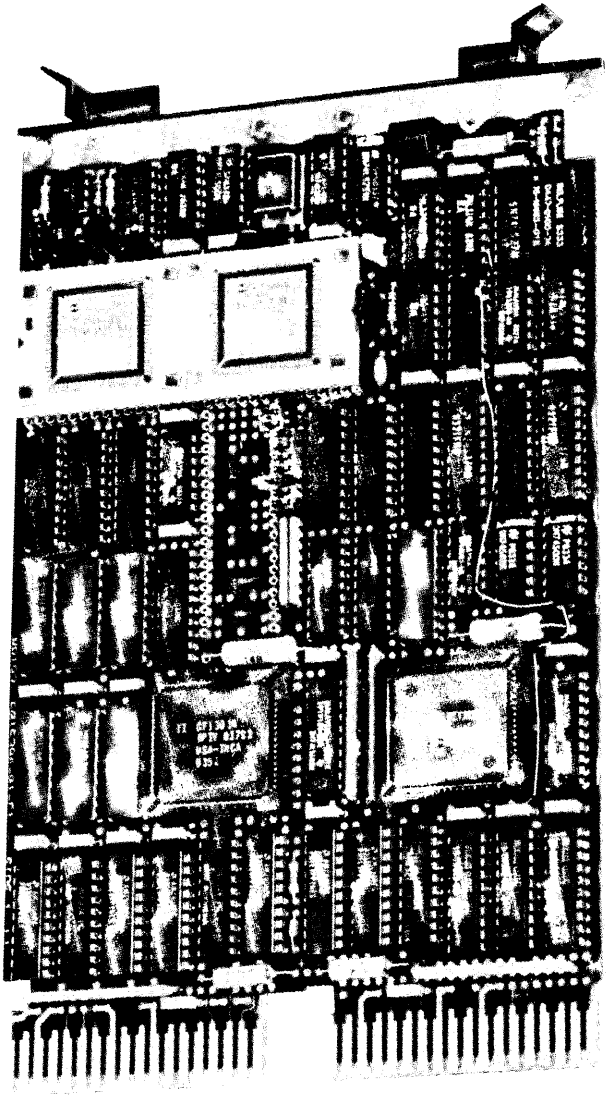


Figure 1-3 ▪ Cabling and Cabinet Kits



Chapter 2 ▪ Introduction to Microcomputers

The Digital Q-bus microcomputer family consists of a set of compatible processors that use a common architecture and a common instruction set. These processors are connected to the Q-bus backplane as a subsystem that executes programs and arbitrates usage of the Q-bus for peripherals.

Note

The KXT11-CA is unique among the processors listed here. While it implements the Q-bus specifications as a bus slave, it is incapable of arbitrating the bus. As a DMA device, however, it can become bus master to transfer data when the arbiter grants the bus. In this mode it serves as an intelligent peripheral or as an I/O processor module (IOP). It can also be used as a single-board computer (SBC) in a stand-alone fashion.

Features common to all Q-bus microcomputers include the following:

- The PDP-11 instruction set, providing powerful and convenient programming.
- Direct addressing of 16-bit words or 8-bit bytes, providing flexibility in defining data structures.
- Twelve addressing modes for specifying operands, permitting absolute, deferred, autoincrement, autodecrement, and index register references.
- Six general purpose and two special purpose internal registers for use as accumulators and for operand addressing, providing flexible programming techniques.
- Stack processing, providing convenient handling of structured data, subroutines, and interrupts.
- Byte-oriented instructions, permitting efficient processing of 8-bit characters without the need to rotate, swap, or mask.
- Q-bus interface, allowing communication with all Q-bus compatible products.
- Direct memory access (DMA), allowing peripherals to access memory without interrupting processor operation.

- Vectored interrupts, providing fast interrupt response without device polling.
- Powerfail/autorestart hardware that detects and protects against ac power fluctuations.
- Compact, modular component design, providing versatile packaging and allowing systems to be configured and upgraded easily.
- Asynchronous bus operation, allowing processor and system components (memory and peripherals) to run at their highest possible speeds.

Additional features available on selected Q-bus microcomputers include the following:

- ODT console emulator, providing ease of debugging.
- Recognition of memory parity errors during every data-in bus cycle providing overall system integrity.
- The extended integer instruction set (EIS) and the floating-point instruction set (FP11 on processors such as the KDJ11-A or the KDF11 with KEF11), providing fixed and floating-point hardware arithmetic.
- Multilevel interrupt bus structure, allowing the priority of bus operation for each level to be conveniently determined by their physical locations on the bus.
- Extended addressing to support more users per system and provide increased system performance.
- Memory management, allowing relocation and protection needed in multitask environments.
- Built-in expansion capability, eliminating the need for an expander box.
- Line-frequency clock, providing the system with timing information at fixed intervals.
- Powerup self-test diagnostics to provide assurance of proper module operation.

See the *PDP-11 Architecture Handbook* for a detailed discussion of these and other features.

There are five board-level Q-bus microcomputers. Table 2-1 summarizes the features of each of these processors.

Table 2-1 ▪ Board-Level Microcomputer Summary/Comparison Chart

	LSI-11/23 KDF11-AA	LSI-11/23+ KDF11-BA	LSI-11/73 KDJ11-AA	FALCON+ KXT11-AB	I/O PROC KXT11-CA
Q-bus addressing	22-bit	22-bit	22-bit	16-bit	22-bit
Memory capacity	4 Mbytes	4 Mbytes	4 Mbytes	64 Kbytes	64 Kbytes
Memory management	yes	yes	yes	no	no
Q-bus interrupts	4-level	4-level	4-level	1-level	not applicable
FIS instruction set	no	no	no	no	no
FP11 instruction set	optional	optional	yes	no	no
EIS instructions	yes	yes	yes	no	no
Memory parity check	yes	yes	yes	no	no
Line-frequency clock	no	yes	no	yes	yes
Self-test diagnostics	no	yes	no	no	yes
Expansion capability	yes	yes	yes	yes	no
Onboard serial I/O	no	2 ports	no	2 ports	3 ports
Onboard parallel I/O	no	no	no	24-line	20-line
Onboard memory	no	no	no	yes	yes
Onboard cache	no	no	yes	no	no
ODT microcode	yes	yes	yes	no	no
ODT firmware	no	no	no	yes	yes

Chapter 3 ▪ KDF11-AA LSI-11/23 Microcomputer

The LSI-11/23 microcomputer (KDF11-AA) is capable of addressing up to four megabytes of main memory. It offers memory management (the KTF11-AA), a microcoded FP11 floating-point instruction set (the KEF11-AA), and a floating-point accelerator module (the FPF11) as options. The KEF11-AA and the FPF11 options are mutually exclusive; only one can be installed at a time. Table 3-1 lists the available LSI-11/23 configurations.

Table 3-1 ▪ LSI-11/23 Configurations

Model Number	Description
KDF11-AC	LSI-11/23 CPU without memory management, one dual module
KDF11-AA	LSI-11/23 CPU with memory management, one dual module; includes KDF11-AC, KTF11-AA
KDF11-HK	LSI-11/23 CPU, 256-Kbyte RAM, five dual modules; includes KDF11-AA, (4) MSV11-DD
KDF11-LK	LSI-11/23 CPU, 256-Kbyte parity memory, two dual modules; includes KDF11-AA, MSV11-LK
KEF11-AA	Floating-point option for KDF11-AA, one 40-pin package
KTF11-AA	Memory management option for LSI-11/23 CPU, one 40-pin package

▪ Specifications

Identification	M8186
Size	Dual
Power Requirements	+5 V ±5%, 2.0 A (typical) 3.2 A (maximum) +12 V ±5%, 0.2 A (typical) 0.6 A (maximum)
Bus Loads	
ac	2.0
dc	1.0

Performance*	
Worst Case	55.7 microseconds (for infrequently used instructions); 10.8 microseconds (for more frequently used group)
Typical	6.0 microseconds
Interrupt Service Time	8.2 microseconds
DMA Latency	3.49 microseconds (worst case)

*Timing (Based on 300-nanosecond CPU microcycle time)

Interrupt Latency (based on MSV11-D without parity, add 500 ns worst case with parity)

▪ Related Documentation

Document Title	Order Number
KDF11-AA User's Guide	EK-KDF11-UG
LSI-11/23 Processor Configuration Sheet	EK-KDFAA-CG
LSI-11/23 Data Sheet July 1981	ED-2136-20
LSI-11/23 High Performance (KDF11-AA)	ED-18325-53
LSI-11/23 (PDP-11/23) Reference Card	EH-17898-20
Field Maintenance Print Set	MP-00734-00

▪ Configuration

Several jumpers on the processor module provide user-selectable features. Table 3-2 lists the jumper configurations. Figure 3-1 shows the Rev A board jumper locations, and Figure 3-2 shows the Rev C board jumper locations. Jumpers not discussed are reserved for use by Digital and should not be used.

Table 3-2 ▪ LSI-11/23 Jumper Configurations

Jumper	Name	In	Out
W1	Master clock	Enable internal master clock	Do not remove—manufacturing use only
W2	Reserved for Digital use	Factory-installed	Do not remove
W4	Event line enable	Disabled	Enabled
W5, W6	Powerup mode selector	See text	See text
W7	Halt/trap option	Trap to 10_8 on halt	Enter console ODT on halt

(continued on next page)

Table 3-2 ▪ LSI-11/23 Jumper Configurations (Cont.)

Jumper	Name	In	Out
W8	Conventional bootstrap start address, enable if powerup mode 2 is selected	Powerup to bootstrap address 173000_8	Powerup to bootstrap address selected by jumpers W9-W15
W9-W15	User-selectable bootstrap starting address for powerup mode 2	See text	See text
W16	Reserved for Digital use	Must be installed	Do not remove
W17	Reserved for Digital use	Must be installed	Do not remove
W18	Wakeup circuit	Disabled	Enabled

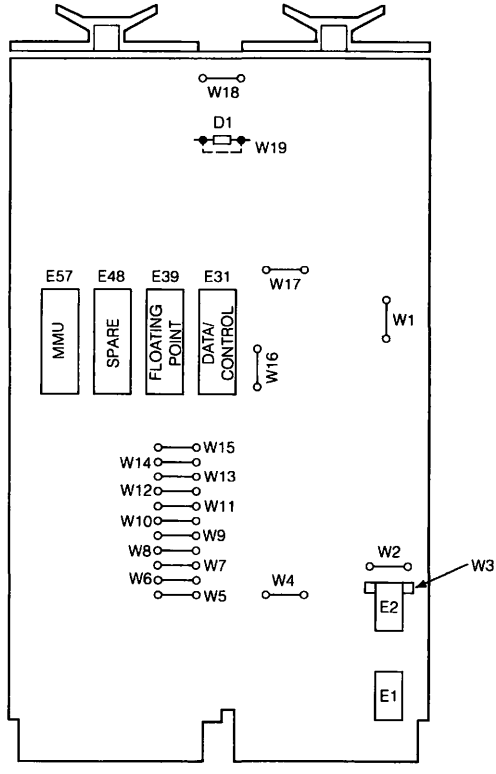


Figure 3-1 ▪ LSI-11/23 Jumper Locations (Rev. A)

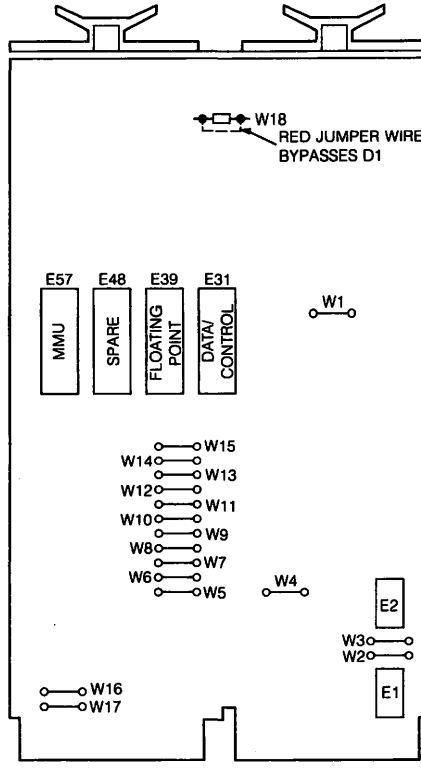


Figure 3-2 ▪ LSI-11/23 Jumper Locations (Rev. C)

Master Clock — W1

The internal 13.8 MHz oscillator is disconnected from the clock circuitry if W1 is removed. This jumper is used by Digital manufacturing and is not to be removed by the user.

Event Line — W4

The bus signal BEVNT causes the event line flip-flop to be set. When the processor enters the service state, the request will be honored if the PS <07:05> is 5 or less. (BEVNT is a level 6 interrupt.) This causes the microcode to clear the request flip-flop and trap to the line clock vector (location 100_8). If W4 is inserted, the request flip-flop is disabled and therefore the BEVNT signal is disabled. In most cases, users would disable BEVNT, which is normally used as a 60 Hz realtime clock, if they have a programmable clock on the Q-bus.

Powerup Mode Selection—W5 and W6

Four powerup modes are available for user selection. Selection is made by removal or insertion of jumpers W5 and W6 as shown in the following table.

Mode	Name	W6	W5
0	PC @24, PS @26	R	R
1	Console ODT	R	I
2	Bootstrap	I	R
3	Extended Microcode	I	I

I = jumper installed; R = jumper removed.

Only the powerup mode is affected—not the powerdown sequence. The following subsections describe the sequence of events after executing common powerup, when selecting each of the four modes. The state of bus signal BHALT is significant in powerup mode operation. Table 3-3 lists powerup mode console printout.

Table 3-3 ▪ LSI-11/23 Console Powerup Printout (or Display)

Mode	BHALT Unasserted	BHALT Asserted
0	Processor will execute program using contents of location 24 as the PC value.	Terminal will print out contents of memory location 24.
1	Terminal will print out a random 6-digit number—the contents of the program counter.	Terminal will print out a random 6-digit number—the contents of the program counter.
2	Processor will execute program at location 173000_8.*	Terminal will print out 173000.*
3	No printout at terminal.†	No printout at terminal.‡

* Normal mode for use with the MXV11 options.If jumpers W15 through W9 are used, that address will be printed.

† If mode 3 is selected and user microcode is not implemented, the processor will trap to memory location 10 and start program execution using the contents of location 10 as the PC value and the contents of location 12 as the PS value.

‡ The terminal printout will consist of six octal digits as specified in the table, followed by a carriage return, line feed, and "@" prompt character in all cases.

- POWERUP MODE 0 (PC @24, PS @26)

  This mode causes the microcode to fetch the contents of memory locations 24_8 and 26_8 and loads their contents into the PC and PS, respectively. The microcode then examines BHALT. If BHALT is asserted, the processor enters console ODT mode. If BHALT is not asserted, the processor begins program execution by fetching an instruction from the location pointed to by the PC. This mode is useful when the power-fail/autorestart capability is desired.

- POWERUP MODE 1 (CONSOLE ODT)
  This mode causes the processor to enter console ODT mode immediately after powerup, regardless of the state of any service signals. This mode is useful in a program development or hardware debug environment, giving the user immediate control over the system after powerup.

- POWERUP MODE 2 (USER BOOTSTRAP STARTING ADDRESS SHOWN BY W8-W15)
  This mode causes the processor to generate a bootstrap starting address internally by looking at jumpers W8 through W15. This address is loaded into the PC. The processor sets the PS to 340_8 (PS <07:05> = 7_8) to inhibit interrupts before the processor is ready for them. If BHALT is asserted, the processor enters console ODT mode. If not, the processor begins execution by fetching an instruction from the location pointed to by the PC. This mode is useful for turnkey applications where the system automatically begins operation without operator intervention.

- POWERUP MODE 3 (USER MICROCODE—FOR FUTURE USE)
  This mode causes the microcode to jump to optional control chip 37_8, location 76_8, and begin microcode execution. This mode is reserved for future Digital use and is not recommended for customer use. If it is erroneously selected, the processor will treat it as a reserved instruction trap to location 10_8.

Halt/Trap Option—W7

If the processor is in kernel mode and decodes a HALT instruction, BPOK is tested. If BPOK is negated, the processor will continue to test for BPOK. The processor will perform a normal powerup sequence if BPOK becomes asserted sometime later. If BPOK is asserted after the HALT instruction decode, the halt/trap jumper (W7) is tested. If the jumper is removed, the processor enters console ODT mode. If the jumper is installed, a trap to location 10_8 will occur.

Note

In user mode, a HALT instruction execution always results in a trap to location 10_8.

This feature is intended for situations, such as unattended operation, in which recovery from erroneous HALT instructions is desirable.

Starting Address 173000_8 — W8

When powerup mode 2 is selected, the processor examines jumper W8 to determine the starting address for program execution. If W8 and a compatible bootstrap module are installed in the system, the microcode will begin execution at 173000_8 (the conventional starting address for Digital systems). If W8 is removed, a trap to 4_8 (nonexistent address) will occur. If W8 is removed, the processor looks at jumpers W9 through W15 for the starting address.

Selectable Starting Address — W9 through W15

If the user wishes to start execution from an address other than 173000_8, jumpers W9 through W15 can be used to specify the high byte <15:09> of the starting address. Jumpers W15 through W9 correspond to address bits <15:09>, respectively. Bits <08:00> of the starting address are set to 0 by the processor. Jumpers are installed for logic 1, removed for logic 0. The starting address can reside on any 256-word boundary in the lower 32 Kbytes of memory address space.

▪ Memory Modules

Several memory modules are available for use in LSI-11/23 systems. However, modules such as MSV11 memory modules that perform memory refresh locally are required, because the LSI-11/23 does not perform memory refresh itself. Other memories will work if provision is made for refresh with some other bus option. However, this will degrade system performance and is not recommended.

▪ Peripheral Options

DMA peripherals should be installed with the faster throughput devices physically closest to the processor and slower ones farther away. The user must ensure that faster devices have adequate access to the bus; otherwise, data drop errors may occur.

Interrupt-driven peripherals can be installed in one of the following ways. If all peripherals use the single-level scheme, they must be installed with faster interrupting devices physically closest to the processor. All current Digital Q-bus peripheral devices use this method. Future peripheral devices, or customer-designed devices, can take advantage of the new 4-level interrupt scheme. With this scheme, peripherals that are designed to perform distributed interrupt arbitration, and that are on different interrupt levels, can be installed in any order. Multiple peripherals on the same request level and peripherals that do not perform distributed arbitration must be installed with the highest priority, or faster, devices closest to the processor.

• Floating-Point Options

Two floating-point options are available, the KEF11-AA and the FPF11. These are described below.

KEF11-AA Floating Point Option
The KEF11-AA is a microcoded FP11 instruction set that resides in two chips on one 40-pin package that mounts on the CPU board. This option provides the same features as the FPF11 floating-point processor described below, but operates at a slower speed.

FPF11 Floating-Point Processor Option
The FPF11 floating-point processor is a hardware option designed to operate with the LSI-11/23 or the LSI-11/23-PLUS central processor units to execute all 46 arithmetic operations of the FP11 floating-point instruction set. The FPF11, contained in one quad-height module, executes instuctions six times faster than the KEF11-AA. The KEF11-AA and the FPF11 options are mutually exclusive.

For a complete list of the 46 floating-point instructions implemented by the floating-point processor, refer to the *PDP-11 Architecture Handbook*.

Specifications

Identification	M8188
Size	Quad
Power Requirements	+5 Vdc, 5.5 A (typical) 7.5 A (maximum)
Bus Loads	None

Related Documentation

Document Title	Order Number
FPF11 Floating-Point Processor Technical Manual	EK-FPF11-TM
FPF11 Field Maintenance Print Set	MP-01285-00

Configuration
When installed in the backplane slot adjacent to the LSI-11/23 or LSI-11/23-PLUS CPU (as illustrated in Figures 3-3 and 3-4), the FPF11 becomes an integral part of the CPU. The module connects to the CPU by a ribbon cable that plugs into the socket normally designated for the optional KEF11-AA floating-point processor chip. The FPF11 receives only power, not signals, from the backplane. The module operates from a single +5.0 Vdc source. The FPF11 also receives + 12 Vdc over the ribbon cable that plugs into the floating-point chip socket on the processor. This option is independent of the type of bus used by the processor. The FPF11 does not connect to the system bus, and has no effect on bus loading.

Before installing the FPF11, run system diagnostics to verify that the system receiving the option is working properly. Then, to ensure proper bus grant continuity, configure the jumpers as indicated in Table 3-4. Refer to Figure 3-5 for the locations of the jumpers on the FPF11.

	SLOT A	SLOT B	SLOT C	SLOT D
ROW 1	CPU			
ROW 2	FPF11		M8188	
ROW 3	OPTION 3		OPTION 4	
ROW 4	OPTION 6		OPTION 5	

VIEW IS FROM MODULE SIDE OF CONNECTORS

Figure 3-3 ▪ FPF11 Module in LSI-11/23 System

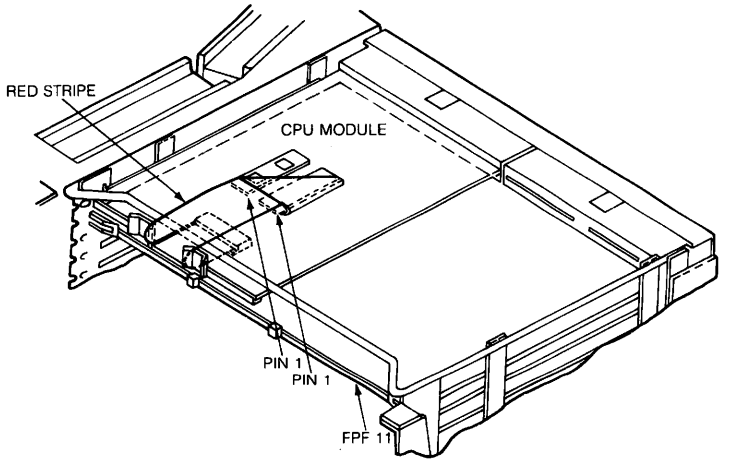


Figure 3-4 ▪ FPF11 Cable Layout in LSI-11/23 System

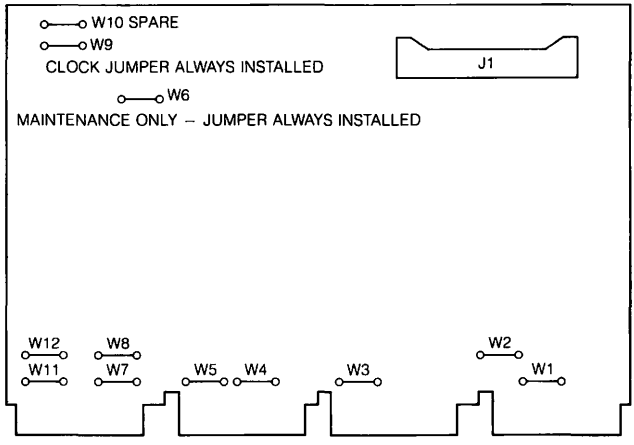


Figure 3-5 ▪ FPF11 Jumper Locations

Table 3-4 ▪ FPF11 Jumper Configurations

W1	W2	W3	W4	W5	W6	W7	W8	W9	W10	W11	W12
I	I	R	I	I	I	R	R	I	I	R	R

I = jumper installed; R = jumper removed

▪ Cabinet Kits

The following cabinet kits are available for use with the various models of the LSI-11/23 microcomputer:

CK-KDF1B-KA	For use with the BA23 enclosure (includes a selectable baud switch)
CK-KDF1B-KB	For use with the BA11-M enclosure (includes a selectable baud switch)
CK-KDF1B-KC	For use with the H349 distribution panel (includes a selectable baud switch)
CK-KDF2B-KB	For use with the BA11-M enclosure (does not include a selectable baud switch)

Chapter 4 • KDF11-B LSI-11/23-PLUS Microcomputer

The LSI-11/23-PLUS microcomputer (KDF11-B) contains a BDV11-compatible diagnostic and bootstrap ROM, a linetime clock (LTC), two asynchronous serial lines, a memory management unit (the KTF11-AA), and three sockets for the optional Commercial Instruction Set (KEF11-BB) and/or floating-point instruction set options (the KEF11-AA or FPF11). It can address up to four megabytes of main memory.

There are three variations of the KDF11-B. Each variation contains a different diagnostic/bootstrap ROM, supporting various bootable devices, as listed in Table 4-1.

Table 4-1 • KDF11-B Variations

Supported Devices	KDF11-BA	KDF11-BE	KDF11-BF
RX01	yes	yes	yes
RX02	yes	yes	yes
TU58	yes	yes	yes
RL01/2	yes	yes	yes
MRV11-C	yes	no	no
RX50	no	yes	yes
RD51	no	yes	yes
RD52	no	no	yes
TSV05	no	no	yes
TK25	no	no	yes
RC25	no	no	yes
DEQNA	no	no	yes
DLVE1	yes	no	no
DLV11-F	yes	no	no
DUV11	yes	no	no

▪ Specifications

Identification	M8189
Size	Quad
Power Requirements	+5 V ±5%, 6.4 A maximum (4.5 A typical) +12 V ±5%, 0.7 A maximum (0.3 A typical)
Bus Loads	
ac	2
dc	1
Performance	
Instruction Timing	Based on 75 ns intervals
Interrupt Latency	5.7 microseconds (typical) 12.6 microseconds (maximum), except EIS 54.225 microseconds (maximum), including EIS
Interrupt Service Time	8.625 microseconds (memory management off) 9.750 microseconds (memory management on)
DMA Latency	1.35 microseconds (maximum)

Note

Interrupt and DMA latencies assume a KDF11-B with memory management enabled and using MSV11-P Memory.

Nonstandard Environmental Specifications	
Operating temperature	5°C to 50°C (41°F to 122°F)
Operating altitude	Up to 2.44 km (8,000 ft)

▪ Related Documentation

Document Title	Order Number
KDF11-B CPU Module User's Guide	EK-KDFEB-UG
PDP-11/23B Mounting Box Technical Manual	EK-23BMB-TM
PDP-11/23B Mounting Box User's Guide	EK-23BMB-UG
KDF11-BA Field Maintenance Print Set	MP-01236-00
11/23-B Field Maintenance Print Set	MP-01234-00
11T23-B Field Maintenance Print Set	MP-01235-00

Configuration

Jumper and Switch Configuration

The LSI-11/23-PLUS contains two dual inline pack (DIP) switchpacks (E102 and E114) and several jumpers that allow the user to select the module features desired. The location of the switchpacks and jumpers is shown in Figure 4-1. The boot/diagnostic switchpack (E102) consists of eight switches that let the user select boot and diagnostic programs. The second switchpack (E114) selects the baud rate for the console SLU and the second SLU. The module contains both wirewrap jumper pins and soldered-in jumpers. The jumpers are divided into the following functional groups:

- Test jumpers
- CPU option jumpers
- Device selection jumpers
- Boot and diagnostic ROM jumpers
- SLU character format jumpers
- Internal/external SLU clock jumpers
- Q-bus backplane jumpers

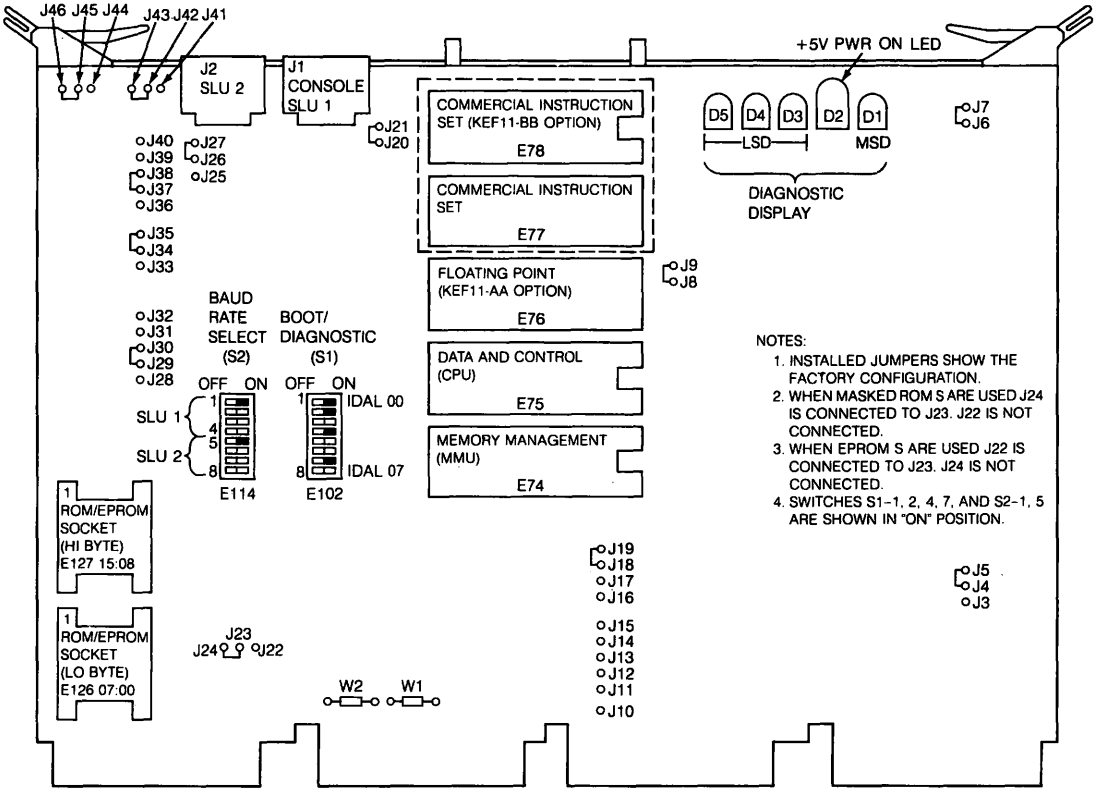


Figure 4-1 ■ LSI-11/23-PLUS Jumper and Switch Locations

Manufacturing Test Jumpers

Five jumpers are provided for manufacturing testing purposes. These jumpers must be configured as shown in Table 4-2 for normal operation.

Table 4-2 ▪ LSI-11/23-PLUS Manufacturing Test Jumpers

From	To	Status
J6	J7	Installed
J8	J9	Installed
J20	J21	Installed
J35	J34	Installed
J33	J34	Removed
J27	J26	Installed
J25	J26	Removed

CPU Option Jumpers

Four wirewrap pins provide user-selectable features associated with the operation of the CPU. The ground pin can be connected to any combination of the other three pins to select the available features. Two powerup mode pins select one of three powerup modes. The halt/trap pin selects the halt/trap options.

Powerup Mode Selection

Three powerup modes are available for user selection. Selection is made by installing or removing wirewrap jumpers between jumper pins (J17, J19) and the ground pin (J18) in various combinations. The jumper configurations for the modes are described in Table 4-3 below.

Table 4-3 ▪ LSI-11/23-PLUS Powerup Mode Jumpers

Mode	Name	J18 to J19	J18 to J17
0	PC @24, PS @26	Removed	Removed
1	Console ODT	Removed	Installed
2	Bootstrap	Installed	Removed
3	Not Implemented	Installed	Installed

Only the powerup mode is affected—not the power-down sequence. The following subsections describe the sequence of events after executing common powerup for each of the four modes. The state of bus signal BHALT is significant in powerup mode operation.

- POWERUP MODE 0 (PC @24, PS @26)
  This mode causes the microcode to fetch the contents of memory locations 24_8 and 26_8 and loads their contents into the PC and PS, respectively. The microcode then examines BHALT. If BHALT is asserted, the processor enters console ODT mode. If BHALT is not asserted, the processor begins program execution by fetching an instruction from the location pointed to by the PC. This mode is useful when the power-fail/autorestart capability is desired.

- POWERUP MODE 1 (CONSOLE ODT)
  This mode causes the processor to enter console ODT mode immediately after powerup regardless of the state of any service signals. This mode is useful in a program development or hardware debug environment, giving the user immediate control over the system after powerup.

- POWERUP MODE 2 — START AT 773000
  This mode causes the processor to generate internally a bootstrap starting address of 773000_8 in 16-bit mode with the memory management unit off. This address is loaded into the PC. The processor sets the PS to 340_8 (PS <07:05> = 7) to inhibit interrupts before the processor is ready for them. If BHALT is asserted, the processor enters console ODT mode. If not, the processor begins execution by fetching an instruction from the location pointed to by the PC. This mode is useful for turnkey applications where the system automatically begins operation without operator intervention.

Halt/Trap Option — J16

If the processor is in kernel mode and decodes a HALT instruction, BPOK is tested. If BPOK is negated, the processor will continue to test for BPOK. The processor will perform a normal powerup sequence if BPOK becomes asserted sometime later. If BPOK is asserted after the HALT instruction decode, the halt/trap jumper (J16) is tested. If the jumper is removed, the processor enters console ODT mode. If the jumper is connected to J18 (ground), a trap to location 10_8 will occur.

Note

In user mode, a HALT instruction execution always results in a trap to location 10_8.

This feature is intended for situations, such as unattended operation, in which recovery from erroneous HALT instructions is desirable. Table 4-4 describes the halt/trap jumper functions for kernel and user processor modes.

Table 4-4 ▪ LSI-11/23-PLUS Halt/Trap Jumpers

Jumper J18 to J16	Processor Mode	Function
Removed	Kernel	Processor enters console ODT microcode when it executes a HALT instruction.
Installed	Kernel	Processor traps to location 10_8 when it executes a HALT instruction.
Installed/ Removed	User	HALT instruction decode results in a trap to location 10_8 regardless of the status of the halt/trap jumper.

Onboard Device Selection Jumpers

Six wirewrap pins on the LSI-11/23-PLUS module are used to select which onboard peripheral devices are enabled or disabled. The ground pin can be connected to any combination of the other five pins to obtain the desired configuration. The jumper functions are described in Table 4-5.

Table 4-5 ▪ LSI-11/23-PLUS Onboard Device Selection Jumpers

Wirewrap Pin Number	Function
J10	This wirewrap pin provides a ground source for the other five wirewrap pins in this group.
J11	When grounded, this signal sets the line clock interrupt enable flip-flop and allows the Q-bus BEVNT signal to request program interrupts.
J15	When grounded, this signal disables the boot/diagnostic registers, the boot/diagnostic ROMs, and the line clock register.

(continued on next page)

Table 4-5 ▪ LSI-11/23-PLUS Onboard Device Selection Jumpers (Cont.)

Wirewrap Pin Number	Function
J12	When J12 is ungrounded, the second SLU device and vector addresses are as follows: Device Addresses Interrupt Vectors RCSR 776500 Receiver 300 RBUF 776502 Transmitter 304 XCSR 776504 XBUF 776506 When J12 is grounded, the device and vector addresses are as follows: Device Addresses Interrupt Vectors RCSR 776540 Receiver 340 RBUF 776542 Transmitter 344 XCSR 776544 XBUF 776546
J13	When grounded, this signal disables the second serial line registers. When ungrounded, the device and vector addresses for the second SLU are determined by the status of the J12 jumper.
J14	When grounded, this signal disables the console serial line registers. When ungrounded, the device and vector addresses for the console SLU are as follows: Device Addresses Interrupt Vectors RCSR 776500 Receiver 300 RBUF 776502 Transmitter 304 XCSR 776504 XBUF 776506

Console SLU Switch and Jumper Configurations

Four switches of a 16-pin DIP switchpack (E114) and four jumpers provide user-selectable features associated with the operation of the console serial line unit. A jumper is available to disable the console SLU.

- CONSOLE SLU BAUD RATES

  Switches 1 through 4 of the S2 switchpack (E114) select one of 16 possible SLU baud rates if the internal baud rate generator is used as the clock source. If the module is configured to operate the SLU with an external clock, the positions of these switches are meaningless. The SLU transmits and receives at the selected baud rate. Split baud operation is not provided. The switch configurations to select any one of the available baud rates are listed in Table 4-6.

Table 4-6 • LSI-11/23-PLUS Console SLU Baud Rate Selection

Switch Position				
S2-4	**S2-3**	**S2-2**	**S2-1**	**Baud Rate**
ON	ON	ON	ON	50
ON	ON	ON	OFF	75
ON	ON	OFF	ON	110
ON	ON	OFF	OFF	124.5
ON	OFF	ON	ON	150
ON	OFF	ON	OFF	300
ON	OFF	OFF	ON	600
ON	OFF	OFF	OFF	1200
OFF	ON	ON	ON	1800
OFF	ON	ON	OFF	2000
OFF	ON	OFF	ON	2400
OFF	ON	OFF	OFF	3600
OFF	OFF	ON	ON	4800
OFF	OFF	ON	OFF	7200
OFF	OFF	OFF	ON	9600
OFF	OFF	OFF	OFF	19200

As stated previously, the UART can be configured to operate at a baud rate that is generated externally. The baud rate is input to the module from the external device through connector J1, pin 1. The jumper options are shown below.

Jumper	Internal Baud Rate	External Baud Rate	Function
J43 to J42	Installed	Removed	Connects internal baud rate generator to console SLU UART (normal configuration)
J41 to J42	Removed	Installed	Connects external clock to SLU UART

- CONSOLE SLU CHARACTER FORMATS

Five wirewrap pins select options to establish the console SLU character format. The ground pin can be connected to any combination of the other four pins to configure the character format options. Table 4-7 describes how to configure the character format.

Table 4-7 ▪ LSI-11/23-PLUS Console SLU Character Jumpers

Jumper*	Status	Character Format Option
J39 to J38	Installed	7-bit characters
	Removed	8-bit characters†
J37 to J38	Installed	One stop bit
	Removed	Two stop bits
J36 to J38	Installed	Parity check enabled
	Removed	Parity check disabled†
J40 to J38‡	Installed	Odd parity
	Removed	Even parity

* J38 is the ground source for these functions.

† If 8-bit characters are selected, parity check must be disabled.

‡ Jumper J38-J40 is meaningful only if jumper J38-J36 is installed.

Break/Halt Jumpers

Two jumpers enable and disable the break/halt feature. If this feature is enabled, the detection of a break condition by the console UART causes the processor to halt and enter the octal debugging technique (ODT) microcode. If this feature is disabled, there is no response to the break condition. Table 4-8 lists the break/halt jumper configurations.

Table 4-8 ▪ LSI-11/23-PLUS Break/Halt Jumpers

Jumper	Break Enabled	Break Disabled	Function
J5 to J4	Removed	Installed	Connects ground to RQ HLT
J3 to J4	Installed	Removed	Connects DL1FE to RQ HLT

Second SLU Switch and Jumper Configurations

The second SLU is configured much the same as the console SLU, except that a different set of switches and jumpers is used to select the available SLU features. Also, the break/halt jumper is not present. Jumpers are also available to select the second SLU, and to select the range of addresses and vectors to be used. The switch positions for the second SLU baud rates are listed in Table 4-9.

Table 4-9 ▪ LSI-11/23-PLUS Second SLU Baud Rate Selection

Switch Position				
S2-8	S2-7	S2-6	S2-5	Baud Rate
ON	ON	ON	ON	50
ON	ON	ON	OFF	75
ON	ON	OFF	ON	110
ON	ON	OFF	OFF	124.5
ON	OFF	ON	ON	150
ON	OFF	ON	OFF	300
ON	OFF	OFF	ON	600
ON	OFF	OFF	OFF	1200
OFF	ON	ON	ON	1800
OFF	ON	ON	OFF	2000
OFF	ON	OFF	ON	2400
OFF	ON	OFF	OFF	3600
OFF	OFF	ON	ON	4800
OFF	OFF	ON	OFF	7200
OFF	OFF	OFF	ON	9600
OFF	OFF	OFF	OFF	19200

The second SLU may be configured to operate at an externally generated baud rate. The baud rate is input to the module from the external device through J2, pin 1. The jumper options are shown below.

Jumper	Internal Baud Rate	External Baud Rate	Function
J46 to J45	Installed	Removed	Connects internal baud rate generator to the second SLU UART (normal configuration)
J44 to J45	Removed	Installed	Connects external clock to the second SLU UART

- SECOND SLU CHARACTER FORMATS

Five wirewrap pins select options to establish the second SLU character format. The ground pin can be connected to any combination of the other four pins to configure the character format options. The jumper pin functions are shown in Table 4-10.

Table 4-10 ▪ LSI-11/23-PLUS Second SLU Character Jumpers

Jumper*	Status	Character Format Option
J31 to J30	Installed	7-bit characters
	Removed	8-bit characters†
J29 to J30	Installed	One stop bit
	Removed	Two stop bits
J28 to J30	Installed	Parity check enabled
	Removed	Parity check disabled†
J32 to J30‡	Installed	Odd parity
	Removed	Even parity

* J30 is the ground source for these functions.

† If 8-bit characters are selected, parity check must be disabled.

‡ Jumper J32-J30 is meaningful only if jumper J28-J30 is installed.

Boot/Diagnostic Switches and Jumpers

A 16-pin DIP switchpack (E102) and two jumpers on the KDF11-B module provide switch-selectable bootstrap and diagnostic programs for hard and floppy disks or the user's own bootstrap program.

- BOOTSTRAP/DIAGNOSTIC CONFIGURATION SWITCHES

Switches S1-1 through S1-4 are used to select a diagnostic and/or a bootstrap program. Switches S1-5 through S1-8 are used in conjunction with switches S1-3 and S1-4 to select the specific bootstrap program desired.

Note

The KDF11-B will have the functionality described below only if BDV11-compatible diagnostic/bootstrap ROMs are installed in sockets E126 and E127.

Table 4-11 ▪ LSI-11/23-PLUS Bootstrap/Diagnostic Switches

Switch	Status	Function
S1-1	ON	When on, execute CPU diagnostic upon powerup or restart.
S1-2	ON	When on, execute memory diagnostic upon powerup or restart.
S1-3	OFF	When on, select DECnet boot (S1-4 through S1-7 are arguments; see Table 4-12).
S1-4	ON	When on (and S1-3 off), select console test and dialogue. When off (and S1-3 off), select turnkey boot (dispatched by S1-5 through S1-8; see Table 4-13).

Table 4-12 ▪ LSI-11/23-PLUS DECnet Boot Arguments

		Switch Positions			
Boot Device	**CSR**	**S1-4**	**S1-5**	**S1-6**	**S1-7**
DUV11	760040*	ON	X	X	X
DLVE1	775610	OFF	ON	X	OFF
DLV11-F	776500	OFF	ON	X	ON

X = Don't care

* DUV11 CSR = 760040 if there are no devices from 760010 to 760036.

All boots other than the DECnet boots listed in Table 4-12 are controlled by the bit patterns in the switches S1-5 through S1-8 or, if the console test is selected, by a mnemonic and unit number.

Table 4-13 ▪ LSI-11/23-PLUS Turnkey Bootstrap Program Selection

Switch Positions					
S1-5	**S1-6**	**S1-7**	**S1-8**	**Program Selected**	**Mnemonic***
OFF	OFF	OFF	ON	RK05 Boot	DKn n<8
OFF	OFF	ON	OFF	RL01 or RL02 Boot	DLn n<4
OFF	OFF	ON	ON	TU58 Boot†	DDn n<2
OFF	ON	OFF	OFF	RX01 Boot	DXn n<2
OFF	ON	ON	OFF	RX02 Boot	DYn n<2

* All bootstraps assume Unit #0, if not specified, and Digital- standard device addresses.

† TU58 SLU at 776500.

- BOOT AND DIAGNOSTIC ROM JUMPERS

Two 24-pin sockets (E126 and E127) are provided for the installation of 2K × 8 ROMs or EPROMs. When EPROMs are inserted in the two ROM sockets, +5 volts must be applied to pin 21 of each socket. For all other ROMs used in this option, ROM address bit 13 (BTRA 13) must be applied to pin 21. Note that Digital-supplied devices may be either ROM or EPROM type.

Jumper	**Status**	**Memory Type**
J24 to J23	Installed	ROM
	Removed	EPROM
J22 to J23	Removed	ROM
	Installed	EPROM

Q-bus Backplane Jumpers

Two soldered jumpers must be installed when the KDF11-B is used in a Q/Q-type backplane in which the Q-bus is connected to both the AB and CD connectors (see Chapter 52). Digital-supplied backplanes of this type include the H9270, H9275, and the DDV11-B. The jumpers provide continuity for the interrupt acknowledge (BIAK) and direct memory access grant (BDMG) Q-bus signals.

Jumper	**Function When Installed**
W1	Connects backplane pins CM2 and CN2 providing continuity for BIAK
W2	Connects backplane pins CR2 and CS2 providing continuity for BDMG

Note

If the KDF11-B is installed in a Q/CD backplane, such as the H9273-A, and the W1 and W2 jumpers are in, pin CM1 is shorted to CN1 and pin CR1 is shorted to CS1 on slot 2. Therefore, do not install peripherals in the slot immediately following the KDF11-B if they use these lines.

Table 4-14 • LSI-11/23-PLUS Factory Jumper Configuration

Jumper	Name	Status	Function
W1	BIAK	I	Provides backplane continuity for BIAK signal. Must be installed when a Q/Q backplane is used.
W2	BDMG	I	Provides backplane continuity for BDMG signal. Must be installed when a Q/Q backplane is used.
J22-J23	+5V	R	When EPROMs are used, jumper J24 to J23 is removed and jumper J22 to J23 is installed.
J24-J23	BTRA 13	I	Connects ROM address bit 13 to pin 21 of both ROM sockets (E126 and E127).
J3-J4	DL1 FE	R	Enables break/halt feature. The detection of a break condition by the console SLU causes the processor to halt and enter ODT.
J5-J4	DL1 FE	R	No halt on break.
J6-J7	Master clock	I	Enables internal master clock — do not remove.
J8-J9	PHASE	I	Connects PHASE signal to F11 chip clock drivers — do not remove.
J11-J10	LTC ENBJ	R	Allows BEVNT signal to request interrupts only if bit 6 in the line clock register (777546) is set.

(continued on next page)

Table 4-14 ▪ LSI-11/23-PLUS Factory Jumper Configuration (Cont.)

Jumper	Name	Status	Function
J12-J10	DL2 ADRJ	R	Selects the following device and vector addresses for the second SLU: Device CSRs: Vectors: RCSR 776500 Receiver 300 RBUF 776502 Transmitter 304 XCSR 776504 XBUF 776506
J13-J10	DL2 DISJ	R	Enables the DL2 ADRJ jumper to determine the device and vector addresses for the second SLU.
J14-J10	DL1 DISJ	R	Selects the following device and vector addresses for the console SLU: Device CSRs: Vectors: RCSR 776560 Receiver 060 RBUF 776562 Transmitter 064 XCSR 776564 XBUF 776566
J15-J10	BDK DISJ	R	Enables boot/diagnostic registers, boot/diagnostic ROMs and the line clock register.
J16-J18	TRAP OPJ	R	Enter console ODT if the processor is in kernel mode and executes a HALT instruction.
J17-J18	PUP CDOJ	R	Powerup code (bit 0) — Bootstrap powerup
J19-J18	PUP CDIJ	I	Powerup code (bit 1) — Mode 2
J20-J21	XTL	I	Connects baud rate oscillator to the baud rate generator. Removed for manufacturing test only.
J25-J26	RCV IN	R	Console loop-back test disabled.
J27-J26	XMIT OUT	I	Connects console SLU output to the console SLU connector.
J28-J30	DL2 PARJ	R	Disable second SLU character parity check.

(continued on next page)

Table 4-14 ▪ LSI-11/23-PLUS Factory Jumper Configuration (Cont.)

Jumper	Name	Status	Function
J29-J30	DL2 ST1J	I	Second SLU character contains one stop-bit.
J31-J30	DL2 CH7J	R	Second SLU character contains 8 bits.
J32-J30	DL2 ODDJ	R	Second SLU parity check disabled by DL2 ODDJ.
J33-J34	DCOKC2B	R	Installed only during manufacturing testing.
J35-J34	LINITF (1)	I	BINIT clears console SLU.
J36-J38	DLI PARJ	R	Disables console SLU character parity check.
J37-J38	DLI ST1J	I	Console SLU character contains one stop-bit.
J39-J38	DLI CH7J	R	Console SLU character contains 8 bits.
J40-J38	DLI ODDJ	R	Console parity check disabled by DLI PARJ.
J41-J42	EXT CLK1	R	Disconnects EXT CLK1 input from the console SLU.
J43-J42	INT CLK1	I	Connects baud rate clock to the console SLU.
J44-J45	EXT CLK2	R	Disconnects EXT CLK2 input from the second SLU.
J46-J45	INT CLK2	I	Connects baud rate clock to the second SLU.

Table 4-15 ▪ LSI-11/23-PLUS Bootstrap/Diagnostic Factory Switch Configuration

E102 Switch	Position	Function
S1-1	ON	Execute CPU diagnostic upon powerup or restart
S1-2	ON	Execute memory diagnostic upon powerup or restart
S1-3	OFF	DECnet boot disabled
S1-4	ON	Console test and dialog enabled
S1-5	OFF	
S1-6	OFF	
S1-7	ON	RL01/RL02 bootstrap program selected
S1-8	OFF	

Note

With the switch configuration shown, the KDF11-B will (upon powerup or restart) execute the CPU diagnostic, the memory diagnostic, and then enter the console test. If the operator wishes to terminate the memory diagnostic and immediately enter the console test, the Control/C keys must be pressed on the console terminal. If the memory test is terminated before completion, some memory locations may have wrong parity written into them.

Table 4-16 ▪ LSI-11/23-PLUS SLU Baud Rate Factory Switch Configuration

E114 Switch	Position	Function
S2-1	ON	
S2-2	OFF	Console SLU set for 9600 baud (see Table 4-6)
S2-3	OFF	
S2-4	OFF	
S2-5	ON	
S2-6	OFF	
S2-7	OFF	Second SLU set for 9600 baud (see Table 4-9)

▪ Cabinet Kits

The following cabinet kits are available for use with the KDF11-B microcomputer:

CK-KDF1B-KA	For use with the BA23 enclosure (includes a selectable baud switch)
CK-KDF1B-KB	For use with the BA11-M enclosure (includes a selectable baud switch)
CK-KDF1B-KC	For use with the H349 distribution panel (includes a selectable baud switch)
CK-KDF2B-KB	For use with the BA11-M enclosure (does not include a selectable baud switch)

Chapter 5 • KDJ11-A LSI-11/73 Microcomputer

The LSI-11/73 microcomputer (KDJ11-A) interfaces to the 22-bit Q-bus and can address up to 4 megabytes of main memory. It offers full memory management and supports block mode DMA transfers. Included with the LSI-11/73 is the FP11 floating-point instruction set. The module also contains 8 Kbytes of write-through direct map cache memory.

• Specifications

Identification	M8192
Size	Dual
Power Requirements	+5 V ±5%, 4.5 A (maximum)
Bus Loads	
ac	3.4
dc	1.0
Instruction Timing	Based on 267-ns CPU microcycle time
DMA Latency	DMA latency is defined as the time between receiving a DMA request (BDMR) and granting the request (BDMG). The worst case DMA latency is 2.2 microseconds.

• Related Documentation

Document Title	Order Number
KDJ11-A CPU Module User's Guide	EK-KDJ1A-UG

• Configuration

The KDJ11-A has nine jumpers for user selection of features. The locations of these jumpers are shown in Figure 5-1 and their functions are described in Table 5-1. A jumper is installed by pushing an insulated jumper wire onto the two wirewrap pins provided on the module.

The factory-installed configuration of the KDJ11-A module is shown in Table 5-2.

Table 5-1 ▪ LSI-11/73 Jumper Identification

Jumper	Function
W1	Bootstrap address bit 15
W2	Bootstrap address bit 14
W3	Powerup option selection bit 02
W4	Bootstrap address bit 13
W5	Halt trap option bit 03
W6	Bootstrap address bit 12
W7	Powerup option selection bit 01
W8	Wakeup disable
W9	BEVNT recognition

Table 5-2 ▪ LSI-11/73 Factory Configuration

Jumper	Status	Feature Selected
W1	Installed	Bootstrap address bit <15> = 1
W2	Installed	Bootstrap address bit <14> = 1
W3	Removed	Powerup option 2
W4	Installed	Bootstrap address bit <13> = 1
W5	Removed	Halt trap to location 4
W6	Installed	Bootstrap address bit <12> = 1
W7	Installed	Powerup option 2
W8	Removed	Wakeup circuit enabled
W9	Removed	BEVNT register enabled

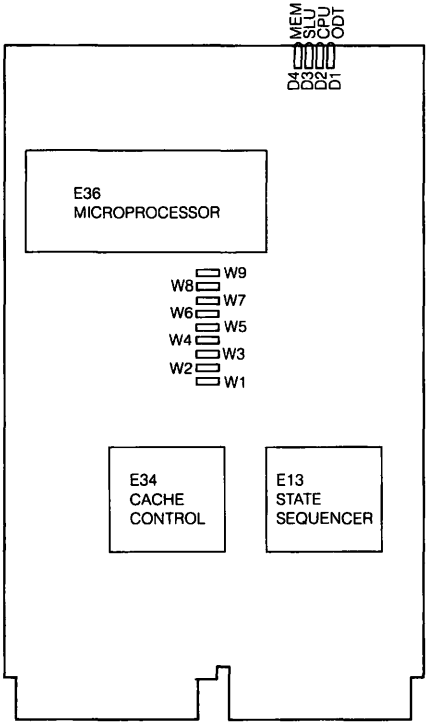


Figure 5-1 • LSI-11/73 Jumper Locations

Powerup Options

There are four powerup options available for user selection. These options are selected by configuring jumpers W7 and W3 as described in Table 5-3. Each option is described below.

- POWERUP OPTION 0

  When this option is selected, the processor reads physical memory locations 24 and 26 and loads the data into the PC and PS, respectively. The processor then either services pending interrupts with a higher priority level than the current processor priority (as specified in the PS) or begins program execution, beginning at the memory location pointed to by the PC.

- POWERUP OPTION 1

  When this option is selected, the processor unconditionally enters micro-ODT with the PS cleared. Pending service conditions are ignored.

- POWERUP OPTION 2
  When this option is selected, the processor sets the PC to 173000 and the PS to 340. The processor then starts program execution, beginning at the memory location pointed to by the PC. This option is used to implement a standard bootstrap.

- POWERUP OPTION 3
  When this option is selected, the processor reads the four bootstrap address jumpers and loads the result into PC <15:12>. PC <11:00> are set to 0. PS is set to 340. The processor then starts program execution, beginning at the memory location pointed to by the PC.

Table 5-3 ▪ LSI-11/73 Powerup Options

Option	W3	W7	Powerup Mode
0	Installed	Installed	PC at 24, PS at 26
1	Installed	Removed	Micro-ODT, PS = 0
2	Removed	Installed	PC = 173000, PS = 340
3	Removed	Removed	User's bootstrap, PS = 340

Halt Option

The Halt option determines the action taken when a HALT instruction is executed in kernel mode. Upon detecting a HALT instruction, the processor tests the BPOK bit (bit <00> of the maintenance register) before checking the Halt option bit 03. IF BPOK is set, the processor recognizes the Halt option, controlled by the W5 jumper. When the jumper is removed, bit 03 is set (1) and the processor will trap to location 4 in kernel data space and set bit 07 of the CPU error register. When the jumper is installed, bit 03 is clear (0) and the processor will enter the micro-ODT mode.

If BPOK bit 00 is not set, the Halt option is not recognized and the processor loops until BPOK is asserted and the powerup sequence is initiated.

Boot Address

The boot address jumpers select the starting address of the user's bootstrap program when powerup option 3 is selected. Jumpers W1, W2, W4, and W6 are used to select the four high-order address bits of the bootstrap address. Installing a jumper creates a logical 1; removing a jumper creates a logical 0.

During the powerup sequence, the processor reads the four high-order address bits from the jumpers and forces the remaining bits to zero. Thus, the user's bootstrap program can reside on any 4 Kbyte boundary.

Wakeup Disable

The KDJ11-A module has an onboard wakeup circuit to properly sequence the BDCOK signal. When jumper W8 is removed, the wakeup circuit is enabled and the module will properly sequence the BDCOK signal. With W8 installed, the wakeup circuit is disabled and external logic must be used to sequence the BDCOK signal.

BEVNT Recognition

The Q-bus signal BEVNT provides an external event interrupt request to the processor. When jumper W9 is installed, this feature is disabled, along with the linetime clock register. When W9 is removed, the BEVNT input is recognized and is under control of the linetime clock register. Specifically, the signal is recognized by the module when bit 06 of the linetime clock register is set (1) and is disabled when bit 06 is clear (0). The linetime clock register is a read/write register with an address of 17777546_8.

Chapter 6 • KXT11-AB FALCON-PLUS SBC-11/21-PLUS Microcomputer

The FALCON-PLUS SBC-11/21-PLUS, KXT11-AB, is a single-board microcomputer. It offers the Digital-designed 16-bit Micro/T-11 microprocessor unit (mpu), 16 Kbytes of RAM, up to 32 Kbytes of PROM, two asynchronous serial line units with programmable baud rates, 24 lines of programmable parallel I/O, and a 50-Hz, 60-Hz, or 800-Hz realtime clock.

• Specifications

Identification	M7676
Size	Dual
Power Requirements	
Power Supply	
+5.0 Vdc ±5%	2.5 A (typical), 2.8 A (maximum)
+12.0 Vdc ±5%	60 mA (typical) used by onboard circuitry, 1.1 A (maximum) includes current provided to outside interface through pin 10 of the serial I/O connector
Battery Backup	
+5.0 V ±5%	170 mA (typical), 260 mA (maximum)

Note

The + 12.0 V typical current is measured with no connections at pin 10 of the serial I/O connectors (fused line).

Bus Loads	
ac	2.7
dc	0.5

• Related Documentation

Document Title	**Order Number**
SBC-11/21-PLUS User's Guide	EK-SBC02-UG-001

▪ Configuration

The SBC-11/21-PLUS module has 61 wirewrap pins with which the user can configure the module for the operating modes necessary to meet any requirements. This is done either by installing or removing jumper wires between the wirewrap pins. The locations and identification numbers of the wirewrap pins are illustrated in Figure 6-1. Table 6-1 lists the pin functions according to the features they support. The standard factory configuration is described in Table 6-2. The following features are user-selectable:

- Battery backup
- Powerup
- Starting address
- Interrupts
- Parallel I/O buffers
- Memory maps

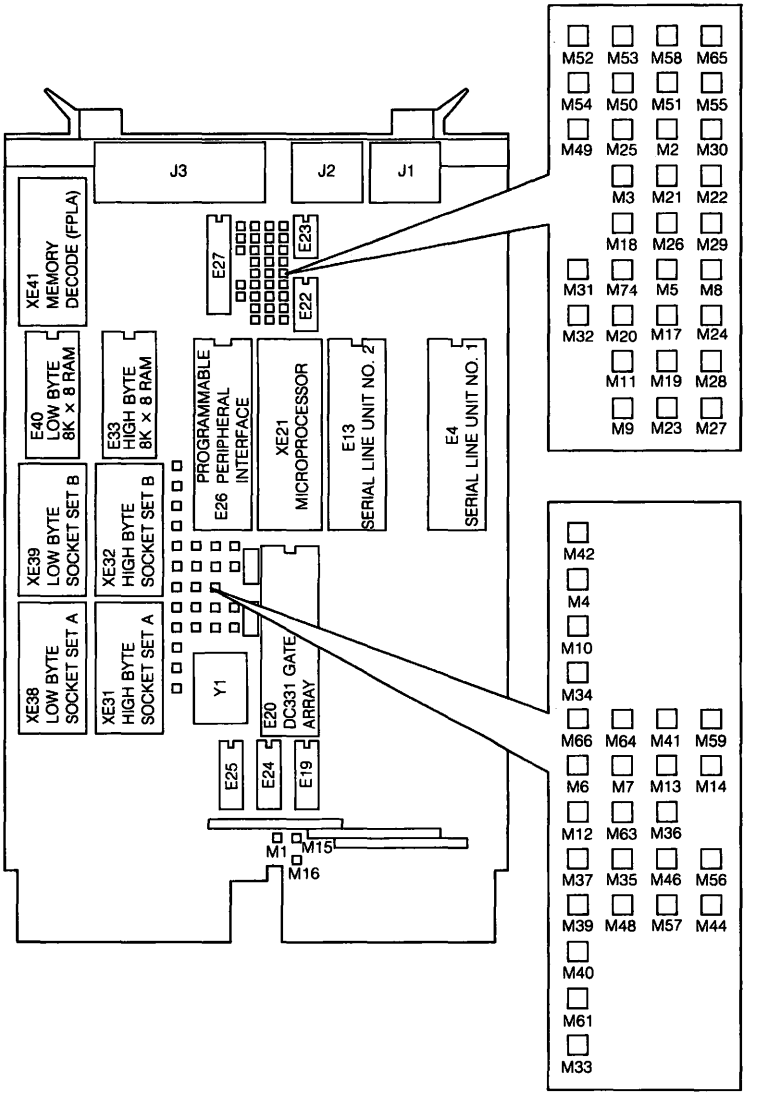


Figure 6-1 ▪ SBC-11/21-PLUS Module Layout

Table 6-1 ▪ SBC-11/21-PLUS Configuration Pin Functions

Pin	Description
Battery Backup	
M16	Battery backup +5 Vdc power source
M15	+5 Vdc power distribution to support static RAM
M1	System +5 V power (+5 VNCR)
M36	High logic level (+5 VNCR)
M41	High logic level (+5 VCR)
M34	High logic level (+5 VCR)
M14	Socket set A, high and low byte, pin 1
M13	Socket set B, high and low byte, pin 1
M7	Socket set A, high and low byte, pin 26
M66	Socket set B, high and low byte, pin 26
M59	Socket set B, high and low byte, pin 28
M64	RAM, high and low byte, pin 26
M4	Wakeup circuit diode, anode side
Powerup (wakeup circuitry)	
M6	System +5 V power, wakeup circuit diode, cathode side (+5 VNCR)
Serial Line unit (SLU 1)	
M31	System GND
M20	Transmit side of BHALT line transceiver
M17	Serial line unit (SLU) 1 BREAK detect
Serial line unit (SLU 2)	
M23	Transmit side of BEVNT line transceiver
M27	50-Hz realtime clock output
M19	60-Hz realtime clock output
M28	800-Hz realtime clock output
M11	System GND
M9	High logic level (+3 Vdc)
Memory map decoder	
M3	High logic level (+3 Vdc)
M25	Memory map select (LSB)
M21	Memory map select (MSB)
M2	System GND

(continued on next page)

Table 6-1 ▪ SBC-11/21-PLUS Configuration Pin Functions (Cont.)

Pin	Description
Start address (mode register)	
M30	Start address control (TDAL 13)
M26	Start address control (TDAL 14)
M22	Start address control (TDAL 15)
M18	High logic level (+3 Vdc)
M29	System GND
Nonmaskable interrupt and trap to the restart address	
M74	HALT request line
M32	System GND
BHALT interrupt (level 7, maskable)	
M20	Transmit side of BHALT line transceiver
M31	System GND
M24	System GND
M17	SLU 1 BREAK detect, interrupt request output
M5	Receive side of BHALT line transceiver
M8	BREAK request clock line
Memory	
M14	Socket set A, high and low byte, pin 1
M13	Socket set B, high and low byte, pin 1
M7	Socket set A, high and low byte, pin 26
M66	Socket set B, high and low byte, pin 26
M59	Socket set B, high and low byte, pin 28
M64	RAM, high and low byte, pin 26
M61	Socket set A, high byte, pin 23
M40	Socket set A, low byte, pin 23
M63	Socket set B, high byte, pin 23
M35	Socket set B, low byte, pin 23
M39	Socket set A, high byte, pin 27
M37	Socket set A, low byte, pin 27
M33	Socket set B, high byte, pin 27
M48	Socket set B, low byte, pin 27
M44	Address line 12

(continued on next page)

Table 6-1 ▪ SBC-11/21-PLUS Configuration Pin Functions (Cont.)

Pin	Description
Memory (Cont.)	
M56	High byte write strobe (-WHB)
M57	Low byte write strobe (-WLB)
M1	High logic level (+5 VNCR)
M6	High logic level (+5 VNCR)
M36	High logic level (+5 VNCR)
M12	High logic level (+5 VNCR)
M46	High logic level (+5 VNCR)
M34	High logic level (+5 VCR)
M15	High logic level (+5 VCR)
M41	High logic level (+5 VCR)
Parallel input/output	
M49	Port B buffer direction control
M51	System GND
M55	System GND
M65	Port C buffered output, to J3 pin 5
M53	Port C buffered output, to J3 pin 7
M58	Port C PC4 output (8255A-5 pin 13)
M54	Port C PC6 output (8255A-5 pin 11)
M50	High logic level (+3 Vdc)
M52	Port A buffer direction control

Table 6-2 • SBC-11/21-PLUS Standard Factory Configuration

Function	Jumper Connection
Battery Backup/Power-Up:	
No battery backup	M1 to M15
Wake-up circuit enabled	—
Starting Address:	
Start address 10000	M22 to M18
Restart address 10004	M26 to M29
	M30 to M26
Memories:	
Map 0	M64 to M7
	M25 to M21
	M21 to M2
Socket A contains 2K × 8 EPROM	M7 to M6
	M61 to M12
	M12 to M40
Socket B contains 8K × 8 SRAM	M59 to M36
	M33 to M56
	M48 to M57
	M66 to M4
	M63 to M44
	M35 to M44
Interrupts:	
SLU 1 BREAK asserts HALT and is received as level 7 interrupt (vector 140)	M17 to M20
	M5 to M8
	M74 to M32
60 Hz realtime clock asserts BEVNT	M19 to M23
Parallel I/O:	
Port A receive	M52 to M50
Port B transmit	M49 to M51
	M65 to M58

Battery Backup

The user can select battery backup mode to maintain a +5 Vdc battery supply to the following:

- The 16 Kbytes of onboard static RAM
- 24-pin devices in socket set A
- 28-pin or 24-pin devices in socket set B

The +5 Vdc battery supply is provided through the Q-bus pin AV1. A maximum of 2 mA is required. This supply is connected to wirewrap pin M16.

To enable battery backup, the jumper wire between M1 and M15 is removed and a jumper wire is installed between M16 and M15. This provides battery backup power for the 16 Kbytes of onboard static RAM. To enable battery backup of 24-pin devices in socket set A, a jumper wire is installed between M7 and M41. To enable battery backup of 28-pin devices in socket set B, a jumper wire is installed between M59 and M41. To enable battery backup of 24-pin devices in socket set B, a jumper wire is installed between M66 and M34.

If the battery backup option is enabled, the wakeup circuitry must also be enabled for all RAMs on the board. The wakeup circuitry is enabled by ensuring that no jumper is installed between M4 and M6. (This is the standard factory configuration.)

Wakeup Circuit

The module has an onboard power wakeup circuit designed for use in systems without the Q-bus power sequencing protocol or in systems with battery backup. This circuit holds the BDCOK line negated until one second after +5 V power is applied. When the module is used in a Q-bus backplane that has a power sequencing routine, the module wake-up circuit must be disabled. To do this, a jumper wire is installed between M6 and M4. The jumper wire is removed when using power supplies without power sequencing or when the battery backup option is installed. The module requires the +5 Vdc and +12 Vdc power supplies to have a rise time of less than 50 nanoseconds.

Starting Address

The user selects the starting address for the microcomputer via wirewrap pins. When the module is powered up, the microcomputer loads this value into R7 (program counter) as the first fetch address. The wirewrap pins are M22, M26, M29, M30, and M18, and are defined in Table 6-1. The user can select from eight available starting addresses. Table 6-3 lists these available addresses and the jumper connections required for each address. The restart address is always the start address incremented by four. The wirewrap pin locations are shown in Figure 6-1.

Table 6-3 • SBC-11/21-PLUS Mode Register Configuration

Start Address	Restart Address	Connect M22 to	Connect M26 to	Connect M30 to
000000	000004	M18	M29	M18
010000*	010004	M18	M29	M29
020000	020004	M29	M18	M18
040000	040004	M29	M18	M29
100000†	100004	M29	M29	M18
140000	140004	M29	M29	M29
172000	172004	M18	M18	M18
173000	173004	M18	M18	M29

* Factory setting. The start address should be selected in conjunction with the memory map configuration. Figure 6-5 shows how the available start addresses fit into the memory maps.

† When using the 27128 EPROM with memory map 3, strap the board for starting address 100000 for actual starting address 40000; strap the board for 40000 for actual address of 100000.

Interrupts

The SBC-11/21-PLUS implements a multilevel interrupt system that has eleven separate interrupts. Three interrupts — CTMER, BKRQ, and REVNT — are user-configurable by means of jumper wires, as shown in Figure 6-2.

The CTMER interrupt is at the highest level (nonmaskable). It is caused by a timeout — that is, a failure to detect BRPLY during a fetch/read, write, or IAK transaction. Such a condition could occur only if the peripheral that caused the interrupt failed to return BRPLY during the vector reading operation. The other two interrupts the user can select are BKRQ and REVNT. All jumper combinations that are "electrically correct" are legal.

A description of some typical configurations follows to familiarize the user with the different combinations available.

Jumper Connections	Interrupt Condition
M7 to M74 M20 to M31 M28 to M23 M8 to M24	Allows the SLU1 BREAK input to set the -CTMER nonmaskable interrupt and trap to restart address. BHALT bus signal is ignored. The SLU2 800 Hz linetime clock and BEVNT bus signal enable the REVNT interrupt.
M5 to M74 M17 to M8 M20 to M31 M23 to M71	Allows the BHALT bus signal to set the -CTMER nonmaskable interrupt and trap to the restart address. SLU1 BREAK input sets the BKRQ level 7 maskable interrupt, and only the BEVNT bus signal enables the REVNT interrupt.
M74 to M32 M17 to M20 M5 to M8 M23 to M9	Allows the timeout (TMER) to set the -CTMER nonmaskable interrupt for all timeouts. SLU1 BREAK or BHALT bus signal set the BKRQ level 7 maskable interrupt, and BEVNT bus line is clamped low; no interrupts can be generated by BEVNT.

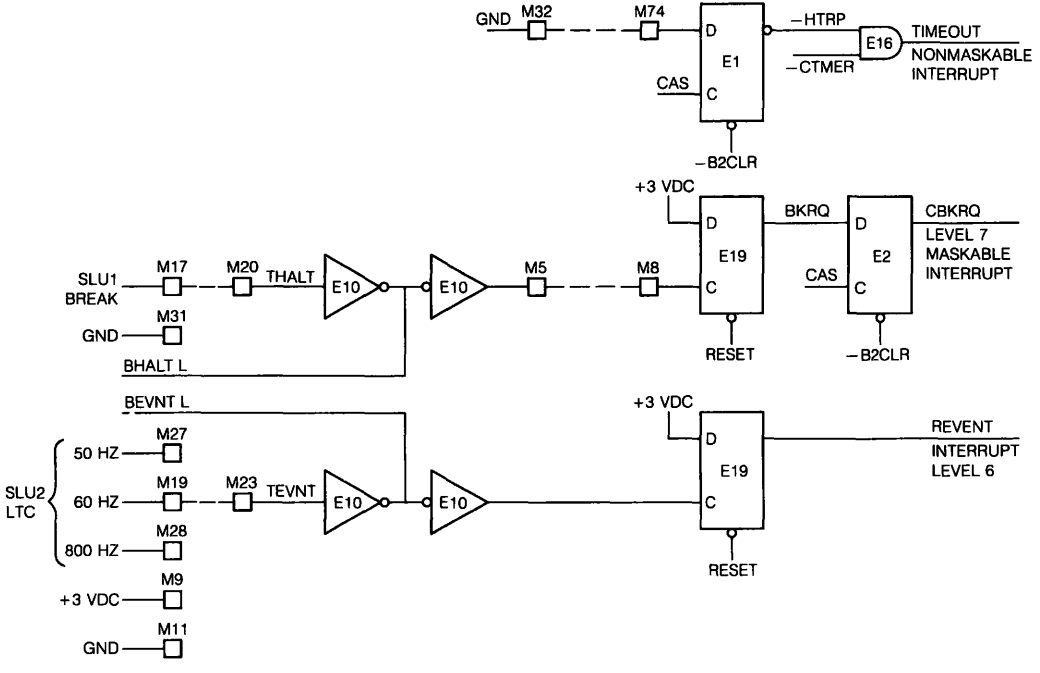


Figure 6-2 ▪ SBC-11/21-PLUS Interrupt Configurations

Parallel I/O

The parallel I/O is implemented with the 8255A-5 programmable peripheral interface (PPI) and connects to the user's interface through the J3 connector. Figure 6-3 illustrates the wirewrap pins used for the configuration of the parallel I/O. The directions of port A and port B transceivers are dependent on the logic level connected to M49 and M52. Wirewrap pin 52 connects to port A through a 200-ns minimum rise time edge delay circuit. When M50 (+ 3 Vdc) is jumpered to pins M49 and M52, port A and port B buffers are inputs to the PPI from the J3 connector. When M51 (GND) is jumpered to pins M49 and M52, port A and port B buffers are outputs from the PPI to the J3 connector.

The direction of port A and port B can also be controlled by a user's program. To make this possible, M58 and M54 must be jumpered to M49 and M52. The data outputs via port C will control the voltage levels at the direction control inputs to ports A and B.

Wirewrap pins M65 and M53 can be jumpered to M49 and M52 to allow the user to control the direction of the transceivers via J3 connector pins 5 and 7. When not using wirewrap pins M58 and M65 or M54 and M53 to control the direction of ports A and B, jumpers connected between M58 and M65 and between M54 and M53 allow PC4 and PC6 to be used as inputs to the PPI from the J3 connector.

Note

If pins M65, M53, M58, or M54 are used for program control off port A or B, the user must ensure that the PPI and the buffer do not contend as driver output to driver output. If this condition is allowed to occur, damage to both drivers may result.

The programmable peripheral interface can function in three modes selected by the software. The jumper configurations and the handshake signals or each of these modes are shown in Tables 6-4, 6-5, and 6-6.

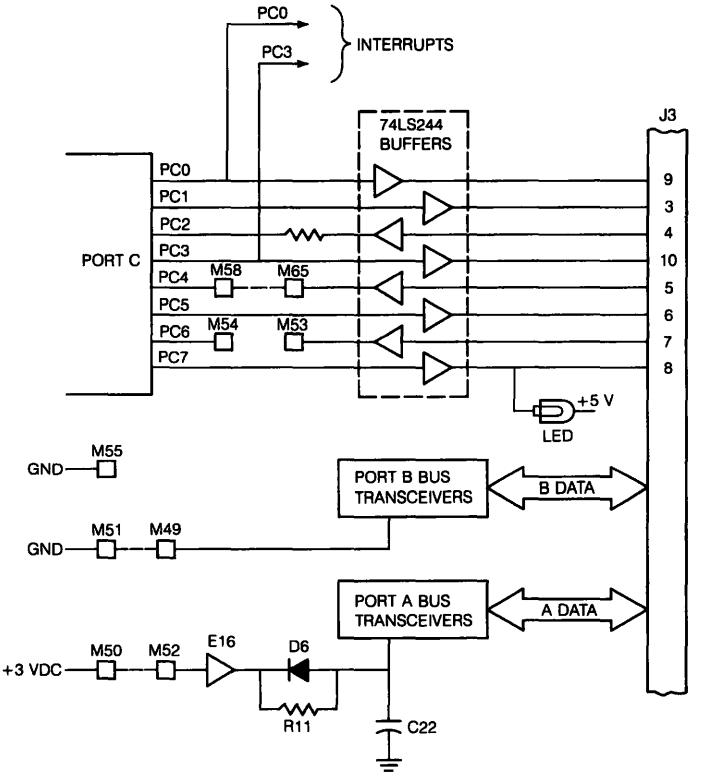


Figure 6-3 ▪ SBC-11/21-PLUS Parallel I/O Configurations

Table 6-4 ▪ SBC-11/21-PLUS Mode 0 Buffer Configuration (No Handshake)

PPI I/O	Input Status	Output Status	Port C Controlled
Port A	M52 to M50	M52 to M51	M52 to M54 or M58
Port B	M49 to M50	M49 to M51	M49 to M54 or M58
PC7	n/a	Output	
PC6	M54 to M53	Never external	
PC5	n/a	Output	
PC4	M58 to M65	Never external	
PC3	n/a	Interrupt A	
PC2	Input	n/a	
PC1	n/a	Output	
PC0	n/a	Interrupt B	

Table 6-5 ▪ SBC-11/21-PLUS Mode 1 Buffer Configuration (Strobed I/O)

PPI I/O	Input Status	Output Status	Port C Controlled
Port A	M52 to M50	M52 to M51	n/a
Port B	M49 to M50	M49 to M51	M49 to M54 or M58
PC7	n/a	Buffer A full	
PC6	M54 to M53 (Acknowledge A)*	Never external	
PC5	n/a	Buffer A full	
PC4	M58 to M65 (Strobe A)	Never external	
PC3	n/a	Interrupt A	
PC2	Strobe B (input) Acknowledge B (output)	n/a	
PC1	n/a	Buffer B full	
PC0	n/a	Interrupt B	

* User's hardware acknowledges receipt of data output by port A.

Table 6-6 ▪ SBC-11/21-PLUS Mode 2 Buffer Configuration and Handshake

PPI I/O	Input Signal	Output Signal
Port A	Bidirectional bus	If M52 to M54 or M53
Port B	n/a	n/a
PC7	n/a	Output buffer A full
PC6	Acknowledge A	n/a
PC5	n/a	Input buffer A full
PC4	Strobe A (if M65 to M58)	n/a
PC3	n/a	Interrupt A
PC2	Input	n/a
PC1	n/a	Output
PC0	n/a	Output

Serial I/O

The jumper options relating to the serial I/O determine the interrupt response of the system. All responses to the BREAK detection by SLU1 are listed in Table 6-7.

Table 6-7 ▪ SBC-11/21-PLUS SLU1 BREAK Detection

Jumper Connection	BREAK Response
M17 to M20 M5 to M8	BHALT signal to the Q-bus and BKRQ interrupt (vector 140)
M20 to M31 M5 to M8	No response
M8 to M17 M20 to M31	BKRQ interrupt (vector 140) (no BHALT to bus)
M17 to M74 M20 to M31 M8 to M24	CTMER interrupt (HALT trap) through restart

Memories

The memory system for the module is the Q-bus, 4 Kbytes of local RAM, and four 28-pin sockets that accept either 24-pin or 28-pin industry-standard +5 V memory chips. These chips are provided by the user and can be either EEPROMs, EPROMs, PROMs, ROMs, or static RAMs. The sockets will accept 2K×8, 4K×8, 8K×8, and 16K×8 PROMs/EPROMs/EEPROMs, or 2K×8 and 8K×8 static RAMs.

There are two socket sets: set A, controlled by -CSKTA and set B, controlled by -CSKTB. Each set has a high-byte socket and a low-byte socket that are interconnected as shown in Figure 6-4. The wirewrap pins used to configure the memory are shown in Figure 6-5 and described in Table 6-1. The standard factory configuration of the installed jumper wires is represented by the dashed lines in Figure 6-5. In addition to configuring the sockets, the user must configure the decode memory address chip to select one of the four memory maps available.

Note

The SBC-11/21-PLUS contains semiconductor devices that may be susceptible to damage by electrostatic charges. When handling the board and configuring the wirewrap pins, you should keep the board on a grounded conductive plane. Also, use wrist straps in contact with the skin to keep yourself at the same ground potential.

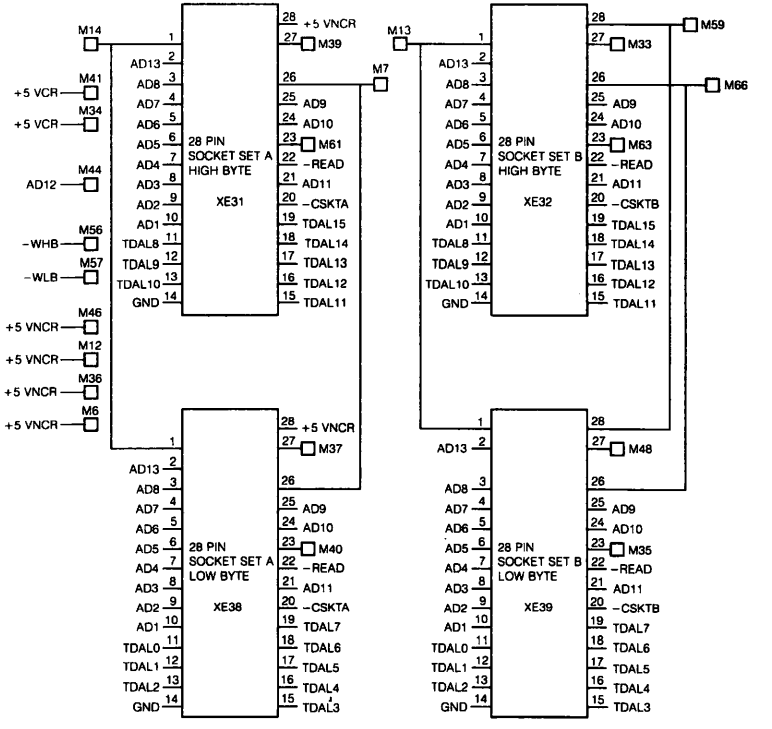
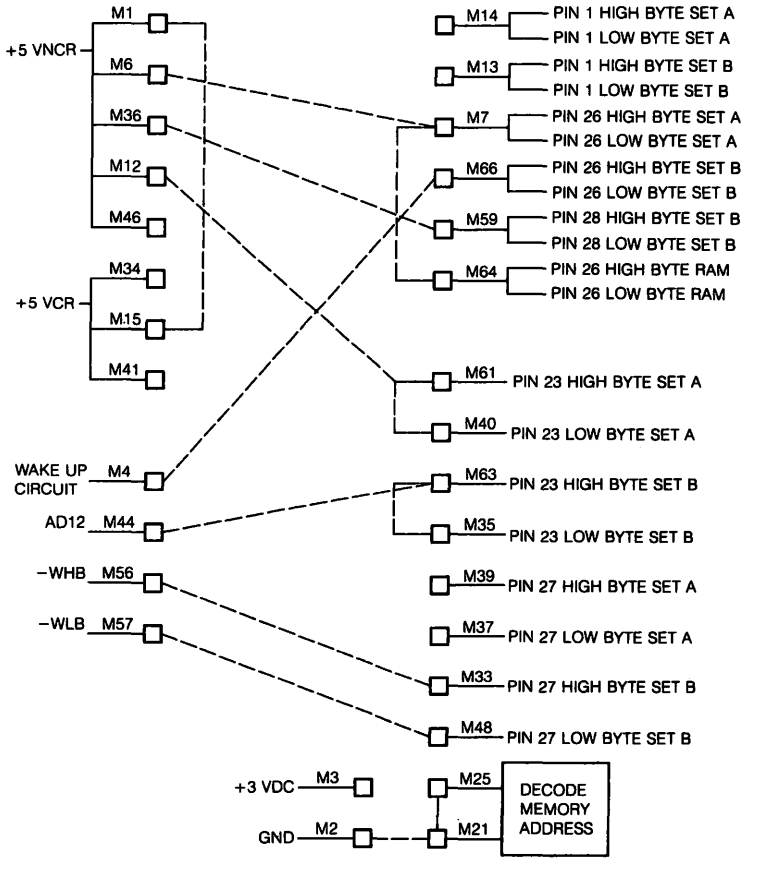


Figure 6-4 ▪ SBC-11/21-PLUS Socket Sets A and B Interconnection

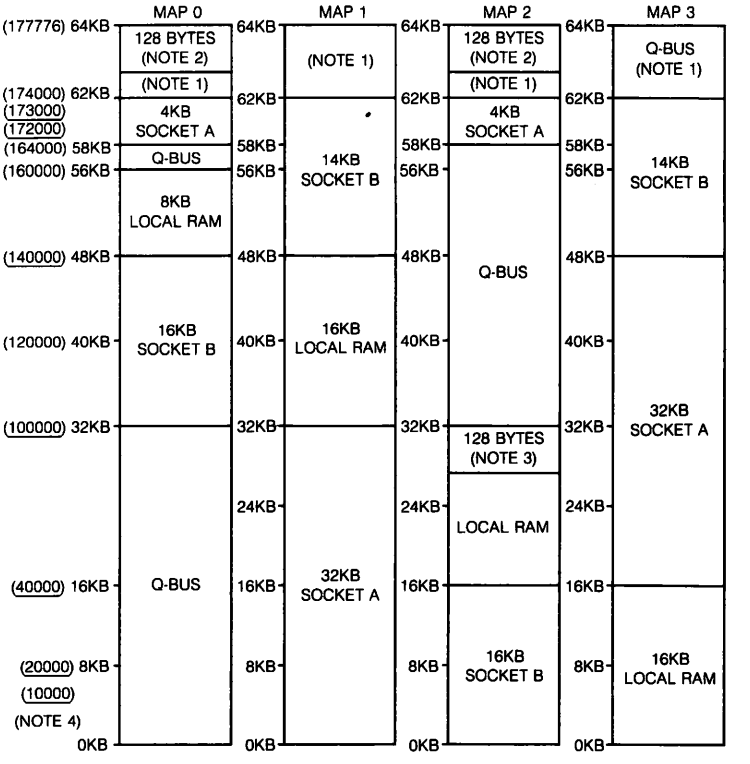


NOTE: DOTTED LINES ILLUSTRATE FACTORY CONFIGURATION.

Figure 6-5 ▪ SBC-11/21-PLUS Memory Configuration

- MEMORY MAPS

Figure 6-6 shows the four memory maps available. The module can be configured to select the one that meets the user's requirements. Wirewrap pins M18, M21, M29, and M25 are used to select the memory map. The jumper requirements are listed in Table 6-8.



NOTES

1. THIS SECTION CONTAINS THE LOCAL I/O ADDRESSES FOR THE SLUS AND PPI. ALL UNASSIGNED ADDRESSES ARE ASSUMED TO RESIDE ON THE Q-BUS.
2. ADDRESSES 177777 - 177600 IN MAPS 0 AND 2 ARE RAM SCRATCHPAD LOCATIONS USED BY MACRO-ODT.
3. ADDRESSES 77777 - 77600 IN MAP 2 ARE ALLOCATED TO THE Q-BUS.
4. UNDERLINED ADDRESSES ARE JUMPER-SELECTABLE START ADDRESS.

Figure 6-6 ▪ SBC-11/21-PLUS Memory Maps

Table 6-8 ▪ SBC-11/21-PLUS Memory Map Jumpers

Map Selection	Jumper M25 to	Jumper M21 to
Map 0	M21	M29
Map 1	M18	M29
Map 2	M29	M18
Map 3	M21	M18

- PROMs/EPROMs/EEPROMs

The 28-pin sockets accept 24-pin and 28-pin PROMs, EPROMs, or EEPROMs. If 24-pin chips are selected, caution must be observed to ensure that pin 1 of the chip is placed into socket hole 3. The configuration requirements of some industry compatible PROMs/EPROMs are described in Tables 6-9 and 6-10. The user may select chips from other vendors; however, the pin configuration must be compatible with the sockets provided. A 250-nanosecond maximum output enable time is also required, and the maximum access time for compatible PROMs/EPROMs is 450 nanoseconds. The maximum output enable time is defined as the time from the assertion of TDIN or TDOUT by a bus master to the time the module asserts valid data onto the bus.

The user installs a jumper wire from the pin referenced by the chip type to the socket pin described in the tables. Figure 6-5 provides a reference for all signals and the socket pins associated with the wirewrap pins. These interconnections are listed separately under socket set A and socket set B, and some jumper wires are common to both socket sets. Some devices may not require a connection or installation of a jumper wire and are designated by an "nc" (requires no connection) in the tables. The wirewrap pin locations are shown in Figure 6-1.

Table 6-9 • SBC-11/21-PLUS Socket Set A Configuration for EEPROMs/EPROMs/PROMs

			Connect Referenced Pin to Socket A Pin						
Part	**Pins**	**Size**	**M40**	**M37**	**M7**	**M61**	**M14**	**M39**	**M64**
EEPROMs									
Intel									
2815	24	2K×8	M12	nc	M6	M12	nc	nc	M7
EPROMs									
Intel									
2716	24	2K×8	M12	nc	M6	M12	nc	nc	M7
2716-1	24	2K×8	M12	nc	M6	M12	nc	nc	M7
2716-2	24	2K×8	M12	nc	M6	M12	nc	nc	M7
2732	24	4K×8	M44	nc	M6	M44	nc	nc	M7
2732A	24	4K×8	M44	nc	M6	M44	nc	nc	M7
2764	28	8K×8	M44	M46	nc	M44	M36	M36	M6
27128	28	16K×8	M44	M39	M10	M44	M39	M36	M6
TI									
TMS2516	24	2K×8	M12	nc	M6	M12	nc	nc	M7
TMS2516-35	24	2K×8	M12	nc	M6	M12	nc	nc	M7
Mostek									
MK2716	24	2K×8	M12	nc	M6	M12	nc	nc	M7
MK2764	28	8K×8	M44	nc	nc	M44	M36	nc	M6

(continued on next page)

Table 6-9 ▪ SBC-11/21-PLUS Socket Set A Configuration for EEPROMs/EPROMs/PROMs (Cont.)

			Connect Referenced Pin to Socket A Pin						
Part	**Pins**	**Size**	**M40**	**M37**	**M7**	**M61**	**M14**	**M39**	**M64**
PROMs									
Intel									
3632	24	4K×8	M12	nc	M6	M12	nc	nc	M7
3632-1	24	4K×8	M12	nc	M6	M12	nc	nc	M7

nc = requires no connection

Table 6-10 ▪ SBC-11/21-PLUS Socket Set B Configuration for EEPROMs/EPROMs/PROMs

			Connect Referenced Pin to Socket A Pin						
Part	**Pins**	**Size**	**M35**	**M48**	**M13**	**M63**	**M59**	**M66**	**M33**
EEPROMs									
Intel									
2815	24	2K×8	M12	nc	nc	M12	nc	M6	nc
EPROMs									
Intel									
2716	24	2K×8	M12	nc	nc	M12	nc	M6	nc
2716-1	24	2K×8	M12	nc	nc	M12	nc	M6	nc
2716-2	24	2K×8	M12	nc	nc	M12	nc	M6	nc
2732	24	4K×8	M44	nc	nc	M44	nc	M6	nc
2732A	24	4K×8	M44	nc	nc	M44	nc	M6	nc
2764	28	8K×8	M44	M46	M36	M44	M36	nc	M36
27128	28	16K×8	M44	M33	M33	M44	M36	M10	M59
TI									
TMS2516	24	2K×8	M12	nc	nc	M12	nc	M6	nc
TMS2516-35	24	2K×8	M12	nc	nc	M12	nc	M6	nc
Mostek									
MK2716	24	2K×8	M12	nc	nc	M12	nc	M6	nc
MK2764	28	8K×8	M44	nc	M36	M44	M36	nc	nc
PROMs									
Intel									
3632	24	4K×8	M12	nc	nc	M12	nc	M6	nc
3632-1	24	4K×8	M12	nc	nc	M12	nc	M6	nc

nc = requires no connection

- RAMs

The 28-pin sockets can also accept 24-pin static RAM chips. Caution must be observed to ensure that pin 1 of the chip is installed into socket hole 3. The configuration requirements of some industry-compatible RAMs are described in Tables 6-11 and 6-12. The user may select chips from other vendors; however, the pin configuration must be compatible with the sockets provided. The selected RAMs are required to meet the maximum output enable time and the maximum access time specified for the PROMs.

The user installs a jumper wire from the pin referenced by the chip type to the socket pin described in the tables. Figure 6-5 provides a reference for all signals and the socket pins associated with the wirewrap pins. These interconnections are listed separately under socket set A and socket set B, and some jumper wires are common to both socket sets. Some devices may not require a connection or installation of a jumper wire and are designated by an "nc" in the tables. The wirewrap pin locations are shown in Figure 6-1.

Table 6-11 • SBC-11/21-PLUS Socket Set A Configuration for RAM

			Connect Referenced Pin to Socket A Pin					
Part	**Pins**	**Size**	**M40**	**M37**	**M7**	**M61**	**M14**	**M39**
Mostek								
MK4802	24	2K×8	M57	nc	M34	M56	nc	nc
Toshiba								
TMM2016P	24	2K×8	M57	nc	M34	M56	nc	nc
TMM2016P-1	24	2K×8	M57	nc	M34	M56	nc	nc
TC5565P/P-1 TC5565PL/PL-1	28	8K×8	M44	M57	M34	M44	nc	M56
Hitachi								
HM6116P	24	2K×8	M57	nc	M34	M56	nc	nc
HM6264P	28	8K×8	M44	M57	M34	M44	nc	M56

nc = requires no connection

Table 6-12 ▪ SBC-11/21-PLUS Socket Set B Configuration for RAM

Part	Pins	Size	Connect Referenced Pin to Socket A Pin M35	M48	M13	M63	M59	M66	M33
Mostek									
MK4802	24	2K×8	M57	nc	nc	M56	nc	M34	nc
Toshiba									
TMM2016P	24	2K×8	M57	nc	nc	M56	nc	M34	nc
TMM2016P-1	24	2K×8	M57	nc	nc	M56	nc	M34	nc
TC5565P/P-1 TC5565PL/PL-1	28	8K×8	M44	M57	nc	M44	M41	M41	M56
Hitachi									
HM6116P	24	2K×8	M57	nc	nc	M56	nc	M34	nc
HM6264P	28	2K×8	M44	M57	nc	M44	M36	M34	M56

nc = requires no connection

▪ Cables and Connectors

The module has a 30-pin connector (J3) for an external interface with the programmable I/O interface and two 10-pin connectors (J1 and J2) for the external interface of the serial line units (SLUs). The locations of these connectors on the module are shown in Figure 6-1.

Parallel I/O Interface

The module connector is a 30-pin AMP MODU connector. The I/O signals are buffered and are capable of driving up to 50 feet (maximum) of flat ribbon or round cable with a 30-pin AMP contact housing at each end. The following list of connectors is compatible with the module connector:

AMP MODU polarized or nonpolarized contact housings for crimp snap-in pin and receptacle contacts:

Latching, polarized housings	2-87631-6 no strain relief 87733-6 strain relief
Nonlatching, polarized housings	1-87977-3 no strain relief 1-102184-3 strain relief
Nonlatching, nonpolarized housings	2-87456-6 no strain relief 2-87832-7 strain relief
Receptacle contacts	87045-3 for 30 to 26 AWG 102098-3 for 32 to 27 AWG

Mass termination connectors for flat cables:

Separate parts (nonpolarized)	1-88378-1 connector 1-86873-2 cover 1-88340-1 strain relief cover
Separate parts (polarized)	1-88392-1 connector 1-86373-2 cover 1-88340-1 strain relief cover
Connector and cover kits (nonpolarized)	1-88379-1 no strain relief 1-88476-1 with strain relief
Connector and cover kits (polarized)	1-88393-1 no strain relief 1-88478-1 with strain relief
Separate parts	1-88392-1 connector 1-86873-2 cover 1-88340-1 strain relief cover
Latching connectors and covers (polarized)	1-88423-1 no strain relief 1-88479-1 with strain relief
Mass modular connector system	1-102393-3 housing for 30-26 AWG 1-102396-3 cover 1-102392-3 kit 1-102398-3 housing for 26-22 AWG 1-102396-3 cover 1-102397-3 kit

Connectors can be terminated to discrete wire in sizes 30-26 AWG, 26-24 AWG, as well as jacketed cable and bonded ribbon cable.

Serial Line Interfaces (J1 and J2)

Each serial line unit (SLU) is compatible with EIA RS-232C and EIA RS-423 serial type interfaces. SLU1 interfaces through J1, and SLU2 interfaces through J2.

The user installs a slew rate resistor determined by the operating baud rate defined in Table 6-13. The slew rate resistor is identified as R6 and its location on the module is shown in Figure 6-1.

The user provides the interconnecting cables. The following list describes some standard Digital cables for use with the KXT11-AB:

BC20N-05 5-foot EIA RS-232C null modem cable to directly interface with the EIA RS-232C terminal (2 × 5 pin AMP female to RS-232C female)

BC21B-05 5-foot EIA RS-232C modem cable to interface with modems and acoustic couplers (2 × 5 pin AMP female to RS-232C male)

BC20M-50 50-foot EIA RS-422 or RS-423 cable for high throughput transmission (19.2 Kbaud) between two SBC-11/21-PLUS computers (2 × 5 pin AMP female to 2 × 5 pin AMP female)

Table 6-13 ▪ EIA Slew Rate Resistor Values

Baud Rate	Resistor R6 (ohms)
38400	22 kΩ*
19200	51 kΩ
9600	120 kΩ†
4800	200 kΩ
2400	430 kΩ
1200	820 kΩ
600	1 MΩ
300	1 MΩ

* Factory-installed value

† Maximum baud rate for SLU1

Chapter 7 • KXT11-CA Single-Board Computer

The KXT11-CA is a single-board computer (SBC) that can operate as a peripheral I/O processor or as a stand-alone computer.

• Specifications

Identification	M8377
Size	Quad
Power Requirements	
Power supply	
+5 Vdc ±5%	3.5 A (typical), 4 A (maximum)
+12 Vdc ±5%	60 milliampere (typical) used by onboard circuity; 2 A (maximum) includes current provided to outside interface through pin 10 of the serial I/O connector for operating the DLV11-KA EIA-20 milliampere converter option. The +12 V typical current is measured with no connections at pin 10 of the serial I/O connector (fused line).
Battery Backup +5 Vdc ±5%	12 milliampere (typical), 20 milliampere (maximum)
Bus Loads	
ac	2.7
dc	1.0

• Related Documentation

Document Title	Order Number
KXT11-CA Single-Board Computer User's Guide	EK-KXTCA-UG
PDP-11 Architecture Handbook	EB-23657-18
Chipkit Users Manual	EJ-17475
Micro/T11 User's Guide	EK-DCT11-UG
TU58 Technical Manual	EK-OTU58-TM
KXT11-CA ROM Listing	EK-KXTCA-HR

▪ Configuration

The KXT11-CA is configured by means of 32 jumpers and two edge-mounted switches. Jumper configurations are done by either installing, repositioning, or removing jumpers between pins. The locations and identification numbers of the pins are shown in Figure 7-1. Table 7-1 defines the pins by functional groups, and the standard factory-shipped configuration is listed in Table 7-2.

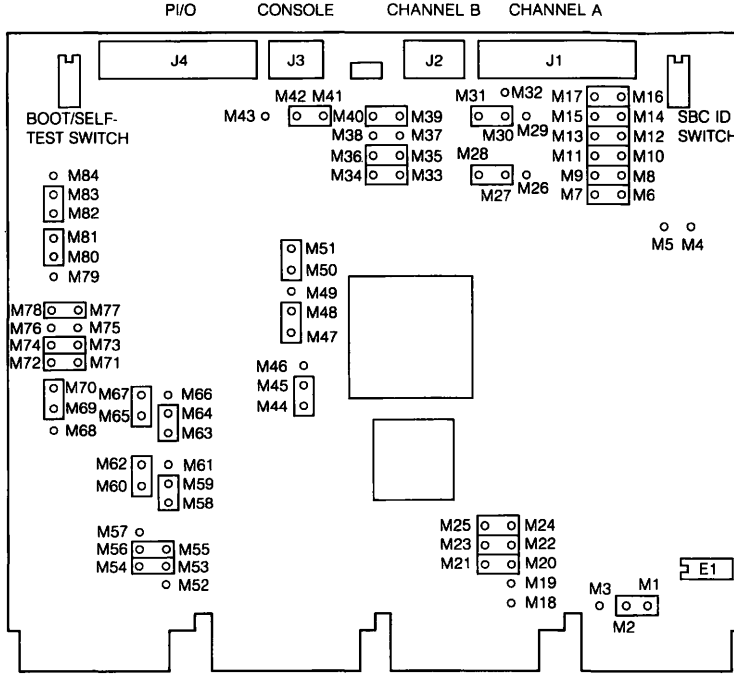


Figure 7-1 ▪ KXT11-CA Jumper Layout

Table 7-1 ▪ KXT11-CA Jumper Pin Definitions

Function	Jumpers
Base address	M18 and M19
DMA requests	M47, M48, M49, M50, M51
Realtime clock (60 Hz or 50 Hz)	M84, M82, M83
SLU1 break (nonmaskable)	M81, M80
User memory socket sites	M57, M66, M61, M55, M60, M65, M63, M58, M52, M67, M64, M59, M56, M53, M62
Memory map selection	M24, M25, M22, M23, M20, M21
Battery Backup:	
Onboard RAM	M1, M2, M3
User RAM	M68, M69, M70
SLU1:	
Programmable baud rate	M72, M74, M76, M78, M75, M73, M71, M77
Serial output (RS-422, RS-423)	M43, M41, M42
Serial input	M5, M4
SLU2:	
Channel A	M13, M12, M17, M16, M11, M10, M9, M8, M15, M14, M7, M6
Channel B	M39, M40, M38, M37, M46, M45, M44, M34, M33, M28, M26, M35, M36, M29, M32, M27, M31, M30, M43

Table 7-2 ▪ KXT11-CA Factory-shipped Jumper Configuration

Function	Jumpers Installed
Base address	Low range (jumper out)
Interrupts:	
Realtime clock RTC60	M82 to M83
SLU1 (break)	M81 to M80
DMA Requests:	
SLU2 channel A	M51 to M50
SLU2 channel B	M47 to M48
Memories:	
2K × 8 EPROM	M53 to M55
Memory map 0	No jumpers installed
Battery backup (no)	M1 to M2
User RAM (no)	M69 to M70
SLU1:	
Serial baud/bits rate (9600)	M78 to M77 M76 to M75 M72 to M71
Receiver (RS-423)	No jumpers installed
Transmitter	M42 to M41
SLU2:	
Channel A receiver (RS-422)	M15 to M14 M13 to M12 M11 to M10 M7 to M6 M8 to M9
Channel B receiver (RS-422)	M36 to M35 M34 to M33
Channel B transmitter (RS-422)	M28 to M27 M32 to M30 M39 to M40
Boot/self-test switch	Position 10
ID switch	Position 2

User EPROM, EEPROM, and RAM

The user can install EPROMs, EEPROMs, or RAMs into the two-user socket sites, shown in Figure 7-2. Table 7-3 lists jumper configurations for several memory chips. The user may select chips from other vendors; however, pin configurations must be compatible. Selected EPROMs or RAMs must meet maximum enable time of 250 nanoseconds and a maximum access time of 450 nanoseconds.

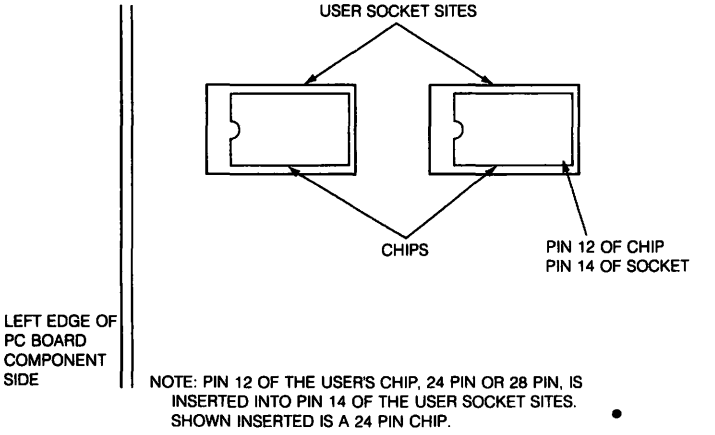


Figure 7-2 ▪ KXT11-CA User Socket Sites

Table 7-3 ▪ KXT11-CA Memory Jumper Configurations

Part No.	Pins	Size	Jumper Connection between Pins								
			56–55	61–62	55–53	52–53	61–59	58–59	66–67	66–64	63–64
Intel											
2716	24	2K×8	R	R	I	R	I	R	R	I	R
2732	24	4K×8	R	R	I	R	R	I	R	R	I
2764	28	8K×8	I	I	R	R	R	I	I	R	I
27128	28	16K×8	I	I	R	I	R	I	I	R	I
			62–60	53–54	53–55	59–60	67–65	64–65	59–58	64–63	56–55
Toshiba											
TMM2016P-01	24	2K×8	R	R	I	I	R	I	R	R	R
TMM5565P-1	28*	8K×8	I	I	R	R	I	R	I	I	I

I = jumper installed; R = jumper removed

* When 28-pin RAM devices are installed, M57 is jumpered to either M56 (+ 5 V source) or M55 (+ 5 V battery backup source).

Battery Backup

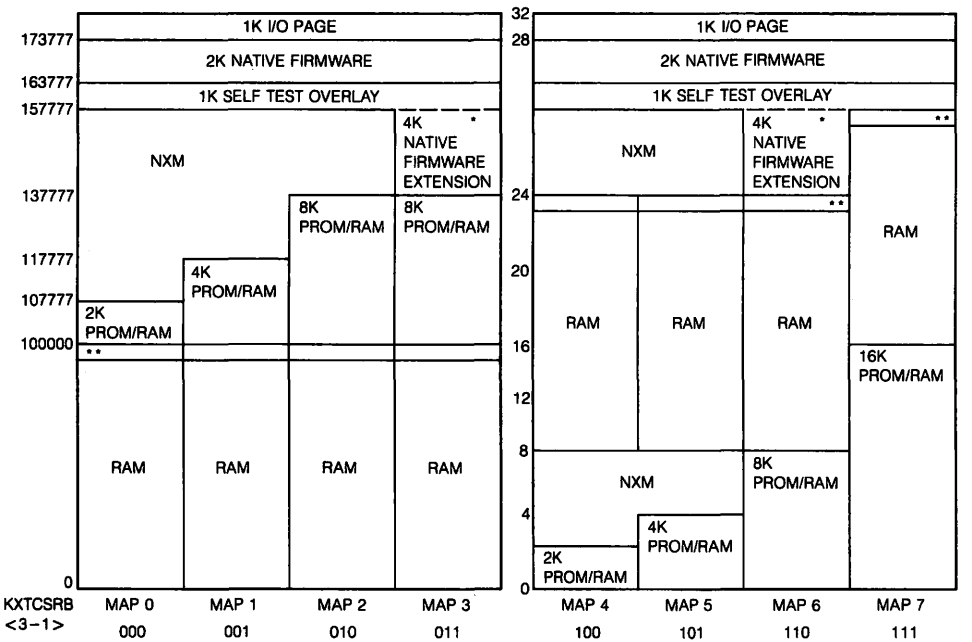
The KXT11-CA is factory-configured with no battery backup for the RAMs with a jumper inserted between pins M1 and M2. By removing this jumper and reinstalling it between pins M2 and M3, the user can select the battery backup configuration to maintain a +5 V battery supply to the 16-Kbyte static RAM after the dc power is removed. The user must then supply battery backup voltage to pin AV1.

User Socket +5 V Power

If the 32-Kbyte static RAM is jumpered for battery backup, then the user socket can also be jumpered for battery backup. This is done by removing the factory-installed jumper from between pins M70 and M69 and reinstalling the jumper between pins M69 and M68.

Memory Maps

The KXT11-CA can be configured for one of eight different memory maps, numbered from 0 to 7, as shown in Figure 7-3. Table 7-4 lists the jumper configurations required to select one of these memory maps.



*NOT CURRENTLY SUPPORTED
**THE TOP 64 BYTES OF NATIVE RAM ARE RESERVED BY NATIVE FIRMWARE

Figure, 7-3 ■ KXT11-CA Memory Maps

Table 7-4 ▪ KXT11-CA Memory Map Jumpers

Memory Map	Jumper Connections M24 to M5	M22 to M23	M20 to M21
0	IN	IN	IN
1	OUT	IN	IN
2	IN	OUT	IN
3	OUT	OUT	IN
4	IN	IN	OUT
5	OUT	IN	OUT
6	IN	OUT	OUT
7	OUT	OUT	OUT

Boot/Self-test Option

The KXT11-CA has a 16-position switch used to configure the bootstrap and self-test options. The location of this switch is shown in Figure 7-1. Table 7-5 lists the options which can be selected.

Table 7-5 ▪ KXT11-CA Boot/Self-test Switch Options

Switch Position	Option Description
Stand-alone Boot	
0	Application code in user ROM is executed; no selftest is performed.
1	Application code in user ROM is executed; self-test is performed.
2	Application code in user ROM is executed; self-test and ROM test are performed.
3	Boot application code from TU58 drive unit; self-test is performed.
4	No auto self-test; enter serial ODT.

(continued on next page)

Table 7-5 ▪ KXT11-CA Boot/Self-test Switch Options (Cont.)

Switch Position	Option Description
System Boot	
5	Self-test is performed; do not boot; wait for command from arbiter.
6	No self-test is performed; do not boot; wait for boot command from arbiter.
7	Reserved
Dedicated Test	
8	Used for stand-alone testing. Self-test is performed; loopback test is run; no application code is run; the RAM is mapped low.
9	Used for stand-alone testing. Self-test and user ROM test are performed; loopback test is run; no application code is run; the RAM is mapped low.
10	Used when running XXDP+ diagnostics. Self-test is performed; wait for additional test commands; the RAM is mapped low.
11-15	Reserved

Base Address

The jumper between pins M18 and M19 enables the user to select either a high- or a low-base address range. Within a particular range, the 16-position system ID switch enables the user to select one of 14 base addresses. Figure 7-1 shows the location of the system ID switch. Table 7-6 lists the jumper and switch configurations required for various base addresses.

Note

Due to a conflict of CPU addressing, the high base address range should be used if a FALCON SBC or more than eight KXT11-CAs are on the Q-bus.

Table 7-6 ▪ KXT11-CA Base Address Configuration

ID Switch Position	SBC Base Address Low Range M18-M19 Out	SBC Base Address High Range M18-M19 In
0*	–	–
1*	–	–
2	17760100	17762100
3	17760140	17762140
4	17760200	17762200
5	17760240	17762240
6	17760300	17762300
7	17760340	17762340
8	17775400	17777400†
9	17775440	17777440†
10	17775500	17777500†
11	17775540	17777540†
12	17775600	17777600†
13	17775640	17777640†
14	17775700	17777700†
15	17775740	17777740†

* For these two switch positions, the Q-bus interface is disabled.

† Caution: Using these base addresses may conflict with existing Q-bus devices.

Realtime Clock Interrupt

The realtime clock interrupt can be set for either 50-Hz or 60-Hz operation, as determined by pins M82, M83, and M84. The factory-shipped configuration is for 60-Hz operation, with a jumper installed between pins M82 and M83. To select 50-Hz operation, the user must removed the factory-installed jumper and reinstall it between pins M83 and M84.

Break Enable

The KXT11-CA is shipped with the console SLU1 BREAK key interrupt enabled. This causes a nonmaskable T-11 trap to restart when the BREAK key is pressed on the SLU1 console terminal. To disable this interrupt, the user must remove the factory-installed jumper from between pins M80 and M81 and reinstall it between pins M79 and M80.

SLU1 Transmitter

SLU1 can be configured to transmit either single-ended (RS-423) or differential (RS-422) asynchronous serial data out on connector J3. The factory-shipped configuration is for RS-423 transmission, with a jumper installed between pins M41 and M42. To select RS-422 transmission on SLU1, the user must remove the factory-installed jumper and reinstall it between pins M42 and M43.

SLU1 Receiver

SLU1 can be configured to receive either single-ended (RS-423) or differential (RS-422) asynchronous serial data in on connector J3. The factory-shipped configuration is for RS-423 input, with no jumper installed between pins M4 and M5. To select RS-422 input on SLU1, the user must install a jumper between pins M4 and M5.

SLU1 Baud Rate

The SLU1 output baud rate can be configured for either hardware or software control. With a jumper installed between pins M77 and M78, the baud rate is determined by the jumper configuration of pins M72 through M76, as shown in Table 7-7. If no jumper is installed between pins M77 and M78, the baud rate is under software control.

The KXT11-CA is factory-shipped with a hardwired SLU1 output baud rate of 9600.

Table 7-7 • KXT11-CA SLU1 Baud Rate Configuration

Baud Rate (Bits/S)	Jumper Connection M72 to M71	M74 to M73	M76 to M75
38400	IN	IN	IN
19200	IN	IN	OUT
9600	IN	OUT	IN
4800	IN	OUT	OUT
2400	OUT	IN	IN
1200	OUT	IN	OUT
600	OUT	OUT	IN
300	OUT	OUT	OUT

DMA Requests

There are three DMA request lines to the direct transfer controller (DTC). Two request lines come from SLU2 channels A (transmit and receive). The third request comes from the counter/timer (8036) chip. The user can select two of these three requests by configuring jumper pins M47 through M51, as shown in Table 7-8.

Table 7-8 ▪ KXT11-CA DMA Request Configuration

Jumper Connection	Description
M50 to M51	DMA request from SLU2 channel A (transmit)
M48 to M49	DMA request from counter/timer chip
M47 to M48	DMA request from SLU2 channel A (receive)

Note

Do not install a jumper between pins M49 and M50. This configuration is not supported.

SLU2 Channel A Receiver

The SLU2 channel A receiver can be configured for either single-ended (RS-423) operation or differential input (RS-422) operation, as shown in Table 7-9.

Table 7-9 ▪ KXT11-CA SLU2 Channel A Receiver Configuration

Jumper	Status	Description
M17 to M16	OUT	SLU2 channel A single-ended (RS-423) receiver operation
M15 to M14	OUT	
M13 to M12	OUT	
M11 to M10	OUT	
M9 to M8	OUT	
M7 to M6	OUT	
M17 to M16	IN	SLU2 differential input (RS-422)
M15 to M14	IN	
M13 to M12	IN	
M11 to M10	IN	
M9 to M8	IN	
M7 to M6	IN	

SLU2 Channel B Operation

SLU2 channel B can be configured to receive either driver (differential or single-ended) or party-line signals (CCITT R1360) on connector J2, as shown in Table 7-10.

Table 7-10 ▪ KXT11-CA SLU2 Channel B Configuration

Jumper Connection	Description
M45 to M6	R1360 party-line input signal
M44 to M45	TT104B input signal (RS-423)

SLU2 Channel B Receiver

The SLU2 channel B input can be configured for RS-422 (differential) or RS-423 (single-ended) receiver operation. Channel B output can be configured for either RS-422 (differential), RS-423 (single-ended), or party line (CCITT R1360) operation, as shown in Table 7-11.

Table 7-11 ▪ KXT11-CA SLU2 Channel B Receiver Configuration

Jumper	Status	Description
M38 to M37	OUT	RS-423 receiver operation
M36 to M35	OUT	
M34 to M33	OUT	
M38 to M37	OUT	RS-422 receiver operation
M36 to M35	IN	
M34 to M33	IN	
M38 to M37	IN	Party-line receiver operation
M36 to M35	OUT	
M34 to M33	OUT	

Note

When the SLU2 channel B receiver is configured for party-line operation, a jumper must be installed between pins M39 and M40 for party-line termination.

SLU2 Channel B Transmitter

The SLU2 channel B transmitter can be configured for either RS-423 (single-ended), RS-422 (differential), or party-line (CCITT 1360) operation, as shown in Table 7-12.

Table 7-12 ▪ KXT11-CA SLU2 Channel B Transmitter Configuration

Jumper Connection	Description
M30 to M31	RS-423 transmitter operation
M30 to M32 M27 to M28	RS-422 transmitter operation
M29 to M30 M39 to M40	CCITT 1360 party-line operation

Note

When the SLU2 channel B transmitter is configured for party-line operation, a jumper must be installed between pins M39 and M40 for party-line termination.

▪ Cables and Connectors

The KXT11-CA has a 40-pin connector (J4) for an external interface with the programmable I/O interface, a 40-pin connector for the full modem support interface (J1), and two 10-pin connectors (J2 and J3) for the external interface of the serial line units (SLUs). The locations of these connectors are shown in Figure 7-1.

Parallel I/O Interface (J4)

The I/O signals are buffered and are capable of driving up to 50 feet (maximum) of flat ribbon or round cable with a 40-pin AMP contact housing at each end. The following two cables are compatible with the module connector:

- BC05L mirror-image cable
- BC06R shielded-ribbon cable

Serial I/O Interfaces (J1, J2, and J3)

Each serial line unit (SLU) is compatible with EIA RS-232C and EIA RS-423 serial type interfaces. SLU1 interfaces through J3, SLU2 channel A interfaces through J1, while SLU2 channel B interfaces through J2.

The user provides the interconnecting cables. The following list describes some standard Digital cables for use with the KXT11-CA.

BC20N-05 5-foot EIA RS-232C null modem cable to directly interface with the EIA terminal (2 × 5 pin AMP female to RS-232C female)

BC21B-05 5-foot EIA RS-232C modem cable to interface with modems and acoustic couplers (2 × 5 pin AMP female to RS-232C male)

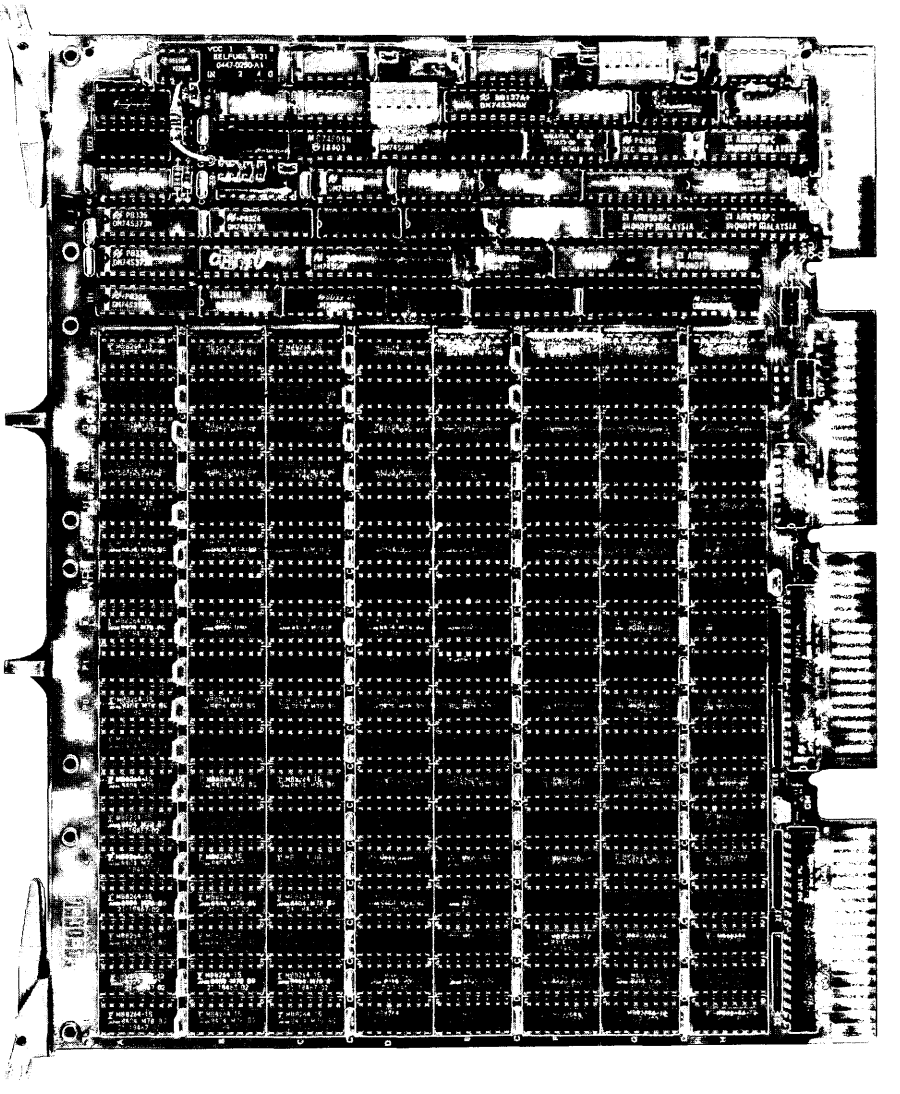
BC20M-50 50-foot EIA RS-422 or RS-423 cable for high throughput transmission (19.2 Kbaud) between two KXT11-CA computers (2 × 5 pin AMP female to 2 × 5 pin AMP female)

Loopback Connectors

Three loopback connectors — part numbers H3021, H3022 and H3270 — are used in testing the KXT11-CA single-board computer. Two 10-pin loopback connectors (H3270) are used with

- SLU2 channel B sync/async I/O connector J2
- SLU1 console I/O connector J3

The 40-pin loopback connector (H3022) is used with SLU2 channel A sync/async I/O connector J1. Note that the J1 connector can be configured, with 10 switches, for RS-422 or RS-423 loopback operation. The 40-pin loopback connector (H3021) is used with the parallel I/O connector J4.



Chapter 8 ▪ Introduction to Memories

Digital offers a wide range of microcomputer memory products, including RAM (random-access memory) read/write modules, ROM (read-only memory) modules, and PROM (programmable read-only memory) modules. The size of the memory array on a single board can range from 4 Kbytes to 4 Mbytes.

All memory boards include Q-bus interface logic, along with timing and control logic. In addition, each module's starting memory address is jumper-selectable to provide flexibility of memory layout within a system.

Additional features, described below, are available on selected memory boards. Table 8-1 summarizes the features of the various memory boards available for use with Q-bus microcomputers.

▪ Parity Operation

Some memory modules contain parity control circuitry that generates parity bits when data is written to memory, and tests parity bits when data is fetched from memory. Parity errors are detected and flagged for processing by the CPU, thereby eliminating the processing of faulty data and the execution of faulty software.

▪ Window Mapping

The MRV11-C and -D PROM/ROM modules can be configured to be accessed in one of two modes — direct addressing mode or page (or window mapping) mode. Direct addressing mode provides total access to all locations on the module. Window-mapped mode, on the other hand, is a virtual addressing scheme that uses two windows in the memory address space to access two segments of the memory array. Using this mode, two virtually adjacent segments can actually be located in nonadjacent physical address space.

▪ Refresh Circuitry

Dynamic metal oxide semiconductor (MOS) memory requires periodic refreshing to retain stored data. Memory modules with onboard refresh circuitry perform this function automatically, eliminating the need for control signals on the bus and thereby improving overall system performance.

▪ Battery Backup

The stored contents of MOS memory is volatile; that is, when operating power is lost, memory data is lost. However, memory contents can be protected during system power failures by supplying battery backup power. The MCV11-D RAM memory module has onboard battery backup. Other memory modules can be configured to support user-supplied battery backup capabilities.

▪ Bootstrap

Some PROM/ROM modules allow the user to install a bootstrap program in a portion of the memory array, thereby eliminating the need for an additional bootstrap board.

▪ I/O Page

In keeping with the standard PDP-11 architecture, the upper 4 Kwords of address space in all Q-bus systems is reserved for communications with peripheral devices. This area is known as the I/O page. Some memory modules, however, can be configured to permit the use of the lower 2 Kwords of the I/O page as actual memory locations. (Note that the system designer must exercise care in assigning these memory locations to avoid conflicts with peripheral device control and status registers.)

▪ Control and Status Registers

Some memory modules contain a control and status register (CSR) used to access certain module features under program control. In particular, the MRV11-C and -D PROM/ROM modules use the control and status register to control the window-mapping access mode, and the MSV11-L, -P and -Q RAM modules use the control and status register to permit program control of certain parity functions.

Table 8-1 ▪ Memory Board Summary/Comparison Chart

Feature	MCV11-D	MRV11-C	MRV11-D
Memory type	static CMOS RAM	user-supplied ROM/PROM	user-supplied ROM/PROM and static RAM
Memory size	8 Kbytes and 32 Kbytes	up to 64 Kbytes	up to 512 Kbytes
Bus addressing	selectable	18-bit	selectable
Window mapping	no	selectable	selectable
Bootstrap	no	yes	yes
Onboard refresh	n/a	n/a	n/a
Battery backup	onboard	n/a	selectable
Start address boundary	4-Kbytes	8-Kbytes[1]	4-Kbytes[1]
Modifiable I/O page	yes	no	no
Access time (DATI max)	250 nanoseconds	selectable	selectable
Parity operation	no	no	no
CSR register	no	yes[2]	yes[2]

Notes

1. In direct addressing mode
2. In window mapping mode
3. 22-bit only on the MSV11-PL
4. Not supported by Digital
5. Except for the MSV11-QA Etch Revision A

Table 8-1 ▪ Memory Board Summary/Comparison Chart (Cont.)

MSV11-D	MSV11-E	MSV11-L	MSV11-P	MSV11-Q
dynamic MOS RAM	dynamic MOS RAM	dynamic MOS RAM	dynamic MOS RAM	dynamic MOS RAM
4 Kbytes to 32 Kbytes	4 Kbytes to 32 Kbytes	128 Kbytes or 256 Kbytes	256 Kbytes or 512 Kbytes	1, 2 or 4 Mbytes
16-/18-bit	16-/18-bit	selectable	selectable[3]	22-bit
no	no	no	no	no
no	no	no	no	no
yes	yes	yes	yes	yes
selectable [4]	selectable [4]	selectable[4]	selectable[4]	selectable[5]
8-Kbytes	8-Kbytes	4-Kbytes	8-Kbytes	128-Kbytes
yes	yes	yes	no	no
225 nanoseconds	265 nanoseconds	230 nanoseconds	260 nanoseconds	358 nanoseconds
no	yes	selectable	yes	yes
no	no	selectable	yes	yes

Chapter 9 ▪ MCV11-D CMOS Read/Write Memory with Battery Backup

The MCV11-D is a static CMOS read/write memory with battery backup. The MCV11-D memory is available in two versions — the MCV11-DA and the MCV11-DC, with storage capacities of 8 Kbytes and 32 Kbytes, respectively.

▪ Specifications

Identification		M8631		
Size		Dual		
Bus Loads				
ac		2.0		
dc		1.0		
Power Requirements				
		Active	**Standby**	**Data Retention**
MCV11-DC (32 Kbytes):				
Current	+5 V Typical*	1.23 A	1.22 A	0
	+5 V Maximum*	2.16 A	2.15 A	0
	+5 V BBU Typical†	1 mA	1 mA	9 mA
	+5 V BBU Maximum†	2 mA	2 mA	14 mA
Power	+5 V Typical	6.2 W	6.1 W	0.045 W
	+5 V Maximum	11.34 W	11.29 W	0.073 W
MCV11-DA (8 Kbytes):				
Current	+5 V Typical*	1.20 A	1.19 A	0
	+5 V Maximum*	2.09 A	2.08 A	0
	+5 V BBU Typical†	1 mA	1 mA	9 mA
	+5 V BBU Maximum†	2 mA	2 mA	14 mA
Power	+5 V Typical	6.0 W	5.95 W	0.045 W
	+5 V Maximum	10.97 W	10.92 W	0.073 W

* +5 V current is recorded with no +5 V BBU supply connected.

† +5 BBU current assumes +5 V equals 4.75 V and +5 BBU equals 5.25 V. In the active and standby mode, a majority of current comes from the +5 V supply. Thus, it appears

as though very little current is required by the +5 BBU supply. In the data retention mode, the +5 V supply is assumed to be at 0 V. The current supplied by +5 BBU is used to trickle charge the batteries. If the batteries were disconnected, +5 BBU would be typically 20 μA.

Data Retention

MCV11-DC	1180 hr (typical); 100 hr (minimum)
MCV11-DA	2647 hr (typical); 333 hr (minimum)

Access and Cycle Times

	Access Time (ns)			Cycle Time (ns)		
Bus Cycle	**Typical**	**Maximum**	**Notes**	**Typical**	**Maximum**	**Notes**
DATI	225	250	(1)	520	570	(4)
DATO(B)	50	55	(2)	500	550	(4)
DATIO(B)	590	620	(3)	1010	1070	(5)

Notes

1. R SYNC to T RPLY with minimum timing (25 ns) from R SYNC to R DIN and typical or maximum module propagation delays.
2. R SYNC to T RPLY with minimum timing (50 ns) from R SYNC to R DOUT typical or maximum module propagation delays.
3. R SYNC to T RPLY (DATO portion of the bus cycle) with minimum timing (25 ns) from R SYNC to R DIN and minimum timing (350 ns) from T RPLY (DATI portion of cycle) to R DOUT.
4. R SYNC to TIM 130 negated.
5. R SYNC to TIM 130 negated (DATO).

Nonstandard Environmental Specifications

Storage Temperature	-30°C to 60°C (-22°F to 140°F)

▪ Related Documentation

Document Title	Order Number
MCV11-D User's Guide	EK-MCV1D-UG
MCV11-D Reference Card	EK-MCV1D-RC
MCV11-D Field Maintenance Print Set	MP-01309-00

▪ Configuration

The MCV11-D is configured by means of several wirewrap jumpers, as shown in Figure 9-1. The user can configure the following MCV11-D features:

- Module starting address
- 16-, 18-, or 22-bit addressing
- Memory I/O page size
- Battery backup

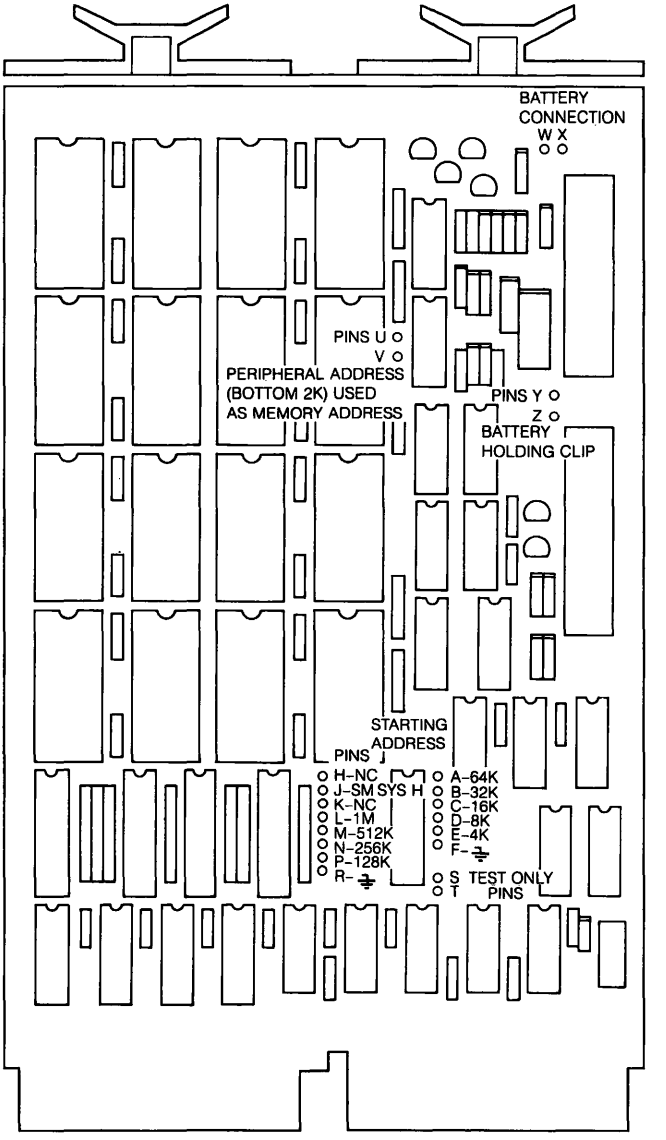


Figure 9-1 ▪ MCV11-D Module Layout

Module Starting Address (MSA)

The module starting address is equal to the number of decimal Kwords already configured in the system. Jumpers L, M, N, P, and R select the first address in the 128-Kword block of addresses that contains the module's MSA. Jumpers A, B, C, D, E, and F select the particular 4-Kword increment in that 128-Kword block where the MSA begins. The 128-Kword block selected is called the FAR (First Address Range). The 2-Kword increment is called the PSA (Partial Starting Address). The following equation shows how the MSA, FAR, and PSA are related:

PSA = MSA–FAR

Refer to Tables 9-1 and 9-2 for jumper locations for the FAR and PSA, respectively.

Table 9-1 ▪ MCV11-D FAR Jumper Configurations

First Address Range (FAR)		Jumpers In (X) to Ground (R)			
Decimal(K)	Octal	L	M	N	P
000-124	00000000-00760000				
128-252	01000000-01760000				X
256-380	02000000-02760000			X	
384-508	03000000-03760000			X	X
512-636	04000000-04760000		X		
640-764	05000000-05760000		X		X
768-892	06000000-06760000		X	X	
896-1020	07000000-07760000		X	X	X
1024-1148	10000000-10760000	X			
1152-1276	11000000-11760000	X			X
1280-1404	12000000-12760000	X		X	
1408-1532	13000000-13760000	X		X	X
1536-1660	14000000-14760000	X	X		
1664-1788	15000000-15760000	X	X		X
1792-1916	16000000-16760000	X	X	X	
1920-2044	17000000-17760000	X	X	X	X

Note

The MCV11-D is shipped for 18-bit systems. For applications in which the module is configured outside this address space, the module must be configured for 22-bit addressing by inserting a jumper from pin J to R.

Table 9-2 ▪ MCV11-D PSA Jumper Configurations

Partial Starting Address (PSA)		Jumpers in (X) to Ground (R)				
Decimal(K)	**Octal**	**A**	**B**	**C**	**D**	**E**
0	00000000					
4	00020000					X
8	00040000				X	
12	00060000				X	X
16	00100000			X		
20	00120000			X		X
24	00140000			X	X	
28	00160000			X	X	X
32	00200000		X			
36	00220000		X			X
40	00240000		X		X	
44	00260000		X		X	X
48	00300000		X	X		
52	00320000		X	X		X
56	00340000		X	X	X	
60	00360000		X	X	X	X
64	00400000	X				
68	00420000	X				X
72	00440000	X			X	
76	00460000	X			X	X
80	00500000	X		X		
84	00520000	X		X		X
88	00540000	X		X	X	
92	00560000	X		X	X	X
96	00600000	X	X			
100	00620000	X	X			X
104	00640000	X	X		X	

(continued on next page)

Table 9-2 ▪ MCV11-D PSA Jumper Configurations (Cont.)

Partial Starting Address (PSA)		Jumpers in (X) to Ground (R)				
Decimal(K)	Octal	A	B	C	D	E
108	00660000	X	X		X	X
112	00700000	X	X	X		
116	00720000	X	X	X		X
120	00740000	X	X	X	X	
124	00760000	X	X	X	X	X

Taking an MSA of 336 Kword as an example, find the FAR in Table 9-1 by locating the first address in the block with the 336th location. This is 256, the FAR value. To find the PSA, subtract 256 from 336. This yields a PSA of 80. Jumper the FAR of 256 by connecting pin N to pin R (ground). Jumper the PSA of 80 by connecting pin A to pin C to pin F (ground).

Selecting 16-, 18-, or 22-bit Addressing

The MCV11-D will support either 16-, 18-, or 22-bit addressing. To select 16- or 18-bit addressing, remove the jumper at pin J. To select 22-bit addressing, connect pin J to R (ground).

Modifying the I/O Page

The top 4 Kwords of address space are usually reserved to address I/O devices. The user may modify the I/O page by jumpering pin U to pin V. This will add the bottom 2 Kwords of the I/O page to memory.

Enabling Battery Backup

The MCV11-D module comes with two batteries already installed. To enable the battery backup function, remove the clip across pins Y and Z and connect it to pins W and X.

The two batteries included with the module are rechargeable nickel cadmium cylindrical cells. Each cell is size AAA, 1.2 V nominal, with a 180 mA hr capacity at 25°C (77°F). The battery operating life is projected at over five years at normal operating temperatures. If the operating temperatures are continuously high, battery life will be shortened substantially. Battery life is sustained for approximately one year in a 60°C (140°F) environment. It is recommended that the module be kept in operation until the battery fails to hold a charge sufficient for the system's application. Only in the most demanding situations, where a data retention loss proves very costly, should a battery replacement schedule be advised. In these situations, the use of an external remote monitored power source on the BBU pin is recommended.

The charge rate for the batteries is approximately 12 mA as long as +5 V is present. It takes 24 hours to totally charge a fully discharged battery. For every hour of charging, approximately 1/24th of the total charge will be replaced.

Chapter 10 ▪ MRV11-C Read-Only Memory Module

The MRV11-C module contains sixteen 24-pin sockets that accept a variety of user-supplied ROM chips. It accepts masked ROMs, fusible link PROMs, and ultraviolet erasable PROMs. It accepts several densities of ROM chips up to and including 4K × 8 chips. Using these high-density chips gives the module a total capacity of 64 Kbytes. The contents of the module can be accessed in either of two ways—directly or window-mapped. A bootstrap capability allows the top 256 words of any 2-Kword page to contain a bootstrap program.

▪ Specifications

Identification	M8048
Size	Dual
Power Requirements	+5 Vdc, 0.8 A
Bus Loads	
ac	2.0
dc	1.0
ROM Specifications	
Power	+5 V ±5%
Pins	24-pin spacing
Access Time	Up to 450 ns
Size	1K × 8, 2K × 8, or 4K × 8 bits
Type	See tables below

UV PROMs

	Chip Array Size	Maximum Memory Size
Intel 2758	1K × 8	16 Kbytes
Intel 2716	2K × 8	32 Kbytes
Intel 2732	4K × 8	64 Kbytes
Mostek MK2716	2K × 8	32 Kbytes
TI TMS 2516	2K × 8	32 Kbytes
TI TMS 2532	4K × 8	64 Kbytes

PROMs

	Chip Array Size	Maximum Memory Size
Intel 3628	1K × 8	16 Kbytes
Signetics 82S 2708	1K × 8	16 Kbytes
Signetics 82S 181	1K × 8	16 Kbytes
Signetics 82S 191	2K × 8	32 Kbytes

▪ Related Documentation

Document Title	Order Number
MRV11-C Field Maintenance Print Set	MP-00871-00

▪ Configuration

The MRV11-C read-only memory (ROM) contains 129 wirewrap pins and 16 ROM chip sockets. The user configures module features by installing jumper wires between the wirewrap pins. The user can configure the following items:

- Memory size
- Direct addressing mode
- Window-mapping mode
- Bootstrap
- Use of multiple MRV11 boards
- ROM chips
- Chip access time
- DATIO bus cycle inhibit

The size of the memory array is determined by the size of the ROM chips installed. The user provides these chips and inserts them into the sockets. All the ROM chips must be the same array size; that is, either 1K × 8, 2K × 8, or 4K × 8 bits. The pin configuration of the chips must also be the same. The user can populate the MRV11-C for any of the three maximum memory sizes — 16, 32, or 64 Kbytes. Subsets of these sizes can also be chosen as shown in Table 10-1. In addition, the user can configure the MRV11-C to be part of a system with more than one MRV11-C module.

Table 10-1 ▪ Storage Capacity per Board as a Function of Chip Array Size and Number of Chips

Number of Chips Installed	Chip Array Size 2758 (Typical) 1024 × 8	2716 (Typical) 2048 × 8	2732 (Typical) 4096 × 8
2	2 Kbytes	4 Kbytes	8 Kbytes
4	4 Kbytes	8 Kbytes	16 Kbytes
6	6 Kbytes	12 Kbytes	24 Kbytes
8	8 Kbytes	16 Kbytes	32 Kbytes
10	10 Kbytes	20 Kbytes	40 Kbytes
12	12 Kbytes	24 Kbytes	48 Kbytes
14	14 Kbytes	28 Kbytes	56 Kbytes
16	16 Kbytes	32 Kbytes	64 Kbytes

The MRV11-C ROM module operates in either the direct addressing mode or the window mapping mode. In the direct addressing mode, the user's program addresses physical memory directly. In the window mapping mode, the user's program addresses a continuous virtual address space that the MRV11-C breaks up into 2-Kbyte segments of physical address space. The 2-Kbyte segments need not be physically adjacent to each other in memory.

The user can also select the starting address of a bootstrap on the module (within the bootstrap address region: 173000_8 to 173776_8.) The bootstrap option can be disabled or can be enabled for use in either addressing mode.

The chip access time must be selected to accommodate the chips with the slowest access time. The user should also inhibit DATIO bus cycles to prevent attempted writes to read-only memory.

The physical locations of the pins are detailed in Figure 10-1. The module is shipped from the factory with no jumper wires installed.

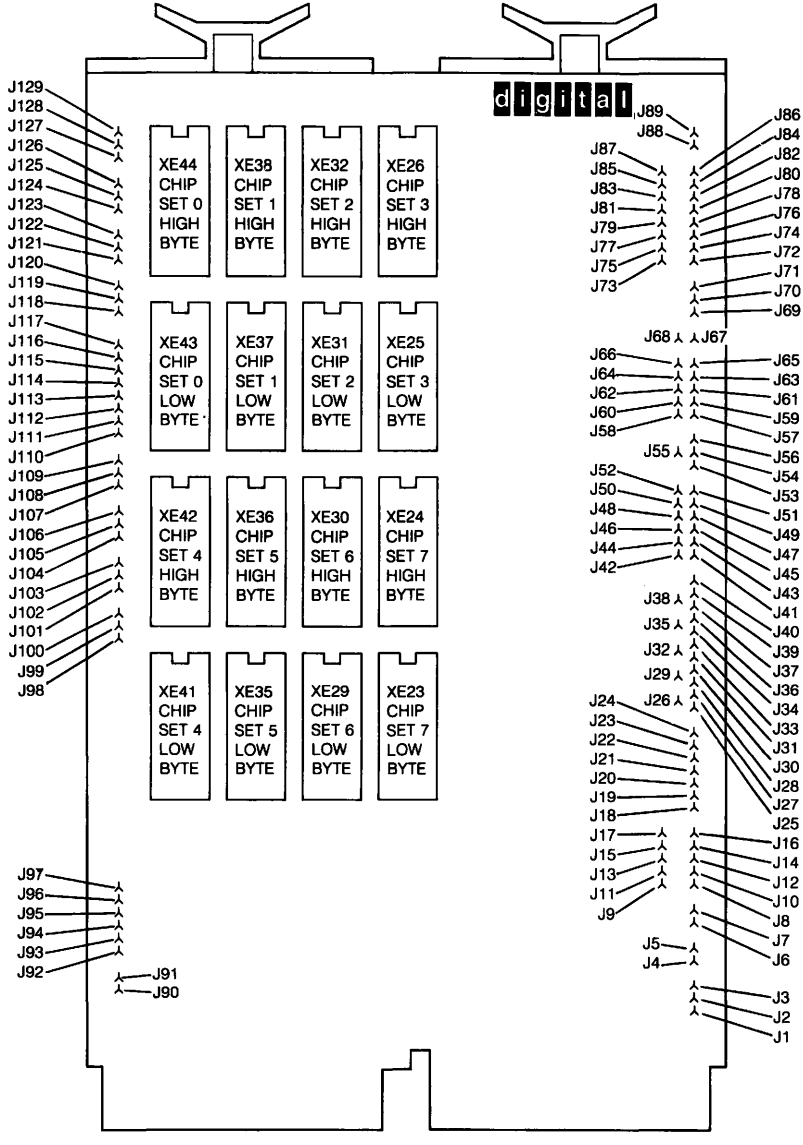


Figure 10-1 ▪ MRV11-C Wirewrap Pin Locations

Direct Addressing Mode

When in direct mode, the MRV11-C serves as a high-density replacement for the MRV11-AA or MRV11-BA ROM modules. The base address of the direct mode ROM area is assignable on any 8-Kbyte boundary from 0 to 248 Kbytes (addresses 000000_8 to 760000_8). When operated in this mode, the application program executes directly from the MRV11-C physical memory.

In direct mode, address bits AD11 through AD15 are used to access data in the ROM. Bits AD14 and AD15 are decoded to enable the memory chips. Bits AD11 and AD12 are used to determine which portion of the chip is being accessed. Only address bits AD13, AD14, and AD15 are used in 64-Kbyte systems, but all five address bits (AD13 through AD17) are used for 256-Kbyte systems. The starting address must be configured to start on 8-Kbyte boundaries as determined by the user.

The range of the direct addresses required depends on the amount of memory installed on the module. The minimum is 2 Kbytes and the maximum is 64 Kbytes. Once the address space is determined, the starting address is configured by installing jumper wires. All the jumper wire configurations for the 8-Kbyte (4-Kword) boundaries are listed in Table 10-2.

Table 10-2 ▪ MRV11-C Jumper Configurations for 8-Kbyte Boundaries

Starting Address	Bank	Bit 17 57 to 60	Bit 16 59 to 58	Bit 15 61 to 62	Bit 14 63 to 64	Bit 13 65 to 66
000000	0	I	I	I	I	I
020000	1	I	I	I	I	R
040000	2	I	I	I	R	I
060000	3	I	I	I	R	R
100000	4	I	I	R	I	I
120000	5	I	I	R	I	R
140000	6	I	I	R	R	I
160000	7	I	I	R	R	R
200000	10	I	R	I	I	I
220000	11	I	R	I	I	R
240000	12	I	R	I	R	I
260000	13	I	R	I	R	R
300000	14	I	R	R	I	I
320000	15	I	R	R	I	R
340000	16	I	R	R	R	I
360000	17	I	R	R	R	R

(continued on next page)

Table 10-2 ▪ MRV11-C Jumper Configurations for 8-Kbyte Boundaries (Cont.)

Starting Address	Bank	Bit 17 57 to 60	Bit 16 59 to 58	Bit 15 61 to 62	Bit 14 63 to 64	Bit 13 65 to 66
400000	20	R	I	I	I	I
420000	21	R	I	I	I	R
440000	22	R	I	I	R	I
460000	23	R	I	I	R	R
500000	24	R	I	R	I	I
520000	25	R	I	R	I	R
540000	26	R	I	R	R	I
560000	27	R	I	R	R	R
600000	30	R	R	I	I	I
620000	31	R	R	I	I	R
640000	32	R	R	I	R	I
660000	33	R	R	I	R	R
700000	34	R	R	R	I	I
720000	35	R	R	R	I	R
740000	36	R	R	R	R	I
760000	37	R	R	R	R	R

I = Jumper installed; R = jumper removed

The starting address and the bank of addresses assigned determine the addressing sequence of the ROM chips. Figure 10-2 shows examples of 32- and 64-Kbyte memories and how the starting address determines which chip is accessed. The user must insert the ROM chips according to the starting address if the data is to be accessed in correct sequential order.

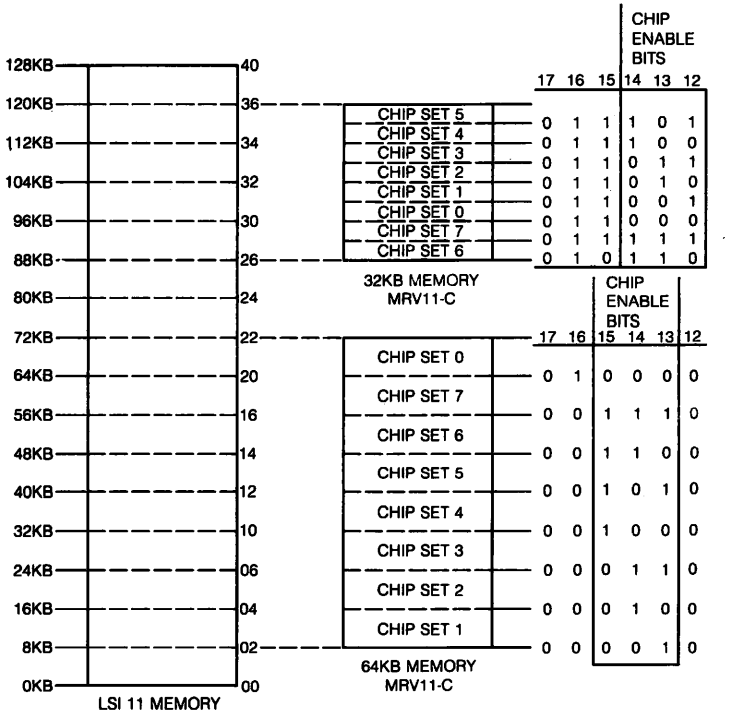


Figure 10-2 ▪ Typical MRV11-C Memory Mapping

For a 64-Kbyte memory the desired starting address is 20000_8, at the 8-Kbyte boundary. For this size memory, address bits <13:15> are decoded to select one of the eight pairs of ROM sockets. Expanding address 20000_8 in binary (i.e., 000 010 000 000 000 000) shows that with this starting address, the first chip set selected is chip set 1.

The starting chip set can be determined similarly for a 32-Kbyte memory. In this case, address bits <12:14> are the chip enable bits, with a starting address at the 8-Kbyte boundary (address 260000_8, or 010 110 000 000 000 000). Chip set 6 is the first set to be accessed. Likewise, a 16-Kbyte memory uses address bits <11:13> as the chip select bits.

Tables 10-3, 10-4, and 10-5 respectively summarize the proper jumper locations for 16-, 32-, and 64-Kbyte direct addressing modes.

Table 10-3 ▪ MRV11-C 16-Kbyte Direct Addressing Jumpers

Function	Jumpers Installed
Enable low-byte MUX	J70 to J71
Disable window mode	J6 to J7
Enable 16K direct mode	J55 to J56
Address bit AD11	J25 to J32
Address bit AD12	J28 to J35
Address bit AD13	J31 to J38

Table 10-4 ▪ MRV11-C 32-Kbyte Direct Addressing Jumpers

Function	Jumpers Installed
Enable low-byte MUX	J70 to J71
Disable window mode	J6 to J7
Enable 32K direct mode	J54 to J55
Chip enable input, address bit AD11	J112 to J113
Address bit AD11	J25 to J26
Address bit AD12	J28 to J32
Address bit AD13	J31 to J35
Address bit AD14	J34 to J38

Table 10-5 ▪ MRV11-C 64-Kbyte Direct Addressing Jumpers

Function	Jumpers Installed
Enable low-byte MUX	J70 to J71
Disable window mode	J6 to J7
Enable 64K direct mode	J53 to J55
Chip enable input, address bit AD11	J112 to J113
Chip enable input, address bit AD12	J115 to J116
Address bit AD11	J25 to J26
Address bit AD12	J28 to J29
Address bit AD13	J31 to J32
Address bit AD14	J34 to J35
Address bit AD15	J37 to J38

Window-mapping Mode

When window-mapping mode is selected, the entire ROM is not visible to the Q-bus address space at any particular point in time. Instead, any two 2-Kbyte segments of the ROM can be addressed through two independent windows defined by the system's address space. The association of segments of the ROM board with windows is controlled by a control and status register (CSR).

The window address function uses a comparator to monitor address bits A16, A17, DAL 12, and DAL 15. The user wires the desired address to the comparator and when the bus selects one of these addresses, the window function is enabled.

- WINDOW DEFINITION

Each MRV11-C board provides a pair of 2-Kbyte windows. These windows are always contiguous with each other, and the base address of the window pair may be set to any 4-Kbyte boundary in the Q-bus address space from 000000_8 to 770000_8. To maximize the amount of space left for system RAM, a default window base of 160000_8 (760000_8 for 18-bit systems) is suggested.

Each MRV11-C uses one 16-bit CSR located in the system I/O page to determine mapping of ROM segments into windows. The default address for this CSR is 177000_8 (777000_8 in 18-bit systems). The valid address range for CSRs is 177000_8 to 177036_8 (777000_8 to 777036_8 in 18-bit systems). Figure 10-3 shows the bit assignments for the MRV11-C control and status register. Table 10-6 lists the control and status register addresses.

Table 10-6 ▪ MRV11-C Control and Status Register Addresses

CSR Address	Bit 4 J90 to J91	Bit 3 J96 to J97	Bit 2 J94 to J95	Bit 1 J92 to J93
177000	R	R	R	R
177002	R	R	R	I
177004	R	R	I	R
177006	R	R	I	I
177010	R	I	R	R
177012	R	I	R	I
177014	R	I	I	R
177016	R	I	I	I
177020	I	R	R	R
177022	I	R	R	I
177024	I	R	I	R
177026	I	R	I	I
177030	I	I	R	R
177032	I	I	R	I
177034	I	I	I	R
177036	I	I	I	I

I = jumper installed; R = jumper removed

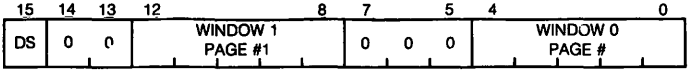


Figure 10-3 ▪ MRV11-C Control and Status Register Format

The CSR contains a 5-bit read/write field for each window. The number stored in this field (0 to 31_{10}) selects the desired 2-Kbyte region from the MRV11-C board to be associated with the window in question. CSR bits <0:4> control the mapping of the low-address window, window 0. The low-order five bits of the upper byte (bits <8:12>) control the mapping of window 1.

The MRV11-C optionally provides a window enable/disable capability. When this option is selected, bit 15 of the CSR is used to enable or disable window response under program control. When bit 15 is a 0, the board will respond to references to the CSR or DATI or DATIO references to either of the windows. When bit 15 is a 1, only the CSR will respond. If the enable/disable option is not selected, bit 15 of the CSR will be read-only and will always be zero. The enable/disable bit has no effect on direct-mode addressing or the bootstrap window capability.

The remaining bits in the CSR (bits <5:7> and <13:14>) are reserved and must always be zero.

Tables 10-7, 10-8, and 10-9 respectively summarize the proper jumper connections for 16-, 32-, and 64-Kbyte window-mapping modes.

Table 10-7 ▪ MRV11-C 16-Kbyte Window-mode Jumpers

CSR Output	Jumpers Installed
Low Byte	
CSR bit 0	J27 to J32
CSR bit 1	J30 to J35
CSR bit 2	J33 to J38
High Byte	
CSR bit 8	J9 to J12
CSR bit 9	J11 to J14
CSR bit 10	J13 to J16
Enable low-byte MUX	J69 to J71

Table 10-8 ▪ MRV11-C 32-Kbyte Window Mode Jumpers

CSR Output	Jumpers Installed
Low Byte	
CSR bit 0	J27 to J26
CSR bit 1	J30 to J32
CSR bit 2	J33 to J35
CSR bit 3	J36 to J38
High Byte	
CSR bit 8	J9 to J8
CSR bit 9	J11 to J12
CSR bit 10	J13 to J14
CSR bit 11	J15 to J16
Enable low-byte MUX	J69 to J71
Address bit AD11	J112 to J113

Table 10-9 ▪ MRV11-C 64-Kbyte Window Mode Jumpers

CSR Output	Jumpers Installed
Low Byte	
CSR bit 0	J27 to J26
CSR bit 1	J30 to J29
CSR bit 2	J33 to J32
CSR bit 3	J36 to J35
CSR bit 4	J39 to J38
High byte	
CSR bit 8	J9 to J8
CSR bit 9	J11 to J10
CSR bit 10	J13 to J12
CSR bit 11	J15 to J14
CSR bit 12	J17 to J16
Enable low-byte MUX	J69 to J71
Address bit AD11	J112 to J113
Address bit AD12	J115 to J116

- STARTING ADDRESS OF WINDOWS

  Wirewrap pins J41 through J52 are used to configure the starting address of windows. The user selects an address and installs the jumper wires as directed in Figure 10-4. The recommended value of the window starting is 160000_8 (or 760000_8 for 18-bit systems). This places the window at the bottom of the I/O page.

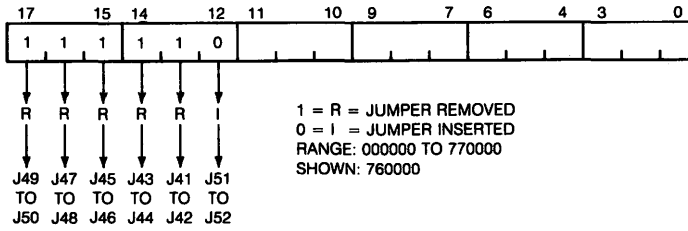


Figure 10-4 ▪ MRV11-C Window Starting Address Selection

Note

The MRV11-C does not select the I/O page on the BBS7 (bank select 7) signal for windows placed in the I/O page. Therefore, the entire address for the window must be asserted by the processor and decoded by the MRV11-C. An LSI-11/23 processor asserts an address of 760000_8 only in 18-bit mode, (i.e., when the memory management unit is enabled) and bank 7 is mapped to the I/O page.

Bootstrap

The MRV11-C allows the user to install a bootstrap program of up to 512 bytes. The bootstrap starting address is hardwired for 16-bit systems at 173000_8 and for 18-bit systems at 773000_8. The bootstrap program is normally enabled and must be disabled if it is not being used. To disable the bootstrap, install a jumper wire between wirewrap pins J88 and J89. The bootstrap program is inserted as the top 512 bytes of any 2-Kbyte page of ROM. The user installs jumper wires for the boot multiplexer to select the starting address for the particular page in which the bootstrap resides. The number of pages vary by the array size of the ROM chips.

Refer to Tables 10-10, 10-11, and 10-12 respectively to jumper the bootstrap starting address of 16-, 32-, and 64-Kbyte ROM memory systems.

Table 10-10 ▪ MRV11-C Bootstrap Starting Address (16-Kbyte ROM)

Starting Address	Install Jumper Wire from J22 to	J21 to	J20 to
003000	J24	J24	J24
007000	J24	J24	J23
013000	J24	J23	J24
017000	J24	J23	J23
023000	J23	J24	J24
027000	J23	J24	J23
033000	J23	J23	J24
037000	J23	J23	J23

Logic 1 = J23; logic 0 = J24

Bootstrap starting address is normalized to memory location 000000.

Table 10-11 ▪ MRV11-C Bootstrap Starting Address (32-Kbyte ROM)

Starting Address	Install Jumper Wire from J22 to	J21 to	J20 to	J18 to
003000	J24	J24	J24	J24
007000	J24	J24	J24	J23
013000	J24	J24	J23	J24
017000	J24	J24	J23	J23
023000	J24	J23	J24	J24
027000	J24	J23	J24	J23
033000	J24	J23	J23	J24
037000	J24	J23	J23	J23
043000	J23	J24	J24	J24
047000	J23	J24	J24	J23
053000	J23	J24	J23	J24
057000	J23	J24	J23	J23

(continued on next page)

Table 10-11 ▪ MRV11-C Bootstrap Starting Address (32-Kbyte ROM) (Cont.)

Starting Address	Install Jumper Wire from J22 to	J21 to	J20 to	J18 to
063000	J23	J23	J24	J24
067000	J23	J23	J24	J23
073000	J23	J23	J23	J24
077000	J23	J23	J23	J23

Logic 1 = J23; logic 0 = J24

Bootstrap starting address is normalized to memory location 000000.

Table 10-12 ▪ MRV11-C Bootstrap Starting Address (64-Kbyte ROM)

Starting Address	Install Jumper Wire from J22 to	J21 to	J20 to	J19 to	J18 to
003000	J24	J24	J24	J24	J24
007000	J24	J24	J24	J24	J23
013000	J24	J24	J24	J23	J24
017000	J24	J24	J24	J23	J23
023000	J24	J24	J23	J24	J24
027000	J24	J24	J23	J24	J23
033000	J24	J24	J23	J23	J24
037000	J24	J24	J23	J23	J23
043000	J24	J23	J24	J24	J24
047000	J24	J23	J24	J24	J23
053000	J24	J23	J24	J23	J24
057000	J24	J23	J24	J23	J23
063000	J24	J23	J23	J24	J24
067000	J24	J23	J23	J24	J23
073000	J24	J23	J23	J23	J24
077000	J24	J23	J23	J23	J23
103000	J23	J24	J24	J24	J24

(continued on next page)

Table 10-12 ▪ MRV11-C Bootstrap Starting Address (64-Kbyte ROM) Cont.

Starting Address	Install Jumper Wire from J22 to	J21 to	J20 to	J19 to	J18 to
107000	J23	J24	J24	J24	J23
113000	J23	J24	J24	J23	J24
117000	J23	J24	J24	J23	J23
123000	J23	J24	J23	J24	J24
127000	J23	J24	J23	J24	J23
133000	J23	J24	J23	J23	J24
137000	J23	J24	J23	J23	J23
143000	J23	J23	J24	J24	J24
147000	J23	J23	J24	J24	J23
153000	J23	J23	J24	J23	J24
157000	J23	J23	J24	J23	J23
163000	J23	J23	J23	J24	J24
167000	J23	J23	J23	J24	J23
173000	J23	J23	J23	J23	J24
177000	J23	J23	J23	J23	J23

Logic 1 = J23; logic 0 = J24

Use of Multiple MRV11-C Boards

Up to 16 MRV11-C boards can be configured in a single system. When multiple boards are present, each board has a unique control and status register address assigned in increasing order from location 177000_8 (777000_8 in 18-bit systems). Refer to Table 10-6 to configure CSR addresses. Each board can have a unique 4-Kbyte area of the physical address space set aside for its windows, but it is also possible to share one 4-Kbyte area of the address space among all MRV11-C boards installed in the system.

The window enable bit of the CSR (bit 15) is used to provide the user software control over the windows. Setting bit 15 to 1 disables both windows on the respective MRV11-C. In order to use bit 15 of the CSR, a jumper must be installed between pins J67 and J68 on all MRV11-C modules that must be disabled under software control, such as modules configured with the same window starting addresses. With the jumper installed, bit 15 will also be set upon system initialization so that module will be disabled on powerup.

When enable/disable is implemented, the disable bit in the CSR is set automatically by BINIT on the bus or by execution of the RESET instruction. Therefore, the initial state of the system will have all boards disabled. To access a particular segment of ROM in this multiboard configuration, the programmer first enables the desired board and maps the segment. When access to that segment is completed, the board is again disabled to allow another board to be selected at a future time.

ROM Chips

There are 16 sockets on the MRV11-C module available for ROM chips. If the module is not fully populated, then the chip-enable signals for the sockets without ROMs should not be jumpered. This prevents the program from accidentally addressing the sockets in which there are no ROMs. It is recommended that the ROMs be installed in pairs of high and low bytes. When a complete set of ROMs is installed, then all the chip-enable jumper wires are installed as listed in Table 10-13.

Table 10-13 ▪ MRV11-C Chip-enable Jumpers

Sockets Enabled	Chip-enable Signal	Wirewrap Pins Jumpered
XE43, XE44	CE0	J86 to J87
XE37, XE38	CE1	J84 to J85
XE31, XE32	CE2	J82 to J83
XE25, XE26	CE3	J80 to J81
XE41, XE42	CE4	J78 to J79
XE35, XE36	CE5	J76 to J77
XE29, XE30	CE6	J74 to J75
XE23, XE24	CE7	J72 to J73

The ROM is provided by the user and consists of up to 16 chips that are inserted into prewired sockets. The chips will be either 1K × 8 bit, 2K × 8 bit, or 4K × 8 bit ROMs. When the MRV11-C is fully populated, the result will be either 16, 32, or 64 Kbytes of memory. These ROMs can be supplied by a variety of vendors and the basic configuration for many of the ROMs is standardized except for pins 18, 19, 20, and 21. The configuration of these pins will vary depending upon the size of the ROM and the vendor who supplies them. Therefore the user should verify the vendor's specifications in order to determine if a particular ROM can be used on the MRV11-C.

The MRV11-C module is configured so that the user can select the signals that are applicable to pins 18, 19, and 21. The board provides wirewrap pins for the user to select A11, A12, +5 Vdc or ground. There are three individual loops that interconnect all chips and three wirewrap pins available for each individual chip. Wirewrap pin J112 interconnects pin 19 of all the chips and pin J116 interconnects pin 21 of all the chips; these are normally designated as the A10 or A11 inputs to the chips. Wirewrap pin J114 interconnects wirewrap pins that are individually associated with each chip. Pin 18 of each chip is individually wired to a wirewrap pin and chip pin 20 is wired to the chip-enable signal. Chip pin 20 is also individually wired to a wirewrap pin. The user must determine from the vendor's specifications which signals apply to which pins and must install jumper wires as needed to configure an operational module.

For example, in Figure 10-5 there are pin configurations for two types of chips, a 2K × 8 ROM that is used for 32-Kbyte memories and a 4K × 8 ROM that is used for 64-Kbyte memories. To configure the 32-Kbyte ROM memory, pin 19 is designated as A10 and, by inserting a jumper wire between pins J112 and J113, pin 19 of all the chips is connected to A11 which is used as the A10 input. The V_{pp} input, designated by pin 21, is specified that it must be connected to a +5 Vdc source. This is accomplished by inserting a jumper wire between pins J116 and J117, which will connect pin 21 of all the chips to +5 Vdc. The OE (pin 20) and CE (pin 18) should be connected together to the chip enable. Therefore each chip must be connected individually and jumper wires are installed between the following pins to operate as a 32-Kbyte memory:

J118	to	J120
J121	to	J123
J124	to	J126
J127	to	J129
J101	to	J103
J98	to	J100
J104	to	J106
J107	to	J109

Using the 4K × 8 ROM to configure a 64-Kbyte memory, pin 19 is designated as A10 and by inserting a jumper wire between pins J112 and J113, pin 19 of all the chips is connected to A11 which is used as the A10 input. However, pin 21 is now designated as A11 and this must be connected to A12. This is accomplished by inserting a jumper wire between pins J116 and J115, that will connect pin 21 of all the chips to A12. The $\overline{OE}/V_{pp}$ (pin 20) and $\overline{CE}$ (pin 18) should be connected together to the chip enable. Therefore each chip must be connected individually and jumper wires installed between the following pins to operate as a 64-Kbyte memory:

J118	to	J120
J121	to	J123
J124	to	J126
J127	to	J129
J101	to	J103
J98	to	J100
J104	to	J106
J107	to	J109

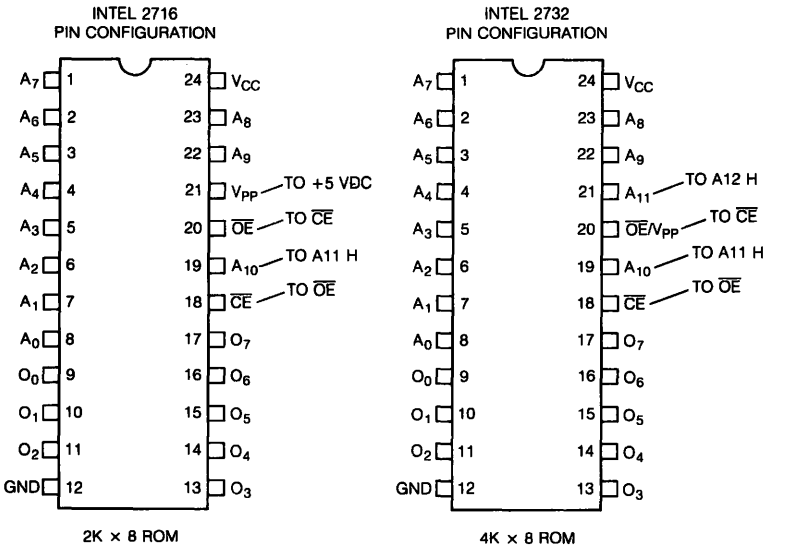


Figure 10-5 ▪ 2K × 8 and 4K × 8 Pin Configurations

Chip Access Time

The MRV11-C can normally interface with chips that have an access time of less than 50 ns. The chip access time is determined by the slowest access time of any individual chip installed on the MRV11-C. If the chip access time is greater than 50 ns and less than 200 ns, then an RC delay can be incorporated into the circuits. This is done by installing jumper wires between wirewrap pins J1 and J3 and pins J2 and J3. If the chip access time is greater than 200 ns and less than or equal to 450 ns, the jumper wire between wirewrap pins J1 and J3 is removed and the jumper wire between wirewrap pins J2 and J3 remains inserted.

DATIO Bus Cycle Inhibit

The processor may attempt to perform DATIO bus cycles to the MRV11-C. These bus cycles are attempts to write the data into the memory (which is read-only memory). This condition is allowed unless a jumper wire is installed between wirewrap pins J4 and J5. With this jumper installed, the BDOUT is inhibited except when the bus is addressing the CSR. This eliminates any writing attempts from the bus except those for the control/status register. The MRV11-C normally responds to DATIO bus cycles and installing the jumper will cause a timeout for a DATIO bus cycle to the ROM.

Wirewrap Pin Identification

The MRV11-C module provides the user with 129 wirewrap pins to configure the module for many types of applications. These wirewrap pins are identified and located on the module in Figure 10-1. In Table 10-14, the wirewrap pins are numerically listed with descriptions of their functional use.

Table 10-14 ▪ MRV11-C Wirewrap Pin Identification

Pin Designation	Function
J1	RXCX pull-up resistor
J2	RXCX optional capacitor
J3	RXCX signal
J4	LMATCH input for BDOUT control
J5	LMATCH for BDOUT control
J6	Window address enable ground
J7	Window address enable
J8	High byte chip enable bit A11
J9	CSR high byte bit 8 chip enable output
J10	High byte chip enable bit A12

(continued on next page)

Table 10-14 ▪ MRV11-C Wirewrap Pin Identification (Cont.)

Pin Designation	Function
J11	CSR high byte bit 9 chip enable output
J12	High byte chip enable least significant bit
J13	CSR high byte bit 10 chip enable output
J14	High byte chip enable intermediate bit
J15	CSR high byte bit 11 chip enable output
J16	High byte chip enable most significant bit
J17	CSR high byte bit 12 chip enable output
J18	Boot address chip enable bit A11
J19	Boot address chip enable bit A12
J20	Boot address chip enable least significant bit
J21	Boot address chip enable intermediate bit
J22	Boot address chip enable most significant bit
J23	Boot address chip enable logic 1
J24	Boot address chip enable logic 0
J25	Direct address bit 11 chip enable output
J26	Low byte chip enable A11 bit
J27	CSR low byte bit 0 chip enable output
J28	Direct address bit 12 chip enable output
J29	Low byte chip enable A12 bit
J30	CSR low byte bit 1 chip enable output
J31	Direct address bit 13 chip enable output
J32	Low byte chip enable least significant bit
J33	CSR low byte bit 2 chip enable output
J34	Direct address bit 14 chip enable output
J35	Low byte chip enable intermediate bit
J36	CSR low byte bit 3 chip enable output
J37	Direct address bit 15 chip enable output
J38	Low byte chip enable most significant bit output

(continued on next page)

Table 10-14 ▪ MRV11-C Wirewrap Pin Identification (Cont.)

Pin Designation	Function
J39	CSR low byte bit 4 chip enable output
J40	Not used (Reserved for future Digital use)
J41	Window address bit 15 compare ground
J42	Window address bit 13 compare input
J43	Window address bit 12 compare ground
J44	Window address bit 14 compare input
J45	Window address bit 14 compare ground
J46	Window address bit 15 compare input
J47	Window address bit 16 compare ground
J48	Window address bit 16 compare input
J49	Window address bit 13 compare ground
J50	Window address bit 17 compare input
J51	Window address bit 17 compare ground
J52	Window address bit 12 compare input
J53	Direct address 32-Kbyte memory limit output
J54	Direct address 16-Kbyte memory limit output
J55	Direct address memory limit input
J56	Direct address 8-Kbyte memory limit output
J57	Direct address bit 17 compare ground
J58	Direct address bit 16 compare input
J59	Direct address bit 16 compare ground
J60	Direct address bit 17 compare input
J61	Direct address bit 15 compare ground
J62	Direct address bit 15 compare input
J63	Direct address bit 14 compare ground
J64	Direct address bit 14 compare input

(continued on next page)

Table 10-14 ▪ MRV11-C Wirewrap Pin Identification (Cont.)

Pin Designation	Function
J65	Direct address bit 13 compare ground
J66	Direct address bit 13 compare input
J67	CSR high byte bit 15 enable ground
J68	CSR high byte bit 15 enable input
J69	High byte chip enable window address function
J70	High byte chip enable direct address function
J71	High byte chip enable function select drivers
J72	Bit 7 chip select enable input
J73	Bit 7 chip enable decoder output
J74	Bit 6 chip select enable input
J75	Bit 6 chip enable decoder input
J76	Bit 5 chip select enable input
J77	Bit 5 chip enable decoder output
J78	Bit 4 chip select enable input
J79	Bit 4 chip enable decoder output
J80	Bit 3 chip select enable input
J81	Bit 3 chip enable decoder output
J82	Bit 2 chip select enable input
J83	Bit 2 chip enable decoder output
J84	Bit 1 chip select enable input
J85	Bit 1 chip enable decoder output
J86	Bit 0 chip select enable input
J87	Bit 0 chip enable decoder output
J88	Boot address enable ground
J89	Boot address enable
J90	DAL 4 CSR address select signal

(continued on next page)

Table 10-14 ▪ MRV11-C Wirewrap Pin Identification (Cont.)

Pin Designation	Function
J91	DAL 4 CSR address select ground
J92	DAL 1 CSR address select signal
J93	DAL 1 CSR address select ground
J94	DAL 2 CSR address select signal
J95	DAL 2 CSR address select ground
J96	DAL 3 CSR address select signal
J97	DAL 3 CSR address select ground
J98	Pin 18 input for chip set 5
J99	Chip wirewrap interconnection for chip set 5
J100	Pin 20 input for chip set 5 (Chip Enable 5)
J101	Pin 18 input for chip set 4
J102	Chip wirewrap interconnection for chip set 4
J103	Pin 20 input for chip set 4 (Chip Enable 4)
J104	Pin 18 input for chip set 6
J105	Chip wirewrap interconnection for chip set 6
J106	Pin 20 input for chip set 6 (Chip Enable 6)
J107	Pin 18 input for chip set 7
J108	Chip wirewrap interconnection for chip set 7
J109	Pin 20 input for chip set 7 (Chip Enable 7)
J110	Not used (Reserved for future Digital use)
J111	ROM interconnection, ground reference
J112	Chip enable bit bus input
J113	Address bit A11, used as chip input A10
J114	Chip interconnection loop (to wirewrap pins)
J115	Address bit A12, used as chip input A11
J116	Chip interconnection loop for chip pin 21

(continued on next page)

Table 10-14 • MRV11-C Wirewrap Pin Identification (Cont.)

Pin Designation	Function
J117	ROM interconnection for chip set 0
J118	Pin 18 input for chip set 0
J119	Chip wirewrap interconnection for chip set 0
J120	Pin 20 input for chip set 0 (Chip Enable 0)
J121	Pin 18 input for chip set 1
J122	Chip wirewrap interconnection for chip set 1
J123	Pin 20 input for chip set 1 (Chip Enable 1)
J124	Pin 18 input for chip set 2
J125	Chip wirewrap interconnection for chip set 2
J126	Pin 20 input for chip set 2 (Chip Enable 2)
J127	Pin 18 input for chip set 3
J128	Chip wirewrap interconnection for chip set 3
J129	Pin 20 input for chip set 3 (Chip Enable 3)

Chapter 11 ▪ MRV11-D Universal Programmable Read-Only Memory

The MRV11-D contains sixteen 28-pin sockets that accept static random-access memory (RAM) and a variety of user-supplied ROMs, such as fusible link PROMs, ultraviolet erasable (UV E) PROMs, and masked ROMs. It accepts several device densities up to and including 32K × 8 bits. With sixteen 32K × 8 devices, memory capacity is 512 Kbytes. The contents of the module can be accessed in one of two modes: direct mode addressing or page mode addressing.

▪ Specifications

Identification		M8578	
Size		Dual	
Power Requirements			
Voltage	**Tolerance**	**Current**	**Pins**
+5 Vdc	±0.25 V	1.6 A	AA2, BA2, BV1
Battery Backup Installed			
+5 VB	±0.25 V	280 mA	AV1
+5 Vdc	±0.25 V	1.3 A	AA2, BA2, BV1

Note

These values are measured for unpopulated modules. Add operating current for each device installed. Only one pair of devices operates at any given time; the rest are in standby mode.

Bus Loads	
ac	3.0
dc	0.5

Nonstandard Environmental Specifications	
Altitude	
Storage	Up to 9.1 km (5.65 mi)
Operating	Up to 2.4 km (1.5 mi)

Lower the maximum operating temperature by 1.8 Celsius degrees (3.24 Fahrenheit degrees) for each 1,000 m (3,280 ft) above sea level.

▪ Related Documentation

Document Title	Order Number
MRV11-D Universal PROM Module User's Guide	EK-MRV1D-UG
MRV11-D Field Maintenance Print Set	MP-01602-00

▪ Configuration

The MRV11-D contains 41 jumper pins, two switchpacks, and 16 memory chip sockets. Configuration is accomplished by setting a bank of PCR switches, setting a bank of starting address switches, and connecting a series of jumper pins. The required jumper pins are connected by means of jumper clips designated as W3 through W16 (see Figure 11-1). These jumper clips allow two adjacent jumper pins to be connected. Nonfunctional holder pins are provided in many jumper groups to avoid the loss of jumper clips when not used. The following features can be configured:

- Page/direct mode adddressing
- Location of PCR
- Bootstrap enable/disable
- Use of multiple MRV11-D modules
- Normal/high-performance timing
- Switch-selectable starting address
- Allow/inhibit DATO bus cycle
- Memory array size and response pattern
- System size (16-, 18-, or 22-bit addressing)
- Static RAM

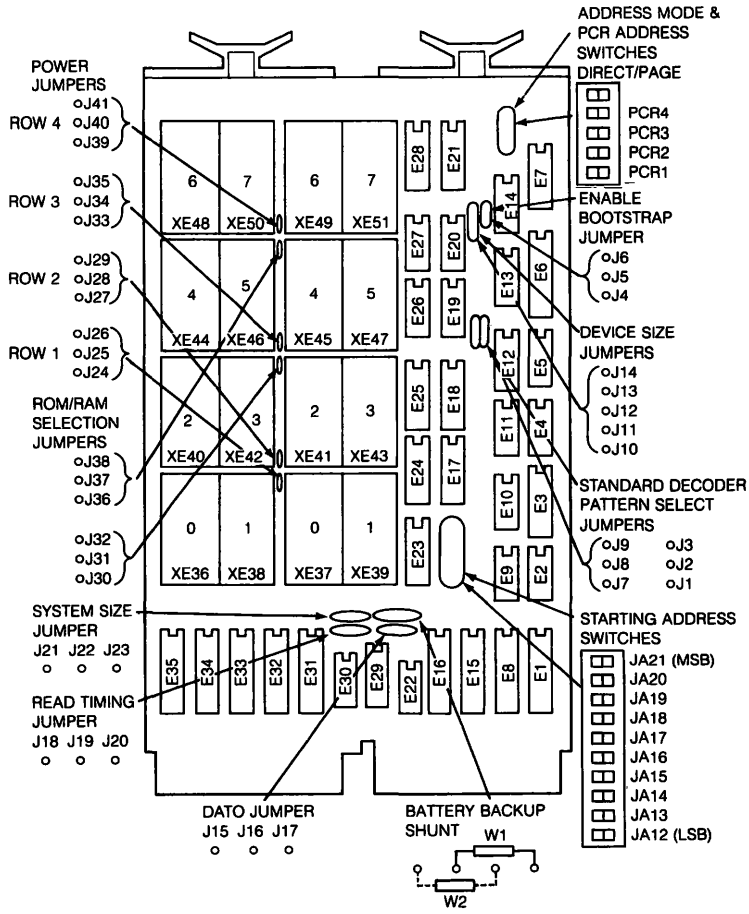


Figure 11-1 ▪ MRV11-D Jumper and Switch Locations

Memory Array

The size of the memory array is determined by the size of the memory devices installed. The MRV11-D is shipped with no memory devices installed, so the user must provide and install them.

Digital supplies a standard array decoder on the module that is a preprogrammed fusible link PROM. In the basic configuration with this array decoder installed, all memory chips must be the same size (2K × 8, 4K × 8, or 8K × 8). The pin configuration of the chips must conform to the Joint Electron Device Engineering Council (JEDEC) standard pinout for bytewide devices. Table 11-1 shows the four patterns available with the standard array decoder supplied by Digital.

Table 11-1 ▪ MRV11-D Standard Array Decoder Patterns

	Jumper Connection	
	W15	**W16**
2K × 8 half-populated	J1-J2	J7-J8
2K × 8 fully populated	J2-J3	J7-J8
4K × 8 fully populated	J1-J2	J8-J9
8K × 8 fully populated	J2-J3	J8-J9

Users can populate the module with many other combinations of devices by programming their own array decoder. There are certain mixtures that are restricted, however. See the *MRV11-D User's Guide* for details on programming the array decoder.

Users can also configure a system with more than one MRV11-D. Table 11-2 shows the storage capacity per module as a function of device size and number of device chips. The table lists the capacities for configurations with similar device sizes. It does not account for the configurations with mixed device sizes that can be used if the customers programs their own array decoders.

Table 11-3 lists typical UV PROMs and PROMs that can be installed on the MRV11-D. Other UV PROMs or PROMs that conform to the JEDEC pinout can also be used.

Table 11-2 ▪ Storage Capacity per ROM Chip Size and Number of Chips

Number of Chips	(Capacity Measured in Kbytes)				
Installed	**2K × 8**	**4K × 8**	**8K × 8**	**16K × 8**	**32K × 8**
2	4	8	16	32	64
4	8	16	32	64	128
6	12	24	48	96	192
8	16	32	64	128	256
10	20	40	80	160	320
12	24	48	96	192	384
14	28	56	112	224	448
16	32	64	128	256	512

Table 11-3 ▪ Typical EPROMs

UV PROMs	Chip Array Size	Maximum Memory Array Size (in Kbytes)
Intel 2716	2K×8	32
Intel 2732	4K×8	64
Intel 2764	8K×8	128
Intel 27128	16K×8	256
Masked ROMs		
Mostek MK3700	8K×8	128
NCR 23128	16K×8	256
NEC 23256	32K×8	512
National 52364	8K×8	128
Signetics 23128	16K×8	256
Synertek 2365	8K×8	128
Synertek 2365A	8K×8	128
Synertek 2316B	2K×8	32
Synertek 2333-3	4K×8	64

The MRV11-D contains sixteen 28-pin memory chip sockets to house the various PROMs and static RAM devices that can be used in the module. The sockets are divided into eight chip sets, chip set 0 through chip set 7. Each chip set is composed of a low byte and a high byte. This arrangement is shown in Figure 11-2.

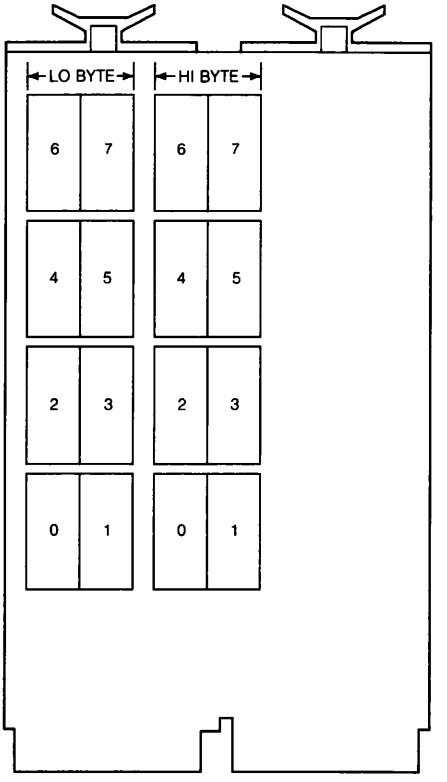


Figure 11-2 ▪ MRV11-D Chip Set Locations

The sockets can house 2K × 8, 4K × 8, 8K × 8, 16K × 8, and 32K × 8 PROMs. In addition, the bottom half of the socket array (chip sets 0 through 3) can accommodate static RAM. The 2K × 8 and 4K × 8 PROMs contain 24 pins while the others contain 28 pins.

Figure 11-3 shows the pin assignments for the 24- and 28-pin memories using the JEDEC standard pinout. The 2K × 8 PROM is represented by the 2716 and the 4K × 8 PROM is represented by the 2732. The other PROM types (8K × 8, 16K × 8, 32K × 8) are represented by the 2764, 27128, and 27256 respectively. The 8K × 8 static RAM is also shown. The basic differences on the 2764, 27128, 27256, and static RAM are in the functions of pins 26 and/or 27. Figure 11-3 shows these differences. For example, on the 16K × 8 PROM (27128), pin 26 is used as an address pin (A13). On the 32K × 8 PROM (27256), pins 26 and 27 are used as address pins (A13 and A14, respectively).

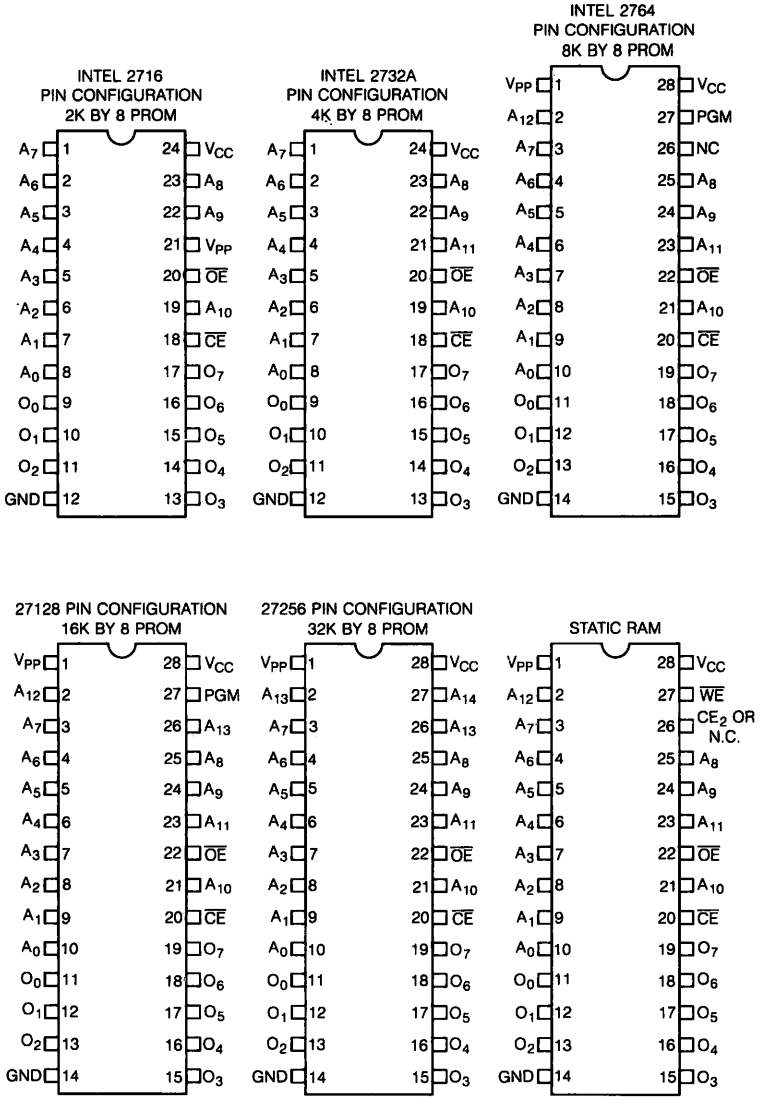


Figure 11-3 ▪ PROM Sizes and Types

eg. MOSTEK 48708

When installing a 24-pin PROM (2K × 8, 4K × 8) in a 28-pin socket, install it with the notch on top and bottom justified. Pin 1 of the PROM inserts into pin 3 of the socket (Figure 11-4). On 28-pin devices, pin 28 is the power pin. For 24-pin devices, pin 28 of the socket must be strapped to pin 26 of the socket to provide power to the device. The power jumpers strap these pins together, as shown in Table 11-4.

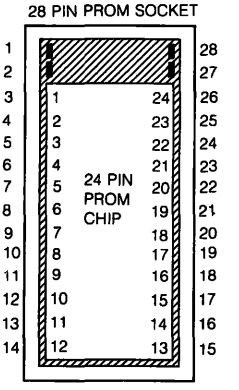


Figure 11-4 ▪ Insertion of 24-Pin PROM Chips

Table 11-4 ▪ MRV11-D Power Jumper Connections

Device Size	Row 4 W12	Row 3 W11	Row 2 W10	Row 1 W9
2K × 8 ROM	J41-J40	J35-J34	J29-J28	J26-J25
4K × 8 ROM	J41-J40	J35-J34	J29-J28	J26-J25
8K × 8 ROM*	n/a	n/a	n/a	n/a
8K × 8 Static RAM	J41-J40	J35-J34	J29-J28	J26-J25
16K × 8	J40-J39	J34-J33	J28-J27	J25-J24
32K × 8	J40-J39	J34-J33	J28-J27	J25-J24

Configuration is done on a row-by-row basis.

*The power jumper can be in either position for 8K × 8 ROMs.

To install static RAM devices in the bottom half of the memory array (chip sets 0 to 3), the user must configure the ROM/RAM selection jumpers as shown in Table 11-5.

The user must also configure the module for the size of the memory devices installed. Table 11-6 shows the possible jumper configurations when using the Digital-supplied array decoder. A new array decoder is required in the following circumstances:

- Both 32K × 8 and 16K × 8 devices are installed.
- The number of devices installed is other than the number expected by the standard decoder.
- A mix of 4K × 8, 8K × 8, or 16K × 8 devices is installed.

The power jumpers must be properly configured for each row, and rows containing 32K × 8 devices must be jumpered for address rather than for power.

Table 11-5 ▪ MRV11-D ROM/RAM Selection Jumpers

Memory Type	Jumper Connection W5	W4
All ROM	J38-J37	J32-J31
ROM/RAM*	J37-J36	J31-J30

*RAM installed in chip sets 0 through 3

Table 11-6 ▪ MRV11-D Device Size Jumpers

Size Chosen	Jumper Connection Rev C Etch* W8	W7	Jumper Connection Rev D Etch* W8	W7
2K×8 only	†	J11-J10	J13-J12	J11-J10
4K×8	J14-J13	J11-J10	J14-J13	J12-J11
8K×8	J14-J13	J11-J10	J14-J13	J12-J11
16K×8	J14-J13	J11-J10	J14-J13	J12-J11
32K×8	J14-J13	J12-J11	J14-J13	J11-J10

*The board etch revision is located on the component side of the module along the left side: Rev C Etch = 5015213C Rev D Etch = 5015213D

†When using 24-pin devices such as the 2716 (2K×8 PROM) on a revision C etch board, the user must wirewrap J13 (V_{pp}) to J40 (pin 26 of row 4). It is also necessary to jumper J40 to J41 (+5 V). The jumper clip cannot be used, however, because a wirewrap exists on J40. Therefore, the user must wirewrap rather than jumper J40 to J41. This procedure ensures proper read mode operation. On a revision D etch board, 2K×8 PROMs can be installed without wirewrap.

Addressing Modes

The MRV11-D can be configured to operate in one of two addressing modes—page mode and direct mode. Direct mode addressing provides immediate access to all memory locations on the module. Page mode addressing, or window mapping, provides two 2-Kbyte windows in bus address space that each map a 2-Kbyte page of the memory array. The page that is viewed or accessed through each window (2 Kbytes per window) can be varied under program control through a page control register (PCR). The PCR must be written with the desired page number before the access.

The addressing mode is selected by setting switch 1 of the PCR switch bank and is not variable under program control. With the module oriented so the handles are on top, push the right side of the rocker switch down (switch on) to select direct mode addressing. Push the left side of the rocker switch down (switch off) to select page mode addressing.

- DIRECT ADDRESS MODE

  In direct address mode, each memory location on the MRV11-D has a corresponding location on the system bus. The number of system bus address locations allocated to the module is equal to the module's configured capacity. For example, an MRV11-D that is fully populated (16 devices) with 4K × 8 PROMs (64 Kbytes) corresponds to 64 Kbytes of the system bus. The starting address of the module and the array decoder pattern determine the boundaries of the module's address range.

  The starting address of the MRV11-D can be placed on any 4-Kbyte boundary from address 0_8 to 17770000_8. This is accomplished by setting the rocker switches in the starting address switch bank. The ten switches correspond to the ten most significant bits of the starting address — address bits <12:21>. With the module oriented so the handles are on top, pushing the right side of the rocker switch down produces a logical 1 (switch on). Pushing the left side of the switch down produces a logical 0 (switch off).

  Note that the module's main memory does not respond to any I/O page accesses, even if the address range overlaps the I/O page. Only the bootstrap areas and the bootstrap PCR, if enabled, respond in the I/O page under direct mode addressing.

- PAGE MODE ADDRESSING

  Page mode addressing is a virtual addressing scheme that extends the addressing capability of the system bus. A 4-Kbyte segment of the system bus and an I/O register called the page control register (PCR) are assigned to the MRV11-D. The MRV11-D's starting address determines the beginning of the module's portion of the system bus. The user configures the PCR address to 1 of 16 locations in the I/O section of the system bus, as shown in Table 11-7.

Table 11-7 ▪ MRV11-D Switch Settings for PCR Address Selection

PCR Address	PCR4	PCR3	PCR2	PCR1
17770000	ON	ON	ON	ON
17770002	ON	ON	ON	OFF
17770004	ON	ON	OFF	ON
17770006	ON	ON	OFF	OFF
17770010	ON	OFF	ON	ON
17770012	ON	OFF	ON	OFF
17770014	ON	OFF	OFF	ON
17770016	ON	OFF	OFF	OFF
17770020	OFF	ON	ON	ON
17770022	OFF	ON	ON	OFF
17770024	OFF	ON	OFF	ON
17770026	OFF	ON	OFF	OFF
17770030	OFF	OFF	ON	ON
17770032	OFF	OFF	ON	OFF
17770034	OFF	OFF	OFF	ON
17770036	OFF	OFF	OFF	OFF

ON = logical 0; OFF = logical 1

Note

With the module oriented so that the handles are on top, pushing down the right side of the rocker switch produces a logical 0 (switch on). Pushing down the left side produces a logical 1 (switch off).

The MRV11-D's portion of the system bus is further divided into two sections called windows. Each window is 2 Kbytes long and can contain any 2-Kbyte page of data on the module. The two pages of data that are currently available to the system have their page numbers stored, one in each byte of the PCR. To move a different page into the window, simply change the contents of the corresponding PCR byte to the number of the desired page.

Bits 7 and 15 are not part of the page numbers. Bit 7 is unused and bit 15 is the window control bit. When bit 15 is asserted (1), the windows are open and the pages in the windows can be accessed. When bit 15 is not asserted (0), the windows are closed and attempted accesses through the windows produce a bus timeout.

Upon powerup and restart, the PCR bits are cleared to 0. Both windows contain the data from page 0, but they are closed because bit 15 of the PCR is also 0. Bit 15 must be set to open the windows.

Bootstrap

The MRV11-D bootstrap operation is similar to page mode addressing. It is independent of the address mode chosen for the module, however. The bootstrap windows are split. Window 0 begins at location 17773000 and runs through 17773776. Window 1 begins at 17765000 and runs through 17765776. The bootstrap PCR is located at 17777520. There are, however, the following important differences between page mode addressing and the bootstrap feature:

- The bootstrap windows and pages are 512 bytes long. In page mode, the windows and pages are 2 Kbytes long.
- Bit 15 of the bootstrap PCR is not a control bit. The windows are always open. In page mode, the windows are open only when bit 15 is asserted (1).
- The bootstrap PCR address is fixed at 17777520. The page mode PCR address is configured by the user between 17777000 and 17777036.

The bootstrap memory device must be physically installed in chip set 7.

The bootstrap program size is limited by the size of the memory devices installed. A pair of 8K × 8 devices can contain a 16-Kbyte bootstrap progam. Note, however, that like page mode addressing, only two 512-byte pages are available to the system at a time. The program must be specifically written to turn its own pages. The MXV11-B2 bootstrap PROM set is written this way and will function if installed and properly configured on an MRV11-D.

If the bootstrap program is smaller than 512 bytes, it can be written on one page, avoiding the need to change pages. In this case, the program should be in the first 512 bytes of the bootstrap device. Because the bootstrap PCR clears on powerup and restart, both windows contain page 0 of the bootstrap device.

The bootstrap feature is enabled by installing jumper clip W14 between pins J5 and J6. Installing W14 between pins J5 and J4 disables the feature.

Battery Backup Shunt

When static RAM is installed in the bottom half of the memory array, the user can configure the MRV11-D module so that the memory and refresh logic are disconnected from the normal bus power and are, instead, connected to a separate battery backup system. This is accomplished by removing the factory-installed 0-ohm shunt (W1) from the second and fourth holes in the printed circuit board and installing another 0-ohm shunt (W2) between the first and third holes.

System Size Jumpers

To configure the MRV11-D for use in a 16- or 18-bit Q-bus system, jumper W3 is installed between posts J21 and J22. To configure the module for use in a 22-bit Q-bus system, W3 is installed between J23 to J22.

DATO Bus Cycle

Ordinarily, when the MRV11-D is accessed by a DATO bus cycle, it does not respond, generating a bus timeout. However, when static RAM is installed in the bottom half of the memory array, the MRV11-D can be configured to respond to DATO cycles. This is accomplished by removing the factory-installed jumper (W6) from pins J15 and J16 and installing it between pins J16 and J17.

Note that the page mode PCR and the bootstrap PCR will not timeout in either configuration when accessed by a DATO cycle.

Read Timing

The MRV11-D can normally interface with chips that have a read access time greater than 450 ns. To obtain some speed advantage, the module can be configured for a read access time of 200 ns. This is accomplished by removing the factory-installed jumper (W13) from between pins J18 and J19 and installing it between pins J19 and J20. Note, however, that the slowest device installed on the board must then meet this 200 ns access time requirement.

Installing the MXV11-B2 ROM

To install the MXV11-B2 PROM set on the MRV11-D, the user must perform the following steps:

- Enable the bootstrap function.
- Set the row 4 power jumper for an 8K × 8 device.
- Set the device size jumper to 8K × 8.
- Install the read timing jumper W13 between J18 and J19.

Install the MXV11-B2 ROM chips in chip set 7. Insert the low-byte ROM (P/N 23-145E4-00) into the low byte 7 socket (XE50). Insert the high-byte ROM (P/N 23-146E4-00) into the high byte 7 socket (XE51). Position the ROMs so that pin 1 is in the upper left corner of the socket.

Note

MXV11-B2 bootstrap ROMs cannot be used if the device size jumper is set for 2K × 8 or if the power jumper connection for row 4 is set for 16K × 8 or 32K × 8 devices.

For additional information on the MXV11-B2 ROM, see Chapter 18 or refer to the *MXV11-B2 ROM Set User Guide* (EK-MXVB2-UG).

Chapter 12 ▪ MSV11-D,-E Dynamic MOS Read/Write Memory

All MSV11-D and MSV11-E memory modules can be used in either 16- or 18-bit systems. There are eight versions of this module, listed below. Memory storage is provided by either 4K × 1-bit or 16K × 1-bit integrated circuits, depending on model.

Model	Memory Capacity	Module	Parity Bits
MSV11-DA	4K × 16 bits	M8044-A	No
MSV11-DB	8K × 16 bits	M8044-B	No
MSV11-DC	16K × 16 bits	M8044-C	No
MSV11-DD	32K × 16 bits	M8044-D	No
MSV11-EA	4K × 18 bits	M8045-A	Yes
MSV11-EB	8K × 18 bits	M8045-B	Yes
MSV11-EC	16K × 18 bits	M8045-C	Yes
MSV11-ED	32K × 18 bits	M8045-D	Yes

▪ Specifications

Identification				
MSV11-DA,-DB,-DC,-DD	M8044-A,-B,-C,-D			
MSV11-EA,-EB,-EC,-ED	M8045-A,-B,-C,-D			
Size	Dual			
Power Requirements				
Supply Voltage	**–DA/–DC**	**–DB/–DD**	**–EA/–EC**	**–EB/–ED**
+5 V system power:				
Typical operating power	1.7 A	1.7 A	2.0 A	2.0 A
Typical standby power	1.7 A	1.7 A	2.0 A	2.0 A
+5 V battery backup:				
Typical operating power	0.7 A	0.7 A	1.0 A	1.0 A
Typical standby power	0.7 A	0.7 A	1.0 A	1.0 A
+12 V system power or battery backup:				
Typical operating power	0.34 A	0.37 A	0.38 A	0.41 A
Typical standby power	0.06 A	0.08 A	0.06 A	0.09 A

Bus Loads

ac	2.0
dc	1.0

Performance

Access and Cycle Time

Bus Cycle	Access Time (ns) (1) Typical	Maximum	Notes	Cycle Time (ns) (1) Typical	Maximum	Notes
MSV11-D:						
DATI	210	225	(2)	500	520	(4)
DATO(B)	100	110	(2)	545	565	(5)
DATIO(B)	630	650	(3)	1075	1100	(6)
MSV11-E:						
DATI	250	265	(2)	500	520	(4)
DATO(B)	100	110	(2)	545	565	(5)
DATIO(B)	670	690	(3)	1115	1140	(6)

All Models:

Refresh cycle time = 575 ns typical, 600 ns maximum (7)

Notes

1. All operating speeds are in nanoseconds and are based on memory not busy and no refresh arbitration. Refresh arbitration adds 100 ns typical (120 ns maximum) to access and cycle times. Refresh conflicts add 575 ns typical (600 ns maximum) to access and cycle times.
2. Access times are defined as internal SYNC to REPLY with minimum times (25 or 50 ns) from SYNC to DIN or DOUT. The DATO(B) access and cycle times assume a minimum 50 ns from SYNC to DOUT at bus receiver outputs. For actual Q-bus measurements, 150 ns should be added to DATO(B) times; that is, access time (typical) = 100 + 150 = 250 ns.
3. Access times are defined as internal SYNC to RPLY [DATO(B)] with minimum time (25 ns) from SYNC to DIN, and minimum time (350 ns) from RPLY (DATI) asserted to DOUT asserted.
4. Cycle times are defined as internal SYNC to LOCKOUT negated.
5. Cycle times are defined as internal SYNC to LOCKOUT negated with minimum time (50 ns) from SYNC to DOUT.
6. Cycle times are defined as internal SYNC to LOCKOUT [DATO(B)] with minimum times (25 ns) from SYNC to DIN and minimum time (350 ns) from RPLY (DATI) asserted to DOUT asserted.
7. Refresh cycle time is defined as internal REF REQ to LOCKOUT negated.

▪ Related Documentation

Document Title	Order Number
MSV11-D,-E User's Manual	EK-MSVI1-OP
MSV11-D Field Maintenance Print Set	MP-00566-00
MSV11-E Field Maintenance Print Set	MP-00567-00

▪ Configuration

The user can configure the MSV11-D or MSV11-E to alter its operation for a specific system application. The following items can be configured:

- Memory starting address
- Battery backup power
- Enable/disable 2-Kword portion of bank 7

Note

Each MSV11-D or -E module contains two factory- installed wirewrap jumpers that select memory size (4, 8, 16, or 32 Kwords); these jumper configurations normally should not be changed.

Address Selection

The MSV11-D or MSV11-E address can start at any 4-Kword boundary. The address configured is the starting address for the contiguous portion of memory contained on the module. Set the switches, located as shown in Figure 12-1, to the desired starting address as listed in Table 12-1. The upper 4-Kword address space is normally reserved for peripheral device register addresses.

Factory-configured modules will not respond to bank 7 addresses. In special applications that permit the use of the lower 2-Kword portion of bank 7 for system memory, enable the lower 2-Kword portion of bank 7 by removing the jumper from the wirewrap pins 1 and 3 and connecting a new jumper from 1 to 2.

Battery Backup Power

The MSV11-D and MSV11-E modules are factory-configured with the power jumpers installed for normal system power. In this configuration, the memory and refresh logic are powered from the normal bus backplane power. The modules are designed so that the dc power required to support them during a backup period is minimized. The jumpers are provided to allow the user to disconnect the memory and refresh logic from the normal bus power and connect it to a separate battery source. The user can configure the jumpers, shown in Figure 12-1, for battery backup operation as follows:

W2, W3	Remove to separate the module from the bus-powered backplane.
W4, W5	Insert to connect the battery power to the memory and refresh logic.

To use the MSV11-D or MSV11-E modules in a battery backup system, the battery or source must be capable of supplying the following:

	MSV11-D (1 module)	MSV11-E (1 module)
+5 Vdc ±3%	0.7 A	1.0 A
+12 Vdc ±3%	0.37 A	0.41 A max

These voltages must remain within ±3 percent of the bus voltage at all times and not vary more than ±3 percent during the transition to or from the battery.

One MSV11-E module draws approximately 7 W when operating in the battery backup mode. A typical backup system that is 30 percent efficient with a 2.5 ampere-hour battery will support each module for approximately two hours. When used in a PDP-11/03 system, or equivalent, no additional cooling of the module is required during the backup period, if the room temperature is maintained to less than 32°C (90°F).

Parity

One jumper is factory-installed for nonparity (MSV11-D) or parity (MSV11-E) operation, depending on the model. Do not reconfigure this jumper. Standard jumper configurations are listed below for reference purposes.

All MSV11-D models: Jumper installed from pin 7 to pin 5.

All MSV11-E models: Jumper installed from pin 6 to pin 5.

Memory Size

Two jumpers are factory-installed to configure addressing logic for memory size (number and type of memory integrated circuits). Do not reconfigure these jumpers. Standard jumper configurations are listed below for reference purposes.

	Jumpers (Two Installed)	
Model	**Memory Range Pins**	**Memory Select Pins**
MSV11-DA, -EA	From 17 to 15	From 17 to 14
MSV11-DB, -EB	From 17 to 15	From 12 to 14
MSV11-DC, -EC	From 16 to 15	From 16 to 14
MSV11-DD, -ED	From 16 to 15	From 10 to 14

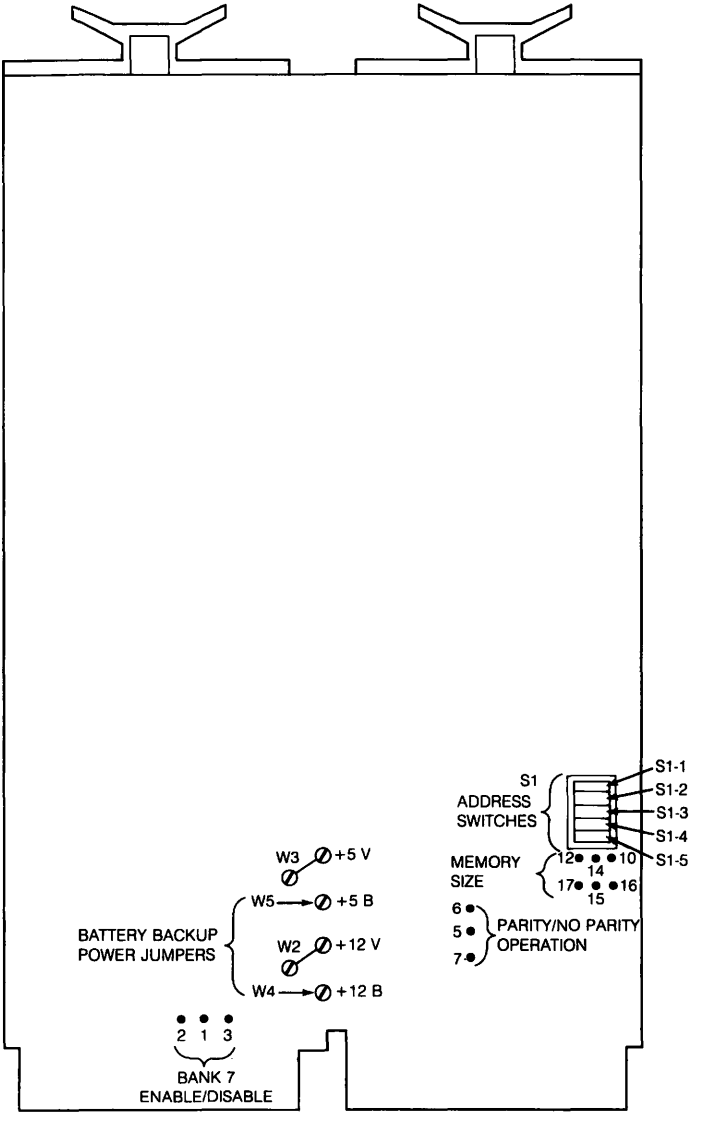


Figure 12-1 ▪ MSV11-D, MSV11-E Switch and Jumper Locations

Table 12-1 ▪ MSV11-D, MSV11-E Addressing Summary

	Switch Settings					Memory Bank(s) Selected			
Address	S1-1	S1-2	S1-3	S1-4	S1-5	-DA,-EA	-DB,-EB	-DC,-ED	-DD,-ED
0	ON	ON	ON	ON	ON	0	0-1	0-3	0-7
20000	ON	ON	ON	ON	OFF	1	1-2	1-4	1-10
40000	ON	ON	ON	OFF	ON	2	2-3	2-5	2-11
60000	ON	ON	ON	OFF	OFF	3	3-4	3-6	3-12
100000	ON	ON	OFF	ON	ON	4	4-5	4-7	4-13
120000	ON	ON	OFF	ON	OFF	5	5-6	5-10	5-14
140000	ON	ON	OFF	OFF	ON	6	6-7	6-11	6-15
160000	ON	ON	OFF	OFF	OFF	7	7-10	7-12	7-16
200000	ON	OFF	ON	ON	ON	10	10-11	10-13	10-17
220000	ON	OFF	ON	ON	OFF	11	11-12	11-14	11-20
240000	ON	OFF	ON	OFF	ON	12	12-13	12-15	12-21
260000	ON	OFF	ON	OFF	OFF	13	13-14	13-16	13-22
300000	ON	OFF	OFF	ON	ON	14	14-15	14-17	14-23
320000	ON	OFF	OFF	ON	OFF	15	15-16	15-20	15-24
340000	ON	OFF	OFF	OFF	ON	16	16-17	16-21	16-25
360000	ON	OFF	OFF	OFF	OFF	17	17-20	17-22	17-26
400000	OFF	ON	ON	ON	ON	20	20-21	20-23	20-27
420000	OFF	ON	ON	ON	OFF	21	21-22	21-24	21-30
440000	OFF	ON	ON	OFF	ON	22	22-23	22-25	22-31
460000	OFF	ON	ON	OFF	OFF	23	23-24	23-26	23-32
500000	OFF	ON	OFF	ON	ON	24	24-25	24-27	24-33
520000	OFF	ON	OFF	ON	OFF	25	25-26	25-30	25-34
540000	OFF	ON	OFF	OFF	ON	26	26-27	26-31	26-35
560000	OFF	ON	OFF	OFF	OFF	27	27-30	27-32	27-36
600000	OFF	OFF	ON	ON	ON	30	30-31	30-33	30-37
620000	OFF	OFF	ON	ON	OFF	31	31-32	31-34	X
640000	OFF	OFF	ON	OFF	ON	32	32-33	32-35	X
660000	OFF	OFF	ON	OFF	OFF	33	33-34	33-36	X
700000	OFF	OFF	OFF	ON	ON	34	34-35	34-37	X
720000	OFF	OFF	OFF	ON	OFF	35	35-36	X	X
740000	OFF	OFF	OFF	OFF	ON	36	36-37	X	X
760000	OFF	OFF	OFF	OFF	OFF	37	X	X	X

X = do not use

Notes

1. Bank 7 cannot be selected as factory-configured; however, the user can enable the lower 2-Kword portion of bank 7 for use.
2. Rocker switch positions are defined by pressing the desired side of the rocker, not by the red line on the opposite side of the rocker.

Chapter 13 ▪ MSV11-L MOS Random-Access Memory

Designed to be used with the Q-bus, MSV11-L dual-height memory modules provide storage for 18-bit words (16 bits of data and 2 parity bits), contain parity control circuitry, and a control and status register (CSR). There are presently two members of the MSV11-L memory module family as shown below.

▪ Specifications

Identification	M8059	
Size	Dual	
Bus Loads		
ac	2.0	
dc	0.5	
Power Requirements		
Supply Voltage	**MSV11-LF**	**MSV11-LK**
+5 V ±5% system power:		
Typical operating power	2.8 A	3.0 A
Typical standby power	1.40 A	1.50 A
+5 V battery backup:		
Typical operating power	1.35 A	1.40 A
Typical standby power	0.9 A	1.0 A

Access and Cycle Times

	Access Time (ns)			Cycle Time (ns)		
Bus Cycle	**Typical**	**Maximum**	**Notes**	**Typical**	**Maximum**	**Notes**
DATI	210	230	2	560	590	4
DATO(B)	90	120	2	605	635	5
DATIO(B)	640	670	3	1140	1170	6
Refresh	-	-	-	650	685	7

Parity–CSR configurations, refer to notes 1, 8, and 9.

Notes

1. Assuming memory not busy and no arbitration.
2. SYNC to RPLY with minimum times (25/50 ns) from SYNC to (DIN/DOUT). The DATO(B) access and cycle times assume a minimum 50 ns from SYNC to DOUT inside memory receivers. For actual Q-bus measurements, a constant (K - 50 ns, where K = 200) should be added to DATO(B) times. That is, access time (typical) = 90 + (200–50) = 240 ns.
3. SYNC to RPLY (DATO(B)) with minimum time (25 ns) from SYNC to DIN and minimum (350 ns) from RPLY (DATI) asserted to DOUT asserted.
4. SYNC to DL220 negated.
5. SYNC to DL220 negated with minimum time (50 ns) from SYNC to DOUT.
6. SYNC to DL220 (DATO(B)) with minimum times (25 ns) from SYNC to DIN and minimum (350 ns) from RPLY (DATI) asserted to DOUT asserted.
7. REF REQ to DL220 negated.
8. Refresh arbitration adds 100 ns (typical) and 120 ns (maximum) to access and cycle times.
9. Refresh conflict adds 650 ns (typical) and 685 ns (maximum) to access and cycle times.

▪ Related Documentation

Document Title	Order Number
MSV11-L User's Guide	EK-MSV0L-UG
MSV11-L Memory Module Configuration Guide	EK-MSV1L-CG
MSV11-L Field Maintenance Print Set	MP-01238-00
MSV11 Diagnostic Documentation Kit	ZJ246-RZ

▪ Configuration

The MSV11-L module is configured by means of jumper wires, shown in Figure 13-1 and listed in Tables 13-1 through 13-5. The user can configure the following features:

- Module starting address (MSA)
- Control status register (CSR) address
- Battery backup

Note

The jumpers listed in Table 13-1 should not be changed and are listed only for reference.

Module Starting Address (MSA)

The MSA is equal to the number of decimal Kwords already configured in the system. Jumpers L, M, N, P, and R select the first address in the 128-Kword block of addresses that contains the module's MSA. Jumpers A, B, C, D, E, and F select the particular 2-Kword increment in that 128-Kword block where the MSA begins. The 128-Kword block selected is called the FAR (First Address Range). The 2-Kword increment is called the PSA (Partial Starting Address). The following equation shows how the MSA, FAR, and PSA are related.

PSA = MSA-FAR.

Refer to Table 13-2 and Table 13-3 for jumper locations for the FAR and PSA respectively.

Taking an MSA of 188-Kwords as an example, find the FAR on Table 13-2 by locating the first address in the block with the 188th location. This is 128, the FAR value. To find the PSA, subtract 128 from 188. This yields a PSA of 60. Jumper the FAR of 128 by connecting pin L to pin K (ground). Jumper the PSA of 60 by connecting pin V to pin W to pin X to pin Y to pin U (ground).

CSR Address Selection

Eight addresses are reserved for the CSR registers. Every MSV11-L module has one CSR. By convention, the memory module with the lowest starting address should be jumpered for the lowest CSR address. The remaining modules should be jumpered in sequence.

To select a CSR address for a module, install jumpers according to Table 13-4. Wirewrap the appropriate pins in daisychain fashion to pin E which is grounded.

Battery Backup

To select either battery backup or no battery backup, jumper the module as shown in Table 13-5.

Note

Digital does not support battery backup for the MSV11-L.

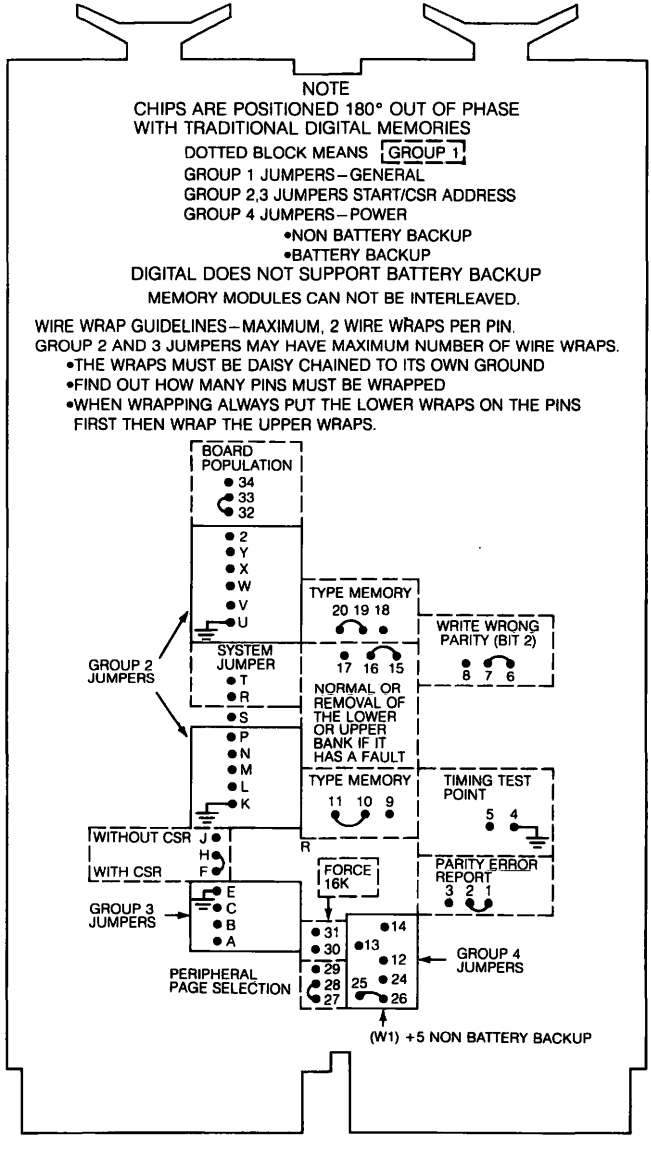


Figure 13-1 ▪ MSV11-L Memory Module Jumpers

Table 13-1 ▪ MSV11-L Jumpers and Functions (Group 1)

Function	Jumper	Normal Status
Type of Memory		
Nonparity	9 to 10	OUT
With parity	11 to 10	IN
Parity nonCSR	18 to 19	OUT
Parity with CSR	20 to 19	IN
Parity Error Report		
Reported BDAL 16 nonCSR	3 to 2	OUT
Reported BDAL 16 and BADL 17 with CSR	1 to 2	IN
Write Wrong Parity		
Diagnostic bit for tester use:		
Disable	8 to 7	OUT
Enable	6 to 7	IN
CSR Selection		
NonCSR	J to H	OUT
With CSR	F to H	IN
Peripheral Page Selection		
2-Kword peripheral page	29 to 28	OUT
4-Kword peripheral page	27 to 28	IN
Full or One-Half Memory Selection		
Half-memory selection	32 to 33	OUT
Full-memory selection	34 to 33	IN
Removal of Lower or Upper Bank (with a Fault)		
Lower bank has failed	17 to 16	OUT
Normal operation or upper bank has failed	15 to 16	IN
Extended or Normal Memory Selection		
Normal operation (128-Kword system)	R to T	OUT
Extended operation (2-Mword system)	R to T	IN

Table 13-2 ▪ MSV11-L Starting Address Jumpers (Group 2)

Starting Address Range (FAR)		Jumpers in (X) to Ground (K)				
		DAL	21	20	19	18
Decimal(K)	Octal	Pins	P	N	M	L
000-124	00000000-00760000					
128-252	01000000-01760000				X	
256-380	02000000-02760000			X		
384-508	03000000-03760000			X	X	
512-636	04000000-04760000		X			
640-764	05000000-05760000		X		X	
768-892	06000000-06760000		X	X		
896-1020	07000000-07760000		X	X	X	
1024-1148	10000000-10760000	X				
1152-1276	11000000-11760000	X			X	
1280-1404	12000000-12760000	X		X		
1408-1532	13000000-13760000	X		X	X	
1536-1660	14000000-14760000	X	X			
1664-1788	15000000-15760000	X	X		X	
1792-1916	16000000-16760000	X	X	X		
1920-2044	17000000-17760000	X	X	X	X	

Table 13-3 ▪ MSV11-L Partial Starting Address Jumpers (Group 2)

Partial Starting Address (PSA)		Jumpers in (X) to Ground (U)					
		DAL	17	16	15	14	13
Decimal(K)	Octal	Pins	Z	Y	X	W	V
0	00000000						
4	00020000					X	
8	00040000				X		
12	00060000				X	X	
16	00100000			X			
20	00120000			X		X	

(continued on next page)

Table 13-3 ▪ MSV11-L Partial Starting Address Jumpers (Group 2) (Cont.)

Partial Starting Address (PSA)		Jumpers in (X) to Ground (U)					
		DAL	17	16	15	14	13
Decimal(K)	Octal	Pins	Z	Y	X	W	V
24	00140000			X	X		
28	00160000			X	X	X	
32	00200000		X				
36	00220000		X			X	
40	00240000		X		X		
44	00260000		X		X	X	
48	00300000		X	X			
52	00320000		X	X		X	
56	00340000		X	X	X		
60	00360000		X	X	X	X	
64	00400000	X					
68	00420000	X				X	
72	00440000	X			X		
76	00460000	X			X	X	
80	00500000	X		X			
84	00520000	X		X		X	
88	00540000	X		X	X		
92	00560000	X		X	X	X	
96	00600000	X	X				
100	00620000	X	X			X	
104	00640000	X	X		X		
108	00660000	X	X		X	X	
112	00700000	X	X	X			
116	00720000	X	X	X		X	
120	00740000	X	X	X	X		
124	00760000	X	X	X	X	X	

Table 13-4 ▪ MSV11-L CSR Address Jumpers (Group 3)

22-Bit CSR Address	18-Bit CSR Address	Jumpers in (X) to Ground (E) C	B	A
17772100	772100			
17772102	772102			X
17772104	772104		X	
17772106	772106		X	X
17772110	772110	X		
17772112	772112	X		X
17772114	772114	X	X	
17772116	772116	X	X	X

Table 13-5 ▪ MSV11-L Power Jumpers (Group 4)

Voltage Connection	Jumper Configuration
+5 V Nonbattery backup	26 to 25 (W1)
+5 V Battery backup	25 to 25 (W2) 14 to 13 (W3)* or 12 to 13 (W4)*

* Availability for the +5 V battery backup

Chapter 14 • MSV11-P MOS Random-Access Memory

There are two MSV11-P memory modules—the MSV11-PL and the MSV11-PK. Because its capacity exceeds the capabilities of an 18-bit Q-bus system, the MSV11-PL can be used only in a 22-bit Q-bus system. The MSV11-PK can be used in either type of system, as long as it is the only memory being used. The two MSV11-P memory modules are listed below.

Model	Identification	MOS Chips	Capacity
MSV11-PK	M8067-KA	128K × 18 bits	256 Kbytes
MSV11-PL	M8067-LA	256K × 18 bits	512 Kbytes

• Specifications

Identification	M8067	
Size	Quad	
Bus Loads		
ac	2.0	
dc	1.0	
Power Requirements		
Supply Voltage	**MSV11-PK**	**MSV11-PL**
+5 V ±5% total system power:		
Typical operating power	3.45 A	3.60 A
Typical standby power	3.00 A	3.10 A
+5 V Battery backup:		
Typical operating power	1.75 A	1.85 A
Typical standby power	1.35 A	1.45 A

Note

These current values represent measured typical values, not maximum values.

Voltages are partitioned; however, battery backup is not supported.

Access and Cycle Times

Bus Cycles	Access Times (ns) + Typical	Maximum	Notes	Cycle Times (ns) + Typical	Maximum	Notes
DATI	240	260	2	560	590	4
DATO(B)	90	120	2	610	640	5
DATIO(B)	660	690	3	1175	1210	6
Refresh	–	–	–	640	690	7

Parity – CSR configurations, refer to notes 1, 8, and 9.

Notes

1. Assuming memory not busy and no arbitration.
2. SYNC to RPLY with minimum times (25/50 ns) from SYNC to (DIN/DOUT). The DATO(B) access and cycle times assume a minimum 50 ns from SYNC to DOUT inside memory receivers. For actual Q-bus measurements, a constant (K - 50 ns, where K = 200) should be added to DATO(B) times. That is, access time (typical) = 90 + (200–50) = 240 ns.
3. SYNC to RPLY (DATO(B)) with minimum time (25 ns) from SYNC to DIN and minimum (350 ns) from RPLY (DATI) asserted to DOUT asserted.
4. SYNC to TIM250 negated.
5. SYNC to TIM250 negated with minimum time (50 ns) from SYNC to DOUT.
6. SYNC to TIM250 (DATO(B)) with minimum times (25 ns) from SYNC to DIN and minimum (350 ns) from RPLY (DATI) asserted to DOUT asserted.
7. REF REQ to TIM250 negated.
8. Refresh arbitration adds 90 ns (typical) and 110 ns (maximum) to access.
9. Refresh conflict adds 640 ns (typical) and 690 ns (maximum) to access and cycle times.

▪ Related Documentation

Document Title	Order Number
MSV11-P User's Guide	EK-MSV0P-UG
MSV11-P Field Maintenance Print Set	MP-01239-00
MSV11 Diagnostic Documentation Kit	ZJ246-RZ

▪ Configuration

The jumpers on the MSV11-P memory module (shown in Figure 14-1) are divided into five functional groups:

- Starting address jumpers
- CSR address jumpers
- Power jumpers
- Bus grant continuity jumpers
- Miscellaneous jumpers

Module Starting Address (MSA)

Each MSV11-P memory module installed in a system is jumpered for its own starting address by the use of wirewrapped pins. The memory module starting address is equal to the amount of memory already configured in the system, expressed as Kwords.

Module starting address jumpers consist of two groups. The First Address of the Range (FAR) selects the first 256-Kword range address in which the starting address falls. (See Table 14-1, Part 1). The Partial Starting Address (PSA) selects the 8-Kword boundary within a specific multiple of 256 Kwords in which the starting address falls. (See Table 14-1, Part 2).

After you have determined your module starting address (MSA), you should determine the FAR and PSA values.

1. Find the FAR value. This is done by referring to Table 14-1, Part 1, and locating the address range of the MSA. The FAR value is the first address of the selected address range. Associated with the FAR value is a specific configuration of jumper pins X, W, and V that use jumper pin Y, a ground pin.
2. Find the PSA value. This is done by inserting the MSA and FAR values into the equation: PSA = MSA–FAR. First, perform the necessary subtraction operation. Then, in Table 14-1, Part 2, locate the proper PSA value. Associated with the PSA is a specific configuration of jumper pins P, N, M, L, and T, all of which use jumper pin R, a ground pin.

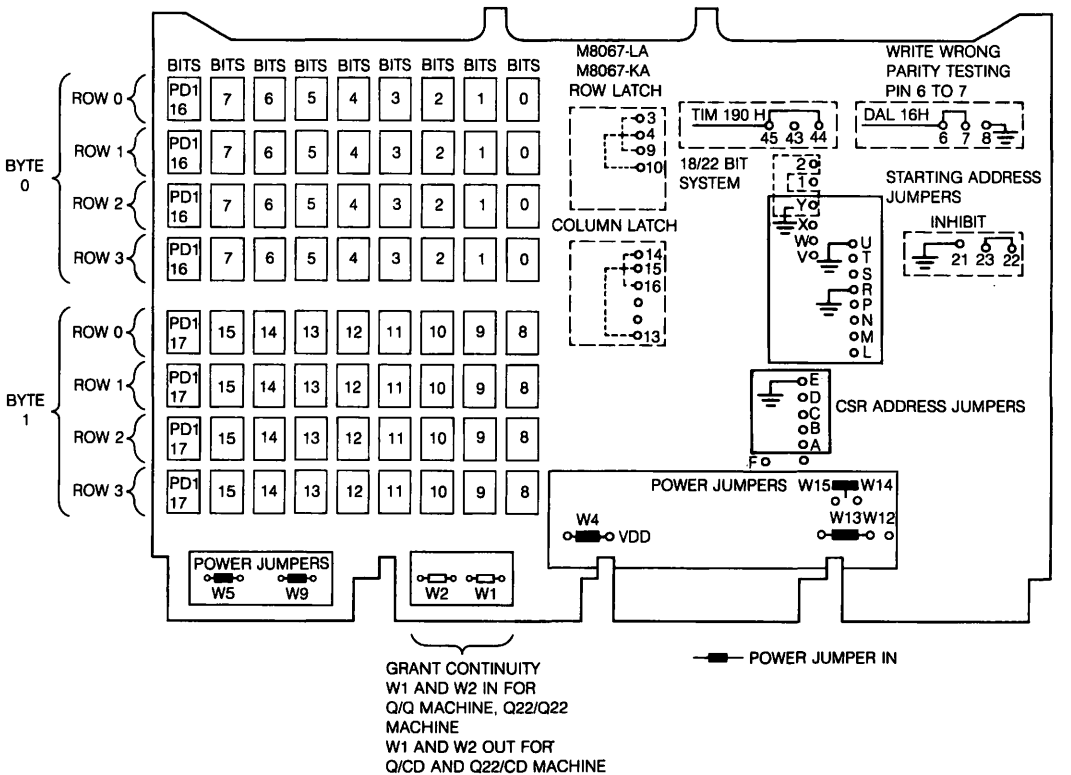


Figure 14-1 ■ MSV11-P Memory Board

Table 14-1 ▪ MSV11-P Starting Address Configurations (Part 1)

First Address Ranges (FAR)		Jumpers In (X) to Ground (Pin Y)		
		Pin X	Pin W	Pin V
Decimal(K)	Octal	A21	A20	A19
000-248	00000000-01740000			
256-504	02000000-03740000			X
512-760	04000000-05740000		X	
768-1016	06000000-07740000		X	X
1024-1272	10000000-11740000	X		
1280-1528	12000000-13740000	X		X
1526-1784	14000000-15740000	X	X	
1742-2040	16000000-17740000	X	X	X

Table 14-1 ▪ MSV11-P Starting Address Configurations (Part 2)

Partial Starting Address (PSA)		Jumpers in (X) to Ground (Pin R)				
		Pin P	Pin N	Pin M	Pin L	Pin T
Decimal(K)	Octal	A18	A17	A16	A15	A14
0	00000000					
8	00040000					X
16	00100000				X	
24	00140000				X	X
32	00200000			X		
40	00240000			X		X
48	00300000			X	X	
56	00340000			X	X	X
64	00400000		X			
72	00440000		X			X
80	00500000		X		X	
88	00540000		X		X	X
96	00600000		X	X		
104	00640000		X	X		X

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Table 14-1 ▪ MSV11-P Starting Address Configurations (Part 2) (Cont.)

Partial Starting Address (PSA)		Jumpers in (X) to Ground (Pin R)				
Decimal(K)	Octal	Pin P A18	Pin N A17	Pin M A16	Pin L A15	Pin T A14
112	00700000		X	X	X	
120	00740000		X	X	X	X
128	01000000	X				
136	01040000	X				X
144	01100000	X			X	
152	01140000	X			X	X
160	01200000	X		X		
168	01240000	X		X		X
176	01300000	X		X	X	
184	01340000	X		X	X	X
192	01400000	X	X			
200	01440000	X	X			X
208	01500000	X	X		X	
216	01540000	X	X		X	X
224	01600000	X	X	X		
232	01640000	X	X	X		X
240	01700000	X	X	X	X	
248	01740000	X	X	X	X	X

Control and Status Register (CSR) Jumpers

Each MSV11-P memory module contains a control and status register. The bus master can read or write the CSR via the Q-bus. The CSR is a 16-bit register with an address that starts in the top 4 Kwords of system address space.

The CSR is assigned to one of the 16 addresses shown in Table 14-2. CSR addresses are assigned as follows.

1. Determine how many memory modules in your system have CSR registers.
2. List the memory modules' sequential position from the CPU.
3. The memory modules closest to the CPU should have the lower module starting address (MSA).
4. The memory module with the lowest MSA is assigned to the lowest CSR address and jumpered according to Table 14-2.
5. The next sequential CSR memory module is assigned the next highest CSR address.

Each memory module has four CSR jumper pins (A, B, C, and D) which can be daisy-chained to pin E, the ground pin. The jumpers allow logic to detect a specific CSR address that has been assigned to a CSR memory module.

For example, assume the system has two memory modules with CSR registers. You are installing the third CSR memory. Refer to Table 14-2 and find the row for the third module. The CSR jumper pin configuration is pin B wirewrapped to pin E. The memory module's CSR address is 17772104 for 22-bit systems or 772104 for 18-bit systems.

Table 14-2 ▪ MSV11-P CSR Address Selection

Module Number	22-Bit System Q-bus Address	18-Bit System Q-bus Address	Jumper in (X) to Ground (Pin E) D	C	B	A
1	17772100	772100				
2	17772102	772102				X
3	17772104	772104			X	
4	17772106	772106			X	X
5	17772110	772110		X		
6	17772112	772112		X		X
7	17772114	772114		X	X	
8	17772116	772116		X	X	X
9	17772120	772120	X			
10	17772122	772122	X			X
11	17772124	772124	X		X	
12	17772126	772126	X		X	X
13	17772130	772130	X	X		
14	17772132	772132	X	X		X
15	17772134	772134	X	X	X	
16	17772136	772136	X	X	X	X

Power Jumpers

The power jumpers for the MSV11-P are configured as follows:

- W3, W10, W11—always out
- W4, W5, W9, W13, W15—in for nonbattery backup
- W4, W5, W12, W14—in for battery backup

For an illustration of these power jumpers, see Figure 14-1.

Note

Digital does not support battery backup.

Bus Grant Continuity Jumpers

Jumpers W1 and W2 are installed only when the module is installed in a Q/Q-type backplane, with Q-bus signals on both sets of connectors. Digital backplanes of this type are the H9270 and the H9275. When the module is installed in a Q/CD-type backplane that uses the CD interconnect on the CD connectors (such as the H9273 and H9276), W1 and W2 are removed. (See Chapter 52 for a discussion of Q/Q and Q/CD backplanes.)

Miscellaneous Jumpers

The miscellaneous jumpers are always configured as follows, and cannot be altered by the user:

Always In: 3-9, 4-10, 6-7, 13-15, 14-16, 43-44
Always Out: 8-7, F-H, 22-23, 44-45

System Size Jumpers

A wirewrap pin is provided to configure the module for the proper addressing mode of the system. Pin 2 is connected to pin Y (ground) when the MSV11-P is used in an 18-bit Q-bus system. In 22-bit systems, this jumper is removed.

Chapter 15 ▪ MSV11-Q MOS Random-Access Memory

The MSV11-Q memory modules each consist of a single, quad-height module containing the Q-bus interface, timing and control logic, refresh circuitry, and up to 4 Mbytes of MOS random-access memory.

There are four variations of the MSV11-Q memory module, as listed in Table 15-1.

Table 15-1 ▪ MSV11-Q Variations

MSV11-QA (Etch Rev A)	64K RAMs fully populated for a total of 1 Mbyte of memory; cannot be configured for battery backup
MSV11-QA (Etch Rev C or later)	64K RAMs fully populated for a total of 1 Mbyte of memory; can be configured for battery backup
MSV11-QB	256K RAMs half populated for a total of 2 Mbytes of memory; can be configured for battery backup
MSV11-QC	256K RAMs fully populated for a total of 4 Mbytes of memory; can be configured for battery backup

Note

The MSV11-QA (Etch Revision C or later), MSV11-QB, and the MSV11-QC all use the same etch. Hereafter in this chapter, these three variations will be collectively referred to as the MSV11-Q to differentiate them from the earlier MSV11-QA (Etch Revision A).

▪ Specifications

Identification	M7551
Size	Quad
Power Requirements	
Bus Loads	
ac	2.4
dc	1.0

Supply Voltage	MSV11-QA*	MSV11-QB	MSV11-QC
+5 V system power:			
Typical operating power	2.8 A	2.3 A	2.5 A
Typical standby power	1.0 A	1.0 A	1.0 A
+5 V battery backup:			
Typical operating power	1.4 A	1.3 A	1.5 A
Typical standby power	1.28 A	1.18 A	1.34 A

* All etch revisions

Access and Cycle Times

	Access Time (ns) (1)			Cycle Time (ns) (1)		
Bus Cycle	**Typical**	**Maximum**	**Notes**	**Typical**	**Maximum**	**Notes**
MSV11-QA (Etch Rev A)						
DATI	320	358	2	520	578	4
DATO(B)	350	376	2	550	597	5
DATIO(B)	1000	1045	3	1220	1255	6
MSV11-Q						
DATI	320	358	2	510	563	4
DATO(B)	160	189	2	550	592	5
DATIO(B)	780	847	3	1220	1250	6
All variations						
Refresh	—	—	—	535	616	7

Parity—CSR configurations, refer to notes 1, 8, and 9.

Notes

1. Assuming memory not busy and no arbitration.
2. SYNC to RPLY with minimum times (25/50 ns) from SYNC to (DIN/DOUT). The DATO(B) access and cycle times assume a minimum of 50 ns from SYNC to DOUT inside memory receivers. For actual Q-bus measurements, a constant (K - 50 ns, where K = 200 ns) should be added to DATI(B) times. That is, access time (typical) = 100 + (200–50) = 250 ns.
3. SYNC to RPLY DATIO(B), with minimum time (25 ns) from SYNC to DIN and minimum 350 ns from RPLY (DATI) asserted to DOUT asserted.
4. SYNC to MBSY negated.
5. SYNC to MBSY negated with minimum time (50 ns) from SYNC to DOUT.

6. SYNC to MBSY (DATIO(B)) with minimum times (25 ns) from SYNC to DIN and minimum 350 ns from RPLY (DATI) asserted to DOUT asserted.
7. REF REQ to MBSY negated.
8. The MSV11-Q does not lose any time due to refresh arbitration.
9. Refresh conflict adds 250 ns typical and 542 ns maximum to access and cycle time.

▪ Related Documentation

Document Title	Order Number
MSV11-QA Memory User's Guide	EK-MSV1Q-UG
MSV11-Q Field Maintenance Print Set	MP-01931-00
MSV11 Diagnostic Documentation Kit	ZJ246-RZ

▪ Configuration of the MSV11-QA (Etch Rev A)

The MSV11-QA (Etch Rev A) module has several jumpers and two dual inline package (DIP) switchpacks used to configure the module. Memory starting and ending addresses and the CSR register address are user-configurable.

Figure 15-1 shows the locations of these jumpers and switches. To jumper two pins, a 0-ohm connector block is used.

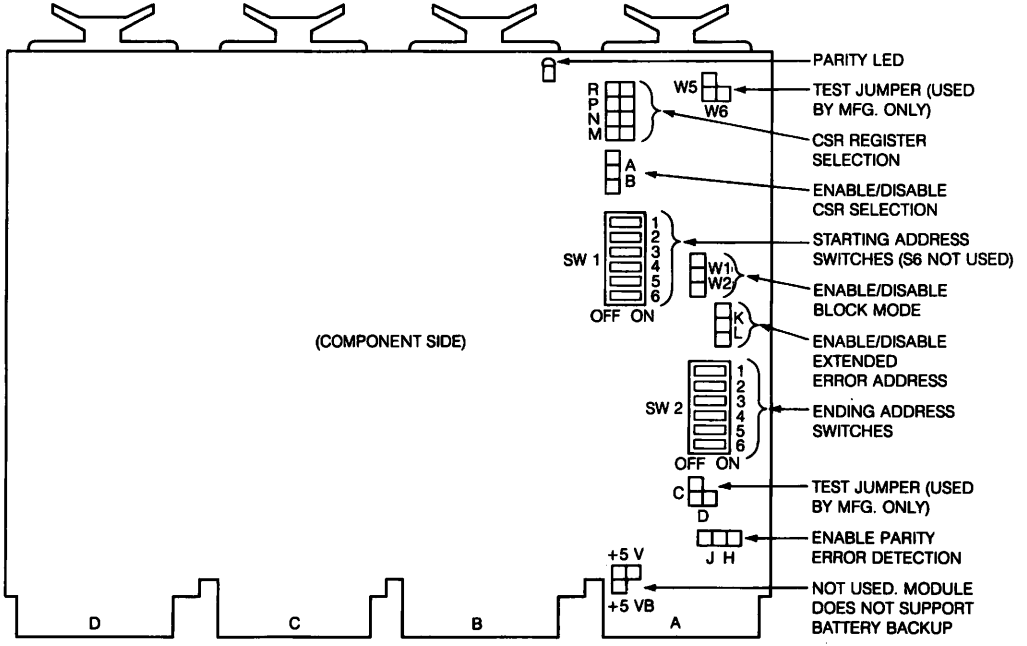

Figure 15-1 ■ MSV11-QA (Etch Rev A) Switches and Jumpers

Memory Starting and Ending Addresses

The two switchpacks on the MSV11-QA memory module are used to configure the memory starting and ending address. The module's starting address is determined by the amount of memory already configured in the system. The ending address is always some number higher than the starting address.

The memory starting address is configured using switches 1 through 5 of switchpack SW1 and switch 6 of switchpack SW2, as shown in Table 15-2. The ending address is configured using switches 1 through 5 of switchpack SW2, as shown in Table 15-3. Note that switch 6 of SW2 is set to the ON position for a starting address of 0 and set to the OFF position for all other starting addresses. Switch 6 of switchpack SW1 is not used.

Table 15-2 ▪ MSV11-QA (Etch Rev A) Starting Address Switches

Starting Address	Switch Settings					
	SW1-1	SW1-2	SW1-3	SW1-4	SW1-5	SW2-6
0 Kbyte	ON	ON	ON	ON	ON	ON
128 Kbytes	OFF	OFF	OFF	OFF	OFF	OFF
256 Kbytes	ON	OFF	OFF	OFF	OFF	OFF
384 Kbytes	OFF	ON	OFF	OFF	OFF	OFF
512 Kbytes	ON	ON	OFF	OFF	OFF	OFF
640 Kbytes	OFF	OFF	ON	OFF	OFF	OFF
768 Kbytes	ON	OFF	ON	OFF	OFF	OFF
896 Kbytes	OFF	ON	ON	OFF	OFF	OFF
1024 Kbytes (1 Mbyte)	ON	ON	ON	OFF	OFF	OFF
1152 Kbytes	OFF	OFF	OFF	ON	OFF	OFF
1280 Kbytes	ON	OFF	OFF	ON	OFF	OFF
1408 Kbytes	OFF	ON	OFF	ON	OFF	OFF
1536 Kbytes	ON	ON	OFF	ON	OFF	OFF
1664 Kbytes	OFF	OFF	ON	ON	OFF	OFF
1792 Kbytes	ON	OFF	ON	ON	OFF	OFF
1920 Kbytes	OFF	ON	ON	ON	OFF	OFF
2048 Kbytes (2 Mbytes)	ON	ON	ON	ON	OFF	OFF

(continued on next page)

Table 15-2 ▪ MSV11-QA (Etch Rev A) Starting Address Switches (Cont.)

Starting Address	Switch Settings SW1-1	SW1-2	SW1-3	SW1-4	SW1-5	SW2-6
2176 Kbytes	OFF	OFF	OFF	OFF	ON	OFF
2304 Kbytes	ON	OFF	OFF	OFF	ON	OFF
2432 Kbytes	OFF	ON	OFF	OFF	ON	OFF
2560 Kbytes	ON	ON	OFF	OFF	ON	OFF
2688 Kbytes	OFF	OFF	ON	OFF	ON	OFF
2816 Kbytes	ON	OFF	ON	OFF	ON	OFF
2944 Kbytes	OFF	ON	ON	OFF	ON	OFF
3072 Kbytes (3 Mbytes)	ON	ON	ON	OFF	ON	OFF
3200 Kbytes	OFF	OFF	OFF	ON	ON	OFF
3328 Kbytes	ON	OFF	OFF	ON	ON	OFF
3456 Kbytes	OFF	ON	OFF	ON	ON	OFF
3584 Kbytes	ON	ON	OFF	ON	ON	OFF
3712 Kbytes	OFF	OFF	ON	ON	ON	OFF
3840 Kbytes	ON	OFF	ON	ON	ON	OFF
3968 Kbytes	OFF	ON	ON	ON	ON	OFF

Note

Note that for a starting address of 0, switch 6 of switchpack SW2 should be set to the ON position; for all other starting addresses, this switch should be set to the OFF position.

Table 15-3 ▪ MSV11-QA (Etch Rev A) Ending Address Switches

Ending Address	Switch Settings SW2-1	SW2-2	SW2-3	SW2-4	SW2-5
128 Kbytes	OFF	OFF	OFF	OFF	OFF
256 Kbytes	ON	OFF	OFF	OFF	OFF
384 Kbytes	OFF	ON	OFF	OFF	OFF
512 Kbytes	ON	ON	OFF	OFF	OFF

(continued on next page)

Table 15-3 ▪ MSV11-QA (Etch Rev A) Ending Address Switches (Cont.)

Ending Address	Switch Settings SW2-1	SW2-2	SW2-3	SW2-4	SW2-5
640 Kbytes	OFF	OFF	ON	OFF	OFF
768 Kbytes	ON	OFF	ON	OFF	OFF
896 Kbytes	OFF	ON	ON	OFF	OFF
1024 Kbytes (1 Mbyte)	ON	ON	ON	OFF	OFF
1152 Kbytes	OFF	OFF	OFF	ON	OFF
1280 Kbytes	ON	OFF	OFF	ON	OFF
1408 Kbytes	OFF	ON	OFF	ON	OFF
1536 Kbytes	ON	ON	OFF	ON	OFF
1664 Kbytes	OFF	OFF	ON	ON	OFF
1792 Kbytes	ON	OFF	ON	ON	OFF
1920 Kbytes	OFF	ON	ON	ON	OFF
2048 Kbytes (2 Mbytes)	ON	ON	ON	ON	OFF
2176 Kbytes	OFF	OFF	OFF	OFF	ON
2304 Kbytes	ON	OFF	OFF	OFF	ON
2432 Kbytes	OFF	ON	OFF	OFF	ON
2560 Kbytes	ON	ON	OFF	OFF	ON
2688 Kbytes	OFF	OFF	ON	OFF	ON
2816 Kbytes	ON	OFF	ON	OFF	ON
2944 Kbytes	OFF	ON	ON	OFF	ON
3072 Kbytes (3 Mbytes)	ON	ON	ON	OFF	ON
3200 Kbytes	OFF	OFF	OFF	ON	ON
3328 Kbytes	ON	OFF	OFF	ON	ON
3456 Kbytes	OFF	ON	OFF	ON	ON
3584 Kbytes	ON	ON	OFF	ON	ON
3712 Kbytes	OFF	OFF	ON	ON	ON
3840 Kbytes	ON	OFF	ON	ON	ON
3968 Kbytes	OFF	ON	ON	ON	ON
4096 Kbytes (4 Mbytes)	ON	ON	ON	ON	ON

Control and Status Register Address

The MSV11-QA has a control and status register (CSR) that can be used for program control of certain parity functions and contains diagnostic information when a parity error occurs. Up to 16 different CSR addresses can be selected using jumpers R, P, N, and M, as shown in Table 15-4.

Table 15-4 ▪ MSV11-QA (Etch Rev A) CSR Address Jumpers

	Jumper Position			
CSR Address	**R**	**P**	**N**	**M**
17772100	IN	IN	IN	IN
17772102	OUT	IN	IN	IN
17772104	IN	OUT	IN	IN
17772106	OUT	OUT	IN	IN
17772110	IN	IN	OUT	IN
17772112	OUT	IN	OUT	IN
17772114	IN	OUT	OUT	IN
17772116	OUT	OUT	OUT	IN
17772120	IN	IN	IN	OUT
17772122	OUT	IN	IN	OUT
17772124	IN	OUT	IN	OUT
17772126	OUT	OUT	IN	OUT
17772130	IN	IN	OUT	OUT
17772132	OUT	IN	OUT	OUT
17772134	IN	OUT	OUT	OUT
17772136	OUT	OUT	OUT	OUT

Miscellaneous Jumpers

The following jumpers are configured at the factory and generally should not be changed:

- TEST JUMPERS

  Jumpers C, D, W5, and W6 are used by manufacturing for test purposes and should not be changed. C and W6 should remain installed; D and W5 should remain removed.

- CSR SELECTION JUMPER
  Jumper B is used to control CSR selection when nonparity memory is used. Since the MSV11-QA is a parity memory, jumper B should remain installed to enable CSR selection.

- BLOCK MODE JUMPER
  Jumper W1 is used to control block mode operation. The jumper should remain installed to enable block mode.

- EXTENDED ADDRESSING JUMPER
  Jumper L is used to select either 18- or 22-bit addressing. The jumper should remain installed to select 22-bit addressing.

- PARITY JUMPER
  Jumper H is used to control parity error detection. The jumper should remain installed to enable parity error detection.

Configuration of the MSV11-Q

The MSV11-Q module has several jumpers and two dual in-line package (DIP) switchpacks used to configure the module. The following features are user-selectable:

- Memory starting and ending addresses
- CSR register address
- Battery backup

Figure 15-2 shows the locations of these jumpers and switches.

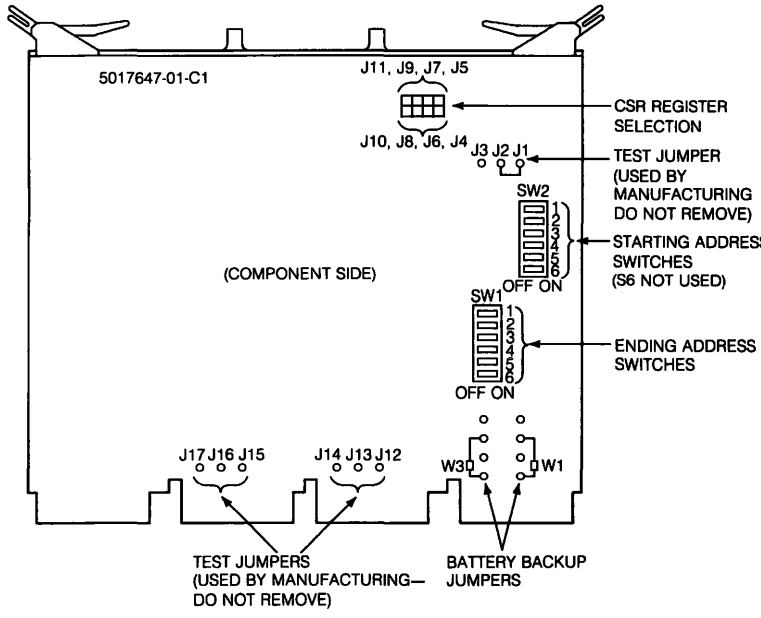

Figure 15-2 ▪ MSV11-Q Switches and Jumpers

Memory Starting and Ending Addresses

The two switchpacks on the MSV11-Q memory module are used to configure the memory starting and ending address. The module's starting address is determined by the amount of memory already configured in the system. The ending address is always some number higher than the starting address.

The memory starting address is configured using switches 1 through 5 of switchpack SW2 and switch 6 of switchpack SW1, as shown in Table 15-5. The ending address is configured using switches 1 through 5 of switchpack SW1, as shown in Table 15-6. Note that switch 6 of SW1 is set to the ON position for a starting address of 0 and set to the OFF position for all other starting addresses. Switch 6 of switchpack SW2 is not used.

Table 15-5 ▪ MSV11-Q Starting Address Switches

Starting Address	Switch Settings					
	SW2-1	SW2-2	SW2-3	SW2-4	SW2-5	SW1-6
0 Kbytes	ON	ON	ON	ON	ON	ON
128 Kbytes	OFF	OFF	OFF	OFF	OFF	OFF
256 Kbytes	ON	OFF	OFF	OFF	OFF	OFF
384 Kbytes	OFF	ON	OFF	OFF	OFF	OFF
512 Kbytes	ON	ON	OFF	OFF	OFF	OFF
640 Kbytes	OFF	OFF	ON	OFF	OFF	OFF
768 Kbytes	ON	OFF	ON	OFF	OFF	OFF
896 Kbytes	OFF	ON	ON	OFF	OFF	OFF
1024 Kbytes (1 Mbyte)	ON	ON	ON	OFF	OFF	OFF
1152 Kbytes	OFF	OFF	OFF	ON	OFF	OFF
1280 Kbytes	ON	OFF	OFF	ON	OFF	OFF
1408 Kbytes	OFF	ON	OFF	ON	OFF	OFF
1536 Kbytes	ON	ON	OFF	ON	OFF	OFF
1664 Kbytes	OFF	OFF	ON	ON	OFF	OFF
1792 Kbytes	ON	OFF	ON	ON	OFF	OFF
1920 Kbytes	OFF	ON	ON	ON	OFF	OFF
2048 Kbytes (2 Mbytes)	ON	ON	ON	ON	OFF	OFF
2176 Kbytes	OFF	OFF	OFF	OFF	ON	OFF
2304 Kbytes	ON	OFF	OFF	OFF	ON	OFF
2432 Kbytes	OFF	ON	OFF	OFF	ON	OFF
2560 Kbytes	ON	ON	OFF	OFF	ON	OFF
2688 Kbytes	OFF	OFF	ON	OFF	ON	OFF
2816 Kbytes	ON	OFF	ON	OFF	ON	OFF
2944 Kbytes	OFF	ON	ON	OFF	ON	OFF
3072 Kbytes (3 Mbytes)	ON	ON	ON	OFF	ON	OFF

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Table 15-5 ▪ MSV11-Q Starting Address Switches (Cont.)

Starting Address	Switch Settings SW2-1	SW2-2	SW2-3	SW2-4	SW2-5	SW1-6
3200 Kbytes	OFF	OFF	OFF	ON	ON	OFF
3328 Kbytes	ON	OFF	OFF	ON	ON	OFF
3456 Kbytes	OFF	ON	OFF	ON	ON	OFF
3584 Kbytes	ON	ON	OFF	ON	ON	OFF
3712 Kbytes	OFF	OFF	ON	ON	ON	OFF
3840 Kbytes	ON	OFF	ON	ON	ON	OFF
3968 Kbytes	OFF	ON	ON	ON	ON	OFF

Note

Note that for a starting address of 0, switch 6 of switchpack SW1 should be set to the ON position; for all other starting addresses, this switch should be set to the OFF position.

Table 15-6 ▪ MSV11-Q Ending Address Switches

Ending Address	Switch Settings SW1-1	SW1-2	SW1-3	SW1-4	SW 1-5
128 Kbytes	OFF	OFF	OFF	OFF	OFF
256 Kbytes	ON	OFF	OFF	OFF	OFF
384 Kbytes	OFF	ON	OFF	OFF	OFF
512 Kbytes	ON	ON	OFF	OFF	OFF
640 Kbytes	OFF	OFF	ON	OFF	OFF
768 Kbytes	ON	OFF	ON	OFF	OFF
896 Kbytes	OFF	ON	ON	OFF	OFF
1024 Kbytes (1 Mbyte)	ON	ON	ON	OFF	OFF
1152 Kbytes	OFF	OFF	OFF	ON	OFF
1280 Kbytes	ON	OFF	OFF	ON	OFF
1408 Kbytes	OFF	ON	OFF	ON	OFF
1536 Kbytes	ON	ON	OFF	ON	OFF
1664 Kbytes	OFF	OFF	ON	ON	OFF

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Table 15-6 • MSV11-Q Ending Address Switches (Cont.)

Ending Address	Switch Settings SW1-1	SW1-2	SW1-3	SW1-4	SW 1-5
1792 Kbytes	ON	OFF	ON	ON	OFF
1920 Kbytes	OFF	ON	ON	ON	OFF
2048 Kbytes (2 Mbytes)	ON	ON	ON	ON	OFF
2176 Kbytes	OFF	OFF	OFF	OFF	ON
2304 Kbytes	ON	OFF	OFF	OFF	ON
2432 Kbytes	OFF	ON	OFF	OFF	ON
2560 Kbytes	ON	ON	OFF	OFF	ON
2688 Kbytes	OFF	OFF	ON	OFF	ON
2816 Kbytes	ON	OFF	ON	OFF	ON
2944 Kbytes	OFF	ON	ON	OFF	ON
3072 Kbytes (3 Mbytes)	ON	ON	ON	OFF	ON
3200 Kbytes	OFF	OFF	OFF	ON	ON
3328 Kbytes	ON	OFF	OFF	ON	ON
3456 Kbytes	OFF	ON	OFF	ON	ON
3584 Kbytes	ON	ON	OFF	ON	ON
3712 Kbytes	OFF	OFF	ON	ON	ON
3840 Kbytes	ON	OFF	ON	ON	ON
3968 Kbytes	OFF	ON	ON	ON	ON
4096 Kbytes (4 Mbytes)	ON	ON	ON	ON	ON

Control and Status Register Address

The MSV11-Q has a control and status register (CSR) that can be used for program control of certain parity functions and contains diagnostic information when a parity error occurs. Up to 16 different CSR addresses can be selected using jumpers J4 through J11, as shown in Table 15-7.

Table 15-7 ▪ MSV11-Q CSR Address Jumpers

	Jumper Connections			
CSR Address	**J4 to J5**	**J6 to J7**	**J8 to J9**	**J10 to J11**
17772100	IN	IN	IN	IN
17772102	OUT	IN	IN	IN
17772104	IN	OUT	IN	IN
17772106	OUT	OUT	IN	IN
17772110	IN	IN	OUT	IN
17772112	OUT	IN	OUT	IN
17772114	IN	OUT	OUT	IN
17772116	OUT	OUT	OUT	IN
17772120	IN	IN	IN	OUT
17772122	OUT	IN	IN	OUT
17772124	IN	OUT	IN	OUT
17772126	OUT	OUT	IN	OUT
17772130	IN	IN	OUT	OUT
17772132	OUT	IN	OUT	OUT
17772134	IN	OUT	OUT	OUT
17772136	OUT	OUT	OUT	OUT

Battery Backup

The MSV11-Q can be configured for battery backup by connecting the 0-ohm jumpers W1 and W3. To configure the module without battery backup, connect the 0-ohm jumpers W2 and W4. All other configurations of jumpers W1 through W4 are illegal.

Note

On systems using backpanel pin <AE1> SSPARE1 for signals other than +5 V BBU, jumper W1 can be omitted when the module is strapped for battery backup operation. However, Digital recommends that backpanel pin <AE1> be used as +5 V battery backup power in this application.

Miscellaneous Jumpers

The following jumpers are configured at the factory and should not be changed.

- CHIP SELECT JUMPERS

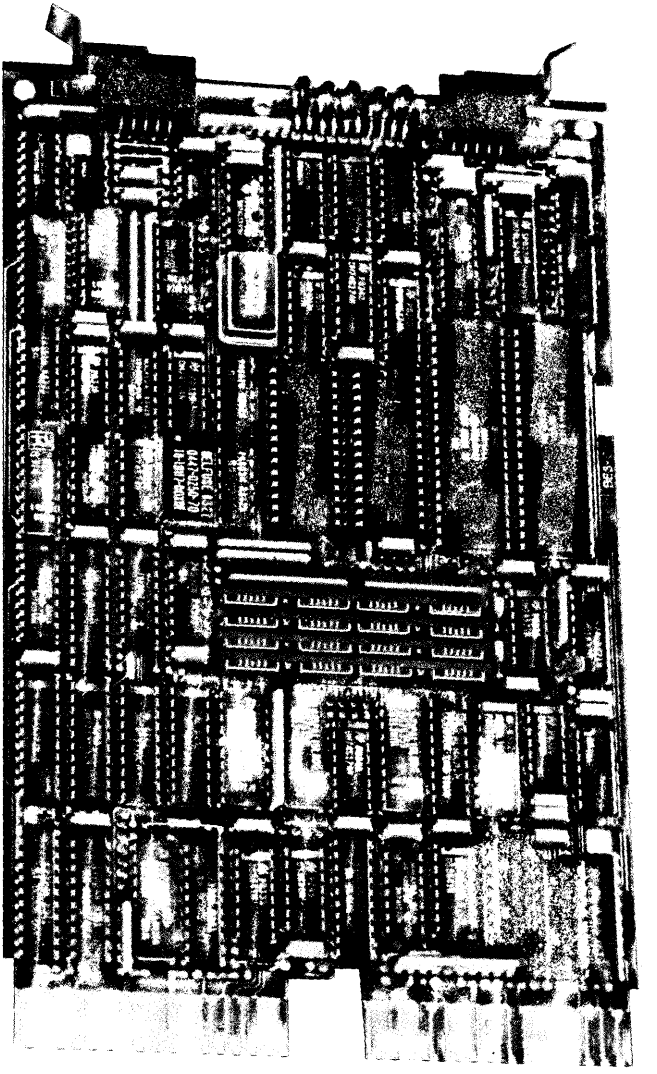
  Jumpers J12 through J17 are used to select the RAM chip size appropriate for the module variation. They are factory-configured as listed below and should not be changed.

Jumper Connections	Chip Size	Module Variation
J13 to J14 J15 to J16	64 Kbytes	MSV11-QA (Etch Rev C or later)
J12 to J13 J16 to J17	256 Kbytes	MSV11-QB or MSV11-QC

- TEST JUMPERS

  Jumpers J1 through J3 are used by manufacturing for test purposes and should not be changed. Jumper J1 should always be connected to J2.

Part IV • Multifunction Modules



Chapter 16 • Introduction to Multifunction Modules

Digital provides two multifunction modules for use with Q-bus systems: the MXV11-A and the MXV11-B. These dual-height modules contain read/write memory, provisions for user-supplied read-only memory, two asynchronous serial line interfaces, and linetime clock signal capabilities. The primary difference between the two modules is that whereas the MXV11-A will operate in 16- and 18-bit systems only, the MXV11-B also is designed for use in 22-bit systems.

Table 16-1 compares the various features of the two modules. Refer to Chapter 8 and Chapter 19 for descriptions of the features listed.

Table 16-1 • Multifunction Module Comparison/Summary Chart

Feature	MXV11-A	MXV11-B
Bus addressing	16- or 18-bit	16-, 18- or 22-bit
Read/write memory		
Memory size	8 or 32 Kbytes	128 Kbytes
Onboard refresh	yes	yes
Battery backup	no	selectable
Start address	8-Kbyte boundary	8-Kbyte boundary
Read-only memory		
Sockets	(2) 24-pin	(2) 28-pin
Chip sizes	1K × 8, 2K × 8, or 4K × 8	2K × 8, 4K × 8, or 8K × 8
Bootstrap ROM	MXV11-A2	MXV11-B2
Window-map access	no	yes
Serial line units		
Interface	RS-232	EIA-423 or RS-232
Baud rates	150, 300, 1200, 2400, 4800, 9600, 19.2K, or 38.4K	300, 1200, 9600, or 38.4K
Console port	SLU 1	SLU 1
Linetime clock	60 Hz	50, 60, or 800 Hz

Chapter 17 • MXV11-A Memory and Asynchronous Serial Line Interface

The MXV11-A is a dual-height multifunction option module for use in 16- or 18-bit Q-bus systems.

• Model Options

MXV11-AA	Q-bus multifunction module, 8 Kbytes of random-access memory
MXV11-AC	Q-bus multifunction module, 32 Kbytes of random-access memory

• Specifications

Identification	
MXV11-AA	M8047-AA
MXV11-AC	M8047-AC
Size	Dual
Power Requirements	+5 Vdc, 1.2 A (typical) +12 Vdc, 0.1 A (typical)
Bus Loads	
ac	2.0
dc	2.0

RAM Performance

	Access Time — T acc (ns)	
Bus Cycle	**Typical**	**Maximum**
DATI	280	300
DATO(B)	395	410

Notes

1. Access time (T acc) is from SYNC to RPLY.
2. Assumes memory is not busy and there is no arbitration.
3. Refresh arbitration adds 100 ns typical and 120 ns maximum to access time.
4. Refresh conflict adds 575 ns typical and 600 ns maximum to access time.
5. Assumes that SYNC to DOUT time = 285 ns.

ROMS	
Power	+5 Vdc ±5%
Pins	24-pin spacing
Access Time	Up to 450 ns
Array Size	1K×8, 2K×8, or 4K×8 bits
Types	See table below

	Chip Array Size	Memory Size
UV PROMS		
Intel 2758	1K×8 bits	1 Kwords
Intel 2716	2K×8 bits	2 Kwords
Intel 2732	4K×8 bits	4 Kwords
Mostek MK2716	2K×8 bits	2 Kwords
TI TMS 2516	2K×8 bits	2 Kwords
TI TMS 2532	4K×8 bits	4 Kwords
Bipolar PROMS		
Intel 3628	1K×8 bits	1 Kwords
Signetics 82S 2708	1K×8 bits	1 Kwords
Signetics 82S 181	1K×8 bits	1 Kwords
Signetics 82S 191	2K×8 bits	2 Kwords

▪ Related Documentation

Document Title	Order Number
MXV11-A Field Maintenance Print Set	MP-00730-00

▪ Configuration

The user can configure the MXV11-A features by using the jumpers provided on the board. The jumpers on this module are of two types. Two jumpers consist of insulated wires soldered to plated-through holes, and the remaining jumpers are wirewrap pins to which connections are made. Figure 17-1 illustrates the MXV11-A jumper locations. The soldered jumpers are factory-configured and should not be changed. When installing jumpers, the wire runs must be arranged so that no more than two wires are on each pin and there is no level jumping between pins. Table 17-1 lists the factory-configured wiring scheme. Table 17-2 lists and describes the function of each jumper on the MXV11-A board.

The ROM and RAM memories should not be configured to cover the same area of memory. There is no overlay protection logic to prevent conflicts in this case. The RAM memory will not respond to addresses in the I/O page area (bank 7 in 16-bit address systems). This prevents conflicts when peripherals (including the onboard SLUs) are addressed.

Table 17-1 ▪ MXV11-A Factory Configuration Guide

Function	Wirewrap Pins From	To
RAM Bank 0	J30	J31
	J32	J33
	J31	J32
SLU Channel 0 Address 176500	J23	J18
	J24	J19
SLU Channel 1 Address 177560	J28	J19
	J26	J15
	J25	J14
	J27	J13
ROM Bootstrap (TU58)	J37	J38
	J21	J22
	J34	J37
	J33	J39
	J29	J15
SLU Vectors CH0 (300)	J53	J57
CH1 (60)	J54	J52
	J55	J54
	J56	J51
SLU Parameters (eight data bits,	J59	J61
no parity, one stop bit)	J62	J64
	J60	J63
	J61	J62
	J59	J66
	J63	J65
Baud Rates CH0 (38400)	J45	J50
CH1 (9600)	J46	J48
Break Generation (Halt option)	J6	J7
Crystal Clock	J68	J67

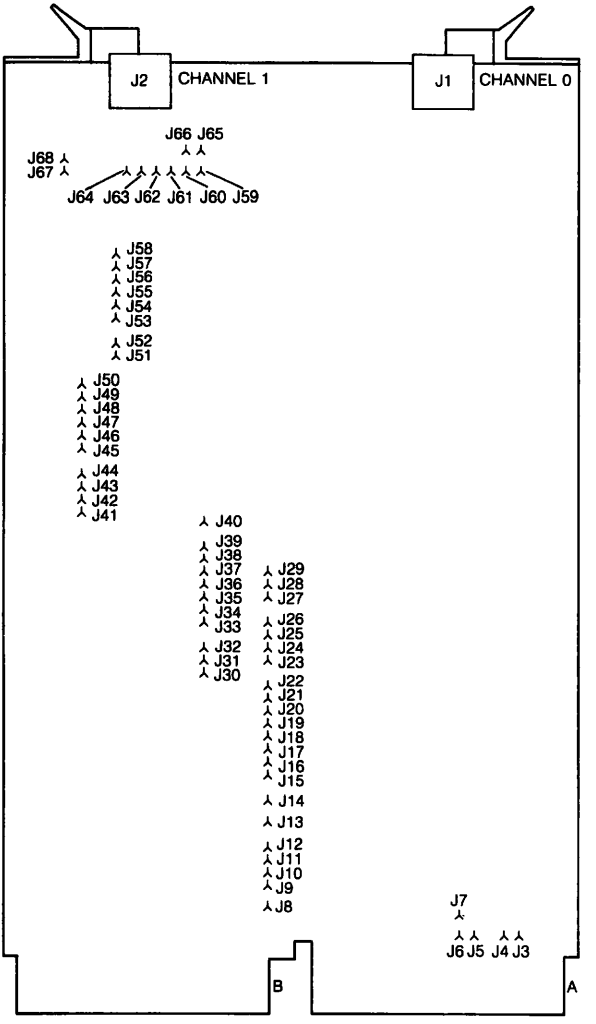


Figure 17-1 ▪ MXV11-A Jumper Locations

Table 17-2 ▪ MXV11-A Jumper Locations

Pin	Option	Function
J3	60 Hz	Clock. Open collector output of the clock. Connected to Pin AF1 (SSpare 2). Wirewrap to J4 to implement the clock option.
J4	60 Hz	BEVNT. Event interrupt (Pin BR1) used for the clock option.
J5	BOOT	BDCOK. DCOK (Pin BA1) when HIGH allows the processor to operate; when LOW initializes the system. Connected to J6 to implement the boot option.
J6	BREAK	Framing error. Open collector output of framing error from serial line one. Connected to Pin AE1 (SSpare 1). Wirewrap to J5 to implement the boot option or to J7 for the halt option. Reset by bus initialize or reception of a valid character.
J7	HALT	BHALT. Halt (Pin AP1) when LOW will stop program execution and cause the processor to enter ODT microcode. Connected to J6 to implement the halt option.
J8	ROM	GND. A ground signal that can be used to disable ROM by wirewrapping to J21 or to disable a serial line by wirewrapping to an address input pin (J23 or J24 for serial line 0; or J25, J26, J27, or J28 for serial line 1).
J9	ROM	A13 L. Address bit 13 asserted LOW. Wirewrap to J11 to select Bank 1 with the ROM address decoder.
J10	ROM	A13 H. Address bit 13 asserted HIGH. Wirewrap to J11 to select Bank 0 with the ROM address decoder.
J11	ROM	A13 M. Address bit 13 input to the ROM address decoder. See J9 and J10. Used only if J20 is wirewrapped to J21.

(continued on next page)

Table 17-2 ▪ MXV11-A Jumper Locations (Cont.)

Pin	Option	Function
J12	SLU	A03 H. Address bit 03 asserted HIGH. Wirewrapped to the serial line address decoders (J23 or J24 for serial line 0; J25, J26, J27 or J28 for serial line 1) when address bit 03 is to be decoded as a 1.
J13	SLU	A04 H. Address bit 04 asserted HIGH. Wirewrapped to the serial line address decoders when address bit 04 is to be decoded as a 1.
J14	SLU	A05 H. Address bit 05 asserted HIGH. Wirewrapped to the serial line 1 address decoder when address bit 05 is to be decoded as a 1.
J15	SLU	A09 H. Address bit 09 asserted HIGH. Wirewrapped to the serial line 1 address decoder when address bit 09 is to be decoded as a 1.
J16	SLU	A09 L. Address bit 09 asserted LOW. Wirewrapped to the serial line 1 address decoder when address bit 09 is to be decoded as a 0.
J17	SLU	A05 L. Address bit 05 asserted LOW. Wirewrapped to the serial line 1 address decoder when address bit 05 is to be decoded as a 0.
J18	SLU	A04 L. Address bit 04 asserted LOW. Wirewrapped to the serial line address decoders when address bit 04 is to be decoded as a 0.
J19	SLU	A03 L. Address bit 03 asserted LOW. Wirewrapped to the serial line address decoders when address bit 03 is to be decoded as a 0.
J20	ROM	ROM address. Output of the ROM address decoder. Connected to J21 when ROM is to be used in Bank 0 or Bank 1.
J21	ROM	ROM select. ROM address selection enable asserted HIGH. Wirewrapped to J8 (GND) to disable ROM, to J20 for Bank 0 or Bank 1, or to J22 for bootstrap.

(continued on next page)

Table 17-2 • MXV11-A Jumper Locations (Cont.)

Pin	Option	Function
J22	BOOT	Boot address. Output of the bootstrap address decoder. Connected to J21 when ROM is to be used in the bootstrap range from 173000-173776 (773000-773776 for 18-bit systems).
J23	SLU	Serial line 0 address decoder input asserted HIGH. May be wirewrapped to A03 H (J12), A03 L (J19), A04 H (J13) or A04 L (J18).
J24	SLU	Serial line 0 address decoder input asserted HIGH. May be wirewrapped to A03 or A04, whichever bit is not wired to J23. May be wirewrapped to GND (J8) to disable serial line zero.
J25-J28	SLU	Serial line 1 address decoder input asserted HIGH. Four address decoder inputs to be connected to address bits A03, A04, A05, and A09. Whether the HIGH or LOW assertion state of a bit is wirewrapped to an input determines if that bit is decoded as a 1 or a 0. See J12 through J19. May be wirewrapped to GND (J8) to disable serial line one.
J29	ROM	ROM address bit 09 input. Wirewrapped to A09 H (J15) for normal ROM addressing and also for the MXV11-A2 option when the TU58 bootstrap is desired. Wirewrapped to A09 L (J16) for the MXV11-A2 option when the disk bootstrap is desired.

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Table 17-2 ▪ MXV11-A Jumper Locations (Cont.)

Pin	Option	Function
J30-J32	RAM	RAM starting address selection. These pins are wirewrapped to J33 (logic 0) or J34 (logic 1) to select the RAM starting address. (See below)

J32	J31	J30	Bank	Address
0	0	0	0	000000
0	0	1	1	020000
0	1	0	2	040000
0	1	1	3	060000
1	0	0	4	100000
1	0	1	5	120000
1	1	0	6	140000
1	1	1	7	160000

J33	RAM,ROM	GND. Logic 0 level signal used for selecting the RAM starting address and for enabling some ROM ICs in the ROM sockets.
J34	RAM,ROM	3V. Logic 1 level signal used for selecting the RAM starting address and for enabling some ROM ICs in the ROM sockets.
J35	ROM	A12 H. Address bit 12 asserted HIGH. Used for addressing 4K × 8 bit ROMs. Wirewrapped to J37, J38, or J39, depending on the ROM used.
J36	ROM	A11 H. Address bit 11 asserted HIGH. Used for addressing 2K × 8 and 4K × bit ROMs. Wirewrapped to J37, J38 or J39, depending on the ROM.
J37	ROM	Pin 18 on both ROM sockets. Used for addressing or enabling ROM. Wirewrapped to J33 for ground, to J34 for +3V, to J35 for A12 or to J36 for A11.
J38	ROM	Pin 19 on both ROM sockets. Used for addressing or enabling ROM. Wirewrapped to J33 for ground, to J34 for +3V, to J35 for A12 or to J36 for A11.

(continued on next page)

Table 17-2 ▪ MXV11-A Jumper Locations (Cont.)

Pin	Option	Function
J39	ROM	Pin 21 on both ROM sockets. Used for addressing or enabling ROM. Wirewrapped to J33 for ground, to J34 for +3V, to J35 for A12, to J36 for A11 or to J40 for +5V.
J40	ROM	+5V. Used to power some ROMs on pin 21.
J41	SLU	Used for 150 baud. Wirewrapped to J45 for serial line 0, to J46 for serial line 1 (see Table 17-9).
J42	SLU	Used for 1200 baud.
J43	SLU	Used for 300 baud.
J44	SLU	Used for 2400 baud.
J45	SLU	Clock 0. The clock input for serial line 0 transmit and receive, 16 times the baud rate. Wirewrapped to either J41, J42, J43, J44, J47, J48, J49, or J50.
J46	SLU	Clock 1. The clock input for serial line 1 transmit and receive, 16 times the baud rate. Wirewrapped to either J41, J42, J43, J44, J47, J48, J49, or J50.
J47	SLU	Used for 4800 baud.
J48	SLU	Used for 9600 baud.
J49	SLU	Used for 19200 baud.
J50	SLU	Used for 38400 baud.
J51	SLU	VEC 0. Vector enable for channel 0. Used to drive vector bits that pass the test: logic 1 for channel 0 and logic 0 for channel 1. Wirewrapped to J53 for bit 03, to J54 for bit 04, to J55 for bit 05, to J56 for bits 06 and 07.
J52	SLU	VEC 1. Vector enable for channel 1. Used to drive vector bits that pass the test: logic 0 for channel 0 and logic 1 for channel 1. Wirewrapped to J53 for bit 03, to J54 for bit 04, to J55 for bit 05, to J56 for bits 06 and 07.

(continued on next page)

Table 17-2 ▪ MXV11-A Jumper Locations (Cont.)

Pin	Option	Function
J53	SLU	Vector bit 03. Selects how bit 03 is to be driven for interrupt vectors. Wirewrapped to J51 if a logic 1 for channel 0 and a logic 0 for channel 1, to J52 if a logic 0 for channel 0 and a logic 1 for channel 1, to J57 if a logic 0 for both channel 0 and channel 1, or to J58 if a logic 1 for both channel 0 and channel 1.
J54	SLU	Vector bit 04. Selects how bit 04 is to be driven for interrupt vectors. Wirewrapped the same as J53.
J55	SLU	Vector bit 05. Selects how bit 05 is to be driven for interrupt vectors. Wirewrapped the same as J53.
J56	SLU	Vector bits 06 and 07. Selects how bits 06 and 07 are to be driven for interrupt vectors. Wire wrapped the same as J53.
J57	SLU	GND. Logic 0 signal for configuring vector bits. Wirewrapped to J53, J54, J55, and/or J56 when the corresponding vector bit(s) will be logical 0 for both serial line channels.
J58	SLU	+3V. Logic 1 signal for configuring vector bits. Wirewrapped to J53, J54 J55, and/or J56 when the corresponding vector bit(s) will be a logical 1 for both serial line channels.
J59	SLU	7 bits with parity/8 bits with no parity, Channel 1. Wirewrapped to ground (J65) for seven bits with parity or to +3V (J66) for eight bits with no parity.
J60	SLU	Two stop bits. Selects one or two stop bits for channel 1. Wirewrapped to ground (J65) for one stop bit or to +3V (J66) for two stop bits.
J61	SLU	Even parity. Selects odd or even parity for channel 1 when seven bits with parity (J59 wirewrapped to ground) is selected. Wirewrapped to ground (J65) for odd parity or to +3 V (J66) for even parity.
J62	SLU	7 bits parity/8 bits no parity, channel 0. Wirewrapped to ground (J65) for seven bits with parity or to +3 V (J66) for eight bits with no parity.

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Table 17-2 ▪ MXV11-A Jumper Locations (Cont.)

Pin	Option	Function
J63	SLU	2 stop bits. Selects one or two stop bits for channel 0. Wirewrapped to ground (J65) for one stop bit or to +3 V (J66) for two stop bits.
J64	SLU	Even parity. Selects odd or even parity for channel 0 when seven bits with parity (J59 wirewrapped to ground) is selected. Wirewrapped to Logic 0 (J65) for odd parity or to Logic 1 (J66) for even parity.
J65	SLU	Logic zero. Ground signal used for configuring serial line interfaces.
J66	SLU	Logic one. +3 V signal used for configuring serial line interfaces.
J67	SLU	Clock in. Clock input for baud rates, memory refresh and negative voltage generator. Wire wrapped to J68. Not a user option.
J68	SLU	Clock out. Crystal oscillator output at 19.6608 MHz. Wirewrapped to J67. Not a user option.

Configuring the RAM

The RAM can be configured to start on any 8-Kbyte boundary below 64 Kbytes. Because of this restriction, the 8-Kbyte version of the MXV11-A cannot be used for memory above 56 Kbytes. The MXV11-A can be used in 18-bit memory address systems, but it is restricted to being assigned to the memory area below 56 Kbytes.

Five wirewrap terminals, J30 through J34, select the starting address. Figure 17-2 shows the jumper configurations required to obtain the desired starting addresses.

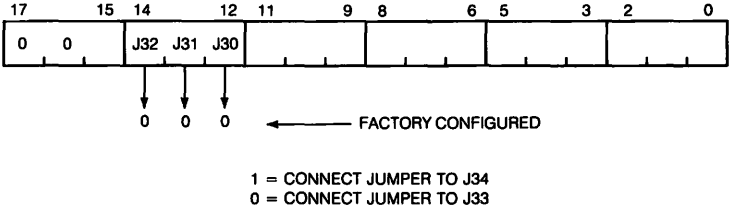


Figure 17-2 ▪ MXV11-A RAM Starting Address Selection

Configuring the ROM

Depending on the ROM type, the module's capacity is 1, 2, or 4 Kwords using a pair of 1024 × 8, 2048 × 8, or 4096 × 8-bit ROMs, respectively. The user configures jumpers on the module for the ROM type being used. The actual procedure for loading data into EPROMs, PROMs (or writing specifications for masked ROMs) will vary depending on the manufacturer, and are beyond the scope of this section. The user must refer to the manufacturer's data sheets. The user must be aware of the relationship of the EPROM, PROM, or ROM pins to the Q-bus data bits, and the relationship of the pins to the memory address bits. Refer to Figure 17-3 for ROM socket pin assignments. All ROMs used on the MXV11-A must conform to these pin assignments.

The factory configuration allows for using the MXV11-A2 bootstrap ROMs.

- CONFIGURING THE BOOTSTRAP ROM

  The ROM can be configured to operate in the I/O page to support bootstrap programs. The address area contains 256 words from 173000 to 173776 (773000 to 773776 for 18-bit systems).

  The MXV11-A is configured at the factory to allow for using the MXV11-A2 TU58 bootstrap. To reconfigure to use the disk bootstrap of the MXV11-A2, remove jumper J29 to J15 and install jumper J29 to J16.

- ROM BANK SELECTION

  If the MXV11-A sockets are used for a program ROM instead of a bootstrap ROM, the memory must be selected by a jumper connecting J20 to J21. When main ROM memory is selected, the entire 4-Kword bank is enabled. If a 1 or 2 Kword ROM is used, it will "wrap around" and give invalid data depending on how the address lines are configured when the nonexisting ROM area is addressed. Main ROM memory can be positioned in bank 0 or bank 1 only. To position the ROM in bank 0, jumper J10 to J11. To position the ROM in bank 1, jumper J9 to J11. These jumper functions are described in Table 17-3.

- CONFIGURING FOR SPECIFIC ROM TYPES

  Additional jumpers must be connected depending on the type of ROM used. Table 17-3 describes the jumper configuration when using typical ROMs such as the Intel 2716 (2K × 8) or 2732 (4K × 8) EPROMs. The user must refer to the manufacturer's data sheets when configuring jumpers for other ROM types.

  The function of wirewrap pins J29, J38, J37, and J39 are shown in the accompanying figure. These pins are to be connected as required to pins J33 through J40.

Table 17-3 ▪ MXV11-A EPROM Address Jumpers

Function	2716 ROM		2732 ROM	
	Bank 0	Bank 1	Bank 0	Bank 1
Bank Enable	J20-J21	J20-J21	J20-J21	J20-J21
Bit 09 Input	J29-J15	J29-J15	J29-J15	J29-J15
Address or Enable	J38-J36	J38-J36	J38-J36	J38-J36
Address or Enable	J37-J33	J37-J33	J37-J35	J37-J35
Address or Enable	J39-J40	J39-J40	J39-J33	J39-J34

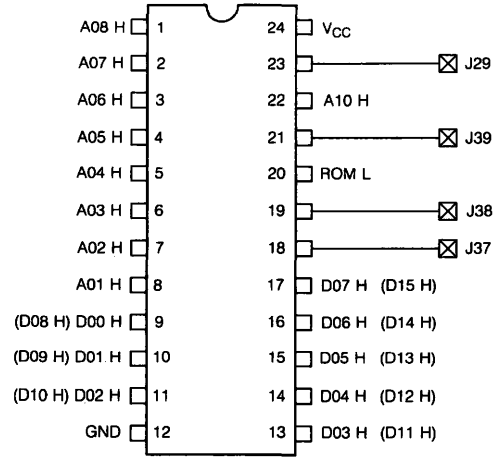


Figure 17-3 ▪ MXV11-A ROM Socket Pin Assignment

Serial Line Register Address Selection

Four device registers (RCSR, RBUF, XCSR and XBUF) are provided for each of the two serial lines. Jumpers are configured to establish separate base addresses for each serial line as shown.

- Serial port 0 may be assigned to one of four starting addresses: 176500, 176510, 176520, or 176530.
- Serial port 1 may be assigned addresses in two ranges. The first range starts at 176500 and covers the eight starting addresses from 176500 to 176570. The second range starts at 177500 and also contains eight possible starting addresses, including the standard console address, 177560. Because several other standard Digital devices use addresses in this second range, it is recommended that only the console address be used.

The format of an SLU address is shown in Figure 17-4. Note that bits <13:17> are not configured on or decoded by the MXV11-A module. These bits are decoded by the bus master module as the bank 7 select (BBS7) bus signal. This signal becomes active only when the I/O page is accessed. Bit 0 is used as the byte pointer. Bits 1 and 2 select one of the four device registers within the addressed serial line. Bits 3 and 4 are used to select one of four possible device addresses for serial line 0. Bits 3, 4, 5 and 9 are used to select the device addresses in two ranges for serial line 1 (console). Table 17-4 describes the jumper combinations to select one of four device addresses for serial line 0 (I/O).

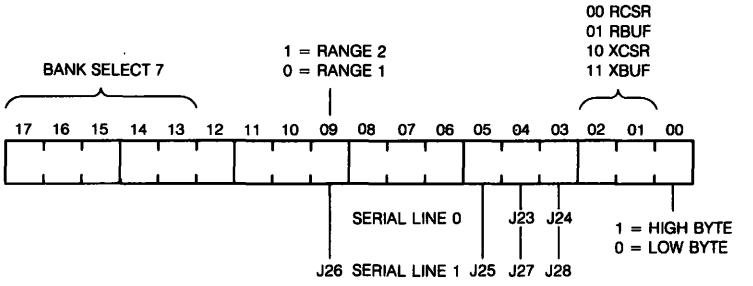
Table 17-4 ▪ MXV11-A Serial Line 0 Address Jumpers

Address (Octal)	Jumper Posts J23 to	J24 to
176500	J18 (Logic 0)	J19 (Logic 0)*
176510	J18 (Logic 0)	J12 (Logic 1)
176520	J13 (Logic 1)	J19 (Logic 0)
176530	J13 (Logic 1)	J12 (Logic 1)

Logic 1	Logic 0
J13 (A04 H)	J18 (A04 L)
J12 (A03 H)	J19 (A03 L)

* Factory configuration

Serial line 1 can have 16 possible device addresses in two ranges. Table 17-5 describes the jumper combinations to select the eight device registers available in range 1. Only one device address is used in range 2.



NOTE:
JUMPER POSTS ARE WIRED TO A HIGH ADDRESS LINE FOR A 1 AND TO A LOW ADDRESS LINE FOR A 0.

Figure 17-4 ▪ MXV11-A SLU Address Format

Table 17-5 ▪ MXV11-A Serial Line 1 Address Jumpers

Address (Octal) Range 1	Jumper Pins J26 to	J25 to	J27 to	J28 to
176500	J16	J17	J18	J19
176510	J16	J17	J18	J12
176520	J16	J17	J13	J19
176530	J16	J17	J13	J12
176540	J16	J14	J18	J19
176550	J16	J14	J18	J12
176560	J16	J14	J13	J19
176570	J16	J14	J13	J12
Range 2				
177560*	J15	J14	J13	J19

Logic 1	Logic 0
J15 (A09 H)	J16 (A09 L)
J14 (A05 H)	J17 (A05 L)
J13 (A04 H)	J18 (A04 L)
J12 (A03 H)	J19 (A03 L)

* Factory configurations use only one address in range 2 to avoid possible device conflicts. The remaining addresses are preassigned to other devices.

Interrupt Vector Selection

Two consecutive interrupt vectors (one for receive and one for transmit) are provided for each of the two serial lines. The interrupt vector format is shown in Figure 17-5. Each SLU port can be independently configured to operate in one of two ranges: 000 to 074, or 300 to 376. Table 17-6 lists the vector addresses that can be assigned to the serial lines. Note that all vector addresses in the 000 to 074 range, except 060, are reserved vector locations. The jumper-selectable bits are bits <3:7>. Bits <6:7> are wired together.

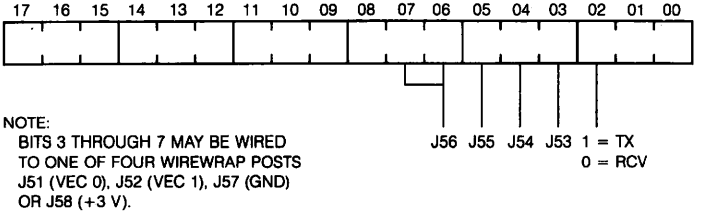


Figure 17-5 ▪ MXV11-A Interrupt Vector Format

Table 17-6 ▪ MXV11-A Serial Line Vector Addresses

Serial Line 1 (Console)		Serial line 0 (I/O)
000		300
010		310
020	Digital-reserved	320
030	Do not use	330
040		340
050		350
060	Console	360
070	Digital-reserved	370

The following example illustrates the procedure to configure the vector addresses. Assume that 60 is the address for serial line 1 (console) and 310 is the address for serial line 0 (I/O). Table 17-7 describes the relationship between the vector bases, vector address bits, and the jumper pins. The jumpers are configured using the following four rules.

- If a bit = 1 in both vector bases, it is tied to J58 (Logic 1).
- If a bit = 0 in both vector bases, it is tied to J57 (Logic 0).
- If a bit = 1 for serial line 1 and a 0 for serial line 0, it is tied to J52 (VEC 1).
- If a bit = 0 for serial line 1 and a 1 for serial line 0, it is tied to J51 (VEC 0).

Table 17-7 ▪ MXV11-A SLU Vector Addresses Example

Serial Line Number	Vector Base	Vector Address Bits 7	6	5	4	3
1 (Console)	060	0	0	1	1	0
0 (I/O)	310	1	1	0	0	1
Jumpers From		J56	J56	J55	J54	J53
To		J51	J51	J52	J52	J51

Serial Line Parameter Jumpers

Each MXV11-A serial line has three options that are selected by wirewrap jumpers. The two serial lines can be configured for one or two stop bits, seven data bits plus odd or even parity, or eight data bits without parity.

The parameters are selected by installing jumpers between the appropriate parameter pin and J65 (Logic 0) or J66 (Logic 1). Table 17-8 describes the jumper configurations required for the desired serial line parameters.

Table 17-8 ▪ MXV11-A Serial Line Parameter Jumpers

SLU 0		SLU 1		Function
From	To*	From	To*	
J62	0	J59	0	7 bits with parity
J62	1	J59	1	8 bits with no parity†
J64	0	J61	0	odd parity
J64	1	J61	1	even parity†
J63	0	J60	0	1 stop bit†
J63	1	J60	1	2 stop bits
J45	J50			38400 baud†
		J46	J48	9600 baud†

* Logic 1 = J66; Logic 0 = J65

† Factory configuration

Bootstrap Jumpers

The MXV11-A2 is a pair of 24-pin ROM chips containing two bootstrap programs. Choosing which bootstrap to use is done with a wirewrap jumper. To bootstrap from the TU58, wire the jumper from J29 to J15. To bootstrap from disk, wire the jumper from J29 to J16. To install the option, place the ROM marked 039D1 in socket XE57, and place 040D1 in socket XE67.

- MXV11 TU58 BOOTSTRAP

  The MXV11 TU58 bootstrap is a 256-word diagnostic and bootstrap program for Q-bus systems using the TU58 DECtape II tape cartridge drives. On power up, the bootstrap sizes and tests memory (up to 60 Kbytes), and then bootstraps the TU58 cartridge disk.

  The TU58 bootstrap contains a feature unique among Digital-standard bootstraps. If the first word read contains a value of 260_8 (rather than the standard 240_8), the bootstrap ROM knows that it must do a "standalone" program load, rather than a normal system load. The bootstrap ROM also provides a MACRO or FORTRAN-callable entry point, which can be used to "chain" from one standalone program to another.

- MXV11 DISK BOOTSTRAP

  This is a 256-word bootstrap program designed to handle most of the disks that are available for the Q-bus. It automatically searches for controllers for the various disks (in a predefined order) and bootstraps the first such device that is found and is operable.

Baud Rate Jumpers

Each serial line can be configured for internal baud rates from 150 to 38400 baud. Both transmitter and receiver for a given serial line operate at the same baud rate; split baud operation is not provided. One baud rate clock input wirewrap pin is provided for each serial line. J46 is the clock input pin for serial line 1 and J45 is the clock input pin for serial line 0. The baud rate generator outputs are applied to jumper pins J41 through J44 and J47 through J50. The baud rates available at these pins are described in Table 17-9. Configure baud rates (except 110 baud) by connecting a jumper from the desired baud rate generator output pin to the serial line clock input pin.

Table 17-9 ▪ MXV11-A Baud Rate Jumpers

From	To	Function
J45		SLU0
J46		SLU1
	J41	150 baud clock
	J43	300 baud clock
	J42	1200 baud clock
	J44	2400 baud clock
	J47	4800 baud clock
	J48	9600 baud clock
	J49	19200 baud clock
	J50	38400 baud clock
		External baud clock

Halt/Reboot on Break

A break signal is a continuous spacing condition on the serial data line that occurs either when an operator presses the BREAK key on the associated terminal or when the line is opened. The MXV11-A detects this condition as a framing error. Serial line 1 (console) may be configured for the break responses described in Table 17-10.

Table 17-10 ▪ MXV11-A Serial Line 1 Break Response Jumpers

Break Response, Operation	Jumper Posts From	To
Reboot	J6	J5
Halt*	J6	J7
No Response	No Jumper installed	

* Factory configuration

60-Hz Clock

A 60-Hz clock is derived from the crystal on the MXV11-A. It can be jumpered to the BEVNT line to provide the equivalent of a linetime clock for a system that otherwise does not have one. In the factory configuration, this signal is disconnected. It should not be connected if there is any other source in the system, such as when there is more than one MXV11-A module in a system.

This clock can be used with the BDV11 clock status and control register feature. The BDV11 can still be used to turn the clock off under program control, since it accomplishes this by pulling the BEVNT line to ground on the bus. If this control feature is to be used, the MXV11-A should be installed in the same expansion box as the BDV11.

To select this option, jumper J3 to J4 or wire backplane pin AF1 to BR1.

▪ Cables and Connectors

Table 17-11 lists the part numbers, applications and lengths of cabling and options available for the MXV11-A module. Digital offers the BC20M-50 cable for MXV11-A to DLVJ1 operation. Because longer cables usually require routing without connectors attached, it is recommended the user make cables for lengths greater than 15 meters (50 feet). Cable material must adhere to EIA RS-423 specifications. The connectors on the MXV11-A module are AMP-87272-8 (2 × 5 pins on 0.1-inch centers). These connectors can mate with a wide variety of low-cost cables including 10-conductor flat cable. Note that pin 1 supplies the SLU clock TTL output, when the module's internal clock is selected, but is used as the SLU clock input when an external baud rate is desired. Pin 10 supplies + 12 Vdc power for use by external options. Cable retention in the module is provided by locking clip contacts (AMP PN87124-1).

Table 17-11 ▪ Cables Available for the MXV11-A

Cable	Length	Application
BC21B-05	1.5 m (5 ft)	EIA RS-232C modem cable to interface with modems and acoustic couplers (2 × 5 pin amp female to RS-232C male)
BC20N-05	1.5 m (5 ft)	EIA RS-232C null modem cable to interface directly with a local EIA RS-232C terminal (2 × 5 pin amp female to RS-232C female)
BC20M-50	15 m (50 ft)	EIA RS-422 or RS-423 cable for high-speed transmission (19200 baud) (2 × 5 pin amp female to 2 × 5 amp female)
BC05D-10	3 m (10 ft)	Extension cable used in conjunction with BC21B-05
BC05D-25	7.6 m (25 ft)	Extension cable used in conjunction with BC21B-05
BC03M-25	7.6 m (25 ft)	Null modem extension cable used in conjunction with BC21B-05

Note

Strapped logic levels are provided on data terminal ready (DTR) and request to send (RTS) to all operation of modems with manual provisions (such as Bell 103A data set with 804B auxiliary set).

The MXV11-A can operate with several peripheral device cables and options for flexibility when configuring systems.

Chapter 18 • MXV11-B Multifunction Option Module

The MXV11-B is a dual-height, multifunction option module for use in 16-, 18-, or 22-bit Q-bus systems.

• Specifications

Identification	M7195
Size	Dual
Bus Loads	
ac	2.3
dc	0.5
Power Requirements	+5 V ±5%, 3.45 A (typical) +12 V ±5%, 60mA (typical)

Power dissipation is as follows:

Voltage	**Typical**	**Maximum**
No battery backup		
+5 V	17.25 W	24.57 W
+12 V	0.67 W	0.71 W
Battery backup configuration		
+5 V	12.90 W	1.95 W
+5 VB	4.35 W	8.60 W
+12 V	0.67 W	0.71 W
Data Retention Mode (VCC = 0 V, +12 V supply = 0)		
+5 VB	4.35 W	5.54 W

Nonstandard Environmental Specifications	
Altitude	
Storage	Up to 9 km
Operating	Up to 3 km Lower the maximum operating temperature by 1.8 Celsius degrees (3.24 Fahrenheit degrees) for each 1,000 m (3,280 ft) above sea level

▪ Related Documentation

Document Title	Order Number
MXV11-B Multifunction Option Module User's Guide	EK-MXV1B-UG
MXV11-B2 ROM Set User Guide	EK-MXVB2-UG

▪ Configuration

The user can configure the MXV11-B features by using the jumpers provided on the board. The jumpers used with this module are of two types—push-on connectors and wirewrap. The push-on connectors are associated with those groupings of pins with one pin open. These connectors allow two adjacent pins to be jumpered. If the jumper relating to a function is to remain disconnected, one end of the push-on connector is placed on the pin associated with that function, and the other end of the connector is placed on the open pin. The open pin is not connected to ground, +5 V, or any logic function, and merely serves as a holder for the connector. If a push-on connector is missing, a wirewrap jumper can be substituted. When installing jumpers, arrange the wire runs so that no more than two wires are on each pin and there is no level jumping between pins.

Figure 18-1 shows the jumper locations on the MXV11-B.

MXV11-B modules shipped from the factory have a 0-ohm resistor supplying the MOS RAMs with nonbattery backup power of +5 V, eight push-on connectors in the open position, and no wirewrap jumpers connected.

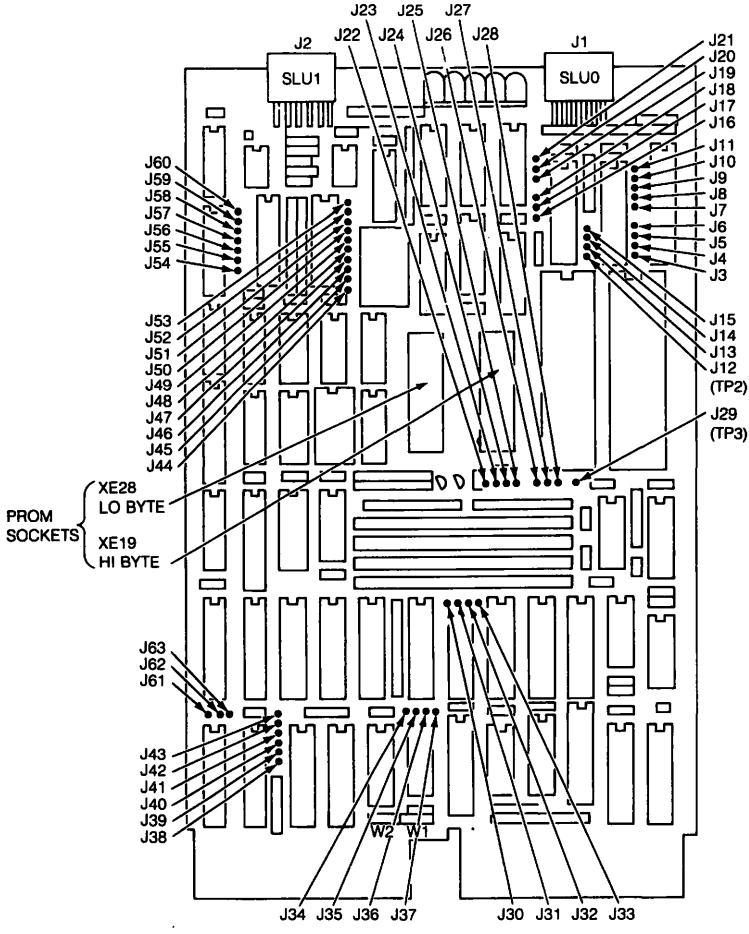


Figure 18-1 ▪ MXV11-B Jumper Locations

Configuring the RAM

The MXV11-B read/write memory consists of 128 Kbytes of dynamic MOS RAM without parity. The RAM can be configured to start on any 4-Kbyte boundary up to 252 Kwords. Note, however, to configure the RAM above 64 Kwords, the MXV11-B must be installed in a 22-bit Q-bus backplane and the module must be configured as a 22-bit system, with a wirewrap jumper installed between pins J37 and J36 (SM/LG to GND).

Seven wirewrap pins, J54 through J60, are used to select the RAM starting address. Table 18-1 shows the jumper configurations required to obtain the desired start address.

Table 18-1 ▪ MXV11-B RAM Starting Addresses

	Jumper Connection to GND (J57)					
Start Address	**AJ18 (J60)**	**AJ17 (J59)**	**AJ16 (J58)**	**AJ15 (J56)**	**AJ14 (J55)**	**AJ13 (J54)**
0 Kw	R	R	R	R	R	R
4 Kw	R	R	R	R	R	I
8 Kw	R	R	R	R	I	R
12 Kw	R	R	R	R	I	I
16 Kw	R	R	R	I	R	R
20 Kw	R	R	R	I	R	I
24 Kw	R	R	R	I	I	R
28 Kw	R	R	R	I	I	I
32 Kw	R	R	I	R	R	R
36 Kw	R	R	I	R	R	I
40 Kw	R	R	I	R	I	R
44 Kw	R	R	I	R	I	I
48 Kw	R	R	I	I	R	R
52 Kw	R	R	I	I	R	I
56 Kw	R	R	I	I	I	R
60 Kw	R	R	I	I	I	I
64 Kw*	R	I	R	R	R	R
68 Kw*	R	I	R	R	R	I
72 Kw*	R	I	R	R	I	R

(continued on next page)

Table 18-1 ▪ MXV11-B RAM Starting Addresses (Cont.)

Start Address	Jumper Connection to GND (J57) AJ18 (J60)	AJ17 (J59)	AJ16 (J58)	AJ15 (J56)	AJ14 (J55)	AJ13 (J54)
76 Kw*	R	I	R	R	I	I
80 Kw*	R	I	R	I	R	R
84 Kw*	R	I	R	I	R	I
88 Kw*	R	I	R	I	I	R
92 Kw*	R	I	R	I	I	I
96 Kw*	R	I	I	R	R	R
100 Kw*	R	I	I	R	R	I
104 Kw*	R	I	I	R	I	R
108 Kw*	R	I	I	R	I	I
112 Kw*	R	I	I	I	R	R
116 Kw*	R	I	I	I	R	I
120 Kw*	R	I	I	I	I	R
124 Kw*	R	I	I	I	I	I
128 Kw*	I	R	R	R	R	R
132 Kw*	I	R	R	R	R	I
136 Kw*	I	R	R	R	I	R
140 Kw*	I	R	R	R	I	I
144 Kw*	I	R	R	I	R	R
148 Kw*	I	R	R	I	R	I
152 Kw*	I	R	R	I	I	R
156 Kw*	I	R	R	I	I	I
160 Kw*	I	R	I	R	R	R
164 Kw*	I	R	I	R	R	I
168 Kw*	I	R	I	R	I	R
172 Kw*	I	R	I	R	I	I
176 Kw*	I	R	I	I	R	R
180 Kw*	I	R	I	I	R	I

(continued on next page)

Table 18-1 ▪ MXV11-B RAM Starting Addresses (Cont.)

Start Address	Jumper Connection to GND (J57) AJ18 (J60)	AJ17 (J59)	AJ16 (J58)	AJ15 (J56)	AJ14 (J55)	AJ13 (J54)
184 Kw*	I	R	I	I	I	R
188 Kw*	I	R	I	I	I	I
192 Kw*	I	I	R	R	R	R
196 Kw*	I	I	R	R	R	I
200 Kw*	I	I	R	R	I	R
204 Kw*	I	I	R	R	I	I
208 Kw*	I	I	R	I	R	R
212 Kw*	I	I	R	I	R	I
216 Kw*	I	I	R	I	I	R
220 Kw*	I	I	R	I	I	I
224 Kw*	I	I	I	R	R	R
228 Kw*	I	I	I	R	R	I
232 Kw*	I	I	I	R	I	R
236 Kw*	I	I	I	R	I	I
240 Kw*	I	I	I	I	R	R
244 Kw*	I	I	I	I	R	I
248 Kw*	I	I	I	I	I	R
252 Kw*	I	I	I	I	I	I

R = jumper removed; I = jumper installed, (Where multiple connections are made, they are daisychained.)

* To use addresses above 64 Kwords, a wirewrap jumper must be installed between pins J37 and J36 (SM/LG to GND).

Note

Be careful while configuring the MXV11-B RAM when ROM is used in the USER ROM address space. USER ROM address space is defined as bus addresses 0 to 16 Kwords, (00000-100000) on 4-Kword boundaries. The RAM start address must be higher than the last location of the ROM or dual responses from both the RAM and ROM will occur.

- BATTERY BACKUP

  MXV11-B modules shipped from the factory have a 0-ohm resistor (W2) installed to supply the RAM with nonbattery backup power of +5 V. In this configuration, the memory and refresh logic are powered from the normal bus backplane power. Removing W2 and installing W1 removes normal system power from the RAM memory circuits, permitting the user to install a separate battery source. Figure 18-1 shows the locations of the W1 and W2 0-ohm resistors.

Note

Digital systems do not supply battery backup voltages to the backplane, and battery backup is not supported by Digital.

ROM Configurations

The MXV11-B contains two 28-pin sockets to house ROMs containing bootstrap code, diagnostic code, or user routines. Wirewrap pins allow the insertion of 2K × 8, 4K × 8, or 8K × 8 PROMs/ROMs in these sockets. The PROM/ROM devices used can be ultraviolet erasable PROMs, fusible link PROMs, or masked ROMs.

The 2K × 8 and 4K × 8 PROMs each contain 24 pins; the 8K × 8 PROM contains 28 pins. Figure 18-2 shows the Intel configuration for each size PROM. Use this configuration or equivalent. For example, the Intel 2716 PROM chip is 2K × 8 UVPROM. A similar PROM chip, compatible with the 2716, can be used as a 2K × 8 PROM.

Note

The MXV11-B supports Intel 2716, 2732, 2732A, and 2764 UVPROMS.

When installing a 2K × 8 or 4K × 8 PROM in the 28-pin PROM sockets (XE28 for low byte or XE19 for high byte), the 24-pin PROM must be installed in the 28-pin socket with the notch on top, pin side down, and bottom justified. This means that pin 1 of the PROM chip must be inserted in pin 3 of the PROM socket (Figure 18-3).

For the 28-pin PROM chip, pin 1 of the chip is plugged into pin 1 of the socket with the notch on the top and pin side down.

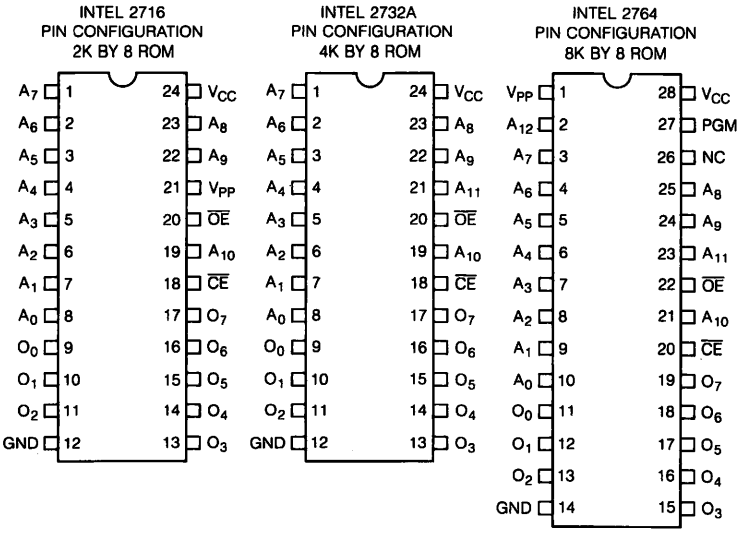


Figure 18-2 ▪ PROM Chips

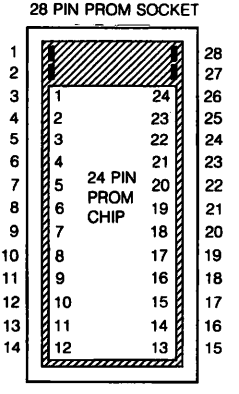


Figure 18-3 ▪ Insertion of 24-Pin PROM Chips

- PROM SIZE JUMPERS

Jumper configurations for the various PROM sizes are shown in Table 18-2. Additional jumpers may be required depending on the selected access and addressing modes, as discussed below.

Table 18-2 • MXV11-B PROM Size Jumpers

PROM Size	Jumper Connection to GND (J51) PROM 2 (J50)	PROM 1 (J49)
No ROMs	R	R
2K×8	R	I
4K×8	I	R
8K×8*	I	I

I = jumper installed; R = jumper removed

* If the MXV11-B2 Boot Diagnostic ROM set is installed, install PROM 2 to PROM 1 to GND (J50 to J49 to J51).

- BOOT VERSUS USER MODE

The 28-pin sockets can house user PROMs or the MXV11-B2 ROM set. If user PROMs are installed, they can be located in either the user area of main memory (000000 through 077776) or in the bootstrap area (a 256-word block from 773000 to 773776). If the MXV11-B2 ROM set is installed, it can reside only in the bootstrap area. When installing a ROM device, the user must configure push-on connector W9 in accordance with the location of the device, as shown in Table 18-3.

Table 18-3 • MXV11-B PROM Mode Jumpers

	W9 Connect		W5 Connect		Wire-Wrap Connect	
Mode	J44-J45	J45-J46	J17-J18	J16-J17	J34-J35	J34-J36
User	R	I	I	R	I	R
Boot/direct	I	R	I	R	R	I
Boot/page	I	R	R	I	I	R

J44 = BOOT L/PROM H J16 = GND J34 = DIR MODE BOOT
J45 = GND J17 = PG L/DIR H J35 = OPEN
J46 = OPEN J18 = OPEN J36 = GND

I = jumper installed; R = jumper removed

- PROM ADDRESSING

When ROM devices are installed in the user area, they are addressed directly, with starting addresses on any 4 K-word boundary under 16 Kwords. If that word bank is selected, only the space containing ROM is enabled, preventing "wrap-around." Any read request to ROM where no ROM exists results in no response from the module. Table 18-4 shows the jumper configurations for permissible ROM starting addresses.

Table 18-4 ▪ MXV11-B PROM Starting Address Jumpers

User PROM Start Address	Jumper Connection to GND (J51) BSK2 (J53)	BSK1 (J52)
000000	R	R
020000	R	I
040000	I	R
060000	I	I

I = jumper installed; R = jumper removed

Note

These addresses are for user-supplied ROMs only. Jumpers J44 to J45 (BOOT L/PROM H to GND) and J17 to J16 (PG L/DIR H to GND) must be removed.

Devices that reside in the boot area can be accessed directly (as described above) or indirectly, using a window-mapping technique.

The ROM in the MXV11-B uses two windows in the I/O page. Each window points to one of 32 256-word blocks in ROM. This method of pointing prevents the whole I/O page from containing ROM code. Using this technique, any 256-word block of ROM can be transferred to the appropriate window area in the I/O page. This window map is used when the MXV11-B is conigured for bootstrap mode. Table 18-5 shows the window addresses used in 16-, 18-, and 22-bit Q-bus systems.

A page control register (PCR) in the MXV11-B is used for the mapping feature. The PCR is a read/write register that supports DATIOB and DATOB operations. It resides at location 177520 in the I/O page and is two bytes in length. Each of the window maps is pointed to by a five-bit address in the PCR (see Figure 18-4).

Table 18-5 ▪ MXV11-B ROM Window Addresses

Q-bus	Window 1 Addresses	Window 0 Addresses
16-bit	165000-165777	173000-173377
18-bit	765000-765777	773000-773377
22-bit	17765000-17765777	17773000-17773377

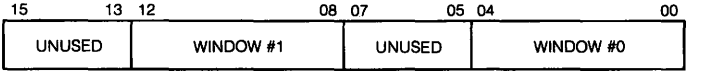


Figure 18-4 ▪ MXV11-B Page Control Register

Table 18-3 shows the jumper configurations for the various combinations of user/boot and direct/page modes. Additional required sizing jumpers are shown in Table 18-6.

Table 18-6 ▪ Additional MXV11-B Size Jumpers for ROM Devices

W6 Connection	Description
J20 to J21 (NA12H to +5V)	Specifies 2K × 8 user UVROMs (2716) installed and direct mode addressing
J20 to J19 (NA12H to BA12H)	Specifies 4K × 8 or 8K × 8 user- supplied ROM in direct mode addressing

Note

In some cases none of these jumpers (J19, J20 or J21) should be connected. In these cases, the push-on connector must be completely removed or must be connected to one of the outside pins to hold the connector. There is no open pin associated with these jumpers. For example, if 2K non-UV PROMs or the MXV11-B2 ROM is to be installed, these jumpers are all disconnected.

Configuring the Serial Line Units

Data between the CPU and a peripheral device is serialized by an asynchronous serial line unit (SLU). The MXV11-B uses two such lines, SLU 0 and SLU 1. Each SLU contains a DLART which is a universal asynchronous receiver/transmitter (UART) that has been modified by Digital. SLU 1 can be used as a console terminal port but SLU 0 cannot.

The SLUs transmit and receive EIA-423 or RS-232 signal levels at 300, 1200, 9600, or 38400 baud.

- SLU REGISTER ADDRESSING

Four device registers are provided for each of the two serial line units. These four registers are as follows:

RCSR	Receiver control/status register
RBUF	Receiver data buffer
XCSR	Transmitter control/status register
XBUF	Transmitter data buffer

The starting address (within the I/O page) of the SLU 0 register set is jumper-selected to any of eight locations in the address range of 776500 to 776570, as shown in Table 18-7. Except when console mode is enabled, the SLU 1 register set is assigned automatically the next starting address after that selected for SLU 0. When console mode is enabled, assigning SLU 1 as the console port, the starting address of SLU 1 is assumed to be 777560.

Table 18-7 ▪ MXV11-B SLU Starting Address Jumpers

Starting Address		Jumper Connection to GND (J31)		
SLU 0	SLU 1*	SLUA3 (J30)	SLUA2 (J32)	SLUA1 (J33)
776500	776510	R	R	R
776510	776520	R	R	I
776520	776530	R	I	R
776530	776540	R	I	I
776540	776550	I	R	R
776550	776560	I	R	I
776560	776570	I	I	R
776570	776600	I	I	I

I = jumper installed; R = jumper removed

* If the J62 to J61 jumper is installed (console enabled), the SLU 1 address is fixed at the standard console address of 777560 and this column does not apply.

- INTERRUPT VECTOR SELECTION

Two consecutive interrupt vectors (one for the transmitter and one for the receiver) are provided for each of the two serial line units. The starting vector address for SLU 0 is jumper-selectable in the address range of 010-376, as shown in Table 18-8. Except when console mode is enabled, the vector address for SLU 1 is assigned automatically to the next address after those selected for SLU 0. When console mode is enabled, assigning SLU 1 as the console terminal port, SLU 1 is assumed to have a vector address of 60 for the transmitter and 64 for the receiver.

Table 18-8 ▪ MXV11-B SLU Vector Address Jumpers

Vector Address		Jumper Connection to GND (J40)				
SLU 0	SLU 1*	JU2 (J39)	JU1 (J38)	JL3 (J43)	JL2 (J42)	JL1 (J41)
300	310	R	R	R	R	R
010	020	R	R	R	R	I
020	030	R	R	R	I	R
030	040	R	R	R	I	I
040	050	R	R	I	R	R
050	060	R	R	I	R	I
060	070	R	R	I	I	R
070	100	R	R	I	I	I
100	110	R	I	R	R	R
110	120	R	I	R	R	I
120	130	R	I	R	I	R
130	140	R	I	R	I	I
140	150	R	I	I	R	R
150	160	R	I	I	R	I
160	170	R	I	I	I	R
170	200	R	I	I	I	I
200	210	I	R	R	R	R
210	220	I	R	R	R	I
220	230	I	R	R	I	R
230	240	I	R	R	I	I
240	250	I	R	I	R	R
250	260	I	R	I	R	I
260	270	I	R	I	I	R
270	300	I	R	I	I	I
300	310	I	I	R	R	R
310	320	I	I	R	R	I

(continued on next page)

Table 18-8 ▪ MXV11-B SLU Vector Address Jumpers (Cont.)

Vector Address		Jumper Connection to GND (J40)				
SLU 0	SLU 1*	JU2 (J39)	JU1 (J38)	JL3 (J43)	JL2 (J42)	JL1 (J41)
320	330	I	I	R	I	R
330	340	I	I	R	I	I
340	350	I	I	I	R	R
350	360	I	I	I	R	I
360	370	I	I	I	I	R
370	Undefined	I	I	I	I	I

R = jumper removed; I = jumper installed. (Where multiple connections are made, they are daisychained.)

* If jumper J62 to J61 is installed (console enabled), SLU 1 vector address is fixed at 60 and this column does not apply.

- CONSOLE MODE

The MXV11-B can be jumpered to interface to the system console. This is done by installing push-on connector W8 between pins J62 (GND) and J61 (OPEN). With console mode enabled in this fashion, the console terminal must be connected to SLU 1. The register set starting address is then fixed at 777560 and the vector address is fixed at 60.

When console mode is disabled by installing W8 between pins J63 (CONSOLE) and J62 (GND), the following features cannot be selected:

- Halt on break condition from SLU 1 (never available with SLU 0)
- Reboot on break condition from SLU 1 (never available with SLU 0)
- Console address (773000)
- MXV11-B2 ROMs or user ROMs addressed at 773000 and 765000
- Software control of the LTC (BEVNT) (address 777546 does not exist)
- Page control register (address 777520 does not exist)
- Diagnostic display register (address 777524 does not exist)

- HALT/REBOOT ON BREAK

  A break signal is a continuous spacing condition on the serial data line that occurs either when an operator presses the break key on the associated terminal or when the line is opened. The MXV11-B detects this condition as a framing error. Serial line unit 1 can be configured to respond to such an error in one of three ways, as shown in Table 18-9.

  If the Halt response is selected, a break character halts program execution and the processor enters the console ODT microcode. If the Boot response is selected, a break character initializes the system, then restarts the processor with the selected powerup mode.

Table 18-9 ▪ MXV11-B SLU 1 Break Response Jumpers

Response	W3 Connection to GND (J4)
Halt	J3 (HALT)
Reboot	J5 (RBOOT)
No response	J6 (OPEN)

Note

To select either the halt or reboot response, console mode must be enabled.

- BAUD RATE SELECTION

  The baud rates for each SLU can be software-programmable or can be jumper-selected to one of four baud rates (300, 1200, 9600, and 38.4K). The baud rates are the same for both transmit and receive.

  To enable software-programmable baud rates, push-on connector W4 must be installed between pins J14 (SOFT EN) and J13 (GND). When W4 is installed between pins J14 (SOFT EN) and J15 (OPEN), the SLU baud rates are selected using wirewrap pins J7 to J11, as shown in Table 18-10.

Table 18-10 ▪ MXV11-B SLU Baud Rate Jumpers

	Jumper Connection to GND (J9)			
	SLU 0		SLU 1	
Baud Rate	J10 (J0B)	J11 (J0A)	J8 (J1A)	J7 (J1B)
300	R	R	R	R
1200	R	I	R	I
9600	I	R	I	R
38400	I	I	I	I

I = jumper installed; R = jumper removed

Note

SOFT EN to GND jumper (J14 to J13) must be removed; otherwise, these jumpers have no effect. If the SOFT EN to GND jumper is installed and PBRE (bit 1) is set in the transmitter control/status register, baud rates are software controlled.

Linetime Clock

The linetime clock (LTC) is a one-bit register (bit 06). When bit 06 is set, the clamp is removed from BEVNT, which enables the LTC. The LTC is derived from a 20-MHz crystal oscillator on the MXV11-B board. The crystal oscillator is also used for memory refresh.

Note

If the LTC feature of the MXV11-B module is used, the module and the processor should be mounted in the same backplane.

A frequency divider connected to the oscillator provides a frequency of 617.4 kHz, which is applied to the DLARTs of SLU 1 and SLU 0. The SLU 1 DLART provides selectable linetime clock frequencies of 50, 60, or 800 Hz. The desired frequency is selected by wirewrapping the frequency to a common wirewrap pin, as shown in Table 18-11.

Table 18-11 ▪ MXV11-B Linetime Clock Frequency Jumpers

Jumper Connection to LTC COMM (J22)	Frequency
J23	50 Hz
J24	60 Hz
J25	800 Hz

The LTC can be enabled or disabled from driving the BEVNT line on the Q-bus by appropriate wirewrap. When push-on connector W7 is installed between pins J27 and J28 (LTC EN IN and LTC EN OUT), the LTC can be software-controlled, enabling control of BEVNT on the bus via bit 06 of the LTC register. When bit 06 of the LTC register is 0, BEVNT will be asserted constantly low. This inhibits LTC interrupts in the system. Note that to address the LTC register (777546), the MXV11-B must be in boot mode (BOOT L/PROM H to GND inserted) and SLU 1 must be the console port (CONSOLE to GND removed).

When push-on connector W7 is installed between pins J27 and J26 (LTC EN IN to OPEN), bit 06 of the LTC register is prevented from controlling the BEVNT line.

Note

There should be only one source driver on the BEVNT line in any system. In most systems, the system power supply supplies the BEVNT signal. This source must be disabled if the MXV11-B is used to drive the line clock.

Master Clock

A wirewrap jumper is installed between pins J47 and J48 (CLOCK IN and CLOCK OUT). This is the master clock and provides onboard refresh and the charge pump to generate -12V. Do not remove this jumper.

▪ MXV11-B2 ROM Set

The MXV11-B2 bootstrap/diagnostic ROM set is a plug-in option for the MXV11-B multifunction module and the MRV11-D universal PROM module. The MXV11-B2 performs bootstrap program loading from mass storage devices and also performs diagnostic tests on the processor, memory and I/O devices during powerup or when manually invoked.

The bootstrap function is automatic at powerup. An operator, however, can enter manual mode and use the console terminal to boot devices at nonstandard I/O page addresses, select a secondary system device, or invoke a diagnostic utility.

Note

Do not use the MXV11-B2 if you are using the battery backup option because the MXV11-B2 will alter the contents of memory. Select a CPU powerup option other than the MXV11-B2. Refer to the specific CPU manual.

The MXV11-B2 can support turnkey operation, so operator intervention is not required to initiate the bootstrap function. Some of the MXV11-B2 features are as follows:

- Loads and runs special stand-alone RT-11 volumes
- Permits configuring a system to downline load via a DECnet link without operator intervention
- Supports all system devices currently available on the Q-bus
- Includes full 22-bit mapping support

Refer to the section above on configuring the ROM for information concerning the installation and use of the MXV11-B2 ROM set.

▪ Cables and Connectors

Table 18-12 lists the part numbers, applications, and lengths of cabling and options available for the MXV11-B module. Digital offers the BC20M-50 cable for MXV11-B to DLVJ1 operation. Because longer cables usually require routing without connectors attached, it is recommended the user make cables for lengths greater than 15 meters (50 feet). Cable material must adhere to EIA RS-423 specifications. The connectors on the MXV11-B module are AMP-87272-8 (2 × 5 pin on 0.1-inch centers). These connectors can mate with a wide variety of low-cost cables including 10-conductor flat cable. Note that a pin 1 baud rate clock is not used on this module.

Pin 10 carries + 12 Vdc power for use by the external options. Cable retention in the module is provided by locking clip contacts (AMP PN87124-1).

Table 18-12 ▪ Cables Available for the MXV11-B

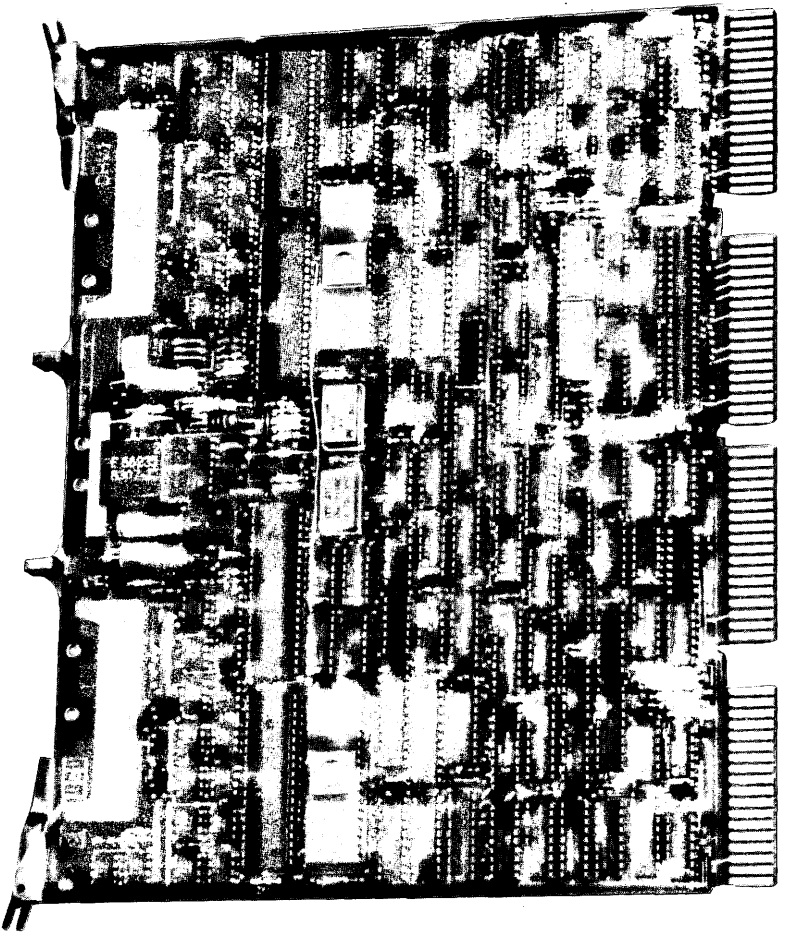
Cable	Length	Application
BC21B-05	1.5 m (5 ft)	EIA RS-232C modem cable to interface with modems and acoustic couplers (2 × 5 pin amp female to RS-232C male)
BC20N-05	1.5 m (5 ft)	EIA RS-232C null modem cable to directly interface with a local EIA RS-232C terminal (2 × 5 pin amp female to RS-232C female)
BC20M-50	15 m (50 ft)	EIA RS-422 or RS-423 cable for high-speed transmission (19200 baud) (2 × 5 pin amp female to 2 × 5 amp female)
BC05D-10	3 m (10 ft)	Extension cable used in conjunction with BC21B-05
BC05D-25	7.6 m (25 ft)	Extension cable used in conjunction with BC21B-05
BC03M-25	7.6 m (25 ft)	Null modem extension cable used in conjunction with BC21B-05

Note

Strapped logic levels are provided on data terminal ready (DTR) and request to send (RTS) to all operation of modems with manual provisions (such as Bell 103A data set with 804B auxiliary set).

The MXV11-B can operate with several peripheral device cables and options for flexibility when configuring systems.

Part V • Asynchronous Communications Interfaces



Chapter 19 • Introduction to Asynchronous Communications Interfaces

The Q-bus asynchronous communications interfaces connect the Q-bus with any of several standard types of serial communications lines. They accept serial data from an external device and assemble it into parallel data for transfer to the bus. They also accept parallel data from the Q-bus, convert it to serial data, and transfer it back to the external device.

All Q-bus asynchronous interfaces provide full-duplex local and remote interconnection between Q-bus systems and EIA RS-232C terminals and other devices. They are also compatible with Digital's family of modems and with Bell 100 and 200 series modems and their equivalents. Additional features available on selected interfaces are listed below. Table 19-1 provides a summary of the available Q-bus asynchronous interfaces and their features.

- Compatibility with EIA RS-423A and RS-422 devices.
- 20 mA current loop operation.
- Generation of reader-run signals for use with ASR-type terminals.
- Full or limited modem control.
- Split speed operation providing different baud rates for input and output.
- Provisions for user-supplied external clock input for baud rate control.
- Direct memory access data transfers.
- SILO buffering of received data.
- Independent (nonmultiplexed) multiple channels.
- Support of 16-, 18-, or 22-bit Q-bus addressing.

Table 19-1 ▪ Q-bus Asynchronous Interface Comparison/Summary Chart

Feature	DHV11	DLV11	DLVE1	DLVJ1	DZQ11	DZV11	KMV11*
Number of lines	8	1	1	4	4	4	1
Multiplexed	yes	n/a	n/a	no	yes	yes	n/a
Bus addressing	16, 18, 22	16, 18, 22	16, 18, 22	16, 18, 22	16, 18, 22	16, 18, 22	16, 18, 22
Interface							
EIA RS-232C	yes	yes	yes	yes	yes	yes	yes
EIA RS-422	yes†	no	no	yes	no	no	yes
EIA RS-423A	yes	no	no	yes	yes	no	yes
20 mA current	no	yes	no	no	no	no	no
Modem control	lim	lim	full	lim	lim	lim	full
Reader-run	no	yes	yes	no	no	no	no
Baud rates							
Program-mable	yes	no	yes	no	yes	yes	yes
Jumper-select	yes	yes	yes	yes	no	no	no
Split speed	yes	no	yes	no	no	yes	yes
External	no	yes	yes	yes	no	no	yes
DMA operation	yes	no	no	no	no	no	yes
Data buffering	yes	no	no	no	yes	yes	yes

* The KMV11 is a single-line programmable communications controller that utilizes a Micro/T11 processor to perform user-defined communications functions. It can be programmed for either synchronous or asynchronous operations.

† By means of cables and connectors not supported by Digital.

Table 19-2 ▪ Q-bus Asynchronous Interface Baud Rate Chart

Baud Rate	DHV11	DLV11	DLVE1	DLVJ1	DZQ11	DZV11	KMV11*
50	X	X	X		X	X	
75	X	X	X		X	X	
110	X	X	X		X	X	
134.5	X	X	X		X	X	
150	X	X	X	X	X	X	
200		X					
300	X	X	X	X	X	X	
600	X	X	X	X	X	X	
1200	X	X	X	X	X	X	X
1800	X	X	X		X	X	
2000	X	X	X		X	X	
2400	X	X	X	X	X	X	X
3600			X		X	X	
4800	X	X	X	X	X	X	X
7200	X		X		X	X	
9600	X	X	X	X	X	X	X
19200	X		X	X		X	X
19800†					X		
38400†	X			X		X	
External		X	X	X			X

* These baud rates are applicable when the KMV11 is programmed in asynchronous mode. In synchronous mode, the KMV11 can operate at speed up to 64000 baud.

† These baud rates are not usually supported by Digital software.

Chapter 20 • DHV11 Asynchronous Multiplexer

The DHV11 option is an asynchronous multiplexer that provides eight full-duplex asynchronous serial data channels for Q-bus systems.

• Specifications

Identification	M3104
Size	Quad
Power Requirements	+5 Vdc ±5%, 4.3 A (typical), 6.6 A (maximum) +12 Vdc ±3%, 480 mA (typical), 980 mA (maximum)

Note

Negative 12 Vdc is generated by a Switch Mode Power Supply (SMPS) circuit on the DHV11. It has the following specification:

−11.85 Vdc ±7.25% at 400 mA (maximum)
Output ripple is 200 mV peak to peak at 33.3 kHz

Bus Loads	
ac	2.9
dc	1.0
Performance	
Data Rates (per channel)	50 to 38,400 bits/second
Maximum throughput	
Per channel (transmit)	1,000 characters/second in single-character transfer mode; 2,000 characters/second in DMA mode
Per channel (receive)	4,000 characters/second
Total (8 channels)	15,000 characters/second
Interface	EIA standard RS-423A, RS-232C
Nonstandard Environmental Specifications	
Storage Temperature	0°C to 66°C (32°F to 151°F)

▪ Related Documentation

Document Title	Order Number
Communications Mini-Reference Guide	EK-CMINI-RM
DHV11 Field Maintenance Print Set	MP-01783-00
DHV11 Maintenance Card	EK-DHV11-MC
DHV11 Technical Manual	EK-DHV11-TM
DHV11 Diagnostic Documentation Kit	ZJ362-RZ

▪ Configuration

The physical layout of the DHV11 module is shown in Figure 20-1. The module is connected to the Q-bus via connectors A and B. J1 and J2 are connected to the communications lines via BC05L-xx cables and H3173-A distribution panels. (The H3173-A distribution panels provide noise filtering and static discharge protection on the communications lines.)

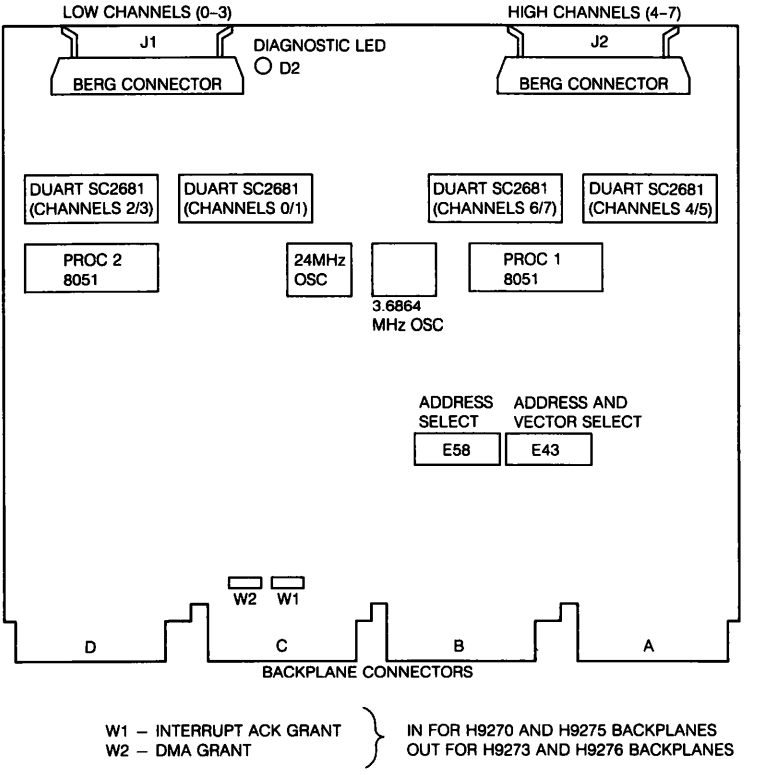
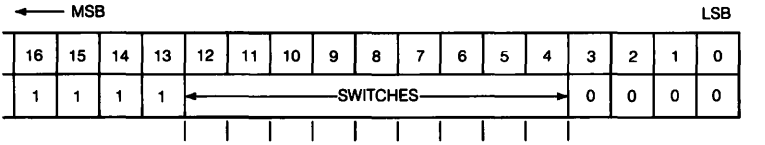


Figure 20-1 ▪ DHV11 Module Layout

Address Switches

The device address for the DHV11 is set on switchpacks E58 and E43, shown in Figure 20-1. Figure 20-2 shows the relationship between device addresses and switch positions. The 22-bit Q-bus address is given for each entry. The equivalent 16- and 18-bit addresses will be 16xxxx and 76xxxx, respectively.



SWITCH NUMBER	E58 1	E58 2	E58 3	E58 4	E58 5	E58 6	E58 7	E58 8	E43 1	DEVICE ADDRESS
									ON	17760020
								ON		17760040
								ON	ON	17760060
							ON			17760100
						ON				17760200
						ON	ON			17760300
					ON					17760400
					ON		ON			17760500
					ON	ON				17760600
					ON	ON	ON			17760700
				ON						17761000
			ON							17762000
			ON	ON						17763000
		ON								17764000
	ON									17770000

ON = SWITCH CLOSED TO RESPOND TO A LOGICAL 1 ON THE BUS

Figure 20-2 ▪ DHV11 Device Address Selection

Vector Switches

During an interrupt acknowledge sequence, the DHV11 returns a 9-bit interrupt vector to the host. The six high-order bits of this vector are derived from switches S3 through S8 of switchpack E43. Figure 20-3 shows how switch positions relate to vector addresses.

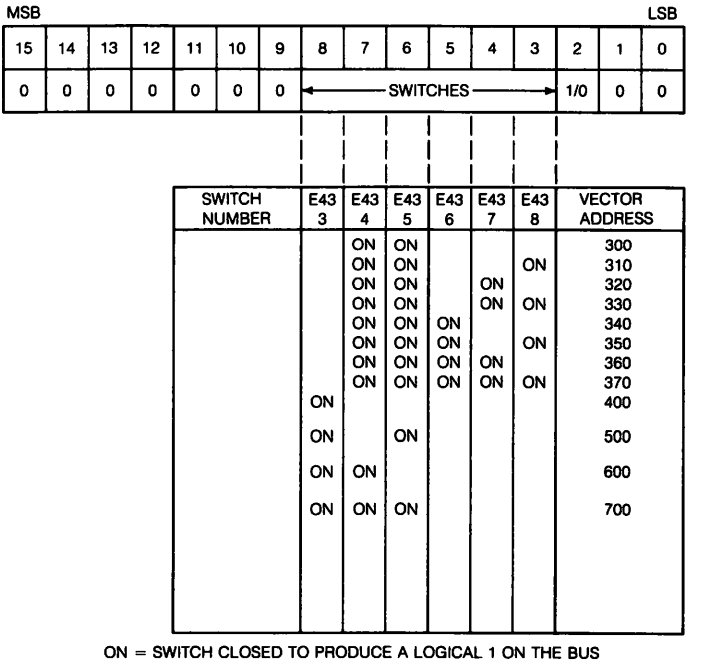


Figure 20-3 ▪ DHV11 Vector Address Selection

Bus Grant Continuity Jumpers

If the DHV11 is installed in a Q/Q-type backplane (such as the H9275 or H9270), jumpers W1 and W2 should be installed to provide continuity to the BIAK and BDMG bus grant signals. If the module is installed in a Q/CD-type backplane (such as the H9276 or H9273) where bus grant signals pass through each module via the AB connectors of each slot, W1 and W2 should be removed. (See Chapter 52 for a discussion of Q/Q and Q/CD backplanes.)

▪ Cables and Cabinet Kits

Each H3173-A distribution panel adapts one of the DHV11's Berg connectors to four subminiature D-type RS-232C connectors. Noise filtering is provided on each pin of the RS-232C connectors. This reduces electromagnetic radiation from the cables. It also provides the logic with some protection against static discharge. Figure 20-4 shows this layout. There is no CCITT equivalent of EIA circuit AA (protective ground). The 0-ohm link (W1) on the H3173-A can be removed to disconnect this circuit as needed.

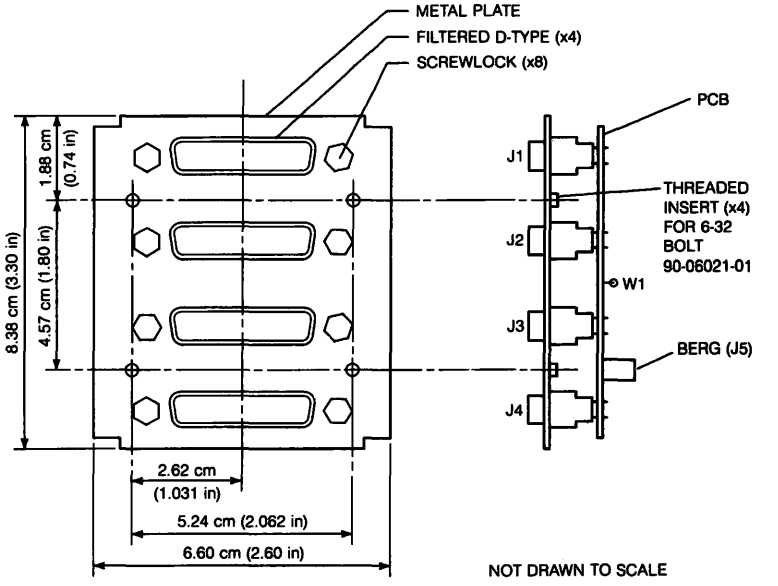


Figure 20-4 ▪ H3173-A Layout

Null Modem Cables

Null modem cables are used for local RS-232C connections. Recommended null modem cables are as follows.

1. BC22D (for EMC/RFI shielded cabinets):

- Round 6-conductor fully shielded cable to FCC specification
- Subminiature 25-pin D-type female connector on each end
- Lengths available:
  BC22D-10 – 3.1 m (10 ft)
  BC22D-25 – 7.62 m (25 ft)
  BC22D-35 – 10.72 m (35 ft)
  BC22D-50 – 15.24 m (50 ft)
  BC22D-75 – 22.9 m (75 ft)
  BC22D-A0 – 30.48 m (100 ft)
  BC22D-B5 – 76.2 m (250 ft)

2. BC03M

- Round 6-conductor (three twisted pairs), each pair shielded
- Cables over 30.48 m (100 ft) have a 25-pin subminiature D-type female connector at one end. The other end is unterminated for passing through conduit.
- Cables 30.48 m (100 ft) and less have a similar connector at each end.
- Lengths available:
  BC03M-25 – 7.62 m (25 ft)
  BC03M-A0 – 30.48 m (100 ft)
  BC03M-B5 – 76.2 m (250 ft)
  BC03M-E0 – 152.4 m (500 ft)
  BC03M-L0 – 304.8 m (1000 ft)

3. BC22A

- Round 6-conductor cable
- Subminiature 25-pin D-type female connector at each end
- Lengths available:
  BC22A-10 – 3.1 m (10 ft)
  BC22A-25 – 7.62 m (25 ft)

These null modem cables are all connected as in Figure 20-5. The cables are not polarized. Thus, either end can be used at the H3173-A panel.

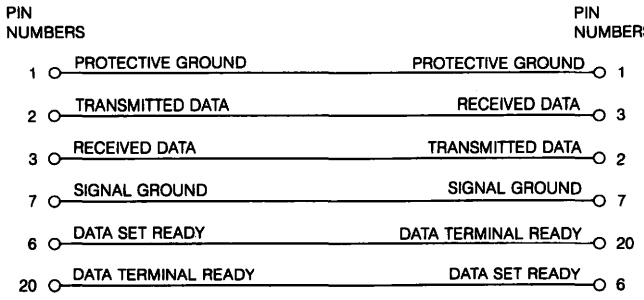


Figure 20-5 ▪ Null Modem Cable Connections

Full Modem Cables

Full modem cables are required for connection to modems and other terminal interface equipment. Recommended full modem cables are as follows.

1. BC22F (for EMC/RFI shielded cabinets)

- Round 25-conductor fully shielded cable
- Subminiature 25-pin D-type female connector on one end, male connector on the other
- Lengths available:
  BC22F-10 – 3.1 m (10 ft)
  BC22F-25 – 7.62 m (25 ft)
  BC22F-35 – 10.72 m (35 ft)
  BC22F-50 – 15.24 m (50 ft)
  BC22F-75 – 22.9 m (75 ft)

2. BC05D

- Round 25-conductor cable
- Subminiature 25-pin D-type female connector on one end, male connector on the other
- Lengths available:
  BC05D-10 – 3.1 m (10 ft)
  BC05D-25 – 7.62 m (25 ft)
  BC05D-50 – 15.24 m (50 ft)
  BC05D-60 – 18.6 m (60 ft)
  BC05D-A0 – 30.48 m (100 ft)

These cables are polarized and can be connected only with the female connector at the H3173-A panel.

Note

In some countries, protective hardware may be needed when connecting to certain lines. Refer to the national regulations before making a connection.

Data Rate to Cable Length Relationships

All the recommended cables have data rate/cable length characteristics as listed in Table 20-1.

Table 20-1 ▪ Data Rate/Cable Length Relationships

Data Rate (Bits/s)	Cable Length (Meters)	Cable Length (Feet)
110	914	3000
200	914	3000
1200	152	500
2400	152	500
4800	76	250
9600	76	250

Cabinet Kits

When ordered at the same time as the system in which it is to be installed, the DHV11 option (model number DHV11-AP) includes the base module (M3104), internal cables, and the I/O connection panel insert.

When ordered as a system upgrade, the DHV11 option (model number DHV11-M) includes the base module only. One of the following cabinet kits should be chosen for system installation:

CK-DHV11-AA	For use with the BA11-MA(MB) enclosure
CK-DHV11-AB	For use with the BA23 enclosure
CK-DHV11-AC	For use with the H349 distribution panel

Chapter 21 ▪ DLV11 Asynchronous Serial Line Unit

The DLV11 is an asynchronous line interface module that interfaces the Q-bus to any of several types of serial communications lines.

▪ Specifications

Identification	M7940
Size	Dual
Power	+5 Vdc ±5% at 1.0 A +12 Vdc ±3% at 0.18 A
Bus loads	
ac	2.5
dc	1.0

▪ Related Documentation

Document Title	**Order Number**
Field Maintenance Print Set	MP-00055-00
Communications Mini-reference Guide	EK-CMINI-RM

▪ Configuration

Using the wirewrap jumpers on the module, the user can select the register address, parity, number of data bits, number of stop bits, baud rate, and type of serial interface. Figure 21-1 shows the locations of the DLV11 jumpers, and Table 21-1 lists the jumper functions, along with their factory configuration.

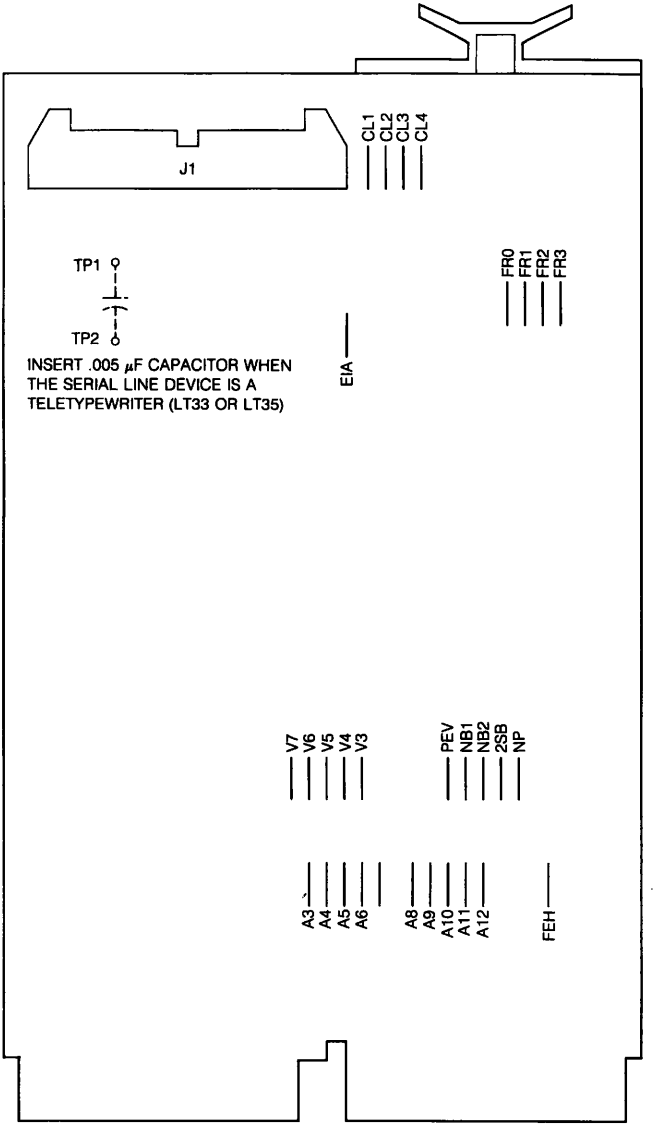


Figure 21-1 ▪ DLV11 Jumper Locations

Table 21-1 ▪ DLV11 Factory Jumper Configuration

Jumper	State	Function
A3	I	This arrangement of jumpers A3 through A12 implements the octal device address 17756X, the assigned address for the console device SLU. The least significant digit is hardwired on the module to address the four SLU device registers, as follows: X = 0, RCSR address; X = 2, RBUF address; X = 4, XCSR address; X = 6, XBUF address
A4	R	
A5	R	
A6	R	
A7	I	
A8	R	
A9	R	
A10	R	
A11	R	
A12	R	
V3	I	This arrangement of jumpers V3 through V7 implements an interrupt vector address of 60 for the receiver and 64 for the transmitter.
V4	R	
V5	R	
V6	I	
V7	I	
NP	R	No parity
2SB	R	Two stop bits
NB2	R	Eight data bits
NB1	R	
PEV	R	Even parity if NP installed
FEH	I	Halt on framing error (allows halt on break operation)
EIA	I	12 V EIA operation enabled
FR0	R	110 baud rate selected
FR1	R	
FR2	R	
FR3	R	
CL1	I	20 mA current loop active receiver and transmitter selected (jumpered with 180 ohm resistors)
CL2	I	
CL3	I	
CL4	I	

I = jumper installed; R = jumper removed

Register Addresses

The DLV11 uses four program-controlled registers, as listed in Table 21-2 Thus, each DLV11 module requires four contiguous register addresses. Addresses for the DLV11 can range from 160000 through 177770. The least-significant three bits address the desired register, as described in Tables 21-1 and 21-2. Address bits <3:12> are jumper-selected, as shown in Figure 21-2.

Addresses 177560 through 177566 are reserved for the DLV11 used with the console peripheral device. Additional DLV11 modules should be assigned addresses from 176500 through 176670, allowing up to 30 additional DLV11 modules to be addressed.

Table 21-2 ▪ DLV11 Standard Address Assignments

Description	Mnemonic	Console Address	2nd Module Address
Registers:			
Receiver Control/Status	RCSR (R/W)	177560	176500
Receiver Data Buffer	RBUF (R-O)	177562	176502
Transmitter Control/Status	XCSR (R/W)	177564	176504
Transmitter Data Buffer	XBUF (R-O)	177566	176506
Interrupt Vectors:			
Receiver		060	300
Transmitter		064	304

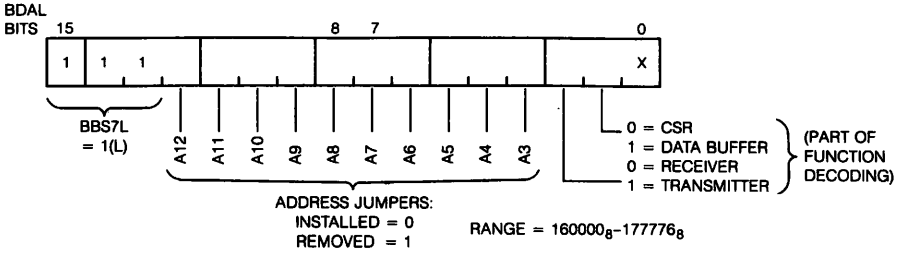


Figure 21-2 ▪ DLV11 Address Selection

Vector Addresses

The DLV11 can generate two interrupts — one for the transmitter and one for the receiver. Thus, each DLV11 requires two consecutive interrupt vectors. Vector addresses can range from 0 to 374. Address bits <3:7> are jumper-selected, as shown in Figure 21-3. Vector addresses 60 and 64 are reserved for the console device.

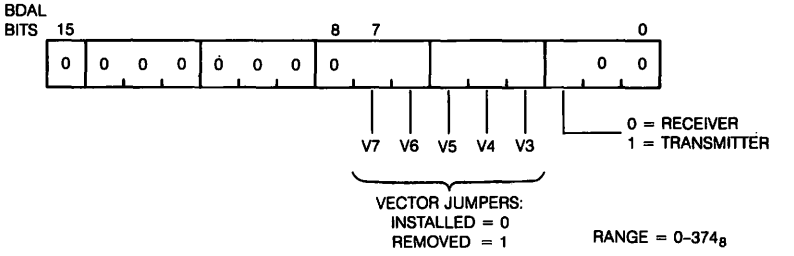


Figure 21-3 ▪ DLV11 Interrupt Vector Address Selection

UART Operation

The UART operation is programmed by using jumpers NP, 2SB, NB1, NB2, and PEV, as shown below.

Parity Transmitted

NP removed	no parity bit
NP and PEV installed	odd parity
NP installed and PEV removed	even parity

Number of Stop Bits Transmitted

2SB installed	one stop bit
2SB removed	two stop bits

Number of Data Bits Transmitted

Bits	NB1	NB2
5	Installed	Installed
6	Removed	Installed
7	Installed	Removed
8	Removed	Removed

Baud Rate Selection

Baud rate is programmed via jumpers FR0 through FR3, as shown in Table 21-3.

Table 21-3 ▪ DLV11 Baud Rate Selection

Baud Rate	FR3	FR2	FR1	FR0
50	I	I	R	I
75	I	I	R	R
110	R	R	R	R
134.5	I	R	I	I
150	R	R	R	I
200	I	R	I	R
300	R	R	I	R
600	I	R	R	I
1200	R	I	R	R
1800	R	I	R	I
2400	I	R	R	R
3600	R	R	I	I
4800	R	I	I	R
9600	R	I	I	I
External*	I	I	I	X

I = jumper installed; R = jumper removed; X = irrelevant

* via pin BH1

EIA Interface

EIA drivers are enabled when jumper EIA is installed. It should be removed during 20 mA current loop operation.

20 mA Current Loop Interface

Jumpers CL1 through CL4 are associated with 20 mA current loop interface operation. CL2 and CL3 are 180-ohm resistors.

Active Current Loop	
Transmit	CL4 jumper installed
	CL3 resistor installed
Receive	CL4 jumper installed
	CL3 resistor installed
Passive Current Loop	
Transmit	CL4 jumper removed
	CL3 resistor removed
Receive	CL4 jumper removed
	CL3 resistor removed

• Cables

The following cables are recommended for use with the DLV11 module:

BC05M	Round, 2-conductor cable with shielded leads for use during 20 mA current loop operation
BC05C	Round, 25-conductor cable for use with a Bell 103 modem and an EIA interface
	When used with either an H312A or H305 connector, for use with an EIA interface terminal

Chapter 22 • DLVE1 Asynchronous Line Interface

The DLVE1 is an asynchronous line interface module that interfaces the Q-bus to any of several types of serial communications lines. It was previously known as the DLV11-E.

• Specifications

Identification	M8017
Size	Dual
Power Requirements	+5.0 Vdc ±5% at 1.0 A (typical) +12.0 Vdc ±3% at 0.15 A (typical)
Bus Loads	
ac	1.6
dc	1.0

• Related Documentation

Document Title	**Order Number**
DLV11-E and DLV11-F Asynchronous Line Interface User's Manual	EK-DLV11-OP
Field Maintenance Print Set	MP-00460-00
DLV11-E Diagnostic Documentation Kit	ZJ243-RZ
Communications Mini-reference Guide	EK-CMINI-RM

• Configuration

The following items are user-selectable on the DLVE1 asynchronous line interface:

- Register addresses
- Interrupt vector address
- Data format
- Baud rate
- Interface mode

The user configures these items by installing and/or removing jumper wires between the wirewrap pins. Figure 22-1 shows the Revision D board jumper locations. A complete listing of the jumpers, their functions, and their factory configurations is given in Table 22-1.

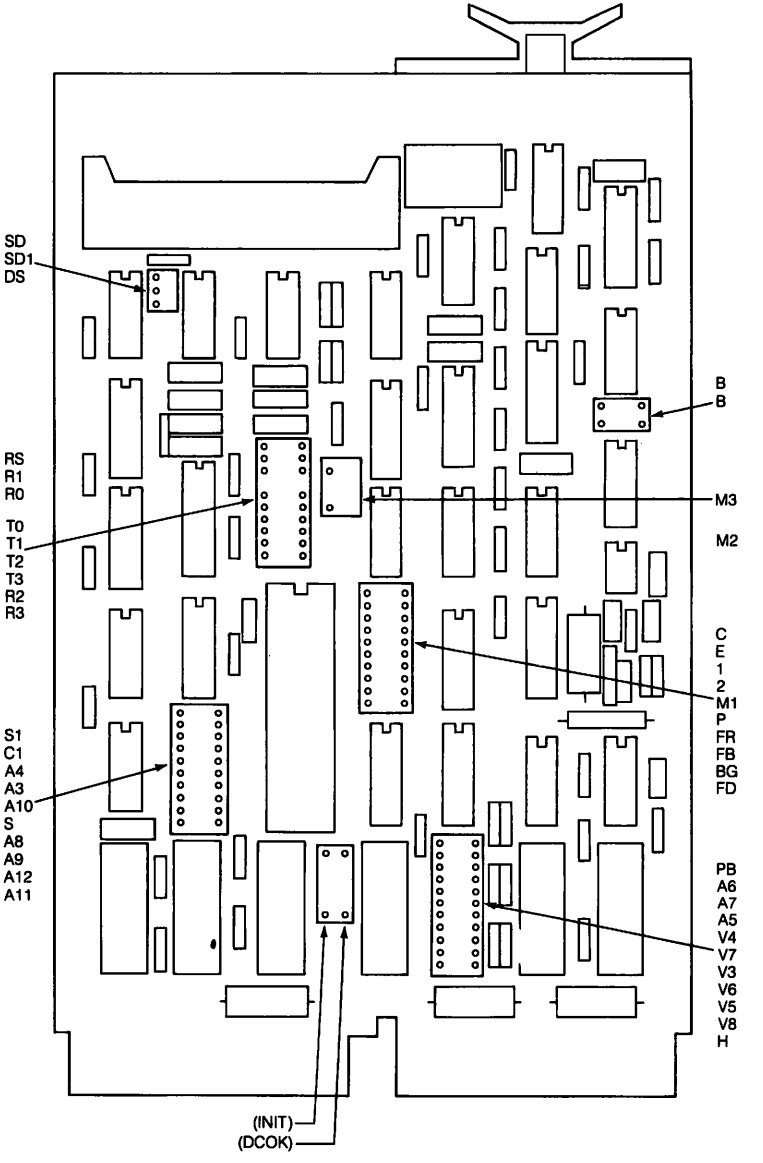


Figure 22-1 ▪ DLVE1 Revision D Etch Jumper Locations

Table 22-1 ▪ DLVE1 Jumper Definitions

Note

Jumpers are inserted to enable the function they control except for those jumpers that indicate negation (such as -B and E). Negated jumpers are removed to enable the functions they control.

Jumper	Function
A3-A12	These jumpers correspond to bits <3:12> of the address word. When inserted, they will cause the bus interface to check for a true condition on the corresponding address bit. Factory-configured for an address of 175610.
V3-V8	These jumpers are used to generate the vector during an interrupt transaction. Each inserted jumper will assert the corresponding vector bit on the Q-bus. Factory-configured for a receiver vector address of 300 and a transmitter vector address of 304.
R0-R3	These jumpers are used to select receiver and transmitter baud rates during common-speed operation. They are used for receiver-only baud-rate-select during split-speed operation, as defined in Table 22-3. They are factory-configured for a baud rate of 110.
T0-T3	These jumpers are used to select transmitter baud rates during split-speed operation. They are used for both receiver and transmitter baud rates if maintenance mode is entered during split-speed operation, as defined in Table 22-3. They are factory-configured for a baud rate of 9600.
BG	Jumper is inserted to enable break generation. Factory-inserted.
P	Jumper is inserted for operation with parity. Factory-removed.
E	Jumper is removed for even parity; inserted for odd parity. Factory-removed.
1,2	These jumpers select the desired number of data bits, as defined in Table 22-4. Factory-configured for eight data bits/character.
PB	Jumper is inserted to enable the programmable baud rate capability. Factory-removed.

(continued on next page)

Table 22-1 • DLVE1 Jumper Definitions (Cont.)

Jumper	Function
C, C1	These jumpers are inserted for common speed operation. (Note that S and S1 must be removed when C and C1 are inserted.) Both jumpers are factory-inserted.
S, S1	Inserted for split speed operation. (Note that C and C1 must be removed when S and S1 are inserted.) Both jumpers are factory-removed.
H	This jumper is inserted to assert BHALT when a framing error is received, except when the maintenance bit is set. This places the processor in the halt mode. The jumper is factory-removed.
B, −B	Jumper B is inserted to negate BDCOK when a break signal or framing error is received, except when the maintenance bit is set. This causes the processor to reboot. (Jumper −B must be removed when B is inserted.) Jumper B is factory-removed; jumper −B is factory-inserted.
−FD	Jumper is removed to force data terminal ready signal on. Factory-inserted.
−FR	Jumper is removed to force request to send signal on. Factory-inserted.
RS	This jumper is inserted to enable normal transmission of the request to send signal. Factory-inserted.
FB	Jumper is inserted to enable transmission of the force busy signal (for Bell model 103E data sets). Factory-removed.
M, M1	These are test jumpers used during the manufacture of the module. They are not defined for field use.

Register Addresses

Register addresses for the DLVE1 can range from 160000 through 177770. Since each module has four registers, each requires four addresses. Table 22-2 lists the registers along with their standard factory-configured addresses.

The low-order three bits of each address indicate the individual register within the register set. Bits <3:12> are jumper-selected as illustrated in Figure 22-2, using jumpers A3 through A12.

Addresses 177560 through 177566 are reserved for the module used with the console peripheral device. Additional modules should be assigned addresses in accordance with the standard Digital floating-address assignment algorithm.

Table 22-2 ▪ DLVE1 Standard Address Assignments

Description	Mnemonic	Console Module	Second Module
Registers:			
Receiver Control/Status	RCSR (R/W)	177560	175610
Receiver Data Buffer	RBUF (R-O)	177562	175612
Transmit Control/Status	XCSR (R/W)	177564	175614
Transmit Data Buffer	XBUF (R-O)	177566	175616
Interrupts:			
Receiver		60	300
Transmitter		64	304

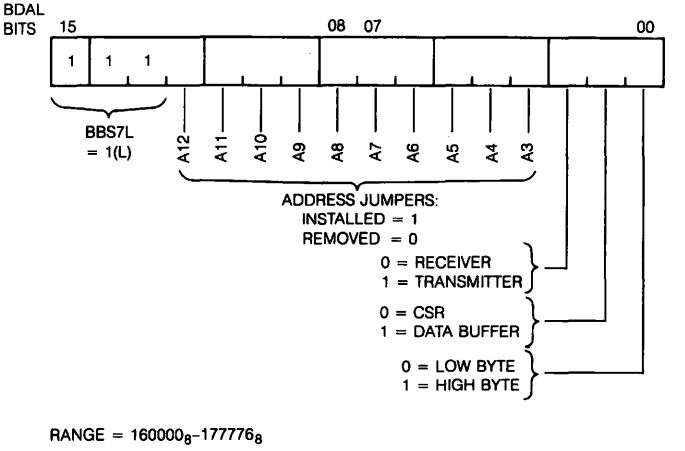


Figure 22-2 ▪ DLVE1 Address Selection

Interrupt Vectors

The interrupt vectors are selected by using jumpers V3 through V8. The standard configuration is shown in Figure 22-3 and Table 22-2. The vectors can range from 001 through 774. Note that vectors 60 and 64 are reserved for the console device. Additional DLVE1 modules should be assigned vectors in accordance with the standard Digital floating vector assignment algorithm.

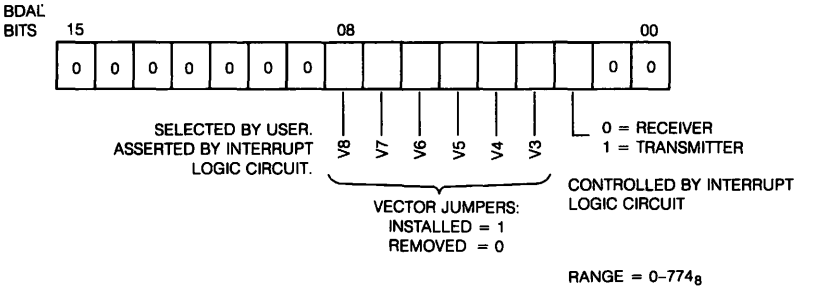


Figure 22-3 ▪ DLVE1 Interrupt Vector Selection

Baud Rate Selection

The DLVE1 allows the user to configure jumpers T0-T3 and R0-R3 for the transmit baud rate and the receiver baud rate, as shown in Table 22-3.

Data Bit Selection

The number of data bits being transmitted or received by the DLVE1 is user-selectable by installing or removing jumpers 1 and 2. The specific number of data bits, as controlled by the configuration of jumpers 1 and 2, is shown in Table 22-4.

Table 22-3 ▪ DLVE1 Baud Rate Selection

R3 T3	R2 T2	R1 T1	R0 T0	Baud Rate
I	I	I	I	50
I	I	I	R	75
I	I	R	I	110
I	I	R	R	134.5
I	R	I	I	150
I	R	I	R	300
I	R	R	I	600
I	R	R	R	1200
R	I	I	I	1800
R	I	I	R	2000
R	I	R	I	2400
R	I	R	R	3600
R	R	I	I	4800
R	R	I	R	7200
R	R	R	I	9600
R	R	R	R	19200

I = jumper installed; R = jumper removed

Table 22-4 ▪ DLVE1 Data Bit Selection

Jumper 2	Jumper 1	Number of Data Bits
I	I	5
I	R	6
R	I	7
R	R	8

▪ Cables and Cabinet Kits

Connection to the peripheral device is via an optional BC05C-*X** modem cable for EIA interface applications. The BC05C cable provides the correct connection to the 40-pin connector on the DLVE1. The peripheral device end of the cable is terminated with a Cinch DB25P connector that is pin-compatible with Bell 103, 113, 202C, 202D, and 212 modems. Connector pinning and signal levels conform to EIA specification RS-232C.

* *X* = Length in feet. Standard length is 25 feet.

When ordered at the same time as the system in which it is to be installed, the DLVE1 option (model number DLVE1-DP) includes the base module (M8017), internal cables, and the I/O connection panel insert.

When ordered as a system upgrade, the DLVE1 option (model number DLVE1-M) includes the base module only. One of the following cabinet kits should be chosen for system installation:

CK-DLVE1-DA	For use with the BA11-MA(MB) enclosure
CK-DLVE1-DB	For use with the BA23 enclosure
CK-DLVE1-DC	For use with the H349 distribution panel
CK-DLVE1-D3	For use with CPUs that do not have an I/O connection panel. Kit contains a 25-foot cable that connects the DLVE1-M module to the RS-232 device.

Chapter 23 ▪ DLVJ1 Four-Channel Asynchronous Serial Interface

The DLVJ1 is a four-channel asynchronous serial line unit used to interface peripheral equipment to a Q-bus. The DLVJ1 was previously known as the DLV11-J.

▪ Specifications

Identification	M8043
Size	Dual
Power Requirements	+5 V ±5% at 1.0 A (typical) +12 V ±3% at 0.25 A (typical)
Bus Loads	
ac	1.0
dc	1.0

▪ Related Documentation

Document Title	Order Number
DLV11-J User's Guide	EK-DLV1J-UG
DLV11-J Print Set	MP-00586-00
DLV11-J User's Guide	EK-DLV1J-UG
DLV11-J Diagnostic Documentation Kit	ZJ269-RZ
Communications Mini-reference Guide	EK-CMINI-RM

▪ Configuration

The DLVJ1 device and vector addressing, serial word formats, baud rates, and interface type are selected by installing and/or removing jumpers. Wirewrap posts are provided on the module for this purpose. The module is factory-configured and ready to use in most user applications. If a system requires different device register addresses and interrupt vectors or operations, however, the module can be reconfigured. The DLVJ1 module is factory-configured for the following operations:

- Base address = 176500
- Base vector address = 300
- Channel 3 enabled as the console device (device addresses 177560 to 177566 and vector addresses 60 and 64).
- Channel 3 halt on break enabled
- Baud rates (transmit and receive are identical): Channels 0, 1, and 2 = 9600 baud; Channel 3 = 300 baud
- Data/parity/stop bit format (all channels): Eight data bits One stop bit No parity
- Serial line signal interface levels (all channels) compatible with both EIA RS-232C and RS-423, simultaneously (slew rate = 2 μs)

Figure 23-1 gives jumper and pad locations on the DLVJ1 module and Table 23-1 gives a summary of the module's factory configuration.

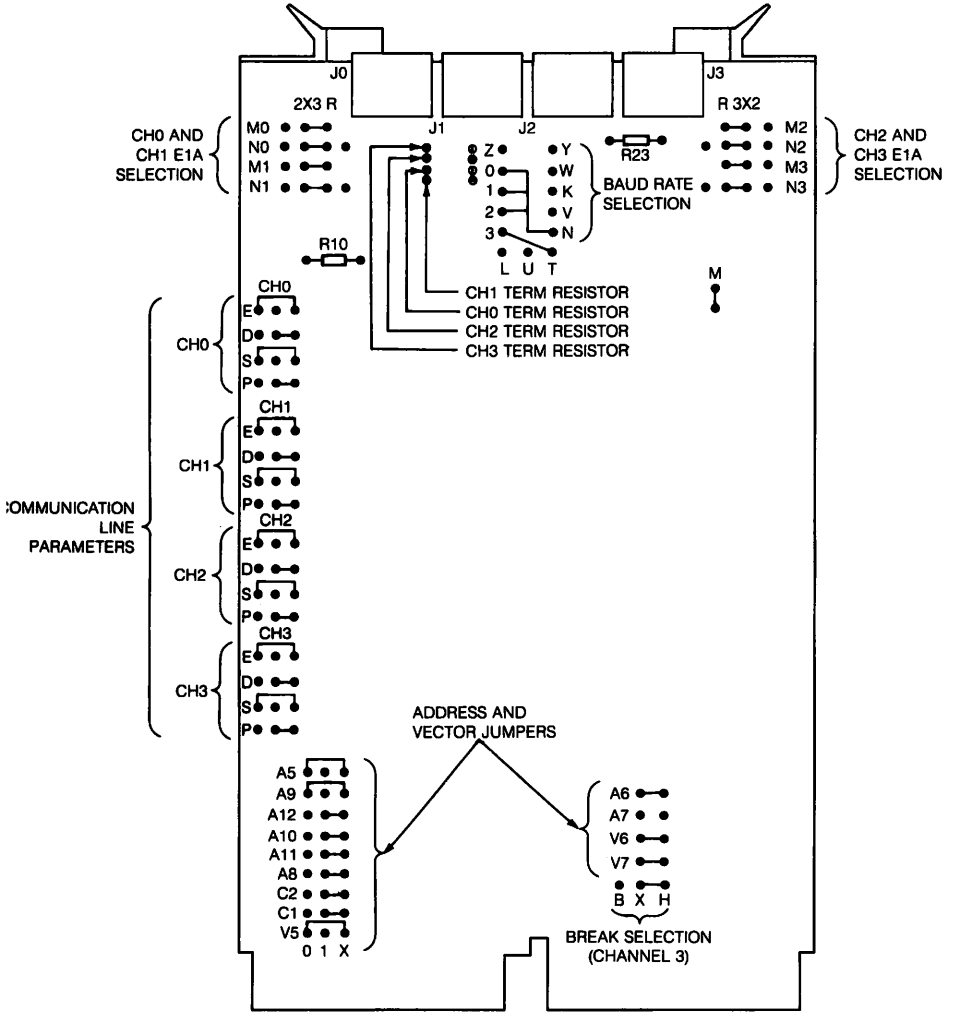


Figure 23-1 ▪ DLVJ1 Jumper Locations

Table 23-1 ▪ DLVJ1 Factory Configuration

Label	Standard Configuration	Function Implemented
A12 A11 A10 A9 A8 A7 A6 A5	X to 1 X to 1 X to 1 X to 0 X to 1 R I X to 0	This arrangement of jumpers A5-A12 implements the octal base device address 1765XX, which is the assigned address for channel 0 RCSR. The least significant digit is decoded on the module during operation to address one of four SLU device registers as follows: X = 0, RCSR X = 2, RBUF X = 4, XCSR X = 6, XBUF
C1 C2	X to 1 X to 1	These jumpers are used to enable channel 3 for console operation. The base address must be 176500, 176540, or 177500 for the console.
(Break response)	X to H	This jumper determines channel 3 break response. The board is configured for halt (console emulator mode) on break condition.
V7 V6 V5	I I X to 0*	This arrangement of jumpers V5-V7 implements the octal base vector of 300 with channel 3 at 60 and 64.
E D S P	X to 0 X to 1 X to 0 X to 1	Odd parity 8 data bits 1 stop bit Parity inhibited These jumpers determine the word format used by the channel. All channels are configured the same at the factory.

(continued on next page)

Table 23-1 ▪ DLVJ1 Factory Configuration (Cont.)

Label	Standard Configuration	Function Implemented
0	0 to N	9600 baud
1	1 to N	9600 baud
2	2 to N	9600 baud
3	3 to T	300 baud These jumpers determine the baud rate of the serial line channel for same baud rate daisychain wirewraps.
NO-3 MO-3	X to 3 X to 3	These jumpers determine the EIA standard compatibility of the channel. All channels are set at the factory to be compatible to both EIA RS-423 and RS-232C simultaneously.
R10	22 KΩ	Channels 0 and 1, slew rate of 2 μs (used when configured for EIA RS-423/RS-232C).
R23	22 KΩ	Channels 2 and 3, slew rate of 2 μs (used when configured for EIA RS-423/RS-232C).

* See interrupt vector format figure.

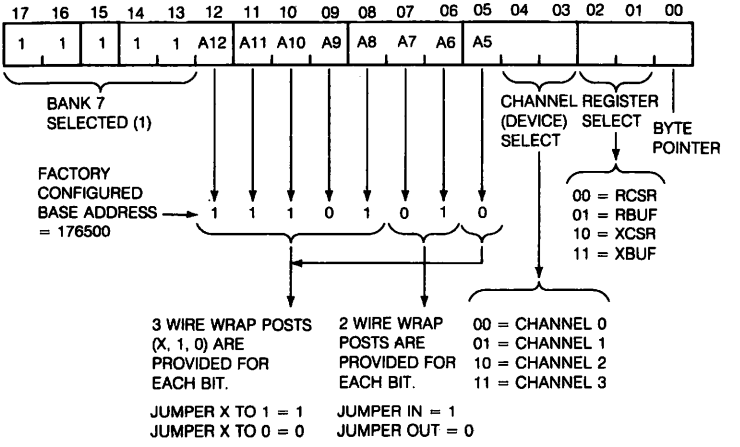
Device Registers

The DLVJ1 contains 16 device registers that can be addressed individually by the program. The four device registers provided for each of the SLU channels (0 through 3) are

Receive Control/Status Registers	(RCSR)
Receive Data Buffer	(RBUF)
Transmit Control/Status Register	(XCSR)
Transmit Data Buffer	(XBUF)

Wirewrap jumpers are configured to establish the base address (BA) for the module. This base address is the channel 0 RCSR address. The device address format is shown in Figure 23-2. The remaining device addresses follow through 16 (decimal) contiguous word addresses, as shown in Table 23-2. Note, however, that it is possible to independently dedicate the last four addresses (channel 3) to a console device. When configured for console device operation, the channel's device register addresses will be 177560 to 177566. For console operation, the board's base address must be one of the following:

176500 (factory-configured)
176540
177500



NOTE:
RANGE 160000_8–177770_8 NONEXTENDED ADDRESS
760000_8–777770_8 EXTENDED ADDRESS

Figure 23-2 ▪ DLVJ1 Channel 0 RCSR Address Format

Table 23-2 ▪ DLVJ1 Address Assignments (with Console Selected)

Address	Device Register	Associated Vector
Channel 0		
Module Base Address (BA)	RCSR	Module Base Vector (BV)
BA+2	RBUF	
BA+4	XCSR	BV+4
BA+6	XBUF	
Channel 1		
BA+10	RCSR	BV+10
BA+12	RBUF	
BA+14	XCSR	BV+14
BA+16	XBUF	
Channel 2		
BA+20	RCSR	BV+20
BA+22	RBUF	
BA+24	XCSR	BV+24
BA+26	XBUF	
Channel 3 (Console Device)		
177560	RCSR	
177562	RBUF	60
177564	XCSR	
177566	XBUF	64

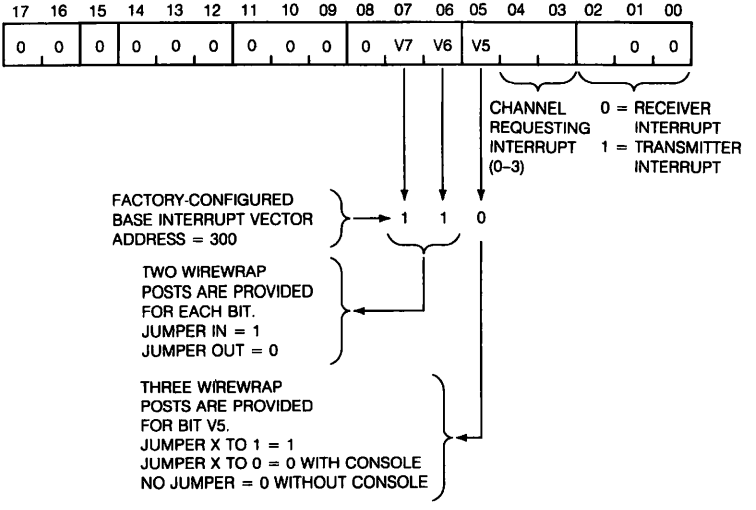
Interrupt Vectors

Two interrupt vectors are provided for each of the four SLU channels (eight vectors total). The procedure for configuring the vectors is similar to that for configuring the base device register address; the configured base vector is the channel 0 receiver interrupt vector. Each interrupt vector references two word locations in memory. Hence, sequential vectors appear in increments of four.

The module is factory-configured with an interrupt vector base of 300. In addition, since the module is configured for channel 3 operation as the console device, channel 3 will automatically have interrupt vectors of 60 and 64. The vector format is shown in Figure 23-3 and a summary of vector jumper configurations is provided in Table 23-3. Table 23-4 gives a list of the factory-configured vector assignments.

Interrupt priority within the DLVJ1 module is structured as follows:

Interrupt Priority	Requesting Function
1 (highest)	Channel 0, receiver
2	Channel 1, receiver
3	Channel 2, receiver
4	Channel 3, receiver
5	Channel 0, transmitter
6	Channel 1, transmitter
7	Channel 2, transmitter
8 (lowest)	Channel 3, transmitter



NOTE:
RANGE 0–377_8 (040_8 NOT ALLOWED IN CONSOLE MODE)

Figure 23-3 ▪ DLVJ1 Interrupt Vector Format

Table 23-3 ▪ Summary of DLVJ1 Vector Jumper Configurations

Label	Logical 1	Logical 0
V7	Jumper installed	Jumper removed
V6	Jumper installed	Jumper removed
V5	Jumper installed between pins X and 1	Console not selected: jumper removed. Console selected: jumper installed between pins X and 0.

Table 23-4 ▪ DLVJ1 Factory-Configured Vector Assignments (with Console Selected)

Standard Address	Interrupt Vector
300 [Module Base Vector (BV)]	Channel 0, receiver
304 (BV+4)	Channel 0, transmitter
310 (BV+10)	Channel 1, receiver
314 (BV+14)	Channel 1, transmitter
320 (BV+20)	Channel 2, receiver
324 (BV+24)	Channel 2, transmitter
60	Channel 3, receiver
64 Console Selected	Channel 3, transmitter

Character Formats

Each of the four channels can be configured independently for various character formats. When a character format is configured (by wirewrap jumpers) for a channel, both the transmitter and receiver use the same format. The character can contain

7 or 8 data bits
1 or 2 stop bits
Parity or no parity
Even or odd parity

Configuration instructions for determining the character formats of each channel are shown in Table 23-5.

Baud Rates

Each channel can be configured for baud rates ranging from 150 to 38,400 bits per second. One baud rate clock input wirewrap pin is provided for each channel (0 through 3). Both the transmitter and receiver for a given channel must operate at the same baud rate; split baud rate operation cannot be configured. Configure baud rates by connecting a jumper from the appropriate baud rate generator output wirewrap pin to the clock input pin of the channel. One jumper is required for each channel. When configuring the same baud rate for more than one channel, the wirewrap pins can be daisychained. Table 23-6 lists the possible baud rates for each channel and their associated labels.

Table 23-5 ▪ DLVJ1 Character Format Jumpers

Label	Channel Parameter	Wirewrap X to 0	Connection X to 1	Comments
D	Number of data bits	7 bits	8 bits	LSB transmitted first
S	Number of stop bits	1 bit	2 bits	
P	Parity inhibit	Parity generation and detection enabled	Parity bit deleted; parity error = 0	
E	Even parity enabled	Odd parity expected	Even parity expected	Only when P = 0

Table 23-6 ▪ DLVJ1 Baud Rate Generator Outputs

Label	Baud Rate (Bits/Second)
U	150
T	300
V	600
W	1200
Y	2400
L	4800
N	9600
K	19200
Z	38400

Console Device Selection

Channel 3 of the DLVJ1 module can be dedicated independently for console device operation. To accomplish this, the console-select jumpers must be configured properly. Table 23-7 gives channel 3 configuration instructions. When configured for console operation, the device addresses are 177560 to 177566 and the interrupt vectors are 60 and 64.

Table 23-7 ▪ Summary of DLVJ1 Console Selection Jumper Configurations

Label	Console Selected	Console Not Selected
C1	Install jumper from X to 1.	Install jumper from X to 0.
C2	Install jumper from X to 1.	Install jumper from X to 0.

Break Response

Channel 3 may be configured to either bootstrap, halt (console emulator mode), or have no response to a receive break condition. A bootstrap response causes the processor to execute the bootstrap program starting at the memory location defined by the powerup mode jumpers of the processor. A halt response causes the processor to halt and the console octal debugging technique (ODT) microcode to be invoked. Configuration instructions are given in Table 23-8.

Table 23-8 ▪ Summary of DLVJ1 Channel 3 Break Operation Jumpers

Break Response	Jumper Connection
Boot*	Install jumper between X and B.
Halt	Install jumper between X and H.
No Response	No jumper installed.

* Do not send continual breaks to a system so configured because it will cause continued reinitialization of any device on the bus.

Peripheral Interface Configuration

Each of the channels can be independently configured for serial line signal compatibility with EIA RS-423 (simultaneously RS-232C), RS-422, or 20 mA current loop devices. Configuration instructions for each of the standards are listed in Table 23-9. Table 23-10 is used in conjunction with Table 23-9 when configuring EIA RS-423 (RS-232C-compatible) slew rates.

Table 23-9 ▪ Summary of DLVJ1 Serial Channel Signal Level Configurations

Serial Channel Signal Level Modifiers	EIA RS-422	EIA RS-232C and RS-423	20 mA Current Loop
M0-3 Jumper	Connect X and 2	Connect X and 3	Connect X and 3
N0-3 Jumper	Connect X and 2	Connect X and 3	Connect X and R for program-controlled paper tape reader
Termination Resistor (one per channel)	Install a 100-Ω, ¼-W, nonwire wound, fusible resistor	No resistor installed	No resistor installed
Wave-Shaping Resistor (one per channel pair; channel pair 0 and 1; 2 and 3)	Not required	Install resistor from Table 23-10 (¼-W nonwire wound)	Install 22-KΩ nonwire wound resistor
Fuse F1	Not required	Not required	Install 2.0 A pico fuse

Table 23-10 ▪ EIA RS-423 and RS-232C Slew Rate Resistor Values

Baud Rate	R10 or R23
38400	22 KΩ
19200	51 KΩ
9600	120 KΩ
4800	200 KΩ
2400	430 KΩ
1200	820 KΩ
600	1 MΩ
300	1 MΩ
150	1 MΩ
110	1 MΩ

▪ Cables and Cabinet Kits

Cables currently available to mate with the 2×5 pin amp connector on the DLVJ1 are listed below.

BC20N-05	5-ft EIA RS-232C null modem cable to interface directly with an EIA RS-232C terminal (2×5 pin amp female to RS-232C female)
BC21B-05	5-ft EIA RS-232C modem cable to interface with modems and acoustic couplers (2×5 pin amp female to RS-232C male)
BC20M-50	50-ft EIA RS-422 or RS-423 cable for high-speed transmission (19.2 Kbaud) between two DLVJ1s (2×5 pin amp female to 2×5 pin amp female)

When ordered at the same time as the system in which it is to be installed, the DLVJ1 option (model number DLVJ1-LP) includes the base module (M8043), internal cables and the I/O connection panel insert.

When ordered as a system upgrade, the DLVJ1 option (model number DLVJ1-M) includes the base module only. One of the following cabinet kits should be chosen for system installation:

CK-DLVJ1-LA	For use with the BA11-MA(MB) enclosure
CK-DLVJ1-LB	For use with the BA23 enclosure
CK-DLVJ1-LC	For use with the H349 distribution panel

Chapter 24 • DZQ11 Asynchronous Multiplexer

The DZQ11 is an asynchronous multiplexer that provides an interface between a Q-bus processor and four asynchronous serial data communication lines. It is functionally equivalent to and software-compatible with the DZV11 option.

• Specifications

Identification	M3106
Size	Dual
Power Requirements	+5 Vdc, 1.1 A (typical) +12 Vdc, 0.24 A (typical)
Bus Loads	
ac	1.5
dc	1.0
Nonstandard Environmental Specifications	
Storage temperature	0°C to 66°C (32°F to 151°F)

• Related Documentation

Document Title	Order Number
DZQ11 Asynchronous Multiplexer User's Guide	EK-DZQ11-UG
DZQ11 Asynchronous Multiplexer Maintenance Card	EK-DZQ11-MC
DZQ11 Asynchronous Multiplexer Technical Manual	EK-DZQ11-TM
Field Maintenance Print Set	MP-01795-00
DZV11 Diagnostic Documentation Kit	ZJ251-RZ
Communications Mini-reference Guide	EK-CMINI-RM

• Configuration

The DZQ11 is configured by means of 13 jumpers and two 10-position switchpacks. Figure 24-1 shows the locations of these jumpers and switches.

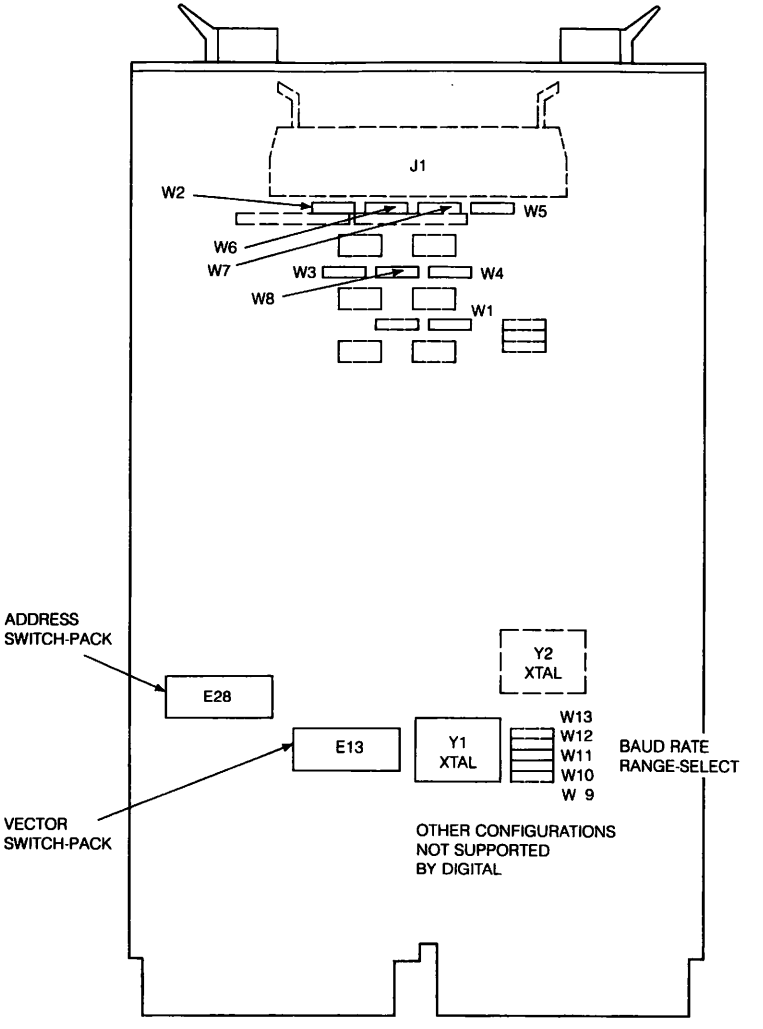


Figure 24-1 ▪ DZQ11 Jumper and Switch Locations

Device Address

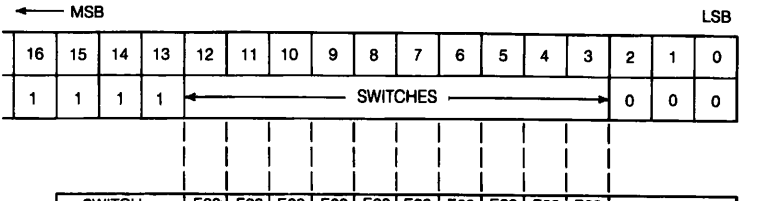
The DZQ11 contains six addressable registers. Table 24-1 lists these registers and their related DZQ11 addresses. The device address of the DZQ11 is that address assigned to the control and status register.

Table 24-1 ▪ DZQ11 Standard Address Assignments

Register	Mnemonic	Address*
Control and Status Register	CSR (R/W)	76XXX0
Receiver Data Buffer	RBUR (R-O)	76XXX2
Line Parameter Register	LPR (W-O)	76XXX2
Transmitter Control Register	TCR (R/W)	76XXX4
Modem Status Register	MSR (R-O)	76XXX6
Transmit Data Register	TDR (W-O)	76XXX6

* XXX is selected in agreement with the floating device address system.

The DZQ11 device address is selected from the floating address space (from 760010 to 763776). The 10-position switchpack, E28, is used to configure the module to its assigned address, as shown in Figure 24-2. Note that when a switch is closed (ON), a binary 1 is encoded for the corresponding address bit; when a switch is open (OFF), a binary 0 is encoded.



SWITCH NUMBER	E28 1	E28 2	E28 3	E28 4	E28 5	E28 6	E28 7	E28 8	E28 9	E28 10	DEVICE ADDRESS
											17760000
										ON	17760010
									ON		17760020
									ON	ON	17760030
								ON			17760040
								ON		ON	17760050
								ON	ON		17760060
								ON	ON	ON	17760070
							ON				17760100
						ON					17760200
						ON	ON				17760300
					ON						17760400
					ON		ON				17760500
					ON	ON					17760600
					ON	ON	ON				17760700
			ON	ON	ON	ON	ON	ON	ON		17763760
			ON	ON	ON	ON	ON	ON	ON	ON	17763770

ON = SWITCH CLOSED TO RESPOND TO A LOGICAL 1 ON THE BUS

Figure 24-2 ▪ DZQ11 Device Address Selection

Vector Address

The DZQ11 is assigned a vector address in the floating vector space (from 300 to 774). The first six switches of the 10-position switchpack, E13, are used to configure the module to its assigned vector address, as shown in Figure 24-3. Note that when a switch is closed (ON), a binary 1 is encoded for the corresponding address bit; when a switch is open (OFF), a binary 0 is encoded.

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	←SWITCHES→						1/0	0	0

SWITCH NUMBER	E13 1	E13 2	E13 3	E13 4	E13 5	E13 6	VECTOR ADDRESS
		ON	ON				300
		ON	ON			ON	310
		ON	ON		ON		320
		ON	ON		ON	ON	330
		ON	ON	ON			340
		ON	ON	ON		ON	350
		ON	ON	ON	ON		360
		ON	ON	ON	ON	ON	370
	ON						400
	ON		ON				500
	ON	ON					600
	ON	ON	ON				700
	ON	ON	ON	ON	ON		760
	ON	ON	ON	ON	ON	ON	770

ON = SWITCH CLOSED TO PRODUCE A LOGICAL 1 ON THE BUS

Figure 24-3 ▪ DZQ11 Vector Address Selection

Test Switch (E13-8)

Switch 8 of the vector selection switchpack, E13, is a test switch used to disconnect the DZQ11 oscillator from all circuitry. This switch must be in the ON position before installation.

Break Character Response

Switches 9 and 10 of the vector selection switchpack, E13, control the DZQ11's response to a BREAK character received on line 3. There are three valid responses—halt, boot, and no response. See Table 24-2.

Table 24-2 ▪ DZQ11 Break Character Response Options

E13-9	E13-10	Response to BREAK
OFF	OFF	No response
ON	OFF	Causes processor to halt
OFF	ON	Causes processor to reboot
ON	ON	(Illegal configuration)

Modem Control

There are eight jumpers used for modem control on the DZQ11 The jumpers labeled W1 to W4 connect the Data Terminal Ready (DTR) circuit to the Request to Send (RTS) circuit. This allows the DZQ11 to assert both DTR and RTS when using modems that need control of RTS. These jumpers must be installed for running the cable and external diagnostic programs.

The four jumpers W5 to W8 connect the Forced Busy (FB) circuits to the RTS circuits. When these jumpers are installed, asserting an RTS circuit also places an ON or BUSY level on the corresponding FB circuit. Jumpers W5 to W8 are normally cut out unless they are needed by the modems used. Table 24-3 shows the jumper line assignments.

Table 24-3 ▪ DZQ11 Modem Control Jumper Configuration

Jumper	Connection	Line
W1	DTR to RTS	3
W2	DTR to RTS	2
W3	DTR to RTS	1
W4	DTR to RTS	0
W5	RTS to FB	3
W6	RTS to FB	2
W7	RTS to FB	1
W8	RTS to FB	0

Baud Rate Jumpers

The DZQ11 is factory-configured for software selection of standard baud rates up to 9600 baud. Using jumpers W9 through W13, the user can configure the module for software selection of other, nonstandard baud rates. Refer to the *DZQ11 Asynchronous Multiplexer User's Guide* for more information.

▪ Cables, Connectors, and Cabinet Kits

The basic DZQ11 option (DZQ11-M) can be supplied with one of five cabinet kits for installation into different systems:

1. CK-DZQ11-DA (21-inch cable) — for use in PDP-11/23S
2. CK-DZQ11-DB (12-inch cable) — for use in Micro/PDP-11
3. CK-DZQ11-DC (30-inch cable) — for use in PDP-11/23-PLUS
4. CK-DZQ11-DF (36-inch cable) — for use in PDP-11/73
5. CK-DZQ11-D3 unshielded option (BC11U-25 cable)

The first four cabinet kits are almost identical except for the length of the flat ribbon cables, and the addition of an adapter plate in the CK-DZQ11-DC. They are made up of the following:

- BC05L-xx cable
- H325 line-loopback connector
- The distribution panel — 70-19964-00
- Mounting bolts and washers for the distribution panel.

Note

The distribution panels provide noise filtering and static discharge protection on the communications lines. The -DC version has an adapter plate that allows the panel to be mounted in the PDP-11/23-PLUS.

BC05L-xx cables are supplied in different lengths for each kit as previously specified.

The CK-DZQ11-D3 cabinet kit is a cable assembly made up of four cables, with D-type connectors at one end, and the other end connected to a socket that fits in the module connector. This kit does not provide noise filtering or static discharge protection on the communications lines.

The connections from the DZQ11 use 25-pin, male, subminiature, D-type connectors as specified for RS-232C.

Chapter 25 • DZV11 Asynchronous Multiplexer

The DZV11 is an asynchronous multiplexer interface module that connects the Q-bus with up to four asynchronous serial data communications channels.

• Specifications

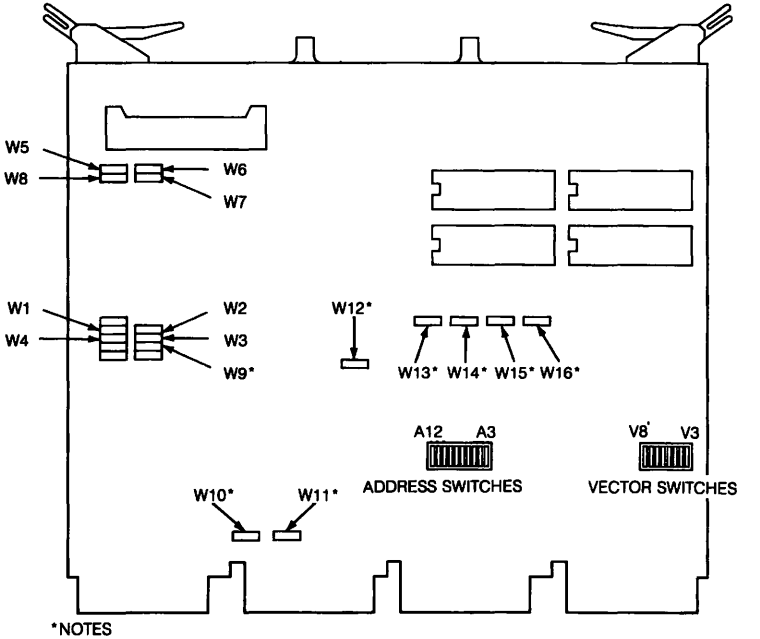
Identification	M7957
Size	Quad
Power Requirements	+5 Vdc ±5% at 1.15 A (typical) +12 Vdc ±3% at 0.39 A (typical)
Bus Loads	
ac	3.9
dc	1.0
Interface	EIA standard RS-232C

• Related Documentation

Document Title	Order Number
DZV11 QMA Asynchronous Multiplexer Technical Manual	EK-DZVQM-TM
DZV11 QMA Asynchronous Multiplexer User's Guide	EK-DZVQM-UG
DZV11 QMA Field Maintenance Print Set	MP-00462-00
DZV11 Diagnostic Documentation Kit	ZJ251-RZ
Communications Mini-reference Guide	EK-CMINI-RM

• Configuration

The DZV11 is configured by means of 16 wirewrap jumpers and two switchpacks, as shown in Figure 25-1.



*NOTES

JUMPERS W9, W12, W13, W14, W15, AND W16 ARE REMOVED ONLY FOR MANUFACTURING TESTS. THEY SHOULD NOT BE REMOVED IN THE FIELD.

JUMPERS W10 AND W11 MUST REMAIN INSTALLED WHEN THE MODULE IS USED IN A BACKPLANE THAT SUPPLIES Q-BUS SIGNALS TO THE C AND D CONNECTORS OF THE DZV11 (SUCH AS THE H9270). WHEN THE MODULE IS USED IN A BACKPLANE THAT INTERCONNECTS THE C AND D SECTIONS TO AN ADJACENT MODULE, JUMPERS W10 AND W11 MUST BE REMOVED.

Figure 25-1 ▪ DZV11 Module Layout

Device Address Selection

The DZV11 is software-controlled by six device registers, listed in Table 25-1. The device address is the address assigned to the control and status register (CSR). The DZV11 device address must be selected from the floating address space (760010 to 763776) and is configured by setting the rocker switches of switchpack E30. The switch to address bit assignments are shown in Figure 25-2. The DZV11 is factory-configured for a device address of 760010.

Table 25-1 ▪ DZV11 Register Address Assignments

Register	Mnemonic	Address*
Control and Status Register	CSR (R/W)	76XXX0
Receiver Data Buffer	RBUF (R-O)	76XXX2
Line Parameter Register	LPR (W-O)	76XXX2
Transmitter Control Register	TCR (R/W)	76XXX4
Modem Status Register	MSR (R-O)	76XXX6
Transmit Data Register	TDR (W-O)	76XXX6

* XXX = Selected in accordance with floating-device address scheme.

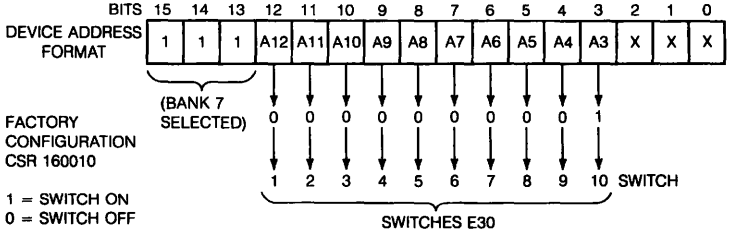


Figure 25-2 ▪ DZV11 Device Address Selection

Interrupt Vector Selection

The DZV11 interrupt vector address must be selected from the floating vector space (300 to 774) and is configured by setting the rocker switches of switchpack E2. The switch to address bit assignments are shown in Figure 25-3. The DZV11 is factory-configured for an interrupt vector of 300.

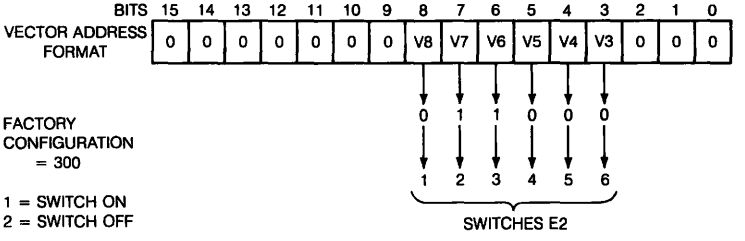


Figure 25-3 ▪ DZV11 Interrupt Vector Selection

- MODEM CONTROL

  There are eight jumpers on the DZV11 used for modem control. Jumpers W1 and W4 connect Data Terminal Ready (DTR) to Request To Send (RTS). This allows the DZV11 to assert both DTR and RTS when using a modem that requires the control of RTS. These jumpers must be installed to run the external cable and test diagnostic programs. Jumpers W5 through W8 connect the forced-busy (FB) leads to the request-to-send (RTS) leads. When these jumpers are installed, the assertion of an RTS signal places an ON or BUSY signal on the corresponding forced-busy lead. Forced-busy jumpers W5-W8 are normally removed unless they are required for the modem. These modem control jumpers are listed in Table 25-2.

Table 25-2 ▪ DZV11 Modem Control Jumpers

Jumper	Connection	Line
W1	DTR to RTS	3
W2	DTR to RTS	2
W3	DTR to RTS	1
W4	DTR to RTS	0
W5	RTS to FB	3
W6	RTS to FB	2
W7	RTS to FB	1
W8	RTS to FB	0

- BUS SIGNALS

  Jumpers W10 and W11 must remain installed when the module is used in a Q/Q-type backplane (such as the H9270) that supplies Q-bus signals to the CD connectors. When the module is used in a Q/CD-type backplane (such as the H9273) that uses the CD interconnect scheme, jumpers W10 and W11 must be removed. (See Chapter 52 for a discussion of Q/Q and Q/CD backplanes.)

- TESTING

  Jumper W9 and jumpers W12 through W16 are only removed for manufacturing test purposes. These jumpers should not be removed by the user.

▪ Cables, Connectors, and Cabinet Kits

The DZV11 interface module comes with a BC11U-25 interface cable and two accessory test connectors (H329 and H325). The H320 connector permits a staggered loopback. The H325 connector is used with the BC11U cable to provide the single-line loopback.

When ordered at the same time as the system in which it is to be installed, the DZV11 interface option (model number DZV11-DP) includes the base module (M7957), internal cables, and the I/O connection panel insert.

When ordered as a system upgrade, the DZV11 interface option (model number DZV11-M) includes the base module only. One of the following cabinet kits should be chosen for system installation:

CK-DZV11-DA	For use with the BA11-MA(MB) enclosure
CK-DZV11-DB	For use with the BA23 enclosure
CK-DZV11-DC	For use with the H349 distribution panel
CK-DZV11-D3	For use with CPUs that do not have an I/O connection panel. Kit contains a 25-ft cable that connects the DZV11-M module to four RS-232 devices.

Chapter 26 • KMV11-A Programmable Communications Controller

The KMV11-A is a medium-speed programmable data communications interface for Q-bus based systems. It is available in three options, as listed below.

KMV11-AA	Single communications line with an RS-232C (V.23) compatible interface
KMV11-AE	Single communications line with an RS-422A (V.11) interface
KMV11-AF	Single communications line with an RS-423A (V.10) interface

• Specifications

Identification	M7500
Size	Quad
Power Requirements	+5 Vdc at 2.6 A +12 Vdc at 0.2 A
Bus Loads	
ac	3.0
dc	1.0

• Related Documentation

Document Title	**Order Number**
KMV11 Programmable Communications Controller Technical Manual	EK-KMV11-TM
KMV11 Programmable Communications Controller User's Guide	EK-KMV11-UG
KMV11 Field Maintenance Print Set	MP-01173-00
RX01 Diagnostic Kit	ZJ360-PY
Communications Mini-reference Guide	EK-CMINI-RM

• Configuration

The KMV11-A base module is configured with fourteen wirewrap jumpers and three switchpacks. The locations of these jumpers and switchpacks are shown in Figure 26-1; Table 26-1 lists their functions and factory configurations.

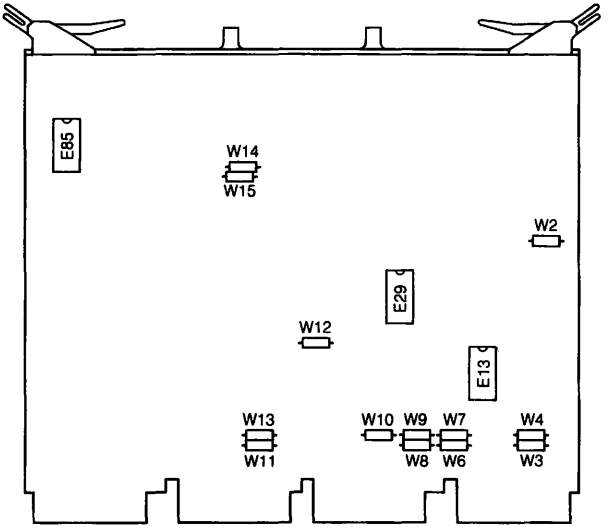


Figure 26-1 ▪ KMV11-A Jumper and Switch Locations

Table 26-1 ▪ KMV11-A Jumper and Switch Functions

Jumpers/Switches	Function
E29 (S1-S9)	These switches are used to configure the device address. The module is factory-configured for a device address of 776020.
E13 (S1-S7)	These switches are used to configure the vector address. The module is factory-configured for a vector address of 320.
E29 (S10) E13 (S8)	These two switches are used to enable or disable the module self-test feature. They are factory-configured for one-pass self-test at powerup.

(continued on next page)

Table 26-1 ▪ KMV11-A Jumper and Switch Functions (Cont.)

Jumpers/Switches	Function
W3, W4, W7-W10	These jumpers are used to enable or disable the extended address lines <16:21> on the Q-bus. They are all factory-installed, thereby enabling the address lines.
W6	This jumper is used to connect or disconnect the BDCOK signal from the Q-bus. It is factory-removed, thereby disconnecting the signal.
W11 and W13	These two jumpers are installed to provide bus grant continuity signals in the C and D connectors of the backplane. They are factory-installed.
W2	This jumper is used to enable or disable the DMA clock. It is factory-installed to enable the clock.
W12	This jumper is used to enable or disable the microprocessor clock. It is factory-installed to enable the clock.
E85 (S1-S10)	These switches are used to select the type of interface. They are factory-configured according to the KMV11 option chosen.
W15	This jumper is used to enable or disable permanent assertion of the carrier detect signal. It is factory-removed to disable this feature.
W14	This jumper is used to connect the terminal-in-service signal to the turn-around connector during loopback testing. It is factory-removed for normal operation.

Device Address Switches

The KMV11-A is controlled via eight contiguous control and status registers. The device address of the module is the address assigned to the first of these eight registers. The KMV11-A device should be selected from the floating address space and configured on the module using switches S1 through S9 of switchpack E29, as shown in Figure 26-2. A switch in the ON position encodes a logical 1 in the corresponding address bit; a switch in the OFF position encodes a logical 0. The KMV11-A is factory-configured with a device address of 760020.

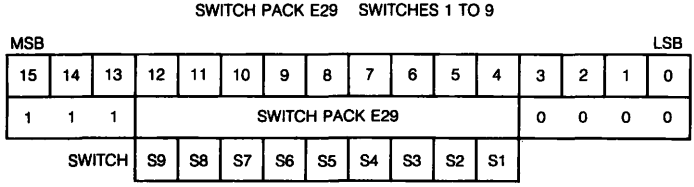


Figure 26-2 ▪ KMV11-A Device Address Selection

Interrupt Vector Address Switches

The KMV11-A can generate one interrupt and therefore requires one interrupt vector. The vector address should be assigned within the floating vector space and configured on the module using switches S1 through S7 of switchpack E13, as shown in Figure 26-3. A switch in the ON position encodes a logical 1 in the corresponding address bit; a switch in the OFF position encodes a logical 0. The KMV11-A is factory-configured with a vector address of 320.

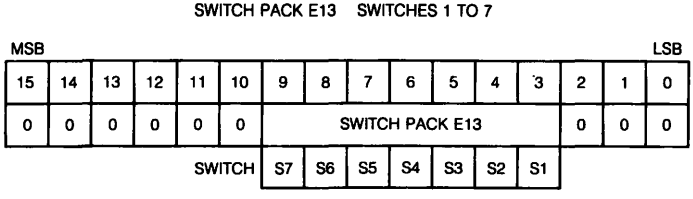


Figure 26-3 ▪ KMV11-A Vector Address Selection

Self-test Switches

The remaining switches in switchpacks E13 and E29 are used to select the desired type of self-test to be used by the KMV11-A. The configuration of these switches is listed in Table 26-2.

Table 26-2 ▪ KMV11-A Self-Test Switch Configuration

E13 (S8)	E29 (S10)	Self-test Option
ON	ON	Self-test disabled
ON	OFF	Self-test started via CSR command or at power-up; one pass
OFF	OFF	Self-test started manually; endless loop
OFF	ON	Extended self-test; endless loop

Extended Address Jumpers
Jumpers W3, W4, and W7 through W10 are normally installed to allow extended addressing on Q-bus lines BDAL <16:21>. They should only be removed when the extended address lines (SPARE lines in older Q-bus configurations) are in conflict with existing signals on those lines.

BDCOK Jumper
Jumper W6 is used to connect or disconnect the BDCOK signal from the Q-bus. This jumper should not be installed since the use of the BDCOK signal is not supported by the KMV11-A

Bus Continuity Jumpers
Jumpers W11 and W13 are used to provide bus grant signal (BIAK and BDMG) continuity across the C and D connectors. They should be installed when the KMV11-A module is installed in a Q/Q-type backplane, and removed when the module is installed in a Q/CD-type backplane (see Chapter 52).

Factory Test Jumpers
Jumper W2 (DMA clock) and jumper W12 (microprocessor clock) are factory test jumpers and should remain installed for normal KMV11-A operation.

Modem Signal Switches and Jumpers
Switches S1 through S8 of switchpack E85 are used to select the desired communications interface. Table 26-3 lists the configurations of these switches; all other configurations are illegal.

Setting switch S9 of E85 to the ON position connects pin 29 of the connector assemblies to CCITT 107-. It should be set to the OFF position only when the modem connects a different signal to this pin.

Setting switch S10 of E85 to the ON position connects pin 2 of the connector assemblies to CCITT 112. It should be set to the OFF position only when the modem connects a different signal to this pin.

Installing jumper W15 permanently asserts CCITT 109 (Carrier Detect). This jumper should normally be removed.

Installing jumper W14 connects pin 28 of the connector assemblies to the Terminal in Service modem signal. This signal is not used by most modems, but is required for loopback testing using the H3251 turn-around connector. It should be removed only when the modem connects a different signal to pin 28.

Table 26-3 ▪ KMV11-A Interface Switches

Interface	S1	S2	S3	S4	S5	S6	S7	S8
RS-422A	ON	ON	ON	ON	OFF	OFF	OFF	OFF
RS-423	OFF	OFF	OFF	OFF	ON	ON	ON	ON
RS-232	OFF	OFF	OFF	OFF	ON	ON	ON	ON

Note

All other switch configurations are illegal.

▪ Cables and Connectors

To install modem cable assemblies properly, the H349 bulkhead connector panel with unoccupied slots J12, J13, J14, or J15 should be available. Otherwise, the cable assembly may be screwed directly to the vertical cabinet mounting rails, selecting a proper location where the EIA spaced holes of the mounting rails match the holes of the connector assembly.

The KMV11 options come with the following cables and connectors:

KMV11-AA	BC55H RS-232 cable assembly H325 Cable turn-around connector RS-232
KMV11-AE	BC55U RS-422 cable assembly H3251 Cable turn-around connector RS-449
KMV11-AF	BC55P RS-423 cable assembly H3251 Cable turn-around connector RS-449

Before installing the BC55H, BC55U, or BC55P, verify and configure the appropriate modem lead jumpers, as listed in Table 26-4.

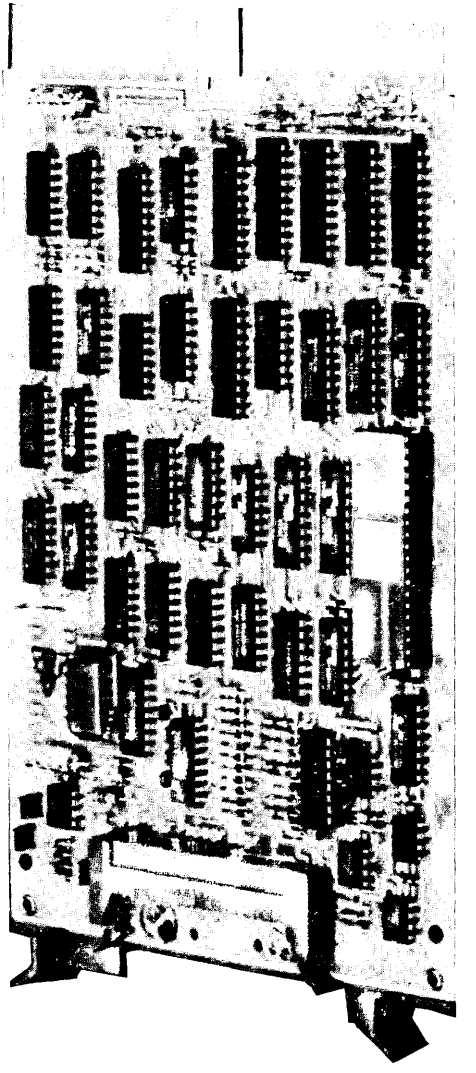
Table 26-4 ▪ KMV11 Cable Jumper Settings

J2 PIN	JUMPER	RS-232-C	BELL 103J	BELL 208B	BELL 209	DATEL 200	DATEL 600	DATEL 2400	DATEL 4800	CCITT V.21	CCITT V.23	CCITT V.26B	CCITT V.27T	ISO2110-1972	ISO2110.2	ISO2110.2	EIA RS-232-C	EIA RS-449	CCITT V.24
																FUTURE D			
																X.21 BIS			
																X.20 BIS			
23	W1	IN				IN	IN	IN		IN	IN	IN	IN	IN			CH	SR	111
21	W2	IN		IN													CG	SQ	110
11	W3				IN				IN				IN					SF	126
23	W4																CI	SF	112
16	W5	IN				IN	IN	IN		IN	IN	IN	IN	IN	IN	IN	SBB	SRD	119
14	W6	IN				IN	IN	IN		IN	IN	IN	IN	IN	IN	IN	SBA	SSD	118
12	W7	IN				IN	IN	IN		IN	IN	IN	IN	IN	IN	IN	SCF	SRR	122
21	W8								IN					IN	IN			RL	140
4	W9	IN		IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	CA	RS	105
15	W10	IN		IN	IN		IN	IN		IN	IN	IN	IN	IN			DB	ST	114
17	W11	IN		IN	IN		IN	IN		IN	IN	IN	IN	IN			DD	RT	115
18	W12								IN					IN	IN			LL	141
19	W13	IN				IN	IN	IN		IN	IN	IN	IN	IN	IN	IN	SCA	SRS	121
	W14	NOT NORMALLY INSTALLED																	
25	W15								IN					IN	IN			TM	142
24	W16	IN		IN	IN			IN			IN	IN		IN	IN	IN	DA	TT	113
25	W17						IN											SB	117
24	W18						IN											SS	116
13	W19	IN				IN	IN	IN		IN	IN	IN	IN	IN	IN	IN	SCB	SCS	121
25	W20																MAKE BUSY		
1	W21	IN	IN	IN	IN	IN	IN	IN					IN				AA		101
2																	BA	SD	103
3																	BB	RD	104
5																	CB	CS	106
6																	CC	DM	107
7																	AB	SG	102
8																	CF	RR	109
20																	CD	TR	108
22																	CE	IC	125

Once the module has been tested successfully, install modem or null modem cables as required by the application. Standard modem cables for use with the KMV11-A are listed below.

Interface	Cable	Description
RS-232C	BC05D-25	7.5 meters (25 feet); connects the modem to 25-pin cinch connector on the BC55H cable assembly
RS-423A	BC55D-33	10 meters (33 feet); connects the modem to 37-pin cinch connector on the BC55P cable assembly
RS-422A	BC55D-33	10 meters (33 feet); connects the modem to 37-pin cinch connector on the BC55U cable assembly

Part VI ▪ Synchronous Communications Interfaces



Chapter 27 • Introduction to Synchronous Communications Interfaces

Digital offers five different synchronous communications interfaces for interconnecting Q-bus systems with other local or remote computer systems.

• DEQNA Ethernet Q-bus Network Controller

The DEQNA is a high-performance synchronous communications controller that connects Q-bus systems to Ethernet local area networks (LANs). It is supported under DECnet Phase IV software and provides Ethernet data link layer functions, as well as a portion of the physical channel functions. The DEQNA allows communications with up to 1,023 addressable devices using direct memory access (DMA) data transfers at a rate of up to 10 Mbits per second. The DEQNA supports both 18- and 22-bit Q-bus addressing.

• DMV11 Synchronous Controller

The DMV11 is an intelligent synchronous line controller that provides high-speed communications for Q-bus systems in distributed networks. There are four DMV11 options supporting four different interfaces — EIA RS-232C, EIA RS-423A/449, CCITT V.35, and integral modem. Using DMA transfers, the DMV11 can operate at speeds up to 56 Kbits per second. It implements the Digital Data Communications Message Protocol (DDCMP) in either point-to-point or multipoint mode. In multipoint mode, it supports up to 12 tributaries and one control station. The DMV11 is compatible with Digital's family of modems and with Bell 200 series modems or their equivalents.

• DPV11 Serial Synchronous Line Interface

The DPV11 is a single-line programmable synchronous interface that provides local or remote interconnection between Q-bus systems and other computer systems using either the EIA RS-232C/CCITT V.28 or V.11 interface. It operates at speeds of up to 56 Kbits per second at half- or full-duplex with full modem control. The DPV11 is programmable for either byte-oriented protocols (DDCMP or BISYNC) or bit-oriented protocols (SDLC or HDLC). It is compatible with Digital's family of modems and with the Bell 200 series modems or their equivalents.

▪ DUV11 Synchronous Line Interface

The DUV11 line interface is a buffered, program-controlled, single-line communications interface used to establish a data communications line between any Q-bus system and a Bell 200 series synchronous modem or equivalent. The DUV11 is fully programmable with respect to sync characters, character length, and parity selection. It provides serial-to-parallel and parallel-to-serial data communications, buffers TTL-to-EIA and EIA-to-TTL voltage levels, and provides half- or full-duplex modem control.

▪ KMV11-A Programmable Communications Controller

The KMV11-A is a high-performance direct memory access single-line programmable communications controller that provides interconnection between Q-bus systems and other computer systems or devices. It supports the EIA RS-232C/CCITT V.28, EIA RS-422/CCITT V.11, and EIA RS-423/CCITT V.10 interfaces. The KMV11-A uses the Micro/T11 processor to perform user-defined communications functions and can be programmed to operate in either synchronous or asynchronous modes. In synchronous mode it is capable of communications speeds up to 64 Kbits per second. The KMV11-A also provides full modem support of Digital's family of modems, the Bell 200 series or equivalent, and European PPT-approved modems.

Chapter 28 ▪ DEQNA Ethernet Q-bus Network Adapter

The DEQNA Q-bus data communications controller interfaces Q-bus processors to the Ethernet local area network.

▪ Specifications

Identification	M7504
Size	Dual
Power Requirements	
DEQNA	+5 Vdc, 3.5 A (typical)
H4000 Transceiver	+12 Vdc, 0.5 A (typical)
Bus Loads	
ac	2.2
dc	0.5
Operating Mode	Half-duplex (nonloopback)
Data Format	Manchester encoded, serial
Ethernet Data Rate	10 Mbits per second

Note

In addition to the above, the DEQNA meets Ethernet Specification, version 2.0, requirements.

Nonstandard Environmental Specifications	
Operating Temperature	5°C to 50°C (41°F to 122°F)

▪ Related Documentation

Document Title	**Order Number**
H4000 Ethernet Transceiver Field Maintenance Print Set	MP-01369
H4000 Ethernet Transceiver Technical Manual	EK-H4000-TM-PRE
The ETHERNET, A Local Area Network, Data Link Layer, and Physical Layer Specifications	AA-K759A-TK
Introduction to Local Area Networks	EB-22714-18
DEQNA User's Guide	EK-DEQNA-UG
Ethernet Installation Guide	EK-ETHER-IN

▪ Configuration

The DEQNA module is configured with three jumpers, W1 through W3. The location of these jumpers is shown in Figure 28-1.

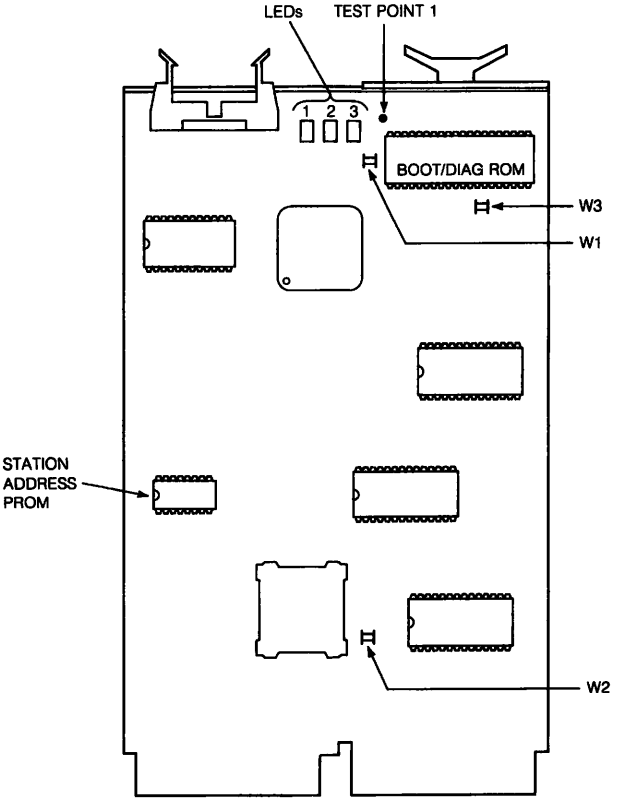


Figure 28-1 ▪ DEQNA Jumper Locations

Device Address Assignment (W1)
Each DEQNA is assigned a block of eight words on the I/O page, used as registers, and available for user program control. The base address of this 8-word block is the device address. The DEQNA is factory-configured with jumper W1 in the first position, assigning the module a device address of 17774440. If the module being installed is the second of two DEQNAs installed in the system, jumper W1 must be removed, thereby assigning the module a device address of 17774460.

Bus Request Hold-off Timer (W2)
With jumper W2 removed the bus request hold-off timer is enabled. This provides "fair" access to all DMA devices using the Q-bus. The module is shipped with this jumper removed; it should not be installed except in unusual circumstances.

Sanity Timer (W3)
Jumper W3 controls the module's "sanity" timer. The timer is enabled and periodically reset by the host software. If the host fails to reset the timer, causing the timer to time out, a system reboot is triggered.

The DEQNA is factory-configured with jumper W3 installed, disabling the sanity timer. To enable the timer, remove jumper W3.

▪ Cables and Cabinet Kits

The DEQNA physically and electrically connects to the Ethernet Coaxial Cable via Ethernet transceiver cables (BNE3C or BNE3A series) and an H4000 Ethernet Transceiver or a Local Network Interconnect (DELNI). The transceiver cable can be a maximum of 45 meters (148 feet) in length for the BNE3x series cable or 11.25 meters for the BNE4x series cable.

When ordered at the same time as the system in which it is to be installed, the DEQNA option (model number DEQNA-KP) includes the base module (M7504), internal cables and the I/O connection panel insert.

When ordered as a system upgrade, the DEQNA option (model number DEQNA-M) includes the base module only. One of the following cabinet kits should be chosen for system installation:

CK-DEQNA-KA	For use with the BA11-MA(MB) enclosure
CK-DEQNA-KB	For use with the BA23 enclosure
CK-DEQNA-KC	For use with the H349 distribution panel

Chapter 29 ▪ DMV11 Synchronous Controller

The multipoint DDCMP-DMV11 Intelligent Communications Synchronous Line Controller is an interface device which provides high-speed synchronous communications for distributed networks.

There are four available DMV11 options, as listed in Table 29-1.

Table 29-1 ▪ Available DMV11 Options

Option	Interface	Line Speed
DMV11-AP	EIA RS-232C/CCITT V.28	Up to 19.2 Kbits/s
DMV11-BP	CCITT V.35/DDS	Up to 56 Kbits/s
DMV11-CP	Integral modem	56 Kbits/s only
DMV11-FP	EIA RS-423A/CCITT V.24	Up to 56 Kbits/s

▪ Specifications

Identification	
-AP, -BP, -FP	M8053
-CP	M8064
Size	Quad
Power Requirements	
-AP, -BP, -FP	+5 Vdc, at 4.7 A (typical) +12 Vdc, at 0.380 A (typical)
-CP	+5 Vdc, at 4.4 A (typical) +12 Vdc, at 0.260 A (typical)

Note

-12 V (at 250 mA), required by the level conversion logic of both modules, is generated off the +12 V by a switching inverter.

Bus Loads	
ac	2.0
dc	1.0
Performance	
Operating Mode	Full- or half-duplex
Data Format	Synchronous DDCMP
Data Rates	Up to 56 Kbits/s
Tributaries Supported	Up to 12

Nonstandard Environmental Specifications	
Operating Temperature	5°C to 50°C (41°F to 122°F)

▪ Related Documentation

Document Title	**Order Number**
QMA DMV11 Synchronous Controller User's Guide	EK-DMVQM-UG
QMA DMV11 Synchronous Controller Technical Manual	EK-DMVQM-TM
DMV11 Field Maintenance Print Set	MP-00942-00
DMV11 Diagnostic Documentation Kit	ZJ328-RZ

▪ Configuration

The DMV11 is configured by means of four switchpacks on each module. Figures 29-1 and 29-2 show the locations of these switchpacks for the M8053 and the M8064 modules, respectively.

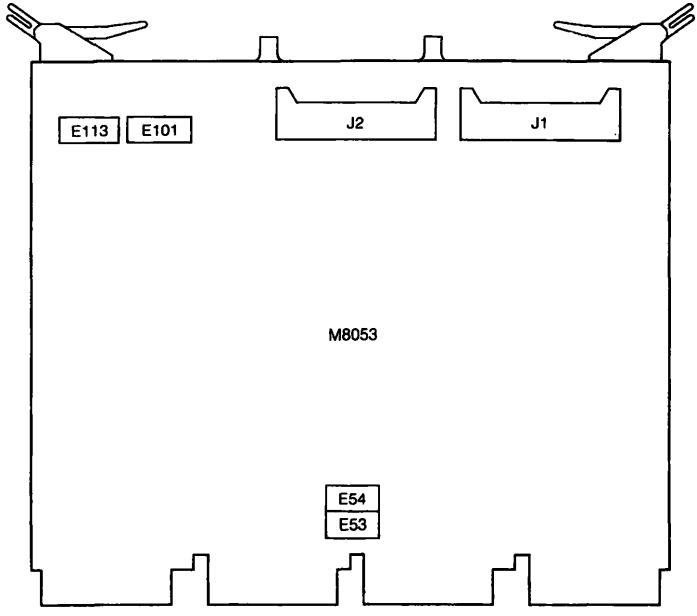


Figure 29-1 ▪ DMV11 Switch Locations (M8053 Module)

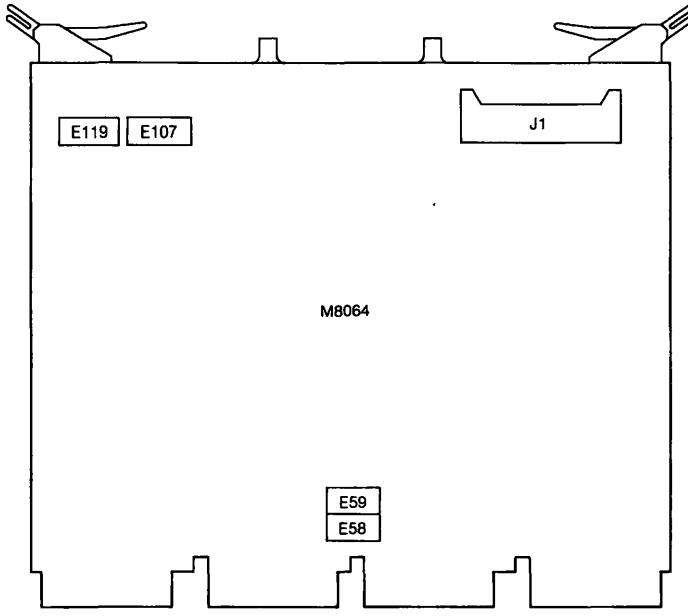
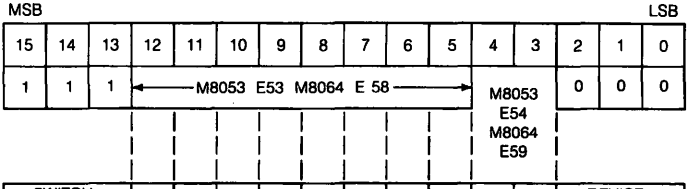


Figure 29-2 ▪ DMV11 Switch Locations (M8064 Module)

Device Address

Four contiguous 16-bit control and status registers are used for software control of the DMV11. The device address is the address assigned to the first of these registers. The DMV11 device address should be selected from the floating address space (160010 through 163776) and is configured by means of the address-selection switchpacks on the module, as shown in Figure 29-3. The M8053 device address is configured using switches E53-S1 through E53-S8, E54-S1, and E54-S2; the M8064 device address is configured using switches E58-S1 through E58-S8, E59-S1, and E59-S2.

A switch in the ON position encodes a logical 1 in the corresponding address bit; a switch in the OFF position encodes a logical 0.



SWITCH NUMBER	S8	S7	S6	S5	S4	S3	S2	S1	S2	S1	DEVICE ADDRESS
									ON		760020
								ON			760040
								ON	ON		760060
							ON				760100 ...
						ON					760200 ...
						ON	ON				760300 ...
					ON						760400 ...
					ON		ON				760500 ...
					ON	ON					760600 ...
					ON	ON	ON				760700 ...
				ON							761000 ...
			ON								762000 ...
			ON	ON							763000 ...
		ON									764000

NOTE: SWITCH ON RESPONDS TO LOGICAL ONE ON THE BUS

Figure 29-3 ▪ DMV11 Device Address Selection

Interrupt Vector Address

The DMV11 interrupt vector address should be selected from the floating vector space (300 through 774), and is configured by means of the address selection switchpack on the module, as shown in Figure 29-4. The M8053 vector address is configured using switches E54-S3 through E54-S8; the M8064 vector address is configured using switches E59-S3 through E59-S8.

A switch in the ON position encodes a logical 1 in the corresponding address bit; a switch in the OFF position encodes a logical 0.

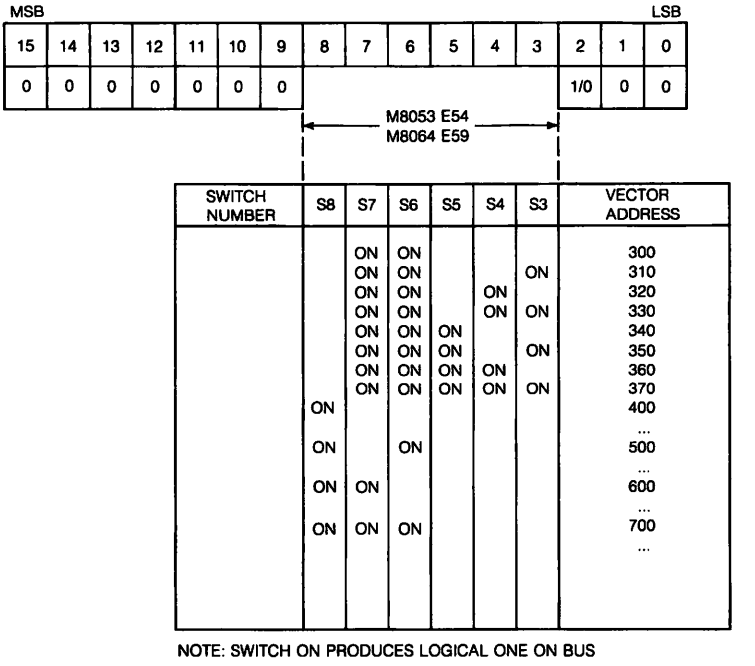


Figure 29-4 ▪ DMV11 Vector Address Selection

Tributary Address

The DMV11 can be used in either point-to-point or multipoint applications. In multipoint applications, each tributary has a unique address that is either assigned by the software or set in the hardware using the address register switchpack. On the M8053 module, this is switchpack E113; on the M8064, it is switchpack E119 (see Figure 29-1).

A switch in the OFF position encodes a 1 in the corresponding bit position of the address register. Any nonzero 8-bit number can be selected as long as it is unique within the network. If the tributary address is to be assigned by the software, the address register switchpack should be set to 0.

Switch-Selectable Features

Switchpacks E107 (on the M8053) and E101 (on the M8064) are used to select other optional features, as shown in Figure 29-5 and discussed in the following subsections.

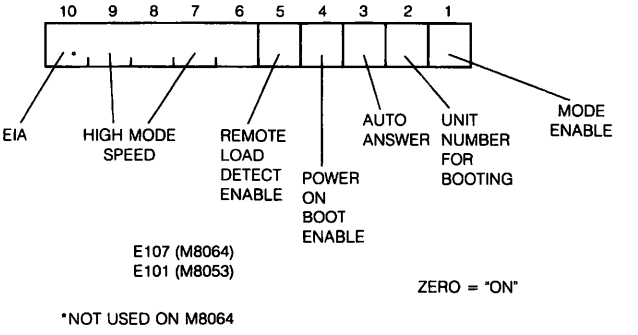


Figure 29-5 ▪ DMV11 Switch-selectable Features

- MODE OF OPERATION

If switch 1 is set to the OFF position, the DMV11's mode of operation is established from switches 6 through 8 (as shown in Table 29-2) when the device is initialized. If switch 1 is set to ON, the mode of operation must be selected by the software.

Table 29-2 ▪ DMV11 Mode Switch Settings

Switch Settings 6	7	8	Line Mode	DMC11 Line Compatible	Network Configuration
ON	ON	ON	Half-duplex	Yes	Point-to-point
OFF	ON	ON	Full-duplex	Yes	Point-to-point
ON	OFF	ON	Half-duplex	No	Point-to-point
OFF	OFF	ON	Full-duplex	No	Point-to-point
ON	ON	OFF	Half-duplex	n/a	Multipoint control station
OFF	ON	OFF	Full-duplex	n/a	Multipoint control station
ON	OFF	OFF	Half-duplex	n/a	Multipoint tributary station
OFF	OFF	OFF	Full-duplex	n/a	Multipoint tributary station

- BOOT UNIT NUMBER
  If two DMV11s are installed on the same Q-bus, switch 2 selects which of the two units is to perform a remote boot. When the switch is in the ON position, unit 0 is selected; when it is in the OFF position, unit 1 is selected.

- AUTOANSWER
  When switch 3 is in the OFF position, the autoanswer feature of the DMV11 is enabled. This causes the DMV11 to assert DTR and wait for the modem ready signal (DSR). DSR is the indication that a call has been established. If a valid DDCMP message is not received within 30 seconds after a connection is established, DTR is dropped and the phone line is hung up. This sequence permits the DMV11 to automatically answer all incoming calls to the computer.

- POWERON BOOT ENABLE
  When switch 4 is in the OFF position, the poweron boot feature is enabled at the remote/tributary station. The node that is to receive the boot requests the host station to start the primary MOP boot procedure. The boot request is sent out when the first poll message is complete following the remote station's powerup sequence.

- REMOTE LOAD DETECT ENABLE
  When switch 5 is in the OFF position, the remote load detect boot feature is enabled at the remote/tributary station. The host node starts the booting sequence by sending the primary MOP boot procedures.

- HIGH-SPEED SWITCH
  When switch 9 is in the OFF position, the baud rate of the DMV11 is set to "high speed" — 19,200 bits per second or greater. When the switch is in the ON position, the baud rate must be lower than 19,200 bits per second.

Note

Switch 9 is always in the OFF position on the M8064 module.

- INTERFACE SELECT SWITCH
  When switch 10 is in the ON position, the CCITT V.35 modem interface is selected. When the switch is in the OFF position, the EIA RS-232C or RS-423A modem interfaces are selected.

Note

Switch 10 is not used on the M8064 module.

▪ Cables and Cabinet Kits

The following external cables are recommended for use with the various DMV11 options:

DMV11-AP	BC22E fully shielded 16-connector asynchronous modem cable with one male and one female RS-232 connector or BC22F fully shielded 25-conductor EIA cable with one male and one female RS-232 connector
DMV11-BP	BC17E 26-conductor, fully shielded V.35 modem cable assembly with one 34-position male and one 37-position female D-subminiature connector*
DMV11-CP	BC55S integral modem interface cable or BC55T integral modem interface cable†
DMV11-FP	BC55D external cable

* The BC17E external cable is included with the DMV11-BP option.

† To connect the BC55S or BC55T to the older BC55M or BC55N cables, BC56A/B/C/D adapter cables are available.

When ordered at the same time as the system in which they are to be installed, the DMV11 options include the base module (M8053 or M8064), internal cables, and the I/O connection panel insert.

When ordered as a system upgrade, the various options include the base module only. One of the following cabinet kits should be chosen for system installation:

DMV11-AP (Upgrade model number DMV11-M)

CK-DMV11-AA	For use with the BA11-MA(MB) enclosure
CK-DMV11-AB	For use with the BA23 enclosure
CK-DMV11-AC	For use with the H349 distribution panel
CK-DMV11-A2	For use with CPUs that do not have an I/O connection panel. Kit contains a 25-ft cable that connects the DMV11-M module to an external device.

DMV11-BP (Upgrade model number DMV11-N)

CK-DMV11-BA	For use with the BA11-MA(MB) enclosure*
CK-DMV11-BB	For use with the BA23 enclosure*
CK-DMV11-BC	For use with the H349 distribution panel*
CK-DMV11-B3	For use with CPUs that do not have an I/O connection panel. Kit contains a 25-ft cable that connects the DMV11-M module to an external device.

DMV11-CP (Upgrade model number DMV11-N)

CK-DMV11-CA	For use with the BA11-MA(MB) enclosure
CK-DMV11-CB	For use with the BA23 enclosure
CK-DMV11-CC	For use with the H349 distribution panel
CK-DMV11-C3	For use with CPUs that do not have an I/O connection panel. Kit contains a 25-ft cable that connects the DMV11-M module to an external device.

DMV11-FP (Upgrade model number DMV11-M)

CK-DMV11-FA	For use with the BA11-MA(MB) enclosure
CK-DMV11-FB	For use with the BA23 enclosure
CK-DMV11-FC	For use with the H349 distribution panel
CK-DMV11-F3	For use with CPUs that do not have an I/O connection panel. Kit contains a 25-ft cable that connects the DMV11-M module to an external device.

* These cabinet kits include the BC17E V.35 modem cable.

Chapter 30 • DPV11 Serial Synchronous Line Interface

The DPV11 is a serial synchronous line interface for connecting a Q-bus to a serial synchronous modem that is compatible with EIA RS-232C interface standards, as well as EIA RS-423A and EIA RS-422A electrical standards.

• Specifications

Identification	M8020
Size	Dual
Power Requirements	+5 V, 1.2 A (maximum), 0.92 A (typical) +12 V, 0.30 A (maximum), 0.15 A (typical)
Bus Loads	
ac	1.0
dc	1.0
Performance	
Operating Mode	Full- or half-duplex
Data format	Synchronous BISYNC, DDCMP, and SDLC
Character size	Program-selectable (5-8 bits with character-oriented protocols and 108 bits with bit-oriented protocols)
Maximum configuration	16 DPV11 modules per Q-bus
Maximum distance	15 m (50 ft) for RS-232C; 61 m (200 ft) for RS-423A/RS-422A. (Distance is directly dependent on speed, and 200 ft is a suggested average. See RS-449 specifications for details.)
Maximum serial data rates	56 Kbits per second. (Can be less due to software and memory refresh limitations.)

▪ Related Documentation

Document Title	Order Number
DPV11-DA Configuration Guide	EK-DPV11-CG
DPV11 Synchronous Interface User's Guide	EK-DPV11-UG
DPV11 Technical Manual	EK-DPV11-TM
DPV11 Field Maintenance Print Set	MP-00919-00
DPV11 Diagnostic Documentation Kit	ZJ314-RZ
Communications Mini-reference Guide	EK-CMINI-RM

▪ Configuration

The DPV11 is configured by inserting or removing jumpers so that the module will function properly within the system. The locations of the jumpers are shown in Figure 30-1. The standard factory configuration is RS-423A-compatible, while the alternate configuration suggested throughout the text is typically RS-422A-compatible.

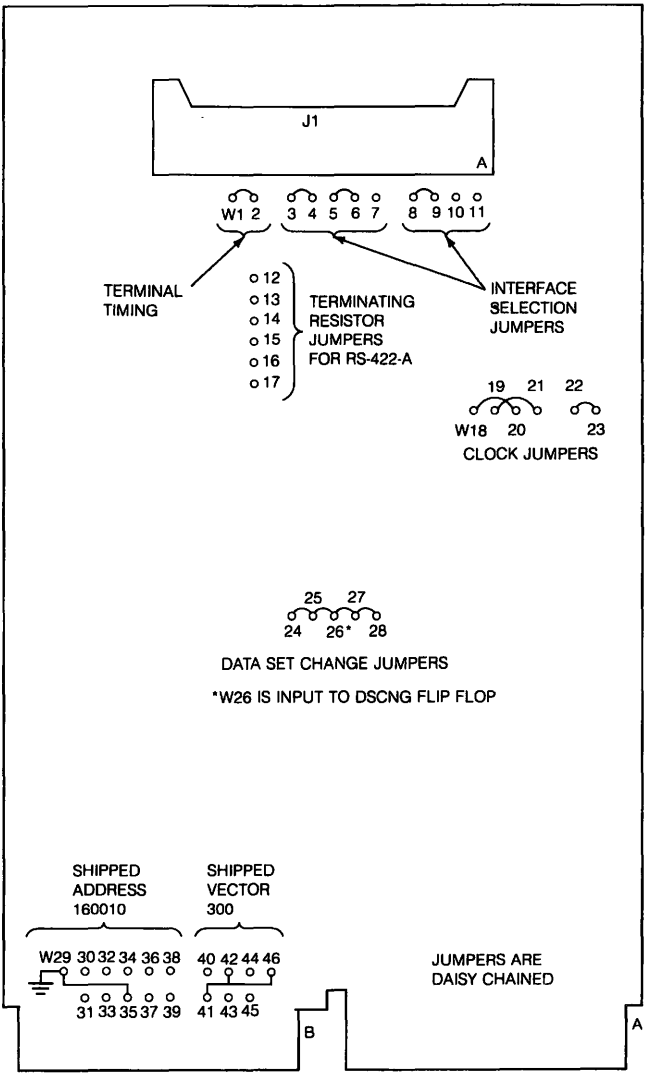


Figure 30-1 ▪ DPV11 Jumper Locations

Device Address

The five registers used in the DPV11 are listed in Table 30-1. The device address is that address assigned to the receiver control and status register. The DPV11 device address should be selected from the range between 160000 and 177770, and is configured using jumper pins W29 through W39. Any jumper connected to pin W29 (ground) is decoded as a logical 1 in the corresponding address bit. The bit assignments for the jumpers are shown in Figure 30-2.

The DPV11 is factory-configured with a device address of 160010.

Table 30-1 ▪ DPV11 Standard Addresses

Description	Mnemonic	Status	Address
Registers:			
Receive Control and Status	RXCSR	R/W	160010
Receive Data and Status	RDSR	R-O	160012
Parameter Control Sync/Address	RCSAR	W-O	160012
Parameter Control/Char Length	PCSCR	R/W	160014
Transmit Data and Status	TDSR	R/W	160016
Interrupt Vectors:			
Break			300

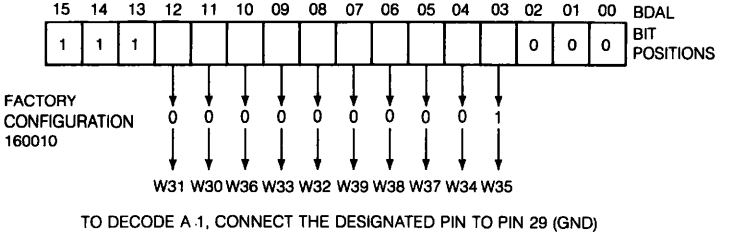


Figure 30-2 ▪ DPV11 Device Address Selection

Interrupt Vector Address

The DPV11 interrupt vector address can be selected in the range of 300 to 760, and is configured using jumper pins W40 through W46. Any jumper connected to pin W46 (ground) is decoded as a logical 1 in the corresponding address bit. The bit assignments for the jumpers are shown in Figure 30-3.

The DPV11 is factory-configured for a vector address of 300.

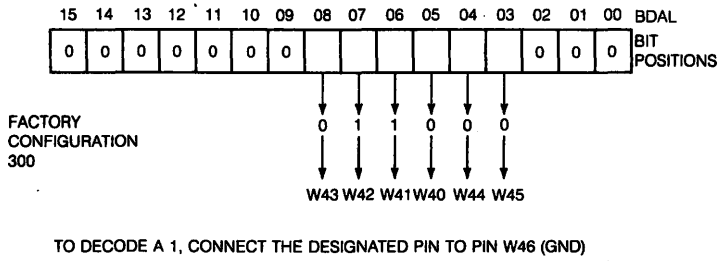


Figure 30-3 ▪ DPV11 Vector Address Selection

Driver Attenuation Jumper

The DPV11 is shipped with a jumper installed between pins W1 and W2. This bypasses the attenuation resistor of the terminal timing driver. This jumper must be removed for certain modems to operate properly.

Interface Selection Jumpers

Jumpers W3 through W11 are the interface selection jumpers. They are used to alter certain input signals according to the interface used. The configuration of these jumpers is listed in Table 30-2.

Table 30-2 ▪ DPV11 Interface Selection Jumpers

Jumper Connection	Input Signals	Description
W5 to W6*	SQ/TM (PCSCR bit 5)	Signal quality
W7 to W6	SQ/TM (PCSCR bit 5)	Test mode
W10 to W9	DM (DSR)	Data mode return (RS-422A)
W3 to W4*	SF/RL (RXCSR bit 0)	Select frequency
W5 to W3	SF/RL (RXCSR bit 0)	Remote loopback
W8 to W9*	Local loopback	Local loopback
W8 to W11	Local loopback	Local loopback (alternate pin)

* Factory configuration

Receiver Termination Jumpers

Jumpers W12 through W17 are used to connect terminating resistors for RS-422A compatibility, as listed in Table 30-3. The DPV11 is factory-configured with none of these jumpers installed.

Table 30-3 ▪ DPV11 Receiver Termination Jumpers

Jumper Connection	Description
W12 to W13	Receive data
W14 to W15	Send timing
W16 to W17	Receive timing

Clock Jumpers

Jumpers W18 through W23 are used to configure the clock, as shown in Table 30-4.

Table 30-4 ▪ DPV11 Clock Jumpers

Jumper Connection	Description
W20 to W18*	Sets the NULL MODEM CLK to 2 kHz
W21 to W18	Sets the NULL MODEM CLK to 50 kHz
W19 to W21 W22 to W23	Enable clock (always installed except for factory testing)

* Factory configuration

Data Set Jumpers

Jumpers W24 to W28 are used to connect the data set change (DSCNG) flip-flop to the respective modem status signal for transition detection, as shown in Table 30-5. W26 is input to the DSCNG flip-flop.

Table 30-5 ▪ DPV11 Data Set Jumpers

Jumper Connection	Modem Status Signal
W26 to W24*	Data Mode (DSR)
W26 to W25*	Clear to Send
W26 to W27*	Incoming Call
W26 to W28*	Receiver Read (Carrier Detect)

* Factory configuration

• Cables and Cabinet Kits

The following external cable is recommended for use with the DPV11 module:

BC26L	Modem cable with 40-pin Berg connector on one end and a male RS-232 connector on the other end; available in 25-ft (7.62-m) and 50-ft (15.24-m) lengths

When ordered at the same time as the system in which it is to be installed, the DPV11 option (model number DPV11-AP) includes the base module (M8020), internal cables, and the I/O connection panel insert.

When ordered as a system upgrade, the DPV11 option (model number DPV11-M) includes the base module only. One of the following cabinet kits should be chosen for system installation:

CK-DPV11-AA	For use with the BA11-MA(MB) enclosure
CK-DPV11-AB	For use with the BA23 enclosure
CK-DPV11-AC	For use with the H349 distribution panel
CK-DPV11-A3	For use with CPUs that do not have an I/O connection panel. Kit contains a 25-ft cable that connects the DPV11-M module to an external device.

Chapter 31 • DUV11 Line Interface

The DUV11 line interface is a program-controlled communications interface that provides a single synchronous, asynchronous, or isochronous serial data channel for Q-bus systems.

• Specifications

Identification	M7951
Size	Quad
Power Requirements	+5 Vdc ±5% at 1.2 A (typical) +12 Vdc ±3% at 0.45 A (typical)
Bus Loads	
ac	3.9
dc	1.0

• Related Documentation

Document Title	Order Number
DUV11 Line Interface User's Manual	EK-DUV11-OP
DUV11 Line Interface Technical Manual	EK-DUV11-TM
DUV11 Field Maintenance Print Set	MP-00297-00
DUV11-DA Diagnostic Documentation Kit	ZJ237-RZ
Communications Mini-reference Guide	EK-CMINI-RM

• Configuration

The DUV11 module contains four sets of switches used to select the device address, interrupt vector address, and various special control functions. The locations of these switches are shown in Figure 31-1.

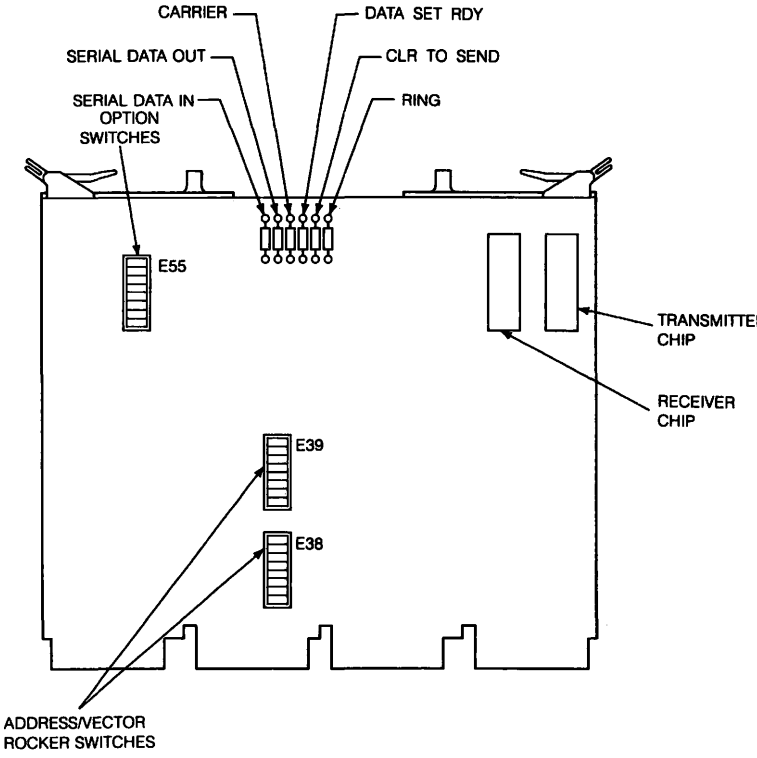


Figure 31-1 ▪ DUV11 Switch Locations

Device Address

The DUV11 is software-controlled by means of five device registers, listed in Table 31-1. The device address is the address assigned to the first of these registers. Electrically, the DUV11 can have any device address in the range 160000 to 177760. However, Digital software requires that the device address fall within the floating address space of 160010 to 163776. If an address is selected that falls outside the floating address range, the software must be modified accordingly.

The DUV11 device address is configured with switches 1 through 8 of switchpack E38 and switches 1 and 2 of switchpack E39, as shown in Figure 31-2. The device address is factory-configured to 160010 to facilitate manufacturing testing.

Table 31-1 ▪ DUV11 Factory-Configured Addresses

Description	Mnemonic	Status	Address
Registers:			
Receiver Status	RXCSR	R/W	160010
Receiver Data Buffer*	RXDBUF	R-O	160013
Parameter Status*	PARCSR	W-O	160012
Transmitter Status	TXCSR	R/W	160014
Transmitter Data Buffer	TXDBUF	W-O	160016
Interrupt Vectors:			
Done	DONE		440

* Dual-purpose read or write register (byte-addressable)

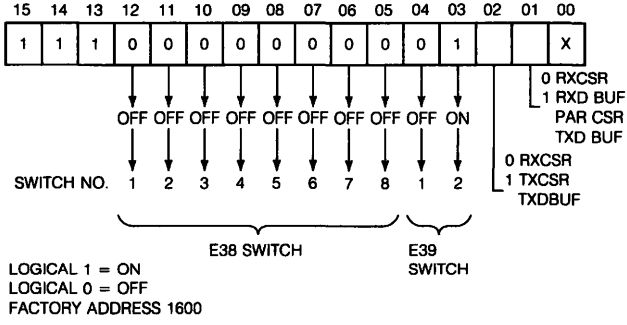


Figure 31-2 ▪ Device Address Selection

Interrupt Vector Address

The DUV11 interrupt vector address is configured using switches 3 through 8 of switchpack E39, as shown in Figure 31-3. Vectors can be assigned anywhere in the range of 000 to 774. Digital software, however, requires the vector address to be in the floating vector space, from 300 to 774. If an address is selected that falls outside this range, the software must be modified accordingly.

The DUV11 is factory-configured for a vector address of 440.

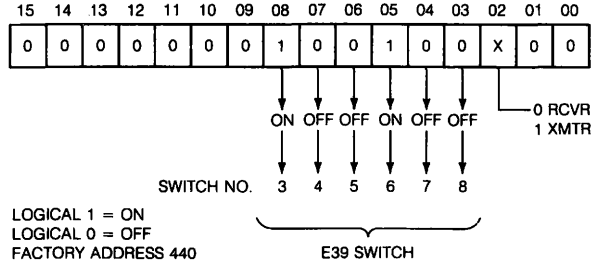


Figure 31-3 ▪ DUV11 Interrupt Vector Selection

Option Switches

The DUV11 can be configured for various optional control functions by using switches 1 through 8 of E55. The detailed operation of these switches is listed in Table 31-2.

Table 31-2 ▪ DUV11 Option Switch Assignments

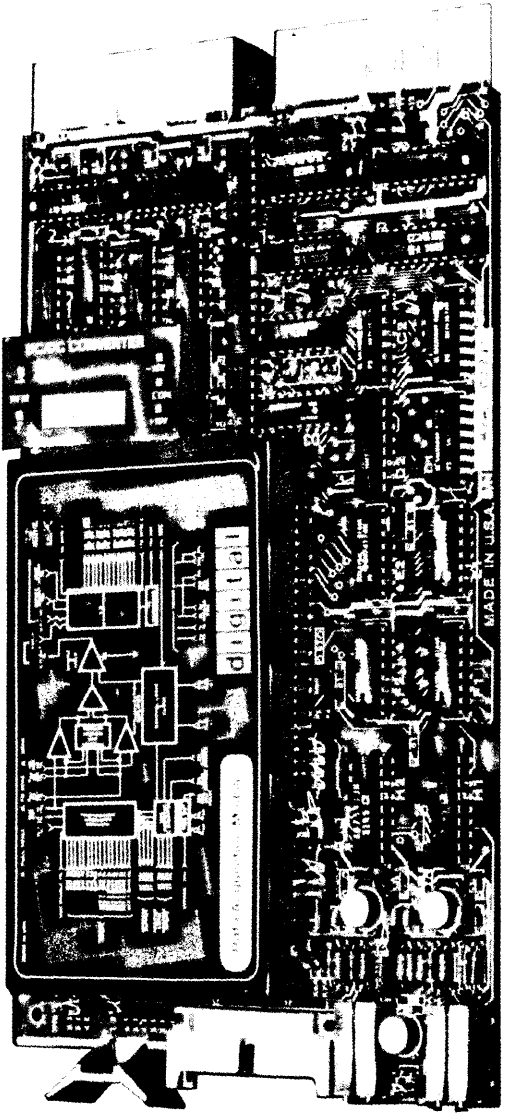
Switch	Function
E55-1	Optional Clear—Switch ON enables CLR OPT, which is used to clear RXCSR bits 3, 2, and 1.
E55-2	Secondary Transmit—Switch ON enables secondary data channel between the modem and DUV11.
E55-3	Secondary Receive—Switch ON enables secondary data channel between the modem and DUV11.
E55-4	Sync Characters—Switch ON enables the receiver to synchronize internally upon receiving one sync character. Two sync characters are required when the switch is OFF (the normal condition).
E55-5	Special Feature—Switch ON allows external clock to be internally generated; used when a modem is not being utilized.
E55-6	Special Feature—Optional feature is switched ON for program control of data rate selection.
E55-7	Maintenance Clock—Switch ON enables the clock that is used for maintenance purposes only.
E55-8	Not used.

▪ Cables

The following external cable is recommended for use with the DUV11 module:

BC05C	Round, 25-conductor cable with a male RS-232 connector on one end and a H856 mating connector on the other end

Part VII • Analog Interfaces



Chapter 32 • Introduction to Analog Interfaces

Digital offers three options for interfacing analog instrumentation to Q-bus systems.

- AAV11-C digital-to-analog output board, with four individually addressable digital-to-analog converters (DACs).
- ADV11-C analog-to-digital input board, with 16 single-ended or 8 differential analog input channels.
- AXV11-C analog input/output board with 16 single-ended or 8 differential input channels and two digital-to-analog output converters.

These three options have the following features in common:

- 12-bit digital resolution
- Selectable unipolar or bipolar I/O, with unipolar voltages ranging from 0 Vdc to 10 Vdc and bipolar voltages ranging from − 10 Vdc to + 10 Vdc
- Selectable output data notation of binary, offset binary, or 2's complement format
- Programmable input gain of 1, 2, 4, or 8
- 16-bit Q-bus addressing support
- Ability to start analog-to-digital conversions either under program control, by an external trigger, or by a realtime clock (such as the KWV11-C)

The KWV11-C is a realtime clock that can be programmed to count from one of five crystal-controlled frequencies, from an external input frequency or event, or from a line frequency clock on the Q-bus. It also has two Schmitt triggers that can be set to operate at any level between ± 12 V on either the positive or negative slope of an external input signal. In response to external events, the Schmitt triggers can be used to start the clock, start analog-to-digital conversions in one of the analog input boards, or generate program interrupts to the processor.

Chapter 33 • AAV11-C Analog Output Board

The AAV11-C is a dual-height, multichannel analog output board designed to interface analog instrumentation to the Q-bus.

• Specifications

Identification	A6006
Size	Dual
Power Requirements	+5.0 V ±5% at 2.5 A
Bus Loads	
ac	0.9
dc	1.0
D/A Resolution	12-bit
Number of D/A Converters	4
Digital Input	12-bits (binary encoded for unipolar output; offset binary for bipolar mode)
Digital Storage	Four separate read/write DAC registers for word or byte storage
Analog Output Voltage	± 10 V @ 10 mA 0 V to 10 V @ 10 mA
Gain Accuracy	Adjustable to (-) full-scale value
Gain Drift	± 30 PPM per °C, maximum
Offset Drift	± 15 PPM per °C, maximum
Offset Error	Adjustable to zero
Linearity (0-10 V)	± ½; LSB; ± 1.2 mV at full-scale range
Differential Linearity	± ½; LSB
Output Impedance	0.5 Ω
Output Current	10 mA @ 10 V minimum
Settling Time	6 μs to 0.1% for a 20 V p-p output change
I/O Connector	20 pins; 3M no. 3421-7020

▪ Related Documentation

Document Title	Order Number
LSI-11 Analog System User's Guide	EK-AXV11-UG
AAV11-C Field Maintenance Print Set	MP-01294-00
AAV11 Diagnostic Documentation Kit	ZJ248-RZ

▪ Configuration

The physical layout of the AAV11-C is shown in Figure 33-1. The AAV11-C has switches and two jumpers to configure the device address. The board also has jumpers to select the output voltage range for unipolar and bipolar operation.

Device Address

The AAV11-C has four addressable read/write registers. Each register is used by one of four digital-to-analog converters and can be addressed as one word or two bytes. The AAV11-C device address is the I/O address assigned to the first of four DAC registers. The user configures the device address via a switchpack (for address bits DAL <3:10>) and two jumpers (for bits <11:12>). A switch in the ON position (or a jumper installed) encodes a logical 0 in the corresponding address bit; a switch in the OFF position (or a jumper removed) encodes a logical 1.

The device address can range from 160000 to 177770 in increments of 10. The device address is factory-configured at 170440, as shown in Figure 33-2.

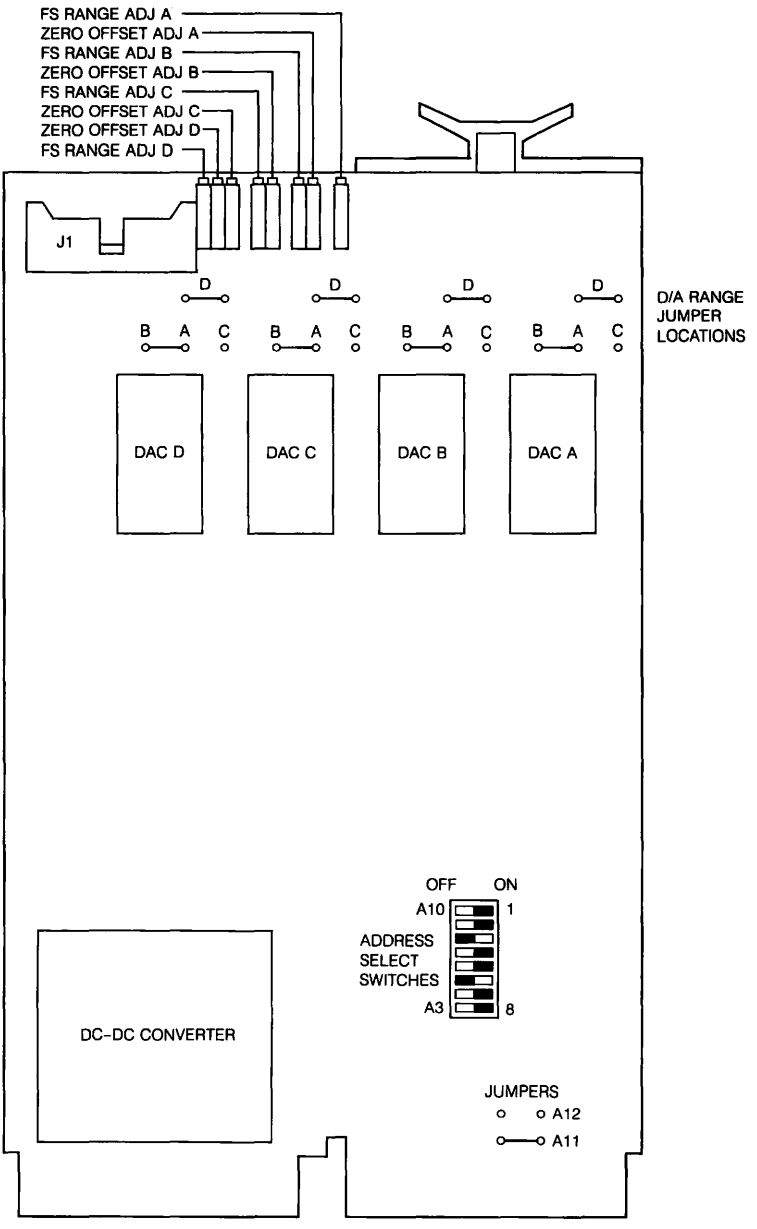


Figure 33-1 ▪ AAV11-C Physical Layout

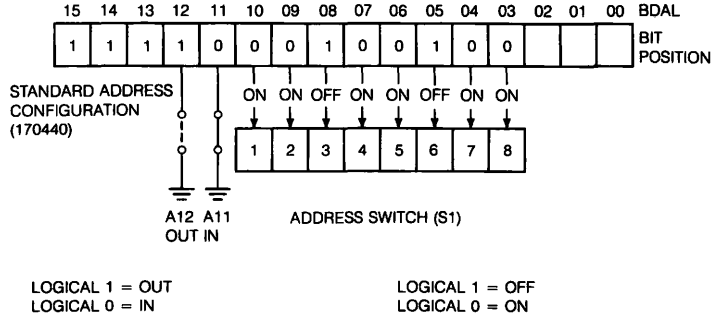


Figure 33-2 ▪ Selecting AAV11-C Device Address

Output Voltage Range Selection

Each DAC on the AAV11-C has separate voltage range jumpers. These jumpers are found above their corresponding D/A converter IC on the printed circuit board (see Figure 33-1). When sent from the factory, the AAV11-C has a voltage range selected for all four DACs of bipolar ± 10 V. Table 33-1 shows which jumpers to install to select the output voltage range. The output of the board can be configured for either straight binary notation for unipolar operation or offset binary notation for bipolar operation. The expected output values are shown in Table 33-1.

Table 33-1 ▪ AAV11-C Output Voltage Range Jumpers

Polarity	Output Voltage Range	Install Jumpers	Notation	Input Code (Octal)	Output Value
Unipolar	0 to + 10 V	A to C	Binary	000000	+ full scale
				007777	0 V
Bipolar	± 10 V	A to B; D	Offset binary	000000	+ full scale
				004000	0 V
				007777	− full scale

▪ Interfacing to the AAV11-C

Figure 33-1 shows the location of the connectors on the AAV11-C. DAC inputs and control signal inputs enter the board via the Q-bus connectors. Analog output voltages and digital control signals leave the board via the top edge connector J1. Each DAC has one output and a corresponding analog ground pin. The four least significant bits of DAC D (D00, D01, D02, and D03) are used for control signals to an analog device. These four bits are TTL-compatible.

Figure 33-3 shows how the AAV11-C is connected to a device that uses differential analog inputs and one control input. Both the AAV11-C and the analog device must be set up for electrical compatibility. The device manual should define which pins to attach to the AAV11-C control bits. The software enables or disables the control bits.

Note

The AAV11-C is available as an **add-on option** for installation by technically experienced customers. It is compatible with the system backplane but is not installed in a Digital manufacturing facility. The AAV11-C option does not include an I/O Connection panel insert, nor does it qualify for use in an FCC Class A system.

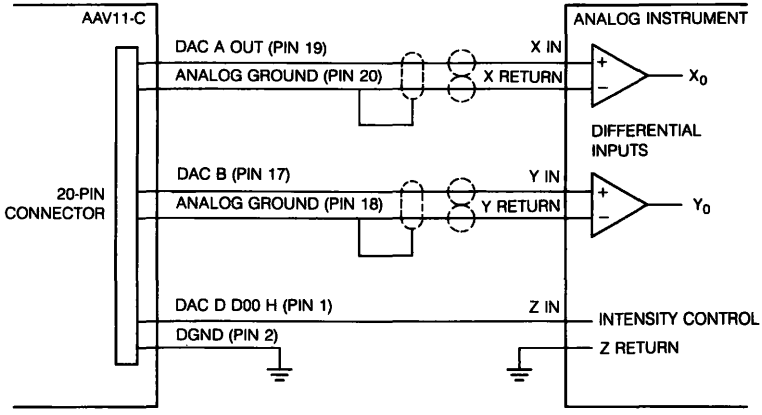


Figure 33-3 ▪ Connecting AAV11-C to a Differential Input Device

Chapter 34 ▪ ADV11-C Analog-to-Digital Converter

The ADV11-C is a Q-bus analog input printed circuit board that performs analog-to-digital conversions.

▪ Specifications

Identification	A8000
Size	Dual
Power Requirements	+5.0 V ±5% at 2.0 A
Bus Loads	
ac	1.3
dc	1.0
I/O Connector	26 pins; 3M no. 3399-7026
Inputs	
Number of Analog Inputs	Eight channels using differential inputs, or 16 channels using single-ended inputs
Analog Input Range	0 V to +10 V −10 V to +10 V
Maximum Input Signal	±10.5 V (signal + common mode voltage)
Input Impedance	
Off Channels	100 M Ω minimum in parallel with 10 pF maximum
On Channels	100 M Ω minimum in parallel with 100 pF maximum
Power Off	1 K ohm in series with a diode
Input Protection	Inputs are current-limited and protected to ±30 V overvoltage without damage
Input Bias Current	20 nA at 25°C (76°F), maximum
A/D Output	
Data Buffer Register	16-bit read-only output register
Resolution	12-bit unipolar; 11-bit bipolar, plus sign
Data Notation	Binary, offset binary, or 2's complement

Sample and Hold Amplifier	
Aperture Uncertainty	Less than 10 ns
Aperture Delay	Less than 0.5 μs from start of conversion to signal disconnect
Front End Settling	Less than 15 μs to ±0.01% of full-scale value for a 20 V p-p input
Input Noise	Less than 0.2 mV rms
A/D Converter Performance	
Linearity	± ½; LSB
Stability (temp coefficient)	±30 ppm/°C
Stability, long-term	±0.05% change per six months
System Accuracy	Input voltage to digitized value ±0.03%
Conversion Time	25 μs from end of front end starting to setting the A/D DONE bit
System Throughput	25 K channel samples per second

▪ Related Documentation

Document Title	Order Number
LSI-11 Analog System User's Guide	EK-AXV11-UG
ADV11-C Field Maintenance Print Set	MP-01292-00
ADV11 Diagnostic Documentation Kit	ZJ250-RZ

▪ Configuration

The ADV11-C, shown in Figure 34-1, has jumpers used to configure the device address, the interrupt vector address, and the analog configuration. The user can also select the A/D input range, polarity, and the output data notation.

There are two types of jumpers on the ADV11-C board. Some are point-to-point jumpers, in which each jumper pin has a unique number. A jumper is installed from one numbered pin to another. The other jumpers are pairs of pins. With each jumper type, a jumper wire is installed across a pair of pins.

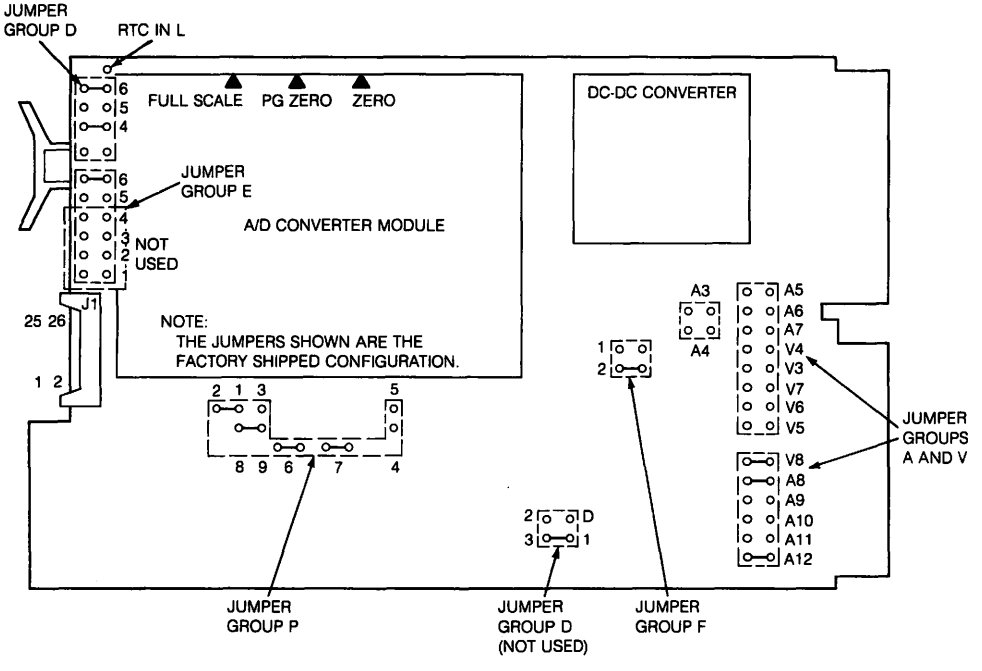


Figure 34-1 ▪ ADV11-C Physical Layout

Device Address

The ADV11-C uses two registers in the I/O page — a control and status register (CSR) and a data buffer register (DBR), listed in Table 34-1. The control and status register is a read/write register used to pass control and status information to and from the ADV11-C. The data buffer register is a read-only register that holds the digital data after the A/D conversion has completed.

Table 34-1 ▪ ADV11-C Standard Address Assignments

Description	Mnemonic	1st Module Address	2nd Module Address
Registers:			
Control and Status	CSR (R/W)	170400	170420
Data Buffer	DBR (W-O)	170402	170422
Interrupt Vectors:			
A/D Done		400	410
Error		404	414

The ADV11-C device address is the I/O address assigned to the A/D control and status register. The device address is selected by means of jumpers A3 through A12. (See jumper groups A and V in Figure 34-1). The jumpers allow the user to set the device address within the range of 160000 to 177770 in increments of 10. The device address is factory-configured at 170400, as listed in Table 34-1 and shown in Figure 34-2. A jumper installed encodes a 1 in the corresponding bit position; a jumper out encodes a 0.

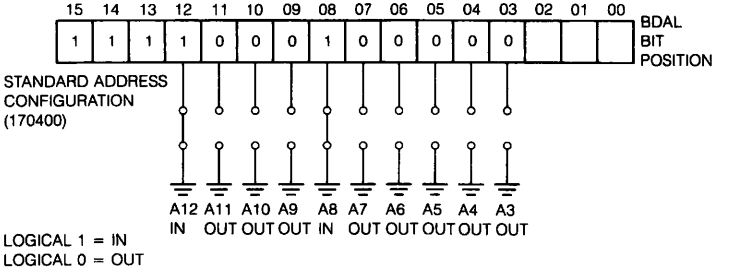


Figure 34-2 ▪ Selecting ADV11-C Device Address

Interrupt Vector Address

The ADV11-C can generate two interrupt vectors, as listed in Table 34-1. The base interrupt vector address is assigned to A/D DONE. (The ERROR interrupt is automatically assigned the base interrupt vector address + 4.)

The base interrupt vector address can be selected in the range of 0 to 770, in increments of 10. It is factory-configured to 400 by jumpers V3 through V8, as shown in Figure 34-3. (See jumper groups A and V in Figure 34-1).

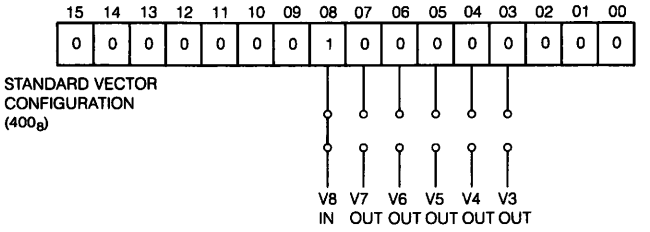


Figure 34-3 ▪ Selecting ADV11-C Interrupt Vector Address

Analog Input Range, Type, and Polarity

The ADV11-C allows software control over the full-scale range selection. The effective ranges provided by the programmable gain are as follows:

Gain	Unipolar	Bipolar
1	0 V to +10 V	±10 V
2	0 V to +5 V	±5 V
4	0 V to +2.5 V	±2.5 V
8	0 V to 1.25 V	±1.25 V

Table 34-2 shows the jumpers that must be installed to set up the analog input type. The board comes from the factory set for 16-channel single-ended, bipolar inputs. Refer to jumper group P in Figure 34-1.

Table 34-2 ▪ Selecting ADV11-C Analog Input Type

Input Type	Install Jumpers
Single-Ended Inputs*	P1 to P2; P8 to P9
Differential Inputs	P2 to P3; P4 to P5

* Factory configuration

Note

Jumpers P6 and P7 are factory-installed for the programmable gain feature and should be left in.

A/D Output Data Notation

The ADV11-C allows the user to select the data notation to be used for the A/D output, as either binary, offset binary, or 2's complement notation. Table 34-3 shows the jumpers that must be installed to select the data notation. Refer to jumper groups D and E near the handle of the board, shown in Figure 34-1.

Table 34-3 ▪ Selecting ADV11-C A/D Output Data Notation

A/D Output Data Notation	Jumpers 1D	4D	5D	6D	5E	6E	Input Voltage	Output Code (Octal)
Binary	IN	OUT	OUT	IN	OUT	IN	+ full scale	007777
							0 V	000000
Offset binary*	OUT	IN	OUT	IN	OUT	IN	+ full scale	007777
							0 V	004000
							− full scale	000000
2's Complement	OUT	IN	IN	OUT	IN	OUT	+ full scale	003777
							0 V	000000
							− full scale	174000

* Factory configuration

External Trigger Source

The A/D conversions within the ADV11-C can be started in one of the following three ways:

- Under program control.
- By a realtime clock input at J1 (pin 21) or at pin RTC IN.
- By an external trigger, either at J1 (pin 19) or at the BEVNT line on the Q-bus.

The user can select the source of the external trigger using two jumpers on the board. (See jumper group F in Figure 34-1). Table 34-4 shows the jumpers to install to select the source of the external trigger.

Table 34-4 ▪ Selecting ADV11-C External Trigger

External Trigger Source	Jumpers F1	F2
BEVNT line (Q-bus)	IN	OUT
EXT TRIG IN (J1 pin 19)*	OUT	IN

* Factory configuration

Interfacing to the ADV11-C

Figure 34-1 shows the location of the I/O connector J1 on the ADV11-C. Analog input signals enter the board through this connector. Up to 16 single-ended analog inputs can be connected to J1 (CH 0 to CH 15), or up to eight differential analog inputs can be connected to J1 using CH 0 to CH 7 and RETURN 0-7. A realtime clock input and an external trigger can also be connected to J1. Under program control, the clock or external trigger can be enabled to start an A/D conversion.

The ADV11-C has two bus interface connectors that plug into the Q-bus. These connectors have signals defined by Q-bus specifications.

Single-Ended Inputs (16 Channels)

Single-ended analog inputs have one side of the user's analog source connected to the A/D converter amplifier and the other side connected to ground, as shown in Figure 34-4.

The benefit of single-ended inputs is that the user gets twice as many channels as in a differential input system. The disadvantage is the loss of the common mode rejection that is available with a differential system. Therefore, the recommended analog inputs are as follows:

- Input level: High, more than 1 V
- Input cable lengths: Short, less than 4.5 m (15 ft)

The user's source may be positioned some distance from the computer, and a voltage difference may occur between the user's source ground and the computer ground. This ground voltage difference (Vn) is included in the signal received by the A/D converter. To decrease this ground difference, plug the user's device into an ac receptacle as close as possible to the one providing power to the computer.

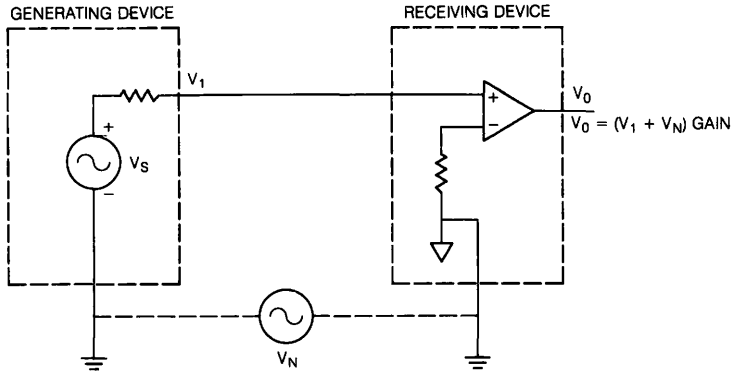


Figure 34-4 ▪ Single-Ended Analog Input

Note

Do not run a wire from the user's ground to the ADV11-C analog ground, because this wire forms a path for ground loop current that can affect the results on all input channels.

Floating-point lines can be created by connecting the common side of the user's devices to the analog ground input on the ADV11-C (J1 pin 17). The ground point is shared among the channels. The signal return path from the A/D converter does not result in a current loop with the device ground.

Pseudo-Differential Inputs (16 Channels)

A pseudo-differential analog input system can be created by connecting all input sensors referenced to a common point, such as AMP, as show in Figure 34-5. This is possible because AMP is an input at connector J1 (pin 18) for user connection. The input amplifier rejects the common mode noise. The recommended analog inputs are as follows:

- Input range: 100 mV to 10 V
- Input cable lengths: Less than 7.5 m (25 ft)

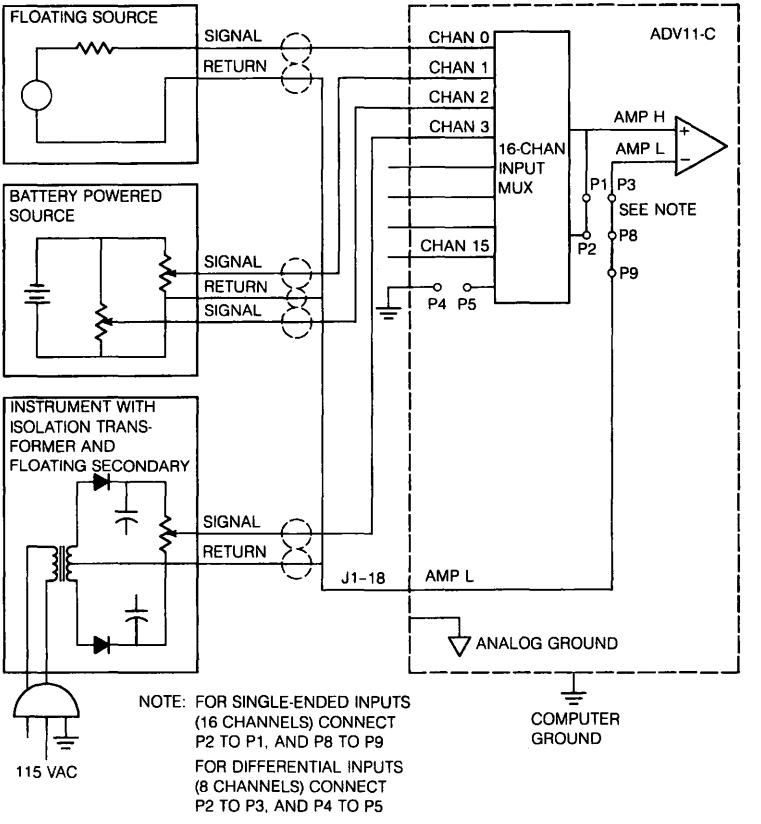


Figure 34-5 ▪ Pseudo-Differential Inputs

Differential Inputs (8 Channels)

Differential inputs have one side of the generating source connected to the positive (+) input of the A/D input amplifier and the other side of the source connected to the negative (−) input of the amplifier, as shown in Figure 34-6.

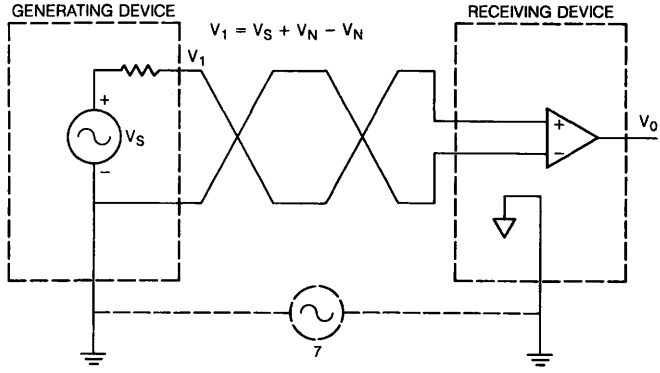


Figure 34-6 ▪ Differential Inputs

The benefit of differential inputs is that noise voltages appearing at the same time on both sides of the source are rejected by the A/D input amplifier. This is called common mode rejection, and provides a system with low noise. The amount of noise rejection is a ratio, the common mode rejection ratio (CMRR), given in decibels (dB). The CMRR for the ADV11-C is 80 dB at full-scale range.

The disadvantage of differential inputs is that the number of available input channels is lowered by half.

The recommended analog inputs are as follows:

- Input range: 10 mV to 10 V
- Input cable length: As needed by user
- Cable type: Twisted-pair, shielded lines with low impedance

Note

The ADV11-C is available as an **add-on option** for installation by technically experienced customers. It is compatible with the system backplane but is not installed in a Digital manufacturing facility. The ADV11-C option does not include an I/O connection panel insert, nor is it qualified for use in an FCC Class A system.

Chapter 35 • AXV11-C Analog Input/Output Board

The AXV11-C is an LSI-11 analog input/output printed circuit board.

• Specifications

Identification	A0026
Size	Dual
Power Requirements	+5 V (±5%) at 2.0 A
Bus Loads	
ac	1.3
dc	1.0
I/O Connector	26 pins; 3 M no. 3399-7026
Analog Input	
Number of Analog Inputs	8 channels using differential inputs, or 16 channels using single-ended inputs
Input Range	0 V to +10 V; −10 V to +10 V
Input Gain (programmable)	Gain (±0.05%) Range 1 10 V 2 5 V 4 2.5 V 8 1.25 V
Maximum Input Signal	10.5 V (signal + common mode voltage)
Input Impedance	
Off Channels	100 MΩ in parallel with 10 pF maximum
On Channels	100 MΩ in parallel with 100 pF maximum
Power Off	1 kΩ in series with a diode
Input Bias Current	20 nA at 25°C, maximum
Common Mode Rejection Ratio	80 dB at 10 V full-scale range at 60 Hz
A/D Output	
Data Buffer Register	16-bit read-only output register
Resolution	12-bit unipolar; 11-bit bipolar plus sign
Data Notation	Binary, offset binary, or 2's complement

Coding

Notation Used	Full-Scale Input Voltage	Output Coding Code (Octal)
Binary	+9.9976 V	007777
	0.0000 V	000000
Offset binary	+9.9951 V	007777
	0.0000	004000
	−10.0000 V	000000
2's complement	+9.9951 V	003777
	0.0000 V	000000
	−10.0000 V	174000

Sample and Hold Amplifier

Aperture Uncertainty	Less than 10 ns
Aperture Delay	Less than 0.5 μs from start of conversion to signal disconnect
Front End Settling	Less than 15 μs to ±0.01% of full-scale value for a 20 V p-p input
Input Noise	Less than 0.2 mV rms

A/D Converter Performance

Linearity	± ½ LSB
Stability (temp coefficient)	±30 ppm/°C
Stability, long-term	±0.05% change per 6 months
Conversion Time	25 μs from end of front end starting to setting the A/D DONE bit
System Throughput	25 K channel samples per second
System Accuracy	Input voltage to digitized value ±0.03%

D/A Converter Specifications

Number of D/A Converters	2
Digital Input	12 bits (Binary code is used for unipolar output; offset binary of 2's complement code is used for bipolar output)
Analog Output	±10 V or 0 V to +10 V
Output Current	±5 mA maximum
Output Impedance	0.1 Ω
Differential Linearity	± ½ LSB
Non-linearity	0.02% of full-scale value
Offset Error	Adjustable to zero
Offset Drift	±30 ppm/°C maximum
Gain Accuracy	Adjustable to full-scale value

Gain Drift	± 30 ppm/°C maximum
Settling Time	65 μs to 0.1% for a 20 V p-p output change
Noise	0.1% full-scale value
Capacitive Load Capability	0.5 μF

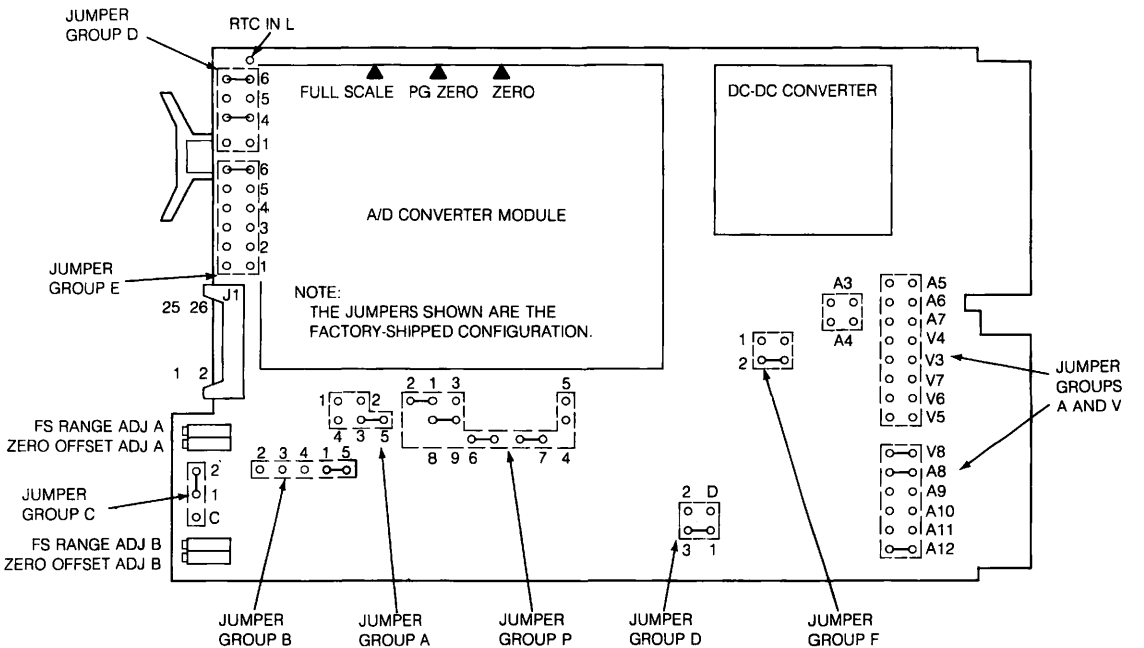
▪ Related Documentation

Document Title	Order Number
LSI-11 Analog System User's Guide	EK-AXV11-UG
AXV11-C Field Maintenance Print Set	MP-011291-00

▪ Configuration

The AXV11-C, shown in Figure 35-1, has jumpers used to configure the device address, the interrupt vector address, the analog configuration, and the DAC configuration. The user can select the A/D input range, polarity, and the output data notation. The user can also select the D/A input data notation, output range, and polarity of each DAC.

There are two types of jumpers on the board. Some are point-to-point jumpers, in which each jumper pin has a unique number. A jumper is installed from one numbered pin to another. The other jumpers are pairs of jumper pins. With each jumper type, a jumper wire is installed across a pair of pins.



AXV11-C Physical Layout

Figure 35-1 ▪ AXV11-C Physical Layout

Device Address

The AXV11-C has four programmable registers, listed in Table 35-1. The control and status register is a read/write register used to pass control and status information to and from the AXV11-C. The data buffer register is a read-only register that holds the digital data after the A/D conversion is complete. The DAC A and DAC B registers are 12-bit write-only registers that accept digital data to be changed to analog voltages.

Table 35-1 ▪ AXV11-C Standard Address Assignments

Description	Mnemonic	1st Module Address	2nd Module Address
Registers:			
Control and Status	CSR (R/W)	170400	170420
Data Buffer	DBR (R-O)	170402	170422
DAC A	DAA (W-O)	170404	170424
DAC B	DAB (W-O)	170406	170426
Interrupt Vectors:			
A/D Done		400	410
Error		404	414

The AXV11-C device address is the I/O address assigned to the control and status register. The device address is selected by means of jumpers A3 through A12, as shown in Figure 35-2. (See jumper groups A and V in Figure 35-1). The jumpers allow the user to set the device address within the range of 160000 to 177770. The device address is factory-configured at 170400, as listed in Table 35-1. A jumper installed encodes a 1 in the corresponding bit position; a jumper removed encodes a 0.

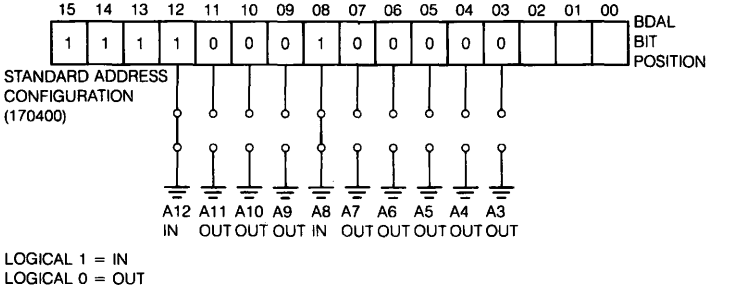


Figure 35-2 ▪ Selecting AXV11-C Device Address

Interrupt Vector Address

The AXV11-C can generate two interrupts, as listed in Table 35-1, and therefore requires two consecutive interrupt vectors. The base interrupt vector address is assigned to A/D DONE. (The ERROR interrupt is automatically assigned the base interrupt vector address + 4.)

The base interrupt vector address can be set in the range of 0 to 770, in increments of 10. The vector address is selected by means of jumpers V3 through V8, as shown in Figure 35-3. (See jumper groups A and V in Figure 35-1.) The standard vector address of the first AXV11-C in a system is 400. If a second module is configured, it is generally assigned a standard vector address of 410.

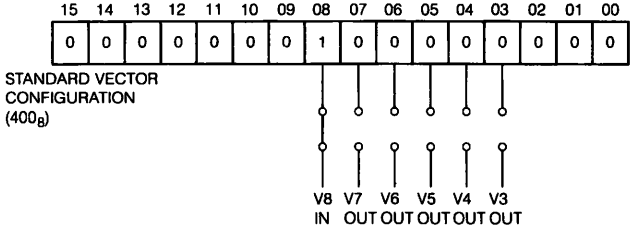


Figure 35-3 ▪ Selecting AXV11-C Interrupt Vector Address

Analog Input Range, Type, and Polarity

The AXV11-C allows software control over the full-scale range selection. The effective ranges provided by the programmable gain are as follows:

	Effective Input Range	
Gain	**Unipolar**	**Bipolar**
1	0 V to +10 V	±10 V
2	0 V to +5 V	±5 V
4	0 V to +2.5 V	±2.5 V
8	0 V to +1.25 V	±1.25 V

Table 35-2 shows the jumpers that must be installed to set up the analog input type. The board comes from the factory set for 16-channel single-ended, bipolar inputs. Refer to jumper group P in Figure 35-1.

Table 35-2 ▪ Selecting AXV11-C Analog Input Type

Input Type	Install Jumpers
Single-Ended Inputs*	P1 to P2; P8 to P9
Differential Inputs	P2 to P3; P4 to P5

* Factory configuration

Note

Jumpers P6 to P7 are factory-installed for the programmable gain feature and should be left in.

A/D Output Data Notation

The AXV11-C allows the user to select the data notation to be used for the A/D output, as either binary, offset binary, or 2's complement notation. Table 35-3 shows the jumpers that must be installed to select the data notation. Refer to jumper groups D and E near the handle of the board, shown in Figure 35-1.

External Trigger Source

The A/D conversions within the AXV11-C can be started in one of the following three ways:

- Under program control.
- By a realtime clock input at J1 (pin 21) or at pin RTC IN.
- By an external trigger, either at J1 (pin 19) or at the BEVNT line on the Q-bus.

The user can select the source of external trigger using two jumpers on the board. (See jumper group F in Figure 35-1.) Table 35-4 shows the jumpers to install to select the source of the external trigger.

Table 35-3 ▪ Selecting AXV11-C A/D Output Data Notation

A/D Output Data Notation	Jumpers 1D	4D	5D	6D	5E	6E	Input Voltage	Output Code (Octal)
Binary	IN	OUT	OUT	IN	OUT	IN	+ full scale	007777
							0 V	000000
Offset binary*	OUT	IN	OUT	IN	OUT	IN	+ full scale	007777
							0 V	004000
							− full scale	000000
2's complement	OUT	IN	IN	OUT	IN	OUT	+ full scale	003777
							0 V	000000
							− full scale	174000

* Factory configuration

Table 35-4 ▪ Selecting AXV11-C External Trigger

External Trigger Source	Jumpers F1	F2
BEVNT line (Q-bus)	IN	OUT
EXT TRIG IN (J1 pin 19)*	OUT	IN

* Factory configuration

D/A Configuration

The user can select the input data notation and the output voltage range for the two D/A converters on the AXV11-C. DAC A and DAC B can be configured for different polarities; however, the input data notation selected and the output polarity selected must be the same for each DAC. Refer to Table 35-5 to set up DAC A; refer to Table 35-6 to set up DAC B. Jumper groups A, B, and D for the DACs are found below the A/D converter module, shown in Figure 35-1.

Table 35-5 ▪ Selecting DAC A Jumper Configuration

	D/A Input Data Notation		
Range and Polarity	Binary	Offset Binary	2's Complement
± 10 V	N/A	3A to 5A* D1 to D3	3A to 5A D to D2
0 to + 10 V	1A to 2A D1 to D3	N/A	N/A

* Factory configuration

Table 35-6 ▪ Selecting DAC B Jumper Configuration

	D/A Input Data Notation		
Range and Polarity	**Binary**	**Offset Binary**	**2's Complement**
± 10 V	N/A	1B to 5B* D1 to D3	1B to 5B D to D2
0 to + 10 V	2B to 3B D1 to D3	N/A	N/A

* Factory configuration

▪ Interfacing to the AXV11-C

Figure 35-1 shows the location of I/O connector J1 on the AXV11-C. Analog input signals enter the board through this connector, and DAC output signals leave through this connector. Up to 16 single-ended analog inputs can be connected to J1 (CH 0-CH 15), or up to eight differential analog inputs can be connected to J1 using CH 0-CH 7 and RETURN 0-7. A realtime clock input and an external trigger can also be connected to J1. Under program control, these two inputs can be enabled to start an A/D conversion.

RTC IN has a separate pin, found near the printed circuit board handle, for easy installation of a wire jumper from a clock board, such as the KWV11-C CLK OVFL tab.

Note

The AXV11-C is available as an **add-on option** for installation by technically experienced customers. It is compatible with the system backplane but is not installed in a Digital manufacturing facility. The AXV11-C option does not include an I/O connection panel insert, nor is it qualified for use in an FCC Class A system.

Chapter 36 ▪ KWV11-C Programmable Realtime Clock

The KWV11-C is a programmable realtime clock printed circuit board.

▪ Specifications

Identification	M4002
Size	Dual
Power Requirements	+5 V ±5% at 2.2 A +12 V ±3% at 13 mA
Bus Loads	
ac	1.0
dc	1.0
Clock	
Crystal Oscillator	10 MHz base frequency
Output Ranges	1 MHz, 100 kHz, 10 kHz, 1 kHz, and 100 Hz
Oscillator Accuracy	0.01%
Other Sources	Line frequency or input at Schmitt trigger 1
I/O Connector	40 pins; 3M no. 3417-7040
Schmitt Trigger Input Signals	
Number of inputs	2
Input Range	±30 V (maximum limits)
Triggering Range	−12 V to +12 V adjustable
Triggering Slope	Positive or negative, switch-selectable
Source	User device
Response Time	Depends on input waveform and amplitude; for TTL logic levels, typically 600 ns
Hysteresis	Approximately 0.5 V, positive and negative
Characteristics	Single-ended input with 100 KΩ impedance to ground
Clock Output	
Single	CLK OVFL (clock overflow, asserted low)

Output Pins	J1 pin RR and CLK OVFL tab
Function	Time base selection from an internal crystal-controlled frequency, an input at ST1, or a line frequency at BEVNT bus line
Duration	Approximately 500 ns
Line Driver	TTL compatible, open collector circuit with 470-Ω pull-up resistor to +5 V
Maximum Source Current	5 mA when output is high (≥2.4 V), measuring from source through load to ground
Maximum Sink Current	8 mA when output is low (0.8 V), measuring from external source voltage through load to output
Schmitt Trigger 1 Output	
Signal	ST1 OUT (asserted low)
Output Pins	J1 pin UU and ST1 OUT tab
Function	External time base input or counter of external events; input frequency function of input signal
Miscellaneous Characteristics	Same as clock output
Schmitt Trigger 2 Output	
Signal	ST2 OUT (asserted low)
Output Pins	J1 pin SS
Function	Starts counter, sets ST2 flag, and generates an interrupt (if enabled); causes buffer preset register (BPR) to be loaded from counter
Miscellaneous Characteristics	Same as clock output

▪ Related Documentation

Document Title	Order Number
LSI-11 Analog System User's Guide	EK-AXV11-UG
KWV11-C Field Maintenance Print Set	MP-01293-00
KWV11 Diagnostic Documentation Kit	ZJ247-RZ

▪ Configuration

The KWV11-C, shown in Figure 36-1, has two switchpacks, SW1 and SW2, used to configure the device and interrupt vector addresses. It also has another switchpack, SW3, to select the Schmitt trigger slope and level controls. For each of the two Schmitt triggers on-board, the user can select a fixed reference level for TTL logic or a variable reference level that permits setting the Schmitt trigger threshold to any point between -12 V and + 12 V. The user can also select whether the Schmitt trigger fires on the positive or negative slope of the input waveform.

Two tabs on the board provide outputs from the clock counter (CLK OVFL) and Schmitt trigger 1 (ST1 OUT). Either of these output tabs can be used to connect a short jumper wire to the A/D input board (pin RTC IN) to start an A/D conversion.

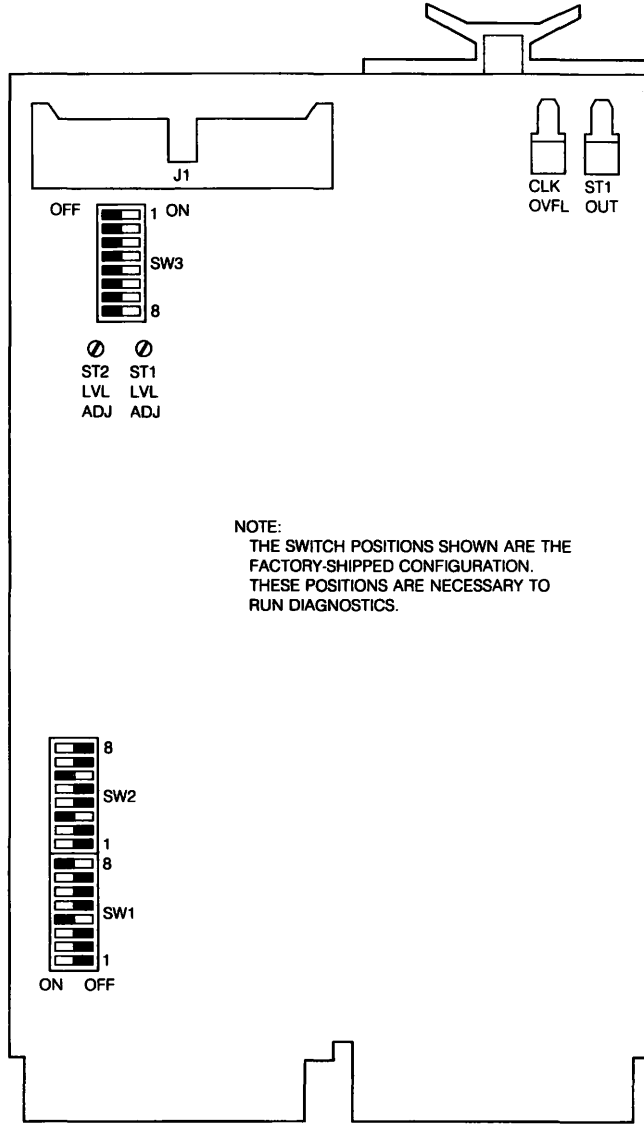


Figure 36-1 ▪ KWV11-C Module Layout

Device Address

The KWV11-C uses two programmable read/write registers, as listed in Table 36-1.

Table 36-1 ▪ KWV11-C Standard Address Assignments

Description	Mnemonic	Status	Address
Registers:			
Control and Status Register	CSR	R/W	170420
Buffer/Preset Register	BPR	R/W	170422
Interrupt Vectors:			
Clock Overflow	CLF OVFL		440
Schmitt Trigger 2	ST2		444

The KWV11-C device address is the base I/O address assigned to the control and status register of the board. The device address is selected by means of two switchpacks, SW1 and SW2. The switches allow the user to set the device address in the range of 170000 to 177774 in increments of 4. The device address is factory-configured at 170420, as shown in Figure 36-2. A switch in the ON position encodes a 1 in the corresponding bit position; a switch in the OFF position encodes a 0.

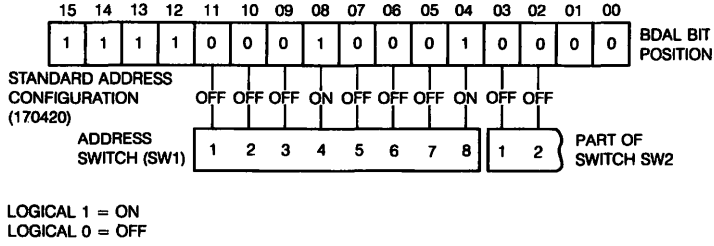


Figure 36-2 ▪ Selecting KWV11-C Device Address

Interrupt Vector Address

The KWV11-C can generate two interrupts (as listed in Table 36-1) and therefore requires two consecutive interrupt vectors. The base interrupt vector is assigned to the clock overflow interrupt and can be assigned any address between 0 and 770 in increments of 10. It is factory-configured to 440 by SW2, as shown in Figure 36-3. A switch in the OFF position encodes a 0; a switch in the ON position encodes a 1.

The interrupt vector for ST2 is automatically four address locations higher than the selected base interrupt vector.

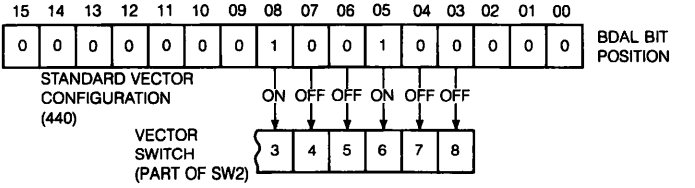


Figure 36-3 ▪ Selecting KWV11-C Interrupt Vector Address

Schmitt Trigger Reference Levels and Slopes

The KWV11-C has two Schmitt triggers that condition the input waveforms to a form needed by the user. Both can be adjusted to trigger at any level in the ± 12 V range (or at TTL fixed levels) and on either the positive or negative slope of the input signal. Each Schmitt trigger has three switches and a potentiometer. The use of these switches and potentiometers is shown in Table 36-2.

Table 36-2 ▪ Setting the KWV11-C Schmitt Triggers

Switch Number	Function
SW3-1	With this switch ON and switch 2 OFF, ST1 fires at a level determined by the ST1 LVL ADJ potentiometer within a range of ± 12 V.
SW3-2	With this switch ON and switch 1 OFF, ST1 fires at a fixed reference level for TTL logic. The potentiometer has no effect.
	Note Switches 1 and 2 cannot be ON together.
SW3-3	With this switch ON and switch 4 OFF, ST2 fires at a level determined by the ST2 LVL ADJ potentiometer within a range of ± 12 V.
SW3-4	With this switch ON and switch 3 OFF, ST2 fires at a fixed reference level for TTL logic. The potentiometer has no effect.
	Note Switches 3 and 4 cannot be ON together.

(continued on next page)

Table 36-2 ▪ Setting the KWV11-C Schmitt Triggers (Cont.)

SW3-5	When this switch is OFF, ST1 fires on the negative slope (high to low transition) of the input signal. When ON, ST1 fires on the positive slope (low to high transition).
SW3-6	When this switch is OFF, ST2 fires on the negative slope of the input signal. When ON, ST2 fires on the positive slope.
SW3-7, SW3-8	Not used

External Control of Schmitt Triggers

The connector J1 on the board allows the user to connect external slope and level controls for each Schmitt trigger. The value of the potentiometers should be between 5 kΩ and 20 kΩ. Selecting a potentiometer with more turns provides for a finer adjustment over the ± 12 V range.

SW3 on the KWV11-C must be set as listed below, and the potentiometers on the KWV11-C should be set to their center of rotation. At the center, the screwdriver slot should be aligned with the notch at its edge.

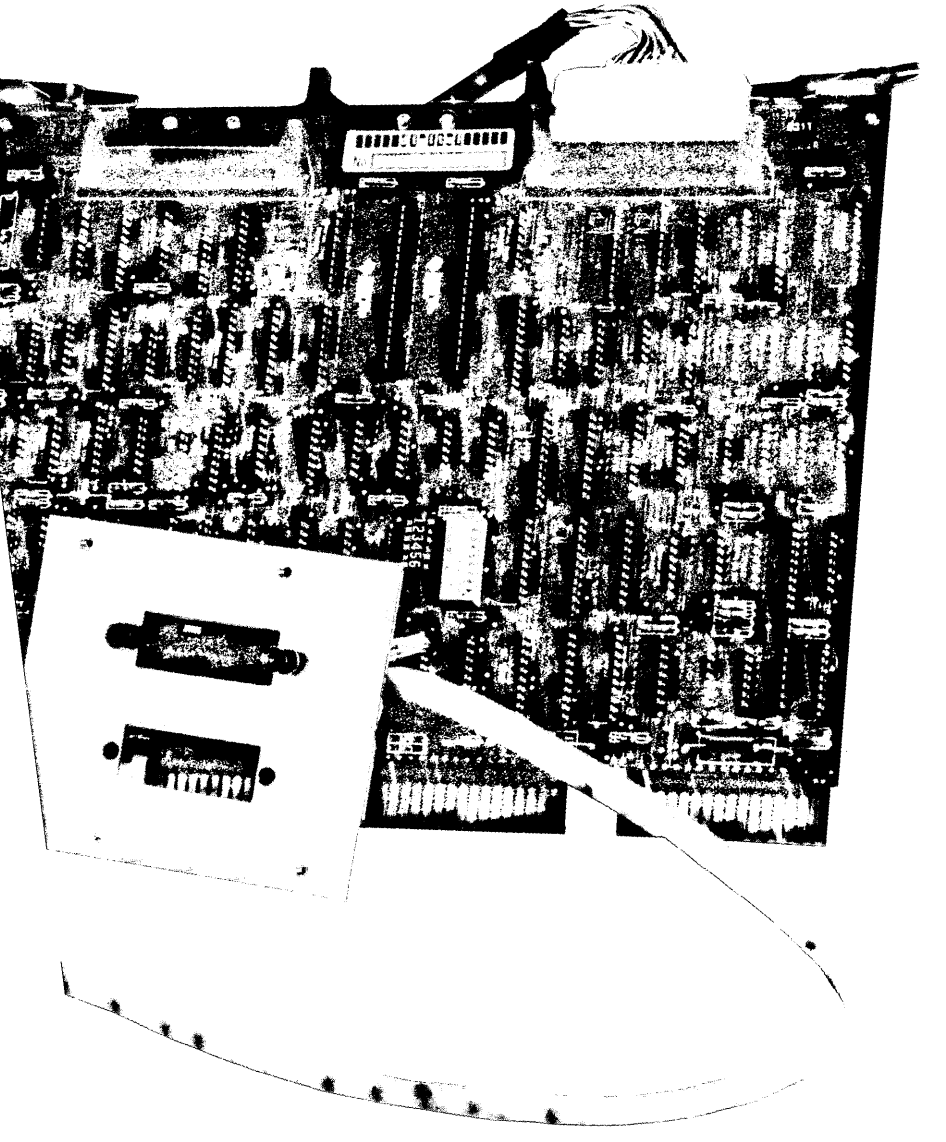
SW3 Switch	Status
1	ON
2	OFF
3	ON
4	OFF
5	OFF
6	OFF
7	Unused
8	Unused

▪ Interfacing to the KWV11-C

The 40-pin I/O connector (J1) on the KWV11-C is provided for user inputs and outputs. In addition, two tabs (shown in Figure 36-1) provide output signals CLK OVFL and ST1 OUT. These tabs are electrically in parallel with pins RR and UU of J1. These tabs make it easier for the user to connect an external start signal because an A/D conversion can be from Schmitt trigger 1 or from the clock counter overflow.

The KWV11-C has two bus interface connectors that plug into the Q-bus. These connectors have signals defined by Q-bus specifications.

Part VIII • Parallel Interfaces



Chapter 37 ▪ Introduction to Parallel Interfaces

The Q-bus parallel I/O interface options provide high-speed data transfers between memory and I/O devices. There are three general-purpose parallel interfaces available, as well as two special-purpose interfaces used to connect the Q-bus to IEEE-488 instrument buses.

▪ DRV11 Parallel Line Unit

The DRV11 is a general purpose interface for connecting parallel line TTL or DTL devices to the Q-bus. It contains a single 16-line port that can execute program-controlled transfers at rates up to 40 Kwords per second. Data is handled by 16 diode-clamped input lines and 16 latched output lines. The DRV11 supports 16-, 18-, or 22-bit addressing.

▪ DRV11-J High-Density Parallel Interface

The DRV11-J is a high-density parallel interface providing four 16-line ports. It also includes an advanced interrupt structure that accepts interrupt requests from up to 16 I/O lines, generating up to 16 individual vector addresses. It supports program selection of fixed or rotating interrupt priorities within the interface. Two DRV11-Js can be connected as a link between two Q-buses. The DRV11-J supports 16-, 18-, or 22-bit addressing.

▪ DRV11-WA General Purpose DMA Interface

The DRV11-WA is a high-speed, general purpose direct memory access (DMA) parallel interface. It is designed for 22-bit Q-bus systems but is also backward-compatible with 18-bit systems. The DRV11-WA can transfer up to 250 Kwords per second in single cycle mode, and up to 500 Kwords per second in burst mode.

▪ IBV11-A Instrument Bus Interface

The IBV11-A interconnects the Q-bus with an instrument bus conforming to the IEEE Standard 488-1975. The IBV11-A can accommodate up to 15 IEEE-488 devices and can transfer up to 40 Kbytes per second. The IBV11-A supports 16-, 18-, or 22-bit addressing.

▪ IEQ11-A DMA IEC/IEEE Bus Interface Option

The IEQ11-A is a DMA controller interconnecting the Q-bus with two independent buses conforming to both the European Standard IEC 625-1 and the U.S. Standard IEEE 488-1978. Each bus can have up to 15 devices in sequential configuration. The IEQ11-A is a bit-parallel byte-serial controller that can perform transfers in either program interrupt or direct memory access mode. It supports both 18-bit and 22-bit addressing.

Chapter 38 • DRV11 Parallel Line Unit

The DRV11 is a general purpose interface unit used for connecting parallel line TTL or DTL devices to the Q-bus.

• Specifications

Identification	M7941
Size	Dual
Power Requirements	5.0 Vdc ±5% at 0.9 A
Bus Loads	
ac	1.4
dc	1.0

• Related Documentation

Document Title	Order Number
ADV11-A, KWV11-A, AAV11-A, DRV11 User's Manual	EK-ADV11-OP
DRV11 Field Maintenance Print Set	MP-00866-00
DRV11 Diagnostic Documentation Kit	ZJ244-RZ

• Configuration

The DRV11 device and vector addresses are configured by inserting and/or removing jumpers on the module. The locations of these jumpers are shown in Figure 38-1.

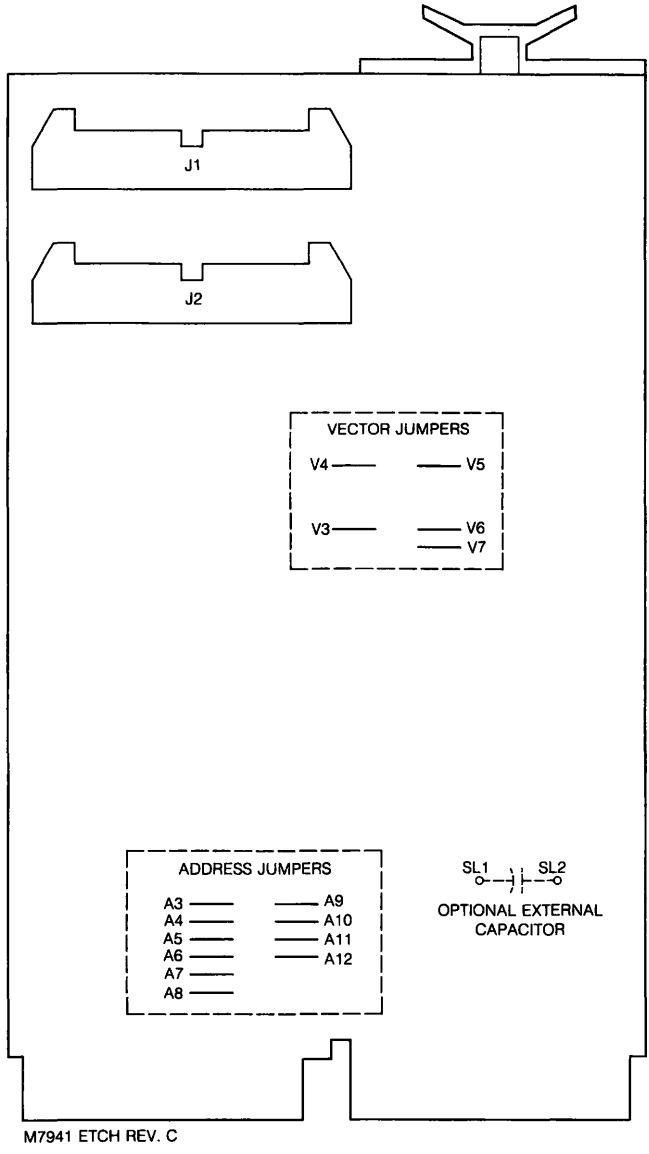


Figure 38-1 ▪ DRV11 Jumper Locations

Device Address

Because each DRV11 uses three registers, each module requires three addresses. Table 38-1 lists the registers along with their standard factory-configured addresses. The base device address is that address assigned to the control and status register. The base address for the DRV11 can range from 160000 through 177770 and is configured using jumpers A3 through A12, as illustrated in Figure 38-2. A jumper removed encodes a logical 1 in the corresponding address bit; a jumper installed encodes a logical 0.

The DRV11 is factory-configured with a device address of 167770. Addresses from 177560 to 177566 are reserved for the console device and should not be used for the DRV11.

Table 38-1 ▪ DRV11 Standard Address Assignments

Description	Mnemonic	1st Module Address	2nd Module Address
Registers:			
Control and Status	DRCSR (R/W)	167770	167760
Output Buffer	DROUTBUF (R/W)	167772	167762
Input Buffer	DRINBUF (R-O)	167774	167764
Interrupt Vectors:			
Request A	REQ A	300	310
Request B	REQ B	304	314

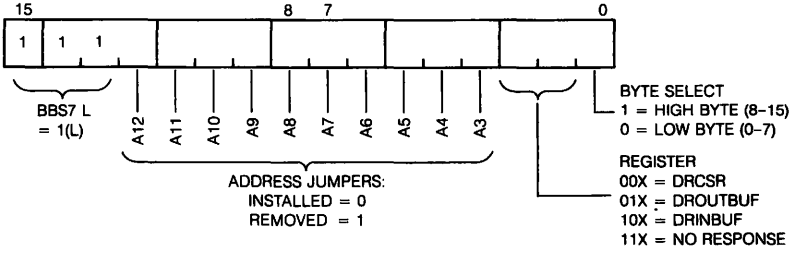


Figure 38-2 ▪ DRV11 Device Address Selection

Interrupt Vector Address

The DRV11 can generate two interrupts, as listed in Table 38-1, and therefore requires two consecutive interrupt vectors. The vector addresses are selected in the range of 000 to 374 by using jumpers V3 to V7, as shown in Figure 38-3. The DRV11 is factory-configured with a vector address of 300.

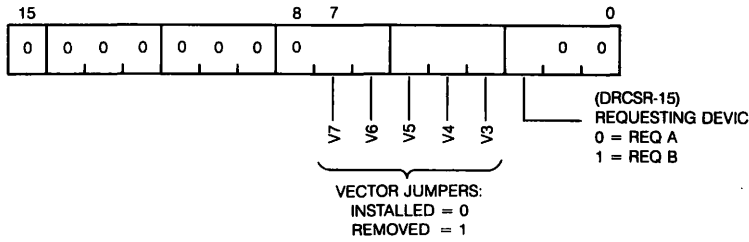


Figure 38-3 ▪ DRV11 Interrupt Vector Selection

NEW DATA RDY and DATA TRANS Pulse Width Modification

An optional capacitor can be added to the DRV11 module to extend the pulse width of both the NEW DATA RDY and DATA TRANS pulse widths. The capacitor can be added in the location shown in Figure 38-1 to produce the approximate pulse widths listed below.

Optional External Capacitance (F)	Approximate Pulse Width (ns)	
	NEW DATA RDY	DATA TRANS
None	350	1150
0.0047	750	1550
0.01	1550	2400
0.02	2330	3200
0.03	3150	3900

▪ Cables and Cabinet Kits

Interfacing the DRV11 to the user's device is via the two board-mounted H854 40-pin male connectors. Optional external cables and connectors for use with the DRV11 include

BC08R-01	1-ft, 40-conductor, flat maintenance cable with H856 connectors on each end
BC07D	Flat, 40-conductor signal cable with H856 connector on one end; other end is terminated by the user. Available in lengths of 3.0, 4.6, and 7.6 m (10, 15, 25 ft)
BCV11	Flat, 40-conductor, twisted pair cable with a single H856 connector on one end; remaining end is connected by the user. Available in lengths of 1.5, 3, 4.6, 6.1, and 7.6 m (5, 10, 15, 20, and 25 ft)
H856	40-pin female socket for user-fabricated cables

When ordered at the same time as the system in which it is to be installed, the DRV11 option (model number DRV11-LP) includes the base module (M7941), internal cables, and the I/O connection panel insert.

When ordered as a system upgrade, the DRV11 option includes the base module only. One of the following cabinet kits should be chosen for system installation:

CK-DRV1B-KA	For use with the BA23 enclosure
CK-DRV1B-KB	For use with the BA11-M enclosure
CK-DRV1B-KC	For use with the H349 distribution panel

Chapter 39 • DRV11-J High-Density Parallel Interface

The DRV11-J is a high-density parallel interface, providing 64 I/O data lines on a dual-height module.

• Specifications

Identification	M8049
Size	Dual
Power Requirements	+5 V ±5%, 1.6 A (typical), 1.8 A (maximum)
Bus Loads	
ac	2.0
dc	1.0
Data Buffer Tri-State Outputs	V_{OL} = 0.5 V @ I_{OL} = 24 mA V_{OL} = 0.4 V @ I_{OL} = 12 mA V_{OL} = 2.4 V @ I_{OH} = -2.6 mA
Data Buffer Inputs	I_{IL} = -0.2 mA @ V_{IL} = 0.4 V I_{IH} = 20 μA @ V_{IH} = 2.7 V
Protocol Signal Tri-State Outputs	V_{OL} = 0.55 V @ I_{OL} = 64 mA V_{OH} = 2.4 V @ I_{OH} = -15 mA
Protocol Signal Inputs	Termination: 120 Ω I_{IL} = -27 mA @ V_{IL} = 0.5 V I_{IH} = 80 μA @ V_{IH} = 2.7 V
Nonstandard Environmental Specifications	
Storage Temperature	−40°C to 60°C (-40°F to 140°F)

▪ Related Documentation

Document Title	Order Number
DRV11-J Parallel Line Interface User's Guide	EK-DRV1J-UG
DRV11-J Field Maintenance Print Set	MP-00866-00
DRV11 Diagnostic Documentation Kit	ZJ244-RZ

▪ Configuration

Eleven wirewrap jumpers or jumper clips can be installed or removed in various combinations to select the desired DRV11-J configuration. Nine of the jumpers (W1 through W9) are used to select the device starting address. Jumper W10 is reserved for future use. Jumper W11 is used to select the combination of high-byte port A signals used to generate the interrupt requests. The locations of these jumpers are shown in Figure 39-1.

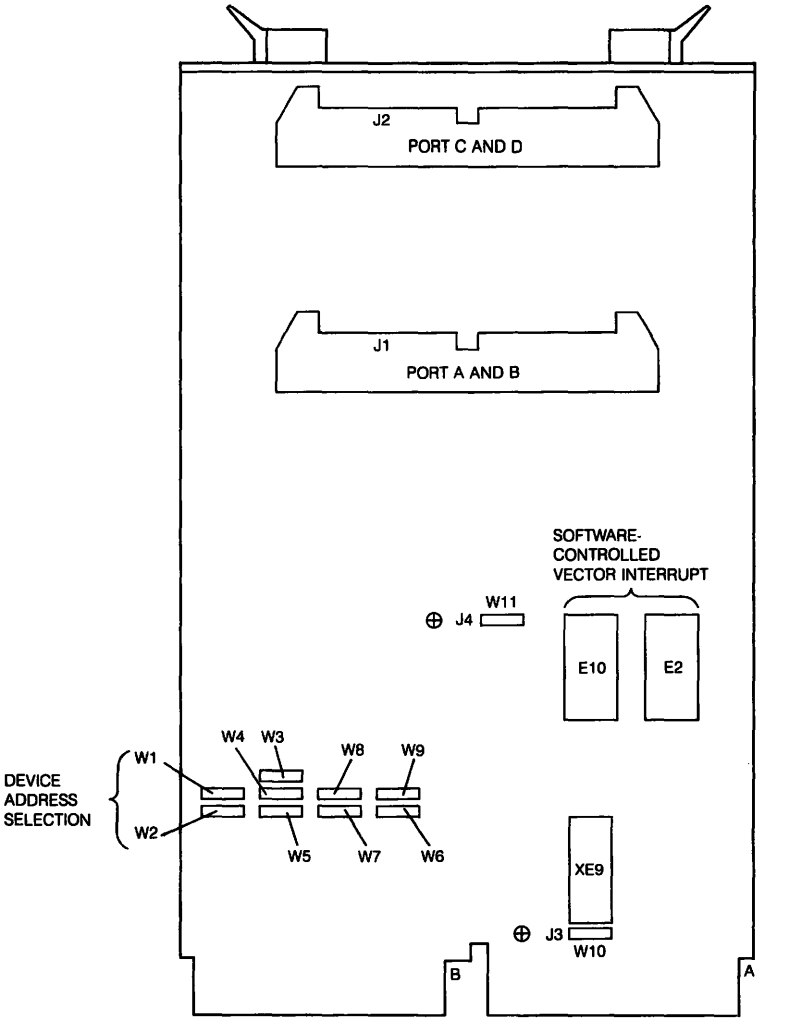


Figure 39-1 ▪ DRV11-J Jumper Locations

Device Address

The DRV11-J contains eight device registers that can be individually addressed by the user program. The eight device registers are divided into four control and status registers and four data buffer registers. Each of the I/O ports is accessed by a control and status register and a data buffer register associated with that port. Table 39-1 lists the eight addressable device registers.

Table 39-1 ▪ DRV11-J Standard Register Addresses

Register	Mnemonic	1st Module Address	2nd Module Address	3rd Module Address
Control and Status A	CSRA	764160	764140	764120
Data Buffer A	DBRA	764162	764142	764122
Control and Status B	CSRB	764164	764144	764124
Data Buffer B	DBRB	764166	764146	764126
Control and Status C	CSRC	764170	764150	764130
Data Buffer C	DBRC	764172	764152	764132
Control and Status D	CSRD	764174	764154	764134
Data Buffer D	DBRD	764176	764156	764136

Three standard device addresses have been assigned for use with DRV11-Js — 764160, 764140, and 764120. The module is configured at the factory for an address of 764160. If two additional modules are used in the system, the second DRV11-J should be configured for 764140 and the third for 764120. If the system application requires more than three DRV11-Js, addresses for the additional modules must be selected from the user-reserved area of the address map (from 764000 to 767776) and assigned in descending order in decrements of 20. When selecting addresses other than the three standard addresses, refer to the current issue of the *PDP-11 Architecture Handbook* to avoid possible I/O device address conflicts.

Nine address jumpers (W1 through W9) are installed or removed to establish a base device register address. Figure 39-2 shows the format of a DRV11-J device address. Note that address bits A13 through A15 are neither configured nor decoded by the module. These bits are decoded by the bus master module as the bank 7 select (BBS7) bus signal. Address bit 0 is used by the program to select a high-byte or a low-byte operation. Address bits <1:3> are used to select one of the eight device registers in the addressed module.

The DRV11-J jumper arrangement provides the capability of configuring any address from 760000 to 777600. However, the address selected must fall within the user area of the address space — from 764000 to 767776.

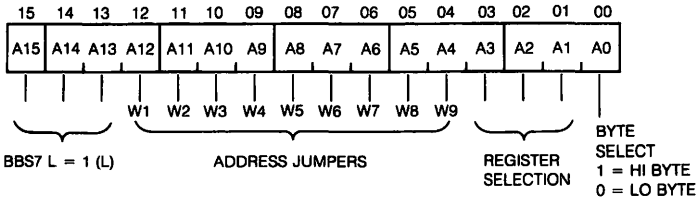


Figure 39-2 ▪ DRV11-J Device Address Format

Interrupt Vector Address

The DRV11-J can be programmed to operate in systems that are either interrupt-driven or software-polled. If the DRV11-J is used in an interrupt-driven system, the interrupt vector addresses must be programmed into a RAM (vector address memory) contained in the two interrupt controller chips, E2 and E10.

A total of 16 vector addresses can be stored in the vector address memory. Although the vector address bits <0:7> provide the capability of programming addresses from 0000 through 1774 (see Figure 39-3), the vector addresses actually assigned must be selected from the floating vector space — from 300 to 776.

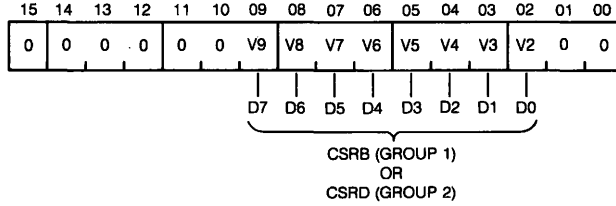


Figure 39-3 ▪ DRV11-J Vector Address Format

▪ Cables and Cabinet Kits

The BC05W cable can be used to connect the DRV11-J to user devices or to link two Q-buses together through two DRV11-Js. The BC05W is a flat, shielded cable with 50-pin connectors at both ends. It is available in lengths of 0.6 m (2 ft), 3.0 m (10 ft) and 7.6 m (25 ft).

A maximum cable length of 25 feet is specified for the distance between two DRV11-Js or from a DRV11-J to a user device with an ac load equivalent to the DRV11-J. The maximum cable length may have to be shortened if the ac load of the user device is greater than the ac load of the DRV11-J.

When ordered at the same time as the system in which it is to be installed, the DRV11-J option (model number DRV11-JP) includes the base module (M8049), internal cables, and the I/O connection panel insert. When ordered as a system upgrade, the DRV11-J option includes the base module only. One of the following cabinet kits should be chosen for system installation:

CK-DRV1J-KA	For use with the BA23 enclosure
CK-DRV1J-KB	For use with the BA11-M enclosure
CK-DRV1J-KC	For use with the H349 distribution panel

Chapter 40 • DRV11-WA General Purpose DMA Interface

The DRV11-WA is a general purpose, direct memory access (DMA) interface for transferring 16-bit data words directly between any LSI-11 microcomputer memory and a user's I/O device.

• Specifications

Identification	M7651
Size	Dual
Power Requirements	+5V at 1.8 A (nominal)
Bus Loads	
ac	2.0
dc	1.0
User I/O Connections	Two 40-pin connectors
Line Loading	
Input Data Lines	1 TTL unit load each
Input Control Lines	1 TTL unit load each
Output Data Lines	10 TTL unit loads each
Output Control Lines	10 TTL unit loads each
Logic Levels	High = logic 1 Low = logic 0
Transfer Mode	DMA or program-controlled with interrupts
Data Transfer Rate	Up to 250,000 16-bit words per second in single-cycle mode Up to 500,000 16-bit words per second in burst mode

Note

While doing burst mode transfers, the DRV11-WA becomes bus master and holds the bus until the entire transfer is complete. This action can potentially lock out other devices from accessing the bus while the transfers are ongoing. This mode of operation is consistent with the operation of the 18-bit predecessor product, DRV11-B.

Nonstandard Environmental Specifications	
Operating Temperature	5°C to 50°C (41°F to 122°F)

▪ Related Documentation

Document Title	**Order Number**
DRV11-WA General Purpose DMA Interface User's Guide	EK-DRVWA-UG
DRV11-WA Field Maintenance Print Set	MP-01582-01
DRV11 Diagnostic Documentation Kit	ZJ244-RZ

▪ Configuration

The DRV11-WA is configured by means of two address selection switchpacks, as shown in Figure 40-1. The user can configure the base device address, the interrupt vector address, and the bus addressing mode.

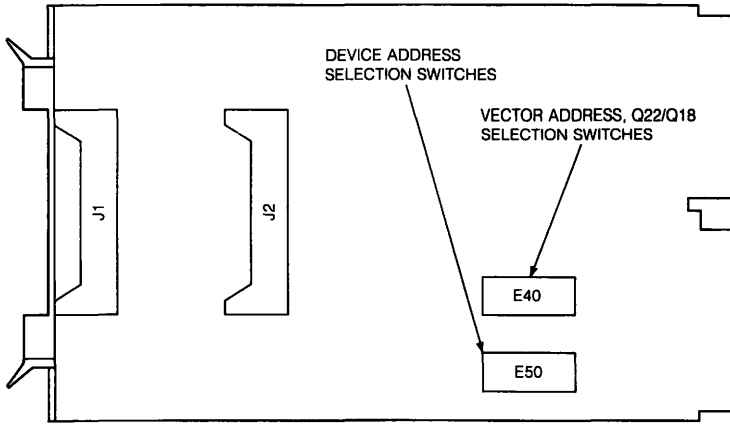


Figure 40-1 ▪ DRV11-WA Connector and Switch Locations

Device Address

The DRV11-WA contains six device registers, as listed in Table 40-1. The factory-configured DMA interface base address is 772410. The user can select another base address for assignment to the word count register by setting the address in the device address selection switches on the module. The remaining register addresses are then decoded by the module, as shown in Table 40-1.

The location of the device address selection switches is shown in Figure 40-1. Switches are set to the ON (closed) position for bits to be encoded as a 1 in the base address. Switches set to the OFF (open) position are encoded as a 0 in the base address. Figure 40-2 shows the address select format and presents the switch-to-bit relationship for the device address selection.

Table 40-1 ▪ DRV11-WA Standard Register Address Assignments

Register	Mnemonic	Status	Address
Word Count Register	WCR	R/W	772410
Bus Address Register	BAR	R/W	772412
Bus Address Extension Register	BAE	R/W	772412
Control and Status Register	CSR	R/W	772414
Input Data Buffer Register	IDBR	R-O	772416
Output Data Buffer Register	ODBR	W-O	772416

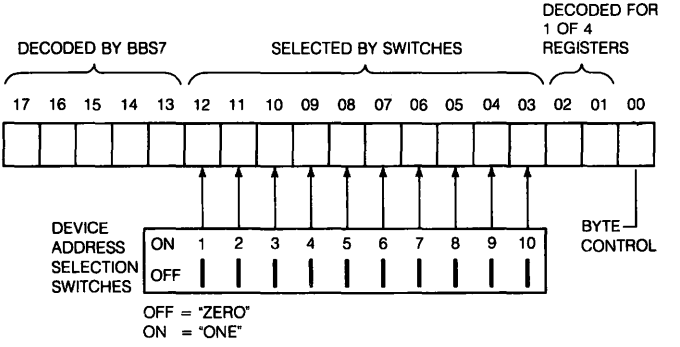


Figure 40-2 ▪ DRV11-WA Device Address Selection

Interrupt Vector Address

Vector addresses 0-774 are reserved for LSI-11 system users. The DRV11-WA is factory-configured with a vector address of 124. The user can select another vector address by reconfiguring the vector address selection switches on the module, shown in Figure 40-1.

Vector address selection switches are set to the ON (closed) position to encode a logical 1 in the corresponding address bit. Switches are set to the OFF (open) position to encode a logical 0. Figure 40-3 shows the address select format and the switch-to-bit relationship for the vector address selection.

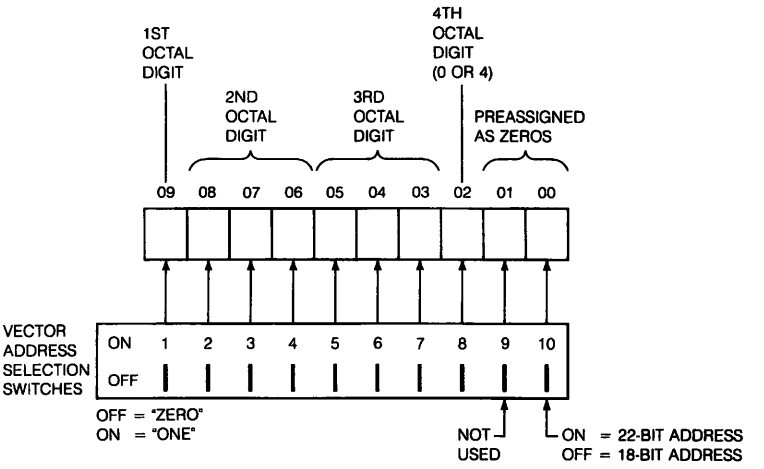


Figure 40-3 ▪ DRV11-WA Interrupt Vector Address Selection

Addressing Mode

The user selects either 18- or 22-bit addressing by means of switch 10 of switchpack E40. Setting this switch to the OFF position selects 18-bit addressing; setting it to the ON position selects 22-bit addressing (see Figure 40-3).

▪ Cables and Cabinet Kits

The DRV11-WA has two 40-pin connectors that provide the interface to the user's device. Two cable assemblies are required. Recommended cables assemblies are listed in Table 40-2. The listed cables are terminated (one or both sides) with H856 40-pin connectors that mate with the connectors on the DRV11-WA.

Cable selection is determined by the type of connections used on the user's device. The desired cable length (xx) must be specified when ordering. (Lengths longer than 25 feet are not recommended for use with the DRV11-WA.

Table 40-2 ▪ Recommended DRV11-WA Cable Assemblies

Cable No.	Connectors	Type	Standard Lengths
BC08R-xx	H856 to H856	Shielded flat	1, 6, 10, 12, 20, 25 ft (0.305, 1.830, 3.050, 3.660, 6.100, 7.625 m)
BC04Z-xx	H856 to open	Shielded flat	6, 10, 15, 25 ft (1.830, 3.050, 4.575, 7.625 m)

When ordered at the same time as the system in which it is to be installed, the DRV11-WA option includes the base module (M7651), internal cables, and the I/O connection panel insert. When ordered as a system upgrade, the option includes only the base module. One of the following cabinet kits should be chosen for system installation:

CK-DRV1B-KA	For use with the BA23 enclosure
CK-DRV1B-KB	For use with the BA11-M enclosure
CK-DRV1B-KC	For use the H349 distribution panel

Chapter 41 • IBV11-A Instrument Bus Interface

The IBV11-A is an option that interfaces the Q-bus with the instrument bus as described in IEEE Standard 488-1975, "Digital Interface for Programmable Instrumentation."

• Specifications

Identification	M7954
Size	Dual
Power Requirements	+5 Vdc ±5% at 0.8 A (typical)
Bus Loads	
ac	1.9
dc	1.0

When connected to the Q-bus, the IBV11-A meets the following subsets of IEEE Standards 488-1975:

SH1	SR1	C1
AH1	RL1	C2
TS	PP2	C3
TE5	DC1	C4
LE3		

This module is designed to be the only controller on the IEEE bus. Therefore, it will not respond to another controller on the bus that issues either a parallel poll configure command or a parallel poll control signal.

• Related Documentation

Document Title	**Order Number**
IBV11-A LSI-11/Instrument Bus Interface User's Manual	EK-IBV11-TM
Digital Interface for Programmable Instrumentation	(IEEE Std. 488- 1975)
IBV11-A Field Maintenance Print Set	MP-00274-00

• Configuration

The IBV11-A option can be installed in any Q-bus to interface various instruments via an "interrupt bus." The instrument bus is defined in the IEEE Standard 488-1985, "Digital Interface for Programmable Instrumentation." Any instruments designed to interface with the bus defined in that standard can be interfaced to the Q-bus system via the IBV11-A.

The IBV11-A is configured by means of two switchpacks located on the module (see Figure 41-1). Switchpack S1 is used to configure the interrupt vector address; switchpack S2 is used to configure the device address.

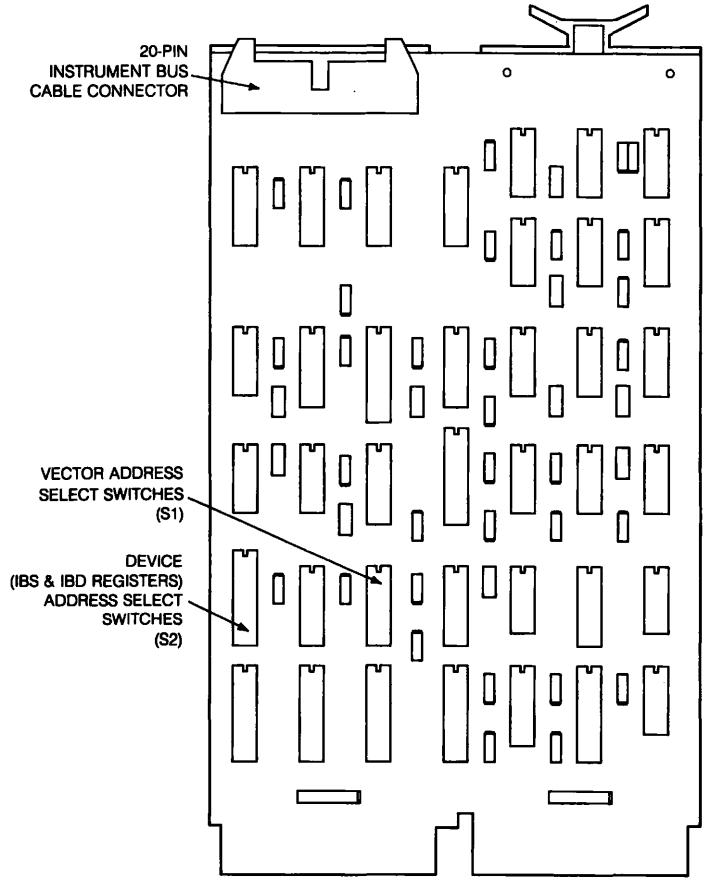


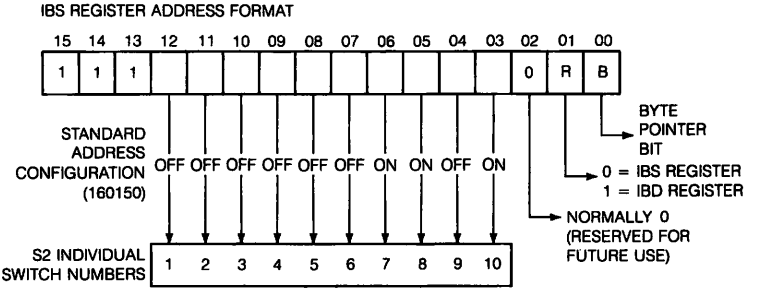
Figure 41-1 ▪ IBV11-A Switch Locations

Device Address

The two registers used by the IBV11-A are listed in Table 41-1. The IBV11-A device address is the address assigned to the control and status register. This address is selected using switchpack S2, and can be located anywhere between 160000 and 177776. A switch in the ON position encodes a logical 1 in the corresponding device address bit; a switch in the OFF position encodes a logical 0. The switch-to-bit assignments are shown in Figure 41-2. The IBV11-A is factory-configured with a device address of 160150.

Table 41-1 ▪ IBV11-A Standard Address Assignments

Description	Mnemonic	Status	Address
Registers:			
Control/Status Register	IBS	R/W	160150
Data Register	IBD	R/W	160152
Interrupt Vectors:			
Error Vector	ER2, ER1		420
Service Vector	SRQ		424
Command and Talker Vector	CMD, TKR		430
Listener Vector	LNR		434



NOTES:
1. OFF = LOGICAL 0; ON = LOGICAL 1
2. ONLY THE IBS REGISTER ADDRESS IS CONFIGURED VIA S2. THE IBD REGISTER ADDRESS ALWAYS EQUALS THE IBS REGISTER ADDRESS +2.

Figure 41-2 ▪ IBV11-A Device Address Selection

Interrupt Vectors

The IBV11-A can generate four separate interrupts, as listed in Table 41-1, and therefore requires four consecutive interrupt vectors. Interrupts are prioritized in the IBV11-A. A summary of the four interrupts is given in Table 41-2.

The base vector address can be assigned in the range of 0-360 by setting switches 1 through 5 of switchpack S1. A switch in the ON position encodes a logical 1 in the corresponding vector address bit; a switch in the OFF position encodes a logical 0. The switch-to-bit assignments are shown in Figure 41-3. The IBV11-A has a factory-configured vector address of 420.

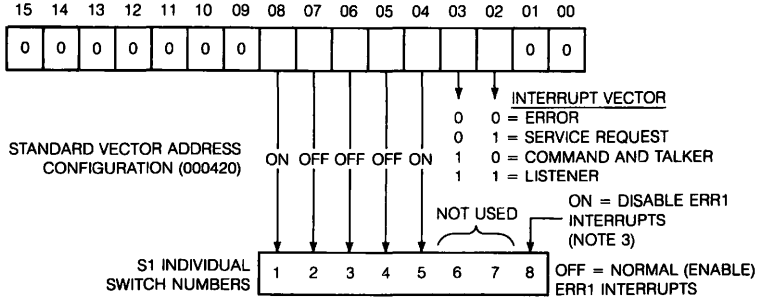
Switch 8 of switchpack S1 is used to enable (the OFF position) or disable (the ON position) the ER1 interrupt.

Switches 6 and 7 of switchpack S1 are unused.

Table 41-2 ▪ IBV11-A Interrupt Summary

Priority	Interrupt	Vector	Cause of Interrupt
Highest	ER2, ER1	XXX+00	Error condition
Second highest	SRQ	XXX+04	A device connected to the instrument bus is requesting service.
Third highest	TKR, CMD	XXX+10	The IBV11-A is an active talker and is ready for the processor to output a byte to the low byte of the IBD register. (The IBV11-A will normally then transmit the byte over the installation bus to the active listener(s).)
Lowest	LNR	XXX+14	The IBV11-A is an active listener and has a data byte to be read by the processor.

XXX = User-configured interrupt vector address



NOTES:

1. OFF = LOGICAL 0; ON = LOGICAL 1
2. ONLY THE VECTOR ADDRESS BITS (8 : 4) ARE CONFIGURED VIA S1. BITS 3 AND 2 ARE IBV11-A HARDWARE-SELECTED FOR THE FUNCTIONS SHOWN.
3. S1-8 OFF = IBV11-A IS THE ONLY SYSTEM CONTROLLER CONNECTED TO THE INSTRUMENT BUS; ERR1 INTERRUPTS ENABLED. S1-8 ON = ANOTHER SYSTEM CONTROLLER IS CONNECTED TO THE INSTRUMENT BUS; ERR1 INTERRUPTS DISABLED.

Figure 41-3 ▪ IBV11-A Vector Address Selection

▪ Cables and Connectors

The IBV11-A is connected to the first device on the instrument bus via a BN11A cable (supplied with the module), as shown in Figure 41-4. One end is terminated with a 20-pin connector that mates with the 20-pin connector on the IBV11-A module; the other end is terminated with a 24-pin double-ended connector that conforms to the IEEE 488-1975 standard — the cable can be connected to any device conforming to that standard. The double-ended connector contains a male 24-pin and a female 24-pin connector in the same housing. These allow for "linear" and "star" connections to instruments connected to the instrument bus, as shown in Figure 41-5. One BN11A cable is required for each IBV11-A module in a system.

The linear arrangement shown in the figure includes five devices (or instruments), A through E. There is no particular significance to the sequence shown, or the electrical position along the instrument bus. Unlike the Q-bus, the position along the bus does not structure device priority in the system.

The star arrangement shown in the figure allows five devices to be connected by stacking instrument cable connectors on the BN11A's double-ended connector. Double-ended connectors on instrument bus cables will normally include captive locking screws on each connector assembly (two each), allowing stacked connectors to be secured together in a single assembly.

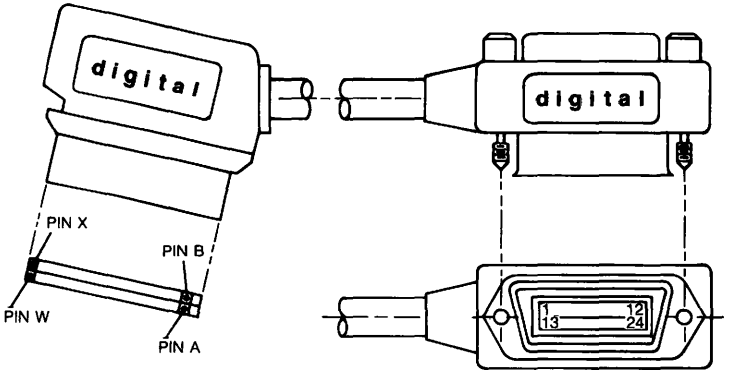


Figure 41-4 ▪ BN11A Instrument Bus Cable

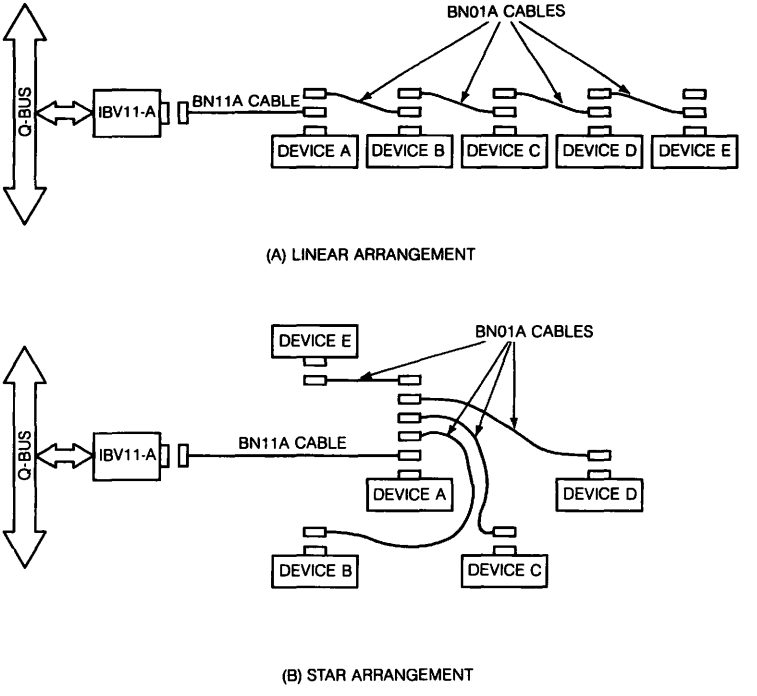


Figure 41-5 ▪ Linear and Star Configurations

Optional Cables

To connect the M7954 module to the first instrument:

BN11A-02	2 m (78.7 in)
BN11A-04	4 m (157.5 in)

To connect instrument to instrument:

BN01A-01	1 m (39.4 in)
BN01A-02	2 m (78.7 in)
BN01A-04	4 m (157.5 in)

Note

The IBV11-A is available as an **add-on option** for installation by technically experienced customers. It is compatible with the system backplane but is not installed in a Digital manufacturing facility. The IBV11-A option does not include an I/O connection panel insert, nor is it qualified for use in an FCC Class A system.

Chapter 42 ▪ IEQ11-A DMA Interface Option

The IEQ11-A option is a DMA controller that interfaces a Q-bus system to two independent instrument buses (IEC/IEEE). These instrument buses conform to both the European Standard IEC 625-1 and the U.S. Standard IEEE 488-1978. Each instrument bus can have up to fifteen devices (including the IEQ11-A option itself) in a sequential configuration.

▪ Specifications

Identification	M8634
Size	Quad
Power Requirements	+5 Vdc ±5%, 3.0 A
Logic Levels	TTL
Bus Loads	
ac	2.0
dc	1.0
IEC/IEEE Bus Load	1
Operating Mode	Programmed I/O transfers with interrupt DMA data transfers, byte addressing
Transfer Rate	Up to 150 Kbytes/sec during a DMA block transfer
Maximum Block Length	65 Kbytes
Addressable Memory Range	256 Kbytes (18-bit) 4 Mbytes (22-bit)
Priority Level	BR4
Nonstandard Environmental Specifications	
Operating Temperature	5°C to 50°C (41°F to 122°F)

▪ Related Documentation

Document Title	Order Number
PDP-11 Bus Handbook	EB-17525-20
IEQ11-A Field Maintenance Print Set	MP-01180-00
IEU/IEQ Diagnostic Documentation Kit	ZJ361-RZ
IEU11-A/IEQ11-A User's Guide	EK-IEUQ1-UG
Service Information Guide for IEC/IEEE Bus Interfaces	EY-1064E-PO

▪ Configuration

The IEQ11-A interface module (M8634) is configured by means of two DIP switchpacks and eight jumpers, as shown in Figure 42-1. These switches and jumpers are used to select the following items:

- Device address
- Interrupt vector address
- Backplane type
- Interrupt priority level

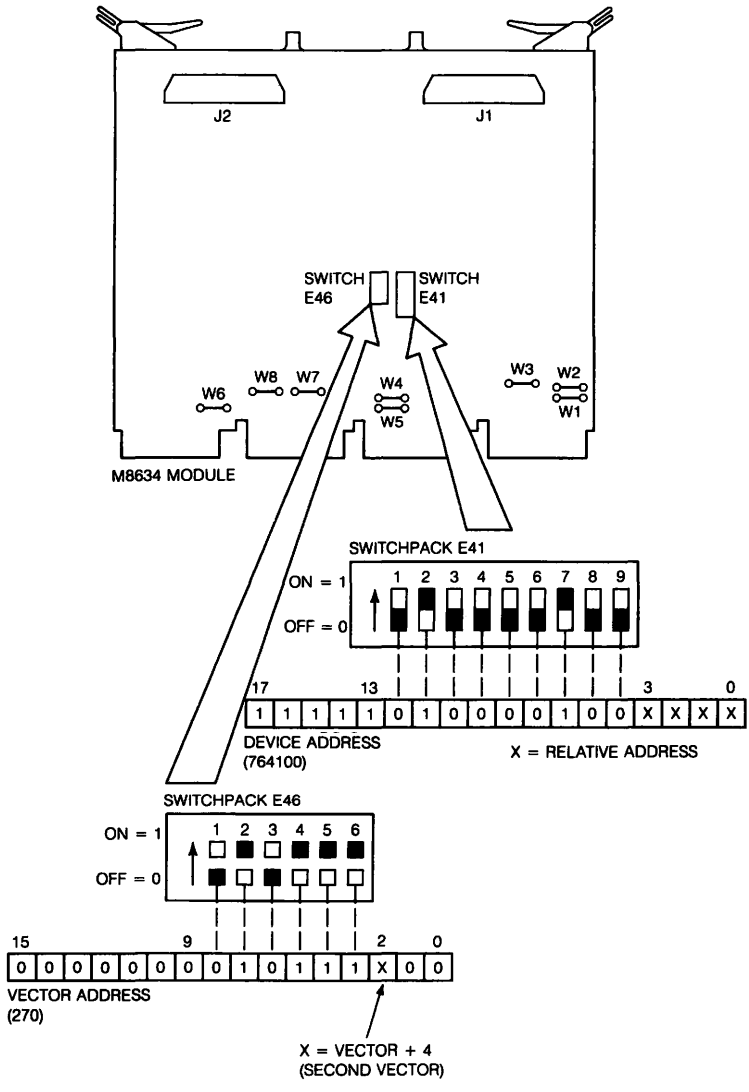


Figure 42-1 ▪ M8634 Module Layout

Device Address

The IEQ11-A interface module contains a set of eight device registers used for program control. The module device address is the address assigned to the first of these eight registers. The IEQ11-A is factory-configured for a device address of 17764100. If the system configuration requires another address (for example, if this is the second of two IEQ11-A modules in the system), the switches in DIP switchpack E41 must be configured for the new address.

A switch set to the ON position encodes a logical 1 in the corresponding device address bit; a switch set to the OFF position encodes a logical 0. Table 42-1 lists the switch-to-bit relationship for the device address selection switches.

Table 42-1 ▪ IEQ11-A Device Address Switches

E41 Switch	1	2	3	4	5	6	7	8	9
Address Bit	12	11	10	9	8	7	6	5	4

Interrupt Vector Address

The IEQ11-A can generate two independent interrupts (one for each bus that it can monitor), and therefore requires two consecutive interrupt vectors. The vector address for which the module is configured is the address assigned to the first of the two interrupt vectors. The IEQ11-A is factory-configured for a starting vector address of 270. If the system configuration requires another address (for example, if this is the second of two IEQ11-A modules in the system), the switches of DIP switchpack E46 must be configured for the new address.

A switch set to the ON position encodes a logical 1 in the corresponding vector address bit; a switch set to the OFF position encodes a logical 0. Table 42-2 lists the switch-to-bit relationship for the vector address selection switches.

Table 42-2 ▪ IEQ11-A Interrupt Vector Address Switches

E46 Switch	1	2	3	4	5	6
Address Bit	8	7	6	5	4	3

Backplane and Continuity Jumpers

The IEQ11-A interface module can be installed in any Q-bus backplane that accepts quad-height modules. It can support either 18-bit or 22-bit addressing. Jumpers W1 through W3 must be configured to accommodate the specific backplane used. In addition, jumpers W7 and W8 must be properly configured to provide continuity for the interrupt acknowledge (BIAK) and direct memory access grant (BDMG) bus signals. Table 42-3 summarizes this backplane-dependent jumpering.

Table 42-3 ▪ IEQ11-A Backplane Configuration Jumpers

Backplanes	Q-Bus Structure Slot A/B	Slot C/D	Module Jumper Settings W1	W2	W3	W7	W8
H9276	22-bit Q-bus	CD-bus	Out	In	In	Out	Out
H9273	18-bit Q-bus	CD-bus	In	Out	Out	Out	Out
H9275	22-bit Q-bus	22-bit Q-bus	Out	In	In	In	In
H9270	18-bit Q-bus	18-bit Q-bus	In	Out	Out	In	In
DDV11-B	18-bit Q-bus	18-bit Q-bus	In	Out	Out	In	In

Note

If the IEQ11-A interface module is installed in a Q/CD backplane and the jumpers W7 and W8 are installed, pin CM1 is shorted to CN1 and pin CR1 is shorted to CS1 on the adjacent higher-numbered slot. These connections can be obstructive in some cases and should be deleted by removing the jumpers.

Interrupt Priority Level

The IEQ11-A interface module is factory-configured to support only one interrupt level (BIRQ 4). However, the module can accept the multilevel interrupt chip, if desired. The desired interrupt level can then be selected by configuring jumpers W4 through W6, as shown in Table 42-4.

Table 42-4 ▪ IEQ11-A Interrupt Priority Level Jumpers

Interrupt Level	W4	W5	W6
BR 4	In	In	In
BR 5	In	Out	Out
BR 6	Out	Out	In
BR 7	Out	In	Out

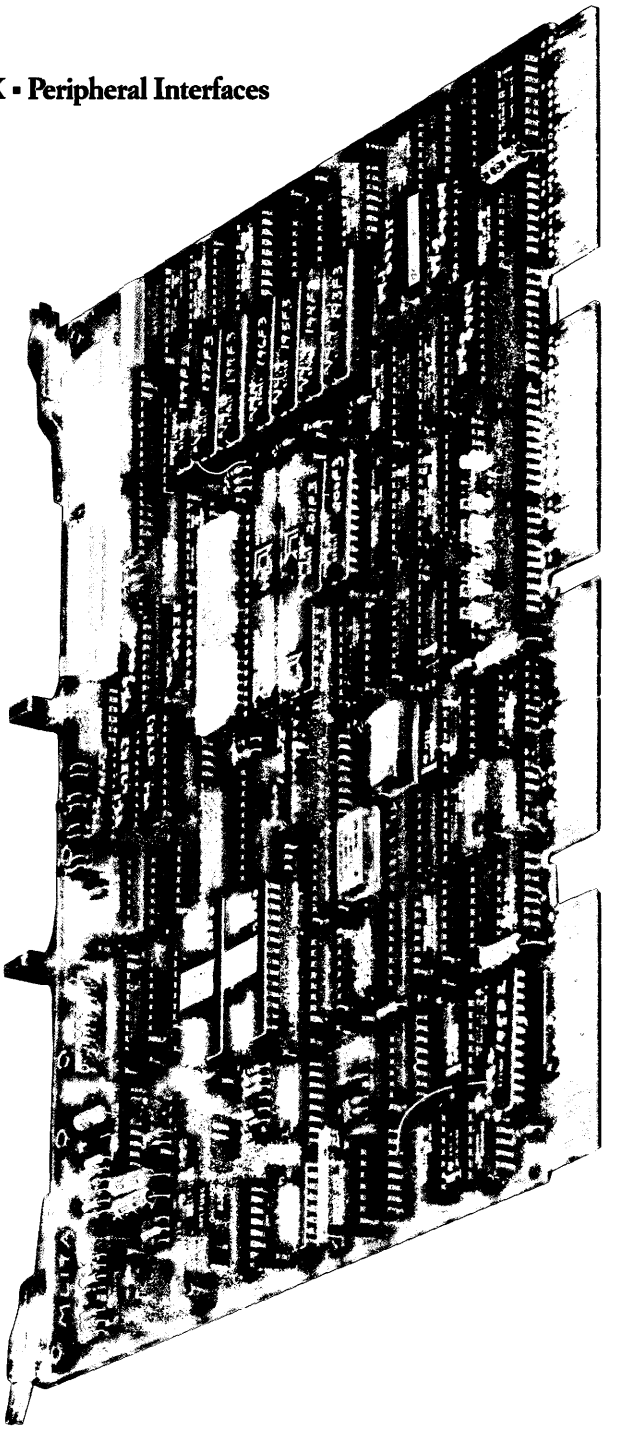
▪ Cables

The IEQ11-A interface module is connected to the IEC bus by the bulkhead/cable assembly BN11E-01 and to the IEEE bus by the bulkhead/cable assembly BN11F-01. In addition to these parts, the following items are also available from Digital:

- IEC standard cable (BN01C-02) that can be used as an interconnecting cable on the IEC bus.
- IEEE standard cable (BN01A-02) that can be used as an interconnecting cable on the IEEE bus.

Up to fifteen devices (including the IEQ11-A interface module) can be connected to the IEC/IEEE bus I, as well as to the IEC/IEEE bus II. The maximum length of cable that can be used to connect two devices is 2 meters, and the total transmission path length over the interconnecting cables cannot exceed 20 meters.

Part IX • Peripheral Interfaces



Chapter 43 • Introduction to Peripheral Interfaces

Digital offers a variety of peripheral options for use in Q-bus systems.

• LPV11 Printer Option

The LPV11 printer option consists of an interface module, an interface cable, and either an LP05 or an LA180 line printer. The interface module provides programmed control of data transfers and provides printer strobe signals appropriate for either printer. The LA180 DECprinter is a high-speed printer that prints 180 characters per second. The LP05 printer can print 240 or 300 lines per minute, depending on the model selected.

• RLV12 Disk Controller

The RLV12 disk controller interfaces up to four RL01/02 disk drives to any Q-bus system. The RL01 and RL02 are random-access, mass storage subsystems that store data in fixed-length blocks on a preformatted disk cartridge. Each RL01 can store 5.24 million bytes and each RL02 can store 10.48 million bytes. The RLV12 transfers data to and from the Q-bus using direct memory access (DMA) transactions. The RLV12 supports 18- or 22-bit addressing.

• RQC25 Disk Controller

The RQC25 is a disk controller module that interconnects the RC25 fixed/removable disk subsystem to any Q-bus system. The RC25 disk subsystem has 52 Mbytes of formatted user data — a 26-Mbyte fixed Winchester disk combined with a 26-Mbyte sealed removable cartridge. Because it uses the Mass Storage Control Protocol (MSCP), the RC25 is compatible with other Digital Storage Architecture disk subsystems.

• RQDX1 Disk Controller

The RQDX1 is an intelligent controller with an onboard microprocessor used to interface the Q-bus with 11-Mbyte RD51 and 31-Mbyte RD52 Winchester disk drives as well as 0.8-Mbyte RX50 dual diskette drives. Data is transferred to the host system via block-mode DMA. Programs in the host system communicate with the controller and disk drives using the Mass Storage Control Protocol (MSCP) of the Digital Storage Architecture.

▪ RXV21 Floppy Disk Option

The RXV21 floppy disk option is a random-access, mass storage device that stores data in fixed-length blocks on a preformatted, flexible diskette. Each diskette can store and retrieve up to 512 Kbytes of data. The RXV21 system consists of an interface module, an interface cable, and either a single or dual RX02 floppy disk drive. The interface module converts the RX02 I/O bus to the Q-bus structure. It controls interrupts, decodes device addresses for register selection, and handles the data exchange between the RX02 and the processor using DMA data transfers.

▪ TQK25 Streaming Tape Drive Interface

The TQK25 interface connects the Q-bus to an external TK25 streaming tape drive. The TK25 is a cartridge tape drive designed for fast backup of the high capacity mini-Winchester disks. The TK25 will serially record up to 60 Mbytes on a ¼-inch tape cartridge.

▪ TSV05 Tape Transport Subsystem

The TSV05 tape transport subsystem provides magnetic tape storage capabilities to Q-bus systems. The subsystem reads or writes up to 160 Kbytes per second in ANSI standard format. Data is recorded by phase encoding 1,600 bits per inch on nine-track tape. Tape formatting, error detection and correction, and self-test diagnostics are included as integral components of the TSV05 subsystem.

▪ TU58 Cartridge Tape Drive

The TU58 is a low-cost intelligent mass storage device that offers random access to block-formatted data on pocket-size cartridge media. It is ideal as an inexpensive archive mass storage or as a software update distribution medium. A dual-drive TU58 offers 512 Kbytes of storage space.

Chapter 44 ▪ LPV11 Printer Option

The LPV11 printer option is a high-speed line printer system for use with a Q-bus system. There are 12 option numbers (listed in Table 44-1) that define the type of printer used and four primary power (line) voltages.

Table 44-1 ▪ LPV11 Option Model Numbers

Option No.	Primary Power	Printer Model
LPV11-PA	115 V, 60 Hz	LA180-PA
LPV11-PB	230 V, 60 Hz	LA180-PB
LPV11-PC	115 V, 50 Hz	LA180-PC
LPV11-PD	230 V, 50 Hz	LA180-PD
LPV11-VA	115 V, 60 Hz	LP05-VA
LPV11-VB	230 V, 60 Hz	LP05-VB
LPV11-VC	115 V, 50 Hz	LP05-VC
LPV11-VD	230 V, 50 Hz	LP05-VD
LPV11-WA	115 V, 60 Hz	LP05-WA
LPV11-WB	230 V, 60 Hz	LP05-WB
LPV11-WC	115 V, 50 Hz	LP05-WC
LPV11-WD	230 V, 50 Hz	LP05-WD

▪ Specifications

Interface Module

Identification	M8027
Size	Dual
Power Requirements	+5 Vdc, at 0.8 A (typical), 1.4 A (maximum)
Bus Loads	
ac	1.4
dc	1.0
LP05 Line Printer	
Power Requirements	115 Vac ± 10% 50 to 60 Hz ± 3 Hz or 230 Vac ± 10% 50 to 60 Hz ± 3 Hz 700 W

Printer Characteristics	
Print Rate	LP05-Vx: 300 lines/min LP05-Wx: 240 lines/min
Characters per Line	132
Character Set	LP05-Vx: uppercase only LP05-Wx: uppercase and lowercase
Dimensions	Height: 1.14 m (45 in) Width: 0.81 m (32 in) Depth: 0.56 m (22 in) Weight: 150 kg (330 lb)
Environmental	
Operating Temperature	10°C to 32°C (50°F to 90°F)
Humidity	30% to 90% (no condensation)
LA180 DECprinter	
Power Requirements	90-132 Vac or 180-264 Vac 50 or 60 Hz ± 1 Hz 400 W maximum (printing) 200 W maximum (idle)
Printer Characteristics	
Print Rate	180 characters/s
Characters per Line	132
Character Set	Uppercase and lowercase

▪ Related Documentation

Document Title	**Order Number**
LP25 Line Printer Maintenance Guide	ER-0LP25-5V
LPV11 Printer User's Manual	EK-LPV11-OP
LA180 DECprinter I User's Manual	EK-LA180-OP
LA180 Field Maintenance Print Set	MP-LA180-00
LA180 DECprinter I Maintenance Manual	EK-LA180-MM
LP05 Technical Manual, Model 2230 Line Printer	Dataproducts Corporation
LPV11-V Field Maintenance Print Set	MP-00467-00

▪ Configuration

The LPV11 interface module is shipped from the factory with jumpers configured for standard (Digital software-compatible) device and interrupt vector assignments. It is normally not necessary for the user to configure the address or vector jumpers unless special device addresses and/or interrupt vectors are desired. The factory-installed jumpers are shown in Figure 44-1. These jumpers can be removed by carefully cutting each end close to the printed circuit board.

In addition to the factory jumpers, there is an alternate set of wirewrap pins that allow the user to install additional or replacement jumpers by using the designated wirewrap pins. In Figure 44-1, the dots represent wirewrap pins and a line indicating a pair of pins shows the electrical connection that must be wirewrapped to insert that jumper. Table 44-2 lists the factory jumpers installed and the additional jumpers that can be installed, as well as the associated functions. The factory-set addresses are listed in Table 44-3.

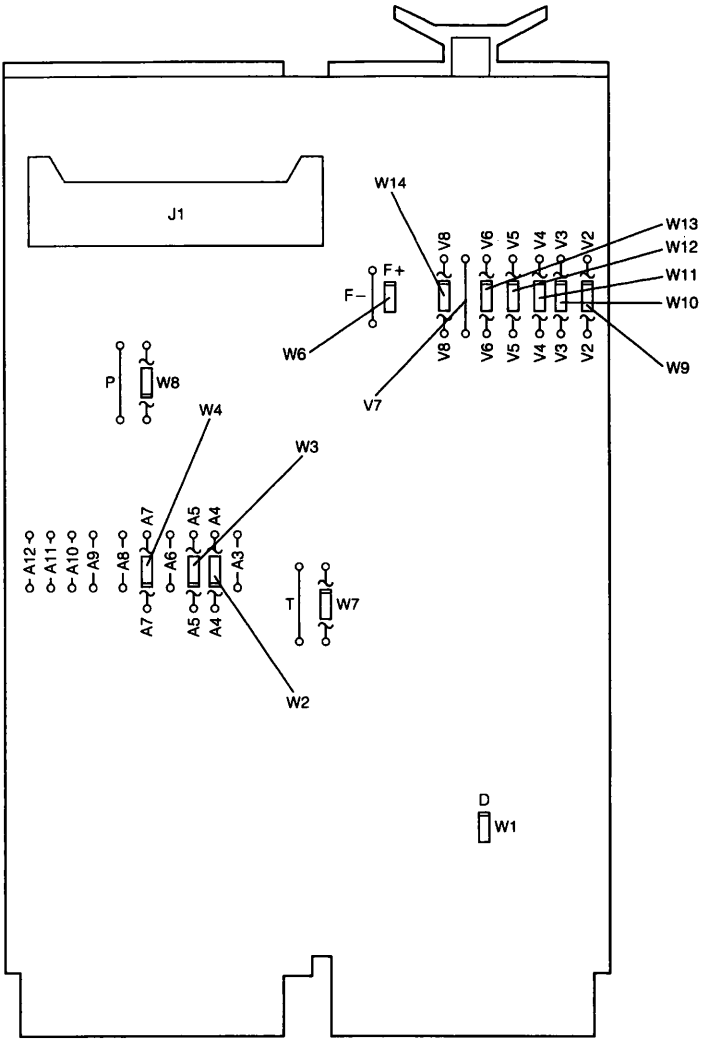
Note

Jumpers F+ (factory-installed W6) and F- do not have associated wirewrap pins. These jumpers must be installed by soldering and removed by cutting or unsoldering.

Table 44-2 ▪ LPV11 Jumper Designations

Jumper*	Function
A3	Device Address
A4 (W2)	Device Address
A5 (W3)	Device Address
A6	Device Address
A7 (W4)	Device Address
A8	Device Address
A9	Device Address
A10	Device Address
A11	Device Address
A12	Device Address
F (W6)	Error Filter
P	Parity
T (W7)	Translate to Uppercase
V2 (W9)	Interrupt Vector
V3 (W10)	Interrupt Vector
V4 (W11)	Interrupt Vector
V5 (W12)	Interrupt Vector
V6 (W13)	Interrupt Vector
V7	Interrupt Vector
V8 (W14)	Interrupt Vector
D (W1)	Bus Reply Timing

* Jumpers without W designation are not normally factory-installed.



NOTE:

♀ = JUMPERS BROKEN FOR CLARITY ON THIS FIGURE. THESE WIREWRAP JUMPERS WOULD NORMALLY BE USED TO REPLACE PREVIOUSLY REMOVED FACTORY INSTALLED (W) JUMPERS (SHOWN INSTALLED).

o = WIREWRAP PIN.

Figure 44-1 ▪ LPV11 Jumper Locations

Table 44-3 ▪ LPV11 Standard Address Assignments

Description	Mnemonic	Status	Address*
Registers:			
Control and Status Register	LPCS	R/W	177514
Data Buffer Register	LPDB	R/W	177516
Interrupt Vector:			
DONE or ERROR			200

* Second module addresses are placed in floating device address and floating vector address space.

Device Address

The LPV11 is factory-configured with a control and status register (LPCS) address of 177514. The data buffer register (LPDB) is always configured at LPCS+2. If more than one LPV11 option is installed in the system, or if special device addresses are required, remove and/or install jumpers (one for each LPCS address bit), as shown in Figure 44-2.

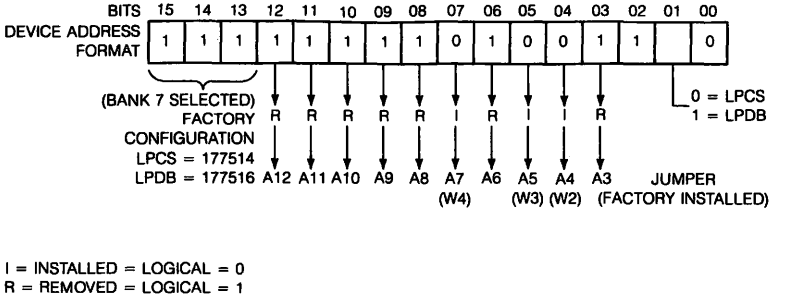


Figure 44-2 ▪ LPV11 Device Address Selection Jumpers

Interrupt Vector

The LPV11 is factory-configured with an interrupt vector address of 200. If more than one LPV11 option is installed in the system, or if a special interrupt vector is required, remove and/or install jumpers (one for each vector bit), as shown in Figure 44-3.

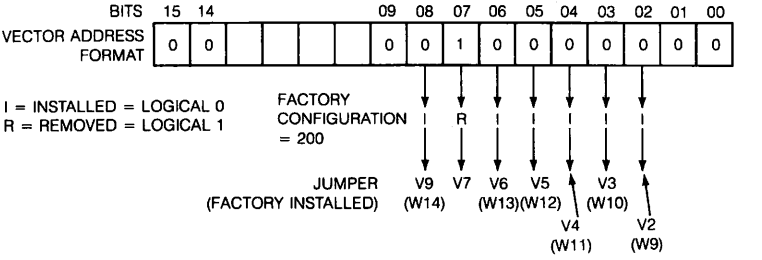


Figure 44-3 ▪ LPV11 Interrupt Vector Selection Jumpers

Bus Reply Timing

Jumper D (W1) is factory-installed to delay the BRPLY bus signal timing for LPV11 use with LA180 printers. If desired, this jumper can be removed for use with future printers. However, the LP05 will function if it is left installed.

Uppercase Only

Jumper W7 is factory-installed and jumper T is not installed, thereby enabling uppercase and lowercase letters to be printed. If lowercase letters are not desired, remove W7 and install jumper T. This will cause the LPV11 interface to translate all lowercase letters to uppercase before transmission to the printer. This feature allows files that have been configured for 96-character printers to be printed on 64-character printers with minimum software overhead.

Do not configure the module with both jumpers W7 and T installed.

Parity

Jumpers W8 and P select the desired parity mode. The LPV11 is factory-configured with W8 installed and jumper P not installed, thereby enabling parity bit 7 to be transmitted to the printer. Configure the parity option desired as shown in the following table. Do not configure the module with both jumpers W8 and P installed.

Parity Option	Jumper W8	Jumper P
Normal parity bit	Installed	Removed
No parity, bit 7 low	Removed	Removed
No parity, bit 7 high	Removed	Installed

Note

If the LPV11 interface module is used with an LP05 printer equipped with the Direct Access Vertical Form Unit (DAVFU), it is recommended that the user remove jumper W8. The LPV11 interface module does not support the DAVFU function.

Error Filter

The LPV11 interface module contains an error filter (time delay) circuit that is automatically selected when the module is used with an LA180 DECprinter. Jumper F+ (W6) is factory-installed, selecting the error filter for use with LP05 printers. However, its use with the LP05 is optional. If desired, remove the error filter by removing jumper W6 and installing F-. Do not configure the module with both F- and W6 installed.

▪ Cables

The following external cables are recommended for use with the LPV11 module:

BC11S-25	25 ft twisted-pair cable with H856 connector on each end, to connect to the LA180 printer
70-11212-25	40-pin Berg to Winchester LP11 interface cable to connect to the LP05 printer

Chapter 45 ▪ RLV12 Disk Controller

The RLV12 disk controller interfaces RL02 and RL01 disk drives to any quad- or hex-size backplane that uses 16-, 18-, or 22-bit Q-bus.

▪ Specifications

RLV12 Disk Controller

Identification	M8061
Size	Quad
Power Requirements	+5 Vdc ±5% at 5.0 A +12 Vdc ±5% at 0.1 A
Bus Loads	
ac	3.0
dc	1.0
Data Transfer Rates	4.9 μs/word (average) drive to controller, controller to memory 13.9 μs/word (peak) drive to controller 2.0 μs/word (peak) controller to memory
Error Detection Capability	Cyclic redundancy check (CRC) on data and headers. Memory parity error abort for use with memories that have parity checking.
RL01/RL02 Disk Drives	
Medium	Magnetic disk cartridge
Recording surfaces	2 data surfaces
Magnetic heads	2 read/write heads

Recording capacity (formatted)	**RL01**	**RL02**
Cylinders per cartridge	256	512
Tracks per cylinder	2	2
Tracks per cartridge	512	1024
Sectors per track	40	40
Bytes per sector	256	256
Bytes per track	10,240	10,240
Bytes per cylinder	20,480	20,480
Mbytes per cartridge	5.24	10.48
Recording method	Modified frequency modulation	
Performance		
Transfer Rate	40-sector (16-bit data words): 4.9 μs/word (avg) drive to controller, controller to memory; 3.9 μs/word (peak) drive to controller	
Head Positioning Time	55 ms (average); 17 ms (one track); 100 ms (maximum)	
Revolution Latency	12.5 ms (average)	
Operating Environment		
Temperature Range	10°C to 40°C (50°F to 114°F) at sea level	
Relative Humidity	10% to 90%, noncondensing	
Wet-bulb Temperature	28°C (82°F) maximum	
Altitude	Up to 2400 m (8000 ft) at maximum temperature of 36°C (96°F)	
Heat Dissipation	150 W (546 Btu/hr)	
Power		
Drive	Single-phase	
Starting Current	5 A (rms) maximum, 120 V, 47/63 Hz; 2.5 A (rms) maximum, 240 V, Hz	

Mechanical Drive	
Size	48 cm × 63.4 cm × 27 cm (19 in × 25 in × 10.5 in)
Weight	33.75 kg (75 lb)
Mounting	The drive mounts on slides in a standard 48.26 cm (19 in) cabinet (provided). Recommended maximum height from floor is 18.9 cm (48 in).
Cartridge	Embedded servo. Top-loading cartridge with two data surfaces.
Standard Length Cables	
Power cord	2.74 m (9 ft)
Controller to First Drive	1.83 m (6 ft)
Drive-to-drive	3.05 m (10 ft)

▪ Related Documentation

Document Title	Order Number
RLV12 Disk Controller User's Guide	EK-RLV12-UG
RLV12 Disk Controller Technical Description	EK-RLV12-TD
RLV12 Field Maintenance Print Set	MP-01282-00
RL01/RL02 User's Guide	EK-RL012-UG
RL01/RL02 Pocket Service Guide	EK-RL012-PS
RL01 Field Maintenance Print Set	MP-00347-00
RL01 Illustrated Parts Breakdown	EK-ORL01-IP
RL02 Field Maintenance Print Set	MP-00553-00
RL02 Illustrated Parts Breakdown	EK-ORL02-IP
RLV11/RL01/RL02 Diagnostic Documentation Kit	ZJ285-RZ

▪ Configuration

The RLV12 module is configured by means of several jumpers, as shown in Figure 45-1. The user can select the following features:

- Device address
- Interrupt vector address
- Bus addressing mode
- Memory parity error abort feature

Device Address Selection

Software control of the RLV12 is performed by four or five device registers — CSR, BAR, DAR, MPR, and BAE. Four registers are used for 16- or 18-bit addressing; five registers are used for 22-bit addressing. The bus address extension register (BAE) is added for upper address bit selection for 22-bit DMA addressing. The device starting address is assigned to the CSR, with the other registers being automatically assigned to the sequential addresses following, as shown in Table 45-1.

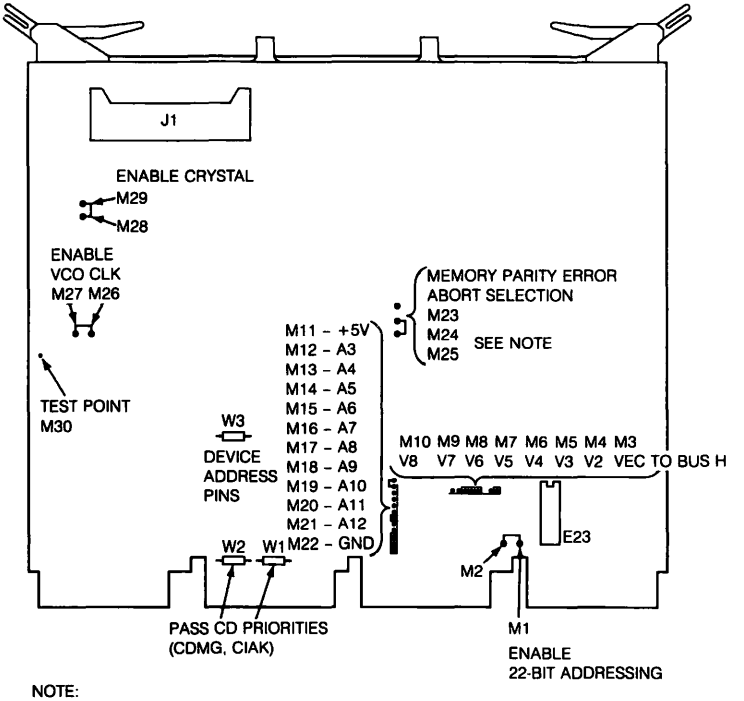
Bits <3:12> of the device starting address are selected by jumpers, as shown in Figure 45-1. A jumper connected to ground (M22) encodes a logical 1 in the corresponding address bit, an unconnected jumper encodes a logical 0, and a jumper connnected to 5V (M11) encodes an X (don't care) condition. Figure 45-2 shown the RLV12 device starting address format.

Note

For 22-bit addressing, bit A3 is not decoded in the starting address

Table 45-1 ▪ Address Selection

Device Address	**16-Bit Addressing**	**18-Bit Addressing**	**22-Bit Addressing**
Address Range	160000-177770	760000-777770	17760000-17777760
Standard Address	174400	774400	17774400
Number of Registers	4	4	8 (only 5 used)
Registers Used	CSR (174400) BAR (174402) DAR (174404) MPR (174406)	CSR (774400) BAR (774402) DAR (774404) MPR (774406)	CSR (17774400) BAR (17774402) DAR (17774404) MPR (17774406) BAE (17774410)
Jumpers Used	M22 ("1") to M17, M20, and M21	M22 ("1") to M17, M20, M21	M22 ("1") to M17, M20, and M21; M11 ("X") to M12
Interrupt Vector			
Address Range	0-774	0-774	0-774
Standard Address	160	160	160
Jumpers Used	M3 ("1") to M6, M7, and M8	M3 ("1") to M6, M7, and M8	M3 ("1") to M6, M7, and M8



NOTE:
THE MEMORY PARITY ERROR ABORT FEATURE IS AVAILABLE FOR USE WITH MEMORIES THAT HAVE PARITY ERROR CHECKING.
THIS FEATURE DOES NOT HAVE TO BE DISABLED FOR MEMORIES THAT DO NOT HAVE PARITY ERROR CHECKING. THE PINS ARE CONNECTED AS FOLLOWS:

CONNECTION	FUNCTION
M23 - M24	NO PARITY
M24 - M25	PARITY ERROR ABORT

Figure 45-1 ▪ RLV12 Jumper Locations

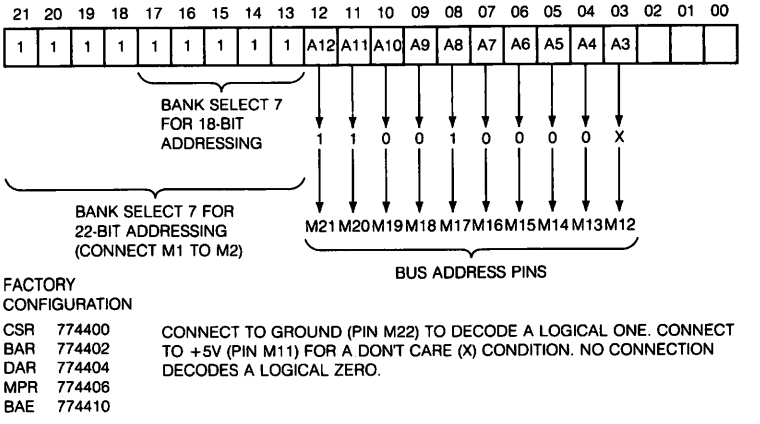


Figure 45-2 ▪ RLV12 Device Address Format

Bus Selection

The RLV12 module can be used in 16-, 18- or 22-bit Q-bus systems. When shipped from the factory, the module operates in 16- and 18-bit systems. To enable 22-bit operation, install jumper M1 to M2, shown in Figure 45-1. When installed, this jumper enables bank select 7 (BBS7) to be determined by the upper address bits <13:21>. When the jumper is removed, the RLV12 has an 18-bit mode bank select 7 and can replace an existing RLV11 as the disk controller for RL01 and RL02 disk drives.

Interrupt Vector

The interrupt vector address can be in the range of 0 to 774. The interrupt vector is preset at the factory to 160. The user can select another vector by changing the jumpers for vector address bits <2:8>, as illustrated in Figure 45-3. A connection to VEC TO BUS (pin M3, shown in Figure 45-1) generates a logical 1 for the corresponding bit; no connection generates a logical 0.

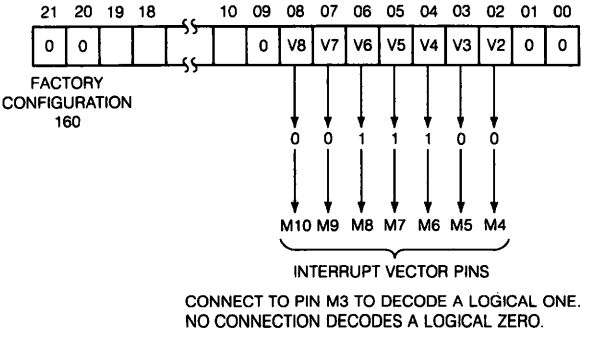


Figure 45-3 ▪ RLV12 Interrupt Vector Format

Interrupt Request Level
The RLV12 interrupts at priority level 4.

Memory Parity Error Abort Feature
When reading the system's optional memory with parity error detection, a parity error will set bits OPI and NXM of the CSR. This is a unique error condition that aborts the current command to the RLV12. This error abort feature is possible only with memories that have parity data bits.

The RLV12 is shipped from the factory with the memory parity error abort feature enabled. To disable the feature, remove the jumper between pins M24 and M25 and install a jumper between pins M23 and M24 (see Figure 45-1). This feature does not need to be disabled for nonparity memories because parity errors are not generated.

Jumpers That Remain Installed
The module has two jumpers, W1 and W2, that enable priority signals to pass through the module. The module is factory-configured with these jumpers installed, and they should be left in.

Jumper	Signal
W1	CIAKI to CIAKO
W2	CDMGI to CDMGO

One jumper, W3, enables the word count register to automatically increment during a DMA operation. This jumper is used for factory testing and should be left in.

Two jumpers on the module disable the crystal oscillator and the voltage-controlled oscillator (VCO) during factory testing. These jumpers should be left in.

Jumper	Oscillator
M26-M27	VCO
M28-M29	Crystal

▪ Cables and Cabinet Kits

The following optional external cables are available for use with the RLV12 disk controller module:

Cable	Part Number	Length
BC20J-20	7012122-20	6 m (20 ft)
BC20J-40	7012122-40	12 m (40 ft)
BC20J-60	7012122-60	18 m (60 ft)

Note

The total length of the cable(s) from the controller to the last drive must not exceed 30 m (100 ft).

When ordered at the same time as the system in which it is to be installed, the RLV12 option (model number RLV12-AP) includes the base module (M8061), internal cables, and the I/O connection panel insert. When ordered as a system upgrade, the RLV12 option includes the base module only. One of the following cabinet kits should be chosen for system installation:

CK-RLV1A-KA	For use with the BA23 enclosure
CK-RLV1A-KB	For use with the BA11-M enclosure
CK-RLV1A-KC	For use with the H349 distribution panel

Chapter 46 • RQC25 Adapter Module

The RQC25 adapter module interfaces the RC25 fixed/removable disk drive to any of the Q-bus microcomputers.

• Specifications

RQC25 Adapter Module

Identification	M7740
Size	Dual
Power Requirements	+5 V ±5%, 3.0 A (typical)
Bus Loads	
ac	2.3
dc	1.0
RC25 Disk Drive	
Physical Characteristics	
Tabletop model	
Height	25.6 cm (10.125 in)
Width	25.4 cm (10 in)
Depth	52.1 cm (20.5 in)
Weight	22.7 kg (50 lb)
Rackmount model	
Height	26.5 cm (10.5 in)
Width	48.3 cm (19 in)
Depth	56.2 cm (22.125 in)
Weight	
Single disk	295 kg (65 lb)
Dual disk	54.4 kg (120 lb)
Environmental Characteristics	
Operating	
Temperature	10°C to 40°C (50°F to 104°F)
Temperature change	10°C (18°F) per hour
Relative humidity	10% to 90% noncondensing
Wet bulb temperature	28°C (82°F) maximum
Dew point	2°C (36°F) minimum
Altitude	Sea level to 2.4 km (8000 ft)

Note

Decrease maximum operating temperatures by a factor of 1°C/1,000 ft (1.8°F/1,000 ft) for operation above sea level.

Nonoperating	
Temperature	-40°C to 66°C (-40°F to 151°F)
Temperature change	20°C (36°F) per hour
Relative humidity	5% to 95% noncondensing
Altitude	Up to 9.1 km (30,000 ft)
Heat dissipation	
Single disk	1,091 Btu/hr
Dual disk	1,828 Btu/hr
Noise level (single disk)	53 dB at 1 m
Electrical Characteristics	
Voltage/frequency	90-128 Vac, 6.6 A, 47-63 Hz 180-256 Vac, 3.5 A, 47-63 Hz
Operating power	
Single disk	320 W
Dual disk	536 W
Disk Capacity (Formatted)	
Single drive	26.06 Mbytes fixed disk 26.06 Mbytes removable cartridge 52.12 Mbytes total
Dual drive	52.12 Mbytes fixed disk 52.12 Mbytes removable cartridge 104.24 Mbytes total
Media	
Fixed	One 20 cm (7.875 in) double-sided nonremovable disk platter per drive
Removable	One 20 cm (7.875 in) double-sided disk platter in cartridge per drive
Seek Time	
Average seek	35 ms maximum
One track seek	10 ms maximum
Maximum seek	55 ms maximum
Latency	
Speed	2850 r/min ±9 r/min
Average rotational latency	10.5 ms
Maximum rotational latency	21.0 ms
Average access	45.5 ms

Start/Stop Time	
Start time	60 s maximum
Stop time	30 s maximum

▪ Related Documentation

Document Title	Order Number
RC25 Disk Subsystem User Guide	EK-0RC25-UG
RC25 Tabletop Slave Disk Drive Installation Guide	EK-RC25S-IN
RC25 Disk Subsystem Installation Guide	EK-0RC25-IN
RC25 Disk Subsystem Pocket Service Guide	EK-0RC25-PS
RC25 Illustrated Parts Breakdown	EK-0RC25-IP
RC25 Field Maintenance Print Set	MP-01612-00
RC25 Diagnostic Kit	ZJ350-RZ

▪ Configuration

There are ten switches and one jumper on the RQC25 adapter module (see Figure 46-1). Switches S1 to S10 on switchpack E58 are used to set Q-bus base address bits <12:3>. Jumper W2 is used to set Q-bus base address bit <2>.

The first suggested Q-bus base address for the RQC25 is 17772150. The switches and jumper are configured for this address at the factory. If the system configuration requires another address, the switches and jumper should be set as shown in Figure 46-2.

The RQC25 adapter module is hardwired for a bus interrupt level of BR 4 (BIRQ4).

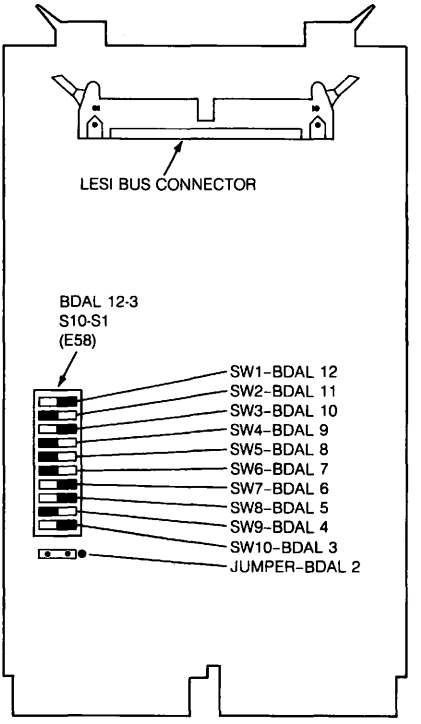
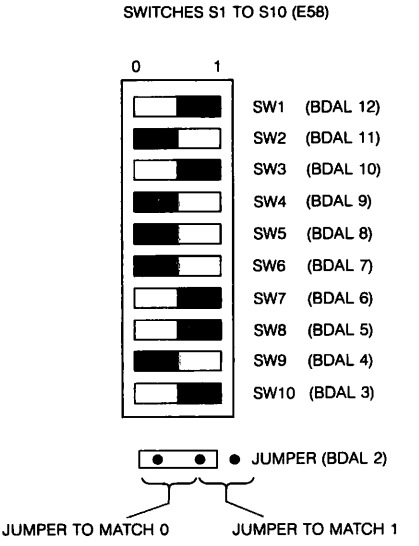


Figure 46-1 ▪ RQC25 Component Layout



NOTE:
SET SWITCH ON (1) TO MATCH ADDRESS BIT = 1
SET SWITCH OFF (0) TO MATCH ADDRESS BIT = 0
EXAMPLE SHOWN IS FOR RECOMMENDED STARTING ADDRESS 17772150_8

Figure 46-2 • RQC25 Address Switch/Jumper Configuration

Chapter 47 ▪ RQDX1 Disk Drive Controller

The RQDX1 option is a disk drive controller that provides interfacing of the RD51 or RD52 Winchester disk drives and/or the RX50 dual 5.25-inch floppy diskette drives to any Q-bus system. A single RQDX1 module can control any one of the configurations listed in Table 47-1.

The RQDX1-E extender module option provides cable connection to a single disk or diskette that is mounted externally from the mounting box.

Table 47-1 ▪ RQDX1 Controller Module Configurations

Configuration	Physical Disk Drives	Logical Disk Drive Numbers
1	One RD51/52 One RX50	Unit 0 = RD51/52 Unit 1, 2 = RX50
2	Two RX50s	Unit 0, 1 = RX50 Unit 2, 3 = RX50
3*	Two RD51/52s One RX50	Unit 0 = RD51/52 Unit 1 = RD51/52 Unit 2, 3 = RX50
4*	Two RD51/52s	Unit 0 = RD51/52 Unit 1 = RD51/52
5	One RX50	Unit 0, 1 = RX50
6	One RD51/52	Unit 0 = RD51/52

* These configurations require the use of the optional RQDX1-E extender module.

▪ Specifications

RQDX1 Disk Controller Module

Identification	M8639
Size	Quad
Power Requirements	+5 Vdc ±5%, 6.4 A (typical), 8.0 A (maximum) +12 Vdc ±5%, 10 mA (typical)
Bus Loads	
ac	2.5
dc	1.0

Drives per Controller	Up to four logical units, no more than two RD51/52 disk drives
Data Transfer Rate	800 ns/word (peak) controller to host; 1.25 Mword/s
Nonstandard Environmental Specifications	
Altitude	
Storage	Up to 9.1 km (30,000 ft)
Operating	Up to 2.4 km (8,000 ft)
RD51/52 Disk Drive	
Storage Type	
Medium	Winchester fixed disk
Recording Surfaces	4 data surfaces
Magnetic Heads	4 read/write heads
Recording Method	Modified frequency modulation
Performance Specifications	
Recording Capacity (formatted)	
Bytes per Sector	512 bytes
Sectors per Track	18 sectors (track size)
Tracks per Group	4 tracks (group size)
Groups per Cylinder	3 groups (cylinder size)
Cylinders per Unit	100 cylinders (+2 reserved)
Total Bytes per Unit	11.059 Mbytes
Transfer Rate	5,000,000 bits/s (625 Kbytes/s)
Access Time (buffered seek, including settling)	85 ms (average) 205 ms (maximum) 8.33 ms (average latency)
Functional Specifications	
Rotational Speed	3,600 r/min (±1%)
Recording Density	9,074 bits/in (maximum)
Track Density	345 tracks/in
Environmental Specifications	
Ambient Temperature	10°C to 50°C (50°F to 122°F)
Relative Humidity	20% to 80%, noncondensing
Maximum Wet Bulb	25.6°C (78°F)

RX50 Diskette Drive	
Storage Type	
Medium	Diskette
Recording Surfaces	Two data surfaces
Magnetic Heads	Two read/write heads
Recording Method	Modified frequency modulation
Performance Specifications	
Recording Capacity (formatted)	
Bytes Per Sector	512 bytes
Sectors Per Track	10 sectors (track size)
Tracks Per Group	5 tracks (group size)
Groups Per Cylinder	16 groups (cylinder size)
Cylinders Per Surface	1 cylinder
Bytes Per Surface	404,480 bytes
Surfaces Per Unit	Two surfaces (Two diskettes)
Bytes Per Unit	808,960
Transfer Rate	250,000 bits/s (31.25 Kbytes/s)
Access Time	
Track to Track	6 ms (minimum)
Head Settling Time	30 ms (maximum)
Head Load Time	30 ms (maximum)
Rotational Latency	100 ms (typical); 200 ms (maximum)
Random Access	264 ms (typical)
Drive Motor Start	250 ms (maximum)
Functional Specifications	
Rotational Speed	300 r/min (±1.5%)
Recording Density	5,576 bits/in (maximum)
Track Density	96 tracks/in
Environmental Specifications	
Ambient Temperature	15°C to 32°C (59°F to 90°F)
Relative Humidity	20% to 80%, noncondensing
Maximum Wet Bulb	25°C (78°F)
RQDX1-E Extender Module Option	
Identification	M7512
Size	Dual
Power Requirements	+5 Vdc, 0.5 A (typical), 0.6 A (maximum)

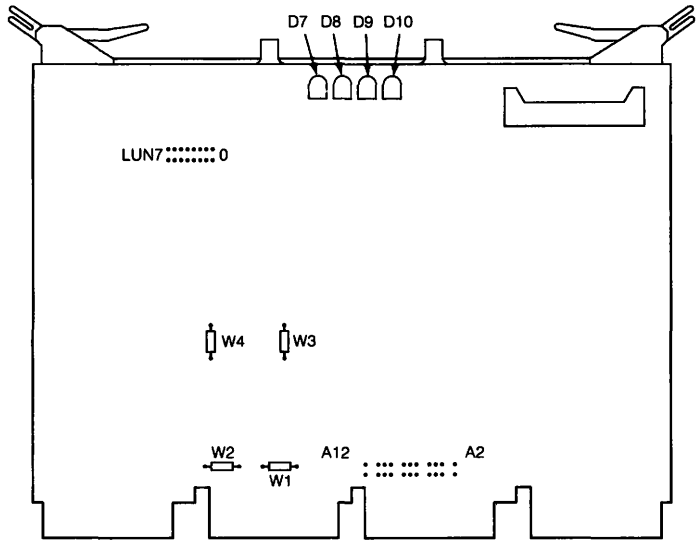
Bus Loads	
ac	0
dc	0
Limitations	Provides signal distribution to a single disk or diskette drive. Cannot be used on the PDP-11/23-PLUS.
Nonstandard Environmental Specifications	
Altitude	
Storage	Up to 9.1 km (30,000 ft)
Operating	Up to 2.4 km (8,000 ft)

▪ Related Documentation

Document Title	Order Number
RQDX1 Controller Module User's Guide	EK-RQDX1-UG
RQDX1 Field Maintenance Print Set	MP-01731-00

▪ Configuration

The RQDX1 controller module must be mounted in the last occupied slot of the backplane due to the DMA and interrupt structure of the Q-bus. The module's device address and logical unit number can be changed by reconfiguring jumpers on the module. Figure 47-1 shows the RQDX1 controller module jumper and diagnostic LED locations.



NOTES:
1. ADDRESS SELECTION (A12 THROUGH A2) AND LOGICAL UNIT NUMBER SELECTION (LUN7 THROUGH LUN0) IS MADE BY ATTACHING TWO POSITION JUMPER CLIPS (PART NO. 12-18783-00). THIS ELIMINATES THE NEED TO WIREWRAP JUMPERS ONTO THE ADDRESS OR LOGICAL UNIT NUMBER STAKES.
2. JUMPERS W1 AND W2 ARE IN FOR Q/Q AND Q22/Q22 MACHINES AND ARE OUT FOR Q/CD AND Q22/CD MACHINES. THEY PROVIDE GRANT CONTINUITY.

Figure 47-1 ▪ RQDX1 Controller Module Jumper and LED Locations

Device Address Selection

The location of the RQDX1 controller module address jumpers is shown in Figure 47-1. The module is factory-configured for a standard module address of 772150. To configure the module for another address, use the format shown in Figure 47-2 to determine the appropriate jumper configuration.

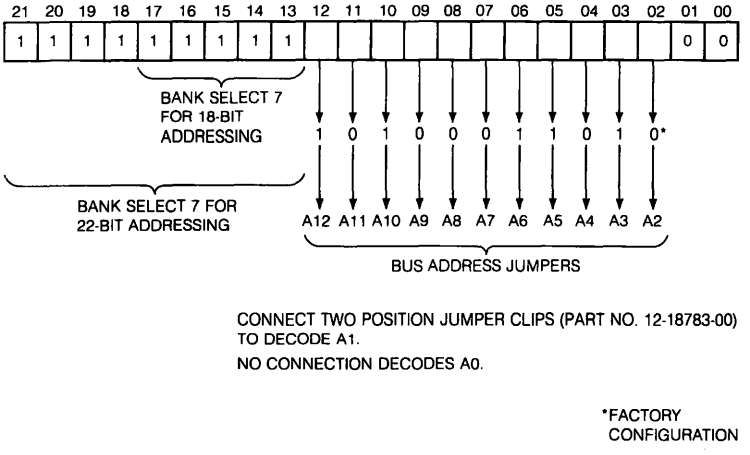


Figure 47-2 ▪ RQDX1 Address Selection Jumper Format

Logical Unit Number Selection

The location of the RQDX1 controller module logical unit number jumpers is shown in Figure 47-1. These jumpers are set to the lowest logical unit number assigned to any disk/diskette drive controlled by the module. The controller module automatically sizes the logical unit configuration during initialization to determine how many (of the four possible units) are actually present. This automatic sizing eliminates the need for reconfiguration of jumpers when units (RD51 or RX50 drives) are added to or removed from the controller module. The standard configuration for the logical unit number jumpers selects logical unit number 0. To configure the module for logical unit numbers beginning with other than unit number 0, use the format shown in Figure 47-3 to determine the appropriate jumper configuration.

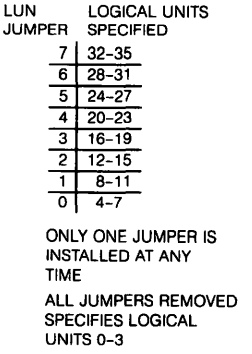


Figure 47-3 ▪ RQDX1 Logical Unit Number Jumper Format

Interrupt Vector

The interrupt vector can be in the range of 0 to 774 and is software-selectable. (A vector selected by software must be greater than 0.) The normal interrupt vector used by the RQDX1 controller module is 154.

The RQDX1 controller module interrupts at priority level 4 determined by E3, a DC003 chip.

▪ RQDX1-E Extender Module Option

Typically, the RQDX1 controller module is located in the same mounting box as the disk and/or diskette drives that it controls. However, if the system mounting box cannot accommodate all of these drives, the optional RQDX1-E extender module can be used to connect the RQDX1 controller module signals to any drive that is external from the system mounting box.

Configuration

As shown in Figure 47-4, the RQDX1-E extender module is a dual-height module that provides signal connectors and requires appropriate jumper configurations. The J2 connector receives signals from the RQDX1 controller module. The other connectors (J1 and J3) distribute these signals to the disk and diskette drives. Jumper functions for the RQDX1-E extender module, as well as the jumpers installed in the factory configuration, are listed in Table 47-2.

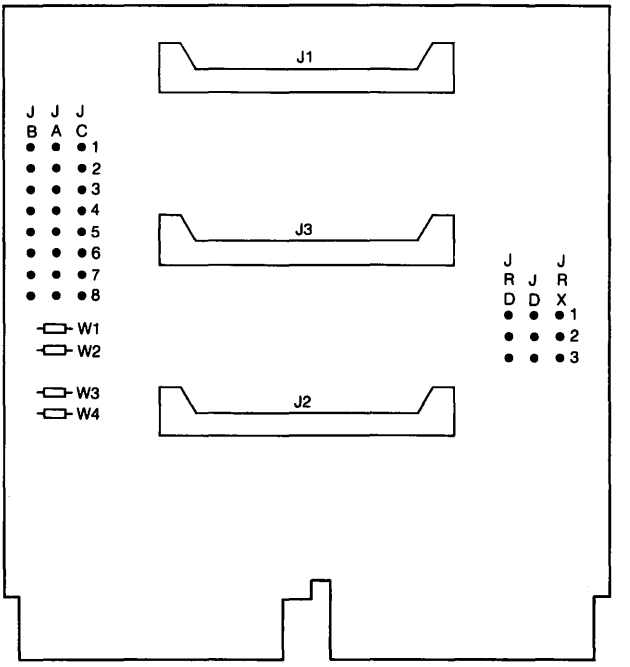


Figure 47-4 ▪ RQDX1-E Extender Module Jumper Locations

Table 47-2 ▪ RQDX1-E Extender Module Jumper Configuration

Jumpers	Functions	Factory Configuration*
W1-W4	Must be installed (manufacturing use only)	W1-W4
JRD1-JRD3 JD1-JD3 JRX1-JRX3	Select the external drive to be connected to the J3 connector	JD1 to JRD1 JD2 to JRD2 JD3 to JRD3
JB1-JB8 JA1-JA8 JC1-JC8	Determine to which connector (J2 or J3) the RD read/write will connect	JA1 to JC1 JA2 to JC2 JA3 to JB3 JA4 to JB4 JA5 to JB5 JA6 to JB6 JA7 to JC7 JA8 to JC8

* Factory configuration is set to connect an external RD51 disk drive to connector J3. To configure the module for an external RX50 (connected to J3), jumpers JD1 through JD3 are connected to JRX1 through JRX3, jumpers JA1 through JA8 are connected to JB1 through JB8.

▪ Cables and Cabinet Kits

The RQDX1 module is typically installed in the last occupied slot of the backplane. If empty slots are left between the other modules and the RQDX1 module, install grant cards (part number G7272) in those empty slots to accommodate the interrupt and direct memory access structure of the backplane.

Install the 50-conductor signal cable (part number BC02D-1D) to the J1 connector on the RQDX1 module. This cable must be connected to a signal distribution panel that will connect the appropriate signals to the RD51 and/or RX50 drives. The RD51 disk drive requires two signal cable connections. One is a 20-conductor cable (part number 17-00282-00), the other is a 34-conductor cable (part number 17-00286-00). The RX50 diskette drive requires a single 34-conductor signal cable (part number 17-00285-02).

The RQDX1-E dual-height module is installed in the backplane slot directly below the RQDX1 module, in connectors A and B. A cable (part number BC02D-0K) connects the RQDX1 controller module to the RQDX1-E extender module through the J2 connector. Another cable (part number 70-18652-01) attached to the J3 connector connects the RQDX1-E extender module to a mounting plate (part number 74-2866-01) that is mounted to the system's patch and filter panel assembly. (The entire cable and mounting plate assembly can be ordered as part number 70-20691-01.) This external plate provides the signals to be sent to the external drive. A third cable (part number BC02D-1D), attached to the J1 connector on the RQDX1-E extender module, is connected to the signal distribution panel in the mounting box, providing signals to the disk or diskette drives that are installed in the system mounting box.

When ordered as a system upgrade, the RQDX1 option does not include any internal cables or connection panel inserts. One of the following cabinet kits should be chosen for system installation:

CK-RQDX1-KA	For use with the BA23 enclosure
CK-RQDX1-KC	For use with the H349 distribution panel
CK-RQDXE-KA	For the RQDX1-E extender module for use in the BA23 enclosure only

Chapter 48 ▪ RXV21 Floppy Disk Option

The RXV21 floppy disk option is a random-access, mass storage device that stores data in fixed-length blocks on a preformatted, flexible diskette.

The RXV21 floppy disk system is available in the configurations described in Table 48-1.

Table 48-1 ▪ RXV21 Configurations

System	Disk Drive	Line Voltage*
RXV21-AA	Single drive system	115 V/60 Hz
RXV21-AC	Single drive system	115 V/50 Hz
RXV21-AD	Single drive system	230 V/50 Hz
RXV21-BA	Dual drive system	115 V/60 Hz
RXV21-BC	Dual drive system	115 V/50 Hz
RXV21-BD	Dual drive system	230 V/50 Hz

* 50 Hz versions are available in voltages of 105, 115, 220, and 240 Vac by field-pluggable conversion.

▪ Specifications

Interface Module	
Identification	M8029
Size	Dual
Power Requirements	+5 V ±5% at 1.8 A (typical)
Bus Loads	
ac	3.0
dc	1.0
Disk Drive	
Identification	RX02
Dimensions	46.3 cm w × 28.7 cm h × 53.3 cm d (19 in w × 10.5 in h × 21 in d)
Recommended Service	55 cm (22 in) clearance (front and rear)
ac Power	4 A at 115 Vac; 2 A at 230 Vac (dual drive)

Cable Included	BC05L-15 (15 ft)
Drive Performance	
Capacity (8-bit bytes)	
Per diskette	512,512 bytes
Per track	6,656 bytes
Per sector	256 bytes
Data Transfer	
Diskette to controller buffer	2 μs/data bit (500 Kbits/s)
Buffer to RXV21 interface	1.2 μs/bit (500 Kbits/s)
RXV21 interface to Q-bus	23 μs/16-bit word
Track-to-track move	6 ms/track maximum
Head settle time	25 ms maximum
Rotational speed	360 rpm ±2.5%; 166 ms/rev nominal
Recording surfaces	1 per disk
Tracks per disk	77 (0-76) or ($0\text{-}114_8$)
Sectors per track	26 (1-26) or ($0\text{-}32_8$)
Sectors per disk	2002
Recording technique	Double frequency (FM) or modified (MFM)
Bit density	3,200 bpi (FM); 6,400 bpi (modified MFM)
Track density	48 tracks/in
Average access	262 ms, computed as follows:

Seek	**Settle**	**Rotate**	**Total**
(77 tks/3) × 6ms +	25 ms +	(166ms/2) =	262 ms

Environmental Characteristics	
Temperature	
RX02, operating	15° to 32°C (59° to 90°F) ambient; maximum temperature gradient = 11°C/hr (20°F/hr)
RX02, nonoperating	−35° to +60°C (−30° to +140°F)
Media, nonoperating	−35° to +52°C (−30° to +125°F)

Note

Media temperature must be within operating temperature range before use.

Relative Humidity	
RX02, operating	25°C (77°F) maximum wet bulb 2°C (36°F) minimum dew point 20 to 80% relative humidity
RX02, nonoperating	5 to 98% relative humidity (no condensation)
Media, nonoperating	10 to 80% relative humidity
Magnetic field	Media exposed to a magnetic field strength of 50 oersteds or greater may lose data.
System Reliability	
Minimum revolutions/track	3 million/media (head-loaded)
Seek error rate	1 in 10^6 seeks
Soft read error rate	1 in 10^9 bits read
Hard read error rate	1 in 10^{12} bits read

Note

The error rates above apply only to Digital- approved media that are properly cared for. Seek error and soft read errors are usually attributable to random effects in the head/media interface, such as electrical noise, dirt, or dust. Both are called "soft" errors in that the error is recoverable in ten additional tries or fewer. "Hard" errors cannot be recovered. Seek error retries should be preceded by an initialize.

▪ Related Documentation

Document Title	Order Number
RXV21 Field Maintenance Print Set	MP-00628-00
RX02 Floppy Disk System User's Guide	EK-RX02-UG
RX02 Floppy Disk System Technical Manual	EK-ORX02-TM
RX01/RX02 Pocket Service Guide	EK-RX012-PS
RX01/RX02 Reference Card	EK-RX102-RC
RX02 Field Maintenance Print Set	MP-00629-00
RX02 Illustrated Parts Breakdown	EK-ORK02-IP

▪ Configuration

The factory jumper locations on the RXV21 interface module are shown in Figure 48-1. All RXV21 interface modules are configured and shipped with preselected register addresses and vectors as described in Table 48-2. The control and status register (RX2CS) address is set to 177170, the data buffer register (RX2DB) address is set to 177172, and the interrupt vector address is set to 264. As supplied, the factory-configured addresses are those used with Digital software. However, in applications where more than one RXV21 system is required, appropriate register addresses and vectors can be configured by installing or removing jumpers. A second RXV21 system would normally be assigned register addresses 177200 (RX2CS) and 177202 (RX2DB), with an interrupt vector of 270 (Table 48-3).

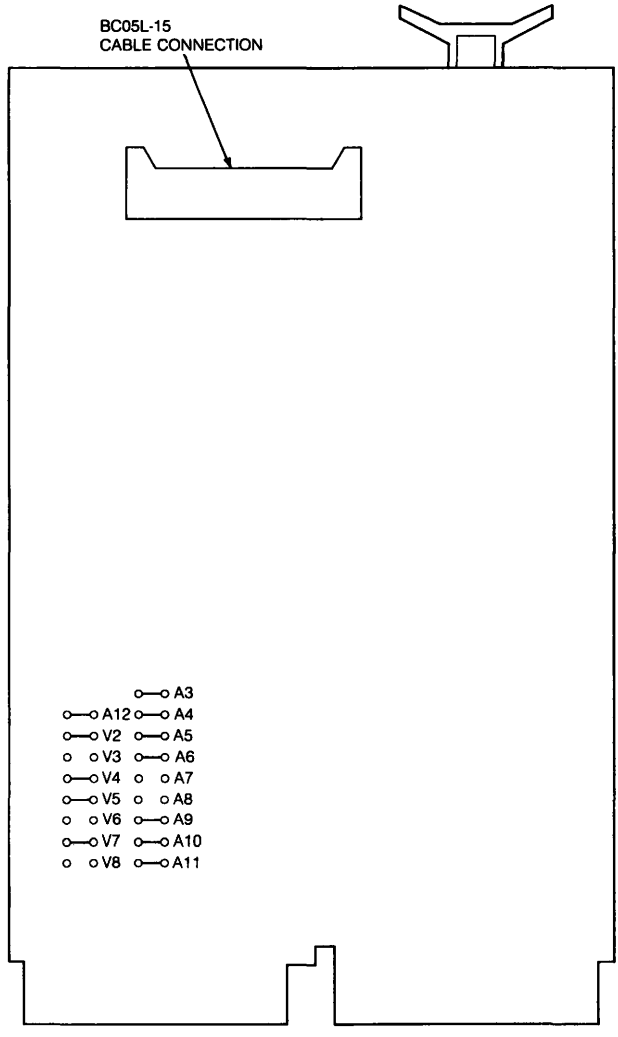


Figure 48-1 ▪ RXV21 Device and Vector Address Jumpers

Table 48-2 ▪ RXV21 Factory Jumper Configuration

Standard Device Register Address	Jumper Connections A12	A11	A10	A9	A8	A7	A6	A5	A4	A3
177170/ 177172	I	I	I	I	R	R	I	I	I	I

Standard Vector Address	Jumper Connections V8	V7	V6	V5	V4	V3	V2
264	R	I	R	I	I	R	I

I = jumper installed; R = jumper removed

Table 48-3 ▪ RXV21 Standard Address Assignments

Description	Mnemonic	1st Module Address	2nd Module Address
Registers:			
Control and Status	RX2CS (R/W)	177170	177150
Data Buffer	RX2DB (R/W)	177172	177152
Interrupt Vector	–	264	270

▪ Cables and Cabinet Kits

The following external cable is recommended for use with the RXV21 interface module:

BC05L-15	15 ft, 40-conductor flat cable with H855 connectors on both ends

When the RXV21 is ordered as an upgrade option, one of the following cabinet kits should be chosen for system installation:

CK-RXV2E-KA	For use with the BA23 enclosure
CK-RXV2E-KB	For use with the BA11-M enclosure
CK-RXV2E-KC	For use with the H349 distribution panel

Chapter 49 ▪ TQK25 Tape Drive Adapter Module

The TQK25 is a tape drive controller that provides interfacing of an external TK25 tabletop streaming tape drive to any Q-bus system.

▪ Specifications

TQK25 Controller Module

Identification	M7605
Size	Quad
Power Requirements	+5 Vdc at 3.5 A (typical), 4.0 A (maximum)
Bus Loads	
ac	2.0
dc	1.0
Nonstandard Environmental Specifications	
Operating Temperature	10°C to 60°C (50°F to 140°F)
TK25 Tape Drive	
Mode of operation	Streaming
Media	600-ft long, ¼-inch wide unformatted magnetic tape; cartridge similar to ANSI Standard X3.55-1982
Start/stop distance	Minimum: 30.5 mm (1.2 in) Nominal: 35.5 mm (1.4 in) Maximum: 48.3 mm (1.9 in)
Recording Specifications	
Recording density	8,000 bits/in
Number of tracks	11
Data rate	440 kbits/s
Tape Speed	55 inches/s
Recording format	Single track of serial NRZI data in a serpentine pattern. A 4-to-5 run length limited code similar to GCR is used.
Access Time	
From cartridge insertion	Maximum: 4 min, 30 sec Minimum: 1 min, 40 sec
From rest w/cartridge inserted	Nominal: 61 ms

Error rate	
Recoverable write data error	1 in 1 × 10^7 bits
Recoverable read data error	1 in 1 × 10^8 bits
Unrecoverable read data error	1 in 1 × 10^{10} bits
Capacity	
8 K blocks	61 Mbytes
4 K blocks	56 Mbytes
2 K blocks	48 Mbytes
1 K blocks	37 Mbytes
Input voltages	Universal 60 Hz/50 Hz power supply with switch-selectable voltage ranges of 120 V/220 V
Environmental Requirements	
Nonoperating (storage)	
Temperature	−10°C to 50°C (14°F to 122°F)
Relative humidity	10 to 90%, noncondensing
Temperature change	15°C (27°F) per hour maximum
Altitude	−300 to 3,655 m (−983 to 12,000 ft)
Nonoperating (transit)	
Temperature	−40°C to 60°C (140°F to 140°F)
Relative humidity	5 to 95% noncondensing
Temperature change	20°C (36°F) per hour maximum
Altitude	−300 to 9,144 m (−983 to 30,000 ft)
Operating	
Temperature	16°C to 32°C (60°F to 90°F)
Relative humidity	20% to 80% noncondensing
Dew point	−4°C to 26°C (20°F to 79°F)
Temperature change	10°C (18°F) per hour maximum
Relative humidity change	10% per hour
Altitude	−300 to 3,655 m (−983 to 12,000 ft)
Heat dissipation	
Typical during idle	45 Watts
Maximum during tape motion	55 Watts
Maximum (worst case)	75 Watts

▪ Related Documentation

Document Title	Order Number
TQK25 Q-Bus CPU Kit Installation Guide	EK-T25QA-IN
TK25 Tape Drive Subsystem User Guide	EK-0TK25-UG
TK25 Tape Drive Customer Installation Guide	EK-T25TD-IN
TK25 Tape Drive Subsystem Pocket Service Guide	EK-0TK25-PS

▪ Configuration

The TQK25 adapter module contains two DIP switchpacks and four jumpers that are used to configure the module. The locations of these jumpers and switchpacks are shown in Figure 49-1. The following features are user-selectable:

- Device base address
- Interrupt vector address
- Block mode DMA
- System size (18- or 22-bit)
- Interrupt priority level

The TQK25 adapter module can be installed in any nondedicated Q-bus slot.

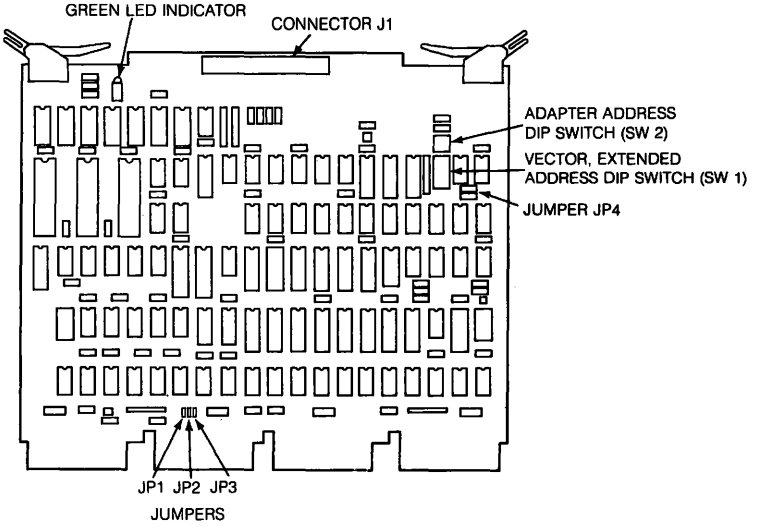


Figure 49-1 ▪ TQK25 Switch and Jumper Locations

Device Address

The TQK25 adapter module contains eight device registers for use in program-control of the TK25 tape drive. These registers are as follows:

TSBA–Address Register
TSDB–Data Buffer Register
TSSR–Status Register
XST–Extended Status Registers (5 of them)

The TQK25 base address is that address assigned to TSBA/TSDB. (Note that these two registers share a single address. This does not present a conflict because TSBA is a read-only register and TSDB is a write-only register.)

The TQK25 factory-configured base address is 17772520. If the system configuration requires another address, the DIP switches in switchpack 2 (SW2) must be configured for the new address, as shown in Table 49-1. These switch settings select the TSDB/TSBA address; TSSR is automatically assigned the next consecutive address.

Note

Although the hardware can be configured for addresses above 17772720, these addresses are not normally used.

Table 49-1 ▪ TQK25 Address Switch Settings

	SW2 Settings*			
Base Address	**S1**	**S2**	**S3**	**S4**
17772520	ON	ON	ON	ON
17772524	ON	ON	ON	OFF
17772530	ON	ON	OFF	ON
17772534	ON	ON	OFF	OFF
17772720	ON	OFF	ON	ON
17772724	ON	OFF	ON	OFF
17772730	ON	OFF	OFF	ON
17772734	ON	OFF	OFF	OFF
17777360	OFF	ON	ON	ON
17777364	OFF	ON	ON	OFF
17777370	OFF	ON	OFF	ON
17777374	OFF	ON	OFF	OFF

(continued on next page)

Table 49-1 ▪ TQK25 Address Switch Settings (Cont.)

	SW2 Settings*			
Base Address	**S1**	**S2**	**S3**	**S4**
17777420	OFF	OFF	ON	ON
17777424	OFF	OFF	ON	OFF
17777530	OFF	OFF	OFF	ON
17777534	OFF	OFF	OFF	OFF

ON = 0; OFF = 1

* SW2 is used to select addresses via the address decode logic. This switch bank does not directly correlate to address lines or address bits.

Interrupt Vector Address

The TQK25 adapter module is factory-configured with an interrupt vector address of 224. If the system configuration requires another address, switches S1 through S7 in switchpack 1 (SW1) must be configured for the new address. A switch set to the ON position encodes a logical 0 in the corresponding vector address bit; a switch set to the OFF position encodes a logical 1. Table 49-2 lists the switch-to-bit relationship for the vector address selection switches.

Table 49-2 ▪ Interrupt Vector Address Switch Settings

Switch Number	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	**S7**
Address Bit	8	7	6	5	4	3	2

Block Mode DMA

The TQK25 is factory-configured to permit block mode direct memory access (DMA). To disable this function, remove jumper JP4.

Q-Bus Addressing Mode

Switch S8 of switchpack SW1 can be used to select either 18- (ON) or 22-bit (OFF) addressing. It is factory-configured to select 22-bit addressing.

Interrupt Priority Level

The TQK25 is factory-configured for an interrupt priority level of BR4. If the system configuration requires another level, jumpers JP1, JP2, and JP3 must be configured for the new level, as shown in Table 49-3.

Table 49-3 ▪ Interrupt Priority Level Selection

Interrupt Priority Level	Jumper Configuration JP1	JP2	JP3
Level 4	Removed	Removed	Removed
Level 5	Installed	Removed	Removed
Level 6	Removed	Installed	Removed
Level 7	Removed	Installed	Installed

▪ Cables and Cabinet Kits

There are two versions of the TQK25, as noted below. The two versions are identical with the exception of the length of the ribbon cable.

TQK25-EA — Includes drive, controller card, external cable, universal power supply, and cabinet kit. Cabinet kit includes a 16-in (0.41-m) BC18S interface CPU cable. For use with Micro/PDP-11 or PDP-11/23-S.

TQK25-EC — Includes drive, controller card, external cable, universal power supply, and cabinet kit. Cabinet kit includes a 32-in (0.82-m) BC18S interface CPU cable. For use with PDP-11/23-PLUS.

Chapter 50 ▪ TSV05 Tape Transport Subsystem

The TSV05 tape transport subsystem provides magnetic tape storage capabilities to computer systems using quad-sized Q-bus backplanes.

▪ Specifications

Interface/Controller Module

Identification	M7196
Size	Quad
Power Requirements	5 Vdc ±5% at 6.5 A
Bus Loads	
ac	3.0
dc	1.0

Tape Transport

Cabinet Dimensions	
Height	111.13 cm (43.75 in)
Width	59.69 cm (23.50 in)
Depth	83.82 cm (33.00 in)
Weight	121 kg (265 lb)
Power Consumption	220 W average 270 W maximum

Voltage (+7% or -15%)

	Nominal Vdc	Low limit Vdc	High limit Vdc
TSV05-BA	120	102	128
TSV05-BB	204	204	256
TSV05-BD	220	187	235

Frequency (± 1 Hz)

Nominal Hz	Low limit Hz	High limit Hz
50 or 60	49	61

Frequency rate of change: 1.5 Hz/sec maximum

Operating Conditions	
Temperature	15°C to 32°C (59°F to 86°F)
Temperature Shock	20°C change/hour maximum
Relative Humidity	20% to 80% noncondensing
Altitude	Sea level to 3 km (10,000 ft)

Pollutants	
Atmospheric Particulates	60 mg/1000 ft^3 air by weight of particle (5 micra diameter)
Electrostatic Discharge	10 kV through 100 Ω from 350 pF
Nonoperating Conditions	
Temperature	−40°C to 66°C (−40°F to 149°F)
Relative Humidity	95% maximum, noncondensing
Altitude	Sea level to 15 km (49,000 ft)
Vibration	
Frequency Range	10 to 300 Hz
Peak Acceleration	1.4 g rms vertical axis; 0.68 g rms longitudinal and lateral axis; 200 Hz maximum
Shock	
Peak Acceleration	20 g
Duration	30 ± 10 ms
Waveshape	½ sine
Emissions	
Heat	1,100 Btu/hour maximum
Acoustic Noise	
Standby (blower on)	57 dB A scale
Operating conditions	60 dB A scale
Electromagnetic Interference	Complies with FCC Part 15, Subpart J, Class A Designed to comply with VDE 0871 B requirements

Note

The TSV05 subsystem has been designed and tested to meet Digital standards, including FCC requirements. Digital cannot guarantee the TSV05 subsystem will meet these specifications if nontested equipment is installed into the TSV05 cabinet or the TSV05 cabinet is installed in nontested configurations.

▪ Related Documentation

Document Title	Order Number
TSV05 Tape Transport Pocket Service Guide	EK-TSV05-PS
Operation and Maintenance Instructions for Model F880 Tape Transport	799816-000*
TSV05 Tape Transport Subsystem User's Guide	EK-TSV05-UG
TSV05 Tape Transport Subsystem User's Guide Addendum	EK-TSV05-U1
TSV05 Tape Transport Subsystem Installation Guide	EK-TSV05-IN
TSV05 Tape Transport Subsystem Installation Guide Addendum	EK-TSV05-I1
TS05 Tape Transport Operation and Acceptance Preventive Maintenance Remove/Replace	EY-D3142-PS
TSV05 Field Maintenance Print Set	MP-01157-00
TSV05 Subsystem Technical Manual	EK-TSV05-TM

* Available from Cipher Data Products, 10225 Willow Creek Road, San Diego, California 92131. This document contains detailed drawings of the TS05 formatter and power supply.

▪ Configuration

The TSV05 interface/controller module plugs into a quad slot in the Q-bus backplane. It connects to the Q-bus on the A and B sets of edge connectors (module fingers).

The module has six wirewrap jumpers (W1 through W6) and two switchpacks used for configuration. Figure 50-1 shows the locations of these jumpers and switchpacks.

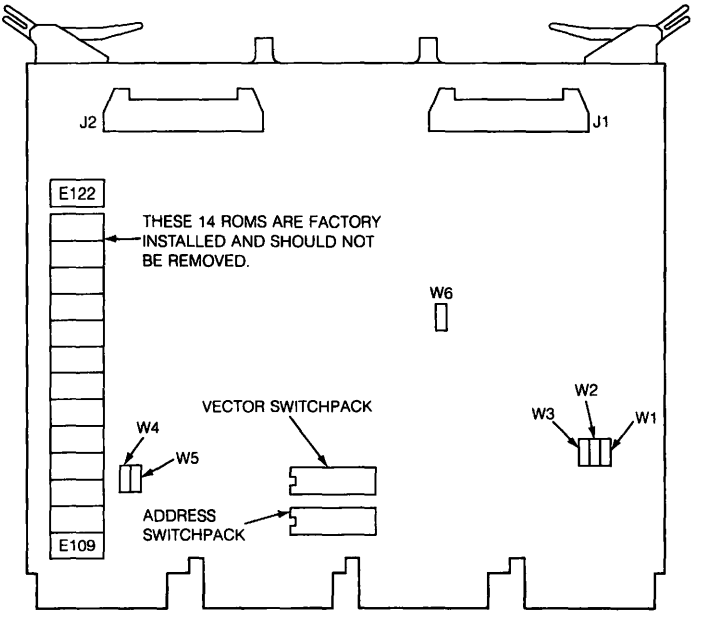


Figure 50-1 ▪ TSV05 Interface Module Switch and Jumper Locations

Device and Vector Address Selection

The TSV05 is factory-configured with a device address of 772520 and a vector address of 224. If necessary, the module can be reconfigured for other addresses. This is done using switchpacks E57 and E58, as shown in Figure 50-2.

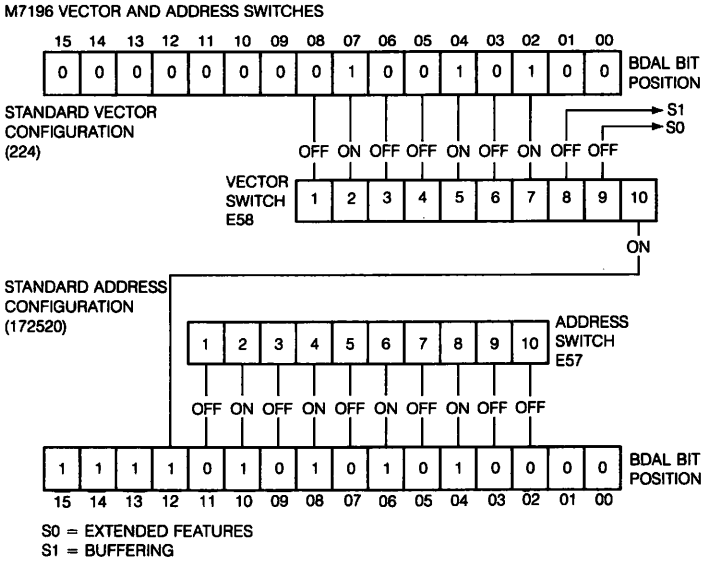


Figure 50-2 ▪ TSV05 Vector and Device Address Selection

Selecting Extended Features

The TSV05 contains four hardware device registers on the M7196 controller module. In addition, if the "extended features" option is selected, five additional "remote" device registers are available. These remote registers are maintained by the controller in a buffer area of the CPU memory.

The extended features option is enabled by setting (to the ON position) switch 9 of the E58 switchpack (see Figures 50-1 and 50-2). The option is disabled by resetting the switch (to the OFF position).

Selecting Record Buffering

The TSV05 supports a record buffering mode of operation designed to optimize system performance when performing read and write operations on a "streaming" tape transport. The technique involves buffering tape records in the controller to avoid many of the long repositioning delays frequently encountered when dealing with a streaming tape transport.

Record buffering can be enabled by either software or hardware. If the extended features option is selected, buffering can be enabled or disabled through program control of the device characteristics register. If the extended features option is not selected, buffering can be enabled or disabled only by the hardware. This is done by setting (to the ON position) or resetting (to the OFF position) switch 8 of the E58 switchpack (see Figures 50-1 and 50-2).

Selecting Interrupt Priority

The TSV05 is factory-configured for an interrupt priority level of BIRQ4. If the system configuration requires another priority level, jumpers W1 through W3 must be configured for the new level, as shown below.

Priority Level	Jumper Connections W1	W2	W3
BIRQ4*	R	R	R
BIRQ5	I	R	R
BIRQ6	R	I	R
BIRQ7	R	R	R

* Factory configuration

Bus Grant Continuity Jumpers

If the TSV05 is installed in a Q/Q-type backplane (such as the H9275 or the H9270), jumpers W4 and W5 should be installed to provide continuity to the BIAK and BDMG bus grant signals. If the module is installed in a Q/CD-type backplane (such as the H9276 or H9273) where bus grant signals pass through each module via the AB connectors of each slot, W4 and W5 should be removed. (See Chapter 52 for a discussion of Q/Q and Q/CD backplanes.)

SCLOCK Enable Jumper

Jumper W6 is used to enable the SCLOCK. It is for manufacturing test purposes only and should not be removed.

▪ Cables and Cabinet Kits

The TSV05 tape transport system is designed to be rackmounted in a H9642-series cabinet, with 874 power controller and remote power control cable. A pair of 7016855 bus cables is also required for connecting the tape transport input and output to the interface module.

Chapter 51 • TU58 Cartridge Tape Drive

The TU58 is a low-cost intelligent mass memory device that offers random-access to block-formatted data on pocket-size cartridge media.

• Specifications

Performance	
Capacity per cartridge	262,144 bytes, formatted in 512 blocks of 512 bytes each
Data reliability	
Soft data error rate	1 in 10^7 bits read (before self-correction)
Hard data error rate	1 in 10^8 bits read (unrecoverable within eight automatic retries)
Hard error rate with write verify and system correction	2 in 10^{11} bits read/written
Error checking	Checksum with rotation
Average access time	9.3 s
Maximum access time	28 s
Read/write tape speed	76 cm/s (30 ips)
Search tape speed	152 cm/s (60 ips)
Bit density	315 bits/cm (800 bits/in)
Flux reversal density	945 fr/cm (2,400 fr/in)
Recording method	Ratio encoding
Medium	DECtape II cartridge with 42.7 m (140 ft) of 3.81 mm (0.150 in) tape Size: 6.1 × 8.1 × 1.3 cm (2.4 × 3.2 × 0.5 in)
Track format	Two tracks, each containing 1024 individually numbered, firmware-interleaved "records." Firmware manipulates four records at each operation to form 512-byte blocks.
Drive	Single motor, head integrally cast into molded chassis.

Drives per controller	One or two. Only one may operate at a time.
Electrical	
Power Consumption	
Module and one or two drives	11 W, typical, drive running +5 V ±5% at 0.75 A, maximum +12 V +10% -5% at 1.2 A, peak 0.6 A average running 0.1 A idle
Serial interface standards	In accordance with RS-422 or RS-423; compatible with RS-232C.
Mechanical	
Drive	8.1 H × 8.3 D × 10.6 W cm (3.2 × 3.3 × 4.1 in) with 19 cm (7.5 in) cable 0.23 kg (0.516 lb)
Board (Module)	13.2 H × 26.5 D × 3.5 W cm (5.19 × 10.44 × 1.4 in) 0.24 kg (0.5316 lb)
Environmental	
Maximum dissipation, TU58-AB, -BB	34 Btu/hour
Temperature	
TU58-AB, BB operating	15°C to 4°C (59°F to 108°F)
TU58-AB, BB nonoperating	−34°C to 60°C (−30°F to 140°F)
Medium operating temperature	0°C to 50°C (32°F to 122°F)
Maximum temperature difference between system ambient and TU58 module	18°C (32.4°F)
Relative Humidity, noncondensing	
TU58 operating	
Maximum wet bulb	26°C (79°F)
Minimum dew point	2°C (36°F)
Relative humidity	20 to 98%
TU58 nonoperating	5 to 98%
Medium nonoperating	10 to 80%

Related Documentation

Document Title	Order Number
TU58 DECtape II User Guide	EK-0TU58-UG
TU58 DECtape II Pocket Service Guide	EK-0TU58-PS
TU58 DECtape II Technical Manual	EK-0TU58-TM
TU58 DECtape II Illustrated Parts Breakdown	EK-0TU58-IP
TU58-CA Field Maintenance Print Set	MP00747
TU58-EA Field Maintenance Print Set	MP01014-00
TU58-VA Field Maintenance Print Set	MP01013-00
TU58-DB Field Maintenance Print Set	MP01063
TU58 Diagnostic Documentation Kit	ZJ287-RZ

Configuration

The TU58 is shipped with factory-installed jumpers for a transmission rate of 38.4 kilobaud, and the RS-423 unbalanced line interface. A variety of standards and rates may be selected by changing the jumpers on the controller module. Table 51-1 provides a list of the wirewrap (WW) pins and their functions. Figure 51-1 shows the physical layout of the TU58 controller module.

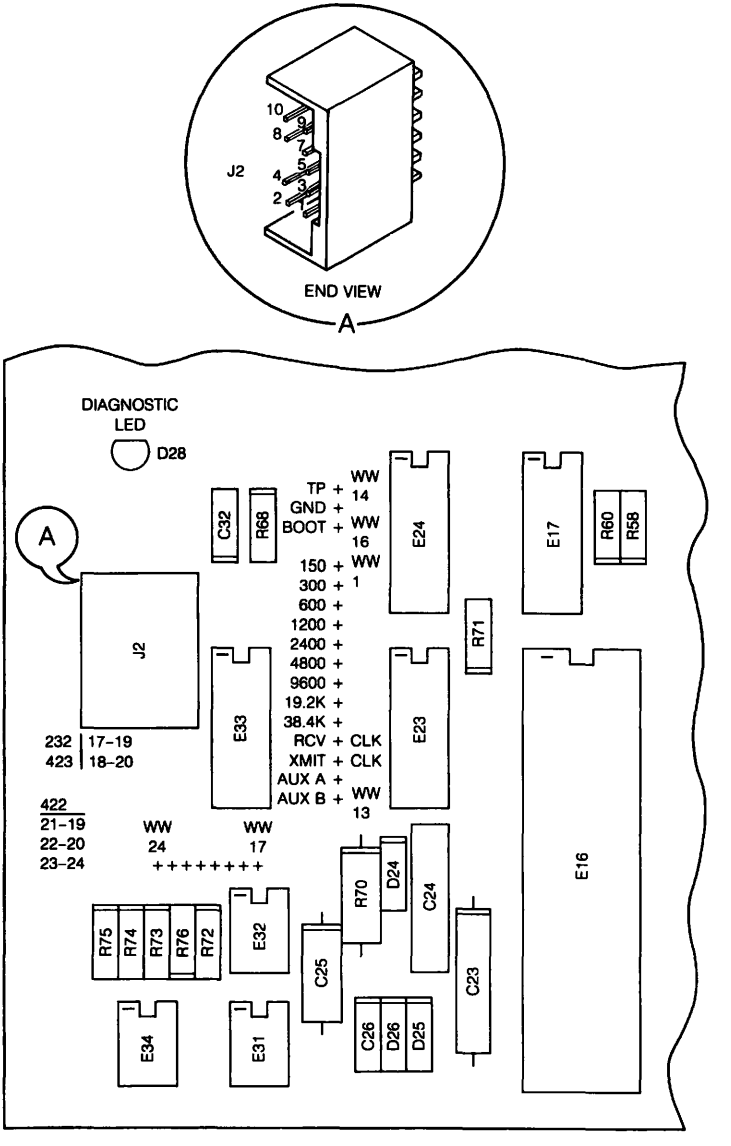
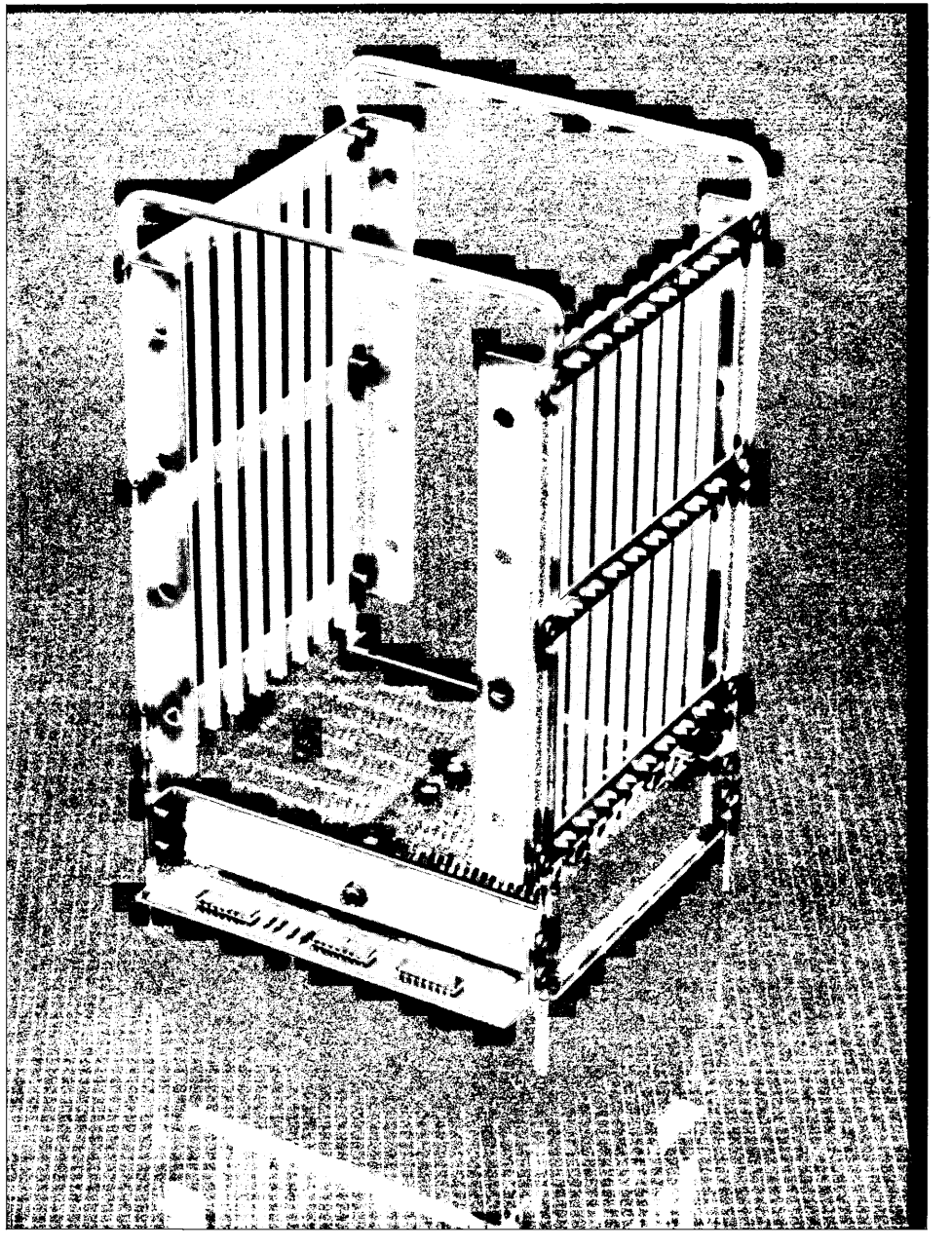


Figure 51-1 ▪ TU58 Controller Board

Table 51-1 ▪ TU58 Module Jumper Connections

Wirewrap Pin	Function
WW1	150 baud
WW2	300 baud
WW3	600 baud
WW4	1200 baud
WW5	2400 baud
WW6	4800 baud
WW7	9600 baud
WW8	19200 baud
WW9	38400 baud
WW10	UART Receive Clock
WW11	UART Transmit Clock
WW12	Auxiliary A (to interface connector pin L)
WW13	Auxiliary B (to interface connector pin A)
WW14	Factory Test Point
WW15 WW16	Ground Boot } Connect together for autoboot on powerup
WW17	RS-423 Driver
WW18	RS-423 Common (Ground)
WW19	Transit Line +
WW20	Transmit Line −
WW21	RS-422 Driver +
WW22	RS-422 Driver −
WW23 WW24	} Receiver Series Resistor (Jump for RS-422)

Part X • Backplanes, Enclosures, and Expansion Cables



Chapter 52 • Introduction to Backplanes, Enclosures, and Expansion Cables

• Backplanes

A backplane is a hardware interface containing edge connector slots for the insertion of modules. Backplanes, therefore, permit the connection of modules to the Q-bus and to a power supply.

Backplanes have either quad slots or dual slots. Those with dual-slots accept only dual-height modules. Those with quad slots accept one quad-height or one dual-height module per slot and may accept two dual-height modules per slot.

Quad-slot backplanes fall into two groups:

- Q/CD backplanes, which have Q-bus signals on the A and B connectors and user-defined signals on the C and D connectors.
- Q/Q backplanes, which have Q-bus signals on the C and D connectors as well as on the A and B connectors.

In Q/CD backplanes, bus grant signals pass through each installed module via the A and B connectors of each slot. These backplanes will accept one quad-height or one dual-height module per slot.

Q/Q backplanes, on the other hand, are designed so that two dual-height modules can be installed in one quad-height slot, with the Q-bus lines routed in a serpentine pattern as follows:

AB, first slot
CD, first slot
CD, second slot
AB, second slot
and so on

Each dual-height module extends the continuity of the bus grant signals (BIAK and BDMG) to the next module. If a quad-height module is installed, however, jumpers on the module must perform the grant continuity function of a dual-height module installed on connectors C and D. In addition, if the installation of a dual-height module leaves an empty slot on the C and D connectors, module G7272 must be installed in the empty slot to perform the continuity function.

Note

The DDV11-B backplane is unique in that it is a hex-slot backplane, with Q-bus signals on the A, B, C, and D connectors and user-defined signals on the E and F connectors.

Table 52-1 lists the available Q-bus backplanes.

Table 52-1 ▪ Q-bus Backplane

Feature	DDV11-B	H9270-Q	H9273-A	H9275-A	H9281-Q
Addressing	18-bit	18- or 22-bit*	18-bit	22-bit	18- or 22-bit*
Number of slots	9	4	9	9	-QA 4 -QB 8 -QC 12
Type	hex†	quad Q/Q	quad Q/CD	quad Q/Q	dual
AC bus loads	6.4	4.4	2.6	10.0	-QA 1.1 -QB 1.8 -QC 2.9
Termination	none	none	none	120 ohms	-QA none -QB 120 ohms -QC 120 ohms

* Jumper-selectable

† See text.

▪ Enclosures

Backplanes can be purchased either as stand-alone units or already mounted in an enclosure. An enclosure provides power and cooling for the backplane and the modules. Enclosures also have I/O connection panels located at the back to facilitate the connection of cables to communications and peripheral devices.

Table 52-2 lists the available Q-bus backplane enclosures.

Table 52-2 ▪ Q-bus Enclosure

Feature	BA11-M	BA11-N	BA11-S	BA23-A
Backplane	H9270-A	H9273-A	H9276*	H9278-A*
Addressing	18-bit	18-bit	22-bit	22-bit
Number of slots	4	9	9	8
Type	quad Q/Q	quad Q/CD	quad Q/CD	quad †
AC bus loads	4.4	2.6	3	
Power supply	H780	H786	H7861	H7864
Line voltage	115V/230V	115V/230V	120V/240V	120V/240V
Bus signals transmitted	BEVNT BPOK BDCOK BHALT	BEVNT BPOK BDCOK	BPOK BDCOK	BEVNT BPOK BDCOK
AC input panel	none	H403-A	H403-B	none

* The H9276 and H9278-A are not available as separate backplanes.

† The H9278-A backplane has Q/CD signals on slots 1 through 3 and Q/Q signals on slots 4 through 8.

▪ Bus Termination

The Q-bus is a 120-ohm transmission line and, therefore, must be terminated at each end by an appropriate terminator, as shown in Figure 52-1. This is done as a voltage divider with its Thevenin equivalent equal to 120 ohms and 3.4 V nominal. This type of termination is provided by the BDV11-AA and TEV11 modules or by certain backplanes and expansion cable connector cards.

Note that the resistive termination can be provided by the combination of two modules (e.g., the processor module supplying 220 ohms to ground, in parallel with another card supplying 250 ohms, providing a total of 120 ohms). Both of these terminators must be physically resident within the same backplane.

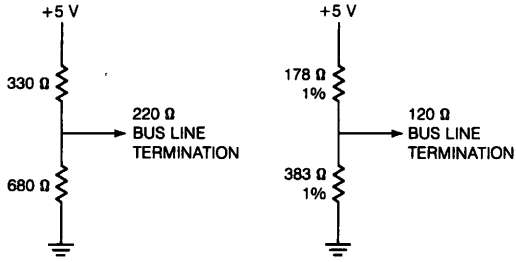


Figure 52-1 ▪ Bus Line Terminations

▪ Expansion Cables

Q-bus systems can be divided into two types: those that use only one backplane and those that have multiple (up to three) backplanes. The characteristics of the two types differ enough to require separate sets of configuration rules. These rules are discussed in detail in Appendix B.

Multiple backplane systems require the use of expansion cable assemblies. The assembly used is determined by the termination requirements of the two backplanes being connected. Table 52-3 lists the expansion assemblies and their subcomponents.

As mentioned above, both ends of the bus must be terminated with 120 ohms. This means that the first and last backplane must have an impedance of 120 ohms. To achieve this, each backplane can be lumped together as a single point on the bus. Also, the resistive termination can be provided by a combination of two modules in the backplane.

In the first backplane, a processor providing 220 ohms to ground, in parallel with an expansion cable connector card providing 250 ohms, gives the needed 120-ohm termination. Alternately, a processor with 120-ohm onboard termination would need no additional termination on the backplane; any terminators on the backplane should be removed, and an expansion cable connector should be chosen without terminators.

In the last backplane, the 120-ohm termination can be provided in two ways. The termination resistors can reside either on the expansion cable connector card or on a bus termination card, such as the BDV11.

Note

The BDV11 was designed to be used in an 18-bit system and, therefore, does not have terminations on the four top address lines. ECO# M8012-ML005 explains how to connect wires from four unused terminations in one of the packs to the four address lines added to the 22-bit bus.

No modules with terminators should be located in the second backplane of a three-backplane system.

Figure 52-2 illustrates a multiple backplane system configuration.

Table 52-3 • Expansion Kits

Subcomponents	
BC05L-xx	120-ohm expansion cable where "xx" is the length in feet.
BC02D-xx	120-ohm expansion cable where "xx" is the length in feet.
M9400-XX	Expansion cable connector card used at the end of the cable nearest the CPU. The -XX designates the terminations on the board: -YD has no terminations -YE has 240-ohm terminations
M9401	Expansion cable connector card used at the end of the cable away from the CPU. Board has no terminations.
M9404-00	Expansion cable connector card used at the end of the cable nearest the CPU. Board has no terminations.
M9405-YA	Expansion cable connector card used at the end of the cable away from the CPU. Board has 120-ohm terminatons.
BCV1A-xx	Consists of M9400-YD cable connector — no terminations M9401 cable connector — no terminations (2) BC05L-xx 120-ohm expansion cable This assembly is typically used to connect the second and third backplanes in a three-backplane system.

(continued on next page)

Table 52-3 ▪ Expansion Kits (Cont.)

Expansion Assemblies	
BCV1B-xx	Consists of: M9400-YE cable connector — 240-ohm termination M9401 cable connector — no terminations (2) BC05L-xx 120-ohm expansion cable This assembly is typically used to connect the first and second backplanes in a multiple backplane system that uses a processor with 220-ohm onboard termination.
BCV2A-xx	Consists of: M9404-00 cable connector — no terminations M9405-YA cable connector — 120-ohm terminations (2) BC02D-xx 120-ohm expansion cable This assembly is typically used to connect the backplanes in a two-backplane system or the second and third backplanes in a three-backplane system.

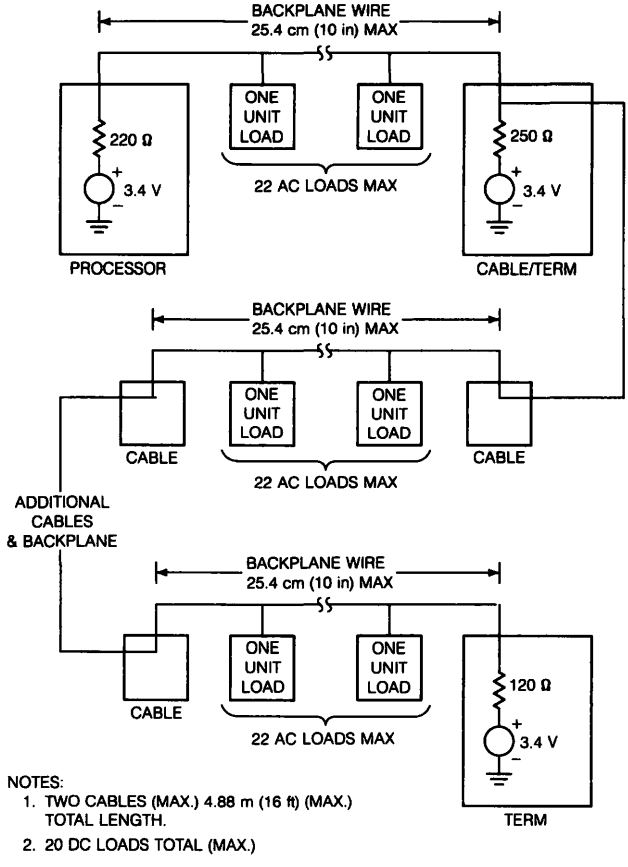


Figure 52-2 ▪ Multiple Backplane Configuration

The expansion cables used to connect the backplanes of a multiple backplane system must conform to the following rules:

- The cables connecting the first two backplanes must be 2 feet (61 cm) or longer in length.
- The cables connecting the second and third backplanes must be 4 feet (122 cm) longer or shorter than the cables connecting the first and second backplanes.
- The combined length of the connecting cables must not exceed 16 feet (4.88 m).

Total power requirements for each backplane can be determined by obtaining the total power requirements for each module in the backplane. When distributing power in multiple backplane systems, do not attempt to distribute power via the Q-bus cables. Provide separate, appropriate power wiring from each power supply to each backplane. Each power supply should be capable of asserting BPOK and BDCOK signals according to bus protocol.

Chapter 53 • BA11-M Enclosure

The BA11-M enclosure includes an H9270-A backplane and an H780 power supply system mounted in an enclosure with a blank front panel. The H9270-A is an 18-bit backplane with four Q/Q quad-slots.

The BA11-M comes in the following variations:

BA11-MA	Mounting box; H9270-A backplane; H780-A power supply for 115 Vac, 60 Hz; with a master console panel
BA11-MB	Mounting box; H9270-A backplane; H780-B power supply for 230 Vac, 50 Hz; with a master console panel
BA11-MC	Mounting box only
BA11-ME	Mounting box; H9270-A backplane; H780-E power supply for 115 Vac, 60 Hz; with a slave console panel
BA11-MF	Mounting box; H9270-A backplane; H780-F power supply for 230 Vac, 50 Hz; with a slave console panel

• Specifications

Dimensions (including bezel)	
Width	48.3 cm (19 in)
Height	8.9 cm (3.5 in)
Depth	
Without mounting brackets	34.3 cm (13.5 in)
With mounting brackets	38.1 cm (15.0 in)
Shipping Weight	18.1 kg (40 lb)
ac input power	100-127 Vrms, 50 ± 1 Hz or 60 ± 1 Hz, 400 W maximum, or 200-254 Vrms, 50 ± 1 Hz or 60 ± 1 Hz, 400 W maximum
dc output power	+5 Vdc ±3%, 0-18 A load (static and dynamic) +12 Vdc ±3%, 0-3.5 A load (static and dynamic) Maximum output power: 120 W (total)
Recommended circuit breaker rating	15 A and 115 Vac or at 230 Vac

▪ Related Documentation

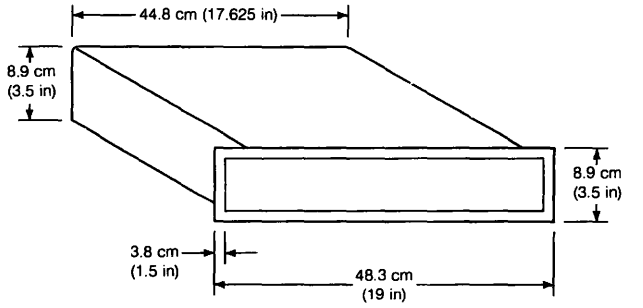
Document Title	Order Number
Illustrated Parts Breakdown	EK-BA11M-IP
BA11-M Field Maintenance Print Set	MP-BA11M-00

▪ Description

The BA11-M is a rackmounted enclosure that provides power and cooling for an H9270-A backplane and the installed modules. The backplane accepts either eight dual- or four quad-size modules. Modules are accessible from the front of the box. A cable area is provided for routing I/O cables from the modules to the rear of the box where a cable clamp allows cables to be strain-relieved before leaving the box. An ac ON/OFF switch and line cord are located at the rear of the box. Two of the eight dual-size slots are normally used for cabling and termination, which leaves six bus slots available for options. Note that multiboard options that require the special backplane interconnection on connections card D (i.e., RLV11) are not accommodated by this expansion box. The BA11-M is available in two line voltage variations—115 V and 230 V. Each version accommodates either 60 Hz or 50 Hz line frequency.

Mechanical and mounting details of the BA11-M are shown in Figures 53-1 and 53-2.

Mounting Box: Physical Specifications



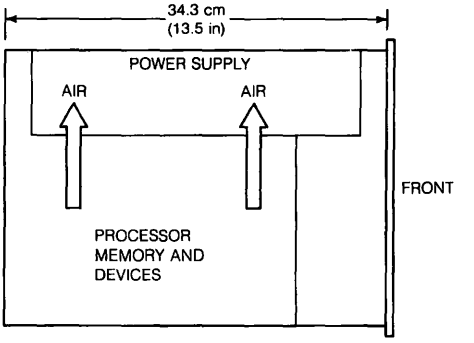


Figure 53-1 ▪ BA11-M Assembly Unit

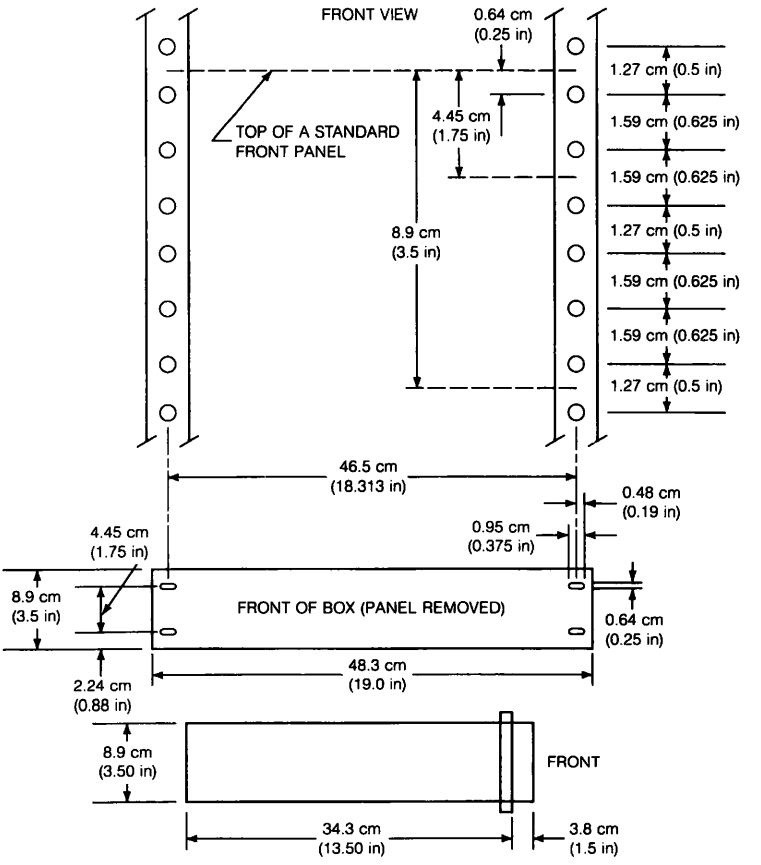


Figure 53-2 ▪ BA11-M Cabinet Mounting

▪ Cables

The following power supply and control panel interface cables are available for use with the BA11-M enclosure:

Cable	Digital Part Number
DC output cable	7011584-0-0
Power supply status cable (logic cable)	7011411-0K-0
Power supply console cable	7008612-0M-0

Chapter 54 • BA11-N Enclosure

The BA11-N enclosure (Figure 54-1) includes an H9273 backplane, an H786 power supply, and an H403-A ac input panel mounted in an enclosure with either a blank front panel or bezel assembly. The H9273-A is an 18-bit backplane with nine Q/CD quad slots.

The BA11-N enclosure comes in the following variations:

BA11-NC	Mounting box; H9273-A backplane; H786 power supply for 115 Vac, 60 Hz; with a bezel assembly
BA11-ND	Mounting box; H9273-A backplane; H786 power supply for 230 Vac, 50 Hz; with a bezel assembly
BA11-NE	Mounting box; H9273-A backplane; H786 power supply for 115 Vac, 60 Hz; with a blank front panel
BA11-NF	Mounting box; H9273-A backplane; H786 power supply for 230 Vac, 50 Hz; with a blank front panel

• Specifications

BA11-N Enclosure:

Dimensions (including bezel)	
Width	48.3 cm (19 in)
Height	13.2 cm (5.19 in)
Depth	
Without mounting brackets	57.8 cm (22.7 in)
With mounting brackets	67.96 cm (26.75 in)
Weight (without modules)	20 kg (44 lb)
Input voltage	
BA11-NC, -NE	115 Vac
BA11-ND, -NF	230 Vac
Input current	
BA11-NC, -NE	12 A maximum
BA11-ND, -NF	6 A maximum

Note

Input current consists of that used by the BA11-N itself, plus whatever current is supplied via the convenience ac outlet (J3) to an expander box; the total current must be less than the maximum specified.

Circuit breaker rating	15 A at 115 Vac or 230 Vac
H786 Power Supply:	
Current rating	5.5 A at 115 Vrms 2.7 A at 230 Vrms
Inrush current	100 A peak, for ½ cycle at 128 Vrms or 256 Vrms
Apparent power	630 VA
Power factor	The ratio of input power to apparent power shall be greater than 0.6 at full load and low input voltage
Output Power	+5 Vdc ±250 mV at 15.5 A (A minimum of 2 A of +5 Vdc power must be drawn to ensure that the +12 Vdc supply regulates properly.) +12 Vdc ±600 mV at 8 A
Powerup/powerdown characteristics	
Static performance	
Powerup	BDCOK goes high; 75 Vac BPOK goes high; 90 Vac
Powerdown	BPOK goes low; 80 Vac BDCOK goes low; 75 Vac
Dynamic performance	
Powerup	3 ms (min) from dc power within specification or to BDCOK asserted 70 ms (min) from BDCOK asserted to BPOK asserted
Powerdown	4 ms (min) from ac power off to BPOK negated 4 ms (min) from BPOK negated to BDCOK negated 5 μsec (min) from BDCOK negated to dc power as of specifications

▪ Related Documentation

Document Title	Order Number
BA11-N Mounting Box User Manual	EK-BA11N-UG
BA11-N Mounting Box Technical Manual	EK-BA11N-TM
Illustrated Parts Breakdown	EK-BA11N-IP
BA11-N Field Maintenance Print Set	MP-00487-00

▪ Description and Configuration

Mechanical and mounting details for the BA11-N are shown in Figure 54-2.

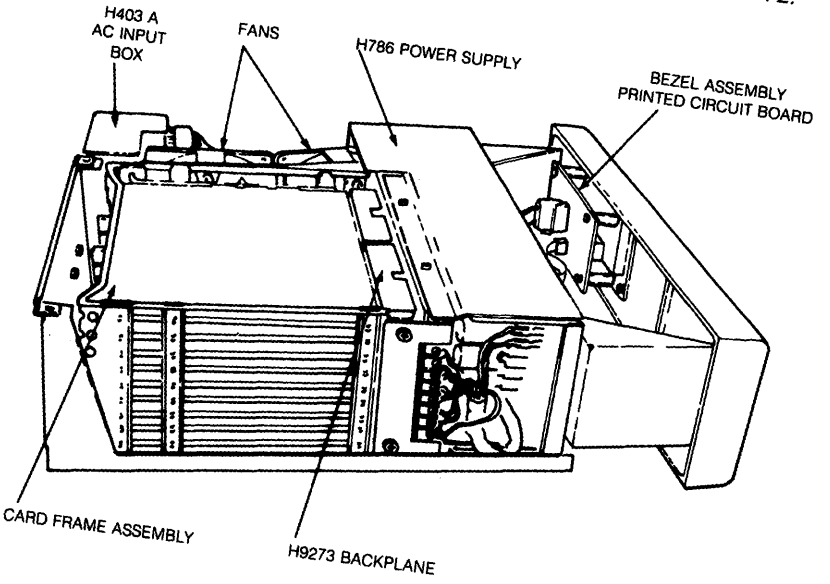


Figure 54-1 ▪ BA11-N Major Assemblies

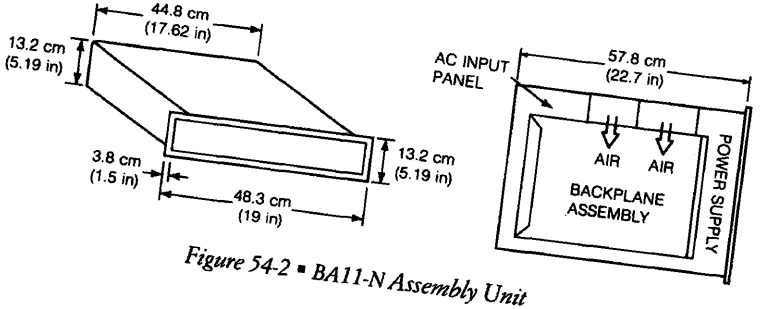


Figure 54-2 ▪ BA11-N Assembly Unit

The ac input box, power supply, and H9273 logic assembly are attached to the logic-box base. The power supply assembly is hinged to the base and can be swung open to expose the internal components; with little effort, the entire assembly can be removed from the base and replaced. Q-bus modules are inserted in the backplane from the rear of the box through an access door that is equipped with strain reliefs for Q-bus and communications cables.

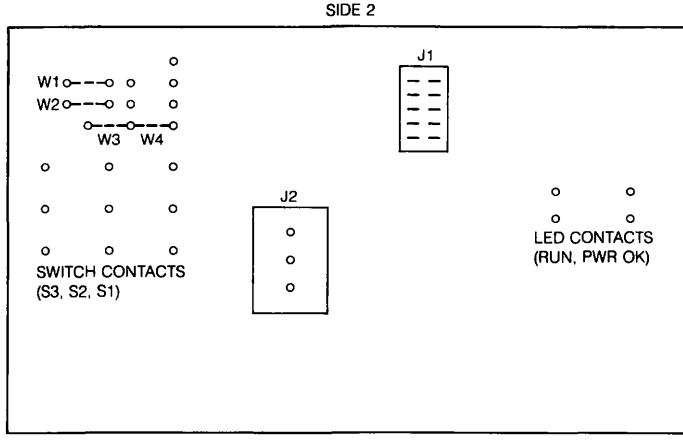
When the unit is to be mounted in an equipment rack, the logic-box cover is attached to the rack with mounting hardware. The logic-box base slides into the mounted cover and a spring-button assembly engages to prevent the base from being accidentally pulled out of the cover.

Backplane Configuration

There are three jumpers used to configure the H9273-A backplane. See Chapter 60 for a discussion of the function and configuration of these jumpers.

Bezel Assembly Jumpers

There are four jumper positions (W1 through W4) on the printed circuit board of the bezel assembly (see Figure 54-3). When the board is manufactured, jumpers are inserted in positions W1, W2 and W4; position W3 is left open. Table 54-1 lists these jumpers and their functions.



NOTES:
1. VIEW IS FROM THE REAR OF THE BEZEL WHEN THE BOARD IS MOUNTED ON THE BEZEL.
2. JUMPERS ARE MOUNTED ON SIDE 1.

Figure 54-3 ▪ Bezel Printed Circuit Board

Table 54-1 ▪ Bezel Assembly Jumpers

Jumper Position	Jumper In	Jumper Out
W1, W2	When the bezel AUX ON/OFF switch is used to control the power supply generated LTC signal. (When the switch is in the AUX ON position, LTC-initiated interrupts are possible.)	When the bezel AUX ON/OFF switch is used to turn the system power controller on and off.
W3	When the bezel is to be mounted on an expander box. (W3 permits the HALT switch to light the RUN indicator).	When the bezel is part of the main box; that is, the CPU is mounted in this bezel's backplane.
W4	When the bezel is part of the main box. (W4 enables the S RUN L signal to light the RUN indicator.)	When the bezel is mounted on an expander box.

Chapter 55 ▪ BA11-S Enclosure

The BA11-S enclosure (Figure 55-1) includes an H9276 backplane, two cooling fans (a 70 cfm fan to cool the logic boards and a 100 cfm fan to cool the power supply), an H7861 power supply, and an H403-B ac input box. The H9276 is a 22-bit backplane, with nine Q/CD quad slots.

The BA11-S enclosure is available in the following variations:

Model	Primary Power and Front Panel
BA11-SA	120 V; control panel
BA11-SB	240 V; control panel
BA11-SC	120 V; blank panel
BA11-SD	240 V; blank panel
BA11-SE	120 V; blank bezel; no cable or expansion modules
BA11-SF	240 V; blank bezel; no cable or expansion modules

▪ Specifications

BA11-S Enclosure:

Dimensions (including bezel)	
Width	48.3 cm (19 in)
Height	13.2 cm (5.19 in)
Depth (without mounting brackets)	57.8 cm (22.75 in)
Input voltage	
BA11-SA, SC, SE	120 Vac
BA11-SB, SD, SF	240 Vac
Input current	
BA11-SA, SC, SE	6 A maximum
BA11-SB, SD, SF	3 A maximum
Output voltage	+5 V at 2 A to 36 A +12 V at 0.0 A to 5 A

H7861 Power Supply:

Current rating	5.5 A, at 120 Vrms 2.7 A, at 240 Vrms
Inrush current	100 A peak, for ½ cycle at 128 V rms or 256 Vrms
Apparent power	630 VA
Power factor	The ratio of input power to apparent power shall be greater than 0.6 at full load and low input voltage.
Output power	+5 Vdc, ± 150 mV, at 36 A (A minimum of 2 A of +5 Vdc power must be drawn to ensure that the +12 Vdc supply regulates correctly.) +12 Vdc at 5 A
Powerup/powerdown characteristics	
Static performance	
Powerup	BDCOK goes high: at 75 Vac BPOK goes high: at 85 Vac
Powerdown	BPOK goes low: at 80 Vac BDCOK goes low: at 75 Vac
Dynamic performance	
Powerup	3 ms (minimum) from dc power within specification to BDCOK asserted 70 ms (minimum) from BDCOK asserted to BPOK asserted
Powerdown	4 ms (minimum) from ac power off to BPOK negated 4 ms (minimum) from BPOK negated to BDCOK negated 5 μs (minimum) from BDCOK negated to dc power outside of specifications

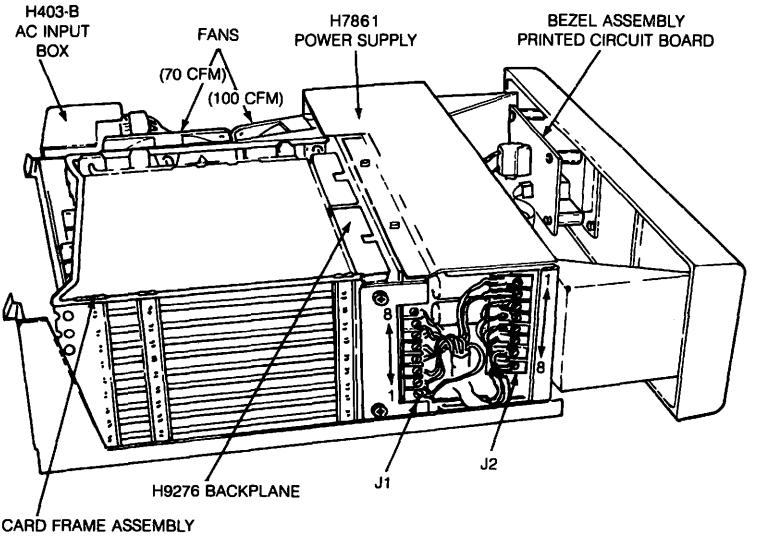


Figure 55-1 ▪ BA11-S Major Assemblies

▪ Related Documentation

Document Title	Order Number
PDP-11/23B Mounting Box Technical Manual	EK-23BMB-TM
PDP-11/23B Mounting Box User's Manual	EK-23BMB-UG
BA11-S Field Maintenance Print Set	MP-01233-00

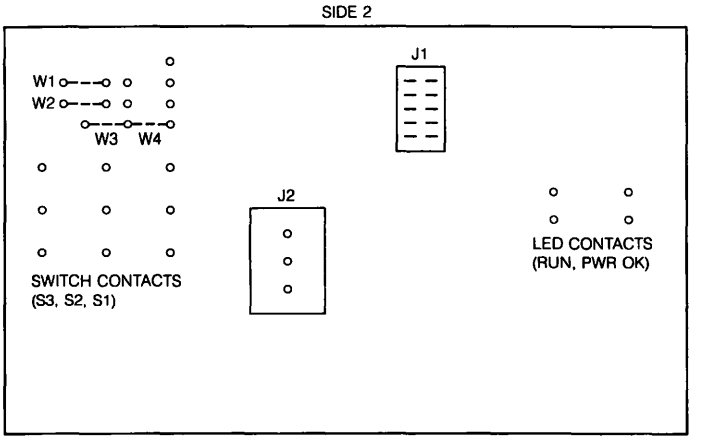
▪ Configuration

The H9276 backplane is configured by means of three jumpers, W1 through W3. When the backplane is manufactured, only jumper W1 is installed. Table 55-1 lists the jumpers and their functions.

Table 55-1 ▪ H9276 Backplane Jumpers

Jumper	Jumper In	Jumper Out
W1	When a power supply generated LTC signal is used to assert the BEVNT Q-bus signal.	To disable the linetime clock as BEVNT from the power supply.
W2, W3	Only when using a KD-11 quad LSI-11 CPU module (M7264) in slot 1.	For all other LSI-11 type processors in slot 1.

There are four jumper positions (W1 through W4) on the printed circuit board of the bezel assembly (see Figure 55-2). When the board is manufactured, jumpers are inserted in positions W1, W2, and W4; position W3 is left open. Table 55-2 lists these jumpers and their functions.



NOTES:
1. VIEW IS FROM THE REAR OF THE BEZEL WHEN THE BOARD IS MOUNTED ON THE BEZEL.
2. JUMPERS ARE MOUNTED ON SIDE 1.

Figure 55-2 ▪ Bezel Printed Circuit Board

Table 55-2 ▪ Bezel Assembly Jumpers

Jumper Position	Jumper In	Jumper Out
W1, W2	When the bezel AUX ON/ OFF switch is used to control the power supply generated LTC signal. (When the switch is in the AUX ON position, LTC- initiated interrupts are possible.)	When the bezel AUX ON/ OFF switch is used to turn the system power controller on and off.
W3	When the bezel is to be mounted on an expander box. (W3 permits the HALT switch to light the RUN indicator.)	When the bezel is part of the main box; that is, the CPU is mounted in this bezel's backplane.
W4	When the bezel is part of the main box. (W4 enables the S RUN L signal to light the RUN indicator.)	When the bezel is mounted on an expander box.

Chapter 56 • BA23-A Enclosure

The BA23-A enclosure contains two dc fans, an H9278-A backplane with a card frame assembly, an H7864 power supply, a control panel (54-15610), and a patch and filter panel assembly. The H9278-A is a 22-bit backplane with eight quad slots. It is unique in that it has Q/CD signals on slots 1 through 3 and Q/Q signals on slots 4 through 8.

The BA23-S is available in two models. The BA23A-AR is the rackmount model, with front plastic cover and sleeves. The BA23A-AF is the floormount model, with front and rear plastic covers, sides, and a pedestal base. The floormount model is easily converted for tabletop use by removing the pedestal base and installing four rubber feet.

• Specifications

Physical Characteristics	BA23A-AR	BA23A-AF
Height	13.34 cm (5.25 in)	64.25 cm (24.5 in)
Width	48.25 cm (19.0 in)	25.40 cm (10.0 in)
Depth	64.34 cm (25.3 in)	72.64 cm (28.6 in)
Weight	24.00 kg (53.0 lb)	31.75 kg (70.0 lb)
Power	+5 V ±2.5%, 36 A (typical) +12 V ±2.5%, 7 A (typical)	
Nonstandard Environmental Specifications		
Operating		
Temperature	15°C to 32°C (59°F to 90°F)	
Relative humidity	20% to 80% noncondensing	
Wet bulb temperature	25°C (77°F) maximum	
Altitude	Up to 8000 ft	
Storage		
Altitude	Up to 40,000 ft	

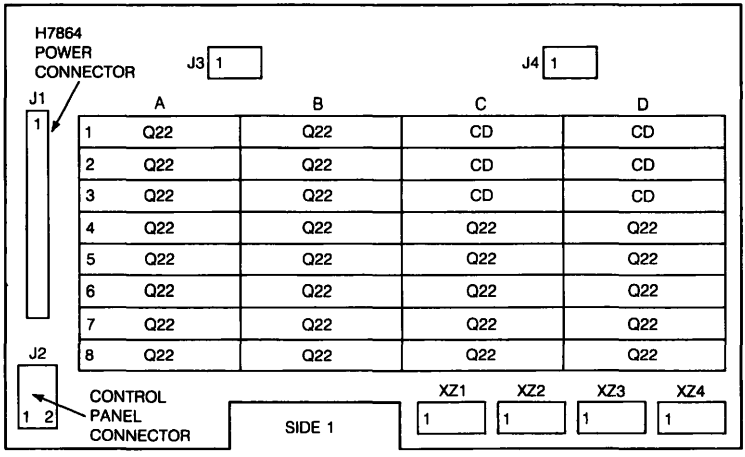
▪ Related Documentation

Document Title	Order Number
Micro/PDP-11 System Technical Manual	EK-OLCP5-TM
Micro/PDP-11 System Pocket Service Guide	EK-OLCP5-PS
BA23 Unit Assembly Drawings	BA23-A-DBP
BA23 Field Maintenance Print Set	MP-01651-00

▪ Description and Configuration

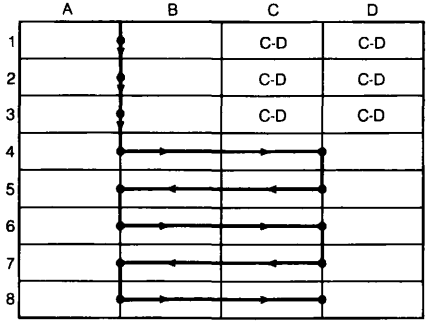
The BA23-A enclosure contains an 8-slot H9278-A backplane for mounting both dual- and quad-height modules. The H9278-A (shown in Figure 56-1) is a 22-bit backplane providing Q/CD signals on slots 1 through 3 and Q/Q signals on slots 4 through 8. The backplanes grant continuity chaining is shown in Figure 56-2.

The backplane is attached to a signal distribution printed circuit board, which provides connectors for a fixed disk drive, diskette drive, RQDX1 controller module, and control panel cables. Figure 56-3 shows the layout of the signal distribution printed circuit board.



NOTES:
1. CONNECTORS J1, J2, J3, AND J4 ARE MOUNTED ON SIDE 2.
2. XZ1–4 ARE BACKPLANE TERMINATOR SOCKETS. THE SIP TERMINATION RESISTORS MOUNTED IN XZ1–4 MUST BE REMOVED WHEN EXPANDING BEYOND THIS BACKPLANE.
3. J3 AND J4 ARE NOT POWER SOURCES. THEY ARE USED TO SUPPLY POWER TO THE BACKPLANE WHEN THE RD51-A FIXED DISK DRIVE OR RX50-AA DISKETTE DRIVE IS NOT INSTALLED.

Figure 56-1 ▪ H9278-A Backplane



NOTE:
C+D (1-3) = CD INTERCONNECT
OTHERS = Q22 FORMAT

Figure 56-2 ▪ H9278-A Backplane Grant Continuity Chaining

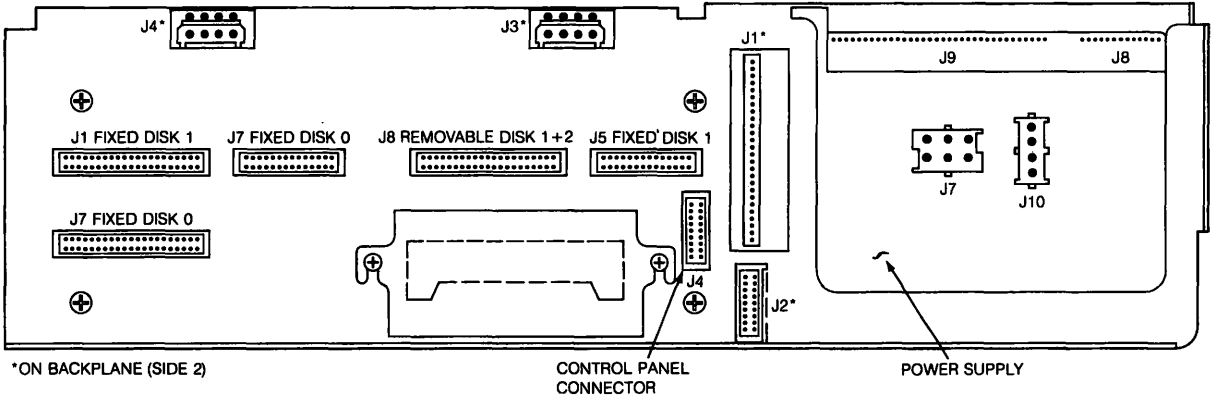


Figure 56-3 ■ Signal Distribution Printed Circuit Board Layout

H7864 Power Supply

The H7864 power supply provides fixed (nonadjustable) voltages of +5 V and +12 V to the H9278-A backplane. The power supply also provides these voltages to any RD51/52 or RX50 disk drives installed in the mounting box. Two brushless dc fans are driven by the power supply. One fan cools the logic modules and power supply. The other fan cools the disk drives.

The H7864 power supply also supplies three system control signals to the H9278-A backplane. Two of these signals, BDCOK and BPOK, are asserted when system power is stable. The third signal, BEVNT, is an external line clock interrupt request to the CPU.

Control Panel

The system control panel (54-15610), shown in Figure 56-4, consists of a printed circuit board equipped with switches and LEDs. The printed circuit board also provides test points for +5 V and +12 V.

The 2-position linetime clock (LTC) switch (switch 1) is used to enable or disable the LTC function. Setting switch 1 ON enables the LTC to function under software control. Setting switch 1 to the OFF position disables the LTC function. The other 2-position switch (switch 2) is not used.

The remaining control panel switches and indicators are discussed at length in the *Micro/PDP-11 System Technical Manual.*

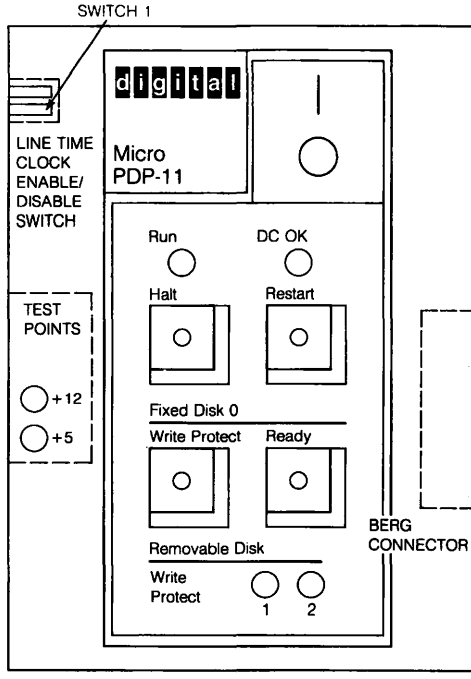
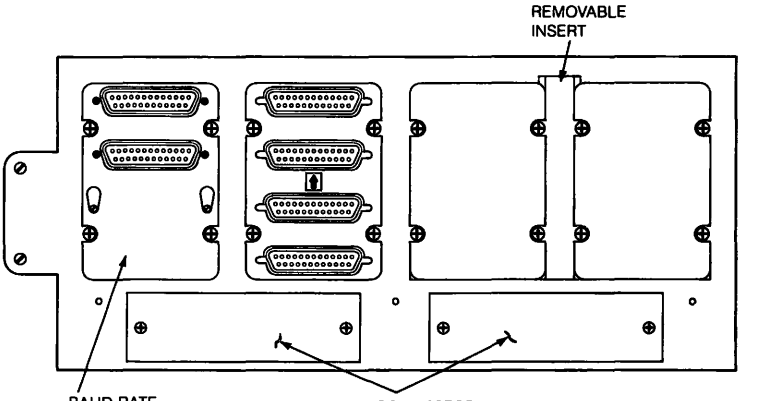


Figure 56-4 ▪ Control Panel Assembly

Patch and Filter Panel Assembly

The patch and filter panel assembly (shown in Figure 56-5) is located behind the rear plastic cover of the BA23-A mounting box. (Rackmount units do not have a rear plastic cover over this assembly.) The assembly provides for the mounting of up to four patch and filter panels (not included), such as those for the CPU and the DZV11 asynchronous multiplexer. A removable division between two of the patch and filter panel spaces allows for the installation of a large panel. The assembly also provides space to accommodate two 50-pin connectors in the event that the system is expanded. Metal plates are mounted in unoccupied panel and connect spaces; these can be easily removed for panel or connector installation.



0	50	8	1800
1	75	9	2000
2	110	10	2400
3	134.5	11	3600
4	150	12	4800
5	300	13	7200
6	600	14	9600
7	1200	15	19200

Figure 56-5 ▪ Patch and Filter Panel Assembly

Chapter 57 • DDV11-B Backplane

The DDV11-B is an optional 18-bit Q-bus expansion backplane for use when additional logic space is required. The DDV11-B is a 9 × 6, 54-slot backplane with a 9 × 4 slot section (18 individual dual-height or nine quad-height module slots) prebused specifically for Q-bus signals, power, and ground connections. The remaining 9 × 2 slot section is provided with +5 Vdc, GND, and −12 Vdc power connections only; this leaves the remaining pins free for use with any special dual-height logic modules to be used in conjunction with the LSI-11 family of modules and bus requirements.

• Description and Specifications

The DDV11-B option consists of the following items:

- Six H863 connector blocks
- Three H8030 connector blocks
- Etched-board bus structure

The etched board completely overlays the entire pin side of all connector blocks and is recessed sufficiently to allow wirewrapping on those same pins with 30-AWG wire. The overall dimensions of the unit are shown in Figure 57-1.

An optional cardcage, type H0341, is also available to provide protection against physical damage to modules and to serve as a cardguide.

The DDV11-B can be mounted in the H909-C enclosure, which includes the H0341 cardguide.

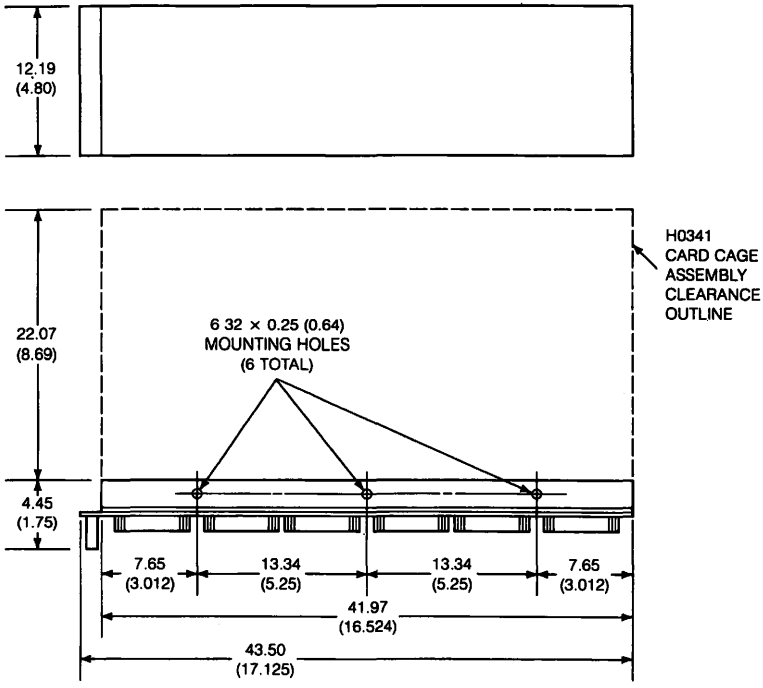


Figure 57-1 ▪ DDV11-B Dimensions

▪ Related Documentation

Document Title	Order Number
DDV11-B Field Maintenance Print Set	MP-00122-00

▪ Configuration

Module Slot Assignments

Figure 57-2 shows the slot location assignments of the DDV11-B. Rows A, B, C, and D are dedicated to the Q-bus. Any module that conforms to the Q-bus specifications can be used in this portion of the DDV11-B. The position numbers indicate the bus-grant wiring scheme with respect to the processor module. The bus-grant signals propagate through the slot locations in the position order shown in Figure 57-2 until they reach the requesting device. Any unused slots must be jumpered to provide bus-grant signal continuity, or it is recommended that unused locations occur only in the highest position-numbered locations.

Rows E and F contain the 18 user-defined slots with power and ground connections provided.

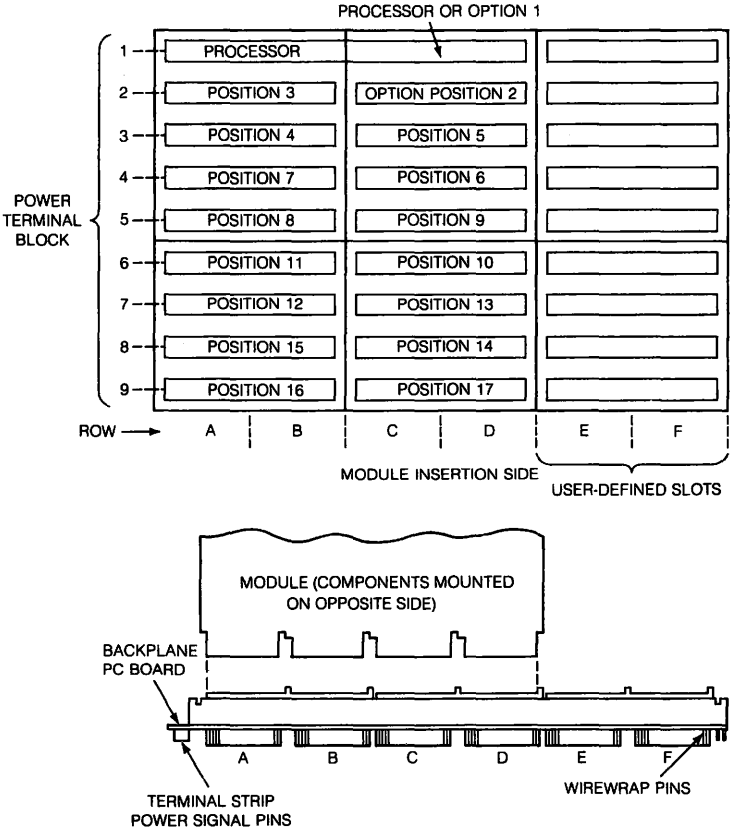


Figure 57-2 ▪ DDV11-B Module Installation and Slot Assignments

dc Power and Power Signal Connections

dc power is supplied to the modules in the DDV11-B through the backplane PC board. The power and ground leads from the external source connect to the seven-position terminal board mounted on the edge of the PC board, as shown in Figure 57-3. Any suitable connector terminals, solder or crimp style, can be attached to the power supply leads and inserted under the terminal strip screws. A jumper tab is mounted between the two +5 V screws and between the two ground (GND) screws on the terminal board. The total current capability of the DDV11-B and the wire size required are listed in Table 57-1.

The power signal pins are located at the opposite end of the backplane PC board from the power terminal strip. A mating female connector (Digital part number 12-11206-02 or 3M part number 3473-3) can be inserted over the pins and used to connect the external signals to the backplane.

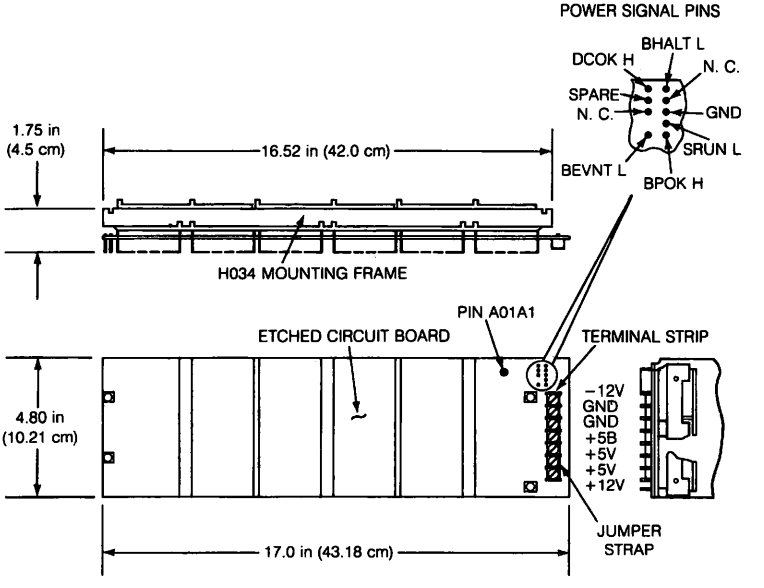


Figure 57-3 ▪ DDV11-B Power Wiring

Table 57-1 ▪ DDV11-B Current Capability

Terminal	Maximum Current	Wire Size (AWG)
+12 V	20 A	14
+5 V (jumped)	40 A	14
+5 V		
+5 B	20 A	
GND (jumped)	40 A	14
GND		
-12 V	20 A	

Chapter 58 ▪ H780 Power Supply

Six H780 power supply options are available for use in Q-bus systems. Individual model numbers determine combinations of 115 or 230 Vac (nominal) primary power and selection of master console, slave console, or no console. Models are listed below.

Model Number	Input Power	Console
H780-C	115V	None
H780-D	230V	None
H780-H	115V	Master
H780-J	230V	Master
H780-K	115V	Slave
H780-L	230V	Slave

▪ Specifications

Temporary Line Dips Allowed	100% of voltage, 20 msec maximum
ac Inrush Current	70 A at 127 V, 60 Hz (8.33 msec) 25 A at 254 V, 50 Hz (10 msec)
Input Power (fans included)	340 W at full load (maximum) 290 W at full load (typical)
Input Protection	H780-C, -H, -K (100-127 Vac) fast blow, 5 A fuse (See Note 1.) H780-D, -J, -L (200-254 Vac) fast blow, 2.5 A fuse
Hi-Potential	2 kV for 60 seconds from input to output, or input to chassis
Output Power (combinations not to exceed 110 W)	+5 V, 1.5 A to 18 A +12 V, 0.25 A to 3.5 A
Maximum dc Current under Fault Conditions	+5 V bus = 28 A +12 V bus = 9.5 A
+5V Output	
Total Regulation	5 V ±3%
Line Regulation	±0.5%
Load Regulation	±1.0%
Stability	0.1%/1000 hours

Thermal Drift	0.025%/°C (See Note 2.)
Ripple	150 mV p-p (1% for f<3 kHz)
Dynamic Load Regulation	±1.2% di/dt = 0.5 A µs delta I = 5 A
Noise	1% peak at f>100 kHz (noise is superimposed on ripple)
Interaction due to +12 V	±0.05%
+12 V Output	
Total Regulation	12 V ±3%
Line Regulation	±0.25%
Load Regulation	±0.5%
Stability	0.1%/1,000 hours (See Note 2.) 0.025%/°C above 25°C
Ripple	350 mVp-p (1% for f<3kHz)
Dynamic Load Regulation	±0.8% di/dt = 0.5 A µsec f<500Hz delta I = 3A
Noise	1% peak at f>100 kHz (noise is superimposed on ripple)
Interaction due to +5 V	±0.02%
Overvoltage Protection	
+5 V	6.3 V nominal 5.65 V minimum 6.8 V maximum
+12 V	15 V nominal 13.6 V minimum 16.5 V maximum
Adjustments	
+5 V Output	4.05 V to 6.8 V Guarantee range 4.55 V to 5.65 V
+12 V Output	10.6 V to 16.5 V Guarantee range 11.7 V to 13.6 V

Controls	
Rear Panel	ac ON/OFF switch
Front Console	dc ON/OFF switch HALT/ENABLE switch
(Master only)	LTC ON/OFF SWITCH
Console Indicators	dc ON RUN (Master) SPARE (Master only)
Backplane Signals	
Generated	BPOK BDCOK BEVNT
Received (Master only)	BHALT SHRUN
Mechanical	
Cooling	Two self-contained fans provide 0.71 m^3/min (30 ft^3/min) air flow.
Size (W × H × L)	13.97 cm × 8.43 cm × 37.15 cm (5 1/2 in × 3 1/3 in × 14 5/8 in)
Weight	5.90 kg (13 lb)
Nonstandard Environmental Specifications	
Ambient (operating) Temperature	5°C to 50°C (41°F to 122°F)

Notes Relating to Specifications

1. Operation from ac lines below 100 V may cause the power supply to overheat because of decreased air flow from the cooling fans.
2. These parameters apply after five minutes of warmup and are measured with an averaging meter at the processor backplane terminal block under system loading.

• Related Documentation

Document Title	Order Number
H780-C, -D, -H, -J, -K, -L Power Supply User's Manual	EK-H780-OP
H780 Field Maintenance Print Set	MP-H780-00

▪ Description

The H780 master console contains RUN and DC ON indicators for monitoring the processor states, as well as DC ON/DC OFF, LTS ON/OFF, and ENABLE/HALT switches for controlling the processor. The slave console contains only a DC ON indicator for monitoring the status of the slave power supply.

Console Controls and Indicators

The H780-H or -J master console has three LED indicators and three two-position toggle switches. One of the LED indicators is a spare indicator. Circuitry to drive this indicator is included on the console printed circuit board for user application. The console on the H780-K and -L slave supplies has only one LED indicator, DC ON. The H780 console controls and indicators are described in Table 58-1. Additionally, the rear panel of the H780 contains an AC ON/OFF toggle switch and an ac line fuse.

+12 V and +5 V Adjustment Procedure

The H780 power supply is factory-adjusted to produce +12 V and +5 V outputs within the operating tolerance of the system. The adjustment procedures presented allow users to trim the dc outputs of the H780 to meet their particular needs. One adjustment is provided for the +12 V output, while two adjustments (one for the output voltage and one for the switching regulator frequency) are provided for the +5 V. A DVM, an oscilloscope, and a small screwdriver are required. Power supply loading is provided by the Q-bus or processor.

Table 58-1 ▪ H780 Controls and Indicators

Control/Indicator	Type	Function
dc ON	LED indicator	Lights up when the dc ON/OFF toggle switch is set to ON and proper dc output voltages are being produced by the H780. If either the +5 V or +12 V output from the H780 is faulty, the dc ON indicator will not light up. This is the only indicator on the H780-K and -L slave supplies.
RUN	LED indicator	Illuminates when the processor is in the run state (see ENABLE/HALT).

(continued on next page)

Table 58-1 ▪ H780 Controls and Indicators (Cont.)

Control/Indicator	Type	Function
SPARE	LED indicator	Not used by the H780 or processor. The H780 contains circuitry for driving this indicator for user applications.
dc ON/OFF	Two-position toggle switch	When set to ON, enables the dc outputs of the H780. The dc ON indicator will light up if the H780 dc output voltages are of proper values. If a slave supply is connected to a master, the slave dc ON indicator will light if the slave dc output voltages are of proper value. When set to OFF, the dc outputs from the H780 are disabled and the dc ON indicator is extinguished. If a slave supply is connected to a master, the slave dc ON indicator will also extinguish.
ENABLE/HALT	Two-position toggle switch	When set to ENABLE, the BHALT line from the H780 to the processor is not asserted and the processor is in the run mode (RUN indicator lights up). When set to HALT, the BHALT line is asserted, allowing the processor to execute console ODT microcode (RUN indicator extinguished).
LTC ON/OFF	Two-position toggle switch	When set to ON, enables the generation of the linetime clock (LTC) BEVNT signal by the H780. When set to OFF, disables the H780 linetime clock.
AC ON/OFF (rear panel)	Two-position toggle switch	When set to ON, applies ac power to the H780. When set to OFF, removes ac power from the H780.
FUSE (rear panel)	5 A or 2.5 A fast-blow	Protects H780 from excessive current. H780-C, -H, and -K use a 5 A fuse. H780-D, -J, and -L use a 2.5 A fuse.

Chapter 59 ▪ H9270-Q Backplane

The H9270-Q backplane assembly is a 22-bit backplane with four Q/Q quad slots, designed to accept Q-bus processors, memories, and option modules. It accepts up to eight dual-height modules, four quad-height modules, or a mix of both.

The H9270-Q backplane is intended as a replacement for the H9270-A.

▪ Specifications

Mechanical	
Height	11 in (27.9 cm)
Width	11.15 in (28.3 cm)
Length	2.8 in (7.11 cm)
Weight	2.6 lb (1.18 kg)
Bus Loads	
ac	4.4
dc	none

Power

Voltage	Terminals	Maximum Current Rating (25°C)
+12 Vdc	one	9 A
+5 Vdc	one	18 A
+5B Vdc	one	12 A
GND	two	20 A
−12 Vdc	one	4 A

External Signals

There are staked-in pins on the backplane that can be used for system control signals as follows:

Signal	Description
BEVNT	External event interrupt request connected to Q-bus pin BR1.
BPOK	Power OK signal connected to Q-bus pin BB1.
BCDOK	dc power OK signal connected to Q-bus pin BA1.
BHALT	Processor halt signal input to the main processor, connected to Q-bus pin AP1.
GND	Two ground pins

Restrictions
The H9270-Q will not accept any module utilizing CD type interconnect.

▪ Configuration

User-supplied +5 Vdc and +12 Vdc power sources are connected to the backplane via a six-position screw type terminal strip. The +5 Vdc power actually has two terminals connected through a jumper. The terminal labeled "+5B" can be separated and used to supply the battery backup voltage as required. The user's system control signals are connected through nine staked-in pins on the backplane. Figure 59-1 shows the layout of the H9270-Q terminal block.

The H9270-Q supports 22-bit Q-bus address space but is also backward compatible with 18-bit Q-bus products by the removal of eight jumpers. These eight jumpers, located at the top of the backplane assembly, are shown in Figure 59-2.

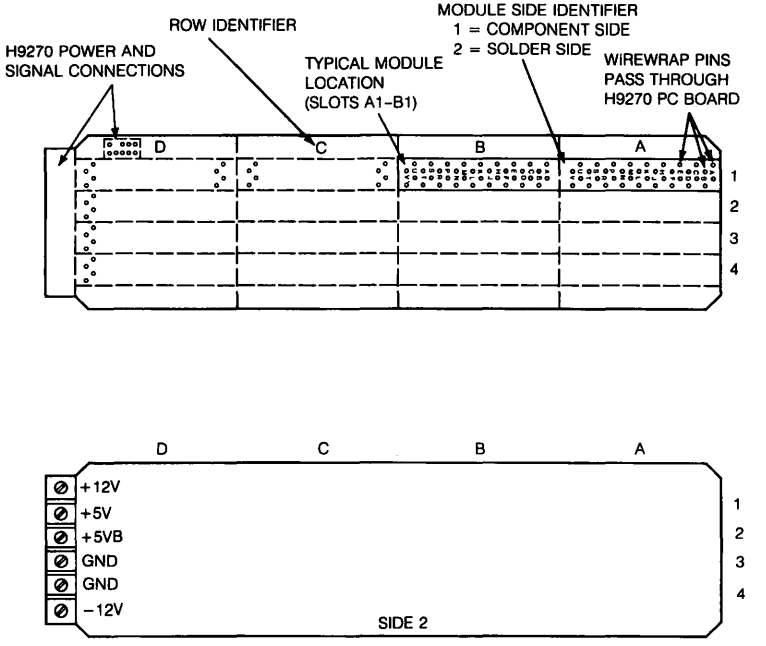


Figure 59-1 ▪ H9270-Q Backplane Terminal Block (Pin Side View Shown)

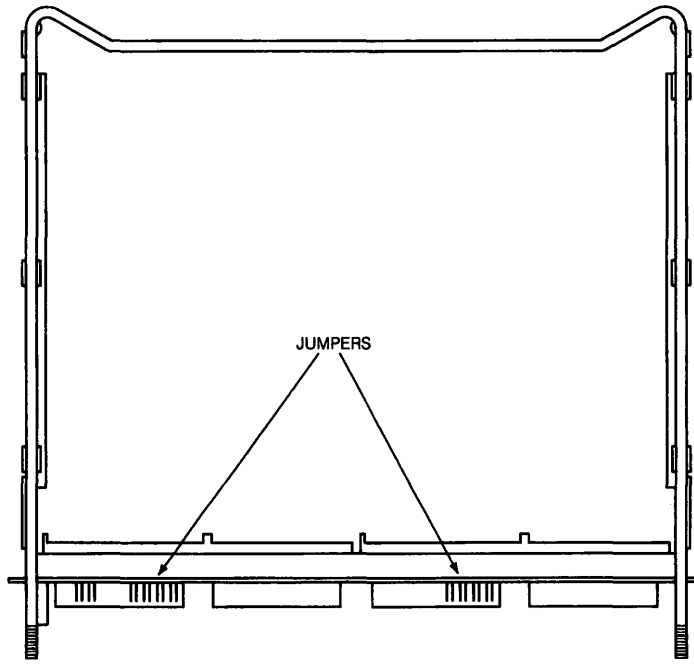


Figure 59-2 ▪ H9270-Q Unit Assembly

Mounting the Backplane

Mounting dimensions and possible methods of mounting the H9270-Q backplane (in any of three planes) are shown in Figure 59-3. Option positions are shown in Figure 59-4. Slot numbers indicate device interrupt and DMA priority in Q-bus systems. The lowest numbered positions receive the highest priority.

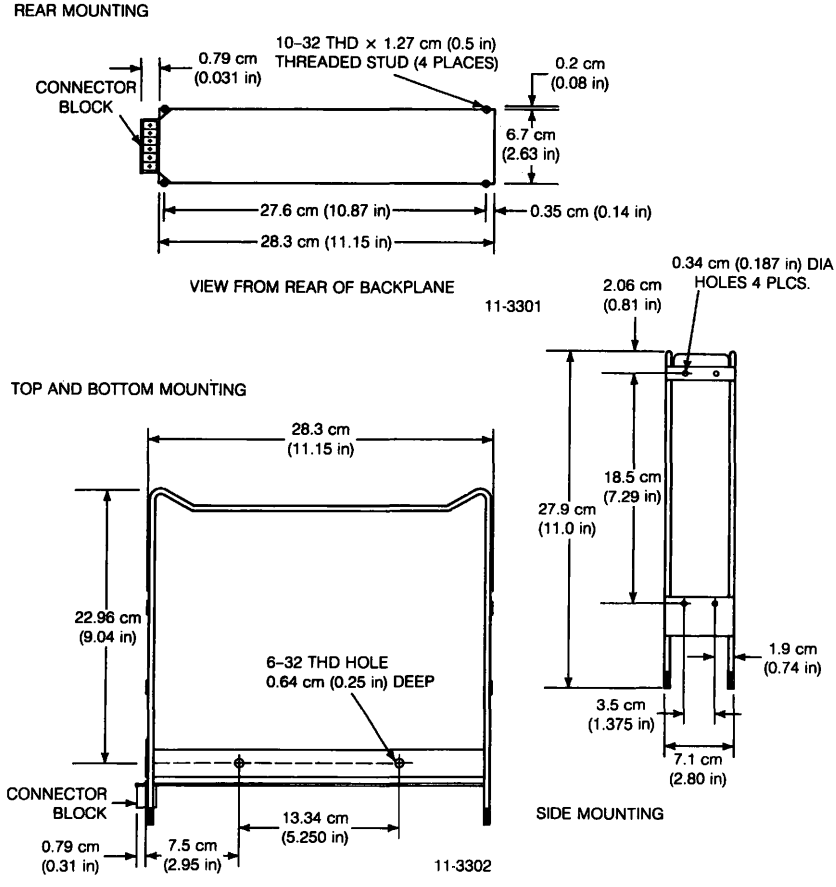


Figure 59-3 ▪ Backplane Mounting

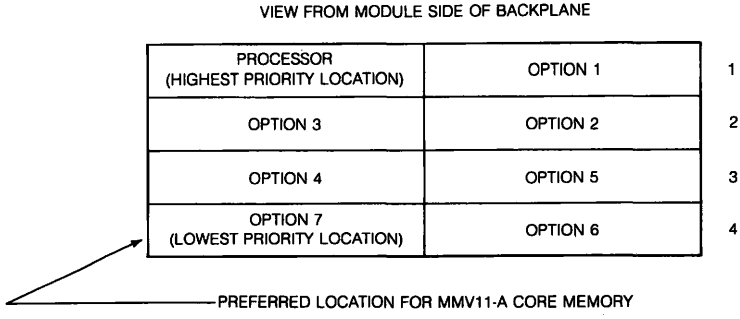


Figure 59-4 ▪ H9270-Q Option Positions

dc Power Connections

The H9270-Q standard power connections are listed in Table 59-1.

▪ VOLTAGE AND CURRENT REQUIREMENTS

A power supply for a single H9270-Q backplane LSI-11 system should have the following capacity:

+5 V ±5% load; 0-18 A static/dynamic
+12 V ±3% load; 1-2.5 A static/dynamic
+5 ripple; less than 1% of nominal voltage
−12 ripple; less than 150 mV p-p (frequency 5 kHz)

Note

Regulation at the H9270-Q backplane must be maintained to the specifications listed above.

The H780 power supply option provides sufficient dc power and generates the required bus signals.

A multiple-backplane system using H9270-Q backplanes should have the same voltage regulation and ripple specification as listed for the single H9270-Q backplane. However, it will be necessary to calculate the actual power requirements, based on individual power requirements for modules used in the system.

- BACKPLANE POWER CONNECTIONS

If the H780 power supply option is not used, perform the following steps to connect power to the H9270-Q backplane.

1. Select wire size. (14 gauge is recommended.) Consider load current and distance between the power supply and backplane.
2. For a standard system, connect the applicable wires to the H9270-Q connector block per Table 59-1. For battery backup, remove the jumper between +5 V and +5 B and connect the applicable wires to the H9270-Q connector block.
3. Connect the ground terminals at the power source.
4. It is recommended that the backplane frame/casting be electrically connected to the system/power supply ground.

Table 59-1 ▪ H9270-Q Backplane Standard Power Connections

Power Source (From)	**H9270-Q Connector Block (To)**	
+12V	+12V	Factory-connected
+5V	+5V	Factory-connected
	+5B	
GND	GND	Factory-connected
GND	GND	Factory-connected
−12V	−12V	This voltage is not required. The connection is available for custom interfaces.

Chapter 60 • H9273-A Backplane

The H9273-A is an 18-bit backplane with nine Q/CD quad slots and a card frame assembly.

• Specifications

Height	12.55 cm (4.94 in)
Length	29.11 cm (11.46 in)
Width	28.3 cm (11.15 in)
Bus Loads	
ac	2.6
dc	0

• Related Documentation

Document Title	Order Number
H9273-A Field Maintenance Print Set	MP-00670-00

• Configuration

The H9273-A backplane logic assembly is shown in Figure 60-1. Power and signals are supplied to the backplane to connectors J7 and J8. These connectors are shown in Figures 60-1, 60-2, and 60-3. Connectors J9 (GND) and J10 (− 12 V) are also shown in Figure 60-2.

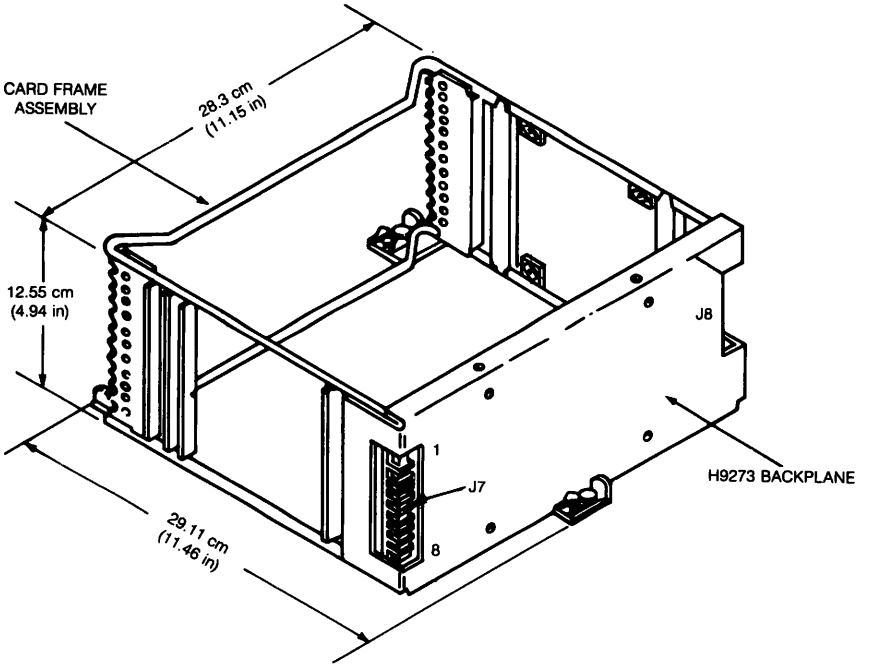


Figure 60-1 ▪ H9273-A Backplane Logic Assembly

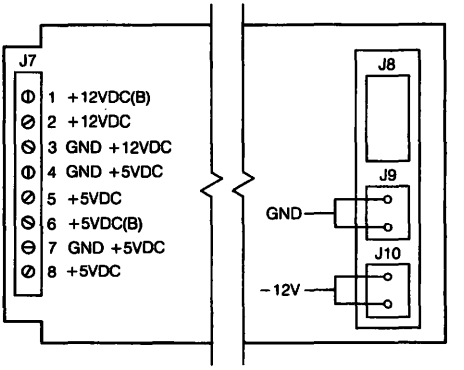


Figure 60-2 ▪ H9273-A Power Connections

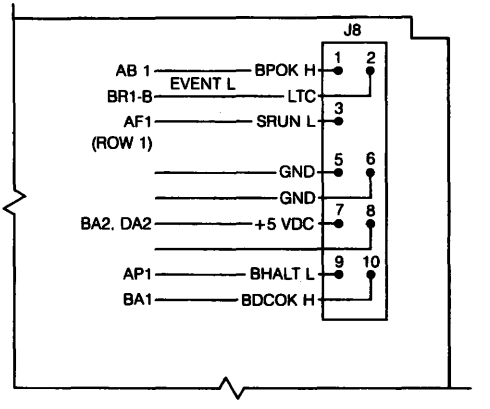


Figure 60-3 ▪ H9273-A Signal Connections

The H9273-A backplane is designed to accept both dual- and quad-height modules. However, as a Q/CD type backplane, it will accept dual-height modules only in the AB slots. (See Chapter 52.)

The H9273-A backplane logic assembly is designed to mount in a BA11-N mounting box or equivalent. Refer to the BA11-N mounting box description for more information.

Note

Connector block pins do not extend beyond the H9273-A printed circuit etch card, thus eliminating the possibility of backplane wirewrapping.

Three jumpers (W1, W2, and W3) are shown in Figure 60-4. Jumper W1 enables the linetime clock when inserted and disables it when removed.

Note

Only one BA11-N mounting box in any system may have the line-time clock enabled.

When inserted, jumpers W2 and W3 allow the LSI-11 quad-height CPU board (module M7264) to run in row 1. Jumpers W2 and W3 are removed when the backplane is used as an expansion backplane in a system.

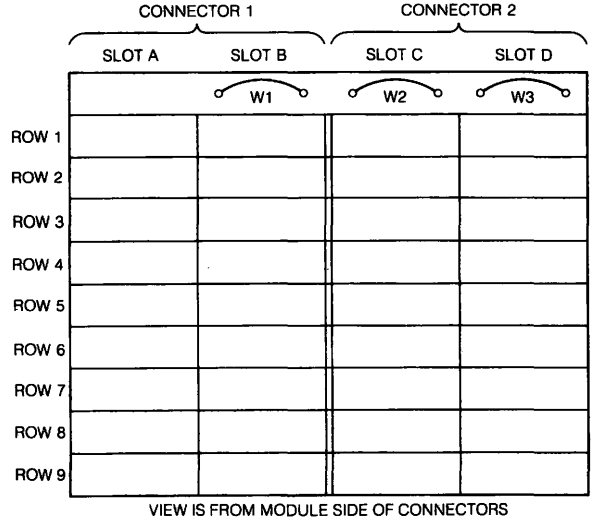


Figure 60-4 ▪ H9273-A Backplane Jumpers

Chapter 61 ▪ H9275-A Backplane

The H9275-A (Figure 61-1) is a 22-bit backplane with nine Q/Q quad slots, designed to accept Q-bus compatible processors, memories, and interface modules.

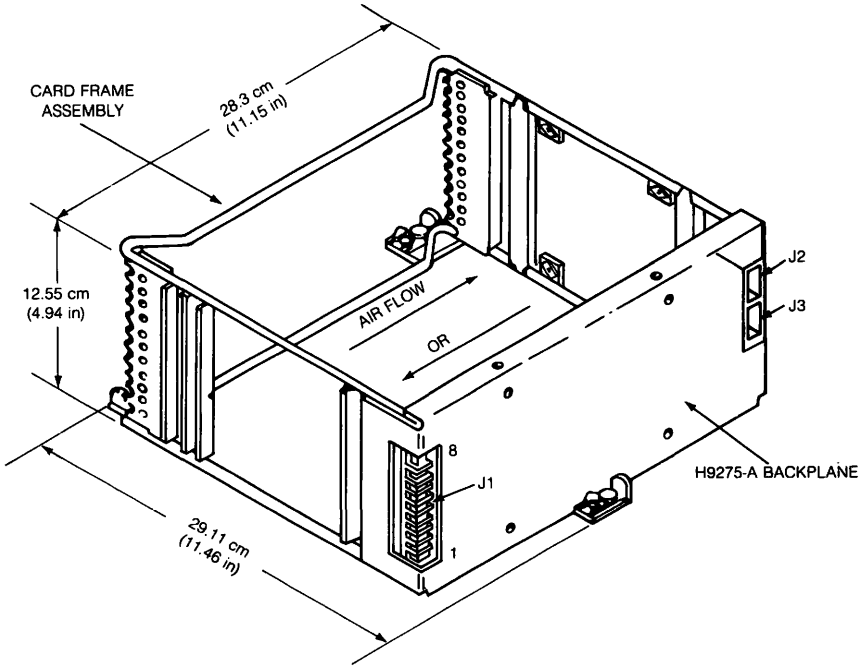


Figure 61-1 ▪ H9275-A Backplane Assembly

▪ Specifications

Height	12.55 cm (4.94 in)
Length	29.11 cm (11.46 in)
Width	28.3 cm (11.15 in)

Bus Loads	
ac	10.0
dc	0

▪ Related Documentation

Document Title	**Order Number**
H9275-A Configuration Guide	EK-H927A-CG

▪ Configuration

The H9275-A backplane assembly has nine jumper wires, designated W1 through W9, that modify the bus configuration. The H9275-A also has connectors that are positioned in four rows, called the A, B, C, and D rows. (These jumpers and connectors are shown in Figure 61-2.) Q-bus compatible modules are plugged into these rows and connected to the bus. Position 1 uses the row A and row B connectors. Position 2 uses the row C and row D connectors. Therefore, row A is wired identically to row C, and row B is wired identically to row D.

As a 22-bit backplane, the H9725-A supports up to four megabytes of memory addressing capability. Processor modules (18-bit) can also be used with the H9275-A with slight variations. Table 61-1 lists the jumper wires that must be removed or installed, depending on which processor is used.

The LSI-11/2 processor can be connected to the H9275-A backplane after the W2, W3, W4, and W5 jumper wires have been removed. These wires connect BDAL <18:21> (the extended address lines that provide 22-bit addressing) address lines to position 1 (the processor position). If jumper wires W2-W5 are not removed, interference of bus operation will result because the LSI-11/2 processor connects signals (not used for addressing) to these jumper wire lines.

The LSI-11 processor can also be used in the H9275-A backplane, provided jumper wires W6, W7, W8, and W9 are removed. Because the LSI-11/2 processor is a quad-height module, it requires positions 1 and 2 on the backplane. Jumper wires W6 through W9 connect the BDAL <18:21> address lines to position 2, which is used by the processor. The W2-W5 jumpers can either be installed or removed, and will not interfere with the operation of the LSI-11 processor.

Table 61-1 ▪ H9275-A Jumper Status for Microprocessors

Processor	Jumper Status W2-W5	W6-W9
LSI-11/23	I	I
FALCON	R	I
LSI-11/2	R	I
LSI-11	-	R

I = jumper installed; R = jumper removed

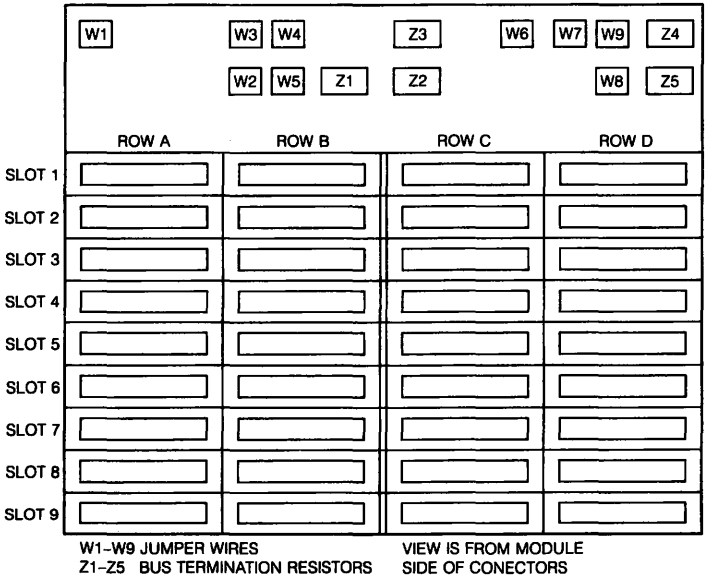


Figure 61-2 ▪ H9275-A Backplane Connectors

Connecting System Power

The H9275-A backplane requires external +5 Vdc and +12 Vdc power sources. The current rating of these power sources is defined by the configuration of the user's system. The external power sources are connected to the standard power connector, J1. The J1 connector is a screw terminal strip located on the rear of the backplane, as shown in Figure 61-3.

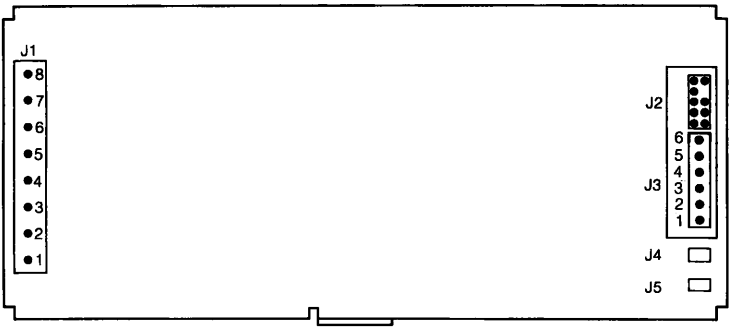


Figure 61-3 ▪ H9275-A Rear View

The J1 terminal strip connectors are rated for 15 amperes per terminal and accept up to a No. 12 wire. The backplane connector pins for the modules are rated at one ampere. Additional +5 Vdc power can be connected to the backplane by using two push-on tabs designated as J4 and J5. J4 and J5 power tabs are used only when the system requires more than 45 amperes of +5 Vdc power. These power tabs are located on the rear of the backplane as shown in Figure 61-3.

Note

The J4 and J5 power tabs should never be used as a +5 Vdc power source from the bus to another device.

The J5 power tab is for the +5 Vdc connection and is rated for 15 amperes. The J4 power tab is for the ground connection and is rated for 15 amperes.

Connecting Control Bus Signals

Control bus signals are connected to the H9275-A backplane through the J2 connector on the rear of the backplane as shown in Figure 61-3. These signals include the power sequence signals BPOK and BDCOK, as well as the signals BHALT and BEVNT. The processor SRUN signal is available to monitor the processor-run condition.

The J2 connector is keyed to accept the LSI-11 console/backplane cable No. 70-11411-OK. This cable must not exceed one meter in length.

Bus Priority

The modules in the system are serviced on a priority basis for bus interrupts and direct memory access (DMA) requests. Bus interrupts function in either a position-dependent priority or a position-independent priority. Position-independent priority is implemented only on the LSI-11/23 CPU.

The bus positions described in Figure 61-4 are numbered in order for the position-dependent priority structure. Priority is determined by the physical placement of the module in the backplane. Position 1 is assigned the highest priority and position 18 is assigned the lowest priority. The priority structure operates with the condition that there are no open or empty positions in the backplane between the placement of the modules. Thus, if a quad-height module is inserted next to a dual-height module, bus grant continuity module G7272 must be installed in the resulting open dual slot.

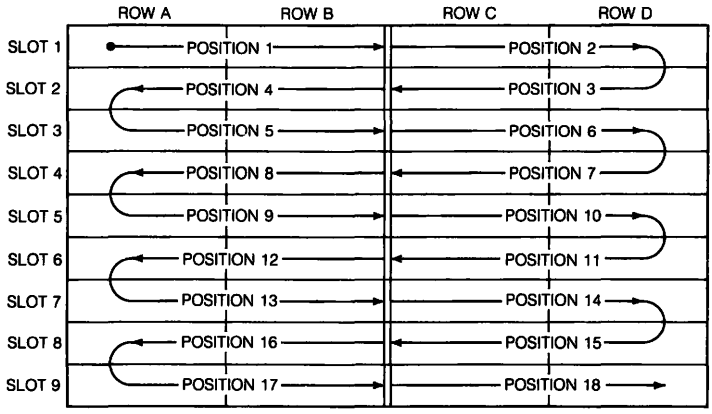


Figure 61-4 ▪ Horizontal Position Priority Structure

Bus Termination

The bused signals are terminated in the backplane with a characteristic impedance of 123 ohms connected to the 3.4 Vdc. The termination resistors are located by Z1 through Z5 in Figure 61-2.

Bus Restrictions

The H9275-A backplane is a maximum LSI-11 system configuration that will not support any external cabling of the bus. This limits any system to the backplane and is not expandable by using additional backplanes. The backplane contains 0.188 inch pins on the connector blocks and will not accept any wirewrap connections.

Chapter 62 ▪ H9281-Q Backplane

The H9281-Q series backplanes are 22-bit, dual-slot backplanes designed to accept dual-height Q-bus modules.

▪ Specifications

Mechanical

	Height (in/cm)	Width (in/cm)	Length (in/cm)	Weight (lb/kg)
H9281-QA	10.8 / 27.4	5.75 / 14.6	3.0 / 7.62	.7 / .32
H9281-QB	10.8 / 27.4	5.75 / 14.6	6.0 / 15.24	1.4 / .64
H9281-QC	10.8 / 27.4	5.75 / 14.6	8.0 / 20.32	2.3 / 1.05

Electrical

	Slots	Rows	ac Bus Loads	dc Bus Loads	Onboard Termination
H9281-QA	4	2	1.1	None	No
H9281-QB	8	2	1.8	None	Yes
H9281-QC	12	2	2.9	None	Yes

+5 Vdc Termination Current (H9281-QB and -QC only)	Normal (no load): 360 mA Maximum (operating): 1,000 mA

Power

Maximum Current Rating (25°C)

Voltage	Model -QA	Model -QB	Model -QC
+12 Vdc	8 A	8 A	8 A
+5 Vdc	8 A	14 A	18 A
+5B Vdc	8 A	10 A	10 A
GND	8 A	20 A	20 A
GND	8 A	20 A	20 A
−12 Vdc	6 A	8 A	8 A
+12B Vdc	8 A	8 A	8 A

External Signals

There is a 10-pin connector (J2) on the backplane which can be used for system control signals as follows:

BEVNT	External event interrupt request connected to Q-bus pin BR1.
BPOK	Power OK signal connected to Q-bus pin BB1.
BDCOK	dc power OK signal connected to Q-bus pin BA1.
BHALT	Processor halt signal input to the main processor, connected to Q-bus pin AP1.
SRUN	Processor-generated signal for driving a run indicator circuit.

Restrictions

The H9281-Q series backplanes will not accept any module utilizing CD type interconnect, nor will they accept any quad-height modules.

▪ Configuration

Mounting dimensions for H9281-Q backplanes are shown in Figures 62-1 and 62-2. The H9281-Q backplanes can be mounted in any plane. The enclosure in which the backplane is mounted, available system space, and cooling air flow will determine an acceptable backplane position in a particular system.

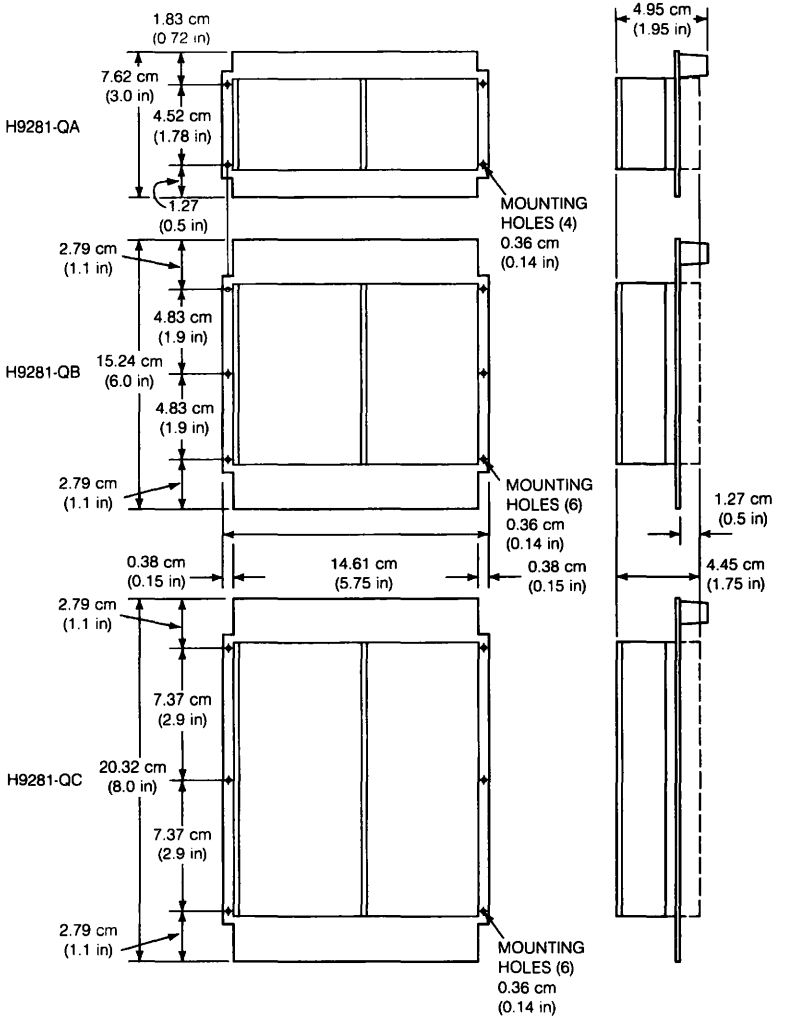


Figure 62-1 ▪ H9281-Q Mounting Dimensions

MODEL	MOUNTING DIMENSION A	ASSEMBLY LENGTH B
H9281-QA	6.86 cm (2.7 in)	7.62 cm (3.0 in)
H9281-QB	11.94 cm (4.7 in)	15.24 cm (6.0 in)
H9281-QC	17.02 cm (6.7 in)	20.32 cm (8.0 in)

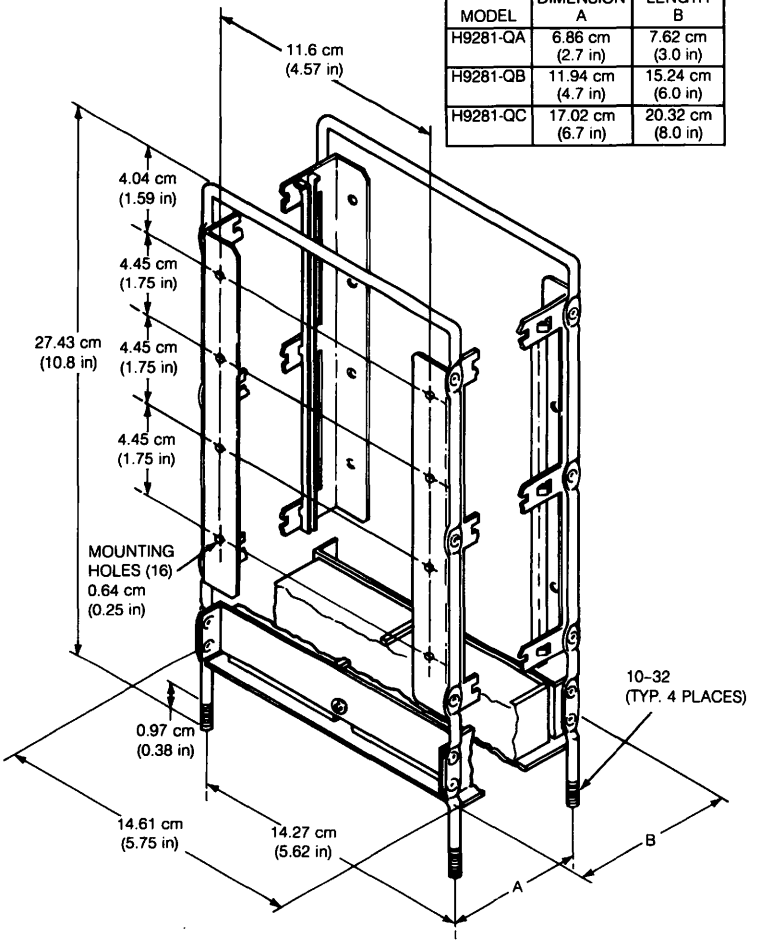


Figure 62-2 ▪ H9281-Q Mounting Dimensions

Connecting System Power

Seven screw terminals are provided on the slot 1 end of the backplane for power connections. Connect system power (and optional battery backup power) as shown in Figure 62-3. Power wiring should be done with a wire gauge appropriate for the total power requirements for options installed in the backplane. The recommended wire size for H9281-Q backplanes is as follows:

H9281-QA	14 gauge
H9281-QB	14 gauge
H9281-QC	12 gauge

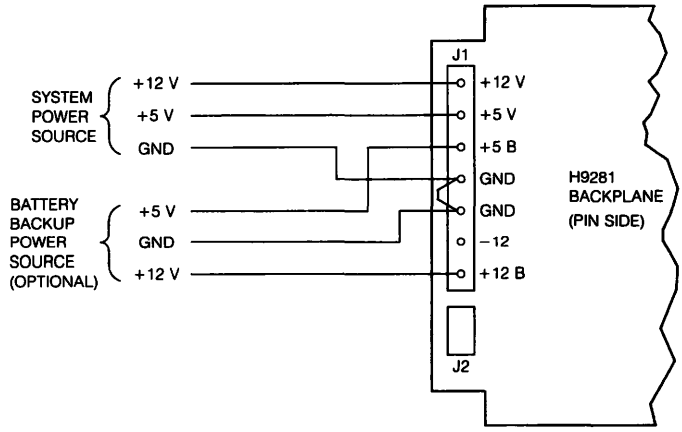


Figure 62-3 ▪ H9281 Power Connections

Select a power supply that will meet LSI-11 system power specifications and supply sufficient current for the options in the system. The H780 power supply is recommended, depending on system power requirements.

Connecting Externally Generated Bus Signals

Externally generated bus signals can be connected to the H9281-Q backplane via connector J2. These signals include power sequence signals BPOK, BDCOK, BHALT and BEVNT. In addition, the processor-generated SRUN signal is available via J2 for driving a RUN indicator circuit. J2 connector pins are fully compatible with the H780 model series power supply or the KPV11-A powerfail/linetime clock.

Device Priority

All Q-bus backplanes are priority structured. Daisychained grant signals for DMA and interrupt requests propagate away from the processor from the first (highest priority device) to successively lower priority devices. Processor module locations and device (option) priorities are shown in Figure 62-4.

Bus Terminations

Backplane models H9281-QB and -QC include 120-ohm bus termination resistors at the electrical end of the bus; therefore, it is not necessary to install a separate 120-ohm bus terminator module in these backplanes.

16- and 18-Bit Addressing

The H9281-Q backplanes support the 22-bit Q-bus address space but can also be configured to be compatible with 18-bit Q-bus products. This is done using pins M1 through M12, located on the backplane between the J1 and J2 connectors, as shown in Figure 62-4. Table 62-1 lists the proper jumper configurations for 18- and 22-bit addressing.

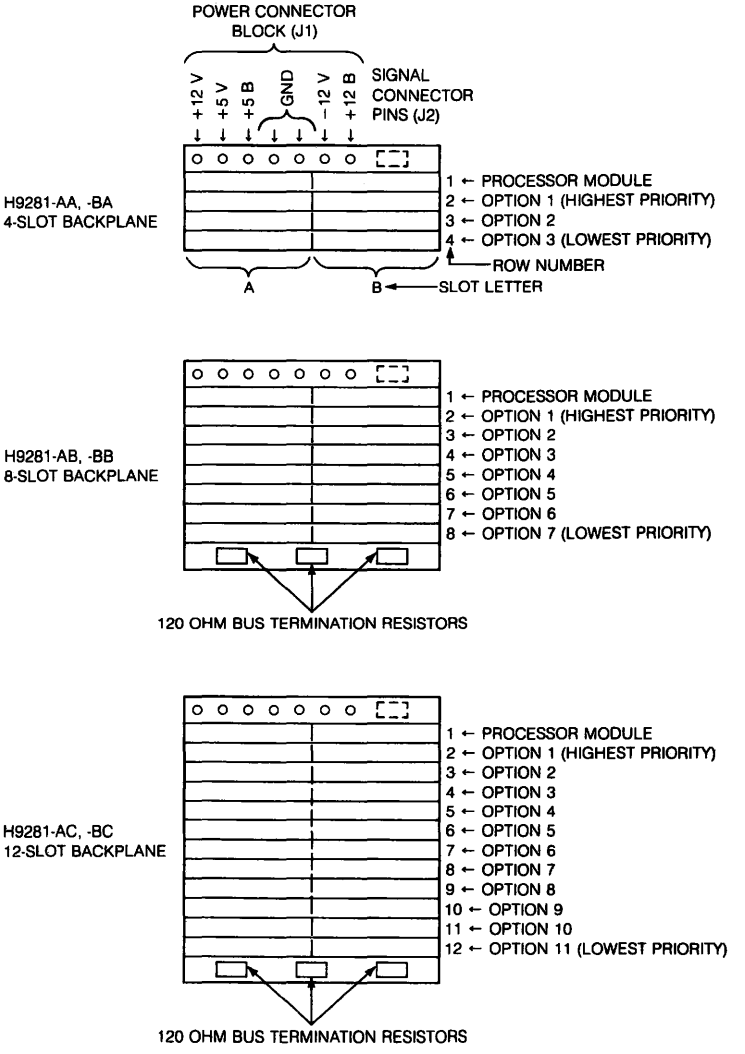


Figure 62-4 ▪ H9281-Q Option and Connector Locations (Module Side)

Table 62-1 ▪ 18- and 22-bit Jumper Configurations

Addressing	Jumper Connections
22-bit	M1 to M2 M4 to M5 M7 to M8 M10 to M11
18-bit*	M2 to M3 M5 to M6 M8 to M9 M11 to M12

* 18-bit addressing can also be configured by simply removing all jumpers from pins M1 through M12.

Chapter 63 ▪ TEV11 Terminator

The TEV11 terminator module provides 120-ohm termination circuits for 18-bit Q-bus systems, as shown in Figure 63-1.

▪ Specifications

Identification	M9400-YB
Size	Dual
Power Requirements	+5 Vdc ±5% at 0.54 A
Bus Loads	
ac	0
dc	0

▪ Related Documentation

Document Title	Order Number
TEV11 Field Maintenance Print Set	MP-00074-00

▪ Description

Each bus signal line terminates with two resistors that perform the voltage division, shown in Figure 63-2. These termination resistors are contained in a 16-pin, dual-in-line package that is identical to an IC package. Each package contains 14 termination pairs. The values used are shown in the figure. Daisychained grant signals are terminated and jumpered. BIAKI is jumpered to BIAKO and BDMGI is connected to BDMGO via factory-installed jumper W1.

Note

The TEV11 is not usable in a 22-bit system because address lines <18:21> are unterminated.

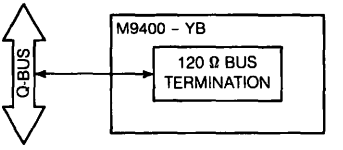


Figure 63-1 ▪ TEV11 Functions

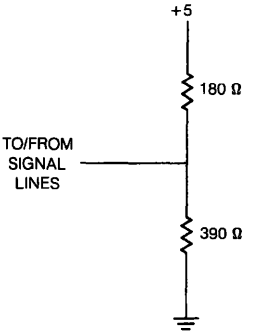


Figure 63-2 ▪ Typical 120-Ohm Bus Termination

Appendix A ▪ Chip Kits

The DCK11 series of LSI integrated circuits is available to Q-bus system users in sets called chip kits. The kits contain the ICs needed to build the foundation of nearly any Q-bus interface, and are available either with or without a Digital wirewrappable board and plug-in cable.

Chip kits minimize the chip count required to implement bus circuitry. This permits the designer to build an interface foundation on the dual-height wirewrappable board provided and still have ample room left for special circuitry. The comparatively small chip count results in backplane space savings, increased system reliability, lower system cost, and a greater opportunity for value to be added to the finished product.

Table A-1 lists the available chip kits. Kits DCK11-AA and DCK11-AC are intended for building the foundations of program control Q-bus interfaces. They are functionally similar to the DRV11-P bus foundation module. Kits DCK11-AB and DCK11-AD are intended for building the foundations of DMA Q-bus interfaces. They are functionally similar to the DRV11-B general purpose DMA interface module.

Table A-1 ▪ Q-bus Chip Kits

DCK11-AA	Program control bus interface chip kit, consisting of: (one) DC003 interrupt chip (one) DC004 protocol chip (four) DC005 transceiver/address decoder/vector select chips
DCK11-AC	Program control bus interface chip kit, consisting of: (one) DC003 interrupt chip (one) DC004 protocol chip (four) DC005 transceiver/address decoder/vector select chips (one) W9512 dual-height, extended-length, wirewrappable module (one) BC07D-10 ten-ft, 40-conductor plug-in cable

(continued on next page)

Table A-1 ▪ Q-bus Chip Kits (Cont.)

DCK11-AB	DMA bus interface chip kit, consisting of: (one) DC003 interrupt chip (one) DC004 protocol chip (four) DC005 transceiver/address decoder/vector select chips (two) DC006 word count/bus address chips (one) DC010 DMA control chip
DCK11-AD	DMA bus interface chip kit, consisting of: (one) DC003 interrupt chip (one) DC004 protocol chip (four) DC005 transceiver/address decoder/vector select chips (two) DC006 word count/bus address chips (one) DC010 DMA control chip (one) W9512 dual-height, extended-length, wirewrappable module (one) BC07D-10 ten-foot, 40-conductor plug-in cable

▪ DC003 Interrupt Chip

The DC003 interrupt chip is an 18-pin, 0.762 cm center × 2.349 cm long (maximum) (0.3 in center × 0.925 in long) dual-in-line-package (DIP) device that provides the circuits to perform an interrupt transaction in a computer system that uses a daisychain type of arbitration scheme. The device is used in peripheral interfaces to provide two interrupt channels labeled A and B, with the A section at a higher priority than the B section. Bus signals use high-impedance input circuits or high-current open-collector outputs, that allow the device to directly attach to the computer system bus. Maximum current required from the V_{cc} supply is 140 mA.

▪ DC004 Protocol Chip

The DC004 protocol chip is a 20-pin, 0.762 cm center × 2.74 cm long (0.3 in center × 1.08 in long) DIP device that functions as a register selector, providing the signals to control data flow into and out of up to four word registers (eight bytes). Bus signals can directly attach to the device because receivers and drivers are provided on the chip. An RC delay circuit is provided to slow the response of the peripheral interface to data transfer requests. The circuit is designed such that if tight tolerance is not required, then only an external 1K ±20 percent resistor is necessary. External RCs can be added to vary the delay. Maximum current required from the V_{cc} supply is 120 mA.

▪ DC005 Transceiver Chip

The 4-bit DC005 transceiver is a 20-pin, 0.762 cm center × 2.74 cm long (0.3 in center × 1.08 in long) DIP, low-power Schottky device; its primary use is in peripheral device interfaces to function as a bidirectional buffer between a data bus and a peripheral device logic bus. It also includes a comparison circuit for device address selection and a constant generator for interrupt vector address generation. The bus I/O port provides high-impedance inputs and high-drive (70 mA) open-collector outputs to allow direct connection to a computer data bus structure. On the peripheral device side, a bidirectional port is also provided, with standard TTL inputs and 20 mA, tristate drivers. Data on this port are the logical inversion of the data on the bus side.

Three address jumper inputs are used to compare against three bus inputs to generate the MATCH signal. The MATCH output is an open collector, allowing the output of several transceivers to be wire-ANDed to form a composite address match signal. The address jumpers can also be put into a third logical state that disables jumpers for "don't care" address bits. In addition to the three address jumper inputs, a fourth high-impedance input line is used to enable or disable the MATCH output.

Three vector jumper inputs are used to generate a constant that can be passed to the computer bus. The three inputs directly drive three of the bus lines, overriding the action of the control lines.

Two control signals are decoded to give three optional states — receive data, transmit data, and disable.

The maximum current required from the V_{cc} supply is 120 mA.

▪ DC006 Word Count/Bus Address Chip

The DC006 word count/bus address (WC/BA) chip is a 20-pin, 0.762 cm center × 2.74 cm long (0.3 in center × 1.08 in long) DIP, low-power Schottky device. Its primary use is in DMA peripheral device interfaces. This IC is designed to connect to the tristate side of the DC005 transceiver. The DC006 has two 8-bit binary up-counters, one for the word (or byte) count and another for the bus address. Two DC006 ICs can be cascaded to increase register implementation.

The chip is controlled by the address latch protocol chip (DC004), the DMA chip (DC010), and a minimum of ancillary logic. Both counters can be cleared simultaneously. Each counter is separately loaded by LD and the corresponding select line from the protocol chip. Each counter is incremented separately. The WC counter (word/byte counter) is always incremented by one; the BA counter (bus address) can be incremented by one or two for byte or word addressing, respectively.

Data from the DC006 IC is placed on the tristate bus via internal tristate drivers. Each counter is separately read by RD and the corresponding select line.

▪ DC010 Direct Memory Access Chip

The DC010 direct memory access (DMA) chip is a 20-pin, 0.762 cm center × 2.74 cm long (0.3 in center × 1.08 in long) DIP, low-power Schottky device primarily for use in DMA peripheral device interfaces using the Q-bus.

This device provides the logic to perform the handshaking operations required to request and to gain control of the system bus. Once bus mastership has been established, the DC010 generates the required signals to perform a DATI, DATO, or DATIO transfer as specified by control lines to the chip. The DC010 IC has a control line that will allow either multiple transfers or a maximum of four transfers to take place before giving up bus mastership.

▪ Related Documentation

Document Title	Order Number
Chipkit User's Manual	EK-01387-92

Appendix B ▪ System Configuration Concepts

The configuration of a Q-bus system is a stepwise process beginning with the definition of the application and ending with the selection of the required components and their final placement in the backplane. The purpose of the following discussion is to outline this configuration process, list the physical configuration rules, and then illustrate the process with an example. More information on configuring Q-bus systems, including summary charts on all Q-bus module products and configuration rules, is available in the *Microcomputer Products Configuration Guide* (order number EB-27318-68).

▪ Configuration Steps

The steps in configuring a Q-bus system are as follows:

1. Write the problem statement.

   Obtain as complete a description of the application as possible. In many cases, what is initially expected and what is finally configured are two totally different sets of hardware and software.

2. Make a block diagram of the application.

   This is done to identify *all* the connections to the system. Frequently, connections requiring an additional module are overlooked because of the minor role they play in the application. Identify all required connections in the beginning.

3. Determine the processing and software requirements.

   Determine the level of CPU performance required, including addressing capability, computational requirements, and throughput. What are the system software requirements? Is the application general purpose or is it a dedicated application? Is the application realtime-intensive? The answers to these questions will help in the selection of an operating environment and the necessary layered products.

4. Select the hardware products.

   From the block diagram, group common functions to facilitate the selection of hardware modules. It is useful to list the modules in tabular form, noting not only the module identification but the module size, power requirements (+5 V and +12 V, as well as the total power in watts), and bus loading (ac and dc loads per module).

5. Select the backplane and the power supply.

   Using the sizes listed in the module table, choose an appropriate backplane. Be aware of system addressing capabilities; if an 18- bit system is being configured that may potentially be upgraded to a 22-bit system in the future, be sure the existing system is compatible with 22-bit addressing. The module table also lists the power requirements of the system. Choose a power supply that is rated higher than apparently required. For reliable operation, the sum of all typical current requirements should be less than 70 percent of the maximum rated current of the power supply. This is not required, however.

6. Arrange the modules in the backplane.

   The way in which the components should be placed in the backplane is determined by a complex set of rules involving bus loading and termination. These rules are discussed in detail in the next section.

7. Determine the cables and cabinet kit needed.

▪ Configuration Rules

Q-bus systems can be divided into two categories — those that use only one backplane, and those that have multiple backplanes. Single backplane systems are viewed as lumped capacitance; the transmission line consists of only the etch run on the backplane and is terminated by the processor and (possibly) a terminator. Multiple backplane systems are regarded as transmission line systems, where the transmission line consists of the cables connecting the backplanes and etch runs are negligible. The transmission line in multiple backplane systems must be terminated at both ends. Capacitance affects both types of system.

The characteristics of single and multiple backplane systems differ enough to require separate sets of configuration rules. The rules are given in terms of power consumption, dc bus loading, and ac bus loading. dc loading is a measure of the leakage current a module's bus signal lines draw when high (undriven). One dc load is nominally 210 μA. ac loading is a measure of the capacitance a module adds to the bus signal lines. One ac load is 9.35 pF. Backplanes also add ac loading to the bus.

Configuring Single Backplane Systems

1. The bus can support up to 20 ac loads before additional termination is required. In general, the processor has onboard termination for one end of the bus; after 20 ac loads, the other end of the bus must be terminated with 120 ohms.
2. A terminated bus can support up to 35 ac loads.
3. The bus can support up to 20 dc loads.
4. The bus signal lines on the backplane can be up to 35.6 cm (14 in) long.

The preceding rules apply to single backplane systems only. The bus cannot be extended off the backplane in any way. If it is, the system is considered a multiple backplane system.

Configuring Multiple Backplane Systems

1. a) Up to three backplanes can be connected together.
   b) The signal lines on each backplane can be up to 254 cm (10 in) long.
2. Each backplane can have up to 22 ac loads. Unused ac loads from one backplane cannot be added to another backplane if the second backplane loading exceeds 22 ac loads. It is desirable to load backplanes equally or with the highest ac loads in the first and second backplanes.
3. Total dc loading of all three backplanes combined cannot exceed 20 loads.
4. Both ends of the transmission line must be terminated with 120 ohms. This means that the first backplane should have a termination of 120 ohms, and the last backplane should have a termination of 120 ohms.
5. a) The cable connecting the first two backplanes should be at least 1.83 meters (6 ft) long.
   b) The cable connecting the second backplane to the third backplane must be at least 1.22 meters (4 ft) longer or shorter than the cable connecting the first and second backplanes.
   c) The combined length of the cables should not exceed 4.88 meters (16 ft).
   d) The cables used must have a characteristic impedance of 120 ohms.

▪ Example

The following example demonstrates the configuration process outlined above.

Problem Statement

The application being developed is a medical lab analyzer. The sample being analyzed will be subjected to a series of light frequencies, and the intensity of the light will be measured after passing through the sample. The measured intensity will be presented as an analog value. The results of the test will be either stored in a local database, printed on an evaluation form, and/or loaded into a central facility database.

Block Diagram

The following block diagram can be drawn from the description given above:

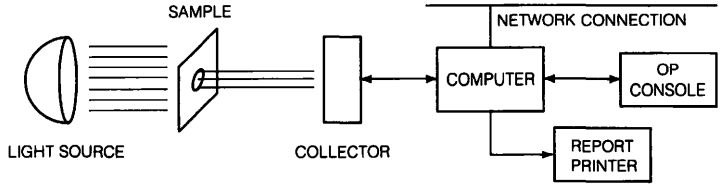


Figure B-1 ▪ Sample Block Diagram

Processing and Software Requirements

This is a dedicated application that must be able to manipulate a database, interface to a network, print reports, interface with an operator, interface to the light frequency collector, and analyze the collected data. Thus, the operating system must be multitasking. It is also undesirable for the operator (a noncomputer professional) to need to bootstrap the system.

The best software choice for this application is MicroPower/Pascal because it is a dedicated, multitasking operating system.

Because information is to be analyzed, floating-point capabilities are probably required for this application. Also, with many tasks resident in memory simultaneously, more than 64 Kbytes of memory are required, necessitating some form of memory management.

Hardware Product Selection

Using the block diagram above, the following modules are selected:

LSI-11/23 (KDF11-AA)	The LSI-11/73 also could have been chosen as the CPU, but the LSI-11/23 has the performance capabilities required.
KEF11-AA	Floating-point capabilities are required for analysis.
MSV11-LK	256 Kbytes are required for data manipulation, online storage of records, and network records.
MRV11-D	ROM memory option which is required for program storage.
DEQNA-M	Required to interface to the network (in this instance, Ethernet). If another network was being used, the appropriate device would be selected.
ADV11-C	Required as the light frequency interface. The block diagram indicates a need for four I/O channels. The ADV11-C can support up to eight differential lines or sixteen single-ended lines.
KWV11-C	The application must take analog samples at a rate that varies depending on the light frequency being sampled. This rate is in the kHz range and a clock is needed to trigger the samplings.
DLVJ1-M	Required for lines to the printer and to the console.

The size, power requirements, and bus loading are entered in the module table as follows:

			Bus Loads		Power	
Option	**+5 V**	**+12V**	**ac**	**dc**	**Watts**	**Size**
KDF11-AA*	2.0	0.2	2.0	1.0	12.4	Dual
MSV11-LK	3.0	0.0	2.0	0.5	15.0	Dual
MRV11-D	1.6	0.0	3.0	0.5	8.0	Dual
DEQNA-M	3.5	0.5	2.2	0.5	23.5	Dual
ADV11-C	2.0	0.0	1.3	1.0	10.0	Dual
KWV11-C	2.2	0.1	1.0	1.0	11.2	Dual
DLVJ1-M	1.0	0.25	1.0	1.0	8.0	Dual
Total	15.3	1.05	12.5	5.5	88.1	

* The KEF11-AA is installed.

Backplane and Power Supply

All the modules selected are dual-height modules and therefore can fit in the H9281 series backplanes. The user might also select an enclosure, such as the BA11-M. In this case, however, because the application is embedded intelligence, the dual-height form factor with a user-supplied power supply is the best choice.

Seven slots are needed. The H9281-QB has eight slots along with the cardcage to support the modules. This backplane uses 1.8 ac loads.

The configuration can support a 22-bit environment because all the modules and the backplane are compatible.

The total number of ac loads does not exceed 20. Therefore, no special termination is needed. Note, however, that the H9281-QB has termination built into it and therefore could support up to 35 ac loads.

The modules are placed in the backplane as follows:

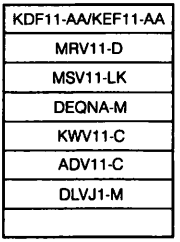


Figure B-2 ▪ Modules in Backplane

Note

Note that the DMA devices (DEQNA) should be placed closer to the processor than the interrupt devices (KMV11, ADV11, DLVJ1). Since the DLVJ1 is needed for slow operation (printing) it is placed near the end of the bus. In general, the order is: processor, memory, DMA/interrupt, interrupt-only, non-DMA/non-interrupt. The placement of DMA/interrupt and interrupt-only devices is dependent on use and critical processor service.

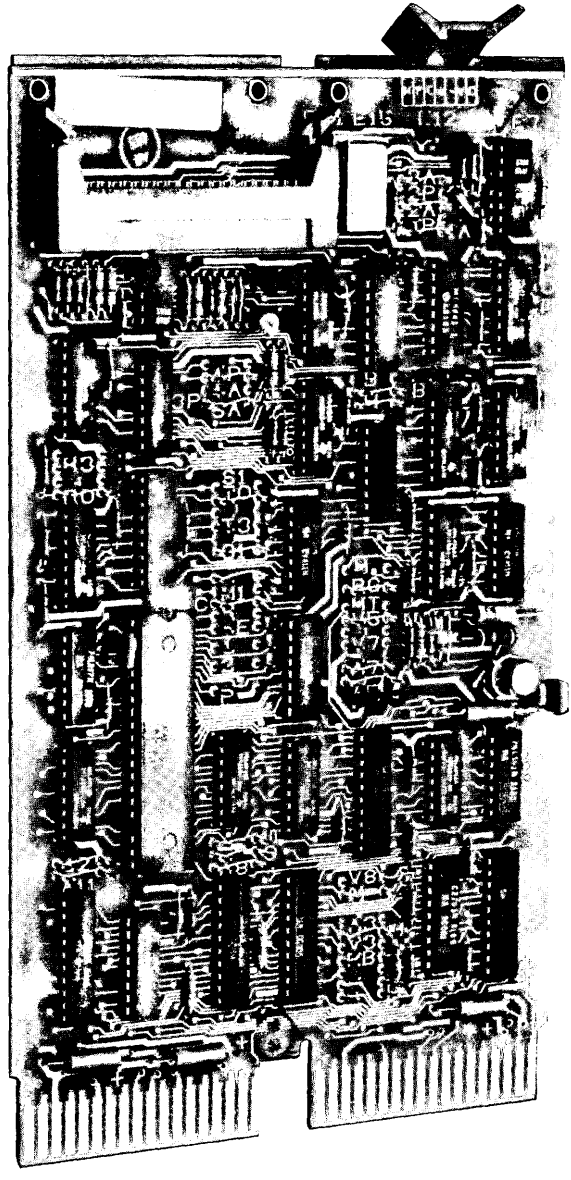
Cables and Cabinet Kit

The system is a single backplane system so no expansion cables are required. The following device cables are required:

- BC20N-05 (device cable) to connect the DLVJ1-M and the printer
- BC20N-05 (device cable) to connect the DLVJ1-M and the console
- BNE3C (transceiver cable) to connect the DEQNA-M and the H4000 transceiver

An H4000 transceiver is also needed to hook up the actual Ethernet cable.

Since the modules are being installed in a stand-alone backplane, the user is responsible for ensuring that the entire system is FCC-compliant. Therefore, no FCC cabinet kits are needed. However, a CK-DEQNA-KA cabinet kit is used to permit the correct electrical hookup to the BNE3C transceiver cable.



Appendix C ▪ Mature Q-bus Products

Appendix C describes those mature Q-bus products that Digital no longer actively markets. These products are divided into two types — first, those which are still available for maintenance purposes rather than design purposes, and second, those which are obsolete and have been replaced by newer products. Specification and configuration details are provided on the maintenance products as a service to the many Digital customers who currently have and use these products.

▪ Maintenance Products

Among the maintenance products included here are: BDV11 Diagnostic/Bootstrap Terminator, DLV11-F Asynchronous Line Interface, KD11-HA LSI-11/2 Microcomputer, and VT103 LSI-11 Video Terminal.

▪ BDV11 Diagnostic, Bootstrap, Terminator

The BDV11 module has 2 Kwords of read-only memory (ROM) that contains both diagnostic programs and bootstrap programs. These programs are user-selectable by setting dip switches. The diagnostic programs test the processor, the memory, and the user's console. The bootstrap programs are used to boot a number of LSI-11 compatible peripherals. The module also contains 120-ohm bus terminator circuits.

Space is available on the module to allow the user to add up to 2 Kwords of erasable programmable ROM (EPROM) and up to 16 Kwords of ROM.

Specifications

Identification	M8012
Size	Quad
Power Requirements	+5 Vdc ±5% at 1.6 A +12 Vdc ±3% at 0.07 A
Bus Loads	
ac	2
dc	0.5

Related Documentation

Document Title	**Order Number**
BDV11 Bus Terminator, Bootstrap, Diagnostic ROM Technical Manual	EK-BDV11-TM
Field Maintenance Print Set	MP-00489-00
BDV11 Bootstrap Documentation Kit	ZJ254-RZ

Configuration

The BDV11 is factory-configured by Digital to let the user expand the diagnostic and bootstrap programs by adding 2 Kwords of EPROM and 16 Kwords of ROM/EPROM memory. Users can modify the configuration for their own software requirements. Thirteen jumpers wires and four switch packs are located on the module as shown in Figure C-1. Eight jumpers are used for selecting sockets, and five are used to accommodate various types of memory chips. The switches are used to select programs.

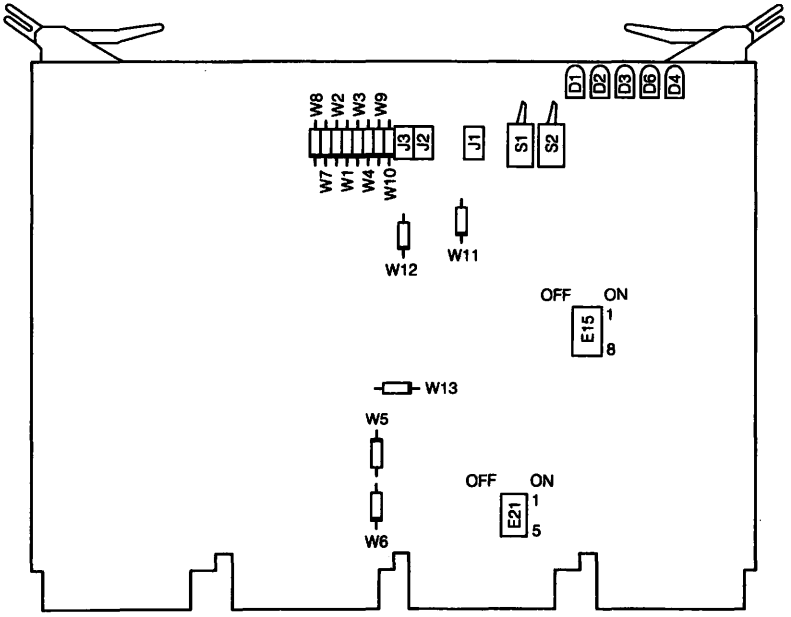


Figure C-1 ▪ BDV11 Switch and Jumper Locations

- SOCKET SELECTION
  The socket selection logic is controlled by jumpers W1-W4 and W9-W12, which can be configured in seven different ways, designated A through G. Group A assigns the PCR pages and socket selections. Groups B through G let the user choose where to begin program execution.

- MEMORY CONFIGURATION
  The user can change the configuration of the BDV11 memory structure by using socket selection jumpers W1-W4 and W9-W12. The standard configuration is given in Table C-1. This table also indicates the installation order for the PROM/ROM chips. The B through G configurations show as alternate ways the user can map the ROM memory. Details about selecting a configuration using the socket selection jumpers are given in Table C-2.

Table C-1 • BDV11 Memory Configurations

Socket Byte High	Byte Low	Configuration Design	ROM Address	PCR Page	Selection Signal
		4K Diagnostic/Bootstrap (Digital)			
E53	E48	A	0-2K	0-17	SB1 L
(2)	(1)	B	4K-6K	40-57	SB1 L
		C	16K-18K	200-217	SB1 L
		D	20K-22K	240-257	SB1 L
E58	E44	A	2K-4K	20-37	SB2 L
(4)	(3)	B	6K-8K	60-77	SB2 L
		C	18K-20K	220-237	SB2 L
		D	22K-24K	260-277	SB2 L

(continued on next page)

Table C-1 ▪ BDV11 Memory Configurations (Cont.)

Socket Byte High	Socket Byte Low	Configuration Design	ROM Address	PCR Page	Selection Signal
		2K User EPROM			
E57	E40	A	4K-5K	40-47	SE1 L
(3)	(1)	B	0-1K	0-7	SE1 L
		C	20K-21K	240-247	SE1 L
		D	16K-17K	200-207	SE1 L
E52	E36	A	5K-6K	50-57	SE2 L
(4)	(2)	B	1K-2K	10-17	SE2 L
		C	21K-22K	250-257	SE2 L
		D	17K-18K	210-217	SE2 L
		16K User ROM			
E54	E49	A	16K-18K	200-217	SP8 L
(2)	(1)	E	16K-17K	200-207	SP8 L
		F	0-2K	0-17	SP8 L
		G	0-1K	0-7	SP8 L
E59	E45	A	18K-20K	220-237	SP7 L
(4)	(3)	E	18K-19K	220-227	SP7 L
		F	2K-4K	20-37	SP7 L
		G	2K-3K	20-27	SP7 L
E60	E41	A	20K-22K	240-257	SP6 L
(6)	(5)	E	20K-21K	240-247	SP6 L
		F	4K-6K	40-57	SP6 L
		G	4K-5K	40-47	SP6 L
E55	E37	A	22K-24K	260-277	SP5 L
(8)	(7)	E	22K-23K	260-267	SP5 L
		F	6K-8K	60-77	SP5 L
		G	6K-7K	60-67	SP5 L
E51	E38	A	24K-26K	300-317	SP4 L
(10)	(9)	E	17K-18K	210-217	SP4 L
		F	8K-10K	100-117	SP4 L
		G	1K-2K	10-17	SP4 L
E47	E42	A	26K-28K	320-337	SP3 L
(12)	(11)	E	19K-20K	230-237	SP3 L
		F	10K-12K	120-137	SP3 L
		G	3K-4K	30-37	SP3 L

(continued on next page)

Table C-1 ▪ BDV11 Memory Configurations (Cont.)

Socket Byte High	Socket Byte Low	Configuration Design	ROM Address	PCR Page	Selection Signal
E43	E46	A	28K-30K	340-357	SP2 L
(14)	(13)	E	21K-22K	250-257	SP2 L
		F	12K-14K	140-157	SP2 L
		G	5K-6K	50-57	SP2 L
E39	E50	A	30K-32K	360-377	SP1 L
(16)	(15)	E	23K-24K	270-277	SP1 L
		F	14K-16K	160-177	SP1 L
		G	7K-8K	70-77	SP1 L

Note

The numbers in parentheses in the socket columns indicate the order for installing each ROM.

Table C-2 ▪ Socket Selection Jumper Configurations

Configuration Design	Jumper Configurations W1	W2	W3	W4	W9	W10	W11	W12
A	R	I	I	R	I	R	R	I
B	X	X	X	X	I	R	I	R
C	X	X	X	X	R	I	R	I
D	X	X	X	X	R	I	I	R
E	I	R	I	R	X	X	X	X
F	R	I	R	I	X	X	X	X
G	I	R	R	I	X	X	X	X

I = installed; R = removed; X = don't care

- CHIP SELECTION

The system ROM sockets can be occupied by either 2K ROMs or 1K ROMs. The ROM socket logic uses jumpers W5-W8 and W13 to select the type of ROM that can be used on the BDV11. Table C-3 shows jumper configurations and the type of ROM or PROM used with these configurations.

Table C-3 ▪ BDV11 Chip Selection Jumpers

	Jumper Configuration				
ROM Type	**W5**	**W6**	**W7**	**W8**	**W13**
2708 (1)	R	I	R	I	R
2716 (2)	R	R	I	R	I
8316E (3)	I	R	I	R	R
8316E (4)	R	R	I	R	I

I = installed; R = removed

Notes

1. CB2 and DB2 must be supplied with external −5 V power.
2. Use only +5 Vdc type components.
3. Chip select signals must be programmed as follows:

CS1	CS2	CS3
LOW	LOW	LOW

4. Chip select signals must be programmed as follows:

CS1	CS2	CS3
LOW	LOW	HIGH

- DIAGNOSTIC/BOOTSTRAP SWITCHES

Dip switchpacks E15 and E21 let the user select diagnostic programs and/or a bootstrap program. The eight switches of E15 are designated A1-A8, and the four switches of E21 are designated B1-B4. The programs selected by these switches are listed in Table C-4.

Table C-4 ▪ BDV11 Diagnostic/Bootstrap Switches

Switch	Status	Program Selected
A1	ON	Execute CPU test upon powerup or restart
A2	ON	Execute memory test upon powerup or restart
A3	ON	DECnet boot (A4, A5, A6 and A7 are arguments as follows:

Boot	A4	A5	A6	A7
DUV11	ON	OFF	OFF	OFF
DLVE1	OFF	ON	OFF	OFF
DLV11-F	OFF	ON	OFF	ON

A4	ON	Console test and dialogue (A3 OFF)
A4	OFF	Turnkey boot dispatched by switch setting, as listed in Table C-5 (A3 OFF)

All boots other than the DECnet boots above are controlled by the bit patterns in switches A5-A8 and B1 (as listed in Table C-5) or, if the console test is selected, by mnemonic and unit number.

Table C-5 ▪ Non-DECnet Boot Selection

Mnemonic	A5	A6	A7	A8	B1	Program Selected
	OFF	OFF	OFF	OFF	ON	Loop on test
DKn; n<8	OFF	OFF	OFF	ON	OFF	RKV11 Boot
DLn; n<4	OFF	OFF	ON	OFF	OFF	RLV11 Boot
DXn; n<2	OFF	ON	OFF	OFF	OFF	RXV11 Boot
DYn; n<2	OFF	ON	ON	OFF	OFF	RXV21 Boot
	ON	OFF	OFF	OFF	OFF	ROM Boot

Note

All unused patterns and mnemonics default to ROM boot if switch B2, B3, or B4 is on.

The ROM boot uses switches B2, B3, and B4 to dispatch as listed in Table C-6.

Table C-6 ▪ BDV11 ROM Boot Switches

B2	B3	B4	ROM
ON	X	X	Extended diagnostic
OFF	ON	X	2708
OFF	OFF	ON	Program ROM

X = don't care

If an unrecognized mnemonic or switch setting (A5 through B1) is encountered, B2, B3, and B4 are checked for the presence of additional ROM. If present, the ROM boot is invoked. If no additional ROM exists, the switch-checking routine will halt or the mnemonic routine will reprompt.

- BEVNT SWITCH
  Contact 5 of dip-socket switch E21 is the BEVNT switch. When the switch is OFF (open), the Q-bus BEVNT signal can be controlled by the power supply generated LTC signal. When the switch is ON (closed), the LTC function is program-controlled.

- HALT/ENABLE SWITCH
  When this switch is in the ENABLE position, the processor can operate under program control. If the switch is placed in the HALT position, the processor enters the halt mode and responds to console ODT commands. While in the halt mode, the processor can execute single instructions for system maintenance.

- RESTART SWITCH
  When the RESTART switch is cycled (i.e., moved from one side to the other and back), the CPU automatically carries out a powerup sequence. Thus, for maintenance purposes, the system can be rebooted at any time.

▪ DLV11-F Asynchronous Line Interface

The DLV11-F asynchronous line interface module interfaces the Q-bus to any of several standard types of serial communications lines. It supports either 20 mA current loop or EIA-standard lines, but does not include modem control.

Specifications

Identification	M8028
Size	Dual
Power Requirements	+5 Vdc ±5% at 1.0 A +12 Vdc ±3% at 0.18 A
Bus Loads	
ac	2.2
dc	1.0

Related Documentation

Document Title	Order Number
DLV11-E and DLV11-F Asynchronous Line Interface User's Manual	EK-DLV11-OP
Field Maintenance Print Set	MP-00461-00
DLV11-F Diagnostic Documentation Kit	ZJ255-RZ

Configuration

The following items are user-selectable on the DLV11-F asynchronous line interface:

- Register addresses
- Interrupt vector address
- Data format
- Baud rate
- Interface mode

The user configures these items by installing and/or removing jumper wires between the wirewrap pins. The locations of the DLV11-F jumpers are shown in Figure C-2. A complete listing of the jumpers, their functions, and their factory configurations are given in Table C-7.

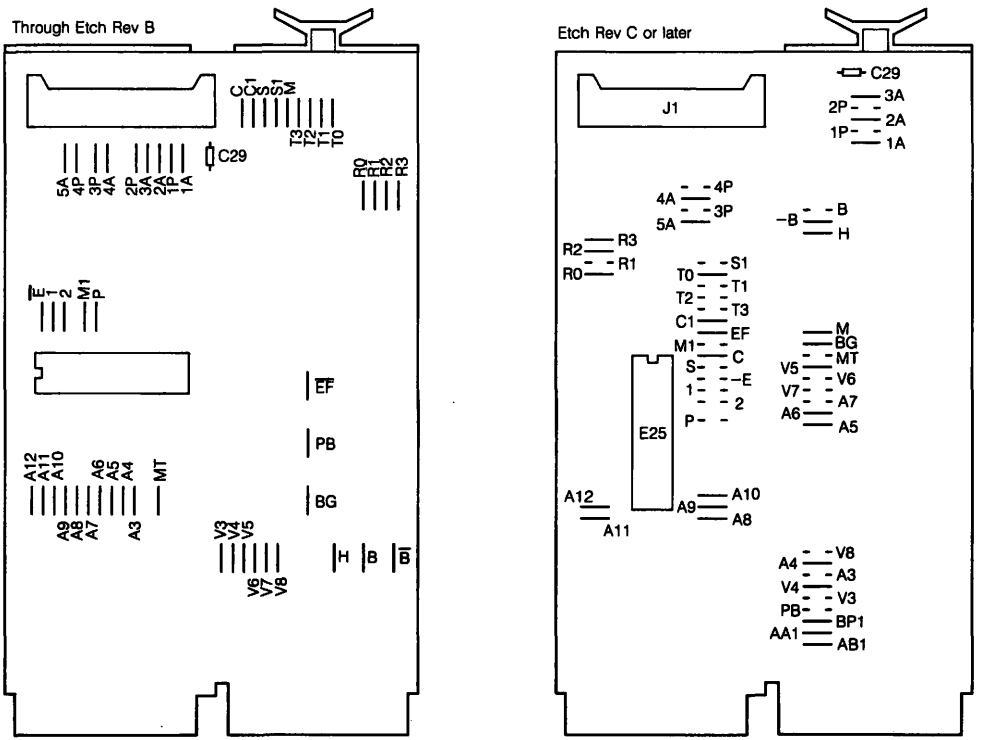


Figure C-2 ■ DLV11-F Jumper Locations

Table C-7 ▪ DLV11-F Jumper Definitions

Note

Jumpers are inserted to enable the function they control except for those jumpers which indicate negation (such as -B and E). Negated jumpers are removed to enable the functions they control.

Jumper	Function
A3-A12	These jumpers correspond to bits 3 through 12 of the address word. When inserted, they will cause the bus interface to check for a true condition on the corresponding address bit. Factory-configured for an address of 177560.
V3-V8	These jumpers are used to generate the vector during an interrupt transaction. Each inserted jumper will assert the corresponding vector bit on the Q-bus. Factory-configured for a receiver vector address of 60 and a transmitter vector address of 64.
R0-R3	These jumpers are used to select receiver and transmitter baud rates during common speed operation. During split speed operation, they are used for selection of receiver-only baud rate as defined in Table C-9. They are factory-configured for a baud rate of 110.
T0-T3	These jumpers are used to select transmitter baud rate during split speed operation. They are used for both receiver and transmitter baud rate selection if maintenance mode is entered during split speed operation, as defined in Table C-9. They are factory-configured for a baud rate of 9600.
BG	Jumper is inserted to enable break generation. Factory-inserted.
P	Jumper is inserted for operation with parity. Factory-removed.
E	Jumper is removed for even parity; inserted for odd parity. Factory-removed.

(continued on next page)

Table C-7 ▪ DLV11-F Jumper Definitions (Cont.)

Jumper	Function
1, 2	These jumpers select the desired number of data bits, as defined in Table C-10. Factory-configured for 8 data bits/character.
PB	Jumper is inserted to enable the programmable baud rate capability. Factory-removed.
C, C1	These jumpers are inserted for common speed operation. (Note that S and S1 must be removed when C and C1 are inserted.) Both jumpers are factory- inserted.
S, S1	Inserted for split speed operation. (Note that C and C1 must be removed when S and S1 are inserted.) Both jumpers are factory-removed.
H	This jumper is inserted to assert BHALT when a framing error is received, except when the maintenance bit is set. This places the processor in the halt mode. The jumper is factory-inserted.
B, −B	Jumper B is inserted to negate BDCOK when a break signal or framing error is received, except when the maintenance bit is set. This causes the processor to reboot. (Jumper −B must be removed when B is inserted.) Jumper B is factory-removed; jumper −B is factory-inserted.
1A, 2A, 3A	These three jumpers are inserted to make the 20 mA current loop receiver active. (Jumpers 1P and 2P must be removed when 1A, 2A, and 3A are inserted.) Jumpers are factory-inserted.
1P, 2P	These jumpers are inserted to make the 20 mA current loop receiver passive. (Jumpers 1A, 2A and 3A must be removed when 1P and 2P are inserted.) Jumpers are factory-removed.

(continued on next page)

Table C-7 ▪ DLV11-F Jumper Definitions (Cont.)

Jumper	Function
4A, 5A	These jumpers are inserted to make the 20 mA current loop transmitter active. (Jumpers 3P and 4P must be removed when 4A and 5A are inserted.) Jumpers are factory-inserted.
3P, 4P	These jumpers are inserted to make the 20 mA current loop transmitter passive. (Jumpers 4A and 5A must be removed when 3P and 4P are inserted.) Jumpers are factory-removed.
EF	Jumper is removed to enable the error flags to be read in the high byte of the receiver buffer. Factory-inserted.
M, M1	These are test jumpers used during the manufacture of the module. They are not defined for field use.

- REGISTER ADDRESSES

Register addresses for the DLV11-F can range from 160000 to 177770. Because each module has four registers, each requires four contiguous addresses. Table C-8 lists the registers along with their standard factory-configured addesses.

The low-order three bits of each address indicate the individual register within the register set. Bits <3:12> are jumper-selected as illustrated in Figure C-3, using jumpers A3 through A12.

Addresses 177560 through 177566 are reserved for the module used with the console peripheral device. Additional modules should be assigned addresses from 176500 through 176670, allowing up to 30 additional DLV11-F modules to be addressed.

Table C-8 ▪ DLV11-F Standard Address Assignments

Description	Mnemonic	Console Module	Second Module
Registers:			
Receiver Control and Status	RCSR (R/W)	177560	176500
Receiver Data Buffer	RBUF (R-O)	177562	176502
Transmit Control and Status	XCSR (R/W)	177564	176504
Transmit Data Buffer	XBUF (W-O)	177566	176506
Interrupts:			
Receiver		60	300
Transmitter		64	304

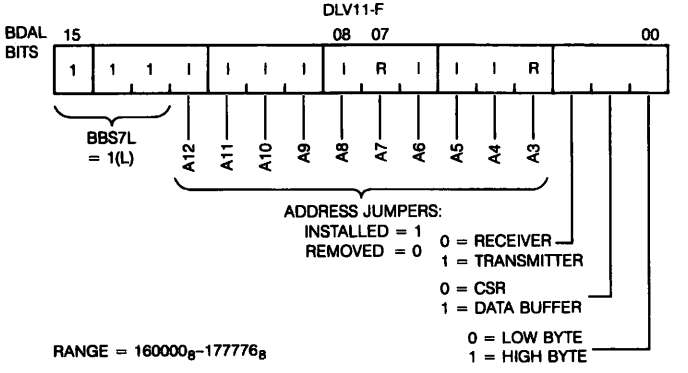


Figure C-3 ▪ DLV11-F Address Selection

- INTERRUPT VECTORS

  The interrupt vectors are selected by using jumpers V3 to V8. The standard configuration is shown in Figure C-4 and Table C-8. The vectors can range from 001 through 774. Note that vectors 60 and 64 are reserved for the console device. Additional DLV11-F modules should be assigned vectors following any DRV11 parallel interface modules installed in the system that start at address 300.

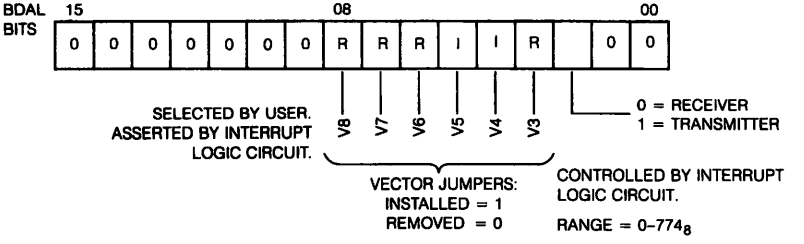


Figure C-4 ▪ DLV11-F Interrupt Vector Selection

- BAUD RATE SELECTION

The DLV11-F allows the user to configure jumpers T0-T3 and R0-R3 for the transmit baud rate and the receiver baud rate, as shown in Table C-9.

Table C-9 ▪ DLV11-F Baud Rate Selection

R3 T3	R2 T2	R1 T1	R0 T0	Baud Rate
I	I	I	I	50
I	I	I	R	75
I	I	R	I	110
I	I	R	R	134.5
I	R	I	I	150
I	R	I	R	300
I	R	R	I	600
I	R	R	R	1200
R	I	I	I	1800
R	I	I	R	2000
R	I	R	I	2400
R	I	R	R	3600
R	R	I	I	4800
R	R	I	R	7200
R	R	R	I	9600
R	R	R	R	19200

I = jumper installed; R = jumper removed

- DATA BIT SELECTION

The number of data bits being transmitted or received by the DLV11-F is user-selectable by installing or removing jumpers 1 and 2. The specific number of data bits, as controlled by the configuration of jumpers 1 and 2, is shown in Table C-10

Table C-10 ▪ DLV11-F Data Bit Selection

Jumper 2	Jumper 1	Number of Data Bits
I	I	5
I	R	6
R	I	7
R	R	8

Cables

Before installing the DLV11-F on the backplane, first establish the desired priority level to determine in which backplane slot to install the module. Then ensure that the module configuration jumpers are configured correctly for your application. Connection to the peripheral device is via an optional data interface cable. Cables are listed below.

Application	Cable Type*
EIA Interface	BC01V-X or BC05C-X modem cable
20 mA Current Loop	BC05M-X cable assembly

* X = Length in feet. Standard length is 25 feet.

- INTERFACING EIA-COMPATIBLE DEVICES

The DLV11-F supports only the data leads of EIA-compatible devices. It uses a BC05C modem cable to interface devices such as the Teletype Model 37 Teletypewriter and the Bell Data Set Model 103 (in auto mode).

- INTERFACING 20 MA CURRENT LOOP DEVICES WITH THE DLV11-F

When interfacing with 20 mA current loop devices, the BC05M cable assembly provides the correct connections to the 40-pin connector on the DLV11-F. The peripheral device end of the cable is terminated with a Mate-N-Lok connector that is pin-compatible with all Digital 20 mA serial interface terminals.

Note

When the DLV11-F is used with teletypewriter devices, a 0.005 F capacitor must be installed.

▪ KD11-HA LSI-11/2 Microcomputer

The LSI-11/2 (KD11-HA) is a 16-bit microcomputer on a dual-height module with no onboard memory.

Specifications

Identification	M7270
Size	Dual
Power Requirements	+5 V ±5% at 1.0 A +12 V ±5% at 0.22 A
Bus Loads	
ac	1.7
dc	1.0
Interrupt Latency	35.05 microseconds ±20% (worst case if KEV11 option is not present) 44.1 microseconds ±20% (worst case if KEV11 option is present)
DMA Latency	6.45 microseconds ±20% (worst case)

Related Documentation

Document Title	Order Number
LSI-11/2 Processor Configuration Sheet	EK-KD1HA-CG
LSI-11/2 Central Processor (KD11-HA)	ED-18323-53

Configuration

Every LSI-11/2 processor module is factory-configured to perform specific functions. For many applications, the module can be used as received. Wirewrap posts are provided on each module for configuring jumper-selectable functions. Processor functions can be altered by installing or removing these jumpers. Figure C-5 shows the location of the jumpers on the module. Table C-11 lists the jumpers, their functions, and their factory configuration.

Processor module etch revisions can be determined by examining the printed circuitboard part number on side 2 (solder side) of the processor module.

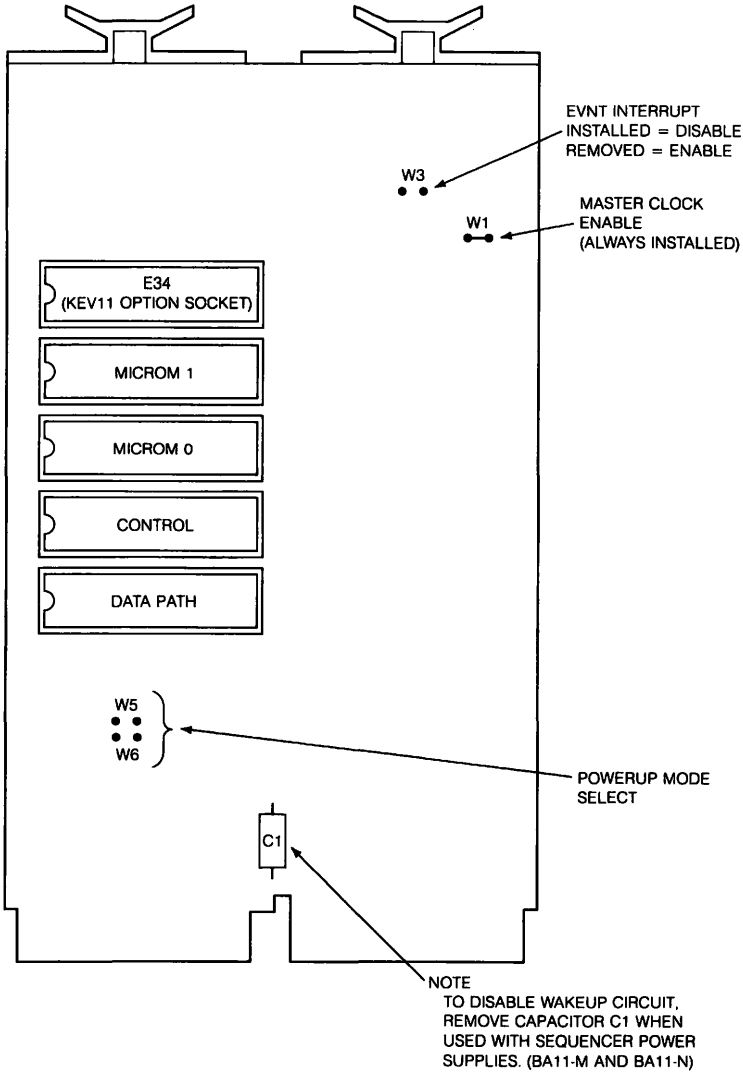


Figure C-5 ▪ LSI-11/2 Jumper Locations

Table C-11 ▪ LSI-11/2 Jumpers

Jumper	Function
W1	This jumper is the master clock enable. It must always be installed.
W3	This jumper controls linetime clock (LTC) and external event (BEVNT) interrupts. When the jumper is removed, LTC or BEVNT interrupts are enabled; when the jumper is installed, they are disabled. The module is factory-configured with W3 removed.
W5 W6	These two jumpers select the powerup mode of the processor. The jumper configurations for the four modes are listed in Table C-12. The module is factory-configured for mode 0.

Note

The M7270 module does not have jumpers W2 and W4.

Table C-12 ▪ LSI-11/2 Powerup Jumpers

Mode	W6	W5	Description
0	R	R	PC @24 and PS @26 or halt mode
1	R	I	ODT microcode
2	I	R	PC @173000 for user bootstrap
3	I	I	Special processor microcode (not implemented)

▪ VT103 LSI-11 Video Terminal

The VT103 is a video terminal that features an internal 18-bit Q-bus backplane, permitting the user to configure an LSI-11 microcomputer system directly within the terminal. The VT103 consists of three basic pieces:

- Video terminal, consisting of a video monitor, terminal controller, detachable keyboard, and monitor cabinet
- LSI-11 support hardware, consisting of a 4 × 4 Q-bus backplane assembly and an H7835 power supply. The backplane can accommodate eight dual-height or four quad-height modules.
- Optional TU58 DECtape II

Specifications

Physical Characteristics	
Monitor	
Height	36.83 cm (14.5 in)
Width	45.72 cm (18 in)
Depth	36.20 cm (14.25 in)
Weight	15 kg (33 lb)
Keyboard	
Height	8.89 cm (3.5 in)
Width	45.72 cm (18 in)
Depth	20.32 cm (8 in)
Weight	2.0 kg (4.5 lb)
Nonstandard Environmental Specifications (Without TU58)	
Operating	
Temperature	5°C to 40°C (41° to 104°F)
Altitude	2.4 km (8,000 ft)
Nonoperating	
Altitude	9.1 km (30,000 ft)
Power	
Line Voltage	90-128 V rms single phase, two-wire 180-256 V rms single phase, two-wire (switch-selectable)
Line frequency	47-63 Hz
Current	4.0 A rms maximum at 115 V rms 2.0 A rms maximum at 230 V rms
Input power	250 VA apparent, 300 W maximum
Power Supply Output	+5 Vdc at 16.0 A +12 Vdc at 5.0 A -12 Vdc at 0.50 A -23 Vdc at 0.01 A Convection cooled Power OK signals (BPOK and BDCOK) and linetime clock signal to backplane

Related Documentation

Document Title	Order Number
VT103 LSI-11 Video Terminal Users Guide	EK-VT103-UG
VT100 Series Technical Manual	EK-VT100-TM
VT100 Series Pocket Service Guide	EK-VT100-J1
VT103 Illustrated Parts Breakdown	EK-VT103-IP
VT100 Illustrated Parts Breakdown	EK-VT100-IP
VT100 Print Set (base terminal)	MP-00663
VT103 Print Set (supplement)	MP-00731

Configuration

The VT103 backplane assembly has five jumpers, as shown in Figure C-6. Only one of these (W4) is user-configurable. With W4 installed, the linetime clock (LTC) is enabled. Be sure your system needs this LTC clock before installing W4.

The remaining four jumpers should not be changed from their factory configuration. W1, W2, and W5 are installed at the factory; W3 is removed at the factory.

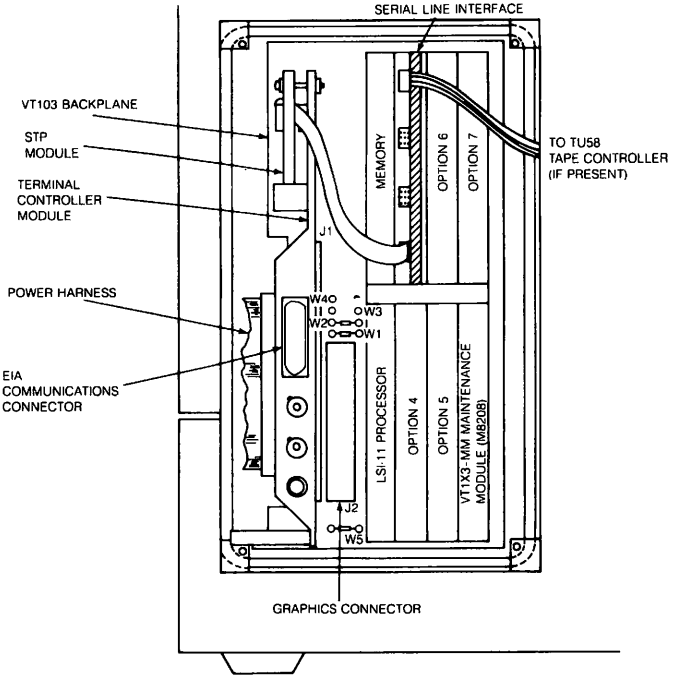


Figure C-6 ▪ VT103 Backplane

Cables and Connectors

The standard terminal port (STP), included with the VT103, has three EIA connectors.

Two 10-pin connectors are for installing cables (supplied) to serial line interfaces such as a DLVJ1 four-channel serial line interface or an MXV11-A multifunction memory and serial in/out module.

The one 40-pin Berg connector is for installing a cable (not supplied) to serial line units that also have a Berg connector, such as a DLVE1 asynchronous line interface or a DUV11 synchronous line interface.

▪ Obsolete or Replaced Products

Most of the following Q-bus products have been replaced or superseded by more current products, as described below. If you need more information on them, refer to the appropriate user documentation listed.

▪ AAV11-A Digital-to-Analog Converter

The AAV11-A is a four-channel, digital-to-analog converter module that includes control and interfacing circuits. Each channel has its own holding register that can be addressed separately and provides 12 bits of resolution.

The AAV11-A has been replaced by the AAV11-C.

Related Documentation

Document Title	Order Number
ADV11-A, KWV11-A, AAV11-A, DRV11 User's Manual	EK-ADV11-OP
AAV11-A Field Maintenance Print Set	MP-00186-00
AAV11 Diagnostic Documentation Kit	ZJ248-RZ

▪ ADV11-A Analog-to-Digital Converter

The ADV11-A is a 12-bit successive approximation analog-to-digital converter that samples analog data at specified rates and stores the digital equivalent value for processing. A multiplexer section can accommodate up to 16 single-ended or 8 quasi-differential inputs.

The ADV11-A has been replaced by the ADV11-C.

Related Documentation

Document Title	Order Number
ADV11-A, KWV11-AA, AAV11-A, DRV11 User's Manual	EK-ADV11-OP
ADV11-A Field Maintenance Print Set	MP-00193-00
ADV11 Diagnostic Documentation Kit	ZJ250-RZ

▪ DRV11-B Direct Memory Access Interface

The DRV11-B is a general purpose direct memory access (DMA) interface used to transfer data directly between the LSI-11 system memory and an I/O device. The interface is programmed by the processor to move variable length blocks of 8- or 16-bit data to or from specified locations in memory by means of the Q-bus.

The DRV11-B has been replaced by the DRV11-WA.

Related Documentation

Document Title	Order Number
DRV11-B General Purpose DMA Interface User's Manual	EK-DRV1B-OP-001
DRV11-B Field Maintenance Print Set	MP-00160-00
DRV11 Diagnostic Documentation Kit	ZJ244-RZ

▪ KD11-F LSI-11 Microcomputer

The KD11-F LSI-11 is a 16-bit microcomputer with the speed and instruction set of a minicomputer. It controls the time allocation of the Q-bus for peripherals and performs arithmetic and logic operations, along with instruction decoding.

The KD11-F was the first of the LSI-11 family of microcomputers and has been superseded by several, more advanced microcomputer models.

Related Documentation

Document Title	Order Number
LSI-11 PDP-11/03 User Manual	EK-LSI11-TM
LSI-11 System Service Manual	EK-LSIFS-SV
LSI-11 The Complete Family Brochure	ED-18647-18
LSI-11 PDP-11/03 Maintenance Card	EK-LSI11-MC
LSI-11 PDP-11/03 Reference Card	EH-07043-53

▪ KPV11 Powerfail/Linetime Clock/Terminator Option

The KPV11 is a Q-bus power-fail/linetime clock (LTC) terminator option. Three versions of the KPV11 were available:

- KPV11-A, with powerfail and LTC functions only
- KPV11-B, with 120-ohm bus terminations in addition to powerfail and LTC functions
- KPV11-C, with 220-ohm bus terminations in addition to powerfail and LTC functions

The KPV11 has been phased out because the functions it performed are now available on a variety of other modules.

Related Documentation

Document Title	Order Number
KPV11 Field Maintenance Print Set	MP-00356-00

▪ KWV11-A Programmable Realtime Clock

The KWV11-A is a programmable clock/counter that provides a variety of methods for determining time intervals and counting events. It can be used to generate interrupts to the processor at predetermined intervals, or to synchronize the processor ratios between input and output events. It can also be used to start the ADV11-A analog-to-digital converter either by clock counter overflow or by the firing of a Schmitt trigger.

The KWV11-A has been replaced by the KWV11-C.

Related Documentation

Document Title	Order Number
ADV11-A, KWV11-A, AAV11-A, DRV11 User's Manual	EK-ADV11-OP
KWV11-A Field Maintenance Print Set	MP-00200-00
KWV11 Diagnostic Documentation Kit	ZJ247-RZ

▪ KXT11-AA Falcon SBC-11/21 Microcomputer

The KXT11-AA Falcon SBC-11/21 is a single-board microcomputer containing the Digital-designed 16-bit Micro/T-11 Microprocessor Unit (MPU), 4 Kbytes of RAM, up to 32 Kbytes of ROM, two asynchronous serial line units with programmable baud rates, and 24 lines of programmable parallel I/O — all packaged on one dual-height board.

The KXT11-AA has been superseded by the KXT11-AB Falcon SBC-11/21 Plus.

Related Documentation

Document Title	Order Number
KXT11-AA Configuration Guide	EK-KXT11-CG
M8063 Falcon SBC-11/21 Single-Board Computer User's Guide (Revision C)	EK-KXT11-UG
SBC-11/21 Single-Board Computer User's Guide (Revision D)	EK-SBC11-UG

▪ LAV11 Printer Option

The LAV11 printer option is a high-speed line printer system for use with a Q-bus system. The option consists of an LAV11 interface module, an interface cable, and a line printer.

The LAV11 has been replaced by the LPV11 printer option.

Related Documentation

Document Title	Order Number
LAV11 User's Manual	EK-LAV11-OP-001
LA180 DECprinter I Maintenance Manual	EK-LA180-MM
LAV11 Field Maintenance Print Set	MP-00306-00

▪ MRV11-AA Read-Only Memory Module

The MRV11-AA is a basic read-only memory module on which the user can install programmable read-only memory (PROM) or masked read-only memory (ROM) chips

The MRV11-AA has been superseded by the MRV11-BA.

Related Documentation

Document Title	Order Number
MRV11-AA Field Maintenance Print Set	MP-00066-00

▪ MRV11-BA UV PROM-RAM Memory Module

The MRV11-BA is a memory option that contains eight sockets in which MRV11-BC ultraviolet (UV), erasable, programmable read-only memory (EPROM) integrated circuits can be installed. The MRV11-BA also contains 256 by 16-bit static random access memory (RAM) that can be used as a "scratchpad" or "stack" by the system software.

The MRV11-BA memory module has been superseded by the MRV11-C.

Related Documentation

Document Title	**Order Number**
LSI-11 UV PROM-RAM User's Manual	EK-MRV11-TM
MRV11-BA Field Maintenance Print Set	MP-00354-00

▪ REV11 DMA Refresh/Bootstrap/Terminator

The REV11-A module consists of DMA refresh circuits, a bootstrap ROM, and 120-ohm termination circuits The REV11-C module is similar to the REV11-A but does not have the termination circuits.

The REV11 has been phased out because the functions it performed are now available on a variety of other modules.

Related Documentation

Document Title	**Order Number**
REV11 Field Maintenance Print Set	MP-00073-00

▪ RKV11-D Disk Drive Controller

The RKV11-D disk controller interfaces RK05 disk drives to the Q-bus.Because the RK05 disk drive has been superseded by the RL01/02 disk drive, the RKV11-D has been superseded by the RLV11 disk controller.

Related Documentation

Document Title	**Order Number**
RKV11-D Disk Drive Controller User's Manual	EK-RKV11-OP-001
RKV11-D Disk Drive Controller Technical Manual	EK-RKV11-TM-001
RK05/RK05J/RK05F Disk Drive Maintenance Manual	EK-RK5JF-MM-001
RK05/RK05J Disk Drive Preventive Maintenance Manual	EK-RK05J-PM-001
RK05F DEC Disk Drive Preventive Maintenance Procedure	ED-RK05F-PM-001
RKV11-D Field Maintenance Print Set	MP-00223-00

▪ RLV11 Disk Controller

The RLV11 disk controller interfaces RL01 and RL02 disk drives to the Q-bus. The RLV11 has been replaced by the RLV12.

Related Documentation

Document Title	Order Number
RLV11 Disk Controller Technical Description	EK-RLV11-TD
RL01/RL02 Disk Drive Technical Manual	EK-RL012-TM
RL01/RL02 Pocket Service Guide	EK-RL012-PG
RL01/RL02 Disk Subsystem User's Guide	EK-RL012-UG
RLV11 Field Maintenance Print Set	MP-00635-00
RLV11/RL01/RL02 Diagnostic Documentation Kit	ZJ285-RZ

▪ RXV11 Floppy Disk Interface

The RXV11 interfaces RX01 floppy disk drives to the Q-bus. The RXV11 has been replaced by the RXV21.

Related Documentation

Document Title	Order Number
RXV11 User's Manual	EK-RXV11-OP-001
RX01/RX8/RX11 Floppy Disk System Maintenance Manual	EK-RX01-MM
RX01/RX02 Reference Card	EK-RX01-RC
RXV11 Field Maintenance Print Set	MP-00024-00
RX8/RX01 Diagnostic Documentation Kit	ZF220-RZ

▪ VK170-CA Serial Video Module

The VK170-CA module is an extended-length, dual-height, single-width board that forms an integral part of a terminal. The module accepts serial ASCII encoded data to be stored in a refresh memory to generate a display for a video monitor. The VK170-CA also accepts parallel data from a keyboard (on strobe demand) to generate serial ASCII output.

Related Documentation

Document Title	Order Number
M7142 Serial Video Module User's Manual	EK-M7142-UG
VK170-CA Field Maintenance Print Set	MP-00775-00

▪ VSV11 Graphics Display

The VSV11 is a high-performance color video graphics system for the Q-bus. The base system consists of three quad-height modules that communicate across the CD interconnect. The base system can be expanded to provide higher resolution and/or multiple graphics planes. The system uses DMA Q-bus transfers and a dedicated display microprocessor to read and execute graphics instructions.

Related Documentation

Document Title	**Order Number**
VSV11 Raster Graphics System Option Description	YM-C193C-00
VSV11 Field Maintenance Print Set	B-TC-VSV11-0-1

Notes

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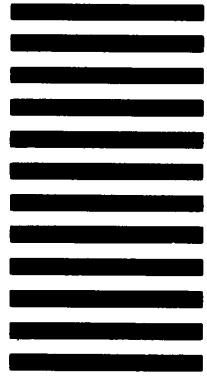

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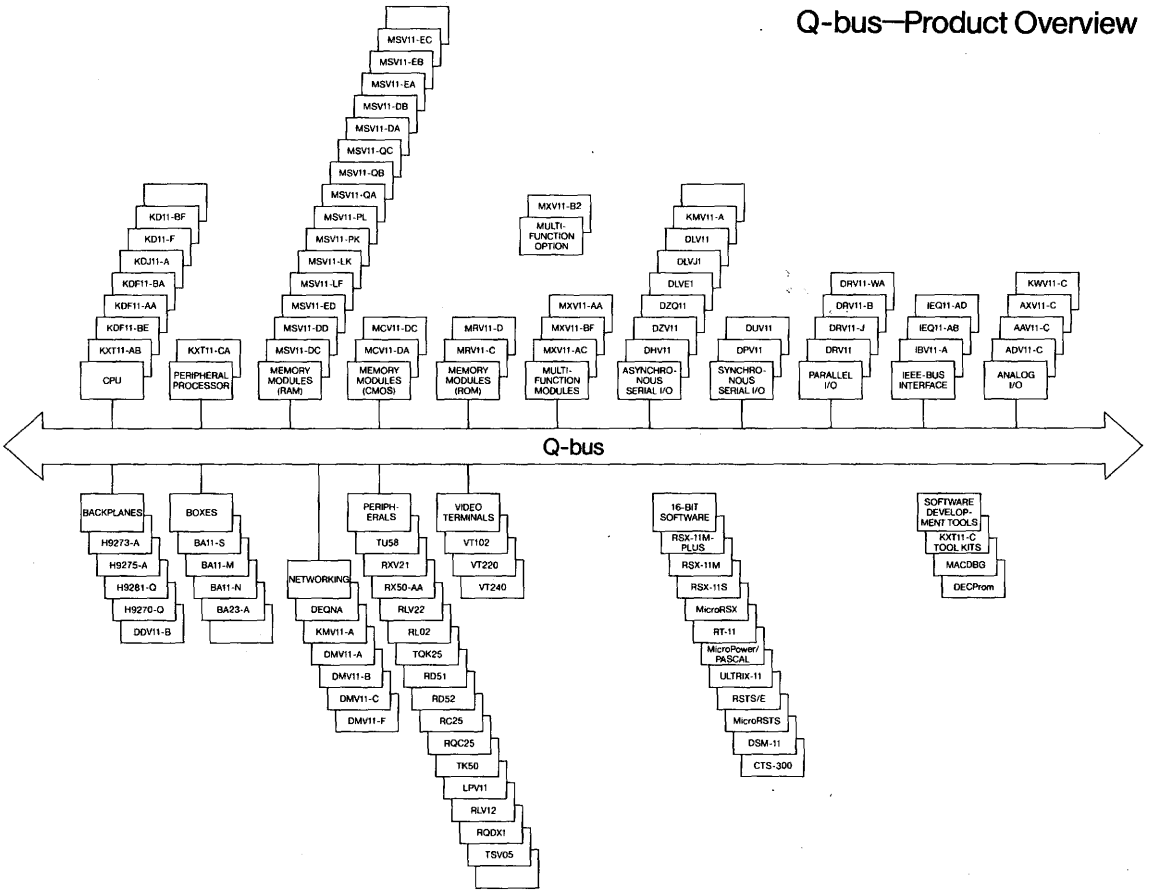
Q-bus—Product Overview



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