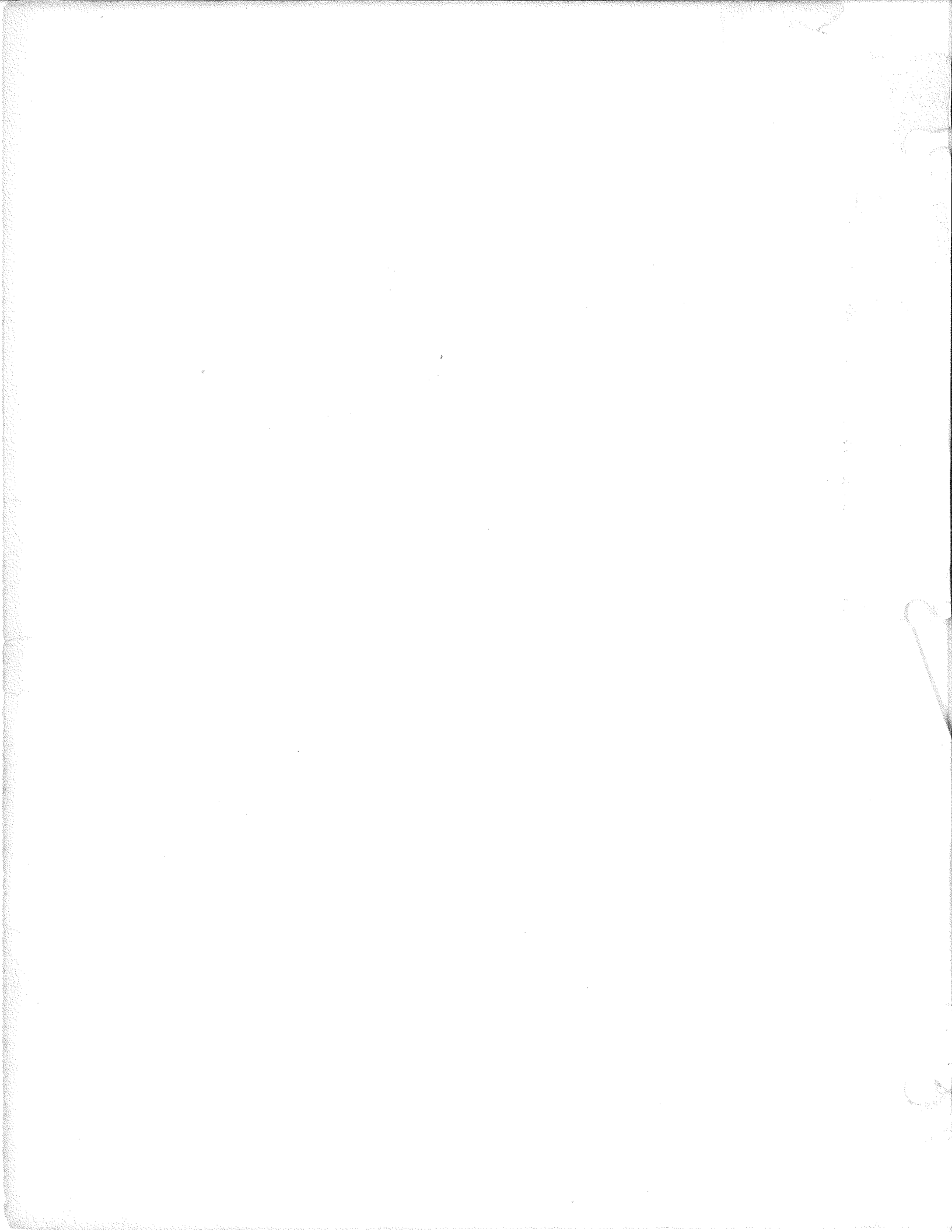IDENTIFICATION

Product Code: MAINDEC-9A-D1BA-D   *CHECKERBOARD*

Product Name: PDP-9 Extended Memory Test

Date Created: January 18, 1967

Maintainer: Diagnostic Group

Author: J. W. Richardson

CONTENTS

CONTENTS (continued)

1   ABSTRACT

The PDP-9 Extended Memory Test tests and verifies the operational status of core memory by testing the ability of core memory to detect a 1 or 0 under maximum half-select noise conditions. The program consists of four subtests, one of which must be selected by the operator.

2   REQUIREMENTS

2.1   Equipment

A standard PDP-9 equipped with from 8,192 to 32,768 words of core memory.

2.2   Storage

The program occupies 2701_8 words of core memory starting at location 21_8 up to and including location 2722_8 when loaded in the lower 4K field of any 8K memory bank. When it occupies the higher 4K field of an 8K bank, it occupies location 10021_8 to 12722_8.

2.3   Programs

None are required except the PDP-9 Extended Memory Test HRI binary tape which is supplied.

3   LOADING PROCEDURE

The binary tape supplied is punched in the HRI mode and may be loaded into the lower 4K of any 8K memory bank by setting the ADDRESS switches as follows:

Memory Bank	ADDRESS Switches
0	00021_8
1	20021_8
2	40021_8
3	60021_8

After placing the correct value in the ADDRESS switches, place the binary tape in the reader. Press I/O RESET and then READ-IN.

The program is self-starting, and at the completion of loading prints a program header followed by a carriage return, line feed, and halt. The contents of the PC after the halt equal 1101. The program header is not printed again unless the program is reloaded.

4   STARTING PROCEDURE

After the program halt at location 1101, set ACS (accumulator switches) 14 through 17 to any value as described in section 4.1 and press CONTINUE. The program then continues to run until manually stopped by the operator.

4.1   Control Switch Settings

Immediately after the program halt at location 1101, the operator must signify the amount of core memory to be tested. This is done by placing the lower order 8K bank to be tested in ACS 14 and 15, and the highest order 8K bank in ACS 16 and 17. The combinations recognized by the program are shown below. Press CONTINUE after placing the desired value in ACS 14 through 17.

Test Memory Bank to Memory Bank			ACS 14	15	16	17
(8K)	0	0	0	0	0	0
(16K)	0	1	0	0	0	1
(24K)	0	2	0	0	1	0
(32K)	0	3	0	0	1	1
(8K)	1	1	0	1	0	1
(16K)	1	2	0	1	1	0
(24K)	1	3	0	1	1	1
(8K)	2	2	1	0	1	0
(16K)	2	3	1	0	1	1
(8K)	3	3	1	1	1	1

All other AC switches must be down.

The program recognizes ACS 14 and 15 as the lowest order 8K bank to be tested, and ACS 16 and 17 as the highest order 8K bank to be tested. The lower limit value must not exceed the higher limit value. When this occurs, the message "L.L. EXCEEDS U.L." is printed on the KSR 33 Teleprinter. A program halt occurs, after printing is done, at location 1100 (C(PC)=1101). (C(PC) means contents of program counter.) To recover, correct the ACS settings and press CONTINUE. The program then continues in a normal manner.

The amount of core memory tested at one time when using a PDP-9 without extended memory is 4K.

The amount of extended core memory tested at one time equals the amount selected by ACS 14 through 17, minus 4K. If 32K of core memory is to be tested, the actual amount tested at one time is 28K. The lower 4K field of the memory bank which contains the program is not tested until program relocation takes place (section 4.3.1).

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4.2   Starting Addresses

To restart the program, two addresses are available, 00021 or 00043. If the program happens to be in the higher 4K field of any 8K memory bank, the restarting address is 10021 or 10043. The restarting address is relative to the memory bank in which the program is currently located.

4.2.1   Restarting Addresses –

The preferred restarting address is 00043 (or 10043). When restarting at this address, the program executes new parameter entries specified by the ACS, and continues to suppress testing any bits selected by input from the KSR 33 keyboard as described in section 9.1.7. Also, the contents of the error word table (section 9) are retained.

Restarting at 00021 or 10021 restores all constants and control words, clears the error word table to zero, and executes new parameter entries.

4.3   Program Action

The program should normally be loaded into memory bank 0. Since loading into any other bank is an exception rather than standard procedure, any reference to program relocation, automatic or forced relocation, will be made with the assumption that the program has been loaded into bank 0.

After pressing CONTINUE or after a restart, the program senses the ACS and checks for invalid switch settings. If all is in order, the lower and upper limit addresses of memory are determined from ACS 14 through 17.

The program next performs the three subtests. A "sliding zero" test (subtest 1) is first executed, followed by subtests 2 and 3 (worst case checkerboard and complement checkerboard).

The action next taken is program relocation.

4.3.1   Program Relocation –

Program relocation depends entirely upon the amount of core memory being tested. For PDP-9s equipped with extended memory, the program normally first relocates to the highest order memory bank under test. From there it relocates to the next lower bank (after performing the three subtests). The program keeps relocating to the next lower memory bank until it reaches the lowest order bank under test. The testing and relocation cycle then are repeated. This cycle continues until manually interrupted by the operator. The program always occupies the lower 4K field of any memory bank.

The program will not relocate if any of the conditions described below exist.

a. A forced relocation has been made (section 9.1.8).

b. The program is currently located in an upper 4K field, and only one or more extended memory banks are under test.

c. The program is currently located in the lower 4K field, and only one extended memory bank is under test.

d. The error word table indicates an error present in all available lower 4K fields under test (section 9).

e. ACS 9 is in the up position (section 9.1.6).

MA (memory address) register bits 3 and 4 indicate the current bank while the program is running.

If the program is testing a single 8K memory bank which contains the program, the program first tests the upper 4K field, relocates to the upper 4K field and tests the lower 4K field, and then moves back to the lower 4K field.

The program will not relocate if any of these conditions exist:

a. A forced relocation has been made (section 9.1.8).

b. The error word table indicates an error present in the destined 4K field (section 9).

c. ACS 9 is in the up position (see section 9.1.6).

One complete pass of the program is defined as the execution of all three subtests on all available core memory from each memory bank or from the low and high 4K fields in the case of a single 8K memory bank being tested.

5 OPERATING PROCEDURES

5.1 Operational Switch Settings

ADDRESS Switches for Loading (0021)

    1,2   Set to the desired memory bank.

AC Switches

    14,15   Set to indicate the lowest order bank to be tested.

    16,17   Set to indicate the highest order bank to be tested.

Press CONTINUE if the program has halted after the header printout.

Press START if executing a program restart.

The current location of the program may be determined by observing MA (memory address) indicators 3, 4, and 5. MA bit 5 equals 1 when the program is in the higher 4K field of a memory bank.

When all core memory has been determined as error free, using nominal and marginal power supply voltages, subtest 4 must be performed. The operator selects this subtest by placing ACS 6 up. Subtest 4 tests the ability of core memory to retain data after A.C. power is dropped and then turned on again.

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Use the procedures below to execute subtest 4.

    a. Press STOP if the program is running.

    b. Place ACS 6 up, and set the ADDRESS switches to 00021.

    c. Press START. The program loads the checkerboard pattern generated by subtest 2 into all core memory, and then halts with (C(PC)=444) before reading the pattern.

    d. Place the POWER switch to OFF and wait until all power is removed.

    e. Place the POWER switch to ON.

    f. Set the ADDRESS switches to 00457 (tagged RRTRN), and press START.

The program reads all selected core memory under test, and provides typeouts upon detection of any errors.

If core memory is error-free, the program halts with C(PC)=1101 after reading core memory once. Program relocation does not take place.

Performing all four subtests sequentially on nominal and marginal power supply settings, with the absence of any error printouts, indicates core memory to be operational.

5.2   Subroutine Abstracts

5.2.1   "Sliding Zero" Subtest – ACS 3 – A pattern consisting of all 1s is first loaded into core memory. Each bit of each memory word is then complemented, stored back into memory, read, complemented and stored back once more, and then tested for error. The memory location under test should always equal 777777_8. If not, a printout is given which contains the subtest number, octal address where the error is located, the bad data word, the good data word, and the bit currently being tested.

5.2.2   Worst Case and Complement Worst Case Checkerboard ACS 4 and 5 – Subtest 2 and its complement, subtest 3, are next performed. Each subtest contains two different patterns which are loaded and read separately.

The first pattern loaded by subtest 2 is loaded into all core memory under test in 200_8-word blocks, complementing the pattern every 200_8 locations. The second pattern is loaded in the same manner, except the pattern is complemented every 400_8 locations.

When the pattern is read, all core memory under test is read as rapidly as possible 16 times. The pattern is complemented after each pass through memory, ending up the pattern originally loaded. No error checking is done during the 16 passes.

On the 17th pass, each memory location is tested for errors in the following manner:

    a. Read the location

    b. Complement the data

    c. Deposit back

    d. Repeat a, b, c; then perform e

    e. Read the location

    f. Compare the data read with a constant.

Steps a through f are repeated six times for each location, checking for errors on every third read.

Should an error be detected, an error printout occurs, after which the next sequential memory location is read and tested for error.

Subtest 3 tests core memory exactly as subtest 2. The only difference is that the two patterns loaded and tested are the complements of those executed by subtest 2.

5.2.3   <u>Generating the Checkerboard Patterns</u> – If the operator wishes to test only a small area of any memory field or bank by using one of the four checkerboard patterns, it is necessary to describe the method of generating the patterns.

Each of the checkerboard patterns, after being loaded into core memory consists of words equal to all 1s and all 0s. In order to place a pattern into memory as rapidly as possible, a pattern control word is used. There is one control word associated with each of the four patterns. Bits 0-15 of the control word are tested individually, and if any bit equals 0, a word of all 0s is written. Likewise, a word of all 1s is written if the tested bit equals 1.

The control word also indicates when to complement the pattern by using bit 17. If bit 17 equals 0, the pattern complements every 200_8 locations. If it equals 1, the pattern complements every 400_8 locations. The reading and testing routines use this same method to determine what the data should equal.

The two control words for subtest 2 are 037700 and 037701. Those used for subtest 3 are 740076 and 740077. These four control words are stored in memory locations 2463, 2464, 2465, and 2466, respectively.

6   ERRORS

6.1   Data Error Printouts

After the program is loaded, the header printout is given to aid in identifying the error. The header appears as:

TEST   OCTAL ADR.   BAD   GOOD   PAT.

where: TEST = subtest number which detected the error (1, 2 or 3).

OCTAL ADR. = The memory location containing the data in error.

BAD = The data (in octal) read from the memory location.

GOOD = What the data (in octal) should have been.

PAT. = For subtest 1, an octal number containing all 0s except for one digit. This indicates the bit presently under test. For subtests 2 and 3, PAT. equals the pattern control word being used.

Example:

TEST	OCTAL ADR.	BAD	GOOD	PAT.
1	010273	776777	777777	001000
1	011073	767777	777777	000001
2	060445	777775	777777	037700
3	031405	200000	000000	740077

From the above example it may be seen that during one pass of the program four errors occurred. The first two, during subtest 1, show that at location 10273, bit 8 was dropped, and at location 11073, bit 5 was dropped.

Subtest 2 shows bit 16 dropped at location 445 in memory bank 3, using the checkerboard pattern which complements every 200_8 locations.

Subtest 3 detects bit 1 being picked up at location 11405, the higher 4K field of memory bank 1. The control word used indicates that the pattern being used complements every 400_8 locations.

6.2   Halt on Error – ACS0

To halt on error, raise ACS0 during any error typeout, and the program halts, after typeout, with the PC=1101. Any new parameters may be entered into the ACS at this point.

Press CONTINUE to recover.

If no new parameters have been specified, the program continues with the current subtest, reading the next sequential memory location. If new parameters are specified, the program performs as if restarted at address 00043.

7   RESTRICTIONS

7.1   Starting Restrictions

Restart at address 00021 to restore all constants and control words and to test all bits for failure.

Restart at 00043 to continue suppressing testing any bits previously selected.

7.2   Operating Restrictions

The PDP-9 Memory Address Test must have been run successfully before attempting to run this test.

The PDP-9 Basic Memory Checkerboard Test should be used prior to this test to eliminate any "hard" errors present in memory.

8   MISCELLANEOUS

8.1   Execution Time

Execution time depends upon the amount of core memory to be tested. The approximate time for the program to execute all three subtests on a single 8K memory bank is approximately 40 seconds, and for 32K approximately 7 minutes. Approximately 20 seconds are required for each 4K field when testing a single memory bank.

9   PROGRAM DESCRIPTION

The PDP-9 Extended Memory Test is designed to verify the operational status of core memory by providing worst case data patterns, and for minimum manual intervention by the operator.

An HRI binary tape is supplied as an aid to loading the program. At the completion of program loading, the program is located in addresses 00021_8 to 2722_8.

After the operator has entered the amount of core memory to be tested in ACS 14 through 17, and pressed CONTINUE, the program executes the three subtests and then relocates as described in section 4.3.1.

After the program completes testing all selected core memory from one memory bank, the next location to be occupied by the program is computed. In the process a 4-word table is scanned. This table contains the address of the first error encountered in any memory bank. If the table shows an error was found in the location to be occupied, the next lower memory bank is checked. If this bank proves to be error-free, it is set up as the new location for the program. The program does not relocate if all available areas have indicated an error. This same procedure is also applied when testing single 8K memory banks.

The table is cleared after each execution of all three or any one subtest, or by restarting the program at location 00021. Restarting at 00043 does not clear the table.

9.1   Applications

For operating convenience, and as an aid to troubleshooting, each AC switch is assigned a unique function. This allows minimum program intervention. The ACS assignments, their effect on the program, and program action are described below. The ACS described, except for ACS 14 through 17, may be raised or lowered while the program is running. Since ACS 14-17 control the amount of core memory to be tested, some other value than the amount desired may be tested. The program may be destroyed if ACS 14-17 are changed while the program is running.

9.1.1   Halt After Loop or Error - ACS 0 - Raising ACS 0 at any time while the program is running causes a halt, after completion of any read or write loop, with C(PC)=1101. ACS settings may then be changed if desired. Press CONTINUE to reinitiate the program. If the ACS were changed, the new parameters are executed, and if there are no changes the next sequential memory location is read by the subtest in progress at the time of the halt.

Raising ACS 0 during an error typeout causes a halt at the completion of printing with C(PC)=1101. Proceed as outlined in the above paragraph.

9.1.2   Inhibit Error Typeout - ACS 1 - Raising ACS 1 inhibits all data error typeouts. The "canned" messages, "L.L. EXCEEDS U.L.," and "ERROR IN SELECTED 4K," are not inhibited. The program still recognizes errors, but no typeout occurs.

9.1.3   Ring Bell on Error - ACS 2 - ACS 2, when "up", enables the program to ring the TTY BELL once for each error detected. ACS 2 takes precedence over ACS 1 if both should happen to be up.

9.1.4   Subtest Selections - ACS 3, 4, 5, 6 - Any one, or any combination of subtests may be executed by specifying any one or any combination of ACS 3, 4, 5, and 6. ACS 3 specifies subtest 1; ACS 4, subtest 2; ACS 5, subtest 3; ACS 6, subtest 4. The subtest specified by the lowest order ACS raised will be executed first.

If all four switches are down, subtests 1, 2, and 3 are executed in that order. The function of subtest 4 is described under section 5.1.

Program relocation, when any one or any combination of subtests is selected, is the same as if all subtests were selected.

9.1.5 'Scope Modes – ACS 7 or 8

9.1.5.1 ACS 7 Continuous Write – Using All 1s Pattern – Provides a continuous write 'scope mode by writing a pattern of all 1s into all core memory specified by ACS 14-17. This pattern may be changed by manually depositing a new word into memory location 2710.

Operating instructions:

a. Halt the program with ACS 0 or, if restarting, set the ADDRESS switches to 00021 or 00043.

b. Place ACS 3 through 6 down.

c. Place ACS 7 up.

d. Press CONTINUE. If restarting the program, press I/O RESET and then START.

Make sure ACS 0 is down, or the 'scope mode loop will halt after writing the pattern once.

To stop the loop, place ACS 0 up at any time, and a halt occurs, with C(PC)=1101. New ACS settings may then be made. Press CONTINUE to execute the new parameters. If no new ACS settings are made, the program goes on with the 'scope mode.

9.1.5.2 ACS 7 – Continuous Write – Using Checkerboard Pattern – ACS 7 also provides a continuous write 'scope mode using any one of the four checkerboard patterns generated by subtests 2 and 3.

Operating instructions:

a. Halt the program with ACS 0, or, if restarting, set the ADDRESS switches to 00021 or 00043.

b. Place ACS 7 up.

c. Place ACS 4 or 5 up. ACS 4 provides a continuous write using control word 037700; ACS 5 using control word 740076.

d. Place ACS 0 down and press CONTINUE. If restarting the program, press I/O RESET and then START, at address 21 or 43.

To stop the loop place ACS 0 up at any time, and a halt will occur with C(PC)=1101. New ACS settings may then be made. Press CONTINUE to execute new parameters. If no new ACS settings are made the program continues with the 'scope mode.

A continuous write may be used with control words 037701 or 740077 by manually depositing the desired control word into location 2463. When this is done, begin with step a of 9.1.5.2 and proceed as outlined. In step c raise ACS 4 only. An alternative to the above method is to select the subtest which uses the desired control word, and raise ACS 7 just before the program writes the pattern

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desired. Control word 037701 is used last by subtest 2 and 740077 is used last by subtest 3. The MA indicator lights, when running subtest 2 or 3, appear to first glow dimly for several seconds. The subtest at this point has written the first pattern and is reading, but not testing for errors. The MA then begins to increment slowly. The subtest is now testing for errors. After testing all of selected memory for errors, the subtest then writes the next pattern using the second control word. The MA indicators appear exactly as when the first pattern was written and read. By placing ACS 7 up anytime before the MA is done incrementing the first time, a continuous write 'scope mode will take place using the second control word associated with the subtest.

The program will not relocate automatically while in the continuous write 'scope mode.

9.1.5.3 ACS 8 – Continuous Read – Using Previously Written Pattern – Provides a continuous read 'scope mode by reading the pattern last written into memory by the last subtest performed, or the pattern which was written by the continuous write loop.

Operating instructions:

a. Halt the program with ACS 0 or, if restarting, set the ADDRESS switches to 00021 or 00043.

b. Place ACS 3 through 6 down.

c. Place ACS 8 up.

d. Place ACS 0 down and press CONTINUE. If restarting the program, press I/O RESET and then START.

To stop the loop, place ACS 0 up at any time and a halt will occur with C(PC)=1101. New ACS settings may then be made. Press CONTINUE to execute the new parameters. If no new ACS settings are made, the program will continue with the 'scope mode.

9.1.5.4 ACS 8 Continuous Read – Using Subtest Generated Pattern – ACS 8 also provides a continuous read 'scope mode on any one of the patterns generated by subtests 1, 2, or 3.

Operating instructions:

a. Halt the program with ACS 0 or, if restarting, set the ADDRESS switches to 00021 or 00043.

b. Place ACS 8 up.

c. Place ACS 3, 4, or 5 up.

d. Place ACS 0 down and press CONTINUE. If restarting the program press I/O RESET and then START.

The program repeatedly reads and tests all of core memory selected by ACS 14-17, using the read and test routine of the selected subtest. If subtest 2 is selected, the pattern read is the one written by control word 037700. If subtest 3 is selected, the pattern read is the one written by control word 740076.

To stop the loop, place ACS 0 up at any time and a halt occurs with C(PC)=1101. New ACS settings may then be made. Press CONTINUE to execute the new parameters. If no new ACS settings are made, the program continues with the 'scope mode.

A continuous read may be used with the patterns generated by control words 037701 (subtest 2) or 740077 (subtest 3) by manually depositing the control word in location 2463. When this is done begin at step a above and proceed. In step c raise ACS 4 only. As with ACS 7, an alternate method may be used. In the case of a continuous read, raise ACS 8 during the time the program is reading the desired pattern. Subtest 2 first generates and reads the pattern using control word 037700. This is indicated by the MA indicator lights glowing dimly for several seconds, and then slowly incrementing. The MA indicators again glow dimly and then slowly increment when writing and reading the second pattern, which is generated by control word 037701. Subtest 3 performs the same, only the pattern control word first used is 740076, followed by 740077. Placing ACS 8 up during the first time the MA increments will cause a 'scope mode using the first pattern generated.

Place ACS 1 up if error printouts are not desired.

To stop the loop, place ACS 0 up at any time, and a halt will occur with C(PC)=1101. New ACS settings may then be made. Press CONTINUE to execute the new parameters. If no new ACS settings are made the program continues with the 'scope mode.

The program will not relocate automatically while in the continuous read 'scope mode.

9.1.6   Inhibit Program Relocation - ACS 9 - The program normally relocates automatically. To contain the program within one 4K field of its current memory bank, raise ACS 9 at any time.

9.1.7   Suppressing the Testing of Bits - ACS 10 - Bits to be suppressed from further testing are selected via the KSR 33 keyboard.

With ACS 10 in the up position, the program halts after the first error typeout and waits for input from the KSR 33.

Basic operating instructions:

   a. Place ACS 10 up at any time. After the next error typeout, the program halts.

   b. Place ACS 10 down.

c. Type the desired bit position (in decimal) to be suppressed.

d. Press the carriage return key. The program resumes testing all but the selected bits.

To suppress more than one bit position:

a. Proceed as above, but separate the selected bit positions with a comma.

Example: To suppress bits 0, 8, and 17 type 0, 8, 17 and then carriage return.

It is not necessary to type the bit positions in their numerical order.

To recover from a typing error:

Press the rub out key and retype all selected positions.

To continue suppressing previously selected bits after halting with ACS 10 up:

a. Press the line feed key. The program continues with the next sequential memory location.

To suppress testing additional bits, or to change previously selected bits:

a. After the halt with ACS 10 up, type in the new bit positions plus the positions of the previously selected bits, if desired.

To resume testing all bit positions:

a. After a halt with ACS 10 up, press the carriage return key.

b. If the program does not halt with ACS 10 up, due to no detected errors, restart the program at location 00021.

9.1.8   Force a Program Relocation - ACS 11 and 12

a. Place ACS 0 up if the program is running, or restart at address 00021 or 00043.

b. Place ACS 12 up to indicate a forced program relocation.

c. Place in ACS 16 and 17 the desired memory bank   (00=bank 0; 01=bank 1; 10=bank 2; 11=bank 3).

d. ACS 11 indicates the high or low order 4K field of the memory bank set in ACS 16 and 17. Set ACS 11 up for the higher 4K; down for the lower 4K.

e. All other ACS are ignored at this point. If a halt was made with ACS 0, press CONTINUE. If restarting, press I/O RESET, and then START at address 21 or 43.   In either case, the program now relocates to the desired area, and halts with the C(PC)=1724.

f. Place ACS 11 and 12 down. If desired, make new ACS settings at this point.

g. Press CONTINUE to resume testing.

The program will not automatically relocate again until restarting at address 00021. Restarting at 00043 will not cause relocation to take place automatically.

In step f above, restore the amount of core memory to be tested in ACS 14 through 17 before pressing CONTINUE.

Before relocation takes place, the destination is first checked to see if any errors have been previously detected in the area to be occupied by the program. If an error is present, a warning of "ERROR IN SELECTED 4K" is typed out on the KSR 33. A halt then occurs with the C(PC)=1101. The operator may then change the destination or, if he wishes to ignore the error warning, press CONTINUE to relocate to the selected area.

ACS 13 - Not used

9.1.9   Upper and Lower Core Memory Testing Limits - ACS 14-17 - ACS 14 and 15 specify to the program the first (or lowest order) memory bank to be tested; ACS 16 and 17 the last (or highest order) bank. A single bank may be tested by setting ACS 16 and 17 to equal ACS 14 and 15.

If an 8K bank under test does not contain the program, relocation will not take place. However, testing more than 8K permits relocation to take place.

9.2   Testing Selected Areas of any 4K Field

Selected areas of core memory may be isolated for testing with the checkerboard patterns by following the procedure outlined below. It is important that the stated restrictions be followed.

Restriction 1: The minimum portion of any 4K field which may be isolated is 200_8 locations, when using pattern control words 037700 or 740076.

The minimum portion of any 4K field which may be isolated, when using pattern control words 037701 or 740077, is 400_8 locations.

The lower and upper limit address values must be multiples of 200_8, with reference to location 00000_8, when using pattern control words 037700 or 740076.

The lower and upper limit address values must be multiples of 400_8, with reference to location 00000_8 when using pattern control words 037701 or 740077.

Restriction 2: This restriction may be ignored if the PDP-9 being used is not equipped with extended memory.

Be sure to place the memory bank number on the lower and upper limit addresses of the block to be tested. Also, if it is necessary that the program relocate in a normal manner, make sure that the isolated block under test is not within the area to be occupied by the program. In this case, it will not interfere if the block's lower limit is 003000_8 or higher.

In order for program relocation to occur, the program must be located in the lower 4K field of any memory bank.

Restriction 3: The lower or upper limit addresses of the bank must not overlap 4K boundaries or bank boundaries.

9.2.1 Instructions for Modifications Using a PDP-9 Without Extended Memory or for a Single 8K Bank of Extended Memory Which Contains the Program –

a. If only one block in a 4K field is to be tested, the program must be in the opposite 4K field. Perform a forced relocation as described under ACS 11 and 12 earlier, if necessary.

If program relocation is desired, it is necessary that two blocks be selected, one in each 4K field.

b. For the lower 4K field, manually deposit the lower limit address into location 2523 (tagged L04KLL), and the upper limit address in 2524 (tagged L04KUL).

For the upper 4K field, deposit the lower limit address into 2525 (tapped HI4KLL), and the upper limit address into 2526 (tagged HI4KUL).

c. The memory error being isolated probably occurs more often with a particular checker-board pattern. Choose the pattern control word for this pattern from the error typeout under the column labeled "PAT".

Manually deposit this control word into location 2463 (tagged KPAT).

d. Place ACS 4 up. Place ACS 9 up if the program relocation is to be inhibited.

e. Set the ADDRESS switches to 00667. Press I/O RESET, then START.

ACS 3, 5, 7, 8 and 14 through 17 cannot be used after the modifications are made. For 'scope mode raise ACS 1 to inhibit error printouts, and ACS 9, if necessary, to inhibit relocation.

ACS 0 may be used to halt the testing. The halt occurs with C(PC)=1101. To restore the program to normal operating conditions:

a. Raise ACS 0 to halt the program.

b. Place the amount of core memory to be tested in ACS 14 through 17.

c. Set the ADDRESS switches to 757.

d. Press I/O RESET, and then START.

The program restores all constants and resumes testing in a normal manner. All ACS are again enabled.

9.2.2 Instructions for Modifications Using a PDP-9 with Extended Memory

a. For the program to relocate normally, it must be located in the lower 4K field of a memory bank. Follow Restriction 2.

b. If the program is to be run from the lower 4K field, manually deposit the lower limit address of the block into location 2525 (tagged HI4KLL), and place the upper limit address in location 2526 (tagged HI4KUL).

If the program is located in the upper 4K field, manually deposit the lower limit address in location 2523 (tagged LO4KLL), and place the upper limit address in location 2524 (tagged LO4KUL).

Only one block may be selected when the block is located in an extended memory bank which does not contain the program.

c. From the error typeout, under the column labeled "PAT.," choose the pattern control word which indicates the error in question most frequently.

Manually deposit the control word into location 2463 (tagged KPAT).

d. Place ACS 4 up. Place ACS 9 up if program relocation is to be inhibited.

e. Set the ADDRESS switches to 00667. Press I/O RESET then START.

ACS 3, 5, 7, 8 and 14 through 17 cannot be used after the modifications are made. For 'scope mode raise ACS 1 to inhibit error printouts, and ACS 9, if necessary, to inhibit relocation.

To restore the program to normal operating conditions follow the procedure explained for restoration after testing a block in a single 8K bank.

9.3 Table of ACS Assignments

The function specified by an ACS will be executed by the program as long as the ACS is in the up position.

ACS	FUNCTION
0	Halts program with C(PC)=1101 after one pass of a load or read loop. Also may be used to halt after an error typeout when raised during the type-out. C(PC)=1101.
1	Inhibits printing of error information.
2	Sounds the TTY BELL on each error.
3	Causes the program to execute the "sliding zero" subtest.
4	Causes the program to execute subtest 2, the worst case checkerboard pattern.
5	Causes the program to execute subtest 3, the complement of subtest 2.
6	Causes the program to load the pattern provided by subtest 2, and halt with C(PC)=444. This is subtest 4.
7	The program enters a continuous write routine with the subtest selected by ACS 4 or 5. If no subtest is selected, it uses its own loop.
8	The program enters a continuous read routine with the subtest selected by ACS 3, 4, or 5. If no subtest is selected, it uses its own loop.
9	Inhibits program relocation.
10	Indicates bit suppression is requested.
11	Indicates high or low 4K field when performing a forced relocation. Up equals the high 4K; down equals the low 4K.
12	Causes the program to perform a forced relocation to another 4K area.
13	Not used.
14, 15	Indicates to the program the lowest order 8K memory bank to be tested. (00=bank 0; 01=bank 1; 10=bank 2; 11=bank 3.)
16, 17	Indicates to the program the highest order 8K memory bank to be tested. ACS 16 and 17 also indicate the desired memory bank when performing a forced relocation.

9.3.1   ACS Order of Precedence

ACS

11,12	–	Forced relocation
14-17	–	Lower and upper limits to test
3	–	Subtest 1
4	–	Subtest 2
5	–	Subtest 3
6	–	Subtest 4
7	–	Continuous write
8	–	Continuous read
0	–	Halt
2	–	Bell on error
1	–	Inhibit print
10	–	Bit suppression
9	–	Inhibit relocation

9.3.2   ACS Functions
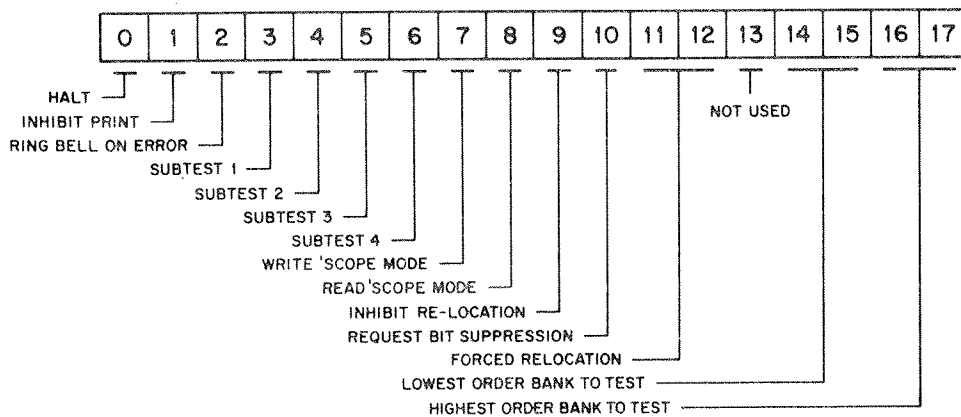
ACS Functions

9.4   Significant Memory Locations Within the Program

LOCATION	DESCRIPTION
21	Restarting address. Restores all constants and control words, and clears the error word table. The program will execute new parameter entries.
43	Restarting address. Permits the program to execute new parameter entries, but at the same time continues to suppress testing any previous selected bits. The contents of the error word table are saved.
667	Starting address. Start here when testing an isolated block of core memory.
757	Restarting address. Restart here to restore program after testing an isolated block of core memory. The program will perform as if restarted at address 21.
1101	Program halt. All program halts, except the halt after a forced relocation, occur at this location. Press CONTINUE to recover. If new ACS settings were made, the program will perform as if restarted at address 43.
1724	Program halt. This halt occurs after performing a forced relocation. Press CONTINUE to recover. The program will perform as if restarted at address 43.
2463	Tagged "KPAT" on the listing. This location contains the checkerboard control word 037700, which is the first control word used by subtest 2. This location is also used to store the desired control word when testing isolated blocks of core memory.
2464	Contains the control word 037701 which is the second control word used by subtest 2. The checkerboard pattern is complemented every 400_8 locations using this control word.
2465	Contains the control word 740076 which is the first used by subtest 3, and writes the complement pattern of that written by control word 037700 used by subtest 2. The pattern is complemented every 200_8 locations.
2466	Contains the control word 740077 which is the second used by subtest 3, and writes the complement pattern of that written by control word 037701 used by subtest 2. The pattern is complemented every 400_8 locations.
2710	Contains 777777, which is used by the continuous write 'scope mode loop to write an all 1s pattern. This may be changed to provide any other pattern. The contents of every location of core memory will equal this word.

IDENTIFICATION

Product Code: MAINDEC 9A-D1BA-LD

Product Name: Octal Dump of PDP-9
                 Extended Memory Test

Maintainer   Software Service Group

```
/PDP-9 EXTENDED MEMORY TEST
/1/
BEGIN,          IOF
                CLLF
                LAW
                DAC BITSUP
                LAC SUPRIT
                DAC HERWD
                LAC (400000
                DAC LAST
                DZM ERWRD+1
                DZM ERWRD+2
                DZM ERWRD+3
                DZM ERWRD+4
                DZM MVCNT
                DZM FRTAB
                JMS FIELD
                AND LLD                   /MASK BANK LOADED
                DAC FLOAD
                DAC FLOADA
STOVER,         LAS                       /READ PARAMETERS
                DAC MCWA
                DAC MCWB
                AND (40
                SZA!CLL
                JMP FCDMV
                LAC MCWA
                AND (3                    /MASK UPPER LIMITS
                DAC TEMP+1
                LAC MCWA
                AND (14                   /MASK LOWER LIMITS
                RTR
                CMA
                TAD (1                    /2'S COMPLEMENT L.L.
                TAD TEMP+1                /SUB U.L. -L.L.
                SPA
                JMP PREXD                          /YES
                LAC MCWA
                AND (17                   /MASK U.L. & L.L.
                TAD BASE                  /BASE + LIMITS
                DAC LOCN
                LEM
                JMP I LOCN                /DETERMINE LIMITS
EXTST,          LAW -17
                DAC READ40
                LAC (074000
                AND MCWA                  /MASK TEST FLAGS
                SNA                       /ALL TESTS?
                JMP TSTAL                          /YES
                LAC MCWA                  /NO
                AND (074000
                SZA                       /DROP POWER TEST?
                JMP TST2                  /YES
                LAC MCWA
                AND LLC
                SZA                       /SLIDING ZERO TEST?
                JMP TST1                  /YES
```

```
EXAM2,          LAC MCWA
                AND LLB
                SZA                        /CHECKERBOARD?
                JMP TST2                   /YES
EXAM3,          LAC MCWA
                AND (010000
                SZA                        /COMPLEMENT CHECKERBOARD?
                JMP TST3                   /YES
                LAS
                AND (400
                SZA
                JMP STOVER
                JMP TSTMV                              /DETERMINE PROGRAM DEST'N
/DETERMINE TEST LIMITS
LOCN,           HLT
                JMP AD01        /BANK 0 TO 0
                JMP AD02        /BANK 0 TO 1
                JMP AD03        /BANK 0 TO 2
                JMP AD04        /BANK 0 TO 3
                HLT
                JMP AD05        /BANK 1 TO 1
                JMP AD06        /BANK 1 TO 2
                JMP AD07        /BANK 1 TO 3
                HLT
                HLT
                JMP AD08        /BANK 2 TO 2
                JMP AD09        /BANK 2 TO 3
                HLT
                HLT
                HLT
                JMP AD10        /BANK 3 TO 3
AD01,           LAC LLB         /U.L.
ADRJP,          DAC ULREG
                DAC ULTAB
                LAC LLA         /L.L.
ADRMP,          DAC LLREG
                DAC LLTAB
                JMP EXTST
TSFLD,          0
                LAC LLREG
                DAC SLREG
                DAC WCREG
                SAD FLOADA
                SKP
                JMP I TSFLD
                ISZ TSFLD
                ISZ TSFLD
                JMP ADJUST
AD02.           LAC LLC         /U.L.
                JMP ADRJP
AD03.           LAC LLD         /U.L.
                JMP ADRJP
AD04.           LAC ULD         /U.L.
                JMP ADRJP
AD05.           LAC LLC         /U.L.
ADR,            DAC ULREG
                DAC ULTAB
                LAC LLB         /L.L.
                JMP ADRMP
```

```
AD 6.          LAC LLD                    /U.L.
               JMP ADR
AD 7.          LAC ULD                    /U.L.
               JMP ADR
AD 8.          LAC LLD
ADRA.          DAC ULREG
               DAC ULTAB
               LAC LLC                    /L.L.
               JMP ADRMP
AD 9.          LAC ULD                    /U.L.
               JMP ADRA
AD10.          LAC ULD                    /U.L.
               DAC ULREG
               DAC ULTAB
               LAC LLD                    /L.L.
               JMP ADRMP
TSTAL,         LAC MCWA
               AND (3000
               SZA                        /CONTINUOUS LOAD OR READ?
               JMP .+5                    /YES
               LAC (070000
               XOR MCWA                   /SET ALL TEST FLAGS
               DAC MCWA
               JMP TST1
               AND (2000
               SZA                        /CONT. LOAD?
               JMP CLOOP                           /YES
               JMP CROOP                           /CONT. READ

/SLIDING ZERO IN A FIELD OF ONES

TST1,          LAW 261                    /TTY CHAR1
               DAC TTY
               JMS TSFLD
               LAM -17777
               DAC WC8K
               LAM
               EEM
               DAC I SLREG                /STORE A WORD
               ISZ LLREG
               ISZ SLREG                          /INCR. ADR
               ISZ WC8K                   /8K?
               JMP .-4
               LAM -17777                         /YES

               DAC WC8K                   /RESTORE COUNT
               LAC LLREG
               SAD ULREG                          /DONE LOADING?
               JMP SLDON                          /YES
               LEM
               LAC SLREG                          /NEXT FIELD S.A.
               JMP TST1+2
```

```
SLDON,      LEM
            LAC LLTAB
            DAC LLREG
RTSTC,      JMS TSFLD
            LAM -17777
            DAC WC8K
SLOOP,      LAM -21
            DAC WC18
            LAC (400000
            DAC PATWD
            LAM
            DAC PATR
LDWRD,      LAC PATR                    /READ
            EEM
            DAC I SLREG
            LAC I SLREG
            XOR PATWD                        /COMPLEMEMT 1 BIT
            DAC I SLREG
            LAC I SLREG
            XOR PATWD                        /COMPLEMEMT AGAIN
            DAC I SLREG
            LAC I SLREG
            SAD PATR                    /SHOULD EQUAL 777777
            SKP
            JMP ERRORA
SLRTN,      LAC PATWD                        /SETUP FOR NEXT BIT
            RCR
            DAC PATWD
            ISZ WC18                    /CHECK FOR 18 BITS DONE
            JMP LDWRD
            ISZ LLREG
            ISZ SLREG
            ISZ WC8K
            JMP SLOOP
            LAM -17777
            DAC WC8K                    /RESTORE COUNT
            LAC LLREG
            SAD ULREG                        /DONE READING ALL?
            JMP SRDON                         /YES
            DAC SLREG
            LEM
            JMP RTSTC
SRDON,      LEM
            LAC LLTAB
            DAC LLREG                         /RESTORE ORIG S.A.
            LAS                         /PARAMS
            SPA                         /HALT?
            JMS HLTA
            LAS
            SAD MCW8
            SKP
            JMP STOVER
            AND (1000
            SZA                         /CONTINUOUS READ?
            JMP RTSTC
            JMP EXAM2                         /NO
```

```
/WORST CASE CHECKERBOARD
TST2.           LAC KPAT
                DAC MPAT
                LAW 262
                DAC TTY
RTRN4,          JMS TSFLD
                LAM -77
                DAC WC64
LCNTA,          LAC MPAT
                DAC PATWD
                LAM -1
                DAC WC256
                LAM -7                  /-8
                DAC WC128
CNTB.           LAM -17                 /-16 DECIMAL
                DAC WC16
                LAC PATWD
                DAC PATR                /CHECKERBOARD GENERATOR
WCLOOP.         LEM
                LAC PATR
                RCL
                DAC PATR                /SAVE PATTERN
                SZL;CLA                 /TEST FOR A1OR0
                CMA
                DAC I WCREG             /STORE  A WORD
                ISZ LLREG
                ISZ WCREG                       /INCR. ADR
                ISZ WC16                /16 WORDS YET?
                JMP WCLOOP              /NO
                ISZ WC128
                JMP CNTB
                ISZ WC64                /CHECK FOR 8K DONE
                SKP
                JMP DONL8K
                LAC MPAT
                RCR
                SNL                     /CHECK FOR 200 OR 400 COMPLEMENT
                JMP .+3
                ISZ WC256
                JMP CNTB-2
                LAC PATWD                       /COMPLEMENT CONTROL WORD
                CMA
                DAC PATWD
                JMP LCNTA+2
DONL8K.         LAM -77
                DAC WC64
                LAC LLREG
                SAD ULREG               /DONE LOADING ALL?
                JMP WCLUN               /YES
                LEM
                LAC WCREG               /NEXT BANK S.A.
                JMP RTRN4               /DO NEXT
```

```
WCLDN,          LEM
                LAC LLTAB
                DAC LLREG                        /ORIG. S.A.
                LAC MCWA
                AND (004000
                SZA                      /POWER DROP TEST?
                HLT                      /YES. DROP POWER HERE
                LAS
                AND (402000
                SAD (402000          /HALT?
                JMS HLTA                 /YES
                LAS
                SAD MCWB
                SKP
                JMP STOVER
                AND (2000
                SAD (2000                        /CHECK FOR CONT.LOAD
                JMP RTRN4

/READ CHECKERBOARD

RRTRN,          JMS TSFLD
                LAM -77
                DAC WC64
RCNTA,          LAC MPAT
                DAC TEMP+1
                LAM -1
                DAC WC256
                LAM -7                   /-8
                DAC WC128
RCNTB,          LAM -17                  /-16 DECIMAL
                DAC WC16
                LAC TEMP+1
                DAC PATR                 /CHECKERBOARD GEN
RLOOP,          FEM
                LAC PATR
                RCL
                DAC PATR                 /SAVE PATTERN
                SZL!CLA                  /TEST FOR A 1 OR 0
                CMA
                DAC PATWD                        /USED FOR COMPARE
                LAC READ40
                SNA                      /SEE IF DONE READING 16 TIMES
                JMP .+5
                LAC I WCREG                      /READ, COMPLEMENT, DEPOSIT BACK.
                CMA
                DAC I WCREG
                JMP WCRJP+2                      /SKIP TESTING FOR ERRORS
```

```
/READ AND LOAD
REPEAT,         LAC I WCREG
                CMA
                LAC I WCREG
                LAC I WCREG
                CMA
                DAC I WCREG
                LAC I WCREG
                SAD PATWD               /COMPARE
                SKP             /OK
                JMP ERROR
                ISZ WC20
                JMP REPEAT
WCRJP,          LAM -5
                DAC WC20
                ISZ LLREG
                ISZ WCREG               /INCR. ADR.
                ISZ WC16        /16 WORDS?
                JMP RLOOP               /NO
                ISZ WC128              /CHECK FOR DONE 200
                JMP RCNTR
                ISZ WC64        /IF 200, MAYBE 8K
                SKP
                JMP DONR8K          /DONE 8K
                LAC MPAT        /PAT. CONTROL WORD
                RCR
                SNL             /CHECK FOR 200 OR 400 WORD BLOCKS
                JMP .+3         /200
                ISZ WC256              /400, SEE IF DONE 2 - 200 WORD BLOCKS
                JMP RCNTR-2            /NO
                LAC TEMP+1
                CMA
                DAC TEMP+1
                JMP RCNTR+2
DONR8K,         LAM -77
                DAC WC64
                LAC LLREG
                SAD ULREG               /DONE READING ALL?
                JMP WCRDN               /YES
                LEM
                DAC WCREG               /NEXT BANK S.A.
                JMP RRTRN               /DO NEXT
```

```
NCHDN,          LAC LLTAB
                LAC LLREG                        /RESTORE ORIG S.A.
                LAC MCWA
                AND (4200
                SZA                      /POWER DROP TEST?
                JMS HLTA                 /YES
                LAS
                SMA
                JMP .+6
                JMS HLTA
                LAS
                SAD MCWB
                SKP
                JMP STOVER
                LAC READ40
                SNA
                JMP .+4
                ISZ READ40
                JMP RRTRN
                JMP RRTRN
                LAM -17
                DAC READ40
                LAS
                AND (1000
                SZA                      /CONTINUOUS READ?
                JMP RRTRN
                LAC MPAT
                RCR
                SNL
                JMP DONXT
                LAC KPAT+3
                SAD MPAT                 /CURRENTLY TEST 3?
                JMP EXAM3+4
                JMP EXAM3                          /NO
DONXT,          LAC KPAT                 /SET UP FOR NEXT PATTERN
                SAD MPAT
                JMP .+4
                LAC KPAT+3
                DAC MPAT
                JMP TST2+4
                LAC KPAT+1
                JMP .-3
TST3,           LAC KPAT+2                         /COMPLEMENT CHECKERBOARD
                DAC MPAT
                LAW 263
                DAC TTY
                JMP TST2+4
```

```
/CONTINUOUS LOAD LOOP

CLOOP,          JMS TSFLD
                NOP
                NOP
                LAC LLREG
                DAC CLREG
                LAC (777777                        /PATTERN
                FEM
                DAC I CLREG
                ISZ CLREG
                LAC CLREG
             SAD ULREG
               SKP
               JMP CLOOP+5
               LAS
               SMA                                 /HALT?
               JMP CLOOP+3
               JMS HLTA
             LAS
               SAD MCWB
               JMP CLOOP+3
               JMP BEGIN

RPART,          LAC RDJMP                          /START ADR FOR SINGLE BLNCKS
                DAC RRTRN
                LAC NOOP
                DAC WCRJP+2
                DAC WCRJP+10
                LAC DONJMP
                DAC DONRBK-1
                JMP BEGIN

STREAD,         LAS
                SPA
                JMS HLTA
                LAC .                              /SEE WHICH 4K FIELD
                AND (010000
                SZA
                JMP INHI4K
                LAC HI4KLL
                DAC WCREG
                LAC HI4KUL
                DAC ULREG
                JMP WATPAT                         /SEE WHICH WORD BOUNDARY
```

```
INH14K,      LAC LO4KLL
             DAC WCREG
             LAC LO4KUL
             DAC ULREG

WAIPAT,      LAC MPAT
             SPA
             JMP RONES
             EEM
             LAC I WCREG
             SZA
             JMP ONES            /PATTERN IS COMPLEMENT
             ISZ READ40
             JMP RCNTA
             JMP RCNTA

RONES,       EEM
             LAC I WCREG
             SZA
             JMP RONES-3
ONES,        LAC MPAT
             CMA
             DAC MPAT
             STL                 /RESTORE BIT 17 OF CONTROL WORD
             GLK
             XOR MPAT
             DAC MPAT
             ISZ READ40
             JMP RCNTA
             JMP RCNTA
DONPRT,      LAC WCREG
             SAD ULREG
             SKP
             JMP RCNTA+2
             LAC READ40
             SZA
             JMP STREAD
             JMP EXAM3+4

RSTRT,       LAC RSTPAT          /START HERE TO RESTORE PROGRAM
             DAC KPAT
             LAC RSTJMP
             DAC RRTRN
             LAC RSTLLR
             DAC WCRJP+2
             LAC RSTC64
             DAC WCRJP+10
             LAC DONPRT+3
             DAC DONRBK-1
             JMP BEGIN

RDJMP,       JMP STREAD
LOOP,        740000
DONJMP,      JMP DONPRT
RSTJMP,      JMS TSFLD
RSTLLR,      ISZ LLREG
RSTC64,      ISZ WC64
```

```
/CONTINUOUS READ LOOP

CROOP,          JMS  TSFLD
                NOP
                NOP
                LAC  LLREG
                DAC  CREG
                FEM
                LAC  I  CREG
                ISZ  CREG
                LAC  CREG
                SAD  ULREG
                SKP
                JMP  CROOP+5
                LAS
                SMA                         /HALT?
                JMP  CROOP+3
                JMS  HLTA
                LAS
                SAD  MCWB                    /PARAMETER CHANGE?
                JMP  CROOP+3
                JMP  REGIN
ADJUST,         LAC  LLREG
                XOR  (010000
                DAC  LLREG
                DAC  SLREG
                DAC  WCREG
                LAM  -37
                DAC  WC64                    /MODIFY 8K COUNT
                LAM  -7777
                DAC  WC8K
                LAC  .
                AND  (010000
                SZA
                JMP  ADJUL
                LEM
                JMP  I  TSFLD
```

```
ADJUI,          LAC  MCWA
                AND  (3
                DAC  TEMP+1
                LAC  MCWA
                RTR
                AND  (3
                SAD  TEMP+1
                JMP  SMFLDS
                JMS  FIELD
                XOR  (010000
                TAD  LLR
                SAD  ULTAR
                SKP
                JMP  HLTA-5

SMFLDS,         LAM  -7777
                TAD  ULTAR
                DAC  ULREG
                LAC  LLREG
                XOR  (010000
                DAC  SLREG
                DAC  WCREG
                DAC  LLREG
                JMP  I  TSFLD
                LAC  LLREG
                XOR  (010000
            DAC  SLREG
            DAC  WCREG
                JMP  I  TSFLD

HLTA,           0
                HLT
                JMP  I  .-2
FIELD,          0
                JMS  .+1
                0
                LAC  .-1
                AND  (070000
                LEM
                JMP  I  FIELD
```

```
/DETERMINE WHICH FIELD FOR 1ST MOVE
1STMV,          LAC MVCNT
                SAP
                SEL
                JMP EXTST
                LAC MVCNT
                SPA                        /IS THIS FIRST MOVE?
                JMP NXTMV                            /NO
                XOR (400000           /SET 1ST TIME FLAG
                DAC MVCNT
                LAS
                AND (3
                DAC TEMP
                LAC MCWA
                CLL
                RTR
                AND (3
                SAD TEMP                   /TEST FOR SINGLE BANK
                JMP FLD1                   /SINGLE
                LAC .
                AND (010000
                SZA
                JMP BEGIN+4
                LAC ULTAB
                TAD (760000
                DAC FLOADA
                TAD (760000
                DAC NXFLD
                JMS FIELD                        /PRESENT BANK
                DAC FLOAD
                SAD FLOADA             /DOES U.L. = BANK LOADED
                JMP SUB1          /YES. GO TO NEXT LOWER
```

```
CKERR,          DZM CNTA                    /CHECK FOR ERROR IN NEXT.
                ISZ .+1
                LAC FRWRD
                AND LLD
                SAD FLOADA                      /CHECK FOR ERROR IN BANK
                JMP ERFLD                           /YES
                LAC (3
                SAD CNTA
                JMP .+3                    /DONE CHECKING
                ISZ CNTA
                JMP CKERR+1
RSTOR,          LAC NXTOK
                DAC CKERR+2
                LAC FLOADA
                DAC TEMP                   /DESTINATION
                LAC FLOAD
                DAC TEMP+1                 /SOURCE
                SAD TEMP
                JMP BEGIN+4
                LAC KJMP
                DAC MVRJP
                JMP MOVE                   /MOVE PROGRAM
ERFLD,          XCT CKERR+2
                SNA
                JMP RSTOR-5
                AND (010000
                SZA
                JMP RSTOR-5
                JMP EQULL
SUB1.           LAC NXFLD                       /TRY NEXT BANK
                SAD FLOADA
                JMP EQULL+1
                DAC FLOADA
                SAD LLTAB
                JMP CKERR
                TAD (760000
                DAC NXFLD
                JMP CKERR
EQULL,          XCT CKERR+2
                AND LLD
                SAD LLTAB
                JMP .+10
                SNA
                SKP
                TAD (760000
                DAC NXFLD
                LAC NXTOK
                DAC CKERR+2
                JMP SUB1
                LAC NXTOK
                DAC CKERR+2
                JMP BEGIN+4
```

```
/DETERMINE NEXT PROGRAM MOVE.
NXTMV,          LAC SNGMV
                SPA                             /MOVE MADE WITHIN A FIELD
                JMP MVSBK                              /YES. MOVE BACK
                JMS FIELD
                DAC TEMP+1              /SOURCE
                DZM CNTA               /CHECK FOR ERROR
CHKNXT,         ISZ .+1
                LAC ERWRD
                AND LLD
                SAD NXFLD                       /ANY ERRORS?
                JMP ERNXT              /YES
                LAC (3
                SAD CNTA
                JMP NXTOK
                ISZ CNTA
                JMP CHKNXT
NXTOK,          LAC FRWRD
                LAC .-1
                DAC CHKNXT+1
                LAC NXFLD
                SAD FLOADA
                JMP .+3
                SAD LLTAB
                JMP MVBK
                SAD LLTAB
                JMP CORRCT
                DAC FLOADA
                TAD (760000           /NO CALCULATE NEXT
                DAC NXFLD
                LAC FLOADA
                DAC TEMP                        /DESTINATION
                LAC KJMP
                DAC MVRJP                        /SET RETURN FOR STOVER
                JMP MOVE
ERNXT,          XCT CHKNXT+1
                SNA                     /DOES ERROR = 000000
                JMP NXTOK-5                     /YES
                AND (010000
                SNA
                JMP SUB2
                JMP NXTOK                        /NO. MOVE PROGRAM
CORRCT,         LAC ULTAB
                TAD (760000
                DAC NXFLD
                DAC FLOAD
                JMP CHKNXT-1
```

```
/ROUTINE TO MOVE PROGRAM TO UPPER 4 K WITHIN ONE BANK.
FLD1,           LAC LLTAB
                SAD FLOADA                      / IS PROGRAM IN TESTED BANK
                JMP .+3
                DZM MVCNT                               /NO, DON'T MOVE
                JMP STOVER
                LAC .
                AND (010000
                SZA
                JMP MVSBK
                LAC (400000
                DAC SNGMV
                LAC KJMP
                DAC MVRJP
                DZM CNTA
CKUPR,          ISZ .+1
                LAC FRWRD
                AND LLD
                SAD LLTAB                               /ERROR PRESENT?
                JMP SNGERR
                LAC (3
                SAD CNTA                        /DONE CHECKING?
                JMP ERRTN                               /YES
                ISZ CNTA
                JMP CKUPR
ERRTN,          LAC NXTOK
                DAC CKUPR+1
                JMS FIELD
                TAD (20
                DAC TEMP+1                      /SOURCE
                XOR (010000                             /INCR. BY 4K
                DAC TEMP                        /DESTINATION
                LAC TEMP
START
```

/PDP-9 EXTENDED MEMORY TEST - PART 2

```
SNFLD,          DAC MOVED
                LAM -7756
                LAC LNGTH
                ISZ MOVED
                DZM I MOVED
                ISZ LNGTH
                JMP .-3
                LAC TEMP+1
                DAC MOVES
                LAC TEMP
                DAC MOVED
                DZM CNTA
ADJID,          ISZ .+1                    /ADJUST INDIRECTS
                LAC PRJP
                XOR (010000
                ISZ .+1
                DAC PRJP
                LAC (5
                SAD CNTA
                JMP SNMOVE
                ISZ CNTA
                JMP ADJID
MRINS,          LAC TEMP+2
                XOR (010000
                JMP MEMREF

SUB2,           LAC NXFLD
                SNA
                JMP .+11
                TAD (760000
                SAD FLOADA
                JMP .+3
                DAC NXFLD
                JMP NXTOK-5
                SZA
                JMP .-6
                JMP .-4
                LAC NXTOK
                DAC CHKNXT+1
                JMP REGIN+4
```

```
SNMOVE,          LAC PRJP
                 LAC .-1
                 LAC ADJID+1
                 XOR (244000
                 DAC ADJID+4
MVRTN,           ISZ MOVES
                 LAC I MOVES
                 DAC TEMP+2
                 AND (700000
                 XOR (700000
                 SZA                        /MEMORY REF INSTRUCTION?
                 JMP MRINS                       /YES
                 LAC TEMP+2
MEMREF,          ISZ MOVED
                 DAC I MOVED
                 SAD PROLTH                 /MOVED ALL INST?
                 SKP                        /YES.   NOW MOVE CONSTANTS
                 JMP MVRTN
MVCNST,          LAM -377
                 DAC KCNT
                 ISZ MOVES
                 LAC I MOVES
                 ISZ MOVED
                 DAC I MOVED
                 ISZ KCNT
                 JMP .-5
                 JMP STRTN                  /GO TO STOVER OR HLTST
SNGERR,          XCT CKUPR+1
                 AND (010000
                 SNA                        /ERROR IN UPPER 4K?
                 JMP ERRTN-5
                 LAC NXTOK
                 DAC CKUPR+1
                 JMP REGIN+4


/MOVE BACK TO ORIG. BANK
MVBK,            LAC NXFLD                        /ORIG. BANK
                 DAC FLOADA
                 DAC TEMP                   /DESTINATION
              JMS FIFLD
                 DAC TEMP+1                 /SOURCE
                 DZM LAST
                 DZM ERTAB
                 DZM MVCNT                        /CLEAR 1ST MOVE FLAG
                 JMP MOVE
/MOVE PROGRAM BACK TO LOWER 4K WHEN
/ONLY ONE BANK IS SELECTED.
MVSBK,           LAC FLOADA
                 DAC TEMP                   /DESTINATION
                 XOR (010000
                 DAC TEMP+1                 /SOURCE
                 DZM SNGMV                       /CLEAR FLAG FOR SAME BANK
                 DZM MVCNT                       /CLEAR MOVED 1ST TIME FLAG
                 LAC KJMP
                 DAC MVRJP
                 JMP CKFLD-1
```

```
/MOVE PROGRAM WHEN A FORCED MOVE
/IS SPECIFIED.

FCDMV,          STL
                CLK                     /SET FLAG FOR FORCED MOVE
                DAC MVCNT
                LAC MCWA
                CLL
                RTR
                RTR
                RTR
                AND LLD                 /MASK SELECTED BANK
                SAD FLOADA                  /IS MOVE WITHIN THIS BANK
                JMP FCDSGL                  /YES
                DAC TEMP                /DESTINATION
                JMS FIELD
                DAC TEMP+1              /SOURCE
                LAC MCWA
                AND (100
                SZA                     /MOVE TO UPPER OR LOWER 4K?
                JMP LDUPR                     /UPPER
                LAC TEMP                /LOWER
                DAC FLOADA
                LAC PRJP+3
                DAC MVRJP
                DZM CNTA                /CHECK FOR ERROR IN LOWER 4K
CKFLD,          ISZ .+1
                LAC ERWRD
                AND LLD
                SAD TEMP
                JMP FCDERR              /ERROR
                LAC (3
                SAD CNTA                /SEE IF DONE CHECKING
                JMP FMOVA                     /YES

                ISZ CNTA
                JMP CKFLD
FMOVA,          LAC NXTOK
                DAC CKFLD+1
                LAC .
                AND (010000
                SNA
                JMP MOVE               /LATERAL TRANSFER
LDLWR,          LAC TEMP               /NOT LATERAL
                TAD (20
                DAC TEMP               /DEST'N
            JMS FIELD
                TAD (20
                DAC TEMP+1             /SOURCE
                FEM
                JMP SNFLD-1
```

```
FCPERR,         XCT CKFLD+1
                SNA                             /=0
                JMP CKFLD+5
                AND (010000
                SZA                             /ERROR IN LOWER 4K
                JMP CKFLD+5
                LAC NXTOK
                DAC CKFLD+1
                LAC PRJP+2                      /YES
                DAC PRJP                        /SET RETURN FOR FMOVA
                JMP PSFL
LDUPR,          LAC TEMP
                DAC FLOADA
                DZM CNTA                        /CHECK FOR ERROR UPPER 4K
                ISZ .+1
                LAC ERWRD
                AND LLD
                SAD TEMP
                JMP UPRERR
                LAC (3
                SAD CNTA                        /DONE CHECKING?
                JMP UPRTN                               /YES
                ISZ CNTA
                JMP LDUPR+3
UPRTN,          LAC NXTOK
                DAC LDUPR+4
                LAC TEMP                        /DEST'N
                XOR (010000
                TAD (20
                DAC TEMP
                JMS FIELD
                TAD (20
                DAC TEMP+1                      /SOURCE
                LAC PRJP+3

                DAC MVRJP                                   /SET RETURN FOR HLTST
                LAC TEMP+1
                AND (010000
                EEM
                SNA                             /CHECK IF IN UPPER 4K
                JMP SNFLD-1             /IN LOWER
                LAC TEMP+1
                XOR (20
                DAC TEMP+1
                LAC TEMP
                XOR (20
                DAC TEMP
                JMP MOVE
UPRERR,         XCT LDUPR+4
                AND (010000
                SNA                             /ERROR IN UPPER 4K?
                JMP UPRTN-5            /NO.  MOVE PROGRAM
                LAC NXTOK
                DAC LDUPR+4
                LAC PRJP+1                      /YES
                DAC PRJP                        /SET RETURN FOR UPRTN
                JMP PSEL                        /PRINT "ERROR IN SELECTED 4K"
```

```
/FORCE MOVE PROGRAM TO UPPER OR LOWER 4K
/OF A SINGLE BANK

FCOSGL,     LAC FLOADA
            DAC TEMP                     /DEST'N
            DAC TEMP+1                   /SOURCE
            LAC .
            AND (010000
            SZA                          /IN LOWER 4K NOW?
            JMP CKFLD-3                          /NO.
            JMP LDUPR


/MOVE ROUTINE FOR A LATERAL TRANSFER
/FROM ONE BANK TO ANOTHER

MOVE.       FEM
            LAC TEMP
            DAC MOVED
            LAM -7756                    /4K DECIMAL
            DAC LNGTH
            ISZ MOVED
            CZM I MOVED
            ISZ LNGTH
            JMP .-3
            LAC TEMP+1                   /SOURCE
            XOR (20
            DAC MOVES
            LAC TEMP
            XOR (20
            DAC TEMP
            DAC MOVED
            LAC NXTOK
            DAC CKERR+2
            ISZ MOVES
            LAC I MOVES
            ISZ MOVED
            DAC I MOVED
            SAD PROLTH
            JMP MVCNST
            JMP .-6
STRTN,      LAC (7777
            AND MVRJP                            /MASK PRESENT FIELD
            XOR TEMP                     /INSERT DEST'N BANK #
            XOR (20
            DAC MVRJP
            JMP I MVRJP         /EXIT TO SPECIFIED ROUTINE
```

```
HLTST,          HLT                         /HALT HERE AFTER FORCED MOVE
                LAC (7777
                AND KJMP
                XOR TEMP                     /INSERT BANK #
                XOR (20
                DAC KJMP
                JMP I KJMP                   /EXIT TO STOVER
ERROR,          DAC TTY+2       /BAD DATA
                LAC PRJP+4
                DAC PRJP                     /SET RETURN FOR WCRJP
                LAC PATWD
                DAC TTY+3       /GOOD DATA
                LAC MPAT
                DAC TTY+4
                LAC WCREG
RTNERR,         DAC TTY+1       /ADDRESS
                AND (070000
                SAD LAST                     /SAME FIELD AS LAST?
                JMP SUPBIT+3    /YES
                LAC (4
                SAD ERTAB
                JMP SUPBIT+1
                ISZ ERTAB
                LAC TTY+1
RERWD,          DAC ERWRD+1
                ISZ .-1                      /STORE ADDRESS OF ERROR
                AND (070000
                DAC LAST
                JMP SUPBIT+3    /PRINT ERROR
SUPBIT,         DAC ERWRD+1
                LAC .-1
                DAC RERWD
                LAC TTY+2
                AND BITSUP
                SZA
                CMA
                AND BITSUP
                SZA                          /NEW BIT ERROR IF NOT ZERO
                JMP PRERR
                LEM
                JMP I PRJP

ERRORA.         DAC TTY+2                         /BAD DATA
                LAM
                DAC TTY+3                         /GOOD DATA
                LAC PRJP+5
                DAC PRJP                     /SET RETURN FOR SLRTN
                LAC PATWD
                DAC TTY+4
                LAC SLREG
                JMP RTNERR
```

```
PRERF,          LEM
                LAS
                AND  (LP
                SNA             /BELL ON ERROR?
                JMP  PERR       /NO
                LAW  207        /YES
                TLS
                TSF
                JMP  .-1
                JMP  I PRJP
PERR,           LAS
                AND  (200000
                SZA             /PRINT?
                JMP  I PRJP         /NO
                DZM  PRINT
                LAM  -5
CHARA,          DAC  SPCNT
                JMP  FIRST
                LAW  240        /SPACE
                TLS
                TSF
                JMP  .-1
                ISZ  SPCNT                 /9 SPACES
                JMP  .-5        /NO
                LAM  -5
                DAC  SPCNT
                LAC  PRINT
                SZA             /1ST CHAR.?
                JMP  PRDATA     /NO
FIRST,          LAC  TTY        /TEST NO
                ISZ  PRINT
                JMP  CHARA+3
PRDATA,         ISZ  .+1
                LAC  TTY
                DAC  TEMP+2
ONMOR,          LAW  260
                DAC  TTYS
                LAM  -77777
                AND  TEMP+2     /MASK AC0-2

                CLL
                RTL
                RTL
                TAD  TTYS       /ASSEMBLE CHARACTER
                DAC  TTYS
                LAC  TEMP+2
                RTL             /POSITION NEXT OCTAL CHAR
                RAL

                DAC  TEMP+2
                LAC  TTYS
                TLS             /PRINT 1 OCTAL NO
                TSF
                JMP  .-1
                ISZ  CHAR6                  /SIX FIGS YET?
                JMP  ONMOR                  /NO
```

```
                LAM  -5                      /-6
                DAC  CHAR6
                ISZ  PRINT                              /SET UP FOR NEXT
                LAC  PRINT
                SAD  (5
                SKP
                JMP  CHARA+2

JONPR,          LAC  TTY
                LAC  .-1
                DAC  PRDATA+1
                DZM  PRCNT
                DZM  PRINT
OOONF,          JMS  KRLLF
                LAS
                SMA                          /CHECK FOR HALT ON ERROR
                JMP  SUPRES
                JMS  HLTA
                LAS
                AND  (200
                SZA
                JMP  SUPRES+4
                LAS
                SAD  MCWB                    /CHECK FOR PARAM. CHANGE
                JMP  I PRJP                      /NO CHANGE
                JMP  STOVER
KRLLF,          0                            /CR, LF
                ISZ  .+1
                LAC  CRLF
                TLS
                TSF
                JMP  .-1
                ISZ  PRCNT
                LAC  (2
                SAD  PRCNT
                SKP
                JMP  KRLLF+1
                LAC  CRLF
                LAC  .-1
                DAC  KRLLF+2
                DZM  PRCNT
                JMP  I KRLLF

SUPRES,         LAS                          /BIT SUPPRESSION
                AND  (200
                SNA                          /BIT 10?
                JMP  I PRJP                  /NO READ ANOTHER
                JMS  KRLLF                           /YES CRLF
                DZM  SCW
                CAF
                KSF                          /WAIT FOR FIRST CHAR.
                JMP  .-1
```

```
AGAIN,          KRB                             /READ BUFFER
                SAD (212                        /CHECK FOR LINEFEED
                JMP I PRJP                           /YES. CONT WITH NO CHANGES
                DAC TTYIN
                LAM -677
                AND TTYIN
                SZA                             /ERROR? RO=ERROR
                JMP OPERR
                LAC CRLF+1
                XOR TTYIN
                SNA                             /EOT? EOT=CR
                JMP EOT                         /YES
                LAC (254
                XOR TTYIN
                SNA                             /EOM? EOM=COMMA
                JMP WAIT                        /YES
                JMS CIFOK                            /TEST VALIDITY
                JMP WAIT                        /NOT VALID
                SNA                             /CHAR.=0?
                JMP ZERO                        /YES
                DAC TTYW
ILLEGL,         KSF                             /WAIT FOR ANOTHER
                JMP .-1
                KRB
                DAC TTYIN
                LAC (254
                XOR TTYIN
                SNA                             /EOM?
                JMP EOM                         /YES
                LAC CRLF+1
                XOR TTYIN
                SNA                             /EOT?
                JMP EOTA                        /YES
                LAM -677
                AND TTYIN
                SZA                             /ERROR?
                JMP OPERR                                /YES
                JMS CIFOK                                /TEST VALIDITY
                JMP ILLEGL                      /NOT VALID
                DAC TTYX                        /OK
                LAC TTYW
                RCL         RCL         RCL

                XOR TTYX                        /COMBINE DIGITS
                CMA
                DAC TTYY
                LAM
                TAD TTYY                        /SUB. 1
ROTOR,          DAC TTYY
                LAC (40000
                RCR                             /SHIFT BIT
                ISZ TTYY                        /IN POSITION?
                JMP .-2                         /NO
                XOR SCW                         /YES
                DAC SCW
WAIT,           KSF
                JMP .-1
                JMP AGAIN
```

```
OPERR,       DZM  SCW                    /CLEAR ALL BITS
             JMP  .-4
EOT,         LAC  SCW                    /ALL DONE SELECTING
             CMA
             DAC  BITSUP
             DZM  SCW
             JMS  KRLLF                                /CR,LF
             LEM
             JMP  I PRJP
EOM,         LAC  TTYW
             CMA
             TAD  (1                     /2'S COMPLEMENT
             JMP  ROTOR
EOTA,        LAC  TTYW
             CMA
             TAD  (1                     /2'S COMPLEMENT
             DAC  TTYY
             LAC  (400000
             RCR
             ISZ  TTYY
             JMP  .-2
             XOR  SCW
             JMP  EOT+1
ZERO.        LAC  SCW
             XOR  (400000
             DAC  SCW
             JMP  WAIT
CIFOK,       0                           /TEST VALIDITY
             LAC  TTYIN
             RCR          RCR       RCR
             XOR  (26
             SZA                         /CHAR.=26X?
             JMP  .+5
             ISZ  CIFOK                          /OK
             LAC  TTYIN
             AND  (7
             JMP  I CIFOK                        /SEE IF CHAR. = 8 OR 9
             SAD  (1
             SKP
             JMP  I CIFOK                    /NO
             LAW  1                   /YES
             AND  TTYIN
             SZA                      /DOES IT = 8
             JMP  .+3
             LAM  -7                  /YES
             JMP  ROTOR
             LAM  -10                 /=9
             JMP  ROTOR
```

```
/PRINT L.L. EXCEEDS U.L.
PREXD,          JMS KRLLF                            /CR
                LAM -12                     /-9 DECIMAL
                DAC PRCNT
                ISZ .+1
EXCDP,          LAC EXCEED
                TLS                         /PRINT 1 CHAR
                TSF
                JMP .-1
                RTR                         /SETUP FOR NEXT
                RTR
                RTR
                RTR
                TLS                         /PRINT 2ND
                TSF
                JMP .-1
                ISZ PRCNT                           /DONE?
                JMP EXCDP-1                          /NO
EXHLT,          JMS KRLLF
                LAC EXCEED
                LAC .-1
                DAC EXCDP
                JMS HLTA
                JMP STOVER                  /READ PARAMETERS AGAIN

/PRINT ERROR IN SELECTED 4K

PSEL.           LAC MVCNT
                RAR
                SNL
                JMP BEGIN+4
                DZM PRINT
                LAM -12                     /11 DECIMAL
                DAC PRCNT
                ISZ .+1
PSELR,          LAC PSLCE
                TLS                         /PRINT 1 CHAR
                TSF
                JMP .-1
                RTR                         /SETUP FOR NEXT
                RTR

            RTR
                RTR
                TLS
                TSF                         /PRINT 2ND
                JMP .-1
                ISZ PRCNT                           /DONE?
                JMP PSELR-1                         /NO
```

```
PSLHIT,      JMS KRLLF
             LAC PSLCE
             LAC .-1
             DAC PSELR
             JMS HLTA
             LAS                        /READ PARAMS.
             AND (143   /MASK NEW
             DAC TEMP+2
             LAC MCWA
             AND (143   /MASK OLD
             SAD TEMP+2                      /SAME?
             JMP I PRJP                 /YES, MOVE ANYWAY
             JMP STOVER                      /NO. DECODE NEW PARAMS
PROLTH,      776777                     /FLAG TO SIGNAL WHEN TO MOVE
                                        /THE CONSTANT TABLE
/CONSTANTS AND STORAGE REGISTERS

FLOAD,       0             /MEMORY BANK FIRST LOADED WITH PROGRAM
FLOADA,      0             /PRESENT BANK CONTAINING PROGRAM
TEMP,        0             /UTILITY STORAGE
             0
             0
MCWA,        0             /STORAGE FOR PARAMETER ENTRIES
MCWB,        0             /SAME AS MCWA
ULREG,       0             /STORAGE FOR UPPER LIMIT MEMORY ADDRESSES
ULTAB,       0             /SAME AS ULREG
LLREG,       0             /STORAGE FOR LOWER LIMIT MEMORY ADDRESSES
LLTAB,       0             /SAME AS LLREG
CLREG,       0             /ADDRESS REG. FOR CONT. LOAD LOOP
CREG,        0             /ADDRESS REG. FOR CONT. READ LOOP
WCREG,       0             /CURRENT MCS ADDRESS REG. FOR CHECKERBOARD
SLREG,       0             /CURRENT MCS ADDRESS REG. FOR SLIDING ZERO
NXFLD,       0             /BANK WHICH WILL NEXT CONTAIN PROGRAM
CNTA,        0             /UTILITY COUNTER
ERWRD,       0             /ERWRD+1 THRU +4 STORES FIRST ERROR
                                /ENCOUNTERED IN ANY BANK
             0
             0
             0
             0
LAST,        400000        /WILL INDICATE LAST BANK IN WHICH AN
                                /ERROR WAS FOUND
MVCNT,       0             /BITS 0 AND 17 TELL IF A MOVE WAS MADE
                                /AS YET AND IF IT WAS FORCED
WC18,        0             /SHIFT COUNTER
READ40,      777760
```

```
SNGMV,        0        /INDICATES IF A MOVE WITHIN ONE BANK
                           /HAS TAKEN PLACE
LNGTH,        0        /USED TO CLEAR A MOVE DESTINATION TO 0'S
PATR.         0        /TEMP. STORAGE OF PATTERN FOR SLIDING ZERO
PATWD,        0        /TEMP. STORAGE OF PATTERN FOR CHECKERBOARD
PAT.          737720   /STORAGE FOR PATTERN CONTROL WORD
KPAT.         037720   /KPAT TO KPAT+3 ARE CONTROL WORDS FOR CHECKERBOARD
              037721
              740076
              740077
LLA,          0        /LLA THRU ULD = L.L. AND U.L. BANK ADDRESSES
LLB,          020000
LLC,          040000
LLD,          060000
ULD,          100000
NC8K.         760000   /COUNTER TO INDICATE END OF AN 8K BANK
NC64.         777700   /COUNTER FOR 64 128 WORD BLOCKS
NC128,        777770   /COUNTER FOR 8 16 WORD BLOCKS
NC16.         777760   /SHIFT COUNTER
NC20.         777772   /COUNTS 10 READS FOR EACH LOCATION
PRJP,         0        /PRJP+1 THRU +5 ARE RETURN JUMP ADDRESSES
              UPRTN
              FMOVA
              HLTST
              KCRJP
              SLRTN
BASE.         LOCN+1   /USED TO CALCULATE L.L. & U.L. FROM ACS 14-17
MVRJP,        HLTST    /MVRJP AND KJMP USED DURING PROGRAM MOVE
KJMP.         STOVER
KCNT.         0        /USED WHEN MOVING THE CONSTANT TABLES
NC256,        777776   /COUNTER FOR 2 - 128 WORD BLOCKS
TTYIN,        0        /TTYIN THRU TTYY USED AS TEMP. STORAGE IN
                           /BIT SUPPRESSION LOOP
TTYW.         0
TTYX.         0
TTYY.         0
SCW,          0        /TEMP. STORAGE OF SUPRESSED BITS
BITSUP.       0        /PERMANENT STORAGE OF SUPRESSED BITS
ERTAB,        0        /COUNTER FOR # OF TIMES THE ERROR WORD
                           /TABLE IS ENTERED.  MAX. = 4
LO4KIL.       0        /LO4KLL THRU HI4KUL ARE USED AS ADR REGS
                           /FOR SINGLE BLOCKS
LO4KUL.       0
HI4KIL.       0
HI4KUL.       0
RSTPAT.       037700   /RESTORES CONTROL WORD IN KPAT
MOVES,        0        /STORES SOURCE ADDRESS FOR RELOCATION
MOVED,        0        /STORES DEST'N ADDRESS FOR RELOCATION
```

/CONSTANTS FOR TTY PRINT-OUT

```
TTYS.            0
TTY,             0
                 0
                 0
                 0
                 0
PRINT,           0
SPCNT,           0
PRCNT,           0
ENTXT,           PRTXT
PRTXT,
                 .
                 2
                 7
                 13
                 20
CHAR6,           777772
CRLF.            0
                 200215
                 200212


PHDR.            JMS KRLLF                              /HEADER ROUTINE
                 ISZ .+1
                 LAC HDRWRD
                 SMA
                 JMP .+6
                 LAC HDRWRD
                 DAC PHDR+2
                 JMS KRLLF
                 JMS HLTA
                 JMP BEGIN
                 TLS                          /PRINT 1 CHAR.
                 TSF
                 JMP .-1
                 RTR        RTR        RTR
                 RTR        RAR
                 TLS
                 TSF
                 JMP .-1
                 JMP PHDR+1
```

/TEXT FOR L.L. EXCEEDS U.L.

EXCEED,   0
                 127314
                 127314
                 142640
                 141730
                 142705
                 151704
                 152640
                 146256
                 106656

/TEXT FOR ERROR IN SELECTED 4K

PSLCF,   0
                 105215
                 151305
                 147722
                 120322
                 147311
                 151640
                 146305
                 141705
                 142724
                 120304
                 145664

/TEXT FOR HEADER

HDRWRD,   LAC HDRWRD
                 305324
                 324323
                 240240
                 303317
                 301324
                 240314
                 304301
                 256322
                 240240
                 240240
                 301302
                 240304
                 240240
                 240240
                 240240
                 307240
                 317317
                 240304
                 240240
                 240240
                 240240
                 320240
                 324301
                 240256
                 400000

PAUSE FHDR

ADJID	1366	EXIST	72
ADJUL	1443	FCDERR	1564
ADJUST	1424	FCDMV	1505
ADR	176	FCDSGL	1654
ADRA	247	FIELD	1102
ADRJP	147	FIRST	2042
ADRMP	152	FL01	1312
AD01	146	FLOAD	2424
AD02	167	FLOADA	2425
AD03	171	FMOVA	1546
AD04	173	HDRWRD	2631
AD05	175	HI4KIL	2525
AD06	202	HI4KUL	2526
AD07	204	HLTA	1077
AD08	206	HLTST	1723
AD09	213	ILLEGL	2202
AD10	215	INHI4K	713
AGAIN	2155	KCNT	2512
BASE	2507	KJMP	2511
BEGIN	21	KPAT	2463
BITSUP	2521	KRLLF	2124
CHARA	2025	LAST	2452
CHAR6	2551	LCNTA	361
CHKNXT	1242	LDLWR	1554
CIFOK	2303	LDUPR	1577
CKERR	1150	LDWRD	276
CKFLD	1534	LLA	2467
CKUPR	1330	LLB	2470
CLOOP	642	LLC	2471
CLREG	2437	LLD	2472
CNTA	2444	LLREG	2435
CNTB	367	LLTAB	2436
CORRCT	1305	LNGTH	2457
CREG	2440	LOCN	125
CRLF	2552	LO4KLL	2523
CROOP	1000	LO4KUL	2524
DONJMP	774	MCWA	2431
DONL8K	425	MCWB	2432
DONPR	2102	MEMREF	1436
DONPRT	747	MOVE	1664
DONR8K	553	MOVED	2531
DONXT	625	MOVES	2530
DOONF	2107	MPAT	2462
ENTXT	2543	MRINS	1400
EOM	2261	MV8K	1463
EOT	2252	MVCNST	1443
EOTA	2265	MVCNT	2453
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ERNXT	1276	MVSBK	1474
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EXHLT	2353	PERR	2017

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RONES	731		WC20	2500
ROTOR	2236		WC256	2513
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SLOOP	270		AD02	167
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SLRTN	313		AD04	173
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SNFLD	1352		ADR	176
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SNGMV	2456		AD07	204
SNMOVE	1421		AD08	206
SPCNT	2541		ADRA	207
SRDON	334		AD09	213
STOVER	43		AD10	215
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SUB2	1403		RTSTC	265
SUPBIT	1760		SLOOP	270
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TTY	2533		DONL8K	425

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CLOOP	642		RERWD	1753
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LO4KUL    2524
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