Digital Equipment Corporation
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digital

PDP-15 Systems
Maintenance Manual

Volume 1

TC59 Magnetic Tape Transport Control

DEC-9A-I3BC-D

PDP-15 SYSTEMS
TC59 MAGNETIC TAPE TRANSPORT CONTROL MAINTENANCE MANUAL VOLUME 1

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CHAPTER 1
INTRODUCTION AND DESCRIPTION

1.1 INTRODUCTION

This manual, together with the documents referenced, provides operation and maintenance information for the TC59 Magnetic Tape Transport Control. It is assumed that the user is familiar with the PDP-9 or PDP-15 Programmed Data Processor and has a working knowledge of DEC logic symbology.

The TC59 controls up to eight magnetic tape transports that conform to the transport bus specification, such as those listed in the following chart:

Type	Characteristics
TU20A, TU20B	9- or 7-track, 45 ips, 36 kHz maximum characters
TU30A, TU30B	9- or 7-track, 75 ips, 60 kHz maximum characters
TU10	9- or 7-track, 45 ips, 36 kHz maximum characters

The TC59 can mount anywhere within a standard 19-in. cabinet and contains three standard DEC Type 1943 Mounting Panels and one standard 5-1/4 in. indicator panel. The total system requires four mounting panel locations.

1.2 PURPOSE OF EQUIPMENT

The TC59 consists of tape control logic, which, under the direction of the PDP-9 or PDP-15, controls the operation of up to eight magnetic tape transport units. The TC59 operates under program control to transfer data between core memory and the selected tape transport. To transfer data to or from core memory, the TC59 uses the data channel facility of the processor; the data channel WC (word count) register specifies the record length (number of words) and the CA (current address) register specifies the starting core memory address of the data transfer.

The TC59 functions in either 7-track operation or 800 bpi 9-track operation; either 200, 556, or 800 bpi density modes are selectable in 7-track operation. It can operate in either binary or BCD parity mode. For writing on tape, the 18-bit data words are transferred from core memory to the data buffer in the tape control logic. The data buffer logic supplies the character to the tape transport write logic as three 7-bit (6-bit character plus parity bit) characters for 7-track operation or two 9-bit characters for a 9-track operation. For reading, the sequence is reversed, information is read from tape as 7-bit characters and is sent to the data buffer. When a complete 18-bit word has been assembled in the data buffer, a data-channel break (word transfer) is initiated to transfer the data buffer word into core memory.

The operations that can be performed by the tape transport, under the control of the TC59, are as follows.

REWIND	The transport rewinds the tape to the load point and stops.
WRITE	N words are written on tape as specified by the 2's complement of the WC register. The CA register specifies the memory block address.
WRITE EOF	An EOF (end-of-file) mark character, 17_8 for 7-track or 23_8 for 9-track, is written on tape.
READ	N words are read from tape as specified by the 2's complement of the WC register. The CA register specifies the memory location which is to receive the words.
READ/COMPARE	N words are read from tape as specified by the 2's complement of the WC register. After each complete word is read, it is compared to a word in memory (specified by CA) producing a read-compare error when they do not compare.
SPACE FORWARD	The tape is spaced forward N records as specified by the 2's complement of the WC register. If EOT (end-of-tape) or EOF is encountered, the tape stops.
SPACE REVERSE	The tape is spaced in reverse for N records as specified by the 2's complement of the WC register. If BOT (beginning-of-tape) or EOF is encountered, the tape stops.

1.3 7-TRACK TAPE FORMAT

The 7-track system uses 1/2 in. tape with seven information tracks as shown in Figure 1-1. The left side of the figure shows the tape in relation to the read and write heads. The tape moves by the heads vertically, with forward direction down. The tape is composed of a mylar base coated on one side with an iron oxide composition. The oxide, or dull side of the tape, faces the heads with the left edge toward the transport drive plate. The recording density is 200 cpi (characters per inch), 556 cpi, or 800 cpi. The method of recording is nonreturn-to-zero (NRZ).

Although the tape has two basic states of remanent magnetization, the remanent magnetic state of the tape at a given position does not determine the value of the bit. A logical 1 is represented by a change of magnetization in either direction. A logical 0 is represented by a constant state of magnetization; therefore, writing a series of characters containing all 0s is equivalent to writing a section of blank tape. Each time a character is transferred into the tape transport write buffer, the NRZ writers produce an equivalent character on the tape. Because of the NRZ method of recording, however, a transfer into the write buffer is not a normal 1s transfer; instead, whenever a 1 bit is to be written in a given tape track, the corresponding flip-flop is complemented to produce a change in the tape magnetization. When a 0 is to be written, the corresponding bit of the buffer remains in the initial stage, and there is no change in tape magnetization.

The structure and relative spacing of the individual tape characters are shown in the right portion of Figure 1-1. Each 18-bit computer word is divided into three 6-bit characters. The writers contain seven flip-flops, however, corresponding to the seven tape tracks. The seventh track is a lateral parity track. The parity of the character may be either odd (binary) or even (BCD) as specified by the program. The smallest unit of information that can be written on the tape is a record. Because each computer word contains three 6-bit characters, a record contains N x 3 data characters, where N is the number of words that the processor transfers.

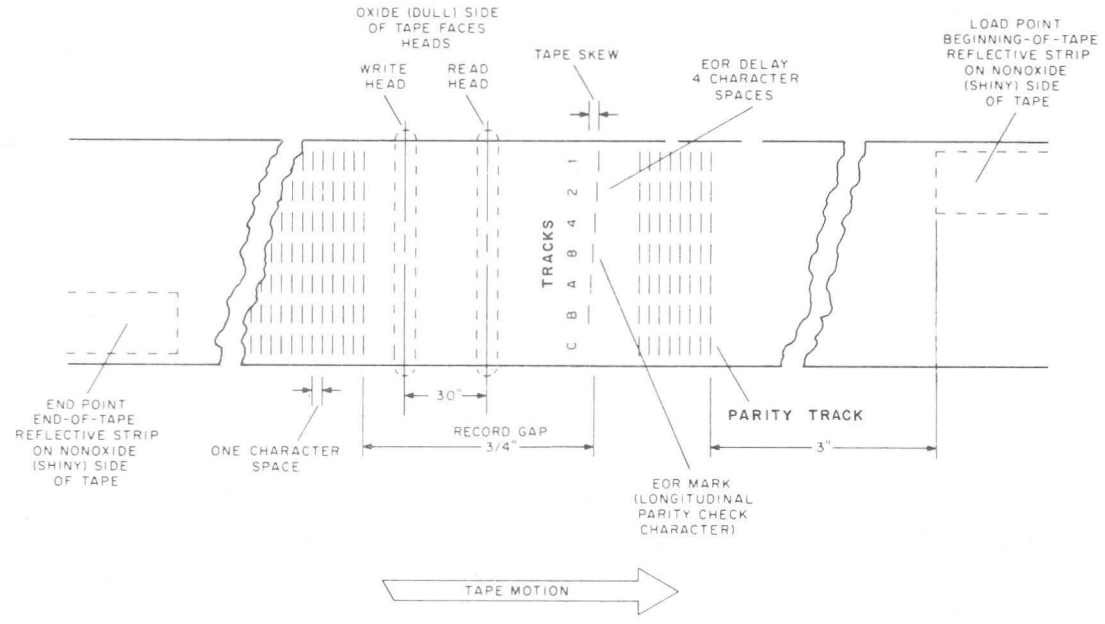


Figure 1-1 7-Track Tape Format

After the last data character of the record is written the tape travels four character spaces of blank tape (EOR gap), and then clears the write buffer to produce an end-of-record character, the EOR mark. The bit configuration of the EOR mark produced by clearing the write buffer leaves an even number of 1 bits in each of the seven tracks. All bits of the write buffer start in the 0 state; to end in the 0 state, they must undergo an even number of transitions. For this reason, the EOR mark is referred to as the longitudinal parity-check character. Besides detecting changes in magnetization through the read heads, the tape transport also includes a photoelectric system for sensing the beginning and end of the tape.

1.3.1 Load Point and End Point

The load and end points of the tape are marked by reflective strips mounted on the side of the tape away from the head (Figure 1-1). These strips are detected by photo diodes that sense light reflected from them. In writing on a newly mounted or rewound tape, a gap of about 6 in. is left from the load point before writing can begin. When load point is sensed during a fast rewind condition, the sensing device shuts off the high speed rewind. Before the tape movement stops, however, the load point will be passed and the forward tape motion will be enabled to advance the tape back to the load-point strip.

1.4 9-TRACK TAPE FORMAT

The 9-track tape format shown in Figure 1-2 is similar to 7-track format except that 9-track format has 9 tracks, the addition of the CRC (cyclic redundancy check) character, and operation is only in the 800 bpi mode.

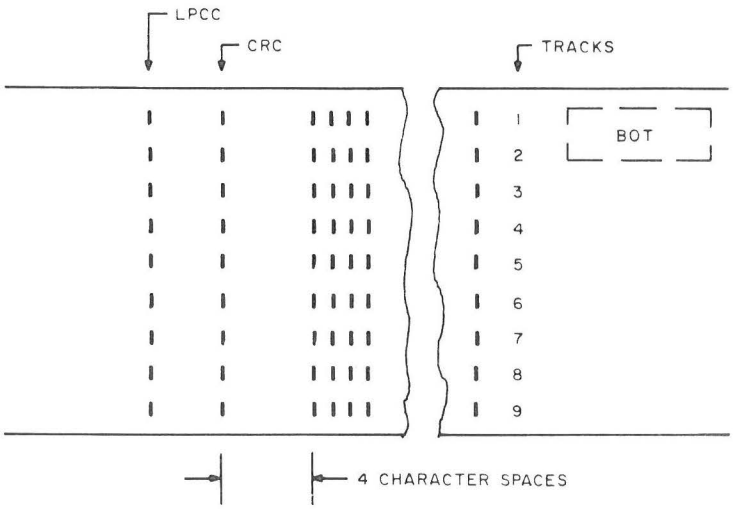


Figure 1-2 9-Track Tape Format

The tape control assembles two 8-bit characters per 18-bit word for recording on tape. Each 8-bit character is recorded with a parity bit which can be either odd or even. The first character recorded contains the most-significant bits of the 18-bit processor word. Because two characters represent 16 bits of information, the first two bits are not recorded on the tape or read back from the tape transport as data. Therefore, the first character represents bits 2 through 9. The second character represents bits 10 through 17. While reading, the parity of the first character is stored in bit 0, and the parity bit of the second character is stored in bit 1. This allows the program to perform error detection.

1.4.1 CRC Character

To write the CRC character, the TC59 control incorporates a 9-position register C_1 through C_9 with the following track assignments:

Register Position	C1	C2	C3	C4	C5	C6	C7	C8	C9
Track Number	4	7	6	5	3	9	1	8	2

To derive the CRC character, all data characters are exclusive-ORed into the CRC register. Between character transfers, the CRC is shifted one position, C_1 to C_2, etc., and C9 to C1. If shifting causes a 1 in C1, then the bits shifted into C4, C5, C6, and C7 are inverted. After the last data character has been added (exclusive-ORed), the CRC register is again shifted and if C1 is a 1, C4, C5, C6, and C7 are inverted.

To write the CRC character on tape, all bit positions except C4 and C6 are inverted. The parity of the CRC character will be odd if the number of data characters within the block is even, and even if the number of data characters within the block is odd. The CRC character may contain all 0 bits, in that case the number of data characters was odd.

The LPCC character for 9-track format is the same as for 7-track format.

1.5 REFERENCE DOCUMENTS

Table 1-1 lists reference documents that contain information related to the TC59 Magnetic Tape Transport Control.

Table 1-1
Reference Documents

Title	Document No.	Contents
PDP-9 User Handbook	F-95	Operation and programming information for the PDP-9.
PDP-9 Maintenance Manual Volumes I and II	F-97	Operation and maintenance information for the PDP-9, including engineering drawings.
Digital Logic Handbook	C-105	Specifications and descriptions of most FLIP CHIP modules, plus simplified explanation of the selection and use of these modules in numerous applications.
TU20 Instruction Manual	DEC-00-I4AA-D	Operation and maintenance information for the TU20 tape transport.
TC59 Instruction Test	MAIN DEC-9A-D4AB-D	Operating instructions and program listing for the TC59 diagnostic program.
PDP-15 Interface Manual	DEC-15-H0AB-D	Describes PDP-15 multicycle data channel interface.
PDP-15 User's Handbook, Volume I	DEC-15-H2DB-D	Lists API channel/priority assignments and IOT device selection codes for TC59.

CHAPTER 2
OPERATION AND PROGRAMMING

2.1 INTRODUCTION

The TC59 controls the operation of a maximum of eight magnetic tape transports. The TC59 uses the processor data channel facility to transfer data between system core memory and magnetic tape. The data transfers are controlled by the memory-resident word counter (WC) and current address (CA) registers associated with the assigned data channel. The TC59 is assigned memory location 32_8 and 33_8 for WC and CA, respectively. The CA is incremented before each data transfer; therefore, the initial contents should be set to the desired initial address minus one. The WC is also incremented before each transfer and must be set to the 2s complement of the desired number of data transfers. In this way, the word transfer that causes the word count overflow (WC becomes 0) is the last transfer to take place.

To control operation, the TC59 maintains a command register (Table 2-1). The program specifies the desired operation by transferring control data (unit selection, density, mode, etc.) from the AC to the command register using IOT instructions (refer to Table 2-2). Tape status information (EOT, BOT, error flags) can be read into the AC from the control unit by IOTs. Similarly, the control unit command register can be read into the AC.

During normal data reading, the control assembles 18-bit computer words from successive frames read from the information channels of the tape. During normal data writing, the control disassembles 18-bit words and distributes the bits so that they are recorded on successive frames of the information channels. The control provides for selection of three recording densities: 200, 556, and 800 bpi.

Although any number of tapes may be simultaneously rewinding, data transfer may take place to or from only one transport at any given time; data transfer includes these functions: read, write, write EOF (end-of-file), read/compare and space. When any of these functions are in process, the tape control is in the not ready condition. A transport is said to be not ready when tape is in motion, when transport power is off, or when it is off-line.

Data transmission may take place in either odd-binary or even-BCD parity mode. When reading a record with an odd number of characters (not divisible by 3), the final characters come into memory left justified.

Fifteen bits in the magnetic tape status register retain error and tape status information. Some error types are combines, such as lateral and longitudinal parity errors (parity checks occur after both reading and writing of data) or have a combined meaning such as illegal, for maximal use of the available bits.

Table 2-1
TC59 Command Register Control Data

UNIT SELECTION	ODD PARITY	CORE DUMP	EXTEND	COMMAND**	INTERRUPT ENABLE	DENSITY
0 1 2	3	4†	5*	6 7 8	9	10 11

†Bit 4 specifies core dump which causes a 9-track tape transport to operate as a 7-track tape transport.

*Bit 5 specifies write extended interrecord gap whereby 3 in. of blank tape is erased (or passed over) before recording occurs.

**Bits 6, 7 and 8 decoding is as follows:

BITS			COMMAND
6	7	8	
0	0	0	NO OP
0	0	1	REWIND
0	1	0	READ
0	1	1	READ/COMPARE
1	0	0	WRITE
1	0	1	WRITE EOF
1	1	0	SPACE FORWARD
1	1	1	SPACE REVERSE

***Bits 10 and 11 are decoded as follows:

BITS		DENSITY
10	11	(BPI)
0	0	200
0	1	556
1	0	800
1	1	800/9-TRACK

2.2 IOT INSTRUCTIONS

Table 2-2 lists the IOT instructions for the TC59.

Table 2-2
TC59 Control IOT Instructions

Mnemonic	Octal Code	Description
MTSF	707341	Skip on error flag or magnetic tape flag. The states of the error flag (EF) and the magnetic tape flag (MTF) are sampled. If either or both are set to 1, the content of the PC is incremented by one to skip the next sequential instruction.
MTCR	707321	Skip on tape control ready (TCR). If the tape control is ready to receive a command, the PC is incremented by one to skip the next sequential instruction.
MTTR	707301	Skip on tape transport ready (TUR). The next sequential instruction is skipped if the tape transport is ready.
MTAF	707322	Clear the status and command registers, and the EF and MTF, if TCR. If not, TCR clears MTF, EF flags only.
MTCM	707324	Inclusively OR the contents of the AC bits 0 through 5, 9 through 11 into the command register; JAM transfer bits 6, 7, 8 (command function).
MTLC	707326	Load the contents of AC bits 0 through 11 into the command register. (MTLC is the summation of MTAF and MTCM.)
--	707342	Inclusively OR the contents of the status register into bits 0 through 11 of the AC.
MTRS	707352	Read the contents of the status register into bits 0 through 16 of the AC.
--	707302	Inclusively OR the contents of the command register into bits 0 through 11 of the AC.
MTRC	707312	Read the contents of the command register into bits 0 through 11 of the AC.
MTGO	707304	Set "go" bit to execute command in the command register, if command is legal.

The magnetic tape status register reflects the state of the currently selected tape unit. Therefore, other units which may be rewinding, for example, will not interrupt when done.

2.3 MAGNETIC TAPE FUNCTIONS

The magnetic tape functions are specified by bits 6, 7, and 8 of the command register. When any of the tape functions has completed its data operation (after the end-of-record character passes the read head) the MTF (magnetic tape flag) is set, an interrupt occurs (if enabled), and errors are checked. The following paragraphs define the tape functions.

2.3.1 No Operation

A NO OP command defines no function in the command register. An MTGO instruction with NOP specified by the command register causes an illegal error.

2.3.2 Space

There are two commands for spacing records — space forward and space reverse. The 2s complement of the number of records to be spaced is loaded into the WC register. The CA register need not be set. The space function terminates when a WC overflow occurs, or EOF (end-of-file) or EOT (end-of-tape), whichever occurs first; the MTF (job done) flag is set and, if enabled, an interrupt occurs. When issuing a space command, the density bits must be set to the density in which the records were originally written. For IBM compatibility, BOT (load point or beginning-of-tape) detection during a backspace terminates the function with the BOT bit set. If a reverse command is given when a transport is at BOT, the command is ignored, the illegal error and BOT bits are set, and an interrupt (if enabled) occurs.

2.3.3 Read Data

Records may be read into memory only in the forward mode. Both CA and WC must be set; CA to the initial core address -1; WC to the 2s complement of the number of words to be read. Both the density (bits 10 and 11) and parity (bit 3) must be specified.

If WC is set to less than the actual record length, only the number of words specified by the WC register are transferred into memory. If WC is greater than or equal to the actual record length, the entire record is read into memory. In any case, both parity checks are performed. The MTF is set, and an interrupt (if enabled) occurs after the LPCC mark passes the read head. If either lateral or longitudinal parity errors or bad tape have been detected, or if an incorrect record-length error occurs (WC not equal to the number of words in the record), the appropriate status bits are set; but the interrupt occurs only when the MTF is set.

To continue reading without tape stopping, issue MTAF (clear MTF) and then issue MTGO. If the MTGO is not given before the shut down delay terminates, the transport will stop.

2.3.4 Write Data

Data may be written on magnetic tape in the forward direction only. For the write data function, CA, WC, and density and parity must be set. The write function is controlled by the WC, such that when WC overflows, data transfer stops, and the EOR (end-of-record or LPCC) character and IRG (inter-record = gap) are written. The MTF is set after the EOR has passed by the read head. To continue writing, MTAF and MTGO must be issued before the shut down delay terminates. If any errors occur, the EF (error flag) will be set when the MTF is set.

2.3.5 Write EOF

The write EOF command transfers a single file-mark character (17_8 for 7-track or 23_8 for 9-track) to magnetic tape plus the EOR character. CA and WC are ignored for write EOF. The density bits must be set and the command register parity bit should be set to even (BCD). If it is set to odd, the control will automatically change it to even. After the EOF marker is detected by the read head, the MTF is set and an interrupt (if enabled) occurs. The tape transport stops, and the EOF status bit is set confirming the writing. If odd parity is required after write EOF, it must be specifically requested through the MTLC command.

2.3.6 Read/Compare

The read/compare function compares tape data with core memory data. It can be useful for searching and positioning a magnetic tape to a specific record, such as a label or leader, whose content is known in core memory or to check a record just written. Read/compare occurs in the forward direction; CA, WC, parity, and density must be set. Each word read from tape is compared to the memory location specified by CA. If there is a comparison failure, CA incrementation stops and the read/compare error bit is set in the status register. Tape motion continues to the end of the record when the MTF is set and the interrupt (if enabled) occurs. If there has been a read/compare error, examination of the CA reveals the word that failed to compare.

2.3.7 Rewind

The high-speed rewind command does not require setting of the CA or WC. Density and parity settings are also ignored. The rewind command rewinds the tape to loadpoint (BOT) and stops. Another unit

may be selected after the command is issued and the rewind is in process. MTF is set and an interrupt occurs (if the unit is selected) when the unit is ready to accept a new command. The selected unit's status can be read to determine or verify that rewind is in progress.

2.3.8 Write Extended Inter-Record Gap

This feature, which occurs when bit 5 of the command register is set, permits a 3-in. interrecord gap to be produced before a record is written. Using this feature, areas of bad tape can be expediently passed over. Bit 5 is automatically cleared when writing begins.

2.4 CONTINUED OPERATION

The presence of the MTF flag signifies the end of the specified operation. To continue operation in the same mode, the MTAF and MTGO instructions should be executed before the interrecord gap delay terminates operation. Since the tape control status will not be ready, MTAF does not clear the command register; therefore, operation continues in the same mode. The MTGO instruction prevents tape control status from reverting to not ready, therefore, tape motion continues. If the operation is a data transfer function, the WC and CA should be reinitialized. Operation continues until the new set of parameters (WC register) terminate operation by setting the MTF flag. If it is desired to continue operation, the MTAF and MTGO instruction must be issued again.

To change modes of operation, in either the same or reverse direction, MTCM, MTAF, and MTGO instructions should be issued. If a change in direction is specified, the transport will stop, pause, and automatically start up again.

For the write function, no change in direction can be effected; the only mode change that can be performed is to a write EOF. To follow a write with a read, space, forward, or read/compare, the program must allow the tape unit to come to a complete stop (TUR) before issuing the new command.

2.5 FLAGS

There are four flags that can be sensed by the I/O skip facility. They are the job done (MTF), error (ER), tape control ready (TCR), and tape transport ready (TUR). The MTF and ER are sensed by the same IOT instruction. If the interrupt is enabled, the MTF and ER flags generate an interrupt.

The MTF flag and the ER flag are set at the completion of the specified function. An exception, however, is when an illegal command occurs; it sets the ER flag as soon as the illegal command is detected. The ER is set by an illegal command or any of the following events:

BAD TAPE ERROR
BOT (Beginning of Tape)
DATA LATE ERROR
PARITY ERROR
EOF (end-of-file)
EOT (end-of-tape)
READ COMPARE ERROR
RECORD LENGTH INCORRECT

If an error occurs as sensed via the ER, the status register can be examined to determine the exact cause of the ER flag.

2.6 STATUS REGISTER

The TC59 status register may be examined by issuing the MTRS instruction which reads the content of status register bits 0 through 16 into bits 0 through 16, respectively, of the AC. The status register format is as shown in Table 2-3; each bit is defined as follows:

Table 2-3
Status Register

Bit	Function (when set)	Bit	Function (when set)
0	Error flag (EF)	8	Record length incorrect WC = 0 (long) WC ≠ 0 (short)
1	Tape rewinding		
2	Beginning of tape (BOT)	9	Data request late
3	Illegal command	10	Bad tape
4	Parity error (Lateral or Longitudinal)	11	Magnetic tape flag (MTF) or job done
5	End of file (EOF)	14	7-track tape
6	End of tape (EOT)	15	Character counter bit CC0
7	Read/compare error	16	Character counter bit CC1

2.6.1 Error Flag (ER)

The error flag is defined in Paragraph 2.5.

2.6.2 Tape Rewinding

When a rewind command is issued to a tape transport and the function is underway, the tape rewinding bit is set by the control. This status is a transport status and any selected transport which is in a high-speed rewind will display this bit.

2.6.3 Beginning of Tape (BOT)

The BOT bit is set when BOT reflective strip is detected on the selected tape transport.

2.6.4 Illegal Command

The illegal command bit is set when the MTLC or MTCM is issued to load the command register and the tape control is not ready and the MTF is not set. The illegal command bit is also set by the MTGO instruction when any of the following events occur.

a. 9-track operation other than rewind specified with a density other than 800 bpi.
b. The write lockout bit from the selected tape transport is set and a write EOF specified.
c. The selected tape transport not ready and the tape control is ready.
d. A NO OP command is selected.
e. A reverse direction and BOT status.

2.6.5 Parity Error

The parity bit is set by either a longitudinal or lateral parity error.

2.6.6 End-Of-File (EOF)

The end-of-file bit is set when the EOF mark is detected during space, read, read/compare, or write EOF operation.

2.6.7 End-Of-Tape (EOT)

EOT detection occurs during any forward command when the EOT reflective strip is sensed. When EOT is sensed on line, the EOT bit is set; but the function continues to completion at which time the MTF is set and EF is set.

2.6.8 Read/Compare Error

This bit is set by a read/compare error (defined in Paragraph 2.3.6).

2.6.9 Record Length Incorrect

During read or read/compare, this bit is set when the number of words read does not agree with the initial 2's complement content of the WC. If the record read was longer than that specified, then WC is 0; if shorter WC $\neq 0$.

2.6.10 Data Request Late Error

The error occurs during a tape function that requires a memory access. If the data flag initiates a memory access, the data must be transmitted before the next read or write pulse; if it does not, this error bit is set. In addition to setting the error flag, this error forces a WC overflow within the tape control to terminate the present operation and prevent any further data transmission.

2.6.11 Bad Tape

Bad tape error indicates detection of a bad spot on tape. Bad tape is defined as not reading two or more consecutive characters and then reading data within the period defined by the shutdown delay. The error bit is set by the tape control when this occurs. MTF and interrupt do not occur until the end-of-record in which the error was detected.

2.6.12 Magnetic Tape Flag (MTF)

The MTF or job done flag is described in Paragraph 2.5.

2.7 MAGNETIC TAPE FUNCTION SUMMARY

Table 2-4 summarizes the tape functions. The legend below is used with Table 2-4.

LEGEND:
- WC = Word Counter Register = 32
- CA = Current Address Register = 33
- F = Forward
- R = Reverse
- DS = Density Setting
- PR = Parity Setting
- EN = Enable Interrupt

Table 2-4
Magnetic Tape Function Summary

Function	Characteristics	Status or Error Types
NO OP	CA: Ignored WC: Ignored DS: Ignored PR: Ignored EN: Ignored	Illegal BOT Tape Rewinding
SPACE FORWARD	CA: Ignored WC: 2s complement of number of records to skip DS: Must be set PR: Ignored EN: Must be set	Illegal EOF Bad Tape MTF BOT, EOT
SPACE REVERSE	Same as Space Forward	Illegal EOF Bad Tape BOT MTF
READ DATA	CA: Core Address - 1 WC: 2s complement of number of words to be transferred DS: Must be set PR: Must be set EN: Must be set	Illegal EOF Parity Bad Tape MTF EOT Request Late Record Length Incorrect
WRITE DATA	Same as READ DATA	Illegal EOT Parity MTF Bad Tape Data Request Late
WRITE EOF	CA: Ignored WC: Ignored DS: Must be set PR: Ignored and set EN: Must be set to EVEN by command	Same as WRITE DATA Except EOF
READ/COMPARE	Same as READ DATA	Illegal EOF Read/Compare Error Bad Tape MTF EOT Data Late Record Length Incorrect

Table 2-4 (Cont)
Magnetic Tape Function Summary

Function	Characteristics	Status or Error Types
REWIND	CA: Ignored WC: Ignored DS: Ignored PR: Ignored EN: Must be set	Illegal Tape Rewinding MTF BOT

CHAPTER 3
PRINCIPLES OF OPERATION

3.1 INTRODUCTION

This chapter describes system and detailed logic for each of the TC59 Magnetic Tape Transport Control functions. The logic drawings in Chapter 6 are referenced in the text for the convenience of the reader.

3.2 SYSTEM DESCRIPTION

A system block diagram of the TC59 Magnetic Tape Transport Control is shown in Figure 3-1. Assuming a write operation, the programming first sets up CA (current address) and WC (word count) registers in the data channel of the processor; the CA specifies the core memory address from which to obtain data to be written; the WC specifies the number of words to be written on tape. The program then loads the command register from the AC with appropriate commands (write, density mode, parity, etc.) and issues the MTGO instruction which initiates operation. The appropriate motion commands are transferred to the tape transport selected. A short delay is implemented to provide the tape interrecord gap. During this delay, the data flag is set to initiate a word transfer from core memory to the data buffer via the processor data channel.

After the interrecord gap delay and data buffer loading, the write operation begins. Assuming 7-track operation, the data buffer 18-bit word must be divided into three 6-bit characters for writing on tape. The character counter sequences the 6-bit character from the data buffer; as a 6-bit character is written from the high-order bits of the data buffer, the character counter is incremented to sequence the next low-order 6-bit character. After the three 6-bit characters from the data buffer are written, the DATA FLAG is set to initiate another word transfer to the data buffer via the data channel.

Operation continues in this manner until the WC register is reduced to zero, at which time the tape control is notified. The LPCC character is written and write operation terminates. The tape continues in the forward motion until the read circuits detect the end-of-record passing under the read head.

The deceleration delay is initiated (time allotted to write the interrecord gap), and the job done (MTF) flag is set. At the end of the deceleration delay, the forward driving force is removed from the tape unit and tape motion ceases.

For the read operation, the initial programming sequence is similar to write. As 6-bit characters are read from tape, they are sequenced into the data buffer by the character counter. When the data buffer is full, the DATA FLAG initiates a data channel transfer of the data buffer word into core memory. Operation continues until the read circuits detect the end-of-record.

As shown in Figure 3-1, the command register and tape control status can be transferred to the processor by using the appropriate IOT instructions. Moreover, the job done flag and the error flag can be enabled to generate a computer interrupt. Through the I/O skip facility, the processor can examine the job done (MTF), tape unit ready (TUR), tape control ready (TCR), or the error (ER) flag.

3.3 NRZ RECORDING

The actual technique of recording on magnetic tape is called the non-return-to-zero (NRZ) method. In this method, a reversal of the direction of magnetization in a channel represents a 1 bit, a lack of reversal represents a 0 bit. Writing is achieved by using a flip-flop to control the direction of magnetizing current in each channel write head; the group of flip-flops is called the write buffer. By applying the 1s lines to the complement inputs of the write buffer, each channel reverses its flux only when a 1 bit is to be written for a character. Further, the write buffer accumulates the LPCC (longitudinal parity check character) to be written as an EOR character. When the write buffer is reset at EOR time, the LPCC character is written automatically because of the nature of NRZ recording.

The NRZ recording method provides self-checking during reading since a transition (or flux reversal) in any track, signifying a 1 bit for that character in that track, is used to strobe or sense all seven tracks for that character. Ideally, all transitions for a single character would be sensed simultaneously by the read head. In fact, tape skew makes these transitions (if more than one in a single character) non-simultaneous on reading. There may be a difference, however, in alignment of the read head with respect to the write head recording the tape (static skew). There are apt to be changes that vary during tape travel (dynamic skew) in tape alignment to the read head from its alignment during writing. To accommodate these timing variations between channels due to skewing, the first detected transition for a character initiates a delay before the character is strobed. This delay is selected to accept the maximum skewing produced at the linear tape transport speed with the designated tape density.

A simplified block diagram of the tape system write and read paths for a single track is shown in Figure 3-2. The write path (WP) is shown at the top of the figure. The WRITE flip-flop in the write amplifier is complemented at each WP pulse, if the data buffer for that particular character contains a 1.

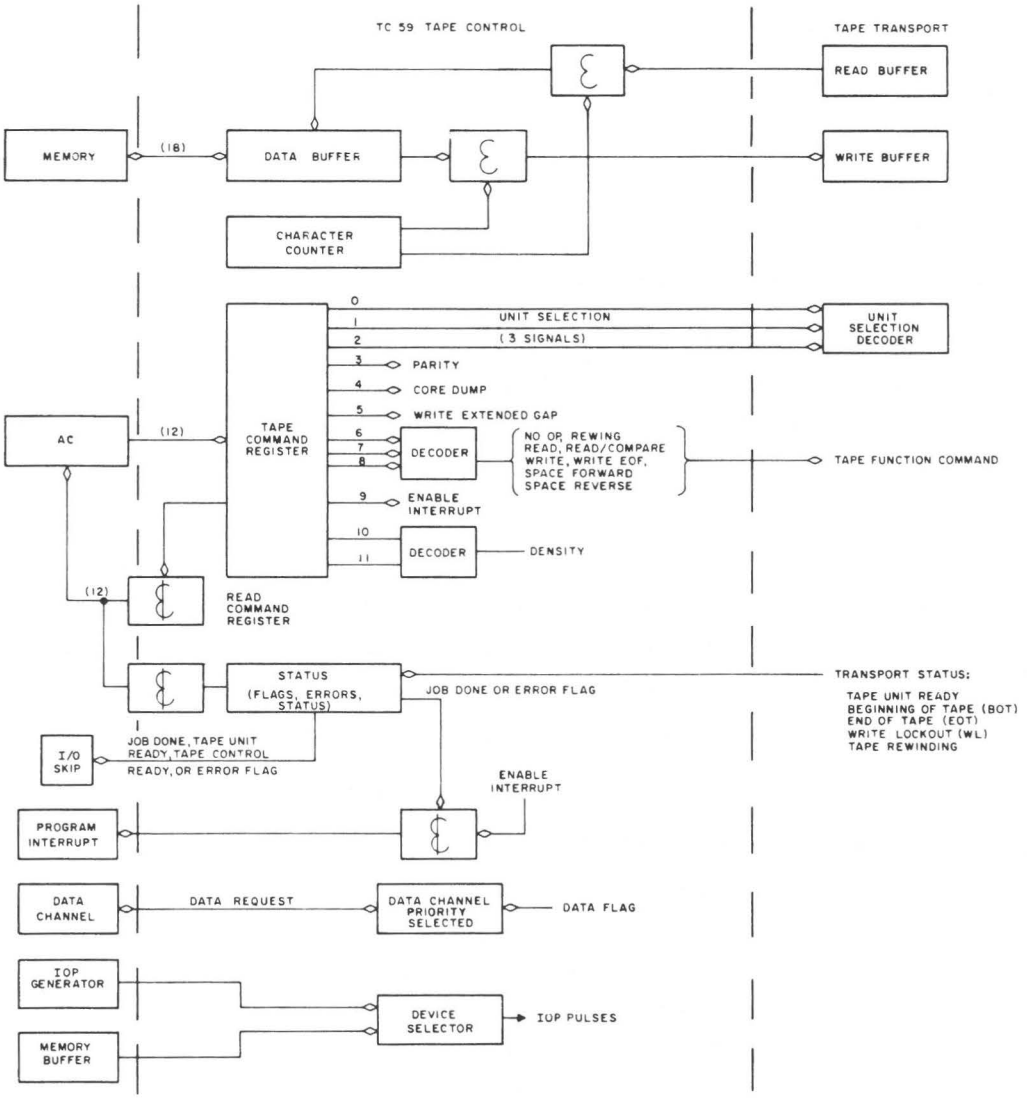


Figure 3-1 System Block Diagram

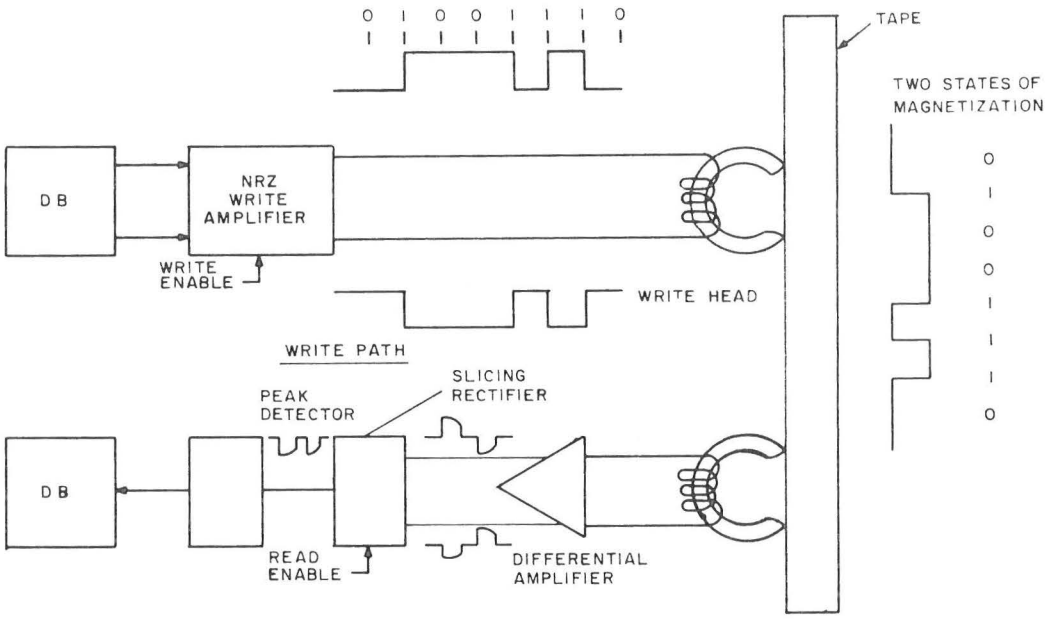


Figure 3-2 Tape Write and Read Signal Flow

When gated by a write-enable signal, the write amplifier drives one or the other of the two opposing directions at the write head. If the WRITE ENABLE level is not present, no current flows through either coil. Whenever a 1 is to be written on a tape, the WRITE flip-flop is complemented by the WP pulse. The transition of the WRITE flip-flop terminates the current through one coil and starts it in the other direction, changing the direction of the tape magnetization, and thus writing a 1 on tape. As long as the WRITE flip-flop remains in the same state, the current flows through the same coil, and 0s are written on the tape. The tape is then magnetized in the same direction over a series of character spaces.

The read path is shown at the bottom of Figure 3-2. The tape reaches the read heads shortly after transversing the write head. As long as the direction of tape magnetization remains constant, no current flows through the read head coil. Each change in the direction of tape magnetization induces a current in the read head. The read current produced by two consecutive tape 1s is shown in the waveform near the read head. These signals are applied to a differential read amplifier to provide amplification for different signals, but only fractional amplification for common mode signals. The output of the read amplifier is then sent through a slicing rectifier. The rectifier output pulse is of the same polarity for an input pulse of either polarity from a read amplifier. No slice output is generated, however, unless the input exceeds a designated special level. A low-level noise input cannot generate an output pulse. Next, the slicing rectifier output is applied to a peak detector. The peak detector produces a logic pulse output at the peak of the input pulse.

3.4 PROGRAMMING SEQUENCE

The following paragraphs, which contain detailed discussion of logic circuits, must assume that there is some program control. Therefore, the following programming sequence is shown to provide this control:

```
LAC TPFN        /LOAD AC WITH TAPE FUNCTIONS
                /TO BE TRANSMITTED TO TAPE
                /CONTROL COMMAND REGISTER
MTCR            /TAPE CONTROL READY ?
JMP .-1         /WAIT
MTLC            /AC TO COMMAND REGISTER
MTRR            /TAPE TRANSPORT READY  ?
JMP XXX
MTGO            /SET GO FLIP-FLOP
```

The first instruction loads the contents of symbolic location TPFN into the AC. Location TPFN should be appropriately coded to the desired tape functions which are to be transmitted to the tape control command register. MTCR checks to see if tape control is ready. If ready, the program skips to the MTLC instruction. The MTLC instruction generates two IOT pulses: MTAF and LCM (refer to drawing TC59-0-3).

Since GO (tape control ready) is reset at this time, the first pulse, MTAF, generates CLEAR ALL (drawing TC50-0-2 SH 2) which clears all flags, the command register, and normalizes key flip-flops. The LCM pulse then strobes the AC content into the command register (CM0-CM11 on drawing TC50-0-2 SH 1). The command register now specifies the desired tape functions: parity, density, tape transport selection, etc. The tape transport is now selected and the next instruction MTTR examines tape transport status. If not ready, the next instruction can be a wait instruction (JMP .-1) to loop until tape transport ready or it can be a jump to some routine to select another transport or determine why the presently selected transport is not ready.

If tape transport is ready, the program skips to the MTGO instruction. Before MTGO is executed, the tape control will have determined whether the command was legal (see drawing TC50-0-2 SH2). If legal, the GO flip-flop (drawing TC50-0-2 SH 1) is enabled so that the MTGO instruction can set the GO flip-flop.

3.5 INTERRECORD GAP DELAY

According to tape format, between each record there is an interrecord gap. Assuming that the tape is in a stopped position, before reading or writing can occur, the tape must attain operating speed within the interrecord gap. To provide the interrecord gap, the tape control timing circuits incorporate a timing delay which is explained as follows.

The next sequential instruction MTGO (from above programming sequence) sets the GO flip-flop (drawing TC50-0-2 Sh 1). The GO signal then performs the following functions.

a. Sets the ALPHA (acceleration delay) flip-flop (TC50-0-4 Sh 1).

b. Generates the SET TAPE FUNCTION pulse (TC50-0-2 Sh 1) which turns the transport status off the bus and sends to the transport, the command direction, forward reverse, rewind, rewind-unload, and write. The transport that receives the command sets the function into the tape transport register.

c. Generates the MOVE signal to move the tape in the specified direction.

d. Enables CM4 to revise the 9-track status to 7-track status. CM4 is the core dump bit and causes a 9-track transport to appear as a 7-track system.

The ALPHA flip-flop being set generates ENABLE MUC (drawing TC50-0-4 Sh 1) which enables the motion-up counter (MUC on TC50-0-1). For the write command, the ALPHA signal initiates the data break cycle to transmit the first word to be recorded to the data buffer. ENABLE MUC now generates MUC pulses at the 800 bpi clock frequency of the selected tape transport. The MUC bits are decoded so that the thirtieth MUC pulse sets the DELAY SYNC flip-flop (DELAY TRANSFERRED will be 0 at this time). DELAY SYNC synchronizes the motion transfer sequence to enable the motion-delay characteristics from the selected tape transport to appear on the read buffer lines. The octal number, representing motion delay characteristics, represents the start-stop characteristics and operating speed of the attached tape transport. The next MUC pulse generates the STROBE DELAY pulse which strobes the content of the read buffer lines into the T-register (TC50-0-4 Sh 1); the T-register is the timing register that provides the necessary acceleration or deceleration delay. STROBE DELAY then sets the DELAY TRANSFERRED flip-flop (indicating transfer complete) and resets the DELAY SYNC flip-flop. The next MUC pulse generates a DOWN COUNT pulse and begins to count down the T-register. The MUC pulses continue producing DOWN COUNT pulses on every thirty-second MUC pulse. Since the DELAYED TRANSFERRED flip-flop is set thereafter, the thirtieth and thirty-first pulse will not reinitialize the T-register. When the T-register has counted down to a one-count, the next DOWN COUNT pulse strobes the T-register to 0 and produces the IRD OVER (interrecord delay over) pulse. The IRD OVER pulse clears the α and DE - α flip-flops, thus ending the acceleration or deceleration delay. It should be noted that the delay sequence just described is used for deceleration of the tape following a tape spacing function as well as the acceleration of the tape before a tape spacing function.

The IRD OVER pulse, enabled by the ALPHA signal, generates the BEGIN OPERATION pulse (TC50-0-4 Sh 2) which initiates the write and write end-of-file operations. If the rewind command is selected, the BEGIN OPERATION pulse resets the GO flip-flop which frees the tape control for a new command to a different tape transport while the previously selected tape transport rewinds.

3.6 WRITE

The write operation is initiated by the BEGIN OPERATION pulse which sets the WRITE ENABLE flip-flop (TC50-0-4 Sh 2). The WRITE ENABLE signal then enables the CLOCK pulses (TC50-0-2 Sh 2) to produce WP (WRITE pulses). The WRITE pulses complement the character count circuits (CC0 and CC1 on TC59-0-2 Sh 1) in order to disassemble the 18-bit word in the data buffer into the appropriate 6-bit (7-track operation) or 8-bit (9-track operation) characters that are to be recorded. In 7-track operation there are three characters per word. In 9-track operation, there are two characters per word.

For 7-track operation, the character count circuits sequentially generate 1ST CHAR 7 CHANNEL, 2ND CHAR 7 CHANNEL, and 3RD CHAR 7 CHANNEL signals (TC59-0-2 Sh 1) which sequentially disassemble the 18-bit data buffer word into 6-bit characters and apply them to the bus of the tape transport. In a similar manner, the 9-track decoding signals are formed. Drawing TC50-0-1 shows the decoding of the 18-bit data buffer word for both 7-track and 9-track operation.

The WRITE pulse also produces RECORD DATA pulses (TC50-0-4 Sh 2) which are sent to the tape transport to record the characters on the tape. For 9-track operation the WRITE pulse exclusive ORs the characters into the CRC register (TC50-0-3 Sh 1), one character at a time. The CRC register then performs the necessary manipulation of the data to conform to 9-track format. The characters are also decoded in the write parity circuit (TC50-0-3 Sh 2) and the parity bit pertaining to that character is sent to the tape transport to be recorded.

When a complete word has been written on, the DATA FLAG flip-flop is set (if the word count overflow WCO is in the 1 state). The DATA FLAG initiates a data break cycle to transfer a new word into the data buffer. The DATA FLAG flip-flop is set in the following manner. The 2ND CHAR 9 CHANNEL or 3RD CHAR 7 CHANNEL (TC59-0-2 Sh 1) generates ENABLE DATA FLAG which in turn permits the WP to generate the WRITING SET DF pulse (TC59-0-2 Sh 2). This pulse generates the +1 → DF pulse (TC50-0-2 Sh 2) which sets the DATA FLAG flip-flop (TC50-0-2 Sh 1). The subsequent data channel discussion describes in detail the data channel transfer.

Operation continues until the desired number of words are transferred as indicated by the word-count overflow (I/O OFLO) pulse from the processor. The I/O OFLO pulse resets the WCO flip-flop (TC59-0-2 Sh 2); when the last character of the last word has been written WCO(0) generates

LAST WORD (TC59-0-2 Sh 1). LAST WORD enables the WP to reset the WRITE ENABLE flip-flop which in turn sets the WRITE EOR flip-flop (TC50-0-4 Sh 2). Since we are at the end of record, a 4-character space must be left on tape and then the LPCC character must be written. This is accomplished as follows.

The WRITE EOR (1) signal enables CLOCK pulses to count up the EOR1 and EOR2 counter (TC50-0-4 Sh 2) to produce the required 4-character space signified by the 4 CHAR pulse. For the 7-track system, the 4 CHAR pulse generates the WRITE LPCC pulse (TC50-0-4 Sh 1) which is sent to the tape transport to write the longitudinal parity check character.

For a 9-track system, the CRC character is written following the first 4-character space. The EOR1 and EOR2 counter recycles for second 4-character space count and then the LPCC is written.

Tape motion continues in the forward motion until the read circuits detect the end-of-record passing under the read head in the tape transport. When the read circuits detect the end of record the RECORD OVER pulse is generated which initiates the deceleration delay. At the start of the deceleration delay, STROBE delay ANDed with STOP sets the MTF (job done) flip-flop. If the interrupt is enabled, MTF interrupts the main program to signify that the record has been written. Subsequently at the end of the deceleration delay, the IRD OVER pulse is produced and is enabled by STOP (DE-α(1) and NOT SPACING) to produce the CLEAR GO pulse (TC50-0-4 Sh 1). The CLEAR GO pulse resets the GO flip-flop which terminates the MOVE signal and stops the tape thus completing the write operation.

3.7 WRITE CONTINUE

To continue writing record, the MTAF and MTGO must be issued before the deceleration delay terminates. The MTAF resets key flip-flops and registers. The MTGO pulse sets the CONTINUE flip-flop (TC50-0-3 Sh 2). Note that the MTGO pulse is enabled only when the interrecord delay is not complete (GO is 1) and no change of direction has been specified. With the CONTINUE flip-flop set, the CLEAR GO pulse at the end of the interrecord delay cannot reset the GO flip-flop. With the CONTINUE flip-flop set, the IRD OVER pulse resets DE-α, the transition of DE-α is enabled by CONTINUE (1) to set the α flip-flop which initiates the acceleration delay. Operation from this point is as described for the write operation.

3.8 WRITE END-OF-FILE MARK

After the interrecord delay, the BEGIN OPERATION pulse sets the SYNC EOF flip-flop (TC50-0-4 Sh 2) which synchronizes the tape operation to write the EOF[1] character. SYNC EOF enables

[1]EOF decoded by R141 modules (TC50-0-1) to write 17_8 if 7-track transport or 23_8 if 9-track transport.

the next CLOCK pulse to set the WRITE EOR flip-flop. The transition of WRITE EOR, enabled by SYNC EOF, generates the RECORD DATA pulse which is sent to the tape transport to write the EOF character on tape. WRITE EOR then enables the 4-character sequence prior to LPCC character; WRITE EOR enables the CLOCK pulses to increment EOR1 and EOR2 to a 4-count and generate the 4 CHAR pulse. For a 7-track system, 4 CHAR generates WRITE LPCC (TC50-0-4 Sh 1) which writes the LPCC character. For a 9-track system, the first 4 CHAR pulse writes the CRC character; a second 4 CHAR pulse is generated to write the LPCC. Operation terminates when the read circuits detect missing data and begin the deceleration of the tape.

3.9 READ

After the initial programming sequence sets up for reading and issues the MTGO instruction, and the interrecord delay sequence is complete, operation begins when the read circuits in the tape transport detect data. For each character detected, the tape transport sends to the tape control a READ SKEW OVER pulse; the READ SKEW OVER pulse becomes the READ STROBE pulse (TC50-0-2 Sh 2); READ OR READ COMPARE and ERF (0) enable the READ STROBE to generate the READ pulse. The character counter (CC0 and CC1 on TC59-0-2 Sh 1) is zero at this time; therefore, 1ST CHAR 7 CHANNEL signal enables the READ pulse to strobe the 6-bit character from the tape transport into the high-order bits of the data buffer (TC59-0-1). The READ pulse also increments the character counter. Parity is checked by the READ STROBE (TC50-0-3 Sh 1) by setting the LATERAL PARITY ERROR flip-flop when an error occurs. The READ STROBE also accumulates the LPCC character by complementing the LPCC register for those bits that are 1. Operation continues in this manner until the data buffer is full. The character count will be two (assuming 7-track operations) which initiates a data break cycle to transfer the data buffer content to the processor. This is accomplished by the READ pulse generating READING SET DF (TC59-0-1) which generates the +1 → DF pulse (TC50-0-2 Sh 2) which in turn sets the DATA FLAG flip-flop.

Operation continues in this manner until the read circuits detect missing data, thus signifying end-of-record. It should be noted that if the WC is less than the record length, only the number of words specified by WC are transferred to memory. If WC is greater than the record length, the entire record, of course, is transferred into memory. In any case, the detection of end-of-record by read circuits is the determining factor for stopping operation. This is accomplished as follows.

The READ STROBE, which signifies that a character has been read from tape, is enabled by MOTION FORWARD AND DE- α (0) to set the DATA PRESENT flip-flop (TC50-0-4 Sh 1). DATA PRESENT then permits the CLOCK pulse to toggle the EOR3 flip-flop (TC50-0-4 Sh 2). As long as data is present, the READ STROBE resets EOR3 before EOR4 can be set. When data is missing, the READ

STROBE does not occur and EOR4 gets set. The next CLOCK PULSE generates the RECORD OVER pulse which sets DE-α to initiate the deceleration delay and thus terminate operation. The LPCC register should be 0 at strobe delay time; if not, LPCC $\neq$ 0 (TC50-0-3 Sh 2) generates a PARITY ERROR (TC50-0-3 Sh 1). To continue operation the program must issue MTAF and MTGO as described in the section on Writing.

3.10 READ/COMPARE

In the read/compare operation, a complete 18-bit word is read from tape and assembled into the data buffer. After the word is assembled, the data break cycle is initiated to obtain the word from memory for comparison. The word from memory is exclusive ORed into the data buffer. Consequently, the data buffer should contain all 0s; if not, the READ/COMPARE ERROR is set.

Operationally, the read/compare mode is similar to the read mode except as follows. In the read/compare mode of operation, the data break cycle is initiated (via READING set DF, TC59-0-1) to obtain a word from memory in which to compare to the data buffer. During the word transfer, the READ/COMPARE signal permits the LDB pulse to exclusive OR the word from memory (I/O BUS) into the data buffer (TC59-0-1). The data buffer is then decoded to determine if it contains all 0s. The CHECK DB = 0 pulse (TC59-0-1) samples the decoded data buffer signal and if DB $\neq$ 0, then the READ COMPARE ERROR flip-flop (TC50-0-2) is set.

The READ/COMPARE ERROR being set inhibits the +1 $\rightarrow$ DF pulse (TC50-0-2) which prevents any future data break cycles (until flags are cleared). This prevents the CA in the processor from being incremented even though operation continues. Operation continues until the read circuits detect the end-of-record. At that time the program may examine read/compare status and if a read/compare error is found, the program can further examine the CA to determine the memory location that was in error.

3.11 DENSITY MODES

Three different tape densities are available: 800, 556, and 200 cpi (character per inch). Bits 10 and 11 of the command register select the densities (see TC50-0-2 Sh 1). The different recording densities are effected by changing the clock pulse frequency. For 800 cpi operation, the 800 bpi clock pulses from the tape transport are enabled to produce the TC59 clock pulse (TC50-0-4 Sh 2); for 556 cpi operation, the 556 bpi clock pulses from the tape transport are enabled. For 200 cpi operation, the 800 bpi clock is counted-down by flip-flops A and B (TC50-0-4 Sh 1) which produce ENABLE 200 every fourth count to enable the 800 bpi clock to produce clock pulses.

3.12 ERRORS

3.12.1 Data Late Errors

The data late error indicates that an extraneous word was either written or read from tape before the data break cycle could supply another word for write or store the present data buffer word for read. The DATA LATE flip-flop (TC50-0-2 Sh 1) is set when DATA FLAG is still set (indicating that the data break cycle has not occurred) when STROBE DATA LATE pulse (WP or READ PULSE) occurs.

3.12.2 Parity Error

As discussed during write and read operation, the parity error is the result of either a longitudinal or lateral parity error.

3.12.3 Read/Compare Error

The read/compare error was discussed in the read/compare discussion.

3.12.4 Record Length Incorrect

During read or read/compare operation, this error signifies that the record length specified by the WC register differs from the record-length read from tape. The RECORD LENGTH INCORRECT flip-flop (TC50-0-2 Sh 2) is set for a long record by the READ STROBE (enabled by WC0(0) indicating WC is 0) and by the RECORD OVER pulse (enabled when the WC register specifies more data) for a short record.

3.12.5 Bad Tape Error

This error indicates that data was in the interrecord gap. The BAD TAPE ERROR flip-flop (TC50-0-4 Sh 2) is set by the READ STROBE (indicating data present) which is enabled by DE- α and INTO RECORD.

All errors are combined, along with BOT, EOF, and EOT, to generate ERROR which sets the ERROR FLAG flip-flop (TC50-0-2 Sh 1) following end-of-record. The ERROR FLAG status is sampled by MTSF to generate a SKIP RQ (skip request) as shown on TC59-0-2 Sh 2.

If interrupt is enabled (CM9=1), the ERROR FLAG generates an interrupt as shown on TC59-0-2 Sh 2.

3.13 ILLEGAL COMMANDS

The ILLEGAL flip-flop (TC50-0-2 Sh 2) is set by the MTGO pulse when one of the following events occur.

a. 9-track operation other than rewind specified and density not set to 800 bpi.

b. Write or write EOF operation specified and the write-lockout bit (WL) from the tape transport is set.

c. Beginning-of-tape status and a reverse motion specified.

d. Tape control (GO=1) and tape transport not ready.

e. A NO-OP (no operation) specified by the command register.

The ILLEGAL flip-flop is also set by the load command (LCM) when tape control is not ready (GO(1)=1) and job done flag (MTF) is not set.

3.14 SPACE

There are two commands for spacing records -- space forward and space reverse. The 2s complement of the number of records to be spaced is set into the WC register. The CA register need not be set. The operation of space forward or space reverse is accomplished in a similar manner to read or write. The program initiates operation by setting the WC register, loading the command register, and issuing the MTGO which starts the tape and initiates the acceleration delay. Subsequently, the read strobe is monitored for end-of-record. While spacing over a record, no data is transferred.

The end-of-record detection, as in normal operation, produces the RECORD OVER pulse which initiates the deceleration delay. However, in a spacing operation it initiates a data channel transfer, if the WC is not 0; that is, it generates +1 → DF which initiates the transfer (TC50-0-2 Sh 2). The WC register is incremented in this manner. The CA is not incremented, since the spacing operation generates INC · MB (TC59-0-2 Sh 2) which prevents the CA from being incremented. (The INC · MB causes the processor data channel break (DCH) to be a 1-cycle break rather than the normal 3- or 4-cycle break. Only the WC register is incremented during the break.) Since GO is still set, the MOVE signal maintains tape motion.

After spacing over the required number of records, the WC flip-flop is reset, thus enabling the STOP signal (TC50-0-4 Sh 1). The IRD OVER pulse generates CLEAR GO which resets the GO flip-flop to terminate operation.

The detection of end-of-record in the space reverse mode is different from that for a forward motion, since the LPCC is always the first character detected. This is accomplished by the INTO RECORD flip-flop (TC50-0-4 Sh 1). The READ STROBE, which occurs as the result of the LPCC character,

sets the INTO RECORD flip-flop. Note that DATA PRESENT will not be set by this READ STROBE. The next READ STROBE occurs when the last character of the record (the first in reverse motion) moves under the read head; this READ STROBE sets the DATA PRESENT flip-flop. When no more READ STROBES occur, EOR 3 (TC50-0-4 Sh 2) remains set and the next CLOCK pulse sets EOR 4; the following CLOCK pulse generates RECORD OVER, which initiates the deceleration delay.

3.15 DATA CHANNEL OPERATION

The processor data channel, multiplexed to permit interfaced service to four peripheral devices, provides a high-speed interface to the core memory along the I/O bus. Requests for data from the tape control are honored by the channel at the completion of the instruction in progress at the time the request is made. The channel is controlled by word count (WC) and address registers (CA) held in core memory; each request updates these registers and transfers the data between the memory and the tape control.

Each of the four devices has a unique pair of (sequential) core memory registers associated with it. The tape control is allocated to locations 32 and 33. These registers must be initialized by the program, before the peripheral device may begin transferring data through the channel. The first (word count) register, location 32, is initialized to contain the 2s complement of the number of words to be transmitted. The second (address) register, location 33, is initialized to contain one less than the first address of the data word block.

These registers may be examined at the end of channel operation to check for final address, if, for example, the tape control indicates that an incorrect record length was read.

The maximum transfer capacity of the channel is between 250,000 and 333,000 words per second, depending on the mix of input and output rates. Each input transfer steals three processor cycles; each output transfer steals four processor cycles. The latency time (maximum wait before service is granted after a request is made) may be as high as 30 μs under adverse conditions.

Priority among I/O devices making simultaneous requests is determined by their physical placement on the I/O bus, with devices close to the processor having priority over devices further away. The establishment of priority requires that each device quickly propagate an enable signal (DCH EN) to the next device on the bus.

The DATA FLAG, as explained previously, is raised asynchronously by a request for data transfer within the tape control. This flag is synchronized by the W104 Multiplexer, which requests a data channel interrupt through the DCH RQ line (TC59-0-2 Sh 2). If more than one device on the channel

is requesting, the multiplexer insures that the lower priority device is shut out by driving its enable (DCH EN IN) input line to ground and thus maintaining its DATA RQ flip-flop in the reset state. This request is recognized by the processor and, at the end of the current instruction, control is relinquished to the channel hardware.

The channel hardware begins operation by identifying the device requesting service. This is performed by issuing a grant signal (DCH GR) to all connected devices. Upon receipt of the grant signal, the device which supplied the DCH RQ transmits the core memory address of its word count register along the I/O address lines. The specified register is read from memory, incremented, and rewritten. If, in this word count updating procedure, the count reaches 0, an I/O overflow signal is sent to all devices. The device hardware interprets the overflow signal as a shut down command. No further transfers are made until the device is reinitialized by the programmer. Note that the READ RQ and WRITE RQ are conditioned by DATA EN B; this assures that only the selected device propagates the read or write request.

After incrementing the word count register, the channel reads the next sequential word from memory. This is taken as the current address register, which is incremented and rewritten into memory. The updated value is used to specify the location into (from) which the data is to be transferred.

3.16 AUTOMATIC PRIORITY INTERRUPT

The priority interrupt operates in a manner somewhat similar to the priority scheme of the data channel. Both make use of the W104 modules. Priority is established by putting the W104 modules in tandem. The API EN IN signal coming into the high-priority module with the API RQ flip-flop set will generate a ground signal on API EN OUT which disables the API RQ flip-flop in the lower-priority chain.

Interrupt requests start when the MTF or ERROR FLAG (enabled by CM9) generate ENABLE API RQ, which in turn sets the INT flip-flop. INT enables the I/O SYNC pulse to set API RQ; API RQ remains set if there are no high priority requests and sends the PROG INT RQ (interrupt request) to the processor. The API GR pulse (priority grant) then transfers the core location address of the program subroutine unique to the tape control to the processor.

CHAPTER 4
MAINTENANCE

This chapter contains the information required for maintaining the TC59 Magnetic Tape Transport Control. Three categories of maintenance are provided: preventive, troubleshooting procedures, and corrective.

Preventive maintenance includes routine periodic checks, such as visual inspections, standard procedures involving cleaning and lubricating, minor mechanical adjustments, and occasional marginal checking to expose weakening conditions before they become malfunctions. It is primarily concerned with mechanical operations of the tape transport.

It should be emphasized that good maintenance procedures are predicated upon a thorough knowledge of not only the tape control unit but also the tape drive and the processor interface. Therefore, if the maintenance technician is not familiar with the theory of operation, he should review Chapter 3 of this manual or the applicable sections of the tape transport manual and the PDP-9 or PDP-15 Maintenance Manual.

Troubleshooting procedures range from basic power-supply checks to intricate logic troubleshooting techniques involving programmed operation of the processor.

Corrective maintenance outlines the measures required for correcting any malfunction, after it has been isolated, by replacement of the module or defective part.

In addition to maintenance information, this section includes assembly-location information, to facilitate locating the circuits and parts within the system.

4.1 MAINTENANCE EQUIPMENT

The maintenance equipment specified in the PDP-9 or PDP-15 Maintenance Manual is adequate for performing tests on the TC59 Magnetic Tape Transport Control. The Datamec Manual references special adjustment tools for aligning the tape transport.

4.2 MODULE LOCATIONS

Drawings D-MU-TC50-0-13 and A-MU-TC59-0-5 in Volume 2 of this manual show the location of the modules within the mounting panels, as viewed from the wiring side. The key functions or signals associated with each circuit on the module are listed within the module location and grouped according to the alpha pin designations.

4.3 PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed periodically, during operating time of the equipment, to ensure satisfactory operation. Performance of such tasks forestalls failures induced by progressive deterioration or minor damage, which, if not corrected, cause eventual down-time. Data obtained during the performance of each task is recorded in a log book. Analysis of this data indicates the rate of circuit operation deterioration and provides information for determining when components must be replaced to prevent failure of the system.

The following mechanical checks must be performed at specified intervals determined by operating time and operating environment. Following is a list of the periodic checks and procedures required.

a. Clean the exterior and the interior of the equipment cabinet with a vacuum cleaner or clean cloths moistened in nonflammable solvent.

b. Clean the air filters at the bottom of the cabinets. Remove each filter by taking out the fan and housing (held in place by two knurled and slotted captive screws), and wash in soapy water and dry in an oven or by spraying with compressed air. Spray each filter with Filter-Kote (Research Products Corporation, Madison, Wisconsin).

c. Lubricate door hinges and casters with a light machine oil, wiping off excess oil.

d. Inspect all wiring and cables for cuts, breaks, fraying, wear, deterioration, kinks, strain, and mechanical security. Tape, solder or replace any defective wiring or cable covering.

e. Inspect the following for mechanical security -- switches, control knobs, lamp assemblies, jacks, connectors, transformers, fans, and capacitors. Tighten or replace as required.

f. Inspect all module mounting panels to assure that each module is securely seated in its connector.

g. Inspect power supply capacitors for leaks, bulges, or discoloration. Replace any capacitors showing these signs of malfunction.

4.3.1 Power Supply Checks

The power-supply output checks described in Table 4-1 are performed by using a multimeter for the output voltage measurements with the normal load connected. The oscilloscope is used to measure the peak-to-peak ripple content on all dc outputs of the supply. The +10 and -15V supplies are not

adjustable; therefore, if the output voltage or ripple content is not within specifications, the power supply is considered defective and troubleshooting procedures are required. Refer to engineering drawing RS-B-728 for the power supply schematic.

Table 4-1
Power Supply Output Checks

Measurement Terminals at Power Supply Output	Nominal Output (Vdc)	Acceptable Output Range (V)	Maximum Output Current (A)	Maximum Peak-to-Peak Output Ripple (V)
Red (+) to Yellow (-)	+10	+9.5 to 11.5	7.5	0.7
Yellow (+) to Blue (-)	-15	-14.5 to 16.5	8.5	0.4

4.4 TROUBLESHOOTING PROCEDURES

4.4.1 PDP-9 Diagnostic Programs

The troubleshooting procedures make use of two programs: TC59 Instruction Test (MAINDEC-9A-D4AB-D) and the TC59 Utility Program. Program descriptions of both are provided as part of the documentation supplied with the equipment; they should be consulted for maximum troubleshooting efficiency. The TC59 Instruction Test exercises the tape control circuits and provides error printouts. The TC59 Utility Program, through its pseudo commands, provides a means to expediently program tape-control functions to exercise and test specific functions in conjunction with the DDT program. Test programs can be easily written, coded and typed in for immediate execution.

4.4.2 PDP-15 Diagnostic Programs

Table 4-2 lists the diagnostic programs provided to test and troubleshoot the TC59 in a PDP-15 system. The MAINDEC program descriptions listed in the table describe how to run and interpret the diagnostic programs.

Table 4-2
PDP-15 Diagnostic Programs for the TC59
Magnetic Tape Transport Control

Name	MAINDEC-15-	Description
TC59 Magnetic Tape Control Instruction Test	D4AA-D	A series of incremental subtests that aid in checkout.
TC59 Magnetic Tape Control Drive Function Timer	D4CC-D	Aids hardware debugging and maintenance of TC59 and associated tape transports, in any configuration from one to eight, 45 or 75 ips, 7- or 9-track.
TC59 Magnetic Tape Control Data Reliability Tests	D4DB-D (7-track) D4EB-D (9-track)	These tests are primarily to collect statistical information pertaining to tape transport data reliability, but may also serve a secondary purpose of debugging and troubleshooting the TC59 system.
TC59 Magnetic Tape Control Random Exerciser	D4GB-D	Simulates tape system usage for any magnetic tape transport configuration.

4.5 MODULE UTILIZATION

Table 4-3 contains a list of the number of modules used within the TC59 Magnetic Tape Transport Control.

Table 4-3
Module Utilization

Type	Description	Number Required
	TC50 Control Logic	
B130	3-Bit Parity Circuit	8
R002	Diode Gate	6
R107	Inverter	7
R111	Diode Gate	4
R113	Diode Gate	12
R123	Diode Gate	11
R141	Diode Gate	6
R151	Binary-to-Octal Decoder	1
R201	Flip-Flop	9

Table 4-3 (Cont)
Module Utilization

Type	Description	Number Required
	TC50 Control Logic (Cont)	
R202	Dual Flip-Flop	11
R203	Triple Flip-Flop	10
R205	Dual Flip-Flop	8
R601	Pulse Amplifier	1
R602	Pulse Amplifier	5
R603	Pulse Amplifier	8
S107	Inverter	4
W005	Clamp Loads	2
W640	Pulse Amplifier	1
G795	Bus Terminator	1
S202	Dual Flip-Flop	1
S603	Pulse Amplifier	1
	TC59 Control Logic	
R002	Diode Gate	2
R107	Inverter	3
R113	Diode Gate	3
R123	Diode Gate	3
R202	Dual Flip-Flop	1
R203	Triple Flip-Flop	1
R205	Dual Flip-Flop	9
R602	Pulse Amplifier	1
R603	Pulse Amplifier	4
S123	Diode Gate	4
W103	Device Selector	4
W104	Multiplexer	2
W107	Bus Receiver	3
W640	Pulse Amplifier	2

CHAPTER 5
INSTALLATION

The magnetic tape control is usually mounted in the main frame of the central processor separate from the magnetic tape transports. Therefore, the magnetic tape transports are packed individually and the cables connecting the transport and tape control are removed. In most cases, the interconnection between the tape control and the associated processor remains intact, unless the tape control is located in some place other than the main frame of the processor. There are five cables which connect to the transport; they are single 9-conductor coax with W021 Connector Boards attached at each end and are approximately 10 ft long.

5.1 PROCESSOR/TC59 CONNECTIONS

5.1.1 PDP-9/TC59 Connections

a. If the TC59 is shipped for field installation, connect the PDP-9 cabinet to the TC59 cabinet according to the field attachment kit instructions.

b. With all power off, connect the 30A twist-lock from the 834 Power Control in the TC59 to its power outlet. Connect the standard 115 Vac 3-prong cable to the available outlet in the PDP-9 841A Power Control.

c. Connect the I/O cables (7-ft W850s) to the PDP-9 and TC59 as follows.

TC59 Connection		PDP-9 Connection
Cable 1	EF 1 and 2	AB 25 and 26
Cable 2	EF 3 and 4	AB 27 and 28

d. The TC59 834 Power Control circuit breaker can be turned on with the 834 Power Control in remote selection. Do not turn on PDP-9 power.

5.1.2 PDP-15/TC59 Connections

The TC59 is a negative I/O bus device and a DW15A Positive-to-Negative Bus Converter is required when the TC59 is implemented in the positive I/O bus PDP-15 system. Refer to the PDP-15 equipment layout drawings, D-AR-PDP15-0-2, that are supplied as part of the PDP-15 Maintenance Manual, Volume 2, Engineering Drawings.

NOTE

If the PDP-15 installation includes the TC02 DECtape Control, the negative I/O bus must first be connected from the DW15A to the TC02, and then connected from the TC02 to the TC59. When the TC15 DECtape Control is used in the PDP-15 system, the negative I/O bus cable is connected directly from the DW15A to the TC59.

The following chart lists the cable connections shown on drawing D-AR-PDP15-0-2 that apply to the TC59.

Connect	From		To	
	Unit	Location	Unit	Location
Positive I/O bus cable BC09B	BA15	AB02, AB03	DW15A	AB02, AB03
Positive I/O bus cable BC09B	BA15	AB04, AB05	DW15A	AB04, AB05
Netative I/O bus cable BC09A	DW15A	AB25, AB26	TC59	EF01, EF02
Negative I/O bus cable BC09A	DW15A	AB27, AB28	TC59	EF03, EF04

5.2 CONTROL/TAPE TRANSPORT CONNECTIONS

5.2.1 TC59/TU20 Connections

Cable connections between a TC59 and a TU20 Magnetic Tape Transport are listed in the following chart:

Connect	From		To	
	Unit	Location	Unit	Location
W021/W011	TC59	A01	TU20	C04
W021/W011	TC59	A02	TU20	C02
W021/W011	TC59	A03	TU20	C05
W021/W011	TC59	B01	TU20	C01
W021/W011	TC59	B02	TU20	C03

5.2.2 TC59/TU30 Connections

Cable connections between the TC59 and a TU30 Magnetic Tape Transport are listed in the following chart:

Connect	From		To	
	Unit	Location	Unit	Location
W841/W021	TU30	D01	TC59	B01
W841/W021	TU30	D02	TC59	A02
W841/W021	TU30	D03	TC59	B02
W841/W021	TU30	D04	TC59	A01
W841/W021	TU30	D05	TC59	A03

5.2.3 TC59/TU10 Connections

Cable connections between a TC59 and a TU10 DECmagtape are listed in the following chart:

Connect	From		To	
	Unit	Location	Unit	Location
BC08C	TU10	A17, side 1	TC59	B01
*	TU10	A17, side 2	TC59	B02
BC08C	TU10	A18, side 1	TC59	A01
*	TU10	A18, side 2	TC59	A02
BC08C	TU10	A19, side 1		No connection
*	TU10	A19, side 2	TC59	A03
*Each BC08C cable has a 2-sided connector that plugs into the specified TU10 location.				

5.3 POWER-ON PROCEDURE

Step	Procedure
1	Apply power to each type of magnetic tape transport as described in the related maintenance manual or the PDP-15 Operator's Guide.
2	Turn on the PDP-9 or PDP-15. The TC59 power should come on with all control panel indicators off, except the write buffer.
3	On the magnetic tape transport, select unit 0 and put the tape at load point and ON LINE. The READY and 7-track indicators should light, and the write buffer indicators remain off.

5.4 POST-INSTALLATION TESTS

Load and run the TC59 diagnostic programs supplied, as described in the MAINDEC diagnostic program descriptions. The appropriate diagnostics are listed in Paragraph 4.4.

CHAPTER 6
ENGINEERING DRAWINGS

6.1 DRAWING INDEX

Volume 2 of this manual contains block schematics, circuit schematics, and engineering drawings necessary to understand and maintain the TC59 Magnetic Tape Transport Control. The drawings are listed in Table 6-1 in the same order as they appear in Volume 2. An introduction to DEC logic symbology used in the block schematics is provided in Appendix A.

Table 6-1
Engineering Drawings

Drawing Number	Title
D-BS-TC59-0-1	DB Register
D-BS-TC59-0-2	Data I/O Control (2 sheets)
D-BS-TC59-0-3	Device Selector
D-BS-TC59-0-4	TC59 Bus
D-MU-TC59-0-5	Module Utilization
D-BS-TC50-0-1	Motion Up Counter and Writing Data
D-BS-TC50-0-2	Command (2 sheets)
D-BS-TC50-0-3	Data Flow (2 sheets)
D-BS-TC50-0-4	Timing (2 sheets)
D-IC-TC50-0-5	Indicator Connections
D-FD-TC50-0-6	General Motion Timing
D-FD-TC50-0-7	Write Flow
D-FD-TC50-0-8	Isolated Flow Logic
D-FD-TC50-0-9	General Flow Graph
D-FD-TC50-0-10	Data Flow Delay Sequence
E-FD-TC50-0-11	Timing Flow
D-MU-TC50-0-13	Module Utilization
D-IC-TC50-0-14	Power Wiring

APPENDIX A
INTRODUCTION TO DEC LOGIC

The logic circuits of the TC59 Magnetic Tape Transport Control are assembled with DEC discrete component FLIP CHIP modules (B, R, S, and W series modules). Logic schematics (called block schematics at DEC) using these modules are usually drawn with DEC pre-MIL-STD-806B logic symbols. Except for shape representation, these logic symbols conform to MIL-STD-806B with additional features added for clarity. Both of these logic symbol standards are discussed below.

The most striking feature of DEC logic (and most puzzling to those not accustomed to it) is that a logic signal may be true (logical 1) either when it is high or when it is low depending on the logic designer's preference. In any given logic network, signals which are high-when-true and signals which are low-when-true will ordinarily exist. Not infrequently, the same logic signal will have two electrical representations, one high-when-true and the other low-when-true. In addition, the logic designer has the freedom of using the logic negation of a signal. This usage is indicated by a not sign (~), and overbar ($\overline{XXXX}$), or a minus sign preceding the signal name (Figure A-1). Whether a signal is true-when-high

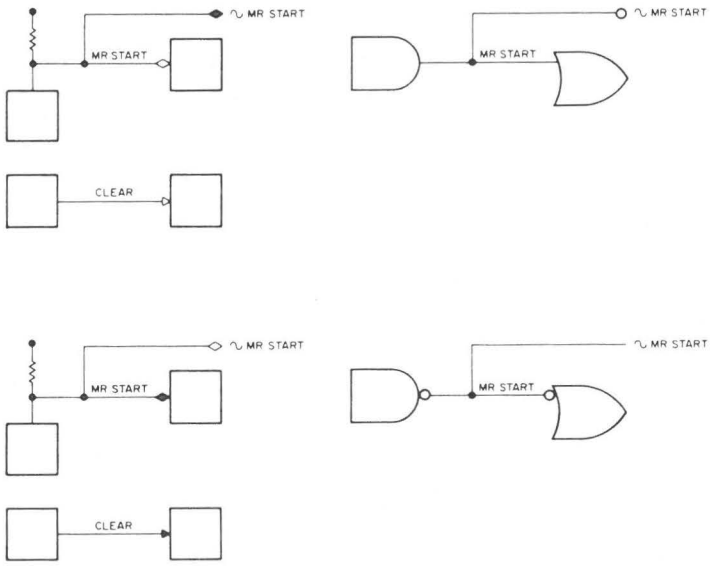


Figure A-1 Digital Logic Signals

or true-when-low is indicated by the type of diamond or arrow (open or solid) in DEC logic symbols or by the presence or absence of a small circle in MIL-STD-806B logic. This convention permits logic design without regard to the inversion properties of most DEC logic. It also permits assignment of logic packages to the realization of the design without requiring undue redesign to account for gate inversions.

Frequently in larger networks, it is convenient to show a named signal's source without a connection to its load which is located elsewhere (Figure A-2). To facilitate this, a small circle may be drawn at the end of the source line when using MIL-STD-806 logic symbols in order to show that the signal is true-when-low.

In DEC logic symbols, wired ANDs and wired ORs are not explicitly marked (Figure A-3 and A-4); they must be recognized. Due to the electrical properties of the TC59's below ground logic (ground and -3V logic levels), a wired OR will usually occur at ground (high) and a wired AND at -3V (low). The B683 is an exception.

In DEC logic, most flip-flops are drawn with four outputs: one which is high when the flip-flop is in the 1 state, one which is low when the flip-flop is in the 1 state, one which is high when the flip-flop is in the 0 state, and one which is low when the flip-flop is in the 0 state. This convention allows the condition "the flip-flop is in the 1 (0) state" to be used with gates that require either high or low inputs without manipulating highs, lows, 1s and 0s. Although a flip-flop has four logical outputs, as noted above, it has only two electrical output connections, as the 1-high and 0-low connections are electrically equivalent (same output pin), as are the 1-low and 0-high connections. Except when the lines are quite short, connections to flip-flop outputs are not usually shown explicitly (Figure A-5).

In MIL-STD-806B logic drawings, DEC shows only the 1-high and 0-high output of a flip-flop, although all outputs are considered present for the purpose of logic design.

Mention should be made of the DEC diode-capacitor-diode (DCD) gate which is both an AND gate and a logic delay (Figure A-6). This gate allows the output of a flip-flop to be sampled (with a DCD gate) at the same time the flip-flop state is changed. The flip-flop state seen by the DCD gate is the state

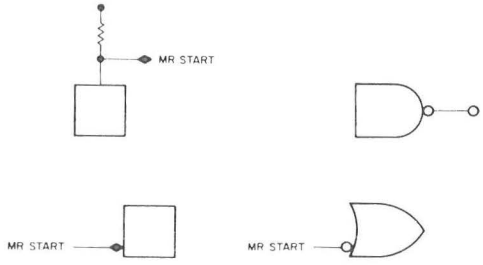


Figure A-2 Sources and Loads Shown Without Connections

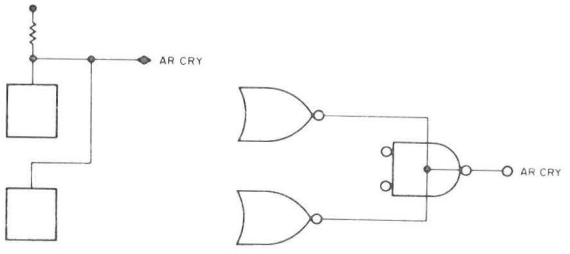


Figure A-3 Wired AND

prior to the change. The DCD gate generates an output pulse when the "level" input has been true (high) for approximately 400 ns and the "pulse" input has a 100 ns positive pulse or a positive-going (ground-going) level change with a rise time of less than 60 ns applied to it.

It is recommended that the DEC rectangular symbol for the DCD gate be used with either the older DEC logic symbols or with the MIL-STD-806B logic symbols in order to distinguish the quite different properties of the two inputs and to indicate the logic delay properties of the DCD gate. DEC logic symbols are all rectangular in shape. The function of the symbol is indicated by a descriptive notation within the rectangle. Examples of the more common symbols are shown in Figures A-7 through A-15.

DEC makes use of the electrical equivalence of various logic configurations. As an aid to understanding, symbols are drawn to represent the logic function intended by the designer rather than as a single standard symbol for each module type. Thus, a particular module type may appear as several different symbols. (See Figure A-15.)

Occasionally, the trailing edge of a signal will be used to cause some action, usually by triggering a DCD gate. This usage is illustrated in Figure A-16. For additional details on the types of logic modules available see the DEC Logic Handbook (C-105).

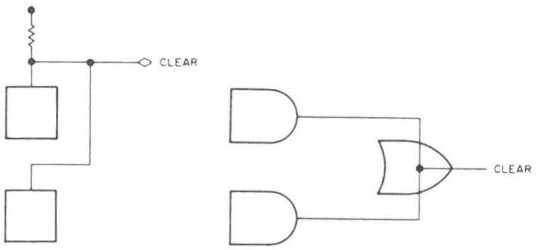


Figure A-4 Wired OR

Figure A-5 Flip-Flop Representation

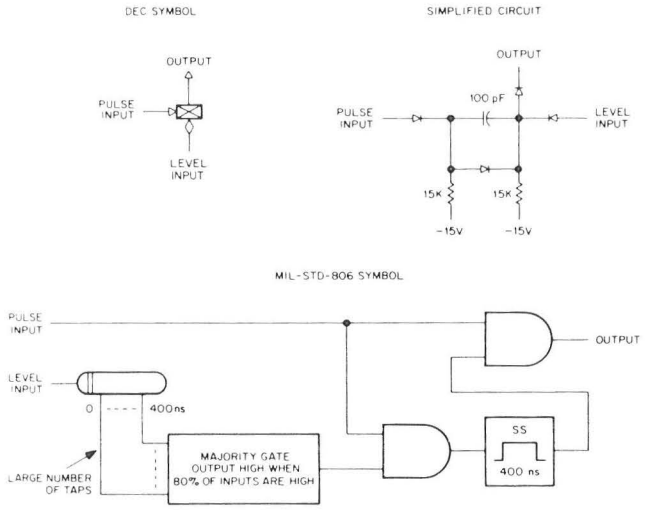


Figure A-6 DCD Gate

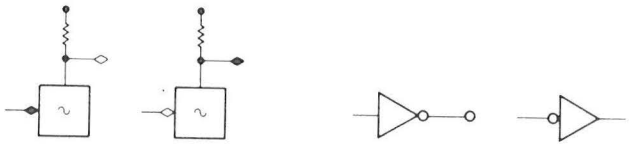


Figure A-7 Inverter (NOT Gate)

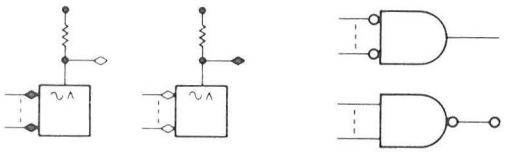


Figure A-8 AND Gate

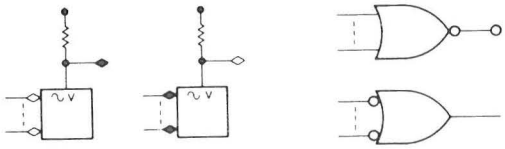


Figure A-9 OR Gate

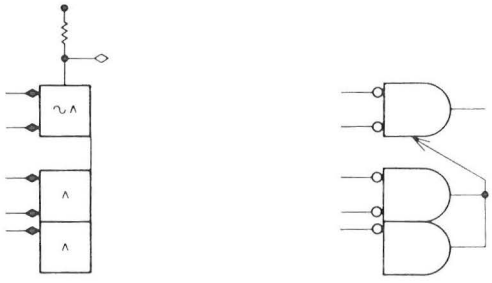


Figure A-10 Expanded Gate

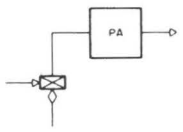
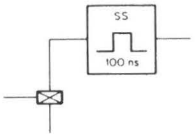


Figure A-11 Pulse Amplifier



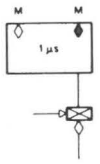
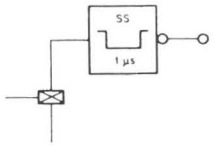
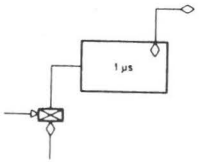


Figure A-12 Monostable Multivibrator (Single Shot)





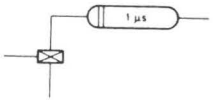


Figure A-13 Monostable Multivibrator (Delay)

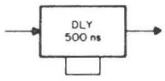
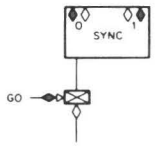


Figure A-14 Delay



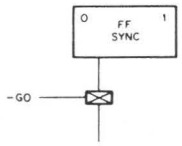


Figure A-15 Different Uses of a Particular Module

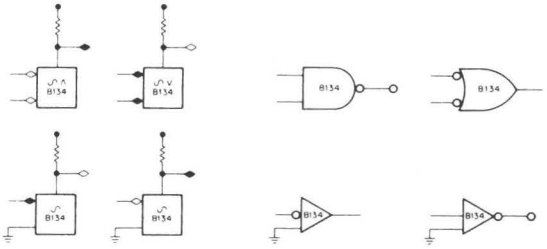


Figure A-16 DCD Usage

Digital Equipment Corporation
Maynard, Massachusetts

digital

printed in U.S.A.