Digital Equipment Corporation
Maynard, Massachusetts

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DEC-8E-HR2B-D-KD8

DATA BREAK INTERFACE OPTION

The information in this preliminary manual will become, in its final form, a part of the *PDP-8/E Maintenance Manual, Volume 2.*

PRELIMINARY

1st Preliminary Edition, August 1971

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1.0 INTRODUCTION

The Data Break interface, KD8-E, is used by peripherals to transfer large blocks of data between the peripheral and memory. This interface cannot provide all the necessary signals for such a data transfer. Consequently, the Positive I/O Bus interface must also be in the system. The concept of data transfers and the inter-relationship of the Data Break interface, the Positive I/O Bus interface, and the OMNIBUS are explained in Chapters 6 and 10 of the Small Computer Handbook - 1971. A detailed discussion of the CPU operation during a data break transfer is presented in Volume 1, Chapter 3, Section 6 of this maintenance manual. The reader should be thoroughly familiar with this referenced information to benefit from the detailed logic discussion presented in this chapter.

2.0 BLOCK DIAGRAM

Figure 2-1 is a functional block diagram of the Data Break interface. OMNIBUS signals are indicated by asterisks (on the block diagram only). When an interface receives a BRK RQST L signal from its peripheral, the request accept logic uses the next INT STROBE to assert signals that indicate acceptance of the request. These signals are used by the CP and the peripheral in preliminary operations, and by the interface priority network. The priority network compares the priority ranking of a peripheral with that of all other peripherals that make a break request at the same time. The interface of the highest ranking peripheral generates a PRIORITY signal that allows its CP Control logic to assert CP control lines. This action enables the peripheral to assume control of the CP Major Register gating and to directly address, via the BKMA Register logic, memory locations associated with the data transfer. The direction of transfer and the type of transfer are controlled by the interface data transfer logic. When the cycle select logic indicates that the true Break (BK) cycle is in progress, the data word is transferred to, or from, the address indicated by the BKMA Register logic. If the data transfer is from the peripheral, the data word is placed on the DATA 0-11 lines of the OMNIBUS by the data transfer logic.

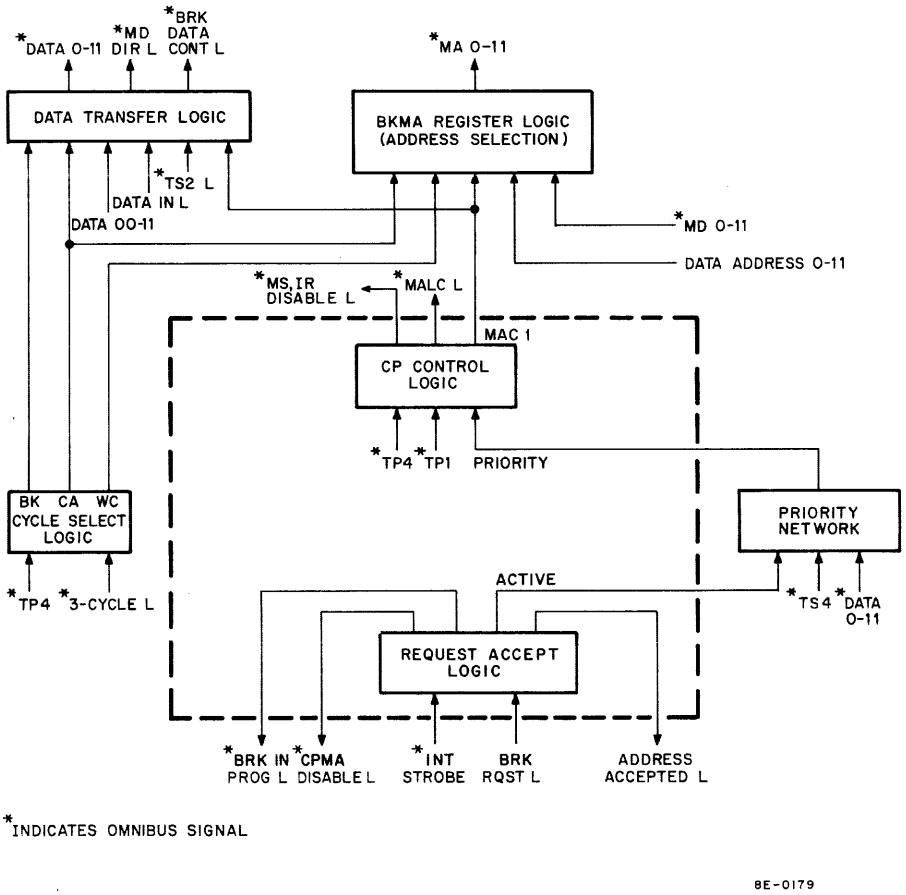


Figure 2-1 Block Diagram, Data Break Interface

3.0 DETAILED LOGIC

3.1 CP REGISTER CONTROL LOGIC

Figure 3-1 shows the CP Register control logic. The NBR flip-flop determines if the interface can assert the CP register control lines in response to a break request from the peripheral. This determination is based on the state of the NEW BRK OK L signal, which is asserted within the interface when conditions allow a data transfer (the NEW BRK OK L signal is discussed fully in Paragraph 3.2, Cycle Select logic). If the NEW BRK OK L signal has been asserted by the interface and the BRK RQST L signal has been asserted by the peripheral, the NBR flip-flop is set by the INT STROBE signal (see Figure 3-1). The 0-output of NBR then sets the ACTIVE flip-flop, which asserts the BRK IN PROG L and CPMA DISABLE L signals. The CPMA DISABLE L signal conditions a flip-flop on the Major Register Control module (see Volume 1, Figure 3-102) so that TP4 can clear the flip-flop; the resulting signal, MAC L, removes the CPMA Register outputs from the MA lines. The BRK IN PROG L signal, which can be displayed on the programmer's console, ensures that only data break devices place priority information on the DATA lines during TS4.

When TS4 is entered, the 1-output of the ACTIVE flip-flop asserts the priority signal for this ('our') interface. If other peripherals have made break requests at INT STROBE time, each peripheral's interface asserts a priority signal at TS4 time. The priority network (see Paragraph 3.3) in each active interface examines these signals to determine if it has the highest priority of all the devices currently attempting to use the data break system. If 'our' peripheral is not of sufficiently high priority, it must wait until the next TS4 signal; at that time the priority signals are again compared. If 'our' peripheral has highest priority, the D inputs of the MAC1 and MAC2 flip-flops are taken to a positive voltage; the flip-flops are then set at TP4 time. The 1-output of MAC1 not only asserts the MS, IR DISABLE L signal, which places the CP in the DMA state, but also conditions the MALC flip-flop so that it can be set when the TP1 pulse occurs. The 1-output of MALC then asserts the MALC L signal, which ensures that the CP MS Register and the CPMA Register will resume normal operation in the correct major state and at the correct memory address, respectively.

Note that ADD ACCEPTED L is asserted during TS1 of the first cycle following INT STROBE, regardless of the outcome of the priority check. This signal clears the break request flip-flop in the peripheral, allowing the peripheral to make another request when it is ready. At TP1 time, the NBR flip-flop is cleared, also regardless of what occurs in the priority network. Thus, this flip-flop is active for only the short time necessary to indicate acceptance of the break request. In contrast, the ACTIVE flip-flop is cleared only at TP2 time of a true break cycle (defined and explained in the following section), which can be delayed for some time by priority considerations. Both NBR and ACTIVE are used extensively as control signals in other functional sections of the interface.

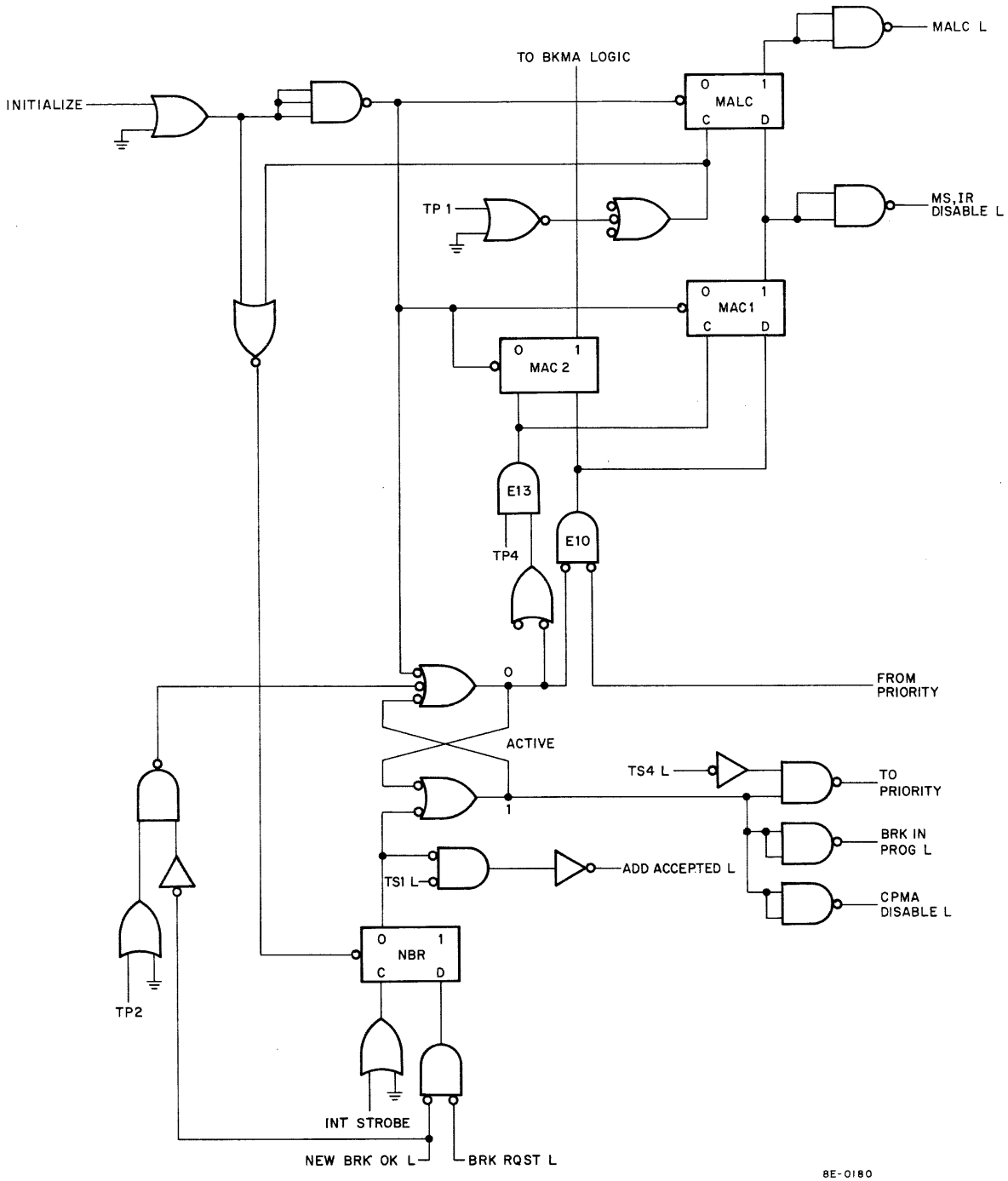


Figure 3-1 CP Register Control Logic

3.2 CYCLE SELECT LOGIC

After 'our' interface takes control of the CPU, as described in the preceding section, a data transfer can be made. The CPU is in the DMA state and remains in this state as long as MS, IR DISABLE L remains low. Each timing cycle (a 'slow' cycle of 1.4 μs) that occurs during the DMA state is used by the interface/peripheral to accomplish tasks necessary for the data transfer. The actual transfer of the data word takes place during the Break (BK) cycle of operation. For 1-cycle peripherals only the BK cycle is necessary; however, 3-cycle devices require a Word Count (WC) cycle and a Current Address (CA) cycle before the BK cycle. This section describes the method of selecting each of the three cycles of operation; the details of what occurs during each cycle are presented in succeeding sections, except that certain BK cycle operations are detailed here.

Figure 3-2 shows the Cycle Select logic. When one of the three flip-flops shown (WC, CA, and BK) is set at TP4 time, the respective cycle of operation is entered. If the peripheral is a 3-cycle device, the 3 CYCLE line is wired to ground within the peripheral. Thus, pin 2 of the DEC 8271 IC is a positive voltage (high). This high is gated to the D-input of the WC flip-flop, providing the 8271 load (L) input is also high and the shift (S) input is low (see Volume 1, Appendix A for details about the 8271 IC). This provision is met each time the interface accepts a break request from the peripheral (the 1-output of NBR goes high at INT STROBE time). The WC flip-flop is set at TP4 time--the same TP4 at which MAC1 and MAC2 are set (because the D input of both the CA and BK flip-flops is low, TP4 clears these flip-flops). Note that TP4 is NANDed with the output of a NOR gate (E18) that can be enabled by the 0-output of the ACTIVE flip-flop. This means that the WC flip-flop can be set even though access to the CPU has been claimed by another peripheral during TS4 (the ACTIVE flip-flop is set prior to the priority check and remains set until TP2 time of the BK cycle). If this happens, the operations that normally occur during the WC cycle are suspended for at least one cycle. One of these normal operations is the clocking of the 8271 flip-flops at TP4 time. To suspend this clocking process, the 8271 is placed in the 'hold' mode by the NBR and MALC flip-flops (see Table 3-1). The NBR flip-flop is cleared at TP1 time of the suspended cycle, while the MALC flip-flop remains in the clear state (MALC is set at TP1 of a normal cycle). The 'hold' conditions remains in effect until 'our' peripheral has priority; at this time a normal WC cycle is entered.

Table 3-1
8271 IC Control Signals

NBR F/F	MALC F/F	S	L	8271 IC Control State
Clear	Clear	Low	Low	Hold
Set	--	Low	High	Parallel Load
Clear	Set	High	Low	Right Shift

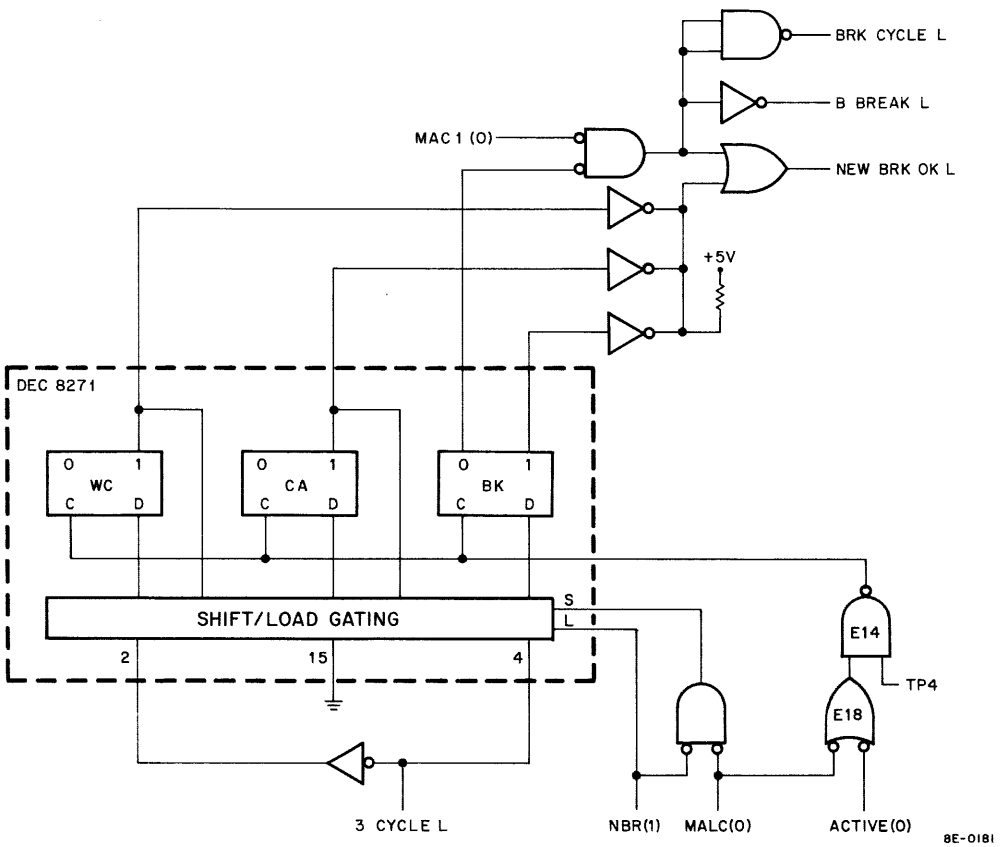


Figure 3-2 Cycle Select Logic

At TP1 time of the normal WC cycle NBR is cleared and MALC is set (NBR remains clear until a new break request is accepted). As Table 3-1 shows, the 8271 is placed in the 'right-shift' mode. In this mode the three flip-flops comprise a shift register that is right-shifted by clock pulses. Thus, TP4 of the WC cycle causes the high at the 1-output of WC to be shifted into the CA flip-flop (CA is set, while WC is cleared). The CA flip-flop, also, can be set regardless of the results of the TS4 priority check (as before, the 0-output of ACTIVE enables TP4 to clock the flip-flop). The normal CA cycle operations are then suspended for at least one timing cycle. At TP1 of the suspended cycle MALC is cleared; the 8271 is placed in the 'hold' mode, preventing TP4 of the suspended CA cycle from clocking the flip-flops. When 'our' peripheral has priority, the normal CA cycle is entered, MALC is set at TP1 time, and the 8271 is again placed in the 'right-shift' mode. The CA cycle operations are carried out and at TP4 time the BK flip-flop is set, while the CA flip-flop is cleared.

The BK flip-flop, too, is set regardless of priority. If another peripheral has priority, the normal BK cycle operations are suspended and the 8271 is placed in the 'hold' condition for at least one cycle. When 'our' peripheral has priority, the normal BK cycle is entered at TP4. The 0-output of BK is NANDed with the 0-output of MAC1 to assert NEW BRK OK L, BRK CYCLE L, and B BREAK L (see Figure 3-2). Because MAC1 is cleared at TP4 if another peripheral has priority, these signals are asserted only during a normal break cycle. NEW BRK OK L tells the NBR flip-flop that data is about to be transferred and that a break request can be accepted at the next INT STROBE time; BRK CYCLE L is applied to the programmer's console display to indicate the normal or 'true break' cycle; B BREAK L clocks the data into or out of the peripheral's buffer register, depending upon the direction of transfer. At TP2 time of the true BK cycle the ACTIVE flip-flop is cleared, negating the CP Register control lines. If the peripheral has not asserted the BRK RQST L signal before INT STROBE time of this cycle, NBR and ACTIVE remain clear and the CP Register control lines remain negated. MAC1, MAC2, and BK are cleared at TP4 time, while MALC is cleared at TP1 time of the next timing cycle (because ACTIVE is clear when this TP4 occurs, the 0-output of MALC is used to enable TP4 to clock the BK flip-flop). If a break request was made before INT STROBE time, the WC flip-flop is set at the same time that the BK flip-flop is cleared; the break operation is repeated as many times as necessary.

Figure 3-3 is a timing diagram relating the signals discussed in this section and in the preceding section, CP Register control logic (the time scale does not reflect true processor timing; refer to Volume 1, Chapter 3 for timing information).

3.3 PRIORITY LOGIC

Figure 3-4 shows the priority logic. Each peripheral interface contains a nearly identical circuit; differences exist only in the placement of jumper wires, which are designated A_0-A_{11} and B_0-B_{11} in

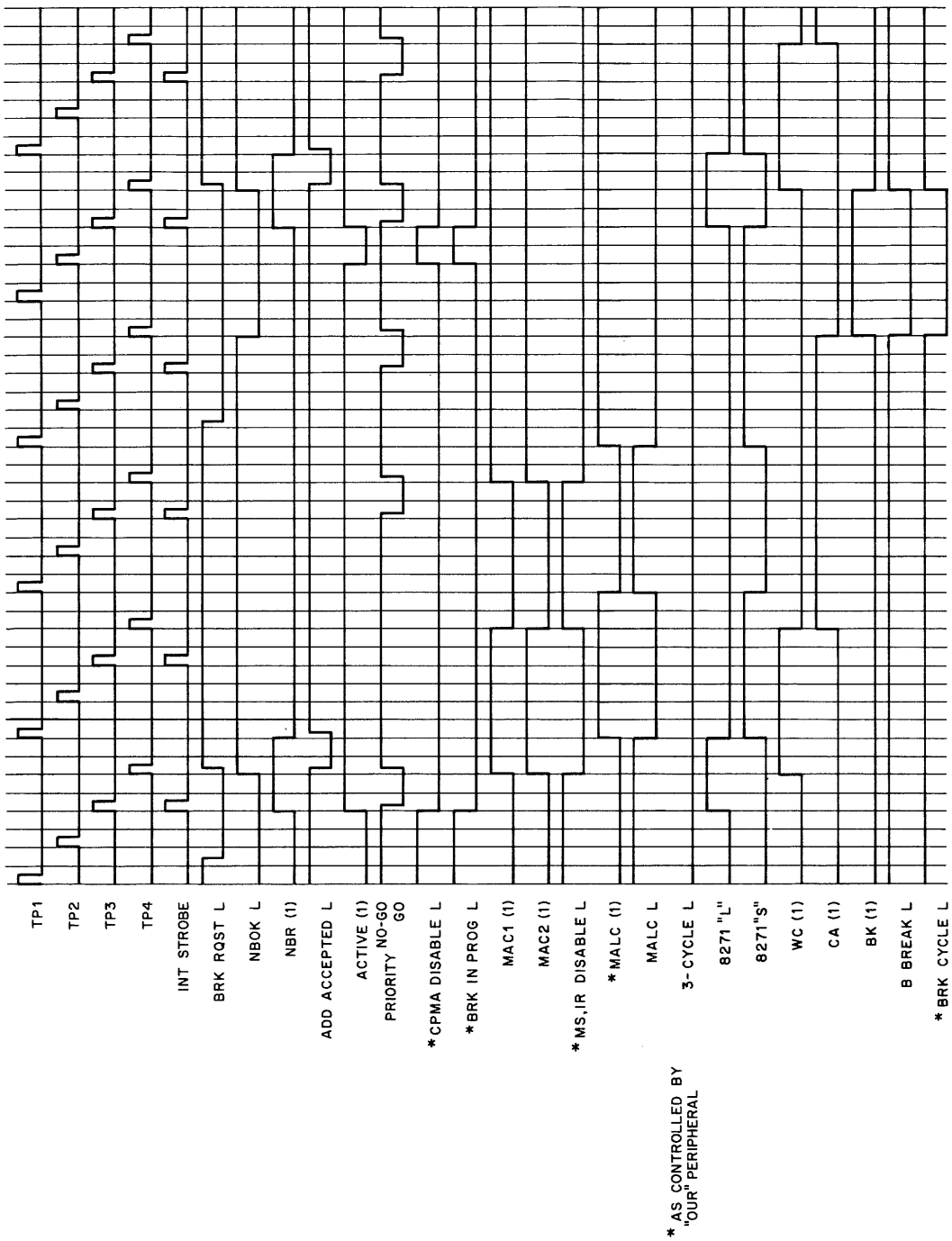


Figure 3-3 Timing, Register Control and Cycle Select Logic

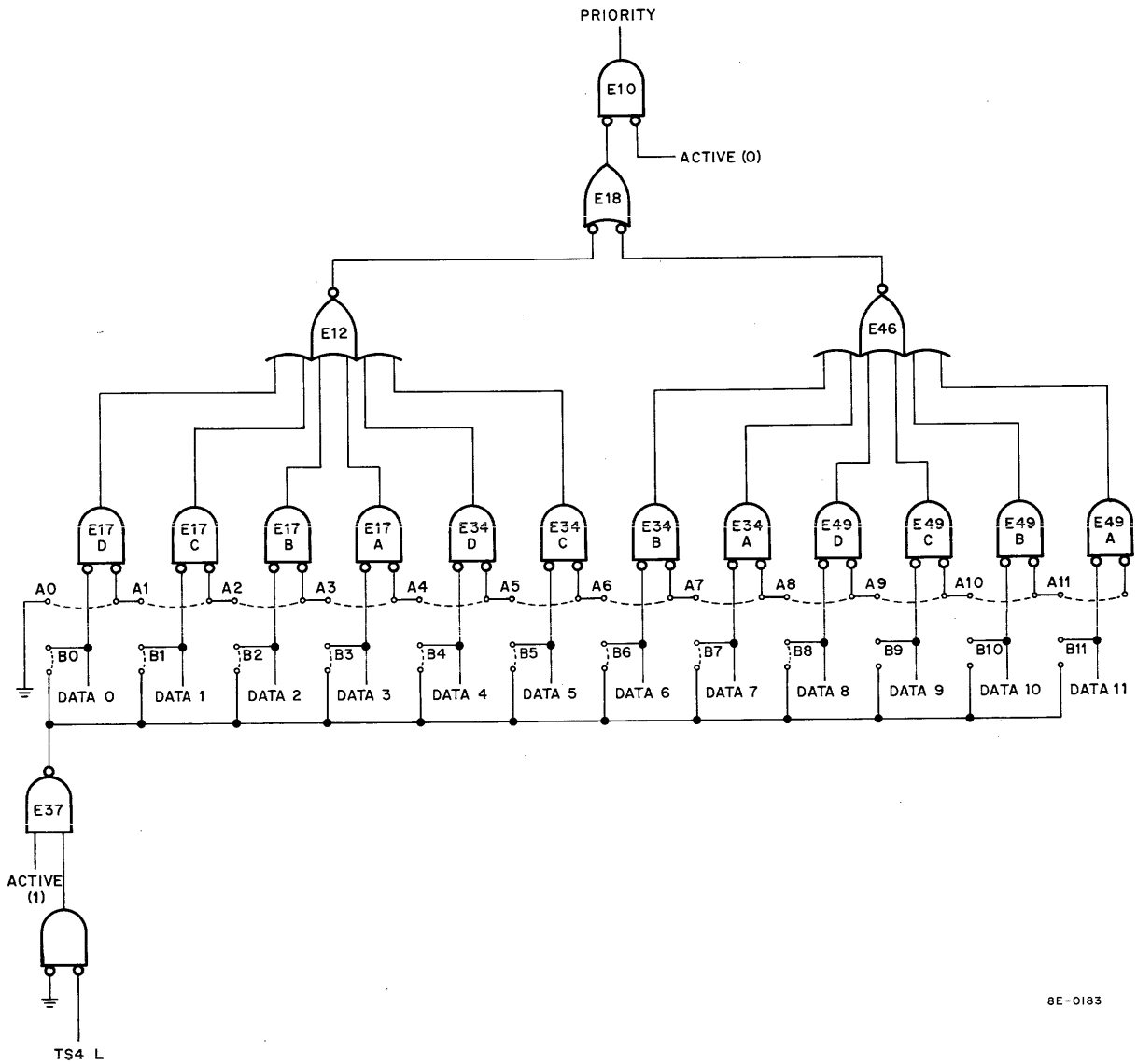


Figure 3-4 Priority Logic

Figure 3-4. The priority of a peripheral is established on the interface by removing a particular A jumper (all A jumpers are wired in place during production of the interface) and installing the corresponding B jumper. For example, to establish a "0" priority for 'our' peripheral, remove A_0 and install jumper B_0. Note that this action disables all 12 NAND gates (ICs E17, E34, and E49). Thus, the output from NOR gate E18 is low. When the interface accepts a break request from the peripheral, the ACTIVE flip-flop is set at INT STROBE time. The 0-output of ACTIVE enables NAND gate E10 to assert the PRIORITY signal; therefore, 'our' interface/peripheral begins the data break operation. Because 'our' peripheral has only to request a break for that request to be granted, 'our' peripheral has been assigned highest priority. No other interface can have its A_0 jumper removed, nor its B_0 jumper connected.

As many as 11 other peripherals can have a break request accepted by their respective interfaces at INT STROBE time. No matter what priority has been established for these peripherals, each of the 11 interfaces has an A_0 jumper in place. Note that when 'our' interface ACTIVE flip-flop is set, NAND gate E37 brings the DATA 0 line low ('our' B_0 jumper is in place) during TS4 time. Because all interfaces monitor the DATA lines, NAND gate E17D of each other interface is enabled. Thus, these interfaces cannot assert their PRIORITY signals as long as 'our' peripheral requests data breaks.

As another example, consider what happens if 'our' peripheral ranks only third highest in the peripheral priority structure. This priority is established on 'our' interface by removing jumper A_2 and connecting jumper B_2. Because jumpers A_0 and A_1 are left in place, two other interfaces can keep 'our' peripheral from beginning a data break operation. If the second highest priority peripheral has a break request accepted at the same time 'our' peripheral's request is accepted, its interface brings the DATA 1 line low during TS4 time. NAND gate E17C on 'our' interface is enabled and the PRIORITY signal remains negated. Until this other peripheral has completed the data break operation, our peripheral remains inactive. As has been implied, priority decreases from left to right, i.e., the lower the priority of the peripheral, the higher the number of the A jumper removed and B jumper installed. Thus, to establish priority on the lowest ranking peripheral's interface, remove jumper A_{11} and install jumper B_{11}.

3.4 BKMA REGISTER LOGIC

Figure 3-5 shows the BKMA Register logic. This logic enables the peripheral to reference memory locations associated with the data break transfer. A peripheral that has made a break request must provide its interface with a memory address via the DATA ADDRESS 0-11 lines (see Figure 3-5). This address is gated through DEC 8266 (see Volume 1, Appendix A for details of this IC) to the parallel-load inputs of the 8271 ICs (the gating for bits 0 through 10 is identical; thus, the description and the illustration detail events for only bit 0 and bit 11). When the interface accepts the peripheral's request

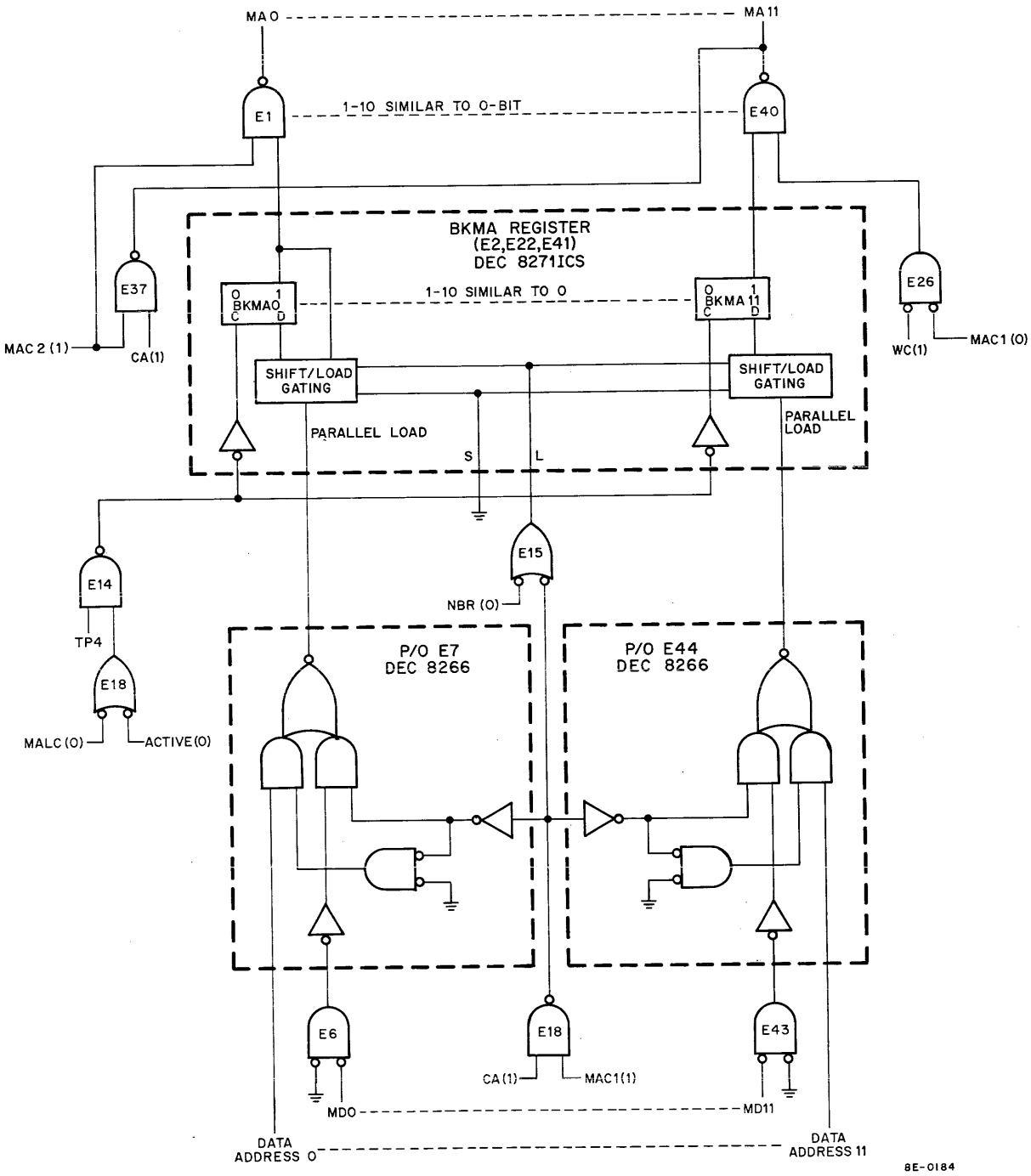


Figure 3-5 BKMA Register Logic

at INT STROBE time, the 0-output of the NBR flip-flop enables NOR gate E15, placing the 8271 ICs in the 'load' condition (see Table 3-1). At the same time, one input of NAND gate E14 is sent high by the 0-output of the ACTIVE flip-flop. At TP4 time, E14 is enabled and the BKMA Register flip-flops are loaded with the address on the DATA ADDRESS lines. If the peripheral has priority, the MAC2 flip-flop is set, also at TP4 time; the 1-output of the flip-flop enables NAND gate E1, placing DATA ADDRESS bit 0 on the MA0 line. If the peripheral does not have priority, the address is retained in the BKMA Register but not gated onto the MA lines until MAC2 is set at a later TP4 time. The NBR flip-flop is cleared at TP1 time, regardless of the outcome of the priority check, and NOR gate E15 places the 8271 ICs in 'hold'.

If the peripheral is a 1-cycle device, the address placed on the MA lines at TP4 time is that of the memory location to or from which the data word is to be transferred. Note that NAND gate E26 is enabled in this situation (the BK flip-flop of the Cycle Select logic is set, the WC flip-flop is clear). Thus, the full 12- or 15-bit address supplied by the peripheral is placed on the MA lines. However, if the peripheral is a 3-cycle device, the WC cycle is entered first after a break request is accepted. NAND gate E26, disabled during the WC cycle, in turn disables NAND gate E40. Thus, DATA ADDRESS bit 11 is not gated onto the MA11 line; rather, MA11 is high, logic 0, during the cycle. The address placed on the MA lines during the WC cycle is that of the memory location containing the peripheral's WC register; this address is hard-wired in the peripheral and is even (bit 11 is logic 0) so that the CA register can be easily referenced during the next timing cycle, as is explained in the next paragraph.

During the WC cycle, the count in the WC Register is transferred from memory to the CP, incremented, and returned to the register. At TP4 time, the WC flip-flop is cleared and the CA flip-flop is set. If the peripheral still has priority, NAND gate E37 is enabled, pulling the MA11 line low. The MA0-10 lines carry the same address as during the WC cycle. Thus, the peripheral's hard-wired address is incremented and the new address is that of the memory location containing the peripheral's CA Register.

At the same time (TP4) that the CA Register address is placed on the MA lines, the CA flip-flop enables NAND gate E18. This gate, in turn, enables NOR gate E15, which places the BKMA Register in the 'load' condition. Also, NAND E18 removes the DATA ADDRESS lines from the parallel-load inputs of the BKMA Register, substituting the MD0-11 lines. Note that these actions do not take place prior to the negative transition at the BKMA Register flip-flop clock inputs. Thus, the BKMA Register retains the WC Register address until TP4 of the CA cycle.

During the CA cycle, the address in the CA Register is transferred from memory to the CP, incremented, and returned to the register. The address before incrementation (the current address) is that

of the location to or from which the data is to be transferred. Thus, this current address must be placed in the BKMA Register, and transferred from there to the MA lines at the beginning of the BK cycle. The current address is sent from memory to the CP via the MD lines and remains on these lines for the entire CA cycle. Therefore, at TP4 time of the CA cycle, the BKMA Register parallel-load inputs reflect the current address. Because the BKMA Register is in the 'load' condition, the current address is loaded into the register. At approximately the same time, the BK flip-flop is set, while the CA flip-flop is cleared. Because E37 is disabled and E26 is enabled, the contents of BKMA0-11 are placed on the MA0-11 lines.

Also at this TP4 time, NAND gate E18 is disabled. This action removes the MD lines from the parallel-load inputs, selects the DATA ADDRESS lines, and places the BKMA Register in 'hold'. Note that the MALC flip-flop keeps NOR gate E18 enabled throughout the BK cycle (ACTIVE is cleared at TP2 time), if the peripheral has priority. These two gates ensure that the BKMA Register is ready to begin a new transfer, if the interface accepts a break request at INT STROBE time of the BK cycle.

During the BK cycle, the data word is transferred to or from the location specified by the current address. The logic that accomplishes this transfer through the interface is covered in the following section, which also details special operations of all three cycles.

3.5 DATA TRANSFER LOGIC

Figure 3-6 shows the data transfer logic. This logic controls the direction and type of data transfer. Table 3-2 shows the relationship between the type and direction of transfer and the signal levels of the various control lines. The table should be used with Figure 3-6 for a good understanding of the logic details.

Table 3-2
Control Signals, Cycle, Type, and Direction of Transfer

Cycle	WC	CA		BK			
Direction of Transfer	In	In		In			Out
Type of Transfer	Word Count Increment	Current Address Increment	No Current Address Increment	MB Increment	ADM	12-Bit Data Word	12-Bit Data Word
MD DIR L	High	High	Low	High	High	High	Low
BRK DATA CONT L	Low	Low	Low	Low	Low	High	High
DATA IN L	Low	Low	Low	High	Low	Low	High
MB INCREMENT L	High	High	High	Low	Low	High	High
CA INC INH L	High	High	Low	High	High	High	High

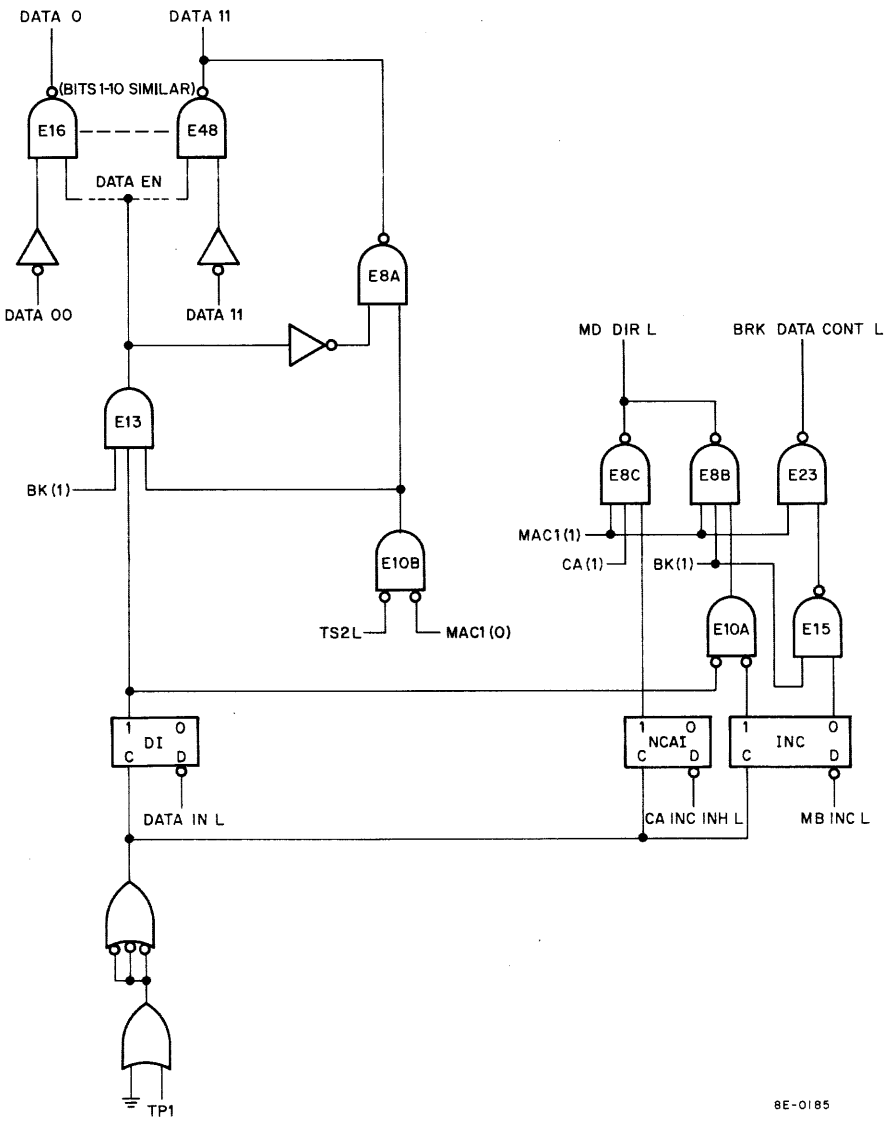


Figure 3-6 Data Transfer Logic

If the transfer is to be from memory to the peripheral, a 12-bit data word is transferred from the addressed location via the Positive I/O Bus interface. The Data Break interface asserts the MD DIR L signal so that the data word is re-written in the memory location during the write half of the timing cycle. NAND gate E8B (Figure 3-6) is used to ground the MD DIR line. The BK(1) and MAC1(1) signals ensure that the true break cycle is in progress. The third input to E8B is high because NAND gate E10A is enabled. E10A is controlled by the DI (Data In) and INC (INCrement) flip-flops, which are both cleared at TP1 time of an output (from memory) transfer.

Note that the peripheral need not assert any control lines for an output transfer. However, if an input (to memory) transfer is to be carried out, the peripheral usually grounds the DATA IN line (exceptions are noted in the discussion). The DI flip-flop is set at TP1 time of the first cycle of the data break. If the peripheral is a 3-cycle device, this first cycle is a WC cycle. Since the BK flip-flop is clear, NAND gate E13 is disabled (note that the DI flip-flop is significant in the operation of E13 only during the BK cycle; thus, the decision to set or clear this flip-flop, by asserting or negating the DATA IN L signal, need not be made during either the WC or the CA cycles). One input of NAND gate E8A is high. If this is a normal WC cycle (this interface's peripheral has priority), E8A is enabled during TS2 by NAND gate E10B, pulling the DATA 11 line low. This single bit of data is transferred to the CPU and added to the word count, which is brought to the CPU from the WC Register, providing the BRK DATA CONT L signal is asserted by the interface. NAND gate E23 is used to assert this signal. Because this is a WC cycle, NAND gate E15 is disabled, enabling E23 (MAC1 is set because the peripheral has priority). Therefore, the word count is incremented. Because the MD DIR L signal is negated (both E8C and E8B are disabled during the WC cycle), this new word count is placed in the WC during the write half of the memory cycle.

During the CA cycle of the 3-cycle transfer, the current address is incremented in much the same way as the word count. Again, DATA 11 is pulled low by E8A during TS2 if the peripheral has priority. E23 asserts the BRK DATA CONT L signal, which enables DATA 11 and the current address to be added in the CPU. If the MD DIR L signal is negated, the new address is sent to the CA Register during the write half of the cycle. Note that the MD DIR L signal is negated only if the NCAI (No Current Address Increment) flip-flop is clear. This flip-flop is clocked at TP1 of a timing cycle and is normally clear. However, the peripheral can ground the CA INC INH line, causing the NCAI flip-flop to be set at TP1. NAND gate E8C then asserts the MD DIR L signal during the CA cycle. Thus, although the current address is incremented as usual, the original address (the one that was in the CA Register at the beginning of the cycle) is returned to the CA Register during the memory write.

During the BK cycle of operation, whether of a 1- or 3-cycle operation, an input or output transfer can take place. As described at the beginning of this section, there is only one type of output data transfer, i.e., the transfer of a 12-bit data word from the addressed location. However, there are

three types of input transfer that can be carried out. One of these is similar to the transfer that takes place during the WC and CA cycles, and is designated MB Increment. To accomplish this transfer, the peripheral grounds only the MB INC line. At TP1 the INC flip-flop is set, while the DI flip-flop is cleared. NAND gates E10A and E15 are disabled by the INC flip-flop. Thus, E32 asserts the BRK DATA CONT L signal and, because E8C is disabled during the BK cycle, E8B negates the MD DIR L signal. During TS2 the DATA 11 line is pulled low by E8A. This single bit is transferred to the CPU, where it is added to the data word that is brought from the addressed memory location. The incremented data is then sent back to the addressed location during memory write.

Another type of input transfer, similar to the MB Increment, is designated Add To Memory (ADM). The peripheral grounds the MB INC and DATA IN lines so that both the DI flip-flop and the INC flip-flop are set at TP1. During TS2 of the true break cycle, a 12-bit data word carried on the peripheral's DATA 00-11 lines is gated through the interface to the OMNIBUS DATA lines. This data is added in the CPU to the data brought from the addressed memory location, and the result is rewritten in the memory location.

The third type of input transfer is that of a 12-bit data word to the addressed memory location. The peripheral grounds only the DATA IN line; thus, TP1 sets the DI flip-flop, while clearing the INC flip-flop. NAND gate E15 is enabled and causes NAND gate E23 to negate the BRK DATA CONT L signal. NAND gate E10A is disabled by the 1-output of DI and, in turn, disables E8B. Because E8C is also disabled, the MD DIR L signal is again high. During TS2, a 12-bit data word is placed on the OMNIBUS DATA lines and transferred to the addressed memory location.

3.6 WC OVERFLOW LOGIC AND EMA REGISTER LOGIC

Figure 3-7 shows the WC OVERFLOW logic and the EMA REGISTER logic. The WC OVERFLOW L signal is generated by the interface during either a normal WC cycle or a true BK cycle if the OMNIBUS OVERFLOW L signal is asserted by the CPU. OVERFLOW L is asserted during a WC cycle to indicate that the last word of a block is about to be transferred. WC OVERFLOW L is then used by the peripheral to terminate the data break operation. During a BK cycle the OVERFLOW L signal is asserted to indicate that an input transfer has resulted in assertion of the CPU Carry Out L signal. In this case WC OVERFLOW L is used in the peripheral as directed by the program.

The EMA REGISTER logic is used to specify the complete 15-bit memory address to or from which data is to be transferred. EMA0 is the MSB of the 15-bit address, while MA11 is the LSB (see Chapters 9 and 10 of the Small Computer Handbook - 1971 for definitions of OMNIBUS and External bus signals relating to extended memory). If the computer contains only the basic 4K of memory, EMA0, EMA1, and EMA2 are logic 0. When memory is extended (up to 32K, if desired), these three most significant bits are used to indicate which memory field is to take part in the data transfer. The peripheral

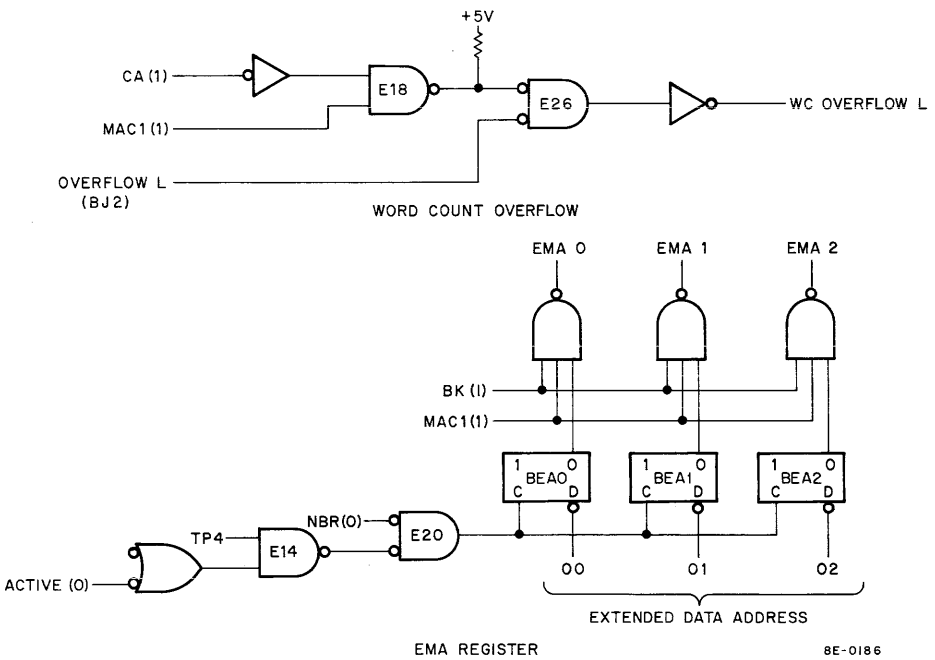


Figure 3-7 Word Count Overflow and EMA Register Logic

specifies the memory field via the External bus Extended Data Address 00-02 lines (see Figure 3-7). This field address is loaded into the BEA (Break Extended Address) register at TP4 time of the first cycle of the break operation (refer to Figure B-4). If the peripheral is a 3-cycle device, the first cycle is the WC cycle. However, note that the BEA register information is placed on the EMA lines only during a true BK cycle. Thus, for a 3-cycle device the WC and CA registers must be located in memory field 0, the basic 4K. The location to or from which data is to be transferred can be contained in an extended memory field.

4.0 MAINTENANCE

There are no specific maintenance procedures for the KD8-E, itself. Each DEC peripheral has an associated MAINDEC or exerciser program that enables the technician to maintain both the option and the KD8-E interface.

General information concerning corrective maintenance is included in Volume 1, Chapter 4. The technician will find this material helpful. The interface schematic, E-CS-M8360-0-1, indicates important test points, IC locations, and pin numbers and should be used whenever maintenance is being performed.

The KD8-E connects directly to a single peripheral via two cables that are supplied with the interface (see the Small Computer Handbook - 1971, Chapter 10 for cabling rules and suggestions). Each cable connects to the interface with a 40-pin Berg connector and to the peripheral with a DEC M953A cable connector. From-To information for the cable is given in Table 4-1 (the cables are identical; see Chapter 10 of the Small Computer Handbook - 1971 for details concerning proper connection of the cables).

Table 4-1
KD8-E Cable Information

From (M953A Cable Conn.)	To (Berg Conn.)	From (M953A Cable Conn.)	To (Berg Conn.)
Gnd	A	Gnd	Y
Gnd	B	M2	Z
Gnd	C	Gnd	AA
B1	D	L1	BB
Gnd	E	Gnd	CC
D2	F	P2	DD

(continued on next page)

Table 4-1 (Cont)
KD8-E Cable Information

From (M953A Cable Conn.)	To (Berg Conn.)	From (M953A Cable Conn.)	To (Berg Conn.)
Gnd	H	Gnd	EE
D1	J	M1	FF
Gnd	K	Gnd	HH
E2	L	S2	JJ
Gnd	M	Gnd	KK
E1	N	P1	LL
Gnd	P	Gnd	MM
H2	R	T2	NN
Gnd	S	Gnd	PP
H1	T	S1	RR
Gnd	U	Gnd	SS
K2	V	V2	TT
Gnd	W	Gnd	UU
J1	X	Gnd	VV

Pins A2, B2, U1 and V1 on M953A not used.

Pins A1, C1, F1, K1, N1, R1, T1, C2, F2, J2, L2, N2, R2, and U2 on M953A are ground pins.

5.0 SPARE PARTS

(to be supplied)

Digital Equipment Corporation
Maynard, Massachusetts

digital

printed in U.S.A.

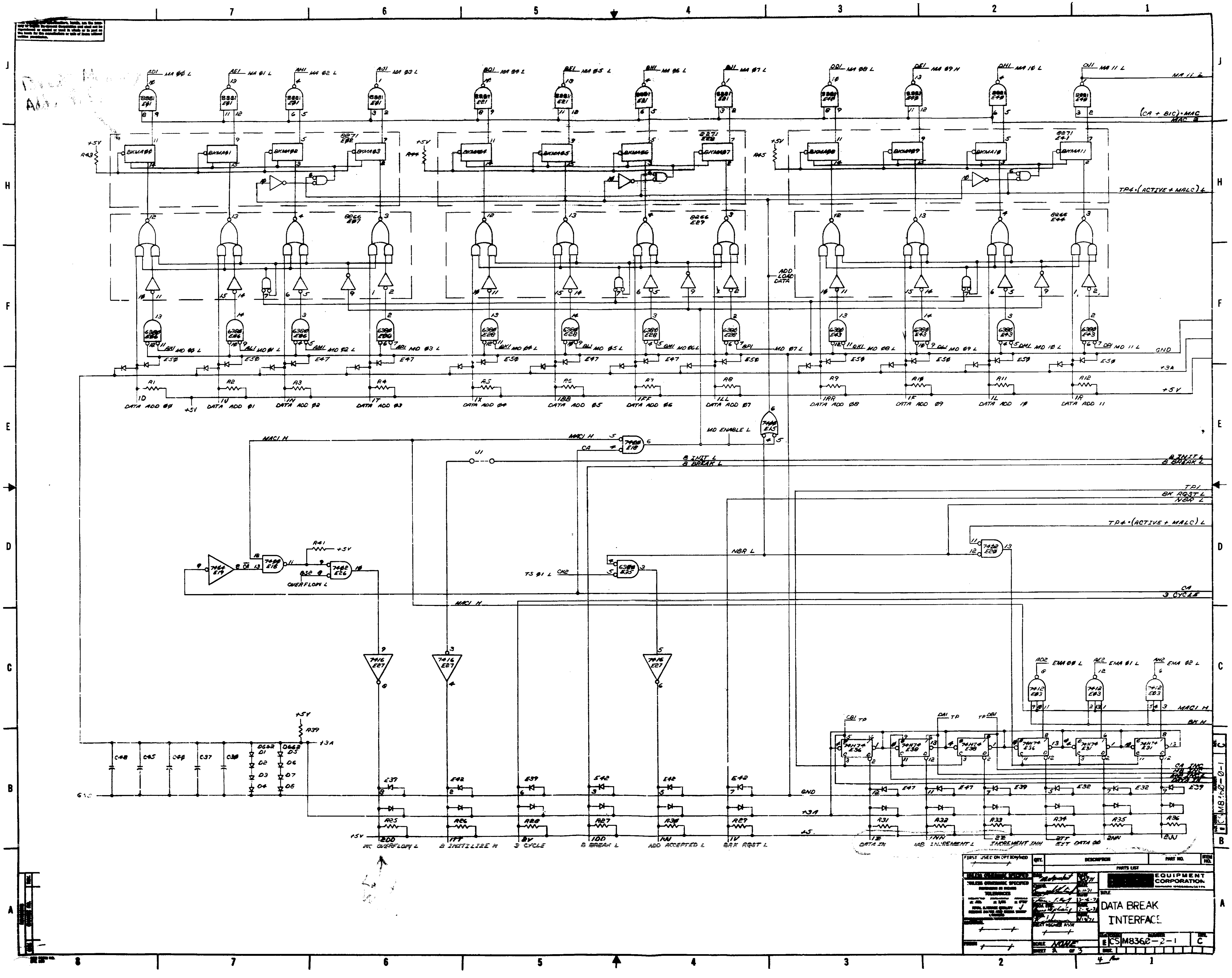
MASTER DRAWING LIST

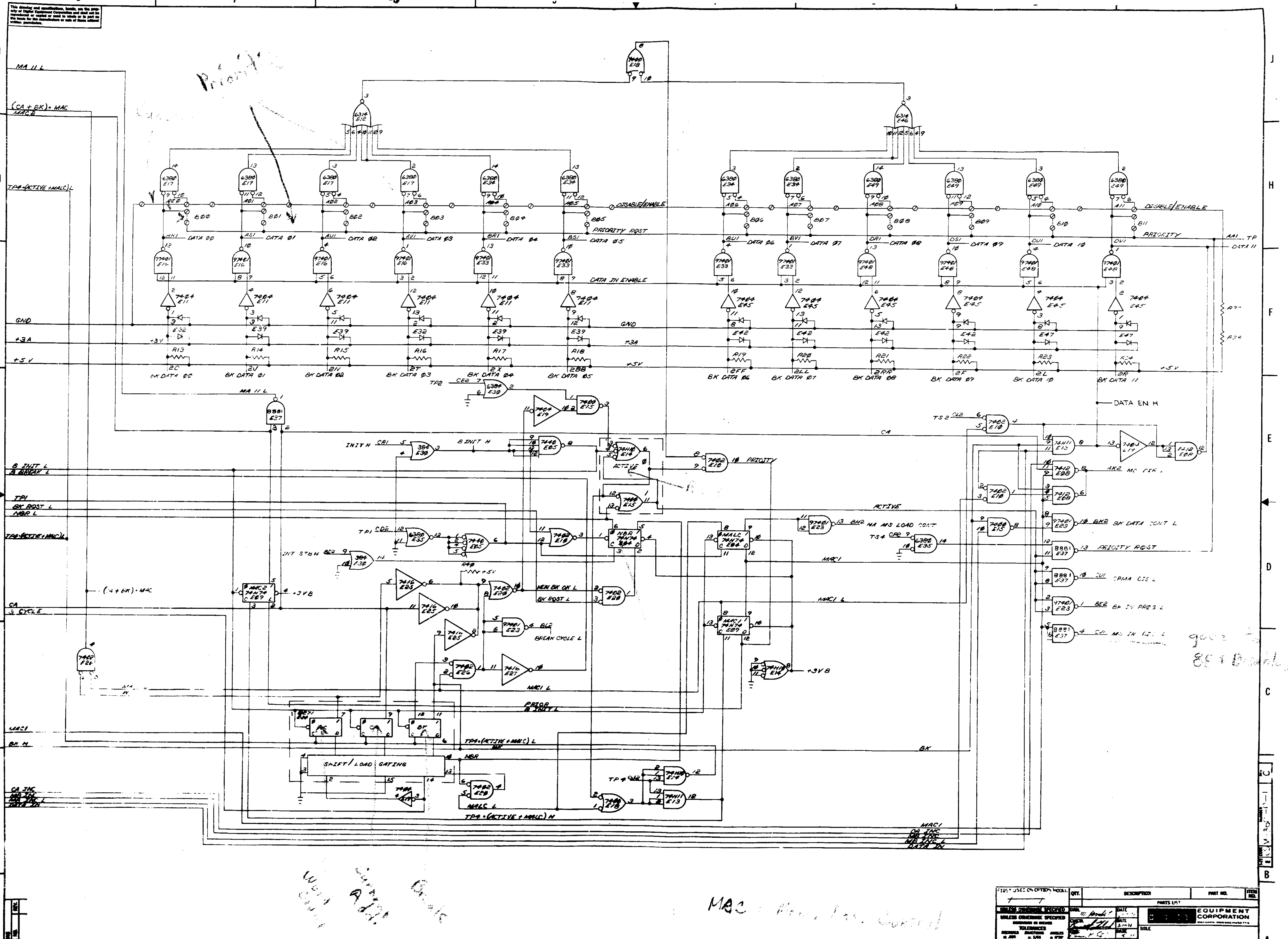
DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
A-PL-KD8-E-0		1	DATA BREAK INTERFACE (PARTS LIST)
E-CS-M8360-0-1	B	3	DATA BREAK INTERFACE
A-SP-KD8-E-1		3	ENGINEERING SPECIFICATIONS

REVISIONS			
REV.	DATE	CHG. NO.	APP'D.
A	3/23/71	00001	L.K.
B	4/71	M8360-1	L.K.
C	4/71	KD8E-2	L.K.

DRN. K. GULICK	DATE 1-15-7	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D K. GULICK	DATE 1-18-71	
ENG. [signature]	DATE 3/5/71	TITLE DATA BREAK
PROJ. ENG. [signature]	DATE 3/5/71	
PROD. [signature]	DATE 3/5/71	
FIRST USED ON PDP8-E		SIZE A / CODE ML / NUMBER KD8-E / REV. C
SCALE NONE		
SHEET 1 OF 1		DIST.

DEC FORM NO. 16-1033
DRA 103


DATA ADD Ø0
DATA ADD Ø1
DATA ADD Ø2
DATA ADD Ø3
DATA ADD Ø4
DATA ADD Ø5
DATA ADD Ø6
DATA ADD Ø7
DATA ADD Ø8
DATA ADD Ø9
DATA ADD 10
DATA ADD 11
TP4·(ACTIVE + MALC) L
MD ENABLE L
B INIT L
B BREAK L
BK RQST L
NBR L
OVERFLOW L
MACI H
3 CYCLE
GND
+3A
+5V
B BREAK L
ADD ACCEPTED L
BRK RQST L
DATA IN
INCREMENT INH
EXT DATA Ø0
EQUIPMENT CORPORATION
DATA BREAK INTERFACE
CS M8360-2-1
C



FIRST USED ON OPTION MODEL

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		

UNLESS OTHERWISE SPECIFIED

TOLERANCES

EQUIPMENT CORPORATION

TITLE

DATA BREAK INTERFACE

SCALE NONE

SHEET 3 OF 3

E CS M8360-C-1 REV. C

4.Ø Programming

A. Non-programmable.

5.Ø Interface Specifications

Refer to 1971 Small Computer Handbook.