digital

AD8-A

Engineering Drawings

Digital Equipment Corporation

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

DRAWING DIRECTORY

CUSTOMER PRINT SET INDEX

THIS IS PRINT SET [X]

	SEQUENCE
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UNIT VARIATIONS

VAR	TITLE	PRINT SET AD8-A
AD8-A	1Ø BIT ANALOG SUBSYSTEM	

REVISIONS	DATE	CHG. NO.	REV
	8-75	AD8-A-5	A

USED ON OPTION/MODEL		DRN.	DATE	TITLE
		D.K.CRABBE	12/10/74	1Ø BIT ANALOG SUBSYSTEM
		CHK'D.	DATE	
		[illegible]	12-13-74	
		PROJ ENG.	DATE	
		[illegible]	1-17-75	
		PROD.	DATE	SIZE B · CODE DD · NUMBER AD8-A · REV A
		[illegible]	4-22-75	
		FIELD SERV.	DATE	DIST
SHEET 1 OF 2		[illegible]	4/18/75	

DEC 16-13251-1062-1A-R972

DRB 106

CUSTOMER PRINT SET AD8-A				MFG. SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
						ELECTRICAL				
X					1	B-DD-AD8-A	#	2	DRAWING DIRECTORY	
X						A-PL-AD8-A-Ø	#	1	1Ø BIT ANALOG SUBSYSTEM	
X						C-OC-AD8-A-1	#	1	CONFIGURATION DRAWING	
X						A-SP-AD8-A-2	#	13	ENGINEERING SPECIFICATION	
X						A-SP-AD8-A-3	#	8	TROUBLESHOOTING	
X						A-SP-AD8-A-4	#	11	CIRCUIT DESCRIPTION	
X						A-SP-AD8-A-5	#	10	INSTALLATION/ACCEPTANCE	
X						D-CS-AØØ8-Ø-1	#	1	1Ø BIT A/D, AD8-A	
X						A-PL-AD8-A-6	#	1	SHIPPING LIST	
X						A-PL-AD8- B-Ø	#	1	SHIPPING KIT LIST	
X						B-IA7011017-0-0	#	1	CONNECTER CABLE	
X						D-UA-BC11L-ØØ	#	1	CABLE, BC11L	
X						D-IA-7010872-0-0	#	1	EXT. CLK. START CABLE	
				X		A-SP-A008-0-3	#	15	A008 TEST PROCEDURE	

CUSTOMER PRINT SET				MFG. SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE

CUSTOMER PRINT SET CODES	X = PRINT OF DOCUMENT INCLUDED IN PRINT SET C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED	TITLE: 1Ø BIT ANALOG SUBSYSTEM	SHEET 2 OF 2	SIZE: B	CODE: DD	NUMBER: AD8-A	REV: A

DRB 108

DEC 16-(325)-1062-2B-R972

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

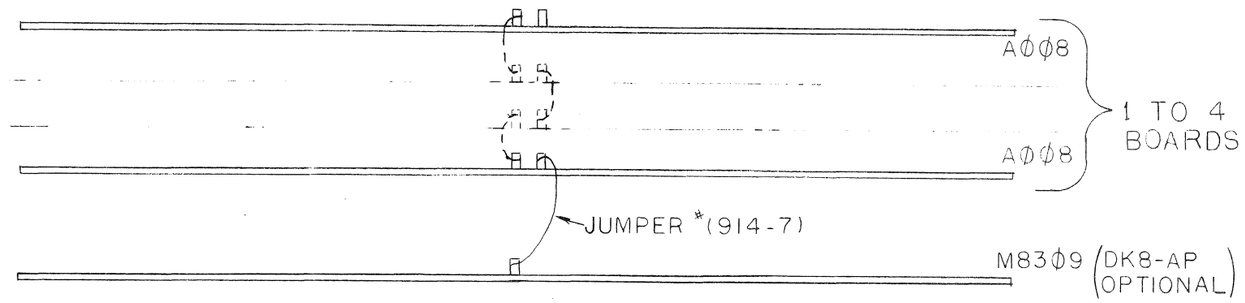
MADE BY D. K. CRABBE	CHECKED D K Crabbe	SECTION
DATE 12/10/74	DATE 12-13-74	1
ENG [illegible]	PROD [illegible]	ISSUED SECT.
DATE 1-3-75	DATE 1-3-75	1

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION AD8-A
1	17-00021-02	SHIELD	2
2	1210918-15	SHELL, BERG	1
3	1210089-6	PIN, BERG	50
4	1211166	STRAIN RELIEF	1
5	7Ø11Ø17-Ø-Ø	FASTON JUMPER	1
6	AØØ8	1Ø BIT A/D, AD8-A	1

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
1Ø BIT ANALOG SUBSYSTEM	//	A	PL	AD8-A-Ø		
	SHEET 1 OF 1	DIST.				

DEC FORM DEC 16-(325)-1031-N870
DRA 110

NOTES:
1. CUSTOMER INSTALLED SHIELDS ON BOTH SIDES OF EACH AØØ8 P.C. BOARD.



FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
AD8-A		PARTS LIST		

DIMENSIONAL TOLERANCE
DIMENSIONS ARE ~~MILLIMETERS~~ / INCHES
UNLESS OTHERWISE SPECIFIED

MILLIMETERS	INCHES	ANGLES
X,XX = ±0,10 X,X = ±0,5 X = ±2,	.XXX = ±.005 .XX = ±.02 .X = ±.1	±0° 30'

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL SEE: A-PL-AD8-A-Ø

FINISH //

		DATE
DRN.	J. Bissol	10DEC74
CHK'D.	[illegible]	12-13-74
ENG.	[illegible]	4-3-75
PROJ. ENG.	[illegible]	4-3-75
PROD.	[illegible]	4-15-75

NEXT HIGHER ASSY. B-DD-AD8-A

SCALE NONE

SHEET 1 OF 1

digital

TITLE 10 BIT ANALOG SUBSYSTEM

SIZE	CODE	NUMBER	REV.
C	AR	AD8-A-1	

DIST.

REVISIONS

REV.	CHANGE NO.	CHK

DEC FORM NO. DRC 100-B

SIZE C CODE AR NUMBER AD8-A-1 REV.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION DATE 9/16/74

TITLE AD8-A Engineering Specification

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

ENG	APPD	SIZE	CODE	NUMBER	REV
Leo. Sirois 7-4-75	Buss Iknajian	A	SP	AD8-A-2	

DEC 16-(392)-1079-N971
DRA 107

Sh. 1 of 13

ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE AD8-A Engineering Specification

1.0 INTRODUCTION

1.1 DESCRIPTION

The AD8-A (A008 module) is a 5 volt FSR, 10-bit A/D Converter having 16 channels of input multiplexing with sample-and-hold for use on the PDP-8 Omnibus family of processors. The device code is selected by PC switches on the module allowing the use of multiple A/D's per system.

1.2 FEATURES

A. Arbitrary device code selection.

B. Self-contained analog power supply operating from +5V DC logic power.

C. Double buffered data output for maximum throughput rate.

D. Programmed unipolar/bipolar operation.

E. Program enabled auto increment of the multiplexer register.

F. AD8-E compatible instruction set

G. Conversions may be initiated by program command, from the DK8-AP real time clock, or from an external source.

H. Compatible with H322 distribution panel.

2.0 GENERAL SPECIFICATIONS (@ 25°C unless otherwise specified)

2.1 INPUTS

Analog Input Impedance ($-5V \leq V_{in} \leq +5V$):

	SIZE	CODE	NUMBER	REV
	A	SP	AD8-A-2	

DEC FORM NO DEC 16—(381)—1022—N370
DRA 108

Unselected Channel = 1000 Megohm min.

Selected Channel = 10 Megohm min.

Analog Input Bias Current ($-5V \leq V_{in} \leq +5V$):

Unselected Channel = ±100 nA max.

Selected Channel = -2 μA max.

Analog Input Voltage (FSR):

Unipolar = 0V to +5V

Bipolar = -2.5V to +2.5V

External Start Input Current:

Low = -3.2 mA max. @ 0V input

High = +1.1 mA max. @ +5V input

External Start Logic Levels:

Low = 0V to +0.7V

High = +2V to +5V

Input Protection:

External Start: 47Ω fusible* resistor guaranteed to open @ 325 mA within 6.25 sec. (fig. 1). Guaranteed not to open from -3V to +8V input.

Analog Inputs: 1K fusible" resistors guaranteed to open @ 70 mA within 6.25 sec. (fig. 2). Guaranteed not to open from -15V to +15V input.

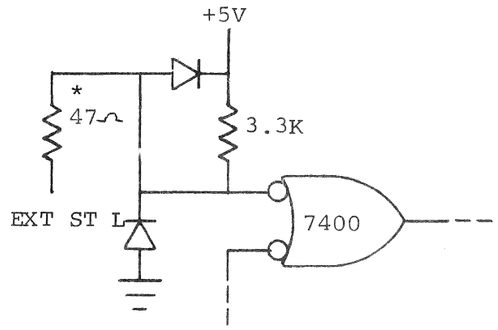


FIG. 1

EXTERNAL START INPUT CIRCUIT

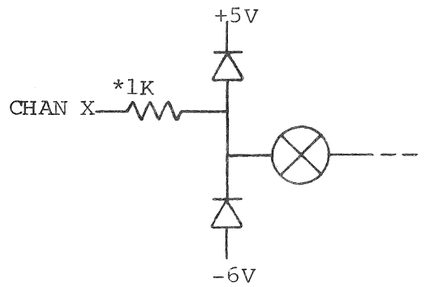


FIG. 2

TYPICAL ANALOG INPUT CIRCUIT

2.2 CODING

UNIPOLAR	
INPUT (V)	OCTAL CODE
+5 - 1 LSB	0777
+2.5	0000
0	7000**

BIPOLAR	
INPUT (V)	OCTAL CODE
+2.5 - 1 LSB	0777
0	0000
-2.5	7000**

** The three MSB's of the output data are tied together

2.3 PERFORMANCE

Accuracy: 0.1% of FSR (1 LSB)

Linearity: 0.05% of FSR (½ LSB)

Temperature Coefficients:

Gain = 50 ppm/°C max.

Linearity = 25 ppm/°C max.

Noise:

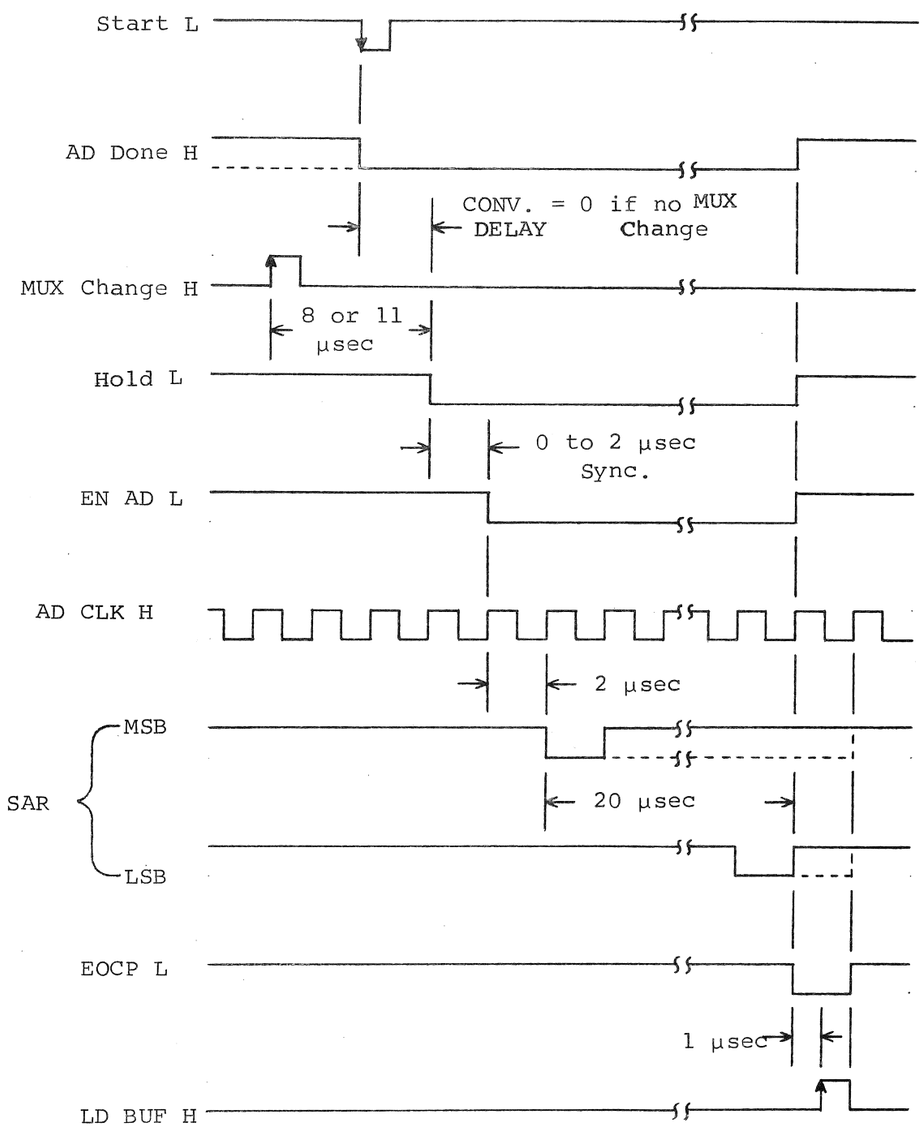
¼ LSB rms max.

1/15 LSB rms typical

Warmup Time = 5 minutes max.

FIGURE 3

TIMING DIAGRAM



2.4 TIMING (fig. 3)

Discrete (nominal):

A. MUX and S & H settling delay = 11 μsec from channel change (8 μsec by removing jumper W3 if channels are all unipolar or all bipolar)

B. Same channel re-acquisition = 4 μs

C. A/D Sync-up = 0-2 μsec (clock dependent)

D. Hold delay = 2 μsec (clock dependent)

E. Conversion = 20 μsec (clock dependent)

Start to A/D done (nominal):

Same Channel:

B + C + D + E = 26 to 28 μsec

Different Channels:

Mixed Unipolar & Bipolar (W3 in)

A_1 + C + D + E = 22 to 35 μsec
(A_1 = 0 to 11μsec)

All Unipolar or Bipolar (W3 out)

A_2 + C + D + E = 22 to 32 μsec
(A2 = 0 to 8 μsec)

Clock Dependent Times:

Accuracy = ±6% with supply @ +5V

±8% with supply from +4.75 to +5.25

Temperature Coefficient = 650 ppm/°C max. @ constant supply voltage

2.5 POWER REQUIREMENTS

+5V DC ±5% @ 3.25 A max.

2.6 ENVIRONMENTAL SPECIFICATIONS (ref. DEC STD. 102, Class C)

Operating Environment:

Temp. range = 5°C to 50°C system amb.
= 5°C to 70°C module amb.
Humidity = 10% to 90%

Storage Environment:

Temp. range = -40°C to +66°C

Humidity = 95% max.

2.7 PACKAGING

The AD8-A is a single A008 quad size module which mounts on to a PDP-8 Omnibus. Included with this option are two RFI shields which should be mounted one on each side of the A008 module. For improved performance it is recommended that at least one slot adjacent to each side of the A008 be left empty, or that the A008 be the last module on the bus assembly with the adjacent slot left empty.

One Berg connector (J1) provides access to the analog inputs. Table 1 shows the pin assignments for J1. Two tabs on the A008 (which are disabled when not connected) provide the input start signal from the DK8-AP.

TABLE 1

CONNECTOR J1

PIN	SIGNAL
K, M, W, Y, AA, CC EE, HH, KK, MM	ANALOG GND
L	CHAN 17
N	CHAN 16
P, S	LOGIC GND
R	CHAN 15
T	CHAN 14
U	EXT ST L
V	CHAN 13
X	CHAN 12
Z	CHAN 11
BB	CHAN 1Ø
DD	CHAN Ø7
FF	CHAN Ø6
JJ	CHAN Ø5
LL	CHAN Ø4
NN	CHAN Ø3
PP	-13V (for test only)
RR	CHAN Ø2
SS	+13V (for test only)
TT	CHAN Ø1
UU	+5V HQ @ 20 mA
VV	CHAN ØØ

3.0 A/D SPECIFICATIONS

Resolution: 10 bits (1 part in 1024)

Differential Linearity:

Guaranteed: No skipped states;
95% of states within $\pm\frac{1}{2}$ LSB.

Typical: 99% of states within $\pm\frac{1}{2}$ LSB.
85% of states within $\pm\frac{1}{4}$ LSB.

4.0 SAMPLE-AND-HOLD SPECIFICATIONS

Tracking:

Small signal bandwidth = 700 KHZ typical

Slew rate = 1V/μsec typical

Aperture:

Delay = 200 nsec max.

Jitter = 1 nsec max.

5.0 MULTIPLEXER SPECIFICATIONS

Switching: break-before-make

Channels: 16 non-expandable single-ended inputs

Crosstalk:

-80 db @ 1 KHZ

-20 db/decade roll-off

6.0 REGISTERS

Ø	1	2	3	4	5	6	7	8	9	1Ø	11
A/D DONE	TMG ERR	DONE INT EN	ERR INT EN	EXT ST EN	INC EN	UNI-POLAR	TEST BIT	MSB			LSB

Status REG. — Enable Register — Multiplexer Register

6.1 Status Register (AC bits Ø & 1)

A/D DONE (Bit Ø) is set = 1 when a conversion is completed. The buffer is updated 1 μsec later.

TMG ERR (Bit 1) is set = 1 when a start conversion is attempted while a conversion is in progress, or when the buffer is updated while a read buffer command (ADRD) is in process.

6.2 Enable Register (AC bits 2 thru 7)

DONE INT EN (bit 2) when set = 1 from the AC will enable the INT RQST line to interrupt when A/D DONE is set.

ERR INT EN (Bit 3) when set = 1 from the AC will enable the INT RQST line to interrupt when TMG ERR is set.

EXT ST EN (Bit 4) when set = 1 from the AC will enable the external A/D start conversion circuit to initiate conversions from the DK8-AP or an external source.

INC EN (Bit 5) when set = 1 from the AC will auto increment the MUX REGISTER to the next sequential channel at the end of each conversion. The MUX REGISTER will overflow to ØØ from 17.

UNIPOLAR (Bit 6) when set = 0 from the AC the A/D will be in bipolar mode. When set = 1 the A/D will be in unipolar mode.

6.3 MULTIPLEXER REGISTER (AC bits 8 thru 11)

The multiplexer register is loaded from the AC and indicates the current channel being monitored by the AD8-A. One of 16 channels is selected by loading the channel number (ØØ - 17 octal) into this register.

NOTE: All AD8-A registers are cleared by a processor generated INITIALIZE.

7.0 PROGRAMMING

Eight instructions are used to program the AD8-A. The device code (XY) is preset by the user using switches provided on the AD8-A (A008 module).

CLEAR ALL (ADCL) - 6XYØ

Clear STATUS, ENABLE, and MUX registers.

LOAD MUX REGISTER (ADLM) - 6XY1

Load MUX REGISTER from the AC, then clear the AC.

START CONVERSION (ADST) - 6XY2

Clear A/D DONE and ERROR flags (STATUS REGISTER), then initiate a conversion on the current channel.

READ A/D BUFFER (ADRB) - 6XY3

Transfer the contents of the A/D BUFFER into the AC (bits Ø thru 2 are the MSB), and clear the A/D DONE flag.

SKIP ON A/D DONE (ADSK) - 6XY4

Skip the next instruction if the A/D DONE flag = 1.

SKIP ON TIMING ERROR (ADSE) - 6XY5

Skip the next instruction if the TMG ERR flag = 1.

LOAD ENABLE REGISTER (ADLE) - 6XY6

Load the ENABLE REGISTER from the AC, then clear the AC.

READ REGISTERS (ADRS) - 6XY7

Transfer the STATUS, ENABLE, and MUX registers into the AC.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 4/15/75

TITLE AD8-A TROUBLESHOOTING PROCEDURE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

ENG	APPD	SIZE	CODE	NUMBER	REV
Geo. F. Chase 4-16-75	Russ Ahrens 4-16-75	A	SP	AD8-A-3	

DEC 16-(392)-1079A-R873
DRA 107A

SHEET 1 OF 8

1.0 SCOPE

This document covers troublshooting procedures for the AD8-A one-module analog sub-system. The AD8-A consists of a 16-channel 10-bit A/D converter with sample-and-hold. Since the AD8-A is a PDP8 Omnibus option, it also contains an Omnibus interface. Because the AD8-A draws power only from the +5V processor power supply, it also contains a dc-to-dc converter to supply power for the analog circuitry.

2.0 RELATED DOCUMENTS

The following material should be referenced when using this document:

2.1 AD8-A User's Guide EK-AD8A-TM-ØØ1

2.2 AØØ8 (AD8-A) Circuit Schematics D-CS-AØØ8-Ø-1

2.3 AD8-A Installation/Acceptance Procedure A-SP-AD8-A-4

2.4 AD8-A Circuit Description A-SP-AD8-A-5

2.5 AD8-A Diagnostics

2.5.1 Logic Test MAINDEC-Ø8-DJADA-A

2.5.2 Analog Test Auto. Cat.-Ø8-QJADA-A

3.0 MAINTENANCE

The AD8-A logic is to be repaired in the normal manner. The AD8-A analog circuitry is to be repaired only in the AD8-A option area. If any analog failures occur either in system integration (FA & T) or in the field, the AD8-A is to be board-swapped and returned to the option area for repair. Likewise, no analog adjustments are to be attempted

in FA & T or in the field. All potentiometers are sealed after final adjustment in the option area, and from then on are considered to be fixed resistors. All AD8-A's have been burned in to assure the reliability necessary for successful implementation of this board-swap maintenance philosophy.

It is the intent of this procedure and of the AD8-A diagnostics to provide the tools necessary to troubleshoot and repair all digital logic problems, to verify analog performance, and, if A/D problems are detected, to isolate the problem to either the digital or analog circuitry so that a decision can be made whether to repair the board (digital problem) or to board-swap and return it to the option area (analog problem). Field (and FA & T) repairs may be made on the dc-to-dc converter (analog power supply).

4.0 DIAGNOSTICS

4.1 Logic Diagnostic MAINDEC-Ø8-DJADA-A

The tests starting at address Ø2ØØ do a complete checkout of all AD8-A logic - Omnibus interface, registers and A/D logic. These tests are set up to automatically test multiple AD8-A's provided that the device codes are in sequence. When originally loaded the tests are for device code 55. To run multiple AD8-A's set address Ø143 to the device code of the first A/D and set address Ø144 to the last A/D code. The diagnostic will print errors that occur and the device code

of the failing AD8-A.

The routine starting at address Ø2Ø1 is a troubleshooting aid. This routine allows switch register selected IOT's to be executed.

The routine starting at address Ø2Ø2 displays continuous A/D conversions in the processor AC. It is used to calibrate the AD8-A using a dc voltage standard and verifying the AD8-A calibration.

If a DK8-E real time programmable clock is to be used to start conversions on the AD8-A then the routine starting at address Ø2Ø3 should be used.

The monotonicity test starting at address Ø2Ø4 uses a ramp input to the A/D. However, if all other factors are ignored, to pass this test, the A/D must have a differential linearity of better than ±1 LSB. For this test to be valid, the A/D must be noiseless. Noise spikes could give false differential linearity readings that would indicate some states are zero in width. Since this routine looks for sequential codes generated by the ramp input any noise spike greater than one state width would generate a code one or more counts different than the code expected.

The successive reads test starting at Ø2Ø6 checks the A/D buffer for noise by reading the buffer twice after each conversion and comparing for equality.

4.2 Analog Diagnostic AUTO.CAT-Ø8-QJADA-A

This diagnostic tests the AD8-A in conjunction with the VC8-E and a G5Ø36 wraparound module. The two D/A converters on the VC8-E are combined in various manners using resistive dividers on the G5Ø36 module and sent to the AD8-A analog inputs. Because the D/A's are divided down before going into the A/D, test resolution far better than 1 LSB is attained. In

addition, the analog power supply levels are divided down and used as inputs, allowing test of the dc-to-dc converter. the INTENSIFY output of the VC8-E is fed into the A/D external start input, thus allowing testing of both program and external starts. Use of the various A/D channels by the wraparound test is as follows:

CH ØØ: Switchable between ground (Ø) and split lug (E) for external inputs (EDC).

CH Ø1: Ground through a 100 K ohm resistor, used for bias current test.

CH Ø2: +5 V HQ power, divided down to +1 volt nominal.

CH Ø3: Positive analog supply, divided down by 50:9.

CH Ø4: Negative analog supply, divided down by 50:9.

CH Ø5: Coarse X and fine Y, Voltage ½X +(1/100)Y, Code X +(1/50)Y.

CH Ø6: Coarse Y and fine X, Voltage ½Y +(1/100)X, Code Y +(1/50)X.

CH Ø7: Fine Y, Voltage (1/100)Y, Code (1/50)Y.

CH 1Ø: Fine X, Voltage (1/100)X, Code (1/50)X.

CH 11: Direct X.

CH 12: Direct Y.

CH 13: ERASE L to +5V pull-up.

CH 14: WRITE-THRU L to +5V pull-up.

CH 15: NON-STORE L to +5V pull-up.

CH 16: CHANNEL Ø2 L to +5V pull-up.

CH 17: +5V HQ power, divided down to +4 volts nominal.

The diagnostic tests only one AD8-A at a time and only for a device code of 55.

5.0 TEST POINTS

The following test points are available on the AD8-A for trouble-shooting purposes:

TP-A: Chopper output of the dc-to-dc converter, switching between ground and +5V with a 32 µsec period.

TP-B: +13V analog power.

TP-C: H.Q. analog ground.

TP-D: -13V analog power.

TP-E: AD CLK H; a 500 KHZ TTL timing signal.

TP-F: MUX NODE; output of the analog multiplexers.

TP-H: DAC and S & H summing node.

TP-J: Sample-and-hold output.

TP-K: EN AD (1) L; TTL signal useful for external scope trigger to synchronize scope to conversions.

6.0 HINTS

6.1 HQ Power Supply

If the ±13V supplies are not up to at least 12.5 volts check the following in sequence:

1) Chopper output. If this signal is correct proceed to no. 2; if not check for a clock input and follow

the signals through.

2) Each grounded capacitor in the doubler circuit should show about a 3V change per section in sequence.

3) If the ±13V supplies recover when the output inductors (L4 & L5) are "lifted" then the low voltage is probably caused by an overload external to the supply.

6.2 A/D Logic

When the ALL "1"s jumper (W1) is in, the converted value should be Ø777. With the ALL "Ø"s jumper (W2) in, the converted value should be 7ØØØ. If these results are obtained and a problem exists, then the fault is in the analog circuitry. If these results are not obtained, there is a problem in the A/D logic. There may also be a fault in the analog circuitry.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 3/31/75

TITLE AD8-A CIRCUIT DESCRIPTION

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

ENG	APPD	SIZE	CODE	NUMBER	REV
Ted F. Elbert 9-15-75	Russ Strazzo 4-15-75	A	SP	AD8-A-4	

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DRA 107A

1.0 INTRODUCTION

1.1 The AD8-A is a one-module analog subsystem that interfaces with the PDP-8 Omnibus computers. Included on the AD8-A module are the following:

1.1.1 Bus control, with switch-selectable device code.

1.1.2 A/D Converter, with 16-channel multiplexer and sample-and-hold.

1.1.3 Analog power supply.

1.2 The following material should be referenced when using this document:

1.2.1 AØØ8 (AD8-A) circuit schematics D-CS-AØØ8-Ø-1.

1.2.2 AD8-A User's Guide EK-AD8A-TM-ØØ1.

1.2.3 PDP8 Small Computer Handbook.

1.2.4 AD8-A Engineering Specification A-SP-AD8-A-2.

1.3 Reading AØØ8 Prints

Appearing in the TITLE block of each sheet is an "A" designation in parentheses. This designation is used as a prefix to signals originating on that sheet and appearing on other sheets for cross-referencing purposes.

Example:

A3 MUX Ø8 (1) H appears on sheet 8. (A3) appears in the TITLE block of sheet 5.
Therefore, A3 MUX Ø8 (1) H is generated on sheet 5.

2.0 BUS CONTROL

The AD8-A Bus Control consists of the DECODER (sheet 4), DATA INTERFACE (sheet 5), and the FLAGS (sheet 6).

2.1 Decoder (Figure 1)

When the Omnibus lines MDØ3 through MDØ8 compare with the S1 settings the outputs of the digital comparator (E1 & E9) go high. Since the comparator outputs are open-collector and wired together, a high will not appear until all outputs should be high. The I/O PAUSE signal then completes the device selection on the comparator which strobes the IOT decoder (E17) thus decoding the Omnibus MDØ9 through MD11 signals into one of eight separate commands, and providing the INTERNAL I/O Signal to the Omnibus. The Omnibus C lines are controlled by one of four IOT commands, depending upon which is currently decoded. The action of each of the four instructions is as follows:

	CØ	C1	
ADLM	L	H	Transfer AC to MUX Register and clear AC.
ADRB	L	L	Transfer A/D Buffer to AC.
ADLE	L	H	Transfer AC to ENABLE Register and clear AC.
ADRS	L	L	Transfer A/D STATUS Register to AC.

The remaining logic establishes the clearing functions for the FLAGS and Registers and ANDS the programmed start command (ADST) to coincide with TP3.

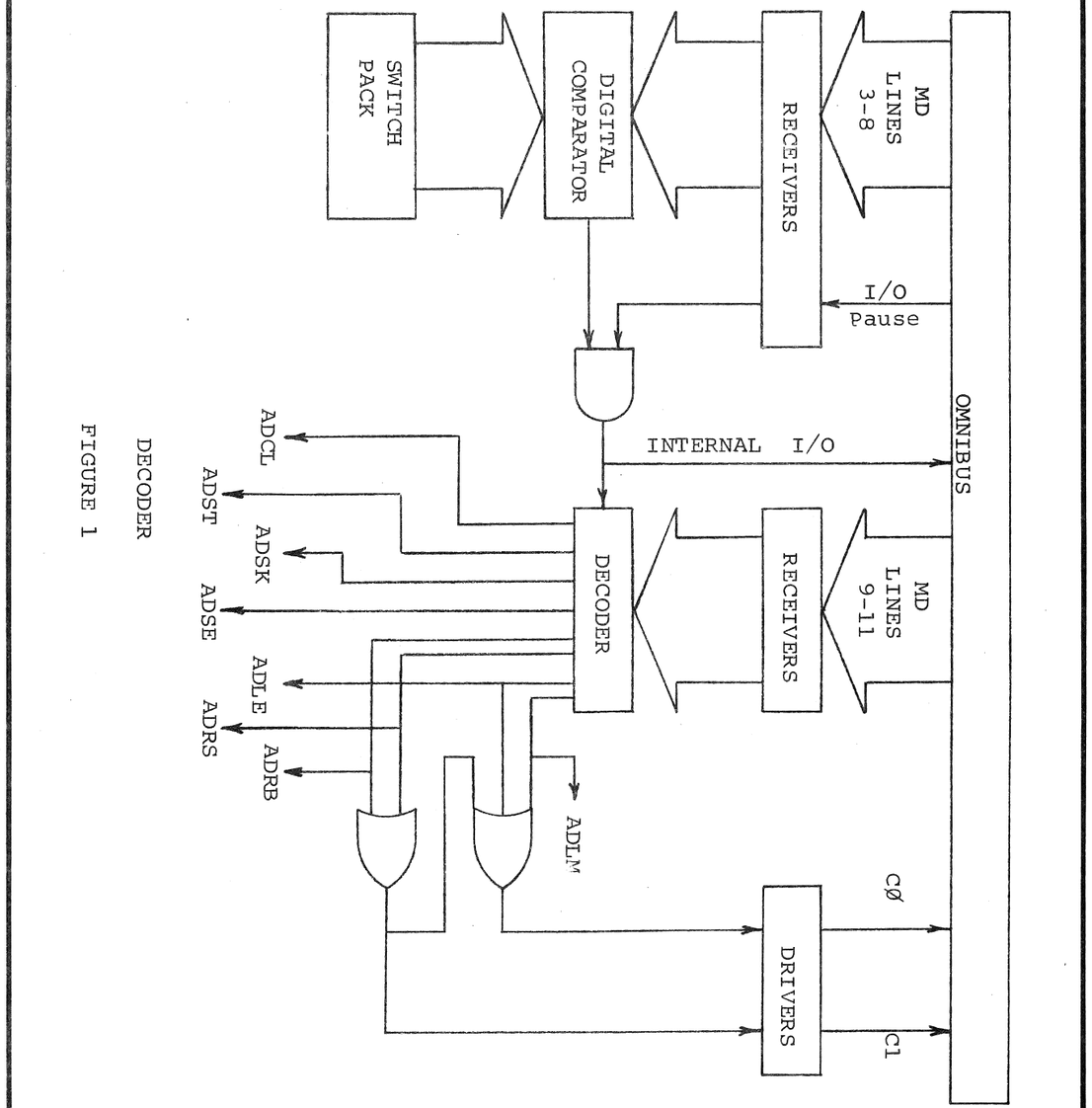


FIGURE 1 DECODER

2.2 Data Interface (Figure 2)

The DATA INTERFACE consists of a digital multiplexer (E6, E26 and E34) which sends the A/D STATUS Register onto the Omnibus DATA lines during ADRS or the A/D Buffer contents during ADRB. The data receivers, E25, read the Omnibus DATA lines into the ENABLE register (E27) during ADLE. The remaining data receivers, E43, read the DATA lines into the MUX register (E36) during ADLM, thus selecting the A/D current channel. If the INC EN bit of the ENABLE register is set then the MUX register will be automatically incremented to the next sequential channel at the completion of each A/D conversion.

2.3 Flags

There are two flags:

TMG ERR (E14 upper)
A/D DONE (E14 lower)

2.3.1 TMG ERR

There are two conditions which set the timing error flag. If an ADRB (read A/D buffer) is being done and the buffer is updated during the read then the flag is set to signal that the data has changed while it was being read. If a start conversion is attempted while a conversion cycle is in progress, then the flag will be set.

2.3.2 A/D DONE

This flag is set when an A/D conversion has been completed

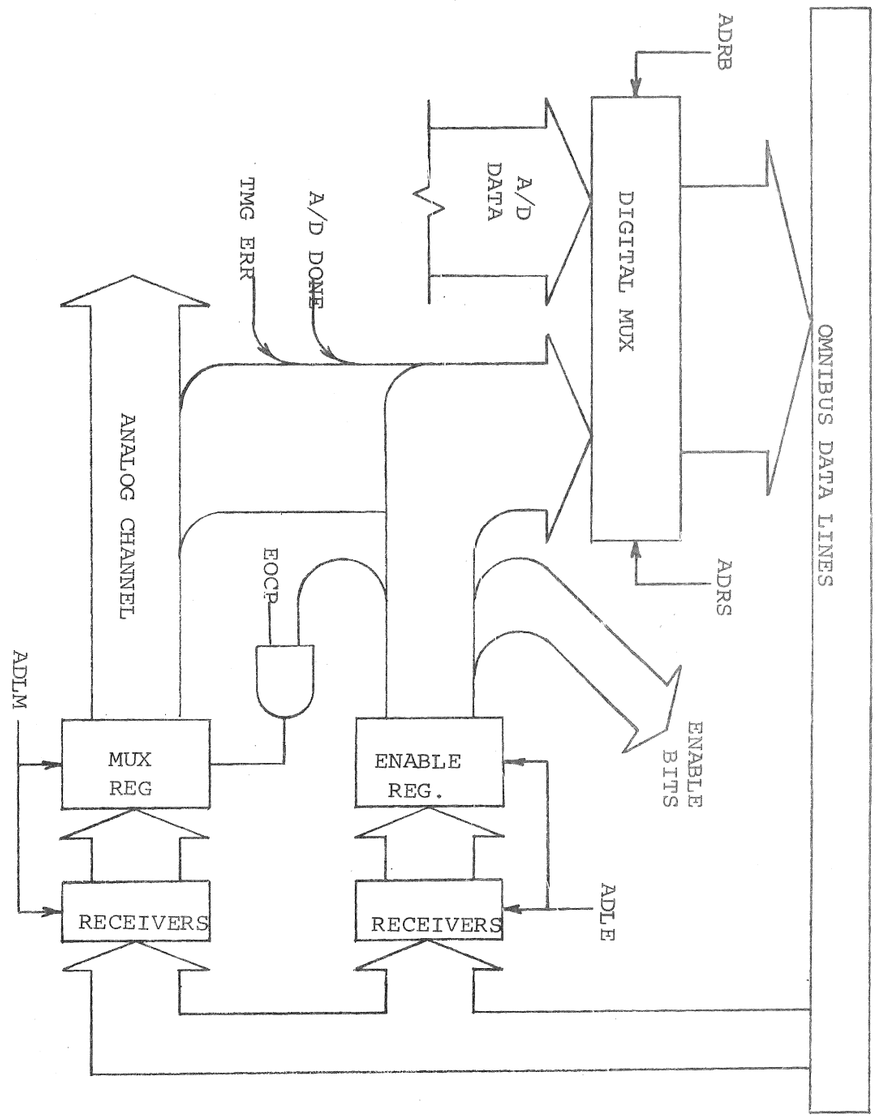


FIGURE 2 DATA INTERFACE

and is cleared at the start of a new conversion. Both the ERR and DONE flags may be sent to the Omnibus SKIP and INT RQST lines by setting the proper bit in the ENABLE register.

2.3.3 OTHER LOGIC

When the MUX register is changed, either by program update or by auto increment, an 8 (W3 out) or 11 μsec (W3 in) delay is triggered that will delay any start conversion until the time-out is completed. The AD8-A is shipped with W3 installed.

3.0 HQ POWER SUPPLY (SHEET 7)

The AD8-A requires only +5V DC logic power from an external source (the processor). A series of voltage doublers are connected in cascade and operated from a power chopper (Q40 and Q41) to derive the higher voltages required by the analog section. A typical doubler section of the positive supply is shown in figure 3. When the chopper is at ground the first capacitor charges from the previous section. The chopper then switches to +5 V causing node A to go more positive thus reverse biasing the input diode and forward biasing the second diode and dumping additional charge onto the output capacitor. The negative supply operates in a similar fashion. Timing for the A/D and power supply is derived from the clock output (Q38) and counter (E4). See Figure 4.

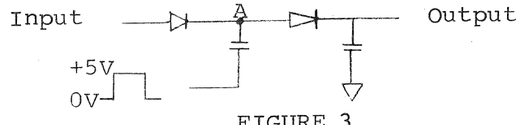


FIGURE 3

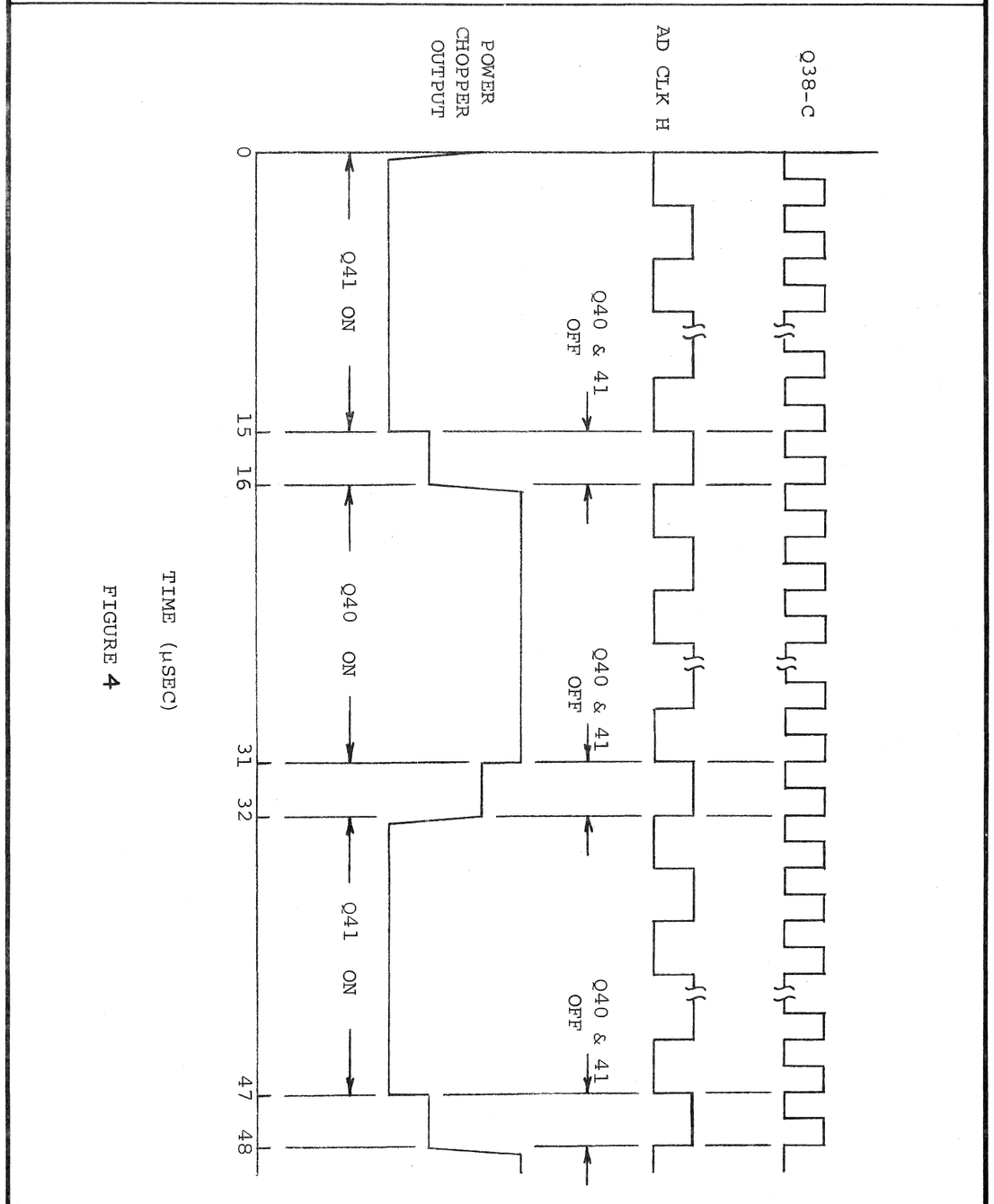


FIGURE 4

4.0 ANALOG SECTION (Figure 5)

The AD8-A analog section consists of the MULTIPLEXER (sheet 8), A/D CONVERTER (sheet 9), and BUFFER (sheet 10).

4.1 Multiplexer

The multiplexers (E37 and E39) are protected by series fusible resistors and diode clamps (E38 and E40) on each channel input. The MSB of the MUX register selects the multiplexer I.C. and the remaining bits select the input within the particular chip. During conversions the multiplexer I.C.'s are disabled (off) and the output of each is shorted to ground by Q42.

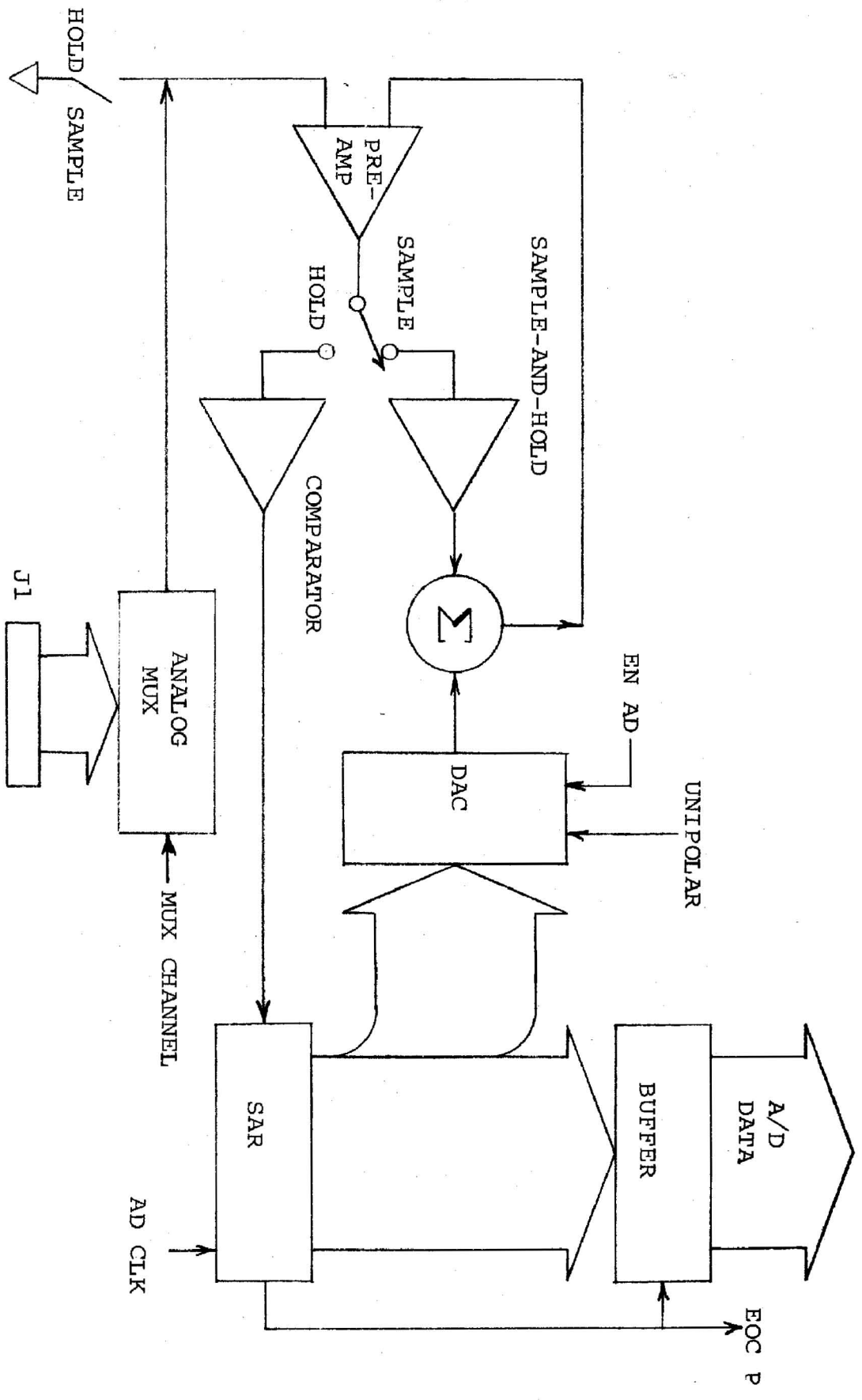
4.2 A/D Converter

This circuit consists of an 8 bit D/A converter (E42) with two external bits added (Q24 and Q26) to form a 10 bit D/A. Pots R82 and R83 provide for the calibration of the added bits. Since the HQ power supply is apt to be noisy, due to the chopper, power for this section is supplied through current sources (Q1 through Q11). The pot acts as a gain control for the output of the 8 bit D/A converter. Q33 and Q34 constitute the sample-and-hold. In bipolar mode the MSB of the D/A is on during sample thus offsetting the sample-and-hold exactly the value of the MSB. The drain of Q36 is the comparator output with R84 provided as the comparator offset control. The intermediate amplifier stages between the MUX NODE and the comparator, and the MUX NODE and the sample-and-hold

serve as the preamps of the sample-and-hold during sample between conversions and as preamps to the comparator during hold while a conversion is in progress.

4.3 Buffer

The SAR I.C. is tied to the D/A bits. During conversion the SAR interogates each bit in sequence starting with the MSB, for 2 μsecs. The D/A output is compared to the sample-and-hold output and the decision to hold or reject the SAR bit is clocked into the SAR at the end of each 2 μsec period from the comparator. At the end of the conversion the EOCP from the SAR sets the A/D DONE Flag and the resulting data in the SAR is the transferred to the buffer registers (E21 and E29) 1 μsec later.



ANALOG SECTION

FIGURE 5

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 3/28/75

TITLE AD8-A INSTALLATION/ACCEPTANCE PROCEDURE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	ECO CHANGE	AD8-A-00005	G. SIROIS	8-20-75	Geo Sirois	9/19/75

ENG	APPD	SIZE	CODE	NUMBER	REV
George Sirois 7-14-75	Russ Ohrazian 4-14-75	A	SP	AD8-A-5	A

DEC 16-(392)-1079A-R873
DRA 107A

SHEET 1 OF 10

ENGINEERING SPECIFICATION digital CONTINUATION SHEET

TITLE AD8-A INSTALLATION/ACCEPTANCE PROCEDURE

1.0 SCOPE

This procedure covers the installation and acceptance of an AD8-A in a PDP8 Omnibus system. It is anticipated that this procedure will be used in one of the following situations:

1.1 Installation and acceptance of an AD8-A on a PDP8 Omnibus system in an in-house FA & T system integration area.

1.2 Add-on installation and acceptance of an AD8-A on an existing PDP8 Omnibus system in the field.

1.3 Acceptance of an AD8-A on a new PDP8 Omnibus system upon installation at a customer site.

1.4 On-going AD8-A verification testing at intervals over the life of a given system.

2.0 MOUNTING AND CONFIGURATION

2.1 The AD8-A is a one-module analog option which interfaces directly to any PDP8 Omnibus processor.

2.2 The AD8-A may be mounted in any Omnibus slot and will operate within specifications with no configuration restrictions whatsoever regarding physical proximity to the processor, memory, or other options. AD8-A analog performance may be further optimized by mounting it in an electrically quiet environment. Consequently, if a choice is available in configuring a particular system, the AD8-A should be mounted

SIZE	CODE	NUMBER	REV
A	SP	AD8-A-5	A

DEC FORM NO DEC 16—(381)—1022—N370
DRA 108

away from the processor and memory modules.

2.3 Cabling

The AD8-A is interfaced to the outside world by means of a single forty pin Berg connector through a BCØ8-R flat cable to an H322 distribution panel, a BC11-L Berg-to-open end cable, or a user built cable.

2.4 Device Code

The AD8-A device code is selected by means of a PC switch-pack (S1) mounted on the AØØ8 module. Care must be taken not to assign the device code of any other option in a particular system and to avoid using special codes such as ØØ which is used for internal IOT microinstructions. An OPEN, or OFF, switch will decode a "1", and a CLOSED, or ON, switch will decode a "Ø". Switches S1-1 and S1-2 are unused. Switch S1-3 is the MSB of the device code, and S1-8 is the LSB.

3.0 INSTALLATION

3.1 Based on the above considerations, choose an Omnibus slot and device code.

3.2 Remove the switch_pack (S1) cover and set the device code switches.

3.3 Re-install the switch-pack (S1) cover and insert the AØØ8 module into the selected Omnibus slot.

3.4 Install the 17-00021-02 RFI shields on both sides of the AD8-A.

3.5 Conduct an acceptance test per section 4.0.

4.0 AD8-A ACCEPTANCE

4.1 AD8-A acceptance testing flow is shown in figure 1. Since the wraparound cable is special and a VC8-E may not be present at a user sight, test 4.3 is intended for in-house use only.

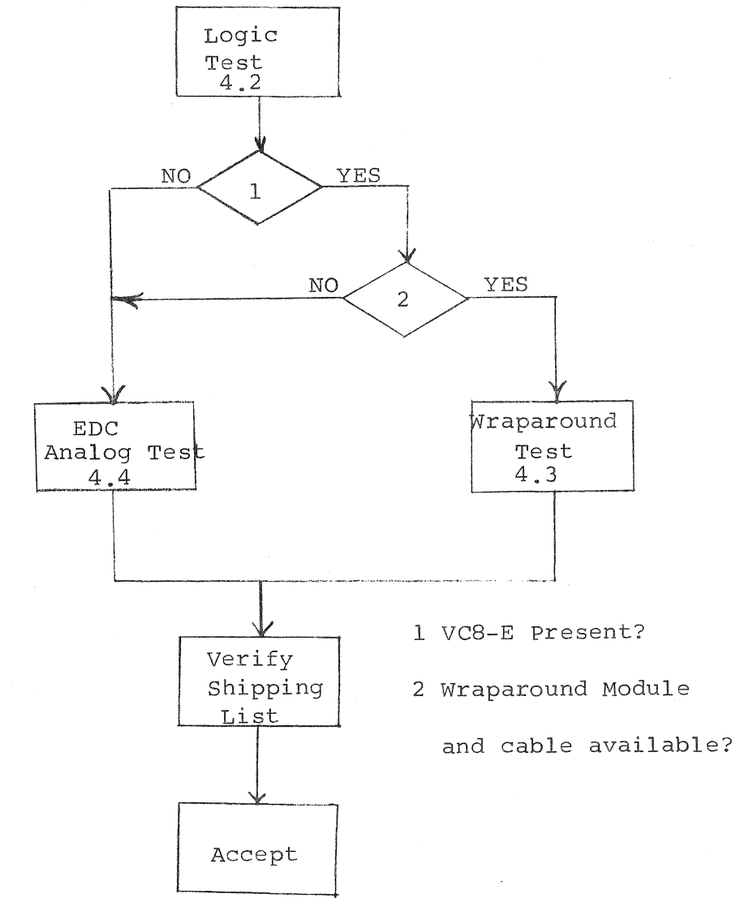


FIGURE 1 AD8-A ACCEPTANCE FLOW

4.2 Logic Test

4.2.1 Equipment

1 AD8-A
1 PDP8 Omnibus Processor (4K)
1 MV116 EDC or equivalent
1 BC11L cable (915 termi-point jumpers may be used by Field Service if care is taken not to short to etch under J1.)

4.2.2 Software

MAINDEC-Ø8-DJADA-A Diagnostic and listing

4.2.3 Load MAINDEC-Ø8-DJADA-A

4.2.4 Load the device code of the first AD8-A in address Ø143.

Example: If first device code = 53
Set SR = Ø143
Load address
Set SR = Ø53Ø
Deposit

4.2.5 Load the device code of the last AD8-A in address Ø144.

Example: If last device code = 55
Set SR = Ø144
Load address
Set SR = Ø55Ø
Deposit

4.2.6 Run the tests starting at address Ø2ØØ. Three passes per AD8-A, without error, are required. "An 113Ø failure will sometimes occur, this is normal due to the fact that the program timing is asynchronous to the A/D timing. It is sufficient to have only one pass."

4.2.7 If a DK8-E clock module is present, connect the 7010872 cable to the Berg connector on the clock module and the tab of the same cable to the tab on

the AD8-A. Interconnect all AD8-A's using the 7011017 cable. (DK must be C.S. rev F, or beyond, on M518).

4.2.8 Run the test starting at address Ø2Ø3. Three passes per AD8-A, without error, are required.

4.2.9 Connect a BC11L cable to J1 (Berg Connector) on the AD8-A.

4.2.10 Connect the EDC through the BC11L cable to the channel (s) to be tested. Ground all unused channels. The EDC must be "floating" to avoid ground loops.

4.2.11 Set addresses Ø143 and Ø144 to the device code of the AD8-A to be tested. Only one AD8-A can be checked at a time in the following calibration check.

4.2.12 Run the test starting at address Ø2Ø2 selecting the channel (s) connected to the EDC. The processor AC shall display the codes indicated in table 1 for the corresponding EDC voltages in bipolar mode.

4.2.13 Repeat sections 4.2.9 through 4.2.12 for each AD8-A in the system.

EDC (V)	AC CODE
-1.875	72ØØ ±1
0	ØØØØ ±1
+1.875	Ø6ØØ ±1

TABLE 1

greater than 1½ LSB shall be equal to, or less than, $63_{(8)}$ or $51_{(10)}$.

4.4 EDC Analog Test

4.4.1 Equipment

1 AD8-A
1 PDP8 Omnibus Processor (4K)
1 MV116 EDC or equivalent
1 BC11-L cable (915 termi-point jumpers may be used by Field Service if care is taken not to short to etch under J1)

4.4.2 Software

MAINDEC-Ø8-DJALA-A Diagnostic and listing

4.4.3 Load MAINDEC-Ø8-DJADA-A.

4.4.4 Set addresses Ø143 and Ø144 to the device code of the AD8-A to be tested. Only one AD8-A can be checked at a time in the following calibration and linearity check.

4.4.5 Connect a BC11L cable to J1 (Berg Connector) on the AD8-A.

4.4.6 Connect the EDC through the BC11L cable to the channel (s) to be tested.

The EDC must be "floating" to avoid ground loops.

4.4.7 Run the test starting at address Ø2Ø2 selecting the channel (s) connected to the EDC. The processor AC shall display the codes indicated in table 2 for the

4.3 Wraparound Test

4.3.1 Equipment

1 AD8-A
1 PDP8 Omnibus Processor (8K)
1 G5036 Wraparound Module
1 VC8-E Scope Control
1 7010923 Wraparound Cable

4.3.2 Software

AUTO. CAT.-Ø8-QJADA-A Diagnostic and listing

4.3.3 Load AUTO. CAT.-Ø8-QJADA-A

4.3.4 Set the device code of the AD8-A to be tested to 55.

4.3.5 Interconnect the G5Ø36, AØØ8 and VC8-E using the wrap-around cable.

4.3.6 Start the diagnostic. (G5Ø36 switch to "Ø")

4.3.7 The STATE-WIDTH printout gives the codes greater than, and less than 1½ and ½ LSB with their octal widths. An octal width of ØØØ1 is equivalent to 0.02 LSB. Therefore, 0.50 LSB = $31_{(8)}$, 1.00 LSB = $62_{(8)}$, 1.50 LSB equals $113_{(8)}$, and 2.00 LSB = $144_{(8)}$.

4.3.8 Following the STATE-WIDTH statement is a summation of states SKIPPED, GREATER THAN 2 LSB, LESS THAN ½ LSB, and GREATER THAN 1½ LSB. There shall be no SKIPPED states nor shall there be any states greater than 2 LSB. The sum of the states less than ½ LSB and those

4.4.8 With the EDC still connected, run each of the tests starting at the following address, one pass is required:

Ø2Ø5 per TABLE 4
Ø2Ø6
Ø2Ø7

4.4.9 Repeat sections 4.4.4 through 4.4.8 for each AD8-A present.

TABLE 4

TEMP A TEMP B DIFFERENCE	MAX. NUMBER ALLOWED
2 LSB	45/1000 conversions*
3 LSB	1/2000 conversions
>3 LSB	0

* 45(10)=55(8)

corresponding EDC voltages in bipolar mode.

TABLE 2

EDC (V)	AC CODE
-2.500	7ØØØ ±1
-1.875	72ØØ ±1
-1.250	74ØØ ±1
-0.625	76ØØ ±1
0.000	ØØØØ ±1
+0.625	Ø2ØØ ±1
+1.250	Ø4ØØ ±1
+1.875	Ø6ØØ ±1

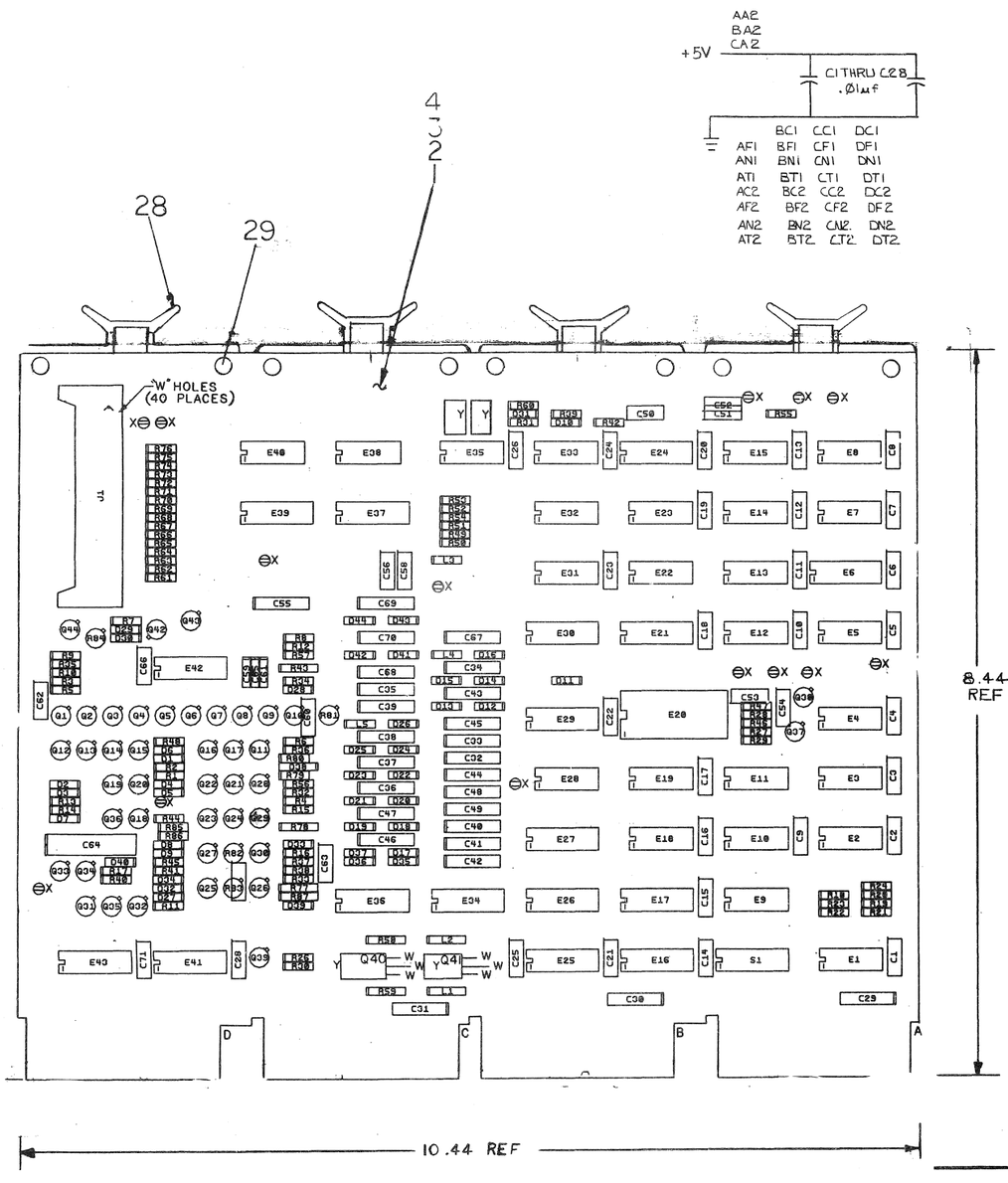
4.4.8 Run the test starting at address Ø2Ø2 again but with SW 6 = 1 (unipolar mode). The processor AC shall display the codes indicated in table 3.

TABLE 3

EDC (V)	AC CODE
0.000	7ØØØ ±1
+0.625	72ØØ ±1
+1.250	74ØØ ±1
+1.875	76ØØ ±1
+2.500	ØØØØ ±1
+3.125	Ø2ØØ ±1
+3.750	Ø4ØØ ±1
+4.375	Ø6ØØ ±1

NOTES:

1. W1 W2 AND W3 ARE OPTIONAL DO NOT INSERT.



REF				
REF		X-Y COORDINATE HOLE LOCATION	K-CO-A008-0-4	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-A008-0-5	2
REF		MODULE ECO HISTORY	B-MH-A008-0-6	3
1		ETCHED CIRCUIT BOARD	5011129	4
36	C1 THRU C28,C56 THRU C63	CAP, .01 UF 100V 20%	1001610-01	5
1	C64	CAP, .001 UF 100V 10%	1009939	6
20	C29 THRU C43,C55,C67 THRU C70	CAP, 15 UF 20V 10%	1004812	7
6	C44,THRU C49	CAP, 39 UF 10V 10%	1000076	8
1	C54	CAP, 82 PF 100V 5%	1000015	9
1	C51	CAP, 560 PF 100V 5%	1000025	10
1	C53	CAP, 56 PF 100V 5%	1000012	11
1	C50	CAP, 270 PF 100V 5%	1000022	12
1	C52	CAP, 220 PF 100V 5%	1000021	13
1	C66	CAP, 27 PF 100V 5%	1001739	14
1	C65	CAP, 100 PF 100V 5%	1000016	15
2		SCREW, BHM #4-40 X .18 LG	9007650-4	16
2		NUT, KEP #4-40	9006557	17
37	D1 THRU D33, D41 THRU D44	DIODE, D872	1105275	18
8	D34, D36 D37	ZENER, IN 4732 A, 4.7V 5%	1105138	19
3	D35, [illegible]	ZENER, IN 749 A, 4.3V 5%	1109977	20
1	D38	ZENER, IN 825, 8.2V 5%	1101385	21
1	D39	ZENER, IN 751 A, 5.1V 5%	1110994	22
1	D40	CURRENT LIMITER, MCL 1301, 1MA	1105610	23
1	S1	SWITCH, ROCKER (8 POS)	1211164-04	24
1	(S1)	COVER, SWITCH (8 POS)	1211284-04	25
1	J1	CONNECTOR, 40 PIN HEADER	1209941	26
14		SPLIT LUGS	9006735	27
2		HANDLE, FLIP CHIP-AMBER	9008337-00	28
42		EYELET	9006732	29
1	R1	RES., 33 OHM 1/4W 5%	1300197	30
2	R2, R26	RES., 100 OHM 1/4 W 5%	1300229	31
1	R3	RES., 560 OHM 1/4W 5%	1301890	32
4	R4, R5	RES., 750 OHM 1/4W 5%	1301401	33
1	R6	RES., 910 OHM 1/4W 5%	1305374	34
15	R7 THRU R17, R24 R25, R28 THRU R30, R46	RES., 1.1K 1/4W 5%	1301475	35
1	R31	RES., 1.5K 1/4W 5%	1300391	36
3	R32, R33, R34	RES., 2K 1/4W 5%	1302388	37
1	R35	RES., 2.2K 1/4W 5%	1300417	38
1	R36, [illegible]	RES., 3K 1/4W 5%	1300432	39
3	R40, R41, R42	RES., 4.7K 1/4W 5%	1300447	40
2	R44, R45	RES., 7.5K 1/4W 5%	1301422	41
7	R48 THRU R54	RES., 20K 1/4W 5%	1302391	42
2	R56, R57	RES., 100K 1/4W 5%	1302466	43
6	R18 THRU R23	RES., 10K 1/4W 5%	1300479	44
2	R58, R59	RES., 82 OHM 1/2W 5%	1301781	45
2	R27, R47	RES., 10K 1/8W 1%	1303312	46
2	R85, R86	RES., 392 OHM 1/8W 0.1% 25 PPM	1309291	47
2	R82, R83	POT, 200 OHM 1/2W 10% 62 PR	1309150-10	48
2	R77, R87	RES., 1.2K 1/4W 0.5% 25 PPM	1301668	49
1	R79	RES., 1.69K 1/8W 0.1% 25 PPM	1309297	50
2	R80, R78	RES., 1.8K 1/8W 0.1% 25 PPM	1309295	51
3	R81, R88, R89	POT, 500 OHM 1/2W 10% 62 PR	1309150-8	52
1	R84	POT, 2K 1/2W 10% 62 PR	1309150-7	53

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

2501	14	1
AM 2504	12	24
8837	8	16
8251	8	16
74175	8	16
8235	8	16
74174	8	16
7493	10	5
74123	8	16
74161	8	16
IC TYPE	GND	+ 5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

FIRST USED ON OPTION MODEL

ETCH BOARD REV B

CHANGE NO. REVISIONS			
DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

DRN. M. Arnold DATE 9/24/74
CHK'D. [signature] DATE 10-28-74
ENG. [signature] DATE 12-3-74
PROJ. ENG. [signature] DATE 12-3-74
PROG. [signature] DATE 12-3-74
NEXT HIGHER ASSY
SCALE 1/4
SHEET 1 OF 10

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE
AD8-A 10 BIT A-D

SIZE D CODE CS NUMBER A008-0-1 REV. A
DIST.

DEC FORM NO. ORD 135-8

NOTES:

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
1	R60	RES., 47 1/4W 1% FUSIBLE	1310881-2	54
16	R61 THRU R76	RES., 1K 1/4W 1% FUSIBLE	1310981-0	55
1	R39	RES., 3.3K 1/4W 5%	1300439	56
1	R55	RES., 46.4K 1/8W 1%	1302414	57
1	R43	RES., 2.21K 1/2W 1%	1310631	58
2	Q37, Q38	TRANSISTOR, DEC 3009B	1503100	59
10	Q11,Q19,Q20,Q24,Q26,Q27, Q28,Q34 Q17, Q44	TRANSISTOR, SE 4020	1509587	60
20	Q1 THRU Q10,Q12 THRU Q16, Q21,Q22,Q23,Q25,Q45	TRANSISTOR, 2N4250	1509142	61
5	Q29,Q30,Q31,Q39,Q43	TRANSISTOR, DEC 8534D	1503409	62
2	Q32,Q35	FET, 2N5480	1510233	63
3	Q33,Q36,Q42	FET, 2N5245	1509681	64
1	Q40	TRANSISTOR, D45C8	1510414	65
1	Q41	TRANSISTOR, D44C3	1510171	66
3	L3,L4,L5	INDUCTOR, 100UH	1610682	67
2	L1,L2	INDUCTOR, 0.22UH	1603377	68
1	E24	I.C., 74123	1910436	69
3	E2,E33,E7	I.C., 7400	1905575	70
2	E10,E12	I.C., 7402	1909004	71
4	E3,E15,E18,E27	I.C., 7404	1909686	72
1	E28	I.C., 7406	1910741	73
1	E11	I.C., 7408	1910155	74
1	E32	I.C., 7418	1909928	75
1	E5	I.C., 742	1905577	76
1	E13	I.C., 7450	1905580	77
4	E8,E14,E23,E36	I.C., 7474	1905547	78
1	E4	I.C., 7493	1909054	79
2	E21,E27	I.C., 74174	1910652	80
1	E38	I.C., 74181	1910650	81
1	E29	I.C., 74175	1910651	82
3	E6,E26,E35	I.C., 8235	1909935	83
2	E1,E9	I.C., 8242	1909712	84
1	E17	I.C., 8251	1909594	85
4	E16,E25,E34,E37	I.C., 8837	1911116	86
2	E19,E31	I.C., 8881	1909705	87
1	E20	I.C., AM2504	1911626	88
2	E40,E42	I.C., DEC 2501 DIODE ARRAY	1910010	89
2	E39,E41	I.C., DG 501 C MUX	1911598	90
1	E30	I.C., MC 1408L-8 DAC	1911629	91
2	R37, R38	RES 2.7K 1/4W 5%	1300426	92
2		TAB, FASTON	9007112	93
1	R30	RES, 390Ω 1/4W 5%	1300309	94
1	R5	RES 750Ω 1/4W 1%	1302955	95

IC TYPE	GND	+ 5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

FIRST USED ON OPTION MODEL

ETCH BOARD REV

PARTS LIST

REV	CHANGE NO.	DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

DRN.	DATE	9/26/74
CHK'D.	DATE	10-28-74
ENG.	DATE	12-3-74
PROJ. ENG.	DATE	12-3-74
PROG.	DATE	12-3-74

NEXT HIGHER ASSY

SCALE

SHEET 2 OF 10

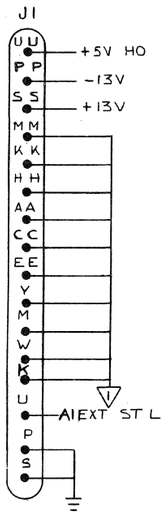
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

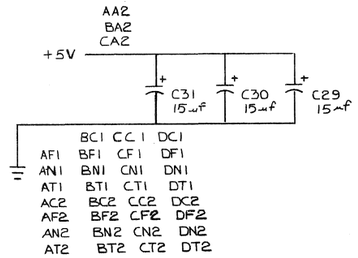
TITLE: AD8-A 10BIT A-D

SIZE D | CODE DCS | NUMBER A008-0-1 | REV. A

DIST.

DEC FORM NO. DRD 135-B

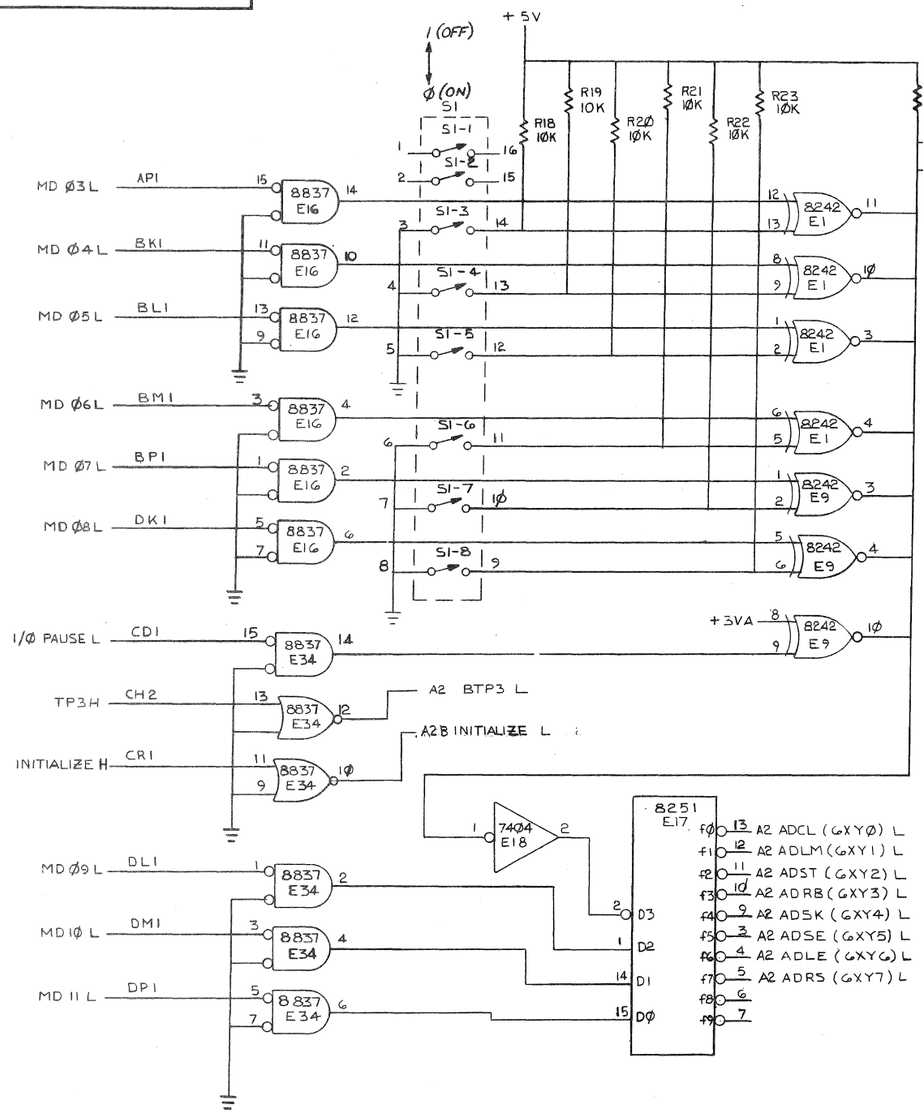


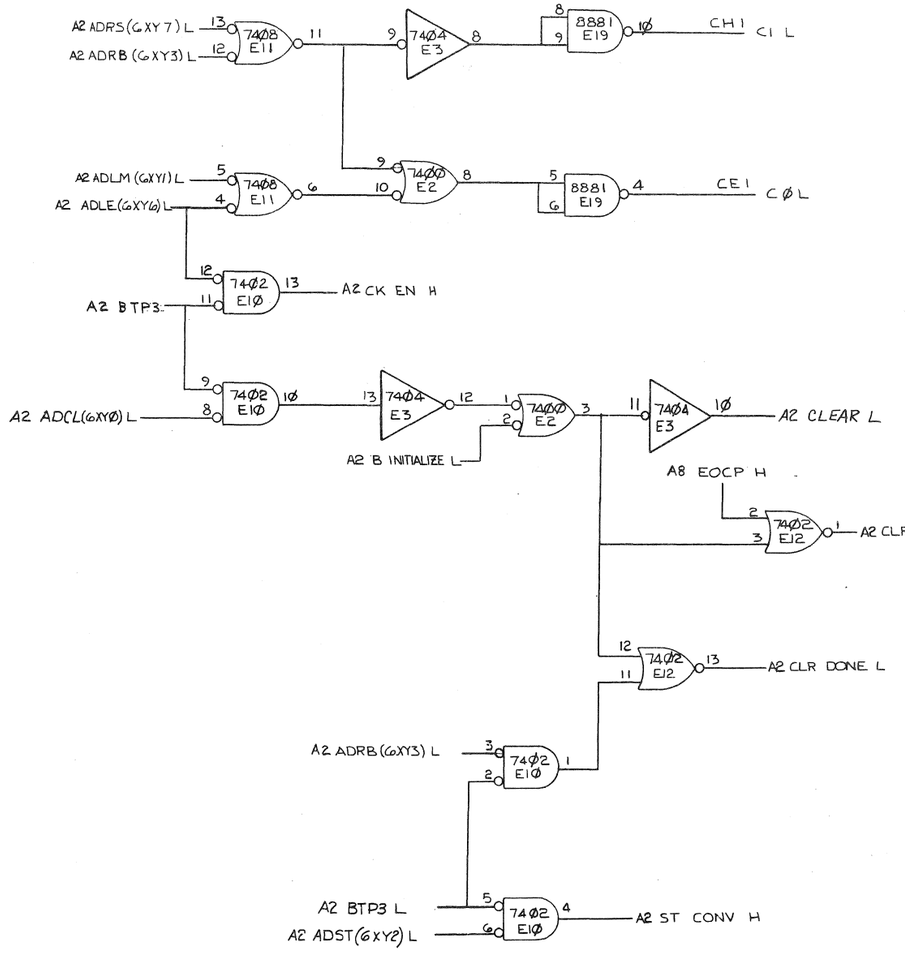


REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	AD8-A 10BIT AD (A1)	SIZE D	CODE CS	NUMBER AØØ8-Ø-1 REV. A
SCALE	SHEET 3 OF 10	DIST.		

DEC FORM NO. DRD 128





REVISIONS		
CHK	CHANGE NO.	REV.

(DECODER)

TITLE	SIZE	CODE	NUMBER	REV.
AD8-A 10 BIT A-D (A2)	D	CS	AØØ8-Ø-1	A

SCALE — SHEET 4 OF 10 — DIST.

DEC FORM NO. DRD 128

8235 E26
A8 ADB Ø4 (1) L
A3 EXT ST EN (1) H
A8 ADB Ø5 (1) L
A3 INC EN (1) H
A8 ADB Ø6 (1) L
A3 UNIPOLAR (1) H
A8 ADB Ø7 (1) L
A4 EN AD (1) L
BR1 DATA Ø4 L
BS1 DATA Ø5 L
BU1 DATA Ø6 L
BV1 DATA Ø7 L
A2 ADRB (6XY3) L

8235 E35
A8 ADB Ø8 (1) L
A3 MUX 8 (1) H
A8 ADB Ø9 (1) L
A3 MUX 9 (1) H
A8 ADB 1Ø (1) L
A3 MUX 1Ø (1) H
A8 ADB 11 (1) L
A3 MUX 11 (1) H
A2 ADRB (6XY7) L
DR1 DATA Ø8 L
DS1 DATA Ø9 L
DU1 DATA 1ØL
DV1 DATA 11L

8235 E6
A8 ADB Ø2 (1) H
A4 AD DØNE (1) H
A4 TMG ERR (1) H
A3 DONE INT EN (1) H
A8 ADB Ø3 (1) L
A3 TMG ERR INT EN (1) H
AR1 DATA ØØ L
AS1 DATA Ø1 L
AU1 DATA Ø2 L
AV1 DATA Ø3 L
A2 ADLE (6YY6) L

8837 E25 (×6)
8837 E37 (×6)

A2 CLEAR L
A2 CK EN H
74174 E27
A3 DONE INT EN (1) H
A3 TMG ERR INT EN (1) H
A3 EXT ST EN (1) H
A3 UNIPOLAR (1) H

A3 INC EN (1) H
A8 EOCP H
7420 E5
7400 E2
A3 MUX CHANGE H
7404 E3
+3VA
7404 E15
+3VB
7404 E15
+3VC
A2 ADLM (6YY1) L
A2 BTP3 L
7404 E3
A3 LD MUX L

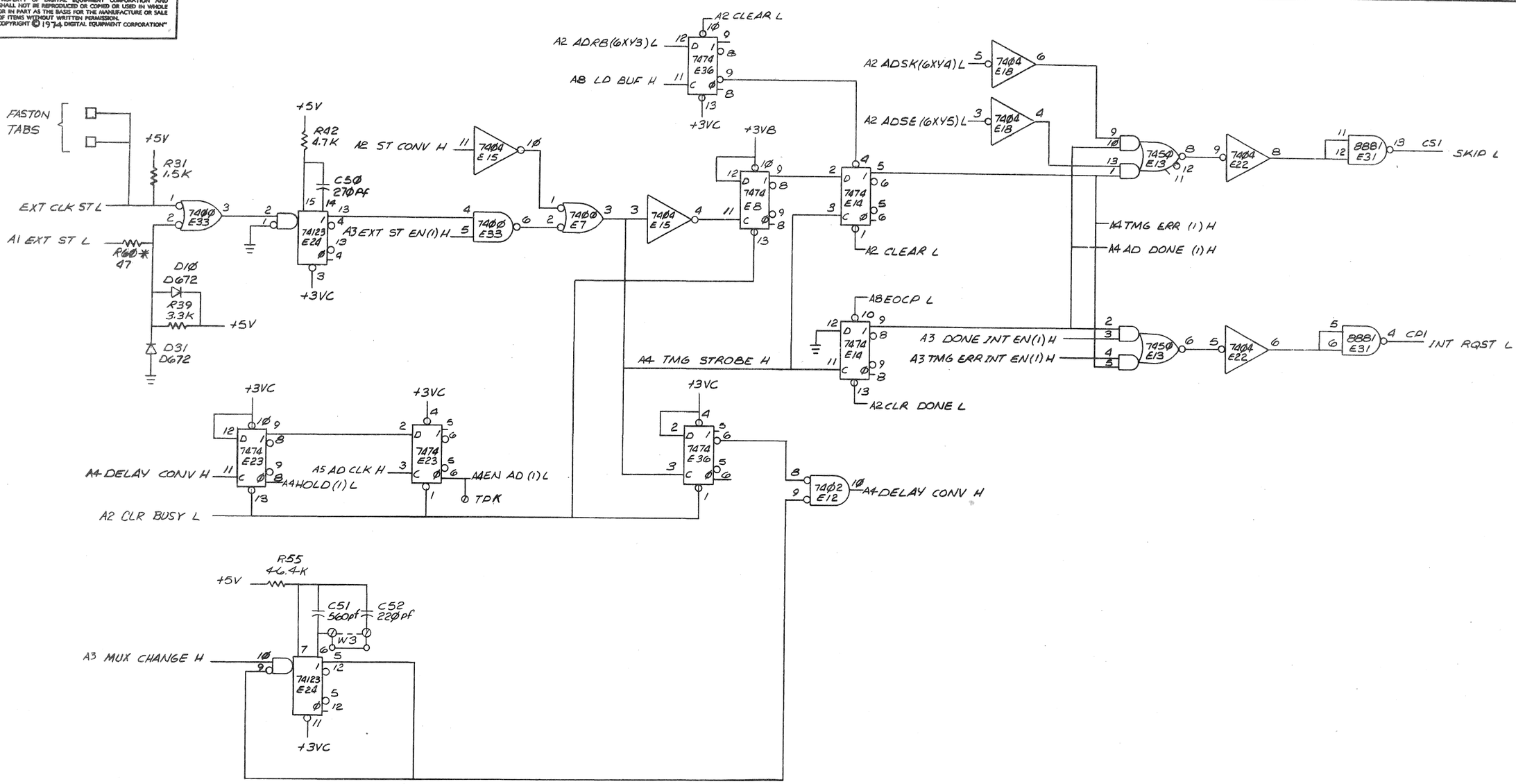
74161 E38
MSB MSB
LSB LSB
A3 MUX Ø8 (1) H
A3 MUX Ø9 (1) H
A3 MUX 1Ø (1) H
A3 MUX 11 (1) H
A2 CLEAR L
CLR
LD
CLK
CNT EN
CRY EN
7408 E11

REVISIONS		
CHK	CHANGE NO.	REV.

DEC FORM NO. DRD 138

(DATA INTERFACE)

TITLE		SIZE	CODE	NUMBER	REV.
AD8-A 1Ø BIT A-D	(A3)	D	CS	AØØ8-Ø-1	A
SCALE	SHEET 5 OF 10	DIST.			



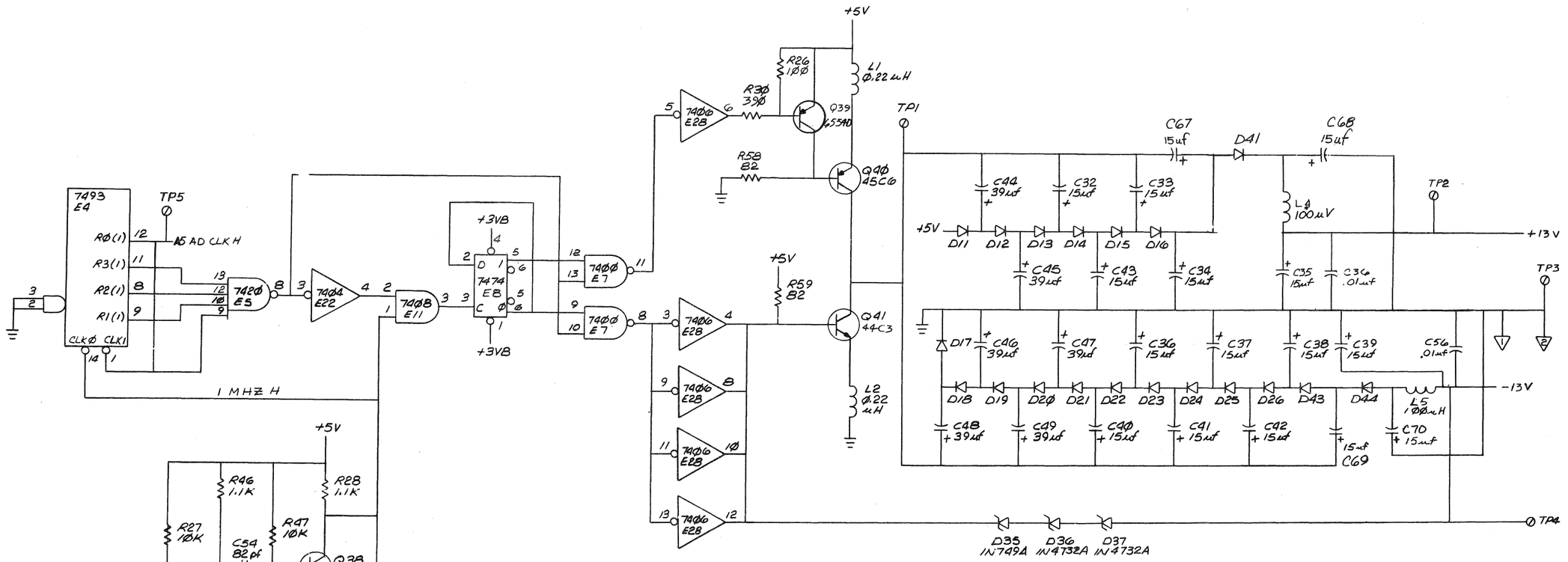
* INDICATES FUSIBLE RESISTOR

REVISIONS		
CHK	CHANGE NO.	REV.

(FLAGS)

TITLE	SIZE	CODE	NUMBER	REV.
AD8-A 10BIT A-D (A4)	D	CS	A008-0-1	A
SCALE	SHEET 6 OF 10	DIST.		

DEC FORM NO. DRD 128



UNLESS OTHER WISE INDICATED ALL DIODES ARE D672

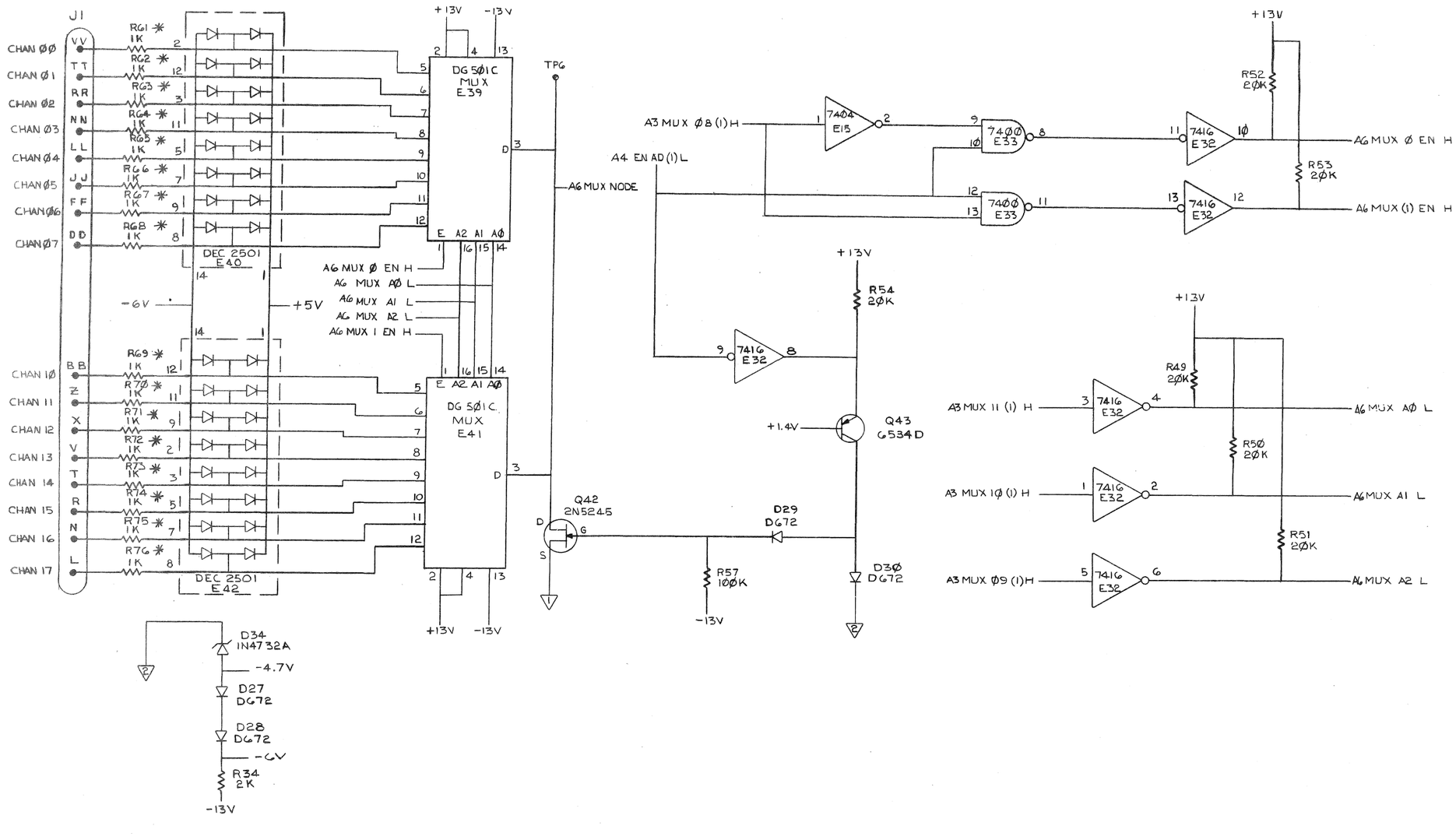
REVISIONS		
CHK	CHANGE NO.	REV.

(HQ POWER SUPPLY)

TITLE	SIZE	CODE	NUMBER	REV.
AD8-A 10BIT A-D (A5)	D	CS	A008-0-1	A
SCALE	SHEET 7 OF 10	DIST.		

DEC FORM NO. DRD 138

NOTES:
1. RG1 THRU R76 ARE FUSIBLE RESISTORS



* INDICATES FUSIBLE RESISTOR

REVISIONS		
CHK	CHANGE NO.	REV.

(MULTIPLEXER)

TITLE	SIZE	CODE	NUMBER	REV.
AD8-A 1ØBIT A-D (AG)	D	CS	AØØ8-Ø-1	A
SCALE	SHEET 8 OF 1Ø	DIST.		

DEC FORM NO. DRD 138

L3 1ØØµH
+5V
+5V HQ
-13V
C66 27pf
C59 .Ø1uf
C55 15uf
MC1Ø8L-8 DAC E3Ø
AB AD Ø2 H
AB AD Ø3 H
AB AD Ø4 H
AB AD Ø5 H
AB AD Ø6 H
AB AD Ø7 H
AB AD Ø8 H
AB AD Ø9 H
R7 1.1K
R8 1.1K
Q1Ø 2N4250
R6 91Ø
+13V
R81 5ØØ (CW)
R79 1.69K
C6Ø .Ø1uf
D38 1N825
R8Ø 1.8K
R36 3K
Q9 2N4250
Q8 2N4250
Q7 2N4250
Q6 2N4250
R4 75Ø
R56 1ØØK
Q11 SE4Ø2Ø
C61 .Ø1uf
R32 2K
R48 2ØK
Q16 2N4250
VB Q17 2N4020
R78 1.8K 0.1%
-13V
R1 33
R2 1ØØ
AGMUX NODE
R12 1.1K
TD7
Q22 2N4250
Q21 2N4250
C65 1ØØpf
D6 DG72
R85 392
R86 392
Q28 SE4Ø2Ø
D33 DG72
R16 1.1K
R15 1.1K
-13V
R9 1.1K
R35 2.2K
R1Ø 1.1K
R5 75Ø 1%
R3 56Ø
C62 .Ø1uf
Q5 2N4250
Q4 2N4250
Q3 2N4250
Q2 2N4250
Q1 2N4250
+1.4V
D2 DG72
VB Q44 2N4020
R84 2K
R43 2.21K
-13V
A7 COMP H
Q15 2N4250
Q14 2N4250
Q13 2N4250
Q12 2N4250
D1 DG72
+5V
R11 1.1K
D4 DG72
D5 DG72
A4 HOLD (1) L
D3 DG72
Q36 2N5245
Q18 2N4250
Q2Ø SE4Ø2Ø
Q19 SE4Ø2Ø
R14 1.1K
R13 1.1K
D7 DG72
C63 .Ø1uf
D39 1N751
-13V
+13V
D4Ø MCL3Ø1
Q34 SE4Ø2Ø
Q33 2N5245
C64 .ØØ1uf
Ø TP8
A3 UNIPOLAR (1) H
A4 EN AD (1) H
A8 AD ØØ H
7400 E22
8881 E19
Q29 G534D
R37 2.7K
R38 2.7K
Q3Ø G534D
A7 EN AD H
A8 AD Ø1 H
8881 E31
+13V
+1.4V
R77 1.2K Ø.5%
R82 2ØØ
R87 1.2K 0.5%
R83 2ØØ
-13V
Q23 2N4250
Q24 SE4Ø2Ø
Q25 2N4250
Q26 SE4Ø2Ø
R44 7.5K
R45 7.5K
CW
D8 DG72
D9 DG72
Q35 2N5460
Q31 G534D
Q32 2N5460
Q27 SE4Ø2Ø
R33 2K
-13V
A4 ENAD (1) L
7404 E22
EN AD H A7
R17 1.1K
R4Ø 4.7K
R41 4.7K
8881 E31
Ø
-4.7V
D32 DG72

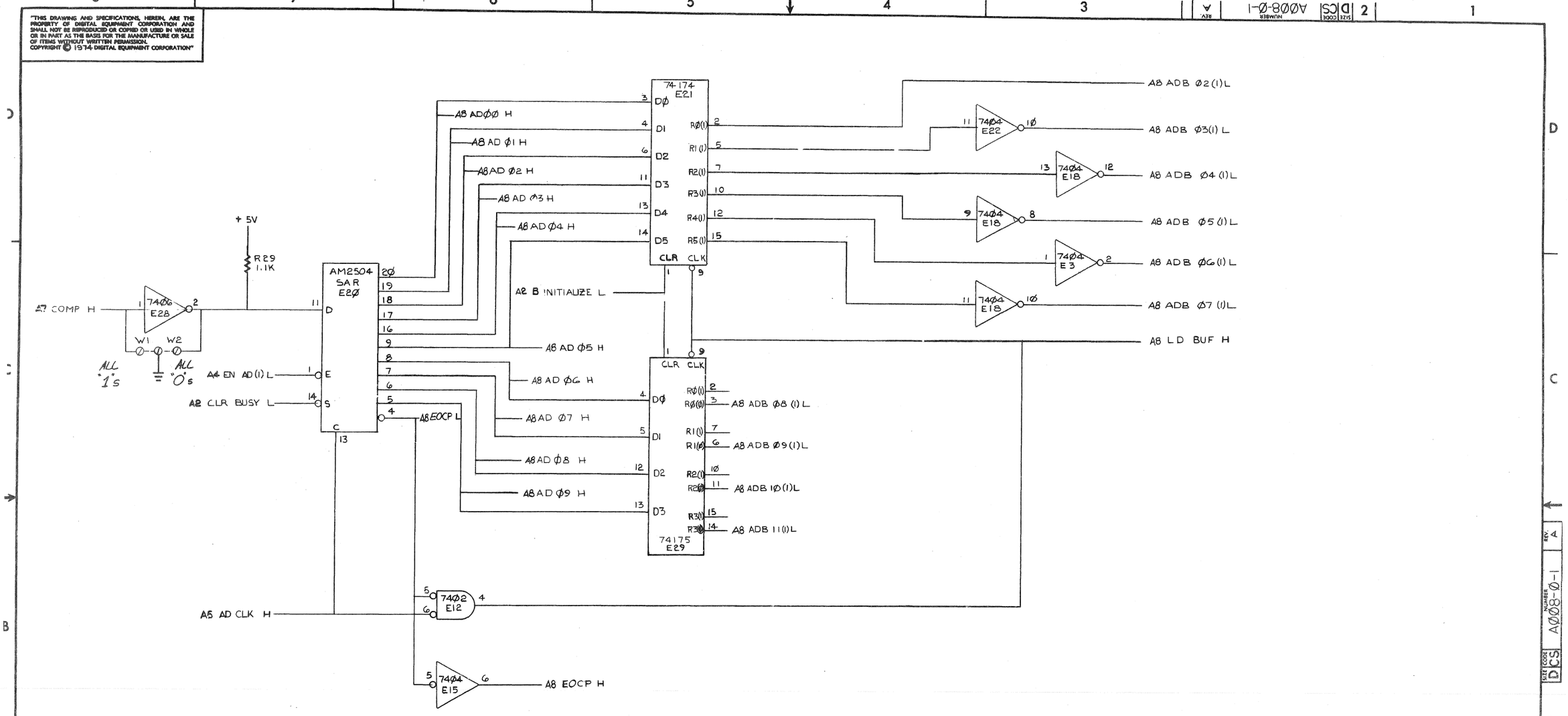
REVISIONS

CHK	CHANGE NO.	REV.

(A/D CONVERTER)

TITLE AD8-A 1Ø BIT A-D (A7)
SIZE D | CODE CS | NUMBER AØØ8-Ø-1 | REV. A
SCALE | SHEET 9 OF 1Ø | DIST.

DEC FORM NO. DRD 128



REVISIONS		
CHK	CHANGE NO.	REV.

(BUFFER)

TITLE	SIZE	CODE	NUMBER	REV.
AD8-A 1ØBIT A-D (A8)	D	CS	AØØ8-Ø-1	A
SCALE	SHEET 10 OF 10	DIST.		

DEC FORM NO. DRD 138

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

MADE BY [illegible] DATE 4-3-75	CHECKED [illegible] DATE 4-3-75	SECTION
ENG [illegible] DATE 4-3-75	PROD DATE [illegible]	ISSUED SECT.

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION
1.	MP-AD8-A	DRAWING DIRECTORY	1
2.	AØØ8	AD8-A MODULE	1
3.	1700021-02	SHIELD	2
4.	1210918-15	SHELL, BERG	1
5.	1210089-6	PIN, BERG	50
6.	1211166	STRAIN RELIEF	1
7.	7011017-Ø-Ø	FASTON JUMPER	1
8.	EK-AD8A-TM-ØØ1	USER'S MANUAL	1
9.	ZF216-RB	AD8-A DIAGNOSTIC (Logic)	1

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
AD8-A SHIPPING LIST	NONE	A	PL	AD8-A-6		
	SHEET 1 OF 1	DIST.				

DEC FORM NO. 16-1031
DRA 110

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

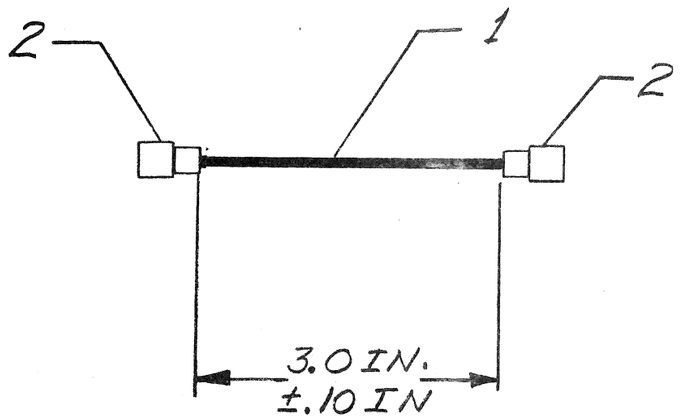
PARTS LIST

MADE BY Geo. Garvin DATE 4-3-75	CHECKED [illegible] DATE 4-3-75	SECTION
ENG Geo. Garvin DATE 4-3-75	PROD John Hollis DATE 4-15-75	ISSUED SECT.

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION
1.	MP-AD8-A	DRAWING DIRECTORY	1
2.	AØØ8	AD8-A MODULE	1
3.	1700021-02	SHIELD	2
4.	1210918-15	SHELL, BERG	1
5.	1210089-6	PIN, BERG	50
6.	1211166	STRAIN RELIEF	1
7.	7011017-0-0	FASTON JUMPER	1
8.	EK-AD8A-TM-ØØ1	USER'S MANUAL	1
9.	ZF216-RB	AD8-A DIAGNOSTIC (Logic)	1
10.	BC08R-Ø8	CABLE, EIGHT FOOT	1
11.	MP-H322-Ø	DRAWING DIRECTORY	1
12.	H322	PANEL AND BRACKETS	1
13.	9007880	TIE WRAPS SST-1.5M	25
14.	A-DC-7412826-Ø-Ø	DECAL SET	1
15.	D-IA-7010872-Ø-Ø	EXT. CLK. START CABLE	1

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
AD8-B SHIPPING LIST	NONE	A	PL	AD8-B-Ø		
	SHEET 1 OF 1	DIST.				

DEC FORM NO. 16-1031
DRA 110



QTY.	DESCRIPTION	PART NO.	ITEM NO.
2	TAB, FASTON (RED)	9007917	2
A/R	WIRE #18AWG STRND.	9107360	1

PARTS LIST

REV.	REVISIONS	CHANGE NO.	CHK

FIRST USED ON OPTION/MODEL	UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES	DRN.	DATE
AD8-A	TOLERANCES	J Bird	7MAR75
	DECIMALS: .xxx = .005, .xx = .02, .x = .1 / ANGLES: ±0° 30'	CHK'D.	DATE 7MAR75
	REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY √	ENG.	DATE 7MAR75
	MATERIAL: H	PROJ. ENG.	DATE 3/7/75
	FINISH: H	PROD.	DATE M-3-75

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: CONNECTOR CABLE

NEXT HIGHER ASSY.: B-DD-AD8-A

SCALE 1/1

SHEET 1 OF 1

SIZE	CODE	NUMBER	REV.
B	IA	7011017-0-0	

DIST.

DEC 16-(325)-1080-1A-R373
DRB 100

WIRE TABLE

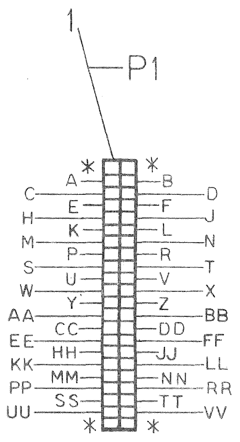
ITEM NO.	DESCRIPTION AWG	DESCRIPTION COLOR	FROM CONNECTION	FROM WITH	TO CONNECTION	TO WITH	REMARKS
3	24 TWP	BLK	CABLE 1		PI-S	2	LOGIC GND
		BLU			PI-U	2	EXT A/D ST L
	SHIELD	—			—	—	CUT FLUSH
	24 TWP	BLK			—	—	CUT FLUSH
		YEL			PI UU	2	+5V HQ
	SHIELD	—			—	—	CUT FLUSH
	24 TWP	GRN			PI-VV	2	A/D CH ØØ
		BLK		SOLDER	PI-MM	2,7	SEE NOTE 3 HQ GND
	SHIELD	—					
	SHIELD	—					
	24 TWP	BLK					
		WHT			PI-TT	2	A/D CH Ø1
	24 TWP	BRN			PI-RR	2	A/D CH Ø2
		BLK		SOLDER	PI-KK	2 7	SEE NOTE 3 HQ GND
	SHIELD	—					
	SHIELD	—					
	24 TWP	BLK					
		RED			PI-NN	2	A/D CH Ø3
	24 TWP	GRN	CABLE 2		PI-LL	2	A/D CH Ø4
		BLK		SOLDER	PI-HH	2,7	SEE NOTE 3 HQ GND
	SHIELD	—					
	SHIELD	—					
	24 TWP	BLK					
		WHT			PI-JJ	2	A/D CH Ø5
	24 TWP	BRN			PI-FF	2	A/D CH Ø6
		BLK		SOLDER	PI-EE	2,7	SEE NOTE 3 HQ GND
	SHIELD	—					
	SHIELD	—					
	24 TWP	BLK					
		RED			PI-DD	2	A/D CH Ø7
	24 TWP	YEL			PI BB	2	A/D CH 1Ø
		BLK		SOLDER	PI-CC	2,7	SEE NOTE 3 HQ GND
	SHIELD	—					
	SHIELD	—					
	24 TWP	BLK					
3		BLU			PI-Z	2	A/D CH 11

WIRE TABLE (CON'T.)

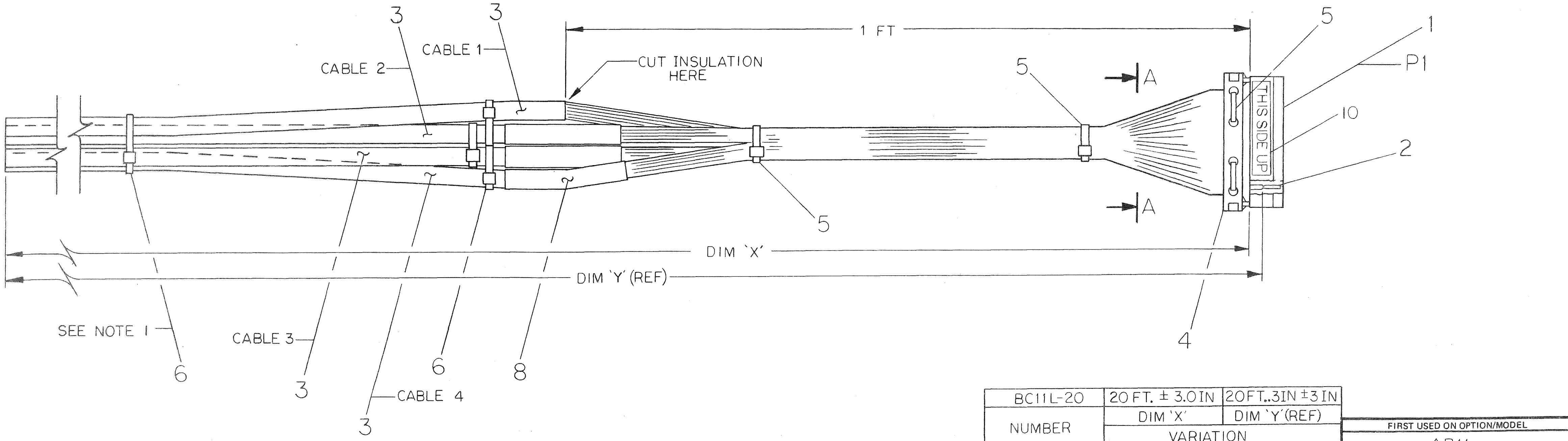
ITEM NO.	DESCRIPTION AWG	DESCRIPTION COLOR	FROM CONNECTION	FROM WITH	TO CONNECTION	TO WITH	REMARKS
3	24 TWP	GRN	CABLE 3		PI-X	2	A/D CH 12
		BLK		SOLDER	PI-AA	2,7	SEE NOTE 3 HQ GND
	SHIELD	—					
	SHIELD	—					
	24 TWP	BLK					
		WHT			PI-V	2	A/D CH 13
	24 TWP	BRN			PI-T	2	A/D CH 14
		BLK		SOLDER	PI-Y	2,7	SEE NOTE 3 HQ GND
	SHIELD	—					
	SHIELD	—					
	24 TWP	BLK					
		RED			PI-R	2	A/D CH 15
	24 TWP	YEL			PI-N	2	A/D CH 16
		BLK		SOLDER	PI-W	2,7	SEE NOTE 3 HQ GND
	SHIELD	—					
	SHIELD	—					
	24 TWP	BLK					
		BLU			PI-L	2	A/D CH 17
	24 TWP	GRN	CABLE 4		PI-A	2	WRITE THRU
		BLK			PI-B	2	DISP CHAN 02
	SHIELD	—			—	—	CUT FLUSH
	24 TWP	WHT			PI-C	2	ERASE
		BLK			PI-D	2	INTENSIFY
	SHIELD	—			—	—	CUT FLUSH
	24 TWP	BRN			PI-E	2	NON STORE
		BLK			PI-H	2	ERASE RET
	SHIELD	—			—	—	CUT FLUSH
	24 TWP	RED			PI-P	2	LOGIC GND
		BLK			—	—	CUT FLUSH
	SHIELD	—			—	—	CUT FLUSH
	24 TWP	YEL			PI-F	2	X OUT
		BLK		SOLDER	PI-M	2,7	SEE NOTE 3 X HQ GND
	SHIELD	—					
	SHIELD	—		SOLDER	PI-K	2,7	SEE NOTE 3 Y HQ GND
	24 TWP	BLK					
3		BLU			PI-J	2	Y OUT

NOTES:

1. PLACE CABLE TIES APPROXIMATELY EVERY 10 IN. AND WHEREVER INDICATED.
2. USE ITEM #9 (CABLE MARKERS) TO IDENTIFY CABLES BY NUMBER. POSITION APPROXIMATELY 2 FT. FROM EACH END.
3. BLACK WIRE (FROM #24 TWP) AND SHIELD TO BE CUT APPROXIMATELY .7" FROM CABLE INSULATION. BLACK WIRE (STRIPPED) AND SHIELD TO BE TWISTED AND SOLDERED TO BLACK IPVC (ITEM #7, APPROXIMATELY 12" LG.)



VIEW A-A
SCALE: NONE
* NOT USED



LEGEND

NUMBER	DIM 'X'	DIM 'Y' (REF)
BC11L-20	20 FT. ± 3.0 IN	20 FT..3 IN ± 3 IN
	VARIATION	

PARTS LIST

QTY.	DESCRIPTION	PART NO.	ITEM NO.
1	LABEL, THIS SIDE UP	3611567	10
A/R	CABLE MARKERS		9
A/R	TUBING, SHRINK BLK	9107685	8
A/R	WIRE, #22 AWG IPVC BLK	9107350-00	7
A/R	CABLE TIE	9007880	6
A/R	CABLE TIE	9007031	5
1	STRAIN RELIEF	1211166	4
A/R	CABLE, BELDEN 8778	1700010	3
38	PIN, BERG (47706)	1210089-6	2
1	CONN. HOUSING, 40 PIN	1210918-15	1

FIRST USED ON OPTION/MODEL: AR11

DIMENSIONAL TOLERANCE
DIMENSIONS ARE MILLIMETERS / INCHES UNLESS OTHERWISE SPECIFIED

MILLIMETERS	INCHES	ANGLES
X.XX = ±0,10	.XXX = ±.005	±0° 30'
X.X = ±0,5	.XX = ±.02	
X = ±2,	.X = ±.1	

THIRD ANGLE PROJECTION
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL: SEE PARTS LIST
FINISH: —//—

		DATE
DRN.	Carl McCoy	6-19-74
CHK'D.	V. K. Cable	6-24-74
ENG.	A. C. Filz	6-25-74
PROJ. ENG.	A. C. Filz	6-25-74
PROD.	[illegible]	6-25-74

NEXT HIGHER ASSY. —//—
SCALE 1/1
SHEET 1 OF 1

digital

TITLE: CABLE, BC11L

SIZE	CODE	NUMBER	REV.
D	UA	BC11L-Ø-Ø	A

DIST.

REVISIONS

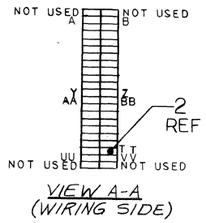
REV.	CHANGE NO.	CHK
A	BC11L-00001 A.C. FILZ 10-1-74	[illegible] 10-4-74

DEC FORM NO. DRD 100 B

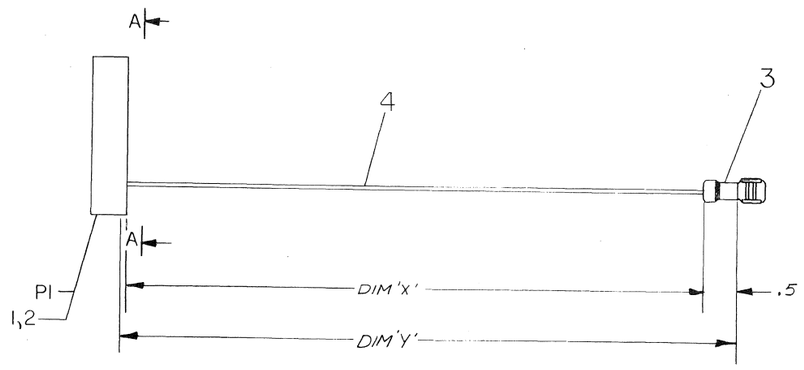
WIRE TABLE

ITEM NO.	DESCRIPTION AWG	COLOR	FROM CONN.	WITH ITEM	TO CONN.	WITH ITEM	SIGNAL NAME
4	22	WHT	P1-11	2	P2	3	EXT. CLK. START L

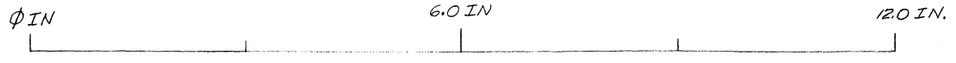
LEGEND NUMBER	DIM 'X' VARIATION	DIM 'Y' (PRECUT) REF
7010872-0J	8 IN. ± .5 IN.	8.65 IN. ± .5 IN



VIEW A-A
(WIRING SIDE)



DO NOT REDUCE
(FOR MANUFACTURING PURPOSES ONLY)
SCALE



A/R			
A/R	WIRE, 22AWG STRAND (WHT)	9107350-99	4
1	FEMALE, TERMINAL	9007970	3
1	PIN, BERG #48015	1210089-4	2
1	CONNECTOR, BERG	1210918-15	1
	DESCRIPTION	DWG./PART NO.	ITEM NO.

7010872-03

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

	CLASS OF ACCURACY (CHECK ONE)	NOMINAL DIMENSION RANGE INCHES: OVER 0 TO 0.2	OVER 0.2 TO 1.2	OVER 1.2 TO 4.0	OVER 4.0 TO 12.0	OVER 12.0 TO 40.0	OVER 40.0 TO 80.0
ANGLES ±0° 30'							
SURFACE QUALITY IN MICROINCHES	MEDIUM ☐	±.004	±.008	±.012	±.016	±.024	±.04
	PREFERRED ☐	±.012	±.016	±.025	±.04	±.063	±0.1

QUANTITY & VARIATION

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DWG

MATERIAL —"—

FINISH —"—

DRN.	J.B.Loof	31 JAN 75
CHK'D		24 MAR 75
ENG.		24 MAR 75
PROJ. ENG.		24 MAR 75
PROD.		15 APR 75

NEXT HIGHER ASSY.

FIRST USED ON: AD8-A

digital

TITLE: EXT. CLK. START CABLE

SIZE	CODE	NUMBER	REV.
D	1A	7010872-0-0	

SCALE NONE

SHEET / OF /

DIST.

REVISIONS	REV.	CHANGE NO.	CHK

B.L.M. 4-75

DEC FORM NO. DRD 100-C