UDC8
universal digital
control subsystem
maintenance manual

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CHAPTER 1
GENERAL INFORMATION

1.1 GENERAL

The UDC8 Universal Digital Controller I/O Subsystem, manufactured by Digital Equipment Corporation, is a peripheral device to be used with PDP-8 Computer Systems in industrial data acquisition and control applications. This device can be used with both the positive and the negative bus PDP-8 computers (refer to the *PDP-8 Maintenance Manual* for information on the computers and I/O bus structures).

1.2 PURPOSE

The UDC8 operates under computer program control as a highly flexible digital input/output device capable of interrogating digital inputs and driving digital outputs connected to functional modules. Up to 256 digital sense and control functional modules, each handling up to 12 individual digital points, can be directly accessed by the UDC8. I/O functions that can be handled by the existing complement of modules include driver output, relay output, contact sense, contact interrupt, and D/A converters. This complement of functional modules provides the means for controlling and monitoring most devices found in an industrial and process control environment. Selection and inclusion of appropriate functional input and output modules in the UDC8 tailors the subsystem to a specific application.

1.3 FUNCTIONAL DESCRIPTION

The UDC8 consists of one *master file,* up to 63 *file units* (DD02) and up to 256 *functional modules* (Figure 1-1). The *interface controller* (DD01) of the master file coordinates all activities within the UDC8 in response to programmed IOT instructions, address, and data from the computer. Each I/O file unit is set up to respond to a unique 2-digit octal address (6 binary bits), and each module slot in this unit responds to a unique 2-bit binary address.

Thus, each module can be accessed directly, using an 8-bit address. Once accessed, data (DATAO) can be loaded into the module for output control, or data (DATAI) can be read into the computer from a module to be sensed. In addition to the direct access feature, the UDC8 contains an interrupt structure, which may be enabled or disabled under program control, and an automatic scan feature to determine the address of an interrupting module. Only those functional modules that require fast program intervention are equipped with and connect to the interrupt structure. A third feature of the UDC8 is a hardware gating scheme for determining when an input contact has changed state, and the direction of that change. Both the interrupt structure and the hardware gating scheme significantly reduce computer processing overhead.
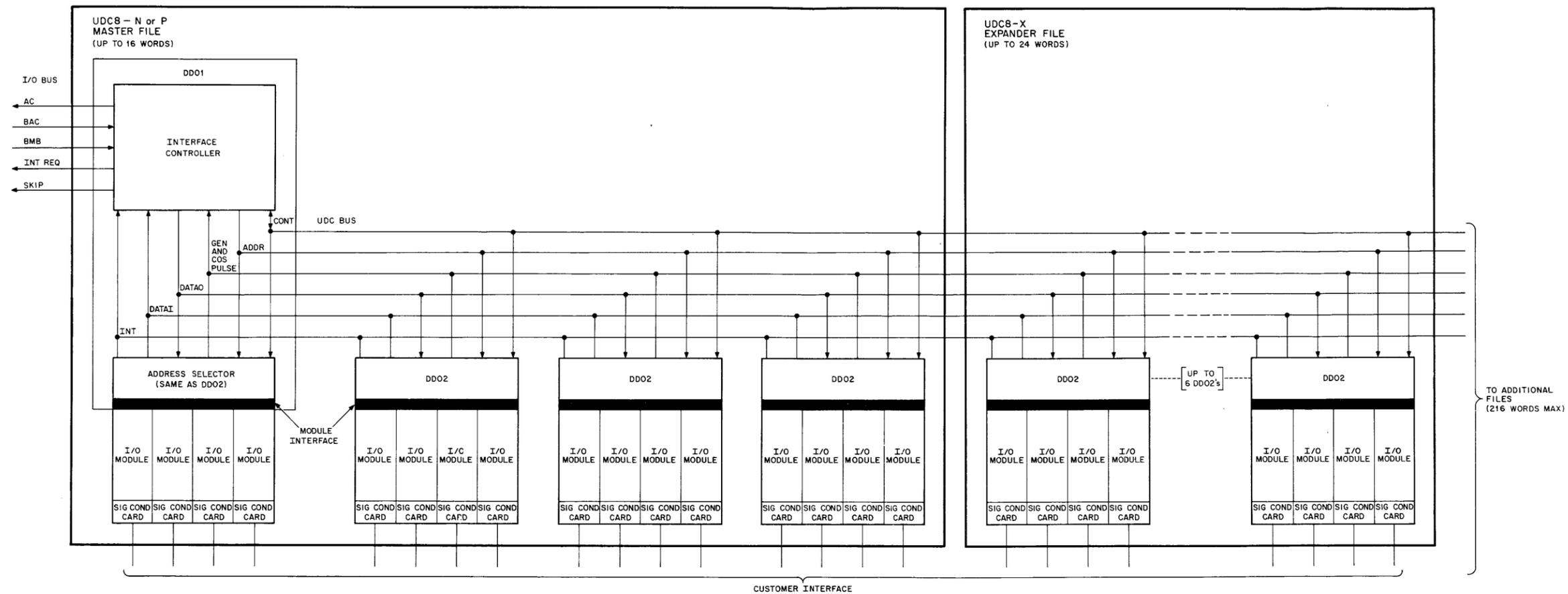
Figure 1-1 UDC8 Overall Block Diagram

1.4 PHYSICAL DESCRIPTION

1.4.1 System Organization

The UDC8 System is completely modular for ease of system configuration and expansion (Table 1-1). For applications requiring 16 digital words (192 digital points) or less, the system is available in a *single-cabinet* configuration. Systems requiring greater than 16 digital words but less than 64 digital words are housed in a *dual-cabinet* configuration — one cabinet to mount the electronics, and one for the screw terminal connectors. Four dual-cabinet configurations are required to implement a maximum system of 256 digital words (3072 digital points).

The system's electronics cabinets are organized in files. The first file in the system is a master file which contains the computer interface, system timing and control, address/scan register, COS gating, and address decoding hardware for selection of up to four digital words. The master file can also contain three additional file units, each providing address decoding for up to four digital words. The hardware for each 4-word group is implemented by adding up to four functional I/O signal-conditioning modules and the required screw terminal cable assemblies — one for each module. Fully implemented, the master file contains 16 digital words.

Expansion beyond 16 words is accomplished by the addition of expander files. Each expander file contains provision for a total of 24 words (288 digital points) in six file units.

Industrial packaging and modular design permit the UDC8 to be configured and modified according to application needs. The UDC8 is available with screw terminals which provide a conveninet means for connecting customer field wiring to the UDC functional modules. The screw terminals can be housed in the logic cabinet or in a separate cabinet located adjacent to the logic cabinet. The logic for a maximum UDC8 configuration of 256 words (functional modules) is housed in four industrial-type cabinets. Figure 1-2 illustrates the maximum configuration, including screw terminal cabinets, and locates the major units and functional modules of the UDC8. The major units and modules are described in the following paragraphs.

1.4.2 Logic and Screw Terminal Cabinet H964AA/AB

The H964AA/AB Cabinet is a 19 in. industrial-type cabinet which contains the 849A Power Control, H740D Power Supply, two top-mounted forced-air-cooling fans, air filters, and full front and rear doors. It will house one UDC8 file and, with H964MA mounting hardware, the necessary screw terminals for connection of field wiring. The UDC8 file is mounted at the top, the screw terminals just underneath, and the power elements at the bottom. Cabinet cooling is accomplished by blowing air down from the top of the cabinet and using the hole in the bottom of the cabinet for exhaust. Bottom entry of field wiring is standard, although top, rear entry is available as an option. See Figure 4-1 for cabinet dimensions.

1.4.3 Logic and Screw Terminal Cabinets H964CA, CB, CC, CD

The H964CA, CB, CC, and CD Cabinets consist of a pair of 19 in. industrial-type cabinets secured to each other. The right-hand cabinet (as viewed from the wirewrap side) houses the UDC logic, while the left-hand cabinet contains the necessary screw terminals. The logic cabinet is capable of housing up to three UDC8 files. In addition to the UDC8 files, the logic cabinet contains the 849A Power Control, one H740D Power Supply for each file implemented, two top-mounted forced-air-cooling fans, air filters, and full front and rear doors. The screw terminal cabinet contains the necessary screw terminals for connection of field wiring. The screw terminals are secured to the cabinet with H964MA mounting hardware. Bottom entry of field wiring is standard, although top, rear entry is available as an option.

Table 1-1

System Organization

Item	Description	Model		Prerequisite
System Cabinets	Single cabinet for UDC System up to 16 digital words (192 digital points). Contains logic power supply, cooling fans, and filters. Screw terminals that mount in the same cabinet requires separate mechanical assembly (Model H964MA).	H964A	(bottom entry only of field cables).	
			A-115V power supply	- - - -
			B-230V power supply	- - - -
	Mechanical assembly for mounting screw terminals in single cabinets.	H964MA		H964AA or H964AB
	EXAMPLE: Model H964AA designates a single cabinet (bottom entry only of field cables, with 115V power supply).			
	Dual cabinet for UDC8 System. One cabinet houses system electronics and logic (contains logic power supplies, cooling fans, and filters). Second cabinet for termination of input field wiring on screw terminals.	H964C	A-top or bottom entry of field cables. 115V power supply	- - - -
			B-bottom entry only of field cables. 115V power supply	- - - -
			C-top or bottom entry of field cables. 230V power supply	- - - -
			D-bottom entry only of field cables. 230V power supply	- - - -
Master File	Basic UDC8 system file contains interface and control, address/scan register, change-of-state (COS) gating, and provision for installing four functional I/O modules (48 digital points) and I/O cable. Master file may be expanded to 16 digital words (192 digital points) by adding three DD02 File Units and appropriate number of functional I/O and signal-conditioning modules.	UDC8	N-negative bus interface	H964A or H964C PDP-8/I
			P-positive bus interface	H964A or H964C PDP-8/L or PDP-8/E

Table 1-1 (Cont)
System Organization

Item	Description	Model		Prerequisite
Expander File	Provides expansion capability. Expander file contains mounting hardware, file I/O cable, and provision for installing four digital words and up to five DD02 File Units, each capable of containing four digital words. (Fully implemented expander file contains 24 functional I/O modules — 24 digital words or 288 digital points.)	UDC8-X	A-second or third file in electronics cabinets B-first file in each additional electronics cabinets	UDC8 Master File plus H964C Dual Cabinet Second H964C Dual Cabinet
File Units	Provides address decoding, control logic, and DD02 capacity for mounting up to four functional I/O and signal-conditioning modules (four digital words or 48 digital points).			UDC8 Master File, Expander Files
Functional I/O Modules	Contact Sense (relay) Contact Interrupt (relay) Contact Sense (Solid State) Contact Interrupt (Solid State) Single-shot Driver Single-shot Relay Flip-flop Driver Flip-flop Relay Latching Relay DAC I/O Counter	W730 W732 W740 W742 M686 M806 M684 M804 M802 A633 W734		Master File, Expander Files, DD02 File Units
Signal-Conditioning Modules	Common Power Isolated Power Solid State Driver Buffer — 0V to +10V Buffer — +1V to +5V Buffer — 4 mA to 20 mA Buffer — 10 mA to 50 mA	W400 W402 W403 A233 A234 A235 A236		Functional I/O Module
Screw Terminal/ Cable Assembly	Provides screw terminal connection for one word. Connects to signal-conditioning module.	BC40C-4		Signal-Conditioning Module
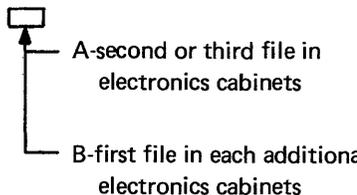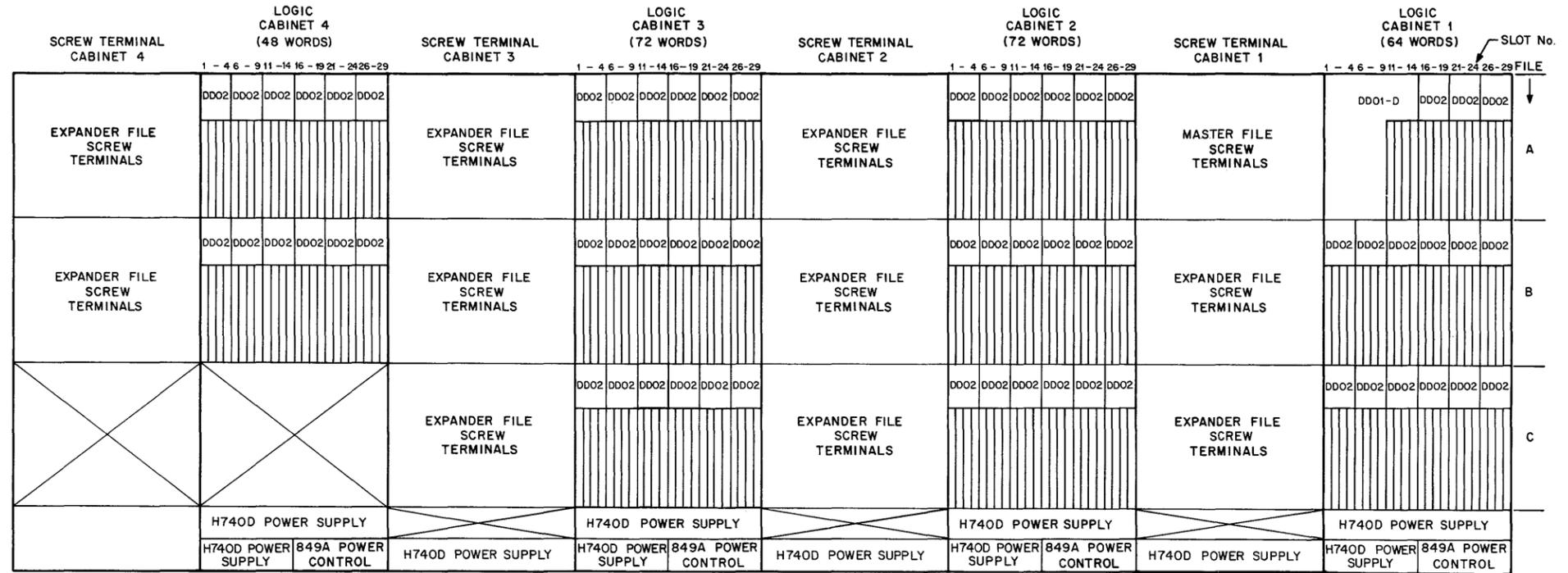
Figure 1-2 UDC8 Maximum Configuration Diagram

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1.4.3.1 849A Power Control Panel — The power control panel located in the front of the logic cabinet controls the application and removal of system primary power. The power control contains a LOCAL/REMOTE switch, a power ON indicator, a primary power contactor, and a circuit breaker. When the LOCAL/REMOTE switch is placed in REMOTE, application and removal of primary power can be controlled from the computer. For the LOCAL position, primary power is controlled by using the front panel 30A circuit breaker.

1.4.3.2 H740D Power Supply — The H740D Power Supplies are located as shown in Figure 1-2. They produce regulated +5V (20A) and –15V potentials for the file logic circuits and I/O modules. The +5V and power ground outputs are made available at an output connector on the rear of the supply. These outputs are routed to each of the files by separate wire runs. Ground and +5V are connected from file unit to file unit, using jumpers on the rear of the G729 Modules. The –15V potential is used only for level conversions involved with a negative I/O bus interface, and is therefore routed only to the master file. The supply contains a 15A fuse for +5V, and a 5A fuse for –15V.

1.4.4 UDC8-N or -P Master File

The master file contains one DD01 Master Control, space for up to three DD02 File Units, power supply harness, I/O bus cables, and bus terminators.

1.4.4.1 Master Control DD01 — The DD01 Master Control (Figure 1-3) occupies three file unit slots in a UDC8 Master File, and offers four insertion slots for functional modules. Only one master control is required for full utilization of the UDC8. Two types of master controls are available. One type is required to interface with the PDP-8 family of computers having a positive I/O bus, and another for the PDP-8 family of computers having a negative bus. The only difference in the two types of master controls is the module complement as listed in Table 1-2.

1.4.4.2 File Unit DD02 — The DD02 File Unit occupies one of six available locations in a file and contains four slots for functional modules. Although 63 file units are required for full utilization of the UDC8, any number of file units (up to 63) can be serviced by one master control. The module complement of the DD02 is listed in Table 1-3. The DD02 is an expander assembly which contains 24 slots arranged in four vertical rows of six slots. The upper two slots in each row constitute an extension of the UDC bus. The lower four slots in each row constitute a unique address within the address field, into which any of the functional modules may be inserted. The M851 Address Decoder and G729 Address Jumper Module occupy the second pair of slots in the bus section (AB2) and serve the four I/O slots below.

1.4.5 UDC8 Expander File

The expander file is a housing which contains a DD02 File Unit and may contain up to five additional DD02 File Units, a BC41A Bus Extender, and one M935 Bus Connector per DD02.

1.4.6 Functional Modules and Signal-Conditioning Modules

There are several types of functional modules available for the UDC8. Some serve as input modules for receiving sensory or control data from customer devices; others perform output functions for controlling customer devices. A detailed description, a simplified schematic, and a photograph of each module currently available are provided in Chapter 4. The functional modules are plugged into slots provided by the master file, expander files, and DD02 File Units (Figure 1-4). Each functional module requires a signal-conditioning module for normalizing input voltages, fusing, arc suppression, and for connection to field wiring. These modules are also described in Chapter 4. The 12 data bits and field power connections on the signal-conditioning module are brought to the screw-terminal cabinet via a cable consisting of 18 twisted pairs.

Figure 1-3 — DD01 and DD02 Configuration Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	M903	M903	M903	G772		M113	M112	M624	M623		M942	M851 G729		M935
B				*		*	M510	M510	M510			**		***
C	*	M169	M169	M169		*	M302	M206	M206		Four Functional Module Slots			
D	*	M111	M111	M115		M115	M113	M112	M206					
E	M206	M112	M113	M602		M111	M302	M307	M401					
F	M206	M112	M112	M602		M304	M401	M401						

	1	2	3	4
A	M935	M851 G729		M935
B	***	**		***
C	M935	Four Functional Module Slots		

*Modules in these slots are as follows

Positive Bus DD01 (P)

B4   - M101
B6 and C6 - M103
C1 and D1 - M623

Negative Bus DD01 (N)

B4   - M100
B6 and C6 - M102
C1 and D1 - M633

**Module G729 plugs into rear of Module M851.

***Flat Mylar Cable BC41A-5 is used to intercon-
nect files within a cabinet from slot AB4 of the
last DD02 of a file to slot AB1 of the first DD02 of
the next file. A BC41A-10 Cable is required
when extending the UDC bus to the first DD02
in a new cabinet. Module M942 plugs into slot
AB4 of the last DD02.

Figure 1-3   DD01 and DD02 Configuration Diagram

Table 1-2
DD01 Module Complement

UDC8-N Negative Bus	UDC8-P Positive Bus	Name	Quantity	Location
M100	M101	Bus Data Interface	1	B4
M102	M103	Device Selector	2	B6 and C6
M111	M111	Inverters	3	D2, D3, and E6
M112	M112	NOR Gates	5	A7, D8, E2, F2, and F3
M113	M113	NAND Gates	3	A6, D7, and E3
M115	M115	NAND Gates	2	D4 and D6
M169	M169	Gating Module	3	C2, C3, and C4
M206	M206	General-Purpose Flip-Flops	5	C8, C9, D9, E1, F1, and F4
M302	M302	Dual Delay Multivibrator	3	C7, E7
M304	M304	Pulse Shaper	1	F6
M307	M307	Dual Integrating One-Shot	1	E8
M401	M401	Variable Clock	3	E9, F7, and F8
M510	M510	I/O Bus Receiver	3	B7, B8, and B9
M602	M602	Pulse Amplifier	2	E4 and F1
M633	M633	Bus Driver	2	C1 and D1
M623	M623	Bus Driver	1	A9
M624	M624	Bus Driver	1	A8
M851	M851	Address Decoder/Bus Receiver	1	AB12
M903	M903	Flat Mylar Connector	3	AB1, AB2, and AB3
M942	M942	Terminator Module	2	AB11 and AB14
G729	G729	Address Jumper Module	1	AB12 (Piggy-back on M851)
G772	G772	Power Connector	1	A4

Table 1-3
DD02 Module Complement

Type/Part No.	Name	Quantity	Location
M935	UDC Bus Extender	1	AB1*
M851	Address Decoder/Bus Receiver	1	AB2
G729	Address Jumper Module	1	AB2 (Piggy-back on M851)

*See Paragraph 4.3.2 for bus extension details.

1.4.7 Screw Terminal Cable Assembly BC40C

Field wiring is connected to screw terminal assemblies (BC40C-4) which make the necessary connections between the signal-conditioning modules and the field-wiring terminations. Each BC40C Assembly makes connections available through 16 of the 18 twisted pairs for control wiring. The two remaining pairs provide paralleled conductors for bringing in external excitation power when using common power signal conditioning. Only 12 control pairs are used with UDC8 Functional Modules. Each circuit is completed through a twisted pair of No. 26 AWG stranded color-coded wires connected to a pair of screw terminals. The terminals will accommodate No. 14 AWG wire, and are arranged in two strips of 17 terminals, each supported in line by a common steel angle support.

ADDRESS
JUMPER CARD
G729

MASTER
CONTROL
DDO1

SIGNAL
CONDITIONING
MODULE

SCREW TERMINAL
ASSEMBLY BC40C

FUNCTIONAL I/O
MODULE
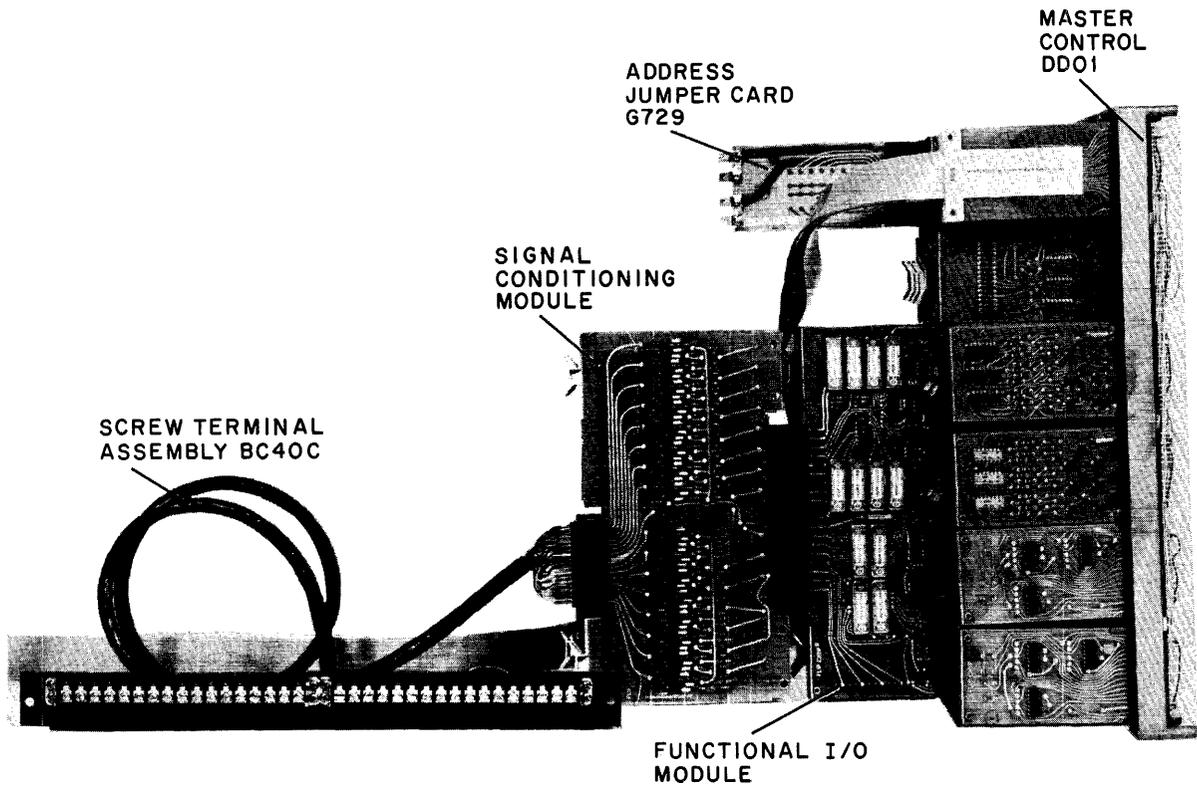
Figure 1-4   UDC8 Assembly Details

1.5 SPECIFICATIONS

1.5.1 General

Operating temperature:	0° to 50°C
Humidity:	Up to 95% without condensation
Cooling and filtering:	Dust filters and blower fans in each logic cabinet with bottom exhaust
Input cabling:	Top or bottom entry to supplied screw terminals. Screw terminals will accommodate No. 14 AWG wires. However, customer wiring should be limited to No. 18 AWG (max) 2-wire twisted pair per digital point for a fully-wired cabinet (72 words).

Cabinet dimensions:	Single Cabinet	Dual Cabinet
Height:		
Bottom entry:	72 in.	72 in.
Top entry:	75 in.	75 in.
Width:	21 in.	42 in.
Depth:	30 in.	30 in.

Power:	115/230V, 50 to 60 Hz, single-phase, 500 VA (max) for logic. Possible additional 700W for 48V field excitation in 72 12-bit words of signal conditioning.
Heat dissipation:	1800 Btu/hr for logic power. Possible additional 2500 Btu/hr for 72 12-bit words of signal conditioning.

1.5.2 System Performance

Modes of operation:	a. Programmed digital output b. Programmed analog output c. Programmed digital input d. Interrupt controlled input e. Interrupt controlled counting function
Data Format:	(Paragraph 2.4)
Number of digital inputs and outputs:	256 12-bit words (3072 digital points) maximum
Type of input and output:	See functional modules described in Chapter 4
Input and output word (module) selection:	Directly addressable
Interrupt module identification:	4-bit module generic code and an 8-bit address
Interrupt scan:	Locates address and module type in a minimum of 5 μs (20 μs worst case)
I/O data rate:	1×10^5 12-bit words/sec
Computer interface:	Direct interface to positive or negative bus PDP-8 Computers
System clock rates:	Three clocks are available to each I/O word: a. 0.63V rms at line frequency b. 175 Hz — 1.75 kHz adjustable c. 1.75 kHz — 17.5 kHz adjustable

For functional and signal-conditioning module specifications, see Chapter 4.

For controller module replacement schematics, see Volume II.

1.6 REFERENCE DOCUMENTS

The following documents are essential in gaining an understanding of the PDP-8 Computer System:

Small Computer Reference Manual
PDP-8 Maintenance Manual
PDP-8 User Guide

The following diagnostic program is essential in establishing the performance of the UDC8 subsystem:

UDC8 System Function Exerciser   UDC-8EX (MainDEC-08-D8YB-D)

CHAPTER 2
PROGRAMMING

2.1 IOT FORMAT AND INSTRUCTIONS

The UDC8 responds to eleven unique IOT instructions employing device select codes 35_8 and 36_8. These eleven instructions, along with other computer instructions, are used to develop the program for controlling the operation of the UDC8. The IOT instruction format is illustrated by Figure 2-1; each instruction is listed and described in Table 2-1.

Figure 2-1   IOT Format

Table 2-1

UDC8 Instruction Set

Mnemonic	Instruction Code (Octal)	Operation
UDSF	6361	Skip on UDC Flag and Clear Flag — If the UDC flag is set this instruction will generate a skip pulse, causing the computer to skip the next instruction and clear the UDC flag.
UDEI	6364	Enable UDC Interrupt Flag
UDDI	6365	Disable UDC Interrupt Flag
UDLA	6363	Load Address — An 8-bit address (AC 04 through 11) is loaded into the address/scanner register of the UDC8 for accessing a specific module, after which accumulator is cleared.

Table 2-1 (Cont)
UDC8 Instruction Set

Mnemonic	Instruction Code (Octal)	Operation
UDRD	6366	Read Data — Clears the accumulator and reads data from whichever module has its address stored in the address/scanner register.
UDLD	6367	Load Data — Loads contents of accumulator into whichever module has its address stored in the UDC address/scanner register, after which accumulator is cleared.
UDSS	6351	Skip On Scan Not Busy — This instruction will cause the computer to skip the next instruction when the scanner register has located the interrupting module (used only after 6353).
UDSC	6353	Start Address Scan — Initiates address scan and clears accumulator. Bit 10 enables scan for immediate interrupts; bit 11 enables scan for deferred interrupts.
UDRA	6356	Read Address and Generic Type — The accumulator is cleared. The contents of the address scanner register and the module type code (generic) of the module in that address are loaded into the accumulator as a 12-bit word.
UDLS	6357	Load Previous Status and Read Change of State (COS) Gates — This instruction loads the contents of the accumulator (previous status of the interrupting module) into the COS register of the UDC, clears the accumulator, and reads the exclusive OR function of the COS gates into the accumulator.
UDRS	6355	Read UDC Status — Read UDC status (immediate AC bit 10, or deferred AC bit 11).

2.2 ADDRESS FORMAT AND GENERIC CODE

The address/scanner register in the UDC serves a dual purpose. It serves as a buffer register when the UDC is directly addressed by the computer, and as a scanner register upon command to find the address of an interrupting module. The address format and the bit values of the address in the accumulator and the scanner/register are illustrated in Figure 2-2. The generic codes, used only to identify which type of module generated an interrupt, are listed and defined in Table 2-2. These codes may be used in directing the program to jump to unique servicing routines.

2.3 INTERRUPT STRUCTURE

The interrupt structure of the UDC can be enabled or disabled under program control. If enabled and a module issues an interrupt, the interrupt structure can be interrogated under program control to determine whether the module requires immediate service or whether services can be deferred. When interrogated, the UDC issues a

status word. The status word format is illustrated in Figure 2-3. Subject to the result of the interrogation, the automatic scan may be started to search selectively for the address of the deferred or the immediate interrupt module. In multiple interrupts, the lowest channel address is always found.
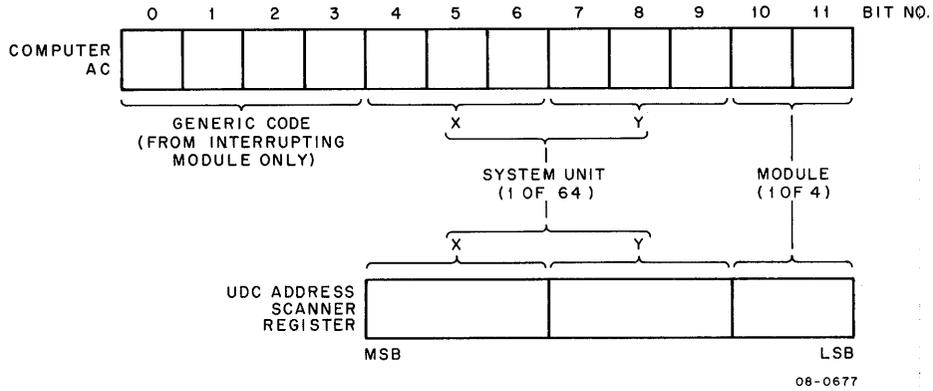
Figure 2-2 Address Format

Table 2-2

UDC8 Generic Codes

Generic Code	Type of Module
0000	No interrupts present
0001	Fault condition
0010	Contact interrupt W733
0011	Contact interrupt W743
0100	I/O counter W734
0101	I/O counter W734
0110	I/O counter W734
0111	I/O counter W734

BIT 10	BIT 11	TYPE OF INTERRUPT
0	0	NO INTERRUPT
0	1	DEFERRED INTERRUPT
1	0	IMMEDIATE INTERRUPT
1	1	DEFERRED AND IMMEDIATE INTERRUPT

08-0676
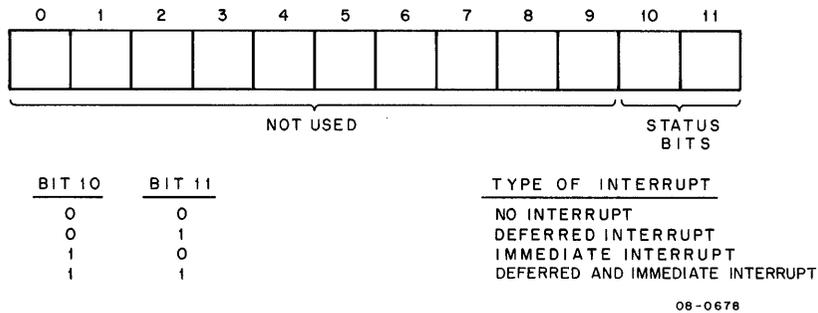
Figure 2-3 Status and Control Word Format

The search is selective because the processor issues a control word when the scan is started to enable one or both types of interrupt modules for the search. The format of the control word is identical to the status word. After locating and servicing an interrupt, it must be determined that no further interrupts await servicing. This may be done either by reading UDC status (6355), or by issuing another start scan (6353) instruction. A return of generic code 0000 indicates no further interrupts are set.

2.4 DATA FORMAT

The data transferred between the computer and the UDC modules is an unstructured 12-bit word. The 12 bits may be unrelated, as in the case of driving or sensing individual digital points, or may represent a 12-bit number for presetting or reading a counter or a 2-bit channel code and a 10-bit number for driving a digital-to-analog converter. Bit 0 on the module corresponds to bit 0 in the accumulator.

2.5 APPLICATION PROGRAMS

Application programs for the UDC8 will vary from one application to the next. However, to provide some insight into the use of the UDC IOT instructions, a flow chart presenting some operational characteristics of the UDC relative to the IOTs is presented in Figure 2-4.

2.6 SAMPLE PROGRAMS

Program No. 1

This sample routine reads the contents of the switch register, then outputs the information to the selected address.

```
BEGIN,    200    7300    CLA,CLL
          201    1211    TAD ADDRESS
          202    6363    UDLA            /LOAD ADDRESS TO UDC
          203    7604    LAS
          204    6367    UDLD            /OUTPUT DATA TO SELECTED
          205    2210    ISZ   DELAY     /ADDRESS THEN
          206    5205    JMP   .-1       /DELAY FOR TIME SPECIFIED
          207    5200    JMP   BEGIN
          210    0000    DELAY, 0000
          211    0000    ADDRESS,0000    /DEPOSIT ADDRESS IN THIS LOCATION
```

Program No. 2

This sample program selects the address, then reads the data into the AC register from the input module.

```
BEGIN     200    7300    CLA,CLL
          201    1207    TAD ADDRESS
          202    6363    UDLA            /LOAD ADDRESS
          203    6366    UDRD            /THEN READ DATA IN
          204    2210    ISZ             /AND DELAY FOR TIME
          205    5204    JMP .-1         /SPECIFIED
          206    5200    JMP BEGIN
          207    0000    ADDRESS,0000    /DEPOSIT ADDRESS IN THIS LOCATION
          210    0000    DELAY,0000
```

INTERRUPT

IS IT THE UDC IOT 6361 ? — NO → TEST OTHER DEVICES ON THE INTERRUPT BUS

YES

READ UDC STATUS IOT 6355

IMMEDIATE OR DEFERRED ? — DEFERRED → SET SOFTWARE INTERRUPT FLAG AND RETURN TO MAIN PROGRAM

IMMEDIATE

START ADDRESS SCAN (BIT 10 = "1") IOT 6353

UDC NOT BUSY IOT 6351 ? — NO

YES

READ ADDRESS GENERIC TYPE IOT 6356

GENERIC TYPE 0000 ? — YES → ENABLE UDC INTERRUPT FLAG IOT 6364 → EXIT

NO

CONTACT INTERRUPT ? — NO → TAKE APPROPRIATE ACTION BASED ON GENERIC TYPE OF INTERRUPTING MODULE

YES

READ AND STORE CURRENT STATUS OF INTERRUPTING MODULE IOT 6366

A   B

A   B

LOAD PREVIOUS STATUS & READ CHANGE OF STATE GATES IOT 6357

ANY BITS CHANGE STATE IN THE SPECIFIED DIRECTION ? — NO

YES

TAKE APPROPRIATE ACTION BASED ON WHICH BIT CHANGED STATE

UPDATE PREVIOUS STATUS OF INTERRUPTING MODULE WITH STORED CURRENT STATUS

08-0679

Figure 2-4   General Application Program, Flow Chart

2-5

Program No. 3

This sample program is a routine to handle interrupts coming from Contact Interrupt (W732) Modules. First the interrupt circuitry is enabled, then, when an interrupt occurs, the scanner is activated to find the address of the interrupting module. When the address is found, it and the generic code are read, the COS is determined, and the data are read in. After each HALT check the data, then press CONTINUE.

```
BEGIN  200  7300  CLA,CLL
       201  6364  UDEI                      /ENABLE THE INTERRUPT CIRCUIT
       202  6361  UDSF                      /AND SKIP ON INTERRUPT FLAG
       203  5203  JMP .-1                   /JUMP BACK AND SENSE FLAG AGAIN
       204  6355  UDRS                      /READ UDC STATUS AND
       205  6353  UDSC                      /START UDC SCANNER
       206  6351  UDSS                      /SKIP ON FLAG NOT BUSY
       207  5206  JMP .-1                   /JUMP BACK AND SENSE FLAG AGAIN
       210  6356  UDRA                      /READ THE ADDRESS AND GENERIC
                                            /CODE
       211  1220  TAD PREVIOUS STATUS
       212  6357  UDLS                      /LOAD PREVIOUS STATUS THEN READ
       213  7402  HLT                       /COS AND HALT TO CHECK THE DATA.
                                            /DEPRESS CONTINUE
       214  6366  UDRD                      /READ THE DATA IN AND
       215  7402  HLT                       /HALT TO CHECK IT. DEPRESS
                                            /CONTINUE
       216  3220  DCA PREVIOUS STATUS
       217  5200  JMP BEGIN
       220  0000  PREVIOUS STATUS, 0000
```

CHAPTER 3
PRINCIPLES OF OPERATION

3.1 GENERAL

The UDC8 is capable of handling several digital control functions. These functions are to sense data, dispatch data, respond to interrupts, and determine change-of-state. Each type of functional module is uniquely associated with one or more of these functions. Therefore, depending on the types of modules used at an installation, some or all of the UDC functions may be employed. Descriptions of the functional modules are presented in Chapter 4. Block and simplified diagrams are included in this chapter and the detailed block schematics are included in Volume II of this manual; see drawings D-BS-DD01-0-01 through D-BS-DD01-0-10.

3.2 BLOCK DIAGRAM ANALYSIS

A detailed block diagram of the UDC8, showing the interface controller, one address selector, and one functional module, is shown in Figure 3-1. The device selector and IOT decoder of the interface controller coordinates all activities within the UDC8, in response to the IOT instructions from the memory buffer of the computer. IOT instructions are available for enabling, disabling, and interrogating the interrupt logic, for data and address gating, and for starting the address scanner.

All module address and data transfers are executed by IOTs and are dispatched to or from the accumulator, via the data and address gating circuits in the interface controller. To sense data at an input module, the computer must issue an IOT to transfer the module address from the accumulator to the address register. This uniquely enables the address logic on one functional module. Another IOT must then be issued by the computer to transfer the data from the input module, through the data and address gating circuits, to the accumulator. To send data to an output module, the module must first be addressed as described above. A second IOT is then issued to transfer the data from the accumulator through the data and address gating circuits to the output module. Those modules that are equipped with the interrupt facility are all monitored by the interrupt logic in the interface controller, which in turn supplies the interrupt request to the computer. Each module contains jumpers which can be initially set up to issue an immediate or a deferred interrupt.

The computer, having determined that the UDC8 has generated an interrupt, will respond to the interrupt request by issuing an IOT to read the UDC status. This IOT causes the UDC status word to be transferred to the accumulator. The contents of the status word will then cause the computer to defer service or to start the address search. The address search is initiated by loading the desired control word into the accumulator and issuing an IOT to start the address scanner. The control word is transferred to the UDC when the IOT is issued, to determine which of the modules are to be included in the search. When the scanner reaches the address of the interrupting module, the scanner is stopped. The module generic code and change-of-state signals, along with the address from the scanner, are applied to the data and address gating circuits in the interface controller. The generic code and address are transferred to the accumulator via the data and address gating circuits by issuing an IOT.
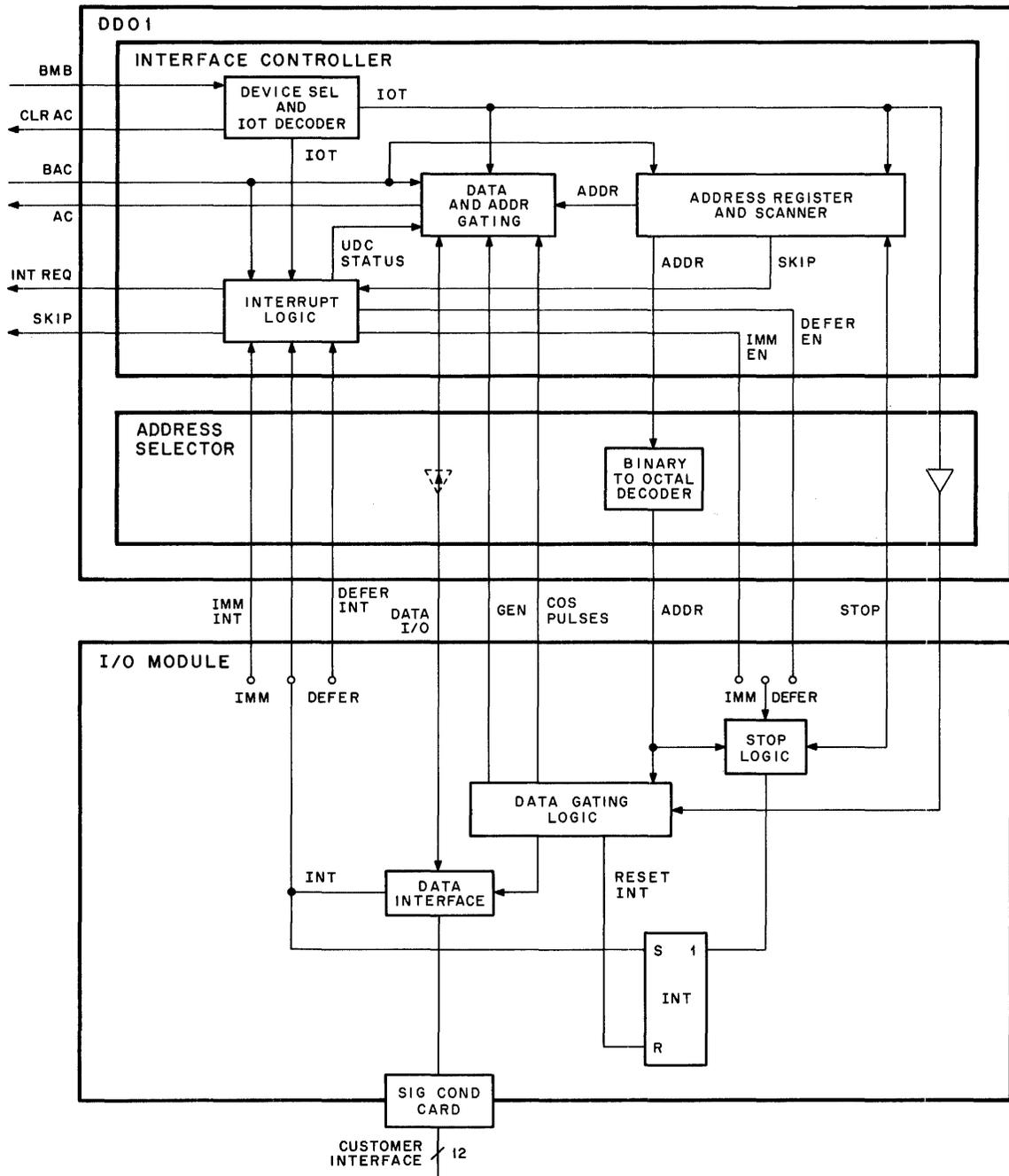
Figure 3-1   UDC8 Detailed Block Diagram

Depending on the type and application of the functional I/O module, the computer program continues in one of three directions by programming different IOTs.

    a.   Data could be read from an input module.

    b.   Data could be loaded into an output module.

    c.   The bit that changed state could be determined.

3.3 DETAILED CIRCUIT ANALYSIS

3.3.1 General

A logic diagram of the UDC8, showing the master file (DD01) and one functional module, is presented in Figure 3-2. Sheet 1 illustrates the device selector and IOT decoder, and the address and data gating circuits; Sheet 2 illustrates the interrupt logic and the address scanning circuits.

3.3.2 Device Selector and IOT Decoder

The device selector and IOT decoder of the UDC8 responds to device select codes 35_8 and 36_8. Five IOT instructions are coded with device code 35_8 and six IOT instructions are coded with device code 36_8, providing a total of eleven instructions for controlling and communicating with the UDC8. The IOT instructions are listed and described in Table 2-1 of Chapter 2. Figure 3-3 correlates the IOT instruction format, decode logic, mnemonics, IOT code, and execution time. For basic IOT decoding information, refer to DEC's *Small Computer Handbook.*

3.3.3 Addressing

A detailed block diagram of the address and scanning circuits is shown in Figure 3-4. Shown are one output module, two input modules, and one interrupt module connected to one address decoder.

An address decoder (M851) is associated with each group of four functional I/O module slots; therefore, there is an address decoder associated with the DD01 and each DD02 in the system.

All functional modules in a UDC8 can be addressed sequentially or at random, depending on the user program. In either case, the Load Address IOT is issued to clear the UDC address/scanner register and load it with the address from the computer accumulator. Once the address appears in the address/scanner register, one of the 64 address decoders (maximum configuration) recognizes the address. The binary-to-octal decoders on the M851 Module decode bits 4 through 9 of the module address and cause one X and one Y output to be asserted. If the decoded X and Y bits correspond to the location of X and Y jumpers on the G729 Module, that file unit is enabled. At the same time, one of the four outputs from the 2-bit decoder in the address decoder (WD 00, 01, 02 or 03) becomes decoded as a function of bits 10 and 11 of the module address to enable one of the four modules that are inserted in that file unit. When addressed, data can be loaded into an output module or read out of an input module, using the Load Data or Read Data IOT instructions.

The interrupt feature of the UDC8 permits the use of modules that are equipped to issue an immediate or a deferred interrupt signal. While the basic input and output modules serve only as direct data interfaces, the interrupt modules provide the interface for inputs which require fast response time. An interrupt command from a functional module will be acknowledged either immediately or at some later time, depending on the type of interrupt that is issued and the nature of the user program. In either case, the address of an interrupting module must be found in order to service the module. This is accomplished by employing the address scanner register in the interface controller as three binary counters that are capable of examining all 256 module addresses and stopping when the address of an interrupting module is located. The scanner is started under program control

CUSTOMER
INTERFACE

MODULE
INTERFACE

UDC
BUS

FUNCTIONAL I/O MODULE
(SEE NOTE 1)

ADDRESS SELECTOR

INTERFACE CONTROLLER

NOTE:

1. Individual modules are limited to input or output functions, but not both.
Module circuits shown on this diagram do not reflect a specific module;
collectively, the circuits shown, illustrate maximum interface and
module capability.

START — B START — PWR CLR

R1F — B RIF — C RIF — DELAY 1.0 μSEC — 6356 READ GEN AND ADDR

SYST INT — B SYST INT — (SEE SHEET 2)

INT

INPUT BUS — SIG COND BOARD — INTERFACE CIRCUIT

POWER

DATA I — B DATA I — C DATA I — READ DATA I 6366

C DATA I

6356 READ GEN AND ADDR
6357 READ COS GATES

P CL — B P CL — C P CL — COS CL

+3V

P OP — B P OP — C P OPN — COS OPN

6357 READ COS GATES — R COS

UDC STATUS 00 AND 01

C AC 00-11 — AC 00-11

GEN 00-03 — B GEN 00-03 — C GEN 00-03

+3V — FAULT

6356 READ GEN AND ADDR

CLK 00 — B CLK 00 — CLOCK 00

175Hz—17.5KHz

C ADDR 00-07 — 8-BIT ADDRESS REGISTER AND SCANNER — SCO 04-11 — 6363 LOAD ADDR

X, Y AND WD 00-03 — BIN TO OCTAL CONVERTER — B ADDR 00-07 — C ADDR 00-07

C CLK X, Y AND WD (SEE SHEET 2)

OPEN — SAC 00-11 — SEL EN — BAC 00-11

CLK 01 — B CLK 01 — CLOCK 01

1.75KHz—17.5KHz

(SEE SHEET 2) SAC 10 AND 11

CLK 60 — B CLK 60 — AC PWR 60Hz

DATA O 00-11 — B DATA O 00-11 — FF00-FF11

CLOSE — DATA O/PREV STATE FF — C L COS — 6357 LOAD PREV STATE
6363 LOAD DATA O

OUTPUT BUS — SIG COND BOARD — INTERFACE CKT

POWER

PWR CLR

LOAD — B LOAD — DELAY 1.5 μSEC — DELAY 1.0 μSEC

SKIP ON SCAN NOT BUSY — 6351 — IOT 1
START INT SCAN — 6353
READ UDC STATUS — 6355 — IOT DECODE LOGIC
READ GEN AND ADDR — 6356
LOAD PREV STATUS (IOT 1) — 6357
AND
READ COS GATES (IOT 4) — 6357 — IOT 4

IOT 2 35

OPT SELEC 35

SMB 09-11

IOT 2 36

SEL EN

SKIP ON UDC FL AND CLR FL — 6361 — IOT 1
LOAD ADDR — 6363
EN UDC INT FL — 6364 — IOT DECODE LOGIC
DIS UDC INT FL — 6365
READ DATA I — 6366
LOAD DATA O — 6367 — IOT 4

Figure 3-2 UDC8 Logic Diagram (Sheet 1 of 2)

CUSTOMER
INTERFACE

FUNCTIONAL I/O MODULE

MODULE
INTERFACE

ADDRESS SELECTOR

UDC
BUS

INTERFACE CONTROLLER

START
B START

PWR CLR

RIF
B RIF
C RIF
DELAY 1.0 μSEC
6356 READ GEN AND ADDR

LOAD
B LOAD
DELAY 1.5 μSEC
DELAY 1.0 μSEC
6367 LOAD DATA AND CLR AC

SYST INT
B SYST INT

CLK OO
B CLK OO
CLOCK OO
175Hz-1.75KHz

I/O BUS 12

SIG COND BOARD

12

INTERFACE CIRCUIT

POWER

S 1 INT R

IMM INT
B IMM INT
6355 READ UDC STATUS
UDC STATUS 01
SAC 10
SEE SHEET 2

DEF INT
B DEF INT
UDC STATUS OO
SAC 11

D 1 IMM EN C O

D 1 DEF EN C O

+3V
D 1 INT FLAG C

6364 ENABLE

6365 DISABLE

D 1 INT EN C

SKIP ON UDC FL AND CL FL 6

PWR CLR
PULSE SHAPER

IMM EN
B IMM EN

DEF EN
B DEF EN
1.75KHz-17.5KHz

CL OO, 01 AND 02
PULSE SHAPER
6353 START INT SCAN
6363 LOAD ADDR

CLK 01
B CLK 01
CLOCK 01

CLK 6O
B CLK 6O
AC PWR 60Hz

PULSE SHAPER

X,Y AND WD 00-03
6
BIN TO OCTAL CONVERTER
B ADDR 00-07
8
8-BIT ADDR REGISTER AND COUNTER
SAC 04-11 (SEE SHEET 1)

+3V

GEN 00-03
B GEN 00-03
4

BUSY FLAG
D 1 C

SKIP ON SCAN NOT BUSY 6351

P OP
B P OP
(SEE SHEET 1)

RESET BUSY FLAG

P CL
B P CL

C CLOCK X, Y AND WD
3

STOP X,Y WD
B STOP X,Y WD
3
C STOP X, Y AND WD

+3V

FAULT
DELAY 2.0 μSEC
ADJUSTABLE CLOCK 175-1750KHz
DELAY 1.5 μSEC

Figure 3-2 UDC8 Logic Diagram (Sheet 2 of 2)

3-7

by issuing the Start Interrupt Scan IOT activating the scanner clock. Before issuing this IOT, bit 10 (immediate) and/or bit 11 (deferred) must be set in the accumulator. These bits determine the type of interrupt being scanned by setting the immediate and/or deferred enable flip-flops. The output of these flip-flops is utilized to enable the appropriate interrupt modules. Each counter (X,Y, and WD) is sequentially clocked until the associated stop commands are issued by the stop logic on an interrupting module. Each interrupt module has its own stop logic, which is enabled when the module has issued an interrupt. If more than one interrupt is present, the module having the lowest address will be located. Therefore, those modules having highest priority should be assigned the lowest module addresses.

First, the X register, with a maximum count of 7, localizes the interrupting module to eight file units having the same X address. The counter stops when it reaches the lowest X address of an interrupting module. Then the Y counter, which also has a maximum count of 7, further localizes the module to the one system file unit containing the interrupting module. Finally, the word counter locates which of the four module slots in that file unit contains the interrupting module. The maximum number of counts required to find an interrupting module in a maximum system configuration is 17 (7 + 7 + 3). Each count requires approximately 1 μs.
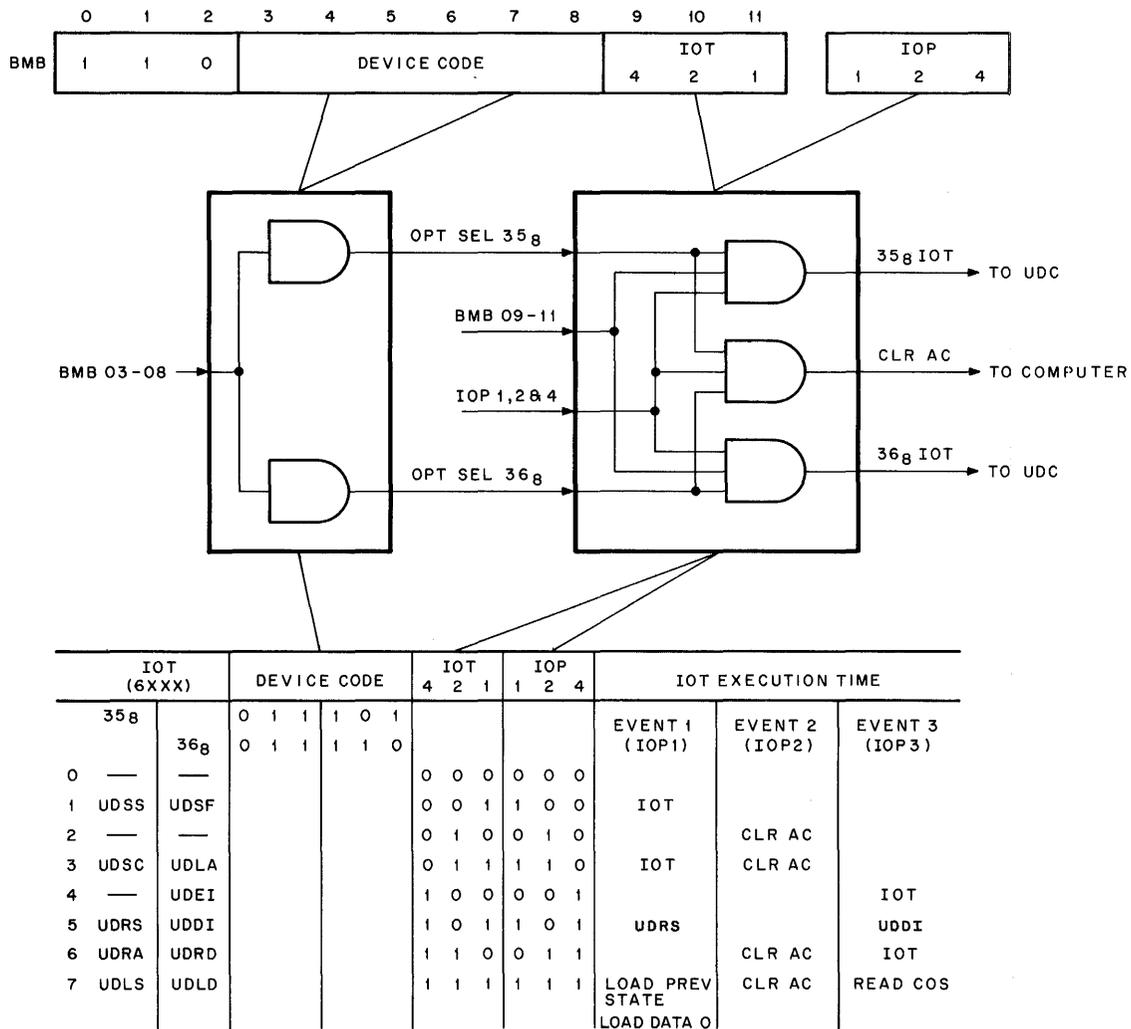
08-0682

Figure 3-3   IOT Decoder and Truth Table

3-9
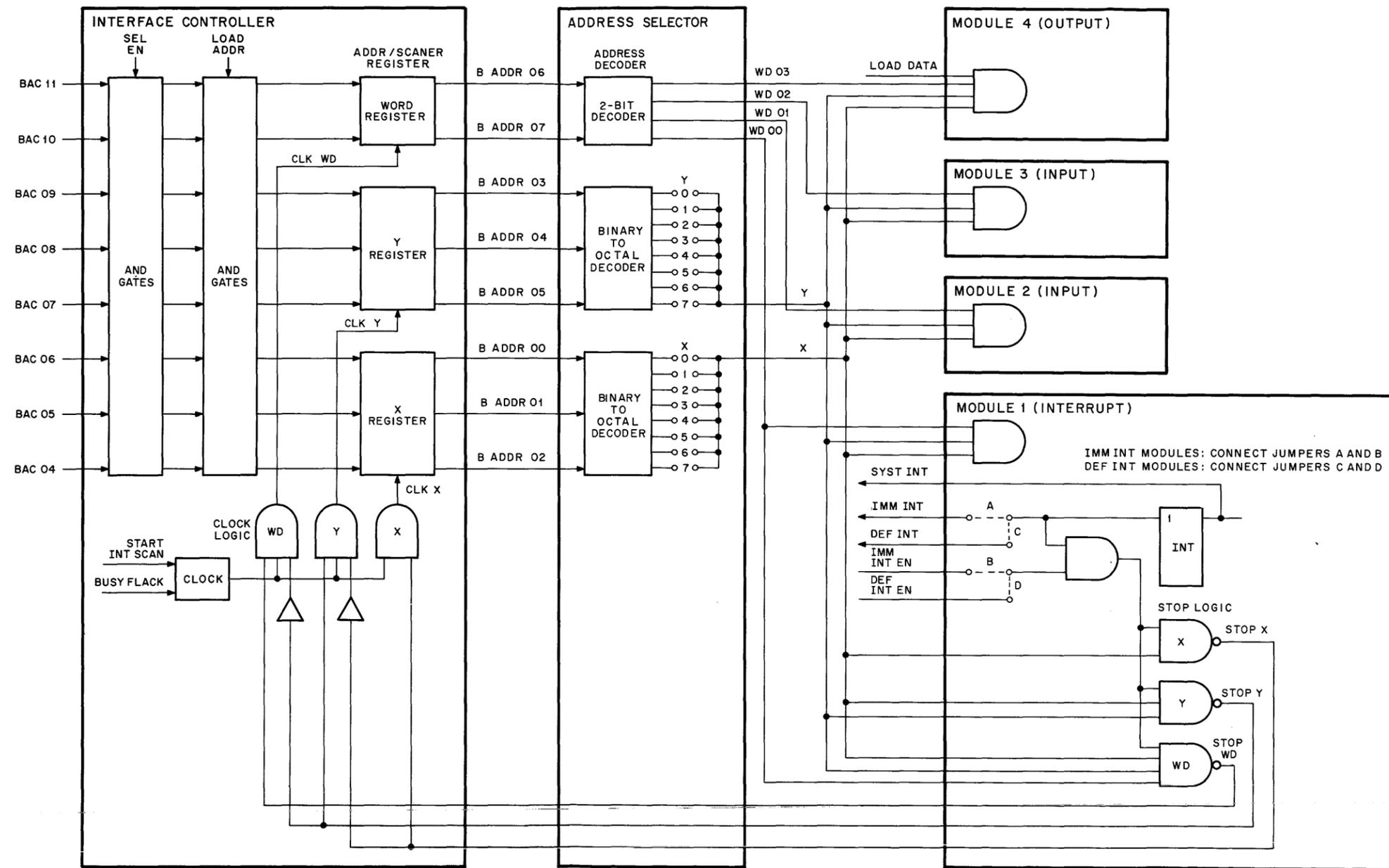
Figure 3-4 Address Scanner Logic

08-0683

After the address of an interrupting module is found by the scanner, the busy flag is reset to notify the computer that the address and the module generic code can now be gated to the computer by issuing the Read Address and Generic Type IOT.

3.3.4 Interrupt and Skip Logic

Interrupt requests and skip commands produced in the UDC8 are used by the computer to jump between main programs and subroutines for finding and servicing the interrupt. The interrupt logic can be enabled and disabled by issuing the Enable UDC Interrupt Flag and Disable UDC Interrupt Flag IOT instructions. The proper management of these instructions is the responsibility of the programmer. The interrupt logic may be disabled while the UDC is being serviced; thus, a subsequent interrupt request does not interfere with the servicing subroutine. After the UDC is serviced, the interrupt logic should again be enabled. All interrupt modules are connected to the interrupt logic. In addition, each module will also send an immediate or a deferred interrupt command to logic gating circuits in the interface controller. A jumper wire must be installed in the module to have it issue one and only one of the two signals. After an interrupt request is issued by the UDC, the computer, under program control, jumps into a subroutine to search for the device issuing the request. If a UDC module issued an interrupt, a skip command is sent to the computer when the Skip on UDC Flag and Clear Flag IOT instruction is issued, thus allowing the computer to jump into a servicing routine to determine what type of interrupt occurred. This skip command also clears the interrupt flag. If the Read UDC Status IOT reveals that an immediate interrupt occurred, the computer will jump into another routine to service the interrupt. A deferred interrupt would allow the computer either to jump to a routine to service the interrupt, or to a routine designed to store the deferred interrupt and continue the main program. The deferred interrupt can then be serviced when computer time is not critical.

Servicing a UDC interrupt request involves finding the address and generic type of the interrupting module, determining which data inputs have changed state in the direction specified by the jumpers on the module, and gating data out of or into the module. An immediate interrupt request is serviced by depositing a control word into the accumulator and issuing the Start Interrupt Scan IOT instruction. The control word for servicing the immediate interrupt request has bit position 10 set and bit position 11 reset to enable the stop logic of only those modules that are set up to issue an immediate interrupt. When the Start Interrupt Scan IOT instruction is issued, the control word appearing in the accumulator will be gated into the UDC by the select enable signal, and will cause the IMM EN and BUSY flip-flops to be set. Setting the IMM EN flip-flop enables the stop scan logic of all the modules that could issue an immediate interrupt. The modules that are set up to issue a deferred interrupt are enabled in the same way, except that a different control word (bit position 10 is reset and bit position 11 is set) is deposited in the accumulator. The next IOT instruction in the servicing routine will be the Skip on Scan Not Busy instruction, which enables logic in the UDC to generate a skip command when the busy flag is reset upon termination of the address scan. The module address and generic code are gated out of the UDC to the accumulator by issuing the Read Address and Generic Type IOT instruction when the scan terminates. This IOT also resets the interrupt flip-flop on the addressed module. The generic code and address are used in the computer to locate in memory the previous status of the interrupting word, which is used in determining the change-of-state information.

3.3.5 Data Gating

The data-gating logic is shown on Sheet 1 of Figure 3-2. Data is gated into or out of a functional module by depositing the module address into the accumulator and issuing the Load Address IOT instruction, and then reading or loading the data by issuing the corresponding IOT instruction. To load data into an output module, the data to be loaded must be deposited in the accumulator before issuing the IOT. The Read Data IOT instruction will clear the accumulator before loading it with the input data. The Load Data IOT will clear the accumulator after transferring the data to the functional module.

3-13

3.3.6 Determining Change-of-State (COS)

The hardware gating network for determining the direction of change (open or close) of inputs to contact interrupt functional modules is illustrated on Figure 3-5. The gating network consists of two circuits used to determine the direction of an input change (1 to 0 defined as an opening and 0 to 1 defined as a closure) by comparing the previous status of the addressed module with its current status. Referring to Figure 3-5, gates A and D are used to test for an input closure, and gates B and C are used to test for an input opening. The jumper installed on the module determines whether a closure or an opening, or both, is of interest to the user. It does this by means of enabling either one or both of the circuits. Issuing the Load Previous Status And Read COS Gates IOT (6357) will transfer the previous status of the addressed module from the accumulator into the UDC controller, clear the accumulator and load the accumulator with a 1 corresponding to each bit that has changed in the direction of interest. Only one IOT instruction, Load Previous Status And Read COS Gates, is required to execute this function.

Jumpers A and B (Figure 3-5) in the interrupt modules must be connected as required by the user upon system installation (refer to Chapter 4). A truth table illustrating the output of the change-of-state gates with various combinations of previous status, current data, and jumpers is presented in Table 3-1.

3.3.7 Initializing

On power up, an initializing signal is generated on a dedicated bus line which is applied to the reset input of every flip-flop on every I/O module. The signal is the result of ORing the output of an integrating-one-shot (M307) set for 75 ms and B INITIALIZE from the PDP-8/I or 8/L. The resulting signal starts approximately 5 ms after power is turned on and lasts for approximately 250 ms.

Table 3-1
COS Definition Table

DATAI Changed From Previous State	DATAI	Previous State	Pulse Open (Jumper A)	Pulse Close (Jumper B)	COS Out (Exclusive OR)
Unchanged	0	0	0	0	0
	0	0	0	1	0
	0	0	1	0	0
	0	0	1	1	0
Opened (1 to 0)	0	1	0	0	0
	0	1	0	1	0
	0	1	1	0	1
	0	1	1	1	1
Closed (0 to 1)	1	0	0	0	0
	1	0	0	1	1
	1	0	1	0	0
	1	0	1	1	1
Unchanged	1	1	0	0	0
	1	1	0	1	0
	1	1	1	0	0
	1	1	1	1	0

MODULE

DATA I

X
Y
WD

A
+3V

P CL

P OP

DATA I

ADDRESS SELECTOR

ADDRESS DECODER

B ADDR. OO-O7
8

INTERFACE CONTROLLER

ADDRESS SCANNER/REGISTER

STOP SCAN   CLOCK   START SCAN

MODULE

DATA I

X
Y
WD1
WD 2

B
+3V

P CL

P OP

ADDRESS SELECTOR

ADDRESS DECODER

B P CL

B P OP

READ CLOSED COS

READ COS GATES

READ OPENED COS

A

B

E

READ COS GATES
12
COS

12

AC OO-11

MODULE

DATA I

A
B
+3V

DATA I
12

ADDRESS SELECTOR

B DATA I OO-11   12

PREV STATE
12

OPEN   C

DATA I
DATA I

CLOSED   D   PREV STATE
12

PREV STATE FF (12)

1   D

O   C

SELEN
12

BAC OO-11

LOAD PREV STATE
LOAD DATA O

08-0684

Figure 3-5 COS Logic

CHAPTER 4
INSTALLATION

This chapter contains necessary installation information for UDC Systems. The chapter covers the following subjects:

- Site Preparation
- Power Requirements, AC, Fusing, Receptacles
- Installation Checkout, DEC Field Service
- UDC System Configuration, Addressing, I/O Module Placement
- Functional I/O Module Setup
- Signal Conditioning (including Arc Suppression)
- Field Wiring

4.1 SITE PREPARATION

Adequate site planning and preparation can simplify the installation process and result in an efficient, reliable UDC system installation. The customer's planning staff should prepare a list of the actual components to be used in the installation. This list should include such items as tape-storage cabinets, work tables and desks, and any other items pertinent to the customer's computer applications. In selecting the site for the installation, consideration should be given not only to the physical dimensions of the units comprising the system, but also to service and operating space requirements and future expansion. The usefulness of a given area depends on many factors, such as length-width ratio, location of columns, and position of doors, windows, and electrical outlets, so that a truly usable area need be distinguished from that which only appears to be usable. Scale drawings of the possible site locations should be prepared and consideration given to factors such as size of entrances into site area (they should be large enough to allow entry of the largest unit of the system), proximity to large inductive machines, circuit availability of adjacent working area (enough room should be allowed to accommodate the equipment, required personnel, storage facilities, and service area).

While operating, the system can produce anywhere from 5,000 to 50,000 Btu/hr (depending on the size) which must be dissipated. While individual units of the system are cooled by blowers and the equipment is designed to operate over a wide temperature range, it is recommended that air-conditioning be installed to ensure reliable long-term operation. An air-conditioned area has the additional advantage of having a positive pressure with respect to the outside area, which materially aids in maintaining a dust and dirt free environment. The atmosphere in the immediate vicinity of the equipment should be maintained as free from offensive dust and corrosive air as possible.

An average illumination of about 40 foot-candles measured 30 inches above the floor should be available in the area. Direct sunlight should be avoided since lower levels of illumination are needed to observe the various indicator lights on the control panels and operator consoles.

4.1.1 Space Requirements

Space requirements are determined by the specific system configuration to be installed, and, when applicable, provision for future expansion. To determine the exact area required for a specific configuration, a machine-room floor plan layout is helpful. When applicable, space is provided in the machine room for storage of tape reels, printer forms, card files, system documentation, etc. The integration of the work area with the storage area depends on the work-flow requirement between areas.

In large installations where test equipment is maintained, DEC recommends that the test equipment storage area be within or adjacent to the machine room. Figure 4-1 shows the space requirements for maximum and minimum UDC8 configurations. This does not include the computer cabinet or other peripheral devices.

4.1.2 Environmental Conditions

An ideal computer room environment has an air distribution system which provides cool, well-filtered, humidified air. The room air pressure should be kept higher than the pressure of adjacent areas to prevent dust infiltration.

4.1.2.1 Humidity and Temperature — The UDC is designed to operate in a temperature range of from 0°C to 50°C, at relative humidity to 95 percent with no condensation. However, typical system configurations using input/output devices such as magnetic tape units, card readers, etc., require an operational temperature range between 18°C and 27.5°C up to 55 percent relative humidity. Nominal operating conditions for a typical system are a temperature of 21°C with a noncondensation relative humidity of 45 percent.

4.1.2.2 Cleanliness — The following precautions are recommended by DEC to ensure optimum UDC system operation:

a. Do not use steel wool for cleaning floors in the computer room.

b. To prevent air flow interference, do not place material on top of the cabinets.

c. Use a nonconductor type nozzle when vacuuming to minimize the possibility of an electrical accident.

d. Avoid spilling liquids (coffee, soda, etc.) on the equipment and operating controls (e.g., console switches, Teletype® keys, and controls).

4.1.2.3 Static Electricity — Static electricity can be an annoyance to operating personnel and can (in extreme cases) affect the operational characteristics of the UDC System and related peripheral equipments. If carpeting is installed on the installation room floor, it should be of a type designed to minimize the effects of static electricity. Flooring consisting of metal panels, or flooring with metal edges, should be adequately grounded.

4.2 POWER REQUIREMENTS

The following information pertains specifically to UDC8 subsystems. For detailed information regarding PDP-8 power requirements, including options, refer to the *PDP-8/E & PDP-8/M Small Computer Handbook.*

UDC Systems are sold in a variety of H964 cabinet configurations. Each cabinet contains a power control (849A) and a power supply (H740D) for each file implemented. The H740D Power Supply is capable of supplying +5V @ 20A. The H738A Power Supply is optional and is available for implementing the A633 DACs.

®Teletype is a registered trademark of Teletype Corporation.

RECOMMENDED
OVERHEAD
CLEARANCE   18 in.

ADDITIONAL 4in. FOR
TERMINATION
CABINET

70.93 in.

SIDE VIEW

APPROX 168 in.

21 in.

| SCREW TERMINAL CABINET 4 | LOGIC CABINET 4 | SCREW TERMINAL CABINET 3 | LOGIC CABINET 3 | SCREW TERMINAL CABINET 2 | LOGIC CABINET 2 | SCREW TERMINAL CABINET 1 | LOGIC CABINET 1 |

30 in.

$66 \frac{7}{16}$ in.

$18 \frac{7}{32}$ in.

PLAIN VIEW
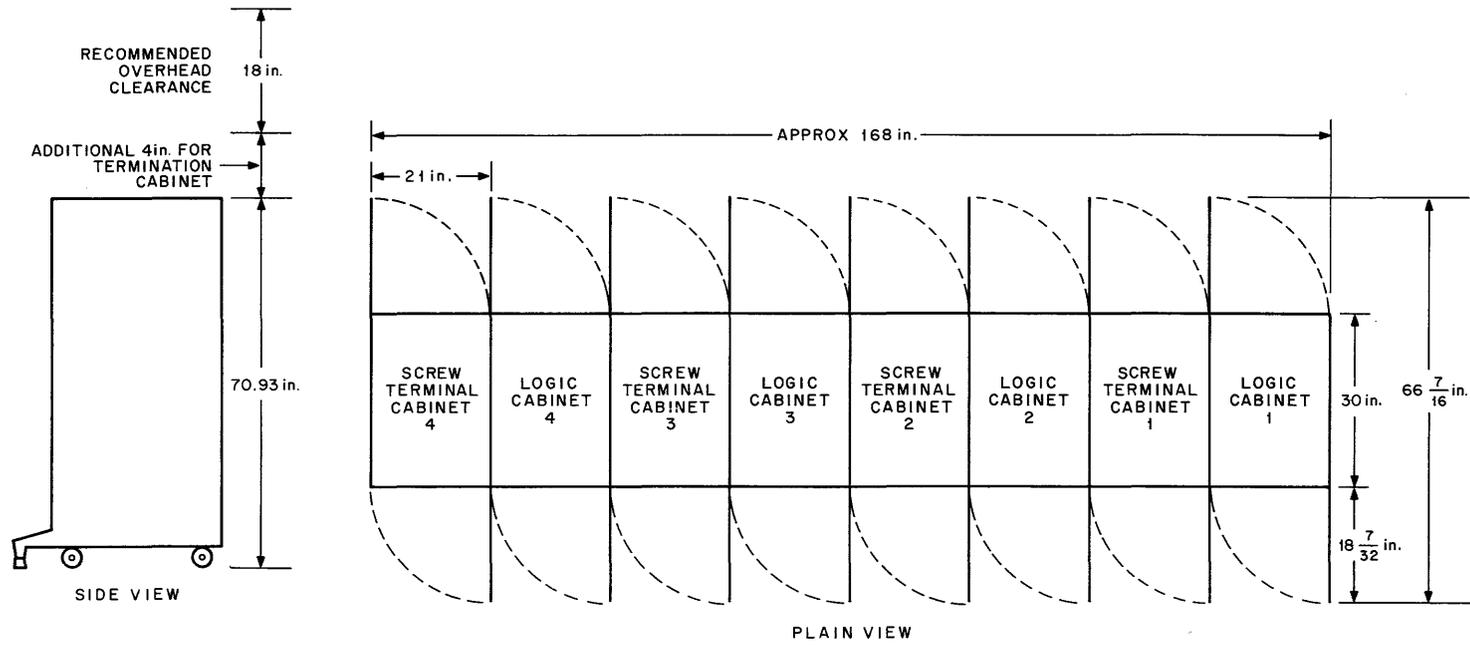
08-0685

Figure 4-1   Space Requirements for UDC8

4.2.1 Logic Power

The internal control and logic power requirements for each logic cabinet are directly dependent on the number and type of functional modules installed in that cabinet. One H740D Power Supply is provided for each file implemented in a cabinet. As previously described, the H740D Power Supply has a maximum current capacity of 20A. The power Requirements for the functional part of the UDC8 are shown in Table 4-1. The power consumption for the total number of modules implemented in the files should not exceed the capacity of the H740D Power Supply.

Table 4-1
UDC8 Power Requirements

Item	Consumption (Amps)
Master File	3.0
Expander File	0.3
DD02	0.3
W730	0.100
W732	0.450
W740	0.350
W742	0.450
M684	* 0.250
M686	* 0.400
M802	* 0.250
M804	* 0.225
M806	* 0.400
W734	1.0
W400	none
W402	none
W403	none
A633 A233 A234 A235 A236	Power supplied by one H738A per four A633 Modules

*This value assumes that 6 of the 12 circuits on the module are energized. The power requirement is directly proportional to the number of circuits energized at one time.

4.2.2 Primary Power Requirements

Each logic cabinet requires a 30/15A (115/230V) primary power source. Both local and remote control is provided. Local control provides the means for energizing each logic cabinet independently. Remote control is chained from one cabinet to the other; therefore, the entire system can be energized by operating the power switch on the computer console. Each cabinet contains all the control circuits and power supplies to establish the type of control desired, and to convert the primary ac power to the dc voltages required by the logic cabinet. Protection for overvoltage and overcurrent is included in the power supplies. A simplified block diagram illustrating the distribution of the power within a cabinet is shown in Figure 4-2. For detailed information concerning distribution and control of ac and dc power, refer to engineering drawings provided in Volume II of this manual.

4-4
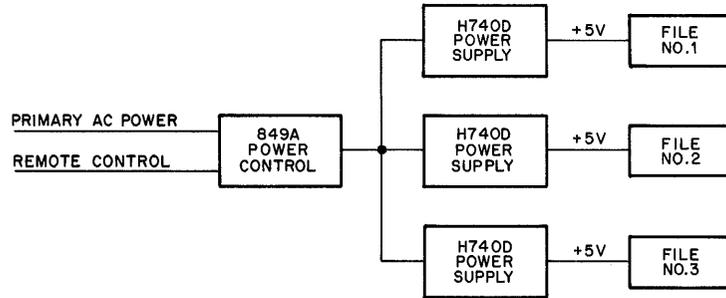
II-0973

Figure 4-2   UDC8 Logic Cabinet Power Distribution Block Diagram

4.2.3 Primary Power Receptacles

The installation site primary power line must terminate in Hubbell wall receptacles (or equivalent) to be compatible with the UDC8 System power line connector. The Hubbell wall receptacle part numbers are shown in Table 4-2.

Table 4-2
Hubbell Wall Receptacle Part Numbers

Line Voltage	Hubbell Receptacle Part Numbers
115 Vac, 60 Hz, 30A	Receptacle 3330-G (3330 may be used) Cap 3331-G (3331 may be used)
230 Vac, 50 Hz, 20A	Receptacle 7310-G (7310 may be used) Cap 3321-G (3321 may be used)

4.3 INSTALLATION CHECKOUT

4.3.1 Unpacking and Visual Inspection

After unpacking the equipment a visual inspection should be made to ensure against loose modules and connections. An inventory should be performed at this time to ensure all equipment and supporting documentation is present. (Refer to Accessory List.)

4.3.2 I/O Bus Connections

Three BC08 Cables are required to connect the PDP-8 I/O bus to the UDC8 from the computer or some other peripheral device. These cables are to be inserted in slots A01, A02, and A03 of the DD01 Interface Controller as follows:

> BAC bus: slot A01
> BMB bus: slot A02
> AC bus: slot A03

Slots B01, B02, and B03 may require M906 Termination Modules if the UDC8 is the last peripheral on the I/O bus. If not, they will contain another set of BC08 Cables to extend the I/O bus to the next peripheral device.

4.3.3 UDC Bus and Connections

The UDC bus consists of 60 lines, 31 driven by open collector-drivers at the DD01 Master Control and 29 driven by open collectors on I/O modules. Bus receivers on M510 Modules in the DD01 and on the M851 in each DD02 allow the full complement of functional modules to share the bus lines. Special double connector modules (M935), a set of flat Mylar® cables, and a set of power cables are required to extend the UDC bus and power throughout the UDC. The UDC bus is chained from one DD02 to another within a file with the M935 Bus Connectors. This module connects the bus lines of slot AB14 in the DD01 to AB01 of the first DD02 File Unit; slot AB04 is connected by an M935 to AB01 of the next DD02. One more DD02 may be thus connected in the first file. Further extension of the UDC bus is accomplished by connecting from the AB04 of the last DD02 in the file to AB01 of the first DD02 in the next file, using a 5-ft flat Mylar (BC41A-5) cable. A 10-ft flat Mylar (BC41A-10) is used to extend the bus between DD02s in different cabinets. Two terminating modules (M942) are also required to construct the UDC bus. These modules must be inserted in slot AB11 of the DD01 and in slot AB04 of the last DD02 on the bus. If no DD02 File Units are used, the second M942 Module is used in slot AB14 of the DD01.

4.3.4 External Cabling

The BC40C Screw Terminal Assembly is the point at which customer control circuits connect to the UDC8 signal-conditioning modules. Each circuit is completed through a twisted pair of No. 26 AWG stranded color-coded wire connected to a pair of screw terminals. The terminals will accommodate No. 14 AWG wire, and are arranged in two strips of 17 contacts, each supported in line by a common steel angle support. The steel supports are mounted, one above the other, 36 in front and 36 at the rear of the dedicated cabinet. In the single file, single-cabinet configuration, the screw terminals are mounted 12 front, 12 rear. The field wiring may enter only from the top or bottom of the cabinet. Field wiring should be twisted pairs per control point. Maximum current per point is 2A, limited by relay contact ratings; large wire is thus unnecessary. The twisted-pair field wiring is used to avoid stray pickups and to minimize the radiation of switching transients by confining their fields largely to the space between the two wires of the twisted pair.

Horizontal bars are located at the top and bottom of the screw terminal cabinet, to be used for strain relief on incoming cables. In addition, strain-relief members are located at both ends of the screw terminal brackets. The input cables should be routed over these members to provide for strain relief as they branch out to individual screw terminals. As the cables enter the screw terminal cabinet, they should be routed over the strain-relief bar and up/down both sides of the cabinet.

4.3.5 Electrical AC Power Cabling

The 849A Power Controller supplies ac power to the UDC. The 849A Power Controller can operate in two modes, remote and local. In the remote mode, an ac power cable is required between the central-processor controlled ac power outlet and the 849A Control Socket. This provides ac power to control the circuit breaker when the central processor is turned on and off. In the local mode, the circuit breaker is controlled manually at the front of the 849A.

The ac power for the UDC is normally 115 Vac, 60 Hz, single-phase, (220 ac, 50 Hz, single-phase) three wire. Power for the UDC should be supplied from the same source as is the central processor.

Before connecting ac power to the UDC, measurements should be made at the Hubbell wall receptacle between ac hot and ground, ac neutral and ground, and ac hot and ac neutral to ensure that proper power is available.

® Mylar is a registered trademark of E. I. DuPont de Nemours and Company.

After determining proper power is available, ensure that the 849A LOCAL/REMOTE switch is in LOCAL and the circuit breaker is off. Plug the 849A ac Power Cable in and measure the voltage between the cabinet and ac power ground; this measurement should be 0V. Energize the 849A by switching the circuit breaker on and again make the measurement from cabinet to ground; again, 0V should be read.

If the system has more than one UDC logic bay, each 849A Power Controller (one per logic bay) will have to be connected and checked individually.

NOTE
If the checks of power outlined above show any discrepancies, these problems must be corrected before proceeding. A SHOCK HAZARD may exist.

4.3.6 DC Voltage Checks

Two types of power supplies can be used in the UDC system. The H740D Power Supply is used to supply file logic power. One H740D Power Supply is provided for each file implemented. The H738A Power Supply is used in UDCs containing D to A options (A633) only.

Check the dc output voltage of each H740D Power Supply by measuring the tabs on the right-hand most G729 (+ tab on top, gnd tab on the bottom) in each UDC file. This measurement ensures that +5 Vdc is supplied to all logic and I/O modules in the UDC.

Check the dc voltages supplied by the H738A to the DAC option for +18, −18, and +5 volts at the screw terminals. The screw terminals that are connected to DAC options are the only terminals that are prewired on the screw side.

4.3.7 UDC Functional Checkout

Using the UDC Acceptance Procedure (A-SP-UDC8-0-4) supplied with the documentation, the UDC Exerciser Program (MAINDEC-08-D8YB-D), and the UDC Field Test Box, proceed to check the functional I/O modules. The UDC Acceptance Procedure details specific steps and procedures used in checking the various functional I/O modules utilizing the test box and the exerciser program.

4.3.8 System Pre-Use Requirements

After the system has been connected and checked out as described in Paragraphs 4.3.1 through 4.3.7, there remain steps the customer must perform before putting the UDC into operation:

    a.   Signal conditioning (arc suppression) for output functional I/O modules. Refer to Paragraph 4.6.

    b.   Field cable connections to the UDC screw terminals.

    c.   Determination of any special addressing of functional I/O modules that require changing the G729 Address Selection Modules.

4.3.9 UDC Add On Expansion

The UDC can be expanded in four ways:

    a.   Addition of more functional I/O modules.

    b.   Addition of DD02 system units.

c. Addition of UDC8-X system files.

d. Addition of other UDC bays.

The latter presumes inclusion of the preceding items.

The additions, as they occur, require the following considerations.

a. The addition of I/O functional modules requires an available I/O slot, adequate power from the H740D Power Supply, and mounting of the screw terminals. After the added modules are installed, functional checkout is accomplished using items described in Paragraph 4.3.7 for those added modules.

b. The addition of other DD02 system units requires adequate mounting space in the BF01 file, power cabling, and the UDC bus continuation with an M935 from the preceding DD02. Before adding I/O modules, a check of (*a*) above should be made.

c. The addition of other UDC8-X system files requires adequate space in the cabinet, power cabling, and continuation of UDC bus via a BC41A cable.

d. The addition of other UDC bays should be treated as described in Paragraphs 4.3.1 through 4.3.7.

4.4 UDC SYSTEM CONFIGURATION

Configuration of UDC Systems is a user task and each system can be set up for optimum performance. In configuring a system, the user should consider his requirements in terms of functional areas. The UDC is basically a digital multiplexer with the added availability of identifying user interrupts. Thus, functionally the UDC can perform the following:

a. Bi-Level Interrupt Identification
  1. Immediate
  2. Deferred

b. Status or State of Operation

c. Control

4.4.1 Bi-Level Interrupt Identification

The UDC control logic contains a hardware scanning feature to search for the address of any interrupting module. Upon recognition of a UDC interrupt by the skip chain program, the hardware scanner may be started under program control to sequentially search the UDC address complement to find the interrupting module. Table 4-3 defines the priorities of all module addresses. The bi-level UDC interrupt structure is useful in that the system programmer can choose two classes of interrupts, those requiring immediate program action and a deferred mode, where program action can be performed at a later time.
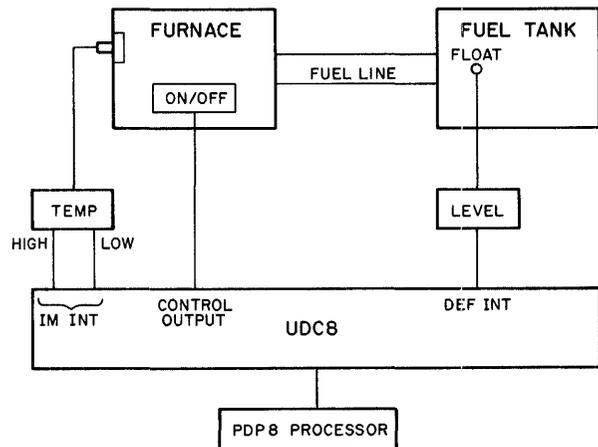
08-0753

Figure 4-3 Interrupt Class Example

The simple example of a temperature monitoring process illustrated in Figure 4-3 shows this concept more readily.

Table 4-3
Scanner Counting Characteristics

Address Jumpers X	Y	**Address Scanner Count (1 μsec per count)** 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
0	0	0	1	2	3												MODULE NUMBERS		
0	1		4	5	6	7													
0	2			8	9	10	11												
0	3				12	13	14	15											
0	4					16	17	18	19										
0	5						20	21	22	23									
0	6							24	25	26	27								
0	7								28	29	30	31							
1	0		32	33	34	35											MODULE NUMBERS		
1	1			36	37	38	39												
1	2				40	41	42	43											
1	3					44	45	46	47										
1	4						48	49	50	51									
1	5							52	53	54	55								
1	6								56	57	58	59							
1	7									60	61	62	63						
2	0			64	65	66	67										MODULE NUMBERS		
2	1				68	69	70	71											
2	2					72	73	74	75										
2	3						76	77	78	79									
2	4							80	81	82	83								
2	5								84	85	86	87							
2	6									88	89	90	91						
2	7										92	93	94	95					
3	0				96	97	98	99									MODULE NUMBERS		
3	1					100	101	102	103										
3	2						104	105	106	107									
3	3							108	109	110	111								
3	4								112	113	114	115							
3	5									116	117	118	119						
3	6										120	121	122	123					
3	7											124	125	126	127				
4	0					128	129	130	131								MODULE NUMBERS		
4	1						132	133	134	135									
4	2							136	137	138	139								
4	3								140	141	142	143							
4	4									144	145	146	147						
4	5										148	149	150	151					
4	6											152	153	154	155				
4	7												156	157	158	159			
5	0						160	161	162	163							MODULE NUMBERS		
5	1							164	165	166	167								
5	2								168	169	170	171							
5	3									172	173	174	175						
5	4										176	177	178	179					
5	5											180	181	182	183				
5	6												184	185	186	187			
5	7													188	189	190	191		
6	0							192	193	194	195						MODULE NUMBERS		
6	1								196	197	198	199							
6	2									200	201	202	203						
6	3										204	205	206	207					
6	4											208	209	210	211				
6	5												212	213	214	215			
6	6													216	217	218	219		
6	7														220	221	222	223	
7	0								224	225	226	227					MODULE NUMBERS		
7	1									228	229	230	231						
7	2										232	233	234	235					
7	3											236	237	238	239				
7	4												240	241	242	243			
7	5													244	245	246	247		
7	6														248	249	250	251	

In this example, the furnace has a control unit that will provide ignition or shut down, a temperature sensing element that will provide an interrupt at a preset temperature, and a fuel supply that contains a float switch to indicate low fuel. If furnace temperature is too high or too low, the UDC should be interrupted immediately and the furnace should be turned off or on depending on the interrupt received. However, the float switch is only an indicator of low fuel supply; this interrupt can be recognized at a later time and thus is placed on the deferred line.

4.4.1.1 Module Interrupt Selection — Each interrupting UDC module can be placed in either immediate or deferred mode. This is accomplished by the proper selection of jumpers on the module and will be covered in Paragraph 4.5, Functional I/O Modules.

4.4.2 System Interrupt Response

The system interrupt response is defined as:

MODULE OPERATE TIME + SCAN TIME + PDP-8 INTERRUPT SERVICE TIME + PROGRAM TIME.

a. Module Operate Time

W732 Relay Input Contact Interrupt — 2 ms
W742 Solid State Input Contact Interrupt — 2.5 ms (50 μs with high-speed option)
W734 I/O Counter — Int on Overflow

b. Scan Time

Table 4-3 gives the search time for each UDC address.

c. PDP-8 Interrupt Service Time

This time depends entirely on the system configuration and the status of the system at the time of the UDC interrupt. For a complete discussion of PDP-8 interrupt facilities, refer to the *1972 Small Computer Handbook,* Chapter 9, page 9-56.

d. Program Time

Program time can be computed from the service routine being used and information regarding processor cycle time which is available in the *1972 Small Computer Handbook.*

It should be noted that although the operate time of the input modules is quite long, interrupts can be waiting for service due to the receipt of two or more at the same time. Thus, the need for fast search time and processor service time is evident.

4.4.3 Generic Codes

Each UDC interrupting module contains a 4-bit code that is present at the time the UDC module address is read. This code allows the user to determine what type module has caused the interrupt. The codes for each module are listed below:

Module	Generic Code	
W732	0010	Hardwired on Module
W742	0011	Hardwired on Module
W734	0100 0101 0110 0111	(Selectable on Module by jumper)

4.4.4 Status and Control

The remaining function of a UDC System is to obtain process status information and to provide control. These functions are provided by the remaining non-interrupting functional I/O modules. Placement of these modules is not critical and their location can be specified by convenience. However, it is advisable to segregate high-voltage switching elements such as mercury-wetted relay outputs from D/A converter outputs (A633) if at all possible.

4.4.5 User Identification — Functional I/O Modules

After the system is configured and functional I/O module place-ment is complete, the user is encouraged to utilize the I/O mod-ule cross reference provided. The cross-reference scheme in-cludes a Functional Module I/O Chart (Figure 4-4) and a Func-tional Module I/O Page (Figure 4-5). The I/O chart is found on the back door of each UDC electronics cabinet and contains space for information to identify each I/O module in the cabinet. The I/O chart also includes a column entitled "Page No.", this column is used to reference the module listed in the I/O chart with detailed module descriptions contained on the Module I/O Page. Module I/O Pages are provided with each UDC system.

4.4.6 Address Assignments

After a system is installed, addresses may be reassigned to the functional modules. This is accomplished by changing two jump-ers (one in the X field and another in the Y field) on the address jumper modules (G729) of the address selectors (Figure 4-6). These jumpers define the first two digits of the addresses of the four module slots in the file unit.

These two digits are straight octal, and the pair may be considered to be the address of the file unit. The 8 x 8 matrix and accom-panying diagram presented in Figure 4-7 illustrates this scheme.

The G729 modules are piggy-back modules that mount on the M851 Address Decoder Modules of the file unit (DD02). By in-stalling a jumper in the X field and a jumper in the Y field, the four functional modules that are housed in that file unit will each respond to a unique address 0 through 3. To maintain configuration simplicity, it is recommended that ad-dresses be assigned to the modules continuously from right to left and from top to bottom (viewing cabinet from rear), starting with channel no. 0.

If the channel numbers are reassigned to the modules, the corresponding screw-terminal strips must be relabeled with the word number. See Figure 4-8 for details on the numbering scheme for slots and screw terminals.

In addition, the channel identification chart on the back door of the logic cabinet must be filled in and an infor-mation page filled out as addresses are assigned, modules are inserted, and customer devices are connected.

dec			cab___		File___				
WORD ADDR		FILE UNIT JUMPERS	W O R D	SCREW TERMINAL			MODULE TYPE		PAGE NO.
DEC	OCTAL	X	Y	0-3	FILE	SLOT	TERM	I/O	SIG COND	
				0		S1	T1F			
				1		S2	T2F			
				2		S3	T3F			
				3		S4	T4F			
				0		S6	T5F			
				1		S7	T6F			
				2		S8	T7F			
				3		S9	T8F			
				0		S11	T9F			
				1		S12	T10F			
				2		S13	T11F			
				3		S14	T12F			
				0		S16	T1R			
				1		S17	T2R			
				2		S18	T3R			
				3		S19	T4R			
				0		S21	T5R			
				1		S22	T6R			
				2		S23	T7R			
				3		S24	T8R			
				0		S26	T9R			
				1		S27	T10R			
				2		S28	T11R			
				3		S29	T12R			

08-0686

Figure 4-4   Functional Module I/O Chart

PAGE NO. _____

MODULE TYPE: _____

SIGNAL CONDITION TYPE: _____

WORD NO. _____

WORD ADDRESS		FILE UNIT		WORD NO.	MODULE LOCATION			FIELD WIRING		FIELD PWR.		CONTACT INTERRUPT		INTERRUPT ENABLE	
DECIMAL	OCTAL	X	Y		C A B	F I L E	S L O T	F I L E	S L O T	T E R M	V	I	PULSE OPEN	PULSE CLOSE	IMMED	DEFERRED

GENERIC CODE

BITS	ARC SUPPRESSION		TIMING S/S	ACTIVE CONTACTS (FORM A OR B)	BIT FUNCTION REMARKS
	RES	CAP			
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					

08-0675

Figure 4-5   Functional Module I/O Page

Figure 4-6   G729 Address Jumper Module

ADDR

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |

X_8 Y_8 WD

2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0

PDP-8 I/O BUS

BMB   IOT

BAC   ADDRESS AND DATA

AC   ADDRESS AND DATA

INTERFACE CONTROLLER DD01 (35_8 AND 36_8)

ADDRESS SELECTOR

NO.0 (00) P/O INTERFACE CONTROLLER

NO.1 (01)

NO. 2 (02)

NO. 63 (77)$_8$

MODULE

0 (SLOT 1)

1 (SLOT 2)

2 (SLOT 3)

3 (SLOT 4)

WD

00 – MODULE 0
01 – MODULE 1
10 – MODULE 2
11 – MODULE 3

	Y							
	0	1	2	3	4	5	6	7
0	000 003	004 007	010 013	014 017	020 023	024 027	030 033	034 037
1	040 043	044 047	050 053	054 057	060 063	064 067	070 073	074 077
2	100 103	104 107	110 113	114 117	120 123	124 127	130 133	134 137
3	140 143	144 147	150 153	154 157	160 163	164 167	170 173	174 177
4	200 203	204 207	210 213	214 217	220 223	224 227	230 233	234 237
5	240 243	244 247	250 253	254 257	260 263	264 267	270 273	274 277
6	300 303	304 307	310 313	314 317	320 323	324 327	330 333	334 337
7	340 343	344 347	350 353	354 357	360 363	364 367	370 373	374 377

X

08-0688

Figure 4-7   Channel Address Scheme

DUAL CABINET CONFIGURATION

FILE SLOT NUMBER ─ S □ □ T □ □ □   MOUNTING PLANE

MASTER FILE [A]   [F] FRONT
EXPANDER FILE [B]   [R] REAR
EXPANDER FILE [C]

SLOT   [0] [1]→[1] [2] STRIP NO.

FILE SLOT [0] [1]→[2] [9]   TERMINAL STRIP

LOGIC CABINET 1 2 3 4 6 ----- 29	SCREW TERMINAL CABINET FRONT	REAR
MASTER FILE	/////	A-S16-T1R
	/////	A-S17-T2R
A	A-S11-T9F	
	A-S12-T10F	
	A-S13-T11F	
	A-S14-T12F	A-S29-T12R
EXPANDER FILE	B-S1-T1F	B-S16-T1R
	B-S2-T2F	B-S17-T2R
B		
	B-S14-T12F	B-S29-T12R
EXPANDER FILE	C-S1-T1F	C-S16-T1R
	C-S2-T2F	C-S17-T2R
C		
	C-S14-T12F	C-S29-T12R

CONTROLLER   MASTER FILE I/O SLOTS

S1 S2 S3 S4 //// S6 S7 S8 S9 //// S11 S12 S13 S14 //// S16 S17 S18 S19 //// S21 S22 S23 S24 //// S26 S27 S28 S29

EXPANDER FILE I/O SLOTS

08-0689

SINGLE CABINET CONFIGURATION

LOGIC AND SCREW TERMINAL CABINET
1 2 3 4 6 ------- 29

MASTER FILE OR EXPANDER FILE

FRONT	REAR
A-S1-T1F	A-S16-T1R
A-S2-T2F	A-S17-T2R
A-S3-T3F	A-S18-T3R
A-S4-T4F	A-S19-T4R
A-S6-T5F	A-S21-T5R
A-S7-T6F	A-S22-T6R
A-S8-T7F	A-S23-T7R
A-S9-T8F	A-S24-T8R
A-S11-T9F	A-S26-T9R
A-S12-T10F	A-S27-T10R
A-S13-T11F	A-S28-T11R
A-S14-T12F	A-S29-T12R

NOT USED FOR MASTER FILE (brackets rows A-S4-T4F through A-S9-T8F)

11-0974

Figure 4-8 Slot and Screw-Terminal Numbering Scheme

The UDC System final factory checkout will be made with address jumpers on G729 Modules installed in such a manner that addresses are sequential, starting with 000, 001, 002 and 003 in the DD01 Control. Addresses will progress down the bus in order. Addresses may be changed by moving jumpers on G729 Modules, but care must be exercised to avoid duplicating X and Y pairs. The address, slot location, and screw-terminal map should be used for cross reference and record-keeping.

The matrix shown in Figure 4-7 enables the user to determine the four addresses that belong to any X and Y combination.

Example:

$$X = 4, Y = 6$$

Matrix Box for above X and Y = [230 / 233]
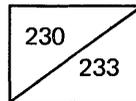
This box shows addresses 0230, 0231, 0232, 0233.
These are the absolute addresses for X4 and Y6:

Address:

```
 0     2     3     3
 |     |     |     |
|000| |010| |011| |011|
      └──┘  └───┘ └─┘
        X=4    Y=6  WD=3
```

Address:

```
 0     2     3     0
 |     |     |     |
|000| |010| |011| |000|
└────┘ └────┘ └─┘
        X=4    Y=6  WD=0
```
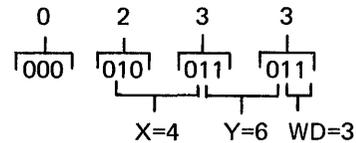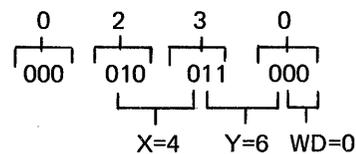
4.5 FUNCTIONAL I/O MODULE SETUP

The following data sheets provide information on all UDC8 functional I/O modules. The user is advised to read the data sheets on each module type in his system carefully; he should pay particular attention to the jumper configurations. The following I/O modules are discussed:

a.	Contact Sense (Relay)	W730
b.	Contact Interrupt (Relay)	W732
c.	Contact Sense (Solid State)	W740
d.	Contact Interrupt (Solid State)	W742
e.	Flip-Flop Driver	M684
f.	Single Shot Driver	M686
g.	Latching Relay Output	M802
h.	Flip-Flop Relay Output	M804
i.	Single-Shot Relay Output	M806
j.	D/A Converter Output	A633
k.	I/O Counter	W734

CONTACT SENSE RELAY INPUT MODULE

FUNCTIONAL SPECIFICATIONS

Power Requirements: +5V @ 0.1A max

Input Response Time: 2 ms including Input Relay Bounce

Input Isolation: $10^9 \, \Omega$ min, 250V

Input Voltage: 6V ± 5% @ 15 mA

Field to Logic Transfer: 0V at Input = Logic 0 DATAI

Signal Conditioning: W400 or W402 required. Provisions for 24 Vdc or 48 Vdc
                               operation are available.

08-0695
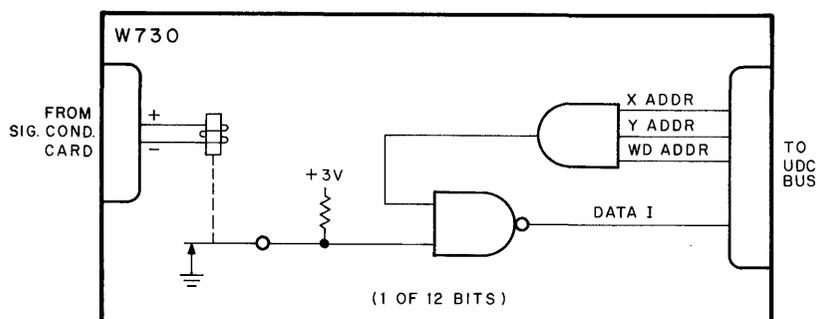
Figure 4-9 Simplified Schematic Diagram (W730)

DESCRIPTION

The W730 Contact Sense Module (Figure 4-9) contains 12 bits of contact sense logic. When addressed by the UDC, information concerning the state of the 12 relays is present at the DATAI gates. This data is the present condition of the 12 relays, and can change at any time. It is not stored in any buffer, and is used for monitoring purposes.

CONTACT INTERRUPT RELAY INPUT MODULE

FUNCTIONAL SPECIFICATIONS:

Power Requirements:	+5V @ 0.45A max
Input Response Time:	1 ms max (Relay Bounce filtered)
Input Isolation:	$10^9 \Omega$ min, 250V
Input Voltage:	6V ± 5% @ 15 mA
Field to Logic Transfer:	Interrupt on Input Transition, 0V = Logic 0 DATA I
Signal Conditioning:	W400 or W402 required. Provisions for 24 Vdc or 48 Vdc operation are available.

08-0696
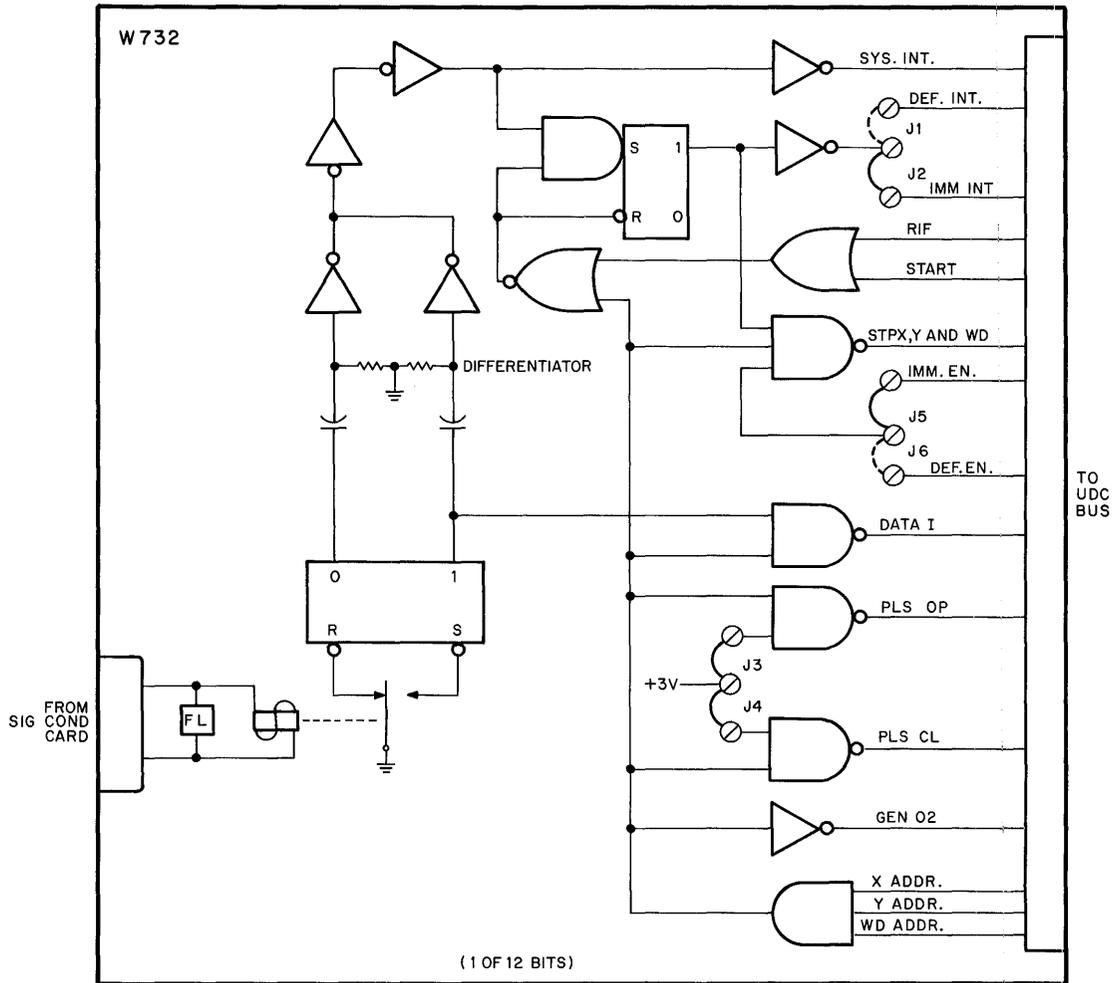
Figure 4-10   Simplified Schematic Diagram (W732)

DESCRIPTION

The W732 Contact Interrupt Module (Figure 4-10) provides electrically isolated, differential inputs for 12 external customer contacts or voltages. Isolation of up to 250V is achieved by a miniature reed relay buffer on each input point. This module provides reliable and trouble-free digital sensing in high noise environments. Also, its differential input characteristics are particularly suited for those applications where the ground of the customer's excitation voltage power supply may be different from (i.e., not directly strapped to) computer system ground. However, excitation voltages of 24V or 48V may be used by jumper selection on the signal-conditioning module that plugs into the W732 Module. The higher excitation voltages of 24V or 48V are recommended for contact wiping action to ensure reliability where field contacts are open, or subject to dust or oxide buildup.

The input circuits of the W732 Module consist of 12 miniature Form C reed relay windings. The common contact of each relay is grounded. The NO (normally open) Form A contact is connected to the set input; the NC (normally closed) Form B contact is connected to the reset input of an RS flip-flop. The consequence of current flow in the relay winding because of a field contact closure will be to switch ground from the NC contact to the NO contact of the input reed relay. This action causes the RS flip-flop to set. The bus driver inputs for each bit are provided by address enabling and the RS flip-flop output. Changing the DATAI bus signal to a true level generates a logic 1 on the UDC DATAI lines when the module is addressed.

The change in state of the flip-flop is differentiated, the resulting pulse is open-collector ORed to the System Interrupt Line.

MODULE JUMPER CONFIGURATION

The jumpers on the W732 Module must be configured by the user to meet his application needs. The jumpers and their function are listed in Table 4-4 and are shown in Figure 4-11.

<div align="center">

Table 4-4
Jumper Options (W732)

Function	Jumpers Required
IMM INT	J2, J5
DEF INT	J1, J6
PLS OP*	J3
PLS CL*	J4

</div>

*PLS OP and PLS CL are logic levels to be used in Software Routines as an aid in determining change of state information.

CUSTOMER INPUTS

Filtering is required for customer contacts when contact bounce duration is greater than the W732 input response time. Multiple interrupts will occur if contacts are not filtered.

PLS OP J3

PLS CL J4

IMM EN J5

DEF EN J6

IMM INT J2

DEF INT J1
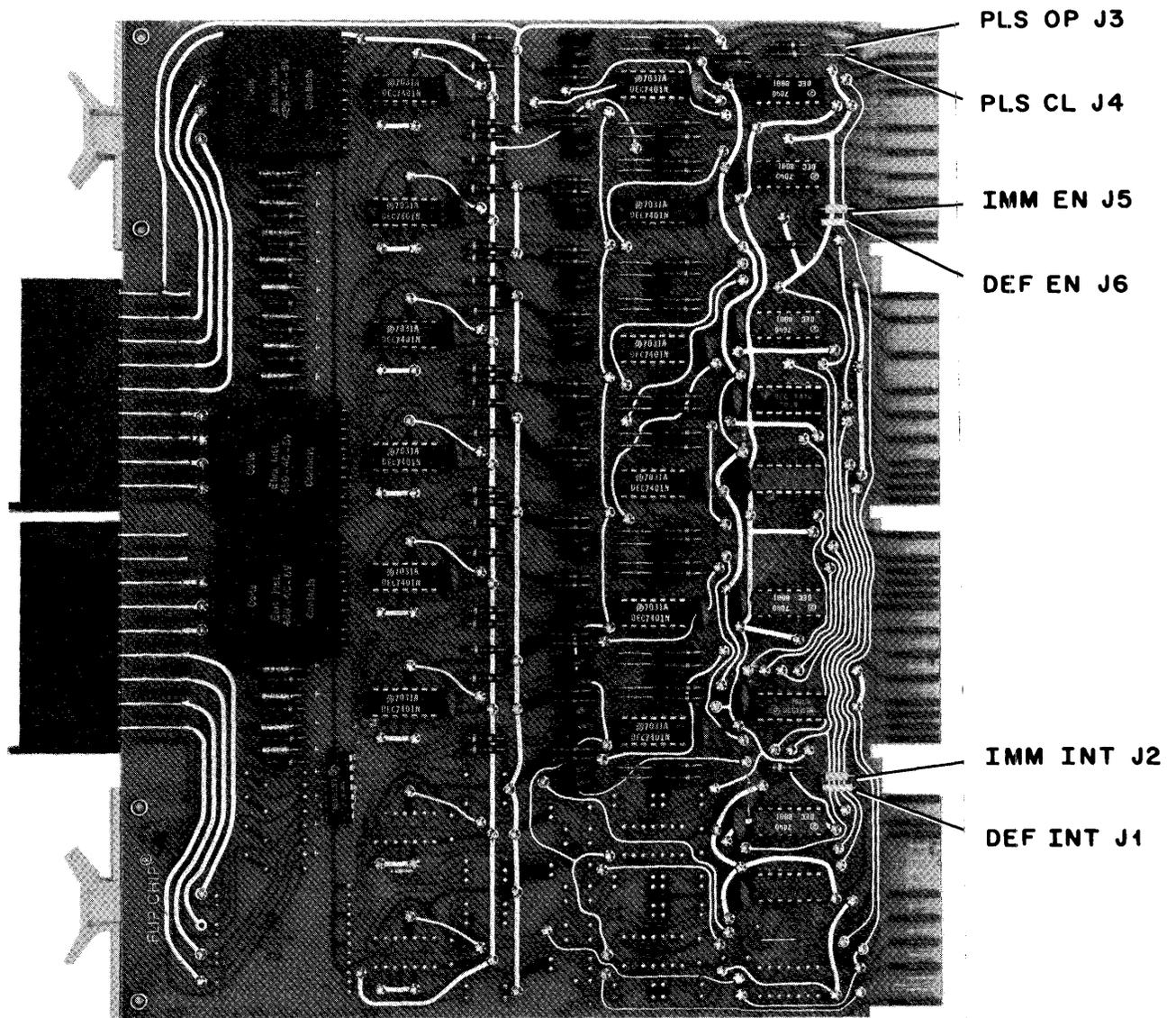
Figure 4-11 Location of Jumpers (W732)

CONTACT SENSE SOLID-STATE INPUT MODULE

FUNCTION SPECIFICATIONS

Power Requirements:	+5V @ 0.25A max
Input Levels:	+4.6V to 7.0V differential input = 1 13 mA to 22 mA
	−1.0V to +1.4V differential input = 0 −2 mA to +2 mA
Input Overvoltage Protection:	±12V max sustained input
Failure Mode:	Fails on per point basis
Response Time:	Normal − 2.5 ms max. High speed − 50 μs max
Input Rate:	Normal − 200 Hz max. High speed − 10 kHz max
Common Mode Input Impedance:	10^{10} Ω min

08-0745
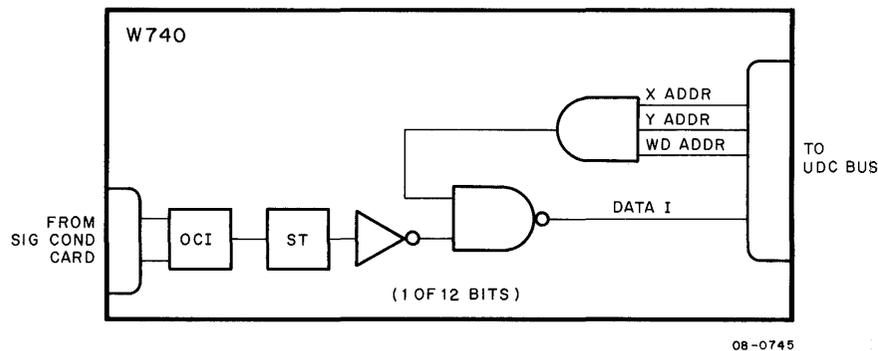
Figure 4-12 Simplified Schematic Diagram (W740)

DESCRIPTION

The W740 Contact Sense Module (Figure 4-12) provides high input isolation with solid-state reliability through the use of a light emitting diode-photo transistor isolation element (OCI) and a Schmitt Trigger (ST). The W740 contains 12 bits of sense logic. When addressed by the UDC, information concerning the state of the 12 bits is present at the data out gates. This data is the present condition of the 12 bits, and can change at any time. It is not stored in any buffer, and is used for monitoring purposes. In addition to contact sensing, the W740 may be directly interfaced to T^2L, RTL, and DTL logic.

HIGH-SPEED OPTION

The W740 Module is capable of a fast response time as indicated in the module specifications. This is accomplished by clipping out the 0.33 μF capacitors shown in Figure 4-13.
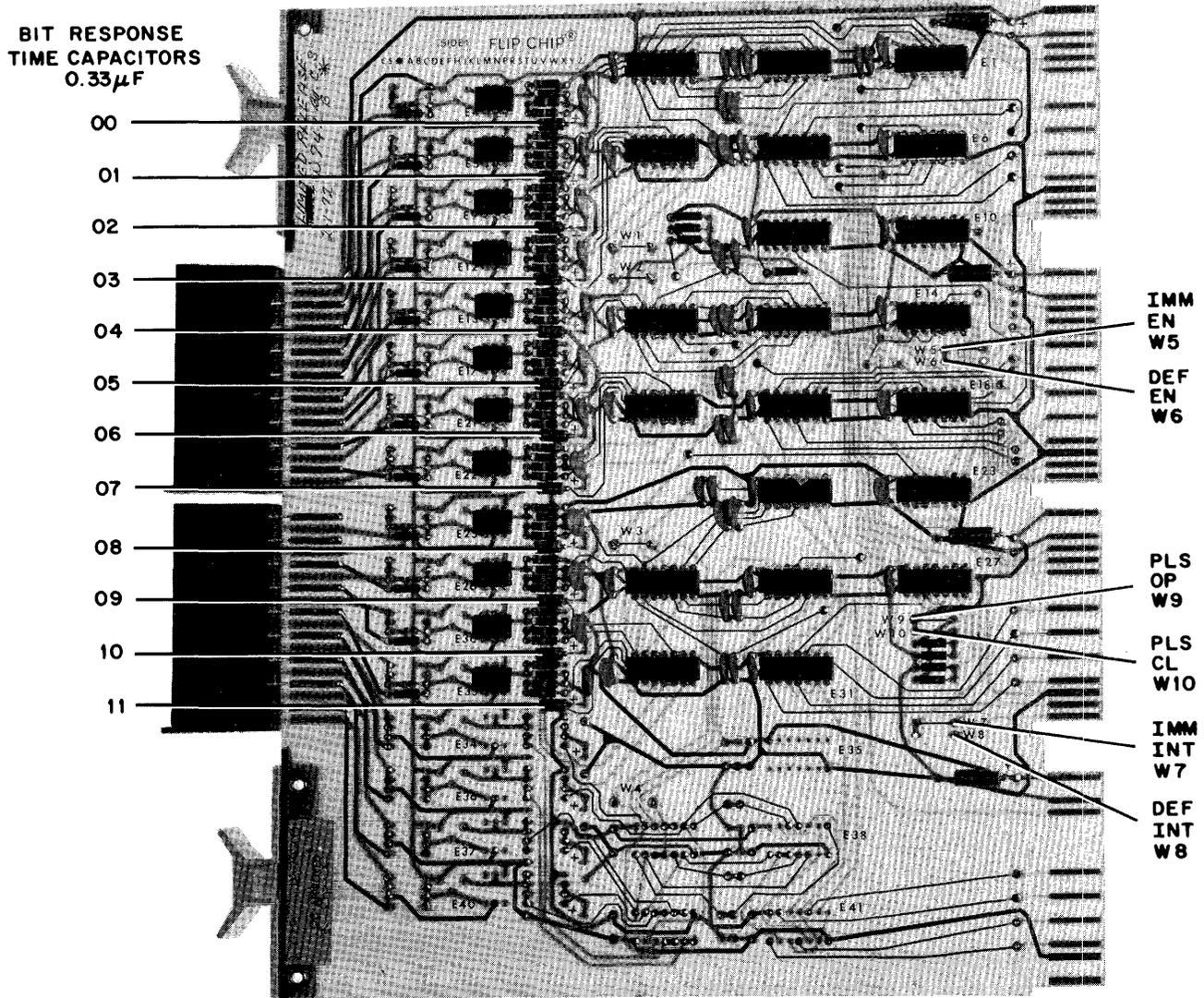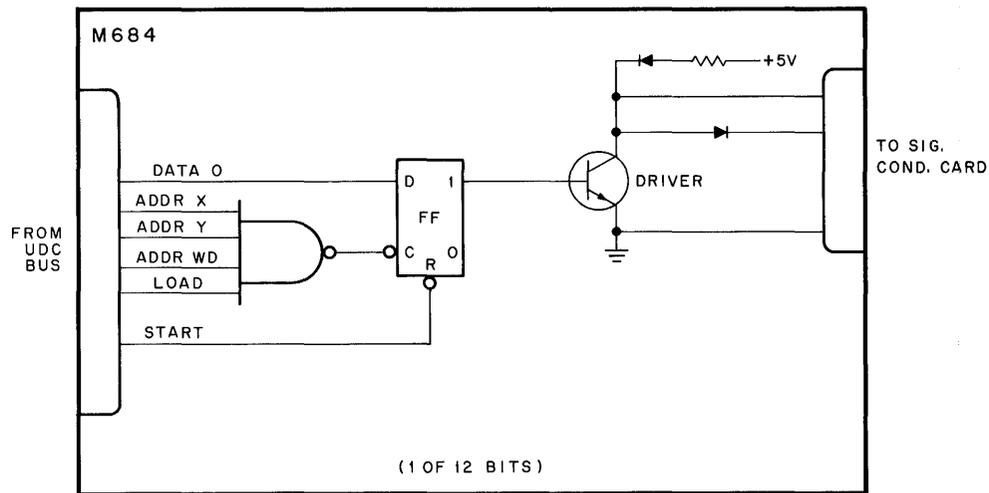
BIT RESPONSE
TIME CAPACITORS
0.33 μF

00
01
02
03
04
05
06
07
08
09
10
11
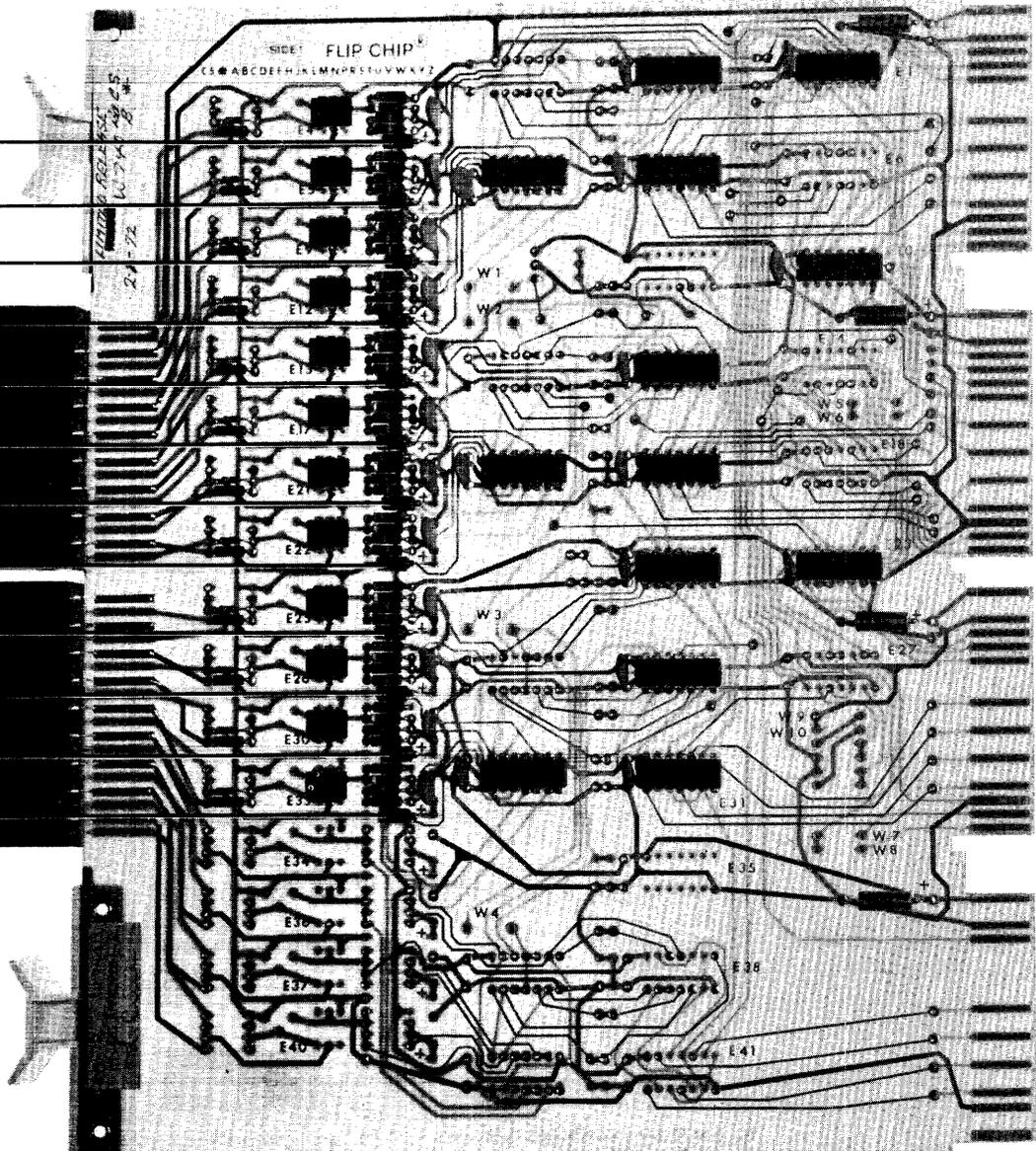
Figure 4-13   Location of Bit Response Time Capacitors (W740)

CONTACT INTERRUPT SOLID-STATE INPUT MODULE

FUNCTIONAL SPECIFICATIONS

Power Requirements:	+5V @ 0.35A max
Input Levels:	+4.6V to 7.0V differential input = 1
	13 mA to 22 mA
	−1.0V to +1.4V differential input = 0
	−2 mA to +2 mA
Input Overvoltage Protection:	±12V max sustained input
Failure Mode:	Fails on per point basis
Response Time:	Normal − 2.5 ms max. High Speed − 50 μs max
Input Rate:	Normal − 200 Hz max. High Speed − 10 kHz max
Common Mode Input Impedance:	$10^{10}\,\Omega$ max

Figure 4-14   Simplified Schematic Diagram (W742)

DESCRIPTION

The W742 Contact Interrupt Module (Figure 4-14) provides high input isolation with solid-state reliability through the use of a light emitting diode-photo transistor isolation element (OCI) and a Schmitt Trigger (ST). The contact interrupt module is similar to the contact sense with the addition of interrupt logic. This logic is activated whenever one of the input points changes state. Via its interrupt and interlocking scan logic, the UDC controller can rapidly identify the interrupting module. The W742 Module can also be directly interfaced to $T^2 L$, RTL and DTL logic.

MODULE JUMPER CONFIGURATION

The jumpers on the W742 Module must be configured by the user to meet his application needs. The jumpers and their function are listed in Table 4-5 and shown in Figure 4-15.

Table 4-5
Jumper Options (W742)

Function	Jumpers Required
IMM INT	W5, W7
DEF INT	W6, W8
PLS OP*	W9
PLS CL*	W10

*PLS OP and PLS CL are logic levels to be used in software routines, as an aid in determining change of state information.

HIGH-SPEED OPTION

The W742 Module is capable of a fast response time as indicated in the module specifications. This is accomplished by clipping out the 0.33 μF capacitors shown in Figure 4-15).

4-28

BIT RESPONSE
TIME CAPACITORS
0.33μF

00
01
02
03
04
05
06
07
08
09
10
11

IMM
EN
W5

DEF
EN
W6

PLS
OP
W9

PLS
CL
W10

IMM
INT
W7

DEF
INT
W8

Figure 4-15   Location of Jumpers and Bit Response Time Capacitors (W742)

FLIP-FLOP DRIVER OUTPUT MODULE

FUNCTIONAL SPECIFICATIONS

Power Requirements: +5V @ 0.5A max

Output Circuit: Solid State — Open collector returned through diode and
                                       resistor to +5V.

Output Drive Capability: Resistive Load — 55 Vdc, 250 mA
                                       Inductive Load — 55 Vdc, 250 mA
                                       (Diode Suppression Supplied)
                                       Incandescent Lamps: Lamps rated at 40 mA, to 48 Vdc
                                                             Lamps rated at 60 mA, to 28 Vdc
                                                             Lamps rated at 80 mA, to 18 Vdc
                                                             Lamps rated at 100 mA, to 12 Vdc
                                       T^2L level compatible (2-unit loads)

Response Time: Rise Time — 10 μs (Resistive load without
                                       Fall Time — 0.5 μs field wiring)

Logic to Field Transfer: A logic 1 will provide current sinking ability

Signal Conditioning: W403 only

Figure 4-16   Simplified Schematic Diagram (M684)

DESCRIPTION

The M684 Flip-Flop Driver Output Module (Figure 4-16) provides 12 identical solid-state buffered outputs. It can be used to drive solid-state logic (0 and +5V) or as a current driver for control of solenoid valves, relays, lamps, displays, etc. Each flip-flop in the output register can be set by the Load Data IOT.

When used to drive logic circuits, a 0V output will be generated by the flip-flop being set and a +5V output will be generated by the flip-flop being cleared. This is accomplished by the load to +5V on the collector of the output circuit. The rise and fall time of this circuit measured at the screw terminals with no external field wiring is 10 μs and 0.5 μs, respectively.

A diode is in series with the +5V load to provide isolation from field voltages when used as a current driver. Each driver circuit is protected from damage by inductive loads. Provided for all 12 circuits is a common ground line, which must be connected to the common side of the field power source.

SINGLE-SHOT DRIVER OUTPUT MODULE

FUNCTIONAL SPECIFICATIONS

Power Requirements:	+5V @ 0.75A max
Output Circuit:	Solid State — Open collector returned through diode and resistor to +5V.
Output Drive Capability:	Resistive Load — 55 Vdc, 250 mA
	Inductive Load — 55 Vdc, 250 mA
	(Diode suppression supplied)
	Incandescent Lamps: Lamps rated at 40 mA, to 48 Vdc
	Lamps rated at 60 mA, to 28 Vdc
	Lamps rated at 80 mA, to 18 Vdc
	Lamps rated at 100 mA, to 12 Vdc
	T^2L Level Compatible (2-unit loads)
Response Time:	Rise Time — 10 μs (Resistive load without
	Fall Time — 0.5 μs field wiring)
Logic to Field Transfer:	A logic 1 will provide current sinking ability
Signal Conditioning:	W403 only
Timing Ranges:	0.5 ms to 80 ms — Short Range
	80 ms to 2 sec — Long Range
	(Adjustable on a per bit basis)
Recovery Time:	0.05 ms — Short Range
	2 ms — Long Range

08-0698
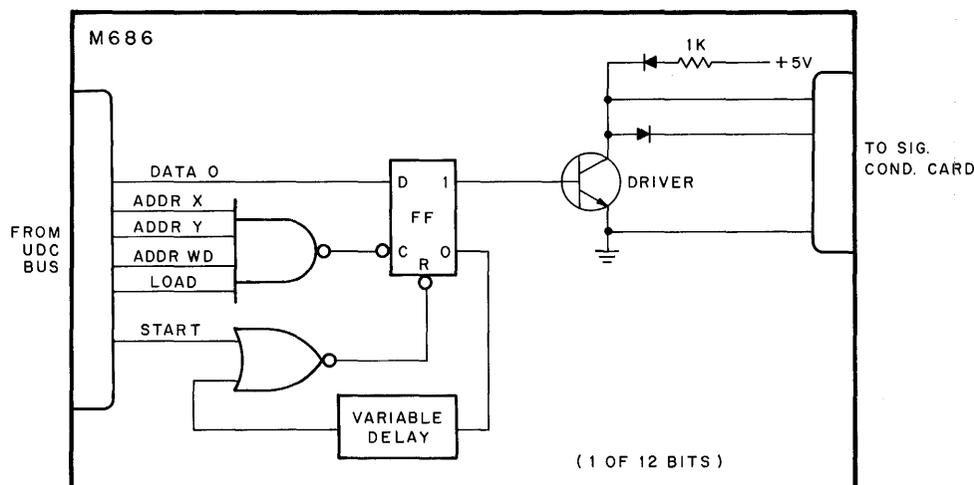
Figure 4-17   Simplified Schematic Diagram (M686)

DESCRIPTION

The M686 Single-Shot Driver Output Module (Figure 4-17) provides 12 individually adjustable solid-state pulse outputs. As noted for the M684, the M686 can be used to drive solid-state logic or as a current driver. The delay circuit is turned on using a Load Data IOT. The pulse duration for each output point is continuously adjustable from 0.5 ms to 80 ms. A connecting jumper allows this range to be increased between 80 ms and 2.0 seconds. The pulse duration will be set to 60 ms when delivered from the factory. The locations of the pulse duration trimpots and jumpers are shown in Figure 4-18. The recovery time of the single-shots is 0.05 ms when operating in the low range, and 2.0 ms when operating in the upper range. This recovery time determines the maximum repetition rate per point.

MODULE JUMPER CONFIGURATION

Jumpers are required for range selection of the timeout. The long timeout range is selected when the jumper is installed (Figure 4-18).
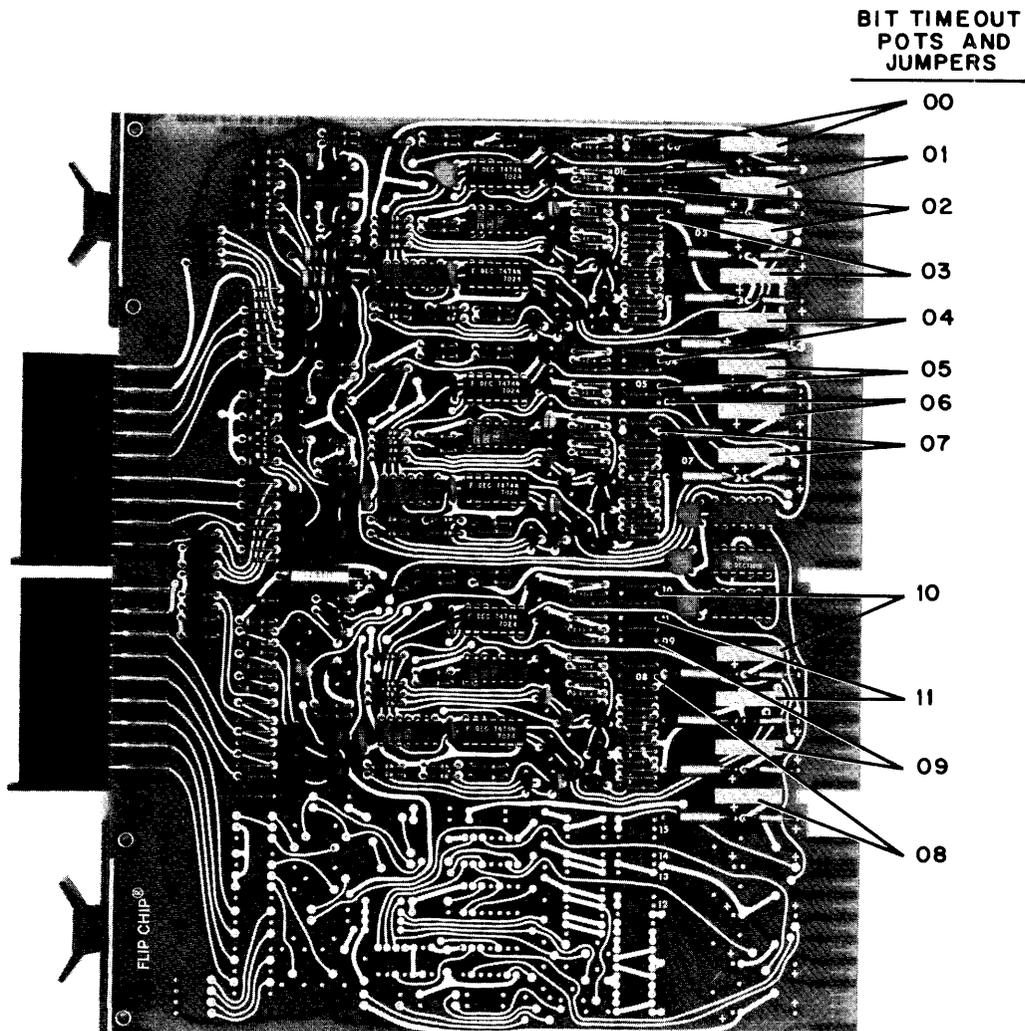
Figure 4-18   Location of Bit Timeout Potentiometers and Jumpers (M686)

4-34

LATCHING RELAY OUTPUT MODULE

FUNCTIONAL SPECIFICATIONS

|	
Power Requirements	+5V @ 0.5A max
Relay Type:	Mercury-Wetted Form C, Magnetic Latching (NO or NC contacts available at screw terminals)
Switching Specification:	250V, 2A (100 VA max)
Response Time:	3 ms max
Logic to Field Transfer:	Logic 1 closes NO contacts
Signal Conditioning:	W400 or W402, arc suppression is required (Paragraph 4.6)
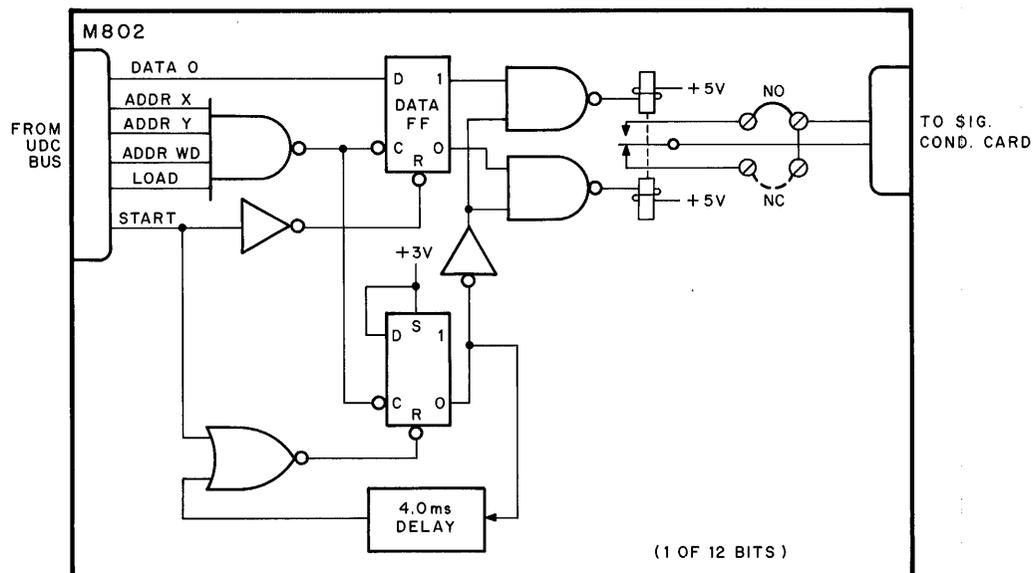
Figure 4-19 Simplified Schematic Diagram (M802)

DESCRIPTION

The M802 Latching Relay Output Module (Figure 4-19) provides "fail-safe" operation of 12 electrically isolated, normally open or normally closed mercury-wetted relay outputs. Magnetically latched relays remain set in event of power failure, ensuring continuity and integrity of field circuits.

The register on the module is loaded by the Load Data IOT. The Load Data IOT generates a 4-ms pulse which is used to energize the relay coils in accordance with the input data. During this period, the latching relays will change state in approximately 3.0 ms (without bounce) and remain in that state until changed under program control.

MODULE JUMPER CONFIGURATION

The board is manufactured and tested with a jumper in place; the normally open (NO) contact, and common is therefore the active pair (Form A). The normally closed (NC) contact may be used with the common as the active pair (Form B) by removing the existing jumper and inserting it in the adjacent set of split lugs. The jumper change can be made on a per point basis (Figure 4-20).
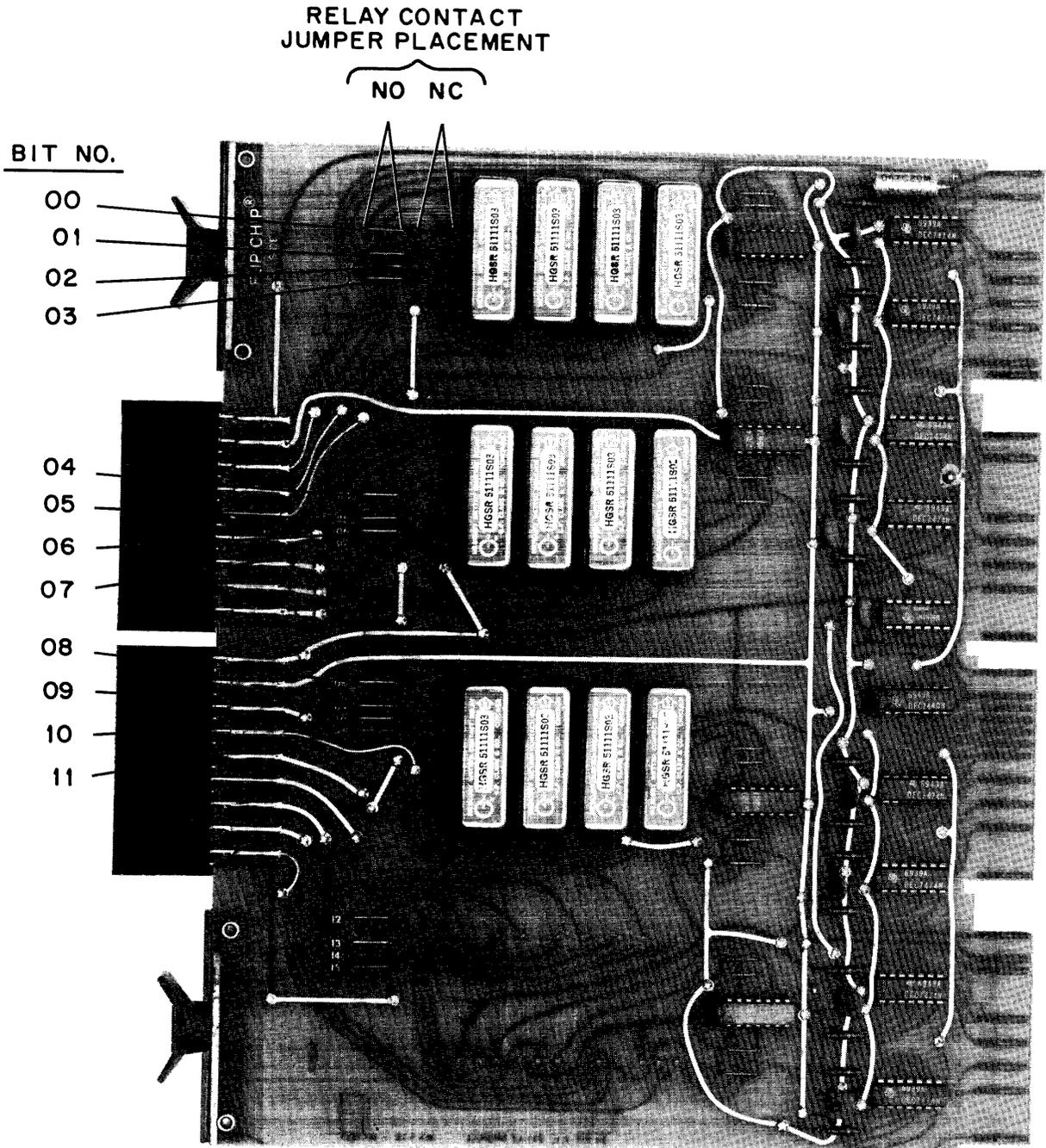

RELAY CONTACT JUMPER PLACEMENT

00-NC
00-NO
01-NC
01-NO
02-NC
02-NO
03-NC
03-NO
04-NC
04-NO
05-NC
05-NO
06-NC
06-NO
07-NC
07-NO
08-NC
08-NO
09-NC
09-NO
10-NC
10-NO
11-NC
11-NO
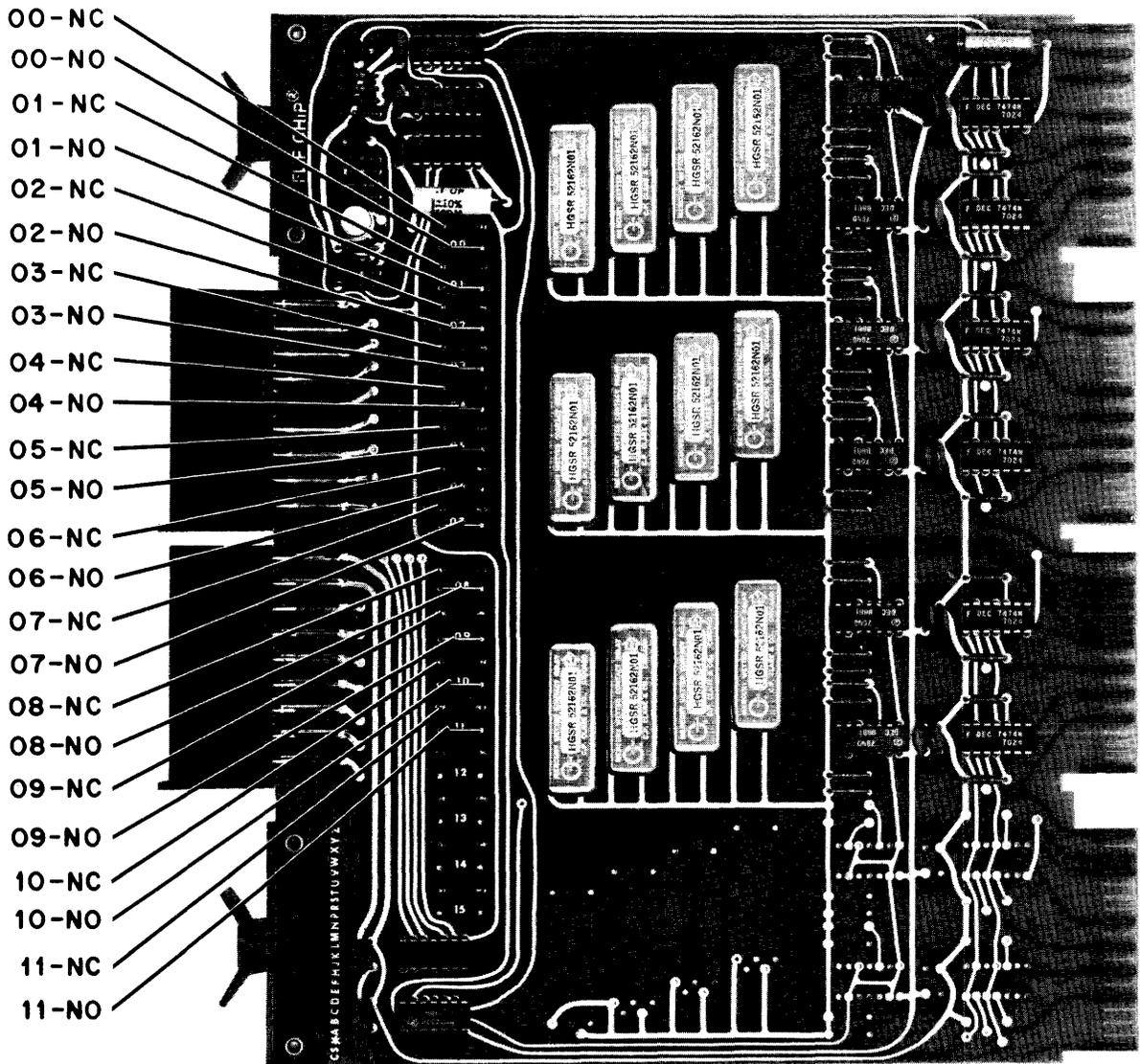
Figure 4-20   Location of Bit Relay Contact Jumpers (M802)

4-36

FLIP-FLOP RELAY OUTPUT MODULE

FUNCTIONAL SPECIFICATION

Power Requirements: +5V @ 0.5A max

Relay Type: Mercury-Wetted Form C
                                      (NO or NC contacts available at screw terminals)

Switching Specifications: 250V, 2A (100 VA max)

Response Time: 3 ms max

Logic to Field Transfer: Logic 1 closes NO contacts

Signal Conditioning: W400 or W402 — arc suppression is required (Paragraph 4.6)

08-0700
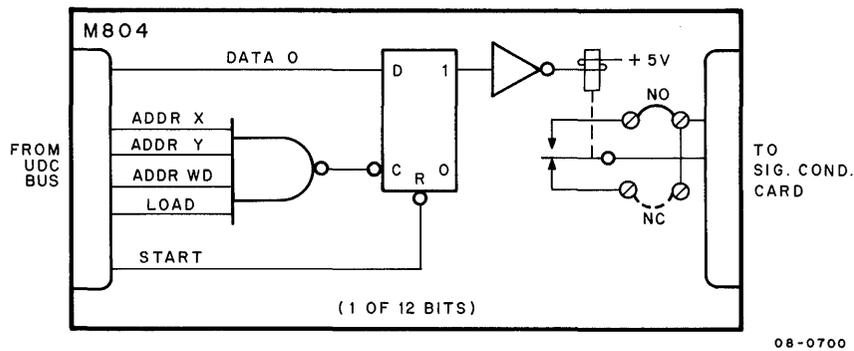
Figure 4-21   Simplified Schematic Diagram (M804)

DESCRIPTION

The M804 Flip-flop Relay Output Module (Figure 4-21) provides 12 electrically isolated, normally open or normally closed mercury-wetted relay output contacts for buffered control of relays, contactors, displays, lamps, etc. The module is supplied with a jumper in place so that the NO and common contacts are the active pair (Form A). The NC and common contacts can be used as the active pair (Form B) by removing the existing jumper and inserting it in the adjacent set of split lugs. This jumper change can be made on a per point basis.

The relays are driven by a flip-flop register which is loaded by a Load Data IOT. A logical 1 energizes the relay coil in approximately 3.0 ms (without bounce), which remains energized until reset by a logical 0 being loaded or a power failure.

MODULE JUMPER CONFIGURATION

The board is manufactured and tested with a jumper in place; the normally open (NO) contact and common is, therefore, the active pair. The normally closed (NC) contact can be used with the common as the active pair (Form B) by removing the existing jumper and inserting it in the adjacent set of split lugs. This jumper change can be made on a per point basis (Figure 4-22).

Figure 4-22   Location of Bit Relay Contact Jumpers (M804)

SINGLE-SHOT RELAY OUTPUT MODULE

FUNCTIONAL SPECIFICATION

Power Requirements:	+5V @ 0.75A max
Relay Type:	Mercury-Wetted Form C (NO or NC contacts available at screw terminals)
Switching Specification:	250V, 2A (100 VA max)
Response Time:	3 ms max
Logic to Field Transfer:	Logic 1 closes NO contacts
Timing Ranges:	0.5 ms to 80 ms — Short Range 80 ms to 2 sec — Long Range (Adjustable on a per bit basis)
Recovery Time:	Recovery time is always less than response time of relay
Signal Conditioning:	W400 or W402, arc suppression is required (Paragraph 4.6)
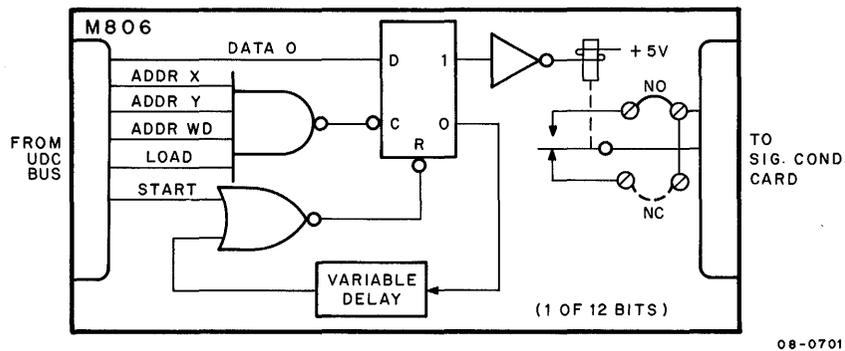
Figure 4-23 Simplified Schematic Diagram (M806)

DESCRIPTION

The M806 Single-Shot Relay Output Module (Figure 4-23) provides 12 electrically isolated, momentary, normally open or normally closed, mercury-wetted contact outputs for initiating alarms, lamps, field relays, etc. The module is supplied with a jumper in place so that the NO and common contacts are the active pair (Form A). The NC and common contacts can be used as the active pair (Form B) by removing the existing jumper and inserting it in the adjacent set of split lugs. The jumper change can be made on a per point basis.

The relays are driven by single-shots which are triggered by the Load Data IOT. A logical 1 energizes the relay coil for the preset pulse duration, thereby operating the output relay contacts for that period of time. The

duration of the contact closure for each output point is continuously adjustable from 0.5 ms to 80 ms. Connecting a jumper in the variable delay circuit allows this range to be increased to between 80 ms and 2.0 seconds. The duration will be set to 60 ms when delivered from the factory. The location of the pulse duration trimpots is shown in Figure 4-24.

MODULE JUMPER CONFIGURATION

Timeout Range — Jumpers are required for Range selection of timeout. The long timeout range is selected when the jumper is installed (Figure 4-24).

Relay Contact — The board is manufactured and tested with a jumper in place; the normally open (NO) contact and common is, therefore, the active pair. The normally closed (NC) contact can be used with the common as the active pair (Form B) by removing the existing jumper and inserting it in the adjacent set of split lugs. This jumper change can be made on a per point basis (Figure 4-24).

BIT RELAY CONTACT
JUMPER PLACMENT

BIT TIMEOUT POTS
AND JUMPERS
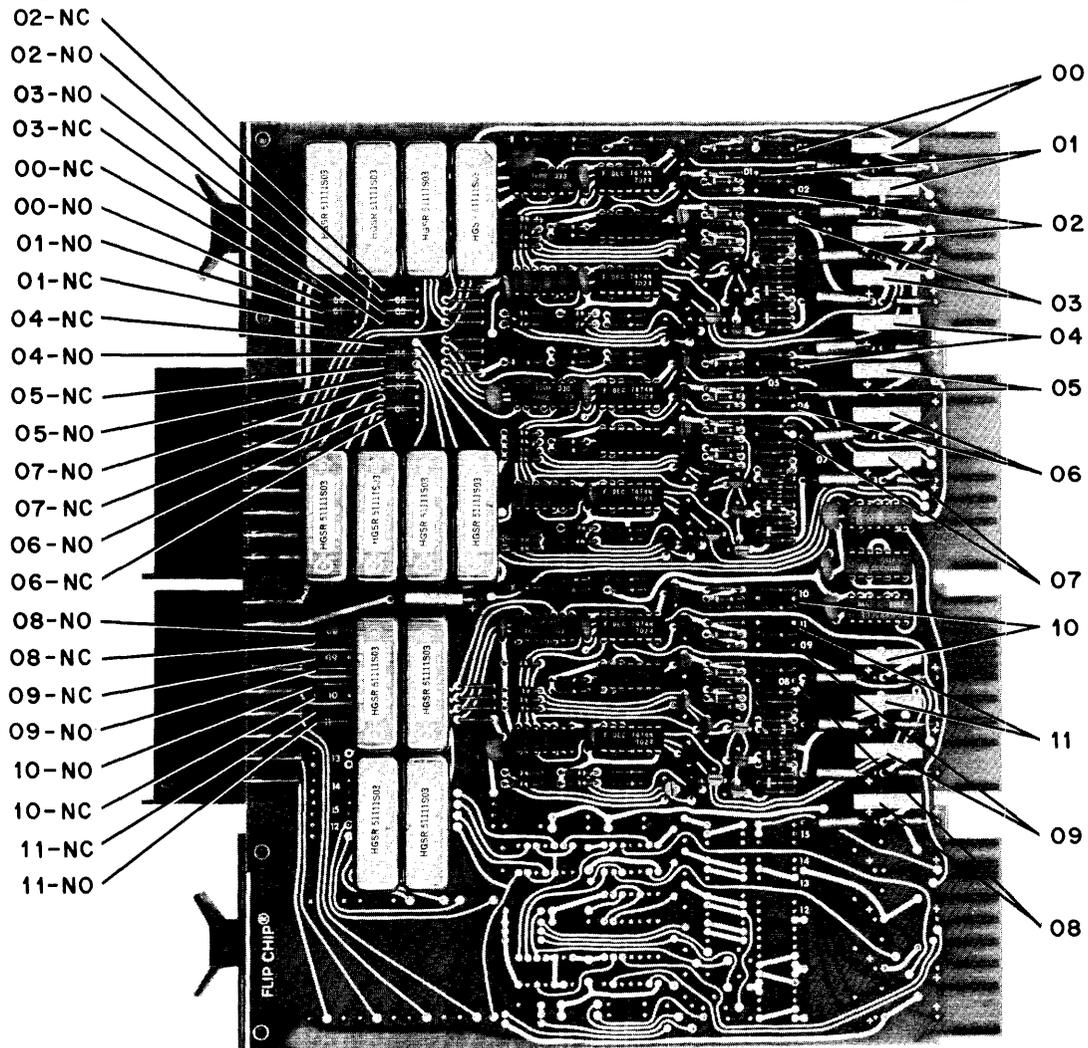
Figure 4-24   Location of Bit Timeout Potentiometers and Jumpers
and Relay Contact Jumpers (M806)

4-40

D/A CONVERTER OUTPUT MODULE

FUNCTIONAL SPECIFICATIONS

Resolution:	One part in 1024 of full scale
Digital Input (CH0):	0000 = 0 output
	1000 = 1/2 full-scale output
	1777 = full-scale output (−1 LSB)
Analog Output:	0V to −10V at 3 mA max
Gain Accuracy:	Adjustable to within ± 0.05% of full scale at 25°C
Zero Offset:	Adjustable through zero
Settling Time:	35 μs max to within ± 0.05% of final value with 150 pF load.
	50 μs with signal-conditioning module.
Linearity:	± 1/2 LSB
Power:	+5V ± 0.25V 450 mA max
	+18V ± 0.01V 147 mA max
	−18V ± 0.01V 30 mA max
	Power is supplied from an external H738A supply and applied through the screw terminals. One H738A supply will supply the necessary power to four A633 DACs and to its signal-conditioning modules.
Signal Conditioning:	Four output signal-conditioning modules are available for use with the A633 DAC Modules.
	A233 0V to +10V output at 15 mA max*
	A234 +1V to +5V output at 15 mA max*
	A235 4 mA to 20 mA into 750 Ω max*
	A236 10 mA to 50 mA into 300 Ω max*

DESCRIPTION

The A633 DAC Module contains four 10-bit D/A converters, with input buffer registers, ladder networks, output voltage amplifier, and a reference supply (Figure 4-25).

There is also a power low circuit on the module, which grounds the input load signal in the event that computer power is low or is lost. This feature is available for the user who cannot afford to lose analog output during a power failure and has the converter connected to an auxiliary back-up supply.

The module operates like any digital output module in the UDC System. The 12-bit input data word is divided into two major parts: the DAC data word (bits 02 through 11) and the channel select code (bits 0 and 1). The 2-bit channel select code determines which D/A channel will be selected.

---

*The outputs from the signal-conditioning modules are single-ended outputs. Therefore, the loads should be the type that can be grounded to the analog ground, which, in turn, is connected to system ground in the UDC.

Bit 0	Bit 1	Channel
0	0	00
0	1	01
1	0	02
1	1	03

The complete 12-bit data word can be loaded on the D/A module at one time. Channel selection must be updated at each data word transfer. There are no status bits on the module; therefore, enough time must be allowed between conversions for settling time purposes.

DATA FORMAT

0	1	2	3	4	5	6	7	8	9	10	11

CHAN SEL   10 BIT DATA
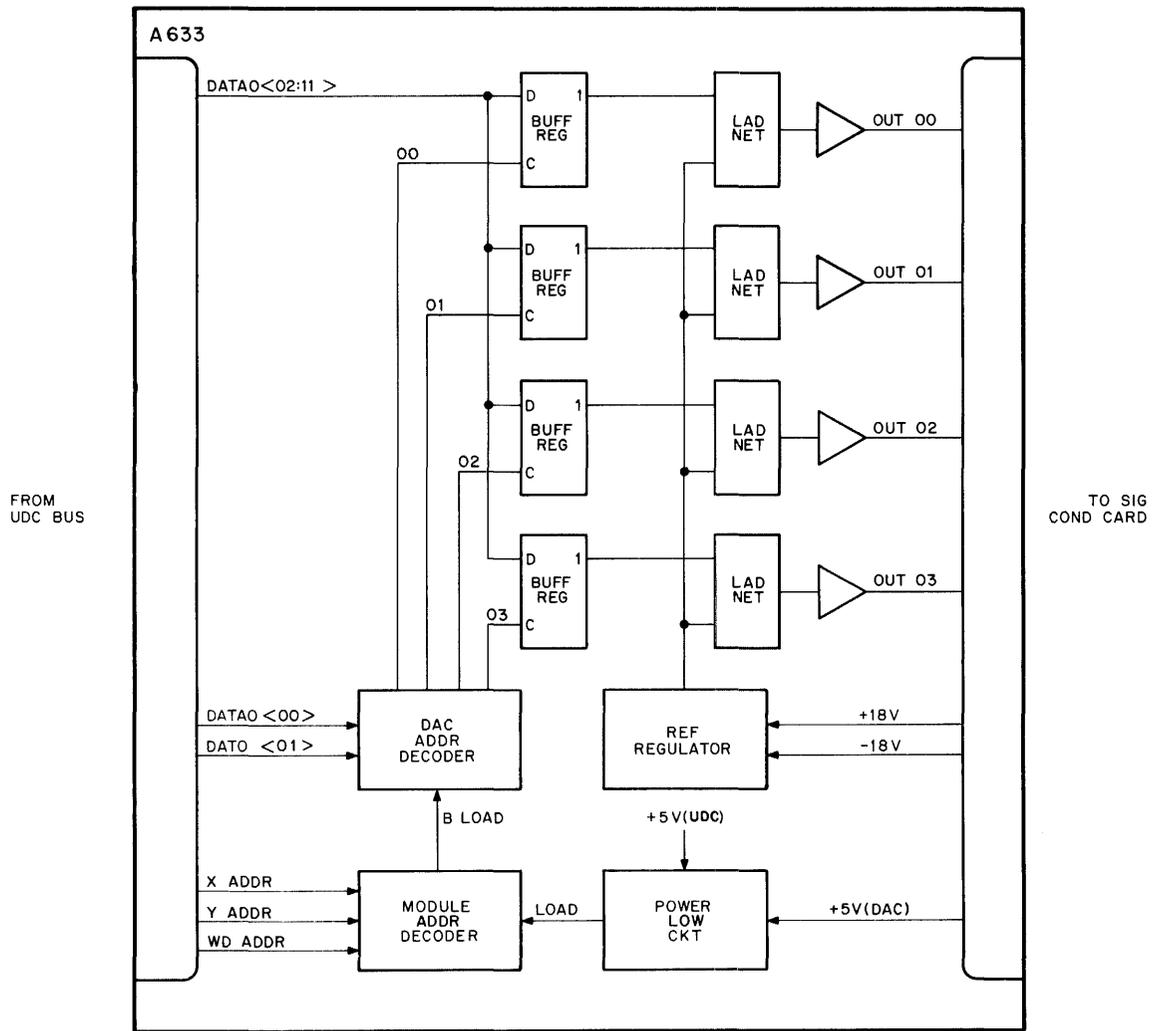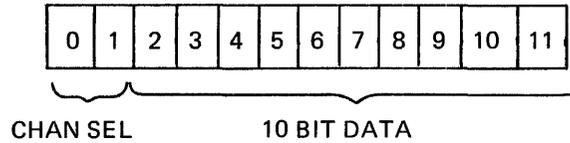
Figure 4-25 Simplified Schematic Diagram (A633)

4-42

MODULE JUMPER CONFIGURATION

The only jumpers provided are those needed for use with a battery or back-up power supply. (Figure 4-26)

Function	Jumper
Battery or Backup Supply	W1
Normal Operation	W2

When the battery or back-up supply is used, the start signal is inhibited from clearing the DACs during power restoration.

MODULE ADJUSTMENTS

All module adjustments are made at the factory. However, if there is a need for readjustment, the A-SP-BA633-0-2 DAC Checkout Procedure should be consulted.
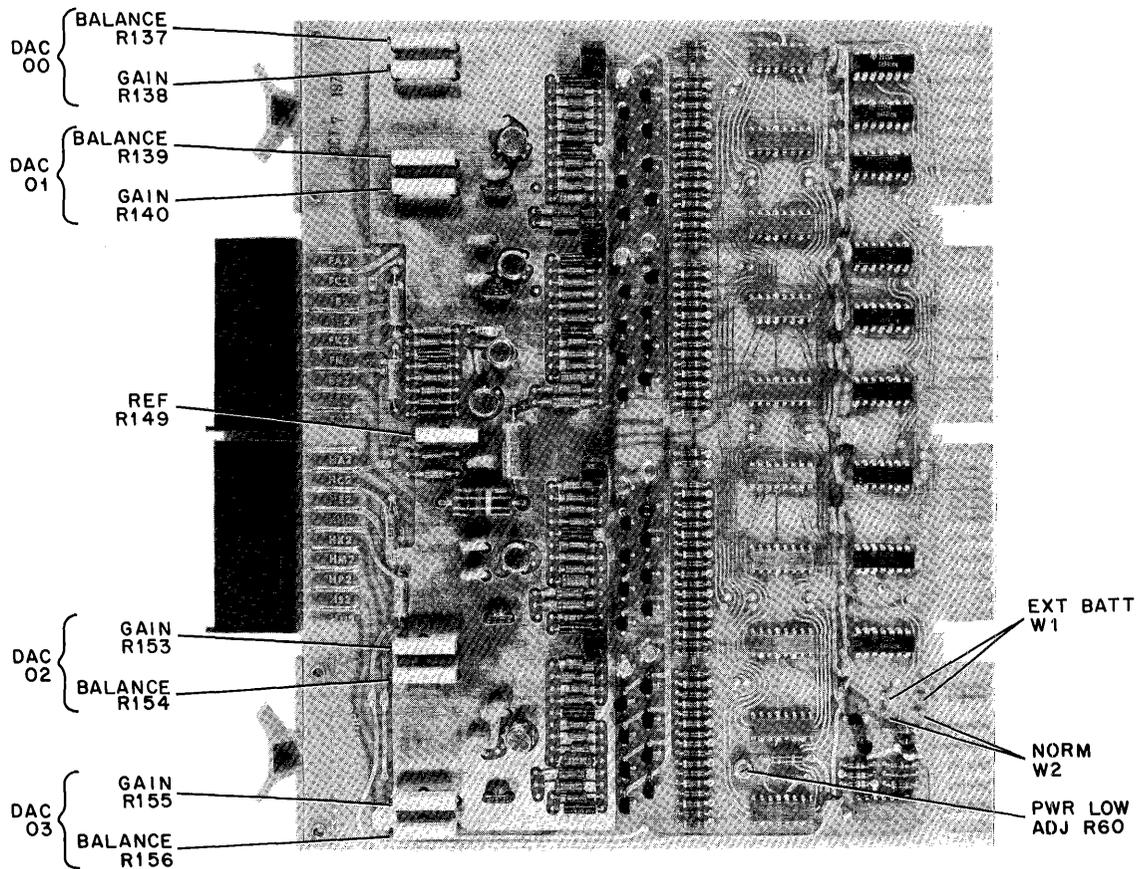
Figure 4-26   Location of Adjustments and Jumpers (A633)

FUNCTIONAL SPECIFICATIONS

Counter Type: 16-bit asynchronous binary up-counter buffered with anti-coincidence circuitry. Read/Write

Power Requirements: +5V @ 1A max

Counter Inputs: Selectable by PC switch

PC Switch Position	Input
1	Contact Input (CONT)
	$10^9 \Omega$ min, 250V, input isolation 6V ± 10% @ 18.5 mA input voltage 100 Hz max input frequency
2	Voltage Input (CV)
	"0" = 0.7V max "1" = +1.4V to 3.5V 25 kHz max input frequency
3	CL00 UDC internal clock (175 Hz to 1.75 kHz adjustable)
4	CL01 UDC internal clock (1.75 kHz to 17.5 kHz adjustable)
5	CLL line frequency clock
6	No input (Ground)

External Enable (EN):   Enabled = 0.7V max; not enabled = 1.4 to 35V

Counter Outputs: Pulse (P)
Control (C)
Sign (S)

Output Drive Capability: Resistive Load: 55 Vdc @ 250 mA
Inductive Load: 55 Vdc @ 250 mA
(Diode Suppression Supplied)
Incandescent Lamps: Lamps rated at 40 mA to 48 Vdc
Lamps rated at 60 mA to 28 Vdc
Lamps rated at 80 mA to 18 Vdc
Lamps rated at 100 mA to 12 Vdc
T^2L Compatible (2 unit loads)

Pulse (P) Output Characteristics: Frequency (At system counting frequency)
CLK 00: 175 Hz to 1.75 kHz, adjustable
CLK 01: 1.75 kHz to 17.5 kHz, adjustable
CLK L: Line frequency

FUNCTIONAL SPECIFICATIONS (Cont)

Width (Adjustable in four ranges)

RANGE 1: 20 μs to 112 μs
RANGE 2: 112 μs to 630 μs
RANGE 3: 630 μs to 3.5 ms
RANGE 4: 3.5 ms to 20 ms

Logic to Field Transfer:

All outputs are enabled when sinking current.

Address Restriction:

Due to the fact that the buffer update is inhibited while the W734 Counter is addressed, the module should not be located in address slot 000.
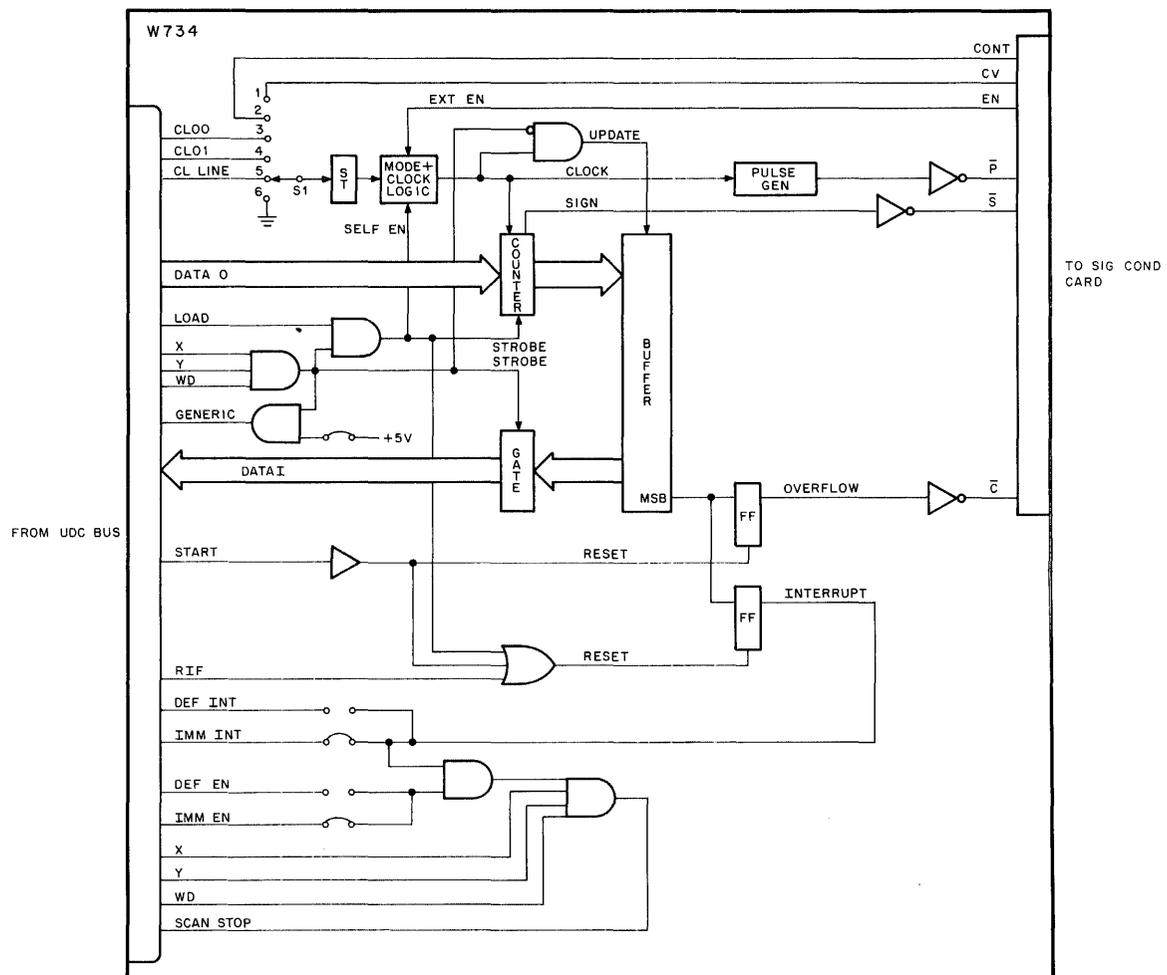
11-0976

Figure 4-27 Simplified Schematic Diagram (W734)

4-46

DESCRIPTION

The W734 Counter Module (Figure 4-27) is a 12-bit (optionally 16-bit) asynchronous binary up-counter. An output buffer register is updated after each counter increment. When the module is addressed (under program control) the buffer update is inhibited, preventing any data change. A full 12-bit data word can be parallel loaded into the counter, allowing the counter to be preset under program control. To use the counter as a down-counter, the 2's complement of a number must be loaded.

One of five inputs, selectable by a PC mounted switch, can be selected for incrementing the counter. Two are external event inputs and three are internal UDC clock inputs. The external inputs include a contact sensing input and a voltage input.

An enable/disable jumper is provided to select either an external enable or an internal self-enable to start the counter after each preload. Upon overflow, the counter generates an interrupt and can continue or stop counting. A jumper is provided to inhibit the counter on interrupt.

The counter provides three solid-state outputs: pulse, control, and sign. The pulse output is a pulse train whose frequency is determined by the counter clocking frequency (counter input) and whose pulse width is established by a jumper and a potentiometer. The control output goes true whenever the counter is enabled. The sign output is available when the counter is set up (by jumper) for 11 bit plus sign operation.

MODULE CONFIGURATION

Setting the counter up for a specific application is a user task. Therefore, the user should familiarize himself with the various operating modes of the counter.

FUNCTIONAL MODES

ENABLE (External/Self)

Two methods are available for enabling the counter: external and self. In the external enable mode, a signal at the EN screw terminals will enable the counter. If a count signal is present at the time the counter is enabled it will not be counted. This mode is useful when external event synchronization is required to start the count. If the counter is set up to operate in the self-enable mode, power up, system initialization or presetting the counter will start the counter. Then, upon OVERFLOW, the counter is disabled or continues counting depending on jumper setup. The counter starts counting from zero or from the count loaded.

OVERFLOW (Halt/Continue)

The module can be set up to halt or continue counting on OVERFLOW. In either case, an interrupt signal is issued by the counter.

SIGN OUTPUT

The module can be set up to provide for a direction bit by selecting the SIGN option. With this option selected, the module becomes a 11-bit counter with a sign bit, and overflow will occur when counter bit 10 (the 11th bit) overflows. The SIGN ("S") output is available at the screw terminals as a solid state driver (open-collector) output.
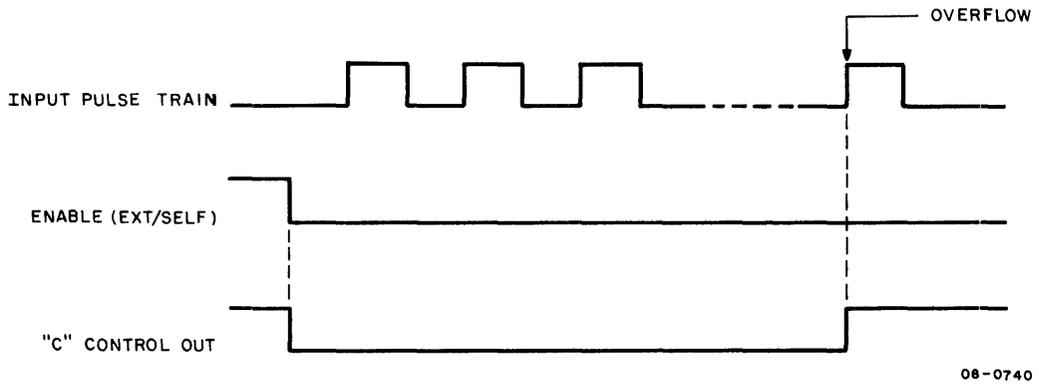
COUNTING MODES

The module is able to count events or periods depending on which jumper is installed. Event and period counting is shown in the following illustration.

08-0739
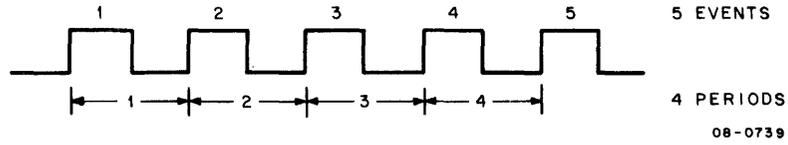
The control output ("$\overline{C}$") from the module behaves uniquely for each of the two counting modes.

EVENT Counting

In this counting mode, the control output becomes TRUE when the counter is enabled and NOT TRUE on counter OVERFLOW as illustrated in the following timing diagram.

08-0740

PERIOD Counting

In this counting mode the control output becomes TRUE at the first count and NOT TRUE on counter OVERFLOW as illustrated in the following timing diagram.

08-0741
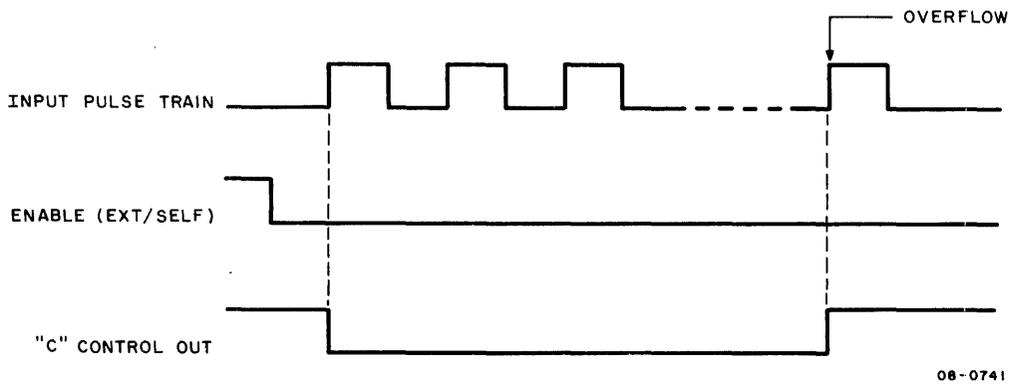
NOTE
OVERFLOW will occur when counter bit 10 or 11
(depending on SIGN option selection) overflows.

4-48

OPERATIONAL MODES

The counter must be set up to operate as an interrupting I/O module in a UDC System. Therefore, the desired *GENERIC code* and *interrupt level* (IMM or DEF) must be established and selected. In addition, the desired *counter input* (clock) and output *pulse width* must be selected to place the counter in operation.

INTERRUPT Levels

The desired interrupt level must be chosen by installing the proper jumper on the counter module. Like all UDC interrupt modules, immediate and deferred interrupt level declarations are available for selection.

GENERIC Code

Since the counter can be used for a variety of functions, the following four GENERIC codes have been assigned to the counter module.

GENERIC Code	0123
	0100
	0101
	0110
	0111

One of these codes can be selected by installing the proper jumper(s) on the counter module.

CLOCK Selection

The input clock or counter input is selected by setting PC switch S1 to the desired position. The switch positions and the corresponding counter inputs are as follows:

Switch Position	Input
1	CONTACT
2	VOLTAGE
3	CL 00
4	CL 01
5	CL LINE
6	GROUND

Position 6 should be selected if the counter is used as a data storage or transfer buffer without being clocked.

OUTPUT PULSE WIDTH

The width of the pulse output ("$\overline{P}$") is continuously adjustable from 20 μs to 20 ms in four ranges. Thus to obtain the desired width, the proper range must be selected by installing the correct jumper and potentiometer R32 must be adjusted. The four ranges are:

RANGE 1: 20 μs to 112 μs
RANGE 2: 112 μs to 630 μs
RANGE 3: 630 μs to 3.5 ms
RANGE 4: 3.5 ms to 20 ms

MODULE JUMPER CONFIGURATIONS

Table 4-6 and Figure 4-28 identify the required jumper for each counter mode. Using the table, the user should make sure that the proper jumpers for the desired modes of operation are installed on the module.

Table 4-6
Jumper Options (W734)

Module Jumpers		W1 or W2	W3	W4 or W5	W6	W7	W8	W9	W10	W11	W12 or W13	W14	W15 or W16	W17	W22 or W18	W19	W29 and W20	W30 and W21	W23	W28 or W24	W25	W27 or W26
FUNCTIONAL MODES																						
EXTERNAL ENABLE																				X		
SELF ENABLE																			X			
HALT ON OVRFL															X							
CONTINUE ON OVRFL																X						
SIGN BIT														X								
COUNTING MODES																						
EVENT COUNT																	X					
PERIOD COUNT																		X				
OPERATIONAL MODES																						
IMM INT		X		X																		
DEF INT			X		X																	
GEN CODES	0100										X		X									
	0101									X			X									
	0110										X	X										
	0111									X		X										
PULSE RANGE	RANGE 1					X																
	RANGE 2						X															
	RANGE 3							X														
	RANGE 4								X													
12 BIT OPERATION																					X	
16 BIT OPERATION																						X

4-50

PULSE WIDTH
RANGE W7-W10

PULSE
WIDTH
R32

GEN3
W11-W12

GEN2
W14-W15

SIGN
W17

EVENT
COUNT
W29

CONTINUE
ON OVERFLOW
W19

PERIOD
COUNT
W21

EXTERNAL
ENABLE
W24

12 BITS
W25

16 BITS
W26

IM EN
W2

DEF EN
W3

PERIOD
COUNT
W30

HALT ON
OVERFLOW
W18

EVENT
COUNT
W20

IM INT
W5

DEF INT
W6

SELF EN
W23

S1 COUNTER
INPUT SWITCH
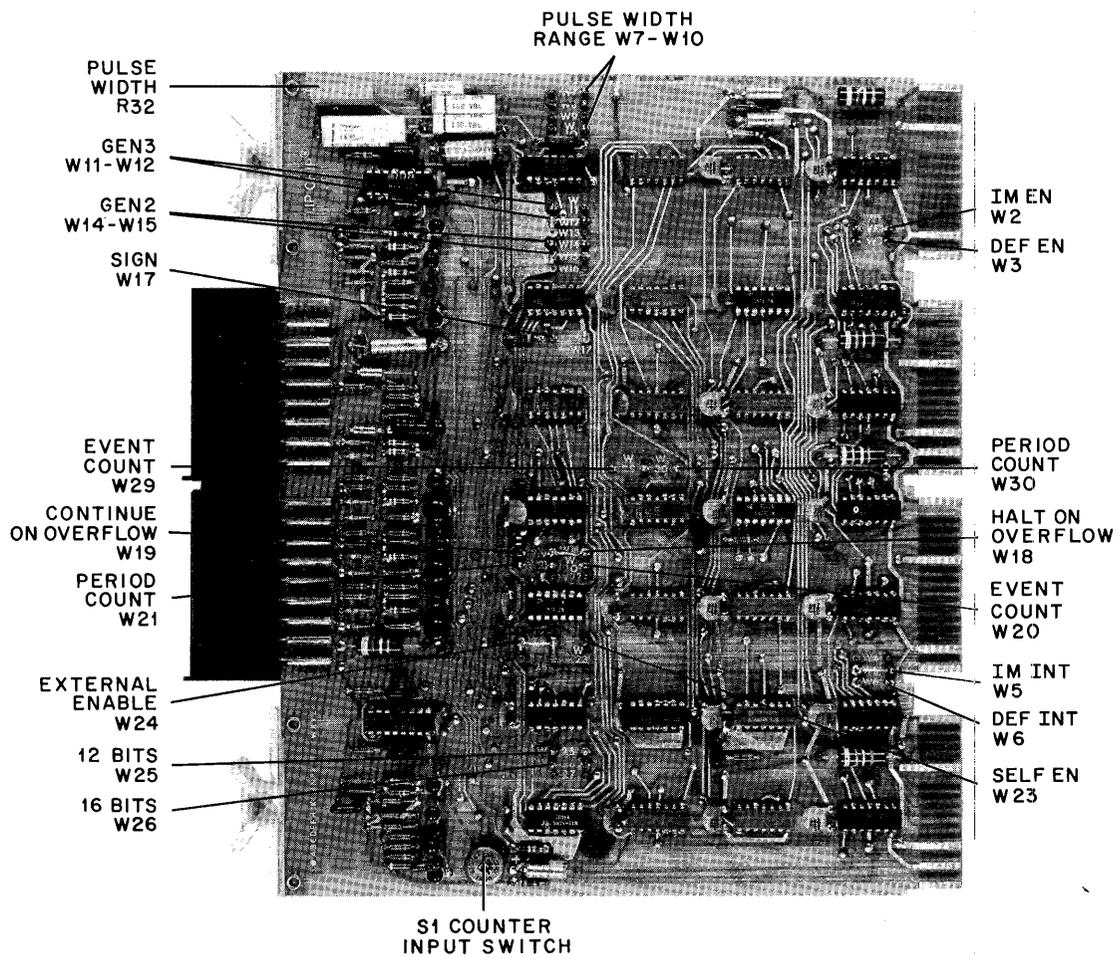
Figure 4-28   Location of Jumpers and Input Switch (W734)

4-51

4.6 SIGNAL CONDITIONING

The signal-conditioning modules serve as the interface between the field devices and the functional I/O modules. These modules plug into the end of the I/O module and accept the BC40C Cable Connector at the handle end. Proper selection of signal-conditioning components and complete understanding and utilization of UDC signal-conditioning options are essential for proper UDC System operation and implementation.

4.6.1 Field Power

In many cases, power from the field will be applied to functional I/O modules for contact sensing and load switching purposes. Two methods of distributing field power to UDC System can be used: common and isolated.

4.6.1.1 Common Power — The common power signal-conditioning module (W402) will distribute a single field power source to all 16 bits on the functional I/O module as shown in Figures 4-29 and 4-30.

4.6.1.2 Isolated Power — The isolated power signal-conditioning module (W400) is used when the field power source for each bit is isolated as shown in Figures 4-31 and 4-32.

4.6.1.3 Driver Output — The driver output signal-conditioning module (W403) provides ground continuity for nonisolated solid-state driver outputs.

4.6.2 Input Module Signal Conditioning for Contact Sensing

The following input modules may be used for contact sensing purposes.

- a. W730
- b. W732
- c. W740
- d. W742

These functional modules require 6V @ 15 mA to drive each of their 12 input circuits. However, the removal of voltage scaling jumpers on the W400 and W402 signal-conditioning modules permits utilization of 24V or 48V as a source power. Table 4-7 defines the jumpers to be cut to permit utilization of higher input voltages. Figures 4-51 and 4-53 identify the location of these jumpers.

Table 4-7
Voltage Scaling Options

Power Source	Jumper
6V	Cut None
24V	Cut A
48V	Cut A and B

4.6.3 Input Module Signal-Conditioning for Logic Level Sensing

The following solid-state input modules can be used for logic level sensing purposes.

- a. W740
- b. W742

TTL, RTL, or DTL logic circuits can be used to supply the logic levels (Figures 4-33 through 4-35). The W400 signal-conditioning module must be used to interface the field logic circuits with the solid-state input modules.
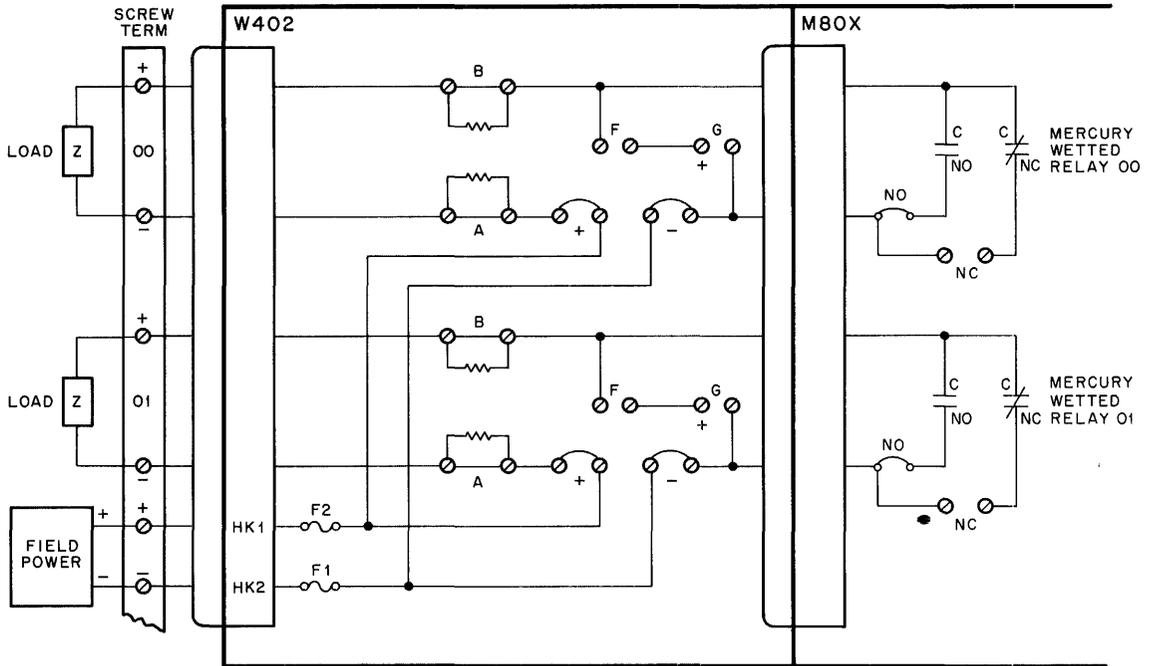
Figure 4-29   Common Power for Load Switching, Wiring Diagram
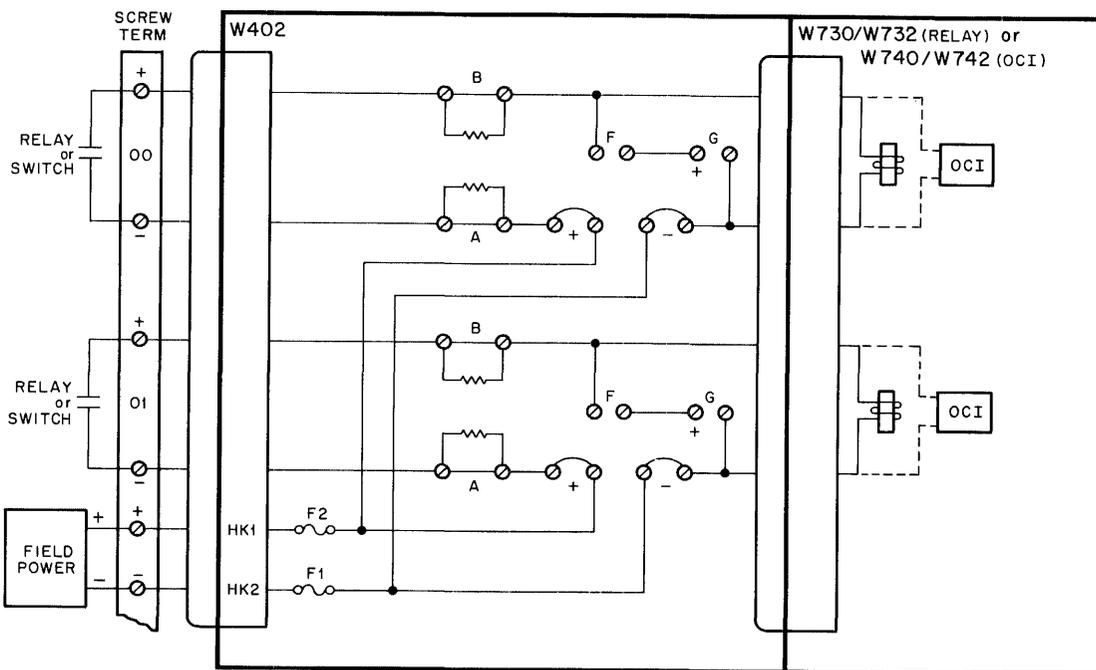
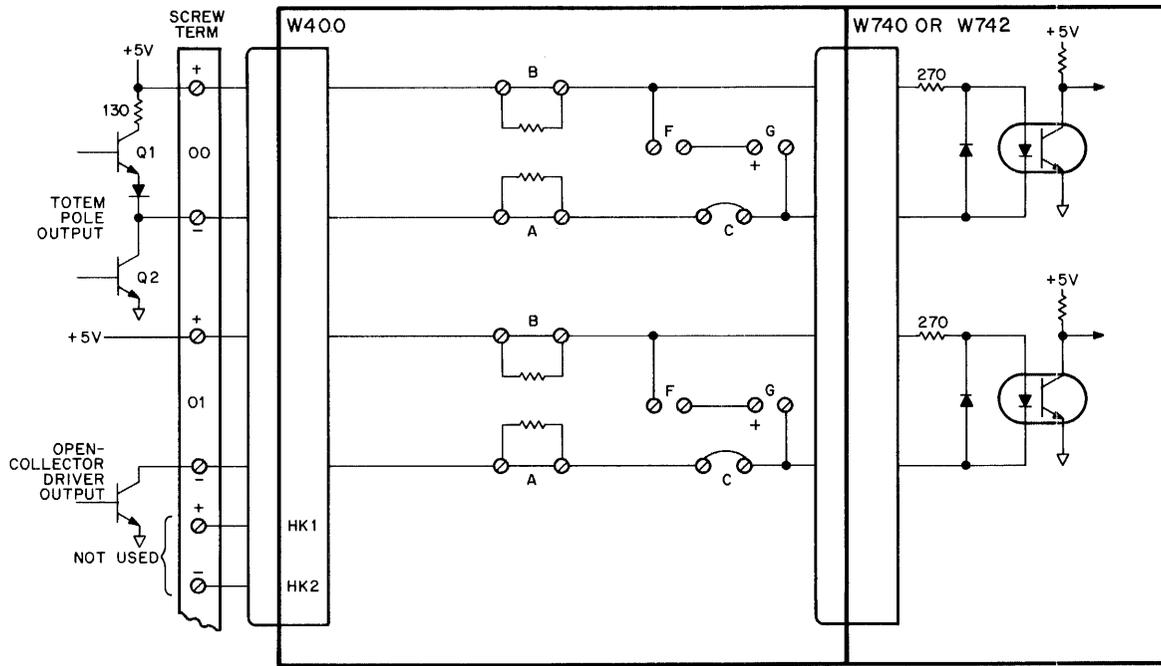Figure 4-30   Common Power for Contact Sensing, Wiring Diagram

4-54
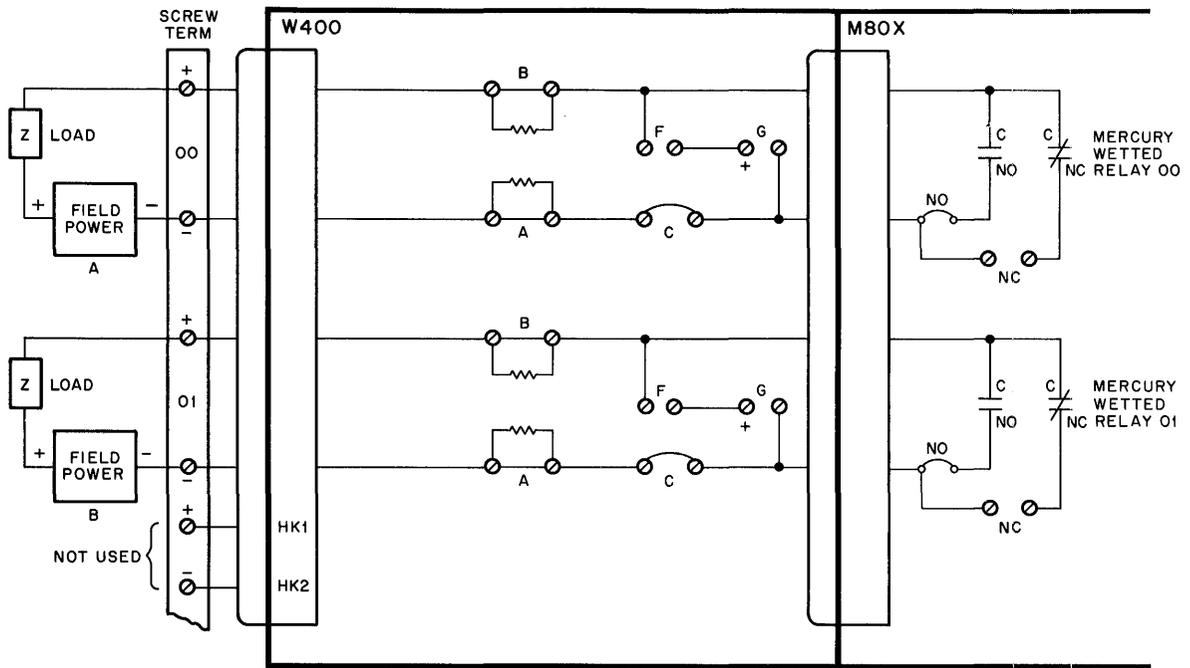
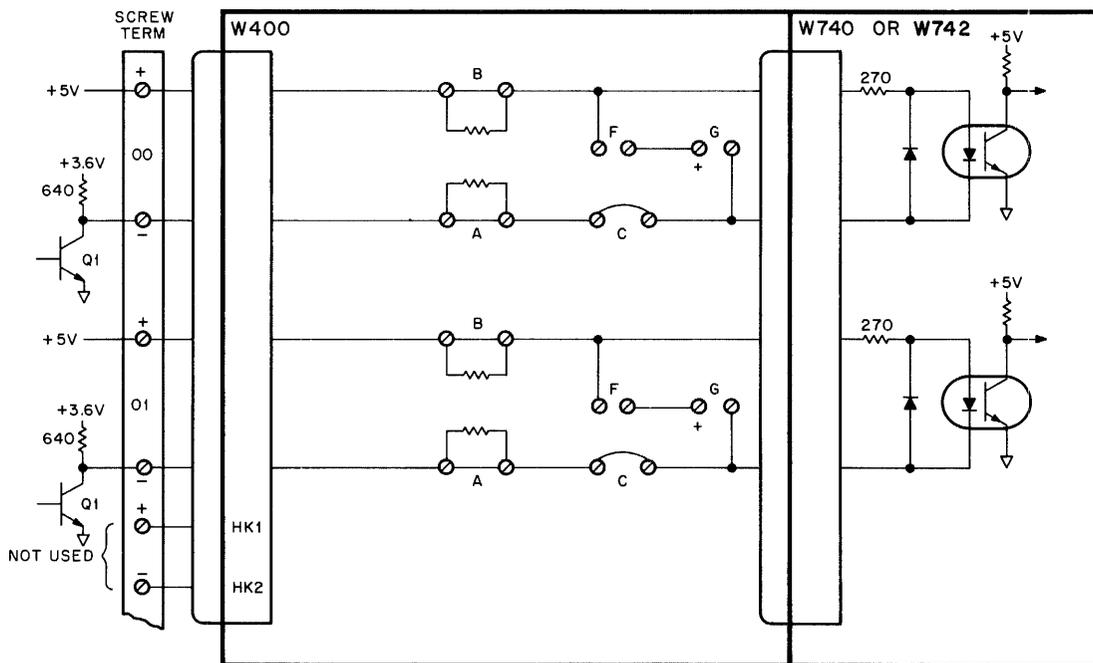Figure 4-31   Isolated Power for Load Switching, Wiring Diagram
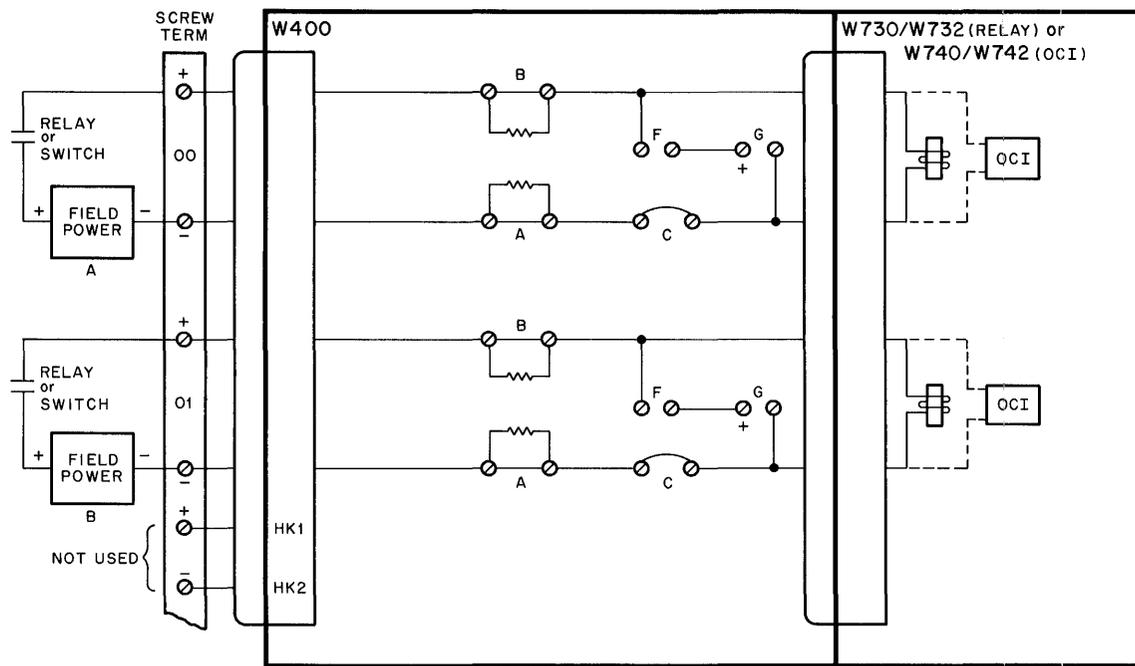
Figure 4-32   Isolated Power for Contact Sensing, Wiring Diagram

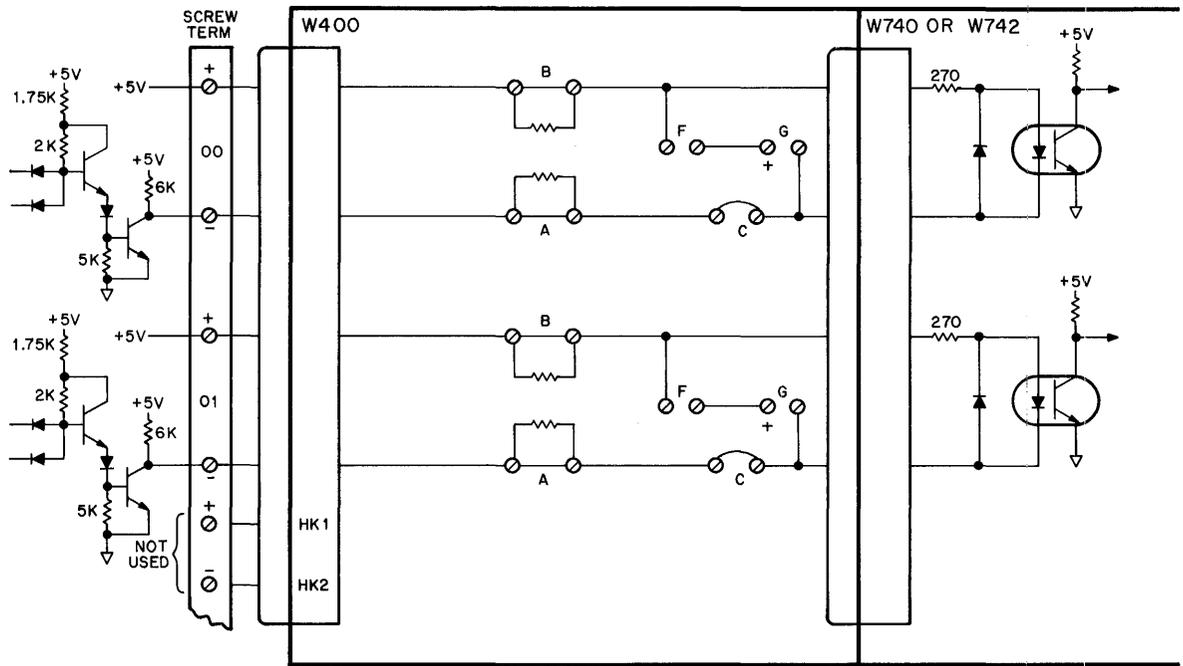4-55

Figure 4-33   Logic Level (TTL) Input, Wiring Diagram

Figure 4-34   Logic Level (RTL) Input, Wiring Diagram

Figure 4-35 Logic Level (DTL) Input, Wiring Diagram

4.6.4 Mercury-Wetted Relay Contact Signal Conditioning

All M800 series functional modules contain 12 mercury-wetted relay outputs. These modules are used for load switching purposes. The contact life expectancy, which can exceed 22 billion operations, depends largely on the use of proper contact protection. Contact protection is required if the contacts are expected to handle energy levels in excess of 40 μJ. This may be represented by the stored energy of a series inductance just prior to opening its circuit or that in a shunt capacitance immediately prior to closing the discharge circuit. In order to handle this and larger energy levels, the following maximum voltage rates and current rises have been set.

    a.   When the contacts close a circuit, the rate of current increase should not exceed 25A/μs.

    b.   When the contacts open a circuit, the rate of change of voltage increase should not exceed 5V/μs.

The arc suppression circuit must bring the rate of current increase and the rate of voltage change increase to the levels specified above. A series RC network across the relay contacts comprises the arc suppression network.

4.6.4.1 Location of the Arc Suppression Network — Space is provided on the W400 and W402 signal-conditioning modules for the RC arc suppression network. The resistor should be installed in field "F" and the capacitor in field "G" (Figures 4-29 through 4-32 and Figures 4-50 and 4-53).

4.6.4.2 Determination of RC — The values of R and C for resistive loads can be determined by using the nomograph and formula presented in Figure 4-36. This nomograph can also be used for reactive loads. However, further transient protection may be required, as discussed in the following paragraphs.

4.6.4.3 Load Consideration — The nature of the load must be carefully considered, especially if the contacts are expected to switch the load current. The following types of loads are commonly used.

4-57

Figure 4-36 Contact Protection Network Nomograph

Reprinted by permission of C.P. Clare & Co., Chicago, Illinois
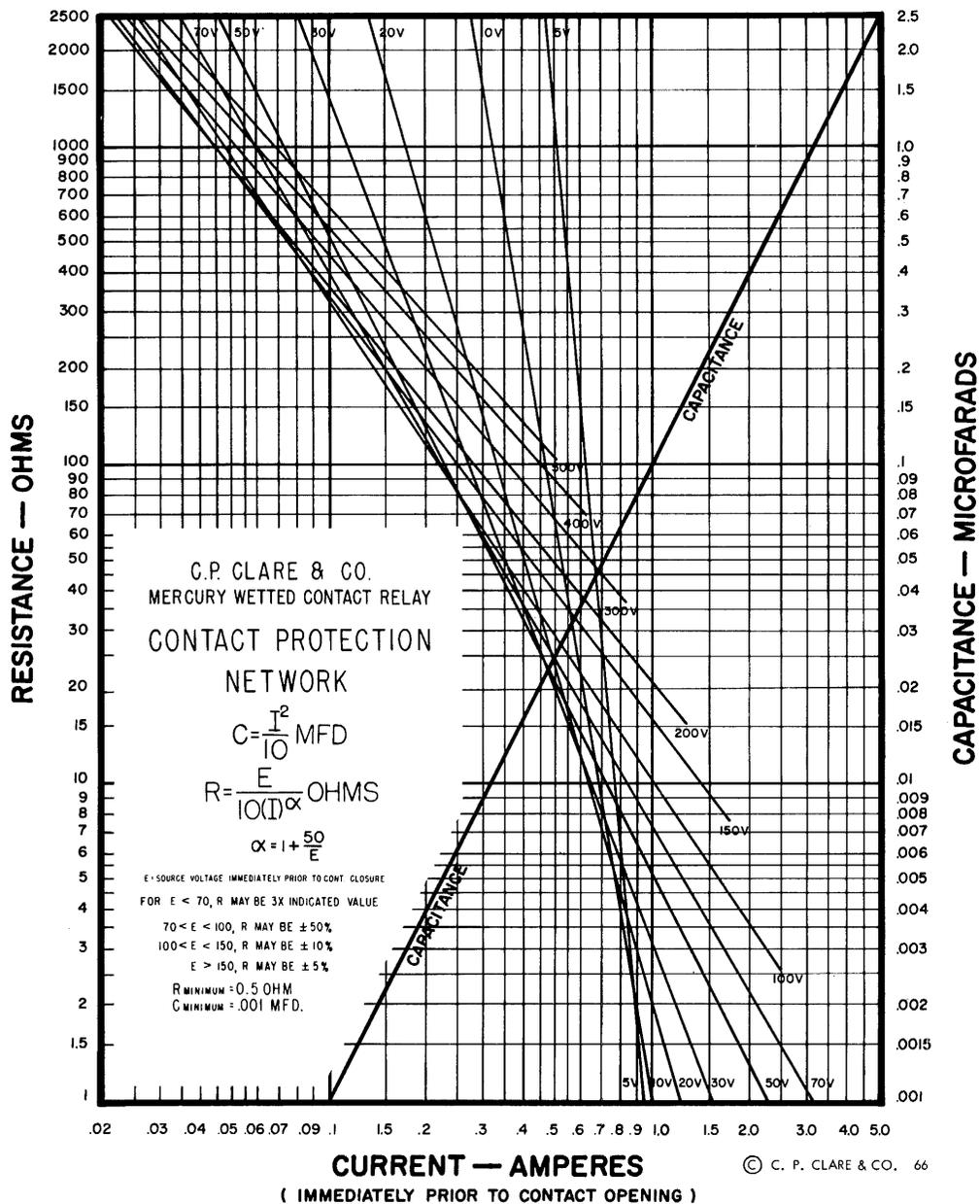
How to Use Nomograph

This nomograph affords a convenient means of determining the necessary contact protection. To determine C, the value of load current is found on the CURRENT axis. Reading directly up to the sloping capacitance line, the value of C is determined from the right hand CAPACITANCE scale. To determine R, read directly up from the load current value to its intersection with appropriate load voltage line. The value of R is then read from the left hand RESISTANCE scale. For AC loads, peak values of current and voltage must be used.

Resistive Loads

Proper arc suppression for resistive loads is relatively easy to accomplish. The RC values as determined by the use of the nomograph and formula will usually provide adequate protection. However, if long lines are run to the load, line inductance may become significant and transient protection may be required.

NOTE
Use peak values in calculating RC when ac power is used for load switching.

DC Inductive Loads

A voltage transient is generated whenever the mecury-wetted relay contacts open and interrupt the current flow in an inductor (Figure 4-37). The instant the contacts open, the inductor behaves like an energy source with

(A) No Arc Suppression

(B) R-C Rate of Rise Protection

(C) Rate of Rise and Transient Protection
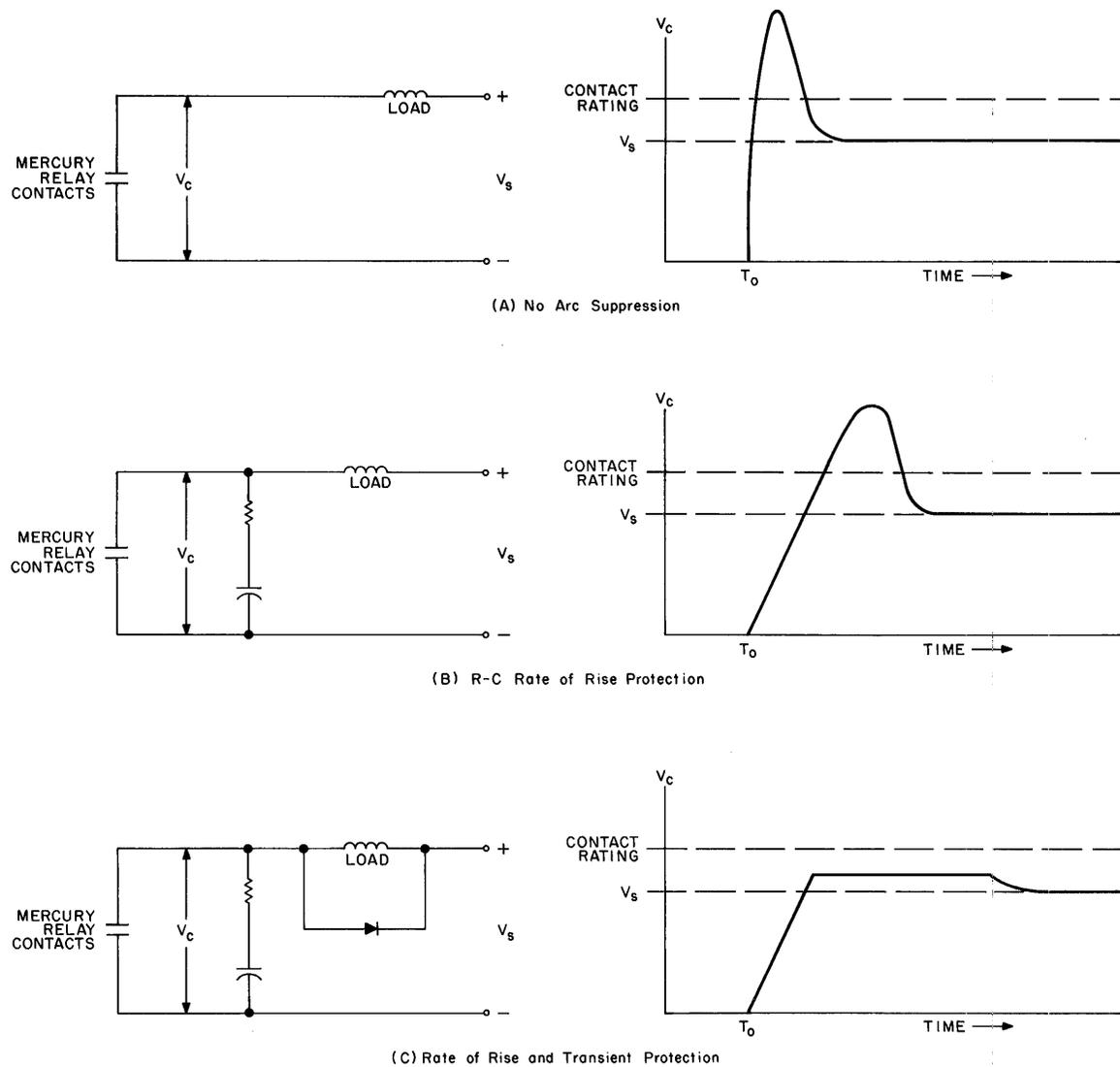
11-0984

Figure 4-37   Arc Suppression Circuit Characteristics

4-59

a high impedance load into which it can dissipate its energy. The high impedance load takes the form of the opening contacts. The voltage across the high impedance load (the contacts) immediately rises to whatever value is necessary for an arc-over to occur, thereby dissipating the energy stored in the inductor. The design objective for this load is to provide control on the rate of current and voltage rise and suppress or limit the voltage transient so that it remains within contact ratings. Since the volt-second area under the transient curve remains constant, the proper transient protection for a given application depends on how long the transient voltage can remain. Effects and characteristics of arc suppression circuits are illustrated in Figure 4-37.

In Part A (Figure 4-37), having no arc suppression, damage will occur to the mercury-wetted relay contacts due to the rate of rise of voltage and the voltage transients exceeding the contact rating specifications.

In Part B (Figure 4-37), the rate of rise is controlled but the transient still exceeds the contact rating specification.

Safe operation is achieved in Part C (Figure 4-37), when both the rate of rise and the transient are controlled.

AC Inductive Loads

Arc suppression for ac inductive loads is difficult to determine by calculation due to the complex nature of the mathematics. It is usually easier to use a bench test setup to identify transients and choose the appropriate RC values for the suppression circuit. One technique, which is useful for extreme loads (above 100 Vac), is to place the main RC arc suppression circuit across the load as shown in Figure 4-38.

This alleviates the problem of ac leakage current through an RC arc suppressor that is in parallel with the contacts. But, this technique can result in a condition that exposes the contacts to voltage transients having a rate of rise in excess of 5V/μs due to the inductance of the field wiring. A secondary arc suppressor, R2-C2, must then be installed in parallel with the contacts. Since C2 need only be one-hundredth of the calculated value, ac leakage is reduced markedly.

An alternate method for protecting the contacts under extreme load conditions is to use a thyristor in parallel with the traditional arc suppression circuit across the contacts, as shown in Figure 4-39. All arc suppression components can then be placed in the arc suppression fields (F and G) of the signal-conditioning modules (W400 and W402).

Capacitive Loads

Since capacitors appear as short circuits when power is switched into them and as high energy sources when power is switched out of them into low impedances, current transients can produce problems. The design objective in protecting mecury-wetted relay contacts is to limit the rate of current increase when the contacts close and also to limit the absolute current so as not to exceed contact specifications. The simplest way to obtain this protection is illustrated in Figure 4-40.
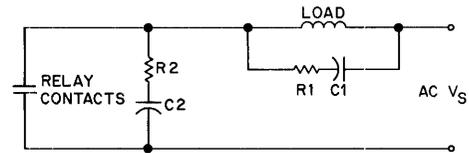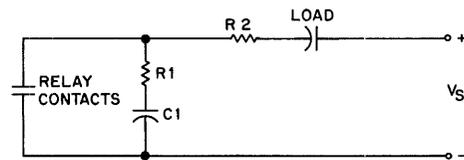

NOTE:
R1 and R2 should be calculated values.
C1 may be increased by 10 times calculated value to further reduce transients.
C2 need only be 1/100 of calculated value.

II-0985

Figure 4-38   Arc Suppression
for Extreme Inductive Loads
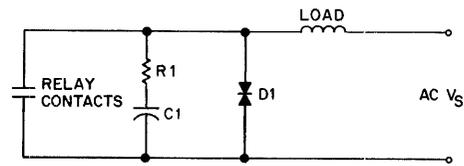
NOTES:
R1 and C1 provide rate of rise protection.
D1 Thyristor provides transient protection.

II-0986

Figure 4-39   Alternate Arc Suppression
for Extreme Inductive Loads

NOTES:
R1 and C1 provide rate of rise protection.
R2 provides current limiting.

II-0987

Figure 4-40   Arc Suppression
for Capacitive Loads

4-60

4.6.5 Driver Output Signal Conditioning

All M600 series functional modules contain 12 buffered open-collector driver output stages for driving loads. The W403 Signal-Conditioning Module must be used as the interface between the field devices and the driver output modules. Diode suppression for inductive loads is included on the driver output modules; therefore, no external suppression circuit is required. The signal-conditioning module is designed to accommodate both common and isolated field power applications. The only difference between common and isolated power configurations is in the way the loads are connected to the screw terminals. Figures 4-41 through 4-44 illustrate the wiring techniques. The maximum current that can be switched by a W403 Module at any one time is 4A.

The M600 series functional modules can also be used to drive T^2L logic because the driver collectors are returned to +5V through a diode and resistor. Again, only the W403 Signal-Conditioning Module can be used as the interface. The wiring technique for this application is illustrated in Figure 4-45.

NOTE

For driver output and logic level output configurations described above, field power is not isolated from UDC power as for load switching, contact sensing, and logic level sensing configurations described previously.

4.6.6 DAC Module Signal Conditioning

The A633 DAC Module contains four D/A converters. Four different signal-conditioning modules are available for interfacing the field devices with the DAC module. They are:

Module Type	Output Characteristics
A233	0 to +10V @ 15 mA max
A234	+1V to +5V @ 15 mA max
A235	4 mA to 20 mA, 750Ω max
A236	10 mA to 50 mA, 300Ω max

The four outputs from the signal-conditioning module are single ended outputs (Figure 4-46). Therefore, the loads should be of the type that can be grounded to the analog ground which, in turn, is connected to system ground in the UDC. Modules A234, A235, and A236 are factory adjusted, but can be adjusted in the field (refer to the A-SP-BA633-0-2 DAC Checkout Procedure) .
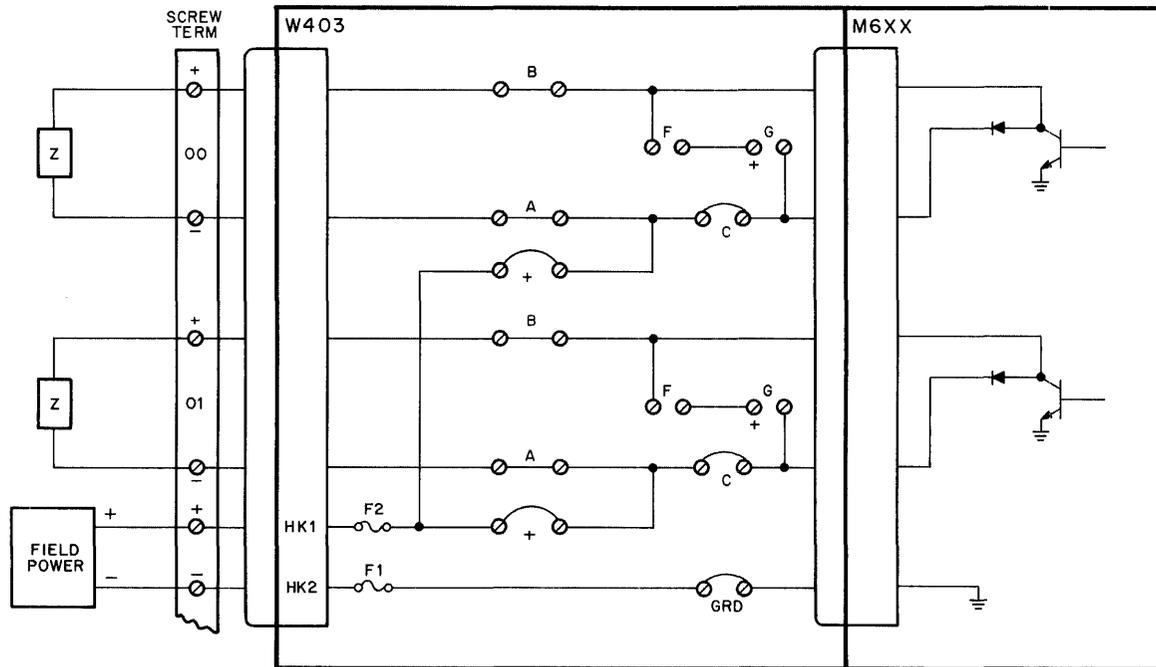
NOTE

Loads, including screw-terminal wiring, having up to 0.1 μF will not cause instability but will affect settling time.
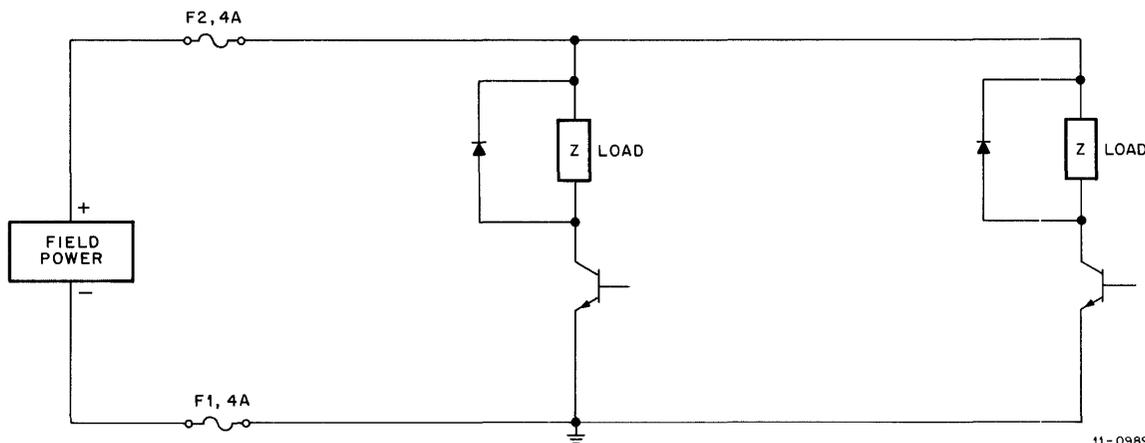
4.6.7 Counter Module Signal Conditioning

The W734 I/O Counter Module is a 12-bit (optionally 16 bits) asynchronous binary counter. The external inputs and outputs include:

 a. EN Input
 b. CONT Input
 c. CV Input
 d. $\overline{P}$ Output
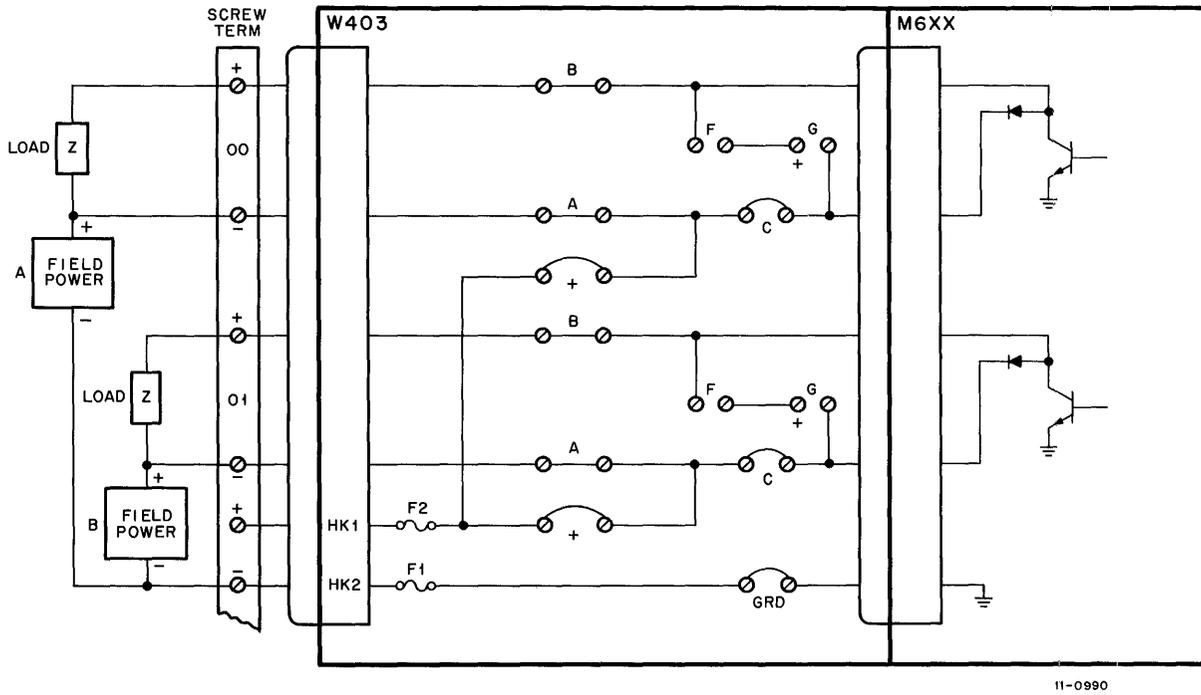 e. $\overline{C}$ Output
 f. $\overline{S}$ Output

Figure 4-41 Common Power for Driver Output, Wiring Diagram

Figure 4-42 Common Power for Driver Output, Schematic Diagram

The W400 Signal-Conditioning Module must be used to interface the field devices (counter inputs and outputs) with the counter. The counter outputs can be connected to accommodate common or isolated field power for driving loads or can be connected to provide logic level outputs (Figures 4-47 through 4-49). No external protection is required for driving inductive loads since diode suppression is included in the counter output circuits.

4-62

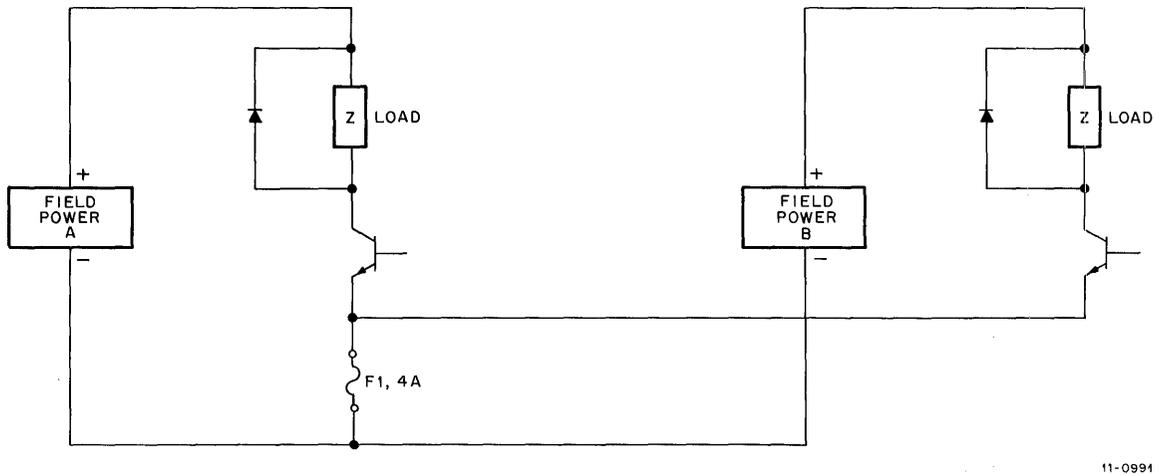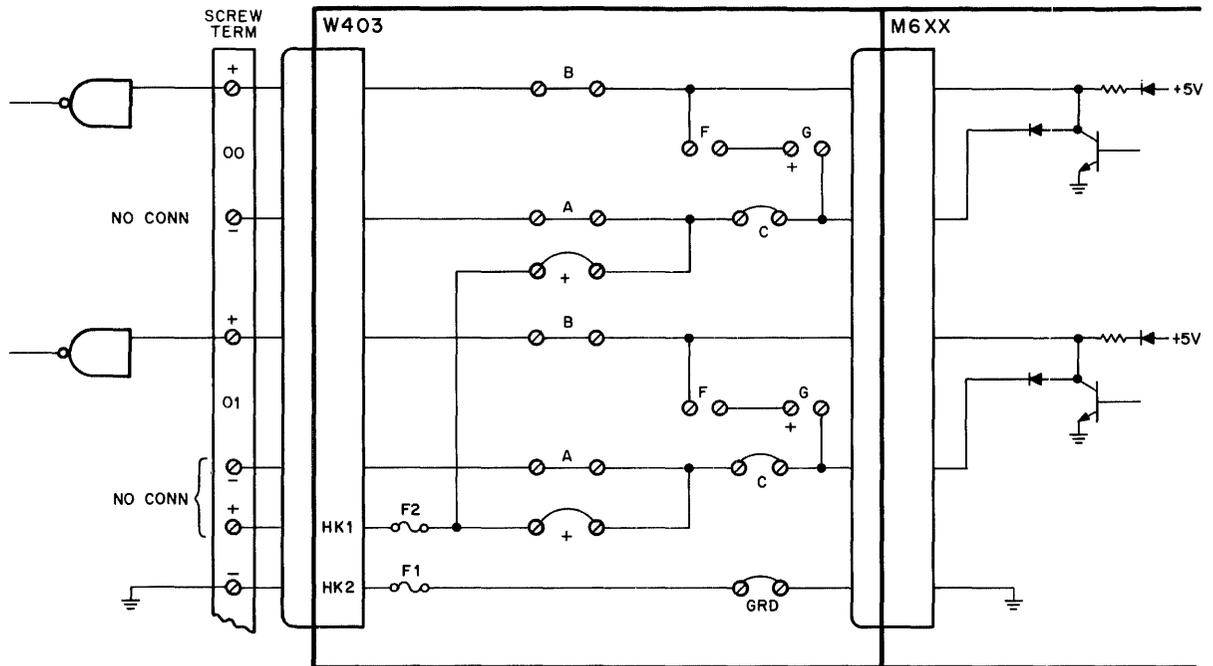Figure 4-43   Isolated Power for Driver Output, Wiring Diagram

Figure 4-44   Isolated Power for Driver Output, Schematic Diagram

Figure 4-45   Logic Level Output, Wiring Diagram

### 4.6.8 Signal-Conditioning Modules

The following data sheets provide information on all UDC8 signal-conditioning modules. The user is advised to read the data sheets on each module in his system carefully and pay particular attention to the jumper configurations. The following signal-conditioning modules are discussed.

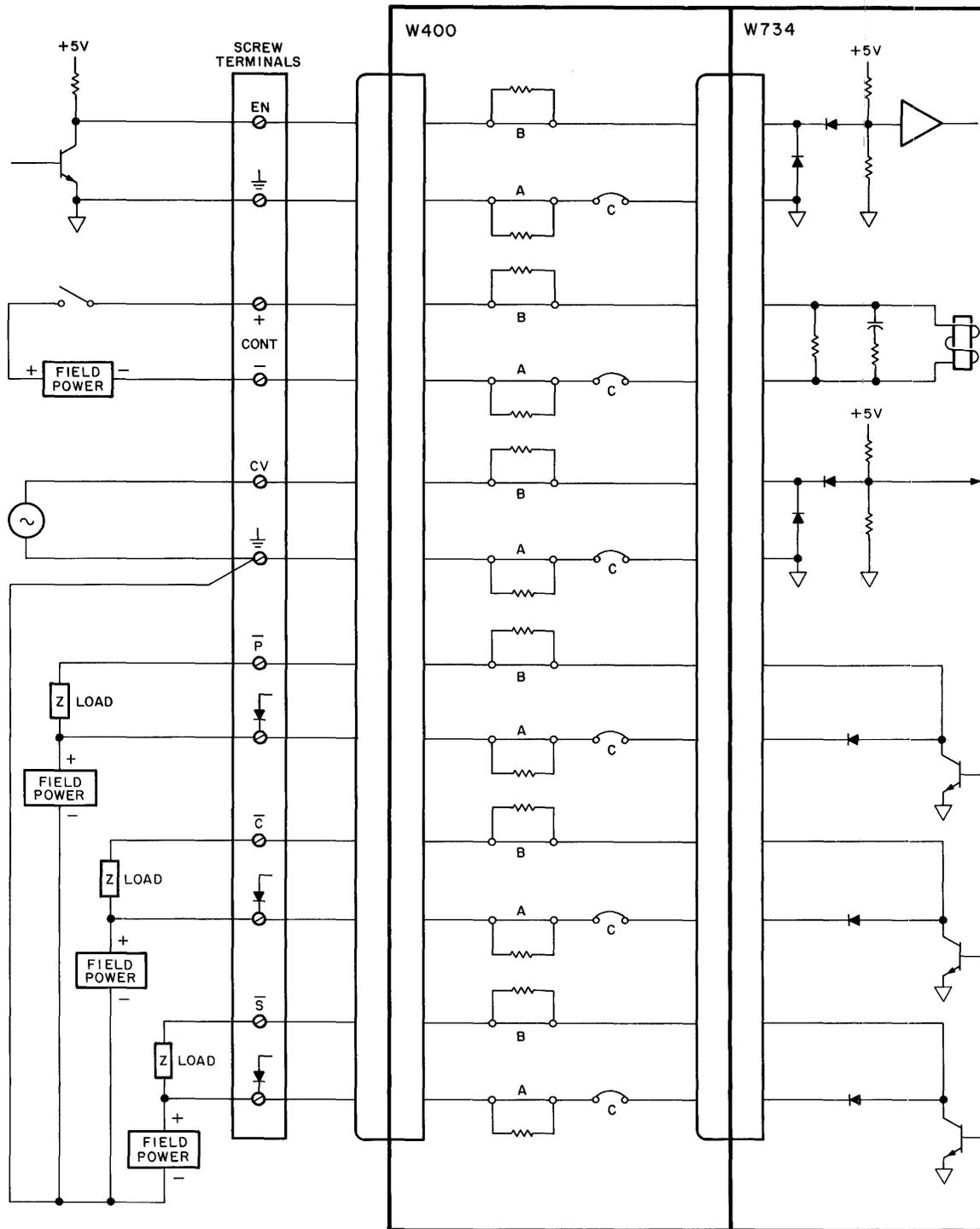|		
a.	Isolated Power	W400
b.	Common Power	W402
c.	Solid-State Driver	W403
d.	Buffered Voltage	A233
e.	Buffered Voltage	A234
f.	Buffered Current	A235
g.	Buffered Current	A236

4-64
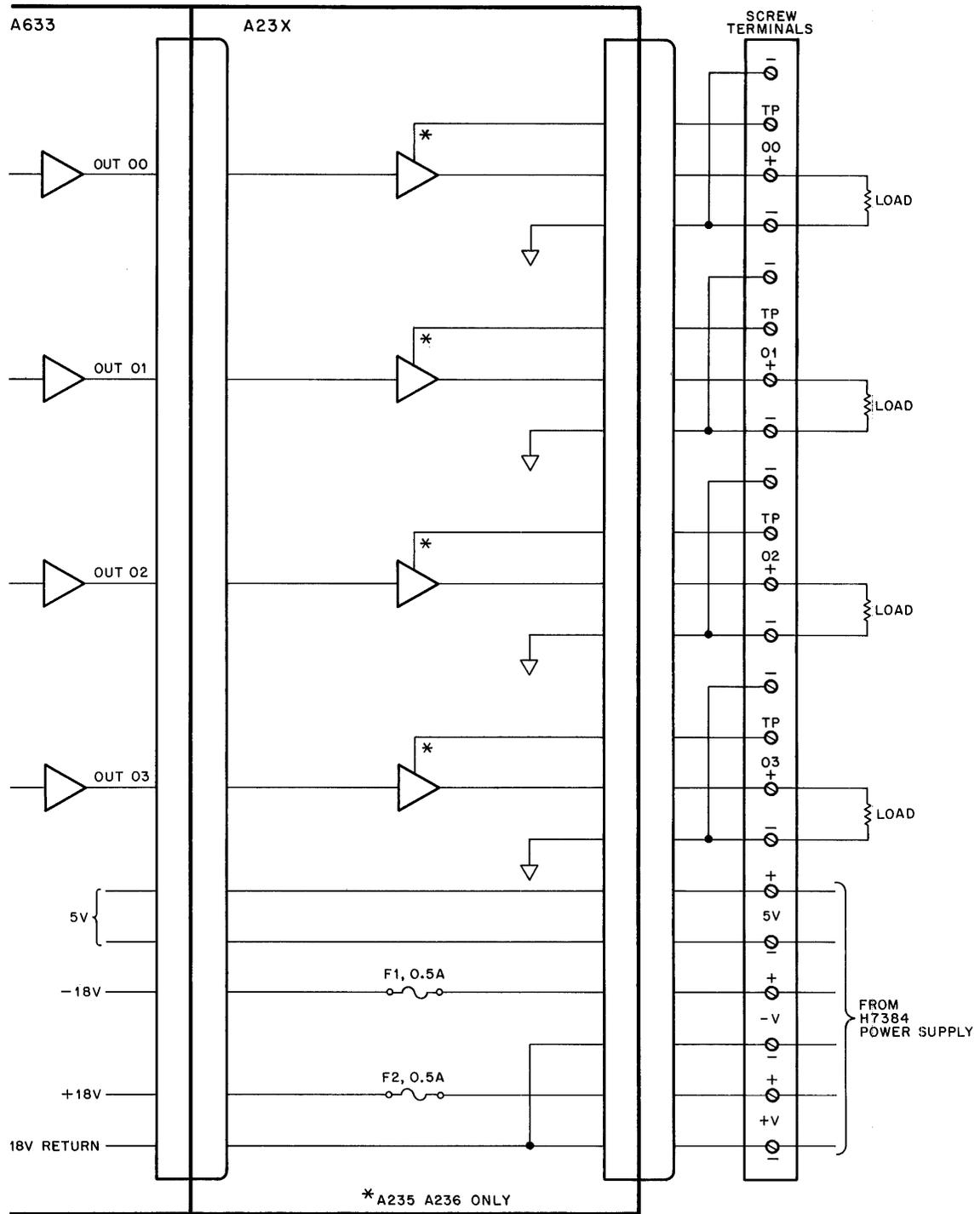
Figure 4-46   DAC Wiring Diagram
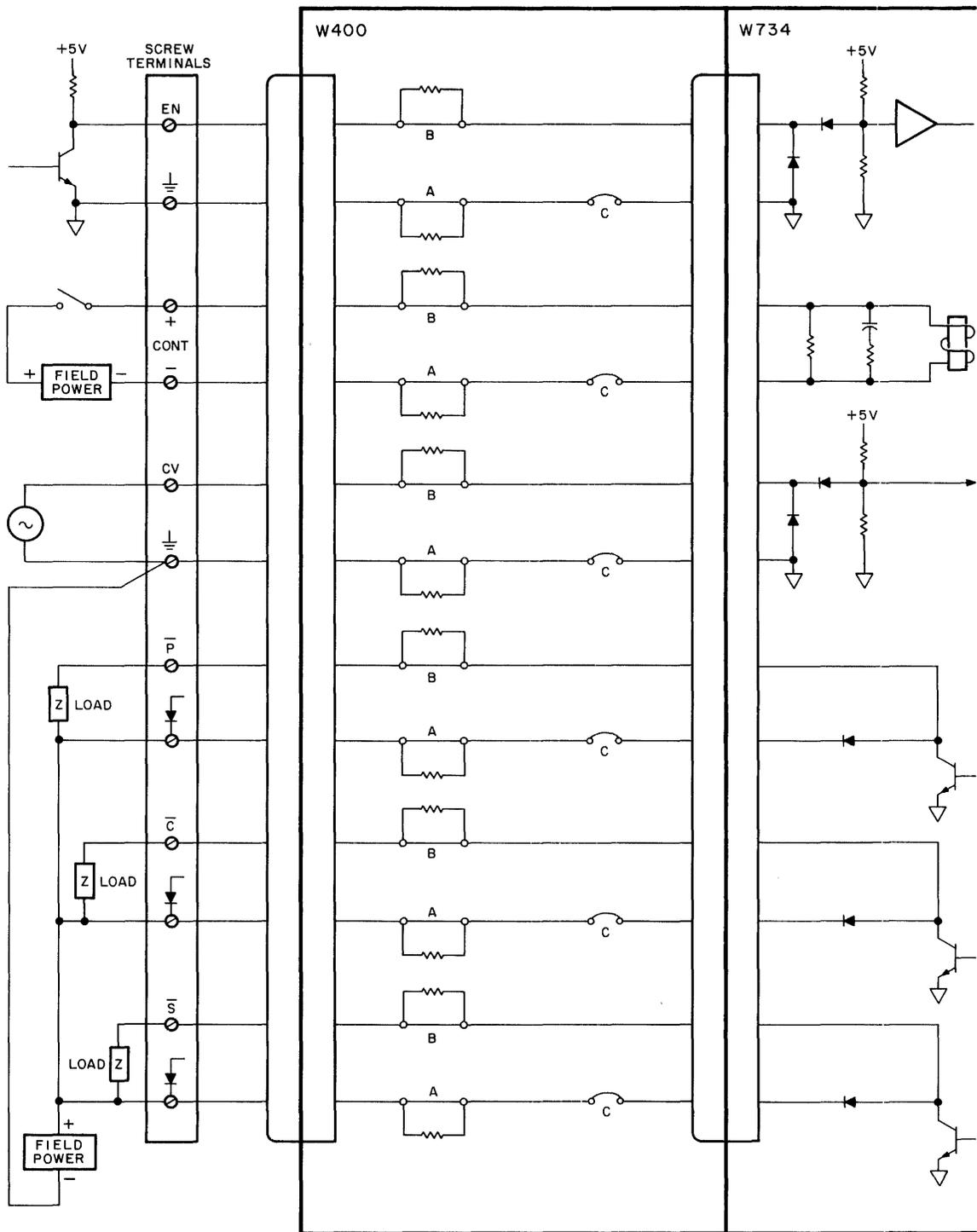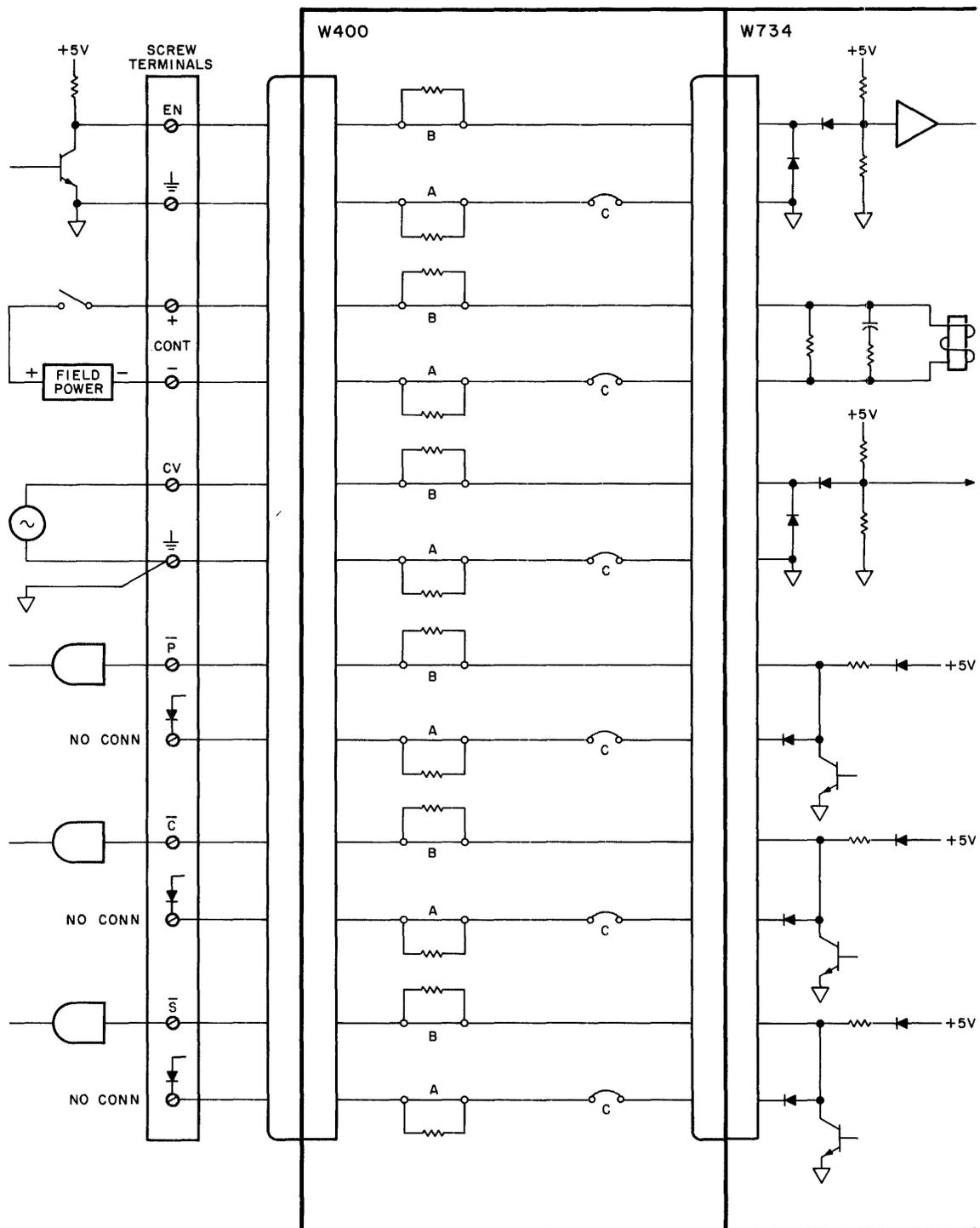
11-0993

Figure 4-47 Counter Input and Output (Common Power), Wiring Diagram

Figure 4-48 Counter Input and Output (Isolated Power), Wiring Diagram

11-0995

Figure 4-49   Counter Input and Output (Logic Level), Wiring Diagram

11-0996

ISOLATED POWER SIGNAL-CONDITIONING MODULE

The isolated power signal-conditioning module (Figures 4-50 and 4-51) is a double-ended module providing the interface between 16 individual points on the functional I/O modules and customer contacts or field signals. Differential pair field wiring from the screw terminals is terminated on a 36-pin connector that connects to the rear of the module.

CAUTION
This module may not be used with M684 Flip-Flop Relay Driver or M686 Single-Shot Relay Driver Modules.
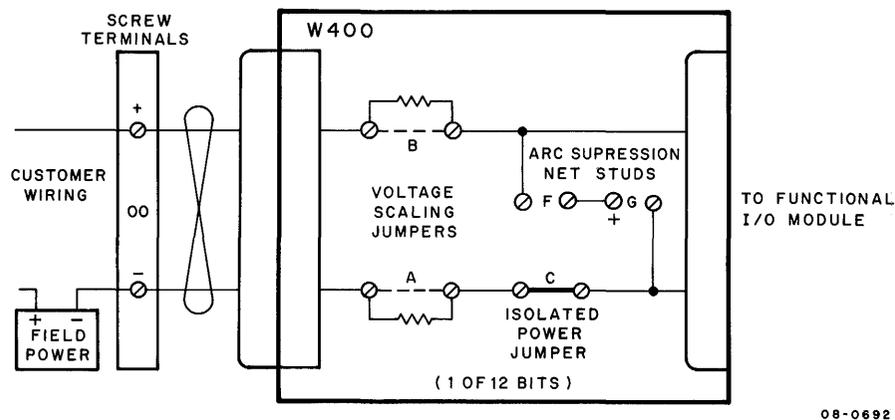

Figure 4-50   Simplified Schematic Diagram (W400)

The isolated power feature is used where each field digital I/O point is supplied with power at the field location. Each pair of control wires is isolated from every other point and from UDC ground.

When used with input modules (Contact Sense, Contact Interrupt), resistor/jumper selection on each circuit scales the field-supplied excitation voltage of 6V, 24V, or 48 Vdc to 6 Vdc at 15 mA point for proper input circuit operation. The module will be delivered setup for 6V operation.

The mercury-wetted relay contacts of the output single-shot relay, flip-flop relay, and latching relay modules are rated at 2A, 250V (the product not to exceed 100 VA) and require arc suppression. Provision for customer-mounting (split lug fields F and G) of the appropriate RC filter elements for arc suppression for each circuit is provided on the W400 and W402.
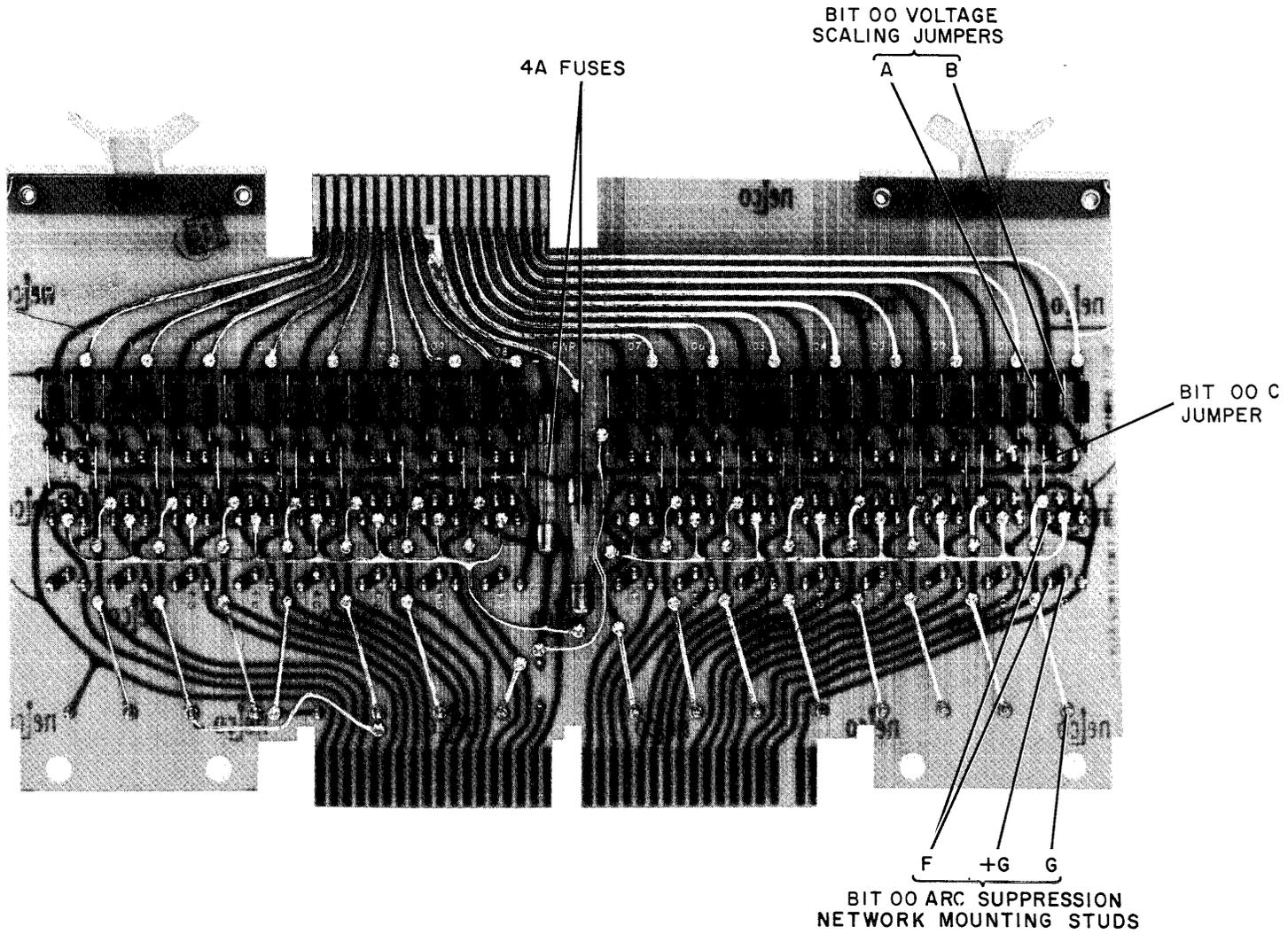
BIT OO VOLTAGE
SCALING JUMPERS

4A FUSES

A   B

BIT OO C
JUMPER

4-70

F   +G   G

BIT OO ARC SUPPRESSION
NETWORK MOUNTING STUDS

Figure 4-51 Location of Jumpers and Component-Mounting Studs (W400)

COMMON POWER SIGNAL-CONDITIONING MODULE

The W402 Common Power Signal-Conditioning Module (Figures 4-52 and 4-53) is a double-ended module providing the interface between 16 individual points on the functional I/O modules and customer contacts or field signals. Differential pair field wiring from the screw terminals is terminated on a 36-pin connector that connects to the rear of the module.

CAUTION
This module may not be used with M684 Flip-Flop Relay Driver or M686 Single-Shot Relay Driver Modules.
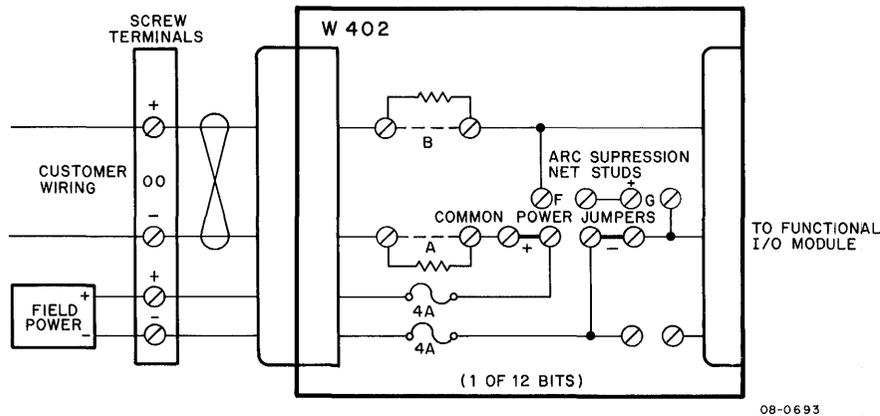

Figure 4-52 Simplified Schematic Diagram (W402)

The common power signal-conditioning module has a power input pair that permits field-supplied excitation or control power to be brought directly to the signal-conditioning module and distributed in parallel (common) to each of the circuits on the functional I/O module. The input is fused for 4A. Therefore, when the combined relay output current exceeds 4A on a module, Module W400 must be used for power distribution and conditioning.

When used with input modules (Contact Sense, Contact Interrupt) resistor/jumper selection on each circuit scales the field-supplied excitation voltage of 6V, 24V, or 48 Vdc at 15 mA per point for proper input circuit operation. The module will be delivered setup for 6V operation.

The mercury-wetted relay contacts of the output single-shot relay, flip-flop relay, and latching relay modules are rated at 2A, 250V (the product not to exceed 100 VA) and require arc suppression. Provision for customer-mounting (split lug fields F and G) of the appropriate RC filter elements for arc suppression for each circuit is provided on the W400 and W402 Modules.

In applications where it is desired to demultiplex an output signal, the common power module can be used to distribute this signal to the contacts of a relay output functional module. This eliminates the necessity of jumpering one side of all the output contacts together.
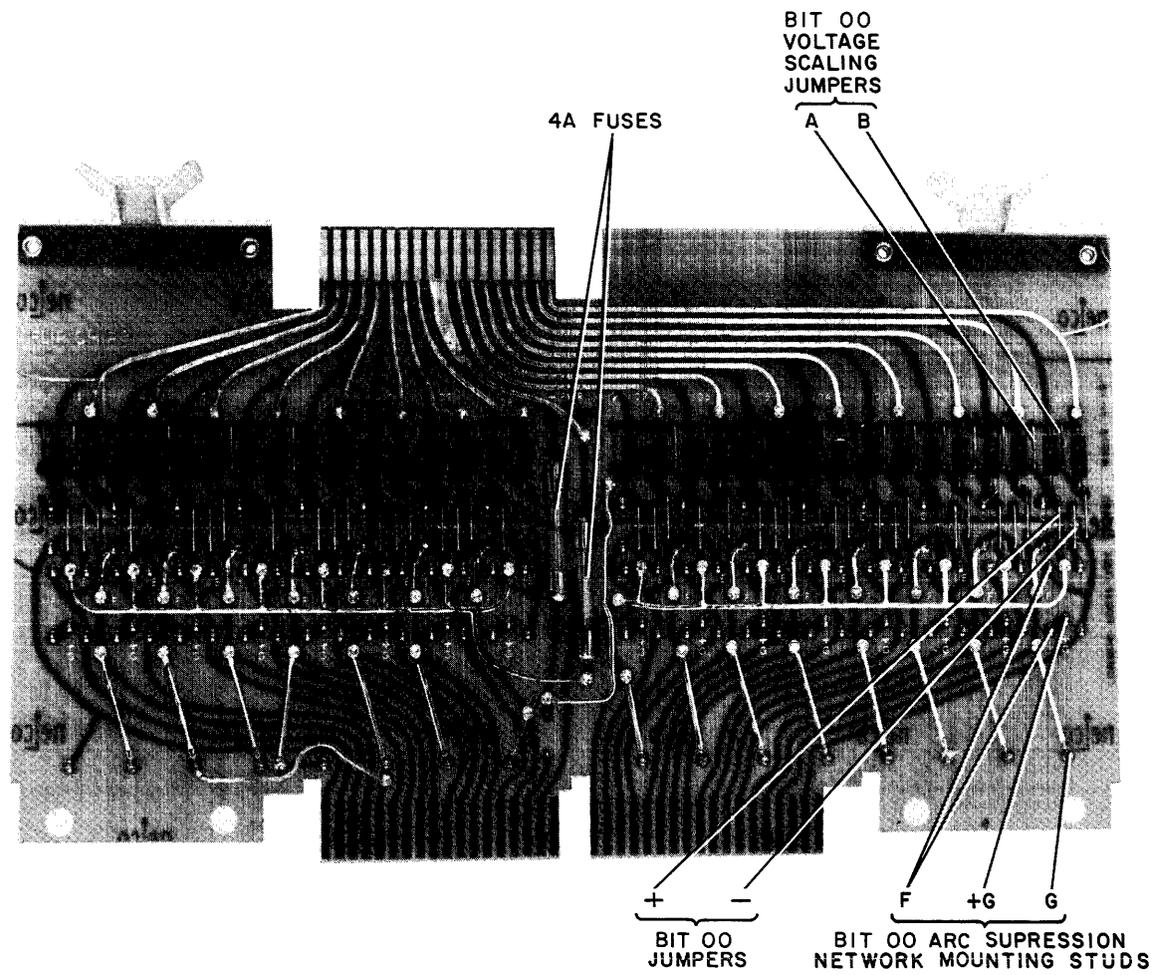
BIT 00
VOLTAGE
SCALING
JUMPERS

4A FUSES

A   B

+   –

F   +G   G

BIT 00
JUMPERS

BIT 00 ARC SUPRESSION
NETWORK MOUNTING STUDS

Figure 4-53   Location of Jumpers and Component-Mounting Studs (W402)

SOLID-STATE DRIVER SIGNAL-CONDITIONING MODULE

This module is a double-ended module providing the interface between 16 individual points on the M684 Flip-Flop Driver or the M686 Single-Shot Driver output modules and field circuits (Figures 4-54 and 4-55). Differential pair field wiring from the screw terminals is terminated on a 36-pin connector that connects to the rear of the module. One wire of each pair connects one side of each field load to the open collector switch on the output module. If only logic levels are required, only this line is needed. The other wire of this pair connects the opposite end of the load to a positive common power source. This power is customer-supplied and is brought in to the W403 Module from the BC40C-4 Screw Terminal Assembly, along with the control point pairs. The positive line is distributed to each of the control point pairs. A common return line for all field loads is connected to UDC logic ground. Both positive and negative power loads are fused for 4A.
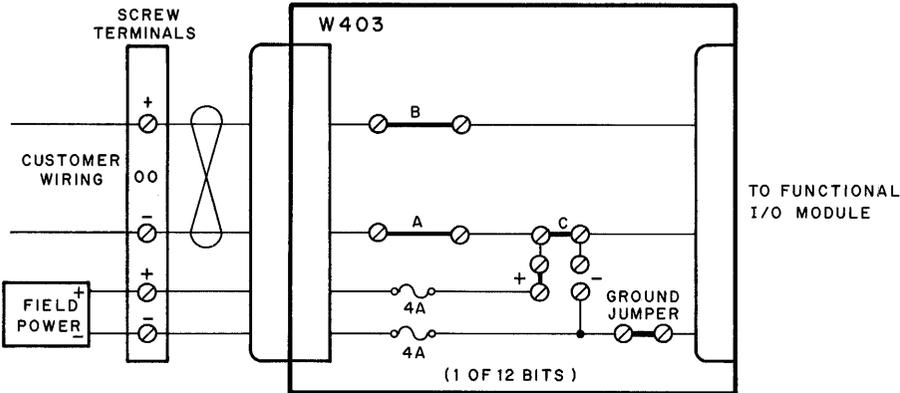
Figure 4-54 Simplified Schematic Diagram (W403)

BIT 00
JUMPERS

A   B

4A FUSES

GROUND JUMPER

C   +

BIT 00
JUMPERS
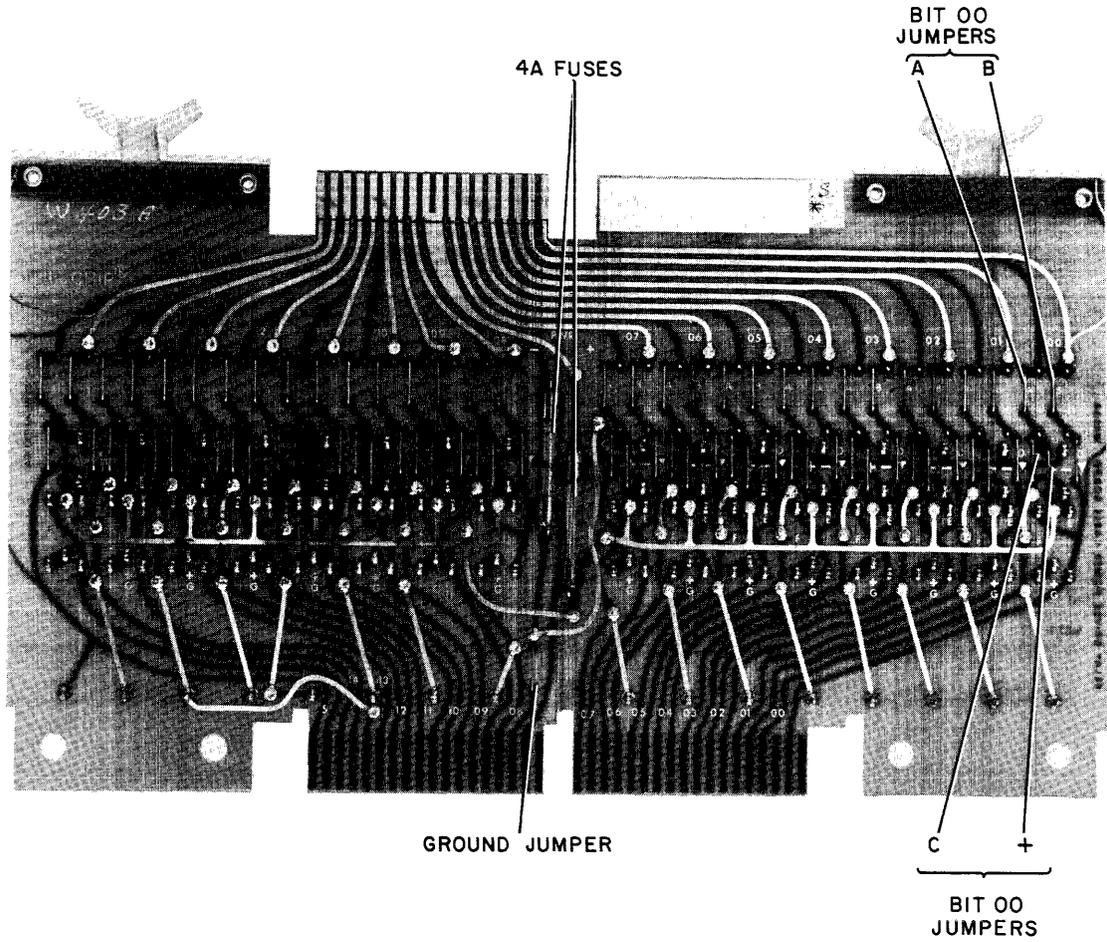
Figure 4-55   Location of Jumpers (W403)

BUFFERED VOLTAGE SIGNAL-CONDITIONING MODULE

FUNCTIONAL SPECIFICATIONS

Analog Output:	0 to +10V at 15 mA max (see below)
Gain Linearity:	−1 ± 0.05%
Zero Input Offset:	6 mV max
Settling Time:	35 μs max to within ± 0.05% of final value with 150 pF load. 50 μs with DAC A633
Power:	+18V ± 0.05V, 45 mA max plus load current −18V ± 0.05V, 45 mA max

Power is supplied from an external H738A Power Supply and applied through the screw terminals (BC40C Cable Assembly).
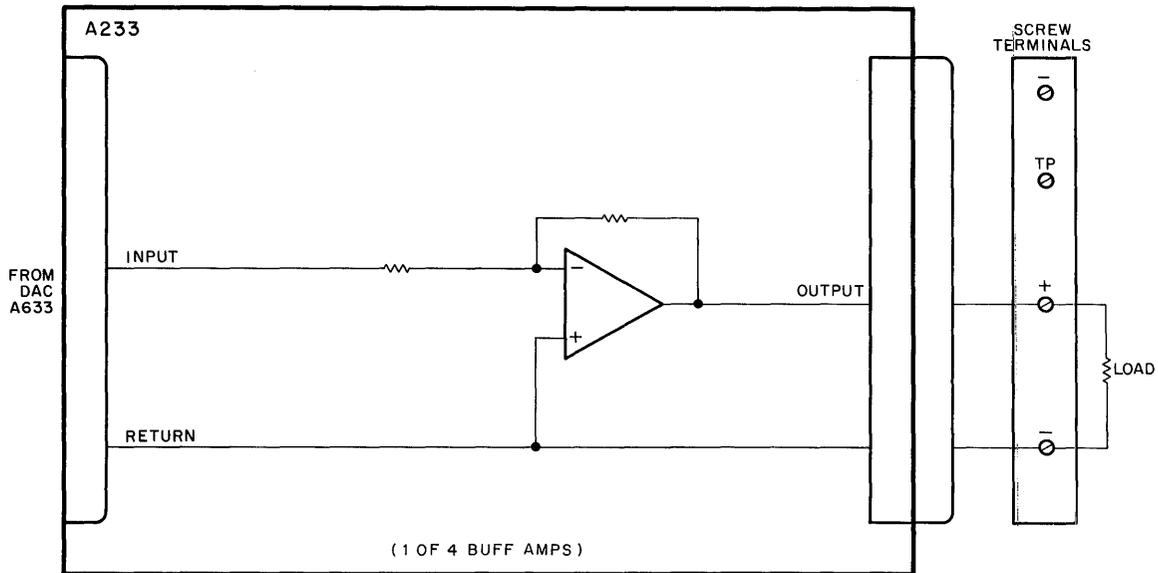
Figure 4-56   Simplified Schematic Diagram (A233)

DESCRIPTION

The A233 Buffered Voltage Signal-Conditioning Module (Figure 4-56) contains four buffered voltage amplifier circuits. This module is used as a signal-conditioning module for the A633 DAC Module. The amplifiers are simple inverting type amplifiers with a gain of 1. A current buffer is used to provide up to 15 mA of output current.

A twisted-pair cable is recommended to connect the output from the screw terminals to the load. This cable should be of sufficient wire size to prevent excessive losses along the cable.

DATA FORMAT (Channel 00)

Digital Input to A633	DAC Voltage from A633	Voltage Output at Screw Terminals
0000	0.000V	0.000V
1000	–5.000V	+5.000V
1777	–9.990V	+9.990V

BUFFERED VOLTAGE SIGNAL-CONDITIONING MODULE

FUNCTIONAL SPECIFICATIONS

Analog Output: +1V to +5V at 15 mA max (see below)

Gain Linearity: −0.4 ± 0.05%

Zero Input Offset: Adjustable to give +1V out

Settling Time: 35 μs max to within ± 0.05% of final value with 150 pF load.
                             50 μs with DAC A633

Power: +18V ± 0.05V 48 mA max plus load current
                             −18V ± 0.05V 48 mA max

Power is supplied from an external H738A Power Supply and applied through the screw terminals (BC40C Cable Assembly).
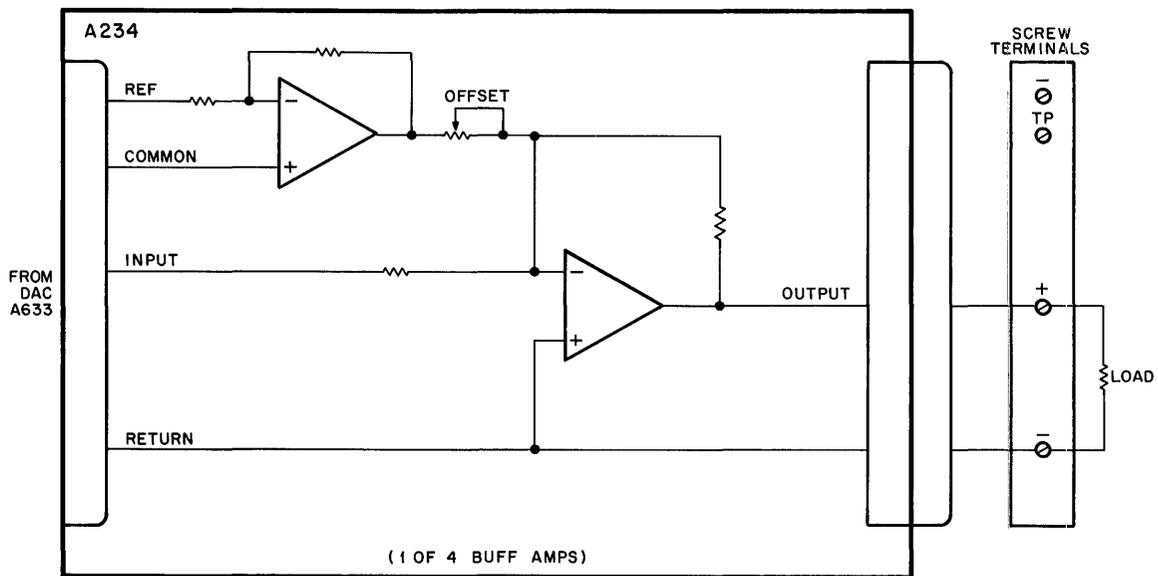
Figure 4-57   Simplified Schematic Diagram (A234)

DESCRIPTION

The A234 Buffered Voltage Signal-Conditioning Module (Figures 4-57 and 4-58) contains four buffered voltage amplifier circuits. This module is used as a signal-conditioning module for the A633 DAC Module. The amplifiers are inverting type amplifiers with individual offset adjustments. A current buffer is used to provide up to 15 mA output current.

4-77

A twisted-pair cable is recommended to connect the output from the screw terminals to the load. This cable should be of sufficient wire size to prevent excessive losses along the cable.

DATA FORMAT (Channel 00)

Digital Input to A633	DAC Voltage from A633	Voltage Output at Screw Terminals
0000	0.000V	+1.000V
1000	−5.000V	+3.000V
1777	−9.990V	+4.996V

Figure 4-58   Location of Adjustments and Fuses (A234)

BUFFERED CURRENT SIGNAL-CONDITIONING MODULE

FUNCTIONAL SPECIFICATIONS

Analog Output:	+4 mA to +20 MA into 750Ω max (see below)
Zero Input Offset:	Adjustable to give +4 mA out
Settling Time:	35 µs max to within 0.05% of final value with 150 pF capacitor across the load. 50 µs with DAC A633
Linearity:	≥ 99.95%
Power:	+18V ± 0.05V 126 mA max −18V ± 0.05V 46 mA max

Power is supplied from an external H738A Power Supply and applied through the screw terminals (BC40C Cable Assembly).
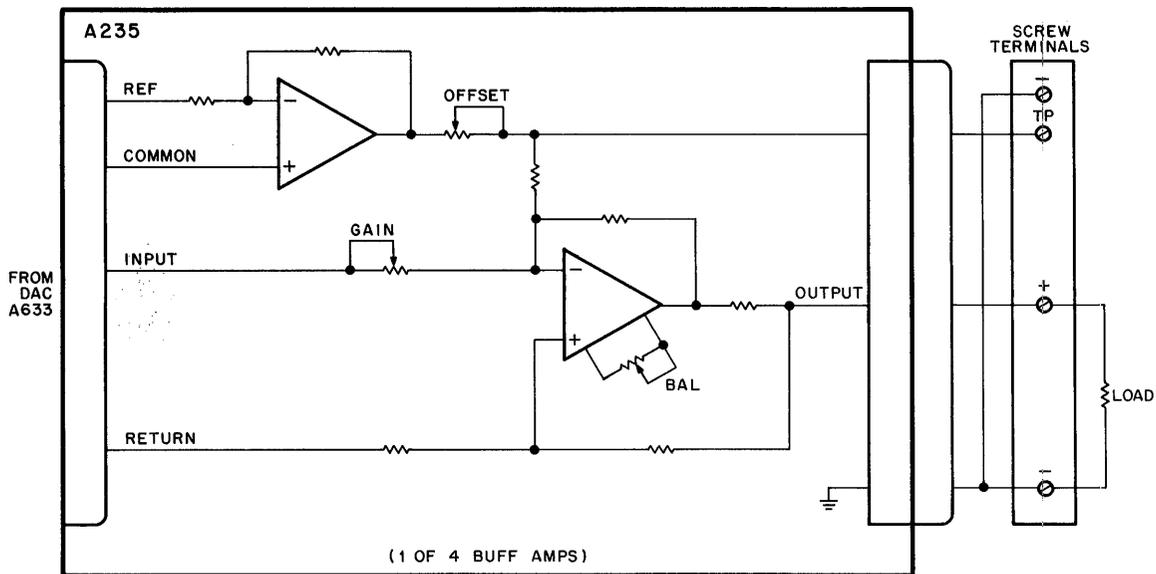
Figure 4-59 Simplified Schematic Diagram (A235)

DESCRIPTION

The A235 Buffered Current Signal-Conditioning Module (Figures 4-59 and 4-60) contain four current source circuits. This module is used as a signal-conditioning module for the A633 DAC Module. The output current is directly proportional to the voltage from the A633 DAC, but is offset by +4 mA. The maximum load which will not cause saturation is 750Ω.

A twisted-pair cable is recommended to connect the output from the screw terminals to the load. This cable should be of sufficient wire size to prevent excessive losses along the cable. The resistance of the cable must be included as part of the load.

DATA FORMAT (Channel 00)

Digital Input to A633	DAC Voltage from A633	Current Output at Screw Terminals
0000	0.000V	+ 4.000 mA
1000	−5.000V	+12.000 mA
1777	−9.990V	+19.984 mA

DAC 00 { GAIN R58, OFFSET R59, BALANCE R60

DAC 01 { GAIN R61, OFFSET R62, BALANCE R63

F1 0.5 AMP

F2 0.5 AMP

DAC 02 { GAIN R64, OFFSET R65, BALANCE R66

DAC 03 { GAIN R67, OFFSET R68, BALANCE R69
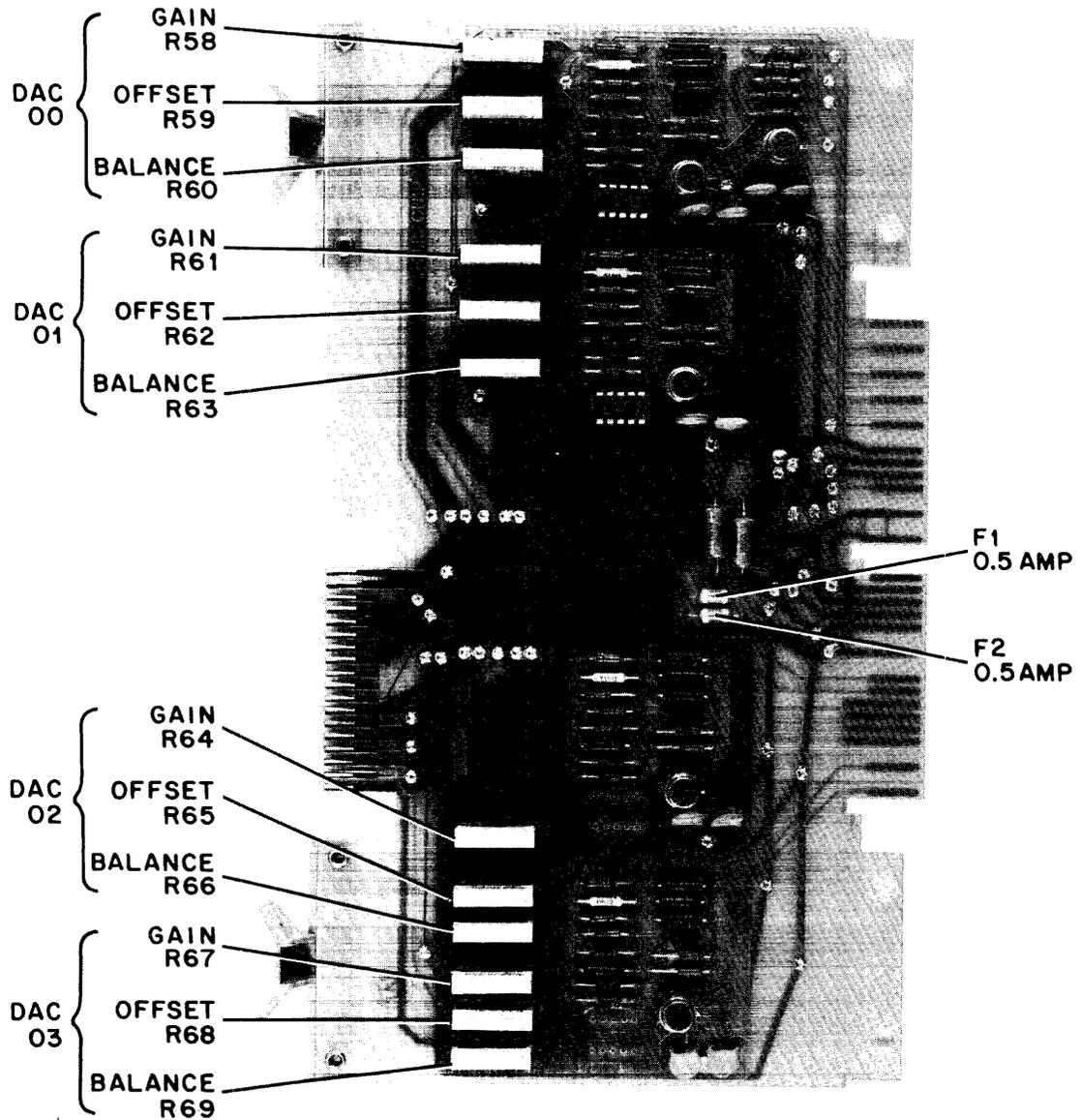
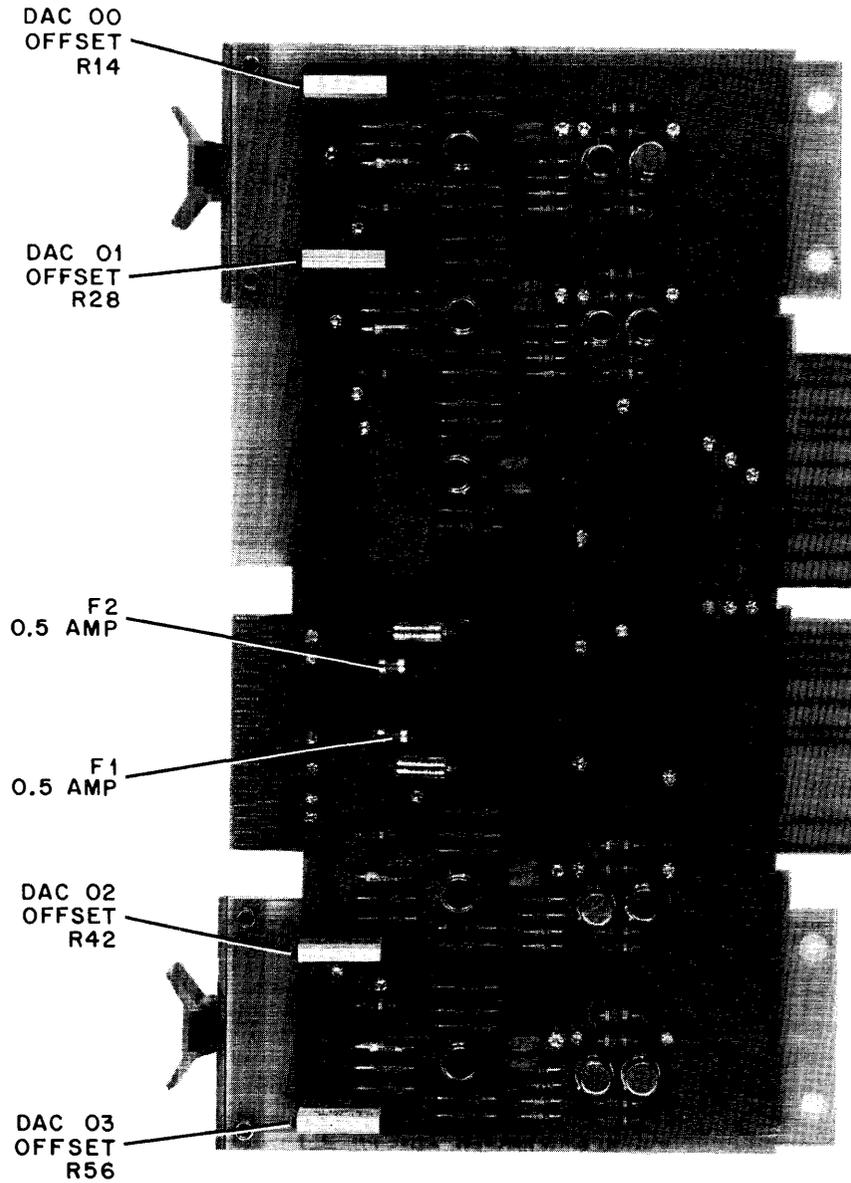Figure 4-60   Location of Adjustments and Fuses (A235)

BUFFERED CURRENT SIGNAL-CONDITIONING MODULE

FUNCTIONAL SPECIFICATIONS

Analog Output:	+10 mA to +50 mA into 300Ω max (see below)
Zero Input Offset:	Adjustable to give +10 mA out
Settling Time:	35 µs max to within 0.05% of final value with 150 pF capacitor across the load. 50 µs with DAC A633
Linearity:	⩾ 99.95%
Power:	+18V ± 0.05V 246 mA
	−18V ± 0.05V 46 mA

Power is supplied from an external H738A Power Supply and applied through the screw terminals (BC40C Cable Assembly).
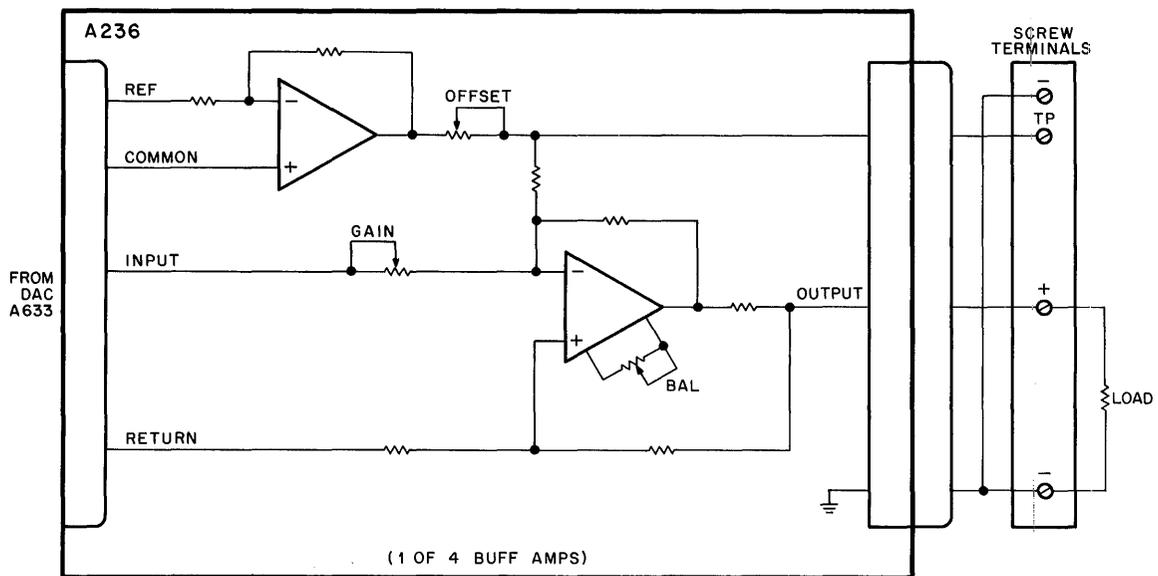
Figure 4-61   Simplified Schematic Diagram (A236)

DESCRIPTION

The A236 Buffered Current Signal-Conditioning Module (Figures 4-61 and 4-62) contains four current source circuits. This module is used as a signal-conditioning module for the A633 DAC Module. The output current is directly proportional to the voltage from the A633 DAC, but is offset by +10 mA. The maximum load which will not cause saturation is 300Ω.

A twisted-pair cable is recommended to connect the output from the screw terminals to the load. This cable should be of sufficient wire size to prevent excessive losses along the cable. The resistance of the cable must be included as part of the load.

DATA FORMAT (Channel 00)

Digital Input to A633	DAC Voltage from A633	Current Output at Screw Terminals
0000	0.000V	+10.000 mA
1000	−5.000V	+30.000 mA
1777	−9.990V	+49.961 mA


```
           GAIN
           R58
DAC {      OFFSET
00         R59
           BALANCE
           R60

           GAIN
           R61
DAC {      OFFSET
01         R62
           BALANCE
           R63

                                        F1
                                        0.5 AMP

                                        F2
                                        0.5 AMP

           GAIN
           R64
DAC {      OFFSET
02         R65
           BALANCE
           R66

           GAIN
           R67
DAC {      OFFSET
03         R68
           GAIN
           R69
```
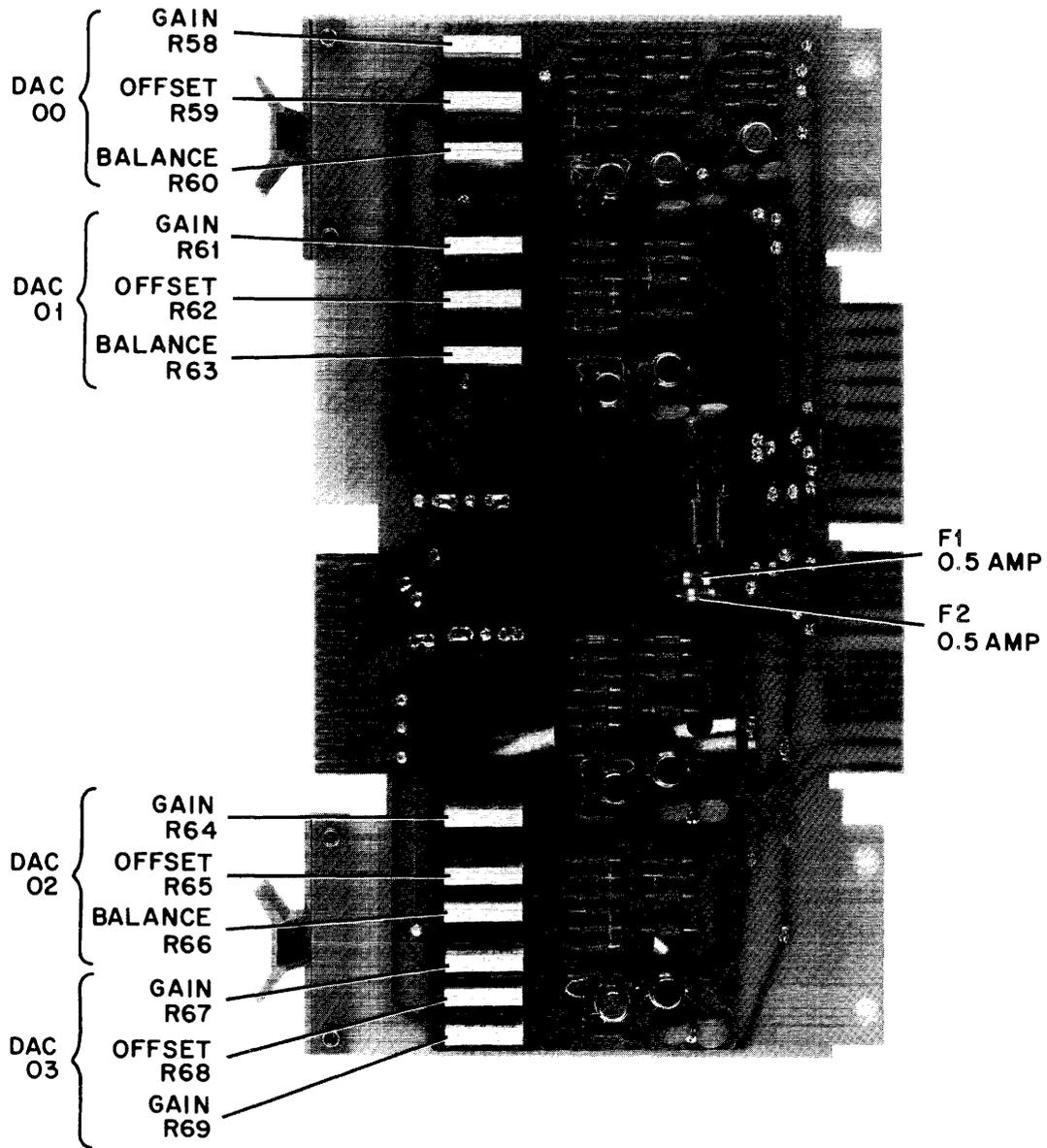
Figure 4-62   Location of Adjustments and Fuses (A236)

4.7 FIELD WIRING

There are certain wiring procedures and practices that are recommended for the proper installation of all lead-in wires connecting remote analog and digital devices with the computer. Deviations from this procedure can introduce unpredictable system errors or inaccuracies because of variables that are unknown and/or uncontrollable. All basic computer accuracies are thus given at the connection cabinet terminals and any inaccuracies caused by lead-in wires must be considered separately.

The field input and output interface circuits have been inherently designed to cope with the majority of adverse industrial plant environments. The design features include such things as:

a. Current rather than voltage sensitive digital inputs for greater immunity to induced voltages.

b. DC isolation between the UDC bus and the individual inputs and outputs.

Although these features allow the user more freedom in his lead-in cable installation, certain special precautions, for the various types of inputs and outputs, are still necessary for optimum operation.

4.7.1 Wire Specifications

All signal wiring should be individual twisted pairs containing about 6 to 12 twists per foot. Cables should be composed of concentric twisted pairs with all lays and pairs twisted in the same direction for greater flexibility.

Recommended wire sizes, contingent upon compliance with specifications for maximum line impedance and voltage drop, are:

a. No. 16 AWG (4.0 ohms per 100 ft) or equivalent.
b. No. 18 AWG (6.4 ohms per 1000 ft) or equivalent.
c. No. 20 AWG (10.1 ohms per 1000 ft) or equivalent.

Stranded wire should be used for flexibility. Tinned copper wire is recommended for oxidation resistance. The insulation resistance between conductor and from either conductor should not be less than 500 megohms per 1000 ft (PVC).

The dielectric strength of the cable and conductor insulation should not be less than 600V. The multi-paired cable should be jacketed in polyvinyl, polyethylene or Teflon at least 0.034-in. thick for mechanical protection. Teflon should be specified for areas where the ambient temperature is expected to be between 105°C (221°F). and 200°C (424°F).

4.7.1.1 Analog Output Wiring — Analog output signals are normally current or high-level voltage signals so that most of the precautions necessary for low-level analog signals can be relaxed. Analog output signal wires should be run as twisted pairs and may be run in multi-pair cable if their destinations are common.

4.7.1.2 Digital Input Wiring — Digital input signal wires can be run as twisted pairs and in multi-paired cables. Digital input signals can also utilize 12 input signal wires and one common, as long as they are closely associated or twisted together in the same cable. Digital input cables should not be run near ac power cables. Digital input wires can be mixed with digital output wires in the same cable tray. Digital input wires should not be mixed with high-level digital output wires in the same cable.

Pulse type (counter) input wires and edge sensing interrupt type (alarm) input wires should be run as twisted pairs in a multi-paired digital input cable.

4.7.1.3 Digital Output Wiring — Digital output signal wires should be run as twisted pairs in multi-paired cables containing no analog wires.

Contact closure type (relay) output wires should be run separate from other input and output signal wires in electrostatically shielded multi-twisted pair cables because of the noise producing characteristics of the devices (lamps and relays) that are frequently powered from these outputs. Contact closure type signals are usually made and broken quite suddenly, which can cause high voltage inductive spikes to appear on these lines and any others in close proximity if the driven inductive devices do not have proper suppression.

It is strongly recommended that all ac devices and dc inductive devices incorporate arc suppression circuits to limit noise spikes to less than 2V above the signal level being switched.

Stepping motor driver output wires can be run as twisted pairs or as four wires and a common as long as they are in close proximity or twisted together in the same cable.

4.7.1.4 Grounding — Ideally, all grounds should be separated into categories such as power grounds, logic grounds, digital grounds, analog grounds and relay grounds, and each category of grounds should be run directly to the ground electrode and tied to it at one point only. Practically this is not very feasible so that divisions can be made only as to analog grounds and nonanalog grounds.

4.7.2 Installation

Field wiring can be brought into the UDC system's cabinets either from the top or bottom. If the field wiring is brought in through conduit, a space should be provided so that the conduit does not touch the IDACS cabinet.

4.7.2.1 Top Entry — A clamping plate is provided on the top entry version of the cabinet so the leads can be securely clamped to the cabinets. Clamps are not provided by DEC. The plate must be drilled and the clamp secured by a nut, bolt, and lock washer.

The H964MA allows the screw terminals to be set back to accommodate larger and larger bundles of leads. The mounting screws are set on 2-in. centers. It is recommended that the screw terminals be set back 2 in. for each complete file implemented.

4.7.2.2 Bottom Entry — No provision is made for clamping bottom entry cables. As in the top entry, the H964MA must be set back 2 in. per file.

4.7.2.3 Cable Routing Lengths — The distance from 2 in. above the cabinet to the first bend is 12 inches. The cable must run 15 in. toward the back of the cabinet to the second bend. It then runs vertically down 6 in. to the bottom of the first screw-terminal assembly. Sixteen inches should be allowed to run and dress the longest lead. The screw terminals are mounted on 1-3/8 in. centers, so incremental increases of 1-3/8 in. must be planned for running additional leads.

4.7.2.4 Breakouts — A 2-in. stand-off is provided at each terminal assembly of the mounting screws. These posts provide a means for anchoring the cable and tying off the lead breakouts to the screw terminal assemblies.

4.7.2.5 Rear Terminal Assemblies — An additional 10 in. is added to the run following the first bend to get to the back of the cabinet. Then, a 40-in. vertical run is made to the first breakout. Note where cables of large diameter are formed, it is necessary to add several inches extra for the radius of each bend.

4.7.3 Screw-Terminal Markers

Each screw-terminal assembly has 17 pairs of screw terminals. Marker strips are supplied with each UDC System to identify each screw-terminal pair. Up to three types of marker strips (in two pieces) can be supplied, one type for each class of I/O modules being utilized. The classes are:

- a. Digital I/O
- b. DAC
- c. Counter

The digital I/O class contains the following modules: W730, W732, W740, W742, M684, M686, M802, M804, and and M806. The marker strips to be used for these modules are shown below.
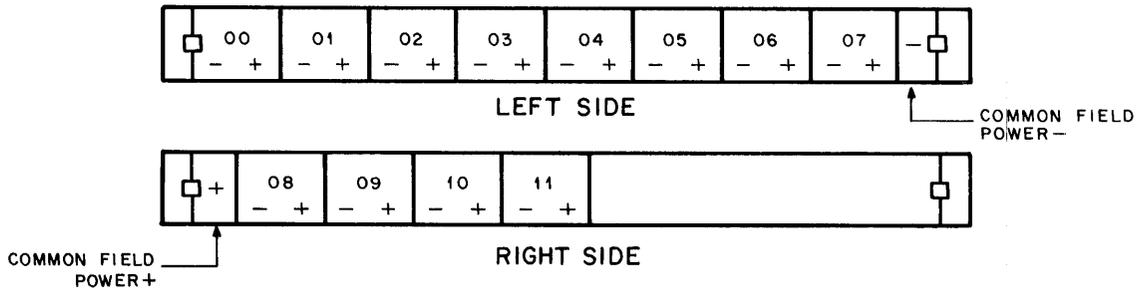
The + and − terminal markings for each bit refer to the input polarity of the W730, W732, W740, and W742 Modules. For mercury-wetted relay contact output modules (M800 series), the marked polarity must also be observed if an arc suppression circuit is installed.

The marker strips for DAC Module A633 are shown below.
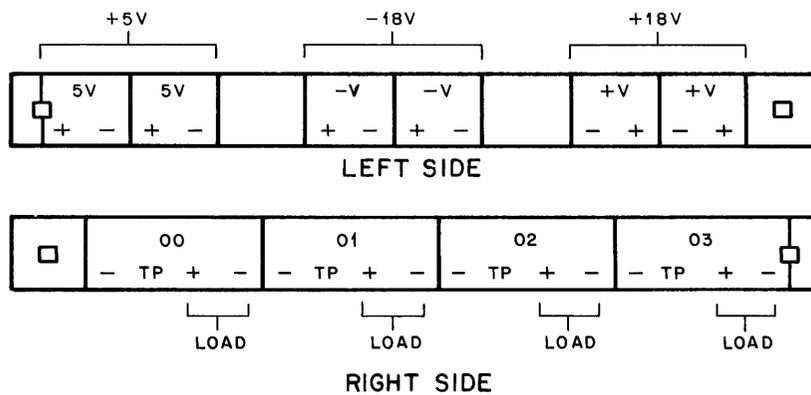
The marker strips for Counter Module W734 are shown below:

RETURN FOR $\bar{P}$, $\bar{C}$ AND $\bar{S}$ OUTPUTS

				CONT			C					
	E N			− +			V				−	

EXTERNAL COUNT
ENABLE INPUT

CONTACT INPUT

VOLTAGE INPUT

LEFT SIDE

	$\bar{P}$		$\bar{C}$			$\bar{S}$	W734 COUNTER	

PULSE
OUTPUT

CONTROL
OUTPUT

SIGN
OUTPUT

RIGHT SIDE
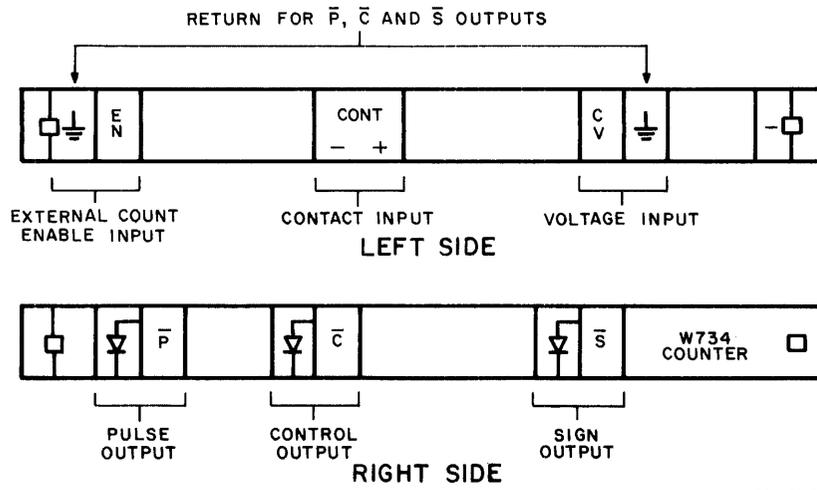
08-0744

5.1 GENERAL

The maintenance procedures presented in this chapter are limited to those required for maintaining and testing the UDC8 equipment bays. Procedures for maintaining and testing the PDP-8 Computer System are contained in the *PDP-8 Maintenance Manual*. The maintenance philosophy to be followed for the UDC8 should be preventive in nature; that is, an optimum amount of preventive procedures performed at a routine schedule will eliminate many costly equipment breakdowns and forecast impending failures long before they occur. When a failure does occur, the modular design of the UDC8 minimizes repair and downtime. To locate a specific module or file unit, refer to the channel/system unit identification chart on the rear of the logic cabinet.

5.2 PREVENTIVE MAINTENANCE

Since the UDC8 peripheral contains no special mechanical devices, only standard computer system maintenance procedures are required to ensure reliable operation of the equipment. Failures encountered in the UDC8 should be recorded in the established system maintenance log for future reference. Regular entries in the maintenance log of maintenance performed, troubles encountered, and corrective measures taken, can serve as a powerful tool in maintaining system reliability. A mechanical inspection (diagnostic referenced in Paragraph 1.6) and voltage checks should be performed at regular intervals to verify proper operation of the UDC8. Voltages and their required tolerances are listed in Table 5-1. Since each equipment bay has its own H740D Power Supplies, the voltage checks should be performed for each bay. Cooling air filters at the top of the logic cabinet should be checked and cleaned as necessary.

5.3 CORRECTIVE MAINTENANCE

5.3.1 General

The simplicity of the universal digital controller and the logic description provided in this manual, along with the results of the diagnostic tests, normally permit the use of standard troubleshooting techniques for isolating a malfunction quickly and efficiently.

Table 5-1
H740D Voltage Tolerances

Voltage	Tolerance
+5V	±0.250V (input to G729 under full load)
+15V (not used)	
−15V (UDC8-N only)	±1.0V

A special UDC Field Tester has been developed to aid the DEC Field Service Engineer in isolating and correcting UDC problems. The tester is used in conjunction with the standard UDC diagnostic (UDC8-EX) and consists of lamps and switches used to test UDC output and simulate field inputs. It also includes cables that bypass the screw terminals and plug directly into the signal-conditioning modules.

CAUTION
In all cases, when troubleshooting the UDC, discon-
nect screw terminal wiring from signal-conditioning
modules, to eliminate hazardous field voltages.

For economical maintenance under most conditions, replace the inoperative module with a spare module, and return the defective module to DEC for repair or replacement.

NOTE
Be sure that the jumpers in the replacement module
are set up to reflect those in the defective module.

Recommended spare modules are listed in Table 5-2, and recommended component spares are listed in Table 5-3.

5.3.2 Test Equipment Required

Maintenance activities for the UDC8 require standard test equipment and special materials as listed in Table 5-4, and standard hand tools, test cables, and probes.

5.3.3 H740D Power Supply Adjustment

The +5V source should be adjusted for 5 ± 0.250V under full-load conditions. Use the jumper connections on the rear of any G729 Module for access points. Figure 5-1 shows the location of the +5V control.

Table 5-2
Recommended Module Spares

Modules	Module Type	Quantity
0–10V DAC Output*	A233	1
+1 to +5V DAC Output*	A234	1
+4 mA to +20 mA DAC Output*	A235	1
+10 mA to +50 mA DAC Output*	A236	1
DAC*	A633	1
X, Y Selector	G729	1
Bus Data Interface**	M100	1
Bus Data Interface**	M101	1
Device Selector**	M102	1
Device Selector**	M103	1
Inverter	M111	1
NOR Gate	M112	1
Ten 2-Input NAND Gates	M113	1
Eight 3-Input NAND Gates	M115	1
Gating Module	M169	1

*If more than ten of any one of these modules are utilized in the system, then one additional spare should be stocked.

**One or the other depending upon positive or negative bus.

Table 5-2 (Cont)
Recommended Module Spares

Modules	Module Type	Quantity
General-Purpose Flip-Flops	M206	2
Dual-Delay Multivibrator	M302	1
Dual Integrating-One-Shot	M307	1
Variable Clock	M401	1
I/O Bus Receiver	M510	1
Pulse Amplifier	M602	1
Bus Driver	M623	1
Bus Driver	M624	1
12-Bit Flip-Flop Relay Driver*	M684	1
12-Bit Single-Shot Relay Driver*	M686	1
12-Bit Latching Relay*	M802	1
12-Bit Flip-Flop Relay*	M804	1
12-Bit Single-Shot Relay*	M806	1
Bus Receiver-Address Decoder	M851	2
Bus Connector	M935	1
Bus Terminator	M942	1
Isolated Power Cable Board*	W400	1
Common Power Cable Board*	W402	1
Relay Driver Power Cable Board	W403	1
12-Bit Contact Sense (Relay)*	W730	1
12-Bit Contact Interrupt (Relay)*	W732	1
12-Bit Contact Sense (Solid State)*	W740	1
12-Bit Contact Interrupt (Solid State)*	W742	1
I/O Counter*	W734	1

*If more than ten of any one of these modules are·utilized in the system, then one additional spare should be stocked.

Table 5-3
Recommended Component Spares

Components	DEC No.	Quantity
Relay, Quad Form B (used on W730)	12-10116-0	2
Relay, Quad Form C (used on W732)	12-10172-0	2
Mercury-Wetted Latching Form C Relay (used on M802)	12-09672-1	2
Mercury-Wetted Form C (used on M804, M806)	12-09757-1	2
Pig-Tail Fuses, 4A 3AG	90-07219-2	5
Optically Coupled Isolator	19-10845	2
DEC 3568 Transistor (M684 and M686)	15-02937	2

5.3.4 Scanner Clock Adjustment

Scanner Clock in slot E09 (Module M401) should be adjusted to a period of 1.0 μs (1.0 MHz) by adjusting the trimpot on the module while viewing the waveform at pins E09D2 or E09E2 (Figure 5-2).

Table 5-4

Test Equipment Required

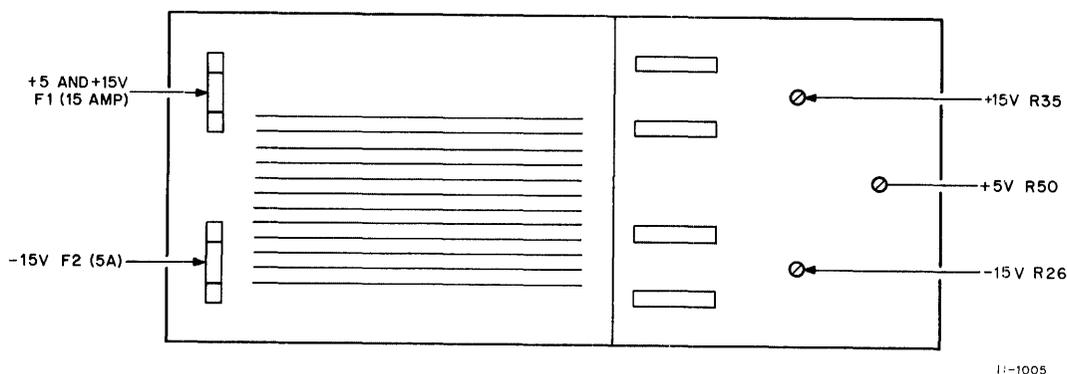| Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630-NA or 260
Oscilloscope	Tektronix	Type 543 or equivalent
Probe (2)	Tektronix	P6010
X10 Probe (2)	Tektronix	P6008
Module Extender*	DEC	Type W982
Test Set	DEC	Optional
Service Kit*	DEC	For single-shot timing adjustments

*Provided with each system.

Figure 5-1   H740D Power Supply Fuses and Adjustment Controls
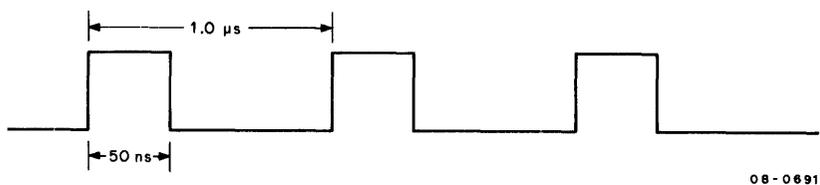
Figure 5-2   Scanner Clock Waveform

5.3.5 Bus Clock Signal Adjustments

System clock (CLK 00) in slot F07 (Module M401) can be adjusted over the range of 175 Hz to 1.75 kHz by adjusting its trimpot while viewing the waveform at pin F06H1. Clock CLK 01 in slot F08 (Module M401) can be adjusted over the range of 1.75 kHz to 17.5 kHz while viewing the waveform at pin F06M1. For testing W734 type modules, these clocks must be set to 1.0 kHz and 16 kHz, respectively, for correct operation of the W734 Module. After the test these clocks should be reset to their original setting.

CHAPTER 6
ENGINEERING DRAWINGS

6.1 GENERAL

This chapter lists DEC block schematics and cabling diagrams that are referenced in other chapters of this maintenance manual (Table 6-1). These drawings are contained in the print set and Volume II of this manual, and provide detailed information about the logic and wiring of the UDC8 peripheral.

Table 6-1
UDC8 Engineering Drawings

Drawing Number	Title
A-ML-IDAC-0	Industrial Data Acquisition and Control
A-PL-IDAC-0-1	Parts List
D-AR-IDAC-0-0	IDAC Arrangements
A-ML-UDC8-N	Digital Input/Output Sub-System (NEG)
A-ML-UDC8-P	Digital Input/Output Sub-System (POS)
A-PL-UDC8-0-0	Digital Input/Output Sub-System (Parts List)
D-DI-UDC8-0-1	Drawing Index List (UDC8)
A-ML-DD01-N	Control and Interface (NEG)
A-ML-DD01-P	Control and Interface (POS)
A-PL-DD01-0-0	Control and Interface (Parts List)
C-DI-DD01-0-01	Drawing Index (DD01)
D-AD-7006825-0-0	Wired Assembly (DD01)
A-PL-7006825-0-0	Wired Assembly (Parts List)
D-MU-DD01-0-02	Module Utilization List
A-PL-DD01-0-02	Module Utilization List (Parts List) (NEG and POS)
D-BS-DD01-0-03	UDC Address Scanner and Register
D-BS-DD01-0-04	Change of State (COS) Gates and Register
D-BS-DD01-0-05	UDC Digital Input Multiplexer
D-BS-DD01-0-06	Device Select and Input Interrupt Generator
D-BS-DD01-0-07	UDC Bus Drivers and Receivers
D-BS-DD01-0-08	Bus Receivers and Address Decoders (DD01)
D-IC-DD01-0-10	I/O Connectors
K-WL-DD01-0-09 (Complete)	Wire List (DD01)
A-ML-DD02-0	System Unit
A-PL-DD02-0-0	System Unit (Parts List)
C-DI-DD02-0-01	Drawing Index (DD02-0)
D-AD-7006838-0-0	Wired Assembly (DD02-0)
A-PL-7006838-0-0	Wired Assembly (Parts List)

Table 6-1 (Cont)
UDC8 Engineering Drawings

Drawing Number	Title
D-MU-DD02-0-02	Module Utilization List
A-PL-DD02-0-02	Module Utilization List (Parts List)
D-BS-DD02-0-04	Bus Receivers and Address Decoders
K-WL-DD02-0-03 (Complete)	Wire List (DD02-0)
E-CS-A233-0-1	0V to +10V Output Buffer Amplifier
D/E-CS-A234-0-1	+1V to +5V Output Buffer Amplifier
D/E-CS-A235-0-1	4 mA to 20 mA Current Output Buffer
D/E-CS-A236-0-1	10 mA to 50 mA Current Output Buffer
D-CS-A633-0-1	4–10 Bit D/A Converter
B-CS-G729-0-1	X-Y Jumper Card
B-CS-G772-0-1	Power Connector Module
ASP-H738-A-0	DAC Option Power Supply
C-CS-M100-0-1	Bus Data Interface
B-CS-M101-0-1	Bus Data Interface
D-CS-M102-0-1	Device Selector
B-CS-M103-0-1	Device Selector
B-CS-M111-0-1	Inverter
B-CS-M112-0-1	NOR Gate
B-CS-M113-0-1	10 2-Input NAND Gates
B-CS-M115-0-1	8 3-Input NAND Gates
C-CS-M169-0-1	Gating Module
B-CS-M206-0-1	Six Flip-Flops
B-CS-M302-0-1	One Shot Delay
C-CS-M304-0-1	One Shot Delay
B-CS-M307-0-1	Integrating One Shot
B-CS-M401-0-1	Variable Clock
C-CS-M510-0-1	I/O Bus Receiver
B-CS-M602-0-1	Pulse Generator
C-CS-M623-0-1	Bus Driver
C-CS-M624-0-1	Bus Driver
C-CS-M633-0-1	Bus Driver
D-CS-M684-0-1	12-Bit Flip-Flop Relay Driver M684
D-CS-M686-0-1	12-Bit Single-Shot Relay Driver
D-CS-M802-0-1	Latching Relay Output Driver
D-CS-M804-0-1	12-Bit Flip-Flop Relay Module M804
D-CS-M806-0-1	12-Bit Single-Shot Relay M806
C-CS-M851-0-1	Bus Receiver Addr Decoder
B-CS-M903-0-1	Connector, Flat Mylar
C-CS-M942-0-1	Bus Terminator
D/E-CS-W400-0-1	Isolated Power Cable Board W400
D/E-CS-W402-0-1	Common Power Cable Board W402
D-CS-W403-0-1	Relay Driver Power Cable Board W403
C-CS-W730-0-1	12-Bit Contact Sense (Relay) W730
D-CS-W732-0-1	12-Bit Contact Interrupt (Relay) W732
D-CS-W740-0-1	12-Bit Contact Sense (Solid State) W740
D-CS-W742-0-1	12-Bit Contact Interrupt (Solid State) W742
D-CS-W734-0-1	Counter Module
B-CS-849A-0-1	Power Control
D-CS-5409728-0-1	Regulator Board for H740D

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