digital

hardware

DECstation technical manual

DECstation technical manual

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CHAPTER 1
INTRODUCTION

1.1 PURPOSE

This manual will help you isolate and repair DECstation equipment malfunctions. It will also be helpful when interfacing the DECstation with systems and devices other than those specifically designed for this system.

NOTE

Although references are made to optional devices throughout this manual, appropriate manuals (Table 1-1) for these devices must be consulted for detailed operating and troubleshooting information.

Table 1-1 Related Documentation

Document	Document No.
DECstation User's Guide (hardware)	EK-VTX78-UG-001
DECstation User's Guide (software)	DEC-S8-0878A-A-D
DECstation Technical Manual	EK-VTX78-TM-001
VT78 MOS Memory Diagnostic	MAINDEC-08-DKVTA-A-D
VT78 CPU Diagnostic	MAINDEC-08-DKVTB-A-D
4K-32K PDP8A Processor Exerciser	MAINDEC-08-DJEXC-B-D
RX8/RX01 Diagnostic Programs	MAINDEC-08-DIRXA-DD
RX8/RX01 Data Reliability Exercise Program	MAINDEC-08-DIRXB-ED
LA180 Printer Diagnostic	MAINDEC-08-DILAC-B-D
LQP-8 Printer Diagnostic	MAINDEC-08-DHLQA-B-D

1.2 GENERAL

The DECstation can be an intelligent terminal in a distributed data processing network or a stand-alone computer. Figures 1-1 and 1-2 show typical intelligent terminal and stand-alone system configurations.

As an intelligent terminal, the minimum system configuration includes the VT78 terminal and an external program loading device. Programs can also be loaded into the system from a host computer.

As a stand-alone computer, the DECstation has a mass storage device such as a floppy disk drive system. Both configurations, intelligent terminal and stand-alone system, may have impact printers for hard copy.

The VT78 terminal combines the functions of a conventional I/O keyboard/video display with those of a sophisticated minicomputer to form a complete computer system within a terminal. It has a full typewriter-style keyboard, capable of generating both upper- and lower-case characters in ASCII code, and a 19-key auxiliary keypad. The video display can show 24 lines of 80 characters. The system utilizes direct cursor addressing.

The processor, located on the processor module, controls all of the computer functions including those of the random access MOS 16k word (32k byte) memory. The processor module also contains interface circuits (see Chapter 2) which process serial and parallel data. This permits the addition of peripheral devices via connectors on the I/O distribution panel (rear of terminal).

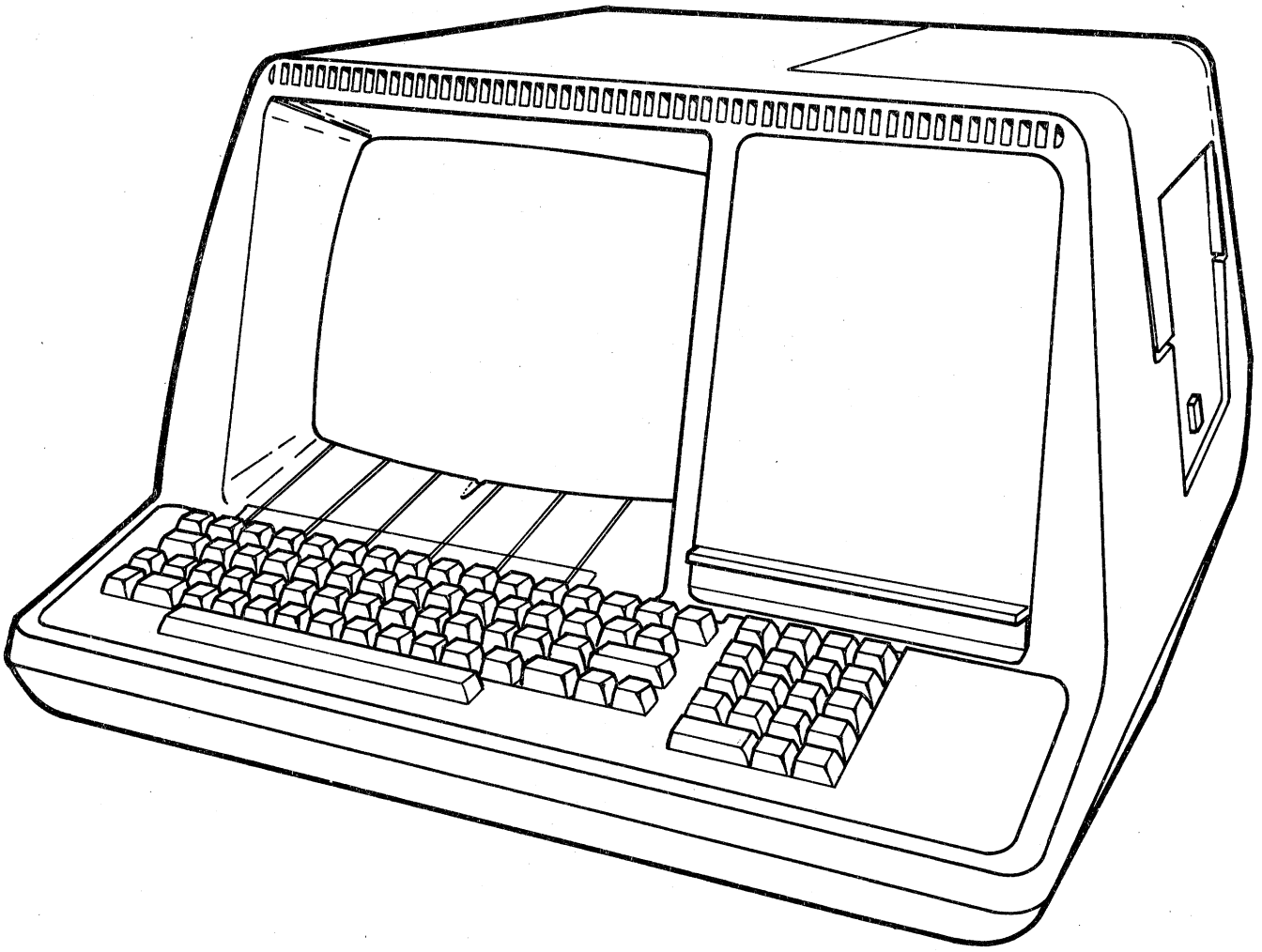

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Figure 1-1 DECstation: Intelligent Terminal Configuration

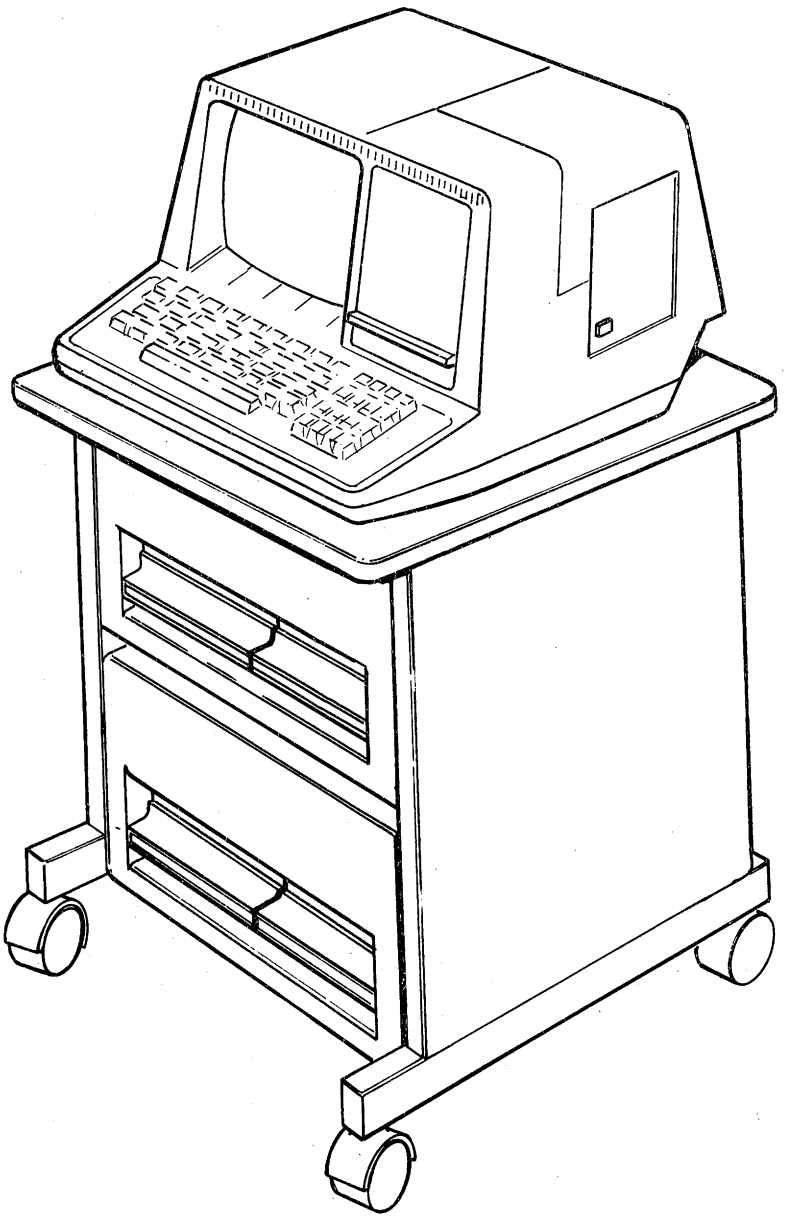

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Figure 1-2 Typical Stand-Alone Computer Configuration

CHAPTER 2
THEORY OF OPERATION

2.1 OVERALL SYSTEM DESCRIPTION

The VT78 terminal (Figure 2-1) has three major functional components: the microprocessor, the keyboard/video display, and the dc power supply.

The processor is a 12-bit, fixed word length, parallel transfer computer using two's complement arithmetic. The processor contains a CPU, a 16k word main memory, a panel memory, an MR78 program loading device interface circuit, a real time clock, and four peripheral I/O interfaces.

The system operation is started by the application of prime power to the dc power supply initiating the power-up sequence. Upon completion of the power-up sequence, the diagnostics (resident-in-panel memory) are performed to verify that the major system components are operating correctly. If there is a malfunction within the system, the panel memory will issue a halt message and provide general status information. Two indicators (DC OK and CPU OK), located at the rear of the terminal, also provide status information.

The panel memory has 256 words of read/write Random Access Memory (RAM) for variable storage and a 1k Read Only Memory (ROM). The ROM contains the resident diagnostics, an MR78 pseudo-papertape loader, and an RX78 bootstrap loader.

Program loading is initiated by momentarily pressing the START switch. This causes the panel memory to select the appropriate program loading device to load its program into main memory.

There are two program loading devices available with the DECstation. One is the MR78 and the other is the floppy disk drive system. The MR78 has priority over the floppy disk drive system when the START switch is pressed. Each device has its own interface. The MR78 interface is uni-directional, receiving 8-bit parallel data from the MR78 in "papertape" format. The floppy disk drive system interface is bi-directional (i.e., programs may be written or read) and permits system interface with two RX78 floppy disk drive systems.

Main memory has 48 NMOS dynamic 4k RAM chips organized as 16k 12-bit words. It has three basic cycles: read-refresh, read-wait, and read-write.

The DECstation has three Serial Line Units (SLUs). The SLU 2 interface permits the processor (using EIA signaling levels) to communicate with any full duplex device. It provides error detection at transmission rates ranging from 50 baud to 19,200 baud. Baud rates, word parity, word length, and stop bit selection are under program control. SLU 3 can communicate with any EIA full duplex device which handles 8-bit data without parity and only one stop bit. Unlike SLU 2, this interface does not have error checking but does provide the same baud rate selection under program control. SLU 1 is similar to SLU 3 with the exception of the EIA signaling levels. It is hardwired directly to the keyboard/video display I/O.

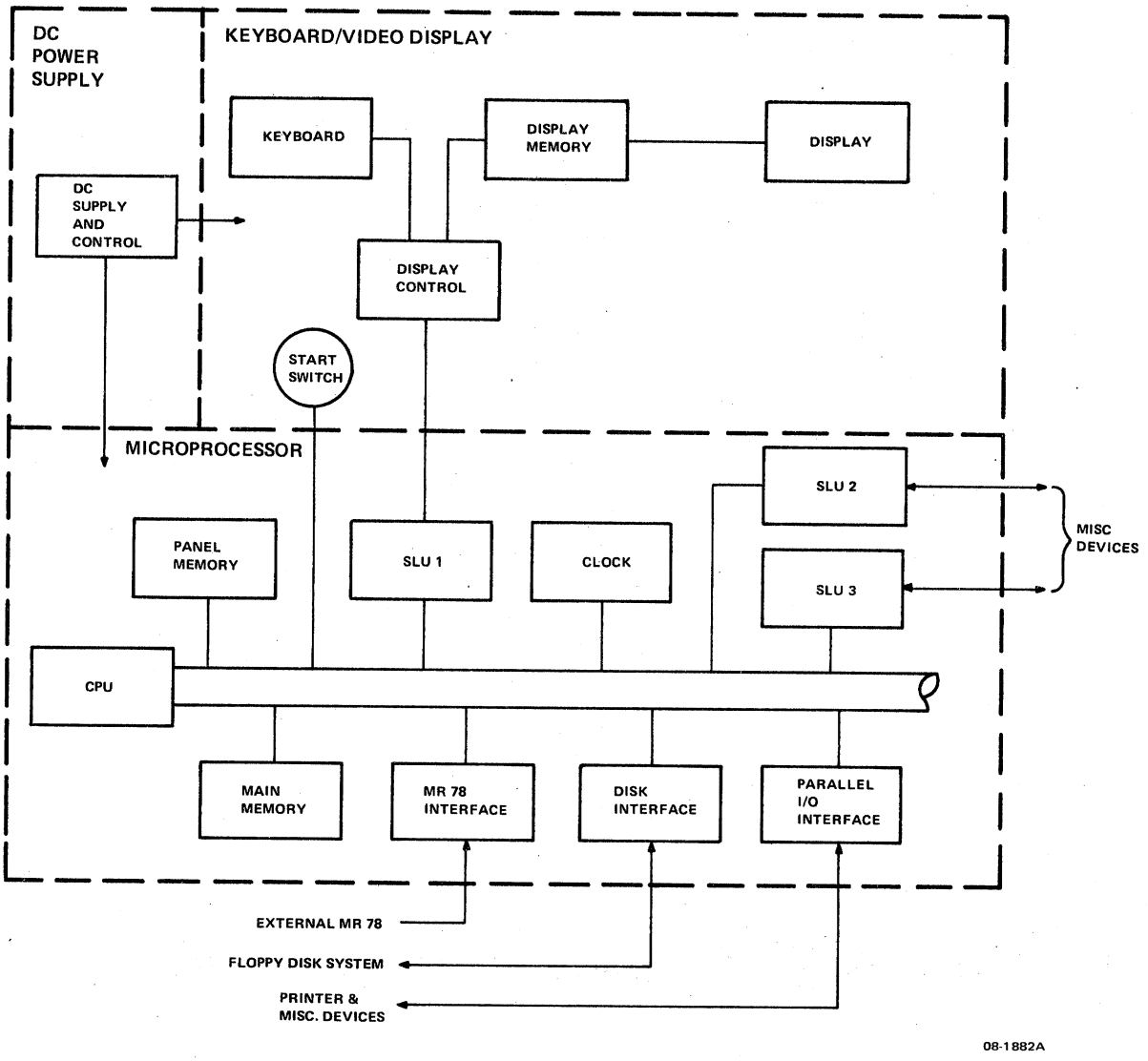

Figure 2-1 DECstation Block Diagram

The parallel I/O interface is a 12-bit bi-directional data port which responds to the instruction sets of either the LA78 or the LQP78 printers. The particular instruction set is determined by the printer used and its associated cable.

The keyboard/video display (Figure 2-2) enables the user to communicate with the microprocessor and control all of the system peripheral devices.

Characters to be displayed on the video screen are transferred to the display via SLU 1 and are stored in a display RAM in ASCII format. There is a RAM location for each character which appears on the screen of the video display; hence, the RAM consists of 1,920 7-bit words (24 lines of 80 characters).

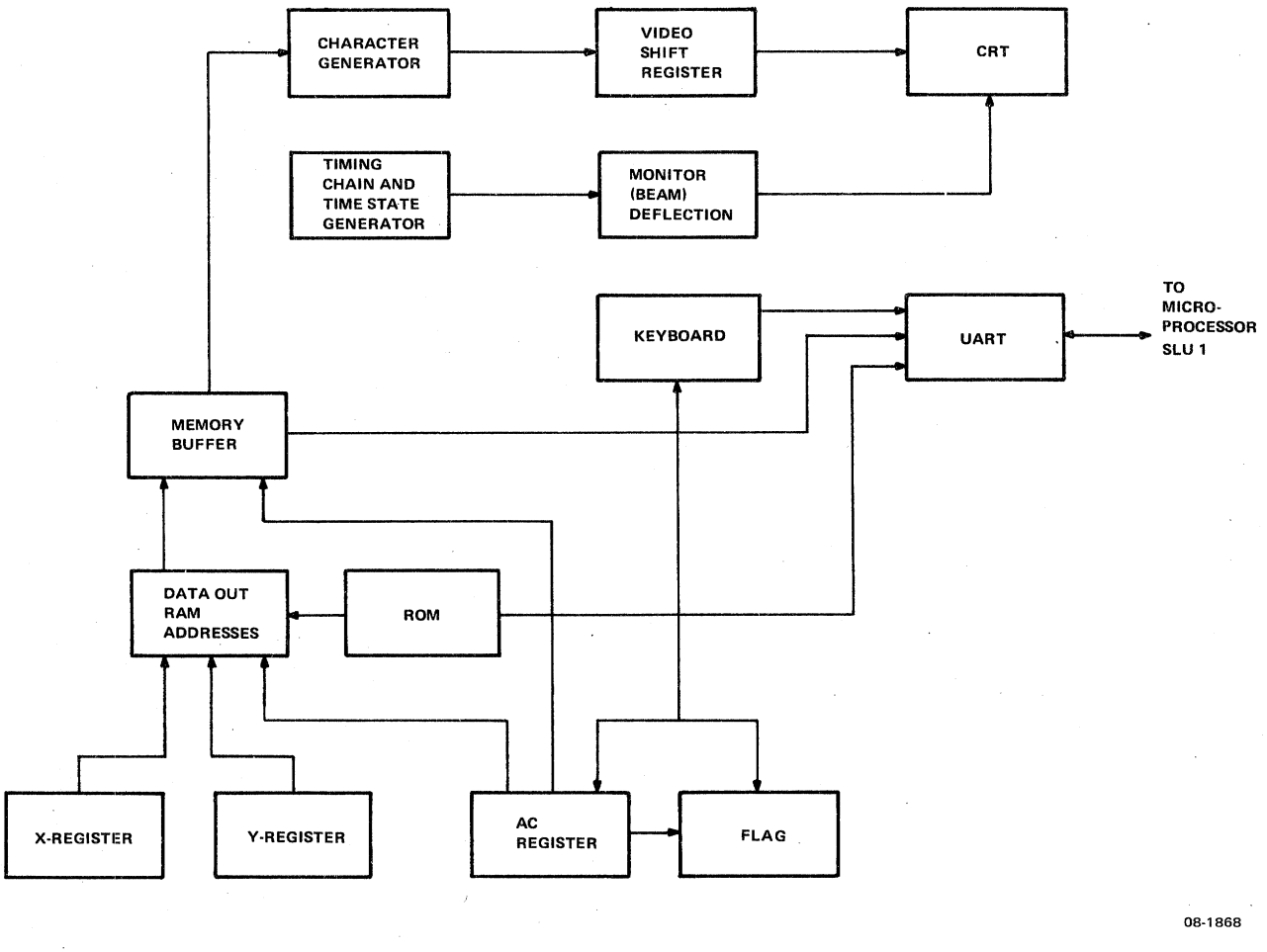

Figure 2-2 Keyboard/Video Display Block Diagram

Characters fetched from the display RAM are applied to a character-generating ROM. The output of this ROM, which is one horizontal line (7 bits) of the 7x7 character matrix (Figure 2-3), is loaded into a video shift register. The video shift register is then shifted to provide an intensity signal to the video display. As the current character is being shifted, the next character is fetched from RAM and applied to the character generator. This process continues until all 80 characters for the line have been processed. When the end of the line is reached, the RAM X-address (horizontal address) is reset to zero. These steps are repeated until all seven lines of the current set of characters have been placed on the screen. The display control then advances to the next value of Y for the next line of characters. Meanwhile, three blank lines (four for 50 Hz units) between the lines of characters (and the cursor) are placed on the screen.

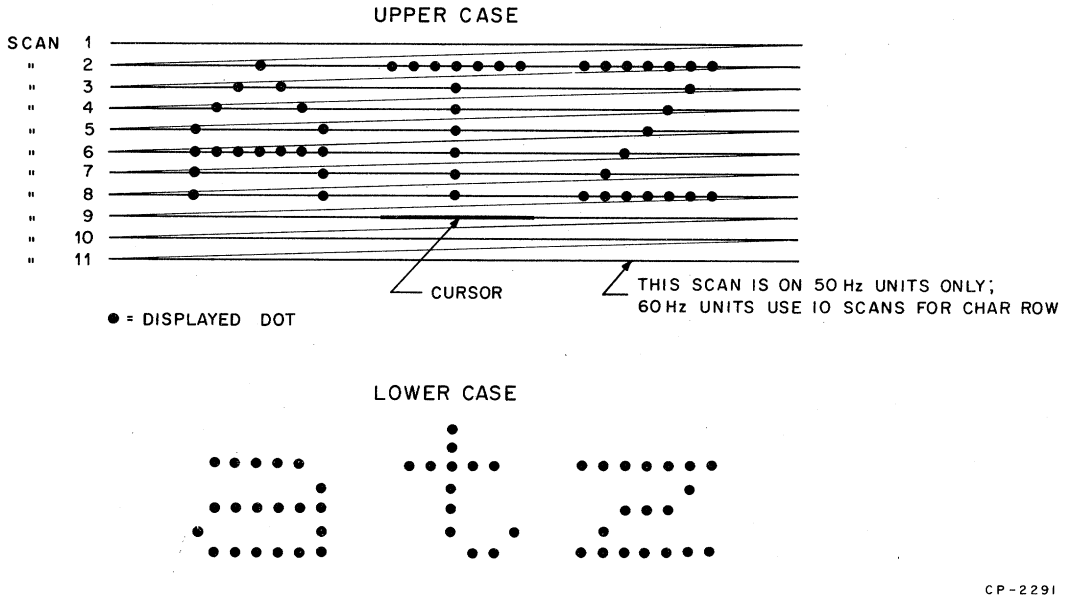

Figure 2-3 7X7 Character Matrix

An internal display processor (not to be confused with the main processor) handles the auxiliary functions of:

1. Updating the X and Y registers.
2. Scanning the keyboard.
3. Clearing the display.
4. Storing incoming characters.
5. Addressing the cursor.
6. Generating escape sequences.

The timing generator chain and time state generator provide vertical and horizontal deflection signals for the CRT, as well as providing timing signals to the display processor and display Universal Asynchronous Receiver/Transmitter (UART). (See Figure 2-4.)

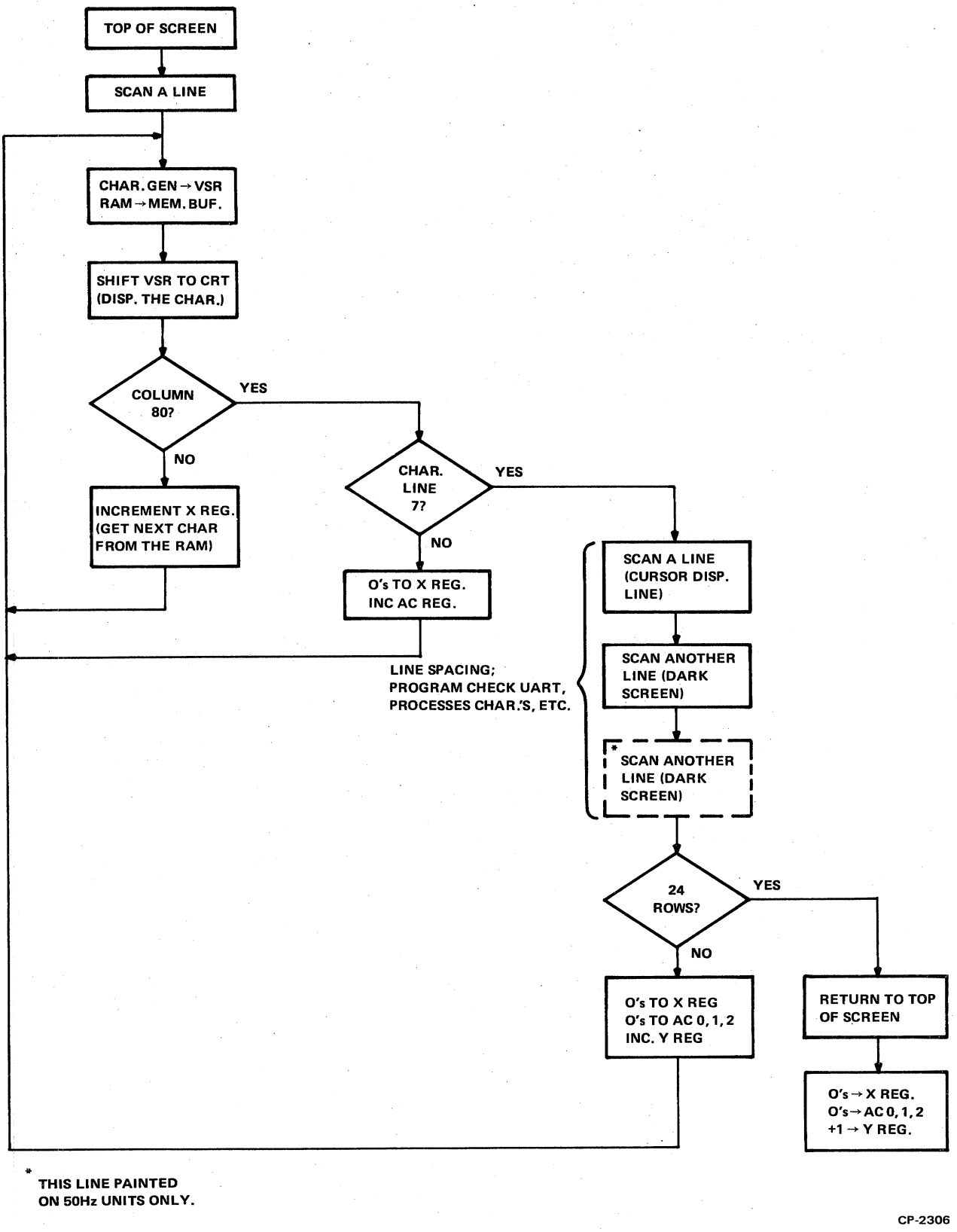

Figure 2-4 Display Cycle Flow Diagram

Keyboard data entered by an operator is transferred to the processor under control of the keyboard/video display microprogram. During vertical retrace time, the microprogram checks the keyboard, searching for a typed key. This is performed 60 times each second (50 times each second on 50 Hz units). To do this the program tests the condition of every key in the keyboard. When it finds a typed key, the ASCII code for the key character is loaded into the UART and transmitted to the VT78 main processor.

At the beginning of every keyboard routine, the program checks the status of the UART. If the UART is still transmitting the previous entry, the program makes no further test of the keyboard. If the UART is not transmitting, the program tests the keyboard to determine if the previously processed keys are still down. If they are, the program does not process them again. Instead, it exits the keyboard routine. When the previously processed keys have been released, the program resumes keyboard testing.

The dc power supply block diagram is shown in Figure 2-5.

Setting the POWER ON/OFF switch to ON causes prime power to be applied to a voltage doubler or a full wave rectifier, depending on the source of the prime power. When the prime power source is 115 V, the voltage select switch is set to select the voltage doubler circuit. When the prime power source is 230 V, the selector switch is set to select the full wave rectifier.

Regardless of the prime power source, the resultant voltage doubler or full wave rectifier output will range from 230 Vdc to 360 Vdc. This is applied to the flyback inverter.

The flyback inverter converts the dc input to 20k Hz which is stepped down by a transformer to produce three output voltages. These voltages are rectified and filtered to become the sources of +5 Vdc, -12 Vdc, and +12 Vdc for the entire VT78 terminal. Regulators are provided at the -12 Vdc and +12 Vdc outputs to ensure that these voltages remain within their regulation band of plus or minus five percent.

The 5 Vdc output is sensed by the control circuit which adjusts the on/off duty ratio of the inverter to maintain this output within its five percent regulation band.

The control power circuit provides startup voltages for the control circuit before the inverter is running.

The dc power supply output voltages are checked in the main processor module by a voltage comparator which indicates an error by turning off the DC OK indicator, if there are any voltages absent or out of tolerance. This circuit will prevent any further operation of the DECstation until the malfunction is corrected.

2.2 DETAILED CIRCUIT ANALYSIS

2.2.1 Microprocessor

2.2.1.1 CPU – The entire CPU (Figure 2-6) is contained on a single 40-pin IC. Table 2-1 lists all of the pin assignments and provides a brief functional description of each.

The accumulator is a 12-bit register with which arithmetic and logical operations are performed. Data words may be fetched from memory to the accumulator or transferred from the accumulator for storage in memory. Arithmetic and logical operations involve two operands, one is held in the accumulator and the other is fetched from memory. The result of the operation remains in the accumulator. The accumulator may be cleared, complemented, tested, incremented, or rotated under program control. The accumulator also serves as an I/O. All programmed data transfers pass through the accumulator.

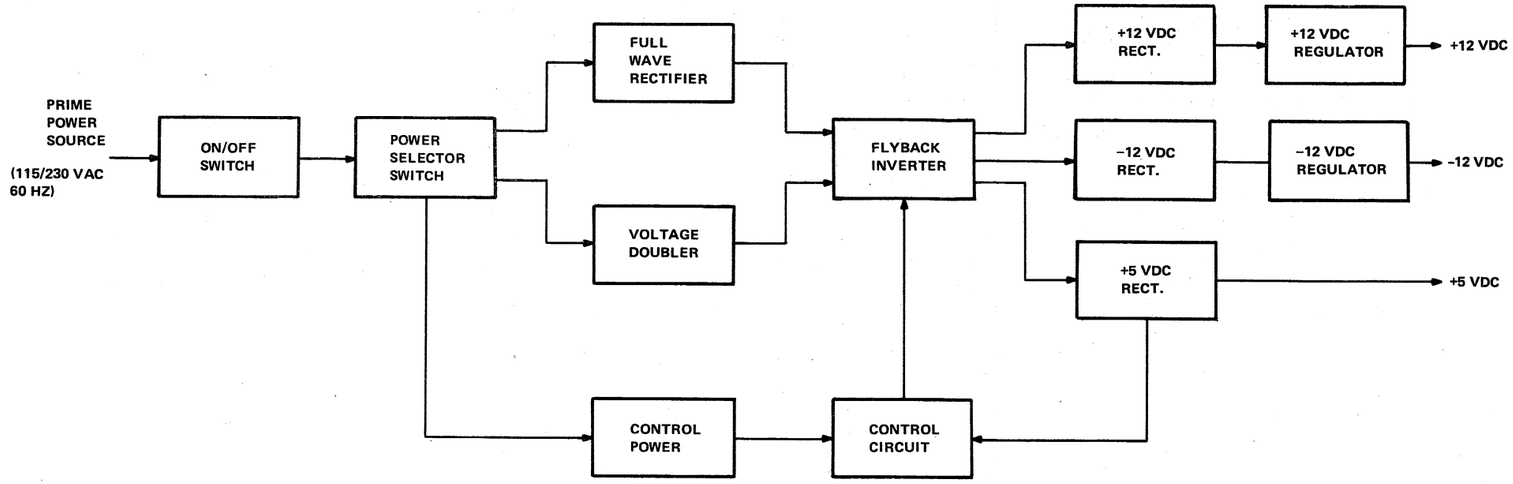

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Figure 2-5 DC Power Supply Block Diagram

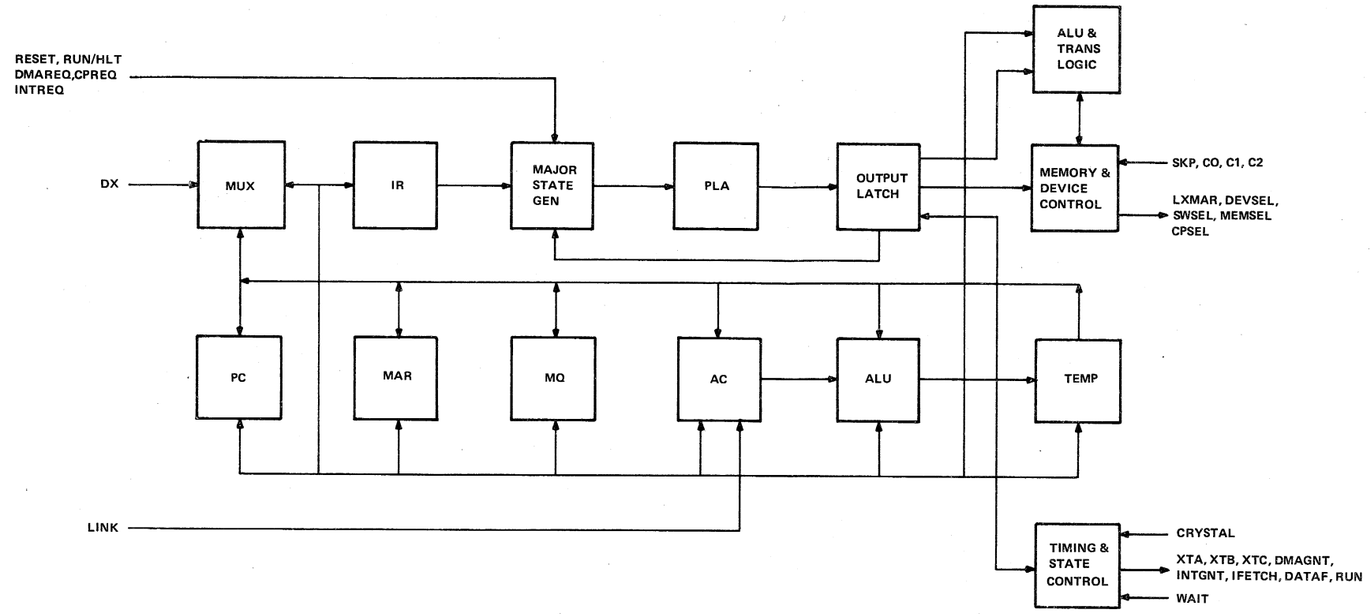


Figure 2-6 CPU Block Diagram

Table 2-1 CPU Pin Assignments

Pin	Symbol	Active Level	Function
1	Vcc		Supply voltage.
2	RUN	H	Indicates the run state of the CPU and may be used to power down the external circuitry. The ground going transition of this signal is used to detect the HLT instruction.
3	DMAGNT	H	Direct memory access grant; DX lines are three state (always low).
4	DMAREQ	L	Not used (tied to Vcc).
5	CPREQ	L	Control panel request, a dedicated interrupt which bypasses the normal device interrupt request structure.
6	RUN/HLT	L	Pulsing the RUN/HLT line causes the CPU to alternately run and halt by changing the state of the internal RUN/HLT flip-flop.
7	RESET	L	Clears the AC and loads 7777_8 into the PC. CPU is halted.
8	INTREQ	L	Peripheral device interrupt request.
9	XTA	H	External coded minor cycle timing, signifies input transfers to the processor.
10	LXMAR	H	The load external address register is used to store memory and peripheral address externally.
11	WAIT	L	Not used.
12	XTB	H	External coded minor cycle timing, signifies output transfers from the processor.
13	XTC	H	External coded minor cycle timing is used with the select lines to specify read or write operations.
14	OSC OUT		Crystal input to generate the internal timing (also external clock input).

Table 2-1 CPU Pin Assignments (Cont)

Pin	Symbol	Active Level	Function
15	OSC IN		Refer to pin 14 (OSC OUT); also external clock ground.
16	DXO		DataX; multiplexed data in, data out.
17	DX1		Refer to pin 16.
18	DX2		Refer to pin 16.
19	DX3		Refer to pin 16.
20	DX4		Refer to pin 16.
21	DX5		Refer to pin 16.
22	DX6		Refer to pin 16.
23	DX7		Refer to pin 16
24	DX8		Refer to pin 16.
25	DX9		Refer to pin 16.
26	GND		Ground.
27	DX10		Refer to pin 16.
28	DX11		Refer to pin 16.
29	LINK	H	Link flip-flop.
30	DEVSEL	L	Device select for I/O transfers.
31	SWSEL	L	Switch register select for the OR THE SWITCH REGISTER INSTRUCTION (OSR). OSR is a group 2 operate instruction which reads a 12-bit external switch register and ORs it with the contents of the AC.
32	C0	L	Control line inputs from the peripheral device during an I/O transfer (Table 2-2).
33	C1	L	Refer to pin 32.
34	C2	L	Not used (tied to Vcc).

Table 2-1 CPU Pin Assignments (Cont)

Pin	Symbol	Active Level	Function
35	SKP	L	Skips the next sequential instruction if active during an I/O instruction.
36	IFETCH	H	Instruction fetch cycle.
37	MEMSEL	L	Memory select for memory transfers.
38	CPSEL	L	The control panel memory select becomes active, instead of MEMSEL for control panel routines. Signal may be used to distinguish between control panel and main memories.
39	INTGNT	H	Peripheral device interrupt grant.
40	DATAF	H	Data field indicates the execute phase of indirectly addressed AND, TAD, ISZ, and DCA instructions so that the data transfers are controlled by the data field DF and not the instruction field (IF), if extended memory control hardware is used to extend the addressing space from 4k to 16k words.

Table 2-2 Control Line Functions

Control Lines			Operation	Description	
C0	C1	C2			
H	H	H	DEV	AC	The content of the AC is sent to the device.
L	H	H	DEV	AC;CLA	The content of the AC is sent to a device and then the AC is cleared.
H	L	H	AC	AC v DEV	Data is received from a device, ORed with the data in the AC, and the result is stored in the AC.
L	L	H	AC	DEV	Data is received from a device and loaded into the AC.
*	H	L	PC	PC + DEV	Not used.
*	L	L	PC	DEV	Not used.

* = Don't care.

The MQ register is a 12-bit temporary register which is program accessible. The contents of the accumulator may be transferred to the MQ register for temporary storage. The contents of the MQ register can be ORed with the accumulator and the result stored in the accumulator. The contents of the accumulator and the MQ register can also be exchanged.

The 12-bit memory address register contains the address of the memory location currently selected for reading or writing. The memory address register can also be used as an internal register for microprogram control during data transfers between memory and peripherals.

The 12-bit program counter contains the address of the memory location from which the next instruction is fetched. During an instruction fetch, the contents of the program counter is transferred to the memory address register, and the program counter is then incremented by one. When there is a jump or JMS to another address in memory, the jump or JMS address is set into the program counter. Branching normally takes place under program control. A Skip instruction increments the program counter by one, causing the next instruction to be skipped.

The Skip instruction may be unconditional or conditional, depending on the state of the accumulator and/or the link.

The Arithmetic and Logical Unit (ALU) performs both arithmetic and logical operations—two's complement binary addition, AND, OR, and complement. The ALU can perform a single position rotate either to the left or to the right. A double rotate is implemented in two single-bit rotates. The ALU can also shift by three positions to implement a byte swap in two steps. The accumulator is always one of the inputs to the ALU. However, under internal microprogram control, the accumulator may be gated off and all ones or all zeros gated in. The second input may be any one of the other registers under internal microprogram control.

During an instruction fetch, the 3-bit Instruction Register (IR) contains the instructions to be executed by the CPU. The IR specifies the initial step of the microprogram sequence for each instruction and is also used as an internal register to store temporary data for microprogram control.

The DX (input/output) multiplexer handles data, address, and instruction transfers between the CPU and external devices such as memory and peripherals on a time-multiplexed basis.

During an instruction fetch, the instruction to be executed is received from memory via the DX multiplexer and loaded into the IR. The Programmed Logic Array (PLA) is then used for the correct sequencing of the CPU for the appropriate instruction. After an instruction is completely sequenced, the major state of the priority network decides whether the system is going to fetch the next instruction in sequence or service one of the external request lines.

The PLA output latch latches the PLA output, thereby permitting the PLA to be pipelined; it fetches the next control sequence while the CPU is executing the current sequence.

The CPU circuit timing sequence is shown in Figure 2-7.

The CPU generates all the timing and state signals used in the microprocessor.

The memory and device control unit provides external control signals to communicate with peripheral devices (DEVESEL), switch register (SWSEL), memory select (MEMSEL), and/or control panel memory (CPSEL). During I/O instructions this unit also modifies the PLA outputs, depending on the states of the four device control lines. The ALU and register transfer logic provides the control signals for the internal register transfers and ALU operation.

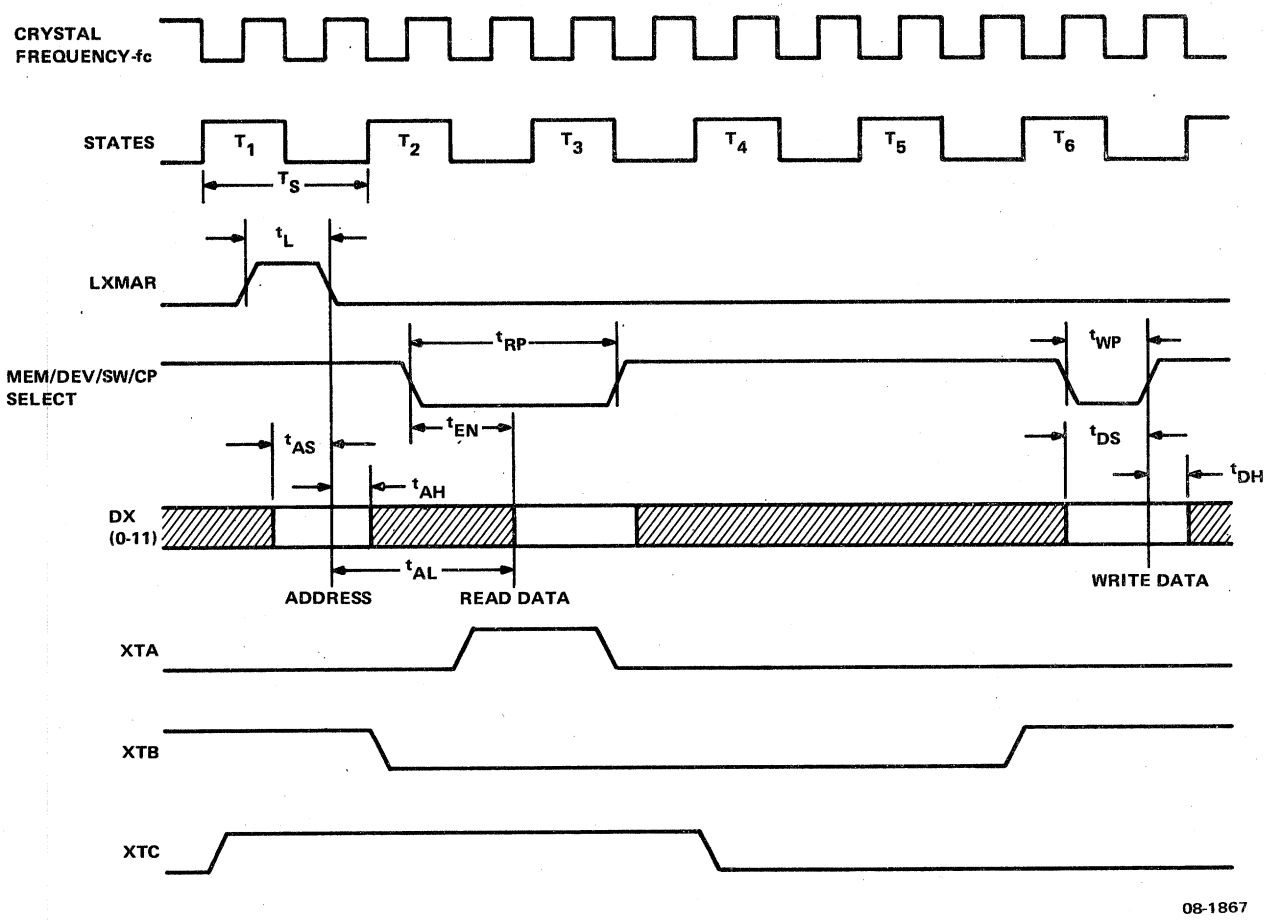


Figure 2-7 CPU Timing Diagram

For memory reference instructions, a 12-bit address is sent on the DX lines. Load External Memory Address Register (LXMAR) is used to clock an external register (MAR) to store the address information externally. The external address register then contains the device address and control information.

Various CPU request lines are priority sampled if the next cycle is an instruction fetch cycle. The current state of the CPU is available externally.

For memory reference instruction, the MEMSEL line is active. For I/O instructions the DEVESEL line is active. Control lines, therefore, distinguish the contents of the external register as memory or device address.

External device sense lines (C0, C1, C2, and Skip) are sampled if the instruction being executed is an I/O instruction. Control panel MEMSEL, CPSEL, and SWSEL become active low for data transfers between the CPU and control memory and the switch register, respectively.

The CPU instructions are 12-bit words stored in memory. The CPU makes no distinction between instructions and data. It can manipulate instructions as stored variables or execute data as instructions when it is programmed to do so. There are three general classes of instructions: Memory Reference Instructions (MRI), Operate Instructions (OPR), and Input/Output Transfer Instructions (IOTs).

2.2.1.2 Main Memory – Figure 2-8 is a simplified block diagram of main memory and its associated control circuits. Figures 2-9 and 2-10 show the read/refresh and read/write memory cycle timing sequences.

Data flow between the CPU and memory is controlled by signal XTC which is generated by the CPU. When XTC is low, memory is in the read cycle. When XTC is high, memory is in the refresh, wait, or write cycle.

During the read portion of XTC, the CPU selects a particular address in memory by placing the contents of its internal memory address register on the DX lines. When a valid address is present on the DX bus (lines DX00 through DX05) LXMAR goes high—loading the external 12-bit memory address register and the 6-bit row latches within the memory chips. The row latches are loaded with the high order bits (0 through 5). Approximately 270 ns later, the contents of the memory address register (MAR 6 through 11) are loaded into the memory chip column address. When MEMSEL is pulsed high, it clocks the read flip-flop, gating memory data to the DX bus to be read by the CPU.

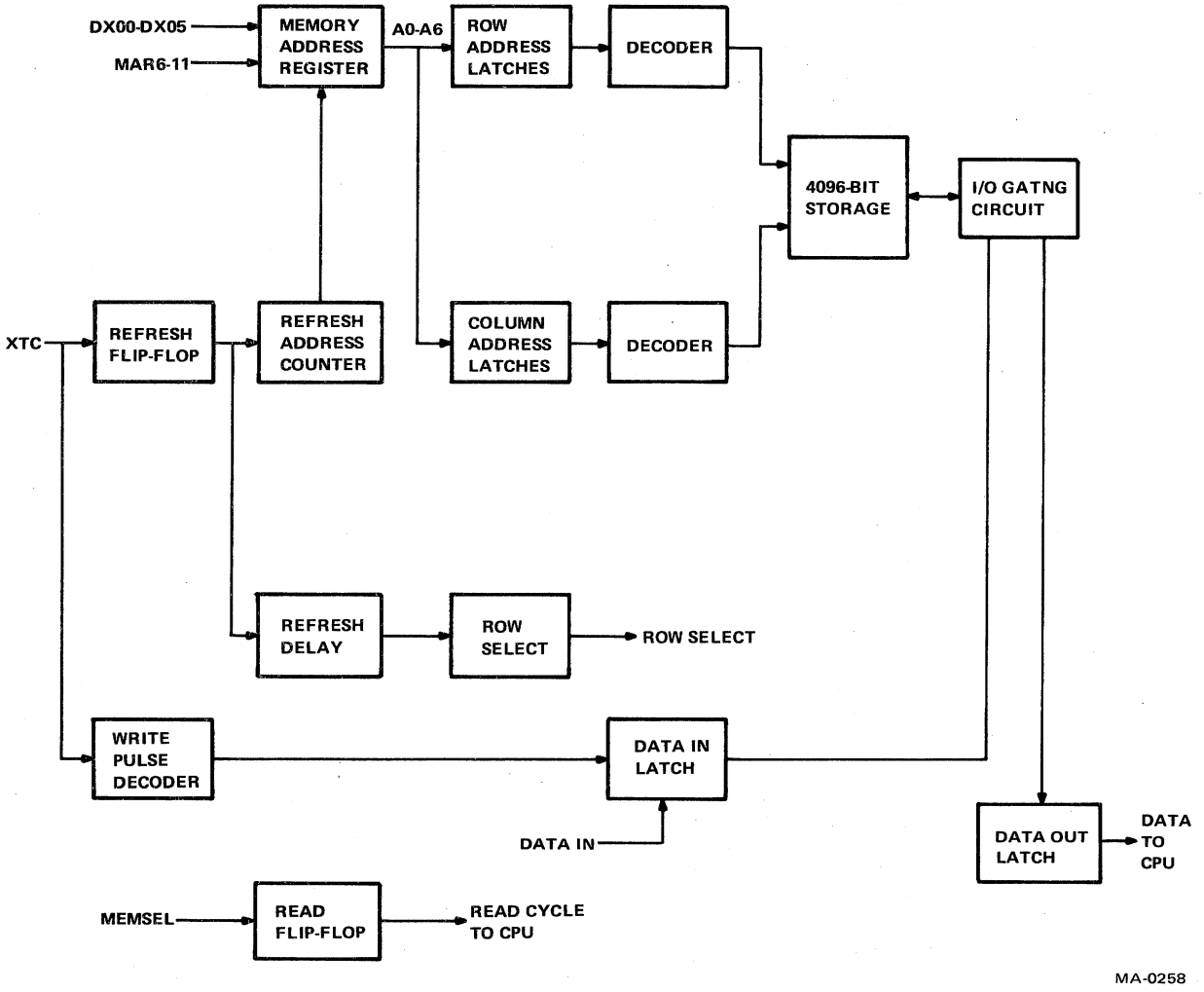


Figure 2-8 Main Memory Block Diagram

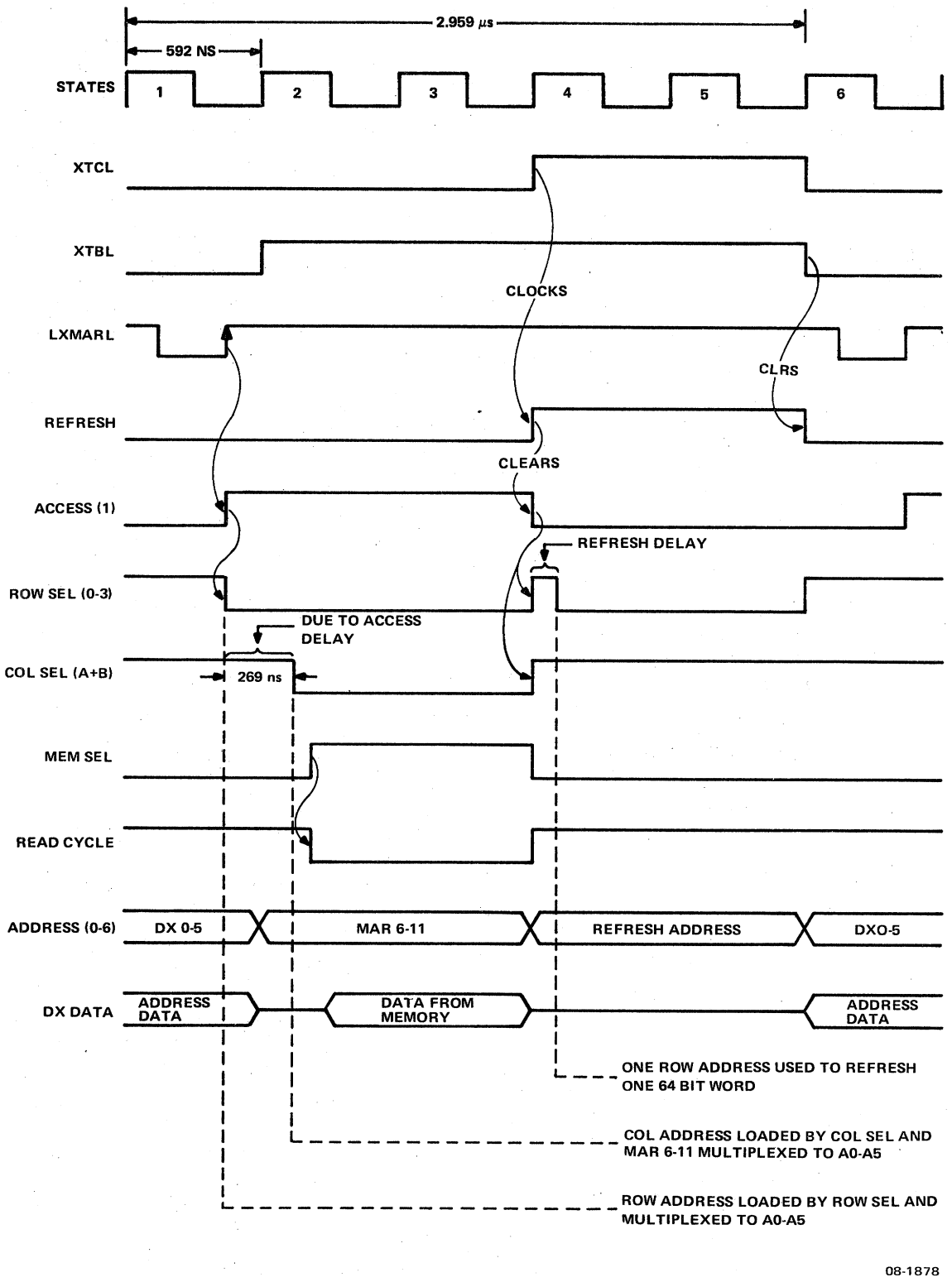


Figure 2-9 Read/Refresh Timing Diagram

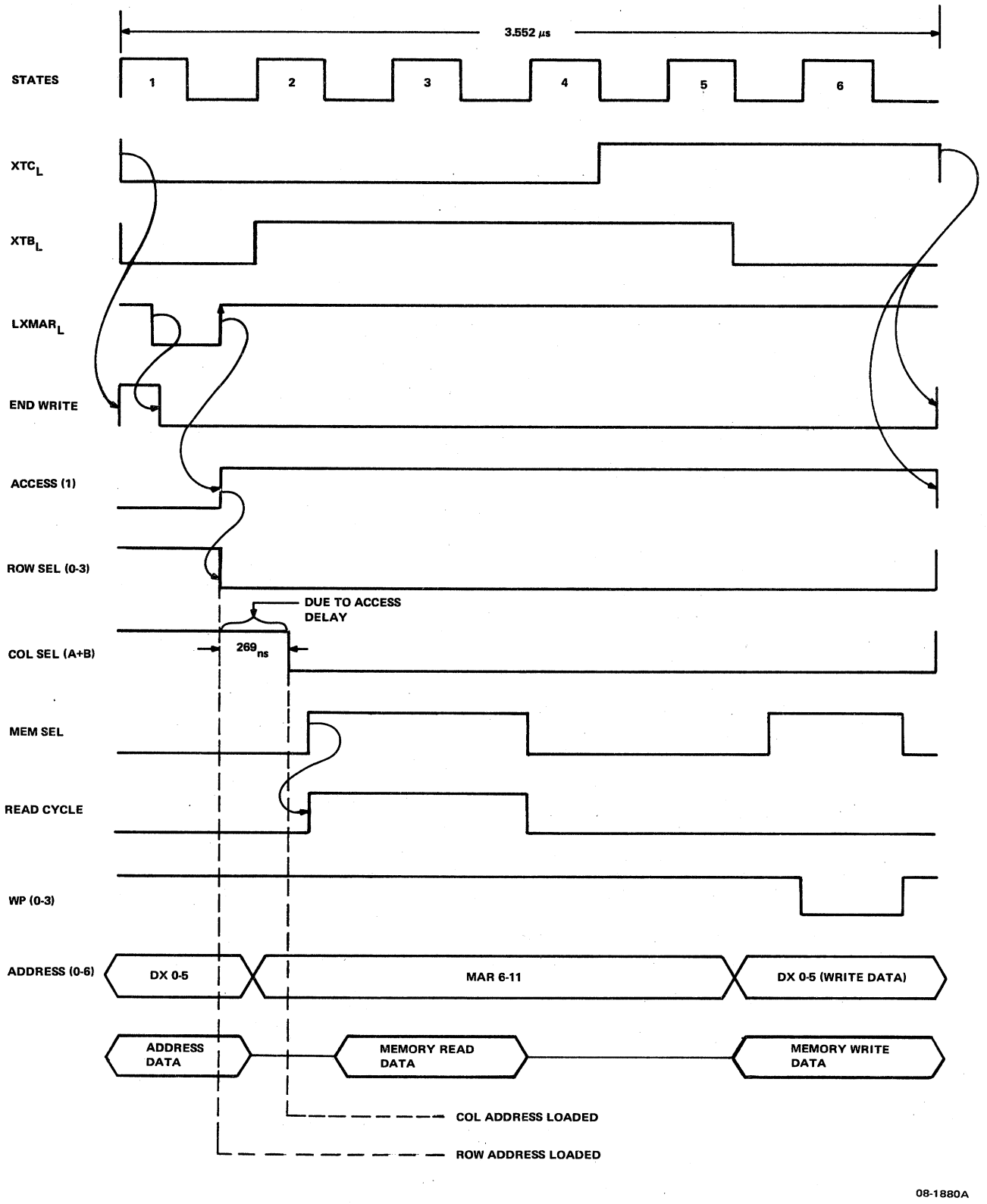


Figure 2-10 Read/Write Timing Diagram

The refresh cycle is a method of preserving data within main memory, when a read or write function is not being performed at that particular address. This cycle is initiated in the second portion of XTC during every second IFETCH. When XTC goes positive, it clocks the refresh flip-flop. The refresh flip-flop, in turn, causes row select to be asserted low after a refresh delay of 270 ns. The refresh address is now loaded into the memory chip row latches to refresh the 64 bits of that row address.

Refresh cycles occur every second instruction fetch cycle, and all 64 memory chip addresses must be refreshed in less than 2 ms. During the next refresh cycle the address is incremented and loaded to refresh the data again. If the processor is stopped, the refresh cycle will occur every eight XTC cycles.

If the second portion of XTC is to be a write cycle, the refresh address will not be loaded. The address used during the read cycle will become the write address. When XTC and MEM SEL are high, a write pulse (WPO through WP3) will gate DX bus data into main memory, after a delay to ensure that valid write data is present on the DX lines.

2.2.1.3 Panel Memory – The panel memory has 256 words of static read/write memory for variable storage and a 1k ROM. The ROM contains the handler which analyzes the panel requests, the floppy disk drive system bootstrap, a pseudo papertape binary loader for use by the MR78, and a resident diagnostic.

Figure 2-11 is a flow diagram showing the operation of panel memory.

When the system is initially powered up or when the START switch is pressed, panel memory is invoked and information from the CPU is stored in panel memory (Figure 2-12). Panel memory can also be invoked by CP REQ, HALT, or a special IOT.

If the panel memory determines that the panel request has been originated by power turn on, the resident diagnostics will be performed. If the panel request has been originated by the START switch, panel memory will select either the MR78 or the floppy disk drive system to input a new program. If the panel memory causes a halt message to be displayed on the CRT, a probable problem exists within the VT78 terminal.

A panel memory request is acknowledged if the CPU CPREQ line is active low. The panel request is granted irrespective of the run or halt state of the CPU. The CPU is temporarily put in the run state for the duration of the panel routine, and the CPU reverts back to its original state after executing the panel program. CPREQ also bypasses the interrupt enable system. An internal flip-flop (CONTROL FF) is set when CPREQ is acknowledged, preventing additional CPREQs from being granted.

As long as CNTRL FF is set, CPSEL is asserted low for memory reference instead of MEMSEL. CPSEL is used to distinguish between main memory and panel memory.

2.2.1.4 Real Time Clock – The real time clock interrupts the processor at a 100 Hz rate if the interrupt enable flag is set. A Skip instruction causes the program to skip an instruction if the clock flag is set.

Figure 2-13 is a simplified block diagram of the real time clock.

The real time clock uses device code 13_8. The real time clock instructions are listed in Table 2-3. MAR bits 9 through 11 are decoded to determine what operation the real time clock will perform.

INTREQ L is asserted when the clock flag sets, if the clock interrupt enable flip-flop is set. The clock interrupt enable flip-flop is set when DX11 (from the AC) equals a "1" and the 6135 instruction is executed by the program. SKIP L is asserted, causing the program to skip an instruction, if the clock flag flip-flop sets when the 6137 instruction is executed by the program. The clock flag is then cleared by the 6136 instruction.

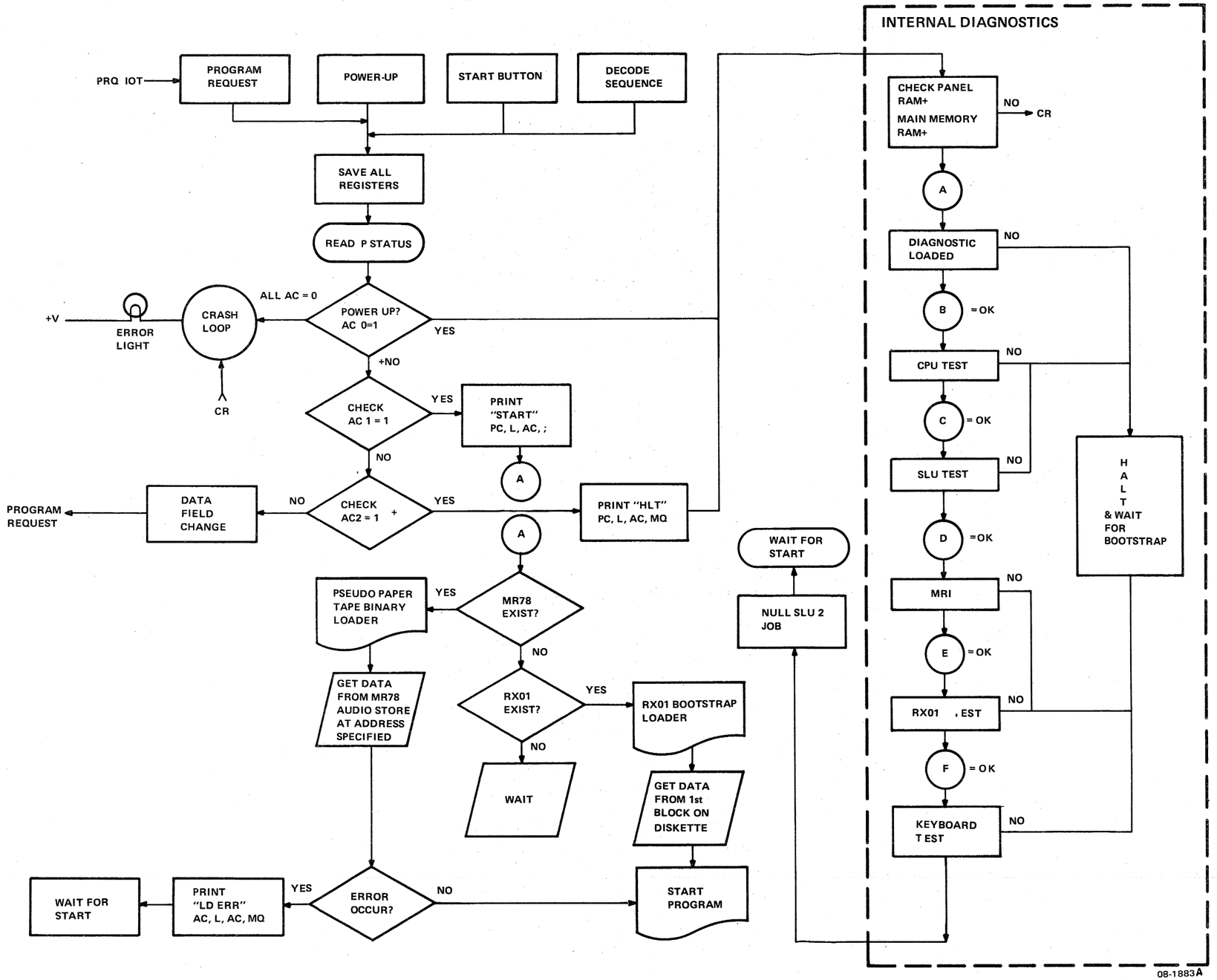


Figure 2-11 Panel Memory Logic Flow Diagram

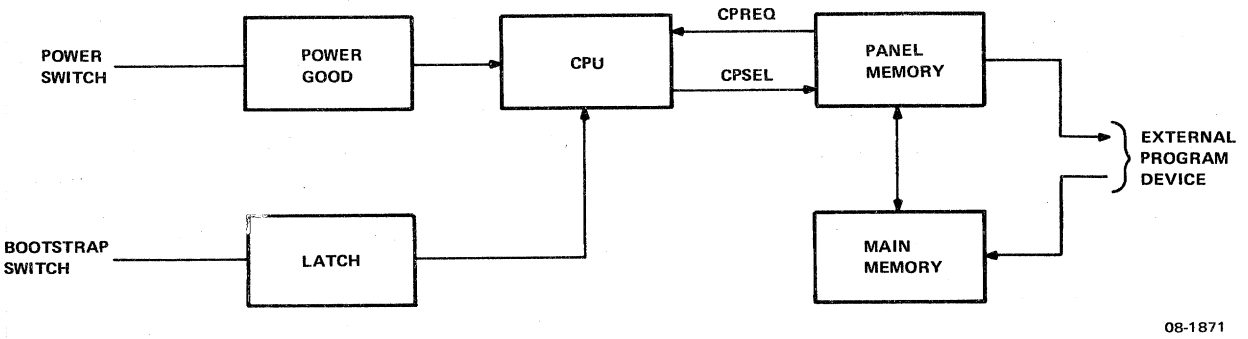


Figure 2-12 Panel Memory Block Diagram

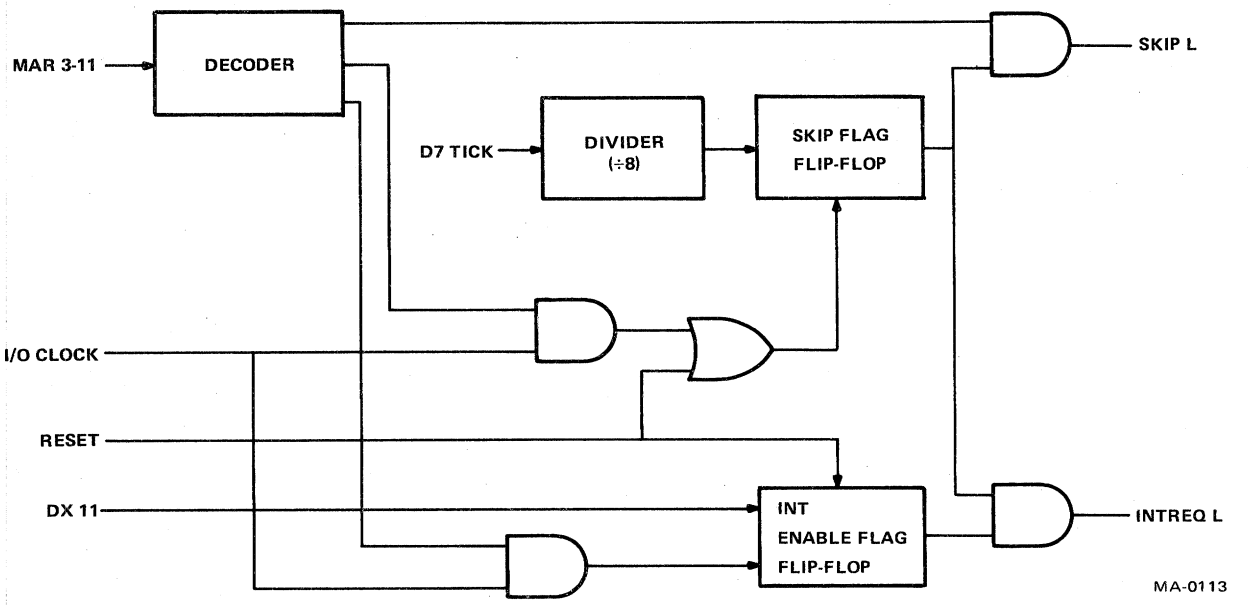


Figure 2-13 Real Time Clock Block Diagram

Table 2-3 Real Time Clock Instructions

Mnemonic	Octal Code	Function
CLIE	6135	Load the interrupt from the AC11: AC11 = 1 (set interrupt enable). AC11 = 0 (clear interrupt enable).
CLCL	6136	Clear clock flag.
CLSK	6137	Skip on clock flag.

2.2.1.5 Floppy Disk Drive Interface – The floppy disk drive interface is used to effect data transfers between the VT78 terminal and up to two dual floppy disk drive systems. Figure 2-14 is a block diagram of the RX78 interface circuits.

The DEVSEL/CON logic decodes instruction bits (3 through 11) to (1) select a floppy disk drive system to transmit or receive data from the VT78 terminal and (2) control all of the functions to be performed. Bit 7 selects the floppy disk drive unit. Drive 0 is selected when bit 7 equals 0. Drive 1 is selected when bit 7 equals 1. Bits 9 through 11 select the function to be performed. The states of these bits and the corresponding functions performed are listed in Table 2-4.

Bit 4 is the maintenance bit which can be used to check the RX78 interface during on-line and off-line conditions. The on-line condition occurs when the cable connecting the VT78 terminal and the RX78 floppy disk drive system is connected. The off-line condition exists when this cable is disconnected.

While the maintenance bit is set (bit 4 equals one), data transfers between the microprocessor and the floppy disk drive system are inhibited. When bit 4 equals zero, the RUN flip-flop may be set producing RUN L or RUN 1 L (depending on the floppy disk drive system selected). The RUN L or RUN 1 L signal initiates communication between the interface and the appropriate disk drive. The RUN flip-flop is clocked in the command transfer mode when LCD is issued or in the data transfer mode to or from the drive when XDR is issued.

The floppy disk drive interface provides two modes of data transfer—a 12-bit mode and an 8-bit mode determined by the state of microprocessor accumulator register bit 5. When bit 5 equals 0, the 12-bit mode is selected. This permits 64 words to be written in a diskette sector; thus two sectors are required to store one page of information. When bit 5 equals 1, the 8-bit mode is selected—permitting 128 8-bit bytes to be written in each sector. This effectively increases the word storage capacity of the diskette by 33 percent.

Figure 2-15 shows the RX78 interface timing sequence.

When data is to be transferred to the floppy disk drive system from the microprocessor, the floppy disk drive system will set the Transfer Request (TR) flag requesting the first data word. The XDR command will load the data word from the microprocessor accumulator into the interface register.

The interface register consists of two 8-bit, edge-triggered universal shift registers used to temporarily store data during transfers between the microprocessor and the floppy disk drive system. Data is parallel loaded into the shift register when LOAD EN is asserted low.

The next XDR IOT will then cause LOAD EN to be asserted high. LOAD EN H is ANDed with EN A H and EN B H to initiate the transfer of the data word (in serial form) from the interface register to the sector buffer in the floppy disk drive system.

Upon receipt of the entire data word, the floppy disk drive system will issue another TR requesting the next data word. The transfer process is then repeated until the sector buffer has been loaded (64 data transfers for 12-bit mode or 128 transfers for 8-bit mode).

After the sector buffer is filled, the floppy disk drive system sets the Done flag indicating that the function has been completed.

SKIP L will be asserted if any of the skip commands [Skip on Transfer Request (STR), Skip on Error (SER), or Skip on Done (SDN)] are decoded by the DEV SEL/CON circuit and the corresponding flag has been asserted.

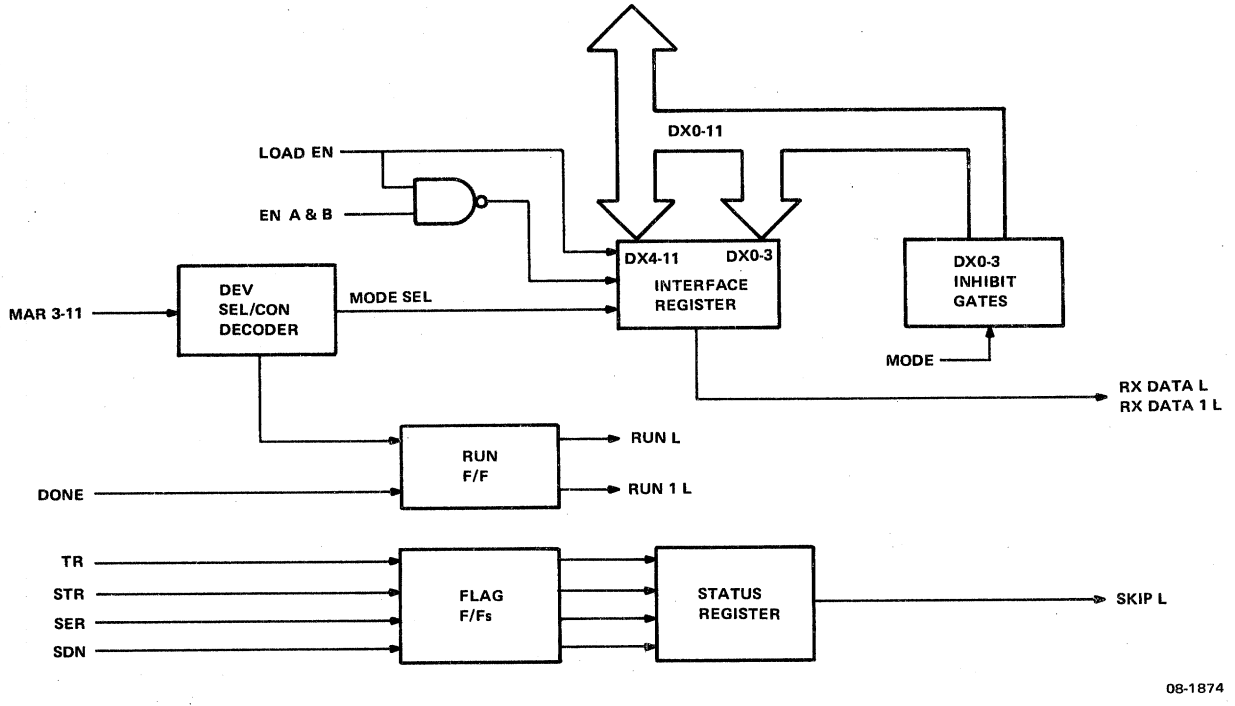


Figure 2-14 Floppy Disk Drive System Interface Block Diagram

Table 2-4 Function Codes for LCD IOTs

Bit Code			Function
8	9	10	
0	0	0	Fill buffer.
0	0	1	Empty buffer.
0	1	0	Write Sector.
0	1	1	Read Sector
1	0	0	Not used.
1	0	1	Read Status.
1	1	0	Write Deleted Data Sector
1	1	1	Read Error Register.

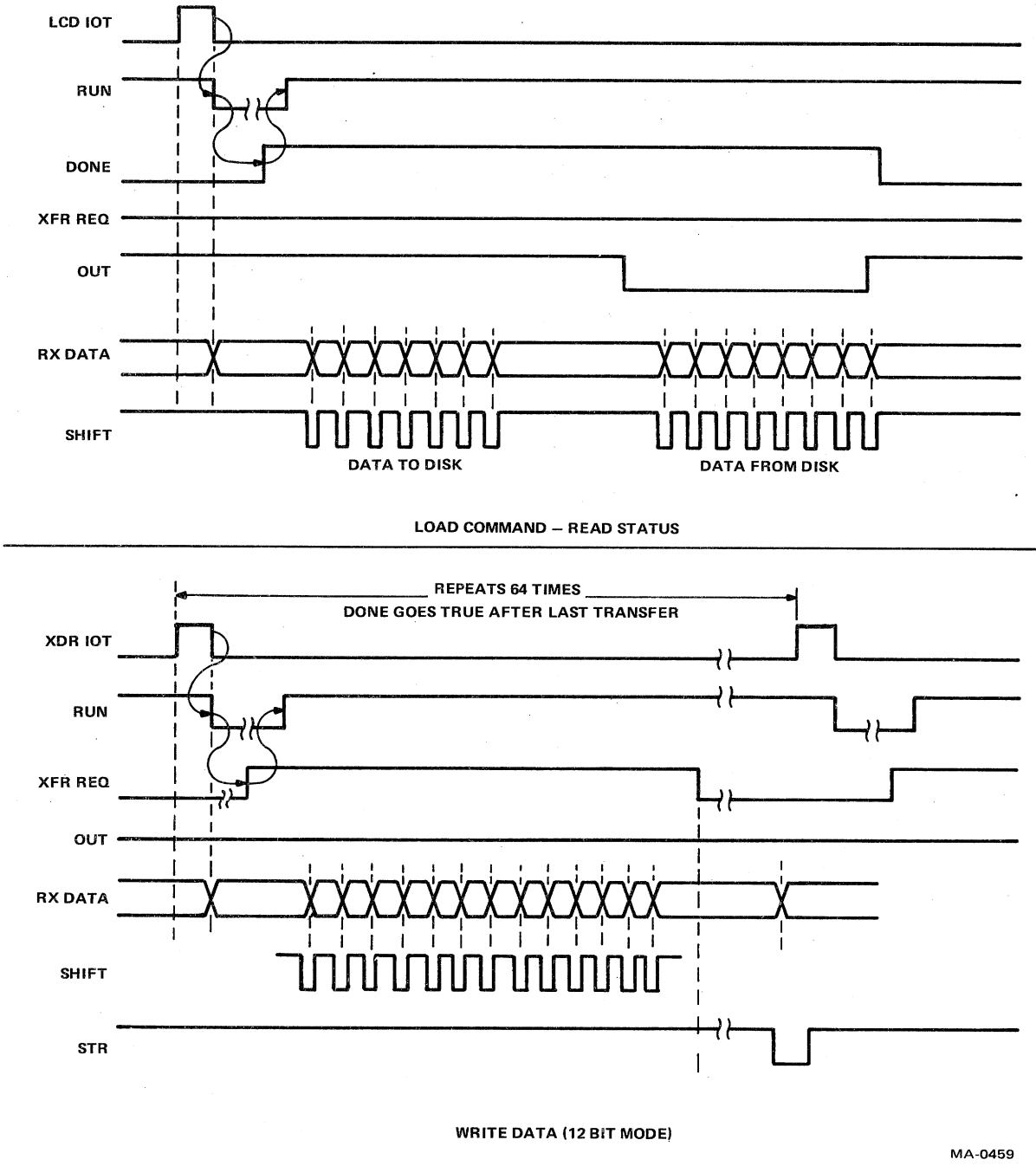


Figure 2-15 Floppy Disk Drive System Interface Timing Diagram

When data is to be transmitted from the floppy disk drive system to the microprocessor, XDR causes LOAD EN, ENA, and ENB to be asserted high—shifting the first word into the interface register. The TR flag is set with the first word in the interface register. This flag denotes that a request for a data transfer from the floppy disk drive system to the microprocessor has been made. After the flag has been tested and cleared, the word will be transferred to the microprocessor accumulator by the next XDR command.

After transferring the next data word into the interface register, the TR flag is set again and the transfer process is repeated until the entire contents of the floppy disk drive system's buffer register has been transferred—emptying the buffer register. The DONE flag is then set indicating the end of the transfer function.

2.2.1.6 MR78 Interface – The MR78 program loader is an optional device which is used to load one of several programs (stored in ROMs) into main memory. A complete functional description of this device is provided in Appendix A.

The MR78 interface consists of four buffer registers and associated gating circuits shown in Figure 2-16.

When program loading is to be implemented, the panel memory handler checks for the existence of the MR78 at the MR78 bootstrap port. If the MR78 device is not installed, the panel handler will check for the existence of a floppy disk drive system as program source. If the MR78 device is installed, CHARACTER RDY L is produced by the MR78 in response to the PI BD L initiation of the program loading sequence. When the fetch new character instruction (6016) is issued, the current character (as it appears at the bootstrap port) is ORed to the accumulator. The MR78 then starts to obtain a new character, clearing the get character flag until the new character is available at the interface.

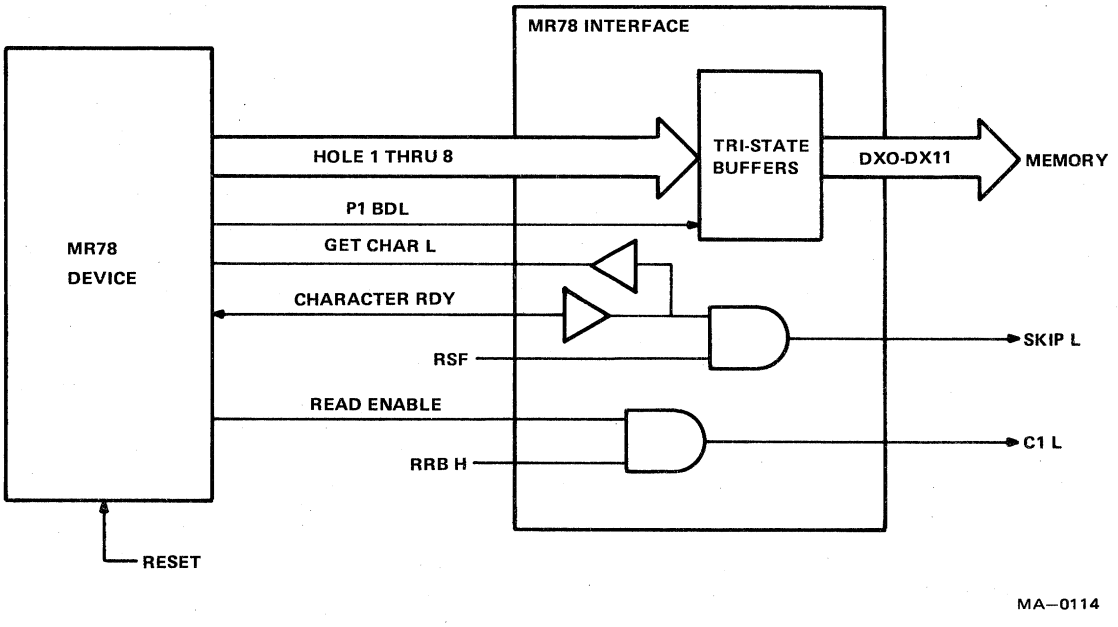


Figure 2-16 MR78 Interface Block Diagram

Three lines at the interface are interrogated by the MR78 program to define the number of programs to be loaded before reading is terminated and the program is started.

NOTE

Although the MR78 bootstrap port was provided specifically for loading MR78 device programs, the port may be used to input 8-bit character data in other than binary format, providing P1 BD L is not present.

2.2.1.7 Serial Line Units – There are three Serial Line Units (SLUs) in the DECstation. Their function is to receive parallel data (characters) from the microprocessor accumulator and shift them out in EIA to a serial device as serial data or to receive EIA data from a serial device, change it to parallel data, and transfer it to the accumulator.

The SLUs consist of a Universal Asynchronous Receiver Transmitter (UART) driven by an oscillator generator package. Figure 2-17 is a simplified block diagram of the SLUs and their associated control circuits.

Timing for each of the SLUs is derived from a 5.066 MHz square wave clock and a network of frequency dividers. The frequency of the clock applied to the UART is the baud rate multiplied by 16. Baud rate selection is accomplished by an IOT instruction which loads 4 bits of the accumulator into the frequency divider as shown in Table 2-5. Each SLU has its own baud rate generator, consequently each baud rate can be programmed independently.

The decoded memory address register bits 3 through 8 select the SLU to effect the transfer of data between the microprocessor accumulator and the external device. Two device codes are used—one for transmitting data and the other for receiving data as listed in Table 2-6. Memory address register bits 9 through 11 determine the function to be performed by the selected SLU. The microprocessor is interrupted by an INT REQ L, if the interrupt enable flag is set and the transmit or receive flag sets. Skip is asserted if the transmit or receive flag is set while flags are being checked by the program.

Since all of the SLUs are similar only one, SLU 2, will be described in detail.

When the UART is in the transmit mode of operation, it changes 8-bit parallel data from the microprocessor accumulator to serial data for transmission to a serial device. Figure 2-18 shows the transmit function timing sequence.

The number of bits per character, stop bits, parity, and error detection is selected by KMD1 IOT. Note that SLU 2 is the only line having this capability. SLU 1 and 3 are fixed at 8 data bits, 1 stop bit, and no parity. When the transmit operation begins, a strobe (TBRL) is generated by ROM D and ROM E at DEV SEL time. ROM D decodes the device selected and ROM E decodes the function desired. Strobe TBRL loads the data from the microprocessor accumulator into the UART transmitter buffer (Figure 2-19) and sets the UART internal transmit flag. The UART will now transfer the data from the buffer to the transmit register and begin shifting data to the serial device.

The first bit transmitted is the start bit followed by bits 11 through 4 and the stop bit (assuming that UART is transmitting in the 8-bit mode). Approximately three clock pulses after the transfer of data from the transmit buffer register to the transmit register, the Transmit Register Empty (TRE) flag is set and another character can be loaded into the transmit register.

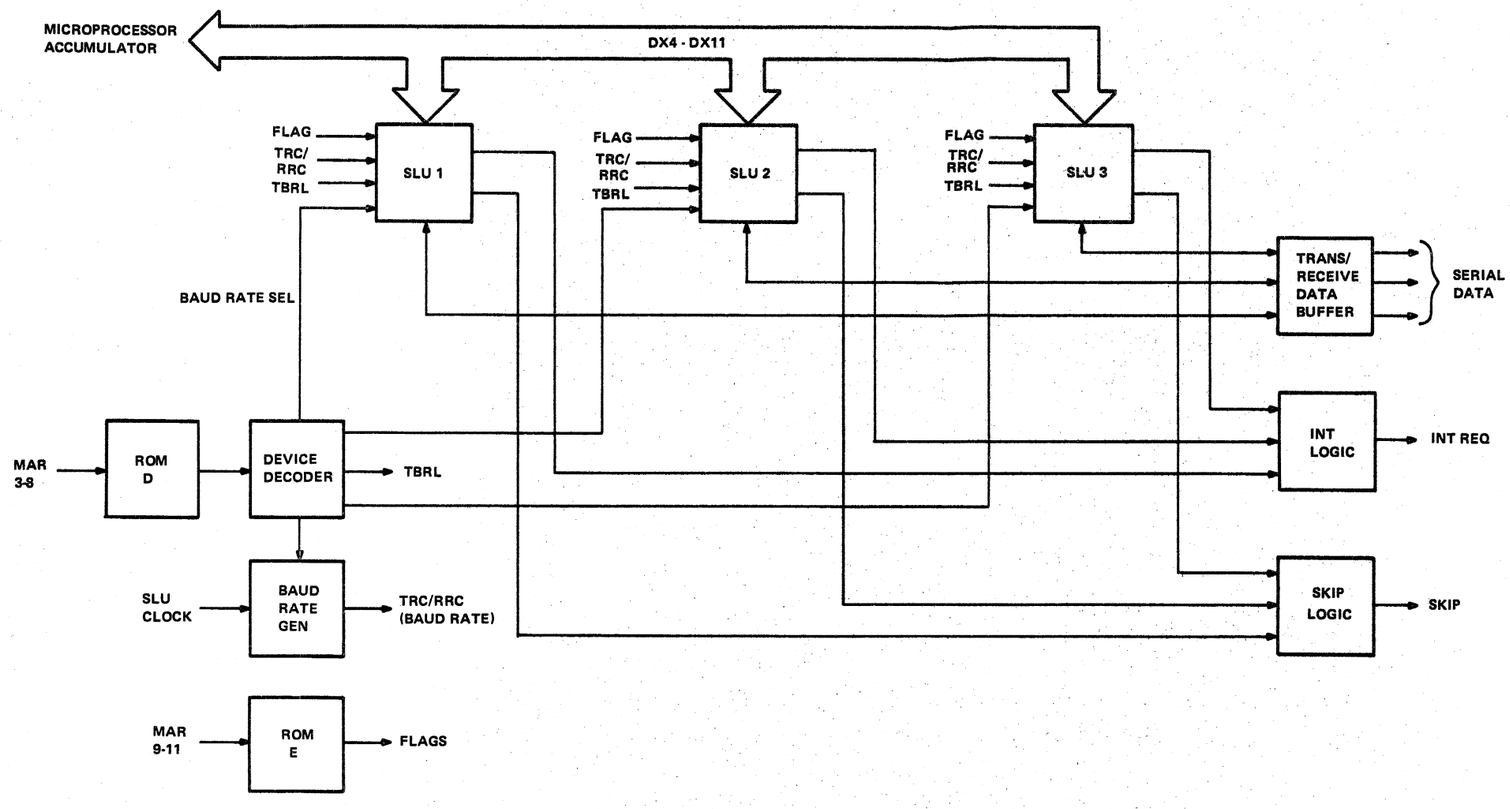


Figure 2-17 SLU and Control Circuits Block Diagram

Table 2-5 Baud Rate Selection (SLU 2 and SLU 3)

Control Bits				Baud Rate	Clock Div	Freq to UART
8	9	10	11			
0	0	0	0	50	6336	799.56 Hz
0	0	0	1	75	4224	1199.34 Hz
0	0	1	0	110	2880	1759.03 Hz
0	0	1	1	134.5	2355	2151.17 Hz
0	1	0	0	150	2112	2398.67 Hz
0	1	0	1	300	1056	4797.35 Hz
0	1	1	0	600	528	9594.70 Hz
0	1	1	1	1200	264	19.1894 kHz
1	0	0	0	1800	176	28.7841 kHz
1	0	0	1	2000	158	82.0633 kHz
1	0	1	0	2400	132	38.3788 kHz
1	0	1	1	3600	88	57.5682 kHz
1	1	0	0	4800	66	76.7576 kHz
1	1	0	1	7200	44	115.1364 kHz
1	1	1	0	9600	33	153.5152 kHz
1	1	1	0	19200	16	316.6250 kHz

Table 2-6 SLU Device Codes

SLU	Receive	Transmit
1	03	04
2	30	31
3	32	33

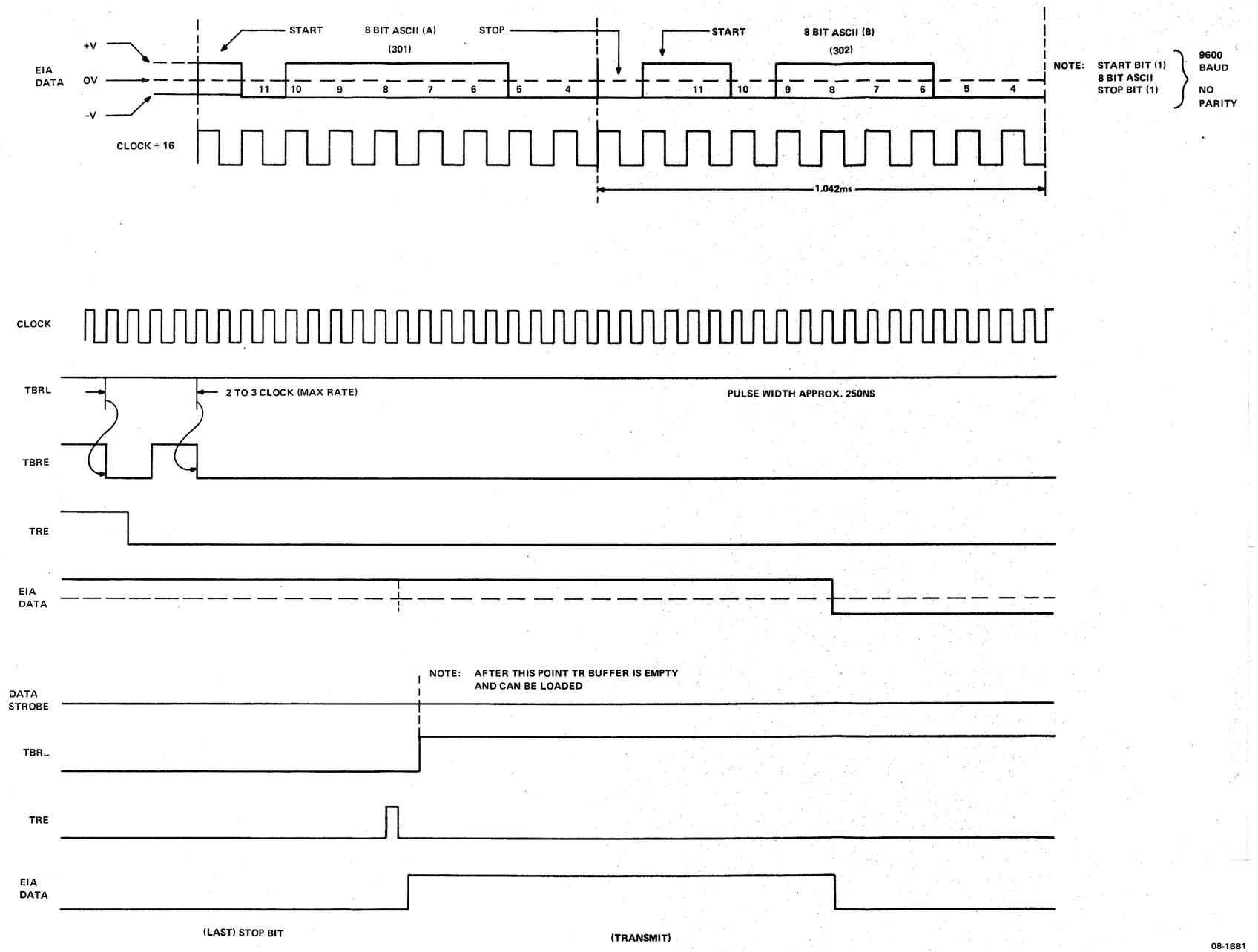


Figure 2-18 UART Transmit Function Timing Diagram

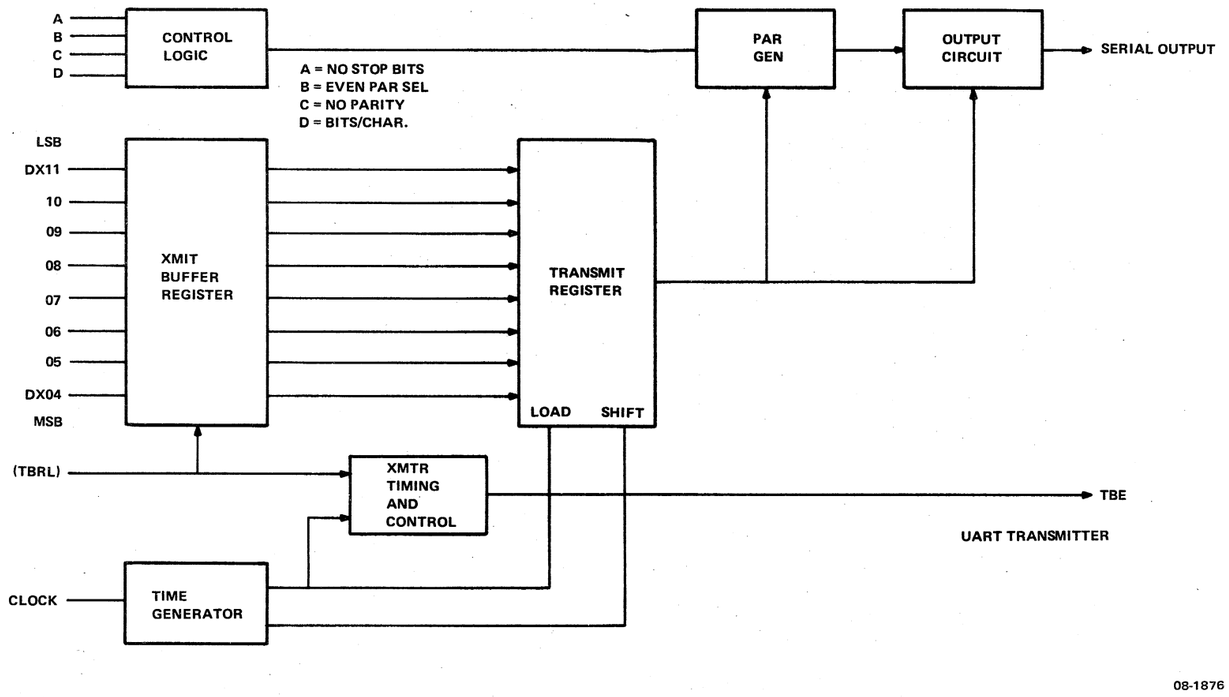


Figure 2-19 UART Transmit Circuits Block Diagram

The receive portion of the UART receives serial data from an external device and changes it to a character to be transmitted, in parallel, to the microprocessor accumulator. This is performed during the next KRB IOT (load receiver command). Figure 2-20 shows the receiver function timing sequence.

Transfer occurs when data, assembled in the receiver shift register (Figure 2-21), is transferred to the holding register. At this time Data Received (DR) is asserted, the receive flag is set, and data is transferred to the microprocessor accumulator. The receive flag is cleared when the content of the holding register is transferred to the accumulator. This can only be done through the clear flag IOTs. If not cleared, receipt of the next character will cause an overrun error.

Table 2-7 contains all of the SLU signals and includes a brief functional description of each.

2.2.1.8 Parallel I/O – The parallel I/O interface is used to connect the LA78 or LQP78 printer to the VT78 terminal. However, any parallel I/O device (using 12-bit data and meeting the I/O interface specifications) can communicate with the VT78 terminal via the parallel I/O interface.

Figure 2-22 is a simplified block diagram of the parallel I/O interface.

The memory address register determines the device to be used in conjunction with the parallel I/O interface and the function to be performed. Device selection (LQP78 or LA78) is accomplished by decoding memory address bits 3 through 8 and the LA/LQP signal using the DVCD SEL register. The function to be performed is determined by decoding memory address bits 9 through 11 using ROM A and ROM B.

The PAPER RDY, CHARACTER RDY, CARRIAGE RDY, and PTR RDY signals show the status of the printer. The use of these signals depends upon the device associated with the parallel I/O interface. When the printer is ready to accept and print data, these signals will set corresponding flip-flops which may be tested by an IOT causing a skip. The status register can be read by an IOT to determine the status of the printer.

Parallel data is transferred using a bi-directional tri-state data bus. Normally IN/OUT is maintained high and the parallel I/O interface will only provide output data. When IN/OUT is asserted low, the output register is disabled and the interface can receive data, if available. An input device must assert the IN/OUT signal low for at least 50 ns prior to asserting new data on the lines and must keep it low until 50 ns after the data has been removed.

NOTE
Parallel I/O signals can not be driven more than 25 ft (approximately 8 meters).

Table 2-8 is a list of the primary control signals used with the parallel I/O interface and includes a brief functional description of each.

2.2.2 Keyboard/Video Display

2.2.2.1 Data Paths, Memory, and Decoder Circuits – The RAM and memory buffer, the character generator, the video shift register, the instruction decoders, and the memory select and program test registers are located on the data paths, memory, and decoder module. Each of these logic groups will be discussed separately.

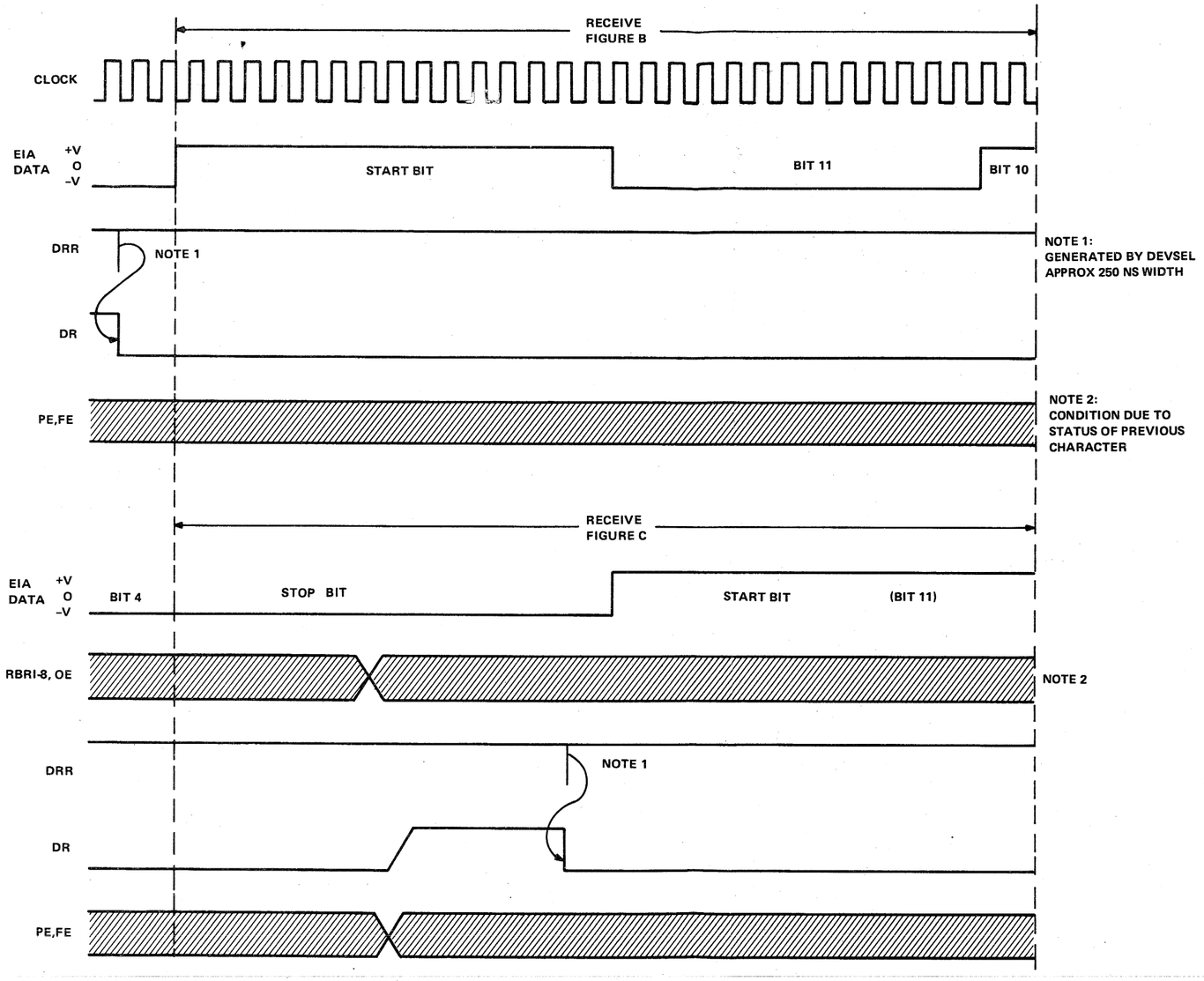


Figure 2-20 UART Receiver Timing Diagram

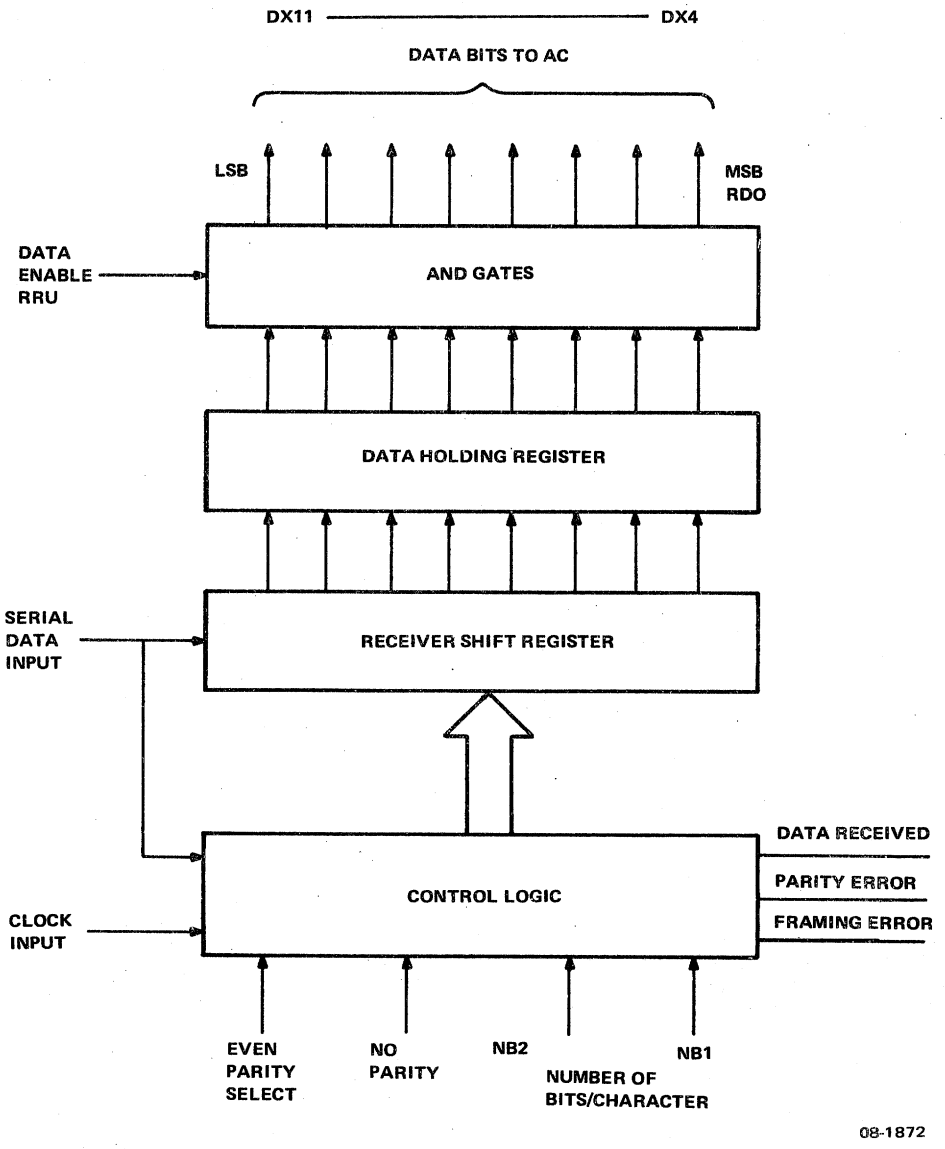


Figure 2-21 UART Receiver Circuits Block Diagram

Table 2-7 SLU Signal Functions

Pin	Mnemonic	Description	Function
4	RRD	Receiver Register Disable	A high on Receiver Register Disable forces the Receiver Holding Register outputs to a high impedance state.
12	RBR1-RBR8	Received Data	The contents of the receiver buffer appear on these tri-state outputs. Words less than eight characters are right justified to RBR1 and the unused bits are zero.
13	PE	Parity Error	A high level indicates received parity does not match parity programmed by control bits. If parity is inhibited, this output is low (SLU 2 only).
14	FE	Framing Error	A high level indicates the first stop bit was invalid (SLU 2 only).
15	OE	Overrun Error	A high level indicates data received flag was not cleared before the last character was transferred to the receiver buffer register (SLU 2 only).
16	SFD	Status Disable	Never disabled (always ground).
17	RRC	Receiver Clock	16 times the baud rate.
18	DRR	Data Received Reset	A low level clears the Data Received DR output to a low level.
19	DR	Data Received	A high level indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Receiver Register Input	Serial data is clocked into the Receiver Register.
21	MR	Master Reset	A high level clears PE, FE, OE, and DR to low levels and sets the transmitter output to a high level.
22	TBRE	Transmitter Register Empty	A high level indicates the buffer has transferred its data to the transmit register and is ready to receive new data.

Table 2-7 SLU Signal Functions (Cont)

Pin	Mnemonic	Description	Function
23	TBRL	Transmitter Buffer Load	A low level transfers data from TBR1 through TBR8 input into the buffer register. A low to high transition transfers the data to the transmit register. If the transmit register is busy, transfer is delayed until the character can be loaded.
24	TRE	Transmitter Register Empty	Not used.
25	TRO	Transmit Output	Character data, start bit, and stop bits are outputted serially.
26 33	TBR1- TBR8	Buffer Register Inputs	Input character data is loaded (in parallel) to the buffer register.
34	CRL	Control Bit Load	A high level loads the control register (SLU 2 only).
35	PI	Parity Inhibit	A high level inhibits parity generation, parity checking, and forces PE output low.
36	SBS	Stop Bit Select	A high level selects 1.5 stop bits for 56 characters and 2 stop bits for all others. A low selects 1.0 stop bits.
37, 38	CLS 2 CLS 1	Character Length Select	These inputs select the character length (SLU 2 only).
39	EPE	Even Parity Enable	When PI is low, a high level generates and clocks even parity. A low level selects 1.0 stop bits (SLU 2 only).
40	TRC	Transmitter Clock	Transmitter clock (16 times baud rate).

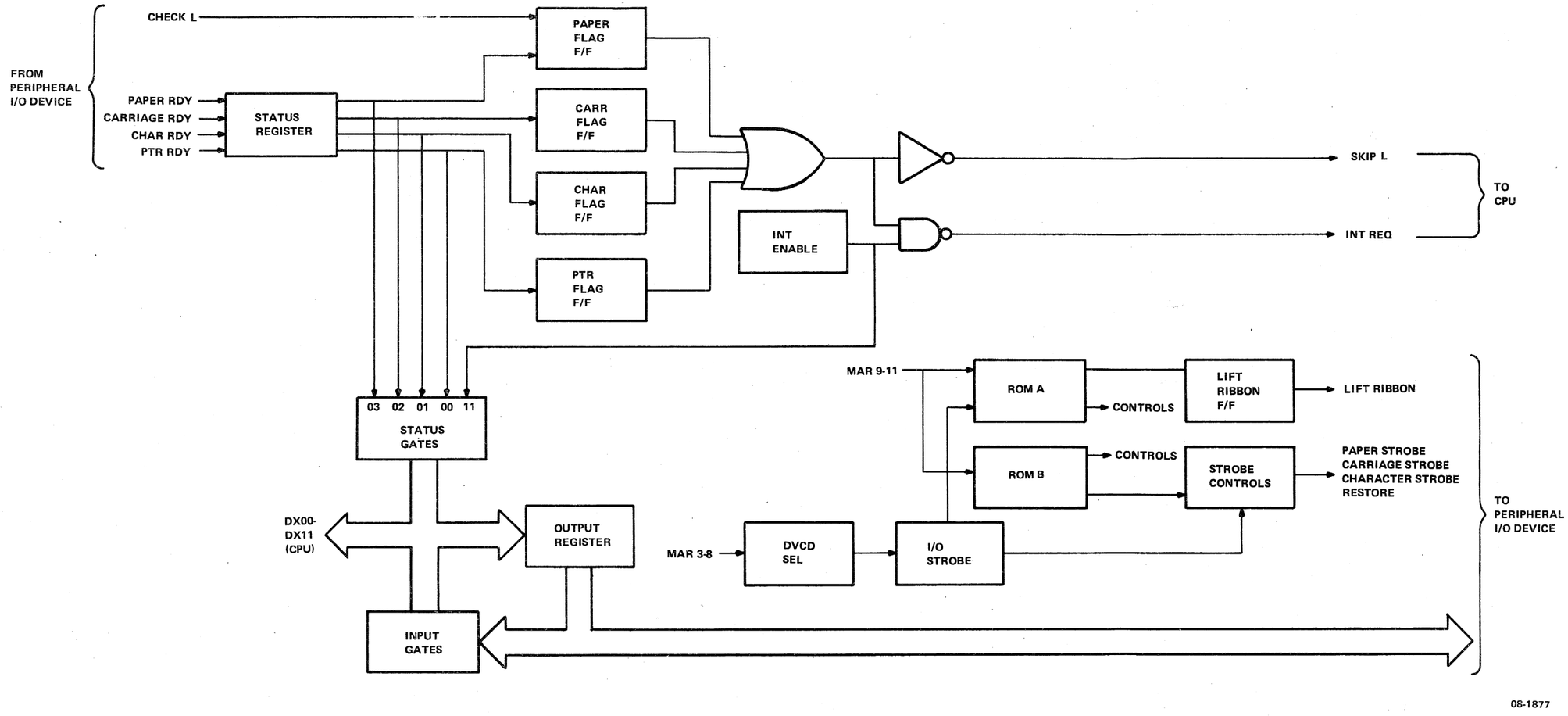


Figure 2-22 Parallel I/O Interface Block Diagram

Table 2-8 Parallel I/O Interface Signal Functions

Signal	Function
Character Strobe	This pulse causes the print wheel in the LQP78 to position the selected character in front of the print hammer. When motion stops, the hammer strikes. In the LA78 this pulse causes data to be loaded into the printer memory. Upon completion of a line of data, the entire line will be printed. For any user application the strobe is generated by the print character command (6504) or the load printer buffer command (6664).
Carriage Strobe	This pulse is used by the LQP. The carriage strobe occurs when the LQMC (6503) IOT is performed and causes the carriage to move in a selected direction and distance, using the value of the data received from the data bus. Each data bit causes the carriage to move 120th of an inch. AC bit 0 determines the direction of motion—right (0) or left (1).
Paper Strobe	This pulse is used with the the LQP and occurs when the LQMP (6502) IOT is performed. The signal causes the paper to move in the direction and distance specified by the data received. Each data bit causes the paper to move 1/48th of an inch per binary bit. Bit 0 determines the direction of motion—a high causes the paper to advance and a low causes the paper to reverse.
Restore Strobe	This pulse is used with the LQP and occurs when the LQRE (6507) IOT is performed. It causes the printer to abort all operations in progress, clear error conditions, and move the carriage to the extreme left position.
LA/LQP	This signal determines which device code IOT will be performed. If the LA78 printer device code (66) is required, the line should be grounded. The user must select the device code. This is accomplished by using the correct cable to connect the LA78 or LQP78.
Data Lines	These signals receive and transmit binary coded information which represents various operations for each command. The data must be asserted true for at least 200 ns prior to the strobe pulse.
Check Line	This input from the LQP indicates an error has occurred as a result of a malfunction or an illegal command. All activity will stop and all inputs and outputs will be disabled except the restore strobe. The restore IOT or a recycle of power is the only way to clear a check condition. This signal is not used with the LA78 printer.
Character Ready	This input indicates that either printer is ready to begin a print cycle. This signal is false while the printer is printing a character or loading a character into memory.
Carriage Ready	This input indicates the LQP is ready to accept a carriage motion command. The line is high (false) while the carriage is in motion. It is not used with the LA78 printer.

Table 2-8 Parallel I/O Interface Signal Functions (Cont)

Signal	Function
Paper Ready	This input indicates the LQP is selected properly and is supplied with power and no internal malfunctions exist.
In/Out	This signal line is normally high. In this mode the interface will only provide output data. If this line is asserted low, the output buffer is disabled and the interface can receive any input data, if available. This line must be asserted low for at least 50 ns prior to receipt of externally supplied data and maintained low until 50 ns after data has been removed.
Printer Select	This signal is only used by the LQP to enable the printer to respond to any input commands. This line enables all printer input and output lines using a grounded line from the interface.

The RAM consists of fourteen 2102 chips arranged to provide two 1024x7 read/write memories. To the programmer, the memory appears as a 2048x7 bit memory, because the RAM addressing scheme assigns all even addresses to one 1024 memory (page 1) and all odd addresses to the other memory (page 2). 1,920 locations are used to store a screenful of characters (24 lines x 80 columns); the remaining 128 locations are used by the microprogram as a scratchpad memory; i.e., temporary storage of keyboard characters, cursor address, etc.

The memory buffer contains the contents of the RAM location selected by the current contents of the X and Y registers. Twice during each instruction time, the selected RAM output is strobed into the memory buffer for transfer to the video circuits during display time, the UART for transmission to the processor, or the X, Y, AC, or B registers because of a command test condition. Data written into the RAM can be from the AC register, the B register, the ROM, or the UART. These inputs are multiplexed into the RAM by signals MUX A and MUX B. The TRUE/FALSE condition of MUX A and MUX B is the result of decoded microprogram transfer commands.

Figure 2-23 illustrates how address mapping is accomplished. The memory is arranged in a 16x64 configuration with Y3, Y2, Y1, and Y0 selecting one of 16 rows and X5, X4, X3, X2, X1, and X0 selecting one of 64 columns. Whenever the X register is greater than 64 or the Y register is greater than 12, the two most significant Y address lines are forced high and the two most significant X address lines are replaced by Y3 and Y2. This effectively divides the RAM into five sections: one 12x64 section and four 4x16 sections. Memory references for characters displayed in columns 0 through 63 will be made to the 12x64 section; memory references for characters displayed in columns 64 through 79 will be made to one of three 4x16 sections. The contents of the Y register will determine which one of the three 4x16 sections will be referenced.

The remaining 4x16 section is used as a scratchpad memory by the microprogram. This section is addressed whenever the Y register contains a number greater than 11. The address mapping circuits replace the two most significant bits of the X register selection bits with Y3 and Y2. Since Y3 and Y2 will both contain Ones when a number greater than 11 is in the Y register, they will select the highest 4x16 memory section. X3, A2, X1, and X0 will select one of the 16 locations in this section.

The Video Shift Register (VSR) is a 7-bit shift register that holds one line of the seven-line character currently being displayed on the CRT screen. During each video scan, the video shift register is loaded from the character generator 80 times, once for each character position. After loading, the contents of the VSR are shifted by B OSC A (the basic timing clock) through the video amplifier to the cathode of

the CRT where they modulate the electron beam. Zeros shifted out of the VSR will cause a +2 V signal on the cathode and light on the screen. Ones will cause a +40 V signal on the cathode, cutting off the CRT and producing a dark screen.

Figure 2-24 illustrates the data path of the character from the RAM to the CRT cathode and the display timing. T2H, a timing pulse that occurs once every timing cycle, simultaneously loads the VSR with one line of the character to be displayed and loads the memory buffer with the character that will be displayed in the following screen location.

Every operation performed by the display is the result of an instruction stored in the 1024x8 bit ROM. The 8-bit ROM word is decoded by the decoder logic to produce an instruction. This instruction will cause some action to take place in the terminal. The bits of the ROM word are labeled A through H.

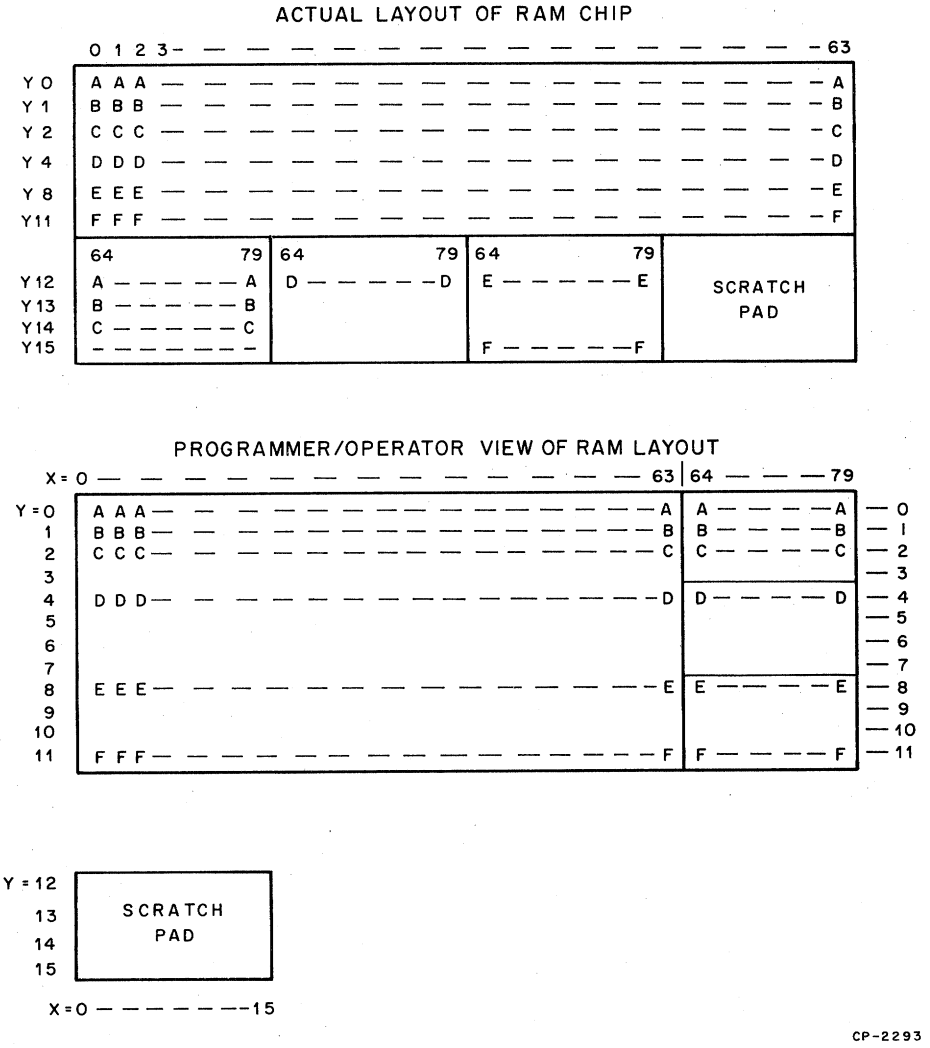


Figure 2-23 RAM Address Mapping

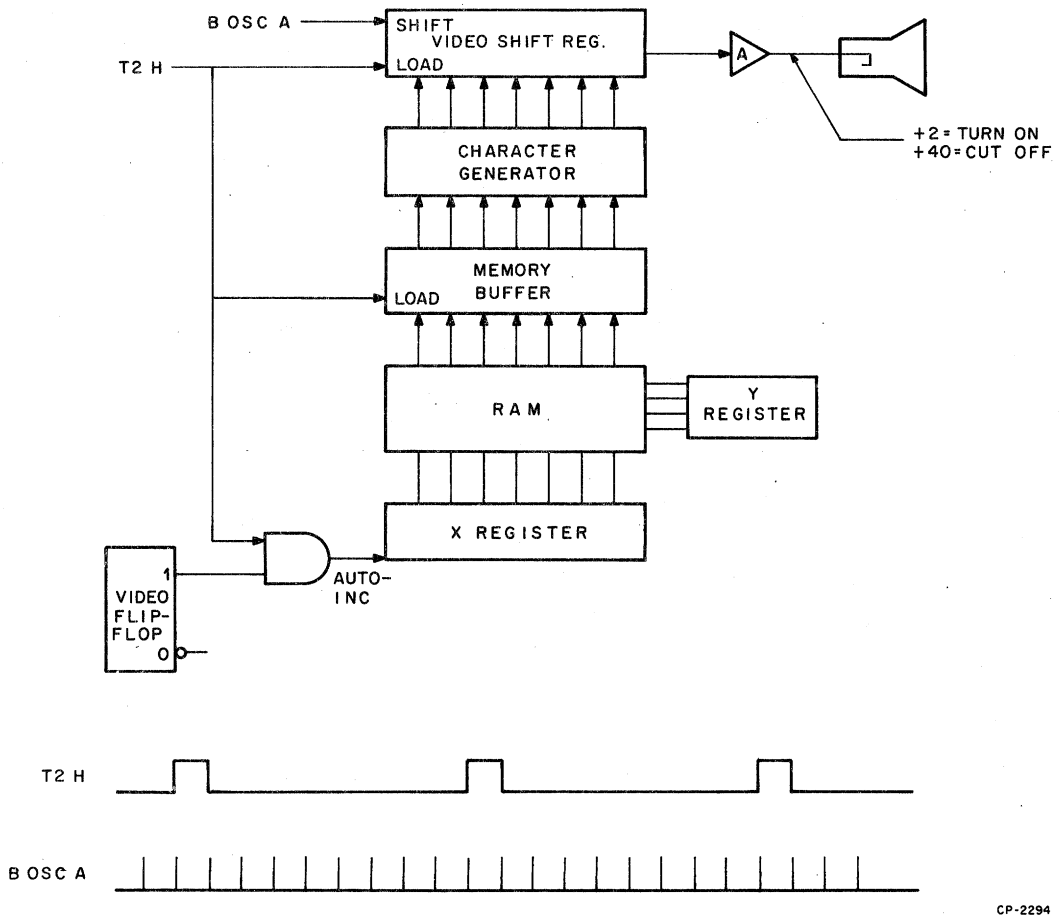


Figure 2-24 Character Display Timing

As Figure 2-25 shows, the ROM word is divided into three groups: A, BCD, and EFGH. If Bit A equals 0, bits B, C, and D are decoded into one of eight instruction groups. Bits E, F, G, and H are sampled to determine what action is to be taken. An action occurs if one or more of the bits are set to 1. For example, if bit E is a 1, a certain action will occur; if both bits E and F are set to 1, two actions will occur but not at the same time. If E, F, G, and H are all set to 0, a different action takes place depending on the state of B, C and D. Table 2-9 is a list of commands that are available when ROM bit A is set to 0. If bit A of the ROM word is set to 1, a load RAM from ROM command will be decoded. When operating in mode 1, the command is conditional. The seven least significant bits of the ROM word (BCDEFGHA) are loaded to the RAM location specified by the contents of the X and Y registers. When operating in mode 0, the load command is conditional. In operation, the command increments the AC register and then compares the AC to the selected RAM location. If AC is less than RAM, the load command is not performed; i.e., the contents of the selected RAM location remains unchanged. If AC is greater than RAM, BCDEFGH is loaded into the RAM and the DONE flip-flop is set. All instructions listed in Table 2-10 are decoded at specific times in the instruction cycle. Six time states (9TE, TF, TW, TG, TH, and TJ) are produced during each instruction cycle (Figure 2-26). These signals are gated with ROM bits EFGH to enable the desired action. Table 2-10 lists the timing states and the instructions performed at each state in the instruction cycle.

The character generator consists of a 1024x8 bit ROM and associated address gating. The display code for all characters displayed on the screen is stored in the ROM.

During display scans, characters fetched from the RAM are loaded into the memory buffer in ASCII format. Because the address selection lines of the character generator are wired directly to the memory buffer, the character generator never needs to be loaded. It is always selecting the ROM location addressed by the ASCII code in the memory buffer. For example, if the memory buffer contains the ASCII coded for "A," the character generator address lines will select the ROM location containing the 7X7 display code for the letter "A." However, since the character display method used by the display requires that only one line of the 7X7 character be displayed during a single horizontal scan, three more address lines are provided to select one of the seven lines of the matrix: the three least significant bits of the AC register. In operation, ASCII characters are loaded into the memory buffer; the character generator uses this code as an address to select the ROM location containing the display code for the desired character. AC bits 0, 1, and 2 are decoded to select one of the seven lines of the character matrix for output to the video shift register.

Character generator outputs CD0 through 6 are loaded into the Video Shift Register during the T2 time of every clock cycle. CD6 will be the first bit shifted out of the VSR; CD0 will be the last.

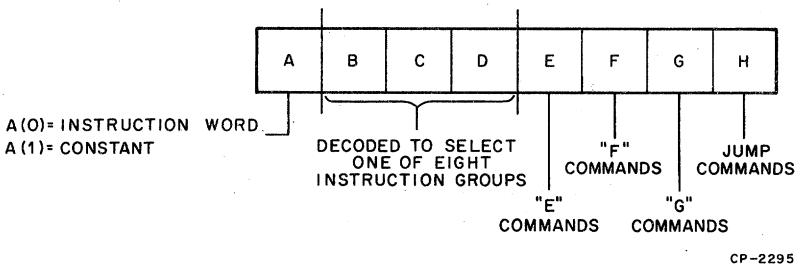


Figure 2-25 ROM Word Division

Table 2-9 Command List

ABCD	E	F	G	H	Display Instruction	Mnemonic
0000	0	0	0	0	Set cursor flip flop.	SCFF
	1	X	X	X	Clear the X and Y registers.	ZXZY
	X	1	X	X	Decrement the X and Y registers.	DXDY
	X	X	1	X	Load AC from memory.	M2A

Table 2-9 Command List (Cont)

ABCD	E	F	G	H	Display Instruction	Mnemonic
	X	X	X	1	Mode 0: Printer scan flag set?	PSCJ
					Mode 1: Jump if UART has received a character.	URJ
0001	0	0	0	0	Set video flip flop.	SV1D
	1	X	X	X	Complement bit X3 (8s-bit) of X register.	X8
	X	1	X	X	Increment AC register.	1A
	X	X	1	X	Load RAM from AC.	A2M
	X	X	X	1	Mode 0: Jump if AC0, 1, 2 = 7_8.	TABJ
					Mode 1: Jump if AC = RAM.	AEMJ
0010	0	0	0	0	Load Y Register from Y buffer.	B2Y
	1	X	X	X	Increment X; decrement Y.	IXDY
	X	1	X	X	Increment AC register.	IA1
	X	X	1	X	Load UART from RAM.	M2U
	X	X	X	1	Mode 0: Jump if key click.	KCLJ
					Mode 1: Jump if AC<RAM.	ALMJ
0011	0	0	0	0	Complement bell flip-flop.	CBFF
	1	X	X	X	Increment X register.	IX

Table 2-9 Command List (Cont)

ABCD	E	F	G	H	Display Instruction	Mnemonic
	X	1	X	X	Increment Y register.	IY
	X	X	1	X	Load RAM from B register.	B2M
	X	X	X	1	Mode 0: Jump if 60 Hz line frequency.	FRQJ
					Mode 1: Jump if AC = X register.	ADXJ
0100	0	0	0	0	Clear cursor and video ff.	ZCAV
	1	X	X	X	Clear AC register.	ZA
	X	1	X	X	Decrement Y register.	DY
	X	X	1	X	Load X register from RAM.	M2X
	X	X	X	1	Mode 0: Printer request flag set?	PRQJ
					Mode 1: Jump if AC = RAM.	AEM2J
0101	0	0	0	0	Load print shift register.	LPB
	1	X	X	X	Enter mode 1.	M1
	X	1	X	X	Increment ROM bank.	IROM
	X	X	1	X	Load RAM from UART.	U2M
	X	X	X	1	Mode 0:	TRUJ
					Mode 1:	

Table 2-9 Command List (Cont)

ABCD	E	F	G	H	Display Instruction	Mnemonic
0110	0	0	0	0	Start printer.	EPR
	1	X	X	X	Clear X register.	ZX
	X	1	X	X	Decrement X register.	DX
	X	X	1	X	Load Y buffer from RAM.	M2B
	X	X	X	1	Mode 0: Jump if UART is transmitting.	UTJ
					Mode 1: Jump if video scan flag.	VSCJ
0111	0	0	0	0	Halt printer and clear Y register.	HPRIZY
	1	X	X	X	Enter Mode 0.	M0
	X	1	X	X	Decrement AC register.	DA
	X	X	1	X	Spare.	
	X	X	X	1	Mode 0: Jump if not top of screen.	TOSJ
					Mode 1: Jump if key not typed.	KEYJ

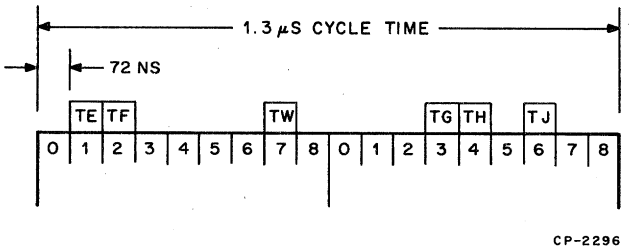


Figure 2-26 Cycle Timing Diagram

Table 2-10 Instruction Time States

Time State	Decoded Instruction	ROM Enabling Signals
TE	ZXZY, X8, IXDY, IX, ZA, M1, 2Z, M0	A.E.
TF	DXDY, IA, IA1, IY, DY, IROM, DX, DA	A.F
TW	SCFF, SVID, B2Y, CBFF, ZCAV, LPB, EPR, HPR, ZY	A.E.F.G.H
TG	CLEAR WRITE FLIP FLOP	
TH	M2A, A2M, M2U, B2M, M2X, U2M, M2B	A.G
TJ	JUMP, NO-OP	A.H

2.2.2.2 ROM, UART, and Timing Circuit – The ROM is a 1024x8 bit read-only memory that stores the display microprogram. It consists of eight 256x4 chips organized as illustrated in Figure 2-27 to provide four pages of 256x8 bit memory. The outputs A through H reflect the contents of the location addressed by the Program Counter (PC). The eight least significant bits of the PC will address one 8-bit ROM word from page 1, 2, 3, or 4. Page selection is determined by the condition of PC bits 8 and 9. The PC is normally counted at the TH time of every instruction cycle to fetch a new command or address from the next sequential ROM address.

Commands that affect the PC and the ROM are JUMP and IROM. A program jump is accomplished by loading a new address into the PC. The new address is always the contents of location JUMP +1. At the TH time of the JUMP command, the PC is counted and the ROM output word will contain the new address (JUMP +1). If the jump conditions have been met, FLAG L will be TRUE and PC COUNT will load the new address into the PC. Program skips are the result of not meeting JUMP conditions; there is no skip command. If JUMP conditions are not met, FLAG L will be false and the PC will not receive the new address. Instead, PC COUNT will increment the PC a second time, fetching the next command from location JUMP +2.

The JUMP command allows jumping within the selected page. To jump to a different page, the program must perform one or more IROM commands followed by a JUMP command. The IROM command increments the page counter. When a JUMP command is executed, the new page address is loaded into PC9 and PC8. At the same time, the contents of ROM location JUMP +1 are loaded into PC7 through PC0 to select one of the 256 locations in the new page.

All operations are synchronized by the basic timing clock and timing chain (Figure 2-28). The clock is a crystal-controlled oscillator operating at 13.824 MHz. Clock output B OSC A provides the basic clock frequency for the timing shift register and frequency dividers. It is also used to perform shift operations in the video shift register. The output of the crystal clock becomes the input clock of an 8-bit shift register. The outputs of the shift register are ANDed together to provide an input data signal to the register. When all bits in the register are set to 1, the input data signal will be a "1." The result is that the register acts like a 9-bit ring counter with a "0" being shifted through all of the bit positions.

The output from this register when ANDed with the time state enable signal produces the six time state signals required for instruction decoding. The tim state enable signal is the output of the first stage of a 4-bit divide-by-10 counter that follows the shift register in the timing chain. The input clock to this counter is wired to the last stage (bit 7) of the shift register. This means that the time state enable flip-flop is toggled once for each complete cycle of the shift register. It also means that it takes two complete cycles of the shift register to produce the six time state signals.

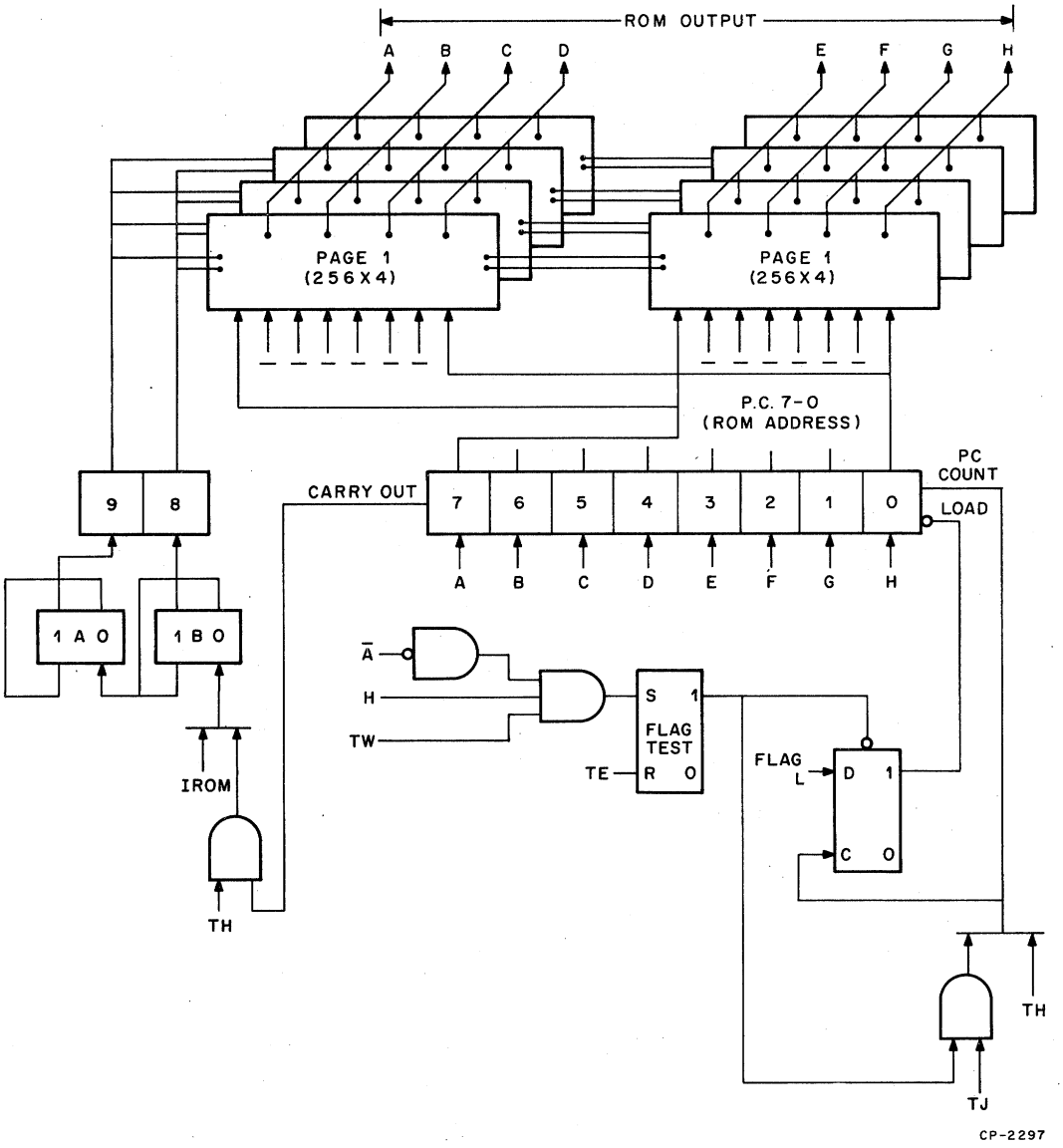


Figure 2-27 Display ROM Organization and Selection

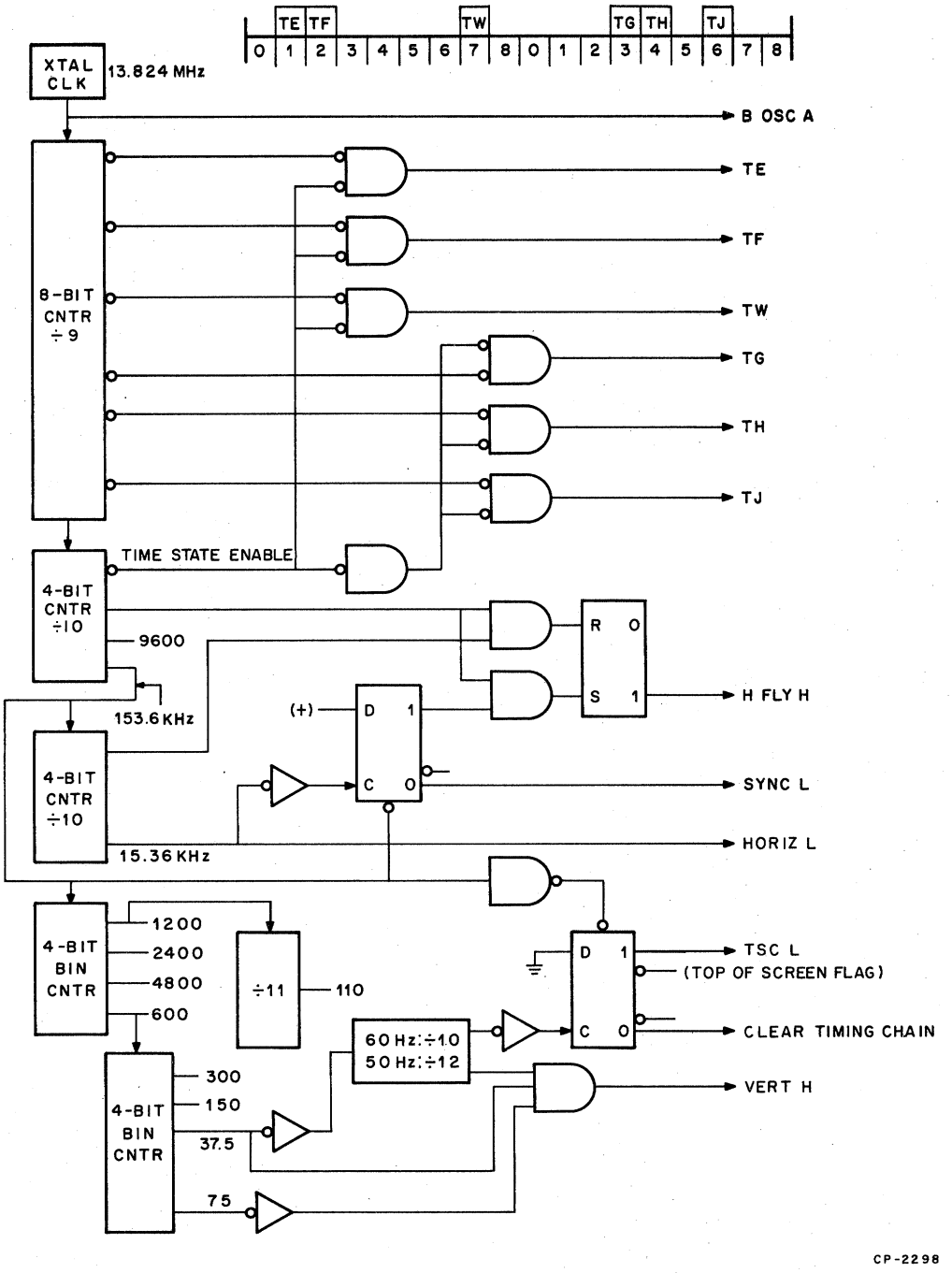


Figure 2-28 Display Basic Timing Circuits

The input clock frequency applied to the 4-bit decade counter is 1.536 MHz which is the crystal clock frequency divided by 9. Since this is a divide-by-10 counter, the frequency at the final stage is one tenth of the input frequency or 153.6 kHz.

The clock is again divided by 10 in a second decade counter producing an output frequency of 15.36 kHz which is the horizontal display frequency. The output of the final stage of this counter is signal HORIZ L which is at ground level during horizontal retrace time. The high-to-low transition of this signal clocks the SYNC flip-flop producing H FLY H which inhibits automatic incrementing of the X register and the loading of the VSR.

The clock is fed to three more counters to produce the clocks for the baud rates available in the display. The last counter in the timing chain is used to develop the vertical display synchronization signal, VERT H. This counter is jumper selected to divide by 10 or divide by 12 to produce a 60 Hz or 50 Hz VERT H signal.

Figure 2-29 is a diagram of the CRT used in the display. It consists of a heater, an electro-emitting cathode, a control grid for biasing, a focus grid for shaping the beam, a screen grid for accelerating the beam to the phosphor-coated face of the tube (screen), and an anode which provides the main accumulator.

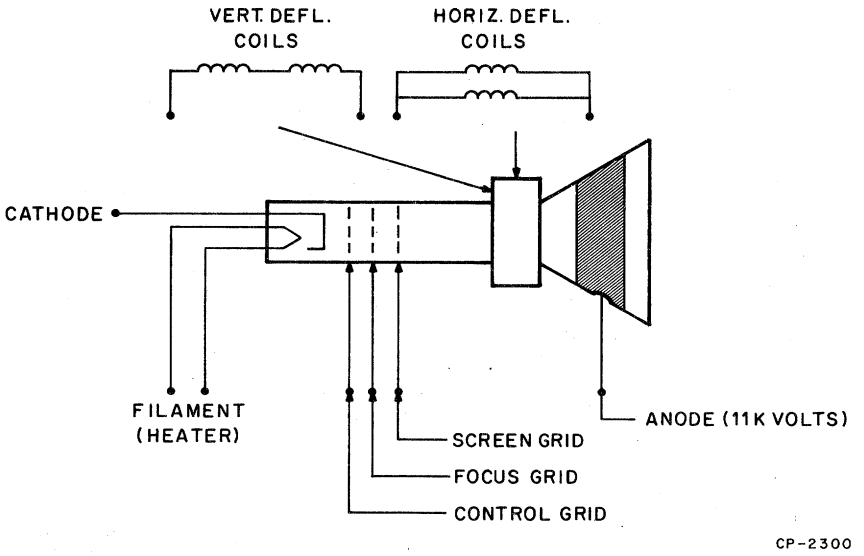


Figure 2-29 Cathode Ray Tube

2.2.2.3 Keyboard Circuits – The keyboard is arranged so that the keys form an 8x10 matrix and every key except the BREAK key has been assigned a unique identifying number representing its position in the matrix. The AC register is used to detect keys that have been activated (typed). AC0, 1, and 2 are decoded to enable one of the eight lines of the matrix; AC3, 4, 5, and 6 are decoded to enable one of the ten columns. Any key can be checked by placing its identifying number in the AC register. If the key is not down, FLAG L will be true.

The keyboard/video display program polls the keyboard during vertical retrace time by loading the AC register with the highest key number and entering a program loop that continually subtracts one from the AC register and tests the result until an active key is found or until the AC equals zero.

When a key is "down," the program leaves the test loop and stores the key number in Keyboard A or Keyboard B of the scratchpad memory. On subsequent keyboard pollings, the program will fetch the numbers stored in Keyboard A and Keyboard B and check the keyboard to see if one or both of these keys are still "down." If both keys are down, the program leaves the loop and no keyboard entries are made. When either of these keys are found to be "up," scratchpad locations Keyboard A and/or Keyboard B are cleared and a new keyboard search is started. This test routine is always performed before every keyboard test to prevent multiple entries of the same character.

After storing the identification number of the active key, the program looks up the ASCII code for that key in a table in the ROM, then transfers the ASCII-coded character to the UART for transmission to the processor.

The BREAK key cannot be tested by the program. The CONTROL key, if activated while a ROM word is being loaded into the RAM, will force the two most significant bits of the ROM word to zero. The ROM word is transferred to the RAM if AC is greater than RAM during a conditional load RAM command. The BREAK key interrupts the UART serial data output line for as long as the key is held. The break key functions independently of the program.

2.2.2.4 Microprogramming – The ROM resident microprogram controls all operations in the display. This includes the three major operations performed by the display: (1) displaying characters and refreshing the screen at a line frequency rate, (2) acting as an input device by transmitting key codes entered by an operator to the SLU, (3) acting as an output device by processing or displaying codes received. In addition, the microprogram directs the advanced features such as controlling data flow in the hold screen mode and performing line relocation when scroll is pressed.

To perform these tasks, the microprogram needs control registers and flip-flops, counters, temporary storage, etc. The scratchpad memory serves all these requirements. All status information is stored, along with incoming characters, in the scratchpad silo. Figure 2-30 is a layout of the scratchpad memory.

Figure 2-31 is a flow diagram of the microprogram operations. Top of-screen tests are performed at line frequency rates; i.e., 60 times each second in 60 Hz units (50 times each second in 50 Hz units). The UART flag is checked after horizontal scans.

The keyboard is checked between displayed frames; i.e., during vertical retrace time. If one or more keys are pressed, the terminal transmits the code representing the depressed key to the processor.

Figure 2-32 is a simplified flow diagram of the keyboard entry subroutine. The AC register is set to equal the highest numbered key on the keyboard, and then a KEY J command tests the fl ag to see if the key is down. If the key is not down, the AC register is decremented and the flag is tested again. This loop is repeated until a pressed key is found. Then an active key is located, the program looks up the ASCII code for the pressed key in a table in the ROM, loads the ASCII character into the UART, and transmits the character to the processor.

If none of the keys are down, the program will exit the routine when the AC register is equal to zero. A jumper in the keyboard is wired to act like a pressed key whenever it is referenced. It is referenced when the AC equals zero, meaning the keyboard was polled but no keys were down.

The identification number of the key is written into the scratchpad to prevent multiple transmissions of the same character. Since the keyboard is polled 60 times a second, it is almost impossible not to detect a pressed key more than once. As a first step then, the program reads the identification numbers stored in Keyboard A and Keyboard B of the scratchpad and checks the keyboard to see if these keys are still down. If they are, no transmission takes place during this scan. If one or both of the keys are up, the program clears the scratchpad location associated with the key and polls the keyboard.

A LF command received from SLU 1 when the cursor is on the bottom line will cause the terminal to scroll; that is, every line on the screen will move up one position leaving the bottom line blank—ready to receive more characters. Information displayed on the top line is lost and will be replaced by information previously displayed on the second line (line 1). To erase every RAM line and rewrite these lines with the contents of the following RAM line would take too much time and be an unreasonable way to accomplish scrolling. Instead, any RAM line can be displayed as the top line of the screen. This means that after one scroll, the top line would be RAM line 1 and the bottom line would be RAM line 0. Successive scrolls would cause RAM line 2, 3, 4, etc. to be displayed as the top line and RAM line 1, 2, 3, etc. to be displayed as the bottom line.

A scratchpad location is used to remember which RAM line is displayed on the top screen line. This location, TOP LINE, contains a line number between 0 and 23 and is cleared to 0 to power-up time. Memory location CUR Y contains the RAM line address of the cursor; location SCREEN LINE contains the screen line address of the cursor.

The hold screen mode allows the operator to control the rate at which data from the processor enters and leaves the screen. If left unchecked, high speed data from the processor would be displayed for a very short time and then scrolled up and off the screen; the operator would not have enough time to read the data. In hold screen mode, scrolling is commanded by the operator.

When the cursor is on the bottom line of the screen and a line feed comand (LF) is received from the processor, the program stores the line feed command in the LINE FEED BUFFER of the scratchpad and transmits the code for signal X OFF. The X OFF signal is used to request that data transmission to the terminal be stopped. A few characters will be sent before the program receives and acts on the request. The program stores these characters in the silo portion of the RAM.

To request more data, the operator presses SCROLL. The display program responds by scrolling the screen and then processing the characters previously stored in the silo until the silo is empty. The program then sends X ON to SUL 1, and data transmission is resumed until another LF is received.

When the terminal receives the code for ESC Z from the processor, it interprets this code as a request for the terminal to identify itself. The terminal does this by transmitting ESC/K to the processor. A terminal with a printer option will transmit ESC/M. The code for these three characters cannot be sent as one sequence; therefore, one character is sent after each frame displayed on the screen. The terminal must remember what portion of the sequence has been sent. Location ID of the scratchpad is used to store the status of the identification process. They are:

0	An ESC Z command is not pending.
135	An ESC Z has been received.
033	An ESC code has been sent to the processor.
057	A Slash (/) code has been sent to the processor.
101	A K or M code has been sent to the processor.

During the identification process, the keyboard is not polled. This is to prevent keyboard characters from being mixed with the three-character escape sequence.

When the first character in the sequence has been sent, location IC is cleared to zero and keyboard polling resumes.

	13	14	15	16	17	0	1	2	3	4	5	6	7	10	11
32															
33								HOST SILO							
34								PRINTER SILO							
35		SILO OUTPUT POINTER	SILO INPUT POINTER	XON / XOF	CURSOR X	FRAME COUNT	BELL COUNT			PRINTER SILO INPUT POINTER	PRINTER SILO OUTPUT POINTER	EQS LINE		PRINTER X	SCROLL COUNT
36	XMIT BUFFER	KEYBOARD BUFFER A	EQS COUNT	SILO COUNTER	CURSOR Y	TOP LINE	VIDEO LINE				PRINTER SILO COUNT	SCREEN CURSOR LINE	AUTO PRINT FF	PRINTER Y	HOLD SCREEN FF
37	TERMINAL I.D.	XMIT BUFFER	KEYBOARD BUFFER	LF. BUFFER	VIDEO SCAN COUNT	PRINTER CONTROLLER FF	PRINTER LINE COUNT	VIDEO LINE COUNT		KEYBOARD APPLICATION MODE FF		ESCAPE FF / DCA COUNTER	INCOMING CHARACTER	GRAPHICS FF	

08-1879A

Figure 2-30 Scratchpad Memory

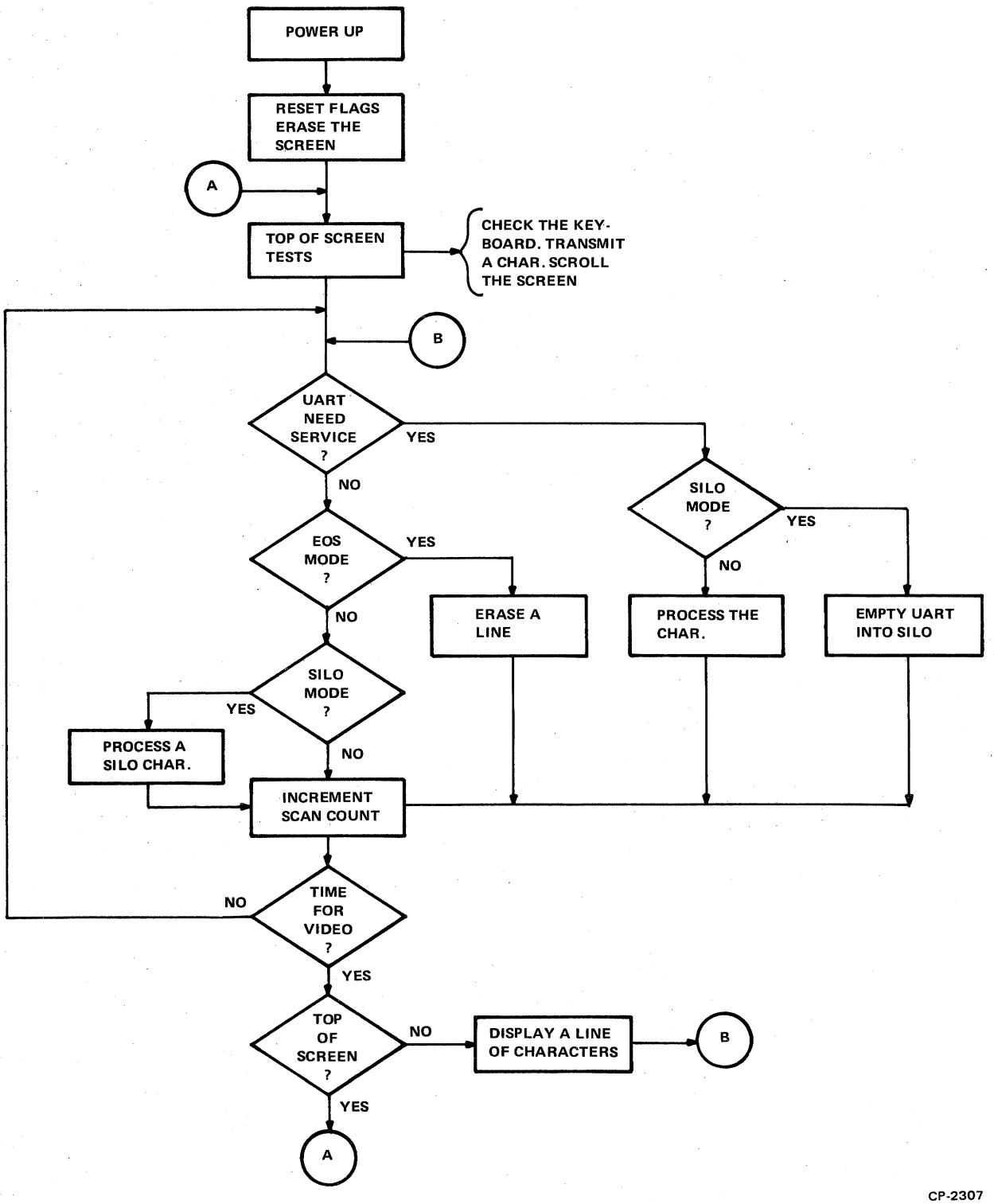


Figure 2-31 Microprogram Flow Diagram

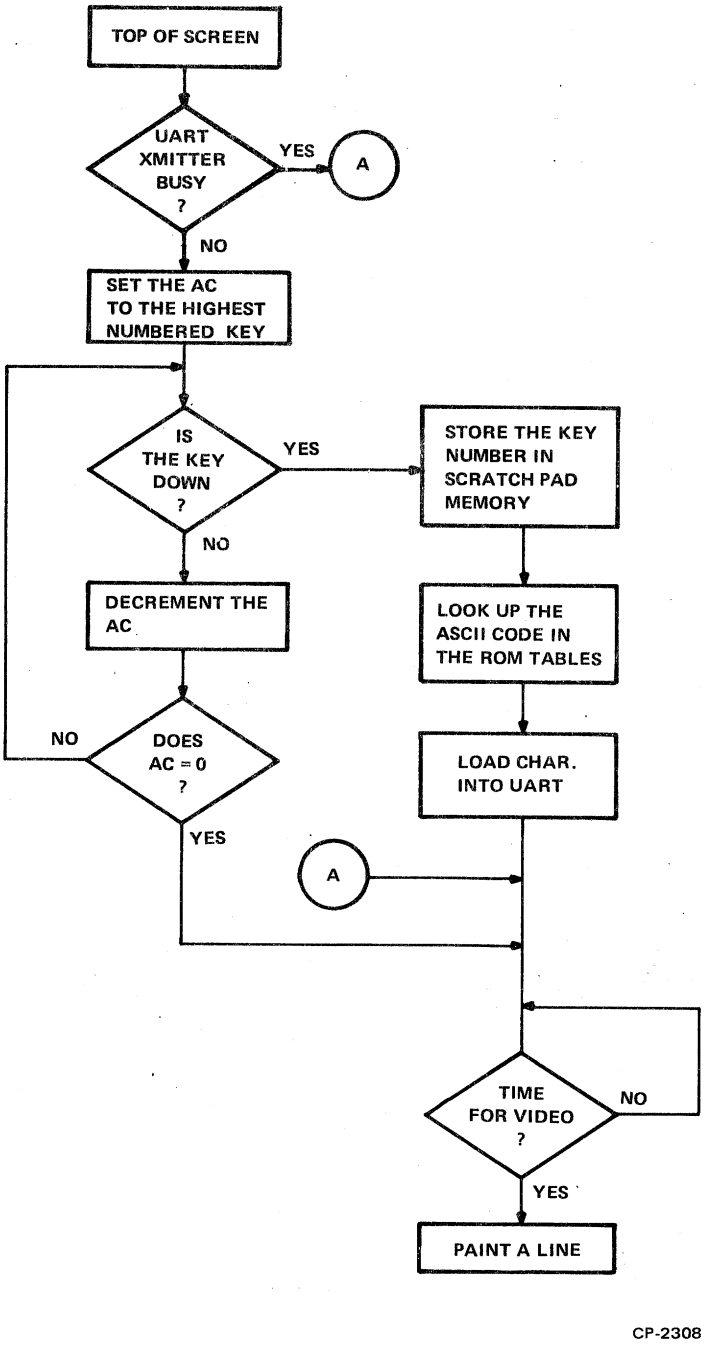


Figure 2-32 Keyboard Entry Flow Diagram

The cursor appears as a flashing underscore on the screen on the ninth scan of one of the ten scan character rows. Although the screen is refreshed 60 times a second, the cursor display is refreshed only 4 times a second to produce a blinking cursor. To achieve this low frequency refresh rate, scratchpad location FRAME COUNT is preset to 160 and is incremented every time the Y line containing the cursor is to be painted on the screen. When FRAME COUNT overflows (every 15 frames), the CRT beam is turned on, displaying the cursor, and FRAME COUNT is again preset to 160.

2.2.3 DC Power Supply

2.2.3.1 20 kHz Oscillator – The 20 kHz oscillator (clock) is a conventional NE555 oscillator. Timing is determined by R18 and C10 for the time that the output is high and R19 and C10 for the time that the output is low. The output is a 20 kHz rectangular wave. High time occurs for approximately 20 μs. This creates a window during which it is possible to turn off the control transistor, Q2. Q2 can never be turned off when the clock is low.

With the output of NE555 high, C10 is charged through R18. When the voltage across C10 reaches 2/3 Vcc, the output of E1 drops and the discharge transistor turns on. C10 is discharged through R19 until the voltage across C10 drops to 1/2 Vcc. The output goes high and the discharge transistor turns off; C10 is again charged through R18. C9 and C18 are decoupling capacitors.

2.2.3.2 Pulse Width Modulator – The trigger of E2 is connected through a 4.7k resistor, R17, to pin 3 of the clock. Whenever the clock is low, the output of the pulse width modulator is high and Q2 is on, holding Q1 (the main power switch) off. Also C11, the timing capacitor for the pulse width modulator, is prevented from charging by forward-biased diode D19. When the clock goes high, C11 is charged from the voltage controlled current source in the error amplifier. The control voltage of E2 is connected to the 5 V reference. Thus when the voltage across C11 reaches 5 V, the output of E2 drops, Q2 turns off, and Q1 turns on. When the clock drops to its low state, pin 3 of the pulse width modulator goes high, turning Q2 on again and Q1 off. At the same time, C11 is discharged and ready to begin the next pulse. The pulse width is determined by the time the clock is high minus the time C11 charges. The faster C11 charges, the longer the pulse width.

2.2.3.3 Inverter – When Q1 turns on, current flows through the primary of T1. When Q1 turns off, the windings of T1 reverse polarity. The rectifiers in the secondaries become forward biased and conduct, thus the energy stored while the primary was conducting is released to the filter capacitors and loads the secondary windings. The control circuit senses the voltage at the 5 V output and adjusts the on/off duty ratio of Q1 to maintain this output at 5 V. All other outputs remain relatively constant also.

2.2.3.4 Short Circuit Protection – The short circuit protection circuit consists of E6, an LM339 comparator, and R29, the current sense resistor. Normally the output of the comparator is high. During an over-current condition, the voltage drop across R29 increases enough to cause the voltage at pin 4 to be greater than at pin 5. The comparator changes state; i.e., pin 2 drops low pulling the trigger of the pulse width modulator to ground. The pulse width modulator output goes high to prevent the main power switch from turning on. As soon as the current through R29 drops below approximately 10 A, the comparator output returns to a high state and normal operation resumes.

CHAPTER 3
MAINTENANCE

3.1 MAINTENANCE PHILOSOPHY

This chapter contains information necessary to isolate and repair DECstation malfunctions.

Figure 3-1 is an index to the troubleshooting procedures contained in Tables 3-1 through 3-4. Step-by-step turn on and operating instructions are followed by normal display illustrations. If these displays are absent or incorrect, refer to the corresponding tables for troubleshooting information.

The use of the MR78 ODT is also described in Paragraph 3.2.2 to help isolate intermittent malfunctions or abnormal symptoms not provided in the troubleshooting tables.

3.2 TROUBLESHOOTING

3.2.1 Troubleshooting Procedures

The possible equipment malfunctions listed in Tables 3-1 through 3-4 are categorized by abnormal symptoms. Corresponding causes are listed in order of probability. Corrective actions are, for the most part, limited to the adjustments and/or substitution of major replaceable subassemblies for those suspected to be defective.

3.2.2 MR78-BB ODT Package

The MR78-BB is a bootstrap ROM for the VT78, containing multifield ODT and a binary loader suitable for use with the PRS01 papertape reader. It provides the Field Service Engineer with a tool to modify diagnostics or customer software. It also allows the Field Service Engineer to generate short programs as an aid in isolating and correcting equipment malfunctions.

It is assumed that the operator is acquainted with the general operation of PDP-8 ODT programs. If not, consult the Introduction to Programming book or the OS8 Handbook for additional ODT information.

NOTE

The VT78 terminal must be able to function well enough to display the letters AB before it displays a HLT message. If it does not, the ODT package can not be run. It is possible to run ODT if there is a HLT message after B and before C, D, or F, but a HLT message after D indicates an extended memory problem which might prevent ODT from running.

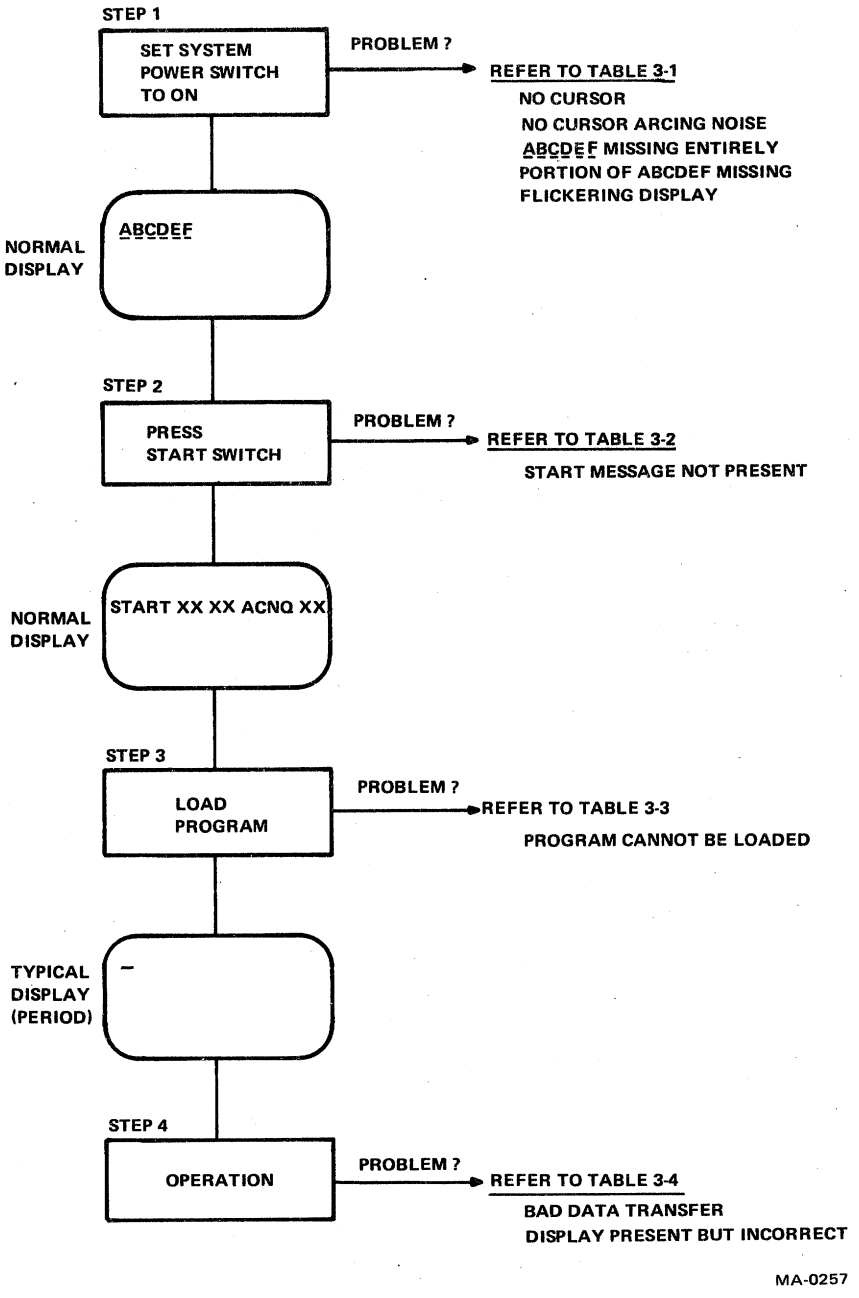


Figure 3-1 Guide to Troubleshooting Procedures

Table 3-1 Power On Troubleshooting Procedure

Symptom	Possible Cause	Corrective Action
No cursor.	Intensity control turned down.	Adjust intensity control (Figure 3-2).
No cursor, raster missing, DC OK light off.	Blown fuse.	Replace fuse (Figure 3-2).

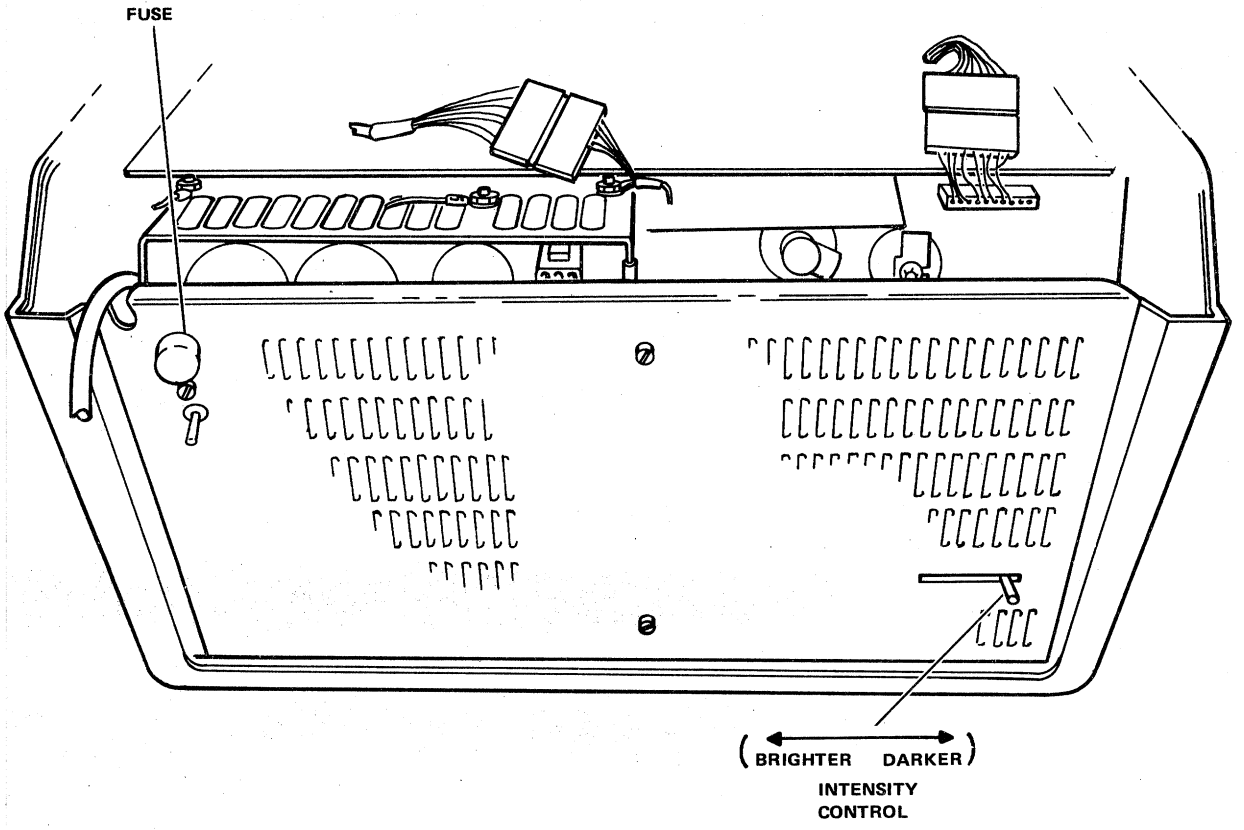


Figure 3-2 Intensity Control and Fuse Locations

Table 3-1 Power On Troubleshooting Procedure (Cont)

Symptom	Possible Cause	Corrective Action
No cursor, raster missing, DC OK light off (Cont).	No prime power.	Restore source of prime power.

WARNING

There are high voltages present in the power supply and CRT. Make sure the terminal power line is unplugged and the CRT and capacitors are discharged as shown in Figure 3-3 before handling the power supply or CRT components. Make sure ground connection is made before discharging these points.

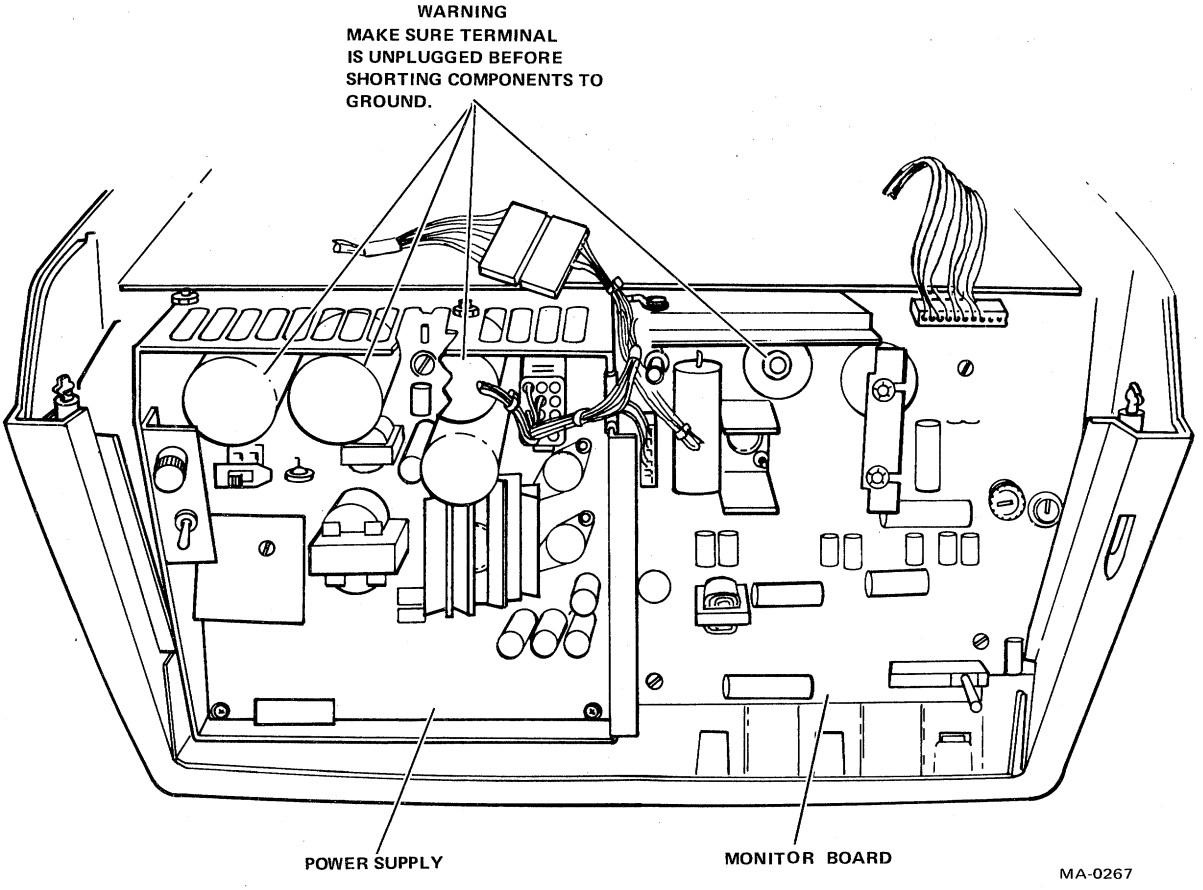


Figure 3-3 High Voltage Discharge Locations

Table 3-1 Power On Troubleshooting Procedure (Cont)

Symptom	Possible Cause	Corrective Action
No cursor, raster missing, DC OK light on.	Anode cap disconnected.	Connect anode cap at power supply (Paragraph 3.3.5).
	Anode clip disconnected.	Connect anode clip at CRT bell (Paragraph 3.3.5 and Figure 3-4).

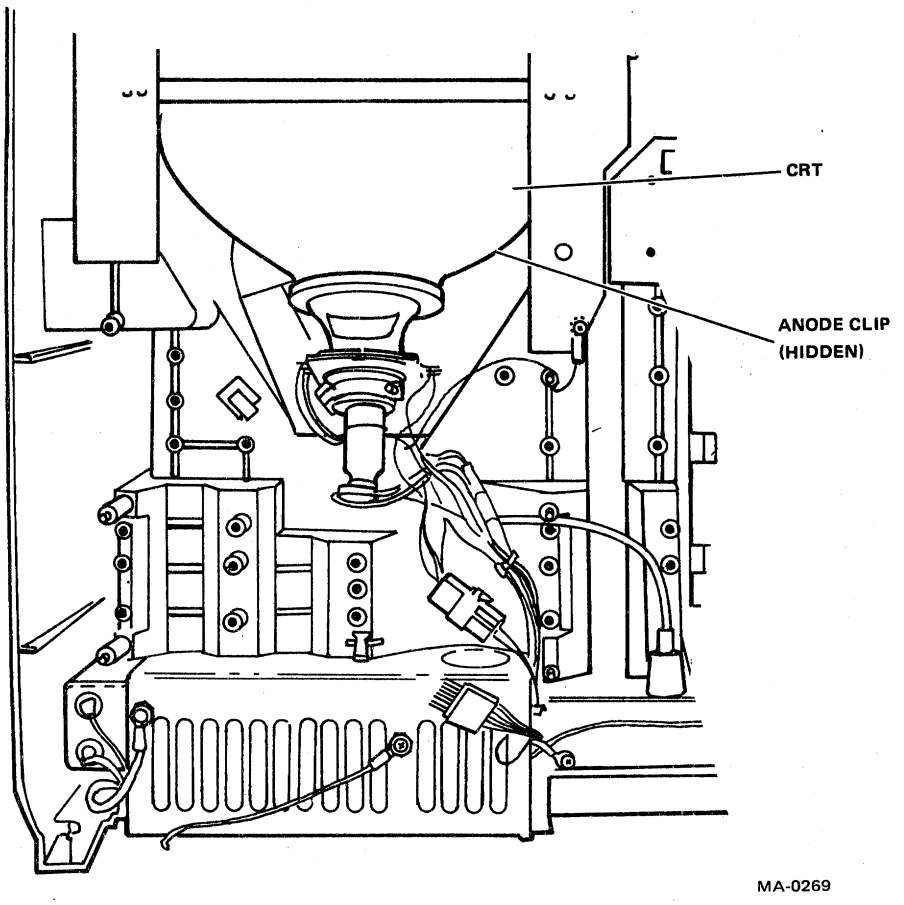


Figure 3-4 Anode Clip Locations

Table 3-1 Power On Troubleshooting Procedure (Cont)

Symptom	Possible Cause	Corrective Action
No cursor, raster missing, DC OK light on (Cont).	Defective power supply assembly.	Replace power supply assembly (Paragraph 3.3.5).
	Defective monitor board.	Replace monitor board (Paragraph 3.3.6).

WARNING

Use caution when handling the CRT to avoid shattering the tube. The CRT is an evacuated device which can implode when broken.

	Defective CRT.	Replace CRT (Paragraph 3.3.8).
No cursor, raster missing, DC OK light on.	Defective RUT module.	Replace RUT module (Paragraph 3.3.4).
	Defective DP module.	Replace DP module (Paragraph 3.3.4).
	Defective keyboard.	Replace keyboard module (Paragraph 3.3.4).
	Defective character generator module.	Replace character generator module (Paragraph 3.3.4).

WARNING

There are high voltages present in the power supply and CRT. Make sure the terminal power line is unplugged and the CRT and capacitors are discharged as shown in Figure 3-3 before handling the power supply or CRT components.

	Defective power supply assembly.	Replace power supply assembly (Paragraph 3.3.5).
No cursor, raster present, arcing heard, DC OK light on.	Anode cap loose.	Tighten cap (Figure 3-3).
	Anode clip loose.	Tighten clip (Figure 3-4).
Cursor present, no ABCDEF, CPU OK light on.	Baud rate switch set incorrectly.	Set baud rate switch (bottom of terminal) to 9600 baud (Figure 3-5).
	Function switch set incorrectly.	Set function switch (on bottom of terminal) to full duplex position (Figure 3-5).

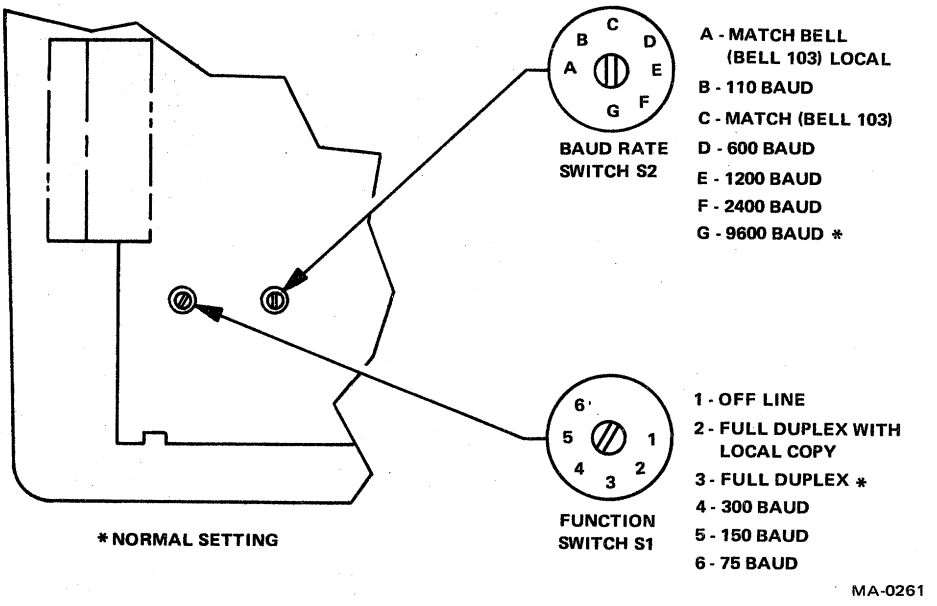


Figure 3-5 Function and Baud Rate Switches

Table 3-1 Power On Troubleshooting Procedure (Cont)

Symptom	Possible Cause	Corrective Action
Cursor present, no ABCDEF, CPU OK light on (Cont).	Defective processor module.	Replace defective module (Paragraph 3.3.2).
Cursor present, no ABCDEF. CPU OK light off.	Defective processor module.	Replace defective processor module (Paragraph 3.3.2).
Cursor present, A only displayed.	Defective processor or memory module.	Replace module (Paragraph 3.3.2).
Cursor present, AB only displayed.	Defective processor module.	Replace defective processor module (Paragraph 3.3.2).
	Defective I/O distribution panel.	Replace defective panel (Paragraph 3.3.3).
Cursor present, ABC only displayed.	Defective processor module.	Replace defective module (Paragraph 3.3.3).
	Defective I/O distribution panel.	Replace defective module (Paragraph 3.3.3).
Cursor present, ABCD only displayed.	Defective processor or memory module.	Replace defective module (Paragraph 3.3.2).
Cursor present, ABCDE only displayed.	Defective processor module.	Replace defective module (Paragraph 3.3.2).
Cursor present, ABCDEF displayed but display flickers.	W7 jumper on RUT.	Remove W7 jumper (60 Hz units) or insert jumper W7 (50 Hz units) (Figure 3-6).

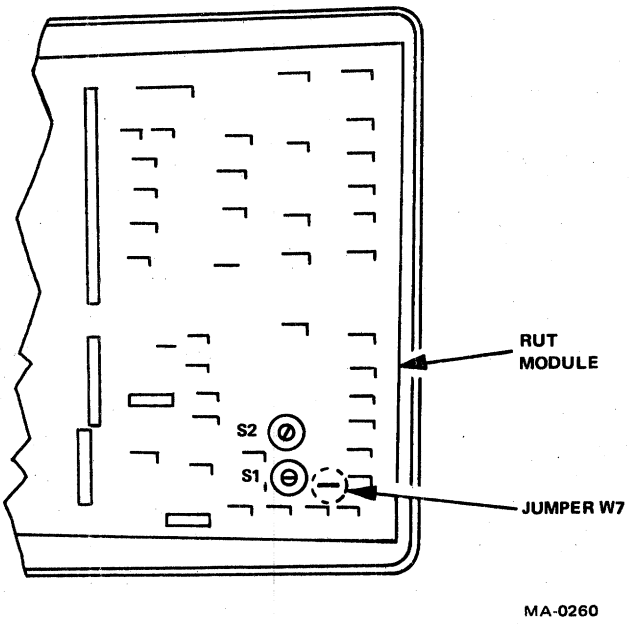


Figure 3-6 Jumper W7 Location

Table 3-2 Start Up Troubleshooting Procedures

Symptom	Possible Cause	Corrective Action
Start message not present.	Defective processor module.	Replace defective module (Paragraph 3.3.2).
	Loose or defective START switch or cable.	Tighten or replace as required.
	Defective I/O distribution panel.	Replace defective panel (Paragraph 3.3.3).

Table 3-3 Program Loading Troubleshooting Procedures

Symptom	Possible Cause	Corrective Action
Program can not be booted.	Defective RX78 program loading device (if applicable).	See applicable maintenance manual (RX78 floppy disk drive system information).
	Defective MR78 program loading device (if applicable).	Replace MR78.
	Defective fuse (F1) on distribution panel (MR78 only).	Replace fuse.
	Defective processor module.	Replace defective module (Paragraph 3.3.2).
	Defective memory module.	Replace defective module (Paragraph 3.3.2).
	Loose I/O distribution panel connector.	Tighten connector.
	Defective I/O panel.	Replace panel (Paragraph 3.3.3).
	Defective I/O cable.	Replace I/O cable.

Table 3-4 Operational Troubleshooting Procedures

Symptom	Possible Cause	Corrective Action
Unable to adjust focus; display remains fuzzy.	Defective monitor board.	Replace monitor board (Paragraph 3.3.6).
Entire raster too short (Figure 3-7).	Vertical size/linearity out of adjustment.	Adjust vertical size/linearity control (Paragraph 3.4.1 or 3.4.3).
Unable to adjust raster or character width.	Defective monitor board.	Replace monitor board (Paragraph 3.3.6).
Entire raster too narrow (Figure 3-8).	Horizontal size out of adjustment.	Adjust horizontal size control (Paragraph 3.4.1).

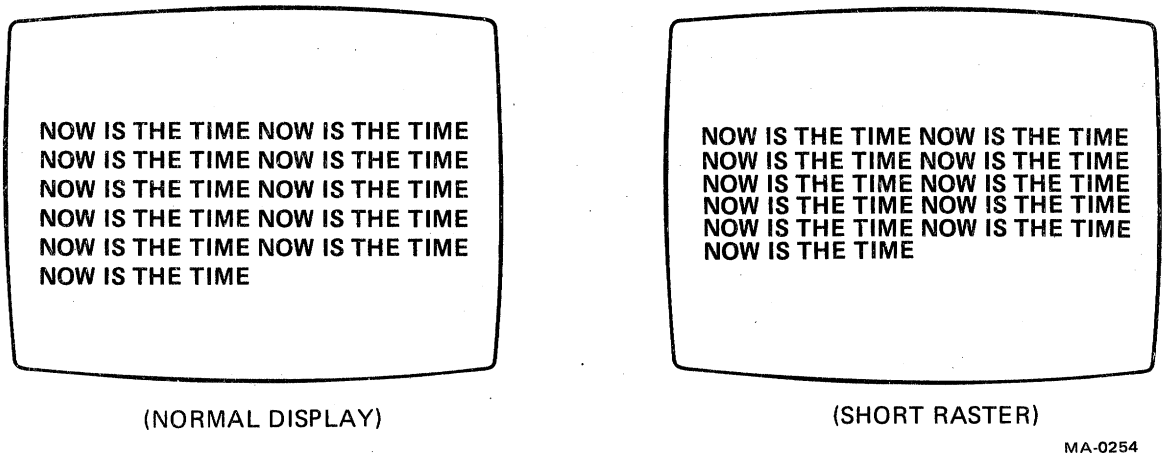


Figure 3-7 Short Raster Indication

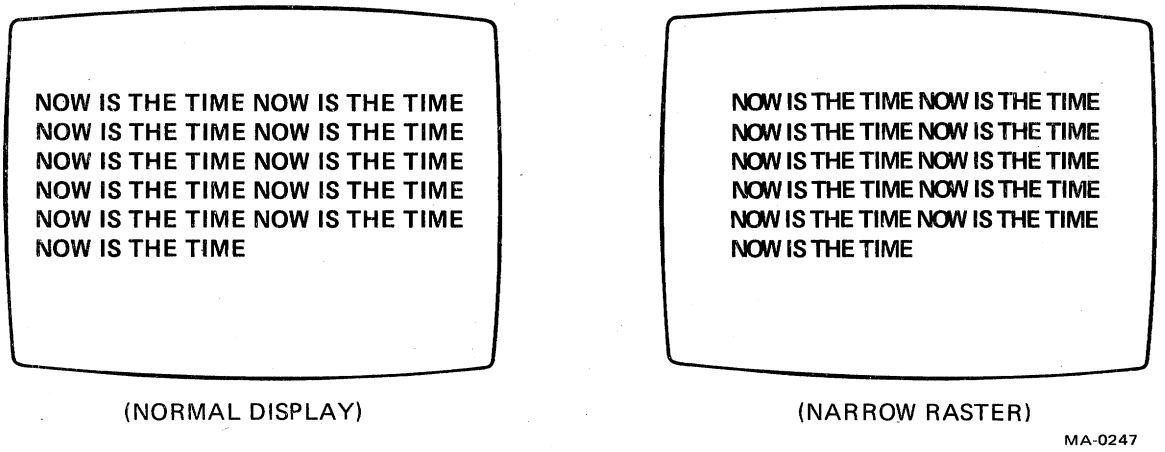


Figure 3-8 Narrow Raster Indication

Table 3-4 Operational Troubleshooting Procedures (Cont)

Symptom	Possible Cause	Corrective Action
Unable to adjust intensity/brightness.	Defective monitor board.	Replace monitor board (Paragraph 3.3.6).
	Defective power supply.	Replace power supply (Paragraph 3.3.5).
	Defective CRT.	Replace CRT (Paragraph 3.4.1).
Characters too short (Figure 3-9).	Vertical size out adjustment.	Adjust vertical size control (Paragraph 3.4.1).
	Vertical linearity out of adjustment.	Adjust vertical linearity control (Paragraph 3.4.3).
	Defective monitor board.	Replace monitor board (Paragraph 3.3.6).
Characters too thin (Figure 3-10).	Horizontal size out of adjustment.	Adjust horizontal size control (Paragraph 3.4.1).
Characters uneven (Figure 3-11).	Defective monitor board.	Replace monitor board (Paragraph 3.3.6).
Distance between lines uneven (Figure 3-12).	Yoke out of adjustment.	Adjust controlling tabs on yoke.
Lost data.	Baud rate switch set incorrectly.	Adjust baud rate to mode of operation (Figure 3-5).
	S2 not set correctly.	Set S2 in any position other than fully clockwise position (Figure 3-5).

Figure 3-9 Short Character Indication

Figure 3-10 Thin Character Indication

Figure 3-11 Uneven Character Indication

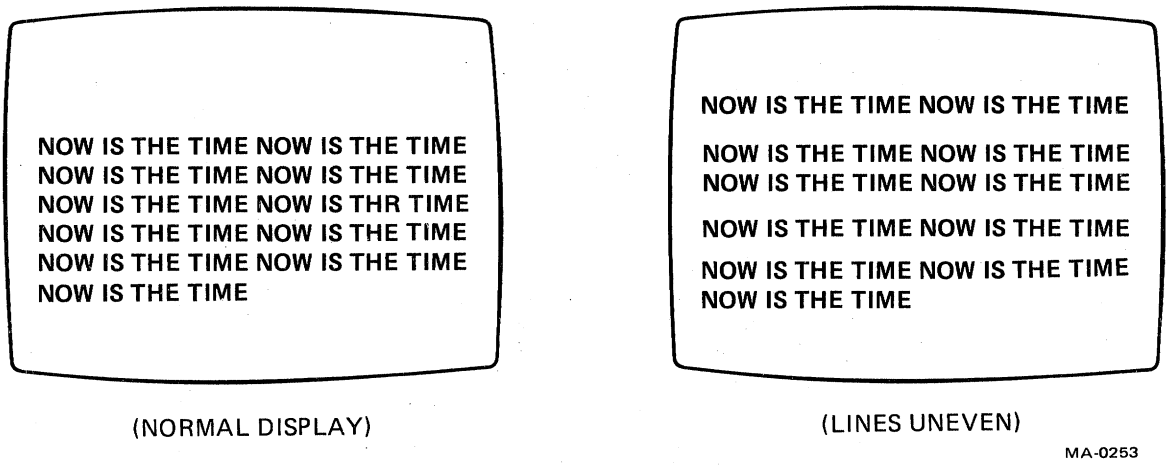


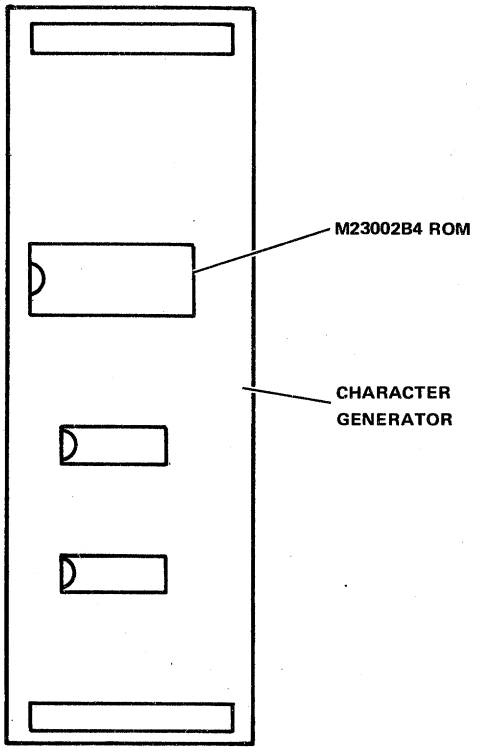
Figure 3-12 Uneven Lines Indication

Table 3-4 Operational Troubleshooting Procedures (Cont)

Symptom	Possible Cause	Corrective Action
Illegal characters generated (Figure 3-13).	Defective character generator board.	Replace character generator board (Paragraph 3.3.4).
	Defective RUT module.	Replace RUT module (Paragraph 3.3.4).
	Baud rate switch set incorrectly.	Set baud rate switch to 9600 baud (Figure 3-5).
Random characters generated or screen fills with random characters when first turned on (Figure 3-15).	RUT/Character ROM/PROM chips are incompatible.	Check that ROM chip is A23002B4 series (Figure 3-14).
	Defective character generator module.	Replace character generator module (Paragraph 3.3.4).
	Defective DP module.	Replace DP module (Paragraph 3.3.4).
	Defective RUT module.	Replace RUT module (Paragraph 3.3.4).
Wrong character displayed when typed.	Defective keyboard.	Replace keyboard (Paragraph 3.3.7).
No key clicks; cursor present.	Defective RUT module.	Replace defective module (Paragraph 3.3.4).
No key click or cursor, raster present.	Defective DP module.	Replace defective module (Paragraph 3.3.4).
	Defective keyboard.	Replace keyboard (Paragraph 3.3.7) .
No key clicks; characters displayed.	Defective RUT module.	Replace defective module (Paragraph 3.3.4).
No key clicks; characters generated wrong but legal.	Defective DP module.	Replace DP module (Paragraph 3.3.4).
	Defective RUT module.	Replace defective module (Paragraph 3.3.4).
	Defective keyboard.	Replace keyboard (Paragraph 3.3.7).

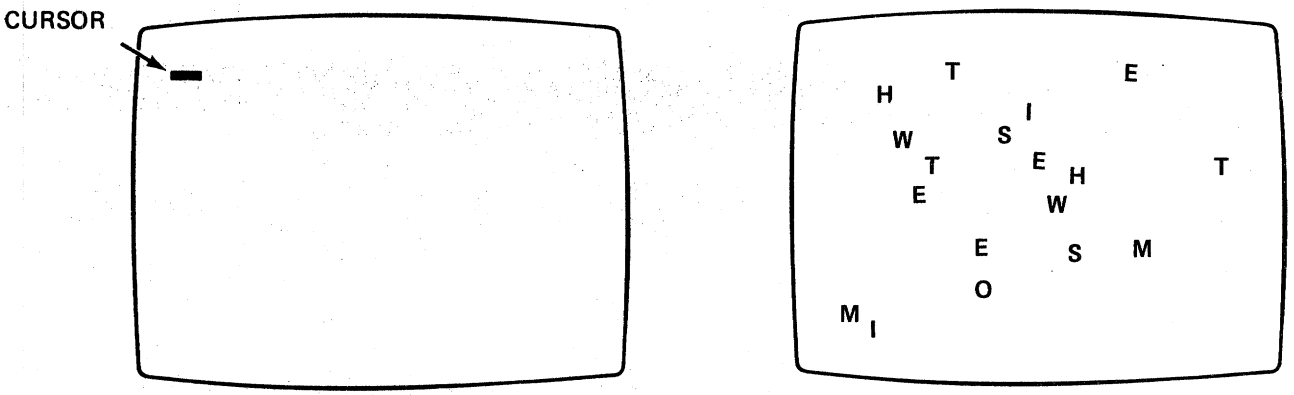
MA-0250

Figure 3-13 Illegal Characters Indication



MA-0270

Figure 3-14 A23002B4 – ROM Chip Location



MA-0246

Figure 3-15 Random Character Indication

Table 3-4 Operational Troubleshooting Procedures (Cont)

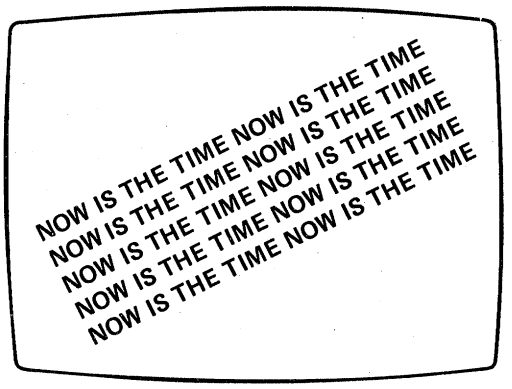
Symptom	Possible Cause	Corrective Action
No key clicks; characters legal but distorted (Figure 3-16).	Defective character generator module.	Replace character generator module (Paragraph 3.3.4).
Entire raster tilted (Figure 3-17).	Incorrect yoke position.	Adjust yoke tilted on the neck of the CRT clockwise or counterclockwise. Make sure the yoke is fully forward. Tighten hold down screw.
Raster too large; all characters enlarged and fuzzy (Figure 3-18).	Incorrect yoke position.	Push yoke forward to the CRT bell as far as it will go. Tighten hold down screw.
Initial diagnostics good but customer's program will not run (SLU 2 or SLU 3 functions).	EIA device defective.	Replace I/O distribution panel.
	Defective I/O cable.	Replace cable.
	Prebaud rate select switch not set correctly.	Set baud rate select switch on I/O distribution panel to correct setting for device used.
Initial diagnostics good but LQP78 or LA78 does not operate properly.	Loose I/O distribution panel cable connector.	Tighten connector.
	Defective cable.	Replace cable.
	Defective processor module.	Replace processor module.
	Defective LA78 or LQP78.	Refer to the appropriate manual for troubleshooting information.

NOW IS THE TIME
(NORMAL CHARACTERS)

NOW IS THE TIME
(DISTORTED CHARACTERS)

MA-0251

Figure 3-16 Distorted Character Indication



MA-0256

Figure 3-17 Tilted Raster Indication

NOW IS THE TIME
(NORMAL DISPLAY)

NOW IS THE TIME
(ENLARGED AND FUZZY CHARACTERS)

MA–0249

Figure 3-18 Enlarged and Fuzzy Characters Indication

3.2.2.1 Starting the ODT – To load and start ODT, perform the following steps:

1. Set the VT78 terminal power switch, located at the rear of the VT78 terminal, to the off (down) position.

2. Attach the MR78-BB to the rear of the VT78. Make sure the connector is seated properly before applying pressure. Tighten the holding screws.

3. Set the VT78 terminal power switch to the on (up) position.

4. Press the VT78 START pushbutton (even if the VT78 is printing a series of HLT messages). Make sure ODT is running by typing an address, followed by a slash (/). ODT should display the contents of that location. Table 3-5 contains a summary of the ODT commands.

3.2.2.2 Running the Reader – To operate the reader perform the following:

CAUTION

Make sure that VT78 terminal power is turned off when connecting the PRS01 cable to prevent possible damage to the terminal's SLU3 EIA receiver.

1. Attach the PRS01 reader to the *auxiliary* connector on the rear of the VT78 terminal (Appendix D).

2. Press the START switch on the VT78 terminal.

3. Place the papertape in the reader with the leader at the read station.

4. Type R or (N)R (N = number of binary tapes to be loaded)

5. Turn the reader on. The tape should run completely through the reader.

6. Turn the reader off. If the (N)R command was used, the binary loader will return to ODT. The operator may then alter the program or start it at a specified address using the "G" command.

NOTE

The PRS01 is available with 300 and 2400 baud rates. The constant in location 37777 sets the SLU 3 baud rate and is correct for 300 baud when the START pushbutton is pressed on the VT78. If your PRS01 has a 2400 baud rate, change this constant from 5 to 12 (using ODT).

Table 3-5 Summary of ODT Commands

Command	Function
NNNNN/	Open location NNNNN.
/	Re-open latest opened location.
NNNN;	Deposit NNNN in currently opened location; close that location and open the next location without typing its address.
;	Do not modify currently opened location; otherwise same as NNNN.
Return	Close currently opened location.
Linefeed	Close opened location; open next sequential location.
NNNN+	Open (current location +NNNN) location. **NOTE** **ODT will not automatically cross field boundaries; instead, it will wrap in the same field.**
+ (plus)	Equivalent to 1+.
NNNN-	Open (current location - NNNN) location.
- (minus)	Equivalent to 1-.
^ (circumflex)	Close current location. Take contents as a memory reference and open the location referenced. If the circumflex indirect bit is set, the indirect address calculation is also performed, and the opened location is in the "F" field. If the instruction performs auto-indexing, the auto-index register is incremented before use. **NOTE** **The op code portion of the instruction is not tested; hence, all op codes (including IOT and OPR) are treated as MRI instructions.**
_ (underscore)	Close location, take its contents as a 12-bit address, and open that address in the "F" field.
NNNNNG	Start the program at address NNNNN. The AC and link are cleared, the interrupt system is off, and the TTO flag is cleared. The data field is made equal to the instruction field.
G	Equivalent to typing "200G."

Table 3-5 Summary of ODT Commands (Cont)

Command	Function
NNNNNB	Set up breakpoint linkage for a breakpoint at address NNNNN. Only one breakpoint is allowed at any time. Locations 4, 5, and 6 of the breakpoint field are used for the linkage. The old contents of these locations are lost. (See Paragraph 3.2.2.3 for restrictions on the placing of breakpoints).
B	Completely remove breakpoint.
A	Open software accumulator.
L	Open software link.
NNNNC	Continue from breakpoint. Load the AC, L, INT ENABLE, data field, and TTO flag with the values held in the software registers in ODT. Resume program execution at the trapped instruction. Iterate past the breakpoint NNNN-1 times. The next time the breakpoint is reached, stop the user's program; type the contents of PC, L, AC, and MQ; and wait for further commands.
C	Equivalent to 1C.
M	Open search mask (initially 7777).
Linefeed following M	Open lower search limit (initially 0).
Linefeed following M linefeed	Open upper search limit (initially 7777).
NNNNW	Search for NNNN. Searching starts with lower search address and ends when upper search address has been processed. For each location in the search range, the word from memory is ANDed with the search mask and subtracted from NNNN. If the result is zero, the address and its contents are printed.
D	Open "D" field. "D" is initially zero and holds the data field in effect at the time of the last breakpoint. "Ds" only useage is to re-establish the data field on "continue from breakpoint." The contents of "D" must be an even multiple of 10 (octal); i.e., D=20 means data field 2.
F	Open "F" field. Like "D," "F" is initially zero and is loaded with the data field at breakpoint. "F" must also be an even multiple of 10 (octal). "F" is the field used in word search and in the MRI and indirect address calculations. "F" is also the default field used when papertapes with no field specifications are loaded. The content of "F" is ignored on "continue."
CTRL 0	Terminate output and return to keyboard input. Used for terminating long word searches or aborting the reader routine.

Table 3-5 Summary of ODT Commands (Cont)

Command	Function
I	Open the register which saves the state of the interrupt enable. The interrupt was off at breakpoint if this location contains 7777.
Linefeed following I	Open the register which saves the state of the local terminal's output flag (the TTO flag). This register is 7777, if the TTO flag was set when the I breakpoint was encountered.
R	Read one program into memory from PRSO1. When the trailer is encountered, start the program running at the last address specified. The loading defaults to the "F" field, as described in the previous paragraph. This feature allows the user to load a very large program that might overlay ODT. The "R" feature does, however, require a final field and origin statement to be on papertape. Field N: This may be omitted if the last instruction was deposited in the field of the starting address. Starting address: This is used to define the 15-bit starting address. If there is no checksum error, the program starts automatically.
NR	Read N programs from the PRSO1, return to ODT, and print the checksum after each program (should be 0000). The program is loaded into the "F" field until a field statement is encountered on the papertape. The papertape field statement then takes precedence. (See Paragraph 3.2.2.2 for details of loading programs). The programs to be loaded must be on one contiguous tape, since there is no way to start and stop the PRSO1 software. The program will not start automatically; the "G" command must be used.
Rubout	Cancels the last command, including any digits. Types "?"

3.2.2.3 ODT Notes – Operating the START pushbutton modifies locations 00004 through 00006 of memory (to turn off the interrupt system) and reads a fresh copy of the ODT/binary loader program into locations 36400 through 37777. Watch for modification of 4 through 6 (20 through 23 in early machines), if the START pushbutton is pressed after a program is loaded.

There are certain restrictions which must be observed when placing breakpoints:

1. The breakpoint must be fetched as an instruction (e.g., it can not be an argument following a JMS).
2. A breakpoint can not be placed at a CIF, RMF, RTF, or ION instruction.
3. A breakpoint can not be placed between CIF, RMF, or RTF and the next JMP or JMS instruction.
4. A breakpoint can not be placed at the instruction following an ION instruction.

Setting a breakpoint changes locations 4, 5, and 6 of the breakpoint field. Many programs, including OS8 USR routines, react badly when breakpoints are used in the same field. If you are experiencing difficulty, a breakpoint without the continue feature may be simulated by placing CIF 30; JMP I (6400) in the program. Although the continue feature is unusable, the contents of all registers at the time of breakpoint are available.

It should be noted that address 36400 is the start of the breakpoint trap routine. This address varies from ODT to ODT and is valid for the MR78-BB version only.

This version of ODT handles the interrupt and TTO flags, allowing the user to continue in an interrupt-driven program. The interrupt service routine in the user program must be able to handle interrupts from any field. This is a problem only in programs written for a 4k machine.

In some instances it may be desirable to use the MR78-BB on a VT78 terminal equipped with an RX78 floppy disk drive system. The MR78-BB is wired so that it responds to the START pushbutton rather than the internal RX78 bootstrap.

The following three-word instruction sequence can be typed into the VT78 when bootstrapping the RX78 from ODT:

1. 6002 /Start here; make sure interrupt off.
2. 6073 /PRQ; make panel request.
3. 6200 /Starting address of the RX78 bootstrap in panel memory.

3.2.2.4 Overlaying ODT – The ODT and binary loader program is loaded into memory as described in Table 3-6.

Papertapes can overlay the first parts of ODT and have the basic ODT functions of register examination; the register modification (i.e., nonbreakpoint starting), the breakpoint removal, and the paper-tape loader remain intact. The user must refrain from using overlapped features, however, because the ODT dispatch table is not changed when features are lost.

Programs which overlay ODT should be loaded last. Any prior programs loaded should not modify locations above 37000. The last program loaded (modifying 37000 through 37577) must be loaded using "R," the automatic starting loader, since the loading of the program demolishes ODT. Under no circumstances can papertapes be loaded into locations 37644 through 37777 since doing so will destroy the binary loader.

Table 3-6 ODT and Binary Loader

Location	Function
36400-36577	Breakpoint, +, -, A, I, TTO flag.
36600-36777	Continue breakpoint start, L, D.
37000-37177	Word Search, , -, F.
37200-37577	ODT keyboard monitor, breakpoint clear, nonbreakpoint start, and all other ODT functions except "R."
37600-3777	R, NR, binary loader.

3.3 SUBASSEMBLY REMOVAL AND REPLACEMENT

3.3.1 Base Assembly (Figure 3-19)

WARNING

There are high voltages present in the VT78 terminal. Make sure that the line cord is disconnected before attempting to remove or replace any of the terminal subassemblies.

1. Turn the VT78 terminal upside down.

2. Using a 1/4-in nut driver, turn the five base-assembly fasteners counterclockwise 90 degrees and lift the base assembly free.

3. The base assembly cables are long enough to allow the base assembly to be placed behind the unit for servicing. However, if the base assembly is to be separated completely from the terminal, disconnect the two patch panel plugs and remove the ground lead shown in Figure 3-20.

4. Reverse steps 1 through 3 to replace the base assembly.

3.3.2 Processor/Memory Module (Figure 3-20)

1. Remove the base assembly as described in Paragraph 3.3.1.

2. Remove the screw in the bottom of the base assembly, securing the processor/memory module to the base.

3. Remove the two screws securing the processor/memory module mounting bracket to the base assembly.

4. Lift the board with an upward and outward motion to disengage the processor/memory module option panel connectors.

5. To separate the memory and processor boards, unscrew the five screws shown in Figure 3-21.

6. Reverse steps 1 through 4 to reassemble the processor/memory module and replace it in the base assembly.

CAUTION

When inserting the processor/memory module in the base assembly, make sure that the processor/memory module and option panel connectors are aligned before applying pressure to avoid damaging the pins.

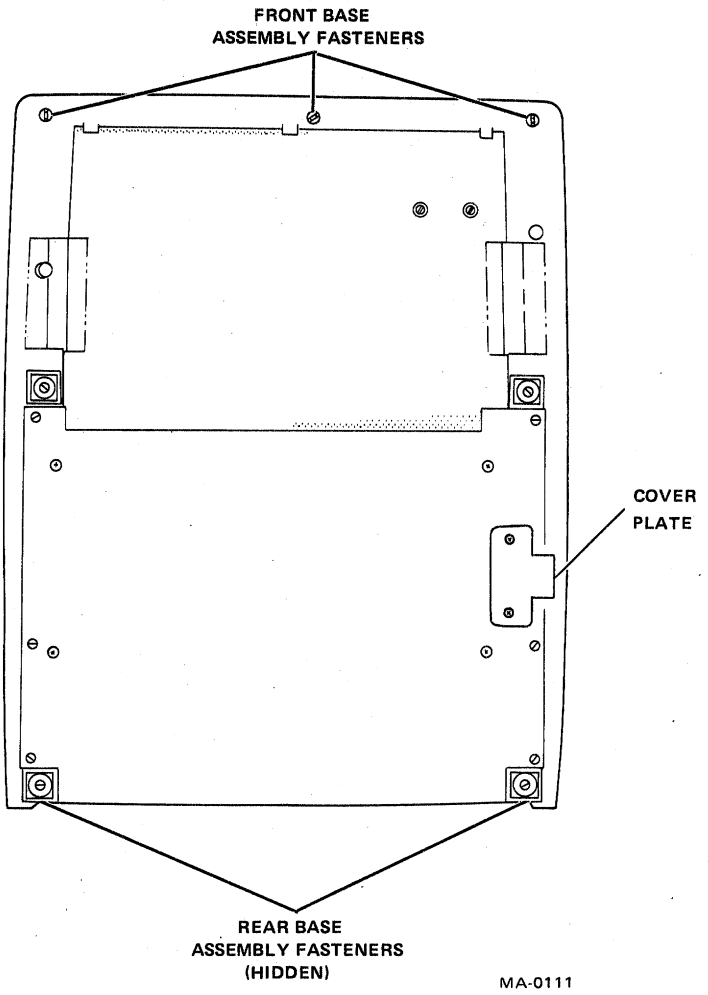


Figure 3-19 Base Assembly Removal and Replacement

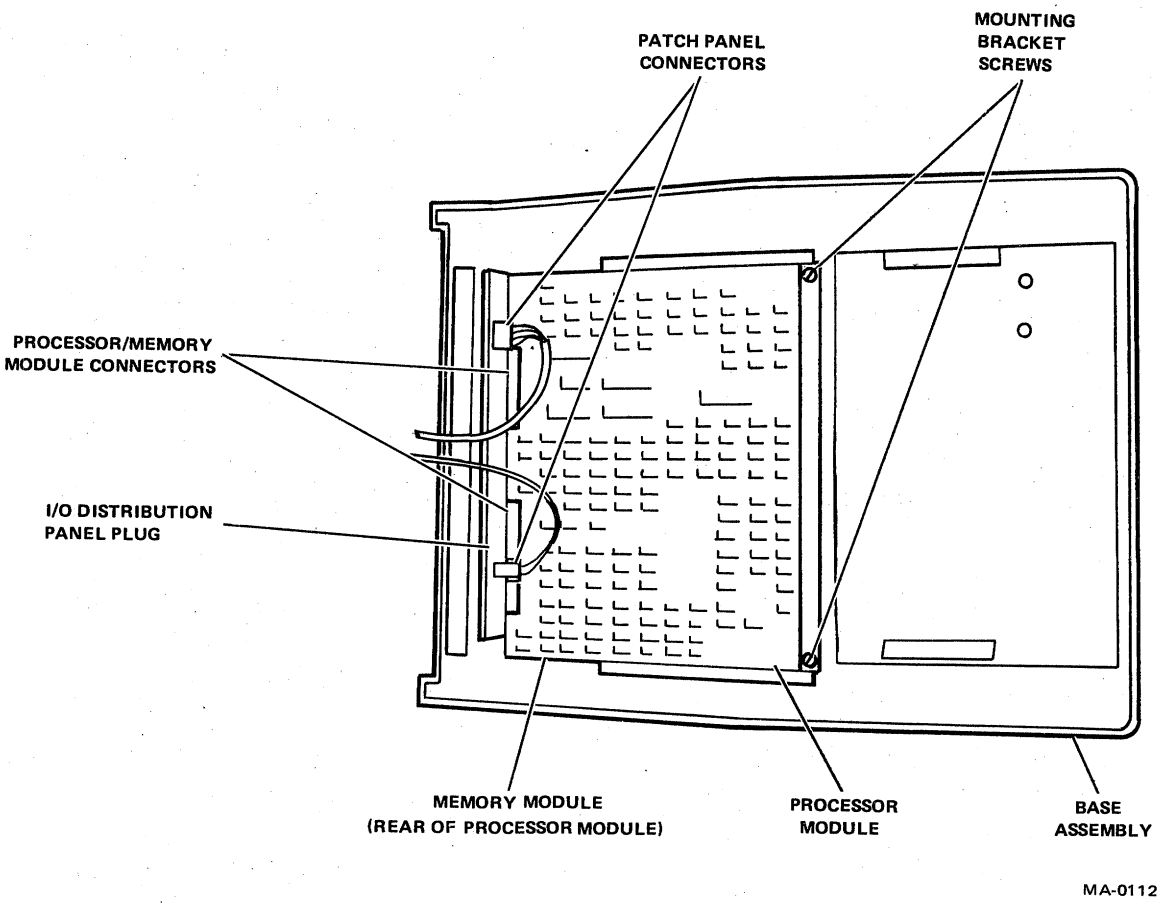


Figure 3-20 Processor/Memory Module Removal and Replacement

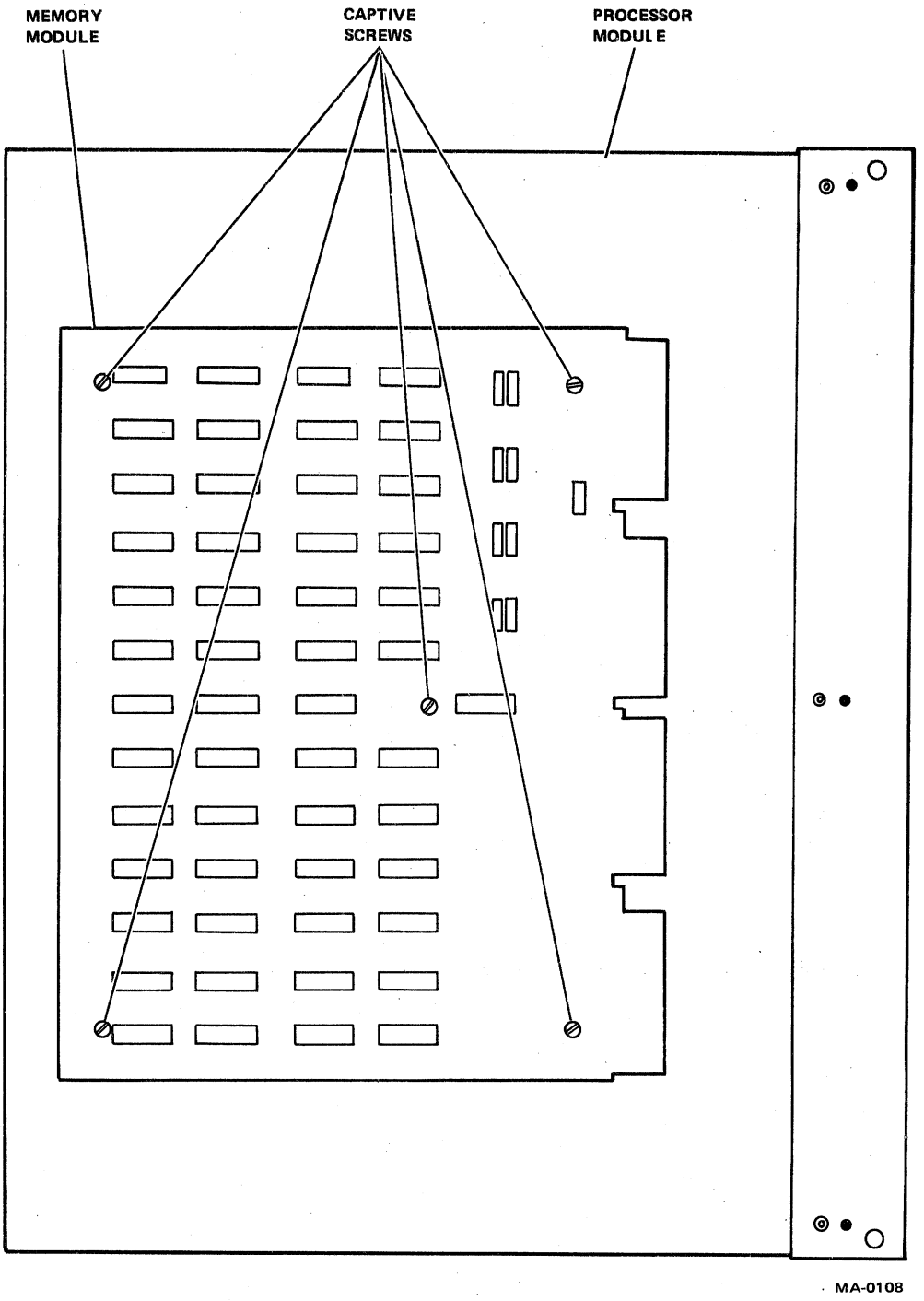


Figure 3-21 Memory Board Removal and Replacement

3.3.3 I/O Distribution Panel (Figure 3-22)

1. Remove the base assembly as described in Paragraph 3.3.1.
2. Remove the processor/memory module as described in Paragraph 3.3.2.
3. If the terminal is equipped with an MR78 program loading device, loosen the two screws securing the MR78 to the option panel and remove the unit.
4. Remove the two option panel plugs (if not already removed in Paragraph 3.3.1).
5. Remove all of the connector screws shown in Figure 3-22. (There are five option panel connectors.)
6. Reverse steps 1 through 5 to replace the option panel assembly.

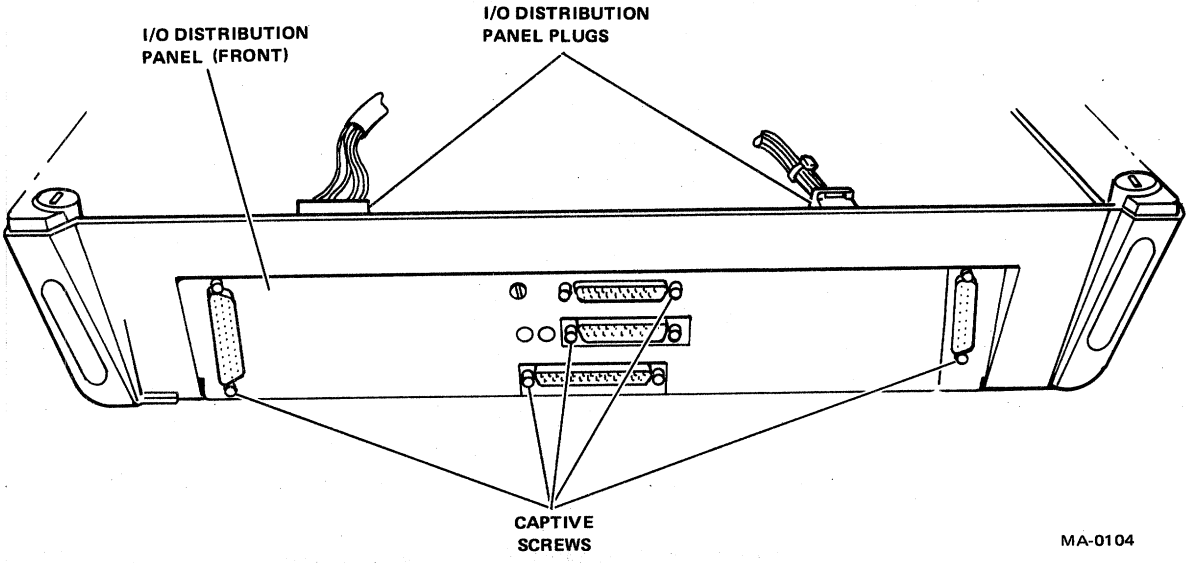


Figure 3-22 Option Panel Removal and Replacement

3.3.4 RUT and DP Modules

NOTE

The RUT and DP modules must be removed and replaced as a unit; they should not be separated until they have been removed from the terminal.

1. Remove the base assembly as described in Paragraph 3.3.1.
2. Remove the two plastic cable ties.
3. Remove the aluminum standoff.
4. Disconnect the monitor, keyboard, video interface, and power connectors.

5. Unscrew the nine small plastic wing nuts.

6. Lift the RUT and DP modules from the terminal.

7. To separate the RUT and DP modules, disconnect J1 and J2 by pulling the modules apart.

8. If the character generator is to be removed from the DP module, unplug the assembly. (The character generator is secured to the DP module by its connectors.)

9. To replace the RUT and DP modules, reverse steps 1 through 8.

CAUTION

When replacing the RUT and DP modules, make sure that connectors are aligned properly before applying pressure. Observe that color-coded wires on both sides of the connectors match and, where indicated, pin 1 is located at the extreme left of the connector as shown in Figure 3-23. If the character generator has been removed, make sure the arrow on the assembly points to the rear of the unit.

3.3.5 Power Supply Assembly

WARNING

There are high voltages present in the power supply. Make sure that the terminal line cord is not plugged into a source of power when servicing, removing, or replacing power supply assemblies or components. Using a screw driver or clip lead, discharge the filter capacitors by shorting the capacitors to the assembly chassis or any suitable ground. Make sure ground connection is made first before discharging the capacitors.

1. Remove the base assembly as described in Paragraph 3.3.1.

2. Remove the RUT and DP modules as described in Paragraph 3.3.4.

3. Remove the three captive screws securing the rear cover and remove the cover (Figure 3-24).

4. Remove the ground leads (Figure 3-25).

5. Disconnect and remove the cable connecting the monitor and power supply boards.

6. Loosen the captive screw until the latch is free enough to be rotated out of its socket.

7. Pull the assembly outward and slightly downward to disengage the catches in the bottom rear of the assembly. Lift the assembly free of the chassis.

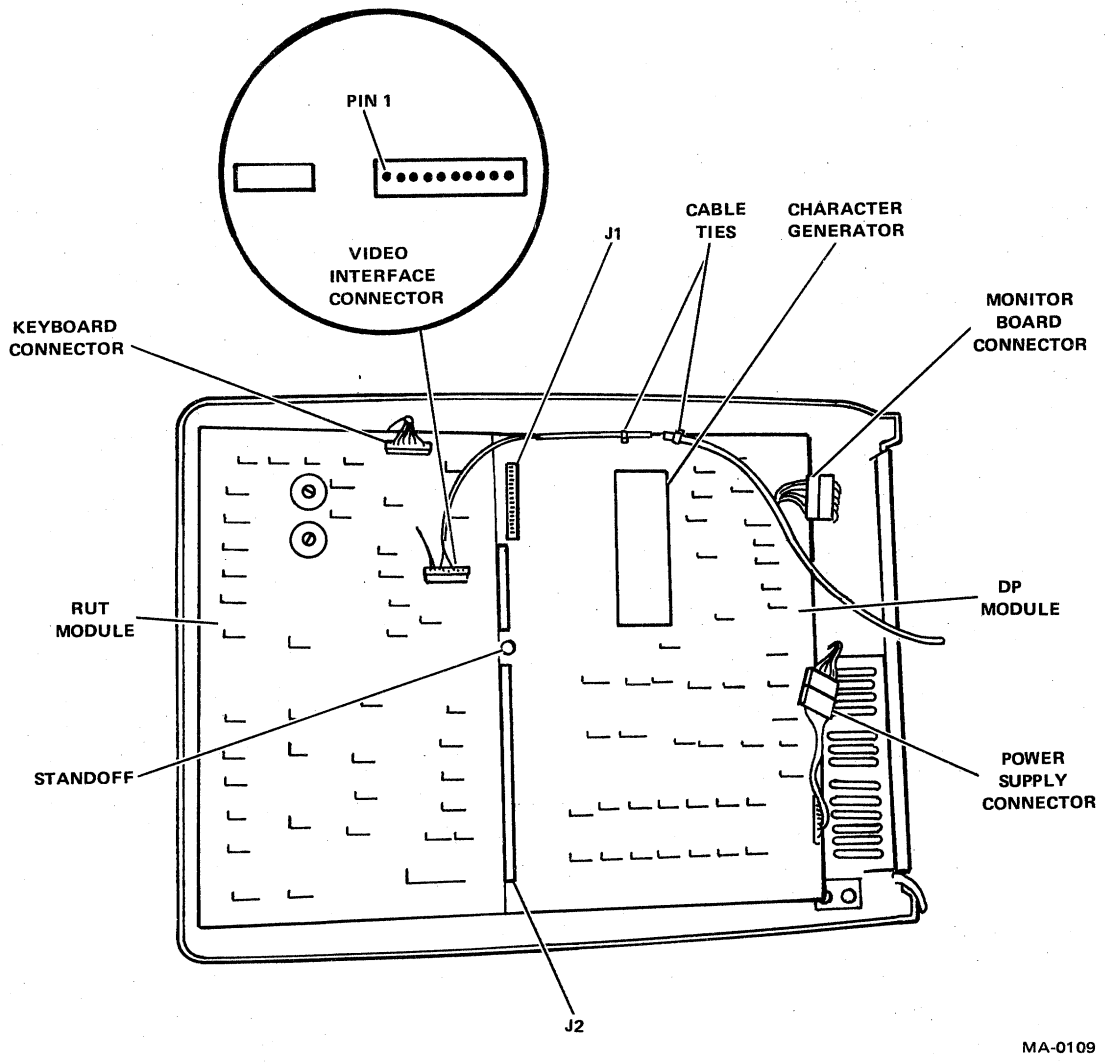


Figure 3-23 RUT and DP Module Removal and Replacement

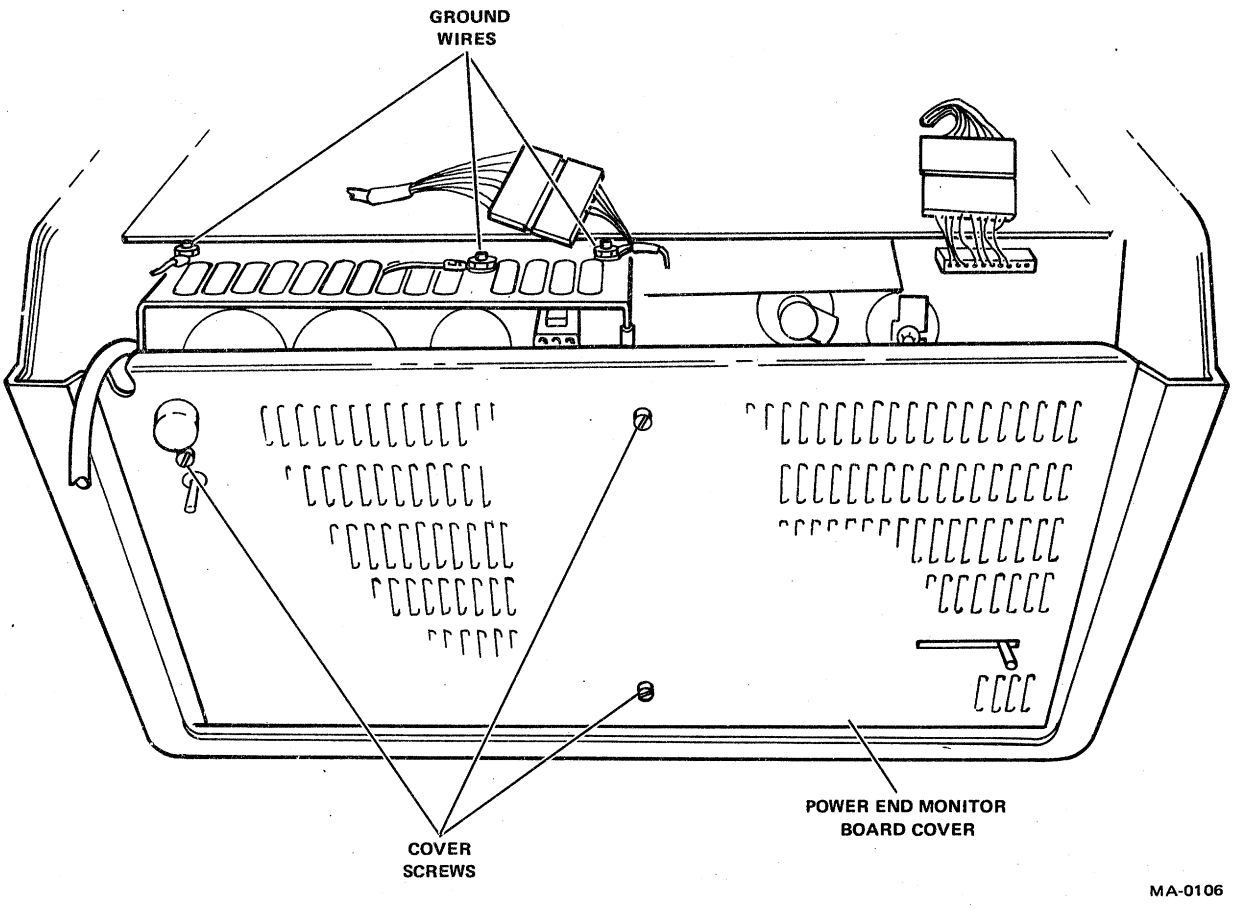


Figure 3-24 Power Supply and Monitor Board Cover Removal and Replacement

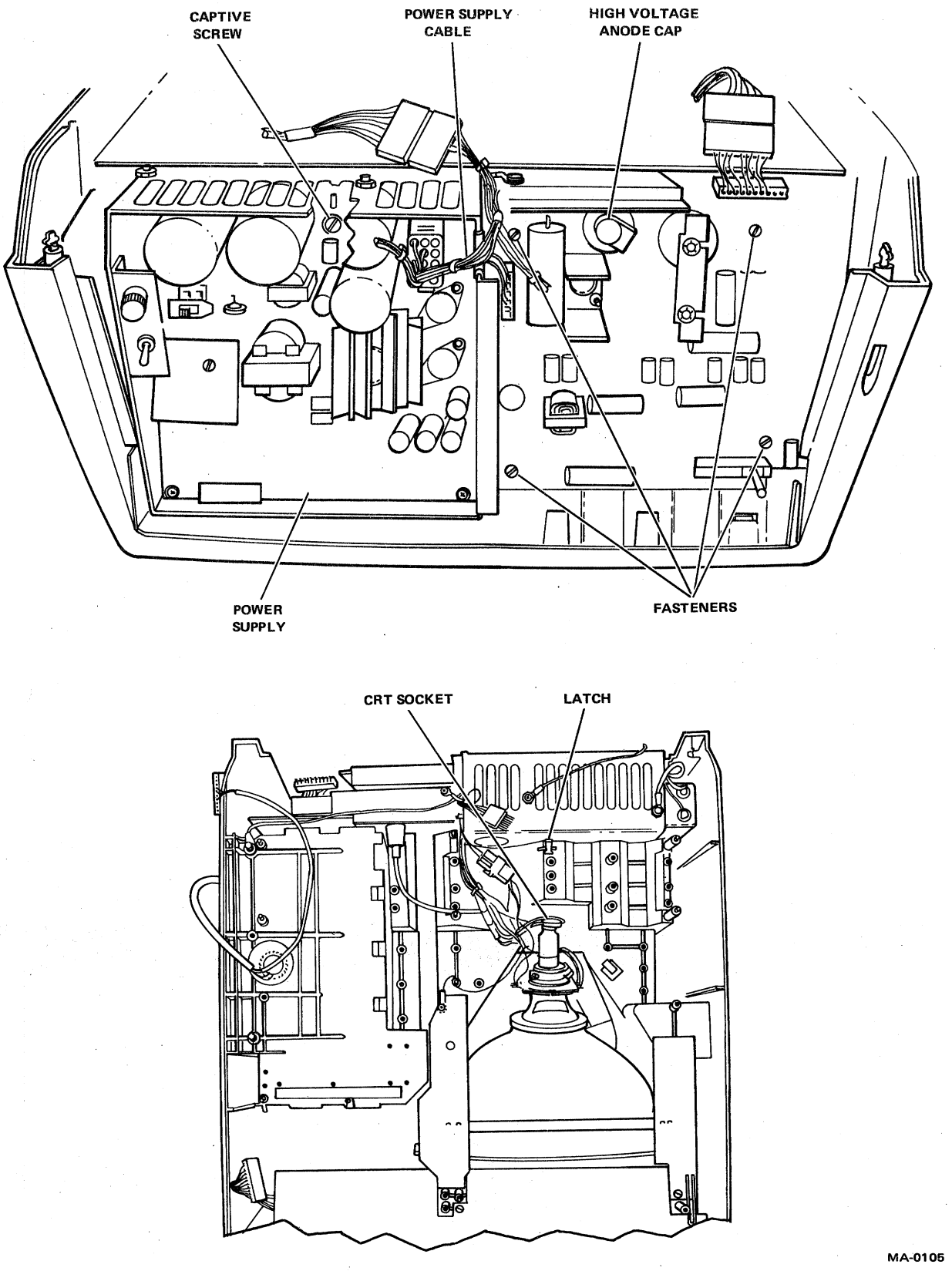


Figure 3-25 Power Supply and Monitor Board Removal and Replacement

3.3.6 Monitor Board

1. Remove the base assembly as described in Paragraph 3.3.1.
2. Remove the RUT and DP modules as described in Paragraph 3.3.4.
3. Remove the power supply board as described in Paragraph 3.3.5.

WARNING

There are high voltages present in the power supply and near the CRT. Make sure the terminal power line is unplugged and the CRT and capacitors shown in Figure 3-3 are discharged before handling the high voltage anode clip and the CRT.

4. Remove the high voltage anode cap (Figure 3-25).
5. Press the tabs on the high voltage lead connector and withdraw the lead through the rear of the assembly.
6. Remove the CRT socket.
7. Unscrew the clamp securing the yoke assembly and remove the yoke.
8. Remove the four screws securing the monitor board to the chassis and remove the board from the terminal.
9. Reverse steps 1 through 8 to replace the power supply assembly.

CAUTION

When replacing the power supply cover, make sure that the wiring is positioned so that it is not pinched between the cover and the power supply assembly chassis.

3.3.7 Keyboard Assembly (Figure 3-26)

1. Remove the base assembly as described in Paragraph 3.3.1.
2. Remove the RUT and DP modules as described in Paragraph 3.3.4.
3. Remove the six screws securing the keyboard assembly to the terminal and remove the assembly.
4. Reverse steps 1 through 3 to replace the keyboard.

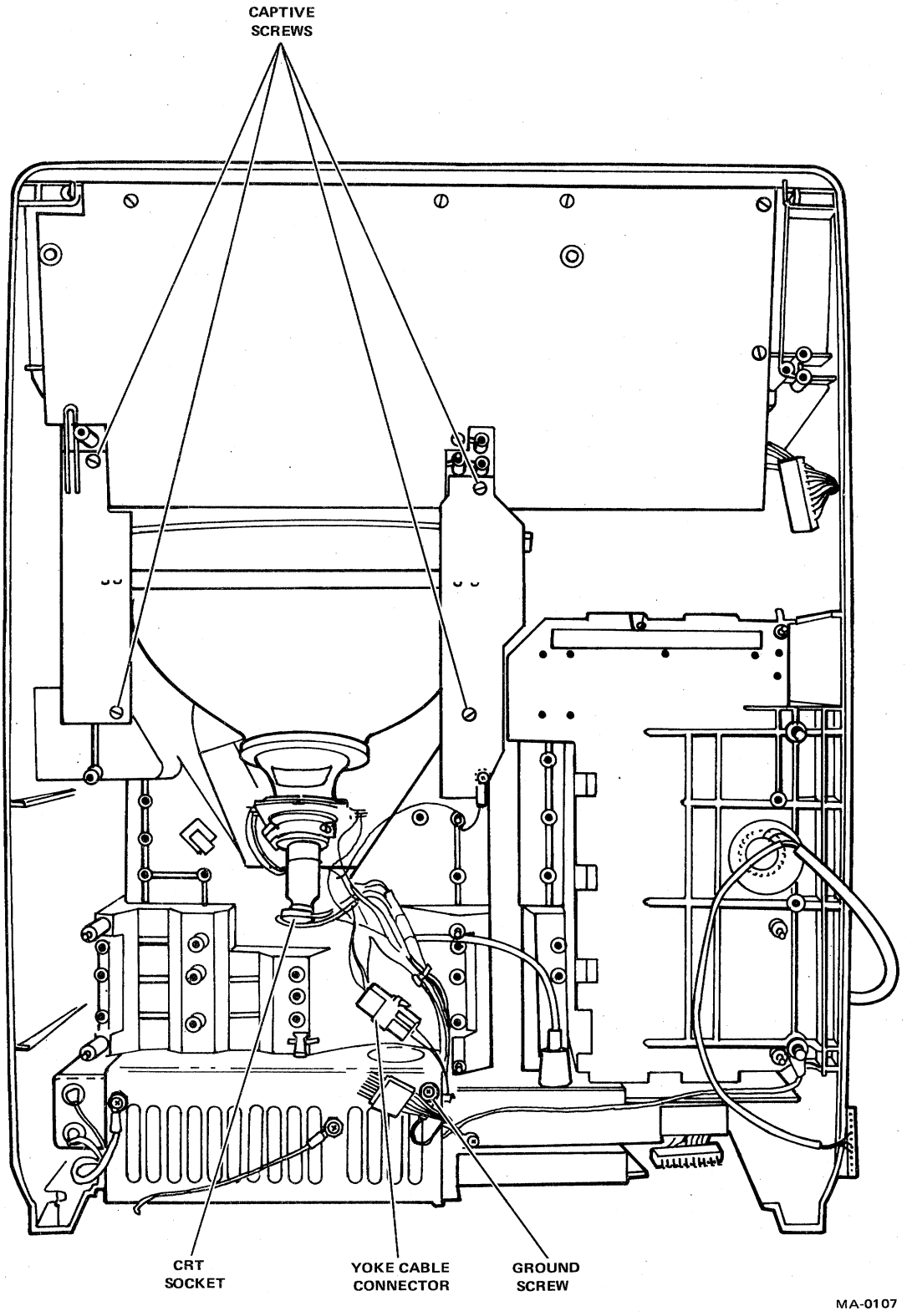


Figure 3-26 Keyboard Assembly Removal and Replacement

3.3.8 CRT Assembly (Figure 3-27)

WARNING

There are high voltages present in the power supply and near the CRT. Make sure the terminal power line is unplugged and the CRT and capacitors shown in Figure 3-3 are discharged before handling the high voltage anode clip and the CRT. Use care when handling the CRT. The CRT is an evacuated device and could shatter if broken.

1. Remove the base assembly as described in Paragraph 3.3.1.
2. Remove the RUT and DP modules as described in Paragraph 3.3.4.
3. Remove the keyboard assembly as described in Paragraph 3.3.7.
4. Unclip the connectors from the yoke assembly.
5. Remove the ground lead.
6. Remove the four captive screws securing the CRT assembly to the terminal.
7. Remove the plastic spacers before removing the CRT. Make sure that these spacers are replaced when reinserting the CRT assembly.
8. Slide the CRT out of the terminal.
9. Reverse steps 1 through 8 to replace the CRT assembly.

NOTE

Normally there are no adjustments required after the initial manufacturing and alignment of the unit. However, after replacing the CRT or deflection yoke, the display must be realigned and adjusted as directed in Paragraph 3.4.

3.4 ALIGNMENT AND ADJUSTMENT PROCEDURES

3.4.1 Video Display Adjustments

NOTE

Normally no terminal adjustments are required after the initial manufacturing checkout and alignment of the unit (except for the intensity control). However, after replacing a CRT or deflection yoke, the display must be realigned and adjusted. All adjustments are located on the power supply/monitor boards. Set the terminal to off-line operation and fill the screen with characters before making any adjustments. Alignment and adjustment controls are shown in Figure 3-28.

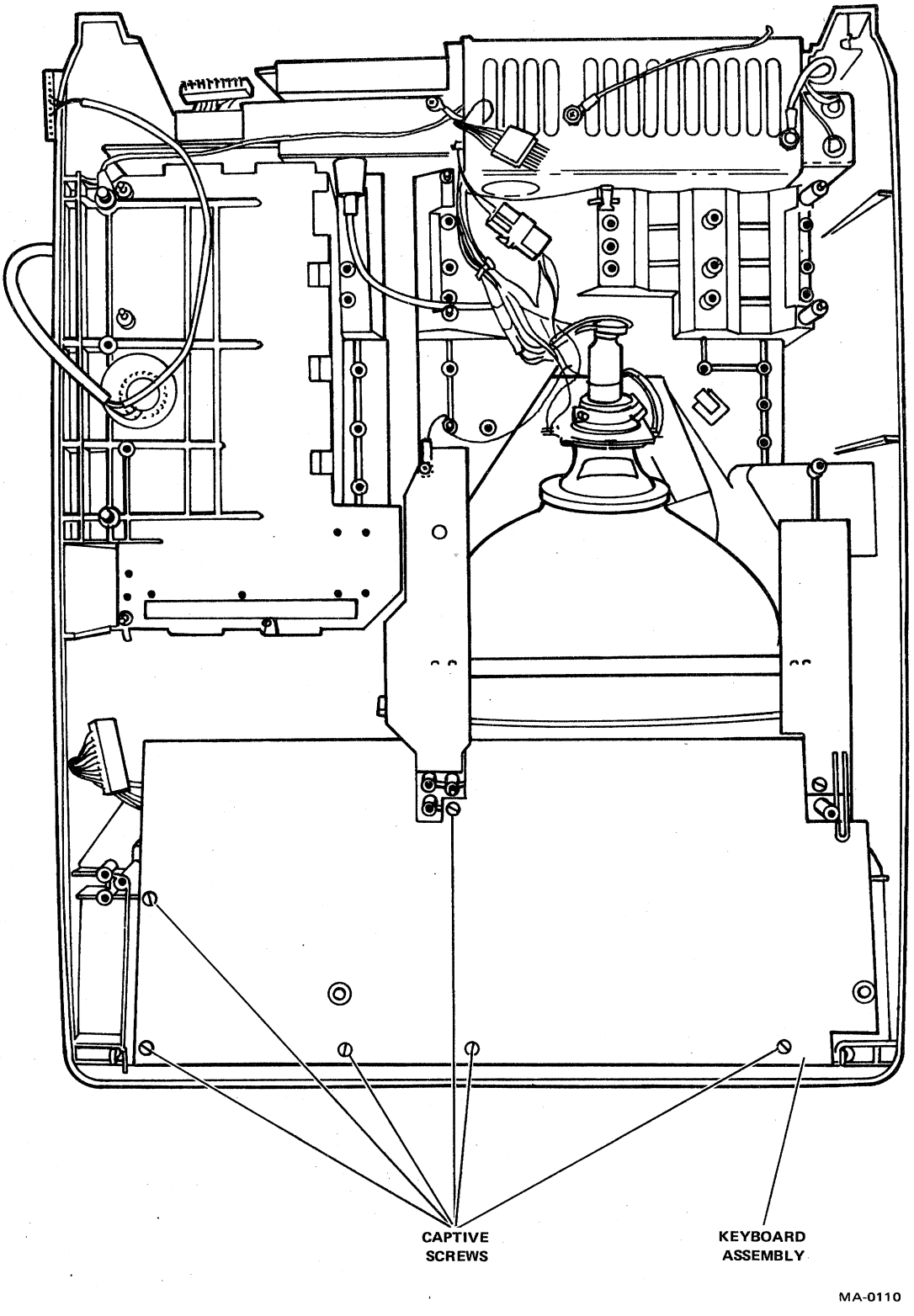


Figure 3-27 CRT Assembly Removal and Replacement

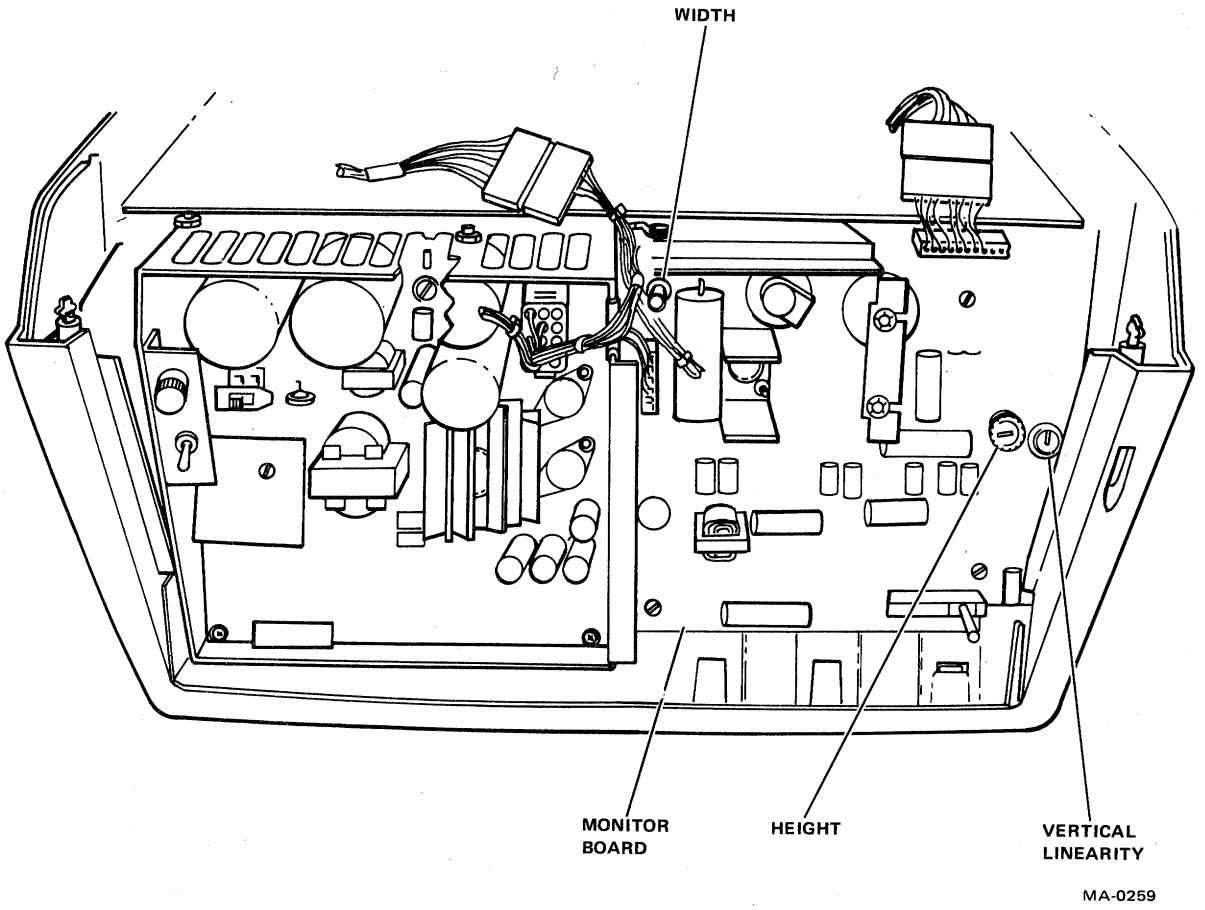


Figure 3-28 Alignment Control Adjustment Locations

3.4.1.1 Height – Adjust the vertical-size potentiometer until the height of the display is 114 mm (4.5 in). This measurement is from the upper edge of the top character line to the lower edge of the bottom character line (Figure 3-28).

3.4.1.2 Width – Using a nonconductive, hexagonal tipped alignment tool, adjust the iron slug in the width coil until the width of the display measures 218 mm (8.6 in) (Figure 3-28).

3.4.1.3 Vertical Linearity – Adjust the vertical linearity potentiometer until the characters displayed on the top line are the same size as the characters displayed on the bottom line (Figure 3-28).

3.4.1.4 Focus – Adjust the focus potentiometer until characters in all sections of the screen are sharp and clear. Refer to Figure 3-28.

3.4.1.5 Processor Board DC OK Adjustment – To adjust the DC OK potentiometer, perform these steps:

1. Use a DVM measure Vcc (approximately +5.0 V) across E138 pins 7 and 14 (Figure 3-29).
2. Subtract 4.74 V from the Vcc measured in step 1.
3. Divide the difference by two.
4. Monitoring the voltage between pins 8 (+) and 9 (-) of E148, adjust the potentiometer (Figure 3-29), until the DVM indicates the value calculated in step 3.

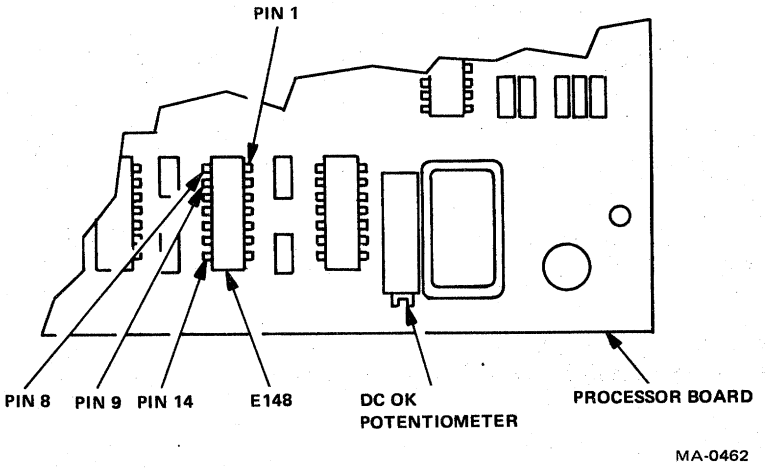


Figure 3-29 DC OK Adjustment Location

APPENDIX A
SYSTEM CHARACTERISTICS

A.1 PHYSICAL

Height	14.4 in (36.6 cm)
Width	20.9 in (53.1 cm)
Depth	27.2 in (69.1 cm)
Weight	42 lb (19.1 kg)

A.2 FUNCTIONAL

Central Processor:

Word length	12 bits
Cycle time	2.96 (3.55) μs
Memory	16,384 words NMOS R/W RAM; internal CMOS ROM for system control.

Video Terminal:

Screen format	24 lines by 80 characters
Keyboard	Standard typewriter format with auxiliary numeric keypad
Character set	Full 96 ASCII plus 32 special graphics.
Character matrix	7x7 dot matrix; direct cursor addressing.

Environmental:

Temperature	10° C through 40° C (50° F through 104° F)
Relative humidity	10% to 90%
Maximum wet bulb	28° C (82° F)
Minimum dew point	2° C (36° F)
Line voltage	95 V through 127 V or 190 through 254 V
Line frequency	47 Hz through 63 Hz

APPENDIX B
MR78 PROGRAM LOADER

B.1 GENERAL

The MR78 program loader (Figure B-1) is an optional device which plugs into the MR78 connector on the I/O distribution panel located at the rear of the VT78 terminal. Its function is to provide a convenient means of loading programs (in pseudo papertape format) into main memory via the MR78 interface circuit described in Paragraph 2.2.1.6.

When the VT78 terminal START switch is pressed (assuming that the system has been powered-up properly), panel memory (described in Paragraph 2.2.1.3) will check for the existence of the MR78 device. If the device is present, its program will be loaded into main memory. If the device is not present, panel memory will check the RX78 floppy disk drive system for an alternate source of programming information.

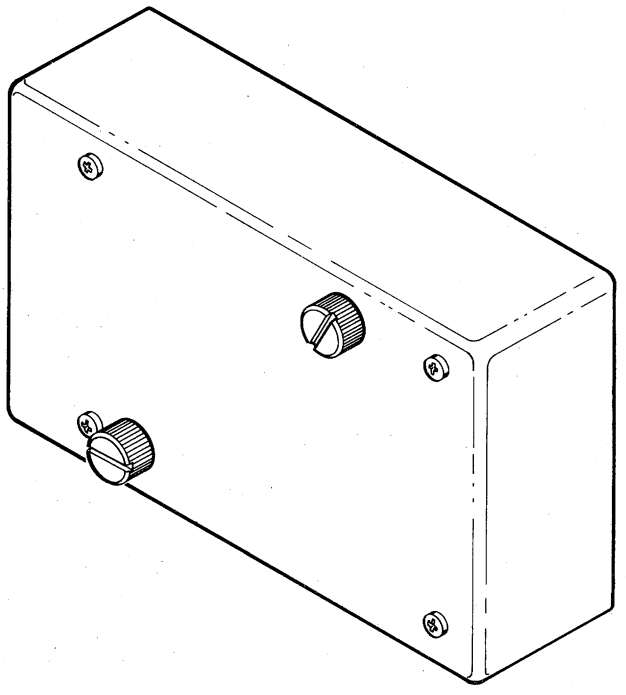


Figure B-1 MR78 Program Loader

B.2 THEORY OF OPERATION (Figure B-2)

The presence of the MR78 is acknowledged when the device is plugged into the VT78 terminal grounding PI BD L. This maintains CHARACTER RDY low. When the GET CHARACTER flag is set, GET CHARACTER will also go low, clocking the 16-bit counter.

The 16-bit counter consists of four, 4-bit binary counters. The first 10 bits (ADDR 0 through ADDR 9) serve as the address for the words stored in the ROM chips. The following three bits are decoded by a 3-to-8 line decoder to select the order in which the ROMs will be read. The switching network minimizes power consumption by switching Vcc to select the ROMs.

There are 16 ROM chips in the MR78. Each ROM is a 4096-bit read-only memory organized as 1024 words by 4 bits. The enable inputs are both maintained at ground. The outputs correspond to the data programmed in the selected word which is, in turn, selected using the 10 address inputs.

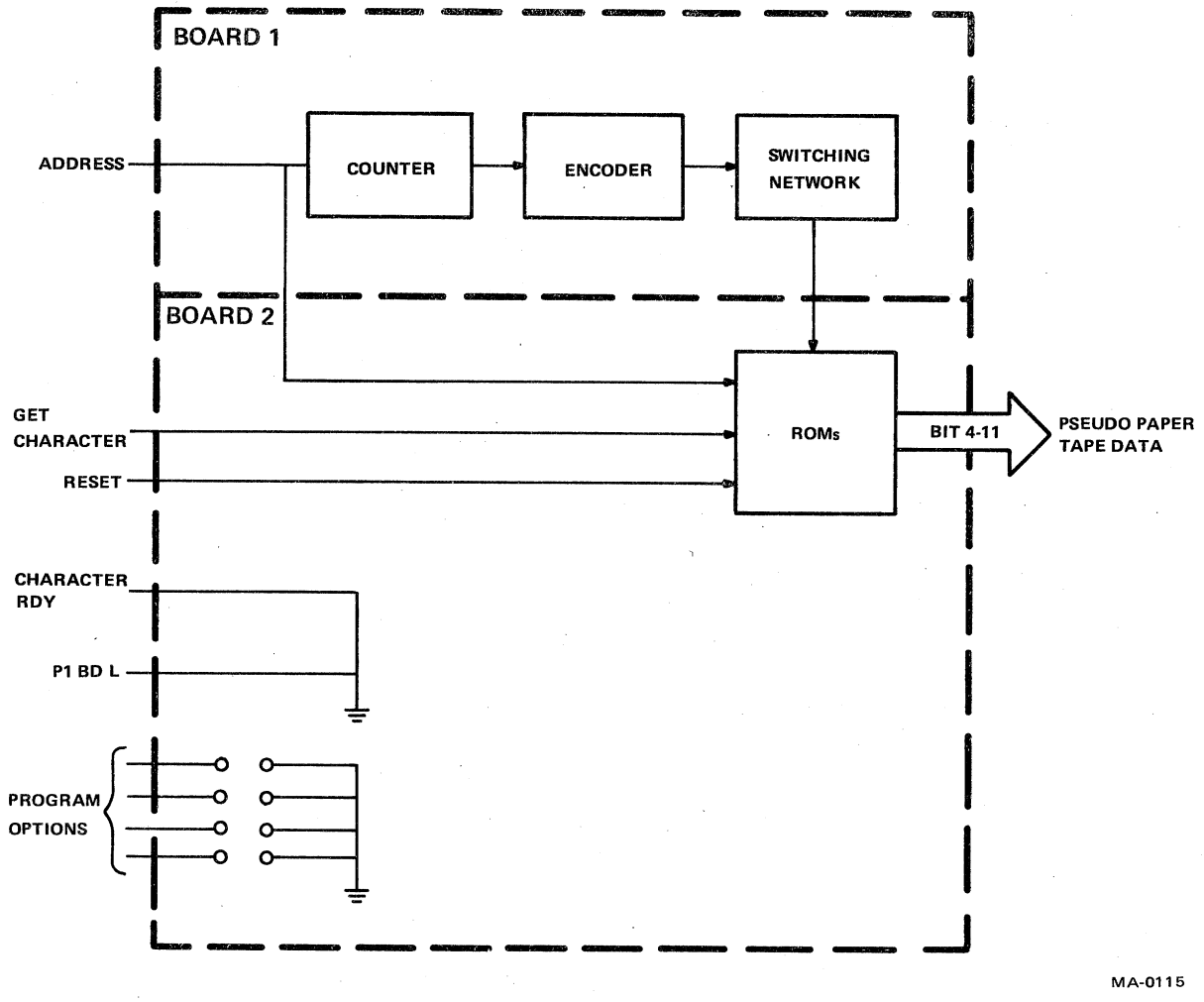


Figure B-2 MR78 Program Loader Block Diagram

The ROMs are read in pairs providing 8-bit words. Each bit corresponds to a hole as in papertape format; i.e., leader (200) followed by data/field origin statements, followed by 12-bit checksum, followed by trailer (200) statements. Field statements are identified by holes 8 and 7 (3X0, where X = field); origin statements have hole 7 only (1YY, where YY is the first two octal digits of address followed by a second character which contains the last two digits). Data statements have neither hole 7 nor 8.

Three jumpers are available which can be inserted to set corresponding interface lines to define the number of programs to be loaded into main memory before reading is terminated and the program is started. The jumper connections and the corresponding number of programs to be loaded are listed in Table B-1.

Table B-1 Program Selection Jumper Configurations

Jumpers			Programs Loaded
W1	**W2**	**W3**	
OUT	OUT	OUT	1
OUT	OUT	IN	2
OUT	IN	OUT	3
OUT	IN	IN	4
IN	OUT	OUT	5
IN	OUT	IN	6
IN	IN	OUT	7
IN	IN	IN	8

APPENDIX C
I/O DISTRIBUTION PANEL PIN ASSIGNMENTS

There are nine connectors interfacing the processor and memory modules with the keyboard/video display and the outside world. These are located on the I/O distribution panel. Figure C1 shows the cabling connnections. Refer to Table C-1 for individual I/O distribution panel connector pin assignments.

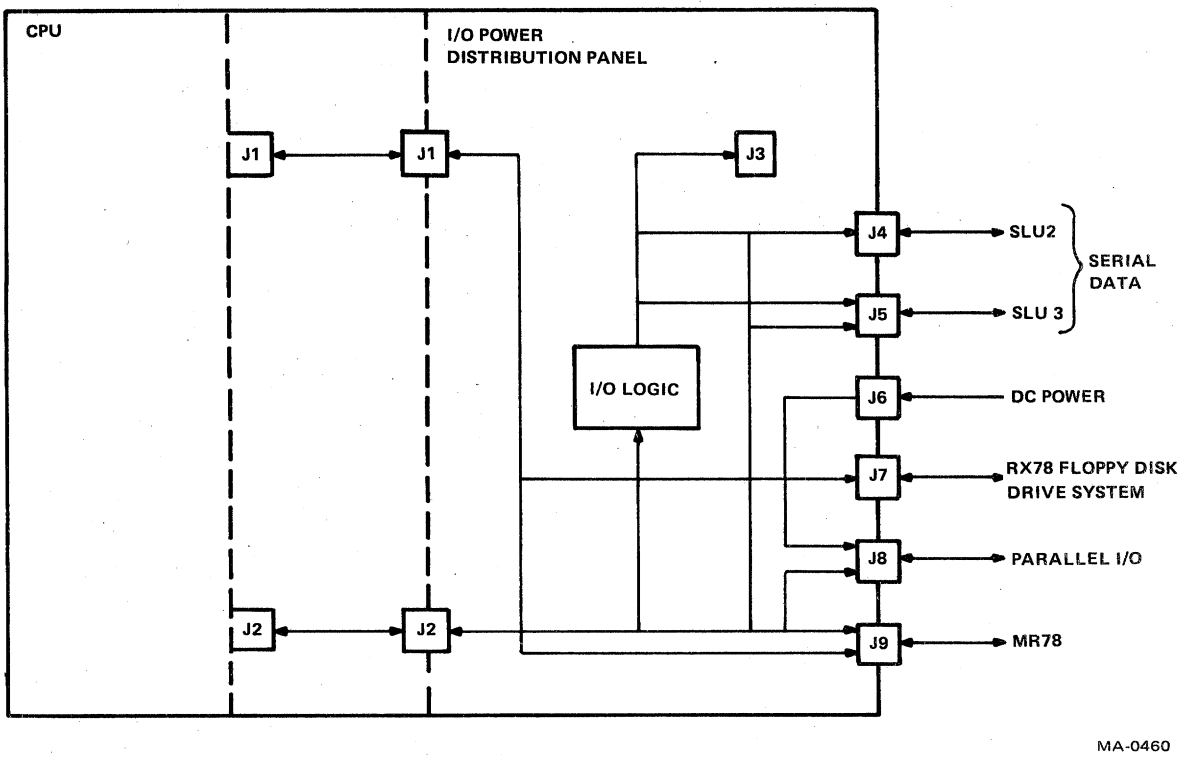


Figure C-1 I/O Distribution Panel Cabling Diagram

Table C-1 I/O Distribution Panel Pin Assignments

Connector	Pin	Mating Connector	Signal	Electrical Characteristics
J3		J1,J2	Normally open start switch.	60 mA @ .4 V (when pressed).
	1	2-4		
	2	2-5	Normally closed start switch.	60 mA @ .4 V (when not pressed.
	3	2-13	SLU1 transmitted data.	TTL output.
	4	2-17	SLU1 received.	1 TTL load.
	5		Ground.	
	6		Ground.	
	7		*	Chassis ground.
J4	1		Ground.	
	2	2-14	SLU2 transmitted data.	Mark = -3 V or more.
	3	2-18	SLU2 received data.	Same as above.
	4		Request to send.	Always > +3 V.
	7		Ground.	
	20		Data terminal ready.	Always > +3 V.
J5	1		Ground.	
	2	2-15	SLU3 transmitted data.	Mark = -3 V or more. Space = +3 V or more.
	3	2-19	SLU3 received data.	Same as above.
	7		Ground.	
	11	2-21	APT EN L	Normally left open-circuited. Grounding this line causes bit 1 of the AC to set when a LAS or OSR instruction is encountered in the program. (Bit 1 is the "APT" bit and causes early termination of the CPU diagnostic followed by a jump to the MR78 loader. Load is 4.7k + 1 TTL input.)

*These signals are loaded with 180 Ω to +5 V and 390 Ω to ground in addition to the load specified. Tri-state drivers sink 16 mA @ 0.4 V, source 5.3 mA @ 2.4 V.

Table C-1 I/O Distribution Panel Pin Assignments (Cont)

Connector	Pin	Mating Connector	Signal	Electrical Characteristics
	18	2-20	FE3	High if SLU3 receiver indicates a framing error. Framing errors are caused when a "break" is sent to the processor by APT.
	25	2-22	APTRST H	Driven by J5-18 when running under APT. When driven high, causes the PWR OK comparator to simulate a DC LOW condition. Hence the processor behaves as though it were just turned on.
J7		1-19	Ground.	
	20	1-35	RUN L	*1 TTL input.
	21	1-40	ERROR L	*1 TTL input.
	22	1-34	INITIL	Tristate output.
	23	1-37	XFR RQST L	*1 TTL input/open collector output.
	24	1-39	DONE K	*1 TTL input.
	25	1-45	DATA L	*1 TTL input.
	26	1-33	12 BIT 1 L	Tri-state output.
	27	1-41	SHIFT L	*1 TTL input.
	28	1-38	OUT L	Open collector driver plus*.
	29	1-36	RUN 1 L	*1 TTL input.
	30	1-42	ERROR 1 L	*1 TTL input.
	31	1-43	INIT L	Tri-state output.
	32	1-46	XFR RQST 1 L	*1 TTL input/open collector out.
	33	1-45	DONE 1 L	*1 TTL input.

*These signals are loaded with 180 Ω to +5 V and 390 Ω to ground in addition to the load specified. Tri-state drivers sink 16 mA @ 0.4 V, source 5.3 mA @ 2.4 V.

Table C-1 I/O Distribution Panel Pin Assignments (Cont)

Connector	Pin	Mating Connector	Signal	Electrical Characteristics
	34	1-47	DATA 1 L	*1 TTL input.
	35	1-44	12 BIT L	Tri-state output.
	36	1-40	SHIFT 1 L	*1 TTL input.
	37	1-35	OUT 1 L	Open collector driver plus*.
J8	1		+12 V	No more than 150 mA.
	2		-12 V	No more than 150 mA.
	3		+5 V	No more than 0.5 A.
	4		Ground.	
	5	2-23	PAPER STROBE.	****
	6		Ground.	
	7	2-24	CARRIAGE STROBE	****
	8		Ground.	
	9	2-25	CHARACTER STROBE	****
	10		Ground.	
	11	2-26	RESTORE.	****
	12		Ground.	
	13	2-27	CHECK L	*****
	14		Ground.	
	15	2-28	PAPER RDY L	*****
	16		Ground.	
	17	2-29	CARRIAGE RDY L	*****
	18	2-30	CHARACTER RDY L	*****
	19		Ground.	
	20	2-31	PRINTER RDY L	*****

All signals marked "" are loaded with 180 Ω to +5 V and 390 Ω to ground in addition to the load specified. Tri-state drivers sink 16 mA @ 0.4 V, source 5.3 mA @ 2.4 V.

****Tri-state driver sinks 32 mA @ 0.4 V.

*****High threshold bus receiver plus 180 Ω to +5 V and 390 Ω to ground.

Table C-1 I/O Distribution Panel Pin Assignments (Cont)

Connector	Pin	Mating Connector	Signal	Electrical Characteristics
	21		Ground.	
	22	2-32	LA/LQP (L/H)	Driver must sink 15 mA.
	23	2-33	LIFT RIBBON	Tri-state driver.
	24		Ground.	
	25		Ground.	
	26	2-35	DATA BIT 0 (msb)	******
	27		Ground.	
	28	2-36	DATA BIT 1	******
	29		Ground.	
	30	2-37	DATA BIT 2	******
	31		Ground.	
	32	2-38	DATA BIT 3	******
	33		Ground.	
	34	2-34	IN/OUT	Driver must sink 2 mA.
	35	2-39	DATA BIT 4	******
	36		Ground.	
	37	2-40	DATA BIT 5	******
	38		Ground.	
	39	2-41	DATA BIT 6	******
	40		Ground.	
	41	2-42	DATA BIT 7	******
	42		Ground.	
	43	2-43	DATA BIT 8	******
	44		Ground.	

******With no connection made to the line "OUT": tri-state driver is defined under "*." With line "OUT" grounded: one TTL input.

Table C-1 I/O Distribution Panel Pin Assignments (Cont)

Connector	Pin	Mating Connector	Signal	Electrical Characteristics
	45	2-44	DATA BIT 9	******
	46		Ground.	
	47	2-45	DATA BIT 10	******
	48		Ground.	
	49	2-46	DATA BIT 11	******
	50		Ground.	
J9	1-3		+5 V	No more than 100 mA.
	4-7		Ground.	
	9	1-32	PO	**
	10	1-31	P1	**
	11	1-30	P2	**
	12	1-29	RESET	***
	13	2-1	MM	**with 15k pullup.
	14	1-9	HOLE 5	**with 15k pullup.
	15	1-10	HOLE 4	**
	16	1-15	HOLE 6	**with 15k pullup.
	17	1-16	HOLE 1	***
	18	1-17	HOLE 3	**
	19	1-18	HOLE 2	**with 15k pullup.
	20	1-21	CHAR READY L	**
	21	1-23	HOLE 7	**
	22	1-24	GET CHAR L	**
	23	1-26	P1 BD L	**
	24	1-27	HOLE 8	**
	25	1-28	READ EN H	**

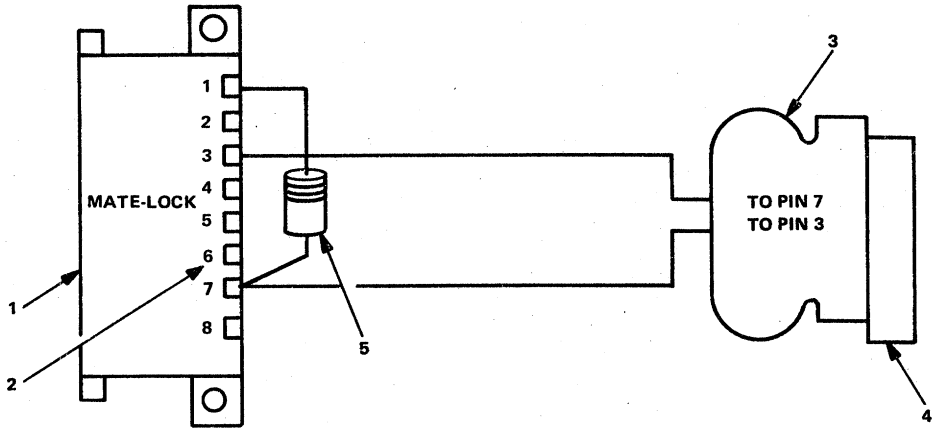
**TTL input.

***TTL output.

******With no connection made to the line "OUT": tri-state driver is defined under "*." With line "OUT" grounded: one TTL input.

APPENDIX D
PRS01 CABLE

Detailed PRS01 cable fabrication information is shown in Figure D-1.



PARTS LIST

ITEM	DIGITAL PART NUMBER
1	12-09340
2	12-09379
3	12-05886
4	12-05885
5	13-00295 (330Ω ¼ω)

MA-0461

Figure D-1 PRS01 Cable

APPENDIX E
APT AUTOMATIC TEST SYSTEM CONNECTIONS

Three normally unused pins on the SLU3 connector are used to implement automatic testing of the VT78 using the APT system (Refer to Table 1-1). These are:

Pin 11 Normally open, grounded by the APT system to indicate that the VT78 is under APT control.

Pin 18 Connected to the framing error output of the UART handling SLU3.

Pin 25 Connected to pin 18 by the special APT connector causing the framing error signal, produced when APT attempts to gain control of the system under test, to initiate a RESET operation within the VT78. This reset condition is similar to that following power-on but the presence of the APT EN bit in the status word (pin 11) causes the built-in diagnostics to load the APT protocol from the special APT MR78 rather than proceed with the full system diagnostic test.

Using the APT interface signals on the SLU3 connector, the APT computer can gain control of the VT78, regardless of the state of the machine, and initiate loading of diagnostics via SLU3.

APPENDIX F
FIELD REPLACEABLE UNITS (REPAIRS)

Unit	Part Number
Processor Module	54-12660
Memory Module	54-12691
I/O Distribution Panel	54-12861
Power Supply Assembly	H7832
Monitor Board	54-11444-01
DP Module	54-11745
RUT Module	54-11743
Character Generator	54-11815
Keyboard Assembly	54-11170-4
CRT Assembly	70-10859
18 in. RX78-to-VT78 Cable	BC80D-1H
5 ft RX78-to-VT78 Cable	BC80D-5K
Two RX78s-to-VT78 Cable	BC80E-

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