

DISCFILE CONTROL  
TYPE 270  
INSTRUCTION MANUAL

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BS-D-270-0-AD	Accumulator and Bit-Control Logic . . . . .
BS-D-270-0-CM	Command Logic . . . . .
BS-D-270-0-FC	File-Control Logic . . . . .
BS-D-270-0-SC	Status Logic . . . . .
BS-D-270-0-TR	Transmitters, Receivers, and Data Clock Logic . . . . .
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## Circuit Schematics (continued)

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RS-B-R181	DC Carry Chain . . . . .
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RS-B-R202	Dual Flip-flop . . . . .
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RS-B-R603	Pulse Amplifier . . . . .
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RS-B-W100	Emitter Follower . . . . .
RS-B-W101	IO Bus Driver . . . . .
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## CHANGES TO DISCFILE CONTROL 270 INSTRUCTION MANUAL

(Notation: "Line 5-B" means 5th line from bottom of page.)

<u>No.</u>	<u>Page</u>	<u>Line</u>	<u>Correction</u>		
1)	viii	5-B	change page 6-9 to page 6-4		
2)	3-4	3-B	~SEL 5 (-SC:B7)		
3)	3-5	4	~SEL 5 level		
4)	3-5	---	(The following entry should be inserted in Table 3-2 between the SELECT entry and the ALERT entry:  <table style="margin-left: 40px; border: none;"> <tr> <td style="padding-right: 40px;">ADDRESS TERMINATION (-TR:A1)</td> <td>Notifies the discfile that the address trans- mission has been com- pleted.</td> </tr> </table>	ADDRESS TERMINATION (-TR:A1)	Notifies the discfile that the address trans- mission has been com- pleted.
ADDRESS TERMINATION (-TR:A1)	Notifies the discfile that the address trans- mission has been com- pleted.				
5)	3-11	10	The ATP pulse steps the octoflop to its third state ADT (Address Terminated) and sends an ADDRESS TERMINATION pulse to the discfile. During the address ... etc.  <u>(Items Below All in Chapter 8 Signal Glossary)</u>		
6)	1d		Insert between 3) and 4) the following:  <div style="margin-left: 40px;">3A) ADDRESS TERMINATION</div>		
	1d		Change 96 to read as follows:  <div style="margin-left: 40px;">96) WCT0-7</div>		
7)	5		Renumber page 5, "5a" and insert page 5b (attached) after page 5a.		
8)	12	7-B	the discfile. It is amplified, redesignated ADDRESS TERMINATION, and sent to the discfile approximately 15 $\mu$ sec after the transmission of the parity bit, the final bit of the 21-bit address.		

Changes to Discfile Control 270 Instruction Manual - Page 2

<u>No.</u>	<u>Page</u>	<u>Line</u>	<u>Correction</u>
9)	34	1-B	ALS state to CMS state, and triggers a 200- $\mu$ sec delay that ends with the generation of the NDP-1 pulse.
10)	90	1-B	The discfile control sends a TAKE A CHARACTER pulse to the Data Control 136.
11)			In general wherever "Take a Character" or "Give a Character" is encountered change to "TAKE A CHARACTER" or "GIVE A CHARACTER", respectively. (The reason for this is that all output pulses from the Discfile Control are for consistency capitalized throughout the manual.)
12)	106	1	<u>WCT0-7 - Word Counter (-WC:A3-7)</u>

(3A) ADDRESS TERMINATION (-TR:A1)

The ADDRESS TERMINATION pulse is sent to the discfile through the odd data 1's twisted-pair transmission line. It notifies the discfile that the address transmission has been completed.

Generated by-

ATP

The discfile control produces an ATP pulse to advance the file-control octoflop from SNA state to ADT state (see ATP below.) After being amplified by pulse amplifier D30, the ATP pulse is redesignated ADDRESS TERMINATION and sent to the discfile.

# CHAPTER 1

## INTRODUCTION

### 1.1 PURPOSE AND SCOPE

The purpose of this instruction manual is to aid personnel in the installation, operation, and maintenance of the DEC Discfile Control 270<sup>^</sup> (Figure 1-1).

### 1.2 MANUAL ORGANIZATION

Chapter 2, General Description, comprises a broad description of system application and specifications. Chapter 3 contains the theory of operation of the discfile control logic; this chapter is organized horizontally by areas of the system logic and presents a brief overall description of all major signals and circuits used in the discfile control. Chapter 3 is fully cross-referenced to the Chapter 8 signal glossary. Chapter 4, System Operating Sequences, adds a vertical time dimension to the theory of operation by presenting a step-by-step analysis of system function in the form of highly detailed micro-flow-charts that illustrate each of the four major operating sequences executed by the discfile control. Chapter 5, Maintenance, includes information useful for inspection, troubleshooting, and repair. Chapter 6, Installation, explains the procedures to be followed when first unpacking and installing the discfile control. Chapter 7, Programming, tabulates the coding of the various I/O instructions used with the discfile control, and gives a listing and brief explanation of several typical subroutines. Chapter 8 presents a complete signal

glossary for the discfile control, its inputs, and its outputs. Chapter 9 contains introductory information on DEC drawing conventions and all pertinent engineering drawings for this manual.

a Figures.

This manual includes four general classes of figures: engineering logic diagrams; flow diagrams; circuit schematics; and miscellaneous figures such as photographs, block diagrams, and module location diagrams. The complete system logic is shown in the seven engineering logic diagrams listed below. These seven drawings are included in Chapter 9.

ENGINEERING LOGIC DIAGRAMS

<u>Drawing Number</u>	<u>Title</u>
BS-D-270-0-AC	Accumulator, Shift Counter, and Address Clock Logic
BS-D-270-0-AD	Accumulator and Bit-Control Logic
BS-D-270-0-CM	Command Logic
BS-D-270-0-FC	File-Control Logic
BS-D-270-0-SC	Status Logic
BS-D-270-0-TR	Transmitters, Receivers, and Data Clock Logic
BS-D-270-0-WC	Word Counter Logic

All system operations are shown in the four flow diagrams listed below; these diagrams are located in Chapter 9.

## FLOW DIAGRAMS

<u>Drawing Number</u>	<u>Title</u>
FD-D-270-0-8	File-Control State Diagram
FD-D-270-0-FD (Sheet 1)	Address Transmission and Data-Output Flow Diagram
FD-D-270-0-FD (Sheet 2)	Data Clock Flow Diagram
FD-D-270-0-FD (Sheet 3)	Processor Instructions, Discfile Command Signals, and Error Indications Flow Diagram

Module location diagrams and circuit schematics for the 27 types of FLIP CHIP Modules that are used in the discfile control are also in Chapter 9.

At the date of issue of this manual, up-to-date engineering drawings are included in Chapter 9. If significant engineering changes occur, DEC customarily issues revised drawing sets to reflect the changes. If any discrepancy exists between the engineering drawings of this manual and a current set of engineering drawings, the current engineering drawing set is correct.

For quick reference, all engineering drawings within a given category (Logic Diagrams, Flow Diagrams, etc.) are arranged numerically. Furthermore, all circuit schematics of Chapter 9 are arranged in order of circuit type designation (e. g. Dual Flip-flop R202 precedes Triple Flip-flop R203).

### 1.3 USE OF MANUAL

This manual is intended to serve two purposes: instruction and reference. Chapters 3 and 4 on theory of operation are intended primarily for instruction. These chapters cover the major logical networks and operating sequences of the system in a systematic and detailed manner, but they are not organized for rapid reference. After being read, they rarely need be referred to again.

To avoid burdening the reader with unnecessary detail, the theory of operation chapters usually concentrate on the single circuit or operation being described. Peripheral description of detailed signal generation conditions and additional uses of the signal mentioned are not included in the instruction text. However, all such detailed reference data is readily available for quick look-up in Chapter 8.

The Chapter 8 signal glossary includes alphabetically-ordered entries for all input and output signals of the discfile control, for all logic levels and pulses used within the system, and for all control and status flip-flops. Each glossary entry comprises a detailed description of both source and application of the signal. The signal glossary as a whole thus provides a random-access description of the entire system logic. Because the glossary is completely cross-referenced, the user can extract the specific information he requires with minimum time and effort.

Once they have been thoroughly understood, the engineering logic drawings and the flow diagrams provide the fastest and most extensive source of reference data. After a reasonable learning period, a competent



maintenance engineer can orient logic function with particular drawings and even with the approximate area of the drawing which shows given sections of the logic. For reference purposes, the Chapter 8 signal glossary can be used as a highly detailed index to the engineering drawings. The glossary includes the drawing coordinates of each signal as well as a description of its source and use.

#### 1.4 REFERENCE CONVENTIONS

The Digital Equipment Corporation engineering drawing conventions and instruction manual referencing should be understood at this point. A study of the material contained in Chapter 9 and the following paragraphs before proceeding with detailed descriptions will save considerable reference time and preserve continuity of thought when reading the text that follows.

Any reference to an illustration by a chapter-oriented figure number indicates that the figure is to be found in the text following the reference.

Example: Figure 2-1 (The first in-text figure of Chapter 2.)

Any reference to an engineering drawing number indicates that the drawing is to be found in a special drawing section or chapter. All engineering drawings are referenced first by the full drawing number.

Example: BS-D-270-516-0-CM

To locate a specific signal or function on a drawing, a system of coordinates is used. As shown on the drawings of Chapter 9, coordinates are designated by a letter and number. Thus, in any drawing reference,

coordinate location appears immediately after the number separated by a colon.

Example: BS-D-270-516-0-CM:A3

One last text reference convention should be noted. Occasionally it is desirable to indicate the state of a circuit within a logic description. This is done by following the mnemonic designation of the circuit with the circuit state in parentheses. For example, the parity error flip-flop is designated PER on the Status Logic drawing. If the flip-flop is in the 1 state, the assertion of either of its output levels is designated PER(1), but if the flip-flop contains 0, then the asserted output levels are designated PER(0).

Its output levels are designated as follows:

When PER contains 1: PER(1) is asserted

When PER contains 0: PER(0) is asserted

Note that the assertion level can be negative or ground for either state of the flip-flop.

The signal glossary of Chapter 8 is also an important adjunct to both the text and the drawings. This glossary can be used in a cross-indexing manner so that any signal and the conditions that generate it can be easily and completely referenced. By using a chain look-up procedure, the user can proceed from any input to its final consequences, or from any output to its original sources.

## 1.5 REFERENCE DOCUMENTS

### By Digital Equipment Corporation:

- 1) FLIP CHIP Modules Catalog, C-105
- 2) MAINDEC 670 - Magnetic Disc Test Maintenance Program

### By Data Products Corp. DISCFILE\* Division:

- 1) General Information Manual dp/f-5022, DISCFILE Storage System (Oct. 1964)
- 2) DISCFILE Instruction Manual Model dp/f-5022 with Addendum 0012 for Series 1-17 Systems (March 15, 1965)
- 3) Specification for Model 5022 DISCFILE Storage System No. 102253 with Addendum A (Dec. 23, 1964)
- 4) Pre-Delivery Acceptance Test for Model 5022 DISCFILE Storage System No. 102254 (Dec. 4, 1964)
- 5) Customer Information Bulletins for Model 5022 DISCFILE Storage Systems

\* Trademark of Data Products Corp. DISCFILE Division, P.O. Box 751, Gateway Station, Culver City, California

## CHAPTER 2

### GENERAL DESCRIPTION

#### 2.1 SYSTEM APPLICATION

The Discfile Control 270 and Discfile 5022 constitute a fast, random-access mass storage system capable of rapidly transferring large blocks of data to or from PDP-6 core memory. Each discfile unit stores 5.76 million 37-bit data words, slightly over twice the amount of data that can be stored on a 2400-foot magnetic tape at 556 frames per inch density. The rate of data transfer to or from the discfile system is about ten times that of magnetic tape (assuming that the tape is operated at 556 density and 112.5 inches per second tape speed). For inner-zone operation, the discfile transfers data at about 400 kc (2.4  $\mu$ sec per bit); the outer-zone data transfer rate is about 700 kc (1.4  $\mu$ sec per bit). Over 63% of the data is stored in outer zone sectors, so the mean data-transfer rate is about 590 kc. Random access is available to any given sector of data but not to individual data words within the sectors; each sector contains 128 data words. Following a single access, up to 44 sequentially-addressed sectors can be processed without further addressing.

Figure 2-1 is a block diagram showing a typical system configuration. Every discfile system contains a Discfile Control 270 and a Discfile 5022. The Discfile 5022 consists of a logic unit and one to four discfile units. During both output and input operations, 19-bit addresses are sent directly from the processor to the discfile control. The actual data sent to or

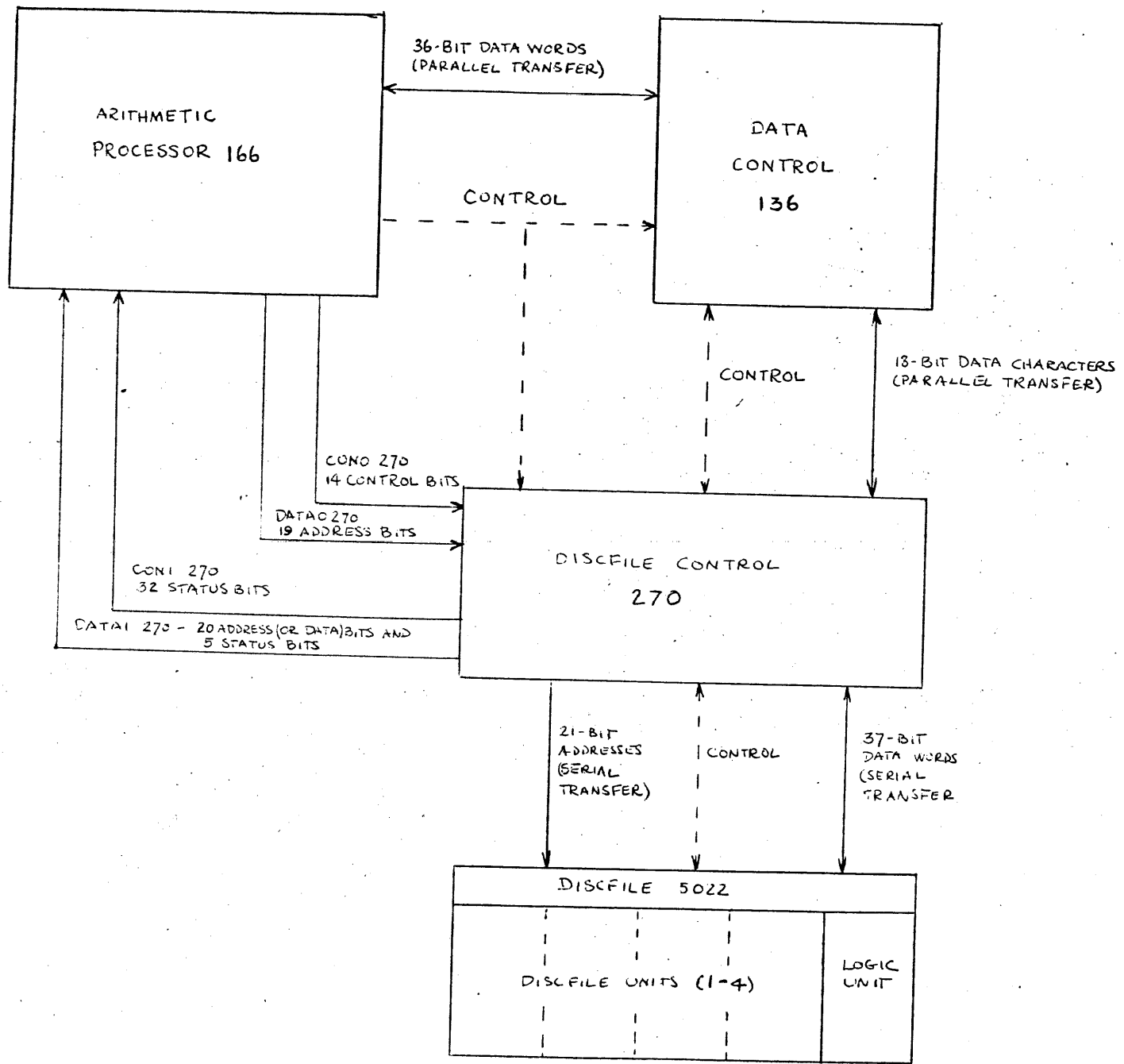


FIGURE 2-1 DISCFILE SYSTEM CONFIGURATION

received from the addressed locations follows a different route between the processor and the discfile control. Data flow from the processor to the discfile control and from the discfile control to the processor is always through the Data Control 136.

Output data from the processor is transferred out to the Data Control 136 in 36-bit data words. After receiving each 36-bit data word from the processor, the Data Control 136 divides it into two 18-bit characters and transfers these characters to the Discfile Control 270 one at a time. If the data is to be written at the discfile (rather than to be used within the discfile control for read comparison), the discfile control transmits the data to the Discfile 5022 serially one bit at a time. After transmitting each pair of characters to the discfile, the discfile control generates a parity bit and transmits it also to the discfile. At the discfile, all 37 bits (36 data bits and the parity bit) are written onto the addressed sector.

For input operations, the process described above is essentially reversed. At the Discfile 5022, data is read from the addressed sector. This data is then serially transferred into the Discfile Control 270, every 36 data bits being followed by a parity bit. At the discfile control, the parity of the incoming data is checked. If the data is to be read into the processor (rather than to be used within the discfile control for read comparison) the discfile control assembles 18-bit data characters for transfer into the Data Control 136. The data control in turn assembles pairs of 18-bit characters into 36-bit data words, and transfers these data words into the processor.

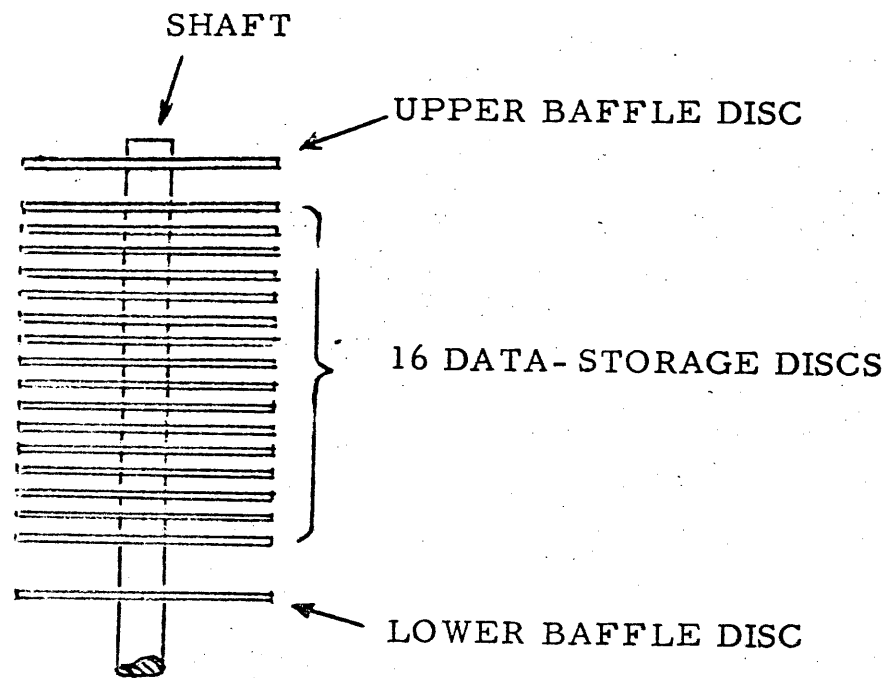
## 2.2 DESCRIPTION OF DISCFILE 5022

A basic understanding of the structure and operation of the Discfile 5022 is of considerable help in learning the function of the Discfile Control 270. The present paragraph is included only as a brief summary description of the discfile; for more detailed information refer to the reference documents listed at the end of Chapter 1.

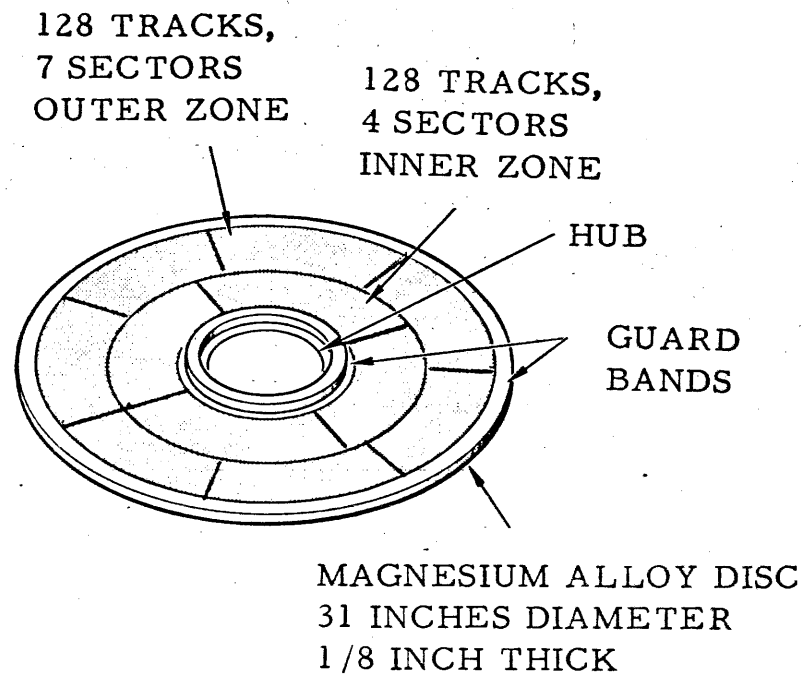
### a Discfile Data-Storage

A Discfile 5022 contains a logic unit and one to four discfile units. Each discfile unit stores data on 16 ferrous-oxide coated magnesium alloy discs 31 inches in diameter, all mounted on a common axial shaft which rotates at about 1200 rpm. Top and bottom baffle discs are mounted on the same shaft above and below the stack of 16 data-storage discs (Figure 2-2). The bottom surface of the upper baffle disc contains the control tracks that provide inner and outer zone write clock pulses, sector characters and index characters. The lower baffle disc contains control tracks or data.

A typical data-storage disc is shown at the right of Figure 2-2. The data is stored on both the top and bottom surfaces of the disc. Each surface of the disc is divided into two zones, each containing 128 concentric data tracks. The tracks are spaced 0.037 inches apart center to center. The inner zone is divided into four sectors; the outer zone is divided into seven sectors. On a single sector of a single track the discfile can store 128 37-bit data words. Because seven outer-zone sectors may be written or read in the same time that is required to write or read four inner-zone



DISC STACK



SINGLE DATA-STORAGE DISC

FIGURE 2-2 THE DATA-STORAGE ASSEMBLY OF A DISCFILE UNIT



sectors, the outer zone uses a faster clock rate than the inner zone (1.4  $\mu$ sec per bit, outer zone; 2.4  $\mu$ sec per bit, inner zone).

Associated with each disc is a forked access arm and a digital positioner. The digital positioner is a linear dc motor which includes a permanent magnet armature that is attached to one end of the access arm. The digital positioner can move the access arm rapidly and precisely to any of 64 evenly spaced radial positions. Each of these 64 positions is permanently fixed by a magnetic "notch" in the stator of the digital positioner.

One branch of each forked access arm passes over the associated disc, the other branch passes under the disc (see Figure 2-3). Each of the two branches of the access arm supports an inner-zone flying-head pad and an outer-zone flying-head pad.

TABLE 2-1 FLYING-HEAD PAD ASSIGNMENT

Branch of Access Arm	Flying-head Pad	Provides Access to the 128 Data Tracks Located In:
Upper	Inner-zone	Inner zone of disc's top surface
Upper	Outer-zone	Outer zone of disc's top surface
-----		
Lower	Inner-zone	Inner zone of disc's bottom surface
Lower	Outer-zone	Outer zone of disc's bottom surface

Each of the four flying-head pads that are mounted on a given access arm contain two separate read-write heads accurately mounted at a fixed radial separation equal to an odd number of track widths. (Each of these

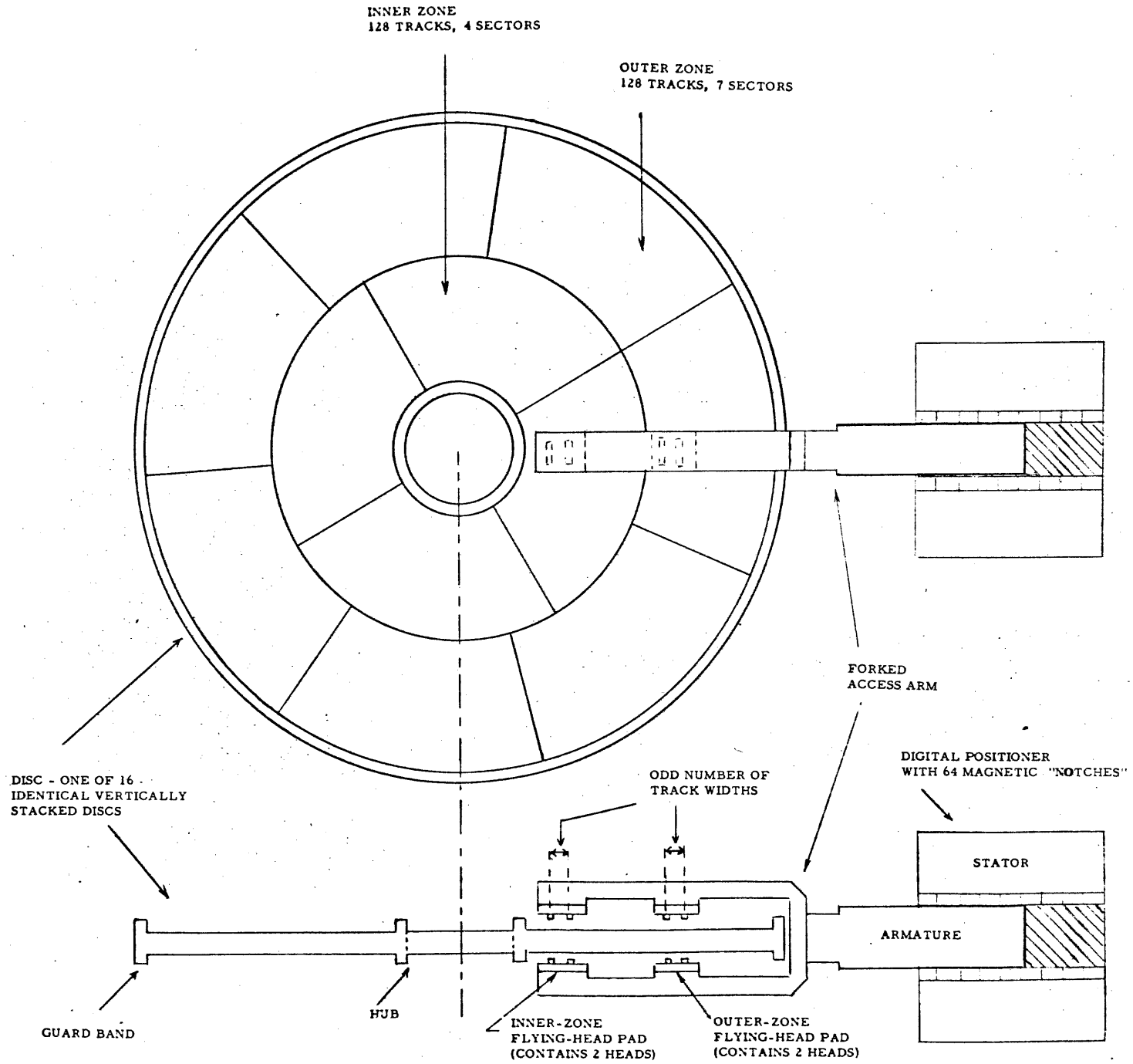


FIGURE 2-3 SIMPLIFIED SCHEMATIC DIAGRAM OF SINGLE DISC AND ACCESS ARM

read-write heads contains a read-write gap and an erase gap.) As a result of this arrangement, eight separate tracks (one track corresponding to each of the eight read-write heads) are available for reading or writing at any given position of the access arm.

If the digital positioner were to move the access arm to each of the 64 discrete radial positions (one after another), the eight read-write heads would index to all 512 data tracks on the disc ( $64 \times 8 = 512$ ). These 512 data tracks would include every one of the 256 outer-zone tracks (128 outer-zone tracks on the top surface of the disc and 128 outer-zone tracks on the bottom surface of the disc) and every one of the 256 inner-zone tracks. When the access arm is at rest in any one of the 64 positions to which the digital positioner may be indexed, 44 sectors of data are available to the read-write heads without further mechanical motion (28 outer-zone sectors, and 16 inner-zone sectors).

The elements that make up a Discfile are summarized in Table 2-2 below.

TABLE 2-2 ELEMENTS OF DISCFILE 5022

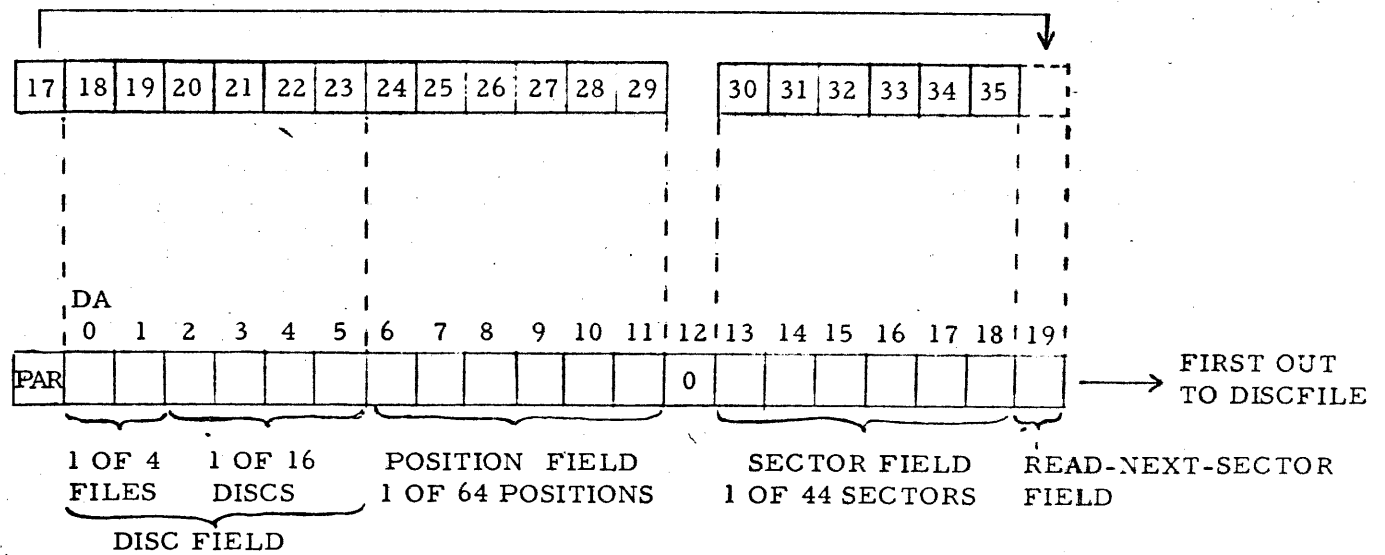
Elements	Number of Elements in Each:			
	Position	Disc	Discfile Unit	Discfile 5022
Discfile Units	-	-	-	1-4
Discs, Access Arms, Positioners	-	-	16	16-64
Flying-head pads	-	4	64	64-256
Read-write Heads	-	8	128	128-512
Positions	-	64	1024	1024-4096
Tracks	8	512	8192	8192-32,768
Sectors	44	2816	45,056	45,056- 180,224

b Address Structure

Data is written into or read from the Discfile 5022 in sectors of 128 data words each (sometimes referred to as records). Any given sector is uniquely addressed by a 21-bit address which specifies its physical location within the discfile. The structure of this address is shown in the lower portion of Figure 2-4. The upper portion of the figure shows the source of the address fields in the DATAO 270 instruction coding. Table 2-3 tabulates the read-write heads addressed by the 44 presently used sector-field configurations.

19-BIT ADDRESS AS SENT  
TO DISCFIELD CONTROL  
FROM PROCESSOR DURING  
DATAO 270 INSTRUCTION

21-BIT ADDRESS AS TRANS-  
MITTED TO DISCFIELD  
FROM DISCFIELD CONTROL



DISCFIELD ADDRESS FIELDS

FIGURE 2-4 ADDRESS STRUCTURE

TABLE 2-3 HEAD ADDRESS TABULATION

Decimal Address	Record Field Binary Equivalent							Addressed Head	Zone
	64	32	16	8	4	2	1		
0 through 3	0	0	0	0	0	0	0	0	IZ
4 through 7	0	0	0	0	1	0	0	1	IZ
8 through 11	0	0	0	1	0	0	0	2	IZ
12 through 15	0	0	0	1	1	0	0	3	IZ
16	0	0	1	0	0	0	0		
20	0	0	1	0	1	0	0		
24	0	0	1	1	0	0	0		
28	0	0	1	1	1	0	0	4	OZ
32	0	1	0	0	0	0	0		
36	0	1	0	0	1	0	0		
40	0	1	0	1	0	0	0		
17	0	0	1	0	0	0	1		
21	0	0	1	0	1	0	1		
25	0	0	1	1	0	0	1		
29	0	0	1	1	1	0	1	5	OZ
33	0	1	0	0	0	0	1		
37	0	1	0	0	1	0	1		
41	0	1	0	1	0	0	1		
18	0	0	1	0	0	1	0		
22	0	0	1	0	1	1	0		
26	0	0	1	1	0	1	0		
30	0	0	1	1	1	1	0	6	OZ
34	0	1	0	0	0	1	0		
38	0	1	0	0	1	1	0		
42	0	1	0	1	0	1	0		

TABLE 2-3 HEAD ADDRESS TABULATION (continued)

Decimal Address	Record Field Binary Equivalent							Addressed Head	Zone
	64	32	16	8	4	2	1		
19	0	0	1	0	0	1	1		
23	0	0	1	0	1	1	1		
27	0	0	1	1	0	1	1		
31	0	0	1	1	1	1	1	7	OZ
35	0	1	0	0	0	1	1		
39	0	1	0	0	1	1	1		
43	0	1	0	1	0	1	1		

The first address bit to be transmitted from the discfile control to the discfile is the read-next-sector bit. When this bit is coded 1 (as it normally is), it causes the discfile to process the single sector of data that is uniquely specified by the next 19 bits of the address. If, however, the read-next-sector bit is coded 0, the discfile ignores the first three bits of the sector field (the three bits that select a single sector to be processed from among the four or seven sectors constituting the addressed track). The discfile then processes whichever sector of the addressed track first passes the heads. (Ordinarily, this mode of operation is useful only for maintenance procedures; it is rarely employed during normal operations.)

There are several differences worth noting between the 19-bit address sent from the processor to the Discfile Control 270, and the 21-bit address transmitted to the Discfile 5022 from the discfile control. A 0 bit, generated within the discfile control, is always transmitted to the

discfile between the sector field and the position field of the address. At the discfile this bit is presently unused, but if the system were to be modified to include smaller but more numerous sectors, the 0 bit would be available for use as a seventh bit of the sector-field. After transmitting 20 address bits to the discfile, the discfile control generates and transmits an address parity bit. This 21st and final bit of the address enables the discfile to determine whether any errors have occurred during the address transmission. The format of the discfile logic requires that the read-next-sector bit be located at the sector-field end of the address (rather than at the disc-field end of the address as it is coded in the DATAO 270 instruction. The requisite transposition is accomplished at the input gating of the discfile control data accumulator.

#### c Minimum-Access Programming

When a new sector is selected for processing, the required access time depends on the amount of switching time and physical positioning time that is needed to index from the last sector processed to the new sector address. Table 2-4, System Operating Specifications, illustrates the method of computing the access time that is expended for any given change of address. For most applications, a typical file of data occupies only a fraction of the total storage capacity of the discfile system. By choosing the shape of the file in an appropriate manner, the average access time can be substantially reduced, and the operating rate of the system can be increased proportionately.



### 2.3 PROGRAMMED OPERATIONS

The DATAI 270 and CONI 270 instructions permit the processor to sample the state of the discfile system. The DATAO 270 instruction is used to send a discfile address to the discfile control. The CONO 270 instruction sends control information to the discfile control.

a DATAI 270 Instruction (Figure FD-D-270-0-FD-Sheet 3-A2, 3)

The DATAI 270 instruction permits the processor to sample the contents of the data accumulator DA0-19, and the contents of the bit-shift counter BSC0-4. The bit assignments pertaining to this instruction are listed in Chapter 7, Table 7-1. This instruction is used primarily for maintenance purposes. During actual operating sequences there is usually no requirement to sample the accumulator or the bit-shift counter at the processor.

b CONI 270 Instruction (Figure FD-D-270-0-FD-Sheet 3-D5-7)

The CONI 270 instruction permits the processor to sample the contents of the command buffer, the file-control octoflop, the nine error-status flags, and the relay-meter test switches. The bit assignments pertaining to the instruction are listed in Chapter 7, Table 7-2. The CONI 270 instruction is perhaps most frequently used for sampling the file-control octoflop and the error-status flags, but like the DATAI 270 instruction described above, the CONI 270 is also used extensively for maintenance purposes.

c DATAO 270 Instruction (Figure FD-D-270-0-FD-Sheet 1)

The Discfile Control 270 can accept an address only during certain portions of its operating cycle. These portions of the operating cycle correspond to the IDS and ADT states of the file-control octoflop (described in Chapter 3 below). The IDS state of the octoflop is frequently used to initiate a priority interrupt request, thus notifying the programmer that the discfile control has completed the preceding operation and is ready to receive a new data address. The CONI 270 instruction provides an alternate means of testing the state of the octoflop and the readiness of the system to receive a new address.

The DATAO 270 instruction transmits 19 discfile address bits to the discfile control. Eighteen of these nineteen bits specify the location of the next data sector to be processed; the nineteenth bit is the read-next-sector bit. This bit determines whether the full address is to be utilized, or only that portion of the address that specifies the appropriate data track (of four or seven sectors, as the case may be). Normally, the read-next-sector bit is coded 0, the full address is used, and the discfile operates on a uniquely-addressed data sector. If, however, the read-next-sector bit is coded 1, the discfile processes the first sector of the addressed track to arrive under the read-write heads.

The DATAO 270 instruction first causes the discfile control to send a SELECT pulse to the discfile; the SELECT prepares the discfile to receive the address. The discfile control then transmits 21 address bits to the discfile (the 19 bits received from the processor, one additional bit

which is always 0, and a parity bit). After completing the address transmission, the discfile control sends the discfile an ADDRESS TRANSMITTED pulse; this pulse disconnects the discfile from the discfile control and initiates the address seek operation. The bit assignments pertaining to the DATAO 270 instruction are listed in Chapter 7, Table 7-3 .

d CONO 270 Instruction (Figure FD-D-270-0-FD-Sheet 3-A-D1, 2)

The processor sends 15 bits of control information to the discfile control at each CONO 270 instruction. Twelve of these 15 control bits are loaded into the command buffer. The remaining three control bits set no flip-flops in the discfile control, but are instead used directly as control inputs.

Functions Controlled by CONO 270 Coding

The functions of the Discfile Control 270 that are controlled by the coding of the CONO 270 instruction include:

1. The choice of the command to be executed (read, write or read compare).
2. Choice of whether or not the command is to be continued beyond the end of the first sector processed. (In the case of the read command only, whether or not the command is to be terminated at the time of the CONO 270 instruction.)
3. Choice of whether or not to remove power from the addressed discfile positioner at the end of the command.
4. Specification of the particular conditions which are to be allowed to initiate a priority interrupt request.

5. Selection of the priority interrupt channel to be assigned to the discfile control.
6. Choice of whether or not to clear the nine error-status flags.
7. Two maintenance functions. These functions provide program control of the GIVE A CHARACTER and TAKE A CHARACTER pulses sent to the Data Control 136.

The bit assignments pertaining to the CONO 270 instruction are listed in Chapter 7, Table 7-4 .

#### Command Repertoire

By suitable coding of the two command-code bits of the CONO 270 instruction (bits 25 and 26), the processor can cause the Discfile Control to execute any of the following three commands.

(1) Read Command - Input data is read from the discfile starting at the beginning of the 128-word sector addressed by the preceding DATAO 270 instruction. The data is loaded into DA2 as it is read in serial fashion, one bit at a time, and is then shifted right until a full 18-bit data character is stored in DA2-19. At the conclusion of this loading process, the discfile control sends a TAKE A CHARACTER pulse to the Data Control 136, causing the data control to strobe the character into its low order accumulator bits, and if necessary, to shift it left to make room for the second character of the data word. A similar process is followed for the second 18-bit data character and all succeeding data characters. Every 36 data bits from the discfile are followed by a parity bit, and the parity of each data word is checked at the discfile control.

The Data Control 136 assembles pairs of data-characters into 36-bit data words and transfers these data words into the processor. Normally this process continues until a full 128-word sector of data has been read into the processor via the data control. Unlike the write and the read compare commands, the read command can, however, be terminated at any point within a sector, or for that matter within a data word, by giving a CONO 270 command with a 1 in bit 23. Such a CONO 270 command sets the END flip-flop in the discfile control, thereby terminating the read operations almost immediately.

(2) Write Command - Output data is written at the discfile starting at the beginning of the 128-word sector addressed by the preceding DATAO 270 instruction. The Data Control 136 loads 18-bit data characters into DA2-19 of the discfile control data accumulator. The discfile control shifts these data characters right, and transmits them to the discfile in serial fashion one bit at a time. As the last bit of each data character is transmitted out to the discfile, the discfile control strobes in the next 18-bit data character from the Data Control 136, and sends the data control a GIVE A CHARACTER pulse, thus signalling the data control to shift the following character into position for transfer out. After every 36 data bits, the discfile control generates an appropriate parity bit and transmits it to the discfile. At the discfile, all 37 bits (36 data bits and the parity bit) are written out onto the addressed location. This process continues until a full 128-word sector is written. If the output data is exhausted before the end of the sector is reached, 0s are written for the rest of the sector.

(3) Read Compare Command - The read compare command compares output data from the processor with corresponding input data read from the discfile. The comparison is executed on a bit-by-bit basis, but does not include parity bits. The output data is sent to the discfile control through the Data Control 136 (as during the write command described above) and the input data is brought in from the discfile (as during the read command described above). The RCE flip-flop in the discfile control is set whenever an output data bit from the Data Control 136 fails to match the corresponding input data bit read from the discfile. The set of the RCE flip-flop can be used to initiate a priority interrupt request, thereby notifying the programmer that a read compare error has been detected.

No output parity bits are generated during read compare commands, and for read comparison purposes the incoming parity bits from the discfile are ignored. (Note, however, that the incoming data from the discfile is subject to the normal parity test during the read compare commands just as during read commands.)

Input data from the discfile is read in serially, one bit at a time, starting at the beginning of the 128-word sector addressed by the preceding DATAO 270 instruction. Eighteen-bit output data characters from the Data Control 136 are parallel-loaded into DA2-19 of the discfile control data accumulator. The discfile control shifts these output data characters right one bit at a time, comparing the contents of DA19 with the corresponding input data bit at each shift. The comparison proceeds one bit at a time, ignoring parity bits. At the first pair of data bits that are not

identical, the comparison fails, causing the RCE flip-flop to be set, and (if the programmer so desires) initiating a priority interrupt request on a predetermined priority interrupt channel.

As the last bit of each output data character is compared and shifted out, the discfile control strobes in the next 18-bit data character from the Data Control 136, and sends the data control a GIVE A CHARACTER pulse (just as during the write command described above). This process always continues until a full 128-word data sector is processed. If the output data is exhausted before the end of the input sector is reached, a read compare error results (unless the remainder of the input sector also contains only 0 data bits).

#### e Parity

During write commands, after transmitting each 36-bit data word to the discfile, the discfile control generates and transmits an appropriate parity bit. At the discfile, this parity bit is written onto the disc immediately after the 36 associated data bits.

During both read and read compare commands, the parity of each incoming 37-bit word is checked by the discfile control. Whenever a parity error is detected, the PER flip-flop is set. The set of the PER flip-flop can be used to initiate a priority interrupt request, thereby notifying the programmer that a read compare error has been detected.

#### f Priority Interrupt

Seven priority interrupt channels are available. See Chapter 3, Priority Interrupt, for a description of interrupt conditions.

## 2.4 SYSTEM DATA

System operating specifications, physical characteristics, and power requirements are listed in Tables 2-4, 2-5, and 2-6 below.

TABLE 2-4 SYSTEM OPERATING SPECIFICATIONS

<u>Storage Capacity</u>		
Data words per sector (37-bit words)		128
Sectors per position		44
Positions per disc		64
Sectors per disc		2816
Discs per disc unit		16
Sectors per disc unit		45,056
Data words per disc unit (37-bit words)		5.76 million
Bits per disc unit		213.4 million
Disc units per Discfile 5022		1 to 4
<u>Operating Speed</u>		
Time per disc revolution		52 ms
<u>Data Transfer Rates:</u>	<u>Inner Zone</u>	<u>Outer Zone</u>
Time per bit	2.4 $\mu$ sec	1.4 $\mu$ sec
Time per 37-bit data word	88.8 $\mu$ sec	51.8 $\mu$ sec
Bit frequency (nominal)	418 kc	714 kc
Note: Bit-to-bit timing may vary as much as $\pm 30\%$ from the average of $\frac{1}{\text{Disc RPS} \times \text{bits per track}}$		



TABLE 2-4 SYSTEM OPERATING SPECIFICATIONS (continued)

<u>Components of Access Time</u>	
Positioner Switching Time	20-30 ms
Head Switching Time	100 $\mu$ sec
Positioning Time (including confirmation time)	Minimum (1 position): 80 ms Maximum (64 positions): 225 ms
Confirmation Time (Confirmation time is required whenever positioner switching or motion takes place.)	39 msec
Latency Time	Maximum: 52 ms

<u>Typical Total Access Times</u>	
<u>Access to address at same position on same disc.</u> (Head switching time + latency time.)	Average: 26 ms
<u>Access to address at same position on different disc.</u> (Positioner switching time + confirmation time + latency time.)	Average: 91 ms
<u>Random Access.</u> (Positioner switching time + motion time + confirmation time + latency time; see Figure 2-4.)	
<u>Average.</u> (16-position move, average switching and latency):	202 ms
<u>Maximum.</u> (63-position move with worst-case switching and latency):	307 ms
<u>Minimum.</u> (1-position move, average switching and latency):	132 ms

TABLE 2-4 SYSTEM OPERATING SPECIFICATIONS (continued)

<u>Recording Parameters</u>		
Track separation (center to center)		37.5 mils
Read/write track width		25 mils
Erase track width		40 mils
Density of recording (average mid-zone)	Inner zone <u>bits/inch</u>	Outer zone <u>bits/inch</u>
Header to data gap	<u>        </u> inches (	<u>        </u> bits)
Inter-sector gap	<u>        </u> inches (	<u>        </u> bits)

Priority Interrupt Conditions

When enabled by the corresponding flip-flop switch each of the following interrupt conditions can initiate a priority interrupt request on a predetermined interrupt channel (seven priority interrupt channels are available).

<u>Interrupt Condition</u>	<u>Signifies</u>	<u>Enabled by Switch</u>
DFR	Discfile Ready	EFR
IDS	Idle State	EIS
SEF	Sector End Flag	EES
FER	File Error	EFE
PER	Parity Error	EFE
RCE	Read Compare Error	EFE
DRL	Data Request Late	EFE

Parity

Odd; each 37-bit word contains 36 data bits followed by a parity bit.

TABLE 2-5 PHYSICAL CHARACTERISTICS

Construction of Discfile Control 270

One standard, all-steel construction DEC cabinet containing three FLIP-CHIP mounting panels.

Modules

Standard DEC FLIP-CHIP modules, series B, G, R and W.

Logic

Solid state. Transistors and crystal diodes utilizing static logic levels (0 vdc and -3 vdc).

Dimensions

	<u>Discfile Control 270</u>	<u>Discfile 5022</u>
Height	69-1/2 inches	63-1/4 inches
Width	22-1/4 inches	87 inches (including logic unit)
Depth	27-1/8 inches	38 inches
Service Clearances		
Front	8-3/4 inches	33 inches
Rear	14-7/8 inches	33 inches
Sides	-	33 inches

Weight and Loading

Discfile Control 270:

Cabinet	160 lbs.
Logic (approx.)	60 lbs.
Total	220 lbs.

TABLE 2-5 PHYSICAL CHARACTERISTICS (continued)

Weight and Loading (continued)

Discfile 5022

Logic Unit	490 lbs.
(Floor Loading	134 psf)
Disc Unit	2575 lbs.
(Floor Loading	107 psf
Pad Loading	33 psf)
Total	3065 lbs.

Environmental Requirements

Discfile Control 270:

Operating Temperature	Maximum:	100°F
	Minimum:	50°F

Discfile 5022:

Operating Temperature	Maximum:	85°F
	Minimum:	60°F
Relative Humidity	Maximum:	80 %
	Minimum:	20 %

TABLE 2-6 POWER REQUIREMENTS

Discfile Control 270:

Power Equipment	DEC Power Supply Type 728 DEC Power Control Type 834-836
Line Voltage Input	100 to 125 volts, 60 cycle, single phase
Power Plug	Hubble Twist-Loc 3-prong, 30 ampere, 250 volt
Current Consumption	Surge: 4.5 ampere Normal: 3 ampere
Power Consumption	240 watts
Heat Dissipation	1375 btu/hour

Discfile 5022:

Line Voltage Input	208 volt $\pm$ 10%, 3 lines, 60 cps
Current Consumption	Start current: 35 ampere maximum on any one line. Run current: 15 amp. maximum on one line, 10 amp. maximum on other two lines.
Power Consumption	Logic unit and one disc unit: 4.5 kw. Additional disc units 3.5 kw each.
Heat dissipation	Logic unit and one disc unit: 15,300 btu/hour. Each additional disc unit 11,900 btu/hour.

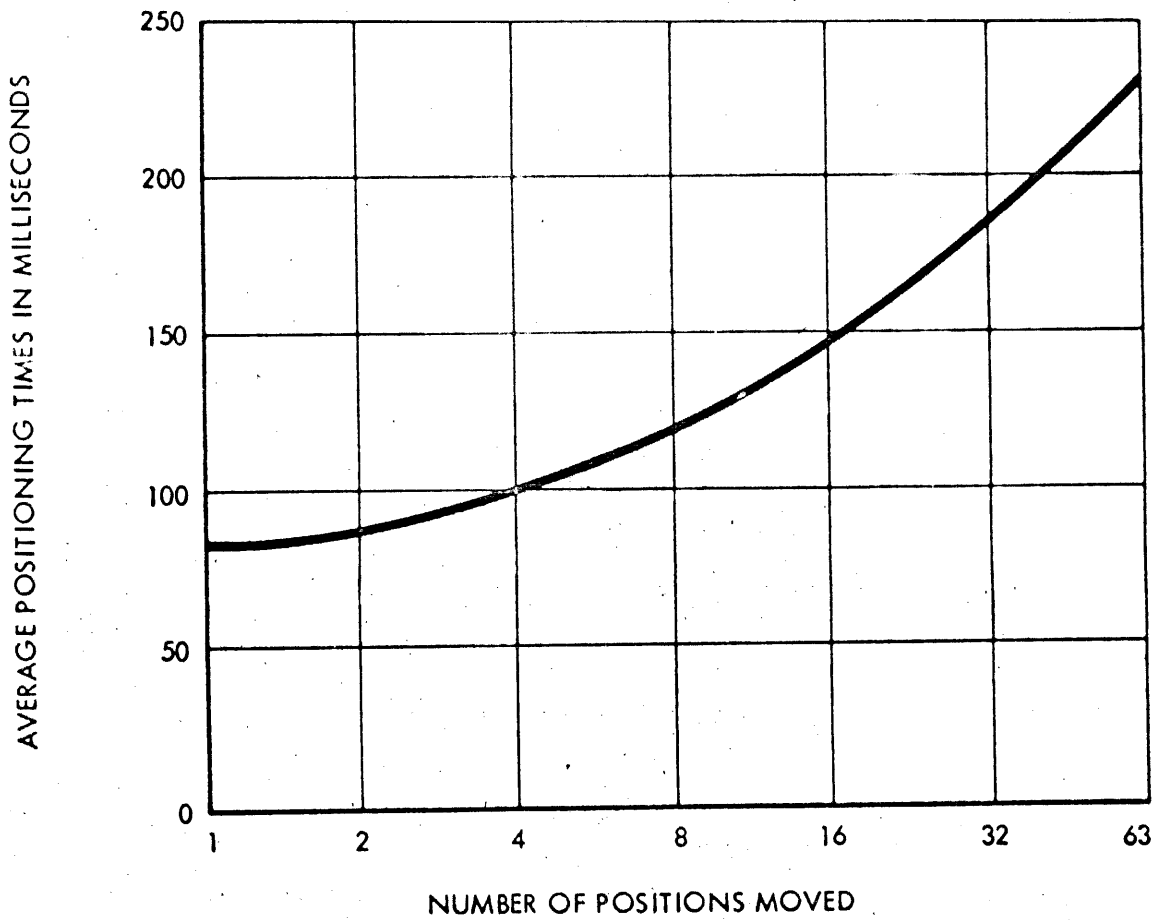


FIGURE 2-5  
TYPICAL POSITIONING TIMES  
INCLUDING CONFIRMATION

## CHAPTER 3

### SYSTEM LOGIC

This chapter is organized horizontally by areas of the system logic. Its purpose is to present a brief overall description of the major signals and circuits used in the Discfile Control 270. All sections of this chapter include tables listing the signals relevant to the section by mnemonic abbreviation. Listed with each signal is the engineering logic diagram designation and coordinate at which the signal is generated. This tabular listing directly corresponds to the entry headings in the Chapter 8 signal glossary. Each signal is there described in full detail.

It is not recommended that the reader attempt to refer to a large number of the glossary entries while reading this chapter for the first time. For most people a more efficient approach is to read this chapter rapidly to get a general understanding of the various functional areas of the system; then to read Chapter 4, System Operating Sequences, to learn the step-by-step time sequence of the major system operations; and only then to return for a second pass through the two chapters. On this second pass it may be helpful to refer to the glossary whenever the operation of a given circuit or the execution of a given operation seems unclear.

### 3.1 INTERFACE SIGNALS

The Discfile Control 270 interacts with three other systems: 1) the PDP-6 Processor; 2) the Data Control 136; and 3) the Discfile 5022.

#### a Processor Interface

This paragraph describes the control signals applied to the discfile control from the processor.

TABLE 3-1 PROCESSOR SIGNALS TO DISCFILE CONTROL

When Occurs	Control Signal from Processor	Signal Produced Within the Discfile Control 270
INITIAL CLEAR:	IOB RESET (-SC:C1)	IBR (SC:C1) CCB (-CM:C4) CDA (-AD:B8) FCL (-AD:C5) SCL (-SC:C6)
ALL COMMANDS:	IOS3-9 (-SC:D1)	SEL (-SC:D2)
CONO:	IOB CONO CLR (-CM:C3) IOB CONO SET (-CM:D3)	CCB (-CM:C4) PTC (-CM:C4)
DATAO:	IOB DATA CLR (-AD:B1) IOB DATA SET (-AD:B1)	CDA (-AD:A8) PTA (-AD:B8)
CONI:	IOB STATUS (-CM:D7)	STP (-CM:C8)
DATAI:	IOB DATA I (-AD:A1)	DTP (-AD:A8)

The IOB RESET pulse (and the resulting IBR) are generated when computer power goes on or when the operator presses the IO reset key on the computer console. The program may also generate a reset. The



IBR pulse and the four additional clear pulses it initiates (CCB, CDA, FCL and SCL) clear the entire discfile control.

The discfile control responds to the four IOT instructions (CONO, DATAO, CONI, and DATAI) only when the 14 IOS lines represented by IOS3-9 assert the device code 270. Whenever the device code portion of an IOT command contains 270, the SEL level is asserted within the discfile control. The SEL level enables the control to respond to the processor control signals associated with the instruction.

The CONO 270 instruction applies two control pulses to the discfile control one microsecond apart. The IOB CONO CLR pulse initiates CCB, which clears the discfile command buffer. The IOB CONO SET pulse then initiates PTC, which loads new control information into the discfile command buffer.

The DATAO 270 instruction also applies two control pulses to the discfile control one microsecond apart. The IOB DATA CLR pulse initiates CDA, which clears the discfile data accumulator DA0-19. The IOB DATA SET pulse then initiates PTA, which loads IOB17-35 into the data accumulator; this data provides 19 bits of the 21-bit discfile address. One of the remaining two bits is always 0, and thus is generated within the discfile control. The final bit is the address parity bit, which is also generated within the discfile control.

The CONI 270 and DATAI 270 instructions permit the processor to sample the state of the discfile control. The 2.5- $\mu$ sec IOB STATUS level enables STP to gate out a variety of CONI status information (including the

contents of the command buffer, the file-control octoflop, the error-status flags, and the relay-meter test switches). Similarly, the 2.5- $\mu$ sec IOB DATA I level enables DTP to gate out the contents of the data accumulator DA0-19 and the bit shift counter BSC0-4.

#### b Data Control 136 Interface

The discfile control applies the following signals to the Data Control 136:

GIVE A CHARACTER (-SC:C7)

TAKE A CHARACTER (SC:C7)

The GIVE A CHARACTER pulse signals the data control that the discfile control has accepted the 18-bit output character currently stored in the high order end of the data control data accumulator, and that the data control must bring another character into position for transfer out to the discfile control. The TAKE A CHARACTER pulse signals the data control that the discfile control has presented an 18-bit input character to the low order strobe data inputs of the data control data accumulator. This indicates to the data control that it may strobe the character into the low order bits of the data control data accumulator.

The Data Control 136 applies the following signals to the discfile control:

DA RQ (-CM:C1)

SEL 5 (-SC:B7)

During the output commands, write and read compare, the assertion of the DA RQ level indicates that the data control has sent out the last of

its output data. The discfile control uses the DA RQ level to detect the end of output data and to terminate the output command.

If the Data Control 136 has not been selected to the discfile in time for the beginning of a given command, the negation of the SEL 5 level causes an error condition.

### c Discfile 5022 Interface

The listing below summarizes the exchange of control information and data between the discfile and the discfile control.

TABLE 3-2 CONTROL SIGNALS TO THE DISCFILE  
FROM THE DISCFILE CONTROL

Signal	Function
MCL (-CM:D7)	Master Clear signal generated by pushbutton at the discfile control. Clears the discfile logic.
SELECT (-TR:A6)	Prepares the discfile to receive and store an address.
ALERT (-TR:A7)	Prepares the discfile logic to receive the forthcoming command signal (READ or WRITE).
READ (-TR:A7)	Commands the discfile to read a sector.
WRITE (-TR:A7)	Commands the discfile to write a sector.
END (-TR:A5)	Disconnects the discfile from the discfile control. After receiving END, the discfile is ready to receive a new SELECT.
CLEAR (-TR:A4)	Starts the turn-off of positioner power at the discfile. An END always accompanies a CLEAR, but the converse is not true.

TABLE 3-3 CONTROL SIGNALS FROM THE DISCFILE  
TO THE DISCFILE CONTROL

Signal	Function
READY (-TR:A4)	Indicates that the discfile has found the header of the "get ready" sector next preceding the sector to be operated upon, and is ready to be alerted for a read or write command.
WRITE CLOCK EVEN (-TR:D5)	During write operations, the discfile sends the discfile control one of these pulses to clock out every even-numbered bit.
WRITE CLOCK ODD (-TR:D5)	During write operations, the discfile sends the discfile control one of these pulses to clock out every odd-numbered bit.
ERROR SIGNAL (-SC:B1)	Indicates that an error has been detected at the discfile.
WRITE LOCKOUT WARNING (-SC:B1)	Indicates that the processor has addressed a locked out disc.
ALARM (-SC:B2)	Indicates presence of an alarm condition at the discfile.
OPERABLE (-SC:C2)	Indicates that the discfile is operable, i. e. ready to receive commands from the discfile control.

TABLE 3-4 DATA SIGNALS TO OR FROM THE DISCFILE

Signal	Meaning
EDO (-TR:C3)	Even-numbered input or output bit a 1.
EDZ (-TR:C4)	Even-numbered input or output bit a 0.
ODO (-TR:C1)	Odd-numbered input or output bit a 1.
ODZ (-TR:C2)	Odd-numbered input or output bit a 0.

### 3.2 COMMAND LOGIC

The command logic accepts control information from the PDP-6 processor, decodes the information, and applies the resulting command levels to various circuits within the discfile control. The command logic includes an 11-bit command buffer register and a decoding network.

TABLE 3-5 COMMAND LOGIC SUMMARY

CM0-1 (-CM:B1, 2)	CCB (-CM:C4)	CLR (-CM:B3)
NOP (-CM:A2)	PTC (-CM:C4)	END flip-flop (-CM:B4)
RED (-CM:A2)	CCE (-CM:D2)	EFE (-CM:B4)
WRT (-CM:A1)		EES (-CM:B5)
RDC (-CM:A1)		EIS (-CM:B6)
		PIA0-2 (-CM:B7, 8)

During the CONO 270 command, the contents of the CONO effective address determines the control information that is loaded into the command buffer. The two most significant bits of the command buffer are CM0 and CM1. The contents of these two bits determine the nature of the command to be performed by the discfile. The outputs of the CM0 and CM1 flip-flops are used directly to control certain functions of the discfile control. These outputs are also applied to a half binary-to-octal decoder which in turn produces one of the four outputs, depending on the contents of CM0-1:

TABLE 3-6 COMMAND CODE DECODING

CM0-1 Contain	Command Level Asserted
0	NOP - No operation.
1	RED - Read command.
2	WRT - Write command.
3	RDC - Read compare command.

The NOP, RED, WRT, and RDC command levels are used widely in the discfile control to govern the operations performed during the corresponding operating sequences.

During the CONO 270 command, a CCB pulse clears the command buffer, and then one microsecond later a PTC pulse loads new control information into the buffer. The two command-code bits CM0 and CM1 cannot be affected by this operation unless the change commands enable level CCE is asserted. This level is only asserted during those portions of the discfile control operating cycle when it is appropriate to change commands.

Whenever the END flip-flop is set, the command code bits CM0-1 are automatically cleared at the end of the first data sector to be processed; two  $\mu$ sec later an END pulse is sent to the discfile. For the write and read compare commands, the current sector will continue for the full 128 words, regardless of whether or not END is set. For the read command, however, the command is terminated immediately after END is set, and the command code bits are cleared at that time. Whenever the CLR flip-flop is set, the END flip-flop is automatically set at the same time. An END pulse is sent to the discfile at the end of any sector during which the END flip-flop is set; if CLR is set, a CLEAR pulse is sent to the discfile as well.

The remaining seven bits of the command buffer are associated with the priority interrupt system. The four flip-flop switches EFE, EES, EFR, and EIS determine which interrupt conditions are to be enabled; the

three priority interrupt assignment flip-flops PIA0-2 determine the priority interrupt channel to be used by the discfile control (and hence the priority of any interrupt break which the discfile control may request).

### 3.3 FILE-CONTROL LOGIC

The file-control logic consists of an 8-state control device (the file-control octoflop) and associated delays and control networks. The file-control logic governs the transmission of control pulses to the discfile and also controls various operations that occur within the discfile control.

#### a Octoflop Structure

The file-control octoflop is composed of two R284 quadraflops. In engineering logic diagram BS-D-270-0-FC the octoflop is shown by a schematic representation resembling eight DEC flip-flops connected in a ring. Logically, the octoflop can be regarded as though it were a set of eight flip-flops one of which (and only one) is in the one state, and the remaining seven of which contain 0. When any one of the eight "flip-flops" is set to the 1 state, the remaining seven are reset to the 0 state.

TABLE 3-7 FILE CONTROL LOGIC SUMMARY

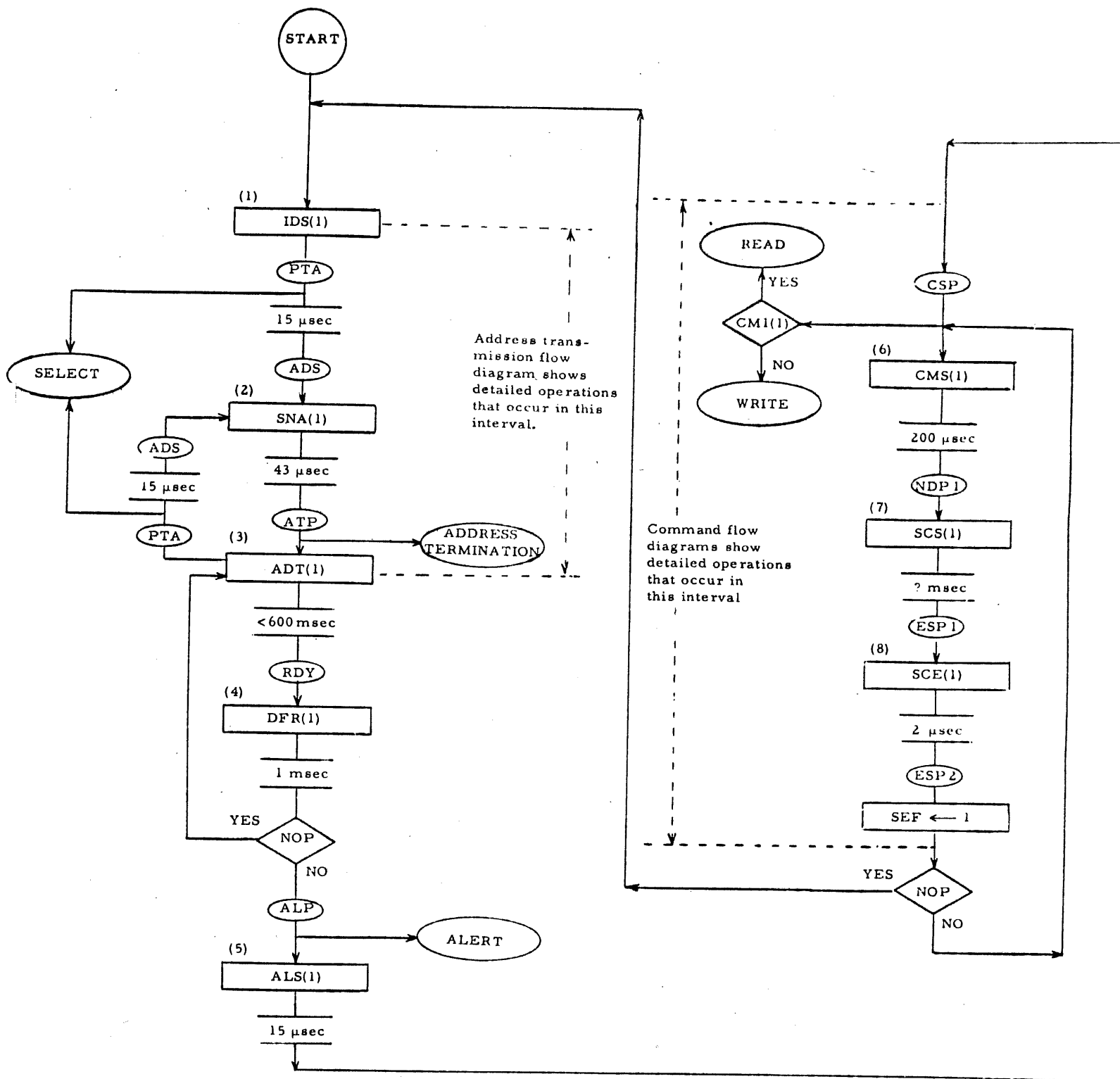
Octoflop State	Set at Pulse
1) IDS (-FC:B2)	IBR (-SC:C1), ESP 2 (-FC:C8)
2) SNA (-FC:B2)	ADS (-FC:C2)
3) ADT (-FC:B3)	ATP (-FC:C3)
4) DFR (-FC:B4)	RDY (-TR:C5)
5) ALS (-FC:B4)	ALP (-FC:B4)
6) CMS (-FC:B5)	CSP (-FC:C4)
7) SCS (-FC:B6)	NDP 1 (-FC:B6)
8) SCE (-FC:B7)	ESP 1 (-FC:C6)
Flip-flop	Set at Pulse
SEF (-SC:A7)	ESP 2 (-FC:C8)
Other	
PTA (-AD:B8)	
FCL (-AD:C5)	
NDP 2 (-FC:B8)	
END flip-flop (-CM:B4)	

b Octoflop Cycle

A detailed flow diagram of the octoflop cycle is shown in Figure 3-1. When the system is turned on, the IBR pulse resets the octoflop to IDS (idle state). This is the quiescent condition that the octoflop holds while the discfile control is waiting for an address.

The DATAO 270 instruction is used to send a new address to the discfile control. At the IOB DATAO SET pulse, the discfile control produces





KEY:



- OUTPUT PULSES FROM 270 - - - - - 
- 270 INTERNAL CONTROL PULSES - - - - - 

FIGURE 3-1 FILE-CONTROL OCTOFLOP CYCLE

a PTA pulse. This PTA sends a SELECT to the discfile and starts a 15- $\mu$ sec delay. At the termination of this delay, an ADS pulse is generated (to start the address clock) and the octoflop is advanced to its second state SNA (Select New Address). During the SNA state, 21 address bits are clocked out to the discfile in a sequential transfer, one bit each 1.33  $\mu$ sec. When the final address bit is transferred out, a 15- $\mu$ sec delay is started. The termination of this delay produces the ATP pulse; ATP is thus generated about 43  $\mu$ sec after the octoflop enters SNA state (28  $\mu$ sec + 15  $\mu$ sec = 43  $\mu$ sec).

The ATP pulse steps the octoflop to its third state ADT (Address Terminated). During the address terminated state, the discfile seeks the sector specified by the address that it received during SNA. A different address can be sent to the discfile control by programming another DATAO instruction while the control is in ADT state. This induces a seek interrupt, and returns the octoflop to SNA state while the new address is transferred out to the discfile.

When the discfile finds the addressed sector (the search normally requires less than 600 ms) a RDY pulse advances the octoflop from ATP to its fourth state DFR (Discfile Ready). The octoflop remains in DFR state for 1 msec. If no command is present in CM0-1, NOP is asserted, and the octoflop returns to ADT state at the termination of DFR state. The octoflop then oscillates between ADT state and DFR state, advancing to DFR each time the addressed sector is sensed, and returning to ADT after a one-millisecond delay.

If, however, there is a command code present in CM0-1, an ALP pulse is generated at the expiration of DFR state. The ALP pulse sends an ALERT to the discfile, and advances the octoflop from DFR state to its fifth state ALS (Alert State). The octoflop remains in ALS state for 15  $\mu$ sec.

A CSP pulse is generated at the expiration of the 15- $\mu$ sec ALS state delay. This CSP pulse sends a READ or a WRITE command pulse to the discfile (the choice depending on the contents of command code bit CM1) and advances the octoflop from ALS state to its sixth state CMS (Command Selected). The octoflop remains in CMS state for 200  $\mu$ sec.

An NDP 1 pulse is generated at the expiration of the 200- $\mu$ sec CMS delay. This NDP 1 pulse advances the octoflop from CMS state to its seventh state SCS (Sector Started). The NDP 1 pulse advances the octoflop from CMS state to its seventh state SCS (Sector Started). The NDP 1 pulse also generates an FCL pulse, and, after a one- $\mu$ sec delay, an NDP 2 pulse. (These pulses are used to initialize the bit shift counter BSC0-4 in preparation for the forthcoming data sector.)

The octoflop is set to SCS state before the first bit of the sector to be processed is detected. (Note that the RDY pulse that stepped the octoflop to DFR state is initiated by the header of the "get ready" sector immediately preceding the sector to be processed; hence there is an appreciable delay between the time when the octoflop is stepped to SCS state and the time when the first data bit of the next sector is read or written.

During the write and read compare commands, the octoflop remains in SCS state throughout the entire interval that is required to process the 128 data words of the current sector. Five microseconds after the final (37th) bit of the final (128th) word is processed, an integrating delay times out, producing the ESP 1 pulse. The ESP 1 pulse advances the octoflop from SCS to its eighth and final state SCE (Sector End).

During the read command, as during write and read compare, the ESP 1 pulse always occurs at the end of the 128-word data sector. However, unlike the write and read compare commands, the read command can also be terminated at any point within a sector by setting the END flip-flop. Approximately five  $\mu$ sec after END is set, the integrating delay times out, producing the ESP 1 pulse. As in the case of the ESP 1 that occurs at the end of the sector, the ESP 1 that is induced by setting END also advances the octoflop from SCS to the SCE (Sector End) state.

The octoflop remains in SCE state for only two  $\mu$ sec. Two  $\mu$ sec after the ESP 1 pulse advances the octoflop to SCE state, the ESP 2 pulse terminates the SCE state. If ESP 1 has cleared CM0-1 (indicating that no further sectors of data are to be processed) NOP is asserted, and ESP 2 resets the octoflop to IDS state. However, if more data is to be processed, the current command code is left in CM0-1, NOP is not asserted, and the ESP 2 pulse returns the octoflop to CMS state in preparation for processing the next sector of data.

Since the 2- $\mu$ sec SCE state is too brief to be available for the programmer to sample, the ESP pulse that terminates SCE state sets the sector end

flag SEF to let the programmer know that the end of the sector has been passed. The SEF remains set until it is reset by an SCL pulse.

### 3.4 DATA LOGIC

During the read command, the discfile control receives 37-bit data words from the discfile through a sequential bit-by-bit transfer. These words are shifted right in the data accumulator DA2-19 and assembled into 18-bit data characters. Two such characters are parallel-transferred out to the Data Control 136 for each 37-bit input data word. The 37th bit of the input word is a parity bit. The discfile control must distinguish this bit from the data bits and apply it only to the parity accumulator flip-flop PAR, but not to the data accumulator.

During the write command and the read compare command, this process is essentially reversed. The Data Control 136 loads 18-bit data characters into the discfile control data accumulator DA2-19 by parallel transfer. The characters are shifted right and are sequentially available bit-by-bit at DA19. For the write command, two full 18-bit characters are shifted out to the discfile control from DA19, and then a parity bit is sent out from PAR, thus writing a full 37-bit data word. For the read compare command, each data bit is compared on a bit-by-bit basis with a corresponding bit read from the discfile. Every 37th incoming bit from the discfile is a parity bit. These bits are used to check the parity of the incoming data during the read compare, but they are not included in the read comparison operation.

The process of transmitting an address out to the discfile is somewhat similar to the write command, but 20 bits rather than 36 are shifted out before the final parity bit is sent to the discfile. Furthermore, the address source is different from that of the data. Data arrives in 18-bit increments from the Data Control 136 and is loaded into DA2-19 for shifting out the discfile. The address comes directly from the processor to the discfile control without being routed through the Data Control 136. Nineteen of the 21 address bits are loaded into DA0-11 and DA13-19 from the IO bus. (The address bit corresponding to DA12 is always 0, and so can be generated within the discfile control.) The 21st bit of the address is the parity bit. This address parity bit is generated by the discfile control, and is sent out to the discfile as the final bit of the address.

The data logic governs all the discfile control operations described above. The data logic is composed of three basic functional sections: 1) data clock logic; 2) data receiving and transmitting logic; and 3) bit, character, and word control logic.

#### a Data Clock Logic

At each address or data bit, the data clock circuitry generates a sequence of five separate clock pulses: DCK 1, DCK 0, DCK 2, DCK 2.1 and DCK 3. With the exception of DCK 0, which is used only for loading purposes within the clock chain itself, all of these clock pulses initiate various logical functions within the discfile control.

TABLE 3-8 DATA CLOCK LOGIC SUMMARY

<u>Data Clock Chain</u>	<u>Clock for Address Transmission</u>
DCK 1 (-TR:B7)	CLK (-AC:D8)
DCK 0 (-TR:B7)	ADS (-FC:C2)
DCK 2 (-TR:C8)	ACE (-AC:D7)
DCK 2.1 (-TR:C8)	ACS (-AC:D8)
DCK 3 (-TR:C8)	WCE (-TR:D7)
<u>Clock for Write Command</u>	<u>Clock for Read and Read Compare Commands</u>
WRITE CLOCK EVEN (-TR:D5)	RDS (-TR:C6)
WRITE CLOCK ODD (-TR:D5)	CM1(1) (-CM:B2)
WCE (-TR:D7)	SCS(1) (-FC:B6)
WCO (-TR:C6)	WCT7(0) (-WC:A7)
RDS (-TR:C6)	END flip-flop (-CM:B4)
WCT7(0) (-WC:A7)	EDO (-TR:C3)
	EDZ (-TR:C4)
	ODO (-TR:C1)
	ODZ (TR:C2)

During address transmission, the data clock chain is triggered by CLK pulses generated by an R401 variable clock circuit. The ACE and ACS flip-flops make up a two-stage synchronizing network that controls the turn-on and turn-off of the address clock. The same ADS pulse that steps the file-control octoflop to SNA state also sets the ACE flip-flop. The first subsequent CLK pulse sets the ACS flip-flop. Each CLK pulse to arrive while ACS remains set is gated through to produce a WCE clock; that clock in turn triggers the DCK clock chain.

During the read and read compare commands, the data clock chain is triggered by incoming data pulses from the discfile. The four data pulse

inputs EDE, EDO, ODO and ODZ, are ORed together, and provided that the clock is enabled, each data pulse to arrive on any of the four inputs triggers the data clock chain. During read and read compare operations, the clock is enabled by the assertion of the RDS level. The RDS level is asserted when CMI(1) is asserted (specifying a read or read compare command) provided that SCS(1) is asserted (file-control octoflop in SCS state) and WCT7(0) is asserted (sector not yet completed, and if the command is read, END not set).

During the write command, the data clock chain is triggered by WRITE CLOCK EVEN and WRITE CLOCK ODD pulses from the discfile. These WRITE CLOCK pulses are inverted in the discfile control and redesignated WCE and WCO. Provided that RDS is negated (which it is during any write command), and that WCT7(0) is asserted (indicating that the end of the 128-word data sector has not yet been reached), each WRITE CLOCK EVEN and WRITE CLOCK ODD starts the sequence of DCK pulses.

As indicated by the above description, each address bit or data bit processed by the discfile control triggers the DCK clock chain and produces the five-pulse sequence: DCK 1, DCK 0, DCK 2, DCK 2.1, and DCK 3. The DCK entry in the Chapter 8 signal glossary includes a comprehensive table listing all functions performed by each of the five DCK pulses produced by the data clock chain. This table can be referred to to help resolve most questions involving the relative timing of the ordered logical steps making up the operating sequences of the discfile control.



b Data Receiving and Transmitting Logic

Addresses and data are transmitted to and from the discfile on four twisted-pair transmission lines. These four twisted-pair lines are used in sets of two; one line of each set is pulsed for a 1; the other line for a 0. Two such sets of lines are used. This allows alternate bits (odd and even) to be transmitted on different lines, thus halving the data transmission frequency. The even data lines are designated EDO and EDZ (Even Data One and Zero); the odd data lines are designated ODO and ODZ.

TABLE 3-9 DATA RECEIVING AND TRANSMITTING LOGIC SUMMARY

<u>Discfile Interface</u>	<u>Within Discfile Control</u>
EDO (-TR:C3)	RDO (-TR:D2)
EDZ (-TR:C4)	RDZ (-TR:D3)
-----	RDS (-TR:C6)
ODO (-TR:C1)	-----
ODZ (-TR:C2)	SDR (AD:B8) and -AC:C1)
	PAR (-AC:A8)
	MSB (-TR:A2)
	-----

During the write command the WCO and WCE pulses clock alternate bits out to the discfile. Data bits are taken from DA19, parity bits are taken from the PAR flip-flop. Each outgoing bit is amplified by a pulse amplifier and sent to the discfile over the appropriate twisted-pair transmission line. The MSB line provides a terminating supply for the transmission line. The odd-numbered bits are clocked by WCO, and transmitted

over the ODO or ODZ twisted pair (the choice depending on whether the bit is a 1 or a 0). Similarly, the even-numbered bits are transmitted over the EDO and EDZ twisted pairs.

For address transmission somewhat similar operations are executed. The major difference between the transmission of data and the transmission of address information is that no WCO pulses are generated during address transmission. Consequently all 21 address bits are clocked out by the WCE pulses and are transmitted to the discfile over only two of the four twisted-pair transmission lines, the EDO and EDZ lines.

During the read and read compare commands, the process described above is essentially reversed. Data from the discfile enters the discfile control on the four twisted-pair transmission lines. The incoming data pulses on each of the four lines are passed through a pair of series-connected inverters to ensure that they are at the correct voltage reference for use within the discfile control logic. Provided that the RDS level is asserted (indicating that the incoming pulses should be accepted by the discfile control) the odd and even pulses are ORed together to produce RDO and RDZ pulses.

An RDO pulse is generated whenever a 1 bit is read in from the discfile (on either the EDO or ODO line), and an RDZ pulse is generated whenever a 0 bit is read in on either EDZ or ODZ. During the read command, the RDO and RDZ pulses load 1s and 0s respectively into bit DA2 of the data accumulator. During read compare, the RDO pulses complement the RCT

flip-flop. (This is the first complement operation of the read compare operation; provided that DA19 contains a 1, a second complement operation occurs at the SDR pulse.)

An SDR pulse is generated at the DCK 2 pulse corresponding to every address or data bit except parity bits. Besides complementing the RCT flip-flop when DA19(1) is asserted, the SDR pulse shifts the contents of DA0-19 right one bit position. During address transmission only, the contents of DA19 are ring-shifted back into DA0. (Since DA0-19 is directly accessible to the processor by means of the DATAI 270 instruction, this ring-shift feature permits a convenient check on the operation of the accumulator shift logic. It has no direct effect on the address transmission sequence.)

#### c Bit, Character, and Word Control Logic

The bit, character, and word control logic is composed of two counters (BSC0-4 and WCT0-7) and two flip-flops (COH and WDC). These circuits control the sequencing of most operations performed by the discfile control.

TABLE 3-10 BIT, CHARACTER AND WORD CONTROL  
LOGIC SUMMARY

<u>Control Circuits</u>	<u>Levels</u>
BSC0-4 (-AC:C2-5)	BCO (-AC:D1)
WCT0-7 (-WC:A3-7)	WCT7(0) (-WC:A7)
COH (-AD:C6)	RDS (-TR:C6)
WDC (-AD:C7)	
END (-CM:B4)	
<u>Pulses</u>	
	TAKE A CHARACTER (-SC:C7)
	DTC (-AD:D2)
	SND (-AD:C8)
	GIVE A CHARACTER (-SC:C7)
	ESP 1 (-FC:C6)
	ESP 2 (-FC:C8)

The bit-shift counter BSC0-4 is a 5-bit count-of-20 binary counter which starts counting in either the 0 state or the 2 state depending upon whether the discfile control is sending out an address or is executing a data operation (a read, write, or read compare command). During address transmission, the bit-shift counter counts the number of address bits that have been clocked out to the discfile; the overflow level BCO is asserted at the 20th bit. For data operations, the BCO occurs at the 18th bit of each 18-bit data character.

One of the functions that the bit-shift counter performs is to control the parallel transfer of 18-bit data characters between the discfile control and the Data Control 136. During read commands, the TAKE A CHARACTER

pulse is generated at the same DCK 1 pulse that initiates the BCO level. This DCK 1 pulse indicates that the 18th and final bit of the incoming data character has been stored in bit DA2 of the discfile control data accumulator. The TAKE A CHARACTER pulse can thus signal the data control to strobe the character into the low order bits of the data control data accumulator.

Similarly, during the write and the read compare commands, the BCO level indicates that the last bit of the previous character has been shifted out of DA19, and that the discfile control is free to receive another data character from the Data Control 136. The BCO level then enables the DCK 2.1 to initiate a DTC pulse. The DTC pulse in turn produces an SND pulse and a GIVE A CHARACTER pulse. The SND pulse causes the contents of the 18 high order bits of the data control data accumulator to be loaded into bits DA2-19 of the discfile control data accumulator. The GIVE A CHARACTER pulse signals the data control to advance the next 18-bit output character into position for the next output transfer.

The COH and WDC flip-flops are used in conjunction with the bit-shift counter to enable the discfile control to distinguish between parity bits and other address or data bits. These circuits interact in such a manner that the COH flip-flop contains 1 only when an address parity bit (the 21st bit of each address) or a data word parity bit (the 37th bit of each data word) is being, or is about to be, processed; during the processing of all other address or data bits, the COH flip-flop remains in the 0 state.

The WDC flip-flop indicates which of the BCO signals precede parity bits. The WDC is set throughout every address transmission. It is so set because the bit counter overflow that occurs at the 20th address bit always immediately precedes the arrival of the address parity bit (the 21st and final address bit). However, during the data operations (read, write, and read compare) every BCO does not signal the imminent arrival of a parity bit. A separate BCO signal is produced at the end of each of the two 18-bit characters making up the data word. Consequently, during data operations, the WDC flip-flop must be used as a count-of-two counter to enable the discfile control to discriminate between the first data character of the data word and the second. Only the second data character is followed by a parity bit. Therefore the COH flip-flop is set to 1 only at the end of that character.

The WDC flip-flop also determines when the word counter WCT0-7 is to be incremented. The word counter is not incremented at every character, but only at every other character, i. e. at every character during which WDC contains 1. The word counter thus counts the number of 37-bit data words that have been processed during the current data sector. When the word counter reaches its final value of 128 (or, in the case of the read command only, when the END flip-flop is set), the WCT7 flip-flop is set to 1. This ends the assertion of WCT7(0) level, and thus terminates the RDS level. The negation of RDS prevents the generation of any further RDO or RDZ pulses and also shuts off the DCK clock chain.

Five  $\mu$ sec after the last DCK 1 pulse, the R303 integrating delay AB01 times out, generating an ESP 1 pulse which advances the file-control octoflop to SCE state. The ESP 2 pulse that follows 2  $\mu$ sec later either returns the octoflop to CMS state (if additional sectors of data are to be processed), or (if no further sectors are to be processed) resets the octoflop to IDS state, thus ending the current command.

### 3.5 ALARM AND ERROR DETECTION LOGIC

The discfile closes the ALARM relay (applying an ALARM level to the discfile control) when positioner power fails below normal, when there is a malfunction in the flying-head air supply, when ambient temperature rises too high, or when a test mode switch is left in test position during normal operate mode.

The discfile will not close the OPERABLE relay when an ALARM condition is present, nor will it do so if the logic unit or any disc unit is in test mode, nor if the POWER OFF pushbutton at the logic unit is depressed. The OPERABLE condition indicates that there is no ALARM, but the absence of an ALARM does not necessarily show that the discfile is OPERABLE.

TABLE 3-11 ALARM AND ERROR DETECTION LOGIC SUMMARY

<u>Levels</u>	<u>Error-Status Flags</u>	<u>Parity</u>
ALARM (-SC:B2)	FER (-SC:A2)	<u>Accumulator Flip-flop</u>
ALM (-SC:B4)		PAR (-A1:A8)
OPERABLE (-SC:C2)	WLE (-SC:A3)	Read Compare
OPR (-SC:C5)	ADE (-SC:A4)	<u>Test Flip-flop</u>
MRB (-SC:D3)	CME (-SC:A4)	RCT (-SC:A8)
MRG (-SC:D3)	DCE (-SC:A5)	
	PER (-SC:A5)	
<u>Pulses</u>	RCE (-SC:A6)	
WRITE LOCKOUT	DRL (-SC:A6)	
WARNING (-SC:B1)		
ERROR SIGNAL (-SC:B1)	<u>Flip-flop Switch</u>	
ERP (-SC:B5)	EFE (-CM:B4)	

The ALARM and OPERABLE levels are each applied to a switch filter and two series-connected inverters. The resulting logic levels are re-designated ALM and OPR. Whenever the OPR level is negated or the ALM level is asserted, the FER flip-flop is set. The FER flip-flop is also set under various error conditions described below; it thus assembles a number of alarm and error conditions which can be used to request a priority interrupt break.

The discfile sends a WRITE LOCKOUT WARNING to the discfile control whenever the processor has addressed a locked out disc. This pulse arrives at the discfile control with or before the READY pulse and immediately sets both the FER flip-flop and the WLE flip-flop. If the command is a read or read compare, there is no difficulty reading the data



from the locked out discs, and no further error indications result. However, if the discfile control should attempt to execute a write command in spite of the WRITE LOCKOUT WARNING, then the writing or erasure of data is prevented and a data check error is generated. The data check error produces a DC error indication at the discfile and also sends an ERROR SIGNAL to the discfile control.

When the discfile detects any error condition, it sends an ERROR SIGNAL to the discfile control. There the ERROR SIGNAL is inverted and redesignated ERP. The ERP pulse always sets the FER flip-flop. If an ERP pulse occurs during the ADT state of the file-control octoflop, it sets the ADE flip-flop as well as the FER; if it occurs during CMS state, it sets the CME flip-flop; and if it occurs during SCS state, it sets the DCE flip-flop. In this way, the error-status flags FER, ADE, CME and DCE not only tell the programmer that an error has been detected, but furthermore when the error has appeared, and therefore what general class of error has occurred. Indicators at the discfile itself can further categorize the error.

There are three additional error conditions that arise within the discfile control rather than at the discfile. These three conditions are parity error, read compare error, and data request late. The FER flip-flop is not set by any of these conditions. The corresponding flags are designated PER, RCE, and DRL. During the read and read compare commands, the <sup>PAK flip-flop in the</sup> discfile control tests <sup>accumulates and tests</sup> the parity of each incoming data word. The PER flip-flop is set whenever the data word currently being read shows incorrect

Insert Page 3-274 here

if the Data Control 136 is not selected to the discfile control in time to operate upon a forthcoming data sector.

Provided that EFE, the Enable File Error priority interrupt switch (a flip-flop switch) is set to 1, a PIE level is produced whenever FER, PER, RCE, or DRL is set. The resulting priority interrupt request may be used to notify the programmer that an error has occurred.

The MRB (Meter Reading Bad) and MRG (Meter Reading Good) signals originate from pushbuttons at the discfile. The address sequencing relays in the discfile can readily be tested with the aid of a relay test program run from the processor. The program cycles through all the relays in pre-determined order. As each relay is tested, a voltmeter at the discfile indicates whether or not its contact resistance is normal. If the contact resistance is excessive, a high meter reading shows that the relay is bad. The maintenance engineer performing the test should then press the Meter Reading Bad pushbutton; this produces an MRB level at the discfile control. If there is a low meter reading (showing normal contact resistance for the relay under test) the Meter Reading Good pushbutton is pressed to produce an MRG level at the discfile control. The CONI 270 samples the MRB and MRG levels on IOB10 and IOB9 respectively.

parity. During the read command, the RCT flip-flop executes the actual bit-by-bit comparison of input data to output data; the RCE flip-flop indicates errors. Whenever an input data bit read from the discfile fails to match the corresponding output bit from the Data Control 136, the RCT flip-flop causes the RCE flip-flop to be set. The DRL flip-flop is set

### 3.6 PRIORITY INTERRUPT

The processor can assign a priority-interrupt request channel to the discfile control by means of a CONO 270 instruction which sets PIA0-2 to some octal number from 1 to 7. If all three PIA bits are 0, no priority interrupt channel is assigned. By asserting the PIE level the discfile control can request a priority interrupt break on the assigned channel. The PI request is sent to the processor by grounding the appropriate PIR (priority interrupt request) line. The lower the channel number, the higher the priority. Breaks on channel 1 take precedence over all other breaks. Breaks on channel 2 take precedence over all breaks except those on channel 1, etc.

TABLE 3-12 PRIORITY INTERRUPT LOGIC SUMMARY

Flip-flops	Levels
	PIE (-CM:A7)
PIA0-2 (-CM:B7, 8)	PIR1-7 (-CM:A7, 8)
EFE (-CM:B4)	FER(1) (-SC:A2)
	PER(1) (-SC:A5)
	RCE(1) (-SC:A6)
	DRL(1) (-SC:A6)
EES (-CM:B5)	SEF(1) (-SC:A7)
EFR (-CM:B6)	DFR(1) (-FC:B4)
EIS (-CM:B6)	IDS(1) (-FC:B2)
	<u>Pulse</u>
	SCL

The conditions under which the PIE level is asserted are themselves subject to program control. There are four flip-flop switches which determine which of four possible priority interrupt conditions is to be allowed to assert the PIE level. Every CONO 270 instruction sets the four priority interrupt enable switches EFE, EES, EFR and EIS to the states determined by bits 29, 30, 31, and 32 respectively of the CONO 270 instruction. When a given switch flip-flop is set to 1, the corresponding interrupt condition (or conditions) is(are) gated through to assert PIE; when the switch is left in the 0 state, the input condition is not allowed to produce a PIE.

The priority interrupt conditions that can be enabled to generate PIE are summarized in Table 3-13 below.

TABLE 3-13 PRIORITY INTERRUPT CONDITIONS

CONO 270 Bit No.	Sets Switch	Permitting Interrupt Condition(s) to Assert PIE
29	EFE	FER(1) ∨ PER(1) ∨ RCE(1) ∨ DRL(1)
30	EES	SEF(1)
31	EFR	DFR(1)
32	EIS	IDS(1)

The FER(1) level is asserted whenever the FER flip-flop is set; this occurs for all alarm and error conditions that arise at the discfile. The remaining interrupt conditions enabled by the EFE switch represent three additional error conditions that arise within the discfile control:

parity error, read compare error, and data request late.

The SEF flag is set 2  $\mu$ sec after the file-control octoflop is advanced to SCE state. The SEF remains set until it is reset by an SCL pulse.

The primary purpose of SEF is to save the SCE state for sampling. Even though SCE is no longer asserted, a 1 in SEF lets the programmer know that the end of the data sector has been passed.

The DFR(1) level is asserted for 1 msec after the discfile has found the addressed sector. The resulting priority interrupt request is often used to notify the programmer that the discfile control may need a command.

The IDS(1) level is asserted whenever the file-control octoflop is reset to IDS state. The resulting priority interrupt request often is used to notify the programmer that the discfile control has completed the preceding command and is ready to receive a new data address.

## CHAPTER 4

### SYSTEM OPERATING SEQUENCES

#### 4.1 ADDRESS TRANSMISSION (Figure 4-1)

The address transmission sequence is the series of operations by which the Discfile Control 270 accepts a 19-bit address from the PDP-6 processor, and transmits a 21-bit address to the Discfile 5022. The address transmission sequence is initiated by a DATAO 270 instruction from the processor. The entire sequence occurs during the portion of the file-control octoflop cycle that precedes ADT state (refer to Figure 3-1).

##### a Load DA0-19

The IOB DATA CLR pulse of the DATAO 270 instruction starts the address transmission sequence. Provided that the file-control octoflop is in an appropriate state (IDS or ADT) and that the MCL pushbutton is not being operated, the IOB DATA CLR produces a CDA pulse, thus clearing the discfile control data accumulator in preparation for the receipt of a new address from the processor.

One microsecond later, the IOB DATA SET pulse arrives. The same conditions that enabled the generation of CDA also enable the generation of PTA. The PTA pulse sends a SELECT to the discfile, clears the discfile control by generating FCL and SCL, and loads a new address into bits DA0-19 of the data accumulator. Nineteen of these 20 address bits arrive from the processor on the IO bus. The remaining bit, DA12, is

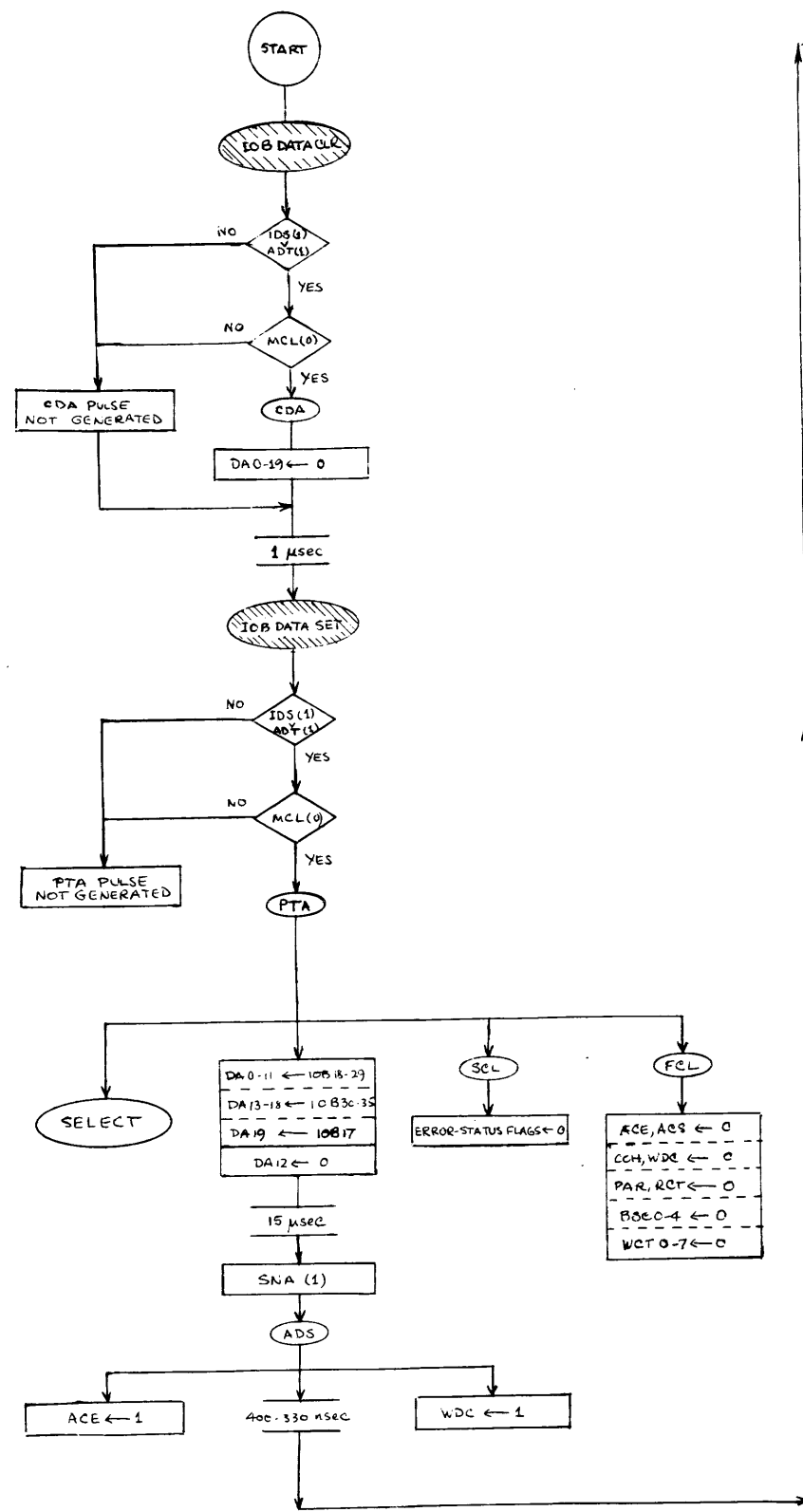
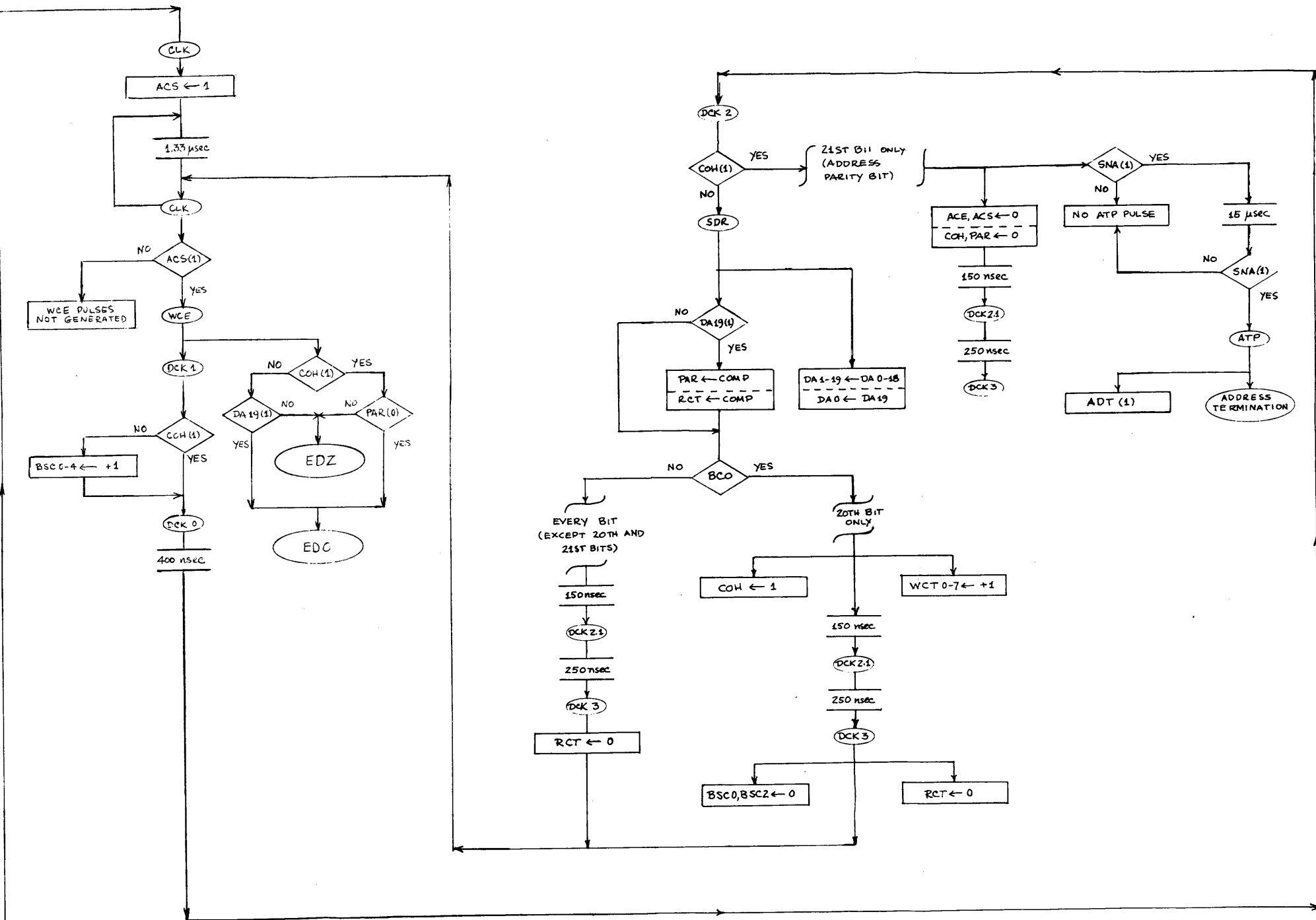


FIGURE 4-1 ADDRESS TRANSMISSION SEQUENCE



KEY:  
 INPUT PULSES TO 270 --- [Hatched Box]  
 OUTPUT PULSES FROM 270 --- [Empty Box]  
 270 INTERNAL CONTROL PULSES --- [Circle]



always 0, and thus can be generated within the discfile control.

#### b Clock Turn-on

The PTA pulse starts a 15- $\mu$ sec delay. The expiration of this delay steps the octoflop from IDS (or ADT) state to SNA state, and produces the ADS pulse. The ADS pulse sets the ACE flip-flop and the WDC flip-flop. The ACE and ACS flip-flops make up a synchronizing network that controls the turn-on and turn-off of the address clock. The ADS pulse starts the turn-on sequence by setting the ACE flip-flop. The first CLK pulse to be generated after ACE is set sets ACS. The internal address clock (within the discfile control) produces one CLK pulse every 1.33  $\mu$ sec, and each CLK that occurs while ACS(1) is asserted produces a WCE pulse.

The set of the WDC flip-flop by the ADS pulse governs the subsequent setting of the COH flip-flop; the COH(1) level enables the discfile control to detect the occurrence of the address parity bit and to distinguish it from the preceding 20 bits of the address.

#### c Address Transmission

All address bits are transmitted to the discfile over the even data twisted-pair transmission lines as EDO and EDZ pulses. The 21 WCE pulses that occur during the time that the ACS flip-flop remains set clock out the 21 bits of the address from the discfile control to the discfile. Each WCE pulse also starts the DCK clock chain, thus producing DCK 1, DCK 0, DCK 2, DCK 2.1, and DCK 3 in that order.

For the first 20 bits of the address, COH(1) is not asserted. Consequently, the contents of DA19 are transmitted to the discfile as the

current address bit and then the bit-shift counter BSC0-4 is incremented at DCK 1 time. For the final 21st bit of the address, COH(1) is asserted and the bit-shift counter is not incremented. The 21st address bit is the address parity bit that enables the discfile to check the address transmission. The source of the address parity bit is not DA19, but is rather the complement of the PAR flip-flop, the circuit that generates both address and data parity within the discfile control.

#### d Shift Address and Generate Parity

The DCK 1 pulse initiates DCK 0, and that pulse in turn produces DCK 2 after a 400-nsec delay. The COH(1) level is asserted during only that DCK 2 pulse that is initiated by the final 21st bit of the address (the parity bit). All other DCK 2 pulses that occur during the address transmission sequence (the 20 DCK 2 pulses corresponding to the 20 address bits that precede the parity bit) produce SDR pulses. The SDR pulse causes the contents of the data accumulator to be shifted right one bit position. The contents of DA19 are ring-shifted back into DA0. This ring-shift feature does not affect the actual address transmission to the discfile, but it does provide a useful maintenance aid for the discfile control. After the address transmission to the discfile is finished, the original address should be completely restored in DA0-19. There it can be sampled from the processor (by a DATAI 270 instruction) in order to test the operation of the data accumulator shift circuitry.

Besides shifting the contents of DA0-19 right, the SDR pulse may also complement the PAR flip-flop and the RCT flip-flop. The SDR

complements PAR and RCT whenever DA19 contains 1 before the shift. The complement of RCT is a don't-care condition during address transmission; its usefulness is confined to the read compare instruction. The FCL pulse ensures that the PAR flip-flop starts in the 0 state at the beginning of the address transmission. The PAR is then complemented at any SDR pulse that follows the transmission of a 1 address bit. In this way, PAR accumulates the parity of the address word. By transmitting PAR(0) as the 21st address bit, the discfile control ensures that the total address word transmitted to the discfile (including the parity bit) has odd parity.

#### e Bit-shift Counter Overflow

The return loop (designated "following every bit except the 20th and 21st") includes the remaining two pulses of the DCK clock chain, DCK 2.1 and DCK 3 and also includes the reset of RCT. Neither these two pulses nor the RCT reset have any logical relevance to the address transmission sequence; they are don't-care conditions included on the flow chart for maintenance purposes only.

The operations described above are identically repeated 19 times during the transmission of the first 19 bits of the address. Each CLK produces a WCE pulse; the WCE in turn transmits one address bit to the discfile and initiates the DCK clock chain.

At the DCK 1 pulse that is initiated by the 20th address bit, the bit-shift counter BSC0-4 is incremented to 20, and the overflow level BCO is asserted. The assertion of BCO causes the DCK 2 and DCK 3 pulses

that correspond to the 20th address bit to perform certain additional functions not performed during the preceding 19 bits of the address. These additional functions are all included in the right-hand ("yes") branch of the flow chart following the BCO decision box.

Most of these BCO "yes" functions can be considered to be don't-care conditions. (The clearing of WCT0-7 and of BSC0,2 is unnecessary, because the WCT and BSC counters are cleared by FCL before the beginning of the first subsequent command sequence; the RCT clear is relevant only during read compare commands.)

The set of the COH flip-flop is, however, directly relevant to the address transmission sequence. The address termination functions initiated by the assertion of the COH(1) level are described below.

#### f Address Termination

The final 21st CLK of the address transmission sequence produces a final 21st WCE pulse. Because COH(1) is then asserted, that WCE pulse transmits the address parity bit taken from PAR(0) rather than the contents of DA19. The same WCE initiates the DCK clock chain for the last (21st) time during the address transmission. Because of the assertion of COH(1), the DCK 1 pulse does not increment BSC0-4.

At DCK 2, the assertion of COH(1) prevents the generation of SDR and instead causes the execution of the additional functions shown at the "yes" side of the COH(1) decision box (following DCK 2). The ACE and ACS flip-flops are reset, turning off the address clock. The clock turn-off prevents the generation of any further WCE pulses and so prevents any further triggering of the DCK clock chain.

The same DCK 2 pulse that resets ACE and ACS also starts a 15- $\mu$ sec delay. Termination of this delay produces the ATP pulse. Note that the ATP pulse can be generated only if the file-control octoflop remains in SNA state until the completion of the 15- $\mu$ sec

delay. (In the unlikely event that an IOB reset pulse were to be applied to the discfile control during the 15- $\mu$ sec delay, it would be necessary to prevent the generation of ATP.) The ATP pulse advances the octoflop from SNA state to ADTstate, and sends an ADDRESS TERMINATION pulse to the discfile over the odd data one's line. This completes the address transmission sequence.

#### 4.2 WRITE COMMAND (Figure 4-2)

The write command is the series of operations by which the Discfile Control 270 transmits one or more sectors of output data to the Discfile 5022. The entire write command occurs during the portion of the file-control octoflop cycle lying between the CSP pulse and the ESP 2 pulse (refer to Figure 3-1).

The Discfile Control 270 receives output data from the Data Control 136 in data characters of 18 bits. The discfile control then transmits the data to the Discfile 5022 in serial form, one bit at a time, over four twisted-pair transmission lines. These four twisted-pair lines are used in sets of two; one line of each set is pulsed for a 1, the other for a 0. Two such sets of two lines are used. This allows alternate bits (odd and even) to be transmitted on different lines, thus halving the data generation frequency.

After transmitting each set of 36 data bits, the discfile control generates and transmits an accompanying parity bit to the discfile. The discfile writes the data in the form of 37-bit data words, each such word containing the 36 data bits and a parity bit of the correct value to yield odd parity for the entire 37-bit word.

### a Sector-Start Operations

Most of the sector-start operations shown at the left of Figure 4-2 are common to all three commands, read, write, and read compare. (The only non-common operations are the DTC, SND and GIVE A CHARACTER pulses which are initiated by the CSP pulse during the write and read compare commands but not during the read command.) During the write command, the CSP pulse that advances the file-control octoflop from ALS state to CMS state produces a DTC pulse. That pulse in turn generates SND and GIVE A CHARACTER. The SND pulse causes the contents of the 18 high-order bits of the Data Control 136 data accumulator to be loaded into bits DA2-19 of the discfile control data accumulator. (This is the first character that will be transmitted bit-by-bit to the discfile for writing.) The GIVE A CHARACTER pulse signals the Data Control 136 that the discfile control has accepted the character currently stored in the high order end of the data control data accumulator (by clocking it in with an SND pulse), and that the data control should bring the following character into position to be transferred out.

The CSP pulse also sends either a READ or a WRITE pulse to the discfile, the choice depending upon the state of the CM1 command code bit. During the write command CM1 contains 0, so a WRITE pulse is sent to the discfile, commanding the discfile to write out the following sector of data.

Besides advancing the octoflop to CMS state, the CSP pulse also starts a 200- $\mu$ sec delay. The expiration of this delay produces the NDP 1 pulse.

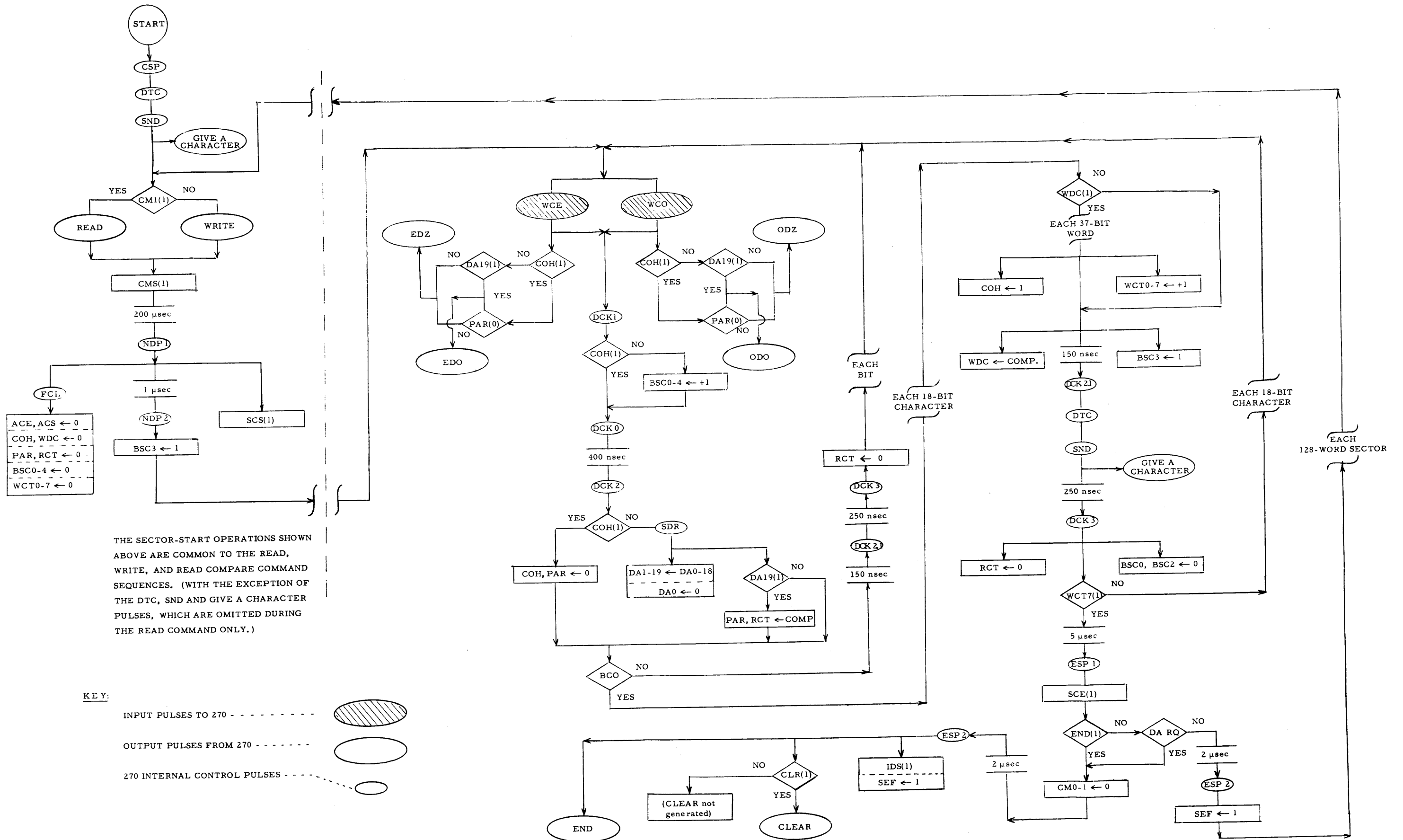


FIGURE 4-2 WRITE COMMAND - WRT; CM0(1), CM1(0)



The NDP 1 pulse advances the octoflop to SCS state and produces the FCL pulse which clears the control flip-flops and registers of the discfile control. One microsecond after the NDP 1 pulse, the NDP 2 pulse sets bit BSC3 of the bit-shift counter. This ensures that the bit-shift counter starts the forthcoming data sector with its contents equal to 2. Since the counter overflows at a count of 20, this means that it overflows after counting 18 bits, the number of bits in a single data character. The sector start operations thus leave the discfile control in an appropriate state to begin writing the first word of the current sector of data.

b Operations That Recur at Each Bit That Is Written

The write command is synchronized to WCE and WCO pulses initiated by WRITE CLOCK EVEN and WRITE CLOCK ODD pulses generated at the discfile and transmitted to the discfile control over two twisted-pair transmission lines. The COH flip-flop contains 1 only during the final bit of each 37-bit data word (the parity bit). During the transmission to the discfile of the 36 data bits that precede the parity bit, COH(1) is not asserted. Consequently, these 36 data bits are taken from the contents of DA19. When DA19 contains 1, a 1 bit is transmitted to the discfile; the WCE pulse then sends the discfile an EDO pulse, or else the WCO pulse sends the discfile an ODO pulse. Similarly, when DA19 contains a 0, a 0 bit is transmitted to the discfile in the form of either an EDZ or an ODZ pulse.

The final bit of the 37-bit word transmitted to the discfile is the parity bit. This data-word parity bit is generated in much the same way

that the address parity bit is generated during the address transmission sequence described in the previous section. The COH flip-flop contains 1 when the parity bit is transmitted to the discfile. If PAR(0) is asserted, a 1 parity bit is transmitted as the 37th bit of the data word; if PAR(0) is not asserted, a 0 parity bit is transmitted.

Besides clocking out a data or parity bit to the discfile, every WCE pulse and every WCO pulse also triggers the DCK clock chain. As a result, there is a full set of DCK clock pulses corresponding to each bit transmitted to the discfile during the write command. The bit-shift counter BSC0-4 is incremented at every DCK 1 pulse except those corresponding to parity bits (when COH(1) is asserted).

Every DCK 2 pulse except those corresponding to parity bits initiates an SDR pulse. The SDR pulse shifts the data accumulator right one bit-position, and shifts a 0 into DA0. If DA19 contained 1 prior to the shift (i. e. if a 1 data bit has just been transmitted to the discfile), then the SDR pulse also complements the PAR flip-flop and the RCT flip-flop. The PAR complement accumulates parity for the current data word. During write commands the RCT complement is a don't-care condition; it is relevant only during the read compare command. The same is true of the RCT clear at DCK 3 time. The DCK 2 pulse corresponding to the final bit of the 37-bit word (the parity bit) clears both COH and PAR in preparation for the next word to be written.

### c End of Character and End of Word

At the DCK 1 pulse corresponding to the 18th bit of each data character, the bit-shift counter is incremented to its overflow value of 20, and the BCO level is asserted. The assertion of BCO causes the DCK 2, DCK 2.1 and DCK 3 pulses that correspond to the 18th bit of the data character to perform certain additional functions not performed during the preceding 17 bits. These additional functions are all included in the "yes" branch of the flow chart following the BCO decision box (the right-hand portion of Figure 4-2).

The WDC flip-flop was cleared at the FCL pulse, so WDC(1) is not asserted during the first data character of the sector. The first character thus bypasses the COH set and the WCT0-7 increment operations. (This bypass is necessary because COH is set and the word counter incremented only at the end of a 37-bit data word, and not at the end of the first of the two 18-bit data characters included in the data word.)

When BCO is asserted, the same DCK 2 pulse that produces SDR also complements WDC and sets BSC3. The WDC flip-flop acts as a count-of-two counter. It is incremented (complemented) at the DCK 2 pulse corresponding to the final data bit of every 18-bit data character. The WDC contains 1 only during the second data character of the data word. Consequently, it can provide the necessary screening condition for allowing COH to be set and WCT0-7 to be incremented. (These two operations are executed at the end of the second data character of each data word, but not at the end of the first.)

The BSC3 set adds two to the contents of the bit-shift counter. This is done in order to enable the bit-shift counter to start the following count in the proper state. By adding two to the overflow count already in the counter, DCK 2 momentarily raises the contents of the counter to 22; however, the DCK 3 pulse that occurs 400 nsec later clears both BSC0 and BSC2, and thus subtracts 20 from the contents of the counter, leaving it in the 2 state for the beginning of the next count sequence. This ensures that the counter will again overflow at the 18th bit of the subsequent data character (when its contents once more reach the overflow value of 20).

The DCK 2 pulse is followed 150 nsec later by DCK 2.1. The DCK 2.1 pulse produces the DTC pulse. That pulse in turn generates SND and GIVE A CHARACTER. The SND pulse causes the contents of the 18 high order bits of the Data Control 136 data accumulator to be loaded into bits DA2-19 of the discfile control data accumulator. (This is the next character that will be transmitted bit-by-bit to the discfile.) The GIVE A CHARACTER pulse signals the Data Control 136 that the discfile control has accepted the character currently stored in the high order end of the data control data accumulator. The DCK 3 pulse also clears RCT. This is a don't care condition during the write command; it is relevant only during read compare.

The BCO level is again asserted at the 36th bit of each data word (the 18th bit of the second data character of the word). The same operations occur that are described above, and in addition to those operations, two more:

the COH flip-flop is set, and the word counter WCT0-7 is incremented. The set of COH enables the discfile control to distinguish the following bit (the 37th bit of the data word) as the parity bit. The incrementing of the word counter reflects the fact that one full data word (with the exception of the parity bit) has been transmitted to the discfile for writing.

The set of the COH flip-flop causes COH(1) to be asserted during transmission of the final 37th bit of the data word. Three results follow:

- 1) The output bit transmitted to the discfile is taken from PAR(0) rather than from DA19(1);
- 2) The bit-shift counter is not incremented; and
- 3) Instead of SDR being generated at DCK 2, the COH and PAR flip-flops are cleared at that time.

The entire sequence described above is repeated for each of the 128 data words making up the data sector being written. This is true even though the output data from the Data Control 136 may be exhausted before the full 128 words are written. In that event, the discfile control transmits 0s in lieu of data bits (and 1s for parity bits) for the remainder of the sector. At the last data bit of the 128th word of the sector, the word counter is incremented to its final value of 128. The WCT7(1) level is then asserted and the discfile control breaks out of the loop and executes the end-of-sector operations described below.

#### d End of Sector

As soon as WCT7(1) is asserted, indicating that the word counter has reached its final value of 128, the DCK clock chain is turned off. (Because the WCE and WCO pulses are not inhibited, the parity bit of the final

data word can still be transmitted to the discfile even after the DCK clock chain is turned off.)

Five microseconds after the final DCK 1 pulse of the sector, an integrating delay times out, producing the ESP 1 pulse. The ESP 1 advances the file-control octoflop from SCS state to SCE state. If the END flip-flop is not set, and if furthermore DA RQ is not asserted (indicating that the Data Control 136 still has more output data to send) the command continues for one or more additional sectors. Two microseconds after the ESP 1 pulse an ESP 2 pulse is generated. The ESP 2 pulse sets the sector end flag SEF to indicate to the programmer that the end of the first sector has been reached. The SEF remains set until being cleared by an SCL pulse. The ESP 2 pulse also returns the file-control octoflop from SCE state to CMS state and simultaneously sends a second WRITE pulse to the discfile, thereby initiating the sector-start operations for the second sector of data that is to be written.

The WRITE pulse automatically causes the discfile to increment its stored address by 1. The next sector is therefore at the next consecutive address following that at which the previous sector was written. This process can be continued for up to 44 consecutive sectors of data without any new DATAO 270 command being given. Note, however, that the programmer must keep count of the number of sectors that have been written since the last change of disc or position address. If more than 44 sectors are written without a new DATAO 270, data will be written over and thus destroyed.

At the end of the first sector during which the END flip-flop is set or the DA RQ level is asserted, the discfile control terminates the write command in the manner described below.

#### e Terminate Write Command

If, when the discfile control reaches the end of a sector, END is set, or DA RQ is asserted, then the ESP 1 pulse clears the two command code bits CM0-1. Two microseconds later the ESP 2 pulse resets the file-control octoflop from SCE state to IDS state and sends an END pulse to the discfile. If the CLEAR flip-flop is set, the ESP 2 pulse also sends a CLEAR pulse to the discfile.

### 4.3 READ COMMAND (Figure 4-3)

The read command is the series of operations by which input data is read in from the discfile. The entire read command occurs during the portion of the file-control octoflop cycle lying between the CSP pulse and the ESP 2 pulse (refer to Figure 3-1).

The Discfile 5022 starts to read data at the beginning of the 128-word sector addressed by the preceding DATAO 270 instruction. The data is loaded into DA2 as it is read in serial fashion, one bit at a time, and is then shifted right until a full 18-bit data character is stored in DA2-19. At the conclusion of this loading process, the discfile control sends a TAKE A CHARACTER pulse to the Data Control 136, causing the data control to strobe the character into its low order accumulator bits, and if necessary, to shift it left to make room for the second character of the data word. A





similar process is followed for the second 18-bit character and all succeeding data characters. Every 36 data bits from the discfile are followed by a parity bit, and the parity of each data word is checked at the discfile control.

#### a Sector-Start Operations

The sector-start operations shown at the left of Figure 4-3 are common to all three commands, read, write and read compare. The read command sector start operations differ from those of the write and read compare commands in only one respect: during the read command the CSP pulse does not produce DTC, SND and GIVE A CHARACTER (as it does during write and read compare). These three pulses are omitted during the read command because there is no need during that command to send output data from the Data Control 136 to the discfile control. Refer to paragraph 4-2a above for a description of the write command sector start operations.

#### b Operations That Recur at Each Bit That Is Read

The read command is synchronized to the read-data pulses from the discfile. These pulses are transmitted to the discfile control over four twisted-pair transmission lines. The EDO and ODO pulses bring in the 1 bits, and the EDZ and ODZ pulses bring in the 0 bits. So long as the read command continues, each read data pulse to arrive at the discfile control triggers the DCK clock chain. As a result, there is a full set of DCK clock pulses corresponding to each bit transmitted to the discfile control during the read command.

In flow chart Figure 4-3, the operations that recur at each bit that is read are shown below the four read data input pulses from the discfile: EDO, ODO, EDZ, and ODZ. Note that there are three major branches of the flow chart below these input pulses. The branch directly below the EDO and ODO pulses represents the results that are produced directly by the arrival of a 1 bit from the discfile; the branch directly below the EDZ and ODZ pulses shows the direct results of the arrival of a 0 bit from the discfile. The center branch reflects the triggering of the DCK clock chain and includes all the effects of the five DCK clock pulses, DCK 1, DCK 0, DCK 2, DCK 2.1 and DCK 3.

At each EDO or ODO pulse from the discfile that arrives while RDS is asserted, the DCK clock chain is triggered, and an RDO pulse is generated, indicating that a 1 bit (either a data bit or a parity bit) has been read in from the discfile. If RDS is not asserted, the triggering of the DCK clock chain is prevented, and so is the generation of RDO.

The read command is unlike the other two commands, write and read compare, in that it may be terminated at any point within a sector by merely setting the END flip-flop. (This can be done by giving a CONO 270 instruction with a 1 in bit 23.) The first DCK 1 pulse to occur after END is set sets WCT7, and thereby ends the assertion of RDS. The negation of RDS turns off the DCK clock chain as described above, and also prevents the generation of both the RDO and the RDZ pulses.

The left branch of the Figure 4-3 flow chart (immediately below the EDO and ODO inputs from the discfile) shows the generation and results

of the RDO pulses. Every RDO pulse complements the parity accumulator flip-flop, PAR, thus accumulating the parity of the incoming data word (by counting the number of 1 bits read into the discfile control). If the parity of the incoming word is correct (odd), the PAR flip-flop ends the word (after the 37th bit, the parity bit, is read in) in the 1 state. If PAR is not in the 1 state at the end of the incoming data word, a parity error is indicated.

The COH flip-flop contains 1 only during the final bit of each 37-bit data word (the parity bit). During the transmission to the discfile control of the 36 data bits that precede the parity bit, COH(1) is not asserted. Provided that the COH flip-flop contains 0, the RDO pulse performs two additional functions: it sets DA2 and complements RCT. The set of DA2 reads the incoming 1 bit into the left end of the discfile control data accumulator. (The complement of RCT is a don't-care condition during the read command; it is relevant only during the read compare command.) The right branch of the Figure 4-3 flow chart (immediately below the EDZ and ODZ inputs from the discfile) shows the generation and results of the RDZ pulses. If the COH flip-flop contains 0, the RDZ pulse loads a 0 into DA2, otherwise RDZ has no effect.

Whenever RDS is asserted, each EDO, ODO, EDZ and ODZ pulse triggers the DCK clock chain. The DCK 1 clock pulse is the first pulse of the DCK clock chain (center branch of Figure 4-3 flow diagram). The effects of the DCK 1 clock depend on the state of the END flip-flop and the COH flip-flop. The END flip-flop is set to 1 only when the read

command is to be terminated immediately. The first subsequent DCK 1 pulse then sets WCT7. The set of WCT7 ends the assertion of RDS, thereby preventing the generation of any further RDO or RDZ pulses and also preventing any further triggering of the DCK clock chain. (The final sequence of DCK clock pulses, that sequence beginning with the DCK 1 pulse that sets WCT7, is of course completed without interruption; a final DCK 0, DCK 2, DCK 2.1, and DCK 3 follow the last DCK 1 pulse.)

If the END flip-flop is not in the 1 state, the discfile control is periodically required to generate a TAKE A CHARACTER pulse at DCK 1 time. This pulse is generated at that DCK 1 pulse that corresponds to the final bit of each 18-bit data character read from the discfile. (Note that the BSC = 19 condition is used to enable the generation of this pulse rather than the normal overflow count of 20. This is done because the TAKE A CHARACTER pulse is generated by the same DCK 1 clock pulse that increments the bit-shift counter to the overflow count of 20.) The TAKE A CHARACTER pulse signals the data control that the discfile control has presented a 19-bit input character to the low order strobe data inputs of the data control data accumulator. This indicates to the data control that it may strobe the character in, and that if required it should shift the character left to make room for the next character.

The bit-shift counter BSC0-4 is incremented at every DCK 1 pulse except those corresponding to parity bits (when COH(1) is asserted). Every DCK 2 pulse except those corresponding to parity bits initiates an SDR pulse. The SDR pulse shifts the discfile control data accumulator

right one bit-position, and shifts a 0 into DA0. If DA19 contained 1 just prior to the shift, the SDR pulse complements RCT. (The RCT complement is a don't-care condition during the read command; it is relevant only during read compare. The same is true of the RCT clear at DCK 3 time.) The DCK 2 pulse corresponding to the final bit of the 37-bit word (the parity bit) tests the parity of the word and sets the parity error flip-flop PER if the parity accumulator flip-flop PAR is left in the 0 state (indicating that the parity is incorrect). The same DCK 2 also clears both COH and PAR in preparation for the next word to be read.

#### c End of Character and End of Word

At the DCK 1 pulse corresponding to the 18th bit of each data character, the bit shift counter is incremented to its overflow value of 20, and the BCO level is asserted. The assertion of BCO causes the DCK 2, DCK 2.1, and DCK 3 pulses that correspond to the 18th bit of the data character to perform certain additional functions not performed during the preceding 17 bits. These additional functions are all included in the "yes" branch of the flow chart following the BCO decision box (the right-hand portion of Figure 4-3).

Because these read command end-of-character and end-of-word functions are quite similar to the corresponding functions that are performed during the same phases of the write command, the present paragraph does not repeat the full description of the common operations, but instead describes only the few operations of the read command that differ from the write command. A comparison of the right hand portions of

Figures 4-2 and 4-3 illustrates the basic similarity of the two commands and also reveals the few respects in which they differ.

The read command flow chart includes an extra step at the DCK 2 pulse corresponding to the 36th data bit of each word. If after that DCK 2 pulse the WCT7 flip-flop contains 1 (indicating that the WCT counter has been incremented to its final value of 128), then the RDS level ceases to be asserted. (This decision is not included in the write command, because the RDS level is never asserted during write.)

Following the DCK 2.1 pulse, the read command omits the DTC pulse and the resulting SND and GIVE A CHARACTER pulses that are generated during the write command. These pulses are omitted during read because the direction of data flow is opposite to that during write. (The read command produces TAKE A CHARACTER pulses at DCK 1 time rather than GIVE A CHARACTER pulses at DCK 2.1.)

#### d End of Sector

The read command end-of-sector operations are almost identical to the corresponding operations of the write command. There is only one difference. The read command does not include the DA RQ decision box that causes the write command to terminate at the end of the first sector during which output data is exhausted. The read command always continues until the END flip-flop is set. If END is not set, the read command reads the contents of the 44 sequentially addressed data sectors at the discfile's presently addressed disc and position, and continues to reread the same 44 sectors of data until a new address is given. At the end of

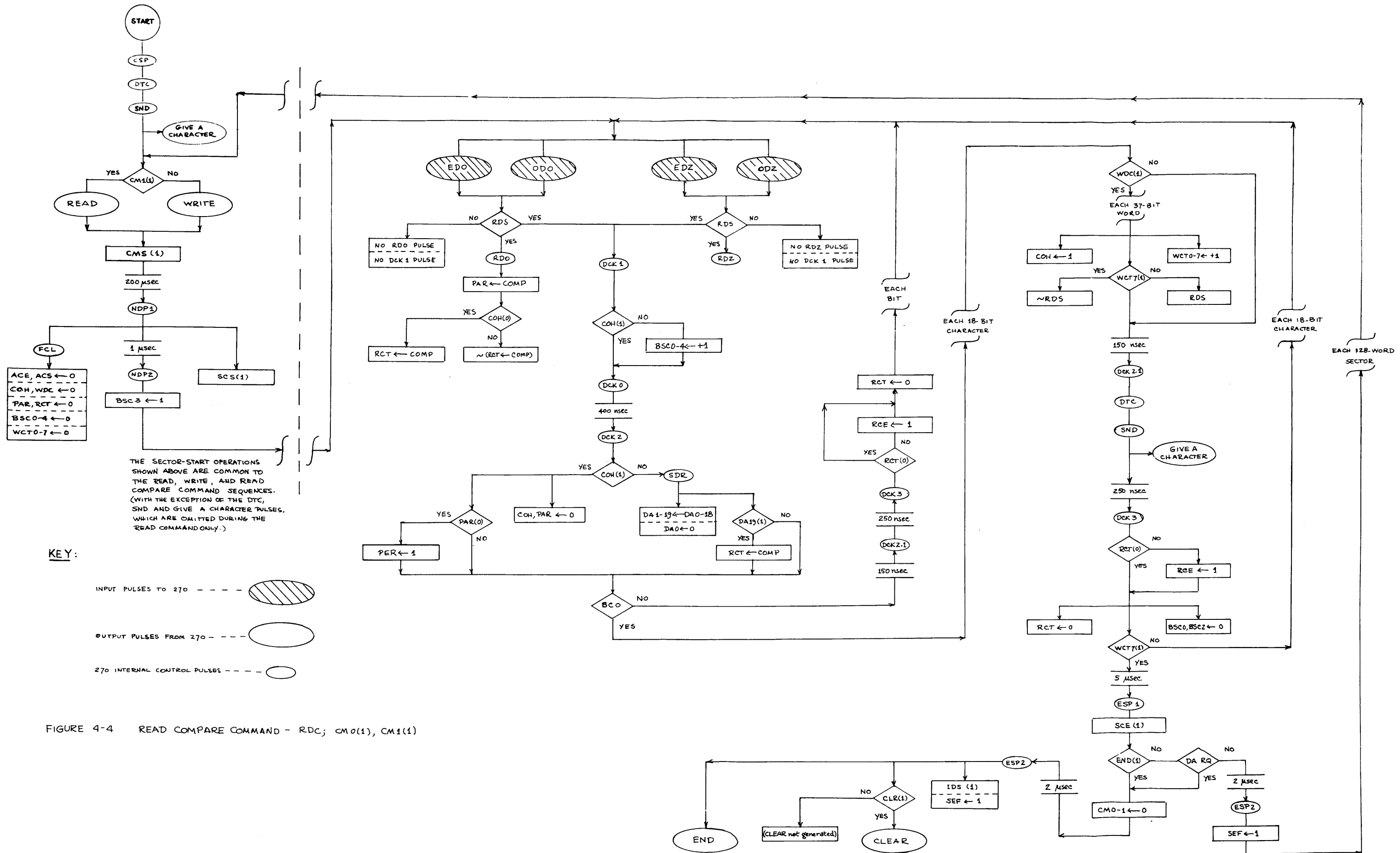
each sector another READ pulse is sent to the discfile, and the discfile address is incremented by 1. (The discfile logic contains a count-of-44 address counter, which cycles through the 44 sector addresses in rotation.)

#### 4.4 READ COMPARE COMMAND (Figure 4-4)

The read compare command is the series of operations by which the discfile control compares output data from the processor with corresponding input data read from the discfile. The entire read compare command occurs during the portion of the file-control octoflop cycle lying between the CSP pulse and the ESP 2 pulse (refer to Figure 3-1).

The comparison is executed on a bit-by-bit basis, but does not include parity bits. The output data is sent to the discfile control through the Data Control 136 (as during the write command described above), and the input data is brought in from the discfile (as during the read command described above). The discfile starts to read data at the beginning of the 128-word sector addressed by the preceding DATAO 270 instruction.

The RCE flip-flop in the discfile control is set whenever an output data bit from the Data Control 136 fails to match the corresponding input data bit read from the discfile. No output parity bits are generated during read compare commands, and for read comparison purposes the incoming parity bits from the discfile are ignored. Note, however, that the incoming data from the discfile is subject to the normal parity test during the read compare command just as during the read command.





#### a Sector Start Operations

The sector-start operations shown at the left of Figure 4-4 are common to the write and read compare commands. For a description of these operations refer to paragraph 4-2a above.

#### b Operations That Recur at Each Bit That is Compared

The read compare command is very similar to the read command, and in most operations where it differs from the read command it is similar to write. Consequently, the present paragraph does not give a full description of the common operations, but instead describes only the few features of the read compare command that distinguish it from the read command described above. A comparison of Figure 4-4 with Figures 4-3 and 4-2 illustrates the basic similarities of the read compare command to the read and write commands, and also reveals the differences between the read compare and the other two commands. Like the read command, the read compare command is synchronized to the read-data pulses from the discfile: EDO, ODO, EDZ and ODZ. Although these incoming pulses are allowed to produce RDO and RDZ pulses whenever RDS is asserted, the RDO and RDZ pulses are not allowed to load data into the data accumulator as they do during the read command.

The RDZ pulse is not used during read compare. The RDO pulse complements the parity accumulator PAR as during the read command. Provided that the COH flip-flop is in the 0 state (indicating that the current bit is a data bit, not a parity bit, and hence is subject to read comparison) each RDO pulse also complements the RCT flip-flop. This is the first of

the two RCT complement operations that make up the comparison. The second RCT complement operation is initiated at DCK 2 time by the SDR pulse provided that DA19 contains a 1.

The two sets of complement operations work together to effect the bit-by-bit read comparison. If both the input and the output data are 0 bits, RCT will not be complemented at all, but will remain in its initial 0 state. If both bits are 1, the end result is the same; although RCT is complemented twice, it is still left in the 0 state after the DCK 2 pulse. However, if the input and output data bits are different, RCT is complemented only once, and is therefore left in the 1 state after DCK 2. The RCE flip-flop is then set by the DCK 3 pulse, thus saving the read compare error indication. The DCK 3 pulse clears RCT after each data bit comparison to prepare the discfile control for the next bit comparison. Once the RCE flip-flop is set, however, it remains set until cleared by an SCL pulse.

Like the write command, the read compare command always continues to the end of a 128-word data sector. It cannot be terminated in mid-sector by setting the END flip-flop as can the read command. Consequently the read compare flow chart (Figure 4-4) omits the DCK 1 set of WCT7 (enabled by END) that is included in the read command flow chart (Figure 4-3). The read compare command also omits the generation of TAKE A CHARACTER at DCK 1 time. The TAKE A CHARACTER pulse is omitted because during read compare no input data is sent to the Data Control 136.

With the exceptions described above, the remaining operations that recur each bit during the read compare command are substantially identical to those that occur during the read command.

c End of Character and End of Word

These operations are almost identical to the corresponding operations that occur during the write command. However, the read compare command, like the read command, includes an extra step at the DCK 2 pulse corresponding to the 36th data bit of each word. If after that DCK 2 pulse the WCT7 flip-flop contains 1 (indicating that the WCT counter has been incremented to its final value of 128), then the RDS level ceases to be asserted. (This decision is not included in the write command, because the RDS level is never asserted during write.) The read compare command also includes an extra step at every DCK 3 pulse (including those DCK 3 pulses that occur at the end of each data character and each data word). This extra step is the RCE set that occurs whenever RCT contains 1 at DCK 3 time.

d End of Sector

The read compare command end-of-sector operations are identical to the corresponding operations of the write command; refer to paragraph 4-2 above.

## CHAPTER 5

### MAINTENANCE

#### 5.1 GENERAL

The Discfile Control 270 and the Discfile 5022 are ordinarily used as peripheral systems of the PDP-6 installation. The maintenance chapters of the PDP-6 Circuits manual and the PDP-6 Processor and Memory manuals include maintenance procedures and suggestions of general relevance not repeated in this manual. Familiarity with this material is essential for the efficient maintenance of the discfile control, the discfile, and all other DEC systems used with the PDP-6. The topics covered include: Tools and Test Equipment, Removal and Replacement of Modules, Module Troubleshooting, Use of Marginal Check, System Troubleshooting, and Maintenance Logs.

#### CAUTION

The procedures described in the maintenance chapters of the PDP-6 Circuits manual and the PDP-6 Processor and Memory manuals should be thoroughly understood before undertaking troubleshooting and repair of the Discfile Control 270 and the Discfile 5022.

#### 5.2 USE OF DRAWINGS

The complete system logic of the Discfile Control 270 is shown in the seven engineering logic drawings of Chapter 9. Because these engineering logic drawings are the most frequently used source of

troubleshooting information, it is important to be familiar with the conventions and symbols which they employ.

Figure 8-1 shows the standard cabling and module location numbering used within the DEC FLIP CHIP logic racks.

### 5.3 EQUIPMENT LAYOUT

The discfile control logic is contained in three DEC FLIP CHIP mounting panels designated from top to bottom A-B, C-D, and E-F. Within the A-B rack, the upper row of FLIP CHIP modules is designated A, and the lower row B; similarly row C is the upper row of the C-D rack, and row E is the upper row of the E-F rack. Each row has 32 module positions numbered from left to right. Thus, for example, module B7 is the seventh module from the left end of the lower row in the top FLIP CHIP logic rack. The module location and use are shown in the two module location diagrams in Chapter 9, UML-D270-0-11 (Sheets 1 and 2). Circuit schematics of all 27 FLIP CHIP module types used in the discfile control logic are presented in order of module type number in Chapter 9.

### 5.4 PREVENTIVE MAINTENANCE OF DISCFILE CONTROL 270

The cooling fan in the bottom of the bay should be checked daily for proper operation and free flow of air. Under normal operating conditions, the air filter at the bottom of the bay should be changed and cleaned monthly. The correct procedure for changing and cleaning filters is described in the PDP-6 processor manual maintenance chapter.

Preventive maintenance procedures for the system logic should also be scheduled on a regular basis. The same considerations that call for preventive maintenance of the PDP-6 processor apply equally to the peripheral systems. Appropriate maintenance procedures will detect and eliminate most potential malfunctions before they can cause operating errors. Refer to PDP-6 processor manual for suggested procedures and schedules. The same basic techniques that are used in maintaining the processor (trouble isolation methods, maintenance programs, marginal check, etc.) are equally useful for maintaining the discfile control and interface units.

#### 5.5 PREVENTIVE MAINTENANCE OF DISCFILE 5022

Routine scheduled preventive maintenance procedures normally require about 8 man-hours per month. This maintenance should be performed by suitable trained and competent customer personnel. The schedule for routine preventive maintenance should be in accordance with the preventive maintenance procedures recommended by Data Products Corporation in the Discfile Instruction Manual and Customer Information Bulletins; refer to paragraph 1.5 above, REFERENCE DOCUMENTS.

If parts and maintenance personnel are available, unscheduled maintenance normally will not exceed an average repair time of one hour per month per 5022 discfile. Spare parts should be functionally interchangeable with like assemblies, sub-assemblies, and replaceable parts as found within the system. They should also be physically interchangeable, one with another. A list of spare parts is supplied to the customer.

## 5.6 ADJUSTMENT AND CALIBRATION

The Discfile Control 270 contains seven adjustable delays and an RC-coupled variable clock. Normally no adjustment or calibration of these circuits is required. They are set to the proper time constants and frequency before the system leaves the factory and there is no appreciable drift. It is desirable to check the delay time constants and the clock frequency once after the system is installed. Thereafter adjustment and calibration should be undertaken only if necessary. These procedures should not be made a part of routine maintenance schedules.

Calibration of all seven delays is done with a screwdriver adjustment and an oscilloscope. The R302 one-shot delay has two delays per module. The adjustment screws are both located at the edge of the card; one at the top, the other at the bottom. The R303 delay module includes only one delay; the adjustment screw is also at the edge of the card. The R401 clock module is calibrated to the correct pulse repetition frequency by an adjustment screw at the edge of the card.

TABLE 5-1 DISCFILE CONTROL DELAY TIME CONSTANTS

Delay Controls	Remarks	Module and Output Terminal	Module Type	Time Constant
ADS	PTA to ADS	B09-M	R302	15 $\mu$ sec
ATP	Precedes ATP	B09-V	R302	15 $\mu$ sec
-----				
CSP	ALP to CSP	B07-V	R302	15 $\mu$ sec
DFR	DFR duration	B07-M	R302	1.0 msec
-----				
ESP 1	Integrating delay senses absence of DCK 1 clock	AB01-BS	R303	5.0 $\mu$ sec
-----				
ESP 2	ESP 1 to ESP 2	B06-M	R302	2.0 $\mu$ sec
NDP 1	Precedes NDP 1	B06-V	R302	0.2 msec

TABLE 5-2 DISCFILE CONTROL ADDRESS CLOCK FREQUENCY AND PERIOD

Output Pulses	Frequency pps	Period
CLK	750 kc	1.33 $\mu$ sec



## 5.7 PROGRAM-CONTROLLED PULSE GENERATION

Three bits of the CONO 270 instruction are reserved for the purpose of generating certain pulses within the discfile control. These program-controlled pulses are useful for maintenance purposes.

**TABLE 5-3 PROGRAM-CONTROLLED PULSES**

When a 1 is Coded in CONO Bit:	The following Discfile Control Pulse(s) are Initiated by the PTC pulse	Function of Pulse
19	DTC	Generates GIVE A CHARACTER.
	SND	Causes the contents of the 18 high order bits of the Data Control 136 data accumulator to be loaded into bits DA2-19 of the discfile control data accumulator.
	GIVE A CHARACTER	Causes the Data Control 136 to advance a new character into position for transfer out to the discfile control.
20	TAKE A CHARACTER	Causes the Data Control 136 to strobe the 18-bit character in DA2-19 into the low order bits of its data accumulator and (if necessary) to shift the character left 18 bit-positions.
28	SCL	The SCL pulse clears the nine error-status flags ADE, CME, DCE, DRL, FER, PER, RCE, SEF, and WLE.

## 5.8 MAINTENANCE PROGRAMS

The MAINDEC 670 program MAGNETIC DISC TEST provides a comprehensive set of test procedures for detecting and isolating malfunctions in the discfile and the discfile control. The test procedures include individual component tests as well as complete system tests.

The MAINDEC 670 program consists of a compiler and disc exerciser routines. Operation is under control of DDT. The program contains numerous routines to manipulate data. It is stored on a single 16K DECtape File. The file contains a 5633-word data buffer, DDT, the test program, and selected portions of the symbol table. A more detailed description of the MAINDEC 670 program is distributed with the program.

## 5.9 RECOMMENDED SPARE PARTS

The most economical quantity of spare parts to be maintained depends on the requirements of the individual user, but the following listing is suitable for most installations.

### a Module Spares

Suggested quantity of spares: one module of each type.

<u>Module</u>	<u>Quantity in Discfile Control 270</u>
B155	1
B171	1
G980	5
R001	4
R002	1

<u>Module</u>	<u>Quantity in Discfile Control 270</u>
R107	7
R111	20
R151	1
R181	2
R201	3
R202	9
R203	6
R205	11
R284	2
R302	3
R303	1
R401	1
R601	2
R602	6
R603	8
W005	2
W100	5
W101	10
W300	1
W607	1
W640	1
W700	1

b Component Spares

<u>Component</u>	<u>Total Quantity in all Modules</u>	<u>Suggested Quantity of Spares</u>
DEC2894-1	89	16
DEC2894-3	17	10
1N645	2116	48

<u>Component</u>	<u>Total Quantity in all Modules</u>	<u>Suggested Quantity of Spares</u>
1N3605	190	20
1N3606	2583	54
2N3009	5	6
2N3639	376	24
16J1	40	12

c Mechanical Spares

<u>Part Number and Description</u>	<u>Suggested Quantity of Spares</u>
53E168, Type CFG: Rotron fan with #2R blade	1
X-1431, 10" x 10" x 2" EZ Kleen Filter	1
Type 418 Super Filter Coat, pints	1

## CHAPTER 6

### INSTALLATION AND PREOPERATIONAL CHECKOUT

#### 6.1 SITE SELECTION

Before installing the discfile control and discfile, select a suitable location near the PDP-6 arithmetic processor. The discfile control should be located within 25 feet of the processor, and the discfile should be located within 25 feet of the discfile control.

The discfile control is located in a cabinet 69-1/2 inches high, 22-1/4 inches wide, and 27-1/8 inches deep. A 3-foot clearance should be allowed on all sides of the equipment for access during maintenance. A level floor is required because the equipment frames are mounted on casters. The floor should be capable of supporting 150 psf. The system is designed to operate efficiently from 50° to 100°F. The plug-in modules are cooled by blowing air out the front of the bay. No additional cooling equipment is required.

The discfile control runs on ordinary 115-volt, 600 cycle current. A 10-ampere line is sufficient. The discfile control power cable is equipped with a Hubble Twist-Loc 3-prong, 30-ampere, 250-volt plug. Although the discfile control draws only about 3 amperes in normal operation, turn-on surges may reach almost 5 amperes, and system power capacity should be planned accordingly.

## 6.2 UNPACKING

The discfile control cabinet is shipped on a skid and may be crated or not, depending on the mode of transportation. For truck shipment, it may be left uncrated. A crate is furnished for air shipment. The crate is approximately 74 inches high, 27 inches wide, and 32 inches deep. The skid upon which it rests is about 6 inches high and 3 feet square. Interconnecting cables are specially made up for each installation and are ordinarily shipped with the equipment.

1. If the discfile control is crated, carefully remove all crating and strapping, and any packing material. If the unit is shipped uncrated, remove the skid and any protective padding.
2. The plenum doors at the rear of the bay have spring catches. To reinforce these doors during shipment, two bolts are used to hold each door shut. Remove these bolts and store them in the plastic loops provided.
3. Remove any packing material, shipping blocks, etc. from the inside of the discfile control cabinet.
4. The plug-in modules are taped into the mounting panels to prevent damage in shipment. Remove the tape.

NOTE: If the user plans to reship the equipment (or to move it more than a short distance) in the near future, special containers and packing materials should be saved for reuse. These items are designed especially to accommodate the equipment and are the safest means of packing it for reshipment.

### 6.3 INSPECTION

The discfile control is thoroughly tested and checked before it leaves the factory. However, the discfile control should be inspected and checked again when installed to make sure that no damage has occurred during shipment. After the equipment is unpacked, check the following:

1. Have all the shipping blocks, packing materials, tape, etc. been removed? If not, remove them.
2. Are all plug-in units inserted firmly in position? Secure any that are loose.
3. Are there any loose nuts or bolts? If so, tighten them.
4. Are there any loose or broken wires? If so, repair them.

### 6.4 CABLE CONNECTIONS

Complete the inspection procedure as given above before connecting the cables.

1. Route the four cables from the PDP-6 processor into the cabinet, and connect the two W028 cable connectors at the end of each processor cable to the corresponding receptacles at the left of mounting panel E-F. The eight cable connectors can be plugged in either positions E4-7 and F4-7 or E11-8 and F11-8, depending on the layout of the specific installation. These positions are paralleled as shown in Figure 6-1 and as listed in Table 6-1.

MCV SWITCHES

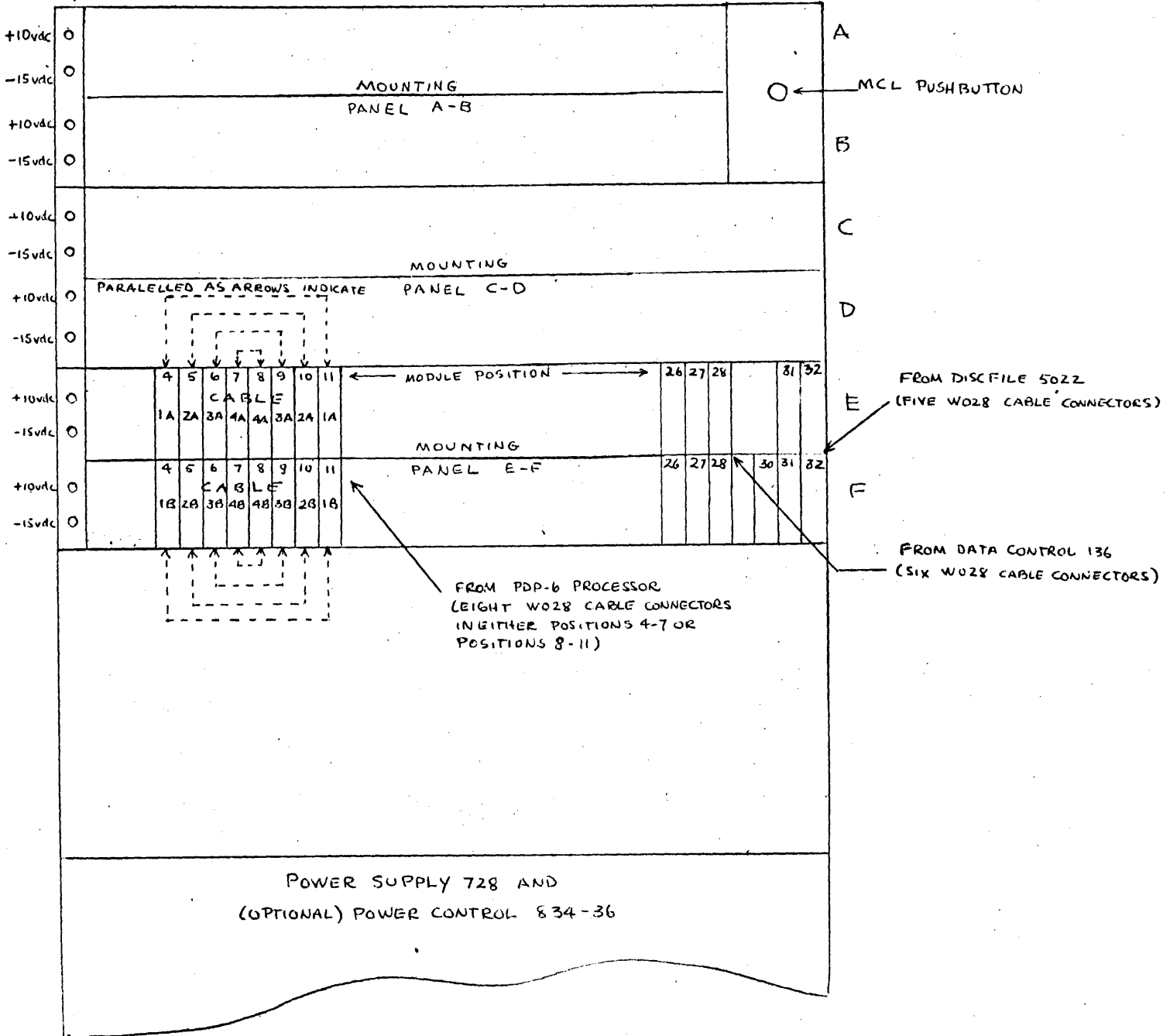


FIGURE 6-1 FRONT VIEW LAYOUT, DISCFILE CONTROL 270



CAUTION

It is essential that each of the eight W028 cable connectors be connected to the correct parallel pair of receptacles. The cable connectors should each be marked with the correct cable number. Check this cable number against Table 6-1 below or against module location diagram UML-D-270-0-11-sheet 2.

TABLE 6-1 PROCESSOR CABLE CONNECTIONS

Cable Connector	To Position	Or To Paralleled Position
1A	E4	E11
1B	F4	F11
2A	E5	E10
2B	F5	F10
3A	E6	E9
3B	F6	F9
4A	E7	E8
4B	F7	F8

2. Route the three cables from the Data Control 136 into the cabinet, and connect the six W028 cable connectors at the cable ends to positions E26-28 and F26-28 as shown in UML-D-270-11-sheet 2.
3. Route the cable from the <sup>5022</sup>discfile into the cabinet, and connect the five W028 cable connectors at the cable end to positions E31-32 and F30-32 as shown.
4. Secure the tie-down brackets over all cable connectors to prevent them from being accidentally loosened or dislodged.

5. A coiled ac power cable is taped to the fan at the bottom of the bay. Remove the tape and route the power cable out through the hole in the bottom of the bay, but do not plug it in.

## 6.5 POWER CONTROLS

To perform the preoperational check-out of the discfile control, the operator should be familiar with the controls described below.

### a. Power Control Type 834-836 (Optional Equipment)

There are two controls on this unit, a circuit breaker and a LOCAL/REMOTE switch. When the switch is in the LOCAL position, the processor has no effect on discfile control power turnon. Power can then be turned on or off by means of the circuit breaker. The LOCAL position is used primarily for maintenance purposes.

For normal operation, it is usually more convenient to leave the circuit breaker on and the switch in the REMOTE position. Discfile control power is then controlled by the processor. When the processor is turned on, power is also applied to the discfile control. If the circuit breaker is turned off, no power is applied to the discfile control regardless of the position of the LOCAL/REMOTE switch.

### b MCV Switches

There are four MCV (Marginal Check Voltage) switches at the left of each mounting panel. The top switch in each set governs the +10 vdc power lines for the upper row of modules, the second switch governs the -15 vdc lines for the upper row of modules, the third and bottom switches respectively govern the +10 vdc and -15 vdc lines for the lower row of modules.

This arrangement is an aid to troubleshooting because it permits selective application of marginal check voltages. In the FIXED position (down), each MCV switch connects the associated module row to the fixed supply voltage from the internal 728 Power Supplies. In the MARGINAL position (up), each MCV switch connects the associated module row to the variable MCV voltage from the processor. This variable MCV voltage can be adjusted at the MCV controls over the operator's control panel of the PDP-6.

### 6.6 PREOPERATIONAL CHECKOUT

Before using the discfile control, make sure that the system turns on and off properly and that the correct voltages are present at all mounting panels. The following check-out procedure should be carried out after completing the cable connections described under Cable Connections. All voltages are measured from chassis ground with a Multimeter (Simpson Model 260A, Triplet Model 630NA, or equivalent).

1. Put the LOCAL/REMOTE switch in LOCAL position.
2. Turn power circuit breaker OFF.
3. Plug in power cable to 110-volt ac outlet.
4. Put all MCV switches in FIXED position.
5. Turn power circuit breaker ON.
6. Check the fixed (internal) supply voltages at terminals A, B, and C of the modules that occupy the extreme right positions (viewed from the front) in both the upper and lower module rows of each mounting panel.

<u>Terminal</u>	<u>Voltage</u>
A	+10 vdc
B	-15 vdc
C	(Ground)

The +10-vdc fixed supply voltages should be between +9.5 vdc and +11.5 vdc. The -15 vdc should be between -14.5 vdc and -16.5 vdc.

If either voltage falls outside the specified range, the 728 Power Supply probably needs maintenance.

7. With the PDP-6 processor turned off, put the LOCAL/REMOTE switch in the REMOTE position. Check each of the two fixed voltages at the terminals specified in step 6. No voltage should be present.
8. Turn on the PDP-6 processor. Again check the two fixed voltages. The same voltage noted in step 6 should be present at each of the terminals checked.
9. Put the LOCAL/REMOTE switch in the LOCAL position.
10. Put the MCV switches that control the +10-vdc lines (top switch and third switch at the left of each mounting panel) in the MARGINAL position.
11. Make the following settings at the MCV controls above the PDP-6 operator's control panel:
  - a. Set polarity switch to +10-volt position.
  - b. Adjust Variac until marginal check voltage meter indicates +5 vdc.

12. Check the +10-vdc voltage at the terminals specified in step 6. It should coincide with the +5-vdc voltage shown on the marginal check voltage meter.
13. Return the MCV switches for +10 vdc to the FIXED position.
14. At the PDP-6 MCV controls, set the MCV polarity switch to the -15-volt position and adjust the Variac until the marginal check voltage meter indicates -8 vdc.
15. Set the MCV switches which control the -15-vdc lines (second switch and bottom switch at the left of each mounting panel) to the MARGINAL position.
16. Check the -15-vdc voltage at the terminals specified in step 6. It should coincide with the -8-vdc voltage shown on the marginal check voltage meter.
17. Return the MCV switches for -15 vdc to the FIXED position.
18. Return the LOCAL/REMOTE switch to REMOTE.
19. Return the polarity switch at the PDP-6 to the off position.
20. Turn off the PDP-6.

CHAPTER 7  
PROGRAMMING

This chapter tabulates the coding of the four I/O instructions used with the Discfile Control 270, and gives a listing and brief explanation of five short subroutines.

7.1 INSTRUCTION CODING

The discfile system is programmed by applying the four basic PDP-6 I/O instructions to the Discfile Control 270. The coding and bit-significance of each of these four instructions are tabulated in Tables 7-1 through 7-4 below.

a DATAI 270 Instruction

The DATAI 270 instruction permits the processor to sample the contents of the data accumulator DA0-19 and the contents of the bit-shift counter BSC0-4. This instruction is used primarily for maintenance purposes.

TABLE 7-1 DATAI 270 CODING

Bit No.	Samples	Bit No.	Samples	Bit No.	Samples
11	DA12	19	DA1	28	DA10
12	BSC0	20	DA2	29	DA11
13	BSC1	21	DA3	30	DA13
14	BSC2	22	DA4	31	DA14
15	BSC3	23	DA5	32	DA15
16	BSC4	24	DA6	33	DA16
		25	DA7	34	DA17
17	DA19	26	DA8	35	DA18
18	DA0	27	DA9		

b CONI 270 Instruction

The CONI 270 instruction permits the processor to sample the contents of the command buffer, the file-control octoflop, the nine error-status flags, and five miscellaneous signals: MCL, MRG, MRB, ALM, and  $\sim$ OPR. The instruction is perhaps most frequently used for sampling the states of the error-status flags and the file-control octoflop, but it also provides a useful aid for maintenance. Note that the CONI 270 bits that sample the command buffer do not correspond to the CONO 270 bits that load the command buffer; the CONI 270 instruction samples the buffer into the left half of the word, but the buffer is loaded from the right half of the CONO instruction (see Table 7-2 below).

TABLE 7-2 CONI 270 CODING

CONI Bit No.	Samples Command Buffer Flip-flop or Miscellaneous Signal Marked with an *.	Set by CONO Bit No.
3	MCL* Master Clear	
4	CLR Clear	22
5	END End	23
6	xxx (Presently unused)	
7	CM0 Command Code Bit 0	25
8	CM1 Command Code Bit 1	26
9	MRG* Meter Reading Good	
10	MRB* Meter Reading Bad	
11	EFE Enable File Error	29
12	EES Enable End of Sector	30
13	EFR Enable File Ready	31
14	EIS Enable Idle State	32
15	PIA0 Priority Interrupt Assignment Bit 0	33
16	PIA1 Priority Interrupt Assignment Bit 1	34
17	PIA2 Priority Interrupt Assignment Bit 2	35

TABLE 7-2 CONI 270 CODING (continued)

CONI Bit No.	Samples File-Control Octoflop State	
18	IDS	Idle State
19	SNA	Select New Address
20	ADT	Address Terminated
21	DFR	Discfile Ready
22	ALS	Alert State
23	CMS	Command Selected
24	SCS	Sector Started
25	SCE	Sector End
-----		
CONI Bit No.	Samples Error-Status Flag or Miscellaneous Signal Marked With *	
26	DCE	Data Clock Error
27	CME	Command Error
28	WLE	Write Lock Error
29	ADE	Address Error
30	ALM*	ALARM
31	DRL	Data Request Late
32	RCE	Read Compare Error
33	PER	Parity Error
34	FER	File Error
35	~OPR*	NOT OPERABLE

c DATAO 270 Instruction

The DATAO 270 instruction loads a 19-bit address from the processor into the data accumulator of the Discfile Control 270, and then causes the discfile control to transmit a 21-bit address to the Discfile 5022. (One of the two additional bits is DA12; this bit is always 0, so it can be generated within the discfile control. The second additional bit is the address parity bit, also generated within the discfile control.) After receiving all 21 bits of the address, the discfile initiates an address seek operation to locate the data sector specified by the address.



The discfile control can accept a DATAO 270 instruction only when the file-control octoflop is in either the IDS state or the ADT state, and when furthermore the MCL pushbutton is not operated.

TABLE 7-3 DATAO 270 CODING

DATAO Bit No.	Is Loaded Into	DATAO Bit No.	Is Loaded Into
17	DA19 (Read-Next- Sector Bit)	27	DA9
18	DA0	28	DA10
19	DA1	29	DA11
20	DA2	--	DA12 (Loaded with 0 generated within discfile control)
21	DA3		
22	DA4	30	DA13
23	DA5	31	DA14
24	DA6	32	DA15
25	DA7	33	DA16
26	DA8	34	DA17
		35	DA18

d CONO 270 Instruction

The processor sends 15 bits of control information to the discfile control at each CONO 270 instruction. Twelve of these 15 control bits are loaded into the command buffer. The remaining three control bits set no flip-flops in the discfile control, but are instead used directly as control inputs.

Note that a CONO 270 instruction to the discfile control will not affect the command code bits CM0 and CM1 unless the Change Commands Enable level CCE is asserted. This level is not asserted when any of the following conditions are present:

ALM	ALARM (discfile in alarm state)
~OPR	NOT OPERABLE (discfile not operable)
ALS	Alert State

CMS	Command Selected State
SCS	Sector Started State
SCE	Sector End State

The command codes can be changed at any of the first four states of the file-control octoflop cycle, IDS, SNA, ADT, or DFR state, but once the ALP pulse has advanced the octoflop to ALS state, no further change of command code is permissible.

TABLE 7-4 CONO 270 CODING

CONO Bit No.	Sets Command Buffer Bit (except *)	Logical Function
19	Direct Control Input*	When coded 1, produces DTC, SND, and GIVE A CHARACTER pulses at PTC time. (Loads an 18-bit character from the Data Control 136 into the discfile control.)
20	Direct Control Input*	When coded 1, produces a TAKE A CHARACTER pulse at PTC time. (Signals the Data Control 136 to accept an 18-bit character from the discfile control.)
21	Presently unused*	
22	CLR	Causes the current command to terminate at the end of the first 128-word data sector that is processed, and sends the discfile an END and a CLEAR at ESP 2 time.
23	END	Causes the current command to terminate at the end of the first 128-word data sector that is processed, and sends the discfile an END at ESP 2 time.
24	Presently unused*	

TABLE 7-4 CONO 270 CODING (continued)

CONO Bit No.	Sets Command Buffer Bit (except *)	Logical Function															
25	CM0	Command Code bit 0															
26	CM1	Command Code bit 1															
		<table border="1"> <thead> <tr> <th>CM0</th> <th>CM1</th> <th>Command Specified</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>NOP - No Operation</td> </tr> <tr> <td>0</td> <td>1</td> <td>RED - Read</td> </tr> <tr> <td>1</td> <td>0</td> <td>WRT - Write</td> </tr> <tr> <td>1</td> <td>1</td> <td>RDC - Read Compare</td> </tr> </tbody> </table>	CM0	CM1	Command Specified	0	0	NOP - No Operation	0	1	RED - Read	1	0	WRT - Write	1	1	RDC - Read Compare
CM0	CM1	Command Specified															
0	0	NOP - No Operation															
0	1	RED - Read															
1	0	WRT - Write															
1	1	RDC - Read Compare															
27	Presently unused*																
28	Direct Control Input*	When coded 1, produces an SCL pulse at PTC time. (Clears the nine error-status flags: ADE, CME, DCE, DRL, FER, PER, RCE, SEF, and WLE.)															
29	EFE	Enables FER(1), PER(1), RCE(1), or DRL(1) to initiate a priority interrupt request.															
30	EES	Enables SEF(1) to initiate a priority interrupt request.															
31	EFR	Enables DFR(1) to initiate a priority interrupt request.															
32	EIS	Enables IDS(1) to initiate a priority interrupt request.															
33	PIA0	The discfile control is assigned a priority interrupt request channel corresponding to the octal contents of PIA0-2. The lower the channel number, the higher the priority. Channel 1 has the highest priority, channel 7 the lowest. If all three PIA bits are left 0, no priority interrupt channel is assigned.															
34	PIA1																
35	PIA2																

## 7.2 PROGRAMMING EXAMPLES

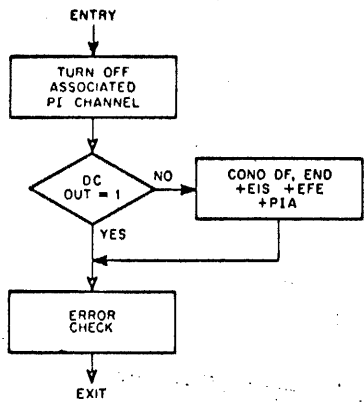
Five representative examples are included here to illustrate how the discfile programming information given above is used. The examples are intended to acquaint persons new to PDP-6 with several standard programming techniques. The reader is urged to review the programming discussions for the priority interrupt and input-output systems and the 136 Data Control in F-65 (pp. 40, 41-43 and 65-58) before proceeding.

Example 1: Interrupt service routine for the 136 Data Control on BLKO/BLKI overflow.

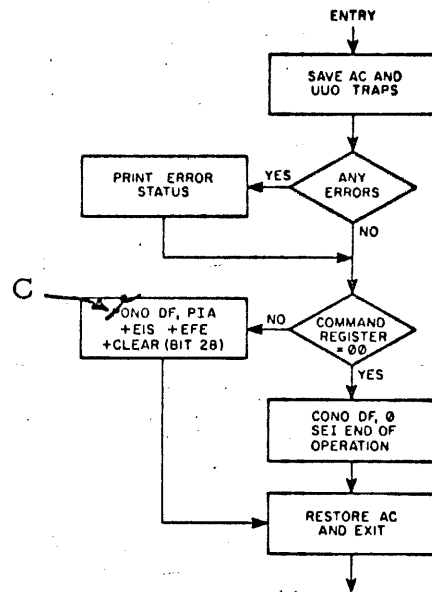
DCINT: 0	JSR at PI channel stores PC.
CONO PI 1000 + PIA	PIA signifies a bit for one of the seven PI channels
CONSO DC, OUT	Turn off PI channel.
CONO DF, EIS + EFE + PIA + END Bit	Send END signal if reading.
CONSZ DC, DCLB	Check DC error flag.
JSR ERROR	Go to an error routine.
JEN,@ DCINT	EXIT.

The first example is a subroutine that returns the discfile's 136 Data Control to inactive status upon completion of a block data transfer (BLKO or BLKI). When the last word is transferred, a jump to this subroutine (JSR) will occur. The 1000 in the first CONO instruction sets a 1 in bit 26 of the PI effective address, which turns off the PI channel specified by the PIA bits (see F-65, p. 41).

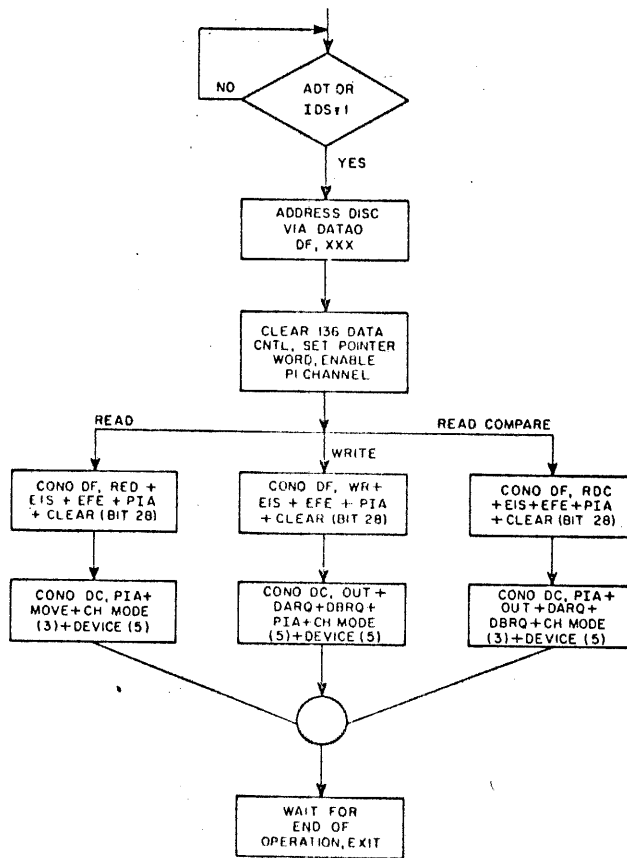
The significant feature of this program occurs at the decision block labeled DC OUT = 1 on the accompanying flow chart (Figure 7-1). The CONSO DC, OUT instruction says that if bit 26 of the control register is 0 (0 = In = write), skip the next instruction which turns off the discfile. The discfile turns itself off automatically except when reading.



Example 1  
Data Control Interrupt Service



Example 2  
Discfile Interrupt Service



Examples 3, 4 and 5  
Read, Write, Read-Compare

Figure 7-1 Programming Examples

The remaining instructions check the DC error flag (DATA CLOBBERED bit 23). A 1 causes a jump to an error subroutine; all 0's permit a skip to the final jump and enable instruction, which causes the program to resume at DCINT using information at the PC location.

**Example 2: Discfile interrupt service routine.**

<pre> DFINT: 0         MOVEM, DFSAVE         CONI DF, 0         CONSZ DF, 1777         JSR ERROR         TLNE RED + WR         JRST DFINT2         CONO DF, 0         MOVE, DFSAVE         JEN, @ DFINT DFINT2: CONO DF, EIS + EFE + 200 + PIA         JRST DFINT2-2 </pre>	<pre> JSR at PI channel stores PC. Save AC 0. Get status. Check error flags. Go to error routine. If command register is cleared, TERMINATE OPERATION. CLEAR DISC FILE. Restore AC. EIT, operation complete. Clear error flags. AND continue. </pre>
---	--

The second programming example gives an instruction sequence for terminating a TRANSFER at the 270 Discfile Control. The first instruction saves the contents of accumulator zero. The following three instructions get discfile status and check for errors just as in the previous example. Next, the left half of the command register is tested for 1's in the read and write bit positions. If no operation is set, the discfile is cleared. If an operation is in progress, the error flags are cleared via DFINTZ (CONO DF, + Bit 28) where 200 octal is clear bit 28. After the AC is restored, control reverts to the instruction indicated by the PC back at DFINT.

The remaining three examples show the three principal discfile operations read, write, and read compare, to be variations on a single theme (see flow diagram). All three begin with a wait cycle which lasts until the

discfile is free from any operation already in progress. When discfile status goes from busy to IDLE or ADDRESS TERMINATED, the address contained in UWO location 40 is transmitted to the discfile. The next instruction causes a jump to subroutine INIT which initializes the 136 Data Control and discfile control, that is, clears the 136 and sets up their PI channels. When the initialization subroutine is complete, a CONO Discfile sets up the required operation, read, write or read compare. The octal number 200 in the CONO Discfile instruction signifies bit 28, the clear bit. Octal 350 in the CONO DC instruction sets 1's in bits 28, 29, 30 and 32 of the 136 command register, signifying packing mode 3 (18-bit word), device number 5 (the discfile) DARQ and DBRQ are mnemonics for bits 25 and 26 of the 136 command register. Notice that in the read compare routine, the CONO DC instruction is the same as for write, where in both cases "out" means the 136 receives data from the CP. In the read compare case, however, the 270 Control Unit is conditioned to read. The result is that a data word read from the discfile into the 270 meets a data word from the 136 where the two are compared one bit at a time in the 270.

Data control uses character mode 3, device 5 to transfer disc information. Routines assume a BLKO for write and read compare, a BLKI for read in the interrupt location.



**Example 3:** Read, called via UUO, effective address of UUO equals DISC ADDRESS.

**DFRED:** 0  
 CONSO DF, IDS + ADT  
 JRST .-1  
 DATAO DF, 40  
 JSR INIT  
 CONO DF, RED + 200 + EIS + EFE + PIA  
 CONO DC, 350 + MOVE + PIA  
 JRST EXIT

JSR PC stored by UUO subroutine  
 Wait if operation  
 in progress.  
 Send disc address.  
 Jump to initialize subroutine INIT, below.  
 Command disc.  
 Setup 136 Data Control.

**Example 4:** Write

**DFWRT:** 0  
 CONSO DF, IDS + ADT  
 JRSR, .-1  
 DATAO DF, 40  
 JSR INIT  
 CONO DF, WR + 200 + EIS + EFE + PIA  
 CONO DC, OUT + DARQ + DBRQ + 350 + PIA  
 JRST EXIT

JSR PC stored by UUO subroutine  
 Wait if operation  
 is in progress.  
 Send disc address.  
 Jump to initialize subroutine INIT, below.  
 Command disc.  
 Setup 136 Data CNT control.

**Example 5:** Read Compare

**DFRDC:** 0  
 CONSO DF, IDS + ADT  
 JRST .-1  
 DATAO DF, 40  
 JSR INIT  
 CONO DF, RDC + 200 + EIS + EFE + PIA  
 CONO DC, OUT + DARQ + DBRQ + 350 + PIA  
 JRST EXIT

JSR PC stored by UUO subroutine  
 Wait if operation  
 is in progress.  
 Send disc address.  
 Jump to initialize subroutine INIT, below.  
 Command disc.  
 Setup 136 data control.

**INIT:**  
 0  
 MOVE AC (BLKI/BLKO)  
 MOVEM AC, 40 + 2J  
 MOVE AC, (JSR DCINT)  
 MOVEM AC, 40 + 2J + 1  
 MOVE AC, (JSR DFINT)  
 MOVEM AC, 40 + 2J  
 CONO DC, 0  
 CONO PI, 4000 + PI  
 JRST @ INIT

;initialize DC with BLKI for  
 ;input or BLKO for output  
 ;initialize interrupt channels  
 ;interrupt return  
 ;initialize discfile  
  
 ;clear data control  
 ;enable PI circuits in CP; bit 25 plus one of seven PI bits  
 ;EXIT

CHAPTER ~~11~~ 8

SIGNAL GLOSSARY

~~(110 Ms. pages 1-113, 1a-e, 53a-b)~~

(122 Ms. pages 1-113, 1a-e, 8a-b,  
51a-b, 53a-b, 71a-b, 112a-b).

## CHAPTER ~~11~~ 8

### SIGNAL GLOSSARY

The signal glossary contained in this chapter provides a comprehensive reference source for all input and output signals of the discfile system, for all logic levels and pulses used within the system, and for all control and status flip-flops. Any signal or flip-flop can be referenced alphabetically. Each signal description includes the logical input conditions that generate the signal as well as the logical functions performed by the signal. Thus by cross-referencing in the glossary, a complete understanding of both signal source and signal use can be obtained. The glossary entries also include the proper drawing reference for each signal; therefore, the glossary can be used in three ways: as a coordinate index to the engineering drawings; to trace a signal back to its source; and to trace a signal forward to its effects. Examples of each of these three uses are presented below.

#### Example 1

**Problem:** What is the ATP pulse, and where is it generated?

**Solution:** Alphabetical lookup of ATP shows that ATP is the address termination pulse and that it is generated at -FC:C3.

#### Example 2

**Problem:** What types of malfunction could prevent the generation of the NOP level at the end of a read command? **Solution:** Alphabetical

lookup of NOP shows (under the caption "Generated by:") the input conditions that produce NOP:  $CM0(0) \wedge CM1(0)$ . These conditions indicate that both the CM0 flip-flop and the CM1 flip-flop are in the 0 state. The next step is the alphabetical lookup of CM0-1 to determine the logical conditions that normally clear these two flip-flops. These logical conditions (under the caption "Cleared by:") are as follows:

IBR  $\vee$ :

CCB  $\wedge$  CCE .  $\vee$ :

ESP 1  $\wedge$  END(1) .  $\vee$ :

ESP 1  $\wedge$  CM0(1)  $\wedge$  DA RQ

Of these conditions, only ESP 1 and END(1) are relevant during the read command (when the CM0(1) level is not asserted, and when neither the IBR pulse nor the CCB pulse occurs). Evidently the trouble involves either a failure to generate the ESP 1 pulse, or else a failure to set the END flip-flop. For practical troubleshooting purposes, the specific signal traced would depend on further information obtained at each stage of the process. In the example given, the ESP 1 pulse might not appear at the proper time. The next step would then be to turn to glossary entry ESP 1, and to determine which of the ESP 1 generating conditions might be defective. This type of referencing gives the maintenance engineer random access to only the information he needs.

### Example 3:

**Problem:** If the discfile control intermittently fails to generate the CSP pulse, what consequences might result? **Solution:** Alphabetical lookup

of CSP shows the uses to which CSP is applied. During the read command CSP initiates the READ pulse. During the write command CSP initiates the WRITE pulse, the SND pulse and the DTC pulse. During the read compare command CSP initiates the READ pulse, the SND pulse and the DTC pulse. (The same process can be carried out again for READ, WRITE, SND, or DTC, etc., for as many steps as are relevant to the particular inquiry.)

Note to editor: Might be useful to leave out numbers below but to add page numbers numbers - eg: "ALP..... page 10"

SIGNAL GLOSSARY

DISCFILE CONTROL 270

Index to Signal Glossary

- |            |                      |                |                            |
|------------|----------------------|----------------|----------------------------|
| 1) ACE     | 28) DRL              | 54) IOB STATUS | 81) RED                    |
| 2) ACS     | 29) DTC              | 55) IOS3-9     | 82) SCE                    |
| 3) ADE     | 30) DTP              | (55A) M5B      | 83) SCL                    |
| 4) ADS     | 31) EDO              | 56) MCL        | 84) SCS                    |
| 5) ADT     | 32) EDZ              | 57) MRB        | 85) SDR                    |
| (5A) ALARM | 33) EES              | 58) MRG        | 86) SEF                    |
| 6) ALERT   | 34) EFE              | 59) NDP 1      | 87) SEL                    |
| 7) ALM     | 35) EFR              | 60) NDP 2      | 88) WSEL 5                 |
| 8) ALP     | 36) EIS              | 61) NOP        | 89) SELECT                 |
| 9) ALS     | 37) END              | 62) ODO        | 90) SNA                    |
| 10) ATP    | 38) END flip-flop    | 63) ODZ        | 91) SND                    |
| 11) BCO    | 39) ERP              | (63A) OPERABLE | 92) STP                    |
| 12) BSC0-4 | 40) ERROR SIGNAL     | 64) OPR        | 93) TAKE A CHARACTER       |
| 13) CCB    | 41) ESP 1            | 65) PAR        | 94) WCE                    |
| 14) CCE    | 42) ESP 2            | 66) PER        | 95) WCO                    |
| 15) CDA    | 43) FCL              | 67) PIA0-2     | 96) WCT                    |
| 16) CLEAR  | 44) FER              | 68) PIE        | 97) WDC                    |
| 17) CLK    | 45) GIVE A CHARACTER | 69) PIR1-7     | 98) WLE                    |
| 18) CLR    | 46) IBR              | 70) PTA        | 99) WRITE                  |
| 19) CME    | 47) IDS              | 71) PTC        | 100) WRITE LOCKOUT WARNING |
| 20) CM0-1  | 48) IOB CONO CLR     | 72) RCE        | 101) WRT                   |
| 21) CMS    | 49) IOB CONO SET     | 73) RCT        | (99A) WRITE CLOCK EVEN     |
| 22) COH    | 50) IOB DATA CLR     | 74) RDC        | (99B) WRITE CLOCK ODD      |
| 23) CSP    | 51) IOB DATA I       | 75) RDO        |                            |
| 24) DA RQ  | 52) IOB DATA SET     | 76) RDS        |                            |
| 25) DCE    | 53) IOB RESET        | 77) RDY        |                            |
| 26) DCK    |                      | 78) RDZ        |                            |
| 27) DFR    |                      | 79) READ       |                            |
|            |                      | 80) READY      |                            |

**(1) ACE - Address Clock Enable Flip-flop (BS-D270-0-AC:D7)**

The ACS and ADE flip-flops make up a 2-stage synchronizing network that controls the turn-on and turn-off of the address clock. During address transmission, this network ensures that the WCE pulses that clock the address out to the discfile are complete and in phase with the address clock CLK. The ACE(1) level enables a DCD gate at the set input of the ACS flip-flop. The first CLK pulse to arrive after the setup delay of the gate sets the ACS flip-flop. For a detailed description of the ACS-ACE synchronizing network refer to ACS below.

The outputs of the ACE flip-flop also control the input levels applied to bit DA0 of the data accumulator. During data operations, when ACE(0) is asserted, 0's are shifted into the left end of the accumulator as data is shifted right. However, during address transmission, when ACE(1) is asserted, the accumulator operates as a ring-shifter. Shortly after each address bit is clocked out of DA19 and into the discfile, the same address bit is also loaded back into DA0. All 20 address bits (but not the address parity bit) are thus reloaded into the data accumulator at the conclusion of the address transmission. Since the contents of the data accumulator can be directly sampled at the processor (by means of

the CONI 270 instruction), this ring-shift feature of the accumulator operation provides a useful means of checking the operation of the shift logic.

Set by:

ADS

Reset by:

FCL  $\vee$  :

DCK 2  $\wedge$  COH(1)

The FCL pulse provides the initial clear that ensures that the ACE flip-flop starts each operation in the 0 state. The DCK 2 pulse that is produced by the final data bit of the address (the 20th bit) sets the COH flip-flop. This enables the DCK 2 that is initiated by the 21st address bit (the parity bit) to reset both ACE and ACS, thereby turning off the address clock.

(2) ACS - Address Clock Sync Flip-flop (- AC:D8)

The ACS and ACE flip-flops make up a 2-stage synchronizing network that controls the turn-on and turn-off of the address clock. During address transmission, this network ensures that the WCE pulses that clock the address out to the discfile are complete and in phase with the address clock CLK.

The DATAO 270 instruction IOB DATA SET pulse produces a PTA pulse and thus starts a 15- $\mu$ sec delay. The termination of this delay initiates the ADS pulse. The ADS pulse in turn starts the address sequence



by setting the ACE flip-flop. The first CLK pulse that arrives in time sets ACS to 1. (The transition of ACS is not necessarily in exact synchronization with the leading edge of the CLK pulse.) The next CLK pulse, and every succeeding CLK which occurs while ACS(1) is asserted, causes pulse amplifier C24 to produce a WCE clock in sync with the CLK.

The WCE clocks out the address data bits and parity bit to the discfile on the EDO and EDZ twisted pairs. During address transmission, every WCE clock also starts the DCK clock chain, producing in sequence the following pulses: DCK 1, DCK 0, DCK 2, DCK 2.1, and DCK 3.

Set by:

CLK  $\wedge$  ADE(1)

Reset by:

FCL  $\vee$ :

DCK 2  $\wedge$  COH(1)

The FCL pulse provides the initial clear that ensures that the ACS flip-flop starts each operation in the 0 state. The DCK 2 pulse that is produced by the final data bit of the address (the 20th bit) sets the COH flip-flop. This enables the DCK 2 that is initiated by the 21st address bit (the parity bit) to reset both ACE and ACS, thereby turning off the address clock.

(3) ADE - Address Error Flip-flop (-SC:A3)

The CONI 270 samples the contents of ADE on IOB29.

Set by:

ERP  $\wedge$  ADT(1)

Reset by:

SCL

The ERROR pulse is transmitted from the discfile through a twisted pair to the discfile control; there it is inverted and redesignated ERP. At the discfile control, the ERP pulse always sets the FER flip-flop. When the ERROR pulse arrives during the ADT state of the file status octoflop, the ADE flip-flop is also set. This not only tells the programmer that an error has been detected, but furthermore when the error has appeared, and therefore what general class of error has occurred.

Although the fact that ADE has been set somewhat narrows the range of possible errors, there are still at least six different types of address error that can set ADE. Indicator lights at the discfile often may further identify the specific type of address error that has caused the ERROR SIGNAL. Six such types of address error are tabulated below.

## Address Error Tabulation

Error Type	Discfile Indicator Light	Error Description
Address Parity Error	PE	Address parity bit received by discfile does not yield odd parity. (Parity checked at receipt of address termination pulse.)
Address Termination Error	AT	Address termination pulse not received during specified time interval ( $10 \pm 9 \mu\text{sec}$ after final bit of address).
Incomplete Address Error	IA	Address termination pulse received by discfile prior to receipt of complete address.
Address Transfer Error	T (Transfer)	Incorrect or non-existent address received at discfile, or contents of discfile shift register do not correspond to contents of discfile storage register (after parallel transfer from shift register to storage register).
Positioning Error	FAULT and DP (Disc Position)	Positioner unable to settle on correct track within 600 milliseconds after ATP pulse. This condition prevents transmission of the READY pulse to the discfile control.
Sector Error	FAULT and S (Sector)	Desired record not found within approximately 120 milliseconds after positioner settles on correct track. This condition also prevents transmission of the READY pulse.

**(4) ADS - Address Selected (-FC:C2)**

The ADS pulse sets the ACE flip-flop and the WDC flip-flop. The ACE and ACS flip-flops make up a synchronizing network that controls the turn-on and turn-off of the address clock. The ADS pulse starts the turn-on sequence by setting the ACE flip-flop.

The set of the WDC flip-flop by the ADS pulse governs the subsequent setting of the COH flip-flop. For both addresses and data, the assertion of the COH(1) level enables the discfile control to detect the occurrence of parity bits and to distinguish them from other bits of the address or data.

**Generated by:**

PTA plus 15- $\mu$ sec delay

The DATAO 270 instruction sends new addresses to the discfile via the discfile control. The IOB DATA SET pulse of the DATAO instruction produces a PTA pulse and thus starts a 15- $\mu$ sec delay. The termination of this delay steps the file-control octoflop from IDS or ADT state to SNA state and simultaneously initiates the ADS pulse.

**(5) ADT - Address Transmitted (-FC:B3)**

Third state of the file-control octoflop. The octoflop is advanced from SNA state to ADT state after the last of the 21 address bits is transmitted to the discfile. For the octoflop to be advanced to DFR state, the ADT(1) level must be asserted.

New address data can be transferred into the data accumulator only when the octoflop is in either IDS state or ADT state. Neither the CDA pulse

nor the PTA pulse can be generated unless the octoflop is in one of these two states. For the octoflop to be stepped to the SNA state, it must also be in either IDS or ADT state. The CONI 270 samples ADT on IOB20.

Generated by:

ATP  $\checkmark$

RDY plus 1.0-ms delay  $\wedge$  ADE(0)  $\wedge$  DFR(1)  $\wedge$  NOP

The octoflop may enter the ADT state from either of the adjacent states, SNA or DFR. Approximately 15  $\mu$ sec after the final address bit is transmitted to the discfile, the ATP pulse advances the octoflop from SNA state to ADT state.

If CM0-1 contains no command code (NOP), the octoflop will (provided that no address errors are present, i. e. that ADE(0) is asserted) oscillate between ADT state and DFR state. The octoflop is held in DFR state for one millisecond after each RDY pulse arrives from the discfile.

When the read-next-sector bit is 0, the octoflop is held in DFR state during only one millisecond of each 52-millisecond disc revolution. When the read-next-sector bit is 1, the octoflop is set to DFR for one millisecond after the header of each sector of the addressed track is sensed. But regardless of the state of the read-next-sector bit, if NOP is asserted, the octoflop is always returned to ADT state after one millisecond in DFR state.

The ADE(0) level must be asserted (indicating no address errors) in order to start the 1.0 millisecond delay that controls the duration of the DFR state. When no address errors are present, the termination of this

delay causes the octoflop to return from DFR to ADT state (if NOP), or else causes the ALP pulse to advance the octoflop from DFR to ALS state (if  $\sim$ NOP). Note, however, that if there were address errors present (so that ADE(0) were not asserted), the octoflop could not even enter DFR state, but would instead end its cycle at ADT state.

→ Insert page 8 b here

(6) ALERT (-TR:A7)

The ALERT pulse is sent to the discfile through a twisted-pair transmission line. It causes the discfile to increment the stored address by 1, and prepares the discfile logic to receive the forthcoming command signal (READ or WRITE as the case may be).

Generated by:

ALP

The discfile control produces an ALP pulse to advance the file-control octoflop from DFR state to ALS state (See ALP below.) After being amplified by pulse amplifier F29, the ALP pulse is redesignated ALERT and sent to the discfile.

(7) ALM - Alarm (-SC:B4)

When the ALM level is asserted, the FER flip-flop is set immediately. Provided that the priority interrupt enable switch EFE (a flip-flop switch) is set to 1, FER(1) produces a PIE level. The resulting priority interrupt request can notify the programmer that an alarm condition has occurred.

It is not permissible to change the command code in CM0-1 while an alarm condition is present. For this reason,  $\sim$ ALM, the negation of

**(5A) ALARM (-SC:B2)**

The discfile sends an ALARM signal to the discfile control through a twisted-pair transmission line to indicate that an alarm condition has occurred. At the discfile control, the ALARM signal is applied to a switch filter and a pair of series-connected inverters and redesignated ALM.

(See ALM below.)

the ALM level, is used as a necessary input condition for the generation of the GCE level. The CONI 270 samples ALM on IOB30.

Generated by:

ALARM (from discfile)

This signal is generated by the closure of a relay within the discfile. This relay closure shunts the discfile end of a twisted-pair line. (For normal operation, the circuit remains open.) Closure of the relay applies +10 vdc to a switch filter and two series-connected inverters, and thereby generates the ALARM signal at both polarities; see Figure'-SC:B2-5.

The discfile closes the ALARM relay under any of the following four conditions:

- 1) If the output of the positioner power supply in any disc unit falls below normal.
- 2) If a malfunction occurs in the flying-head air supply.
- 3) Should the ambient temperature in the logic unit or in any disc unit rise to the alarm level.
- 4) When any test mode switch is left in test position during normal operate mode.

Note that although any of these four ALARM conditions will always terminate the OPERABLE signal, absence of the ALARM does not guarantee the presence of OPERABLE. The ALARM signal usually implies the existence of an abnormal condition that carries with it the hazard of equipment damage should operations be continued without taking corrective action. The OPERABLE signal goes beyond this minimum standard, and indicates



not only that there is no ALARM, but furthermore that the discfile is operable - that it is ready to receive commands from the discfile control. See OPR below.

(8) ALP - Alert Pulse (-FC:B4)

The ALP pulse steps the file-control octoflop from DFR state to ALS state. Furthermore, the ALP pulse (amplified and redesignated ALERT) is sent through a twisted-pair transmission line to the discfile. The ALERT pulse causes the discfile to increment the stored address by 1 and prepares the discfile logic to receive the forthcoming command signal (READ or WRITE as the case may be).

The discfile control always sends the discfile the address of the sector immediately preceding the sector to be processed. The READY pulse is returned to the discfile control <sup>after</sup> ~~when~~ the header of this preceding "get ready" sector is sensed. The ALERT pulse then increments the stored address of the "get ready" sector, and thereby produces the correct address of the sector actually to be processed. The discfile compares the header of this sector with the incremented address, the extent of the compare depending on the state of the read-next-sector bit.

Within the discfile control, the ALP pulse starts a 15- $\mu$ sec delay. Termination of this delay produces the CSP pulse that ends the ALS state of the octoflop and that actually transmits the READ or WRITE command pulse to the discfile.

Generated by:

RDY plus 1.0 ms delay  $\wedge$  ADE(0)  $\wedge$  DFR(1)  $\wedge$   $\sim$ NOP

Since the file status octoflop is stepped to ALS state by the ALP pulse, the same conditions of generation apply to the pulse as to the state. The significance of these generating conditions is described under ALS below.

(9) ALS - Alert State (-FC:B4)

Fifth state of the file-control octoflop. The ALS(1) level enables the CSP pulse to advance the octoflop from ALS to CMS state.

The octoflop remains in the ALS state for the 15- $\mu$ sec interval between the ALP and the CSP pulses. The ALP pulse that begins the alert state prepares the discfile logic to receive a command signal (the READ or WRITE pulse as the case may be); the CSP pulse that ends the ALS state 15  $\mu$ sec later actually transmits the READ or WRITE pulse to the discfile.

It is not permissible to change the command code in CM0-1 after the ALP has advanced the octoflop from DFR to ALS state. For this reason the ALS(0) level is used as a necessary input condition for the generation of the CCM level. The CONI 270 samples ALS on IOB22.

Generated by:

RDY plus 1.0 ms delay  $\wedge$  ADE(0)  $\wedge$  DFR(1)  $\wedge$   $\sim$ NOP

The octoflop enters DFR state at the arrival of the RDY pulse from the discfile. It remains in DFR state for one millisecond. This one-millisecond

window gives the programmer time to set up the command buffer and thereby to specify what operations are to be performed during the forthcoming sector. After one millisecond in DFR state, either the ALP pulse advances the octoflop to ALS state (if  $\sim$ NOP is asserted, indicating that there is a command code in bits CM0-1 of the command buffer) or else the octoflop is returned to ADT state (if NOP is asserted, indicating that no command code is stored in CM0-1).

The ADE(0) level must be asserted (indicating no address errors) in order to start the 1.0-millisecond delay that controls the duration of the DFR state. When no address errors are present, the termination of this delay causes the octoflop to return from DFR to ADT state, or, in the alternative, produces the ALP pulse (at RDY plus 1.0 ms) which advances the octoflop from DFR to ALS state. Note, however, that if there were address errors present (so that ADE(0) were not asserted), the octoflop could not even enter DFR state, but would instead end its cycle at ADT state.

(10) ATP - Address Termination Pulse (-FC:C3)

The ATP pulse signals the completion of the address transmission to the discfile. It is sent to the discfile through a twisted-pair transmission line approximately 15  $\mu$ sec after the transmission of the parity bit, the final bit of the 21-bit address. Within the discfile control, the ATP pulse advances the file status octoflop from SNA state to ADT state.

Generated by:

SNA(1)  $\wedge$  COH(1) .  $\wedge$  :

DCK 2 plus 15  $\mu$ sec delay  $\wedge$  SNA(1)

Each of the 21 address bits is transmitted to the discfile by a DCK 1 clock pulse. Every DCK 1 clock is followed approximately 400 nsec later by a DCK 2 clock. The DCK 2 pulse shifts the contents of the data accumulator right one bit-position, thereby bringing the next address bit into position to be transmitted to the discfile. The DCK 2 pulse that shifts the parity bit of the address into position for transmission to the discfile also sets the COH flip-flop to the 1 state. The next DCK 1 clock then completes the address transmission by clocking the parity bit into the discfile; about 400 nsec later the final DCK 2 pulse of the address transmission cycle turns off the address clock (this DCK 2 pulse clears ACE, ACS, COH, and WDC) and starts a 15- $\mu$ sec delay. Termination of this delay produces the ATP pulse. Note that the ATP pulse can be generated only if the octoflop remains in SNA state until the completion of the 15- $\mu$ sec delay. (In the unlikely event that an IOB reset pulse were to be applied to the discfile control during the 15- $\mu$ sec delay, it would be necessary to prevent generation of ATP.)

(11) BCO - Bit Counter Overflow (-AC:D1)

During address transmission, the BCO level indicates that all 20 data bits of the address have been clocked out to the discfile. For data operations (read, write, or read compare), the BCO level is asserted at the 18th bit of each 18-bit data character.

The single DCK 2 pulse that occurs during the short period while BCO is asserted always complements the WDC flip-flop. If the WDC flip-flop

contains 1 before being complemented, then the same DCK 2 pulse also sets the COH flip-flop and increments the word counter WCT. Note that although the BCO level is not itself applied to the COH flip-flop set logic, two other ANDed conditions which are so applied are the exact logical equivalent of BCO. (The BSC0(1) and BSC2(1) inputs are used instead of BCO only to simplify wiring, and not from any logical necessity.)

During the two output commands, write and read compare, the BCO level is ANDed with SCS(1) to enable the DCK 2.1 clock to produce the SND and DTC pulses. The SND pulse gates an 18-bit character from the Data Control 136 into the data accumulator of the discfile control. The DTC pulse sends the Data Control 136 a Give a Character pulse to shift the next output character into position.

At the DCK 3 pulse that follows about 800 nsec after the DCK 1 pulse which first asserts BCO, the BCO level causes both the BSC0 and BSC2 bits of the bit counter to be reset (thus terminating the BCO level).

Generated by:

$BSC0(1) \wedge BSC2(1)$

The BCO level is always first asserted at the DCK 1 pulse that causes the bit counter to reach the count of 20. For address transmission, the count starts at 0, and 20 bits are transmitted to the discfile before the count reaches 20. For data operations, the count starts at 2, so only 18 bits need be processed to generate the BCO.

(12) BSC0-4 - Bit-Shift Counter (-AC:C2-5)

The bit-shift counter is a 5-bit count-of-20 binary counter which starts counting in either the 0 state or the 2 state depending upon whether the discfile control is sending out an address to the discfile, or is executing a data operation (a read, write, or read compare command). During address transmission, the bit-shift counter counts the number of address bits that have been clocked out to the discfile; the overflow level BCO is asserted at the 20th bit. For data operations, the overflow occurs at the 18th bit of each 18-bit data character. Besides producing the BCO level, the outputs of the bit-shift counter are also used directly to set the COH flip-flop (see BCO above).

The outputs of the bit-shift counter also determine the time at which the Take a Character pulse is to be sent to the Data Control 136. During the read command, the DCK 1 clock that occurs while the counter contains 19 initiates the Take a Character pulse. This same DCK 1 pulse increments the counter to its overflow count of 20. The Take a Character pulse causes the data control to strobe the input character into its low order accumulator bits, and (if the character is the first of the two 18-bit characters making up the 36-bit data word) to shift it left to make room for the second character.

The CONI 270 instruction samples the contents of the bit-shift counter on IOB12-16.

Cleared by:

Entire counter BSC0-4: FCL

BSC0 and BSC2 only: DCK 3  $\wedge$  BCO

Incremented by:

DCK 1  $\wedge$  COH(0)

BSC3 Set by:

NDP 2  $\vee$  :

DCK 2  $\wedge$  SCS(1)  $\wedge$  BSC0(1)  $\wedge$  BSC2(1)

The FCL pulse clears the bit-shift counter before each new address is transferred out, and at the beginning of each new data sector. When the count reaches 20, the BCO level is asserted; the BSC0 and BSC2 bits are then in the 1 state, and the other three bits of the counter contain 0s. The BSC0 and BSC2 bits are cleared by DCK 3 (about 800 nsec after the DCK 1 pulse that initiates the BCO level).

The counter is incremented only at DCK 1 time. The COH(0) condition ensures that no count is made for parity bits during either address transmission or data operations. (See COH below.)

The BSC3 set conditions enable the counter to act as a count-of-18 counter rather than a count-of-20 counter. For data operations, these set conditions cause the counter to begin its count in the two state. The NDP 2 pulse sets the counter to two at the beginning of each data sector. The second line of set conditions listed above sets the counter to two prior to the beginning of each 18-bit data character after the first one; BSC3 is set at the final overflow count of each character, thus preparing

the counter for the next character. The counter reaches 20, its overflow count, at DCK 1 time; it is incremented to 22 at DCK 2 time; it is reset to its correct initial state of 2 at DCK 3 time. This operating sequence is summarized below in tabular form.

Bit-Shift Counter Sequence - Data Operations

Counter State	Initiated by
0	FCL (Generated at NDP 1 time.)
2	NDP 2 (First character of sector.)
3, 4, ... 16, 17, 18, 19	DCK 1 corresponding to each data bit increments counter by 1.
20	DCK 1 for final (18th) data bit.
22	DCK 2 $\wedge$ SCS(1) $\wedge$ BSC0(1) $\wedge$ BSC2(1) (BSC3 set - to prepare counter for next data character.)
2	DCK 3 $\wedge$ BCO (Clear BSC0 and BSC2.)
3, 4, ... 16, 17, 18, 19	DCK 1 corresponding to each data bit (of second 18-bit character) increments counter by 1.
	etc.

For address transmission, operation of the counter is somewhat more simple.



Bit-Shift Counter Sequence - Address Transmission

Counter State	Initiated by
0	FCL (Generated at PTA time.)
1, 2, ..., 17, 18, 19	DCK 1 corresponding to each address bit increments counter by 1.
20	DCK 1 for (20th) address bit (the bit immediately preceding the address parity bit).
0	DCK 3 $\wedge$ BCO (Clear BSC0 and BSC2).

Note that the counter is not stepped from 20 to 22 as in the case of data operations. This is because the SCS(1) level is not asserted.

(13) CCB - Clear Command Buffer (-CM:C4)

The CCB pulse always clears the nine low-order bits of the command buffer: CLR, EES, EFE, EFR, EIS, END and PIA0-2. If the CCE level is asserted, the CCB pulse also clears the two command code bits CM0 and CM1. Clearing these two bits permits the PTC pulse to load them with the next command.

Generated by:

IBR  $\vee$  :

IOB CONO CLR  $\wedge$  SEL

Although CCE must be asserted for CM0-1 to be cleared by the IOB CONO CLR  $\wedge$  SEL condition, these two bits are also cleared by IBR alone (regardless of the state of CCE).

(14) CCE - Change Commands Enable (-CM:D2)

This level must be asserted to permit immediate program control of the contents of the two command code bits, CM0 and CM1. The CCE level enables CCB to clear CM0-1, and enables PTC to gate in a new command code on IOB7 and IOB8. (The IOB7 and IOB8 inputs correspond to bits 25 and 26 of the CONO instruction word.)

Generated by:

OPR  $\wedge$   $\sim$ ALM .  $\wedge$ :

ALS(0)  $\wedge$  CMS(0)  $\wedge$  SCS(0)  $\wedge$  SCE(0)

To change commands, the discfile must be operable, and must not be sending an alarm signal to the control. Furthermore, the discfile control must be in an appropriate status for changing commands. During any of the first four states of the file-control octoflop (IDS, SNA, ADT, or DFR) it is permissible to send a CONO instruction which changes the command in CM0-1. However, once the Alert pulse has been sent to the discfile, the octoflop is stepped into ALS state, and no further change in command code is permissible. The command code in CM0-1 cannot be changed during any of the last four states of the octoflop (ALS, CMS, SCS, or SCE).

(15) CDA - Clear Data Accumulator (-AD:A8)

The CDA pulse clears the data accumulator DA0-19.

Generated by:

IBR ∨ : IOB DATA CLR ∧ .

SEL ∧ .

MCL(0) ∧ .

IDS(1) ∨ ADT(1)

The IBR pulse always produces a CDA pulse as part of the initial clear operation. During the DATAO instruction, IOB DATA CLR also initiates a CDA provided that certain necessary conditions are met. The discfile control must be selected by the device selection code of the DATAO instruction. Furthermore, the master clear switch must be open, and the discfile control must be in either the idle state or in the address terminated state.

(16) CLEAR (-TR:A4)

At the end of any sector during which the CLR flip-flop is set, the discfile control sends a CLEAR pulse to the discfile. (See CLR below.) (The CLEAR pulse is sent to the discfile through the same twisted-pair line upon which the READY pulse is received.) The CLEAR pulse signals the discfile to end the power-hold state by removing power from the addressed positioner.

The switching time (exclusive of motion time, confirmation time, and latency time) required to change disc and/or position field ranges from about 20 to 30 ms. This switching time can be reduced to about 7 ms if power can be completely removed from the previously addressed

positioner before the discfile starts to reapply power for the new address.

The CLEAR pulse starts the positioner-power turn-off. Note that the programmer must not send a new address to the discfile control during the 25-ms powering-off period following the CLEAR. To do so would cause an error condition. The programmer must use this 25 ms elsewhere for programming some other device. After the 25 ms have elapsed, the programmer can return to the discfile control with a new address.

Generated by:

ESP 2  $\wedge$  CLR(1)

Regardless of when the CLR flip-flop is set, the CLEAR pulse is always sent to the discfile at the ESP 2 pulse that follows the end of the sector. Note that when the CLR flip-flop is set, the END flip-flop is also set automatically. As a result, a CLEAR pulse will never be sent to the discfile unless an END pulse is sent at the same time. (An END pulse may, however, be sent without a CLEAR pulse.)

(17) CLK - Clock (-AC:D8)

The CLK pulses are generated every 1.33  $\mu$ sec so long as the discfile control is turned on. However, the CLK pulses are used only during the address transmission portion of the discfile control operating cycle. The ACS and ACE flip-flops make up a synchronizing network that controls the turn-on and turn-off of the address clock. (The CLK pulses are not turned off, but they are gated through to where they take effect only during the address transmission; see ACS above.) The ACE(1) level enables a

DCD gate at the set input of the ACS flip-flop. The first CLK to arrive after the gate is enabled sets the ACS flip-flop. So long as the ACS(1) level is asserted, each succeeding CLK pulse produces a WCE pulse. The WCE clocks out the address data bits and parity bit to the discfile and also starts the DCK clock chain.

Generated by:

Variable Clock B02

The CLK pulses are standard 100-nsec pulses that are generated at 1.33- $\mu$ sec intervals by variable clock B02, an R401 stable RC-coupled oscillator.

(18) CLR - Clear Flip-flop (-CM:B3)

When the CLR flip-flop is set, the ESP 2 pulse that follows the end of the sector sends a CLEAR pulse to the discfile. At the discfile, the CLEAR pulse ends the power-hold state by removing power from the addressed positioner. This may save time in switching to the next address (See CLEAR Pulse above.)

When the CLR flip-flop is set, the END flip-flop is also set automatically by a diode shunt. The END flip-flop can, however, be set without setting CLR. The result of this arrangement is that whenever the discfile control sends a CLEAR pulse to the discfile, it also sends an END pulse.

When the CLR flip-flop is set, the negation of the CLR(0) level prevents the generation of a RDY pulse even though a READY may arrive from the discfile. The RDY pulse is inhibited when CLR is set ~~because~~ *to prevent the CLEAR pulse from generating a RDY pulse.*

Generated by:

PTC  $\wedge$  IOB4(1)

The CLR flip-flop may be set by programming a CONO 270 instruction with a 1 in bit 22. To reset CLR, give a CONO 270 with 0 in bit 22.

(The IOB4 input corresponds to bit 22 of the CONO instruction word.)

(19) CME - Command Error Flip-flop (-SC:A4)

The CONI 270 samples the contents of CME on IOB27.

Set by:

ERROR (from discfile)  $\wedge$  CMS(1)

Reset by:

SCL

The ERROR pulse is transmitted from the discfile through a twisted pair to the discfile control; there it is inverted and redesignated ERP. At the discfile control, the ERP pulse always sets the FER flip-flop. When the ERROR pulse arrives during the CMS state of the file-control octoflop, the CME flip-flop is also set. This not only tells the programmer that an error has been detected, but furthermore, when the error has appeared, and therefore what type of error has occurred.

The End error is the most common discfile error condition that could cause the transmission of an ERROR pulse to the discfile control during CMS state and thus set CME. If no END, READ, or WRITE pulse is received by the discfile within the 8- $\mu$ sec guard slot following the final pulse of a sector, an End error occurs. The ERROR pulse is then

transmitted to the discfile control, and the END indicator at the discfile is lighted. Since, for multi-sector operations, the discfile control is returned to CMS state seven microseconds after the final DCK 1 pulse of a sector, the control would reach CMS state prior to the arrival of the ERROR pulse induced by the End error.

(20) CM0-1 - Command Register (-CM:B1, 2)

The command register CM0-1 includes 2 of the 11 bits making up the command buffer. These two bits store the command codes that govern most operations performed by the discfile control. For a description of the remaining nine bits of the command buffer, refer to CLR, EES, EFE, EFR, EIS, and PIA0-2 below.

The outputs of the two command register bits CM0-1 are applied to a half binary-to-octal decoder, which then asserts one of four output command levels depending upon the states of CM0 and CM1. These four command levels are tabulated below.

Command Register Decoding				
CM0	CM1	Octal Contents	Output Level Asserted by Decoder	
0	0	0	NOP	(No Operation)
0	1	1	RED	(Read)
1	0	2	WRT	(Write)
1	1	3	RDC	(Read Compare)

For a description of the uses to which these command levels are put throughout the discfile control, refer to NOP, RDC, RED, and WRT below.

Besides serving as inputs to the binary-to-octal decoder, three of the four output levels from flip-flops CM0-1 also are used directly as control signals. The levels CM0(0), CM0(1), and CM1(1) are so used; CM1(0) is at present unused. The table below shows that each of these three levels is asserted whenever either of two command levels is asserted. Because certain operations of the discfile control are common to two commands, it simplifies the system logic to use these command-pair output levels as control functions.

<u>Command-Pair Control Functions</u>		
Output Level	Asserted During Either	Used to Generate
CM0(0)	NOP $\vee$ RED	Take a Character, set WCT7
CM0(1)	WRT $\vee$ RDC	CM0-1 Clear, DTC, SND
CM1(1)	RED $\vee$ RDC	PER, RDS, READ

The use of CM0(0) to set WCT7 and to generate the Take a Character pulse is logically equivalent to the use of RED, because in both cases the CM0(0) level is ANDed with SCS(1), which can never be asserted during NOP. (The CM0(0) level is used instead of the RED level only to ~~simplify wiring~~ *reduce signal propagation time* and not from any logical necessity.)

The three signals controlled by CM0(1) are common to both the write and the read compare commands. The clear conditions for CM0-1 are



described below under the heading "Cleared by:". The DTC pulse sends a Give a Character pulse to the Data Control 136; that pulse shifts the next 18-bit data character into position for sampling. The SND pulse reads the current 18-bit data character into the data accumulator of the discfile control.

Similarly, the three signals enabled by CM1(1) are common to both the read and the read compare commands. The parity of incoming data from the discfile is tested during both commands. Consequently the PER flip-flop set logic requires the assertion of CM1(1). The RDS signal puts the DCK clock chain under control of incoming data pulses (ED0, EDZ, ODO, and ODZ pulses) during read and read compare commands. The third and final operation that is governed by the assertion of CM1(1) is the transmission of READ pulses to the discfile.

Set by:

CM0:            PTC ^ CCE ^ IOB7(1)

CM1:            PTC ^ CCE ^ IOB8(1)

The processor instruction CONO 270 loads command codes into CM0 and CM1 via IOB7 and IOB8. (The IOB7 and IOB8 inputs correspond to bits 25 and 26 of the CONO instruction word.) Note, however, that unlike the other nine bits of the command buffer, which can be loaded at any time, the two command code bits can be loaded only when the CCE level is asserted.

Cleared by:

IBR  $\vee$ :

CCB  $\wedge$  CCE .  $\vee$ :

ESP 1  $\wedge$  END(1) .  $\vee$ :

ESP 1  $\wedge$  CM0(1)  $\wedge$  DA RQ

The IBR clear condition is initiated by IOB reset and is an unconditional clear. The CCB clear pulse occurs at IOB CONO CLR during each CONO 270 instruction, but does not always clear CM0-1. The contents of these two command code bits are under immediate program control only during a specific portion of the operating cycle, i. e. that portion of the cycle when CCE is asserted.

It is, however, possible to clear CM0-1 at the conclusion of any sector of data. This can be done (third line of clear conditions above) by simply setting the END flip-flop (with a CONO 270 which contains 1 in bit 23; see END below). The next ESP 1 pulse then clears CM0-1, and thus enables the ESP 2 pulse, which follows 2  $\mu$ sec later, to reset the discfile control to IDS state. For write and read compare commands, the current sector runs its normal course, and no ESP pulses will be generated until the entire sector is traversed. However, for read commands the assertion of END(1) immediately sets WCT7, turning off the clock and starting the 5  $\mu$ sec delay that terminates with the ESP 1 pulse.

The fourth and last line of the clear conditions listed above governs the automatic clear that occurs at the end of the final sector of output data. The CM0(1) level (see table above) indicates that the current command is

either write or read compare. The DA RQ level from the Data Control 136 is asserted as soon as the data control has transmitted the last of its data to the discfile control.

Note that the output command nevertheless continues to the end of the current sector. Even if the output data ends prior to the normal end of sector, clock pulses continue to be generated, and the bit and word counters continue to count until the 128 full 36-bit words have been traversed. If the command is write, 0's are written for the rest of the sector after the output data ends. If the command is a read compare, a read compare error is generated when the output data ends (unless the input data from the discfile ends at the same point as the output data from the Data Control 136).

(21) CMS - Command Selected (-FC:B5)

Sixth state of the file-control octoflop. The octoflop may enter CMS state from either ALS state or SCE state. When processing the first sector of data, the octoflop advances from ALS state to CMS. At the beginning of each subsequent data sector, the octoflop returns from SCE state to CMS state.

The same conditions which step the octoflop to CMS state also start a 200- $\mu$ sec delay. If still asserted at the termination of this delay, the CMS(1) level enables the transition of the delay output to produce an NDP 1 pulse and (1  $\mu$ sec later) an NDP 2 pulse. In the unlikely event that an IOB reset pulse were to be applied to the discfile control during

the 200- $\mu$ sec delay, it would be necessary to prevent both NDP 1 and NDP 2. (Because the IOB reset would reset the octoflop from CMS to IDS state, CMS(1) would not be asserted at the end of the delay, and therefore the NDP pulses would not be generated.)

It is not permissible to change the command code in CM0-1 after the ALP has advanced the octoflop from DFR to ALS state. For this reason, the CMS(0) level is used as a necessary input condition for the generation of the CCM level.

If an ERROR signal arrives from the discfile while the octoflop is in CMS state, the CME flip-flop is set, indicating that the error is a command error. The CONI 270 samples CMS on IOB23.

Generated by:

CSP  $\wedge$  ALS(1) .  $\vee$ :

ESP  $\wedge$   $\sim$ NOP

At the beginning of each input or output sequence, the same CSP that transmits the READ or WRITE command pulse to the discfile also advances the octoflop from ALS state to CMS state. This is represented by the first condition above.

The second condition for CMS state represents the processing of additional data sectors. At the end of each sector, the discfile control senses the end of the data by means of a 5- $\mu$ sec integrating delay. When this delay times out, an ESP 1 pulse is generated, and then, 2  $\mu$ sec later, an ESP 2 pulse is generated. The ESP 1 pulse advances the octoflop from SCS state to SCE state. The ESP 2 pulse then performs one of two

alternate functions. If there is no command code present in CM0-1 (NOP), no further operations are required, and the ESP 2 pulse returns the octoflop to IDS state. However, if a command code is present ( $\sim$ NOP), additional sectors of data are to be processed. The ESP 2 pulse then sends another READ or WRITE pulse to the discfile, and simultaneously returns the octoflop from SCE state to CMS state.

(22) COH - Counter Overflow Hold Flip-flop (-AD:C6)

The state of the COH flip-flop enables the discfile control to distinguish between parity bits and other address or data bits. The COH flip-flop contains 1 only when an address parity bit (the 21st bit of each address) or a data word parity bit (the 37th bit of each data word) is being (or is about to be) processed; during the processing of all other address or data bits, the COH flip-flop remains in the 0 state.

During the write command, the state of the COH flip-flop determines what output data is returned to the discfile on the even and odd data lines. (See EDO, EDZ, ODO and ODZ below.) When COH(0) is asserted, the WCE and WCO pulses sample the output data bit in DA19, but when COH(1) is asserted, the WCE and WCO pulses transmit a parity bit determined by the state of the PAR flip-flop. (The parity bit transmitted is the complement of PAR at the single WCE or WCO that coincides with the COH(1) level.)

During the read command, every input bit read from the discfile (parity as well as data) produces an RDO or an RDZ pulse. So long as

COH(0) is asserted, indicating that the current RDO or RDZ pulse represents an input data bit (not an input parity bit), the pulse is gated through to load the data bit into DA2. However, for the single RDO or RDZ pulse of each data word that represents the 37th bit of the word (the parity bit), the COH(1) level is asserted; the negation of COH(0) prevents the parity bit from entering the accumulator. The incoming parity bits from the discfile are filtered out in this way because the parity test is completed within the data control. Once the test is made there is no further need to preserve the parity bits.

The read compare command compares one or more sectors of output data (or even some fraction of a full sector) with corresponding input data read from the discfile. The comparison is executed one bit at a time, but does not include parity bits. No output parity bits are generated during read compare commands, and, although a normal parity test is made, the incoming parity bits are ignored for purposes of the read comparison.

During the read compare command, as during the read command, every input bit read from the discfile (parity as well as data) produces an RDO or an RDZ pulse. So long as COH(0) is asserted, indicating that the current pulse represents an input data bit rather than an input parity bit, each RDO pulse complements the RCT flip-flop. (See RCT below.) However, for the single RDO or RDZ pulse of each data word that represents the 37th bit of the word (the parity bit), the COH(1) level is asserted. The negation of COH(0) prevents the parity bit from complementing RCT even if the parity is a 1 and therefore initiates an RDO.

For address transmission, and for all data operations (read, write, and read compare), the bit-shift counter counts all address or data bits that are processed, but not parity bits. Consequently, the BSC is incremented at each DCK 1 pulse so long as COH(0) is asserted. When the COH flip-flop is set, indicating that an address parity bit, or a data-word parity bit is the bit that has initiated the current DCK 1 pulse, the counter is not incremented. (See BSC0-4 above.)

Similarly, for both address transmission and data operations, the data accumulator DA0-19 is shifted right one bit position after each address or data bit is processed, but is not shifted for parity bits. The data accumulator is therefore shifted right at each DCK 2 pulse so long as COH(0) is asserted; it is not shifted right at DCK 2 if COH(1) is asserted.

Besides inhibiting those functions which must be prevented during the processing of the address or data word parity bits, the COH flip-flop also enables certain other operations which must occur during the processing of the address or data word parity bits.

During address transmission, the DCK 2 pulse corresponding to the 21st bit of the address (the address parity bit) initiates the address termination pulse ATP. The DCK 2 pulse is enabled to produce an ATP only when SNA(1) and COH(1) are asserted. (The DCK 2 does not produce the ATP directly, but rather triggers a 15- $\mu$ sec delay. If the SNA(1) level continues throughout the delay, as it does except in the uncommon case of an intervening IOB reset, the termination of the delay produces the ATP pulse.)

The address clock is turned on and off by a two-stage synchronizing network comprising the ACE and ACS flip-flops. The COH(1) level enables DCK 2 to reset ACE and ACS, thus turning off the address clock. (See ACS above.) The COH(1) level is asserted at only a single DCK 2 pulse, at that DCK 2 that is initiated by the 21st and final bit of the address (the address parity bit).

For read and read compare commands, the parity error flip-flop PER can only be set by the DCK 2 pulse initiated by the 37th bit of the input data word (the parity bit). The COH(1) level is used as a necessary condition for the setting of the PER flip-flop.

Set by:

$DCK\ 2 \wedge WDC(1) \wedge BSC0(1) \wedge BSC2(1)$

Reset by:

FCL  $\vee$ :

$DCK\ 2 \wedge COH(1)$

Although the COH flip-flop set and reset conditions are somewhat complex, the end result of these conditions is not complicated. The COH flip-flop is always set to the 1 state at the DCK 2 pulse of the address or data bit immediately preceding the parity bit, and is always reset to the 0 state at the DCK 2 pulse that is actually initiated by the parity bit.

The FCL pulse provides the initial clear; it clears the COH before each new address is transferred out and at the beginning of each new data sector.



Throughout the address transmission, the WDC flip-flop contains 1, and the WDC(1) level is asserted. The DCK 1 pulse corresponding to the 20th bit of the address being sent to the discfile (the bit immediately preceding the address parity bit) leaves both BSC0 and BSC2 in the 1 state. (See BSC0-4 above.) The DCK 2 pulse that follows about 400 nsec later thus sets the COH flip-flop to the 1 state. The next DCK 2, the DCK 2 that is initiated by the address parity bit itself, resets COH.

During all data operations (read, write and read compare commands), the BSC0 and BSC2 bits of the bit shift counter both contain 1 (the counter then contains 20) on two separate occasions during the processing of each 37-bit data word. The BSC first reaches the count of 20 at the DCK 1 pulse corresponding to the final data bit of the first 18-bit data character. The BSC is counted to 20 a second time at the final bit of the second 18-bit data character of the 27-bit data word. However, the WDC flip-flop contains 1 only during the processing of the second data character. Consequently, only the DCK 2 pulse initiated by the final bit of that second 18-bit character (the 36th and final data bit of the data word) is allowed to set the COH flip-flop to 1. The next DCK 2 pulse, the DCK 2 initiated by the 37th and final bit of the data word (the data parity bit itself) resets COH.

(23) CSP - Command Select Pulse (-FC:C4)

At the expiration of the 15- $\mu$ sec delay started by ALP, the CSP pulse advances the file-control octoflop from ALS state to CMS state.

Depending on the command code stored in CM0-1, the CSP pulse causes the transmission of either a READ pulse or a WRITE pulse to the discfile. If CM0-1 contains 10 (write), then CSP transmits a WRITE pulse to the discfile. However, if CM1 contains a 1, the command code must be either 01 (read) or 11 (read compare). In either case, CSP transmits a READ pulse to the discfile.

Again depending on the contents of CM0-1, the CSP pulse may also initiate an SND pulse and a DTC pulse. The CSP pulse produces both SND and DTC whenever the command code in CM0-1 specifies either of the two output commands, write or read compare; i. e. whenever CM0 contains 1. The SND pulse gates an 18-bit output data word from the Data Control 136 into the data accumulator of the discfile control. The DTC pulse sends the Data Control 136 a Give a Character pulse to shift the next output character into position for transfer into the discfile control.

Generated by:

ALP plus 15  $\mu$ sec delay.

Summary of Pulses Initiated by CSP

<u>Command</u> Code			<u>To Discfile</u>		
	CM0	CM1	WRITE	READ	SND & DTC
NOP	0	0	(Neither ALP nor CSP generated)		
Read	0	1		X	
Write	1	0	X		X
Read Compare	1	1		X	X

(24) DA RQ - Data Accumulator Request (-CM:C1)

This level is applied to the discfile control from the Data Control 136. During the output commands, write and read compare, the assertion of the DA RQ level indicates that the data control has sent out the last of its output data.

At the discfile control, the DA RQ level is used to detect the end of the output data and to terminate the output command. The CM0(1) command-pair function is asserted whenever the command register specifies either a write or a read-compare command. (See CM0-1 above.)

The assertion of CM0(1) ANDed with the assertion of DA RQ enables the ESP 1 pulse to clear the command register CM0-1 at the end of the current sector. The ESP 2 pulse that occurs 2  $\mu$ sec after ESP 1 then sends the discfile an END pulse and resets the discfile control to IDS state.

Generated by:

Status Bit DA RQ (in Data Control 136) contains 1.

During output operations, the Data Control 136 sets the DA RQ status bit (and thus asserts the DA RQ level) when the data control data accumulator becomes empty.

(25) DCE - Data Clock Error Flip-flop (-SC:A5)

The CONI 270 samples the contents of DCE on IOB26.

Set by:

ERP  $\wedge$  SCS(1)

Reset by:

SCL

The ERROR pulse is transmitted from the discfile through a twisted pair to the discfile control; there it is inverted and redesignated ERP. At the discfile control, the ERP pulse always sets the FER flip-flop. When the ERROR pulse arrives during the SCS state of the file-control octoflop, the DCE flip-flop is also set. This not only tells the programmer that an error has been detected, but furthermore, when the error appeared, and therefore what general class of error has occurred.

Although the fact that DCE has been set somewhat narrows the possible range of errors, there are still at least five different types of data clock error that can set DCE. Indicator lights at the discfile often may further identify the specific type of data clock error that has caused the ERROR signal. Five such types of data clock error are tabulated below.

Data Clock Error Tabulation

Error Type	Discfile Indicator Light	Error Description
Write Clock Error	WC	Missing pulse from the write clock control track (Write operations only).
Data-In Error	DI	Two successive output data pulses separated by more than 150% of the normal time interval. (Note that the data-in terminology is only correct with respect to the discfile. The data pulses referred to are output pulses from the discfile control; the DI error can occur only during writing.)
Data-Out Error	DO	Two successive input data pulses separated by more than 150% of the normal time interval. (Note that the data-out terminology is only correct with respect to the discfile. The data pulses referred to are input pulses to the discfile control; the DO error can occur only during reading and read comparing.)
Clock Check Error	CC	<ol style="list-style-type: none"> <li>1) Odd or even output data pulse dropped during write operation; or</li> <li>2) Even outer-zone clock generated during inner-zone write operation; or</li> <li>3) Write amplifier malfunction.</li> </ol>
Data Check Error	DC	<ol style="list-style-type: none"> <li>1) Discrepancy detected in bit-by-bit comparison between data transmitted by discfile logic unit, and data content of the discfile write current (write operations only); or</li> <li>2) Processor attempts to write on locked out disc. Note that when this condition arises, the discfile sends the discfile control a WRITE LOCKOUT WARNING before the ERROR <del>pulse</del> (See WLE below.)</li> </ol>

\*  
SIGNAL pulse.

(26) DCK - Data Clock (-TR:B, C7-8)

The data clock chain includes a sequence of five separate clock pulses: DCK 1, DCK 0, DCK 2, DCK 2.1 and DCK 3. With the exception of DCK 0, which is used only for proper loading within the clock chain itself, all of these clock pulses initiate logical functions throughout the discfile control. These functions are summarized below in tabular form (at the end of the present glossary entry). More detailed descriptions of most of the operations initiated by the DCK clocks can be found under other glossary entries corresponding to the abbreviations in the second ("Clocks Operation") column of the table below.

Whenever the DCK 1 pulse is triggered, the remaining four DCK pulses always follow with fixed delays in the order specified. The DCK 1 pulse is applied to two series-connected inverters and a W607 pulse amplifier B22; the output of this pulse amplifier follows approximately 20 nsec after DCK 1, and is designated DCK 0. The DCK 0 pulse is an auxiliary pulse used only in the clock chain and nowhere else in the discfile control. The DCK 0 pulse serves only one function; that function is to trigger the W300 clock-chain generator that produces the DCK 2 pulse, the DCK 2.1 pulse, and the DCK 3 pulse. Between these three pulses and the DCK 0 pulse that initiates them, there are delays of 400, 550, and 800 nsec respectively; see figure -TR:C8.

Because the DCK 1 pulse always initiates the remaining four pulses of the clock chain, the generating conditions described below refer only to DCK 1; the remaining four pulses always follow DCK 1 in the sequence

described above. The DCK 1 pulse is generated in three different modes:  
1) address transmission; 2) write commands; and 3) read or read compare  
commands.

Address Transmission Mode: DCK 1 Generated by:

$WCE \wedge \sim RDS \wedge WCT7(0)$

Write Command Mode: DCK 1 Generated by:

$WCE \vee WCO. \wedge:$

$\sim RDS \wedge WCT7(0)$

Read or Read Compare Command Mode: DCK 1 Generated by:

$EDO \vee EDZ \vee ODO \vee ODZ. \wedge:$

RDS

During address transmission, the WCT7 flip-flop is always in the 0 state, and, because SCS(1) is not asserted,  $\sim RDS$  is asserted. (See RDS below.) Consequently, each WCE pulse initiates a DCK 1 pulse. Note that during address transmission, the WCE pulses are not generated by one of the write clock control tracks in the discfile, but instead are generated by the internal address clock of the discfile control itself. (See WCE below.)

For write commands, the DCK 1 pulse is initiated by each WRITE CLOCK EVEN and WRITE CLOCK ODD pulse generated by the appropriate write clock control track in the discfile (inner-zone or outer-zone depending upon the location of the sector to be written; see WRITE CLOCK EVEN below.) The WRITE CLOCK pulses are inverted within the discfile control, and redesignated WCE and WCO. Even and odd WRITE CLOCK pulses from the discfile continue to trigger DCK 1 until the word count reaches 128 and the WCT7 flip-flop is set to 1 (at the end of the sector). As soon as WCT7(0) is no longer asserted, the DCK clock is turned off; no further DCK 1 pulses can be

generated. The  $\sim$ RDS level is asserted throughout all write commands, because CM1(1) is then negated. (See RDS below.)

Note that every write command must continue to the end of the 128-word sector, even if the output data from the discfile is exhausted prior to that time. Incoming ~~WCE and WCO clocks~~ <sup>WRITE CLOCK pulses</sup> continue to arrive at the discfile control, and the DCK clock chain continues to function. If no further output data is available, 0's are written for the rest of the 128-word sector. Similar considerations apply to the read compare command. It is only the read command that can be terminated in mid-sector by setting the END flip-flop.

For the read and read compare commands, the DCK 1 is initiated by each incoming data pulse (EDO, EDZ, ODO, and ODZ) from the discfile. The RDS level is always asserted until the WCT7 flip-flop is set to 1. The WCT7 flip-flop is set to 1 only when the word count reaches 128, or (in the case of the read command only) at the first DCK 1 pulse after the END flip-flop is set to 1.



NOTE TO EDITOR: If it wouldn't introduce too many production problems, it would be useful to treat this entire two-page table as a B-sized tip-out page.

OPERATIONS INITIATED BY DCK CLOCK PULSES

Pulse	Clocks Operation	When Enabled	Remarks
DCK 1	DCK 0	20-nsec delay	DCK 0 always follows DCK 1.
	BSC count	COH(0)	BSC is incremented at every DCK 1 except those corresponding to parity bits.
	Take a Character	CM0(0) ^ SCS(1) ^ END(0) ^ BSC0(1) ^ BSC3(1) ^ BSC4(1)	Read command, Take a Character initiated by DCK 1 corresponding to 18th data bit of the input character.
	Set WCT7	CM0(0) ^ SCS(1) ^ END(1)	If END set during read command, the first DCK 1 ends RDS and stops the clock.
DCK 0	DCK 2	400-nsec delay	DCK 2 always follows DCK 0
	DCK 2.1	550-nsec delay	DCK 2.1 always follows DCK 0
	DCK 3	800-nsec delay	DCK 3 always follows DCK 0

DCK 2

SDR

COH(0)

DA0-19 shifted right for all address and data bits except parity bits.

ACE, ACS reset

COH(1)

Address clock turned off after sending address parity bit.

WDC comple-  
mented

BCO

WDC in the 1 state for address transmission and for the 2nd data character of each data word.

COH set

$WDC(1) \wedge BSC0(1) \wedge BSC2(1)$

COH is set by the DCK 2 of the address or data bit immediately preceding the address or data parity bit.

COH reset

COH(1)

COH is reset again by the DCK 2 of the address or data parity bit.

WCT count

$WDC(1) \wedge BCO$

WCT is incremented at the 36th bit of each data word.

PER set

$CM1(1) \wedge COH(1) \wedge PAR(0)$

For read and read compare, parity bit DCK 2 pulse tests parity by sampling PAR.

BSC3 set

$SCS(1) \wedge BSC0(1) \wedge BSC2(1)$

BSC set to 2-state in preparation for next 18-bit data character.

DCK 2.1

SND, DTC, and  
Give a Character

$CM0(1) \wedge SCS(1) \wedge BCO$

For output commands, a new 18-bit data character is transferred into DA2-19 150 nsec after the last SDR of the previous data character.

DCK 3

RCE set

$RDC \wedge RCT(1)$

RCE set when read comparison fails.

RCT reset

---

RCT reset after each read comparison.

BSC0, BSC2 reset

BCO

Bit counter decremented by 20 in preparation for next count.

Fourth state of the file-control octoflop. Each sector of data begins with a 21-bit header. The address of the sector makes up the first 19 bits of these 21. The read-next-sector and parity bits are not included in the header. In place of these two bits, immediately after the 19 address bits, two 0 bits are written into the header. When a header that matches the last address sent to the discfile is sensed, the discfile sends a RDY pulse to the discfile control. The RDY pulse indicates that the discfile has sensed the "get-ready" sector (the sector with the matching header) and is ready to accept a command with respect to the next sector (the sector that immediately follows the "get-ready" sector). The RDY pulse advances the octoflop from ADT state to DFR.

The DFR(1) level is applied to the logic nets that govern octoflop entry to ADT state and ALS state. The octoflop remains in DFR state for one millisecond. This one-millisecond window gives the programmer time to set up the command buffer and thereby to specify what operations are to be performed during the forthcoming sector. After remaining in DFR state for one millisecond, the octoflop either advances to ALS state (if  $\sim$ NOP is asserted, indicating that there is a command code in bits CM0-1 of the command buffer), or else the octoflop returns to ADT state (if NOP is asserted, indicating that no command code is stored in CM0-1).

When the read-next-sector bit is 0, the octoflop is held in DFR state during only one millisecond of each 52-millisecond disc revolution. However, when the read-next-sector bit is 1, the octoflop is set to DFR for one millisecond after the header from each sector of the addressed track is sensed.

Provided that the priority interrupt enable switch EFR (a flip-flop switch) is set to 1, DFR(1) produces a PIE level. The resulting priority interrupt request often is used to notify the programmer that the discfile has found the required address and that the discfile control may need a command.

The CONI 270 samples DFR on IOB21.

Generated by:

$RDY \wedge ADE(0) \wedge ADT(1)$

The octoflop can enter DFR state only from ADT state. If ADE(0) is asserted, indicating that no address errors are present, the RDY pulse advances the octoflop from ADT to DFR state. Note that ADE(0) must also be asserted in order to start the 1.0-millisecond delay that controls the duration of DFR state. When no address errors are present, the termination of this delay causes the octoflop to advance from DFR to ALS state, or to return from DFR to ADT state.

(28) DRL - Data Request Late Flip-flop (-SC:A6)

The DRL flip-flop is set ~~of~~<sup>if</sup> the Data Control 136 is not selected to the discfile control in time to operate upon a forthcoming data sector. Provided that the priority interrupt switch EFE (a flip-flop switch) is set to 1, DRL(1) produces a PIE level. The resulting priority interrupt request may be used to notify the programmer that the intended operation cannot be performed until an appropriate CONO command is sent to the data control. This CONO DATA CONTROL must set up the control-

status register bits IC30-32 to internal device address 5, and thus select the Data Control 136 to the discfile control.

Set by:

NDP 2  $\wedge$  SEL 5

Reset by:

SCL

If the Data Control 136 has not been selected to the discfile control by NDP 2 time (a number of milliseconds before the data sector that is to be processed begins), the DRL flip-flop is set. This provides ample time to send the processor a priority interrupt, and for the processor to respond with the requisite CONO DATA CONTROL.

(29) DTC - Data to Control (270) (AD:D2)

The DTC pulse is used only for the purpose of generating two additional pulses, SND, and GIVE A CHARACTER. The DTC pulse is inverted to produce the SND pulse. To produce the GIVE A CHARACTER pulse, the DTC pulse is amplified by pulse amplifier D26.

The SND pulse causes the contents of the 18 high order bits of the Data Control 136 data accumulator to be loaded into bits DA2-19 of the discfile control data accumulator.

The GIVE A CHARACTER pulse is sent to the Data Control 136 accumulator shift logic. The GIVE A CHARACTER pulse signals the data control that the discfile control has accepted the character currently stored in the high order end of the data control data accumulator (by

clocking it in with an SND pulse), and that unless that character was the last (second) character in the output data word, the data control must shift the contents of its accumulator left by 18 bit-positions in order to bring the next character into the high order bit-positions.

Generated by:

CSP  $\wedge$  CM0(1).  $\vee$ :

DCK 2.1  $\wedge$  CM0(1)  $\wedge$  SCS(1)  $\wedge$  BCO.  $\vee$ :

PTC  $\wedge$  IOB1(1)

The first two lines of the DTC generating conditions listed above both include the CM0(1) command-pair function. This function is asserted during the output commands, write and read compare. For most operations of the discfile control, the DTC pulse is required only for those two output commands.

The first line of the generating conditions includes the CSP pulse that precedes the beginning of each data sector; that pulse produces the first DTC pulse of the sector. That DTC in turn initiates the SND pulse that loads the first 18-bit data character of the sector into DA2-19; furthermore that DTC sends the Data Control 136 the first GIVE A CHARACTER pulse of the sector. That first GIVE A CHARACTER causes the second 18-bit data character of the sector to be shifted left 18 bit-positions in the data control data accumulator. The second character is then properly positioned for transfer out into the discfile control data accumulator.

The second line of the DTC generating conditions produces an additional

DTC pulse for each additional data character after the first one. The BCO level is asserted at the DCK 1 pulse initiated by the write clock or the input data pulse corresponding to the 18th and final data bit of the first data character of the sector. The DCK 2 pulse that follows about 400 nsec later shifts the first character right for the 18th and last time. The DCK 2.1 pulse then follows 150 nsec after the shift, and initiates the second DTC pulse of the sector. That DTC in turn initiates the SND pulse that loads the second 18-bit character of the sector into DA2-19, and furthermore sends the GIVE A CHARACTER pulse to the Data Control 136. This process continues until the end of the 128-word data sector when the DCK clock is turned off.

The third and final line of the DTC generating conditions listed above represents a programmed DTC that can be given at will from the processor. This DTC is generated at the IOB CONO SET time of any CONO 270 instruction that has a 1 in bit 19. (The IOB1 input corresponds to bit 19 of the CONO instruction word.)

(30) DTP - Data to Processor (-AD:A8)

This 2.5- $\mu$ sec level gates the contents of the data accumulator DA0-19 and the bit shift counter BSC0-4 onto the IO bus. The processor reads in this information from the bus at the 2- $\mu$ sec point. Note that for this transfer, as for the PTA transfer described below, the DA12 and DA19 bits are connected out of sequence. (This is done to match the format of the discfile address.)

Generated by:

IOB DATA I ^ SEL

The processor DATAI instruction produces a 2.5- $\mu$ sec negative IOB DATA I level. This command level is effective at the discfile control only when SEL is asserted, i. e. only when the DATAI instruction device selection code is 270 octal.

(31) EDO - Even Data Ones (-TR:C3)

Addresses and data are transmitted to and from the discfile on four twisted-pair transmission lines. These four twisted-pair lines are used in sets of two; one line of each set is pulsed for a 1; the other line for a 0. Two such sets of two lines are used. This allows alternate bits (odd and even) to be transmitted on different lines, thus halving the data transmission frequency.

For address transmission, and for write commands, each EDO pulse is amplified by pulse amplifier D31 and then transmitted to the discfile over the even data 1's twisted pair.

During read and read compare commands, if RDS is asserted (indicating that the word counter has not yet reached its final count of 128), each EDO pulse initiates an RDO pulse and starts the DCK clock chain. The RDO pulse in turn is used to complement RCT, and (for read commands only) to set DA2.



Generated by:

Even data 1 (read at discfile) .  $\nabla$ :

WCE  $\wedge$ :

COH(0)  $\wedge$  DA19(1) .  $\nabla$ :

COH(1)  $\wedge$  PAR(0)

When reading, or read comparing, the EDO pulses enter the discfile control on the even data 1's line from the discfile. The two series-connected inverters through which the EDO pulses are passed before generating RDO are used for noise isolation and for adjusting the voltage reference to the usual DEC logic levels (-3 vdc to ground).

During writing, the EDO pulses are clocked by the write clock even, WCE. So long as address bits or data bits are being sent to the discfile, COH(0) is asserted; COH(1) is asserted only when the parity bit is sent to the discfile. Because odd parity is generated for both address and data, a 1 parity bit is sent to the discfile when the total number of 1 bits in the address, or in the data word, is even; i. e. when PAR (0) is asserted.

(32) EDZ - Even Data Zeros (-TR:C4)

See EDO above.

For address transmission and for write commands, each EDZ pulse is amplified by pulse amplifier D31 and then transmitted to the discfile over the even data 0's twisted pair.

During read and read compare commands, if RDS is asserted, each EDZ pulse initiates an RDZ pulse and starts the DCK clock chain. The RDZ pulse resets DA2, but only during read commands.

Generated by:

Even data 0 (read at discfile) .  $\vee$ :

WCE  $\wedge$ :

COH(0)  $\wedge$  DA19(0) .  $\vee$ :

COH(1)  $\wedge$  PAR(1)

So long as address bits or data bits are being sent to the discfile, COH(0) is asserted; COH(1) is asserted only when the parity bit is sent to the discfile. Because odd parity is generated for both address and data, a 0 parity bit is sent to the discfile when the total number of 1 bits in the address or data word is odd as it stands (without the parity bit); i. e. when PAR(1) is asserted.

(33) EES - Enable End of Sector Flip-flop (-CM:B5)

The EES flip-flop enables or disables the sector end flag priority interrupt condition. If the EES flip-flop contains 1, a priority interrupt enable level PIE is produced whenever the sector end flag SEF is set to 1. However, if the EES flip-flop contains 0, the SEF(1) level is not allowed to initiate PIE.

Set by:

PTC  $\wedge$  IOB12(1)

Reset by:

CCB

The EES flip-flop may be set by programming a CONO 270 instruction with a 1 in bit 30. To reset EES, give a CONO 270 with 0 in bit 30. (The IOB12 input corresponds to bit 30 of the CONO instruction word.)

(34) EFE - Enable File Error Flip-flop (-CM:B4)

The EFE flip-flop enables or disables the following four priority interrupt conditions:

- 1) File error (see FER below);
- 2) Parity error (see PER below);
- 3) Read compare error (see RCE below);
- 4) Data request late (see DRL above).

If the EFE flip-flop contains 1, a priority interrupt enable level PIE is produced whenever any of the four priority interrupt conditions, FER(1), PER(1), RCE(1), or DRL(1) is asserted. However, if the EFE flip-flop contains 0, these conditions are not allowed to initiate PIE.

Set by:

PTC  $\wedge$  IOB11(1)

Reset by:

CCB

The EFE flip-flop may be set by programming a CONO 270 instruction with a 1 in bit 29. To reset EFE, give a CONO 270 with 0 in bit 19. (The IOB11 input corresponds to bit 29 of the CONO instruction word.)

(35) EFR - Enable File Ready (-CM:B6)

The EFR flip-flop enables or disables the discfile ready priority interrupt condition. If the EFR flip-flop contains 1, a priority interrupt level PIE is produced whenever the file status octoflop is stepped to the discfile ready state DFR. However, if the EFR flip-flop contains 0, the DFR(1) level is not allowed to initiate PIE.

Set by:

PTC  $\wedge$  IOB13(1)

Reset by:

CCB

The EFR flip-flop may be set by programming a CONO 270 instruction with a 1 in bit 31. To reset EFR, give a CONO 270 with 0 in bit 31. (The IOB13 input corresponds to bit 31 of the CONO instruction word.)

(36) EIS - Enable Idle State Flip-flop (-CM:B6)

The EIS flip-flop enables or disables the idle state priority interrupt condition. If the EIS flip-flop contains 1, a priority interrupt level PIE is produced whenever the file status octoflop is reset to the idle state IDS. However, if the EIS flip-flop contains 0, the IDS(1) level is not allowed to initiate PIE.

Set by:

PTC  $\wedge$  IOB14(1)

Reset by:

CCB

The EIS flip-flop may be set by programming a CONO 270 instruction with a 1 in bit 32. To reset EIS, give a CONO 270 with 0 in bit 32. (The IOB14 input corresponds to bit 32 of the CONO instruction word.)

(37) END (-TR:A5)

The discfile control sends an END pulse to the discfile (through a twisted-pair transmission line) as a signal that the current command is finished and that communication may be discontinued. The END pulse disconnects the discfile from the discfile control. After the END pulse has been received, the discfile is ready to receive a new SELECT (sent to the discfile at the PTA pulse of the next DATAO 270 address command).

After receiving the END pulse, the discfile transmits no more than one additional write clock pulse or data bit. Regardless of when the END flip-flop is set, the END pulse is always sent to the discfile at ESP 2 time. If the discfile does not receive either an END, a READ, or a WRITE within an 8- $\mu$ sec guard slot following the last data pulse of the record, an end error is generated (usually causing the CME flip-flop to be set at the discfile control).

Generated by:

ESP 2  $\wedge$  NOP

If the END flip-flop is set, the ESP 1 pulse clears the command register CM0-1. Consequently, the NOP level is asserted when the ESP 2 pulse arrives 2  $\mu$ sec later, and an END pulse is then applied to the discfile.

Note that when the CLR flip-flop is set, the END flip-flop is also set automatically (although the converse is not true). As a result, a CLEAR pulse will never be sent to the discfile unless an END pulse is

sent at the same time. An END pulse may, however, be sent to the discfile without a CLEAR pulse.

(38) END Flip-flop (-CM:B4)

When the END flip-flop is set the ESP 1 pulse that marks the end of the current sector clears the command register CM0-1. The ESP 2 pulse, which follows ESP 1 two  $\mu$ sec later, then sends an END pulse to the discfile. The END pulse terminates the current operation. (See END Pulse above.)

Generated by:

PTC  $\wedge$  IOB5(1)

The END flip-flop may be set by programming a CONO 270 instruction with a 1 in bit 23. To reset END, give a CONO 270 with 0 in bit 23. (The IOB5 input corresponds to bit 23 of the CONO instruction word.)

(39) ERP - Error Pulse (-SC:B5)

An ERP is produced whenever the discfile detects an error condition. The ERP always sets the FER flip-flop. Provided that the priority interrupt enable switch EFE (a flip-flop switch) is set to 1, the FER(1) produces a PIE level. The resulting priority interrupt may be used to notify the programmer that an error has occurred.

When an ERP occurs during the ADT state of the file-control octoflop, it sets the ADE flip-flop as well as the FER; when it occurs during CMS state, it sets the CME flip-flop; and when it occurs during SCS state, it sets the DCE flip-flop. This arrangement not only tells the programmer that an error has been detected, but furthermore when the error has appeared, and therefore what general class of error has occurred. Indicators at the discfile itself can further categorize the error. For a listing and description of the various types of error that the discfile can detect, refer to ADE, CME, and DCE above.

Generated by:

ERROR SIGNAL (from discfile)

The ERROR SIGNAL is transmitted from the discfile to the discfile control through a twisted pair transmission line.

(40) ERROR SIGNAL (-SC:B1)

The discfile sends an ERROR SIGNAL to the discfile control through a twisted-pair transmission line to indicate that a ~~data or sequence~~ <sup>discfile</sup> error has been detected. At the discfile <sup>control</sup> the ERROR SIGNAL is inverted and redesignated ERP. (See ERP above.)

(41) ESP 1 - End of Sector Pulse 1 (-FC:C6)

The ESP 1 pulse, and the ESP 2 pulse which follows it 2  $\mu$ sec later, mark the end of each data sector. The ESP 1 pulse advances the file-control octoflop from SCS state to SCE state. The ESP 1 pulse may also clear CM0-1. This clear function is performed if no further data sectors are to be processed. During output commands (write or read compare), ESP 1 will clear CM0-1 only when the Data Control 136 applies a DA RQ signal to the discfile control. (The DA RQ signal indicates that the data control data accumulator is empty and that no further data is to be sent to the discfile control.) During all commands, output or input, the ESP 1 pulse will clear CM0-1 whenever the END(1) level is asserted.

Generated by:

DCK 1  $\wedge$  SCS(1) plus 5- $\mu$ sec delay

Throughout SCS state, the SCS(1) level enables each DCK 1 clock pulse to restart integrating delay AB01. This delay permits the discfile control to sense the end of each sector of data. When no DCK 1 pulses have been applied to the delay for 5  $\mu$ sec, the delay times out, producing the ESP 1 pulse that signals the end of the sector. The ESP 2 pulse is always generated 2  $\mu$ sec after ESP 1.



(42) ESP 2 - End of Sector Pulse 2 (-FC:C8)

The ESP 2 pulse always occurs 2  $\mu$ sec after the ESP 1 pulse that marks the end of each data sector. The ESP 1 pulse clears out command code bits CM0-1 if and only if no further data sectors are to be processed. If, however, the present operation is to be continued throughout additional sectors of data, the contents of CM0-1 are left intact.

The effect of ESP 2 depends upon whether or not ESP 1 has cleared out CM0-1. If ESP 1 has not cleared CM0-1 ( $\sim$ NOP), then ESP 2 returns the file-control octoflop from SCE state to CMS state and simultaneously sends an appropriate command pulse (READ or WRITE as the case may be) to the discfile. On the other hand, if CM0-1 are cleared at ESP 2 time (NOP), then ESP 2 resets the octoflop from SCE state to IDS state and sends an END pulse to the discfile. If the CLR(1) level is asserted, ESP 2 also applies a CLEAR signal to the discfile.

The ESP 2 pulse sets the SEF flag whenever SCE(1) is asserted. The SCE state of the octoflop lasts for only the 2- $\mu$ sec interval between ESP 1 and ESP 2, but the SEF flag saves SCE for sampling. The SEF remains set until being reset by an SCL pulse. The programmer can reset the SEF flag at will by generating a programmed SCL pulse (by means of a CONO 270 instruction with a 1 in bit 28).

Generated by:

ESP 1 plus 2- $\mu$ sec delay

(43) FCL - File Clear (-AD:C5)

The FCL pulse clears the bit-shift counter BSC0-4, the word counter WCT0-7, and the following six control flip-flops: ACE, ACS, COH, PAR, RCT, and WDC.

Generated by:

IBR ∨ PTA ∨ NDP 1

An FCL pulse is generated by IBR when computer power is first turned on, when the IO reset key is operated, and when a programmed reset is executed. This ensures that the discfile control begins operations in the correct initial state. Whenever a DATAO 270 instruction is used to send a new address to the discfile control, a PTA pulse is produced and the PTA in turn produces an FCL pulse to clear the discfile control. An additional FCL is produced at the NDP 1 pulse that signals the beginning of each sector to be processed.

(44) FER - File Error (-SC:A2)

Provided that the priority interrupt enable switch EFE (a flip-flop switch) is set to 1, the FER(1) produces a PIE level. The resulting priority interrupt may be used to notify the programmer that a file error has occurred. The CONI 270 samples the contents of FER on IOB 34.

Set by:

ERP ∨ ALM ∨ OPR ∨ WRITE LOCKOUT WARNING (from discfile)

Reset by:

SCL

(45) GIVE A CHARACTER (-SC:C7)

The GIVE A CHARACTER pulse is sent to the Data Control 136 accumulator shift logic. The GIVE A CHARACTER pulse signals the data control that the discfile control has accepted the 18-bit character currently stored in the high order end of the data control data accumulator (by clocking it in with an SND pulse), and that unless that character was the last (second) character in the output data word, the data control must shift the contents of its accumulator left by 18 bit-positions in order to bring the next character into the high order bit-positions. If the character just accepted by the discfile control was the last character of the output data word, the GIVE A CHARACTER pulse causes the data control to advance a new 36-bit output data word from its data buffer DB into its data accumulator DA.

Generated by:

DTC

(46) IBR - In-Out Bus Reset (-SC:C1)

At the discfile control, IOB RESET is inverted, and the resulting positive pulse is designated IBR. The IBR pulse itself directly clears the two command code bits CM0 and CM1. Furthermore, IBR produces four additional clear pulses: CCB, CDA, SCL, and FCL. These four pulses clear the command buffer and data accumulator, and reset all status and control flip-flops to the 0 state.

Generated by:

IOB RESET

The IOB RESET pulse (and the resulting IBR pulse) are generated when computer power goes on or when the operator presses the IO reset key on the computer console. The program may also generate a reset.

(47) IDS - Idle State (-FC:B2)

Initial state of the file-control octoflop. The DATAO 270 instruction can transfer a new address into the data accumulator only when the octoflop is in either IDS state or ADT state. Neither the CDA pulse nor the PTA pulse can be generated unless the octoflop is in one of these two states. For the octoflop to be stepped to the SNA state, it must also be in either IDS or ADT state.

Provided that the priority interrupt enable switch EIS (a flip-flop switch) is set to 1, IDS(1) produces a PIE level. The resulting priority interrupt request often is used to notify the programmer that the discfile control has completed the preceding operation, and is ready to receive a new data address. The CONI 270 samples IDS on IOB18.

Generated by:

IBR  $\vee$ .

MCL(1)  $\vee$ .

ESP 2  $\wedge$  NOP

The IBR pulse resets the file-control octoflop to IDS state when computer power is first turned on, when the IO reset key is operated, and

when a programmed reset is executed. This ensures that the discfile control begins operations with the octoflop in IDS state. The octoflop is also reset to IDS state when the master clear button is operated.

At the end of each sector of data the ESP 2 pulse causes the octoflop to return from SCE state to either IDS state or to CMS state. The octoflop is reset from SCE to IDS whenever command code bits CM0 and CM1 are both in the 0 state (specifying NOP). If CM0 and CM1 are not both in the 0 state ( $\sim$ NOP), then instead of returning from SCE to IDS state, the octoflop returns from SCE to CMS state.

(48) IOB CONO CLR - In-Out Bus Conditions Out Clear (-CM:C3)

When gated by the SEL level, the IOB CONO CLR pulse produces a CCB pulse which clears the entire command buffer if CCM is asserted (and which otherwise clears the nine low-order bits of the command buffer, but leaves CM0 and CM1 unchanged).

The processor CONO instruction produces an IOB CONO CLR pulse followed one microsecond later by an IOB CONO SET pulse. These two command pulses are effective only at that IO device or control unit specified by the CONO instruction device selection code.

(49) IOB CONO SET - In-Out Bus Conditions Out Set (-CM:D3)

When gated by the SEL level, the IOB CONO SET pulse produces a PTC pulse which gates new control information into the command buffer. (A new command code is gated into CM0 and CM1 only if CCM is asserted. Otherwise the contents of these two bits are left unchanged.)

The processor CONO instruction produces an IOB CONO SET one microsecond after IOB CONO CLR.

(50) IOB DATA CLR - In-Out Bus Data Clear (-AD:B1)

The first processor signal to reach the discfile control during the DATAO instruction is IOB DATA CLR. When gated by appropriate conditions, the IOB DATA CLR pulse produces a CDA pulse that clears the data accumulator DA0-19.

The processor DATAO instruction produces an IOB DATA CLR pulse followed one microsecond later by an IOB DATA SET pulse. These two command pulses are effective at the discfile control only when the DATAO instruction device selection code is 270 octal. (This causes the SEL level to be asserted within the discfile control.)

(51) IOB DATA I - In-Out Bus Data In (-AD:A1)

The IOB DATA I level is inverted to produce the DTP level. During the 2.5  $\mu$ sec while DTP is present, the contents of the data accumulator and the bit shift counter are placed on the IO bus. The processor reads this information in from the bus at the 2- $\mu$ sec point.

The processor DATAI instruction produces a negative 2.5- $\mu$ sec IOB DATA I level. This command level is effective at the discfile control only when the DATAI instruction device selection code is 270 octal. (This causes the SEL level to be asserted within the discfile control.)

(52) IOB DATA SET - In-Out Bus Data Set (-AD:B1)

When gated by appropriate conditions, the IOB DATA SET pulse produces a PTA pulse which loads a discfile address from IOB17-35 into the data accumulator of the discfile control.

The processor DATAO instruction produces an IOB DATA SET one microsecond after IOB DATA CLR.

(53) IOB RESET - In-Out Bus Reset (-SC:C1)

The IOB RESET pulse is a negative ungated clear pulse which is applied to all IO devices and control units. It clears the control registers and data buffers of all equipment attached to the in-out bus. At the discfile control, IOB RESET is inverted, and the resulting positive pulse is designated IBR.

The IOB RESET pulse is generated when computer power goes on or when the operator presses the IO reset key on the computer console. The program may also generate a reset.

(54) IOB STATUS - In-Out Bus Status (-CM:D7)

The IOB STATUS level is gated by SEL to produce an STP level. During the 2.5  $\mu$ sec while STP is present, a variety of CONI status information (including the contents of the command buffer, the file-control octoflop, the error-status flags, and the relay-meter test switches) is placed on the IO bus. The processor reads this information in from the bus at the 2- $\mu$ sec point.

The processor CONI instruction produces a negative 2.5- $\mu$ sec IOB STATUS level. This command level is effective at the discfile control only when the CONI instruction device selection code is 270 octal. (This causes the SEL level to be asserted within the discfile control.)

(55) IOS3-9 - In-Out Selection Lines (-SC:D1)

Two IOS lines are associated with each of the seven bits 3-9. These 14 lines represent both states of the 7 bits of the device code contained in bits 3-9 of the instruction register (assertion is at ground). Every device control contains one or more diode nets, each of which receives inputs from seven of the 14 IOS lines, one from each bit in IR3-9. The input connections that are wired in determine the selection code for the device, and its control unit then responds to IOT commands only when the appropriate number appears in the device code portion of the instruction word. The discfile control uses the device code 270. The diode net output corresponding to this code is designated SEL.

(55A) MSB - Minus Five Volt BUS (-TR:A2)

(56) MCL - Master Clear (-CM:D7) The MSB line provides a

When pressed, the MCL pushbutton closes two normally-open switches in the discfile control. One of these switches is connected across the two ends of a twisted-pair line to the discfile. The other switch applies +10 vdc through a switch filter to a pair of series-connected inverters, thus producing the MCL level at both polarities.

↓ terminating supply for the twisted-pair transmission lines.



When the normally open-circuited twisted pair is shorted by operating the MCL pushbutton, the discfile executes a master clear function. This includes the removal of power from the previously selected head positioner, and the clearing of the discfile logic and error indicators. The discfile requires 20 ms to complete the master clear operation; throughout this period the discfile will not accept any commands.

Within the discfile control, the MCL level prevents the generation of the CDA and PTA pulses, and resets the file-control octoflop to IDS state. The CONI 270 samples the MCL level on IOB 3.

Generated by:

MCL pushbutton (at discfile control)

The MCL pushbutton is located on the front of the discfile control logic at the right end of rack A. The master clear should be given when the system is first turned on and when one programmer replaces another at the console.

(57) MRB - Meter Reading Bad (-SC:D3)

The address sequencing relays in the discfile can readily be tested with the aid of a relay test program run from the processor. The program cycles through all the sequencing relays in a predetermined order. As each relay is tested, a discfile voltmeter indicates whether or not its contact resistance is normal. If the contact resistance is excessive, a high meter reading shows that the relay is bad. The maintenance engineer performing the test should then press the Meter Reading Bad

pushbutton, and thus produce an MRB level at the discfile control.

The CONI 270 samples the MRB level on IOB10.

Generated by:

MRB pushbutton (at discfile)

When pressed, the MRB pushbutton opens a normally-closed switch in the discfile. This switch is connected across the two ends of a twisted-pair line to the discfile control. In the normal quiescent state the closed switch returns +10 vdc to a switch filter in the discfile control. When the MRB pushbutton is operated, the normally-closed switch is opened, removing the +10 vdc from the switch filter and causing the MRB level to be negatively asserted.

(58) MRG - Meter Reading Good (-SC:D3)

See MRB above. If there is a low meter reading, showing normal contact resistance for the relay under test, the maintenance engineer performing the test should then press the Meter Reading Good pushbutton and thus produce an MRG level at the discfile control. The CONI 270 samples the MRG level on IOB9.

Generated by:

MRG pushbutton (at discfile)

(59) NDP 1 - New Data Pulse 1 (-FC:B6)

The NDP 1 pulse, and the NDP 2 pulse which follows it 1.0  $\mu$ sec later, precede (by a number of milliseconds) the beginning of each new sector of data. The NDP 1 pulse advances the file-control octoflop from

CMS state to SCS state. A READ or WRITE command pulse is sent to the discfile at the beginning of the CMS state; CMS state is ended 200  $\mu$ sec later when NDP 1 advances the octoflop to SCS state. The NDP 1 pulse also generates an FCL pulse which clears the bit-shift counter BSC0-4, the word counter WCT0-7, and the following five control flip-flops: ACE, ACS, COH, WDC, and RCT.

Generated by:

CSP  $\wedge$  ALS(1) .  $\vee$  . ESP(2)  $\wedge$  NOP :  $\wedge$  :  
 plus 200- $\mu$ sec delay  $\wedge$  CMS(1)

The NDP 1 pulse is produced by the termination of a 200- $\mu$ sec delay that is started whenever the octoflop is advanced to CMS state. The NDP 2 pulse is always generated 1.0  $\mu$ sec after NDP 1. The first line of the conditions listed above is identical to the conditions that step the octoflop to CMS state. The requirement that CMS(1) still be asserted at the expiration of the delay is to guard against the unlikely contingency that an IOB reset pulse might occur during the 200- $\mu$ sec delay. If that should happen, it would not be desirable to advance the octoflop to SCS state. The octoflop would instead be reset to IDS state and neither the NDP 1 nor the NDP 2 pulse would be required.

(60) NDP 2 - New Data Pulse 2 (-FC:B8)

The NDP 2 pulse always occurs 1.0  $\mu$ sec after the NDP 1 pulse that steps the file status octoflop to SCS state. If the Data Control 136 has not yet been selected to the discfile control at NDP 2 time, then the SEL 5

level is ground, and the data request late flip-flop DRL is set by NDP 2. Provided that the priority interrupt switch EFE (a flip-flop switch) is set to 1, DRL(1) produces a PIE level. The resulting priority interrupt request may be used to notify the programmer that the intended operation cannot be performed until he has sent the data control an appropriate CONO command.

The NDP 2 pulse also is used to initialize the bit-shift counter prior to the commencement of each data sector. An FCL pulse that clears the bit-shift counter is initiated by NDP 1. The NDP 2 pulse then sets BSC3 to the 1 state, thus leaving the counter with contents equal to 2 at the beginning of the data sector. Although the counter always overflows when its contents are 20, if BSC3 is initially set before counting is begun, only 18 counts are required to reach the overflow count of 20. This ensures that overflow occurs at the DCK 1 clock corresponding to the eighteenth and final data bit of the first 18-bit character. (For the remaining characters of the data sector, SCS(1) enables BSC3 to be set to 1 at the end of each character.)

Generated by:

NDP 1 plus 1.0- $\mu$ sec delay

(61) NOP - No Operation (-CM:A2)

The NOP level, and its complement,  $\sim$ NOP, control two branch points of the file-control octoflop cycle. The first of these branch points occurs at the end of the 1-ms DFR state; at that time, the octoflop either advances

to ALS state or returns to ADT state, the choice depending upon whether or not NOP is asserted. If  $\sim$ NOP is asserted, indicating that a command has already been given to the discfile control, then an ALP pulse is sent to the discfile, and the octoflop is advanced to ALS state. However, if NOP is asserted, indicating that as yet no command has been received from the processor, the octoflop returns to ADT state.

The octoflop remains in ADT state until the next RDY pulse initiates another DFR state. After 1 ms, that DFR state ends, and the branch-point decision is repeated. The discfile control continues to oscillate between ADT and DFR until a command code arrives from the processor. The first such command to arrive ends NOP and enables the octoflop to advance to ALS state.

The second branch point of the octoflop cycle that is controlled by the NOP level occurs at the ESP 2 pulse marking the end of the SCE state. If NOP is then asserted, indicating that the current operation is finished, the octoflop is immediately reset to IDS, and the discfile control is ready to accept a new address (which can be sent to it by means of a DATAO 270 instruction). On the other hand, if the current operation is not yet finished, but is to continue for one or more additional sectors of data, then  $\sim$ NOP is asserted and the octoflop is stepped to CMS state rather than to IDS state from SCE state. At the same time, another READ or WRITE command pulse is sent to the discfile, causing the current discfile address to be incremented.

Generated by:

CM0(0) ^ CM1(0)

The NOP level is asserted only if both bits of the command register CM0-1 contain 0. The other three possible configurations of these two bits each correspond to one of the three discfile command codes. (See RDC, RED, and WRT below.)

(62) ODO - Odd Data Ones (-TR:C1)

Addresses and data are transmitted to and from the discfile on four twisted-pair transmission lines. These four twisted-pair lines are used in sets of two; one line of each set is pulsed for a 1, the other line for a 0. Two such sets of two lines are used. This allows alternate bits (odd and even) to be transmitted on different lines, thus halving the data transmission frequency.

For address transmission, and for write commands, each ODO pulse is amplified by pulse amplifier D30 and then transmitted to the discfile over the odd data 1's twisted pair.

During read and read compare commands, if RDS is asserted (indicating that the word counter has not yet reached its final count of 128), each ODO pulse initiates an RDO pulse (Read Data Ones) and starts the DCK clock-chain. The RDO pulse in turn is used to complement RCT, and (for read commands only) to set DA2.

Generated by:

Odd data 1 (read at discfile).  $\vee$  . :

WCO  $\wedge$  :

COH(0)  $\wedge$  DA19(1) .  $\vee$  .

COH(1)  $\wedge$  PAR(0)

When reading, or read comparing, the ODO pulses enter the discfile control on the odd data 1's line from the discfile. The two series-connected inverters through which the ODO pulses are passed before generating RDO are used for noise isolation and for adjusting the voltage reference to the usual DEC logic levels (-3 vdc to ground).

During writing, the ODO pulses are clocked by the write clock odd, WCO. So long as address bits or data bits are being sent to the discfile, COH(0) is asserted; COH(1) is asserted only when the parity bit is sent to the discfile. Because odd parity is generated for both address and data, a 1 parity bit is sent to the discfile when the total number of 1 bits in the address or data word is even; i. e. when PAR(0) is asserted.

(63) ODZ - Odd Data Zeros (-TR:C2)

See ODO above.

For address transmission and for write commands, each ODZ pulse is amplified by pulse amplifier D30 and then transmitted to the discfile over the odd data 0's twisted pair.

During read and read compare commands, if RDS is asserted, each ODZ pulse initiates an RDZ pulse, and starts the DCK clock chain. The RDZ pulse resets DA2, but only during read commands.

Generated by:

Odd data zero (read at discfile) .  $\vee$  . :

WCO  $\wedge$  :

COH(0)  $\wedge$  DA19(0) .  $\vee$  .

COH(1)  $\wedge$  PAR(1)

So long as address bits or data bits are being sent to the discfile, COH(0) is asserted; COH(1) is asserted only when the parity bit is sent to the discfile. Because odd parity is generated for both address and data, a 0 parity bit is sent to the discfile when the total number of 1 bits in the address or data word is odd as it stands (without the parity bit); i. e. when PAR (1) is asserted.

$\rightarrow$  Insert page 71b here

(64) OPR - Operable (-SC:C5)

When the OPR level is negated ( $\sim$ OPR), the FER flip-flop is set immediately. Provided that the priority interrupt enable switch EFE (a flip-flop switch) is set to 1, FER(1) produces a PIE level. The resulting priority interrupt request can notify the programmer that the discfile is not operable.

It is not permissible to change the command code in CM0-1 unless the OPR level is asserted. For this reason, OPR is used as a necessary input condition for the generation of the CCM level. The CONI 270 samples  $\sim$ OPR, the negation of Operable, on IOB35.

Generated by:

OPERABLE (from discfile).



(63A) OPERABLE (-SC:C2)

The discfile sends an OPERABLE signal to the discfile control through a twisted-pair transmission line to indicate that the discfile is operable. At the discfile control, the OPERABLE signal is applied to a switch filter and a pair of series-connected inverters and redesignated OPR. (See OPR below.)

This signal is generated by the closure of a relay within the discfile. The relay closure shunts the discfile end of a twisted-pair line, applying +10 vdc to a switch filter and two series-connected inverters, and thereby generating the OPERABLE signal at both polarities; see Figure -SC:C2-5.

The discfile will not close the OPERABLE relay under any of the following five conditions:

- 1) If the output of the positioner power supply in any disc unit falls below normal.
- 2) If a malfunction occurs in the flying-head air supply.
- 3) Should the ambient temperature in the logic unit or in any of the disc units rise to the alarm level.
- 4) If the logic unit or any disc unit is in test mode.
- 5) If the POWER OFF pushbutton at the logic unit is depressed.

Note that there cannot be an ALARM signal when the OPERABLE signal is present, although absence of ALARM does not guarantee the presence of OPERABLE. ~~Conditions 1, 2, and 3 above generate an ALARM; conditions 4 and 5 ordinarily do not. (See ALM above.)~~

(65) PAR - Parity Accumulator Flip-flop (-AC:A8)

During the read and read compare commands, the PAR flip-flop accumulates the parity of the 36 data bits and the 37th (parity) bit of each input data word. The DCK 2 pulse that is initiated by the parity bit samples the final state of PAR, and sets the PER flip-flop if PAR contains 0 (indicating that the data word currently being read shows incorrect parity).

Although a separate parity test is made for each word of the sector being processed, once any parity error is detected, the PER flip-flop remains set until reset by SCL; see PER below.

The PAR flip-flop serves an entirely different function during address transfers and write commands. For these operations, the PAR flip-flop does not test parity, but instead generates it. During SNA state of the file-control octoflop, 21 address bits are transmitted to the discfile. This includes 19 address bits, the read-next-sector bit, and a final parity bit chosen so as to make the parity of the full 21-bit address odd. The inclusion of a parity check bit in the address format permits the discfile to verify the accuracy of each address transmission.

A parity check is also provided during write operations. Each output data word sent to the discfile includes a total of 37 bits: 36 data bits followed by a 37th (parity) bit chosen so as to make the parity of the entire 37-bit data word odd.

Cleared by:

FCL  $\vee$ :

DCK 2  $\wedge$  COH(1)

Complemented by:

RDO  $\vee$  :

SDR  $\wedge$  DA19(1)  $\cdot$   $\wedge$   $\cdot$  SNA(1)  $\vee$  WRT

The PAR flip-flop is initially cleared by the FCL pulse. An FCL occurs at the IOB reset, at PTA, and at the NDP 1 pulse that signals the beginning of each data sector. For both input and output operations, the

second clear condition listed above occurs immediately following the sampling or use of the contents of PAR. During read and read compare, the DCK 2 pulse that clears PAR is the same DCK 2 that samples the state of PAR and (if PAR contains 0) sets PER. For write commands, the DCK 2 pulse that clears PAR follows the parity-bit write clock by about 400 nsec.

The PAR complement conditions implement both the parity testing and the parity generating functions described above. For read and read compare, each RDO pulse represents the reading of a 1 bit (data or parity); therefore each RDO complements PAR.

During address transfers and write commands, the complement conditions are somewhat different. With the output operations, the purpose of the PAR complement logic is to generate an appropriate odd parity bit. Consequently, the PAR flip-flop must be complemented by each non-zero address or data bit that is transferred out, but not by either the address parity bit or the output data parity bit. (After these conditions are satisfied, the correct output parity bit can be generated by simply using the complement of the final state of the PAR flip-flop; see, for example, ODO and ODZ above.)

The second line of the complement conditions listed above accomplishes just this logical function. The SNA(1) level is asserted throughout the address transmission to the discfile, and the WRT level is asserted whenever a write operation is being executed. The SDR pulse is produced by  $DCK\ 2 \wedge COH(0)$ . For both address transmission and data operations,

the COH flip-flop is set to 1 state by the DCK 2 pulse associated with the the bit that immediately precedes the parity bit (the 20th address bit, or the 36th data bit as the case may be). Consequently, no SDR pulse accompanies the transmission of either the address parity bit or the parity bit of an output data word. Although the PAR flip-flop is complemented by all other non-zero address and data bits transferred out to the discfile, it is not complemented by the associated parity bits.

(66) PER - Parity Error (-SC:A5)

Provided that the priority interrupt enable switch EFE (a flip-flop switch) is set to 1, PER(1) produces a PIE level. The resulting priority interrupt request may be used to notify the programmer that a parity error has been detected during a read or a read compare operation. The CONI 270 samples PER on IOB33.

Set by:

$DCK\ 2 \wedge CM1(1) \wedge COH(1) \wedge PAR(0)$

Reset by:

SCL

The CM1(1) level is asserted during read and read compare commands. The only DCK 2 pulses that coincide with the assertion of COH(1) are the DCK 2 pulses that are initiated by the final bits (parity bits) of the successive 37-bit data words making up the sector that is being processed. If the PAR flip-flop is left in the 0 state after such a parity bit has been read, then a parity error is indicated. (Odd parity is used throughout the

discfile control; see PAR above.)

Note that this parity test requires somewhat compressed timing. The DCK 2 pulse that samples PAR (and sets the PER flip-flop if PAR contains 0) is initiated by the very reading of the parity bit itself, and that parity bit may require PAR to be complemented. For example, assume that the 36 data bits of the word being read from the disc have even parity. Unless an error has occurred, the 37th (parity) bit should then be 1. If it is 1, the PAR flip-flop is complemented (from 0 to 1) at the parity bit RDO time, thus leaving only about 400 nsec for PAR(0) to be negated before it is sampled by the DCK 2 pulse.

(67) PIA0-2 - Priority Interrupt Assignment Flip-flops 0-2 (-CM:B7, 8)

The processor can assign a priority-interrupt request channel to the discfile control by means of a CONO 270 instruction that sets PIA0-2 to some octal number from one to seven. If all three PIA bits are left 0, no priority interrupt channel is assigned. By asserting the PIE level, the discfile control can request a priority interrupt break on the assigned channel. The lower the channel number, the higher the priority. Breaks on channel 1 take precedence over all other breaks. Breaks on channel 2 take precedence over all breaks except those on channel 1, etc.

The PI request is sent to the processor by grounding the appropriate PIR line, i. e. the line selected from PIR1-7 by the contents of PIA0-2. If all three PIA bits are 0, the assertion of PIE has no effect on PIR0-7. The discfile control is then disabled from requesting a priority interrupt break.

Set by:

PIA0: PTC  $\wedge$  IOB15(1)

PIA1: PTC  $\wedge$  IOB16(1)

PIA2: PTC  $\wedge$  IOB17(1)

Reset by:

CCB

Like all other bits of the command buffer, the three PIA bits can be set to any desired configuration by a CONO 270 command from the processor. (The IOB15-17 inputs correspond to bits 33-35 of the CONO instruction word.)

(68) PIE - Priority Interrupt Enable (-CM:A7)

By asserting the PIE level, the discfile control can request a priority interrupt break on the assigned channel, channel 1-7. The PI request is sent to the processor by grounding the appropriate PIR line. See PIA above, and PIR below.

Generated by:

IDS(1)  $\wedge$  EIS(1) .  $\vee$  :

DFR(1)  $\wedge$  EFR(1) .  $\vee$  :

SEF(1)  $\wedge$  EES(1) .  $\vee$  :

FER(1)  $\vee$  PER(1)  $\vee$  RCE(1)  $\vee$  DRL(1) .  $\wedge$  . EFE(1)

When set to 1, each of the four flip-flop switches, EIS, EFR, EES, and EFE, enables the corresponding interrupt condition, or conditions (in the case of EFE), to assert the PIE level and to request a priority interrupt break on the assigned channel.

(69) PIR1-7 - Priority Interrupt Request Lines 1-7 (-CM:A7,8)

From the discfile control to the processor run seven priority interrupt request lines PIR1-7. The discfile control can request a priority interrupt break on the assigned channel by applying a ground level to the corresponding PIR line. See PIA above.

PIR<sub>n</sub> generated by:

PIE ^ :

Contents of PIA0-2 = n octal

Unless all three priority interrupt assignment bits PIA0-2 contain 0, the assertion of PIE initiates a priority interrupt request on the channel selected by PIA0-2. If PIA0-2 all contain 0, no priority interrupt channel is assigned, and no priority interrupt breaks can be requested.

(70) PTA - Processor to Accumulator (-AD:B8)

This pulse loads IOB17-35 into the data accumulator. Bits DA0-11 are loaded from IOB18-29, DA12 remains cleared, DA13-18 are loaded from IOB30-35, and DA19 is loaded from IOB17.

Although the logic of the Discfile 5022 provides for a seven-bit sector address, the present 44-sector format requires only six address bits. For this reason DA12 always remains cleared when the processor sends a new address to the discfile control. The read-next-sector bit is sent to the discfile control over IOB17. However, the format of the discfile logic requires this bit to be at the low-order end of the address. Consequently IOB17 is loaded into DA19.



The PTA pulse also initiates the SCL and FCL clear pulses which clear most of the status and control flip-flops within the discfile control (but not the file-control octoflop).

Furthermore, the PTA pulse starts a 15- $\mu$ sec delay. At the termination of this delay, an ADS pulse is produced and the file-control octoflop is stepped from IDS or ADT state to the SNA state.

Generated by:

IOB DATA SET  $\wedge$  .

SEL  $\wedge$  .

MCL(0)  $\wedge$  .

IDS(1)  $\vee$  ADT(1)

The processor instruction DATAO 270 sends an address to the discfile control and initiates the seek for the addressed sector at the discfile. The DATAO instruction produces an IOB DATA CLR pulse followed one microsecond later by an IOB DATA SET. The same gating conditions that permit the IOB DATA CLR to produce a CDA pulse (thereby clearing the data accumulator) also permit the IOB DATA SET to produce a PTA pulse.

In order for the IOB DATA CLR and IOB DATA SET pulses to produce CDA and PTA pulses respectively, the DATAO instruction device selection code must be 270 octal. (This causes the SEL level to be asserted within the discfile control). The master clear switch must be open, since it is not proper to send a new address to the discfile control while in the process of executing a master clear operation. Finally, the discfile

control must be in either the IDS state or the ADT state (the only two states in which it is permissible to send a new address to the discfile control).

(71) PTC - Processor to Command (-CM:C4)

The PTC pulse always loads the nine low-order bits of the command buffer (CLR, EES, EFE, EFR, EIS, END, and PIA0-2) with CONO command bits from the IO bus. If the CCE level is asserted, the PTC pulse also loads the two command bits CM0 and CM1 from the bus.

Generated by:

IOB CONO SET  $\wedge$  SEL

The processor instruction CONO 270 sends command information to the command buffer of the discfile control, thereby setting up the control to execute the required commands (read, write, etc.). The CONO instruction produces an IOB CONO CLR pulse, followed one microsecond later by an IOB CONO SET. These pulses in turn produce CCB, which clears the command buffer, and PTC, which loads the command buffer with the new command information.

(72) RCE - Read Compare Error Flip-flop (-SC:A6)

When this flip-flop is set to 1, it indicates that a read compare error has occurred. During RDC command, the RCE flip-flop is set whenever an output data bit from the Data Control <sup>136</sup> fails to match the corresponding input data bit read from the discfile.

Provided that the priority interrupt enable switch EFE (a flip-flop switch) is set to 1, RCE(1) produces a PIE level. The resulting priority interrupt request may be used to notify the programmer that a read compare error has been detected. The CONI 270 samples RCE on IOB32.

Set by:

DCK 3  $\wedge$  RDC  $\wedge$  RCT(1)

Reset by:

SCL

The RDC command compares one or more sectors of output data (or even some fraction of a full sector) with corresponding input data read from the discfile. The comparison is executed one bit at a time, but does not include parity bits. At the first pair of bits that are not identical, the comparison fails. The failure is detected by the fact that the DCK 2 pulse leaves the RCT flip-flop in the 1 state; see RCT below. The RCT remains set for only about 400 nsec; it is cleared at DCK 3, and the comparison then continues until the output data is exhausted. Although RCT is cleared soon after being set, the RCE flip-flop saves the read compare error for sampling. The same DCK 3 pulse that clears RCT sets RCE, and RCE remains set until being reset by SCL.

(73) RCT - Read Compare Test Flip-flop (-SC:A8)

If, during a read compare, RCT contains 1 at DCK 2 time, then the DCK 3 pulse sets the RCE flip-flop, thus indicating a read compare error.

Cleared by:

FCL  $\vee$  DCK 3

Complemented by:

RDO  $\wedge$  COH(0)  $\cdot$   $\vee$  :

SDR  $\wedge$  DA19(1)

The RCT flip-flop is initially cleared by the FCL pulse. An FCL occurs at IOB reset, at PTA, and at the NDP 1 pulse that signals the beginning of each data sector. The DCK 3 pulse also clears RCT. This clear occurs after each data bit comparison. The same DCK 3 pulse that clears RCT also sets RCE if RCT contains 1 (indicating a read compare error).

The first line of the complement conditions listed above represents input data read from the discfile; the second line represents output data from the Data Control 136. Throughout the read compare command, RCT is complemented twice or not at all for each error-free bit comparison. Single complementing, which leaves RCT in the 1 state after the DCK 2 pulse, occurs only when an input data bit fails to match the corresponding output data bit; i. e. when there is a read compare error. No output parity bits are generated during RDC commands, and for read comparison purposes the incoming parity bits are ignored. (Note, however, that the incoming data from the discfile is subject to the normal parity test during read compare commands, just as during read commands. See PER above.)

The clock chain is started by incoming data pulses from the discfile. Each non-zero bit produces an RDO pulse. Every RDO except those that are initiated by input parity bits (and so are screened out by the 1 state

of the COH flip-flop) complements the RCT flip-flop from 0 to 1. This is the first complement operation (input data).

The second complement operation (output data) is clocked by the SDR pulse. The SDR pulse is produced by  $DCK\ 2 \wedge COH(0)$ . Every incoming data pulse starts the clock chain, and thus results in the generation of a DCK 2 pulse. Except for parity bits (again screened out by the 1 state of COH), every DCK 2 generates an SDR pulse. Provided that the output data bit in DA19 is a 1, the SDR pulse recomplements the RCT flip-flop at DCK 2 time.

The two sets of complement conditions work together to effect the bit-by-bit read comparison. If both the input and the output data are 0 bits, RCT will not be complemented at all, but will remain in its initial 0 state. If both bits are 1, the result is the same; although RCT is complemented twice, it is still left in the 0 state after the DCK 2 pulse. If, however, the input and output data bits are different, RCT is complemented only once, and is therefore left in the 1 state after DCK 2. The RCE flip-flop is then set by the DCK 3 pulse, thus saving the read compare error indication.

(74) RDC - Read Compare Command (-CM:A1)

This level indicates that the contents of CM0-1 specify the read compare command. If the RCT flip-flop ever remains in the 1 state at DCK 3 time while RDC is asserted, then the RCE flip-flop is set, indicating the detection of a read compare error.

There are certain other operations of the discfile control that are common to both the read compare command and the write command. These operations are enabled by the CM0(1) command-pair function rather than by the RDC level. Similarly, the CM1(1) command pair function is used instead of the RDC level to enable other operations that are common to the read compare command and the read command. (See CM0-1 above for a more detailed description of these two command-pair functions and the logical operations which they govern.)

Generated by:

CM0(1)  $\wedge$  CM1(1)

(75) RDO - Read Data Ones (-TR:D2)

During read commands, every RDO pulse except those initiated by data word parity bits loads a 1 into bit DA2. During <sup>both read and</sup> read compare commands, every RDO pulse except those initiated by data word parity bits complements the RCT flip-flop. For both read and read compare commands, every RDO pulse (including those produced by the parity bits) complements the PAR flip-flop.

Generated by:

EDO  $\vee$  ODO  $\cdot$   $\wedge$ :

RDS

For both the read and read compare commands, the RDS level enables each EDO or ODO input data pulse to initiate an RDO pulse. During both commands, the RDS level is asserted until the WCT7 flip-flop is set to 1;

this always occurs when the word count reaches 128. For the read command only, WCT7 can also be set to 1 by setting the END flip-flop. (See RDS below.)

(76) RDS - Receive Data Signal (-TR:C6)

The RDS level enables the generation of RDO and RDZ data pulses. When RDS is asserted, every EDO or ODO input data pulse from the discfile produces an RDO pulse, and every EDZ or ODZ produces an RDZ pulse.

The RDS level also determines what signals are allowed to start the DCK clock chain. The assertion of the RDS level prevents the WCE and WCO pulses from triggering DCK 1. However, the RDS level must be asserted in order for the input data pulses (EDO, EDZ, ODO, and ODZ) to trigger DCK 1.

Throughout the address transmission, the RDS level is not asserted (even if the command is read or read compare) because, when the file-control octoflop is in SNA state, SCS(1) is not asserted. Because RDS is negated, the WCE pulses initiated by the address clock are able to trigger DCK 1 and thus to initiate the DCK clock chain.

During the execution of the write command, CM1 is in the 0 state and therefore the RDS level is not asserted. Because RDS is negated, ~~both the WCE and WCO~~ **THE WRITE CLOCK EVEN and WRITE CLOCK ODD** pulses initiated by the write clock control track in the discfile (inner-zone or outer-zone track depending upon the location of the sector to be written) are allowed to trigger DCK 1.

For both the read and the read compare commands, the assertion of the RDS level enables each input data pulse (EDO, EDZ, ODO, or ODZ) to trigger DCK 1 and thus initiate the DCK 1 clock chain.

Generated by:

$CM1(1) \wedge SCS(1) \wedge WCT7(0)$

The WCT7(0) condition provides the means of terminating the read and read compare commands. During both of these commands, the RDS level is asserted until the WCT7 flip-flop is set to 1; this always occurs when the word count reaches 128. For the read command only, WCT7 can also be set to 1 by setting the END flip-flop. When END contains 1, the first DCK 1 pulse to appear sets WCT7 and thereby ends RDS and turns off the DCK clock. With RDS no longer asserted, neither RDO nor RDZ pulses can be generated. The turn-off of the DCK clock initiates the remaining operations required to end the command and reset the system. The read command can thus be terminated at any point by merely setting the END flip-flop.

(77) RDY - Ready (-TR:C5)

Provided that ADE(0) is asserted (indicating that no address errors are present), the RDY pulse advances the file-control octoflop from ADT state to DFR state, and starts the 1-ms delay that measures the duration of DFR. If, at the termination of this delay, no command code is present in CM0-1 (NOP), the octoflop returns from DFR state to ADT state. However, if a command code is present ( $\sim$ NOP), then an ALP pulse is



sent to the discfile, and the octoflop is advanced to ALS state.

Generated by:

READY  $\wedge$  CLR(0)

Except when the CLR flip-flop is set, each READY pulse from the discfile produces a RDY pulse within the discfile control. When CLR is set, END is also set, and it is not desirable to generate RDY pulses.

While CLR is set, the discfile control cannot advance beyond ADT state.

When the read-next-sector bit is 0, the discfile sends the discfile control one READY pulse for each 52-ms revolution of the discs. The pulse is transmitted when the discfile senses the header of the sector immediately preceding the sector to be operated upon.

If the read-next-sector bit is 1, the discfile sends a READY at every sector; i. e. either four or seven times each revolution (depending upon whether the addressed track is in the inner or outer zone of the addressed disc).

Once an ALERT pulse has been accepted by the discfile, no further READY signals are emitted. The ALERT is always followed 15  $\mu$ sec later by a READ or WRITE pulse. Since the READY pulse is sent at the header of the "get ready" sector preceding the sector to be operated upon, the ALP and the READ or WRITE command pulse arrive in ample time to govern the operations to be performed.

(78) RDZ - Read Data Zeros      -(TR:D3)

During read commands, every RDZ pulse except those initiated by data word parity bits loads a 0 into bit DA2.

Generated by:

EDZ  $\vee$  ODZ . . :

RDS

For both the read and read compare commands, the RDS level enables each EDZ or ODZ input data pulse to initiate an RDZ pulse. During both commands, the RDS level is asserted until the WCT7 flip-flop is set to 1; this always occurs when the word count reaches 128. For the read command only, WCT7 can also be set to 1 by setting the END flip-flop. (See RDS above.)

(79) READ      (-TR:A7)

The discfile control sends a READ pulse to the discfile through a twisted-pair transmission line to command the discfile to read a sector. If an additional READ signal is sent during the 8- $\mu$ sec guard slot after the final data pulse of the sector, then the discfile increments its stored address by 1 and reads the next sector as well.

Generated by:

CSP  $\wedge$  CM1(1) .  $\vee$ :

ESP 2  $\wedge$  CM1(1)

The CM1(1) command-pair function is asserted during the read and read compare commands. For both these commands, a READ pulse is

sent to the discfile at the CSP pulse that precedes the beginning of the first sector of the command. If the command code is still in the command register CM0-1 after the ESP 1 pulse marking the end of a given sector (indicating that the command is to continue to read or read compare additional sectors), then the closely following ESP 2 sends another READ pulse to the discfile. This process can continue throughout the 44 sequentially addressed sectors at a given disc position before the same data is read a second time. To read a file containing more than 44 sectors the programmer must give an additional DATAO 270 instruction that changes the disc and/or position fields.

(80) READY (-TR:A4)

When the discfile is ready to be alerted for a read or write operation it sends a READY pulse to the discfile control. The READY pulse is sent to the discfile control through the same twisted-pair line upon which the CLEAR pulse is received. The READY pulse marks the completion of the discfile's address seek position. It is generated after the positioner has settled on the address track and the read-write head has sensed the header of the "get ready" sector immediately preceding the sector in which the reading or writing is to be performed.

If the read-next-sector bit is 0, the discfile sends the discfile control only one READY pulse for each revolution of the discs. That pulse is transmitted when the discfile senses the header of the sector immediately preceding the sector to be operated upon. The header must agree completely with the entire address that has been sent to the discfile.

However, if the read-next-sector bit is 1, complete matching of the stored address to the header sensed is not required. It is sufficient to produce a READY if the header that is sensed agrees with the first sixteen bits of the address. Those sixteen bits comprise the disc and position fields, and the track portion of the record field. The header that is sensed need not, in order to generate a READY pulse, match the next three address bits, those which specify a single sector within the addressed track. (The addressed track may contain four or seven sectors depending upon whether it is located in the inner or outer zone of the addressed disc.) Once the discfile has found the addressed track, it sends the discfile control a READY at every sector; i. e. four or seven times each revolution. The READY pulses continue until an ALERT pulse has been received by the discfile; once the ALERT has been accepted, no further READY pulses are generated.

(81) RED - Read Command (-CM:A2)

This level indicates that the contents of CM0-1 specify the read command. When COH(0) is also asserted (indicating that the current RDO or RDZ pulse has been initiated by a data bit rather than by a parity bit) the RED level gates the RDO or RDZ data bit through into DA2.

Input data from the discfile is loaded into DA2 as it is read in serial fashion, one bit at a time, and is then shifted right until a full 18-bit data character is stored in DA2-19. At the conclusion of this loading process, the discfile control sends a Take a Character pulse to the Data Control 136,

causing the data control to strobe the character into its low order accumulator bits, and (if the character is the first of the two 18-bit characters making up the 36-bit data word) to shift it left to make room for the second character.

Although the Take a Character pulse is produced only during the execution of read commands, the RED level is not used to enable the generation of Take a Character. Instead of the RED level, the CM0(0) command-pair function (which is logically equivalent to  $\text{NOP} \vee \text{RED}$ ) is used for this purpose. The same CM0(0) level enables END(1) to set the WCT7 flip-flop during read commands only. The use of CM0(0) for these purposes rather than RED is, however, of no logical significance. Because the CM0(0) level is ANDed with SCS(1) (which can never be asserted during NOP), the resulting enable function is the exact logical equivalent of the RED level. (The CM0(0) level is used instead of the RED level only to ~~simplify wiring~~ *reduce signal propagation time*, and not from any logical necessity.)

There are certain other operations of the discfile control that are common to both the read command and the read compare command. These operations are enabled by the CM1(1) command-pair function rather than by the RED level. (See CM0-1 above for a more detailed description of this command-pair function and the logical operations which it governs.)

Generated by:

CM0(0)  $\wedge$  CM1(1)

(82) SCE - Sector End (-FC:B7)

Eighth and final state of the file-control octoflop. The ESP 1 pulse advances the octoflop from SCS state to SCE state at the end of each sector. The octoflop remains in SCE state for 2  $\mu$ sec. At the end of that interval, the octoflop is either reset to IDS state or returns to CMS state.

Although the SCE state lasts only for 2  $\mu$ sec, the SEF flag saves SCE for sampling. The SCE(1) level enables the ESP 2 pulse to set SEF, which then remains set until being reset by an SCL pulse.

It is not permissible to change the command code in CM0-1 after the ALP has advanced the octoflop from DFR to ALS state. For this reason, the SCS(0) level is used as a necessary input condition for the generation of the CCM level.

Generated by:

ESP 1.

The discfile control senses the end of each sector of data by means of an integrating 5- $\mu$ sec delay. When no DCK 1 clock pulses have been sensed for 5  $\mu$ sec, this delay times out, providing the ESP 1 pulse and, 2  $\mu$ sec later, the ESP 2 pulse. The octoflop is advanced from SCS state to SCE state by ESP 1. The ESP 2 pulse then performs one of two alternate functions. If there is no command code present in CM0-1 (NOP), no further operations are required, and the ESP 2 pulse resets the octoflop to IDS state. However, if a command code is present ( $\sim$ NOP), additional

sectors of data are to be operated upon. The ESP 2 pulse then sends another READ or WRITE pulse to the discfile, and simultaneously returns the octoflop from SCE state to CMS state.

(83) SCL - Status Clear (-SC:C6)

The SCL pulse clears the nine error-status flags: ADE, CME, DCE, DRL, FER, PER, RCE, SEF, and WLE.

Generated by:

IBR  $\checkmark$ .

PTA  $\checkmark$ .

PTC  $\wedge$  IOB10(1)

An SCL pulse is generated by IBR when computer power is first turned on, when the IO reset key is operated, and when a programmed reset is executed. This ensures that the discfile control begins operations with the error-status flags cleared. Whenever a DATAO 270 instruction is used to send a new address to the discfile control, a PTA pulse is produced and the PTA in turn produces an SCL pulse to clear the discfile control.

The SCL pulse can also be controlled by the program. A CONO 270 instruction with bit 28 in the 1 state produces an SCL pulse at PTC time. (The IOB10 input corresponds to bit 28 of the CONO instruction word.) This permits the programmer to clear the error-status flags (usually after printing out the error status and executing other appropriate steps to service the error-induced interrupt).

(84) SCS - Sector Started (-FC:B6)

Seventh state of the file-control octoflop. After the octoflop has been in CMS state for 200  $\mu$ sec, the NDP 1 pulse steps it to SCS state. The octoflop remains in SCS state until reaching the end of the sector; at that point the ESP 1 pulse advances the octoflop to its final SCE state.

Throughout the SCS state, the SCS(1) level enables each DCK 1 clock pulse to restart the 5- $\mu$ sec integrating delay AB01. This delay permits the discfile control to sense the end of each sector of data. When no DCK 1 pulses have been applied to the delay for 5  $\mu$ sec, the delay times out, producing the ESP 1 and ESP 2 pulses that mark the end of sector.

The SCS(1) level is applied to the input gating of BSC3. Since BSC3 has a weight of two in the bit-shift counter, setting it at the start of a count reduces the actual final count of the bit-shift counter by two. Although the counter always overflows when its contents are 20, if BSC3 is set before counting is begun only 18 counts are required to reach the overflow count of 20. For address transmission, SCS(1) is not asserted, BSC3 is not set, and the full 20 count is required to produce the overflow signal, BCO. However, for operations upon data (both output and input), SCS(1) is asserted, and therefore BSC3 is set at the end of each character. This ensures that the bit count of the following character starts at two so that overflow occurs at the DCK 1 clock corresponding to the eighteenth and final bit of each 18-bit character.

During read and read-compare commands SCS(1) causes RDS to be asserted, thereby enabling the data clock chain. Each incoming data bit



from the discfile then produces the following sequence of clock pulses:  
DCK 1, DCK 0, DCK 2, DCK 2.1, and DCK 3.

During the read command (data input from discfile to processor via Data Control 136), SCS(1) permits the application of a Take a Character pulse to the Data Control 136. The Take a Character pulse is sent to the Data Control at the same DCK 1 pulse that initiates the BCO. The Take a Character pulse causes the data control to strobe the 18-bit character into its low order accumulator bits, and (if required) to shift the accumulator left to make room for the second 18-bit character of the 36-bit data word.

The SCS(1) level also performs a second function during read commands. It permits the END(1) level to set the WCT7 flip-flop, thereby terminating the RDS level and turning off the clock. This permits terminating the read command at any point (even within a sector of data, or for that matter within a word within a sector).

During the output commands, write and read compare, assertion of SCS(1) causes the DCK 2.1 pulse that immediately follows the next BCO to initiate an SND pulse and a DTC pulse. The SND pulse gates an 18-bit output word from the Data Control 136 into the data accumulator of the discfile control. The DTC pulse sends the Data Control 136 a Give a Character pulse to shift the next output word into position for transfer into the discfile control.

It is not permissible to change the command code in CM0-1 after the ALP has advanced the octoflop from DFR to ALS state. For this reason, the SCS(0) level is used as a necessary input condition for the generation of the CCM level.

If an ERROR signal arrives from the discfile while the octoflop is in SCS state, the DCE flip-flop is set, indicating that the error is a data clock error. (See DCE above.) The CONI 270 samples SCS on IOB24.

Generated by:

NDP 1

An NDP 1 pulse is almost invariably produced 200  $\mu$ sec after the octoflop is stepped to CMS state. (In the unlikely event that an IOB reset pulse should occur during the 200- $\mu$ sec interval, no NDP 1 pulse would be generated. Instead of being advanced from CMS to SCS state, the octoflop would then be reset from CMS to IDS state.)

(85) SDR - Shift Data Right (-AD:B8 and -AC:C1)

The SDR pulse shifts the contents of DA2-18 one bit-position to the right. If ACE(1) is asserted, indicating that address transmission is in progress, the contents of DA19 are ring-shifted back into DA0. Since DA0-19 is directly accessible to the processor by means of the DATAI 270 instruction, this ring-shift feature permits a convenient check on the operation of the data accumulator shift logic. If ACE(0) is asserted, indicating that the current operation is a data operation, rather than address transmission, the contents of DA19 are not ring-shifted back into DA0; instead, at each SDR, a 0 is loaded into DA0.

Generated by:

DCK 2  $\wedge$  COH(0)

An SDR pulse is generated at the DCK 2 pulse initiated by each address and data bit with the exception of the address and data parity bits. Because of the heavy load which SDR drives, it is generated by two independent pulse amplifiers with identical input conditions.

(86) SEF - Sector End Flag (-SC:A7)

This flag is set 2  $\mu$ sec after the ~~file status~~ <sup>file-control</sup> octoflop is advanced to SCE state. The SEF remains set until being reset by an SCL pulse. The primary purpose of SEF is to save the SCE state for sampling. Even though SCE is no longer asserted, a 1 in SEF lets the programmer know that the end of the data sector has been passed. The CONI 270 samples SEF on IOB25.

Set by:

ESP 2  $\wedge$  SCE(1)

Reset by:

SCL

The SCE state of the octoflop lasts only for the 2- $\mu$ sec interval between ESP 1 and ESP 2; the SEF flag is set just as the octoflop is stepped out of SCE state. The SEF remains set until being reset by an SCL pulse. The SCL pulse that resets SEF can be produced in three ways: 1) by an IOB reset; 2) by the PTA pulse that accompanies a new DATAO 270 command; and 3) as a deliberately programmed SCL: the CONO 270 instruction produces an SCL at PTC time provided that bit 28 is coded to contain a 1.

(87) SEL - Select Discfile Control 270 (-SC:D2)

During the CONO instruction, this level gates the IOB CONO CLR and IOB CONO SET pulses from the processor to produce the CCB and PTC pulses. These two pulses clear the command buffer and set it to the new configuration specified by the CONO. For the CONI instruction, the SEL level allows the IOB STATUS pulse from the processor to produce the STP pulse; STP causes the processor to sample the status of various registers and flip-flops within the discfile control.

The SEL level also gates the processor signals sent to the discfile control during DATAO and DATAI instructions. For DATAO commands SEL is one of the conditions that must be present for the IOB DATA CLR and IOB DATA SET pulses to initiate CDA and PTA respectively. These two pulses clear the data accumulator, and transfer in a new address from IOB17-35. At a DATAI instruction, SEL allows IOB DATA I to initiate DTP. The DTP pulse then gates the contents of the data accumulator and the bit shift counter onto the IO bus.

Generated by:

Device selection code 270 applied to IOS3-9.

*Not selected*

(88)  $\bar{N}$ SEL 5 - ~~Select Device 5~~ (-SC:B7)

*If the  $\bar{N}$ SEL 5 level is asserted (at ground),*  
~~Unless the SEL 5 level is negatively asserted,~~ the data request late

flip-flop DRL is set by the NDP 2 pulse.

Generated by:

DC DEVICE SEL 5 (From Data Control.136)

When the internal device address in control-status register bits IC30-32 selects device 5 (the discfile control), the Data Control 136 sends a negative DC DEVICE SEL 5 level to the discfile control. If the Data Control 136 has not been selected to the discfile control, the DC DEVICE SEL 5 level is ground, thus asserting  $\bar{N}$  SEL 5 at ground.

(89) SELECT (-TR:A6)

The discfile control sends a SELECT pulse to the discfile through a twisted-pair transmission line to prepare the discfile to receive and store an address. The SELECT pulse connects the discfile to the discfile control and clears the discfile of previously induced error conditions.

Generated by:

PTA

The DATAO 270 instruction IOB DATA SET initiates the PTA pulse that generates SELECT. Neither the PTA pulse nor the SELECT pulse can be produced unless the file-control octoflop is in IDS state or ADT state. If a SELECT pulse is sent to the discfile during ADT state (after the ATP pulse, but before RDY), the SELECT causes a seek interrupt at the discfile. The seek interrupt automatically interrupts the seek operation being executed by the discfile. (This would occur if the programmer were to send an address to the discfile and then were to send another new address before the discfile had found the first address.)

The time required to execute a seek interrupt depends upon how far the interrupted seek operation has progressed. If the new SELECT arrives

before the positioner has been set in motion, the discfile can begin to operate upon the new address immediately, so there is no increase in the required access time. If, however, the new SELECT pulse is received after the positioner has already been set in motion, there is an added delay before the new address can be operated upon. This delay is required to ensure that power is not removed from the positioner while it is in motion; its duration is dependent upon the time that the discfile has spent operating upon the old address, but shall not exceed a nominal 250 ms.

(90) SNA - Select New Address (-FC:B2)

Second state of the file-control octoflop. During this state, the address of the "get-ready" sector preceding the next data sector to be operated upon is transmitted to the discfile. A total of 21 bits are sent to the discfile. This includes 19 address bits, the read-next-sector bit, and a parity bit which permits the discfile to verify the accuracy of the address transmission. The SNA state is a necessary condition for the generation of the ATP pulse. The SNA(1) level also provides an input to the PAR flip-flop complement logic. When SNA(1) is asserted, the PAR flip-flop is complemented whenever DA19 contains a 1 at the time of the SDR pulse. In this way, the PAR flip-flop generates the address parity bit. The CONI 270 samples SNA on IOB19.

Generated by:

PTA plus 15- $\mu$ sec delay ^ .

IDS v ADT

The PTA pulse starts a 15- $\mu$ sec delay. The termination of this delay steps the octoflop from IDS or ADT state to SNA state and simultaneously generates an ADS pulse. (See ADS above.) Usually the DATAO 270 instruction that produces PTA is given during the IDS state of the octoflop. However, the programmer has the option of changing addresses at any time during ADT state.

After completion of the address transmission, an ATP pulse is sent to the discfile, and the octoflop advances from SNA to ADT state. If there is no command code stored in CM0-1, the octoflop then oscillates between ADT state and DFR state (it is held in DFR state during only one millisecond of each 52-millisecond disc-revolution). The programmer can change addresses whenever the octoflop is in ADT state or in IDS state, but not during DFR state.

(91) SND - Sample New Data (-AD:C8)

The SND pulse causes the contents of the 18 high order bits of the Data Control 136 data accumulator to be loaded into bits DA2-19 of the discfile control data accumulator.

Generated by:

DTC

The DTC pulse always produces both an SND pulse and a GIVE A CHARACTER pulse. During the two output commands, write and read compare, the DTC pulse is generated at the CSP pulse that precedes the beginning of each data sector, and at the DCK 2.1 pulse corresponding to

the 18th and final data bit of each data character throughout the 128-word sector. A programmed DTC can also be given at will from the processor. This DTC is generated at the IOB CONO SET time of any CONO 270 instruction that has a 1 in bit 19. (See DTC above for a more detailed description of the function and generating conditions of DTC, SND, and GIVE A CHARACTER.)

(92) STP - Status to Processor (-CM:C8)

This 2.5- $\mu$ sec level gates the contents of the command buffer, the file-control octoflop, the nine error-status flags, and the relay-meter test switches onto the IO bus. The processor reads in this information from the bus at the 2- $\mu$ sec point.

Generated by:

IOB STATUS  $\wedge$  SEL

The processor CONI instruction produces a 2.5- $\mu$ sec negative IOB STATUS level. This command level is effective at the discfile control only when SEL is asserted, i. e. only when the CONI instruction device selection code is 270 octal.

(93) TAKE A CHARACTER (-SC:C7)

The TAKE A CHARACTER PULSE is sent to the Data Control 136 accumulator shift logic. The TAKE A CHARACTER PULSE signals the data control that the discfile control has presented an 18-bit input character to the low order strobe data inputs of the data control data accumulator. This indicates to the data control that it may strobe the



character into the low order bits of the data control data accumulator and that unless the character is the last (second) character in the input data word, it should begin to shift the contents of its accumulator left by 18 bit-positions to make room for the next character to be read in. If the character is the last character of the input data word, the TAKE A CHARACTER pulse causes the data control to strobe the character into the low order accumulator bits and then to advance the entire 36-bit data word from its data accumulator DA into its data buffer DB.

Generated by:

DCK 1  $\wedge$  CM0(0)  $\wedge$  SCS(1)  $\wedge$  END(0)  $\wedge$   
BSC0(1)  $\wedge$  BSC3(1)  $\wedge$  BSC4(1) .  $\vee$  :  
PTC  $\wedge$  IOB2(1)

The CM0(0) command-pair function is asserted both for NOP and for the read command. However, CM0(0) and SCS(1) are asserted together only during the read command. If the END flip-flop is set, no further input characters may be strobed into the data control.

The DCK 1 pulse that generates the TAKE A CHARACTER pulse is initiated by the final data bit of each 18-bit data character. Note that the BSC enabling conditions represent a count of only 19; the 19 count is used rather than the usual overflow count of 20 because the TAKE A CHARACTER is generated early in the DCK chain; it is generated at the DCK 1 pulse, the same DCK pulse that increments the bit-shift counter.

The last line of the generating conditions listed above represents a programmed TAKE A CHARACTER pulse that can be given at will from

the processor. This TAKE A CHARACTER is generated at the IOB CONO SET time of any CONO 270 instruction that has a 1 in bit 20. (The IOB2 input corresponds to bit 20 of the CONO instruction word.)

(94) WCE - Write Clock Even (-TR:D7)

Address transmission to the discfile is synchronized to WCE pulses generated within the discfile control. (See CLK above.) Write operations, however, are synchronized to WCE and WCO pulses initiated by WRITE CLOCK EVEN and WRITE CLOCK ODD pulses generated at the discfile. These WRITE CLOCK pulses are transmitted from the discfile over two twisted-pair transmission lines to the discfile control. (See WRITE CLOCK EVEN below.)

Depending upon whether the address bit (during address transmission) or the data bit (during write operations) corresponding to a given WCE pulse is a 1 or a 0, the WCE pulse produces an EDO or an EDZ pulse. These pulses in turn are returned to the discfile over twisted pairs, and there clock in the address (data and parity) or cause the writing of 1s or 0s (data and parity) as the case may be.

During address transmission, the WCE pulse starts the DCK clock chain, producing in sequence the following pulses: DCK 1, DCK 0, DCK 2, DCK 2.1, and DCK 3. For write operations, the WCE also starts the DCK clock chain (but only provided that the WCT counter has not yet reached its final count of 128).

Generated by:

CLK  $\wedge$  ACS(1)  $\vee$  :

WRITE CLOCK EVEN

The first condition specified above governs the generation of WCE pulses during address transmission. See CLK and ACS above.) The discfile control tracks furnish both WRITE CLOCK EVEN and WRITE CLOCK ODD pulses during the execution of write commands.

(95) WCO - Write Clock Odd (-TR:C6)

Write operations are synchronized to WCE and WCO pulses initiated by WRITE CLOCK EVEN and WRITE CLOCK ODD pulses generated at the discfile. These WRITE CLOCK pulses are transmitted from the discfile over two twisted-pair transmission lines to the discfile control. (See WRITE CLOCK EVEN below.)

the discfile control. Depending upon whether the data bit (or parity bit) corresponding to a given write clock odd is a 1 or a 0, the WCO pulses produce ODO or ODZ pulses; these pulses are returned to the discfile over twisted pairs and there cause the writing of 1s or 0s respectively.

Provided that the current command is a write command, and that the WCT counter has not yet reached its final count of 128, each write clock (even or odd) starts the DCK clock chain, resulting in the generation of DCK 1, DCK 0, DCK 2, DCK 2.1, and DCK 3.

Generated by:

Discfile control tracks

(See WCE above.)

(96) WCT - Word Counter (-WC:A3-7)

The word counter's function is to count the number of 37-bit data words that have been processed, and to end the current command when the count reaches 128 or, in the case of the read command only, when the END flip-flop is set. The only output from the word counter is the WCT7(0) level; this level is asserted so long as the contents of the word counter are less than 128. The WCT7(0) level must be asserted in order for RDS to be asserted. Neither the odd write clock pulses WCO nor the even write clock pulses WCE can initiate the DCK clock chain unless WCT7(0) is asserted.

Cleared by:

FCL

Incremented by:

DCK 2  $\wedge$  BCO  $\wedge$  WDC(1)

WCT7 Set by (Adds 128 to WCT Contents):

DCK 1  $\wedge$  CM0(0)  $\wedge$  SCS(1)  $\wedge$  END(1)

The FCL provides an initial clear; it clears the WCT before each new address is transferred out and at the beginning of each new data sector. The WCT is incremented once at the end of the address transmission. This is a "don't care" condition, since an FCL pulse clears out the 1 count at the beginning of the first data sector to be processed.

Throughout all data operations (read, write, read compare commands) the WCT is incremented at the 36th bit of each 37-bit data word (the final data bit before the parity bit). No incrementing occurs at the BCO corresponding to the final bit of the first character of each data word; this is because WDC(1) is asserted only during alternate (even-numbered) data characters. (See WDC below.)

The CM0(0) command-pair function is asserted both for NOP and for the read command. However, CM)(0) and SCS(1) are asserted together only during the read command. The read command can be terminated at any point by setting the END flip-flop. (This can easily be done by giving a CONO 270 instruction with a 1 in bit 23.) When END is set to 1, the first DCK 1 pulse to appear sets WCT7, and thereby ends the RDS level and turns off the DCK clock. With RDS no longer asserted, neither RDO nor RDZ pulses can be generated. The turn-off of the DCK clock initiates the remaining operations required to end the read command and reset the

system. Five  $\mu$ sec after the last DCK 1 pulse, the integrating delay AB01 times out, producing an ESP 1 pulse. That ESP 1 pulse clears the command register CM0-1, and 2  $\mu$ sec later the ESP 2 pulse resets the octoflop to IDS state. The discfile control is then ready to receive a new command.

The read command differs from the output commands (write and read compare) in that it can be terminated in mid-sector. The output commands must always proceed to the end of the current 128-word sector even though the END flip-flop is set prior to the end of the sector. This is true even if the output data from the discfile is exhausted before the sector ends. If no further output data is available, 0's are written (or compared) for the rest of the 128-word sector.

(97) WDC - Word Control Flip-flop (-AD:C7)

The WDC flip-flop must be in the 1 state in order for the COH flip-flop to be set. The WDC flip-flop must also be in the 1 state for the WCT counter to be incremented.

Set by:

ADS

Reset by:

FCL

Complemented by:

DCK 2  $\wedge$  BCO

The FCL provides an initial clear; it clears WDC before each new address is transferred out and at the beginning of each new data sector. The

ADS pulse that initiates the turn-on of the address clock sets WDC at the beginning of address transmission. The WDC flip-flop remains in the 1 state throughout the address transmission. The BCO level is asserted at the DCK 1 pulse corresponding to the 20th bit of the address (the last address bit before the parity bit). The single DCK 2 pulse that occurs while BCO is asserted sets the COH flip-flop and complements the WDC flip-flop (resetting it to the 0 state). The COH(1) level remains until the next DCK 2 pulse; it thus identifies the following address bit (the 21st and final bit of the address) as the address parity bit.

Throughout the data operations (the read, write, and read compare commands) the WDC flip-flop acts as a count-of-two counter. The FCL pulse ensures that the WDC flip-flop starts the data sector in the 0 state. The DCK 2 pulse then complements WDC at the BCO corresponding to the final data bit of each of the 18-bit data characters making up the sector. Provided that the WDC flip-flop already contains 1, the same DCK 2 pulse that complements the WDC flip-flop also sets the COH flip-flop to the 1 state and increments the WCT counter. As a result, only the DCK 2 pulse initiated by the 36th data bit of each data word sets the COH flip-flop and increments the WCT counter. The COH(1) level remains until the next DCK 2 pulse; it thus identifies the following data bit (the 37th and final bit of the current data word) as the data word parity bit. The WCT counter is incremented only at the even-numbered 18-bit data characters. This allows the use of the WCT to count the number of 37-bit data words that have been processed during the current sector.

(98) WLE - Write Lock Error Flip-flop (-SC:A3)

When this flip-flop is set, it indicates that a locked out disc has been addressed. The CONI 270 samples the contents of WLE on IOB28.

Set by:

WRITE LOCKOUT WARNING (from discfile)

Reset by:

SCL

Each discfile unit contains a panel of 16 lockout switches; each of these switches corresponds to one of the 16 data discs in the discfile. When a given switch is operated, it becomes impossible to write upon or erase the corresponding disc. The data on the locked out disc is preserved for reading only. The usefulness of this data-protection safeguard is augmented by the fact that the lockout switch panel is located behind a door which can be locked.

Should the processor address a locked out disc for either reading or writing, the discfile sends a WRITE LOCKOUT WARNING to the discfile control. This pulse arrives at the discfile control with or before the READY pulse and immediately sets both the FER flip-flop and the WLE flip-flop. Provided that the priority interrupt enable switch EFE (a flip-flop switch) is set to 1, FER(1) produces a PIE level. The resulting priority interrupt request can be used to warn the programmer that he has addressed a locked out disc.

If the command is a read or read compare, there is no difficulty in reading the data from the locked out discs, and no further error indications



result. However, if the discfile control should attempt to execute a write command in spite of the WRITE LOCKOUT WARNING, then the writing or erasure of data is prevented and a data check error is generated. The data check error produces a DC error indication at the discfile, and also sends an ERROR SIGNAL to the discfile control. At the discfile control, the ERROR SIGNAL sets the FER flip-flop and also the ~~DC~~<sup>CME</sup> flip-flop.

(99) WRITE (-TR:A8)

The discfile control sends a WRITE pulse to the discfile through a twisted-pair transmission line to command the discfile to write out a sector of data. If an additional WRITE signal is sent during the 8- $\mu$ sec guard-slot after the final data pulse of the sector, then the discfile increments its stored address by 1 and writes another sector.

Generated by:

CSP  $\wedge$  WRT .  $\vee$ :

ESP 2  $\wedge$  WRT

During every write command, a WRITE pulse is sent to the discfile at the CSP pulse that precedes the beginning of the first sector of the command. If the command code is still in the command register CM0-1 after the ESP 1 pulse marking the end of a given sector (indicating that the command is to continue to write additional sectors), then the closely following ESP 2 pulse sends another WRITE pulse to the discfile. This process can continue throughout the 44 sequentially addressed sectors at a given disc position before any sector is written upon a second time. To

prevent inadvertent destruction of data, it is important that the programmer keep count of the number of records sequentially written at a single position. In order to write a file containing more than 44 sectors, the programmer should give additional DATAO 270 instructions that change the disc and/or position fields.

→ Insert page 112b here

(100) WRITE LOCKOUT WARNING (-SC:B1)

The discfile sends a WRITE LOCKOUT WARNING to the discfile control through a twisted-pair transmission line to indicate that the processor has addressed a locked out disc. This pulse arrives at the discfile control with or before the READY pulse and immediately sets both the FER flip-flop and the WLE flip-flop. (See WLE above.)

(101) WRT - Write Command (-CM:A1)

This level indicates that the contents of CM0-1 specify the write command. The WRT level enables both the CSP pulse and the ESP 2 pulse to transmit WRITE pulses to the discfile. The CSP pulse initiates the first WRITE pulse of a write command. If the command is to write more than one sector of output data, the ESP 2 pulse that follows the end of each sector sends the discfile another WRITE. Each WRITE pulse after the first increments the discfile address. Up to 44 successive sectors can be written at a single position without destroying any data previously written.

There are certain other operations of the discfile control that are common to both the write command and the read compare command.

(99A) WRITE CLOCK EVEN (-TR:D5)

The discfile control tracks furnish both WRITE CLOCK EVEN pulses and WRITE CLOCK ODD pulses during the execution of write commands. Within the discfile control these pulses are inverted and redesignated WCE and WCO. Note that during address transmission WCE pulses are also generated within the discfile control. (See WCE above.) One of the four control tracks on the top baffle disc of the discfile generates clock pulses for inner zone writing; a second control track generates control pulses for outer zone writing. The write clock frequency depends upon whether the addressed sector (at which the writing is to be done) is located in the inner or outer zone. The control track for the outer zone contains <sup>approximately 35,000</sup> ~~34,840~~ bits; the control track for the inner zone contains only <sup>about 21,000</sup> ~~20,904~~ bits; both tracks are recorded with a one-bit maximum anomaly at the splice point.

Write clock pulses from both control tracks are sent to the discfile control on two twisted pairs (odd and even). The first, third, and succeeding odd pulses are transmitted on the odd twisted pair; the even pulses are transmitted on the even pair. Since the nominal period for a single disc revolution is 52 ms, the interval between successive clock pulses is about <sup>1.4</sup> ~~1.5~~  $\mu$ sec for the outer-zone control track, and about <sup>2.4</sup> ~~2.5~~  $\mu$ sec for the inner-zone control track. The intervals between successive even write clocks (or successive odd write clocks) are twice the intervals stated.

(99B) WRITE CLOCK ODD (-TR:D5)

See WRITE CLOCK EVEN above.

These operations are enabled by the CM0(1) command-pair function rather than by the WRT level. (See CM0-1 above for a more detailed description of this command-pair function and the logical operations which it governs.)

Generated by:

CM0(1)  $\wedge$  CM1(0)

## CHAPTER 9

### ENGINEERING DRAWINGS

This chapter contains reduced copies of engineering logic diagrams, flow diagrams, circuit schematics, and other engineering drawings necessary for understanding and maintaining the Discfile Control 270. Only those drawings which are essential and are not available in the pertinent reference documents are included. For a list of all drawings in this manual refer to the table of contents.

A complete set of engineering drawings is supplied with the equipment. Should any discrepancy exist between the drawings in this chapter and those supplied, the assumption is that the latter drawings are correct.

#### 9.1 DRAWING NUMBERS

Engineering drawing numbers contain five pieces of information, separated by hyphens. This information consists of a 2-letter code specifying the type of drawing; a 1-letter code specifying the size of the drawing; and variable-length codes specifying the type number of the equipment, the manufacturing series of the equipment, and a serial number for the drawing. The drawing type codes are:

BS, block schematic or logic diagram

CD, cable diagram

CS, circuit schematic

FD, flow diagram

ID, interconnection drawing  
PW, power wiring  
RS, replacement schematic  
SD, system diagram  
TD, timing diagram  
TFD, timing and flow diagram  
UML, utilization module list  
WD, wiring diagram

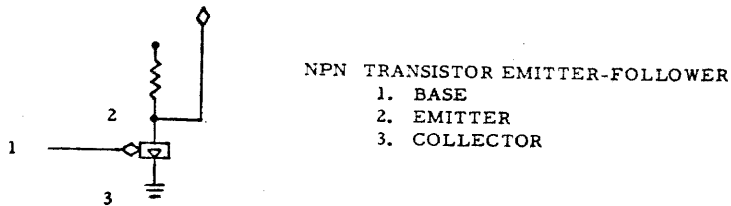
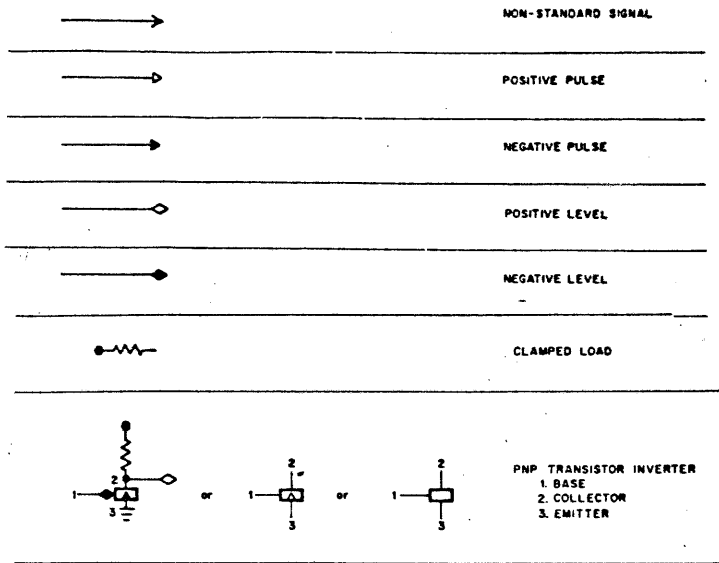
## 9.2 CIRCUIT SYMBOLS

The block schematics of Digital equipment are multipurpose drawings that combine signal flow, logical function, circuit type and location, wiring, and other pertinent information. Individual circuits are shown in block or semiblock form, using special symbols that define the circuit operation. These symbols are similar to those in the Digital System Modules Catalog and the FLIP CHIP Modules Catalog but are often simplified. Figure 9-1 illustrates most of the symbols used in Digital engineering drawings.

## 9.3 LOGIC SIGNAL SYMBOLS

A Digital logic signal symbol is shown at the input of almost all circuit symbols to specify the logic conditions that must be asserted to produce the output shown. These logic signal symbols are summarized in Figure 9-1.

All logic signals are either standard Digital logic levels or standard Digital pulses. A standard Digital logic level is either a ground (0 to -0.3v)



CAPACITOR-DIODE GATE, POSITIVE OR NEGATIVE INDICATED BY POLARITY OF THE INPUTS

1. PULSE INPUT
2. CONDITIONING LEVEL INPUT
3. PULSE OUTPUT

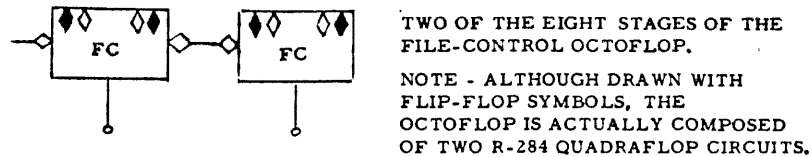
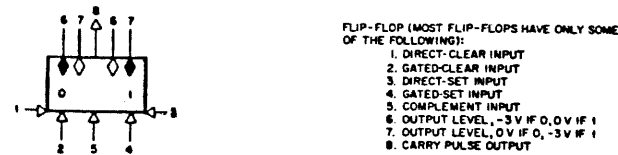
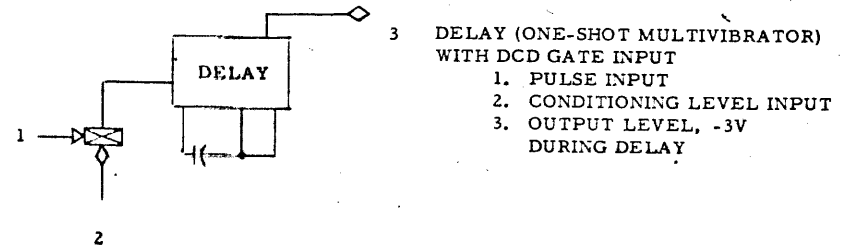
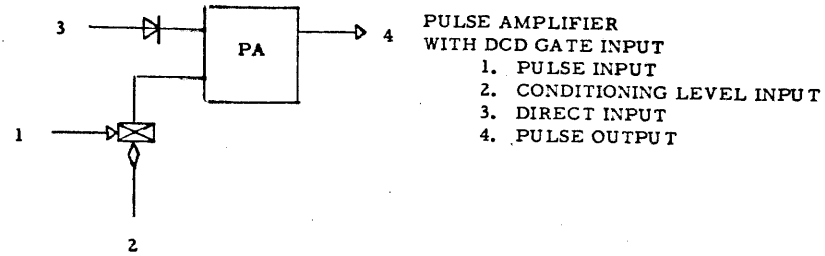


FIGURE 9-1 DEC LOGIC SYMBOLS

or -3v (-2.5 to -3.5v). Logic signals are generally given mnemonic names (e.g. RED, WRT, END) which indicate the condition represented by assertion of the signal. An open diamond ( —◇ ) indicates that the signal is a level and that ground represents assertion; a solid diamond ( —◊ ) indicates that the signal is a level and that -3v represents assertion.

The standard Digital negative pulse is indicated by a solid triangle ( —▶ ) and goes from ground to -3v. The standard Digital positive pulse, indicated by an open triangle ( —▷ ) goes from -3v to ground. The width of the standard pulses used in this equipment is either 70, 100, 400 nsec or 1.0 μsec, depending on the module and application.

#### 9.4 COÖRDINATE SYSTEM

Each engineering logic diagram is divided into 32 zones (4 horizontal, and 8 vertical) by marginal map coordinates. Figure references in the text are usually followed by a letter and a digit specifying the zone in which the referenced circuit is located.

Example:

Figure -FC:B4

|     |  
|     + - - - - - zone B4  
|

+ - - - - - in Figure BS-D-270-FC

(To avoid needless repetition of the full drawing number most in-text references include only the difference modifier portion of the number.)



## 9.5 MODULE IDENTIFICATION

Two numbers appear in or near each circuit symbol or inside the dotted line surrounding multiple circuit symbols. The upper number designates the module type and is usually composed of a letter followed by three digits. Standard modules are identified by this number in the FLIP CHIP Modules Catalog. Nonstandard FLIP CHIP modules are prefixed by the letter G. The only nonstandard module included in the Discfile Control 270 is the G980 pulse amplifier. A circuit schematic of the G980 pulse amplifier is included in this chapter.

The lower number is the module location code. This number consists of a letter followed by two digits. The letter identifies the two-row mounting panel and row within the panel and the number identifies the module location within the row. The mounting panels are lettered alphabetically with panel A-B in the upper location. Within each row, the modules are numbered consecutively 1 to 32 from left to right.

Module connector terminals are identified by letters next to the circuit symbol. To identify any particular terminal, the terminal letter is added to the module location as a suffix. These letters run in alphabetical order, with the letters G, I, O and Q omitted. See Figure 9-2 for examples.

### Example:

Figure 9-2 is a portion of engineering logic diagram BS-D-270-0-FC repeated here to illustrate Digital symbols and nomenclature.

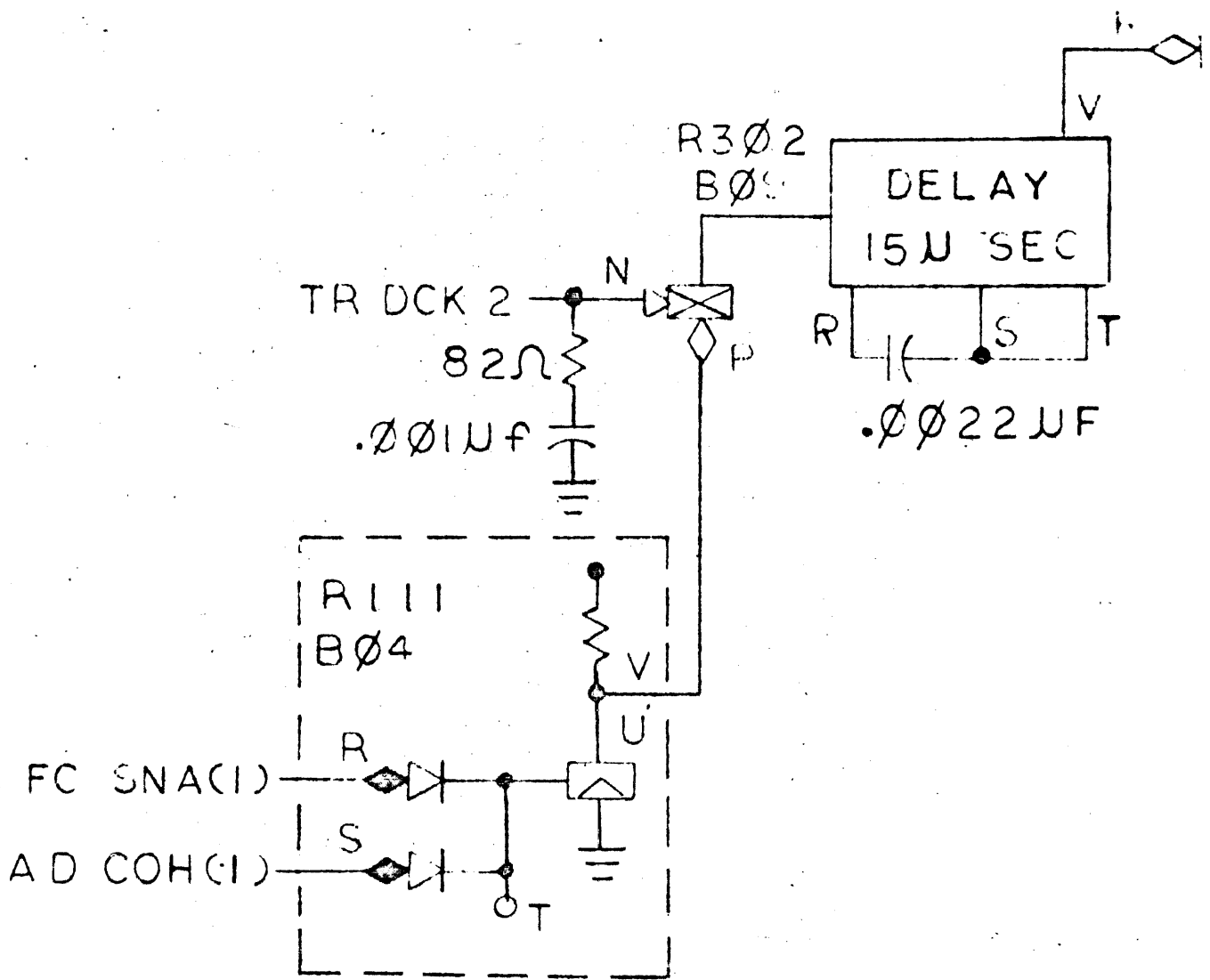


Figure 9-2

Typical DEC Engineering Logic Diagram

Portions of two separate modules are shown. (To determine what other circuits may also be contained in these two modules, consult the utilization module list drawing UML-D-270-0-11-sheet 1.) Both modules are located in Row B, the second row of modules in the top (A-B) mounting panel of the cabinet. The R302 one-shot delay is located in position B09 (ninth module from the left end of the row). The R111 diode gate is located in position B04 (fourth module from the left end of the row).

The two inputs to diode gate B04 are FC SNA(1) and AD COH(1). The two-letter prefixes FC and AD indicate that these signals originate on engineering logic diagrams BS-D-270-0-FC and BS-D-270-0-AD, respectively. As shown by the solid diamond, the SNA(1) level is asserted negative (-3 vdc) whenever the SNA flip-flop contains 1. Similarly, the COH(1) level is asserted at -3 vdc whenever the COH flip-flop contains 1.

If both the SNA(1) and the COH(1) input levels are asserted negative, then the R111 diode gate generates a ground-assertion output level. This level (shown by a hollow diamond) is applied to terminal P of the DCD gate at the input of the delay B09. When the level is asserted (ground), it enables the DCD gate to trigger the delay at the arrival of a positive DCK 2 pulse (shown by a hollow triangle). As indicated by the TR prefix, the TR DCK 2 pulse originates on engineering logic diagram BS-D-270-0-TR.

The output of the R302 delay is normally at ground. When the delay is triggered, the output drops from ground to -3 vdc, and remains at that negative level for the duration of the delay. When the delay period terminates, the output level returns to ground. (As shown in Figure 9-2, the

delay is calibrated to 15  $\mu$ sec, but its duration can be varied by adjusting a potentiometer or changing the capacitor.)

**digital**EQUIPMENT  
CORPORATION  
MAYNARD, MASSACHUSETTS**MASTER DRAWING LIST**

CODE	DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
BS	D-270-0-AC	A	1	ADDRESS SHIFT COUNTER & CLOCK
BS	D-270-0-AD	B	1	ADDRESS HOLD & DATA ACCUMULATOR
BS	D-270-0-CM	B	1	COMMAND & CONTROL
BS	D-270-0-FC	B	1	FILE CONTROL
BS	D-270-0-SC	A	1	STATUS & CONTROL
BS	D-270-0-TR	B	1	TRANSMITTERS & RECEIVERS
BS	D-270-0-WC	A	1	WORD COUNTER
FPL	D-270-0-17		1	FRONT PANEL LAYOUT
CP	D-270-0-19		3	270 DISC FILE CHECKOUT PROCEDURE
FD	D-270-0-FD	A	3	FLOW DIAGRAM
FD	D-270-0-8		1	CONTROL STATES
<b>ISSUED</b>				
UML	D-270-0-11	B	2	UTILIZATION MODULE LIST <b>APR 14 1966</b>
WL	B-270-0-10	B	1	DISC FILE CONTROL WIRING LIST
PW	D-270-0-18		1	ACDC POWER WIRING
WD	D-270-0-13	B	1	BUS SCHEDULE FOR 270 CONTROL
ID	A-270-0-14		7	270 CABLING COMPONENTS
CL	A-270-0-15	A	2	COMPONENTS LIST
LAD	C-270-0-9		1	RELAY TEST SWITCH PLATE
MD	B-270-0-16		1	DISC FILE NAME PLATE
MD	C-270-0-6		1	MASTER CLEAR SWITCH PLATE
SP	A-270-0-20		6	SYSTEM ACCEPTANCE TEST & PROCEDURE

REV.	ECO	ENG	DATE	MADE BY	CHECKER	ENG	
A	166	S.A.L.	7/29/65	C. LaCorti	<i>[Signature]</i>		
B	232	S.A.L.	11/22/65				
C	255	AAV	2/17/66				
				TITLE	270 CONTROL		
				FOR	THIS SCHEMATIC IS FURNISHED ONLY FOR TEST & MAINTAINANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE & SHOULD BE TREATED ACCORDINGLY.		
				SHEET	OF 1	CODE	DWG. NO.
				MDL			A-270-0
						REV LET	C

A-270-0-14

CODE

ID

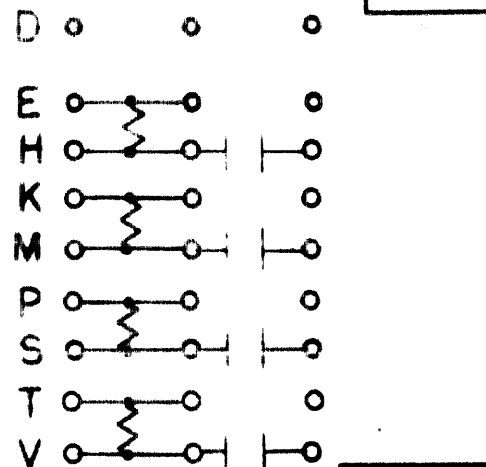
W028

ELCO

D	
H	D4
H	E5
K	D14
M	E15
P	E1
S	D2
T	E11
V	D12

270  
E31

W028

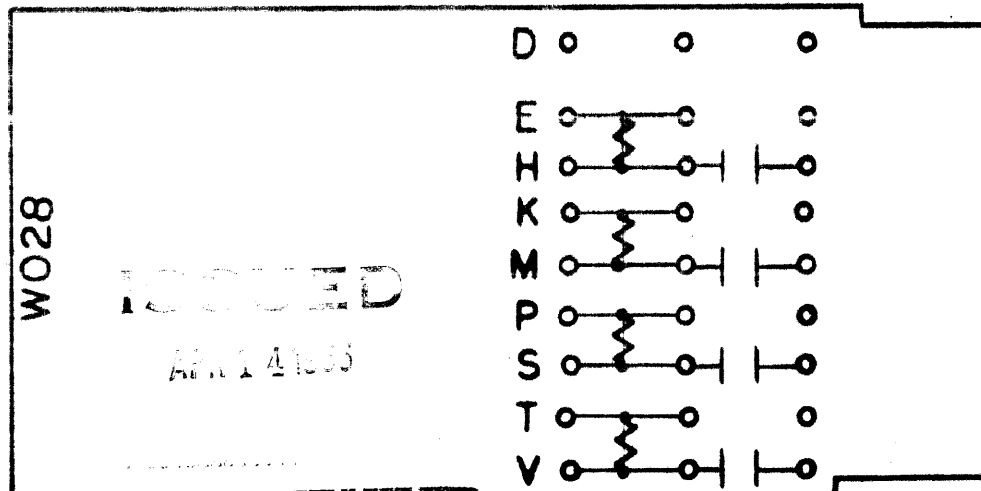


CABLE TO DISCFILE MODEL 5022

D	
E	F2
H	F4
K	F6
M	F8
P	F10
S	F12
T	H2
V	H4

270  
E32

W028



Elco Connector #00-8017-100-000-012  
Resistors are 100 OHM 1/4w  
Capacitors are .001uf

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CODE

ID

SHEET 1 OF 7

270 CABLING COMPONENTS

digital

A-270-0-14

Super.  
*[Handwritten signatures and notes]*

A-270-0-14

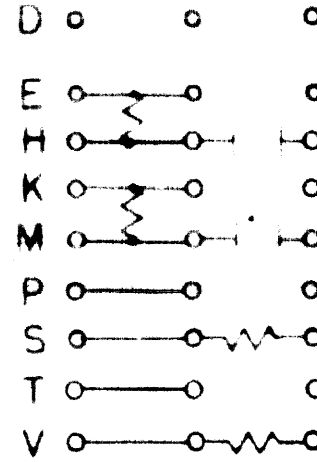
CODE

ID

W028	ELCO
D	
E	B4
H	B2
K	C1
M	C3
P	C5
S	C7
T	C9
V	C11

1111  
P30

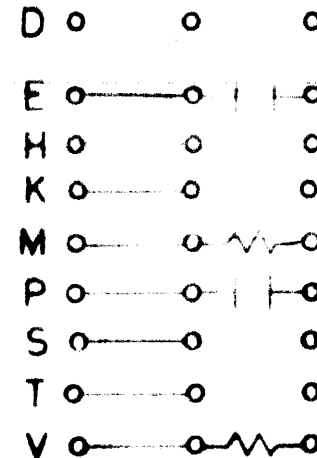
W028



CABLE TO DISCFIELD MODEL 5022

D	
E	L1
H	L3
K	M2
M	M4
P	S3
S	S1
T	U9
V	U11

W028



Elco Connector #00-8017-10  
 Resistors are 100 OHM 1/4w  
 Capacitors are .001uf

CODE

ID

SHEET 2 OF 7

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drawn  
*B. Simpson*  
 checked  
*A. M. [unclear]*  
 engineer

# 270 CABLING COMPONENTS

## digital

APR 14 1964

A-270-0-14

A 270-0-14

CODE

ID

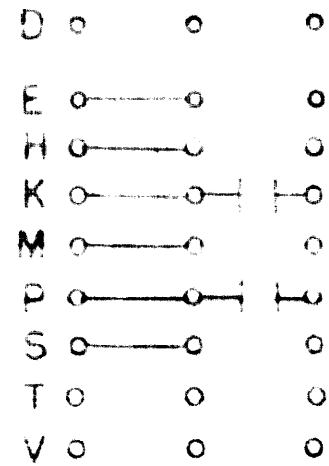
W028

ELCO

270  
232

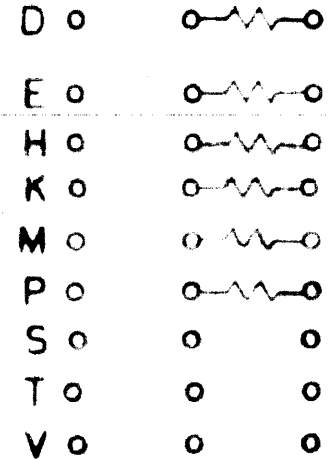
D	
E	17
H	17
K	01
M	02
P	03
S	14

W028



CABLE TO DISCIPLINE MODEL 2021

W028



TERMINATION  
CAPS

Elco Connector #00-6017-1  
 Resistors are 47 OHM 1/4W  
 Capacitors are .001uf

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 & MAINTENANCE PURPOSES. THE CIRCUITS ARE  
 PROPRIETARY AND SHOULD BE TREATED  
 ACCORDINGLY.

SHEET 3 OF 7

CODE

ID

Checked  
1/11/66

exper.  
 J. E. D.  
 1/11/66

drawn  
 B. J. ...  
 checked  
 M. J. ...  
 engineer

# 270 CABLING COMPONENTS

## digital

A-270-0-14



A-270 0 14

CODE

ID

W028

1032L

D	B
E	C
H	D
K	E
M	F
P	H
S	K
T	L
V	M
D	N
E	P
H	R
K	T
M	U
P	V
S	W
T	X
V	Y

E04  
E05  
E06  
E07  
E08  
E09  
E10  
E11

270

F01  
F02  
F07  
F08  
F09  
F10  
F11

W028

D ○ — ○ ○  
E ○ — ○ ○  
H ○ — ○ ○  
K ○ — ○ ○  
M ○ — ○ ○  
P ○ — ○ ○  
S ○ — ○ ○  
T ○ — ○ ○  
V ○ — ○ ○

JOB CABLE

W028

D ○ — ○ ○  
E ○ — ○ ○  
H ○ — ○ ○  
K ○ — ○ ○  
M ○ — ○ ○  
P ○ — ○ ○  
S ○ — ○ ○  
T ○ — ○ ○  
V ○ — ○ ○

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\* MAINTAINANCE PURPOSES. THE CIRCUITS ARE  
PROPRIETARY IN NATURE & SHOULD BE TREATED  
ACCORDINGLY.

CODE

ID

SHEET 4 OF 7

ISS

APR

Checked  
14  
Apr. 1963

ED  
Changes

excer.

production

other

drawn

B. Lumbino

checked

Apr 1963

engineer

# 270 CABLING COMPONENTS

## digital

A-270-0-14

A-270-0-14

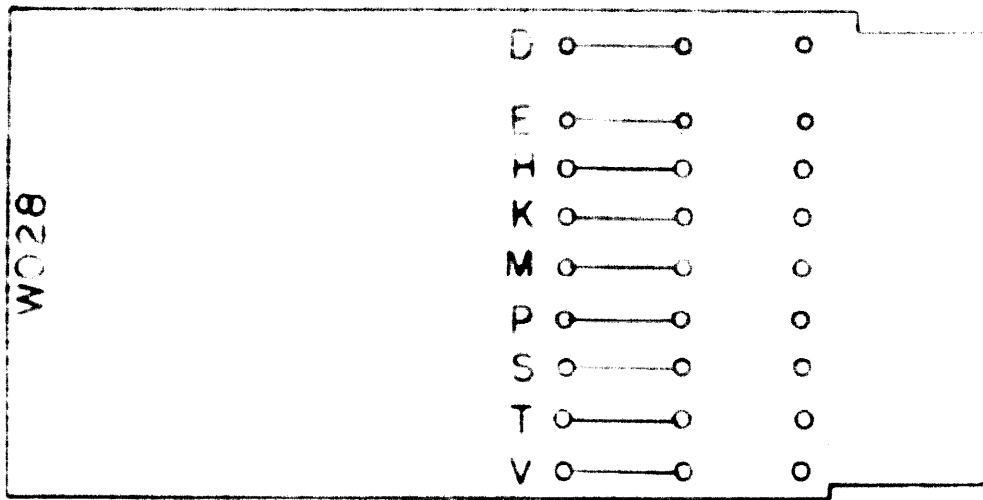
CODE

ID

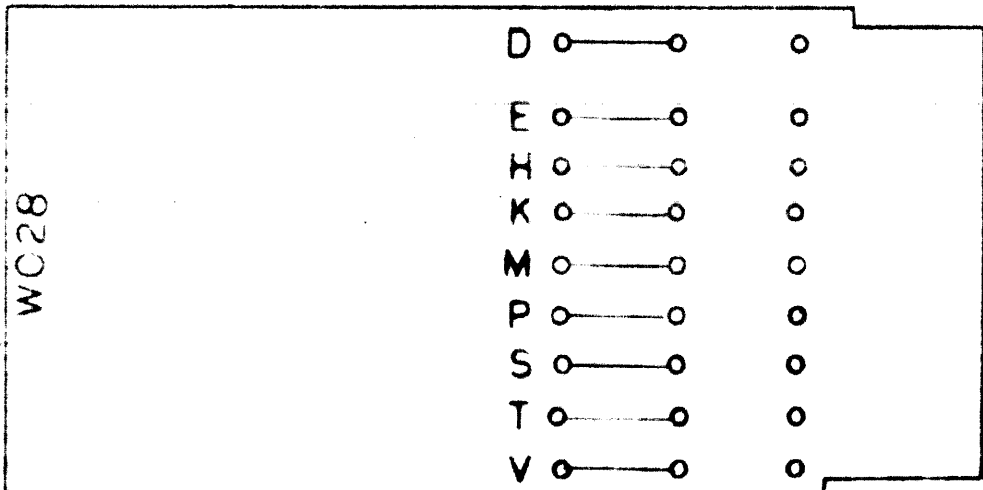
W028

1032A

D	B		
E	C	136	1018
H	D	1018	820
K	E		
M	F		
P	H		
S	K		
T	L		
V	M		
D	N		
E	P		
H	R		
K	T		
M	U		
P	V		
S	W		
T	X	136	1018
V	Y	1018	820



CABLE TO 136 DATA CONTROL



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ISSUED

SHEET 5 OF 7

CODE

ID

APR 14 1963

Changes

exper.  
production  
other

drawn  
*B. Simons*  
checked  
*M. H. ...*  
engineer

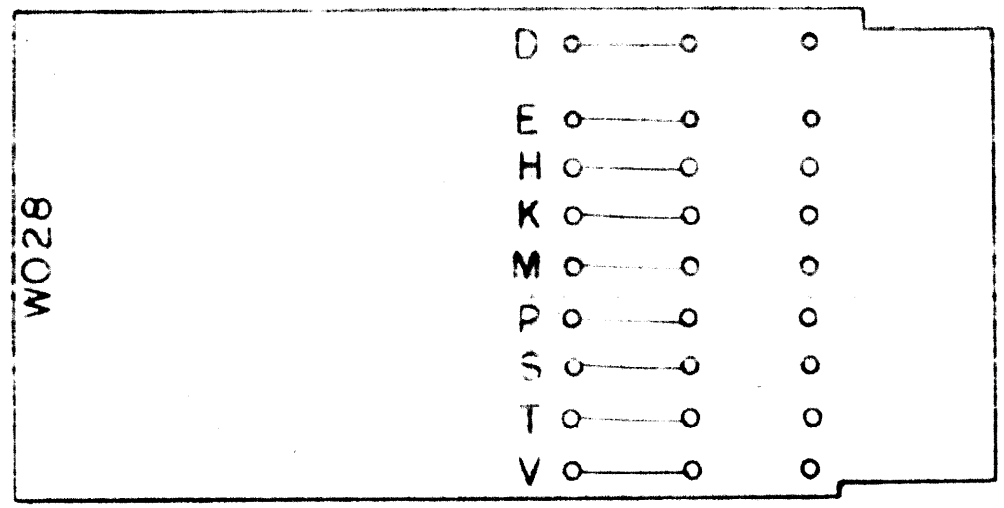
270 CABLING COMPONENTS

digital

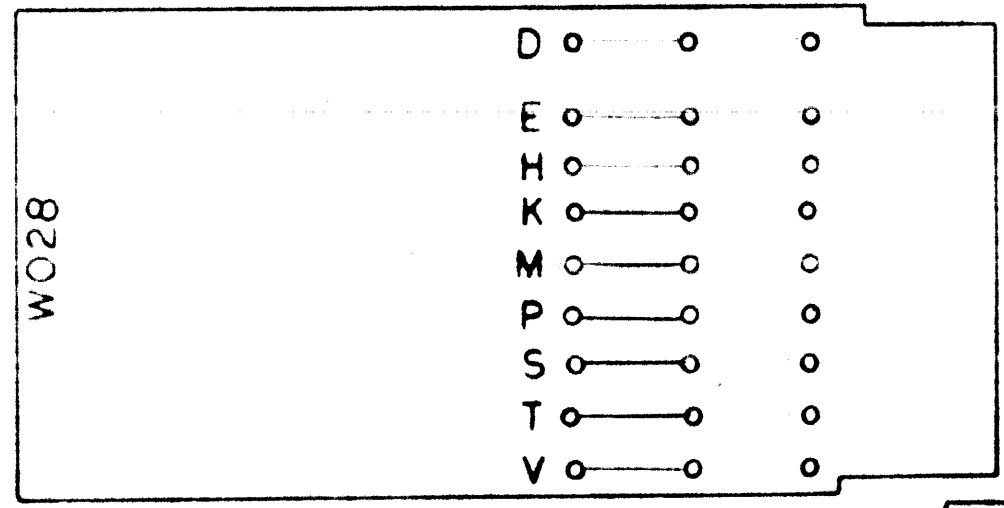
A-270-0-14

A-270-0-14

CODE  
ID



CABLE TO 136 DATA CONTROL



<u>W028</u>	<u>1032A</u>	<u>136</u>	<u>270</u>
D	B	1D17	E27
E	C		
H	D		
K	E		
M	F		
P	H		
S	K		
T	L		
V	M		
D	N		
E	P		
H	R		
K	T		
M	U		
P	V	136	270
S	W	1D17	E27
T	X		
V	Y		

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SHEET 6 OF 7  
CODE  
ID

ISSUED  
APR

Chg. app.  
Changes  
exper.  
production  
other

drawn  
*B. L. ...*  
checked  
*...*  
engineer

270 CABLING COMPONENTS  
digital  
A-270-0-14

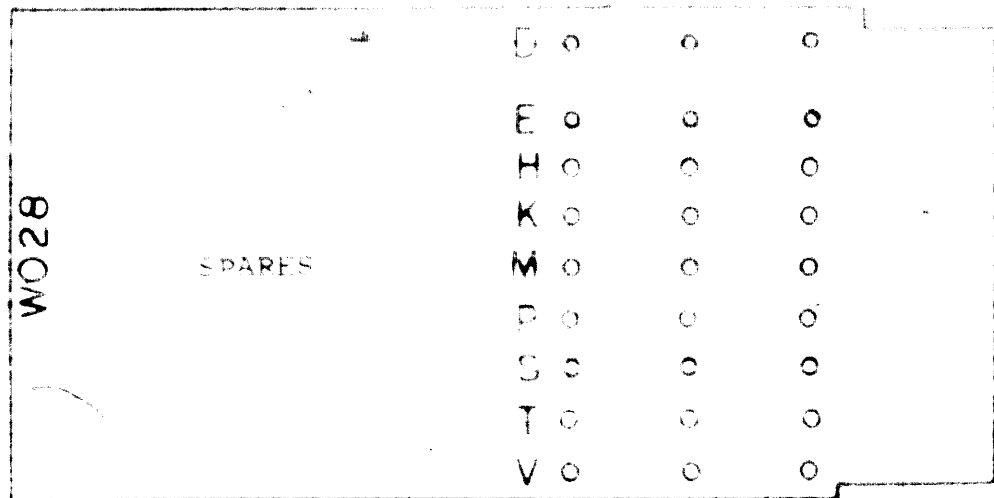
A-270-0-14

CODE

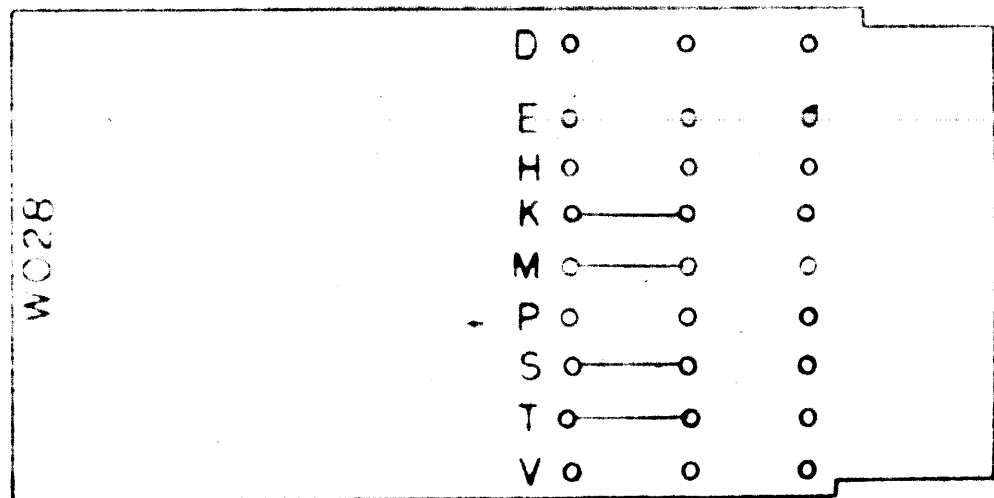
ID

W028 1032A

D	B	136	270
E	C	1D20	F28
H	D		
K	E		
M	F		
P	H		
S	K		
T	L		
V	M		
D	N		
E	P		
H	R		
K	T		
M	U		
P	V		
S	W	136	270
T	X	1D20	F28
V	Y		



CABLE TO 136 DATA CONTROL



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CODE

ID

SHEET 7 OF 7

APR 1 1961

sh. app. app.

Changes

exper. production other

drawn B. L. Simpson checked P. W. Johnson engineer

# 270 CABLING COMPONENTS

## digital

A-270-0-14

**DIGITAL EQUIPMENT CORPORATION**

MAYNARD, MASSACHUSETTS

**ENGINEERING SPECIFICATION**

DATE 11/22/65

TITLE 270 DISC FILE CHECKOUT PROCEDURE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
-	ORIGINATED BY ECO 232		S.A.L.	11/22/65	S.A.L.	11/22/65

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**ISSUED**

APR 14 1966

ENG Steve Lambert	APPD Steve Lambert	CODE CP	SIZE A	NUMBER 270-0-19	REV
----------------------	-----------------------	------------	-----------	--------------------	-----

TITLE 270 DISC FILE CHECKOUT PROCEDURE

EQUIPMENT REQUIRED: PDP-6-16K COMPUTER  
 136 DATA CONTROL  
 270 DISC FILE CONTROL  
 5022 DATA PRODUCTS DISC FILE

NOTE: Remove all modules before starting checkout.  
 Remove all logic voltages when setting up logic for checkout.

1. Inspect for all obvious errors, such as broken wires, components, and other things of that nature. Record all defects, and rework in log book provided for that purpose.
2. Connect up IO Buss cables and logic voltages.
3. Place all M.C. switches to down position and turn on logic voltages via the PDP-6. Check for +10A and -15V B on logic panels A to F.
4. Place +10V A M.C. switches up. Vary +10 M.C. on PDP-6 and observe similar variations on logic.
5. Place +10V A M.C. switches down and -15V B M.C. switches up. Vary -15 M.C. on PDP-6 and observe similar variation on all logic panels A to F.
6. Place -15 M.C. switches down and turn off logic voltages. Install all modules except delays and clock in their respective positions as designated on UML-D-270-0-11. The W300 delay should be installed at this time.
7. Using a bench setup, adjust the delays and clock as indicated on the Block schematics or flow diagram before installing them in the 270 logic system. This can be accomplished by using a low rep-rate clock at the input to the delays and a scope for observing the duration. Any external components wired on the logic must also be used on the bench setup. Install the delays and clock after they have been adjusted.
8. Turn on power to the PDP-6 and 270 logic. Read in Maindec program #670 (Magnetic Disc Test) and follow the instructions set forth in the program write-up. The first test used in the checkout of the 270 is called DISK DFST. During this test, error typeouts will give an indication as to which area of the logic is failing. The program will loop on the error so that a scope can be connected to the failing logic. When an error is found, be sure to turn power off before taking corrective action.

CODE CP	SIZE A	NUMBER 270-0-19	REV
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TITLE 270 DISC FILE CHECKOUT PROCEDURE

9. When an error condition has been corrected, turn power on and restart the DISK DFST program. If another error typeout appears, follow the procedure indicated in paragraph 8 and above until the DISK DFST program completes without any error typeouts.
10. The Magnetic Disc Test has many data transferring programs contained in one package. The first test to be tried after DISK DFST is to transfer\* to the Disk and back "all ones." Once this has been accomplished "all zeros" should be transferred. If both these conditions work, then the worst case condition of random numbers (DISK DRAND) should be tried. If DISK DRAND works it can be assumed that the 270 logic is fully checkout.
11. Once DISK DRAND works, the next step is to take margins on both +10V and -15V. These margins are to be entered on the data sheet provided with the 270 logic.

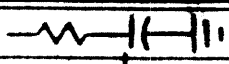

\*Transfer "All ones"

"All zeros"

START	3500/ JSR INT	3510/ JSR INT
	3501/ GEN ONES	3511/ GEN ZEROS
	3502/ DISKW 0	3512/ DISKW 0
	3503/ GEN ZEROS	3513/ GEN ONES
	3504/ DISKR 0	3514/ DISKR 0
	3505/ CHECK ONES	3515/ CHECK ZEROS
	3506/ JRST DDT	3516/ JRST DDT

CODE  
CPSIZE  
ANUMBER  
270-0-19

REV

CONNECTION MEDIA	POL	PIN	PIN	NAME
		C24R 82Ω RES TO	.001uf CAP TO GND	AC CLK
		D18S		AC SDR
		D17F		AD CDA
		C09T		AD DTP
		E22N		AD FCL
		E22P		AD SDR
		F 5K		CM CCB
		D25P		CM PTC
		E12T		CM STP
		C10K		
		B05R		
		F29P		FC ALP
		F20N		FC ESP 1
		D32E		FC SSP 2
		C21J		FC NDP 1
		E20N		FC NDP 2
		D17M		AD PTA
		F25P		SC IRR
		F25D		TR, DCK 1
		B09N 82Ω RES TO	.001uf CAP TO GND	TR DCK 2

DRAWN  
 Maureen Mariano 5/25/65  
 CHECKED  
 R. J. [Signature] 5-23-65  
 ENG  
 J. J. Lambert 5-28-65



EXTERNAL COMPONENTS LIST  
 TITLE  
 TYPE 270  
 COMPONENTS LIST

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**ISSUED**  
 APR 14 1965

DWG NO  
 A-270-0-13  
 SHEET 1 OF 2

REV. LTR.  
 A  
 CODE CL

SH-1  
 A-166  
 APPV  
 ECO. NO.  
 REV. LTR.





**DIGITAL EQUIPMENT CORPORATION**  
**MAYNARD, MASSACHUSETTS**

**ENGINEERING SPECIFICATION**

DATE 1/12/66

TITLE TYPE 270 DISC FILE SYSTEM ACCEPTANCE TEST AND PROCEDURE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

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**ISSUED**

APR 14 1966

ENG <i>S. A. Lambert</i>	APPD <i>R. Small</i>	CODE <i>66-107</i>	SIZE	NUMBER	REV
			A-270-0-20		

TITLE TYPE 270 DISC FILE SYSTEM ACCEPTANCE TEST AND PROCEDURE

PURPOSE OF TEST

The purpose of the test described herein is to assure that the performance of the system meets the criteria for acceptance set forth. The testing procedure includes individual component tests as well as complete system tests. When all conditions of the tests have been satisfied, Digital Equipment Corporation considers the system acceptable. Customer acceptance of the Type 270 Disc File System is to be based on the performance of the system as indicated by the test programs supplied by DEC personnel.

TESTS PERFORMED

DISK DFST (Disc File Status Test)

Individual tests are performed on all parts of the Type 270 System including the portion of the 136 Data Control connected to the Disk Control. Error typeouts will appear if any logic component fails. This test requires approximately 10 minutes run time.

DISK DADDR (Disc Address Test)

The Disc Address test is performed on every Disc in the following manner. Each position on the specified positioner is Written, Read and Checked. When all portions have been written, the program will re-read and check all the data on the positioner. The pattern used is such, that each word of a sector will contain the Disc, Position and Address of that sector. This test insures that all locations exist. There are 3072 address operations performed,  $2.1 \times 10^8$  bits\* written,  $4.3 \times 10^8$  bits \* read, during this test. The program requires 39 minutes operation time.

DISK DRAND (Random Disc Address)

This program selects at random a Disc Position, and sector whereupon, random numbers are Written, Read-Compared, Read and Checked for accuracy over one revolution or 44 sectors.  $1 \times 10^3$  operations are performed in random sequence.  $2.1 \times 10^8$  bits are written and  $4.2 \times 10^8$  bits are read. This test consumes 30 minutes of machine time.

\*Bits read or written include parity bits.

CODE 8F	SIZE A-270-0-20	NUMBER	REV
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TITLE TYPE 270 DISC FILE SYSTEM ACCEPTANCE TEST AND PROCEDURE

### DISK DFZO (Floating Zero/One Test)

This test is performed using a pattern of floating zeros and ones on alternate positions throughout the 16 Discs. A floating zero consists of a 36 bit word of all ones except one bit which is zero. This bit changes position on each successive word. A floating one is the complement of a floating zero. The program will Write, Read and Check all words at a single position. The position is then decremented and the procedure is repeated using the complement pattern. When all positions on a positioner have been written, the data is Read, Checked and the position is incremented. When checking is complete, the above process is repeated using the complement of the above pattern. The total number of operations executed is 1024. There are  $4.3 \times 10^8$  bits written and  $8.6 \times 10^8$  bits read during this test. Program run time is 1 hour 4 minutes.

### DISK DOXIDE (Surface Oxide Test)

This test is identical to the DISK DFZO test except the pattern is alternate ones and zeros 5252 etc, 2525 etc. The program run time is 1 hour. The bits transferred are the same as DFZO.

### Acceptance Program - Maindec(---):

The program is initiated by starting at address 3500. The sequence with run time and bits transferred is:

<u>Comment</u>	<u>Instruction</u>	<u>Run Time</u>	<u>Bits Read</u>	<u>Bits Written</u>
Start	JSR INT	None	None	None
	DISK DFST	10 min.	None	None
	DISK DADDR	39 min.	$4.3 \times 10^8$	$2.1 \times 10^8$
Repeat 10X	DISK DRAND	5 hrs.	$4.2 \times 10^9$	$2.1 \times 10^9$
Repeat 2X	DISK DFZO	2 hrs. 8 min.	$1.72 \times 10^9$	$8.6 \times 10^8$
	DISK DFZO	2 hrs. 8 min.	$1.72 \times 10^9$	$8.6 \times 10^8$
	DISK DOXIDE	2 hrs. 0 min.	$1.72 \times 10^9$	$8.6 \times 10^8$
	DISK DOXIDE	2 hrs. 0 min.	$1.72 \times 10^9$	$8.6 \times 10^8$
	TOTAL	14 hrs. 5 min.	$1.151 \times 10^{10}$	$5.75 \times 10^9$

$1.9 \times 10^4$  operations during test.

CODE AS7	SIZE A-270-0-20	NUMBER	REV
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TITLE TYPE 270 DISC FILE SYSTEM ACCEPTANCE TEST AND PROCEDURE

Equipment Life

The file has a design life of at least three (3) years before major overhaul is required, assuming that proper scheduled maintenance is performed.

Error Warranty

There should be no errors due to failure of the magnetic recording medium (bad spots) for the warrantable life of the equipment assuming that recommended maintenance procedures are followed. In addition, the equipment shall not exhibit any magnetic degradation with time of pre-written data sufficient to cause errors while reading.

Acceptance Error Rates

The following paragraphs define the acceptance error rates of the DISCFILE System.

Malfunction DefinitionsReading Error

A data error is detected and three repeated reading operations initiated under program control, are error-free.

Writing Error

A data error is detected as the result of a write check\* and three repeated writing operations, followed by write checks initiated under program control are error-free.

Incomplete Operation Error

A malfunction of the equipment occurs during which there are no data error. Under program control, the operation is repeated and is completed successfully.

Failure

A condition which causes errors or other malfunctions which can only be corrected by unscheduled maintenance.

Acceptance Test Error Rates

Following are the acceptance test criteria for the final acceptance test performed by Digital Equipment Corporation personnel:

Incomplete Operation Error Rate

Not more than 1 in  $2 \times 10^4$  operations.

\*The first operation of reading and checking data written on a previous revolution of the disc.

CODE	SIZE	NUMBER	REV
4-SP	A-270-0-20		

TITLE **TYPE 270 DISC FILE SYSTEM ACCEPTANCE TEST AND PROCEDURE**

Read Error Rate

Not more than 1 in  $2 \times 10^9$  data bits transferred.

Write Error Rate

Not more than 1 in  $10^{10}$  data bits transferred.

Failure Rate

Four maximum within 250 hours of cumulative file operation.

Storage Capacity

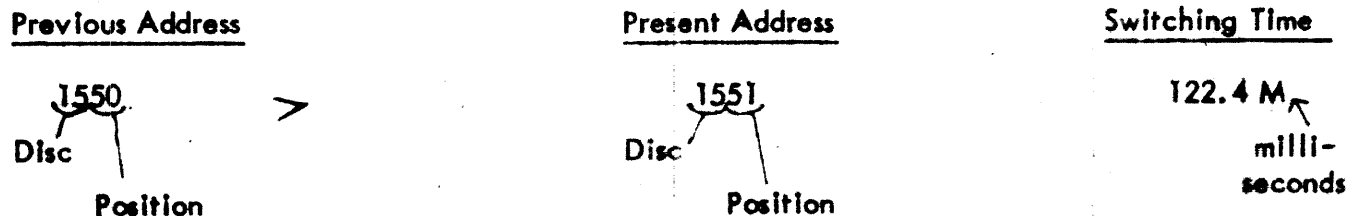
Words per sector		128
Sectors per position	x	44
Words per position		5,632
Bits per word (including parity)	x	37
Bits per position		208,384
Positions per Disc	x	64
Bits per Disc		13,336,576
Discs per file	x	16
Bits per file		213,385,216

Selection Time

The time to switch from one Disc and Position to another and receive a ready signal from the newly selected sector, should not exceed 351 milliseconds (worst case).

While the DISK DRAND test is operating, set bit 34 of the Console Data Switches to a one.

All selection times will be printed on the Type 646 Line Printer (if one is available) in the following format:



CODE A-270-0-20	SIZE A-270-0-20	NUMBER	REV
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TITLE TYPE 270 DISC FILE SYSTEM ACCEPTANCE TEST AND PROCEDURE

The acceptance test program must be run from beginning to end (14 hours 5 minutes consecutively) with no more than five Read or Read Check, one Write and one Incomplete Operation error typeout.

Signatures by a DEC Field Engineer and the Customer constitutes acceptance of the Type 270 Disc File System.

Signed \_\_\_\_\_  
DEC Field Engineer

Signed \_\_\_\_\_  
Customer

CODE BP	SIZE A-270-0-20	NUMBER	REV
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REVISED

REVISED

B-270-0-10


B

REVISIONS			
REV LTR	ECO NO	DATE	ENG
A	166	7-65	S.A.L.
B	232	11-22-65	S.A.L.

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST & MAINTAINANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE & SHOULD BE TREATED ACCORDINGLY.

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CHECKED BY	DATE		DISC FILE CONTROL WIRING LIST	
ENG	DATE		TAPE #	FILE #
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		ASSY NO	CODE	
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