PROGRAMMED DATA PROCESSOR-5

MAINTENANCE MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

COPY NO.

75047 PRINTED IN U.S.A. 10-10/64

PREFACE

This manual contains information for the planning and execution of all tasks involved in the installation, operation, and maintenance of the Programmed Data Processor-5, a core memory, stored program, parallel, digital computer designed and manufactured by the Digital Equipment Corporation. Information in this manual is prepared for engineers and technicians familiar with digital logic techniques and digital computer principles, and is not intended to teach basic theory. The manual does attempt to describe and explain the operation of the PDP-5 computer in detail. Every attempt has been made to organize this manual to allow rapid access of information required for a specific task. In an attempt to emphasize the importance of study and planning before the actual performance of a physical task, the first portion of this manual contains expository information, and the last portion contains task-oriented information and detailed procedures.

This manual is organized into the following sections:

Section 1, Introduction and Description - Information of a general nature which is applicable to the entire PDP-5 system is contained in this chapter. The chapter contains a detailed summary which describes the system as consisting of a processor, core memory, and input/output facilities. An understanding of this information is a prerequisite for reading the chapters containing detailed theory.

Section 2, Processor; Section 3, Core Memory; and Section 4, Input/Output - These chapters contain detailed theory of operation for the three major logic elements which constitute the PDP-5. The function of each circuit is explained and the generation of all control signals is described in detail with the aid of references to the block schematic engineering drawings.

Section 5, Logic Function - All operations involved in the performance of computing functions are described in detail in this chapter with the aid of the engineering flow diagram. Operations are described in detail with regard to accomplishing a specific task and are not encumbered by explanations of circuit operations as described in the previous chapters. This chapter tends to integrate the reader's understanding of the functions performed by the processor, core memory, and input/output logic elements.

Section 6, Interface - The technical characteristics of the interface circuits of the PDP-5 are defined and described in detail in this chapter to allow adequate design and installation planning of special peripheral equipment.

Section 7, Installation - Information is contained in this chapter to allow personnel to plan and implement the installation of a PDP-5 system.

Section 8, Operation - The function of controls and indicators of the computer and the standard Teletype unit are listed, and procedures are given to allow operation of this system. These procedures are written to allow interpretation and expansion required for the performance of specific tasks.

Section 9, Maintenance - Planning information and specific detailed procedures are contained in this chapter to allow personnel to perform thorough preventive maintenance and rapid logical corrective maintenance of the standard PDP-5.

Section 10, Pertinent Documents - Reference material in the form of a list of publications and copies of the engineering drawings are reproduced in this chapter as an aid to understanding the information contained in the manual.

CONTENTS

CONTENTS (continued)

CONTENTS (continued)

CONTENTS (continued)

CONTENTS (continued)

CONTENTS (continued)

CONTENTS (continued)

TABLES

TABLES (continued)

ILLUSTRATIONS

DRAWINGS

DRAWINGS (continued)

DRAWINGS (continued)

DRAWINGS (continued)

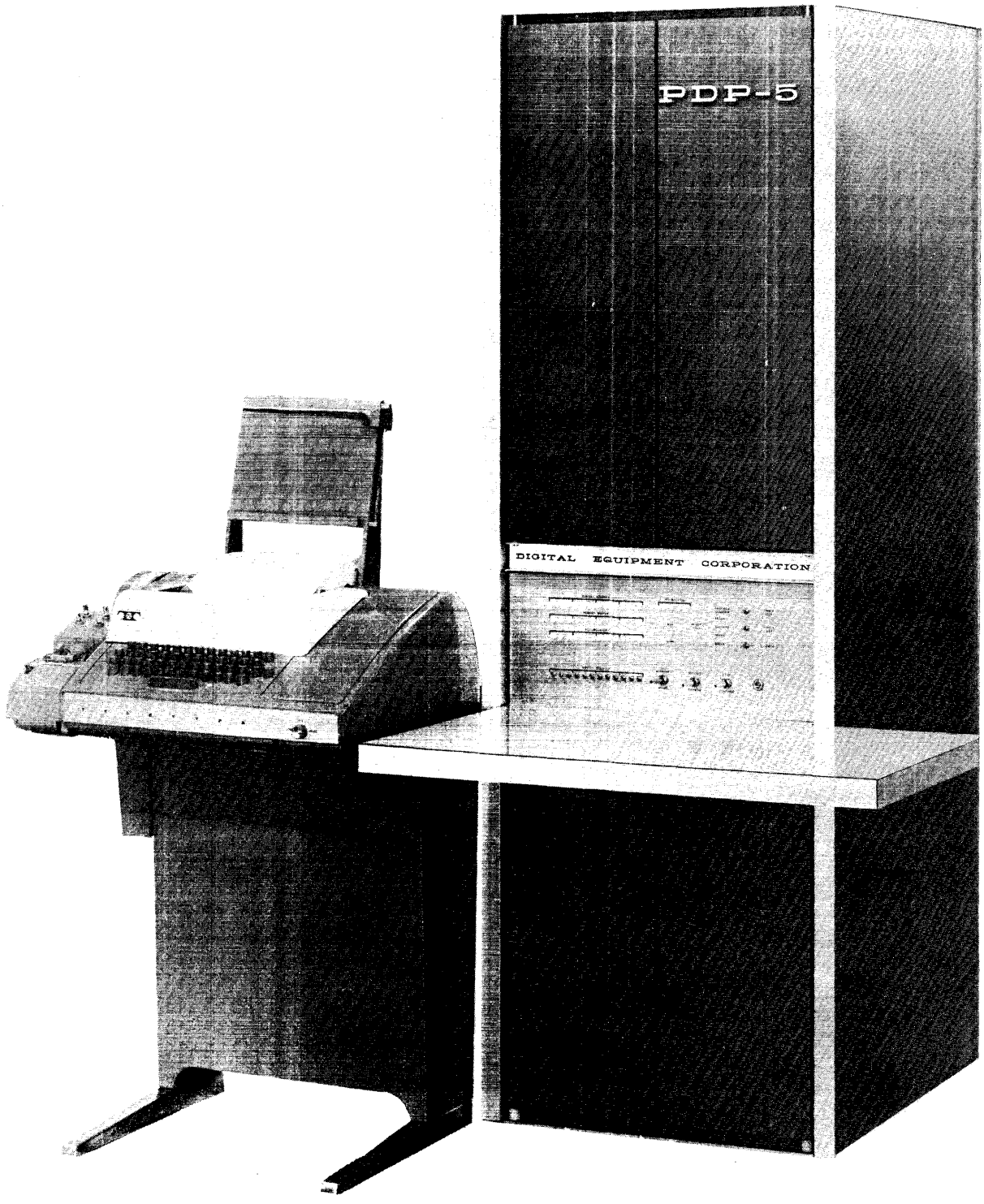


Figure 1-1 A Standard PDP-5 System

SECTION 1

INTRODUCTION AND DESCRIPTION

The Digital Equipment Corporation (DEC) Programmed Data Processor-5 (PDP-5) is a small, general-purpose, stored-program, digital computer that performs 2's complement binary arithmetic. The PDP-5 is a 1-address, 12-bit, parallel machine with a 6-microsecond cycle time. A standard PDP-5 contains a 1024- or 4096-word ferrite-core memory, which can be expanded in fields of 4096 words to a 32,768-word maximum by the addition of memory options. High-capacity, flexible, input/output circuits of the computer allow it to operate all types of modern peripheral data processing equipment and many types of process control instruments. Standard equipment for the PDP-5 includes a Teletype unit that provides an input to the computer from a keyboard or perforated tape and provides a page printer or perforated-tape output.

COMPUTER ORGANIZATION

The PDP-5 is a completely integrated system constructed of standard DEC system modules using transistor-diode switching circuits and self-contained solid-state power supplies. The computer operates on static dc levels, or the shift of them, and is organized into a data processor, a core memory, and facilities for input/output devices. The major functional elements of the PDP-5 and their signal interrelationship are shown in Figure 1-2.

Processor

All arithmetic, logic, and system control operations of the standard PDP-5 are performed by the processor. The major circuit elements which perform these functions are as follows:

Accumulator (AC) - The AC is the primary arithmetic register of the PDP-5. It also serves as an input/output register for programmed information transfers between core memory and peripheral equipment.

Link (L) - This 1-bit register serves as an extension of the AC and is used as a carry or overflow register for arithmetic operations.

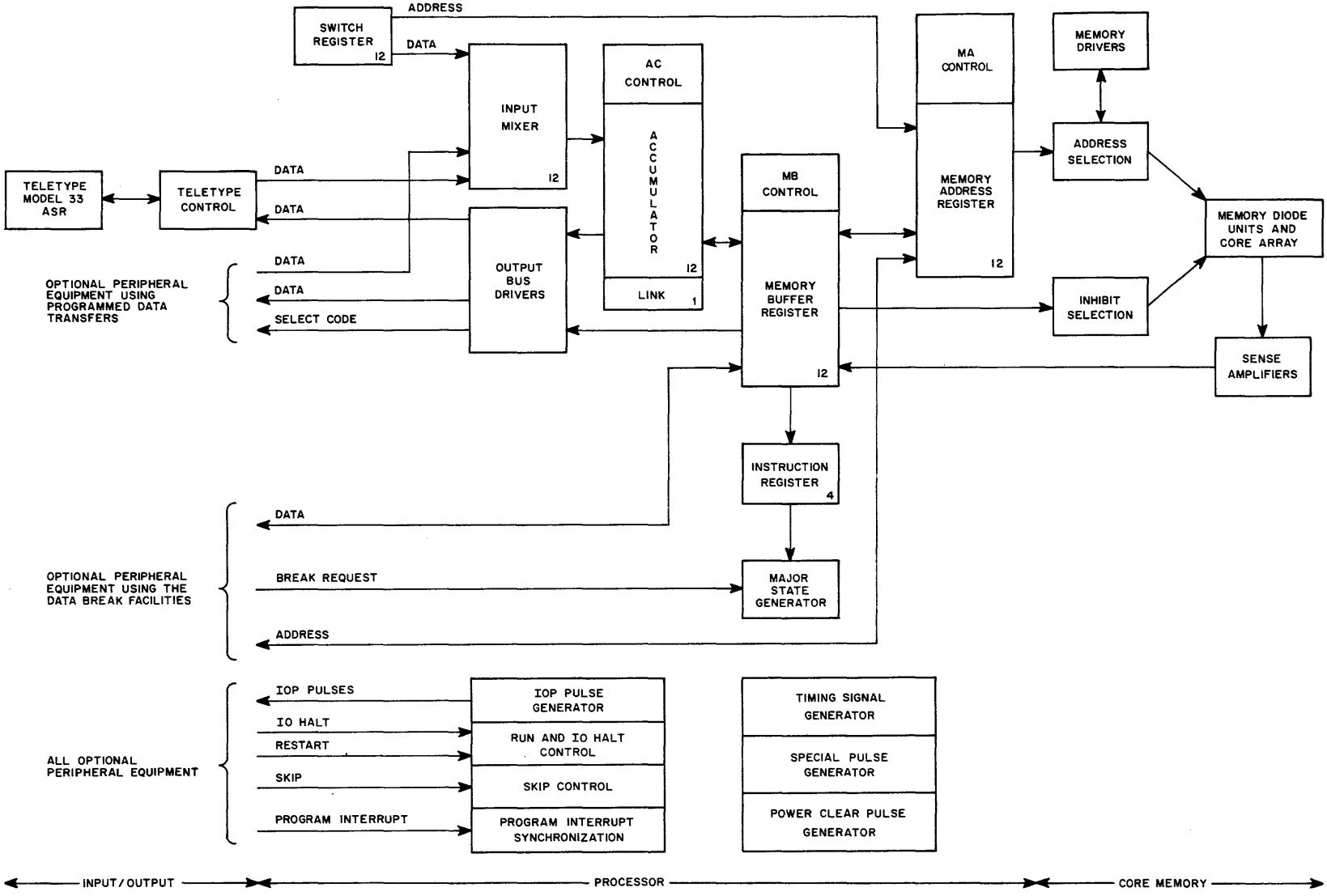


Figure 1-2 Simplified Block Diagram

Memory Buffer Register (MB) - The MB serves as a buffer register for all information passing between the processor and the core memory. The MB also serves as a buffer directly between core memory and peripheral equipment during data break information transfers and is used as a digital shift register for the Type 137 Analog-To-Digital Converter option.

Memory Address Register (MA) - The location in core memory which is selected for data storage or retrieval is determined by the MA. This 12-bit register can directly address all 4096 words of the standard core memory.

Instruction Register (IR) - This 4-bit register is loaded from the four most significant bits of the MB during a fetch cycle and so contains the four most significant bits of the instruction to be performed. The contents of the three most significant bits of the IR are decoded to produce the eight instruction performed by the computer. The least significant bit of the IR serves as a control bit to specify direct or indirect addressing of core memory to locate the operand during memory reference instructions, and is used to differentiate between the two groups of operate instructions.

Major State Generator - Two or more major control states are entered to determine and execute an instruction. The major state generator produces the signals which determine the machine state during each computer cycle. Each state is produced as a function of the current instruction, the current state, and the condition of the Break Request signal supplied to an input bus by peripheral equipment.

Program Counter (PC) - The address in core memory from which the next instruction will be drawn is controlled by the PC. The PC is located in address 0000 of core memory.

Input Mixer (IM) - The IM extends the input gating capability of the accumulator to allow it to handle information received from the switch register, the Teletype unit, and from peripheral equipment.

Switch Register (SR) - Twelve toggle switches on the operator console allow manual selection of addresses to be set into the MA and data to be written in core memory by passing through the IM, AC, and MB.

Output Bus Drivers - When necessary, output signals from the computer can be power amplified by removal of dummy plugs and insertion of output bus driver modules.

Basic Timing Generators - Timing pulses used to determine the 6-microsecond computer cycle time and produce time-synchronized gating operations are produced by the timing signal generator. Timing pulses used during operations resulting from use of the keys and switches on the operator console are produced by the special pulse generator. Pulses that reset registers and control circuits during power turn on and turn off operations are produced by the power clear pulse generator.

Control Elements - Circuits are also included in the PDP-5 that produce the IOP pulses that initiate operations involved in input/output transfers, determine the advance of the computer program under normal and I/O halt/restart conditions, allow instructions to be skipped as a function of the status of registers and control circuits within the computer or in peripheral equipment, and allow peripheral equipment to cause an interruption of the main computer program to transfer program control to a subroutine which performs some service for the I/O device. Other control elements generate the signals that control and activate the AC, MB, and MA.

Core Memory

Permanent (longer than one instruction time) local information storage and retrieval operations are performed by the core memory. The memory is continuously cycling, automatically performing a read and write operation during each computer cycle. Input and output address and data buffering for the core memory is performed by the MA and MB of the processor, and operation of the memory is under control of signals produced by the timing signal generator of the processor. The major functional elements of the core memory are as follows:

Memory Drivers - The direction of read-write drive current passing through the address drive lines of the core memory is determined by the memory drivers.

Address Selection - Addresses contained in the MA are decoded to enable passage of read-write current through an X and a Y drive line of the core memory.

Inhibit Selection - Data to be written in core memory is contained in the MB. Since the read-write current passing through the address selection lines produce binary ones in each bit of the addressed memory register, the inhibit selection circuits inhibit setting of cores in planes corresponding to bits of the MB containing zeros.

Memory Diode Units and Core Array - The ferrite core array consists of 12 planes that are 64 cores wide by 64 cores deep for a 4096-word memory. Memory diode unit modules connected directly to the array prevent read-write current from passing through unselected drive lines.

Sense Amplifiers - Signals induced on the sense windings of the core array during reading are detected by the sense amplifiers and converted to pulses that set corresponding bits of the MB to transfer information from a specific address in core memory to the MB.

Input/Output

Interface circuits for the processor allow bussed connections to a variety of peripheral equipment. Each input/output device is responsible for detecting its own select code and for providing any necessary input or output gating. Individually programmed data transfers between the processor and peripheral equipment take place through the accumulator. Single or multiple data transfers can be initiated by peripheral equipment, rather than by the program, by means of the data break facilities. Standard features of the PDP-5 also allow peripheral equipment to perform certain control functions such as program stop and start by means of the I/O halt and restart facilities, instruction skipping, and program control transfers initiated by a program interrupt.

Standard peripheral equipment provided with each PDP-5 system consists of a Teletype Model 33 Automatic Send Receive set and a Teletype control. The Teletype unit is a standard machine operating from serial 11-unit-code characters at a rate of ten characters per second. The Teletype provides a means of supplying data to the computer from perforated tape or by means of a keyboard, and supplies data as an output from the computer in the form of perforated tape or typed copy. The Teletype control serves as a serial-to-parallel converter for Teletype inputs to the computer and serves as a parallel-to-serial converter for computer output signals to the Teletype unit.

Facilities for the Type 137 Analog-To-Digital Converter are wired into each PDP-5. The converter operates by the successive approximation process, using the computer memory buffer register as a distributor shift register and using the accumulator as a digital buffer register. Conversion time for this option is a function of the predetermined accuracy, which varies

from 24.5 microseconds for 6-bit accuracy to 132 microseconds for 11-bit accuracy. The converter is able to use the registers of the computer because it stops the computer program by means of the I/O halt facility during its operation. Space and wiring within the processor are provided so that activation of this option requires little more than insertion of eight modules in a mounting panel.

Standard equipment, which can be obtained as peripheral equipment for the PDP-5 at the customer's option, includes high-speed perforated-tape readers and punches, card readers and punches, line printers and digital plotters, a variety of cathode-ray tube display equipment, a choice of magnetic tape equipment, Teletype data communication equipment, and multiplexer equipment which allows up to four I/O devices to use the computer data break facilities.

FUNCTIONAL DESCRIPTION

Operation of the computer is accomplished on a limited scale by keys on the operator console. Operation in this manner is limited to address and data storage by means of the switch register, core memory data examination, the normal start/stop/continue control, and the single step or single instruction operation that allows a program to be monitored visually as a maintenance operation. Most of these manually initiated operations are performed by executing an instruction in the same manner as by automatic programming, except that the gating is performed by special pulses rather than by the normal clock pulses. In automatic operation, instructions stored in core memory are loaded into the MB and executed during two or more computer cycles. Each instruction determines the major control states that must be entered for its execution. Each control state lasts for one 6-microsecond computer cycle and is divided into six 1-microsecond time states which can be used to perform logical operations. Performance of any function of the computer is controlled by gating of a specific instruction during a specific major control state and a specific time state.

Instructions

The three most significant bits of words brought from core memory which are to be used as instructions are loaded into the IR. The IR decodes the first three bits as the operation code to generate the eight instruction signals. Instructions that store or retrieve data from core memory are called memory reference instructions and are designated by operation codes 0 through

5. Instructions that do not reference core memory can be microprogrammed to cause a variety of operations to be performed as a function of binary ones in the remaining nine bits of the instruction. In a sense, these instructions use bits 3 through 11 to augment (or as an extension of) the operation code. Augmented instructions with an operation code of 6 perform input/output transfer (IOT) operations, and instructions with an operation code of 7 perform local data handling and control operations (OPR). Microprogramming of the IOT instruction allows combining of several bits to perform multiple operations within the limit of the capabilities of the peripheral equipment selected. Microprogramming of the operate instruction allows bit combinations and multifunction operations to be performed in two groups, as determined by the contents of bit 3 of the instruction. The format of all instruction classes is indicated in Figure 1-3.

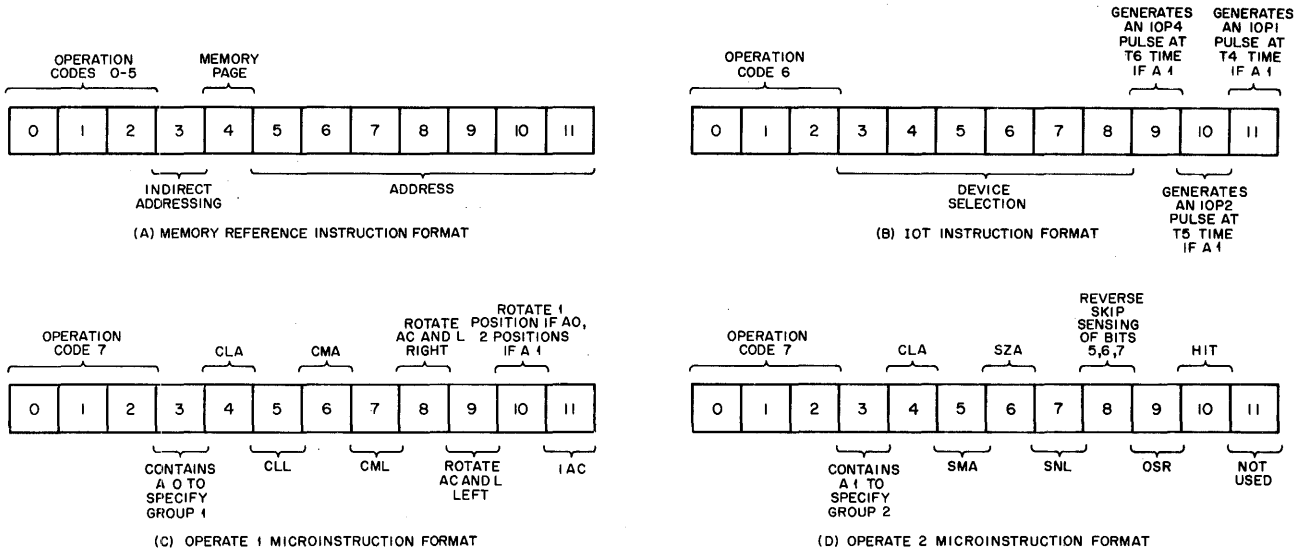


Figure 1-3 Instruction Formats

A memory reference instruction specifies a 12-bit core memory address for the operand in one of the following four ways:

a. When bits 3 and 4 of the instruction contain zeros, bits 0 through 4 of the address are zeros and bits 5 through 11 of the address are taken from the corresponding bits of the instruction.

b. When bit 3 contains a 0 and bit 4 contains a 1, bits 0 through 4 of the address are the same as the address of the current instruction and bits 5 through 11 are taken from corresponding bits of the instruction.

c. When bit 3 contains a 1 and bit 4 contains a 0, the address of the operand is taken from the content of the core memory register whose address contains zeros in bits 0 through 4 and corresponds to the content of the instruction for bits 5 through 11.

d. When both bits 3 and 4 contain ones, the address of the operand is taken from the content of the core memory register at an address corresponding to the address of the current instruction for bits 0 through 4 and corresponding to the content of the current instruction for bits 5 through 11.

The memory reference instructions are as follows:

AND (operation code 0) - The logical AND. This operation is performed between the content of the specified core memory register and the content of the accumulator. The result of this combination is left in the accumulator; the original content of the accumulator is lost, and the content of the addressed core memory register is restored.

TAD (operation code 1) - Twos complement add. The content of the specified core memory address is added to the content of the accumulator in 2's complement arithmetic. The result is left in the accumulator, the original content of the accumulator is lost, and the content of the addressed core memory register is restored. If there is a carry from AC_0 during this operation, the link is complemented.

ISZ (operation code 2) - Index and skip if zero. The content of the specified core memory register is incremented by one in 2's complement arithmetic and then restored. If the result of this incrementing is zero, the program counter is incremented an additional time so that the succeeding instruction is skipped.

DCA (operation code 3) - Deposit and clear accumulator. The content of the AC is deposited in the core memory location specified, and the content of the accumulator is cleared. The previous content of the specified core memory register is lost.

JMS (operation code 4) - Jump to subroutine. The content of the program counter is incremented by one and depositied at the specified core memory location. The next instruction is taken from the content of the specified core memory address +1.

JMP (operation code 5) - Jump. The core memory address specified in the instruction is set into the program counter so that the next instruction is taken from this specified core memory address. The original content of the program counter is lost.

An augmented instruction having an operation code of 6 is designated an input/output transfer (IOT) instruction and uses bits 3 through 8 to signify a select code for a specific I/O device or register, enabling it to produce IOT pulses during computer time states T4, T5, and T6 as a result of binary ones in bits 11, 10, and 9 respectively of the instruction. These IOT pulses initiate operation of logic elements within the peripheral equipment and/or execute data transfers to or from the processor.

Augmented instructions having an operation code of 7 specify the operate (OPR) instruction. When bit 3 of an OPR instruction contains a 0, a group 1 (OPR1) microinstruction is indicated; and when bit 3 contains a 1, a group 2 (OPR2) microinstruction is indicated. Group 1 microinstructions are used primarily for clearing, complementing, rotating, and incrementing operations, and group 2 microinstructions are used principally in test and skip operations. Any logical combination of bits within one group can be combined into one microinstruction. Naturally, bits which cause diverse functions cannot be programmed simultaneously.

Major States

Two or more states are entered during each instruction. Assuming that the core memory address of the next instruction to beperformed is contained in the MA, each instruction can be considered as beginning in the fetch state. The fetch state draws an instruction from core memory and begins executing it. At the conclusion of a fetch state other states are entered as a function of the current instruction. If no other states need be entered, the program count state is entered to load the content of the program counter into the MB, to modify the program count suitably, then to load the program count into the MA and the PC. At the conclusion of a program count state the fetch state is always entered. The operations performed in each of the major states are as follows:

Fetch (F) - During this state, instructions are brought from core memory and their operation code is transferred into the IR. The JMP, IOT, and OPR instructions are completely executed during the F state.

Execute 1 (E1) - The content of a core memory address specified by a memory reference instruction is loaded into the MB, and the instruction is executed during this state.

Execute 2 (E2) - This state is entered during a JMS instruction to write the program count into the core memory address specified by the instruction.

Defer (D) - The effective address of an indirectly addressed instruction is brought from core memory into the MB during this state.

Break (B) - This state is entered in response to a break request signal received from peripheral equipment and is used to execute data transfers directly between the MB and the device. Successive break cycles can be entered for multiple-word transfers. When the transfer has been completed, the normal program sequence is resumed.

Program Count (P) - This state is responsible for retrieving the program count from the PC at core memory address 0000 and modifying it according to the current instruction. Modification of the program count involves incrementing by one for non-branching instructions, incrementing by two for satisfied skip instructions, and changing the address for JMP or JMS instructions.

Time States

Six 1-microsecond time states designated T1 through T6 occur during each computer cycle (or major state). Major states are changed at the beginning of time state T6 of each cycle so that logical operations in the new major state can commence with time pulses produced during time state T1. Time pulses, designated TP, occur at the start of each time state except T2. These time pulses initiate gating circuits to perform sequential or synchronized logical operations. Core memory is automatically cycled during each computer cycle so that reading occurs during time states T2 and T3, and writing occurs during time states T5 and T6.

PHYSICAL DESCRIPTION

The standard PDP-5 is contained in a single DEC computer cabinet 60-1/8 inches high, 47 inches wide, and 27-1/16 inches deep. A table 30 inches wide and 18 inches deep is attached to the front of the cabinet, just below the operator console. The operator console contains all keys, switches, and indicators used in normal operation of the computer. When sufficient optional equipment is used with the standard PDP-5, additional cabinets are bolted to the main cabinet. In such cases, the table extends the width of two or more cabinets.

A cabinet is constructed of a welded steel frame covered with sheet steel. Double rear doors are held closed by magnetic latches. A full-width plenum door provides mounting for the power control and power supplies inside the double doors. Controls and indicators used in maintenance activities are located on components mounted on the plenum door. The plenum door is latched by a spring-loaded pin at the top. Double doors at the front of the cabinet conceal module mounting panels above and below the operator console. These mounting panels are positioned within the cabinets so that the connector block wiring is accessible by opening the front doors, and the modules are accessible from the back of the equipment. A fan mounted in the bottom of each cabinet draws cooling air through a dust filter, passes it over the electronic components, and exhausts it through louvered panels and other openings in the cabinet. Four casters allow mobility of each cabinet.

A coordinate system is used to locate cabinets, module mounting panels, modules and signal cable connectors and terminals within a PDP-5 system. The cabinet containing the operator console is always designated cabinet 1, and additional cabinets may be numbered from left to right or right to left, depending upon the configuration. Each 5-1/4 inch position on the front of a cabinet is assigned a capital letter, beginning with A at the top. Figure 1-4 indicates the location of components within the standard PDP-5. Modules are numbered from 1 through 25 from left to right in a mounting panel, as viewed from the wiring side. Connectors on the connector panel (1J) are numbered from 1 through 6, from right to left as viewed from the back of the machine. Blank module and connector locations are numbered. Terminals on a module connector are designated by capital letters from top to bottom. The letters G, I, O, and Q are omitted from module and terminal designations. Therefore, 1C06J is in cabinet 1 (1), the third component location from the top (C), the sixth module from the left (06), and the ninth terminal from the top of the module (J). Components mounted on the plenum door are not identified by location.

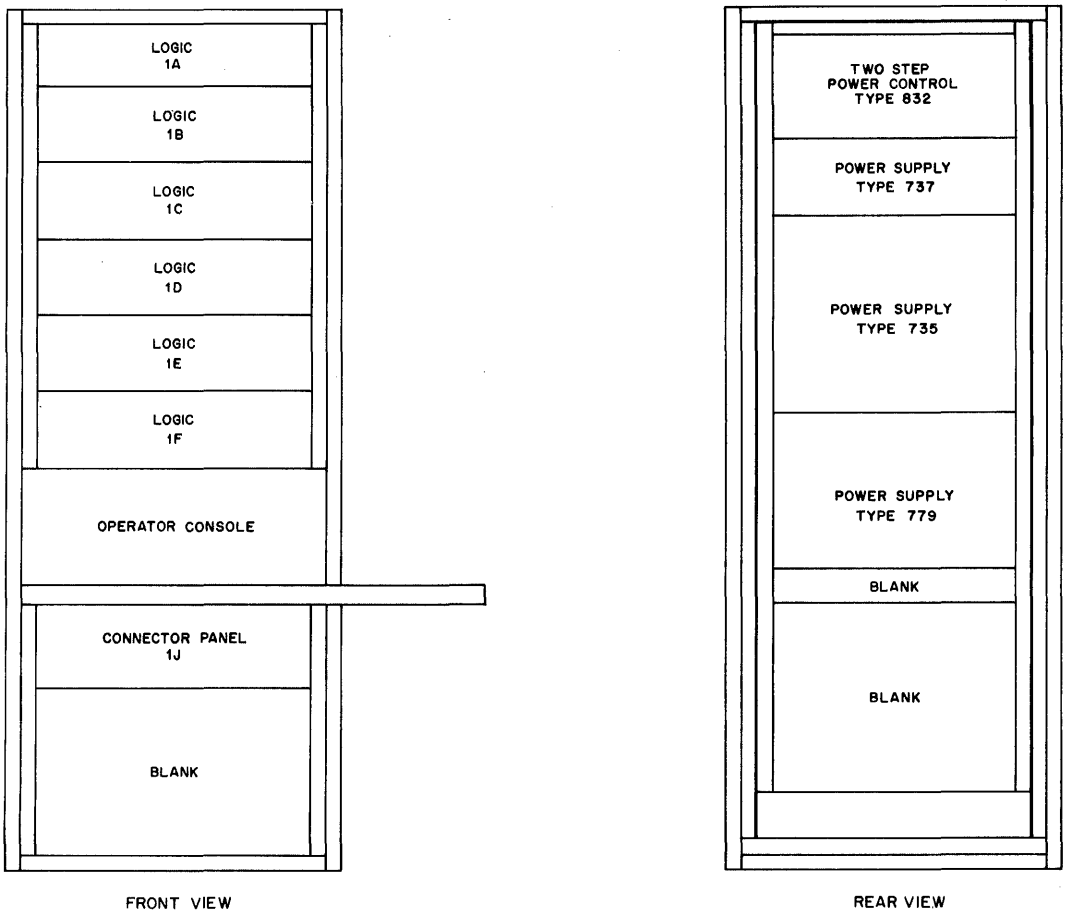


Figure 1-4 Component Locations

The Teletype unit which is standard equipment with the PDP-5 can be used on either side of cabinet 1. This unit is approximately 33 inches high, 22-1/4 inches wide, and 18-1/2 inches deep and is described in detail in the Teletype technical manual.

SPECIFICATIONS

Physical

Cabinet Height:	69-1/8 inches
Cabinet Width:	22-1/4 inches for a single-cabinet PDP-5 (30-inch table) 42 inches for a dual-cabinet PDP-5
Cabinet Depth:	45-1/16 inches

Cabinet Door Clearance:	14-7/8 inches at back
Teltype Height:	33 inches to top of console 44-1/4 inches to top of copyholder
Teletype Width:	22-1/4 inches
Teletype Depth:	18-1/2 inches
Cabinet Weight:	540 pounds for a standard PDP-5 890 pounds (average) for a dual-cabinet PDP-5
Teletype Weight:	40 pounds

Electrical

Power Requirements:	115 volts, 60 cycles, 1 phase, 7.5 amperes for standard PDP-5 (can be constructed for 220 volts or 50 cycles upon special request)
Power Dissipation:	780 watts
Digital Signal Levels:	ground and -3 volts

Ambient Conditions

Operating Temperature:	50 to 104°F (10 to 40°C)
Operating Humidity:	0 to 90% relative humidity
Storage Temperature:	32 to 104°F (0 to 40°C)
Storage Humidity:	less than 90%
Heat Dissipation:	2370 BTU/hour

Functional

Cycle Time:	6 μsec
Word Length:	12 bits
Core Memory Size:	1024 or 4096 words, expandable to 32,768 in fields of 4096 words.

Instructions:	8 basic instructions, 6 memory reference and 2 augmented. The augmented instructions are microprogrammed to produce more than 100 commands.
Input/Ouput Capability:	64 different devices can be individually selected and addressed by 3 command pulses.

SYMBOLS AND TERMINOLOGY

Engineering drawing numbers for this equipment contain five pieces of information, separated by hyphens. Read from left to right these bits of information are a lettered code specifying the type of drawing, a lettered code specifying the size of the drawing, the type number of the equipment, the manufacturing series of the equipment, and the number of a drawing within a particular series. The drawing type codes are:

a. BS, block schematic or logic diagram

b. CL, cable list

c. FD, flow diagram

d. ML, module location diagram

e. RS, replacement schematic

f. UML, utilization module list

g. WD, wiring diagram

In the succeeding sections of this manual, block schematic engineering drawings are specified only by the drawing number. A reference to engineering drawing 9 is interpreted as a reference to BS-E-5-0-9. Block schematic drawings for optional equipment and for all other type drawings are referenced by the complete identification number.

Symbols used on engineering drawings to represent basic logic circuits are defined in Figure 1-5.

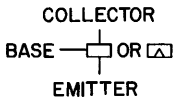
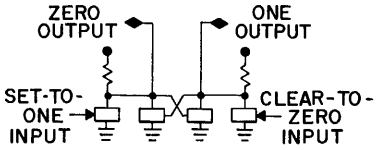
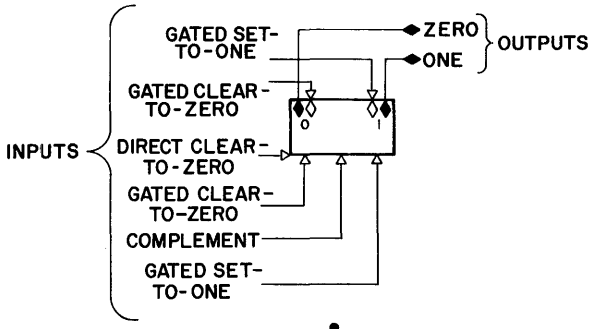
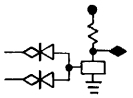
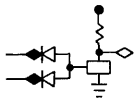
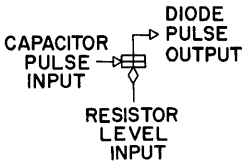
SYMBOL	DEFINITION
	STANDARD DEC POSITIVE PULSE OR POSITIVE-GOING TRANSITION
	STANDARD DEC NEGATIVE PULSE OR NEGATIVE-GOING TRANSITION
	STANDARD DEC GROUND LEVEL SIGNAL
	STANDARD DEC NEGATIVE LEVEL SIGNAL (-3 VOLTS)
	NON-DIGITAL SIGNAL
	LOAD RESISTER CLAMPED AT -3 VOLTS
	PNP TRANSISTOR INVERTER
	NPN TRANSISTOR INVERTER
	BISTABLE MULTIVIBRATOR CONSTRUCTED OF TWO CROSS-COUPLED INVERTERS
	FLIP-FLOP CONSTRUCTED OF FIXED COMPONENTS WITHIN A SYSTEMS MODULE
	DIODE GATE, GROUND-LEVEL NAND OR NEGATIVE-LEVEL NOR
	DIODE GATE, NEGATIVE-LEVEL NAND OR GROUND-LEVEL NOR
	CAPACITOR-DIODE GATE (POSITIVE OR NEGATIVE AS INDICATED BY INPUT SIGNALS)
	CAPACITOR-DIODE GATE (NEGATIVE) WITH OUTPUT PULSE INVERTER

Figure 1-5 Logic Symbols

Conventions and notation on engineering drawings and in text describing the PDP-5 are used as follows:

V	Programming notation for the inclusive OR function.
$\not\vee$	Programming notation for the exclusive OR function.
$\wedge$	Programming notation for the AND function.
=>	Programming notation for an information transfer.
+	Design notation for the inclusive OR function and program notation for addition.
.	Design notation for the AND function.
⟶	Design notation for an information transfer accomplished by a single signal (used without parentheses).
⟶ (jam)	Design notation for a jam transfer of information accomplished by gating both the 1 and 0 inputs of a storage device.
( )	The content of a storage device.
C(A) V C(B) =>(A)	The content of register B is OR combined with the content of register A with the result stored in register A.

$A_{0-5} \xrightarrow{J} B_{6-11}$	The contents of bits 0 through 5 of register A are jam transferred into the contents of bits 6 through 11 of register B.
A_2^1	Bit 2 of register A is in the state corresponding to a binary 1, or contains a 1.
A2(1)	Same as above.
$+1 \longrightarrow A$	The content of A is incremented by 1.
$0 \longrightarrow A$	Register A is cleared or set to contain all zeros.

Other terms used in this manual are defined as follows:

set - means to set a storage device to the state corresponding to a binary 1.

clear - means to establish the state corresponding to a binary 0.

flag - a flip-flop or signal that is sensed by the program to indicate a specific equipment condition or status.

instruction - a computer word which causes a specific machine function and which is identified by a distinct operation code.

microinstruction - an instruction in which numerous different machine functions can be programmed by the placement of ones and zeros in bits other than in the operation code. Effectively the entire word is used as an operation code which is decoded, not only by the instruction register, but by gating circuits within the machine.

command - a signal that causes a specific operation to occur as the whole or partial execution of an instruction or microinstruction.

subroutine - a routine that can be called upon from any core memory address of the main program to provide a service to the main program or peripheral equipment, usually to perform operations that are repeated many times, and thus to simplify the main program.

program interrupt - an interruption in the main program caused by transfer of program control to a subroutine, after storing the current program count. The interruption is initiated by peripheral equipment to cause a subroutine to be executed. Usually the subroutine is used to locate the equipment that caused the interrupt and to transfer information with it, or service it in some way.

data break - a temporary halt or break in the main program used to transfer data with peripheral equipment under control of the peripheral equipment (not under direct computer program control).

operand - a stored number to be mathematically operated upon.

address of the operand - the location of a core memory register currently containing the operand.

absolute address - a 12-bit number used directly to specify any address in core memory.

effective address - the address of the operand as specified in an instruction or by an absolute address.

SECTION 2

PROCESSOR

The major arithmetic, logic, and control functions performed by the PDP-5 are accomplished by logic circuit elements of the processor. All operations of the PDP-5 are performed by the processor except those directly concerning data storage and retrieval in core memory, and information transfers to or from peripheral equipment. In performing these operations the processor draws instructions from core memory and executes them by sequentially entering one of six major control states. Each control state lasts for the duration of one computer cycle in which there are six time states, each of which produces various logical operations depending upon the major control state.

Functional operation of the processor can be compared to a three dimensional matrix. As in the matrix an X, Y, and Z coordinate must be specified to locate a given point, so within the processor an instruction, major state, and timing pulse determine the specific logic function performed. A change in any of these three items changes the resultant logical operation. Therefore, assuming one instruction and one state, as many different operations may be executed as there are timing pulses employed. In general, states are entered as a function of the current instruction, except that the break state is initiated by a break request originating in peripheral equipment, and the program count state is entered to locate the next instruction when no other state need be entered. Execution of each of the eight instructions requires two or more states to be entered. Each state lasts for 6 microseconds and so has five timing pulses available for initiating sequential logical operations.

POWER CLEAR GENERATOR (5)

During the power turn on sequence, the power clear generator produces repeated Power Clear pulses at a 500 kc rate. These pulses clear the run and I/O-hlt flip-flops to assure that transients within the machine do not start computer operation. These pulses are also supplied to terminals 1J01-49 and 1J03-47 of the interface connectors and to the line unit out (LUO) buffer of the Teletype control to assure that registers of I/O devices are cleared or are in some preset state prior to programmed operation. The logic circuits for this functional element are shown on the upper left side of engineering drawing 5.

In the power turn on sequence, the 735 Power Supply, which produces the memory currents, is energized through the delayed closure/fast release contact K2 of the 832 Power Control. The time delay of K2 is between 3 and 5 seconds, so for this period of the turn on sequence the -35 volt output of the 735 supply is essentially at ground potential. The ground potential is supplied through the centertap of the power transformer and diode D4 of the rectifier in the 735 Power Supply. This potential from terminal E of the 735 Power Supply is isolated by two series-connected inverters of the 4102 module at location 1E04 and is used to enable or disable the 4401 Clock module at location 1E05. The initial ground potential is isolated from the clock module by an external diode connected to terminal V, so the clock is uninhibited and generates the standard DEC negative pulses designated the Power Clear pulses. After the initial delay the -35 volt power supply output causes a -3 volt level to be supplied to terminal V of the clock from the clamped load resistor of the last inverter. This level inhibits operation of the clock and prevents generation of Power Clear pulses during full computer excitation.

SPECIAL PULSE GENERATOR (5)

Operation of the keys and switches causes the computer to perform functions similar to those performed automatically during execution of instructions. These operations require sequenced timing pulses which are provided by the special pulse generator. The special pulse generator is shown on the upper left portion of engineering drawing 5.

Initiation of the special pulse generator occurs at the positive-going leading edge of the Key Manual signal. This signal is produced when any of the manual keys, except the STOP key, are operated. The Key Manual signal is inverted to produce the negative shift required to initiate operation of the 4410 Pulse Generator module at location 1E06. The output of this pulse generator is a 1-microsecond negative pulse, designated the SP0 pulse, which is distributed to the run control element to clear the run flip-flop, to terminal 46 of interface connector 1J03, and to the pulse input of the 4301 Delay module at location 1E07. The delay module produces a 10-microsecond delay between generation of the SP0 pulse, which is generally used to clear registers and control devices in peripheral equipment using the data break facility, and generation of the SP1 through SP3 pulses, which strobe registers or transfer information. The standard DEC negative pulse output of the delay module initiates operation of the first pulse amplifier circuit on the 4604 module at location 1E08. Each of the three pulse amplifier circuits on this

module produces a 1-microsecond negative pulse which is designated by an appropriate SP number. The series connection of these pulse amplifiers causes turn off of SP1 to initiate generation of SP2, and the turn off of SP2 to initiate generation of SP3. When SP3 expires, the special pulse generator has completed its operation and awaits another Key Manual signal, since this circuit is not regenerative.

TIMING SIGNAL GENERATOR (17)

The basic timing cycle of the PDP-5 is determined by the 1406 Crystal Clock module at location 1C25. The standard DEC 70-nanosecond negative pulse output of this 1-megacycle crystal clock is converted to 400-nanosecond DEC standard negative pulses, required to operate the 4000 series system modules of the computer, by the 4604 Pulse Amplifier module at location 1C24. The negative pulse output from this pulse amplifier is supplied to terminal 45 of interface connector 1J01 and provides the trigger pulse input to the 4127 Pulse Inverter module at location 1C21 which drives the 4215 Four-Bit Counter module at location 1C22. All timing pulses used in automatic operation of the computer are derived from the state of these flip-flops and are shown in the timing diagram of Figure 2-1. The pulse inverter circuit which drives the least significant bit (TG_3) of the counter is controlled by the 4115 Positive Diode NOR module at location 1D10 which functions as a ground-level NOR to enable the pulse inverter, and serves as a negative NAND gate to inhibit operation of the counter. Therefore, if any of the flip-flops in this 4-bit ring counter are in the 1 state except TG3, or if the run flip-flop is in the 1 status, a ground potential is applied to one of the signal inputs to this gate, and the counter is enabled and allowed to advance upon receipt of each output pulse of the crystal clock. Conversely, the counter will run until all inputs to this gate are negative; this occurs in time state T1 when the run flip-flop is in the 0 state. The state and/or transition of the 4-bit counter initiates operation of the 4604 and 4606 Pulse Amplifier modules at locations 1C24 and 1C23 to produce the TP pulses used throughout the logic circuits to initiate clock-based sequence operations.

When the computer is energized initially, the counter commences in time state T1, and so no TP1 pulse is generated as a function of the counter. A TP1 pulse is generated under either of the following conditions:

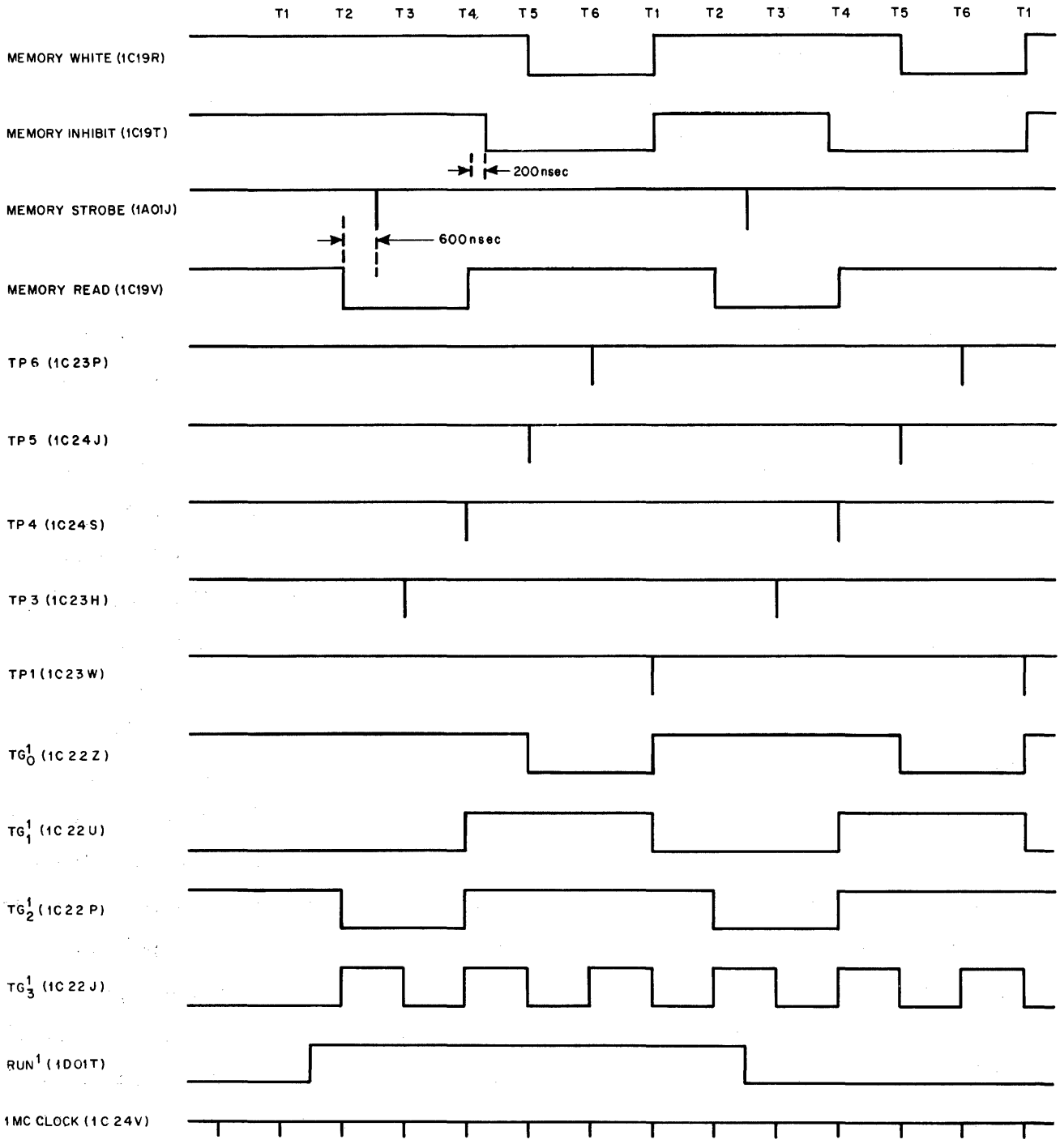


Figure 2-1 Timing Diagram

a. During SP1 after operation of the CONTINUE key.

b. When TG_1 changes from the 1 to the 0 state and either the EXAMINE or DEPOSIT key is operated, or the run flip-flop is in the 1 state, or the I/O-hlt flip-flop is in the 1 state.

This gating is effected by the negative NAND circuit of the 4113 module at location 1C11 and the ground-level NOR gate of the 4115 module at location 1D10 which provide enabling levels to the pulse amplifier circuit producing the TP1 pulse. Therefore, the TP1 pulse is produced for each machine cycle except the first cycle of operation initiated by the START key, and during time state T1 immediately following receipt of an I/O Halt signal. Timing pulses TP4 and TP5 are supplied to terminals 39 and 40 of the data break interface connector 1J03 for use in input-output equipment as well as for use in the processor.

The timing pulses which control cyclic memory functions are generated by transistor gating circuits which combine the conditions of various flip-flops in the 4-bit counter directly and through delay lines. Since the TP pulses which produce operations in the processor and the memory control signals are derived from the same timing source (the 1-megacycle crystal clock), the processor and the core memory are synchronized. During each computer cycle, core memory is in the read status during time states T2 and T3 due to the presence of the Memory Read signal derived from the binary 1 state of flip-flop TG_2 and is in the write state during time states T5 and T6 due to generation of the Memory Write signal derived from the binary 1 status of flip-flop TG_0. The Memory Strobe pulse, which allows the sense amplifiers to sample information induced on the sense windings during the read operation, is a DEC standard negative pulse produced by a circuit of the 1607 Pulse Amplifier module of 1A01. Operation of this pulse amplifier is initiated 600 nanoseconds after the start of the Memory Read signal, except under the conditions specified by the signal supplied to the 4-input negative NOR diode gate of the 4115 module at location 1C18. This gate inhibits generation of the Memory Strobe pulse during the program count state of a JMP or JMS instruction, during the execute 1 state of a DCA instruction, during the execute 2 state of a JMS instruction, or during a data break in which the direction of data transfer is into the PDP-5. To assure that data bits containing zeros are inhibited during writing, the Memory Inhibit signal is generated beginning 200 nanoseconds after the end of the Memory Read signal and ending with expiration of the Memory Write signal. The Memory Inhibit signal is generated as a function of the binary 1 state of flip-flop TG_1 by

the 2-transistor NOR circuit composed of inverter ST of the module at location 1C19 and inverter UVW of the module at location 1A01. The 1311 Delay Line module at location 1C20, whose output line is normally held at -3 volts by clamped load resistor F of the module at 1D07, and the inverter ST inhibit generation of the Memory Inhibit signal during the first 200 nanoseconds of the 1 state of TG_1. The inverter UVW assures turn off of the Memory Inhibit signal as soon as TG_1 reverts to the 0 state.

OPERATOR CONSOLE (WD-D-5-0-10)

The operator console provides a means of manually controlling the operation of the computer, manually inserting data into flip-flop and core memory registers, and provides visual indication of the contents of the most important registers and control flip-flops. Wiring connections to the keys and switches on the operator console are shown on engineering drawing WD-D-5-0-10, and the logic signal level gating of the signals produced by the keys and switches is indicated on engineering drawing BS-D-5-0-5. Indicator lamps and drivers are shown on the appropriate replacement schematic drawings; connections to these drivers are indicated on cable lists CL-A-5-0-20 and 21, and the isolating resistors and connections between flip-flops or registers and the input to the indicator drivers are shown on the appropriate block schematic engineering drawings for the registers or control flip-flops.

Interlock and POWER Switches

One deck of the interlock switch is connected in parallel with the POWER switch so that if either of these switches is closed, a short circuit is provided between terminals 2 and 4 of the 832 Power Control. This short circuit supplies primary power to the coils of the time-delay relays which control the application of primary power to the power supplies. The POWER indicator is connected directly between ground and the -15 volt output of one of the power supplies and therefore lights to indicate the presence of secondary power.

A second deck of the interlock switch supplies either ground or -15 volts to the circuits of the keys and switches on the operator console. When this switch is in the locked position, ground potential is supplied to these circuits to disable them. When the switch is unlocked, -15 volts

enables the switch circuits. Therefore, in the locked position the interlock switch prevents power turn off by means of the POWER switch and disables all of the keys and switches on the operator console except the SWITCH REGISTER toggle switches.

Key Circuits

When the computer is energized and the interlock switch is in the unlocked position, operating any of the keys or setting either the SINGLE STEP or SINGLE INST switch to the right position supplies -15 volts to an appropriate terminal of connector 1H04. Negative 15-volt signals supplied to this connector are combined in transistor and diode gating circuits shown in the lower left portion of engineering drawing 5. These diode-transistor gating circuits produce the Key Manual signal (which initiates operation of the special pulse generator) and produce other conditioning signal levels (which enable appropriate gates which are triggered by SP pulses during manual operations).

Indicator Circuits

Indicators on the operator console are 28-volt incandescent lamps driven by 4903 Light Bracket Assemblies or 4904 Short Light Bracket Assemblies. These assemblies contain a number of series circuits consisting of a transistor switch connected between an indicator and ground potential. One side of each of the indicators is connected in common to -15 vdc. Ground potential is connected in common to the emitter of each transistor switch through parallel-connected diodes which provide the appropriate emitter-base junction bias. Each transistor switch is turned on by a negative signal level applied to the base through a 3000-ohm resistor connected to the output of a flip-flop. When the output of a flip-flop is at ground potential, the transistor switch is cut off, and the circuit to the indicator lamp is incomplete. When the output of the flip-flop is at -3 volts, the transistor switch is closed to energize the indicator with approximately 14 volts.

SWITCH REGISTER Toggle Switch Circuits

The 12 toggle switches which comprise the switch register (SR) supply enabling or disabling signal levels to the level input of positive capacitor-diode gates of the input mixer to allow the condition of the switches to be sensed automatically by the OSR instruction. A switch set

to the up position corresponds to a binary 1, and supplies a ground-potential enabling signal level to a capacitor-diode gate of the appropriate bit of the input mixer through a 1k resistor and a terminal of connector 1H04. A switch in the down position corresponds to a binary 0, and supplies a -15 volt signal to disable an input mixer capacitor-diode gate through the same path. Connections to the input mixer from the SR are indicated on engineering drawing 14.

RUN AND I/O HALT CONTROL (5)

Control of the circuits which produce the timing signals of the PDP-5, and hence which control automatic operation of the computer, is exercised by the run and I/O-hlt flip-flops. These flip-flops and their associated input gating circuits are shown on the right side of engineering drawing 5. The run flip-flop enables the timing circuits to generate timing signals when in the 1 state. The 1 output from this flip-flop is also supplied to terminal 42 of the data break interface connector 1J03 (via a bus driver circuit shown on engineering drawing 31). The I/O-hlt flip-flop provides a means of setting and clearing the run flip-flop by means of signals supplied by an I/O device.

The run flip-flop is cleared by a positive pulse that grounds terminal U of the 4215 module at location 1D01 under one of the following conditions:

a. During the power turn off and turn on sequence by the Power Clear pulses.

b. By an SP0 pulse following operation of either the START, LOAD ADDRESS, EXAMINE, DEPOSIT, or CONTINUE key.

c. By a TP6 pulse to conclude operations when the STOP key is pressed or to conclude an operation when the SINGLE STEP or SINGLE INST switches are in the on (right) position.

d. By a TP5 pulse during an operate 2 instruction in which bit 10 is a 1 to provide a programmed halt.

e. By the positive transistion of the signal at terminal 1D01N when the I/O-hlt flip-flop changes from the 0 to the 1 state.

The run flip-flop is set by a positive pulse that grounds terminal T under one of the following conditions:

a. By an SP3 pulse after operation of either the CONTINUE, START, EXAMINE, or DEPOSIT key.

b. Upon receipt of a Restart pulse from an I/O device when the I/O-hlt flip-flop is in the 1 state.

The I/O-hlt flip-flop is cleared by a positive pulse that grounds terminal P by Power Clear pulses, by an SP0 pulse, or by a Restart signal in the same manner as these pulses clear the run flip-flop. The I/O-hlt flip-flop is set by a positive pulse that grounds terminal N when a standard DEC negative pulse is supplied to terminal 1S12U during T6 of an ADC miscroinstruction for the Type 37 Analog-to-Digital Converter, or by receipt of a similar negative I/O-Halt signal received at terminal 46 of interface connector 1J01.

PROGRAM COUNTER

Address 0000 in core memory is used as the program counter (PC) and contains the core memory address from which the last instruction was taken. During a program count (P) state, the contents of the PC is read into the memory buffer register, is incremented, and is written back into the PC. The contents of the memory buffer register is then transferred into the memory address register as the address of the current instruction. Use of a core memory register for the PC allows the program sequence to be manipulated by the program in the same manner as the contents of any core memory location.

INSTRUCTION REGISTER (6)

The instruction register (IR) consists of a 4-bit flip-flop register that determines the instruction currently being performed, based on the 3-bit operation code, and controls entry into the defer state during memory reference instructions. This register consists of a 4215 4-Bit Counter module at location 1D22 with the associated input gating circuits and output decoding circuits indicated on the right side of engineering drawing 6.

The IR is cleared by the positive pulse output at terminal 1C01X of a gated pulse amplifier on a Type 4606 module. The IR is cleared by one of the following:

a. During manual operation by the SP1 pulse following operation of either the START, EXAMINE, or DEPOSIT key. Clearing by the SP1 pulse allows the register to be set by the SP2 pulse to a specific operation code appropriate to the key which is operated. The gate pulse that initiates clearing the IR under these conditions is routed to the program interrupt synchronization logic as the 0 ⟶ Int Ack signal.

b. By a TP5 pulse in either the program count or break state.

During the program count state, the IR is cleared in preparation for receiving the new operation code during time state T3 of the following fetch state. During the break state, the IR is cleared to dispose of the instruction preceding the break in case the break lasts for longer than one cycle. If the instruction in progress at the time of the break request is a rotate or increment accumulator microinstruction, these operations are completed during T1 of the break cycle. Therefore, the IR is cleared at T5 of the first break cycle so that these operations are not repeated in successive break cycles.

The IR is set by supplying a standard DEC positive pulse to ground the flip-flop output terminal which is normally at ground level when the flip-flop is in the 1 state. During manual operation, bits 0 through 3 of the IR are set by an SP2 pulse to force an instruction determined by the key which is operated. (START sets bits 0 and 2 to force a JMP; DEPOSIT sets bits 1 and 2 to force a DCA instruction, or EXECUTE sets bit 2 to force a TAD instruction.) This gating is produced in the 4127 Pulse Inverter module at location 1D23.

During a program interrupt, when the Interrupt Acknowledge signal level is present, bit 0 of the IR is set during T3 of the fetch state to force a JMS instruction. Forcing the JMS instruction causes the fetch state to be followed by the execute 1 state, the execute 2 state, and the program count state. These states are entered to store the contents of the program counter in core memory location 0001 and to transfer program control to address 0002. In normal operation, when no interrupt request is present, all four bits of the IR are set to correspond with the contents of memory buffer register bits 0 through 3 during time state T3 of the fetch cycle.

This operation corresponds to sensing the operation code and indirect address bit, and instigates execution of a new instruction. The gating which performs setting of the IR in this manner consists of the 4127 Pulse Inverter module at location 1D24 and the 4112 Negative Diode NOR module at location 1D16. In this application the 4112 module circuits function as ground-level NAND gates.

The outputs from bits 0 through 2 of the IR are supplied to indicators on the operator console and to a 1151 Binary-to-Octal Decoder module at location 1D21. Decoding of the content of the IR produces the eight instruction control signals used in the PDP-5.

MAJOR STATE GENERATOR (6)

The six complementary pairs of control signals which indicate the state, or mode, in which the computer is operating are produced by the logic element shown on the left side of engineering drawing 6. These signals, combined with the instruction in progress and timing pulses, perform most of the gating which performs the logical operations of the computer. The operations performed by the computer in each state are described in detail in Section 5 of this manual.

The major state generator consists of a 6-state device composed of six 5-input ground-level NOR gates composed of the 4117 modules at locations 1D18 and 1D19. The output from each of these gates is the normal state signal which is at ground potential during the indicated state; program count (P), fetch (F), execute 1 (E1), execute 2 (E2), defer (D), and break (B). Each of these signals is inverted by a circuit of the 4102 module at location 1D20 to provide a complementary signal for each of the control states. The inverted state signals are distributed with the normal state signals throughout the processor and are supplied to circuits which drive the indicators on the operator console. The inverted break signal is also supplied to terminal 41 of the data break interface connector 1J03 via the output bus drivers shown on engineering drawing 31. The output of each NOR gate is also supplied to one input of each of the other NOR gates. This arrangement prevents any state signal from being generated during any of the other states. A state is set by grounding the output terminal of the NOR gate with a positive pulse from a 4127 Pulse Inverter module at location 1D17 or 1D23. Forcing the output of a NOR gate to ground potential by the positive output of a pulse inverter disables all other state NOR circuits and so enables the input to the gate whose output is pulsed.

The pulse inverters which set the states are enabled by diode gating circuits as a function of the current state, the current instruction, the content of bit 3 of the instruction, and/or the condition of the Break Request signal supplied externally and are all initiated by the TP6 pulse. Pulse amplifiers of the module at location 1D23 set the P state during SP2 when the START key is operated or set the E1 state during SP2 when either the EXAMINE or DEPOSIT key is pressed. Setting of a state is normally triggered by a TP6 pulse so that operations within that state can commence, or be initiated, by a TP1 pulse. The gating circits which enable entry into each state respond to the following conditions:

a. The program count state can be entered from any other state and is normally entered when the conditions present do not allow entry into any other state. Entry into the P state is enabled by the 4116 module at location 1D12 which functions as a negative NOR circuit to inhibit setting P if any other state can be entered. When conditions are not present to set the execute state, defer state, or break state, and the current state is not the P state, all of the inputs to this NOR gate are at ground potential. Therefore, entry into the P state is not inhibited, so the negative P Set signal level is produced to enable the pulse inverter.

b. The fetch state is entered following each P state and can not be entered from any other state. Therefore, the inverted P signal alone supplies the direct enable signal to the pulse amplifier to set the F state.

c. The defer state is entered only at the conclusion of the fetch state when bit 3 of the instruction is a 1 (indicating indirect addressing or deferring) and the current instruction is a memory reference instruction (which is not an IOT or an operate instruction).

d. The execute 1 state is entered from either the fetch or defer states for all instructions requiring more than two cycles. These instructions are JMS and the instructions having an operation code of less than four (AND, TAD, ISZ, and DCA). Therefore, the E1 state is entered from the defer state for

instructions requiring more than two cycles and is entered from the fetch state for instructions requiring more than two cycles which do not employ indirect addressing (bit 3 of the instruction is a 0).

e. The execute 2 state is entered only from the execute 1 state during a JMS instruction or following operation of either the EXAMINE or DEPOSIT key. Note that execution of a JMS instruction or pressing of either the EXAMINE or DEPOSIT key causes entry into the E1 state and thus enables entry into the E2 state for the following computer cycle.

f. The break state is entered only from the fetch state at the conclusion of 2-cycle instructions or from the execute 1 state at the conclusion of instructions requiring more than two cycles. When a Break Request signal is present at terminal 43 of interface connector 1J03 at T4 time, this condition is stored in a flip-flop composed of inverter LK of the 4102 module at location 1D06 and negative NOR SRT of the 4112 module at location 1E03. This flip-flop is cleared by the TP3 pulse to synchronize operations of the computer with peripheral equipment during a data break by assuring that break requests made after T4 time are not honored until the next cycle. The 1 status of this flip-flop, in which terminal 1D06L is at ground potential, provides one of the conditioning signal inputs to the ground-level 2-input diode NAND gate which produces the B Set signal.

The second input to the NAND gate which produces the B Set signal is present if the computer is currently in the break state (to allow multiple-cycle data break operation), or if the computer is in the execute 1 state but not performing a JMS instruction (indicating that the last cycle of instructions requiring more than two cycles is taking place), or if the computer is currently in the fetch state and is executing either an IOT or OPR instruction (indicating that the last cycle of a 2-cycle instruction is being executed).

MEMORY ADDRESS REGISTER CONTROL (7)

All of the signals used to control the operation of the memory address register (MA) are produced by the control logic circuit shown on the left side of engineering drawing 7. This logic element consists of six pulse amplifiers which produce the standard DEC positive pulses that cause the clearing, shifting, and transfers of information within the MA and also consists of the diode gating circuits which control the initiation of these pulse amplifiers. Diode gating circuits and a flip-flop composed of two cross-coupled inverters are also contained in this logic element and produce the Disable MA signal, which forces the output terminals of the MA to simulate address 0000.

Pulse amplifier circuits FJHKL and NRST of the 4606 module at location 1C15 produce pulses which clear the least significant seven bits of the memory address register and the five most significant bits of the memory address register respectively. Both pulse amplifiers are initiated simultaneously and thus clear the entire MA under either of the following conditions:

a. At SP1 time following operation of the LOAD ADDRESS key, thereby clearing the MA to allow a new address to be set into it from the switch register.

b. By the TP1 pulse during the execute 1 state of program interrupt operations, so that the program count can be read and subsequently stored in address 0001.

The Clear MA_{0-4} pulse is also produced under either of the following conditions:

a. By the PT1 pulse during the execute 1 state of a memory reference instruction in which both the indirect bit and the memory page bit contain a 0, indicating that the effective address is to be taken from page 0 of core memory at the address specified by bits 5 through 11 of the instruction.

b. By the TP1 pulse during the defer state for an instruction in which the memory page bit is a 0 (MB_4^0), indicating that the effective address is to be taken from memory page 0 at the address currently specified by bits 5 through 11 of the MA.

The MA Carry Enable signal is a DEC standard ground level that enables the capacitor-diode gate at the complement input of each flip-flop of the MA, thus allowing the MA to function as a binary counter. This signal is produced at terminal 1C11H of the 4113 Diode module under any of the following conditions:

a. When either the EXAMINE or DEPOSIT key is pressed, allowing the MA to be incremented and facilitating examination or depositing of information in core memory at sequential addresses without specifying each address.

b. During the execute 2 state of a program interrupt operation to allow incrementing of the MA to address 0001 for storing the program count.

c. During the break state when the Increment Request signal is received at terminal 45 of interface connector 1J03 to allow data break transfers to occur at sequential core memory addresses without specifying each address.

The MA Carry Enable signal also is gated by the TP1 pulse to produce the Count MA signal at terminal 1C11P. This positive pulse is supplied to the pulse input of the capacitor-diode gate at the complement input of flip-flop MA_{11}, thus incrementing the content of the MA at T1 time under any of the conditions specified for generation of the MA Carry Enable signal.

The Data Address ⊣► MA signal is a standard DEC positive pulse produced at terminal 1C16F of the 4102 Pulse Amplifier module. This pulse initiates operation of the capacitor-diode gates at the input of the MA to provide a jam transfer (a transfer of both ones and zeros) into the MA of the address supplied to terminals 26 through 37 of interface connector 1J03 from an external device. This signal is also supplied to terminal 49 of interface connector 1J03 as the Address Accepted pulse. The signal is produced by a TP1 pulse during the break state when the Increment Request signal is not present at terminal 1J03-45.

The SR ⟶ MA signal is produced at terminal 1C16K. This standard DEC positive pulse is applied to a capacitor-diode gate at the 1 input of each MA flip-flop to provide a ones transfer from the contents of the switch register into the MA. This pulse is produced during SP2 following operation of the LOAD ADDRESS key (the MA having been cleared during SP1).

The MB $\rightarrow$ MA_{5-11} pulse is a standard DEC positive pulse produced at terminal 1C16N. This pulse strobes the positive capacitor-diode gates at the input of each MA flip-flop to provide a jam transfer between the 7-bit address of an instruction into the MA. This pulse is produced by a TP1 pulse during the fetch state, or during the defer state, or during an execute 1 state which is not caused by a program interrupt.

The MB $\rightarrow$ MA_{0-4} signal is a standard DEC positive pulse produced at terminal 1C12F of a 4603 Pulse Amplifier module. This signal triggers the capacitor-diode gates at the input of MA flip-flops 0 through 4 to provide a jam transfer between the contents of corresponding bits of the memory buffer register and the memory address register. This signal is produced under either of the following conditions:

a. By the TP1 pulse at the beginning of a fetch state to correspond with generation of the MB $\rightarrow$ MA_{5-11} pulse to transfer the entire word contained in the MB into the MA.

b. By a TP1 pulse at the beginning of an execute 1 state of an instruction in which the indirect address bit is a 1 (IR_3^1).

The Disable MA signal is a standard DEC positive signal level which forces the output terminals of the MA to simulate address 0000 without disturbing the contents of the register. Therefore this signal allows information to be read or written in the program counter. The signal is produced at terminal 1D09Z, which is the buffered 1 output of the flip-flop composed of crossed-coupled inverters WX and YZ of the 4102 module at location 1D06. This flip-flop is in the binary 1 state when terminal 1D06X is at -3 volts, thus producing a ground-potential Disable MA signal. The flip-flop is set by a positive pulse that grounds terminal 1D06D under one of the following conditions:

a. During SP3 following operation of the START key.

b. By a TP1 pulse occurring at the start of a program count state.

c. By a TP1 pulse at the start of an execute 1 state for a JMS instruction.

The flip-flop is cleared by a positive pulse that grounds terminal 1D06X under either of the following conditions:

a. During SP1 time following operation of the LOAD ADDRESS, EXAMINE, or DEPOSIT key.

b. By a TP1 pulse at the start of all states that are not the program count state or which are not the execute 1 state of a JMS instruction.

MEMORY BUFFER REGISTER CONTROL (7)

The logic circuits which produce the signals that control the operation of the memory buffer register (MB) are shown on the right side of engineering drawing 7. This logic consists of transistor and diode gating circuits and six pulse amplifiers.

The Clear MB signals for bits 5 through 11 and 0 through 4 are produced at terminals 1C15X and 1C14X, respectively. These standard DEC positive pulses are applied to the direct clear input terminals of the respective MB flip-flops. Since generation of the Clear MB_{5-11} pulse initiates operation of the pulse amplifier to produce the Clear MB_{0-4} pulse, the entire MB is cleared under one of the following conditions:

a. Upon receipt of a Restart 1 pulse from the Type 137 Analog-to-Digital Converter signifying that the program can continue. The converter leaves unwanted information in the MB during its programmed I/O halt operation, and so the MB is cleared before resumption of the main computer program.

b. During SP1 following operation of either the START, EXAMINE, or DEPOSIT key to remove any extraneous number from the content of the MB at the start of a program or when a word is to be read from or written into core memory by means of the keys.

c. By means of a TP1 pulse during the fetch, defer, execute 1, or break state of any instruction or during the program count state of either a JMP or JMS instruction.

The Clear MB_{0-4} signal is also produced by the TP1 pulse at the beginning of a program count state of a JMP instruction directly to an address on memory page 0.

The AC → MB signal is a DEC standard positive pulse produced at terminal 1C12K during T3 of an execute 1 state of a DCA instruction. This pulse triggers capacitor-diode gates at the input of each MB flip-flop to transfer the content of the AC into the MB so that the word contained in the accumulator can be written in core memory.

The Count MB signal is a standard DEC negative pulse produced at terminal 1D09Z and supplied to a 2-input negative NAND gate which provides the pulse input to the capacitor-diode gate at the complement input of the MB_{11} and MB_{10} flip-flops. The content of the MB is incremented by one or by two to advance the program count as a function of the condition of the skip flip-flop. The Count MB signal triggers diode gate EFH of the 4113 module at location 1D02 to complement MB_{11} and increment the content of the MB by one if the skip flip-flop contains a 0. The Count MB signal triggers diode gate EFH of the 4113 module at location 1D13 to complement MB_{10} and increment the content of the MB by two if the skip flip-flop contains a 1. The Count MB signal pulse occurs 2 microseconds after the MB Carry Enable signal is produced so that the carry pulses produced by incrementing the MB can be propogated through the register. The content of the MB can also be incremented by one upon receipt of a positive pulse received from an external device at terminal 38 of data break interface connector 1J03. The Count MB pulse is produced by a TP4 pulse under one of the following conditions:

a. During the defer state when the address of the operand is between 0010 and 0017 (indicating an instruction using the auto-indexing core memory registers).

b. During the program count state of all instructions except the JMP. The MB is not incremented during a JMP instruction because program control is transferred to an address specified in the instruction so that the sequential instruction address sequence is broken.

c. During the execute 1 state of an ISZ instruction to provide the incrementing prior to sensing by the skip control element.

d. During the execute 2 state of a JMS instruction (not during a program interrupt).

The MB Carry Enable signal is produced at terminal 1C18Z of the 4115 Positive Diode NOR module. This DEC standard positive level signal enables the capacitor-diode gates at the complement input of each MB flip-flop to allow operation of the MB as a binary counter. This signal is produced from the start of time state T2 until the end of time state T4 during all major states utilizing a memory strobe, in other words in all states except execute 1 of a DCA instruction.

The MA $\dashrightarrow$ MB signals are produced at terminals 1C14J and 1C14R for bits 0 through 4 and bits 5 through 11 of the MB, respectively. These DEC positive pulses initiate operation of the positive capacitor-diode gates at both the 1 and 0 inputs of each MB flip-flop to effect a jam transfer from the memory address register into the memory buffer register. Both pulse amplifiers are initiated to provide a 12-bit transfer between the MA and MB under the following conditions:

a. During SP3 following operation of the START key, thereby setting an effective program starting address into the MB.

b. By a TP1 time pulse during the program count state of a JMS instruction, allowing the effective address to be set into the MB from the instruction address rather than from core memory.

The MA $\dashrightarrow$ MB_{0-4} pulse is also produced by a TP1 pulse during the program count state of a JMP instruction in which bit 3 is a 0 and bit 4 is a 1. This transfer allows the five most significant bits of the instruction address to be saved during jump instructions within the current memory page.

The Data $\longrightarrow$ MB signal is a DEC standard positive pulse produced at terminal 1C12N. This pulse triggers the capacitor-diode gates at the 1 input of each MB flip-flop to transfer information into the MB from an external device supplying signals to terminals 13 through 24 of the data break interface connector 1J03. This pulse is also returned to terminal 48 of connector 1J03 to indicate to the external device that data supplied to the computer has been received.

This pulse is produced by a TP3 pulse during the break state in which the direction of transfer is into the PDP-5 (core memory write request). The direction of this transfer is indicated by a -3 volt signal supplied by the external device to terminal 43 of connector 1J03 which is connected to terminal 1C17S of a 2-input negative NAND gate on the 4113 Diode module.

ACCUMULATOR CONTROL (8)

The logic circuits that produce the six positive and two negative DEC standard pulses which control the operation of the accumulator (AC) are shown in the top left portion of engineering drawing 8. The circuits consist of 4606 Pulse Amplifier modules with appropriate diode and pulse inverter gating.

The Clear AC signal is produced at 1C01J under any of the following conditions:

a. During SP2 following operation of either the DEPOSIT, EXAMINE, or START key.

b. By the TP6 pulse during the fetch state of IOT microinstruction KCC (command 6032, clear AC and keyboard flag).

c. Upon receipt of a standard DEC positive pulse at terminal 47 of interface connector 1J01 from an I/O device.

d. By a TP6 pulse in the fetch state of IOT microinstruction ADC (command 6004, convert analog signal to digital value on the Type 137 Analog-to-Digital Converter).

e. By a TP4 pulse during the fetch state of an operate 1 or operate 2 instruction in which bit 4 is a 1. These conditions designate a CLA microinstruction.

f. By a TP3 pulse during the execute 1 state of a DCA microinstruction.

The positive SR ⟶ AC signal initiates operation of the capacitor-diode gates in the input mixer to transfer the word contained in the switch register into the accumulator. Connection of this signal to the input mixer is shown on engineering drawing 14. This signal is produced

at SP3 time following operation of the DEPOSIT key or by a TP5 pulse during the fetch state of an OSR microinstruction (these conditions being determined by the presence of an operate 2 instruction having a binary 1 in bit 9).

The Half Add signal is a positive pulse produced at 1C02J. This pulse initiates operation of the capacitor-diode gate at the complement input of each AC flip-flop to perform an exclusive OR operation between the content of the memory buffer register and the content of the accumulator. This pulse is produced by a TP4 pulse during the execute 1 state of a TAD instruction. The second half of the TAD instruction takes place during time state T6 by means of the Carry Initiate pulse.

The Carry Initiate signal is a negative pulse produced at terminal 1C02W. This pulse is supplied to the pulse input of a negative capacitor-diode gate whose input is enabled when a memory buffer bit holds a binary 1 and the corresponding bit of the accumulator holds a 0. The output of this capacitor-diode gate is inverted by a pulse inverter to provide a direct input to the next most significant bit of the accumulator (or link). The Carry Initiate pulse is produced by a TP6 pulse during the execute 1 state of the TAD instruction.

The MB0 ⟶ AC signal is a positive pulse produced at 1C02R. This pulse triggers operation of a positive capacitor-diode gate at the clear input of each AC flip-flop. The capacitor-diode gates are enabled when the corresponding bit of the MB contains a binary 0. The MB0 ⟶ AC signal is produced by a TP4 pulse during the execute 1 state of the AND instruction.

The Complement AC signal is a standard negative pulse produced at terminal 1C03H. This pulse initiates operation of the pulse inverter that provides the direct complement input to each AC flip-flop. This signal is produced by a TP5 pulse during the fetch state of a CMA instruction as designated by an operate 1 instruction signal and bit 6 of the instruction being a 1.

The Right Rotate and Left Rotate signals are produced at terminals R and X of the 4606 module at location 1C03. These signals provide the initiating pulse for capacitor-diode gates at both the 1 and 0 inputs of each AC flip-flop to provide a jam transfer of information into the AC from either the next most significant or next least significant bit of the accumulator (or link). The Right Rotate signal is produced under either of the following conditions:

a. By a TP5 pulse during the fetch state of the RAR microinstruction, as designated by an operate 1 instruction signal and a binary 1 in bit 8.

b. By a TP1 pulse during T1 time of the cycle following the fetch state of the RTR microinstruction. These conditions provide the additional rotate command during a rotate two microinstruction and are designated by binary ones in bits 8 and 10 of an operate instruction designated as group 1 by the presence of a 0 in bit 3 of the IR.

The Left Rotate signal is produced under conditions similar to those described for the Right Rotate signal except that bit 8 is replaced by bit 9.

The Index AC signal is a positive pulse produced at terminal 1C05L of a 4127 Pulse Inverter module. This signal provides a direct pulse input to the complement terminal of the AC_{11} flip-flop. This signal is produced by a TP1 pulse during the cycle following the fetch state of an IAC microinstruction as determined by the presence of the operate instruction signal, the presence of a 0 in IR_3 to designate operate group 1, and the presence of a binary 1 in bit 11 of the instruction to signify the IAC microinstruction.

The AC Carry Enable signal is a complementary level produced by diode gating circuits. The primary purpose of this signal is to enable the capacitor-diode gate whose pulse inverted output complements each bit of the accumulator. This signal is produced under any of the following conditions:

a. From time state T4 to time state T2 during the execute 1 state of a TAD instruction. This gating assures that the capacitor-diode gates are enabled for at least 1 microsecond prior to being strobed by the TP6 pulse.

b. During time states T5 and T6 of the fetch state during execution of the IAC microinstruction. This gating assures that the capacitor-diode gates are enabled for at least 1 microsecond prior to being strobed by the TP1 pulse.

c. During the program count or break state of a TAD instruction, and not during a rotate or IOT instruction, and not following the operation of either the EXAMINE or DEPOSIT key. This gating assures that the AC Carry Enable

signal is present during the cycle following execution of the TAD instruction (program count or break follow the execute 1) to allow the AC Carry pulse to ripple through the accumulator. This gating also inhibits generation of the AC Carry Enable signal during any rotate microinstruction (as determined by bit 10 of the instruction being a 0) to assure that carry pulses are not introduced into the accumulator during the second rotation, during any IOT pulse to prevent any interference with the accumulator during the ADC microinstruction, and during manual operations involving the EXAMINE or DEPOSIT keys which must clear the accumulator.

MEMORY ADDRESS REGISTER (9)

The memory address register (MA) determines the core memory address currently selected for reading or writing. The register is shown at the top of both sheets of engineering drawing 9 to consist of 1 flip-flop and associated gating from each of the 12 4206 Triple Flip-Flop modules at locations 1B02 through 1B13. Since the register contains 12 bits, it can directly address 4096 words of core memory. The register can be set or cleared by gated signals, can be complemented by gated signals, can be cleared directly, can be disabled, and the status of each flip-flop in the register is visually denoted by an indicator on the operator console. All gating inputs are accomplished through positive capacitor-diode gates which require 1-microsecond setup time.

The gating circuits allow the MA flip-flops to be set to correspond with binary ones in the switch register when the SR $\dashv\!\blacktriangleright$ MA signal is produced, allow the content of corresponding bits of the memory buffer register to be jam transferred into the MA by means of an MB $\dashv\!\blacktriangleright$ MA signal, and allow signals supplied to terminals 26 through 37 of interface connector 1J03 to be jam transferred into the MA by a Data Address $\dashv\!\blacktriangleright$ MA signal. The MA can operate as a binary counter when the MA Carry Enable signal is present at the capacitor-diode gate connected to the complement input of each flip-flop, thus allowing each flip-flop to be complemented on the positive shift produced as the next least significant flip-flop changes from the 1 to the 0 state. The input to the complement capacitor-diode gate of the least significant bit is provided by the Count MA signal. The Clear MA signal is supplied in parallel to the direct clear input of each flip-flop bit. The MA can be disabled (forced to indicate that all

flip-flops are in the 0 status without affecting the contents of the register) by the standard DEC ground-level Disable MA signal. The MA is disabled to select address 0000 when reading or writing the program count.

MEMORY BUFFER REGISTER (9)

The memory buffer register (MB) serves as a data buffer between the flip-flop logic of the processor and core memory. The MB consists of 1 flip-flop and associated gating from each of the 12 4206 Triple Flip-Flop modules at locations 1B02 through 1B13, and is shown in the center of both sheets of engineering drawing 9. Circuit operation of the MB is identical to that of the MA except that the MB cannot be disabled, is provided with an additional set of capacitor-diode gates for jam transfer inputs, and is provided with a direct set-to-1 input from the sense amplifiers.

Each flip-flop of the MB is cleared by the Clear MB signal supplied to the direct input and is set by a positive pulse supplied to the gated set-to-1 input from the corresponding bit of the sense amplifier when data is being read from core memory. The gating circuits allow the MB flip-flops to be set to correspond with binary 1 signals supplied to terminals 13 through 24 of data break interface connector 1J03, the transfer being initiated by the presence of the Data ⟶ MB signal. Jam transfers into MB flip-flops are accomplished by capacitor-diode gates enabled from corresponding bits of the accumulator and initiated by the AC ⟶| MB signal or enabled from corresponding bits of the memory address register and initiated by the MA ⟶| MB signal. Another pair of positive capacitor-diode gates is provided for jam transfers into each flip-flop of the MB and is used with the Type 137 Analog-to-Digital Converter. These gates allow a binary 1 to be set into MB_0 during the start of a conversion and permit this 1 to be shifted to the right through the MB until the conversion has been made to the desired accuracy. During the first approximation, the A-D Start signal from the converter is supplied to enable the level input of these capacitor-diode gates of flip-flop MB_0, and the enabling input to the capacitor-diode gates of successive MB flip-flops is provided by the 1 output of the next most significant flip-flop of the MB. These gates are initiated to perform the jam transfer by the MB Shift pulse which is also supplied from the Type 137 converter.

The complement capacitor-diode gate functions in the same manner as the corresponding circuit of the MA to allow the MB to be used as a binary counter when the MB Carry Enable

signal is provided. These capacitor-diode gates for flip-flops MB_{0-9} are initiated directly when the next least significant flip-flop changes from the 1 to the 0 state. Complementing of the two least significant bits of the MB is controlled by gating circuits shown at the right of sheet 2 of engineering drawing 9. This gating initiates the complement capacitor-diode gate of MB_{11} when the skip flip-flop is in the 0 state or when a positive pulse is supplied to 1J03-38 from an external device, thus incrementing the content of the MB by one. If MB_{11} changes from the 1 to the 0 state when complemented, this change initiates pulse inverter XYZ of the module at location 1C05 to propagate the carry pulse that complements flip-flop MB_{10}. The complement capacitor-diode gate of MB_{10} is also triggered by a count MB pulse when the skip flip-flop is in the 1 state, thus incrementing the content of the MB by two.

Terminal K of each MB flip-flop is supplied to terminals 1 through 12 of the data break interface connector 1J03 through the output bus drivers (shown on engineering drawing 31) for use by peripheral equipment. Terminal L of each MB flip-flop is routed to an indicator driver on the operator console. The L terminals of MB bits 3 through 8 are also supplied to terminals 27 through 38 of interface connectors 1J01 and 1J02 via the output bus drivers. These signals allow complementary outputs of MB_{3-8} to be used by device selectors in all peripheral equipment.

ACCUMULATOR (9)

The accumulator (AC) is the major arithmetic register and input-output register of the PDP-5. The AC is shown on the bottom portion of both sheets of engineering drawing 9 to consist of one flip-flop and associated gating from each of the 12 4206 Triple Flip-Flop modules at locations 1B02 through 1B13. The accumulator can be cleared directly, complemented through a variety of gating, and cleared and set through jam-transfer gating circuits under the control of signals generated by the accumulator control element. The accumulator can also be cleared and set by means of gating circuits which provide a jam transfer under the control of signals received from the Type 137 Analog-to-Digital Converter, and can be set directly by pulses received from the input mixer as a result of data supplied by peripheral equipment.

Complementation of a flip-flop occurs when a positive pulse is applied to the direct-complement terminal from either the complement capacitor-diode gate or from the pulse inverter shown above the indicator connector for the accumulator on engineering drawing 9. During T5 of

the CMA microinstruction, the Complement Accumulator signal is produced as a negative pulse which is applied to this pulse inverter, causing complementation of the associated AC flip-flop. During the TAD instruction, the AC flip-flop can be complemented in each of the following three stages:

a. If the corresponding bit of the MB is a 1, the complement capacitor-diode gate is enabled during T4 and is triggered by the Half Add signal.

b. If an AC bit contains a 0 and an MB bit contains a 1 following the half add operation, carry pulses for the half add are produced by one of the negative capacitor-diode gate that precede the pulse inverter. This gate is triggered during T6 by the Carry Initiate pulse, and the pulse inverter is initiated to produce the AC Carry pulse supplied to the complement input of the next most significant AC flip-flop.

c. The second negative capacitor-diode gate preceding the pulse inverter is enabled between time states T4 and T1 and is initiated when any AC bit changes from the 1 to the 0 state, thus initiating operation of the pulse inverter to complement the next most significant AC flip-flop.

The set and clear operations of each AC flip-flop are performed very simply. A flip-flop is cleared when the positive Clear AC signal is supplied to its direct-clear input, this signal being produced by the accumulator control element as a function of the CLA instruction, pulses supplied by peripheral equipment, or by various control states within the computer. Positive pulses supplied to the gated set input of each flip-flop from the input mixer effectively transfer information into the accumulator from signals supplied by peripheral equipment to terminals 17 through 24 of interface connector 1J01. During an AND instruction, the MB0 ⟶ AC signal is produced to initiate operation of the positive capacitor-diode gate enabled by the 0 status of the corresponding MB flip-flop, thus transferring zeros into the AC flip-flop if the corresponding bit of the core memory word held in the MB is a binary 0. Other gates to the input of the AC flip-flops provide a jam transfer of information from the next higher significant AC flip-flop bit during rotate right commands and from the next lower significant AC flip-flop bit during rotate left commands. Still other gates to the input of the AC flip-flops allow an AC flip-flop to be cleared when the next higher significant MB flip-flop

bit contains a 1 or allow it to be cleared when the corresponding MB flip-flop contains a 1 when the Comparator signal is present. The Comparator signal and the A-D convert signal that effect this gating are produced by the Type 137 converter.

Output signals from terminal F of each accumulator flip-flop are supplied to indicator drivers on the operator console and to the ladder network of the Type 137 converter. Outputs from terminal E of each flip-flop are supplied to the output bus drivers for application to terminals 1 through 12 of interface connectors 1J01 and 1J02 for transfers to peripheral equipment.

LINK (9)

The link (L) is a 1-bit register used to extend the arithmetic capabilities of the accumulator by serving as a carry or overflow register. The link is shown at the lower left corner of sheet 1 of engineering drawing 9 to be one flip-flop of the 4215 4-Bit Flip-Flop at location 1D01 and associated gating circuits.

The link is cleared by a standard DEC positive pulse applied to the direct input from terminal 1D24Z. A pulse occurs at this terminal during SP3 of an operation initiated by pressing the START key or during T4 of the fetch state of the CLL microinstruction (as indicated by the negative NOR gate conditioned by TP4, MB_5^1, and the OP1 signals). The link is complemented by supplying a positive pulse to both gated-set and gated-clear inputs to the flip-flop from positive capacitor-diode gates on the module at location 1E01. Gates MN and YZ of this module are enabled by the condition of bit 7 of an instruction during T5 of a CML microinstruction (as designated by the negative NAND gate on module 1D02 which is conditioned by the TP5 pulse and the OP1 instruction signal). The three remaining pairs of capacitor-diode gates serve to control the link in the same manner as corresponding capacitor-diode gates function in the accumulator during the execution of rotate commands and the TAD instruction. The binary status of the link flip-flop is indicated visually on the operator console.

OUTPUT BUS DRIVERS (31)

Accumulator output signals, memory buffer register output signals, the Break signal, and the Run^1 signal supplied to peripheral equipment connected to the interface connectors can be power amplified by 1684 Bus Driver modules at locations 1F09 through 1F13 and by 1685 Bus

Driver modules at locations 1F06 through 1F08. Wiring from the origin of these signals is brought to module terminal connectors which correspond to the input terminals of the bus driver modules, and wiring is run to the interface connectors from terminals at these locations which correspond to module outputs. Normally module locations 1F06 through 1F13 contain dummy plugs which jumper terminals corresponding to bus driver module input and output terminals, thus completing the path of these signals from their origin to the interface connectors. When additional connections to these signals would overload the logic circuits producing them, the dummy plugs are removed and replaced by bus driver modules. Signal flow to the bus drivers and from the bus drivers to the interface connectors is shown on engineering drawing 31.

INPUT MIXER (14)

The input mixer (IM) expands the input capabilities of the accumulator to allow information to be set into the accumulator from the switch register or from interface connectors 1J01 and 1J02. The IM is shown on engineering drawing 14 to consist of six 4130 Positive Capacitor-Diode Gate modules at locations 1E10 through 1E15 and a 1000 Clamped Load Resistor module at location 1E16. Two sets of capacitor-diode gates are used for each bit of the IM. The first is enabled when the corresponding bit of the shift register is in the (up) position corresponding to a binary 1, thus supplying ground potential to the resistor level input. The capacitor-diode gates enabled in this manner are triggered by the SR ⟶ AC signal produced by the accumulator control element during SP3 following operation of the DEPOSIT key, or during T5 of the fetch state of the OSR instruction. The second capacitor-diode gate for each bit of the IM is permanently enabled by connection to system ground. The capacitor pulse input for each of these gates is supplied from a separate terminal of the interface connectors. Each signal input line from the interface connector is clamped at -3 volts by a separate circuit of the clamped load resistor module. Bus connections from each of these terminals to various peripheral equipment require that gating in each device be used to supply positive DEC standard pulses to the input mixer to set the accumulator at the proper time.

SKIP CONTROL (8)

The skip control element provides a means of skipping an instruction as a function of the performance of group 2 operate microinstructions or IOT microinstructions. During the program

count state of every instruction, the address for the preceding instruction is read from address 0000 of core memory and placed in the memory buffer register. The contents of the memory buffer register is then used to determine the address of the current instruction. Since the word read from core memory is the address of the previous instruction, the content of the memory buffer register is normally incremented by one; however, the skip control can cause the content of the memory buffer register to be incremented by two to "skip" over an instruction by advancing the program count past it. The skip control logic circuits consist of a skip flip-flop shown in the upper right hand corner of engineering drawing 8 and various gating circuits shown directly beneath the flip-flop and in the lower left hand corner of the same engineering drawing.

The skip status is established during a fetch state by clearing the skip flip-flop and complementing it as a function of the instruction being performed and the contents of the accumulator and/or the link. The skip condition is then sensed during a program count state by gating circuits at the input of flip-flop MB_{10} and MB_{11} shown at the right center portion of sheet 2 of engineering drawing 9. This sensing increments the content of the MB by one to establish the normal program count if the skip flip-flop is in the 0 status and increments the content of the MB by two if the skip flip-flop is in the 1 status. Incrementing by one is performed by supplying a positive pulse to the complement capacitor-diode gate of flip-flop MB_{11}, and incrementing by two is accomplished by supplying a positive initiating pulse to the complement capacitor-diode gate at the input of flip-flop MB_{10}. The MB carry chain from MB_{11} to MB_{10} is propagated through the 4127 Pulse Inverter module at location 1C05 which triggers the complement capacitor-diode gate at the input of MB_{10} when MB_{11} changes from the binary 1 to the binary 0 state.

The skip condition is reset at the start of each fetch cycle by negative NAND gate JKL of the 4113 module at location 1D02 which produces a positive pulse supplied to the direct-clear input of the skip flip-flop. The skip condition is then established by complementing the skip flip-flop one or two times as a function of the instruction being performed and the state of the accumulator, link, and/or peripheral equipment flags. A positive pulse is supplied to terminal 1D03E to complement the skip flip-flop under each of the following conditions:

a. In the execute 1 state of an ISZ instruction when the MB Carry Enable signal is present if flip-flop MB_0 changes from the binary 1 to the binary 0 state, indicating that the increment pulse applied to MB_{11} during this instruction initiated a carry through each stage of the MB, leaving each bit in the 0 state.

b. By a TP4 pulse during the fetch state of an operate 2 instruction ($IRB_3^1 \cdot OPR \cdot F = OP2$) and AC_0 holds a 1, and MB_5 contains a 1 to designate performance of an SMA microinstruction.

c. By an SP4 pulse of an operate 2 instruction in which each bit of the accumulator contains a binary 0 and MB_6 contains a 1 to designate performance of an SZA microinstruction.

d. By a TP4 pulse during an operate 2 instruction in which the link is in the 1 state and a binary 1 is contained in MB_7 to designate execution of an SNL microinstruction.

3. By a TP5 pulse of an operate 2 instruction in which MB_8 of the instruction contains a 1 to signify the reverse sensing of the skip condition. For example to skip on 0 link, if the link contains a 1 the skip flip-flop is complemented during T4 and is complemented again during T5 to indicate the skip conditions were not fulfilled. If the link contains a 0, the skip flip-flop is not complemented during T4 and is complemented during T5, so that skipping takes place.

f. By an IOT 6031 pulse (which occurs during T4 of the fetch state of microinstruction KSF) when the keyboard flag of the Teletype unit is in the 1 state.

g. By an IOT 6041 pulse (which occurs during T4 of the fetch state of the TSF microinstruction) when the teleprinter flag of the Teletype unit is in the 1 state.

h. When a standard DEC positive pulse grounds terminal 25 of interface connector 1J01 from the skip gates of peripheral equipment (skip gates in peripheral equipment contain logic gating similar to that connected directly to the complement input of the skip flip-flop).

IOP PULSE GENERATOR (6)

During the fetch state of an IOT instruction, standard DEC negative IOP pulses are generated as a function of the contents of bits 9, 10, and 11 of the instruction. These IOP pulses are supplied to terminals 40, 42, and 44 of the interface connectors 1J01 and 1J02 for distribution to the device selector of each peripheral equipment. Gating of these pulses in selected peripheral equipment generates the IOT pulses which initiate operations within the peripheral equipment and perform operations such as strobing data into the accumulator, initiating I/O Halt or Skip pulses, etc. within the computer. Generation of the IOP 1, 2, and 4 pulses is performed by the circuits indicated in the lower right portion of engineering drawing 6.

Each of the IOP pulses is produced by a pulse amplifier circuit of the module at location 1D25. Each pulse amplifier is triggered by gating circuits which are similar except for the bit of the memory buffer which is sensed and the time state pulse which triggers operation of the circuit. Pulse IOP1 is produced by a TP4 pulse during the fetch state of an IOT instruction in which bit 11 contains a 1. Pulse IOP2 is produced by a TP5 pulse during the fetch state of an IOT instruction in which bit 10 is a 1. Pulse IOP4 is produced by a TP6 pulse during the fetch state of an IOT instruction in which bit 9 is a 1. The output from each pulse amplifier is applied to adjacent terminals of the interface connector by means of a twisted pair of wires, the pulse output being connected to the higher numbered terminal and the ground connection being made to the lower numbered terminal. These pulses are also wired directly to the device selector within the standard PDP-5 which serves the Type 137 Analog-to-Digital Converter and the program interrupt synchronization logic. This device selector is shown on engineering drawing 8 as the 4605 Pulse Amplifier module at location 1F18 and is typical of device selectors in peripheral equipment.

PROGRAM INTERRUPT SYNCHRONIZATION (8)

Control of the computer program sequence, when a Program Interrupt signal is supplied to terminal 26 of interface connector 1J01, is exercised by the logic circuits shown in the lower right portion of engineering drawing 8. The program interrupt synchronization element determines if the computer program can be interrupted by signals from peripheral equipment and, when in the interrupt enable condition, initiates the program interrupt at the conclusion of the instruction currently being executed. Program interrupt is similar to a JMS instruction to store the program count at address 0001 and transfer program control to the instruction stored at address 0002.

The program interrupt synchronization element consists of three flip-flops of the 4215 4-Bit Counter at location 1D03 and appropriate diode and pulse inverter gating circuits. These three flip-flops, designated INT. ENABLE (interrupt enable), INT. DELAY (interrupt delay), and INT. ACK (interrupt acknowledge) perform the three functions accomplished by this logic element. The interrupt enable flip-flop enables or disables entry into the program interrupt condition by controlling an input to gating circuits of the interrupt delay flip-flop. The interrupt delay flip-flop enables program interrupt operations to occur only after completion of any instruction (following the ION which sets the interrupt enable flip-flop) by controlling a signal input to gating circuits of the interrupt acknowledge flip-flop. The interrupt acknowledge flip-flop initiates program interrupt operations when enabled to do so by the interrupt delay flip-flop and the presence of a Program Interrupt signal supplied by an external device.

Both the interrupt enable and interrupt delay flip-flops are cleared by a positive pulse supplied to the direct-clear input from terminal V of the 3-input negative NOR gate at location 1D04. These flip-flops are cleared under any of the following conditions:

a. During SP3 following operation of either the START, EXAMINE, or DEPOSIT key.

b. By the IOT 6002 pulse which occurs during T5 of the fetch state of the IOF microinstruction.

c. When the interrupt acknowledge flip-flop changes to the 1 state.

Execution of an ION microinstruction is the only method of enabling program interrupt operation. During T4 of the fetch state of the ION microinstruction, an IOT 6001 pulse sets the interrupt enable flip-flop.

The interrupt delay flip-flop is set by a 3-input negative NAND gate during T3 of a fetch state when the interrupt enable flip-flop is set.

The interrupt acknowledge flip-flop is cleared by a positive pulse generated by the control circuits for the instruction register during SP1 following operation of either the START, EXAMINE, or DEPOSIT key. This pulse is supplied to the direct-clear input of the flip-flop and is designated the 0 ⟶ Int Ack signal. This flip-flop is also cleared during T6 of an execute 2 instruction, indicating the conclusion of the JMS instruction forced by the program interrupt. The flip-flop is set by a positive pulse supplied from terminal R of the 4115 Negative NAND Gate at location 1D05. This gate sets the flip-flop during T5 of the program count state when the interrupt delay flip-flop is in the 1 state and a Program Interrupt signal is produced by an I/O device. This timing allows the Int Ack signal to be supplied to the instruction register to allow IR_0 to be set during T3 of the following fetch cycle, thus forcing a JMS instruction. When set, the interrupt acknowledge flip-flop also causes the memory address register control element to generate the Clear MA_{5-11} signal, the Clear MA_{0-4} signal, the MA Carry Enable signal, and the Count MA signal. In this manner the address contained in the MA is set to address 0001 to store the current program count. After the program count has been stored, the content of the memory buffer register is incremented by one so that the next instruction is taken from core memory address 0002. The instruction stored in address 0002 is usually a JMP which transfers program control to a subroutine which services the interrupt. Exit from this subroutine is then accomplished by an ION microinstruction to allow additional program interrupts and a JMP I 0001 instruction to return program control to the conditions which existed prior to the interrupt.

TYPE 153 AUTOMATIC MULTIPLY AND DIVIDE OPTION

This standard option for the PDP-5 consits of two module mounting panels of circuits capable of performing parallel multiplication of 12-bit numbers and parallel division of a 24-bit dividend by a 12-bit divisor. Arithmetic operations are performed on positive binary numbers by this option approximately 18 times faster than by computer subroutine, as described in computer

option bulletin F-53(153). Circuits of this option are shown on engineering drawings BS-D-153-0-5, 6, and 7 and their operation is indicated on flow diagram FD-D-153-0-11. The following explanation of these circuits describes the functional components and conditions for control signal generation, then explains the logical operations involved in multiplication and division.

The algorithm for multiplication is simply shift right and add. Multiplication begins with the multiplicand in the accumulator, the multiplier in a multiplier quotient register, and a cleared arithmetic register and arithmetic register link. The least significant bit of the multiplier is sampled, and if it contains a 1, the multiplicand is added to the partial product contained in the arithmetic register. If the least significant bit of the multiplier contains a 0, the addition is not performed since any number multiplied by 0 equals 0. Then the contents of the arithmetic register and the multiplier quotient register are shifted together one position to the right; therefore, one bit of the product is shifted into the multiplier quotient register, and the bit of the multiplier just used is lost. The following example illustrates this operation performed on 4-bit numbers for the probelm: 15 x 5.

	1111		Start with multiplicand in AC, multiplier in MQ, and with AR and AR link cleared.
0	0000	0101	
	1111		Since $MQ_{11} = 1$, add. After the addition shift ARL, AR, MQ right one position.
0	0000	0101	
0	1111	0101	
	1111		After the shift $MQ_{11} = 0$, so do not add, just shift.
0	0111	1010	
	1111		After the shift $MQ_{11} = 1$, so add, then shift.
0	0011	1101	
1	0010	1101	
	1111		After the shift $MQ_{11} = 0$, so do not add, just shift.
0	1001	0110	

	1111		After the shift the most significant half of the product is contained in the AR, and the least significant half of the product is contained in the MQ.
0	0100	1011	

This operation is analogous to solving the problem by hand as follows:

```
  1 1 1 1      multiplicand in AC
x 0 1 0 1      multiplier in MQ
---------
  1 1 1 1
0 0 0 0
1 1 1 1
0 0 0 0
---------------
0 1 0 0 1 0 1 1 = 75
AR      MQ
```

The algorithm for division is subtract and rotate left. Division begins with the divisor in the accumulator, the most significant half of the dividend in the arithmetic register, and the least significant half of the dividend in the multiplier quotient register. The most significant portion of the dividend is then subtracted from the divisor. If the result is a positive number, a 1 is placed in the quotient; if the result is a negative number, a 0 is placed in the quotient. If the result of the first subtraction is a positive number, divide overflow occurs to stop the operation and to allow rescaling of either argument. If the result of the subtraction is a positive number in any cycle but the first one, the dividend is rotated left one binary place with respect to the divisor, and the operation continues with another subtraction. In some binary division hardware, a subtraction which results in a negative number is followed by an addition to restore the dividend; the dividend is rotated left one binary place, and the subtraction is repeated to determine the next bit of the quotient. If the divisor is represented by A and the dividend is represented by B, each cycle of this operation is $A - B + B - 1/2B = A - 1/2B$. To simplify this operation the Type 153 option subtracts, does not add the divisor to the result of the subtraction, then adds 1/2 of the dividend to the quotient. Each cycle of this operation can be represented as $A - B + 1/2B = A - 1/2B$, which produces the same result. The following example illustrates this operation in a problem containing an 8-bit dividend and a 4-bit divisor, quotient, and remainder.

Problem: 85 ÷ 9 or 0101 0101 ÷ 1001

	1001		Begin with divisor in AC, least significant half of dividend in MQ, the complement of most significant half of dividend in AR, and a 1 in ARL.
1	1010	0101	
	1001		First cycle, so add divisor to most significant half of dividend.
1	1010	0101	
0	0011	0101	
	1001		First cycle, so complement the contents of AR and ARL.
1	1100	0101	
	1001		Rotate the contents of the ARL, AR, and MQ left so that the complement of the content of the ARL is set into the least significant bit of the MQ, which is MQ_{11}.
1	1000	1010	
	1001		MQ_{11} = 0 so do not complement, just add.
1	1000	1010	
0	0001	1010	
	1001		Rotate left as before.
0	0011	0101	
	1001		MQ_{11} = 1 so complement the contents of the AR and ARL, add the contents of the AC to the content of the AR, and recomplement the contents of the ARL and AR.
1	1100	0101	
0	0101	0101	
1	1010	0101	
	1001		Rotate left as before.
1	0100	1010	
	1001		MQ_{11} = 0 so do not complement, just add.
1	0100	1010	
1	1101	1010	

	1001		
1	1011	0100	Rotate left as before.
	1001		
1	1011	0100	Since $MQ_{11} = 0$, do not complement, just add.
0	0100	0100	
	1001		
0	0100	1001	Last cycle so rotate ARL and MQ, but do not rotate AR; ARL = 0 so halt. Quotient is now in MQ and remainder is in AR.

If the ARL = 1 after performing a number of cycles equal to the number of bits in the divisor +1, another half cycle of operation is performed to produce an accurate remainder by adding the divisor to the content of the AR.

Functional Components

The major functional components of this option are a 12-bit multiplier quotient register (MQ), a 12-bit arithmetic register (AR), and a 1-bit register, designated the arithmetic register link (ARL), which serves as an overflow for the AR. Other elements of the option count the operations performed by these arithmetic registers, produce the timing pulses required for sequential operation from a variable-cycle timing generator, produce all of the necessary control signals, and select the option as a function of the instruction being performed in the same manner as an I/O device is activated.

The option is assumed to be located in module mounting panel positions 1K and 1L within the PDP-5 cabinet. An operator console containing indicators for the three major arithmetic elements of the option is substituted for the normal PDP-5 operator console with addition of the Type 153 option to the system. All interface connections to the Type 153 are made to connectors 1L01 and 1L02, whose terminals are bussed together to provide connection compatibility with computer interface connectors 1J01 and 1J02.

Device Selector

The Type 153 circuits require nine programmed command pulses, and so use three 4605 Pulse Amplifier modules. These modules are shown on the lower left portion of engineering drawing BS-D-153-0-5 at module locations 1L10, 1L11, and 1L12, these modules are activated by IOT select codes of 10, 11, and 12 respectively.

Time Generator

The timing of all operations performed by the Type 153 option (as mentioned in this text) is controlled by a 3-bit shift register shown at the upper right portion of engineering drawing BS-D-153-0-5. The 1 mc Clock signal produced by the timing signal generator of the processor is regenerated by pulse amplifier WXYZ of the 4606 module at location 1L17, synchronizing operation of the option with the processor. This regenerated negative pulse is inverted and used to drive the positive capacitor-diode gates at both the clear and set inputs of each flip-flop of the shift register. These flip-flops are designated TG_0, TG_1, and TG_2 from the least significant to the most significant. In operation a binary 1 is shifted through the register, and reset of the register is controlled by gating circuits that enable the capacitor-diode gates at the input of flip-flop TG_0. This gating allows the shift register to cycle every 4 or 6 microseconds. The time generator cycles every 6 microseconds unless the control flip-flop is in the multiply state, or unless MQ_{11} contains a 0, the step counter does not contain a 0, and the control flip-flop is in the divide state. Division of binary numbers involves subtraction which is performed by complementing one argument, adding the two numbers, then recomplementing the result. This action requires 6 microseconds per cycle. When the result of the previous divide cycle leaves a negative remainder (MQ^0_{11}), the complementation is omitted and the cycle is performed in 4 microseconds. Multiplication of binary numbers involves addition, so each cycle is 4 microseconds long.

This dual cycle time of the time generator is indicated on the timing diagram shown at the right side of engineering drawing BS-D-153-0-5 and is accomplished by gating circuits at the input to TG_0. When 6-microsecond operation is indicated [$\overline{\text{Multiply}} \cdot (\text{SCD-0} + MQ^1_{11})$] terminals 1L18N and 1L18X are at -3 volts, enabling the capacitor-diode gate at the clear input of TG_0 when TG_2 contains a 1, and enabling the capacitor-diode gate at the set input of TG_0 when TG_2 contains a 0. When 4-microsecond operation is indicated [$\text{Multiply} + (\overline{\text{SCD-0}} \cdot MQ^0_{11})$],

terminals 1L23Y and 1L23U are at -3 volts, enabling the capacitor-diode gate at the clear input of TG_0 when TG_1 contains a 1, and enabling the capacitor-diode gate at the set input to TG_0 when TG_1 contains a 0.

The direct outputs from the flip-flops of the shift register provide enabling levels to gating circuits in the arithmetic unit control logic and initiate operation of the gated pulse amplifiers in the time generator that produce the timing pulses used to initiate information transfers or control signal generation. These timing pulses are designated with TGP numbers (Time Generator Pulse), are produced by the 4606 module at location 1L20, and are all standard negative pulses of 400 nanosecond duration. These pulse amplifiers are enabled in common by the negative Run^1 signal which conditions the 1-microsecond negative capacitor-diode gates at the input. These gates are triggered to produce the TGP pulses under the following conditions:

a. TGP_0^0 is produced when flip-flop TG_0 changes from the binary 1 to the binary 0 state.

b. TGP_1^0 is produced when flip-flop TG_1 changes from the binary 1 to the binary 0 state.

c. TGP_2^0 is produced when flip-flop TG_2 changes from the binary 1 to the binary 0 state and thus occurs only during divide operations.

Arithmetic Unit Control Logic

This logic element contains four flip-flops that determine or indicate control functions in the Type 153 option and signal generating circuits consisting of a flip-flop, diode gates, and pulse amplifiers. The four control flip-flops are shown in the upper left portion of engineering drawing BS-D-153-0-5, and the signal generating circuits are spread over the remainder of this drawing. The functions and conditions that control each of these flip-flops or control signals are described in the following text.

Control Flip-Flop - This device produces the complementary pair of Multiply (MUL) and complementary Divide (DIV) signals. The flip-flop is cleared by the Multiply Go signal when a MUL microinstruction (IOT 6111) is executed and is set when a DIV microinstruction (IOT 6121) is executed.

Run Flip-Flop - This device serves as a generator of the complementary Run^1 signals, and provides on/off control of the option in the same manner as the corresponding flip-flop controls operations in the PDP-5 processor. The negative Run^1 signal at terminal 1K25T is routed to the time generator to enable generation of the TGP pulses and to advance the state of the TG shift register. The ground-potential Run^1 signal at terminal 1K25U is supplied to the direct-clear input of each flip-flop of the step counter to initialize it when operation of this option begins. The run flip-flop is set to establish the operating mode of the option by the Control Clear signal supplied to the direct-set input. Note that the binary state of this flip-flop is opposite to that normally shown on DEC drawings in that the 1 state is indicated on the left and the 0 state is indicated on the right. The flip-flop is cleared to discontinue the operation of the option in any one of the following:

a. When divide overflow occurs, a pulse is applied to the complement input. This pulse is generated when the L & AR Complement signal occurs (during T4 and T6 of a 6-microsecond divide operation), the step counter contains 0, and the arithmetic register link is in the 1 state.

b. When power is being sequenced in the PDP-5, Power Clear pulses received from the processor are inverted and applied to the normal minus-on-1 output to prevent operation of this option until power has stabilized.

c. When a TGP_1^0 pulse occurs, the step counter contains 11, and the control flip-flop is in the multiply state.

d. When a TGP_1^0 pulse occurs, the step counter contains 12, the control flip-flop is in the divide state, and the arithmetic register link contains 0.

e. When flip-flop TG_2 changes from the 0 to the 1 state, the step counter contains 13, and the control flip-flop is in the divide state.

Busy Flag Flip-Flop - This device indicates to the computer program that the Type 153 option is or is not available for use. The condition of this flip-flop is sampled by the SAF microinstruction (IOT 6124) to produce a Skip signal when the flip-flop is in the binary 1 state, indicating that it is available for use in the program. This indication is given prematurely so that the minimum amount of time elapses between completion of an arithmetic operation by this option and use of the data obtained or reuse of the option. The time at which this flip-flop is set assures that operations in the Type 153 circuits will be completed by the time the program can sample the flag and execute any instruction to store the result or effect any transfers to or from the option. This flag is cleared by a direct-clear input of the Control Clear signal and is set by either of the following conditions:

a. When divide overflow occurs as indicated by conditions listed under entry (a) for clearing the run flip-flop.

b. When a TGP_1^0 pulse occurs, the step counter equals 8, and the control flip-flop is in the multiply condition.

c. When a TGP_1^0 pulse occurs, the step counter contains 11, and the control flip-flop is in the divide state.

Divide Overflow Flip-Flop - Divide overflow occurs when the divisor is a smaller number than the most significant portion of the dividend (contained in the AR). Under these conditions operation of the Type 153 option is stopped at the conclusion of the first cycle of operation and this flip-flop is set. The state of this flip-flop can be sampled by the SZO microinstruction (IOT 6114), allowing this condition to be sampled immediately following issuance of a DIV microinstruction. Therefore, program time is not wasted by allowing the entire divide operation to occur, and rescaling can be accomplished immediately. If a division were allowed to continue with a divisor of less magnitude than the dividend, a quotient of more than 12 bits would result which cannot be accommodate by the Type 153 option or by the PDP-5. The minus-on-0 output of the divide overflow flip-flop supplies one input to a 2-input negative NAND diode gate whose

second input is provided by the SZO microinstruction. The output of this gate provides one of the two possible conditions for generation of the Skip signal, supplied to the processor from the Type 153 option. Upon execution of either a MUL or DIV microinstruction this flip-flop is cleared by the Control Clear signal supplied to the direct-clear input. The flip-flop is set by the conditions specified under entry (a) for setting the run flip-flop. When divide overflow occurs, the run flip-flop is cleared to discontinue operation of the Type 153 option and the busy flag flip-flop is set to designate that operations of the option are completed.

Clear AR Signal - This standard DEC positive pulse is produced at terminal 1L15X by a pulse amplifier of the 4604 module shown at the right side of the engineering drawing. This pulse amplifier is triggered by the Register Clear pulse received from the device selector when a CAM (IOT 6101) command is given. The Clear AR pulse provides a direct-clear input to both the AR and the ARL.

Clear AC Signal - This positive pulse is produced by NOR combining the AC ⟶ MQ and the AC ⟶ AR signals produced by the device selector. The AC ⟶ MQ signal is produced during execution of an LMQ microinstruction (IOT 6102), and the AC ⟶ AR signal occurs during execution of a LAR microinstruction (IOT 6104).

Control Clear Signal - This signal is produced upon execution of either the DIV or MUL microinstruction to clear the Type 153 option control logic and time generator prior to the performance of any arithmetic operation. This standard DEC positive 400-nanosecond pulse is produced at terminal 1L15T by satisfying either of the input conditions required for operation of the appropriate pulse amplifier on the 4604 module. This signal sets the run flip-flop and clears the busy flag flip-flop, div overflow flip-flop, and all of the flip-flops of the time generator.

XOR Signal - This standard DEC negative pulse is generated at location 1L17H by one of the pulse amplifiers on the 4606 module shown at the top right portion of the engineering drawing. This signal is generated when TG_1 changes from the 0 to the 1 state, which occurs during T1 of a multiply operation in which the least significant bit of the multiplier (contained in the MQ) is a 1, or during T1 in every divide cycle. This signal is applied to the gating circuits at the input of the AR to initiate a half add operation between the content of the AR and the

input of a negative capacitor-diode gate at the clear input of the ARL and to the trigger input of the capacitor-diode gates at the clear and set input of each MQ flip-flop. Enabling of these capacitor-diode gates causes the ARL to be cleared, causes the least significant bit of the AR to be shifted into the most significant bit of the MQ, causes the content of bits MQ_{0-10} to be shifted to the next less significant bit, and causes the least significant bit of the MQ to be shifted out of the register and lost when the L & MQ Shift Right signal occurs.

AR Shift Right Signal - Parallel-connected inverters WX of the module at location 1K20 and KL of the module at location 1L14 provide the driving and signal inversion of the L & MQ Shift Right signal required to produce the positive AR Shift Right signal. This signal, occurring at T4, triggers the capacitor-diode gates at both the clear and set inputs to each AR flip-flop. These capacitor-diode gates for flip-flops AR_{1-11} are enabled by the condition of the next higher order flip-flop, and the input gates to AR_0 are conditioned by the content of the ARL. This signal, in conjunction with the L & MQ Shift Right signal, in binary multiplication provides the required basic right shift operation which is indicated in the lower block diagram in the Shift & Rotate Connections portion of the engineering flow diagram.

L & AR Complement Signal - This standard DEC negative pulse is produced at terminal 1L16H by a pulse amplifier of the 4606 module shown near the center of the engineering drawing. During a 6-microsecond divide cycle this pulse is produced at T4 by the negative capacitor-diode gate input and is produced at T6 by a direct ground-level pulse input. The capacitor-diode gate is enabled by the Divide signal and is triggered by the TGP^0_0 pulse; the direct input is supplied by a 2-input negative NAND diode gate which is enabled by the Divide signal and the TGP^0_2 pulse. This signal triggers permanently enabled negative capacitor-diode gates at the complement input of the AR and the ARL.

L & MQ Rotate Left Signal - This standard DEC negative pulse is produced at terminal 1L16P by a pulse amplifier of the 4606 module shown at the lower right portion of the engineering drawing. This pulse amplifier is initiated by the negative capacitor-diode gate input, which is enabled by the control flip-flop being in the divide state and is triggered by the TGP^0_1 pulse. Therefore, this pulse occurs at T5 of each divide cycle. This signal initiates operation of capacitor-diode gates in the ARL and in the MQ. The gates in the ARL are enabled by the most

content of the accumulator, and is also supplied to gating circuits to initiate generation of the Carry Enable signal. This timing is produced by the negative capacitor-diode gate at the input to the pulse amplifier which is enabled by a 2-input ground-level diode gate in turn enabled by the Divide signal or the MQ_{11}^{1} signal. This capacitor-diode gate is triggered when TG_0 changes from the 0 to the 1 state.

Carry Enable Signal - To perform a full add or full subtract operation the Carry Enable signal is produced during time states T1 and T2 in each cycle in which the XOR signal is generated. The Carry Enable signal is produced by a flip-flop composed of inverters UV, WX, and YZ of the 4102 module at location 1L14 and negative NAND diode gate RST of the 4113 module at location 1L18. This flip-flop is cleared by the Power Clear pulses received from the processor at T3 (when TG_2 is cleared). This flip-flop is set by the XOR signal and the 1 output is driven by two parallel-connected inverters to become the negative Carry Enable signal. This signal begins with the XOR signal (at T1) so that the negative capacitor-diode gates of the AR and the ARL are enabled to propagate a carry pulse for each flip-flop cleared by the Carry Initiate pulse at T2.

Carry Initiate Signal - This standard DEC negative pulse is produced at location 1L17P by a pulse amplifier of a 4606 module. This pulse is produced when the negative capacitor-diode gate input initiates the pulse amplifier. This capacitor-diode gate is enabled when the control flip-flop is in the divide mode or when MQ_{11} contains a 1 (the same circumstances condition the capacitor-diode gate that enables generation of the XOR signal) and is triggered when TG_1 changes from the 0 to the 1 state at T2. The Carry Initiate pulse triggers negative capacitor-diode gates at the input of the ARL and the AR to initiate the second exclusive OR operation between the content of the accumulator and the content of the AR and ARL to complete an add or subtract operation.

L & MQ Shift Right Signal - This standard DEC negative pulse is produced at location 1K20W by a pulse amplifier of the 4606 module shown in the lower right corner of the engineering drawing. This pulse amplifier is initiated by the negative capacitor-diode gate input, which is enabled when the control flip-flop is in the multiply state and is triggered by the TGP_1^0 pulse. Therefore, this signal is produced at T4 of each multiply operation and is supplied to the trigger

significant bit of the AR, the gates of MQ_{0-10} are enabled by the condition of the next less significant flip-flop bit of the MQ, and the gates of MQ_{11} are conditioned by the status of the ARL. Therefore, this signal provides a data rotation from the most significant bit of the AR into the ARL, from the ARL into the MQ, and through the MQ; then the most significant bit of the MQ is shifted out of the register and is lost. This operation is performed as the last cycle of a divide function and is shown on the Shift & Rotate Connections diagram on engineering flow diagram FD-D-153-0-11. During divide operations preceding the last cycle, the L & MQ Rotate Left signal and the AR Rotate Left signal collaborate to provide a complete loop of rotating data through the AR, from the most significant bit of the AR into the ARL, from the ARL into the least significant bit of the MQ, through the MQ, and from the most significant bit of the MQ into the least significant bit of the AR. This operation is indicated in the top diagram of the Shift & Rotate Connections diagram of the engineering flow diagram.

AR Rotate Left Signal - This standard DEC positive pulse is produced at terminal 1L25H by a pulse amplifier of the 4604 module shown at the right portion of the engineering drawing. This pulse amplifier is triggered by the output of the 4127 Pulse Inverter module at location 1L25Z. This pulse is produced during each divide cycle by the TGP_1^0 pulse except when the negative capacitor-diode gate is inhibited, which occurs during the last full divide cycle (the step counter contains 12) or when the control flip-flop is in the multiply state. The AR Rotate Left signal provides the initiating pulse for a positive capacitor-diode gate at both the set and clear inputs of each flip-flop of the AR. The capacitor-diode gates at the clear input of each flip-flop are enabled by the next less significant flip-flop being in the 0 status, and the gates at the set inputs are enabled by the next less significant flip-flop being in the 1 status. When these gates are triggered, the content of the AR is shifted one position to the left and the content of MQ_0 is shifted into AR_{11}, providing one of the basic operations required for binary division.

Step Counter

Each divide or multiply operation performed by the Type 153 option is counted by a 4-stage flip-flop counter. As shown on the lower portion of the engineering drawing, this counter consists of a 4215 Four-Bit Counter module at location 1L22 and negative NAND diode gates that decode the flip-flop outputs of a 4115 Positive Diode NOR module at location 1L22. The counter is cleared by the positive shift of the ground-level Run^1 signal and is advanced (at T4

of a 4-microsecond cycle or at T5 of a 6-microsecond cycle) when flip-flop TG_1 is cleared. When the step counter is cleared, the decoding circuits produce the SCD-0 signal which provides one of the conditions for setting the divide overflow flip-flop. When the step counter reaches the count of 12, the decoding circuits produce the ground-level SCD-12 signal used by the gating circuits which clear the run flip-flop to determine that the arithmetic operations are completed during division. The SCD-12 signal also inhibits generation of the AR Rotate Left signal after 12 operations have occurred.

Multiplier Quotient Register

The multiplier quotient register (MQ) is one of the two major 12-bit arithmetic registers and is shown logically on engineering drawing BS-D-153-0-6. The arithmetic operations performed by this register are those of shifting right, rotating left, and transferring information to or from the accumulator. The MQ holds the multiplier at the beginning of a multiplication operation and holds the least significant half of the product at the conclusion. It holds the least significant half of the dividend at the start of a divide operation and at the end holds the quotient. The following functions are performed by the MQ:

a. The MQ is cleared by the Register Clear signal supplied to the direct-clear input to each flip-flop. This signal is produced by the device selector upon execution of a CAM microinstruction (IOT 6101).

b. The MQ can be loaded from the content of the accumulator by a binary-ones transfer. A capacitor-diode gate at the set input of each MQ flip-flop is enabled by the binary 1 state of each flip-flop of the accumulator and is initiated by the AC$\longrightarrow$MQ signal. The AC$\longrightarrow$MQ signal is produced by the device selector upon execution of an LMQ microinstruction (IOT 6102).

c. The content of the MQ can be shifted right, with the content of the ARL shifted into the most significant bit of the MQ. This operation

is accomplished by positive capacitor-diode gates that effect a jam transfer of information when triggered by the L & MQ Shift Right signal during multiply operations.

d. The content of the MQ can be rotated left, with the content of the ARL shifted into the least significant bit of the MQ, during divide operations. This rotation is accomplished by positive capacitor-diode gates that effect a jam transfer of information when initiated by the L & MQ Rotate Left signal.

e. The content of the MQ can be sampled and transferred into the accumulator by execution of a RDM microinstruction (IOT 6122). This microinstruction causes the device selector to generate the MQ⟶AC pulse which is supplied in common to one input of a 2-input negative NAND diode gate for each MQ flip-flop. The second input to each gate is supplied by the minus-on-1 output from the appropriate MQ flip-flop. Therefore, when the MQ⟶AC pulse is produced, positive pulses are supplied to the processor input mixer for bits of the MQ containing a binary 1, therefore transferring ones into the accumulator.

f. The content of the MQ is visually indicated by lamps on the operator console.

Arithmetic Register

The arithmetic register (AR) is the major processing register or accumulator of the option. This 12-bit flip-flop register is shown on engineering drawing BS-D-153-0-7. During multiplication, the content of the AR is cleared automatically at the beginning, and holds the most significant half of the product at the conclusion. During division the AR holds the most significant half of the dividend at the beginning and holds the remainder at the conclusion. This register can be shifted right or left, can be loaded and unloaded from the content of the accumulator, can be complemented, and can perform binary addition with the content of the accumulator. Specifically, the AR can perform the following tasks:

a. The AR can be cleared by receipt of the Clear AR signal which is supplied to the direct-clear input of each flip-flop. The Clear AR signal is produced by a pulse amplifier triggered by the Register Clear pulse. The Register Clear pulse is produced by the device selector during execution of a CAM microinstruction (IOT 6101).

b. The AR can be loaded from the content of the accumulator by means of the AC ⟶ AR pulse. In this transfer the AR is set to the complement of the content of the accumulator, since the 0 condition of an AC flip-flop is used to enable a negative capacitor-diode gate of the corresponding AR flip-flop. This capacitor-diode gate complements the AR flip-flop after it has been cleared by the Clear AR pulse.

c. The content of the AR can be rotated left during each divide operation (except the last operation) by means of the AR Rotate Left pulse. In this transfer the content of MQ_0 is transferred into the content of AR_{11}.

d. The content of the AR can be shifted right during each multiply operation by means of the AR Shift Right pulse. During this operation the content of the ARL is transferred into the content of AR_0.

e. The half add operation can be performed between the content of the accumulator and the content of the AR with the result left in the AR. In this operation the output of each bit of the accumulator containing a 1 is used to enable a capacitor-diode gate which is triggered by the XOR signal to complement each AR flip-flop.

f. The second half of binary additions or subtractions, between the content of the accumulator and the content of the AR, is performed by capacitor-diode gates triggered by the Carry Initiate pulse. Carries are then propagated to trigger complementing of each next higher order flip-flop bit through capacitor-diode gates enabled by the Carry Enable signal.

g. The content of the AR can be complemented by means of the L & AR Complement pulse which is used during divide operations to perform subtraction. The pulse triggers permanently enabled capacitor-diode gates so that the content of each AR bit is complemented in preparation for being added to the content of the accumulator.

h. The content of the AR can be loaded into the accumulator by means of an AR⟶AC pulse. This pulse is produced by the device selector during execution of an RDA microinstruction (IOT 6112). This signal gates a 2-input negative NAND diode gate, as described in entry (e) for the MQ, to transfer the content of each bit of the AR into the input mixer.

i. The content of the AR is visually indicated on the operator console.

Arithmetic Register Link

The arithmetic register link (ARL) is a 1-bit extension of the AR and is shown on the left side of engineering drawing BS-D-153-0-7. The operations of the ARL are as follows:

a. The ARL is cleared by the Clear AR pulse applied to the direct-clear input in the same manner as this signal clears the AR.

b. The content of the ARL can be complemented by a pulse received from the AR when AR_0 is cleared if the Carry Enable signal is present.

c. The ARL can be loaded from the content of the AR_0 flip-flop by means of the L & MQ Rotate Left pulse which occurs during the left rotate operations involved in binary division.

d. The ARL can be cleared by the L & MQ Shift Right pulse applied to a permanently enabled capacitor-diode gate. This pulse occurs during multiply operations.

e. The ARL can set by receipt of the Divide Go pulse to clear the AR at the beginning of a divide operation. The Divide Go pulse is produced by the device selector upon execution of a DIV microinstruction (IOT 6121).

f. The content of the ARL can be complemented by receipt of the L & AR Complement pulse which triggers permanently enabled capacitor-diode gates. This complementation occurs during each divide cycle as one of the functions involved in binary subtraction.

g. A 1-bit half add operation is performed by the ARL as an extension of the carry initiate operation performed by the AR. In this operation the ARL is either set or cleared by the Carry Initiate pulse as a function of the content of both AR_0 and AC_0.

h. The content of the ARL is indicated on the operator console.

Logical Function

Logical operation of the Type 153 option is indicated on engineering flow diagram FD-D-153-0-11. Parallel binary multiplication and division are well documented in text books, and the reader is urged to refer to his choice of text for a thorough explanation of the digital principles involved in these operations.

Multiplication

Every multiply routine must contain the following instruction sequence, assuming that the multiplier is in the accumulator and the multiplicand is in core memory:

1. Clear the AR and MQ, then load the MQ with the multiplier using instruction 6103 which combines the CAM (IOT 6101) and LMQ (IOT 6102) microinstructions.

2. Load the AC with the multiplicand.

3. Give the multiply command (IOT 6111).

4. Enter a loop which continually checks the busy flag by means of the SAF microinstruction (IOT 6124) and jumps out of the loop when the flag is raised, indicating that the multiplication is completed.

5. Clear the accumulator in preparation for receiving the product.

6. Load the most significant half of the product into the AC from the AR, using the RDA microinstruction (IOT 6112). This portion of the product can be stored in core memory, and the accumulator can be cleared. The least significant 12-bits of the product can then be transferred into the AC from the MQ using the RDM microinstruction (IOT 6122).

The sequence of control signal generation and information flow caused by the preceding routine begins with the CAM command which clears the MQ directly and causes generation of the Clear AR signal that clears the AR and ARL. The LMQ command then transfers the content of the AC into the MQ and causes the control logic to generate a Clear AC pulse which is returned to the processor. When the MUL command is given, the control flip-flop is cleared to the multiply condition and a Control Clear pulse is generated to set the run flip-flop and to clear the busy flag, divide overflow flip-flop, and the time generator. When the run flip-flop is set, the step counter is cleared, and the time generator is enabled to start repeated 4-microsecond multiply cycles.

Multiplication is performed by adding the content of the accumulator (containing the multiplicand) to the content of the AR (which is cleared for the first operation and contains the most significant portion of the product at the end of the multiplication) and leaving the result in the AR. The contents of the AR and the MQ are then shifted by 0 equals 0, the addition is not performed if the least significant bit of the multiplier (contained in the MQ) is a binary 0. Therefore, for each cycle of multiplication the Type 153 circuits sample the content of MQ_{11} and perform a binary addition between the content of the AC and the content of the AR if this number is a 1, and inhibit the addition if this number is a 0. The contents of both the AR and MQ are shifted one position to the right and a step counter is incremented by one at the conclusion of each multiply operation. The step counter determines how many cycles of operation

are required to perform the multiplication and clears the run flip-flop when the multiplication is complete. The 12 most significant bits of the product are then contained in the AR, and the 12 least significant bits of the product are contained in the MQ. This data can be transferred to the accumulator and stored or manipulated as necessary under program control.

Each cycle of the multiply operation performs the following functions:

a. During T1 the XOR signal is generated if MQ_{11} contains a 1 to enact a half add operation between the content of the accumulator and the content of the AR.

b. During T2 a Carry Initiate signal is produced if MQ_{11} contains a 1 and the carry operation is performed to complete the addition between the content of the accumulator and the content of the AR.

c. During T3 the Carry Enable signal still exists; so carries from the carry initiate operations are rippled through the AR.

d. During T4 the L & MQ Shift Right signal and the AR Shift Right signal are produced to shift the contents of the ARL, AR, and MQ one position to the right so that a 0 is set into the ARL and the bit of the multiplier which was just used is shifted out of the MQ. The step counter is then advanced and the flag and run control circuits sample the content of the step counter. If the step counter contains an 8 (signifying that the multiply operation will be concluded in three more cycles or in 12 microseconds), the busy flag flip-flop is set. If the step counter contains 11 (signifying that 12 multiplication cycles have been performed), the run flip-flop is cleared, disabling the time generator and stopping operation of the Type 153 option. If the step counter does not equal 11, the next cycle of operation is entered.

Division

A divide routine should contain the following sequential steps, assuming that half of the dividend is in the accumulator and half is in core memory, and assuming that the divisor is in core memory:

1. Clear the AR and MQ, and load the content of the accumulator into the AR if it contains the 12 most significant bits of the dividend or load it into the MQ if it contains the 12 least significant bits of the dividend. This clearing and loading can be accomplished by one instruction which combines the CAM microinstruction (IOT 6101) and either the LAR (IOT 6104) or the LMQ (IOT 6102) command.

2. Load the remaining half of the dividend into the accumulator and transfer it to the AR if it is the most significant half of the dividend or into the MQ if it is the least significant half of the dividend.

3. Load the divisor into the accumulator.

4. Give the divide command (IOT 6121).

5. Check the divide overflow flag by using an SZO microinstruction (IOT 6114) followed by a jump to a subroutine which deals with divide overflow. This subroutine can cause the program to type out an error indication, rescale the divisor or the dividend, or perform other mathematical corrections and repeat the divide routine.

6. Enter a loop which continually checks the busy flag and jumps out of the loop when the flag is raised, indicating that the division is completed.

7. Clear the accumulator in preparation for receiving the quotient.

8. Load the quotient into the accumulator from the MQ using the RDM microinstruction (IOT 6122).

As in the multiply routine, the divide routine begins with the CAM command that clears the MQ directly and causes the AR and ARL to be cleared. The most significant 12 bits of the dividend are then transferred into the AR from the AC by the LAR command, and the 12 least significant bits of the dividend are transferred into the MQ from the AC by means of the LMQ command. Both of these commands cause the control logic to generate a Clear AC pulse which is returned to the processor. When the DIV command is given, the control flip-flop is set to the divide condition and the Control Clear pulse is generated to set the run flip-flop and to clear the busy flag, divide overflow flip-flop, and the time generator. When the run flip-flop is set, the step counter is cleared and the time generator is enabled to start repeated 6-microsecond divide operations.

Division is performed by subtracting the content of the accumulator (containing the divisor) from the content of the AR (which contains the most significant portion of the dividend) and leaving the result in the AR. The contents of the ARL, AR, and MQ are then rotated one position to the left so that the complement of the content of the ARL is shifted into the least significant bit of the MQ. Following the rotation the least significant bit of the MQ is sampled to determine if the rotation resulted in a negative remainder in the AR. If the remainder is negative, as indicated by MQ_{11} containing a 0, the binary addition between the content of the accumulator and the content of the AR is performed in 4 microseconds. This operation is indicated as the divide B path through the engineering flow diagram. In this flow, time states T3 and T6 are eliminated by advance of the time generator by means of gating circuits at the input of TG_0. These circuits sample the content of MQ_{11}. If MQ_{11} contains a 1, indicating that the remainder is a positive number, the divide A path is used in a 6-microsecond divide operation. In this operation subtraction is performed by complementing the content of the AR and adding the content of the AC to the complemented content of the AR. The step counter is incremented during each divide cycle to determine the number of divide cycles that must be performed to complete the division and to determine when the busy flag is to be set. When the arithmetic operations have been completed, the run flip-flop is cleared, the quotient is held in the MQ, and the remainder is held in the AR. These numbers can then be transferred to the accumulator for storage or manipulation or can be used for multiple precision division.

Each cycle of the divide operation performs the following functions:

a. During T1 the XOR signal is generated unconditionally and the Carry Enable signal is produced. At the beginning of a divide operation the SCD-0 output of the step counter decoder is sampled by the time generator gating circuits to force a 6-microsecond cycle for the first divide operation. In all subsequent cycles this same gating samples the content of MQ_{11} and enables a 6-microsecond cycle if the content of MQ_{11} is a 1 or forces a 4-microsecond cycle if MQ_{11} contains a 0. The half add operation is accomplished between the content of the accumulator and the content of the AR during T1. During a divide A cycle this half add exclusive OR function is also performed between the content of the AC and the complement of the previous content of the AR, since the content of the AR was complemented during T6 of the previous cycle. During a divide B cycle this exclusive OR function is performed directly between the content of the AR and the content of the AC since the AR contains a negative remainder that allows subtraction to be performed by binary addition (without complementing).

b. During T2 the Carry Initiate signal is produced unconditionally and the carry operation is performed to complete the binary addition between the content of the accumulator and the content of the AR.

c. During T3 the Carry Enable signal is asserted so that carries from the carry initiate operation are propagated through the registers during a divide A function. If the step counter contains 13 (signifying that 12 rotations have taken place), the run flip-flop is cleared, disabling the time generator and stopping operation of a Type 153 option.

d. During T4 of a divide A cycle the L & AR Complement signal is produced to complement the content of the ARL and AR. During a divide A cycle the step counter is also advanced at this time. During the first divide cycle the content of the ARL is sampled and if it contains a 1 the

divide overflow flip-flop is set, the busy flag is set, and the run flip-flop is cleared as an indication of divide overflow. In a divide B operation this time state does not exist since it is one of the two time states which are removed to reduce the 6-microsecond divide cycle to a 4-microsecond divide cycle.

e. During T5 the AR Rotate Left pulse is produced if the step counter has not yet reached a count of 12, and the L & MQ Rotate Left signal is produced. Therefore, during the first 12 divide cycles the most significant bit of the remainder (contained in AR_0) is shifted into the ARL, the complement of the content of the ARL is shifted into the least significant bit of the MQ to form a bit of the quotient, and the content of the MQ is rotated left so that the most significant bit is shifted into the least significant bit of the AR. When the step counter reaches a count of 12, the last full divide cycle is in progress; so the AR Rotate Left signal generation is inhibited to allow the rotation as mentioned previously, except that the most significant bit of the MQ is shifted out of MQ_0 and lost, and the content of the AR is not shifted. If the step counter contains 11 (signifying that 1 or 1-1/2 divide cycles remain to complete the computation) the busy flag flip-flop is set providing advance warning of from 8 to 16 microseconds. If the step counter contains 12 and the ARL contains a 0, the computation is completed and the run flip-flop is cleared.

f. During T6 the content of MQ_{11} is sampled to determine if the remainder is positive or negative. If MQ_{11} contains a 1 the remainder is positive, the L & AR Complement signal is produced to complement the content of the AR and the ARL in preparation for performance of a divide A operation during the succeeding cycle. If the content of MQ_{11} contains a 0, signifying the remainder is a negative number, generation of the L & AR Complement signal is inhibited, and this state is eliminated from the timing chain by advance of the time generator during the succeeding divide B cycle.

SECTION 3

CORE MEMORY

Local address and data storage and retrieval in the standard PDP-5 are performed by the core memory. The memory is a simple coincident-current ferrite-core array operated by currents originating in transistor power supplies and gating circuits. Input and output registers for core memory are located in the processor, and all signals which control functions of the memory are generated by the timing signal generator of the processor. These timing control signals are derived from the 1-megacycle crystal clock and the 6-microsecond TG counter of the timing signal generator, so all memory operations are synchronized with processor operations. The memory is continuously cycling, performing a read operation during time states T2 and T3, and a write function during time states T5 and T6 of each computer cycle. Time state T4 is used by the processor to modify data and addresses, when necessary, between retrieve and restore functions. Refer to Figure 2-1 and engineering drawing FD-D-5-0-2 for information concerning timing synchronization between the core memory and the processor. Also refer to Section 2 for an explanation of the time signal generator, the memory address register, and the memory buffer register for information concerning all circuit elements which interface with the core memory.

Logic circuits for the core memory are shown on engineering drawings 16 and 17, and the array and memory diode units are shown on engineering drawings 11 (for 4096-word storage) and 12 (for 1024-word capacity). The 4K memory is described in this section of the manual because it is far more common and since operation of a 1K storage is obvious if the operation of the 4K memory is understood. Briefly, the differences between the two storage sizes are that the full 12 bits of the memory address register are used to specify one of 4096 core addresses, while the ten least significant bits are used to specify one of 1024 addresses, and that a 4K array is assembled of planes 64 cores wide by 64 cores deep, while the 1K array is composed of planes 32 cores wide by 32 cores deep.

MEMORY ORGANIZATION

The elements which constitute the core memory and their interrelationships are indicated in Figure 3-1. Operation of core memory is initiated by Memory Read and Memory Write timing

signals received from the processor by the read memory driver and write memory driver. When an input signal to a memory driver is at ground potential, the output is at the common -3 volt level. The output of a memory driver drops to -13 volts for the duration of a standard DEC negative signal level applied to the input. The potential difference between the output terminals of the read memory driver and the write memory driver determines the direction of current flow through the address drive lines of the array. In the memory array the location of cores, which are selected to be read from or written into, is determined by the X and Y address decoder preceding and following the core array. Each address decoder decodes complementary signal outputs from six bits of the memory address register to form both an X and Y address path for the read or write current. The read and write currents produced by the read memory driver and write memory driver are identical in magnitude but of opposite polarity. The polarity is established by the connection of the driver in the system. Cores are driven by read current in a series circuit from the output terminal of the write driver, through the X and Y address decoder read-write switches, through an X and a Y path through the memory diode units and the core array and the resistor boards to a second X and Y address decoder read-write switches, and to the output terminal of the read memory driver. Write current flows through the same circuit in the opposite direction, that is, from the read driver output terminal to the write driver output terminal. This current reversal is obtained by lowering the voltage output of one of the memory drivers from the nominal -3 volt level to -13 volts during the period when the driver is enabled by either the Memory Read or Memory Write signal. This current flows through both an X and a Y drive line in the core array, and the amplitude of this current is determined primarily by the 50-ohm resistance in the resistor boards. Coincidence of the half-select current in both the X and the Y direction is required to fully select, and thus read or write, at a memory address or column of 1 selected core from each of the 12 planes.

The entire equivalent circuit for either an X or a Y address selection system of a 4K memory is shown in Figure 3-2. This entire circuit, except for the memory drivers, is duplicated for the second drive line passing through each of the cores. In this diagram the decoding of address lines which control the circuit elements is not shown since the lines are not in the actual path of read-write current. The read memory driver, at the left side of the drawing, is shown in the enabled condition, and the write memory driver, at the right side of the drawing, is shown in the disabled condition. Each read-write switch contains decoding circuits which

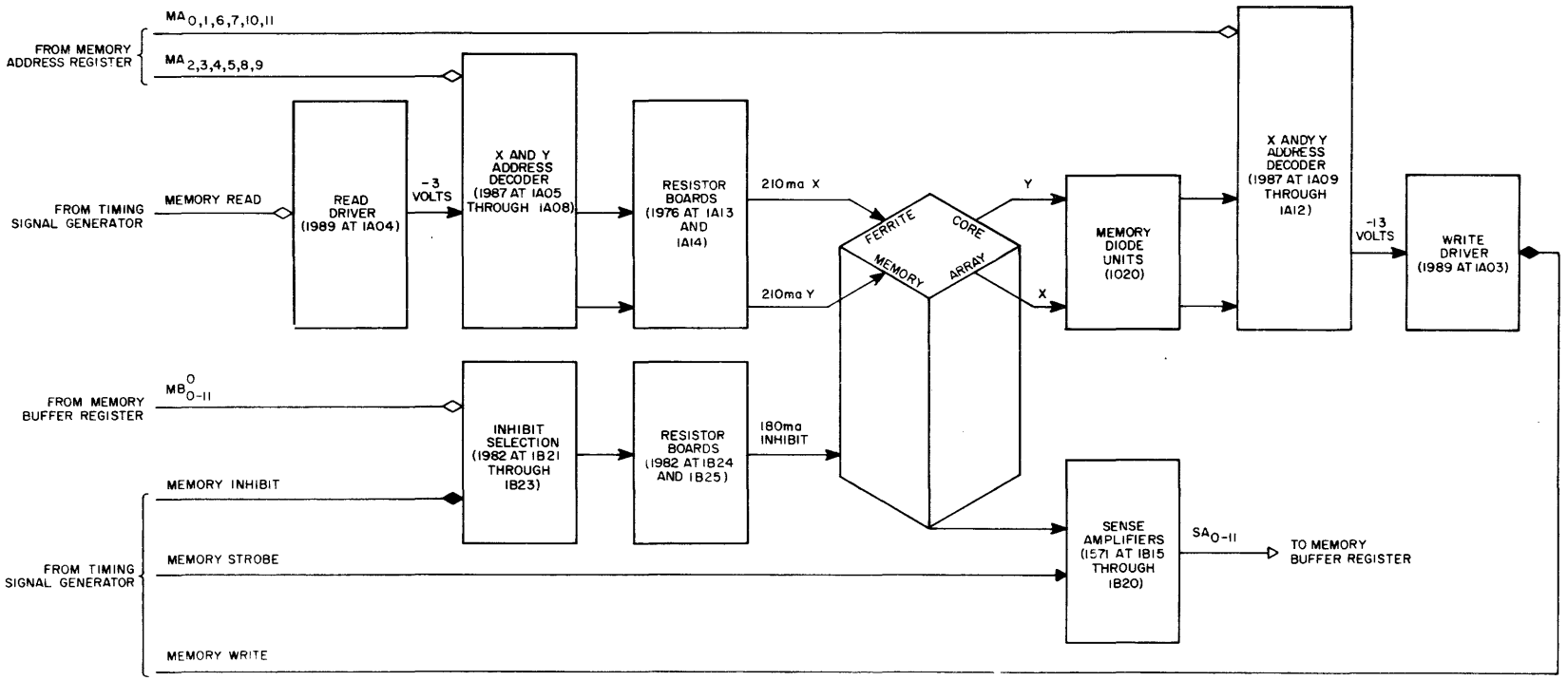


Figure 3-1 Core Memory Block Diagram (During Writing)

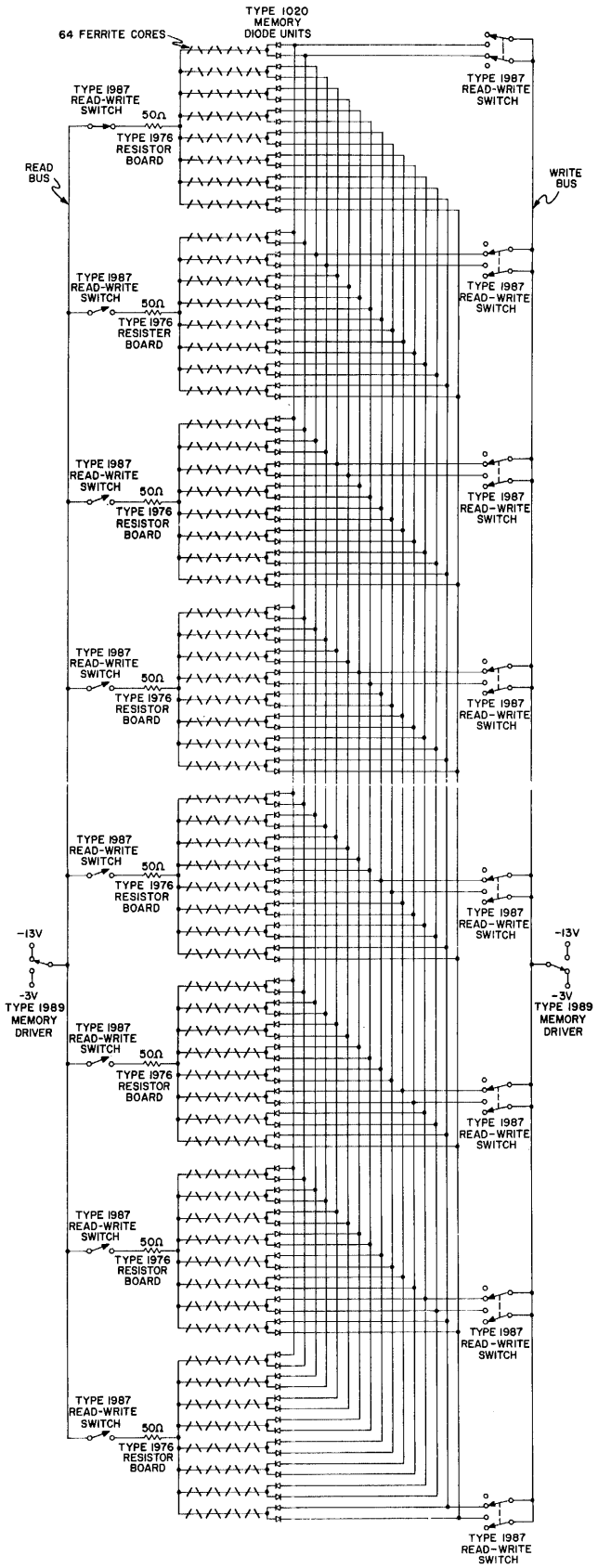


Figure 3-2 Core Memory Drive System Equivalent Circuit

control two unidirectional current switches. On the read side of the core array, these switches are connected in parallel to allow passage of either read or write current and so are indicated by a single switch on the diagram. The current switches of the read-write switch modules on the write side of the core array are not connected in parallel since the direction of current flow through these switches is controlled by the memory diode units. The read-write switches at the top of Figure 3-2 are shown in the selected condition, while all other read-write switches are shown in the disabled condition.

During the read cycle, pulses induced on the sense windings of each of the 12 planes are sampled by the sense amplifiers and compared with a preset slice level during receipt of the Memory Strobe pulse. If the voltage induced on the sense winding is of greater amplitude than the differential slice level voltage, a DEC standard positive pulse is produced by the sense amplifier to set a corresponding bit of the memory buffer register to the binary 1 state. The Memory Strobe signal is timed to produce the most reliable transfer of information from the core array into the memory buffer register, with the best signal-to-noise ratio.

During the write cycle, the Memory Inhibit signal enables operation of the inhibit selection element to produce half-select bucking currents in planes corresponding to bits containing zeros in the word being written into memory. Inhibit current flows through each core in the selected plane in a direction which cancels the effect of either the X or the Y address drive line, thereby preventing full selection and writing of ones. The planes receiving inhibit current are selected as a function of bits of the memory buffer register containing zeros. The timing of the Memory Inhibit signal causes the inhibit currents to be generated for a period which begins before and lasts until the address currents are no longer generated, thereby providing absolute surety that cores in inhibited planes cannot be set to 1.

CURRENT SOURCE

The 735 Power Supply, shown in the lower left corner of engineering drawing 7, provides the current which is switched by the address and inhibit circuits and drives the core array. Core array drive currents are produced by this supply as the -13 volt R/W and -3 volt common line supplied to both the read and write memory drivers, and the -13 volt inhibit and -3 volt common line supplied to the inhibit drivers and inhibit resistor boards. These voltages are regulated

and temperature compensated by thermistors mounted in a dummy plane between bits 5 and 6 of the array. This supply also produces the -35 volt potential which is required by all of the decoding circuits and produces a +10 volt level which is used in the internal shunt-regulator and power supply control circuits.

This supply consists of a dual power supply, as shown on engineering schematic RS-735, and a 1701 Power Supply Control module, as shown on engineering schematic RS-1701. The supply outputs at terminals B and C provide the compensated currents required by the inhibit circuits, and the outputs at terminals B and D provide the compensated current required by the read-write circuits.

Since the read-write and inhibit voltages must be well regulated, compound-connection shunt-regulator circuits are used across these outputs. The bases of shunt-regulator transistors Q1 and Q3 are brought to terminals F and N (for connection to power control 1701) rather than to their respective output voltage points. The inhibit and read-write supplies are similar except that the output current adjustment range of the read-write supply is from 0.0 to 0.4 amperes, and the output of the inhibit supply can be varied from 0.0 to 1.0 amperes. Consequently, both the inhibit supply series dropping resistance (R1-R2) and the emitter resistor (R4) of the principal shunting transistor Q4 are smaller than the corresponding resistors in the read-write supply.

Besides regulating the output voltages, the 1701 control compensates the output voltages according to the ambient temperature at the core array and permits output voltage adjustments to meet individual requirements of a specific core array. The 1701 control module contains two identical circuits, the one shown in the lower half of schematic diagram RS-1701 controls the -13 volt R/W supply, and the one shown at the top of the schematic controls the -13 volt inhibit supply of the 735. Operation of the control is implicit with the terminal connections as follows:

a. Terminals E and M are connected to the -3 volt common.

b. Terminals H and P are connected to the -13 volt R/W and -13 volt inhibit line, respectively.

c. Terminals F and N are the control outputs for the read-write and inhibit supplies, respectively.

d. Terminal A receives +10-volt operating potential from the 735 supply.

As an adjunct to the 735 supply, the control circuits perform the following functions:

a. The outputs at terminals F and N bias the base of the shunt-regulator transistors Q1 and Q3 in the 735. This bias determines the read-write and inhibit output voltage. The bias and the resulting output voltage can be adjusted by turning rheostats R13 and R3.

b. The thermistors in the dummy plane makes the bias temperature-dependent. Because the thermal coefficient of this thermistor is negative (-4.4% per degree centigrade), the supply output voltage is a negative function of temperature (-0.5% per degree centigrade). As the temperature of the core array increases, the read-write and inhibit voltages and currents decrease. This compensation adjusts the output voltages in inverse proportion to the ambient temperature at the core array, since the core winding current required to switch a memory core is inversely proportional to the core temperature.

c. The third function of the control circuit is to compensate for changes in the supply output voltages which are caused by variations in the load and in the primary input voltage.

Currently DEC purchases memories which have two different core sizes and so have different current-correction coefficients. Total read-write current and inhibit current is compensated -0.7% per degree centigrade in a Ferroxcube array and is compensated -0.4% per degree centigrade in Electronic Memories Incorporated core arrays.

MEMORY DRIVERS (17)

The read and write memory drivers are shown in the lower left portion of engineering drawing 17 to consist of the 1989 modules at locations 1A03 and 1A04. The X and Y address drive currents at the outputs of these drivers are identical in magnitude but of opposite polarity, the polarity being established by the connection of the driver in the memory system. Each memory driver functions as a programmable switch, the output terminal being switched to the -3 volt common when the input signal is at ground potential, or the output being switched to the -13 volt read-write potential when the input is a standard DEC negative level.

The exact value of the X and Y half-select current passed by the output terminal of a memory driver is determined by the temperature-compensated -13 volt R/W output of the 735 Power Supply and by the impedance of the resistor boards and other circuit resistance between the output terminals of the read and write memory drivers. Both the X and the Y half-select currents are nominally 210 milliamperes; however optimum current settings are determined at the factory and are designated on a label attached to the core array. These values are determined empirically for each memory system to assure maximum reliability and to assure peak performance of the address, inhibit, and sense circuits.

A memory driver, shown on schematic diagram RS-1989, consists of an output line which is connected to the -13 volt read/write output of the 735 Power Supply through parallel-connected transistor current switches containing Q5, Q7, Q9, and Q11. The output terminal is also connected to the -3 volt common output of the 735 supply through parallel-connected transistor current switches containing Q6, Q8, Q10, and Q12. The output circuit containing Q5 through Q11 serves as a current switch controlled by the emitter output from the circuit containing Q3. The output circuit containing transistors Q6 through Q12 functions as a current switch controlled by the circuit containing Q1. These two output circuits are identical and operate in complementary fashion, due to insertion of the inverter containing Q4 which precedes the input to the control circuit containing Q3. When the input to terminal J of this module is negative, transistor Q2 of the input stage becomes saturated, so that its collector output assures cutoff of transistors Q4, Q1, Q6, Q8, Q10, and Q12. The negative collector potential from cutoff transistor Q4 enables control transistor Q3 to conduct and thus turn on the odd-numbered output transistors to essentially connect the -13 volt potential at terminal X to the output terminal V. Conversely, when the input is at ground potential, Q2 is cut off causing conduction of Q4 and cut off of the output circuit containing odd numbered transistors. Under these conditions Q1 conducts to turn on the transistors in the output circuit containing even numbered transistors to effectively connect the -3 volt common at terminal R to output terminal V. Current equalization through the output stages is accomplished by resistor networks in the emitter circuit of each output transistor. Output-circuit overshoot protection is provided by diode D6, which parallels the emitter-base junction of Q3, and by diode D4, which parallels the emitter-base junction of Q1.

ADDRESS SELECTION (16)

The address selection circuits specify one of 64 X address lines and one of 64 Y address lines which will be conditioned to pass read or write current through the core array. Address selection is performed by the eight 1987 Read-Write Switch modules connected to the output of the memory drivers. Each module contains diode gating circuits that control four high-current read-write switch circuits. Half of the address selection is performed before the half after the current passes through the core array. Address switching performed at the output of the write memory driver is shown on the right side of engineering drawing 16, and switching performed at the output of the read memory driver is shown at the left side of this drawing.

All address selection is performed as a function of the address contained in the memory address register. Complementary output signals from the 12 bits of the MA are decoded by four groups of two read-write switches as follows:

a. MA_2, MA_4, and MA_5 are decoded by modules at locations 1A05 and 1A06 to select the X address on the read side of the array.

b. MA_3, MA_8, and MA_9 are decoded by modules at locations 1A07 and 1A08 to select the Y address on the read side of the array.

c. MA_0, MA_6, and MA_7 are decoded by modules at locations 1A09 and 1A10 to select the X address on the write side of the core array.

d. MA_1, MA_{10}, and MA_{11} are decoded by modules at locations 1A11 and 1A12 to select the Y address on the write side of the core array.

Half-select current drives 64 cores selected by the X address switching in each plane and 64 cores selected by the Y switching in each plane. Coincidence of X and Y write current in each plane provides the flux necessary to drive a core to the binary 1 state, if it is not inhibited by current from the inhibit selection circuits. Coincidence of X and Y read current in each plane completely switches a core to the binary 0 state. Drive lines for each coordinate of each of the 12 planes are connected in series. Half-select current for the X coordinate passes through one drive line for each of the 12 planes, each drive line of each plane containing 2^6 or 64 cores. Half-select current for the Y coordinate also passes through one drive line of each of the 12 planes and drives 64 cores in each plane.

A 1987 Read-Write Switch module contains four similar circuits, each circuit consisting of a 4-input ground-potential NAND gate which enables or disables transistor switching circuits to allow passage of read or write current. Two unipolarity switching circuits which pass current in opposite directions are controlled by each NAND gate. A common bus provides read-write current from terminal S to one side of each of the eight switches within a module. On the read side of the core array the output terminals for each pair of switches in a 1987 module are connected in parallel, and the outputs of each pair of switches on the write side of the core array are connected in parallel after passing through the memory diode units. The output switches enabled by each combination of input signals are indicated in Table 3-1.

TABLE 3-1 READ-WRITE SWITCH GATING

Grounded Input Terminals	Selected Positive* Current Switch		Selected Negative* Current Switch	
	Transistor	Output Terminal	Transistor	Output Terminal
E · F · M · N	Q4	Y	Q3	Z
H · J · M · N	Q12	W	Q11	X
E · K · M · N	Q8	U	Q7	V
J · L · M · N	Q16	P	Q15	R

*Polarities are specified with respect to terminal S

MEMORY DIODE UNITS AND CORE ARRAY (11, 12)

The core array is composed of 12 core planes, each containing 4096 ferrite memory cores. Each plane is 64 cores wide by 64 cores deep, corresponding to the 64X and 64Y drive lines. Every core is threaded by four windings: X and Y address windings; an inhibit winding or digit line; and a sense winding. Each X or Y address line is threaded through a row of 64 cores in each plane; jumper connections between the planes connect corresponding rows of each plane in series. A single X winding and a single Y winding intersect at only one core location or address in each plane; corresponding cores in each plane constitute a 12-bit memory address or memory register. Each plane contains an inhibit winding which passes through each core in the plane. One end of each of these windings is connected to the inhibit selection circuits, and the other end is connected in common for all 12 planes and is connected to the -3 volt common

output of the 735 Power Supply. Sense windings are also wired on a per-plane basis. A sense winding passes through each core in a single plane, and both ends of the winding are connected to separate input terminals of a sense amplifier. Connectors on the core array allow plug-in mounting of the 1020 Memory Diode Unit modules directly on the array. These diodes prevent read-write current from passing through unselected address drive lines. Coordinate X and Y address drive lines are shown on engineering drawings 11 and 12 with their connection to the memory diode units and the connectors which mate with the address selection circuits.

INHIBIT SELECTIONS (17)

During write operations, the inhibit selection circuits supply half-select current in the read polarity to all cores corresponding to bits in which zeros are to be written. This half-select current cancels the effect of one of the half-select write currents supplied by the X and Y drive lines, so that a core is prevented from being set to the binary 1 status. Inhibit selection is different from address selection in that up to 12 planes, or 0 planes can be selected simultaneously as determined by the contents of corresponding bits of the memory buffer register. The inhibit selection element is shown in the upper right portion of engineering drawing 17 to consist of 1982 Inhibit Drive modules at locations 1B21 through 1B23 and 50-ohm 1978 Resistor Board modules at locations 1B24 and 1B25.

Each 1982 Inhibit Driver module consists of four identical circuits, each circuit consisting of a 2-input ground-level NAND gate which controls the operation of a current switch transistor. One input to each NAND gate is provided by the inverted Memory Inhibit signal produced by the timing signal generator of the processor, thus enabling the inhibit selection circuits during time states T4, T5, and T6 of each memory cycle. The second input to each NAND gate is provided by the output of the associated memory buffer register flip-flop which is in the ground condition during the binary 0 state. When enabled, the current switch operated by each NAND gate allows current to flow from the -3 volt common through the core array, through the resistor boards, and through the switch to the -13 volt inhibit output of the 735 Power Supply. The inhibit current amplitude is determined by the potential difference between the temperature-compensated -13 volt inhibit output and the -3 volt common output of the 735 Power Supply and by the resistance in the circuit which is mainly determined by the 50-ohm resistors in the

resistor board modules. Like the address drive current, exact inhibit current is specified by a label attached to the memory to specify optimum values for each particular memory system. Inhibit current is nominally 180 milliamperes.

SENSE AMPLIFIERS (17)

Sense system connections are made on a per-plane basis; each sense winding passes through each core in a particular plane, and both ends of the winding are connected directly to the input terminals of a sense amplifier circuit. The geometry of the winding and of the plane form a 2 by 2 checkerboard pattern of positive and negative polarity pulses induced on the sense winding as a function of the core addressing. Full or partial magnetic flux changes of all cores in a plane induce a voltage on the sense winding. During the 70-nanosecond duration of the Memory Strobe signal produced during read operations, the rectifying sense amplifiers compare the amplitude of the voltage induced on the sense winding with a preset slice level. If the amplitude of the induced voltage is greater than the amplitude of the slice level, the circuit produces a DEC standard positive pulse at the output terminal. The output pulse from each sense amplifier is applied to the direct-set input of the corresponding bit flip-flop of the memory buffer register. The sense amplifiers are shown in the lower right portion of engineering drawing 17 to consist of either 1571 or 4554 Dual Sense Amplifier modules at locations 1B15 through 1B20.

When a core is switched from a binary 1 to the binary 0 state by a full-read current, a signal of approximately 60 millivolts is induced on the sense winding in that core plane. This 60-millivolt signal is sensed by one of the two sense amplifiers on a 1571 or 4554 module and compared with an internally-generated slice level. These modules are similar except that the slice level is adjustable in the 1571 modules and is not adjustable in the 4554 modules. Sense winding attenuation is provided by a balanced input circuit of the differential preamplifier. This preamplifier has a difference gain of approximately 20 and a common-mode gain of 0.5. The output of this preamplifier is ac coupled to a rectifying slicer with a variable slicing voltage. The output of this slicer is amplified and used as the enabling level for a pulse amplifier which functions as the final stage of the module.

TYPE 154 MEMORY EXTENSION CONTROL OPTION

Field select control and address extension control for Type 155 Memory Modules are provided by the Type 154 Memory Extension Control. Extension of the storage capacity of the PDP-5 beyond the capacity of the standard 4096-word core memory is accomplished by adding fields of 4096-word core memories, each field being a Type 155 Memory Module. Up to seven fields can be added to the standard 4096-word memory, providing a maximum storage of 32,768 words. Direct addressing of 32,768 words requires 15 binary bits ($2^{15}=32,768$). However, since programs and data need not be directly addressed for execution of each instruction, a field can be program-selected, and all 12-bit addresses are then assumed to be within the current memory field. The memory extension control consists of several 3-bit flip-flop registers that extend addresses to 15 bits to establish or select a field.

The Type 154 Memory Extension Control consists of one mounting panel of modules which can be added to a cabinet containing the added Type 155 Memory Modules. The logic circuits of the memory extension control are shown on engineering drawing BS-D-154-0-4. The wiring of the module mounting panel and the type and location of modules within this panel are shown on engineering drawings WD-D-154-0-5 and UML-D-154-0-6, respectively. Addition of a memory extension control to a standard PDP-5 requires a modification of the operator console to add indicators and switches associated with the instruction field register and the data field register of the control. These indicators are similar to all other indicators on the operator console, and the switches function in the same manner as the switch register to load information into the flip-flop registers when the LOAD ADDRESS key is lifted.

The nine functional circuit elements which comprise the memory extension control perform as follows:

Inst. Field Register - The instruction field register is a 3-bit flip-flop register which determines the memory field from which instructions are to be taken from memory. This register consists of three flip-flops of a 4218 Quadruple Flip-Flop module at location 2A13 which can be set by the 4127 Pulse Inverter module at location 2A16, and whose outputs are decoded by the 4151 Binary-to-Octal Decoder module at location 2A04. The register is cleared directly during SP1 and is set by a ones transfer of information contained in the INSTRUCTION FIELD switch register during SP2 following operation of the LOAD ADDRESS key. The register

is also set by a jam transfer of information contained in the instruction buffer register by a TP5 pulse during the program count state of a JMP or JMS instruction. This latter transfer is performed to establish the instruction field when changed under program control or to re-establish the field as an exit from a program interrupt subroutine. The octal numbered output signals from the decoder are routed to input points of the enable field signal generator of the corresponding numbered field memory module.

Data Field Register - This 3-bit flip-flop register determines the memory field used for programmed data storage and retrieval. The register consists of three flip-flops of the 4218 Quadruple Flip-Flop at location 2A14 and pulse inverters of the 4127 modules at locations 2A15 and 2A16. The register is directly cleared during SP1 and set by a ones transfer of information contained in the DATA FIELD switch register during SP2 following operation of the LOAD ADDRESS key. The register is set by a jam transfer of information from bits 6 through 8 of the MB during a CDF microinstruction to establish a microprogrammed field. This transfer is initiated by an IOT 62X1 pulse which loads the data field register from MB_{6-8} during a change data field microinstruction. The register is also set by a jam transfer of information from bits 3 through 5 of the save field register. This transfer is enacted by execution of the RMF (restore memory field) IOT microinstruction to restore program control at the conclusion of the program interrupt subroutine. The output of this register is decoded by the 4151 Binary-to-Octal Decoder at location 2A03 and supplied to enable field signal generator circuits of the corresponding field memory modules.

Break Field Register - This 3-bit flip-flop register provides a means of enabling a memory module field during data break transfers. In addition to specifying an initial address and a break request, a peripheral device can specify a memory field by supplying three address lines to the input terminals of this register. The register consists of the 4218 Quadruple Flip-Flop at location 2A19, three circuits of the 4102 Inverter module at location 2A18, and the 4151 module at location 2A05 which decodes the flip-flop output signals. Addresses supplied by an external device must be at ground potential to signify a binary 1. These signals and their complement enable the set and clear positive capacitor-diode gates at the input of each break field flip-flop. These gates are triggered to produce a jam transfer of information from the external device into the register by the Data Address $\dashv\blacktriangleright$ MA signal produced by the MA control element. Therefore, the transfer occurs during T1 of the break state in which there is no address Increment Request signal.

Inst. Buff Register - The instruction buffer register serves as a 3-bit flip-flop input buffer for the instruction field register. All field number transfers into the instruction field register are made through the instruction buffer, except transfers from the operator console switches. The instruction buffer consists of the 4218 module at location 2A10 and the 4127 modules at locations 2A11 and 2A12. The buffer is cleared and set by operation of the LOAD ADDRESS key in the same manner as the instruction field register. Jam transfer of information into the instruction buffer is accomplished by the positive capacitor-diode gates at the input or by supplying positive pulses to ground the output terminals from the pulse inverters. During a CIF microinstruction (change instruction field), the IOT 62X2 pulse triggers the capacitor-diode gates to load the buffer with the programmed field number contained in MB_{6-8}. During an RMF microinstruction, the pulse inverters at location 2A12 are triggered to transfer the contents of bits 0 through 2 of the save field register into the instruction buffer to restore the instruction field to the conditions that existed prior to a program interrupt.

Save Field Register - When a program interrupt occurs, this 6-bit register is cleared, then loaded from the instruction field and data field registers. The RMF microinstruction can be given immediately prior to the exit from the program interrupt subroutine to restore the instruction field and data field by transferring the contents of the save field (SF) register into the instruction buffer and the data field register. The SF consists of the 4220 8-Bit Buffer Register module at location 2A17 and the 4102 Inverter module at location 2A18 which serves as an output buffer amplifier for the register. The register is directly cleared during T1 of the execute 1 state of the operations which transfer program control for a program interrupt (in other words during the cycle in which the program count is stored at address 0001 of the JMS instruction forced by a program interrupt request). Then the instruction field and data field are strobed into the SF by a ones transfer by the capacitor-diode gates at the gated 1 input of each flip-flop. These capacitor-diode gates are triggered by the output of pulse amplifier NPRST at location 2A08, which in turn is triggered by a TP3 pulse during the E1 state following the program interrupt request.

State Register - The three states or conditions for generating the Enable Field signals are produced by a 3-state circuit. This circuit is designed exactly like the major states generator of the processor, and is constructed of the 4113 Diode modules at locations 2A24 and 2A25. Circuits EFH, JKL, and MNP of the module at 2A24 serve as 2-input negative NAND gates to maintain a condition set by the corresponding circuits of the module at 2A25. The E1 output

signal enables generation of the Enable Field signal as a function of the data field and is produced by a TP1 pulse during every execute 1 major state. The F V E2 output signal enables generation of the Enable Field signal as a function of the instruction field and is produced by a TP1 pulse during both fetch and execute 2 major states. The B output signal enables generation of the Enable Field signal as a function of the break field and is produced by a TP1 pulse during every break major state. Entry into any one state disables the other two states by inhibiting the inputs to the NAND gates that maintain them.

Enable Field Signal Generator - When the PDP-5 core memory capacity is extended, the standard memory is designated as field 0. This designation is effected by connecting terminal N of all 1987 Read-Write Switch modules to the Enable Field 0 signal produced by the memory extension control. This signal is generated by diode gating circuits of the 4114 module at location 2A06 and circuit RST of the 4113 module at location 2A25. The configuration of these circuits produces the ground-level Enable Field 0 signal as a function of any of the following conditions:

a. When the Disable MA signal produced by the MA control element is at ground potential, which is indicated by the $\overline{\text{MAD}}$ signal being at -3 volts.

b. When the $\overline{\text{MAD}}$ signal is at ground potential during the execute 1 state when the appropriate data field (0) is selected.

c. When the $\overline{\text{MAD}}$ signal is at ground potential during either the execute 1 or fetch state when the appropriate instruction field (0) is selected.

d. When the $\overline{\text{MAD}}$ signal is at ground potential during the break state when the appropriate break field (0) is selected.

NOTE: The $\overline{\text{MAD}}$ signal is the unbuffered output from terminal 1D09Y of the disable MA flip-flop of the MA control element. Therefore, this signal provides ground-level enabling of circuits in the memory extension control when the computer MA is <u>not</u> disabled.

A circuit similar to this one is provided in each Type 155 Memory Module to control the address selection circuits. In a memory module the circuit differs only in that the output line from the decoders that corresponds to the field number is used as the input to each of the three ground-level NAND gates, and the condition when the $\overline{MAD}$ signal is at -3 volts (entry a of the previous list) is not used.

Accumulator Transfer Gating - Diode gating circuits allow the contents of the SF, instruction field register, or the data field register to be strobed into the accumulator. Transfer of information in this manner is accomplished by circuits of 4113 Diode modules which sample the contents of registers and supply positive pulses to the input mixer upon receipt of IOT command pulses. During an RIB microinstruction, bits 6 through 11 of the AC are set by the content of the SF by 2-input negative NAND gates of the 4113 module at location 2A20. During an RIF microinstruction, bits 6 through 8 of the AC are set by the content of the instruction field register through gates EFH, JKL, and MNP of the module at 2A21. During an RDF microinstruction, bits 6 through 8 of the AC are set by the content of the data field register through gates RST, UVW, and XYZ of the module at 2A21. Initiation of the 4113 modules to produce the pulses applied to the input mixer is caused by pulse amplifier circuits of the 4606 module at location 2A22. These pulse amplifiers are gated by the IOT 62X4 pulse and the contents of the memory buffer register bits that specify the appropriate IOT microinstruction.

Device Selector - Bits 3 through 5 of the IOT instruction are decoded by the 4605 Pulse Amplifier module at location 2A07 to produce the IOT command pulses for the memory extension control. Bits 6 through 8 of the instruction are not used for device selection since they specify a field number in some commands. Therefore, the select code for this device selector is designated as 2X.

Note that the PC is always contained in address 0000 of field 0. Programming considerations for the Type 154 Memory Extension Control are discussed in computer option bulletin F-53(154).

TYPE 155 MEMORY MODULE OPTION

Extension of the PDP-5 core memory beyond the standard 4096-word capacity is accomplished by addition of Type 155 Memory Modules to the system. Each 155 module extends memory by 4096 12-bit words. Up to seven memory modules can be added to a standard PDP-5 containing

4096 words, increasing the capacity of the system to 32,768 words. Addition of from one to seven memory modules requires that a Type 154 Memory Extension Control be added to the system.

A 155 module consists of a core array, address selection circuits, inhibit selection circuits, sense amplifiers, memory drivers, and a 735 Power Supply which are identical with these described previously in this section for the standard PDP-5. The minor differences between the standard core memory and a 155 module are as follows:

a. A Field Enable signal generator is added which is identical with that described previously in this section of the manual under Type 154 Memory Extension Control Option. This generator in each module is operated from different octal field select code output signals of the data field, instruction field, and break field register decoders of the extension control. When the assigned code is present in any of these register, the generator produces a Field Enable signal during appropriate major states. This signal is connected to input terminal N of all 1987 Read-Write Switch modules in the 155 module to enable address selection. In the standard PDP-5 with no memory extension, no connection is made to terminal N of all of the 1987 modules. With the addition of memory extension these terminals of the standard machine are connected to the Enable Field 0 signal produced by the Type 154 Memory Extension Control.

b. The Memory Strobe signal produced by the timing signal generator of the processor is reshaped by a 1607 Pulse Amplifier module in the memory module before it is supplied to the sense amplifiers.

Each 155 memory module added to the PDP-5 system requires two mounting panels of system modules. Engineering drawings for the memory module are designated by the type number and are not included in this manual because of their similarity with engineering drawings 16 and 17, and BS-D-154-0-4.

intricately involved in the operations of the PDP-5. The Type 153 Automatic Multiply and Divide option described in Section 2 of this manual, the Type 154 Memory Extension Control, and the Type 155 Memory Module options described in Section 3 of this manual are not peripheral equipment options.

TELETYPE MODEL 33 AUTOMATIC SEND RECEIVE SET

The Teletype unit supplied as standard equipment with a PDP-5 serves as a keyboard input and page printer output and as a perforated-tape reader input and a tape-punch output device. This unit is a standard Model 33 Automatic Send and Receive set (ASR) as described in the bulletins 273B and 1184B produced by the Teletype Corporation. For operation with the PDP-5, this unit has been modified as follows:

a. The WRU (who are you) pawl is removed. This pawl is used only when several Teletypes are connected in a communication system so that a unit receiving a message sends a "who are you" message to the transmitting unit. The transmitting unit automatically produces the "here is" identification code and supplies it to the receiving station. In the computer system this pawl is removed to prevent insertion of the "here is" code into data supplied to the computer from the Teletype unit.

b. In early units containing a dial call control unit the OUT OF SERVICE lamp is drawn down into the console (not disconnected) and the ON LINE/LOCAL toggle switch is put in its place.

c. Cable connections are made between the Teletype unit and the control as shown on engineering drawing 18. On units containing a dial call control a signal cable is permanently connected to one of the two cables within the unit which are terminated in 50-pin connectors. In Teletype units without the dial call control, these connections are made to a terminal block within the stand. In both cases a relay is added and connections are made to the tape reader advance magnet that enable tape motion while a character is being assembled in the control and disable the magnet when the keyboard flag is a 1, indicating that the character has been assembled and is ready for transfer to the computer.

SECTION 4

INPUT/OUTPUT

Signals which pass between peripheral equipment and the PDP-5 are normally in the form of pulses supplied to a processor input bus or static levels as processor output signals which may be sampled or strobed by a selected I/O device. The exceptions to this rule are the address and data signals supplied to the processor during data break operations as static levels and the Address Accepted and IOP pulses, which are pulse outputs of the processor. The bussed nature of input/output signals of the processor requires that the peripheral equipment contain gating circuits to control the application of input pulses to the processor and timing control circuits to strobe processor output lines to transfer information into external device buffers. The design of circuits in input/output equipment that performs these operations depends upon the characteristics of the processor interface circuits as described in Section 6, the functional operation of the processor interface logic elements as explained in Section 2, and by the nature of the circuits in the peripheral equipment which receives or transmits signals. Gating circuits in peripheral equipment that supplies input pulses to the processor can be similar to those shown on the processor drawings for standard input/output devices. Programmed information transfers (including initializing of equipment using the data break facility) between the processor and all other devices require that each circuit (or group of circuits) transmitting or receiving information be enabled by a pre-established select code contained in bits 3 through 8 of an IOT instruction, and require that transfers are accomplished in synchronism with the timing of the processor. These operations are accomplished by a 4605 Pulse Amplifier module that serves as a device selector. Typical device selectors are shown on engineering drawing 8 for both the program interrupt synchronization element and the Type 137 Analog-To-Digital Converter, and on engineering drawing 18 for the Teletype control. The schematic circuit for a device selector is shown on drawing RS-4605.

The standard peripheral equipment supplied with a PDP-5 consists of a Teletype Model 33 Automatic Send Receive set and a Teletype Control which are described in this section of the manual. Optional peripheral equipment is described in separate documents, except for the Type 137 Analog-To-Digital Converter which is described in this section because it is

This modification takes only a few minutes and does not permanently limit any normal use which can be made of the 33 ASR.

TELETYPE CONTROL (18)

Serial information read or written by the Teletype unit is assembled or disassembled by the control for parallel transfer to the input mixer or from the accumulator of the processor. The control also provides the program flags which cause a program interrupt or an instruction skip based upon the availability of the Teletype unit and thus controls the rate of information transfer flow between the Teletype and the processor as a function of the program. The control is shown on engineering drawing 18 to consist of the eight system modules at locations 1F18 through 1F25. This drawing also shows the interface connections between the control and the Teletype unit. Interface connections between the control and the processor are indicated on Table 4-1, except for the standard inputs to the device selectors from the IOP generator and the memory buffer register, which are described in detail in Section 6 of this manual.

TABLE 4-1 TELETYPE CONTROL INTERFACE WITH PROCESSOR

Signal	Processor			Symbol and Direction	Teletype Control Terminal
	Logic Element	Engineering Drawing	Terminal		
Power Clear	Power Clear Gen	5	1E05E	→	1F25M
AC_4^1	AC	9	1B06F	—◇	1F25X
AC_5^1	AC	9	1B07F	—◇	1F25Y
AC_6^1	AC	9	1B08F	—◇	1F25Z
AC_7^1	AC	9	1B09F	—◇	1F25L
AC_8^1	AC	9	1B10F	—◇	1F25K
AC_9^1	AC	9	1B11F	—◇	1F25J

TABLE 4-1 TELETYPE CONTROL INTERFACE WITH PROCESSOR (continued)

Signal	Processor			Symbol and Direction	Teletype Control Terminal
	Logic Element	Engineering Drawing	Terminal		
AC^{1}_{10}	AC	9	1B12F	—◇	1F25H
AC^{1}_{11}	AC	9	1B13F	—◇	1F25F
Teleprinter Flag	Skip Control	8	1C04X	◆—	1F25P
Teleprinter Flag	Interrupt Sync	8	1D04F	◆—	1F25P
Keyboard Flag	Skip Control	8	1E09Y	◆—	1F24V
Keyboard Flag	Interrupt Sync	8	1D04H	◆—	1F24V
IOT 6031	Skip Control	8	1E09X	◀—	1F19E
IOT 6032	AC Control	8	1C01E	◀—	1F19H
IOT 6034	IM	14	1E12K	◁—	1F19K
IOT 6041	Skip Control	8	1C04W	◀—	1F20E
LUI_1	IM	14	1E15X	◇—	1F24E
LUI_2	IM	14	1E15L	◇—	1F24J
LUI_3	IM	14	1E14X	◇—	1F24K
LUI_4	IM	14	1E14L	◇—	1F24L
LUI_5	IM	14	1E13X	◇—	1F24N
LUI_6	IM	14	1E13L	◇—	1F24F
LUI_7	IM	14	1E12X	◇—	1F24H
LUI_8	IM	14	1E12L	◇—	1F24V

In all programmed operation, the Teletype unit is considered as two separate devices. It is considered a line unit in (LUI) as a source of input intelligence from the keyboard or the perforated-tape reader and is considered a line unit out (LUO) for computer output information to be printed and/or punched on tape. Therefore, two device selectors are used; the 4605 Pulse Amplifier at location 1F19 is assigned the select code of 03 to initiate operations associated

with the keyboard/reader, and the device selector at 1F20 is assigned the select code of 04 to perform operations associated with the teleprinter/punch. Parallel input and output functions are performed by corresponding IOT pulses produced by the two device selectors. Pulses produced by IOP1 pulse trigger skip gates in the skip control element; pulses produced by the IOP2 pulse clear the control flags and/or the accumulator; and pulses produced by the IOP4 pulse initiate data transfers to or from the control.

Signals used by the Teletype unit are standard 11-unit-code serial current pulses consisting of marks (bias current) and spaces (no current). Each 11-unit Teletype character consists of a 1-unit start space, eight 1-unit character bauds, and a 2-unit stop mark. Teletype characters from the keyboard/reader are received by the 4706 Teletype Incoming Line Unit module at location 1F24 containing the 8-bit flip-flop shift register LUI. The character code of a Teletype character is loaded into the LUI so that spaces correspond with binary zeros and marks correspond to binary ones. Upon program command the content of the LUI is transferred in parallel to the accumulator, via the input mixer. Eight-bit computer characters from the accumulator are loaded in parallel into the 8-bit flip-flop shift register LUO of the 4707 Teletype Transmitter module at location 1F25 for transmission to the Teletype unit. This module generates the start space, then shifts the eight character bits into a flip-flop which controls the printer selector magnets of the Teletype unit, and then produces the stop mark. This transfer of information from the LUO into the Teletype unit is accomplished in a serial manner at the normal Teletype rate.

A negative Active signal is produced by the control circuit of the Teletype incoming line unit module when a Teletype character starts to enter the LUI. This signal clears control flip-flop FF_1, which in turn de-energizes a relay in the Teletype unit to release the tape feed latch. When released, the latch mechanism stops tape motion only when a complete character has been sensed and before sensing of the next character is started. A keyboard flag on the 4706 module is set and causes a program interrupt when an 8-bit computer character has been assembled in the LUI from a Teletype character. The program senses the condition of this flag with a KSF microinstruction (skip if keyboard flag is a 1, IOT 6031) and issues a KRB microinstruction (IOT 6036) which clears the AC, clears the keyboard flag, transfers the content of the LUI into the AC, and sets FF_1 to enable advance of the tape feed mechanism.

A teleprinter flag in the Teletype transmitter module is set when the last bit of the Teletype code has been sent to the teleprinter/punch, indicating that the LUO is ready to receive a new character from the AC. This flag is connected to both the program interrupt synchronization element and the skip control element. Upon detecting the set condition of the flag by

means of the TSF microinstruction (skip if teleprinter flag is a 1, IOT 6041) the program issues a TLS microinstruction (IOT 6046) which clears the flag and loads a new computer character into the LUO.

Operation of the Teletype incoming line unit module requires an input clock signal which is eight times the baud frequency of the Teletype unit. This signal is used to control the strobing of Teletype information into the LUI during the center of each baud (which is the most reliable time for sensing) and to control the shifting of information through the flip-flops of the LUI. The Teletype transmitter module requires an input clock frequency which is twice the baud frequency of the Teletype unit. This signal is used to control the shifting of the LUO and thus determines the timing of the 11-unit-code Teletype character it generates. The LUI Clock and LUO Clock signals are produced by the 4225 8-Bit BCD or Binary Counter module at location 1F23. Six flip-flops of this module are connected as a binary counter which provides frequency division of the output from the 4407 Crystal Clock module at location 1F22. This frequency division method is used since electronic clocks are not reliable at the low frequency required for Teletype operation. The 14.08-kc frequency of the clock is 128 times the baud frequency of the Teletype unit. Division of the clock frequency by 16 (4 binary flip-flops) yields the LUI Clock signal, which is 8 times the baud frequency, and division by 64 (6 binary flip-flops) yields the LUO Clock signal, which is twice the baud frequency.

TYPE 137 ANALOG-TO-DIGITAL CONVERTER (137-2-1)

This converter operates in the conventional successive approximation manner, using the memory buffer register as a distributor shift register and using the accumulator as the digital buffer register. This process starts by assuming that the value of the analog input signal is at mid scale by setting a binary 1 into the most significant bit of the accumulator and producing a voltage equal to the center of the range of the converter (ground to -10 volts). This voltage is produced by a digital-to-analog converter which operates as a function of a number contained in the accumulator. This voltage is then compared with the analog input signal and the results of the comparison are used to clear the least significant bit of the accumulator if the approximated voltage generated is of greater amplitude than the analog input signal. This process is then repeated by setting the next least significant bit of the accumulator to the 1 state, generating the analog signal according to the contents of the accumulator, and comparing

this signal with the analog input signal to clear the bit of the AC which was just set previously if the generated signal is greater than the input signal being measured. This process is repeated a number of times depending upon the preset accuracy of the conversion. Each approximation reduces the error of the resultant binary number in the AC by approximately one half. The bit of the accumulator which is first set then evaluated is controlled by the memory buffer register. During the first approximation, a binary 1 is set into most significant bit of the MB and is shifted right one place at the conclusion of each approximation. The bit of the accumulator which is processed is controlled by the location of this binary 1 in the MB. The location of this binary 1 in the MB is also used to control the number of approximations performed, and hence determines the accuracy of the conversion. Since the conversion is started at the time the binary 1 is shifted in the MB, one conversion takes place after the sensing of the 1 in the MB which discontinues the conversion process. At the conclusion of the conversion, the unsigned binary number contained in the accumulator is accurate to ± one half of the digital value of the least significant bit converted. At the conclusion of the conversion a Restart 1 pulse is produced by the converter which clears the MB and continues the normal computer program.

The Type 137 Analog-To-Digital Converter consists of the eight system modules in locations 1E17 through 1E24 and a flip-flop and three inverters in module mounting panel 1D which are unused in the operation of the processor. Complete module mounting panel wiring for the converter is provided in the standard PDP-5, so that addition of the 137 option requires only addition of the modules and wiring connections that determine the accuracy of the conversion and connection of the analog input signal to be measured. The block schematic for the logic circuits of the converter is shown on engineering drawing BS-D-137-0-1, and the interface connections between the converter and the PDP-5 processor are indicated in Table 4-2, except for the inputs to the device selector. Note that the input connection to converter terminal 1E17L is one of six possible connections to the MB and determines the accuracy of the conversion. The origin of this signal in the MB is indicated in Table 4-3 with other characteristics of the converter affected by the accuracy connection. To save program running time, the converter should be connected to provide only the accuracy required by the program application. Maximum error of the converter is equal to the switching point error plus the quantization error. Maximum quantization error is equal to ± one half of the digital value of the least significant bit. Switching point error, total conversion time, and execution time of the IOT microinstruction which initiates operation of the converter are indicated in Table 4-3.

TABLE 4-2 ANALOG-TO-DIGITAL CONVERTER INTERFACE WITH PROCESSOR

Signal	Processor			Symbol and Direction	Converter Terminal
	Logic Element	Engineering Drawing	Terminal		
IOT 6004	I/O Halt	5	1D12U	◄—	1F18K
IOT 6004	AC Control	8	1C04K	◄—	1F18K
Restart 1	Restart	5	1E02W	◄—	1E17H
Restart 1	MB Control	7	1C15U	◄—	1E17H
A-D Start	MB	9	1B02M	◆—	1D01J
Shift MB	MB	9	1B02B	◁—	1E17X
A-D Convert	AC	9	1B02W	◁—	1E17R
Comparator	AC	9	1B02T	◇—	1D20Z
MB^1_{5-10}	MB	9	1B07-11L	—◆	1E17L
AC^1_0	AC	9	1B02F	—◆	1E21F
AC^1_1	AC	9	1B03F	—◆	1E21H
AC^1_2	AC	9	1B04F	—◆	1E21J
AC^1_3	AC	9	1B05F	—◆	1E21K
AC^1_4	AC	9	1B06F	—◆	1E21F
AC^1_5	AC	9	1B07F	—◆	1E20F
AC^1_6	AC	9	1B08F	—◆	1E20H
AC^1_7	AC	9	1B09F	—◆	1E20J
AC^1_8	AC	9	1B10F	—◆	1E20K
AC^1_9	AC	9	1B11F	—◆	1E20L

TABLE 4-2 ANALOG-TO-DIGITAL CONVERTER INTERFACE WITH PROCESSOR (continued)

Signal	Processor			Symbol and Direction	Converter Terminal
	Logic Element	Engineering Drawing	Terminal		
AC^{1}_{10}	AC	9	1B12F	◆—	1E19F
AC^{1}_{11}	AC	9	1B13F	◆—	1E19H

TABLE 4-3 CHARACTERISTICS OF THE 137

Adjusted Bit Accuracy	Origin of MB Signal to 1E18T	Switching Point Error	Conversion Time per Bit (in μsec)	Total Conversion Time (in μsec)	Instruction Execution Time (in μsec)
6	1B07L	±1.6%	3.5	24.5	36.5
7	1B08L	±0.8%	4.0	32.0	44.0
8	1B09L	±0.4%	4.5	40.5	52.0
9	1B10L	±0.2%	5.0	50.0	62.0
10	1B11L	±0.1%	6.0	66.0	78.0
11	1B12L	±0.05%	11.0	132.0	144.0

Operation of this converter is initiated by execution of an ADC microinstruction which causes generation of an IOT 6004 pulse. This pulse is produced by the device selector at location 1F18 which has the assigned select code of 00. This device selector also serves the program interrupt synchronization element and is shown on engineering drawing 8. This pulse performs the following operations:

a. Sets the I/O-hlt flip-flop which in turn clears the run flip-flop, as shown on engineering drawing 5, to temporarily halt the computer program after issuing the TP1 pulse. The TP1 pulse initiates generation of signals which clear the MB.

b. Initiates operation of the pulse amplifier in the AC control element, shown on engineering drawing 8, that produces the Clear AC signal.

c. Sets the A-D start flip-flop to the 1 status by supplying a positive grounding pulse to the 1 output terminal.

d. Initiates operation of the 4303 Integrating Single Shot at location 1E18.

The binary 1 output of the A-D start flip-flop enables a capacitor-diode gate at the set-to-1 input of the most significant bit of the MB and the AC. These capacitor-diode gates are triggered by the Shift MB and A-D Convert signals produced by pulse amplifiers UWX and MPR of the 4606 module at location 1E17 of the converter. These pulse amplifiers are initiated by the negative shift of the 0 output level of the integrating single shot when the time delay has expired. The integrating single shot is a monostable multivibrator whose 0 output (at terminal U) is at ground potential during the delay period and whose 1 output (at terminal W) is at -3 volts during the delay period. This circuit is self-regenerative through a positive capacitor-diode gate which is enabled by a binary 1 output from a selected flip-flop of the MB. The output from this flip-flop of the MB is in the ground condition until a specified number of approximations have taken place, at which time this MB flip-flop is set to 1 and the signal changes to -3 volts, disabling the capacitor-diode gate. This gate is initiated by the positive transition of the 1 output of the multivibrator at the conclusion of each delay period as long as the MB accuracy control flip-flop remains in the 0 state. The timing of the single shot delay period is adjusted by an internal potentiometer to correspond with the conversion time per bit as specified in Table 4-3.

When the MB accuracy control bit becomes a binary 1, it enables the capacitor-diode gate at the input to pulse amplifier JH of the module at location 1E17. This pulse amplifier is initiated by the negative shift of the 0 output from the integrating single shot at the expiration of the final delay period, and thus produces the Restart 1 pulse. The Restart 1 pulse sets the run flip-flop to allow the computer program to advance, clears the I/O-hlt flip-flop, and causes generation of the pulses which clear the MB..

The A-D Convert signal is supplied to the direct-clear input of the A-D start flip-flop so that a single 1 is set into the MB. This flip-flop is also cleared during the power turn on and turn off sequence by the Power Clear pulses.

Having been cleared by the IOT 6004 pulse, then having a binary 1 set into the most significant bit flip-flop, the accumulator contains a binary number which corresponds to one half of its possible maximum value during the first approximation. The state of each bit of the accumulator controls a level amplifier of the modules at locations 1E19 through 1E21. The level amplifiers also receive a -10 volt potential from the output of the 1704 -10 Volt Precision Power Supply module at location 1E23. Each level amplifier circuit provides an output ground potential when the input signal is at ground level, and produces a -10 volt output signal when the input is at -3 volts. The output from each level amplifier is combined in a 1574 12-Bit Digital-To-Analog Converter module at location 1E22 that produces the analog voltage to represent the binary number contained in the accumulator. The output of this converter is compared with the analog input signal to be measured by a 1572 Difference Amplifier module at location 1E24. The output (at terminal F) of this difference amplifier is -3 volts if the input from the converter (at terminal P) is more negative than the analog input signal (at terminal N) being measured. The output of this amplifier is at ground potential if the input from the converter is more positive than the analog input signal. This output is inverted and supplied to the accumulator as the Comparator signal.

The Comparator signal is supplied to one input of a 2-input ground-level AND gate at the input of each flip-flop of the accumulator. The second input to each AND gate is enabled by the corresponding bit of the memory buffer register being in the 1 state. When the AND gate is enabled by both conditions, it supplies the enabling level to a positive capacitor-diode gate at the clear input of the accumulator flip-flop. A corresponding positive-capacitor diode gate at the set-to-1 input of each AC flip-flop is enabled by the binary 1 state of the next most significant bit of the memory buffer register. This input to the set-to-1 capacitor-diode gate of AC_0 is conditioned by the binary 1 state of the A-D start flip-flop of the converter. These capacitor-diode gates are triggered at the conclusion of each delay period of the integrating single shot. At this time also, the Shift MB signal is produced to shift the contents of the memory buffer register one position to the right. This shifting is accomplished by a jam transfer of information from the next most significant bit of the MB (and from the A-D start flip-flop for MB_0). This operation transfers a binary 1 into MB_0 during the first conversion and shifts it to the right for each successive conversion. The MB bit containing a 1 enables the next least significant bit of the accumulator to be set to 1 for the next approximation.

In summary, the IOT 6004 pulse clears the MB and AC, initiates an I/O halt, starts operation of an integrating single shot whose period is determined by the time required to generate and compare an analog signal with the signal to be measured, and sets the A-D start flip-flop which serves as an extension for the memory buffer register. When the single shot period elapses for the first time, the content of the memory buffer register is shifted to the right so that all bits contain zeros except the most significant bit which contains a 1. At this time also, themost significant bit of the accumulator is set to 1. The content of the accumulator is then used to produce an analog signal which is compared with the signal to be measured. If the generated analog signal is more negative (greater amplitude) than the signal being measured, the Comparator signal is at ground level, enabling the capacitor-diode gate at the clear input of AC_0. When the time period of the integrating single shot elapses again, AC_0 is cleared if the Comparator signal is at ground potential and AC_1 is set to 1 from the content of MB_0. This operation of setting a 1 into the next least significant AC flip-flop, producing a comparator signal to clear the AC bit based on the comparison with the signal being measured, and advance of a binary 1 through the MB continues until the integrating single shot is no longer regenerative. Regenerative operation of the single shot is inhibited when the binary 1 shifted through the MB reaches a preselected bit. At this time the MB bit output enables a pulse amplifier to produce the Restart 1 signal when the last time period of the single shot expires. The restart pulse restores the processor timing signal generator to allow the program to continue and clears the MB. At this time the AC holds an unsigned binary number that corresponds with the value of the analog input signal. This number can be processed under program control.

SECTION 5

LOGIC FUNCTION

Manual and automatic operation of the PDP-5 is required in the performance of any complete task. Manual operation is normally limited to storing a readin mode loader program, modifying data or addresses in an existing stored program, or establishing the starting conditions for a program to be run automatically. Automatic operation is used in the performance of all programs except in maintaining the equipment or troubleshooting a new program. The functions performed during each time state of each major state for both manual and automatic operation are shown on engineering drawing FD-D-5-0-2. Manual operation and manual timing are indicated on the right side of this drawing, and automatic operation is indicated on the remaining portion of the drawing. All manual operations are performed in one cycle of the special pulse generator, and automatic operation cycles through major states, determined mainly by the instruction currently in progress. Automatic operation is initiated by a manual operation and, since there is no instruction in progress when operations are started, automatic operation always begins in the program count state to locate the first instruction to be executed.

MANUAL OPERATION

Keys and switches on the operator console allow information to be stored in core memory, allow the contents of a specified core memory register to be displayed for visual examination, and allow execution of a program automatically or semi-automatically. Operation of either the LOAD ADDRESS, DEPOSIT, EXAMINE, START, or CONTINUE key initiates operation of the special pulse generator to produce the four SP time states. These time states enable sequential actions to occur, beginning during time state SP0 by clearing the run flip-flop. Operation of either the DEPOSIT, EXAMINE, STOP, key or setting of either the SINGLE STEP or SINGLE INST switch to the right position causes operations to stop by clearing the run flip-flop during T6 of any time cycle or the final time cycle of the current instruction.

LOAD ADDRESS Key

This key is lifted to load a number, manually set into the SR, into the MA to specify an address for succeeding manual or automatic operations. Operation of the key clears the run flip-flop during SP0, clears and enables the MA during SP1, and transfers the content of the SR into the MA during SP2.

DEPOSIT Key

This key provides a means of storing a number, manually set into the SR, into the core memory register currently specified by the MA. When this key is lifted, immediately the MA Carry Enable signal level is produced, and the following actions take place during the cycle of the special pulse generator:

a. During SP0 the run flip-flop is cleared.

b. During SP1 the MA is enabled, the IR is cleared, the int ack (interrupt acknowledge) flip-flop is cleared, and the MB is cleared.

c. During SP2 flip-flop IR_1 and IR_2 are set to designate the DCA instruction, the AC is cleared, and the major state generator is set to the execute 1 state.

d. During SP3 the int (interrupt) delay flip-flop is cleared, the content of the SR is transferred into the AC, and the run flip-flop is set.

Setting the run flip-flop enables operation of the timing signal generator, and the computer commences normal operation beginning with time state T2 during major state E1 of a DCA instruction. During time state T3, the content of the AC is transferred into the MB and the accumulator is cleared. The content of the MB is then written into core memory during T5 and T6, and the E1 major state expires at the beginning of T6 when a new state is entered. In automatic operation the E1 state of the DCA instruction is normally followed by a P state, however during the P state the MA is disabled, and so the E2 state is forced at T6 of this manual operation. During T6 the run flip-flop is cleared, disabling the time pulse generator at the end of the T1 state. During T1 of the E2 major state the content of the MA is incremented by one to allow successive operations of the DEPOSIT key to store information at successive core memory addresses without the necessity of loading each address into the MA by means of LOAD ADDRESS key. Since the time pulse generator is disabled and stops at the end of T1, the operations performed by the DEPOSIT key are then concluded.

EXAMINE Key

This key provides a means of reading the information contained in a specified core memory address so that its content can be examined as displayed by the indicators of the MB. Immediately upon pressing this key, the MA is enabled and the following operations occur during the cycle of the special pulse generator:

a. During SP0 the run flip-flop is cleared.

b. During SP1 the MA is enabled, the IR is cleared, the int ack flip-flop is cleared, and the MB is cleared.

c. During SP2 the AC is cleared, the major state generator is set to the execute 1 state, and the IR_2 flip-flop is set to establish the TAD instruction.

d. During SP3 the int delay flip-flop is cleared and the run flip-flop is set.

When the run flip-flop is set, the timing signal generator is enabled and operation continues in the E1 state of the TAD instruction. During T2 and T3, the content of the core memory register currently selected by the MA is read and transferred into the MB. During T4 of a TAD instruction, the content of the MB is combined with the content of the AC in a half add operation. Since the accumulator was cleared during SP2, this operation serves as a direct transfer between the MA and the AC. During T5, the content of the MB is rewritten into core memory. During T6, the major state generator is forced to the E2 state and the run flip-flop is cleared. During T1 of the E2 state the content of the MA is incremented and the cycle stops to complete the operations performed by the EXAMINE key. The incrementing of the MA during major state E2 allows repeated operation of the EXAMINE key to display the contents of successive core memory registers without specifying each address.

START Key

Operation of this key initiates automatic operation of the PDP-5, commencing at the program count currently contained in the MA. When this key is pressed, the timing signal generator is initiated and the following operations take place:

a. During SP0 the run flip-flop is cleared.

b. During SP1 the int ack flip-flop is cleared, the IR is cleared, and the MB is cleared.

c. During SP2 the AC is cleared, the major state generator is set in the P state, and flip-flops IR_0 and IR_2 are set to establish the JMP instruction.

d. During SP3 the int delay and int enable flip-flops are cleared, the content of the MA is transferred into the MB, the link is cleared, the MA is disabled, and the run flip-flop is set.

When the run flip-flop is set, the timing signal generator is enabled and automatic operations commence at time state T2 in the program count state of a JMP instruction. Since the MB already contains the address of the first instruction to be performed, no Memory Strobe signal is produced and automatic operation continues as normal. During time state T5 the IR is cleared, and during T6 the fetch state is entered to bring the specified instruction from core memory and to commence executing it.

CONTINUE Key

This key provides a means of restarting a program at the beginning of any cycle under the conditions which currently exist in the program counter and major state generator. When the CONTINUE key is pressed, the special pulse generator is initiated to perform the following operations:

a. During SP0 the run flip-flop is cleared.

b. During SP1 a TP1 pulse is produced to allow clearing of registers and other functions performed during time state T1 of a normal cycle.

c. During SP3 the run flip-flop is set.

When the run flip-flop is set, the program continues in the normal automatic mode of operation beginning in time state T2.

STOP Key

Lifting of the STOP key provides a means of halting the program. Operation of this key causes the run flip-flop to be cleared at T6 so that the timing signal generator is inhibited and stops at the conclusion of the T1 state.

SINGLE STEP and SINGLE INST Switches

These two switches provide a means of advancing through a program semi-automatically, either one cycle at a time or one instruction at a time. In normal automatic operation both of these switches are set to the left position so that they perform no function. When the SINGLE STEP switch is in the right position, the run flip-flop is cleared during T6 of any cycle so that operations stop during T1 time. When the SINGLE INST switch is set to the right position, the run flip-flop is cleared during T6 of the major state that normally precedes the program count state, therefore halting operation at the conclusion of the execution of any instruction before another instruction is read from core memory. When either of these switches is set in the right position, a program can be advanced by means of the CONTINUE key. Both of these modes of semi-automatic operation are useful in monitoring the operation of a program as a means of checking a new program or in maintaining the PDP-5.

AUTOMATIC OPERATION

The normal mode of PDP-5 operation is automatic execution of programmed instructions. Automatic programmed operation can be modified by a program interrupt (produced by peripheral equipment to transfer program control to a subroutine) and can be temporarily disrupted by a data break (initiated by a peripheral device for a transfer of information between that device and core memory). Features of automatic programmed instruction execution such as I/O skip, and I/O halt and restart are standard means which can be utilized during a program and so are not program modes in themselves and are not discussed in this chapter. These features are discussed in detail in Section 2 and in Section 4.

Instructions

The following explanations of the functions performed during the execution of each instruction assume that the PDP-5 is energized and operating normally and that the address of the next instruction is located in the MB. Therefore, each instruction explanation begins at the start of the fetch state.

Logical AND (AND)

The AND function is performed between the content of a specified core memory register and the content of the accumulator in three cycles; fetch, execute 1, and program count. As in

all instructions, the fetch state is entered with the program count stored in the MB. During T1 of the F state the content of the MB is transferred into the MA, the MB is cleared in preparation for receiving the current instruction, and the skip flip-flop is cleared. At the start of T2, reading of the new instruction begins and strobing of the instruction into the MB occurs during T3. Also during T3 the four most significant bits of a new instruction word are transferred into the IR from the MB. As in all instructions, the instruction word is restored in the original core memory address during T5 and T6 of the fetch state. Since the AND instruction is a memory reference instruction (not an IOT and not an OPR), nothing further is accomplished during the fetch state. During T6 of the fetch state, the major state generator is set to the E1 state since the instruction is not a JMP and contains a 0 in bit 3, assuming direct addressing. If the instruction does contain a 1 in bit 3, the defer state is entered from the fetch state, and then the execute 1 state is entered from the defer state.

If the AND instruction contains a 1 in bit 3, the defer state is entered to load the MB with the 12-bit effective address of the operand from the core memory address specified in the instruction. During time state T1 the core memory address containing the effective address is loaded into the MA by transferring the content of bits 5 through 11 of the MB into corresponding bits of the MA, and by maintaining the current content of bits 0 through 4 of the MA (containing the PC) if bit 4 of the instruction is a 1, or clearing bits 0 through 4 of the MA if bit 4 of the instruction contains a 0. After this transfer the MB is cleared during T1 and the content of the core memory register at the modified address is read into the MB as the effective address. If this effective address is one of the eight auto-index registers (address 0010 through 0017) the content of the MB is incremented by one during T4. The content of the MB is restored in memory during T5 and T6. During T6 of the defer state, the major state generator is set to the E1 status since the current instruction is not a JMP.

The E1 state of the AND instruction is entered to locate the operand and perform the logical AND operation (in other words to execute the instruction). The effective address of the operand is loaded into the MA as a function of the content of bits 3 and 4 of the current instruction. If bit 3 of the instruction contains a 1, the 12-bit effective address of the operand is loaded into the MB during the defer state, so the content of the MB is transferred into the MA. If the instruction contains a 0 in bit 3, the address portion of the instruction (bits 5 through 11) is transferred into the MA (which currently contains the program count) from the MB and bits 0

through 4 of the effective address are established in the MA as a function of the content of bit 4 of the instruction. If the instruction contains a 1 in bit 4, bits 0 through 4 of the MA are cleared (to specify memory page 0); if the instruction contains a 0 in bit 4, bits 0 through 4 of the MA are undisturbed (to specify the current memory page contains the operand). After this transfer the MB is cleared and the operand is read from core memory into the MB during T2 and T3. The logical AND operation is then transacted between the content of the MB and the content of the AC by a transfer of zeros. In other words, if an MB bit contains a 0, the corresponding bit of the AC is set to 0. Therefore, at the end of this operation all bits of the AC are cleared except bits which contained a 1 in both the accumulator and in the operand prior to the operation. During T6 the E1 state is concluded by setting the P state into the major state generator. This operation takes place because the instruction is not a JMS and since a break request is not present. If a break request is present, the break state is entered rather than the program count state.

The P state is used to load the address of the next instruction into the MB from the program counter. During the entire P state, the MA is disabled so that the program counter is addressed. Since the AND instruction is not a JMP instruction and is not a JMS instruction, the MB is cleared during T1. During T2 and T3 the address of the next instruction is read from core memory at address 0000 and strobed into the MB. Since the skip flip-flop is in the 0 state (it was clear during T1 of the fetch state), the content of the MB is incremented by one to advance the program count to the address of the instruction to be performed next. During T5 and T6 this address is restored into the program counter at address 0000 of core memory, and the instruction register is cleared. During T6 the major state generator is set to the fetch state so that the new instruction is drawn from core memory during the following cycle at the address currently contained in the MB.

Twos Complement Add (TAD)

The TAD instruction is performed by a fetch, execute 1, and program count cycle normally, but can have a defer cycle interposed between the fetch and execute 1 states to locate an indirectly addressed address of the operand. The fetch, defer, and program count cycles of this instruction perform operations identical to those described previously for the AND instruction. The operations performed during time states T1, T2 ,and T3 of the E1 state are identical to the operations performed under the corresponding conditions of the AND instruction.

During the T4 state of the E1 cycle of the TAD instruction, the 2's complement add operation is performed by executing a half add between the content of the MB and the content of the AC. During T5 the AC carry chain is enabled, and the carry pulses are propagated during T6. The operand is restored in core memory during T5 and T6, and a new state is set into the major state generator at T6 time. This new state is the program count state unless a break request has been made, in which case the break state is entered following expiration of the E1 state.

Index and Skip If Zero (ISZ)

The ISZ instruction is performed in three cycles consisting of a fetch, execute 1, and program count. If the address of the operand must be determined indirectly, a defer state is executed between the fetch and the execute 1 state. The ISZ instruction is performed exactly as specified for the AND instruction during the fetch , defer, and program count states and during time states T1, T2, and T3 of the execute 1 state. During time state T4 of the E1 cycle, the content of the MB is incremented by one and the MB carry is enabled. If the most significant bit of the MB changes from the 1 to the 0 state as a result of the carry being propagated through the register, the skip flip-flop is complemented (to set it since it was cleared during T1 of the fetch cycle). The skip flip-flop is complemented only when the MB carry signal ripples through the entire register to change the contents of the register from -1 to 0. During T5 and T6 the operand is restored in core memory, and during T6 the E1 state expires and is replaced by the P state.

The program count state of the ISZ instruction performs functions identical to those described for the P cycle during execution of the AND instruction except that the sensing of the skip flip-flop increments the content of the MB by two if the skip coniditions are satisfied (the content of the MB changed from 7777 to 0000 when incremented by one) so that the program count is incremented to skip one instruction.

Deposit and Clear Accumulator (DCA)

Information contained in the AC is deposited in a core memory register specified in a DCA instruction by performance of a fetch, execute 1, program count cycle, and possibly by a defer cycle between the fetch and execute 1 if the instruction designates indirect addressing. The functions performed by the fetch, defer, program count states, and during time state T1 of the E1 state are identical to the functions performed during corresponding cycles and times of the AND instruction.

During T3 of the E1 state the Memory Strobe signal is inhibited so that the MB is settled to receive the new information, the content of the AC is jam transferred into the MB, and the AC is cleared. The MB carry path is disabled from T2 to T5 times to prevent carry pulses from setting adjacent flip-flops if a flip-flop containing a 1 is cleared by the transfer of AC information into the MB. During T5 and T6 the information in the MB is written in the specified core memory register to complete execution of the deposit and clear accumulator operation. During T6 the execute 1 state expires and the program count state is entered to locate the address of the next instruction to be performed.

Jump to Subroutine (JMS)

The JMS is the most complicated instruction performed by the PDP-5. This instruction is performed to store the current program count in a specified address and to transfer program control to the first instruction of a subroutine as contained in the specified address +1. Exit from this subroutine is normally executed by a jump to the specified address which is performed as the final instruction of the subroutine. This JMP instruction transfers program control to the instruction contained in the specified address of the JMS instruction and thus continues the main program with the instruction following the JMS. The JMS is performed by a fetch cycle in which the instruction is brought from memory and placed in the MB and the IR, a defer cycle to locate the effective address if indirect addressing is specified, an execute 1 cycle performed to load the effective address into the MA and to load the MB with the program count, an execute 2 state to increment the program count contained in the MB and to store this incremented PC in the designated core memory address, and a program count state in which the specified core memory address is transferred into the MB to be used as the starting program count for the subroutine. The functions performed during the fetch and defer states of the JMS instruction are identical to those performed during the AND instruction.

During the execute 1 state of the JMS instruction, the address of the operand is set into the MA as a function of the conditions of bits 3 and 4 of the IR in the same manner that these operations occur during the AND instruction. Also during this time state, the MB is cleared and the MA is disabled in preparation for reading the program count from core memory during time states T2 and T3. After the program count is read into the MB it is restored in core memory and the major state is transferred to E2 during T6.

Assuming there is no program interrupt, the E2 state is used to increment the program count stored in the MB and to store this incremented program count in the core memory address specified in the instruction. This is accomplished by inhibiting generation of the Memory Strobe signal so that the program count in the MB (obtained during the E1 state) is not disturbed. Then the content of the MB is incremented by one during T4 and written into core memory during T5 and T6. Also during T6 the E2 state expires and the program count state is set.

The P state is entered with the specified address in the MA and with the incremented program count in the MB. During T1 the 12-bit absolute address containing the program count is jam transferred into the MB. The Memory Strobe signal is inhibited during T3 so that the program count in the MB is not disturbed. During T4 the program count is incremented by one so that the MB now contains the starting address of the subroutine to be retrieved from core memory during the following fetch state. In preparation for the fetch state the IR is cleared during T5 and the fetch state is set during T6.

Jump (JMP)

The JMP instruction is used to transfer program control to an address specified in the instruction. This operation is performed by a fetch cycle. If indirect addressing is indicated, a defer cycle is employed, and the instruction is completed by a program count cycle. The fetch and defer cycles perform functions identical to those performed during execution of the AND instruction. The fetch state is used to load the MB with the instruction specified by the program count and the defer state is used to locate the effective address. The program count state is entered from the defer state with a 12-bit absolute effective address contained in the MB. Since this address is to be taken as the program count for the succeeding instruction, no operations occur during the P state until T4. The program count state is entered from the fetch state with the instruction in the MB and with the current program count in the MA. The content of the MA is modified to form the new program count during T1. This address modification is effected as a function of the content of bit 4 of the instruction. If bit 4 contains a 0, bits 0 through 4 of the MB are cleared. If bit 4 contains a 1, bits 0 through 4 of the MB are jam-set to correspond with bits 0 through 4 of the MB. In any event at the end of T1 the new program count is contained in the MB. Therefore, no program count need be drawn from core memory, so generation of the Memory Strobe pulse is inhibited. No incrementing is performed as a function of the skip flip-flop. As in program count cycles the program count contained in the MB is written into core memory address 0000 during

time states T5 and T6, the IR is cleared during T5, and the fetch state is set during T6. This operation is terminated with the new program count contained in the MB and in the PC.

Input/Output Transfer (IOT)

The IOT instruction is an augmented instruction which can be microprogrammed to address one of 64 devices and supply from one to three time pulses to initiate I/O device operations. During this instruction the processor generates IOP pulses during time states T4, T5, and T6 and supplies them to the device selectors of each peripheral device. The content of bits 3 through 8 of the instruction is used as a device select code that is made directly available to the device selector of all peripheral equipment. When a device selector is enabled by its specific select code, IOP pulses gate generation of correspondingly numbered IOT pulses as a function of binary ones in bits 11, 10, and 9 of the instruction. The IOT pulses, in turn, initiate appropriate operations. The IOT instruction is performed by a fetch cycle followed by a program count cycle.

The fetch state of the IOT instruction is entered with the program count contained in the MB. During time state T1 the program count is transferred from the content of the MB into the MA, the MB is cleared, and the skip flip-flop is cleared. During T2 and T3 the content of the core memory register specified by the program count is read into the MB so that the MB now contains the IOT instruction to be executed. Assuming that no program interrupt occurs, bits 0 through 4 of the MB are transferred into the IR and the instruction is executed during T4, T5, and T6 of the current cycle by generating IOP 1, IOP 2, and IOP 4 pulses respectively. During T5 and T6 the instruction is restored in memory for future use. During T6 the fetch state is concluded by setting the major state generator to the program count state. The functions performed during the program count state of an IOT instruction are identcial to the functions performed during the corresponding state of the AND instruction. As described previously, the program count state disables the MA, clears the MB, and reads the address of the forthcoming instruction from the program counter at locations 0000 into the MB. The P state is concluded by clearing the IR in preparation for receiving the new instruction and setting the fetch state.

Operate (OPR)

The OPR augmented instruction decodes the content of bits 4 through 11 of the instruction in two ways, determined by the content of bit 3. If bit 3 contains a 0, bits 4 through 11 are decoded as an operate group 1 microinstruction; and if bit 3 contains a 1, bits 4 through 11 are decoded as a group 2 operate microinstruction. The decoding of these bits in both operate groups is clearly indicated in Figure 1-3. The instruction is executed during a fetch and a program count state. The fetch state is used to load the instruction into the MB from core memory and to perform the operations specified by bits 4 through 11. The program count state is used to locate the address of the next instruction to be performed in the manner described for the AND instruction.

The functions performed during time states T1, T2, and T3 of the fetch state of the OPR instruction are exactly the same as those performed during any of the instructions described previously. The functions performed during time states T4 and T5 are different from other instructions and can be separated into the two classes as a function of the content of bit 3 of the instruction. If bit 3 contains a 0, an OPR 1 microinstruction is indicated, and bits 4 through 11 are decoded as follows:

a. If bit 4 is a 1, the AC is cleared during T4 (CLA).

b. If bit 5 contains a 1, the link is cleared during T4 (CLL).

c. If bit 6 contains a 1, the content of each bit of the AC is complemented during T5 (CMA).

d. If bit 7 contains a 1, the link flip-flop is complemented during T5 (CML).

e. If bit 8 contains a 1, the content of the AC and the L is rotated one position to the right during T5 (RAR).

f. If bit 9 contains a 1, the content of the AC and the L is rotated to the left one position during T5 (RAL).

g. If bits 8 and 10 both contain ones, the content of the AC and L is rotated one additional place to the right during time state T1 of the following cycle (RTR).

h. If bits 9 and 10 both contain ones, the content of the AC and L is rotate an additional position to the left during time state T1 of the following cycle (RTL).

i. If bit 11 contains a 1, the content of the AC is incremented by one during time state T1 of the ensuing cycle (IAC).

If the instruction contains a 1 in bit 3, an OPR 2 microinstruction is indicated, and bits 4 through 9 are decoded as follows:

a. If bit 4 contains a 1, the content of the AC is cleared during T4 (CLA).

b. If bit 5 contains a 1, the skip flip-flop is complemented (set since the flip-flop is cleared during T1 of the fetch state) during T4 if AC_0 contains a 1, indicating that the accumulator contains a 2's complement negative number (SMA).

c. If bit 6 contains a 1, the skip flip-flop is complemented during T4 if each bit of the AC contains a 0 (SZA).

d. If bit 7 contains a 1, the skip flip-flop is complemented during T4 if the link contains a 1 (SNL).

e. If bit 8 contains a 1, the skip flip-flop is complemented during T5 to reverse the sense of skipping for microinstructions containing ones in bits 5 through 7.

f. If bit 9 contains a 1, the content of the switch register is transferred into the accumulator during T5 (OSR).

g. If bit 10 contains a 1, the run flip-flop is cleared during T5 (HLT).

During time state T6 the fetch state expires and the major state generator is set to the P state. However, if a Break Request signal is present, the fetch state is followed by a break state. Therefore, the operations performed by the OPR 1 microinstructions having binary ones in bits 8 through 11 are normally performed during the P state but might also be performed during a break state.

Program Interrupt

Peripheral equipment connected to the program interrupt bus can cause an unscheduled JMS instruction to be executed during the running of the main program. Program interrupts initiated by grounding of the program interrupt bus allow the instruction in process at the time to be completely executed; then a JMS to address 0001 instruction is forced so that the current program count is stored at location 0001 and program control is transferred to 0002. The instruction

stored in core memory address 0002 is executed next as the first instruction of a program interrupt subroutine. The program interrupt subroutine is responsible for finding the peripheral equipment causing the interrupt, performing any necessary service to the I/O device, enabling the program interrupt synchronization element for another program interrupt, and returning to the original program. Enabling of the program interrupt synchronization element is accomplished by an ION microinstruction (IOT 6001), and exit from the subroutine back to the original program can be accomplished by a JMP I 1 instruction. This mode of operation is used to expedite the transfer of information to I/O devices by allowing alarm conditions to be checked by a subroutine initiated by them rather than by a program which checks them periodically.

If the program interrupt synchronization element is enabled by prior performance of the ION microinstruction (IOT 6001) and a peripheral device supplies a program interrupt request, the program interrupt synchronization element generates the Interrupt Acknowledge signal.

Generation of the Interrupt Acknowledge signal immediately clears the interrupt synchronization element by automatically performing the operations accomplished by the IOF microinstruction (IOT 6002) so that no additional interrupt requests are honored during the interrupt subroutine (until an ION microinstruction is performed). Generation of the Interrupt Acknowledge signal is delayed so that the interrupt does not occur until T5 of the next P state of the program in progress at the time the request is received. Therefore, the program count is the only factor that must be saved to reinstitute the main program following completion of the program interrupt subroutine.

All operations performed during the P state prior to the interrupt are normal for the execution of instructions. During T1 of the following fetch state, the program count is transferred from the MB into the MA, and the MB and skip flip-flop are cleared. The normal instruction is drawn from core memory and stored in the MB during T2 and T3; however, transfer of this instruction into the IR is inhibited, and IR_0 is set to force a JMS instruction. The instruction drawn from memory during T2 and T3 is rewritten during T5 and T6, and the major state generator is set to the execute 1 state during T6 (since IR_3 contains a 0 as a result of clearing during T5 of the previous P state).

During the E1 state the MA and MB are cleared, and the MA is disabled during T1. During T2 and T3 the program count is read from core memory into the MB and is rewritten during T5 and T6. During T6 the major state generator is set to the execute 2 state.

During T1 of the E2 state the MA is incremented by one to establish address 0001. The Memory Strobe pulse is inhibited during the core memory read cycle, and the program count contained in the MB is written into address 0001 during T5 and T6. During T6 the int ack flip-flop of the program interrupt synchronization element is cleared and the major state generator is set to the P state.

During the program count state address 0001 is transferred from the MA into the MB during T1. Memory Strobe pulse generation is inhibited during T3 so that no core memory reading operation takes place. During T4 the content of the MB is incremented by one (since the skip flip-flop has remained cleared since T1 of the previous fetch state) so that it now contains address 0002 which serves as the program count for the succeeding fetch state. The IR is cleared at T5 and the major state generator is set to the fetch state during T6 to complete the operations of the program count cycle and the program interrupt mode. Exit from this mode leaves a program count of 0002 in the MB for transferring to the MA during T1 of the succeeding fetch cycle to transfer program control to that address, and the current program count is stored in core memory register 0001 to provide a return to the original program at the conclusion of the subroutine.

Data Break

One external device can be connected directly to the data break facility or up to four devices can be connected to it through the Type 129 Data Channel Multiplexer.

Peripheral equipment connected to the data break facility can cause a pause in the program in progress to transfer information between the device and core memory, via the MB. This mode of operation provides a high speed transfer of blocks of information at sequential core memory addresses or at addresses individually specified by the device. Since program execution is not involved in these transfers, the program counter is not disturbed or involved in these transfers. The program is merely suspended at the conclusion of an instruction execution, and the break state is entered to perform the transfer; then the program count state is entered to continue the main program. The timing of signals involved in a data break is indicated in Figure 5-1.

To initiate a data break, an I/O device must supply three signals simultaneously to the data break facility. These signals are the Break Request, which sets a flip-flop in the major state generator to control entry into the break state; a Transfer Direction signal, supplied to the MB

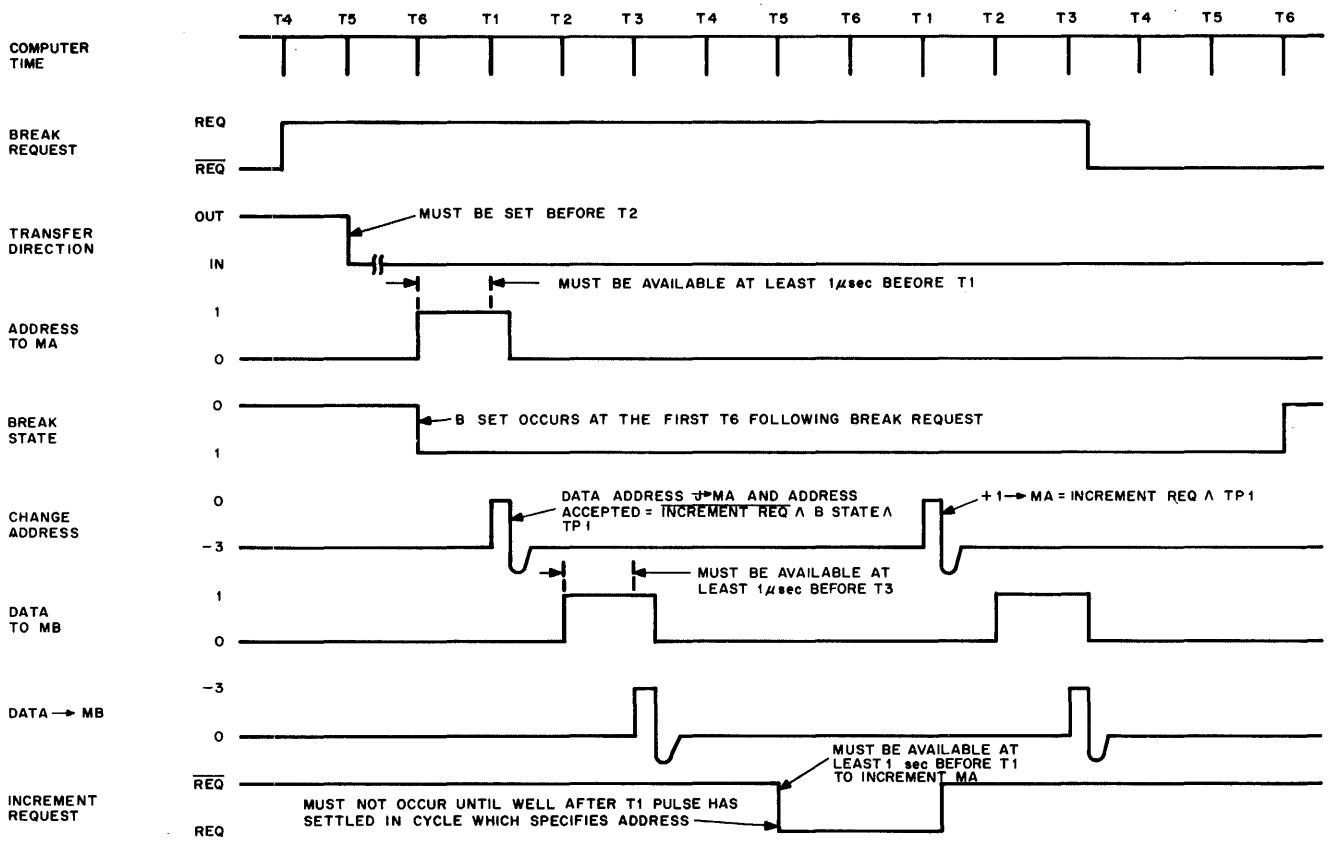


Figure 5-1 Data Break Timing

control element to allow generation of the Data ⟶ MB signal which strobes data into the MB from the peripheral equipment and inhibits generation of the Memory Strobe pulse; and an address of the transfer which is supplied to the gating circuits at the input of the MA. When the break request is made, the break state is set into the major state generator prior to entry into the program count state of an instruction. Therefore, the break state is entered at the conclusion of the execute 1 state of all memory reference instructions and at the conclusion of a fetch state for augmented instructions. Having established the break state, each machine cycle is a break cycle until all data transfers have taken place, as indicated by removal of the Break Request signal by the peripheral equipment. Each computer cycle can be used to transfer a data word at addresses specified to the input gating circuits of the MA by the peripheral equipment or can be specified initially by the peripheral equipment and then occur at sequential addresses by application of an Increment Request signal to the MA control element. This signal allows generation of the Count MA signal to increment the content of the MA during T1 of each break cycle. Entry into the break cycle is indicated to the peripheral equipment by means of an Address Accepted pulse so that the device can initiate internal operations involved in the

transfer and supply data to the input gating circuits of the MB. The Address Accepted pulse supplied to the external device is designated the Data Address —J►MA pulse within the PDP-5. Data is strobed into the MB by a Data ——►MB signal produced during time state T3.

The operations performed during each computer cycle in the break state are shown on the engineering flow diagram. During T1 the data supplied to the gating circuits at the input of the MA is strobed into the MA if the Increment Request signal is not present, or the content of the MA is incremented by one if the Increment Request signal is supplied by the external device. Also during T1 the MB is cleared in preparation for receipt of data from either the core memory or the external device. If the Transfer Direction signal establishes the transfer direction as out of the computer, the content of the core memory register at the address specified during T1 is transferred into the MB during time states T2 and T3 and is immediately available for strobing by the peripheral equipment. If the Transfer Direction signal specifies a data direction into the PDP-5, generation of the Memory Strobe signal is inhibited and the Data ——►MB signal is generated to transfer information into the MB from signals supplied by the peripheral equipment. Data read from core memory during T2 and T3 is restored in core memory or the data set into the MB during T3 is stored in core memory during T5 and T6. The Break Request signal is sampled again at T6 to determine if additional break cycles are needed. If the Break Request signal is still present, the B Set signal is produced to maintain the break state of the major state generator. If the Break Request signal is not present at this time, the program count state is set into the major state generator to complete the data break operation.

SECTION 6

INTERFACE

All logic signals which pass between the PDP-5 computer and the input/output equipment are standard DEC levels or standard DEC pulses. A standard DEC level is either ground potential (0.0 to -0.3 volts) or -3 volts (-3.0 to -4.0 volts). Standard DEC pulses are 2.5 volts in amplitude (2.3 to 3.0 volts) and are referenced to ground potential. The standard pulse duration is 70 nanoseconds for pulses originating in Series 1000 modules and 400 nanoseconds for Series 4000 modules.

Three 50-terminal Amphenol 115-114S cable connectors are available on the connector panel (1J01-1J03) for connection to I/O devices. Interface connections to 1J01 and 1J02 are used in normal programmed information transfers between the PDP-5 and peripheral equipment. Connections to 1J03 are used for data and control signals transferred in the data break mode. Corresponding terminals of 1J01 and 1J02 are connected together and routed to signal origins or destinations in the machine logic. Additional connector locations (1J04-1J06) are available for installation of connectors, as needed. Wiring to a new signal connector can be planned for bus connection to either 1J02 or 1J03, so direct connection to the logic is not necessary. It is suggested that bus connections be made from all terminals of existing connectors to all terminals (used and unused in the device being added) of new connectors. In this manner the bus connections can be maintained for all future expansions of the system. Connections to the interface connectors are summarized in Table 6-1 for input signals and in Table 6-2 for output signals.

TABLE 6-1 INPUT SIGNALS

Signal	Symbol	Connector Terminals		Destination	Logic	BS Drawing
		Programmed	Data Break			
AC^1_0	⟶▷	1J01-13	---	1E16E	IM	14
AC^1_1	⟶▷	1J01-14	---	1E16F	IM	14
AC^1_2	⟶▷	1J01-15	---	1E16H	IM	14
AC^1_3	⟶▷	1J01-16	---	1E16J	IM	14
AC^1_4	⟶▷	1J01-17	---	1E16K	IM	14
AC^1_5	⟶▷	1J01-18	---	1E16L	IM	14
AC^1_6	⟶▷	1J01-19	---	1E16M	IM	14
AC^1_7	⟶▷	1J01-20	---	1E16N	IM	14
AC^1_8	⟶▷	1J01-21	---	1E16P	IM	14
AC^1_9	⟶▷	1J01-22	---	1E16R	IM	14
AC^1_{10}	⟶▷	1J01-23	---	1E16S	IM	14
AC^1_{11}	⟶▷	1J01-24	---	1E16T	IM	14
Skip	⟶▷	1J01-25	---	1D03E	Skip Control	8
Prog. Interrupt	⟶◇	1J01-26	---	1E04Y	Prog. Int'pt Sync.	8
MB^1_0	⟶◇	---	1J03-13	1B02V	MB	9

TABLE 6-1 INPUT SIGNALS (continued)

Signal	Symbol	Connector Terminals		Destination	Logic	BS Drawing
		Programmed	Data Break			
MB^1_1	—◇	---	1J03-14	1B03V	MB	9
MB^1_2	—◇	---	1J03-15	1B04V	MB	9
MB^1_3	—◇	---	1J03-16	1B05V	MB	9
MB^1_4	—◇	---	1J03-17	1B06V	MB	9
MB^1_5	—◇	---	1J03-18	1B07V	MB	9
MB^1_6	—◇	---	1J03-19	1B08V	MB	9
MB^1_7	—◇	---	1J03-20	1B09V	MB	9
MB^1_8	—◇	---	1J03-21	1B10V	MB	9
MB^1_9	—◇	---	1J03-22	1B11V	MB	9
MB^1_{10}	—◇	---	1J03-23	1B12V	MB	9
MB^1_{11}	—◇	---	1J03-24	1B13V	MB	9
Data Addr. 0	—◇	---	1J03-26	1B02R	MA	9
Data Addr. 1	—◇	---	1J03-27	1B03R	MA	9
Data Addr. 2	—◇	---	1J03-28	1B04R	MA	9
Data Addr. 3	—◇	---	1J03-29	1B05R	MA	9
Data Addr. 4	—◇	---	1J03-30	1B06R	MA	9

TABLE 6-1 INPUT SIGNALS (continued)

Signal	Symbol	Connector Terminals		Destination	Logic	BS Drawing
		Programmed	Data Break			
Data Addr. 5	—◇	---	1J03-31	1B07R	MA	9
Data Addr. 6	—◇	---	1J03-32	1B08R	MA	9
Data Addr. 7	—◇	---	1J03-33	1B09R	MA	9
Data Addr. 8	—◇	---	1J03-34	1B10R	MA	9
Data Addr. 9	—◇	---	1J03-35	1B11R	MA	9
Data Addr. 10	—◇	---	1J03-36	1B12R	MA	9
Data Addr. 11	—◇	---	1J03-37	1B13R	MA	9
Increment MB	—▷	---	1J03-38	1B13X	MB	9 (sheet 2)
Break Request	—◇	---	1J03-43	1D16X	Major State Gen.	6
Transfer Direction	—◆ *	---	1J03-44	1C17S	MB Control	7
Increment Request	—◆	---	1J03-45	2C11F	MA Control	7
I/O Halt	—▶	1J01-46	---	1D12Y	I/O Halt Control	5
Clear AC	—▷	1J01-47	---	1C01F	AC Control	8
Restart	—▶	1J01-48	---	1E02W	Run Control	5
Ground	⏚	1J01-50	1J03-50	---	---	---

*Into PDP-5 when -3 volts, out of PDP-5 when ground.

TABLE 6-2 OUTPUT SIGNALS

Signal	Symbol	Connector Terminals		Bus Driver Output	Origin	Logic	BS Drawing
		Programmed	Data Break				
AC^1_0	—◇	1J01-1	---	1F06L	1B02E	AC	9
AC^1_1	—◇	1J01-2	---	1F06N	1B03E	AC	9
AC^1_2	—◇	1J01-3	---	1F06T	1B04E	AC	9
AC^1_3	—◇	1J01-4	---	1F06R	1B05E	AC	9
AC^1_4	—◇	1J01-5	---	1F07L	1B06E	AC	9
AC^1_5	—◇	1J01-6	---	1F07N	1B07E	AC	9
AC^1_6	—◇	1J01-7	---	1F07T	1B08E	AC	9
AC^1_7	—◇	1J01-8	---	1F07R	1B09E	AC	9
AC^1_8	—◇	1J01-9	---	1F08L	1B10E	AC	9
AC^1_9	—◇	1J01-10	---	1F08N	1B11E	AC	9
AC^1_{10}	—◇	1J01-11	---	1F08T	1B12E	AC	9
AC^1_{11}	—◇	1J01-12	---	1F08R	1B13E	AC	9
MB^1_0	—◇	---	1J03-1	1F12L	1B02K	MB	9
MB^1_1	—◇	---	1J03-2	1F12N	1B03K	MB	9
MB^1_2	—◇	---	1J03-3	1F12T	1B04K	MB	9

TABLE 6-2 OUTPUT SIGNALS (continued)

Signal	Symbol	Connector Terminals		Bus Driver Output	Origin	Logic	BS Drawing
		Programmed	Data Break				
MB_3^0	—◇	1J01-28	---	1F09L	1B05L	MB	9
MB_3^1	—◇	1J01-27	1J03-4	1F09N	1B05K	MB	9
MB_4^0	—◇	1J01-30	---	1F09T	1B06L	MB	9
MB_4^1	—◇	1J01-29	1J03-5	1F09R	1B06K	MB	9
MB_5^0	—◇	1J01-32	---	1F10L	1B07L	MB	9
MB_5^1	—◇	1J01-31	1J03-6	1F10N	1B07K	MB	9
MB_6^0	—◇	1J01-34	---	1F10T	1B08L	MB	9
MB_6^1	—◇	1J01-33	1J03-7	1F10R	1B08K	MB	9
MB_7^0	—◇	1J01-36	---	1F11L	1B09L	MB	9
MB_7^1	—◇	1J01-35	1J03-8	1F11N	1B09K	MB	9
MB_8^0	—◇	1J01-38	---	1F11T	1B10L	MB	9
MB_8^1	—◇	1J01-37	1J08-9	1F11R	1B10K	MB	9
MB_9^1	—◇	---	1J03-10	1F13L	1B11K	MB	9
MB_{10}^1	—◇	---	1J03-11	1F13N	1B12K	MB	9
MB_{11}^1	—◇	---	1J03-12	1F13T	1B13K	MB	9

TABLE 6-2 OUTPUT SIGNALS (continued)

Signal	Symbol	Connector Terminals		Bus Driver Output	Origin	Logic	BS Drawing
		Programmed	Data Break				
IOP 1**	---	1J01-39	---	---	1D25J	IOP Pulse Gen.	6
IOP 1	→	1J01-40	---	---	1D25H	IOP Pulse Gen.	6
IOP 2**	---	1J01-41	---	---	1D25R	IOP Pulse Gen.	6
IOP 2	→	1J01-42	---	---	1D25P	IOP Pulse Gen.	6
IOP 4**	---	1J01-43	---	---	1D25X	IOP Pulse Gen.	6
IOP 4	→	1J01-44	---	---	1D25W	IOP Pulse Gen.	6
1MC Clock	→	1J01-45	---	---	1C24V	Timing Signal Gen.	17
Power Clear	→	1J01-49	1J03-47	---	1E05E	Power Clear Gen.	5
TP 4	→	---	1J03-39	---	1C24S	Timing Signal Gen.	17
TP 5	→	---	1J03-40	---	1C24J	Timing Signal Gen.	17
Break	◆→	---	1J03-41	1F12R	1D20T	Major State Gen.	6
Run	◆→	---	1J03-42	1F13R	1D01U	Run Control	5
SP 0	→	---	1J03-46	---	1E06E	SP Gen.	5
Data → MB	▷	---	1J03-48	---	1C12N	MB Control	7
Address Accepted	▷	---	1J03-49	---	1C13F	MA Control	7
Ground	⏚	1J01-50	1J03-50	---	---	---	---

**Ground side of pulse transformer secondary winding

LOADING AND DRIVING DEFINITIONS

The following definitions and rules serve as a useful guide in determining the driving capability of output signals and the load presented to input signals by the PDP-5.

Base Load

Base load is the current which must be drawn from the base of a dc inverter to keep it saturated. In this condition the inverter circuit input terminal is at -3 volts, the emitter is at ground, and a nominal 1 milliampere of current flows through the 3000-ohm base resistor from ground. A 1500-ohm load resistor clamped at -3 volts can nominally accept 8 milliamperes, but tolerance considerations limit this number to 7 milliamperes. Thus, an inverter collector with a 1500-ohm clamped load can drive a maximum of 7 base loads.

Pulse Load

Pulse load is the load presented to the output of a pulse source by an inverter base in the same speed series, or by the direct set or clear input of a flip-flop. Pulse amplifiers are usually limited to driving 16 pulse loads. This number should be decreased if the bases are widely separated physically, and can be increased to 18 if the bases are all physically close together. The series inductance and shunt capacity of connecting wires can make pulses at the end of a series of bases either large or small. Consequently, when driving nearly the maximum number of bases, the pulse amplitude should be carefully checked after installation. A terminating resistor in the 100-to-300 ohm range is desirable to reduce ringing on a heavily loaded pulse line. The loading on a pulse source is approximately the same when driving a base as a direct input to a flip-flop. One pulse source, of course, cannot drive both direct inputs of flip-flops and inverter bases because the direct inputs require DEC standard positive pulses and base inputs require DEC standard negative pulses. A pulse load is largely determined by the value of the speed-up capacitor connected in parallel with the 3000-ohm base resistor. In the 4000 Series 500 kc modules this capacitor is 680 pf; in 1000 Series 5 mc modules it is 82 pf; and in 6000 Series 10 kc modules it is 56 pf.

Pulsed Emitter Load

Pulsed emitter load is the load applied to the collector of an inverter which drives the pulse input to a flip-flop, pulse amplifier, or delay. The pulse current passes through all of the inverters in series with the pulse input, and it should be assumed to be the load on each of the series inverters.

DC Emitter Load

The load applied to the collector of an inverter driving a clamped load resistor is the dc emitter load. This load is also presented by the collector of an inverter which drives an emitter in an inverter network terminated by a clamped load resistor. Under these conditions, the collector of an inverter driving an emitter in a transistor gating network must also supply the base current leaving the succeeding inverters which are saturated. This current is small, but in complex networks it must be considered. An inverter in the DEC 1000 or 6000 Series modules can supply 15 milliamperes, and in the 4000 Series modules can supply 20 milliamperes.

An inverter network can always be analyzed by assuming:

a. that a short circuit exists between the emitter and collector when -3 volts is applied to the base.

b. that 1 milliampere of base current will flow if either the collector or emitter is held at ground potential.

c. that the maximum dc collector current through an inverter is 20 milliamperes for 4000 Series 500-kc modules and is 15 milliamperes for all other DEC series modules.

A capacitor-diode gate level input does not present any dc load. A transient load occurs when the input level changes. Note that all capacitor-diode gates in the standard PDP-5 require that the level input precede the initiating pulse input by at least 1 microsecond.

POWER CLEAR GENERATOR (5)

The Power Clear pulses generated and used within the PDP-5 are made available to both the programmed and data break interface connections. External equipment can make use of these pulses to clear registers and control logic during the power turn on period. Use of the Power Clear pulses in this manner is valid only when the logic circuits cleared by them are energized under the control of, or in synchronism with, the 832 Power Control in the PDP-5.

The Power Clear pulses are DEC standard negative 0.4 microsecond pulses produced during the the first 5 to 10 seconds after the POWER switch is turned on. These pulses are generated at approximately a 500-kc rate by the 4401 Variable Clock module at location 1E05. Interface cable connections to the Power Clear pulses can drive 15 pulse loads.

When an I/O device is mounted within the main PDP-5 cabinet or in cabinets bolted to it, the normal wiring practice is to use a single source of primary power and a single power control. When the I/O device is external to the PDP-5 and utilizes a separate source of primary power, a separate cable can be used to connect the power controls of the PDP-5 and the device. This connection can be made to allow contact operations in the computer power control to cause similar operations in the I/O device power control. Under these conditions an I/O device can make effective use of the Power Clear pulses.

SPECIAL PULSE GENERATOR (5) AND TIMING SIGNAL GENERATOR (17)

Four timing pulses used in the PDP-5 are supplied to I/O devices using the data break facility. These signals can be used to synchronize operations in external equipment with the computer. The 1-mc clock, TP4, and TP5 pulses are produced by 4604 Pulse Amplifier modules, and the SP0 pulse is produced by the 4410 Pulse Generator module at location 1E06. All of these signals are standard DEC negative 0.4-microsecond pulses. The 1-mc clock pulse output can drive 15 pulse loads; and the TP4, TP5, and SP0 pulse outputs can each drive 5 pulse loads.

RUN AND I/O HALT CONTROL (5)

Run

The 1 output of the run flip-flop is supplied to external equipment using the data break. This signal is at -3 volts when the computer is performing instructions, and is at ground potential

when the program is halted. Magnetic tape and DECtape equipment make use of this signal to stop transport motion when the PDP-5 halts, and thus prevent the tape from running off the end of a reel. The signal is routed to the interface connector via contacts of the dummy plug at location 1F13. With the dummy plug in the circuit, this signal can drive 1 base load. With the dummy plug replaced by a 1684 Bus Driver module this signal is capable of driving 15 5-mc base loads at 500 kc or 8 500-kc base loads at 500 kc or 15 500-kc base loads at lower frequencies. It can supply a maximum current of ±15 milliamperes.

I/O Halt and Restart

The I/O halt facility provides a means of halting the advance of the program for an undetermined length of time while an I/O device executes a programmed operation. A specific IOT instruction is decoded in the device selector of an I/O equipment to produce IOT pulses which initiate device operation and return to the PDP-5 as an I/O Halt pulse. The I/O Halt pulse sets the I/O-hlt flip-flop, which in turn clears the run flip-flop, so that the program stops. When the I/O device completes the operation specified by the IOT instruction, it supplies a Restart pulse to the PDP-5 which returns the run flip-flop to the 1 state to continue the program and clears the I/O-hlt flip-flop.

I/O Halt pulses are received by a 4116 Diode module at location 1D12 which functions as a negative NOR gate. When it is at ground potential, the inverted output of this gate sets the I/O-hlt flip-flop. This flip-flop is contained in the 4215 module at location 1D01. When the I/O-hlt flip-flop is set, the positive transition of the 1 output clears the run flip-flop. The run flip-flop is also contained in the module at location 1D01.

I/O Halt pulses must be standard DEC negative pulses (0.4 microseconds) or equivalent. The dc load presented to the signal by the input is 1/8 dc emitter load. This load is shared by those inputs which are at ground. The transient load presented to a pulse input is 1 pulse load.

Restart pulses are received at the pulse input of a 4129 (negative) Capacitor-Diode Gate at location 1E02 and at the 4116 Diode module at location 1D12. The conditioning level input to this capacitor-diode gate is provided by the 1 status of the I/O-hlt flip-flop. The Restart pulse may be driven from a standard DEC 0.4 microsecond negative pulse, or equivalent

source having a negative-going level change from 2.5 to 3.3 volts, with a maximum fall time of 0.4 microseconds. This input represents 3 pulse loads and 1/8 dc emitter load.

MAJOR STATE GENERATOR (6)

Break Request

The break state is entered to transfer information between a peripheral device and the core memory via the memory buffer register. This state is entered only after a ground-level Break Request signal is supplied to the computer by the external device. The signal is buffer inverted and supplied to one input of a 2-input negative NAND diode gate in the 4113 module at location 1D15. The second input to this gate is the TP4 pulse that strobes the Break Request signal into a synchronizing flip-flop. This flip-flop is cleared during T3 of each cycle so the Break Request signal must be present during T4 of the cycle in which the break state is entered. Entry into the break state occurs during T6 of the cycle preceding the program count cycle of the instruction in progress when the Break Request signal is present. The major state generator presents one base load to the Break Request signal source.

Break

When the computer is in the break state, a negative signal level is supplied to external devices. This signal is at -3 volts when the computer is in the break state and is often logically combined with a timing pulse to initiate operations in an I/O device. Generated in diode gate circuits, this signal is supplied to the interface connector through the dummy plug at location 1F12. With the dummy plug in the circuit this signal can drive 1 base load. With the dummy plug replaced by a 1684 Bus Driver module, the signal can supply ±15 milliamperes and can drive a load as described for the Run signal.

MEMORY ADDRESS REGISTER CONTROL (7)

Address Accepted

During T1 of each cycle during the break state, the PDP-5 produces a standard DEC positive pulse when the externally supplied address is strobed into the MA. The Address Accepted

pulse is produced by the same pulse amplifier circuit on the 4603 module at location 1C13 which triggers the input capacitor-diode gates of the MA. This signal output can drive four pulse loads.

Increment Request

An Increment Request signal is used to determine the signals produced by the memory address register control element during each break cycle. If this signal is at ground potential, the Data Address —J→ MA pulse is produced during T1 of the break state to strobe an address into the MA from signals supplied to it externally. If this signal is at -3 volts, indicating a request to increment the transfer address by one, the MA Carry Enable signal is generated during the entire break cycle, and the Count MA pulse is produced during T1 to increment the content of the MA. If the address is to be supplied to the MA by an I/O device, the Increment Request signal should be at ground potential during computer time state T1. If the address is to be incremented by one, the Increment Request signal must be at -3 volts during and for approximately 1 microsecond prior to T1. The signal is received as one input to a 2-input negative NAND diode gate on the 4113 module at location 1C11 and by an inverter on the 4102 module at location 1C16. The gate is conditioned by the Break signal to enable generation of the MA Carry Enable signal and the Count MA pulse. The inverter output is also supplied to a 2-input negative NAND diode gate conditioned by the Break signal. The output of this latter gate enables generation of the Data Address —J→ MA pulse. The PDP-5 presents one base load to the Increment Request signal.

MEMORY BUFFER REGISTER CONTROL (7)

Transfer Direction

A Transfer Direction signal must be supplied to the computer before and during computer time states T2 and T3 of a break state to determine the read or write status of the memory. At ground potential this signal designates transfer from the core memory to the I/O device, and at -3 volts the signal specifies transfer into core memory from an external device. This signal must be at ground potential before T2 or no Memory Strobe pulse is produced and data cannot be transferred out of core memory. If the signal is at -3 volts, the Data ——→ MB pulse is

produced during T3 and the data supplied to the MB inputs is strobed into the MB flip-flops. This Transfer Direction signal is received by one input of a 2-input negative NAND diode gate in the 4113 module at location 1C17. The second input to the gate is provided by the Break signal so that the direction signal has effect only when the computer is in the Break state. This input presents 1/8 emitter load upon the Transfer Direction signal source.

Data ⟶ MB

During a data break in which the direction of transfer is into core memory, this pulse signal can be used as an indication that the data has been strobed into the MB, and the device register supplying the data can be changed. This signal is a standard DEC positive pulse of 0.4-microsecond duration, produced during computer time state T3 by the 4603 Pulse Amplifier module at location 1C12. Four pulse loads can be driven by this signal.

ACCUMULATOR CONTROL (8)

Clear AC

Input connection to the PDP-5 is provided to allow a programmed I/O device to clear the accumulator. An external device supplying information to the computer input mixer can assure that the word being read into the AC is not transferred in over an existing word by clearing the AC prior to strobing the IM. Transferring a word into the AC from the IM without clearing the AC first, results in the inclusive OR of the new word with the previous word being held in the accumulator after the transfer. The Clear AC signal initiates operation of the 4606 Pulse Amplifier module at location 1C01 by driving the input terminal to ground. A standard DEC positive pulse or a positive-going transition of from 2.5 to 4.0 volts, with a rise time less than 0.4 microsecond and a duration greater than 70 nanoseconds, supplied to this input triggers the pulse amplifier. This connection presents one pulse load to the pulse source.

Address Accepted

During time state T1 of each break state cycle, the PDP-5 produces a standard DEC positive pulse when the address upplied externally is strobed into the MA. This Address Accepted pulse

is produced by the same pulse amplifier circuit on the 4603 Pulse Amplifier module at location 1C13 which triggers the input capacitor-diode gates of the MA. This signal output can drive four pulse loads.

MEMORY ADDRESS REGISTER (9)

Data Address signals supplied to the PDP-5 during data break operations to designate a transfer address condition a pair at ground-potential capacitor-diode gates at the input of each MA flip-flop. A Data Address signal is applied directly to the gate at the 1 input and is applied to the gate at the 0 input through an inverter, therefore providing a jam transfer. These gates require a 1 microsecond set up time and are triggered during computer time state T1. Therefore, the Data Address signals must be supplied during T6 of the cycle preceding the break state. To assure this timing, these signals should be presented concurrent with the Break Request signal. Each Data Address connection presents one base load to the signal source in the I/O device.

MEMORY BUFFER REGISTER (9)

MB Outputs

Bits 3 through 8 of an IOT instruction held in the MB are used to select the I/O device addressed by the instruction. Complementary output signals from flip-flops MB_{3-8} supply the input to each device selector module. When the device selector is located within the I/O device, these MB lines must be connected through an interface connector. During the data break, 12-bit words are transferred between core memory and an I/O device, via the MB. The binary 1 output of each MB flip-flop is available at the data break interface connector for these transfers.

Memory buffer register outputs are wired from their point of origin in a 4206 Triple Flip-Flop module at locations 1B02 through 1B13 to module connectors at 1F09 through 1F13. Normally, locations 1F09 through 1F13 contain dummy plugs with jumpers between terminals corresponding to the inputs and outputs of a 1684 Bus Driver module. Therefore, when sufficient device selectors are added to the system or when a device which utilizes the data break draws sufficient current to overload the normal driving capabilities of the 4206 modules, these dummy plugs can be replaced by 1684 Bus Driver modules. Each 4206 output can drive four 4605 Pulse Amplifier

modules in device selectors. When the bus drivers are inserted in the system, each MB signal can drive at least 12 device selector modules, since a 1684 module can supply ±15 milliamperes, and each device selector module requires 1.25 milliamperes shared among the grounded inputs. Under most circumstances, a single 1684 module output can drive more than 12 device selector modules because the load presented by a 4605 module is shared by all of the 1684 modules that drive it. The maximum number of 4605 modules which can be driven by 1684 modules is determined by the condition where the minimum number of driver circuits hold the maximum number of outputs at ground level. Under this condition, the current delivered by each driver circuit in a 1684 module is equal to 1.25 milliamperes multiplied by the number of loads, divided by the number of driver circuits. This current must not exceed 15 milliamperes per driver circuit.

Data Bit Inputs

Input connections to the MB are also made at the data break interface connector. These connections are made to the Data Bit level input of the ground-potential capacitor-diode gate in each 4206 module. Therefore, these inputs present no dc load.

These gates require a 1-microsecond set-up time and are strobed during computer time state T3. Data Bit signals must, therefore, be present during T2 and T3.

Increment MB

A signal input connection is provided to allow an external device using the data break facility to increment the content of the MB. This connection is used in pulse-height analysis and time-of-flight applications. This signal triggers the ground-level capacitor-diode gate at the complement input to flip-flop MB_{11} if the gate has been conditioned for at least 1 microsecond by the MB Carry Enable signal level. Therefore, this gate is enabled during T2, T3, and T4 of each computer cycle except the execute 1 state of the DCA instruction. The Increment MB signal input connection represents one emitter load.

ACCUMULATOR (9) AND INPUT MIXER (14)

AC Outputs

Data contained in the AC is available as static levels to supply information to I/O devices. These static levels can be strobed into an I/O device register by IOT pulses from the associated device selector. The static output signal level of each AC flip-flop is at -3 volts when the bit contains a binary 0 and ground potential when that bit contains a binary 1.

Accumulator outputs are wired from their point of origin in a 4206 Triple Flip-Flop module to connectors at locations 1F06, 07, and 08. Normally these locations contain dummy plugs which jumper terminals corresponding to the inputs and outputs of a 1685 Bus Driver module. When sufficient I/O devices are connected to the AC output to overload the 4206 modules, these dummy plugs can be removed and replaced by 1685 Bus Driver modules. With the dummy plugs in the system, each AC output signal is capable of driving six 1500-ohm capacitor-diode gate level inputs, or ten 5-mc base loads, or six 500-kc base loads, or two dc emitter loads. With the dummy plugs replaced by bus drivers, each AC output signal is capable of driving 100 1500-ohm capacitor-diode gate level inputs, or 15 base loads, or 12 negative NOR diode gates.

Each driver circuit of a 1685 module can supply ±15 milliamperes. The rise and fall times of the output signals are approximately 1 microsecond. For more than a 5000-picofarad output load, the maximum rise of fall time, in microseconds, is equal to the capacitance in picofarads divided by 5000. Maximum rise or fall time of a bus driver output should be limited to 10 microseconds.

AC Inputs

Data transferred from an I/O device to the PDP-5 is received at the input mixer and transferred to the accumulator input. The AC input is accessible to I/O devices only through a pulse input to the 4130 Capacitor-Diode Gate modules at locations 1E10 through 1E15 which comprise the IM. The level input to these gates is permanently connected to system ground, and the pulse input is clamped at -3 volts by the 1000 Clamped Load Resistor module at location 1E16. Therefore, gated register outputs from many I/O devices can be connected to the pulse inputs of the IM, so that programmed IOT pulses set the information into the AC of the PDP-5.

Driving an IM input connection point to ground potential sets a 1 into the corresponding AC flip-flop. The input signal change should be a maximum of 0.5 volts to avoid setting a flip-flop to a 1, and must be at least 2 volts with a rise time of less than 0.3 microseconds to reliably set a 1 into the AC. Each input presents a load of one standard clamped load resistor in parallel with 330 picofarads to ground.

SKIP CONTROL (8)

A skip bus is available for input connections to the PDP-5 from gated Skip pulses generated in I/O equipment. Input Skip pulses are usually produced by a flag or device status level which is strobed or sampled by an IOT pulse. The IOT pulse from the device selector strobes the flag; and if it is in the preselected binary condition, the instruction following the IOT is skipped.

These input pulses provide the complement input to the skip flip-flop, which is one of the four circuits on the 4215 4-Bit Counter module at location 1D03. Within the computer, this point is clamped at -3 volts by the collector load resistor of a 4129 Negative Capacitor-Diode Gate at location 1C04.

To cause an instruction to be skipped, the skip bus must be driven to ground potential for 0.4 microsecond by a pulse with a rise time of less than 0.2 microsecond. This pulse must originate in a high-impedance source, such as a transistor in a standard DEC inverter, diode gate, or capacitor-diode gate. The source of the Skip pulse cannot exhibit more than 1000 picofarads for the driving transistor.

IOP PULSE GENERATOR (6)

The IOP 1, 2, and 4 pulses trigger pulse amplifiers in the selected device selector located in peripheral equipment. These pulses are produced in a 4606 Pulse Amplifier module in location 1D25 and are routed by twisted-wire pairs to the appropriate input terminals of all 4605 Pulse Amplifier modules in the PDP-5 system. Each IOP pulse can drive 16 pulse amplifiers in 4605 modules.

PROGRAM INTERRUPT SYNCHRONIZATION (6)

Signals from I/O devices which interrupt the program in progress are connected to a bus on the PDP-5. Connections to this bus must be in the form of static levels: ground potential to interrupt, -3 volts for no effect. The Program Interrupt signal is clamped at -3 volts by the collector load of the 4114 Diode NOR module at location 1D04, is inverted and isolated by the 4102 module at location 1E04, and is supplied to one input of the 4115 Diode NAND module at location 1D05 as the primary condition for initiating the internal interrupt gate. Connection to the program interrupt bus represents 1 dc emitter load. The maximum total leakage current from all sources connected to the bus must not exceed 6 milliamperes

DEVICE SELECTOR (RS-4605)

The device selector function is performed by a 4605 Pulse Amplifier module for each I/O device or external register which is individually selected. Each I/O device added to the system must contain a 4605 module which has been prepared to select the device for a given combination of bits 3 through 8 of an IOT microinstruction. When selected in this manner, a 4605 module produces IOT pulses (related to the IOP pulses) in accordance with the presence of binary ones in bits 9, 10, and 11 of the IOT microinstruction. These IOT pulses, in turn, must be wired to initiate operations in the I/O device or can be returned to the computer as I/O Skip, I/O Halt, Restart, etc. signals.

Cable connections must supply inputs to each 4605 module from both the 1 and 0 outputs of memory buffer register bits 3 through 8 (12 lines in 6 twisted pairs) and from the three IOP pulse generator outputs (6 lines in 3 twisted pairs). Connections are then made from the three output terminals of a 4605 module directly to the logic circuits of the I/O device or to the interface connector for return to the computer.

The 4605 Pulse Amplifier modules are delivered with jumper wires connecting each input of the 6-input negative NAND diode gate to both the 1 and 0 input terminals for the appropriate MB input signal. The user must remove one jumper from each of the six NAND gate inputs to establish the appropriate select code. (Both jumpers may be removed if the select code requires it, such as in the Type 154 Memory Extension Control option.) This system allows select codes to be changed in the module and not in cable connections. As delivered, these modules are

also wired to produce negative IOT pulses. Positive IOT pulses can be obtained by reversing both jumper wire connections of a pulse transformer secondary winding on a module printed-wiring board.

Note that the MB and IOP connections to the 4605 modules are fixed and cannot be modified to operate more than one pulse amplifier (per module) at the same time. Should an I/O device require coincident positive and negative IOT pulses, two separate 4605 modules must be used or an IOT pulse can be used to trigger external positive and negative pulse amplifiers. Note also that positive IOT pulses cannot be inverted to produce negative IOT pulses but can be used to trigger a negative pulse amplifier.

Output pulses from a 4605 Pulse Amplifier are standard for the DEC 4000 Series systems modules (0.4 microsecond). Each output is capable of driving 16 pulse loads.

SECTION 7

INSTALLATION

SITE PREPARATION

Space must be provided at the installation site to accommodate the PDP-5 and all peripheral equipment and to allow freedom of access to all doors and panels for maintenance. In larger systems, consideration should be given to human engineering factors which minimize the effort required by an operator seated at the operator console to obtain visual or physical access to all controls, indicators, input bins, and output hoppers of all equipment in the system. A single-cabinet PDP-5 requires a floor space 30 inches wide and 45-1/16 inches deep with a minimum service clearance of 14-7/8 inches at the back. A dual cabinet PDP-5 requires a space 42 inches wide with the same depth and service clearance, since the table on a dual-cabinet system does not extend beyond the end panels. Additional width of 19-3/4 inches is required for each additional computer cabinet which is bolted to the main frame or console cabinet. Figure 7-1 indicates the space requirements, cable access, and floor loading for a single-cabinet PDP-5. This diagram can also be used in planning the installation of all I/O equipment housed in standard DEC computer cabinets, realizing that other cabinets do not have the table at the front of the operator console and that 1-1/4 inch end panels are added to the side of each multiple-cabinet configuration constructed of 19-3/4 inch cabinets bolted together. The standard Teletype Automatic Send Receive set requires a floor space approximately 22-1/4 inches wide by 18-1/2 inches deep. Signal cable length restricts the location of the Teletype to within 18 inches of the side of the computer.

No special environmental condition need be met for proper operation of the PDP-5. Ambient temperature at the installation site can vary between 50 and 104 degrees Fahrenheit (between 10 and 40 degrees centigrade) where the relative humidity varies between 0 and 90 percent with no adverse effect on computer operation. To extend the life expectancy of the system, it is recommended that the ambient temperature at the installation site be maintained between 68 and 86 degrees Fahrenheit (between 20 and 30 degrees centigrade) and that the relative humidity be held below 70 percent. During shipping or storing of the system, the ambient

temperature may vary between 32 and 104 degrees Fahrenheit (between 0 and 40 degrees centigrade) and the relative humidity should not be allowed to rise above 90 percent. Although all exposed surfaces of all DEC cabinets and hardware are treated to prevent corrosion, exposure of systems to climates where the relative humidity rises above 90 percent for long periods of time should be avoided to prevent rusting.

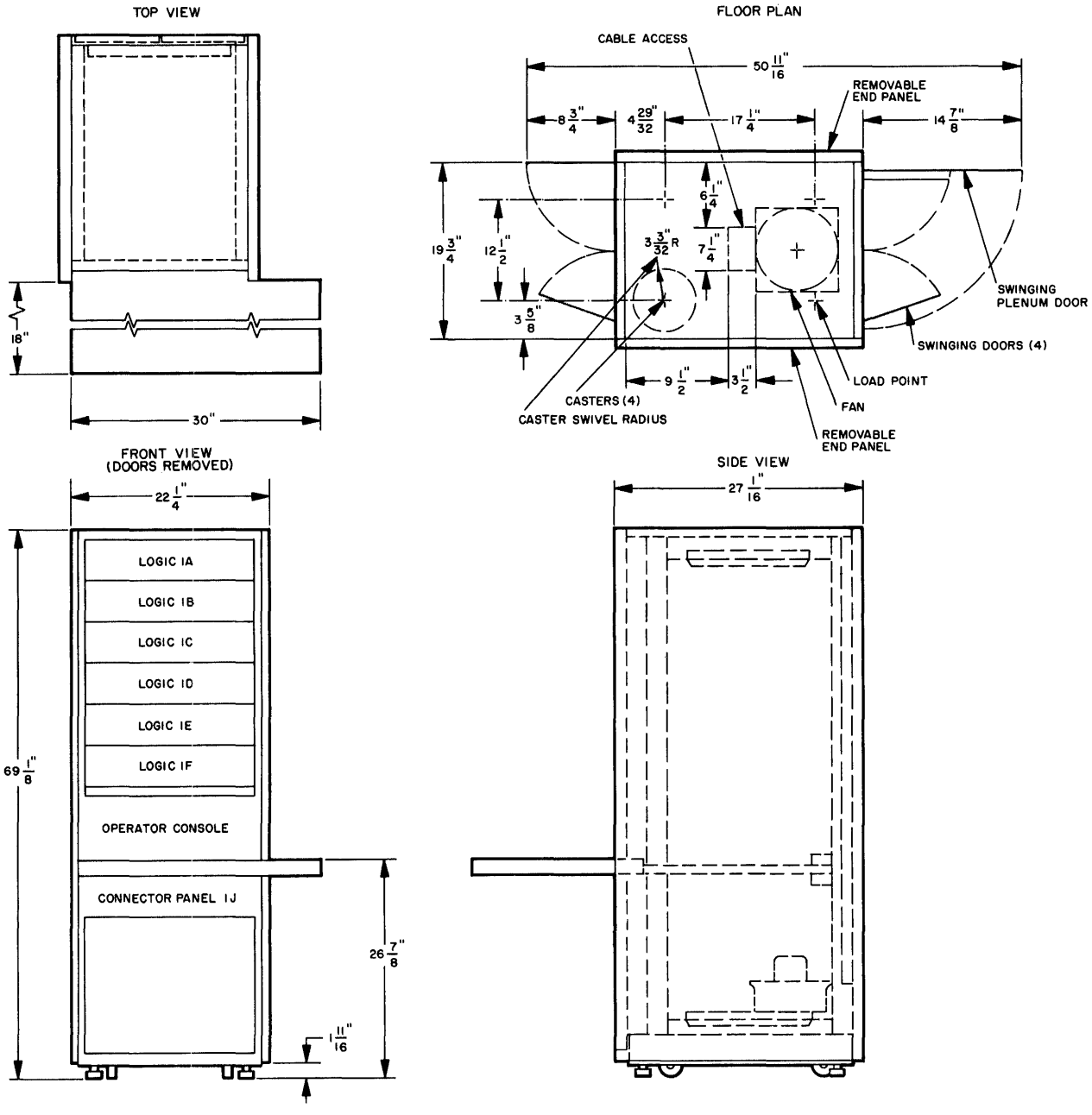


Figure 7-1 Installation Outline Drawing

A source of 115-volt (±17 volts), 60-cycle (±0.5 cycle), single-phase power capable of supplying at least 7.5 amperes must be provided to operate a standard PDP-5. To allow connection to the power cable of the computer, this source should be provided with a Hubbel 7310B, or equivalent twist-lock flush receptacle rated at 20 amperes at 250 volts. Power dissipation of a standard PDP-5 is approximately 780 watts, and the heat dissipation is approximately 2370 BTU/hour. Upon special request a PDP-5 can be constructed to operate from a 220-volt (±33 volts), 60-cycle (±0.5 cycle), single-phase power source or from a 100-volt (±15 volts), 50-cycle (±0.5 cycle), single-phase power source.

PREPARATION FOR SHIPMENT

The following shipping practices are followed by the factory in preparing a system for delivery to a customer and should be adhered to by the customer in any future shipment or relocation. Usually a shipment consists of at least three parcels containing the computer main frame, the Teletype, and a carton containing related documentation, cables, and other miscellaneous material. Shipping weight of a standard single-cabinet main frame is approximately 600 pounds, and is approximately 950 pounds for a dual-cabinet equipment. Shipping weight of the Teletype equipment is approximately 60 pounds, and the miscellaneous equipment carton weighs up to 100 pounds.

The cabinet of a PDP-5 system is prepared for shipment as follows:

a. The cabinet is placed upon a sturdy wooden pallet and held in place by passing a machine screw through the center of the tubular frame on each side of the bottom of the cabinet and turning this screw securely to the pallet.

b. The table is removed from the cabinet by removing the two mounting screws which attach the table extension arms to the side of the cabinet at the back; then the screws are returned to their position in the cabinet.

c. Modules are taped within the mounting panels and the power cables are coiled and taped to the floor of the cabinet. The plenum door is then bolted shut.

d. The table is cushioned by packing material and attached to the outside of the cabinet by metal straps. A wooden protector plate, wrapped in packing material, is strapped to the front of the cabinet to cover the operator console.

e. A full-height plastic bag is placed over the entire cabinet.

f. A wooden cover plate with appropriate packing material is placed on top of the cabinet and metal shipping straps are run vertically around the cabinet, over the cover plate, and under the pallet. When preparing the cabinet for overseas shipment, boards are nailed between the cover plate and the pallet to form a shipping crate which totally encloses the cabinet.

The Teletype is packaged in the original manufacturer's shipping carton and is prepared for shipment to the customer as follows:

a. Having disconnected the Teletype from the computer cabinet, the copyholder and chad box are removed.

b. The back panel of the stand is removed, all cables are disconnected, and the power pack is removed.

c. The Teletype console is removed from the stand and attached to a wooden pallet by four shipping screws. The pallet is then placed in the shipping carton and corrugated packing material is placed on all sides of the console.

d. The stand is placed in the shipping carton above the Teletype console. The copyholder, chad box, and power pack are individually wrapped in shipping material and packed within the stand; then the back of the stand is attached by means of the two normal mounting screws.

e. Additional packing material is added and the carton is sealed.

INSTALLATION PROCEDURE

No special tools or equipment are required for installation of a PDP-5 system. A fork-lift truck or other pallet-handling equipment and normal hand tools, including shears to cut the shipping straps, should be available for receiving and installing the equipment. To install the computer:

1. Place the computer cabinet package within the installation site near the final location. Cut the shipping straps and remove all packing material. Remove the table from the side of the cabinet and remove the protector plate from the front of the cabinet. Open the rear doors, remove the shipping bolts which hold the plenum door closed, and open the plenum door. Remove the machine screw which holds each side of the cabinet to the pallet. Slide the cabinet off of the pallet, using a ramp (approximately 4-3/4 inches high) from the floor to the top of the pallet. Move the cabinet to its final location within the installation site (this location must be within 18 feet of the primary power connector within the site).

2. Remove the tape which holds the modules in place within the mounting panels and the tape which holds the power cables to the floor of the cabinet. Assure that all modules are securely mounted in their connectors.

3. Remove the machine screw from the table mounting guide at each side of the back of the cabinet; install the table by passing the extension arms through the openings in the front of the cabinet and into the guides at the back of the cabinet; then replace the machine screws by passing them through the extension arms and turning them into the captive nut in each guide. The table extension arms are shown installed in the guides in Figure 7-2.

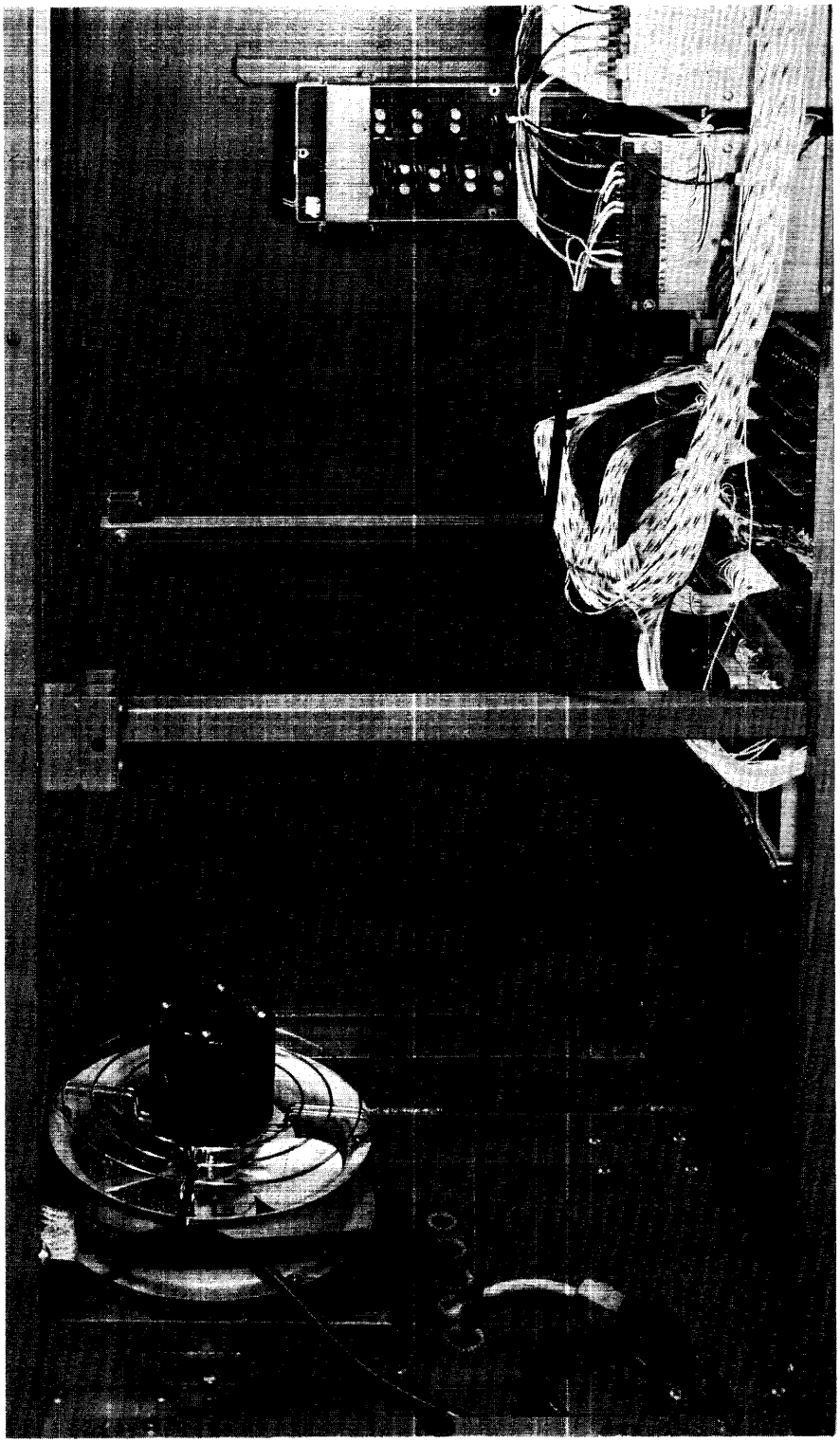


Figure 7-2 Installation Connections

4. Open the Teletype carton and remove the packing material. Remove the back cover from the stand and remove and unwrap the copyholder, chad box, and power pack. Remove the stand from the shipping carton. Remove the Teletype console from the carton, holding it by means of the wooden pallet attached to the bottom. Remove the Teletype console from the pallet and mount it on the stand. Snap the power pack in place within the top front of the stand, and connect the Teletype console to the power pack (a 6-lead cable attached at the console is connected to the power pack by means of a white plastic Molex 1375 female connector which mates with a male output plug on the power pack). Pass the 3-wire power cable and the 7-conductor signal cable (which is terminated in a female Amphenol 143-022-04 connector) through the opening at the lower left hand corner of the Teletype stand; then replace the back cover of the stand by means of the two mounting screws.

5. Adjust the stabilizing feet on the four corners of the computer cabinet and on any I/O equipment. Adjust the leveling devices on the feet of the Teletype stand.

6. Remove the fan and filter assembly from the bottom of the computer cabinet by disconnecting the captive screw at each side of the filter housing. Slide the rear portion of the cable port towards the rear door. Pass the larger diameter computer power cable out through the cable port, pass the Teletype signal and power cables into the cabinet through the cable port, and pass any other I/O equipment signal cables through the cable port; then replace the back half of the cable port and the fan and filter assembly. The computer power cable, the Teletype power cable, and the Teletype signal cable are shown passing through the cable port in Figure 7-2.

7. Connect the 3-prong male connector of the Teletype power cable to the female connector at the end of the smaller diameter power cable within the computer cabinet. Connect the Amphenol 22-pin female connector of the

Teletype signal cable to the mating connector to the right of module mounting panel 1F (as viewed from the inside of the cabinet). Connect all I/O device 50-pin cable connectors to the female interface connectors on connector panel 1J, remembering that connectors 1J01 and 1J02 are used for normal programmed connections, and connector 1J03 is used for data break signal connections. Assure that the lock switch is turned fully clockwise and that the POWER switch is set to the left position, then connect the computer power cable to the primary power source.

8. Turn the lock switch counterclockwise, set the POWER switch to the right position, and observe that the adjacent indicator lights.

9. Install the printer paper in the Teletype printer/keyboard, and install a tape in the punch as described in the Teletype Technical Manual or as described in Section 8 of this manual.

10. Set the LINE/OFF/LOCAL switch on the front of the Teletype unit to either side position (for early Teletype units press the LCL pushbutton-indicator, and observe that the indicator lights). Press the punch ON pushbutton. Strike several keys and observe that the printer and punch operate. Set the LINE/OFF/LOCAL switch to the OFF position (or on early models press any of the pushbuttons adjacent to the LCL pushbutton-indicator, and observe that this latter indicator becomes extinguished).

11. Set the POWER switch to the left position, and observe that the adjacent indicator becomes extinguished.

This completes the installation of a standard PDP-5 system. Before commencing normal use, verify the operating capability of the system by performing the Power Supply Checks and perform the Marginal Checks while running all of the diagnostic (Maindec) programs as described under Preventive Maintenance in Section 9 of this manual. Be sure to enter the margins obtained during each of these programs in the maintenance log, since these levels are essential to determining rate of change in future preventive maintenance.

SECTION 8

OPERATION

CONTROLS AND INDICATORS

Manual control of the PDP-5 is exercised by means of keys and switches on the operator console. Visual indication of the machine status and the content of major registers and control flip-flops is also given on this console. Indicator lamps light to denote the presence of a binary 1 in specific register bits and in control flip-flops. The function of these controls and indicators is listed in Table 8-1, and their location is shown in Figures 8-1 and 8-2. The function of all controls and indicators of the Model 33 ASR Teletype are described in Table 8-2, as they apply to operation of the computer. The Teletype console is shown in Figure 8-3.

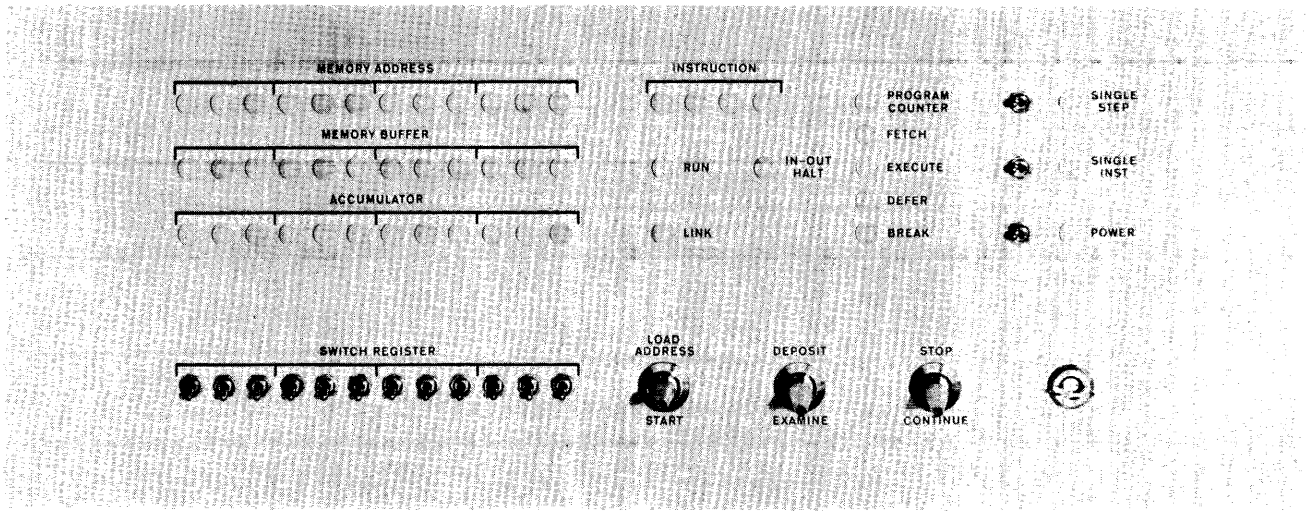


Figure 8-1 Standard Operator Console

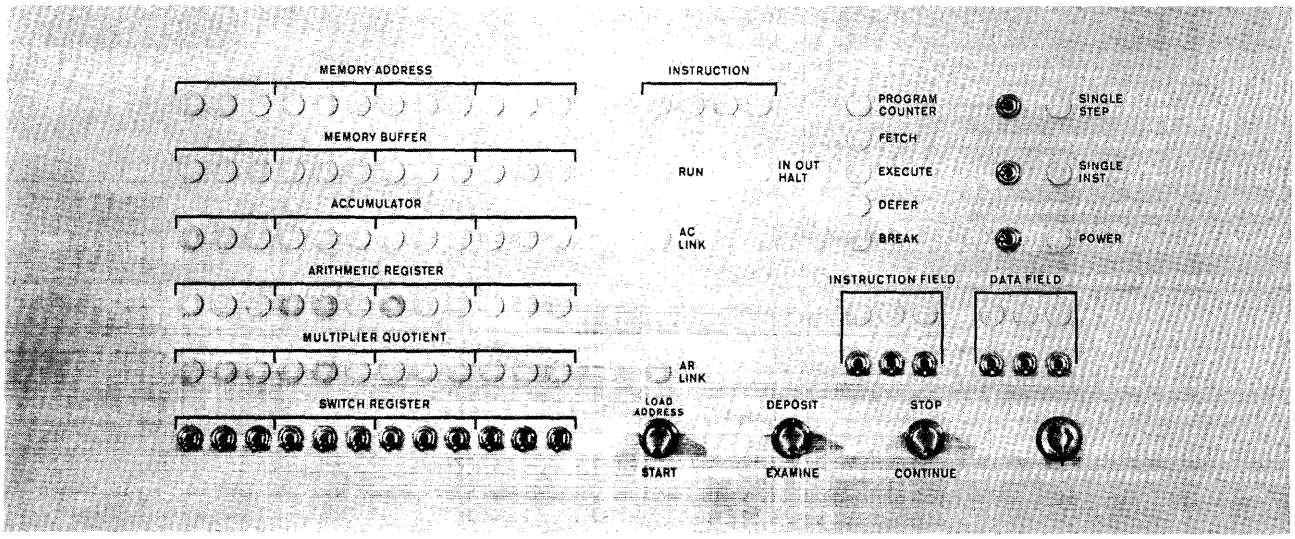


Figure 8-2 Operator Console with Type 153 Automatic Multiply and Divide, and Type 154 Memory Extension Control

TABLE 8-1 OPERATOR CONSOLE CONTROLS AND INDICATORS

Control or Indicator	Function
MEMORY ADDRESS indicators	Indicate the C(MA). Usually the C(MA) denotes the core memory address of the word currently or previously read or written. After operation of either the DEPOSIT or EXAMINE key, the C(MA) indicates the core memory address to be selected for the next memory cycle.
MEMORY BUFFER indicators	Indicate the C(MB). Usually the C(MB) designates the word just read or written at the core memory address held in the MA.
ACCUMULATOR indicators	Indicate the C(AC).
ARITHMETIC REGISTER indicators*	Indicate the C(AR). The arithmetic register (AR) holds the most significant half of the product at the conclusion of multiplication, holds the most significant half of the dividend at the beginning of division, and holds the remainder at the conclusion of a divide operation.

*Provided only on systems containing the Type 153 Automatic Multiply and Divide option.

TABLE 8-1 OPERATOR CONSOLE CONTROLS AND INDICATORS (continued)

Control or Indicator	Function
MULTIPLIER QUOTIENT indicators*	Indicate the C(MQ). The multiplier quotient (MQ) holds the multiplier at the beginning of a multiplication operation and the least significant half of the product at the conclusion. It holds the least significant half of the divident at the start of a divide operation and at the end holds the quotient.
AR LINK indicator*	Indicates the C(ARL). The arithmetic register link (ARL) is used as an extension of the AR and to indicate overflow to the control logic.
SWITCH REGISTER switches	Provide a means of manually setting a 12-bit word into the machine. Switches in the up position correspond to binary ones, down to zeros. The content of this register is loaded into the MA by the LOAD ADDRESS key, or into the MB and core memory by the DEPOSIT key. The C(SR) can be set into the AC under program control by means of the OSR instruction.
INSTRUCTION indicators	Indicate the C(IR), and so denote the operation code of the instruction currently being performed.
RUN indicator	Indicates the 1 status of the run flip-flop. When lit, the internal timing circuits are enabled and the machine performs instructions.
IN-OUT HALT indicator	Indicates the 1 status of the I/O-hlt flip-flop when lit. An I/O device programmed to use the I/O Halt feature of the PDP-5 produces an I/O Halt pulse which sets the I/O-hlt flip-flop when the device is initiated, and produces a Restart pulse which clears both the I/O-hlt and run flip-flops when it has completed the programmed operation. When the I/O-hlt flip-flop is set, it clears the run flip-flop to prevent program advance.
LINK or AC LINK indicator	Indicates the C(L).
PROGRAM COUNTER, FETCH, EXECUTE, DEFER, BREAK indicators	Indicate the primary control state of the machine and that the next memory cycle will be a program count, fetch, execute 1 or 2, defer, or break cycle, respectively.

*Provided only on systems containing the Type 153 Automatic Multiply and Divide option.

TABLE 8-1 OPERATOR CONSOLE CONTROLS AND INDICATORS (continued)

Control or Indicator	Function
SINGLE STEP switch and indicator	The switch is off in the left position. In the right position the switch causes the run flip-flop to be cleared during T6 to disable the timing circuits at the end of one cycle of operation. Thereafter, repeated operation of the CONTINUE key steps the program one cycle at a time so that the content of registers can be observed in each state. The indicator lights to denote the single-step mode of operation.
SINGLE INST switch and indicator	The switch is off in the left position. In the right position the switch causes the run flip-flop to be cleared at the end of the next instruction execution. When the computer is started by means of the START or CONTINUE key, this switch causes the run flip-flop to be cleared at the end of the last cycle of the current instruction (during T6 of the program count state). Therefore repeated operation of the CONTINUE key steps the program one instruction at a time. The indicator lights to denote the single-instruction mode of operation.
POWER switch and indicator	In the left position this switch removes primary power from the computer, and in the right position it applies power. The indicator lights to denote the energized condition.
INSTRUCTION FIELD indicators and switches**	The indicators denote the C(IF), and the switches serve as an extension of the SR to load the IF by means of the LOAD ADDRESS key. The instruction field register (IF) determines the core memory field from which instructions are to be taken.
DATA FIELD indicators and switches**	The indicators denote the C(DF) and the switches serve as an extension of the SR to load the DF by means of the LOAD ADDRESS key. The data field register (DF) determines the core memory field of data storage and retrieval.
LOAD ADDRESS key	Lifting this key sets the C(SR) into the MA, sets the C(INSTRUCTION FIELD switches) into the IF, and sets the C(DATA FIELD switches) into the DF.

**Provided only on systems containing the Type 154 Memory Extension Control option.

TABLE 8-1 OPERATOR CONSOLE CONTROLS AND INDICATORS (continued)

Control or Indicator	Function
START key	Starts the computer program by turning off the program interrupt circuits, clearing the AC and L, setting the program count state, and forcing the instruction JMP to the address currently held by the MA. Therefore, the word stored at the address held by the MA is taken as the first instruction.
DEPOSIT key	Lifting this key sets the C(SR) into the MB and core memory at the address specified by the current C(MA). This operation is performed by setting the execute 2 state and forcing a DCA instruction. The C(MA) is then incremented by one, to allow storing of information in sequential memory addresses by repeated operation of the DEPOSIT key.
EXAMINE key	Pressing this key sets the content of core memory at the address specified by the C(MA) into the MB and AC. This operation is performed by clearing the AC, setting the execute 1 state, and forcing a TAD instruction. The C(MA) is then incremented by one to allow examination of the contents of sequential core memory addresses by repeated operation of the EXAMINE key.
STOP key	Causes the run flip-flop to be cleared at the end (T6) of the cycle in progress at the time the key is lifted.
CONTINUE key	Pressing this key sets the run flip-flop to continue the program in the state designated by the lighted console indicator at the instruction currently held in the PC.
Lock switch	With this switch turned clockwise, all keys and switches except the SWITCH REGISTER switches on the operator console are disabled. In this condition the power can not be turned off by the POWER switch, and the program can not be disturbed by inadvertent key operation. The program can, however, monitor the C(SR) by execution of the OSR instruction and can be modified accordingly by skip instructions.

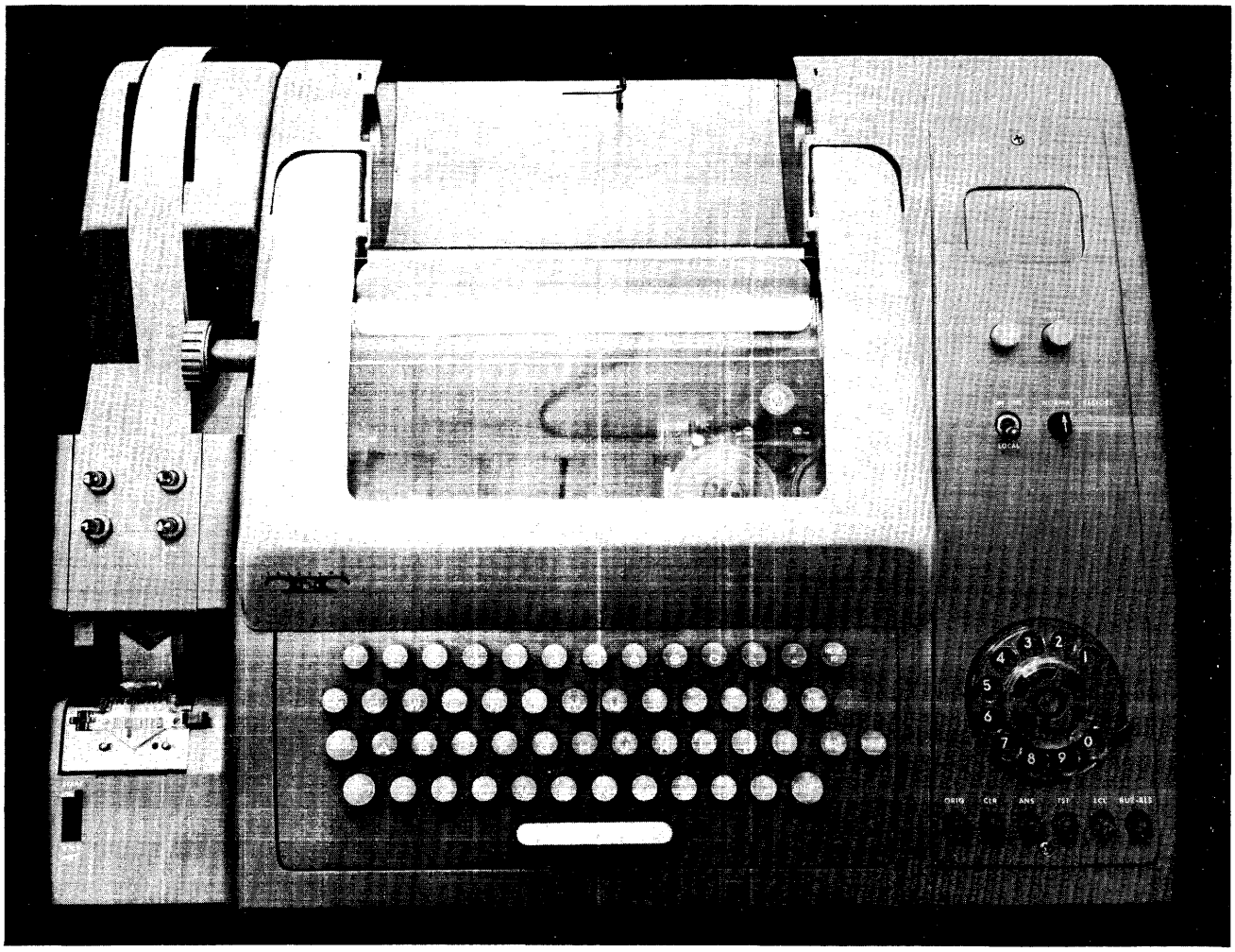


Figure 8-3 Teletype Console

TABLE 8-2 TELETYPE CONTROLS AND INDICATORS

Control or Indicator	Function
REL. pushbutton	Disengages the tape in the punch to allow tape removal or tape loading.
B. SP. pushbutton	Backspaces the tape in the punch by one space, allowing manual correction or rub out of the character just punched.
OFF and ON pushbuttons	Control use of the tape punch with operation of the Teletype keyboard/printer.

TABLE 8-2 TELETYPE CONTROLS AND INDICATORS (continued)

Control or Indicator	Function
START/STOP/FREE switch	Controls use of the tape reader with operation of the Teletype. In the lower FREE position the reader is disengaged and can be loaded or unloaded. In the center STOP position the reader mechanism is engaged but de-energized. In the upper START position the reader is engaged and operated under program control.
Keyboard	Provides a means of printing on paper in use as a typewriter and punching tape when the punch ON pushbutton is pressed, and provides a means of supplying input data to the computer when the LINE/OFF/LOCAL switch is in the LINE position (or in early machines when the ON LINE/LOCAL switch is in the ON LINE position).
LINE/OFF/LOCAL switch	Controls application of primary power in the Teletype and controls data connection to the processor. In the LINE position the Teletype is energized and connected as an I/O device of the computer. In the OFF position the Teletype is de-energized. In the LOCAL position the Teletype is energized for off-line operation, and signal connection to the processor is broken. Both line and local use of the Teletype require that the computer be energized through the POWER switch.
ON LINE/LOCAL switch*	Allows use of the Teletype as an input/output device of the computer in the ON LINE position or separate, off line use in the LOCAL position. Both on line and local use of the Teletype require that the computer POWER switch be in the on position.
REST indicator*	Not used.
NORMAL RESTORE switch*	Not used.
Dial*	Not used.
LCL pushbutton-indicator*	Power control which energizes the Teletype with primary power from the computer when pressed. The indicator lights to signify the energized status of the Teletype.

*These devices are provided on early PDP-5 systems due to unavailability of more appropriate Teletype equipment. In later systems these devices are replaced by a LINE/OFF/LOCAL switch.

TABLE 8-2 TELETYPE CONTROLS AND INDICATORS (continued)

Control or Indicator	Function
ORIG, CLR, ANS, TST, and BUZ-RLS pushbutton-indicators.	Not used electrically but pressed to mechanically reset the LCL pushbutton indicator to de-energize the Teletype.
VOL control*	Not used.

*These devices are provided on early PDP-5 systems due to unavailability of more appropriate Teletype equipment. In later systems these devices are replaced by a LINE/OFF/LOCAL switch.

OPERATING PROCEDURES

Many means are available for loading and unloading PDP-5 information. The means used are, of course, dependent upon the form of the information, time limitations, and the peripheral equipment connected to the computer. The following procedures are basic to any use of the PDP-5, and although they may be used infrequently as the programming and use of the computer become more sophisticated, they are valuable in preparing the initial programs and learning the function of machine input and output transfers.

Manual Data Storage and Modification

Programs and data can be stored or modified manually by means of the facilities on the operator console. Chief use of manual data storage is made to load the readin mode loader program into the computer core memory. The readin mode (RIM) loader is a program used to automatically load programs into PDP-5 from perforated tape in RIM format. This program and the RIM tape format are described in the PDP-5 handbook and in Digital Program Library descriptions. The RIM program is listed in Table 8-3 for rapid reference and can be used as an exercise in manual data storage. To store data manually in the PDP-5 core memory:

1. Turn the lock switch counterclockwise and set the POWER switch to the right.

2. Set the bit switches of the SWITCH REGISTER (SR) to correspond with the address bits of the first word to be stored. Lift the LOAD ADDRESS key and observe that the address set by the SR is held in the MA, as designated by lighted MEMORY ADDRESS indicators corresponding to switches in the 1 (up) position and unlighted indicators corresponding to switches in the 0 (down) position.

3. Set the SR to correspond with the data or instruction word to be stored at the address just set into the MA. Lift the DEPOSIT key and observe that the MB, and hence the core memory, hold the word set by the SR.

Also, observe that the MA has been incremented by one so that additional data can be stored at sequential addresses by repeated SR setting and DEPOSIT key operation.

TABLE 8-3 READIN MODE LOADER PROGRAM

Address	Content	Mnemonic		Comments
700	6032	BEG,	KCC	CLEAR AC AND FLAG
701	6031		KSF	SKIP IF FLAG = 1
702	5301		JMP .-1	LOOKING FOR CHAR
703	6036		KRB	READ BUFFER
704	7106		CLL RTL	
705	7006		RTL	CH 8 IN AC_0
706	7510		SPA	CHECKING FOR LEADER
707	5301		JMP BEG +1	FOUND LEADER
710	7006		RTL	OK, CH 7 IN LINK
711	6031		KSF	
712	5311		JMP .-1	READ, DO NOT CLEAR
713	6034		KRS	CHECKING FOR ADDRESS
714	7420		SNL	
715	3720		DCA I TEMP	STORE CONTENTS
716	3320		DCA TEMP	STORE ADDRESS
717	5300		JMP BEG	NEXT WORD
720		TEMP,		TEMP STORAGE

To check the content of an address in core memory, set the address into the MA as in step 2, then press the EXAMINE key. The content of the address is then designated by the MEMORY BUFFER indicators. The content of the MA is incremented by one with operation of the EXAMINE key, so the content of sequential addresses can be examined by repeated operation of the key after the original (or starting) address is loaded. The content of any address can be modified by repeating both steps 2 and 3.

Loading Data Under Program Control

Information can be stored or modified in the computer automatically only by enacting programs previously stored in core memory. For example, having the RIM loader stored in core memory allows RIM format tapes to be loaded as follows:

1. Turn the lock switch counterclockwise and set the POWER switch to the right.

2. Set the Teletype LINE/OFF/LOCAL switch to the LINE position.

3. Load the tape in the Teletype reader by setting the START/STOP/FREE switch to the FREE position, releasing the cover guard by means of the latch at the right, loading the tape so that the sprocket wheel teeth engage the feed holes in the tape, closing the cover guard, and setting the switch to the STOP position. Tape is loaded in the back of the reader so that it moves toward the front as it is read. Proper positioning of the tape in the reader finds three bit positions being sensed to the left of the sprocket wheel and five bit positions being sensed to the right of the sprocket wheel.

4. Load the starting address of the RIM loader program (not the address of the program to be loaded) into the MA by means of the SR and the LOAD ADDRESS key.

5. Press the computer START key and set the 3-position Teletype reader switch to the START position. The tape will be read automatically. The program contained on the tape might be initialized and started automatically

because some tapes in RIM format are concluded with address 0000 and a data word equal to one less than the starting address of the program just read. Therefore, after the last tape character is read, the program starting address is taken by the program counter as the address of the next instruction to be executed.

Automatic storing of the binary loader (BIN) program is performed by means of the RIM loader program as previously described. With the BIN loader stored in core memory, program tapes in the program assembly language (PAL) binary format can be stored as described in the previous procedure except that the starting address of the BIN loader (1777 or 7777 depending on the size of core memory) is used in step 4. When storing a program in this manner, the computer stops and the AC should contain all zeros if the program is stored properly. If the computer stops with a number other than zero in the AC, a checksum error has been detected; so the program has been stored incorrectly, and the storage procedure should be repeated. When the program has been stored correctly, it can be initiated by loading the program starting address (usually designated on the leader of the tape) into the MA by means of the SR and LOAD ADDRESS key, then pressing the START key.

Off-Line Teletype Operation

The Teletype can be used separately from the PDP-5 for typing, punching tape, or duplicating tapes. To use the Teletype in this manner:

1. Assure that the computer lock switch is turned counterclockwise and set the POWER switch to the right.

2. Set the Teletype LINE/OFF/LOCAL switch to the LOCAL position.

3. If the punch is to be used, load it by raising the cover, manually feeding the tape from the top of the roll into the guide at the back of the punch, advancing the tape through the punch by manually turning the friction wheel, and then closing the cover. Energize the punch by pressing the ON pushbutton, and produce about two feet of leader. The leader-trailer can be code 200 or 377. To produce the code 200 leader, simultaneously press

and hold the CTRL and SHIFT keys with the left hand; press and hold the REPT key; press and release the @ key; when the required amount of leader has been punched release all keys. To produce the 377 code, simultaneously press and hold both the REPT and RUB OUT keys until a sufficient amount of leader has been punched.

If an incorrect key is struck while punching a tape, the tape can be corrected as follows: If the error is noticed after typing and punching N characters, press the punch B. SP. (backspace) pushbutton N + 1 times and strike the keyboard RUB OUT key N + 1 times. Then continue typing and punching with the character which was in error.

To duplicate an existing tape: perform steps 1 and 2 of the procedure under the current heading and repeat step 2 of the procedure outlined under Loading Data Under Program Control to energize the equipment and load the tape to be duplicated into the reader. Then perform step 3 of the procedure under the current heading. Initiate tape duplication by setting the reader START/STOP/FREE switch in the START position.

Corrections to insert or delete information on a perforated tape can be made by duplicating the correct portion of the tape, and manually punching additional information or inhibiting punching of information to be deleted. This is accomplished by duplicating the tape and carefully observing the information being typed as the tape is read. In this manner the reader START/STOP/FREE switch can be set to the STOP position just before the point of the correction is typed. Information to be inserted can then be punched manually by means of the keyboard. Information can be deleted by pressing the punch OFF pushbutton and operating the reader until the portion of the tape to be deleted has been typed. It may be necessary to backspace and rub out one or two characters on the new tape if the reader is not stopped precisely on time. The number of characters to be rubbed out can be determined exactly by the typed copy. Be sure to count spaces when counting typed characters. Continue duplicating the tape in the normal manner after making the corrections.

New, duplicated, or corrected perforated tapes should be verified by reading them off line and carefully proofreading the typed copy.

Assembling Programs With PAL

Programs prepared in binary format and written in PAL symbolic language can be assembled into binary, machine-language program tapes by PAL as described in appropriate Digital Program Library documents. Basically, this operation is accomplished as follows:

1. Energize the computer by assuring that the lock switch is turned counter-clockwise and by setting the POWER switch to the right.

2. Energize the Teletype by setting the LINE/OFF/LOCAL switch to the LINE position. Check the paper supply in the printer and punch and replenish as necessary.

3. Store the RIM loader program as described under Manual Data Storage and Modification.

4. Store the BIN loader program as described under Loading Data Under Program Control.

5. Load the PAL program tape in the Teletype reader and set the START/STOP/FREE switch to the STOP position.

6. Load the starting address of the BIN loader program (1777 or 7777) into the MA by means of the SR and the LOAD ADDRESS key.

7. Press the START key, set the Teletype reader switch to the START position, and wait until the tape has been completely read. When the tape stops, the AC should contain all zeros. If any ACCUMULATOR indicator is lit, a checksum error has been encountered and this procedure should be repeated from step 5. Repeated errors indicate defects in the tape being read or in the operation of the PDP-5 system.

8. Load the binary tape in symbolic language into the reader and set the START/STOP/FREE switch to the STOP position.

9. Load the starting address of the assembler (200) into the MA by means of the SR and the LOAD ADDRESS key.

10. Set bit 0 of the SR to the 0 position, and set bit 1 to the 1 position. These switch settings indicate to the program that the first pass of this 2-pass assembler is to be performed. If a starting address other than 200 is to be generated for the program being assembled, set this address into bits 7 through 11 of the SR.

11. Assure that the Teletype punch is turned off by pressing the OFF pushbutton.

12. Press the computer START key, start the tape reader by setting the 3-position switch to the START position, and wait for the tape to be completely read and a symbol table to be typed. If an error printout is obtained at this time, the symbolic tape must be corrected and this procedure is repeated from step 8. If no error printout is obtained, proceed to step 13.

13. Remove and reload the tape in the reader.

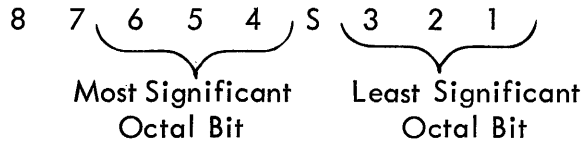
14. Repeat step 9, then set SR bit 0 to 1 and bit 1 to 0 to indicate that the second pass is to be performed.

15. Press the Teletype punch ON pushbutton, press the START key, and wait until a leader is automatically punched. When leader punching stops, start the tape reader, and wait until the program stops. The perforated tape obtained in the second pass (reading) of the symbolic tape is an assembled binary tape which can be stored by means of the BIN loader and can be run as described under Loading Data Under Program Control.

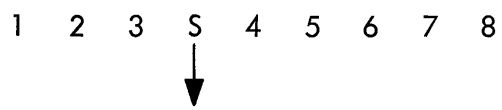
Teletype Code

The 8-bit code used by the Model 33 ASR Teletype unit is the American Standard Code for Information Interchange (ASCII) modified. To convert the ASCII code to Teletype code add

200 octal (ASCII + 200_8 = Teletype). This code is read in the reverse of the normal octal form used in the PDP-5 since bits are numbered from right to left, from 1 through 8, with bit 1 having the most significance. Therefore perforated tape is read:



Tape is loaded into the reader:



The Model 33 ASR set can generate all assigned codes except 340 through 374 and 376. Generally codes 207, 212, 215, 240 through 337, and 377 are sufficient for Teletype operation. The Model 33 ASR set can detect all characters, but does not interpret all of the codes that it can generate as commands. The standard number of characters printed per line is 72. The sequence for proceeding to the next line is a carriage return followed by a line feed (as opposed to a line feed followed by a carriage return). Key or key combinations required to produce octal codes from 200 through 337, 375, and 377 are indicated in Table 8-4 with the associated ASCII character.

TABLE 8-4 TELETYPE CODE

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
220	Null/Idle	NULL	---	CTRL @
201	Start of Message	SOM	---	CTRL A
202	End of Address	EOA	---	CTRL B
203	End of Message	EOM	---	CTRL C
204	End of Transmission	EOT	---	CTRL D
205	Who Are You	WRU	---	CTRL E
206	Are You	RU	---	CTRL F
207	Audible Signal	BELL	---	CTRL G

TABLE 8-4 TELETYPE CODE (continued)

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
210	Format Effector	FE	---	CTRL H
211	Horizontal Tabulation	H TAB	---	CTRL I
212	Line Feed	LF	---	CTRL J
213	Vertical Tabulation	V TAB	---	CTRL K
214	Form Feed	FF	---	CTRL L
215	Carriage Return	CR	---	CTRL M
216	Shift Out	SO	---	CTRL N
217	Shift In	SI	---	CTRL O
220	Device Control Reversed for Data Line Escape	DC0	---	CTRL P
221	Device Control On	DC1	---	CTRL Q
222	Device Control (TAPE)	DC2	---	CTRL R
223	Device Control Off	DC3	---	CTRL S
224	Device Control (~~TAPE~~)	DC4	---	CTRL T
225	Error	ERR	---	CTRL U
226	Synchronous Idle	SYNC	---	CTRL V
227	Logical End of Media	LEM	---	CTRL W
230	Separator, Information	S0	---	CTRL X
231	Separator, Data Delimiters	S1	---	CTRL Y
232	Separator, Words	S2	---	CTRL Z
233	Separator, Groups	S3	---	SHIFT CTRL K
234	Separator, Records	S4	---	SHIFT CTRL L
235	Separator, Files	S5	---	SHIFT CTRL M
236	Separator, Misc.	S6	---	SHIFT CTRL N
237	Separator, Misc.	S7	---	SHIFT CTRL O
240	Space	SP	Space	Space Bar
241	Exclamation Point	!	!	SHIFT !
242	Quotation Marks	"	"	SHIFT "

TABLE 8-4 TELETYPE CODE (continued)

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
243	Number Sign	#	#	SHIFT #
244	Dollar Sign	$	$	SHIFT $
245	Percent Sign	%	%	SHIFT %
246	Ampersand	&	&	SHIFT &
247	Apostrophe	'	'	SHIFT '
250	Parenthesis, Beginning	(	(	SHIFT (
251	Parenthesis, Ending	)	)	SHIFT)
252	Asterisk	*	*	SHIFT *
253	Plus Sign	+	+	SHIFT +
254	Comma	,	,	,
255	Hyphen	-	-	-
256	Period	.	.	.
257	Virgule	/	/	/
260	Numeral 0	0	0	0
261	Numeral 1	1	1	1
262	Numeral 2	2	2	2
263	Numeral 3	3	3	3
264	Numeral 4	4	4	4
265	Numeral 5	5	5	5
266	Numeral 6	6	6	6
267	Numeral 7	7	7	7
270	Numeral 8	8	8	8
271	Numeral 9	9	9	9
272	Colon	:	:	:
273	Semicolon	;	;	;
274	Less Than	<	<	SHIFT <
275	Equals	=	=	SHIFT =
276	Greater Than	>	>	SHIFT >

TABLE 8-4 TELETYPE CODE (continued)

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
277	Interrogation Point	?	?	SHIFT ?
300	At	@	@	SHIFT @
301	Letter A	A	A	A
302	Letter B	B	B	B
303	Letter C	C	C	C
304	Letter D	D	D	D
305	Letter E	E	E	E
306	Letter F	F	F	F
307	Letter G	G	G	G
310	Letter H	H	H	H
311	Letter I	I	I	I
312	Letter J	J	J	J
313	Letter K	K	K	K
314	Letter L	L	L	L
315	Letter M	M	M	M
316	Letter N	N	N	N
317	Letter O	O	O	O
320	Letter P	P	P	P
321	Letter Q	Q	Q	Q
322	Letter R	R	R	R
323	Letter S	S	S	S
324	Letter T	T	T	T
325	Letter U	U	U	U
326	Letter V	V	V	V
327	Letter W	W	W	W
330	Letter X	X	X	X
331	Letter Y	Y	Y	Y
332	Letter Z	Z	Z	Z

TABLE 8-3 TELETYPE CODE (continued)

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
333	Bracket, Left	[	[	SHIFT K
334	Reverse Virgule	\	\	SHIFT L
335	Bracket, Right	]	]	SHIFT M
336	Up Arrow (exponentation)	↑	↑	SHIFT ↑
337	Left Arrow	←	←	SHIFT ←
340 through 374 are not available				
375	Unassigned Control	ⓘ	---	ALT MODE
376	Not Available			
377	Delete/Idle/Rub Out	DEL	---	RUB OUT

PROGRAMMING

Refer to the PDP-5 Programming Handbook F-55 for information on basic programming of the system. Refer to individual Digital Program Library documents for specific information on the format, specifications, and procedure for using a particular program language, such as PAL or FORTRAN.

SECTION 9

MAINTENANCE

Maintenance of the PDP-5 consists of procedures repeated periodically as preventive maintenance and tasks performed as corrective maintenance in the event of equipment malfunction. Maintenance activities require use of the equipment listed in Table 9-1, or equivalent, as well as the use of standard hand tools, cleansers, and test cables and probes.

TABLE 9-1 MAINTENANCE EQUIPMENT

Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630-NA or 260
Potentiometric Voltmeter**	John Fluke	Model 801H
Audio Oscillator**	Hewlett Packard	Model 200CD
Oscilloscope	Tektronix	Type 540 Series
Clip-on Current Probe	Tektronix	Type P6016
Current Probe Amplifier	Tektronix	Type 131
Plug-In Unit**	Tektronix	Type L
System Module Extender*	DEC	Type 1954
System Module Puller*	DEC	Type 1960
Maindec 501, Instruction Test*	DEC	DEC-5-12-M
Maindec 502, Memory Checkerboard Test*	DEC	DEC-5-15-M
Maindec 503, Address Test*	DEC	DEC-5-16-M
Maindec 510, Read Paper Tape Test*	DEC	DEC-5-13-M
Maindec 512, Punch Tape Test*	DEC	DEC-5-14-M
Maindec 514, Teleprinter Test*	DEC	DEC-5-19-M

*One is supplied with the equipment
**Required only for the Type 137 Analog-to-Digital Converter

TABLE 9-1 MAINTENANCE EQUIPMENT (continued)

Equipment	Manufacturer	Designation
Paint Spray Can*	DEC	DEC Blue 5150-865
Paint Spray Can*	DEC	DEC Gray 3277-1R55
Air Filter*	Research Products Corp.	E Z Kleen 2-inch Type MV
Filter-Kote*	Research Products Corp.	By Name

*One is supplied with the equipment

The Maindec routines are diagnostic programs designed to exercise or test specific functions within the computer system. Maindec routines are prepared as a perforated-paper program tape in readin mode format and are accompanied by a detailed description of the program contained on the tape, procedures for using the program, and information on analyzing the program results to locate specific circuit failures. Use of these routines is indicated at the appropriate points in this manual as they apply to preventive or corrective maintenance of the standard PDP-5 system.

If is is necessary to remove a module during either preventive or corrective maintenance, the Type 1960 System Module Puller should be used. Turn off all power before extracting or inserting modules. Carefully hook the small flange of the module puller over the center of the module rim, and gently pull the module from the rack. Use a straight even pull to avoid damage to plug connections or twisting of the printed-wiring board. Since the puller does not fasten to the module, grasp the rim of the module to prevent it from falling. Access to controls on the module for use in adjustment, or access to points used in signal tracing can be gained by removing the module, connecting a Type 1954 System Module Extender into the vacated module connector in the mounting panel, and then inserting the module into the extender.

The procedures presented here assume that the reader understands the function of the keys, switches, and indicators on the operator console and is familiar with machine programming as described in the PDP-5 Programming Handbook, F55.

In addition to the controls and indicators on the operator console and on the Teletype unit (described in Table 8-1 and Table 8-2), maintenance operations use controls and indicators

on component assemblies mounted on the plenum door of the computer. The function of these controls and indicators is described in Table 9-2.

TABLE 9-2 MAINTENANCE CONTROLS AND INDICATORS

Control or Indicator	Function
	832 Power Control
Circuit breaker	Protects the computer power source from overload due to failure of the computer power circuits.
REMOTE/OFF/LOCAL switch	Allows control of the computer primary power from the back of the machine during maintenance. In the REMOTE position, application and removal of computer power is controlled by the lock and POWER switches on the operator console. In the OFF position the computer is de-energized, regardless of the position of switches on the operator console. In the LOCAL position the computer is energized regardless of the position of operator console switches or door interlocks.
Elapsed time meter	Indicates the total number of hours the computer has been energized and so provides a unit of measure that is more appropriate than calendar time for determining preventive maintenance schedules.
MEM. POWER switch	Controls the application and removal of operating voltages for the memory circuits.
	737 (Marginal-Check) Power Supply
-15/off/+10 switch	Controls the output of the marginal-check power supply. In the -15 position the output is negative and is connected to the blue connector on each module mounting panel. In the off (center) position the supply is de-energized and the output is disconnected. In the +10 position the output is positive and is connected to the green connector on each module mounting panel.

TABLE 9-2 MAINTENANCE CONTROLS AND INDICATORS (continued)

Control or Indicator	Function
MARGINAL CHECK voltmeter	Indicates the output voltages of the marginal-check power supply.
Control knob	Controls the amplitude of the marginal-check voltage between 0 and 20 v.

PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed prior to the initial operation of the equipment and periodically during its operating life to ensure that it is in satisfactory operating condition. Faithful performance of these tasks will forestall possible future failure by discovering progressive deterioration and correcting minor damage at an early stage. Data obtained during the performance of each preventive maintenance task should be recorded in a log book. Analysis of this data will indicate the rate of circuit operation deterioration and provide information to determine when components should be replaced to prevent failure of the equipment. These tasks consist of mechanical checks, which include cleaning and visual inspections; marginal checks, which aggravate border line circuit conditions or intermittent failures so that they can be detected and corrected; and checks of specific circuit elements such as the power supplies, sense amplifiers, and memory currents. All preventive maintenance tasks should be performed as a function of conditions at the installation site. Perform the mechanical checks at least once each month or as often as required to allow efficient functioning of the air filter. All other tasks should be performed on a regular schedule, at an interval determined by the reliability requirements of the system. For a typical application, a schedule of every 600 equipment operating hours or every four months, whichever occur first, is suggested.

The most important schedule to maintain is that of the simplest procedure, -- the Mechanical Checks. Many hours of computer down time can be avoided by rigid adherence to a schedule based upon the condition of the air filter. Machine failures can occur due to overheating caused by an air filter becoming so dirty that no cooling air can be drawn into the cabinet by the fan.

Mechanical Checks

Assure good mechanical operation of the equipment by performing the following steps and the indicated corrective action for any substandard conditions found:

1. Clean the exterior and the interior of the equipment cabinet using a vacuum cleaner or clean cloths moistened in nonflammable solvent.

2. Clean the air filter at the bottom of the cabinet. Remove the filter by removing the fan and housing, which are held in place by two knurled and slotted captive screws. Wash the filter in soapy water and dry it in an oven or by spraying with compressed gas. Spray the filter with Filter-Kote (Research Products Corporation, Madison, Wisconsin).

3. Lubricate door hinges and casters with a light machine oil. Wipe off excess oil.

4. Visually inspect the equipment for completeness and general condition. Repaint any scratched or corroded areas with DEC blue tweed paint number 5150-865 or DEC gray enamel number 3277-1R55.

5. Inspect all wiring and cables for cuts, breaks, fraying, wear, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring or cable covering.

6. Inspect the following for mechanical security: keys, switches, control knobs, lamp assemblies, jacks, connectors, transformers, fan, capacitors, elapsed time meter, etc. Tighten or replace as required.

7. Inspect all module mounting panels to assure that each module is securely seated in its connector.

8. Inspect power supply capacitors for leaks, bulges, or discoloration. Replace any capacitors giving these signs of malfunction.

Power Supply Checks

Check the output voltage and ripple content of the 779 Power Supply (not the 735), and assure that they are within the tolerance specified in Table 9-3. Use a multimeter to make the output voltage measurements without disconnecting the load. Usė the oscilloscope to measure the peak-to-peak ripple content on dc outputs of the supply. This supply is not adjustable, so if the output voltage or ripple content is not within the tolerance specified, the supply is considered defective and troubleshooting procedures should be undertaken.

TABLE 9-3 TYPE 779 POWER SUPPLY OUTPUTS

Measurement Terminals at Power Supply Output	Nominal Output Voltage	Output Voltage Range	Maximum Peak-to-Peak Output Ripple
Orange (+) to Yellow (-)	+10	9.0 to 11.0	1.0 volt
Yellow (-) to Blue (-)	-15	14.0 to 16.0	0.5 volt
Red (+) to Yellow (-)	+15	14.0 to 16.0	1.25 volt
Yellow (+) to Green (-)	-15	14.0 to 16.0	1.25 volt

Check the operation of the varible-output 737 Power Supply which produces the marginal-check voltages. With all of the normal/marginal switches in the normal (down) position, make the following measurements at the color-coded connector at the right side of any convenient module mounting panel:

1. Connect a multimeter between the yellow (-) and black (+) terminals; set the -15/off/+10 switch to the -15 position, and turn the control knob clockwise to assure that at least -20 volts can be produced by the supply (as indicated on the multimeter). Record the indication given on the MARGINAL CHECK voltmeter and on the multimeter. These indications should be equal ±1 volt. Connect the oscilloscope to the yellow terminal, and measure the peak-to-peak ripple content to assure that it is no more than 1.0 volt. Turn the control knob fully counterclockwise; set the -15/off/+10 switch to the off position, and disconnect the multimeter and oscilloscope.

2. Connect the multimeter between the green (+) and black (-) terminals; set the -15/off/+10 switch to the +10 position, and turn the control knob clockwise to assure that at least +20 volts can be produced by the supply. Turn the control knob fully counterclockwise, set the -15/off/+10 switch to the off position, and disconnect the multimeter.

Marginal Checks

Marginal checking utilizes the Maindec diagnostic programs to test the functional capabilities of the computer with the module operating voltages biased above and below the nominal levels within a specified margin. Biasing the operating voltages aggravates borderline circuit conditions within the modules to produce failures which are detected by the program. When the program detects an error, it usually provides a printout or visual indication which is helpful in locating the source of the fault and then halts. Therefore, marginal components can be replaced during scheduled preventive maintenance to forestall possible future equipment failure. If no marginal components exist, the operating voltages are biased beyond the specified margins, and the operating voltages at which circuits fail are recorded in the maintenance log. By plotting the bias voltages obtained during each scheduled preventive maintenance, progressive deterioration can be observed and expected failure dates can be predicted. In this manner these checks provide a means of planned replacement. These checks can also be used as a troubleshooting aid to locate marginal or intermittent components, such as deteriorating transistors.

Raising the operating voltage above +10 volts increases the transistor cut-off bias that must be overcome by the previous driving transistor. Therefore low-gain transistors fail. Lowering the bias voltage below +10 volts reduces transistor base bias and noise rejection and thus provides a test to detect high-leakage transistors and simulates high temperature conditions (to check for thermal run away). Raising and lowering the -15 volt supply increases and decreases the output pulse amplitude of pulse amplifier modules. Since the -15 volt supply is the collector load voltage (which is clamped at -3 volts in most modules), raising and lowering this source would have little effect upon the logic circuits. Therefore, wiring in the PDP-5 allows marginal checking of the -15 volt supply connected to pulse amplifier modules only.

The +10 volt margin should be about ±5 volts, and the -15 volt margin should be about +3 (-18 v) and -8 (-7 v) volts. It is important that the -15 volt margin not be increased above 18 volts or damage can result within the logic.

The 779 Power Supply produces the normal module operating voltages of +10 vdc and -15 vdc. The 737 Power Supply produces an adjustable voltage which is used to check for marginal circuit operations under biased conditions. The output of this supply can be selected to be positive, disconnected, or negative by means of a -15/off/+10 switch; is adjusted by means of the large knob on the supply; and is indicated on a MARGINAL CHECK voltmeter on the supply. Outputs from both of these supplies are connected to each module mounting panel through a color-coded connector at the right side of each panel, as seen from the module side. The color coding of these connectors is as follows, from top to bottom:

a. Green, +10 vdc marginal-check supply

b. Red, normal +10 vdc supply

c. Black, ground

d. Blue, normal -15 vdc supply

e. Yellow, -15 vdc marginal-check supply

Three single-pole double-throw, normal/marginal switches at the end of each module mounting panel allow selection of either the normal power source or the marginal-check power supply output for distribution to the modules. The top switch selects the +10 volt supply routed to terminal A of all modules in the panel. In the down position the normal fixed +10 volt supply connected to the red terminal is supplied to the modules, and in the up position the marginal-check voltage supplied to the green terminal is supplied to terminal A of the modules. The center switch performs the same selection as the top switch for connection of a nominal +10 volt level to terminal B of all modules in the panel. The bottom switch selects the -15 volt supply to be routed to terminal C of all pulse amplifier modules in the panel. In the down position the normal 15-volt output of the fixed power supply, received at the blue terminal, is supplied to pulse amplifier modules. In the up position the marginal-check voltage, connected to the yellow terminal, is supplied to terminal C of all pulse amplifier modules.

The normal/marginal switches at the end of panel 1B are wired slightly differently so that the top switch selects the +10A supply for all modules in the panel except the sense amplifiers at locations 1B15 through 1B20; the center switch functions as normal; and the bottom switch selects the +10A supply for the sense amplifiers. This connection allows separate checking of the sense amplifiers, since no pulse amplifier modules are contained in the panel.

To perform the checks:

1. Assure that all three normal/marginal-check switches on each module mounting panel are in the down position.

2. Set the -15/off/+10 switch on the marginal-check power supply to the +10 position.

3. Adjust the output of the marginal-check power supply so that the MARGINAL CHECK voltmeter indicates 10 volts.

4. Set the top normal/marginal switch to the up position on the panel to be checked.

5. Start computer operation in a diagnostic program or routine which fully utilizes the circuits in the panel to be tested. If no program is suggested by the normal system application, select an appropriate Maindec program from Table 9-4. To completely test the PDP-5, all Maindec programs listed in Table 9-4 should be performed at elevated and reduced voltages for each terminal (+10A, +10B, and -15C) and for each module mounting panel indicated in the table.

TABLE 9-4 MAINDEC PROGRAMS USED IN MARGINAL CHECKING

Module Panel	Maindec Program					
	501	502	503	510	512	514
1 A		A, B, C	A, B, C			
1 B	A, B, C	A, B				
S A		A*				
1 C	A, B, C					
1 D	A, B, C					
1 E	A, B, C					
1 F				A, B, C	A, B, C	A, B, C

*Bottom normal/marginal switch on module mounting panel 1B.

6. Decrease the marginal-check power supply output until normal system operation is interrupted. Record the marginal-check voltage. At this point marginal transistors can be located and replaced, if desired. Readjust the marginal-check power supply output to the nominal +10 volt level.

7. Restart computer operation. Increase the marginal-check supply output until normal computer operation is interrupted, at which point record the marginal-check voltage. Transistors can again be located and replaced. Readjust the marginal-check power supply to the nominal +10 volt level.

8. Return the top normal/marginal switch to the down position.

9. Repeat steps 4 through 8 for the center normal/marginal switch on the mounting panel being checked.

10. Set the -15/off/+10 switch on the marginal-check power supply to the -15 position and adjust the output until the MARGINAL CHECK voltmeter indicates 15 volts.

11. Set the bottom normal/marginal switch to the up position for the panel to be checked, then repeat step 5.

12. Repeat steps 6 and 7, readjusting the marginal-check power supply to the nominal -15 volt level at the end of each step. Return the bottom normal/marginal switch to the down position.

13. Repeat steps 2 through 12 for each module mounting panel to be tested.

14. Turn the marginal-check power supply control knob fully counterclockwise, and set the -15/off/+10 switch to the off position.

Memory Current Check

Measure and compare the memory currents with the values listed on the memory array label. This label indicates the optimum memory settings determined at the factory. Allow the equipment to warm up for approximately one hour before making measurements. Whenever possible this check should be performed at an ambient temperature of 25 degrees centigrade. Compensate measured read-write and inhibit currents by subtracting 1 milliampere for every degree of ambient temperature above 25°C. (Add 1 milliampere for each degree below 25°C. The Memory Current Check and Sense Amplifier Check procedures must not be performed when the equipment temperature is below 20°C.

Measure the read-write current using the oscilloscope and clip-on current probe at the read side of a fully selected drive line. Synchronize the oscilloscope with the negative-shift of the Memory Read signal at 1C19V. Adjust the read-write current to the value specified on the label of the core memory array label. Clockwise rotation of the lower potentiometer (R13) on the 1701 Power Supply Control module in the 735 Power Supply increases the read-write current.

In like manner, measure the inhibit current by connecting the clip-on current probe at a selected output line of the 1978 Resistor Board at either location 1B24 or 1B25. Synchronize the oscilloscope on the negative shift of the Memory Read signal at 1C19V. Adjust the memory inhibit current to the value indicated on the memory array label. Clockwise rotation of the upper potentiometer (R3) on the 1701 module increases the memory inhibit current.

To obtain consistent measurements, the current probe should be positioned to indicate read current as a negative pulse, and write and inhibit currents as positive pulses as displayed on the oscilloscope. All current amplitude measurements should be made just before the knee in the curve at the trailing edge of a pulse. Note that read and write currents are measured from base line to peak amplitude, not from peak to peak.

Sense Amplifier Check

The 1571 Dual Sense Amplifiers are adjusted for optimum efficiency through marginal checking techniques. This check is not performed on systems containing 4554 Dual Sense Amplifiers, since these modules have a fixed slice level. Perform the Marginal Checks procedure using the Memory Checkerboard Program (Maindec 502) and the bottom switch (+10A) on module mounting panel 1B. Check and, if necessary, adjust each sense amplifier circuit so that approximately equal positive and negative margins can be obtained for the +10A supply. The sense amplifiers are located at 1B15 through 1B20, 1B15 containing SA_0 and SA_1, and 1B20 containing SA_{10} and SA_{11}. The sense amplifier for the more significant bit in a module is adjusted by the upper potentiometer (R26), and the less significant bit is adjusted by means of the lower potentiometer (R28). Clockwise rotation of a potentiometer decreases the clipping level of the sense amplifier.

Type 137 Analog-To-Digital Converter Maintenance

The checks and adjustments presented in this portion of the manual apply only to PDP-5 systems containing the Type 137 option. Maintenance of the Type 137 involves program-repeated operation of the converter performed during each scheduled preventive maintenance to check the general accuracy and function of the option, and adjustment checks and procedures used to verify and/or adjust the operation of specific functional components. The functions which are checked by module are the timing of the 4303 Integrating Single Shot, the -10 volt output of the 1704 Precision Power Supply, the adjustment of the ladder network in the 1574 12-Bit Digital-To-Analog Converter, and the common balance and zero set of the 1572 Difference Amplifier. The timing checks and ladder network adjustments should be performed only when the need to do so is indicated by the converter check or by normal troubleshooting procedures. The -10 volt reference supply and the difference amplifier should be checked approximately

every three weeks or every 100 equipment operating hours, whichever occurs first. Maintenance of the Type 137 option requires use of the following equipment:

a. A potentiometric voltmeter which has infinite input resistance at null and which has an accuracy of ±0.025%.

b. A single-frequency sine wave source, between 30 and 1000 cps. The output should be floating and the amplitude should be variable from 2 to 20 millivolts. A 115-volt 60-cycle power source may be used as this source if it is suitably stepped down in amplitude.

c. A dc source of 5 ±0.5 volts for biasing the output of the sine wave source. A voltage divider connected across output terminals 1E23D (ground) and 1E23E (-10 volts) can be used as this source.

d. A dual-tracer oscilloscope having a vertical-deflection sensitivity of 5 millivolts per centimeter.

There are many ways to check and adjust the components of an analog-to-digital converter. The information and procedures presented here can be varied greatly as a function of the test equipment available and the object of the test or adjustment. Additional background information and procedures for testing and adjusting converters is found in the Analog-Digital Conversion handbook, form E-5100, published by DEC.

Converter Check

This test repeatedly operates the converter by means of a 2-step program. With a known analog input, the conversion result displayed in the accumulator is then verified by the operator.

To perform the check:

1. Physically disconnect the normal analog input from the input to the Type 137. This connection usually is made by means of a connector on panel 1J that can be disconnected. If the connection is made directly to the module connector, it must be broken at terminal 1E24N.

2. Supply a known constant dc voltage to the input connector or to terminal 1E24N. This potential can be obtained by connecting a voltage divider across output terminals D (ground) and E (-10 volts) of the 1704 Precision Power Supply at location 1E23.

3. Store the following 2-instruction sequence into the computer core memory by means of the switch register, LOAD ADDRESS key, and DEPOSIT key on the operator console.

Address		Instruction	Mnemonic
BEG,	6000	6004	ADC
	6001	5200	JMP BEG

4. Start the program by loading the initial address into the MA by means of the switch register and LOAD ADDRESS key; then press the START key.

5. Record and compare the binary number in the accumulator with the value of the voltage connected in step 2. The answer in the accumulator is in 2's complement unsigned representation and can be converted to a decimal voltage value by using Table 9-5.

6. Repeat steps 2, 4, and 5 for several values of input voltage between 0.0 and -10 volts. Record the analog input signal and the binary answer obtained in each measurement. From these results determine if the answers obtained are within the limits specified by the accuracy connection of the converter or if the converter requires adjustment. If no adjustment is necessary, halt the program by lifting the STOP key; then remove the test connections made to the analog input, and restore the normal connection from the signal measured during programmed operation of this system.

TABLE 9-5 ANALOG-DIGITAL NUMBER CONVERSION

Twos Complement Octal Number		Analog Voltage
Signed	Unsigned	(Negative)
4000	0000	0.
4001	0001	0.00244140625
4002	0002	0.0048828125
4004	0004	0.009765625
4010	0010	0.01953125
4020	0020	0.0390625
4040	0040	0.078125
4100	0100	0.15625
4200	0200	0.3125
4400	0400	0.625
5000	1000	1.25
6000	2000	2.5
0000	4000	5.
2000	6000	7.5
3000	7000	8.75
3400	7400	9.375
3600	7600	9.6875
3700	7700	9.84375
3740	7740	9.921875
3760	7760	9.9609375
3770	7770	9.98046875
3774	7774	9.990234375
3776	7776	9.9951171875
3777	7777	9.99755859375
---	10000	10.

Integrating Single Shot Check and Adjustment

Check the timing of the 4303 module at location 1E18 to assure that sufficient time is allowed for the conversion of each bit. To perform the check:

1. Connect the oscilloscope signal input to terminal 1E18W; connect the trigger input to 1E18K, and adjust for synchronizing on an external negative pulse.

2. Perform steps 3 and 4 of the previous procedure.

3. Observe that the pulse displayed on the oscilloscope is negative for the duration listed under "Conversion Time per Bit" and occurs every 12 microseconds plus the duration listed under the column "Instruction Execution Time" in Table 4-3 for the adjusted bit accuracy of the converter. Make any necessary adjustment in the conversion time by turning the potentiometer in the 4303 module (accessible through a hole in the handle of module 1E18).

Precision Power Supply Check and Adjustment

The -10 volt output of the 1704 Precision Power Supply module at location 1E23 supplies the reference voltage used by the level amplifiers and determines the accuracy of the analog voltage generated by the converter ladder network. A rough check of this adjustment can be made using the oscilloscope. However, an accurate check or adjustment MUST be made with a high impedance instrument which is accurate to within at least 0.1%, such as the John Fluke potentiometric voltmeter. Adjustment of the supply must be performed within 1 minute due to drifting of the voltmeter. To adjust the supply:

1. Calibrate the potentiometric voltmeter.

2. Connect the potentiometric voltmeter between terminals 1E23D (ground) and 1E23E (-10 volts).

3. Turn the screw-driver adjustment, accessible through the hole in the

handle of the module, until the voltmeter indicates -10 vdc ±0.1 mv. (This adjustment controls the setting of the fine control potentiometer R7 shown on schematic diagram RS-1704. The coarse control potentiometer R9 and the current control potentiometer R2 are preset at the factory and must not be adjusted in the field.)

If the output of the supply is 0.0 volts check the external circuit for short circuits to ground. If the output can not be adjusted within the tolerance specified in this procedure, return the module to the factory for calibration.

Digital-To-Analog Converter Check and Adjustment

This procedure is performed to check and adjust the ladder network of the 1574 12-Bit Digital-To-Analog Converter module at location 1E22. This procedure should be used if the module has been subjected to a drastic change in temperature, a mechanical shock sufficient to change the setting of the potentiometers, or following repair or replacement of the level amplifiers on the 4678 modules associated with bits 0 through 7. This test checks and aligns the ladder to compensate for variations in resistors of the divider network and for variations in the output impedance of the level amplifiers. The ladder output voltage obtained only from the bit to be tested is compared with the output voltage resulting from all of the bits of lesser significance. The difference is trimmed so that it is equal to one least significant bit. This is accomplished by a test configuration which monitors the output of the module or terminal 1E22E on a high-gain ac-coupled oscilloscope as the content of the bit being adjusted and the complementary content of all of the lesser significant bits are program alternated. All bits of greater significance are disabled by permanent test connections to stimulate zeros, and the test is performed from the least significant to the most significant adjustable bits (from bit 7 to bit 0).

The ladder network is shown on engineering schematic RS-1574. This module contains a biasing leg consisting of potentiometer R1 and resistor R10, adjustable-resistance legs containing potentiometers R2 through R9 for bits 0 through 7, non-adjustable legs for bits 8 through 11 containing odd-numbered resistors R28 through R33, and the terminating resistor R34. The module is physically arranged in three horizontal groups of circuits. The group of circuits at

the top of the module contains potentiometer R5 for bit 3, R4 for bit 2, R3 for bit 1, and R2 for bit 0 progressing from the handle end to the connector end of the module. The center group of circuits contains potentiometer R9 for bit 7, R8 for bit 6, R7 for bit 5, and R6 for bit 4 progressing from the handle towards the connector end of the module. The bottom group of circuits contains fixed resistors R27 for bit 8, R29 for bit 9, R31 for bit 10, R33 for bit 11, and R34, the terminating resistor progressing from the handle towards the connector. The biasing resistor R1 is also located on the bottom group of circuits near the connector end.

Perform the test as follows:

1. Connect the oscilloscope input to terminal 1E22E and adjust it for negative internal sweep triggering. Be sure the oscilloscope is solidly connected to the analog ground at terminal 1E23D. The oscilloscope vertical preamplifier should be set to a sensitivity of approximately 5 millivolts per centimeter and calibrated with an external reference so that the least significant bit value of 2.4 millivolts can be readily observed.

2. Turn off all power in the PDP-5; remove the ladder module at location 1E22 by means of a 1960 System Module Puller; connect a 154 System Module Extender into the module connector at location 1E22; insert the ladder module to the extender, and then restore PDP-5 power.

3. Connect the analog ground at terminal 1E24D to the level amplifier input terminals corresponding to bits 0 through 6 at terminals 1E21F, 1E21H, 1E21J, 1E21K, 1E21L, 1E20F, and 1E20H.

4. Store the program listed in Table 9-6 in the PDP-5 core memory by means of the switch register, LOAD ADDRESS key, and DEPOSIT key. If this test is to be repeated periodically, the program can be punched on tape and stored by means of the Readin Mode Loader as described in Section 8 of this manual.

TABLE 9-6 DIGITAL-TO-ANALOG CONVERTER ADJUSTMENT PROGRAM

Address	Content	Mnemonic	Comments
6000	7200	CLA	INITIALIZE
6001	1107	TAD PAD	FETCH PATTERN ADDRESS-1
6002	7001	IAC	CORRECT PATTERN ADDRESS
6003	3007	DCA	STORE CORRECTED PATTERN ADDRESS
6004	1607	TAD I PAD	LOAD APPROPRIATE PATTERN
6005	7040	CMA	COMPLEMENT PATTERN
6006	5005	JMP .-1	ALTERNATE PATTERN CONTINUOUSLY
PAD 6007	6007		PATTERN ADDRESS (PAD)
6010	0020		PATTERN BIT 7
6011	0040		PATTERN BIT 6
6012	0100		PATTERN BIT 5
6013	0200		PATTERN BIT 4
6014	0400		PATTERN BIT 3
6015	1000		PATTERN BIT 2
6016	2000		PATTERN BIT 1
6017	4000		PATTERN BIT 0

5. Start the program by loading the initial address into the MA by means of the switch register and the LOAD ADDRESS key.

6. Read and record the value of the two levels of the square wave displayed on the oscilloscope. The higher amplitude value corresponds to the condition when the bit being checked (bit 7) is a binary 1 and all less significant bits are zeros. The lower amplitude value corresponds to the condition when the bit being checked is a binary 0 and all less significant bits are ones. Compare these two values, and adjust the potentiometer (R9 for bit 7) until the higher amplitude is 2.4 millivolts greater than the smaller amplitude, or until the higher amplitude is equal to the value listed in

Table 9-5. During this adjustment it is possible to invert the relative values of the two signal amplitudes; so care should be taken to prevent adjustment so that the bit being checked is of lower value than the value of the less significant bits.

Since the ladder potentiometers are wire wound, it is necessary to assure that they are adjusted to a stable position in which the sliding arm is resting in a position that cannot be moved in either direction by vibration or shock. Therefore, after adjusting the potentiometer, tap the module once or twice, and note any change in the output voltage displayed on the oscilloscope. If a change is observed, readjust the potentiometer to a more stable position closer to the ideal value.

7. Stop the program by lifting the STOP key on the operator console.

8. Disconnect the ground connection from terminal 1E20H made during step 3.

9. Check bit 6 by repeating steps 5 through 7 and adjusting potentiometer R8. Then disconnect the ground connection made to terminal 1E20F made during step 3.

10. Check bit 5 by repeating steps 5 through 7 and adjusting potentiometer R7. Then disconnect the ground connection made to terminal 1E21L during step 3.

11. Check bit 4 by repeating steps 5 through 7 and adjusting potentiometer R6. Then disconnect the ground connection made to terminal 1E21K during step 3.

12. Check bit 3 by repeating steps 5 through 7 and adjusting potentiometer R5. Then disconnect the ground connection made to terminal 1E21J during step 3.

13. Check bit 2 by repeating steps 5 through 7 and adjusting potentiometer R4. Then disconnect the ground connection made to terminal 1E21H during step 3.

14. Check bit 1 by repeating steps 5 through 7 and adjusting potentiometer R3. Then disconnect the ground connection made to terminals 1E21F and 1E23D during step 3.

15. Check bit 0 by repeating steps 5 through 7 and adjusting potentiometer R2.

The zero end point of the ladder network can be checked and adjusted as follows:

1. Load a word containing all zeros into any convenient core memory address by means of the switch register, LOAD ADDRESS key, and the DEPOSIT key. Then clear the accumulator by setting this word into the AC by means of the switch register, LOAD ADDRESS key, and the EXAMINE key.

2. Calibrate the oscilloscope so that analog ground can be determined by a fixed position on the graticule.

3. Connect the oscilloscope to the ladder output at terminal 1E22E, and measure any voltage differential between the analog ground and the ladder output. Adjust the biased terminal potentiometer R1 until no difference can be measured between the output voltage and analog ground.

4. Disconnect the ladder inputs from analog ground.

The full scale end point of the ladder network can be checked and adjusted as follows:

1. Load a word containing all binary ones into the AC by using the keys and switches on the operator console as in step 1 of the previous procedure.

2. Connect the oscilloscope input to terminal 1E23E, and adjust the position to some fixed measuring point on the graticule; then disconnect the oscilloscope from this point.

3. Connect the oscilloscope input to terminal 1E22E and measure the output voltage of the ladder network. Adjust the output of the 1704 Precision Power Supply module at location 1E23 until the voltage obtained on the oscilloscope is exactly -10 volts.

4. Remove all test connections.

Since the two end point adjustments interact, it is difficult to align them both perfectly while maintaining linearity. A somewhat more convenient method is to adjust the zero and half-full scale points for optimum fit, which permits closer control over the lower-weighted (and therefore more error sensitive) bits. The two end points can be checked and adjusted more accurately if the potentiometric voltmeter is substituted for the oscilloscope in the two preceding procedures.

The Difference Amplifier Check and Adjustment

The 1572 Difference Amplifier module at location 1E24 should be tested periodically and at any time when it has undergone severe temperature change or mechanical shock. The need for readjustment depends upon the accuracy required and upon the environment. Adjustment of the common balance is made by turning potentiometer R1 (accessible through the lower hole in the module handle), and zero set is adjusted by means of potentiometer R4 (accessible through the upper hole in the module handle).

To perform the checks:

1. De-energize the PDP-5; remove the module from location 1E22; then energize the PDP-5.

2. Connect the two inputs of a dual-trace oscilloscope to the two output terminals 1E24F and 1E24W of the difference amplifier. Connect the oscilloscope ground to the module ground at terminal 1E24D.

3. Connect the difference amplifier input terminals 1E24N and 1E24P to an ungrounded sine wave source of approximately 10 millivolts amplitude, 30 to 1000 cps, and biased at - 5 volts.

4. Connect the oscilloscope trigger input to one of the difference amplifier input terminals to synchronize the trace.

5. Observe that the two difference amplifier output signals displayed on the oscilloscope appear as two complementary square waves. Adjust the lower module potentiometer so that the output signal at terminal 1E24 W is symmetrical, and then adjust the upper module potentiometer until the output signal at terminal 1E24F is symmetrical (these adjustments must be performed in the sequence given).

To improve the resolution of these adjustments, repeat the procedure with the sine wave input reduced to 5 millivolts. It may be necessary to repeat the adjustment sequence several times since there is interaction between the two potentiometers.

This concludes the maintenance of the Type 137 Analog-To-Digital Converter. De-energize the PDP-5, test connections, and restore the original connections and condition of the converter.

CORRECTIVE MAINTENANCE

The PDP-5 is constructed of highly reliable transistorized modules. Use of these circuits and faithful performance of the preventive maintenance tasks ensure relatively little equipment down time due to failure. Should a malfunction occur, the condition should be analyzed and corrected as indicated in the following procedures. No special tools or test equipment are required for corrective maintenance other than a broad bandwidth oscilloscope and a standard multimeter. However, a clip-on current probe such as the Tektronix Type P6016 with a Type 131 Current Probe Amplifier is very helpful in monitoring memory currents. The best corrective maintenance tool is a thorough understanding of the physical and electrical

characteristics of the equipment. Persons responsible for maintenance should become thoroughly familiar with the system concept, the logic drawings, the operation of specific module circuits, and the location of mechanical and electrical components.

It is virtually impossible to outline any specific procedures for locating faults within complex digital systems such as the PDP-5. However, diagnosis and remedial action for a fault condition can be undertaken logically and systematically in the following phases:

a. Preliminary investigation to gather all information and to determine the physical and electrical security of the computer.

b. System troubleshooting to locate the fault to within a module through the use of control panel troubleshooting, signal tracing, or aggravation techniques.

c. Circuit troubleshooting to locate defective parts within a module.

d. Repairs to replace or correct the cause of the malfunction.

e. Validation tests to assure that the fault has been corrected.

f. Log entry to record pertinent data.

Preliminary Investigation

Before commencing troubleshooting procedures, explore every possible source of information. Ascertain all possible information concerning any unusual function of the machine prior to the fault and all possible data about the symptoms given when the fault occurred, such as the program in progress, condition of operator console indicators, etc. Search the maintenance log to determine if this type of fault has occurred before or if there is any cyclic history of this kind of fault, and determine how this condition was previously corrected. When the entire machine fails, perform a visual inspection to determine the physical and electrical security of all power sources, cables, connectors, etc. Assure that the power supplies are working properly and that there are no power short circuits by performing the Power Supply Checks as

described under Preventive Maintenance. Check the condition of the air filter in the bottom of the cabinet. If this filter becomes clogged, the temperature within the cabinet might rise sufficiently to cause marginal semiconductors to become defective.

System Troubleshooting

Do not attempt to troubleshoot the system without first gathering all information possible concerning the fault, as outlined in the Preliminary Investigation.

Commence troubleshooting by performing that operation in which the malfunction was initially observed, using the same program. Thoroughly check the program for proper control settings. Careful checks should be made to assure that the PDP-5, and not the peripheral equipment, is actually at fault before continuing with corrective maintenance procedures. Faults in equipment which transmits or receives information or improper connection of the system frequently give indications very similar to those caused by computer malfunction. Faulty ground connections between peripheral equipment and the computer are a common source of trouble. From that portion of the program being performed and the general condition of the indicators, the logical section of the machine at fault can usually be determined.

If the fault has been determined to be within the computer but cannot be immediately localized to a specific logic function, it can usually be determined to be within either the core memory or the processor logic circuits. Proceed to the Memory Troubleshooting or Logic Troubleshooting procedures. When the location of a fault has been narrowed to a logic element, continue troubleshooting to locate the defective module or component by means of signal tracing. If the fault is intermittent, a form of aggravation test should be employed to locate the source of the fault.

Memory Troubleshooting

If the entire memory system fails, use the multimeter to check the outputs of the 735 Power Supply. Measure the voltages at the terminal strip as indicated on engineering drawing BS-D-5-0-17. Do not attempt to adjust this supply. If the supply is defective, troubleshoot it and correct the cause of the trouble; then adjust the output voltage by performing the Memory Current Check. If the power supply is functioning properly, proceed as follows:

1. De-energize the computer.

2. Connect a jumper from chassis ground to the following module terminals: 1C19Z, 1C09Y, 1C11J, and 1D01T.

3. Remove the modules at locations 1C01 through 1C03 and 1C12 through 1C14.

4. Restore computer power and press the START key.

This procedure causes the memory address register to advance in a normal binary counting sequence and causes the memory to cycle continuously. With the memory cycling continuously (from the preceding procedure or by a simple program loop) continue troubleshooting by using the oscilloscope and current probe to measure full read and write currents at the output of the 1989 Memory Driver modules. Measure read current at 1A04V and write current at 1A03V. If these currents are far in excess of the value specified on the memory, multiple address selection is indicated. If the base line of the oscilloscope trace is present during the read or write current pulse, an address is not being selected. Check the 1987 Read-Write Switches for short circuits or for a permanently closed switch when multiple address selection is indicated. When nonselection is indicated, check the 1987 modules for an open or disabled switch. Also check the 1976 Resistor Board modules for an open circuit and check the 2010 Memory Diode Unit modules for an open diode if nonselection occurs.

If the read and write currents are acceptable at the output of the memory drivers, use the oscilloscope and current probe to trace them to the core array. Trace read current from 1A04V through the wiring to terminal S of each of the read-write switches at locations 1A08 through 1A05. Trace write current from A103V through the wiring to terminal S of each of the read-write switches at locations 1A12 through 1A09. When read-write current is not observable at terminal S of a read-write switch, continue tracing the current from the output of the previous read-write switch to one of the memory plug connectors at locations 1A13 through 1A21. Refer to engineering drawing BS-D-5-0-16 when tracing read-write current in this manner.

Perform the Memory Address Test program (Maindec 503) to locate defective core memory addresses. Complete the entire program and record all addresses which fail. Inspect the record of failure addresses for common bits. Refer to engineering drawing BS-D-5-0-16 and Table 3-1, and check the read-write switches that decode common bits of the failing addresses. If

this read-write switch is on the read side of the array, also check the associated resistor board; if it is on the write side of the array, also check the associated memory diode units. Substituting a known good memory diode unit at successive locations for each pass of the memory Address Test program is an effective troubleshooting technique.

If an address is dropping bits, use the operator console to deposit all binary ones in that address. Then examine the address to determine which bit position is not being set (contains a 0). Check the sense amplifier, inhibit driver, and resistor board for the associated bit. If bits are dropping out, check the memory inhibit current as described in the Memory Current Check.

If an address is picking up bits, use the operator console to deposit all binary zeros in that address, and proceed as described in the previous paragraph.

To locate the cause of a specific address failure, use the oscilloscope and current probe to trace read and write current while performing a repetitive program such as the memory Address Test program or the Memory Checkerboard Test program. Trace read current from 1A04V through the wiring to terminal S of each of the read-write switches at locations 1A08 through 1A05. Trace write current from 1A03V through the wiring to terminal S of each of the read-write switches at locations 1A12 through 1A09. When read-write current is not observable at terminal S of a read-write switch, continue tracing the current from the output of the previous read-write switch to one of the memory plug connectors at location 1A13 through 1A21. Refer to engineering drawing D-5-0-16 when tracing read-write current in this manner.

Perform the Memory Checkerboard Test program (Maindec 502) to troubleshoot all other memory conditions.

Logic Troubleshooting

If the instructions do not seem to be functioning properly, perform the Instruction Test program (Maindec 501). This test halts to indicate instructions that fail. When an instruction fails, as indicated by the operator console indicators when the program stops, manually load a short program loop which exercises that instruction. For example, if the rotate right instruction fails, load the program:

```
        CLA  CLL
        TAD (4000)
A,      RAR
        JMP A
```

With the SINGLE STEP switch on (set to the right) this program can be executed by repeated operation of the CONTINUE key, and the advance of a single 1 through the accumulator and link can be observed. Failure of a routine of this nature should suggest specific areas of logic circuits to be checked by signal tracing.

If the computer interrupt system or the Teletype teleprinter do not seem to be functioning properly, perform the Teleprinter Test program (Maindec 514). If the Teletype tape reader or punch operation is questionable, perform the Read Paper Tape Test (Maindec 510) or the Punch Tape Test (Maindec 512). Refer to the Teletype documents for detailed maintenance information on the Model 33 ASR set.

Signal Tracing

If the fault has been located within a functional logic element, program the computer to repeat some operation in which all functions of that element are utilized. Use the oscilloscope to trace signal flow through the suspected logic element. Oscilloscope sweep can be synchronized by control signals or clock pulses, which are available on individual module terminals at the wiring side (front) of the equipment. Circuits transferring signals with external equipment are most likely to encounter difficulty. Trace output signals from the interface connector back to the origin, and trace input signals from the connector to the final destination. The signal tracing method can be used to certify signal qualities such as pulse amplitude, duration, rise time, and the correct timing sequence. If an intermittent malfunction occurs, signal tracing must be combined with an appropriate form of aggravation test.

Aggravation Tests

Intermittent faults should be traced through aggravation techniques. Intermittent logic malfunctions are located by the performance of marginal-check procedures as described under Preventive Maintenance.

Intermittent failures caused by poor wiring connections can often be revealed by vibrating modules while running a repetitive test program. Often, wiping the handle of a screw driver across the back of a suspect panel of modules is a useful technique. By repeatedly starting the test program and vibrating fewer and fewer modules, the malfunction can be localized to within one or two modules. After isolating the malfunction in this manner, check the seating of the modules in the connector; check the module connector for wear or misalignment, and check the module wiring for cold solder joints or wiring kinks.

Circuit Troubleshooting

The procedure followed for troubleshooting and correcting the cause of faults within specific circuits depends upon the down time limitations of equipment use. Where down time must be kept at a minimum, it is suggested that a provisioning parts program be adopted to maintain one spare module, power supply, or standard component which can be inserted into the cabinet when system troubleshooting procedures have traced the fault to a particular component. Static and dynamic bench tests can then be performed without interfering with system operation. Where down time is not critical, the spare parts list can be reduced and module troubleshooting procedures can be performed with the modules in-line (within the system). Although in-line module troubleshooting extends the down time of the system, it is economical of personnel time because the module can be program exercised to locate the cause of the fault more rapidly.

Module Circuits

Circuit schematics of each module are supplied in Section 10 of this manual and should be referred to for detailed circuit information. The basic function and specifications for standard systems modules are presented in the System Modules Catalog, C-100. The following design considerations may also be helpful in troubleshooting such standard modules:

a. Forward-biased silicon diodes are used in the same manner as Zener diodes, usually to provide a voltage differential of 0.75 volts. For instance a series string of four diodes is used to produce the -3 vdc clamp voltage used in most modules.

b. The state of DEC flip-flops is changed by an incoming pulse which turns

off the conducting transistor amplifier. Since these flip-flops use PNP transistors, the input pulse must be positive and must be coupled to the base of the transistor. Flip-flop modules that accept negative pulses to change the state invert this pulse by means of a normal transistor inverter circuit.

c. Fixed-length delay lines such as the 1310 and 1311 are extremely reliable and very seldom malfunction. However, if a malfunction should occur, these delay lines should not be replaced on the printed-wiring board. In such cases the entire module should be returned to DEC for repair.

d. Each 4301 Delay module consists of an input buffer amplifier which is transformer-coupled to a monostable multivibrator. The multivibrator output is directly coupled to a level amplifier and transformer coupled to an output pulse amplifier.

e. The 1607 and 4603 modules both contain three independent pulse amplifiers, each with its own input inverter. Output pulse duration is determined by the time required to saturate the interstate coupling transformer. No multivibrators or other RC timing circuits are used in the pulse amplifiers.

f. The 4604 and 4606 Pulse Amplifier modules both contain three independent circuits, each containing a monostable multivibrator and an output pulse amplifier. The period of the multivibrator is established by an RC time constant which is determined by external connections to the module. The output from the pulse amplifier is determined by the period of the monostable multivibrator and so ranges between 0.4 and 1 microsecond.

In-Line Dynamic Tests

To troubleshoot a module while maintaining its connection within the system:

1. De-energize the computer.

2. Remove the suspect module from the mounting panel by means of a 1960 System Module Puller.

3. Insert a 1954 System Module Extender into the mounting panel connector which normally holds the suspect module.

4. Insert the suspect module into the module extender. All components and wiring points of the module are now accessible.

5. Energize the computer and establish the program conditions desired for troubleshooting the module. Trace voltages or signals through the module, using a dc voltmeter or an oscilloscope, until the source of the fault is located.

In-Line Marginal Checks

Marginal checks of individual modules can be performed within the computer to test specific modules of questionable reliability, or to further localize the cause of an intermittent failure which has been localized to within one module mounting panel by the normal marginal checking method. These checks are performed with the aid of a modified 1954 System Module Extender. To modify an extender for these checks, disconnect the small wire leads from terminals A, B, and C of the connector block, and solder a 3-foot test lead to each of the three wires. Attach a spade lug, such as an AMP 42025-1 Power Connector, to the end of each test lead, and label each lead to correspond to the A, B, or C terminal from which the wire was disconnected. To marginal check a module within the computer:

1. De-energize the computer.

2. Remove the module to be checked from the module mounting panel; replace it with the modified extender, and insert the module in the extender.

3. Connect test leads A, B, and C to the appropriate terminals of the color-coded connector at the end of the mounting panel. The module being checked can draw the power from the marginal-check power supply via the green (+10 vdc) or yellow (-15 vdc) terminals, or from the normal power supply via the red (+10 vdc) or blue (-15 vdc) terminals. Note that the marginal check switches at the end of the rack should remain in the down position during the entire procedure.

4. Restore computer power, adjust the marginal-check power supply to provide the nominal voltage output, and start operation of a routine which fully utilizes the module being checked. The procedures and routines suggested in Preventive Maintenance for use in marginal checking the computer can be used as a guide to marginal checking modules.

5. Increase or decrease the output of the marginal-check power supply until the routine stops, indicating module failure. Record each bias voltage at which the module fails. Also record the condition of all operator console controls and indicators when a failure occurs. This information indicates the module input conditions at the time of the failure and is often helpful in tracing the cause of a fault to a particular component part.

6. Repeat steps 4 and 5 for each of the three bias voltages. If margins of ±5 volts on the ±10 vdc supplies can be obtained, and the -15 vdc supply can be adjusted between -7 volts and -18 volts without module failure, a module can be assumed to be operating satisfactorily. If the module fails before these margins are obtained, use normal signal tracing techniques within the module to locate the source of the fault.

If an external dual-voltage variable power supply is available, such as a DEC 730, perform steps 1 and 2; connect test leads A, B, and C to either the normal machine power supplies at the red (+10 vdc) and blue (-15 vdc) terminals at the end of the module panel or directly to output at this supply; then continue the procedure from step 4. When using this connector, the ground connections of the dual-voltage supply must be connected to computer signal ground. This connection can be made to the black connector at the end of any module mounting panel.

Static Bench Tests

Visually inspect the module on both the component side and the printed-wiring side to check for short circuits in the etched wiring and for damaged components. If this inspection fails to reveal the cause of trouble or to confirm a fault condition observed, use the multimeter to measure resistances.

CAUTION

Do not use the lowest or highest resistance ranges of the multimeter when checking semiconductor devices. The X10 range is suggested. Failure to heed this warning may result in damage to components.

Measure the forward and reverse resistances of diodes. Diodes should measure approximately 20 ohms forward and more than 1000 ohms reverse. If readings in each direction are the same, and no parallel paths exist, replace the diodes.

Measure the emitter-collector, collector-base, and emitter-base resistances of transistors in both directions. Most catastrophic failures are due to short circuits between the collector and the emitter or are due to an open circuit in the base-emitter path. A good transistor indicates an open circuit in both directions between collector and emitter. Normally 50 to 100 ohms exist between the emitter and the base or between the collector and the base in the forward direction, and open-circuit conditions exist in the reverse direction. To determine forward and reverse directions, a transistor can be considered as two diodes connected back-to-back. In this analogy PNP transistors are considered to have both cathodes connected together to form the base, and both the emitter and collector assume the function of an anode. In NPN transistors the base is assumed to be a common-anode connection, and both the emitter and collector are assumed to be the cathode.

Multimeter polarity must be checked before measuring resistances, since many meters (including the Triplett 630) apply a positive voltage to the common lead when in the resistance mode. Note that although incorrect resistance readings are a sure indication that a transistor is defective, correct readings give no guarantee that the transistor is functioning properly. A more reliable indication of diode or transistor malfunction is obtained by using one of the many inexpensive in-circuit testers commercially available.

Damaged or cold-solder connections can also be located using the multimeter. Set the multimeter to the lowest resistance range and connect it across the suspected connection. Poke at the wires or components around the connection, or alternately rap the module lightly on a wooden surface, and observe the multimeter for open-circuit indications.

Often the response time of the multimeter is too slow to detect the rapid transients produced by intermittent connections. Current interruptions of very short durations, caused by an intermittent connection, can be detected by connecting a 1.5-volt flashlight battery in series with a 1500-ohm resistor across the suspected connection. Observe the voltage across the 1500-ohm resistor with an oscilloscope while probing the connection.

Dynamic Bench Tests

Dynamic bench testing of modules can be performed through the use of special equipment. A 922 Test Power Cable and either a 730 or 765 Power Supply can be used to energize a system module. These supplies provide both the +10 vdc and -15 vdc operating supply for the module as well as ground and -3 volt sources which may be used as signal inputs. The signal inputs can be connected to any terminal normally supplied by a logic level by means of eyelets provided on the power cable. Type 911 Patch Cords may be used to make these connections between eyelets on the plug. In this manner logic operations and voltage measurements can be made. When using the 765 Bench Power Supply, marginal checks of an individual module can also be obtained.

Repair

In all soldering and unsoldering operations in the repair and replacement of parts, avoid placing excessive solder or flux on adjacent parts or service lines. When soldering semiconductor devices (transistors, crystal diodes, and metallic rectifiers) which may be damaged by heat, the following special precautions should be taken:

a. Use a heat sink, such as a pair of pliers, to grip the lead between the device and the joint being soldered.

b. Use a 6-volt soldering iron with an isolation transformer. Use the smallest soldering iron adequate for the work.

c. Perform the soldering operation in the shortest possible time, to prevent damage to the component and delamination of the module etched wiring.

When any part of the equipment is removed for repair and replacement, make sure that all leads or wires which are unsoldered, or otherwise disconnected, are legibly tagged or marked for identification with their respective terminals. Replace defective components only with parts of equal or greater quality and equal or narrower tolerance.

Spare Parts

For rapid maintenance and minimum system down time it is suggested that the following spare parts be stocked at or near each installation:

1. A complete Model 33 Automatic Send Receive set by Teletype Corporation.

2. The quantity of transistors and diodes listed in Table 9-7.

3. The quantity of miscellaneous spare parts listed in Table 9-8.

4. The quantity of Potter Instrument Company spare parts listed in Table 9-9 for systems containing Type 50 Magnetic Tape Transports containing the Potter Instrument Model 90611-2 mechanism.

5. One of each module or accessory in the following list for the standard PDP-5 and the appropriate options.

TABLE 9-7 SUGGESTED SPARE SEMICONDUCTORS

Quantity	Type	Vendor
	Transistors	
4	2N2451	Sprague
1	2N2488	Sprague
1	2N2489	Sprague
1	2N527	General Electric
2	2N599	Texas Instrument
1	2N2894-1	Fairchild
1	2N2894-3	Fairchild
2	2N2714	General Electric

TABLE 9-7 SUGGESTED SPARE SEMICONDUCTORS (continued)

Quantity	Type	Vendor
10	2N1754	Sprague
2	2N1304	Texas Instrument
7	2N1305	Texas Instrument
2	2N1309	Texas Instrument
2	2N2904	Motorola
1	2N398A	Motorola
1	DEC 3009	DEC
	Diodes	
2	D007	DEC
10	1N645	Transitron
1	1N748	Transitron
10	1N914	Transitron
20	1N994	Transitron

TABLE 9-8 SUGGESTED MISCELLANEOUS SPARE PARTS

Quantity	Item	Part No.	Vendor
1	Switch for Bat-Handle Keys	Telever Switch 16006 Cat. No. S-302 Reworked per DEC Drawing MA-C-01510	Switchcraft Inc.
2	Sub Miniature Toggle Switches	6AT1 2 Position SPDT Micro Switch	Micro Switch
1	Lockout Switch	1575-L DPDT	Arrow Hart
1	Rotron Fan	53E168 Type CFG	Rotron Mfg. Co.
1	Rotron Filter	34-X1431	Rotron Mfg. Co.
3	Indicator Lights	MC48-639B	Transistor Electric

TABLE 9-9 SUGGESTED SPARE PARTS FOR TYPE 50 MAGNETIC TAPE TRANSPORTS

Quantity	Item	Part Number
1	Tension Arm	425633-2
1	Vacuum Motor	S 209-5273
2	Break Pads	352719
1	Ferrite Plate	423252-3
2	Drag Plate	419056-2
1	Bulb and Tube Assembly	427513
1	Pinch Roller	419260
1	Potentiometer	812-3
1	Cleaning Kit	452-484
1	Solar Cell (Upper)	A 413314-1
1	Solar Cell (Lower)	A 413314-2
1	Idle Bearing	206-5279
1	Servo Amplifier Module	3323-101

Standard PDP-5 Spare Module List

735	1684	4114	4410
737	1685	4115	4603
779	1701	4116	4604
832	1976	4117	4605
1000	1978	4127	4606
1011	1982	4129	4706
1020	1987	4130	4707
1151	1989	4206	4801
1310	4102	4215	4802
1311	4106	4225	4903
1406	4111	4301	4904
1571/4554	4112	4401	6102
1607	4113	4407	

Type 34B Oscilloscope Display Spare Module List

1564	4126	4303	4687
1704	4214	4676	
4105	4220	4678	

Type 50 Magnetic Tape Transport Spare Module List

1536	1669	4105	4514
1542	1681	4303	

Type 57A Automatic Tape Control with Type 157 Interface Spare Module List

1150	4213	4303	4305
4143	4222	4304	6122

Type 75A High Speed Perforated Tape Punch and Control Spare Module List

4105	4220	4681

Type 137 Analog-To-Digital Converter Spare Module List

1572	1704	4303	4678
1574			

Type 139 General Purpose Multiplexer and Control Spare Module List

1578	4222	4202	6401
4150			

Type 153 Automatic Multiply and Divide Spare Module List

4123	4205	4218	4231

Type 154 Memory Extension Control Spare Module List

4151	4217	4218	4220

Type 155 Memory Module Spare Module List

None

Type 350 Incremental Plotter and Control Spare Module List

4303	4667

Type 552 DECtape (formerly called Microtape) Control Spare Module List

1501	4218	4260	4671
1802	4222	4303	4689
4110	4227	4306	
4151	4228	4523	

Type 750 High Speed Perforated Tape Reader and Control Spare Module List

4220

Validation Test

Following the replacement of any electrical component of the equipment, a test should be performed to assure the correction of the fault condition and to make any adjustments of timing or signal levels affected by the replacement. This test should be taken from the Preventive Maintenance procedure most applicable to the portion of the system in which the error was found. For example, if a filter capacitor is replaced in a section of the 779 Power Supply, the ripple check for that section should be repeated as specified under Power Supply Checks. If repairs or replacement are made in an area which is not checked during preventive maintenance, the appropriate diagnostic program (Maindec) should be run or an appropriate operational test should be devised. For example, if a flip-flop is repaired or replaced, the register or control function performed by the flip-flop should be completely checked by manual setting and clearing, by improvised programmed exercise of the function, or by performance of the appropriate diagnostic program.

When time permits, it is suggested that the entire preventive maintenance task be performed as a validation test. The reasons for this are:

a. If one fault has been detected and corrected, other components may be marginal.

b. While the equipment is down and available, preventive maintenance can be performed and need not be scheduled again for four months (or the normal period).

Log Entry

Corrective maintenance activities are not completed until they are recorded in the maintenance log. Record all data indicating the symptoms given by the fault, the method of fault detection, the component at fault, and any comments which would be helpful in maintaining the equipment in the future.

SECTION 10

PERTINENT DOCUMENTS

PUBLICATIONS

The following documents serve as source material and complement the information in this manual.

a. System Modules catalog, C-100, printed by DEC. This book presents information pertaining to the function and specifications for the basic systems modules and module accessories comprising the PDP-5.

b. Programmed Data Processor-5 Handbook, F-55, printed by DEC. Programming, instruction format, and general computer function are presented in this document.

c. PDP-5 Software Package. Perforated program tapes and descriptive matter for the Program Assembly Language (PAL), utility subroutines, and the maintenance programs (Maindec) are contained in this package prepared by DEC.

d. Instruction manuals and Maindec programs for appropriate input/output devices are prepared by DEC.

e. Technical Manual, Automatic Send and Receive Sets (ASR), Bulletin 273B. This manual covers operation and maintenance of the Teletype unit.

f. Parts, Model 33 Page Printer Set, Bulletin 1184B. This illustrated parts breakdown can be used as a guide to disassembly, reassembly, and ordering parts of the Teletype unit.

One copy of the publications described in b through f is supplied by DEC with each PDP-5. Copies of item a, or additional copies of items b through d can be obtained from the nearest DEC district office or from:

Customer Relations Department
Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts 01754
U.S.A.

Additional copies of items e and f can be procured from:

Teletype Corporation
5555 Touhy Avenue
Skokie, Illinois 60076
U.S.A.

DRAWINGS

Engineering drawings in the following list are reproduced here as an aid to understanding and maintaining the standard PDP-5. A complete set of formal engineering drawings is supplied separately with each PDP-5 system. Should any discrepancy exist between the drawings in this manual and those supplied with the equipment, assume the formal drawings to be correct.

Power Supply and Control

Power Supply	RS-735
Power Supply Control (Module in 735)	RS-1701
Power Supply	RS-737
Power Supply	RS-779
Two Step Power Control	RS-832

System Modules

Clamped Load Resistors	RS-1000
Diode	RS-1011
Memory Diode Unit	RS-1020
Binary-to-Octal Decoder	RS-1151
Delay Line	RS-1310
Delay Line	RS-1311
Crystal Clock	RS-1406
Dual Sense Amplifier	RS-1571
Difference Amplifier	RS-1572
12-Bit Digital-to-Analog Converter	RS-1574
Pulse Amplifier	RS-1607
Bus Driver	RS-1684

System Modules (continued)

Bus Driver	RS-1685
-10V Precision Power Supply	RS-1704
Resistor Board	RS-1976
Resistor Board	RS-1978
Inhibit Driver	RS-1982
Read-Write Switch	RS-1987
Memory Driver	RS-1989
Inverter	RS-4102
Inverter	RS-4106
Diode	RS-4111
Negative Diode NOR	RS-4112
Diode	RS-4113
Negative Diode NOR	RS-4114
Positive Diode NOR	RS-4115
Diode	RS-4116
Positive Diode NOR	RS-4117
Negative Capacitor Diode Gate	RS-4123
Pulse Inverter	RS-4127
Pulse Inverter	RS-4129
Positive Capacitor-Diode Gate	RS-4130
Binary-to-Octal Decoder	RS-4151
Dual Flip-Flop	RS-4205
Triple Flip-Flop	RS-4206
4-Bit Counter	RS-4215
4-Bit Counter	RS-4217
Quadruple Flip-Flop	RS-4218
8-Bit Buffer Register	RS-4220
8-Bit BCD or Binary Counter	RS-4225
Quadruple Flip-Flop	RS-4231
Delay (One Shot)	RS-4301
Integrating Single Shot	RS-4303

System Modules (continued)

Variable Clock	RS-4401
Crystal Clock	RS-4407
Pulse Generator	RS-4410
Dual Sense Amplifier	RS-4554
Pulse Amplifier	RS-4603
Pulse Amplifier	RS-4604
Pulse Amplifier	RS-4605
Pulse Amplifier	RS-4606
Level Amplifier	RS-4678
Teletype Incoming Line Unit	RS-4706
Teletype Transmitter	RS-4707
22-Pin Plug Adapter with Bus Driver	RS-4801
22-Pin Plug Adapter with Bus Driver	RS-4802
18-Lamp Bracket	RS-4903
9-Lamp Bracket	RS-4904
Inverter	RS-6102

Logic

Flow Diagram	FD-D-5-0-2
Keys, Switches, Run, I/O Halt, SP's, Power Clear	BS-D-5-0-5
Major States, Instruction Register, IOP's	BS-D-5-0-6
MA and MB Control	BS-D-5-0-7
AC Control, Skip, and Interrupt Sync	BS-E-5-0-8
Link, AC, MB, MA (2 sheets)	BS-E-5-0-9
Memory Stack Diagram 4K	BS-E-5-0-11
Memory Stack Diagram 1K	BS-E-5-0-12
Input Mixer	BS-D-5-0-14
Memory "X" and "Y" Selection	BS-D-5-0-16
Memory System Timing, Inhibit, Sense Amplifier Output	BS-D-5-0-17
Keyboard/Printer Control	BS-D-5-0-18

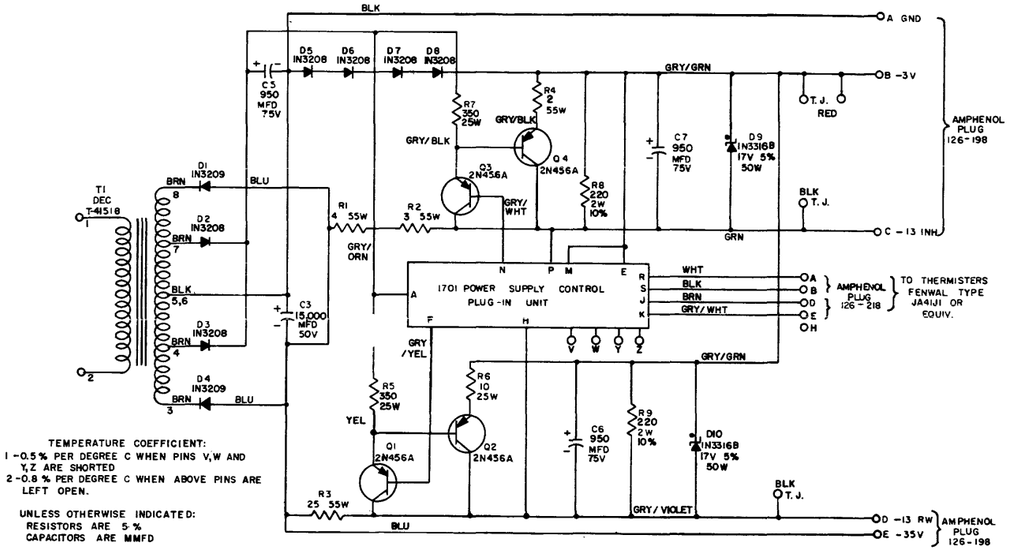
Logic (continued)

Output Bus Drivers	BS-D-5-0-31
Analog-to-Digital Converter	BS-D-137-0-1
AR Control, IOT Gen., Step Counter, Time Gen	BS-D-153-0-5
MQ Register	BS-D-153-0-6
AR Register	BS-D-153-0-7
Flow Diagram, Automatic Multiply and Divide	FD-D-153-0-11
Memory Extension Logic	BS-D-154-0-4

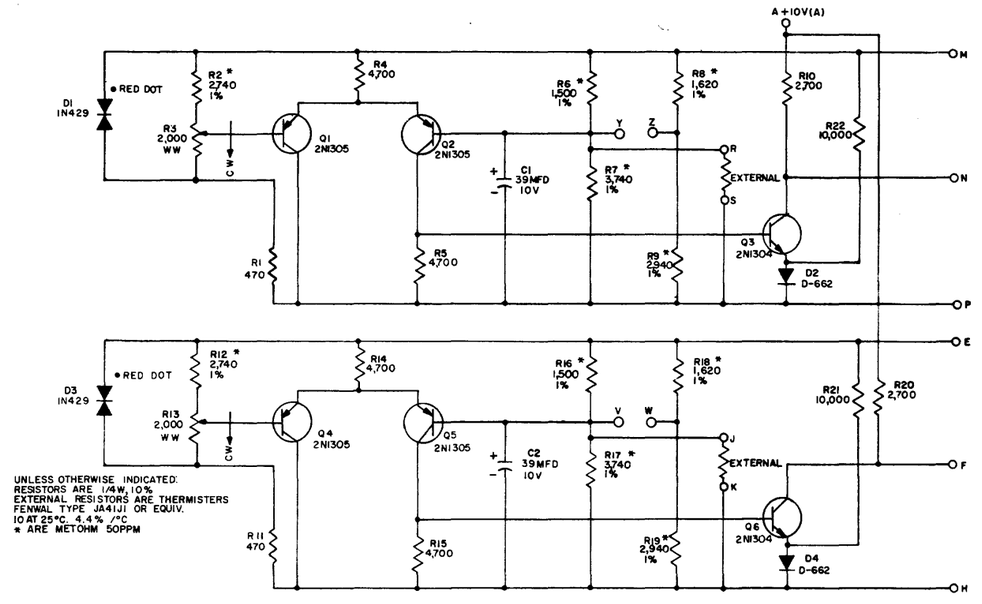
Module Location and Wiring

System Module Location	ML-D-5-0-15
Wiring Diagram 1A, 1B, 1C	WD-E-5-0-3
Wiring Diagram 1D, 1E, 1F	WD-E-5-0-4
Operator Control Keys and Switches	WD-D-5-0-10
Utilization Module List for Type 153	UML-D-153-0-3
Wiring Diagram 1K and 1L (2 sheets)	WD-D-153-0-4
Utilization Module List for Type 154	UML-D-154-0-6
Wiring Diagram for Type 154	WD-D-154-0-5

Power Supply RS-735
Power Supply Control (Module in 735) RS-1701

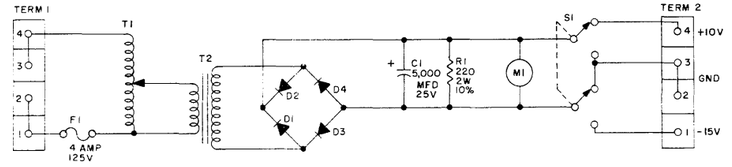


Power Supply RS-735



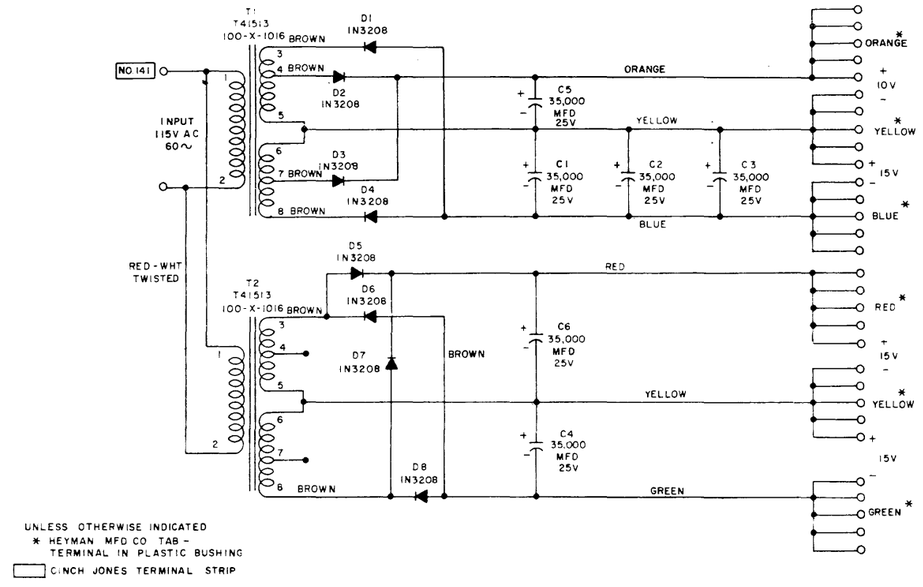
Power Supply Control (Module in 735) RS-1701

Power Supply RS-737
Power Supply RS-779



NOTE:
DIODES ARE IN3208 #MR312 MOTOROLA
TERM 1 & 2 ARE BARRIER TERMINAL BLOCK
#602 3/4 - ST4 KULKA ELECTRIC CORP.
T1 IS A VARIABLE TRANSFORMER #VT2 OHMITE
T2 IS A #F47U TRIAD CO.
F1 IS A SLO-BLO FUSE #313004
M1 IS A DC METER 0-30V RED BEZEL TYPE #DO-91 CAT #518X4 G.E.
S1 IS A TOGGLE SWITCH DPDT, 2 POS. #8386K7 CUTLER HAMMER

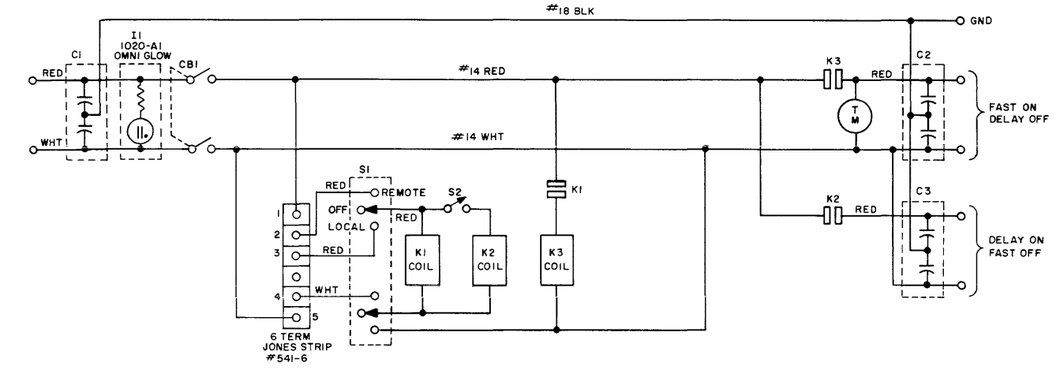
Power Supply RS-737



UNLESS OTHERWISE INDICATED
* HEYMAN MFD CO TAB - TERMINAL IN PLASTIC BUSHING
CINCH JONES TERMINAL STRIP

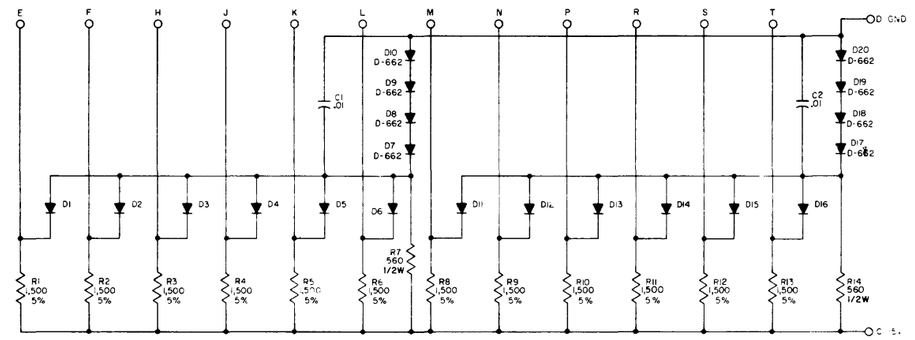
Power Supply RS-779

Two Step Power Control RS-832
Clamped Load Resistors RS-1000



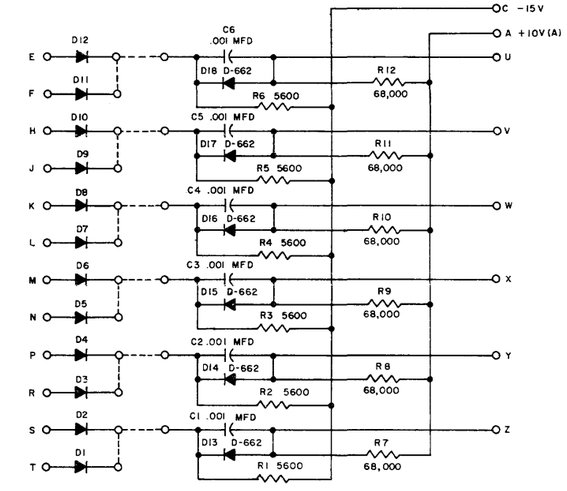
NOTES:
C1 CAPACITOR 2 X .1 MFD 1000VDC #YAT 10011
CORNELL DUBLIER.
C2 & C3 CAPACITOR BATHTUB-DEC PURCH. SPEC #CAF-0001
2X.1MFD 600VDC CORNELL DUBLIER.
S1 TOGGLE SWITCH #ST52P.
S2 TOGGLE SWITCH SPDT 2 POS #7505-KE.
K1 RELAY #1040-8-687 NORMALLY OPEN 115VAC COIL 3-5 SEC DELAY
QUICK OPERATE, SLOW RELEASE.
K2 RELAY #1040-8-58 NORMALLY OPEN 115 VAC COIL 3-5 SEC DELAY
SLOW OPERATE QUICK RELEASE.
K3 RELAY #EM-1 115 VAC EBERT ELECTRONICS.
CB1 CIRCUIT BREAKER #190-220-101 20AMPS 250V, 60 CYC-CURVE 4

Two Step Power Control RS-832



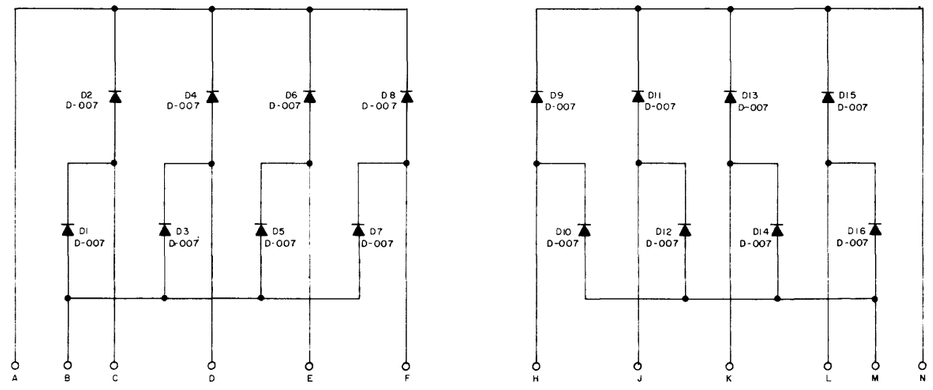
UNLESS OTHEWISE INDICATED:
RESISTORS ARE 1/4W: 10%
CAPACITORS ARE MFF
DIODES ARE D-664

Clamped Load Resistors RS-1000



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%.
DIODES ARE D-001

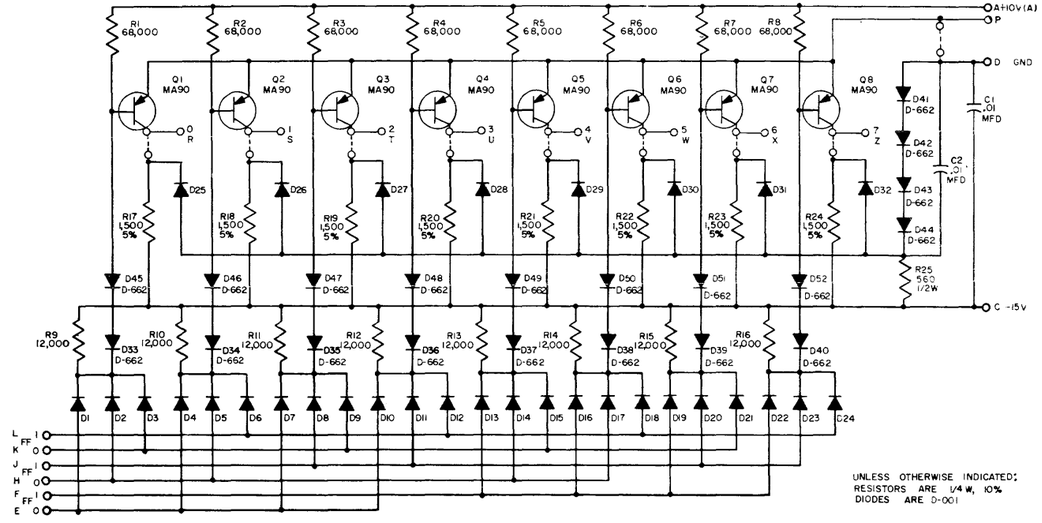
Diode RS-1011



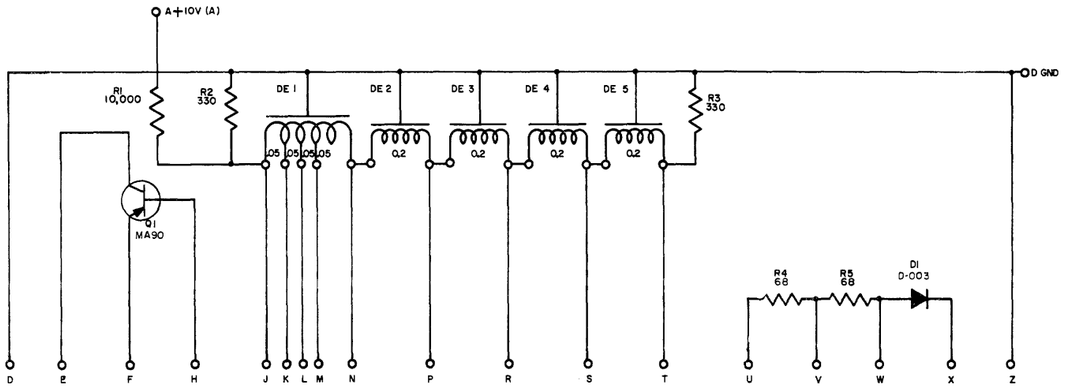
NOTE:
REFER TO MAD-B-1020 FOR MECHANICAL ASSEMBLY AND DETAILS.

Memory Diode Unit RS-1020

Binary-to-Octal Decoder RS-1151
Delay Line RS-1310



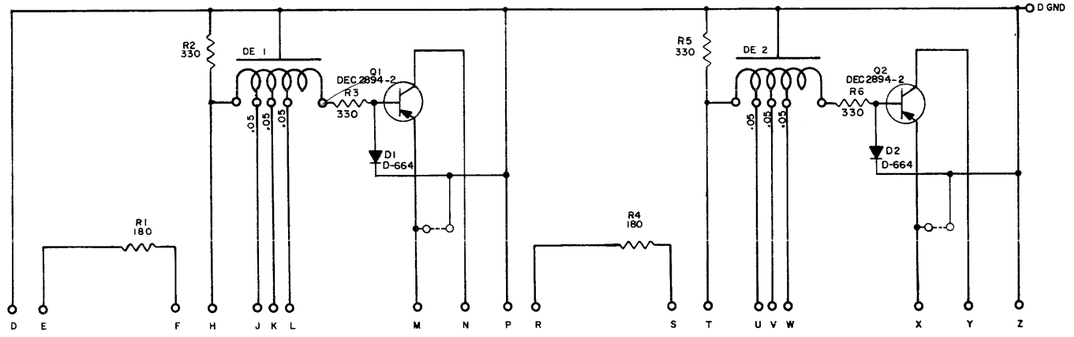
Binary-to-Octal Decoder RS-1151



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/2W; 10%
DE1= TECHNITROL 0.2 μ sec DELAY LINE 330 OHMS
TAPPED AT 0.05 μ sec. INTERVAL
DE2= DE5 TECHNTROL 0.2 μ sec. DELAY LINE

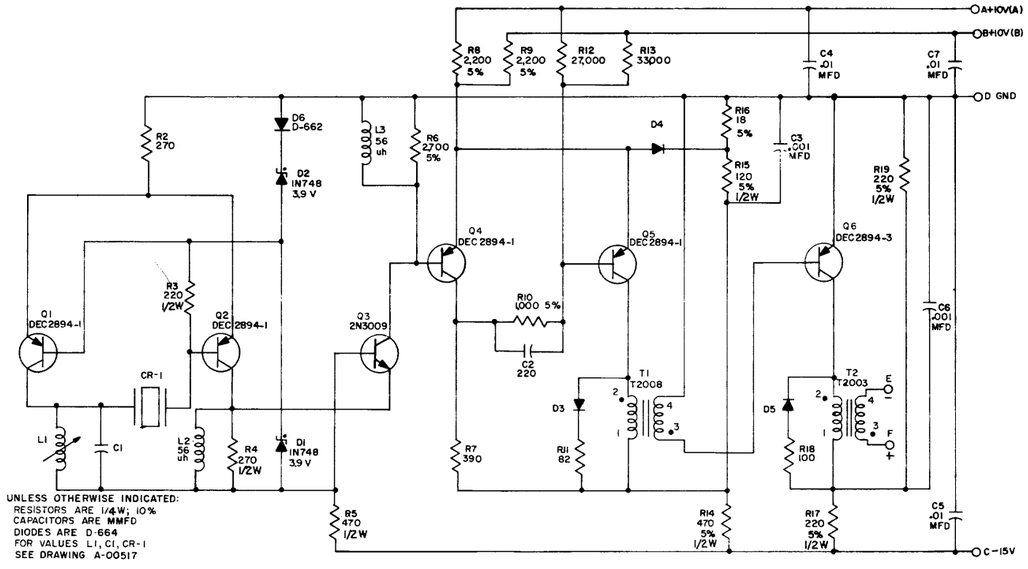
Delay Line RS-1310

Delay Line RS-1311
Crystal Clock RS-1406



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
DE 1 & DE2 ARE TECHNITROL DELAY LINE
0.2 μ sec 330 OHMS TAPPED AT 0.05 μ sec

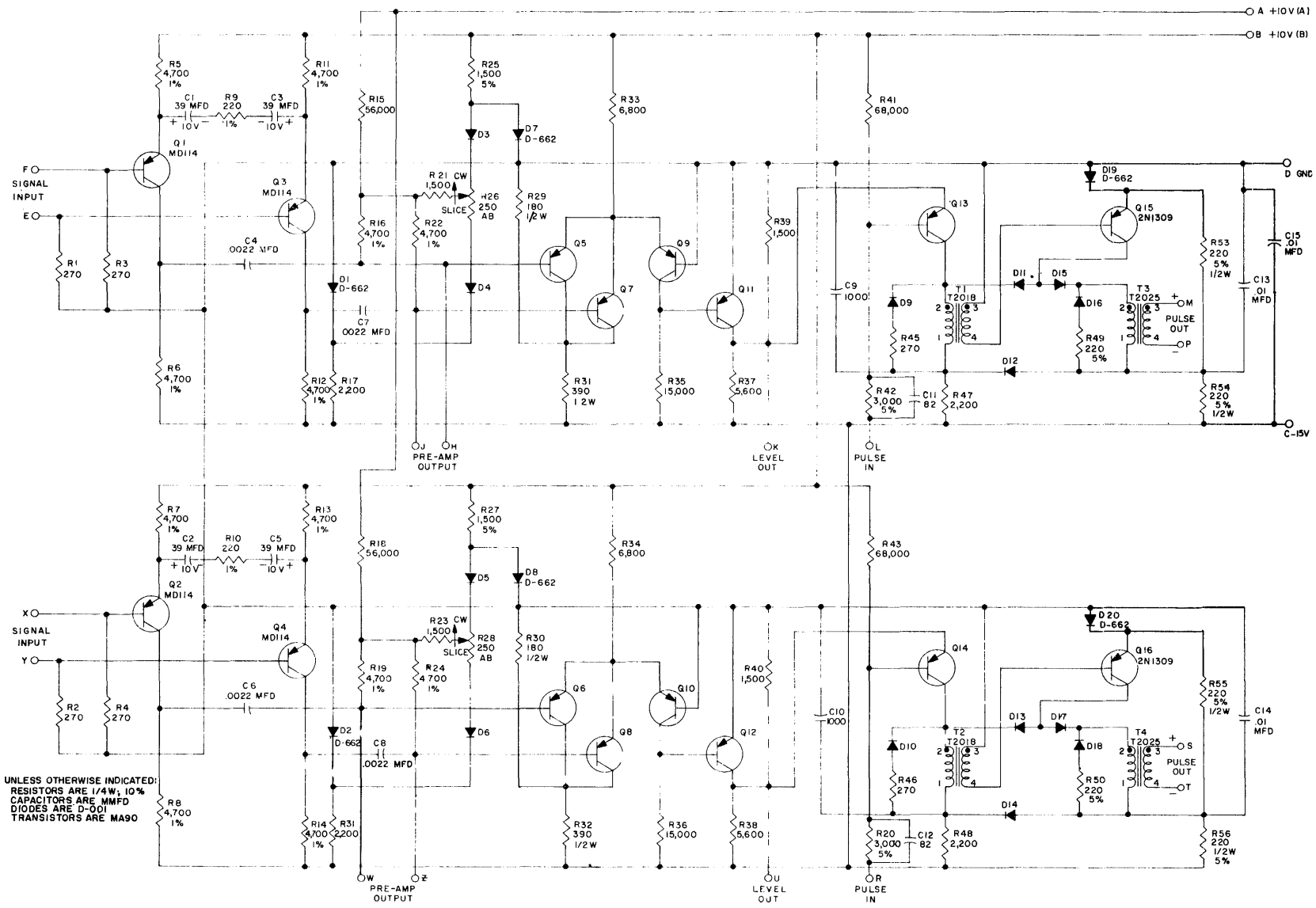
Delay Line RS-1311



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD
DIODES ARE D-664
FOR VALUES L1, C1, CR-1
SEE DRAWING A-00517

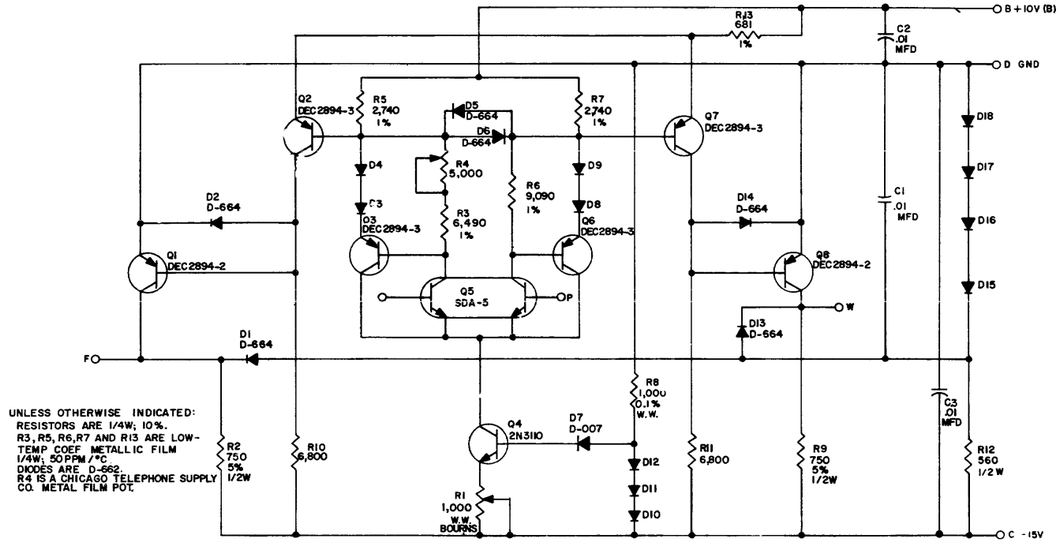
Crystal Clock RS-1406

Dual Sense Amplifier RS-1571



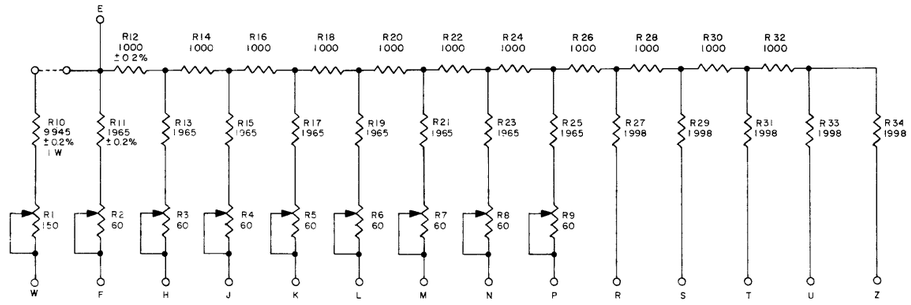
Dual Sense Amplifier RS-1571

Difference Amplifier RS-1572
12-Bit Digital-to-Analog Converter RS-1574



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%.
R3, R5, R6, R7 AND R13 ARE LOW-TEMP COEF METALLIC FILM 1/4W, 50PPM/°C.
DIODES ARE D-662.
R4 IS A CHICAGO TELEPHONE SUPPLY CO. METAL FILM POT.

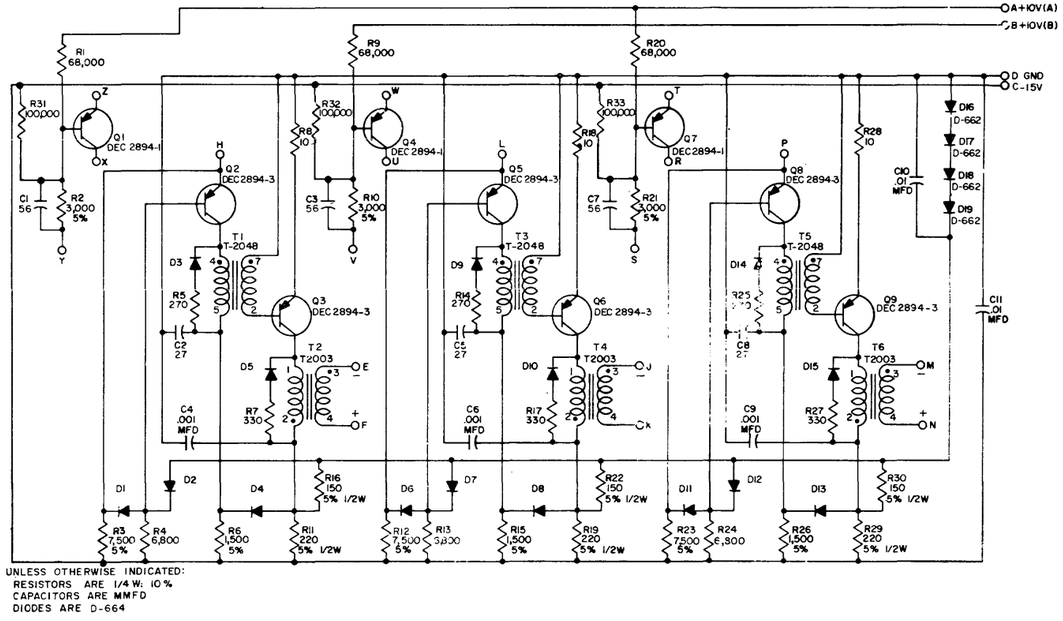
Difference Amplifier RS-1572



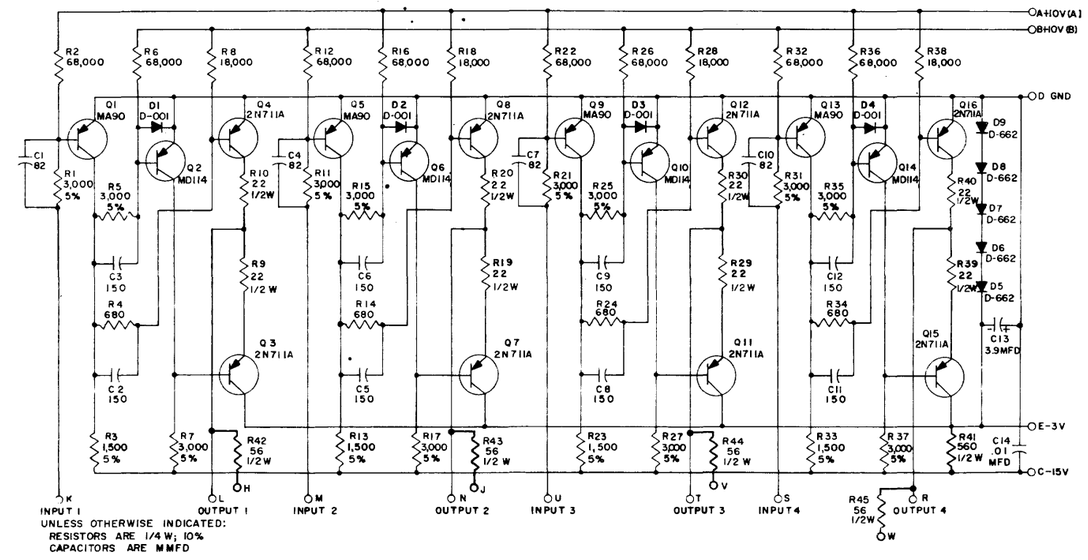
UNLESS OTHERWISE INDICATED
RESISTORS ARE ACI METAL FILM 0.5%, 1/2W
R10 - R.8 ±10 ppm/°C
R19 - R22 ±50 ppm/°C
R23 - R34 ±150 ppm/°C
POTENTIOMETERS: DAYSTROM TYPE 510, ±5%, ±50 ppm/°C
R1: RESOLUTION OF .55%, MAX. END RESISTANCE OF 2Ω
R2 - R9: RESOLUTION OF .6%, MAX. END RESISTANCE OF 0.5Ω

12-Bit Digital-to-Analog Converter RS-1574

Pulse Amplifier RS-1607
Bus Driver RS-1684

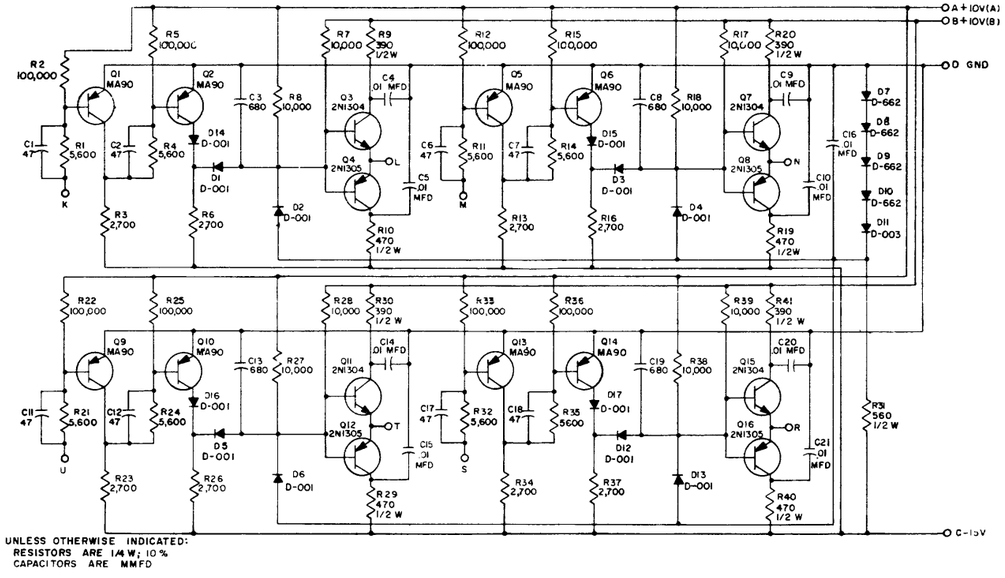


Pulse Amplifier RS-1607

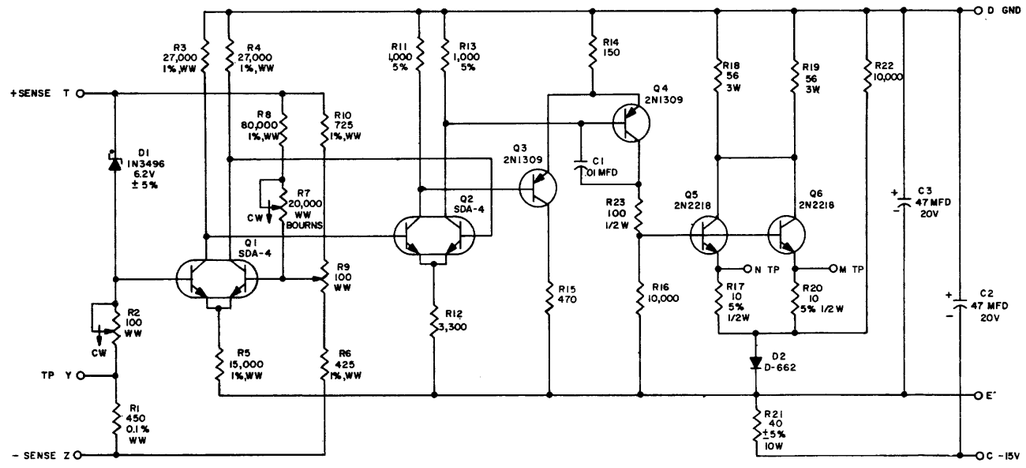


Bus Driver RS-1684

Bus Driver RS-1685
-10V Precision Power Supply RS-1704



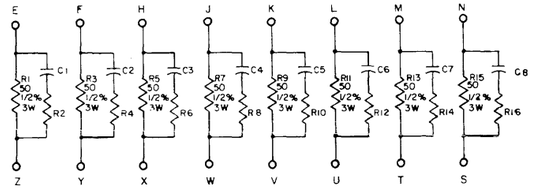
Bus Driver RS-1685



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10%
R10, R6 AND R1 ARE DAVEN 3 PPM TYPE 1195
R3, R4, R5 AND R8 ARE DAVEN 20 PPM TYPE 1283
R2, R9, ARE 50 PPM DAYSTRUM TRANSITRIM

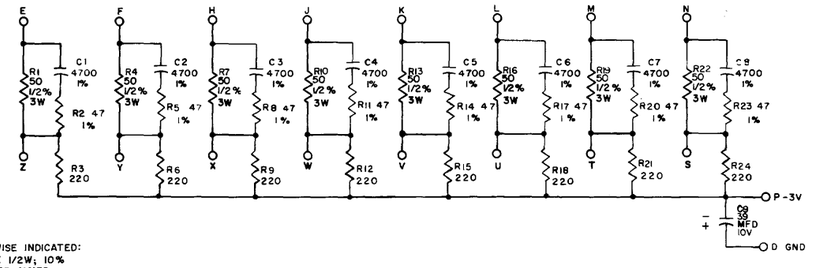
-10V Precision Power Supply RS-1704

Resistor Board RS-1976
Resistor Board RS-1978



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 47 OHMS 1%
CAPACITORS ARE 4700 MMFD 1%

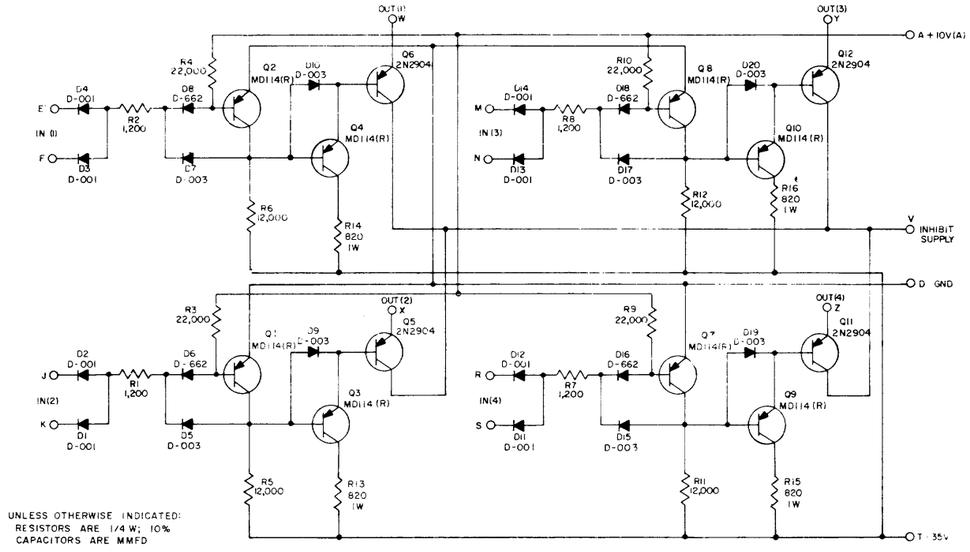
Resistor Board RS-1976



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/2W; 10%
CAPACITORS ARE MMFD

Resistor Board RS-1978

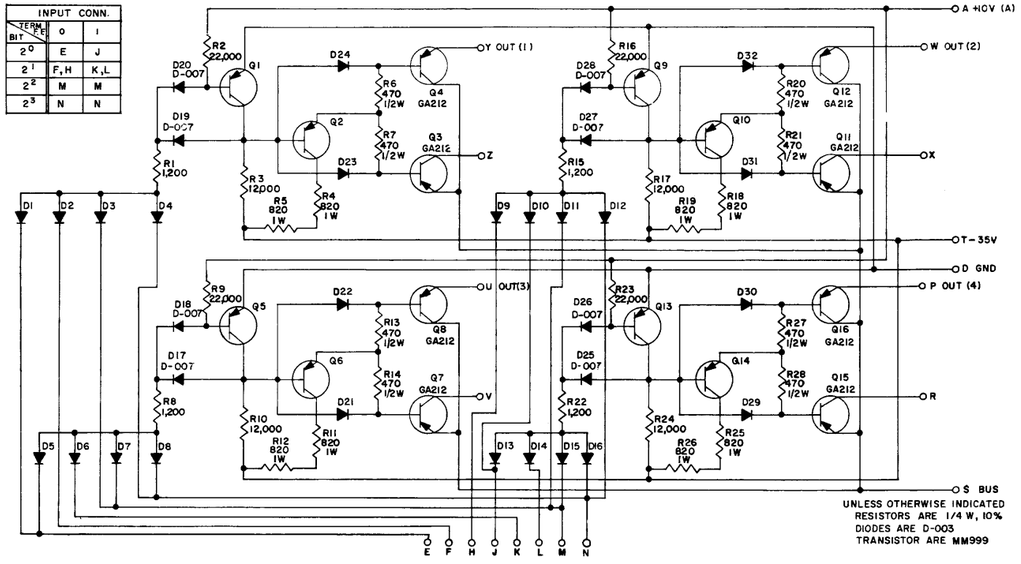
Inhibit Driver RS-1982
Read-Write Switch RS-1987



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W; 10%
CAPACITORS ARE MMFD

Inhibit Driver RS-1982

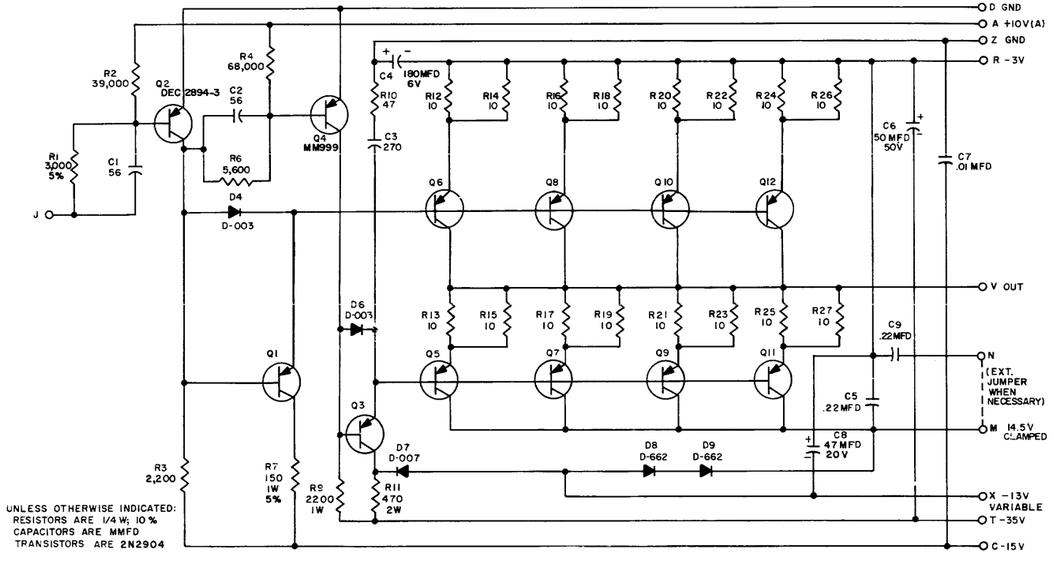
INPUT CONN.		
TERM TYPE / BIT	0	1
2^0	E	J
2^1	F, H	K, L
2^2	M	M
2^3	N	N



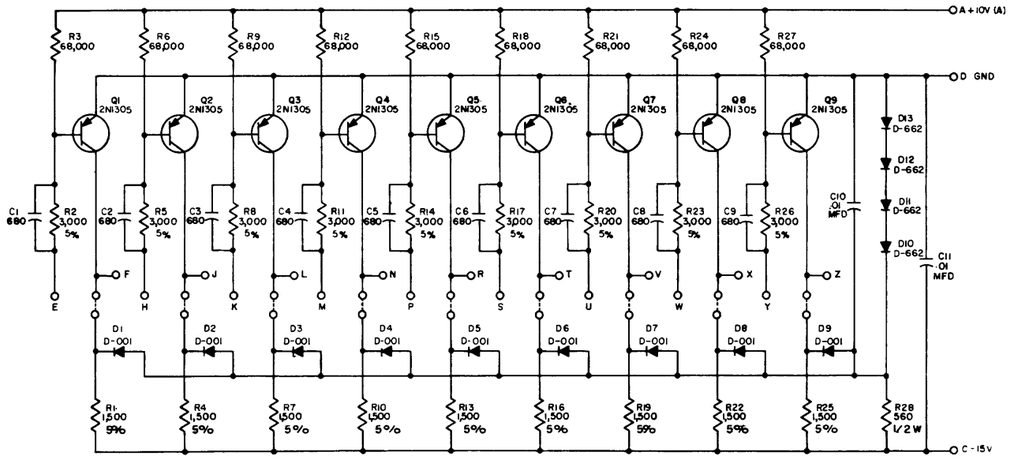
UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
DIODES ARE D-003
TRANSISTOR ARE MM999

Read-Write Switch RS-1987

Memory Driver RS-1989
Inverter RS-4102



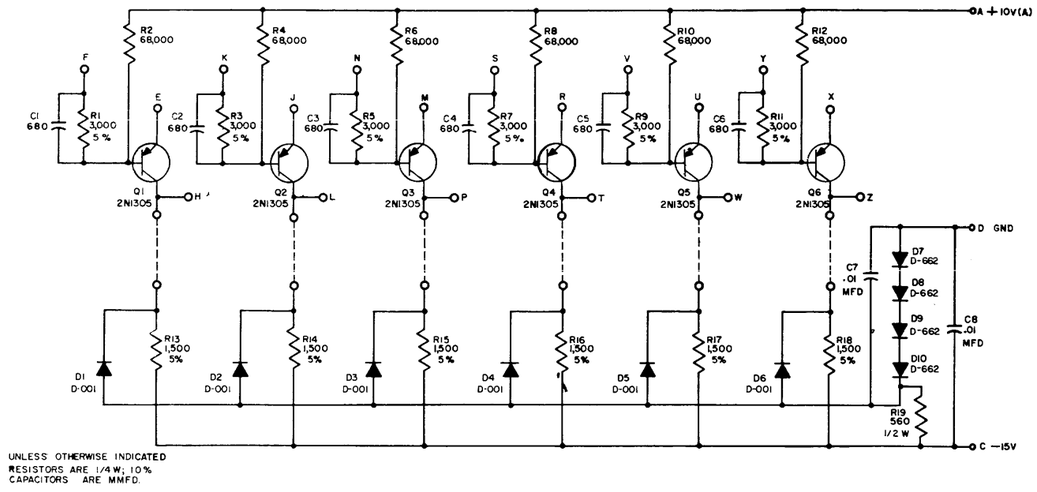
Memory Driver RS-1989



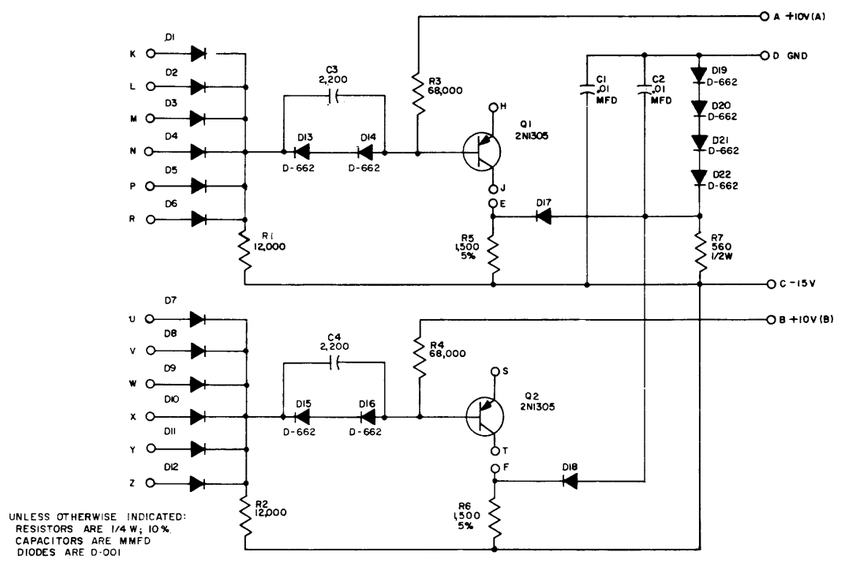
UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4W, 10%
CAPACITORS ARE MMFD

Inverter RS-4102

Inverter RS-4106
Diode RS-4111

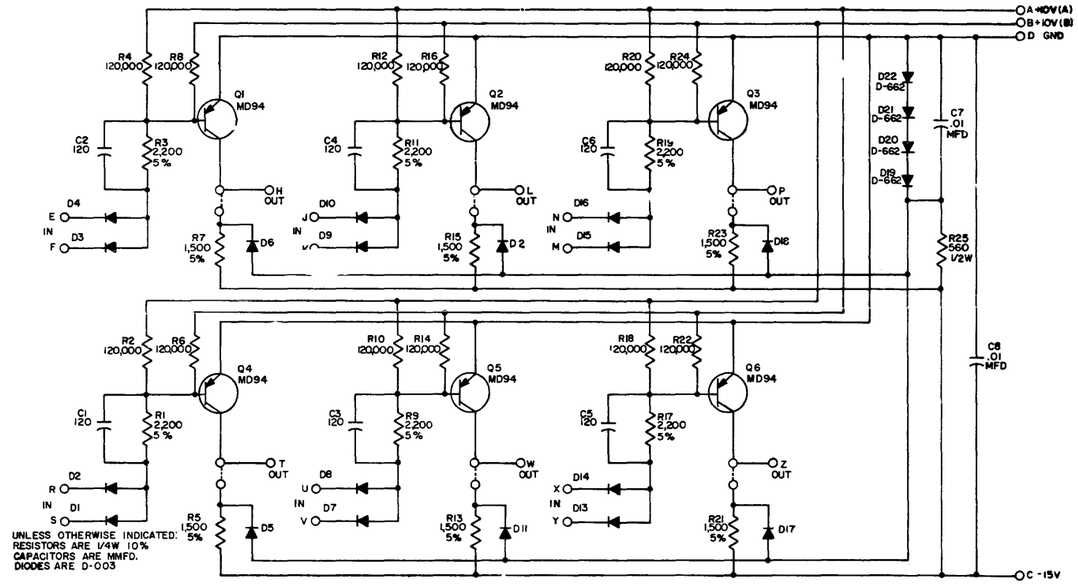


Inverter RS-4106

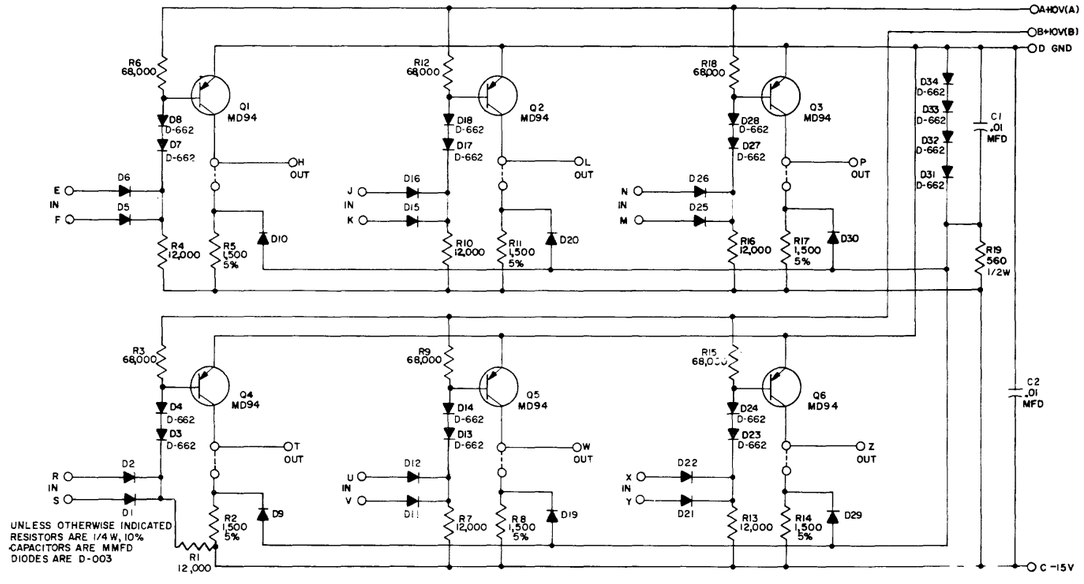


Diode RS-4111

Negative Diode NOR RS-4112
Diode RS-4113

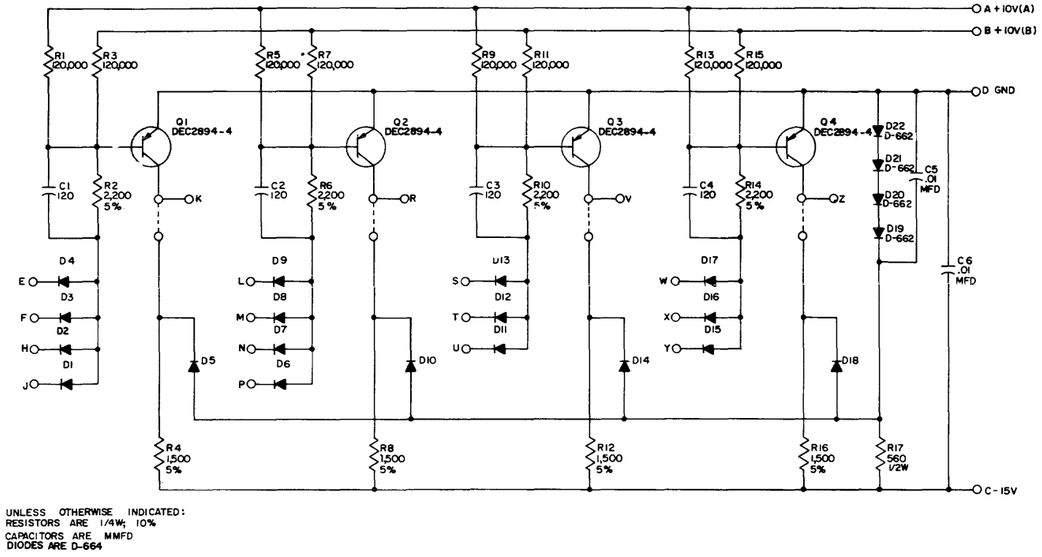


Negative Diode NOR RS-4112



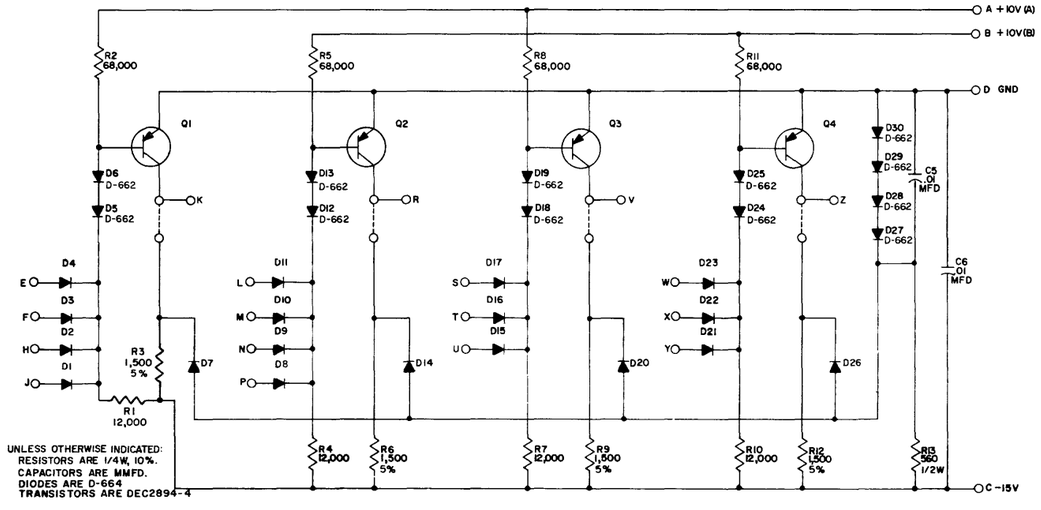
Diode RS-4113

Negative Diode NOR RS-4114
Positive Diode NOR RS-4115



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD
DIODES ARE D-664

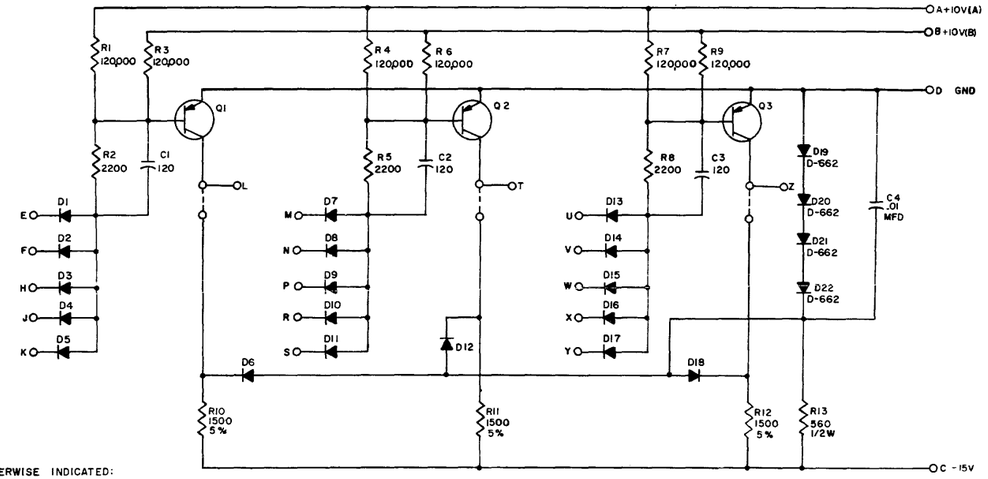
Negative Diode NOR RS-4114



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 10%.
CAPACITORS ARE MMFD.
DIODES ARE D-664
TRANSISTORS ARE DEC2894-4

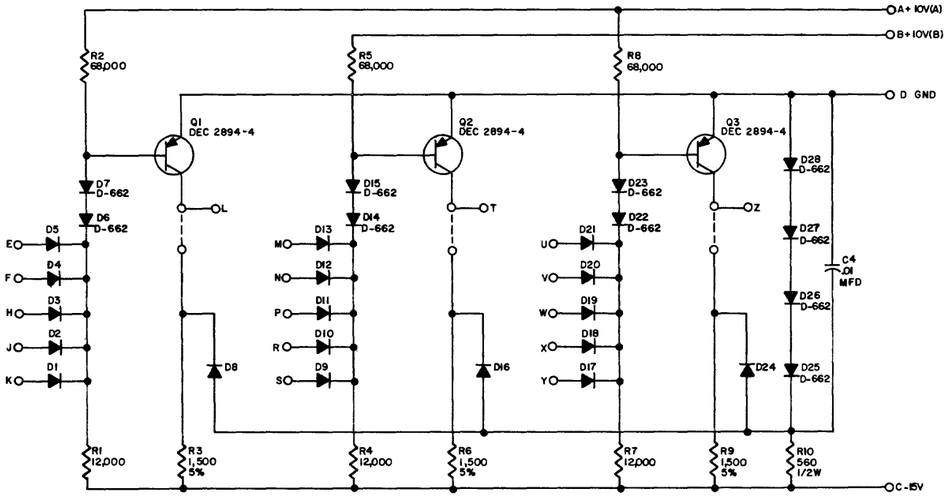
Positive Diode NOR RS-4115

Diode RS-4116
Positive Diode NOR RS-4117



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD
DIODES ARE D-664
TRANSISTORS ARE 2894-4

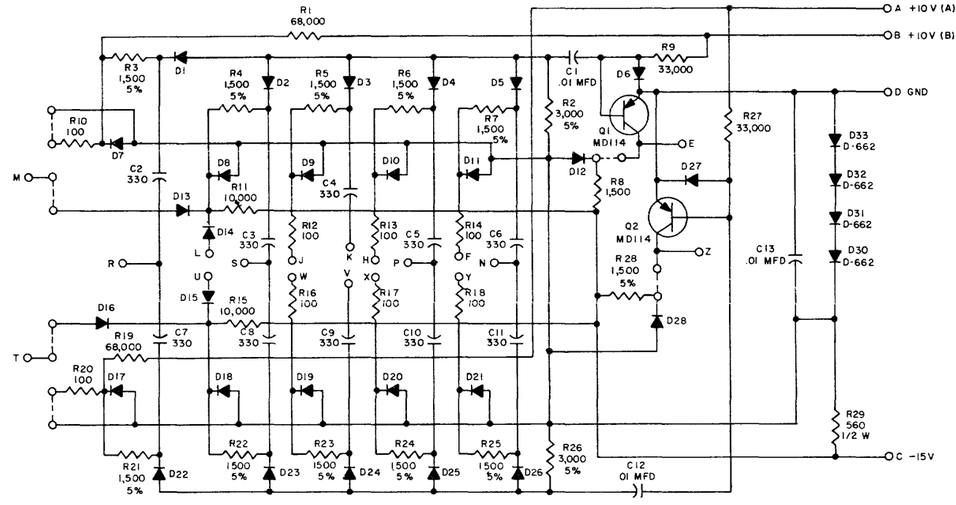
Diode RS-4116



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
DIODES ARE D-664

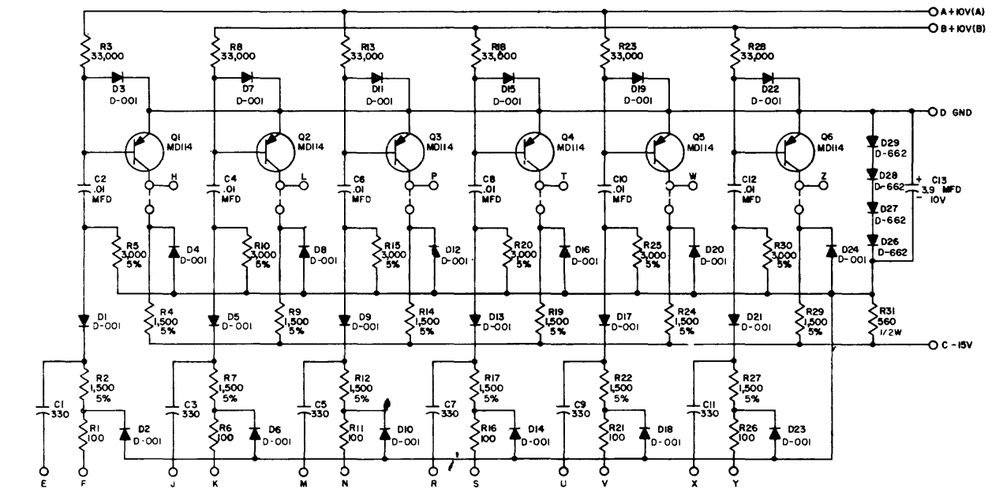
Positive Diode NOR RS-4117

Negative Capacitor Diode Gate RS-4123
Pulse Inverter RS-4127



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD
DIODES ARE D-001

Negative Capacitor Diode Gate RS-4123

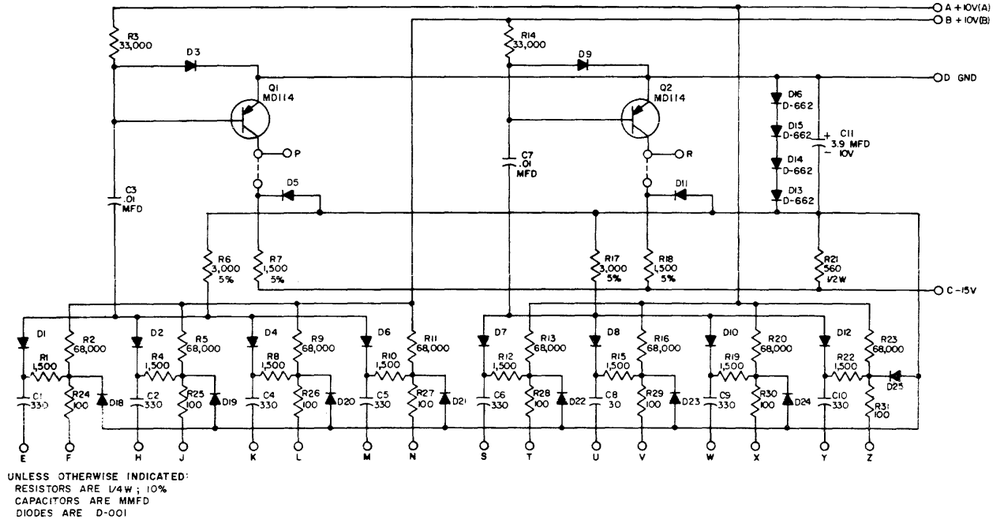


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 10%
CAPACITORS ARE MMFD

Pulse Inverter RS-4127

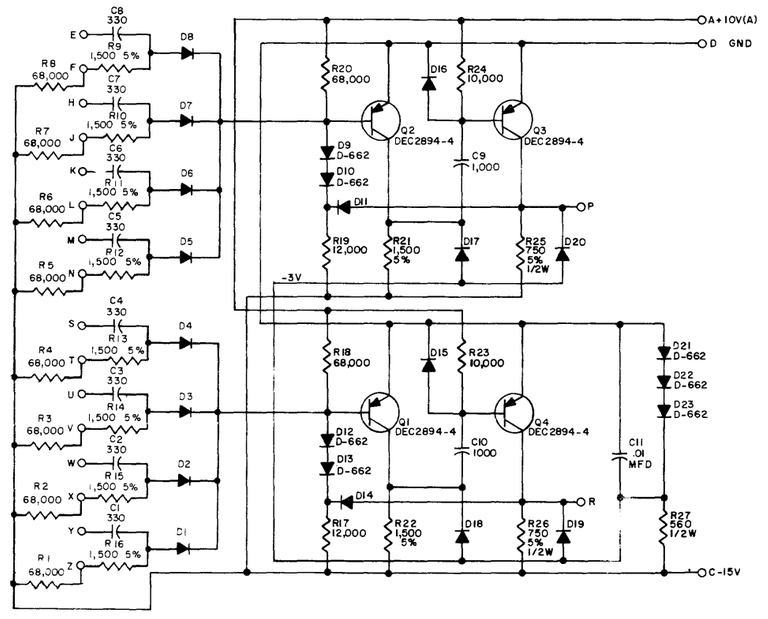
Pulse Inverter RS-4129
Positive Capacitor-Diode Gate RS-4130

10-43



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W ; 10%
CAPACITORS ARE MMFD
DIODES ARE D-001

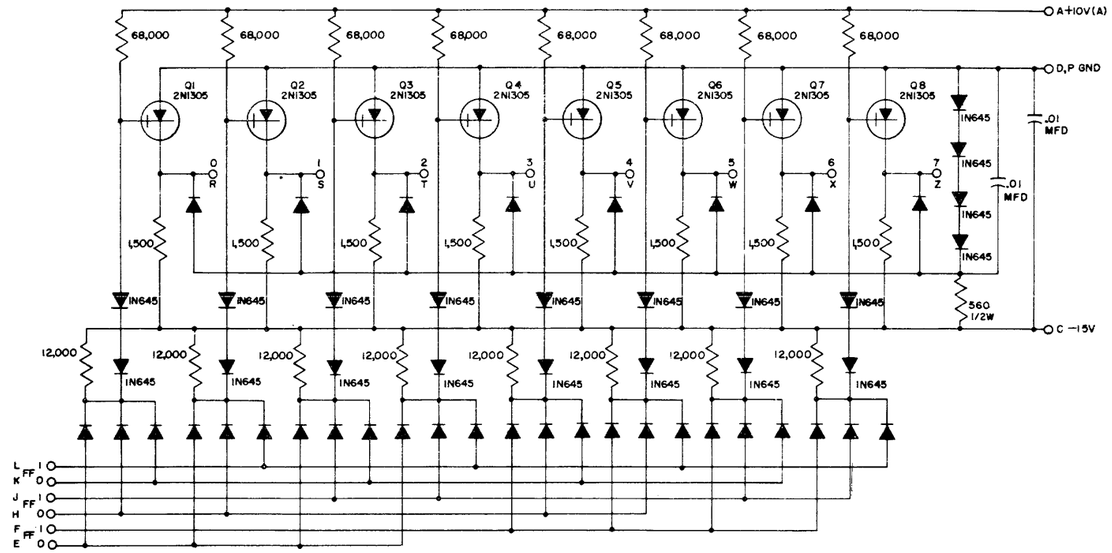
Pulse Inverter RS-4129



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W; 10%
CAPACITORS ARE MMFD
DIODES ARE D-664

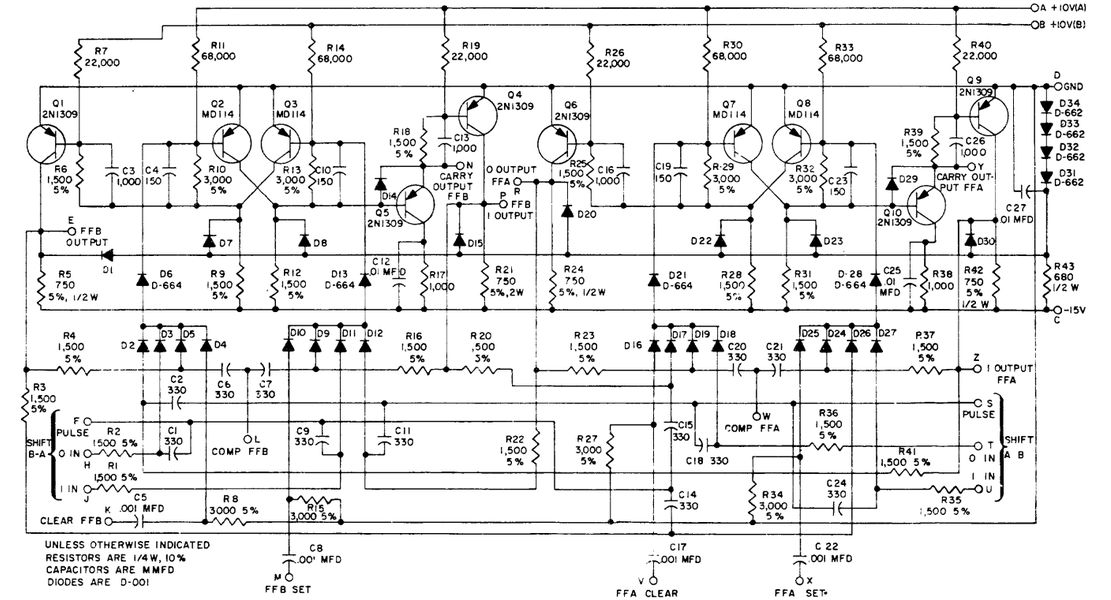
Positive Capacitor-Diode Gate RS-4130

Binary-to-Octal Decoder RS-4151
Dual Flip-Flop RS-4205



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10%
DIODES ARE IN276

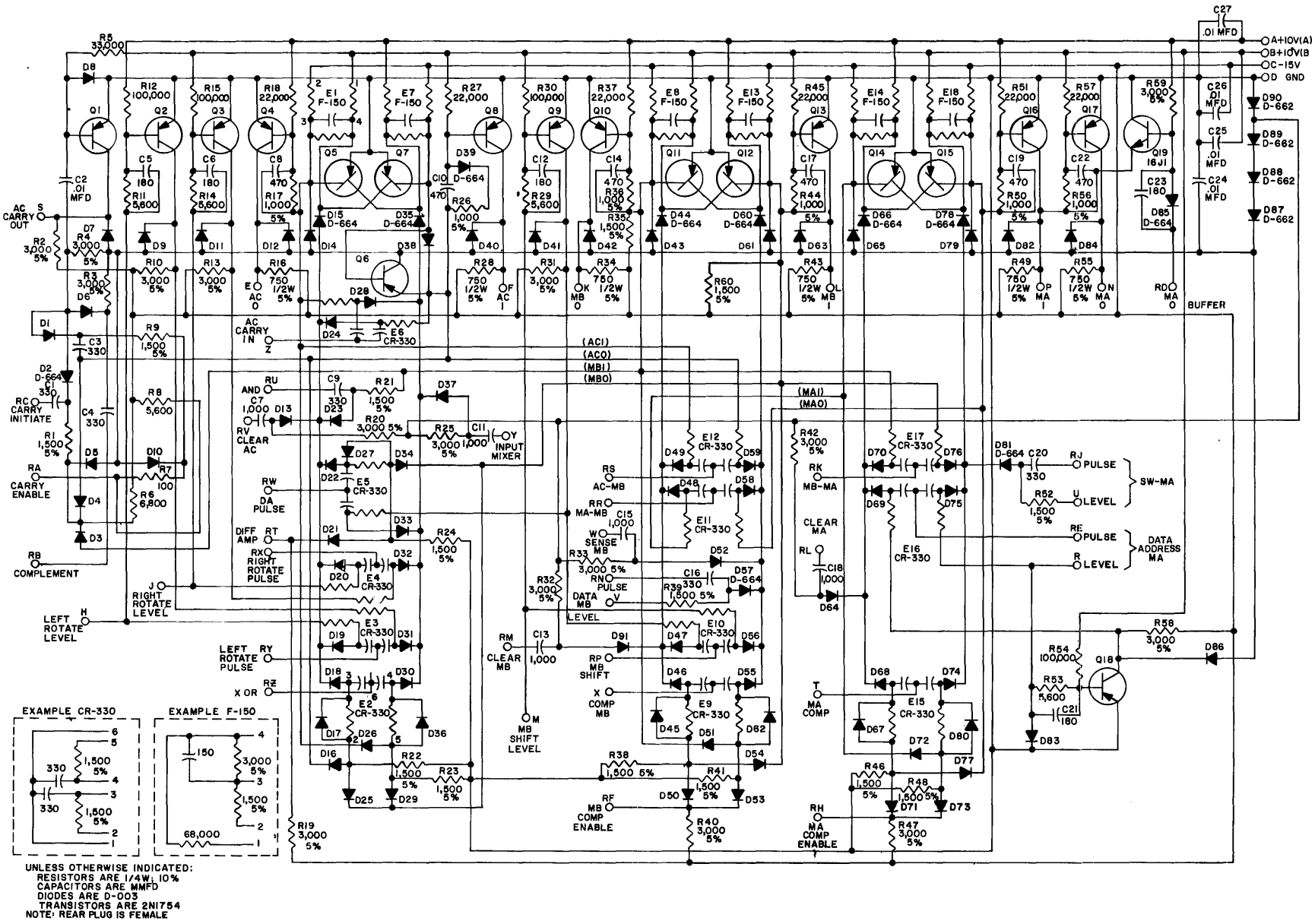
Binary-to-Octal Decoder RS-4151



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4W, 10%
CAPACITORS ARE MMFD
DIODES ARE D-001

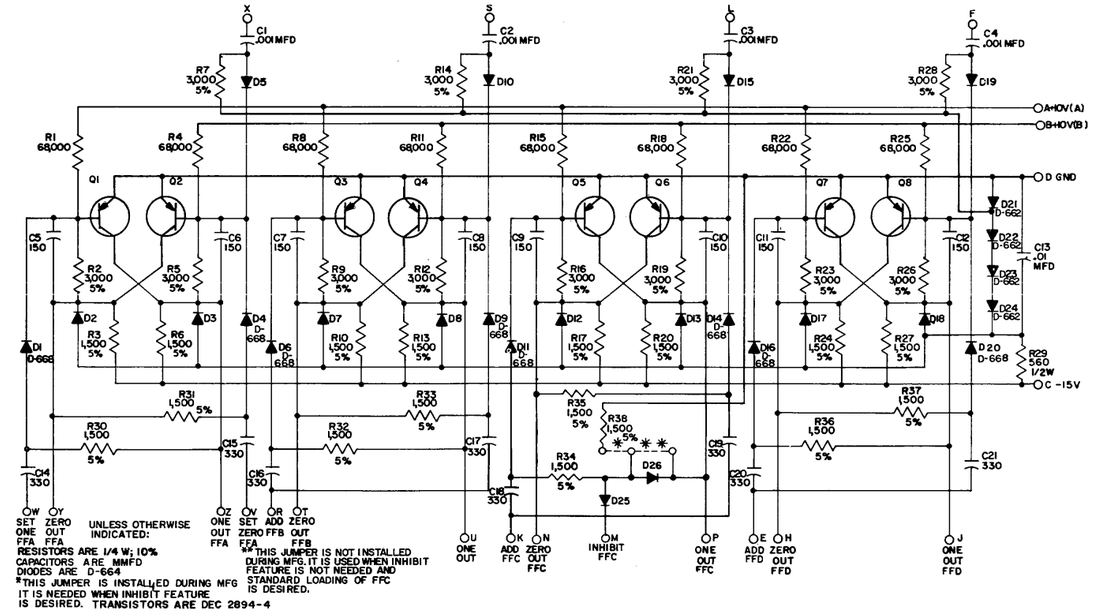
Dual Flip-Flop RS-4205

Triple Flip-Flop RS-4206

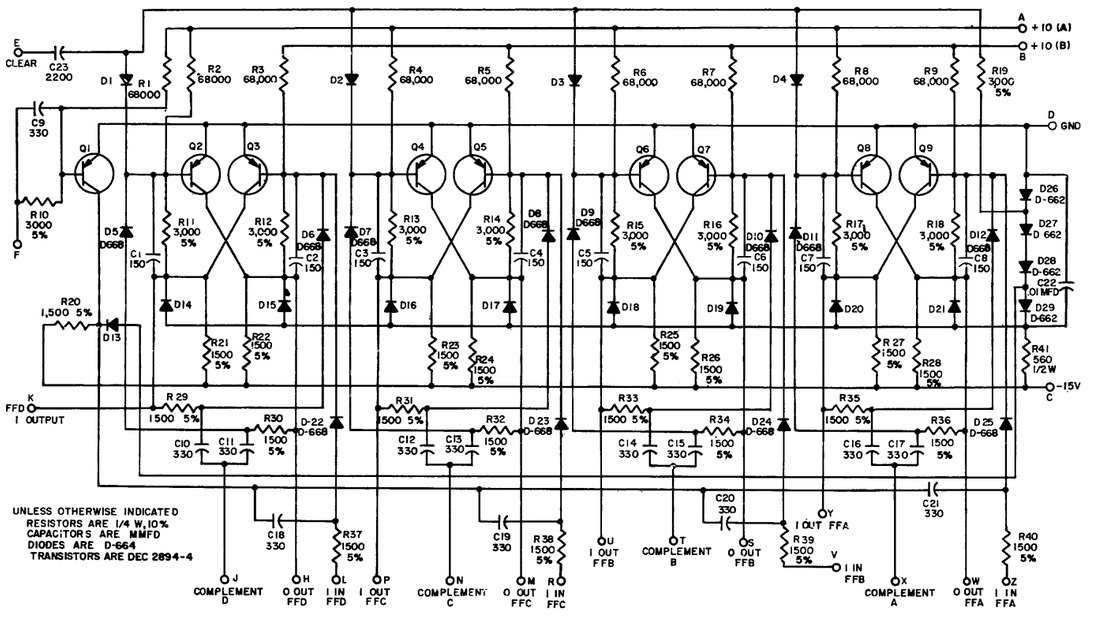


Triple Flip-Flop RS-4206

4-Bit Counter RS-4215
4-Bit Counter RS-4217

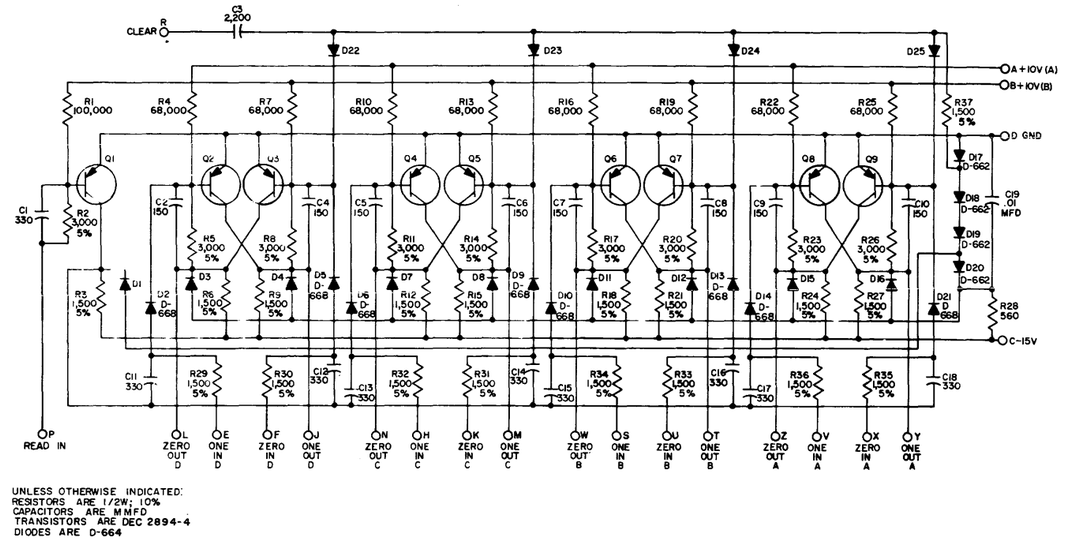


4-Bit Counter RS-4215



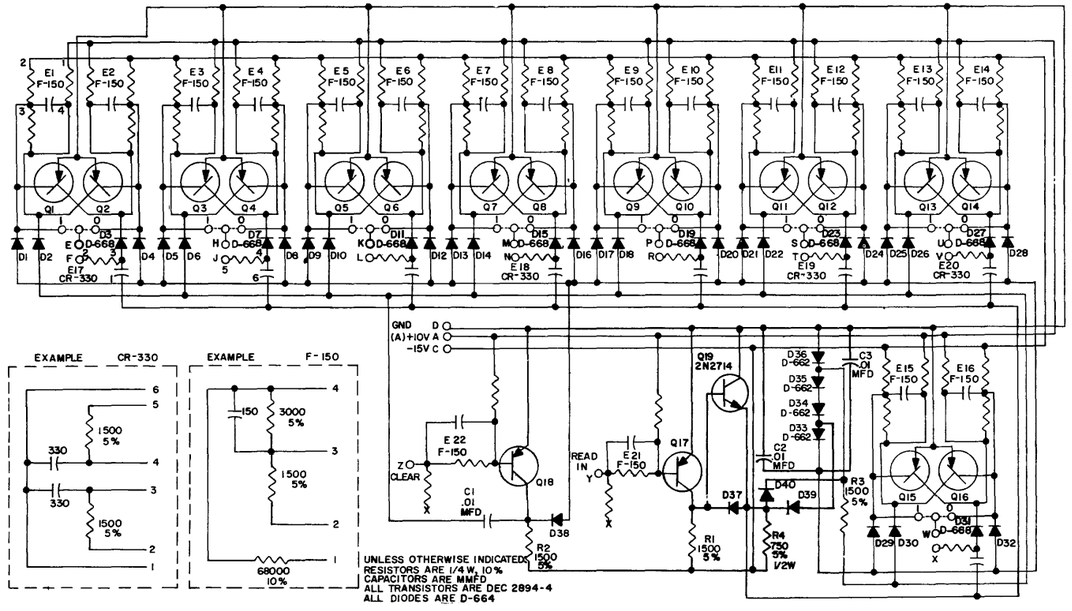
4-Bit Counter RS-4217

Quadruple Flip-Flop RS-4218
8-Bit Buffer Register RS-4220



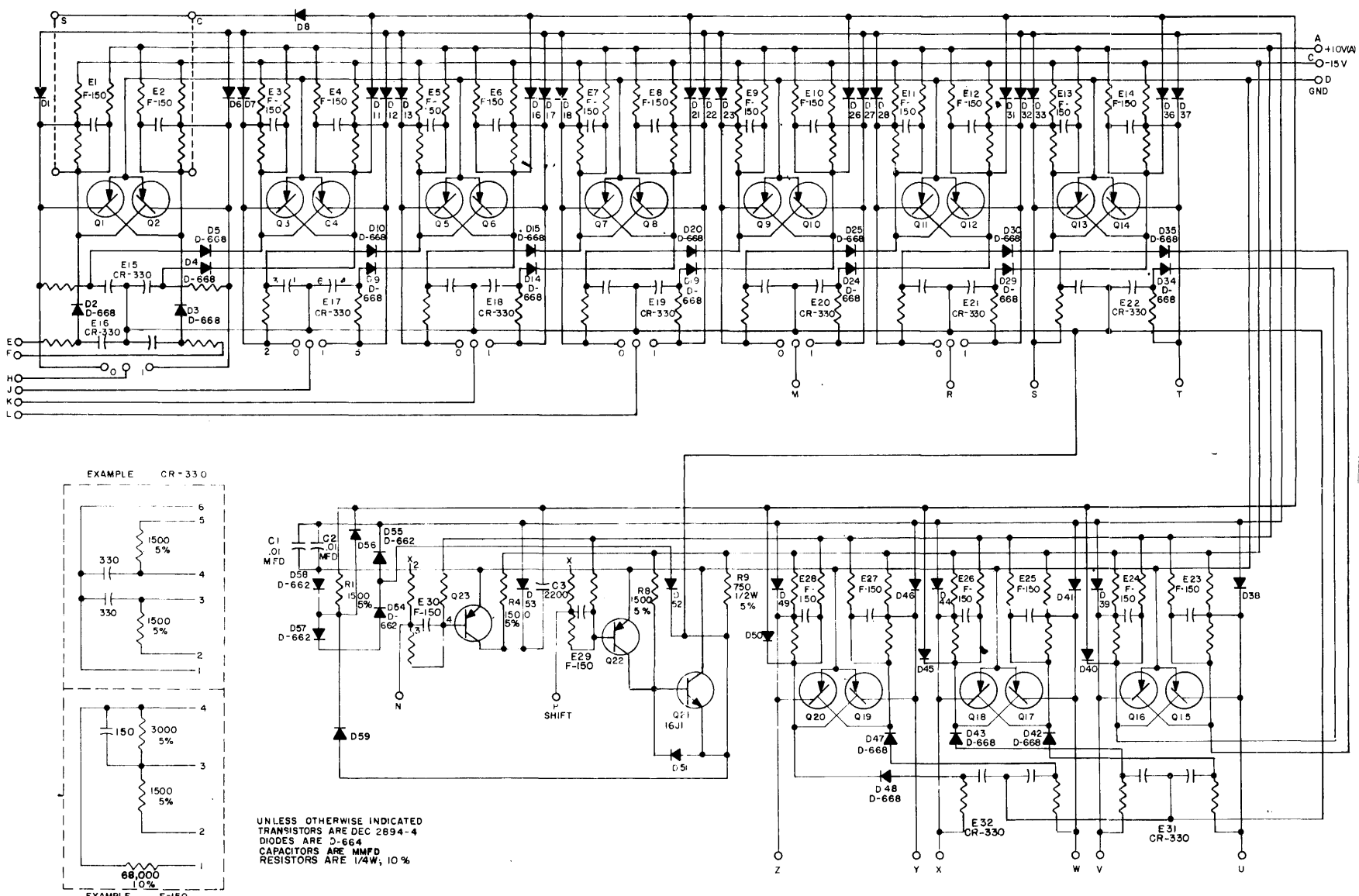
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/2W; 10%
CAPACITORS ARE MMFD
TRANSISTORS ARE DEC 2894-4
DIODES ARE D-664

Quadruple Flip-Flop RS-4218



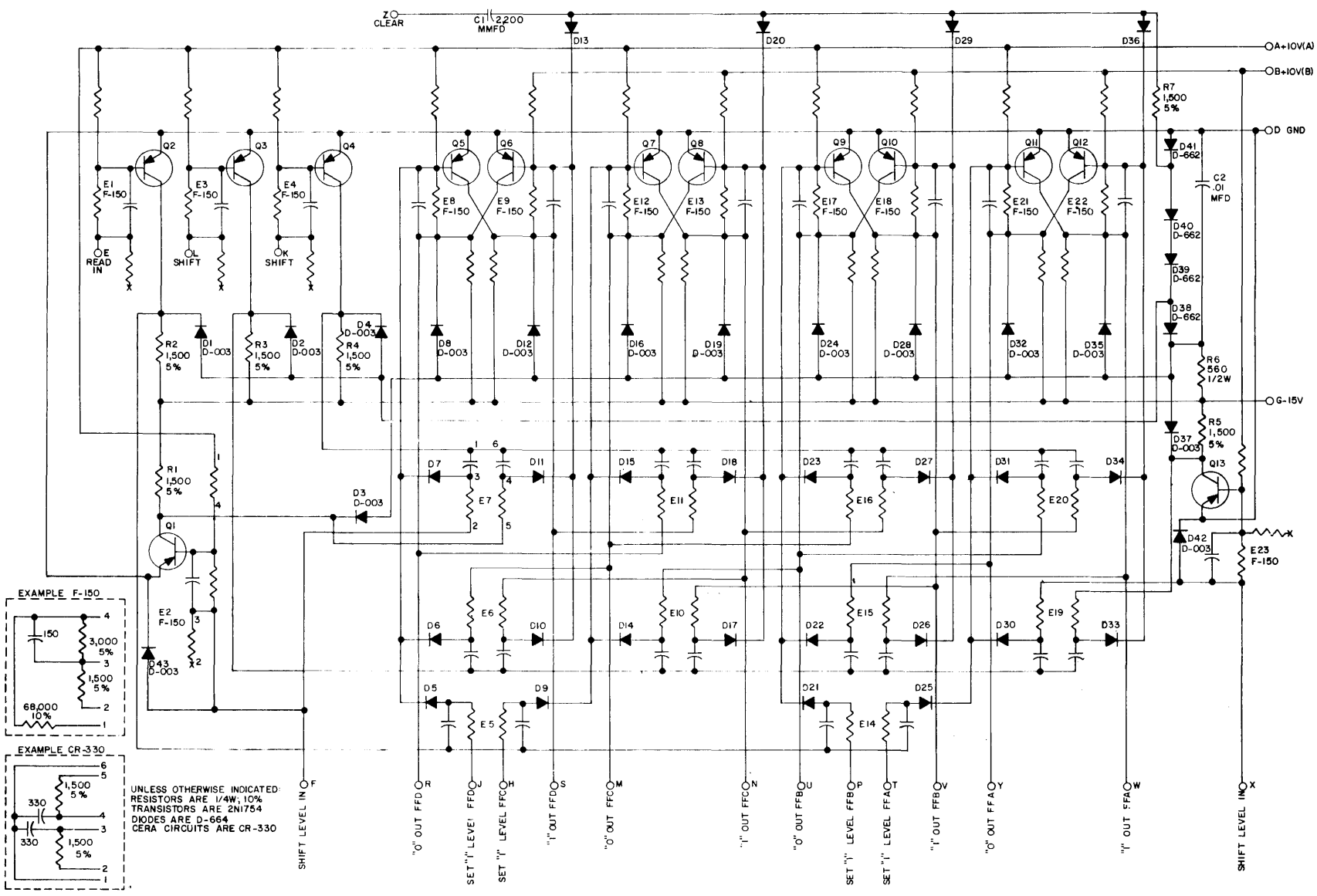
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD
ALL TRANSISTORS ARE DEC 2894-4
ALL DIODES ARE D-664

8-Bit Buffer Register RS-4220



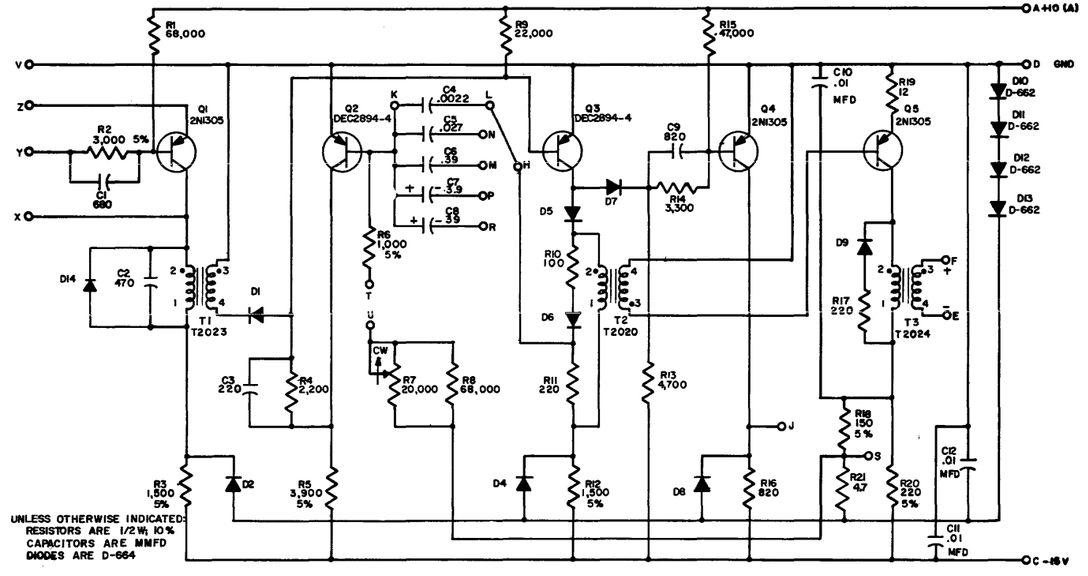
UNLESS OTHERWISE INDICATED
TRANSISTORS ARE DEC 2894-4
DIODES ARE D-664
CAPACITORS ARE MMFD
RESISTORS ARE 1/4W; 10 %

8-Bit BCD or Binary Counter RS-4225

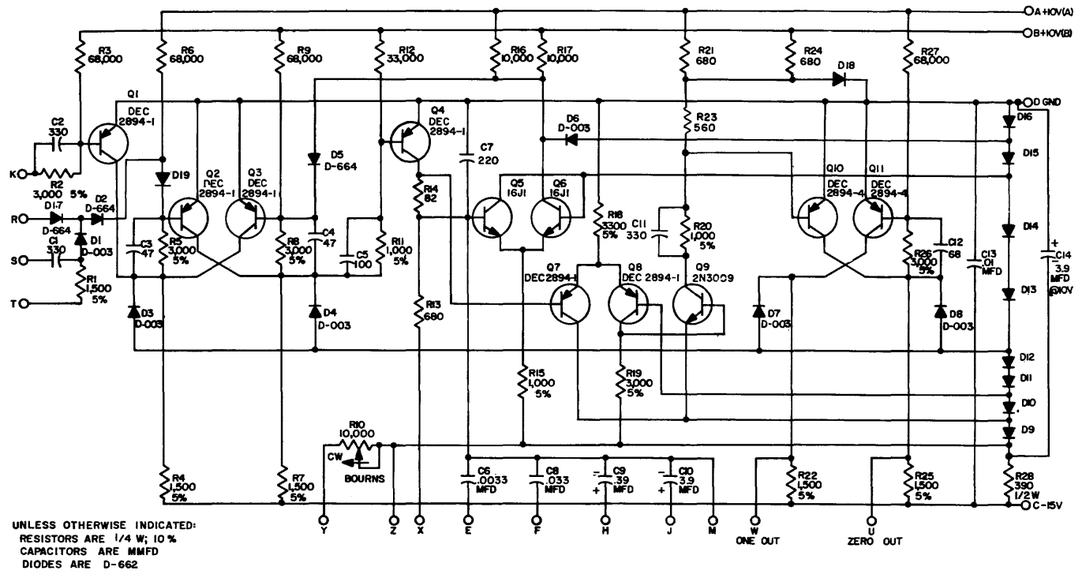


Quadruple Flip-Flop RS-4231

Delay (One Shot) RS-4301
Integrating Single Shot RS-4303

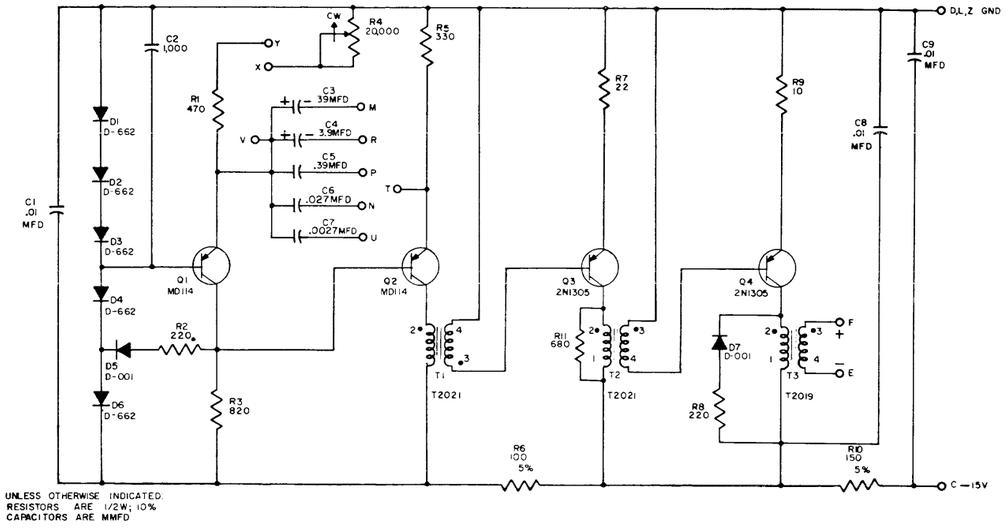


Delay (One Shot) RS-4301

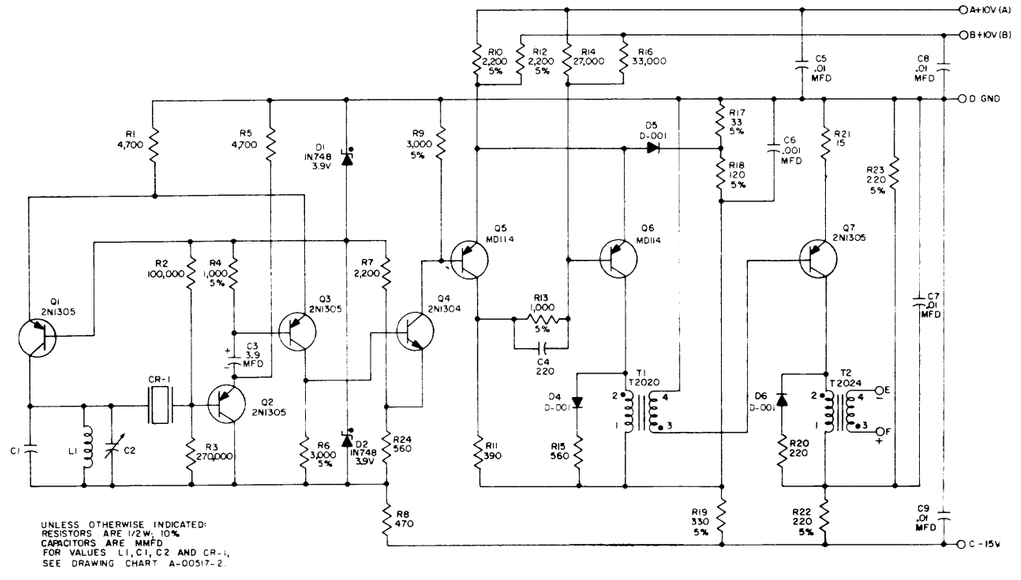


Integrating Single Shot RS-4303

Variable Clock RS-4401
Crystal Clock RS-4407



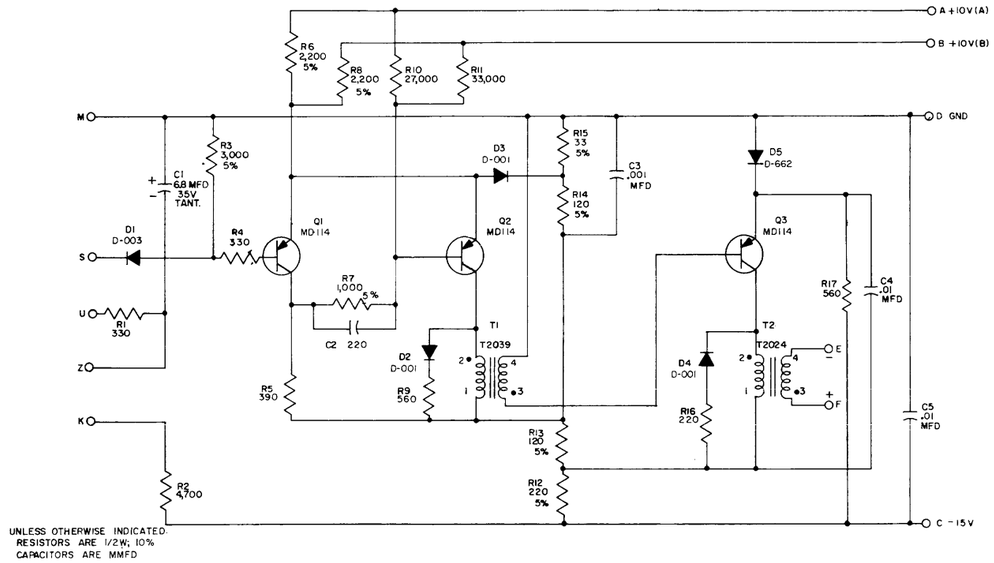
Variable Clock RS-4401



Crystal Clock RS-4407

Pulse Generator RS-4410

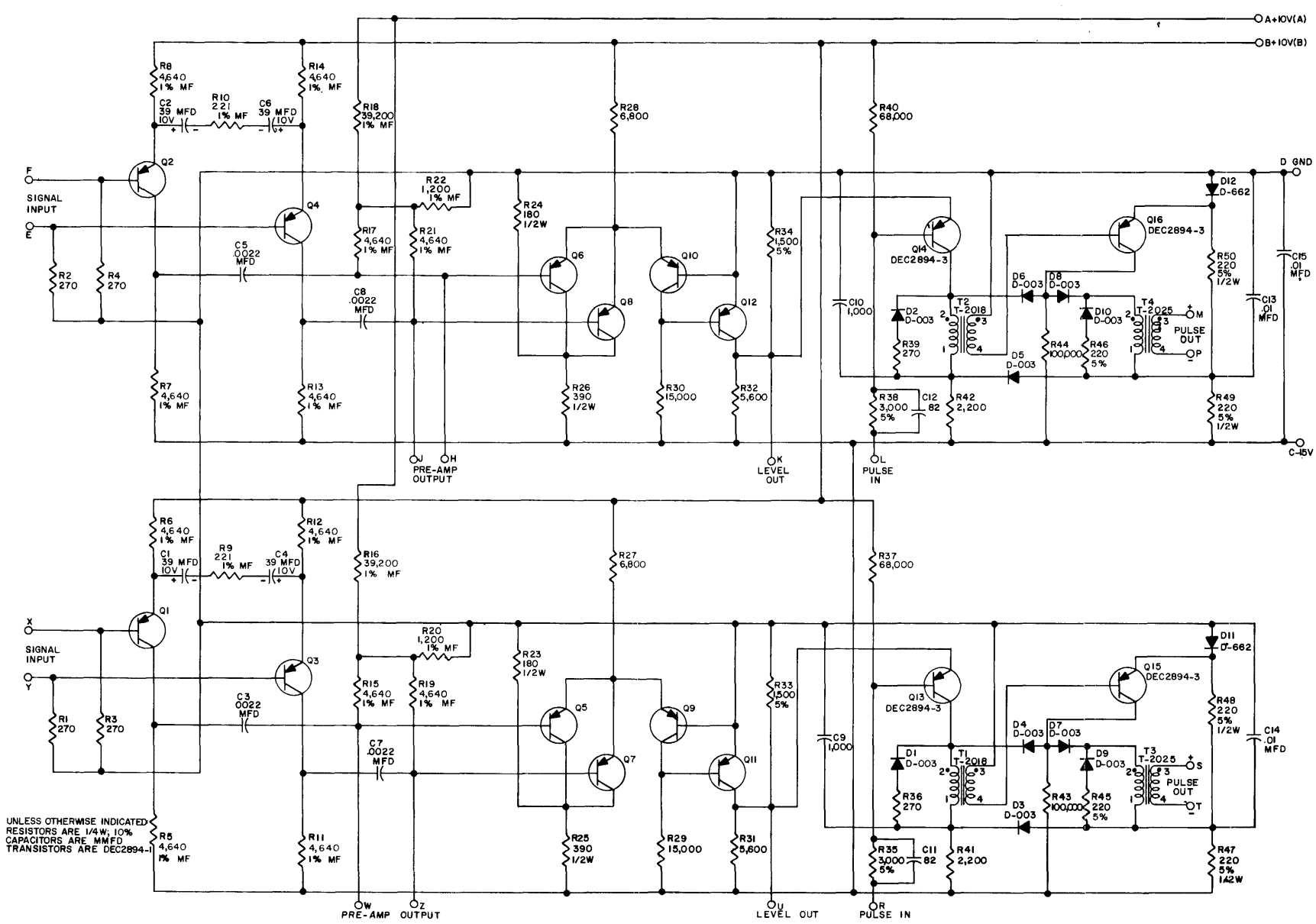
10-61



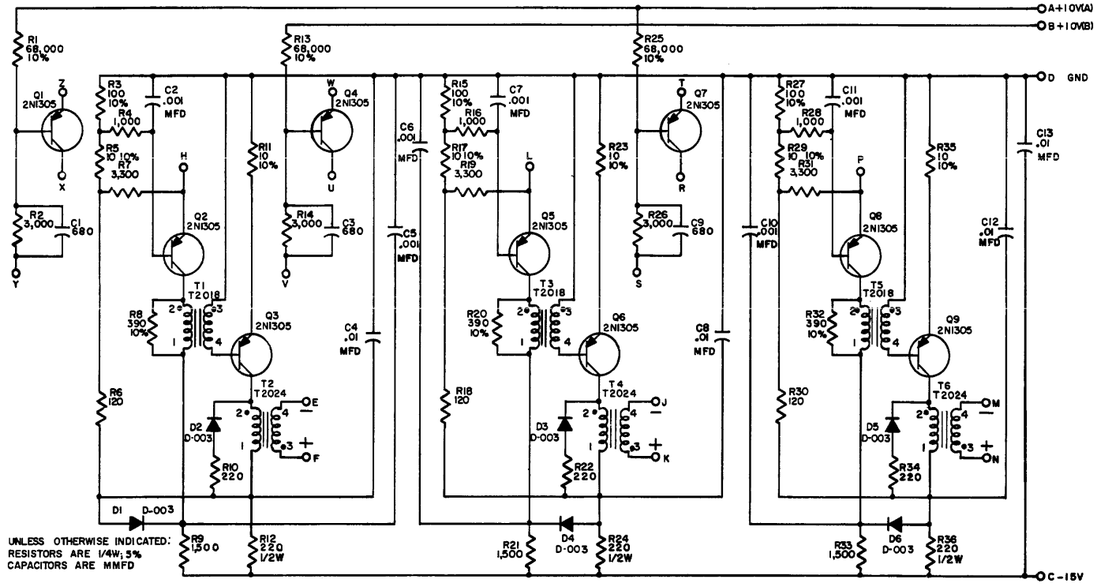
Pulse Generator RS-4410

Dual Sense Amplifier RS-4554

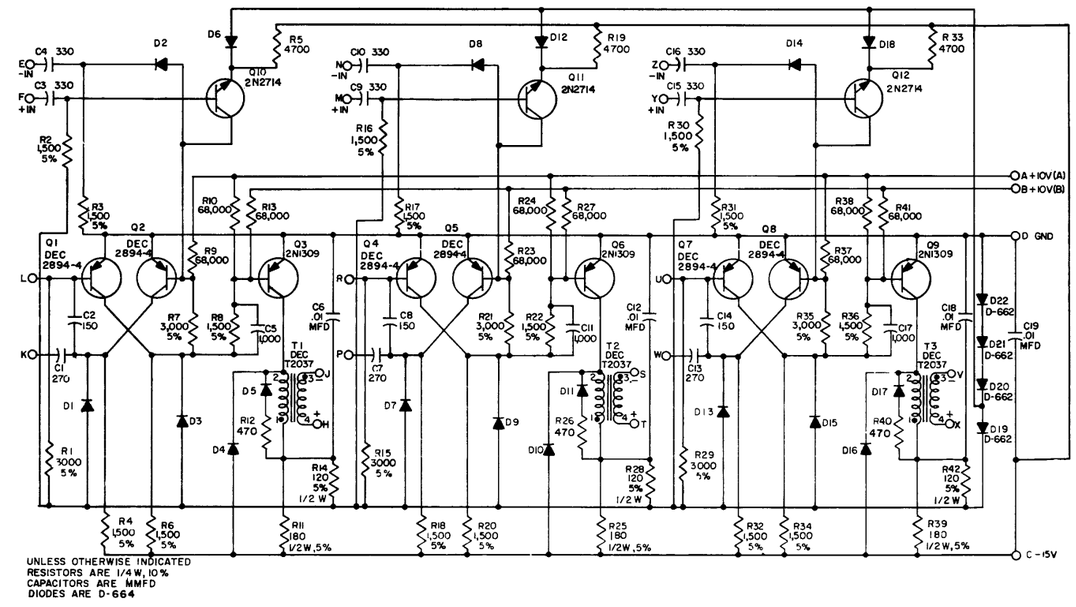
10-63



Dual Sense Amplifier RS-4554

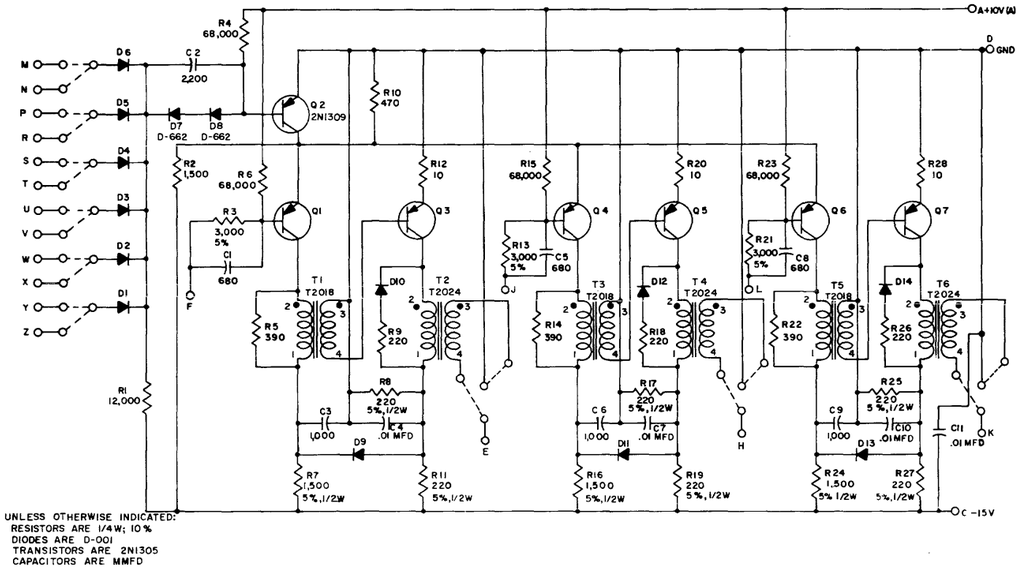


Pulse Amplifier RS-4603

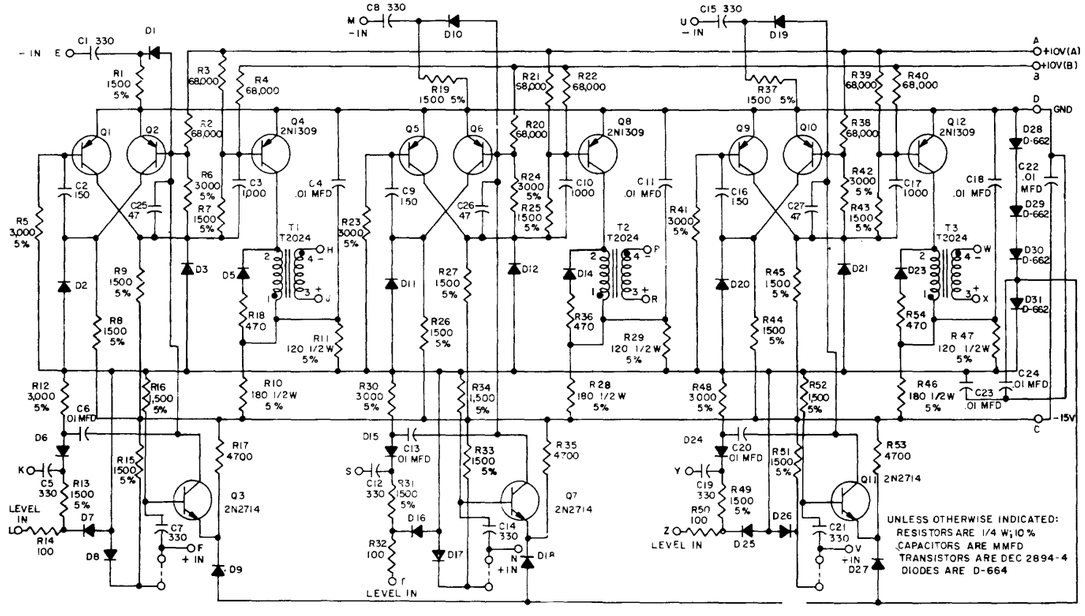


Pulse Amplifier RS-4604

Pulse Amplifier RS-4605
Pulse Amplifier RS-4606



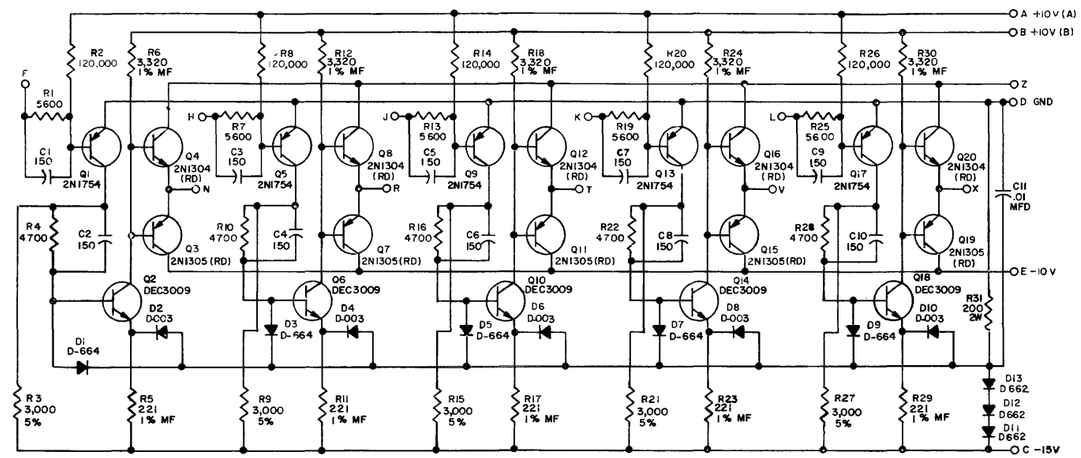
Pulse Amplifier RS-4605



Pulse Amplifier RS-4606

Level Amplifier RS-4678

10-69

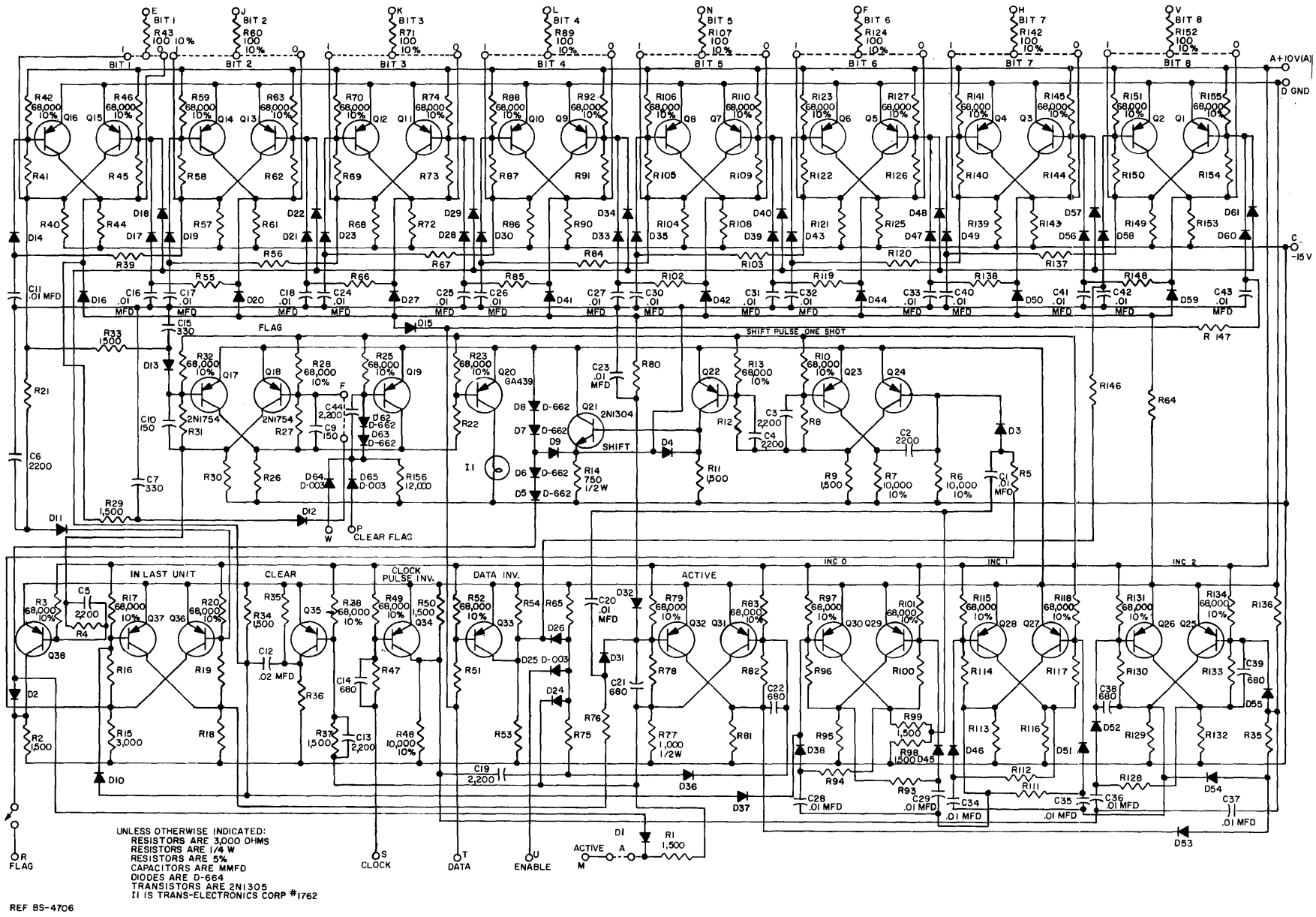


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W; 10%
TRANSISTORS MARKED WITH (RD) ARE SPECIALLY TESTED
CAPACITORS ARE MMFD

Level Amplifier RS-4678

Teletype Incoming Line Unit RS-4706

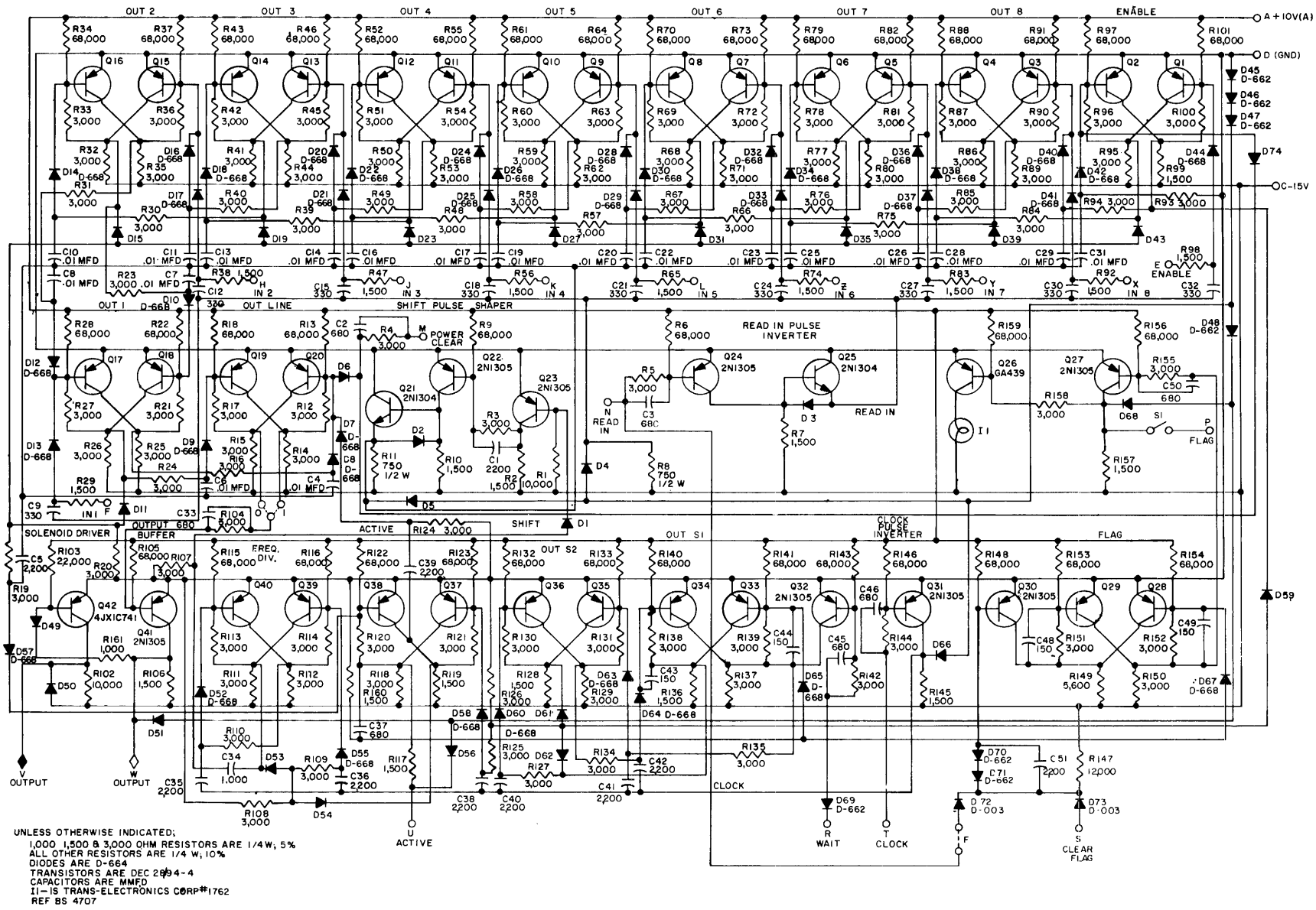
10-71



Teletype Incoming Line Unit RS-4706

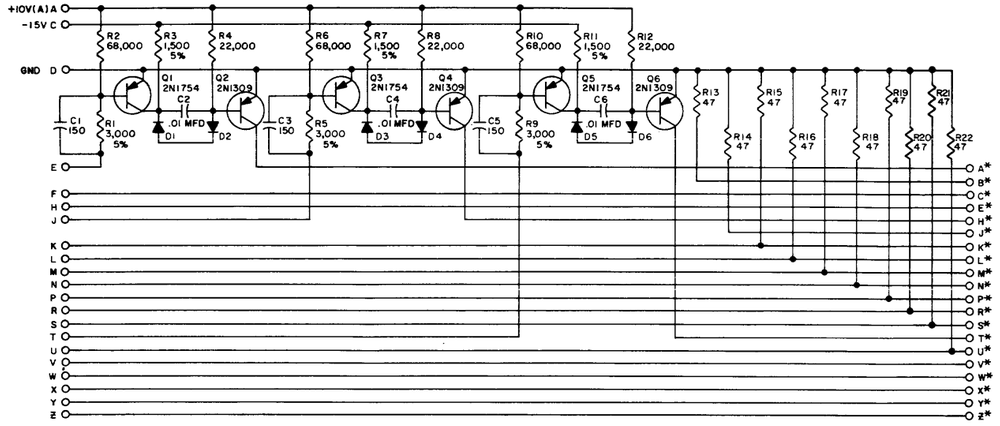
Teletype Transmitter RS-4707

10-73



Teletype Transmitter RS-4707

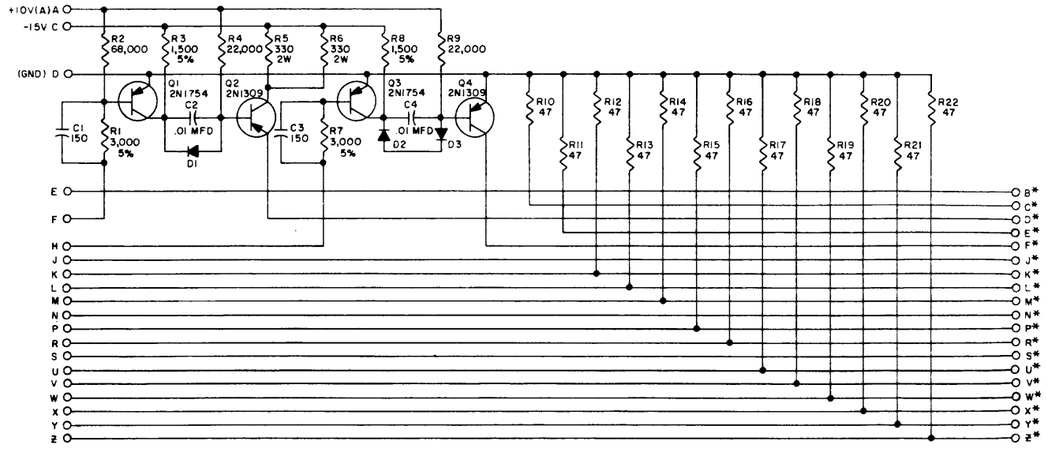
22-Pin Plug Adapter with Bus Driver RS-4801
22-Pin Plug Adapter with Bus Driver RS-4802



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD
DIODES ARE D-662

*INDICATES BACK PANEL PLUG
22 PIN AMPHENOL #143-022-04

22-Pin Plug Adapter with Bus Driver RS-4801

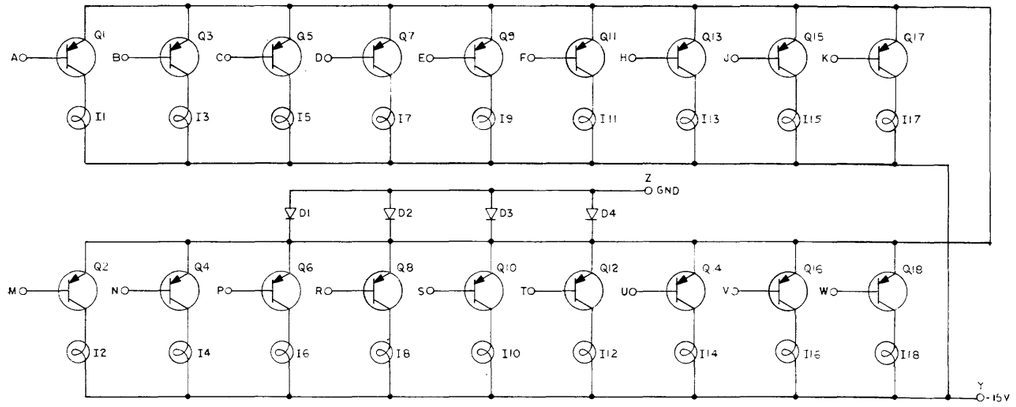


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD
DIODES ARE D-662

*INDICATES BACK PANEL PLUG
22 PIN AMPHENOL #143-022-04

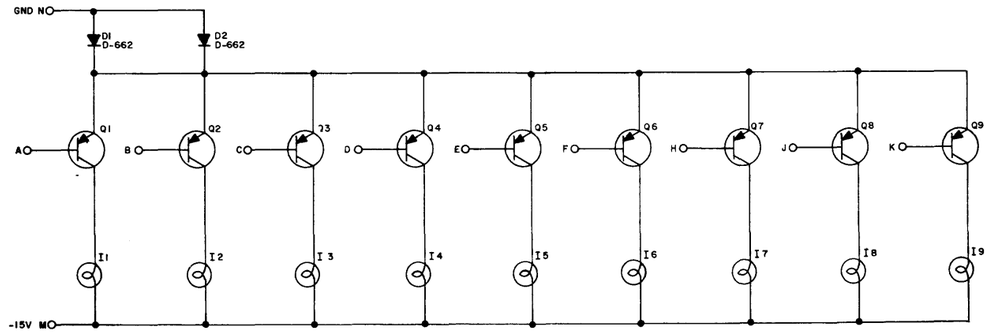
22-Pin Plug Adapter with Bus Driver RS-4802

18-Lamp Bracket RS-4903
9-Lamp Bracket RS-4904



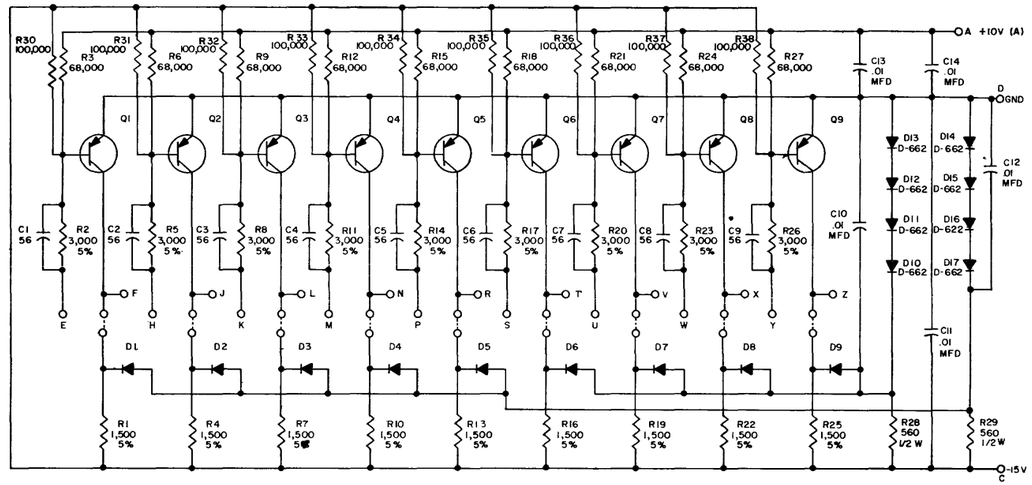
UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE 4JXIC741
DIODES ARE D-662
INDICATOR LIGHTS ARE
DRAKE #11-504, DIALCO #39-28-375
ELDEMA CF ZWT-1762

18-Lamp Bracket RS-4903



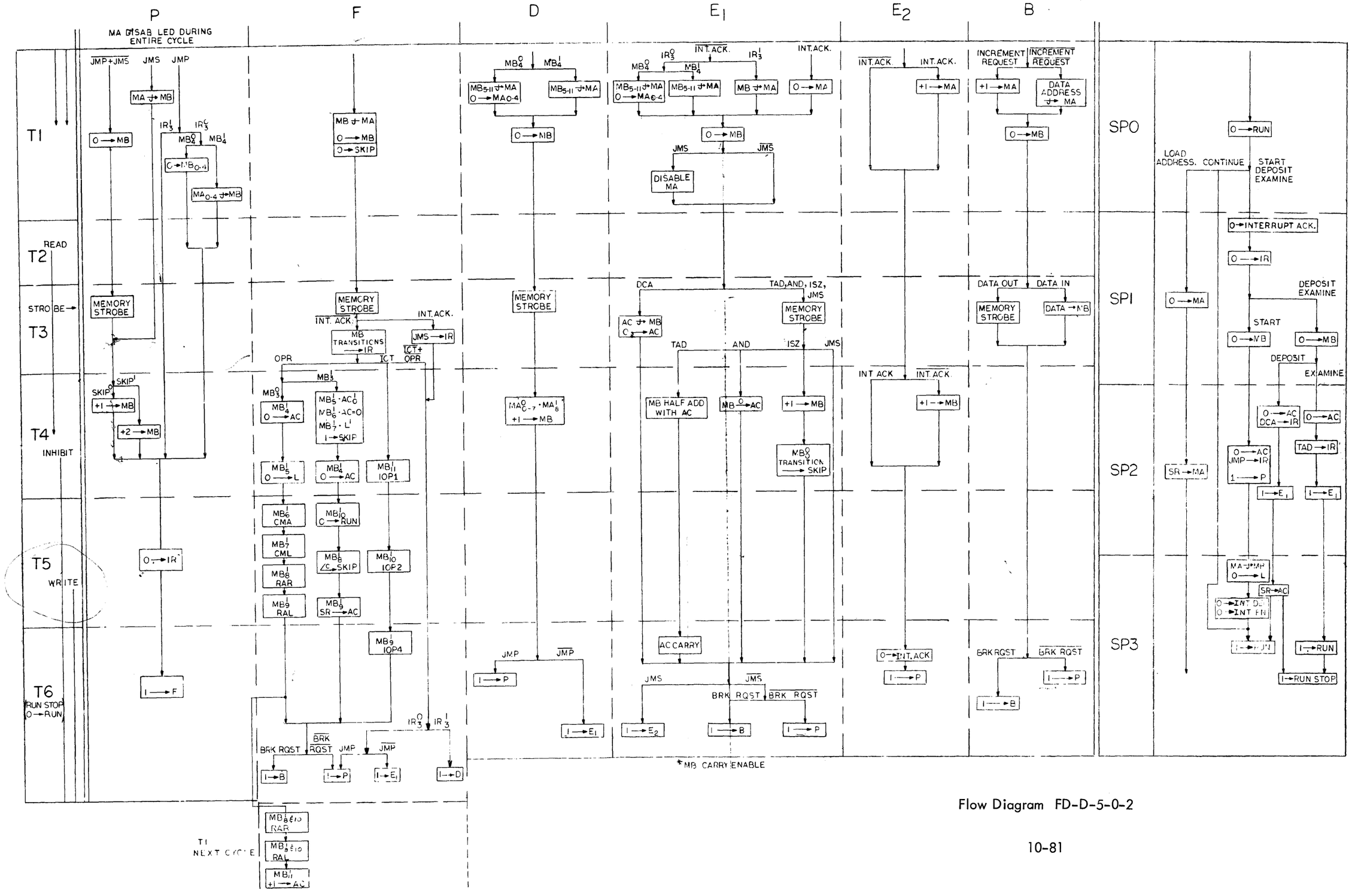
UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE 4JXIC741
INDICATOR LIGHTS ARE ONE OF
THE FOLLOWING;
DRAKE NO. 11-504
DIALCO NO. 39-28-375
ELDEMA NO. CF2-WT-1762

9-Lamp Bracket RS-4904



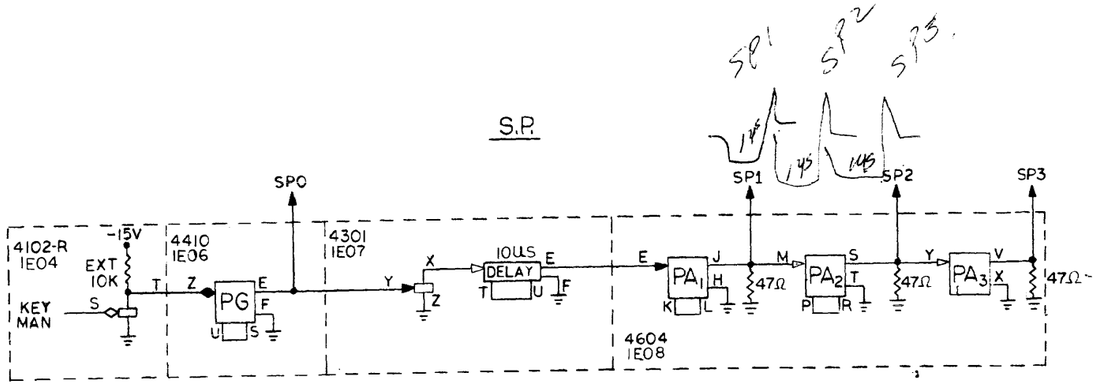
UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD
TRANSISTORS ARE DEC 2894-1
DIODES ARE D-664

Inverter RS-6102

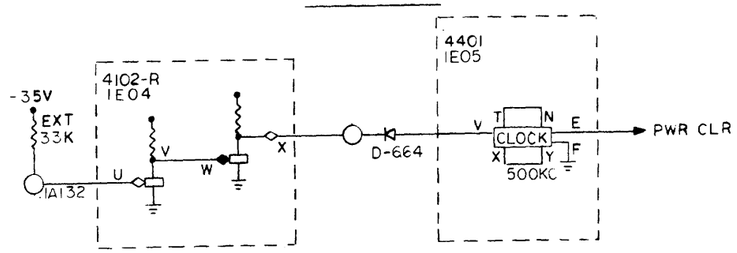


Flow Diagram FD-D-5-0-2

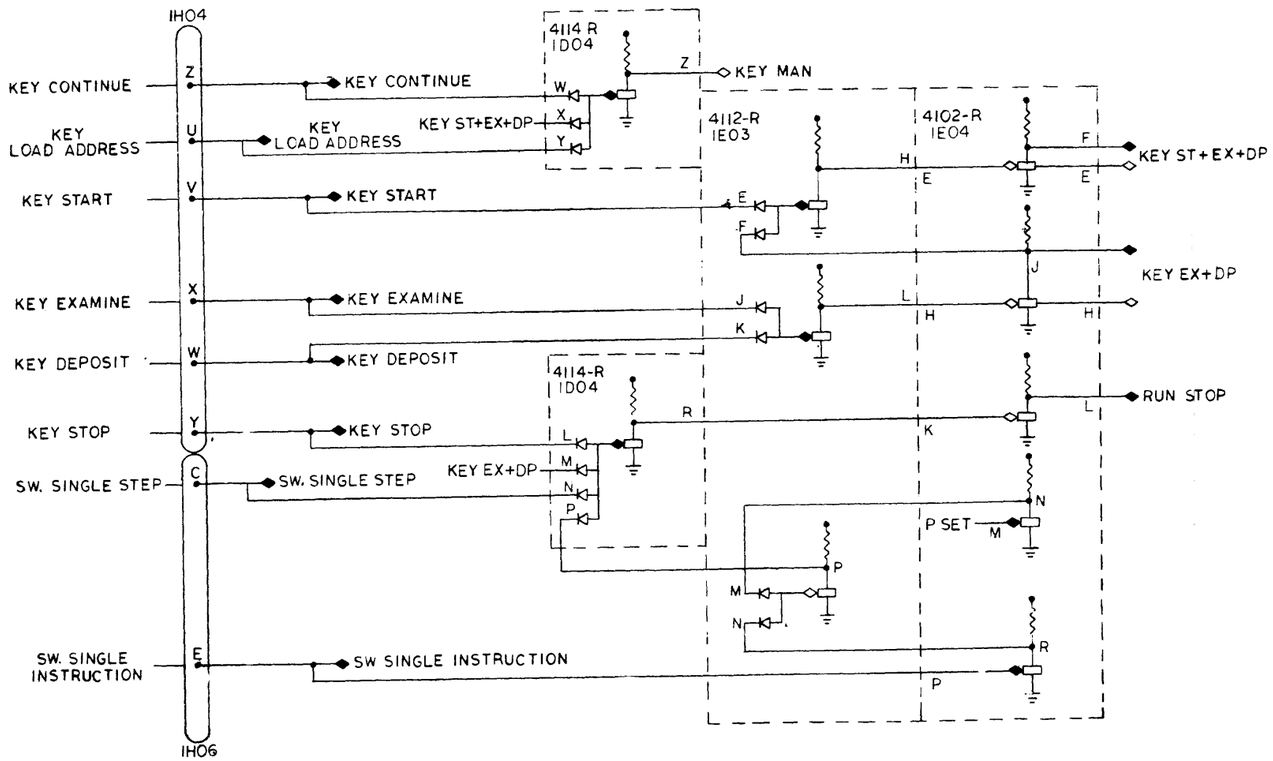
S.P.

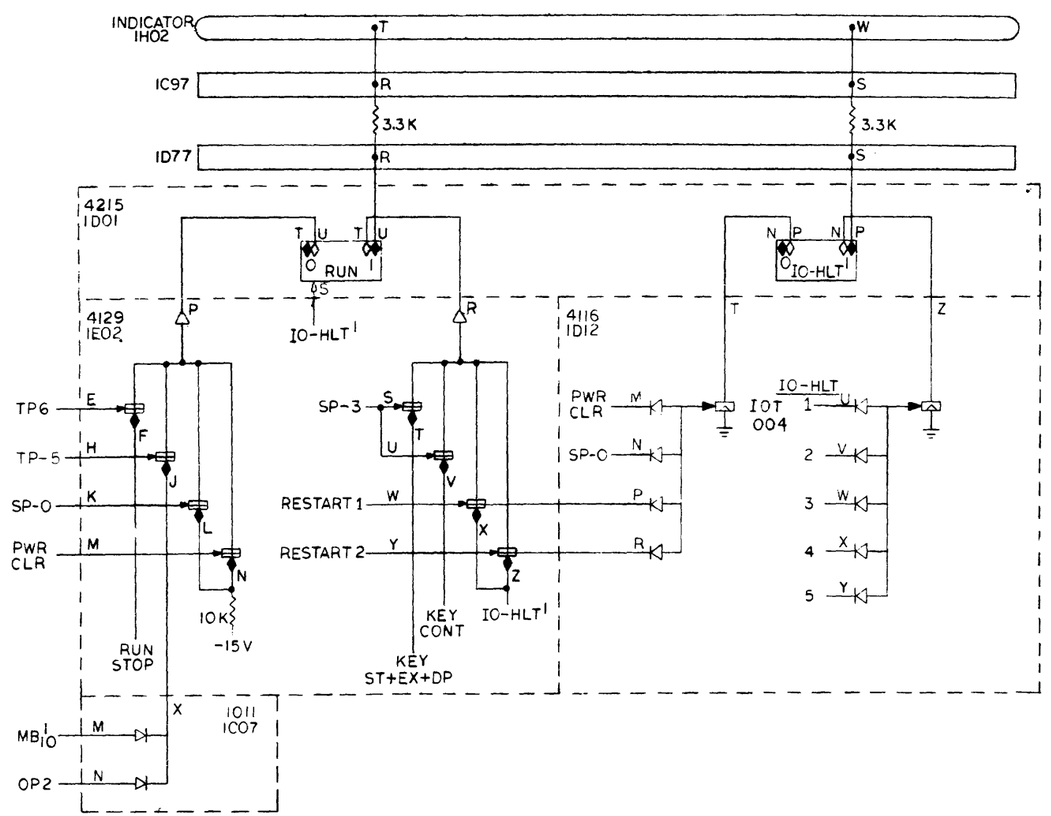


PWR. CLR.

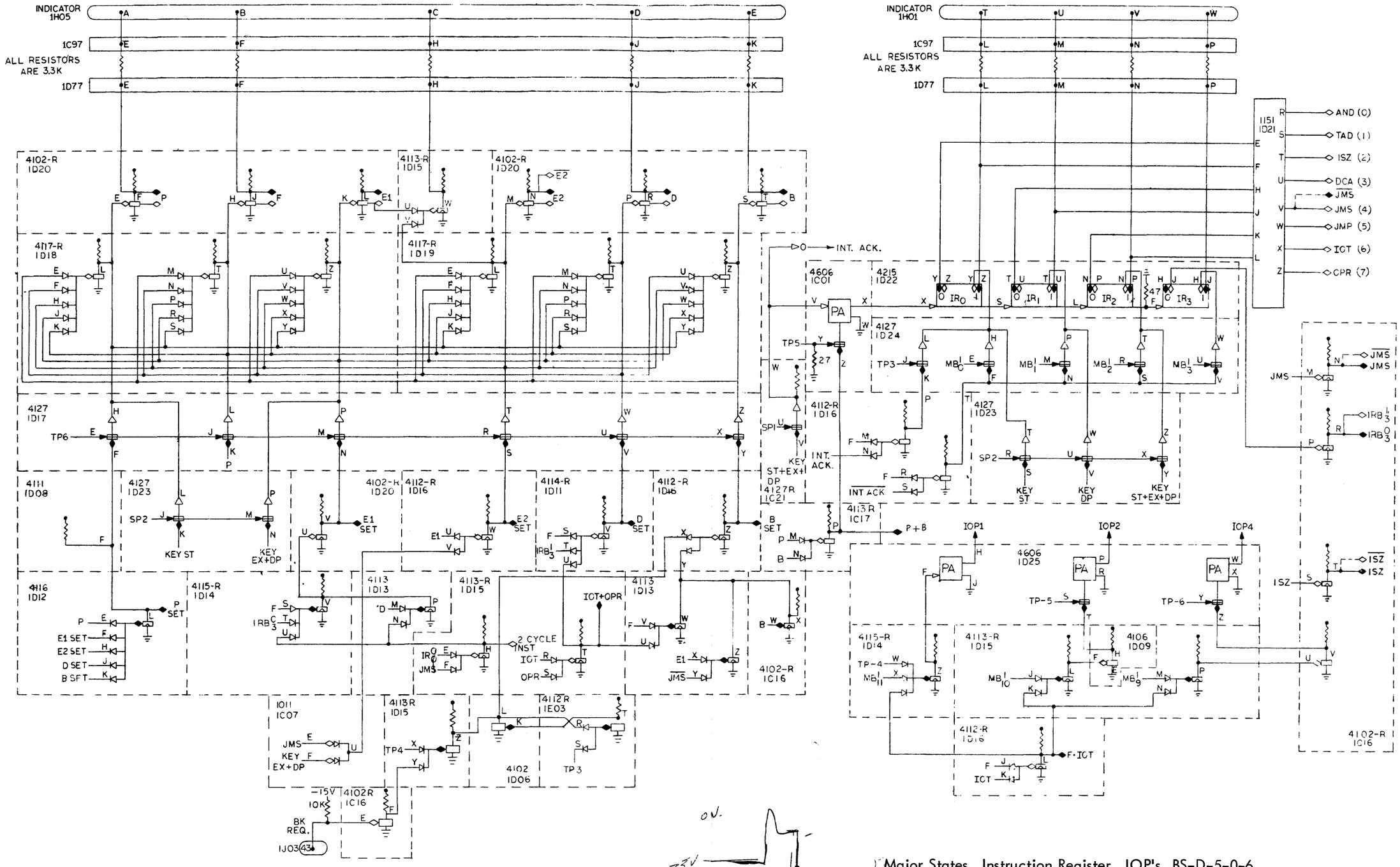


KEYS / SW'S





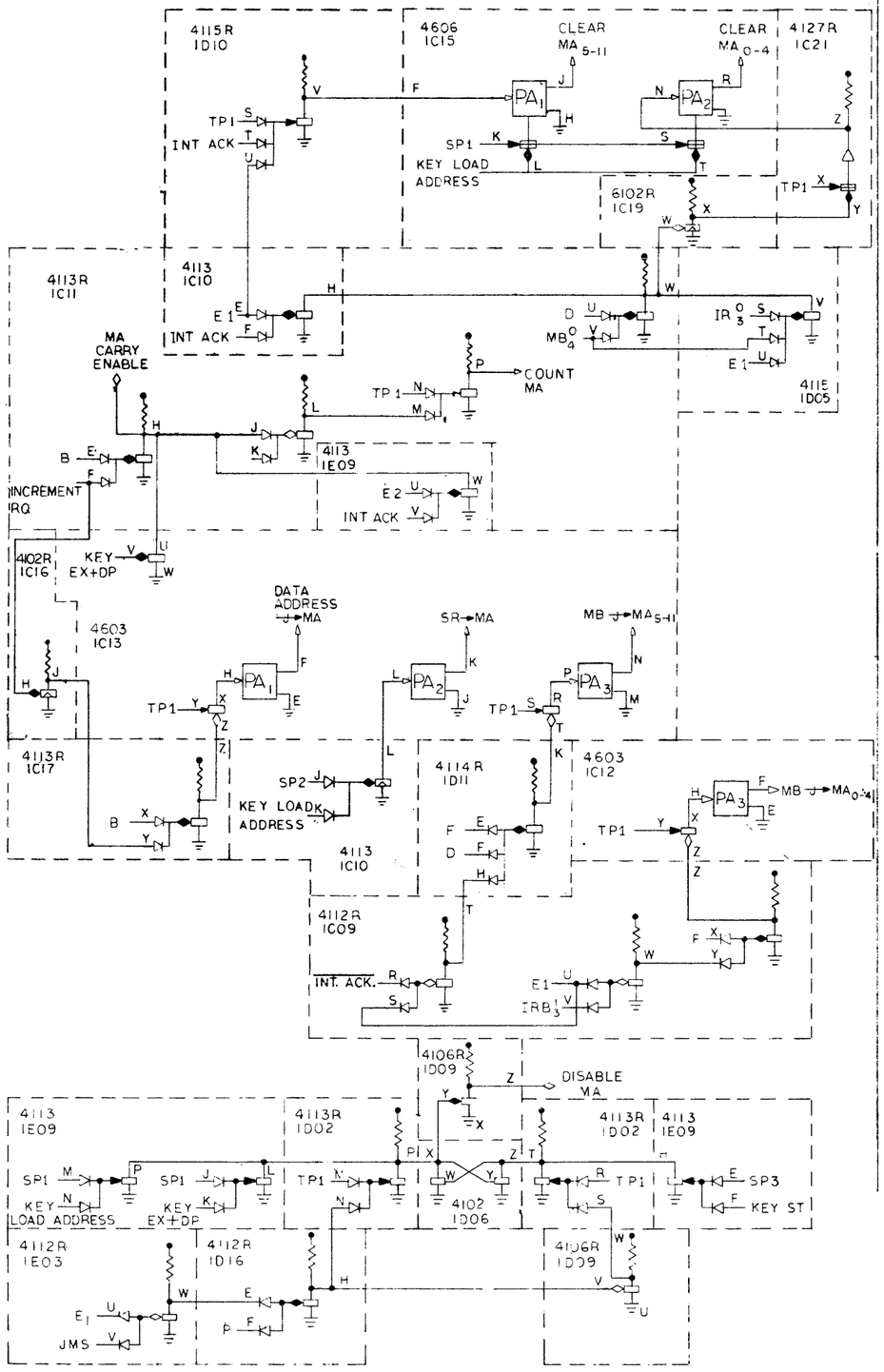
Keys, Switches, Run, I/O Halt, SP's, Power Clear BS-D-5-0-5

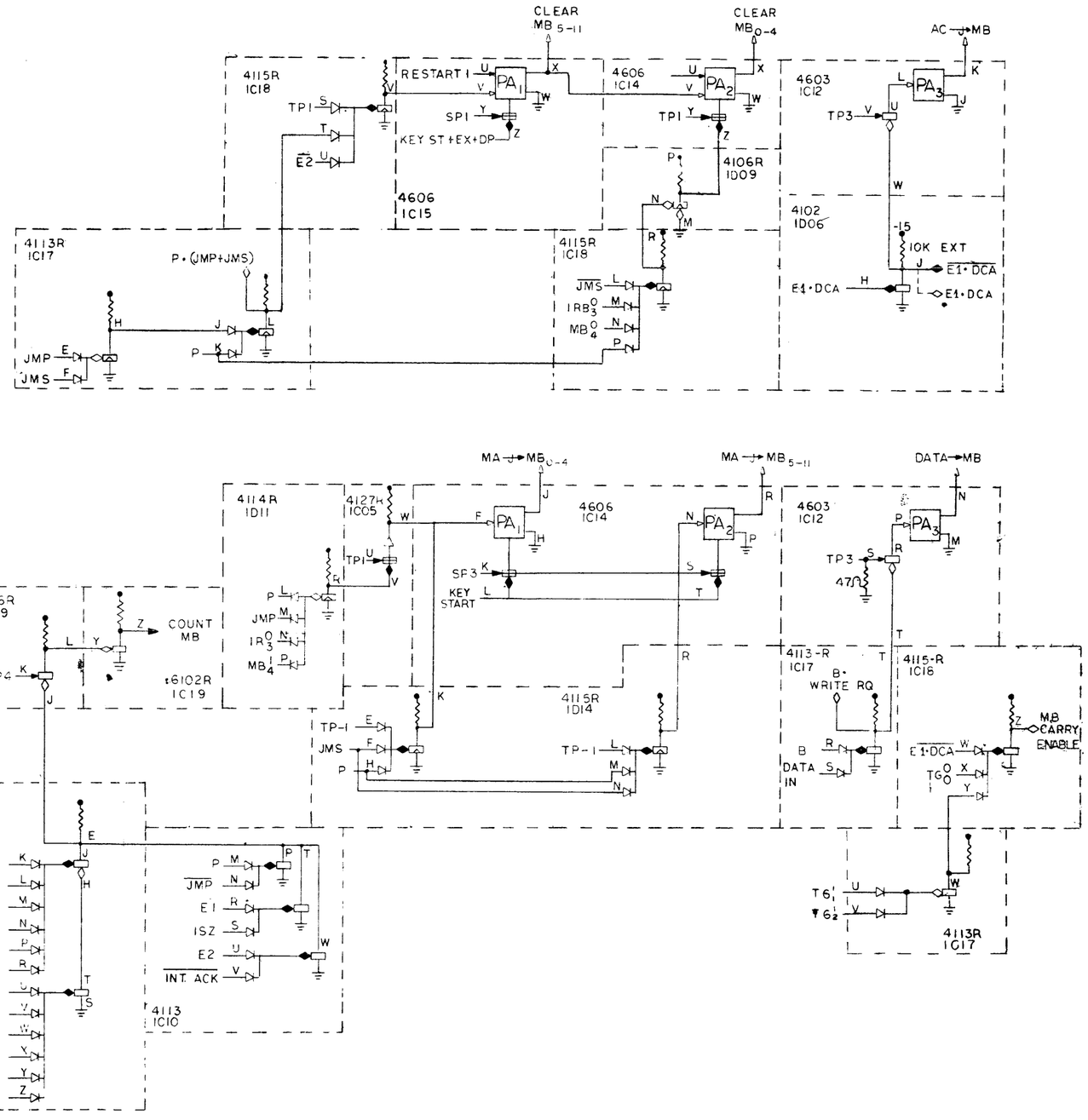


0V.

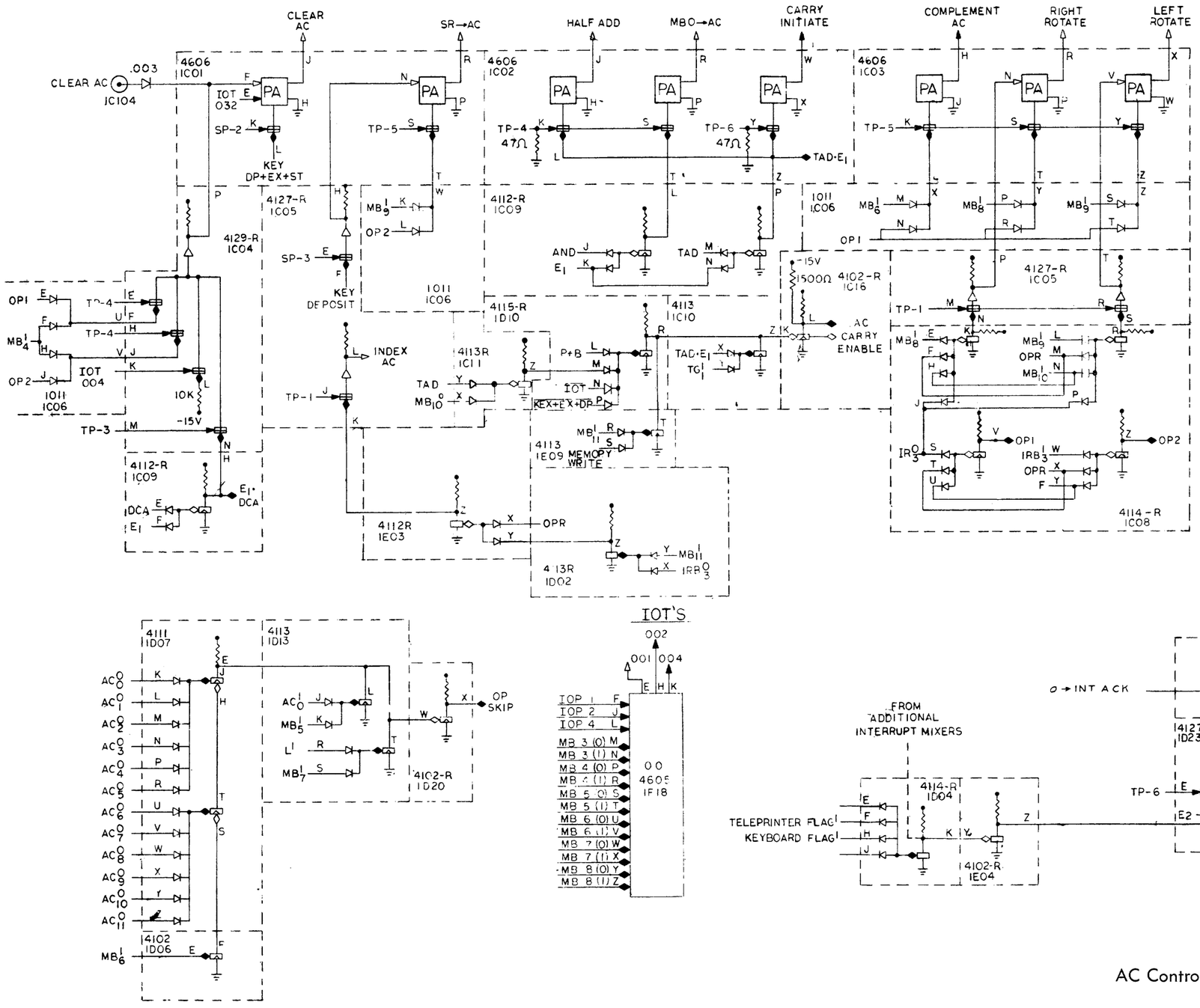
-3V

Major States, Instruction Register, IOP's BS-D-5-0-6

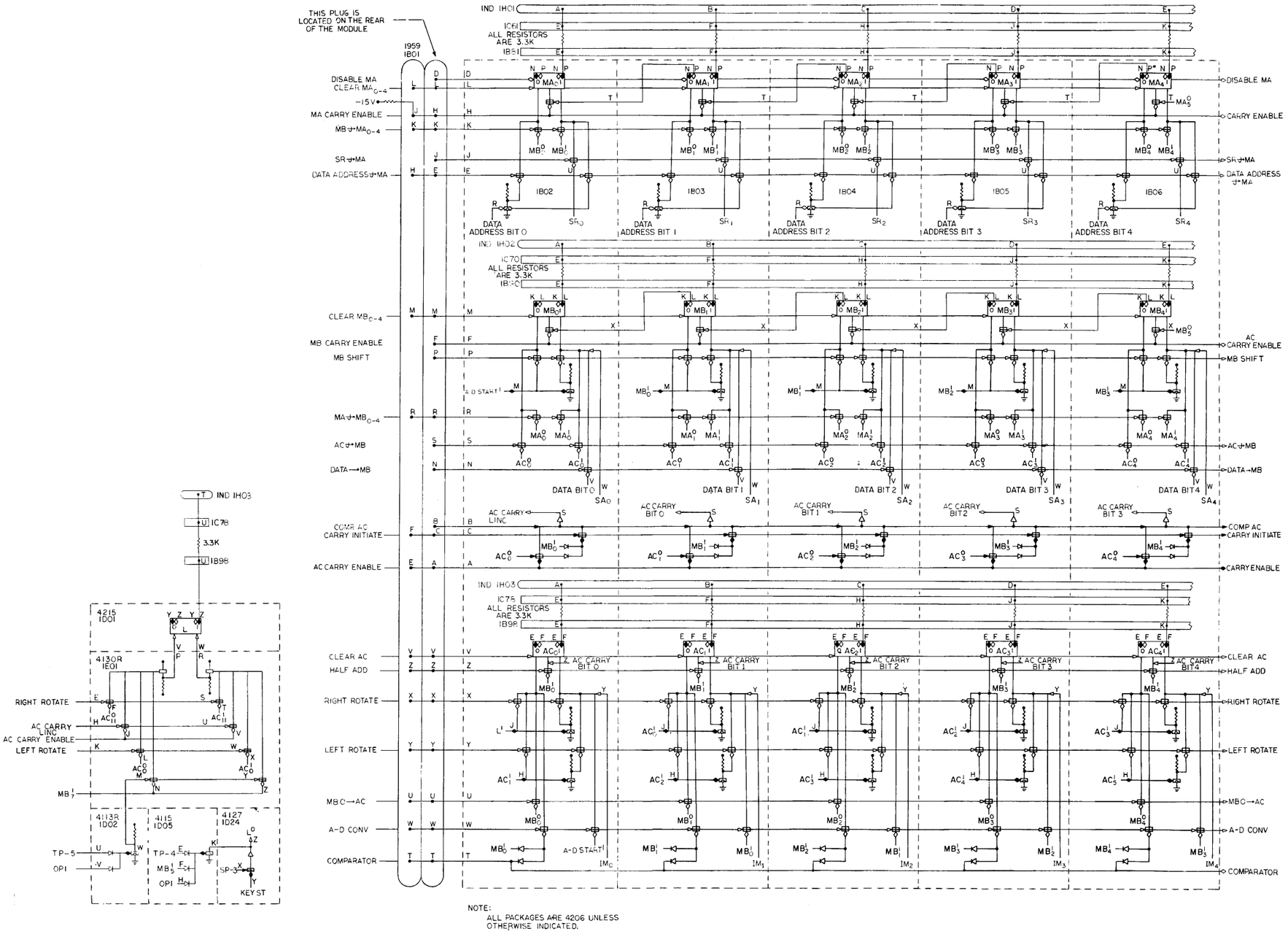




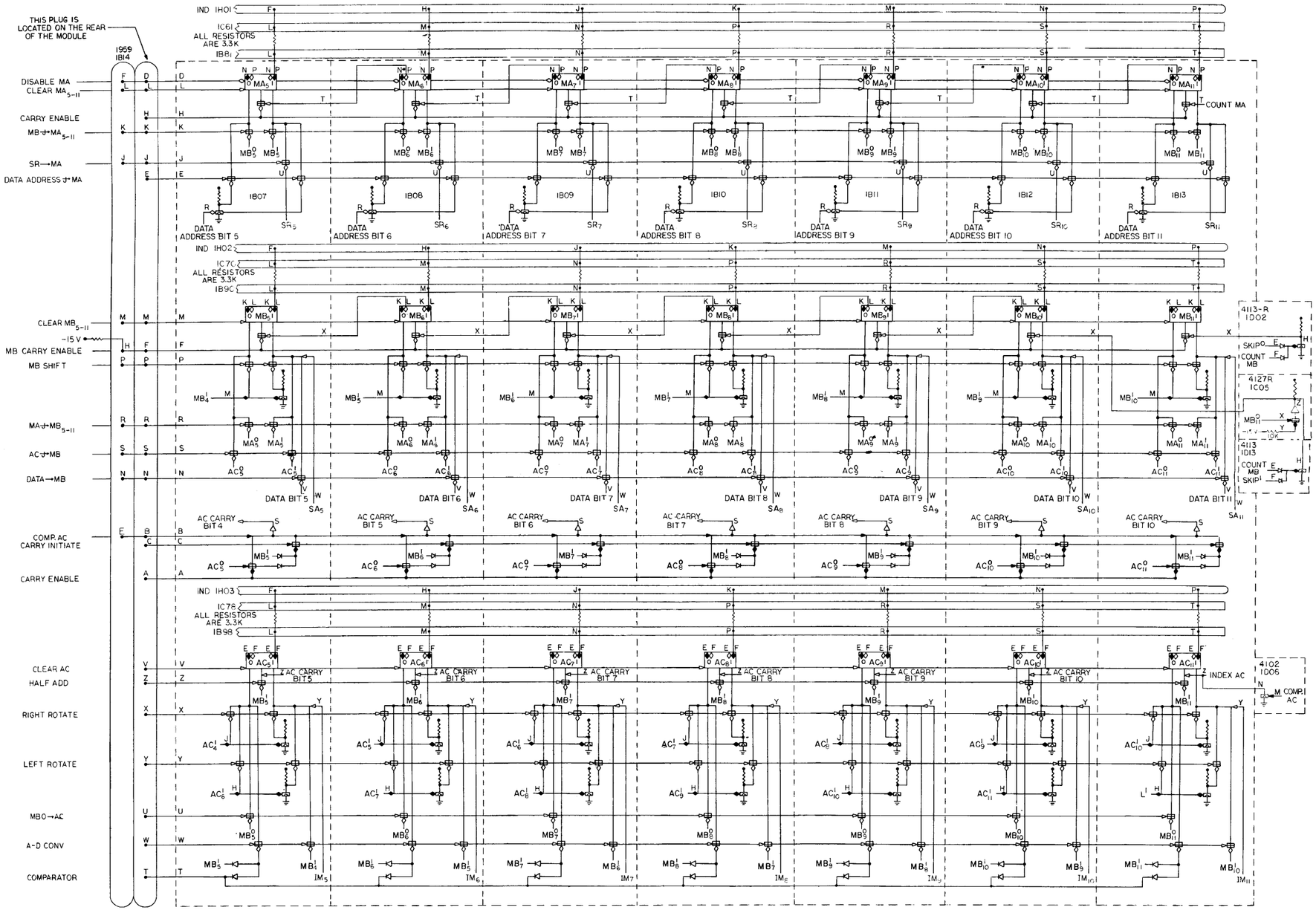
MA and MB Control BS-D-5-0-7



AC Control, Skip, and Interrupt Sync BS-E-5-0-8

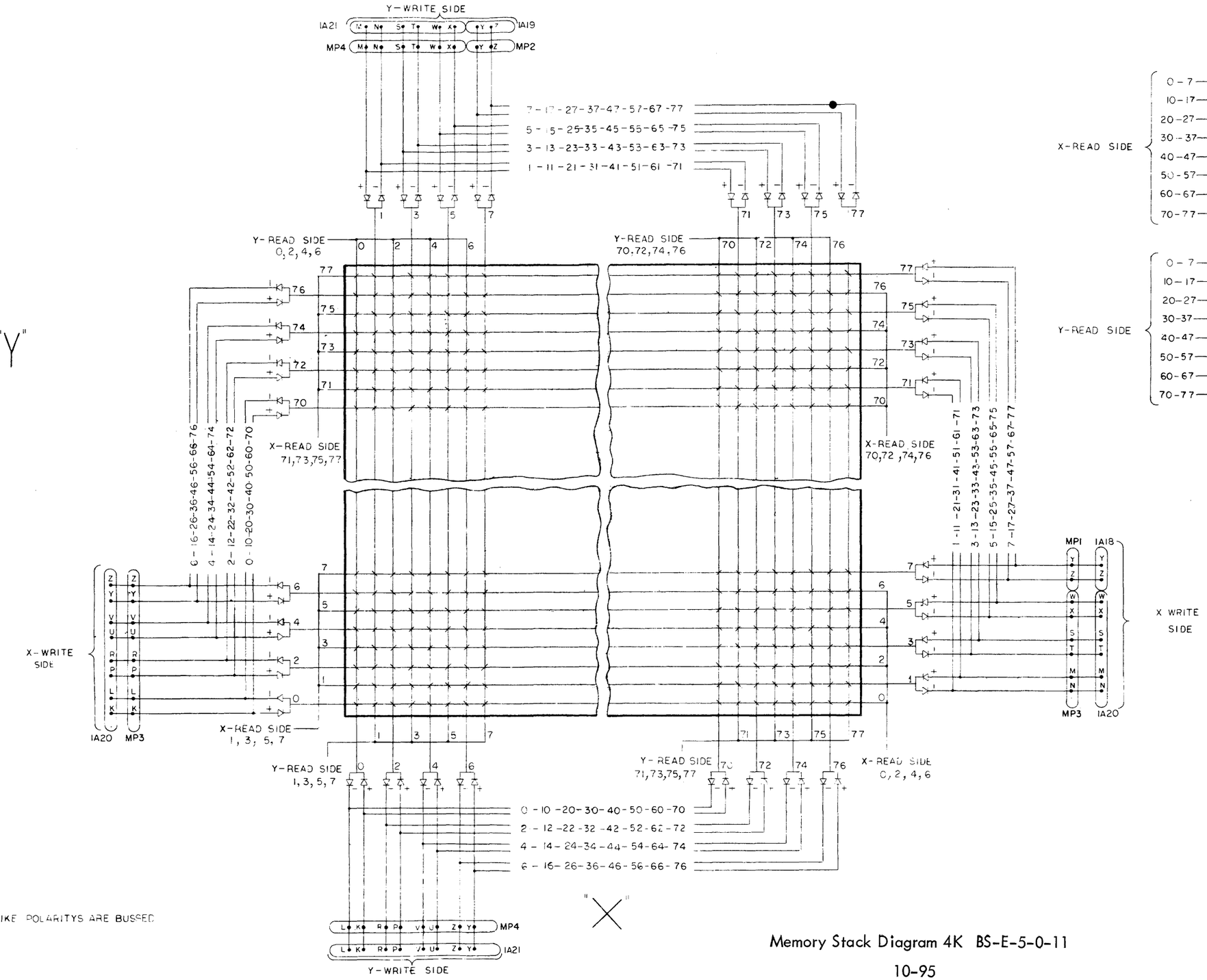


NOTE:
ALL PACKAGES ARE 4206 UNLESS OTHERWISE INDICATED.



NOTE:
ALL PACKAGES ARE 4206 UNLESS OTHERWISE INDICATED.

"Y"



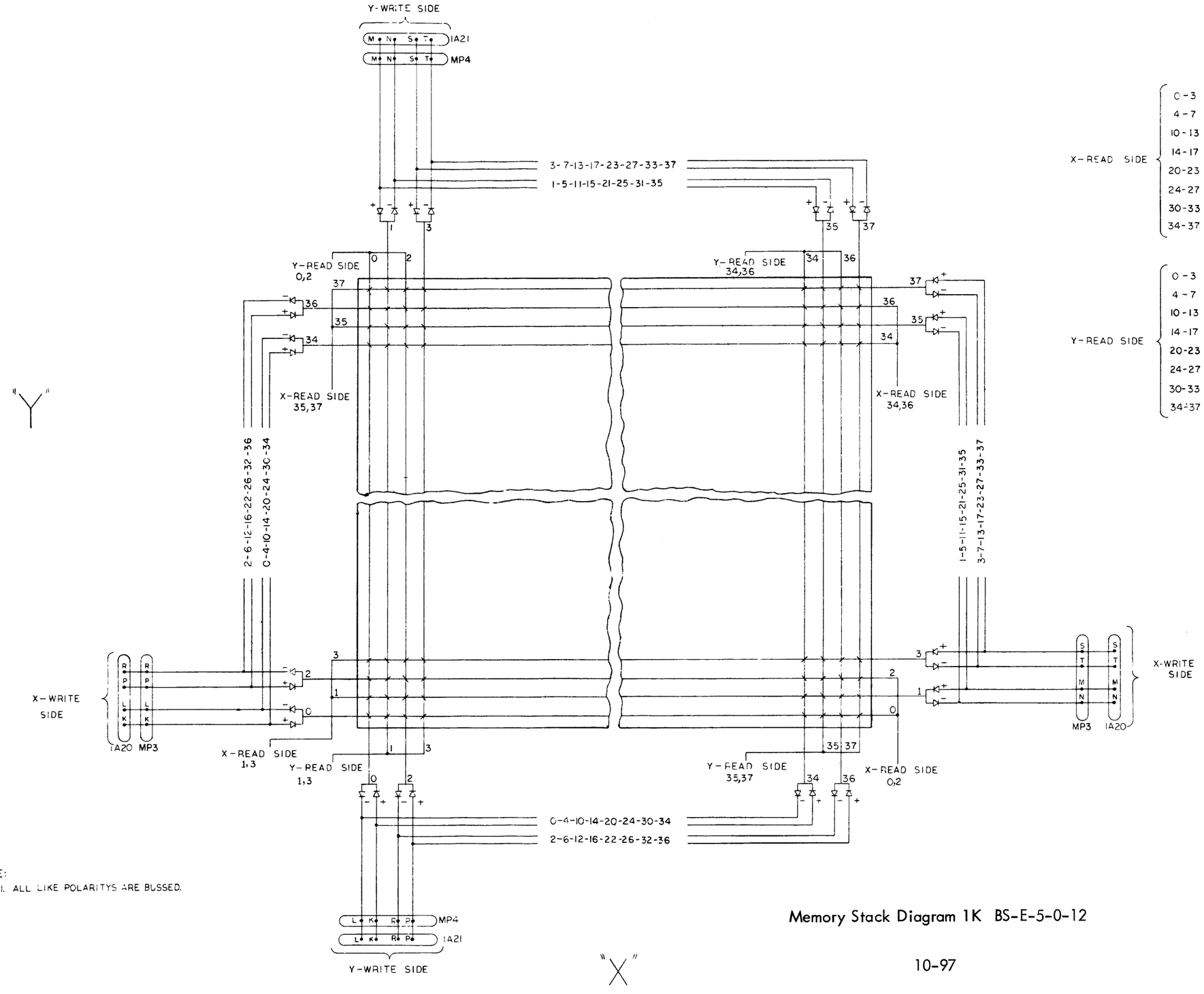
NOTE.

1. ALL LIKE POLARITYS ARE BUSSED

"X"

Memory Stack Diagram 4K BS-E-5-0-11

10-95



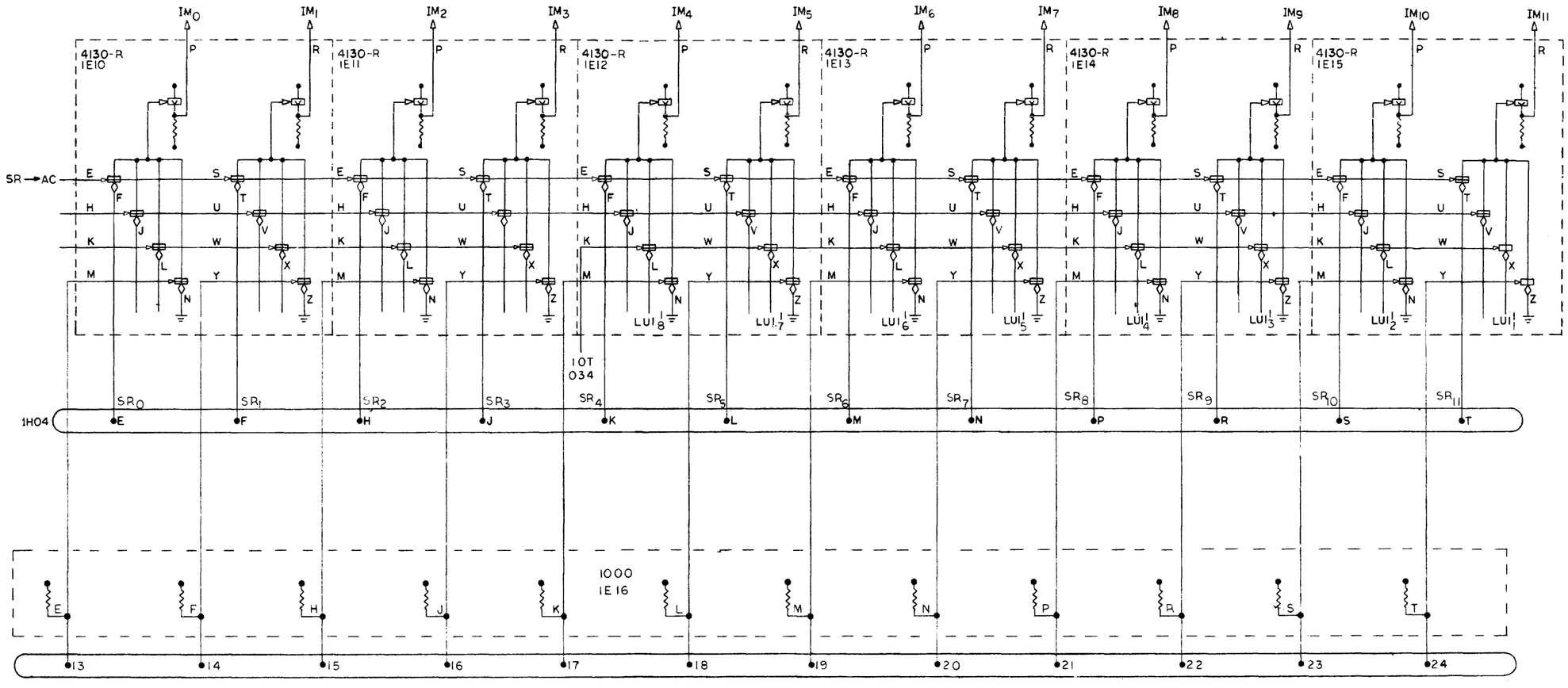
"Y"

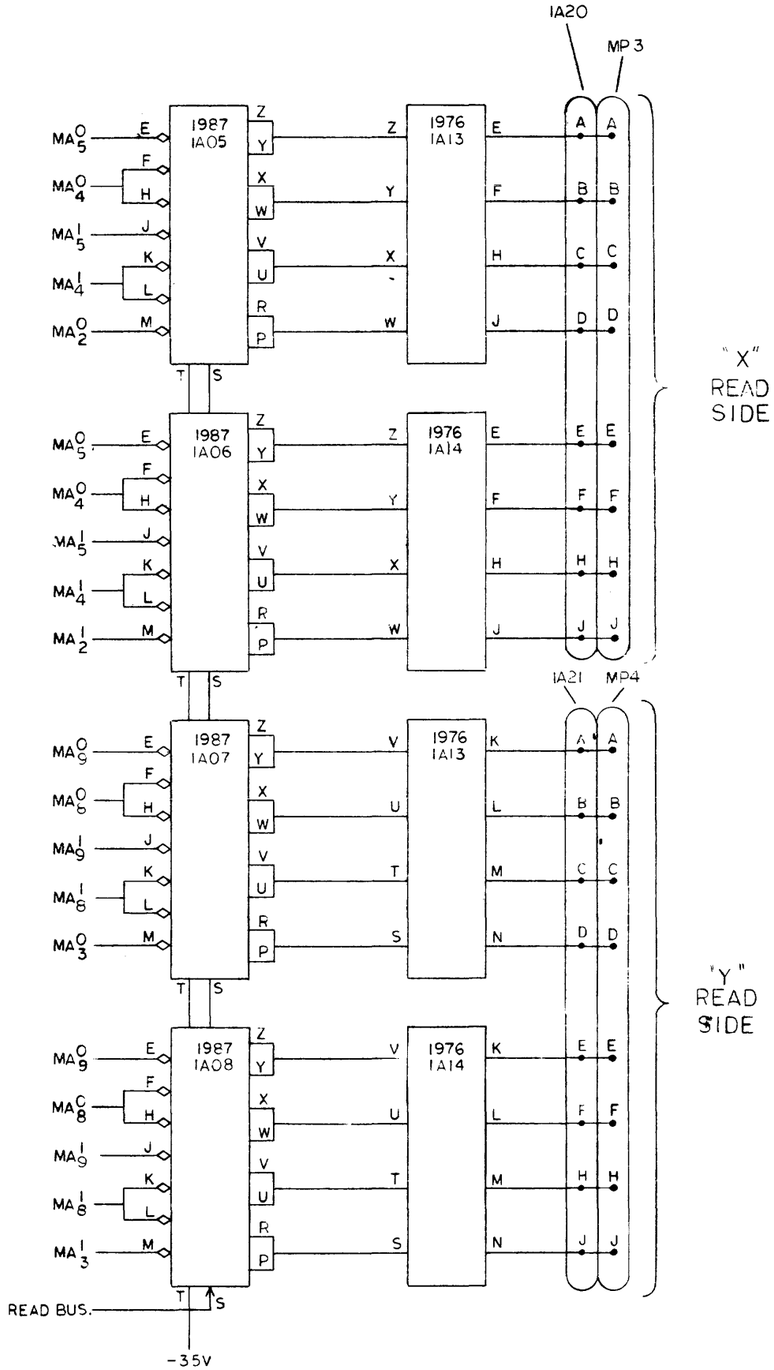
"X"

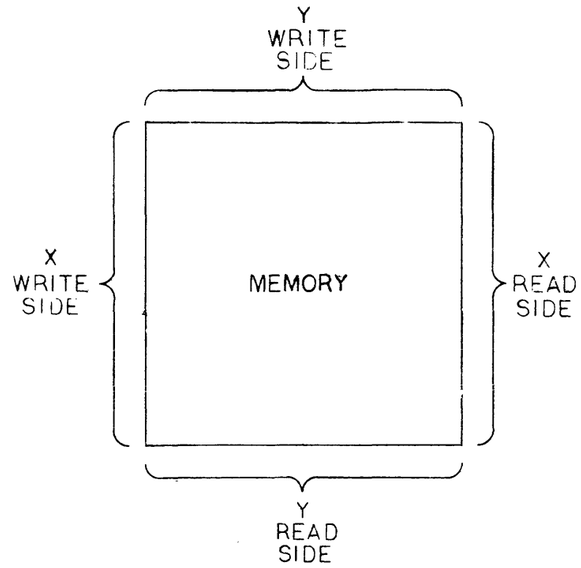
NOTE:
1. ALL LIKE POLARITYS ARE BUSSED.

Memory Stack Diagram 1K BS-E-5-0-12

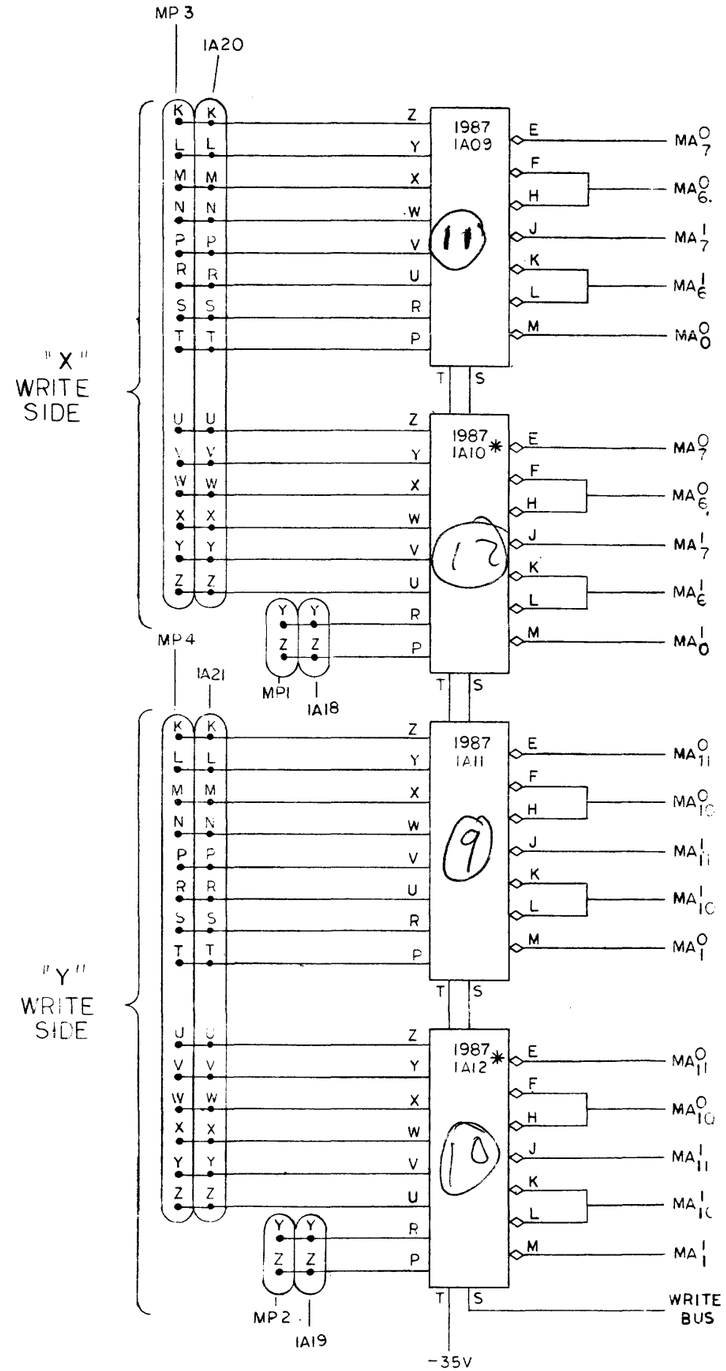
10-97


IM0
IM1
IM2
IM3
IM4
IM5
IM6
IM7
IM8
IM9
IM10
IM11
4130-R
1E10
4130-R
1E11
4130-R
1E12
4130-R
1E13
4130-R
1E14
4130-R
1E15
P
R
SR → AC
E
S
F
T
H
U
J
V
K
W
L
X
M
Y
N
Z
LUI8
LUI7
LUI6
LUI5
LUI4
LUI3
LUI2
LUI1
1OT
034
SR0
SR1
SR2
SR3
SR4
SR5
SR6
SR7
SR8
SR9
SR10
SR11
1H04
1000
1E16
50 PIN
AMP
1J1
13
14
15
16
17
18
19
20
21
22
23
24

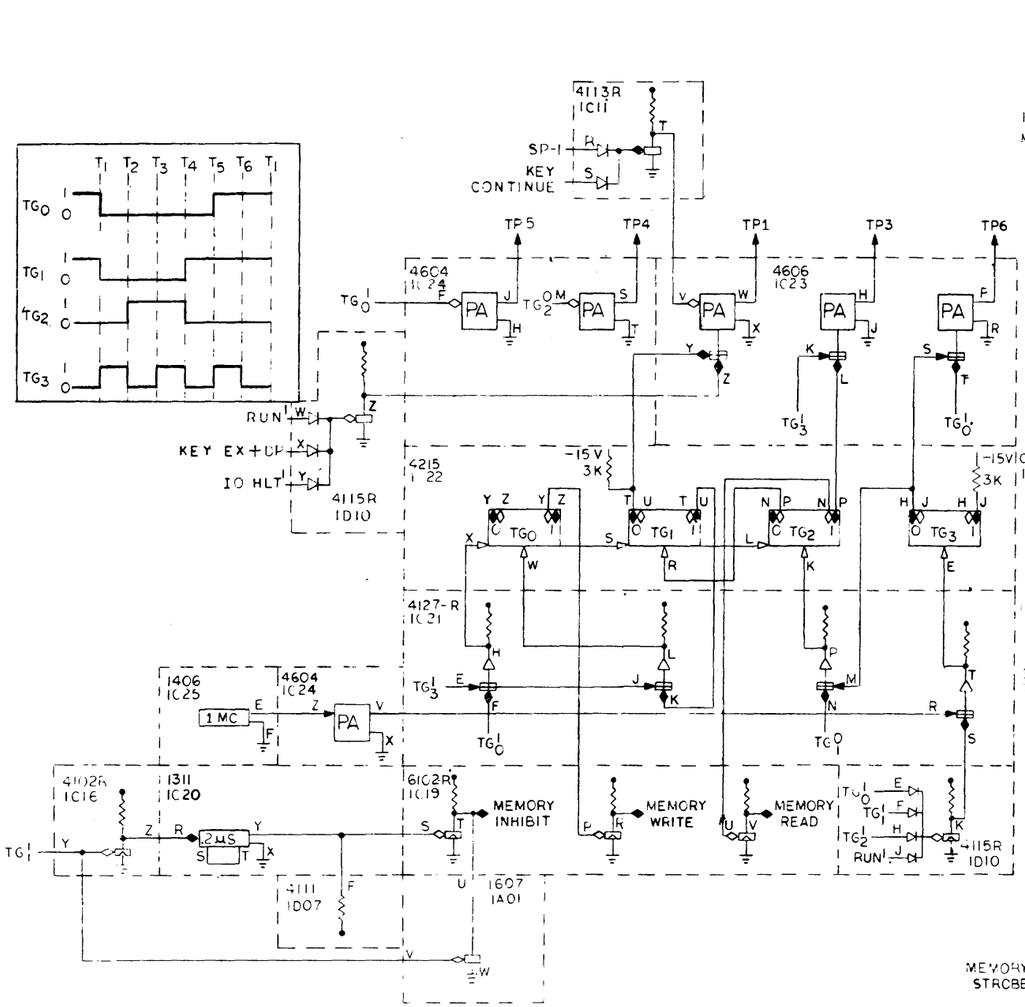


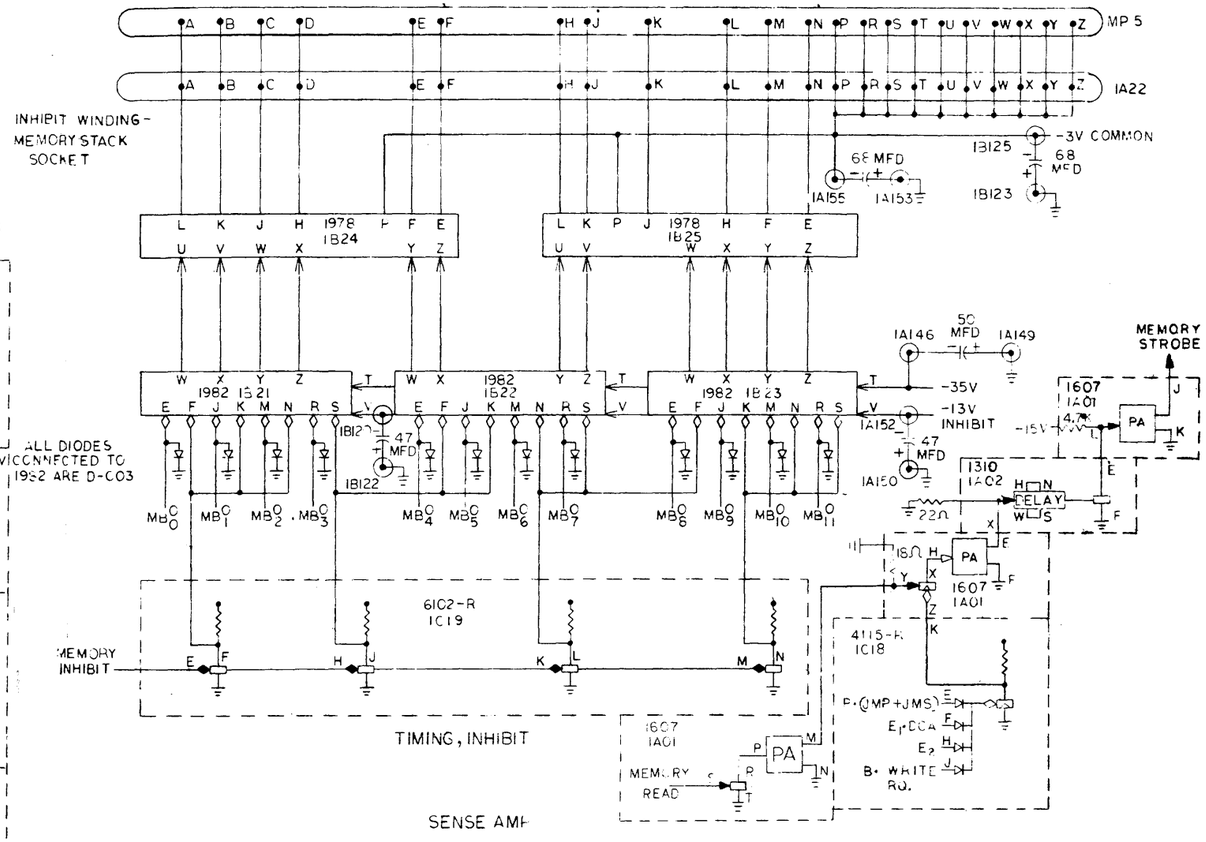


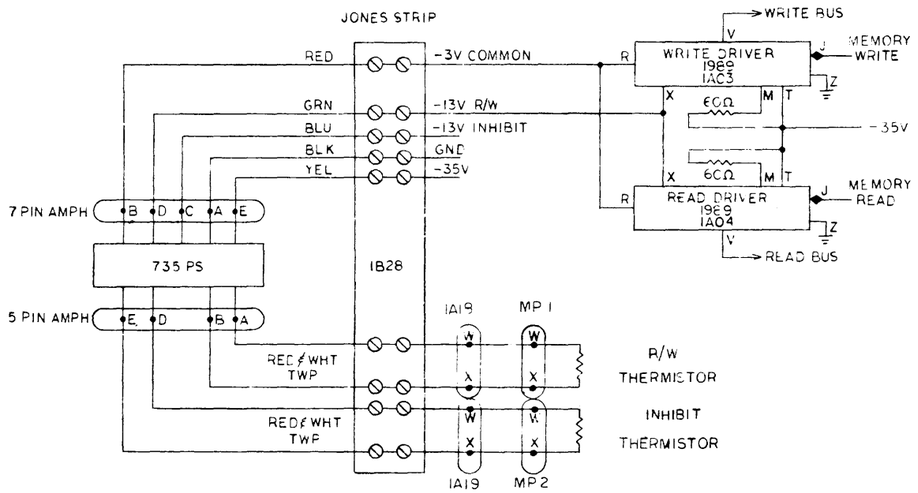
NOTE:
* IF 1K MEMORY IS USED REMOVE PACKAGES 1987 IA10 AND 1987 IA12

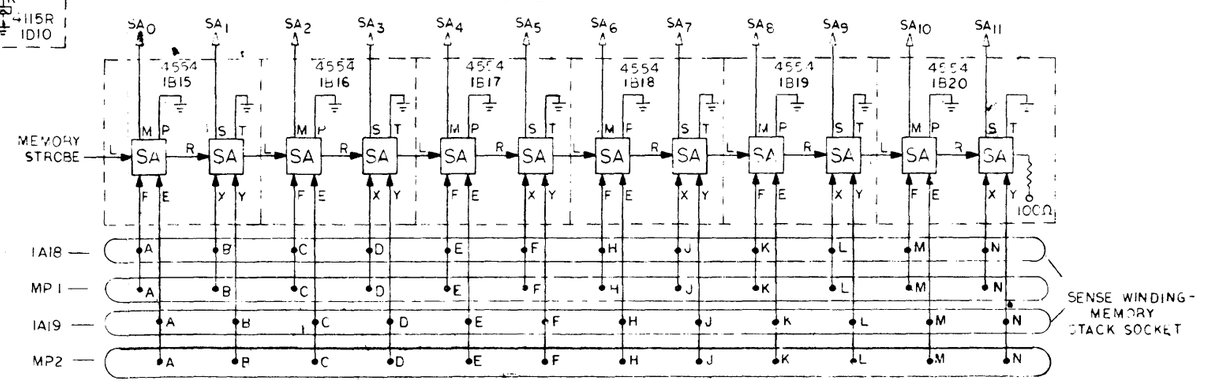


Memory "X" and "Y" Selection BS-D-5-0-16

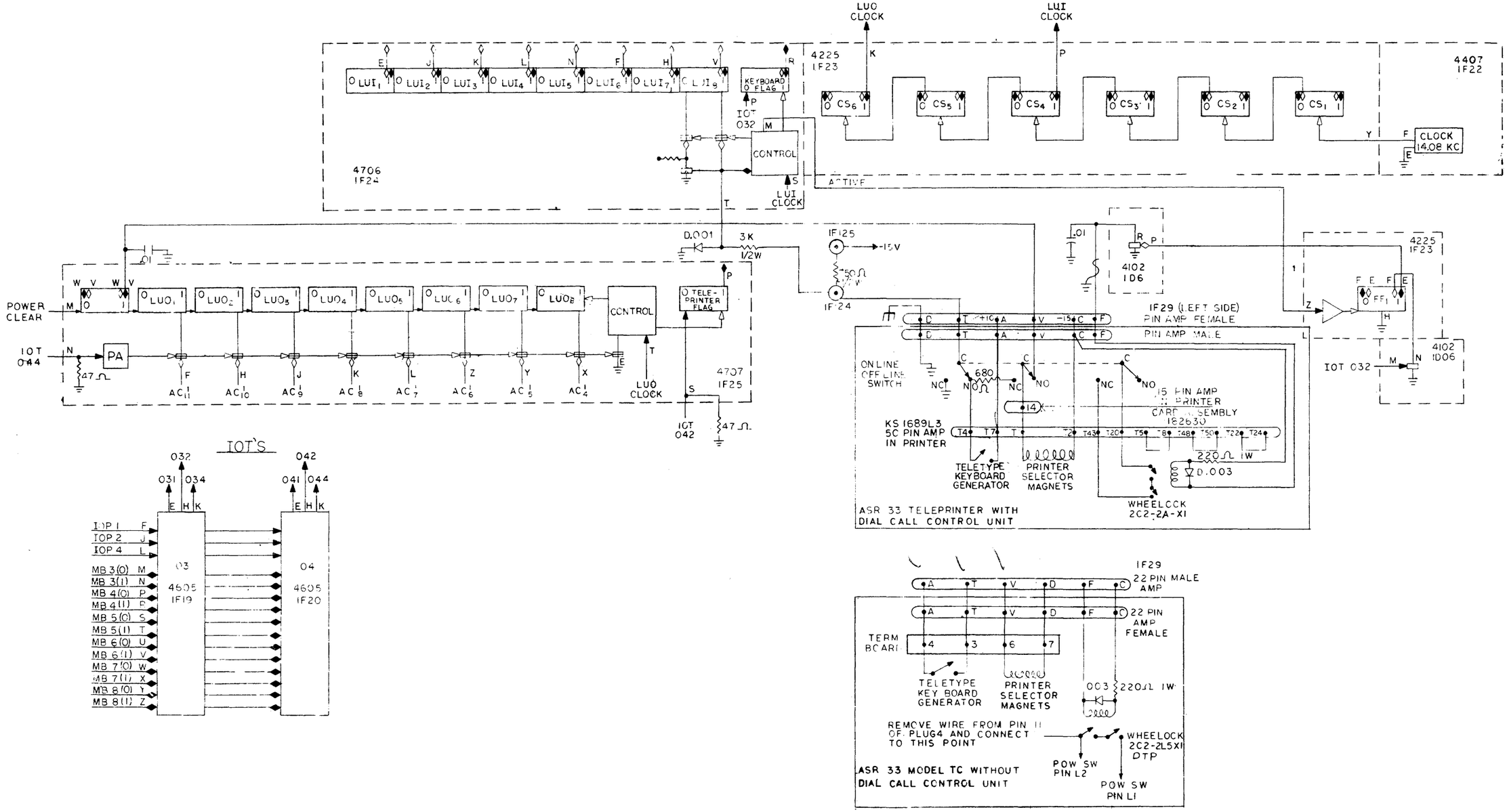






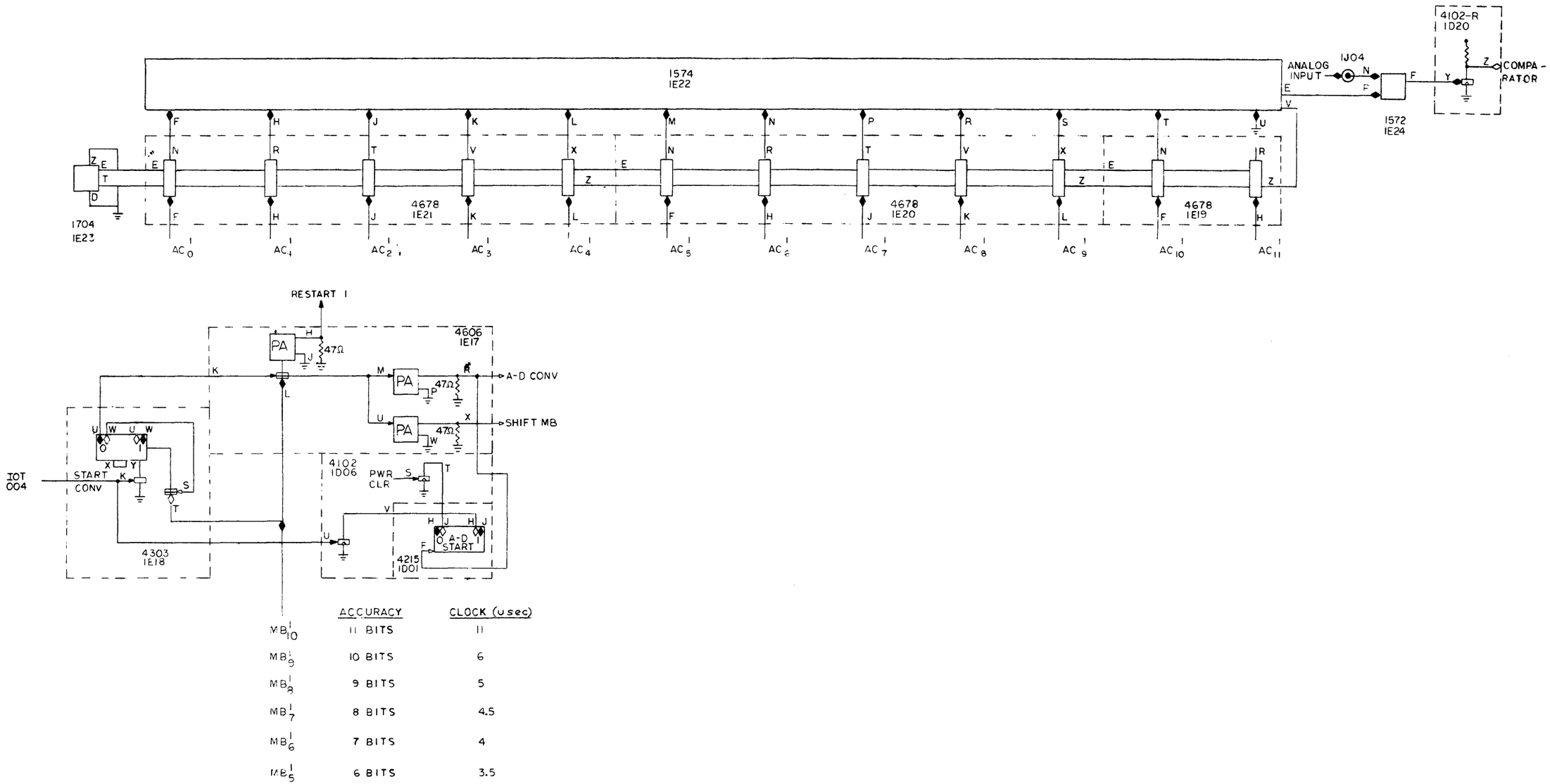


Memory System Timing, Inhibit, Sense Amplifier Output BS-D-5-0-17

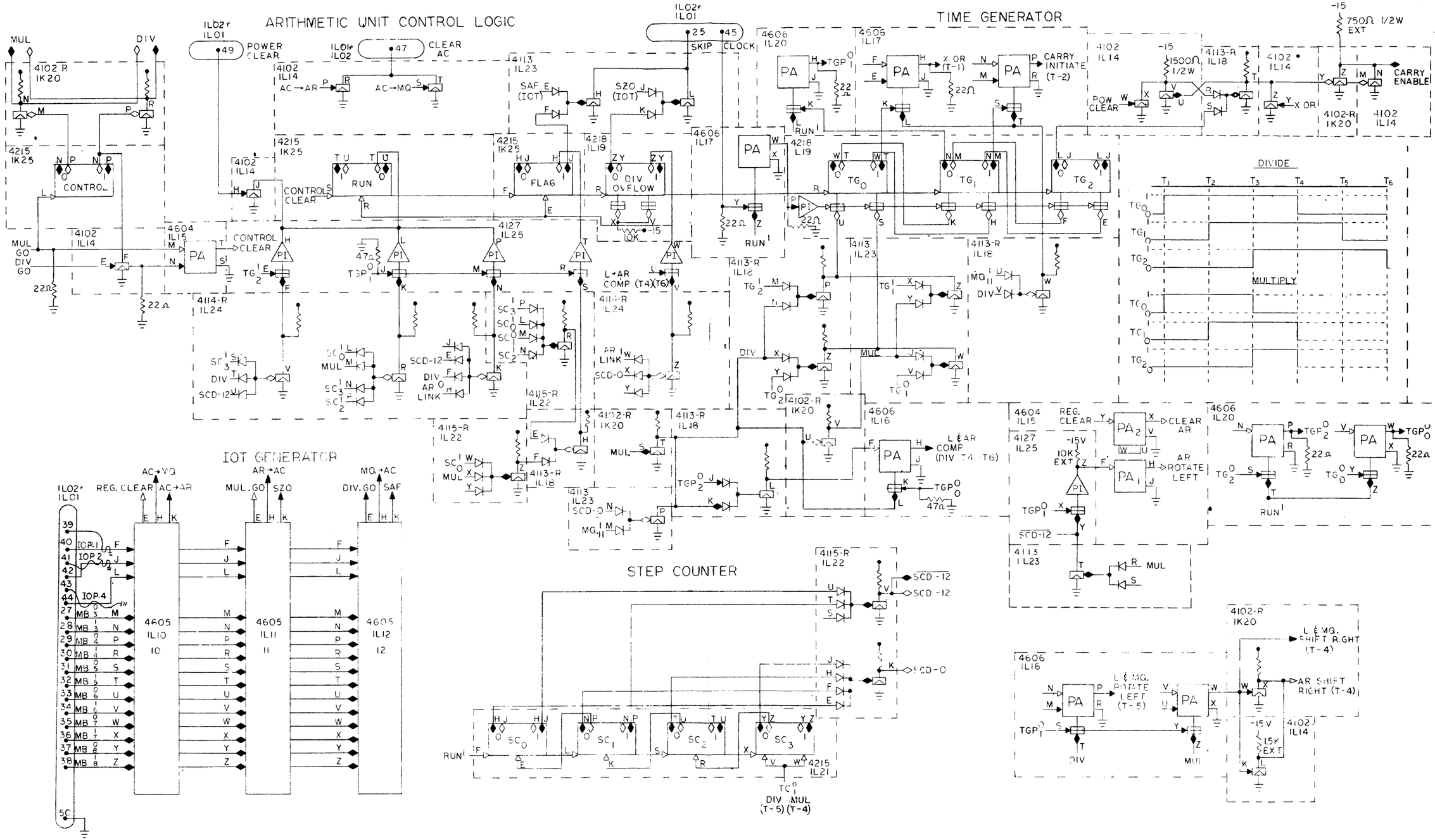

LUO CLOCK
LUI CLOCK
4225 IF23
4407 IF22
4706 IF24
KEYBOARD FLAG
IOT 032
CONTROL
LUI CLOCK
ACTIVE
CLOCK 14.08 KC
D.001
3K 1/2W
IF125
-15V
50Ω 1/2W
IF24
.01
4102 1D6
POWER CLEAR
IOT 044
PA
47Ω
TELE-PRINTER FLAG
LUO CLOCK
4707 IF25
IOT 042
IF29 (LEFT SIDE)
PIN AMP FEMALE
PIN AMP MALE
ON LINE OFF LINE SWITCH
680Ω
15 PIN AMP IN PRINTER CARD ASSEMBLY 182630
KS 1689L3 5C PIN AMP IN PRINTER
220Ω 1W
D.003
TELETYPE KEYBOARD GENERATOR
PRINTER SELECTOR MAGNETS
WHEELOCK 2C2-2A-X1
ASR 33 TELEPRINTER WITH DIAL CALL CONTROL UNIT
IOT 032
IOT'S
032
031 034
041 044
03
4605 IF19
04
4605 IF20
IOP 1
IOP 2
IOP 4
MB 3(0)
MB 3(1)
MB 4(0)
MB 4(1)
MB 5(0)
MB 5(1)
MB 6(0)
MB 6(1)
MB 7(0)
MB 7(1)
MB 8(0)
MB 8(1)
IF29
22 PIN MALE AMP
22 PIN AMP FEMALE
TERM BOARD
TELETYPE KEY BOARD GENERATOR
PRINTER SELECTOR MAGNETS
D03 220Ω 1W
REMOVE WIRE FROM PIN 11 OF PLUG4 AND CONNECT TO THIS POINT
WHEELOCK 2C2-2L5X1 DTP
POW SW PIN L2
POW SW PIN L1
ASR 33 MODEL TC WITHOUT DIAL CALL CONTROL UNIT

Output Bus Drivers BS-D-5-0-31

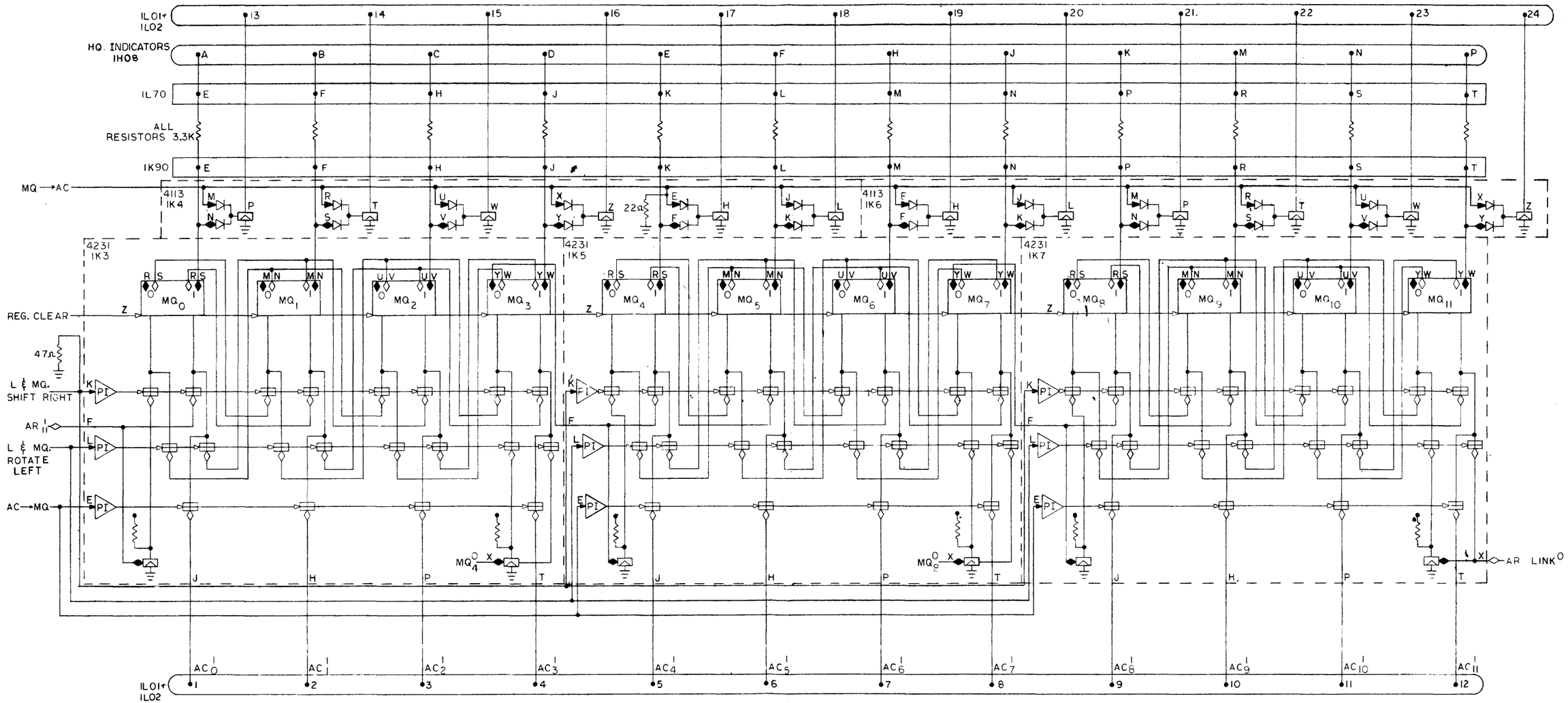
Output Bus Drivers BS-D-5-0-31



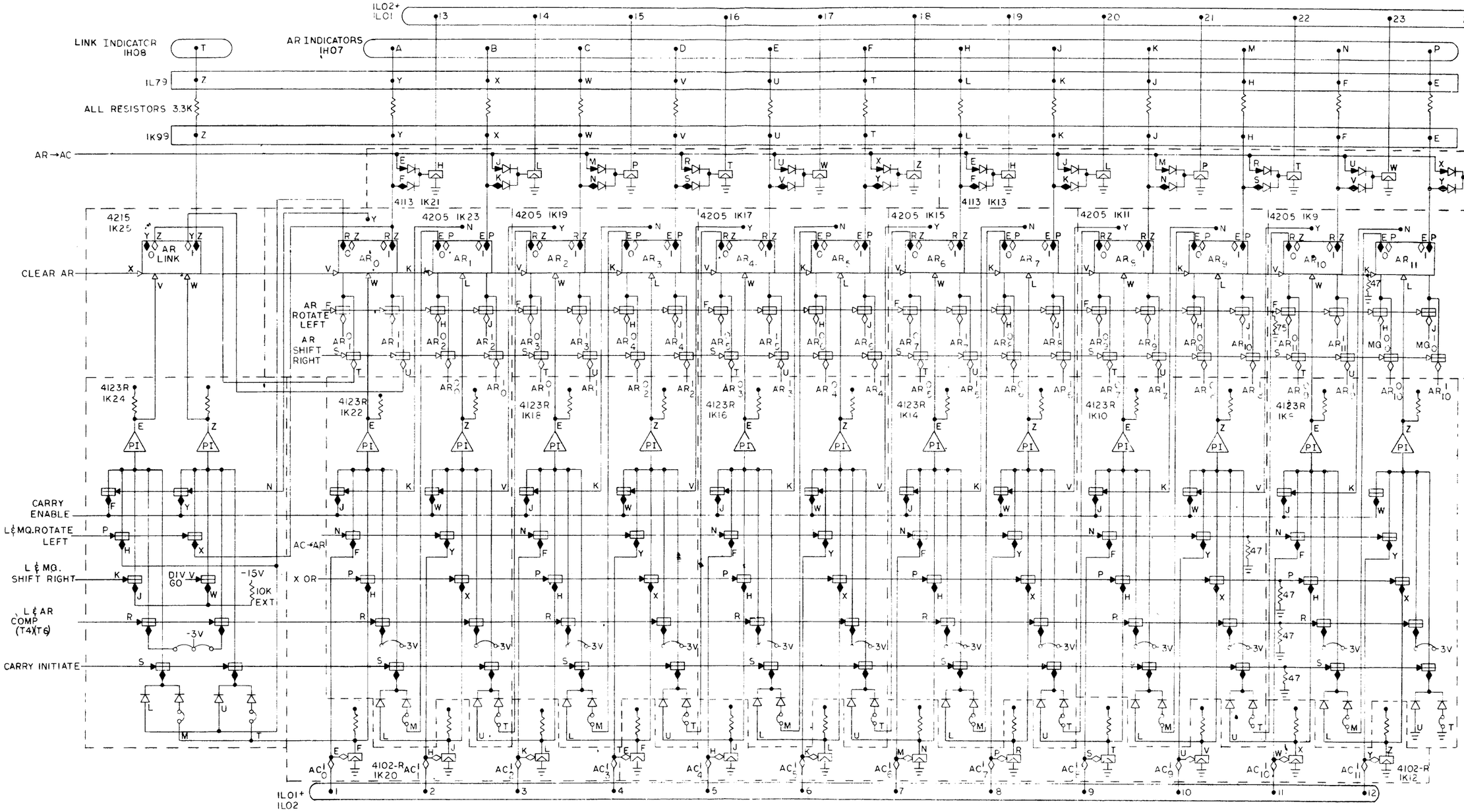
	ACCURACY	CLOCK (μsec)
MB_{10}^{I}	11 BITS	11
MB_{9}^{I}	10 BITS	6
MB_{8}^{I}	9 BITS	5
MB_{7}^{I}	8 BITS	4.5
MB_{6}^{I}	7 BITS	4
MB_{5}^{I}	6 BITS	3.5



AR Control, IOT Gen., Step Counter, Time Gen BS-D-153-0-5

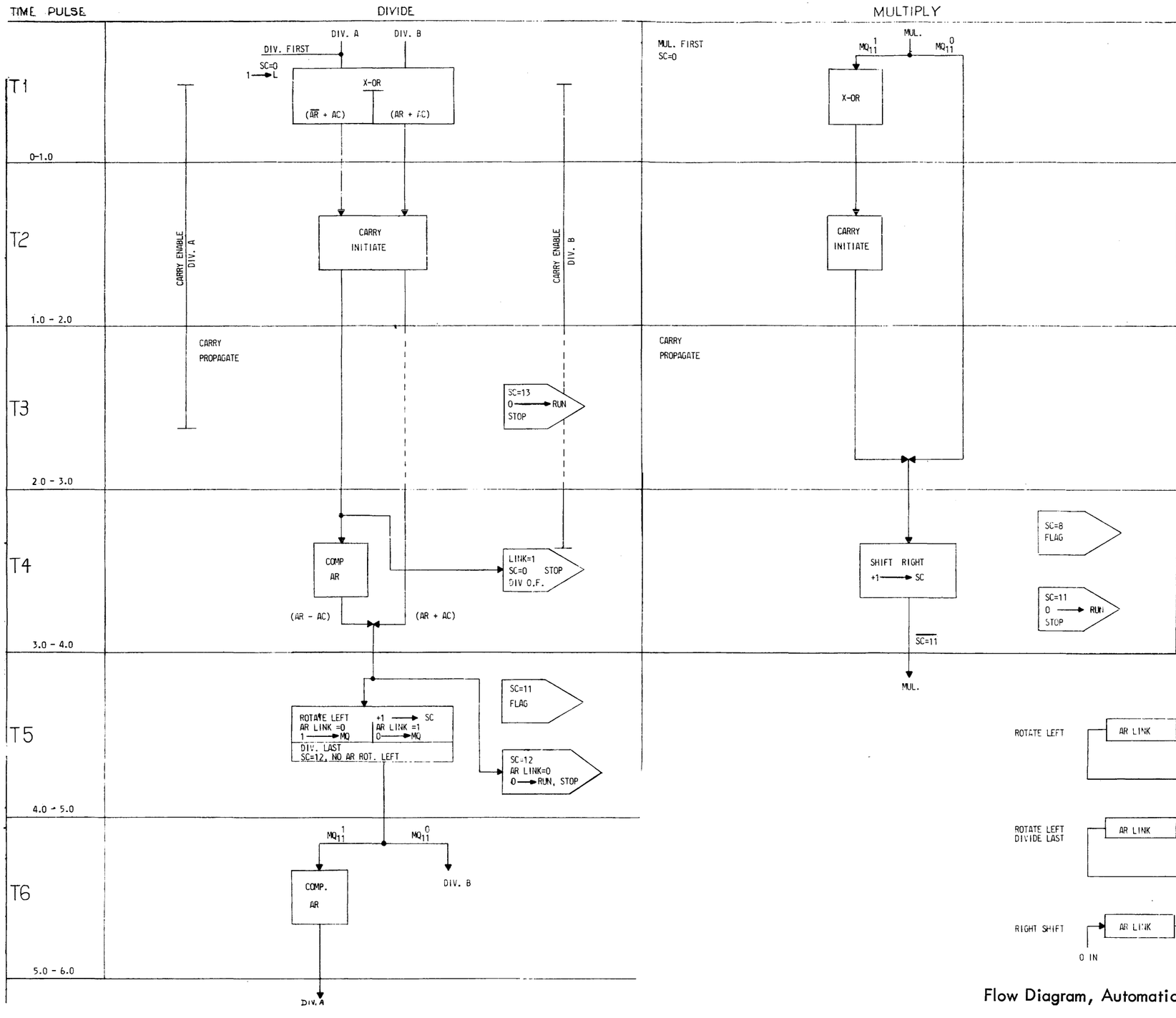


NOTE
1. PLUGS ILO1+ILO2 ARE BUSSED TOGETHER.



NOTE
1 PLUGS ILO1+ILO2 ARE BUSSED TOGETHER.

AR Register BS-D-153-0-7



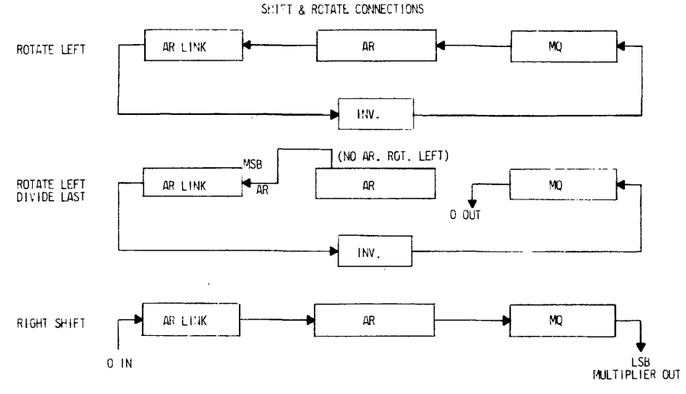
SET UP CONDITIONS

DIVIDE

AR = DIVIDEND 0-11
MQ = DIVIDEND 12-23
AC = DIVISOR 0-11
L ≙ 1

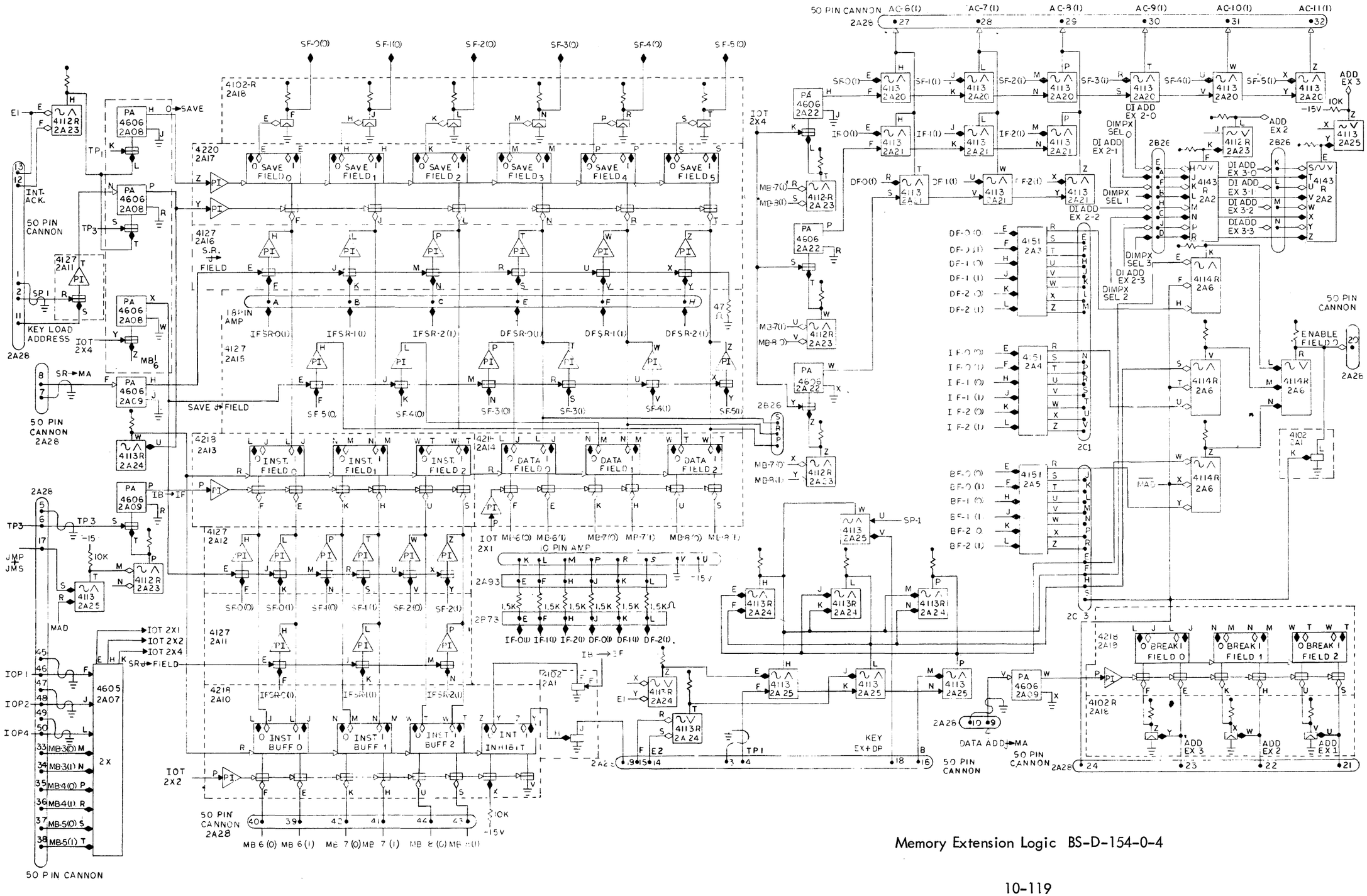
MULTIPLY

AR = 0
MQ = MULTIPLIER 0-11
AC = MULTIPLICAN 0-11



Flow Diagram, Automatic Multiply and Divide FD-D-153-0-11

Check with multiplexer
129



Memory Extension Logic BS-D-154-0-4

NOTE: * INSTALL ONLY WITH 4K MEMORY

1A

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
	PULSE AMPLIFIER 1607	DELAY LINE 1310	MEMORY DRIVER 1989	MEMORY DRIVER 1989	READ-WRITE SWITCH 1987						READ-WRITE SWITCH 1987	RESISTOR BOARD 1976	RESISTOR BOARD 1976	MEMORY STACK											MEMORY STACK

1B

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
	22 PIN PLUG ADAPTER 4801	TRIPLE FLIP-FLOP 4706										TRIPLE FLIP-FLOP 4206	22 PIN PLUG ADAPTOR4802	DUAL SENSE AMP. 4554						DUAL SENSE AMP. 4554	INH1811 DRIVER 1982	INH1811 DRIVER 1982	INH1811 DRIVER 1982	RESISTOR BOARD 1978	RESISTOR BOARD 1978

1C

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
PULSE AMPLIFIER 4606	PULSE AMPLIFIER 4606	PULSE AMPLIFIER 4606	PULSE INVERTER 4129R	PULSE INVERTER 4122R	DIODE 1011	DIODE 1011	POS.DIODE NOR 4115R	NEG. DIODE NOR 4112R	POS. DIODE NOR 4113	POS. DIODE NOR 4113R	PULSE AMPLIFIER 4603	PULSE AMPLIFIER 4603	PULSE AMPLIFIER 4606	PULSE AMPLIFIER 4606	INVERTER 4102R	POS. DIODE NOR 4113R	POS. DIODE NOR 4115R	INVERTER 6102R	DELAY LINE 1311	PULSE INVERTER 4122R	4-BIT COUNTER 4215	PULSE AMPLIFIER 4606	PULSE AMPLIFIER 4604	CRYSTAL CLOCK 1406

1D

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
4-BIT COUNTER 4215	POS.DIODE NOR 4113R	4-BIT COUNTER 4215	NEG.DIODE NOR 4114R	POSITIVE DIODE NOR 4115	INVERTER 4102	DIODE 4111	DIODE 4111	INVERTER 4106R	POS. DIODE NOR 4115R	NEG. DIODE NOR 4114R	DIODE 4116	POS. DIODE NOR 4113	POS. DIODE NOR 4115R	POS. DIODE NOR 4113R	NEG. DIODE NOR 4112R	PULSE INVERTER 4127	POS. DIODE NOR 4117R	POS. DIODE NOR 4112R	INVERTER 4102R	BINARY-TO-OCT-DEC. 1151	4-BIT COUNTER 4215	PULSE INVERTER 4127	PULSE INVERTER 4127	PULSE AMPLIFIER 4606

1E

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
POS.CAP.DIODE GATE 4130R	PULSE INVERTER 4129	NEG. DIODE NOR 4112R	INVERTER 4102R	VARIABLE CLOCK 4401	PULSE GENERATOR 4410	DELAY (ONE SHOT) 4301	PULSE AMPLIFIER 4604	DIODE 4113	POS.CAP.DIODE GATE 4130R					POS.CAP.DIODE GATE 4130R	LOAD RESISTORS 1000	PULSE AMPLIFIER 4606	1:1 FEGRATING SNGL SHOT4303	LEVEL AMPLIFIER 4678	LEVEL AMPLIFIER 4678	LEVEL AMPLIFIER 4678	12-BIT DAC 1574	10V PREC. PWR SUP. 1704	DIFFERENCE AMPLIFIER1572	

NOTE: O INSTALL ONLY WITH A-D CONVERTER OPTIONS

NOTE. INSTALLED ONLY WITH BUFFERED OUTPUT OPTION.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
					BUS DRIVER 1685	BUS DRIVER 1685	BUS DRIVER 1685	BUS DRIVER 1684	BUS DRIVER 1684	BUS DRIVER 1684	BUS DRIVER 1684	BUS DRIVER 1684					PULSE AMP 4605	PULSE AMP 4605	PULSE AMP 4605	RELAY 1907	CRYSTAL CLOCK 4407	3 BIT BCD CH. COUNTER 4225	TELETYPE TXCOMTNG LINE UNIT 4706	TELETYPE TRANSMITTER 4702

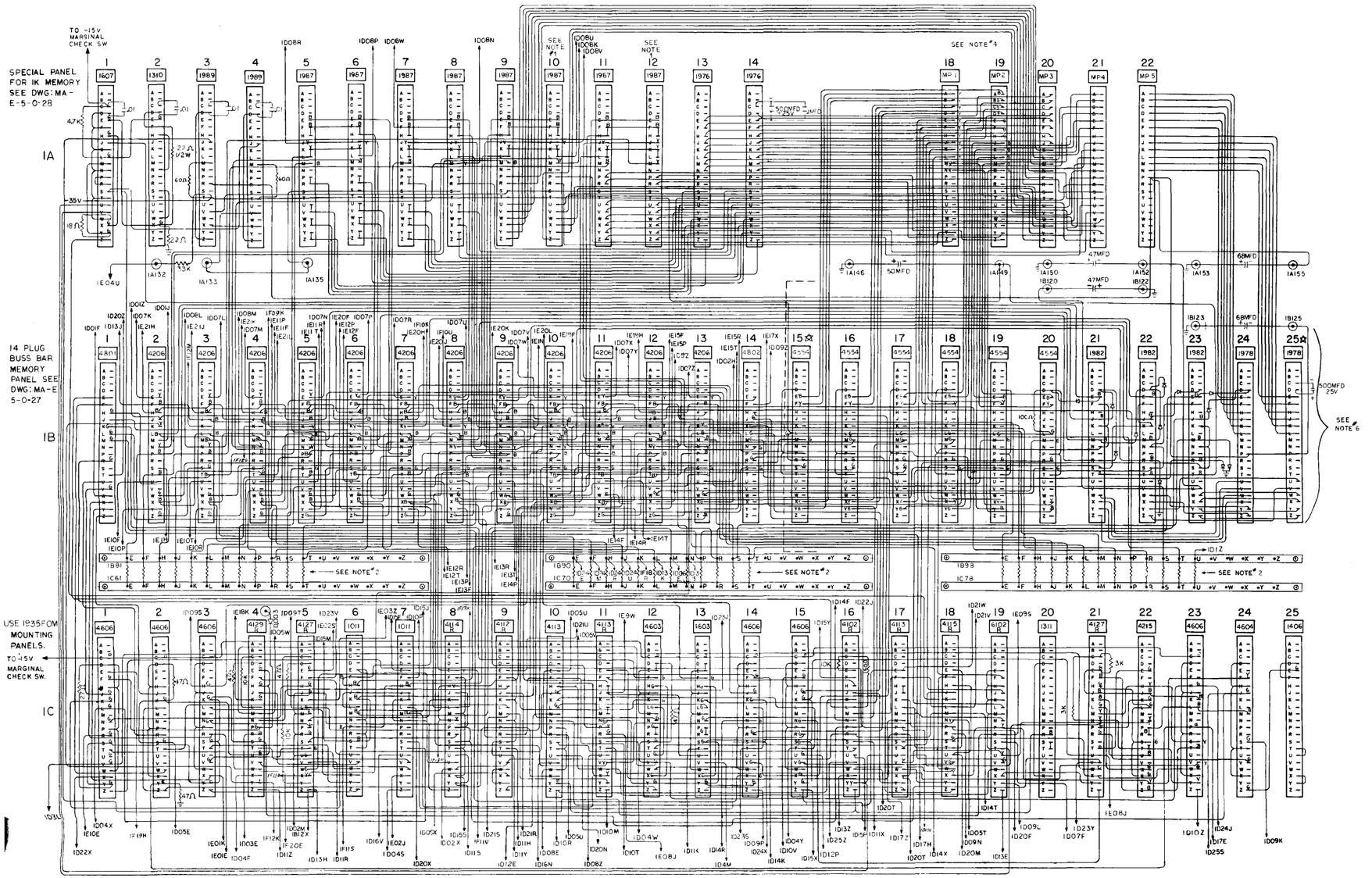
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25

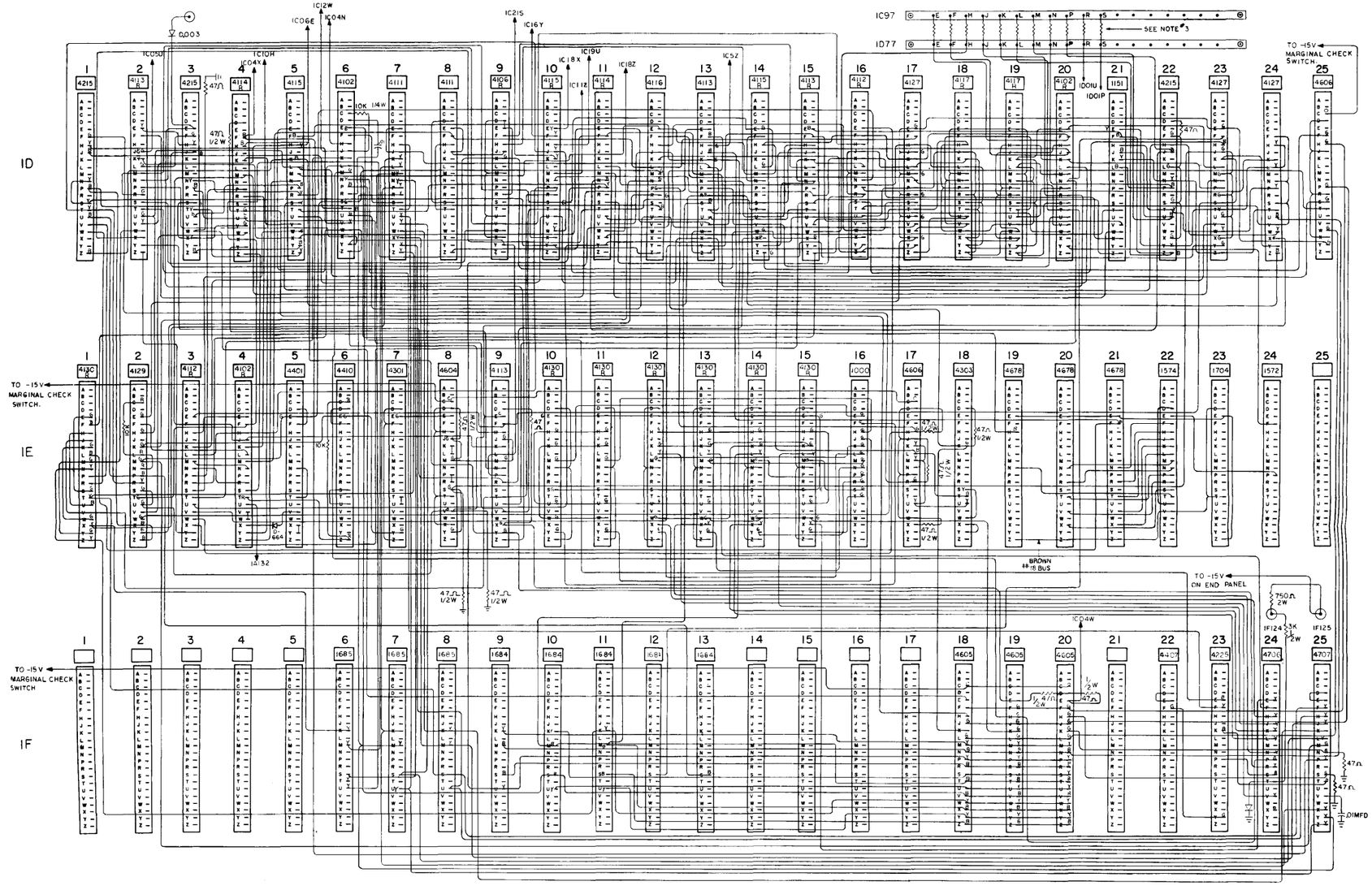
System Module Location ML-D-5-0-15



NOTES:

1. IF 1K MEMORY IS USED, REMOVE PACKAGES 1927 1A10 AND 1987 1A12.
2. ALL RESISTORS LOCATED ON STANDOFF-BOARDS ARE 3.3K.
3. UNLESS OTHERWISE INDICATED ALL DIODES ARE D-003.
4. 1A18A-N AND 1A19-N ARE YEL/BLK TW. PR.
5. SEE DRAWING B-5-0-30 FOR SPECIAL MARGINAL CHECKING PANEL FOR 1B.
6. DO NOT RUN ANY WIRES ACROSS 1B15 THRU 1B25 UNLESS IT'S GOING TO A PIN LOCATION ON ONE OF THOSE PLUGS.

Wiring Diagram 1A, 1B, 1C WD-E-5-0-3

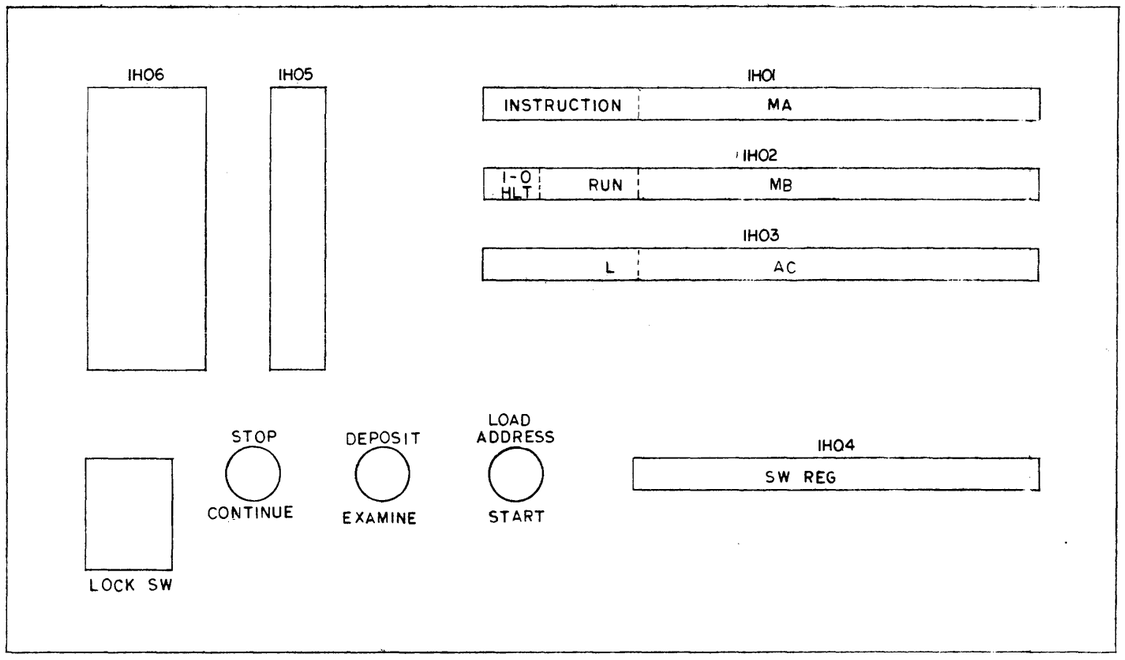


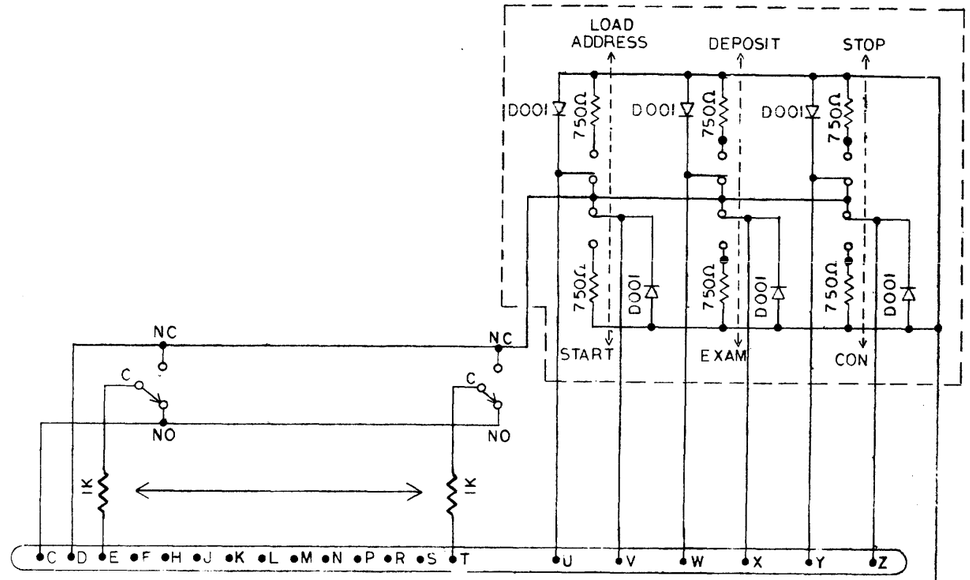
NOTES:

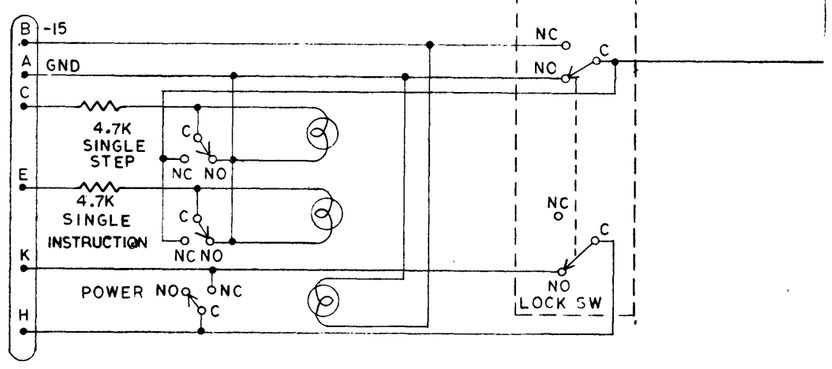
1. USE 1935FOM MOUNTING PANELS.
2. UNLESS OTHERWISE INDICATED ALL CAPACITORS LOCATED ON STANDOFF-BOARD ARE 6.8MFD 35V.
3. ALL RESISTORS LOCATED ON STANDOFF-BOARD ARE 3.3k

Wiring Diagram 1D, 1E, 1F WD-E-5-0-4

REAR VIEW

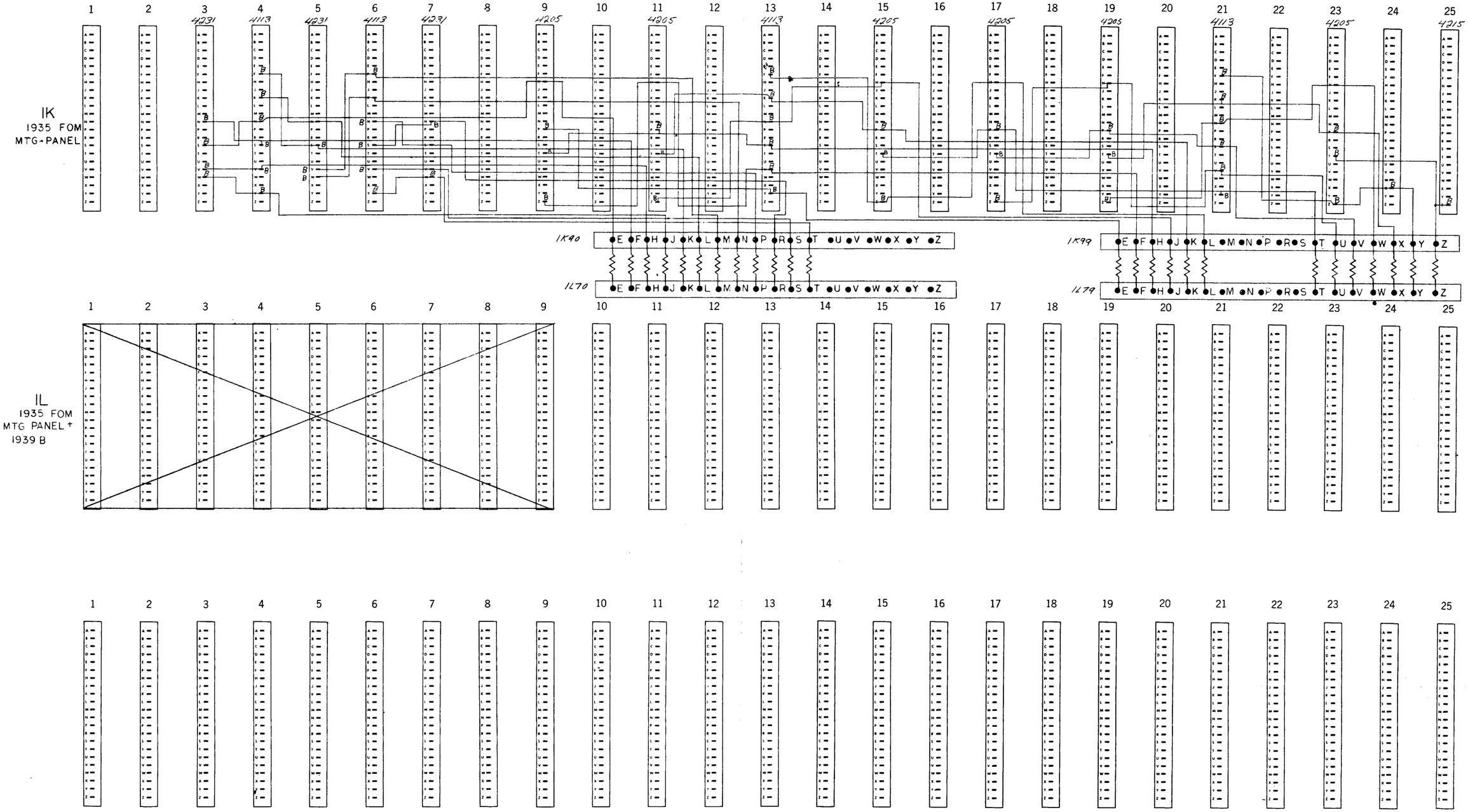






Operator Control Keys and Switches WD-D-5-0-10

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
			4231	4113	4233	4	4234	4123	4235	4123R	4125	4102R	4113	4131	4207	4123R	4205	4123R	4206	4115	4115	4123	4205	4123R	4215
1K			MQ 0-3	MQ→AC 0-5	MQ 4-7	MQ→AC 6-11	MQ 8-11	COMP AR$_{10}$ COMP AR$_{11}$	AR 10-11	COMP AR$_8$ COMP AR$_9$	AR 8-9	AC 3 AC 4 AC 5 AC 6 AC 7 AC 8 AC 9 AC 10 AC 11	AR→AC 6-11	COMP AR$_6$ COMP AR$_7$	AR 6-7	COMP AR$_4$ COMP AR$_5$	AR 4-5	COMP AR$_2$ COMP AR$_3$	AR 2-3	AC$_0$ AC$_1$ AC$_2$ MUL DIV DIV MUL AR SHIFT CARRY ENB	AR→AC 0-5	COMP AR$_0$ COMP AR$_1$	AR 0-1	AR LINK	DIV OVERFLO CONTROL RUN^0 AR LINK
			4605	4605	4605					4605	4605	4605		4102	4604	4606	4606	4113R	4218	4606	4215	4115R	4113	4114R	4127
1L										REG CLR MC→AQ AC→AR	MUL GO AR→AC SZO	DIV MR→AC SAF		CONTROL POWER CLR AR SHIFT CARRY ENB CLEAR AC X OR POWER CLR X OR	AR ROTATE LEFT CONTROL CLEAR CLEAR AR	L+AR COMP (T4-T6) L+MQ ROTATE LEFT (T-5) L+MQ SHIFT RIGHT (T-4)	X OR (T-1) CARRY INITATE (T-2) READ PULSE TG$_{0-2}$	FLAG$_1$ COMP (T4-T6) TG$_0$ CARRY ENABLE X OR (T-1) POWER CLR	TG$_2$ TG$_1$ TG$_0$ FLAG	TGP$^0_1$ TGP$^0_2$ TGP$^0_0$	SC$_0$ SC$_1$ SC$_2$ SC$_3$	SCD-0 FLAG$_1$ SCD-12 SCD-12 FLAG$_L$	-SKIP- DIV CD-12 TG$_0$ TG$_0$	RUN FF DIV-OVERFLO	RUN$_0$ FLAG$_0$ DIV OVERFLOW AR ROT



NOTE: ALL RESISTORS ARE 3.3K

Wiring Diagram 1K and 1L (Sheet 1) WD-D-153-0-4

1K
1935 FOM
MTG. PANEL

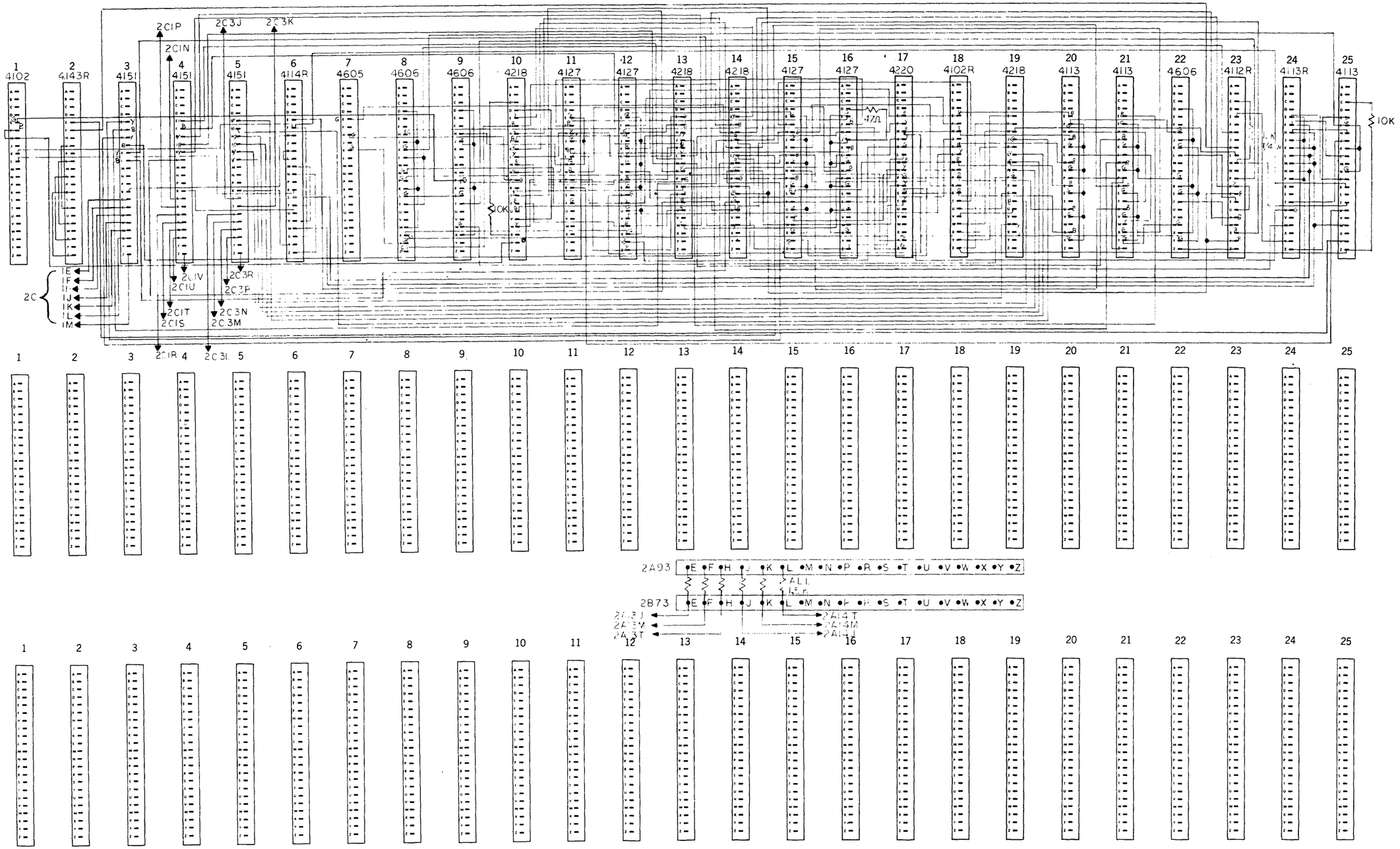
1L
1935 FOM
MTG. PANEL +
19398

Wiring Diagram 1K and 1L (Sheet 2) WD-D-153-0-4

2A

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
4102	4143	4151	4151	4151	4114R	4605	4606	4606	4218	4127	4127	4218	4218	4217	4217	4220	4102R	4218	4113		4606	4112R	4113R	4113
INT. INHIBIT (0)					SELECT D. F. 0		0→SAVE	SR→FIELD	INST BUFF$_0$			INST FIELD$_0$	DATA FIELD$_0$			SAVE FIELD 0	SF-0 (0)	BREAK FIELD$_0$	SF$_0$→AC$_6$(1)	IF$_0$→AC$_6$(1)		INT. ACK	IF ENABLE	IF ENABLE
INT. INHIBIT (1)										SR→						1	SF-1 (0)		SF$_1$→AC$_7$(1)	IF$_1$→AC$_7$(1)		ADD EX 2	DF ENABLE	DF ENABLE
ENABLE FIELD	ADD EX 2				SELECT IF 0		IF→SF	IB→IF	INST BUFF$_1$	INST FIELD	SAVE→ INST FIELD	INST FIELD$_1$	DATA FIELD$_1$	SAVE→ DATA FIELD	SR→ SAVE FIELD	2	SF-2 (0)	BREAK FIELD$_1$	SF$_2$→AC$_8$(1)	IF$_2$→AC$_8$(1)		P JUMP JMS	BF ENABLE	BF ENABLE
		DECODER DF	DECODER IF	DECODER BF		IOT 2X				LOAD IF→SF						3	SF-3 (0)							
					ENABLE FIELD 0				INST BUFF$_2$			INST FIELD$_2$	DATA FIELD$_2$			4	SF-4 (0)		SF$_3$→AC$_9$(1)	DF$_0$→AC$_9$(1)		IOT 234	DF ENABLE	ENABLE FIELD$_0$
																SAVE FIELD 5	SF-5 (0)	BREAK FIELD$_2$			IOT 2X4			
	ADD EX 3						SAVE→ FIELD	DATA ADD→MA									SET BF$_0$		SF$_4$→AC$_{10}$(1)	DF$_1$→AC$_{10}$(1)		IOT 224	CLEAR IF	CLEAR ENABLE FIELD
					SELECT B. F. 0				INT. INHIBIT								SET BF$_1$							
																	SET BF$_2$		SF$_5$→AC$_{11}$(1)	DF$_2$→AC$_{11}$(1)		IOT 214	E1	ADD EX 3

2A
1 OF 2



Wiring Diagram for Type 154 WD-D-154-0-5