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IDENTIFICATION

PRODUCT CODE: AC-E667J-MC
PRODUCT NAME: CXCPBJO EIS EXER MOD
PRODUCT DATE: SEPTEMBER 1978
MAINTAINER: DEC/X11 SUPPORT GROUP

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1. ABSTRACT:

CPB IS A BKMOD THAT EXERCISES THE EIS IN THE PDP11/45
AND THE PDP11/40.

2. REQUIREMENTS:

HARDWARE: ANY PDP11/45 OR PDP11/40 WITH EIS OPTION.
STORAGE:: CPB REQUIRES:
1. DECIMAL WORDS: 471
2. OCTAL WORDS: 0727
3. OCTAL BYTES: 1656

3. PASS DEFINITION:

ONE PASS OF THE CPB MODULE CONSISTS OF EXECUTING EACH
INSTRUCTION 12500 TIMES.

4. EXECUTION TIME:

CPB RUNNING ALONE ON A PDP11/45 TAKES APPROXIMATELY
30 SECONDS.

5. CONFIGURATION REQUIREMENTS:

11/40 OR LSI WITHOUT EIS OPTION, SEE SECTION 8.

6. DEVICE/OPTION SETUP:

MAKE SURE EIS IS INSTALLED.

7. MODULE OPERATION:

- A. SETUP CYCLE COUNTER.
- B. TEST ALL EIS INSTRUCTIONS UNLESS SRI BIT#1 = 1.
IF SRI BIT#1 = 1, CHECK ONLY XOR, SOB, MARK, SXT, AND RTT.
- C. IF NOT EOP, GO TO B.
- D. ELSE DO EOP AND GO TO A.

8. OPERATING OPTIONS:

SRI

BIT #0=0 DO ALL EIS INSTRUCTIONS
BIT #0=1 11/40, LSI WITHOUT EIS (11V03)
DO ONLY XOR, SOB, MARK, SXT, AND RTT.
BIT #2=0 ACCESS PROCESSOR STATUS DIRECTLY.
BIT #2=1 USE MFPS INSTRUCTION.

I.E.
SRI=0 ALL EIS, PSW DIRECT.
SRI=1 NO EIS, PSW DIRECT.
SRI=4 ALL EIS, USE MFPS
SRI=5 NO EIS, USE MFPS.

9. NON-STANDARD PRINTOUTS:

NONE

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000000* -
000000*   MODUL BKMOD <CPBJ > 12500,2
          ;   40020,CPBJ 12500,2
          ;   .TITLE CPBJ DEC/X11 SYSTEM EXERCISER MODULE
          ;   DDSCOM VERSION 6 23-MAY-78
          ;*****
000000*   .LIST BIN
000000*   BGIN:
000000* 050103 045102 040 ;ASCII /CPBJ / ;MODULE NAME.
000005* 000 ;BYTE OPEN ;USFD TO KEEP TRACK OF WBUF USAGE
000006* 000000 ;ADDR: +0 ;1ST DEVICE ADDR.
000010* 000000 ;VECTOR: +0 ;1ST DEVICE VECTOR.
000012* 000 ;BR1: .RYTE PRTY+0 ;1ST BR LEVEL.
000013* 000 ;BR2: .BYTE PRTY+0 ;2ND BR LEVEL.
000014* 000001 ;DVI01: +1 ;DEVICE INDICATOR 1.
000016* 000000 ;SR1: OPEN ;SWITCH REGISTER 1.
000020* 000000 ;SR2: OPEN ;SWITCH REGISTER 2.
000022* 000000 ;SR3: OPEN ;SWITCH REGISTER 3.
000024* 000000 ;SR4: OPEN ;SWITCH REGISTER 4.
          ;*****
000026* 040020 ;STAT: 40020 ;STATUS WORD.
000030* 000224 ;MODNAM: START ;MODULE START ADDR.
000032* 000224 ;SPOINT: MODSP ;MODULE STACK POINTER.
000034* 000000 ;PASCNT: 0 ;PASS COUNTER.
000036* 012500 ;ICONT: 12500 ;# OF ITERATIONS PER PASS=12500
000040* 000000 ;SOFcnt: 0 ;LOC TO COUNT ITERATIONS
000042* 000000 ;HRDCNT: 0 ;LOC TO SAVE TOTAL SOFT ERRORS
000044* 000000 ;SOPPAS: 0 ;LOC TO SAVE TOTAL HARD ERRORS
000046* 000000 ;HRDPAS: 0 ;LOC TO SAVE SOFT ERRORS PER PASS
000050* 000000 ;SYSCNT: 0 ;LOC TO SAVE HARD ERRORS PER PASS
000052* 000000 ;RANUM: 0 ;# OF SYS ERRORS ACCUMULATED
000054* 000000 ;CONFIG: ;HOLDS RANDOM # WHEN RAND MACRO IS CALLED
000056* 000000 ;RES1: 0 ;RESERVED FOR MONITOR USE
000060* 000000 ;RES2: 0 ;RESERVED FOR MONITOR USE
000062* 000000 ;SVR0: OPEN ;LOC TO SAVE R0.
000064* 000000 ;SVR1: OPEN ;LOC TO SAVE R1.
000066* 000000 ;SVR2: OPEN ;LOC TO SAVE R2.
000070* 000000 ;SVR3: OPEN ;LOC TO SAVE R3.
000072* 000000 ;SVR4: OPEN ;LOC TO SAVE R4.
000074* 000000 ;SVR5: OPEN ;LOC TO SAVE R5.
000076* 000000 ;SVR6: OPEN ;LOC TO SAVE R6.
001000* 000000 ;CSR: OPEN ;ADDR OF CURRENT CSR.
001002* 000000 ;SPADR: ;ADDR OF GOOD DATA, OP
001004* 000000 ;ACSR: OPEN ;CONTENTS OF CSR.
001006* 000000 ;WASADR: ;ADDR OF BAD DATA, OR
001008* 000000 ;ASTAT: OPEN ;STATUS REG CONTENTS.
001010* 000000 ;ERRTYP: ;TYPE OF ERROR
001012* 000000 ;ASB: OPEN ;EXPECTED DATA.
001014* 000000 ;AWAS: OPEN ;ACTUAL DATA.
001016* 000224 ;RSTRT: RSTRT ;RESTART ADDRFS AFTER END OF PASS
001018* 000000 ;WDT0: OPEN ;WORDS TO MEMORY PER ITERATION
001020* 000000 ;WDFR: OPEN ;WORDS FROM MEMORY PER ITERATION
001022* 000000 ;INTR: OPEN ;# OF INTERRUPTS PER ITERATION
001024* 000040 ;IDNUM: 2 ;MODULE IDENTIFICATION NUMBER=2
          ; .REPT SPSIZ ;MODULE STACK STARTS HERE.

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```

000224*   .NLIST
          ; .WORD 0
          ; .LIST
          ; .ENDR
000224*   MODSP:
          ;*****

```

```

173 000224*
174 000224*
175 000224*
176 000224*
177 000224* 104413 000000*
178
179
180 000230* 012702 000010
181 000234* 012701 052525
182 000240* 012767 177777 001342
183 000246* 074162 001600*
184 000252* 022767 125252 001330
185 000252* 001403
186 000262*
187
188
189 000262* 104405 000000* 000000
190
191
192 000
193
194
195
196
197
198 000270* 012703 125252
199 000274* 012704 000010
200 000300* 012767 001624* 001330
201 000306* 012767 177777 001310
202 000314* 074162 001626*
203 000320* 022767 052525 001276
204 000326* 001403
205 000330*
206
207 000330* 104405 000000* 000000
208
209
210 000
211
212
213
214
215 000336* 000401
216 000340* 000406
217 000342* 012701 000010
218 000346* 077104
219 000350*
220
221
222 000350* 104405 000000* 000000
223
224
225 000
226
227
228

```

```

START:
RFSTRT:
ENDIT
ENDITS,BEGIN
;SIGNAL END OF ITERATION.
;MONITOR SHALL TEST END OF PASS
XOR1: MOV #10,R2 ;SET NP INDEX REGISTER
MOV #52525,R1 ;LOAD SOURCE OPERAND
MOV #-1,TEMP ;LOAD DESTINATION OPERAND
XOR R1,C(R2) ;XOR SOURCE,DFST.
CMP #125252,TEMP
BEQ 15
HRDR / ***** <XOR INSTRUCTION FAILED> *****
;*****
-IF B <>
HRDRS,BEGIN,NULL ;XOR INSTRUCTION FAILED
-IFP
HRDRS,BEGIN, ;XOR INSTRUCTION FAILED
-ENDC
;*****
;SBTTL TEST XOR USING INDEX DEFERRFD
1S: MOV #125252,R3
MOV #10,R4
MOV #Y,X+10
MOV #-1,Y
XOR R3,8X(R4)
CMP #52525,Y
BEQ 25
HRDR / ***** <XOR -1,125252 FAILED> *****
;*****
-IF B <>
HRDRS,BEGIN,NULL ;XOR -1,125252 FAILED
-IFP
HRDRS,BEGIN, ;XOR -1,125252 FAILED
-ENDC
;*****
;SBTTL TEST SOB FOR BRANCH
2S: BR SOB1
SOB2: BR SOB3
SOB1: MOV #10,R1
SOB : R1,SOR2
HRDR / ***** <SOB SHOULD HAVE BRANCHED> *****
;*****
-IF B <>
HRDRS,BEGIN,NULL ;SOB SHOULD HAVE BRANCHED
-IFP
HRDRS,BEGIN, ;SOB SHOULD HAVE BRANCHED
-ENDC
;*****
;SBTTL TEST SOB FOR NO BRANCH

```

```

229
230 000356* 000404
231 000360*
232
233 000360* 104405 000000* 000000
234
235
236 000
237
238
239 000366* 000403
240 000370* 012701 000001
241 000374* 077107
242
243
244
245
246
247
248 000376* 016706 177430
249 000402* 005001
250 000404* 012746 000007
251 000410* 012746 000001
252 000414* 012746 006401
253 000420* 018605
254 000422* 004767 000002
255 000426* 000403
256 000430* 016501 000002
257 000434* 000205
258 000436* 022701 000001
259 000442* 001403
260 000444*
261
262 000444* 104405 000000* 000000
263
264 000
265
266 000452* 026706 177354
267 000456* 001403
268 000460*
269
270
271 000460* 104405 000000* 000000
272
273 000
274
275
276 000466* 022705 000007
277 000472* 001403
278 000474*
279
280 000474* 104405 000000* 000000
281
282
283
284 000

```

```

SOB3: BR SOB4
SOB5:
;*****
-IF B <>
HRDRS,BEGIN,NULL ;SOB SHOULD NOT HAVE BRANCHED
-IFP
HRDRS,BEGIN, ;SOB SHOULD NOT HAVE BRANCHED
-ENDC
;*****
SOB4: BR MA
MOV #1,R1
SOB : R1,SORS
;SBTTL TEST MARK INSTRUCTION
MA: MOV SPOINT,SP ;INITIALIZE STACK POINTER
CLR R1
MOV #,-(SP)
MOV #1,-(SP) ;PUSH A PARAMETER ON THE STACK
MOV #MARK1,-(SP) ;PUSH MARK 1 ON THE STACK
MOV SP,R5 ;LOAD PARAMETER POINTER
JSR PC,MARKO ;GO TO SUBROUTINE
BR MARKOA
MARKO: MOV 2(R5),R1 ;GET THE PARAMETER
RTS R5 ;EXIT SUBROUTINE
MARKOA: CMP #1,R1 ;DID SUBROUTINE GET THE PARAMETER
BEQ 15
HRDR / ***** <SUBROUTINE DID NOT GET PUSHED PARAMETER> *****
;*****
-IF B <>
HRDRS,BEGIN,NULL ;SUBROUTINE DID NOT GET PUSHED PARAMETER
-IFP
HRDRS,BEGIN, ;SUBROUTINE DID NOT GET PUSHED PARAMETER
-ENDC
;*****
1S: CMP SPOINT,SP ;IS STACK POINTER CORRECT?
BEQ 25
HRDR / ***** <STACK POINTER INCORRECT FOR MARK> *****
;*****
-IF B <>
HRDRS,BEGIN,NULL ;STACK POINTER INCORRECT FOR MARK
-IFP
HRDRS,BEGIN, ;STACK POINTER INCORRECT FOR MARK
-ENDC
;*****
2S: CMP #7,R5 ;IS R5 CORRECT?
BEQ 35
HRDR / ***** <MARK DID NOT LOAD R5> *****
;*****
-IF B <>
HRDRS,BEGIN,NULL ;MARK DID NOT LOAD R5
-IFP
HRDRS,BEGIN, ;MARK DID NOT LOAD R5
-ENDC

```

```

285 ;*****
286 ;
287 ;SBTTL TEST THE SXT INSTRUCTION
288
289 000502* 012702 000010 001074 3S: MOV #10,R2 ;SET UP INDFX REGISTER
290 000506* 012767 177777 001074 MOV #-1,TEMP
291 000514* 000257 000000 000000 CCC ;CLEAR ALL CONDITION CODES
292 000516* 006762 001600* SXT C(R2) ;EXTEND 0'S INTO TEMP [C(R2)]
293 000522* 005767 001062 TST TEMP
294 000526* 001403 BEQ 4S
295 000530* HRDPR <0'S DOID NOT EXTEND INTO TEMP>
296 ;*****
297 ;
298 000530* 104405 000000* 000000 ;IF B <>
299 HRDPRS,BEGIN,NULL ;0'S DOID NOT EXTEND INTO TEMP
300 ;IFB
301 HRDPRS,BEGIN, ;0'S DOID NOT EXTEND INTO TEMP
302 ;ENDC
303 ;*****
304 000536* 005067 001046 4S: CLR TEMP
305 000542* 000277 SCC ;SET ALL CONDITION CODES
306 000544* 006767 001040 SXT TEMP ;EXTEND 1'S INTO TEMP
307 000550* 022767 177777 001032 CMP #-1,TEMP
308 000556* 001403 BEQ 5S
309 000560* HRDPR <-1 DID NOT EXTEND INTO TEMP>
310 ;*****
311 ;
312 000560* 104405 000000* 000000 ;IF B <>
313 HRDPRS,BEGIN,NULL ;-1 DID NOT EXTEND INTO TEMP
314 ;IFB
315 HRDPRS,BEGIN, ;-1 DID NOT EXTEND INTO TEMP
316 ;ENDC
317 ;*****
318 ;SBTTL TEST THE RTT INSTRUCTION
319
320 000566* 016706 177240 177216 5S: MOV SPOINT,SP ;RESET THE STACK POINTER
321 000572* 032767 000004 BIT #4,SRI ;ACCESS PSH DIRECT?
322 000600* 001403 BEQ 6S ;YES
323 000602* 000257 CCC ;CLEAR STATUS
324 000604* 106746 MPPS -(SP) ;PUSH ON STACK FOR RTT
325 000606* 000403 BR 7S ;SET UP PC FOR RTT
326 000610* 000257 CCC ;CLR COND CODES
327 000612* 016746 177776 MOV PS,-(SP) ;PUSH IT ON STACK AS PS FOR RTT
328 000616* 012746 000642* 7S: MOV #RTTA,-(SP) ;PUSH RETURN PC ONTO STACK
329 000624* 000277 SCC ;INSURE N=Z=V=C=1 BEFORE RTT
330 000626* 000006 RTT <RTT FAILED>
331 ;*****
332 ;
333 000626* 104405 000000* 000000 ;IF B <>
334 HRDPRS,BEGIN,NULL ;RTT FAILED
335 ;IFB
336 HRDPRS,BEGIN, ;RTT FAILFD
337 ;ENDC
338 ;*****
339 000634* 005726 TST (SP)+ ;POP STACK
340 000636* 005726 TST (SP)+ ;POP STACK

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341 000640* 000407 RTTA: BR RTTR ;GO ON WITH TEST
342 000642* 000403 BMI 10S ;IF N SET,REPORT ERROR
343 000644* 100403 BLOS 10S ;IF C OR Z SET,REPORT ERROR
344 000646* 102401 BVS 10S ;IF V SET,REPORT ERROR
345 000650* 000403 BR RTTR ;IF YES GO ON WITH TEST
346 000652* HRDPR <INCORRECT STATUS>
347 ;*****
348 ;
349 000652* 104405 000000* 000000 ;IF B <>
350 HRDPRS,BEGIN,NULL ;INCORRECT STATUS
351 ;IFB
352 HRDPRS,BEGIN, ;INCORRECT STATUS
353 ;ENDC
354 ;*****
355 000660* 032767 000001 177130 RTTB: BIT #1,SRI
356 000666* 001402 BEQ MUL1
357 000670* 000167 177330 JMP START
358 ;*****
359 ;
360 000674* 005003 MUL1: CLR R3 ;CLEAR R3
361 000676* 012702 MOV #5,R2 ;LOAD MULTIPICAND
362 000702* 005067 000746 CLR PLIER ;LOAD MULTIPLIER
363 000706* 012767 000002 000740 MOV #2,PLIER ;PRESET CONDITION CODES
364 000714* 000277 SCC ;MULTIPLY 2X5 RESULT IN R2 (MSH);R3 (LSH)
365 000716* 070267 000732 MUL PLIER,R2 ;IF N SET,REPORT ERROR
366 000722* 100402 BMI 10S ;IF C OR Z SET,REPORT ERROR
367 000724* 101401 BLOS 10S ;IF V = 0,GO ON WITH TEST
368 000726* 102003 BVC 1S
369 000730* HRDPR <CC'S NOT = TO 0'S>
370 000730* ;*****
371 ;
372 000730* 104405 000000* 000000 ;IF B <>
373 HRDPRS,BEGIN,NULL ;CC'S NOT = TO 0'S
374 ;IFB
375 HRDPRS,BEGIN, ;CC'S NOT = TO 0'S
376 ;ENDC
377 ;*****
378 000736* 022703 000012 1S: CMP #12,R3 ;RESULT =12?
379 000742* 001403 BEQ 2S ;BRANCH IF THE RESULT (LSH) IS CORRECT
380 000744* HRDPR <INCORRECT RESULT (LSH)>
381 ;*****
382 ;
383 000744* 104405 000000* 000000 ;IF B <>
384 HRDPRS,BEGIN,NULL ;INCORRECT RESULT (LSH)
385 ;IFB
386 HRDPRS,BEGIN, ;INCORRECT RESULT (LSH)
387 ;ENDC
388 ;*****
389 000752* 005702 2S: TST R2 ;CORRECT RESULT (MSH)?
390 000754* 001403 BEQ MUL2
391 000756* HRDPR <INCORRECT RESULT (MSH)>
392 ;*****
393 ;
394 000756* 104405 000000* 000000 ;IF B <>
395 HRDPRS,BEGIN,NULL ;INCORRECT RESULT (MSH)
396 ;IFB
397 HRDPRS,BEGIN, ;INCORRECT RESULT (MSH)

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```

397          000          ;FNDC
398          ;*****
399
400
401 000764- 005003      MUL2: CLR      R3
402 000765- 005067      CLR      PLIER
403 000770- 012702      MOV      #125252,R2 ;LOAD MULTIPICAND
404 000772- 012767      MOV      #2,PLIER
405 001004- 070267      MUL      PLIER,R2 ;MULTIPLY 2X125252 RESULT=-1(R2)
406                                     ;52524(R3),N=1,Z=0,V=0,C=1
407 001010- 103003      JCC     10$ ;IF C = 0,REPORT ERROR
408 001012- 100002      BPL     10$ ;IF N = 0,REPORT ERROR
409 001014- 102401      BVS     10$ ;IF V SET,REPORT ERROR
410 001016- 001003      BNE     1$ ;IF Z = 0,GO ON WITH TEST
411 001020-
412 001020- 10$: HRDR   < <INCORRECT CONDITION CODES>
413          ;*****
414          ;IF B <>
415 001020- 104405      HRDRS,BEGIN,NULL ;INCORRECT CONDITTON CODES
416          ;IF
417 HRDRS,BEGIN, ;INCORRECT CONDITION CODES
418          ;FNDC
419          ;*****
420 001026- 022702      1$: CMP      #-1,R? ;CORRECT MSH RESULT?
421 001032- 001403      BQO     2$
422 001034-
423          HRDR   < <INCORRECT MSH RESULT>
424          ;*****
425 001034- 104405      ;IF B <>
426 HRDRS,BEGIN,NULL ;INCORRECT MSH RESULT
427          ;IF
428 HRDRS,BEGIN, ;INCORRECT MSH RESULT
429          ;FNDC
430          ;*****
431 001042- 022703      2$: CMP      #52524,R3 ;CORRECT LSH RESULT?
432 001046- 001403      BQO     ASH1
433 001050-
434          HRDR   < <INCORRECT LSH RESULT>
435          ;*****
436 001050- 104405      ;IF B <>
437 HRDRS,BEGIN,NULL ;INCORRECT LSH RESULT
438          ;IF
439 HRDRS,BEGIN, ;INCORRECT LSH RESULT
440          ;FNDC
441          ;*****
442          ;SBTTL TEST ASH INSTRUCTION
443          ASH1: CLR      PLIER
444 001062- 005067      MOV      #1,PLIER ;LOAD SHIFT VALUE (+1 OR 1 PLACE LEFT)
445 001070- 012767      MOV      #125252,R2 ;GET VALUE TO BE SHIFED (#125252)
446 001074- 000257      CCC     ;PRE-CLEAR ALL CC BITS
447 001076- 000264      SEZ     ;PRE-SET Z BIT
448 001100- 000270      SEN     ;PRE-SET N BIT
449 001102- 072267      ASH     PLIER,R2 ;SHIFT 1 PLACE LEFT RESULT = 52524
450                                     ;N=0,Z=0,V=1,C=1
451 001106- 100403      BMI     10$ ;IF N SET,REPORT ERROR
452 001110- 001402      BQI     10$ ;IF Z SET,REPORT ERROR

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453 001112- 102001      10$: BVC     10$ ;IF V = 0,REPORT ERROR
454 001114- 103403      BCS     1$ ;IF C SET,GO ON WITH TEST
455 001116-
456 001116-
457          HRDR   < <INCORRECT CONDITION CODES>
458          ;*****
459 001116- 104405      ;IF B <>
460 HRDRS,BEGIN,NULL ;INCORRECT CONDITION CODES
461          ;IF
462 HRDRS,BEGIN, ;INCORRECT CONDITION CODES
463          ;FNDC
464          ;*****
465 001124- 022702      1$: CMP      #52524,R2 ;RESULT CORRECT?
466 001132- 001403      BQO     ASH2
467 001132-
468          HRDR   < <INCORRECT RESULT>
469          ;*****
470 001132- 104405      ;IF B <>
471 HRDRS,BEGIN,NULL ;INCORRECT RESULT
472          ;IF
473 HRDRS,BEGIN, ;INCORRECT RESULT
474          ;FNDC
475          ;*****
476 001140- 005067      ASH2: CLR      PLIER
477 001144- 012767      MOV      #-1,PLIER ;LOAD SHIFT VALUE (-1 OR 1 PLACE RIGHT)
478 001152- 012701      MOV      #52525,R1 ;GET VALUE TO BE SHIFED (#52525)
479 001156- 072167      ASH     PLIER,R1 ;SHIFT 1 PLACE RIGHT RESULT = #25252
480 001162- 020127      CMP      R1,#25252 ;RESULT CORRECT?
481 001166- 001403      BQO     ASHC1
482 001170-
483          HRDR   < <INCORRECT RESULT>
484          ;*****
485 001170- 104405      ;IF B <>
486 HRDRS,BEGIN,NULL ;INCORRECT RESULT
487          ;IF
488 HRDRS,BEGIN, ;INCORRECT RESULT
489          ;FNDC
490          ;*****
491          ;SBTTL TEST ASHC INSTRUCTION
492          ASHC1: CLR      #2
493 001200- 005067      CLR      PLIER ;CLEAR MSH RESULT REGISTER
494 001204- 012767      MOV      #16,PLIER ;LOAD SHIFT COUNT (16 PLACES LEFT)
495 001212- 012703      MOV      #125252,R3 ;GET VALUE TO BE SHIFED (#125252)
496 001216- 000257      CCC     ;PRE-CLEAR ALL CC BITS
497 001220- 000264      SEZ     ;PRE-SET Z BIT
498 001222- 000261      SEC     ;PRE-SET C BIT
499 001224- 073267      ASHC     PLIER,R2 ;SHIFT # IN R3 TO R2
500                                     ;CC: N=1,Z=0,V=1,C=0
501 001230- 100003      BPL     10$ ;IF N = 0,REPORT ERROR
502 001232- 001402      BQO     10$ ;IF Z SET,REPORT ERROR
503 001234- 102001      BVC     10$ ;IF V = 0,REPORT ERROR
504 001238- 103003      BCC     1$ ;IF C = 0,GO ON WITH TEST
505 001240-
506 001240- 10$: HRDR   < <INCORRECT CONDITION CODES>
507          ;*****
508          ;IF B <>

```

```
509 001240 104405 000000 000000 HRDERS,BEGIN,NULL ;INCORRECT CONDITION CODES
510 .IFF
511 HRDERS,BEGIN, ;INCORRECT CONDITION CODES
512 .FNDC
513 *****
514 001246 022702 125252 15: CMP #125252,R2 ;R2=#125252?
515 001252 001403 BEQ 2S ;BRANCH IF CORRECT RESULT
516 001254 HRDERS, ;INCORRECT RESULT FOR ASHC LEFT SHIFT
517 *****
518 .IF B <>
519 001254 104405 000000 000000 HRDERS,BEGIN,NULL ;INCORRECT RESULT FOR ASHC LEFT SHIFT
520 .IFF
521 HRDERS,BEGIN, ;INCORRECT RESULT FOR ASHC LEFT SHIFT
522 .FNDC
523 *****
524 001262 005703 25: TEST R3 ;WAS # SHIFTED OUT OF R3?
525 001264 001403 BEQ ASHC2
526 001266 HRDERS, ;# WAS NOT SHIFTED OUT OF R3 PROPERLY
527 *****
528 .IF B <>
529 001266 104405 000000 000000 HRDERS,BEGIN,NULL ;# WAS NOT SHIFTED OUT OF R3 PROPERLY
530 .IFF
531 HRDERS,BEGIN, ;# WAS NOT SHIFTED OUT OF R3 PROPERLY
532 .FNDC
533 *****
534 001274 005003 ASHC2: CLR R3 ;CLEAR RESULT REGISTER
535 001276 005067 CLR PLIER ;CLEAR PLIER REGISTER
536 001302 012767 000352 000344 MOV #16,PLIER ;LOAD SHIFT COUNT (16 PLACES RIGHT)
537 001310 012702 125252 MOV #125252,R2 ;LOAD # TO BE SHIFTED (#125252)
538 001314 000250 CLN ;PRE-CLEAR N BIT
539 001316 000264 STZ ;PRE-SET Z BIT
540 001320 000262 SEV ;" "
541 001322 000261 SEC ;" C "
542 001324 073267 000324 ASHC PLIER,R2 ;SHIFT R2 16 PLACES RIGHT INTO R3
543 .CC: N=1,Z=V=C=0
544 001330 100002 BPL 10S ;IF N = 0,REPORT ERROR
545 001332 101401 BLS 10S ;IF C OR Z SET,REPORT ERROR
546 001334 102003 BVC 1S ;IF V = 0,GO ON WITH TEST
547 001336 15: HRDERS, ;INCORRECT CONDITION CODES
548 *****
549 001336 104405 000000 000000 HRDERS,BEGIN,NULL ;INCORRECT CONDITION CODES
550 .IFF
551 HRDERS,BEGIN, ;INCORRECT CONDITION CODES
552 .FNDC
553 *****
554 001344 022702 177777 15: CMP #-1,R2 ;DID SIGN EXTEND IN R2?
555 001350 001403 BEQ 2S ;SIGN FAILED TO EXTEND
556 001352 HRDERS, ;SIGN FAILED TO EXTEND
557 *****
558 001352 104405 000000 000000 HRDERS,BEGIN,NULL ;SIGN FAILED TO EXTEND
559 .IFF
560 HRDERS,BEGIN, ;SIGN FAILED TO EXTEND
561 .FNDC
562 *****
563
564
```

```
565 000 .FNDC
566 *****
567 001360 022703 125252 25: CMP #125252,R3 ;DID R2 SHIFT TO R3
568 001364 001403 BEQ DIV1 ;R2 DID NOT SHIFT INTO R3
569 001366 HRDERS, ;INCORRECT RESULT FOR ASHC LEFT SHIFT
570 *****
571 .IF B <>
572 001366 104405 000000 000000 HRDERS,BEGIN,NULL ;R2 DID NOT SHIFT INTO R3
573 .IFF
574 HRDERS,BEGIN, ;R2 DID NOT SHIFT INTO R3
575 .FNDC
576 *****
577 ;SBTTL TEST THE DIVIDE INSTRUCTION
578
579 001374 012701 000004 DIV1: MOV #4,R1 ;LOAD INDEX REGISTER
580 001400 005002 CLR R2 ;CLEAR QUOTIENT REGISTER
581 001402 012703 052525 MOV #52525,R3 ;LOAD LSH DIVIDEND
582 001406 000277 DIV B(R1),R2 ;PRE SET THE CONDITION CODES
583 001410 071261 001556 BMI 10S ;DIVIDE #52525 BY B(R1) (#52525)
584 001414 100402 BLS 10S ;QUOTIENT=1,REM=0,C=N=V=2=0
585 001416 101401 BVC 10S ;IF N SET,REPORT ERROR
586 001420 102003 BVC 1S ;IF C OR Z SET,REPORT ERROR
587 001422 15: HRDERS, ;INCORRECT CONDITION CODES
588 *****
589 001422 104405 000000 000000 HRDERS,BEGIN,NULL ;INCORRECT CONDITION CODES
590 .IFF
591 HRDERS,BEGIN, ;INCORRECT CONDITION CODES
592 .FNDC
593 *****
594 001430 020227 000001 15: CMP R2,#1 ;QUOTIENT CORRECT?
595 001434 001403 BEQ 2S ;BRANCH IF THE QUOTIENT IS CORRECT
596 001436 HRDERS, ;INCORRECT QUOTIENT
597 *****
598 001436 104405 000000 000000 HRDERS,BEGIN,NULL ;INCORRECT QUOTIENT
599 .IFF
600 HRDERS,BEGIN, ;INCORRECT QUOTIENT
601 .FNDC
602 *****
603 001444 005703 25: TEST R3 ;REMAINDER CORRECT?
604 001446 001403 BEQ DIV2 ;BRANCH IF THE REMAINDER IS CORRECT
605 001450 HRDERS, ;INCORRECT REMAINDER
606 *****
607 .IF B <>
608 001450 104405 000000 000000 HRDERS,BEGIN,NULL ;INCORRECT REMAINDER
609 .IFF
610 HRDERS,BEGIN, ;INCORRECT REMAINDER
611 .FNDC
612 *****
613 001456 005067 000172 DIV2: CLR PLIER ;LOAD MSH DIVIDEND
614 001462 012704 157777 MOV #157777,R4
```



```

621 001466 012705 100001
622 001472 012767 100000 000154
623 001500 000277
624 001502 071467 000146
625 001506 100402
626 001510 101401
627 001512 102003
628 001514
629 001514
630 001514
631
632
633 001514 104405 000000 000000
634
635
636 000
637
638 001522 020427 040000
639 001526 001403
640 001530
641
642 001530 104405 000000 000000
643
644
645 000
646
647 001536 020527 100001
648 001542 001403
649 001544
650 001544 104405 000000 000000
651
652
653 001544 104405 000000 000000
654
655
656 000
657
658
659 001552 000167 176446
660 001556 125252
661 001560 001556
662 001562 052525
663
664
665 001566 001566
666 001570 177777
667 001570 001572
668
669 001572 001572
670 001574 125252
671 001574 001576
672 001576 052525
673 001600 000000
674 001602 001600
675
676 001610

```

```

MOV #100001,R5 ;LOAD LSH DIVIDEND
MOV #100000,PLIER ;LOAD DIVISOR INTO TEMP
SCC ;PRE-SET ALL CC BITS
DIV PLIER,R4 ;DIVIDE #157777 100001 BY 100000
;QUOTIENT=40000,RFM=100001,C=N=V=Z=0
BMI 10S ;IF N SET, REPORT ERROR
BLOS 10S ;IF C OR Z SET, REPORT ERROR
BVC 1S ;IF V = 0,GD ON WITH TEST
;*****<INCORRECT CONDITION CODES>
;*****
;IF B <>
HDRS,BEGIN,NULL ;INCORRECT CONDITION CODES
;IF
HDRS,BEGIN, ;INCORRECT CONDITION CODES
;FNDC
;*****
CMP R4,#40000 ;QUOTIENT CORRECT?
BEQ 2S ;BRANCH IF THE QUOTIENT IS CORRECT
HDRF 4 ;INCORRECT QUOTIENT
;*****
;IF B <>
HDRS,BEGIN,NULL ;INCORRECT QUOTIENT
;IF
HDRS,BEGIN, ;INCORRECT QUOTIENT
;FNDC
;*****
CMP R5,#100001 ;REMAINDER CORRECT?
BEQ 3S ;BRANCH IF THE REMAINDER IS CORRECT
HDRF 4 ;INCORRECT REMAINDER
;*****
;IF B <>
HDRS,BEGIN,NULL ;INCORRECT REMAINDER
;IF
HDRS,BEGIN, ;INCORRECT REMAINDER
;FNDC
;*****
3S: JMP START
B: B 125252 ;ADDRESS OF B
B 052525
;=B+10
A: -1
A+4
;=A+4
125252
A+10 ;ADDRESS OF A+10
052525
C: 0
C ;ADDRESS OF C
;=C+10

```

```

677 001610 000000
678 001612 001610
679
680 001616 001616
681 001616 001620
682 001620 000000
683 001620 006401
684 001622 000000
685 001622 140000
686
687
688 001624 000000
689 001626 000013
690 001654 000000
691 000001

```

```

TEMP: 0
TEMP ;ADDRESS OF TEMP
;=TEMP+5
TEMP+10 ;ADDRESS OF TEMP+10 OR "0"
D:0
MARK1= 6401
CNT: 0
UM=140000
PS=177776 ;PROCESSOR STATUS WORD
V:0
PLKW 11-
PLIER:0
.END

```


SOBS	000360R	231#	241																
SOPCNT	000042R	137#																	
SOPFRS=	104406	173#																	
SOPFAS=	000048R	139#																	
SPOINT	000032R	133#	246	266	370														
SPSIZ =	000040	1#																	
SR1	000016R	136#																	
SR2	000020R	127#																	
SR3	000022R	128#																	
SR4	000024R	129#																	
START	000224R	132#	174#	358	660														
STAT	000026R	131#																	
SVR0	000062R	146#																	
SVR1	000064R	147#																	
SVR2	000066R	148#																	
SVR3	000070R	149#																	
SVR4	000072R	150#																	
SVR5	000074R	151#																	
SVR6	000076R	152#																	
SYSCNT	000052R	141#																	
TEMP	001610R	182#	184	290*	293	304*	306*	307	677#	678	680	681							
TRPDEF=	000022	173#																	
UM	= 140000	685#																	
VECTOR	000010R	122#																	
WASADR	000104R	156#																	
WDFR	000116R	163#																	
WDT0	000114R	162#																	
X	001626R	199#	201*	689#															
XFLAG	000005R	120#																	
XDR1	000230R	180#																	
Y	001624R	199#	200*	202	688#														
.	= 001656R	665#	669#	676#	680#	689#													

- ABS. 000000 000
 001656 001

ERRORS DETECTED: 0
 DEFAULT GLOBALS GENERATED: 0
 XCPBJ0,XCPRJ0/SOL/CRF:SYM=DDXCOM,XCPRJ0
 RUN-TIME: 1 2 .3 SFCONDS
 RUN-TIME RATIO: 12/4=3.0
 CORE USED: 7K (13 PAGES)