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1.0 ABSTRACT

THIS PROGRAM TESTS THE KW11-P REAL TIME CLOCK. IT CONTAINS A SERIES OF INCREMENTAL ROUTINES THAT TEST THE CONTROL AND STATUS REGISTER, COUNT SET BUFFER, COUNTER, AND INTERRUPT VECTOR ADDRESS USING 100KHZ, 10KHZ, LINE AND EXTERNAL FREQUENCIES.

2.0 REQUIREMENTS
2.1 EQUIPMENT

PDP-11 WITH KW11-P

2.2 STORAGE

THIS PROGRAM OCCUPIES MEMORY FROM 0 TO 11626.

3.0 LOADING PROCEDURE

3.1 METHOD

PROCEDURE FOR NORMAL BINARY TAPES SHOULD BE FOLLOWED

1. ABSOLUTE LOADER MUST BE IN MEMORY.
2. PLACE BINARY TAPE IN READER.
3. LOAD ADDRESS *7500 (* DETERMINED BY LOCATION OF LOADER).
4. PRESS "START" (PROGRAM WILL LOAD).

4.0 STARTING PROCEDURE

4.1 CONTROL SWITCH SETTINGS

SET SW0=1 TO SUPPRESS TESTS USING EXTERNAL FREQUENCY.
SET SW2=1 TO INCLUDE REPEATABILITY TEST T25 & T26 IF COW IS PRESENT

4.2 STARTING ADDRESSES

200 BASIC TEST
 204 RESTART ADDRESS-PRIMARYLY USED BY XOR TESTER
 210 TIMING TEST
 214 DOUBLE OR SINGLE REAL TIME CLOCK TEST. 100KHZ.
 220 DOUBLE OR SINGLE REAL TIME CLOCK TEST. 10KHZ.
 224 DOUBLE OR SINGLE REAL TIME CLOCK TEST. 60HZ.
 230 DOUBLE OR SINGLE REAL TIME CLOCK TEST 50HZ

4.3 PROGRAM AND/OR OPERATOR ACTION

**NOTE: IF NO HARDWARE SWITCH REGISTER IS AVAILABLE THE PROGRAM WILL AUTOMATICALLY USE THE CONTENTS OF LOC. 176 AS THE SOFTWARE SWITCH REGISTER. THE USER SHOULD SET UP THIS LOC. BEFORE STARTING THE PROGRAM.

LOAD PROGRAM INTO MEMORY
 SET SWITCH REGISTER TO STARTING ADDRESS ...
 LOAD ADDRESS.
 IF DESIRED TO SUPPRESS EXTERNAL FREQUENCY TESTS SET SW0=1.
 PRESS START
 PROGRAM WILL BEGIN TESTING

5. OPERATING PROCEDURE

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1665.1 OPERATIONAL SWITCH SETTINGS
5.1.1 BASIC TEST

WITH SWITCHES 12 THRU 15=0 (DOWN) THE PROGRAM WILL PRINT OUT ON ERRORS AND CONTINUE IN TEST. BELL WILL RING AT COMPLETION OF A PASS.

SWITCH SETTINGS ARE:

SW15=1 OR UP...HALT ON ERROR

SW14=1 OR UP...SCOPE LOOP

SW13=1 OR UP...INHIBIT PRINTOUT

SW11=1 OR UP...SINGLE ITERATIONS ONLY

SW4 =1 OR UP...ENABLE SYNCHRONIZATION TESTS

SW3 =1 OR UP...ADJUSTS DELAYS FOR 11/70 OR 11/45 WITH MOS OR BIPOLAR MEMORY

SW2 =1 OR UP...CLK2 PRESENT-EXECUTE REPEATABILITY TESTS

5.2 SUBROUTINE ABSTRACTS

5.2.1 SCOPE

THIS SUBROUTINE CALL IS PLACED BETWEEN EACH SUB-TEST IN THE BASIC TEST SECTION. IT RECORDS THE STARTING ADDRESS OF EACH SUB-TEST AS IT IS BEING ENTERED. IF A SCOPE LOOP IS REQUESTED, IT WILL JUMP TO THE START OF THE SUB-TEST INDICATED BY "SCOPE".

5.2.2 HLT

THIS SUBROUTINE CALL PRINTS THE ADDRESS THAT TAGS THE FAILING SUB-TEST AND THE CONTENTS OF THE CONTROL AND STATUS REGISTER, COUNTER, AND "TEMP".

6.1 ERRORS

6.1 ERROR PRINTOUT FORMAT

WITH SW13=0 (OR DOWN) THE FOLLOWING PRINTOUT WILL APPEAR ON AN ERROR:

```

PC      STATUS  COUNTER  TEMP
XXXXXX XXXXXX XXXXXX XXXXXX

```

PC = ADDRESS OF TEST WHERE ERROR OCCURRED
STATUS = CONTENTS OF COMMAND AND STATUS REGISTER AT TIME OF ERROR
COUNTER = CONTENTS OF COUNTER AT TIME OF ERROR
TEMP = CONTENTS OF ADDRESS "TEMP" USED BY SOME TESTS.

NOTE: NOT ALL OF THE INFORMATION PRINTED IS INTENDED TO BE USEFUL FOR EVERY TYPE OF ERROR. THIS IS SIMPLY A STANDARD ERROR REPORT FOR ALL ERRORS. THE OPERATOR MUST REFER TO THE PROGRAM LISTING AT THE ADDRESS OR THE ERROR FOR A DESCRIPTION OF THE CAUSE OF THE ERROR.

6.2 ERROR RECOVERY

WITH SWITCH 15=1 (OR UP) THE PROGRAM WILL HALT ON AN ERROR. DEPRESS "CONTINUE" TO RESUME TESTING.

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7. RESTRICTIONS

7.1 OPERATIONAL RESTRICTIONS

FOR PURPOSES OF TESTING THE EXTERNAL FREQUENCY SELECTION IT IS NECESSARY TO SUPPLY A KNOWN FREQUENCY TO THE EXTERNAL FREQUENCY INPUT. THIS PROGRAM USES THE INTERNAL 60HZ FOR ITS SOURCE. TO DO THIS IT IS REQUIRED THAT A JUMPER WIRE BE CONNECTED BETWEEN PINS CF1 AND DA1 OF THE SLOT IN WHICH THE CLOCK MODULE IS INSERTED. IF THIS IS NOT DONE, THEN THE PROGRAM MUST ALWAYS BE RUN WITH SWD=1 TO SUPPRESS THE EXTERNAL TESTS.

* IF A SECOND P CLOCK IS BEING USED FOR TEST PURPOSES, SET THE SWITCH REG = 000004 TO ENABLE TESTS T25 AND T26, DURING THE BASE TEST

8. MISCELLANEOUS

8.1 EXECUTION TIME

BASIC TEST REQUIRES 11 SECONDS PER PASS W/O ITERATIONS 66 WITH. TIMING TEST REQUIRES 4 MINUTES PER PASS. DOUBLE OR SINGLE REAL TIME CLOCK TEST-DETERMINED BY OPERATOR SUGGESTED EXECUTION TIMES ARE:

1. IF THE SINGLE CLOCK TEST IS RUN WITHOUT BEING FOLLOWED BY THE DUAL CLOCK TEST: 17 MINUTES FOR EACH FREQUENCY (100KHZ,10KHZ,60KHZ)
2. IF THE SINGLE CLOCK TEST IS FOLLOWED BY THE DUAL TEST
 RUN SINGLE CLOCK TEST FOR ONE MINUTE (FOR EACH FREQUENCY)
 RUN DUAL CLOCK TEST FOR FIFTY SECONDS (10 PRINTOUTS) (FOR EACH FREQUENCY)

NOTE: THIS TIME NOMINAL TIME FOR PDP-11/05
OTHER C.P.U.'S THE TIME WILL VARY

9. PROGRAM DESCRIPTION

THE PROGRAM CONSISTS OF THREE SECTIONS: THE BASIC TEST THE TIMING TEST AND THE REAL TIME CLOCK TEST. THE BASIC TEST CHECKS EACH OF THE INDIVIDUAL BITS IN THE CONTROL AND STATUS REGISTER, COUNT SET BUFFER, AND COUNTER ALONG WITH PROPER OPERATION UNDER INTERRUPT CONTROL (SINGLE OR REPEATED INTERRUPTS) COUNT UP OR COUNT DOWN, AND REPEATABILITY. THE TIMING TEST USES ALL CLOCK FREQUENCIES TO RING THE TELETYPE BELL AT 10 SECOND INTERVALS. THE CLOCK TEST PROVIDES A REAL TIME CLOCK WHOSE ACCURACY CAN BE MEASURED AGAINST AN ACCURATE EXTERNAL SOURCE.

9.1 BASIC TEST

TEST	DESCRIPTION
TO THRU T9	TEST THAT CSR, COUNT SET BUFFER AND COUNTER BITS MAY BE SET AND CLEARED.

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T10 THRU T11 TEST FIX(BITS) TO SINGLE CLOCK COUNTER.
T12 THRU T15 TEST CLOCK TO COUNT UP.
T16 THRU T19 TEST CLOCK TO COUNT DOWN.
T20 THRU T24 TEST INTERRUPT MODES.
T25 THRU T26 TEST REPEATABILITY BY CHECKING THAT THE COUNTER
CONTAINS THE SAME NUMBER OF COUNTS OVER TWO
EQUAL PERIODS OF TIME.

9.2 TIMING TEST

THIS TEST USES THE REPEATED INTERRUPT MODE TO RING THE TELETYPE BELL AT 10 SECOND INTERVALS. FIRST THE BELL IS RUNG AT 10 SECOND INTERVALS FOR 1 MINUTE USING 100HZ, FOLLOWED BY 1 MINUTE AT 10KHZ FOLLOWED BY 1 MINUTE AT LINE FREQ. (60HZ OR 50HZ) AND (IF SWO=0) 1 MINUTE AT LINE FREQ. USING EXTERNAL FREQUENCY INPUT.

9.3 DOUBLE OR SINGLE REAL TIME CLOCK TEST

9.3.1 SINGLE CLOCK REAL TIME TEST

THE 24 HOUR CYCLE:
THIS TEST TRANSFORMS YOUR COMPUTER INTO AN ACCURATE DIGITAL "WALL CLOCK." A NORMAL CLOCK'S 12 HOUR CYCLE HAS BEEN REPLACED BY A 24 HOUR CYCLE.

EXAMPLES OF THE 24 HOUR CYCLE FOLLOW:

ACTUAL TIME	PRINTOUT			
	HRS	MINS	SECS	TENTHS+HUNDRETHS OF SECS.
MIDNIGHT	00	: 00	: 00	: 00
8:32 AM	08	: 32	: 00	: 00
12 NOON	12	: 00	: 00	: 00
2:15 PM	14	: 15	: 00	: 00
11:30 PM	23	: 30	: 00	: 00

9.3.1.1 ENTERING THE TIME

THE CLOCK CAN BE UPDATED BY HOLDING THE CTRL KEY DOWN AND TAPPING THE I KEY. THE CTRL KEY IS THEN RELEASED, AND THE STARTING TIME IS ENTERED.

THE MOST SIGNIFICANT HOUR DIGIT IS ENTERED FIRST. THIS DIGIT MUST BE A ZERO, A ONE OR A TWO. THE LEAST SIGNIFICANT HOURS DIGIT IS ENTERED NEXT FOLLOWED BY THE TWO MINUTES DIGIT, FOLLOWED BY THE TWO SECONDS DIGIT. THE FRACTION OF A SECOND DIGITS ARE NOT ENTERED. THE USER WILL ENTER A TOTAL OF SIX DIGITS WITH NO SPACES, COLONS, OR ANY OTHER CHARACTERS BETWEEN DIGITS. THE USER MUST

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ENTER A TIME THAT WILL OCCUR A HALF MINUTE OR MORE IN THE FUTURE, TO ALLOW ENOUGH TIME TO ENTER THE REQUIRED INFORMATION. AFTER THE INFORMATION HAS BEEN ENTERED, THE USER MONITORS THE TIME STANDARD. WHEN THAT STANDARD REACHES THE TIME ENTERED VIA THE KEYBOARD, THE USER HITS THE CARRAGE RETURN (CR) KEY TO START THE CLOCK. NOTE THAT THE CHARACTERS WILL NOT BE PRINTED OUT AS THE TIME IS BEING ENTERED.

9.3.1.2 READING THE TIME

TO PRINT THE TIME, DEPRESS THE CTRL KEY. WHILE HOLDING THE CTRL KEY DOWN, SMARTLY TAP THE T KEY. THE TIME WHICH CORRESPONDS TO THE INSTANT THAT THE T KEY WAS DOWN, WILL BE PRINTED OUT. THE FORMAT OF THE PRINTOUT WILL BE SIMILAR TO THAT SHOWN IN THE 24 HOUR TIME EXAMPLE. THE ONLY DIFFERENCE WILL BE THE ABSENCE OF SPACES.

9.3.1.3 TIME REFERENCES

SINCE THE SYSTEM CLOCK IS MORE ACCURATE THAN MANY WRIST WATCHES, IT IS A GOOD IDEA TO USE AN ACCURATE TIME STANDARD. MANY TELEPHONE COMPANIES PROVIDE A NUMBER WHERE THE TIME, SYNCHRONIZED TO THE NATIONAL BUREAU OF STANDARDS RADIO STATION (WWV), IS AVAILABLE. CONSULT WITH YOUR LOCAL TELEPHONE COMPANY TO SEE IF THIS SERVICE IS AVAILABLE IN YOUR AREA.

9.3.1.4 PROCEDURE FOR SINGLE CLOCK REAL TIME TEST.

1. PERFORM THE BASIC TEST, PRIOR TO THE PERFORMANCE OF THIS TEST. PROCEED ONLY IF THE BASIC TEST HAS PASSED.
2. LOAD ADDRESS 214 VIA THE SWITCH REGISTER, (100KHZ TEST)
3. PLACE ALL ZEROS IN SWITCH REG., DEPRESS START
4. EXAMINE YOUR TIME REFERENCE, AND SELECT A TIME THAT WILL ALLOW YOU ENOUGH TIME TO ENTER THE TIME VIA THE KEYBOARD.
5. ENTER THE TIME, AS DESCRIBED PREVIOUSLY.
6. START THE CLOCK (HIT THE CR KEY) AT THE INSTANT THE TIME REFERENCE CORRELATES WITH THE TIME ENTERED.
7. MONITOR YOUR TIME REFERENCE, EXACTLY 1 MINUTE FROM THE TIME YOU STARTED THE CLOCK, READ THE PROGRAM CLOCK AS DESCRIBED PREVIOUSLY.
8. THE ONE MINUTE TIME ERROR SHOULD BE WITHIN ONE SECOND OF THE ACTUAL TIME.
9. IF THE RESULT OF STEP 8 IS NOT WITHIN ONE SECOND, ALLOW EXACTLY ONE MORE MINUTE TO PASS (FROM THE ORIGINAL START TIME). READ THE TIME AGAIN. IF THE TOTAL ERROR DOUBLED, THE BOARD IS DEFECTIVE. IF THE ERROR IS CONSTANT,

H01

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RESTART THE TEST.

- 10.* IF THE ONE MINUTE TEST WAS PASSED, ALLOW THE TEST TO RUN FOR EXACTLY 16 MINUTES MORE. AT THE EXACT END OF THE 16TH MINUTE INTERVAL, READ THE CLOCK. IT SHOULD BE WITHIN THREE SECONDS OF THE CORRECT TIME. IF IT IS NOT, THE BOARD IS DEFECTIVE. IN THE EVENT THAT THE DUAL CLOCK REAL TIME TEST IS GOING TO BE PERFORMED, THIS STEP CAN BE OMITTED.
 11. LOAD ADDRESS 220 VIA SWITCH REGISTER, DEPRESS START (10KHZ TEST) REPEAT STEPS 3-10
 12. LOAD ADDRESS 224 VIA SWITCH REGISTER, DEPRESS START (224 IF 60HZ, OR 230 IF 50HZ LINE TEST) REPEAT STEPS 3-10
- * THE DURATION OF THIS TEST IS ARBITRARY. IT IS NOMINALLY A THOUSAND SECOND TEST. LONGER TESTS ARE PERMISSIBLE. THE RESULTS OF LONG TERM TESTS SHOULD BE WITHIN (PLUS OR MINUS) 1 MINUTE FOR A 24 HR TEST.

NOTE THAT THE TIME CAN BE READ AT ANY POINT WITHIN THE TEST WITHOUT AFFECTING THE TEST.

9.3.2 DUAL CLOCK REAL TIME CLOCK TEST

THE USE OF A TEMPORARY CLOCK (REFERED AS COW) REDUCES THE TIME REQUIRED FOR THE REAL TIME TEST. THE SECOND CLOCK INTERRUPTS THE FIRST CLOCK EVERY FIVE SECONDS. THE DURATION OF THE COMBINED REAL TIMES TESTS, WHEN THE DUAL CLOCK TEST IS USED IS 1 MIN : 50 SEC/FREQ VERSUS 17 MIN/FREQ FOR THE SINGLE CLOCK REAL TIME TEST ALONE.

THE DUAL CLOCK TEST REQUIRES THAT THE CLOCK BE STARTED AS IN THE SINGLE MODE. RAISING SWITCHES #0 AND #2 CAUSE THE PRINTOUT TO OCCUR AUTOMATICALLY.

THE COW MODULE SHOULD ONLY BE INSTALLED IN THE SYSTEM WHILE THIS DIAGNOSTIC IS BEING USED.

TO CONVERT A STANDARD P CLOCK TO A "COW" MODULE:

1. REMOVE JUMPER A4
CSR=772560
CSB=772562
CTR=772564
2. ADD JUMPER V8
VECTOR LOCATION IS 504
PSW " " 506

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NOTE: THIS VECTOR IS IN FLOATING VECTOR SPACE, CAUTION IS ADVISED WITH RESPECT TO ALLOWING VECTOR CONFLICTS.

9.3.2.1 PROCEDURE FOR DUAL CLOCK REAL TIME CLOCK TEST

1. LOAD ADDRESS 214, DEPRESS START (100KHZ TEST)
2. ENTER THE TIME VIA THE TTY KEYBOARD AS DESCRIBED PREVIOUSLY
3. SET THE SWITCHES IN THE SWITCH REGISTER TO 000005, THE TTY WILL PRINT THE TIME AT 5 SECOND INTERVALS
4. CONSECUTIVE PRINTOUTS WILL BE WITHIN 5.00 PLUS OR MINUS .01 SECONDS OF EACH OTHER. ALLOW THE TEST TO RUN FOR AT LEAST TEN PRINTOUTS. IF THE TOLERANCE IS EXCEEDED, THE CLOCK IS DEFECTIVE.
5. LOAD ADDRESS 220, DEPRESS START (10KHZ TEST)
6. REPEAT STEPS 2-4
7. LOAD ADDRESS 224, IF 60HZ, OR 230 IF 50HZ DEPRESS START (LINE TEST)
8. REPEAT STEPS 2 & 3
9. CONSECUTIVE PRINTOUTS WILL BE WITHIN 5.00 PLUS OR MINUS .04 SECONDS OF EACH OTHER. TYPICALLY, AND 5.00 PLUS OR MINUS .2 SECONDS WORST CASE, DUE TO POSSIBLE AC LINE FREQUENCY VARIATIONS. ALLOW THE TEST TO RUN FOR AT LEAST TEN PRINTOUTS. IF THE TOLERANCE IS EXCEEDED, THE CLOCK IS DEFECTIVE.

10.

THIS KW11-P DIAGNOSTIC WILL GO OUT & FIND IF THIS SHOULD RUN WITH CPU THAT HAS A SWITCH REG. OR WILL RUN WITH A PDP-11/04 THAT HAS NO SWITCH REGISTER. IF CPU HAS NO SWITCH REG. LOCATION 176 EQUALS SOFTWARE SWITCH REGISTER. IN THE ABOVE TEST TYPING !G(CONTROL-G) WILL ALLOW YOU TO ENTER/ALTER THE SOFTWARE SWITCH SETTINGS
... .ENDR


```

430
431
432
433
434      000000
435
436      000030
437 000030 005630
438 000032 000340
439 000034 006130
440 000036 000340
441
442 000046 000046
443      005154
444      104000
445      177776
446      000240
447      104400
448      000176
449      000776
450 000200 000137 001046
451 000204 000137 001130
452 000210 000137 005170
453 000214 000137 006640
454 000220 000137 006724
455 000224 000137 007010
456 000230 000137 007074
457
458      001000
459 001000 172540
460 001002 172542
461 001004 172544
462 001006 000104
463 001010 000106
464 001012 177566
465 001014 177564
466 001016 000000
467 001020 000000
468 001022 000001
469 001024 177740
470 001026 177730
471 001030 160000
472 001032 160000
473 001034 177700
474
475 001036 177660
476 001040 140000
477 001042 140000
478 001044 177570
479
480
481
482
483 001046 012706 000776
484 001052 004737 011566
485 001056 004737 011524
    
```

```

.SBTTL      BASIC TEST
;COPYRIGHT 1971, 1972 DIGITAL EQUIPMENT CORP., MAYNARD, MASS. 01754
;JOHN RODENHISER/JIM LACEY
    
```

```

.ENABL AMA,ABS
.=0
;TRAP CATCHER 0-200
    
```

```

.=30
PRINT
340
SCOPEC
340
.=46
LOGICAL
HLT=EMT
CC=177776
NOP=240
SCOPE=TRAP
SOFTSR=176
BUFF=776
    
```

; SOFTWARE SWITCH REGISTER

```

.=200
JMP      J#BEGIN2
JMP      J#BEGIN
JMP      J#BEGIN1
JMP      J#K100HZ
JMP      J#K10HZ
JMP      J#H60Z
JMP      J#H50Z
    
```

```

;START BASIC TEST
;RESTART BASIC TEST
;START TIMING TEST
;DOUBLE OR SINGAL CLK TEST. 100KHZ.
;DOUBLE OR SINGLE CLK TEST. 10KHZ.
;DOUBLE OR SINGLE CLK TEST. 60HZ.
;DOUBLE OR SINGLE CLK TEST. 50HZ
    
```

```

.=1000
CSR:     172540
CSB:     172542
CTR:     172544
CKV:     104
CKVS:    106
TDBR:    177566
TCSR:    177564
TEMP1:   0
TEMP:    0
ICOUNT:  1
DEL1:    -40
DEL2:    -50
DEL3:    -20000
DEL4:    -20000
ADJ:     -100
    
```

```

;CONTROL AND STATUS REGISTER
;COUNT SET BUFFER
;COUNTER
;CLOCK VECTOR ADDRESS
    
```

SR: 177570

```

;DELAY ADJUSTMENT FOR 11/70
; & 11/45 WITH MOS MEM.
    
```

```

BEGIN2: MOV      #BUFF,%6
        JSR      %7,SWADJ
        JSR      %7,DELADJ
    
```

```

;HAS THIS CPU HAVE A SWITCH REG.?
;IS ADJUSTMENT IN DELAY REQUIRED
    
```



```

486 001062 013746 000004          MOV    a#4, -(%b)
487 001066 012737 001210 000004    MOV    #XOR, a#4
488 001074 005737 177060          TST    a#177060
489 001100 012637 000004          MOV    (%b)+, a#4
490 001104 012737 177777 006232    MOV    #-1, a#XORFLG
491 001112 012737 000001 001022    MOV    #1, a#ICOUNT
492 001120 012702 006464          MOV    #XORM, %2
493 001124 004737 006246          JSR    %7, TOP
494
495 001130 012706 000776          BEGIN: MOV    #BUFF, %b
496 001134 004737 011566          JSR    %7, SWADJ
497 001140 004737 011524          JSR    %7, DELADJ
498 001144 012737 005552 000024    MOV    #PWR1, 24
499 001152 005077 005406          CLR    aPSW
500 001156 005037 001020          CLR    TEMP
501 001162 005037 006230          CLR    SCOPEF
502 001166 005037 001016          CLR    TEMP1
503 001172 012737 001234 006244    MOV    #TO, RETURN
504 001200 005037 005744          CLR    PRINT1
505 001204 000137 001234          JMP    TO
506
507 001210 022626          XOR:   CMP    (%b)+, (%b)+
508 001212 012637 000004          MOV    (%b)+, a#4
509 001216 012737 000005 001022    MOV    #5, a#ICOUNT
510 001224 005037 006232          CLR    a#XORFLG
511 001230 000137 001130          JMP    a#BEGIN
512
513          ;TEST INIT TO CLEAR CONTROL AND STATUS REGISTER
514 001234 013746 000004          TO:   MOV    a#4, -(%b)
515 001240 012737 001272 000004    MOV    #CSRT, a#4
516 001246 012777 100377 177524    MOV    #100377, aCSR
517 001254 000005          RESET
518 001256 032777 100377 177514    BIT    #100377, aCSR
519 001264 001413          BEQ    T1
520 001266 104000          HLT
521 001270 000411          BR    T1
522 001272 022626          CSRT: CMP    (%b)+, (%b)+
523 001274 012637 000004          MOV    (%b)+, a#4
524 001300 032777 040000 177536    BIT    #40000, aSR
525 001306 001352          BNE    TO
526 001310 000000          HALT
527 001312 000750          BR    TO
528          ;TEST COUNT SET BUFFER
529 001314 012637 000004          T1:  MOV    (%b)+, a#4
530 001320 104400          SCOPE
531 001322 012777 177777 177452    MOV    #-1, aCSB
532 001330 005777 177446          TST    aCSB
533 001334 001401          BEQ    .+4
534 001336 104000          HLT
535 001340 012737 177777 001020    MOV    #-1, a#TEMP
536 001346 012777 000000 177430    MOV    #0, aCTR
537 001354 023777 001020 177422    CMP    a#TEMP, aCTR
538 001362 001401          BEQ    .+4
539 001364 104000          HLT
540          ;CTR CHANGED WHEN WRITTEN TO
541          ;TEST COUNT SET BUFFER TO ACCEPT A COUNT PATTERN
          ;TEST COUNTER TO CONTAIN COUNT SET BUFFER VALUE

```

```

;SET UP STACK FOR SCOPE LOOPS
;HAS THIS CPU HAVE A SWITCH REG.?
;IS ADJUSTMENT IN DELAY REQUIRED
;INIT POWER FAIL POINTER
;CLEAR PROC. STATUS REG.
;INIT. SCOPEF TAG
;SET UP RESTART OF PROGRAM
;INITIALIZE ERROR PRINTOUT READING

```

```

;ERROR, INIT FAILED TO CLEAR ALL BITS OF CSR.

```

```

;NO SSYN FROM DEVICE

```

```

;ERR, FAILED TO GIVE ZERO'S FROM WRITE ONLY REG.

```

```

542 001366 005037 001020          CLR      TEMP
543 001372 104400          SCOPE
544 001374 013777 001020 177400 T3:  MOV     TEMP, @CSB
545 001402 023777 001020 177374  CMP     TEMP, @CTR
546 001410 001401          BEQ     .+4
547 001412 104000          HLT
548 001414 005237 001020          INC     TEMP
549 001420 001365          BNE     T3
;ERROR, CTR NOT=TEMP
;+1 TO COUNT PATTERN
;REPEAT UNTIL COUNT OVERFLOWS
550          ;TEST THAT CTR REMAINS CONSTANT IF RUN CLEAR
551 001422 104400          T3A:  SCOPE
552 001424 005077 177350          CLR     @CSR
553 001430 012777 177777 177344  MOV     #-1, @CSB
554 001436 013737 001030 001020  MOV     @DEL3, @TEMP
555 001444 005237 001020          IS:   INC     @TEMP
556 001450 001375          BNE     IS
557 001452 022777 177777 177324  CMP     #-1, @CTR
558 001460 001401          BEQ     .+4
559 001462 104000          HLT
;CTR CHANGED ALTHOUGH RUN 0
560          ;TEST THAT CTR REMAINS CONSTANT WHEN CSR IS REF'D
561 001464 104400          T3B:  SCOPE
562 001466 005077 177306          CLR     @CSR
563 001472 012777 177777 177302  MOV     #-1, @CSB
564 001500 013737 001030 001020  MOV     @DEL3, @TEMP
565
566 001506 012777 177736 177264  IS:   MOV     #177736, @CSR
567 001514 017700 177260          MOV     @CSR, %0
568 001520 012777 000000 177252  MOV     #0, @CSR
569 001526 017700 177246          MOV     @CSR, %0
570 001532 005237 001020          INC     @TEMP
571 001536 001363          BNE     IS
572 001540 022777 177777 177236  CMP     #-1, @CTR
573 001546 001401          BEQ     .+4
574 001550 104000          HLT
;CTR CHANGED BY CSR REF
575          ;TEST INIT TO CLEAR COUNT SET BUFFER WHEN IT IS =-1
576 001552 104400          T4:   SCOPE
577 001554 012777 177777 177220  MOV     #-1, @CSB
578 001562 000005          RESET
579 001564 005777 177214          TST    @CTR
580 001570 001401          BEQ     .+4
581 001572 104000          HLT
;ERROR, INIT FAILED TO CLEAR CSB
582          ;TEST RATE SELECT (BIT,2) MAY BE SET AND CLEARED
583 001574 104400          T5:   SCOPE
584 001576 012777 000002 177174  MOV     #2, @CSR
585 001604 022777 000002 177166  CMP     #2, @CSR
586 001612 001401          BEQ     .+4
587 001614 104000          HLT
;ERROR, CSR NOT = 2
588 001616 012777 000004 177154  MOV     #4, @CSR
589 001624 022777 000004 177146  CMP     #4, @CSR
590 001632 001401          BEQ     .+4
591 001634 104000          HLT
;ERROR, CSR NOT = 4
592 001636 012777 000006 177134  MOV     #6, @CSR
593 001644 022777 000006 177126  CMP     #6, @CSR
594 001652 001401          BEQ     .+4
595 001654 104000          HLT
;ERROR, CSR NOT = 6
596 001656 005077 177116          CLR     @CSR
597 001662 005777 177112          TST    @CSR
  
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MO1

MAIN. MACY11 27(732) 10-SEP-76 13:04 PAGE 12
 DZKWBG.P11 BASIC TEST

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598 001666 001401          BEQ      .+4
599 001670 104000          HLT
600                                ;TEST MODE (BIT 3) CAN BE SET AND CLEARED
601 001672 104400          T6:  SCOPE
602 001674 012777 000010 177076  MOV     #10, @CSR
603 001702 022777 000010 177070  CMP     #10, @CSR
604 001710 001401          BEQ     .+4
605 001712 104000          HLT
606 001714 005077 177060          CLR     @CSR
607 001720 005777 177054          TST     @CSR
608 001724 001401          BEQ     .+4
609 001726 104000          HLT
610                                ;TEST UP/DN (BIT 4) CAN BE SET AND CLEARED
611 001730 104400          T7:  SCOPE
612 001732 012777 000020 177040  MOV     #20, @CSR
613 001740 022777 000020 177032  CMP     #20, @CSR
614 001746 001401          BEQ     .+4
615 001750 104000          HLT
616 001752 005077 177022          CLR     @CSR
617 001756 005777 177016          TST     @CSR
618 001762 001401          BEQ     .+4
619 001764 104000          HLT
620                                ;TEST INTERRUPT ENABLE (BIT 6) CAN BE SET AND CLEARED
621
622
623 001766 104400          T9:  SCOPE
624 001770 012737 000340 177776  MOV     #340, CC
625 001776 012777 000100 176774  MOV     #100, @CSR
626 002004 022777 000100 176766  CMP     #100, @CSR
627 002012 001401          BEQ     .+4
628 002014 104000          HLT
629 002016 005077 176756          CLR     @CSR
630 002022 005777 176752          TST     @CSR
631 002026 001401          BEQ     .+4
632 002030 104000          HLT
633                                ;TEST RUN (BIT 0) CAN BE SET AND CLEARED
634
635 002032 104400          T9A: SCOPE
636 002034 005077 176740          CLR     @CSR
637 002040 005037 001020          CLR     TEMP
638 002044 013777 001020 176730  MOV     TEMP, @CSB
639 002052 012777 000021 176720  MOV     #21, @CSR
640 002060 032777 000001 176712  BIT     #1, @CSR
641 002066 001001          BNE     .+4
642 002070 104000          HLT
643 002072 104400          SCOPE
644 002074 005077 176700          CLR     @CSR
645 002100 005037 001020          CLR     TEMP
646 002104 013777 001020 176670  MOV     TEMP, @CSB
647 002112 012777 000020 176660  MOV     #20, @CSR
648 002120 052777 000001 176652  BIS     #1, @CSR
649 002126 032777 000001 176644  BIT     #1, @CSR
650 002134 001001          BNE     .+4
651 002136 104000          HLT
652 002140 104400          SCOPE
653 002142 005077 176632          CLR     @CSR

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654 002146 005037 001020          CLR      TEMP
655 002152 013777 001020 176622      MOV      TEMP, @CSB
656 002160 012777 000021 176612      MOV      #21, @CSR
657 002166 012777 000020 176604      MOV      #20, @CSR
658 002174 032777 000001 176576      BIT      #1, @CSR
659 002202 001401          BEQ      .+4
660 002204 104000          HLT
; START AT ZERO
; DISABLE INTERRUPT, COUNT UP, SET RUN
; LEAVE ALL SAME RESET RUN
; CHECK BIT 0
; BRANCH IF NOT SET
; CSR PICKED BIT 0 ON A MOV.

661
662
663 ; TEST FIX (BIT 5) TO SINGLE CLOCK COUNTER
664 ; SET UP/DN (BIT 4) = 0 TO ENABLE COUNT DOWN
†10: SCOPE
665 002206 104400          CLR      @CSR
666 002210 005077 176564          MOV      #-1, @CSB
667 002214 012777 177777 176560      MOV      #-2, TEMP
668 002222 012737 177776 001020      MOV      #40, @CSR
669 002230 012777 000040 176542      MOV      #40, @CSR
670 002236 023777 001020 176540      CMP      TEMP, @CTR
671 002244 001401          BEQ      .+4
672 002246 104000          HLT
673 002250 005337 001020          DEC      TEMP
674 002254 023727 001020 000000      CMP      TEMP, #0
675 002262 001362          BNE      T10A
; ERROR, COUNTER NOT = TEMP, DIDN'T COUNT DOWN
; -1 TO PATTERN COUNT
; DONE ALL COUNTS?
; NO

676
677 ; TEST FIX (BIT 5) TO SINGLE CLOCK COUNTER
678 ; SET UP/DN (BIT 4) = 1 TO ENABLE COUNT UP
†11: SCOPE
679 002264 104400          CLR      @CSR
680 002266 005077 176506          CLR      @CSB
681 002272 005077 176504          MOV      #1, TEMP
682 002276 012737 000001 001020      MOV      #60, @CSR
683 002304 012777 000360 176466      MOV      #60, @CSR
684 002312 023777 001020 176464      CMP      TEMP, @CTR
685 002320 001401          BEQ      .+4
686 002322 104000          HLT
687 002324 005237 001020          INC      TEMP
688 002330 023727 001020 000000      CMP      TEMP, #0
689 002336 001362          BNE      T11A
; ERROR, COUNTER NOT = TEMP, FAILED TO COUNT UP.
; +1 TO PATTERN COUNT
; DONE ALL COUNTS ?
; NO

690 ; TEST CLOCK TO COUNT DOWN AT ALL FREQUENCIES
691 ; 100KHZ
†12: SCOPE
692 002340 104400          CLR      @CSR
693 002342 005077 176432          MOV      #2, @CSB
694 002346 012777 000002 176426      MOV      #1, @CSR
695 002354 012777 000001 176416      MOV      #1, @CSR
696 002362 013737 001024 001020      MOV      @DEL1, @TEMP
697 002370 105777 176404          TSTB    @CSR
698 002374 100410          BMI     T12B
699 002376 062737 000001 001020      ADD     #1, @TEMP
700 002404 001371          BNE     T12A
701 002406 042777 000001 176364      BIC     #1, @CSR
702 002414 104000          HLT
703 002416 005777 176362          TST     @CTR
704 002422 001401          BEQ     .+4
705 002424 104000          HLT
; ERROR, P INTR (BIT 7) NOT = 1.
; ERROR, COUNTER DID NOT COUNT DOWN TO 0

706
707 ; 10KHZ
†13: SCOPE
708 002426 104400          CLR      @CSR
709 002430 005077 176344          MOV      #2, @CSB
710 002434 012777 000002 176340      MOV      #2, @CSB

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710 002442 012777 000003 176330      MOV      #3,DCSR      ;DOWN COUNT, 10KHZ, GO
711 002450 013737 001026 001020      MOV      @DEL2,@TEMP
712 002456 105777 176316      T13A:   TSTB      DCSR
713 002462 100410      BMI      T13B
714 002464 062737 000001 001020      ADD      #1,@TEMP
715 002472 001371      BNE      T13A
716 002474 042777 000001 176276      BIC      #1,DCSR
717 002502 104000      HLT
718 002504 005777 176274      T13B:   TST      @CTR      ;ERROR, P INTR (BIT 7) NOT = 1.
719 002510 001401      BEQ      .+4
720 002512 104000      HLT      ;ERROR, COUNTER DID NOT COUNTDOWN TO 0
721
722
723 002514 104400      ;LINE FREQ.
724 002516 005737 006232      T14:   SCOPE
725 002522 100432      TST      @XORFLG
726 002524 005077 176250      BMI      T15
727 002530 012777 000002 176244      CLR      @CSR
728 002536 012777 000005 176234      MOV      #2,@CSB
729 002544 013737 001030 001020      MOV      #5,DCSR      ;DOWN COUNT, LINE FREQ., GO
730 002552 105777 176222      T14A:  TSTB      @DEL3,@TEMP
731 002556 100410      BMI      T14B
732 002560 062737 000001 001020      ADD      #1,@TEMP
733 002566 001371      BNE      T14A
734 002570 042777 000001 176202      BIC      #1,DCSR
735 002576 104000      HLT      ;ERROR, P INTR (BIT 7) NOT=1
736 002600 005777 176200      T14B:  TST      @CTR
737 002604 001401      BEQ      .+4
738 002606 104000      HLT      ;ERROR, COUNTER DID NOT COUNT DOWN TO 0
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740
741 002610 104400      ;EXT FREQ
742 002612 032777 000001 176224      T15:   SCOPE
743 002620 001032      BIT
744 002622 005077 176152      BNE      T16
745 002626 012777 000002 176146      CLR      @CSR
746 002634 012777 000007 176136      MOV      #2,@CSB
747 002642 013737 001032 001020      MOV      #7,DCSR      ;DOWN COUNT, EXT., GO
748 002650 105777 176124      T15A:  TSTB      @DEL4,@TEMP
749 002654 100410      BMI      T15B
750 002656 062737 000001 001020      ADD      #1,@TEMP
751 002664 001371      BNE      T15A
752 002666 042777 000001 176104      BIC      #1,DCSR
753 002674 104000      HLT      ;ERROR, P INTR (BIT 7) NOT=1
754 002676 005777 176102      T15B:  TST      @CTR
755 002702 001401      BEQ      .+4
756 002704 104000      HLT      ;ERROR, COUNTER DID NOT COUNT DOWN TO 0
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758 002706 104400      ;TEST CLOCK TO COUNT UP AT ALL FREQUENCIES
759 002710 005077 176064      ;100 KHZ
760 002714 012777 177776 176060      T16:   SCOPE
761 002722 012777 000021 176050      CLR      @CSR
762 002730 013737 001024 001020      MOV      #-2,@CSB
763 002736 105777 176036      MOV      #21,DCSR      ;UP COUNT, 100 KHZ, GO
764 002742 100410      MOV      @DEL1,@TEMP
765 002744 062737 000001 001020      T16A:  TSTB      @CSR
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766	002752	001371			BNE	T16A	
767	002754	042777	000001	176016	BIC	#1, @CSR	
768	002762	104000			HLT		;ERROR
769	002764	005777	176014		T16B: TST	@CTR	
770	002770	001401			BEQ	+.4	
771	002772	104000			HLT		;ERROR
772					:10 KHZ		
773	002774	104400			T17: SCOPE		
774	002776	005077	175776		CLR	@CSR	
775	003002	012777	177776	175772	MOV	#-2, @CSB	
776	003010	012777	000023	175762	MOV	#23, @CSR	;UP COUNT, 10 KHZ, GO
777	003016	013737	001026	001020	MOV	@DEL2, @TEMP	
778	003024	105777	175750		T17A: TSTB	@CSR	
779	003030	100410			BMI	T17B	
780	003032	062737	000001	001020	ADD	#1, @TEMP	
781	003040	001371			BNE	T17A	
782	003042	042777	000001	175730	BIC	#1, @CSR	
783	003050	104000			HLT		;ERROR
784	003052	005777	175726		T17B: TST	@CTR	
785	003056	001401			BEQ	+.4	
786	003060	104000			HLT		;ERROR
787					:LINE FREQ.		
788	003062	104400			T18: SCOPE		
789	003064	005737	006232		TST	@XORFLG	
790	003070	100432			BMI	T19	
791	003072	005077	175702		CLR	@CSR	
792	003076	012777	177776	175676	MOV	#-2, @CSB	
793	003104	012777	000025	175666	MOV	#25, @CSR	;UP COUNT, LINE, GO
794	003112	013737	001030	001020	MOV	@DEL3, @TEMP	
795	003120	105777	175654		T18A: TSTB	@CSR	
796	003124	100410			BMI	T18B	
797	003126	062737	000001	001020	ADD	#1, @TEMP	
798	003134	001371			BNE	T18A	
799	003136	042777	000001	175634	BIC	#1, @CSR	
800	003144	104000			HLT		;ERROR
801	003146	005777	175632		T18B: TST	@CTR	
802	003152	001401			BEQ	+.4	
803	003154	104000			HLT		;ERROR
804							
805					:EXT FREQ.		
806	003156	104400			T19: SCOPE		
807	003160	032777	000001	175656	BIT	#1, @SR	
808	003166	001033			BNE	T20	
809	003170	005077	175604		CLR	@CSR	
810	003174	012777	177776	175600	MOV	#-2, @CSB	
811	003202	012777	000027	175570	MOV	#27, @CSR	;UP COUNT, EXT FREQ, GO
812	003210	013737	001032	001020	MOV	@DEL4, @TEMP	
813	003216	105777	175556		T19A: TSTB	@CSR	
814	003222	100411			BMI	T19B	
815	003224	062737	000001	001020	ADD	#1, @TEMP	
816	003232	001371			BNE	T19A	
817	003234	042777	000001	175536	BIC	#1, @CSR	
818	003242	104000			HLT		;ERROR,
819	003244	000005			RESET		
820	003246	005777	175532		T19B: TST	@CTR	
821	003252	001401			BEQ	+.4	


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822 003254 104000 HLT ;ERROR
823 ;TEST THAT INTERRUPT OCCURS TO PROPER VECTOR WITH PROCESSOR PRIORITY 4
824 003256 104400 T20: SCOPE
825 003260 012737 000200 177776 MOV #200,CC ;SET PROCESSOR PRIORITY 4
826 003266 005077 175516 CLR @CKVS ;CLEAR INTERRUPT RETURN STATUS
827 003272 005077 175502 CLR @CSR
828 003276 012777 000002 175476 MOV #2,@CSB
829 003304 012777 003346 175474 MOV #T20A,@CKV ;SET UP INTERRUPT RETURN VECTOR
830 003312 012777 000101 175460 MOV #101,@CSR ;ENABLE INTERRUPT
831 003320 013737 001024 001020 MOV @DEL1,@TEMP
832 003326 005237 001020 IS: INC @TEMP
833 003332 001375 BNE IS
834 003334 042777 000001 175436 BIC #1,@CSR
835 003342 104000 HLT ;ERROR, INTERRUPT FAILED TO OCCUR.
836 003344 000420 BR T21
837 003346 017737 175426 001020 T20A: MOV @CSR,@TEMP
838 003354 105737 001020 TSTB @TEMP
839 003360 100401 BMI .+4
840 003362 104000 HLT ;DONE NOT SET ON INT.
841 003364 032737 000001 001020 BIT #1,@TEMP
842 003372 001401 BEQ .+4
843 003374 104000 HLT ;RUN NOT CLEARED
844 003376 005077 175376 CLR @CSR
845 003402 012706 000776 MOV #BUFF,%6
846 ;TEST THAT INTERRUPT OCCURS WITH PROCESSOR PRIORITY 5
847 003406 104400 T21: SCOPE
848 003410 012737 000240 177776 MOV #240,CC ;SET PROCESSOR PRIORITY 5
849 003416 012777 003472 175362 MOV #T21A,@CKV ;SET UP INTERRUPT RETURN STATUS
850 003424 005077 175350 CLR @CSR
851 003430 012777 000002 175344 MOV #2,@CSB
852 003436 012777 000101 175334 MOV #101,@CSR ;ENABLE INTERRUPT
853 003444 013737 001024 001020 MOV @DEL1,@TEMP
854 003452 005237 001020 IS: INC @TEMP
855 003456 001375 BNE IS
856 003460 042777 000001 175312 BIC #1,@CSR
857 003466 104000 HLT ;ERROR, INTERRUPT FAILED TO OCCUR
858 003470 000404 BR T22
859 003472 005077 175302 T21A: CLR @CSR ;RETURN HERE AFTER INTERRUPT
860 003476 012706 000776 MOV #BUFF,%6
861 ;TEST THAT INTERRUPT IS INHIBITED WITH PROCESSOR PRIORITY 6
862 003502 104400 T22: SCOPE
863 003504 012737 000300 177776 MOV #300,CC ;SET PROCESSOR PRIORITY 6
864 003512 012777 003562 175266 MOV #T22A,@CKV ;SET UP INTERRUPT RETURN
865 003520 005077 175254 CLR @CSR
866 003524 012777 000002 175250 MOV #2,@CSB
867 003532 012777 000101 175240 MOV #101,@CSR ;INTERRUPT ENABLE
868 003540 013737 001024 001020 MOV @DEL1,@TEMP
869 003546 005237 001020 IS: INC @TEMP
870 003552 001375 BNE IS
871 003554 005077 175220 CLR @CSR
872 003560 000406 BR T23
873 003562 042777 000001 175210 T22A: BIC #1,@CSR
874 003570 104000 HLT ;ERROR, INT SHOULDN'T HAVE OCCURRED
875 003572 012706 000776 MOV #BUFF,%6
876
877 ;TEST SINGLE INTERRUPT (MODE 0) ON OVERFLOW

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878 003576 104400 T23: SCOPE
879 003600 012737 000200 177776 MOV #200,CC ;SET PROCESSOR PRIORITY 4
880 003606 005077 175166 CLR JCSR
881 003612 012777 177776 175162 MOV #-2,JCSB
882 003620 012777 003662 175160 MOV #T23A,JCKV ;SET INTERRUPT RETURN
883 003626 012777 000121 175144 MOV #121,JCSR ;INTERRUPT ENABLE, UP COUNT, 100 KHZ, GO
884 003634 013737 001024 001020 MOV J#DEL1,J#TEMP
885 003642 062737 000001 001020 T23AA: ADD #1,J#TEMP ;WASTE TIME
886 003650 001374 BNE T23AA
887 003652 042777 000001 175120 BIC #1,JCSR
888 003660 104000 HLT ;ERROR, INTERRUPT FAILED TO OCCUR.
889 003662 005077 175112 T23A: CLR JCSR ;RETURN HERE AFTER INTERRUPT.
890 003666 012706 000776 MOV #BUFF,%6 ;RESET STACK
891 ;TEST REPEATED INTERRUPT (MODE 1).
892 003672 104400 T24: SCOPE
893 003674 012737 177700 001016 MOV #-100,TEMP1 ;SET UP COUNTER FOR INTER
894 003702 012777 003754 175076 MOV #T24B,JCKV ;SET INTERRUPT RETURN
895 003710 012777 000010 175064 MOV #10,JCSB ;SET UP COUNT SET BUFFER
896 003716 012777 000111 175054 MOV #111,JCSR ;INTERRUPT ENABLE, REPEATED INTERRUPTS, 100 KHZ,
897 003724 013737 001024 001020 T24A: MOV J#DEL1,J#TEMP
898 003732 062737 000001 001020 ADD #1,J#TEMP
899 003740 001374 BNE -6
900 003742 042777 000001 175030 BIC #1,JCSR
901 003750 104000 HLT ;ERROR, INTERRUPT FAILED TO OCCUR
902 003752 000406 BR T24C
903 003754 022626 T24B: CMP (6)+(6)+ ;POP STACK
904 003756 005237 001016 INC TEMP1 ;DONE 100 INTERRUPTS?
905 003762 001360 BNE T24A ;NO
906 003764 005077 175010 CLR JCSR ;CLEAR CLOCK
907
908
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910
911 ;SYNCHRONIZATION TEST
912 ;NO. 1 FOR
913 ;KW11-P BOARDS THAT
914 ;ARE REV F OR GREATER
915
916
917 003770 104400 T24C: SCOPE
918 003772 005003 CLR %3 ;
919 003774 032777 000020 175042 BIT #20,JSR ;
920 004002 001002 BNE 1$ ;
921 004004 000137 004244 JMP T25 ;
922 004010 012777 010000 174764 1$: MOV #10000,JCSB ;LOAD COUNTER
923 004016 012777 000001 174754 MOV #1,JCSR ;GO COUNT DOWN, 100 KHZ
924 004024 017700 174754 MOV JCTR,%0 ;SAVE CTR
925 004030 020027 010000 CMP %0,#10000 ;DID COUNT INCREASE?
926 004034 101404 BLOS 2$ ;BRANCH IF OK TO 1$
927 004036 010037 001020 MOV %0,J#TEMP ;
928 004042 104000 HLT ;SYNC ERROR
929 004044 000404 BR T24D ;END TEST
930 004046 005077 174726 2$: CLR JCSR ;CLR CSR
931 004052 005203 INC %3 ;NO OF TIMES THROUGH PROGRAM DETECTS 2(16)
932 004054 001355 BNE 1$ ;2(16) YET, IF NOT GO BACK TO LOOP 1
933

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935
936           ;SYNCHRONIZATION TEST
937           ;NO. 2 FOR KW11-P
938           ;BOARDS THAT ARE
939           ;REV F OR GREATER
940
941
942 004056 104400           T24D:  SCOPE
943 004060 017746 174722  MOV      @CKV,-(%6)           ;SAVE CLOCK VECTOR
944 004064 012777 000340 002472  MOV      @340,@PSW           ;PS=7 STOPS ALL INTRS
945 004072 005037 004226           CLR      TIKTIK             ;CLEAR CLOCK COUNTER
946 004076 005037 006556           CLR      CNT                ;CLEAR ITERATION COUNT
947 004102 012777 004220 174676  MOV      @CLKSER,@CKV       ;SETUP INTR SERVICE RTN
948 004110 012777 000300 174672  MOV      @300,@CKVS         ;SETUP INTR PSW
949 004116 012777 000010 174656  MOV      @10,@CSB           ;KW11 COUNT = 10
950 004124 012777 000111 174646  MOV      @111,@CSR         ;SET TO RUN @100KH
951                                     ;INTR ENABLE & COUNT DOWN
952                                     ;AND REPEAT INTR MODE
953
954 004132 012777 000340 002424  LOOP:  MOV      @340,@PSW           ;PS=7 STOPS ALL INTRS
955 004140 004737 004230           JSR      PC,TYPE            ;100MS DELAY @PR7
956 004144 005077 002414           CLR      @PSW               ;PS=0 ALLOWS INTRS
957 004150 013701 004226           MOV      TIKTIK,R1          ;GET CURRENT CLK COUNT
958 004154 004737 004230           JSR      PC,TYPE            ;100MS DELAY @PRO
959 004160 023701 004226           CMP      TIKTIK,R1          ;ANY INTRS DURING DELAY?
960 004164 001001           BNE      @15                 ;IF YES, GO TO 15
961 004166 104000           HLT                          ;ELSE THERE WAS AN ERROR
962                                     ;CHECK FOR JUMPERS ON THE
963                                     ;KW11-P BOARD NEAR I.C.
964                                     ;LOCATIONS E41 & E51 ON REV F
965                                     ;BOARD & GREATER ONLY
966
967 004170 005237 006556           15:  INC      CNT                ;120 ITERATIONS?
968 004174 022737 000170 006556  CMP      @120.,CNT          ;IF NOT, GO BACK TO LOOP
969 004202 001353           BNE      LOOP                ;ELSE RESTORE THE VECTOR
970 004204 012677 174576           MOV      (%6)+,@CKV         ;CLEAR CONTROL REG
971 004210 005077 174564           CLR      @CSR               ;AND GO TO NEXT TEST
972 004214 000137 004244           JMP      T25
973
974 004220           CLKSER:  INC      TIKTIK           ;INC CLK COUNTER
975 004220 005237 004226           CLKXIT:  RTI                ;ELSE EXIT RTN
976 004224
977 004224 000002
978
979 004226 000000           TIKTIK:  0
980
981 004230 105777 174560           TYPE:  TSTB  @TCSR           ;READY TO SEND
982 004234 100375           BPL      TYPE                ;BR IF NOT
983 004236 110077 174550           MOVB    RD,@TDBR            ;SEND THEM A MESSAGE
984 004242 000207           RTS      PC
985
986
987
988
989

```

```

990          :TEST 100 KHZ REPEATABILITY
991 004244 104400          †25: SCOPE
992 004246 032777 000004 174570 BIT #4, JSR          ;ARE TWO CLK'S PRESENT
993 004254 001002          BNE 3$          ;BRANCH IF SW#2 IS UP
994 004256 000137 004720 JMP T27          ;EXIT IF ONLY ONE CLK
995 004262 005077 174512          CLR @CSR
996 004266 012777 000000 174506 3$: MOV #0, @CSB          ;SET CTR
997 004274 012777 000021 174476 MOV #21, @CSR          ;COUNT UP 100KHZ GO
998 004302 004537 004376 JSR R5, DELY          ;GO TO DELAY SUBROUTINE
999 004306 105777 174466 TSTB @CSR          ;TEST DONE BIT SET
1000 004312 100001          BPL 1$
1001 004314 104000          HLT
1002 004316 017737 174462 001020 1$: MOV @CTR, @TEMP          ;DONE BIT SET TOO SOON
1003 004324 005077 174450 CLR @CSR          ;DONE NOT SET SO SAVE CTR
1004 004330 012777 000000 174444 MOV #0, @CSB
1005 004336 012777 000021 174434 MOV #21, @CSR
1006 004344 004537 004376 JSR R5, DELY
1007 004350 105777 174424 TSTB @CSR
1008 004354 100001          BPL 2$
1009 004356 104000          HLT
1010 004360 017737 174420 001016 2$: MOV @CTR, @TEMP1          ;HERE WE ARE SAVING SEC CNT
1011 004366 004537 004426 JSR R5, CACL          ;GO DETERMINE ACCURACY OF CNT'S
1012 004372 104000          HLT
1013 004374 000432          BR T25A
1014
1015 004376 005077 002120          DELY: CLR @CSR1          ;DELAY SUBROUTINE
1016 004402 012777 001130 002110 MOV #1130, @CSB1
1017 004410 012777 000021 002104 MOV #21, @CSR1
1018 004416 105777 002100 1$: TSTB @CSR1          ;WAIT 600 MIL.
1019 004422 100375          BPL 1$
1020 004424 000205          RTS R5
1021
1022 004426 013700 001020          CACL: MOV @TEMP, R0          ;COMPARE CTR1 WITH CTR2
1023 004432 013701 001016 MOV @TEMP1, R1
1024 004436 160001          SUB R0, R1
1025 004440 100001          BPL 1$
1026 004442 005401          NEG R1
1027 004444 022701 000005 1$: CMP #5, R1          ;DIFFERENCE MUST BE LESS THAN 5
1028 004450 002401          BLT 2$
1029 004452 005725          TST (R5)+          ;UPDATE RETURN
1030 004454 010137 001020 2$: MOV R1, TEMP          ;DEFRENCE FOR PRINT OUT
1031 004460 000205          RTS R5
1032
1033          :TEST 10 KHZ REPEATABILITY
1034          :THIS TEST IS THE SAME AS T25 EXCEPT IT IS
1035          :FOR 10KHZ.
1036          †25A: SCOPE
1037 004462 104400          CLR @CSR
1038 004464 005077 174310 MOV #0, @CSB
1039 004470 012777 000000 174304 MOV #23, @CSR
1040 004476 012777 000023 174274 JSR R5, DELY
1041 004504 004537 004376 JSR R5, DELY
1042 004510 105777 174264 TSTB @CSR
1043 004514 100001          BPL 1$
1044 004516 104000          HLT
1045 004520 017737 174260 001020 1$: MOV @CTR, @TEMP
1045 004526 005077 174246 CLR @CSR

```



```

1046 004532 012777 000000 174242      MOV      #0, @CSB
1047 004540 012777 000023 174232      MOV      #23, @CSR
1048 004546 004537 004376      JSR      R5, DELY
1049 004552 105777 174222      TSTB    @CSR
1050 004556 100001      BPL     2$
1051 004560 104000      HLT
1052 004562 017737 174216 001016 2$:      MOV      @CTR, @TEMP1
1053 004570 004537 004426      JSR      R5, CACL
1054 004574 104000      HLT

```

```

;TEST LINE REPEATABILITY
;THIS TEST IS THE SAME AS T25 EXCEPT IT IS
;FOR LINE FREQ.

```

```

1059 004576 104400      T26:     SCOPE
1060 004600 005737 006232      TST      @XORFLG
1061 004604 100445      BMI     T27
1062 004606 005077 174166      CLR     @CSR
1063 004612 012777 000000 174162      MOV      #0, @CSB
1064 004620 012777 000025 174152      MOV      #25, @CSR
1065 004626 004537 004376      JSR      R5, DELY
1066 004632 105777 174142      TSTB    @CSR
1067 004636 100001      BPL     1$
1068 004640 104000      HLT
1069 004642 017737 174136 001020 1$:      MOV      @CTR, @TEMP
1070 004650 005077 174124      CLR     @CSR
1071 004654 012777 000000 174120      MOV      #0, @CSB
1072 004662 012777 000025 174110      MOV      #25, @CSR
1073 004670 004537 004376      JSR      R5, DELY
1074 004674 105777 174100      TSTB    @CSR
1075 004700 100001      BPL     2$
1076 004702 104000      HLT
1077 004704 017737 174074 001016 2$:      MOV      @CTR, @TEMP1
1078 004712 004537 004426      JSR      R5, CACL
1079 004716 104000      HLT

```

```

;TEST ERROR (BIT 15) TO SET WHEN INTERRUPT IS NOT SERVICED IN REPEAT MODE

```

```

1081 004720 104400      T27:     SCOPE
1082 004722 005077 174052      CLR     @CSR
1083 004726 012737 000340 177776      MOV      #340, CC
1084 004734 012777 000002 174040      MOV      #2, @CSB
1085 004742 012777 000111 174030      MOV      #111, @CSR
1086 004750 013737 001024 001020      MOV      @DEL1, @TEMP
1087 004756 062737 000001 001020      ADD     #1, @TEMP
1088 004764 001374      BNE     -6
1089 004766 005777 174006      TST     @CSR
1090 004772 100404      BMI     1$
1091 004774 042777 000001 173776      BIC     #1, @CSR
1092 005002 104000      HLT
1093 005004 005077 173770 1$:      CLR     @CSR
1094 005010 005777 173764      TST     @CSR
1095 005014 100001      BPL     +4
1096 005016 104000      HLT

```

```

;SET PROCESSOR PRIORITY 7
;SET COUNTER FOR FAST INTERRUPTS
;INT'EN, REPEATED INT, DOWN COUNT, 100 KHZ, GO

```

```

;ERROR, ERROR (BIT 15) NOT SET

```

```

;ERR, FAILED TO CLEAR WHEN REF.

```

```

;TEST BIT 15 IS CLEARED BY INIT

```

```

1097 005020 104400      T27A:    SCOPE
1098 005022 012737 000340 177776      MOV      #340, CC
1099 005030 012777 000002 173744      MOV      #2, @CSB
1100 005036 012777 000111 173734      MOV      #111, @CSR

```

1102	005044	013737	001024	001020		MOV	2#DEL1,2#TEMP	
1103	005052	062737	000001	001020		ADD	#1,2#TEMP	
1104	005060	001374				BNE	-6	
1105	005062	005777	173712			TST	2CSR	
1106	005066	100404				BMI	15	
1107	005070	042777	000001	173702		BIC	#1,2CSR	
1108	005076	104000				HLT		;BIT 15 NOT SET
1109	005100	000005			15:	RESET		
1110	005102	005777	173672			TST	2CSR	
1111	005106	100001				BPL	+.4	
1112	005110	104000				HLT		;BIT 15 NOT CLEARED BY RESET
1113	005112	104400				SCOPE		
1114								
1115								
1116	005114	012777	000207	173670	:BELL ON PASS COMPLETE	MOV	#207,2DDBR	
1117	005122	105777	173666		TSTEND:	TSTB	2CSR	
1118	005126	100375				BPL	-4	
1119	005130	012777	000000	173654		MOV	#0,2DDBR	;SEND A NULL CHAR.
1120	005136	105777	173652			TSTB	2CSR	
1121	005142	100375				BPL	-4	
1122	005144	013702	000042			MOV	2#42,%2	
1123	005150	001405				BEQ	TRPA	
1124	005152	000005				RESET		
1125	005154	004712			LOGICAL:	JSR	%7,(2)	
1126	005156	000240				NOP		
1127	005160	000240				NOP		
1128	005162	000240				NOP		
1129	005164	000137	001130		TRPA:	JMP	BEGIN	

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005170 012706 000776
 005174 004737 011566
 005200 013777 001010 173600
 005206 012777 000002 173574
 005214 012737 005562 000024
 005222 000005
 005224 012777 141520 173550
 005232 012700 177772
 005236 012701 177754
 005242 012777 000111 173530
 005250 000001
 005252 005201
 005254 001375
 005256 105777 173532
 005262 100375
 005264 012777 000207 173520
 005272 005200
 005274 001360
 005276 042777 000101 173474
 005304 012777 011610 173470
 005312 012700 177772
 005316 012701 177754
 005322 012777 000113 173450
 005330 000001
 005332 005201
 005334 001375
 005336 105777 173452
 005342 100375
 005344 012777 000207 173440
 005352 005200
 005354 001360
 005356 042777 000101 173414
 005364 005737 006232
 005370 100677
 005372 012737 001130 005550
 005400 032777 000002 173436
 005406 001403
 005410 012737 000764 005550
 005416 013777 005550 173356
 005424 012700 177772
 005430 012777 000115 173342
 005436 000001
 005440 105777 173350
 005444 100375

```

.SBTTL          TIMING TEST
;RING TELETYPE BELL AT 10 SECOND INTERVALS USING REPEATED INTERRUPT MODE
;1ST MINUTE = 100 KHZ
;2ND MINUTE = 10 KHZ
;3RD MINUTE = LINE
;4TH MINUTE = EXTERNAL

BEGIN1: MOV      #BUFF,%6
        JSR      %7,SWADJ      ;HAS THIS CPU HAVE A SWITCH REG.?
        MOV      CKVS,ACKV
        MOV      #RTI,ACKVS
        MOV      #PWR2,24      ;INIT POWER FAIL POINTER
        RESET
;100 KHZ
        MOV      #50000.,ACSB  ;INIT COUNT SET BUFFER FOR .5 SECONDS
        MOV      #-6,%0        ;COUNT 6(10 SECOND) INTERVALS
T28:    MOV      #-20,%1       ;COUNT 20(.5 SECOND) INTERVALS
        MOV      #111,ACSR     ;100 KHZ, REPEATED INTERRUPTS, INTERRUPT ENABLE, GO
T28A:   WAIT
        INC      %1           ;DONE 10 SECONDS?
        BNE     T28A         ;NO
        TSTB    @TCSR
        BPL     .-4
        MOV      #207,@TDBR
        INC     %0           ;DONE 6 TIMES?
        BNE     T28         ;NO
        BIC     #101,ACSR    ;YES DISABLE INTERRUPTS
;10 KHZ
        MOV      #5000.,ACSB  ;INIT COUNT SET BUFFER FOR .5 SECONDS
        MOV      #-6,%0        ;COUNT 6(10SECOND) INTERVALS
T29:    MOV      #-20,%1       ;COUNT 20(.5 SECOND) INTERVALS
        MOV      #113,ACSR     ;10 KHZ, REPEATED INTERRUPTS, INTERRUPT ENABLE, GO
T29A:   WAIT
        INC      %1           ;DONE 10 SECONDS?
        BNE     T29A         ;NO
        TSTB    @TCSR       ;YES, RING BELL
        BPL     .-4
        MOV      #207,@TDBR
        INC     %0           ;DONE 6 TIMES?
        BNE     T29         ;NO
        BIC     #101,ACSR    ;YES, DISABLE INTERRUPTS
;SET UP FOR 10 SECONDS AT LINE FREQ.
        TST     @#XORFLG
        BMI     BEGIN1
        MOV      #600.,LINE
        BIT     #2,ISR
        BEQ     .+10
        MOV      #500.,LINE
;LINE
        MOV      LINE,ACSB     ;INITIALZE COUNT SET BUFFER FOR 10 SECONDS
        MOV      #-6,%0        ;COUNT 6 (10 SECOND) INTERVALS
T30:    MOV      #115,ACSR     ;LINE, REPEATED INTERRUPTS, INTERRUPT ENABLE, GO
        WAIT
        TSTB    @TCSR
        BPL     .-4
    
```

1186	005446	012777	000207	173336	MOV	#207, @TDBR	:RING BELL
1187	005454	005200			INC	%0	:DONE 6 TIMES
1188	005456	001367			BNE	T30	:NO
1189	005460	042777	000101	173312	BIC	#101, @CSR	:YES--DISABLE INTERRUPTS
1190	005466	032777	000001	173350	BIT	#1, @SR	:
1191	005474	001235			BNE	BEGIN1	:
1192							:
1193	005476	013777	005550	173276	MOV	LINE, @CSB	:INITIALZE COUNT SET BUFFER FOR 10 SECONDS
1194	005504	012700	177772		MOV	#-6, %0	:COUNT 6 (10 SECOND) INTERVALS
1195	005510	012777	000117	173262	MOV	#117, @CSR	:EXT FREQ, REPEATED INTERRUPTS, INTERRUPT ENABLE , GO
1196	005516	000001			T31: WAIT		
1197	005520	105777	173270		TSTB	@TCSR	
1198	005524	100375			BPL	.-4	
1199	005526	012777	000207	173256	MOV	#207, @TDBR	:RING BELL
1200	005534	005200			INC	%0	:DONE 6 TIMES
1201	005536	001367			BNE	T31	:NO
1202	005540	042777	000100	173232	BIC	#100, @CSR	:YES, DISABLE INTERRUPTS
1203	005546	000610			BR	BEGIN1	:REPEAT
1204	005550	001130			LINE:	600.	

1205					.SBTTL	SUBROUTINES	
1206					:POWER FAIL HANDLERS		
1207	005552	012737	001130	005626	PWRF1: MOV	#BEGIN, PWRRTN	
1208	005560	000403			BR	PWRDWN	
1209	005562	012737	005170	005626	PWRF2: MOV	#BEGIN1, PWRRTN	
1210	005570	012737	005600	000024	PWRDWN: MOV	#PWRUP, 24	
1211	005576	000000			HALT		
1212	005600	012706	000776		PWRUP: MOV	#BUFF, %6	
1213	005604	005000			CLR	%0	
1214	005606	005200			INC	%0	
1215	005610	001376			BNE	.-2	
1216	005612	012702	006416		MOV	#MSGPWR, %2	
1217	005616	004737	006246		JSR	%7, TOP	
1218	005622	000177	000000		JMP	@PWRRTN	
1219	005626	001130			PWRRTN: BEGIN		
1220							
1221					:ENTERED WITH SYSTEM TRAP CALL (HLT)		
1222					:PRINT PC, STATUS REGISTER, COMAND REGISTER, BYTE COUNT, CURRENT ADDRESS, DATA		
1223	005630	037727	173210	020000	PRINT: BIT	JSR, #20000	:TEST FOR INHIBIT PRINT OUT
1224	005636	001401			BEQ	+.4	:BRANCH TO PRINT
1225	005640	000002			RTI		:INHIBIT, RETURN TO MAIN STREAM
1226	005642	012702	006350		MOV	#MSG1, %2	
1227	005646	005737	005744		TST	PRINT1	
1228	005652	001402			BEQ	+.6	
1229	005654	012702	006412		MOV	#MSG2, %2	
1230	005660	004737	006246		JSR	%7, TOP	:PRINT ERROR HEADING
1231	005664	005237	005744		INC	PRINT1	
1232	005670	011602			MOV	(6), %2	
1233	005672	162702	000002		SUB	#2, %2	
1234	005676	004737	005746		JSR	%7, OCTPRT	:PRINT PC
1235	005702	017702	173072		MOV	@CSR, %2	:PRINT STATUS REGISTER
1236	005706	004737	005746		JSR	%7, OCTPRT	:PRINT COUNTER
1237	005712	017702	173066		MOV	@CTR, %2	:PRINT TEMP
1238	005716	004737	005746		JSR	%7, OCTPRT	:CHECK SR FOR HALT SWITCH
1239	005722	013702	001020		MOV	TEMP, %2	
1240	005726	004737	005746		JSR	%7, OCTPRT	
1241	005732	005777	173106		TST	JSR	
1242	005736	100001			BPL	+.4	:HALT ON ERROR UP
1243	005740	000000			HALT		:RETURN TO MAINLINE
1244	005742	000002			RTI		
1245	005744	000000			PRINT1: 0		
1246					:PRINT OCTAL VALUE IN REGISTER2		
1247	005746	012737	000060	006060	OCTPRT: MOV	#'0, CHAR	:INITIALIZE 1ST NUMBER AS 0
1248	005754	005702			TST	%2	:IS VALUE POSITIVE
1249	005756	100003			BPL	OCT1	:YES PRINT 0
1250	005760	012737	000061	006060	MOV	#'1, CHAR	:NO PRINT 1
1251	005766	004737	006062		OCT1: JSR	%7, OCTP	
1252	005772	006102			ROL	%2	
1253	005774	006102			ROL	%2	
1254	005776	012737	177773	006056	OCT2: MOV	#-5, OCT	:COUNT 5 DIGITS
1255	006004	006102			ROL	%2	
1256	006006	006102			ROL	%2	
1257	006010	006102			ROL	%2	
1258	006012	010237	006060		MOV	%2, CHAR	:SAVE DIGIT
1259	006016	042737	177770	006060	BIC	#177770, CHAR	:CLEAR OTHER BITS
1260	006024	052737	000060	006060	BIS	#60, CHAR	:MAKE ASCII DIGIT

```

1261 006032 006002          ROR      %2
1262 006034 004737 006062    JSR      %7, OCTP          ;PRINT
1263 006040 006102          ROL      %2
1264 006042 005237 006056    INC      OCT              ;+1 TO DIGIT COUNT
1265 006046 001356          BNE     OCT2             ;NOT DONE
1266 006050 004737 006100    JSR      %7, SP3
1267 006054 000207          RTS      %7              ;EXIT
1268 006056 000000          OCT:    0
1269 006060 000000          CHAR:  0
1270 006062 105777 172726    OCTP:  TSTB      @TCSR
1271 006066 100375          BPL     -4              ;WAIT FOR READY
1272 006070 013777 006060 172714  MOV     CHAR, @TDBR      ;PRINT
1273 006076 000207          RTS      %7
1274          ;TYPE 3 SPACES
1275 006100 012702 006112    SP3:   MOV     #SP3A, %2
1276 006104 004737 006246    JSR      %7, TOP
1277 006110 000207          RTS      %7
1278 006112 020057 027440    SP3A:  .ASCII  ;/ /;
1279          .EVEN
1280
1281 006116 022606          SCOPEB: CMP     (%b)+, %b          ;REPOSITION THE STACK
1282 006120 012637 177776    MOV     (%b)+, CC
1283 006124 000177 000114    JMP     @RETURN          ;SCOPE RETURN
1284
1285          ;SCOPE OR/AND ITERATION LOOP FOR EACH TEST
1286 006130 032777 040000 172706  SCOPEC: BIT     #4000, @SR          ;TEST SR FOR SCOPE.
1287 006136 001367          BNE     SCOPEB          ;YES SCOPE
1288 006140 005737 006232    TST     @#XORFLG
1289 006144 100011          BPL     1$
1290 006146 013746 000004    MOV     @#4, -(%b)
1291 006152 012737 006234 000004  MOV     #XORA, @#4
1292 006160 005737 177060    TST     @#177060
1293 006164 012637 000004    MOV     (%b)+, @#4
1294 006170 032777 004000 172646  1$:    BIT     #4000, @SR          ;RESTORE STACK
1295 006176 001007          BNE     SCOPEG          ;NO - TEST FOR ITERATION
1296 006200 023737 006230 001022  CMP     SCOPEF, ICOUNT    ;INHIBIT ITERATION
1297 006206 001403          BEQ     SCOPEG
1298 006210 005237 006230    INC     SCOPEF
1299 006214 000740          BR     SCOPEB
1300 006216 005037 006230    SCOPEG: CLR    SCOPEF
1301 006222 011637 006244    MOV     @%b, RETURN
1302 006226 000002          RTI
1303 006230 000000          SCOPEF: 0
1304 006232 000000          XORFLG: 0
1305 006234 022626          XORA:  CMP     (%b)+, (%b)+
1306 006236 012637 000004    MOV     (%b)+, @#4
1307 006242 000725          BR     SCOPEB
1308 006244 001130          RETURN: BEGIN          ;ADDRESS OF LAST TEST
1309          ;MOV ADDRESS OF MESSAGE TO REGISTER 2
1310          ;THEN JSR %7, TOP
1311 006246 142777 000177 172540  TOP:   BICB     #177, @TCSR          ;CLR INT FLAG
1312 006254 112237 006346    MOV     (2)+, EOMK        ;MOVE IN EOM MARKER
1313 006260 121237 006346    TOP1:  CMP     @%2, EOMK      ;COMPARE FOR EOM
1314 006264 001001          BNE     +4              ;NO
1315 006266 000207          RTS      %7              ;YES, EXIT
1316 006270 121227 000100    CMP     @%2, #'a

```


1317	006274	001406			BEQ	TOP2		
1318	006276	105777	172512		TSTB	@TCSR		;CK TTY
1319	006302	100375			BPL	-4		;WAIT FOR DONE
1320	006304	112277	172502		MOVB	(2)+,@TDBR		;MOVE CHARACTER
1321	006310	000763			BR	TOP1		;BRANCH BACK
1322	006312	105777	172476		TOP2: TSTB	@TCSR		
1323	006316	100375			BPL	-4		
1324	006320	112777	000215	172464	MOVB	#215,@TDBR		;SEND CARRIAGE RETURN
1325	006326	105777	172462		TSTB	@TCSR		
1326	006332	100375			BPL	-4		
1327	006334	112777	000212	172450	MOVB	#212,@TDBR		;SEND LINE FEED
1328	006342	005202			INC	%2		;INCRMTN R2
1329	006344	000745			BR	TOP1		;NO EOM, SO LOOP
1330	006346	000			EOMK:	.BYTE	0	
1331		006350				.EVEN		
1332	006350	040057	020040	041520	MSG1:	.ASCII	;/@ PC STATUS COUNTER TEMP@/;	
1333	006356	020040	020040	052123				
1334	006364	052101	051525	020040				
1335	006372	047503	047125	042524				
1336	006400	020122	052040	046505				
1337	006406	040120	057					
1338		006412				.EVEN		
1339	006412	040057	057		MSG2:	.ASCII	;/@/;	
1340		006416				.EVEN		
1341	006416	040057	042522	052123	MSGPWR:	.ASCII	;/@RESTARTING AFTER A POWER FAILURE@/;	
1342	006424	051101	044524	043516				
1343	006432	040440	052106	051105				
1344	006440	040440	050040	053517				
1345	006446	051105	043040	044501				
1346	006454	052514	042522	040100				
1347	006462	057						
1348		006464				.EVEN		
1349	006464	040057	047531	020125	XORM:	.ASCII	;/@YOU ARE ON AN XOR TESTER@/;	
1350	006472	051101	020105	047117				
1351	006500	040440	020116	047530				
1352	006506	020122	042524	052123				
1353	006514	051105	027500					
1354						.EVEN		
1355						;TIMER FOR KW11-P CLOCK		
1356								
1357	006520	172562			CSB1:	172562		
1358	006522	172560			CSR1:	172560		
1359	006524	172564			CTR1:	172564		
1360	006526	000504			CKV1:	504		
1361	006530	000506			CKVS1:	506		
1362	006532	000000			CLKFLG:	0		
1363	006534	000000			INTFLG:	0		
1364	006536	177566			PDBR:	177566		
1365	006540	177564			PCSR:	177564		
1366	006542	000064			PVEC:	64		
1367	006544	000066			PVECS:	66		
1368	006546	177562			KDBR:	177562		
1369	006550	177560			KCSR:	177560		
1370	006552	000060			KVEC:	60		
1371	006554	000062			KVECS:	62		
1372	006556	000000			CNT:	0		

```

1373 006560 000000
1374 006562 000000
1375      000211
1376      000224
1377 006564 177776
1378 006566 000000
1379 006570 000000
1380 006572 000000
1381 006574 000000
1382 006576 000000
1383 006600 000000
1384 006602 000000
1385 006604 000000
1386 006606 000000
1387 006610 000000
1388 006612 000000
1389 006614 000000
1390 006616 000000
1391 006620 000000
1392 006622 000000
1393 006624 000000
1394 006626 000000
1395 006630      000
1396 006631      000
1397 006632      000
1398 006633      000
1399 006634      000
1400 006635      000
1401 006636      000
1402      006640
1403
1404
1405
1406

```

```

CNT1: 0
CNT8: 0
CTRL1=211
CTRLT=224
PSW: 177776
HRS1: 0
HRS2: 0
MIN1: 0
MIN2: 0
SEC1: 0
SEC2: 0
LST: 0
MST: 0
HRS1A: 0
HRS2A: 0
MIN1A: 0
MIN2A: 0
SEC1A: 0
SEC2A: 0
LSTA: 0
MSTA: 0
TMPSWR: 0
BYT1: .BYTE 0
BYT2: .BYTE 0
BYT3: .BYTE 0
BYT4: .BYTE 0
BYT5: .BYTE 0
BYT6: .BYTE 0
BYT7: .BYTE 0
.EVEN

```

```

:TEMP LOC FOR SOFT-SWR CONTENTS
:LOC FOR 1ST # INPUT VIA TTY
:      " 2ND " " "
:      " 3RD " " "
:      " 4TH " " "
:      " 5TH " " "
:      " 6TH " " "
:      " 7TH " " "

```

```

1407 006640 012706 000776
1408 006644 004737 011566
1409 006650 005077 177710
1410 006654 012737 000000 007614
1411 006662 012737 000131 007622
1412 006670 012700 010272
1413 006674 012701 010312
1414 006700 004537 007160
1415 006704 012737 000043 010422
1416 006712 012737 001217 010452
1417 006720 000137 007174
1418
1419 006724 012706 000776
1420 006730 004737 011566
1421 006734 005077 177624
1422 006740 012737 164217 007614
1423 006746 012737 000133 007622
1424 006754 012700 010272
1425 006760 012701 010332
1426 006764 004537 007160
1427 006770 012737 000000 010422
1428 006776 012737 001130 010452

```

```

K100HZ: MOV #BUFF,%6
        JSR %7,SWADJ ;HAS THIS CPU HAVE A SWITCH REG.?
        CLR @PSW
        MOV #0,CLK+2 ;100KHZ
        MOV #131,CLK1+2
        MOV #TABL,%0
        MOV #TABL1,%1
        JSR %5,@MOVE
        MOV #35,CLK3+2 ;LEAST VALUE
        MOV #655,CLK4+2 ;MOST VALUE
        JMP @INIT

K10HZ:  MOV #BUFF,%6
        JSR %7,SWADJ ;HAS THIS CPU HAVE A SWITCH REG.?
        CLR @PSW
        MOV #-13561,CLK+2 ;10KHZ
        MOV #133,CLK1+2
        MOV #TABL,%0
        MOV #TABL2,%1
        JSR %5,@MOVE
        MOV #0,CLK3+2
        MOV #600,CLK4+2

```


1429	007004	000137	007174		JMP	0#INIT	
1430							
1431	007010	012706	000776	H60Z:	MOV	#BUFF,%6	
1432	007014	004737	011566		JSR	%7,SWADJ	;HAS THIS CPU HAVE A SWITCH REG.?
1433	007020	005077	177540		CLR	0PSW	
1434	007024	012737	177733	007614	MOV	#-45,CLK+2	;60HZ
1435	007032	012737	000135	007622	MOV	#135,CLK1+2	

1436	007040	012700	010272		MOV	#TABL,%0	
1437	007044	012701	010352		MOV	#TABL3,%1	
1438	007050	004537	007160		JSR	%5,@#MOVE	
1439	007054	012737	000000	010422	MOV	#00,CLK3+2	
1440	007062	012737	001130	010452	MOV	#600,CLK4+2	
1441	007070	000137	007174		JMP	@#INIT	
1442							
1443	007074	012706	000776		H502: MOV	#BUFF,%6	
1444	007100	004737	011566		JSR	%7,SWADJ	;HAS THIS CPU HAVE A SWITCH REG.?
1445	007104	005077	177454		CLR	@#SW	
1446	007110	012737	177742	007614	MOV	#-36,CLK+2	:50HZ
1447	007116	012737	000135	007622	MOV	#135,CLK1+2	
1448	007124	012700	010272		MOV	#TABL,%0	
1449	007130	012701	010372		MOV	#TABL4,%1	
1450	007134	004537	007160		JSR	%5,@#MOVE	
1451	007140	012737	000000	010422	MOV	#0,CLK3+2	
1452	007146	012737	001104	010452	MOV	#580,CLK4+2	
1453	007154	000137	007174		JMP	@#INIT	
1454							
1455	007160	012702	177771		MOVE: MOV	#-7,%2	
1456	007164	012120			IS: MOV	(%1)+,(%0)+	
1457	007166	005202			INC	%2	
1458	007170	001375			BNE	IS	
1459	007172	000205			RTS	%5	
1460							
1461	007174	013737	005552	000024	INIT: MOV	PWRFL,24	
1462	007202	012706	000776		MOV	#BUFF,%6	:INITIALIZE
1463	007206	005037	006602		CLR	@#LST	
1464	007212	005037	006604		CLR	@#MST	
1465	007216	012737	000060	006566	MOV	#60,@#HRS1	
1466	007224	012737	000060	006570	MOV	#60,@#HRS2	
1467	007232	012737	000060	006572	MOV	#60,@#MIN1	
1468	007240	012737	000060	006574	MOV	#60,@#MIN2	
1469	007246	012737	000060	006576	MOV	#60,@#SEC1	
1470	007254	012737	000060	006600	MOV	#60,@#SEC2	
1471	007262	012777	010412	171516	MOV	#CLK1,@CKV	
1472	007270	012777	000340	171512	MOV	#340,@CKVS	
1473	007276	012777	007504	177246	MOV	#KINTR,@KVEC	
1474	007304	012777	000200	177242	MOV	#200,@KVECS	
1475	007312	012777	000200	177224	MOV	#200,@PVECS	
1476	007320	012777	000100	177222	MOV	#100,@KCSR	
1477	007326	005037	006532		CLR	@#CLKFLG	
1478	007332	005037	006534		CLR	@#INTFLG	
1479	007336	005077	171436		START: CLR	@CSR	
1480	007342	005077	171434		CLR	@CSB	
1481	007346	032777	000002	171470	WAITA: BIT	#2,@SR	:WAIT LOOP, SW 1 CAUSE WAIT
1482	007354	001401			BEQ	CLKON	
1483	007356	000001			WAITB: WAIT		
1484	007360	032777	000001	171456	CLKON: BIT	#1,@SR	:SW 0 TURNS ON CLK2
1485	007366	001432			BEQ	3S	
1486	007370	032777	000004	171446	BIT	#4,@SR	:SW 2 DETERMINES PRESENCE OF CLOCK 2.
1487	007376	001426			BEQ	3S	
1488	007400	005737	006532		TST	@#CLKFLG	:CLKFLG ALLOW CLK 2 TO BE TURNED ON
1489	007404	001360			BNE	WAITA	:ONLY ONCE
1490	007406	005077	177106		CLR	@CSB1	
1491	007412	012777	007702	177106	MOV	#KOUT,@CKV1	


```

1492 007420 012777 000200 177102      MOV      #200, @CKVSI
1493 007426 012737 177777 006532      MOV      #-1, @CLKFLG
1494 007434 012777 141521 177056      MOV      #141521, @CSB1
1495 007442 012777 000113 177052      MOV      #113, @CSR1      ;TURN ON CLK 2
1496 007450 000137 007356      JMP      WAITB
1497 007454 005037 006532      CLR      @CLKFLG      ;CLEAR CLK 2 IF PRESENT
1498 007460 032777 000004 171356      BIT      #4, @SR
1499 007466 001404      BEQ      4$
1500 007470 005077 177026      CLR      @CSR1
1501 007474 005077 177020      CLR      @CSB1
1502 007500 000137 007346      JMP      WAITA      4$:
1503
1504 007504 017701 177036      KINTR:  MOV      @KDBR, %1      ;KEYBOARD INTERRUPT HANDLER
1505 007510 022701 000207      CMP      #207, %1      ;IS CHAR A ↑G(CONTROL-G)?
1506 007514 001557      BEQ      CNGSWR      ;IF YES, GO TO CNGSWR
1507 007516 022701 000211      CMP      @CTRLI, %1
1508 007522 001404      BEQ      KIN
1509 007524 022701 000224      CMP      @CTRLT, %1
1510 007530 001464      BEQ      KOUT
1511 007532 000002      RTI
1512
1513
1514 007534 005077 171240      KIN:    CLR      @CSR      ;HANDLER FOR CTRL I
1515 007540 005077 171236      CLR      @CSB      ;SETUP TIME OF DAY
1516 007544 012737 177772 006556      MOV      #-6, @CNT
1517 007552 012737 006566 006560      MOV      @HRS1, @CNT1      ;INPUT
1518 007560 005037 006602      CLR      LST
1519 007564 005037 006604      CLR      MST
1520 007570 012777 007630 176754      MOV      @KINI, @KVEC
1521 007576 000002      RTI
1522
1523 007600 012777 007504 176744      KINI2:  MOV      @KINTR, @KVEC      ;AWAIT A CHAR TO START
1524 007606 017701 176734      MOV      @KDBR, %1
1525 007612 012777 000000 171162      CLK:    MOV      #0, @CSB      ;CLK 1
1526 007620 012777 000131 171152      CLK1:  MOV      #131, @CSR
1527 007626 000002      RTI
1528
1529 007630 013704 006560      KINI:  MOV      @CNT1, %4      ;STORE TIME OF DAY
1530 007634 017701 176706      MOV      @KDBR, %1
1531 007640 042701 000300      BIC      #300, %1
1532 007644 010124      MOV      %1, (%4)+
1533 007646 010437 006560      MOV      %4, @CNT1
1534 007652 005237 006556      INC      @CNT
1535 007656 001003      BNE      1$
1536 007660 012777 007600 176664      MOV      @KINI2, @KVEC
1537 007666 000002      RTI      1$:
1538
1539 007670 017737 176652 007700      HOLDIT: MOV      @KDBR, @HOLD      ;DUMMY INTERRUPT SERVICE ROUTINE
1540 007676 000002      RTI
1541
1542 007700 000000      HOLD:  0
1543
1544 007702 005037 006534      KOUT:  CLR      @INTFLG      ;INPUT HANDLER FOR CTRL T
1545 007706 012777 007670 176636      MOV      @HOLDIT, @KVEC      ;SET DUMMY VECTOR
1546 007714 012700 006566      MOV      @HRS1, %0      ;GET TIME OF DAY INTO
1547 007720 012703 006606      MOV      @HRS1A, %3      ;WORK AREA

```

1548	007724	012704	177770		MOV	#-10,%4	
1549	007730	012023		1S:	MOV	(%0)+,(%3)+	
1550	007732	005204			INC	%4	
1551	007734	001375			BNE	1S	
1552	007736	017701	171042		MOV	QCTR,%1	
1553	007742	005737	006534		TST	Q#INTFLG	;SEE IF CLK HAS INTERRUPTED IN THIS TIME
1554	007746	001355			BNE	KOUT	;CALC VALUE OF CTR
1555	007750	005737	007614		TST	Q#CLK+2	;IS CLOCK RUNNING AT 100KHZ ?
1556	007754	001416			BEQ	2S	
1557	007756	163701	007614		SUB	Q#CLK+2,%1	;SUB INIT VALUE
1558	007762	006301			ASL	%1	
1559	007764	006301			ASL	%1	
1560	007766	023727	007614	164217	CMP	Q#CLK+2,#-13561	;IS CLOCK RUNNING AT 10KHZ ?
1561	007774	001405			BEQ	3S	
1562	007776	000301			SWAB	%1	
1563	010000	023727	007614	177742	CMP	Q#CLK+2,#-36	;IS CLOCK RUNNING AT 50HZ ?
1564	010006	001001			BNE	2S	
1565	010010	006301			3S:	ASL	%1
1566	010012	005000			2S:	CLR	%0
1567	010014	005003				CLR	%3
1568	010016	012704	010272		5S:	MOV	#TABL,%4
1569	010022	005701			6S:	TST	%1
1570	010024	100001				BPL	4S
1571	010026	061403				ADD	Q%4,%3
1572	010030	006301			4S:	ASL	%1
1573	010032	005724				TST	(%4)+
1574	010034	005200				INC	%0
1575	010036	022700	000007			CMP	#7,%0
1576	010042	001367				BNE	6S
1577	010044	060337	006624			ADD	%3,Q#MSTA
1578	010050	000137	010706			JMP	Q#CLK2
1579	010054				CNGSWR:		
1580	010054	010246			MOV	%2,-(6)	;SAVE R2
1581	010056	010346			MOV	%3,-(6)	;SAVE R3
1582	010060				SETBYT:		
1583	010060	005037	006626		CLR	TMPSWR	;CLEAR TEMP SWR
1584	010064	005003			CLR	%3	;CLEAR R3
1585	010066	004737	010240		JSR	PC,CRLF	;PRINT <CR><LF>
1586	010072	012702	006630		MOV	#BYT1,%2	;INIT R2 TO 1ST BYTE LOC
1587	010076				CKCSR:		
1588	010076	105777	176446		TSTB	QKCSR	;IS CHAR TYPED?
1589	010102	100375			BPL	CKCSR	;IF NOT WAIT
1590	010104	017701	176436		MOV	QKDBR,%1	;ELSE MOVE THE CHAR TO R1
1591	010110				5S:		
1592	010110	105777	176424		TSTB	QPCSR	
1593	010114	100375			BPL	5S	
1594	010116	010177	176414		MOV	%1,QPDBR	
1595	010122	122701	000225		CMPB	#225,%1	;IS CHAR +U (CONTROL-U)?
1596	010126	001754			BEQ	SETBYT	;IF YES START OVER
1597	010130	122701	000215		CMPB	#215,%1	;ELSE IS IT <CR>?
1598	010134	001412			BEQ	SWDONE	;IF EQUAL GO TO SWDONE
1599	010136	122701	000212		CMPB	#212,%1	;IS IT <LF>?
1600	010142	001407			BEQ	SWDONE	;IF EQUAL GO TO SWDONE
1601	010144	005203			INC	%3	;INDICATE A CHAR INPUTTED
1602	010146	042701	177770		BIC	#177770,%1	;LEAVE ONLY BINARY # IN R1
1603	010152	110122			MOVB	%1,(2)+	;MOVE # TO PROPER BYTE LOC

1604	010154	022702	006636		CMP	#BYT7,%2		: IS R2 PAST BYT6 ADDR?
1605	010160	001346			BNE	CKCSR		: IF NOT, GO BACK FOR ANOTHER CHAR
1606	010162							
1607	010162	005703			TST	%3		: WAS A CHAR TYPED?
1608	010164	001420			BEQ	30\$: IF NOT, EXIT
1609	010166	012703	006630		MOV	#BYT1,%3		: INIT R3 TO 1ST BYTE ADDR
1610	010172			10\$:				
1611	010172	152337	006626		BISB	(3)+,TMP\$WR		: SET LOW 3 BITS OF TMP\$WR
1612	010176	020302			CMP	%3,%2		: IS R3 EQUAL BYTE ADDR IN R2?
1613	010200	001407			BEQ	20\$: IF YES, EXIT
1614	010202	006137	006626		ROL	TMP\$WR		: ELSE
1615	010206	006137	006626		ROL	TMP\$WR		: SHIFT
1616	010212	006137	006626		ROL	TMP\$WR		: NEXT 3 BITS UP
1617	010216	000765			BR	10\$: AND GO GET ANOTHER #
1618	010220			20\$:				
1619	010220	013777	006626	170616	MOV	TMP\$WR,%SR		: SET UP NEW \$WR
1620	010226			30\$:				
1621	010226	012603			MOV	(6)+,%3		: RESTORE R3
1622	010230	012602			MOV	(6)+,%2		: RESTORE R2
1623	010232	004737	010240		JSR	PC,CRLF		: PRINT <CR><LF>
1624	010236	000002			RTI			
1625								
1626	010240							
1627	010240	105777	176274		TSTB	%PCSR		: IS TTY READY?
1628	010244	100375			BPL	CRLF		: IF NOT, WAIT
1629	010246	012777	000215	176262	MOV	#215,%PDBR		: ELSE TYPE <CR>
1630	010254			10\$:				
1631	010254	105777	176260		TSTB	%PCSR		: IS TTY READY?
1632	010260	100375			BPL	10\$: IF NOT, WAIT
1633	010262	012777	000212	176246	MOV	#212,%PDBR		: ELSE TYPE <LF>
1634	010270	000207			RTS	PC		
1635								
1636	010272	000510			TABL:	328.		: TABLE FOR WORK AREA
1637	010274	000244				164.		
1638	010276	000122				82.		
1639	010300	000051				41.		
1640	010302	000024				20.		
1641	010304	000012				10.		
1642	010306	000005				5.		
1643	010310	000003				3.		
1644								
1645	010312	000510			TABL1:	328.		: 100KHZ TIME TABLE
1646	010314	000244				164.		
1647	010316	000122				82.		
1648	010320	000051				41.		
1649	010322	000024				20.		
1650	010324	000012				10.		
1651	010326	000005				5.		
1652	010330	000003				3.		
1653								
1654	010332	000632			TABL2:	410.		: 10KHZ TIME TABLE
1655	010334	000315				205.		
1656	010336	000146				102.		
1657	010340	000063				51.		
1658	010342	000032				26.		
1659	010344	000015				13.		

```

1660 010346 000006
1661 010350 000003
1662
1663 010352 001025
1664 010354 000413
1665 010356 000205
1666 010360 000103
1667 010362 000041
1668 010364 000021
1669 010366 000000
1670 010370 000000
1671
1672 010372 000500
1673 010374 000240
1674 010376 000120
1675 010400 000050
1676 010402 000024
1677 010404 000000
1678 010406 000000
1679 010410 000000
1680

```

```

6.
3.
TABL3: 533.
267.
133.
67.
33.
17.
0.
0.
TABL4: 320.
160.
80.
40.
20.
0.
0.
0.

```

;60HZ TIME TABLE

;50HZ TIME TABLE

```

1681 ;THIS ROUTINE KEEPS THE 24 HOUR
1682 ;TIME OF DAY
1683

```

```

1684 010412 012737 177777 006534
1685 010420 062737 000044 006602
1686 010426 022737 000144 006602
1687 010434 003005
1688 010436 162737 000144 006602
1689 010444 005237 006604
1690 010450 062737 001217 006604
1691 010456 022737 001750 006604
1692 010464 003011
1693 010466 162737 001750 006604
1694 010474 005237 006600
1695 010500 022737 000072 006600
1696 010506 001401
1697 010510 000002
1698 010512 012737 000060 006600
1699 010520 005237 006576
1700 010524 022737 000066 006576
1701 010532 001401
1702 010534 000002
1703 010536 012737 000060 006576
1704 010544 005237 006574
1705 010550 022737 000072 006574
1706 010556 001401
1707 010560 000002
1708 010562 012737 000060 006574
1709 010570 005237 006572
1710 010574 022737 000066 006572
1711 010602 001401
1712 010604 000002
1713 010606 012737 000060 006572
1714 010614 005237 006570
1715 010620 022737 000064 006570

```

```

CLKI: MOV # -1, @INTFLG
CLK3: ADD #36, @LST
CMP #100, @LST
BGT CLK4
SUB #100, @LST
INC @MST
CLK4: ADD #655, @MST
CMP #1000, @MST
BGT 25
SUB #1000, @MST
INC @SEC2
CMP #72, @SEC2
BEQ .+4
25: RTI
MOV #60, @SEC2
INC @SEC1
CMP #66, @SEC1
BEQ .+4
RTI
MOV #60, @SEC1
INC @MIN2
CMP #72, @MIN2
BEQ .+4
RTI
MOV #60, @MIN2
INC @MIN1
CMP #66, @MIN1
BEQ .+4
RTI
MOV #60, @MIN1
INC @HRS2
CMP #64, @HRS2

```

```

;CLOCK INTERRUPT SERVICE ROUTINE
;ADD LSB TO LST
;DID IT OVER FLOW
;YES
;INC MST
;ADD MSB TO MST
;DID IT OVER FLOW
;YES
;INC SECOND
;HAS 10 SECONDS ELAPSED
;YES
;INC MSB OF SECOND
;HAS 60 MIN ELAPSED
;YES
;INC LSB OF MIN
;HAS 10 MIN ELAPSED
;INC MSB OF MIN
;HAS 60 MIN ELAPSED
;INC LSB OF HOURS
;IS LSB A 4

```


1716	010626	001014				BNE	NEWTM		
1717	010630	022737	000062	006566		MOV	#62, @#HRS1		; IF YES, IS MSB A 2
1718	010636	001401				RTI	.+4		
1719	010640	000002				RTI			
1720	010642	012737	000060	006566		MOV	#60, @#HRS1		; IF 24 HOURS RESET
1721	010650	012737	000060	006570		MOV	#60, @#HRS2		; LSB AND MSB OF HOURS
1722	010656	000002				RTI			
1723	010660	022737	000072	006570	NEWTM:	CMP	#72, @#HRS2		; IF NOT 4 IS IT 10 HOURS
1724	010666	001401				BEQ	.+4		
1725	010670	000002				RTI			
1726	010672	005237	006566			INC	@#HRS1		; YES INC MSB OF HOURS
1727	010676	012737	000060	006570		MOV	#60, @#HRS2		
1728	010704	000002				RTI			
1729									
1730									
1731									
1732									
1733	010706	022737	001750	006624	CLK2:	CMP	#1000., @#MSTA		; THIS ROUTINE IS THE WORK
1734	010714	003011				BGT	25		
1735	010716	162737	001750	006624		SUB	#1000., @#MSTA		; AREA ROUTINE AND IS THE
1736	010724	005237	006620			INC	@#SEC2A		; SAME AS INTERRUPT HANDLER
1737	010730	022737	000072	006620		CMP	#72, @#SEC2A		; SERVICE ROUTINE
1738	010736	001401				BEQ	.+4		
1739	010740	000475			25:	BR	END1A		
1740	010742	012737	000060	006620		MOV	#60, @#SEC2A		
1741	010750	005237	006616			INC	@#SEC1A		
1742	010754	022737	000066	006616		CMP	#66, @#SEC1A		
1743	010762	001401				BEQ	.+4		
1744	010764	000463				BR	END1A		
1745	010766	012737	000060	006616		MOV	#60, @#SEC1A		
1746	010774	005237	006614			INC	@#MIN2A		
1747	011000	022737	000072	006614		CMP	#72, @#MIN2A		
1748	011006	001401				BEQ	.+4		
1749	011010	000451				BR	END1A		
1750	011012	012737	000060	006614		MOV	#60, @#MIN2A		
1751	011020	005237	006612			INC	@#MIN1A		
1752	011024	022737	000066	006612		CMP	#66, @#MIN1A		
1753	011032	001401				BEQ	.+4		
1754	011034	000437				BR	END1A		
1755	011036	012737	000060	006612		MOV	#60, @#MIN1A		
1756	011044	005237	006610			INC	HRS2A		
1757	011050	022737	000064	006610		CMP	#64, @#HRS2A		
1758	011056	001014				BNE	NEWT		
1759	011060	022737	000062	006606		CMP	#62, @#HRS1A		
1760	011066	001401				BEQ	.+4		
1761	011070	000421				BR	END1A		
1762	011072	012737	000060	006606		MOV	#60, @#HRS1A		
1763	011100	012737	000060	006610		MOV	#60, @#HRS2A		
1764	011106	000412				BR	END1A		
1765	011110	022737	000072	006610	NEWT:	CMP	#72, @#HRS2A		
1766	011116	001401				BEQ	.+4		
1767	011120	000405				BR	END1A		
1768	011122	005237	006606			INC	@#HRS1A		
1769	011126	012737	000060	006610		MOV	#60, @#HRS2A		
1770	011134	012777	011202	175400	END1A:	MOV	#CR, @PVEC		; SET UP FOR PRINTER OUTPUT
1771	011142	012737	177776	006562		MOV	#-2, @#CNTB		

1772	011150	012737	006606	006560		MOV	#HRS1A, @CNT1	
1773	011156	012737	177767	006556		MOV	#-11, @CNT	
1774	011164	012777	000000	175344		MOV	#0, @PDBR	
1775	011172	012777	000100	175340		MOV	#100, @PCSR	
1776	011200	000002				RTI		
1777								
1778								
1779	011202	012777	011220	175332	CR:	MOV	#LF, @PVEC	; OUTPUT CR
1780	011210	012777	000215	175320		MOV	#215, @PDBR	
1781	011216	000002				RTI		
1782								
1783	011220	012777	011236	175314	LF:	MOV	#PINTR, @PVEC	; OUTPUT LF
1784	011226	012777	000212	175302		MOV	#212, @PDBR	
1785	011234	000002				RTI		
1786	011236	005237	006556		PINTR:	INC	@CNT	; PRINT TWO DIGITS FOLLOWED
1787	011242	001414				BEQ	DONE	; BY COLON UNTIL TIME OF
1788	011244	005737	006562			TST	CNTB	; DAY IS PRINTED
1789	011250	001420				BEQ	COLON	
1790	011252	013704	006560			MOV	@CNT1, %4	
1791	011256	012477	175254			MOV	(%4)+, @PDBR	
1792	011262	010437	006560			MOV	%4, @CNT1	
1793	011266	005237	006562			INC	@CNTB	
1794	011272	000002				RTI		
1795	011274	012777	011330	175240	DONE:	MOV	#PER, @PVEC	; WHEN DONE PRINT "."
1796	011302	012777	000056	175226		MOV	#56, @PDBR	
1797	011310	000002				RTI		
1798								
1799	011312	012737	177776	006562	COLON:	MOV	#-2, @CNTB	
1800	011320	012777	000072	175210		MOV	#72, @PDBR	
1801	011326	000002				RTI		
1802								
1803	011330	005037	006562		PER:	CLR	@CNTB	; PRINT MSB OF MILLISEC
1804	011334	000250				CLN		
1805	011336	013737	006624	006560		MOV	@MSTA, @CNT1	
1806	011344	012737	177767	006556		MOV	#-9, @CNT	
1807	011352	162737	000144	006560	1S:	SUB	#100., @CNT1	
1808	011360	100406				BMI	2S	
1809	011362	005237	006562			INC	@CNTB	
1810	011366	005237	006556			INC	@CNT	
1811	011372	001367				BNE	1S	
1812	011374	000404				BR	3S	
1813	011376	062737	000144	006560	2S:	ADD	#100., @CNT1	
1814	011404	000250				CLN		
1815	011406	062737	000060	006562	3S:	ADD	#60, @CNTB	
1816	011414	012777	011432	175120		MOV	#NUM1, @PVEC	
1817	011422	013777	006562	175106		MOV	@CNTB, @PDBR	
1818	011430	000002				RTI		
1819								
1820	011432	012777	011514	175102	NUM1:	MOV	#NUM2, @PVEC	; PRINT LSB OF MILLISEC
1821	011440	005037	006562			CLR	@CNTB	
1822	011444	000250				CLN		
1823	011446	012737	177767	006556		MOV	#-9, @CNT	
1824	011454	162737	000012	006560	1S:	SUB	#10., @CNT1	
1825	011462	100405				BMI	3S	
1826	011464	005237	006562			INC	@CNTB	
1827	011470	005237	006556			INC	@CNT	


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1828 011474 001367      BNE      1$
1829 011476 062737      ADD      #60, @#CNTB
1830 011504 013777      MOV      @#CNTB, @PDBR
1831 011512 000002      RTI
1832
1833 011514 012777      MOV      #KINTR, @KVEC      ;RESTORE KEYBOARD VECTOR
1834 011522 000002      RTI
1835
1836
1837
1838
1839
1840
1841 011524 032777      DELADJ: BIT      #10, @SR      ;TEST FOR SR3=1 WHICH INDICATES
1842                                     ;11/70 & 11/45 WITH MOS
1843 011532 001001      BNE      1$      ;ADJUST DELAY TIMES
1844 011534 000207      RTS      %7      ;NO ADJUSTMENTS REQUIRED
1845 011536 012701      MOV      #ADJ, R1      ;GET START OF REG. FOR ADJUST
1846 011542 012700      MOV      #DEL1, R0      ;GET START OF REG. TO ADJUST
1847 011546 012702      MOV      #DEL4, R2      ;GET END TAG OF ADJUSTMENT
1848 011552 062702      ADD      #2, R2      ;UPDATE END CHECK
1849 011556 012120      MOV      (R1)+, (R0)+      ;UPDATE DELAY COUNTS
1850 011560 020200      CMP      R2, R0      ;ARE WE DONE
1851 011562 001375      BNE      2$      ;NO CONTINUE UPDATE
1852 011564 000207      RTS      %7      ;ADJUSTMENT MADE
1853
1854 011566 013746      SWADJ: MOV      @#4, -(%)      ;SAVE CONTENT OF TRAP
1855                                     ;VECTOR
1856 011572 012737      MOV      #SWADJ1, @#4      ;SET UP NEW TRAP VECTOR
1857 011600 005777      TST      @SR      ;TEST FOR SWITCH REG.
1858 011604 012637      MOV      (%)+, @#4      ;RESTORE STACK NO
1859                                     ;TIME OUT ACCONED.
1860 011610 000207      RTS      %7
1861
1862 011612 022626      SWADJ1: CMP      (%)+, (%)+      ;UPDATE STACK
1863 011614 012637      MOV      (%)+, @#4      ;RESTORE TRAP VECTOR
1864 011620 012737      MOV      #SOFTSR, SR      ;SET SWITCH REG. (SR) TO
1865                                     ;EQUAL SOFTSR
1866 011626 000207      RTS      %7      ;RETURN TO CALLER
1867
1868
1869
1870      000001      .END

```


M03

.MAIN. MACY11 27(732) 10-SEP-76 13:04 PAGE 39
 DZKWBG.P11 CROSS REFERENCE TABLE -- USER SYMBOLS

CTR	001004	461#	536*	537	545	557	572	579	670	683	702	718	735	752
		769	784	801	820	924	1002	1010	1044	1052	1069	1077	1237	1552
CTRLI =	000211	1375#	1507											
CTRLT =	000224	1376#	1509											
CTR1	006524	1359#												
DELADJ	011524	485	497	1841#										
DELY	004376	998	1006	1015#	1040	1048	1065	1073						
DEL1	001024	469#	695	762	831	853	868	884	897	1086	1102	1846		
DEL2	001026	470#	711	777										
DEL3	001030	471#	554	564	728	794								
DEL4	001032	472#	745	812	1847									
DONE	011274	1787	1795#											
END1A	011134	1739	1744	1749	1754	1761	1764	1767	1770#					
EOMK	006346	1312*	1313	1330#										
HLT =	104000	443#	520	534	539	547	559	574	581	587	591	595	599	605
		609	615	619	628	632	642	651	660	672	685	701	704	717
		720	734	737	751	754	768	771	783	786	800	803	818	822
		835	840	843	857	874	888	901	928	961	1001	1009	1012	1043
		1051	1054	1068	1076	1079	1092	1096	1108	1112				
HOLD	007700	1539*	1542#											
HOLDIT	007670	1539#	1545											
HRS1	006566	1378#	1465*	1517	1546	1717	1720*	1726*						
HRS1A	006606	1386#	1547	1759	1762*	1768*	1772							
HRS2	006570	1379#	1466*	1714*	1715	1721*	1723	1727*						
HRS2A	006610	1387#	1756*	1757	1763*	1765	1769*							
H50Z	007074	456	1443#											
H60Z	007010	455	1431#											
ICOUNT	001022	468#	491*	509*	1296									
INIT	007174	1417	1429	1441	1453	1461#								
INTFLG	006534	1363#	1478*	1544*	1553	1684*								
KCSR	006550	1369#	1476*	1588										
KDBR	006546	1368#	1504	1524	1530	1539	1590							
KIN	007534	1508	1514#											
KINI	007630	1520	1529#											
KINI2	007600	1523#	1536											
KINTR	007504	1473	1504#	1523	1833									
KOUT	007702	1491	1510	1544#	1554									
KVEC	006552	1370#	1473*	1520*	1523*	1536*	1545*	1833*						
KVECS	006554	1371#	1474*											
K10HZ	006724	454	1419#											
K100HZ	006640	453	1407#											
LF	011220	1779	1783#											
LINE	005550	1175*	1178*	1180	1193	1204#								
LOGICA	005154	442	1125#											
LOOP	004132	953#	969											
LST	006602	1384#	1463*	1518*	1685*	1686	1688*							
LSTA	006622	1392#												
MIN1	006572	1380#	1467*	1709*	1710	1713*								
MIN1A	006612	1388#	1751*	1752	1755*									
MIN2	006574	1381#	1468*	1704*	1705	1708*								
MIN2A	006614	1389#	1746*	1747	1750*									
MOVE	007160	1414	1426	1438	1450	1455#								
MSGPWR	006416	1216	1341#											
MSG1	006350	1226	1332#											
MSG2	006412	1229	1339#											
MST	006604	1385#	1464*	1519*	1689*	1690*	1691	1693*						

ADD	698	714	731	748	765	780	797	815	885	898	1087	1103	1571	1577	1695
ASL	1690	1813	1815	1829	1848										
BEG	1558	1559	1565	1572											
BGT	519	533	538	546	558	573	580	586	590	594	598	604	608	614	618
BIC	627	631	659	671	684	703	719	736	753	770	785	802	821	842	1123
BICB	1177	1224	1228	1297	1317	1482	1485	1487	1499	1506	1508	1510	1556	1561	1596
BIS	1598	1600	1608	1613	1696	1701	1706	1711	1718	1724	1738	1743	1748	1753	1760
BISB	1766	1787	1789												
BIT	1687	1692	1734	750	767	782	799	817	834	856	873	887	900	1091	1107
BLOS	700	716	733												
BLT	1157	1171	1189	1202	1259	1531	1602								
BMI	1311														
BNE	648	1260													
BPL	1611														
BR	518	524	640	649	658	740	807	841	919	992	1176	1190	1223	1286	1294
CLN	1481	1484	1486	1498	1841										
CLR	926														
CMP	1028														
CMPB	697	713	724	730	747	764	779	790	796	814	839	1061	1090	1106	1174
DEC	1808	1825													
EMT	525	549	556	571	641	650	675	688	699	715	732	741	749	766	781
HALT	798	808	816	833	855	870	886	899	905	920	932	960	969	993	1088
INC	1104	1151	1156	1165	1170	1188	1191	1201	1215	1265	1287	1295	1314	1458	1489
JMP	1535	1551	1554	1564	1576	1605	1716	1758	1811	1829	1843	1851			
JSR	982	1000	1008	1019	1025	1042	1050	1067	1075	1095	1111	1118	1121	1153	1167
MOV	1185	1198	1242	1249	1271	1289	1319	1323	1326	1570	1589	1593	1628	1632	
	521	527	836	858	872	902	929	1013	1203	1208	1299	1307	1321	1329	1617
	1739	1744	1749	1754	1761	1764	1767	1812							
	1804	1814	1822												
	499	500	501	502	504	510	542	552	562	596	606	616	629	636	637
	644	645	653	654	666	679	680	692	708	725	742	759	774	791	809
	826	827	844	850	859	865	871	880	889	906	918	930	945	946	956
	971	995	1003	1015	1037	1045	1062	1070	1082	1093	1213	1300	1409	1421	1433
	1445	1463	1464	1477	1478	1479	1480	1490	1497	1500	1501	1514	1515	1518	1519
	1544	1566	1567	1583	1584	1803	1821								
	507	522	537	545	557	572	585	589	593	603	613	626	670	674	683
	687	903	925	959	968	1027	1281	1296	1305	1505	1507	1509	1560	1563	1575
	1604	1612	1686	1691	1695	1700	1705	1710	1715	1717	1723	1733	1737	1742	1747
	1752	1757	1759	1765	1850	1862									
	1313	1316	1595	1597	1599										
	673														
	443														
	436	526	1211	1243											
	548	555	570	686	832	854	869	904	931	967	975	1150	1155	1164	1169
	1187	1200	1214	1231	1264	1298	1328	1457	1534	1550	1574	1601	1699	1694	1699
	1704	1709	1714	1726	1736	1741	1746	1751	1756	1768	1786	1793	1809	1810	1826
	1827														
	450	451	452	453	454	455	456	505	511	921	972	994	1129	1218	1293
	1417	1429	1441	1453	1496	1502	1578								
	484	485	493	496	497	955	958	998	1006	1011	1040	1048	1053	1065	1073
	1078	1125	1139	1217	1230	1234	1236	1238	1240	1251	1262	1266	1276	1408	1414
	1420	1426	1432	1438	1444	1450	1585	1623							
	483	486	487	489	490	491	492	495	498	503	508	509	514	515	516
	523	529	531	535	536	544	553	554	563	564	566	567	568	569	577
	584	588	592	602	612	624	625	638	639	646	647	655	656	657	667
	668	669	681	682	693	694	695	709	710	711	726	727	728	743	744

	745	760	761	762	775	776	777	792	793	794	810	811	812	825	828
	829	830	831	837	845	848	849	851	852	853	860	863	864	866	867
	868	875	879	881	882	883	884	890	893	894	895	896	897	922	923
	924	927	943	944	947	948	949	950	954	957	970	996	997	1002	1004
	1005	1010	1016	1017	1022	1023	1030	1038	1039	1044	1046	1047	1052	1063	1064
	1069	1071	1072	1077	1083	1084	1085	1086	1099	1100	1101	1102	1116	1119	1122
	1138	1140	1141	1142	1145	1146	1147	1148	1154	1159	1160	1161	1162	1168	1175
	1178	1180	1181	1182	1186	1193	1194	1195	1199	1207	1209	1210	1212	1216	1226
	1229	1232	1235	1237	1239	1247	1250	1254	1258	1272	1275	1282	1290	1291	1293
	1301	1306	1407	1410	1411	1412	1413	1415	1416	1419	1422	1423	1424	1425	1427
	1428	1431	1434	1435	1436	1437	1439	1440	1443	1446	1447	1448	1449	1451	1452
	1455	1456	1461	1462	1465	1466	1467	1468	1469	1470	1471	1472	1473	1474	1475
	1476	1491	1492	1493	1494	1495	1504	1516	1517	1520	1523	1524	1525	1526	1529
	1530	1532	1533	1536	1539	1545	1546	1547	1548	1549	1552	1568	1580	1581	1586
	1590	1594	1609	1619	1621	1622	1629	1633	1684	1698	1703	1708	1713	1720	1721
	1727	1740	1745	1750	1755	1762	1763	1769	1770	1771	1772	1773	1774	1775	1779
	1780	1783	1784	1790	1791	1792	1795	1796	1799	1800	1805	1806	1816	1817	1820
	1823	1830	1833	1845	1846	1847	1849	1854	1856	1858	1863	1864			
MOV8	983	1312	1320	1324	1327	1603									
NEG	1026														
NOP	1126	1127	1128												
RESET	517	578	819	1109	1124	1143									
ROL	1252	1253	1255	1256	1257	1263	1614	1615	1616						
ROR	1261														
RTI	977	1141	1225	1244	1302	1511	1521	1527	1537	1540	1624	1697	1702	1707	1712
	1719	1722	1725	1728	1776	1781	1785	1794	1797	1801	1818	1831	1834		
RTS	984	1020	1031	1267	1273	1277	1315	1459	1634	1844	1852	1860	1866		
SUB	1024	1233	1557	1688	1693	1735	1807	1824							
SWAB	1562														
TRAP	446														
TST	488	532	579	597	607	617	630	702	718	723	735	752	769	794	789
	801	820	1029	1060	1089	1094	1105	1110	1173	1227	1241	1248	1288	1292	1488
	1553	1555	1569	1573	1607	1788	1857								
TSTB	696	712	729	746	763	778	795	813	838	981	999	1007	1018	1041	1049
	1066	1074	1117	1120	1152	1166	1184	1197	1270	1318	1322	1325	1588	1592	1627
	1631														
WAIT	1149	1163	1183	1196	1483										
.ASCII	1278	1332	1339	1341	1349										
.BYTE	1330	1395	1396	1397	1398	1399	1400	1401							
.ENABL	433														
.END	1870														
.EVEN	1279	1331	1338	1340	1348	1354	1402								
.LIST	436														
.NLIST	436														
.PAGE	1130	1205													
.REPT	1	436													
.SBTTL	430	1131	1205												

ERRORS DETECTED: 0
 DEFAULT GLOBALS GENERATED: 0

*DZKWBG.DZKWBG.SEG/SOL/CRF/DS:ERFZ/EN:ABS=DSKM:DZKWBG.P11
 RUN-TIME: 6 12 2 SECONDS

F04

MAIN. MACY11 27(732) 10-SEP-76 13:04 PAGE 46
DZKWBG.P11 CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

RUN-TIME RATIO: 50/21=2.3
CORE USED: 10K (19 PAGES)

