

PDP11

BASIC MICROPROCESSOR TST
MD-11-DZKCC-A

EP-DZKCC-A-DL-A
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FICHE 1 OF 1

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This microfiche card contains a grid of 14 columns and 24 rows of tiny frames. Each frame contains a small amount of data, likely representing a single instruction or data point from a program. The data is too small to be legible in this image, but the overall layout is a structured grid of information.

IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DZKCC-A-D
PRODUCT NAME: BASIC W/R AND MICRO-PROCESSOR TESTS
DATE: MAY 1977
MAINTAINER: DIAGNOSTICS
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1. ABSTRACT

The function of the KMC11 diagnostics is to verify that the option operates according to specifications. The diagnostics verify that there are no malfunctions and that all operations of the KMC11 are correct in its environment.

Parameters must be set up to alert the diagnostics to the KMC11 configuration. These parameters are contained in the STATUS TABLE and are generated in two ways: 1) Manual Input - the operator answers questions. 2) Autosizing - the program determines the parameters automatically.

DZKCC tests the KMC11 micro-processor (MB204). It performs write/read tests on the KMC unibus registers, checks the micro-processor operation, checks out Main Memory, scratch pad memory, the ALU functions as well as interrupts and NPR operation. DZKCC performs no tests on the line unit or any CRAM dependent tests. It will run on KMC11's containing CRAM (IOP). It does not require a line unit to run.

Currently there are four off line diagnostics that are to be run in sequence to insure that if an error should occur it will be detected at an early stage.

NOTE: Additional diagnostics may be added in the future.

The four diagnostics are:

1. DZKCC [REV] Basic W/R and Micro-processor tests
2. DZKCD [REV] Jump and memory tests (Heat test tape)
3. DZKCE [REV] DDCMP Line unit tests
4. DZKCF [REV] BITSTUFF Line unit tests
5. DZKCA [REV] KMC11 CPU MICRO-DIAGNOSTICS.

2. REQUIREMENTS

2.1 EQUIPMENT

Any PDP11 family CPU (except an LSI-11) with minimum 8k memory
ASR 33 (or equivalent)
KMC11-AN IOP (MB204)

2.2 STORAGE

Program will use all 8K of memory except where ABL and BOOTSTRAP LOADER reside. Locations 2100 thru 2300; contain the "STATUS TABLE" information which is generated at start of diagnostics by manual input (questions) or automatically (auto-sizing). This area is an overlay area and should not be altered by the operator.

3. LOADING PROCEEDURE

3.1 METHOD

All programs are in absolute format and are loaded using the ABSOLUTE LOADER. NOTE: if the diagnostics are on a media such as DISK, MAGTAPE, DECTAPE, or CASSETTE; follow instructions for the monitor which has been provided on that specific media.

ABSOLUTE LOADER starting address *500

MEMORY * SIZE

4k	17
8k	37
12k	57
16k	77
20k	117
24k	137
28k	157

- 3.1.1 Place address of ABS loader into switch register.
(also place 'HALT' SW up)
- 3.1.2 Depress 'LOAD ADDRESS' key on console and release.
- 3.1.3 Depress 'START KEY' on console and release (program should now be loading into CPU)

4. STARTING PROCEEDURE

- a. Set switch register to 000200
- b. Depress 'LOAD ADDRESS' key and release
- c. Set SWR to zero for 'AUTO SIZING' or SWR bit0=1 for manual input (questions) or SWR bit7=1 to use existing parameters set up by a previous start or a previously run KMC11 diagnostic.
- d. Depress 'START KEY' and release. The program will type Maindec Name and program name (if this was the first start up of the program) and also the following:

MAP OF KMC11 STATUS

PC	CSR	STAT1	STAT2	STAT3
--	--	--	--	--
002100	160010	045310	177777	000000
002110	160020	045320	177777	000000

The program will type 'R' and proceed to run the diagnostic. The above is only an example. This would indicate the status table starting at add. 2100 in the program. In this example the table contains the information and status of two KMC11'S. THE STATUS TABLE MUST BE VERIFIED BY THE USER IF AUTO SIZING IS DONE. For information of status table see section 8.4 for help.

If the diagnostic was started with SW00=1 indicating manual parameter input then the following shows an example of the questions asked and some example answers:

HOW MANY KMC11'S TO BE TESTED?1

01
 CSR ADDRESS?160010
 VECTOR ADDRESS?310
 BR PRIORITY LEVEL? (4,5,6,7)?5
 WHICH LINE UNIT? IF NONE TYPE "N", IF M8201 TYPE "1", IF M8202 TYPE "2"?1
 IS THE LOOP BACK CONNECTOR ON?Y
 SWITCH PAC#1 (DDCMP LINE#)?377
 SWITCH PAC#2 (BMB73 BOOT ADD)?377

Following the questions the status map is printed out as described above, the information in the map reflects the answers to the questions. If the diagnostic was started with SW00=0 and SW07=0 (AUTO-SIZING) then no questions are asked and only the status-map is printed out. If AUTO-SIZING is used the status information must be verified to be correct (match the hardware). if it does not match the hardware the diagnostic must be restarted with SW00=1 and the questions answered.

4.1 CONTROL SWITCH SETTINGS

SW 15 Set: Halt on error
SW 14 Set: Loop on current test
SW 13 Set: Inhibit error print out
SW 12 Set: Inhibit type out abell on error.
SW 11 Set: Inhibit iterations. (quick pass)
SW 10 Set: Escape to next test on error
SW 09 Set: Loop with current data
SW 08 Set: Catch error and loop on it
SW 07 Set: Use previous status table.
SW 06 Set: Halt in ROMCLK routine before clocking
micro-processor
SW 05 Set: Reserved
SW 04 Set: Reserved
SW 03 Set: Reselect KMC11's desired active
SW 02 Set: Lock on selected test
SW 01 Set: Restart program at selected test
SW 00 Set: Build new status table from questions. (If SW07=0
and SW00=0 a new status table is built by
auto-sizing)

Switch 06 and 08-15 are dynamic and can be changed as needed while the diagnostic is running. Switches 00-03 and switch 07 are static, and are used only on starting or restarting the diagnostic.

4.1.2 SWITCH REGISTER OPTIONS (at start up)

SW 01 RESTART PROGRAM AT SELECTED TEST. It is strongly suggested that at least one pass has been made before trying to select a test, the reason being is that the program has to clear areas and set up parameters. When this switch is used the diagnostic will ask TEST NO.? Answer by typing the number of the test desired and carriage return to begin execution at the selected test.

SW 02 LOCK ON SELECTED TEST. This switch when used with SW01 will cause the program to constantly loop on the selected test. Hitting any key on the console will let it advance to the next test and loop until a key is hit again. If SW02=0 when SW01 is used. The program will begin at the selected test and continue normal operations.

SW 03 RESELECT KMC11'S DESIRED ACTIVE. Please note that a message is typed out for setting the switch register equal to KMC11's active. this means if the system has four KMC11s; bits 00,01,02,03 will be set in loc 'KMACTV' from the switch register. Using this switch(SW00) alters that location; therefore if four KMC11s are in the system *****DO NOT***** set switches greater than SW 03 in the up position. this would be a fatal error. do not select more active KMC11s than there is information on in the status table.

METHOD: A: Load address 200
 B: Start with SW 00=1
 C: Program will type message
 D: Set a switch for each KMC desired active.
 EXAMPLE: If you have 4 KMC's but only want to run the first and the last set SWR bits 0 and 3 = 1. PRESS CONTINUE
 E: Number (IF VALID) will be in data lights (excluding 11/05)
 F: Set with any other switch settings desired. PRESS CONTINUE.

4.1.3 DYNAMIC SWITCHES

ERROR SWITCHES

1. SW 12 Delete print out/bell on error.
2. SW 13 Delete error printout.
3. SW 15 Halt on the error.
4. SW 08 Goto beginning of the test(on error).
5. SW 10 Goto next test(on error).

SCOPE SWITCHES

1. SW06 Halt in ROMCLK routine before clocking micro-processor instruction. This allows the operator to scope a micro-processor instruction in the static state before it is clocked. Hit continue to resume running.
2. SW09 (if enabled by 'SCOPI') on an error; If an '#' is printed in front of the test no. (ex. #TEST NO. 10) SW09 is incorporated in that test and therefore SW09 is usually the best switch for the scope loop (SW14=0, SW10=0, SW09=1, SW08=0). If SW09 is not enableed; and there is a HARD error (constant); SW08 is best. (SW14=1,0, SW10=0, SW09=0, SW08=1). for intermitent errors; SW14=1 will loop on test regardless of error or not error. (SW14=1, SW10=0, SW09=0, SW08=1,0)
3. SW11 Inhibit interations.
4. SW14 Loop on current test.

4.2 STARTING ADDRESS

Starting address is at 000200 there are no other starting addresses for the KMC11 diagnostics. (See Section 4.0)

NOTE: If address 000042 is non-zero the program assumes it is under ACT11 or XXDP control and will act accordingly after all available KMC11's are tested the program will return to 'XXDP' or 'ACT-11'.

5. OPERATING PROCEDURE

When program is initially started messages as described in section 4.0 will be printed, and program will begin running the diagnostic

5.2 PROGRAM AND/OR OPERATOR ACTION

The typical approach should be

1. Halt on error (via SW 15=1) when ever an error occurs.
2. Clear SW 15.
3. Set SW 14: (loop on this test)
4. Set SW 13: (inhibit error print out)

The TEST NUMBER and PC will be typed out and possibly an error message (this depends on the test) to give the operator an idea as to the source of the problem. If it is necessary to know more information concerning the error report; LOOK IN THE LISTING for that TEST NUMBER which was typed out and then NOTE THE PC of the ERROR REPORT this way the EXACT FUNCTION of the test CAN BE DETERMINED.

6. ERRORS

As described previously there will always be a TEST NUMBER and PC typed out at the time of an error (providing SW 13=0 and SW 12=0). in most cases additional information will be supplied in the the error message to give the operator an indication of the error.

6.2 ERROR RECOVERY

If for some reason the KMC11 should 'HANG THE BUS' (gain control of bus so that console manual functions are inhibited) an init or power down/up is necessary for operator to regain control of cpu. If this should happen; look in location 'STSTNM' (address 1202) for the number of the test that was running at the time of the catastrophic error. In this way the operator will have an idea as to what the KMC11 was doing at the time of the error.

7. RESTRICTIONS

7.1 STARTING RESTRICTIONS

See section 4. (PLEASE)
Status table should be verified regardless of how program was started. Also it is important to use this listing along with the information printed on the TTY to completely isolate problems.

7.2 OPERATING RESTRICTIONS

The first time a KMC11 diagnostic is loaded into core and run the STATUS TABLE must be set up. This is done by manual input (SW00=1) or by autosizing (SW00=0 and SW07=0). Thereafter however the status table need not be setup by subsequent restarts or even loading the next KMC diagnostic because the STATUS TABLE is overlaid. The current parameters in the STATUS TABLE are used when SW07=1 on start up.

7.3 HARDWARE CONFIGURATION RESTRICTIONS

KMC11 IOP(MB204)- Jumper W1 must be in,

8. MISCELLANEOUS

8.1 EXECUTION TIME

All KMC11 device diagnostics will give an 'END PASS' message (providing no errors and sw12=0) within 4 mins. This is assuming SW11=1 (DELETE ITERATIONS) is set to give the fastest possible execution. The actual execution time depends greatly on the PDP11 CPU configuration and the amount of memory in the system.

8.2 PASS COMPLETE

NOTE: EVERY time the program is started; the tests will run as if SW11 (delete iterations) was up (=1). This is to 'VERIFY NO HARD ERRORS' as soon as possible. Therefore the first pass -EACH TIME PROGRAM IS STARTED- will be a 'QUICK PASS' until all KMC11's in system are tested. When the diagnostic has completed a pass the following is an example of the print out to be expected.

```
END PASS DZKCC CSR: 175000 VEC: 0300 PASSES: 000001
ERRORS: 000000
```

NOTE: The pass count and error counts are cummulative for each KMC11 that is running, and are set to zero only when the diagnostic is started. Therefore after an overnight run for example, the total passes and errors for each KMC11 since the diagnostic was started are reflected in PASSES: and ERRORS:.

B.4 KEY LOCATIONS

SLPADR (1206) Contains the address where program will return when iteration count is reached or if loop on test is asserted.

NEXT (1442) Contains the address of the next test to be performed.

STSTNM (1202) Contains the number of the test now being performed.

RUN (1500) The bit in 'RUN' always points to the KMC11 currently being tested. EXAMPLE: (RUN) 1500/000000001000000 Means that KMC11 no.06 is the KMC11 now running.

KMCROO-KMCR17
KMSTOO-KMST17
(2100)-(2300)

These locations contain the information needed to test up to 16 (decimal) KMC11s sequentially. they contain the CSR, VECTOR and STATUS concerning the configuration of each KMC11.

KMACTV (1306) Each bit set in this location indicates that the associated KMC11 will be tested in turn. EXAMPLE: (KMACTV) 1470/0000000000011111 means that KMC11 no. 00,01,02,03,04 will be tested. EXAMPLE: (KMACTV) 1470/0000000000010001 Means that KMC11 no. 00,04 will be tested.

KMCSR (2066) Contains the CSR of the current KMC11 under test.

B.4A 'STATUS TABLE' (2100-2300)

The table is filled by AUTO SIZING or by the manual parameter input (questions) as described previously. Also if desired by user; the locations may be altered by hand (toggled in) to suit the specific configuration.

The example status map shown below contains information for two KMC11'S. the table can contain up to 16 KMC11'S. Following the map is a description of the bits for each map entry

MAP OF KMC11 STATUS

PC	CSR	STAT1	STAT2	STAT3
002100	160010	045310	177777	000000
002110	160020	016320	000000	000000

Each map entry contains 4 words which contain the status information for 1 KMC11. The PC shows where in core memory the first of the 4 words is. In the example above the first KMC'S status is in locations, 2100, 2102, 2104, and 2106. The second KMC status is located at 2110, 2112, 2114, and 2116. The information contained in each 4 word entry is defined as follows:

CSR: Contains KMC11 CSR address

STAT1: BITS 00-08 IS KMC11 VECTOR ADDRESS
BIT14=1 TURNAROUND CONNECTOR IS ON
BIT14=0 NO TURNAROUND CONNECTOR
BIT13=0 LINE UNIT IS AN M8201
BIT13=1 LINE UNIT IS AN M8202
BIT12=1 NO LINE UNIT
BITS 09-11 IS KMC11 BR PRIORITY LEVEL

STAT2: LOW BYTE IS SWITCH PAC#1 (DDCMP LINE NUMBER)
HIGH BYTE IS SWITCH PAC#2 (BM873 BOOT ADD)

STAT3: NOT USED

8.5 METHOD OF AUTO SIZING

8.5.1 FINDING THE CONTROL STATUS REGISTER.

The auto-sizing routine finds a KMC11 as follows: It starts at address 160000 and tests all address in increments of 10 up to and including address 167760. If the address does not time out, the following is done, the first CROM address is written to a 125252 then it is read back. If it contains a -1 or 125252 a KMC11 has been found, if not, the address is updated by 10 and the search continues. A -1 indicates a KMC11 with no CRAM, and a 125252 indicates a KMC11 with CRAM. Further tests are performed at this point to determine which line unit, if any, is installed, if a loop-back connector is installed and various switch settings on the line unit. THIS IS WHY THE STATUS TABLE MUST BE VERIFIED BY THE USER AND IF ANY OF THE INFORMATION DOES NOT AGREE WITH THE HARDWARE THE DIAGNOSTIC MUST BE RESTARTED AND THE QUESTIONS MUST BE ANSWERED. All KMC11's in the system will be found by the auto-sizer. If it does not find a KMC11 the diagnostic must be restarted and the questions answered.

8.5.2 FINDING THE VECTOR AND BR LEVEL

The vector area (address 300-776) is filled with the instruction IOT and '+2' (next address). The processor status is started at 7 and the KMC is programmed to interrupt. The PS is lowered by 1 until the KMC interrupts, a delay is made and if no interrupt occurs at PS level 3 (because of a bad KMC11) the program assumes vector address 300 at BR level 5 and the problem should be fixed in the diagnostic. Once the problem is fixed; the program should be re-setup again to get correct vector. If an interrupt occurred; the address to which the KMC11 interrupted to is picked up and reported as the vector. NOTE: if the vector reported is not the vector set up by you; there is a problem and AUTO SIZING should not be done.

8.5 SOFTWARE SWITCH REGISTER

If the diagnostic is run on an 11/04 or other CPU without a switch register then a software switch register is used to allow user the same switch options as described previously. If the hardware switch register does not exist or if one does and it contains all ones (177777) this software switch register is used.

Control:

To obtain control at any allowable time during execution of the diagnostic the operator types a CTRL G on the console terminal keyboard. As soon as the CTRL G is recognized, by the diagnostic, the following message will be displayed:

SWR=XXXXXX NEW?

Where XXXXXX is the current contents of the software switch register in octal. The software control routine will then await operator action. At which time the operator is required to type one or more of the legal characters: 1) 0 - 7, 2) line feed(<LF>), 3) carriage return(<CR>), or 4) control-U (CTRL U). No check is made for legality. If the input character is not a <LF>, <CR>, or CTRL U it is assumed to be an octal digit.

To change the contents of the SSR the operator simply types the new desired value in octal - leading zeros need not be typed. And terminates the input string with a <CR> or <LF> depending on the program action desired as described below. The input value will be truncated to the last 6 digits typed. At least one digit must be typed on any given input string prior to the terminator before a change to the SSR will occur.

When the input string is terminated with a <CR> the diagnostic will continue execution from the point at which it was interrupted. If a <CR> is the only thing typed the program will continue without changing the SSR. The <LF> differs from the <CR> by restarting the program as if it were restarted at address 200.

If a CTRL U is typed at any point in the input string prior to the terminator the input value will be disregarded and the prompt displayed (SWR = XXXXXX NEW?).

To set the SSR for the starting switches, first load the diagnostic, then hit CTRL G, then start the diagnostic.

APT/ACT/XXDP/SLIDE

THIS DIAGNOSTIC IS APT/ACT/XXDP/SLIDE COMPATIBLE USER WOULD BE ABLE TO RUN IT UNDER APT/ACT/XXDP ENVIRONMENT.

NOTE: FOR MANUFACTURING PURPOSE ONLY ITS DESCRIBED HOW TO RUN UNDER APT ENVIRONMENT.

ETABLE SETTING FOR APT TO RUN UNDER APT

FIRST PASS TIME:

LONGEST TEST TIME:

ADDITIONAL TEST TIME:

ALL THE ABOVE PARAMETERS ARE DEPENDENT ON PARTICULAR DIAGNOSTICS AND SHOULD BE LOADED AT THE TIME OF SETTING ETABLE.THERE IS NO DEFAULT TIME SET UP.

SOFTWARE ENVIRONMENT:001 ENVIRONMENT MODE:200

SWITCH 1:-SHOULD BE USED AS NORMAL SWITCH REGISTER.

SWITCH 2:-NOT USED.

CPU OPTIONS:-NOT USED.

MEMORY TYPE 1:-BITS<2:4>:=BITS <12:14> OF STAT1 OF DEV:0.

MAXIMUM ADDRESS:-BITS<17:19>:=BITS<12:14> OF STAT1 OF DEV:1

BITS<2:4>:=BITS <12:14> OF STAT1 OF DEV:2

BITS<10:12>:=BITS<12:14> OF STAT1 OF DEV:3

IN THE SAME MANNER

MEMORY TYPE 2 MAXIMUM ADDRESS:-GETS STAT1<12:14> OF DEVICE 4,5,6,7.

MEMORY TYPE 3 MAXIMUM ADDRESS:-GETS STAT1<12:14> OF DEVICE 8,9,10,11.

MEMORY TYPE 4 MAXIMUM ADDRESS:-GETS STAT1<12:14> OF DEVICE 12,13,14,15.

INTERRUPT VECTOR 1:FIRST DEVICE RECEIVE VECTOR.

REST OF THE DEVICE(KMC'S) VECTOR SHOULD BE SET UP SEQUENTIALLY
IN INCREMENTS OF 10.

BUS PRIORITY:KMC'S PRIORITY(SHOULD BE SAME FOR ALL KMC'S UNDER
TEST).

INTERRUPT VECTOR 2:NOT USED.

BUS PRIORITY:NOT USED.

BASE ADDRESS:FIRST DEVICE CSR ADDRESS.

REST SHOULD FOLLOW SEQUENTIALLY
IN INCREMENTS OF 10.

DEVICE MAP:AS DESCRIBED IN APT MANUAL.

CONTROLLER SPECIFIC CODE 1:-NO. OF DEVICES UNDER TEST.

CONTROLLER SPECIFIC CODE 2:-NOT USED.

DEVICE DESCRIPTOR WORD 0:STAT2 OF FIRST DEVICE.

. .

. .

TO

. .

. .

DEVICE DESCRIPTOR WORD 15:STAT2 OF 16TH DEVICE.(KMC)

DOCUMENT

MAINDEC-11-DZKCC-A

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- 2225 ***** TEST 1 *****
VERIFY THAT REFERENCING UNIBUS DEVICE REGISTERS
DOES NOT CAUSE A TIME OUT TRAP

- 2256 ***** TEST 2 *****
VERIFY THAT RUN CAN BE CLEARED

- 2275 ***** TEST 3 *****
UNIBUS REGISTER WORD DUAL ADDRESSING TEST
LOAD ALL REGISTERS WITH INCREMENTING PATTERN
READ BACK ALL REGISTERS TO VERIFY CORRECT ADDRESSING

- 2318 ***** TEST 4 *****
CONTROL STATUS REGISTER WRITE/READ TEST
SET BIT0, VERIFY BIT0 WAS SET
CLEAR BIT0, VERIFY BIT0 WAS CLEARED

- 2350 ***** TEST 5 *****
CONTROL STATUS REGISTER WRITE/READ TEST
SET BIT1, VERIFY BIT1 WAS SET
CLEAR BIT1, VERIFY BIT1 WAS CLEARED

- 2382 ***** TEST 6 *****
- 2383 CONTROL STATUS REGISTER WRITE/READ TEST
SET BIT2, VERIFY BIT2 WAS SET
CLEAR BIT2, VERIFY BIT2 WAS CLEARED

- 2414 ***** TEST 7 *****
CONTROL STATUS REGISTER WRITE/READ TEST
SET BITS, VERIFY BITS WAS SET
CLEAR BITS, VERIFY BITS WAS CLEARED

- 2446 ***** TEST 10 *****
CONTROL STATUS REGISTER WRITE/READ TEST
SET BIT6, VERIFY BIT6 WAS SET
CLEAR BIT6, VERIFY BIT6 WAS CLEARED

- 2478 ***** TEST 11 *****
CONTROL STATUS REGISTER WRITE/READ TEST
SET BIT7, VERIFY BIT7 WAS SET
CLEAR BIT7, VERIFY BIT7 WAS CLEARED
- 2510 ***** TEST 12 *****
CONTROL STATUS REGISTER WRITE/READ TEST
SET BIT9, VERIFY BIT9 WAS SET
CLEAR BIT9, VERIFY BIT9 WAS CLEARED
- 2542 ***** TEST 13 *****
CONTROL STATUS REGISTER WRITE/READ TEST
SET BIT11, VERIFY BIT11 WAS SET
CLEAR BIT11, VERIFY BIT11 WAS CLEARED
- 2574 ***** TEST 14 *****
CONTROL STATUS REGISTER WRITE/READ TEST
SET BIT12, VERIFY BIT12 WAS SET
CLEAR BIT12, VERIFY BIT12 WAS CLEARED
- 2606 ***** TEST 15 *****
- 2607 CONTROL OUT REGISTER WRITE/READ TEST
SET BIT0, VERIFY BIT0 WAS SET
CLEAR BIT0, VERIFY BIT0 WAS CLEARED
- 2638 ***** TEST 16 *****
CONTROL OUT REGISTER WRITE/READ TEST
SET BIT1, VERIFY BIT1 WAS SET
CLEAR BIT1, VERIFY BIT1 WAS CLEARED
- 2670 ***** TEST 17 *****
CONTROL OUT REGISTER WRITE/READ TEST
SET BIT2, VERIFY BIT2 WAS SET
CLEAR BIT2, VERIFY BIT2 WAS CLEARED
- 2702 ***** TEST 20 *****
CONTROL OUT REGISTER WRITE/READ TEST
SET BIT6, VERIFY BIT6 WAS SET
CLEAR BIT6, VERIFY BIT6 WAS CLEARED
- 2734 ***** TEST 21 *****
CONTROL OUT REGISTER WRITE/READ TEST
SET BIT7, VERIFY BIT7 WAS SET
CLEAR BIT7, VERIFY BIT7 WAS CLEARED
- 2766 ***** TEST 22 *****
CONTROL OUT REGISTER WRITE/READ TEST
SET BIT12, VERIFY BIT12 WAS SET
CLEAR BIT12, VERIFY BIT12 WAS CLEARED

2798 ***** TEST 23 *****
CONTROL OUT REGISTER WRITE/READ TEST
SET BIT13, VERIFY BIT13 WAS SET
CLEAR BIT13, VERIFY BIT13 WAS CLEARED

2830 ***** TEST 24 *****

2831 PORT4 REGISTER WRITE/READ TEST
FLOAT A ONE THROUGH PORT4 REGISTER
FLOAT A ZERO THROUGH PORT4 REGISTER

2874 ***** TEST 25 *****
PORT6 REGISTER WRITE/READ TEST
FLOAT A ONE THROUGH PORT6 REGISTER
FLOAT A ZERO THROUGH PORT6 REGISTER

2918 ***** TEST 26 *****
UNIBUS REGISTER BYTE DUAL ADDRESSING TEST
LOAD ALL REGISTERS WITH INCREMENTING PATTERN
READ BACK ALL REGISTERS TO VERIFY CORRECT ADDRESSING

2961 ***** TEST 27 *****
MAINTENANCE INSTRUCTION REGISTER TEST
VERIFY THAT THE MAINT IR CAN BE WRITTEN TO ALL ZEROS'
AND ALL ONES'. VERIFY THAT IT IS CLEARED ON A BUS RESET.

3003 ***** TEST 30 *****
MAINTENANCE INSTRUCTION REGISTER TEST
VERIFY THAT THE MAINT IR CAN BE WRITTEN TO ALL ZEROS'
AND ALL ONES'. VERIFY THAT IT IS CLEARED ON A MASTER RESET.

3045 ***** TEST 31 *****
MICRO PROCESSOR TEST
LOAD KMP06 WITH A MICRO-PROCESSOR INSTRUCTION, CLOCK IT
VERIFY INSTRUCTION EXECUTED PROPERLY
INSTRUCTION SHOULD MOVE IBUS*4 TO IBUS*5, IBUS*4 IS ALL 1'S
AND IBUS*5 IS ALL 0'S. RESULT SHOULD BE ALL 1'S IN SEL4

3074 ***** TEST 32 *****
MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
FLOAT A 1 THROUGH IBUS* REGISTER 0
FLOAT A 0 THROUGH IBUS* REGISTER 0

3131 ***** TEST 33 *****
MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
FLOAT A 1 THROUGH IBUS* REGISTER 2
FLOAT A 0 THROUGH IBUS* REGISTER 2

3188 ***** TEST 34 *****
MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
FLOAT A 1 THROUGH IBUS* REGISTER 4
FLOAT A 0 THROUGH IBUS* REGISTER 4

- 3241 ***** TEST 35 *****
MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
FLOAT A 1 THROUGH IBUS* REGISTER 5
FLOAT A 0 THROUGH IBUS* REGISTER 5

- 3294 ***** TEST 36 *****
MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
FLOAT A 1 THROUGH IBUS* REGISTER 10
FLOAT A 0 THROUGH IBUS* REGISTER 10

- 3351 ***** TEST 37 *****
MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
FLOAT A 1 THROUGH IBUS* REGISTER 11
FLOAT A 0 THROUGH IBUS* REGISTER 11

- 3410 ***** TEST 40 *****
MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
FLOAT A 1 THROUGH IBUS REGISTER 0
FLOAT A 0 THROUGH IBUS REGISTER 0

- 3463 ***** TEST 41 *****
MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
FLOAT A 1 THROUGH IBUS REGISTER 1
FLOAT A 0 THROUGH IBUS REGISTER 1

- 3516 ***** TEST 42 *****
MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
FLOAT A 1 THROUGH IBUS REGISTER 2
FLOAT A 0 THROUGH IBUS REGISTER 2

- 3569 ***** TEST 43 *****
MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
FLOAT A 1 THROUGH IBUS REGISTER 3
FLOAT A 0 THROUGH IBUS REGISTER 3

- 3622 ***** TEST 44 *****
MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
FLOAT A 1 THROUGH IBUS REGISTER 4
FLOAT A 0 THROUGH IBUS REGISTER 4

- 3675 ***** TEST 45 *****
MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
FLOAT A 1 THROUGH IBUS REGISTER 5
FLOAT A 0 THROUGH IBUS REGISTER 5

- 3728 ***** TEST 46 *****
MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
FLOAT A 1 THROUGH IBUS REGISTER 6
FLOAT A 0 THROUGH IBUS REGISTER 6

3781 ***** TEST 47 *****
MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST

3783 FLOAT A 1 THROUGH IBUS REGISTER 7
FLOAT A 0 THROUGH IBUS REGISTER 7

3834 ***** TEST 50 *****
MICRO PROCESSOR IBUS DUAL ADDRESS TEST
WRITE ALL IBUS REGISTERS WITH INCREMENTING PATTERN
READ ALL IBUS REGISTERS TO VERIFY CORRECT ADDRESSING

3897 ***** TEST 51 *****
MICRO PROCESSOR BR REGISTER TEST
FLOAT A 1 THROUGH THE BR
FLOAT A 0 THROUGH THE BR

3949 ***** TEST 52 *****
SCRATCH PAD TEST

3951 FLOAT A 1 THROUGH EACH SCRATCH PAD LOCATION
FLOAT A 0 THROUGH EACH SCRATCH PAD LOCATION

4016 ***** TEST 53 *****
SCRATCH PAD DUAL ADDRESSING TEST
WRITE AN INCREMENTING PATTERN IN ALL SP LOCATIONS
READ ALL SP LOCATIONS TO VERIFY CORRECT ADDRESSING

4077 ***** TEST 54 *****
INTERRUPT TEST
TEST THAT DEVICE CAN INTERRUPT TO VECTOR A

4108 ***** TEST 55 *****
INTERRUPT TEST
TEST THAT DEVICE CAN INTERRUPT TO VECTOR B

4138 ***** TEST 56 *****
PRIORITY INTERRUPT TESTS
SET PS TO ALL BR LEVELS EQUAL OR GREATER THAN
THE KMC11 LEVEL, VERIFY THAT KMC11 DOES NOT INTERRUPT

4178 ***** TEST 57 *****
PRIORITY INTERRUPT TESTS
SET PS TO ALL BR LEVELS LESS THAN THE KMC11 LEVEL
VERIFY THAT THE KMC11 WILL INTERRUPT

4224 ***** TEST 60 *****
NPR TEST
TEST OF DAT0, 1 WORD FROM UPROC TO 11 MEMORY

4259 ***** TEST 61 *****
NPR TEST
TEST OF DATI, 1 WORD FROM 11 MEMORY TO UPROC

4297 ***** TEST 62 *****
NPR TEST
TEST OF DATOB, 1 BYTE FROM UPROC TO 11 MEMORY

4331 ***** TEST 63 *****
TEST OF EA BITS 16 AND 17
DO A DATO TO AN ADDRESS USING OUT BA BITS 16 AND 17
VERIFY CORRECT RESULTS

4372 ***** TEST 64 *****
TEST OF EA BITS 16 AND 17
DO A DATI USING IN BA BITS 16 AND 17
VERIFY CORRECT RESULTS

4410 ***** TEST 65 *****
NPR NON-EXISTENT MEMORY TEST
DO A DATO TO A NON-EXISTENT ADDRESS
VERIFY THAT THE NON-EXISTENT BIT SET IN IBUS REG 11

4447 ***** TEST 66 *****
NPR NON-EXISTENT MEMORY TEST
DO A DATI FROM A NON-EXISTENT ADDRESS
VERIFY THAT THE NON-EXISTENT BIT SET IN IBUS REG 11

4484 ***** TEST 67 *****
NPR TEST
USING DATO, NPR A BINARY COUNT (0-377)
FROM MICRO-PROCESSOR TO ALL AVAILABLE MEMORY

4546 ***** TEST 70 *****
ALU C BIT TEST
TEST THAT AN ADD OF 377 AND 377 WILL SET THE C BIT

4586 ***** TEST 71 *****
ALU TEST
TEST OF ALU FUNCTION SEL B WITH C BIT CLEARED
ALU FUNCTION (B) CODE=11
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4637 ***** TEST 72 *****
ALU TEST
TEST OF ALU FUNCTION SEL A WITH C BIT CLEARED
ALU FUNCTION (A) CODE=10
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4688 ***** TEST 73 *****
ALU TEST
TEST OF ALU FUNCTION A OR NOTB WITH C BIT CLEARED
ALU FUNCTION (A OR NOTB) CODE=12
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4739 ***** TEST 74 *****
ALU TEST
TEST OF ALU FUNCTION A AND B WITH C BIT CLEARED
ALU FUNCTION (A AND B) CODE=13
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4790 ***** TEST 75 *****

4791 ALU TEST
TEST OF ALU FUNCTION A OR B WITH C BIT CLEARED
ALU FUNCTION (A OR B) CODE=14
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4841 ***** TEST 76 *****
ALU TEST
TEST OF ALU FUNCTION A XOR B WITH C BIT CLEARED
ALU FUNCTION (A XOR B) CODE=15
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4892 ***** TEST 77 *****
ALU TEST
TEST OF ALU FUNCTION ADD WITH C BIT CLEARED
ALU FUNCTION (A PLUS B) CODE=00
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4943 ***** TEST 100 *****
ALU TEST
TEST OF ALU FUNCTION 2A W/C WITH C BIT CLEARED
ALU FUNCTION (A PLUS A PLUS C) CODE=6
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4994 ***** TEST 101 *****
ALU TEST
TEST OF ALU FUNCTION SUB WITH C BIT CLEARED
ALU FUNCTION (A-B) CODE=16
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5045 ***** TEST 102 *****
ALU TEST
TEST OF ALU FUNCTION ADD W/C WITH C BIT CLEARED
ALU FUNCTION (A PLUS B PLUS C) CODE=01
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5096 ***** TEST 103 *****
ALU TEST
TEST OF ALU FUNCTION SUB W/C WITH C BIT CLEARED
ALU FUNCTION (A-B-C) CODE=2
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5147 ***** TEST 104 *****
ALU TEST
TEST OF ALU FUNCTION INC A WITH C BIT CLEARED
ALU FUNCTION (A PLUS 1) CODE=3
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5198 ***** TEST 105 *****
ALU TEST
TEST OF ALU FUNCTION 2A WITH C BIT CLEARED
ALU FUNCTION (A PLUS A) CODE=5
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5249 ***** TEST 106 *****
ALU TEST
TEST OF ALU FUNCTION A PLUS C WITH C BIT CLEARED
ALU FUNCTION (A PLUS C) CODE=4
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5300 ***** TEST 107 *****
ALU TEST
TEST OF ALU FUNCTION 2'S COMP SUB WITH C BIT CLEARED
ALU FUNCTION (A-B-1) CODE=17
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5351 ***** TEST 110 *****
ALU TEST
TEST OF ALU FUNCTION DEC A WITH C BIT CLEARED
ALU FUNCTION (A-1) CODE=7
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5402 ***** TEST 111 *****
ALU TEST
TEST OF ALU FUNCTION SEL B WITH C BIT SET
ALU FUNCTION (B) CODE=11
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA

5407 PERFORM THE FUNCTION, VERIFY THE RESULTS

5453 ***** TEST 112 *****
ALU TEST
TEST OF ALU FUNCTION SEL A WITH C BIT SET
ALU FUNCTION (A) CODE=10
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5504 ***** TEST 113 *****
ALU TEST
TEST OF ALU FUNCTION A OR NOTB WITH C BIT SET
ALU FUNCTION (A OR NOTB) CODE=12
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5555 ***** TEST 114 *****
ALU TEST
TEST OF ALU FUNCTION A AND B WITH C BIT SET
ALU FUNCTION (A AND B) CODE=13
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5606 ***** TEST 115 *****
ALU TEST
TEST OF ALU FUNCTION A OR B WITH C BIT SET
ALU FUNCTION (A OR B) CODE=14
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5657 ***** TEST 116 *****
ALU TEST
TEST OF ALU FUNCTION A XOR B WITH C BIT SET
ALU FUNCTION (A XOR B) CODE=15
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5708 ***** TEST 117 *****
ALU TEST
TEST OF ALU FUNCTION ADD WITH C BIT SET
ALU FUNCTION (A PLUS B) CODE=00
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

- 5759 ***** TEST 120 *****
 ALU TEST
 TEST OF ALU FUNCTION 2A W/C WITH C BIT SET
 ALU FUNCTION (A PLUS A PLUS C) CODE=6
 LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
 PERFORM THE FUNCTION, VERIFY THE RESULTS

- 5810 ***** TEST 121 *****
 ALU TEST
 TEST OF ALU FUNCTION SUB WITH C BIT SET
 ALU FUNCTION (A-B) CODE=16
 LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
 PERFORM THE FUNCTION, VERIFY THE RESULTS

- 5861 ***** TEST 122 *****
 ALU TEST
 TEST OF ALU FUNCTION ADD W/C WITH C BIT SET
 ALU FUNCTION (A PLUS B PLUS C) CODE=01
 LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
 PERFORM THE FUNCTION, VERIFY THE RESULTS

- 5912 ***** TEST 123 *****
 ALU TEST
 TEST OF ALU FUNCTION SUB W/C WITH C BIT SET
 ALU FUNCTION (A-B-C) CODE=2
 LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
 PERFORM THE FUNCTION, VERIFY THE RESULTS

- 5963 ***** TEST 124 *****
 ALU TEST
 TEST OF ALU FUNCTION INC A WITH C BIT SET
 ALU FUNCTION (A PLUS 1) CODE=3

- 5967 LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
 PERFORM THE FUNCTION, VERIFY THE RESULTS

- 6014 ***** TEST 125 *****
 ALU TEST
 TEST OF ALU FUNCTION 2A WITH C BIT SET
 ALU FUNCTION (A PLUS A) CODE=5
 LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
 PERFORM THE FUNCTION, VERIFY THE RESULTS

- 6065 ***** TEST 126 *****
 ALU TEST
 TEST OF ALU FUNCTION A PLUS C WITH C BIT SET
 ALU FUNCTION (A PLUS C) CODE=4
 LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
 PERFORM THE FUNCTION, VERIFY THE RESULTS

- 6116 ***** TEST 127 *****
ALU TEST
TEST OF ALU FUNCTION 2'S COMP SUB WITH C BIT SET
ALU FUNCTION (A-B-1) CODE=17
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS
- 6167 ***** TEST 130 *****
ALU TEST
TEST OF ALU FUNCTION DEC A WITH C BIT SET
ALU FUNCTION (A-1) CODE=7
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS
- 6218 ***** TEST 131 *****
TEST OF PROGRAM CLOCK BIT
DO A MASTER CLEAR, VERIFY THAT PROGRAM CLOCK IS SET
WRITE PROGRAM CLOCK BIT TO A ONE, VERIFY THAT IT CLEARS,
AND THEN SETS SOME TIME LATER
- 6269 ***** TEST 132 *****
FORCE POWER FAIL TEST
SET FORCE POWER FAIL BIT VERIFY THAT PROCESSOR TRAPS TO 24
GOING DOWN AND COMING UP. VERIFY ALSO THAT BUS INIT WAS
BLOCKED FROM GETTING TO THE KMC DURING THE POWER FAIL
- 6317 ***** TEST 133 *****
MICRO-PROCESSOR NOISE TEST
WRITE ALL ZERO'S THEN ALL ONE'S THEN A DATA PATTERN
TO THE IBUS* AND IBUS REGISTERS AND TO THE SP AND MAIN MEM
THEN GO BACK AND READ THE DATA PATERNS TO VERIFY THAT
READING AND WRITING OF OTHER LOCATIONS AND REGISTERS
DID NOT CHANGE THE DATA.

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.TITLE MAINDEC-11-DZKCC-A
:*COPYRIGHT (C) 1976
:*DIGITAL EQUIPMENT CORP.
:*MAYNARD, MASS. 01754
:*
:*PROGRAM BY DINESH GORADIA
:*
:*THIS PROGRAM WAS ASSEMBLED USING THE PDP-11 MAINDEC SYSMAC
:*PACKAGE (MAINDEC-11-DZQAC-C3), JAN 19, 1977.
:*

.*MAINDEC-11-DZKCC-A BASIC KMC11 CONTROLLER TEST
.*COPYRIGHT 1976, DIGITAL EQUIPMENT CORP., MAYNARD, MASS. 01754
.*-----

:STARTING PROCEDURE
:LOAD PROGRAM
:LOAD ADDRESS 000200
:SMR=0 AUTOSIZE KMC11
:SMO7=1 USE CURRENT KMC11 PARAMETERS
:SMO0=1 INPUT NEW KMC11 PARAMETERS
:PRESS START
:PROGRAM WILL TYPE "MAINDEC-11-DZKCC-A BASIC KMC11 CONTROLLER TEST"
:PROGRAM WILL TYPE STATUS MAP
:PROGRAM WILL TYPE "R" TO INDICATE THAT TESTING HAS STARTED
:AT THE END OF A PASS, PROGRAM WILL TYPE PASS COMPLETE MESSAGE
:AND THEN RESUME TESTING
:SUBSEQUENT RESTARTS WILL NOT TYPE PROGRAM TITLE

.SBTTL BASIC DEFINITIONS

001200

.*INITIAL ADDRESS OF THE STACK POINTER *** 1200 ***
STACK= 1200
.EQUIV EMT,ERROR ;;BASIC DEFINITION OF ERROR CALL
.EQUIV IOT,SCOPE ;;BASIC DEFINITION OF SCOPE CALL

.*MISCELLANEOUS DEFINITIONS
HT= 11 ;;CODE FOR HORIZONTAL TAB
LF= 12 ;;CODE FOR LINE FEED
CR= 15 ;;CODE FOR CARRIAGE RETURN
CRLF= 200 ;;CODE FOR CARRIAGE RETURN-LINE FEED
PS= 177776 ;;PROCESSOR STATUS WORD
.EQUIV PS,PSW
STKLMT= 177774 ;;STACK LIMIT REGISTER
PIRQ= 177772 ;;PROGRAM INTERRUPT REQUEST REGISTER
DSWR= 177570 ;;HARDWARE SWITCH REGISTER
DDISP= 177570 ;;HARDWARE DISPLAY REGISTER

000000
000001
000002

.*GENERAL PURPOSE REGISTER DEFINITIONS
R0= %0 ;;GENERAL REGISTER
R1= %1 ;;GENERAL REGISTER
R2= %2 ;;GENERAL REGISTER

57	000003	R3=	%3	::	GENERAL REGISTER
58	000004	R4=	%4	::	GENERAL REGISTER
59	000005	R5=	%5	::	GENERAL REGISTER
60	000006	R6=	%6	::	GENERAL REGISTER
61	000007	R7=	%7	::	GENERAL REGISTER
62	000006	SP=	%6	::	STACK POINTER
63	000007	PC=	%7	::	PROGRAM COUNTER

.*PRIORITY LEVEL DEFINITIONS

66	000000	PRO=	0	::	PRIORITY LEVEL 0
67	000040	PR1=	40	::	PRIORITY LEVEL 1
68	000100	PR2=	100	::	PRIORITY LEVEL 2
69	000140	PR3=	140	::	PRIORITY LEVEL 3
70	000200	PR4=	200	::	PRIORITY LEVEL 4
71	000240	PR5=	240	::	PRIORITY LEVEL 5
72	000300	PR6=	300	::	PRIORITY LEVEL 6
73	000340	PR7=	340	::	PRIORITY LEVEL 7

.*"SWITCH REGISTER" SWITCH DEFINITIONS

76	100000	SW15=	100000		
77	040000	SW14=	40000		
78	020000	SW13=	20000		
79	010000	SW12=	10000		
80	004000	SW11=	4000		
81	002000	SW10=	2000		
82	001000	SW09=	1000		
83	000400	SW08=	400		
84	000200	SW07=	200		
85	000100	SW06=	100		
86	000040	SW05=	40		
87	000020	SW04=	20		
88	000010	SW03=	10		
89	000004	SW02=	4		
90	000002	SW01=	2		
91	000001	SW00=	1		
92		.EQUIV	SW09, SW9		
93		.EQUIV	SW08, SW8		
94		.EQUIV	SW07, SW7		
95		.EQUIV	SW06, SW6		
96		.EQUIV	SW05, SW5		
97		.EQUIV	SW04, SW4		
98		.EQUIV	SW03, SW3		
99		.EQUIV	SW02, SW2		
100		.EQUIV	SW01, SW1		
101		.EQUIV	SW00, SW0		

.*DATA BIT DEFINITIONS (BIT00 TO BIT15)

104	100000	BIT15=	100000
105	040000	BIT14=	40000
106	020000	BIT13=	20000
107	010000	BIT12=	10000
108	004000	BIT11=	4000
109	002000	BIT10=	2000
110	001000	BIT09=	1000
111	000400	BIT08=	400
112	000200	BIT07=	200

BASIC DEFINITIONS

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113      000100      BIT06= 100
114      000040      BIT05= 40
115      000020      BIT04= 20
116      000010      BIT03= 10
117      000004      BIT02= 4
118      000002      BIT01= 2
119      000001      BIT00= 1
120      .EQUIV      BIT09,BIT9
121      .EQUIV      BIT08,BIT8
122      .EQUIV      BIT07,BIT7
123      .EQUIV      BIT06,BIT6
124      .EQUIV      BIT05,BIT5
125      .EQUIV      BIT04,BIT4
126      .EQUIV      BIT03,BIT3
127      .EQUIV      BIT02,BIT2
128      .EQUIV      BIT01,BIT1
129      .EQUIV      BIT00,BIT0
130
131      ;#BASIC "CPU" TRAP VECTOR ADDRESSES
132      000004      ERRVEC= 4          ;; TIME OUT AND OTHER ERRORS
133      000010      RESVEC= 10         ;; RESERVED AND ILLEGAL INSTRUCTIONS
134      000014      TBITVEC=14        ;; "T" BIT
135      000014      TRTVEC= 14        ;; TRACE TRAP
136      000014      BPTVEC= 14        ;; BREAKPOINT TRAP (BPT)
137      000020      IOTVEC= 20        ;; INPUT/OUTPUT TRAP (IOT) **SCOPE**
138      000024      PWRVEC= 24        ;; POWER FAIL
139      000030      EMTVEC= 30        ;; EMULATOR TRAP (EMT) **ERROR**
140      000034      TRAPVEC=34        ;; "TRAP" TRAP
141      000060      TKVEC= 60         ;; TTY KEYBOARD VECTOR
142      000064      TPVEC= 64         ;; TTY PRINTER VECTOR
143      000240      PIRQVEC=240       ;; PROGRAM INTERRUPT REQUEST VECTOR
144
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146
147
148      ; INSTRUCTION DEFINITIONS
149      ;-----
150
151      005746      PUSH1SP=5746      ; DECREMENT PROCESSOR STACK 1 WORD
152      005726      POP1SP=5726      ; INCREMENT PROCESSOR STACK 1 WORD
153      010046      PUSHRO=10046     ; SAVE R0 ON STACK
154      012600      POPRO=12600      ; RESTORE R0 FROM STACK
155      024646      PUSH2SP=24646   ; DECREMENT STACK TWICE
156      022626      POP2SP=22626    ; INCREMENT STACK TWICE
157      .EQUIV EMT,HLT ; BASIC DEFINITION OF ERROR CALL
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TRAPCATCHER FOR UNEXPECTED INTERUPTS

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-----
: TRAPCATCAER FOR ILLEGAL INTERRUPTS
: THE STANDARD "TRAP CATCHER" IS PLACED
: BETWEEN ADDRESS 0 TO ADDRESS 776.
: IT LOOKS LIKE "PC+2 HALT".
-----
*****

.=0
      .WORD 0,0
; STANDARD INTERRUPT VECTORS
-----

.=20
      $SCOPE          ; SCOPE LOOP HANDLER.
      PR7             ; SERVICE AT LEVEL 7.
      $PWRDN          ; POWER FAIL HANDLER
      PR7             ; SERVICE AT LEVEL 7
      $ERRR           ; ERROR HANDLER
      PR7             ; SERVICE AT LEVEL 7
      $STRAP          ; GENERAL HANDLER DISPATCH SERVICE
      PR7             ; SERVICE AT LEVEL 7

.SBTTL ACT11 HOOKS

; *****
; HOOKS REQUIRED BY ACT11
      $SVPC=.         ; SAVE PC
      .=46
      $ENDAD          ; ;1)SET LOC.46 TO ADDRESS OF SENDAD IN .SEOP
      .=52
      .WORD 0         ; ;2)SET LOC.52 TO ZERO
      .=$SVPC        ; ; RESTORE PC

.=174
DISPREG:0           ; SOFTWARE DISPLAY REGISTER
SWREG: 0           ; SOFTWARE SWITCH REGISTER

.=200
      JMP .START     ; GO TO START OF PROGRAM

.=1000
MTITLE: .ASCII <200><12>/MAINDEC-11-DZKCC-A/<200>
        .ASCIZ /BASIC KMC11 CONTROLLER TEST/<200>

DSWR = 177570
DDISP = 177570

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.SBTTL COMMON TAGS

*THIS TABLE CONTAINS VARIOUS COMMON STORAGE LOCATIONS
*USED IN THE PROGRAM.

SCMTAG: .=1200

;; START OF COMMON TAGS

.WORD 0
\$TSTNM: .BYTE 0
\$ERFLG: .BYTE 0
\$ICNT: .WORD 0
\$LPADR: .WORD 0
\$LPERR: .WORD 0
\$ERTTL: .WORD 0
\$ITEMB: .BYTE 0
\$ERMAX: .BYTE 1
\$ERRPC: .WORD 0
\$GDADR: .WORD 0
\$BDADR: .WORD 0
\$GDDAT: .WORD 0
\$BDDAT: .WORD 0
\$AUTOB: .BYTE 0
\$INTAG: .BYTE 0
\$SWR: .WORD DSWR
\$DISPLAY: .WORD DDISP
\$TKS: 177560
\$TKB: 177562
\$TPS: 177564
\$TPB: 177566
\$NULL: .BYTE 0
\$FILLS: .BYTE 2
\$FILLC: .BYTE 12
\$TPFLG: .BYTE 0
\$REGAD: .WORD 0
\$REG0: .WORD 0
\$REG1: .WORD 0
\$REG2: .WORD 0
\$REG3: .WORD 0
\$REG4: .WORD 0
\$REG5: .WORD 0
\$TMP0: .WORD 0
\$TMP1: .WORD 0
\$TMP2: .WORD 0
\$TMP3: .WORD 0
\$TMP4: .WORD 0
\$TIMES: 0
\$QUES: .ASCII /?/
\$CRLF: .ASCII <15>
\$LF: .ASCII <12>

CONTAINS THE TEST NUMBER
CONTAINS ERROR FLAG
CONTAINS SUBTEST ITERATION COUNT
CONTAINS SCOPE LOOP ADDRESS
CONTAINS SCOPE RETURN FOR ERRORS
CONTAINS TOTAL ERRORS DETECTED
CONTAINS ITEM CONTROL BYTE
CONTAINS MAX. ERRORS PER TEST
CONTAINS PC OF LAST ERROR INSTRUCTION
CONTAINS ADDRESS OF 'GOOD' DATA
CONTAINS ADDRESS OF 'BAD' DATA
CONTAINS 'GOOD' DATA
CONTAINS 'BAD' DATA
RESERVED--NOT TO BE USED
AUTOMATIC MODE INDICATOR
INTERRUPT MODE INDICATOR
ADDRESS OF SWITCH REGISTER
ADDRESS OF DISPLAY REGISTER
TTY KBD STATUS
TTY KBD BUFFER
TTY PRINTER STATUS REG. ADDRESS
TTY PRINTER BUFFER REG. ADDRESS
CONTAINS NULL CHARACTER FOR FILLS
CONTAINS # OF FILLER CHARACTERS REQUIRED
INSERT FILL CHARS. AFTER A "LINE FEED"
"TERMINAL AVAILABLE" FLAG (BIT<07>=0=YES)
CONTAINS THE ADDRESS FROM WHICH (\$REG0) WAS OBTAINED
CONTAINS ((\$REGAD)+0)
CONTAINS ((\$REGAD)+2)
CONTAINS ((\$REGAD)+4)
CONTAINS ((\$REGAD)+6)
CONTAINS ((\$REGAD)+10)
CONTAINS ((\$REGAD)+12)
USER DEFINED
USER DEFINED
USER DEFINED
USER DEFINED
USER DEFINED
MAX. NUMBER OF ITERATIONS
QUESTION MARK
CARRIAGE RETURN
LINE FEED

.SBTTL APT MAILBOX-ETABLE

264
265
266
267 001316
268 001316 000000
269 001320 000000
270 001322 000000
271 001324 000000
272 001326 000000
273 001330 000000
274 001332 000000
275 001334 000000
276 001336
277 001336 002
278 001337 000
279 001340 000000
280 001342 000000
281 001344 000000
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288 001346 000
289 001347 000
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294 001350 000000
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299 001356 000
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306 001370 000000
307 001372 000000
308 001374 000000
309 001376 000000
310 001400 000000
311 001402 000000
312 001404 000000
313 001406 000000
314 001410 000000
315 001412 000000
316 001414 000000
317 001416 000000
318 001420 000000
319 001422 000000

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:EVEN
$MAIL:
$MSGTY: .WORD  AMSGTY  ;; APT MAILBOX
$FATAL: .WORD  AFATAL  ;; MESSAGE TYPE CODE
$TESTN: .WORD  ATESTN  ;; FATAL ERROR NUMBER
$PASS:  .WORD  APASS   ;; TEST NUMBER
$DEVCT: .WORD  ADEVCT  ;; PASS COUNT
$UNIT:  .WORD  AUNIT   ;; DEVICE COUNT
$MSGAD: .WORD  AMSGAD  ;; I/O UNIT NUMBER
$MSGLG: .WORD  AMSGLG  ;; MESSAGE ADDRESS
SETABLE:      ;; MESSAGE LENGTH
$ENV:  .BYTE  AENV     ;; APT ENVIRONMENT TABLE
$ENVM: .BYTE  AENVM   ;; ENVIRONMENT BYTE
$SWREG: .WORD  ASWREG  ;; ENVIRONMENT MODE BITS
$USWR:  .WORD  AUSWR   ;; APT SWITCH REGISTER
$CPUOP: .WORD  ACPUOP  ;; USER SWITCHES
: *
: * 11/04=01,11/05=02,11/20=03,11/40=04,11/45=05
: * 11/70=06,POQ=07,Q=10
: * BIT 10=REAL TIME CLOCK
: * BIT 9=FLOATING POINT PROCESSOR
: * BIT 8=MEMORY MANAGEMENT
$MAMS1: .BYTE  AMAMS1  ;; HIGH ADDRESS, M.S. BYTE
$MTYP1: .BYTE  AMTYP1  ;; MEM. TYPE, BLK#1
: * MEM. TYPE BYTE -- (HIGH BYTE)
: * 900 NSEC CORE=001
: * 300 NSEC BIPOLAR=002
: * 500 NSEC MOS=003
$MADR1: .WORD  AMADR1  ;; HIGH ADDRESS, BLK#1
: * MEM. LAST ADDR.=3 BYTES, THIS WORD AND LOW OF "TYPE" ABOVE
$MAMS2: .BYTE  AMAMS2  ;; HIGH ADDRESS, M.S. BYTE
$MTYP2: .BYTE  AMTYP2  ;; MEM. TYPE, BLK#2
$MADR2: .WORD  AMADR2  ;; MEM. LAST ADDRESS, BLK#2
$MAMS3: .BYTE  AMAMS3  ;; HIGH ADDRESS, M.S. BYTE
$MTYP3: .BYTE  AMTYP3  ;; MEM. TYPE, BLK#3
$MADR3: .WORD  AMADR3  ;; MEM. LAST ADDRESS, BLK#3
$MAMS4: .BYTE  AMAMS4  ;; HIGH ADDRESS, M.S. BYTE
$MTYP4: .BYTE  AMTYP4  ;; MEM. TYPE, BLK#4
$MADR4: .WORD  AMADR4  ;; MEM. LAST ADDRESS, BLK#4
$VECT1: .WORD  AVECT1  ;; INTERRUPT VECTOR#1, BUS PRIORITY#1
$VECT2: .WORD  AVECT2  ;; INTERRUPT VECTOR#2, BUS PRIORITY#2
$BASE:  .WORD  ABASE   ;; BASE ADDRESS OF EQUIPMENT UNDER TEST
$DEVN:  .WORD  ADEVN   ;; DEVICE MAP
$CDW1:  .WORD  ACDW1   ;; CONTROLLER DESCRIPTION WORD#1
$CDW2:  .WORD  ACDW2   ;; CONTROLLER DESCRIPTION WORD#2
$DDW0:  .WORD  ADDW0   ;; DEVICE DESCRIPTOR WORD#0
$DDW1:  .WORD  ADDW1   ;; DEVICE DESCRIPTOR WORD#1
$DDW2:  .WORD  ADDW2   ;; DEVICE DESCRIPTOR WORD#2
$DDW3:  .WORD  ADDW3   ;; DEVICE DESCRIPTOR WORD#3
$DDW4:  .WORD  ADDW4   ;; DEVICE DESCRIPTOR WORD#4
$DDW5:  .WORD  ADDW5   ;; DEVICE DESCRIPTOR WORD#5
$DDW6:  .WORD  ADDW6   ;; DEVICE DESCRIPTOR WORD#6
$DDW7:  .WORD  ADDW7   ;; DEVICE DESCRIPTOR WORD#7
$DDW8:  .WORD  ADDW8   ;; DEVICE DESCRIPTOR WORD#8

```

320 001424 000000
 321 001426 000000
 322 001430 000000
 323 001432 000000
 324 001434 000000
 325 001436 000000
 326 001440 000000
 327
 328
 329 001442
 330
 331
 332
 333
 334 001442 000000
 335 001444 000000
 336
 337
 338
 339 001446 000000
 340 001450 000000
 341 001452 000000
 342 001454 000000
 343 001456 000000
 344 001460 000000
 345 001462 000000
 346 001464 000001
 347 001466 000000
 348 001470 000001
 349 001472 000001
 350 001474 000001
 351 001476 000001
 352 001500 000000
 353
 354 001502 002072
 355 001504 002276
 356
 357
 358
 359 001506 000
 360 001510 001510
 361 001510 000
 362 001511 000
 363
 364

SDDW9: .WORD ADDW9 :; DEVICE DESCRIPTOR WORD#9
 SDDW10: .WORD ADDW10 :; DEVICE DESCRIPTOR WORD#10
 SDDW11: .WORD ADDW11 :; DEVICE DESCRIPTOR WORD#11
 SDDW12: .WORD ADDW12 :; DEVICE DESCRIPTOR WORD#12
 SDDW13: .WORD ADDW13 :; DEVICE DESCRIPTOR WORD#13
 SDDW14: .WORD ADDW14 :; DEVICE DESCRIPTOR WORD#14
 SDDW15: .WORD ADDW15 :; DEVICE DESCRIPTOR WORD#15

SETEND:

PROGRAM CONTROL PARAMETERS

NEXT: .WORD 0 ; ADDRSS OF NEXT TEST TO BE EXECUTED
 LOCK: .WORD 0 ; ADDRESS FOR LOCK CURRENT DATA

PROGRAM VARIABLES

STRTSM: .WORD 0 ; SWITCHES AT START OF PROGRAM
 STAT: .WORD 0 ; KM STATUS WORD STORAGE
 CLKX: .WORD 0
 MASKX: .WORD 0
 SAVSP: .WORD 0 ; STACK POINTER STORAGE
 SAVPC: .WORD 0 ; PROGRAM COUNTER STORAGE
 ZERO: .WORD 0
 ONE: .WORD 1
 MEM LIM: .WORD 0 ; HIGHEST LOCATION FOR NPR'S
 KRACTV: .BLKW 1 ; KMC11 SELECTED ACTIVE
 KMINUM: .BLKW 1 ; OCTAL NUMBER OF KMC11'S
 SAVACT: .BLKW 1 ; ORIGINAL ACTIVE DEVICES.
 SAVNUM: .BLKW 1 ; WORKABLE NUMBER.
 RUN: .WORD 0 ; POINTER TO RUNNING DEVICES
 CREAM: .WORD KM.MAP-6 ; TABLE POINTER
 MILK: .WORD CNT.MAP-4 ; TABLE POINTER

PROGRAM CONTROL FLAGS

INIFLG: .BYTE 0 ; PROGRAM INITIALIZING FLAG
 LOKFLG: .BYTE 0 ; LOCK ON CURRENT TEST FLAG
 QV.FLG: .BYTE 0 ; QUICK VERIFY FLAG
 .EVEN ; ON FIRST PASS OF EACH KMC11 ITERATIONS WILL BE SUPPRES

ERROR POINTER TABLE

.SBTTL ERROR POINTER TABLE

;;THIS TABLE CONTAINS THE INFORMATION FOR EACH ERROR THAT CAN OCCUR.
;;THE INFORMATION IS OBTAINED BY USING THE INDEX NUMBER FOUND IN
;;LOCATION SITEMB. THIS NUMBER INDICATES WHICH ITEM IN THE TABLE IS PERTINENT.
;;NOTE1: IF SITEMB IS 0 THE ONLY PERTINENT DATA IS (SERRPC).
;;NOTE2: EACH ITEM IN THE TABLE CONTAINS 4 POINTERS EXPLAINED AS FOLLOWS:

;; * EM ;;POINTS TO THE ERROR MESSAGE
;; * DH ;;POINTS TO THE DATA HEADER
;; * DT ;;POINTS TO THE DATA
;; * DF ;;POINTS TO THE DATA FORMAT

SERRTB:
.EVEN
;*

;; DOES NOT APPLY IN THIS DIAGNOSTIC.

365
366
367
368
369
370
371
372
373
374
375
376
377
378
379 001512
380
381
382 001512 000000
383 001514 000000
384 001516 000000
385 001520 035746
386 001522 036632
387 001524 037112
388 001526 036013
389 001530 036673
390 001532 037124
391 001534 036054
392 001536 036731
393 001540 037142
394 001542 036102
395 001544 036752
396 001546 037154
397 001550 036102
398 001552 037014
399 001554 037172
400 001556 036143
401 001560 036731
402 001562 037210
403 001564 036165
404 001566 037055
405 001570 037172
406 001572 036207
407 001574 000000
408 001576 000000
409 001600 036243
410 001602 000000
411 001604 000000
412 001606 036307
413 001610 036731
414 001612 037142
415 001614 036321
416 001616 037055
417 001620 037172
418 001622 036343
419 001624 037055
420 001626 037172

DF
0
0
0
EM1 ; ERROR 1
DH1
DT1
EM2 ; ERROR 2
DH2
DT2
EM3 ; ERROR 3
DH3
DT3
EM4 ; ERROR 4
DH4
DT4
EM4 ; ERROR 5
DH5
DT5
EM5 ; ERROR 6
DH3
DT6
EM6 ; ERROR 7
DH6
DT5
EM7 ; ERROR 10
0
0
EM10 ; ERROR 11
0
EM11 ; ERROR 12
DH3
DT3
EM12 ; ERROR 13
DH6
DT5
EM13 ; ERROR 14
DH6
DT5

421	001630	036355	EM14	
422	001632	036731	DH3	; ERROR 15
423	001634	037210	DT6	
424	001636	036367	EM15	
425	001640	036752	DH4	; ERROR 16
426	001642	037154	DT4	
427	001644	036413	EM16	
428	001646	000000	0	; ERROR 17
429	001650	000000	0	
430	001652	036443	EM17	
431	001654	000000	0	; ERROR 20
432	001656	000000	0	
433	001660	036307	EM11	
434	001662	037055	DH6	; ERROR 21
435	001664	037172	DT5	
436	001666	036471	EM20	
437	001670	036731	DH3	; ERROR 22
438	001672	037222	DT7	
439	001674	036524	EM21	
440	001676	036731	DH3	; ERROR 23
441	001700	037142	DT3	
442	001702	036471	EM20	
443	001704	000000	0	; ERROR 24
444	001706	000000	0	
445	001710	036573	EM22	
446	001712	036731	DH3	; ERROR 25
447	001714	037142	DT3	
448		002034		

. =2034
.SBTTL APT PARAMETER BLOCK

```

*****
;SET LOCATIONS 24 AND 44 AS REQUIRED FOR APT
*****
.SX=      ;SAVE CURRENT LOCATION
.=24     ;SET POWER FAIL TO POINT TO START OF PROGRAM
200      ;FOR APT START UP
.=44     ;POINT TO APT INDIRECT ADDRESS PNTR.
$APTHDR  ;POINT TO APT REORDER BLOCK
.=.SX    ;RESET LOCATION COUNTER
*****
;SETUP APT PARAMETER BLOCK AS DEFINED IN THE APT-POP11 DIAGNOSTIC
;INTERFACE SPEC.

```

464	002034		\$APTHD:	
465	002034	000000	\$HIPTS:	.WORD 0 ; TWO HIGH BITS OF 18 BIT MAILBOX ADDR.
466	002036	001316	\$MADR:	.WORD \$MAIL ; ADDRESS OF APT MAILBOX (BITS 0-15)
467	002040	000132	\$TSTM:	.WORD 90 ; RUN TIM OF LONGEST TEST
468	002042	000137	\$PASTM:	.WORD 95 ; RUN TIME IN SECS. OF 1ST PASS ON 1 UNIT (QUICK VERIFY)
469	002044	000137	\$UNITM:	.WORD 95 ; ADDITIONAL RUN TIME (SECS) OF A PASS FOR EACH ADDITIONAL UNIT
470	002046	000052		.WORD \$ETEND-\$MAIL/2 ; LENGTH MAILBOX-ETABLE(WORDS)
471				

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472
473 ;KMC11 CONTROL INDICATORS FOR CURRENT KMC11 UNDER TEST
474 -----
475
476 002050 000000 STAT1: 0
477 002052 000000 STAT2: 0
478 002054 000000 STAT3: 0
479
480 ;KMC11 VECTOR AND REGISTER INDIRECT POINTERS
481 -----
482
483 002056 000000 KMRVEC: 0 ; POINTER TO KMC11 RECEIVER INTERRUPT VECTOR
484 002060 000000 KMRLVL: 0 ; POINTER TO KMC11 RECEIVER INTERRUPT SERVICE PS
485 002062 000000 KMTVEC: 0 ; POINTER TO KMC11 TRANSMITTER INTERRUPT VECTOR
486 002064 000000 KMTLVL: 0 ; POINTER TO KMC11 TRANSMITTER INTERRUPT SERVICE PS
487 002066 000000 KMCSR: 0 ; POINTER TO KMC11 CONTROL STATUS REGISTER
488 002070 000000 KMCSRH: 0 ; POINTER TO KMC11 CONTROL STATUS REGISTER HIGH BYTE.
489 002072 000000 KMCTL: 0 ; POINTER TO KMC11 CONTROL OUT REGISTER
490 002074 000000 KMP04: 0 ; POINTER TO KMC11 PORT REGISTER(SEL 4)
491 002076 000000 KMP06: 0 ; POINTER TO KMC11 PORT REGISTER(SEL 6)
492
493 ;TEMP STORAGE
494 -----
495
496 ;TEMP: 0
497 ;.=.+40
498
499 ;KMC11 STATUS TABLE AND ADDRESS ASSIGNMENTS
500 -----
501
502 . =2100
503 002100 000001 KM.MAP:
504 002100 000001 KMC00: .BLKW 1 ; CONTROL STATUS REGISTER FOR KMC11 NUMBER 00
505 002102 000001 KMS100: .BLKW 1 ; VECTOR FOR KMC11 NUMBER 00
506 002104 000001 KMS200: .BLKW 1 ; DDCMP LINE# FOR KMC11 NUMBER 00
507 002106 000001 KMS300: .BLKW 1 ; 3RD STATUS WORD
508
509 002110 000001 KMC01: .BLKW 1 ; CONTROL STATUS REGISTER FOR KMC11 NUMBER 01
510 002112 000001 KMS101: .BLKW 1 ; VECTOR FOR KMC11 NUMBER 01
511 002114 000001 KMS201: .BLKW 1 ; DDCMP LINE# FOR KMC11 NUMBER 01
512 002116 000001 KMS301: .BLKW 1 ; 3RD STATUS WORD
513
514 002120 000001 KMC02: .BLKW 1 ; CONTROL STATUS REGISTER FOR KMC11 NUMBER 02
515 002122 000001 KMS102: .BLKW 1 ; VECTOR FOR KMC11 NUMBER 02
516 002124 000001 KMS202: .BLKW 1 ; DDCMP LINE# FOR KMC11 NUMBER 02
517 002126 000001 KMS302: .BLKW 1 ; 3RD STATUS WORD
518
519 002130 000001 KMC03: .BLKW 1 ; CONTROL STATUS REGISTER FOR KMC11 NUMBER 03
520 002132 000001 KMS103: .BLKW 1 ; VECTOR FOR KMC11 NUMBER 03
521 002134 000001 KMS203: .BLKW 1 ; DDCMP LINE# FOR KMC11 NUMBER 03
522 002136 000001 KMS303: .BLKW 1 ; 3RD STATUS WORD
523
524 002140 000001 KMC04: .BLKW 1 ; CONTROL STATUS REGISTER FOR KMC11 NUMBER 04
525 002142 000001 KMS104: .BLKW 1 ; VECTOR FOR KMC11 NUMBER 04
526 002144 000001 KMS204: .BLKW 1 ; DDCMP LINE# FOR KMC11 NUMBER 04
527 002146 000001 KMS304: .BLKW 1 ; 3RD STATUS WORD
    
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528					
529	002150	000001	KMCR05: .BLKW	1	;CONTROL STATUS REGISTER FOR KMC11 NUMBER 05
530	002152	000001	KMS105: .BLKW	1	;VECTOR FOR KMC11 NUMBER 05
531	002154	000001	KMS205: .BLKW	1	;DDCMP LINE# FOR KMC11 NUMBER 05
532	002156	000001	KMS305: .BLKW	1	;3RD STATUS WORD
533					
534	002160	000001	KMCR06: .BLKW	1	;CONTROL STATUS REGISTER FOR KMC11 NUMBER 06
535	002162	000001	KMS106: .BLKW	1	;VECTOR FOR KMC11 NUMBER 06
536	002164	000001	KMS206: .BLKW	1	;DDCMP LINE# FOR KMC11 NUMBER 06
537	002166	000001	KMS306: .BLKW	1	;3RD STATUS WORD
538					
539	002170	000001	KMCR07: .BLKW	1	;CONTROL STATUS REGISTER FOR KMC11 NUMBER 07
540	002172	000001	KMS107: .BLKW	1	;VECTOR FOR KMC11 NUMBER 07
541	002174	000001	KMS207: .BLKW	1	;DDCMP LINE# FOR KMC11 NUMBER 07
542	002176	000001	KMS307: .BLKW	1	;3RD STATUS WORD
543					
544	002200	000001	KMCR10: .BLKW	1	;CONTROL STATUS REGISTER FOR KMC11 NUMBER 10
545	002202	000001	KMS110: .BLKW	1	;VECTOR FOR KMC11 NUMBER 10
546	002204	000001	KMS210: .BLKW	1	;DDCMP LINE# FOR KMC11 NUMBER 10
547	002206	000001	KMS310: .BLKW	1	;3RD STATUS WORD
548					
549	002210	000001	KMCR11: .BLKW	1	;CONTROL STATUS REGISTER FOR KMC11 NUMBER 11
550	002212	000001	KMS111: .BLKW	1	;VECTOR FOR KMC11 NUMBER 11
551	002214	000001	KMS211: .BLKW	1	;DDCMP LINE# FOR KMC11 NUMBER 11
552	002216	000001	KMS311: .BLKW	1	;3RD STATUS WORD
553					
554	002220	000001	KMCR12: .BLKW	1	;CONTROL STATUS REGISTER FOR KMC11 NUMBER 12
555	002222	000001	KMS112: .BLKW	1	;VECTOR FOR KMC11 NUMBER 12
556	002224	000001	KMS212: .BLKW	1	;DDCMP LINE# FOR KMC11 NUMBER 12
557	002226	000001	KMS312: .BLKW	1	;3RD STATUS WORD
558					
559	002230	000001	KMCR13: .BLKW	1	;CONTROL STATUS REGISTER FOR KMC11 NUMBER 13
560	002232	000001	KMS113: .BLKW	1	;VECTOR FOR KMC11 NUMBER 13
561	002234	000001	KMS213: .BLKW	1	;DDCMP LINE# FOR KMC11 NUMBER 13
562	002236	000001	KMS313: .BLKW	1	;3RD STATUS WORD
563					
564	002240	000001	KMCR14: .BLKW	1	;CONTROL STATUS REGISTER FOR KMC11 NUMBER 14
565	002242	000001	KMS114: .BLKW	1	;VECTOR FOR KMC11 NUMBER 14
566	002244	000001	KMS214: .BLKW	1	;DDCMP LINE# FOR KMC11 NUMBER 14
567	002246	000001	KMS314: .BLKW	1	;3RD STATUS WORD
568					
569	002250	000001	KMCR15: .BLKW	1	;CONTROL STATUS REGISTER FOR KMC11 NUMBER 15
570	002252	000001	KMS115: .BLKW	1	;VECTOR FOR KMC11 NUMBER 15
571	002254	000001	KMS215: .BLKW	1	;DDCMP LINE# FOR KMC11 NUMBER 15
572	002256	000001	KMS315: .BLKW	1	;3RD STATUS WORD
573					
574	002260	000001	KMCR16: .BLKW	1	;CONTROL STATUS REGISTER FOR KMC11 NUMBER 16
575	002262	000001	KMS116: .BLKW	1	;VECTOR FOR KMC11 NUMBER 16
576	002264	000001	KMS216: .BLKW	1	;DDCMP LINE# FOR KMC11 NUMBER 16
577	002266	000001	KMS316: .BLKW	1	;3RD STATUS WORD
578					
579	002270	000001	KMCR17: .BLKW	1	;CONTROL STATUS REGISTER FOR KMC11 NUMBER 17
580	002272	000001	KMS117: .BLKW	1	;VECTOR FOR KMC11 NUMBER 17
581	002274	000001	KMS217: .BLKW	1	;DDCMP LINE# FOR KMC11 NUMBER 17
582	002276	000001	KMS317: .BLKW	1	;3RD STATUS WORD
583					

N03

DZKCC MACY11 27(1006) 12-MAY-77 18:34 PAGE 13
DZKCC.P11 21-MAR-77 17:19 APT PARAMETER BLOCK
584 002300 000000 KM.END: 000000

PAGE: 0039

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;KMC11 PASS COUNT AND ERROR COUNT TABLE

CNT.MAP:

```

PACT00: 0 ;PASS COUNT FOR KMC11 NUMBER 00
ERCT00: 0 ;ERROR COUNT FOR KMC11 NUMBER 00

PACT01: 0 ;PASS COUNT FOR KMC11 NUMBER 01
ERCT01: 0 ;ERROR COUNT FOR KMC11 NUMBER 01

PACT02: 0 ;PASS COUNT FOR KMC11 NUMBER 02
ERCT02: 0 ;ERROR COUNT FOR KMC11 NUMBER 02

PACT03: 0 ;PASS COUNT FOR KMC11 NUMBER 03
ERCT03: 0 ;ERROR COUNT FOR KMC11 NUMBER 03

PACT04: 0 ;PASS COUNT FOR KMC11 NUMBER 04
ERCT04: 0 ;ERROR COUNT FOR KMC11 NUMBER 04

PACT05: 0 ;PASS COUNT FOR KMC11 NUMBER 05
ERCT05: 0 ;ERROR COUNT FOR KMC11 NUMBER 05

PACT06: 0 ;PASS COUNT FOR KMC11 NUMBER 06
ERCT06: 0 ;ERROR COUNT FOR KMC11 NUMBER 06

PACT07: 0 ;PASS COUNT FOR KMC11 NUMBER 07
ERCT07: 0 ;ERROR COUNT FOR KMC11 NUMBER 07

PACT10: 0 ;PASS COUNT FOR KMC11 NUMBER 10
ERCT10: 0 ;ERROR COUNT FOR KMC11 NUMBER 10

PACT11: 0 ;PASS COUNT FOR KMC11 NUMBER 11
ERCT11: 0 ;ERROR COUNT FOR KMC11 NUMBER 11

PACT12: 0 ;PASS COUNT FOR KMC11 NUMBER 12
ERCT12: 0 ;ERROR COUNT FOR KMC11 NUMBER 12

PACT13: 0 ;PASS COUNT FOR KMC11 NUMBER 13
ERCT13: 0 ;ERROR COUNT FOR KMC11 NUMBER 13

PACT14: 0 ;PASS COUNT FOR KMC11 NUMBER 14
ERCT14: 0 ;ERROR COUNT FOR KMC11 NUMBER 14

PACT15: 0 ;PASS COUNT FOR KMC11 NUMBER 15
ERCT15: 0 ;ERROR COUNT FOR KMC11 NUMBER 15

PACT16: 0 ;PASS COUNT FOR KMC11 NUMBER 16
ERCT16: 0 ;ERROR COUNT FOR KMC11 NUMBER 16

PACT17: 0 ;PASS COUNT FOR KMC11 NUMBER 17
ERCT17: 0 ;ERROR COUNT FOR KMC11 NUMBER 17
    
```

638
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FORMAT OF STATUS TABLE

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00													
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	CSR											
I	C	O	N	T	R	O	L	I	R	E	G	I	S	T	E	R	I											
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I												
I	*	I	*	I	*	I	*	I	*	I	*	I	*	I	*	I	STAT1											
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I												
I	*	I	B	I	M	I	I	A	D	I	D	*	I	*	I	L	I	I	N	E	I	I	*	I	*	I		
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	

DEFINITION OF FORMAT

- CSR: CONTAINS KMC11 CSR ADDRESS
- STAT1: BITS 00-08 IS KMC11 VECTOR ADDRESS
 BIT14=1 ???? TURNAROUND CONNECTOR IS ON
 BIT14=0 NO TURNAROUND CONNECTOR
 BIT13=0 LINE UNIT IS AN M8201
 BIT13=1 LINE UNIT IS AN M8202
 BIT12=1 NO LINE UNIT
 BITS 09-11 IS KMC11 BR PRIORITY LEVEL
- STAT2: LOW BYTE IS SWITCH PAC#1 (DDCMP LINE NUMBER)
 HIGH BYTE IS SWITCH PAC#2 (BM873 BOOT ADD)
- STAT3: BIT0=1 DO FREE RUNNING TESTS ON KMC
 (MUST BE SET TO A ONE MANUALLY [PROGRAMS G AND H ONLY])

```

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699
700 002402 012737 000340 177776 .START: MOV #340,PS ;LOCK OUT INTERRUPTS
701 002410 012706 001200 MOV #STACK,SP ;SET UP STACK
702 002414 012737 007126 000024 MOV #SPWDM,2#24 ;SET UP POWER FAIL VECTOR
703 002422 013737 001472 001476 MOV #KMINUM,SAMNUM ;SAVE NUMBER OF DEVICES IN SYSTEM.
704 002430 005037 011416 CLR SWFLG ;CLEAR SOFT TIMEOUT FLAG
705 002434 105037 001203 CLRB SERFLG ;CLEAR ERROR FLAG
706 002440 105037 001511 CLRB QV.FLG ;ZERO QUICK VERIFY FLAG
707 002444 012737 002070 001502 MOV #KM.MAP-10,CREAM ;GET MAP POINTER.
708 002452 012737 002276 001504 MOV #CNT.MAP-4,MILK ;GET PASS COUNT MAP POINTER
709 002460 012737 100000 001500 MOV #BIT15,RUN ;POINT POINTER TO FIRST DEVICE.
710 002466 012700 002302 MOV #CNT.MAP,RO ;PASS COUNT POINTER TO RO
711 002472 005020 23$: CLR (RO)+ ;CLEAR TABLE
712 002474 022700 002402 CMP #CNT.MAP+100,RO ;DONE YET?
713 002500 001374 BNE 23$ ;KEEP GOING
714 002502 005037 001216 CLR SERRPC ;CLEAR LAST ERROR POINTER
715 002506 012737 000001 001202 MOV #1,STSTNM ;SET UP FOR TEST 1
716 002514 012737 002402 001206 MOV #.START,SLPADR ;SET UP FOR POWER FAIL BEFORE
717 ;TESTING STARTS
718 002522 132737 000001 001336 BITB #1,SENV ;IS IT RUNNING UNDER APT?
719 002530 001404 BEQ 3$ ;IF NOT CHECK FOR TYPE OF SWITCH REGISTER.
720 002532 013737 001340 000176 MOV #SWREG,SWREG ;LOAD SOFTWARE SWITCH REG.
721 002540 000423 BR 6$+2 ;GO SET UP SOFTWARE SWITCH REG.
722 002542 013746 000006 3$: MOV #6,-(SP) ;SAVE CURRENT VECTORS
723 002546 013746 000004 MOV #4,-(SP)
724 002552 012737 002606 000004 MOV #6$,2#4 ;SET UP FOR TIMEOUT
725 002560 012737 177570 001240 MOV #177570,SWR ;SET SWR TO HARD SWR ADDRESS
726 002566 012737 177570 001242 MOV #177570,DISPLAY ;SET DISPLAY TO HARD SWR ADDRESS
727 002574 022777 177777 176436 CMP #-1,2SWR ;REFERENCE HARDWARE SWITCH REGISTER
728 002602 001402 BEQ 6$+2 ;IF = -1 USE SOFT SWR ANYWAY
729 002604 000407 BR 7$ ;IF IT EXISTS AND NOT = -1 USE HARD SWR
730 002606 022626 6$: CMP (SP)+,(SP)+ ;ADJUST STACK
731 002610 012737 000176 001240 MOV #SWREG,SWR ;POINTER TO SOFT SWR
732 002616 012737 000174 001242 MOV #DISPREG,DISPLAY ;POINTER TO SOFT DISPLAY REG
733 002624 012637 000004 7$: MOV (SP)+,2#4 ;RESTORE VECTORS
734 002630 012637 000006 MOV (SP)+,2#6
735 002634 105737 001506 TSTB INIFLG ;HAS INITIALIZATION BEEN PERFORMED
736 002640 001006 BNE 20$ ;BR IF YES
737 002642 022737 004070 000042 CMP #SENDAD,2#42 ;IF ACT-11 AUTOMATIC MODE, DON'T TYPE ID
738 002650 001402 BEQ 20$
739 002652 104401 001000 TYPE ,MTITLE ;TYPE TITLE MESSAGE
740 002656 004737 011212 20$: JSR PC,CKSWR ;CHECK FOR SOFT SWR
741 002662 017737 176352 001446 MOV #2SWR,STRTSW ;STORE STARTING SWITCHES
742 002670 005737 000042 TST 2#42 ;IS IT RUNNING IN AUTO MODE?
743 002674 001402 BEQ +6 ;BR IF NO
744 002676 005037 001446 CLR STRTSW ;IF YES, CLEAR SWITCHES
745 002702 032737 000001 001446 BIT #SW00,STRTSW ;IF SW00=1, QUESTIONS ARE ASKED.
746 002710 001012 BNE 17$ ;BR IF SW00=1
747 002712 105737 001446 TSTB STRTSW ;BIT7=1??

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PROGRAM INITIALIZATION AND START UP.

```

748 002716 100007          BPL      17$          ;BR IF SW07=0
749 002720 005737 001470  TST      KMACTV      ;ARE ANY DEVICES SELECTED?
750 002724 001027          BNE      16$          ;BR IF YES
751 002726 104401 010731  TYPE,    NOACT        ;NO DEVICES SELECTED.
752 002732 000000          HALT                    ;STOP THE SHOW
753 002734 000776          BR       -2           ;DISQUALIFY CONTINUE SWITCH
754 002736 105737 001336  17$:    TSTB     $ENV      ;IS IT UNDER APT DUMP MODE?
755 002742 001405          BEQ      27$          ;YES, CHECK IF APT SIZED IT?
756 002744 132737 000001 001336  BITB     #1,$ENV      ;IS IT UNDER Q,V OR RUN MODE?
757 002752 001012          BNE      30$          ;YES, NEEDS ONLY APT SIZING.
758 002754 000406          BR       33$          ;NO, NEEDS REGULAR AUTO.SIZE.
759 002756 105737 001337  27$:    TSTB     $ENVM     ;IS IT SIZED BY APT?
760 002762 100406          BMI      30$          ;YES, NEEDS ONLY APT SIZING.
761 002764 042737 000001 001446  BIC      #SW00,STRTSW ;SIZE ONLY IN AUTO MODE.
762 002772 004737 012110  33$:    JSR      PC,AUTO.SIZE ;GO DO THE AUTO.SIZE.
763 002776 000402          BR       16$          ;GO PRINT THE MAP.
764 003000 004737 013510  30$:    JSR      PC,APT.SIZE  ;GO DO THE APT SIZING.
765 003004 105737 001506  16$:    TSTB     INIFLG     ;FIRST TIME?
766 003010 001410          BEQ      21$          ;BR IF YES
767 003012 105737 001446  TSTB     STRTSW      ;IF USING SAME PARAMETERS DONT TYPE MAP
768 003016 100431          BMI      1$           ;
769 003020 032737 000006 001446  BIT      #BIT1!BIT2,STRTSW ;IS TEST NO. OR LOCK SELECTED
770 003026 001403          BEQ      24$          ;IF NO THEN TYPE STATUS
771 003030 000424          BR       1$           ;IF YES DO NOT TYPE STATUS
772 003032 105137 001506  21$:    COMB     INIFLG     ;SET FLAG
773 003036 104401 010077  24$:    TYPE     ,XHEAD     ;TYPE HEADER
774 003042 012704 002100  MOV      #KM.MAP,R4    ;SET POINTER
775 003046 010437 001276  5$:    MOV      R4,$TMP0     ;SET ADDRESS
776 003052 012437 001300  MOV      (R4)+,$TMP1    ;SET CSR
777 003056 001411          BEQ      1$           ;ALL DONE IF ZERO
778 003060 012437 001302  MOV      (R4)+,$TMP2    ;SET STAT1
779 003064 012437 001304  MOV      (R4)+,$TMP3    ;SET STAT2
780 003070 012437 001306  MOV      (R4)+,$TMP4    ;SET STAT3
781 003074 104416          CONVRT                    ;TYPE OUT STATUS MAP
782 003076 011060          XSTATQ                    ;
783 003100 000762          BR       5$           ;
784 003102 012700 002100  1$:    MOV      #KM.MAP,R0  ;R0 POINTS TO STATUS TABLE
785
786 ;*****
787 ;*AUTO SIZE TEST
788 ;*THIS TEST VERIFYS THAT THE KMC11S AND/OR KMC11S ARE AT THE CORRECT FLOATING
789 ;*ADDRESSES FOR YOUR SYSTEM. IF THIS TEST FAILS, IT IS NOT A HARDWARE ERROR.
790 ;*CHECK THE ADDRESSES OF ALL FLOATING DEVICES (DJ,DH,DQ,DU,DUP,LK,DMC,DZ,KMC).
791 ;*IF THERE ARE NO OTHER FLOATING DEVICES BEFORE THE KMC11, THE FIRST
792 ;* KMC11 IS 760110. NO DEVICE SHOULD EVER BE AT
793 ;*ADDRESS 760000.
794 ;*****
795
796 003106 013746 000004          MOV      @#4,-(SP)      ;SAVE LOC 4
797 003112 013746 000006          MOV      @#6,-(SP)      ;SAVE LOC 6
798 003116 005037 000006          CLR      @#6           ;CLEAR VEC+2
799 003122 005037 001302          CLR      $TMP2        ;CLEAR FLAG
800 003126 011037 002066  AUSTRT: MOV      (R0),KMCSR ;GET NEXT KMC CSR
801 003132 001510          BEQ      AUDONE       ;BR IF DONE
802 003134 012737 003240 000004  2$:    MOV      #NODEV,@#4   ;SET UP FOR TIMEOUT
803 003142 012703 000010  3$:    MOV      #10,R3       ;R3 IS COUNT OF DEVICES BEFORE KMC

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 DZKCC.P11 21-MAR-77 17:19 PROGRAM INITIALIZATION AND START UP.

804	003146	012702	003342	4S:	MOV	#DEV TAB,R2	;R2 IS DEVICE TABLE PONTER
805	003152	012701	160010		MOV	#160010,R1	;START WITH ADDRESS 160010
806	003156	005711		FLOAT:	TST	(R1)	;CHECK ADDRESS IN R1
807	003160	111204			MOVB	(R2),R4	;IF NO TIMEOUT, GET NEXT ADDRESS
808	003162	060401			ADD	R4,R1	;IN R1
809	003164	005201			INC	R1	
810	003166	040401			BIC	R4,R1	
811	003170	005703			TST	R3	;ANY MORE DEVICES TO CHECK FOR?
812	003172	001371			BNE	FLOAT	;BR IF YES
813	003174	012737	003244 000004		MOV	#ERR,#4	;OK ONLY KMC'S ARE LEFT, SET UP FOR TIMEOUT
814	003202	005711		FY:	TST	(R1)	;CHECK KMC ADDRESS
815	003204	020137	002066		CMP	R1,KMCSR	;DOES IT MATCH
816	003210	001403			BEQ	OK	;BR IF YES
817	003212	062701	000010		ADD	#10,R1	;GET NEXT KMC ADDRESS
818	003216	000771			BR	FY	;DO IT AGAIN
819	003220	062700	000010	OK:	ADD	#10,R0	;SKIP TO NEXT KMC CSR
820	003224	062701	000010		ADD	#10,R1	;GET NEXT KMC ADDRESS
821	003230	011037	002066		MOV	(R0),KMCSR	;GET NEXT KMC CSR
822	003234	001447			BEQ	AUDONE	;BRANCH IF ALL DONE.
823	003236	000761			BR	FY	;DO IT AGAIN.
824	003240	122243		NODEV:	CMPB	(R2)+,-(R3)	;ON TIMEOUT, INC R2, DEC R3
825	003242	000002			RTI		;SLPADR
826	003244	005737	001302	ERR:	TST	\$TMP2	;CHECK FLAG IF = 0 TYPE HEADER
827	003250	001014			BNE	IS	;SKIP HEADER
828	003252	104401			TYPE		;TYPEOUT HEADER MESSAGE
829	003254	010762			CONERR		;CONFIGURATION ERROR!!!!
830	003256	012737	003244 001460		MOV	#ERR,SAVPC	;SAVE PC FOR TYPEOUT
831	003264	104417			CONVRT		;TYPE OUT ERROR PC
832	003266	003322			ERRPC		
833	003270	104401			TYPE		;TYPE REST OF HEADER
834	003272	011027			CONVRT		
835	003274	012737	177777 001302	IS:	MOV	#-1,\$TMP2	;SET FLAG SO IT ONLY GETS TYPED ONCE
836	003302	010137	001264		MOV	R1,\$REG1	;SAVE R1 FOR TYPEOUT
837	003306	104416			CONVRT		
838	003310	003330			CONTAB		;TYPE CSR VALUES
839	003312	104401		3S:	TYPE		
840	003314	011050			KMCM		
841	003316	022626		4S:	CMP	(SP)+,(SP)+	;ADJUST STACK
842	003320	000737			BR	OK	;BR TO GET OUT
843	003322	000001		ERRPC:	1		
844	003324	006	002		.BYTE	6,2	
845	003326	001460			SAVPC		
846	003330	000002		CONTAB:	2		
847	003332	006	004		.BYTE	6,4	
848	003334	001264			\$REG1		
849	003336	006	002		.BYTE	6,2	
850	003340	002066			KMCSR		
851	003342	007		DEVTAB:	.BYTE	7	;DJ
852	003343	017			.BYTE	17	;DH
853	003344	007			.BYTE	7	;DQ
854	003345	007			.BYTE	7	;DU
855	003346	007			.BYTE	7	;DUP
856	003347	007			.BYTE	7	;LK
857	003350	007			.BYTE	7	;DMC
858	003351	007			.BYTE	7	;DZ
859	003352	007			.BYTE	7	;KMC

Line	Address	Code	Label	Op	Opnd	Comment
860	003354	003354				
861	003354		EVEN			
862	003354	012637	000006	1\$:	MOV (SP)+,2#6	:RESTORE LOC 6
863	003360	012637	000004		MOV (SP)+,2#4	:RESTORE LOC 4
864	003364	032737	000010	001446	BIT #SW03,STRTSW	:SELECT SPECIFIC DEVICES??
865	003372	001422			BEQ 3\$:BR IF NO.
866	003374	104401	010017		TYPE MNEW	:TYPE THE MESSAGE.
867	003400	005000			CLR RO	:ZERO DATA LIGHTS
868	003402	000000			HALT	:WAIT FOR USER TO TELL WHAT DEVICES TO RUN
869	003404	027737	175630	001474	CMP 2SWR,SAVACT	:IS THE NUMBER VALID?
870	003412	101404			BLOS 2\$:BR IF NUMBER IS OK.
871	003414	104401	007672		TYPE ,MERR3	:TELL USER OF INVALID NUMBER.
872	003420	000000			HALT	:STOP EVERY THING.
873	003422	000776			BR -2	:RESTART THE PROGRAM AGAIN.
874	003424	017737	175610	001470	2\$:	MOV 2SWR,KMACTV
875	003432	013700	001470		MOV KMACTV,RO	:GET NEW DEVICE PATTERN
876	003436	000000			HALT	:SHOW THE USER WHAT HE SELECTED.
877	003440	012700	000300	3\$:	MOV #300,RO	:CONTINUE DYNAMIC SWITCHES.
878	003444	012701	000302		MOV #302,R1	:PREPARE TO CLEAR THE FLOATING
879	003450	010120		4\$:	MOV R1,(R0)+	:VECTOR AREA. 300-776
880	003452	005021			CLR (R1)+	:START PUTTING "PC+2 - HALT"
881	003454	022021			CMP (RO)+,(R1)+	:IN VECTOR AREA.
882	003456	022700	001000		CMP #1000,RO	:POP POINTERS
883	003462	001372			BNE 4\$:ALL DONE??
884						:BR IF NO.
885						
886						
887						
888	003464	012706	001200		.BEGIN: MOV #STACK,SP	:SET UP STACK
889	003470	013746	000006		MOV 2#6,-(SP)	:SAVE LOC 6
890	003474	013746	000004		MOV 2#4,-(SP)	:SAVE LOC 4
891	003500	005000			CLR RO	:START AT 0
892	003502	012737	003546	000004	MOV 2\$,2#4	:SET UP FOR TIME OUT
893	003510	005037	000006		CLR 2#6	:TO AUTOSIZE MEMORY
894	003514	005720		6\$:	TST (RO)+	:CHECK ADDRESS IN RO
895	003516	022700	157776		CMP #157776,RO	:IS IT AT LEAST 28K
896	003522	001374			BNE 6\$:BR IF NO
897	003524	162700	007776		SUB #7776,RO	:SAVE 2K FOR MONITORS
898	003530	010037	001466	7\$:	MOV RO,MEMLIM	:STORE MEMORY LIMIT
899	003534	012637	000004		MOV (SP)+,2#4	:RESTORE LOC 4
900	003540	012637	000006		MOV (SP)+,2#6	:RESTORE LOC 6
901	003544	000413			BR 10\$:CONTINUE
902	003546	022626		2\$:	CMP (SP)+,(SP)+	:ADJUST STACK
903	003550	162700	000004		SUB #4,RO	:GET LAST GOOD ADDRESS
904	003554	162700	007776		SUB #7776,RO	:SAVE 2K FOR MONITORS
905	003560	022700	030000		CMP #30000,RO	:IS IT 8K?
906	003564	001361			BNE 7\$:BR IF NO
907	003566	012700	037400		MOV #37400,RO	:IF 8K DON'T SAVE 2K
908	003572	000756			BR 7\$	
909	003574	012737	000340	177776	10\$:	MOV #340,PS
910	003602	032737	000004	001446	BIT #BIT2,STRTSW	:LOCK OUT INTERRUPTS
911	003610	001406			BEQ 1\$:CHECK FOR LOCK ON TEST
912	003612	104401	007716		TYPE ,MLOCK	:BR IF NO LOCK DESIRED.
913	003616	012737	000240	004146	MOV #NOP,TTST	:TYPE LOCK SELECTED.
914	003624	000403			BR 3\$:SET UP TO LOCK
915	003626	013737	004360	004146	1\$:	MOV BRW,TTST

:TEST START AND RESTART

.BEGIN: MOV #STACK,SP

:SET UP STACK
:SAVE LOC 6
:SAVE LOC 4
:START AT 0
:SET UP FOR TIME OUT
:TO AUTOSIZE MEMORY
:CHECK ADDRESS IN RO
:IS IT AT LEAST 28K
:BR IF NO
:SAVE 2K FOR MONITORS
:STORE MEMORY LIMIT
:RESTORE LOC 4
:RESTORE LOC 6
:CONTINUE
:ADJUST STACK
:GET LAST GOOD ADDRESS
:SAVE 2K FOR MONITORS
:IS IT 8K?
:BR IF NO
:IF 8K DON'T SAVE 2K
:LOCK OUT INTERRUPTS
:CHECK FOR LOCK ON TEST
:BR IF NO LOCK DESIRED.
:TYPE LOCK SELECTED.
:SET UP TO LOCK
:CONTINUE ALONG.
:PREPARE NORMAL SCOPE ROUTINE

H04

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PROGRAM INITIALIZATION AND START UP.

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916	003634	012737	011460	001206	3\$:	MOV	#CYCLE,\$LPADR	; START AT "CYCLE" FIND WHICH DEVICE TO TEST
917	003642	032737	000002	001446	4\$:	BIT	#SW01,\$RTSW	; IS TEST NO. SELECTED?
918	003650	001002				BNE	\$S	; BR IF YES
919	003652	104401	007642			TYPE	MR	; TYPE R
920	003656	000177	175324		5\$:	JMP	\$LPADR	; START TESTING

```

921 ;END OF PASS
922 ;TYPE NAME OF TEST
923 ;UPDATE PASS COUNT
924 ;CHECK FOR EXIT TO ACT-11
925 ;RESTART TEST
926
927
928
929
930
931
932
933

```

.SBTTL END OF PASS ROUTINE

```

;*****
;INCREMENT THE PASS NUMBER ($PASS)
;IF THERES A MONITOR GO TO IT
;IF THERE ISN'T JUMP TO CYCLE

```

SEOP:

934	003662				RESET			
935	003662	000005			INC	\$PASS		INCREMENT THE PASS COUNT
936	003664	005237	001324		CLRB	\$ERFLG		CLEAR ERROR FLAG
937	003670	105037	001203		TYPE	,MEPASS		TYPE END PASS.
938	003674	104401	007620		TYPE	,MCSR		TYPE "CSR"
939	003700	104401	007745		CONVRT	,XCSR		SHOW IT.
940	003704	104417	004104		TYPE	,MVECX		TYPE VECTOR.
941	003710	104401	007753		CONVRT	,XVEC		SHOW IT.
942	003714	104417	004112		TYPE	,MPASSX		TYPE "PASSES"
943	003720	104401	007761		CONVRT	,XPASS		SHOW IT.
944	003724	104417	004120		TYPE	,MERRX		TYPE "ERRORS"
945	003730	104401	007772		CONVRT	,XERR		SHOW IT.
946	003734	104417	004126		MOV	\$MILK,RO		SET POINTER TO PASSCNT.
947	003740	013700	001504		MOV	\$PASS,(RO)+		SAVE THE PASS COUNT.
948	003744	013720	001324		MOV	\$ERTTL,(RO)+		SAVE ERROR COUNT
949	003750	013720	001212		MOV	\$MRLVL,\$KMRVEC		RESTORE THE RECEIVER INTERRUPT VECTOR.
950	003754	013777	002060	176074	CLR	\$KMLVL		RESTORE RECEIVER LEVEL
951	003762	005077	176072		MOV	\$KMTLVL,\$KMTVEC		RESTORE THE TRANSMIT INTERRUPT VECTOR.
952	003766	013777	002064	176066	CLR	\$KMTLVL		RESTORE TRANSMITTER LEVEL
953	003774	005077	176064		DEC	\$AVNUM		ALL DEVICE TESTED?
954	004000	005337	001476		BNE	\$DOAGN		BRANCH IF NO.
955	004004	001035			MOVB	\$377,\$QV,FLG		SET QUICK VERIFY FLAG.
956	004006	112737	000377	001511	MOV	\$MNUM,\$AVNUM		RESTORE DEVICE COUNT.
957	004014	013737	001472	001476	CLR	\$ERRPC		CLEAR LAST ERROR PC
958	004022	005037	001215		CLR	\$TIMES		ZERO THE NUMBER OF ITERATIONS
959	004026	005037	001310		INC	\$PASS		INCREMENT THE PASS NUMBER
960	004032	005237	001324		BIC	\$100000,\$PASS		DON'T ALLOW A NEG. NUMBER
961	004036	042737	100000	001324	DEC	(PC)+		LOOP?
962	004044	005327			SEOPCT:	.WORD	1	
963	004046	000001			BGT	\$DOAGN		::YES
964	004050	003013			MOV	(PC)+,\$(PC)+		::RESTORE COUNTER
965	004052	012737			SENDCT:	.WORD	1	
966	004054	000001			SEOPCT			
967	004056	004046			SGET42:	MOV	\$42,RO	::GET MONITOR ADDRESS
968	004060	013700	000042		BEQ	\$DOAGN		::BRANCH IF NO MONITOR
969	004064	001405			RESET			::CLEAR THE WORLD
970	004066	000005			SENDAD:	JSR	PC,(RO)	::GO TO MONITOR
971	004070	004710			NOP			::SAVE ROOM
972	004072	000240			NOP			::FOR
973	004074	000240			NOP			::ACT11
974	004076	000240			SDOAGN:			
975	004100				JMP	\$(PC)+		::RETURN
976	004100	000137						

END OF PASS ROUTINE

977	004102	011460	
978	004104	000001	
979	004106	006	002
980	004110	002066	
981	004112	000001	
982	004114	004	002
983	004116	002056	
984	004120	000001	
985	004122	006	002
986	004124	001324	
987	004126	000001	
988	004130	006	002
989	004132	001212	

```

SRTNAD: .WORD   CYCLE
XCSR:   1
        .BYTE   6,2
        KMCSR
XVEC:   1
        .BYTE   4,2
        KMRVEC
XPASS:  1
        .BYTE   6,2
        $PASS
XERR:   1
        .BYTE   6,2
        $ERTTL

```

;SCOPE LOOP AND INTERATION HANDLER

.SBTTL SCOPE HANDLER ROUTINE

```

*****
;THIS ROUTINE CONTROLS THE LOOPING OF SUBTESTS. IT WILL INCREMENT
;AND LOAD THE TEST NUMBER($TSTNM) INTO THE DISPLAY REG.(DISPLAY<7:0>)
;AND LOAD THE ERROR FLAG ($ERFLG) INTO DISPLAY<15:08>
;THE SWITCH OPTIONS PROVIDED BY THIS ROUTINE ARE:
;SW14=1      LOOP ON TEST
;SW11=1      INHIBIT ITERATIONS
;CALL
;*          SCOPE          ;;SCOPE=IOT

$SCOPE:
        CLR          $ERRPC          ; CLEAR LAST ERROR PC
        CMP          TST1+2,(SP)     ; IS THIS TEST #1 ?
        BEQ          $XTSTR          ; IF SO DON'T LOOP.
TTST:   BR          1$
        TSTB        $STKS           ; KEYBOARD DONE ?
        BPL          $OVER           ; IF NO DONT WAIT.
1$:     MOV          $STKB,-2(SP)
        BIT          $BIT14,$SWR     ; LOOP ON PRESENT TEST?
        BNE          $OVER           ; YES IF SW14=1
;*****START OF CODE FOR THE XOR TESTER*****
$XTSTR: BR          6$
        MOV          $ERRVEC,-(SP)   ; IF RUNNING ON THE "XOR" TESTER CHANGE
        MOV          $5,$ERRVEC     ; THIS INSTRUCTION TO A "NOP" (NOP=240)
        TST         $177060        ; SAVE THE CONTENTS OF THE ERROR VECTOR
        MOV          (SP)+,$ERRVEC  ; SET FOR TIMEOUT
        BR          $5VLAD         ; TIME OUT ON XOR?
5$:     CMP          (SP)+,(SP)+     ; RESTORE THE ERROR VECTOR
        MOV          (SP)+,$ERRVEC  ; GO TO THE NEXT TEST
        BR          $OVER          ; CLEAR THE STACK AFTER A TIME OUT
6$:     ;*****END OF CODE FOR THE XOR TESTER*****
        TSTB        $ERFLG         ; HAS AN ERROR OCCURRED?
        BEQ          3$            ; BR IF NO
4$:     CLRB        $ERFLG         ; ZERO THE ERROR FLAG
1031:  CLB          $TIMES         ; CLEAR THE NUMBER OF ITERATIONS TO MAKE
1032:  BIT          $BIT11,$SWR     ; INHIBIT ITERATIONS?

```

SCOPE HANDLER ROUTINE

```

1033 004256 001011 BNE 1$ ;:BR IF YES
1034 004260 005737 001324 TST $PASS ;:IF FIRST PASS OF PROGRAM
1035 004264 001406 BEQ 1$ ;:INHIBIT ITERATIONS
1036 004266 005237 001204 INC $ICNT ;:INCREMENT ITERATION COUNT
1037 004272 023737 001310 001204 CMP $TIMES,$ICNT ;:CHECK THE NUMBER OF ITERATIONS MADE
1038 004300 002015 BGE $OVER ;:BR IF MORE ITERATION REQUIRED
1039 004302 012737 000001 001204 1$: MOV #1,$ICNT ;:REINITIALIZE THE ITERATION COUNTER
1040 004310 013737 004362 001310 MOV $SMXCNT,$TIMES ;:SET NUMBER OF ITERATIONS TO DO
1041 004316 105237 001202 $SVLAD: INCB $STSTNM ;:COUNT TEST NUMBERS
1042 004322 113737 001202 001322 MOV $STSTNM,$STSTNM ;:SET TEST NUMBER IN APT MAILBOX
1043 004330 011637 001206 MOV (SP),$LPADR ;:SAVE SCOPE LOOP ADDRESS
1044 004334 013777 001202 174700 $OVER: MOV $STSTNM,$DISPLAY ;:DISPLAY TEST NUMBER
1045 004342 013716 001206 MOV $LPADR,(SP) ;:FUDGE RETURN ADDRESS
1046 004346 005037 001444 CLR LOCK ;:RESET LOCK ON DATA.
1047 004352 013701 002066 MOV $KMC SR,R1 ;:R1 CONTAINS BASE KMC ADDRESS.
1048 004356 000002 RTI
1049 004360 000406 BRW: WORD 406
1050 004362 000020 $SMXCNT: 20 ;:MAX. NUMBER OF ITERATIONS
1051
1052 ;:CHECK FOR FREEZE ON CURRENT DATA
1053 ;-----
1054
1055 004364 004737 011212 .SCOP1: JSR PC,$CKSWR ;:CHECK FOR SOFT SWR
1056 004370 032777 001000 174642 BIT #SW09,$SWR ;:IS SW09=1(SET)?
1057 004376 001405 BEQ 1$ ;:BR IF NOT SET.
1058 004400 005737 001444 TST LOCK
1059 004404 001402 BEQ 1$
1060 004406 013716 001444 1$: MOV LOCK,(SP) ;:GOTO THE ADDRESS IN LOCK.
1061 004412 000002 RTI ;:GO BACK.
1062
1063 ;:TELETYPE OUTPUT ROUTINE
1064 ;-----
1065
1066 .SBTTL TYPE ROUTINE
1067
1068 ;:*****
1069 ;:ROUTINE TO TYPE ASCIZ MESSAGE. MESSAGE MUST TERMINATE WITH A 0 BYTE.
1070 ;:THE ROUTINE WILL INSERT A NUMBER OF NULL CHARACTERS AFTER A LINE FEED.
1071 ;:NOTE1: $NULL CONTAINS THE CHARACTER TO BE USED AS THE FILLER CHARACTER.
1072 ;:NOTE2: $FILLS CONTAINS THE NUMBER OF FILLER CHARACTERS REQUIRED.
1073 ;:NOTE3: $FILLC CONTAINS THE CHARACTER TO FILL AFTER.
1074 ;:
1075 ;:CALL:
1076 ;:1) USING A TRAP INSTRUCTION
1077 ;: TYPE ,MESADR ;:MESADR IS FIRST ADDRESS OF AN ASCIZ STRING
1078 ;:OR
1079 ;: TYPE
1080 ;: MESADR
1081 ;:
1082
1083 004414 105737 001257 $TYPE: TSTB $TFPLG ;:IS THERE A TERMINAL?
1084 004420 100002 BPL 1$ ;:BR IF YES
1085 004422 000000 HALT ;:HALT HERE IF NO TERMINAL
1086 004424 000430 BR 3$ ;:LEAVE
1087 004426 010046 1$: MOV R0,-(SP) ;:SAVE R0
1088 004430 017600 000002 MOV #2(SP),R0 ;:GET ADDRESS OF ASCIZ STRING

```


APT COMMUNICATIONS ROUTINE

.SBTTL APT COMMUNICATIONS ROUTINE

```

1145
1146
1147
1148 004676 112737 000001 005142 $ATY1: MOVB #1,SFFLG ;; TO REPORT FATAL ERROR
1149 004704 112737 000001 005140 $ATY3: MOVB #1,SMFLG ;; TO TYPE A MESSAGE
1150 004712 000403
1151 004714 112737 000001 005142 $ATY4: MOVB #1,SFFLG ;; TO ONLY REPORT FATAL ERROR
1152 004722 $ATYC:
1153 004722 010046 MOV R0,-(SP) ;; PUSH R0 ON STACK
1154 004724 010146 MOV R1,-(SP) ;; PUSH R1 ON STACK
1155 004726 105737 005140 TSTB SMFLG ;; SHOULD TYPE A MESSAGE?
1156 004732 001450 BEQ 5S ;; IF NOT: BR
1157 004734 122737 000001 001336 CMPB #APTENV,SENV ;; OPERATING UNDER APT?
1158 004742 001031 BNE 3S ;; IF NOT: BR
1159 004744 132737 000100 001337 BITB #APTPOOL,SENVM ;; SHOULD SPOOL MESSAGES?
1160 004752 001425 BEQ 3S ;; IF NOT: BR
1161 004754 017600 000004 MOV #4(SP),R0 ;; GET MESSAGE ADDR.
1162 004760 062766 000002 000004 ADD #2,4(SP) ;; BUMP RETURN ADDR.
1163 004766 005737 001316 1S: TST $MSGTYPE ;; SEE IF DONE W/ LAST XMISSION?
1164 004772 001375 BNE 1S ;; IF NOT: WAIT
1165 004774 010037 001332 MOV R0,$MSGAD ;; PUT ADDR IN MAILBOX
1166 005000 105720 2S: TSTB (R0)+ ;; FIND END OF MESSAGE
1167 005002 001376 BNE 2S
1168 005004 163700 001332 SUB $MSGAD,R0 ;; SUB START OF MESSAGE
1169 005010 006200 ASR R0 ;; GET MESSAGE LNTH IN WORDS
1170 005012 010037 001334 MOV R0,$MSGLGT ;; PUT LENGTH IN MAILBOX
1171 005016 012737 000004 001316 MOV #4,$MSGTYPE ;; TELL APT TO TAKE MSG.
1172 005024 000413 BR 5S
1173 005026 017637 000004 005052 3S: MOV #4(SP),4S ;; PUT MSG ADDR IN JSR LINKAGE
1174 005034 062766 000002 000004 ADD #2,4(SP) ;; BUMP RETURN ADDRESS
1175 005042 013746 177776 MOV 177776,-(SP) ;; PUSH 177776 ON STACK
1176 005046 004737 004414 JSR PC,$TYPE ;; CALL TYPE MACRO
1177 005052 000000 4S: .WORD 0
1178 005054 5S:
1179 005054 105737 005142 10S: TSTB $FFLG ;; SHOULD REPORT FATAL ERROR?
1180 005060 001416 BEQ 12S ;; IF NOT: BR
1181 005062 005737 001336 TST SENV ;; RUNNING UNDER APT?
1182 005066 001413 BEQ 12S ;; IF NOT: BR
1183 005070 005737 001316 11S: TST $MSGTYPE ;; FINISHED LAST MESSAGE?
1184 005074 001375 BNE 11S ;; IF NOT: WAIT
1185 005076 017637 000004 001320 MOV #4(SP),$FATAL ;; GET ERROR #
1186 005104 062766 000002 000004 ADD #2,4(SP) ;; BUMP RETURN ADDR.
1187 005112 005237 001316 INC $MSGTYPE ;; TELL APT TO TAKE ERROR
1188 005116 105037 005142 12S: CLRB $FFLG ;; CLEAR FATAL FLAG
1189 005122 105037 005141 CLRB $LFLG ;; CLEAR LOG FLAG
1190 005126 105037 005140 CLRB $MFLG ;; CLEAR MESSAGE FLAG
1191 005132 012601 MOV (SP)+,R1 ;; POP STACK INTO R1
1192 005134 012600 MOV (SP)+,R0 ;; POP STACK INTO R0
1193 005136 000207 RTS PC ;; RETURN
1194 005140 000 $MFLG: .BYTE 0 ;; MESSG. FLAG
1195 005141 000 $LFLG: .BYTE 0 ;; LOG FLAG
1196 005142 000 $FFLG: .BYTE 0 ;; FATAL FLAG
1197 005144 .EVEN
1198 000200 APTSIZE=200
1199 000001 APTENV=001
1200 000100 APTPOOL=100

```

APTCSUP=040

.SBTTL TTY INPUT ROUTINE

.ENABL LSB

.DSABL LSB

THIS ROUTINE WILL INPUT A SINGLE CHARACTER FROM THE TTY

*CALL:

* RDCHR ;: INPUT A SINGLE CHARACTER FROM THE TTY
* RETURN HERE ;: CHARACTER IS ON THE STACK
* ;: WITH PARITY BIT STRIPPED OFF

1201 000040
1202
1203
1204
1205
1206
1207
1208
1209
1210
1211
1212
1213
1214
1215
1216
1217
1218
1219
1220 005144 011646
1221 005146 016666 000004 000002
1222 005154 105777 174064
1223 005160 100375
1224 005162 117766 174060 000004
1225 005170 042766 177600 000004
1226 005176 026627 000004 000023
1227 005204 001013
1228 005206 105777 174032 2\$:
1229 005212 100375
1230 005214 117746 174026
1231 005220 042716 177600
1232 005224 022627 000021
1233 005230 001366
1234 005232 000750
1235 005234 026627 000004 000140 3\$:
1236 005242 002407
1237 005244 026627 000004 000175
1238 005252 003003
1239 005254 042766 000040 000004 4\$:
1240 005262 000002

SRDCHR: MOV (SP), -(SP) ;: PUSH DOWN THE PC
MOV 4(SP), 2(SP) ;: SAVE THE PS
1\$: TSTB 2\$TKS ;: WAIT FOR
BPL 1\$;: A CHARACTER
MOVB 2\$TKB, 4(SP) ;: READ THE TTY
BIC #177, 4(SP) ;: GET RID OF JUNK IF ANY
CMP 4(SP), #23 ;: IS IT A CONTROL-S?
BNE 3\$;: BRANCH IF NO
2\$: TSTB 2\$TKS ;: WAIT FOR A CHARACTER
BPL 2\$;: LOOP UNTIL ITS THERE
MOVB 2\$TKB, -(SP) ;: GET CHARACTER
BIC #177, (SP) ;: MAKE IT 7-BIT ASCII
CMP (SP)+, #21 ;: IS IT A CONTROL-Q?
BNE 2\$;: IF NOT DISCARD IT
BR 1\$;: YES, RESUME
3\$: CMP 4(SP), #140 ;: IS IT UPPER CASE?
BLT 4\$;: BRANCH IF YES
CMP 4(SP), #175 ;: IS IT A SPECIAL CHAR?
BGT 4\$;: BRANCH IF YES
BIC #40, 4(SP) ;: MAKE IT UPPER CASE
4\$: RTI ;: GO BACK TO USER

THIS ROUTINE WILL INPUT A STRING FROM THE TTY

*CALL:

* RDLIN ;: INPUT A STRING FROM THE TTY
* RETURN HERE ;: ADDRESS OF FIRST CHARACTER WILL BE ON THE STACK
* ;: TERMINATOR WILL BE A BYTE OF ALL 0'S

1241
1242
1243
1244
1245
1246
1247
1248 005264 010346
1249 005266 005046
1250 005270 012703 005520
1251 005274 022703 005527
1252 005300 101456
1253 005302 104402
1254 005304 112613
1255 005306 122713 000177
1256 005312 001022

SRDLIN: MOV R3, -(SP) ;: SAVE R3
CLR -(SP) ;: CLEAR THE RUBOUT KEY
1\$: MOV #STTYIN, R3 ;: GET ADDRESS
2\$: CMP #STTYIN+7, R3 ;: BUFFER FULL?
BLOS 4\$;: BR IF YES
RDCHR ;: GO READ ONE CHARACTER FROM THE TTY
MOVB (SP)+, (R3) ;: GET CHARACTER
10\$: CMPB #177, (R3) ;: IS IT A RUBOUT
BNE 5\$;: BR IF NO

```

1257 005314 005716          TST      (SP)          ;; IS THIS THE FIRST RUBOUT?
1258 005316 001007          BNE      6$           ;; BR IF NO
1259 005320 112737 000134 005516  MOVB     #' \, 9$     ;; TYPE A BACK SLASH
1260 005326 104401 005516          TYPE     9$
1261 005332 012716 177777          MOV      4-1, (SP)    ;; SET THE RUBOUT KEY
1262 005336 005303          6$: DEC      R3         ;; BACKUP BY ONE
1263 005340 020327 005520          CMP      R3, #STTYIN ;; STACK EMPTY?
1264 005344 103434          BLO      4$           ;; BR IF YES
1265 005346 111337 005516          MOVB     (R3), 9$     ;; SETUP TO TYPEOUT THE DELETED CHAR.
1266 005352 104401 005516          TYPE     9$         ;; GO TYPE
1267 005356 000746          BR       2$           ;; GO READ ANOTHER CHAR.
1268 005360 005716          5$: TST      (SP)        ;; RUBOUT KEY SET?
1269 005362 001406          BEQ      7$           ;; BR IF NO
1270 005364 112737 000134 005516  MOVB     #' \, 9$     ;; TYPE A BACK SLASH
1271 005372 104401 005516          TYPE     9$
1272 005376 005016          CLR      (SP)        ;; CLEAR THE RUBOUT KEY
1273 005400 122713 000025 7$: CMPB     #25, (R3)   ;; IS CHARACTER A CTRL U?
1274 005404 001003          BNE      8$           ;; BR IF NO
1275 005406 104401 005527          TYPE     $CNTLU      ;; TYPE A CONTROL "U"
1276 005412 000726          BR       1$           ;; GO START OVER
1277 005414 122713 000022 8$: CMPB     #22, (R3)   ;; IS CHARACTER A "r"?
1278 005420 001011          BNE      3$           ;; BRANCH IF NO
1279 005422 105013          CLRB     (R3)        ;; CLEAR THE CHARACTER
1280 005424 104401 001313          TYPE     $CRLF       ;; TYPE A "CR" & "LF"
1281 005430 104401 005520          TYPE     $TTYIN      ;; TYPE THE INPUT STRING
1282 005434 000717          BR       2$           ;; GO PICKUP ANOTHER CHARACTER
1283 005436 104401 001312 4$: TYPE     $QUES      ;; TYPE A '?'
1284 005442 000712          BR       1$           ;; CLEAR THE BUFFER AND LOOP
1285 005444 111337 005516 3$: MOVB     (R3), 9$     ;; ECHO THE CHARACTER
1286 005450 104401 005516          TYPE     9$
1287 005454 122723 000015          CMPB     #15, (R3)+  ;; CHECK FOR RETURN
1288 005460 001305          BNE      2$           ;; LOOP IF NOT RETURN
1289 005462 105063 177777          CLRB     -1(R3)     ;; CLEAR RETURN (THE 15)
1290 005466 104401 001314          TYPE     $LF         ;; TYPE A LINE FEED
1291 005472 005726          TST     (SP)+        ;; CLEAN RUBOUT KEY FROM THE STACK
1292 005474 012603          MOV      (SP)+, R3   ;; RESTORE R3
1293 005476 011646          MOV      (SP), -(SP) ;; ADJUST THE STACK AND PUT ADDRESS OF THE
1294 005500 016666 000004 000002  MOV      4(SP), 2(SP) ;; FIRST ASCII CHARACTER ON IT
1295 005506 012766 005520 000004  MOV      #STTYIN, 4(SP)
1296 005514 000002          RTI
1297 005516          000          9$: .BYTE    0          ;; RETURN
1298 005517          000          ;; STORAGE FOR ASCII CHAR. TO TYPE
1299 005520 000007          $TTYIN: .BLKB    7   ;; TERMINATOR
1300 005527          136 006525 000012 $CNTLU:  .ASCIZ  /?U/<15><12> ;; RESERVE 7 BYTES FOR TTY INPUT
1301 005534 043536 005015          000 $CNTLG:  .ASCIZ  /?G/<15><12> ;; CONTROL "U"
1302 005541          015 051412 051127 $MSWR:   .ASCIZ  <15><12>/SWR = / ;; CONTROL "G"
1303 005546 036440 000040          000
1304 005552 020040 042516 020127 $MNEW:   .ASCIZ  / NEW = /
1305 005560 020075          000
1306          005564
1307          .EVEN
1308          .SBTTL READ AN OCTAL NUMBER FROM THE TTY
1309
1310          ;; *****
1311          ;; *THIS ROUTINE WILL READ AN OCTAL (ASCII) NUMBER FROM THE TTY AND
1312          ;; *CHANGE IT TO BINARY.
          ;; *THE INPUT CHARACTERS WILL BE CHECKED TO INSURED THEY ARE LEGAL

```

READ AN OCTAL NUMBER FROM THE TTY

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1313 ;*OCTAL DIGITS. IF AN ILLEGAL CHARACTER IS READ A "?" WILL BE TYPED
1314 ;*FOLLOWED BY A CARRIAGE RETURN-LINE FEED. THE COMPLETE NUMBER MUST
1315 ;*THEN BE RETYPED. THE INPUT IS TERMINATED BY TYPING A CARRIAGE RETURN.
1316 ;*CALL:
1317 ;*      RDOCT          ;: READ AN OCTAL NUMBER
1318 ;*      RETURN HERE   ;: LOW ORDER BITS ARE ON TOP OF THE STACK
1319 ;*                   ;: HIGH ORDER BITS ARE IN SHIOCT
1320
1321 005564 011646          $RDOCT: MOV      (SP),-(SP)      ;: PROVIDE SPACE FOR THE
1322 005566 016666 000004 000002 MOV      4(SP),2(SP)    ;: INPUT NUMBER
1323 005574 010046          MOV      RO,-(SP)      ;: PUSH RO ON STACK
1324 005576 010146          MOV      R1,-(SP)      ;: PUSH R1 ON STACK
1325 005600 010246          MOV      R2,-(SP)      ;: PUSH R2 ON STACK
1326 005602 104403          1$:  RDLIN      ;: READ AN ASCII LINE
1327 005604 012600          MOV      (SP)+,RO      ;: GET ADDRESS OF 1ST CHARACTER
1328 005606 010037 005712 MOV      RO,5$        ;: AND SAVE IT
1329 005612 005001          CLR      R1          ;: CLEAR DATA WORD
1330 005614 005002          CLR      R2
1331 005616 112046          2$:  MOV8B   (RO)+,-(SP)    ;: PICKUP THIS CHARACTER
1332 005620 001420          BEQ      3$          ;: IF ZERO GET OUT
1333 005622 122716 000060 CMP8B   #'0,(SP)      ;: MAKE SURE THIS CHARACTER
1334 005626 003026          BGT      4$          ;: IS AN OCTAL DIGIT
1335 005630 122716 000067 CMP8B   #'7,(SP)
1336 005634 002423          BLT      4$
1337 005636 006301          ASL      R1          ;: *2
1338 005640 006102          ROL      R2
1339 005642 006301          ASL      R1          ;: *4
1340 005644 006102          ROL      R2
1341 005646 006301          ASL      R1          ;: *8
1342 005650 006102          ROL      R2
1343 005652 042716 177770 BIC      #'C7,(SP)    ;: STRIP THE ASCII JUNK
1344 005656 062601          ADD      (SP)+,R1    ;: ADD IN THIS DIGIT
1345 005660 000756          BR       2$          ;: LOOP
1346 005662 005726          3$:  TST      (SP)+      ;: CLEAN TERMINATOR FROM STACK
1347 005664 010166 000012 MOV      R1,12(SP)    ;: SAVE THE RESULT
1348 005670 010237 005722 MOV      R2,SHIOCT
1349 005674 012602          MOV      (SP)+,R2    ;: POP STACK INTO R2
1350 005676 012601          MOV      (SP)+,R1    ;: POP STACK INTO R1
1351 005700 012600          MOV      (SP)+,RO    ;: POP STACK INTO RO
1352 005702 000002          RTI          ;: RETURN
1353 005704 005726          4$:  TST      (SP)+      ;: CLEAN PARTIAL FROM STACK
1354 005706 105010          CLRB    (RO)        ;: SET A TERMINATOR
1355 005710 104401          TYPE    ;: TYPE UP THRU THE BAD CHAR.
1356 005712 000000          5$:  .WORD   0          ;: "?" "CR" & "LF"
1357 005714 104401 001312 TYPE    $QUES        ;: TRY AGAIN
1358 005720 000730          BR       1$          ;: HIGH ORDER BITS GO HERE
1359 005722 000000          SHIOCT: .WORD 0
1360
1361 ;-----
1362 ; INPUT OCTAL NUMBER ROUTINE
1363 ;-----
1364 005724 010546          $INPUT: MOV      R5,-(SP) ;: SAVE REGISTER R5.
1365 005726 016605 000002 MOV      2(SP),R5    ;: GET FIRST PARAMETER ADDRESS.
1366 005732 012537 005770 MOV      (R5)+,WHAT  ;: GET MESSAGE ADDRESS.
1367 005736 012537 006050 MOV      (R5)+,LOLIM ;: GET LOW LIMIT FOR THE #
1368 005742 012537 006052 MOV      (R5)+,HILIM ;: GET HIGH LIMIT FOR THE #.
    
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1369 005746 012537 006054      MOV      (R5)+,WHERE      ; GET ADDRESS OF INBUFFER.
1370 005752 112537 006056      MOVB    (R5)+,LOBITS     ; GET LOWMASK BITS.
1371 005756 112537 006057      MOVB    (R5)+,ADRCNT     ; GET # OF #'S TO BE GENERATED.
1372 005762 010566 000002      MOV      R5,2(SP)        ; SAVE THE RETURN ADDRESS.
1373 005766 104401                INLP1:  TYPE              ; TYPE THE MESSAGE.
1374 005770 000000                WHAT:   .WORD            0
1375 005772 104404                RDOCT   .WORD            0
1376 005774 021637 006052      CMP      (SP),HILIM      ; READ OCTAL # FROM KEYBOARD.
1377 006000 003003                BGT     2$               ; IS IT IN HIGH LIMIT?
1378 006002 021637 006050      CMP      (SP),LOLIM      ; BRANCH IF NO.
1379 006006 002005                BGE     3$               ; IS IT MORE THAN LOW LIMIT.
1380 006010 104401 001312      2$:     TYPE              ; BRANCH IF YES.
1381 006014 104401 001313                .SQUES
1382 006020 000762                TYPE   ' ? '
1383 006022 013705 006054      3$:     TYPE              ; TYPE <CR>,<LF>
1384 006026 011625                .SCRLF
1385 006030 062716 000002      4$:     BR      INLP1
1386 006034 105337 006057      MOV      WHERE,R5        ; GET BUFFER ADDRESS.
1387 006040 001372                MOV     (SP),(R5)+       ; SAVE THE # IN RIGHT PLACE.
1388 006042 005726                ADD     #2,(SP)          ; NEXT SEQUENTIAL NUMBER.
1389 006044 012605                DECB   ADRCNT           ; COUNT BY 1.
1390 006046 000002                BNE    4$               ; BRANCH IF NOT DONE.
1391 006050 000000                TST    (SP)+            ; POP THE STACK POINTER.
1392 006052 000000                MOV     (SP)+,R5        ; POP THE REG.5
1393 006054 000000                RTI
1394 006056      000                LOLIM:  .WORD            0
1395 006057      000                HILIM:  .WORD            0
1396                WHERE:  .WORD            0
1397                LOBITS: .BYTE            0
1398                ADRCNT: .BYTE            0
1399                ; ADVANCE TO NEXT TEST HANDLER
1400 006060 013716 001442      .ADVANCE: MOV     NEXT,(SP) ; CRUNCH STACK WITH ADDRESS OF SCOPE CALL
1401 006064 005037 001444                CLR     LOCK            ; RESET TIGHT LOOP ADDRESS
1402 006070 000002                RTI                    ; CHECK TO SEE IF OLD TEST GETS REPEATED
1403                ; SAVE PC OF TEST THAT FAILED AND RO-R5
1404                ;-----
1405                ;
1406                ;
1407 006072 016637 000004 001460 .SAVOS: MOV     4(SP),SAVPC ; SAVE R7 (PC)
1408                ;
1409                ; SAVE RO-R5
1410                ;
1411 006100 010537 001274      SVOS:   MOV     R5,$REG5  ; SAVE R5
1412 006104 010437 001272                MOV     R4,$REG4        ; SAVE R4
1413 006110 010337 001270                MOV     R3,$REG3        ; SAVE R3
1414 006114 010237 001266                MOV     R2,$REG2        ; SAVE R2
1415 006120 010137 001264                MOV     R1,$REG1        ; SAVE R1
1416 006124 010037 001262                MOV     R0,$REG0        ; SAVE R0
1417 006130 000002                RTI                    ; LEAVE.
1418                ;
1419                ; RESTORE RO-R5
1420                ;
1421 006132 013700 001262      .RESOS: MOV     $REG0,R0  ; RESTORE R0
1422 006136 013701 001264                MOV     $REG1,R1        ; RESTORE R1
1423 006142 013702 001266                MOV     $REG2,R2        ; RESTORE R2
1424 006146 013703 001270                MOV     $REG3,R3        ; RESTORE R3

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1425	006152	013704	001272		MOV	\$REG4,R4	;RESTORE R4
1426	006156	013705	001274		MOV	\$REG5,R5	;RESTORE R5
1427	006162	000002			RTI		;LEAVE
1428							
1429							
1430							
1431							
1432	006164	104401	001313				
1433	006170	010046					
1434	006172	010146					
1435	006174	010346					
1436	006176	010446					
1437	006200	010546					
1438	006202	017601	000012				
1439	006206	062766	000002	000012			
1440	006214	012137	006406				
1441	006220	112137	006410		1\$:		
1442	006224	112137	006411				
1443	006230	013137	006412				
1444	006234	122737	000003	006410			
1445	006242	001003					
1446	006244	042737	177400	006412			
1447	006252	013704	006412		2\$:		
1448	006256	113705	006410				
1449	006262	012700	011106				
1450	006266	010403			3\$:		
1451	006270	042703	177770				
1452	006274	062703	000060				
1453	006300	110320					
1454	006302	000241					
1455	006304	006004					
1456	006306	000241					
1457	006310	006004					
1458	006312	000241					
1459	006314	006004					
1460	006316	005305					
1461	006320	001362					
1462	006322	012703	011150				
1463	006326	114023			4\$:		
1464	006330	105337	006410				
1465	006334	001374					
1466	006336	105737	006411				
1467	006342	001405					
1468	006344	112723	000040		5\$:		
1469	006350	105337	006411				
1470	006354	001373					
1471	006356	105013			6\$:		
1472	006360	104401	011150				
1473	006364	005337	006406				
1474	006370	001313					
1475	006372	012605					
1476	006374	012604					
1477	006376	012603					
1478	006400	012601					
1479	006402	012600					
1480	006404	000002					

 ;CONVRT: TYPE \$CRLF
 ;CONVRT: MOV R0,-(SP)
 MOV R1,-(SP)
 MOV R3,-(SP)
 MOV R4,-(SP)
 MOV R5,-(SP)
 MOV @12(SP),R1
 ADD #2,12(SP)
 MOV (R1)+,WRDCNT
 1\$: MOV (R1)+,CHRCNT
 MOV (R1)+,SPACNT
 MOV @2(R1)+,BINWRD
 CMPB #3,CHRCNT
 BNE 2\$
 BIC #177400,BINWRD
 2\$: MOV BINWRD,R4
 MOVB CHRCNT,R5
 MOV #TEMP,R0
 3\$: MOV R4,R3
 BIC #177770,R3
 ADD #060,R3
 MOVB R3,(R0)+
 CLC
 ROR R4
 CLC
 ROR R4
 CLC
 ROR R4
 DEC R5
 BNE 3\$
 MOV #MDATA,R3
 4\$: MOVB -(R0),(R3)+
 DECB CHRCNT
 BNE 4\$
 TSTB SPACNT
 BEQ 6\$
 5\$: MOVB #040,(R3)+
 DECB SPACNT
 BNE 5\$
 6\$: CLRB (R3)
 TYPE ,MDATA
 DEC WRDCNT
 BNE 1\$
 MOV (SP)+,R5
 MOV (SP)+,R4
 MOV (SP)+,R3
 MOV (SP)+,R1
 MOV (SP)+,R0
 RTI

1481 006406 000000
 1482 006410 000000
 1483 006411 000411
 1484 006412 000000
 1485
 1486
 1487
 1488
 1489
 1490
 1491
 1492
 1493
 1494
 1495
 1496
 1497
 1498
 1499

WRDCNT: 0
 CHRCNT: 0
 SPACNT=CHRCNT+1
 BINWRD: 0

;; TRAP DISPATCH SERVICE
 ;; ARGUMENT OF TRAP IS EXTRACTED
 ;; AND USED AS OFFSET TO OBTAIN POINTER
 ;; TO SELECTED SUBROUTINE

.SBTTL TRAP DECODER

;; *****
 ;; THIS ROUTINE WILL PICKUP THE LOWER BYTE OF THE "TRAP" INSTRUCTION
 ;; AND USE IT TO INDEX THROUGH THE TRAP TABLE FOR THE STARTING ADDRESS
 ;; OF THE DESIRED ROUTINE. THEN USING THE ADDRESS OBTAINED IT WILL
 ;; GO TO THAT ROUTINE.

1500 006414 010046
 1501 006416 016600 000002
 1502 006422 005740
 1503 006424 111000
 1504 006426 006300
 1505 006430 016000 006450
 1506 006434 000200
 1507
 1508
 1509
 1510

STRAP: MOV RO, -(SP) ;; SAVE RO
 MOV 2(SP), RO ;; GET TRAP ADDRESS
 TST -(RO) ;; BACKUP BY 2
 MOVB (RO), RO ;; GET RIGHT BYTE OF TRAP
 ASL RO ;; POSITION FOR INDEXING
 MOV \$TRPAD(RO), RO ;; INDEX TO TABLE
 RTS RO ;; GO TO ROUTINE

;; THIS IS USE TO HANDLE THE "GETPRI" MACRO

1511 006436 011646
 1512 006440 016666 000004 000002
 1513 006446 000002
 1514
 1515
 1516

STRAP2: MOV (SP), -(SP) ;; MOVE THE PC DOWN
 MOV 4(SP), 2(SP) ;; MOVE THE PSW DOWN
 RTI ;; RESTORE THE PSW

.SBTTL TRAP TABLE

;; THIS TABLE CONTAINS THE STARTING ADDRESSES OF THE ROUTINES CALLED
 ;; BY THE "TRAP" INSTRUCTION.

1517
 1518
 1519
 1520
 1521
 1522 006450 006436
 1523 006452 004414
 1524
 1525
 1526 006454 005144
 1527 006456 005264
 1528 006460 005564
 1529 006462 004364
 1530 006464 006072
 1531 006466 006132
 1532 006470 007362
 1533 006472 007332
 1534 006474 007400
 1535 006476 007446
 1536 006500 007512

ROUTINE			
STRPAD: WORD	\$TRAP2		
\$TYPE	;; CALL=TYPE	TRAP+1(104401)	TTY TYPEOUT ROUTINE
\$RDCHR	;; CALL=RDCHR	TRAP+2(104402)	TTY TYPEIN CHARACTER ROUTINE
\$RDLIN	;; CALL=RDLIN	TRAP+3(104403)	TTY TYPEIN STRING ROUTINE
\$RDOCT	;; CALL=RDOCT	TRAP+4(104404)	READ AN OCTAL NUMBER FROM TTY
\$.SCOPI	;; CALL=SCOPI	TRAP+5(104405)	CALL TO LOOP ON CURRENT DATA HANDLER
\$.SAVDS	;; CALL=SAVDS	TRAP+6(104406)	CALL TO REGISTER SAVE ROUTINE
\$.RESOS	;; CALL=RESOS	TRAP+7(104407)	CALL TO REGISTER RESTORE ROUTINE
\$.MSTCLR	;; CALL=MSTCLR	TRAP+10(104410)	CALL TO ISSUE A MASTER CLEAR
\$.DELAY	;; CALL=DELAY	TRAP+11(104411)	CALL TO DELAY
\$.ROMCLK	;; CALL=ROMCLK	TRAP+12(104412)	CALL TO CLOCK ROM ONCE
\$.DATACLK	;; CALL=DATACLK	TRAP+13(104413)	CALL TO CLOCK DATA
\$.TIMER	;; CALL=TIMER	TRAP+14(104414)	CALL TO DELAY A CLOCK TICK

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1537 006502 005724 $INPUT ;;CALL=INPUT TRAP+15(104415) CALL TO OCTAL # INPUT ROUTINE
1538 006504 006164 .CONVRT ;;CALL=CONVRT TRAP+16(104416) CALL TO .....
1539 006506 006170 .CNVRT ;;CALL=CNVRT TRAP+17(104417) CALL TO
1540 006510 006060 .ADVANCE ;;CALL=ADVANCE TRAP+20(104420) CALL TO ADVANCE TO NEXT TEST
1541
1542
1543 :-----:
1544 :*****:
1545 :ERROR HANDLER:
1546 :-----:
1547 006512 004737 011212 $ERROR: JSR PC,CKSWR ;CHECK FOR SOFT SWR
1548 006516 032777 010000 172514 BIT #SW12,JSWR ;BELL ON ERROR?
1549 006524 001406 BEQ XBZ ;BR IF NO BELL
1550 006526 105777 172516 TSTB JSWPS ;TTY READY.
1551 006532 100003 BPL XBZ ;DON'T WAIT IF TTY NOT READY.
1552 006534 112777 000207 172510 MOVB #207,JSWPB ;PUSH A BELL AT THE TTY.
1553 006542 032777 020000 172470 XBZ: BIT #SW13,JSWR ;DELETE ERROR PRINT OUT?
1554 006550 001107 BNE HALTS ;BR IF NO PRINT OUT WANTED.
1555 006552 021637 001216 CMP (SP),SERRPC ;WAS THIS ERROR FOUND LAST TIME?
1556 006556 001404 BEQ IS ;BR IF YES
1557 006560 011637 001216 MOV (SP),SERRPC ;RECORD BEING HERE
1558 006564 105037 001203 CLRB SERFLG ;PREPARE HEADER
1559 006570 104406 IS: SAVOS ;SAVE ALL PROC REGISTERS
1560 006572 011605 MOV (SP),R5 ;GET THE PC OF ERROR
1561 006574 162705 000002 SUB #2,R5 ;GET ADDRESS OF TRAP CALL
1562 006600 011504 MOV (R5),R4 ;GET ERROR INSTRUCTION
1563 006602 110437 001214 MOVB R4,$ITEMB ;COPY ERROR # FOR APT HANDLING
1564 006606 006304 ASL R4 ;MULT BY TWO
1565 006610 061504 ADD (R5),R4 ;DOUBLE IT
1566 006612 006304 ASL R4 ;MULT AGAIN
1567 006614 042704 177001 BIC #177001,R4 ;CLEAR JUNK
1568 006620 062704 001512 ADD #SERRTB,R4 ;GET POINTER
1569 006624 012437 006740 MOV (R4)+,ERRMSG ;GET ERROR MESSAGE
1570 006630 012437 006752 MOV (R4)+,DATAHD ;GET DATA HEADER
1571 006634 011437 006764 MOV (R4),DATABP ;GET DATA TABLE
1572 006640 105737 001203 TSTB SERFLG ;TYPE HEADREER
1573 006644 001403 BEQ TYPMSG ;BR IF YES
1574 006646 005737 006764 TST DATABP ;DOES DATA TABLE EXIST?
1575 006652 001040 BNE TYPDAT ;BR IF YES.
1576 006654 104401 001313 TYPMSG: TYPE ,SCLF
1577 006660 104401 001313 TYPE ,SCLF
1578 006664 005737 001444 TST LOCK
1579 006670 001402 BEQ IS
1580 006672 104401 010015 TYPE ,MASTEK
1581 006676 104401 010003 IS: TYPE ,MTSTN
1582 006702 104417 007120 CNVRT ,XTSTN ;SHOW IT
1583 006706 104401 010072 TYPE ,MERRPC ;TYPE PC.
1584 006712 104417 007112 CNVRT ,ERTABO ;SHOW IT
1585 006716 104401 001313 TYPE ,SCLF ;GIVE A CR/LF
1586 006722 112737 177777 001203 MOVB #-1,SERFLG ;NO MORE HEADER UNLESS NO DATA TABLE.
1587 006730 005737 006740 TST ERRMSG ;IS THERE AN ERROR MESSAGE?
1588 006734 001402 BEQ WRKO.FM ;BR IF NO.
1589 006736 104401 TYPE ;TYPE
1590 006740 000000 ERRMSG: 0 ;ERROR MESSAGE
1591 006742 WRKO.FM: ;
1592 006742 005737 006752 TST DATAHD ;DATA HEADER?

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1593 006746 001402          BEQ      TYPDAT      ;BR IF NO
1594 006750 104401          TYPE
1595 006752 000000          DATAHD: 0          ;TYPE
1596 006754 005737 006764  TYPDAT: TST      DATABP ;DATA HEADER
1597 006760 001402          BEQ      RESREG      ;DATA TABLE?
1598 006762 104416          CONVRT ;BR IF NO.
1599 006764 000000          DATABP: 0          ;SHOW
1600 006766 104407          RESREG: RESOS      ;DATA TABLE
1601 006770 122737 000001 001336 HALTS:  CMPB      #APTENV,SENV ;RESTORE PROC REGISTERS
1602 006776 001007          BNE      3$          ;IS APT RUNNING?
1603 007000 113737 001214 007012  MOVB     $ITEMB,6$ ;SKIP APT CALL IF NOT.
1604 007006 004737 004714          JSR      PC,$ATY4   ;COPY ERROR #.
1605 007012 000000          .WORD   0          ;CALL APT SERVICES.
1606 007014 000777          BR       9$          ;ERROR # GOES HERE.
1607 007016 022737 004070 000042 3$:     CMP      #SENDAD,2#42 ;LOCK HERE.
1608 007024 001403          BEQ      1$          ;IF ACT-11 AUTOMATIC MODE, HALT!!
1609 007026 005777 172206          TST      2$SWR
1610 007032 100005          BPL      EXITER
1611 007034 010046          1$:     PUSHRO ;HALT ON ERROR?
1612 007036 016600 000002          MOV      2(SP),RO  ;BR IF NO HALT ON ERROR
1613 007042 000000          HALT ;SAVE RO
1614 007044 012600          POPRO  ;SHOW ERROR PC IN DATA LIGHTS
1615 007046 005237 001212          EXITER: INC      $ERTTL ;HALT
1616 007052 032777 000400 172160  BIT      #SW08,2$SWR ;GET RO
1617 007060 001007          BNE      1$          ;UPDATE ERROR COUNT
1618 007062 032777 002000 172150  BIT      #SW10,2$SWR ;GOTO TOP OF TEST?
1619 007070 001407          BEQ      2$          ;BR IF YES
1620 007072 013737 001442 001206  MOV      NEXT,$LPADR ;GOTO NEXT TEST?
1621 007100 012706 001200 1$:     MOV      #STACK,SP ;BR IF NO
1622 007104 000177 172076          JMP      2$LPADR   ;SET FOR NEXT TEST
1623 007110 000002          RTI ;RESET SP
1624 007112 000001          ERTABO: 1          ;GOTO SPECIFIED TEST
1625 007114 006 002          .BYTE   6,2 ;$LPADR
1626 007116 001460          SAVPC ;
1627 007120 000001          XTSTN: 1          ;
1628 007122 003 002          .BYTE   3,2 ;
1629 007124 001202          $STNM ;
1630 ;ENTER HERE ON POWER FAILURE
1631 ;-----
1632
1633 .SBTTL POWER DOWN AND UP ROUTINES
1634
1635 ;*****
1636 ;POWER DOWN ROUTINE
1637 007126 012737 007316 000024 $PWDRN: MOV      #ILLUP,2#PWRVEC ;:SET FOR FAST UP
1638 007134 012737 000340 000026  MOV      8340,2#PWRVEC+2 ;:PRIO:7
1639 007142 010046          MOV      RO,-(SP) ;:PUSH RO ON STACK
1640 007144 010146          MOV      R1,-(SP) ;:PUSH R1 ON STACK
1641 007146 010246          MOV      R2,-(SP) ;:PUSH R2 ON STACK
1642 007150 010346          MOV      R3,-(SP) ;:PUSH R3 ON STACK
1643 007152 010446          MOV      R4,-(SP) ;:PUSH R4 ON STACK
1644 007154 010546          MOV      R5,-(SP) ;:PUSH R5 ON STACK
1645 007156 017746 172056  MOV      2$SWR,-(SP) ;:PUSH 2$SWR ON STACK
1646 007162 010637 007322  MOV      SP,$SAVR6 ;:SAVE SP
1647 007166 012737 007200 000024  MOV      #PWRUP,2#PWRVEC ;:SET UP VECTOR
1648 007174 000000          HALT

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1649 007176 000776 BR -2 ;;HANG UP
1650
1651 ;:*****
1652 ;:POWER UP ROUTINE
1653 007200 012737 007316 000024 $PWRUP: MOV $SILLUP, @PWRVEC ;;SET FOR FAST DOWN
1654 007206 013706 007322 MOV $SAVR6, SP ;;GET SP
1655 007212 005037 007322 CLR $SAVR6 ;;WAIT LOOP FOR THE TTY
1656 007216 005237 007322 1$: INC $SAVR6 ;;WAIT FOR THE INC
1657 007222 001375 BNE 1$ ;;OF WORD
1658 007224 104401 007562 TYPE ,MPFAIL
1659 007230 104417 007324 CNVRT ,PFTAB
1660 007234 105037 001203 CLRB $ERFLG ;;CLEAR ERROR FLAG.
1661 007240 005037 001216 CLR $ERRPC ;;CLEAR LAST ERROR PC
1662 007244 013701 002066 MOV KMCSR, R1 ;;RESTORE DEVICE ADDRESS.
1663 007250 005011 CLR (R1) ;;CLEAR THE CSR.
1664 007252 104410 MSTCLR
1665 007254 012677 171760 MOV (SP)+, @SWR ;;POP STACK INTO @SWR
1666 007260 012605 MOV (SP)+, R5 ;;POP STACK INTO R5
1667 007262 012604 MOV (SP)+, R4 ;;POP STACK INTO R4
1668 007264 012603 MOV (SP)+, R3 ;;POP STACK INTO R3
1669 007266 012602 MOV (SP)+, R2 ;;POP STACK INTO R2
1670 007270 012601 MOV (SP)+, R1 ;;POP STACK INTO R1
1671 007272 012600 MOV (SP)+, R0 ;;POP STACK INTO R0
1672 007274 012737 007126 000024 MOV $PWRDN, @PWRVEC ;;SET UP THE POWER DOWN VECTOR
1673 007302 012737 000340 000026 MOV #340, @PWRVEC+2 ;;PRIO:7
1674 007310 104401 TYPE REPORT THE POWER FAILURE
1675 007312 007562 $PWRMG: .WORD MPFAIL ;;POWER FAIL MESSAGE POINTER
1676 007314 000002 RTI
1677 007316 000000 $SILLUP: HALT ;;THE POWER UP SEQUENCE WAS STARTED
1678 007320 000776 BR -2 ;;BEFORE THE POWER DOWN WAS COMPLETE
1679 007322 000000 $SAVR6: 0 ;;PUT THE SP HERE
1680
1681 007324 000001 PFTAB: 1
1682 007326 003 002 .BYTE 3,2
1683 007330 001202 $TSTNM
1684
1685 007332 .DELAY:
1686 007332 012777 000020 172534 MOV #20, @KMP04
1687 007340 104412 ROMCLK ;;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1688 007342 121111 121111 ;;POKE CLOCK DELAY BIT
1689 007344 1$: ROMCLK ;;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1690 007344 104412 121224 ;;PORT4+IBUS#11
1691 007346 121224 BIT #BIT4, @KMP04 ;;IS CLOCK BIT SET?
1692 007350 032777 000020 172516 BEQ 1$ ;;BR IF NO
1693 007356 001772 RTI
1694 007360 000002
1695
1696 007362 .MSTCLR:
1697 007362 152777 000100 172500 BISB #BIT6, @KMCSRH ;;SET MASTER CLEAR
1698 007370 142777 000300 172472 BICB #BIT6, BIT7, @KMCSRH ;;CLEAR MASTER CLEAR AND RUN
1699 007376 000002 RTI ;;RETURN
1700
1701 007400 .ROMCLK:
1702 007400 152777 000002 172462 BISB #BIT1, @KMCSRH ;;SET ROMI
1703 007406 013677 172464 MOV @SP, @KMP06 ;;LOAD INSTRUCTION IN SEL6
1704 007412 062746 000002 ADD #2, -(SP) ;;ADJUST STACK
    
```

POWER DOWN AND UP ROUTINES

```

1705 007416 032777 000100 171614 BIT #SW06,SWR ;HALT IF SW06 =1
1706 007424 001401 BEQ IS ;BR IF SW06 =0
1707 007426 000000 HALT ;HALT BEFORE CLOCKING INSTRUCTION
1708 007430 152777 000003 172432 1S: BISR #BIT1:BIT0,AKMCSRH ;CLOCK INSTRUCTION
1709 007436 142777 000007 172424 BICB #BIT2:BIT1:BIT0,AKMCSRH ;CLEAR ROMI, ROMI, STEP
1710 007444 000002 RTI
1711
1712 007446 .DATACLK:
1713 007446 013637 011106 MOV @2(SP)+,TEMP ;PUT TICK COUNT IN TEMP
1714 007452 062746 000002 ADD #2,-(SP) ;ADJUST STACK
1715 007456 152777 000020 172404 1S: BISR #BIT4,AKMCSRH ;SET STEP LU
1716 007464 027777 172376 172374 CMP AKMCSR,AKMCSR ;WASTE TIME
1717 007472 142777 000020 172370 BICB #BIT4,AKMCSRH ;CLEAR STEP LU
1718 007500 005337 011106 DEC TEMP ;DEC TICK COUNT
1719 007504 001364 BNE IS ;BR IF NOT DONE
1720 007506 000002 RTI ;RETURN
1721 007510 000001 3S: .BLKW 1
1722
1723 007512 .TIMER:
1724 007512 013637 011106 MOV @2(SP)+,TEMP ;MOVE COUNT TO TEMP
1725 007516 062746 000002 ADD #2,-(SP) ;ADJUST STACK
1726 007522 104412 1S: ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1727 007524 021364 021364 ;PORT4+IBUS* REG11
1728 007526 032777 000002 172340 BIT #2,AKMP04 ;IS PGM CLOCK BIT CLEAR?
1729 007534 001772 BEQ IS ;BR IF YES
1730
1731 007536 104412 2S: ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1732 007540 021364 021364 ;PORT4+IBUS* REG11
1733 007542 032777 000002 172324 BIT #2,AKMP04 ;IS PGM CLOCK BIT SET?
1734 007550 001372 BNE 2S ;BR IF YES
1735 007552 005337 011106 DEC TEMP ;DEC COUNT
1736 007556 001361 BNE IS ;BR IF NOT DONE
1737 007560 000002 RTI ;RETURN
1738
1739
1740 007562 050200 051127 043040 MPFAIL: .ASCIZ <200>/PWR FAILED. RESTART AT TEST /
(2) 007620 042600 042116 050040 MEPASS: .ASCIZ <200>/END PASS DZKCC /
(2) 007642 051200 000 MR: .ASCIZ <200>/R/
(2) 007645 200 047516 042040 MERR2: .ASCIZ <200>/NO DEVICES PRESENT./
(2) 007672 044600 051516 043125 MERR3: .ASCIZ <200>/INSUFFICIENT DATA!/
(2) 007716 046200 041517 020113 MLOCK: .ASCIZ <200>/LOCK ON SELECTED TEST/
(2) 007745 103 051123 020072 MCSR: .ASCIZ /CSR: /
(2) 007753 126 041505 020072 MVEC: .ASCIZ /VEC: /
(2) 007761 120 051501 042523 MPASSX: .ASCIZ /PASSES: /
(2) 007772 051105 047522 051522 MERRX: .ASCIZ /ERRORS: /
(2) 010003 124 051505 020124 MTSTN: .ASCIZ /TEST NO: /
(2) 010015 052 000 MASTEK: .ASCIZ /*/
(2) 010017 200 042523 020124 MNEW: .ASCIZ <200>/SET SWITCH REG TO KMC11'S DESIRED ACTIVE./
(2) 010072 041520 020072 000 MERRPC: .ASCIZ /PC: /
(2) 010077 200 020040 020040 XHEAD: .ASCII <200>/
(2) 010136 020200 020040 020040 .ASCII <200>/
(2) 010175 200 020040 041520 .ASCII <200>/ PC CSR STAT1 STAT2 STAT3/
(2) 010247 200 026455 026455 .ASCIZ <200>/-----
(2) 010323 200 047510 020127 NUM: .ASCIZ <200>/HOW MANY KMC11'S TO BE TESTED?/
(2) 010363 200 051503 020122 CSR: .ASCIZ <200>/CSR ADDRESS?/
(2) 010401 200 042526 052103 VEC: .ASCIZ <200>/VECTOR ADDRESS?/

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POWER DOWN AND UP ROUTINES

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(2) 010422 041200 020122 051120 PRIO: .ASCIZ <200>/BR PRIORITY LEVEL? (4,5,6,7)?/
(2) 010461 200 044127 041511 MODU: .ASCIZ <200>/WHICH LINE UNIT? IF NONE TYPE "N", IF M8201 TYPE "1", IF M8202 TYP
(2) 010573 200 053523 052111 LINE: .ASCIZ <200>/SWITCH PAC#1 (DDCMP LINE #)?/
(2) 010631 200 053523 052111 BM: .ASCIZ <200>/SWITCH PAC#2 (BM873 BOOT ADD)?/
(2) 010671 200 051511 052040 CONN: .ASCIZ <200>/IS THE LOOP BACK CONNECTOR ON?/
(2) 010731 200 047516 042040 NOACT: .ASCIZ <200>/NO DEVICES ARE SELECTED/
(2) 010762 100200 046513 030503 CONERR: .ASCIZ <200><200>/KMC11 AT NONSTANDARD ADDRESS PC: /
(2) 011027 200 054105 042520 CNERR: .ASCIZ <200>/EXPECTED FOUND/
(2) 011050 024040 046513 024503 KCM: .ASCIZ / (KMC) /
(2) .EVEN
(2) 011060 000005 XSTATQ: 5
1741 011062 006 003 .BYTE 6,3
1742 011064 001276 $TMPO
1743 011066 006 003 .BYTE 6,3
1744 011070 001300 $TMP1
1745 011072 006 003 .BYTE 6,3
1746 011074 001302 $TMP2
1747 011076 006 003 .BYTE 6,3
1748 011100 001304 $TMP3
1749 011102 006 002 .BYTE 6,2
1750 011104 001306 $TMP4
1751 .EVEN
1752
1753 ;BUFFERS FOR INPUT-OUTPUT
1754
1755 011106 000000 TEMP: 0
1756 011150 011150 .=. +40
1757 011150 000000 MDATA: 0
1758 011212 011212 .=. +40
1759
1760
1761 ;ROUTINE USED TO CHANGE SOFTWARE SWITCH
1762 ;REGISTER USING THE CONSOLE TERMINAL
1763 -----
1764
1765 011212 022737 000176 001240 CKSWR: CMP #SWREG, SWR ; IS THE SOFT SWR BEING USED?
1766 011220 001075 BNE CKSWR5 ; BR IF NO
1767 011222 132737 000001 001336 BITB #1, SENV ; IS IT RUNNING UNDER APT?
1768 011230 001071 BNE CKSWR5 ; EXIT IF YES.
1769 011232 022777 000007 170006 CMP #7, #STKB ; WAS CTRL G TYPED? (7 BIT ASCII)
1770 011240 001404 BEQ 1$ ; BR IF YES
1771 011242 022777 000207 167776 CMP #207, #STKB ; WAS CTRL G TYPED? (8 BIT ASCII)
1772 011250 001061 BNE CKSWR5 ; BR IF NO
1773 011252 010246 1$: MOV R2, -(SP) ; STORE R2
1774 011254 010346 MOV R3, -(SP) ; STORE R3
1775 011256 010446 MOV R4, -(SP) ; STORE R4
1776 011260 012737 177777 011416 MOV #-1, SWFLG ; SET SOFT TYPE OUT FLAG
1777 011266 005002 CKSWR1: CLR R2 ; CLEAR NEW SWR CONTENTS
1778 011270 012704 177777 MOV #-1, R4 ; SET FLAG TO ALL ONES
1779 011274 104401 005541 TYPE #MSWR ; TYPE "SWR="
1780 011300 104417 CKSWR2: CNVRT ; TYPE OUT PRESENT CONTENTS
1781 011302 011452 SOFTSW ; OF SOFT SWITCH REGISTER
1782 011304 104401 005552 CKSWR3: TYPE #MNEW ; TYPE "NEW="
1783 011310 004737 011420 CKSWR4: JSR PC, INCHAR ; GET RESPONSE
1784 011314 022703 000015 CMP #15, R3 ; WAS IT A CR?
1785 011320 001424 BEQ 5$ ; BR IF YES
    
```

1786	011322	022703	000012			CMP	#12,R3	: WAS IT A LF?
1787	011326	001416				BEQ	45	: BR IF YES
1788	011330	022703	000025			CMP	#25,R3	: WAS IT CTRL U?
1789	011334	001754				BEQ	CKSWR1	: BR IF YES(START OVER)
1790	011336	022703	000007			CMP	#7,R3	: IF CNTL G GET NEXT CHAR
1791	011342	001762				BEQ	CKSWR4	
1792	011344	005004				CLR	R4	: IT MUST BE A DIGIT SO CLR FLAG
1793	011346	042703	177770			BIC	#177770,R3	: ONLY 0-7 ARE LEGAL SO MASK OFF BITS
1794	011352	006302				ASL	R2	: SHIFT R2 3 TIMES
1795	011354	006302				ASL	R2	
1796	011356	006302				ASL	R2	
1797	011360	050302				BIS	R3,R2	: ADD LAST DIGIT
1798	011362	000752				BR	CKSWR4	: GET NEXT CHARACTER
1799	011364	012766	002402	000006	45:	MOV	#.START,6(SP)	: LF WAS TYPED SO GO TO START
1800	011372	005704			55:	TST	R4	: IS FLAG CLEAR?
1801	011374	001002				BNE	65	: IF NOT DON'T CHANGE SOFT SWR
1802	011376	010277	167636			MOV	R2,@SWR	: IF YES THEN WRITE NEW CONTENTS TO SOFT SWR
1803	011402	005037	011416		65:	CLR	SWFLG	: CLEAR TYPEOUT FLAG
1804	011406	012604				MOV	(SP)+,R4	: RESTORE R4
1805	011410	012603				MOV	(SP)+,R3	: RESTORE R3
1806	011412	012602				MOV	(SP)+,R2	: RESTORE R2
1807	011414	000207				CKSWRS: RTS	PC	: RETURN
1808								
1809	011416	000000				SWFLG: 0		
1810								
1811	011420	105777	167620			INCHAR: TSTB	@STKS	
1812	011424	100375				BPL	-4	
1813	011426	017703	167614			MOV	@STKB,R3	
1814	011432	105777	167612			TSTB	@STPS	
1815	011436	100375				BPL	-4	
1816	011440	010377	167606			MOV	R3,@STPB	
1817	011444	042703	000200			BIC	#BIT7,R3	
1818	011450	000207				RTS	PC	
1819								
1820	011452	000001				SOFTSM: 1		
1821	011454	006	002			.BYTE	6,2	
1822	011456	000176				SWREG		

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011460	005737	001470	
011464	001004		
011466	104401	010731	
011472	000000		
011474	000776		
011476	000241		
011500	006137	001500	
011504	005537	001500	
011510	062737	000004	001504
011516	062737	000010	001502
011524	022737	002300	001502
011532	001006		
011534	012737	002100	001502
011542	012737	002302	001504
011550	033737	001500	001470
011556	001747		
011560	013700	001502	
011564	013702	001504	
011570	012037	002066	
011574	011037	002056	
011600	042737	177000	002056
011606	012037	002050	
011612	012037	002052	
011616	012037	002054	
011622	012237	001324	
011626	012237	001212	
011632	012700	000002	
011636	013737	002066	002070
011644	005237	002070	
011650	013737	002070	002072
011656	005237	002072	
011662	013737	002072	002074
011670	060037	002074	
011674	013737	002074	002076
011702	060037	002076	
011706	013737	002056	002060
011714	060037	002060	
011720	013737	002060	002062
011726	060037	002062	
011732	013737	002062	002064
011740	060037	002064	
011744	032737	000002	001446
011752	001447		
011754	005737	000042	

```

ROUTINE USED TO "CYCLE" THROUGH UP TO 16 KMC11'S
THIS ROUTINE SETS UP THE CONTROL ADDRESS FOR THE DIAGNOSTIC
AND RUNS THE SPECIFIED KMC11'S. THIS ROUTINE *MUST*
BE RUN FIRST BEFORE ENTERING THE DIAGNOSTIC FOR THE
SETUP NECESSARY.
    
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CYCLE:	TST	KMACTV			:ARE ANY KMC11'S TO BE TESTED?
	BNE	1\$:BR IF OK.
	TYPE	,NOACT			:NO KMC11'S SELECTED!!
	HALT				:STOP THE SHOW.
	BR	.-2			:DISQUALIFY CONT. SW.
1\$:	CLC				:CLEAR PROC. CARRY BIT.
	ROL	RUN			:UPDATE POINTER
	ADC	RUN			:CATCH CARRY FROM RUN
	ADD	#4,MILK			:UPDATE POINTER
	ADD	#10,CREAM			:UPDATE ADDRESS POINTER.
	CMP	#KM.MAP+200,CREAM			
	BNE	2\$:KEEP GOING; NOT ALL TESTED FOR.
	MOV	#KM.MAP,CREAM			:RESET ADDRESS POINTER.
	MOV	#CNT.MAP,MILK			:RESET PASS COUNT POINTER
2\$:	BIT	RUN,KMACTV			:IS THIS ONE ACTIVE?
	BEQ	1\$:BR IF NO
	MOV	CREAM,R0			:GET ADDRESS POINTER
	MOV	MILK,R2			:GET PASS COUNT POINTER
	MOV	(R0)+,KMCSR			:LOAD SYSTEM CTRL. REG
	MOV	(R0),KMRVEC			:LOAD VECTOR
	BIC	#177000,KMRVEC			:CLEAR UNWANTED BITS
	MOV	(R0)+,STAT1			:LOAD STAT1
	MOV	(R0)+,STAT2			:LOAD STAT2
	MOV	(R0)+,STAT3			:LOAD STAT3
	MOV	(R2)+,SPASS			:LOAD PASS COUNT
	MOV	(R2)+,SERTTL			:LOAD ERROR COUNT
	MOV	#2,R0			:SAVE CORE THIS WAY!
	MOV	KMCSR,KMCSRH			
	INC	KMCSRH			
	MOV	KMCSRH,KMCTL			
	INC	KMCTL			
	MOV	KMCTL,KMP04			
	ADD	R0,KMP04			
	MOV	KMP04,KMP06			
	ADD	R0,KMP06			
	MOV	KMRVEC,KMRLVL			:PTY LVL
	ADD	R0,KMRLVL			
	MOV	KMRLVL,KMTVEC			:TX VEC
	ADD	R0,KMTVEC			
	MOV	KMTVEC,KMTLVL			:TX LVL
	ADD	R0,KMTLVL			
	BIT	#SW01,STRTSW			:IS TEST NO. SELECTED
	BEQ	7\$:BR IF NO
4\$:	TST	#42			:RUNNING IN AUTO MODE?

```

1879 011760 001044      BNE      7$          ;BR IF YES
1880 011762 104401 001313  TYPE      ,SCRLF
1881 011766 104415      INPUT
1882 011770 010003      MTSTN
1883 011772 000001      1
1884 011774 001000      1000
1885 011776 001202      $TSTNM
1886 012000      000      .BYTE
1887 012001      001      .BYTE
1888 012002 012700 013732      MOV      #TST1,R0
1889 012006 022710      5$:      CMP      (PC)+,(R0)      ;CMP FIRST WORD TO 12737
1890 012010 012737      MOV      (PC)+,2(PC)+
1891 012012 001020      BNE      6$          ;BR IF NOT SAME
1892 012014 023760 001202 000002      CMP      $TSTNM,2(R0)      ;DOES $TSTNM MATCH?
1893 012022 001014      BNE      6$          ;BR IF NO
1894 012024 022760 001202 000004      CMP      #TSTNM,4(R0)      ;IS LAST WORD OK?
1895 012032 001010      BNE      6$          ;BR IF NO
1896 012034 010037 001206      MOV      R0,$LPADR      ;IT IS A LEGAL TEST SO DO IT
1897 012040 104401 007642      TYPE      MR
1898 012044 042737 000002 001446      BIC      #SW01,STRTSW
1899 012052 000412      BR
1900 012054 005720      6$:      TST      (R0)+          ;POP R0
1901 012056 020027 034670      CMP      R0,#TLAST+10      ;AT END YET?
1902 012062 001351      BNE      5$          ;BR IF NO
1903 012064 104401 001312      TYPE      $QUES          ;YES ILLEGAL TEST NO.
1904 012070 000731      BR      4$          ;TRY AGAIN
1905
1906 012072 012737 013732 001206 7$:      MOV      #TST1,$LPADR      ;PREPARE $LPADR ADDRESS
1907 012100 013701 002066 8$:      MOV      KMC$R,R1          ;R1 = BASE KMC11 ADDRESS
1908 012104 000177 167076      JMP      2$LPADR          ;GO START TESTING.
1909
1910
1911      ;ROUTINE USED TO "AUTO SIZE" THE KMC11
1912      ;CSR AND VECTOR.
1913      ;NOTE: THE CSR MAY BE ANY WHERE IN THE FLOATING
1914      ;ADDRESS RANGE (160000:164000)
1915      ;AND THE VECTOR MAY BE ANY WHERE IN THE
1916      ;FLOATING VECTOR RANGE (300:770)
1917      ;
1918      ;
1919      AUTO.SIZE:
1920 012110 000005      RESET
1921 012112 012702 002100      CSRMAP: MOV      #KM.MAP,R2      ;INSURE A BUS INIT.
1922 012116 005022      1$:      CLR      (R2)+          ;LOAD MAP POINTER.
1923 012120 022702 002300      CMP      #KM.END,R2      ;ZERO ENTIRE MAP
1924 012124 001374      BNE      1$          ;ALL DONE?
1925 012126 005037 001472      CLR      K$NUM          ;BR IF NO
1926 012132 012702 002100      MOV      #KM.MAP,R2      ;SET OCTAL NUMBER OF KMC11'S TO 0
1927 012136 005037 001470      CLR      K$ACTV          ;R2 POINTS TO KMC MAP
1928 012142 032737 000001 001446      BIT      #SW00,STRTSW      ;CLEAR ACTIVE
1929 012150 001002      BNE      .+6          ;QUESTIONS?
1930 012152 000137 012532      JMP      7$          ;BR IF YES
1931 012156 012737 000001 001306      MOV      #1,$TMP4          ;IF NO SKIP QUESTIONS
1932 012164 104415      INPUT
1933 012166 010323      NUM
1934 012170 000001      1          ;START WITH 1
    
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1935	012172	000020			16.			
1936	012174	001302			STMP2			
1937	012176	000			.BYTE	0		
1938	012177	001			.BYTE	1		
1939	012200	013737	001302	001472	MOV	STMP2,KMNUM		;KMNUM = HOW MANY
1940	012206	104401	001313	12S:	TYPE	,SCLF		
1941	012212	104416			CONVRT			;TYPE WHICH KMC IS BEING DONE
1942	012214	013164			WHICH			;STMP4 IS WHICH KMC
1943	012216	005237	001306		INC	STMP4		
1944	012222	104415			INPUT			
1945	012224	010363			CSR			
1946	012226	160000			160000			
1947	012230	164000			164000			
1948	012232	001304			STMP3			
1949	012234	000			.BYTE	0		
1950	012235	001			.BYTE	1		
1951	012236	013722	001304		MOV	STMP3,(R2)+		;STORE CSR IN MAP
1952	012242	104415			INPUT			
1953	012244	010401			VEC			
1954	012246	000000			0			
1955	012250	000776			776			
1956	012252	001304			STMP3			
1957	012254	000			.BYTE	0		
1958	012255	001			.BYTE	1		
1959	012256	013712	001304		MOV	STMP3,(R2)		;STORE VECTOR IN MAP
1960	012262	104401		10S:	TYPE			
1961	012264	010422			PRIO			;ASK WHAT BR LEVEL
1962	012266	004737	013456		JSR	PC,INTTY		;GET RESPONSE
1963	012272	022703	000024		CMP	#24,R3		
1964	012276	101014			BHI	50S		;BR IF LESS THAN 4
1965	012300	022703	000027		CMP	#27,R3		
1966	012304	103411			BLO	50S		;BR IF GREATER THAN 7
1967	012306	012704	000011		MOV	#11,R4		;R4 = NUMBER OF SHIFTS
1968	012312	006303			ASL	R3		;SHIFT R3 LEFT
1969	012314	005304			DEC	R4		;DEC SHIFT COUNT
1970	012316	001375			BNE	.-4		;BR IF NOT DONE
1971	012320	042703	170777		BIC	#170777,R3		;BIC UNWANTED BITS
1972	012324	050312			BIS	R3,(R2)		;PUT BR LEVEL IN STATUS MAP
1973	012326	000403			BR	8S		;CONTINUE
1974	012330	104401		50S:	TYPE			
1975	012332	001312			SQUES			;RESPONSE IS OUT OF LIMITS
1976	012334	000752			BR	10S		;TRY AGAIN
1977	012336			8S:				
1978	012336			9S:				
1979	012336	104401		16S:	TYPE			
1980	012340	010461			MODU			;ASK WHICH LINE UNIT
1981	012342	004737	013456		JSR	PC,INTTY		;GET REPLY
1982	012346	022703	000021		CMP	#21,R3		; "1"
1983	012352	001417			BEQ	30S		
1984	012354	022703	000022		CMP	#22,R3		; "2"
1985	012360	001412			BEQ	31S		
1986	012362	022703	000116		CMP	#116,R3		; "N"
1987	012366	001403			BEQ	32S		
1988	012370	104401			TYPE			
1989	012372	001312			SQUES			; IF NOT A 1,2 OR N TYPE "?"
1990	012374	000760			BR	16S		;TRY AGIAN

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1991 012376 052722 010000 32$: BIS #BIT12,(R2)+ ;SET BIT 12 IN STAT2 IF NO LU
1992 012402 022222 CMP (R2)+,(R2)+ ;POP OVER STAT2 AND STAT3
1993 012404 000445 BR 33$
1994 012406 052712 020000 31$: BIS #BIT13,(R2) ;SET BIT 13 IN STAT2 IF M8202
1995 012412 104401 30$: TYPE
1996 012414 010671 CONN ;ASK IF LOOP-BACK IS ON
1997 012416 004737 013456 JSR PC,INTTY ;GET REPLY
1998 012422 022703 000131 CMP #131,R3 ;Y
1999 012426 001406 BEQ 17$
2000 012430 022703 000116 CMP #116,R3 ;N
2001 012434 001406 BEQ 18$
2002 012436 104401 TYPE
2003 012440 001312 SQUES ;IF NOT Y OR N TYPE "?"
2004 012442 000763 BR 30$ ;TRY AGAIN
2005 012444 052722 040000 17$: BIS #BIT14,(R2)+ ;TURNAROUND IS CONNECTED
2006 012450 000402 BR 19$
2007 012452 042722 040000 18$: BIC #BIT14,(R2)+ ;NO TURNAROUND
2008 012456 19$:
2009 012456 104415 INPUT
2010 012460 010573 LINE
2011 012462 000000 0
2012 012464 000377 377
2013 012466 001304 STMP3
2014 012470 000 .BYTE 0
2015 012471 001 .BYTE 1
2016 012472 113722 001304 MOV#B STMP3,(R2)+ ;STORE SWITCH PAC IN MAP
2017 012476 104415 INPUT
2018 012500 010631 BM
2019 012502 000000 0
2020 012504 000377 377
2021 012506 001304 STMP3
2022 012510 000 .BYTE 0
2023 012511 001 .BYTE 1
2024 012512 113722 001304 MOV#B STMP3,(R2)+ ;STORE SWITCH PAC IN MAP
2025 012516 005722 TST (R2)+ ;POP OVER STAT3
2026 012520 005337 001302 33$: DEC STMP2 ;DEC KMC COUNT
2027 012524 001230 BNE 12$ ;BR IF MORE TO DO
2028 012526 000137 013064 JMP 13$ ;CONTINUE
2029 012532 012701 160000 7$: MOV #160000,R1 ;SET FOR FIRST ADDRESS TO BE TESTED
2030 012536 012737 013156 000004 MOV #6$,R4 ;SET FOR NON-EXISTANT DEVICE TIME OUT
2031 012544 005011 2$: CLR (R1) ;CLEAR SEL0
2032 012546 005711 TST (R1) ;IF KMC11 KMCSR S/B 0
2033 012550 001135 BNE 3$ ;IF NO DEV ; TRAP TO 4. IF NO BIT 8 THEN NO KMC11
2034 012552 005061 000006 CLR 6(R1) ;CLEAR SEL6
2035 012556 005761 000006 TST 6(R1) ;IF KMC11 THEN KMERIC S/B =0!
2036 012562 001130 BNE 3$ ;BR IF NOT KMC11
2037 012564 012711 002000 MOV #BIT10,(R1) ;SET ROM0
2038 012570 005061 000004 CLR 4(R1) ;CLEAR SEL4
2039 012574 012761 125252 000006 MOV #125252,6(R1) ;WRITE THIS TO SEL6
2040 012602 052711 020000 BIS #BIT13,(R1) ;WRITE IT!
2041 012606 022761 125252 000004 CMP #125252,4(R1) ;WAS IT WRITTEN?
2042 012614 001113 BNE 3$ ;IF NO IT IS NOT CRAM
2043 ;AT THIS POINT IT IS ASSUMED THAT R1 HOLDS A KMC11 CSR ADDRESS.
2044 21$:
2045 012616 010122 22$: MOV R1,(R2)+ ;STORE CSR IN CORE TABLE.
2046 012620 012711 001000 15$: MOV #BIT9,(R1) ;CLEAR LINE UNIT LOOP

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2047	012624	005061	000004		CLR	4(R1)	: CLEAR PORT4
2048	012630	012761	122113	000006	MOV	#122113,6(R1)	: LOAD INSTRUCTION (CLR DTR)
2049	012636	052711	000400		BIS	#BIT8,(R1)	: CLOCK INSTRUCTION
2050	012642	012761	021264	000006	MOV	#021264,6(R1)	: LOAD INSTRUCTION
2051	012650	052711	000400		BIS	#BIT8,(R1)	: CLOCK INSTRUCTION
2052	012654	122761	000377	000004	CMPB	#377,4(R1)	: IS IT ALL ONES?
2053	012662	001003			BNE	.+10	: BR IF NO
2054	012664	052712	010000		BIS	#BIT12,(R2)	: IF YES, NO LINE UNIT, SET STATUS BIT
2055	012670	000436			BR	205	
2056	012672	032761	000002	000004	BIT	#BIT1,4(R1)	: IS SWITCH A ONE?
2057	012700	001403			BEQ	.+10	: BR IF M8201
2058	012702	052712	060000		BIS	#BIT13:BIT14,(R2)	: M8202 ASSUME CONNECTOR
2059	012706	000427			BR	205	: CONNECTOR ON)
2060	012710	032761	000010	000004	BIT	#BIT3,4(R1)	: IS MRDY SET
2061	012716	001023			BNE	205	: BR IF M8201 NO CONNECTOR (ON LINE)
2062	012720	012761	000100	000004	MOV	#BIT6,4(R1)	: LOAD PORT4
2063	012726	012761	122113	000006	MOV	#122113,6(R1)	: LOAD INSTRUCTION
2064	012734	052711	000400		BIS	#BIT8,(R1)	: CLOCK INSTRUCTION (SET DTR)
2065	012740	012761	021264	000006	MOV	#021264,6(R1)	: LOAD INSTRUCTION
2066	012746	052711	000400		BIS	#BIT8,(R1)	: CLOCK INSTRUCTION (READ MODEM REG)
2067	012752	032761	000010	000004	BIT	#BIT3,4(R1)	: IS MRDY SET NOW?
2068	012760	001402			BEQ	205	: BR IF NO CONNECTOR
2069	012762	052712	040000		BIS	#BIT14,(R2)	: SET STATUS BIT FOR CONNECTOR
2070	012766	005722			TST	(R2)+	: POP POINTER
2071	012770	012761	021324	000006	MOV	#021324,6(R1)	: PUT INSTRUCTION IN PORT6
2072	012776	012711	001400		MOV	#BIT9:BIT8,(R1)	: PORT4+LU 15
2073	013002	156122	000004		BISB	4(R1),(R2)+	: STORE DCMP LINE # IN TABLE
2074	013006	012761	021344	000006	MOV	#021344,6(R1)	: PORT6+INSTRUCTION
2075	013014	012711	001400		MOV	#BIT8:BIT9,(R1)	: CLOCK INSTR.
2076	013020	156122	000004		BISB	4(R1),(R2)+	: STORE BM873 ADD IN TABLE
2077	013024	005722			TST	(R2)+	: POP OVER STAT3
2078	013026	005011			CLR	(R1)	: CLEAR ROMI
2079	013030	005237	001472		INC	KMNUM	: UPDATE DEVICE COUNTER
2080	013034	022737	000020	001472	CMP	#20,KMNUM	: ARE MAX. NO. OF DEV FOUND?
2081	013042	001410			BEQ	135	: YES DON'T LOOK FOR ANY MORE.
2082	013044	005011			CLR	(R1)	: CLEAR BIT 10
2083	013046	005061	000006		CLR	6(R1)	: CLEAR SEL 6
2084	013052	062701	000010		ADD	#10,R1	: UPDATE CSR POINTER ADDRESS
2085	013056	022701	164000		CMP	#164000,R1	
2086	013062	001230			BNE	25	: BR IF MORE ADDRESS TO CHECK.
2087	013064	005037	001470		CLR	KMACTV	
2088	013070	005737	001472		TST	KMNUM	: WERE ANY KMC11'S FOUND AT ALL?
2089	013074	001423			BEQ	55	: ERROR AUTO SIZER FOUND NO KMC11'S IN THIS SYS.
2090	013076	013701	001472		MOV	KMNUM,R1	
2091	013102	010137	001476		MOV	R1,SAVNUM	: SAVE NUMBER OF DEVICES
2092	013106	000241			CLC		
2093	013110	006137	001470		ROL	KMACTV	: GENERATE ACTIVE REGISTER OF DEVICES.
2094	013114	005237	001470		INC	KMACTV	: SET THE BIT
2095	013120	005301			DEC	R1	
2096	013122	001371			BNE	45	: BR IF MORE TO GENERATE
2097	013124	012737	000006	000004	MOV	#6,2#4	: RESTORE TRAP VECTOR
2098	013132	013737	001470	001474	MOV	KMACTV,SAVACT	: SAVE ACTIVE REGISTER
2099	013140	000137	013172		JMP	VECMAP	: GO FIND THE VECTOR NOW.
2100	013144	104401	007645		TYPE	MERR2	: NOTIFY OPR THAT NO KMC11'S FOUND.
2101	013150	005000			CLR	RO	: MAKE DATA LIGHTS ZERO
2102	013152	000000			HALT		: STOP THE SHOW

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2103 013154 000776          BR          -2          ;DISABLE CONT. SW.
2104 013156 012716 013052 6S:  MOV      #14$, (SP) ;ENTERED BY NON-EXISTANT TIME-OUT.
2105 013162 000002          RTI          ;RETURN TO MAINSTREAM
2106
2107 013164 000001          WHICH: 1
2108 013166      002      002      .BYTE      2,2
2109 013170 001306          STMP4
2110
2111 013172 032737 000001 001446 VECMAP: BIT      #SW00, STRTSW
2112 013200 001114          BNE      5$
2113 013202 012737 000340 000022  MOV      #340, 2#22 ;SET IOT TRAP PRIO TO 7
2114 013210 012737 013364 000020  MOV      #4$, 2#20 ;SET IOT TRAP VECTOR
2115 013216 012702 002100  MOV      #KM.MAP, R2 ;SET SOFTWARE POINTER
2116 013222 012700 000300  MOV      #300, R0 ;FLOATING VECTORS START HERE.
2117 013226 012701 000302  MOV      #302, R1 ;PC OF IOT INSTR.
2118 013232 010120 15:  MOV      R1, (R0)+ ;START FILLING VECTOR AREA
2119 013234 012721 000004  MOV      #4, (R1)+ ;WITH .+2; IOT
2120 013240 022021  CMP      (R0)+, (R1)+ ;ADD 2 TO R0 +R1
2121 013242 020127 001000  CMP      R1, #1000
2122 013246 101771 15:  BLOS     ;BR IF MORE TO FILL
2123 013250 013737 001470 001276  MOV      KMACTV, STMP0 ;STORE TEMPORALLY
2124 013256 006037 001276 25:  ROR      STMP0 ;BRING OUT A BIT
2125 013262 103063  BCC      5$ ;BR IF ALL DONE
2126 013264 012704 000012  MOV      #12, R4 ;R4 IS INDEX REGISTER
2127 013270 016437 013442 177776  MOV      BRLVL(R4), PS ;SET PS TO 7
2128 013276 011201  MOV      (R2), R1
2129 013300 012761 000200 000004  MOV      #200, 4(R1)
2130 013306 012711 001000  MOV      #BIT9, (R1) ;SET ROMI
2131 013312 012761 121111 000006  MOV      #121111, 6(R1) ;PUT INSTRUCTION IN PORT6
2132 013320 012711 001400  MOV      #BIT9:BIT8, (R1) ;FORCE AN INTERRUPT
2133 013324 105200 75:  INCB     RO ;STALL
2134 013326 001376  BNE      -2 ;FOR TIME TO INTERUPT
2135 013330 162704 000002  SUB      #2, R4 ;GET NEXT LOWEST PS LEVEL
2136 013334 001404  BEQ      6$ ;BR IF R4 = 0
2137 013336 016437 013442 177776  MOV      BRLVL(R4), PS ;MOVE NEXT LOWER LEVEL IN PS
2138 013344 000767  BR       7$ ;BR TO DELAY
2139 013346 052762 005300 000002 6S:  BIS      #5300, 2(R2) ;NO INTERUPT ASSUME 300 AT LEVEL 5 AND FIX KMC1! LATER
2140 013354 005011 35:  CLR      (R1) ;CLEAR ROMI
2141 013356 062702 000010  ADD      #10, R2 ;POP SOFTWARE POINTER
2142 013362 000735  BR       2$ ;KEEP GOING
2143 013364 051662 000002 45:  BIS      (SP), 2(R2) ;GET VECTOR ADDRESS
2144 013370 042762 000007 000002  BIC      #7, 2(R2) ;CLEAR JUNK
2145 013376 016405 013444  MOV      BRLVL+2(R4), R5 ;GET BR LEVEL OF KMC11
2146 013402 006305  ASL      R5 ;SHIFT LEVEL 4 PLACES
2147 013404 006305  ASL      R5 ;TO THE LEFT FOR THE
2148 013406 006305  ASL      R5 ;STATUS TABLE
2149 013410 006305  ASL      R5
2150 013412 042705 170777  BIC      #170777, R5 ;CLEAR UNWANTED BITS
2151 013416 050562 000002  BIS      R5, 2(R2) ;PUT BR LEVEL IN STATUS TABLE
2152 013422 022626  CMP      (SP)+, (SP)+ ;POP IOT JUNK OFF STACK
2153 013424 012716 013354  MOV      #3$, (SP) ;SET FOR RETURN
2154 013430 000002  RTI
2155 013432 012737 004134 000020 55:  MOV      #$$SCOPE, 2#20 ; RESTORE SCOPE VECTOR
2156 013440 000207  RTS      PC ;ALL DONE WITH "AUTO SIZING"
2157
2158 013442 000000  BRLVL:  PRO ;LEVEL 0

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2159 013444 000000          PRO      ;LEVEL 0
2160 013446 000200          PR4     ;LEVEL 4
2161 013450 000240          PR5     ;LEVEL 5
2162 013452 000300          PR6     ;LEVEL 6
2163 013454 000340          PR7     ;LEVEL 7
2164
2165
2166 013456 105777 165562    INTTY:  TSTB    2STKS      ;WAIT FOR DONE
2167 013462 100375          BPL     -4
2168 013464 017703 165556    MOV     2STKB,R3      ;PUT CHAR IN R3
2169 013470 105777 165554    TSTB    2STPS      ;WAIT UNTIL PRINTER IS READY
2170 013474 100375          BPL     -4
2171 013476 010377 165550    MOV     R3,2STPB     ;ECHO CHAR
2172 013502 042703 000240    BIC     #BIT7:BITS,R3 ;MASK OFF LOWER CASE
2173 013506 000207          RTS     PC           ;RETURN
2174
2175
2176 013510 000005          APT.SIZE:  RESET
2177 013512 010046          MOV     RD,-(SP)     ;: PUSH RD ON STACK
2178 013514 010146          MOV     R1,-(SP)     ;: PUSH R1 ON STACK
2179 013516 010246          MOV     R2,-(SP)     ;: PUSH R2 ON STACK
2180 013520 010346          MOV     R3,-(SP)     ;: PUSH R3 ON STACK
2181 013522 005037 013724    CLR     VECTR        ;: CLEAR THE LOCAL VARIABLE
2182 013526 005037 013730    CLR     PRIORITY     ;: CLEAN UP LOCAL VARIABLE
2183 013532 013700 001376    MOV     $CDW1,RD     ;: GET THE DEVICE COUNT
2184 013536 010037 001476    MOV     RD,SAVNUM    ;: SAVE THE NO. OF DEVICES
2185 013542 012701 001346    MOV     #SAMS1,R1    ;: GET EXTRA INFO, BITS POINTER
2186 013546 013737 001372 013726  MOV     $BASE,BASE   ;: GET BASE CSR ADDRESS
2187 013554 113737 001366 013724  MOVVB   $VECT1,VECTR ;: GET THE VECTOR
2188 013562 113737 001367 013730  MOVVB   $VECT1+1,PRIORITY ;: GET THE PRIORITY
2189 013570 013737 001374 001470  MOV     $DEVM,KMACTV ;: SAVE THE KMC'S SELECTED ACTIVE
2190 013576 013737 001470 001474  MOV     KMACTV,SAVACT ;: SAVE THE ACTIVE REGISTER
2191 013604 012702 001402          MOV     #SDW0,R2     ;: GET ADDRESS OF FIRST DEVICE DESCRIPTOR WORD
2192 013610 012703 002100          MOV     #KM.MAP,R3  ;: GET POINTER TO DEVICE MAP
2193 013614 005023          CLR     (R3)+        ;: CLEAR DEVICE MAP
2194 013616 022703 002300    3$:    CMP     #KM.END,R3  ;: IS WHOLE DEV.MAP CLEARED?
2195 013622 003374          BGT     3$          ;: NO, THEN GO ON.
2196 013624 012703 002100          MOV     #KM.MAP,R3  ;: RESTORE DEV.MAP POINTER.
2197 013630 013723 013726    1$:    MOV     BASE,(R3)+  ;: LOAD CSR ADDRESS
2198 013634 112163 000001          MOVVB   (R1)+,1(R3) ;: GET EXTRA INFO. BITS
2199 013640 006213          ASR     (R3)         ;: SET IT IN RIGHT POSITION.
2200 013642 006213          ASR     (R3)         ;: SET IT IN RIGHT POSITION.
2201 013644 053713 013730    BIS     PRIORITY,(R3) ;: GET PRIORITY IN STAT1
2202 013650 006313          ASL     (R3)         ;: SET THEM IN RIGHT POSITION
2203 013652 006313          ASL     (R3)         ;:
2204 013654 006313          ASL     (R3)         ;:
2205 013656 006313          ASL     (R3)         ;:
2206 013660 053723 013724    BIS     VECTR,(R3)+ ;: GET THE VECTOR IN STAT1.
2207 013664 012223          MOV     (R2)+,(R3)+ ;: GET THE STAT2 FROM DDWXX
2208 013666 005723          TST     (R3)+        ;: SKIP OVER STAT3
2209 013670 005300          DEC     RD           ;: COUNT BY 1
2210 013672 001407          BEQ     2$          ;: ALL DONE?
2211 013674 062737 000010 013726  ADD     #10,BASE     ;: INCREMENT BASE CSR ADDRESS BY 10
2212 013702 062737 000010 013724  ADD     #10,VECTR    ;: INCREMENT VECTOR ADDRESS BY 10
2213 013710 000747          BR      1$          ;: SET THE NEXT MAP ENTRY
2214 013712

```

2215 013712 012603
2216 013714 012602
2217 013716 012601
2218 013720 012600
2219 013722 000207
2220 013724 000000
2221 013726 000000
2222 013730 000000

MOV (SP)+,R3 ; POP STACK INTO R3
MOV (SP)+,R2 ; POP STACK INTO R2
MOV (SP)+,R1 ; POP STACK INTO R1
MOV (SP)+,R0 ; POP STACK INTO R0
RTS PC ; RETURN
VECTR: .WORD 0
BASE: .WORD 0
PRIRTY: .WORD 0

***** TEST 1 *****
;VERIFY THAT REFERENCING UNIBUS DEVICE REGISTERS
;DOES NOT CAUSE A TIME OUT TRAP

TEST 1

2232
2233 013732 000004
2234 013734 012737 000001 001202
2235 013742 012737 014042 001442
2236 013750 012737 014002 001444
2237
2238 013756 013701 002066
2239 013762 012700 000004
2240 013766 012737 014034 000004
2241 013774 012737 000340 000006
2242 014002 005711
2243 014004 000240
2244 014006 104405
2245 014010 062701 000002
2246 014014 005300
2247 014016 001371
2248 014020 012737 000006 000004
2249 014026 005037 000006
2250 014032 104420
2251 014034 011602
2252 014036 104001
2253 014040 000002
2254
2255
2256
2257
2258
2259
2260
2261
2262

TST1: SCOPE ;
MOV #1,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST2,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1\$,LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
MOV KMCSR,R1 ; R1 CONTAINS BASE KMC11 ADDRESS
MOV #4,R0 ; 4 REGISTERS TO BE TESTED
MOV #2\$,4 ; SET UP TIMEOUT TRAP
MOV #340,6 ; LEVEL 7
1\$: TST (R1) ; REFERENCE DEVICE REGISTER
NOP
SCOPI ; SW09=1?
ADD #2,R1 ; NEXT REGISTER
DEC R0 ; DEC REGISTER COUNT
BNE 1\$; BR IF NOT LAST REGISTER
MOV #6,4 ; RESTORE LOC 4
CLR 6 ; RESTORE LOC 6
ADVANCE ; ADVANCE TO NEXT TEST
2\$: MOV (SP),R2 ; GET PC OF TRAP
ERROR 1 ; TIME-OUT ERROR
RTI

***** TEST 2 *****
;VERIFY THAT RUN CAN BE CLEARED

TEST 2

2263 014042 000004 -
2264 014044 012737 000002 001202
2265 014052 012737 014072 001442
2266
2267 014060 005011
2268 014062 005005
2269 014064 011104
2270 014066 001401

TST2: SCOPE ;
MOV #2,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST3,NEXT ; POINT TO THE START OF NEXT TEST.
; R1 CONTAINS BASE KMC11 ADDRESS
CLR (R1) ; CLEAR KMCSR
CLR R5 ; CLEAR "EXPECTED"
MOV (R1),R4 ; PUT KMCSR IN "FOUND"
BEG 1\$; BR IF CLEARED

2271 014070 104002
2272 014072
2273
2274
2275
2276
2277
2278
2279
2280
2281
2282
2283
2284 014072 000004
2285 014074 012737 000003 001202
2286 014102 012737 014222 001442
2287 014110 012737 014124 001444
2288
2289 014116 104410
2290 014120 012700 000001
2291 014124 005011
2292 014126 010005
2293 014130 010011
2294 014132 011104
2295 014134 020504
2296 014136 001401
2297 014140 104002
2298 014142 104405
2299 014144 005721
2300 014146 005200
2301 014150 022700 000005
2302 014154 001363
2303 014156 013701 002066
2304 014162 012700 000001
2305 014166 012737 014174 001444
2306 014174 010005
2307 014176 011104
2308 014200 020504
2309 014202 001401
2310 014204 104002
2311 014206 104405
2312 014210 005721
2313 014212 005200
2314 014214 022700 000005
2315 014220 001365
2316
2317
2318
2319
2320
2321
2322
2323
2324
2325
2326

ERROR 2 ;ERROR KMCSR NOT CLEARED
1\$:

***** TEST 3 *****
:UNIBUS REGISTER WORD DUAL ADDRESSING TEST
:LOAD ALL REGISTERS WITH INCREMENTING PATTERN
:READ BACK ALL REGISTERS TO VERIFY CORRECT ADDRESSING
:*****

TEST 3

TST3: SCOPE ; LOAD THE NO. OF THIS TEST
MOV #3,STSTNM ; POINT TO THE START OF NEXT TEST.
MOV #TST4,NEXT ; ADDRESS FOR LOCK ON DATA.
MOV #1\$,LOCK ; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
1\$: MOV #1,R0 ; START PATTERN AT 1
CLR (R1) ; CLEAR REGISTER
MOV R0,R5 ; PUT DATA IN "EXPECTED"
MOV R0,(R1) ; WRITE KMC REGISTER WITH PATTERN
MOV (R1),R4 ; READ KMC REGISTER INTO "FOUND"
CMP R5,R4 ; IS DATA CORRECT
BEQ 2\$; BR IF YES
2\$: ERROR 2 ; DATA ERROR
SCOPI ; SW09=1?
TST (R1)+ ; NEXT REGISTER
INC R0 ; INCREMENT DATA PATTERN
CMP #5,R0 ; LAST REGISTER?
BNE 1\$; BR IF NO
MOV KMCSR,R1 ; BASE KMC11 ADDRESS TO R1
MOV #1,R0 ; RESTART PATTERN AT 1
MOV #3\$,LOCK ; NEW SCOPI
3\$: MOV R0,R5 ; PUT DATA IN "EXPECTED"
MOV (R1),R4 ; READ KMC REGISTER INTO "FOUND"
CMP R5,R4 ; IS DATA CORRECT
BEQ 4\$; BR IF YES
4\$: ERROR 2 ; DUAL ADDRESSING ERROR
SCOPI ; SW09=1?
TST (R1)+ ; NEXT REGISTER
INC R0 ; INCREMENT PATTERN
CMP #5,R0 ; LAST REGISTER?
BNE 3\$; BR IF NO

***** TEST 4 *****
:CONTROL STATUS REGISTER WRITE/READ TEST
:SET BIT0, VERIFY BIT0 WAS SET
:CLEAR BIT0, VERIFY BIT0 WAS CLEARED
:*****

TEST 4

KMC11 UNIBUS REGISTER TESTS

```

2327 014222 000004
2328 014224 012737 000004 001202
2329 014232 012737 014320 001442
2330 014240 012737 014250 001444
2331 014246 104410
2332 014250 013701 002066
2333 014254 012705 000001
2334 014260 010511
2335 014262 011104
2336 014264 020504
2337 014266 001401
2338 014270 104002
2339 014272 104405
2340 014274 012737 014302 001444
2341 014302 042711 000001
2342 014306 005005
2343 014310 011104
2344 014312 001402
2345 014314 104002
2346 014316 104405
2347 014320
2348
2349
2350
2351
2352
2353
2354
2355
2356
2357
2358
2359 014320 000004
2360 014322 012737 000005 001202
2361 014330 012737 014416 001442
2362 014336 012737 014346 001444
2363 014344 104410
2364 014346 013701 002066
2365 014352 012705 000002
2366 014356 010511
2367 014360 011104
2368 014362 020504
2369 014364 001401
2370 014366 104002
2371 014370 104405
2372 014372 012737 014400 001444
2373 014400 042711 000002
2374 014404 005005
2375 014406 011104
2376 014410 001402
2377 014412 104002
2378 014414 104405
2379 014416
2380
2381
2382

```

```

TST4: SCOPE
MOV #4, $TSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST5, NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1$, LOCK ; ADDRESS FOR LOCK ON DATA.
MSTCLR ; MASTER CLEAR KMC11
1$: MOV KMCSR, R1 ; PUT REGISTER ADDRESS IN R1
MOV #BIT0, R5 ; PUT DATA IN "EXPECTED"
MOV R5, (R1) ; WRITE BIT 0
MOV (R1), R4 ; READ CONTROL STATUS REGISTER
CMP R5, R4 ; IS DATA CORRECT
BEQ 2$ ; BR IF YES
ERROR 2 ; DATA ERROR
2$: SCOP1 ; SW09 UP?
MOV #3$, LOCK ; NEW SCOP1
BIC #BIT0, (R1) ; CLEAR BIT 0
CLR R5 ; CLEAR "EXPECTED"
MOV (R1), R4 ; READ CONTROL STATUS REGISTER
BEQ 4$ ; BR IF ZERO
ERROR 2 ; DATA ERROR BIT0 NOT CLEARED
4$: SCOP1 ; SW09 UP?

```

```

***** TEST 5 *****
*CONTROL STATUS REGISTER WRITE/READ TEST
*SET BIT1, VERIFY BIT1 WAS SET
*CLEAR BIT1, VERIFY BIT1 WAS CLEARED
*****

```

TEST 5

```

*****
TST5: SCOPE
MOV #5, $TSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST6, NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1$, LOCK ; ADDRESS FOR LOCK ON DATA.
MSTCLR ; MASTER CLEAR KMC11
1$: MOV KMCSR, R1 ; PUT REGISTER ADDRESS IN R1
MOV #BIT1, R5 ; PUT DATA IN "EXPECTED"
MOV R5, (R1) ; WRITE BIT 1
MOV (R1), R4 ; READ CONTROL STATUS REGISTER
CMP R5, R4 ; IS DATA CORRECT
BEQ 2$ ; BR IF YES
ERROR 2 ; DATA ERROR
2$: SCOP1 ; SW09 UP?
MOV #3$, LOCK ; NEW SCOP1
BIC #BIT1, (R1) ; CLEAR BIT 1
CLR R5 ; CLEAR "EXPECTED"
MOV (R1), R4 ; READ CONTROL STATUS REGISTER
BEQ 4$ ; BR IF ZERO
ERROR 2 ; DATA ERROR BIT1 NOT CLEARED
4$: SCOP1 ; SW09 UP?

```

```

***** TEST 6 *****

```

KMC11 UNIBUS REGISTER TESTS

```

2383 ;*CONTROL STATUS REGISTER WRITE/READ TEST
2384 ;*SET BIT2, VERIFY BIT2 WAS SET
2385 ;*CLEAR BIT2, VERIFY BIT2 WAS CLEARED
2386 ;*****
2387
2388 ; TEST 6
2389 ;-----
2390 ;*****

```

```

2391 014416 000004 000006 001202 1$T6: SCOPE
2392 014420 012737 000006 001202 MOV #6,$STSTNM ; LOAD THE NO. OF THIS TEST
2393 014426 012737 014514 001442 MOV #TST7,NEXT ; POINT TO THE START OF NEXT TEST.
2394 014434 012737 014444 001444 MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
2395 014442 104410 MSTCLR ; MASTER CLEAR KMC11
2396 014444 013701 002066 1$: MOV KMCSR,R1 ; PUT REGISTER ADDRESS IN R1
2397 014450 012705 000004 MOV #BIT2,R5 ; PUT DATA IN "EXPECTED"
2398 014454 010511 MOV R5,(R1) ; WRITE BIT 2
2399 014456 011104 MOV (R1),R4 ; READ CONTROL STATUS REGISTER
2400 014460 020504 CMP R5,R4 ; IS DATA CORRECT
2401 014462 001401 BEQ 2$ ; BR IF YES
2402 014464 104002 ERROR 2 ; DATA ERROR
2403 014466 104405 2$: SCOPI ; SW09 UP?
2404 014470 012737 014476 001444 3$: MOV #3$,LOCK ; NEW SCOPI
2405 014476 042711 000004 BIC #BIT2,(R1) ; CLEAR BIT 2
2406 014502 005005 CLR R5 ; CLEAR "EXPECTED"
2407 014504 011104 MOV (R1),R4 ; READ CONTROL STATUS REGISTER
2408 014506 001402 BEQ 4$ ; BR IF ZERO
2409 014510 104002 ERROR 2 ; DATA ERROR BIT2 NOT CLEARED
2410 014512 104405 4$: SCOPI ; SW09 UP?
2411 014514
2412
2413
2414
2415 ;***** TEST 7 *****
2416 ;*CONTROL STATUS REGISTER WRITE/READ TEST
2417 ;*SET BITS, VERIFY BITS WAS SET
2418 ;*CLEAR BITS, VERIFY BITS WAS CLEARED
2419 ;*****
2420 ; TEST 7
2421 ;-----
2422 ;*****

```

```

2423 014514 000004 000007 001202 1$T7: SCOPE
2424 014516 012737 000007 001202 MOV #7,$STSTNM ; LOAD THE NO. OF THIS TEST
2425 014524 012737 014612 001442 MOV #TST10,NEXT ; POINT TO THE START OF NEXT TEST.
2426 014532 012737 014542 001444 MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
2427 014540 104410 MSTCLR ; MASTER CLEAR KMC11
2428 014542 013701 002066 1$: MOV KMCSR,R1 ; PUT REGISTER ADDRESS IN R1
2429 014546 012705 000040 MOV #BIT5,R5 ; PUT DATA IN "EXPECTED"
2430 014552 010511 MOV R5,(R1) ; WRITE BIT 5
2431 014554 011104 MOV (R1),R4 ; READ CONTROL STATUS REGISTER
2432 014556 020504 CMP R5,R4 ; IS DATA CORRECT
2433 014560 001401 BEQ 2$ ; BR IF YES
2434 014562 104002 ERROR 2 ; DATA ERROR
2435 014564 104405 2$: SCOPI ; SW09 UP?
2436 014566 012737 014574 001444 3$: MOV #3$,LOCK ; NEW SCOPI
2437 014574 042711 000040 BIC #BIT5,(R1) ; CLEAR BIT 5
2438 014600 005005 CLR R5 ; CLEAR "EXPECTED"

```

2439 014602 011104
2440 014604 001402
2441 014606 104002
2442 014610 104405
2443 014612

MOV (R1),R4 ;READ CONTROL STATUS REGISTER
BEQ 4\$;BR IF ZERO
ERROR 2 ;DATA ERROR BITS NOT CLEARED
SCOPI ;SW09 UP?
4\$:

***** TEST 10 *****
*CONTROL STATUS REGISTER WRITE/READ TEST
*SET BIT6, VERIFY BIT6 WAS SET
*CLEAR BIT6, VERIFY BIT6 WAS CLEARED

TEST 10

2451
2452
2453
2454
2455
2456 014612 000004
2457 014614 012737 000010 001202
2458 014622 012737 014710 001442
2459 014630 012737 014640 001444
2460 014636 104410
2461 014640 013701 002066
2462 014644 012705 000100
2463 014650 010511
2464 014652 011104
2465 014654 020504
2466 014656 001401
2467 014660 104002
2468 014662 104405
2469 014664 012737 014672 001444
2470 014672 042711 000100
2471 014676 005005
2472 014700 011104
2473 014702 001402
2474 014704 104002
2475 014706 104405
2476 014710

†ST10: SCOPE ;
MOV #10,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST11,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1\$,LOCK ; ADDRESS FOR LOCK ON DATA.
MSTCLR ;MASTER CLEAR KMC11
1\$: MOV KMCSR,R1 ;PUT REGISTER ADDRESS IN R1
MOV #BIT6,R5 ;PUT DATA IN "EXPECTED"
MOV R5,(R1) ;WRITE BIT 6
MOV (R1),R4 ;READ CONTROL STATUS REGISTER
CMP R5,R4 ;IS DATA CORRECT
BEQ 2\$;BR IF YES
ERROR 2 ;DATA ERROR
SCOPI ;SW09 UP?
2\$: MOV #3\$,LOCK ;NEW SCOPI
3\$: BIC #BIT6,(R1) ;CLEAR BIT 6
CLR R5 ;CLEAR "EXPECTED"
MOV (R1),R4 ;READ CONTROL STATUS REGISTER
BEQ 4\$;BR IF ZERO
ERROR 2 ;DATA ERROR BIT6 NOT CLEARED
SCOPI ;SW09 UP?
4\$:

***** TEST 11 *****
*CONTROL STATUS REGISTER WRITE/READ TEST
*SET BIT7, VERIFY BIT7 WAS SET
*CLEAR BIT7, VERIFY BIT7 WAS CLEARED

TEST 11

2487 014710 000004
2488 014712 012737 000011 001202
2489 014720 012737 015006 001442
2490 014726 012737 014736 001444
2491 014734 104410
2492 014736 013701 002066
2493 014742 012705 000200
2494 014746 010511

†ST11: SCOPE ;
MOV #11,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST12,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1\$,LOCK ; ADDRESS FOR LOCK ON DATA.
MSTCLR ;MASTER CLEAR KMC11
1\$: MOV KMCSR,R1 ;PUT REGISTER ADDRESS IN R1
MOV #BIT7,R5 ;PUT DATA IN "EXPECTED"
MOV R5,(R1) ;WRITE BIT 7

KMC11 UNIBUS REGISTER TESTS

```

2495 014750 011104      MOV      (R1),R4      ;READ CONTROL STATUS REGISTER
2496 014752 020504      CMP      R5,R4       ;IS DATA CORRECT
2497 014754 001401      BEQ      2$          ;BR IF YES
2498 014756 104002      ERROR   2           ;DATA ERROR
2499 014760 104405      SCOPI   ;SW09 UP?
2500 014762 012737 014770 001444 2$:  MOV      #3$,LOCK    ;NEW SCOPI
2501 014770 042711 000200 3$:  BIC      #BIT7,(R1)  ;CLEAR BIT 7
2502 014774 005005      CLR      R5         ;CLEAR "EXPECTED"
2503 014776 011104      MOV      (R1),R4    ;READ CONTROL STATUS REGISTER
2504 015000 001402      BEQ      4$          ;BR IF ZERO
2505 015002 104002      ERROR   2           ;DATA ERROR BIT7 NOT CLEARED
2506 015004 104405      SCOPI   ;SW09 UP?
2507 015006

```

```

;***** TEST 12 *****
;CONTROL STATUS REGISTER WRITE/READ TEST
;SET BIT9, VERIFY BIT9 WAS SET
;CLEAR BIT9, VERIFY BIT9 WAS CLEARED
;*****

```

TEST 12

```

2518 015006 000004      TST12: SCOPE
2519 015010 012737 000012 001202  MOV      #12,$TSTNM ; LOAD THE NO. OF THIS TEST
2520 015016 012737 015104 001442  MOV      #TST13,NEXT ; POINT TO THE START OF NEXT TEST.
2521 015024 012737 015034 001444  MOV      #1$,LOCK   ; ADDRESS FOR LOCK ON DATA.
2522 015032 104410      MSTCLR ;MASTER CLEAR KMC11
2523 015034 013701 002066 1$:  MOV      KMCSR,R1   ;PUT REGISTER ADDRESS IN R1
2524 015040 012705 001000  MOV      #BIT9,R5   ;PUT DATA IN "EXPECTED"
2525 015044 010511      MOV      R5,(R1)   ;WRITE BIT 9
2526 015046 011104      MOV      (R1),R4   ;READ CONTROL STATUS REGISTER
2527 015050 020504      CMP      R5,R4     ;IS DATA CORRECT
2528 015052 001401      BEQ      2$          ;BR IF YES
2529 015054 104002      ERROR   2           ;DATA ERROR
2530 015056 104405      SCOPI   ;SW09 UP?
2531 015060 012737 015066 001444 2$:  MOV      #3$,LOCK    ;NEW SCOPI
2532 015066 042711 001000 3$:  BIC      #BIT9,(R1) ;CLEAR BIT 9
2533 015072 005005      CLR      R5         ;CLEAR "EXPECTED"
2534 015074 011104      MOV      (R1),R4    ;READ CONTROL STATUS REGISTER
2535 015076 001402      BEQ      4$          ;BR IF ZERO
2536 015100 104002      ERROR   2           ;DATA ERROR BIT9 NOT CLEARED
2537 015102 104405      SCOPI   ;SW09 UP?
2538 015104

```

```

;***** TEST 13 *****
;CONTROL STATUS REGISTER WRITE/READ TEST
;SET BIT11, VERIFY BIT11 WAS SET
;CLEAR BIT11, VERIFY BIT11 WAS CLEARED
;*****

```

TEST 13

```

2540
2541
2542
2543
2544
2545
2546
2547
2548
2549
2550
;*****

```

KMC11 UNIBUS REGISTER TESTS

```

2551 015104 000004 TST13: SCOPE
2552 015106 012737 000013 001202 MOV #13,$STSTNM ; LOAD THE NO. OF THIS TEST
2553 015114 012737 015202 001442 MOV #TST14,NEXT ; POINT TO THE START OF NEXT TEST.
2554 015122 012737 015132 001444 MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
2555 015130 104410 MSTCLR ; MASTER CLEAR KMC11
2556 015132 013701 002066 1$: MOV KMCSR,R1 ; PUT REGISTER ADDRESS IN R1
2557 015138 012705 004000 MOV #BIT11,R5 ; PUT DATA IN "EXPECTED"
2558 015142 010511 MOV R5,(R1) ; WRITE BIT 11
2559 015144 011104 MOV (R1),R4 ; READ CONTROL STATUS REGISTER
2560 015146 020504 CMP R5,R4 ; IS DATA CORRECT
2561 015150 001401 BEQ 2$ ; BR IF YES
2562 015152 104002 ERROR 2 ; DATA ERROR
2563 015154 104405 2$: SCOPI ; SW09 UP?
2564 015156 012737 015164 001444 MOV #3$,LOCK ; NEW SCOPI
2565 015164 042711 004000 3$: BIC #BIT11,(R1) ; CLEAR BIT 11
2566 015170 005005 CLR R5 ; CLEAR "EXPECTED"
2567 015172 011104 MOV (R1),R4 ; READ CONTROL STATUS REGISTER
2568 015174 001402 BEQ 4$ ; BR IF ZERO
2569 015176 104002 ERROR 2 ; DATA ERROR BIT11 NOT CLEARED
2570 015200 104405 SCOPI ; SW09 UP?
2571 015202 4$:

```

```

;***** TEST 14 *****
;CONTROL STATUS REGISTER WRITE/READ TEST
;SET BIT12, VERIFY BIT12 WAS SET
;CLEAR BIT12, VERIFY BIT12 WAS CLEARED
;*****

```

TEST 14

```

2582 ;*****
2583 015202 000004 TST14: SCOPE
2584 015204 012737 000014 001202 MOV #14,$STSTNM ; LOAD THE NO. OF THIS TEST
2585 015212 012737 015300 001442 MOV #TST15,NEXT ; POINT TO THE START OF NEXT TEST.
2586 015220 012737 015230 001444 MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
2587 015226 104410 MSTCLR ; MASTER CLEAR KMC11
2588 015230 013701 002066 1$: MOV KMCSR,R1 ; PUT REGISTER ADDRESS IN R1
2589 015234 012705 010000 MOV #BIT12,R5 ; PUT DATA IN "EXPECTED"
2590 015240 010511 MOV R5,(R1) ; WRITE BIT 12
2591 015242 011104 MOV (R1),R4 ; READ CONTROL STATUS REGISTER
2592 015244 020504 CMP R5,R4 ; IS DATA CORRECT
2593 015246 001401 BEQ 2$ ; BR IF YES
2594 015250 104002 ERROR 2 ; DATA ERROR
2595 015252 104405 2$: SCOPI ; SW09 UP?
2596 015254 012737 015262 001444 MOV #3$,LOCK ; NEW SCOPI
2597 015262 042711 010000 3$: BIC #BIT12,(R1) ; CLEAR BIT 12
2598 015266 005005 CLR R5 ; CLEAR "EXPECTED"
2599 015270 011104 MOV (R1),R4 ; READ CONTROL STATUS REGISTER
2600 015272 001402 BEQ 4$ ; BR IF ZERO
2601 015274 104002 ERROR 2 ; DATA ERROR BIT12 NOT CLEARED
2602 015276 104405 SCOPI ; SW09 UP?
2603 015300 4$:

```

```

;***** TEST 15 *****

```

KMC11 UNIBUS REGISTER TESTS

```

2607
2608
2609
2610
2611
2612
2613
2614
2615 015300 000004
2616 015302 012737 000015 001202
2617 015310 012737 015376 001442
2618 015316 012737 015326 001444
2619 015324 104410
2620 015326 013701 002072
2621 015332 012705 000001
2622 015336 010511
2623 015340 011104
2624 015342 020504
2625 015344 001401
2626 015346 104002
2627 015350 104405
2628 015352 012737 015360 001444
2629 015360 042711 000001
2630 015364 005005
2631 015366 011104
2632 015370 001402
2633 015372 104002
2634 015374 104405
2635 015376
2636
2637
2638
2639
2640
2641
2642
2643
2644
2645
2646
2647 015376 000004
2648 015400 012737 000016 001202
2649 015406 012737 015474 001442
2650 015414 012737 015424 001444
2651 015422 104410
2652 015424 013701 002072
2653 015430 012705 000002
2654 015434 010511
2655 015436 011104
2656 015440 020504
2657 015442 001401
2658 015444 104002
2659 015446 104405
2660 015450 012737 015456 001444
2661 015456 042711 000002
2662 015462 005005

```

```

:CONTROL OUT REGISTER WRITE/READ TEST
:SET BIT0, VERIFY BIT0 WAS SET
:CLEAR BIT0, VERIFY BIT0 WAS CLEARED
:*****

```

TEST 15

```

:*****
TST15: SCOPE
MOV #15,$STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST16,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
MSTCLR ; MASTER CLEAR KMC11
1$: MOV KMCTL,R1 ; PUT REGISTER ADDRESS IN R1
MOV #BIT0,R5 ; PUT DATA IN "EXPECTED"
MOV R5,(R1) ; WRITE BIT 0
MOV (R1),R4 ; READ CONTROL OUT REGISTER
CMP R5,R4 ; IS DATA CORRECT
BEQ 2$ ; BR IF YES
ERROR 2 ; DATA ERROR
2$: SCOP1 ; SW09 UP?
MOV #3$,LOCK ; NEW SCOP1
3$: BIC #BIT0,(R1) ; CLEAR BIT 0
CLR R5 ; CLEAR "EXPECTED"
MOV (R1),R4 ; READ CONTROL OUT REGISTER
BEQ 4$ ; BR IF ZERO
ERROR 2 ; DATA ERROR BIT0 NOT CLEARED
4$: SCOP1 ; SW09 UP?

```

```

:***** TEST 16 *****
:CONTROL OUT REGISTER WRITE/READ TEST
:SET BIT1, VERIFY BIT1 WAS SET
:CLEAR BIT1, VERIFY BIT1 WAS CLEARED
:*****

```

TEST 16

```

:*****
TST16: SCOPE
MOV #16,$STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST17,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
MSTCLR ; MASTER CLEAR KMC11
1$: MOV KMCTL,R1 ; PUT REGISTER ADDRESS IN R1
MOV #BIT1,R5 ; PUT DATA IN "EXPECTED"
MOV R5,(R1) ; WRITE BIT 1
MOV (R1),R4 ; READ CONTROL OUT REGISTER
CMP R5,R4 ; IS DATA CORRECT
BEQ 2$ ; BR IF YES
ERROR 2 ; DATA ERROR
2$: SCOP1 ; SW09 UP?
MOV #3$,LOCK ; NEW SCOP1
3$: BIC #BIT1,(R1) ; CLEAR BIT 1
CLR R5 ; CLEAR "EXPECTED"

```

KMC11 UNIBUS REGISTER TESTS

2663 015464 011104
2664 015466 001402
2665 015470 104002
2666 015472 104405
2667 015474

45: MOV (R1),R4 ; READ CONTROL OUT REGISTER
BEQ 45 ; BR IF ZERO
ERROR 2 ; DATA ERROR BIT1 NOT CLEARED
SCOPI ; SW09 UP?

***** TEST 17 *****
*CONTROL OUT REGISTER WRITE/READ TEST
*SET BIT2, VERIFY BIT2 WAS SET
*CLEAR BIT2, VERIFY BIT2 WAS CLEARED

TEST 17

2678
2679 015474 000004
2680 015476 012737 000017 001202
2681 015504 012737 015572 001442
2682 015512 012737 015522 001444
2683 015520 104410
2684 015522 013701 002072
2685 015526 012705 000004
2686 015532 010511
2687 015534 011104
2688 015536 020504
2689 015540 001401
2690 015542 104002
2691 015544 104405
2692 015546 012737 015554 001444
2693 015554 042711 000004
2694 015560 005005
2695 015562 011104
2696 015564 001402
2697 015566 104002
2698 015570 104405
2699 015572

15: SCOPE ; *****
↑ST17: MOV #17,\$STNM ; LOAD THE NO. OF THIS TEST
MOV #↑ST20,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #15,LOCK ; ADDRESS FOR LOCK ON DATA.
MSTCLR ; MASTER CLEAR KMC11
15: MOV KMCTL,R1 ; PUT REGISTER ADDRESS IN R1
MOV #BIT2,R5 ; PUT DATA IN "EXPECTED"
MOV R5,(R1) ; WRITE BIT 2
MOV (R1),R4 ; READ CONTROL OUT REGISTER
CMP R5,R4 ; IS DATA CORRECT
BEQ 25 ; BR IF YES
ERROR 2 ; DATA ERROR
SCOPI ; SW09 UP?
25: MOV #35,LOCK ; NEW SCOPI
35: BIC #BIT2,(R1) ; CLEAR BIT 2
CLR R5 ; CLEAR "EXPECTED"
MOV (R1),R4 ; READ CONTROL OUT REGISTER
BEQ 45 ; BR IF ZERO
ERROR 2 ; DATA ERROR BIT2 NOT CLEARED
SCOPI ; SW09 UP?
45:

***** TEST 20 *****
*CONTROL OUT REGISTER WRITE/READ TEST
*SET BIT6, VERIFY BIT6 WAS SET
*CLEAR BIT6, VERIFY BIT6 WAS CLEARED

TEST 20

2708
2709
2710
2711 015572 000004
2712 015574 012737 000020 001202
2713 015602 012737 015670 001442
2714 015610 012737 015620 001444
2715 015616 104410
2716 015620 013701 002072
2717 015624 012705 000100
2718 015630 010511

15: SCOPE ; *****
↑ST20: MOV #20,\$STNM ; LOAD THE NO. OF THIS TEST
MOV #↑ST21,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #15,LOCK ; ADDRESS FOR LOCK ON DATA.
MSTCLR ; MASTER CLEAR KMC11
15: MOV KMCTL,R1 ; PUT REGISTER ADDRESS IN R1
MOV #BIT6,R5 ; PUT DATA IN "EXPECTED"
MOV R5,(R1) ; WRITE BIT 6

KMC11 UNIBUS REGISTER TESTS

```

2719 015632 011104      MOV      (R1),R4      ;READ CONTROL OUT REGISTER
2720 015634 020504      CMP      R5,R4      ;IS DATA CORRECT
2721 015636 001401      BEQ      2$          ;BR IF YES
2722 015640 104002      ERROR   2           ;DATA ERROR
2723 015642 104405      SCOPI   ;SW09 UP?
2724 015644 012737      MOV      #3$,LOCK    ;NEW SCOPI
2725 015652 042711      BIC      #BIT6,(R1)  ;CLEAR BIT 6
015652 000100      CLR     R5           ;CLEAR "EXPECTED"
2726 015656 005005      MOV      (R1),R4    ;READ CONTROL OUT REGISTER
2727 015660 011104      BEQ      4$          ;BR IF ZERO
2728 015662 001402      ERROR   2           ;DATA ERROR BIT6 NOT CLEARED
2729 015664 104002      SCOPI   ;SW09 UP?
2730 015666 104405
2731 015670

```

```

***** TEST 21 *****
*CONTROL OUT REGISTER WRITE/READ TEST
*SET BIT7, VERIFY BIT7 WAS SET
*CLEAR BIT7, VERIFY BIT7 WAS CLEARED
*****

```

TEST 21

```

2742
2743 015670 000004      ;*****
2744 015672 012737      TST21: SCOPE
2745 015700 012737      MOV      #21,$STSTM  ; LOAD THE NO. OF THIS TEST
2746 015706 012737      MOV      #TST22,NEXT ; POINT TO THE START OF NEXT TEST.
2747 015714 104410      MOV      #1$,LOCK   ; ADDRESS FOR LOCK ON DATA.
2748 015716 013701      MSTCLR  ;MASTER CLEAR KMC11
2749 015722 012705      MOV      KMCTL,R1   ;PUT REGISTER ADDRESS IN R1
000200      MOV      #BIT7,R5  ;PUT DATA IN "EXPECTED"
2750 015726 010511      MOV      R5,(R1)   ;WRITE BIT 7
2751 015730 011104      MOV      (R1),R4   ;READ CONTROL OUT REGISTER
2752 015732 020504      CMP      R5,R4     ;IS DATA CORRECT
2753 015734 001401      BEQ      2$        ;BR IF YES
2754 015736 104002      ERROR   2         ;DATA ERROR
2755 015740 104405      SCOPI   ;SW09 UP?
2756 015742 012737      MOV      #3$,LOCK  ;NEW SCOPI
2757 015750 042711      BIC      #BIT7,(R1) ;CLEAR BIT 7
000200      CLR     R5         ;CLEAR "EXPECTED"
2758 015754 005005      MOV      (R1),R4  ;READ CONTROL OUT REGISTER
2759 015756 011104      BEQ      4$        ;BR IF ZERO
2760 015760 001402      ERROR   2         ;DATA ERROR BIT7 NOT CLEARED
2761 015762 104002      SCOPI   ;SW09 UP?
2762 015764 104405
2763 015766

```

```

***** TEST 22 *****
*CONTROL OUT REGISTER WRITE/READ TEST
*SET BIT12, VERIFY BIT12 WAS SET
*CLEAR BIT12, VERIFY BIT12 WAS CLEARED
*****

```

TEST 22

```

2771
2772
2773
2774
;*****

```

```

2775 015766 000004          TST22: SCOPE
2776 015770 012737 000022 001202  MOV      #22,$STSTNM      ; LOAD THE NO. OF THIS TEST
2777 015776 012737 016064 001442  MOV      #TST23,NEXT     ; POINT TO THE START OF NEXT TEST.
2778 016004 012737 016014 001444  MOV      #1$,LOCK        ; ADDRESS FOR LOCK ON DATA.
2779 016012 104410          MSTCLR
2780 016014 013701 002072          1$:  MOV      KMCTL,R1        ; MASTER CLEAR KMC11
2781 016020 012705 010000          MOV      #BIT12,R5       ; PUT REGISTER ADDRESS IN R1
2782 016024 010511          MOV      R5,(R1)         ; PUT DATA IN "EXPECTED"
2783 016026 011104          MOV      (R1),R4         ; WRITE BIT 12
2784 016030 020504          MOV      (R1),R4         ; READ CONTROL OUT REGISTER
2785 016032 001401          CMP      R5,R4           ; IS DATA CORRECT
2786 016034 104002          BEQ      2$              ; BR IF YES
2787 016036 104405          ERROR   2               ; DATA ERROR
2788 016040 012737 016046 001444          2$:  SCOP1
2789 016046 042711 010000          MOV      #3$,LOCK        ; NEW SCOP1
2790 016052 005005          3$:  BIC      #BIT12,(R1)    ; CLEAR BIT 12
2791 016054 011104          CLR      R5              ; CLEAR "EXPECTED"
2792 016056 001402          MOV      (R1),R4         ; READ CONTROL OUT REGISTER
2793 016060 104002          BEQ      4$              ; BR IF ZERO
2794 016062 104405          ERROR   2               ; DATA ERROR BIT12 NOT CLEARED
2795 016064          SCOP1                    ; SW09 UP?

```

```

2796
2797
2798
2799
2800
2801
2802
2803
2804
2805
2806
2807
2808
2809
2810
2811
2812
2813
2814
2815
2816
2817
2818
2819
2820
2821
2822
2823
2824
2825
2826
2827
2828
2829
2830

```

```

;***** TEST 23 *****
;CONTROL OUT REGISTER WRITE/READ TEST
;SET BIT13, VERIFY BIT13 WAS SET
;CLEAR BIT13, VERIFY BIT13 WAS CLEARED
;*****

```

TEST 23

```

2807 016064 000004          TST23: SCOPE
2808 016066 012737 000023 001202  MOV      #23,$STSTNM     ; LOAD THE NO. OF THIS TEST
2809 016074 012737 016162 001442  MOV      #TST24,NEXT     ; POINT TO THE START OF NEXT TEST.
2810 016102 012737 016112 001444  MOV      #1$,LOCK        ; ADDRESS FOR LOCK ON DATA.
2811 016110 104410          MSTCLR
2812 016112 013701 002072          1$:  MOV      KMCTL,R1        ; MASTER CLEAR KMC11
2813 016116 012705 020000          MOV      #BIT13,R5       ; PUT REGISTER ADDRESS IN R1
2814 016122 010511          MOV      R5,(R1)         ; PUT DATA IN "EXPECTED"
2815 016124 011104          MOV      (R1),R4         ; WRITE BIT 13
2816 016126 020504          MOV      (R1),R4         ; READ CONTROL OUT REGISTER
2817 016130 001401          CMP      R5,R4           ; IS DATA CORRECT
2818 016132 104002          BEQ      2$              ; BR IF YES
2819 016134 104405          ERROR   2               ; DATA ERROR
2820 016136 012737 016144 001444          2$:  SCOP1
2821 016144 042711 020000          MOV      #3$,LOCK        ; NEW SCOP1
2822 016150 005005          3$:  BIC      #BIT13,(R1)    ; CLEAR BIT 13
2823 016152 011104          CLR      R5              ; CLEAR "EXPECTED"
2824 016154 001402          MOV      (R1),R4         ; READ CONTROL OUT REGISTER
2825 016156 104002          BEQ      4$              ; BR IF ZERO
2826 016160 104405          ERROR   2               ; DATA ERROR BIT13 NOT CLEARED
2827 016162          SCOP1                    ; SW09 UP?

```

```

;***** TEST 24 *****

```

```

2831
2832
2833
2834
2835
2836
2837
2838
2839 016162 000004
2840 016164 012737 000024 001202
2841 016172 012737 016306 001442
2842 016200 012737 016220 001444
2843 016206 104410
2844 016210 013701 002074
2845 016214 012700 000001
2846 016220
2847 016220 010005
2848 016222 010511
2849 016224 011104
2850 016226 020504
2851 016230 001401
2852 016232 104002
2853 016234 104405
2854 016236 000241
2855 016240 006100
2856 016242 001366
2857 016244 012737 016256 001444
2858 016252 012700 000001
2859 016256
2860 016256 005100
2861 016260 010005
2862 016262 010511
2863 016264 011104
2864 016266 020504
2865 016270 001401
2866 016272 104002
2867 016274 104405
2868 016276 005100
2869 016300 000241
2870 016302 006100
2871 016304 001364

```

```

; *PORT4 REGISTER WRITE/READ TEST
; *FLOAT A ONE THROUGH PORT4 REGISTER
; *FLOAT A ZERO THROUGH PORT4 REGISTER
; *****

```

TEST 24

```

; *****
†ST24: SCOPE
MOV #24,$STSTNM ; LOAD THE NO. OF THIS TEST
MOV #†ST25,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #64$,$LOCK ; ADDRESS FOR LOCK ON DATA.
MSTCLR ; MASTER CLEAR KMC11
MOV KMP04,R1 ; PUT REGISTER ADDRESS IN R1
MOV #1,R0 ; START WITH BIT0

64$: MOV R0,R5 ; PUT "EXPECTED" IN R5
MOV R5,(R1) ; WRITE PORT4 REGISTER
MOV (R1),R4 ; READ PORT4 REGISTER
CMP R5,R4 ; COMPARE EXPECTED AND FOUND
BEQ 65$ ; BR IF OK
ERROR 2 ; WRITE/READ ERROR
65$: SCOP1 ; LOOP TO 64$ IF SW09=1
CLC ; CLEAR CARRY
ROL R0 ; SHIFT TO NEXT BIT
BNE 64$ ; BR IF NOT DONE YET?
MOV #66$,$LOCK ; NEW SCOP1
MOV #1,R0 ; START WITH BIT0

66$: COM R0 ; CHANGE TO A FLOATING ZERO
MOV R0,R5 ; PUT "EXPECTED" IN R5
MOV R5,(R1) ; WRITE PORT4 REGISTER
MOV (R1),R4 ; READ PORT4 REGISTER
CMP R5,R4 ; COMPARE EXPECTED AND FOUND
BEQ 67$ ; BR IF OK
ERROR 2 ; WRITE/READ ERROR
67$: SCOP1 ; LOOP TO 66$ IF SW09=1
COM R0 ; CHANGE BACK TO A FLOATING ONE
CLC ; CLEAR CARRY
ROL R0 ; SHIFT TO NEXT BIT
BNE 66$ ; BR IF NOT DONE YET?

```

```

; ***** TEST 25 *****
; *PORT6 REGISTER WRITE/READ TEST
; *FLOAT A ONE THROUGH PORT6 REGISTER
; *FLOAT A ZERO THROUGH PORT6 REGISTER
; *****

```

TEST 25

```

2882
2883 016306 000004
2884 016310 012737 000025 001202
2885 016316 012737 016432 001442
2886 016324 012737 016344 001444

```

```

; *****
†ST25: SCOPE
MOV #25,$STSTNM ; LOAD THE NO. OF THIS TEST
MOV #†ST26,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #64$,$LOCK ; ADDRESS FOR LOCK ON DATA.

```

KMC11 UNIBUS REGISTER TESTS

```

2887 016332 104410          MSTCLR          ;MASTER CLEAR KMC11
2888 016334 013701 002076  MOV          KMP06,R1          ;PUT REGISTER ADDRESS IN R1
2889 016340 012700 000001  MOV          #1,R0          ;START WITH BIT0
2890 016344          64$: MOV          R0,R5          ;PUT "EXPECTED" IN R5
2891 016344 010005          MOV          R5,(R1)        ;WRITE PORT6 REGISTER
2892 016346 010511          MOV          (R1),R4       ;READ PORT6 REGISTER
2893 016350 011104          CMP          R5,R4        ;COMPARE EXPECTED AND FOUND
2894 016352 020504          BEQ          65$         ;BR IF OK
2895 016354 001401          ERROR       2          ;WRITE/READ ERROR
2896 016356 104002          SCOPI          ;LOOP TO 64$ IF SW09=1
2897 016360 104405          CLC          ;CLEAR CARRY
2898 016362 000241          ROL          R0          ;SHIFT TO NEXT BIT
2899 016364 006100          BNE          64$        ;BR IF NOT DONE YET?
2900 016366 001366          MOV          #66$,LOCK   ;NEW SCOPI
2901 016370 012737 016402 001444  MOV          #1,R0          ;START WITH BIT0
2902 016376 012700 000001  66$: COM          R0          ;CHANGE TO A FLOATING ZERO
2903 016402          MOV          R0,R5        ;PUT "EXPECTED" IN R5
2904 016402 005100          MOV          R5,(R1)     ;WRITE PORT6 REGISTER
2905 016404 010005          MOV          (R1),R4     ;READ PORT6 REGISTER
2906 016406 010511          CMP          R5,R4       ;COMPARE EXPECTED AND FOUND
2907 016410 011104          BEQ          67$         ;BR IF OK
2908 016412 020504          ERROR       2          ;WRITE/READ ERROR
2909 016414 001401          SCOPI          ;LOOP TO 66$ IF SW09=1
2910 016416 104002          COM          R0          ;CHANGE BACK TO A FLOATING ONE
2911 016420 104405          CLC          ;CLEAR CARRY
2912 016422 005100          ROL          R0          ;SHIFT TO NEXT BIT
2913 016424 000241          BNE          66$        ;BR IF NOT DONE YET?
2914 016426 006100
2915 016430 001364

```

```

***** TEST 26 *****
;UNIBUS REGISTER BYTE DUAL ADDRESSING TEST
;LOAD ALL REGISTERS WITH INCREMENTING PATTERN
;READ BACK ALL REGISTERS TO VERIFY CORRECT ADDRESSING
*****

```

TEST 26

```

2926 016432 000004          ;*****
2927 016434 012737 000026 001202  TST26: SCOPE          ;LOAD THE NO. OF THIS TEST
2928 016434 012737 000026 001202  MOV          #26,$TSTNM    ;POINT TO THE START OF NEXT TEST.
2929 016442 012737 016562 001442  MOV          #TST27,NEXT   ;ADDRESS FOR LOCK ON DATA.
2930 016450 012737 016464 001444  MOV          #1$,LOCK     ;R1 CONTAINS BASE KMC11 ADDRESS
2931 016456 104410          ;MASTER CLEAR KMC11
2932 016456 104410          MSTCLR
2933 016460 012700 000001  MOV          #1,R0        ;START PATTERN AT 1
2934 016464 105011          CLR          (R1)        ;CLEAR REGISTER
2935 016466 110005          MOV          R0,R5        ;PUT DATA IN "EXPECTED"
2936 016470 110011          MOV          R0,(R1)     ;WRITE KMC REGISTER WITH PATTERN
2937 016472 111104          MOV          (R1),R4     ;READ KMC REGISTER INTO "FOUND"
2938 016474 020504          CMP          R5,R4       ;IS DATA CORRECT
2939 016476 001401          BEQ          2$         ;BR IF YES
2940 016500 104002          ERROR       2          ;DATA ERROR
2941 016502 104405          SCOPI          ;SW09=1?
2942 016504 105721          TST          (R1)+       ;NEXT REGISTER

```

```

2943 016506 005200          INC      RO          ; INCREMENT DATA PATTERN
2944 016510 022700 000011  CMP      #11,RO     ; LAST REGISTER?
2945 016514 001363          BNE      1$         ; BR IF NO
2946 016516 013701 002066  MOV      KMCSR,R1   ; BASE KMC11 ADDRESS TO R1
2947 016522 012700 000001  MOV      #1,RO      ; RESTART PATTERN AT 1
2948 016526 012737 016534 001444  MOV      #3$,LOCK   ; NEW SCOPE
2949 016534 110005          MOV      RO,R5     ; PUT DATA IN "EXPECTED"
2950 016536 111104          MOV      (R1),R4   ; READ KMC REGISTER INTO "FOUND"
2951 016540 020504          CMP      R5,R4     ; IS DATA CORRECT
2952 016542 001401          BEQ      4$         ; BR IF YES
2953 016544 104002          ERROR   2         ; DUAL ADDRESSING ERROR
2954 016546 104405          SCOPE  1         ; SMO9=1?
2955 016550 105721          TSTB   (R1)+      ; NEXT REGISTER
2956 016552 005200          INC      RO          ; INCREMENT PATTERN
2957 016554 022700 000011  CMP      #11,RO     ; LAST REGISTER?
2958 016560 001365          BNE      3$         ; BR IF NO

```

```

;***** TEST 27 *****
;#MAINTENANCE INSTRUCTION REGISTER TEST
;#VERIFY THAT THE MAINT IR CAN BE WRITTEN TO ALL ZEROS'
;#AND ALL ONES'. VERIFY THAT IT IS CLEARED ON A BUS RESET.
;*****

```

TEST 27

```

2969          ;*****
2970 016562 000004          TST27: SCOPE
2971 016564 012737 000027 001202  MOV      #27,$TSTNM ; LOAD THE NO. OF THIS TEST
2972 016572 012737 016722 001442  MOV      #TST30,NEXT ; POINT TO THE START OF NEXT TEST.
2973 016600 012737 016616 001444  MOV      #1$,LOCK   ; ADDRESS FOR LOCK ON DATA.
2974          ;R1 CONTAINS BASE KMC11 ADDRESS
2975 016606 104410          MSTCLR ; MASTER CLEAR KMC11
2976 016610 012711 003000  MOV      #BIT9:BIT10,(R1) ; SEL6 IS NOW THE IR
2977 016614 005005          CLR      R5        ; PUT "EXPECTED" IN R5
2978 016616 010561 000006 1$:  MOV      R5,6(R1)   ; CLEAR THE IR
2979 016622 016104 000006  MOV      6(R1),R4   ; READ THE IR
2980 016626 020504          CMP      R5,R4     ; IS IT CLEARED?
2981 016630 001401          BEQ      2$         ; BR IF YES
2982 016632 104023          ERROR   23        ; ERROR IR IS NOT CLEAR
2983 016634 104405          SCOPE  2         ; LOOP TO 1$ IF SMO9=1
2984 016636 012737 016650 001444  MOV      #3$,LOCK   ; NEW SCOPE
2985 016644 012705 177777  MOV      #-1,R5     ; PUT "EXPECTED" IN R5
2986 016650 010561 000006 3$:  MOV      R5,6(R1)   ; WRITE ALL ONES TO THE IR
2987 016654 016104 000006  MOV      6(R1),R4   ; READ THE IR
2988 016660 020504          CMP      R5,R4     ; IS IT ALL ONES?
2989 016662 001401          BEQ      4$         ; BR IF YES
2990 016664 104023          ERROR   23        ; ERROR IR IS NOT = ALL ONES
2991 016666 104405          SCOPE  4         ; LOOP TO 3$ IF SMO9=1
2992 016670 012737 016700 001444  MOV      #5$,LOCK   ; NEW SCOPE
2993 016676 005005          CLR      R5        ; PUT "EXPECTED" IN R5
2994 016700 000005 5$:  RESET ; BUS RESET
2995 016702 012711 003000  MOV      #BIT9:BIT10,(R1) ; SEL6 IS IR
2996 016706 016104 000006  MOV      6(R1),R4   ; READ THE IR
2997 016712 020504          CMP      R5,R4     ; IS IT CLEARED?
2998 016714 001401          BEQ      6$         ; BR IF YES

```

2999 016716 104023
3000 016720 104405

6\$: ERROR 23 ;ERROR, IR IS NOT CLEARED
SCOPI ;LOOP TO 5\$ IF SW09=1

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016722 000004
016724 012737 000030 001202
016732 012737 017064 001442
016740 012737 016756 001444
016746 104410
016750 012711 003000
016754 005005
016756 010561 000006
016762 016104 000006
016766 020504
016770 001401
016772 104023
016774 104405
016776 012737 017010 001444
017004 012705 177777
017010 010561 000006
017014 016104 000006
017020 020504
017022 001401
017024 104023
017026 104405
017030 012737 017040 001444
017036 005005
017040 052711 040000
017044 012711 003000
017050 016104 000006
017054 020504
017056 001401
017060 104023
017062 104405

```
***** TEST 30 *****
;MAINTENANCE INSTRUCTION REGISTER TEST
;VERIFY THAT THE MAIN? IR CAN BE WRITTEN TO ALL ZEROS'
;AND ALL ONES'. VERIFY THAT IT IS CLEARED ON A MASTER RESET.
*****

; TEST 30
-----
;*****
;TST30: SCOPE
;MOV #30,STSTNM ; LOAD THE NO. OF THIS TEST
;MOV #TST31,NEXT ; POINT TO THE START OF NEXT TEST.
;MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
;R1 CONTAINS BASE KMC11 ADDRESS
;MASTER CLEAR KMC11
;SEL6 IS NOW THE IR
;PUT "EXPECTED" IN R5
;CLEAR THE IR
;READ THE IR
;IS IT CLEARED?
;BR IF YES
;ERROR IR IS NOT CLEAR
;LOOP TO 1$ IF SW09=1
;NEW SCOPI
;PUT "EXPECTED" IN R5
;WRITE ALL ONES TO THE IR
;READ THE IR
;IS IT ALL ONES?
;BR IF YES
;ERROR IR IS NOT = ALL ONES
;LOOP TO 3$ IF SW09=1
;NEW SCOPI
;PUT "EXPECTED" IN R5
;MASTER CLEAR
;SEL6 IS IR
;READ THE IR
;IS IT CLEARED?
;BR IF YES
;ERROR, IR IS NOT CLEARED
;LOOP TO 5$ IF SW09=1

1$: MOV #BIT9:BIT10,(R1)
CLR R5
MOV R5,6(R1)
MOV 6(R1),R4
CMP R5,R4
BEQ 2$
ERROR 23
SCOPI

2$: MOV #3$,LOCK
MOV #-1,R5
MOV R5,6(R1)
MOV 6(R1),R4
CMP R5,R4
BEQ 4$
ERROR 23
SCOPI

4$: MOV #5$,LOCK
CLR R5
BIS #BIT14,(R1)
MOV #BIT9:BIT10,(R1)
MOV 6(R1),R4
CMP R5,R4
BEQ 6$
ERROR 23
SCOPI

6$:
```

```
***** TEST 31 *****
;MICRO PROCESSOR TEST
;LOAD KMP06 WITH A MICRO-PROCESSOR INSTRUCTION, CLOCK IT
;VERIFY INSTRUCTION EXECUTED PROPERLY
;INSTRUCTION SHOULD MOVE IBUS*4 TO IBUS*5, IBUS*4 IS ALL 1'S
;AND IBUS*5 IS ALL 0'S. RESULT SHOULD BE ALL 1'S IN SEL4
*****

; TEST 31
-----
```

```

3055
3056 017064 000004
3057 017066 012737 000031 001202
3058 017074 012737 017150 001442
3059
3060 017102 104410
3061 017104 012761 000377 000004
3062 017112 012711 001000
3063 017116 012761 121105 000006
3064 017124 052711 001400
3065 017130 000240
3066 017132 012705 177777
3067 017136 016104 000004
3068 017142 020504
3069 017144 001401
3070 017146 104003
3071 017150

```

```

*****
†ST31: SCOPE
MOV #31,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #ST32,NEXT ; POINT TO THE START OF NEXT TEST.
;R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ;MASTER CLEAR KMC11
MOV #377,4(R1) ;PORT4 HI-BYTE=0'S LO-BYTE=1'S
MOV #BIT9,(R1) ;SET ROMI
MOV #121105,6(R1) ;INSTRUCTION TO PORT6
BIS #BIT8!BIT9,(R1) ;CLK INSTRUCTION, MOVE IBUS*4 TO IBUS*5
NOP
MOV #-1,R5 ;PUT "EXPECTED" IN R5
MOV 4(R1),R4 ;PUT "FOUND" INTO R4
CMP R5,R4 ;IS DATA CORRECT
BEQ 1$ ;BR IF YES
ERROR 3 ;ERROR
1$:

```

```

3072
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3074
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```

```

***** TEST 32 *****
;MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
;FLOAT A 1 THROUGH IBUS* REGISTER 0
;FLOAT A 0 THROUGH IBUS* REGISTER 0
*****
; TEST 32
-----

```

```

3083 017150 000004
3084 017152 012737 000032 001202
3085 017160 012737 017350 001442
3086 017166 012737 017206 001444
3087
3088 017174 104410
3089 017176 012702 000000
3090 017202 012700 000001
3091 017206
3092 017206 010061 000004
3093 017212 042761 000030 000004
3094 017220 104412
3095 017222 121100
3096 017224 104412
3097 017226 121005
3098 017230 010005
3099 017232 042705 000030
3100 017236 116104 000005
3101 017242 120504
3102 017244 001401
3103 017246 104004
3104 017250 104405
3105 017252 000241
3106 017254 106100
3107 017256 001353
3108 017260 012737 017274 001444
3109 017266 012700 000001
3110 017272 005100

```

```

*****
†ST32: SCOPE
MOV #32,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #ST33,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #64$,LOCK ; ADDRESS FOR LOCK ON DATA.
;R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ;MASTER CLEAR KMC11
MOV #0,R2 ;SAVE REGISTER ADDRESS FOR TYPEOUT
MOV #1,R0 ;START WITH BIT 0
64$: MOV R0,4(R1) ;PUT PATTERN INTO PORT4
BIC #30,4(R1) ;CLEAR UNWANTED BITS
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
121100!0 ;MOV DATA TO IBUS* REGISTER 0
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
121005!(0*20) ;READ FROM IBUS* REGISTER 0
MOV R0,R5 ;PUT EXPECTED IN R5
BIC #30,R5 ;CLEAR UNWANTED BITS
MOVB 5(R1),R4 ;PUT "FOUND" INTO R4
CMPB R5,R4 ;DATA CORRECT?
BEQ 65$ ;BR IF YES
ERROR 4 ;ERROR
65$: SCOPI ;SW09=1?
CLC ;CLEAR CARRY
ROLB R0 ;SHIFT BIT IN R0
BNE 64$ ;IF R0=0 THEN DONE
MOV #67$,LOCK ;NEW SCOPI
MOV #1,R0 ;START WITH BIT 0
69$: COM R0 ;CHANGE TO FLOATING ZERO

```

KMC11 MICRO PROCESSOR IBUS* TESTS

```

3111 017274          67$: MOV      RO,4(R1)      ;PUT PATTERN INTO PORT4
3112 017274 010061 000004      BIC      #30,4(R1)    ;CLEAR UNWANTED BITS
3113 017300 042761 000030 000004 ROMCLK    ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3114 017306 104412          121100!0    ;MOV DATA TO IBUS* REGISTER 0
3115 017310 121100 ROMCLK    ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3116 017312 104412          121005!<0*20> ;READ FROM IBUS* REGISTER 0
3117 017314 121005 MOV      RO,R5      ;PUT EXPECTED IN R5
3118 017316 010005 BIC      #30,R5      ;CLEAR UNWANTED BITS
3119 017320 042705 000030      MOVVB    5(R1),R4    ;PUT "FOUND" INTO R4
3120 017324 116104 000005      CMPB    R5,R4      ;DATA CORRECT?
3121 017330 120504 BEQ      68$        ;BR IF YES
3122 017332 001401 ERROR    4          ;ERROR
3123 017334 104004          68$: SCOPE1     ;SW09=1?
3124 017336 104405 COM      RO      ;CHANGE TO FLOATING 1
3125 017340 005100 CLC          ;CLEAR CARRY
3126 017342 000241 ROLB    RO      ;SHIFT BIT IN RO
3127 017344 106100 BNE      69$        ;IF RO=0 THEN DONE
3128 017346 001351

```

```

***** TEST 33 *****
;MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
;FLOAT A 1 THROUGH IBUS* REGISTER 2
;FLOAT A 0 THROUGH IBUS* REGISTER 2
*****

```

TEST 33

```

3130
3131
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3139
3140 017350 000004          ;*****
3141 017352 012737 000033 001202 TST33: SCOPE
3142 017360 012737 017550 001442 MOV      #33,$TSTNM  ; LOAD THE NO. OF THIS TEST
3143 017366 012737 017406 001444 MOV      #TST34,NEXT ; POINT TO THE START OF NEXT TEST.
3144          MOV      #64$,LOCK ; ADDRESS FOR LOCK ON DATA.
3145 017374 104410 MSTCLR    ;R1 CONTAINS BASE KMC11 ADDRESS
3146 017376 012702 000002      ;MASTER CLEAR KMC11
3147 017402 012700 000001      MOV      #2,R2      ;SAVE REGISTER ADDRESS FOR TYPEOUT
3148 017406          MOV      #1,R0 ;START WITH BIT 0
3149 017406 010061 000004          64$: MOV      RO,4(R1)    ;PUT PATTERN INTO PORT4
3150 017412 042761 000070 000004 BIC      #70,4(R1)  ;CLEAR UNWANTED BITS
3151 017420 104412          ROMCLK    ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3152 017422 121102          121100!2    ;MOV DATA TO IBUS* REGISTER 2
3153 017424 104412          ROMCLK    ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3154 017426 121045          121005!<2*20> ;READ FROM IBUS* REGISTER 2
3155 017430 010005 MOV      RO,R5      ;PUT EXPECTED IN R5
3156 017432 042705 000070      BIC      #70,R5      ;CLEAR UNWANTED BITS
3157 017436 116104 000005      MOVVB    5(R1),R4    ;PUT "FOUND" INTO R4
3158 017442 120504 CMPB    R5,R4      ;DATA CORRECT?
3159 017444 001401 BEQ      65$        ;BR IF YES
3160 017446 104004 ERROR    4          ;ERROR
3161 017450 104405          65$: SCOPE1     ;SW09=1?
3162 017452 000241 CLC          ;CLEAR CARRY
3163 017454 106100 ROLB    RO      ;SHIFT BIT IN RO
3164 017456 001353 BNE      64$        ;IF RO=0 THEN DONE
3165 017460 012737 017474 001444 MOV      #67$,LOCK  ;NEW SCOPE1
3166 017466 012700 000001      MOV      #1,R0 ;START WITH BIT 0

```


KMC11 MICRO PROCESSOR IBUS* TESTS

```

3167 017472 005100      69$: COM      RO      ;CHANGE TO FLOATING ZERO
3168 017474      67$:      ;
3169 017474 010061 000004      MOV      RO,4(R1)      ;PUT PATTERN INTO PORT4
3170 017500 042761 000070 000004      BIC      #70,4(R1)      ;CLEAR UNWANTED BITS
3171 017506 104412      ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3172 017510 121102      121100!2      MOV      DATA TO IBUS* REGISTER 2
3173 017512 104412      ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3174 017514 121045      121005!<2*20>      READ FROM IBUS* REGISTER 2
3175 017516 010005      MOV      RO,R5      ;PUT EXPECTED IN R5
3176 017520 042705 000070      BIC      #70,R5      ;CLEAR UNWANTED BITS
3177 017524 116104 000005      MOV      5(R1),R4      ;PUT "FOUND" INTO R4
3178 017530 120504      CMPB     R5,R4      ;DATA CORRECT?
3179 017532 001401      BEQ      68$      ;BR IF YES
3180 017534 104004      ERROR    4      ;ERROR
3181 017536 104405      68$: SCOPI      ;SW09=1?
3182 017540 005100      COM      RO      ;CHANGE TO FLOATING 1
3183 017542 000241      CLC      ;CLEAR CARRY
3184 017544 106100      ROLB     RO      ;SHIFT BIT IN RO
3185 017546 001351      BNE      69$      ;IF RO=0 THEN DONE

```

```

3186
3187
3188      ;***** TEST 34 *****
3189      ;*MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
3190      ;*FLOAT A 1 THROUGH IBUS* REGISTER 4
3191      ;*FLOAT A 0 THROUGH IBUS* REGISTER 4
3192      ;*****

```

```

3193
3194      ; TEST 34
3195      ;-----

```

```

3196
3197 017550 000004      ;*****
3198 017552 012737 000034 001202      †TST34: SCOPE
3199 017560 012737 017724 001442      MOV      #34,$STSTM      ; LOAD THE NO. OF THIS TEST
3200 017566 012737 017606 001444      MOV      #TST35,NEXT      ; POINT TO THE START OF NEXT TEST.

```

```

3201      MOV      #64$,$LOCK      ; ADDRESS FOR LOCK ON DATA.
3202 017574 104410      MSTCLR      ;R1 CONTAINS BASE KMC11 ADDRESS
3203 017576 012702 000004      MOV      #4,R2      ;MASTER CLEAR KMC11
3204 017602 012700 000001      MOV      #1,RO      ;SAVE REGISTER ADDRESS FOR TYPEOUT
3205 017606      64$:      ;START WITH BIT 0

```

```

3206 017606 010061 000004      64$: MOV      RO,4(R1)      ;PUT PATTERN INTO PORT4
3207 017612 104412      ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3208 017614 121104      121100!4      MOV      DATA TO IBUS* REGISTER 4
3209 017616 104412      ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3210 017620 121105      121005!<4*20>      READ FROM IBUS* REGISTER 4
3211 017622 010005      MOV      RO,R5      ;PUT EXPECTED IN R5
3212 017624 116104 000005      MOV      5(R1),R4      ;PUT "FOUND" INTO R4
3213 017630 120504      CMPB     R5,R4      ;DATA CORRECT?
3214 017632 001401      BEQ      65$      ;BR IF YES
3215 017634 104004      ERROR    4      ;ERROR
3216 017636 104405      65$: SCOPI      ;SW09=1?
3217 017640 000241      CLC      ;CLEAR CARRY
3218 017642 106100      ROLB     RO      ;SHIFT BIT IN RO
3219 017644 001360      BNE      64$      ;IF RO=0 THEN DONE

```

```

3220 017646 012737 017662 001444      MOV      #67$,$LOCK      ;NEW SCOPI
3221 017654 012700 000001      MOV      #1,RO      ;START WITH BIT 0
3222 017660 005100      69$: COM      RO      ;CHANGE TO FLOATING ZERO

```

KMC11 MICRO PROCESSOR IBUS* TESTS

3223	017662			67\$:	MOV	RO,4(R1)	;PUT PATTERN INTO PORT4
3224	017662	010061	000004		ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3225	017666	104412			121100!4		;MOV DATA TO IBUS* REGISTER 4
3226	017670	121104			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3227	017672	104412			121005!<4*20>		;READ FROM IBUS* REGISTER 4
3228	017674	121105			MOV	RO,R5	;PUT EXPECTED IN R5
3229	017676	010005			MOVB	5(R1),R4	;PUT "FOUND" INTO R4
3230	017700	116104	000005		CMPB	R5,R4	;DATA CORRECT?
3231	017704	120504			BEQ	68\$;BR IF YES
3232	017706	001401			ERROR	4	;ERROR
3233	017710	104004			68\$:	SCOPI	;SW09=1?
3234	017712	104405			COM	RO	;CHANGE TO FLOATING 1
3235	017714	005100			CLC		;CLEAR CARRY
3236	017716	000241			ROLB	RO	;SHIFT BIT IN RO
3237	017720	106100			BNE	69\$;IF RO=0 THEN DONE
3238	017722	001356					

***** TEST 35 *****
 ;MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
 ;FLOAT A 1 THROUGH IBUS* REGISTER 5
 ;FLOAT A 0 THROUGH IBUS* REGISTER 5
 ;*****

TEST 35

3240							
3241							
3242							
3243							
3244							
3245							
3246							
3247							
3248							
3249							
3250	017724	000004		TST35:	SCOPE		
3251	017726	012737	000035	001202	MOV	#35,\$STSTM	; LOAD THE NO. OF THIS TEST
3252	017734	012737	020100	001442	MOV	#TST36,NEXT	; POINT TO THE START OF NEXT TEST.
3253	017742	012737	017762	001444	MOV	#64\$,\$LOCK	; ADDRESS FOR LOCK ON DATA.
3254							;R1 CONTAINS BASE KMC11 ADDRESS
3255	017750	104410			MSTCLR		;MASTER CLEAR KMC11
3256	017752	012702	000005		MOV	#5,R2	;SAVE REGISTER ADDRESS FOR TYPEOUT
3257	017756	012700	000001		MOV	#1,RO	;START WITH BIT 0
3258	017762			64\$:			
3259	017762	010061	000004		MOV	RO,4(R1)	;PUT PATTERN INTO PORT4
3260	017766	104412			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3261	017770	121105			121100!5		;MOV DATA TO IBUS* REGISTER 5
3262	017772	104412			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3263	017774	121125			121005!<5*20>		;READ FROM IBUS* REGISTER 5
3264	017776	010005			MOV	RO,R5	;PUT EXPECTED IN R5
3265	020000	116104	000005		MOVB	5(R1),R4	;PUT "FOUND" INTO R4
3266	020004	120504			CMPB	R5,R4	;DATA CORRECT?
3267	020006	001401			BEQ	65\$;BR IF YES
3268	020010	104004			ERROR	4	;ERROR
3269	020012	104405		65\$:	SCOPI		;SW09=1?
3270	020014	000241			CLC		;CLEAR CARRY
3271	020016	106100			ROLB	RO	;SHIFT BIT IN RO
3272	020020	001360			BNE	64\$;IF RO=0 THEN DONE
3273	020022	012737	020036	001444	MOV	#67\$,\$LOCK	;NEW SCOPI
3274	020030	012700	000001		MOV	#1,RO	;START WITH BIT 0
3275	020034	005100		69\$:	COM	RO	;CHANGE TO FLOATING ZERO
3276	020036			67\$:			
3277	020036	010061	000004		MOV	RO,4(R1)	;PUT PATTERN INTO PORT4
3278	020042	104412			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

```

3279 020044 121105      121100!5      ;MOV DATA TO IBUS* REGISTER 5
3280 020046 104412      ROMCLK        ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3281 020050 121125      121005!<5*20> ;READ FROM IBUS* REGISTER 5
3282 020052 010005      MOV          R0,R5 ;PUT EXPECTED IN R5
3283 020054 116104      000005      MOVB        5(R1),R4 ;PUT "FOUND" INTO R4
3284 020060 120504      CMPB        R5,R4 ;DATA CORRECT?
3285 020062 001401      BEQ         68$ ;BR IF YES
3286 020064 104004      ERROR      4 ;ERROR
3287 020066 104405      68$: SCOPI   ;SW09=1?
3288 020070 005100      COM         R0 ;CHANGE TO FLOATING 1
3289 020072 000241      CLC        ;CLEAR CARRY
3290 020074 106100      ROLB        R0 ;SHIFT BIT IN R0
3291 020076 001356      BNE         69$ ;IF R0=0 THEN DONE

```

```

***** TEST 36 *****
;MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
;FLOAT A 1 THROUGH IBUS* REGISTER 10
;FLOAT A 0 THROUGH IBUS* REGISTER 10
*****

```

TEST 36

```

3300
3301
3302
3303 020100 000004      TST36: SCOPE
3304 020102 012737 000036 001202      MOV          #36,STSTNM ;LOAD THE NO. OF THIS TEST
3305 020110 012737 020300 001442      MOV          #TST37,NEXT ;POINT TO THE START OF NEXT TEST.
3306 020116 012737 020136 001444      MOV          #64$,LOCK ;ADDRESS FOR LOCK ON DATA.
3307
3308 020124 104410      MSTCLR      ;R1 CONTAINS BASE KMC11 ADDRESS
3309 020126 012702 000010      MOV          #10,R2 ;MASTER CLEAR KMC11
3310 020132 012700 000001      MOV          #1,R0 ;SAVE REGISTER ADDRESS FOR TYPEOUT
3311 020136
3312 020136 010061 000004      64$: MOV          R0,4(R1) ;PUT PATTERN INTO PORT4
3313 020142 042761 000141 000004      BIC          #141,4(R1) ;CLEAR UNWANTED BITS
3314 020150 104412      ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3315 020152 121110      121100!10 ;MOV DATA TO IBUS* REGISTER 10
3316 020154 104412      ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3317 020156 121205      121005!<10*20> ;READ FROM IBUS* REGISTER 10
3318 020160 010005      MOV          R0,R5 ;PUT EXPECTED IN R5
3319 020162 042705 000141      BIC          #141,R5 ;CLEAR UNWANTED BITS
3320 020166 116104 000005      MOVB        5(R1),R4 ;PUT "FOUND" INTO R4
3321 020172 120504      CMPB        R5,R4 ;DATA CORRECT?
3322 020174 001401      BEQ         65$ ;BR IF YES
3323 020176 104004      ERROR      4 ;ERROR
3324 020200 104405      65$: SCOPI   ;SW09=1?
3325 020202 000241      CLC        ;CLEAR CARRY
3326 020204 106100      ROLB        R0 ;SHIFT BIT IN R0
3327 020206 001353      BNE         64$ ;IF R0=0 THEN DONE
3328 020210 012737 020224 001444      MOV          #67$,LOCK ;NEW SCOPI
3329 020216 012700 000001      MOV          #1,R0 ;START WITH BIT 0
3330 020222 005100      69$: COM         R0 ;CHANGE TO FLOATING ZERO
3331 020224
3332 020224 010061 000004      67$: MOV          R0,4(R1) ;PUT PATTERN INTO PORT4
3333 020230 042761 000141 000004      BIC          #141,4(R1) ;CLEAR UNWANTED BITS
3334 020236 104412      ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

```

```

3335 020240 121110          121100!10          ;MOV DATA TO IBUS* REGISTER 10
3336 020242 104412          ROMCLK           ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3337 020244 121205          121005!<10*20> ;READ FROM IBUS* REGISTER 10
3338 020246 010005          MOV R0,R5       ;PUT EXPECTED IN R5
3339 020250 042705 000141  BIC #141,R5     ;CLEAR UNWANTED BITS
3340 020254 116104 000005  MOVB 5(R1),R4   ;PUT "FOUND" INTO R4
3341 020260 120504          CMPB R5,R4     ;DATA CORRECT?
3342 020262 001401          BEQ 68$        ;BR IF YES
3343 020264 104004          ERROR 4       ;ERROR
3344 020266 104405          SCOPE         ;SW09=1?
3345 020270 005100          COM R0        ;CHANGE TO FLOATING 1
3346 020272 000241          CLC           ;CLEAR CARRY
3347 020274 106100          ROLB R0       ;SHIFT BIT IN R0
3348 020276 001351          BNE 69$       ;IF R0=0 THEN DONE
3349
3350

```

```

***** TEST 37 *****
;MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
;FLOAT A 1 THROUGH IBUS* REGISTER 11
;FLOAT A 0 THROUGH IBUS* REGISTER 11
*****

```

TEST 37

```

3351
3352
3353
3354
3355
3356
3357
3358
3359
3360 020300 000004          ;*****
3361 020302 012737 000037 001202  TST37: SCOPE
3362 020310 012737 020510 001442  MOV #37,$TSTNM ; LOAD THE NO. OF THIS TEST
3363 020316 012737 020336 001444  MOV #TST40,NEXT ; POINT TO THE START OF NEXT TEST.
3364          MOV #64$,$LOCK ; ADDRESS FOR LOCK ON DATA.
3365 020324 104410          ;R1 CONTAINS BASE KMC11 ADDRESS
3366 020326 012702 000011  MSTCLR        ;MASTER CLEAR KMC11
3367 020332 012700 000001  MOV #11,R2    ;SAVE REGISTER ADDRESS FOR TYPEOUT
3368 020336          MOV #1,R0     ;START WITH BIT 0
3369 020336 010061 000004          64$: MOV R0,4(R1) ;PUT PATTERN INTO PORT4
3370 020342 042761 000262 000004  BIC #262,4(R1) ;CLEAR UNWANTED BITS
3371 020350 104412          ROMCLK        ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3372 020352 121111          121100!11    ;MOV DATA TO IBUS* REGISTER 11
3373 020354 104412          ROMCLK        ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3374 020356 121225          121005!<11*20> ;READ FROM IBUS* REGISTER 11
3375 020360 010005          MOV R0,R5     ;PUT EXPECTED IN R5
3376 020362 042705 000262  BIC #262,R5   ;CLEAR UNWANTED BITS
3377 020366 052705 000020  BIS #20,R5    ;ADD THESE BITS
3378 020372 116104 000005  MOVB 5(R1),R4 ;PUT "FOUND" INTO R4
3379 020376 120504          CMPB R5,R4   ;DATA CORRECT?
3380 020400 001401          BEQ 65$      ;BR IF YES
3381 020402 104004          ERROR 4     ;ERROR
3382 020404 104405          SCOPE         ;SW09=1?
3383 020406 000241          CLC           ;CLEAR CARRY
3384 020410 106100          ROLB R0     ;SHIFT BIT IN R0
3385 020412 001351          BNE 64$     ;IF R0=0 THEN DONE
3386 020414 012737 020430 001444  MOV #67$,$LOCK ;NEW SCOPE
3387 020422 012700 000001  MOV #1,R0    ;START WITH BIT 0
3388 020426 005100          69$: COM R0  ;CHANGE TO FLOATING ZERO
3389 020430          67$:
3390 020430 010061 000004          MOV R0,4(R1) ;PUT PATTERN INTO PORT4

```

```

3391 020434 042761 000262 000004      BIC      #262,4(R1)      ;CLEAR UNWANTED BITS
3392 020442 104412                      ROMCLK                    ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3393 020444 121111                      121100!11                ;MOV DATA TO IBUS* REGISTER 11
3394 020446 104412                      ROMCLK                    ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3395 020450 121225                      121005!<11*20>          ;READ FROM IBUS* REGISTER 11
3396 020452 010005                      MOV      R0,R5            ;PUT EXPECTED IN R5
3397 020454 042705 000262          BIC      #262,R5          ;CLEAR UNWANTED BITS
3398 020460 052705 000020          BIS      #20,R5          ;ADD THESE BITS
3399 020464 116104 000005          MOV8    5(R1),R4         ;PUT "FOUND" INTO R4
3400 020470 120504                      CMPB    R5,R4            ;DATA CORRECT?
3401 020472 001401                      BEQ     68$              ;BR IF YES
3402 020474 104004                      ERROR   4                ;ERROR
3403 020476 104405                      68$:  SCOP1              ;SM09=1?
3404 020500 005100                      COM     R0                ;CHANGE TO FLOATING 1
3405 020502 000241                      CLC                                ;CLEAR CARRY
3406 020504 106100                      ROLB   R0                ;SHIFT BIT IN R0
3407 020506 001347                      BNE    69$              ;IF R0=0 THEN DONE

```

```

;***** TEST 40 *****
;MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
;FLOAT A 1 THROUGH IBUS REGISTER 0
;FLOAT A 0 THROUGH IBUS REGISTER 0
;*****

```

; TEST 40

```

3418 020510 000004                      ;*****
3419 020512 012737 000040 001202      †ST40: SCOP1              ;LOAD THE NO. OF THIS TEST
3420 020512 012737 000040 001202      MOV     #40,STSTNM        ;POINT TO THE START OF NEXT TEST.
3421 020520 012737 020664 001442      MOV     #TST41,NEXT      ;ADDRESS FOR LOCK ON DATA.
3422 020526 012737 020546 001444      MOV     #64$,LOCK        ;R1 CONTAINS BASE KMC11 ADDRESS
3423 020534 104410                      MSTCLR                    ;MASTER CLEAR KMC11
3424 020534 104410                      MOV     #0,R2            ;SAVE REGISTER ADDRESS FOR TYPEOUT
3425 020536 012702 000000          MOV     #1,R0            ;START WITH BIT 0
3426 020542 012700 000001          64$:  MOV     R0,4(R1)    ;PUT PATTERN INTO PORT4
3427 020546 010061 000004          ROMCLK                    ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3428 020546 010061 000004          122100!0                ;MOV DATA TO IBUS REGISTER 0
3429 020552 104412                      ROMCLK                    ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3430 020554 122100                      21005!<0*20>           ;READ FROM IBUS REGISTER 0
3431 020556 104412                      MOV     R0,R5            ;PUT EXPECTED IN R5
3432 020560 021005                      MOV8    5(R1),R4         ;PUT "FOUND" INTO R4
3433 020562 010005                      CMPB    R5,R4            ;DATA CORRECT?
3434 020564 116104 000005          BEQ     65$              ;BR IF YES
3435 020570 120504                      ERROR   5                ;ERROR
3436 020572 001401                      65$:  SCOP1              ;SM09=1?
3437 020574 104005                      CLC                                ;CLEAR CARRY
3438 020576 104405                      ROLB   R0                ;SHIFT BIT IN R0
3439 020600 000241                      BNE    64$              ;IF R0=0 THEN DONE
3440 020602 106100                      MOV     #67$,LOCK        ;NEW SCOP1
3441 020604 001360                      MOV     #1,R0            ;START WITH BIT 0
3442 020606 012737 020622 001444      COM     R0                ;CHANGE TO FLOATING ZERO
3443 020614 012700 000001          69$:  MOV     R0,4(R1)    ;PUT PATTERN INTO PORT4
3444 020620 005100                      67$:
3445 020622 010061 000004
3446 020622 010061 000004

```

```

3447 020626 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3448 020630 122100 122100!0 ;MOV DATA TO IBUS REGISTER 0
3449 020632 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3450 020634 021005 21005!<0*20> ;READ FROM IBUS REGISTER 0
3451 020636 010005 MOV RO,R5 ;PUT EXPECTED IN R5
3452 020640 116104 000005 MOVB 5(R1),R4 ;PUT "FOUND" INTO R4
3453 020644 120504 CMPB R5,R4 ;DATA CORRECT?
3454 020646 001401 BEQ 68$ ;BR IF YES
3455 020650 104005 ERROR 5 ;ERROR
3456 020652 104405 68$: SCOP1 ;SM09=1?
3457 020654 005100 COM RO ;CHANGE TO FLOATING 1
3458 020656 000241 CLC ;CLEAR CARRY
3459 020660 106100 ROLB RO ;SHIFT BIT IN RO
3460 020662 001356 BNE 69$ ;IF RO=0 THEN DONE

```

```

:***** TEST 41 *****
:MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
:*FLOAT A 1 THROUGH IBUS REGISTER 1
:*FLOAT A 0 THROUGH IBUS REGISTER 1
:*****

```

TEST 41

```

3471 :*****
3472 020664 000004 TST41: SCOP1 ;*****
3473 020666 012737 000041 001202 MOV #41,STSTNM ;LOAD THE NO. OF THIS TEST
3474 020674 012737 021040 001442 MOV #TST42,NEXT ;POINT TO THE START OF NEXT TEST.
3475 020702 012737 020722 001444 MOV #64$,LOCK ;ADDRESS FOR LOCK ON DATA.
3476 ;R1 CONTAINS BASE KMC11 ADDRESS
3477 020710 104410 MSTCLR ;MASTER CLEAR KMC11
3478 020712 012702 000001 MOV #1,R2 ;SAVE REGISTER ADDRESS FOR TYPEOUT
3479 020716 012700 000001 MOV #1,RO ;START WITH BIT 0
3480 020722 64$:
3481 020722 010061 000004 MOV RO,4(R1) ;PUT PATTERN INTO PORT4
3482 020726 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3483 020730 122101 122100!1 ;MOV DATA TO IBUS REGISTER 1
3484 020732 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3485 020734 021025 21005!<1*20> ;READ FROM IBUS REGISTER 1
3486 020736 010005 MOV RO,R5 ;PUT EXPECTED IN R5
3487 020740 116104 000005 MOVB 5(R1),R4 ;PUT "FOUND" INTO R4
3488 020744 120504 CMPB R5,R4 ;DATA CORRECT?
3489 020746 001401 BEQ 65$ ;BR IF YES
3490 020750 104005 ERROR 5 ;ERROR
3491 020752 104405 65$: SCOP1 ;SM09=1?
3492 020754 000241 CLC ;CLEAR CARRY
3493 020756 106100 ROLB RO ;SHIFT BIT IN RO
3494 020760 001360 BNE 64$ ;IF RO=0 THEN DONE
3495 020762 012737 020776 001444 MOV #67$,LOCK ;NEW SCOP1
3496 020770 012700 000001 MOV #1,RO ;START WITH BIT 0
3497 020774 005100 69$: COM RO ;CHANGE TO FLOATING ZERO
3498 020776 67$:
3499 020776 010061 000004 MOV RO,4(R1) ;PUT PATTERN INTO PORT4
3500 021002 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3501 021004 122101 122100!1 ;MOV DATA TO IBUS REGISTER 1
3502 021006 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

```

```

3503 021010 021025
3504 021012 010005
3505 021014 116104 000005
3506 021020 120504
3507 021022 001401
3508 021024 104005
3509 021026 104405
3510 021030 005100
3511 021032 000241
3512 021034 106100
3513 021036 001356

```

68\$:

```

21005!<1*20>
MOV RO,R5
MOVB 5(R1),R4
CMPB R5,R4
BEQ 68$
ERROR 5
SCOPI
COM RO
CLC
ROLB RO
BNE 69$

```

```

;READ FROM IBUS REGISTER 1
;PUT EXPECTED IN R5
;PUT "FOUND" INTO R4
;DATA CORRECT?
;BR IF YES
;ERROR
;SW09=1?
;CHANGE TO FLOATING 1
;CLEAR CARRY
;SHIFT BIT IN RO
;IF RO=0 THEN DONE

```

```

3514
3515
3516
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3519
3520
3521
3522
3523
3524

```

```

;***** TEST 42 *****
;MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
;FLOAT A 1 THROUGH IBUS REGISTER 2
;FLOAT A 0 THROUGH IBUS REGISTER 2
;*****

```

TEST 42

```

3525 021040 000004
3526 021042 012737 000042 001202
3527 021050 012737 021214 001442
3528 021056 012737 021076 001444
3529
3530 021064 104410
3531 021066 012702 000002
3532 021072 012700 000001
3533 021076
3534 021076 010061 000004
3535 021102 104412
3536 021104 122102
3537 021106 104412
3538 021110 021045
3539 021112 010005
3540 021114 116104 000005
3541 021120 120504
3542 021122 001401
3543 021124 104005
3544 021126 104405
3545 021130 000241
3546 021132 106100
3547 021134 001360
3548 021136 012737 021152 001444
3549 021144 012700 000001
3550 021150 005100
3551 021152
3552 021152 010061 000004
3553 021156 104412
3554 021160 122102
3555 021162 104412
3556 021164 021045
3557 021166 010005
3558 021170 116104 000005

```

†ST42:

```

;*****
SCOPE
MOV #42,STSTNM
MOV #ST43,NEXT
MOV #64$,LOCK
MSTCLR
MOV #2,R2
MOV #1,RO
64$:
MOV RO,4(R1)
ROMCLK
122100!2
ROMCLK
21005!<2*20>
MOV RO,R5
MOVB 5(R1),R4
CMPB R5,R4
BEQ 65$
ERROR 5
65$:
SCOPI
CLC
ROLB RO
BNE 64$
MOV #67$,LOCK
MOV #1,RO
69$:
COM RO
67$:
MOV RO,4(R1)
ROMCLK
122100!2
ROMCLK
21005!<2*20>
MOV RO,R5
MOVB 5(R1),R4

```

```

;LOAD THE NO. OF THIS TEST
;POINT TO THE START OF NEXT TEST.
;ADDRESS FOR LOCK ON DATA.
;R1 CONTAINS BASE KMC11 ADDRESS
;MASTER CLEAR KMC11
;SAVE REGISTER ADDRESS FOR TYPEOUT
;START WITH BIT 0
;PUT PATTERN INTO PORT4
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;MOV DATA TO IBUS REGISTER 2
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;READ FROM IBUS REGISTER 2
;PUT EXPECTED IN R5
;PUT "FOUND" INTO R4
;DATA CORRECT?
;BR IF YES
;ERROR
;SW09=1?
;CLEAR CARRY
;SHIFT BIT IN RO
;IF RO=0 THEN DONE
;NEW SCOPI
;START WITH BIT 0
;CHANGE TO FLOATING ZERO

```

65\$:

69\$:
67\$:

```

;PUT PATTERN INTO PORT4
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;MOV DATA TO IBUS REGISTER 2
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;READ FROM IBUS REGISTER 2
;PUT EXPECTED IN R5
;PUT "FOUND" INTO R4

```

3559 021174 120504
3560 021176 001401
3561 021200 104005
3562 021202 104405
3563 021204 005100
3564 021206 000241
3565 021210 106100
3566 021212 001356

68\$: CMPB R5,R4 ; DATA CORRECT?
BEQ 68\$; BR IF YES
ERROR 5 ; ERROR
SCOPI ; SW09=1?
COM RO ; CHANGE TO FLOATING 1
CLC ; CLEAR CARRY
ROLB RO ; SHIFT BIT IN RO
BNE 69\$; IF RO=0 THEN DONE

***** TEST 43 *****
*MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
*FLOAT A 1 THROUGH IBUS REGISTER 3
*FLOAT A 0 THROUGH IBUS REGISTER 3

TEST 43

3577
3578 021214 000004
3579 021216 012737 000043 001202
3580 021224 012737 021370 001442
3581 021232 012737 021252 001444
3582
3583 021240 104410
3584 021242 012702 000003
3585 021246 012700 000001
3586 021252
3587 021252 010061 000004
3588 021256 104412
3589 021260 122103
3590 021262 104412
3591 021264 021065
3592 021266 010005
3593 021270 116104 000005
3594 021274 120504
3595 021276 001401
3596 021300 104005
3597 021302 104405
3598 021304 000241
3599 021306 106100
3600 021310 001360
3601 021312 012737 021326 001444
3602 021320 012700 000001
3603 021324 005100
3604 021326
3605 021326 010061 000004
3606 021332 104412
3607 021334 122103
3608 021336 104412
3609 021340 021065
3610 021342 010005
3611 021344 116104 000005
3612 021350 120504
3613 021352 001401
3614 021354 104005

64\$: ST43: SCOPE ; *****
MOV #43,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #ST44,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #64\$,LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
MOV #3,R2 ; SAVE REGISTER ADDRESS FOR TYPEOUT
MOV #1,RO ; START WITH BIT 0
MOV RO,4(R1) ; PUT PATTERN INTO PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
122100!3 ; MOV DATA TO IBUS REGISTER 3
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
21005!<3*20> ; READ FROM IBUS REGISTER 3
MOV RO,R5 ; PUT EXPECTED IN R5
MOVB 5(R1),R4 ; PUT "FOUND" INTO R4
CMPB R5,R4 ; DATA CORRECT?
BEQ 65\$; BR IF YES
ERROR 5 ; ERROR
65\$: SCOPI ; SW09=1?
CLC ; CLEAR CARRY
ROLB RO ; SHIFT BIT IN RO
BNE 64\$; IF RO=0 THEN DONE
MOV #67\$,LOCK ; NEW SCOPI
MOV #1,RO ; START WITH BIT 0
69\$: COM RO ; CHANGE TO FLOATING ZERO
67\$: MOV RO,4(R1) ; PUT PATTERN INTO PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
122100!3 ; MOV DATA TO IBUS REGISTER 3
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
21005!<3*20> ; READ FROM IBUS REGISTER 3
MOV RO,R5 ; PUT EXPECTED IN R5
MOVB 5(R1),R4 ; PUT "FOUND" INTO R4
CMPB R5,R4 ; DATA CORRECT?
BEQ 68\$; BR IF YES
ERROR 5 ; ERROR

3615 021356 104405
3616 021360 005100
3617 021362 000241
3618 021364 106100
3619 021366 001356
3620
3621
3622
3623
3624
3625
3626
3627
3628
3629
3630
3631 021370 000004
3632 021372 012737 000044 001202
3633 021400 012737 021544 001442
3634 021406 012737 021426 001444
3635
3636 021414 104410
3637 021416 012702 000004
3638 021422 012700 000001
3639 021426
3640 021426 010061 000004
3641 021432 104412
3642 021434 122104
3643 021436 104412
3644 021440 021105
3645 021442 010005
3646 021444 116104 000005
3647 021450 120504
3648 021452 001401
3649 021454 104005
3650 021456 104405
3651 021460 000241
3652 021462 106100
3653 021464 001360
3654 021466 012737 021502 001444
3655 021474 012700 000001
3656 021500 005100
3657 021502
3658 021502 010061 000004
3659 021506 104412
3660 021510 122104
3661 021512 104412
3662 021514 021105
3663 021516 010005
3664 021520 116104 000005
3665 021524 120504
3666 021526 001401
3667 021530 104005
3668 021532 104405
3669 021534 005100
3670 021536 000241

```
68$: SCOPI ;SW09=1?
COM RO ;CHANGE TO FLOATING 1
CLC ;CLEAR CARRY
ROLB RO ;SHIFT BIT IN RO
BNE 69$ ;IF RO=0 THEN DONE

;***** TEST 44 *****
;MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
;FLOAT A 1 THROUGH IBUS REGISTER 4
;FLOAT A 0 THROUGH IBUS REGISTER 4
;*****

; TEST 44
-----
;*****
†ST44: SCOPE ;LOAD THE NO. OF THIS TEST
MOV #44,STSTNM ; POINT TO THE START OF NEXT TEST.
MOV #ST45,NEXT ; ADDRESS FOR LOCK ON DATA.
MOV #64$,LOCK ;R1 CONTAINS BASE KMC11 ADDRESS
;MASTER CLEAR KMC11
;SAVE REGISTER ADDRESS FOR TYPEOUT
;START WITH BIT 0

64$: MOV RO,4(R1) ;PUT PATTERN INTO PORT4
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
122100!4 ;MOV DATA TO IBUS REGISTER 4
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
21005!<4*20> ;READ FROM IBUS REGISTER 4
MOV RO,R5 ;PUT EXPECTED IN R5
MOVB 5(R1),R4 ;PUT "FOUND" INTO R4
CMPB R5,R4 ;DATA CORRECT?
BEQ 65$ ;BR IF YES
ERROR 5 ;ERROR

65$: SCOPI ;SW09=1?
CLC ;CLEAR CARRY
ROLB RO ;SHIFT BIT IN RO
BNE 64$ ;IF RO=0 THEN DONE
MOV #67$,LOCK ;NEW SCOPI
MOV #1,RO ;START WITH BIT 0
69$: COM RO ;CHANGE TO FLOATING ZERO
67$: MOV RO,4(R1) ;PUT PATTERN INTO PORT4
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
122100!4 ;MOV DATA TO IBUS REGISTER 4
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
21005!<4*20> ;READ FROM IBUS REGISTER 4
MOV RO,R5 ;PUT EXPECTED IN R5
MOVB 5(R1),R4 ;PUT "FOUND" INTO R4
CMPB R5,R4 ;DATA CORRECT?
BEQ 68$ ;BR IF YES
ERROR 5 ;ERROR

68$: SCOPI ;SW09=1?
COM RO ;CHANGE TO FLOATING 1
CLC ;CLEAR CARRY
```

3671 021540 106100
3672 021542 001356
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3684 021544 000004
3685 021546 012737 000045 001202
3686 021554 012737 021720 001442
3687 021562 012737 021602 001444
3688
3689 021570 104410
3690 021572 012702 000005
3691 021576 012700 000001
3692 021602
3693 021602 010061 000004
3694 021606 104412
3695 021610 122105
3696 021612 104412
3697 021614 021125
3698 021616 010005
3699 021620 116104 000005
3700 021624 120504
3701 021626 001401
3702 021630 104005
3703 021632 104405
3704 021634 000241
3705 021636 106100
3706 021640 001360
3707 021642 012737 021656 001444
3708 021650 012700 000001
3709 021654 005100
3710 021656
3711 021656 010061 000004
3712 021662 104412
3713 021664 122105
3714 021666 104412
3715 021670 021125
3716 021672 010005
3717 021674 116104 000005
3718 021700 120504
3719 021702 001401
3720 021704 104005
3721 021706 104405
3722 021710 005100
3723 021712 000241
3724 021714 106100
3725 021716 001356
3726

ROLB RO ;SHIFT BIT IN RO
BNE 69\$;IF RO=0 THEN DONE

***** TEST 45 *****
*MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
*FLOAT A 1 THROUGH IBUS REGISTER 5
*FLOAT A 0 THROUGH IBUS REGISTER 5

TEST 45

TST45: SCOPE ; LOAD THE NO. OF THIS TEST
MOV #45,STSTNM ; POINT TO THE START OF NEXT TEST.
MOV #TST46,NEXT ; ADDRESS FOR LOCK ON DATA.
MOV #64\$,LOCK ; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
MOV #5,R2 ; SAVE REGISTER ADDRESS FOR TYPEOUT
MOV #1,R0 ; START WITH BIT 0
64\$: MOV R0,4(R1) ; PUT PATTERN INTO PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
122100!5 ; MOV DATA TO IBUS REGISTER 5
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
21005!<5*20> ; READ FROM IBUS REGISTER 5
MOV R0,R5 ; PUT EXPECTED IN R5
MOVB 5(R1),R4 ; PUT "FOUND" INTO R4
CMPB R5,R4 ; DATA CORRECT?
BEQ 65\$; BR IF YES
ERROR 5 ; ERROR
65\$: SCOP1 ; SW09=1?
CLC ; CLEAR CARRY
ROLB RO ; SHIFT BIT IN RO
BNE 64\$; IF RO=0 THEN DONE
MOV #67\$,LOCK ; NEW SCOP1
MOV #1,R0 ; START WITH BIT 0
69\$: COM RO ; CHANGE TO FLOATING ZERO
67\$: MOV R0,4(R1) ; PUT PATTERN INTO PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
122100!5 ; MOV DATA TO IBUS REGISTER 5
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
21005!<5*20> ; READ FROM IBUS REGISTER 5
MOV R0,R5 ; PUT EXPECTED IN R5
MOVB 5(R1),R4 ; PUT "FOUND" INTO R4
CMPB R5,R4 ; DATA CORRECT?
BEQ 68\$; BR IF YES
ERROR 5 ; ERROR
68\$: SCOP1 ; SW09=1?
COM RO ; CHANGE TO FLOATING 1
CLC ; CLEAR CARRY
ROLB RO ; SHIFT BIT IN RO
BNE 69\$; IF RO=0 THEN DONE

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3737 021720 000004
3738 021722 012737 000046 001202
3739 021730 012737 022074 001442
3740 021736 012737 021756 001444
3741
3742 021744 104410
3743 021746 012702 000006
3744 021752 012700 000001
3745 021756
3746 021756 010061 000004
3747 021762 104412
3748 021764 122106
3749 021766 104412
3750 021770 021145
3751 021772 010005
3752 021774 116104 000005
3753 022000 120504
3754 022002 001401
3755 022004 104005
3756 022006 104405
3757 022010 000241
3758 022012 106100
3759 022014 001360
3760 022016 012737 022032 001444
3761 022024 012700 000001
3762 022030 005100
3763 022032
3764 022032 010061 000004
3765 022036 104412
3766 022040 122106
3767 022042 104412
3768 022044 021145
3769 022046 010005
3770 022050 116104 000005
3771 022054 120504
3772 022056 001401
3773 022060 104005
3774 022062 104405
3775 022064 005100
3776 022066 000241
3777 022070 106100
3778 022072 001356
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***** TEST 46 *****
;MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
;FLOAT A 1 THROUGH IBUS REGISTER 6
;FLOAT A 0 THROUGH IBUS REGISTER 6
*****

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TEST 46

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TST46: SCOPE
MOV #46,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST47,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #64$,LOCK ; ADDRESS FOR LOCK ON DATA.

;R1 CONTAINS BASE KMC11 ADDRESS
;MASTER CLEAR KMC11
;SAVE REGISTER ADDRESS FOR TYPEOUT
;START WITH BIT 0

64$: MOV R0,4(R1) ; PUT PATTERN INTO PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
122100!6 ; MOV DATA TO IBUS REGISTER 6
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
21005!<6*20> ; READ FROM IBUS REGISTER 6
MOV R0,R5 ; PUT EXPECTED IN R5
MOVB 5(R1),R4 ; PUT "FOUND" INTO R4
CMPB R5,R4 ; DATA CORRECT?
BEQ 65$ ; BR IF YES
ERROR 5 ; ERROR
65$: SCOP1 ; SW09=1?
CLC ; CLEAR CARRY
ROLB R0 ; SHIFT BIT IN R0
BNE 64$ ; IF R0=0 THEN DONE
MOV #67$,LOCK ; NEW SCOP1
MOV #1,R0 ; START WITH BIT 0
69$: COM R0 ; CHANGE TO FLOATING ZERO
67$: MOV R0,4(R1) ; PUT PATTERN INTO PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
122100!6 ; MOV DATA TO IBUS REGISTER 6
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
21005!<6*20> ; READ FROM IBUS REGISTER 6
MOV R0,R5 ; PUT EXPECTED IN R5
MOVB 5(R1),R4 ; PUT "FOUND" INTO R4
CMPB R5,R4 ; DATA CORRECT?
BEQ 68$ ; BR IF YES
ERROR 5 ; ERROR
68$: SCOP1 ; SW09=1?
COM R0 ; CHANGE TO FLOATING 1
CLC ; CLEAR CARRY
ROLB R0 ; SHIFT BIT IN R0
BNE 69$ ; IF R0=0 THEN DONE

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***** TEST 47 *****
;MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST

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KMC11 MICRO PROCESSOR IBUS TESTS

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3790 022074 000004
3791 022076 012737 000047 001202
3792 022104 012737 022250 001442
3793 022112 012737 022132 001444
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3795 022120 104410
3796 022122 012702 000007
3797 022126 012700 000001
3798 022132
3799 022132 010061 000004
3800 022136 104412
3801 022140 122107
3802 022142 104412
3803 022144 021165
3804 022146 010005
3805 022150 116104 000005
3806 022154 120504
3807 022156 001401
3808 022160 104005
3809 022162 104405
3810 022164 000241
3811 022166 106100
3812 022170 001360
3813 022172 012737 022206 001444
3814 022200 012700 000001
3815 022204 005100
3816 022206
3817 022206 010061 000004
3818 022212 104412
3819 022214 122107
3820 022216 104412
3821 022220 021165
3822 022222 010005
3823 022224 116104 000005
3824 022230 120504
3825 022232 001401
3826 022234 104005
3827 022236 104405
3828 022240 005100
3829 022242 000241
3830 022244 106100
3831 022246 001356
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; *FLOAT A 1 THROUGH IBUS REGISTER 7
; *FLOAT A 0 THROUGH IBUS REGISTER 7
; *****
; TEST 47
; -----
; *****
↑ST47: SCOPE
MOV #47,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST50,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #64$,LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
MOV #7,R2 ; SAVE REGISTER ADDRESS FOR TYPEOUT
MOV #1,R0 ; START WITH BIT 0
64$: MOV R0,4(R1) ; PUT PATTERN INTO PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
122100!7 ; MOV DATA TO IBUS REGISTER 7
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
21005!(<7*20) ; READ FROM IBUS REGISTER 7
MOV R0,R5 ; PUT EXPECTED IN R5
MOVB 5(R1),R4 ; PUT "FOUND" INTO R4
CMPB R5,R4 ; DATA CORRECT?
BEQ 65$ ; BR IF YES
ERROR 5 ; ERROR
65$: SCOP1 ; SW09=1?
CLC ; CLEAR CARRY
ROLB R0 ; SHIFT BIT IN R0
BNE 64$ ; IF R0=0 THEN DONE
MOV #67$,LOCK ; NEW SCOP1
MOV #1,R0 ; START WITH BIT 0
69$: COM R0 ; CHANGE TO FLOATING ZERO
67$: MOV R0,4(R1) ; PUT PATTERN INTO PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
122100!7 ; MOV DATA TO IBUS REGISTER 7
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
21005!(<7*20) ; READ FROM IBUS REGISTER 7
MOV R0,R5 ; PUT EXPECTED IN R5
MOVB 5(R1),R4 ; PUT "FOUND" INTO R4
CMPB R5,R4 ; DATA CORRECT?
BEQ 68$ ; BR IF YES
ERROR 5 ; ERROR
68$: SCOP1 ; SW09=1?
COM R0 ; CHANGE TO FLOATING 1
CLC ; CLEAR CARRY
ROLB R0 ; SHIFT BIT IN R0
BNE 69$ ; IF R0=0 THEN DONE
; ***** TEST 50 *****
; *MICRO PROCESSOR IBUS DUAL ADDRESS TEST
; *WRITE ALL IBUS REGISTERS WITH INCREMENTING PATTERN
; *READ ALL IBUS REGISTERS TO VERIFY CORRECT ADDRESSING
; *****

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022250 000004
022252 012737 000050 001202
022260 012737 022476 001442
022266 012737 022304 001444

022274 104410
022276 012700 000001
022302 005002
022304 010203
022306 010061 000004
022312 042737 000017 022326
022320 050337 022326
022324 104412
022326 122100
022330 006303
022332 006303
022334 006303
022336 006303
022340 042737 000360 022354
022346 050337 022354
022352 104412
022354 021005
022356 010005
022360 116104 000005
022364 120504
022366 001401
022370 104005
022372 104405
022374 005200
022376 005202
022400 022702 000010
022404 001337
022406 012737 022424 001444
022414 012700 000001
022420 005002
022422 005003
022424 042737 000360 022440
022432 050337 022440
022436 104412
022440 021005
022442 010005
022444 116104 000005
022450 120504
022452 001401
022454 104005
022456 104405
022460 005200
022462 005202
022464 062703 000020
022470 022702 000010
022474 001353

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; TEST 50
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*****
†ST50: SCOPE
MOV #50,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST51,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.

;R1 CONTAINS BASE KMC11 ADDRESS
;MASTER CLEAR KMC11
;START WITH A ONE
;R2 CONTAINS ADDRESS OF REGISTER
;R3=REGISTER ADDRESS
;WRITE DATA TO PORT4
;CLEAR ADDRESS FIELD OF INSTRUCTION
;ADD ADDRESS TO INSTRUCTION
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;MOVE DATA TO IBUS REGISTER
;SHIFT ADDRESS
;4 TIMES TO GET
;IT TO BITS 4-7
;OF NEXT INSTRUCTION
;CLEAR ADDRESS FIELD
;ADD ADDRESS TO INSTRUCTION
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;READ FROM IBUS REGISTER
;PUT "EXPECTED" IN R5
;PUT "FOUND" IN R4
;IS DATA CORRECT?
;BR IF YES
;DATA ERROR
;SW09=1?
;INCREMENT PATTERN
;INCREMENT REGISTER ADDRESS
;LAST ADDRESS DONE?
;BR IF NO
;NEW SCOPI
;RESTART PATTERN TO 1
;RESTART AT ADDRESS 0
;RESTART AT ADDRESS 0
;CLEAR ADDRESS FIELD OF INSTRUCTION
;ADD ADDRESS TO INSTRUCTION
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;READ FROM IBUS REGISTER
;PUT "EXPECTED" IN R5
;PUT "FOUND" IN R4
;DATA CORRECT?
;BR IF YES
;DUAL ADDRESSING ERROR
;SW09=1?
;INCREMENT PATTERN
;NEXT ADDRESS
;ADD 1 TO ADDRESS IN R3(SHIFTED 4 TIMES)
;BR IF NO

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***** TEST 51 *****
*MICRO PROCESSOR BR REGISTER TEST
*FLOAT A 1 THROUGH THE BR
*FLOAT A 0 THROUGH THE BR

TEST 51

```

*****
TST51: SCOPE
MOV #51,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST52,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #64$,LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
; MASTER CLEAR KMC11
; START PATTERN WITH BIT0
64$: MOV R0,4(R1) ; WRITE PATTERN IN PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
120500 ; MOVE DATA TO THE BR REGISTER
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
061225 ; MOVE BR TO PORT 5
MOV R0,R5 ; PUT "EXPECTED" IN R5
MOVVB 5(R1),R4 ; PUT "FOUND" IN R4
CMPB R5,R4 ; DATA CORRECT?
BEQ 65$ ; BR IF YES
ERROR 6 ; DATA ERROR
65$: SCOP1
CLC ; CLEAR CARRY
ROLB R0 ; SHIFT BIT IN R0
BNE 64$ ; DONE IF R0=0
MOV #67$,LOCK ; NEW SCOP1
MOV #1,R0 ; START PATTERN WITH BIT0
69$: COM R0 ; CHANGE TO FLOATING ZERO
67$: MOV R0,4(R1) ; WRITE PATTERN IN PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
120500 ; MOVE DATA TO THE BR REGISTER
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
061225 ; MOVE BR TO PORT 5
MOV R0,R5 ; PUT "EXPECTED" IN R5
MOVVB 5(R1),R4 ; PUT "FOUND" IN R4
CMPB R5,R4 ; DATA CORRECT?
BEQ 68$ ; BR IF YES
ERROR 6 ; DATA ERROR
68$: SCOP1
COM R0 ; CHANGE BACK TO A ONE
CLC ; CLEAR CARRY
ROLB R0 ; SHIFT BIT IN R0
BNE 69$ ; DONE IF R0=0

```

***** TEST 52 *****
*SCRATCH PAD TEST

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3951 ;#FLOAT A 1 THROUGH EACH SCRATCH PAD LOCATION
3952 ;#FLOAT A 0 THROUGH EACH SCRATCH PAD LOCATION
3953 ;:*****
3954 ;
3955 ; TEST 52
3956 ;-----
3957 ;:*****
3958 022646 000004 000052 001202 TST52: SCOPE
3959 022650 012737 000052 001202 MOV #52,$STNM ; LOAD THE NO. OF THIS TEST
3960 022656 012737 023114 001442 MOV #TST53,NEXT ; POINT TO THE START OF NEXT TEST.
3961 022664 012737 022702 001444 MOV #64$,LOCK ; ADDRESS FOR LOCK ON DATA.
3962 ;
3963 022672 104410 MSTCLR ; R1 CONTAINS BASE KMC11 ADDRESS
3964 022674 005002 CLR R2 ; MASTER CLEAR KMC11
3965 022676 012700 000001 MOV #1,R0 ; START AT ADDRESS ZERO
3966 022702 042737 000017 022722 64$: BIC #17,65$ ; START WITH BIT0
3967 022710 050237 022722 BIC #17,65$ ; CLEAR ADDRESS FIELD OF INSTRUCTION
3968 022714 010061 000004 MOV R2,65$ ; ADD ADDRESS TO INSTRUCTION
3969 022720 104412 ROMCLK ; WRITE PATTERN TO PORT4
3970 022722 123100 65$: 123100 ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3971 022724 042737 000017 022740 BIC #17,66$ ; WRITE SCRATCH PAD(ADDRESS IN R2)
3972 022732 050237 022740 BIS R2,66$ ; CLEAR ADDRESS FIELD OF INSTRUCTION
3973 022736 104412 ROMCLK ; ADD ADDRESS TO INSTRUCTION
3974 022740 040600 66$: 040600 ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3975 022742 104412 ROMCLK ; MOV SP TO BR
3976 022744 061225 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3977 022746 010005 MOV R0,R5 ; MOVE BR TO PORT5
3978 022750 116104 000005 MOVB 5(R1),R4 ; PUT "EXPECTED" IN R5
3979 022754 120504 CMPB R5,R4 ; PUT "FOUND" IN R4
3980 022756 001401 BEQ 67$ ; DATA CORRECT
3981 022760 104007 ERROR 7 ; BR IF YES
3982 022762 104405 67$: SCOP1 ; DATA ERROR
3983 022764 000241 CLC ; SWD9=1?
3984 022766 106100 ROLB R0 ; CLEAR CARRY
3985 022770 001344 BNE 64$ ; SHIFT BIT IN R0
3986 022772 012737 023006 001444 MOV #69$,LOCK ; DONE IF R0=0
3987 023000 012700 000001 MOV #1,R0 ; NEW SCOP1
3988 023004 005100 73$: COM R0 ; START WITH BIT0
3989 023006 042737 000017 023026 69$: BIC #17,70$ ; CHANGE TO FLOATING ZERO
3990 023014 050237 023026 BIS R2,70$ ; CLEAR ADDRESS FIELD OF INSTRUCTION
3991 023020 010061 000004 MOV R0,4(R1) ; ADD ADDRESS TO INSTRUCTION
3992 023024 104412 ROMCLK ; WRITE PATTERN TO PORT4
3993 023026 123100 70$: 123100 ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3994 023030 042737 000017 023044 BIC #17,71$ ; WRITE SCRATCH PAD(ADDRESS IN R2)
3995 023036 050237 023044 BIS R2,71$ ; CLEAR ADDRESS FIELD OF INSTRUCTION
3996 023042 104412 ROMCLK ; ADD ADDRESS TO INSTRUCTION
3997 023044 040600 71$: 040600 ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3998 023046 104412 ROMCLK ; MOV SP TO BR
3999 023050 061225 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4000 023052 010005 MOV R0,R5 ; MOVE BR TO PORT5
4001 023054 116104 000005 MOVB 5(R1),R4 ; PUT "EXPECTED" IN R5
4002 023060 120504 CMPB R5,R4 ; PUT "FOUND" IN R4
4003 023062 001401 BEQ 72$ ; DATA CORRECT
4004 023064 104007 ERROR 7 ; BR IF YES
4005 023066 104405 72$: SCOP1 ; DATA ERROR
4006 023070 005100 COM R0 ; SWD9=1?
;CHANGE BACK TO A ONE

```

4007 023072 000241
4008 023074 106100
4009 023076 001342
4010 023100 012700 000001
4011 023104 005202
4012 023106 022702 000020
4013 023112 001273

CLC ; CLEAR CARRY
ROLB RO ; SHIFT BIT IN RO
BNE 73\$; DONE IF RO=0
MOV #1,RO ; RESTART AT BIT 0
INC R2 ; NEXT SP ADDRESS
CMP #20,R2 ; LAST ADDRESS?
BNE 64\$; BR IF NO

***** TEST 53 *****
*SCRATCH PAD DUAL ADDRESSING TEST
*WRITE AN INCREMENTING PATTERN IN ALL SP LOCATIONS
*READ ALL SP LOCATIONS TO VERIFY CORRECT ADDRESSING

TEST 53

4025 023114 000004
4026 023116 012737 000053 001202
4027 023124 012737 023336 001442
4028 023132 012737 023150 001444
4030 023140 104410
4031 023142 012700 000001
4032 023146 005003
4033 023150 010302
4034 023152 042737 000017 023172
4035 023160 050237 023172
4036 023164 010061 000004
4037 023170 104412
4038 023172 123100
4039 023174 042737 000017 023210
4040 023202 050237 023210
4041 023206 104412
4042 023210 060600
4043 023212 104412
4044 023214 061225
4045 023216 010005
4046 023220 116104 000005
4047 023224 120504
4048 023226 001401
4049 023230 104007
4050 023232 104405
4051 023234 005200
4052 023236 005203
4053 023240 022703 000020
4054 023244 001341
4055 023246 012737 023262 001444
4056 023254 012700 000001
4057 023260 005003
4058 023262 010302
4059 023264 042737 000017 023300
4060 023272 050237 023300
4061 023276 104412
4062 023300 060600

TST53: SCOPE ;
MOV #53,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST54,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1\$,LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
MOV #1,RO ; START WITH A 1
CLR R3 ; ADDRESS 0
1\$: MOV R3,R2 ; MOVE ADDRESS TO R2
BIC #17,2\$; CLEAR ADDRESS FIELD
BIS R2,2\$; ADD ADDRESS TO INSTRUCTION
MOV RO,4(R1) ; WRITE PATTERN TO PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
123100 ; WRITE SP(ADDRESS IN R2)
2\$: BIC #17,3\$; CLEAR ADDRESS FIELD OF INSTRUCTION
BIS R2,3\$; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3\$: 60600 ; MOV SP TO BR
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
61225 ; MOV BR TO PORTS
MOV RO,R5 ; PUT "EXPECTED" IN R5
MOVB 5(R1),R4 ; PUT "FOUND" IN R4
CMPB R5,R4 ; DATA CORRECT?
BEQ 4\$; BR IF YES
ERROR 7 ; DATA ERROR
4\$: SCOP1 ; SMO9=0
INC RO ; INCREMENT PATTERN
INC R3 ; NEXT ADDRESS
CMP #20,R3 ; LAST ADDRESS DONE?
BNE 1\$; BR IF NO
MOV #5\$,LOCK ; NEW SCOP1
MOV #1,RO ; RESTART PATTERN AT 1
CLR R3 ; RESTART AT ADDRESS ZERO
5\$: MOV R3,R2 ; PUT ADDRESS IN R2
BIC #17,6\$; CLEAR ADDRESS FIELD OF INSTRUCTION
BIS R2,6\$; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6\$: 60600 ; MOV SP TO BR


```

4063 023302 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4064 023304 061225 61225 ;MOV BR TO PORTS
4065 023306 010005 MOV R0,R5 ;PUT "EXPECTED" IN R5
4066 023310 116104 000005 MOV# 5(R1),R4 ;PUT "FOUND" IN R4
4067 023314 120504 CMPB R5,R4 ;DATA CORRECT?
4068 023316 001401 BEQ 7$ ;BR IF YES
4069 023320 104007 ERROR 7 ;SP ADDRESSING ERROR
4070 023322 104405 7$: SCOP1 ;SW09=1?
4071 023324 005200 INC R0 ;INCREMENT PATTERN
4072 023326 005203 INC R3 ;NEXT ADDRESS
4073 023330 022703 000020 CMP #20,R3 ;LAST ADDRESS DONE?
4074 023334 001352 BNE 5$ ;BR IF NO

```

```

;***** TEST 54 *****
;*INTERRUPT TEST
;*TEST THAT DEVICE CAN INTERRUPT TO VECTOR A
;*****

```

TEST 54

```

4084 023336 000004 000004 001202 1$: SCOP1
4085 023340 012737 000054 001202 MOV #54,$STSTNM ; LOAD THE NO. OF THIS TEST
4086 023346 012737 023432 001442 MOV #TST55,NEXT ; POINT TO THE START OF NEXT TEST.
4087 ; R1 CONTAINS BASE KMC11 ADDRESS
4088 RESET ;BUS RESET
4089 CLR (R1) ;CLEAR RUN
4090 JSR R5,SETVEC ;SET UP VECTORS
4091 3$ ;XX0
4092 2$ ;XX4
4093 .BYTE 340,340 ;LEVEL 7
4094 MOV #340,PS ;PS = LEVEL 7
4095 MOV #200,4(R1) ;WRITE PORT4
4096 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4097 121111 ;SET BR R0 IN IBUS* REG 11
4098 CLR PS ;ALLOW INTERRUPT
4099 NOP
4100 ERROR 10 ;NO INTERRUPT
4101 BR 4$
4102 ERROR 11 ;WRONG VECTOR
4103 MOV #STACK,SP ;RESET STACK
4104
4105
4106
4107

```

```

;***** TEST 55 *****
;*INTERRUPT TEST
;*TEST THAT DEVICE CAN INTERRUPT TO VECTOR B
;*****

```

TEST 55

```

4115 023432 000004 000004 001202 1$: SCOP1
4116 023434 012737 000055 001202 MOV #55,$STSTNM ; LOAD THE NO. OF THIS TEST
4117 023442 012737 023524 001442 MOV #TST56,NEXT ; POINT TO THE START OF NEXT TEST.
4118

```

```

4119                                     ;R1 CONTAINS BASE KMC11 ADDRESS
4120 023450 104410 MSTCLR ;MASTER CLEAR KMC11
4121 023452 004537 035516 JSR R5,SETVEC ;SET UP VECTORS
4122 023456 023516 2$ ;XX0
4123 023460 023520 3$ ;XX4
4124 023462 340 340 .BYTE 340,340 ;LEVEL 7
4125 023464 012737 000340 177776 1$: MOV #340,PS ;PS = LEVEL 7
4126 023472 012761 000300 000004 MOV #300,4(R1) ;WRITE PORT4
4127 023500 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4128 023502 121111 121111 ;SET BR RQ IN IBUS* REG 11
4129 023504 005037 177776 CLR PS ;ALLOW INTERRUPT
4130 023510 000240 NOP ;NO INTERRUPT
4131 023512 104010 ERROR 10 ;NO INTERRUPT
4132 023514 000403 BR 4$
4133 023516 104011 2$: ERROR 11 ;WRONG VECTOR
4134 023520 012706 001200 3$: MOV #STACK,SP ;RESET STACK
4135 023524 4$:

```

```

4136
4137
4138 ;***** TEST 56 *****
4139 ;*PRIORITY INTERRUPT TESTS
4140 ;*SET PS TO ALL BR LEVELS EQUAL OR GREATER THAN
4141 ;*THE KMC11 LEVEL, VERIFY THAT KMC11 DOES NOT INTERRUPT
4142 ;*****
4143

```

```

4144 ; TEST 56
4145 -----

```

```

4146 ;*****
4147 023524 000004 TST56: SCOPE
4148 023526 012737 000056 001202 MOV #56,$TSTNM ; LOAD THE NO. OF THIS TEST
4149 023534 012737 023646 001442 MOV #TST57,NEXT ; POINT TO THE START OF NEXT TEST.
4150                                     ;R1 CONTAINS BASE KMC11 ADDRESS
4151 023542 104410 MSTCLR ;MASTER CLEAR KMC11
4152 023544 012702 000340 MOV #340,R2 ;PUT LEVEL 7 IN R2
4153 023550 010237 177776 MOV R2,PS ;SET PRIORITY TO 7
4154 023554 013700 002050 MOV STAT1,R0 ;GET BR LEVEL OF KMC11
4155 023560 006200 ASR R0 ;SHIFT R0 4 TIMES
4156 023562 006200 ASR R0 ;TO GET PROPER LEVEL
4157 023564 006200 ASR R0
4158 023566 006200 ASR R0
4159 023570 042700 177437 BIC #177437,R0 ;CLEAR UNWANTED BITS
4160 023574 004537 035516 JSR R5,SETVEC ;SET UP VECTORS
4161 023600 023642 2$ ;A VECTOR
4162 023602 023642 2$ ;B VECTOR
4163 023604 340 340 .BYTE 340,340 ;PRIORITY 7
4164 023606 012761 000200 000004 4$: MOV #200,4(R1) ;LOAD PORT4
4165 023614 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4166 023616 121111 121111 ;SET BR REQUEST
4167 023620 010237 177776 5$: MOV R2,PS ;PUT LEVEL IN R2 IN PS
4168 023624 000240 NOP
4169 023626 020002 CMP R0,R2 ;IS PRESENT PS LEVEL = TO KMC LEVEL
4170 023630 001403 BEQ 1$ ;BR IF YES
4171 023632 162702 000040 SUB #40,R2 ;NO GET NEXT LOWER LEVEL IN R2
4172 023636 000770 BR 5$ ;AND CONTINUE WITH TEST
4173 023640 104420 1$: ADVANCE ;ADVANCE LOOP
4174 023642 104020 2$: ERROR 20 ;ERROR UNEXPECTED INTERRUPT

```

4175 023644 000002

RTI

4176
4177
4178
4179
4180
4181
4182
4183
4184
4185
4186
4187 023646 000004
4188 023650 012737 000057 001202
4189 023656 012737 024014 001442
4190
4191 023664 104410
4192 023666 012702 000340
4193 023672 010237 177776
4194 023676 013700 002050
4195 023702 006200
4196 023704 006200
4197 023706 006200
4198 023710 006200
4199 023712 042700 177437
4200 023716 010002
4201 023720 162702 000040
4202 023724 004537 035516
4203 023730 023776
4204 023732 024004
4205 023734 340 340
4206 023736 012761 000200 000004 4S:
4207 023744 104412
4208 023746 121111
4209 023750 010237 177776 5S:
4210 023754 000240
4211 023756 104010
4212 023760 022702 000140 6S:
4213 023764 001403
4214 023766 162702 000040
4215 023772 000761
4216 023774 104420 1S:
4217 023776 012716 023760 2S:
4218 024002 000002
4219 024004 104011 3S:
4220 024006 012716 023760
4221 024012 000002
4222
4223
4224
4225
4226
4227
4228
4229
4230

***** TEST 57 *****
: *PRIORITY INTERRUPT TESTS
: *SET PS TO ALL BR LEVELS LESS THAN THE KMC11 LEVEL
: *VERIFY THAT THE KMC11 WILL INTERRUPT
: *****

: TEST 57
:-----

1ST57: SCOPE ; LOAD THE NO. OF THIS TEST
MOV #57,STSTNM ; POINT TO THE START OF NEXT TEST.
MOV #ST56,NEXT ; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
MOV #340,R2 ; PUT LEVEL 7 IN R2
MOV R2,PS ; SET PRIORITY TO 7
MOV STAT1,R0 ; GET BR LEVEL OF KMC11
ASR R0 ; SHIFT R0 4 TIMES
ASR R0 ; TO GET PROPER LEVEL
ASR R0
BIC #177437,R0 ; CLEAR UNWANTED BITS
MOV R0,R2 ; PUT KMC LEVEL IN R2
SUB #40,R2 ; GET NEXT LOWER LEVEL IN R2
JSR R5,SETVEC ; SET UP VECTORS
2S ; A VECTOR
3S ; B VECTOR
.BYTE 340,340 ; PRIORITY 7
MOV #200,4(R1) ; LOAD PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
121111 ; SET BR REQUEST
5S: MOV R2,PS ; PUT LEVEL IN R2 IN PS
NOP
4211: ERROR 10 ; ERROR, NO INTERRUPT
6S: CMP #140,R2 ; IS IT DOWN TO LEVEL 3 YET?
BEQ 1S ; YES, KMC DID NOT INTERRUPT, ERROR
SUB #40,R2 ; PUT NEXT LOWER LEVEL IN R2
BR 4S ; CONTINUE TEST
1S: ADVANCE ; ADVANCE LOOP
2S: MOV #6S,(SP) ; SET UP FOR RTI
RTI
3S: ERROR 11 ; ERROR, WRONG VECTOR
MOV #6S,(SP) ; SET UP FOR RTI
RTI

***** TEST 60 *****
: *NPR TEST
: *TEST OF DATO, 1 WORD FROM UPROC TO 11 MEMORY
: *****

: TEST 60
:-----

```

4231
4232 024014 000004
4233 024016 012737 000060 001202
4234 024024 012737 024122 001442
4235
4236 024032 000005
4237 024034 005011
4238 024036 005061 000004
4239 024042 004537 035540
4240 024046 000000
4241 024050 177777
4242 024052 024120
4243 024054 024116
4244 024056 005037 024116
4245 024062 012761 000021 000004
4246 024070 104412
4247 024072 121110
4248 024074 000240
4249 024076 012705 177777
4250 024102 013704 024116
4251 024106 020504
4252 024110 001401
4253 024112 104012
4254 024114 104420
4255 024116 000000
4256 024120 000000
4257
4258
4259
4260
4261
4262
4263
4264
4265
4266
4267 024122 000004
4268 024124 012737 000061 001202
4269 024132 012737 024240 001442
4270
4271 024140 104410
4272 024142 005061 000004
4273 024146 004537 035540
4274 024152 000000
4275 024154 177777
4276 024156 024236
4277 024160 024234
4278 024162 012737 177777 024236
4279 024170 012761 000001 000004
4280 024176 104412
4281 024200 121110
4282 024202 000240
4283 024204 012705 177777
4284 024210 104412
4285 024212 021004
4286 024214 104412

```

```

*****
†ST60: SCOPE
MOV #60,$STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST61,NEXT ; POINT TO THE START OF NEXT TEST.
; R1 CONTAINS BASE KMC11 ADDRESS
RESET ; BUS RESET
CLR (R1) ; CLEAR RUN
CLR 4(R1) ; CLR PORT4
JSR R5,NPRSET ; SET UP IBUS REG 0-7
0 ; IN DATA
-1 ; OUT DATA
3$ ; IN BA
2$ ; OUT BA
CLR 2$ ; CLEAR 2$
MOV #21,4(R1) ; WRITE PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
121110 ; SET NPR BITS IN IBUS* REG 11
NOP
MOV #-1,R5 ; PUT "EXPECTED" IN R5
MOV 2$,R4 ; PUT "FOUND" IN R4
CMP R5,R4 ; DATA CORRECT?
BEQ 4$ ; BR IF YES
ERROR 12 ; ERROR NPR FAILED
4$: ADVANCE ; ADVANCE LOOP
2$: 0 ; OUT BA
3$: 0 ; IN BA

```

```

***** TEST 61 *****
; *NPR TEST
; *TEST OF DAT1, 1 WORD FROM 11 MEMORY TO UPROC
; *****

```

TEST 61

```

4267 024122 000004
4268 024124 012737 000061 001202
4269 024132 012737 024240 001442
4270
4271 024140 104410
4272 024142 005061 000004
4273 024146 004537 035540
4274 024152 000000
4275 024154 177777
4276 024156 024236
4277 024160 024234
4278 024162 012737 177777 024236
4279 024170 012761 000001 000004
4280 024176 104412
4281 024200 121110
4282 024202 000240
4283 024204 012705 177777
4284 024210 104412
4285 024212 021004
4286 024214 104412

```

```

*****
†ST61: SCOPE
MOV #61,$STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST62,NEXT ; POINT TO THE START OF NEXT TEST.
; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
CLR 4(R1) ; CLR PORT4
JSR R5,NPRSET ; SET UP IBUS REG 0-7
0 ; IN DATA
-1 ; OUT DATA
3$ ; IN BA
2$ ; OUT BA
MOV #-1,3$ ; PUT DATA IN 3$
MOV #1,4(R1) ; WRITE PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
121110 ; SET NPR BITS IN IBUS* REG 11
NOP
MOV #-1,R5 ; PUT "EXPECTED" IN R5
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
021004 ; MOVE IN DATA LOW BYTE TO PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

```

```

4287 024216 021025          021025          ;MOVE IN DATA HIGH BYTE TO PORTS
4288 024220 016104 000004  MOV      4(R1),R4          ;PUT "FOUND" IN R4
4289 024224 020504          CMP      R5,R4           ;DATA CORRECT?
4290 024226 001401          BEQ     4$              ;BR IF YES
4291 024230 104012          ERROR   12             ;ERROR NPR FAILED
4292 024232 104420          4$:    ADVANCE         ;ADVANCE LOOP
4293 024234 000000          2$:    0                ;OUT BA
4294 024236 000000          3$:    0                ;IN BA

```

```

4295
4296
4297 ;***** TEST 62 *****
4298 ;*NPR TEST
4299 ;*TEST OF DATOB, 1 BYTE FROM UPROC TO 11 MEMORY
4300 ;*****
4301

```

```

4302 ; TEST 62
4303 ;-----

```

```

4304 ;*****
4305 024240 000004          †ST62: SCOPE
4306 024242 012737 000062 001202  MOV      #62,$STSTNM      ; LOAD THE NO. OF THIS TEST
4307 024250 012737 024344 001442  MOV      #TST63,NEXT     ; POINT TO THE START OF NEXT TEST.
4308 ;*****
4309 024256 104410          MSTCLR          ;R1 CONTAINS BASE KMC11 ADDRESS
4310 024260 005061 000004  CLR      4(R1)         ;MASTER CLEAR KMC11
4311 024264 004537 035540  JSR     R5,NPRSET      ;CLR PORT4
4312 024270 000000          0              ;SET UP IBUS REG 0-7
4313 024272 177777          -1             ;IN DATA
4314 024274 024342          3$            ;OUT DATA
4315 024276 024341          2$+1          ;IN BA
4316 024300 005037 024340  CLR      2$           ;OUT BA
4317 024304 012761 000221 000004  MOV      #221,4(R1)      ;CLEAR 2$
4318 024312 104412          ROMCLK         ;WRITE PORT4
4319 024314 121110          121110        ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4320 024316 000240          NOP            ;SET NPR BITS IN IBUS* REG 11
4321 024320 012705 177400  MOV      #177400,R5      ;PUT "EXPECTED" IN R5
4322 024324 013704 024340  MOV      2$,R4          ;PUT "FOUND" IN R4
4323 024330 020504          CMP      R5,R4         ;DATA CORRECT?
4324 024332 001401          BEQ     4$           ;BR IF YES
4325 024334 104012          ERROR   12             ;ERROR NPR FAILED
4326 024336 104420          4$:    ADVANCE         ;ADVANCE LOOP
4327 024340 000000          2$:    0                ;OUT BA
4328 024342 000000          3$:    0                ;IN BA
4329
4330

```

```

4331 ;***** TEST 63 *****
4332 ;*TEST OF EA BITS 16 AND 17
4333 ;*DO A DATO TO AN ADDRESS USING OUT BA BITS 16 AND 17
4334 ;*VERIFY CORRECT RESULTS
4335 ;*****
4336

```

```

4337 ; TEST 63
4338 ;-----

```

```

4339 ;*****
4340 024344 000004          †ST63: SCOPE
4341 024346 012737 000063 001202  MOV      #63,$STSTNM      ; LOAD THE NO. OF THIS TEST
4342 024354 012737 024502 001442  MOV      #TST64,NEXT     ; POINT TO THE START OF NEXT TEST.

```

```

4343                                     ;R1 CONTAINS BASE KMC11 ADDRESS
4344 024362 104410 MSTCLR ;MASTER CLEAR KMC11
4345 024364 013737 002074 024412 MOV KMP04,15 ;USE SEL4 FOR ADDRESS
4346 024372 013737 002074 024410 MOV KMP04,25 ;USE SEL4 FOR ADDRESS
4347 024400 004537 035540 JSR R5,NPRSET ;LOAD BA AND DATA
4348 024404 000000 0 ;IN DATA
4349 024406 125252 0 ;OUT DATA
4350 024410 000000 2S: 0 ;IN BA
4351 024412 000000 1S: 0 ;OUT BA
4352 024414 012761 000014 000004 MOV #14,4(R1) ;LOAD SEL 4 WITH OUT BA16 AND 17
4353 024422 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4354 024424 121111 121111 ;SET OUTBA 16 AND 17
4355 024426 012761 000021 000004 MOV #21,4(R1) ;LOAD SEL4
4356 024434 012761 121110 000006 MOV #121110,6(R1) ;PUT INSTRUCTION IN SEL6
4357 024442 012711 003000 MOV #BIT9!BIT10,(R1) ;SET CROMI AND CROMO!!
4358 024446 052711 000400 BIS #BIT8,(R1) ;CLOCK IT!
4359 024452 000240 NOP ;WAIT FOR NPR
4360 024454 012705 121110 MOV #121110,R5 ;PUT "EXPECTED" IN R5
4361 024460 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4362 024462 021044 021044 ;MOVE OUT DATA LB TO SEL4
4363 024464 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4364 024466 021065 021065 ;MOVE OUT DATA HB TO SEL5
4365 024470 016104 000004 MOV 4(R1),R4 ;PUT "FOUND" IN R4
4366 024474 020504 CMP R5,R4 ;CORRECT RESULTS ?
4367 024476 001401 BEQ 3S ;BR IF YES
4368 024500 104012 ERROR 12 ;ERROR BA 16 AND 17 FAILED
4369 024502 3S:

```

```

4370
4371
4372 ;***** TEST 64 *****
4373 ;*TEST OF EA BITS 16 AND 17
4374 ;*DO A DATI USING IN BA BITS 16 AND 17
4375 ;*VERIFY CORRECT RESULTS
4376 ;:*****
4377

```

TEST 64

```

4378 ;-----
4379 ;:*****
4380 ;:*****
4381 024502 000004 TST64: SCOPE
4382 024504 012737 000064 001202 MOV #64,$TSTNM ; LOAD THE NO. OF THIS TEST
4383 024512 012737 024626 001442 MOV #TST65,NEXT ; POINT TO THE START OF NEXT TEST.
4384 ;R1 CONTAINS BASE KMC11 ADDRESS
4385 024520 104410 MSTCLR ;MASTER CLEAR KMC11
4386 024522 013737 002074 024550 MOV KMP04,15 ;USE SEL4 FOR ADDRESS
4387 024530 013737 002074 024546 MOV KMP04,25 ;USE SEL4 FOR ADDRESS
4388 024536 004537 035540 JSR R5,NPRSET ;LOAD BA AND DATA
4389 024542 000000 0 ;IN DATA
4390 024544 125252 0 ;OUT DATA
4391 024546 000000 2S: 0 ;IN BA
4392 024550 000000 1S: 0 ;OUT BA
4393 024552 012761 000015 000004 MOV #15,4(R1) ;LOAD SEL4
4394 024560 012761 121110 000006 MOV #121110,6(R1) ;PUT INSTRUCTION IN SEL6
4395 024566 012711 003000 MOV #BIT9!BIT10,(R1) ;SET CROMI AND CROMO!!
4396 024572 052711 000400 BIS #BIT8,(R1) ;CLOCK IT!
4397 024576 000240 NOP ;WAIT FOR NPR
4398 024600 012705 121110 MOV #121110,R5 ;PUT "EXPECTED" IN R5

```

4399	024604	104412		ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4400	024606	021004		021004		:MOVE IN DATA LB TO SEL4
4401	024610	104412		ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4402	024612	021025		021025		:MOVE IN DATA HB TO SEL5
4403	024614	016104	000004	MOV	4(R1),R4	:PUT "FOUND" IN R4
4404	024620	020504		CMP	R5,R4	:CORRECT RESULTS ?
4405	024622	001401		BEG	3\$:BR IF YES
4406	024624	104012		ERROR	12	:ERROR BA 16 AND 17 FAILED
4407	024626					

3\$:

```

***** TEST 65 *****
* NPR NON-EXISTENT MEMORY TEST
* DO A DATO TO A NON-EXISTENT ADDRESS
* VERIFY THAT THE NON-EXISTENT BIT SET IN IBUS REG 11
*****

```

TEST 65

4418						:*****
4419	024626	000004		TST65:	SCOPE	
4420	024630	012737	000065	001202	MOV	#65,\$TSTNM ; LOAD THE NO. OF THIS TEST
4421	024636	012737	024736	001442	MOV	#TST66,NEXT ; POINT TO THE START OF NEXT TEST.
4422						:R1 CONTAINS BASE KMC11 ADDRESS
4423	024644	104410		MSTCLR		:MASTER CLEAR KMC11
4424	024646	004537	035540	JSR	R5,NPRSET	:LOAD IBUS REGISTERS 0-7
4425	024652	000000		0		:IN DATA
4426	024654	000000		0		:OUT DATA
4427	024656	177320		177320		:IN BA
4428	024660	177320		177320		:OUT BA
4429	024662	012761	000014	000004	MOV	#14,4(R1) ;SET OUT BA BITS 16+17 IN PORT4
4430	024670	104412		ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4431	024672	121111		121111		:SET OUTBA 16 AND 17
4432	024674	012761	000021	000004	MOV	#21,4(R1) ;SET NPR REQUEST BITS IN PORT4
4433	024702	104412		ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4434	024704	121110		121110		:MOV IBUS* 4 TO IBUS* 10
4435	024706	000240		NOP		
4436	024710	104412		ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4437	024712	121225		121225		:MOV IBUS*11 TO IBUS*5
4438	024714	012705	000001	MOV	#1,R5	:PUT "EXPECTED" IN R5
4439	024720	116104	000005	MOV	5(R1),R4	:PUT "FOUND" IN R4
4440	024724	042704	177776	BIC	#177776,R4	:CLEAR UNWANTED BITS
4441	024730	020504		CMP	R5,R4	:DATA CORRECT?
4442	024732	001401		BEG	1\$:BR IF YES
4443	024734	104012		ERROR	12	:ERROR NON-EXISTENT MEM BIT FAILED TO SET
4444	024736					

1\$:

```

***** TEST 66 *****
* NPR NON-EXISTENT MEMORY TEST
* DO A DATI FROM A NON-EXISTENT ADDRESS
* VERIFY THAT THE NON-EXISTENT BIT SET IN IBUS REG 11
*****

```

TEST 66

```

-----

```

```

4455          ;*****
4456 024736 000004 1ST66: SCOPE
4457 024740 012737 000066 001202 MOV #66,$STSTNM ; LOAD THE NO. OF THIS TEST
4458 024746 012737 025044 001442 MOV #TST67,NEXT ; POINT TO THE START OF NEXT TEST.
4459          ;R1 CONTAINS BASE KMC11 ADDRESS
4460 024754 104410 MSTCLR ;MASTER CLEAR KMC11
4461 024756 004537 035540 JSR R5,NPRSET ;LOAD IBUS REGISTERS 0-7
4462 024762 000000 0 ;IN DATA
4463 024764 000000 0 ;OUT DATA
4464 024766 177320 ;IN BA
4465 024770 177320 ;OUT BA
4466 024772 005061 000004 CLR 4(R1)
4467 024776 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4468 025000 121111 ;CLEAR NON-EXISTENT BIT
4469 025002 012761 000015 000004 MOV #15,4(R1) ;SET NPR REQUEST BITS IN PORT4
4470 025010 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4471 025012 121110 121110 ;MOV IBUS* 4 TO IBUS* 10
4472 025014 000240 NOP
4473 025016 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4474 025020 121225 121225 ;MOV IBUS*11 TO IBUS*5
4475 025022 012705 000001 MOV #1,R5 ;PUT "EXPECTED" IN R5
4476 025026 116104 000005 MOVB 5(R1),R4 ;PUT "FOUND" IN R4
4477 025032 042704 177776 BIC #177776,R4 ;CLEAR UNWANTED BITS
4478 025036 020504 CMP R5,R4 ;DATA CORRECT?
4479 025040 001401 BEQ 1$ ;BR IF YES
4480 025042 104012 ERROR 12 ;ERROR NON-EXISTENT MEM BIT FAILED TO SET
4481 025044
4482
4483
4484          ;***** TEST 67 *****
4485          ;*NPR TEST
4486          ;*USING DATO, NPR A BINARY COUNT (0-377 )
4487          ;*FROM MICRO-PROCESSOR TO ALL AVAILABLE MEMORY
4488          ;:*****
4489
4490          ; TEST 67
4491          ;-----
4492          ;*****
4493 025044 000004 1ST67: SCOPE
4494 025046 012737 000067 001202 MOV #67,$STSTNM ; LOAD THE NO. OF THIS TEST
4495 025054 012737 000003 001310 MOV #3,$TIMES ; LOAD ITERATION COUNT
4496 025062 012737 025244 001442 MOV #TST70,NEXT ; POINT TO THE START OF NEXT TEST.
4497          ;R1 CONTAINS BASE KMC11 ADDRESS
4498 025070 104410 MSTCLR ;MASTER CLEAR KMC11
4499 025072 005037 025242 CLR 5$ ;START FLAG AT 0
4500 025076 005000 CLR R0 ;DATA
4501 025100 012702 037234 MOV #CORMAX,R2 ;ADDRESS
4502 025104
4503 025104 010037 025134 1$: MOV R0,2$ ;LOAD DATA
4504 025110 010237 025140 MOV R2,4$ ;LOAD BA
4505 025114 032702 000001 BIT #810,R2 ;IS BA ODD?
4506 025120 001402 BEQ .+6 ;BR IF NO
4507 025122 000337 025134 SWAB 2$ ;IF ODD PUT DATA IN HI-BYTE
4508 025126 004537 035540 JSR R5,NPRSET ;LOAD NPR REGISTERS
4509 025132 000000 0 ;IN DATA
4510 025134 000000 0 ;OUT DATA

```



```

4511 025136 000000
4512 025140 000000
4513 025142 105012
4514 025144 012761 000221 000004
4515 025152 104412
4516 025154 121110
4517 025156 000240
4518 025160 010005
4519 025162 111204
4520 025164 120504
4521 025166 001401
4522 025170 104021
4523 025172 104405
4524 025174 005200
4525 025176 042700 177400
4526 025202 005737 025242
4527 025206 001402
4528 025210 005700
4529 025212 001412
4530 025214 005202
4531 025216 023702 001466
4532 025222 001330
4533 025224 012702 037234
4534 025230 012737 177777 025242
4535 025236 000722
4536 025240 104420
4537 025242 000000
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4554 025244 000004
4555 025246 012737 000070 001202
4556 025254 012737 025360 001442
4557 025262 012737 025306 001444
4558
4559 025270 104410
4560 025272 004737 035602
4561 025276 025350
4562 025300 004737 035636
4563 025304 025350
4564 025306
4565 025306 104412
4566 025310 010000

; IN BA
; OUT BA
; CLEAR MEMORY LOCATION
; LOAD PORT4
; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
; DO THE NPR
; PUT "EXPECTED" IN R5
; PUT "FOUND" IN R4
; IS DATA CORRECT?
; BR IF YES
; ERROR, DATA INCORRECT
; NEXT CHARACTER
; USE ONLY LOW BYTE
; HAS MAX MEMORY BEEN REACHED YET?
; BR IF NO
; DONE PATTERN?
; BR IF YES
; INC BA
; REACHED MEMORY LIMIT YET?
; BR IF NOT
; RESTART BA AT FIRST ADDRESS
; SET FLAG TO END TEST AT END OF DATA PATTERN
; CONTINUE
; ADVANCE LOOP
; THIS LOCATION IS A FLAG, IT STARTS AT 0,
; AND IS SET TO -1 WHEN LAST MEMORY ADDRESS
; IS USED, TEST IS THEN ENDED WHEN PATTERN IS FINISHED

;SMEM1
;SMEM0
;SMEM2 1K
;SMEM3 1K

***** TEST 70 *****
;ALU C BIT TEST
;TEST THAT AN ADD OF 377 AND 377 WILL SET THE C BIT
*****

; TEST 70
-----
;*****
;ST70: SCOPE
;MOV #70,STSTNM ; LOAD THE NO. OF THIS TEST
;MOV #TST71,NEXT ; POINT TO THE START OF NEXT TEST.
;MOV #15,LOCK ; ADDRESS FOR LOCK ON DATA.
;R1 CONTAINS BASE KMC11 ADDRESS
;MASTER CLEAR KMC11
;LOAD MAINMEM DATA
;POINTER TO DATA
;LOAD SP DATA
;POINTER TO DATA
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;MAR←0

```

```

4567 025312 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4568 025314 054400 054400!<0*20> ;ADD 377 AND 377, TO SET C BIT
4569 025316 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4570 025320 040421 040401!<1*20> ;ADD 0 AND 0 AND THE C BIT
4571 025322 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4572 025324 061224 61224 ;PUT RESULTS IN PORT4
4573 025326 012705 000001 MOV #1,R5 ;PUT "EXPECTED" IN R5
4574 025332 016104 000004 MOV 4(R1),R4 ;PUT "FOUND" IN R4
4575 025336 120504 CMPB R5,R4 ;DATA CORRECT?
4576 025340 001401 BEQ 2$ ;BR IF YES
4577 025342 104015 ERROR 15 ;ERROR C BIT NOT SET
4578 025344 104405 2$: SCOP1 ;SW09=1?
4579 025346 104420 ADVANCE ;ADVANCE LOOP
4580 025350 377 000 000 TDATA: .BYTE -1,0,0,0,0,0,0,0
4581 025353 000 000 000
4582 025356 000 000 000
4583 .EVEN

```

```

***** TEST 71 *****
*ALU TEST
*TEST OF ALU FUNCTION SEL B WITH C BIT CLEARED
*ALU FUNCTION (B) CODE=11
*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
*PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

TEST 71

```

4597 025360 000004 TST71: SCOPE ;*****
4598 025362 012737 000071 001202 MOV #71,$STNM ;LOAD THE NO. OF THIS TEST
4599 025370 012737 025536 001442 MOV #TST72,NEXT ;POINT TO THE START OF NEXT TEST.
4600 025376 012737 025430 001444 MOV #1$,LOCK ;ADDRESS FOR LOCK ON DATA.
4601 ;R1 CONTAINS BASE KMC11 ADDRESS
4602 025404 104410 M$TCLR ;MASTER CLEAR KMC11
4603 025406 005000 CLR R0 ;MEM + SP ADDRESS
4604 025410 012702 025526 MOV #5$,R2 ;POINTER TO CORRECT DATA
4605 025414 004737 035602 JSR PC,MEMLD ;LOAD 8 WORDS OF MAIN MEMORY
4606 025420 035726 MEMDAT ;POINTER TO DATA
4607 025422 004737 035636 JSR PC,SPLD ;LOAD 8 WORDS OF SP
4608 025426 035736 SPDAT ;POINTER TO DATA
4609 025430 004737 035702 1$: JSR PC,CLRC ;CLEAR C BIT!
4610 025434 042737 000017 025450 BIC #1,2$ ;CLEAR ADDRESS FIELD OF INSTRUCTION
4611 025442 050037 025450 BIS R0,2$ ;ADD ADDRESS TO INSTRUCTION
4612 025446 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4613 025450 010000 010000 ;LOAD MAR
4614 025452 042737 000017 025466 2$: BIC #17,3$ ;CLEAR ADDRESS OF INSTRUCTION
4615 025460 050037 025466 BIS R0,3$ ;ADD ADDRESS TO INSTRUCTION
4616 025464 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4617 025466 040620 040400!<11*20> 3$: BR + SEL B
4618 025470 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4619 025472 061224 61224 ;MOVE BR TO PORT4
4620 025474 111205 MOVB (R2),R5 ;PUT "EXPECTED" IN R5
4621 025476 116104 000004 MOVB 4(R1),R4 ;PUT "FOUND" IN R4
4622 025502 120504 CMPB R5,R4 ;DATA CORRECT?

```

```

4623 025504 001401 BEA 4$ :BR IF YES
4624 025506 104015 ERROR 15 :ALU ERROR
4625 025510 104405 4$: SCOP1 :SW09=1?
4626 025512 005202 INC R2 :NEXT DATA
4627 025514 005200 INC R0 :NEXT ADDRESS
4628 025516 022700 000010 CMP #10,R0 :DONE YET?
4629 025522 001342 BNE 1$ :BR IF NO
4630 025524 104420 ADVANCE :ADVANCE LOOP
4631 025526 000 377 000 5$: .BYTE 0,-1,0,-1,125,252,125,252
4632 025531 377 125 252
4633 025534 125 252
4634 .EVEN
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```

```

***** TEST 72 *****
*ALU TEST
*TEST OF ALU FUNCTION SEL A WITH C BIT CLEARED
*ALU FUNCTION (A) CODE=10
*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
*PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

: TEST 72

```

4648 025536 000004 TST72: SCOPE
4649 025540 012737 000072 001202 MOV #72,STSTNM :LOAD THE NO. OF THIS TEST
4650 025546 012737 025714 001442 MOV #TST73,NEXT :POINT TO THE START OF NEXT TEST.
4651 025554 012737 025606 001444 MOV #1$,LOCK :ADDRESS FOR LOCK ON DATA.
4652
4653 025562 104410 MSTCLR :R1 CONTAINS BASE KMC11 ADDRESS
4654 025564 005000 CLR R0 :MASTER CLEAR KMC11
4655 025566 012702 025704 MOV #5$,R2 :MEM + SP ADDRESS
4656 025572 004737 035602 JSR PC,MEMLD :POINTER TO CORRECT DATA
4657 025576 035726 MEMDAT :LOAD 8 WORDS OF MAIN MEMORY
4658 025600 004737 035636 JSR PC,SPLD :POINTER TO DATA
4659 025604 035736 SPDAT :LOAD 8 WORDS OF SP
4660 025606 004737 035702 1$: JSR PC,CLRC :POINTER TO DATA
4661 025612 042737 000017 025626 BIC #17,2$ :CLEAR C BIT!
4662 025620 050037 025626 BIS R0,2$ :CLEAR ADDRESS FIELD OF INSTRUCTION
4663 025624 104412 ROMCLK :ADD ADDRESS TO INSTRUCTION
4664 025626 010000 2$: 010000 :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4665 025630 042737 000017 025644 BIC #17,3$ :LOAD MAR
4666 025636 050037 025644 BIS R0,3$ :CLEAR ADDRESS OF INSTRUCTION
4667 025642 104412 ROMCLK :ADD ADDRESS TO INSTRUCTION
4668 025644 040600 3$: 040400! <10*20> :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4669 025646 104412 ROMCLK :BR + SEL A
4670 025650 061224 61224 :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4671 025652 111205 MOVB (R2),R5 :MOVE BR TO PORT4
4672 025654 116104 000004 MOVB 4(R1),R4 :PUT "EXPECTED" IN R5
4673 025660 120504 CMPB R5,R4 :PUT "FOUND" IN R4
4674 025662 001401 BEQ 4$ :DATA CORRECT?
4675 025664 104015 ERROR 15 :BR IF YES
4676 025666 104405 4$: SCOP1 :ALU ERROR
4677 025670 005202 INC R2 :SW09=1?
4678 025672 005200 INC R0 :NEXT DATA
: NEXT ADDRESS

```

```

4679 025674 022700 000010      CMP      #10,R0      :DONE YET?
4680 025700 001342      BNE      1$         :BR IF NO
4681 025702 104420      ADVANCE      :ADVANCE LOOP
4682 025704      000      000      377 5$: .BYTE 0,0,-1,-1,125,125,252,252
4683 025707      377      125      125
4684 025712      252      252

```

.EVEN

```

***** TEST 73 *****
:ALU TEST
:TEST OF ALU FUNCTION A OR NOTB WITH C BIT CLEARED
:ALU FUNCTION (A OR NOTB) CODE=12
:LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
:PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

: TEST 73

```

4698
4699 025714 000004      TST73: SCOPE
4700 025716 012737 000073 001202      MOV      #73,$STSTNM      : LOAD THE NO. OF THIS TEST
4701 025724 012737 026072 001442      MOV      #TST74,NEXT      : POINT TO THE START OF NEXT TEST.
4702 025732 012737 025764 001444      MOV      #1$,LOCK        : ADDRESS FOR LOCK ON DATA.
4703
4704 025740 104410      MSTCLR      :R1 CONTAINS BASE KMC11 ADDRESS
4705 025742 005000      CLR      R0      :MASTER CLEAR KMC11
4706 025744 012702 026062      MOV      #5$,R2      :MEM + SP ADDRESS
4707 025750 004737 035602      JSR      PC,MEMLD     : POINTER TO CORRECT DATA
4708 025754 035726      MEMDAT     :LOAD 8 WORDS OF MAIN MEMORY
4709 025756 004737 035636      JSR      PC,SPLD     : POINTER TO DATA
4710 025762 035736      SPDAT     :LOAD 8 WORDS OF SP
4711 025764 004737 035702 1$: JSR      PC,CLRC     : POINTER TO DATA
4712 025770 042737 000017 026004      BIC      #17,2$      : CLEAR C BIT!
4713 025776 050037 026004      BIS      R0,2$      : CLEAR ADDRESS FIELD OF INSTRUCTION
4714 026002 104412      ROMCLK     :ADD ADDRESS TO INSTRUCTION
4715 026004 010000      010000     :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4716 026006 042737 000017 026022 2$: BIC      #17,3$      : LOAD MAR
4717 026014 050037 026022      BIS      R0,3$      : CLEAR ADDRESS OF INSTRUCTION
4718 026020 104412      ROMCLK     :ADD ADDRESS TO INSTRUCTION
4719 026022 040640 3$: ROMCLK 040400!<12*20> :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4720 026024 104412      ROMCLK     :BR + A OR NOTB
4721 026026 061224      61224     :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4722 026030 111205      MOVB      (R2),R5     : MOVE BR TO PORT4
4723 026032 116104 000004      MOVB      4(R1),R4    : PUT "EXPECTED" IN R5
4724 026036 120504      CMPB     R5,R4      : PUT "FOUND" IN R4
4725 026040 001401      BEQ      4$         : DATA CORRECT?
4726 026042 104015      ERROR     1$       : BR IF YES
4727 026044 104405 4$: SCOP1     :ALU ERROR
4728 026046 005202      INC      R2         : SW09=1?
4729 026050 005200      INC      R0         : NEXT DATA
4730 026052 022700 000010      CMP      #10,R0      : NEXT ADDRESS
4731 026056 001342      BNE      1$         : DONE YET?
4732 026060 104420      ADVANCE   :BR IF NO
4733 026062      377      000      377 5$: .BYTE -1,0,-1,-1,-1,125,252,-1
4734 026065      377      377      125

```

```

4735 026070 252 377
4736 .EVEN
4737
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4749
4750 026072 000004
4751 026074 012737 000074 001202
4752 026102 012737 026250 001442
4753 026110 012737 026142 001444
4754
4755 026116 104410
4756 026120 005000
4757 026122 012702 026240
4758 026126 004737 035602
4759 026132 035726
4760 026134 004737 035636
4761 026140 035736
4762 026142 004737 035702 1$:
4763 026146 042737 000017 026162
4764 026154 050037 026162
4765 026160 104412
4766 026162 010000 2$:
4767 026164 042737 000017 026200
4768 026172 050037 026200
4769 026176 104412
4770 026200 040660 3$:
4771 026202 104412
4772 026204 061224
4773 026206 111205
4774 026210 116104 000004
4775 026214 120504
4776 026216 001401
4777 026220 104015
4778 026222 104405 4$:
4779 026224 005202
4780 026226 005200
4781 026230 022700 000010
4782 026234 001342
4783 026236 104420
4784 026240 000 000 5$:
4785 026243 377 125 000
4786 026246 000 252
4787 .EVEN
4788
4789
4790

```

```

***** TEST 74 *****
*ALU TEST
*TEST OF ALU FUNCTION A AND B WITH C BIT CLEARED
*ALU FUNCTION (A AND B) CODE=13
*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
*PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

TEST 74

```

-----
*****
TST74: SCOPE
MOV #74,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST75,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
CLR R0 ; MEM + SP ADDRESS
MOV #5$,R2 ; POINTER TO CORRECT DATA
JSR PC,MEMLD ; LOAD 8 WORDS OF MAIN MEMORY
MEMDAT ; POINTER TO DATA
JSR PC,SPLD ; LOAD 8 WORDS OF SP
SPDAT ; POINTER TO DATA
JSR PC,CLRC ; CLEAR C BIT!
BIC #17,2$ ; CLEAR ADDRESS FIELD OF INSTRUCTION
BIS R0,2$ ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
010000 ; LOAD MAR
BIC #17,3$ ; CLEAR ADDRESS OF INSTRUCTION
BIS R0,3$ ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
040400! <13*20> ; BR + A AND B
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
61224 ; MOVE BR TO PORT4
MOV# (R2),R5 ; PUT "EXPECTED" IN R5
MOV# 4(R1),R4 ; PUT "FOUND" IN R4
CMPB R5,R4 ; DATA CORRECT?
BEQ 4$ ; BR IF YES
ERROR 15 ; ALU ERROR
SCOPI 4$ ; SW09=1?
INC R2 ; NEXT DATA
INC R0 ; NEXT ADDRESS
CMP #10,R0 ; DONE YET?
BNE 1$ ; BR IF NO
ADVANCE ; ADVANCE LOOP
.BYTE 0,0,0,-1,125,0,0,252

```

***** TEST 75 *****

```

4791
4792
4793
4794
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4796
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4798
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4800
4801 026250 000004
4802 026252 012737 000075 001202
4803 026260 012737 026426 001442
4804 026266 012737 026320 001444
4805
4806 026274 104410
4807 026276 005000
4808 026300 012702 026416
4809 026304 004737 035602
4810 026310 035726
4811 026312 004737 035636
4812 026316 035736
4813 026320 004737 035702
4814 026324 042737 000017 026340
4815 026332 050037 026340
4816 026336 104412
4817 026340 010000
4818 026342 042737 000017 026356
4819 026350 050037 026356
4820 026354 104412
4821 026356 040700
4822 026360 104412
4823 026362 061224
4824 026364 111205
4825 026366 116104 000004
4826 026372 120504
4827 026374 001401
4828 026376 104015
4829 026400 104405
4830 026402 005202
4831 026404 005200
4832 026406 022700 000010
4833 026412 001342
4834 026414 104420
4835 026416 000 377 377
4836 026421 377 125 377
4837 026424 377 252
4838
4839 .EVEN
4840
4841
4842
4843
4844
4845
4846

```

```

;*ALU TEST
;*TEST OF ALU FUNCTION A OR B WITH C BIT CLEARED
;*ALU FUNCTION (A OR B) CODE=14
;*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
;*PERFORM THE FUNCTION, VERIFY THE RESULTS
;*****

```

TEST 75

```

†T75: SCOPE
MOV #75,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #T75,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.

;R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
CLR R0 ; MEM + SP ADDRESS
MOV #5$,R2 ; POINTER TO CORRECT DATA
JSR PC,MEMLD ; LOAD 8 WORDS OF MAIN MEMORY
MEMDAT ; POINTER TO DATA
JSR PC,SPLD ; LOAD 8 WORDS OF SP
SPDAT ; POINTER TO DATA
JSR PC,CLRC ; CLEAR C BIT!
BIC #17,2$ ; CLEAR ADDRESS FIELD OF INSTRUCTION
BIS R0,2$ ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
010000 ; LOAD MAR
BIC #17,3$ ; CLEAR ADDRESS OF INSTRUCTION
BIS R0,3$ ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
040400! <14*20> ; BR ← A OR B
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
61224 ; MOVE BR TO PORT4
MOVB (R2),R5 ; PUT "EXPECTED" IN R5
MOVB 4(R1),R4 ; PUT "FOUND" IN R4
CMPB R5,R4 ; DATA CORRECT?
BEQ 4$ ; BR IF YES
ERROR 15 ; ALU ERROR
SCOPI 4$ ; SW09=1?
INC R2 ; NEXT DATA
INC R0 ; NEXT ADDRESS
CMP #10,R0 ; DONE YET?
BNE 1$ ; BR IF NO
ADVANCE ; ADVANCE LOOP
.BYTE 0,-1,-1,-1,125,-1,-1,252

```

***** TEST 76 *****

```

;*ALU TEST
;*TEST OF ALU FUNCTION A XOR B WITH C BIT CLEARED
;*ALU FUNCTION (A XOR B) CODE=15
;*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
;*PERFORM THE FUNCTION, VERIFY THE RESULTS

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4867
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4871
4872
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4874
4875
4876
4877
4878
4879
4880
4881
4882
4883
4884
4885
4886
4887
4888
4889
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4899
4900
4901
4902

026426 000004
026430 012737 000076 001202
026436 012737 026604 001442
026444 012737 026476 001444

026452 104410
026454 005000
026456 012702 026574
026462 004737 035602
026466 035726
026470 004737 035636
026474 035736
026476 004737 035702
026502 042737 000017 026516
026510 050037 026516
026514 104412
026516 010000
026520 042737 000017 026534
026526 050037 026534
026532 104412
026534 040720
026536 104412
026540 061224
026542 111205
026544 116104 000004
026550 120504
026552 001401
026554 104015
026556 104405
026560 075202
026562 005200
026564 022700 000010
026570 001342
026572 104420
026574 000 377 377
026577 000 000 377
026602 377 000

```

;:*****
; TEST 76
-----
;:*****
TST76: SCOPE
MOV #76,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST77,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #18,LOCK ; ADDRESS FOR LOCK ON DATA.

;R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
CLR R0 ; MEM + SP ADDRESS
MOV #58,R2 ; POINTER TO CORRECT DATA
JSR PC,MEMLD ; LOAD 8 WORDS OF MAIN MEMORY
MEMDAT ; POINTER TO DATA
JSR PC,SPLD ; LOAD 8 WORDS OF SP
SPDAT ; POINTER TO DATA
1$: JSR PC,CLRC ; CLEAR C BIT!
BIC #17,2$ ; CLEAR ADDRESS FIELD OF INSTRUCTION
BIS R0,2$ ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
010000 ; LOAD MAR
2$: BIC #17,3$ ; CLEAR ADDRESS OF INSTRUCTION
BIS R0,3$ ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3$: 040400!<15*20> ; BR + A XOR B
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
61224 ; MOVE BR TO PORT4
MOV# (R2),R5 ; PUT "EXPECTED" IN R5
MOV# 4(R1),R4 ; PUT "FOUND" IN R4
CMPB R5,R4 ; DATA CORRECT?
BEQ 4$ ; BR IF YES
ERROR 15 ; ALU ERROR
4$: SCOP1 ; SW09=1?
INC R2 ; NEXT DATA
INC R0 ; NEXT ADDRESS
CMP #10,R0 ; DONE YET?
BNE 1$ ; BR IF NO
ADVANCE ; ADVANCE LOOP
5$: .BYTE 0,-1,-1,0,0,-1,-1,0
.EVEN

```

```

;***** TEST 77 *****
;*ALU TEST
;*TEST OF ALU FUNCTION ADD WITH C BIT CLEARED
;*ALU FUNCTION (A PLUS B) CODE=00
;*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
;*PERFORM THE FUNCTION, VERIFY THE RESULTS
;:*****

```

TEST 77

;:*****

```

4903 026604 000004          TST77: SCOPE
4904 026606 012737 000077 001202  MOV      #77,$STSTNM          ; LOAD THE NO. OF THIS TEST
4905 026614 012737 026762 001442  MOV      #TST100,NEXT      ; POINT TO THE START OF NEXT TEST.
4906 026622 012737 026654 001444  MOV      #1$,LOCK          ; ADDRESS FOR LOCK ON DATA.
4907                                ; R1 CONTAINS BASE KMC11 ADDRESS
4908 026630 164410          MSTCLR   ; MASTER CLEAR KMC11
4909 026632 005000          CLR      R0                ; MEM + SP ADDRESS
4910 026634 012702 026752  MOV      #5$,R2            ; POINTER TO CORRECT DATA
4911 026640 004737 035602  JSR      PC,MEMLD          ; LOAD 8 WORDS OF MAIN MEMORY
4912 026644 035726          MEMDAT   ; POINTER TO DATA
4913 026646 004737 035636  JSR      PC,SPLD          ; LOAD 8 WORDS OF SP
4914 026652 035736          SPDAT   ; POINTER TO DATA
4915 026654 004737 035702  JSR      PC,CLRC          ; CLEAR C BIT!
4916 026660 042737 000017 026674  BIC      #17,2$           ; CLEAR ADDRESS FIELD OF INSTRUCTION
4917 026666 050037 026674  BIS      R0,2$           ; ADD ADDRESS TO INSTRUCTION
4918 026672 104412          ROMCLK  ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4919 026674 010000          O10000 ; LOAD MAR
4920 026676 042737 000017 026712  BIC      #17,3$           ; CLEAR ADDRESS OF INSTRUCTION
4921 026704 050037 026712  BIS      R0,3$           ; ADD ADDRESS TO INSTRUCTION
4922 026710 104412          ROMCLK  ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4923 026712 040400          O40400! <00*20> ; BR + ADD
4924 026714 104412          ROMCLK  ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4925 026716 061224          61224  ; MOVE BR TO PORT4
4926 026720 111205          MOVB     (R2),R5           ; PUT "EXPECTED" IN R5
4927 026722 116104 000004  MOVB     4(R1),R4         ; PUT "FOUND" IN R4
4928 026726 120504          CMPB     R5,R4           ; DATA CORRECT?
4929 026730 001401          BEQ      4$              ; BR IF YES
4930 026732 104015          ERROR   15            ; ALU ERROR
4931 026734 104405          4$: SCOPI              ; SW09=1?
4932 026736 005202          INC      R2             ; NEXT DATA
4933 026740 005200          INC      R0             ; NEXT ADDRESS
4934 026742 022700 000010  CMP      #10,R0          ; DONE YET?
4935 026746 001342          BNE     1$              ; BR IF NO
4936 026750 104420          ADVANCE ; ADVANCE LOOP
4937 026752          000      377 377 5$: .BYTE 0,-1,-1,376,252,-1,-1,124
4938 026755          376      252 377
4939 026760          377      124

```

.EVEN

```

***** TEST 100 *****
;ALU TEST
;TEST OF ALU FUNCTION 2A W/C WITH C BIT CLEARED
;ALU FUNCTION (A PLUS A PLUS C) CODE=6
;LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
;PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

; TEST 100

```

*****
;TST100: SCOPE
MOV      #100,$STSTNM          ; LOAD THE NO. OF THIS TEST
MOV      #TST101,NEXT        ; POINT TO THE START OF NEXT TEST.
MOV      #1$,LOCK            ; ADDRESS FOR LOCK ON DATA.
;R1 CONTAINS BASE KMC11 ADDRESS

```


4959	027006	104410				MSTCLR		: MASTER CLEAR KMC11
4960	027010	005000				CLR	RO	: MEM + SP ADDRESS
4961	027012	012702	027130			MOV	#55,R2	: POINTER TO CORRECT DATA
4962	027016	004737	035602			JSR	PC, MEMLD	: LOAD 8 WORDS OF MAIN MEMORY
4963	027022	035726				MEMDAT		: POINTER TO DATA
4964	027024	004737	035636			JSR	PC, SPLD	: LOAD 8 WORDS OF SP
4965	027030	035736				SPDAT		: POINTER TO DATA
4966	027032	004737	035702	15:		JSR	PC, CLRC	: CLEAR C BIT!
4967	027036	042737	000017	027052		BIC	#17, 25	: CLEAR ADDRESS FIELD OF INSTRUCTION
4968	027044	050037	027052			BIS	RO, 25	: ADD ADDRESS TO INSTRUCTION
4969	027050	104412				ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4970	027052	010000			25:	010000		: LOAD MAR
4971	027054	042737	000017	027070		BIC	#17, 35	: CLEAR ADDRESS OF INSTRUCTION
4972	027062	050037	027070			BIS	RO, 35	: ADD ADDRESS TO INSTRUCTION
4973	027066	104412				ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4974	027070	040540			35:	040400! <6*20>		: BR + 2A W/C
4975	027072	104412				ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4976	027074	061224				61224		: MOVE BR TO PORT4
4977	027076	111205				MOVB	(R2), R5	: PUT "EXPECTED" IN R5
4978	027100	116104	000004			MOVB	4(R1), R4	: PUT "FOUND" IN R4
4979	027104	120504				CMPB	R5, R4	: DATA CORRECT?
4980	027106	001401				BEG	45	: BR IF YES
4981	027110	104015				ERROR	15	: ALU ERROR
4982	027112	104405			45:	SCOPI		: SW09=1?
4983	027114	005202				INC	R2	: NEXT DATA
4984	027116	005200				INC	RO	: NEXT ADDRESS
4985	027120	022700	000010			CMP	#10, RO	: DONE YET?
4986	027124	001342				BNE	15	: BR IF NO
4987	027126	104420				ADVANCE		: ADVANCE LOOP
4988	027130	000	000	376	55:	.BYTE	0, 0, 376, 376, 252, 252, 124, 124	
4989	027133	376	252	252				
4990	027136	124	124					

.EVEN

```

***** TEST 101 *****
: *ALU TEST
: *TEST OF ALU FUNCTION SUB WITH C BIT CLEARED
: *ALU FUNCTION (A-B) CODE=16
: *LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
: *PERFORM THE FUNCTION, VERIFY THE RESULTS
: *****

```

: TEST 101

```

: *****
: *ST101: SCOPE
: *MOV #101, $STNM ; LOAD THE NO. OF THIS TEST
: *MOV #ST102, NEXT ; POINT TO THE START OF NEXT TEST.
: *MOV #15, LOCK ; ADDRESS FOR LOCK ON DATA.
: *R1 CONTAINS BASE KMC11 ADDRESS
: *MSTCLR
: *CLR RO ; MASTER CLEAR KMC11
: *MOV #55, R2 ; MEM + SP ADDRESS
: *JSR PC, MEMLD ; POINTER TO CORRECT DATA
: *MEMDAT ; LOAD 8 WORDS OF MAIN MEMORY
: * ; POINTER TO DATA

```

5005	027140	000004						
5006	027142	012737	000101	001202				
5007	027150	012737	027316	001442				
5008	027156	012737	027210	001444				
5009								
5010	027164	104410				MSTCLR		
5011	027166	005000				CLR	RO	
5012	027170	012702	027306			MOV	#55, R2	
5013	027174	004737	035602			JSR	PC, MEMLD	
5014	027200	035726				MEMDAT		

```

5015 027202 004737 035636 JSR PC, SPLD ; LOAD 8 WORDS OF SP
5016 027206 035736 SPDAT ; POINTER TO DATA
5017 027210 004737 035702 1$: JSR PC, CLRC ; CLEAR C BIT!
5018 027214 042737 000017 027230 BIC #17, 2$ ; CLEAR ADDRESS FIELD OF INSTRUCTION
5019 027222 050037 027230 BIS RO, 2$ ; ADD ADDRESS TO INSTRUCTION
5020 027226 104412 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5021 027230 010000 2$: 010000 ; LOAD MAR
5022 027232 042737 000017 027246 BIC #17, 3$ ; CLEAR ADDRESS OF INSTRUCTION
5023 027240 050037 027246 BIS RO, 3$ ; ADD ADDRESS TO INSTRUCTION
5024 027244 104412 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5025 027246 040740 3$: 040400! <16*20> ; BR + SUB
5026 027250 104412 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5027 027252 061224 61224 ; MOVE BR TO PORT4
5028 027254 111205 MOVB (R2), R5 ; PUT "EXPECTED" IN R5
5029 027256 116104 000004 MOVB 4(R1), R4 ; PUT "FOUND" IN R4
5030 027262 120504 CMPB R5, R4 ; DATA CORRECT?
5031 027264 001401 BEQ 4$ ; BR IF YES
5032 027266 104015 ERROR 15 ; ALU ERROR
5033 027270 104405 4$: SCOP1 ; SHOW=1?
5034 027272 005202 INC R2 ; NEXT DATA
5035 027274 005200 INC RO ; NEXT ADDRESS
5036 027276 022700 000010 CMP #10, RO ; DONE YET?
5037 027302 001342 BNE 1$ ; BR IF NO
5038 027304 104420 ADVANCE ; ADVANCE LOOP
5039 027306 000 001 377 5$: .BYTE 0, 1, -1, 0, 0, 253, 125, 0
5040 027311 000 000 253
5041 027314 125 000
5042 .EVEN
5043
5044
5045
5046
5047
5048
5049
5050
5051
5052
5053
5054
5055

```

```

***** TEST 102 *****
; *ALU TEST
; *TEST OF ALU FUNCTION ADD W/C WITH C BIT CLEARED
; *ALU FUNCTION (A PLUS B PLUS C) CODE=01
; *LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
; *PERFORM THE FUNCTION, VERIFY THE RESULTS
; *****

```

TEST 102

```

5056 027316 000004 ; *****
5057 027320 012737 000102 001202 †ST102: SCOPE ; LOAD THE NO. OF THIS TEST
5058 027326 012737 027474 001442 MOV #102, STSTNM ; POINT TO THE START OF NEXT TEST.
5059 027334 012737 027366 001444 MOV #ST103, NEXT ; ADDRESS FOR LOCK ON DATA.
5060 MOV #1$, LOCK ; R1 CONTAINS BASE KMC11 ADDRESS
5061 027342 104410 MSTCLR ; MASTER CLEAR KMC11
5062 027344 005000 CLR RO ; MEM + SP ADDRESS
5063 027346 012702 027464 MOV #5$, R2 ; POINTER TO CORRECT DATA
5064 027352 004737 035602 JSR PC, MEMLD ; LOAD 8 WORDS OF MAIN MEMORY
5065 027356 035726 MEMDAT ; POINTER TO DATA
5066 027360 004737 035636 JSR PC, SPLD ; LOAD 8 WORDS OF SP
5067 027364 035736 SPDAT ; POINTER TO DATA
5068 027366 004737 035702 1$: JSR PC, CLRC ; CLEAR C BIT!
5069 027372 042737 000017 027406 BIC #17, 2$ ; CLEAR ADDRESS FIELD OF INSTRUCTION
5070 027400 050037 027406 BIS RO, 2$ ; ADD ADDRESS TO INSTRUCTION

```

```

5071 027404 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5072 027406 010000 2$: 010000 ;LOAD MAR
5073 027410 042737 000017 027424 BIC #17,3$ ;CLEAR ADDRESS OF INSTRUCTION
5074 027416 050037 027424 BIS RO,3$ ;ADD ADDRESS TO INSTRUCTION
5075 027422 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5076 027424 040420 3$: 040400! <01*20> ;BR + ADD W/C
5077 027426 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5078 027430 061224 61224 ;MOVE BR TO PORT4
5079 027432 111205 MOVB (R2),R5 ;PUT "EXPECTED" IN R5
5080 027434 116104 000004 MOVB 4(R1),R4 ;PUT "FOUND" IN R4
5081 027440 120504 CMPB R5,R4 ;DATA CORRECT?
5082 027442 001401 BEQ 4$ ;BR IF YES
5083 027444 104015 ERROR 15 ;ALU ERROR
5084 027446 104405 4$: SCOPI ;SW09=1?
5085 027450 005202 INC R2 ;NEXT DATA
5086 027452 005200 INC RO ;NEXT ADDRESS
5087 027454 022700 000010 CMP #10,RO ;DONE YET?
5088 027460 001342 BNE 1$ ;BR IF NO
5089 027462 104420 ADVANCE ;ADVANCE LOOP
5090 027464 000 377 377 5$: .BYTE 0,-1,-1,376,252,-1,-1,124
5091 027467 376 252 377
5092 027472 377 124
5093 .EVEN
5094
5095
5096
5097
5098
5099
5100
5101
5102
5103
5104
5105
5106

```

```

***** TEST 103 *****
;ALU TEST
;TEST OF ALU FUNCTION SUB W/C WITH C BIT CLEARED
;ALU FUNCTION (A-B-C) CODE=2
;LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
;PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

; TEST 103

```

5107 027474 000004 ;*****
5108 027476 012737 000103 001202 TST103: SCOPE
5109 027504 012737 027652 001442 MOV #103,$STSTM ;LOAD THE NO. OF THIS TEST
5110 027512 012737 027544 001444 MOV #TST104,NEXT ;POINT TO THE START OF NEXT TEST.
5111 MOV #1$,LOCK ;ADDRESS FOR LOCK ON DATA.
5112 027520 104410 ;R1 CONTAINS BASE KMC11 ADDRESS
5113 027522 005000 MSTCLR ;MASTER CLEAR KMC11
5114 027524 012702 027642 CLR RO ;MEM + SP ADDRESS
5115 027530 004737 035602 MOV #5$,R2 ;POINTER TO CORRECT DATA
5116 027534 035726 JSR PC,MEMLD ;LOAD 8 WORDS OF MAIN MEMORY
5117 027536 004737 035636 MEMDAT ;POINTER TO DATA
5118 027542 035736 JSR PC,SPLD ;LOAD 8 WORDS OF SP
5119 027544 004737 035702 SPDAT ;POINTER TO DATA
5120 027550 042737 000017 027564 1$: JSR PC,CLRC ;CLEAR C BIT!
5121 027556 050037 027564 BIC #17,2$ ;CLEAR ADDRESS FIELD OF INSTRUCTION
5122 027562 104412 BIS RO,2$ ;ADD ADDRESS TO INSTRUCTION
5123 027564 010000 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5124 027566 042737 000017 027602 2$: 010000 ;LOAD MAR
5125 027574 050037 027602 BIC #17,3$ ;CLEAR ADDRESS OF INSTRUCTION
5126 027600 104412 BIS RO,3$ ;ADD ADDRESS TO INSTRUCTION
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

```

```

5127 027602 040440      3$: 040400! <2*20>      ; BR + SUB W/C
5128 027604 104412      ROMCLK      ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5129 027606 061224      61224      ; MOVE BR TO PORT4
5130 027610 111205      MOVB      (R2),R5      ; PUT "EXPECTED" IN R5
5131 027612 116104 000004 MOVB      4(R1),R4      ; PUT "FOUND" IN R4
5132 027616 120504      CMPB      R5,R4      ; DATA CORRECT?
5133 027620 001401      BEQ      4$          ; BR IF YES
5134 027622 104015      ERROR     15          ; ALU ERROR
5135 027624 104405      4$: SCOP1      ; SW09=1?
5136 027626 005202      INC      R2          ; NEXT DATA
5137 027630 005200      INC      R0          ; NEXT ADDRESS
5138 027632 022700 000010 CMP      #10,R0      ; DONE YET?
5139 027636 001342      BNE      1$          ; BR IF NO
5140 027640 104420      ADVANCE   ; ADVANCE LOOP
5141 027642      377      000      376 5$: .BYTE -1,0,376,-1,-1,252,124,-1
5142 027645      377      377      252
5143 027650      124      377
5144                                     .EVEN
5145
5146
5147                                     ;***** TEST 104 *****
5148                                     ;*ALU TEST
5149                                     ;*TEST OF ALU FUNCTION INC A WITH C BIT CLEARED
5150                                     ;*ALU FUNCTION (A PLUS 1) CODE=3
5151                                     ;*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
5152                                     ;*PERFORM THE FUNCTION, VERIFY THE RESULTS
5153                                     ;*****
5154
5155                                     ; TEST 104
5156                                     ;-----
5157                                     ;*****

```

```

5158 027652 000004      †ST104: SCOPE      ;*****
5159 027654 012737 000104 001202 MOV      #104,STSTNM      ; LOAD THE NO. OF THIS TEST
5160 027662 012737 030030 001442 MOV      #TST105,NEXT      ; POINT TO THE START OF NEXT TEST.
5161 027670 012737 027722 001444 MOV      #1$,LOCK        ; ADDRESS FOR LOCK ON DATA.
5162                                     ; R1 CONTAINS BASE KMC11 ADDRESS
5163 027676 104410      MSTCLR      ; MASTER CLEAR KMC11
5164 027700 005000      CLR      R0          ; MEM + SP ADDRESS
5165 027702 012702 030020 MOV      #5$,R2          ; POINTER TO CORRECT DATA
5166 027706 004737 035602 JSR      PC,MEMLD      ; LOAD 8 WORDS OF MAIN MEMORY
5167 027712 035726      MEMDAT      ; POINTER TO DATA
5168 027714 004737 035636 JSR      PC,SPLD      ; LOAD 8 WORDS OF SP
5169 027720 035736      SPDAT      ; POINTER TO DATA
5170 027722 004737 035702 1$: JSR      PC,CLRC      ; CLEAR C BIT!
5171 027726 042737 000017 027742 BIC      #17,2$        ; CLEAR ADDRESS FIELD OF INSTRUCTION
5172 027734 050037 027742 BIS      R0,2$          ; ADD ADDRESS TO INSTRUCTION
5173 027740 104412      ROMCLK      ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5174 027742 010000      010000      ; LOAD MAR
5175 027744 042737 000017 027760 2$: BIC      #17,3$        ; CLEAR ADDRESS OF INSTRUCTION
5176 027752 050037 027760 BIS      R0,3$          ; ADD ADDRESS TO INSTRUCTION
5177 027756 104412      ROMCLK      ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5178 027760 040460      3$: 040400! <3*20>      ; BR + INC A
5179 027762 104412      ROMCLK      ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5180 027764 061224      61224      ; MOVE BR TO PORT4
5181 027766 111205      MOVB      (R2),R5      ; PUT "EXPECTED" IN R5
5182 027770 116104 000004 MOVB      4(R1),R4      ; PUT "FOUND" IN R4

```

```

5183 027774 120504          CMPB   R5,R4          ;DATA CORRECT?
5184 027776 001401          BEQ    4$            ;BR IF YES
5185 030000 104015          ERROR  15           ;ALU ERROR
5186 030002 104405          4$: SCOP1          ;SW09=1?
5187 030004 005202          INC    R2           ;NEXT DATA
5188 030006 005200          INC    R0           ;NEXT ADDRESS
5189 030010 022700 000010        CMP    #10,R0       ;DONE YET?
5190 030014 001342          BNE   1$           ;BR IF NO
5191 030016 104420          ADVANCE          ;ADVANCE LOOP
5192 030020          001    001    000 5$: .BYTE 1,1,0,0,126,126,253,253
5193 030023          000    126    126
5194 030026          253    253
5195                                     .EVEN
5196
5197
5198
5199

```

```

***** TEST 105 *****
*ALU TEST
*TEST OF ALU FUNCTION 2A WITH C BIT CLEARED
*ALU FUNCTION (A PLUS A) CODE=5
*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
*PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

TEST 105

```

5200
5201
5202
5203
5204
5205
5206
5207
5208
5209 030030 000004          ;*****
5210 030032 012737 000105 001202  †TST105: SCOPE
5211 030040 012737 030206 001442          MOV    #105,$STSTNM ; LOAD THE NO. OF THIS TEST
5212 030046 012737 030100 001444          MOV    #TST106,NEXT ; POINT TO THE START OF NEXT TEST.
5213                                     MOV    #1$,LOCK    ; ADDRESS FOR LOCK ON DATA.
5214 030054 104410          ;R1 CONTAINS BASE KMC11 ADDRESS
5215 030056 005000          ;MASTER CLEAR KMC11
5216 030060 012702 030176          CLR    R0           ;MEM + SP ADDRESS
5217 030064 004737 035602          MOV    #5$,R2       ;POINTER TO CORRECT DATA
5218 030070 035726          JSR    PC,MEMLD     ;LOAD 8 WORDS OF MAIN MEMORY
5219 030072 004737 035636          MEMDAT          ;POINTER TO DATA
5220 030076 035736          JSR    PC,SPLD      ;LOAD 8 WORDS OF SP
5221 030100 004737 035702          SPDAT          ;POINTER TO DATA
5222 030104 042737 000017 030120 1$: JSR    PC,CLRC      ;CLEAR C BIT!
5223 030112 050037 030120          BIC    #17,2$       ;CLEAR ADDRESS FIELD OF INSTRUCTION
5224 030116 104412          BIS    R0,2$        ;ADD ADDRESS TO INSTRUCTION
5225 030120 010000          ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5226 030122 042737 000017 030136 2$: 010000          ;LOAD MAR
5227 030130 050037 030136          BIC    #17,3$       ;CLEAR ADDRESS OF INSTRUCTION
5228 030134 104412          BIS    R0,3$        ;ADD ADDRESS TO INSTRUCTION
5229 030136 040520          ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5230 030140 104412          040400! <5*20>    ;BR + 2A
5231 030142 061224          ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5232 030144 111205          61224          ;MOVE BR TO PORT4
5233 030146 116104          MOVB   (R2),R5     ;PUT "EXPECTED" IN R5
5234 030152 120504          MOVB   4(R1),R4    ;PUT "FOUND" IN R4
5235 030154 001401          CMPB   R5,R4       ;DATA CORRECT?
5236 030156 104015          BEQ    4$          ;BR IF YES
5237 030160 104405          ERROR  15         ;ALU ERROR
5238 030162 005202          4$: SCOP1          ;SW09=1?
          INC    R2           ;NEXT DATA

```

5239	030164	005200				INC	RO	:NEXT ADDRESS
5240	030166	022700	000010			CMP	#10,RO	:DONE YET?
5241	030172	001342				BNE	1\$:BR IF NO
5242	030174	104420				ADVANCE		: ADVANCE LOOP
5243	030176	000	000	376	5\$:	.BYTE	0,0,376,376,252,252,124,124	
5244	030201	376	252	252				
5245	030204	124	124					

.EVEN

```

***** TEST 106 *****
:ALU TEST
:TEST OF ALU FUNCTION A PLUS C WITH C BIT CLEARED
:ALU FUNCTION (A PLUS C) CODE=4
:LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
:PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

: TEST 106

5259						ST106:	SCOPE	
5260	030206	000004				MOV	#106,STSTNM	: LOAD THE NO. OF THIS TEST
5261	030210	012737	000106	001202		MOV	#TST107,NEXT	: POINT TO THE START OF NEXT TEST.
5262	030216	012737	030364	001442		MOV	#1\$,LOCK	: ADDRESS FOR LOCK ON DATA.
5263	030224	012737	030256	001444				:R1 CONTAINS BASE KMC11 ADDRESS
5264						MSTCLR		:MASTER CLEAR KMC11
5265	030232	104410				CLR	RO	:MEM + SP ADDRESS
5266	030234	005000				MOV	#5\$,R2	: POINTER TO CORRECT DATA
5267	030236	012702	030354			JSR	PC,MEMLD	:LOAD 8 WORDS OF MAIN MEMORY
5268	030242	004737	035602			MEMDAT		: POINTER TO DATA
5269	030246	035726				JSR	PC,SPLD	:LOAD 8 WORDS OF SP
5270	030250	004737	035636			SPDAT		: POINTER TO DATA
5271	030254	035736				JSR	PC,CLRC	:CLEAR C BIT!
5272	030256	004737	035702		1\$:	BIC	#17,2\$:CLEAR ADDRESS FIELD OF INSTRUCTION
5273	030262	042737	000017	030276		BIS	RO,2\$:ADD ADDRESS TO INSTRUCTION
5274	030270	050037	030276			ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5275	030274	104412				010000		:LOAD MAR
5276	030276	010000			2\$:	BIC	#17,3\$:CLEAR ADDRESS OF INSTRUCTION
5277	030300	042737	000017	030314		BIS	RO,3\$:ADD ADDRESS TO INSTRUCTION
5278	030306	050037	030314			ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5279	030312	104412			3\$:	040400! <4*20>		:BR + A PLUS C
5280	030314	040500				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5281	030316	104412				61224		:MOVE BR TO PORT4
5282	030320	061224				MOVB	(R2),R5	:PUT "EXPECTED" IN R5
5283	030322	111205				MOVB	4(R1),R4	:PUT "FOUND" IN R4
5284	030324	116104	000004			CMPB	R5,R4	:DATA CORRECT?
5285	030330	120504				BEQ	4\$:BR IF YES
5286	030332	001401				ERROR	1\$:ALU ERROR
5287	030334	104015			4\$:	SCOPI		:SWJ9=1?
5288	030336	104405				INC	R2	:NEXT DATA
5289	030340	005202				INC	RO	:NEXT ADDRESS
5290	030342	005200				CMP	#10,RO	:DONE YET?
5291	030344	022700	000010			BNE	1\$:BR IF NO
5292	030350	001342				ADVANCE		: ADVANCE LOOP
5293	030352	104420				.BYTE	0,0,-1,-1,125,125,252,252	
5294	030354	000	000	377	5\$:			

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5295 030357 377 125 125
5296 030362 252 252
5297
5298 .EVEN
5299
5300
5301
5302
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5304
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5308
5309
5310
5311 030364 000004
5312 030366 012737 000107 001202
5313 030374 012737 030542 001442
5314 030402 012737 030434 001444
5315
5316 030410 104410
5317 030412 005000
5318 030414 012702 030532
5319 030420 004737 035602
5320 030424 035726
5321 030426 004737 035636
5322 030432 035736
5323 030434 004737 035702
5324 030440 042737 000017 030454 1$:
5325 030446 050037 030454
5326 030452 104412
5327 030454 010000 2$:
5328 030456 042737 000017 030472
5329 030464 050037 030472
5330 030470 104412
5331 030472 040760 3$:
5332 030474 104412
5333 030476 061224
5334 030500 111205
5335 030502 116104 000004
5336 030506 120504
5337 030510 001401
5338 030512 104015
5339 030514 104405 4$:
5340 030516 005202
5341 030520 005200
5342 030522 022700 000010
5343 030526 001342
5344 030530 104420
5345 030532 377 000 376 5$:
5346 030535 377 377 252
5347 030540 124 377
5348 .EVEN
5349
5350

```

```

***** TEST 107 *****
:ALU TEST
:TEST OF ALU FUNCTION 2'S COMP SUB WITH C BIT CLEARED
:ALU FUNCTION (A-B-1) CODE=17
:LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
:PERFORM THE FUNCTION, VERIFY THE RESULTS
:*****

```

TEST 107

```

*****
TST107: SCOPE
MOV #107,$STNM ; LOAD THE NO. OF THIS TEST
MOV #TST110,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
CLR RO ; MEM + SP ADDRESS
MOV #5$,R2 ; POINTER TO CORRECT DATA
JSR PC,MEMLD ; LOAD 8 WORDS OF MAIN MEMORY
MEMDAT ; POINTER TO DATA
JSR PC,SPLD ; LOAD 8 WORDS OF SP
SPDAT ; POINTER TO DATA
1$: JSR PC,CLRC ; CLEAR C BIT!
BIC #17,2$ ; CLEAR ADDRESS FIELD OF INSTRUCTION
BIS RO,2$ ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
010000 ; LOAD MAR
2$: BIC #17,3$ ; CLEAR ADDRESS OF INSTRUCTION
BIS RO,3$ ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
040400! <17*20> ; BR + 2'S COMP SUB
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
61224 ; MOVE BR TO PORT4
MOV# (R2),R5 ; PUT "EXPECTED" IN R5
MOV# 4(R1),R4 ; PUT "FOUND" IN R4
CMP# R5,R4 ; DATA CORRECT?
BEQ 4$ ; BR IF YES
ERROR 15 ; ALU ERROR
SCOPI ; SW09=1?
INC R2 ; NEXT DATA
INC RO ; NEXT ADDRESS
CMP #10,RO ; DONE YET?
BNE 1$ ; BR IF NO
ADVANCE ; ADVANCE LOOP
5$: .BYTE -1,0,376,-1,-1,252,124,-1

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5351
5352
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5357
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5360
5361
5362 030542 000004
5363 030544 012737 000110 001202
5364 030552 012737 030720 001442
5365 030560 012737 030612 001444
5366
5367 030566 104410
5368 030570 005000
5369 030572 012702 030710
5370 030576 004737 035602
5371 030602 035726
5372 030604 004737 035636
5373 030610 035736
5374 030612 004737 035702
5375 030616 042737 000017 030632
5376 030624 050037 030632
5377 030630 104412
5378 030632 010000
5379 030634 042737 000017 030650
5380 030642 050037 030650
5381 030646 104412
5382 030650 040560
5383 030652 104412
5384 030654 061224
5385 030656 111205
5386 030660 116104 000004
5387 030664 120504
5388 030666 001401
5389 030670 104015
5390 030672 104405
5391 030674 005202
5392 030676 005200
5393 030700 022700 000010
5394 030704 001342
5395 030706 104420
5396 030710 377 377 376
5397 030713 376 124 124
5398 030716 251 251
5399
5400
5401
5402
5403
5404
5405
5406

```

```

***** TEST 110 *****
*ALU TEST
*TEST OF ALU FUNCTION DEC A WITH C BIT CLEARED
*ALU FUNCTION (A-1) CODE=7
*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
*PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

: TEST 110
-----
*****
†ST110: SCOPE
MOV #110,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST111,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
CLR R0 ; MEM + SP ADDRESS
MOV #5$,R2 ; POINTER TO CORRECT DATA
JSR PC,MEMLD ; LOAD 8 WORDS OF MAIN MEMORY
MEMDAT ; POINTER TO DATA
JSR PC,SPLD ; LOAD 8 WORDS OF SP
SPDAT ; POINTER TO DATA
JSR PC,CLRC ; CLEAR C BIT!
BIC #17,2$ ; CLEAR ADDRESS FIELD OF INSTRUCTION
BIS R0,2$ ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
010000 ; LOAD MAR
BIC #17,3$ ; CLEAR ADDRESS OF INSTRUCTION
BIS R0,3$ ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
040400!(7*20) ; BR + DEC A
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
61224 ; MOVE BR TO PORT4
MOVB (R2),R5 ; PUT "EXPECTED" IN R5
MOVB 4(R1),R4 ; PUT "FOUND" IN R4
CMPB R5,R4 ; DATA CORRECT?
BEQ 4$ ; BR IF YES
ERROR 15 ; ALU ERROR
4$: SCOP1 ; SMO9=1?
INC R2 ; NEXT DATA
INC R0 ; NEXT ADDRESS
CMP #10,R0 ; DONE YET?
BNE 1$ ; BR IF NO
ADVANCE ; ADVANCE LOOP
5$: .BYTE -1,-1,376,376,124,124,251,251
.EVEN

***** TEST 111 *****
*ALU TEST
*TEST OF ALU FUNCTION SEL B WITH C BIT SET
*ALU FUNCTION (B) CODE=11
*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA

```



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5407
5408
5409
5410
5411
5412
5413 030720 000004
5414 030722 012737 000111 001202
5415 030730 012737 031076 001442
5416 030736 012737 030770 001444
5417
5418 030744 104410
5419 030746 005000
5420 030750 012702 031066
5421 030754 004737 035602
5422 030760 035726
5423 030762 004737 035636
5424 030766 035736
5425 030770 004737 035714
5426 030774 042737 000017 031010
5427 031002 050037 031010
5428 031006 104412
5429 031010 010000
5430 031012 042737 000017 031026
5431 031020 050037 031026
5432 031024 104412
5433 031026 040620
5434 031030 104412
5435 031032 061224
5436 031034 111205
5437 031036 116104 000004
5438 031042 120504
5439 031044 001401
5440 031046 104015
5441 031050 104405
5442 031052 005202
5443 031054 005200
5444 031056 022700 000010
5445 031062 001342
5446 031064 104420
5447 031066 000 377 000 5447
5448 031071 377 125 252 5448
5449 031074 125 252 5449
5450
5451
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5454
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5456
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5462

```

```

; *PERFORM THE FUNCTION, VERIFY THE RESULTS
; *****
; TEST 111
; -----
; *****
TST111: SCOPE
MOV #111, $TSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST112, NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1$, LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
CLR R0 ; MEM + SP ADDRESS
MOV #5$, R2 ; POINTER TO CORRECT DATA
JSR PC, MEMLD ; LOAD 8 WORDS OF MAIN MEMORY
MEMDAT ; POINTER TO DATA
JSR PC, SPLD ; LOAD 8 WORDS OF SP
SPDAT ; POINTER TO DATA
1$: JSR PC, SETC ; SET C BIT!
BIC #17, 2$ ; CLEAR ADDRESS FIELD OF INSTRUCTION
BIS R0, 2$ ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
010000 ; LOAD MAR
2$: BIC #17, 3$ ; CLEAR ADDRESS OF INSTRUCTION
BIS R0, 3$ ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
040400! <11*20> ; BR + SEL B
3$: ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
61224 ; MOVE BR TO PORT4
MOVB (R2), R5 ; PUT "EXPECTED" IN R5
MOVB 4(R1), R4 ; PUT "FOUND" IN R4
CMPB R5, R4 ; DATA CORRECT?
BEQ 4$ ; BR IF YES
ERROR 15 ; ALU ERROR
4$: SCOP1 ; SW09=1?
INC R2 ; NEXT DATA
INC R0 ; NEXT ADDRESS
CMP #10, R0 ; DONE YET?
BNE 1$ ; BR IF NO
ADVANCE ; ADVANCE LOOP
5$: .BYTE 0, -1, 0, -1, 125, 252, 125, 252
; ***** TEST 112 *****
; *ALU TEST
; *TEST OF ALU FUNCTION SEL A WITH C BIT SET
; *ALU FUNCTION (A) CODE=10
; *LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
; *PERFORM THE FUNCTION, VERIFY THE RESULTS
; *****
; TEST 112
; -----

```

```

5463
5464 031076 000004
5465 031100 012737 000112 001202
5466 031106 012737 031254 001442
5467 031114 012737 031146 001444
5468
5469 031122 104410
5470 031124 005000
5471 031126 012702 031244
5472 031132 004737 035602
5473 031136 035726
5474 031140 004737 035636
5475 031144 035736
5476 031146 004737 035714
5477 031152 042737 000017 031166
5478 031160 050037 031166
5479 031164 104412
5480 031166 010000
5481 031170 042737 000017 031204
5482 031176 050037 031204
5483 031202 104412
5484 031204 040600
5485 031206 104412
5486 031210 061224
5487 031212 111205
5488 031214 116104 000004
5489 031220 120504
5490 031222 001401
5491 031224 104015
5492 031226 104405
5493 031230 005202
5494 031232 005200
5495 031234 022700 000010
5496 031240 001342
5497 031242 104420
5498 031244 000 000 377 55:
5499 031247 377 125 125
5500 031252 252 252
5501
5502
5503
5504
5505
5506
5507
5508
5509
5510
5511
5512
5513
5514
5515 031254 000004
5516 031256 012737 000113 001202
5517 031264 012737 031432 001442
5518 031272 012737 031324 001444

```

```

*****
†TST112: SCOPE
MOV #112,$STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST113,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
CLR R0 ; MEM + SP ADDRESS
MOV #5$,R2 ; POINTER TO CORRECT DATA
JSR PC,MEMLD ; LOAD 8 WORDS OF MAIN MEMORY
MEMDAT ; POINTER TO DATA
JSR PC,SPLD ; LOAD 8 WORDS OF SP
SPDAT ; POINTER TO DATA
1$: JSR PC,SETC ; SET C BIT!
BIC #17,2$ ; CLEAR ADDRESS FIELD OF INSTRUCTION
BIS R0,2$ ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
010000 ; LOAD MAR
BIC #17,3$ ; CLEAR ADDRESS OF INSTRUCTION
BIS R0,3$ ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3$: 040400! <10*20>
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
61224 ; MOVE BR TO PORT4
MOVB (R2),R5 ; PUT "EXPECTED" IN R5
MOVB 4(R1),R4 ; PUT "FOUND" IN R4
CMPB R5,R4 ; DATA CORRECT?
BEQ 4$ ; BR IF YES
ERROR 15 ; ALU ERROR
4$: SCOP1 ; SW09=1?
INC R2 ; NEXT DATA
INC R0 ; NEXT ADDRESS
CMP #10,R0 ; DONE YET?
BNE 1$ ; BR IF NO
ADVANCE ; ADVANCE LOOP
55: .BYTE 0,0,-1,-1,125,125,252,252
.EVEN

```

```

***** TEST 113 *****
; *ALU TEST
; *TEST OF ALU FUNCTION A OR NOTB WITH C BIT SET
; *ALU FUNCTION (A OR NOTB) CODE=12
; *LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
; *PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

```

; TEST 113
-----
*****
†TST113: SCOPE
MOV #113,$STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST114,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.

```

```

5519
5520 031300 104410 MSTCLR ;R1 CONTAINS BASE KMC11 ADDRESS
5521 031302 005000 CLR RO ;MASTER CLEAR KMC11
5522 031304 012702 031422 MOV #5$,R2 ;MEM + SP ADDRESS
5523 031310 004737 035602 JSR PC,MEMLD ;POINTER TO CORRECT DATA
5524 031314 035726 MEMDAT ;LOAD 8 WORDS OF MAIN MEMORY
5525 031316 004737 035636 JSR PC,SPLD ;POINTER TO DATA
5526 031322 035736 SPDAT ;LOAD 8 WORDS OF SP
5527 031324 004737 035714 1$: JSR PC,SETC ;POINTER TO DATA
5528 031330 042737 000017 031344 BIC #17,2$ ;SET C BIT!
5529 031336 050037 031344 BIS RO,2$ ;CLEAR ADDRESS FIELD OF INSTRUCTION
5530 031342 104412 ROMCLK ;ADD ADDRESS TO INSTRUCTION
5531 031344 010000 2$: 010000 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5532 031346 042737 000017 031362 BIC #17,3$ ;LOAD MAR
5533 031354 050037 031362 BIS RO,3$ ;CLEAR ADDRESS OF INSTRUCTION
5534 031360 104412 ROMCLK ;ADD ADDRESS TO INSTRUCTION
5535 031362 040640 3$: 040400! <12*20> ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5536 031364 104412 ROMCLK ;BR ← A OR NOTB
5537 031366 061224 61224 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5538 031370 111205 MOVB (R2),R5 ;MOVE BR TO PORT4
5539 031372 116104 000004 MOVB 4(R1),R4 ;PUT "EXPECTED" IN R5
5540 031376 120504 CMPB R5,R4 ;PUT "FOUND" IN R4
5541 031400 001401 BEQ 4$ ;DATA CORRECT?
5542 031402 104015 ERROR 15 ;BR IF YES
5543 031404 104405 4$: SCOP1 ;ALU ERROR
5544 031406 005202 INC R2 ;SW09=1?
5545 031410 005200 INC RO ;NEXT DATA
5546 031412 022700 000010 CMP #10,RO ;NEXT ADDRESS
5547 031416 001342 BNE 1$ ;DONE YET?
5548 031420 104420 ADVANCE 1$ ;BR IF NO
5549 031422 377 000 377 5$: .BYTE -1,0,-1,-1,-1,125,252,-1 ;ADVANCE LOOP
5550 031425 377 125
5551 031430 252 377
5552 .EVEN

```

```

***** TEST 114 *****
;ALU TEST
;TEST OF ALU FUNCTION A AND B WITH C BIT SET
;ALU FUNCTION (A AND B) CODE=13
;LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
;PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

TEST 114

```

5565 *****
5566 031432 000004 †ST114: SCOPE
5567 031434 012737 000114 001202 MOV #114,$STNM ; LOAD THE NO. OF THIS TEST
5568 031442 012737 031610 001442 MOV #TST115,NEXT ; POINT TO THE START OF NEXT TEST.
5569 031450 012737 031502 001444 MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
5570 *****
5571 031456 104410 MSTCLR ;R1 CONTAINS BASE KMC11 ADDRESS
5572 031460 005000 CLR RO ;MASTER CLEAR KMC11
5573 031462 012702 031600 MOV #5$,R2 ;MEM + SP ADDRESS
5574 031466 004737 035602 JSR PC,MEMLD ;POINTER TO CORRECT DATA
;LOAD 8 WORDS OF MAIN MEMORY

```

5575	031472	035726				MEMDAT			: POINTER TO DATA
5576	031474	004737	035636			JSR	PC, SPLD		: LOAD 8 WORDS OF SP
5577	031500	035736				SPDAT			: POINTER TO DATA
5578	031502	004737	035714		15:	JSR	PC, SETC		: SET C BIT!
5579	031506	042737	000017	031522		BIC	#17, 25		: CLEAR ADDRESS FIELD OF INSTRUCTION
5580	031514	050037	031522			BIS	RO, 25		: ADD ADDRESS TO INSTRUCTION
5581	031520	104412				ROMCLK			: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5582	031522	010000			25:	010000			: LOAD MAR
5583	031524	042737	000017	031540		BIC	#17, 35		: CLEAR ADDRESS OF INSTRUCTION
5584	031532	050037	031540			BIS	RO, 35		: ADD ADDRESS TO INSTRUCTION
5585	031536	104412				ROMCLK			: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5586	031540	040660			35:	040400! <13*20>			: BR + A AND B
5587	031542	104412				ROMCLK			: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5588	031544	061224				61224			: MOVE BR TO PORT4
5589	031546	111205				MOVB	(R2), R5		: PUT "EXPECTED" IN R5
5590	031550	116104	000004			MOVB	4(R1), R4		: PUT "FOUND" IN R4
5591	031554	120504				CMPB	R5, R4		: DATA CORRECT?
5592	031556	001401				BEG	45		: BR IF YES
5593	031560	104015				ERROR	15		: ALU ERROR
5594	031562	104405			45:	SCOPI			: SMO9=1?
5595	031564	005202				INC	R2		: NEXT DATA
5596	031566	005200				INC	RO		: NEXT ADDRESS
5597	031570	022700	000010			CMP	#10, RO		: DONE YET?
5598	031574	001342				BNE	15		: BR IF NO
5599	031576	104420				ADVANCE			: ADVANCE LOOP
5600	031600	000	000	000	55:	.BYTE	0,0,0,-1,125,0,0,252		
5601	031603	377	125	000					
5602	031606	000	252						

.EVEN

```

***** TEST 115 *****
: *ALU TEST
: *TEST OF ALU FUNCTION A OR B WITH C BIT SET
: *ALU FUNCTION (A OR B) CODE=14
: *LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
: *PERFORM THE FUNCTION, VERIFY THE RESULTS
: *****

```

TEST 115

5617	031610	000004				↑ST115: SCOPE			: *****
5618	031612	012737	000115	001202		MOV	#115, STSTNM		: LOAD THE NO. OF THIS TEST
5619	031620	012737	031766	001442		MOV	#TST116, NEXT		: POINT TO THE START OF NEXT TEST.
5620	031626	012737	031660	001444		MOV	#15, LOCK		: ADDRESS FOR LOCK ON DATA.
5621									: R1 CONTAINS BASE KMC11 ADDRESS
5622	031634	104410				MSTCLR			: MASTER CLEAR KMC11
5623	031636	005000				CLR	RO		: MEM + SP ADDRESS
5624	031640	012702	031756			MOV	#55, R2		: POINTER TO CORRECT DATA
5625	031644	004737	035602			JSR	PC, MEMLD		: LOAD 8 WORDS OF MAIN MEMORY
5626	031650	035726				MEMDAT			: POINTER TO DATA
5627	031652	004737	035636			JSR	PC, SPLD		: LOAD 8 WORDS OF SP
5628	031656	035736				SPDAT			: POINTER TO DATA
5629	031660	004737	035714		15:	JSR	PC, SETC		: SET C BIT!
5630	031664	042737	000017	031700		BIC	#17, 25		: CLEAR ADDRESS FIELD OF INSTRUCTION

```

5631 031672 050037 031700      BIS      RO,2$      ;ADD ADDRESS TO INSTRUCTION
5632 031676 104412      ROMCLK     ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5633 031700 010000      010000      LOAD MAR
5634 031702 042737 000017 031716 2$:      BIC      #17,3$    ;CLEAR ADDRESS OF INSTRUCTION
5635 031710 050037 031716      BIS      RO,3$    ;ADD ADDRESS TO INSTRUCTION
5636 031714 104412      ROMCLK     ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5637 031716 040700      040400! <14*20> 3$:      BR + A OR B
5638 031720 104412      ROMCLK     ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5639 031722 061224      61224      MOVE BR TO PORT4
5640 031724 111205      MOVB      (R2),R5  ;PUT "EXPECTED" IN R5
5641 031726 116104 000004      MOVB      4(R1),R4 ;PUT "FOUND" IN R4
5642 031732 120504      CMPB      R5,R4   ;DATA CORRECT?
5643 031734 001401      BEQ      4$      ;BR IF YES
5644 031736 104015      ERROR     15     ;ALU ERROR
5645 031740 104405      4$:      SCOP1      ;SWD9=1?
5646 031742 005202      INC      R2      ;NEXT DATA
5647 031744 005200      INC      RO      ;NEXT ADDRESS
5648 031746 022700 000010      CMP      #10,RO  ;DONE YET?
5649 031752 001342      BNE      1$      ;BR IF NO
5650 031754 104420      ADVANCE   ;ADVANCE LOOP
5651 031756      000      377      377 5$:      .BYTE 0,-1,-1,-1,125,-1,-1,252
5652 031761      377      125      377
5653 031764      377      252
5654      .EVEN

```

```

***** TEST 116 *****
;ALU TEST
;TEST OF ALU FUNCTION A XOR B WITH C BIT SET
;ALU FUNCTION (A XOR B) CODE=15
;LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
;PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

TEST 116

```

5667      ;*****
5668 031766 000004      ;TST116: SCOPE
5669 031770 012737 000116 001202      MOV      #116,$STNM ; LOAD THE NO. OF THIS TEST
5670 031776 012737 032144 001442      MOV      #TST117,NEXT ; POINT TO THE START OF NEXT TEST.
5671 032004 012737 032036 001444      MOV      #1$,LOCK   ; ADDRESS FOR LOCK ON DATA.
5672      ;R1 CONTAINS BASE KMC11 ADDRESS
5673 032012 104410      MSTCLR    ;MASTER CLEAR KMC11
5674 032014 005000      CLR      RO      ;MEM + SP ADDRESS
5675 032016 012702 032134      MOV      #5$,R2   ;POINTER TO CORRECT DATA
5676 032022 004737 035602      JSR      PC,MEMLD ;LOAD 8 WORDS OF MAIN MEMORY
5677 032026 035726      MEMDAT    ;POINTER TO DATA
5678 032030 004737 035636      JSR      PC,SPLD  ;LOAD 8 WORDS OF SP
5679 032034 035736      SPDAT    ;POINTER TO DATA
5680 032036 004737 035714      1$:      JSR      PC,SETC  ;SET C BIT!
5681 032042 042737 000017 032056      BIC      #17,2$   ;CLEAR ADDRESS FIELD OF INSTRUCTION
5682 032050 050037 032056      BIS      RO,2$    ;ADD ADDRESS TO INSTRUCTION
5683 032054 104412      ROMCLK     ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5684 032056 010000      2$:      010000      ;LOAD MAR
5685 032060 042737 000017 032074      BIC      #17,3$   ;CLEAR ADDRESS OF INSTRUCTION
5686 032066 050037 032074      BIS      RO,3$    ;ADD ADDRESS TO INSTRUCTION

```

5687	032072	104412					ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5688	032074	040720				3\$:	040400! <15*20>		:BR + A XOR B
5689	032076	104412					ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5690	032100	061224					61224		:MOVE BR TO PORT4
5691	032102	111205					MOVB (R2),R5		:PUT "EXPECTED" IN R5
5692	032104	116104	000004				MOVB 4(R1),R4		:PUT "FOUND" IN R4
5693	032110	120504					CMPB R5,R4		:DATA CORRECT?
5694	032112	001401					BEQ 4\$:BR IF YES
5695	032114	104015					ERROR 15		:ALU ERROR
5696	032116	104405				4\$:	SCOP1		:SW09=1?
5697	032120	005202					INC R2		:NEXT DATA
5698	032122	005200					INC R0		:NEXT ADDRESS
5699	032124	022700	000010				CMP #10,R0		:DONE YET?
5700	032130	001342					BNE 1\$:BR IF NO
5701	032132	104420					ADVANCE		:ADVANCE LOOP
5702	032134	000	377	377	5\$:		.BYTE 0,-1,-1,0,0,-1,-1,0		
5703	032137	000	000	377					
5704	032142	377	000						
5705							.EVEN		

```

***** TEST 117 *****
*ALU TEST
*TEST OF ALU FUNCTION ADD WITH C BIT SET
*ALU FUNCTION (A PLUS B) CODE=00
*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
*PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

```

; TEST 117
;-----

```

5718							*****		
5719	032144	000004				1\$:	ST117: SCOPE		
5720	032146	012737	000117	001202			MOV #117,STSTNM		: LOAD THE NO. OF THIS TEST
5721	032154	012737	032322	001442			MOV #TST120,NEXT		: POINT TO THE START OF NEXT TEST.
5722	032162	012737	032214	001444			MOV #1\$,LOCK		: ADDRESS FOR LOCK ON DATA.
5723									:R1 CONTAINS BASE KMC11 ADDRESS
5724	032170	104410					MSTCLR		:MASTER CLEAR KMC11
5725	032172	005000					CLR R0		:MEM + SP ADDRESS
5726	032174	012702	032312				MOV #5\$,R2		: POINTER TO CORRECT DATA
5727	032200	004737	035602				JSR PC,MEMLD		:LOAD 8 WORDS OF MAIN MEMORY
5728	032204	035726					MEMDAT		: POINTER TO DATA
5729	032206	004737	035636				JSR PC,SPLD		:LOAD 8 WORDS OF SP
5730	032212	035736					SPDAT		: POINTER TO DATA
5731	032214	004737	035714			1\$:	JSR PC,SETC		:SET C BIT!
5732	032220	042737	000017	032234			BIC #17,2\$:CLEAR ADDRESS FIELD OF INSTRUCTION
5733	032226	050037	032234				BIS R0,2\$:ADD ADDRESS TO INSTRUCTION
5734	032232	104412					ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5735	032234	010000				2\$:	010000		:LOAD MAR
5736	032236	042737	000017	032252			BIC #17,3\$:CLEAR ADDRESS OF INSTRUCTION
5737	032244	050037	032252				BIS R0,3\$:ADD ADDRESS TO INSTRUCTION
5738	032250	104412					ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5739	032252	040400				3\$:	040400! <00*20>		:BB + ADD
5740	032254	104412					ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5741	032256	061224					61224		:MOVE BR TO PORT4
5742	032260	111205					MOVB (R2),R5		:PUT "EXPECTED" IN R5

5743	032262	116104	000004						MOVB	4(R1),R4	:PUT "FOUND" IN R4
5744	032266	120504							CMPB	R5,R4	:DATA CORRECT?
5745	032270	001401							BEG	4\$:BR IF YES
5746	032272	104015							ERROR	15	:ALU ERROR
5747	032274	104405			4\$:				SCOPI		:SW09=1?
5748	032276	005202							INC	R2	:NEXT DATA
5749	032300	005200							INC	RO	:NEXT ADDRESS
5750	032302	022700	000010						CMP	#10,RO	:DONE YET?
5751	032306	001342							BNE	1\$:BR IF NO
5752	032310	104420							ADVANCE		:ADVANCE LOOP
5753	032312	000	377	377	5\$:				.BYTE	0,-1,-1,376,252,-1,-1,124	
5754	032315	376	252	377							
5755	032320	377	124								

.EVEN

```

5756
5757
5758
5759 ;***** TEST 120 *****
5760 ;#ALU TEST
5761 ;#TEST OF ALU FUNCTION 2A W/C WITH C BIT SET
5762 ;#ALU FUNCTION (A PLUS A PLUS C) CODE=6
5763 ;#LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
5764 ;#PERFORM THE FUNCTION, VERIFY THE RESULTS
5765 ;*****
5766
5767
5768 ; TEST 120
5769 ;-----

```

```

5770 032322 000004 000120 001202 ;*****
5771 032324 012737 000120 001202 ;TST120: SCOPE
5772 032332 012737 032500 001442 ;MOV #120,$STNM ; LOAD THE NO. OF THIS TEST
5773 032340 012737 032372 001444 ;MOV #TST121,NEXT ; POINT TO THE START OF NEXT TEST.
5774 ;MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
5775 032346 104410 ;R1 CONTAINS BASE KMC11 ADDRESS
5776 032350 005000 ;MASTER CLEAR KMC11
5777 032352 012702 032470 ;CLR RO ; MEM + SP ADDRESS
5778 032356 004737 035602 ;MOV #5$,R2 ; POINTER TO CORRECT DATA
5779 032362 035726 ;JSR PC,MEMLD ; LOAD 8 WORDS OF MAIN MEMORY
5780 032364 004737 035636 ;MEMDAT ; POINTER TO DATA
5781 032370 035736 ;JSR PC,SPLD ; LOAD 8 WORDS OF SP
5782 032372 004737 035714 ;SPDAT ; POINTER TO DATA
5783 032376 042737 000017 032412 1$: ;JSR PC,SETC ; SET C BIT!
5784 032404 050037 032412 ;BIC #17,2$ ; CLEAR ADDRESS FIELD OF INSTRUCTION
5785 032410 104412 ;BIS RO,2$ ; ADD ADDRESS TO INSTRUCTION
5786 032412 010000 ;ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5787 032414 042737 000017 032430 2$: ;010000 ; LOAD MAR
5788 032422 050037 032430 ;BIC #17,3$ ; CLEAR ADDRESS OF INSTRUCTION
5789 032426 104412 ;BIS RO,3$ ; ADD ADDRESS TO INSTRUCTION
5790 032430 040540 3$: ;ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5791 032432 104412 ;040400! <6*20> ; BR + 2A W/C
5792 032434 061224 ;ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5793 032436 111205 ;61224 ; MOVE BR TO PORT4
5794 032440 116104 000004 ;MOVB (R2),R5 ; PUT "EXPECTED" IN R5
5795 032444 120504 ;MOVB 4(R1),R4 ; PUT "FOUND" IN R4
5796 032446 001401 ;CMPB R5,R4 ; DATA CORRECT?
5797 032450 104015 ;BEG 4$ ; BR IF YES
5798 032452 104405 4$: ;ERROR 15 ; ALU ERROR
;SCOPI ; SW09=1?

```

```

5799 032454 005202      INC      R2      ;NEXT DATA
5800 032456 005200      INC      R0      ;NEXT ADDRESS
5801 032460 022700 000010  CMP      #10,R0 ;DONE YET?
5802 032464 001342      BNE      1$      ;BR IF NO
5803 032466 104420      ADVANCE ; ADVANCE LOOP
5804 032470      001      001      377 5$: .BYTE 1,1,-1,-1,253,253,125,125
5805 032473      377      253      253
5806 032476      125      125

```

.EVEN

```

5810 ***** TEST 121 *****
5811 *ALU TEST
5812 *TEST OF ALU FUNCTION SUB WITH C BIT SET
5813 *ALU FUNCTION (A-B) CODE=16
5814 *LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
5815 *PERFORM THE FUNCTION, VERIFY THE RESULTS
5816 *****

```

TEST 121

```

5820 *****
5821 032500 000004      †TST121: SCOPE
5822 032502 012737 000121 001202  MOV      #121,$STNM ; LOAD THE NO. OF THIS TEST
5823 032510 012737 032656 001442  MOV      #TST122,NEXT ; POINT TO THE START OF NEXT TEST.
5824 032516 012737 032550 001444  MOV      #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
5825 ; RI CONTAINS BASE KMC11 ADDRESS
5826 032524 104410      MSTCLR ; MASTER CLEAR KMC11
5827 032526 005000      CLR      R0 ; MEM + SP ADDRESS
5828 032530 012702 032646  MOV      #5$,R2 ; POINTER TO CORRECT DATA
5829 032534 004737 035602  JSR      PC,MEMLD ; LOAD 8 WORDS OF MAIN MEMORY
5830 032540 035726      MEMDAT ; POINTER TO DATA
5831 032542 004737 035636  JSR      PC,SPLD ; LOAD 8 WORDS OF SP
5832 032546 035736      SPDAT ; POINTER TO DATA
5833 032550 004737 035714 1$: JSR      PC,SETC ; SET C BIT!
5834 032554 042737 000017 032570  BIC      #17,2$ ; CLEAR ADDRESS FIELD OF INSTRUCTION
5835 032562 050037 032570      BIS      R0,2$ ; ADD ADDRESS TO INSTRUCTION
5836 032566 104412      ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5837 032570 010000 2$: 010000 ; LOAD MAR
5838 032572 042737 000017 032606  BIC      #17,3$ ; CLEAR ADDRESS OF INSTRUCTION
5839 032600 050037 032606      BIS      R0,3$ ; ADD ADDRESS TO INSTRUCTION
5840 032604 104412      ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5841 032606 040740 3$: 040400! <16*20> ; BR + SUB
5842 032610 104412      ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5843 032612 061224      61224 ; MOVE BR TO PORT4
5844 032614 111205      MOVB      (R2),R5 ; PUT "EXPECTED" IN R5
5845 032616 116104 000004      MOVB      4(R1),R4 ; PUT "FOUND" IN R4
5846 032622 120504      CMPB      R5,R4 ; DATA CORRECT?
5847 032624 001401      BEQ      4$ ; BR IF YES
5848 032626 104015      ERROR    15 ; ALU ERROR
5849 032630 104405      4$: SCOP1 ; SW09=1?
5850 032632 005202      INC      R2 ; NEXT DATA
5851 032634 005200      INC      R0 ; NEXT ADDRESS
5852 032636 022700 000010  CMP      #10,R0 ; DONE YET?
5853 032642 001342      BNE      1$ ; BR IF NO
5854 032644 104420      ADVANCE ; ADVANCE LOOP

```


5855 032646 000 001 377 5\$: .BYTE 0,1,-1,0,0,253,125,0
5856 032651 000 000 253
5857 032654 125 000
5858 .EVEN

***** TEST 122 *****
*ALU TEST
*TEST OF ALU FUNCTION ADD W/C WITH C BIT SET
*ALU FUNCTION (A PLUS B PLUS C) CODE=01
*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
*PERFORM THE FUNCTION, VERIFY THE RESULTS

TEST 122

5871
5872 032656 000004
5873 032660 012737 000122 001202
5874 032666 012737 033034 001442
5875 032674 012737 032726 001444
5876
5877 032702 104410
5878 032704 005000
5879 032706 012702 033024
5880 032712 004737 035602
5881 032716 035726
5882 032720 004737 035636
5883 032724 035736
5884 032726 004737 035714 1\$:
5885 032732 042737 000017 032746
5886 032740 050037 032746
5887 032744 104412
5888 032746 010000 2\$:
5889 032750 042737 000017 032764
5890 032756 050037 032764
5891 032762 104412
5892 032764 040420 3\$:
5893 032766 104412
5894 032770 061224
5895 032772 111205
5896 032774 116104 000004
5897 033000 120504
5898 033002 001401
5899 033004 104015
5900 033006 104405 4\$:
5901 033010 005202
5902 033012 005200
5903 033014 022700 000010
5904 033020 001342
5905 033022 104420
5906 033024 001 000 000 5\$:
5907 033027 377 253 000
5908 033032 000 125
5909 .EVEN
5910

:ST122: SCOPE
MOV #122,\$STNM ; LOAD THE NO. OF THIS TEST
MOV #ST123,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1\$,LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
CLR RO ; MEM + SP ADDRESS
MOV #5\$,R2 ; POINTER TO CORRECT DATA
JSR PC,MEMLD ; LOAD 8 WORDS OF MAIN MEMORY
MEMDAT ; POINTER TO DATA
JSR PC,SPLD ; LOAD 8 WORDS OF SP
SPDAT ; POINTER TO DATA
JSR PC,SETC ; SET C BIT!
BIC #17,2\$; CLEAR ADDRESS FIELD OF INSTRUCTION
BIS RO,2\$; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
010000 ; LOAD MAR
BIC #17,3\$; CLEAR ADDRESS OF INSTRUCTION
BIS RO,3\$; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
040400! <01*20> ; BR + ADD W/C
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
61224 ; MOVE BR TO PORT4
MOVB (R2),R5 ; PUT "EXPECTED" IN R5
MOVB 4(R1),R4 ; PUT "FOUND" IN R4
CMPB R5,R4 ; DATA CORRECT?
BEQ 4\$; BR IF YES
ERROR 15 ; ALU ERROR
SCOP1 ; SW09=1?
INC R2 ; NEXT DATA
INC RO ; NEXT ADDRESS
CMP #10,RO ; DONE YET?
BNE 1\$; BR IF NO
ADVANCE ; ADVANCE LOOP
5\$: .BYTE 1,0,0,-1,253,0,0,125

```

5911
5912
5913
5914
5915
5916
5917
5918
5919
5920
5921
5922
5923 033034 000004
5924 033036 012737 000123 001202
5925 033044 012737 033212 001442
5926 033052 012737 033104 001444
5927
5928 033060 104410
5929 033062 005000
5930 033064 012702 033202
5931 033070 004737 035602
5932 033074 035726
5933 033076 004737 035636
5934 033102 035736
5935 033104 004737 035714
5936 033110 042737 000017 033124
5937 033116 050037 033124
5938 033122 104412
5939 033124 010000
5940 033126 042737 000017 033142
5941 033134 050037 033142
5942 033140 104412
5943 033142 040440
5944 033144 104412
5945 033146 061224
5946 033150 111205
5947 033152 116104 000004
5948 033156 120504
5949 033160 001401
5950 033162 104015
5951 033164 104405
5952 033166 005202
5953 033170 005200
5954 033172 022700 000010
5955 033176 001342
5956 033200 104420
5957 033202 000 001 377
5958 033205 000 000 253
5959 033210 125 000
5960
5961
5962
5963
5964
5965
5966

```

```

***** TEST 123 *****
:ALU TEST
:TEST OF ALU FUNCTION SUB W/C WITH C BIT SET
:ALU FUNCTION (A-B-C) CODE=2
:LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
:PERFORM THE FUNCTION, VERIFY THE RESULTS
:*****

```

```

: TEST 123
:-----
:*****
TST123: SCOPE
MOV #123,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST124,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
;R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
CLR RO ; MEM + SP ADDRESS
MOV #5$,R2 ; POINTER TO CORRECT DATA
JSR PC,MEMLD ; LOAD 8 WORDS OF MAIN MEMORY
MEMDAT ; POINTER TO DATA
JSR PC,SPLD ; LOAD 8 WORDS OF SP
SPDAT ; POINTER TO DATA
JSR PC,SETC ; SET C BIT!
BIC #17,2$ ; CLEAR ADDRESS FIELD OF INSTRUCTION
BIS RO,2$ ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
010000 ; LOAD MAR
BIC #17,3$ ; CLEAR ADDRESS OF INSTRUCTION
BIS RO,3$ ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
040400! <2*20> ; BR + SUB W/C
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
61224 ; MOVE BR TO PORT4
MOV# (R2),R5 ; PUT "EXPECTED" IN R5
MOV# 4(R1),R4 ; PUT "FOUND" IN R4
CMPB R5,R4 ; DATA CORRECT?
BEQ 4$ ; BR IF YES
ERROR 15 ; ALU ERROR
SW09=1? ; SW09=1?
INC R2 ; NEXT DATA
INC RO ; NEXT ADDRESS
CMP #10,RO ; DONE YET?
BNE 1$ ; BR IF NO
ADVANCE ; ADVANCE LOOP
5$: .BYTE 0,1,-1,0,0,253,125,0

```

```

.EVEN
***** TEST 124 *****
:ALU TEST
:TEST OF ALU FUNCTION INC A WITH C BIT SET
:ALU FUNCTION (A PLUS 1) CODE=3

```

```

5967
5968
5969
5970
5971
5972
5973
5974 033212 000004
5975 033214 012737 000124 001202
5976 033222 012737 033370 001442
5977 033230 012737 033262 001444
5978
5979 033236 104410
5980 033240 005000
5981 033242 012702 033360
5982 033246 004737 035602
5983 033252 035726
5984 033254 004737 035636
5985 033260 035736
5986 033262 004737 035714
5987 033266 042737 000017 033302
5988 033274 050037 033302
5989 033300 104412
5990 033302 010000
5991 033304 042737 000017 033320
5992 033312 050037 033320
5993 033316 104412
5994 033320 040460
5995 033322 104412
5996 033324 061224
5997 033326 111205
5998 033330 116104 000004
5999 033334 120504
6000 033336 001401
6001 033340 104015
6002 033342 104405
6003 033344 005202
6004 033346 005200
6005 033350 022700 000010
6006 033354 001342
6007 033356 104420
6008 033360 001 001 000 55:
6009 033363 000 126 126
6010 033366 253 253
6011
6012
6013
6014
6015
6016
6017
6018
6019
6020
6021
6022

```

```

; *LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
; *PERFORM THE FUNCTION, VERIFY THE RESULTS
; *****
; TEST 124
; -----
; *****
TST124: SCOPE
MOV #124, STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST125, NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1$, LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
CLR R0 ; MEM + SP ADDRESS
MOV #5$, R2 ; POINTER TO CORRECT DATA
JSR PC, MEMLD ; LOAD 8 WORDS OF MAIN MEMORY
MEMDAT ; POINTER TO DATA
JSR PC, SPLD ; LOAD 8 WORDS OF SP
SPDAT ; POINTER TO DATA
1$: JSR PC, SETC ; SET C BIT!
BIC #17, 2$ ; CLEAR ADDRESS FIELD OF INSTRUCTION
BIS R0, 2$ ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
010000 ; LOAD MAR
2$: BIC #17, 3$ ; CLEAR ADDRESS OF INSTRUCTION
BIS R0, 3$ ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
040400! <3*20> ; BR + INC A
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
61224 ; MOVE BR TO PORT4
MOV# (R2), R5 ; PUT "EXPECTED" IN R5
MOV# 4(R1), R4 ; PUT "FOUND" IN R4
CMPB R5, R4 ; DATA CORRECT?
BEQ 4$ ; BR IF YES
ERROR 15 ; ALU ERROR
4$: SCOP1 ; SW09=1?
INC R2 ; NEXT DATA
INC R0 ; NEXT ADDRESS
CMP #10, R0 ; DONE YET?
BNE 1$ ; BR IF NO
ADVANCE ; ADVANCE LOOP
5$: .BYTE 1, 1, 0, 0, 126, 126, 253, 253
.EVEN
; ***** TEST 125 *****
; *ALU TEST
; *TEST OF ALU FUNCTION 2A WITH C BIT SET
; *ALU FUNCTION (A PLUS A) CODE=5
; *LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
; *PERFORM THE FUNCTION, VERIFY THE RESULTS
; *****
; TEST 125

```

```

6023
6024
6025 033370 000004
6026 033372 012737 000125 001202
6027 033400 012737 033546 001442
6028 033406 012737 033440 001444
6029
6030 033414 104410
6031 033416 005000
6032 033420 012702 033536
6033 033424 004737 035602
6034 033430 035726
6035 033432 004737 035636
6036 033436 035736
6037 033440 004737 035714
6038 033444 042737 000017 033460
6039 033452 050037 033460
6040 033456 104412
6041 033460 010000
6042 033462 042737 000017 033476
6043 033470 050037 033476
6044 033474 104412
6045 033476 040520
6046 033500 104412
6047 033502 061224
6048 033504 111205
6049 033506 116104 000004
6050 033512 120504
6051 033514 001401
6052 033516 104015
6053 033520 104405
6054 033522 005202
6055 033524 005200
6056 033526 022700 000010
6057 033532 001342
6058 033534 104420
6059 033536 000 000 376
6060 033541 376 252 252
6061 033544 124 124
6062
6063
6064
6065
6066
6067
6068
6069
6070
6071
6072
6073
6074
6075
6076 033546 000004
6077 033550 012737 000126 001202
6078 033556 012737 033724 001442

```

```

-----
*****
TST125: SCOPE
MOV #125,$STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST126,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
;R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
CLR R0 ; MEM + SP ADDRESS
MOV #5$,R2 ; POINTER TO CORRECT DATA
JSR PC,MEMLD ; LOAD 8 WORDS OF MAIN MEMORY
MEMDAT ; POINTER TO DATA
JSR PC,SPLD ; LOAD 8 WORDS OF SP
SPDAT ; POINTER TO DATA
1$: JSR PC,SETC ; SET C BIT!
BIC #17,2$ ; CLEAR ADDRESS FIELD OF INSTRUCTION
BIS R0,2$ ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
010000 ; LOAD MAR
2$: BIC #17,3$ ; CLEAR ADDRESS OF INSTRUCTION
BIS R0,3$ ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
040400! <5*20> ; BR + 2A
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
61224 ; MOVE BR TO PORT4
MOV (R2),R5 ; PUT "EXPECTED" IN R5
MOV 4(R1),R4 ; PUT "FOUND" IN R4
CMPB R5,R4 ; DATA CORRECT?
BEQ 4$ ; BR IF YES
ERROR 15 ; ALU ERROR
4$: SCCP! ; SW09=1?
INC R2 ; NEXT DATA
INC R0 ; NEXT ADDRESS
CMP #10,R0 ; DONE YET?
BNE 1$ ; BR IF NO
ADVANCE ; ADVANCE LOOP
5$: .BYTE 0,0,376,376,252,252,124,124
.EVEN
***** TEST 126 *****
*ALU TEST
*TEST OF ALU FUNCTION A PLUS C WITH C BIT SET
*ALU FUNCTION (A PLUS C) CODE=4
*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
*PERFORM THE FUNCTION, VERIFY THE RESULTS
*****
; TEST 126
-----
*****
TST126: SCOPE
MOV #126,$STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST127,NEXT ; POINT TO THE START OF NEXT TEST.

```

```

6079 033564 012737 033616 001444      MOV      #15,LOCK
6080                                     ; R1 CONTAINS BASE KMC11 ADDRESS
6081 033572 104410      MSTCLR
6082 033574 005000      CLR      RO
6083 033576 012702 033714      MOV      #55,R2
6084 033602 004737 035602      JSR      PC,MEMLD
6085 033606 035726      MEMDAT
6086 033610 004737 035636      JSR      PC,SPLD
6087 033614 035736      SPDAT
6088 033616 004737 035714 15:      JSR      PC,SETC
6089 033622 042737 000017 033636      BIC      #17,25
6090 033630 050037 033636      BIS      RO,25
6091 033634 104412      ROMCLK
6092 033636 010000 25:      010000
6093 033640 042737 000017 033654      BIC      #17,35
6094 033646 050037 033654      BIS      RO,35
6095 033652 104412      ROMCLK
6096 033654 040500 35:      040400! <4*20>
6097 033656 104412      ROMCLK
6098 033660 061224      61224
6099 033662 111205      MOV      (R2),R5
6100 033664 116104 000004      MOV      4(R1),R4
6101 033670 120504      CMP      R5,R4
6102 033672 001401      BEQ     45
6103 033674 104015      ERROR  15
6104 033676 104405 45:      SCOPI
6105 033700 005202      INC      R2
6106 033702 005200      INC      RO
6107 033704 022700 000010      CMP      #10,RO
6108 033710 001342      BNE     15
6109 033712 104420      ADVANCE
6110 033714 001 001 000 55:      .BYTE  1,1,0,0,126,126,253,253
6111 033717 000 126 126
6112 033722 253 253
6113                                     .EVEN

```

```

***** TEST 127 *****
: *ALU TEST
: *TEST OF ALU FUNCTION 2'S COMP SUB WITH C BIT SET
: *ALU FUNCTION (A-B-1) CODE=17
: *LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
: *PERFORM THE FUNCTION, VERIFY THE RESULTS
: *****

```

TEST 127

```

6127 033724 000004      TST127: SCOPE
6128 033726 012737 000127 001202      MOV      #127,$STNM ; LOAD THE NO. OF THIS TEST
6129 033734 012737 034102 001442      MOV      #TST130,NEXT ; POINT TO THE START OF NEXT TEST.
6130 033742 012737 033774 001444      MOV      #15,LOCK ; ADDRESS FOR LOCK ON DATA.
6131                                     ; R1 CONTAINS BASE KMC11 ADDRESS
6132 033750 104410      MSTCLR
6133 033752 005000      CLR      RO
6134 033754 012702 034072      MOV      #55,R2 ; MASTER CLEAR KMC11
; MEM + SP ADDRESS
; POINTER TO CORRECT DATA

```

6135	033760	004737	035602				JSR	PC, MEMLD	: LOAD 8 WORDS OF MAIN MEMORY
6136	033764	035726					MEMDAT		: POINTER TO DATA
6137	033766	004737	035636				JSR	PC, SPLD	: LOAD 8 WORDS OF SP
6138	033772	035736					SPDAT		: POINTER TO DATA
6139	033774	004737	035714	1\$:			JSR	PC, SETC	: SET C BIT!
6140	034000	042737	000017	034014			BIC	#17, 2\$: CLEAR ADDRESS FIELD OF INSTRUCTION
6141	034006	050037	034014				BIS	RO, 2\$: ADD ADDRESS TO INSTRUCTION
6142	034012	104412					ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6143	034014	010000		2\$:			010000		: LOAD MAR
6144	034016	042737	000017	034032			BIC	#17, 3\$: CLEAR ADDRESS OF INSTRUCTION
6145	034024	050037	034032				BIS	RO, 3\$: ADD ADDRESS TO INSTRUCTION
6146	034030	104412					ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6147	034032	040760		3\$:			040400! <17*20>		: BR + 2'S COMP SUB
6148	034034	104412					ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6149	034036	061224					61224		: MOVE BR TO PORT4
6150	034040	111205					MOVB	(R2), R5	: PUT "EXPECTED" IN R5
6151	034042	116104	000004				MOVB	4(R1), R4	: PUT "FOUND" IN R4
6152	034046	120504					CMPB	R5, R4	: DATA CORRECT?
6153	034050	001401					BEQ	4\$: BR IF YES
6154	034052	104015					ERROR	15	: ALU ERROR
6155	034054	104405		4\$:			SCOPI		: SW09=1?
6156	034056	005202					INC	R2	: NEXT DATA
6157	034060	005200					INC	RO	: NEXT ADDRESS
6158	034062	022700	000010				CMP	#10, RO	: DONE YET?
6159	034066	001342					BNE	1\$: BR IF NO
6160	034070	104420					ADVANCE		: ADVANCE LOOP
6161	034072	377	000	376	5\$:		.BYTE	-1, 0, 376, -1, -1, 252, 124, -1	
6162	034075	377	377	252					
6163	034100	124	377						

.EVEN

```

***** TEST 130 *****
: *ALU TEST
: *TEST OF ALU FUNCTION DEC A WITH C BIT SET
: *ALU FUNCTION (A-1) CODE=7
: *LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
: *PERFORM THE FUNCTION, VERIFY THE RESULTS
: *****

```

TEST 130

```

: *****
: *TST130: SCOPE
: MOV #130, $TSTNM ; LOAD THE NO. OF THIS TEST
: MOV #TST131, NEXT ; POINT TO THE START OF NEXT TEST.
: MOV #1$, LOCK ; ADDRESS FOR LOCK ON DATA.
: R1 CONTAINS BASE KMC11 ADDRESS
: *MSTCLR
: CLR RO ; MASTER CLEAR KMC11
: MOV #5$, R2 ; MEM + SP ADDRESS
: JSR PC, MEMLD ; POINTER TO CORRECT DATA
: MEMDAT ; LOAD 8 WORDS OF MAIN MEMORY
: JSR PC, SPLD ; POINTER TO DATA
: SPDAT ; LOAD 8 WORDS OF SP
: JSR PC, SETC ; POINTER TO DATA
: ; SET C BIT!

```

6191	034156	042737	000017	034172	BIC	#17,25	: CLEAR ADDRESS FIELD OF INSTRUCTION
6192	034164	050037	034172		BIS	RO,25	: ADD ADDRESS TO INSTRUCTION
6193	034170	104412			ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6194	034172	010000			010000		: LOAD MAR
6195	034174	042737	000017	034210	BIC	#17,35	: CLEAR ADDRESS OF INSTRUCTION
6196	034202	050037	034210		BIS	RO,35	: ADD ADDRESS TO INSTRUCTION
6197	034206	104412			ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6198	034210	040560			040400! <7*20>		: BR + DEC A
6199	034212	104412			ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6200	034214	061224			61224		: MOVE BR TO PORT4
6201	034216	111205			MOVB	(R2),R5	: PUT "EXPECTED" IN R5
6202	034220	116104	000004		MOVB	4(R1),R4	: PUT "FOUND" IN R4
6203	034224	120504			CMPB	R5,R4	: DATA CORRECT?
6204	034226	001401			BEQ	45	: BR IF YES
6205	034230	104015			ERROR	15	: ALU ERROR
6206	034232	104405			SCOPI		: SMO9=1?
6207	034234	005202			INC	R2	: NEXT DATA
6208	034236	005200			INC	RO	: NEXT ADDRESS
6209	034240	022700	000010		CMP	#10,RO	: DONE YET?
6210	034244	001342			BNE	15	: BR IF NO
6211	034246	104420			ADVANCE		: ADVANCE LOOP
6212	034250	377	377	376	.BYTE	-1,-1,376,376,124,124,251,251	
6213	034253	376	124	124			
6214	034256	251	251				
6215							.EVEN

```

6216
6217
6218 :***** TEST 131 *****
6219 :*TEST OF PROGRAM CLOCK BIT
6220 :*DO A MASTER CLEAR, VERIFY THAT PROGRAM CLOCK IS SET
6221 :*WRITE PROGRAM CLOCK BIT TO A ONE, VERIFY THAT IT CLEARS,
6222 :*AND THEN SETS SOME TIME LATER
6223 :*****

```

```

6224 :
6225 : TEST 131
6226 :-----
6227 :*****
6228 034260 000004 000131 001202 †ST131: SCOPE
6229 034262 012737 034466 001442 MOV #131,$STNM ; LOAD THE NO. OF THIS TEST
6230 034270 012737 MOV #TST132,NEXT ; POINT TO THE START OF NEXT TEST.
6231 :R1 CONTAINS BASE KMC11 ADDRESS
6232 034276 104410 MSTCLR ; MASTER CLEAR KMC11
6233 034300 005037 011106 CLR TEMP ; PREPARE FOR
6234 034304 005037 001276 CLR $TMP0 ; DELAY
6235 034310 012702 000011 MOV #11,R2 ; SAVE FOR TYPEOUT
6236 034314 104412 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6237 034316 121224 121224 ; PORT4+LUI1
6238 034320 016104 000004 MOV 4(R1),R4 ; PUT "FOUND" IN R4
6239 034324 042704 000357 BIC #357,R4 ; CLEAR UNWANTED BITS
6240 034330 012705 000020 MOV #20,R5 ; PUT "EXPECTED" IN R5
6241 034334 120504 CMPB R5,R4 ; IS PGM CLOCK SET?
6242 034336 001401 BEQ 15
6243 034340 104016 ERROR 16 ; ERROR, PGM CLOCK IS NOT SET
6244 034342 012761 000020 000004 15: MOV #20,4(R1) ; LOAD PORT 4
6245 034350 152761 000002 000001 BISB #BIT1,1(R1) ; SET ROMI
6246 034356 012761 121111 000006 MOV #121111,6(R1) ; SEL6 + INSTRUCTION

```

```

6247 034364 152761 000003 000001 B1SB #BIT1:BIT0,1(R1); SET CLOCK BIT
6248 034372 012761 121224 000006 MOV #121224,6(AI); LOAD NEXT INSTRUCTION
6249 034400 152761 000003 000001 B1SB #BIT1:BIT0,1(R1); READ CLOCK BIT
6250 034406 142761 000003 000001 B1CB #BIT1:BIT0,1(R1); CLEAR MAINT BITS
6251 034414 016104 000004 MOV 4(R1),R4; PUT "FOUND" IN R4
6252 034420 005005 CLR R5; PUT "EXPECTED" IN R5
6253 034422 120504 CMPB R5,R4; IS PGM CLOCK CLEAR?
6254 034424 001401 BEQ 2$
6255 034426 104016 ERROR 16; ERROR, PGM CLOCK IS NOT CLEAR
6256 034430 2$:
6257 034430 104412 ROMCLK; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6258 034432 121224; PORT4+LUI1
6259 034434 122761 000020 000004 CMPB #20,4(R1); IS PGM CLOCK SET?
6260 034442 001411 BEQ 3$; BR IF YES
6261 034444 005237 011106 INC TEMP; INCREMENT DELAY
6262 034450 005537 001276 ADC $TMPQ; INCREMENT DELAY
6263 034454 022737 000006 001276 CMP #6,$TMPQ; IS DELAY DONE
6264 034462 001362 BNE 2$; BR IF NO
6265 034464 104016 ERROR 16; ERROR PGM CLOCK NOT SET
6266 034466 3$:
6267
6268
6269 ;***** TEST 132 *****
6270 ;*FORCE POWER FAIL TEST
6271 ;*SET FORCE POWER FAIL BIT VERIFY THAT PROCESSOR TRAPS TO 24
6272 ;*GOING DOWN AND COMING UP. VERIFY ALSO THAT BUS INIT WAS
6273 ;*BLOCKED FROM GETTING TO THE KMC DURING THE POWER FAIL
6274 ;*****
6275
6276 ; TEST 132
6277 ;-----
6278
6279 034466 000004 ;*****
6280 034470 012737 000132 001202 †TST132: SCOPE
6281 034476 012737 034660 001442 MOV #132,$STNM; LOAD THE NO. OF THIS TEST
6282 MOV #TST133,NEXT; POINT TO THE START OF NEXT TEST.
6283 034504 104410 ;R1 CONTAINS BASE KMC11 ADDRESS
6284 034506 005037 011106 MSTCLR; MASTER CLEAR KMC11
6285 034512 013746 000024 CLR TEMP; PREPARE FOR DELAY
6286 034516 012737 034562 000024 MOV @#24,-(SP); STORE POWER FAIL ADDRESS
6287 034524 012761 000002 000004 MOV #15,@#24; SET UP FOR FORCE POWER FAIL
6288 034532 012711 001000 MOV #2,4(R1); LOAD PORT4
6289 034536 012761 121111 000006 MOV #BIT9,(R1); SET ROMI
6290 034544 012711 001400 MOV #121111,6(R1); LOAD INSTRUCTION
6291 034550 005237 011106 5$: MOV #BIT9:BIT8,(R1); CLOCK INSTRUCTION
6292 034554 001375 INC TEMP; WAIT FOR POWER FAIL
6293 034556 104017 BNE 5$; BR IF DELAY NOT DONE
6294 034560 000426 ERROR 17; ERROR, NO POWER FAIL
6295 034562 012737 034600 000024 1$: BR 4$
6296 034570 010637 034576 MOV #3$,@#24; POWER UP ADDRESS
6297 034574 000000 MOV SP,2$; STORE STACK
6298 034576 000000 HALT; WAIT FOR POWER UP SEQUENCE
6299 034600 013706 034576 2$: 0
6300 034604 022626 3$: MOV 2$,SP; RESTORE STACK
6301 034606 012637 000024 POP2SP; POP STACK TWICE
6302 034612 022737 007126 000024 MOV (SP)+,@#24; RESTORE TRUE POWER FAIL ADDRESS
CMP #SPWRDN,@#24; IS IT CORRECT?

```



```

6303 034620 001406 BEQ 4$ ;BR IF YES
6304 034622 104017 ERROR 17 ;ERROR, STACK IS INCORRECT
6305 034624 012737 007126 000024 MOV #SPWRDN,2#24 ;RESTORE TRUE POWER FAIL ADDRESS
6306 034632 012706 001200 MOV #STACK,SP ;RESTORE STACK
6307 034636 012711 003000 4$: MOV #BIT9!BIT10,(R1) ;SEL6 = MAINT IR
6308 034642 012705 121111 MOV #121111,R5 ;R5 = EXPECTED
6309 034646 016104 000004 MOV 4(R1),R4 ;R4 = FOUND
6310 034652 020504 CMP R5,R4 ;MAINT IR SHOULD = 12111
6311 034654 001401 BEQ +4 ;BR IF OK
6312 034656 104025 ERROR 25 ;IF = 0 THEN BUS INIT WAS
;NOT BLOCKED FROM CLEARING
;THE KMC-11

```

```

***** TEST 133 *****
;#MICRO-PROCESSOR NOISE TEST
;#WRITE ALL ZERO'S THEN ALL ONE'S THEN A DATA PATTERN
;#TO THE IBUS* AND IBUS REGISTERS AND TO THE SP AND MAIN MEM
;#THEN GO BACK AND READ THE DATA PATERNS TO VERIFY THAT
;#READING AND WRITING OF OTHER LOCATIONS AND REGISTERS
;#DID NOT CHANGE THE DATA.
*****

```

TEST 133

```

6328 *****
6329 034660 000004 ;#ST133: SCOPE
6330 034662 012737 000133 001202 MOV #133,STSTNM ; LOAD THE NO. OF THIS TEST
6331 034670 012737 003662 001442 MOV #SEOP,NEXT ; POINT TO THE END OF PASS HANDLER.
6332 ;R1 CONTAINS BASE KMC11 ADDRESS
6333 034676 104410 MSTCLR ;MASTER CLEAR KMC11
6334 034700 005002 CLR R2 ;R2 IS INDEX REGISTER
6335 034702 042737 000017 034726 1$: BIC #17,2$ ;CLEAR ADDRESS FIELD
6336 034710 156237 035502 034726 BISB 30$(R2),2$ ;ADD IBUS* REG ADDRESS TO INSTRUCTION
6337 034716 116261 035510 000004 MOVB 31$(R2),4(R1) ;LOAD PORT4
6338 034724 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6339 034726 121100 2$: 121100 ;WRITE IBUS* REGISTER
6340 034730 005202 INC R2 ;INC INDEX REGISTER
6341 034732 022702 000005 CMP #5,R2 ;DONE YET?
6342 034736 001361 BNE 1$ ;BR IF NO
6343 034740 005002 CLR R2 ;R2 IS IBUS REGISTER ADDRESS
6344 034742 042737 000017 035006 3$: BIC #17,4$ ;CLEAR ADDRESS FIELD OF INSTRUCTIONS
6345 034750 042737 000017 035020 BIC #17,5$
6346 034756 042737 000017 035030 BIC #17,6$
6347 034764 050237 035006 ;ADD IBUS REG ADDRESS TO INSTRUCTION
6348 034770 050237 035020 BIS R2,4$
6349 034774 050237 035030 BIS R2,5$
6350 035000 105061 000004 CLRB 4(R1) ;CLEAR PORT4
6351 035004 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6352 035006 122100 4$: 122100 ;WRITE 0 TO IBUS REG
6353 035010 112761 000377 000004 MOVB #377,4(R1) ;LOAD PORT4
6354 035016 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6355 035020 122100 5$: 122100 ;WRITE ALL ONES TO IBUS REG
6356 035022 110261 000004 MOVB R2,4(R1) ;LOAD PORT4
6357 035026 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6358 035030 122100 6$: 122100 ;WRITE ITS OWN ADDRESS TO IBUS REG

```

6359	035032	005202				INC	R2		:NEXT ADDRESS
6360	035034	022702	000010			CMP	#10,R2		:DONE YET?
6361	035040	001340				BNE	3\$:BR IF NO
6362	035042	005002				CLR	R2		:START AT SP ADDRESS 0
6363	035044	042737	000017	035110	7\$:	BIC	#17,8\$:CLEAR ADDRESS FIELD
6364	035052	042737	000017	035122		BIC	#17,9\$		
6365	035060	042737	000017	035132		BIC	#17,10\$		
6366	035066	050237	035110			BIS	R2,8\$:ADD ADDRESS TO INSTRUCTION
6367	035072	050237	035122			BIS	R2,9\$		
6368	035076	050237	035132			BIS	R2,10\$		
6369	035102	105061	000004			CLRB	4(R1)		:CLEAR PORT4
6370	035106	104412				ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6371	035110	123100			8\$:	123100			:WRITE ZERO TO SP
6372	035112	112761	000377	000004		MOVB	#377,4(R1)		:LOAD PORT4
6373	035120	104412				ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6374	035122	123100			9\$:	123100			:WRITE ALL ONES TO SP
6375	035124	110261	000004			MOVB	R2,4(R1)		:LOAD PORT4
6376	035130	104412				ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6377	035132	123100			10\$:	123100			:WRITE SP ADDRESS TO ITSELF
6378	035134	005202				INC	R2		:NEXT SP ADDRESS
6379	035136	022702	000020			CMP	#20,R2		:DONE YET?
6380	035142	001340				BNE	7\$:BR IF NO
6381	035144	005002				CLR	R2		:R2 = MAIN MEM ADDRESS
6382	035146	104412				ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6383	035150	010000				010000			:MAR + 0
6384	035152	105061	000004		11\$:	CLR	4(R1)		:CLEAR PORT4
6385	035156	104412				ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6386	035160	122500				122500			:WRITE ZEROS TO MEM
6387	035162	112761	000377	000004		MOVB	#377,4(R1)		:LOAD PORT4
6388	035170	104412				ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6389	035172	122500				122500			:WRITE ONES TO MEM
6390	035174	110261	000004			MOVB	R2,4(R1)		:LOAD PORT4
6391	035200	104412				ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6392	035202	136500				136500			:WRITE TO MEM IT OWN ADDRESS
6393	035204	005202				INC	R2		:NEXT MEM ADDRESS
6394	035206	022702	001000		CMP	#1000,R2			:DONE YET?
6395	035212	001357				BNE	11\$:BR IF NO
6396									
6397									
6398									:NOW GO BACK AND READ EVERYTHING
6399	035214	104412				ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6400	035216	010000				010000			:MAR+0
6401	035220	104412				ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6402	035222	004000				4000			:MAR HI + 0 (KMC ONLY)
6403	035224	005000				CLR	R0		:R0 IS INDEX REGISTER
6404	035226	042737	000360	035264	12\$:	BIC	#360,13\$:CLEAR ADDRESS FIELD
6405	035234	116002	035502			MOVB	30\$(R0),R2		:R2 = IBUS* ADDRESS
6406	035240	010203				MOV	R2,R3		:PUT IBUS* ADDRESS IN R3
6407	035242	006303				ASL	R3		:SHIFT ADDRESS TO BITS 4-7
6408	035244	006303				ASL	R3		
6409	035246	006303				ASL	R3		
6410	035250	006303				ASL	R3		
6411	035252	050337	035264			BIS	R3,13\$:ADD ADDRESS TO INSTRUCTION
6412	035256	116005	035510			MOVB	31\$(R0),R5		:R5 = "EXPECTED"
6413	035262	104412				ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6414	035264	121004			13\$:	121004			:PORT4 + IBUS* REGISTER

6415	035266	016104	000004			MOV	4(R1),R4		;R4 = "FOUND"
6416	035272	120504				CMPB	R5,R4		;IBUS# CONTENTS OK?
6417	035274	001401				BEQ	.+4		;BR IF YES
6418	035276	104004				ERROR	4		;IBUS# DATA ERROR
6419	035300	005200				INC	R0		;INC COUNTER
6420	035302	022700	000005			CMP	#5,R0		;DONE YET?
6421	035306	001347				BNE	12\$;BR IF NO
6422	035310	005002				CLR	R2		;R2 = IBUS REG ADDRESS
6423	035312	042737	000360	035342	14\$:	BIC	#360,15\$;CLEAR ADDRESS FIELD OF INSTRUCTION
6424	035320	010203				MOV	R2,R3		;R3 = IBUS ADDRESS
6425	035322	006303				ASL	R3		;SHIFT ADDRESS TO BITS 4-7
6426	035324	006303				ASL	R3		
6427	035326	006303				ASL	R3		
6428	035330	006303				ASL	R3		
6429	035332	050337	035342			BIS	R3,15\$;ADD ADDRESS TO INSTRUCTION
6430	035336	010205				MOV	R2,R5		;R5 = "EXPECTED"
6431	035340	104412				ROMCLK			;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6432	035342	021004			15\$:	021004			;PORT4 + IBUS REG
6433	035344	016104	000004			MOV	4(R1),R4		;R4 = "FOUND"
6434	035350	120504				CMPB	R5,R4		;IBUS CONTENTS OK?
6435	035352	001401				BEQ	.+4		;BR IF YES
6436	035354	104005				ERROR	5		;IBUS DATA ERROR
6437	035356	005202				INC	R2		;NEXT IBUS REGISTER
6438	035360	022702	000010			CMP	#10,R2		;DONE YET?
6439	035364	001352				BNE	14\$;BR IF NO
6440	035366	005002				CLR	R2		;R2 = SP ADDRESS
6441	035370	042737	000017	035404	16\$:	BIC	#17,17\$;CLEAR	;CLEAR ADDRESS FIELD OF INSTRUCTION
6442	035376	050237	035404			BIS	R2,17\$;ADD ADDRESS TO INSTRUCTION
6443	035402	104412				ROMCLK			;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6444	035404	040600			17\$:	040600			;BR + SP
6445	035406	010205				MOV	R2,R5		;R5 = "EXPECTED"
6446	035410	104412				ROMCLK			;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6447	035412	061224				061224			;PORT4 + BR
6448	035414	016104	000004			MOV	4(R1),R4		;R4 = "FOUND"
6449	035420	120504				CMPB	R5,R4		;SP CONTENTS OK?
6450	035422	001401				BEQ	.+4		;BR IF YES
6451	035424	104007				ERROR	7		;SP DATA ERROR
6452	035426	005202				INC	R2		;NEXT SP LOCATION
6453	035430	022702	000020			CMP	#20,R2		;DONE YET?
6454	035434	001355				BNE	16\$;BR IF NO
6455	035436	005002				CLR	R2		;R2 = MEMORY ADDRESS
6456	035440	104412				ROMCLK			;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6457	035442	010000				010000			;MAR + 0
6458	035444	104412				ROMCLK			;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6459	035446	004000				4000			;MAR HI + 0 (KMC ONLY)
6460	035450	010205			18\$:	MOV	R2,R5		;R5 = "EXPECTED"
6461	035452	104412				ROMCLK			;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6462	035454	055224				055224			;PORT4 + MAIN MEM
6463	035456	016104	000004			MOV	4(R1),R4		;R4 = "FOUND"
6464	035462	120504				CMPB	R5,R4		;MAIN MEM CONTENTS OK?
6465	035464	001401				BEQ	.+4		;BR IF YES
6466	035466	104013				ERROR	13		;MAIN MEM DATA ERROR
6467	035470	005202				INC	R2		;NEXT MEM ADDRESS
6468	035472	022702	001000		CMP	#1000,R2			;DONE YET?
6469	035476	001364				BNE	18\$;BR IF NO
6470	035500	104420				ADVANCE			; ADVANCE LOOP


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6527 035636          SPLD:
6528                ;THIS SUBROUTINE LOADS THE FIRST 8 SCRATCH PAD
6529                ;LOCATIONS WITH: 0,0,-1,-1,125,125,252,252
6530
6531 035636 013605          MOV    @ (SP)+,R5      ;PUT POINTER TO DATA IN R5
6532 035640 062746 000002    ADD    #2,-(SP)      ;ADJUST STACK
6533 035644 005004          CLR    R4            ;START AT SP ADDRESS 0
6534 035646 112577 144222    1$:   MOVB  (R5)+,@KMP04   ;LOAD PORT4 WITH DATA
6535 035652 042737 000017    BIC   #17,2$        ;CLEAR ADDRESS FIELD OF INSTRUCTION
6536 035660 050437 035666    BIS   R4,2$         ;ADD ADDRESS TO INSTRUCTION
6537 035664 104412          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6538 035666 123100          2$:   123100      ;MOVE DATA TO SP
6539 035670 005204          INC    R4            ;INCREMENT COUNT
6540 035672 022704 000010    CMP   #10,R4        ;DONE YET?
6541 035676 001363          BNE   1$            ;BR IF NO
6542 035700 000207          RTS    PC            ;RETURN
6543
6544
6545 035702          CLRC:
6546                ;THIS SUBROUTINE CLEARS THE MICRO PROCESSOR C BIT
6547
6548 035702 104412          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6549 035704 010000          010000      ;MAR+0
6550 035706 104412          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6551 035710 040400          040400!<0*20> ;CLEAR C BIT
6552 035712 000207          RTS    PC            ;RETURN
6553
6554
6555 035714          SETC:
6556                ;THIS SUBROUTINE SETS THE MICRO PROCESSOR C BIT
6557
6558 035714 104412          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6559 035716 010003          010003      ;MAR+3
6560 035720 104412          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6561 035722 040403          040403!<0*20> ;SET C BIT
6562 035724 000207          RTS    PC            ;RETURN
6563
6564
6565 035726      000      377      000  MEMDAT: .BYTE 0,-1,0,-1,125,252,125,252
6566 035731      377      125      252
6567 035734      125      252
6568 035736      000      000      377  SPDAT: .BYTE 0,0,-1,-1,125,125,252,252
6569 035741      377      125      125
6570 035744      252      252
6571
6572 035746 052600 044516 052502 .EVEN
036013      200 047125 041111 EM1: .ASCIZ <200>/UNIBUS REGISTER ADDRESSING TIME-OUT/
036054 046600 041511 047522 EM2: .ASCIZ <200>/UNIBUS REGISTER WRITE/READ TEST/
036102 046600 041511 047522 EM3: .ASCIZ <200>/MICRO PROCESSOR TEST/
036143      200 051102 051040 EM4: .ASCIZ <200>/MICRO PROCESSOR WRITE/READ TEST/
036165      200 041523 040522 EM5: .ASCIZ <200>/BR REGISTER TEST/
036207      200 042504 044526 EM6: .ASCIZ <200>/SCRATCH PAD TEST/
036243      200 042504 044526 EM7: .ASCIZ <200>/DEVICE FAILED TO INTERRUPT/
036307      200 050116 020122 EM10: .ASCIZ <200>/DEVICE INTERRUPTED TO WRONG VECTOR/
036321      200 040515 047111 EM11: .ASCIZ <200>/NPR TEST/
036343      200 040515 020122 EM12: .ASCIZ <200>/MAIN MEMORY TEST/
EM13: .ASCIZ <200>/MAR TEST/
    
```

036355	200	046101	020125	EM14:	.ASCIZ	<200>/ALU TEST/		
036367	200	051120	043517	EM15:	.ASCIZ	<200>/PROGRAM CLOCK TEST/		
036413	200	047506	041522	EM16:	.ASCIZ	<200>/FORCE POWER FAIL ERROR/		
036443	200	047125	054105	EM17:	.ASCIZ	<200>/UNEXPECTED INTERRUPT/		
036471	200	046513	030503	EM20:	.ASCIZ	<200>/KMC11 CONFIGURATION ERROR/		
036524	046600	044501	052116	EM21:	.ASCIZ	<200>/MAINTENANCE INSTRUCTION REGISTER TEST/		
036573	200	047520	042527	EM22:	.ASCIZ	<200>/POWER FAIL INITIALIZE FAILURE/		
036632	051200	043505	051511	DH1:	.ASCIZ	<200>/REGISTER	TRAPPED FROM/	
036673	200	054105	042520	DH2:	.ASCIZ	<200>/EXPECTED	FOUND	REGISTER/
036731	200	054105	042520	DH3:	.ASCIZ	<200>/EXPECTED	FOUND/	
036752	042600	050130	041505	DH4:	.ASCIZ	<200>/EXPECTED	FOUND	IBUS* REGISTER/
037014	042600	050130	041505	DH5:	.ASCIZ	<200>/EXPECTED	FOUND	IBUS REGISTER/
037055	200	054105	042520	DH6:	.ASCIZ	<200>/EXPECTED	FOUND	ADDRESS/
					.EVEN			
037112	000002			DT1:	2			
037114	006	015			.BYTE	6,15		
037116	001264				\$REG1			
037120	006	002			.BYTE	6,2		
037122	001266				\$REG2			
037124	000003			DT2:	3			
037126	006	004			.BYTE	6,4		
037130	001274				\$REG5			
037132	006	004			.BYTE	6,4		
037134	001272				\$REG4			
037136	006	002			.BYTE	6,2		
037140	001264				\$REG1			
037142	000002			DT3:	2			
037144	006	004			.BYTE	6,4		
037146	001274				\$REG5			
037150	006	002			.BYTE	6,2		
037152	001272				\$REG4			
037154	000003			DT4:	3			
037156	003	007			.BYTE	3,7		
037160	001274				\$REG5			
037162	003	011			.BYTE	3,11		
037164	001272				\$REG4			
037166	002	002			.BYTE	2,2		
037170	001266				\$REG2			
037172	000003			DT5:	3			
037174	003	007			.BYTE	3,7		
037176	001274				\$REG5			
037200	003	007			.BYTE	3,7		
037202	001272				\$REG4			
037204	006	002			.BYTE	6,2		
037206	001266				\$REG2			
037210	000002			DT6:	2			
037212	003	007			.BYTE	3,7		
037214	001274				\$REG5			
037216	003	002			.BYTE	3,2		
037220	001272				\$REG4			
037222	000002			DT7:	2			
037224	006	004			.BYTE	6,4		
037226	001264				\$REG1			
037230	006	002			.BYTE	6,2		

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PAGE: 0150

037232 002066
037234 000001

KMCSR
CORMAX:
.END

CROSS REFERENCE TABLE -- USER SYMBOLS

CORMAX	037234	4501	4533	6572#						
CR	= 000015	44#	1135	1145						
CREAM	001502	354#	707*	1841*	1842	1844*	1848			
CRLF	= 000200	45#	1106	1145						
CSR	010363	1740#	1945							
CSRMAP	012112	1921#								
CYCLE	011460	916	977	1832#						
DATABP	006764	1571*	1574	1596	1599#					
DATACL	= 104413	1535#								
DATAHD	006752	1570*	1592	1595#						
DDISP	= 177570	51#	207#	236						
DELAY	= 104411	1533#								
DEVTAB	003342	804	851#							
DH1	036632	386	6572#							
DH2	036673	389	6572#							
DH3	036731	392	401	413	422	437	440	446	6572#	
DH4	036752	395	425	6572#						
DH5	037014	398	6572#							
DH6	037055	404	416	419	434	6572#				
DISPLA	001242	236#	726*	732*	1044*					
DISPRE	000174	197#	732							
DSMR	= 177570	50#	206#	235						
DT1	037112	387	6572#							
DT2	037124	390	6572#							
DT3	037142	393	414	441	447	6572#				
DT4	037154	396	426	6572#						
DT5	037172	399	405	417	420	435	6572#			
DT6	037210	402	423	6572#						
DT7	037222	438	6572#							
DZDME	= *****	382								
DZDMG	= *****	382								
EMTVEC	= 000030	139#								
EM1	035746	385	6572#							
EM10	036243	409	6572#							
EM11	036307	412	433	6572#						
EM12	036321	415	6572#							
EM13	036343	418	6572#							
EM14	036355	421	6572#							
EM15	036367	424	6572#							
EM16	036413	427	6572#							
EM17	036443	430	6572#							
EM2	036013	388	6572#							
EM20	036471	436	442	6572#						
EM21	036524	439	6572#							
EM22	036573	445	6572#							
EM3	036054	391	6572#							
EM4	036102	394	397	6572#						
EM5	036143	400	6572#							
EM6	036165	403	6572#							
EM7	036207	406	6572#							
ERCT00	002304	591#								
ERCT01	002310	594#								
ERCT02	002314	597#								
ERCT03	002320	600#								
ERCT04	002324	603#								
ERCT05	002330	606#								

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CROSS REFERENCE TABLE -- USER SYMBOLS

NOACT	010731	751	1740#	1834															
NODEV	003240	802	824#																
NPRSET	035540	4239	4273	4311	4347	4388	4424	4461	4508	6492#									
NUM	010323	1740#	1933																
OK	003220	816	819#	842															
ONE	001464	346#																	
PACT00	002302	590#																	
PACT01	002306	593#																	
PACT02	002312	596#																	
PACT03	002316	599#																	
PACT04	002322	602#																	
PACT05	002326	605#																	
PACT06	002332	608#																	
PACT07	002336	611#																	
PACT10	002342	614#																	
PACT11	002346	617#																	
PACT12	002352	620#																	
PACT13	002356	623#																	
PACT14	002362	626#																	
PACT15	002366	629#																	
PACT16	002372	632#																	
PACT17	002376	635#																	
PARBIT=	040000	159#																	
PERFOR=	004537	159#																	
PFTAB	007324	1659	1681#																
PIRQ =	177772	49#																	
PIRQVE=	000240	143#																	
POPRD =	012600	154#	1614																
POP1SP=	005726	152#																	
POP2SP=	022626	156#	6300																
PRI0	010422	1740#	1961																
PRIORITY	013730	2182*	2188*	2201	2222#														
PRO =	000000	66#	2158	2159															
PR1 =	000040	67#																	
PR2 =	000100	68#																	
PR3 =	000140	69#																	
PR4 =	000200	70#	2160																
PR5 =	000240	71#	2161																
PR6 =	000300	72#	2162																
PR7 =	000340	73#	178	180	182	184	2163												
PS =	177776	46#	47	700*	909*	2127*	2137*	4095*	4099*	4125*	4129*	4153*	4167*	4193*					
		4209#																	
PSW =	177776	47#																	
PUSHRO=	010046	153#	1611																
PUSH1S=	005746	151#																	
PUSH2S=	024646	155#																	
PMRVEC=	000024	138#	1637*	1638*	1647*	1653*	1672*	1673*											
QV.FLG	001511	362#	706*	956*															
RDOCHR =	104402	1253	1526#																
RDLIN =	104403	1326	1527#																
RDOCT =	104404	1375	1528#																
RESREG	006766	1597	1600#																
RESVEC=	000010	133#																	
RESOS =	104407	1531#	1600																
ROMCLK=	104412	1534#	1687	1690	1727	1732	3094	3096	3114	3116	3151	3153	3171	3173					
		3207	3209	3225	3227	3260	3262	3278	3280	3314	3316	3334	3336	3371					

CROSS REFERENCE TABLE -- USER SYMBOLS

		3373	3392	3394	3429	3431	3447	3449	3482	3484	3500	3502	3535	3537
		3553	3555	3588	3590	3606	3608	3641	3643	3659	3661	3694	3696	3712
		3714	3747	3749	3765	3767	3800	3802	3818	3820	3855	3863	3881	3915
		3917	3933	3935	3969	3973	3975	3992	3996	3998	4037	4041	4043	4061
		4063	4097	4127	4165	4207	4246	4280	4284	4286	4318	4353	4361	4363
		4399	4401	4430	4433	4436	4467	4470	4473	4515	4565	4567	4569	4571
		4612	4616	4618	4663	4667	4669	4714	4718	4720	4765	4769	4771	4816
		4820	4822	4867	4871	4873	4918	4922	4924	4969	4973	4975	5020	5024
		5026	5071	5075	5077	5122	5126	5128	5173	5177	5179	5224	5228	5230
		5275	5279	5281	5326	5330	5332	5377	5381	5383	5428	5432	5434	5479
		5483	5485	5530	5534	5536	5581	5585	5587	5632	5636	5638	5683	5687
		5689	5734	5738	5740	5785	5789	5791	5836	5840	5842	5887	5891	5893
		5938	5942	5944	5989	5993	5995	6040	6044	6046	6091	6095	6097	6142
		6146	6148	6193	6197	6199	6236	6257	6338	6351	6354	6357	6370	6373
		6376	6382	6385	6388	6391	6399	6401	6413	6431	6443	6446	6456	6458
		6461	6501	6517	6520	6537	6548	6550	6558	6560				
RUN	001500	352#	709*	1838*	1839*	1846								
SAVACT	001474	350#	869	2098*	2190*									
SAVNUM	001476	351#	703*	954*	957*	2091*	2184*							
SAVPC	001460	344#	830*	845	1407*	1626								
SAVSP	001456	343#												
SAVDS =	104406	1530#	1559											
SCOP1 =	104405	1529#	2244	2298	2311	2339	2346	2371	2378	2403	2410	2435	2442	2467
		2474	2499	2506	2531	2538	2563	2570	2595	2602	2627	2634	2659	2666
		2691	2698	2723	2730	2755	2762	2787	2794	2819	2826	2853	2867	2897
		2911	2941	2954	2983	2991	3000	3025	3033	3042	3104	3124	3161	3181
		3216	3234	3269	3287	3324	3344	3382	3403	3438	3456	3491	3509	3544
		3562	3597	3615	3650	3668	3703	3721	3756	3774	3809	3827	3870	3888
		3924	3942	3982	4005	4050	4070	4523	4578	4625	4676	4727	4778	4829
		4880	4931	4982	5033	5084	5135	5186	5237	5288	5339	5390	5441	5492
		5543	5594	5645	5696	5747	5798	5849	5900	5951	6002	6053	6104	6155
SETC	035714	6206												
		5425	5476	5527	5578	5629	5680	5731	5782	5833	5884	5935	5986	6037
SETVEC	035516	6088	6139	6190	6555#									
SOFTSM	011452	4091	4121	4160	4202	6482#								
SPACNT=	006411	1781	1820#											
SPDAT	035736	1442*	1466	1469*	1483#									
		4608	4659	4710	4761	4812	4863	4914	4965	5016	5067	5118	5169	5220
		5271	5322	5373	5424	5475	5526	5577	5628	5679	5730	5781	5832	5883
		5934	5985	6036	6087	6138	6189	6568#						
SPLD	035636	4562	4607	4658	4709	4760	4811	4862	4913	4964	5015	5066	5117	5168
		5219	5270	5321	5372	5423	5474	5525	5576	5627	5678	5729	5780	5831
		5882	5933	5984	6035	6086	6137	6188	6527#					
STACK =	001200	37#	701	888	1621	4104	4134	6306						
STAT	001450	340#												
STAT1	002050	476#	1853*	4154	4194									
STAT2	002052	477#	1854*											
STAT3	002054	478#	1855*											
STKLMT=	177774	48#												
STRTSM	001446	339#	741*	744*	745	747	761*	767	769	864	910	917	1875	1898*
		1928	2111											
SVDS	006100	1411#												
SMFLG	011416	704*	1776*	1803*	1809#									
SMR	001240	235#	725*	727	731*	741	869	874	1014	1032	1056	1548	1553	1609
		1616	1618	1645	1665*	1705	1765	1802*						
SMREG	000176	198#	720*	731	1765	1822								

TST121	032500	5772	5821#	
TST122	032656	5823	5872#	
TST123	033034	5874	5923#	
TST124	033212	5925	5974#	
TST125	033370	5976	6025#	
TST126	033546	6027	6076#	
TST127	033724	6078	6127#	
TST13	015104	2521	2551#	
TST130	034102	6129	6178#	
TST131	034260	6180	6228#	
TST132	034466	6230	6279#	
TST133	034660	6281	6329#	6572
TST134=	***** U	6331		
TST14	015202	2553	2583#	
TST15	015300	2585	2615#	
TST16	015376	2617	2647#	
TST17	015474	2649	2679#	
TST2	014042	2235	2263#	
TST20	015572	2681	2711#	
TST21	015670	2713	2743#	
TST22	015766	2745	2775#	
TST23	016064	2777	2807#	
TST24	016162	2809	2839#	
TST25	016306	2841	2883#	
TST26	016432	2885	2927#	
TST27	016562	2929	2970#	
TST3	014072	2265	2284#	
TST30	016722	2972	3012#	
TST31	017064	3014	3056#	
TST32	017150	3058	3083#	
TST33	017350	3085	3140#	
TST34	017550	3142	3197#	
TST35	017724	3199	3250#	
TST36	020100	3252	3303#	
TST37	020300	3305	3360#	
TST4	014222	2286	2327#	
TST40	020510	3362	3419#	
TST41	020664	3421	3472#	
TST42	021040	3474	3525#	
TST43	021214	3527	3578#	
TST44	021370	3580	3631#	
TST45	021544	3633	3684#	
TST46	021720	3686	3737#	
TST47	022074	3739	3790#	
TST5	014320	2329	2359#	
TST50	022250	3792	3843#	
TST51	022476	3845	3906#	
TST52	022646	3908	3958#	
TST53	023114	3960	4025#	
TST54	023336	4027	4085#	
TST55	023432	4087	4116#	
TST56	023524	4118	4147#	
TST57	023646	4149	4187#	
TST6	014416	2361	2391#	
TST60	024014	4189	4232#	
TST61	024122	4234	4267#	

CROSS REFERENCE TABLE -- USER SYMBOLS

SERFLG	001203	218#	705*	937*	999	1028	1030*	1051	1558*	1572	1586*	1660*		
SERMAX	001215	224#	1051											
SERROR	006512	181	1547#											
SERRPC	001216	225#	714*	958*	1007*	1555	1557*	1661*						
SERRTB	001512	379#	1568											
SERTTL	001212	222#	949	989	1615*	1857*								
SETABL	001336	276#												
SETEND	001442	329#	470											
SFATAL	001320	269#	1185*											
SFFLG	005142	1148#	1151*	1179	1188*	1196#								
SFILLC	001256	243#	1114	1145										
SFILLS	001255	242#	1145											
SGADR	001220	226#												
SGDAT	001224	228#												
SGET42	004060	968#												
SGTSMR=	***** U	1525												
SHD =	000000	11												
SHIBTS	002034	465#												
SHIOCT	005722	1348#	1359#											
SICNT	001204	219#	1036*	1037	1039*	1050								
SILLUP	007316	1637	1653	1677#										
SINPUT	005724	1364#	1537											
SINTAG	001235	233#												
SITEMB	001214	223#	1563*	1603										
SLF	001314	261#	1145	1290	1300	1360								
SLFLG	005141	1189#	1195#											
SLPADR	001206	220#	716*	916*	920	1043*	1045	1050	1620*	1622	1896*	1906* 1908		
SLPERR	001210	221#												
SMADR1	001350	294#												
SMADR2	001354	298#												
SMADR3	001360	301#												
SMADR4	001364	304#												
SMAIL	001316	267#	466	470	1042	1089								
SMAMS1	001346	288#	2185											
SMAMS2	001352	296#												
SMAMS3	001356	299#												
SMAMS4	001362	302#												
SMBADR	002036	466#												
SMFLG	005140	1149#	1155	1190*	1194#									
SMNEW	005552	1304#	1782											
SMGAD	001332	274#	1165*	1168										
SMGLG	001334	275#	1170*											
SMGTY	001316	268#	1163	1171*	1183	1187*								
SMWR	005541	1302#	1779											
SMTYP1	001347	289#												
SMTYP2	001353	297#												
SMTYP3	001357	300#												
SMTYP4	001363	303#												
SMXCNT	004362	1040	1050#											
SN =	000133	1#	2223	2228	2230	2238#	2254	2258	2260	2267#	2273	2279	2281	2289
		2290#	2316	2322	2324	2331	2332#	2348	2354	2356	2363	2364#	2380	2386
		2388	2395	2396#	2412	2418	2420	2427	2428#	2444	2450	2452	2459	2460#
		2476	2482	2484	2491	2492#	2508	2514	2516	2523	2524#	2540	2546	2548
		2555	2556#	2572	2578	2580	2587	2588#	2604	2610	2612	2619	2620#	2636
		2642	2644	2651	2652#	2668	2674	2676	2683	2684#	2700	2706	2708	2715
		2716#	2732	2738	2740	2747	2748#	2764	2770	2772	2779	2780#	2796	2802

.SAVOS	006072	1407#	1530		
.SCOP1	004364	1055#	1529		
.START	002402	201	700#	716	1799
.TIMER	007512	1536	1723#		
.\$ASTA=	***** U	1149	1152		
.\$X =	002034	454#	459		

TYPNUM	1448														
TYPOCS	1448														
TYPOCT	1448														
TYPTXT	1448														
SADD1	18	2223													
SADD2	18	2254													
SADD3	18	2273	2916												
SADD4	18	2316	2348	2380	2412	2444	2476	2508	2540	2572	2604	2636	2668	2700	2732
	2764	2796													
SALU	18	4584	4635	4686	4737	4788	4839	4890	4941	4992	5043	5094	5145	5196	5247
	5298	5349	5400	5451	5502	5553	5604	5655	5706	5757	5808	5859	5910	5961	6012
	6063	6114	6165												
SALUD	18	4544													
SAUTO	18	785													
SBR	18	3912	3929												
SBUFFE	18	1752													
SCOMP	18	6238	6251												
SCYCLE	18	1823													
SEOP	18	921													
SERTBL	18	381													
SFINI	18	6572													
SFLOAT	18	3090	3109	3147	3166	3204	3221	3257	3274	3310	3329	3367	3387	3426	3443
	3479	3496	3532	3549	3585	3602	3638	3655	3691	3708	3744	3761	3797	3814	
SGETPA	18														
SHEADE	18	11													
SINTR	18	4075	4106												
SIR	18	2959	3001												
SMARHI	18	6401	6458												
SMEMFL	18														
SMEMO	18														
SMEM1	18														
SMEM2	18														
SMEM3	18														
SNOCK	18														
SMSG	18	1740													
SNOISE	18	6315													
SNPRBI	18	4482													
SNPR1	18	4222	4257	4295											
SNPR2	18	4329	4370												
SNPR3	18	4408	4445												
SPAEN	18	935													
SPFAIL	18	1630													
SPOWER	18	6267													
SPRIO	18	4136	4176												
SPROC1	18	3043													
SPROC2	18	3072	3129	3186	3239	3292	3349	3408	3461	3514	3567	3620	3673	3726	3779
SPROC3	18	3832													
SPROC4	18	3895													
SPROCS	18														
SQUEST	18	1932	1944	1952	2009	2017									
SRAMCL	18	1684													
SRCLK	18	1687	1690	1727	1732	3094	3096	3114	3116	3151	3153	3171	3173	3207	3209
	3225	3227	3260	3262	3278	3280	3314	3316	3334	3336	3371	3373	3392	3394	3429
	3431	3447	3449	3482	3484	3500	3502	3535	3537	3553	3555	3588	3590	3606	3608
	3641	3643	3659	3661	3694	3696	3712	3714	3747	3749	3765	3767	3800	3802	3818
	3820	3855	3863	3881	3915	3917	3933	3935	3969	3973	3975	3992	3996	3998	4037

	1540	
SSSKIP	1448	
.EQUAT	18	34
.HEADE	18	
.SETUP	18	
.SACT1	18	185
.SAPT8	18	2638
.SAPTH	18	449
.SAPTY	18	1145
.SCATC	18	
.SCHTA	18	208
.SEOP	18	927
.SERRO	18	
.SERRT	18	
.SPOWE	18	1633
.SRDOC	18	1307
.SREAD	18	1204
.SSCOP	18	994
.STRAP	18	1492
.STYPE	18	1066
.STYPO	18	

. ABS. 037234 000

ERRORS DETECTED: 0
 DEFAULT GLOBALS GENERATED: 0

DZKCC,DZKCC/SOL/CRF+DZKCC.MAC,DZKCC.P11
 RUN-TIME: 34 32 2 SECONDS
 RUN-TIME RATIO: 116/69=1.6
 CORE USED: 49K (98 PAGES)