

DV11

FREE RUNNING ROM 1
MD-11-DZDVC-C

EP-DZDVC-C-DL-A

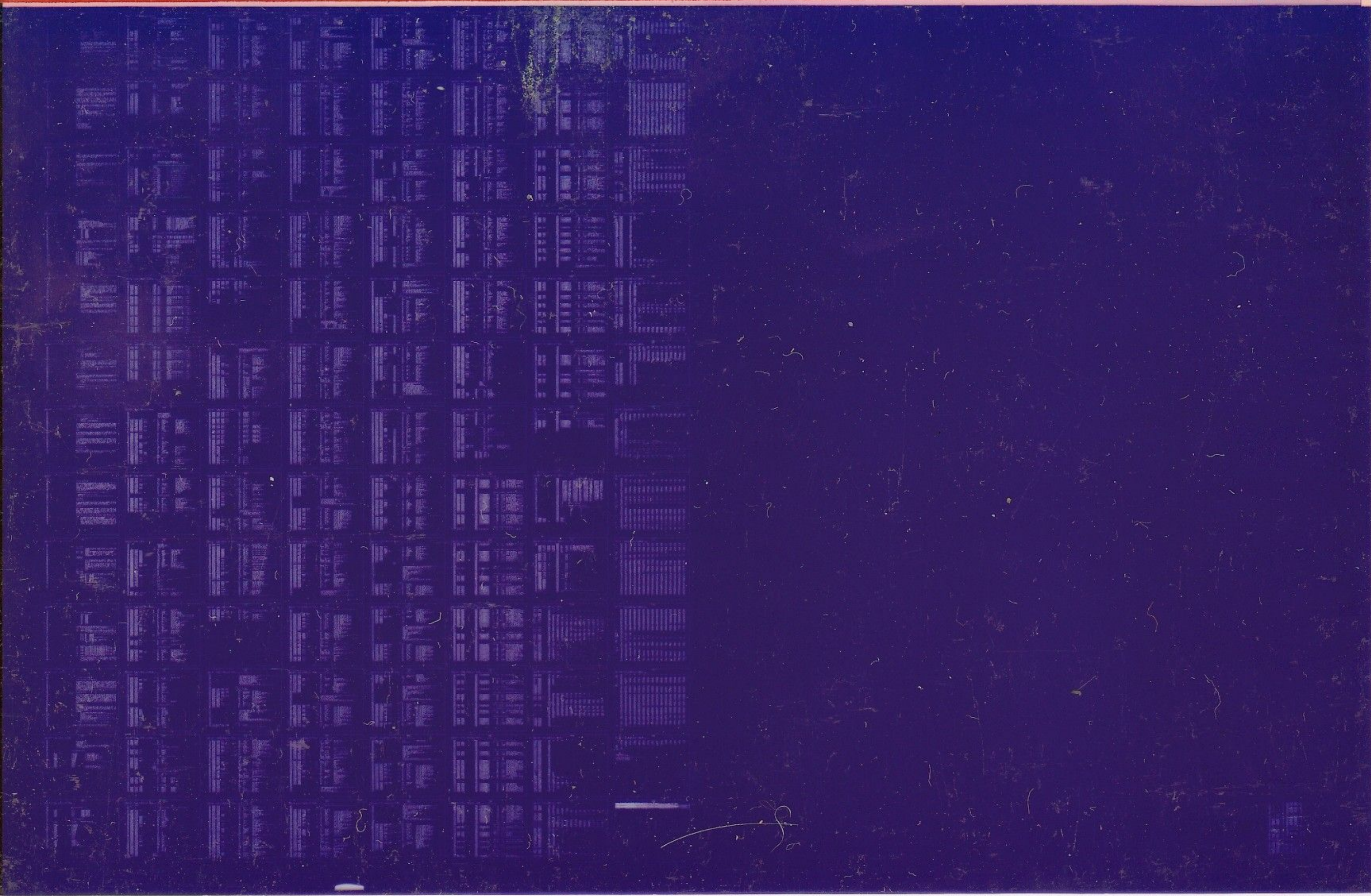
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IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DZDVC-C-C
PRODUCT NAME: "FREE RUNNING" ROM TEST PART 1
DATE RELEASED: 21-APRIL-1976
MAINTAINER: DIAGNOSTICS
AUTHOR: JOHN EGOLF

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2.2 STORAGE

PROGRAM WILL USE ALL 8K OF MEMORY EXCEPT WHERE ABL AND BOOTSTRAP LOADER RESIDE. LOCATION 1500 THRU 1736 ARE ESPECIALLY TO BE NOTED AND TO BE UNTOUCHED BY OPERATOR AFTER DV11 TRIAL PROGRAM HAS BEEN EXECUTED: AFTER THE 'AUTO SIZING' HAS BEEN DONE.

3. LOADING PROCEEDURE

3.1 METHOD

ALL PROGRAMS ARE IN ABSOLUTE FORMAT AND ARE LOADED USING THE ABSOLUTE LOADER. NOTE: IF THE DIAGNOSTICS ARE ON A MEDIA SUCH AS DISK, MAGTAPE, DECTAPE, OR CASSETTE; FOLLOW INSTRUCTIONS FOR THE MONITOR WHICH HAS BEEN PROVIDED ON THAT SPECIFIC MEDIA.

ABSOLUTE LOADER STARTING ADDRESS *500

MEMORY * SIZE

4K	17
8K	37
12K	57
16K	77
20K	117
24K	137
28K	157

3.1.1 PLACE ADDRESS OF ABS LOADER INTO SWITCH REGISTER. (ALSO PLACE 'HALT' SW UP)

3.1.2 DEPRESS 'LOAD ADDRESS' KEY ON CONSOLE AND RELEASE.

3.1.3 DEPRESS 'START KEY' ON CONSOLE AND RELEASE (PROGRAM SHOULD NOW BE LOADING INTO CPU)

Vertical text on the left margin, possibly a page number or document identifier, appearing as a series of small characters.

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8.4A MORE ON THAT 'STATUS TABLE' (1500-1736)

'MAP OF DV11 STATUS'

1500	175000
1502	000300
1504	000226
1506	000062
1510	000226
1512	000062
1514	004000
1516	000000
1520	004000
1522	000000

THE ABOVE INFORMATION WILL BE REPEATED FOR EACH OF UP TO 8 DV11'S IN THE SYSTEM (THESE WILL FOLLOW UNDER THIS TABLE). EXPLANATION:

1500	175000	THIS IS THE SYSTEM CONTROL REGISTER FOR THE 1ST DV11 IN THE SYSTEM.
1502	000300	THIS IS VECTOR 'A' FOR THE FIRST DV11 IN THE SYSTEM.
1504	000226	THIS REPRESENTS 'SYNC A' AND THE SOFTWARE STATUS FOR THE 1ST LINE CARD IN THE 1ST DV11. THE BITS ARE AS FOLLOWS:

BIT 15	SET:	LINE CARD *NOT INSTALLED (AND WONT BE TESTED)
BIT 14	SET:	RESERVED
BIT 13	SET:	RESERVED
BIT 12	SET:	ONE SYNC, =0; TWO SYNCs.
BIT 11	SET:	ASYNC LINE CARD, =0 SYNC LINE CARD.
BIT 10	SET:	RESERVED
BIT 09	SET:	BITS PER CHAR. (USED WITH BIT8)
BIT 08	SET:	BITS PER CHAR. (USED WITH BIT9)

BIT09	BIT08	BITS PER CHAR.
0	0	8
0	1	7
1	0	6
1	1	5

BIT 07-00		SYNC 'A' FOR SPECIFIED LINE CARD.
1506	000062	THIS REPRESENTS 'SYNC B' FOR THE 1ST LINE CARD.
1510	000226	THIS IS 'SYNC A' AND LINE STATUS FOR THE 2ND LINE CARD. (FOR BITS DEFINATION SEE EXPLANATION FOR LINE CARD 1).
1512	000062	THIS IS 'SYNC B' FOR THE SECOND LINE CARD.
1514	000226	THIS IS 'SYNC A' AND LINE STATUS FOR THE 3RD LINE CARD. (FOR BITS DEFINATION SEE EXPLANATION FOR LINE CARD 1).
1516	000062	THIS IS 'SYNC B' FOR LINE CARD NO. 3.
1520	000226	THIS IS 'SYNC A' AND LINE STATUS FOR THE 4TH LINE CARD. (FOR BITS DEFINATION SEE EXPLANATION FOR LINE CARD 1).
1522	000062	THIS IS SYNC B FOR THE 4TH LINE CARD.

THE ABOVE IS REPEATED FOR EACH DV11 IN THE SYSTEM. THE TABLE IS FILLED BY AUTO SIZING OR BY THE MANUAL PARAMETER INPUT PROGRAM AS DESCRIBED PREVIOUSLY. ALSO IF DESIRED BY USER, THE LOCATIONS MAY BE ALTERED BY HAND (TOGGLED IN) TO SUIT THE SPECIFIC CONFIGURATION.

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8.5 *** METHOD OF AUTO SIZING ***

8.5.1 FINDING THE CONTROL STATUS REGISTER.

THE PROGRAM WILL START AT ADDRESS 175000 AND START 'REFERENCEING' ADDRESS. IF A NON-EX MEMORY TRAP OCCURES; THE POINTER (HOLDING 175000) IS UPDATED BY 10 AND THE ABOVE IS REPEATED UNTILL ADDRESS 175400 IS REACHED. IF A 'SLAVE SYNC RESPONSE' WAS ISSUED BY THE DV11 (OR ANY OTHER DEVICE) (NO NXM TRAP)(AND IT (SEL0) WAS=0) ; POINTER PLUS 12 (SEL12) IS TESTED TO CONTAIN 177777 (MUST BE EXACTLY 177777); IF A TRAP IS ENCOUNTERED OR IF SEL12 DOES NOT CONTAIN 177777 THE ABOVE UPDATING IS PERFORMED. IF SEL12 WAS EQUAL TO 177777 THE POINTER IS STORED AWAY AND THE ROUTINE CONTINUES AS ABOVE:
 NOTE: IF THE PROGRAM DOES NOT FIND YOUR DV11; SOMETHING IS WRONG AND AUTO SIZING SHOULD NOT BE DONE.

8.5.2 FINDING THE VECTOR

THE VECTOR AREA (ADDRESS 300-776) IS FILLED WITH THE INSTRUCTION IOT AND '+2' (NEXT ADDRESS). BIT7 AND BIT6 (RX INTERRUPT AND RX INTERRUPT IE) ARE SET INTO DVSCR REGISTER; A DELAY IS MADE AND IF NO INTERRUPT OCCURES (BECAUSE OF A BAD DV11) THE PROGRAM ASSUMES VECTOR ADDRESS 300 AND THE PROBLEM SHOULD BE FIXED IN THE DIAGNOSTIC. ONCE THE PROBLEM IS FIXED; THE PROGRAM SHOULD BE RE-SETUP AGAIN TO GET CORRECT VECTOR. IF AN INTERRUPT OCCURED; THE ADDRESS TO WHICH THE DV11 INTERRUPTED TO IS PICKED UP AND REPORTED AS THE VECTOR. NOTE: IF THE VECTOR REPORTED IS NOT THE VECTOR SET UP BY YOU; THERE IS A PROBLEM AND AUTO SIZING SHOULD NOT BE DONE.

8.5.3 PARAMETER ASSUMPTIONS.

SINCE TOO MUCH HARDWARE WOULD NEED TO BE TURNED ON TO SIZE THE REST OF THE PARAMETERS; THE PROGRAM MUST ASSUME THE REMAINING VARIATIONS. THE RESULT IF NOT TO YOUR SPECIFIC CONFIGURATION MAY BE ALTERED BY HANG (TOGGLE IN) IS DESIRED. IN THIS WAY 95% OF THE PARAMETER SETUP WAS DONE BY THE PROGRAM AND 5% BY YOU.
 THEREFORE:

- 1) ALL LINE CARDS(4) ARE ASSUMED TO BE INSTALLED.
 SET BIT15 OF STATUS MAP OF ANY (APPROIATE) LINE CARDS MISSING
- 2) TWO SYNC.
 SET BIT12 IF YOU HAVE A 4 LINE GROUP SET FOR 1 SYNC.
- 3) EIGHT BITS PER CHAR.
 ADJUST BITS 9 AND BIT 8 IN STATUS MAP FOR YOUR CORRECT CONFIG.
- 4) SYNCHRONOUS LINE CARDS INSTALLED
 SET BIT11 OF STATUS MAP FOR ASYNC LINE CARD AND ZERO SYNC CHARS.
- 5) SYNC "A"=226 AND SYNC "B"=062

IN ALL ADJUSTMENTS PLEASE REFER TO SECTION 8.4A FOR GREATER DEATAIL.
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:*MAINDEC-11-DZDVC-C/<377>/ROM DATA CHECK AND "FREE RUNNING" TESTS
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DZDVC-C MACY11 27(732) 17-SEP-76 11:40 PAGE 14
DZDVCC.P11 INTRODUCTION TO DV11 DIAGNOSTIC

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; STARTING PROCEDURE  
; LOAD PROGRAM  
; LOAD ADDRESS 000200  
; PRESS START  
; PROGRAM WILL TYPE "MAINDEC-11-DZDVC-C/377" ROM DATA CHECK AND "FREE RL"  
; PROGRAM WILL TYPE "R" TO INDICATE THAT TESTING HAS STARTED  
; AT THE END OF A PASS, PROGRAM WILL TYPE PASS COMPLETE MESSAGE  
; AND THEN RESUME TESTING
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; SWITCH REGISTER OPTIONS

100000
040000
020000
010000
004000
002000
001000
000400
000200
000100
000040
000020
000010
000004
000002
000001

SW15=100000
SW14=40000
SW13=20000
SW12=10000
SW11=4000
SW10=2000
SW09=1000
SW08=400
SW07=200
SW06=100
SW05=40
SW04=20
SW03=10
SW02=4
SW01=2
SW00=1

```
=1, HALT ON ERROR  
=1, LOOP ON CURRENT TEST  
=1, INHIBIT ERROR TYPEOUT  
=1, DELETE TYPEOUT/BELL ON ERROR.  
=1, INHIBIT ITERATIONS  
=1, ESCAPE TO NEXT TEST ON ERROR  
=1, LOOP WITH CURRENT DATA  
=1, LOOP ON ERROR  
=1, DO "AUTO SIZING" ON INITIAL START UP.  
  
; LOCK ON TEST SELECT  
; RESTART PROGRAM AT SELECTED TEST  
; RESELECT DV11 DESIRED ACTIVE  
; NOTE: THIS MUST NOT EXCEED ORIGINAL COUNT
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;REGISTER DEFINITIONS

 ;

000000	R0=%0	;GENERAL REGISTER
000001	R1=%1	;GENERAL REGISTER
000002	R2=%2	;GENERAL REGISTER
000003	R3=%3	;GENERAL REGISTER
000004	R4=%4	;GENERAL REGISTER
000005	R5=%5	;GENERAL REGISTER
000006	SP=%6	;PROCESSOR STACK POINTER
000007	PC=%7	;PROGRAM COUNTER

;LOCATION EQUIVALENCIES

 ;

177776	FS=177776	;PROCESSOR STATUS WORD
001200	STACK=1200	;START OF PROCESSOR STACK
100000	BIT15=100000	
040000	BIT14=40000	
020000	BIT13=20000	
010000	BIT12=10000	
004000	BIT11=4000	
002000	BIT10=2000	
001000	BIT9=1000	
000400	BIT8=400	
000200	BIT7=200	
000100	BIT6=100	
000040	BIT5=40	
000020	BIT4=20	
000010	BIT3=10	
000004	BIT2=4	
000002	BIT1=2	
000001	BIT0=1	
010000	ALU=BIT12	
020000	RAM=BIT13	
030000	XFR=BIT13+BIT12	
040000	NPR=BIT14	
050000	S.C=BIT14+BIT12	
060000	BCC=BIT14+BIT13	
070000	BRB=BIT14+BIT13+BIT12	

 ;

:DVII VECTOR AND REGISTER INDIRECT POINTERS

00135	000000	DVRVEC:	0	: POINTER TO DVII RECEIVER INTERRUPT VECTOR
00136	000000	DVRLVL:	0	: POINTER TO DVII RECEIVER INTERRUPT SERVICE PS
00137	000000	DVTVEC:	0	: POINTER TO DVII TRANSMITTER INTERRUPT VECTOR
00138	000000	DVTLVL:	0	: POINTER TO DVII TRANSMITTER INTERRUPT SERVICE PS
00139	000000	DVSCR:	0	: POINTER TO DVII SYSTEM CONTROL REGISTER
00140	000000	DVSCRH:	0	: POINTER TO DVII SYSTEM CONTROL REGISTER HIGH BYTE.
00141	000000	DVRIC:	0	: POINTER TO DVII NEXT RECEIVED CHARACTER REGISTER
00142	000000	DVLCR:	0	: POINTER TO DVII LINE PARAMETER REGISTER
00143	000000	DVSRAS:	0	: POINTER TO DVII SECONDARY REGISTER SELECT REGISTER
00144	000000	DVSRSH:	0	: POINTER TO DVII SECONDARY REGISTER SELECT HIGH BYTE.
00145	000000	DVSRAR:	0	: POINTER TO DVII SECONDARY REGISTER ACCESS REGISTER
00146	000000	DVSFR:	0	: POINTER TO DVII SPECIAL FUNCTIONS REGISTER
00147	000000	DVNSR:	0	: POINTER TO DVII NPR STATUS REGISTER
00148	000000	RESV16:	0	: POINTER TO RESERVED REGISTER.

:DVII CONTROL INDICATORS FOR CURRENT DVII UNDER TEST

001406	000	MASK.A:	.BYTE 000	: LAST CHAR TO TEST AND PARITY MASK FOR LINES 00-03
001407	000	MASK.B:	.BYTE 000	: LAST CHAR TO TEST AND PARITY MASK FOR LINES 04-07
001410	000	MASK.C:	.BYTE 000	: LAST CHAR TO TEST AND PARITY MASK FOR LINES 08-11
001411	000	MASK.D:	.BYTE 000	: LAST CHAR TO TEST AND PARITY MASK FOR LINES 12-15
001412	010	CLK.A:	.BYTE 8.	: NUMBER OF CLOCKS NEEDED FOR ONE CHAR FOR LINES 00-03
001413	010	CLK.B:	.BYTE 8.	: NUMBER OF CLOCKS NEEDED FOR ONE CHAR FOR LINES 04-07
001414	010	CLK.C:	.BYTE 8.	: NUMBER OF CLOCKS NEEDED FOR ONE CHAR FOR LINES 08-11
001415	010	CLK.D:	.BYTE 8.	: NUMBER OF CLOCKS NEEDED FOR ONE CHAR FOR LINES 12-15
001416	000000	L00.03:	000000	: PARAMETERS FOR LINES 00-03
001420	000000	L04.07:	000000	: PARAMETERS FOR LINES 04-07
001422	000000	L08.11:	000000	: PARAMETERS FOR LINES 08-11
001424	000000	L12.15:	000000	: PARAMETERS FOR LINES 12-15
001426	000000	SYNC2A:	000000	: SYNC 2
001430	000000	SYNC2B:	000000	:
001432	000000	SYNC2C:	000000	:
001434	000000	SYNC2D:	000000	:

:SUMMARY

:	MASK.X	040	5	BITS	PER	CHAR.
:		100	6	BITS	PER	CHAR.
:		200	7	BITS	PER	CHAR.
:		000	8	BITS	PER	CHAR.
:	CLK.X	005	5	BITS	PER	CHAR.
:		006	6	BITS	PER	CHAR.
:		007	7	BITS	PER	CHAR.
:		010	8	BITS	PER	CHAR.

:DV11 STATUS TABLE AND ADDRESS ASSIGNMENTS

000					
001					
002					
003					
004		001500	. =1500		
005	001500	000001	DV.MAP:		
006	001502	000001	DVCRO0: .BLKW 1	: CONTROL STATUS REGISTER FOR DV11 NUMBER 00	
007	001504	000001	DVTR00: .BLKW 1	: VECTOR "A" FOR DV11 NUMBER 00	
008	001506	000001	DV00.A: .BLKW 1	: PARAMETER FOR LINES 00-03 FOR DV11 NUMBER 00	
009	001510	000001	SYNA00: .BLKW 1	: SYNC TWO	
010	001512	000001	DV00.B: .BLKW 1	: PARAMETER FOR LINES 04-07 FOR DV11 NUMBER 00	
011	001514	000001	SYNB00: .BLKW 1	: SYNC TWO	
012	001516	000001	DV00.C: .BLKW 1	: PARAMETER FOR LINES 08-11 FOR DV11 NUMBER 00	
013	001520	000001	SYNC00: .BLKW 1	: SYNC TWO	
014	001522	000001	DV00.D: .BLKW 1	: PARAMETER FOR LINES 12-15 FOR DV11 NUMBER 00	
015			SYND00: .BLKW 1	: SYNC TWO	
016	001524	000001	DVCRO1: .BLKW 1	: CONTROL STATUS REGISTER FOR DV11 NUMBER 01	
017	001526	000001	DVTR01: .BLKW 1	: VECTOR "A" FOR DV11 NUMBER 01	
018	001530	000001	DV01.A: .BLKW 1	: PARAMETER FOR LINES 00-03 FOR DV11 NUMBER 01	
019	001532	000001	SYNA01: .BLKW 1	: SYNC TWO	
020	001534	000001	DV01.B: .BLKW 1	: PARAMETER FOR LINES 04-07 FOR DV11 NUMBER 01	
021	001536	000001	SYNB01: .BLKW 1	: SYNC TWO	
022	001540	000001	DV01.C: .BLKW 1	: PARAMETER FOR LINES 08-11 FOR DV11 NUMBER 01	
023	001542	000001	SYNC01: .BLKW 1	: SYNC TWO	
024	001544	000001	DV01.D: .BLKW 1	: PARAMETER FOR LINES 12-15 FOR DV11 NUMBER 01	
025	001546	000001	SYND01: .BLKW 1	: SYNC TWO	
026					
027	001550	000001	DVCRO2: .BLKW 1	: CONTROL STATUS REGISTER FOR DV11 NUMBER 02	
028	001552	000001	DVTR02: .BLKW 1	: VECTOR "A" FOR DV11 NUMBER 02	
029	001554	000001	DV02.A: .BLKW 1	: PARAMETER FOR LINES 00-03 FOR DV11 NUMBER 02	
030	001556	000001	SYNA02: .BLKW 1	: SYNC TWO	
031	001560	000001	DV02.B: .BLKW 1	: PARAMETER FOR LINES 04-07 FOR DV11 NUMBER 02	
032	001562	000001	SYNB02: .BLKW 1	: SYNC TWO	
033	001564	000001	DV02.C: .BLKW 1	: PARAMETER FOR LINES 08-11 FOR DV11 NUMBER 02	
034	001566	000001	SYNC02: .BLKW 1	: SYNC TWO	
035	001570	000001	DV02.D: .BLKW 1	: PARAMETER FOR LINES 12-15 FOR DV11 NUMBER 02	
036	001572	000001	SYND02: .BLKW 1	: SYNC TWO	
037					
038	001574	000001	DVCRO3: .BLKW 1	: CONTROL STATUS REGISTER FOR DV11 NUMBER 03	
039	001576	000001	DVTR03: .BLKW 1	: VECTOR "A" FOR DV11 NUMBER 03	
040	001600	000001	DV03.A: .BLKW 1	: PARAMETER FOR LINES 00-03 FOR DV11 NUMBER 03	
041	001602	000001	SYNA03: .BLKW 1	: SYNC TWO	
042	001604	000001	DV03.B: .BLKW 1	: PARAMETER FOR LINES 04-07 FOR DV11 NUMBER 03	
043	001606	000001	SYNB03: .BLKW 1	: SYNC TWO	
044	001610	000001	DV03.C: .BLKW 1	: PARAMETER FOR LINES 08-11 FOR DV11 NUMBER 03	
045	001612	000001	SYNC03: .BLKW 1	: SYNC TWO	
046	001614	000001	DV03.D: .BLKW 1	: PARAMETER FOR LINES 12-15 FOR DV11 NUMBER 03	
047	001616	000001	SYND03: .BLKW 1	: SYNC TWO	
048					
049	001620	000001	DVCRO4: .BLKW 1	: CONTROL STATUS REGISTER FOR DV11 NUMBER 04	
050	001622	000001	DVTR04: .BLKW 1	: VECTOR "A" FOR DV11 NUMBER 04	
051	001624	000001	DV04.A: .BLKW 1	: PARAMETER FOR LINES 00-03 FOR DV11 NUMBER 04	
052	001626	000001	SYNA04: .BLKW 1	: SYNC TWO	
053	001630	000001	DV04.B: .BLKW 1	: PARAMETER FOR LINES 04-07 FOR DV11 NUMBER 04	
054	001632	000001	SYNB04: .BLKW 1	: SYNC TWO	
055	001634	000001	DV04.C: .BLKW 1	: PARAMETER FOR LINES 08-11 FOR DV11 NUMBER 04	

001636	000001	SYN004: .BLKW 1	:SYNC TWO
001640	000001	DV04.D: .BLKW 1	:PARAMETER FOR LINES 12-15 FOR DV11 NUMBER 04
001642	000001	SYN004: .BLKW 1	:SYNC TWO
001644	000001	DVCR05: .BLKW 1	:CONTROL STATUS REGISTER FOR DV11 NUMBER 05
001646	000001	DVTR05: .BLKW 1	:VECTOR "A" FOR DV11 NUMBER 05
001650	000001	DV05.A: .BLKW 1	:PARAMETER FOR LINES 00-03 FOR DV11 NUMBER 05
001652	000001	SYNA05: .BLKW 1	:SYNC TWO
001654	000001	DV05.B: .BLKW 1	:PARAMETER FOR LINES 04-07 FOR DV11 NUMBER 05
001656	000001	SYNB05: .BLKW 1	:SYNC TWO
001660	000001	DV05.C: .BLKW 1	:PARAMETER FOR LINES 08-11 FOR DV11 NUMBER 05
001662	000001	SYN005: .BLKW 1	:SYNC TWO
001664	000001	DV05.D: .BLKW 1	:PARAMETER FOR LINES 12-15 FOR DV11 NUMBER 05
001666	000001	SYND05: .BLKW 1	:SYNC TWO
001670	000001	DVCR06: .BLKW 1	:CONTROL STATUS REGISTER FOR DV11 NUMBER 06
001672	000001	DVTR06: .BLKW 1	:VECTOR "A" FOR DV11 NUMBER 06
001674	000001	DV06.A: .BLKW 1	:PARAMETER FOR LINES 00-03 FOR DV11 NUMBER 06
001676	000001	SYNA06: .BLKW 1	:SYNC TWO
001700	000001	DV06.B: .BLKW 1	:PARAMETER FOR LINES 04-07 FOR DV11 NUMBER 06
001702	000001	SYNB06: .BLKW 1	:SYNC TWO
001704	000001	DV06.C: .BLKW 1	:PARAMETER FOR LINES 08-11 FOR DV11 NUMBER 06
001706	000001	SYN006: .BLKW 1	:SYNC TWO
001710	000001	DV06.D: .BLKW 1	:PARAMETER FOR LINES 12-15 FOR DV11 NUMBER 06
001712	000001	SYND06: .BLKW 1	:SYNC TWO
001714	000001	DVCR07: .BLKW 1	:CONTROL STATUS REGISTER FOR DV11 NUMBER 07
001716	000001	DVTR07: .BLKW 1	:VECTOR "A" FOR DV11 NUMBER 07
001720	000001	DV07.A: .BLKW 1	:PARAMETER FOR LINES 00-03 FOR DV11 NUMBER 07
001722	000001	SYNA07: .BLKW 1	:SYNC TWO
001724	000001	DV07.B: .BLKW 1	:PARAMETER FOR LINES 04-07 FOR DV11 NUMBER 07
001726	000001	SYNB07: .BLKW 1	:SYNC TWO
001730	000001	DV07.C: .BLKW 1	:PARAMETER FOR LINES 08-11 FOR DV11 NUMBER 07
001732	000001	SYN007: .BLKW 1	:SYNC TWO
001734	000001	DV07.D: .BLKW 1	:PARAMETER FOR LINES 12-15 FOR DV11 NUMBER 07
001736	000001	SYND07: .BLKW 1	:SYNC TWO
001740	000000	DZ.END: 000000	

950	002244	000000				HALT			:WAIT FOR USER TO TELL WHAT DEVICES TO R
951	002246	127737	176730	001302		CMPS	QSWR, SAVACT		:IS THE NUMBER VALID?
952	002254	101404				BLOS	2\$:BR IF NUMBER IS 0V.
953	002256	104402	005243			TYPE	.MERR3		:TELL USER OF INVALID NUMBER.
954	002262	000000				HALT			:STOP EVERY THING.
955	002264	009776				BR	.-2		:RESTART THE PROGRAM AGAIN.
956	002266	117737	176710	001300	2\$:	MOVB	QSWR, DVACTV		:GET NEW DEVICE PATTERN
957	002274	113700	001300			MOVB	DVACTV, RO		:SHOW THE USER WHAT HE SELECTED.
958	002300	042700	177400			BIC	#1C<377>, RO		:USE ONLY LOW BYTE.
959	002304	000000				HALT			:CONTINUE DYNAMIC SWITCHES.
960	002306	012700	000300		3\$:	MOV	#300, RO		:PREPARE TO CLEAR THE FLOATING
961	002312	012701	000302			MOV	#302, R1		:VECTOR AREA. 300-776
962	002316	010120			4\$:	MOV	R1, (RO)+		:START PUTTING "PC+2 - HALT"
963	002320	005021				CLR	(R1)+		:IN VECTOR AREA.
964	002322	022021				CMF	(RO)+, (R1)+		:POP POINTERS
965	002324	022700	001000			CMF	#1000, RO		:ALL DONE?"
966	002330	001372				BNE	4\$:BR IF NO.
967									
968									
969									
970									
971									
972	002332	012737	000340	177776		.BEGIN:	MOV	#340, PS	:LOCK OUT INTERRUPTS
973	002340	012706	001200			MOV	#STACK, SP		:SET UP STACK
974	002344	005737	000042			TST	Q#42		:IS PROGRAM UNDER MONITOR CONTROL
975	002350	001023				BNE	3\$:BR IF YES
976	002352	032777	000004	176622		BIT	#BIT2, QSWR		:CHECK FOR LOCK ON TEST
977	002350	001411				BEQ	1\$:BR IF NO LOCK DESIRED.
978	002362	104402	005301			TYPE	.MLOCK		:TYPE LOCK SELECTED.
979	002366	012737	000240	002702		MOV	#NOP, TTST		:ADJUST SCOPE ROUTINE.
980	002374	012737	000240	002704		MOV	#NOP, TTST+2		:SET UP TO LOCK
981	002402	000406				BR	2\$:CONTINUE ALONG.
982	002404	013737	003014	002702	1\$:	MOV	BRW, TTST		:PREPARE NORMAL SCOPE ROUTINE
983	002412	013737	003016	002704		MOV	BRX, TTST+2		:LOCK NOT SELECTED, SET UP FOR NORMAL SC
984	002420	012737	005666	001214	2\$:				
985	002426	104402	005171		3\$:	MOV	#CYCLE, RETURN		:START AT "CYCLE" FIND WHICH DEVICE TO T
986	002432	000177	176556		4\$:	TYPE	MR		:TYPE R
						JMP	QRETURN		:START TESTING

:TEST START AND RESTART

```

987 :END OF PASS
988 :TYPE NAME OF TEST
989 :UPDATE PASS COUNT
990 :CHECK FOR EXIT TO ACT-11
991 :RESTART TEST
992
993 002436 000005 .EOP: RESET :MAKE THE WORLD CLEAN AGAIN.
994 002440 005037 001234 CLR LSTERR :CLEAR LAST ERROR PC
995 002444 105037 001311 CLR B ERRFLG :CLEAR ERROR FLAG
996 002450 005237 001230 INC PASCNT :UPDATE PASS COUNT
997 002454 013777 001230 176516 MOV PASCNT, @LIGHTS :DISPLAY PASS COUNT
998 002462 104402 005145 TYPE ,MEPASS :TYPE END PASS
999 002466 104402 005330 TYPE ,MCSR X :TYPE CSR
1000 002472 104411 002604 CNVRT ,XCSR :SHOW IT
1001 002476 104402 005336 TYPE ,MVECX :TYPE VECTOR
1002 002502 104411 002612 CNVRT ,XVEC :SHOW IT
1003 002506 104402 005344 TYPE ,MPASSX :TYPE PASSES
1004 002512 104411 002620 CNVRT ,XPASS :SHOW IT
1005 002516 104402 005355 TYPE ,MERRX :TYPE ERRORS
1006 002522 104411 002626 CNVRT ,XERR :SHOW IT
1007 002526 105337 001303 DECB SAVNUM :ARE ALL DEVICES TESTED?
1008 002532 001017 BNE RESTR :BR IF NO.
1009 002534 112737 000377 001313 MOVB #377, QV.FLG :SET THE QUICK VERIFY FLAG.
1010 002542 113737 001301 001303 MOVB DVNUM, SAVNUM :RESTORE THE COUNT
1011 002550 013701 000042 MOV @#42, R1 :CHECK FOR ACT-11 OR DDP
1012 002554 001406 BEQ RESTR :IF NOT, CONTINUE TESTING
1013 002556 000005 RESET :STOP THE SHOW--CLEAR THE WORLD
1014 002560
1015 002560 004711 LOGICAL: JSR PC, (R1)
1016 002562 000240 NOP
1017 002564 000240 NOP
1018 002566 000240 NOP
1019 002570 000240 NOP
1020 002572 012737 005666 001214 RESTR: MOV #CYCLE, RETURN
1021 002500 000137 005666 JMP CYCLE
1022 002604 000001 XCSR: 1
1023 002606 006 002 .BYTE 6.2
1024 002610 001362 DVSCR
1025 002612 000001 XVEC: 1
1026 002614 003 002 .BYTE 3.2
1027 002616 001352 DVRVEC
1028 002620 000001 XPASS: 1
1029 002622 006 002 .BYTE 6.2
1030 002624 001230 PASCNT
1031 002626 000001 XERR: 1
1032 002630 006 002 .BYTE 6.2
1033 002632 001232 ERRCNT
1034
1035 ;SCOPE LOOP AND INTERATION HANDLER
1036 -----
1037
1038 002634 .SCOPE:
1039 002634 022737 177570 001202 CMP #177570, SWR ;IS THERE A REAL SWR?
1040 002642 001411 BEQ 64$ ;BR IF YES
1041 002644 017746 176336 MOV @TKDBR, -(SP) ;SAVE KEYBOARD CHAR
1042 002650 042716 000200 BIC #BIT7, (SP) ;CLEAR PARITY BIT

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K02

DZDVC-C MACY11 27(732) 17-SEP-76 11:40 PAGE 25
 DZDVCC.P11 GENERAL UTILITIES (TYPE OUT, ERROR, SCOPE, ETC.)

```

1043 002654 122726 000007      CMPB   #7,(SP)+      ;WAS IT CNTRL 'G' ?
1044 002660 001002          SNE     .+6         ;BR IF NO.
1045 002662 004737 00464C      JSR    PC,SERV.G    ;SERVICE "CNTRL 'G'".
1046 002666 005037 001234      CLR    LSTERR      ;CLEAR LAST ERROR PC.
1047 002672 010016          MOV    PD,(SP)     ;SAVE PD ON THE STACK
1049 002674 032777 040000 176300  BIT    #BIT14,DSWR  ;"LOOP ON THIS TEST."
1049 002702 001407      TTST:  BEQ    1$      ;BR IF NO. (IF LOCK SW01=1: THIS LOC =240)
1050 002704 000437          BR     3$         ;GOTO 3$ (IF LOCK SW01=1: THIS LOC =240)
1051 002706 105777 176272      TSTB  @TKCSR      ;KEYBOARD DONE?
1052 002712 100034          BPL    3$         ;BR IF NO. (LOCK: HIT KEY TO GOTO NEXT TEST)
1053 002714 017700 176266      MOV    @TKDBR,RO  ;CLEAR DONE BIT
1054 002720 000415          BR     2$         ;CONTINUE
1055 002722 032777 004000 176252  1$:   BIT    #SW11,DSWR ;DELETE ITERATION? (QUICK PASS)
1056 002730 001011          BNE    2$         ;BR IF YES
1057 002732 105737 001313      TSTB  QV.FLG      ;HAVE PASSES BEECOMPLETED?
1058 002736 001406          BEQ    2$         ;BR IF QUICK PASS.
1059 002740 005237 001224      INC    LPCNT      ;UPDATE ITERATION COUNTER
1060 002744 023737 001224 001222  CMP    LPCNT,ICOUNT ;ARE ALL ITERATIONS DONE??
1061 002752 001014          BNE    3$         ;BR IF NOT YET
1062 002754 105037 001311      CLRB  ERRFLG      ;PREPARE FOR NEW TEST
1063 002760 005037 001224      CLR    LPCNT      ;START ICOUNTER AT 0
1064 002764 005037 001220      CLR    LOCK
1065 002770 012737 000024 001222  MOV    #20,ICOUNT  ;RESET ITERATIONS
1066 002776 013737 001216 001214  MOV    NEXT,RETURN ;GET NEXT TEST
1067 003004 011600      3$:   MOV    (SP),RO    ;POP PD OFF OF THE STACK
1068 003006 022626          PCP2SP ;FAKE AN "RTI"
1069 003010 000177 176200      JMP    @RETURN    ;GO DO THE TEST
1070 003014 001407      BRW:  1407
1071 003016 000437      BRX:  437

;CHECK FOR FREEZE ON CURRENT DATA
;-----
1076 003020 032777 001000 176154  .SCOPE: BIT    #SW09,DSWR  ;IS SW09=1(SET)?
1077 003026 001405          BEQ    1$         ;BR IF NOT SET.
1078 003030 005737 001220      TST   LOCK
1079 003034 001402          BEQ    1$
1080 003036 013716 001220      1$:   MOV    LOCK,(SP)  ;GOTO THE ADDRESS IN LOCK.
1081 003042 000002          RTI    ;GO BACK.

;TELETYPE OUTPUT ROUTINE
;-----
1086 003044 010546      .TYPE: MOV    R5, -(SP) ;SAVE R5 ON THE STACK.
1087 003046 017605 000002      MOV    @2(SP),R5  ;GET ADDRESS OF MESSAGE.
1088 003052 062766 000002 000002  ADD    #2,2(SP)   ;POP OVER ADDRESS.
1089 003060 032777 010000 176114  1$:   BIT    #SW12,DSWR ;INHIBIT ALL PRINT OUT??
1090 003066 001012          BNE    3$         ;BR IF NO PRINT OUT WANTED (SW12=1)
1091 003070 105715          TSTB  (R5)       ;IS NUMBER MINUS? (MSB=1(BIT7))
1092 003072 100002          BPL    2$         ;BR IF NUMBER IS PLUS
1093 003074 104402 005104      TYPE  ,MCRLF     ;TYPE A CR/LF!
1094 003100 105777 176104      2$:   TSTB  @TPCSR    ;TTY READY?
1095 003104 100375          BPL    2$         ;BR IF NO.
1096 003106 112577 176100      MOVB  (R5)+,@TPDBR ;PRINT CURRENT CHAR.
1097 003112 001362          BNE    1$         ;IF NOT ZERO KEEP PRINTING!
1098 003114 012605      3$:   MOV    (SP)+,R5  ;END OF OUTPUT. RESTORE R5
  
```



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1099 003116 000002          RTI          :GO HOME
1100
1101
1102 003120 010346          .INSTR: MOV      R3,-(SP)          ;SAVE R3 ON STACK
1103 003122 010446          MOV      R4,-(SP)          ;SAVE R4 ON STACK
1104 003124 017637 000004 003142  MOV      @4(SP),.MSG
1105 003132 062766 000002 000004  ADD      #2,4(SP)
1106 003140 104402          .INST1: TYPE
1107 003142 000000          .MSG: 0
1108 003144 012704 005520          MOV      #INBUF,R4
1109 003150 012703 000007          MOV      #7,R3
1110 003154 105777 176024          1$:  TSTB   @TKCSR
1111 003160 100375          BPL      1$
1112 003162 117714 176020          MOVB   @TKDBR,(R4)
1113 003166 142714 000200          BICB   #200,(R4)
1114 003172 122427 000015          CMPB   (R4),#15
1115 003176 001417          BEQ     INSTR2
1116 003200 105777 176004          2$:  TSTB   @TPCSR
1117 003204 100375          BPL      2$
1118 003206 017777 175774 175776          MOV      @TKDBR,@TPDBR
1119 003214 005303          DEC     R3
1120 003216 001356          BNE     1$
1121 003220 012604          MOV      (SP)+,R4
1122 003222 012503          MOV      (SP)+,R3
1123 003224 104402 005100          .INSTE: TYPE
1124 003230 010346          MOV      R3,-(SP)
1125 003232 010446          MOV      R4,-(SP)
1126 003234 000741          BR      .INST1
1127 003236 012604          INSTR2: MOV      (SP)+,R4          ;RESTORE R4
1128 003240 012603          MOV      (SP)+,R3          ;RESTORE R3
1129 003242 000002          RTI
1130
1131          ;CONVERT ASCII STRING TO OCTAL
1132          -----
1133
1134 003244 010546          .PARAM: MOV      R5,-(SP)
1135 003246 010446          MOV      R4,-(SP)
1136 003250 016605 000004          MOV      4(SP),R5
1137 003254 012537 003434          MOV      (R5)+,LOLIM
1138 003260 012537 003436          MOV      (R5)+,HILIM
1139 003264 012537 003440          MOV      (R5)+,DEVADR
1140 003270 112537 003442          MOVB   (R5)+,LOBITS
1141 003274 112537 003443          MOVB   (R5)+,ADRCNT
1142 003300 010566 000004          MOV      R5,4(SP)
1143 003304 005005          PARAM1: CLR     R5
1144 003306 012704 005520          MOV      #INBUF,R4
1145 003312 122714 000015          CMPB   #15,(R4)
1146 003316 001420          BEQ     PARERR
1147 003320 121427 000060          1$:  CMPB   (R4),#60
1148 003324 002415          BLT     PARERR
1149 003326 121427 000067          CMPB   (R4),#67
1150 003332 003012          BGT     PARERR
1151 003334 142714 000060          BICB   #60,(R4)
1152 003340 152405          BISB   (R4)+,R5
1153 003342 122714 000015          CMPB   #15,(R4)
1154 003346 001406          BEQ     LIMITS

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M02

DZDVC-C MACY11 27(732) 17-SEP-76 11:40 PAGE 27
 DZDVCC.P11 GENERAL UTILITIES (TYPE OUT, ERROR, SCOPE, ETC.)

1155	003350	006305		ASL	R5	
1156	003352	006305		ASL	R5	
1157	003354	006305		ASL	R5	
1158	003356	000760		BR	1\$	
1159	003360	104404		PARERR:	INSTER	
1160	003362	000750		BR	PARAM1	
1161						
1162						
1163						
1164						
1165	003364	020537	003436	LIMITS:	CMP	R5, HILIM
1166	003370	101373			BHI	PARERR
1167	003372	020537	003434		CMP	R5, LOLIM
1168	003376	103770			BLO	PARERR
1169	003400	133705	003442		BITB	LOBITS, R5
1170	003404	001365			BNE	PARERR
1171						
1172						
1173						
1174	003406	013704	003440			
1175	003412	010524		1\$:	MOV	DEVADR, R4
1176	003414	062705	000002		MOV	R5, (R4)+
1177	003420	105337	003443		ADD	#2, R5
1178	003424	001372			DECB	ADR CNT
1179	003426	012604			BNE	1\$
1180	003430	012605			MOV	(SP)+, R4
1181	003432	000002			MOV	(SP)+, R5
1182	003434	000000			RTI	
1183	003436	000000		LOLIM:	0	
1184	003440	000000		HILIM:	0	
1185	003442	000000		DEVADR:	0	
1186		003443		LOBITS:	0	
1187				ADR CNT=	LOBITS+1	
1188						
1189						
1190						
1191	003444	016637	000004 001276	.SAV05:	MOV	4(SP), SAVPC ;SAVE R7 (PC)
1192						
1193						
1194						
1195	003452	010537	001272	SV05:	MOV	R5, SAVR5 ;SAVE R5
1196	003456	010437	001270		MOV	R4, SAVR4 ;SAVE R4
1197	003462	010337	001266		MOV	R3, SAVR3 ;SAVE R3
1198	003466	010237	001264		MOV	R2, SAVR2 ;SAVE R2
1199	003472	010137	001262		MOV	R1, SAVR1 ;SAVE R1
1200	003476	010037	001260		MOV	R0, SAVR0 ;SAVE R0
1201	003502	000002			RTI	;LEAVE.
1202						
1203						
1204						
1205	003504	013700	001260	.RES05:	MOV	SAVR0, R0 ;RESTORE R0
1206	003510	013701	001262		MOV	SAVR1, R1 ;RESTORE R1
1207	003514	013702	001264		MOV	SAVR2, R2 ;RESTORE R2
1208	003520	013703	001266		MOV	SAVR3, R3 ;RESTORE R3
1209	003524	013704	001270		MOV	SAVR4, R4 ;RESTORE R4
1210	003530	013705	001272		MOV	SAVR5, R5 ;RESTORE R5

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1211 003534 000002 RTI ;LEAVE
1212
1213 ;CONVERT OCTAL NUMBER TO ASCII AND OUTPUT TO TELEPRINTER
1214 -----
1215
1216 003536 104402 005104 .CONVR: TYPE MCRLF
1217 003542 010046 .CNVRT: MOV R0,-(SP)
1218 003544 010146 MOV R1,-(SP)
1219 003546 010346 MOV R3,-(SP)
1220 003550 010446 MOV R4,-(SP)
1221 003552 010546 MOV R5,-(SP)
1222 003554 017601 000012 MOV @12(SP),R1
1223 003560 062766 000002 000012 ADD #2,12(SP)
1224 003566 012137 003742 MOV (R1)+,WRDCNT
1225 003572 112137 003744 1$: MOVB (R1)+,CHRCNT
1226 003576 112137 003745 MOVB (R1)+,SPACNT
1227 003602 013137 003746 MOV @2(R1)+,BINWRD
1228 003606 013704 003746 2$: MOV BINWRD,R4
1229 003612 113705 003744 MOVB CHRCNT,R5
1230 003616 012700 005562 MOV #TEMP,R0
1231 003622 010403 3$: MOV R4,R3
1232 003624 042703 177770 BIC #177770,R3
1233 003630 062703 000060 ADD #060,R3
1234 003634 110320 MOVB R3,(R0)+
1235 003636 000241 CLC
1236 003640 006004 ROR R4
1237 003642 000241 CLC
1238 003644 006004 ROR R4
1239 003646 000241 CLC
1240 003650 006004 ROR R4
1241 003652 005305 DEC R5
1242 003654 001362 BNE 3$
1243 003656 012703 005624 MOV #MDATA,R3
1244 003662 114023 4$: MOVB -(R0),(R3)+
1245 003664 105337 003744 DECB CHRCNT
1246 003670 001374 BNE 4$
1247 003672 105737 003745 TSTB SPACNT
1248 003676 001405 BEQ 6$
1249 003700 112723 000040 5$: MOVB #040,(R3)+
1250 003704 105337 003745 DECB SPACNT
1251 003710 001373 BNE 5$
1252 003712 105013 6$: CLRB (R3)
1253 003714 104402 005624 TYPE ,MDATA
1254 003720 075337 003742 DEC WRDCNT
1255 003724 001322 BNE 1$
1256 003726 012605 MOV (SP)+,R5
1257 003730 012604 MOV (SP)+,R4
1258 003732 012603 MOV (SP)+,R3
1259 003734 012601 MOV (SP)+,R1
1260 003736 012600 MOV (SP)+,R0
1261 003740 000002 RTI
1262 003742 000000 WRDCNT: 0
1263 003744 000000 CHRCNT: 0
1264 003745 003745 SPACNT=CHRCNT+1
1265 003746 000000 BINWRD: 0
1266

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1323	004202	001402			BEG	IS		
1324	004204	104402	005400		TYPE	.MASTEK		
1325	004210	104402	005366		TYPE	.MTSTN		
1326	004214	104411	004374		IS:	.XTSTN		:SHOW IT
1327	004220	104402	005454		CNVRT	.MERRPC		:TYPE PC.
1328	004224	104411	004366		TYPE	.ERTAB0		:SHOW IT
1329	004230	104402	005104		CNVRT	.MCRLF		:GIVE A CR/LF
1330	004234	112737	174677	001311	TYPE	.ERRFLG		:NO MORE HEADER UNLESS NO DATA TABLE.
1331	004242	005737	004252		MOV	ERRMSG		:IS THERE AN ERROR MESSAGE?
1332	004246	001402			TST	WRKO.FM		:BR IF NO.
1333	004250	104402			BEG			:TYPE
1334	004252	000000			TYPE			:ERROR MESSAGE
1335	004254				ERRMSG:	0		
1336	004254	005737	004264		WRKO.FM:			
1337	004260	001402			TST	DATAHD		:DATA HEADER?
1338	004262	104402			BEG	TYPDAT		:BR IF NO
1339	004264	000000			TYPE			:TYPE
1340	004266	005737	004276		DATAHD:	0		:DATA HEADER
1341	004272	001402			TYPDAT:	TST	DATAHP	:DATA TABLE?
1342	004274	104410			RESREG:	BEG	RESREG	:BR IF NO.
1343	004276	000000			CONVRT			:SHOW
1344	004306	104407			DATAHP:	0		:DATA TABLE
1345	004302	005777	174674		RESREG:	RESOS		:RESTORE PROC REGISTERS
1346	004306	100005			HALTS:	TST	QSWR	:HALT ON ERROR?
1347	004310	010046			BPL	EXITER		:BR IF NO HALT ON ERROR
1348	004312	016600	000002		PUSHRO			:SAVE RO
1349	004316	000000			MOV	2:SP),RO		:SHOW ERROR PC IN DATA LIGHTS
1350	004320	012600			HALT			:HALT
1351	004322	005237	001232		POPPO			:GET RO
1352	004326	032777	000400	174646	EXITER:	INC	ERRCNT	:UPDATE ERROR COUNT
1353	004334	001007			BIT	QSWO6,QSWR		:GOTO TOP OF TEST?
1354	004336	032777	002000	174636	BNE	IS		:BR IF YES
1355	004344	001407			BIT	QSW:0,QSWR		:GOTO NEXT TEST?
1356	004346	013737	001216	001214	BEG	25		:BR IF NO
1357	004354	012706	001200		MOV	NEXT,RETURN		:SET FOR NEXT TEST
1358	004360	000177	174630		IS:	MOV	QSTACK,SP	:RESET SP
1359	004364	000002			25:	JMP	QRETURN	:GOTO SPECIFIED TEST
1360	004366	000001			RTI			:RETURN
1361	004370	006	002		ERTAB0:	1		
1362	004372	001276			.BYTE	6.2		
1363	004374	000001			SAVPC			
1364	004376	003	002		XTSTN:	1		
1365	004400	001226			.BYTE	3.2		
1366					TSTNO			
1367					:ENTER HERE ON POWER FAILURE			
1368					-----			
1369								
1370	004402				.PFAIL:			
1371	004402	012737	004414	000024	MOV	QRESTART.24		:SET UP FOR POWER UP TRAP
1372	004410	000000			HALT			:HALT ON POWER DOWN NORMAL
1373	004412	000777			BR			
1374								
1375								:PROCESSOR WILL TRAP HERE WHEN POWER IS RESTORED
1376								
1377	004414				RESTAR:			
1378	004414	012737	004402	000024	MOV	Q.PFAIL.24		:SET UP FOR POWER FAILURE

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004422 012706 001200 MOV #STACK, SP ; RESET THE STACK POINTER
004424 005037 005562 CLR TEMP ; READY FOR TIMER
004426 005237 005562 INC TEMP ; PLUS ONE TO THE TIMER!
004430 001375 BNE -4 ; BR IF MORE TO GO
004432 104402 005107 TYPE ,MPFAIL ; TYPE THE MESSAGE
004434 104411 004470 CNVRT ,PFTAB ; TELL WHAT TEST TO RETURN TO.
004436 105037 001211 CLRB ERRFLG ; START CLEAN
004438 005037 001234 CLR LSTERR ;
004440 104412 MSTCLR ; START CLEAN-UP OF DEVICE
004442 104412 RAMCLR ; CLEAR IT ALL!
004444 000177 174524 JMP @RETURN ; START DOING THAT TEST AGAIN.
004446 000001 PFTAB: 1
004448 000 002 .BYTE 3,2
004450 001226 TSTNO
004452 010046 .DELAY: MOV RO, -(SP)
004454 013700 004514 MOV IS, RO
004456 005300 DEC RO
004458 001376 BNE -2
004460 012600 MOV (SP)+, RO
004462 000002 RTI
004464 000036 IS: 30.

004516 012777 004000 174536 .RAMCLR: MOV #MRESET, @DVSCR ; ISSUE A MASTER CLEAR
004518 010146 MOV R1, -(SP) ; SAVE R1 ON THE STACK
004520 010446 MOV R4, -(SP) ; SAVE R4 ON THE STACK
004522 013701 001372 MOV DVSR, R1 ; GET SECONDARY SEL. REG.
004524 013704 001376 MOV DVSR, R4 ; GET SECONDARY REGISTER ACCESS REG.
004526 005014 IS: CLR (R4) ; ZERO THE SECONDARY REGISTER.
004528 062711 170361 ADD #10<BIT11+BIT10+BIT9+BIT8+BIT3+BIT2+BIT1+BIT0>, R1
004530 001374 IS
004532 012604 MOV (SP)+, R4 ; RESTORE R4
004534 012601 MOV (SP)+, R1 ; RESTORE R1
004536 000002 RTI

004556 012777 004000 174576 .MSTCLR: MOV #MRESET, @DVSCR ; ISSUE MASTER CLEAR.
004558 000002 RTI

004566 052777 000002 174566 .ROMCLK: BIS #BIT1, @DVSCR
004568 000002 RTI

004576 010046 .DATACLK: MOV RO, -(SP)
004578 005000 CLR RO
004580 052777 000400 174560 004636 IS: BIS #BIT9, @DVLCR
004582 017737 174554 004636 MOV @DVLCR, 35
004584 106037 004637 RORB 35+1
004586 103003 BCC 25
004588 005200 INC RO
004590 001370 BNE 15
004592 104000 HLT 0
004594 012600 25: MOV (SP)+, RO
004596 000002 RTI
004598 000001 35: .BLKW 1

```

1435	004644	032777	004000	174336	SERV.G:	BIT	#4000, @TKCSR	:RX BUSY?
1436	004644	001374				BNE	SERV.G	:PR IF YES
1438	004650	017737	174326	005072		MOV	@SWR, 90\$:SAVE (SWR).
1439	004656	013777	005072	174316	1\$:	MOV	90\$, @SWR	:
1440	004664	104402	005052			TYPE	.89\$:
1441	004670	104411	005064			CNVRT	.89\$:
1442	004674	104402	005074			TYPE	.91\$:
1443	004700	105777	174300			TSTB	@TKCSR	:WAIT FOR DONE.
1444	004704	100375				BPL	-4	:
1445	004706	017746	174274			MOV	@TKDBR, -(SP,	:
1446	004712	042716	000200			BIC	#BIT7, (SP)	:
1447	004716	122726	000015			CMPB	#15, (SP)+	:
1448	004720	001450				BEG	5\$:
1449	004724	005077	174252			CLR	@SWR	:
1450	004730	105777	174254		2\$:	TSTB	@TKCSR	:
1451	004734	100375				BPL	-4	:
1452	004736	016677	177776	174246		MOV	-2(SP), @TKDBR	:
1453	004744	000241				CLC		:
1454	004746	006177	174230			ROL	@SWR	:
1455	004750	006177	174224			ROL	@SWR	:
1456	004756	006177	174220			ROL	@SWR	:
1457	004762	103735				BOS	1\$:ERROR
1458	004764	026627	177776	000060		CMP	-2(SP), #60	:
1459	004772	002731				BLT	1\$:
1460	004774	026627	177776	000057		CMP	-2(SP), #67	:
1461	005002	003325				BGT	1\$:
1462	005004	042766	177770	177776		BIC	#10(7), -2, SP,	:
1463	005012	056677	177776	174162		BIS	-2(SP), @SWR	:
1464	005020	105777	174160			TSTB	@TKCSR	:
1465	005024	100375				BPL	-4	:
1466	005026	017746	174154			MOV	@TKCSR, -(SP)	:
1467	005032	042716	000200			BIC	#BIT7, (SP)	:
1468	005036	122726	000015			CMPB	#15, (SP)+	:
1469	005042	001332				BNE	2\$:
1470	005044	104402	005104		5\$:	TYPE	MCRLF	:
1471	005050	000207				RTS	PC	:
1472	005052	020377	051450	051127	99\$:	.ASCIZ	<377>? (SWR)= ?	:
1473	005060	035451	000057			.EVEN		:
1474	005064	000001			88\$:	1		:
1475	005066	006	000			.BYTE	6,0	:
1476	005070	005072			90\$:	.WORD	0	:
1477	005072	000000			91\$:	.ASCIZ	? = / ?	:
1478	005074	035457	000057			.EVEN		:
1479	005100	020040	000077			MOM:	.ASCIZ / ? /	:
1480	005104	005015	000			MCRLF:	.ASCIZ <15><12>	:
1481	005107	377	053520	020122		MPFAIL:	.ASCIZ <377>/PWR FAILED. RESTART AT TEST	:
1482	005145	377	047105	020104		MEPASS:	.ASCIZ <377>/END PASS DZDVC-C	:
1483	005171	377	000122			MR:	.ASCIZ <377>/R/	:
1484	005174	050377	047522	051107		MERR2:	.ASCIZ <377>/PROGRAM INDICATES NO DEVICES PRESENT.	:
1485	005243	377	047111	052523		MERR3:	.ASCIZ <377>/INSUFFICIENT DATA!	:
1486	005267	377	042524	052123		MTSTPC:	.ASCIZ <377>/TEST PC-	:
1487	005301	377	047514	045503		MLOCK:	.ASCIZ <377>/LOCK ON SELECTED TEST	:

H03

MACY11 271732 17-SEP-76 11:40 PAGE 35
 P11 GENERAL UTILITIES (TYPE OUT, ERROR, SCOPE, ETC.)

1553	006166	013737	001376	001400	MOV	DVSRA, DVSFR	:SPEC. FUN. REG.
1554	006174	060037	001400		ADD	RO, DVSFR	
1555	006200	013737	001400	001402	MOV	DVSFR, DVNSR	:NPR STAT. REG.
1556	006206	060037	001402		ADD	RO, DVNSR	
1557	006212	013737	001402	001404	MOV	DVNSR, RESV16	:RESERVED REG
1558	006220	060037	001404		ADD	RO, RESV16	
1559							
1560	006224	013737	001352	001354	MOV	DVRVEC, DVRLVL	:PTY LVL
1561	006232	060037	001354		ADD	RO, DVRLVL	
1562	006236	013737	001354	001356	MOV	DVRLVL, DVTVEC	:TX VEC
1563	006244	060037	001356		ADD	RO, DVTVEC	
1564	006250	013737	001356	001358	MOV	DVTVEC, DVTLVL	:TX LVL
1565	006256	060037	001360		ADD	RO, DVTLVL	
1566							
1567	006262	012700	001416		MOV	#L00.03, RO	:LOAD STAU 00-03
1568	006266	012701	001406		MOV	#MASK.A, R1	:PREPARE MASK.
1569	006272	012702	001412		MOV	#CLK.A, R2	:PREPARE CLOCKS
1570	006276	004737	006516		JSR	PC, FIX.00	:GO AND CALCULATE CONFIGURATION.
1571							
1572	006302	012700	001420		MOV	#L04.07, RO	:LOAD STAU 00-03
1573	006306	012701	001407		MOV	#MASK.B, R1	:PREPARE MASK.
1574	006312	012702	001413		MOV	#CLK.B, R2	:PREPARE CLOCKS
1575	006316	004737	006516		JSR	PC, FIX.00	:GO AND CALCULATE CONFIGURATION.
1576							
1577	006322	012700	001422		MOV	#L08.11, RO	:LOAD STAU 00-03
1578	006326	012701	001410		MOV	#MASK.C, R1	:PREPARE MASK.
1579	006332	012702	001414		MOV	#CLK.C, R2	:PREPARE CLOCKS
1580	006336	004737	006516		JSR	PC, FIX.00	:GO AND CALCULATE CONFIGURATION.
1581							
1582	006342	012700	001424		MOV	#L12.15, RO	:LOAD STAU 00-03
1583	006346	012701	001411		MOV	#MASK.D, R1	:PREPARE MASK.
1584	006352	012702	001415		MOV	#CLK.D, R2	:PREPARE CLOCKS
1585	006356	004737	006516		JSR	PC, FIX.00	:GO AND CALCULATE CONFIGURATION.
1586	006362	032777	000002	172612	BIT	#SW01, 2SWR	
1587	006370	001445			BEQ	7\$	
1588	006372						
1589	006372	005737	000042		TST	2#42	
1590	006376	001042			BNE	7\$	
1591	006400	104402	005104		TYPE	.MORLF	
1592	006404	104403			INSTR		
1593	006406	005366			MTSTN		
1594	006410	104405			PARAM		
1595	006412	000001			I		
1596	006414	001000			I		
1597	006416	001226			I		
1598	006420	000			I		
1599	006421	001			I		
1600	006422	012700	007256		MOV	#TST1, RO	
1601	006426	022710			CMP	(PC)+, (RO)	
1602	006430	012737			MOV	(PC)+, 2(PC)+	
1603	006432	001015			BNE	6\$	
1604	006434	023760	001226	000002	CMP	TSTNO, 2(RO)	
1605	006442	001011			BNE	6\$	
1606	006444	022760	001226	000004	CMP	#TSTNO, 4(RO)	
1607	006452	001005			BNE	6\$	
1608	006454	010037	001214		MOV	RO, RETLRN	

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1609 006460 104402 005104          TYPE      MCRLF
1610 006464 000412          BR      8$
1611 006466 005720          6$: TST      (R0)+
1612 006470 020027 017056      CMP      R0, #TLAST+10
1613 006474 001354          BNE     5$
1614 006476 104402 005100      TYPE     MQM
1615 006502 000733          BR      4$
1616 006504 012737 007256 001214      7$: MOV     #TST1, RETURN      :PREPARE RETURN ADDRESS
1617 006512 000177 172476      5$: JMP     @RETURN          :GO START TESTING.
1618
1619 006516 011003          FIX.00: MOV     (R0), R3      :GET PARAMETERS.
1620 006520 042703 176377      BIC     #1<1400>, R3      :CLEAR JUNK.
1621 006524 005703          TST     R3                :TEST FOR EIGHT BITS.
1622 006526 001004          BNE     1$                :BR IF NOT 8 BITS.
1623 006530 105011          CLRB   (R1)              :SET
1624 006532 112712 000010      MCVB   #8., (R2)         :
1625 006536 000424          BR      4$
1626 006540 022703 000400          1$: CMP     #400, R3      :CHECK FOR SEVEN BITS.
1627 006544 001005          BNE     2$                :BR IF NOT 7 BITS.
1628 006546 112711 000200      MOVB   #200, (R1)        :
1629 006552 112712 000007      MOVB   #7., (R2)         :
1630 006556 000414          BR      4$
1631 006560 022703 001000          2$: CMP     #1000, R3     :CHECK FOR SIX BITS.
1632 006564 001005          BNE     3$                :BR IF NOT SIX BITS.
1633 006566 112711 000300      MOVB   #300, (R1)        :
1634 006572 112712 000006      MOVB   #6., (R2)         :
1635 006576 000404          BR      4$
1636 006600 112711 000340          3$: MOVB   #340, (R1)     :IF NONE OF THE ABOVE; MUST BE 5 BITS.
1637 006604 112712 000005      MOVB   #5., (R2)         :
1638 006610 032710 040000          4$: BIT     #PARBIT, (R0)  :PARITY ENABLED?
1639 006614 001401          BEQ     5$                :IF =0; THEN NO PARITY.
1640 006616 105212          INCB   (R2)              :PLUS ONE TO THE CLOCK!
1641 006620 000207          5$: RTS     PC
1642
1643          : *ROUTINE USED TO "AUTO SIZE" THE DV11
1644          : *CSR AND VECTOR.
1645          : *NOTE: THE CSR MAY BE ANY WHERE IN THE FLOATING
1646          : *      ADDRESS RANGE (175000:175400)
1647          : *      AND THE VECTOR MAY BE ANY WHERE IN THE
1648          : *      FLOATING VECTOR RANGE (300:770)
1649          : *
1650
1651 006622          AUTO.SIZE:
1652 006622 000005          RESET
1653 006624 012702 001500      CSRMAP: MOV     #DV.MAP, R2      :INSURE A BUS INIT.
1654 006630 005022          1$: CLR     (R2)+          :LOAD MAP POINTER.
1655 006632 022702 001740      CMP     #DV.END, R2      :ZERO ENTIRE MAP
1656 006636 001374          BNE     1$                :ALL DONE?
1657 006640 105037 001301      CLRB   DVNUM            :BR IF NO
1658 006644 012702 001500      MOV     #DV.MAP, R2      :SET OCTAL NUMBER OF DV11'S TO 0
1659 006650 012701 175000      MOV     #175000, R1      :SET FOR FIRST ADDRESS TO BE TESTED
1660 006654 012737 007074 000004      MOV     #6$, @#4        :SET FOR NON-EXISTANT DEVICE TIME OUT
1661 006662 005711          2$: TST     (R1)          :IF DV11 DVSCR S/B 0
1662 006664 001037          BNE     3$                :IF NO DEV; TRAP TO 4. IF NO BIT 9 THEN NO DV11
1663 006666 022761 177777 000012      CMP     #177777.12(R1)  :IF DV11 THEN DVSR S/B ALL 1'S ON INIT!
1664 006674 001033          BNE     3$                :BR IF NOT DV11
    
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1665	006676	005761	000016		TST	16(R1)	: IF DV11 THEN RESV16 S/B ALL D'S
1666	006702	001030			SNE	3\$: BR IF NOT D/11
1667					: AT THIS POINT IT IS ASSUMED THAT R1 HOLDS A DV11 CSR ADDRESS.		
1669	006704	010122			MOV	R1,(R2)+	: STORE CSR IN CORE TABLE.
1669	006706	005722			TST	(R2)+	: POP OVER VECTOR STORE AREA
1670	006710	052722	000226		BIS	#226,(R2)+	: SET LINE CARD 1 STAT AND SYNC
1671	006714	052722	000062		BIS	#62,(R2)+	:
1672	006720	052722	000226		BIS	#226,(R2)+	: SET LINE CARD 2 STAT AND SYNC
1673	006724	052722	000062		BIS	#62,(R2)+	:
1674	006730	052722	000226		BIS	#226,(R2)+	: SET LINE CARD 3 STAT AND SYNC
1675	006734	052722	000062		BIS	#62,(R2)+	:
1676	006740	052722	000226		BIS	#226,(R2)+	: SET LINE CARD 4 STAT AND SYNC
1677	006744	052722	000062		BIS	#62,(R2)+	:
1678	006750	105237	001301		INCB	DVNUM	: UPDATE DEVICE COUNTER
1679	006754	122737	000010	001301	CMPB	#10,DVNUM	: ARE MAX. NO. OF DEV FOUND?
1680	006762	001405			BEQ	100\$: YES DON'T LOOK FOR ANY MORE.
1681	006764	062701	000010		ADD	#10,R1	: UPDATE CSR POINTER ADDRESS
1682	006770	022701	175400		CMP	#175400,R1	:
1683	006774	001332			BNE	2\$: BR IF MORE ADDRESS TO CHECK.
1684	006776	012722	177777		MOV	#177777,(R2)+	: TERMINATER.
1685	007002	105037	001300		CLAB	DVACTV	:
1686	007006	105737	001301		TSTB	DVNUM	: WERE ANY DV11'S FOUND AT ALL?
1687	007012	001423			BEQ	5\$: ERROR AUTO SIZER FOUND NO DV11'S IN THIS SYS.
1688	007014	113701	001301		MOVB	DVNUM,R1	:
1689	007020	110137	001303		MOVB	R1,SAVNUM	: SAVE NUMBER OF DEVICES
1690	007024	000241			CLC		:
1691	007026	106137	001300		ROLB	DVACTV	: GENERATE ACTIVE REGISTER OF DEVICES.
1692	007032	105237	001300		INCB	DVACTV	: SET THE BIT
1693	007036	005301			DEC	R1	:
1694	007040	001371			BNE	4\$: BR IF MORE TO GENERATE
1695	007042	012737	000006	000004	MOV	#6,D#4	: RESTORE TRAP VECTOR
1696	007050	113737	001300	001302	MOV	DVACTV,SAVACT	: SAVE ACTIVE REGISTER
1697	007056	000137	007102		JMP	VECMAP	: GO FIND THE VECTOR NOW.
1698	007062	104402	005174		TYPE	MERR2	: NOTIFY OPR THAT NO DV11'S FOUND.
1699	007066	005000			CLR	RO	: MAKE DATA LIGHTS ZERO
1700	007070	000000			HALT		: STOP THE SHOW
1701	007072	000776			BR	.-2	: DISABLE CONT. SW.
1702	007074	012716	006754		MOV	#3\$(SP)	: ENTERED BY NON-EXISTANT TIME-OUT.
1703	007100	000002			RTI		: RETURN TO MAINSTREAM
1704							
1705	007102	012737	000340	000022	VECMAP: MOV	#340,D#22	: SET IOT TRAP PRIO TO 7
1706	007110	012737	007232	000020	MOV	#4\$,D#20	: SET IOT TRAP VECTOR
1707	007116	012702	001500		MOV	#DV.MAP,R2	: SET SOFTWARE POINTER
1708	007122	012700	000300		MOV	#300,RO	: FLOATING VECTORS START HERE.
1709	007126	012701	000302		MOV	#302,R1	: PC OF IOT INSTR.
1710	007132	010120			MOV	R1,(RO)+	: START FILLING VECTOR AREA
1711	007134	012721	000004		MOV	#4,(R1)+	: WITH .+2: IOT
1712	007140	022021			CMP	(RO)+(R1)+	: ADD 2 TO RO +R1
1713	007142	020127	001000		CMP	R1,#1000	:
1714	007146	101771			BLOS	1\$: BR IF MORE TO FILL
1715	007150	113737	001300	001246	MOV	DVACTV,TEMP1	: STORE TEMPORALLY
1716	007156	006037	001246		ROR	TEMP1	: BRING OUT A BIT
1717	007162	103034			BCC	5\$: BR IF ALL DONE
1718	007164	005037	177776		CLR	PS	: ZERO CPU PRIO
1719	007170	012772	001300	000000	MOV	#BIT9+BIT7+BIT6,D(R2)	:
1720	007176	005000			CLR	RC	: ATTEMPT TO FORCE AN INTERRUPT

K03

1721	007200	005200			INC	R0	:STALL
1722	007202	001376			ONE	:-2	: FOR TIME TO INTERRUPT
1723	007204	052762	000300	000002	BIS	#300,2(R2)	:NO INTERRUPT ASSUME 300 AND FIX DV11 LATER
1724	007212	042772	176777	000000	BIC	#1C<BIT9>,0(R2)	
1725	007220	005072	000000		CLR	0(R2)	
1726	007224	062702	000024		ADD	#24,R2	:POP SOFTWARE POINTER
1727	007230	000752			BR	2\$:KEEP GOING
1728	007232	051662	000002		BIS	(SP),2(R2)	:GET VECTOR ADDRESS
1729	007236	042762	000007	000002	BIC	#7,2(R2)	:CLEAR JUNK
1730	007244	022626			CHP	(SP)+,(SP)+	:POP ICT JUNK OFF STACK
1731	007246	012716	007212		MOV	#3\$, (SP)	:SET FOR RETURN
1732	007252	000002			RTI		
1733	007254	000207			RTS	PC	:ALL DONE WITH "AUTO SIZING"

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007256	012737	000001	001226
007264	012737	007372	001216
007272	104412		
007274	012777	000010	172060
007302	012777	000400	172070
007310	012700	023750	
007314	005002		
007316	012777	000002	172036
007324	052777	000004	172030
007332	011005		
007334	017704	172040	
007340	020504		
007342	001401		
007344	104001		
007346	005720		
007350	022700	025536	
007354	001405		
007356	052777	000002	171776
007364	005202		
007366	000761		
007370	104400		
007372	012737	000002	001226
007400	012737	010160	001216
007406	012700	000000	

```

:***** TEST 1 *****
:*TEST TO VERIFY DV11 ROM DATA.
:*THIS PROGRAM WILL PLACE ROM ADDRESS
:*ZERO INTO THE DVSFR AND BIT 8
:*(TEST POINT 1(+3 VOLTS(TRUE))) AND BRANCH "A".
:*A ROM CYCLE WILL BE ISSUED AND
:*BRANCH "NEVER" WILL BE ASSERTED.
:*THE DATA WILL BE COMPARED AGAINST THE
:*CORE IMAGE FOR VALIDITY
:*AND THE ROM WILL BE CYCLED TO THE END.
:*****

```

: TEST 1

```

-----
TST1:  MOV    #1,TSTNO
      MOV    #TST2,NEXT
      MSTCLR
      MOV    #BIT3,DVSCR      ;INIT DV11
      MOV    #BIT8,DVSFR     ;SET "SOURCE SEL"
      MOV    #ROMDATA,R0     ;SET BRA +3 VOLT (SURE TRUE)
      CLR    R2              ;GET SOFTWARE POINTER FOR COMPARISON
      MOV    #BIT1,DVSCR     ;ZERO ROM ADDRESS IMAGE
      BIS    #BIT2,DVSCR     ;SET ROM CLK
      MOV    (R0),R5         ;SET BRANCH DSABLE
      CMP    #ENDROM,R0     ;GET SOFTWARE ROM IMAGE
      BEQ    2$              ;GET ACTUAL ROM DATA
      HLT    1               ;ROM DATA CORRECT
      TST    (R0)+          ;BR IF YES
      CMP    #ENDROM,R0     ;ROM DATA COMPARISON ERROR
      BEQ    3$              ;UPDATE SOFTWARE POINTER
      BIS    #BIT1,DVSCR     ;ALL DATA DONE
      INC    R2              ;BR IF YES
      BR    1$              ;CLK ROM
      SCOPE
      1$:  MOV    #DVSFR,R4   ;UPDATE ROM IMAGE ADDRESS
      CMP    R5,R4          ;CONT TESTING
      BEQ    2$              ;SCOPE THIS TEST
      2$:  HLT    1
      3$:  HLT    1

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:***** TEST 2 *****
:*TEST OF DV11 MICRO PROCESSOR "FREE RUNNING"
:*TEST TO XMIT ONE CHAR (ALL 0'S) MAKING SURE THAT
:*BIT 15 OF DVSCR =1
:*TX WC PRIMARY =0
:*TX BA PRIMARY =#TXBAP+1
:*LINE STATE =BIT7
:*TX BA SECONDARY =0
:*TX WC SECONDARY =0
:*NPR STATUS REG 00:03 =LINE DESIRED PLUS BIT 8 SET
:*THIS TEST IS EXERCISED FOR BOTH ASYNC AND SYNC LINE CARDS.
:*****

```

: TEST 2

```

-----
TST2:  MOV    #2,TSTNO
      MOV    #TST3,NEXT
      MOV    #0.,R0         ;PLACE LINE NUMBER INTO R0

```

M03

DZDVC-C MACY11 27(732) 17-SEP-76 11:40
 DZDVCC.P11 DV11 DEVICE DIAGNOSTICS.

PAGE 40
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1791	007412	013737	001416	001236		MOV	L00.03, STAT	;LOAD LINE CARD STATUS INTO STAT
1792	007420	100402				BMI	100\$;BR IF LINE CARD NOT TO BE TESTED
1793	007422	004737	007510			JSR	PC, 105\$;GO DO THE TEST FOR LINE CARD 1
1794	007426	012700	000004		100\$:	MOV	#4, R0	;PLACE LINE NUMBER INTO R0
1795	007432	013737	001420	001236		MOV	L04.07, STAT	;LOAD LINE CARD STATUS INTO STAT
1796	007440	100402				BMI	101\$;BR IF LINE CARD NOT TO BE TESTED
1797	007442	004737	007510			JSR	PC, 105\$;GO DO THE TEST FOR LINE CARD 2
1798	007446	012700	000010		101\$:	MOV	#8, R0	;LOAD LINE NUMBER
1799	007452	013737	001422	001236		MOV	L08.11, STAT	;LOAD LINE CARD STATUS INTO STAT
1800	007460	100402				BMI	102\$;BR IF LINE CARD NOT TO BE TESTED
1801	007462	004737	007510			JSR	PC, 105\$;DO THE TEST FOR LINE CARD 3
1802	007466	012700	000014		102\$:	MOV	#12, R0	;LOAD LINE NO.
1803	007472	013737	001424	001236		MOV	L12.15, STAT	;LOAD LINE CARD STATUS
1804	007500	100402				BMI	103\$;BR IF LINE CARD NOT TO BE TESTED
1805	007502	004737	007510			JSR	PC, 105\$;DO THE TESTS FOR LINE CARD 4
1806	007506	104400			103\$:	SCOPE		;SCOPE THIS TEST.
1807	007510				105\$:			;TEST ENTRANCE.
1808	007510	104413				RAMCLR		;CLEAR ALL DV11 SECONDARY REGISTERS
1809	007512	012705	022350			MOV	#TXTAB, R5	;CLEAR
1810	007516	005001				CLR	R1	TX
1811	007520	105025			21\$:	CLRB	(R5)+	CONTROL
1812	007522	105201				INCB	R1	TABLE
1813	007524	001375				BNE	21\$	
1814	007526	012702	000004			MOV	#4, R2	;SET FOR 4 LINE GROUP
1815	007532	012737	007540	001220		MOV	#1\$, LOCK	;SET FOR SW09=1
1816	007540	110077	171626		1\$:	MOV#	R0, @DVSR5	;LOAD LINE NUMBER
1817	007544	004537	021026			PERFORM	SETREG	
1818	007550	000	010			.BYTE	000, 010	;BUS ADDRESS. CONTROL TABLE
1819	007552	021350				TXBAP		
1820	007554	022350				TXTAB		
1821	007556	005037	021350			CLR	TXBAP	;SET TX DATA TO 0
1822	007562	004537	021026			PERFORM	SETREG	
1823	007566	013	001			.BYTE	013, 001	;LINE STATE, PRINCIPLE BYTE COUNT
1824	007570	000004				BIT2		;LINE STATE CONTENTS
1825	007572	177777				-1		;ONE CHAR
1826	007574	032737	004000	001236		BIT	#ASYNC, STAT	;#IS THIS ASYNC LINE CARD?
1827	007602	001407				BEQ	60\$;#BR IF NO.
1828	007604	004537	021072			PERFORM	LOAD.MODE	
1829	007610	015000				<BIT12+BIT11>+BIT9		;#8 BITS/PER/CHAR
1830	007612	004537	021072			PERFORM	LOAD.MODE	;#SET BAUD RATE REGISTER.
1831	007616	072000				<BIT14+BIT13+BIT12>+BIT10		
1832								;#9600 BAUD.
1833	007620	000403				BR	61\$;#CONTINUE TEST.
1834	007622	004537	021072		60\$:	PERFORM	LOAD.MODE	;LOAD MODE
1835	007626	014000				BIT12+BIT11		
1836	007630	005277	171526		61\$:	INC	@DVSCR	;SET MICRO-PROCESSOR GO!
1837	007634	005005				CLR	R5	;WAIT FOR 15=1
1838	007636	005777	171520		2\$:	TST	@DVSCR	;DVSCR 15=1?
1839	007642	100403				BMI	3\$;BR IF YES
1840	007644	104414				DELAY		;WASTE TIME
1841	007646	005205				INC	R5	;DELAY
1842	007650	001372				BNE	2\$;ALL DONE?
1843	007652	013701	001362		3\$:	MOV	DVSCR, R1	;SET POINTER
1844	007656	011104				MOV	(R1), R4	;READ SCR
1845	007660	012705	100001			MOV	#BIT15+BIT0, R5	;SET EXPECTED
1846	007664	020504				CMF	R5, R4	;RESULTS GOOD?

N03

1847	007666	001401			BEQ	4\$;BR IF OK
1848	007670	104002			HLT	2	;DVSCR WRONG
1849	007672	005777	171470	4\$:	TST	2DVSCR	;MAKE SURE NO RIC ENTRIES
1850	007676	001405			BEQ	5\$;BR IF OK
1851	007700	013701	001356		MOV	DVSCR,R1	;SET POINTER
1852	007704	011104			MOV	(R1),R4	;SAVE FOR TYPE OUT
1853	007706	005005			CLR	R5	;MAKE EXPECTED=0
1854	007710	104002			HLT	2	;REPORT RIC NOT=0
1855	007712	010005		5\$:	MOV	R0,R5	;LOAD LINE NUMBER
1856	007714	052705	100400		BIS	#BIT15+BIT8,R5	;SILO ENTRY PRINCIPLE BYTE COUNT=0
1857	007720	012703	000020		MOV	#16,R3	;SET FOR 16 REGISTERS
1858	007724	013701	001402		MOV	DVNSR,R1	;SET POINTER
1859	007730	011104			MOV	(R1),R4	;READ NSR
1860	007732	020504			CMP	R5,R4	;OK?
1861	007734	001401			BEQ	6\$;BR IF OK
1862	007736	104002			HLT	2	;DVNSR NOT CORRECT
1863	007740	013701	001362	6\$:	MOV	DVSCR,R1	;SET POINTER
1864	007744	011104			MOV	(R1),R4	;READ DVSCR (DID BITS CLEAR)
1865	007746	100005			BPL	7\$;BR IF 15=0
1866	007750	012705	000001		MOV	#BIT0,R5	;SET EXPECTED RESULTS
1867	007754	104002			HLT	2	;BIT 15 OF DVSCR NOT CLEARED BY READING NSR
1868	007756	005777	171420		TST	2DVNSR	;REFERENCE NSR
1869	007762	005303		7\$:	DEC	R3	;ALL REGISTERS DONE?
1870	007764	001365			BNE	6\$;BR IF NO
1871	007766	042777	000001 171366		BIC	#BIT0,2DVSCR	;CLEAR MICRO-PROCESSOR GO
1872	007774	012705	021351		MOV	#TXBAP+1,R5	;SET EXPECTED
1873	010000	010077	171366		MOV	R0,2DVSR5	;LOAD LINE NUMBER
1874	010004	017704	171366		MOV	2DVSR4,R4	;READ BUS ADDRESS
1875	010010	117701	171360		MOVB	2DVSR5H,R1	;GET SEC REG.
1876	010014	020504			CMP	R5,R4	;GOOD?
1877	010016	001401			BEQ	8\$;BR IF GOOD
1878	010020	104003			HLT	3	;BUS ADDRESS NOT INCREMENTED CORRECTLY
1879	010022	105277	171345	8\$:	INCB	2DVSR5H	;EXAMINE
1880	010026	005201			INC	R1	
1881	010030	017704	171342		MOV	2DVSR4,R4	;BYTE COUNT REGISTER
1882	010034	001402			BEQ	10\$;IS IT=0?
1883	010036	005005			CLR	R5	;SET EXPECTED
1884	010040	104003			HLT	3	;BYTE COUNT NOT=0!
1885	010042	010077	171324	10\$:	MOV	R0,2DVSR5	;LOAD LINE NUMBER
1886	010046	112777	000002 171320		MOVB	#002,2DVSR5H	;GET OPPOSITE BUS ADDRESS
1887	010054	005005			CLR	R5	;SET EXPECTED
1888	010056	117701	171312		MOVB	2DVSR5H,R1	;GET SEC REG.
1889	010062	017704	171310		MOV	2DVSR4,R4	;READ RESULT
1890	010066	001401			BEQ	11\$;BRANCH IF=0
1891	010070	104003			HLT	3	;OPPOSITE BUS ADDRESS SHOULDN'T BE ALTERED.
1892	010072	105277	171276	11\$:	INCB	2DVSR5H	;GET OPPOSITE BYTE COUNT
1893	010076	005201			INC	R1	;SET SEC POINTER
1894	010100	017704	171272		MOV	2DVSR4,R4	;READ
1895	010104	001401			BEQ	12\$;BRANCH IF=0
1896	010106	104003			HLT	3	;OPPOSITE BYTE CNT S/B=0
1897	010110	012705	000200	12\$:	MOV	#BIT7,R5	;SET EXPECTED RESULTS
1898	010114	112777	000013 171252		MOVB	#13,2DVSR5H	;SEL LINE STATE
1899	010122	112701	000013		MOVB	#13,R1	;SET SEC REG POINTER
1900	010126	017704	171244		MOV	2DVSR4,R4	;READ LINE STATE
1901	010132	020504			CMP	R5,R4	;OK
1902	010134	001401			BEQ	13\$;OK!


```

:LINE STATE INCORRECT
:LINE DIV
:LINE POINTERS
:LINE PHONE
:BA YES
:BA NO
:RETURN FOR NEXT GROUP

```

```

***** TEST 3 *****
:TEST OF DV11 MICRO PROCESSOR "FREE RUNNING"
:TEST TO XMIT ONE CHAR (ALL 0'S) "MAKING SURE THAT"
:BIT 15 OF DVSCR = 1
:TX WC PRIMARY = 0
:TX BA PRIMARY = 0
:LINE STATE = 0
:TX BA SECONDARY = TXBAS+1
:TX WC SECONDARY = 0
:NPR STATUS REG 00:03=LINE SELECTED +BIT9+BIT8=1
:THIS TEST IS EXERCISED FOR BOTH ASYNC AND SYNC LINE CARDS.
*****

```

: TEST 3

```

:-----
:TEST3: MOV #3,TSTNO
: MOV #TST4,NEXT
: MOV #0,R0
: MOV LO0.03,STAT
: BMI 100$
: JSR PC,105$
:100$: MOV #4,R0
: MOV LO4.07,STAT
: BMI 101$
: JSR PC,105$
:101$: MOV #8,R0
: MOV LO8.11,STAT
: BMI 102$
: JSR PC,105$
:102$: MOV #12,R0
: MOV L12.15,STAT
: BMI 103$
: JSR PC,105$
:103$: SCOPE
:105$: RAMCLR
: MOV #TXTAB,R5
: CLR R1
:21$: CLRB (R5)+
: INCB R1
: BNE 21$
: MOV #4,R2
: MOV #1$,LOCK
:1$: MOV# R0,DVSR5
: PERFORM SETREG
: .BYTE 002,010

```

```

:PLACE LINE NUMBER INTO R0
:LOAD LINE CARD STATUS INTO STAT
:BR IF LINE CARD NOT TO BE TESTED
:GO DO THE TEST FOR LINE CARD 1
:PLACE LINE NUMBER INTO R0
:LOAD LINE CARD STATUS INTO STAT
:BR IF LINE CARD NOT TO BE TESTED
:GO DO THE TEST FOR LINE CARD 2
:LOAD LINE NUMBER
:LOAD LINE CARD STATUS INTO STAT
:BR IF LINE CARD NOT TO BE TESTED
:DO THE TEST FOR LINE CARD 3
:LOAD LINE NO.
:LOAD LINE CARD STATUS
:BR IF LINE CARD NOT TO BE TESTED
:DO THE TESTS FOR LINE CARD 4
:SCOPE THIS TEST.
:TEST ENTRANCE.
:CLEAR ALL DV11 SECONDARY REGISTERS
:CLEAR
: TX
: CONTROL
: TABLE
:SET FOR 4 LINE GROUP
:SET FOR SW09=1
:LOAD LINE NUMBER
:BUS ADDRESS. CONTROL TABLE

```

```

:012737 000003 001226
:012737 012754 001216
:012700 000000
:013737 001416 001236
:100402
:004737 010276
:012700 000004
:013737 001420 001236
:100402
:004737 010276
:012700 000010
:013737 001422 001236
:100402
:004737 010276
:012700 000014
:013737 001424 001236
:100402
:004737 010276
:104400
:104413
:012705 022350
:005001
:105025
:105201
:001375
:012705 000004
:012737 010326 001220
:110077 171040
:004537 021026
:002 010

```

C04

```

:959 010340 021750
:960 010342 022350
:961 010344 005037 021750
:962 010350 004537 021026
:963 010354 013 003
:964 010356 000204
:965 010360 117777
:966 010362 032737 004003 001236
:967 010370 001401
:968 010372 004537 021072
:969 010376 015000
:970 010400 004537 021072
:971 010404 072000
:972 010406 000403
:973 010410 004537 021072
:974 010414 014000
:975 010416 005277 170740
:976 010420 005005
:977 010424 005777 170732
:978 010430 100403
:979 010434 104414
:980 010438 005205
:981 010442 001372
:982 010446 013701 001362
:983 010450 011104
:984 010454 012705 100001
:985 010458 020504
:986 010462 001401
:987 010466 104002
:988 010470 005777 170702
:989 010474 001405 001366
:990 010478 011104
:991 010482 005005
:992 010486 104002
:993 010490 010005 55:
:994 010502 052705 101400
:995 010506 012703 000020
:996 010512 013701 001402
:997 010516 011104
:998 010520 020504
:999 010524 104002
0000 010526 013701 001362
0001 010532 011104
0002 010534 100005
0003 010536 012705 000001
0004 010542 104002
0005 010544 005777 170632
0006 010550 005303 75:
0007 010552 001365
0008 010554 042777 000001 170600
0009 010562 012705 021751
0010 010566 010077 170600
0011 010572 112777 000002 170574

```

```

TXBAS
TXTAB
CLR TXBAS ;SET TX DATA TO 0
PERFORM SETREG
.BYTE 013,003 ;LINE STATE, ALTERNATE BYTE COUNT
BIT7+BIT2 ;LINE STATE CONTENTS
-1 ;ONE CHAR
BIT #ASYNC,STAT ;IS THIS ASYNC LINE CARD?
BEQ 605 ;BR IF NO.
PERFORM LOAD.MODE
<BIT12+BIT11>+BIT9 ;#8 BITS PER/CHAR
PERFORM LOAD.MODE ;SET BAUD RATE REGISTER.
<BIT14+BIT13+BIT12>+BIT10 ;#9500 BAUD.
BR 615 ;CONTINUE TEST.
PERFORM LOAD.MODE ;LOAD MODE
BIT12+BIT11
605: INC DVSCR ;SET MICRO-PROCESSOR GO!
CLR R5 ;WAIT FOR 15=1
TST DVSCR ;DVSCR 15=1?
BMI 35 ;BR IF YES
DELAY ;WASTE TIME
INC R5 ;DELAY
BNE 25 ;ALL DONE?
MOV DVSCR,R1 ;SET POINTER
MOV (R1),R4 ;READ SCR
MOV #BIT15+BIT0,R5 ;SET EXPECTED
CMP R5,R4 ;RESULTS GOOD?
BEQ 45 ;BR IF OK
HLT ;DVSCR WRONG
TST DVSCR ;MAKE SURE NO RIC ENTRIES
BEQ 55 ;BR IF OK
MOV DVSCR,R1 ;SET POINTER
MOV (R1),R4 ;SAVE FOR TYPE OUT
CLR R5 ;MAKE EXPECTED=0
HLT ;REPORT RIC NOT=0
MOV R0,R5 ;LOAD LINE NUMBER
BIS #BIT15+BIT9+BIT8,R5 ;SILO ENTRY ALTERNATE BYTE COUNT=0
MOV #16,R3 ;SET FOR 16 REGISTERS
MOV DVNSR,R1 ;SET POINTER
MOV (R1),R4 ;READ NSR
CMP R5,R4 ;OK?
BEQ 65 ;BR IF OK
HLT ;DVNSR NOT CORRECT
MOV DVSCR,R1 ;SET POINTER
MOV (R1),R4 ;READ DVSCR (DID BITS CLEAR)
BPL 75 ;BR IF 15=0
MOV #BIT0,R5 ;SET EXPECTED RESULTS
HLT ;BIT 15 OF DVSCR NOT CLEARED BY READING NSR
TST DVNSR ;REFERENCE NSR
DEC R3 ;ALL REGISTERS DONE?
BNE 65 ;BR IF NO
BIC #BIT0,DVSCR ;CLEAR MICRO-PROCESSOR GO
MOV #TXBAS+1,R5 ;SET EXPECTED
MOV R0,DVSR5 ;LOAD LINE NUMBER
MOVB #2,DVSR5H ;SEL ALTERNATE BUS ADDRESS

```

```

010600 017704 170572
010604 117701 170564
010610 020504
010612 001401
010614 104003
010616 105277 170552
010622 005201
010624 017704 170546
010630 001402
010632 005005
010634 104003
010636 010077 170530
010642 112777 000000 170524
010650 005005
010652 117701 170516
010656 017704 170514
010662 001401
010664 104003
010666 105277 170502
010672 005201
010674 017704 170476
010700 001401
010702 104003
010704 012705 000000
010710 112777 000013 170456
010716 112701 000013
010722 017704 170450
010726 020504
010730 001401
010732 104003
010734 104412 133:
010736 104401
010740 005200
010742 005302
010744 001402
010746 000137 010326
010752 000201

```

```

MOV DVSRA,R4 :READ BUS ADDRESS
MOVB DVSRSH,R1 :GET SEC REG.
CMP R5,R4 :GOOD?
BEQ 85 :BR IF GOOD
HLT 3 :BUS ADDRESS NOT INCREMENTED CORRECTLY
INCB DVSRSH :EXAMINE
INC R1 :
MOV DVSRA,R4 :BYTE COUNT REGISTER
BEQ 105 :IS IT=0?
CLR R5 :SET EXPECTED
HLT 3 :BYTE COUNT NOT=0!
MOV R0,DVSR5 :LOAD LINE NUMBER
MOVB #000,DVSRSH :GET OPPOSITE BUS ADDRESS
CLR R5 :SET EXPECTED
MOVB DVSRSH,R1 :GET SEC REG.
MOV DVSRA,R4 :READ RESULT
BEQ 115 :BRANCH IF=0
HLT 3 :OPPOSITE BUS ADDRESS SHOULDN'T BE ALTERED.
INCB DVSRSH :GET OPPOSITE BYTE COUNT
INC R1 :SET SEC POINTER
MOV DVSRA,R4 :READ
BEQ 125 :BRANCH IF=0
HLT 3 :OPPOSITE BYTE CNT S B=0
MOV #0,R5 :SET EXPECTED RESULTS
MOVB #13,DVSRSH :SEL LINE STATE
MOVB #13,R1 :SET SEC REG POINTER
MOV DVSRA,R4 :READ LINE STATE
CMP R5,R4 :OK
BEQ 135 :OK!
HLT 3 :LINE STATE INCORRECT
MSTCLR :INIT DV11
SCOPI :SW09=1?
INC R0 :UPDATE LINE POINTER
DEC R2 :4 LINES DONE YET?
BEQ .+6 :BR IF YES
JMP 15 :JMP IF NO
RTS PC :RETURN FOR NEXT GROUP

```

```

***** TEST 4 *****
*TEST OF TRANSMITTER NON-EXISTANT MEMORY FLAGING.
*THIS TEST VERIFIES THAT THE MICRO-PROCESSOR
*CAN FLAG A NON-EXISTANT TX BUS ADDRESS.
*EXPECTED: (THIS IS FOR LINES )
*DVSCR 9IT15+BIT0
*DVNSR 03:00=LINE 11:08=0 BIT15=1
*TXBAP 177320
*TXWCP 177777
*DVLINE STATE BIT4=1
*THIS TEST IS DONE FOR SYNC AND ASYNC LINE CARDS.
*****

```

```

010754 012737 000004 001226
010762 012737 011434 001216

```

```

: TEST 4
-----
TST4: MOV #4,TSTNO
MOV #TSTS,NEXT

```

E04

27.732' 17-SEP-76 11:40
 DV11 DEVICE DIAGNOSTICS.

PAGE 45
 COPYRIGHT 1975 DIGITAL EQUIP. CORP.

Address	Hex	Dec	Label	Instruction	Comments
011070	012700	000000		MOV #0.,R0	:PLACE LINE NUMBER INTO R0
011072	013737	001416	001236	MOV L00.03,STAT	:LOAD LINE CARD STATUS INTO STAT
011002	100402			BMI 100\$:BR IF LINE CARD NOT TO BE TESTED
011004	004737	011072		JSR PC.105\$:GO DO THE TEST FOR LINE CARD 1
011010	012700	000004	100\$:	MOV #4.,R0	:PLACE LINE NUMBER INTO R0
011014	013737	001420	001236	MOV L04.07,STAT	:LOAD LINE CARD STATUS INTO STAT
011022	100402			BMI 101\$:BR IF LINE CARD NOT TO BE TESTED
011024	004737	011072		JSR PC.105\$:GO DO THE TEST FOR LINE CARD 2
011030	012700	000010	101\$:	MOV #8.,R0	:LOAD LINE NUMBER
011034	013737	001422	001236	MOV L08.11,STAT	:LOAD LINE CARD STATUS INTO STAT
011042	100402			BMI 102\$:BR IF LINE CARD NOT TO BE TESTED
011044	004737	011072		JSR PC.105\$:DO THE TEST FOR LINE CARD 3
011050	012700	000014	102\$:	MOV #12.,R0	:LOAD LINE NO.
011054	013737	001424	001236	MOV L12.15,STAT	:LOAD LINE CARD STATUS
011062	100402			BMI 103\$:BR IF LINE CARD NOT TO BE TESTED
011064	004737	011072		JSR PC.105\$:DO THE TESTS FOR LINE CARD 4
011070	104400		103\$:	SCOPE	:SCOPE THIS TEST.
011072			105\$:		:TEST ENTRANCE.
011074	104413			RAMCLP	:CLEAR ALL SEC. REGISTERS
011076	012737	011106	001220	MOV #15,LOCK	:SET IF SW09=1
011102	012702	000004		MOV #4,R2	:SET FOR A 4 LINE GROUP
011106	010077	170260		MOV R0,DVSR5	:LOAD LINE NO.
011112	052777	000060	170242	BIS #BIT5+BIT4,DVSCR	
011120	004537	021026		PERFORM SETREG	:SET EA BITS
011124	000	013		.BYTE 000,010	:GO LOAD BUS ADDRESS AND CNTRL. TABLE
011126	177320			177320	:THIS IS ADDRESS OF 2ND KE11
011130	022350			TXTAB	
011132	042777	000060	170222	BIC #BIT5+BIT4,DVSCR	
011140	004537	021026		PERFORM SETREG	:CLEAR EA BITS FOR CERTAIN
011144	013	001		.BYTE 013,001	:LOAD LINE STATE AND PRINCIPLE BYTE CNT.
011146	000004			BIT2	:TX GO
011150	177777			-1	:ONE CHAR
011152	032737	004000	001236	BIT #ASYNC,STAT	:#IS THIS ASYNC LINE CARD?
011156	001407			BEQ 60\$:#BR IF NO.
011162	004537	021072		PERFORM LOAD.MODE	
011166	015000			<BIT12+BIT11>+BITS	:#8 BITS/PER/CHAR
011170	004537	021072		PERFORM LOAD.MODE	:#SET BAUD RATE REGISTER.
011174	072000			<BIT14+BIT13+BIT12>+BIT10	
011176	000403			BR 61\$:#9600 BAUD.
011200	004537	021072	60\$:	PERFORM LOAD.MODE	:#CONTINUE TEST.
011204	014000			BIT12+BIT11	:LOAD
011206	005277	170150	61\$:	INC DVSCR	:MODE
011212	005005			CLR R5	:SET MICRO PROCESSOR GO
011214	005777	170142	2\$:	TST DVSCR	:PREPARE TIMER
011220	100403			BMI 3\$:SILO ENTRY
011222	104414			DELAY	:BR IF DONE
011224	005205			INC R5	:WASTE TIME
011226	001372			BNE 2\$:DELAY
011230	013701	001362	3\$:	MOV DVSCR,R1	:SET POINTER
011234	011104			MOV (R1),R4	:READ SCR
011236	012705	100001		MOV #BIT15+BIT0,R5	:SET EXPECTED RESULTS
011242	020504			CMP R5,R4	:DVSCR OK?
011244	001401			BEQ 4\$	
011246	104002			HLT 2	:DVSCR INCORRECT
011250	042777	000001	170104	BIC #BIT0,DVSCR	:CLEAR MICRO CPU GO

F04

27.7321 17-SEP-76 11:40
DVI1 DEVICE DIAGNOSTICS.

PAGE 46
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011256	013005		MOV	R0,R5	:LOAD LINE NO.
011260	052705	100000	BIS	#BIT15,R5	:SET SILO ENTRY
011264	013701	001403	MOV	DVNSR,R1	:SET POINTER
011270	011104		MOV	(R1),R4	:READ NSR
011274	020504		CMP	R5,R4	:NSR OK?
011276	001401		BEQ	5\$	
011280	104003		HLT	2	:DVNSR INCORRECT
011300	005005		CLR	R5	:SET EXPECTED RESULTS TO 0
011302	013701	001362	MOV	DVSCR,R1	:SET POINTER
011306	011104		MOV	(R1),R4	:READ DVSCR
011310	001401		BEQ	6\$:IS IT=0?
011312	104003		HLT	2	:MOST LIKELY BIT 15 IS NOT=0
011314	010077	170052	MOV	R0,DVSR5	:LOAD LINE NO.
011320	017704	170052	MOV	DVSR4,R4	:READ TX BUS ADDRESS PRINCIPLE
011324	012705	177320	MOV	#177320,R5	:LOAD EXPECTED
011330	005001		CLR	R1	:SET SEC REG POINTER
011332	020504		CMP	R5,R4	:DID IT INCREMENT?
011334	001401		BEQ	7\$:BR IF NO
011336	104003		HLT	3	:BUS ADDRESS INCORRECT
011340	012705	177777	MOV	#-1,R5	:SET EXPECTED BYTE COUNT
011344	105277	170024	INCB	DVSR5H	:SEL PRINCIPLE BYTE COUNT
011350	005201		INC	R1	:SET SEC REG POINTER
011352	017704	170020	MOV	DVSR4,R4	:READ IT
011356	020504		CMP	R5,R4	:DID IT GO TO ZERO?
011360	001401		BEQ	9\$:BR IF NO
011362	104003		HLT	3	:BYTE CNT S/B=-1
011364	012705	000020	MOV	#BIT4,R5	:LINE STATE S/B TX NXM
011370	012701	000013	MOV	#13,R1	:SET SEC REG POINTER
011374	112777	000013	MOVB	#13,DVSR5H	:SEL LINE STATE
011402	017704	167770	MOV	DVSR4,R4	:READ IT
011406	020504		CMP	R5,R4	:OK
011410	001401		BEQ	10\$	
011412	104003		HLT	3	:TX NUM S/B ONLY THING SET IN LINE STATE
011414	104412		MSTCLR		:INIT DVI1
011416	104401		SCOPI		:LOCK ON LINE?
011420	005200		INC	R0	:UPDATE LINE POINTER
011422	005302		DEC	R2	:4 LINE GROUP DONE
011424	001402		BEQ	11\$:BR IF YES
011426	000137	011106	JMP	1\$:JMP IF NO
011432	000207		RTS	PC	:EXIT FOR NEXT GROUP

```

***** TEST 5 *****
*TEST TO FORCE ALL POSSIBLE
*TRANSMITTER NXM ERRORS PAYING
*ATTENTION TO THE DVNSR ENTRY.
* EXERCISED EXPECTED DVNSR (BIT15 ALWAYS=!)
* TXBAP 11:08=0 03:00=LINE NO.
* TXBAS BIT9=1 03:00=LINE NO.
* TXTAB BIT11=! 03:00=LINE NO.
*THIS TEST IS DONE FOR SYNC AND ASYNC LINE CARDS.
*****

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TEST 5

011434	012737	000005	001226	TST5: MOV #5,TSTNC
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000000.F11

27.732 17-SEP-76 11:40
DVI: DEVICE DIAGNOSTICS.

PAGE 48
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Address	Hex	Hex	Hex	Hex	Label	Comment
011732	104401			45:	SCOPI	: LOCK?
011734	012737	011732	001220		MOV #55, LOCK	: PREPARE LOOP
011736	104412			55:	MSTCLR	: INIT DVI
011738	010077	167432			MOV R0, DVSR5	: LOAD LINE NO.
011740	052777	000060	167414		BIS #BITS+BIT4, DVSCR	
011742	004537	021026			PERFORM SETREG	: SET EA BITS
011744	002	010			.BYTE 002, 010	: ALTERNATE BA, CNTRL TABLE
011746	177320				177320	: NXM [2ND KE11]
011748	022350				TXTAB	
011750	004537	021026			PERFORM SETREG	
011752	013	003			.BYTE 013, 003	: LINE STATE, ALTERNATE BYTE CNT
011754	000204				BIT7+BIT2	: USE ALTERNATE TABLE, TXGO
011756	177777				-1	: ONE CHAR
011758	032737	004000	001236		BIT #ASYNC, STAT	: #IS THIS ASYNC LINE CARD?
012000	001407				BEG 615	: #BR IF NO.
012002	004537	021072			PERFORM LOAD.MODE	
012004	015000				<BIT12+BIT11>+BIT9	: #8 BITS/PER/CHAR
012006	004537	021072			PERFORM LOAD.MODE	: #SET BAUD RATE REGISTER.
012008	072000				<BIT14+BIT13+BIT12>+BIT10	
012010						: #9600 BAUD.
012012	000400			615:	BR 615	: #CONTINUE TEST.
012014	005277	167336			INC DVSCR	: SET MICRO CPU GC
012016	005005				CLR R5	: DELAY
012018	005777	167330		65:	TST DVSCR	: WAITING
012020	100404				BMI 75	: FOR
012022	104414				DELAY	
012024	005205				INC R5	: SILO
012026	001372				BNE 65	: ENTRY
012028	104000				HLT 0	: NO SILO ENTRY
012030	017704	167332		75:	MOV DVNSR, R4	: READ NSR
012032	010005				MOV R0, R5	: LOAD LINE NO
012034	052705	101000			BIS #BIT15+BIT9, R5	: SET SILO ENTRY, ALTERNATE NXM
012036	020504				CMP R5, R4	: NSR OK?
012038	001401				BEG 85	
012040	104002				HLT 2	: ALTERNATE BA NXM FAILED
012042	104401			85:	SCOPI	: SW09=1?
012044	012737	012074	001220		MOV #95, LOCK	: SET SCOPE LOOP
012046	104412			95:	MSTCLR	: INIT DVI
012048	010077	167270			MOV R0, DVSR5	: LOAD LINE NUMBER
012050	052777	000060	167252		BIS #BITS+BIT4, DVSCR	
012052	004537	021026			PERFORM SETREG	: SET EA BITS
012054	010	000			.BYTE 010, 000	: TX CNTRL TABLE, PRINCIPLE BA
012056	177320				177320	: NXM [2ND KE11]
012058	021350				TXBAP	: BA
012060	004537	021026			PERFORM SETREG	
012062	013	001			.BYTE 013, 001	: LINE STATE, PRINCIPLE BC
012064	000004				BIT2	: TX GO
012066	177777				-1	: ONE XFR
012068	032737	004000	001236		BIT #ASYNC, STAT	: #IS THIS ASYNC LINE CARD?
012070	001407				BEG 625	: #BR IF NO.
012072	004537	021072			PERFORM LOAD.MODE	
012074	015000				<BIT12+BIT11>+BIT9	: #8 BITS/PER/CHAR
012076	004537	021072			PERFORM LOAD.MODE	: #SET BAUD RATE REGISTER.
012078	072000				<BIT14+BIT13+BIT12>+BIT10	
012080						: #9600 BAUD.
012082	000400				BR 625	: #CONTINUE TEST.

012162	005277	167174	62\$:	INC	ADVSCR	:SET MICRO CPU GO
012166	005005			CLR	R5	:DELAY
012170	005777	167166	10\$:	TST	ADVSCR	:FOR
012174	100404			BMI	11\$:SILO
012176	104414			DELAY		
012200	005205			INC	R5	:ENTRY
012202	001372			BNE	10\$	
012204	104000			HLT	0	:NO SILO ENTRY
012206	017704	167170	11\$:	MOV	ADVNSR,R4	:READ NSR
012212	010005			MOV	R0,R5	:LOAD LINE NUMBER
012214	052705	104000		BIS	#BIT15+BIT11,R5	:SET SILO ENTRY, CNTRL TABLE NXM
012220	020504			CMP	R5,R4	:NSR OK?
012222	001401			BEQ	12\$:YES
012224	104002			HLT	2	:CNTRL TABLE NXM FAILED
012226	104401		12\$:	SCOPE		:SW09=1
012230	005200			INC	R0	:UPDATE LINE NO.
012232	005302			DEC	R2	:4 LINE GROUP DONE
012234	001402			BEQ	16	:BR IF YES
012236	000137	011566		JMP	1\$:JMP IF NO.
012242	000207			RTS	PC	:EXIT FOR NEXT GROUP OF LINES

***** TEST 6 *****
 : *TEST OF TRANSMITTER BCC OPERATIONS
 : *TEST THAT THE CHAR "25" WILL
 : *BE INCLUDED INTO THE BCC
 : *THE POLY USED WILL BE LRCB
 : *THIS TEST IS EXERCISED FOR BOTH ASYNC AND SYNC LINE CARDS.
 : *****

: TEST 6

012244	012737	000006	001226	157\$:	MOV	#6,TSTNO	
012252	012737	012610	001216		MOV	#TST7,NEXT	
012260	012700	000000			MOV	#0,R0	:PLACE LINE NUMBER INTO R0
012264	013737	001416	001236		MOV	LO0.03,STAT	:LOAD LINE CARD STATUS INTO STAT
012272	100402				BMI	100\$:BR IF LINE CARD NOT TO BE TESTED
012274	004737	012362			JSR	PC,105\$:GO DO THE TEST FOR LINE CARD 1
012300	012700	000004		100\$:	MOV	#4,R0	:PLACE LINE NUMBER INTO R0
012304	013737	001420	001236		MOV	LO4.07,STAT	:LOAD LINE CARD STATUS INTO STAT
012312	100402				BMI	101\$:BR IF LINE CARD NOT TO BE TESTED
012314	004737	012362			JSR	PC,105\$:GO DO THE TEST FOR LINE CARD 2
012320	012700	000010		101\$:	MOV	#8,R0	:LOAD LINE NUMBER
012324	013737	001422	001236		MOV	LO8.11,STAT	:LOAD LINE CARD STATUS INTO STAT
012332	100402				BMI	102\$:BR IF LINE CARD NOT TO BE TESTED
012334	004737	012362			JSR	PC,105\$:DO THE TEST FOR LINE CARD 3
012340	012700	000014		102\$:	MOV	#12,R0	:LOAD LINE NO.
012344	013737	001424	001236		MOV	L12.15,STAT	:LOAD LINE CARD STATUS
012352	100402				BMI	103\$:BR IF LINE CARD NOT TO BE TESTED
012354	004737	012362			JSR	PC,105\$:DO THE TESTS FOR LINE CARD 4
012360	104400			103\$:	SCOPE		:SCOPE THIS TEST.
012362				105\$:			:TEST ENTRANCE.
012362	104413				RAMCLR		:CLEAR ALL SEC REGISTERS
012364	012737	000200	021020		MOV	#LRCB,XPOLY	:SET SOFTWARE POLYNOMIAL
012372	012705	000025			MOV	#25,R5	:SET DATA CHAR
012376	110537	021050			MOVB	R5,1XBAP	:LOAD DATA

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DZDVCC-C MACY11 270732 17-SEP-76 11:40
 DZDVCC.P11 DV11 DEVICE DIAGNOSTICS.

PAGE 50
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2351	012402	112765	000010	022350		MOV B #BIT3, TXTAB(R5) ; SET CNTRL BYTE
2352	012410	012702	000004			MOV #4, R2 ; SET FOR 4 LINE GROUP
2353	012414	010077	166652		1\$:	MOV R0, DVSR5 ; LOAD LINE NO.
2354	012420	004537	021026			PERFORM SETREG
2355	012424	000	001			.BYTE 000,001 ; PRINCIPLE BA, BC
2356	012426	021350				TXBAP
2357	012430	117777				-1
2358	012432	004537	021026			PERFORM SETREG
2359	012436	013	010			.BYTE 013,010 ; LINE STATE, CNTRL TABLE
2360	012440	000004				BIT2 ; TXGO
2361	012442	022350				TXTAB ; TABLE
2362	012444	004537	021026			PERFORM SETREG
2363	012450	006	012			.BYTE 006,012 ; TX BCC REG. LINE PROTOCOL
2364	012452	000037				37 ; BCC
2365	012454	000000				0 ; POLYNOMIAL SELECT
2366	012456	032737	004000	001236		BIT #ASYNC, STAT ; #IS THIS ASYNC LINE CARD?
2367	012464	001407				BEQ 60\$; #BR IF NO.
2368	012466	004537	021072			PERFORM LOAD.MODE ; #
2369	012472	015000				<BIT12+BIT11>+BIT9 ; #8 BITS/PER/CHAR
2370	012474	004537	021072			PERFORM LOAD.MODE ; #SET BAUD RATE REGISTER.
2371	012500	072000				<BIT14+BIT13+BIT12>+BIT10 ; #9600 BAUD.
2372	012502	000403				BR 61\$; #CONTINUE TEST.
2373	012504	004537	021072		60\$:	PERFORM LOAD.MODE ; LOAD
2374	012510	014000				BIT12+BIT11 ; MODE
2375	012512	005277	166644		61\$:	INC DVSCR ; SET MICRO CODE GO
2376	012516	005005				CLR R5 ; DELAY
2377	012520	005777	166636		2\$:	TST DVSCR ; FOR
2378	012524	100403				BMI 3\$; SILO
2379	012526	104414				DELAY ; WASTE TIME
2380	012530	005205				INC R5 ; ENTRY
2381	012532	001372				BNE 2\$
2382	012534	112777	000006	166632	3\$:	MOV B #6, DVSR5H ; SEL BCC REGISTER
2383	012542	017704	166630			MOV DVSR4, R4 ; READ DVSR4 (BCC REG)
2384	012546	004537	020646			JSR R5, SIMBCC ; GO GET SOFTWARE BCC RESULT
2385	012552	000010				8. ; SHIFTS
2386	012554	000025				25 ; DATA
2387	012556	000037				37 ; PREVIOUS BCC RESULTS
2388	012560	013705	021024			MOV CALBCC, R5 ; READ SOFTWARE BCC RESULTS
2389	012564	117701	166604			MOV DVSR5H, R1 ; SET SEC REG POINTER
2390	012570	020504				CMP R5, R4 ; SOFTWARE=HWWARE?
2391	012572	001401				BEQ 4\$; #BR IF YES
2392	012574	104003				HLT 3 ; #RDWARE BCC WRONG
2393	012576	104412			4\$:	MSTCLR ; INIT DV11
2394	012600	005200				INC R0 ; UPDATE LINE NO.
2395	012602	005302				DEC R2 ; 4 LINE GROUP DONE?
2396	012604	001303				BNE 1\$; #BR IF NO
2397	012606	000207				RTS PC ; EXIT FOR NEXT 4 LINE GROUP

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;***** TEST 7 *****
; *TEST OF TRANSMITTER BCC OPERATIONS
; *TEST THAT THE CHAR "25" WILL
; *BE INCLUDED INTO THE BCC
; *THE POLY USED WILL BE CRC16
; *THIS TEST IS EXERCISED FOR BOTH ASYNC AND SYNC LINE CARDS.

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012610 012737 000007 001226
012616 012737 013154 001216
012624 012700 000000
012630 013737 001416 001236
012636 100402
012640 004737 012726
012644 012700 000004
012650 013737 001420 001236
012656 100402
012660 004737 012726
012664 012700 000010
012670 013737 001422 001236
012676 100402
012700 004737 012726
012704 012700 000014
012710 013737 001424 001236
012716 100402
012720 004737 012726
012724 104400
012726 104413
012730 012737 120001 021020
012736 012705 000025
012742 110537 021350
012746 112765 000010 022350
012754 012702 000004
012760 010077 166406
012764 004537 021026
012770 000 001
012772 021350
012774 177777
012776 004537 021026
013002 013 010
013004 000004
013006 022350
013010 004537 021026
013014 006 012
013016 000037
013020 000010
013022 032737 004000 001236
013030 001407
013032 004537 021072
013036 015000
013040 004537 021072
013044 072000
013046 000403
013050 004537 021072
013054 014000
013056 005277 166300
013062 005005
013064 005777 166272

: TEST 7

TST7: MOV #7,TSTNO
MOV #TST.C,NEXT
MOV #0,R0
MOV L00.03,STAT
BMI 100\$
JSR PC,105\$
100\$: MOV #4,R0
MOV L04.07,STAT
BMI 101\$
JSR PC,105\$
101\$: MOV #8,R0
MOV L08.11,STAT
BMI 102\$
JSR PC,105\$
102\$: MOV #12,R0
MOV L12.15,STAT
BMI 103\$
JSR PC,105\$
103\$: SCOPE
105\$:
RAMCLR
MOV #CRC16,XPOLY
MOV #25,R5
MOVB R5,TXBAP
MOVB #BIT3,XTAB(R5)
MOV #4,R2
1\$: MOV R0,ADVSR5
PERFORM SETREG
.BYTE 000,001
TXBAP
-1
PERFORM SETREG
.BYTE 013,010
BIT2
TXTAB
PERFORM SETREG
.BYTE 006,012
37
BIT3
BIT #ASYNC,STAT
BEQ 60\$
PERFORM LOAD.MODE
<BIT12+BIT11>+BIT9
PERFORM LOAD.MODE
<BIT14+BIT13+BIT12>+BIT10
BR 61\$
60\$: PERFORM LOAD.MODE
BIT12+BIT11
61\$: INC ADVSCR
CLR R5
2\$: TST ADVSCR

:PLACE LINE NUMBER INTO R0
:LOAD LINE CARD STATUS INTO STAT
:BR IF LINE CARD NOT TO BE TESTED
:GO DO THE TEST FOR LINE CARD 1
:PLACE LINE NUMBER INTO R0
:LOAD LINE CARD STATUS INTO STAT
:BR IF LINE CARD NOT TO BE TESTED
:GO DO THE TEST FOR LINE CARD 2
:LOAD LINE NUMBER
:LOAD LINE CARD STATUS INTO STAT
:BR IF LINE CARD NOT TO BE TESTED
:DO THE TEST FOR LINE CARD 3
:LOAD LINE NO.
:LOAD LINE CARD STATUS
:BR IF LINE CARD NOT TO BE TESTED
:DO THE TESTS FOR LINE CARD 4
:SCOPE THIS TEST.
:TEST ENTRANCE.
:CLEAR ALL SEC REGISTERS
:SET SOFTWARE POLYNOMIAL
:SET DATA CHAR
:LOAD DATA
:SET CNTRL BYTE
:SET FOR 4 LINE GROUP
:LOAD LINE NO.
:PRINCIPLE BA, BC
:LINE STATE, CNTRL TABLE
:TXGO
:TABLE
:TX BCC REG, LINE PROTOCOL
:BCC
:POLYNOMIAL SELECT
:#IS THIS ASYNC LINE CARD?
:#BR IF NO.
:#
:#8 BITS/PER/CHAR
:#SET BAUD RATE REGISTER.
:#9600 BAUD.
:#CONTINUE TEST.
:LOAD
:MODE
:SET MICRO CODE GC
:DELAY
:FJR

2463	013070	100403			BMI	3\$:SILO
2464	013072	104414			DELAY			:WASTE TIME
2465	013074	005205			INC	R5		:ENTRY
2466	013076	001372			BNE	2\$		
2467	013100	112777	000006	166266	3\$:	MOVB	#6, QDVSRSH	:SEL BCC REGISTER
2468	013106	017704	166264		MOV	QDVSR, R4		:READ DVSRA (BCC REG)
2469	013112	004537	020646		JSR	R5, SIMBCC		:GO GET SOFTWARE BCC RESULT
2470	013116	000010			8.			:SHIFTS
2471	013120	000025			25			:DATA
2472	013122	000037			37			:PREVIOUS BCC RESULTS
2473	013124	013705	021024		MOV	CALBCC, R5		:READ SOFTWARE BCC RESULTS
2474	013130	117701	166240		MOVB	QDVSRSH, R1		:SET SEC REG POINTER
2475	013134	020504			CMP	R5, R4		:SOFTWARE=HWWARE?
2476	013136	001401			BEQ	4\$:BR IF YES
2477	013140	104003			HLT	3		:HWWARE BCC WRONG
2478	013142	104412			4\$:	MSTCLR		:INIT DV11
2479	013144	005200			INC	R0		:UPDATE LINE NO.
2480	013146	005302			DEC	R2		:4 LINE GROUP DONE?
2481	013150	001303			BNE	1\$:BR IF NO
2482	013152	000207			RTS	PC		:EXIT FOR NEXT 4 LINE GROUP

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:***** TEST 10 *****
:*TEST OF TRANSMITTER BCC OPERATIONS
:*TEST THAT THE CHAR "25" WILL
:*BE INCLUDED INTO THE BCC
:*THE POLY USED WILL BE CRC.CCITT
:*THIS TEST IS EXERCISED FOR BOTH ASYNC AND SYNC LINE CARDS.
:*****

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; TEST 10

2495	013154	012737	000010	001226	TST10:	MOV	#10, TSTNO	
2496	013162	012737	013520	001216		MOV	#TST11, NEXT	
2497	013170	012700	000000			MOV	#0, R0	:PLACE LINE NUMBER INTO R0
2498	013174	013737	001416	001236		MOV	LO0.03, STAT	:LOAD LINE CARD STATUS INTO STAT
2499	013202	100402				BMI	100\$:BR IF LINE CARD NOT TO BE TESTED
2500	013204	004737	013272			JSR	PC, 105\$:GO DO THE TEST FOR LINE CARD 1
2501	013210	012700	000004		100\$:	MOV	#4, R0	:PLACE LINE NUMBER INTO R0
2502	013214	013737	001420	001236		MOV	LO4.07, STAT	:LOAD LINE CARD STATUS INTO STAT
2503	013222	100402				BMI	101\$:BR IF LINE CARD NOT TO BE TESTED
2504	013224	004737	013272			JSR	PC, 105\$:GO DO THE TEST FOR LINE CARD 2
2505	013230	012700	000010		101\$:	MOV	#8, R0	:LOAD LINE NUMBER
2506	013234	013737	001422	001236		MOV	LO8.11, STAT	:LOAD LINE CARD STATUS INTO STAT
2507	013242	100402				BMI	102\$:BR IF LINE CARD NOT TO BE TESTED
2508	013244	004737	013272			JSR	PC, 105\$:DO THE TEST FOR LINE CARD 3
2509	013250	012700	000014		102\$:	MOV	#12, R0	:LOAD LINE NO.
2510	013254	013737	001424	001236		MOV	L12.15, STAT	:LOAD LINE CARD STATUS
2511	013262	100402				BMI	103\$:BR IF LINE CARD NOT TO BE TESTED
2512	013264	004737	013272			JSR	PC, 105\$:DO THE TESTS FOR LINE CARD 4
2513	013270	104400			103\$:	SCOPE		:SCOPE THIS TEST.
2514	013272				105\$:			:TEST ENTRANCE.
2515	013272	104413				RAMCLR		:CLEAR ALL SEC REGISTERS
2516	013274	012737	102010	021020		MOV	#CRC.CCITT, XPOLY	:SET SOFTWARE POLYNOMIAL
2517	013302	012705	000025			MOV	#25, R5	:SET DATA CHAR
2518	013306	110537	021350			MOVB	R5, TXBAP	:LOAD DATA

M04

2519	013312	112765	000010	022350		MOVB	#BIT3,TXTAB(R5)	:	SET CNTRL BYTE
2520	013320	012702	000004			MOV	#4,R2	:	SET FOR 4 LINE GROUP
2521	013324	010077	166042		1\$:	MOV	RO,ADVSR5	:	LOAD LINE NO.
2522	013330	004537	021026			PERFORM	SETREG	:	
2523	013334	000	001			.BYTE	000,001	:	PRINCIPLE BA, BC
2524	013336	021350				TXBAP		:	
2525	013340	177777				-1		:	
2526	013342	004537	021026			PERFORM	SETREG	:	
2527	013346	013	010			.BYTE	013,010	:	LINE STATE, CNTRL TABLE
2528	013350	000004				BIT2		:	TXGO
2529	013352	022350				TXTAB		:	TABLE
2530	013354	004537	021026			PERFORM	SETREG	:	
2531	013350	006	012			.BYTE	006,012	:	TX BCC REG, LINE PROTOCOL
2532	013362	000037				37		:	BCC
2533	013364	000030				BIT4+BIT3		:	POLYNOMIAL SELECT
2534	013366	032737	004000	001236		BIT	#ASYNC,STAT	:	#IS THIS ASYNC LINE CARD?
2535	013374	001407				BEQ	60\$:	#BR IF NO.
2536	013376	004537	021072			PERFORM	LOAD.MODE	:	#
2537	013402	015000				<BIT12+BIT11>+BIT9		:	#8 BITS/PER/CHAR
2538	013404	004537	021072			PERFORM	LOAD.MODE	:	#SET BAUD RATE REGISTER.
2539	013410	072000				<BIT14+BIT13+BIT12>+BIT10		:	#9600 BAUD.
2540								:	#CONTINUE TEST.
2541	013412	000403				BR	61\$:	
2542	013414	004537	021072		60\$:	PERFORM	LOAD.MODE	:	LOAD
2543	013420	014000				BIT12+BIT11		:	MODE
2544	013422	005277	165734		61\$:	INC	ADVSCR	:	SET MICRO CODE GO
2545	013426	005005				CLR	R5	:	DELAY
2546	013430	005777	165726		2\$:	TST	ADVSCR	:	FOR
2547	013434	100403				BMI	3\$:	SILO
2548	013436	104414				DELAY		:	WASTE TIME
2549	013440	005205				INC	R5	:	ENTRY
2550	013442	001372				BNE	2\$:	
2551	013444	112777	000006	165722	3\$:	MOVB	#6,ADVSR5H	:	SEL BCC REGISTER
2552	013452	017704	165720			MOV	ADVSR5,R4	:	READ DVSR5 (BCC REG)
2553	013456	004537	020646			JSR	R5,SIMBCC	:	GO GET SOFTWARE BCC RESULT
2554	013462	000010				8.		:	SHIFTS
2555	013464	000025				25		:	DATA
2556	013466	000037				37		:	PREVIOUS BCC RESULTS
2557	013470	013705	021024			MOV	CALBCC,R5	:	READ SOFTWARE BCC RESULTS
2558	013474	117701	165674			MOVB	ADVSR5H,R1	:	SET SEC REG POINTER
2559	013500	020504				CMP	R5,R4	:	SOFTWARE=HWWARE?
2560	013502	001401				BEQ	4\$:	BR IF YES
2561	013504	104003				HLT	3	:	HWWARE BCC WRONG
2562	013506	104412			4\$:	MSTCLR		:	INIT DV11
2563	013510	005200				INC	RO	:	UPDATE LINE NO.
2564	013512	005302				DEC	R2	:	4 LINE GROUP DONE?
2565	013514	001303				BNE	1\$:	BR IF NO
2566	013516	000207				RTS	PC	:	EXIT FOR NEXT 4 LINE GROUP
2567								:	
2568								:	
2569								:	
2570								:	
2571								:	
2572								:	
2573								:	
2574								:	

***** TEST 11 *****
 ;*TEST OF TRANSMITTER BCC OPERATIONS
 ;*TEST THAT THE CHAR "25" WILL
 ;*WILL SEND THE BCC.
 ;*THE POLY USED WILL BE CRC.CCITT
 ;*THIS TEST IS EXERCISED FOR BOTH ASYNC AND SYNC LINE CARDS.

NO4

DZDVC-C MACY11 27(732) 17-SEP-75 11:40
 DZDVCC.P11 DV11 DEVICE DIAGNOSTICS.

PAGE 54
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:*****

```

2575
2576
2577
2578
2579 013520 012737 000011 001226
2580 013526 012737 014064 001216
2581 013534 012700 000000
2582 013540 013737 001416 001236
2583 013546 100402
2584 013550 004737 013636
2585 013554 012700 000004
2586 013560 013737 001420 001236
2587 013566 100402
2588 013570 004737 013636
2589 013574 012700 000010
2590 013600 013737 001422 001236
2591 013606 100402
2592 013610 004737 013636
2593 013614 012700 000014
2594 013620 013737 001424 001236
2595 013626 100402
2596 013630 004737 013636
2597 013634 104400
2598 013636
2599 013636 104413
2600 013640 012737 102010 021020
2601 013646 012705 000025
2602 013652 110537 021350
2603 013656 112765 000004 022350
2604 013664 012702 000004
2605 013670 010077 165476
2606 013674 004537 021026
2607 013700 000 001
2608 013702 021350
2609 013704 177777
2610 013706 004537 021026
2611 013712 013 010
2612 013714 000004
2613 013716 022350
2614 013720 004537 021026
2615 013724 006 012
2616 013726 000037
2617 013730 000030
2618 013732 032737 004000 001236
2619 013740 001407
2620 013742 004537 021072
2621 013746 015000
2622 013750 004537 021072
2623 013754 072000
2624
2625 013756 000403
2626 013760 004537 021072
2627 013764 014000
2628 013766 005277 165370
2629 013772 005005
2630 013774 005777 165362
  
```

```

; TEST 11
-----
TST11: MOV #11,TSTNO
MOV #TST12,NEXT
MOV #0,R0 ;PLACE LINE NUMBER INTO R0
MOV LO0.03,STAT ;LOAD LINE CARD STATUS INTO STAT
BMI 100$ ;BR IF LINE CARD NOT TO BE TESTED
JSR PC,105$ ;GO DO THE TEST FOR LINE CARD 1
100$: MOV #4,R0 ;PLACE LINE NUMBER INTO R0
MOV LO4.07,STAT ;LOAD LINE CARD STATUS INTO STAT
BMI 101$ ;BR IF LINE CARD NOT TO BE TESTED
JSR PC,105$ ;GO DO THE TEST FOR LINE CARD 2
101$: MOV #8,R0 ;LOAD LINE NUMBER
MOV LO8.11,STAT ;LOAD LINE CARD STATUS INTO STAT
BMI 102$ ;BR IF LINE CARD NOT TO BE TESTED
JSR PC,105$ ;DO THE TEST FOR LINE CARD 3
102$: MOV #12,R0 ;LOAD LINE NO.
MOV LO12.15,STAT ;LOAD LINE CARD STATUS
BMI 103$ ;BR IF LINE CARD NOT TO BE TESTED
JSR PC,105$ ;DO THE TESTS FOR LINE CARD 4
103$: SCOPE ;SCOPE THIS TEST.
105$: ;TEST ENTRANCE.
RAMCLR ;CLEAR ALL SEC REGISTERS
MOV #CRC.CCITT,XPOLY ;SET SOFTWARE POLYNOMINAL
MOV #25,R5 ;SET DATA CHAR
MOVB R5,TXBAP ;LOAD DATA
MOVB #BIT2,XTAB(R5) ;SET CNTRL BYTE
MOV #4,R2 ;SET FOR 4 LINE GROUP
1$: MOV R0,ADVSR5 ;LOAD LINE NO.
PERFORM SETREG ;PRINCIPLE BA, BC
.BYTE 000,001
TXBAP
-1
PERFORM SETREG
.BYTE 013,010 ;LINE STATE, CNTRL TABLE
BIT2 ;TXGO
XTAB ;TABLE
PERFORM SETREG
.BYTE 006,012 ;TX BCC REG, LINE PROTOCOL
37 ;BCC
BIT4+BIT3 ;POLYNOMIAL SELECT
BIT #ASYNC,STAT ;#IS THIS ASYNC LINE CARD?
BEQ 60$ ;#BR IF NO.
PERFORM LOAD.MODE ;#
<BIT12+BIT11>+BIT9 ;#8 BITS/PER/CHAR
PERFORM LOAD.MODE ;#SET BAUD RATE REGISTER.
<BIT14+BIT13+BIT12>+BIT10 ;#9600 BAUD.
60$: BR 61$ ;#CONTINUE TEST.
PERFORM LOAD.MODE ;LOAD
BIT12+BIT11 ;MODE
61$: INC ADVSCR ;SET MICRO CODE 30
CLR R5 ;DELAY
2$: TST ADVSCR ;FOR
  
```


C05

```

004537 021026
021350 001
021350
177777
004537 021026
010 013
022250
000004
005007 022350
005007 021350
032777 004000 001236
001401
004537 021072
015000
004537 021072
072000

014274 000403
014276 004537 021072
014300 014000
014304 005277 165052
014310 012703 000077
014314 112777 000013 165052
014318 032777 000004 165046
014322 001402
014326 104414

014330 000767
014334 032777 002000 165016
014338 001401
014342 104000
014346 005303
014350 001414
004537 021026
000 001
021350
177777
014366 112777 000013 165022
014370 012777 000004 164774
014374 000744
014378 004537 021026
001 013
014382 177777
014386 000004
014390 112777 000013 164750
014394 032777 000004 164744
014398 001402
014402 104414

014406 000767
014410 012704 000010
014414 104414
014418 005304
014422 001375
014426 013701 001362
014430 011101

```

```

PERFORM SETREG
.BYTE 000,001
TXBAP
TX BA P, TX BC P

-1
PERFORM SETREG
.BYTE 010,013
TXTAB
TX CNTRL TABLE, LINE STATE

BIT2
TX GO
CLR TXTAB
CLEAR CNTRL BYTE
CLR TXBAP
CLEAR TX DATA
BIT #ASYNC,STAT
IS THIS ASYNC LINE CARD?
BEQ 60$
BR IF NO.

PERFORM LOAD.MODE
<BIT12+BIT11>+BIT9
PERFORM LOAD.MODE
<BIT14+BIT13+BIT12>+BIT10
BR 61$
PERFORM LOAD.MODE
BIT12+BIT11
MODE
INC 3DVSCR
SET MICRO CPL GO
MOV #63, R3
SET FOR 63 ENTRIES INTO SILO
MOVB #13, 3DVSRSH
SEL LINE STATE
BIT #BIT2, 3DVSR
IS TX GO SET?
BEQ 3$
BR IF NO
DELAY
GIVE UCPU TIME
TO ACCESS REG

BR 2$
BIT #BIT10, 3DVSCR
LOOK AGAIN
BEQ +4
CID SILO FULL SET?
HLT 0
BR IF NO
SILO FULL SET TOO SOON
DEC R3
63 ENTRIES MADE?
BEQ 4$
BR IF NO
PERFORM SETREG
.BYTE 000,001
TXBAP TXBCP
RELOAD BA
BC

MOVB #13, 3DVSRSH
SEL LINE STATE
MOV #BIT2, 3DVSR
CLEAR "USE SEC. TABLE" SET TX GO
BR 2$
CONTINUE

PERFORM SETREG
.BYTE 001,013
TX BC, LINE STATE
-1
SET FOR 64TH ENTRY
BIT2
TX GO
MOVB #13, 3DVSRSH
SEL LINE STATE
BIT #BIT2, 3DVSR
TX GO SET?
BEQ 5$
BR IF NO
DELAY
GIVE UCPU TIME
TO ACCESS REG
CONTINUE

BR 6$
MOV #10, R4
DELAY
R4
DEC -4
BNE
MOV DVSCR, R1
SET POINTER
MOV R1, R4
READ DVSCR

```


E05

2799 014622 000240 04500
2800 014624 004537 04600
2801 014630 000 04700
2802 014632 000001 04900
2803 014634 177750 04900
2804 014636 004537 05000
2805 014642 010 05100
2806 014644 022350 05200
2807 014646 000004 05300
2808 014650 005202 05400
2809 014652 005200 05500
2810 014654 022700 05600
2811 014656 001351 05700
2812 014658 005005 05800
2813 014664 005037 05900
2814 014670 012700 06000
2815 014672 012704 06100
2816 014700 005020 06200
2817 014702 005024 06300
2818 014704 022700 06400
2819 014710 001373 06500
2820 014712 005277 06600
2821 014716 012702 164444
2822 014722 005777 021242
2823 014726 100005 164434
2824 014730 017722 164446
2825 014734 005337 025540
2826 014740 001404
2827 014742 104414
2828 014744 005205
2829 014746 001365
2830 014750 104000
2831 014752
2832 014752 005737 001416 06800
2833 014756 100403 06900
2834 014760 004537 020054 07000
2835 014764 000000 07100
2836 014766 005737 001420 07200
2837 014772 100403 07300
2838 014774 004537 020054 07400
2839 015000 000004 07500
2840 015002 005737 001422 07600
2841 015006 100403 07700
2842 015010 004537 020054 07800
2843 015014 000010 07900
2844 015016 005737 001424 08000
2845 015022 100403 08100
2846 015024 004537 020054 08200
2847 015030 000014 08300
2848 015032 104400 08400
2849 08500
2850 08700
2851 08900
2852 08900
2853 08900
2854 09000

NOP ;
PERFORM SETREG
.BYTE 000,001
.BLKW 1
-30
PERFORM SETREG
.BYTE 010,013
TXTAB
BIT2
INC R2
INC R0
CMP #16.,R0
BNE 5\$
CLR R5
CLR TXTAB
MOV #TXBAP,R0
MOV #TXBAS,R4
CLR (R0)+
CLR (R4)+
CMP #TXBAP+50,R0
BNE -10
INC 00VSCR
MOV #REGBUF,R2
TST 00VSCR
BPL 9\$
MOV 00VNSR,(R2)+
DEC COUNT
BEQ 10\$
DELAY
INC R5
BNE 8\$
HLT 0
TST L00.03
BMI 27\$
JSR R5,LINT1
C.
TST L04.07
BMI 28\$
JSR R5,LINT1
4.
TST L08.11
BMI 29\$
JSR R5,LINT1
8.
TST L12.15
BMI 30\$
JSR R5,LINT1
12.
SCOPE

:TX BA P, TX BC P
:TXBA
:TXBC
:TX CNTRL TAB, LINE STATE
:TX GO
:UPDATE BA POINTER
:UPDATE LINE NO.
:ALL LINES DONE?
:BR IF NO
:CLEAR CNTRL TABLE (1.0)
:PRINCIPLE POINTER
:ALTERNATE POINTER
:CLEAR
:TX BUFFERS
:ALL DONE
:BR IF NO
:SET UCPU GC
:SET BUFFER POINTER IN R2
:SILO ENTRY?
:BR IF NO
:STORE SILO ENTRY AWAY
:ALL ENTRIES MADE?
:BR IF YES
:WASTE TIME
:COUNT WAIT
:FOR SILO ENTRY
:NO SILO ENTRY! (0VSCR)=1.
:LINE CARD 1 EXIST?
:BR IF NO
:GOSUB
:LINES 00-03
:LINE CARD 2 EXIST?
:BR IF NO
:GOSUB
:LINES 04-07
:LINE CARD 3 EXIST?
:BR IF NO
:GOSUB
:LINES 08-11
:LINE CARD 4 EXIST?
:BR IF NO
:GOSUB
:LINES 12-15
:SCOPE TEST

:***** TEST 14 *****
:*TEST TO TURN ON ALL
:*AVAILABLE TRANSMITTERS AT THE SAME TIME.
:*30(8) CHARS WILL BE XMITTED.
:*EXPECTED:

F05

```

09100
09200
09300
09400
09500
09600
09700
09800
09900
10000
10100
10200
10205
10400
015034 012737 000014 001226
015042 012737 015400 001216
015050 104413
015052 005001
015054 012700 000004
015060 005737 001416
015064 100401
015066 060001
015070 005737 001420
015074 100401
015076 060001
015100 005737 001422
015104 100401
015106 060001
015110 005737 001424
015114 100401
015116 060001
015120 005000
015122 010137 025540
015126 012737 021350 015172 10700
015134 012737 021750 015216 10800
015142 105077 000024 10900
015146 105077 000044 11000
015152 010077 164214 11100
015156 000240 11200
015160 000240 11300
015162 000240 11400
015164 004537 021026 11500
015170 000 001 11600
015172 000001 11700
015174 177750 11800
015176 004537 021026 11900
015202 010 013 12000
015204 022350 12100
015206 000004 12200
015210 004537 021026 12300
015214 002 003 12400
015216 000001 12500
015220 177750 12600
  
```

```

:*1)NUMBER OF LINES PRESENT Y2 ENTRIES INTO DVNSR
:*2)ALL TXBAP = TXBPA+30+LINE NO.
:*3)ALL TXWCP = 0
:*4)ALL LINE STATE REGS =0
:*5)PRIMARY ENTRY IN DVNSR = BIT15+BIT8+LINE NO.
:*6)SECONDARY ENTRY IN DVNSR =BIT15+BIT9+BIT8+LINE NO.
:*7)ALL TX BAS = TXBAS+30+LINE NO.
:*8) ALL TXWCS =0
:*
:*NOTE: PRIMARY REGISTERS ARE USED FIRST; AND THEN THE SECONDARY.
:*NOTE:TURN AROUND CONNECTOR MUST BE INSTALLED
:* AND THE 'EIA' GATES ARE USED.
:*THIS TEST IS DONE FOR BOTH ASYNC AND SYNC LINE CARDS.
:*****
  
```

: TEST 14

```

-----
TST14: MOV #14,TSTNO
MOV #TST15,NEXT
RAMCLR ;ZERO ALL SEC REGISTERS
CLR R1 ;SET COUNTER TO ZERO
MOV #4,R0 ;SET 4 LINE COUNT
TST L00.C3 ;LINE CARD 1 EXIST?
BMI 1$ ;BR IF NO
ADD R0,R1 ;UPDATE COUNT
TST L04.07 ;LINE CARD 2 EXIST?
BMI 2$ ;BR IF NO
ADD R0,R1
TST L08.11 ;LINE CARD 3 EXIST?
BMI 3$ ;BR IF NO
ADD R0,R1
TST L12.15 ;LINE CARD 4 EXIST?
BMI 4$ ;BR IF NO
ADD R0,R1
CLR R0 ;SET POINTER TO 0
MOV R1,COUNT ;STORE LINE CARD COUNT
MOV #TXBAP,6$ ;SET TX BA POINTER
MOV #TXBAS,11$ ;SET ALTERNATE POINTER
5$: CLRB 06$ ;ZERO DATA
CLRB 011$ ;ZERO DATA
MOV R0,DVNSR ;LOAD LINE NUMBER
60$: NOP ;PERFORM LOAD.MODE
NOP ;BIT12+BIT11
61$: NOP
PERFORM ;SETREG
.BYTE 000,001 ;TX BA P, TX BC F
6$: .BLKW 1 ;TXBA
-30 ;TX BC
PERFORM ;SETREG
.BYTE 010,013 ;TX CNT TAB, LINE STATE
TXTAB ;TX GO
BIT2 ;TX BA (ALT), TX BC (ALT)
PERFORM ;SETREG
.BYTE 002,003 ;TX BA
11$: .BLKW 1 ;TX BA
-30 ;TX BC
  
```

G05

015222	005237	015216	12700
015226	005237	015172	12800
015232	005200		12900
015234	022700	000020	13000
015240	001340		13100
015242	005005		13200
015244	063737	025540	13300
015252	005037		13400
015256	005277		13500
015262	012702		
015266	005777		
015272	100005		
015274	017722	164102	
015300	005337	025540	
015304	001404		
015306	104414		
015310	005205		
015312	001365		
015314	104000		
015316			
015316	005737	001416	13700
015322	100403		13800
015324	004537	020316	13900
015330	000000		14000
015332	005737	001420	14100
015336	100403		14200
015340	004537	020316	14300
015344	000004		14400
015346	005737	001422	14500
015352	100403		14600
015354	004537	020316	14700
015360	000010		14800
015362	005737	001424	14900
015366	100403		15000
015370	004537	020316	15100
015374	000014		15200
015376	104400		15300
			15400

```

INC 11$ :UPDATE TX BA POINTER (ALT)
INC 6$ :UPDATE TX BA POINTER (P)
INC R0 :UPDATE LINE POINTER
CMP #16.,R0 :ALL LINES DONE?
SNE 5$ :BR IF NO
CLR R5
ADD COUNT,COUNT :DOUBLE THE COUNT (P+A)
CLR TXTAB :CLEAR CNTRL TABLE (1.0)
MOV #R0,R2 :SET UCPU GO
MOV #R0,R2 :SET BUFFER POINTER IN R2
TST #R0 :SILO ENTRY?
BPL 9$ :BR IF NO
MOV #R0,R2 :STORE SILO ENTRY AWAY
DEC COUNT :ALL ENTRIES MADE?
BEQ 10$ :BR IF YES
DELAY :WASTE TIME
INC R5 :COUNT WAIT
SNE 8$ :FOR SILO ENTRY
HLT 0 :NO SILO ENTRY! (OVSCRIS=1)

10$: TST LOC.03 :LINE CARD 1 EXIST?
BMI 27$ :BR IF NO
JSR R5,LINT2 :GOSUB
0. :LINES 00-03
27$: TST LOC.07 :LINE CARD 2 EXIST?
BMI 28$ :BR IF NO
JSR R5,LINT2 :GOSUB
4. :LINES 04-07
28$: TST LOC.11 :LINE CARD 5 EXIST?
BMI 29$ :BR IF NO
JSR R5,LINT2 :GOSUB
8. :LINES 08-11
29$: TST LOC.15 :LINE CARD 4 EXIST?
BMI 30$ :BR IF NO
JSR R5,LINT2 :GOSUB
12. :LINES 12-15
30$: SCOPE :SCOPE YES+

```

```

***** TEST 15 *****
: *TEST TO TURN ON ALL TRANSMITTER
: *BCC'S (USING LRC 8).
: *ALL TRANSMITTER PRIMARY REGISTERS
: *WILL XMIT 1 CHARACTER (20(8)+LINE NO.)
: *AT THIS TIME ALL BCC REGISTERS WILL BE
: *CHECKED FOR CORRECT DATA. (20(8)+LINE NO.)
: *NOTE: BCC INSTRUCTION HAS BEEN CHECKED AND
: *LRC 8 ALSO BUT IT IS NOT PROVEN
: *THAT THE CHAR HAS BEEN "TAKEN FROM" CORE BY THE MICRO-PROCESSOR YET.
: *NOTE: TURN AROUND CONNECTOR MUST BE INSTALLED
: * AND THE 'EIA' GATES ARE USED.
: *THIS TEST IS DONE FOR BOTH ASYNC AND SYNC LINE CARDS.
: *****

```

015400	012737	000015	001226
--------	--------	--------	--------

```

: TEST 15
-----
TST15: MOV #15,TSTNO

```

H05

000000-0 MACY11
000000.P11

27.7321 17-SEP-75 11:40
DV11 DEVICE DIAGNOSTICS.

PAGE 61
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Address	Hex	Hex	Hex	Hex	Instruction	Comment
015406	012737	015176	001216		MOV #TST16.NEXT	
015414	104413				RAMCLR	:ZERO ALL SEC REGISTERS
015416	005001				CLR R1	:SET COUNTER TO ZERO
015420	012700	003024			MOV #4,R0	:SET 4 LINE COUNT
015424	005737	001416			TST LOC.03	:LINE CARD 1 EXIST?
015428	100401				BMI 1\$:BR IF NO
015432	060001				ADD R0,R1	:UPDATE COUNT
015434	005737	001420		1\$:	TST LOC.07	:LINE CARD 2 EXIST?
015440	100401				BMI 2\$:BR IF NO
015442	060001				ADD R0,R1	
015444	005737	001422		2\$:	TST LOC.11	:LINE CARD 3 EXIST?
015450	100401				BMI 3\$:BR IF NO
015452	060001				ADD R0,R1	
015454	005737	001424		3\$:	TST LOC.15	:LINE CARD 4 EXIST?
015460	100401				BMI 4\$:BR IF NO
015462	060001				ADD R0,R1	
015464	005000			4\$:	CLR R0	:SET POINTER TO 0
015466	010137	025540			MOV R1,COUNT	:STORE LINE CARD COUNT
015472	012700	022350	17:00		MOV #TXTAB,R0	:SET CNTL TABLE POINTER
015476	012703	000020	17200		MOV #16,R3	:SET FOR 16 LINES
015502	062700	000020	17300		ADD #20,R0	:SET DATA CHAR
015506	112720	000010	17400	5\$:	MOV8 #BIT3,(R0)+	:INC BCC
015512	005303		17500		DEC R3	:16 X DONE?
015514	001374		17600		BNE 5\$:BR IF NO
015516	012702	000020	17700		MOV #20,R2	:SET DATA
015522	012700	021350	17800		MOV #TXBAP,R0	:SET TX BUFFER POINTER
015526	012703	000020	17900		MOV #16,R3	:16 LINES
015532	110220		18000	6\$:	MOV8 R2,(R0)+	:LOAD DATA
015534	005202		18100		INC R2	:UPDATE DATA
015536	005303		18200		DEC R3	:ALL DONE
015540	001374		18300		BNE 6\$:BR IF NO
015542	012737	021350	18400		MOV #TXBAP,8\$:SET POINTER
015550	005000		18500		CLR R0	:SET TO LINE 0.
015552	010077	153614	18500	7\$:	MOV R0,ADVSR5	:LOAD LINE NO.
015556	000240		18700	8\$:	NOP	:PERFORM LOAD.MODE
015560	000240		18800		NOP	
015562	000240		18900	9\$:	NOP	
015564	004537	021026	19000		PERFORM SETREG	
015570	000	001	19100		.BYTE 000,001	:TX BA P, TX BC P
015572	000001		19200	9\$:	.BLKW 1	:TX BA
015574	177777		19300		-1	:TX BC
015576	004537	021026	19400		PERFORM SETREG	
015602	010	012	19500		.BYTE 010,013	:TX CNTL TAB, LINE STATE
015604	022350		19600		TXTAB	
015606	000004		19700		BIT2	:TX GO
015610	005237	015572	19800		INC 8\$:UPDATE BA POINTER
015614	005200		19900		INC R0	:UPDATE LINE POINTER
015616	022700	000020	20000		CMP #16.,R0	:ALL DONE?
015622	001353		20100		BNE 7\$:BR IF NO
015624	005005		20200		CLR R5	
015626	005277	153530	20300		INC ADVSCR	:SET UCPU GO
015632	005777	163544	20400	9\$:	TST ADVNSR	:SILO ENTRY?
015636	100003		20500		BPL 11\$:BR IF NO
015640	005337	025540	20600		DEC COUNT	:ALL DONE?
015644	001404		20700		BEQ 10\$:BR IF NO
015646	104414		20800	11\$:	DELAY	:WASTE TIME

3023	015650	005205		20900		INC	R5	:UPCOUNT DELAY
3024	015652	001357		21000		BNE	9\$:BR
3025	015654	104000		21100		HLT	0	:DVNSR15 NOT=1 (NO SILO ENTRY)
3026	015656	042777	000001	163475	21200	BIC	#BIT0,ADVSCR	:CLEAR UCPU GO
3027								
3028	015664	005737	001416			TST	L00.03	:DOES LINE CARD EXIST?
3029	015670	100426				BMI	66\$:BR IF NO
3030	015672	012700	000000			MOV	#0,R0	:LOAD LINE POINTER
3031	015676	012702	000004			MOV	#4,R2	:SET FOR 4 LINE GROUP
3032	015702	010077	163464			MOV	R0,ADVSR5	:LOAD LINE NO.
3033	015706	112777	000006	163450		MOVB	#6,ADVSRSH	:SEL TX BCC REG
3034	015714	017704	163456			MOV	ADVSR4,R4	:READ IT
3035	015720	012705	000020			MOV	#20,R5	:SET EXPECTED=20
3036	015724	060005				ADD	R0,R5	:ADD LINE NO TO EXPECTED
3037	015726	117701	163442			MOVB	ADVSRSH,R1	:SET SEC REG POINTER
3038	015732	020504				CMP	R5,R4	:TX BCC OK?
3039	015734	001401				BEQ	65\$:BR IF YES
3040	015736	104003				HLT	3	:TX BCC ERROR
3041	015740	005200				INC	R0	:UPDATE LINE POINTER
3042	015742	005302				DEC	R2	:4 LINE DONE?
3043	015744	001356				BNE	64\$:BR IF NO
3044	015746							
3045								
3046	015746	005737	001420			TST	L04.07	:DOES LINE CARD EXIST?
3047	015752	100426				BMI	69\$:BR IF NO
3048	015754	012700	000004			MOV	#4,R0	:LOAD LINE POINTER
3049	015760	012702	000004			MOV	#4,R2	:SET FOR 4 LINE GROUP
3050	015764	010077	163402			MOV	R0,ADVSR5	:LOAD LINE NO.
3051	015770	112777	000006	163376		MOVB	#6,ADVSRSH	:SEL TX BCC REG
3052	015776	017704	163374			MOV	ADVSR4,R4	:READ IT
3053	016002	012705	000020			MOV	#20,R5	:SET EXPECTED=20
3054	016006	060005				ADD	R0,R5	:ADD LINE NO TO EXPECTED
3055	016010	117701	163360			MOVB	ADVSRSH,R1	:SET SEC REG POINTER
3056	016014	020504				CMP	R5,R4	:TX BCC OK?
3057	016016	001401				BEQ	68\$:BR IF YES
3058	016020	104003				HLT	3	:TX BCC ERROR
3059	016022	005200				INC	R0	:UPDATE LINE POINTER
3060	016024	005302				DEC	R2	:4 LINE DONE?
3061	016026	001356				BNE	67\$:BR IF NO
3062	016030							
3063								
3064	016030	005737	001422			TST	L08.11	:DOES LINE CARD EXIST?
3065	016034	100426				BMI	72\$:BR IF NO
3066	016036	012700	000010			MOV	#8,R0	:LOAD LINE POINTER
3067	016042	012702	000004			MOV	#4,R2	:SET FOR 4 LINE GROUP
3068	016046	010077	163320			MOV	R0,ADVSR5	:LOAD LINE NO.
3069	016052	112777	000006	163314		MOVB	#6,ADVSRSH	:SEL TX BCC REG
3070	016060	017704	163312			MOV	ADVSR4,R4	:READ IT
3071	016064	012705	000020			MOV	#20,R5	:SET EXPECTED=20
3072	016070	060005				ADD	R0,R5	:ADD LINE NO TO EXPECTED
3073	016072	117701	163276			MOVB	ADVSRSH,R1	:SET SEC REG POINTER
3074	016076	020504				CMP	R5,R4	:TX BCC OK?
3075	016100	001401				BEQ	71\$:BR IF YES
3076	016102	104003				HLT	3	:TX BCC ERROR
3077	016104	005200				INC	R0	:UPDATE LINE POINTER
3078	016106	005302				DEC	R2	:4 LINE DONE?

J05

3079	016110	J01356			BNE	70\$:BR IF NO
3080	016112			72\$:			
3081							
3082	016112	005737	001424		TST	L12.15	:DOES LINE CARD EXIST?
3083	016116	100426			BMI	75\$:BR IF NO
3084	016120	012700	000014		MOV	#12.,R0	:LOAD LINE POINTER
3085	016124	012702	000004		MOV	#4,R2	:SET FOR 4 LINE GROUP
3086	016130	010077	163236		MOV	R0,DVSR5	:LOAD LINE NO.
3087	016134	112777	000006	163232	MOVB	#6,DVSR5H	:SEL TX BCC REG
3088	016142	017704	163230		MOV	DVSR5,R4	:READ IT
3089	016146	012705	000020		MOV	#20,R5	:SET EXPECTED=20
3090	016152	060005			ADD	R0,R5	:ADD LINE NO TO EXPECTED
3091	016154	117701	163214		MOVB	DVSR5H,R1	:SET SEC REG POINTER
3092	016160	020504			CMP	R5,R4	:TX BCC OK?
3093	016162	001401			BEG	74\$:BR IF YES
3094	016164	104003			HLT	3	:TX BCC ERROR
3095	016166	005200			INC	R0	:UPDATE LINE POINTER
3096	016170	005302			DEC	R2	:4 LINE DONE?
3097	016172	001356			BNE	73\$:BR IF NO
3098	016174						
3099	016174	104400					
3100				21700		SCOPE	
3101				21800			
3102				21900			

```

:***** TEST 16 *****
:*TEST OF RECEIVER WITH MICRO-PROCESSOR FREE RUNNING.
:*TEST OF RECEIVER BYTE COUNT =0
:*TEST OF ***"ERROR CODES"*** AND RECEIVER ENTRIES INTO DVIC
:*REGISTER.
:*EXPECTED: (THIS IS FOR LINES $B )
:*DVSCR BIT15=1 BIT7=1 BIT0=1
:*DVRIC 11:08=LINE NUMBER BIT15+32
:*DVNSR 03:00=LINE NUMBER BIT15=1 BITS=1
:*TXBAP =TXBAP+1
:*TXWCP =0
:*RXBA =RXBA +0
:*RXWC =0
:*LINE STATE =BIT7=1 BIT0=1
:*IS TEST IS DONE FOR BOTH ASYNC AND SYNC LINE CARDS.
:*****

```

: TEST 16

3121	016176	012737	000016	001226	TST16:	MOV	#16,TSTNO	
3122	016204	012737	016350	001216		MOV	#TST17,NEXT	
3123	016212	012700	000000			MOV	#0.,R0	:PLACE LINE NUMBER INTO R0
3124	016216	013737	001416	001236		MOV	LO0.03,STAT	:LOAD LINE CARD STATUS INTO STAT
3125	016224	100402				BMI	100\$:BR IF LINE CARD NOT TO BE TESTED
3126	016226	004737	016314			JSR	PC,105\$:GO DO THE TEST FOR LINE CARD 1
3128	016232	012700	000004		100\$:	MOV	#4.,R0	:PLACE LINE NUMBER INTO R0
3129	016236	013737	001420	001236		MOV	LO4.07,STAT	:LOAD LINE CARD STATUS INTO STAT
3130	016244	100402				BMI	101\$:BR IF LINE CARD NOT TO BE TESTED
3131	016246	004737	016314			JSR	PC,105\$:GO DO THE TEST FOR LINE CARD 2
3132	016252	012700	000010		101\$:	MOV	#8.,R0	:LOAD LINE NUMBER
3133	016256	013737	001422	001236		MOV	LO8.11,STAT	:LOAD LINE CARD STATUS INTO STAT
3134	016264	100402				BMI	102\$:BR IF LINE CARD NOT TO BE TESTED

K05

DZDVC-C MACY11 27.7321 17-SEP-76 11:40
DZDVCC.P11 DV11 DEVICE DIAGNOSTICS.

PAGE 64
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3135	016266	004737	016314	
3136	016272	012700	000014	
3137	016276	013737	001424	001236
3138	016304	100402		
3139	016306	004737	016314	
3140	016312	104400		
3141	016314			
3142	016314	012737	022750	025544
3143	016322	012737	000000	025546
3144	016330	004537	017220	
3145	016334	023350		
3146	016336	000000		
3147	016340	022750		
3148	016342	000000		
3149	016344	100032		
3150	016346	000207		

```

103$: JSR PC,105$ ;DO THE TEST FOR LINE CARD 3
MOV #12, R0 ;LOAD LINE NO.
MOV L12, R15, STAT ;LOAD LINE CARD STATUS
BMI 103$ ;BR IF LINE CARD NOT TO BE TESTED
JSR PC,105$ ;DO THE TESTS FOR LINE CARD 4
103$: SCOPE ;SCOPE THIS TEST.
105$: ;TEST ENTRANCE.
MOV #RXBA, EXPRBA ;EXPECTED RX BA
MOV #0, EXPRWC ;EXPECTED RX BC
JSR R5, RXT01 ;GOTO SUBROUTINE
RXTAB ;LOADED INTO RX CNTR TABLE REG
0 ;LOADED INTO CORE TABLE
RXBA ;LOADED INTO RX BA
0 ;LOADED INTO RX BC
BIT15+32 ;RIC ENTRY
RTS PC ;EXIT

```

```

:***** TEST 17 *****
;*TEST OF RECEIVER WITH MICRO-PROCESSOR FREE RUNNING.
;*TEST OF RECEIVER BYTE COUNT WARNING
;*TEST OF ***"ERROR CODES"*** AND RECEIVER ENTRIES INTO DVRIC
;*REGISTER.
;*EXPECTED: (THIS IS FOR LINES $B )
;*DVSCR BIT15=1 BIT7=1 BIT0=1
;*DVRIC 11:08=LINE NUMBER BIT14+32
;*DVNSR 03:00=LINE NUMBER BIT15=1 BIT9=1
;*TXBAP =TXBAP+1
;*TXWCP =0
;*RXBA =RXBA+1
;*RXWC =0
;*LINE STATE =BIT7=1 BIT0=1
;*IS TEST IS DONE FOR BOTH ASYNC AND SYNC LINE CARDS.
:*****

```

: TEST 17

3172	016350	012737	000017	001226
3173	016356	012737	016522	001216
3174	016364	012700	000000	
3175	016370	013737	001416	001236
3176	016376	100402		
3177	016400	004737	016466	
3178	016404	012700	000004	
3179	016410	013737	001420	001236
3180	016416	100402		
3181	016420	004737	016466	
3182	016424	012700	000010	
3183	016430	013737	001422	001236
3184	016436	100402		
3185	016440	004737	016466	
3186	016444	012700	000014	
3187	016450	013737	001424	001236
3188	016456	100402		
3189	016460	004737	016466	
3190	016464	104400		

```

TST17: MOV #17, TSTNO
MOV #TST20, NEXT
MOV #0, R0 ;PLACE LINE NUMBER INTO R0
MOV L00, R03, STAT ;LOAD LINE CARD STATUS INTO STAT
BMI 100$ ;BR IF LINE CARD NOT TO BE TESTED
JSR PC,105$ ;GO DO THE TEST FOR LINE CARD 1
100$: MOV #4, R0 ;PLACE LINE NUMBER INTO R0
MOV L04, R07, STAT ;LOAD LINE CARD STATUS INTO STAT
BMI 101$ ;BR IF LINE CARD NOT TO BE TESTED
JSR PC,105$ ;GO DO THE TEST FOR LINE CARD 2
101$: MOV #8, R0 ;LOAD LINE NUMBER
MOV L08, R11, STAT ;LOAD LINE CARD STATUS INTO STAT
BMI 102$ ;BR IF LINE CARD NOT TO BE TESTED
JSR PC,105$ ;DO THE TEST FOR LINE CARD 3
102$: MOV #12, R0 ;LOAD LINE NO.
MOV L12, R15, STAT ;LOAD LINE CARD STATUS
BMI 103$ ;BR IF LINE CARD NOT TO BE TESTED
JSR PC,105$ ;DO THE TESTS FOR LINE CARD 4
103$: SCOPE ;SCOPE THIS TEST.

```

L05

```

3191 016466
3192 016466 012737 022751 025544
3193 016474 012737 000000 025546
3194 016502 004537 017220
3195 016506 023350
3196 016510 000000
3197 016512 022750
3198 016514 177777
3199 016516 040032
3200 016520 000207
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3222 016522 012737 000020 001226
3223 016530 012737 016674 001216
3224 016536 012700 000000
3225 016542 013737 001416 001236
3226 016550 100402
3227 016552 004737 016640
3228 016556 012700 000004
3229 016562 013737 001420 001236
3230 016570 100402
3231 016572 004737 016640
3232 016576 012700 000010
3233 016602 013737 001422 001236
3234 016610 100402
3235 016612 004737 016640
3236 016616 012700 000014
3237 016622 013737 001424 001236
3238 016630 100402
3239 016632 004737 016640
3240 016636 104400
3241 016640
3242 016640 012737 177320 025544
3243 016646 012737 177775 025546
3244 016654 004537 017220
3245 016660 023350
3246 016662 000000

```

105\$:

```

MOV #RXBA+1,EXPRBA ;TEST ENTRANCE.
MOV #0,EXPRWC ;EXPECTED RX BA
JSR R5,RXT01 ;EXPECTED RX BC
RXTAB ;GOTO SUBROUTINE
0 ;LOADED INTO RX CNTR TABLE REG
RXBA ;LOADED INTO CORE TABLE
-1 ;LOADED INTO RX BA
BIT14+32 ;LOADED INTO RX BC
RTS PC ;RIC ENTRY
;EXIT

```

```

:***** TEST 20 *****
: *TEST OF RECEIVER WITH MICRO-PROCESSOR FREE RUNNING.
: *TEST OF RECEIVER "RXBA NXM"
: *TEST OF ***"ERROR CODES"*** AND RECEIVER ENTRIES INTO DVRIC
: *REGISTER.
: *EXPECTED: (THIS IS FOR LINES $B )
: *DVSCR BIT15=1 BIT7=1 BIT0=1
: *DVRIC 11:08=LINE NUMBER BIT15+BIT14+32
: *DVNSR 03:00=LINE NUMBER BIT15=1 BIT8=1
: *TXBAP =TXBAP+1
: *TXWCP =0
: *RXBA =177320 +0
: *RXWC =-3
: *LINE STATE =BIT7=1 BIT0=1
: *IS TEST IS DONE FOR BOTH ASYNC AND SYNC LINE CARDS.
:*****

```

: TEST 20

```

-----
TST20: MOV #20,TSTNO
MOV #TST21,NEXT
MOV #0,R0 ;PLACE LINE NUMBER INTO R0
MOV L00.03,STAT ;LOAD LINE CARD STATUS INTO STAT
BMI 100$ ;BR IF LINE CARD NOT TO BE TESTED
JSR PC,105$ ;GO DO THE TEST FOR LINE CARD 1
100$: MOV #4,R0 ;PLACE LINE NUMBER INTO R0
MOV L04.07,STAT ;LOAD LINE CARD STATUS INTO STAT
BMI 101$ ;BR IF LINE CARD NOT TO BE TESTED
JSR PC,105$ ;GO DO THE TEST FOR LINE CARD 2
101$: MOV #8,R0 ;LOAD LINE NUMBER
MOV L08.11,STAT ;LOAD LINE CARD STATUS INTO STAT
BMI 102$ ;BR IF LINE CARD NOT TO BE TESTED
JSR PC,105$ ;DO THE TEST FOR LINE CARD 3
102$: MOV #12,R0 ;LOAD LINE NO.
MOV L12.15,STAT ;LOAD LINE CARD STATUS
BMI 103$ ;BR IF LINE CARD NOT TO BE TESTED
JSR PC,105$ ;DO THE TESTS FOR LINE CARD 4
103$: SCOPE ;SCOPE THIS TEST.
105$: ;TEST ENTRANCE.
MOV #177320,EXPRBA ;EXPECTED RX BA
MOV #-3,EXPRWC ;EXPECTED RX BC
JSR R5,RXT01 ;GOTO SUBROUTINE
RXTAB ;LOADED INTO RX CNTR TABLE REG
0 ;LOADED INTO CORE TABLE

```


M05

DZDVC-C MACY11 27(732) 17-SEP-76 11:40
DZDVCC.P11 DV11 DEVICE DIAGNOSTICS.

PAGE 66
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3247 016664 177320
3248 016666 177775
3249 016670 140032
3250 016672 000207

177320 ;LOADED INTO RX BA
-3 ;LOADED INTO RX BC
BIT15+BIT14+32 ;RIC ENTRY
RTS PC ;EXIT

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***** TEST 21 *****
*TEST OF RECEIVER WITH MICRO-PROCESSOR FREE RUNNING.
*TEST IF RECEIVER "RXTAB NXM"
*TEST OF ***"ERROR CODES"*** AND RECEIVER ENTRIES INTO DVRIC
*REGISTER.
*EXPECTED: (THIS IS FOR LINES \$B)
*DVSCR BIT15=1 BIT7=1 BIT0=1
*DVRIC 11:08=LINE NUMBER BIT15+BIT14+BIT12+32
*DVNSR 03:00=LINE NUMBER BIT15=1 BIT8=1
*TXBAP =TXBAP+1
*TXWCP =0
*RXBA =RXBA +0
*RXWC =-3
*LINE STATE =BIT7=1 BIT0=1
*IS TEST IS DONE FOR BOTH ASYNC AND SYNC LINE CARDS.

3272 016674 012737 000021 001226
3273 016702 012737 017046 001216
3274 016710 012700 000000
3275 016714 013737 001416 001236
3276 016722 100402
3277 016724 004737 017012
3278 016730 012700 000004
3279 016734 013737 001420 001236
3280 016742 100402
3281 016744 004737 017012
3282 016750 012700 000010
3283 016754 013737 001422 001236
3284 016762 100402
3285 016764 004737 017012
3286 016770 012700 000014
3287 016774 013737 001424 001236
3288 017002 100402
3289 017004 004737 017012
3290 017010 104400
3291 017012
3292 017012 012737 022750 025544
3293 017020 012737 177775 025546
3294 017026 004537 017220
3295 017032 177266
3296 017034 000000
3297 017036 022750
3298 017040 177775
3299 017042 150032
3300 017044 000207
3301
3302

; TEST 21

TST21: MOV #21,TSTNO
MOV #TST22,NEXT
MOV #0,R0 ;PLACE LINE NUMBER INTO R0
MOV L00.03,STAT ;LOAD LINE CARD STATUS INTO STAT
BMI 100\$;BR IF LINE CARD NOT TO BE TESTED
JSR PC,100\$;GO DO THE TEST FOR LINE CARD 1
100\$: MOV #4,R0 ;PLACE LINE NUMBER INTO R0
MOV L04.07,STAT ;LOAD LINE CARD STATUS INTO STAT
BMI 101\$;BR IF LINE CARD NOT TO BE TESTED
JSR PC,100\$;GO DO THE TEST FOR LINE CARD 2
101\$: MOV #8,R0 ;LOAD LINE NUMBER
MOV L08.11,STAT ;LOAD LINE CARD STATUS INTO STAT
BMI 102\$;BR IF LINE CARD NOT TO BE TESTED
JSR PC,100\$;DO THE TEST FOR LINE CARD 3
102\$: MOV #12,R0 ;LOAD LINE NO.
MOV L12.15,STAT ;LOAD LINE CARD STATUS
BMI 103\$;BR IF LINE CARD NOT TO BE TESTED
JSR PC,100\$;DO THE TESTS FOR LINE CARD 4
103\$: SCOPE ;SCOPE THIS TEST.
105\$: ;TEST ENTRANCE.
MOV #RXBA,EXPRBA ;EXPECTED RX BA
MOV #-3,EXPRWC ;EXPECTED RX BC
JSR R5,RXT01 ;GOTO SUBROUTINE
177320-32 ;LOADED INTO RX CNTR TABLE REG
0 ;LOADED INTO CORE TABLE
RXBA ;LOADED INTO RX BA
-3 ;LOADED INTO RX BC
BIT15+BIT14+BIT12+32 ;RIC ENTRY
RTS PC ;EXIT

N05

DZDVC-C MACY11 27.732) 17-SEP-75 11:40
 DZDVCC.P11 DV11 DEVICE DIAGNOSTICS.

PAGE 67
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3322 017046 012737 000022 001226
3323 017054 012737 002436 001216
3324 017062 012700 000000
3325 017066 013737 001416 001236
3326 017074 100402
3327 017076 004737 017164
3328 017102 012700 000004
3329 017106 013737 001420 001236
3330 017114 100402
3331 017116 004737 017164
3332 017122 012700 000010
3333 017126 013737 001422 001236
3334 017134 100402
3335 017136 004737 017164
3336 017142 012700 000014
3337 017146 013737 001424 001236
3338 017154 100402
3339 017156 004737 017164
3340 017162 104400
3341 017164
3342 017164 012737 022750 025544
3343 017172 012737 177775 025546
3344 017200 004537 017220
3345 017204 023350
3346 017206 000001
3347 017210 022750
3348 017212 177775
3349 017214 000032
3350 017216 000207
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3352
  
```

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:***** TEST 22 *****
:*TEST OF RECEIVER WITH MICRO-PROCESSOR FREE RUNNING.
:*TEST OF RECEIVER "SPECIAL CHARACTER"
:*TEST OF ***"ERROR CODES"*** AND RECEIVER ENTRIES INTO DVRIC
:*REGISTER.
:*EXPECTED: (THIS IS FOR LINES $B )
:*DVSCR BIT15=1 BIT7=1 BIT0=1
:*DVRIC 11:08=LINE NUMBER 32
:*DVNSR 03:00=LINE NUMBER BIT15=1 BIT8=1
:*TXBAP =TXBAP+1
:*TXWCP =0
:*RXBA =RXBA +0
:*RXWC =-3
:*LINE STATE =BIT7=1 BIT0=1
:*IS TEST IS DONE FOR BOTH ASYNC AND SYNC LINE CARDS.
:*****
  
```

: TEST 22

```

-----
TST22: MOV #22,TSTNO
MOV #.EOP,NEXT
MOV #0.,R0
MOV L00.03,STAT ;PLACE LINE NUMBER INTO R0
BMI 100$ ;LOAD LINE CARD STATUS INTO STAT
;BR IF LINE CARD NOT TO BE TESTED
JSR PC,105$ ;GO DO THE TEST FOR LINE CARD 1
100$: MOV #4.,R0 ;PLACE LINE NUMBER INTO R0
MOV L04.07,STAT ;LOAD LINE CARD STATUS INTO STAT
BMI 101$ ;BR IF LINE CARD NOT TO BE TESTED
JSR PC,105$ ;GO DO THE TEST FOR LINE CARD 2
101$: MOV #8.,R0 ;LOAD LINE NUMBER
MOV L08.11,STAT ;LOAD LINE CARD STATUS INTO STAT
BMI 102$ ;BR IF LINE CARD NOT TO BE TESTED
JSR PC,105$ ;DO THE TEST FOR LINE CARD 3
102$: MOV #12.,R0 ;LOAD LINE NO.
MOV L12.15,STAT ;LOAD LINE CARD STATUS
BMI 103$ ;BR IF LINE CARD NOT TO BE TESTED
JSR PC,105$ ;DO THE TESTS FOR LINE CARD 4
103$: SCOPE ;SCOPE THIS TEST.
105$: ;TEST ENTRANCE.
MOV #RXBA,EXPRBA ;EXPECTED RX BA
MOV #-3,EXPRWC ;EXPECTED RX BC
JSR R5,AXT01 ;GOTO SUBROUTINE
RXTAB ;LOADED INTO RX CNTR TABLE REG
BIT0 ;LOADED INTO CORE TABLE
RXBA ;LOADED INTO RX BA
-3 ;LOADED INTO RX BC
32 ;RIC ENTRY
RTS PC ;EXIT
  
```


C06

Address	Hex	Dec	Label	Code	Comment
017464	J72000				(BIT14+BIT13+BIT12)+BIT10
017466	000403				:#9600 BAUD.
017470	004537	021072			:#CONTINUE TEST.
017474	034000				:LOAD
017476	012737	000032	021350	60S:	:MODE+RX ENABLE
017504	005037	022402		61S:	:SET DATA CHAR
017510	004537	021210			:SET CNTRL BYTE TO ZERO
017514	005277	161642		23:	:ADJUST SYNC CHAR S
017520	005005				:SET UCPU GO
017522	105777	161634		33:	:DVSCRO7=1?
017526	100417				:BR IF YES
017530	104414				:WASTE TIME
017532	005205				:DELAY
017534	001372				
017536	112777	000013	161630		:SEL LINE STATE.
017544	032777	000001	161624		:IS RX ACTIVE SET?
017552	001001				:BR IF RX ACTIVE SET.
017554	104000				:RECEIVER ACTIVE IS NOT SET!
017556	105777	161600			:RE-VERIFY DVSCRO7.
017562	100401				:BR IF BIT7 IS SET.
017564	104000				:DVSCRO7 NEVER SET (=1)!
017566	017704	161570		4S:	:READ DVSCR
017572	012705	100201			:R5
017576	020504				:NPR STATUS ENTRY, RX INTR, UCPL GO
017600	001401				:BR IF OK
017602	104002				:DVSCR INCORRECT
017604	017704	161556		5S:	:GET DVRIC
017610	013701	001366			:SET POINTER
017614	010005				:GET LINE NUMBER
017616	000305				:PLACE IN HIGH BYTE
017620	000705	020052			:SET OTHER BITS EXPECTED
017624	020504				:DVRIC OK?
017626	001401				
017630	104002				:DVRIC INCORRECT
017632	017704	161544		6S:	:READ DVNSR
017636	010005				:LOAD LINE NO.
017640	052705	100400			:SILO ENTRY, PRINCIPLE BC=C
017644	020504				:DVNSR OK
017646	001403				
017650	013701	001402			
017654	104002				:DVNSR INCORRECT
017656	010077	161510		7S:	:LOAD LINE NO.
017662	017704	161510			:READ TX BA?
017666	012705	021351			:SET EXPECTED
017672	005001				:SET SEC REG POINTER
017674	020504				:OK?
017676	001401				
017700	104003				:TX BA P INCORRECT
017702	105277	161466		8S:	:SEL TX BC?
017706	005201				:SET SEC REG POINTER
017710	017704	161462			:READ IT
017714	001402				:BR IF IT=0
017716	005005				
017720	104003				:TX BC P NOT=C
017722	112777	000004	161444	9S:	:RX BA

G06

020V0-C MACY11
020V00.P11

27.732 17-SEP-75 11:40
DV11 DEVICE DIAGNOSTICS.

PAGE 73
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3633	020636	001303		
3634	020640	012605		
3635	020642	000205		
3636	020644	000001		
3637	020646	010046		
3638	020650	010146		
3639	020652	010246		
3640	020654	012537	001246	
3641	020660	012537	001250	
3642	020664	012537	001252	
3643	020670	005037	021022	
3644	020674	013700	001252	
3645	020700	006037	001250	
3646	020704	005500		
3647	020706	032700	000001	
3648	020712	001402		
3649	020714	005137	021022	
3650	020720	013700	021020	
3651	020724	005100		
3652	020726	040037	021022	
3653	020732	000241		
3654	020734	006037	001252	
3655	020740	013700	021022	
3656	020744	013700	001252	
3657	020750	010102		
3658	020752	040100		
3659	020754	043702	021022	
3660	020760	050200		
3661	020762	043737	021020	001252
3662	020770	050037	001252	
3663	020774	005337	001246	
3664	021000	001333		
3665	021002	013737	001252	021024
3666	021010	012602		
3667	021012	012601		
3668	021014	012600		
3669	021016	000205		
3670	021020	000000		
3671	021022	000000		
3672	021024	000000		
3673		000200		
3674		020001		
3675		102010		
3676				
3677				
3678	021026	010046	13300	
3679	021030	010146	13400	
3680	021032	112500	13500	
3681	021034	112501	13600	
3682	021036	110077	160332	
3683	021042	012577	160330	
3684	021046	042777	000060	160306
3685	021054	110177	160314	
3686	021060	012577	160312	
3687	021064	012601		
3688	021066	012600		

```

BNE 675 :BR IF NO
MOV (SP)+,R5 :RESTORE R5
RTS R5 :EXIT
735: .BLKW 1
SIMSC0: MOV R0,-(SP)
MOV R1,-(SP)
MOV R2,-(SP)
MOV (R5)+,TEMP1
MOV (R5)+,TEMP2
MOV (R5)+,TEMP3
15: CLR BCCFBK
MOV TEMP3,R0
ROR TEMP2
ADC R0
BIT #BIT0,R0
SEQ ZS
COM BCCFBK
25: MOV XPOLY,R0
COM R0
BIC R0,BCCFBK
CLC
ROR TEMP3
MOV BCCFBK,R0
MOV TEMP3,R1
MOV R1,R2
BIC R1,R0
BIC BCCFBK,R2
BIS R2,R0
BIC XPOLY,TEMP3
BIS R0,TEMP3
DEC TEMP1
15: BNE 15
MOV TEMP3,CALBCC
MOV (SP)+,R2
MOV (SP)+,R1
MOV (SP)+,R0
RTS R5
XPOLY: 0
BCCFBK: 0
CALBCC: 0
LRC8=200
CRC16=120001
CRC.CCITT=102010
SETREG: MOV R0,-(SP)
MOV R1,-(SP)
MOV8 (R5)+,R0
MOV8 (R5)+,R1
MOV8 R0,@DVSRSR
MOV (R5)+,@DVSRA
BIC #BITS+BIT4,@DVSOR
MOV8 R1,@DVSRSR
MOV (R5)+,@DVSRA
MOV (SP)+,R1
MOV (SP)+,R0

```


H06

3689	021070	000205		14400	EXIT	
3690				14500		
3691	021072			14600	LOAD.MODE:	
3692	021072	012577	160272	14700	MOV	(R5)+,ADVLCR
3693	021076	052777	100000	14800	BIS	#BIT15,ADVLCR
3694	021104	010046		14900	MOV	RO,-(SP)
3695	021106	005000		15000	CLR	RO
3696	021110	005777	160254	15100	1S: TST	ADVLCR
3697	021114	100004		15200	BPL	2S
3698	021116	104414		15300	DELAY	
3699	021120	005200		15305	INC	RO
3700	021122	001372		15400	BNE	1S
3701	021124	104000		15500	HLT	C
3702	021126	012600		15600	2S: MOV	(SP)+,RO
3703	021130	000205		15700	EXIT	:BIT 15 FAILED TO CLEAR
3704						
3705	021132				SETSCAN:	
3706	021132	010346			MOV	R3,-(SP)
3707	021134	052777	000010	160220	BIS	#BIT3,ADVSCR
3708	021142	012503			MOV	(R5)+,R3
3709	021144	001414			BEQ	2S
3710	021146	012777	050102	160224	1S: MOV	#BIT14+BIT12+BIT6+BIT1,ADVSR
3711	021154	104415			ROMCLK	
3712	021156	005201			INC	R1
3713	021160	012777	050102	160212	MOV	#BIT14+BIT12+BIT6+BIT1,ADVSR
3714	021166	104415			ROMCLK	
3715	021170	005201			INC	R1
3716	021172	005302			DEC	R3
3717	021174	001364			BNE	1S
3718	021176	012603			2S: MOV	(SP)+,R3
3719	021200	010100			MOV	R1,RO
3720	021202	000241			CLC	
3721	021204	006000			ROR	RO
3722	021206	000205			EXIT	
3723	021210				SETSYNC:	
3724	021210	113737	001236	021346	MOVB	STAT,SYNC
3725	021216	113737	021346	021347	MOVB	SYNC,SYNC+!
3726	021224	032737	010000	001236	BIT	#TWO\$YN,STAT
3727	021232	001402			BEQ	1S
3728	021234	105037	021346		CLRB	SYNC
3729	021240	000205			1S: EXIT	:SET SYNC FOR THIS LINE. :PLACE SYNC IN HIGH BYTE :ONE SYNC OR TWO? :BR IF JUMPERED FOR TWO. :SET FIRST SYNC TO NON-SYNC
3730				15000		
3731	021242	000042		16100	REGBUF: .BLKW	34.
3732	021346	000001		16200	SYNC: .BLKW	1
3733	021350	000400		16300	TXBAP: .BLKB	400
3734	021750	000400		16400	TXBAS: .BLKB	400
3735	022350	000400		16500	TXTAB: .BLKB	400
3736	022750	000400		16600	RXBA: .BLKB	400
3737	023350	000400		16700	RXTAB: .BLKB	400
3738	023750			16800	ROMDATA:	

3739			17500		:: IDLE LOOP	
3740			17600			
3741	023750	050102	17700	↑B<0101000001000010>	: ILOOP S/C	6,2 : INCREMENT SCANNER
3742	023752	030124	17800	↑B<0011000001010100>	: XFR	5,4 : MOVE MASTER SCAN TO RAM ADDRESS
3743	023754	001344	17900	↑B<0000001011100100>	: BRA	2,↑RSERV : TEST FOR TRANSMIT FLAG WAITING.
3744	023756	002012	18000	↑B<0000010000001010>	: BRA	4,RSERV : TEST FOR RECEIVER FLAG WAITING.
3745	023760	001503	18100	↑B<0000001101000011>	: BRA	3,SSERV : TEST FOR RECEIVED CHARACTER WAITING.
3746	023762	020013	18200	↑B<0010000000001011>	: ILOP2 RAM	0,0,13 : OBTAIN LINE STATE
3747	023764	070456	18300	↑B<0111000100101110>	: BRB	1,RSYNC : TEST RAM OUTPUT 01 (RESYNC), IF
3748	023766	071072	18400	↑B<0111001000111010>	: BRB	2,TMARK : TEST RAM OUTPUT 02 (XMIT GO), IF
3749	023770	002451	18500	↑B<0000010100101001>	: ILOP5 BRA	5,↑RSERV : TEST FOR CHARACTER DISPATCH PROC.
3750	023772	000400	18600	↑B<0000000100000000>	: BRA	1,ILOOP : TEST FOR SURE TRUE, IF YES BRAN
3751			18700			
3752			18800			
3753			18900			
3754			19000			
3755			19100			
3756	023774	020013	19200	↑B<0010000000001011>	: RSERV RAM	0,0,13 : OBTAIN LINE STATE
3757	023776	070036	19300	↑B<0111000000011110>	: BRB	0,TESTX : TEST RAM OUTPUT 00 (RECEIVER ACT
3758	024000	076417	19400	↑B<0111110100001111>	: BRB	15,S/ACT : TEST MATCH DETECT, IF Y
3759	024002	050106	19500	↑B<0101000001000110>	: S/C	6,6 : SET RESYNC PULSE.
3760	024004	000400	19600	↑B<0000000100000000>	: BRA	1,ILOOP : TEST FOR SURE TRUE, IF YES BRAN
3761	024006	020012	19700	↑B<0010000000001010>	: S/ACT RAM	0,0,12 : OBTAIN DLE/PROTOCOL
3762	024010	070420	19800	↑B<0111000100011000>	: BRB	1,SACT2 : TEST RAM 01 (STRIP LEADING SYNC
3763	024012	020013	19900	↑B<0010000000001011>	: SACT1 RAM	0,0,13 : OBTAIN LINE STATE
3764	024014	050047	20000	↑B<0101000000100111>	: S/C	5,7 : SET RAM OUTPUT 00 (RECEIVER ACT
3765	024016	020673	20100	↑B<0010000110111011>	: RAM	1,13,13 : WRITE NEW LINE STATE
3766	024020	077021	20200	↑B<0111111000010001>	: BRB	16,SACT1 : TEST FOR WRITE INHIBIT.
3767	024022	050023	20300	↑B<0101000000010011>	: CLRRF S/C	4,3 : SET RECEIVE DATA ENABLE
3768	024024	050022	20400	↑B<0101000000010010>	: S/C	4,2 : CLEAR RECEIVE DATA ENABLE AND 0
3769	024026	000400	20500	↑B<0000000100000000>	: BRA	1,ILOOP : TEST FOR SURE TRUE, IF YES BRAN
3770	024030	020013	20600	↑B<0010000000001011>	: SACT2 RAM	0,0,13 : OBTAIN LINE STATE
3771	024032	050047	20700	↑B<0101000000100111>	: S/C	5,7 : SET RAM OUTPUT 00 (RECEIVER ACT
3772	024034	050206	20800	↑B<0101000010000110>	: S/C	7,6 : SET RAM OUTPUT 06 (STRIP SYNC 0
3773	024036	020673	20900	↑B<0010000110111011>	: RAM	1,13,13 : WRITE NEW LINE STATE
3774	024040	077030	21000	↑B<0111111000011000>	: BRB	16,SACT2 : TEST FOR WRITE INHIBIT.
3775	024042	000425	21100	↑B<0000000100010101>	: BRA	1,CLRRF : TEST FOR SURE TRUE, IF YES BRAN
3776			21200			
3777			21300			
3778	024044	020013	21400	↑B<0010000000001011>	: TESTX RAM	0,0,13 : OBTAIN LINE STATE
3779	024046	073041	21500	↑B<0111011000100001>	: BRB	6,TMD : TEST RAM OUTPUT 06 (STRIP SYNC
3780	024050	000445	21600	↑B<0000000100100101>	: BRA	1,S/RDE : TEST FOR SURE TRUE, IF YES BRAN
3781	024052	076425	21700	↑B<0111110100010101>	: TMD BRB	15,CLRRF : TEST MATCH DETECT, IF Y
3782	024054	050202	21800	↑B<0101000010000010>	: S/C	7,2 : CLEAR RAM OUTPUT 06 (STRIP SYNC
3783	024056	020673	21900	↑B<0010000110111011>	: RAM	1,13,13 : WRITE NEW LINE STATE
3784	024060	077012	22000	↑B<0111111000001010>	: BRB	16,RSERV : TEST FOR WRITE INHIBIT.
3785	024062	050023	22100	↑B<01010000000010011>	: S/RDE S/C	4,3 : SET RECEIVE DATA ENABLE
3786	024064	050021	22200	↑B<01010000000010001>	: S/C	4,1 : SET SILO IN
3787	024066	050022	22300	↑B<01010000000010010>	: S/C	4,2 : CLEAR RECEIVE DATA ENABLE AND 0
3788	024070	000400	22400	↑B<0000000100000000>	: BRA	1,ILOOP : TEST FOR SURE TRUE, IF YES BRAN
3789			22500			
3790			22600			
3791			22700			
3792			22800			
3793	024072	030301	22900	↑B<0011000011000001>	: ISERV XFR	14,1 : MOVE SILO OUT TO A REGISTER
3794	024074	010037	23000	↑B<0001000000011111>	: ALU	37 : LET ALU RESULT = A REGISTER

3795	024076	330144	23100	↑B<0011000001100100>	:	XFR	6.4	:MOVE ALU RESULT 08-11 TO RAM AD
3796	024100	050016	23200	↑B<0101000000001110>	:	S/C	3.6	:CLEAR SCRO8
3797	024102	000542	23300	↑B<0000000101100010>	:	BRA	1.CTEST	:TEST FOR SURE TRUE, IF YES BRAN
3798			23400		:			
3799			23500		:			
3800			23600		:			
3801			23700		:			
3802			23800		:			
3803	024104	020013	23900	↑B<0010000000001011>	:	RSYNC RAM	0.0.13	:OBTAIN LINE STATE
3804	024106	050043	24000	↑B<0101000000100011>	:	S/C	5.3	:CLEAR RAM OUTPUT 00 (RECEIVER A
3805	024110	050041	24100	↑B<0101000000100001>	:	S/C	5.1	:CLEAR RAM OUTPUT 01 (RESYNCHRON
3806	024112	020673	24200	↑B<0010000110111011>	:	RAM	1.13.13	:WRITE NEW LINE STATE
3807	024114	077056	24300	↑B<011111000101110>	:	BRB	16.RSYNC	:TEST FOR WRITE INHIBIT,
3808	024116	020016	24400	↑B<0010000000001110>	:	PSI RAM	0.0.16	:OBTAIN LINE PROTOCOL
3809	024120	050204	24500	↑B<0101000010000100>	:	S/C	7.4	:SET RAM OUTPUT 07
3810	024122	020676	24600	↑B<0010000110111110>	:	RAM	1.13.16	:WRITE NEW LINE PROTOCOL
3811	024124	077053	24700	↑B<011111000110011>	:	BRB	16.PSI	:TEST FOR WRITE INHIBIT, IF YES
3812	024126	050106	24800	↑B<0101000001000110>	:	S/C	6.6	:SET RESYNC PULSE
3813	024130	050021	24900	↑B<010100000010001>	:	S/C	4.1	:SET SILO IN
3814	024132	000405	25000	↑B<000000100000101>	:	BRA	1.ILOP2	:TEST FOR SURE TRUE, IF YES BRAN
3815			25100		:			
3816			25200		:			
3817			25300		:			
3818			25400		:			
3819			25500		:			
3820			25600		:			
3821	024134	050101	25700	↑B<0101000001000001>	:	TMARK S/C	6.1	:CLEAR TMARK
3822	024136	000410	25800	↑B<0000000100001000>	:	BRA	1.ILOP5	:TEST FOR SURE TRUE, IF YES BRAN
3823			25900		:			
3824			26000		:			
3825			26100		:			
3826			26200		:			
3827			26300		:			
3828			26400		:			
3829	024140	000076	26500	↑B<0000000000111110>	:	TFRF BRA	0.CRAM7	:TEST BIT 15 OF ALU RESULT, IF Y
3830	024142	000603	26600	↑B<0000000110000011>	:	BRA	1.DISC	:TEST FOR SURE TRUE, IF YES BRAN
3831	024144	020016	26700	↑B<0010000000001110>	:	CRAM7 RAM	0.0.16	:OBTAIN LINE PROTOCOL
3832	024146	050200	26800	↑B<0101000010000000>	:	S/C	7.0	:CLEAR RAM OUTPUT 07 (RESYNCH FL
3833	024150	020676	26900	↑B<0010000110111110>	:	RAM	1.13.16	:WRITE NEW LINE PROTOCOL
3834	024152	077076	27000	↑B<011111000111110>	:	BRB	16.CRAM7	:TEST FOR WRITE INHIBIT,
3835	024154	000603	27100	↑B<0000000110000011>	:	BRA	1.DISC	:TEST FOR SURE TRUE, IF YES BRAN
3836			27200		:			
3837			27300		:			
3838			27400		:			
3839			27500		:			
3840	024156	002451	27600	↑B<0000010100101001>	:	SSERV BRA	5.ISERV	:TEST FOR SCRO8 (COULD HAVE SET
3841	024160	030301	27700	↑B<0011000011000001>	:	XFR	14.1	:MOVE SILO OUT TO A REGISTER
3842	024162	010037	27800	↑B<0001000000011111>	:	ALU	37	:LET ALU RESULT = A REGISTER
3843	024164	030144	27900	↑B<0011000001100100>	:	XFR	6.4	:MOVE ALU RESULT 08-11 TO RAM AD
3844	024166	020013	28000	↑B<0010000000001011>	:	RAM	0.0.13	:OBTAIN LINE STATE
3845	024170	070603	28100	↑B<0111000110000011>	:	BRB	1.DISC	:TEST RAM OUTPUT 01 (RESYNC), IF
3846	024172	020016	28200	↑B<0010000000001110>	:	RAM	0.0.16	:OBTAIN LINE PROTOCOL
3847	024174	073474	28300	↑B<0111011100111100>	:	BRB	7.TFRF	:TEST RAM OUTPUT 07, IF YES BRAN
3848	024176	104261	28400	↑B<1000100010110001>	:	BRA	10.POER	:TEST BITS 13, 12 OF ALU RESULT
3849	024200	073272	28500	↑B<0111011010111010>	:	BRB	6.TBC2	:TEST RAM OUTPUT 06, IF YES BRAN
3850	024202	072645	28600	↑B<0111010110100101>	:	BRB	5.TBC1	:TEST RAM OUTPUT 05, IF YES BRAN

K06

3851	024204	020005	28700	↑B<0010000000000101>	:	RAM	0,0,5	:OBTAIN RECEIVER BYTE COUNT
3852	024206	076214	28800	↑B<0111110010001100>	:	BRB	14,CRBCO	:TEST RAM OUTPUT 0-14=0
3853	024210	020012	28900	↑B<0010000000001010>	:	RAM	0,0,12	:OBTAIN TRANSMITTER DLE/LINE PR0
3854	024212	072576	29000	↑B<0111010101111110>	:	BRB	5,00CMR	:TEST RAM OUTPUT 05, IF YES BRAM
3855	024214	020015	29100	↑B<0010000000001101>	:	RAM	0,0,15	:OBTAIN RECEIVER MODE BITS
3856	024216	030242	29200	↑B<0011000010100010>	:	XFR	12,2	:MOVE RAM OUTPUT DATA TRANSLATED
3857	024220	050027	29300	↑B<0101000000010111>	:	S/C	4,7	:CLEAR ALU RESULT UPPER BYTE
3858	024222	030361	29400	↑B<0011000011110001>	:	XFR	17,1	:MOVE ALU RESULT TO A REGISTER
3859	024224	010026	29500	↑B<0001000000010110>	:	ALU	26	:LET ALU RESULTS = A PLUS B
3860	024226	030362	29600	↑B<0011000011110010>	:	XFR	17,2	:MOVE ALU RESULTS TO B REGISTER
3861	024230	020011	29700	↑B<0010000000001001>	:	RAM	0,0,11	:OBTAIN RECEIVER CONTROL TABLE B
3862	024232	030261	29800	↑B<0011000010110001>	:	XFR	13,1	:MOVE RAM OUTPUT DATA TO A REGIS
3863	024234	010026	29900	↑B<00010000000010110>	:	ALU	26	:LET ALU RESULTS = A PLUS B (EFF
3864	024236	030363	30000	↑B<0011000011110011>	:	XFR	1,17,3	:MOVE ALU RESULTS TO NPR ADDRESS
3865	024240	040000	30100	↑B<0100000000000000>	:	NPR		:DO NPR TO GET CONTROL BYTE
3866	024242	074535	30200	↑B<0111100101011101>	:	BRB	11,RBUS1	:TEST REQUEST BUS, IF YE
3867	024244	003332	30300	↑B<0000011011011010>	:	BRA	6,RNXMC	:TEST NXM, IF YES, BRANCH TO REC
3868	024246	075327	30400	↑B<0111101011010111>	:	BRB	12,RMPEC	:TEST MEM PAR ERR, IF YE
3869	024250	020017	30500	↑B<0010000000001111>	:	RAM	0,0,17	:OBTAIN CONTROL BYTE STORAGE REG
3870	024252	020637	30600	↑B<0010000110011111>	:	RAM	1,11,17	:MOVE DATA REGISTER TO RAM AND W
3871			30700		:			
3872			30800		:			
3873			30900		:			
3874			31000		:			
3875			31100		:			
3876			31200		:			
3877	024254	020017	31300	↑B<0010000000001111>	:	CTEST RAM	0,0,17	:OBTAIN CONTROL BYTE STORAGE REG
3878	024256	030262	31400	↑B<0011000010110010>	:	XFR	13,2	:MOVE RAM OUTPUT TO B REGISTER
3879	024260	010005	31500	↑B<0001000000000101>	:	ALU	5	:LET ALU RESULT = B REGISTER
3880	024262	020575	31600	↑B<0010000101111101>	:	RAM	1,7,15	:MOVE ALU RESULTS TRANSLATED 5-7
3881	024264	105253	31700	↑B<1000101010101011>	:	BRA	12,CBINT	:TEST BIT 0 OF ALU RESULT
3882	024266	006233	31800	↑B<0000110010011011>	:	BRA	14,E3CC	:TEST BIT 02 OF ALU RESULT, IF Y
3883	024270	006605	31900	↑B<0000110110000101>	:	EPSIL BRA	15,RBCC	:TEST BIT 03 OF ALU RESULT, IF Y
3884			32000		:			
3885			32100		:			
3886			32200		:			
3887			32300		:			
3888	024272	007203	32400	↑B<0000111010000011>	:	RRBCC BRA	16,DISC	:TEST BIT 4 OF ALU RESULT, IF YE
3889	024274	020004	32500	↑B<0010000000000100>	:	RAM	0,0,4	:OBTAIN RECEIVER CURRENT ADDRESS
3890	024276	031663	32600	↑B<0011001110110011>	:	XFR	0,13,3	:MOVE RAM OUTPUT TO NPR ADDRESS
3891	024300	030305	32700	↑B<0011000011000101>	:	XFR	14,5	:MOVE SILO OUT TO DATA REGISTER
3892	024302	040000	32800	↑B<0100000000000000>	:	NPR		:DO NPR TO STORE RECEIVED CHARAC
3893	024304	074556	32900	↑B<0111100101101110>	:	BRB	11,RBUS2	:TEST REQUEST BUS, IF YE
3894	024306	003340	33000	↑B<0000011011100000>	:	BRA	6,RNXM	:TEST NXM, IF YES, BRANCH TO REC
3895	024310	020005	33100	↑B<0010000000000101>	:	ORBC RAM	0,0,5	:OBTAIN RECEIVER BYTE COUNT
3896	024312	030261	33200	↑B<0011000010110001>	:	XFR	13,1	:MOVE RAM OUTPUT TO REGISTER A
3897	024314	010077	33300	↑B<0001000000111111>	:	ALU	17	:LET ALU RESULTS = A+1
3898	024316	020765	33400	↑B<0010000111110101>	:	RAM	1,17,5	:MOVE ALU RESULTS TO RAM INPUT
3899	024320	077160	33500	↑B<0111111001110000>	:	BRB	16,ORBC	:TEST FOR WRITE INHIBIT, IF YES
3900	024322	020004	33600	↑B<0010000000000100>	:	ORCA RAM	0,0,4	:OBTAIN RECEIVER CURRENT ADDRESS
3901	024324	030261	33700	↑B<0011000010110001>	:	XFR	13,1	:MOVE RAM OUTPUT DATA TO REGISTE
3902	024326	010077	33800	↑B<0001000000111111>	:	ALU	17	:LET ALU RESULTS = A+1
3903	024330	020764	33900	↑B<0010000111110100>	:	RAM	1,17,4	:MOVE ALU RESULTS TO RAM INPUT
3904	024332	077165	34000	↑B<0111111001110101>	:	BRB	16,ORCA	:TEST FOR WRITE INHIBIT, IF YES
3905	024334	020005	34100	↑B<0010000000000101>	:	RAM	0,0,5	:OBTAIN RECEIVER BYTE COUNT
3906	024336	076217	34200	↑B<0111110010001111>	:	BRB	14,NBCO	:TEST RAM OUTPUT 0-14=0, IF YES.

L06

3907	024340	050020	34300	↑B<0101000000010000>	S/C	4,0	;SET SILO OUT
3908	024342	000400	34400	↑B<0000000100000000>	BRA	1,ILOOP	;TEST FOR SURE TRUE, IF YES BRAN
3909			34500				
3910			34600				
3911			34700				
3912			34800				;DDCMP RECEPTION
3913	024344	020015	34900	↑B<0010000000001101>	DDCMR	RAM	0,0,15 ;OBTAIN RECEIVER MODE BITS
3914	024346	076201	35000	↑B<0111110010000001>	BRB	14,DDCM2	;TEST RAM OUTPUT 0-14=0,
3915	024350	000523	35100	↑B<0000000101010011>	BRA	1,ZETA	;TEST FOR SURE TRUE, IF YES BRAN
3916	024352	010014	35200	↑B<0001000000001100>	DDCM2	ALU	14 ;LET ALU RESULT = 0
3917	024354	000605	35300	↑B<0000000110000101>	BRA	1,RBCC	;TEST FOR SURE TRUE, IF YES BRAN
3918			35400				
3919			35500				
3920			35600				;DISCARD RECEIVED CHARACTER
3921			35700				
3922	024356	050020	35800	↑B<0101000000010000>	DISC	S/C	4,0 ;SET SILO OUT
3923	024360	000400	35900	↑B<0000000100000000>	BRA	1,ILOOP	;TEST FOR SURE TRUE, IF YES BRAN
3924			36000				
3925			36100				
3926			36200				;CALCULATE RECV BCC (ASSUME RECEIVED CHARACTER IN SILO
3927			36300				
3928	024362	030301	36400	↑B<0011000011070001>	RBCB	XFR	14,1 ;MOVE SILO OUT REGISTER TO A REG
3929	024364	020007	36500	↑B<0010000000000111>	RAM	0,0,7	;OBTAIN RECV BCC CALCULATED TO D
3930	024366	030262	36600	↑B<0011000010110010>	XFR	13,2	;MOVE RAM OUTPUT DATA TO B REGIS
3931	024370	020012	36700	↑B<0010000000001010>	RAM	0,0,12	;OBTAIN TRANSMITTER DLE/LINE PRO
3932	024372	060000	36800	↑B<0110000000000000>	BCC		;PERFORM SPECIFIED BCC CALCULATI
3933	024374	020747	36900	↑B<0010000111100111>	RAM	1,16,7	;MOVE BCC TO RAM INPUT AND WRITE
3934	024376	000551	37000	↑B<0000000101101001>	BRA	1,RRBCC	;TEST FOR SURE TRUE, IF YES, BRA
3935			37100				
3936			37200				
3937			37300				;CHARACTER RECEIVED WHILE RECV BC=0
3938			37400				
3939	024400	030306	37500	↑B<0011000011000110>	CRBCD	XFR	14,6 ;MOVE SILO OUT REGISTER TO R1CR
3940	024402	050010	37600	↑B<0101000000001000>	S/C	3,0	;SET R1CR 15 (TO INDICATE RECEPT
3941	024404	100662	37700	↑B<1000000110110010>	BRA	1,CNACB	;TEST FOR SURE TRUE, IF YES BRAN
3942			37800				
3943			37900				;NEXT CHARACTER WILL HAVE BC=0 (SILO OUT HAS BEEN SET
3944			38000				
3945	024406	030326	38100	↑B<0011000011010110>	NBCD	XFR	15,6 ;MOVE NPR DATO REGISTER TO R1CR
3946	024410	050011	38200	↑B<0101000000001001>	S/C	3,1	;SET R1CR 14 (TO INDICATE RECEPT
3947	024412	075623	38300	↑B<0111101110010011>	BRB	13,MCBCX	;TEST RAM OUTPUT 15, IF
3948	024414	100662	38400	↑B<1000000110110010>	BRA	1,CNACB	;TEST FOR SURE TRUE, IF YES BRAN
3949			38500				
3950			38600				
3951			38700				;MODE CHANGE AND BCC EXPECT
3952			38800				
3953	024416	020013	38900	↑B<0010000000001011>	MCBCX	RAM	0,0,13 ;OBTAIN LINE STATE
3954	024420	030262	39000	↑B<0011000010110010>	XFR	13,2	;MOVE RAM OUTPUT TO B REGISTER
3955	024422	030202	39100	↑B<0011000010000010>	XFR	10,2	;MOVE B REGISTER 8-15 TO B REGIS
3956	024424	010005	39200	↑B<0001000000000101>	ALU	5	;LET ALU RESULT = B REGISTER
3957	024426	020575	39300	↑B<0010000101111101>	RAM	1,7,15	;MOVE ALU RESULTS TRANSLATED TO
3958	024430	020777	39400	↑B<0010000111111111>	RAM	1,17,17	;WRITE CONTROL BYTE STORAGE FROM
3959	024432	006240	39500	↑B<0000110010100000>	BRA	14,EBCN	;TEST ALU RESULT 02, IF YES BRAN
3960	024434	100662	39600	↑B<1000000110110010>	BRA	1,CNACB	;TEST FOR SURE TRUE, IF YES BRAN
3961			39700				
3962			39800				

N06

4019	024560	010034	45500	↑B<0001000000011100>	BCCCK	ALU	34	;LET ALU RESULT = MINUS 1
4020	024562	050027	45600	↑B<0101000000010111>		S/C	4,7	;CLEAR ALU RESULT UPPER BYTE
4021	024564	030361	45700	↑B<0011000011110001>		XFR	,17,1	;MOVE ALU RESULT TO A REGISTER
4022	024566	030302	45800	↑B<0011000011000010>		XFR	,14,2	;MOVE SILO OUT TO B REGISTER
4023	024570	010015	45900	↑B<0001000000001101>		ALU	15	;LET ALU RESULT = AND OF A CCMPL
4024	024572	030362	46000	↑B<0011000011110010>		XFR	,17,2	;MOVE ALU RESULT TO B REGISTER
4025	024574	030341	46100	↑B<0011000011100001>		XFR	,16,1	;MOVE BCC TO A REGISTER
4026	024576	010037	46200	↑B<0001000000011111>		ALU	37	;LET ALU RESULT = A
4027	024600	050027	46300	↑B<0101000000010111>		S/C	4,7	;CLEAR ALU RESULT UPPER BYTE
4028	024602	030361	46400	↑B<0011000011110001>		XFR	,17,1	;MOVE ALU RESULT TO A REGISTER
4029	024604	010036	46500	↑B<0001000000011110>		ALU	36	;LET ALU RESULT= A OR B
4030	024606	030361	46600	↑B<0011000011110001>		XFR	,17,1	;MOVE ALU RESULT TO A REGISTER
4031	024610	030342	46700	↑B<0011000011100010>		XFR	,16,2	;MOVE BCC TO B REGISTER
4032	024612	030202	46800	↑B<0011000010000010>		XFR	,10,2	;MOVE B REGISTER 8-15 TO B REGIS
4033	024614	010036	46900	↑B<0001000000011110>		ALU	36	;LET ALU RESULT = A OR B
4034	024616	030366	47000	↑B<0011000011110110>		XFR	,17,6	;MOVE ALU RESULT TO R1CR REGISTE
4035	024620	050015	47100	↑B<0101000000001101>		S/C	3,5	;SET R1CR 12
4036	024622	050011	47200	↑B<0101000000001001>		S/C	3,1	;SET R1CR 14
4037	024624	100662	47300	↑B<1000000110110010>		BRA	1,CNACB	;TEST FOR SURE TRUE, IF YES BRAN
4038			47400					
4039			47500					;RECEIVER MPE / CONTROL BYTE
4040			47600					
4041	024626	030306	47700	↑B<0011000011000110>		RMPEC XFR	,14,6	;MOVE SILO OUT TO R1CR REGISTER
4042	024630	050014	47800	↑B<0101000000001100>		S/C	3,4	;SET R1CR 13
4043	024632	000733	47900	↑B<0000000111011011>		BRA	1,GAMMA	;TEST FOR SURE TRUE, IF YES BRAN
4044			48000					
4045			48100					;RECEIVER NXM / CONTROL BYTE
4046			48200					
4047	024634	030306	48300	↑B<0011000011000110>		RNXMC XFR	,14,6	;MOVE SILO OUT TO R1CR REGISTER
4048	024636	050015	48400	↑B<0101000000001101>		GAMMA S/C	3,5	;SET R1CR 12
4049	024640	050011	48500	↑B<0101000000001001>		BETA S/C	3,1	;SET R1CR 14
4050	024642	050010	48600	↑B<0101000000001000>		S/C	3,0	;SET R1CR 15
4051	024644	050017	48700	↑B<0101000000001111>		S/C	3,7	;CLEAR NXM
4052	024646	100662	48800	↑B<1000000110110010>		BRA	1,CNACB	;TEST FOR SURE TRUE, IF YES BRAN
4053			48900					
4054			49000					
4055			49100					;RECEIVER NXM (WE GOT HERE FROM RECEIVED CHARACTER SIL
4056			49200					
4057	024650	030306	49300	↑B<0011000011000110>		RNXM XFR	,14,6	;MOVE SILO OUT TO R1CR REGISTER
4058	024652	000734	49400	↑B<0000000111011100>		BRA	1,BETA	;TEST FOR SURE TRUE, IF YES BRAN
4059			49500					
4060			49600					
4061			49700					;NPR SILO OVERFLOW
4062			49800					
4063	024654	050012	49900	↑B<0101000000001010>		NPRSO S/C	3,2	;SET SCR 10 INDICATING NPR SILO
4064	024656	000400	50000	↑B<0000000100000000>		BRA	1,ILOOP	;TEST FOR SURE TRUE, IF YES BRAN
4065			50100					
4066			50200					
4067			50300					;TRANSMIT SERVICE
4068			50400					
4069			50500					
4070			50600					;CHECK FOR BCC TRANSMISSION
4071			50700					
4072	024660	020016	50800	↑B<0010000000001110>		TSERV RAM	0,0,16	;OBTAIN LINE PROTOCOL
4073	024662	030261	50900	↑B<0011000010110001>		XFR	,13,1	;MOVE RAM OUTPUT DATA TO A REGIS
4074	024664	010037	51000	↑B<0001000000011111>		ALU	37	;LET ALU RESULT=A REGISTER

E07

```
025200 020001 67900
025200 176132 69000
025200 000400 68100 1B<0010000000000001>
025200 020003 68200 1B<1111110001011010>
025200 176137 68300 1B<0000000100000000>
025200 000400 68400 1B<0010000000000011>
025200 176137 68500 1B<1111110001011111>
025200 000400 68600 1B<0000000100000000>
68700
68800
68900
69000
69100 1B<0010000100000011>
69200 1B<1000000101001001>
69300
69400
69500
69600
69700 1B<0010000000001011>
69800 1B<0101000000100010>
69900 1B<0010000110111011>
70000 1B<1111111001011111>
70100 1B<0000000100000000>
70200
70300
70400
70500 1B<0010000000001010>
70600 1B<1111000001100111>
70700 1B<0000000100000000>
70800 1B<0101000001000101>
70900 1B<0000000100000000>
71000
71100
71200
71300
71400 1B<0010000000001011>
71500 1B<0101000000100100>
71600 1B<0010000110111011>
71700 1B<1111111001101001>
71800 1B<1000000100010010>
71900
72000
72100
72200
72300 1B<0010000000001011>
72400 1B<0101000000100100>
72500 1B<0010000110111011>
72600 1B<1111111001101110>
72700 1B<1000000101111011>
72800
72900
73000
73100
73200
73300
73400

;;CHECK FOR BOTH BC=0
CBCO RAM 0,0,1 ;OBTAIN PRINCIPAL BYTE COUNT
BRB 14,DELTA ;TEST RAM OUTPUT 0-14-0
BRA 1,1LOOP ;TEST FOR SURE TRUE, IF YES BRAN
DELTA RAM 0,0,3 ;OBTAIN ALTERNATE BYTE COUNT
BRB 14,C/GO ;TEST RAM OUTPUT 0-14-0, IF YES,
BRA 1,1LOOP ;TEST FOR SURE TRUE, IF YES BRAN

;CLEAR ALTERNATE BYTE COUNT
ESS RAM 1,0,3 ;ZERO ALTERNATE BYTE COUNT
BRA 1,C/MB ;TEST FOR SURE TRUE, BRANCH TO 0

;CLEAR GO
C/GO RAM 0,0,13 ;OBTAIN LINE STATE
S/C 5,2 ;CLEAR RAM 02 (TRANSMITTER GO)
RAM 1,13,13 ;WRITE NEW LINE STATE
BRB 16,C/GO ;TEST FOR WRITE INHIBIT, IF YES
BRA 1,1LOOP ;TEST FOR SURE TRUE, IF YES BRAN

;SELECT TYPE OF IDLE
ITYPE RAM 0,0,12 ;OBTAIN TRANSMITTER DLE PROTOCOL
BRB 0,BCOCC ;TEST RAM OUTPUT 00, IF YES BRAN
BRA 1,1LOOP ;TEST FOR SURE TRUE, IF YES BRAN
BCOCC S/C 6,5 ;SET T MARK
BRA 1,1LOOP ;TEST FOR SURE TRUE, IF YES BRAN

;SENT IDLE (LINE STATE IS IN RAM OUTPUT)
SIDE RAM 0,0,13 ;OBTAIN LINE STATE
S/C 5,4 ;SET RAM 03 (TRANSMITTER UNDERRU
RAM 1,13,13 ;MOVE RAM OUTPUT TO RAM (AND WRI
BRB 16,SIDE ;TEST FOR WRITE INHIBIT
BRA 1,ALPHA ;TEST FOR SURE TRUE, IF YES, BRA

;SENT IDLE/DLE
MU RAM 0,0,13 ;OBTAIN LINE STATE
S/C 5,4 ;SET 03 (UNDERRUN)
RAM 1,13,13 ;WRITE LINE STATE
BRB 16,MU ;TEST FOR INHIBIT
BRA 1,MU ;GO BACK TO SEND IDLE

;SEND DLE FIRST
;WE GOT HERE FROM TRANSMIT SERVICE. THE CONTROL BYTE
;IN ALU RESULT AND B REGISTER. MASTER SCAN POSITION 1
;RAM ADDRESS REGISTER 0-3).
```


G07

4355		79100
4356		79200
4357		79300
4358		79400
4359		79500
4360		79600
4361		79700
4362		79800
4363		79900
4364	025424	80000
4365	025426	80100
4366	025428	80200
4367	025430	80300
4368	025432	80400
4369	025434	80500
4370	025436	80600
4371	025438	80700
4372	025440	80800
4373	025442	80900
4374	025444	81000
4375	025446	81100
4376	025448	81200
4377	025450	81300
4378	025452	81400
4379		81500
4380		81600
4381		81700
4382		81800
4383		81900
4384	025454	82000
4385	025456	82100
4386	025460	82200
4387		82300
4388		82400
4389		82500
4390	025462	82600
4391	025464	82700
4392	025466	82800
4393	025470	82900
4394	025472	83000
4395	025474	83100
4396		83200
4397		83300
4398		83400
4399		83500
4400		83600
4401		83700
4402		83800
4403		83900
4404	025476	84000
4405	025500	84100
4406	025502	84200
4407	025504	84300
4408	025506	84400
4409	025510	84500
4410		84600

```

†B<0010000000001110>
†B<0011000010110001>
†B<0010000001111111>
†B<0010000111111110>
†B<111111010010110>
†B<001000000000110>
†B<0011000010110000>
†B<001000000001010>
†B<1111001110100001>
†B<1111010010100001>
†B<1000000110100101>
†B<0000000100000000>
†B<001000000000110>
†B<0011000010110010>
†B<0011000010000000>
†B<0010000100000110>
†B<0010000000001110>
†B<01010000000100001>
†B<0010000110111110>
†B<111111010100101>
†B<0000000100000000>
†B<0010000000001111>
†B<0101000000100011>
†B<0010000110111111>
†B<0011000011000110>
†B<0101000000001011>
†B<0000000100000000>

```

:SEND BCC 1

: (WE GOT HERE FROM TRANSMIT SERVICE. THE MASTER SCAN IS IN THE RAM ADDRESS REGISTER 0-3. THE LINE PROTOCOL THE A REGISTER AND THE ALU RESULT REGISTER.)

```

SBC1 RAM 0,0,16 :OBTAIN LINE PROTOCOL
XFR 13,1 :MOVE RAM OUTPUT TO A REGISTER
ALU 77 :LET ALU RESULT = A PLUS 1
RAM 1,17,16 :MOVE ALU RESULT TO RAM INPUT DATA
BRB 16,SBC1 :TEST FOR WRITE INHIBIT, IF YES
RAM 0,0,6 :OBTAIN TRANSMITTER BCC
XFR 13,0 :MOVE RAM OUTPUT DATA TO TRANSMIT
RAM 0,0,12 :OBTAIN TRANSMITTER DLE/LINE PRO
BRB 3,GCIDL :TEST RAM OUTPUT 03, IF YES BRAN
BRB 4,GCIDL :TEST RAM OUTPUT 04, IF YES BRAN
BRA 1,C/LL1 :TEST FOR SURE TRUE, IF YES BRAN
GCIDL BRA 1,ILOOP :TEST FOR SURE TRUE, IF YES BRAN

```

:SEND BCC2

: (WE GOT HERE FROM TRANSMIT SERVICE. THE MASTER SCAN IS IN THE RAM ADDRESS REGISTER 0-3. THE LINE PROTOCOL THE A REGISTER AND IN THE ALU RESULT REGISTER.)

```

SBC2 RAM 0,0,6 :OBTAIN TRANSMITTER BCC
XFR 13,2 :MOVE RAM OUTPUT DATA TO REGISTER
XFR 10,0 :MOVE REGISTER B 9-15/0-7 TO TRANSMIT
C/LL1 RAM 1,0,6 :MOVE ZERO TO RAM INPUT DATA AND
RAM 0,0,16 :OBTAIN LINE PROTOCOL
S/C 5,1 :CLEAR RAM BIT 01 (SEND BCC 2)
RAM 1,13,16 :MOVE RAM INPUT TO RAM INPUT DATA
BRB 16,C/LL1 :TEST FOR WRITE INHIBIT, IF YES BRAN
BRA 1,ILOOP :TEST FOR SURE TRUE, IF YES BRAN

```

:RECEIVED ERRORS

:CONTROL BYTE INTERRUPT

```

CBINT RAM 0,0,17 :READ CONTROL BYTE HOLDING REGISTER
S/C 5,3 :CLEAR RAM 00 (GENERATE INTERRUPT)
RAM 1,13,17 :WRITE CONTROL BYTE HOLDING REGISTER
XFR 14,6 :MOVE SILC OUT TO RICA REGISTER
S/C 3,3 :SET SCRD7 (RECEIVER INTERRUPT)
BRA 1,ILOOP :TEST FOR SURE TRUE, IF YES BRAN

```

H07

```
025512 030306          84700
                        84800
                        84900
                        85000  ↑B<0C11000011000110>
                        85100
                        85200
                        85300
                        85400
                        85500
025514 020017          85600  ↑B<0010000000001111>
025516 050043          85700  ↑B<0101000000100011>
025520 050041          85800  ↑B<0101000000100001>
025522 050042          85900  ↑B<0101000000100010>
025524 050040          86000  ↑B<0101000000100000>
025526 050207          86100  ↑B<0101000010000111>
025528 020577          86200  ↑B<0010000110111111>
025530 050013          86300  ↑B<0101000000001011>
025534 000400          86400  ↑B<0000000100000000>
                        86500
                        86600
                        86700
                        86800

:PARITY AND OVERRUN ERRORS
PCER XFR .14.6 ;MOVE SILO OUT TO RICR REGISTER

:CREATE NULL ACTION CONTROL BYTE (MODE IS PRESERVED)
CNACB RAM 0,0,17 ;READ CONTROL BYTE HOLDING REGIS
S/C 5,3 ;CLEAR RAM 00
S/C 5,1 ;CLEAR RAM 01
S/C 5,2 ;CLEAR RAM 02
S/C 5,0 ;CLEAR RAM 03
S/C 7,7 ;SET RAM OUTPUT 04 (DISCARD)
RAM 1,13,17 ;WRITE CONTROL BYTE HOLDING REGI
S/C 3,3 ;SET SCR 07 (RECEIVER INTERRUPT)
BRA 1,1LOOP ;TEST FOR SURE TRUE. IF YES BRAN

:END
```

```

4472 025536 000000
4473 025536 000000
4474 025540 000000
4475 025542 000000
4476 025544 000000
4477 025546 000000
4478
4479
4480
4481
4482

```

```

00100
00200
00300
00400
00500
00600
00700
00800
00900
01000
01100
01200
01300
01400
01500
01600
01700
01800
01900
02000
02100
02200
02300
02400
02500
02600
02700
02800
02900
03000
03100
03200
03300
03400
03500
03600
03700
03800
03900
04000
04100
04200
04300
04900
05000
05100
05200
05300

```

```

ENDROM:
NPRLOC: 0
COUNT: 0
DATA: 0
EXPRBA: 0
EXPRWC: 0

```

SYMBOL TABLE
[IN ORDER AS THEY APPEAR IN PROGRAM]

000000000	ILOOP	000000101	ILOP2	000001000	ILOPS	000001010	RSERV
000001111	S/ACT	000010001	SACT1	000010101	CLRRF	000011000	SACT2
000011110	TESTX	000100001	TMD	000100101	S/RDE	000101001	ISERV
000101110	RSYNC	000110011	PSI	000111010	TMARK	000111100	TFRF
000111110	CRAM7	001000011	SSERV	001010011	ZETA	001011101	RBUS1
001100010	CTEST	001101000	EPSIL	001101001	RRBCC	001101110	RBUS2
001110000	ORBC	001110101	ORCA	001111110	DDCMR	010000001	DDCM2
010000011	DISC	010000101	RBCC	010001100	CRBCO	010001111	NBCO
010010011	MCBCX	010011011	EBCC	010100000	EBCN	010100101	TBC1
010110011	MRTHA	010111000	TBC1X	010111010	TBC2	011000100	BCCCK
011010111	RMPEC	011011010	RNXMC	011011011	GAMMA	011011100	BETA
011100000	RNXM	011100010	NPRSO	011100100	TSERV	011101101	SIGMA
011110010	USCA	011110101	OXCB	011110111	RBUS3	100000000	PI
100001000	RBUS4	100001110	RDLE	100010000	RSSBN	100010001	RXBCC
100010010	ALPHA	100010101	UPBC	100011011	OPCA	100100011	USBC
100101001	OSCA	100110001	TNXMC	100110010	IOTA	100111001	TMPEC
100111010	OMEGA	101000000	XPBCO	101001000	RED	101001001	OTMB
101010000	XSBCO	101010111	CBCO	101011010	DELTA	101011101	ESS
101011111	C/GO	101100100	ITYPE	101100111	BCCG	101101001	SIDLE
101101110	MU	101110011	SDLE	101111011	NU	101111101	GRAM2
110000010	SSBN	110000111	BCOSB	110001100	DDCMX	110001111	XBCC
110010110	SBC1	110100001	GOICL	110100010	SBC2	110100101	C/LU1
110101011	CBINT	110110001	POER	110110010	CNACB		

NUMBER OF TAGS FOUND: 91

LAST ROM ADDRESS USED: 110111010

INSTRUCTION	NUMBER OF TIMES USED.
BRA	78
ALU	25
RAM	124
XFR	67
NPR	4
S/C	65
BCC	4
BRB	76

```

4483          00100
4484          00200
4485 025550 051377 040505 020104 00600
      025616 021377 051106 042505 00700
      025666 042777 051122 051117 00800
      025727      377 043042 042522 00900
      026000 051377 046517 040440 01000
      026032 042777 050130 041505 01100
      026101      377 054105 042520 01200
          01300
          01700
4486 026152 000004          01800
4487 026154      006      004      01800
4488 026156 001272          01900
4489 026160      006      002      02000
4490 026162 001270          02100
4491 026164      002      006      02200
4492 026166 001260          02300
4493 026170      002      001      02400
4494 026172 001262          02500
4495 026174 000004          02600
4496 026176      006      004      02700
4497 026200 001272          02800
4498 026202      006      002      02900
4499 026204 001270          03000
4500 026206      002      006      03100
4501 026210 001260          03200
4502 026212      006      001      03300
4503 026214 001262          03400
4504          03500
4505 026216 000003          03600
4506 026220      003      006      03700
4507 026222 001264          03800
4508 026224      006      004      03900
4509 026226 001272          04000
4510 026230      006      001      04100
4511 026232 001270          04200
4512 026234          04300
4513 026234 025666          04400
4514 026236 000000          04500
4515 026240 000000          04600
4516 026242 025550          04700
4517 026244 026000          04800
4518 026246 026216          04900
4519 026250 025616          05000
4520 026252 026032          05100
4521 026254 026174          05200
4522 026256 025727          05300
4523 026260 026101          05400
4524 026262 026152          05500
4525          05600
4526 026264          05700
4527          000001          05800
          06300

```

```

EM1: .ASCIZ <377>/READ OF ROM PRODUCED A COMPARE ERROR/
EM2: .ASCIZ <377>/"FREE RUNNING" PRIMARY REGISTER ERROR./
EM2A: .ASCIZ <377>/ERROR! SEE LISTING FOR DETAILS./
EM3: .ASCIZ <377>/"FREE RUNNING" SECONDARY REGISTER ERROR/
DH1: .ASCIZ <377>/ROM ADD EXPECTED FOUND/
DH2: .ASCIZ <377>/EXPECTED FOUND LINE(9) PRIMARY REG/
DH2A: .ASCIZ <377>/EXPECTED FOUND LINE(8) SECONDARY REG/
.EVEN
DT1: 4
      .BYTE 6.4
      SAVR5
      .BYTE 6.2
      SAVR4
      .BYTE 2.6
      SAVR0
      .BYTE 2.1
      SAVR1
DT2: 4
      .BYTE 6.4
      SAVR5
      .BYTE 6.2
      SAVR4
      .BYTE 2.6
      SAVR0
      .BYTE 6.1
      SAVR1
DT1A: 3
      .BYTE 3.6
      SAVR2
      .BYTE 6.4
      SAVR5
      .BYTE 6.1
      SAVR4
.ERRTAB:
EM2A
0
0
EM1
DH1 :HALT 1
DT1A
EM2
DH2 :HALT 2
DT2
EM3
DH2A :HALT 3
DT1
:*****
CORMAX:
.END

```


DV.END	001740	993#	1517	1526	1655					
DV.MAP	001500	695	804#	909	936	1519	1529	1653	1658	1707
DV00.A	001504	807#								
DV00.B	001510	809#								
DV00.C	001514	911#								
DV00.D	001520	913#								
DV01.A	001530	818#								
DV01.B	001534	820#								
DV01.C	001540	822#								
DV01.D	001544	824#								
DV02.A	001554	829#								
DV02.B	001560	831#								
DV02.C	001564	833#								
DV02.D	001570	835#								
DV03.A	001600	840#								
DV03.B	001604	842#								
DV03.C	001610	844#								
DV03.D	001614	846#								
DV04.A	001624	851#								
DV04.B	001630	853#								
DV04.C	001634	855#								
DV04.D	001640	857#								
DV05.A	001650	862#								
DV05.B	001654	864#								
DV05.C	001660	866#								
DV05.D	001664	868#								
DV06.A	001674	873#								
DV06.B	001700	875#								
DV06.C	001704	877#								
DV06.D	001710	879#								
DV07.A	001720	884#								
DV07.B	001724	886#								
DV07.C	001730	888#								
DV07.D	001734	890#								
EM1	025550	4485#	4516							
EM2	025616	4485#	4519							
EM2A	025666	4485#	4513							
EM3	025727	4485#	4522							
ENDROM	025536	1765	4476#							
ERRCNT	001232	666#	911#	1033	1351*					
ERRFLG	001311	701#	907#	995*	1062*	1303*	1316	1330*	1385*	
ERRMSG	004252	1313*	1331	1334#						
ERTAB0	004366	1328	1360#							
EXIT =	000205	605#	3689	3703	3722	3729				
EXITER	004322	1346	1351#							
EXPRBA	025544	3142*	3192*	3242*	3292*	3342*	3467	4480#		
EXPRWC	025546	3143*	3193*	3243*	3293*	3343*	3474	4481#		
FIX.OO	006516	1570	1575	1580	1585	1619#				
HALTS	004302	1299	1345#							
HILIM	003436	1138*	1165	1183#						
ICOUNT	001222	662#	1060	1065*						
INBUF	005520	1108	1144	1491#						
INIFLG	001310	700#	916	931*						
INSTR=	104404	723#	1159							
INSTR =	104403	721#	1592							
INSTR2	003236	1115	1127#							

R1	*:000001	2999*	3000	3013*	3014	3030*	3032	3036	3041*	3048*	3050	3054	3059*	3065*
		3069	3072	3077*	3084*	3086	3090	3095*	3124*	3129*	3132*	3136*	3174*	3178*
		3182*	3186*	3224*	3228*	3232*	3236*	3274*	3278*	3282*	3286*	3324*	3328*	3332*
		3336*	3372	3438	3445	3451	3485*	3499*	3500	3502*	3507*	3508	3520*	3524*
		3525	3530	3550*	3561*	3562	3564*	3569*	3570	3572*	3573	3585*	3589*	3593*
		3595	3617	3631*	3637	3644*	3646*	3647	3650*	3651*	3652	3655*	3658*	3659*
		3662	3668*	3678	3680*	3682	3688*	3694	3695*	3699*	3702*	3719*	3721*	3725*
		566*	961*	962	963*	964	1011*	1015	1199	1206*	1218	1222*	1224	1225
		1226	1227	1259*	1403	1405*	1409*	1411*	1568*	1573*	1578*	1583*	1623*	1628*
		1633*	1636*	1659*	1661	1663	1665	1668	1691*	1682	1688*	1689	1693*	1703*
		1710	1711*	1712	1713	1810*	1812*	1843*	1844	1851*	1852	1858*	1859	1863*
		1854	1875*	1880*	1888*	1893*	1899*	1950*	1952*	1983*	1984	1991*	1992	1999*
		1999	2003*	2004	2016*	2021*	2029*	2034*	2040*	2120*	2121	2129*	2130	2135*
		2136	2142*	2148*	2154*	2232*	2233	2390*	2474*	2558*	2544*	2741*	2742	2777*
		2781*	2784*	2787*	2790*	2792	2875*	2879*	2882*	2895*	2988*	2990	2999*	2973*
		2976*	2979*	2982*	2984	3037*	3055*	3073*	3091*	3437*	3449*	3454*	3459*	3465*
		3472*	3479*	3505*	3510*	3513	3516*	3527*	3537*	3542*	3557*	3575*	3578	3581*
		3592*	3602*	3607*	3619*	3624*	3638	3656*	3657	3658	3667*	3679	3681*	3685
		3687*	3712*	3715*	3719									
R2	*:000002	567*	1198	1207*	1569*	1574*	1579*	1584*	1624*	1629*	1634*	1637*	1640*	1653*
		1654*	1655	1658*	1668*	1669	1670*	1671*	1672*	1673*	1674*	1675*	1676*	1677*
		1684*	1707*	1719*	1723*	1724*	1725*	1726*	1728*	1739*	1756*	1768*	1814*	1907*
		1954*	2048*	2091*	2163*	2204*	2311*	2352*	2396*	2436*	2480*	2520*	2564*	2604*
		2650*	2685*	2750*	2793*	2794	2795*	2808*	2821*	2824*	2920*	2923*	2991*	2994
		2995*	3031*	3042*	3049*	3060*	3067*	3078*	3085*	3096*	3504*	3508	3515*	3517*
		3549*	3566*	3570	3573	3580*	3582*	3630*	3639	3657*	3659*	3660	3666*	3667*
R3	*:000003	568*	1102	1109*	1119*	1122*	1124	1128*	1197	1208*	1219	1231*	1232*	1233*
		1234	1243*	1244*	1249*	1252*	1258*	1619*	1620*	1621	1626	1631	1857*	1859*
		1997*	2009*	2636*	2640*	2708*	2718*	2995*	2999*	2993*	2996*	3503*	3521*	3522*
		3551*	3565*	3586*	3588*	3632*	3706	3708*	3716*	3719*				
R4	*:000004	563*	1103	1108*	1112*	1113*	1114	1121*	1125	1127*	1135	1144*	1145	1147
		1149	1151*	1152	1153	1174*	1175*	1179*	1196	1209*	1220	1228*	1231	1238*
		1238*	1240*	1257*	1307*	1308*	1309*	1310*	1311*	1312*	1313	1314	1315	1404*
		1406*	1407*	1410*	1760*	1761	1844*	1845	1852*	1859*	1860	1864*	1874*	1876
		1881*	1889*	1894*	1900*	1901	1984*	1986	1992*	1999*	2000	2004*	2015*	2017*
		2022*	2030*	2035*	2041*	2042	2121*	2123	2130*	2131	2136*	2140*	2143	2149*
		2150*	2156*	2157	2232*	2236	2269*	2271	2303*	2306	2394*	2391	2468*	2475*
		2552*	2553	2638*	2645	2737*	2739*	2742*	2743	2745	2815*	2817*	3034*	3039*
		3052*	3056	3070*	3074	3088*	3092	3431*	3433	3436*	3441	3444*	3447	3458*
		3455	3460*	3466*	3468	3473*	3475	3480*	3482	3506*	3519*	3528*	3532	3538*
		3543*	3545	3568*	3583*	3593*	3597	3603*	3609*	3610	3615*	3620	3625*	3638*
R5	*:000005	570*	1086	1087*	1091	1096	1098*	1134	1136*	1137	1138	1139	1140	1141
		1142	1143*	1152*	1155*	1156*	1157*	1165	1167	1169	1175	1176*	1180*	1195
		1210*	1221	1229*	1241*	1256*	1305*	1306*	1307	1309	1759*	1761	1809*	1811*
		1837*	1841*	1845*	1846	1853*	1855*	1856*	1860	1866*	1972*	1876	1893*	1897*
		1897*	1901	1949*	1951*	1977*	1981*	1985*	1996	1993*	1995*	1996*	2000	2005*
		2012*	2017	2024*	2028*	2038*	2042	2114*	2118*	2122*	2123	2127*	2128*	2131*
		2134*	2141*	2143	2146*	2150	2153*	2157	2225*	2229*	2234*	2235*	2236*	2237*
		2265*	2269*	2270*	2271	2296*	2300*	2304*	2305*	2306	2349*	2350	2351*	2352*
		2381*	2385*	2389*	2391	2433*	2434	2435*	2461*	2465*	2469*	2473*	2475*	2476*
		2518	2519*	2545*	2549*	2553*	2557*	2559	2601*	2602	2603*	2629*	2633*	2634*
		2645	2743*	2744*	2745	2812*	2828*	2834*	2839*	2842*	2846*	2916*	2921*	2922*
		2937*	2941*	2945*	3016*	3023*	3035*	3036*	3038	3053*	3054*	3056	3071*	3072*
		3074	3089*	3090*	3092	3144*	3194*	3244*	3294*	3344*	3357	3358	3359	3360*
		3361	3362	3363*	3366*	3367	3418*	3422*	3432*	3433	3439*	3439*	3440*	3441*
		3445*	3446*	3447	3453*	3455	3452*	3457*	3468	3474*	3475	3481*	3482	3483*

SY109	001000	549#	1076							
SY110	002000	549#	1354							
SY111	004000	547#	1055							
SY112	010000	546#	1089	1293						
SY113	020000	545#	1298							
SY114	040000	544#								
SY115	100000	543#								
SY700	001506	808#								
SY701	001532	819#								
SY702	001558	820#								
SY703	001602	841#								
SY704	001626	852#								
SY705	001652	863#								
SY706	001678	874#								
SY707	001722	885#								
SY708	001512	810#								
SY709	001538	821#								
SY710	001562	832#								
SY711	001606	843#								
SY712	001632	854#								
SY713	001658	865#								
SY714	001702	876#								
SY715	001728	887#								
SYNC	021346	3282#	3724*	3725*	3728*	3732*				
SYNCX	001240	673#								
SYNCO0	001516	812#								
SYNCO1	001542	823#								
SYNCO2	001566	834#								
SYNCO3	001512	845#								
SYNCO4	001636	856#								
SYNCO5	001662	867#								
SYNCO6	001706	878#								
SYNCO7	001732	889#								
SYNC2A	001426	784#	1533*							
SYNC2B	001430	785#	1535*							
SYNC2C	001432	786#	1537*							
SYNC2D	001434	787#	1539*							
SYNC00	001522	814#								
SYNC01	001546	825#								
SYNC02	001572	836#								
SYNC03	001616	847#								
SYNC04	001642	858#								
SYNC05	001666	869#								
SYNC06	001712	880#								
SYNC07	001736	891#								
SYNC08	050000	601#								
TEMP	005562	1230	1380*	1381*	1493#					
TEMP1	001246	676#	936*	937	942*	1484	1715*	1716*	3640*	3663*
TEMP2	001250	677#	937*	938	1485	3641*	3645*			
TEMP3	001252	678#	3542*	3644	3654*	3656	3661*	3662*	3665	
TEMP4	001254	679#								
TEMP5	001256	680#								
TKCER	001204	651#	1051	1110	1436	1443	1464			
TKCER	001206	652#	1041	1053	1112	1118	1288	1445	1466	
TPCER	001210	1612	4482#							
TPCER	001210	653#	1094	1116	1295	1450				

F08

DZDVC-C MACY11 27(732) 17-SEP-76 11:40 PAGE 99
 DZDVCC.P11 CROSS REFERENCE TABLE -- USER SYMBOLS

TPDR	001212	554*	1096*	1118*	1297*	1452*								
TRPOK	002762	1276*												
TSTNO	001226	664*	913*	1365	1392	1597	1604	1606	1750*	1788*	1928*	2063*	2122*	2327*
		2411*	2495*	2579*	2664*	2774*	2872*	2966*	3122*	3172*	3222*	3272*	3322*	
TST1	007256	1600	1616	1750*										
TST10	013154	2412	2495*											
TST11	013520	2496	2579*											
TST12	014064	2580	2664*											
TST13	014506	2665	2774*											
TST14	015034	2775	2872*											
TST15	015400	2873	2966*											
TST16	016176	2967	3122*											
TST17	016350	3123	3172*											
TST2	007372	1751	1788*											
TST20	016522	3173	3222*											
TST21	016674	3223	3272*											
TST22	017046	3273	3322*	4482										
TST23	= *****	3323												
TST3	010160	1799	1928*											
TST4	010754	1929	2069*											
TST5	011434	2070	2182*											
TST6	012244	2183	2327*											
TST7	012610	2328	2411*											
TTST	002702	978*	979*	981*	982*	1049*								
TWOSYN=	010000	605*	3726											
TXBAF	021350	1819	1821*	1872	2282	2350*	2356	2434*	2440	2518*	2524	2602*	2608	2668
		2696*	2722	2793	2814	2818	2891	2992	2998	3377	3414*	3453	3529	3594
		3733*												
TXBAS	021750	1959	1961*	2012	2815	2892	3616	3734*						
TXTAB	022350	1809	1820	1949	1960	2097	2211	2247	2351*	2361	2435*	2445	2519*	2523
		2603*	2613	2693	2695*	2806	2813*	2906	2918*	2985	3010	3397	3415*	3733*
TYPCAT	004266	1319	1337	1340*										
TYPE =	104402	719*	930	935	948	953	977	985	39	999	1001	1003	1005	1093
		1106	1123	1216	1252	1320	1321	1324	1325	1327	1329	1333	1338	1393
		1440	1442	1470	1508	1591	1609	1614	1698					
TYPMSG	004166	1317	1320*											
VECMAP	007102	1697	1705*											
WADCNT	003742	1224*	1254*	1262*										
WPKO.F	004254	1332	1335*											
XBX	004060	1294	1296	1298*										
XCSR	002604	1000	1022*											
XERR	002626	1006	1031*											
XFR =	030000	599*												
XHEAD	005461	935	1482*											
XPASS	002620	1004	1028*											
XPOLY	021020	2348*	2432*	2516*	2600*	3650	3661	3670*						
XSTATG	005536	941	1482*											
XTSTN	004374	1326	1363*											
XVEC	002612	1002	1025*											
SCRAP =	177777	1*	1736*	1746*	1773*	1784*	1913*	1924*	2054*	2065*	2169*	2178*	2317*	2323*
		2401*	2407*	2485*	2491*	2569*	2575*	2654*	2660*	2755*	2770*	2850*	2868*	2949*
		2962*	3103*	3118*	3153*	3168*	3203*	3218*	3253*	3268*	3303*	3319*	3335*	3351*
SE =	000024	1*	1751	1752*	1789	1790*	1929	1930*	2070	2071*	2182*	2194*	2328	2329*
		2412	2413*	2496	2497*	2580	2581*	2665	2666*	2775*	2776*	2874*	2875*	2961*
		2968*	3123	3124*	3173	3174*	3223	3224*	3273	3274*	3323*	3324*	3372*	3373*
SN =	000022	1*	1736	1748	1752*	1773	1786	1790*	1913	1926	1930*	2054	2067	2271*

ADC	2646														
ADC8	1515	1523													
ADC	9422	1088	1105	1176	1223	1233	1278	1309	1312	1408	1516	1525	1546	1548	1554
	1556	1558	1561	1563	1565	1681	1726	2781	2784	2787	2790	2879	2882	2885	2888
	2917	2973	2975	2979	2982	2997	3036	3054	3072	3090	3530	3531	3595	3596	3617
	3618														
ASL	1155	1156	1157	1276	1308	1310									
ASL	1428	1717													
ASL	1457														
	939	947	976	1012	1040	1049	1058	1077	1079	1115	1146	1154	1248	1287	1294
	1301	1317	1323	1332	1337	1341	1355	1448	1587	1639	1680	1697	1762	1766	1827
	1847	1850	1861	1877	1892	1890	1895	1902	1908	1967	1987	1990	2001	2018	2023
	2031	2036	2043	2049	2104	2124	2132	2137	2144	2151	2158	2164	2217	2237	2253
	2272	2288	2307	2312	2367	2392	2451	2476	2535	2560	2619	2639	2646	2698	2711
	2716	2719	2733	2746	2826	2925	3021	3039	3057	3075	3093	3374	3403	3434	3442
	3448	3456	3461	3469	3476	3483	3487	3509	3514	3533	3539	3546	3571	3574	3579
	3598	3604	3611	3621	3626	3648	3709	3727							
BGT	1150	1461													
BGT	1166														
BIC	958	1042	1232	1277	1289	1311	1446	1462	1467	1620	1724	1729	1871	2011	2098
	2126	3026	3507	3569	3652	3658	3659	3651	3684						
BIC8	1113	1151													
BIS	1419	1425	1463	1670	1671	1672	1673	1674	1675	1676	1677	1723	1728	1758	1767
	1856	1996	2093	2128	2207	2235	2243	2270	2278	2305	2744	3386	3393	3440	3446
	3502	3564	3572	3660	3662	3693	3707								
BIS8	1152														
BIT	946	975	1048	1055	1076	1089	1293	1298	1352	1354	1436	1586	1638	1826	1966
	2103	2216	2252	2287	2366	2450	2534	2618	2697	2710	2715	2732	3373	3402	3425
	3647	3726													
BIT8	1169	1511													
BLO	1168														
BLOS	952	1714													
BLT	1148	1459													
BMI	933	1732	1796	1800	1804	1839	1932	1936	1940	1944	1979	2073	2077	2081	2085
	2116	2186	2190	2194	2198	2227	2263	2298	2331	2335	2339	2343	2379	2415	2419
	2423	2427	2463	2499	2503	2507	2511	2547	2593	2597	2591	2595	2631	2668	2672
	2676	2680	2780	2783	2786	2789	2833	2837	2841	2845	2878	2891	2884	2887	2932
	2936	2940	2944	2972	2975	2978	2991	3029	3047	3065	3083	3126	3130	3134	3138
	3176	3180	3184	3188	3226	3230	3234	3238	3276	3280	3284	3289	3326	3330	3334
	3338	3420	3429												
BNE	917	945	966	974	1008	1044	1056	1061	1090	1097	1120	1170	1178	1242	1246
	1251	1255	1291	1299	1319	1353	1382	1396	1409	1430	1437	1469	1507	1512	1519
	1528	1590	1603	1605	1607	1613	1622	1627	1632	1656	1662	1664	1666	1683	1694
	1722	1813	1842	1870	1953	1982	2010	2119	2230	2266	2301	2392	2397	2466	2481
	2550	2565	2634	2641	2651	2740	2751	2811	2819	2829	2915	2928	2990	2997	3015
	3024	3043	3061	3079	3097	3368	3385	3392	3423	3426	3511	3519	3522	3552	3576
	3584	3597	3633	3664	3700	3717									
BPL	1052	1092	1095	1111	1117	1296	1346	1444	1451	1465	1865	2005	2923	2922	3019
	3697														
BR	924	943	955	980	1050	1054	1126	1158	1160	1373	1510	1520	1610	1615	1625
	1630	1635	1701	1727	1769	1833	1973	2110	2223	2259	2294	2373	2457	2541	2625
	2704	2714	2726	2736	3379	3411									
CLC	1235	1237	1239	1453	1513	1521	1690	3653	3720						
CLP	906	911	912	920	949	963	994	1046	1063	1064	1143	1380	1386	1407	1424
	1449	1654	1699	1718	1720	1725	1756	1810	1821	1837	1853	1883	1887	1950	1961
	1977	1993	2024	2028	2114	2134	2142	2225	2261	2296	2377	2461	2545	2629	2643

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DZDVOC-C MACY11 27(732) 17-SEP-76 11:40 PAGE 105
 DZDVOC.P11 CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

	2695	2696	2777	2791	2812	2813	2816	2817	2875	2889	2916	2918	2969	2983	2999
CLRB	3016	3415	3418	3454	3462	3527	3535	3592	3600	3609	3627	3643	3695	2983	2894
	907	908	995	1052	1252	1303	1385	1623	1657	1685	1811	1951	2795	2893	2894
OMP	3526	3591	3728												
	925	939	964	965	1039	1060	1165	1167	1286	1300	1458	1460	1517	1526	1601
	1604	1606	1612	1626	1631	1655	1663	1682	1712	1713	1730	1751	1765	1846	1850
	1875	1901	1986	2000	2017	2042	2123	2131	2143	2150	2157	2236	2271	2306	2391
	2475	2559	2645	2745	2810	2818	2914	3014	3038	3056	3074	3092	3367	3384	3391
OMP8	3433	3441	3447	3455	3468	3475	3482	3509	3532	3545	3570	3573	3597	3610	3620
COM	951	1043	1114	1145	1147	1149	1153	1290	1447	1468	1679				
COMB	3649	3651													
DEC	931														
	1119	1241	1254	1395	1693	1869	1907	2009	2048	2163	2311	2396	2480	2564	2640
	2650	2718	2739	2750	2825	2924	2989	2996	3020	3042	3050	3078	3096	3496	3510
	3518	3521	3551	3575	3583	3586	3632	3663	3716						
DECB	1007	1177	1245	1250											
EMT	579														
HALT	617	950	954	959	1349	1372	1509	1700							
INC	996	1059	1351	1381	1429	1542	1544	1550	1552	1721	1768	1836	1841	1880	1893
	1906	1976	1981	2021	2034	2047	2113	2118	2148	2162	2224	2229	2260	2255	2295
	2300	2310	2376	2381	2395	2460	2465	2479	2544	2549	2563	2628	2633	2649	2707
	2749	2908	2909	2820	2828	2911	2912	2913	2919	2927	2995	3012	3013	3017	3023
	3041	3059	3077	3095	3417	3422	3459	3472	3485	3520	3537	3549	3550	3585	3602
	3624	3630	3631	3699	3712	3715									
INCB	1540	1678	1692	1812	1879	1892	1952	2020	2033	2147	3458	3471	3536	3601	3623
JMP	639	986	1021	1069	1280	1358	1389	1617	1697	1909	2050	2165	2313	3488	
JSR	934	1015	1045	1292	1570	1575	1580	1595	1793	1797	1801	1805	1933	1937	1941
	1945	2074	2078	2082	2086	2187	2191	2195	2199	2332	2335	2340	2344	2385	2416
	2420	2424	2428	2469	2500	2504	2508	2512	2553	2584	2588	2592	2596	2669	2673
	2677	2681	2834	2838	2842	2846	2933	2937	2941	2945	3127	3131	3135	3139	3144
	3177	3181	3185	3189	3194	3227	3231	3235	3239	3244	3277	3281	3285	3289	3294
	3327	3331	3335	3339	3344										
MCV	902	903	904	909	913	914	918	919	921	926	927	928	929	936	937
	960	961	962	971	972	978	979	981	982	984	997	1011	1020	1041	1047
	1053	1065	1066	1067	1080	1086	1087	1098	1102	1103	1104	1108	1109	1118	1121
	1122	1124	1125	1127	1128	1134	1135	1136	1137	1138	1139	1142	1144	1174	1175
	1179	1180	1191	1195	1196	1197	1198	1199	1200	1205	1206	1207	1208	1209	1210
	1217	1218	1219	1220	1221	1222	1224	1227	1228	1230	1231	1243	1256	1257	1258
	1259	1260	1273	1275	1279	1288	1302	1305	1307	1313	1314	1315	1348	1356	1357
	1371	1378	1379	1393	1394	1397	1402	1403	1404	1405	1406	1410	1411	1415	1423
	1426	1432	1438	1439	1445	1452	1456	1519	1524	1529	1530	1531	1532	1533	1534
	1535	1536	1537	1538	1539	1540	1541	1543	1545	1547	1549	1551	1553	1555	1557
	1560	1562	1564	1567	1568	1569	1572	1573	1574	1577	1578	1579	1582	1583	1584
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	1707	1708	1709	1710	1711	1719	1731	1750	1751	1753	1754	1755	1757	1759	1760
	1788	1789	1790	1791	1794	1795	1798	1799	1802	1803	1809	1814	1815	1843	1844
	1845	1851	1852	1855	1857	1858	1859	1863	1864	1866	1872	1873	1874	1881	1885
	1889	1894	1897	1900	1928	1929	1930	1931	1934	1935	1938	1939	1942	1943	1949
	1954	1955	1983	1984	1985	1991	1992	1995	1997	1998	1999	2003	2004	2006	2012
	2013	2015	2022	2026	2030	2035	2038	2041	2069	2070	2071	2072	2075	2076	2079
	2080	2083	2084	2090	2091	2092	2120	2121	2122	2127	2129	2130	2135	2136	2139
	2140	2141	2146	2149	2153	2154	2156	2182	2183	2184	2185	2188	2189	2192	2193
	2196	2197	2203	2204	2206	2232	2233	2234	2240	2242	2269	2269	2275	2277	2303
	2304	2327	2328	2329	2330	2333	2334	2337	2338	2341	2342	2348	2349	2352	2353
	2384	2389	2411	2412	2413	2414	2417	2419	2421	2422	2425	2426	2432	2432	2436
	2437	2469	2473	2495	2496	2497	2498	2501	2502	2505	2506	2509	2510	2516	2517

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DZDVCC-C MACY11 27,732) 17-SEP-76 11:40 PAGE 106
 DZDVCC.P11 CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

	2520	2521	2552	2557	2579	2580	2581	2582	2585	2586	2589	2590	2593	2594	2600
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	2685	2686	2708	2725	2737	2741	2742	2743	2774	2775	2778	2792	2793	2794	2796
	2814	2815	2821	2824	2872	2873	2876	2890	2891	2892	2895	2920	2923	2966	2967
	2970	2994	2985	2986	2991	2992	2993	2998	3000	3030	3031	3032	3034	3035	3048
	3049	3050	3052	3053	3066	3067	3068	3070	3071	3084	3085	3096	3088	3089	3122
	3123	3124	3125	3128	3129	3132	3133	3136	3137	3142	3143	3172	3173	3174	3175
	3178	3179	3182	3183	3186	3187	3192	3193	3222	3223	3224	3225	3228	3229	3232
	3233	3236	3237	3242	3243	3272	3273	3274	3275	3278	3279	3282	3283	3286	3287
	3292	3293	3322	3323	3324	3325	3328	3329	3332	3333	3336	3337	3342	3343	3357
	3358	3359	3360	3361	3362	3363	3364	3370	3414	3431	3432	3436	3437	3438	3444
	3445	3449	3451	3452	3453	3460	3466	3467	3473	3474	3479	3480	3481	3483	3499
	3500	3501	3503	3504	3505	3506	3515	3516	3517	3523	3524	3525	3528	3529	3538
	3542	3543	3544	3553	3561	3562	3563	3565	3566	3567	3568	3580	3581	3582	3588
	3589	3590	3593	3594	3603	3607	3608	3615	3616	3625	3634	3637	3638	3639	3640
	3641	3642	3644	3650	3655	3656	3657	3665	3666	3667	3668	3678	3679	3683	3686
	3687	3688	3692	3694	3702	3706	3708	3710	3713	3718	3719				
MOV8	905	910	956	957	1009	1010	1095	1112	1140	1141	1225	1226	1229	1234	1244
	1249	1297	1330	1624	1628	1629	1633	1634	1636	1637	1688	1699	1696	1715	1816
	1875	1886	1888	1898	1899	1956	2014	2016	2027	2029	2039	2040	2155	2350	2351
	2283	2390	2434	2435	2467	2474	2518	2519	2551	2558	2602	2603	2635	2644	2709
	2724	2731	2988	2994	3033	3037	3051	3055	3069	3073	3087	3091	3366	3372	3424
	3464	3465	3478	3541	3606	3614	3619	3680	3681	3682	3685	3724	3725		
NOF	923	978	979	1016	1017	1018	1019	2797	2798	2799	2896	2897	2898	3001	3002
	3003														
RESET	993	1013	1652												
ROL	1454	1455	1456												
ROLB	1514	1522	1691												
ROR	1236	1238	1240	1716	3645	3654	3721								
RORB	1427														
RTI	1081	1099	1129	1181	1201	1211	1261	1359	1398	1412	1416	1420	1433	1703	1732
RTS	1471	1641	1733	1910	2051	2166	2314	2398	2482	2566	2652	2752	3150	3200	3250
	3300	3350	3490	3554	3635	3669									
SUB	1274	1306													
SWAB	3439														
TRAP	715	717	719	721	723	725	727	729	731	733	735	737	739	741	743
TST	922	944	973	1078	1318	1322	1331	1336	1340	1345	1599	1611	1621	1661	1665
	1669	1764	1838	1849	1868	1978	1989	2008	2115	2226	2262	2297	2378	2462	2546
	2520	2779	2782	2785	2788	2822	2832	2836	2840	2844	2877	2890	2883	2886	2921
	2931	2935	2939	2943	2971	2974	2977	2980	3018	3028	3046	3064	3082	3359	3513
	3578	3696													
TSTB	916	932	1051	1057	1091	1094	1110	1116	1247	1295	1316	1443	1450	1464	1505
	1686	3419	3428												
.ASCIZ	643	1473	1480	1482	4485										
.BLKB	689	690	691	692	693	3733	3734	3735	3736	3737					
.BLKW	628	629	630	805	806	807	808	809	810	811	812	813	814	816	817
	818	819	820	821	822	823	824	825	827	828	829	830	831	832	833
	834	835	836	838	839	840	841	842	843	844	845	846	847	849	850
	851	852	853	854	855	856	857	858	860	861	962	863	864	865	866
	867	868	869	871	872	873	874	875	876	877	878	879	880	882	883
	884	885	886	887	888	889	890	891	1434	2802	2901	2909	3006	3555	3636
	3731	3732													
.BYTE	700	701	702	703	769	770	771	772	774	775	776	777	1023	1026	1029
	1032	1361	1364	1391	1477	1483	1485	1598	1599	1918	1923	1959	1963	2095	2100
	2209	2213	2245	2249	2280	2284	2355	2359	2363	2439	2443	2447	2523	2527	2531
	2607	2611	2615	2688	2692	2721	2728	2801	2805	2900	2904	2908	3005	3009	3376

	3381	3398	3395	3399	4486	4488	4490	4492	4496	4499	4500	4502	4506	4508	4510
.ENABL	539														
.END	4527														
.ENDC	1735	1737	1747	1752	1774	1783	1785	1790	1828	1914	1923	1925	1930	1968	2055
	2066	2071	2105	2170	2179	2184	2218	2254	2289	2318	2324	2329	2368	2390	2402
	2408	2413	2452	2474	2486	2492	2497	2536	2558	2570	2576	2591	2620	2644	2655
	2661	2666	2699	2756	2771	2776	2851	2869	2874	2950	2963	2968	3104	3106	3115
	3116	3119	3124	3143	3144	3154	3155	3156	3165	3166	3169	3174	3193	3194	3204
	3205	3206	3215	3216	3219	3224	3243	3244	3254	3255	3256	3265	3266	3269	3274
	3293	3294	3304	3305	3306	3315	3316	3319	3324	3343	3344	3406	3549	3630	3739
	4477	4527													
.EQUIV	579														
.EVEN	694	705	1475	1481	1482	1487	4485								
.IF	525	1736	1746	1751	1773	1777	1784	1789	1828	1913	1917	1924	1929	1968	2054
	2065	2070	2105	2169	2178	2183	2218	2254	2289	2317	2320	2323	2328	2368	2401
	2404	2407	2412	2452	2485	2488	2491	2496	2536	2569	2572	2575	2580	2620	2654
	2660	2665	2699	2755	2770	2775	2850	2868	2873	2949	2962	2967	3103	3105	3106
	3114	3115	3118	3123	3142	3143	3153	3155	3156	3164	3165	3168	3173	3192	3193
	3203	3205	3206	3214	3215	3218	3223	3242	3243	3253	3255	3256	3264	3265	3268
	3273	3292	3293	3303	3305	3314	3315	3318	3323	3342	3343	3404	3497	3559	3739
	4477	4527													
.IFF	1737	1746	1751	1752	1774	1783	1784	1789	1790	1914	1917	1924	1929	1930	2055
	2065	2070	2071	2170	2178	2183	2184	2318	2320	2323	2328	2329	2384	2385	2402
	2404	2407	2412	2413	2468	2469	2486	2488	2491	2496	2497	2552	2553	2570	2572
	2575	2580	2581	2643	2644	2655	2660	2665	2666	2756	2770	2775	2776	2851	2869
	2873	2874	2950	2962	2967	2968	3104	3114	3115	3118	3123	3124	3142	3143	3154
	3165	3166	3168	3173	3174	3193	3194	3204	3214	3215	3218	3223	3224	3242	3243
	3254	3264	3265	3268	3273	3274	3292	3293	3304	3314	3315	3318	3323	3342	3343
	3498	3507	3510	3517	3544	3549	3559	3567	3572	3581	3609	3614			
.IFT	525	1735	1736	1746	1773	1777	1784	1913	1917	1924	2054	2065	2169	2178	2317
	2321	2323	2384	2385	2401	2405	2407	2468	2469	2485	2489	2491	2552	2553	2569
	2572	2575	2636	2643	2654	2660	2755	2770	2850	2868	2949	2962	3103	3114	3115
	3118	3142	3143	3153	3164	3165	3168	3192	3193	3203	3214	3215	3218	3242	3243
	3253	3264	3265	3268	3292	3293	3303	3314	3315	3318	3342	3343	3497	3505	3516
	3544	3559	3567	3581	3610										
.IFTF	525	2321	2405	2489	2573	3498	3507	3510	3517	3545	3560	3569	3575	3582	3610
.IIF	1751	1752	1789	1790	1791	1795	1799	1803	1823	1824	1856	1857	1874	1929	1930
	1931	1935	1939	1943	1963	1996	2014	2070	2071	2072	2076	2080	2084	2183	2184
	2185	2189	2193	2197	2328	2329	2330	2334	2338	2342	2412	2413	2414	2418	2422
	2426	2496	2497	2498	2502	2506	2510	2580	2581	2582	2586	2590	2594	2665	2666
	2667	2671	2675	2679	2775	2776	2873	2874	2967	2968	3123	3124	3125	3129	3133
	3137	3173	3174	3175	3179	3183	3187	3223	3224	3225	3229	3233	3237	3273	3274
	3275	3279	3283	3287	3323	3324	3325	3329	3333	3337					
.IRP	715	717	719	721	723	725	727	729	731	733	735	737	739	741	743
	805	1736	1748	1751	1773	1786	1789	1913	1926	1929	2054	2067	2070	2169	2180
	2183	2317	2325	2328	2401	2409	2412	2485	2493	2496	2569	2577	2580	2654	2662
	2665	2755	2772	2775	2850	2870	2873	2949	2964	2967	3103	3120	3123	3153	3170
	3173	3203	3220	3223	3253	3270	3273	3303	3320	3323	4482				
.LIST	1	525	539	560	579	605	607	617	641	643	717	719	721	723	725
	727	729	731	733	735	737	739	741	743	745	800	894	987	1035	1492
	1735	1736	1746	1752	1773	1784	1790	1913	1924	1930	2054	2065	2071	2169	2178
	2184	2317	2323	2329	2401	2407	2413	2485	2491	2497	2569	2575	2581	2654	2660
	2666	2755	2770	2776	2850	2868	2874	2949	2962	2968	3103	3118	3124	3153	3168
	3174	3203	3218	3224	3253	3268	3274	3303	3318	3324	3739	4477	4482	4485	
.MACRO	1	525													
.NLIST	1	525	539	560	579	605	607	617	641	643	717	719	721	723	725

DZDVC-C MACY11 27(732) 17-SEP-76 11:40 PAGE 108
 DZDVCC.P11 CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

	727	729	731	733	735	737	739	741	743	745	800	894	987	1035	1482
.PAGE	560	607	696	748	800	894	987	1497	1735	3739					
.REM	1	894													
.REPT	617														
.SBTTL	525	560	607	641	894	987	1035	1735							
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.WORD	1479														

ERRORS DETECTED: 0
 DEFAULT GLOBALS GENERATED: 0

*, DZDVCC.SEG/SOL/CRF/DS:ERFZ=DZDVCC.MAC, DZDVCC.P11
 RUN-TIME: 31 50 6 SECONDS
 RUN-TIME RATIO: 242/89=2.7
 CORE USED: 23K (45 PAGES)

