DT11

DIAGNOSTIC

MD-11-DZDTA-B

EP-DZDTA-B-DL-A

FICHE 1 OF 1

NOV 1976

digital

MADE IN U.S.A

```
.REM *
```

IDENTIFICATION

PRODUCT CODE:	MAINDEC-11-DZDTA-B
PRODUCT NAME:	DT11 DIAGNOSTIC
DATE CREATED:	15 AUGUST 1972
MAINTAINER:	DIAGNOSTIC GROUP
AUTHOR:	RICK FADDEN

```
>
```

1. ABSTRACT

THIS PROGRAM IS DESIGNED TO TEST ALL THE FUNCTIONS OF THE DT11-A AND B BUS SWITCHES WHICH CAN BE TESTED WITHOUT ASSUMING SPECIFIC DEVICES TO BE ON THE SWITCHED BUS. A GREAT DEAL OF OPERATOR INTERVENTION IS REQUIRED DUE TO THE DUAL-PROCESSOR NATURE OF THE SWITCH AND THE VARIOUS MODES OF OPERATION CONTROLLED BY TWO TWO-POSITION SWITCHES. THIS OPERATOR INTERVENTION IS DIRECTED BY PRINTOUTS ON THE TELETYPE.

2. REQUIREMENTS

2.1 EQUIPMENT

PDP-11 FAMILY STANDARD COMPUTER(S)
DT11-A OR -B BUS SWITCH

2.2 STORAGE

THE PROGRAM USES THE FIRST 5K OF MEMORY.
THIS IS IN ACCORD WITH THE CURRENT RESTRICTION THAT BUS SWITCH SYSTEMS MUST HAVE AT LEAST 8K OF MEMORY ON THE PROCESSOR BUS(ES).

3. LOADING PROCEDURE

PROCEDURE FOR NORMAL ABSOLUTE TAPES SHOULD BE FOLLOWED.

4. STARTING PROCEDURE

4.1 CONTROL SWITCH SETTINGS

BASIC SWITCH REGISTER SETTINGS ARE:

SW15=1 OR UP --- HALT ON ERROR
SW14=1 OR UP --- SCOPE LOOP
SW13=1 OR UP --- INHIBIT ERROR PRINTOUT IF SCOPE LOOP IS REQUESTED
SW12=1 OR UP --- INHIBIT TRACE TRAPPING
SW11=1 OR UP --- INHIBIT SUBTEST ITERATION
SW10=1 OR UP --- INHIBIT POWER FAIL TESTING
SW09=1 OR UP --- INHIBIT MOST SWITCHED BUS POWER FAIL TESTING
                 (ONLY CHECK TO SEE THAT AC LO SETS)
SW08=1 OR UP --- INHIBIT ALL SWITCHED BUS POWER FAIL TESTING
                 (SET THIS SWITCH ONLY IF THERE IS NO DEVICE
                 ON THE SWITCHED BUS WHICH CAN BE POWERED DOWN)

4.2 STARTING ADDRESSES

200= BASIC LOGIC TESTING OF THE DT11-B
210= STARTING ADDRESS OF THE ROUTINE RUN ON THE OTHER
     PROCESSOR WHEN A DT11-B IS BEING TESTED.

220= RESTART ADDRESS FOR BASIC LOGIC TESTING
STARTING HERE SKIPS THE INITIAL REQUESTS FOR AN
ADDRESS ON THE SWITCHED BUS, AND ASSUMES THE PREVIOUSLY
GIVEN INFORMATION. USE FOR DT11-A OR B.
230= RESTART ADDRESS FOR SA 210. STARTING HERE ASSUMES THE
INFORMATION PREVIOUSLY GIVEN.
240= SINGLE SUBTEST LOOP. ALLOWS RUNNING ANY DESIRED SUBTEST
WITHOUT GOING THRU THE REST OF THE PROGRAM FIRST.
250= TIMER ADJUSTMENT LOOP. CODE REPEATEDLY FIRES THE
TIMEOUT AND BUS INIT ONE-SHOTS.
260= BASIC LOGIC TESTING OF THE DT11-A

4.3 PROGRAM AND/OR OPERATOR ACTION

4.3.1 SA 200 (NORMAL TESTING, DT11-B)

1. LOAD THE PROGRAM INTO MEMORY OF PROCESSOR A.
2. LOAD THE PROGRAM INTO MEMORY OF PROCESSOR B.
3. PUT THE "MANUAL-PROGRAMMABLE" SWITCH IN "PROGRAMMABLE" POSITION.
4. PUT THE "INIT-INHIBIT INIT" SWITCH IN "INIT" POSITION.
5. PUT THE "HALT-ENABLE" SWITCH ON PROCESSOR B IN "HALT" POSITION,
AND THEN PRESS "START" ON PROCESSOR B.
6. LOAD STARTING ADDRESS 200 ON PROCESSOR A.
7. SET DYNAMIC SWITCH REGISTER SWITCHES AS DESIRED ON PROCESSOR A (SEE 4.1).
8. PRESS START ON PROCESSOR A.
9. FOLLOW THE INSTRUCTIONS AS THEY ARE PRINTED OUT.
10. WHEN THE END OF PASS MESSAGE IS FINISHED PRINTING OUT, HALT PROCESSOR B.
11. PUT THE "HALT-ENABLE" SWITCH ON PROCESSOR A IN "HALT" POSITION.
12. PRESS "START" ON PROCESSOR A.
13. PUT THE "INIT-INHIBIT INIT" SWITCH IN "INIT" POSITION.
14. LOAD STARTING ADDRESS 200 ON PROCESSOR B.
15. SET SWITCH REGISTER SWITCHES AS DESIRED ON PROCESSOR B.
16. PRESS "START" ON PROCESSOR B.
17. FOLLOW THE INSTRUCTIONS AS THEY ARE PRINTED. WHEN THE
END OF PASS MESSAGE IS FINISHED PRINTING, THE TEST IS COMPLETE.

SEE SECTION 5.3.1 FOR FURTHER OPERATING DETAILS.

4.3.2 SA 210 (SWITCH REGISTER MONITOR - SRMON)

WHEN THE MAIN DIAGNOSTIC (SA 200) REACHES A POINT WHERE
IT NEEDS TO HAVE OPERATIONS DONE TO THE OTHER SIDE OF THE
SWITCH, A MESSAGE IS PRINTED REQUESTING THE OPERATOR TO START
THE OTHER PROCESSOR AT SA 210. WHEN THE OTHER PROCESSOR IS
STARTED AT 210, A GROUP OF PRINTOUTS WILL OCCUR REQUESTING
INFORMATION. THIS INFORMATION MUST BE THE SAME AS THAT GIVEN
TO THE PROCESSOR RUNNING THE MAIN DIAGNOSTIC WHEN IT WAS
STARTED. SEE SECTION 5.2.9 FOR A COMPLETE DESCRIPTION OF THE
INFORMATION NEEDED. NOTE THAT ONCE THIS INFORMATION HAS BEEN
GIVEN, RESTART ADDRESS 230 MAY BE USED INSTEAD OF SA 210.

4.3.3 SA 220 (RESTART NORMAL TESTING, DT11-A OR -B)

SA 220 IS THE SAME AS SA 200 OR 260, EXCEPT THAT INFORMATION INITIALLY REQUESTED WHEN USING SA 200 OR 260 IS ASSUMED TO BE PRESENT ALREADY WHEN SA 220 IS USED. THUS SA 220 SKIPS THE INITIAL TYPEOUTS.

4.3.4 SA 230 (RESTART ADDRESS FOR SWITCH REGISTER MONITOR)

THIS RESTART ADDRESS SKIPS THE INITIAL REQUEST FOR INFORMATION MADE WHEN THE PROGRAM IS STARTED AT SA 210. THE INFORMATION GIVEN PREVIOUSLY IS USED.

4.3.5 SA 240 (SINGLE SUBTEST LOOP)

1. LOAD SA 240 AND PRESS "START".
2. AT THE FIRST HALT, LOAD THE ADDRESS OF THE TEST DESIRED (THE ADDRESS OF THE TESTXX TAG) INTO THE SWITCH REGISTER. THEN PRESS "CONTINUE".
3. AT THE SECOND HALT, SET THE CONTROL SWITCH REGISTER SETTING DESIRED. (SW11 MUST BE SET TO ZERO). THEN PRESS CONTINUE.
4. THE DESIRED SUBTEST WILL BE REPEATEDLY EXECUTED. SETTING SW11 WILL RETURN THE PROGRAM TO THE NORMAL FLOW.

4.3.6 SA 250 (ADJUST TIMERS LOOP)

LOAD BOTH PROCESSORS WITH STARTING ADDRESS 250, THEN PRESS "START" ON BOTH PROCESSORS. THE LOOP WILL NOT FUNCTION IF RUN ON ONLY ONE PROCESSOR.

4.3.7 SA 260 (NORMAL TESTING, DT11-A)

1. LOAD THE PROGRAM USING THE ABS LOADER
2. PUT THE "MANUAL-PROGRAMMABLE" SWITCH IN "PROGRAMMABLE"
3. PUT THE "INIT-INHIBIT INIT" SWITCH IN "INIT"
4. LOAD STARTING ADDRESS 26C
5. SET DYNAMIC SWITCH REGISTER SWITCHES (SEE 4.1)
6. PRESS START
7. FOLLOW THE INSTRUCTIONS AS THEY ARE PRINTED OUT

5. OPERATING PROCEDURE

5.1 OPERATIONAL SWITCH SETTINGS

SEE SECTION 4.1

F01

5.2 SUBROUTINE ABSTRACTS

5.2.1 BEGIN SA 200 FOR DT11-B, SA 260 FOR DT11-A

5.2.2 SCOPEC

THIS SUBROUTINE IS CALLED BY A TRAP CALL (SCOPE) PLACED BETWEEN EACH SUBTEST. IT RECORDS THE STARTING ADDRESS OF EACH SUB-TEST AS IT IS BEING ENTERED. IF A SCOPE LOOP IS REQUESTED, IT WILL JUMP TO THE START OF THE SUBTEST THAT THE SCOPE LOOP IS REQUESTED FOR. IF SCOPE LOOP IS NOT REQUESTED, THERE WILL BE 64 ITERATIONS ON THAT SUBTEST BEFORE THE NEXT SUBTEST IS ENTERED. SWITCH 11 ON A 1 INHIBITS ITERATION OF SUBTESTS.

5.2.3 PRINT

THIS ROUTINE IS CALLED BY A TRAP CALL (HLT) WHEN AN ERROR IS DETECTED. IT PRINTS OUT THE LOCATION COUNTER AND THE CONTENTS OF THE PROCESSOR STATUS REGISTER AT THE TIME OF FAILURE.
NOTE THAT THE LOCATION COUNTER WILL BE THE ADDRESS OF THE HLT PLUS TWO.

5.2.4 TTRAP AND TRCK

THESE ROUTINES ALLOW THE TRACE BIT TO BE SET ON ALTERNATE LOOPS OF THE PROGRAM. THE FIRST INSTRUCTION EXECUTED UPON TRAPPING IS AN "RTI" (OR "RTT" ON THE 11/45) WHICH RETURNS TO THE INTERRUPTED SEQUENCE. THIS CONTINUES UNTIL THE END OF THE PROGRAM LOOP IS REACHED.

5.2.5 TRAPCATCHER

THIS IS A SERIES OF INSTRUCTIONS STARTING AT LOCATION 0 DESIGNED TO DETECT AND ISOLATE UNEXPECTED TRAPS AND INTERRUPTS TO THE TRAP AND INTERRUPT VECTOR AREA OF MEMORY.

EACH VECTOR ENTRANCE ADDRESS IS LOADED WITH THE ADDRESS OF THE NEXT LOCATION. THE NEXT LOCATION IS LOADED WITH A HALT (000000). THUS AN ILLEGAL TRAP OR INTERRUPT WILL CAUSE A HALT AT THE TRAP LOCATION PLUS TWO.

IF A HALT OCCURS IN THE TRAP OR INTERRUPT AREA, EXAMINE REGISTER SIX. IT WILL CONTAIN THE CURRENT STACK ADDRESS. THE CONTENTS OF THE CURRENT STACK ADDRESS IS THE VALUE OF THE LOCATION COUNTER WHEN THE TRAP OR INTERRUPT OCCURRED.

5.2.6 TESTX (SINGLE TEST LOOP)

THIS ROUTINE ALLOWS A SINGLE SUBTEST TO BE RUN CONTINUOUSLY FOR SCOPE LOOP PURPOSES. WHILE A SCOPE LOOP SWITCH OPTION EXISTS, IT REQUIRES THAT YOU ARE WITHIN THE TEST IN WHICH YOU WISH TO LOOP. THIS SUBROUTINE ALLOWS YOU TO LOAD THE ADDRESS OF ANY SUBTEST AND THEN GO DIRECTLY TO THAT TEST.

5.2.7 SRMON (SWITCH REGISTER MONITOR)

THIS ROUTINE IS RUN ON PROCESSOR B WHILE THE A SIDE OF THE SWITCH IS BEING CHECKED, AND ON PROCESSOR A WHILE THE B SIDE OF THE SWITCH IS BEING CHECKED. IT MONITORS THE PROCESSOR SWITCH REGISTER, AND RUNS VARIOUS ROUTINES DEPENDING ON WHICH SWITCH IS SET.

5.2.8 TOUT AND TYPE

THESE ROUTINES PRINT ASCII MESSAGES. TOUT IS CALLED REPEATEDLY BY THE ROUTINE TYPE TO OUTPUT MESSAGES COMPOSED OF ASCII STRINGS. EACH MESSAGE IS GIVEN A MESSAGE TABLE, WHICH IS SIMPLY A LIST OF THE ADDRESSES OF THE ASCII STRINGS WHICH MUST BE TYPED TO CREATE THE FULL MESSAGE. CORE IS THUS CONSERVED BY ELIMINATING DUPLICATE PORTIONS OF STORED MESSAGES.

5.2.9 INFORM

THIS ROUTINE REQUESTS AND STORES THE INFORMATION NECESSARY TO CHECK A LOCATION ON THE SWITCHED BUS. IF ANY NPR DEVICES ARE ON THE SWITCHED BUS, THE ADDRESS OF ONE OF THE WORD COUNT OR BUS ADDRESS REGISTERS SHOULD BE GIVEN. THIS WILL ALLOW INIT ON THE SWITCHED BUS TO BE CHECKED, SINCE THE REGISTER CAN BE SET TO MINUS ONE AND THEN CLEARED BY INIT. IF NO WORD COUNT OR BUS ADDRESS REGISTER IS LOCATED ON THE SWITCHED BUS, GIVE THE ADDRESS OF ANY REGISTER WHICH HAS AT LEAST ONE BIT THAT CAN BE SET BY THE PROGRAM AND CLEARED BY INIT. IF THERE ARE NO LOCATIONS ON THE SWITCHED BUS SATISFYING THIS, GIVE AN ADDRESS OF A READ/WRITE LOCATION ON THE SWITCHED BUS (SUCH AS A MEMORY LOCATION). IN THIS CASE, INIT CANNOT BE TESTED ON THE SWITCHED BUS, BUT TESTS CAN BE MADE TO SEE IF THE SWITCH CAN CONNECT THE SWITCHED BUS TO THE PROCESSOR BUS.

THERE ARE 3 HALTS REQUESTING INFORMATION. AT THESE HALTS, SET THE NUMBER REQUIRED IN THE SWITCH REGISTER SWITCHES, AND THEN PRESS CONTINUE. THE INFORMATION NEEDED IS:

1ST HALT - ADDRESS OF A SWITCHED BUS LOCATION, AS DESCRIBED IN THE PREVIOUS PARAGRAPH

2ND HALT - THE BITS THAT ARE READ/WRITE IN THAT LOCATION (THOSE BITS THAT CAN BE SET TO ONE AND CLEARED TO ZERO BY A DATO FROM THE CPU- DON'T INCLUDE INTERRUPT ENABLE)

3RD HALT - THE BITS THAT ARE CLEARED BY INIT IN THAT LOCATION.

NOTE THAT AT THE SECOND HALT, IF THE ADDRESS GIVEN WAS THAT OF A CONTROL STATUS REGISTER, INTERRUPT ENABLE SHOULD NOT BE INCLUDED AS A READ/WRITE BIT.

5.2.10 EMTSRV (EMT DECODER)

ALL MESSAGE PRINTOUTS ARE CALLED BY EMTS. THESE EMT CALLS ARE DECODED BY EMTSRV, WHICH SETS UP THE ADDRESS OF THE MESSAGE REQUESTED AND THEN CALLS THE TYPE ROUTINE.

5.2.11 TRPSRV (TRAP DECODER)

HLT (ERROR PRINTOUT CALL) AND SCOPE (SCOPE AND ITERATION LOOP CALL) ARE BOTH CODED AS TRAPS. TRPSRV DECODES THESE CALLS AND GOES TO THE DESIRED ROUTINE. THERE IS ALSO ROOM AVAILABE TO USE TRAP CALLS 104400, 104402, AND 104404 AS CALLS ON ROUTINES SETUP BY THE USER. THE ADDRESS OF THE CORRESPONDING ROUTINE IS LOADED IN THE 1ST, 2ND, OR 3RD LOCATION OF THE TRAP TABLE (TPTAB) AND TRPSRV WILL ESSENTIALLY JUMP TO THE DESIRED ROUTINE WHEN THE TRAP CALL OCCURS. THE ROUTINE ADDED BY THE USER SHOULD PASS CONTROL BACK TO THE LOCATION AFTER THE CALL BY ENDING WITH AN RTI.

5.3 PROGRAM AND/OR OPERATOR ACTION

5.3.1 SA 200 (BASIC LOGIC TEST FOR THE DT11-B)

FOR A BASIC OUTLINE OF OPERATOR ACTION REQUIRED TO TEST THE DT11-B, SEE SECTION 4.3.1.

5.3.1 CONTINUED

THE PROGRAM INITIALLY CHECKS ALL FEATURES OF THE SWITCH WHICH CAN BE TESTED WITHOUT OPERATOR INTERVENTION. WHEN THESE TESTS ARE COMPLETE, THE PROGRAM PRINTS DIRECTIONS ON THE TELETYPE. AFTER A FEW TESTS OF FUNCTIONS RELATED TO THE "INIT-INHIBIT INIT" SWITCH, THE OPERATOR IS INSTRUCTED TO START THE OTHER PROCESSOR AT SA 210. THIS IS THE STARTING ADDRESS OF THE SWITCH REGISTER MONITOR R[illegible] (S[illegible]N), SAMON RUNS VARIOUS SUBROUTINES DEPENDING ON WHICH [illegible] SET IN THE SWITCH REGISTER. THE REMAINING TESTS IN T[illegible] DIRECT THE OPERATOR TO SET AND CLEAR VARIOUS SWITCHES IN THE SWITCH REGISTER OF THE PROCESSOR RUNNING THE SAMON ROUTINE. WHEN THE OPERATOR FOLLOWS THESE INSTRUCTIONS, HE CAUSES THE NECESSARY SUBROUTINES TO BE SELECTED. THE SUBROUTINES PERFORM SUCH FUNCTIONS AS REQUESTING AND RELEASING THE BUS SWITCH, SETTING AND CLEARING THE COMMUNICATION BIT, CHECKING AC LO (BIT14 IN THE DT11 CSR), AND RUNNING VARIOUS POWER FAIL TESTS. AT THE END OF THESE TESTS, THE PROGRAM REQUESTS THAT THE "INIT-INHIBIT INIT" SWITCH BE SET TO "INHIBIT INIT". MOST OF THE PROGRAM IS THEN REPEATED WITH THE SWITCH SET TO "INHIBIT INIT", TO MAKE SURE THAT ALL OTHER BUS SWITCH FUNCTIONS STILL WORK IN THIS MODE. WHEN THE PROGRAM PRINTS OUT "END OF PASS", A FULL TEST PASS HAS BEEN COMPLETED ON ONE SIDE OF THE SWITCH.

A NUMBER OF TESTS ARE INCLUDED WHICH CHECK POWER FAIL. THESE TESTS REQUIRE THE SYSTEM TO HAVE EACH BUS SEPARATELY POWERED, SO THAT POWERING DOWN ONE PROCESSOR, FOR EXAMPLE, DOES NOT ALSO POWER DOWN A DEVICE ON THE SWITCHED BUS. IF THE SYSTEM IS NOT SET UP IN THIS FASHION, THESE TESTS WILL FAIL. IF THE SYSTEM IS NOT INTENDED TO FUNCTION IN POWER FAIL APPLICATIONS SUCH AS THOSE REQUIRING HIGH RELIABILITY, THESE TESTS DO NOT NEED TO BE RUN. SETTING SWITCH 10 WILL INHIBIT POWER FAIL TESTING.

5.3.2 TO ADJUST THE TIMEOUT, NO MASTER SYNC, AND SWITCHED BUS INIT TIMERS, USE SA 250. (SEE 4.3.3). THIS ROUTINE, WHEN RUN ON BOTH PROCESSORS, WILL REPEATEDLY RETRIGGER EACH OF THESE ONE-SHOTS, SO THAT THEIR OUTPUTS CAN BE SCOPED EASILY.

5.3.3 TO GO DIRECTLY TO A SINGLE SUBTEST AND RUN IT CONTINUOUSLY, USE SA 240. INPUT THE STARTING ADDRESS OF THE DESIRED TEST (I.E., THE ADDRESS OF THE CORRESPONDING TESTXX TAG) AT THE INITIAL HALT AND PRESS CONTINUE. AT THE NEXT HALT, SET THE SWITCH REGISTER OPTIONS AS DESIRED (SWITCH 11 MUST BE DOWN), THEN PRESS CONTINUE. THIS FEATURE IS ESPECIALLY USEFUL WHEN FAILURES OCCUR WHILE RUNNING THE SECTION REQUIRING OPERATOR INTERVENTION.

6. ERRORS

6.1 ERROR PRINTOUT

PRINTOUTS ARE IN A STANDARD TWO WORD FORMAT. THE FIRST WORD IS THE OCTAL VALUE OF THE PC+2 OF THE DETECTED ERROR. THE SECOND IS THE CONTENTS OF THE PROCESSOR STATUS REGISTER WHEN THE ERROR WAS DETECTED.

6.2 ERROR RECOVERY

IN GENERAL, TEST FAILURES WILL PRINTOUT AN ERROR MESSAGE AND CONTINUE. IF THE "HALT ON ERROR" SWITCH IS SET, HITTING CONTINUE WILL RECOVER. IF THE PROGRAM HANGS UP IN A LOOP, THE ERROR IS LIKELY TO BE A SIGNAL WHICH WAS NEVER RECEIVED. IF A HALT OCCURS IN THE TRAP AND VECTOR AREA THE PROGRAM MUST BE RESTARTED. IF THE PROGRAM HALTS IN THE MAIN FLOW, CONSULT THE LISTING IF NO MESSAGE IS TYPED OUT.

7. RESTRICTIONS

7.1 STARTING PROCEDURE

NONE

7.2 OPERATIONAL RESTRICTIONS

NONE

8. MISCELLANEOUS

8.1 EXECUTION TIME

OPERATOR DEPENDENT. WHEN DONE, THE PROGRAM PRINTS OUT "END OF PASS".

8.2 TESTING SYSTEMS WITH MORE THAN ONE DT11

BY SUBSTITUTING INTO THE LOCATIONS BUSCSR, BUSCRH, BUSIV1, BUSST1, BUSIV2, AND BUSST2, THE ADDRESSES OF THE CSR, THE CSR HIGH BYTE, INTERRUPT VECTOR AND INTERRUPT STATUS ONE, AND INTERRUPT VECTOR AND INTERRUPT STATUS TWO, A DT11 MAY BE TESTED AT ANY ADDRESS ASSIGNED TO IT.

8.3 MESSAGE PRINTOUTS

THE DUAL-PROCESSOR NATURE OF THE BUS SWITCH REQUIRES A GREAT DEAL OF OPERATOR INTERVENTION TO TEST THE SWITCH. THE MESSAGES DIRECTING THIS OPERATOR ACTION MAY AT TIMES BE REDUNDANT, REQUESTING THE OPERATOR TO CLEAR A SWITCH REGISTER THAT ALREADY IS CLEAR, FOR EXAMPLE. THESE REDUNDANT MESSAGES ARE ACTUALLY IN SEPARATE TESTS, AND ARE INCLUDED ONLY TO ALLOW CORRECT OPERATOR ACTION IF SCOPE LOOPING ON A SINGLE SUBTEST IS REQUESTED. WHEN THEY OCCUR, SIMPLY MAKE SURE THAT THE CONDITIONS REQUESTED ARE CORRECTLY SETUP AND THEN GO ON.

9. PROGRAM DESCRIPTION

THIS SET OF TESTS IS DESIGNED TO TEST ALL OPERATIONS OF THE DT11-A AND B BUS SWITCHES, WITH THE NECESSARY EXCEPTION THAT FEATURES INVOLVING USE OF A SPECIFIC DEVICE ON THE SWITCHED BUS ARE NOT TESTED (I.E., ADDRESS AND DATA LINES ARE NOT FULLY TESTED). THE FEATURES NOT FULLY TESTED BY THE PROGRAM MAY BE TESTED BY PLACING THE SWITCH IN "MANUAL" AND RUNNING THE STANDARD DIAGNOSTICS OF ALL DEVICES ON THE SWITCHED BUS.

10. LISTING

SEE FOLLOWING PAGES.

11. FLOWCHART

NOT APPLICABLE - TEST BASICALLY IS STRAIGHT-LINE CODING.

```
;*
;DIAGNOSTIC FOR DT11-A AND -B BUS SWITCHES
;COPYRIGHT 1972, DIGITAL EQUIPMENT CORP., MAYNARD, MASS.

;*****************************************************************************
;OPERATING INSTRUCTIONS - BASIC LOGIC TEST FOR THE DT11-B (SA 200,RESTART 220)
;       1. LOAD TAPE WITH THE ABSOLUTE LOADER INTO BOTH PROCESSORS
;       2. LOAD STARTING ADDRESS 200 ON THE SIDE BEING TESTED.
;       3. SET THE "INIT- INHIBIT INIT" SWITCH TO "INIT"
;       4. SET THE "MANUAL-PROGRAMABLE" SWITCH TO "PROGRAMABLE"
;       5. PUT THE HALT SWITCH ON THE OTHER PROCESSOR IN "HALT" POSITION
;          AND THEN PRESS START ON THAT PROCESSOR (TO INIT THE BUS SWITCH)
;       6. SET THE DESIRED DYNAMIC SWITCH REGISTER SWITCHES.
;       7. PRESS START ON THE PROCESSOR RUNNING THE TEST
;       8. FOLLOW THE DIRECTIONS AS THEY ARE PRINTED OUT.
;       9. WHEN THE PROCESSOR BEGINS THE SECTION REQUIRING BOTH CPU'S,
;          A MESSAGE REQUESTING THAT THE OTHER CPU BE STARTED
;          AT 210 IS PRINTED OUT. AT THAT TIME, LOAD
;          STARTING ADDRESS 210 ON THE OTHER PROCESSOR AND PRESS START.
;      10. WHEN THE END OF PASS MESSAGE IS PRINTED OUT, STOP THE PROCESSOR BEING TESTED
;          AND START THE OTHER PROCESSOR AT 200. REPEAT THE PROCEDURE FROM (3) THRU (9),
;          NOW TESTING THE SECOND SIDE OF THE SWITCH.
;*****************************************************************************

;OPERATING INSTRUCTIONS - BASIC LOGIC TEST FOR THE DT11-A (SA 260, RESTART 220)
;       1. LOAD TAPE WITH THE ABS LOADER
;       2. LOAD STARTING ADDRESS 260
;       3. SET THE "INIT- INHIBIT INIT" SWITCH TO "INIT"
;       4. SET THE "MANUAL- PROGRAMABLE" SWITCH TO "PROGRAMABLE"
;       5. SET THE DESIRED DYNAMIC SWITCH REGISTER SWITCHES
;       6. PRESS START
;       7. FOLLOW THE DIRECTIONS AS THEY ARE PRINTED OUT

;OPERATING INSTRUCTIONS - SINGLE SUBTEST LOOP (SA 240)
;       1.  LOAD SA 240
;       2.  PRESS "START"
;       3.  AT THE FIRST HALT, LOAD THE ADDRESS OF THE TEST DESIRED
;           (THE ADDRESS OF THE TESTXX TAG) INTO THE SWITCH
;           REGISTER, THEN PRESS "CONTINUE"
;       4.  AT THE SECOND HALT, SET THE CONTROL SWITCH REGISTER SETTING
;           DESIRED, THEN PRESS "CONTINUE" (SW11 MUST BE = 0)
;       5.  THE DESIRED SUBTEST WILL BE REPEATEDLY EXECUTED. SETTING
;           SWITCH 11 WILL RETURN THE PROGRAM TO THE NORMAL
;           FLOW.

;OPERATING INSTRUCTIONS - TIMER ADJUSTMENT LOOP (SA 250)
;       1.  PUT THE "INIT-INHIBIT INIT" SWITCH IN "INIT" POSITION
;       2.  PUT THE "MANUAL - PROGRAMMABLE" SWITCH IN "PROGRAMMABLE"
;       3.  LOAD SA 250 ON ONE PROCESSOR AND PRESS "START".
;       4.  LOAD SA 250 ON THE OTHER PROCESSOR AND PRESS "START".
;       5.  THE ROUTINE WILL SWITCH THE SWITCH BACK AND FORTH
;           BETWEEN THE PROCESSORS, USING TIMEOUT ON EACH SIDE.
;           THE USE OF A WAIT INSTRUCTION AND INTERRUPT ENABLE ON
;           THE SIDE THAT DOESN'T HAVE THE SWITCH SIMPLIFIES
;           ADJUSTMENT OF THE NO MSYN TIMER.
```

```
                        ;STARTING ADDRESSES ARE:
                        ;       200 -   STANDARD STARTING ADDRESS FOR MAIN DIAGNOSTIC
                        ;       210 -   STARTING ADDRESS OF THE ROUTINE RUN ON THE OTHER PROCESSOR
                        ;               WHEN A DT11-B IS BEING TESTED
                        ;       220 -   DIAGNOSTIC RESTART ADDRESS.  STARTING HERE SKIPS THE
                        ;               INITIAL REQUESTS FOR AN ADDRESS ON THE SWITCHED BUS, AND
                        ;               ASSUMES THE PREVIOUSLY GIVEN INFORMATION (USE AFTER SA 200 OR SA 260)
                        ;       230 -   RESTART ADDRESS OF THE ROUTINE RUN ON THE OTHER PROCESSOR
                        ;               WHEN A DT11-B IS BEING TESTED.  THE PREVIOUSLY GIVEN
                        ;               INFORMATION IS ASSUMED.
                        ;       240 -   SINGLE SUBTEST LOOP. ALLOWS RUNNING ANY DESIRED
                        ;               SUBTEST WITHOUT GOING THRU THE REST OF THE
                        ;               PROGRAM FIRST.
                        ;       250 -   TIMER ADJUSTMENT LOOP. CODE REPEATEDLY FIRES
                        ;               THE TIMEOUT AND BUS INIT ONE - SHOTS.
                        ;       260 -   BASIC LOGIC TEST OF THE DT11-A

                        ;SWITCH REGISTER SETTINGS
                                ;SW15=1 OR UP - HALT ON ERROR
                                ;SW14=1 OR UP - LOOP ON CURRENT TEST (SCOPE LOOP)
                                ;SW13=1 OR UP - INHIBIT PRINT OUT IF LOOPING
                                ;SW12=1 OR UP - INHIBIT TRACE TRAPPING
                                ;SW11=1 OR UP - INHIBIT ITERATIONS OF SUBTESTS
                                ;SW10=1 OR UP - INHIBIT POWER FAIL TESTS
                                ;SW09=1 OR UP - INHIBIT MOST SWITCHED BUS POWER FAIL TESTING
                                                ;(JUST CHECK TO SEE THAT AC LO SETS SOMETIME)
                                ;SW08=1 OR UP - INHIBIT ALL SWITCHED BUS POWER FAIL TESTING
                                                ;(USE ONLY IF NO DEVICE ON THE SWITCHED BUS CAN
                                                ;BE POWERED DOWN)


                        ;DEFINITIONS
000240                          NOP=240
000000                          R0=%0
000001                          R1=%1
000002                          R2=%2
000003                          R3=%3
000004                          R4=%4
000005                          R5=%5
000006                          SP=%6
000007                          PC=%7

                        ;LOAD TRAP CATCHER IN LOCATIONS 0 TO 377
                        ;EACH VECTOR ENTRANCE ADDRESS IS LOADED WITH THE ADDRESS OF THE
                        ;NEXT LOCATION.  THE NEXT LOCATION IS LOADED WITH A HALT (000000).
                        ;THUS AN ILLEGAL TRAP OR INTERRUPT WILL CAUSE A HALT AT THE TRAP LOCATION
                        ;PLUS TWO.

                        ;LOAD VECTOR AREA
000030                          .=30
000030  021236                  EMTSRV
000032  000340                  340
000034  021432                  TRPSRV
000036  000340                  340
000314                          .=14
```

```
000014  001044                          TTRAP
000016  000340                          340

                                ;LOAD STARTING AREA
        000200                          .=200
000200  012706  001000                  MOV     #STACK,SP
000204  000167  000724                  JMP     START
        000210                          .=210
000210  012706  001000                  MOV     #STACK,SP
000214  000167  015672                  JMP     SRMONX
        000220                          .=220
000220  012706  001000                  MOV     #STACK,SP
000224  000167  000726                  JMP     RSTART
        000230                          .=230
000230  012706  001000                  MOV     #STACK,SP
000234  000167  015660                  JMP     SRMONX+6
        000240                          .=240
000240  012706  001000                  MOV     #STACK,SP
000244  000167  021234                  JMP     TESTX
        000250                          .=250
000250  012706  001000                  MOV     #STACK,SP
000254  000167  020716                  JMP     TIMERS
        000260                          .=260
000260  012706  001000                  MOV     #STACK,SP
000264  000167  000620                  JMP     DT11A

                                ;LOAD DATA AREA
        001000                          .=1000
001000  000000                  STACK:  0
        001012                          .=.+10          ;IN CASE STACK OVERRUNS
001012  177420                  BUSCSR: 177420          ;ADDRESS OF DT11 CSR
001014  177421                  BUSCRH: 177421          ;ADDRESS OF DT11 CSR, HIGH BYTE
001016  000300                  BSIV1:  300             ;ADDRESS OF INTERRUPT VECTOR 1
001020  000302                  BSST1:  302
001022  000304                  BSIV2:  304             ;ADDRESS OF INTERRUPT VECTOR 2
001024  000306                  BSST2:  306
001026  177564                  TCSR:   177564          ;TELETYPE REGISTERS
001030  177566                  TDBR:   177566
001032  177560                  TKR:    177560
001034  177776                  PSR:    177776          ;PROCESSOR STATUS REGISTER
001036  177570                  SR:     177570          ;SWITCH REGISTER
001040  177772                  PIRQ:   177772
001042  000000                  INTFLG: 0               ;INTERRUPT TEST INFORMATION
001044  000002                  TTRAP:  RTI             ;TRACE TRAP RETURN (SET TO RTT IF 11/45)
001046  000000                  CNT40:  0
001050  000000                  CNT40A: 0
001052  000000                  SBINH:  0               ;FLAG INDICATING SR9 IS SET (IF LOW BYTE IS NOT ZERO)
                                                        ;FLAG INDICATING SR8 IS SET (IF HIGH BYTE IS NOT ZERO)
001054  000000                  DVADR:  0               ;LOADED WITH ADDRESS OF A DEVICE REGISTER ON THE SWITCHED BUS
001056  000000                  RWBITS: 0               ;INDICATES THE BITS THAT ARE R/W IN THE DEVICE REGISTER
001060  000000                  INBITS: 0               ;INDICATES THE BITS THAT ARE CLEARED BY INIT
001062  000000                  ANDBTS: 0               ;LOGICAL AND OF INBITS AND RWBITS
001064  000000                  ANDCOM: 0               ;COMPLEMENT OF ANDBTS
001066  000000                  COUNT:  0
001070  000000                  SPSAV:  0               ;STORAGE FOR STACK POINTER IN POWER FAIL TESTS
001072  000000                  PFSAV:  0               ;STORAGE FOR CONTENTS OF CSR WHEN POWER DOWN OCCURS
```

```
001074  000000                  SHORTF: 0               ;INDICATES FULL TEST HAS ALREADY BEEN RUN
001076  000000                  INITF:  0               ;INDICATES THAT CURRENT PASS IS BEING RUN
                                                        ;WITH "INHIBIT-INIT" SET
001100  000000                  TFLAG:  0               ;INDICATES TRACE BIT SHOULD BE SET ON CURRENT PASS
001102  000000                  NOPF:   0               ;INDICATES POWER FAIL IS NOT BEING TESTED
001104  000000                  DT11AF: 0               ;SET NONZERO TO INDICATE TESTING A DT11-A
001106  000000                  TSTX:   0               ;SET TO INDICATE RUNNING SINGLE SUBTEST STARTUP



001110  012767  000001  177766 DT11A:  MOV     #1,DT11AF       ;SET FLAG INDICATING TESTING A DT11-A
001116  005067  177720          CLR     INTFLG
001122  004767  000036          JSR     %7,SETUP
001126  004767  017742          JSR     %7,INFORM
001132  000515                  BR      BEGIN

001134  005067  177744  START:  CLR     DT11AF
001140  005067  177676          CLR     INTFLG
001144  004767  000014          JSR     %7,SETUP
001150  004767  017720          JSR     %7,INFORM       ;REQUEST INFORMATION ABOUT A LOCATION
                                                        ;ON THE SWITCHED BUS
001154  000504                  BR      BEGIN
001156  004767  000002  RSTART: JSR     %7,SETUP
001162  000501                  BR      BEGIN
001164  005067  177704  SETUP:  CLR     SHORTF          ;CLEAR FLAGS
001170  005067  177702          CLR     INITF
001174  005067  177700          CLR     TFLAG
001200  005067  177702          CLR     TSTX
001204  005077  177624          CLR     @PSR            ;INITIALIZE PROCESSOR STATUS
001210  005067  020516          CLR     ERR             ;INITIALIZE FLAG TO INDICATE NO ERRORS SO FAR
001214  032777  002000  177614  BIT     #2000,@SR       ;CK SR10
001222  001404                  BEQ     .+12            ;SKIP IF NOT SET
001224  012767  177777  177650  MOV     #-1,NOPF        ;SET FLAG IF SET
001232  000402                  BR      .+6
001234  005067  177642          CLR     NOPF            ;CLEAR FLAG IF NOT SET
001240  005067  177506          CLR     SBINH
001244  032777  001000  177564  BIT     #1000,@SR
001252  001402                  BEQ     .+6
001254  005267  177572          INC     SBINH           ;SET LOW BYTE IF SW9 IS SET
001260  032777  000400  177550  BIT     #400,@SR
001266  001402                  BEQ     .+6
001270  105267  177557          INCB    SBINH+1         ;SET HIGH BYTE IF SW8 IS SET
001274  016777  177520  177514  MOV     @#ST1,@#SIV1
001302  016777  177516  177512  MOV     @#ST2,@#SIV2
001310  005077  177504          CLR     @#ST1
001314  005077  177504          CLR     @#ST2
001320  012737  001346  000004  MOV     #TRET,@#4       ;SETUP BUS ADDRESS TRAP RETURN
001326  005037  000006          CLR     @#6
001332  005777  177502          TST     @#IRQ
001336  012737  000006  001044  MOV     #RTT,@#TTRAP    ;IF NO TRAP THIS IS AN 11/45
001344  000404                  BR      .+12
001346  012737  000002  001044  TRET:   MOV     #RTI,@#TTRAP    ;IF TRAP, NOT AN 11/45
001354  022626                  CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
001356  012737  000006  000004  MOV     #6,@#4
```

```
001364  000207                          RTS     %7
001366  012767  000100  020722  BEGIN:  MOV     #100,ICOUNT
001374  012767  001414  020720          MOV     #TEST1+2,RETURN

                                ;CHECK FOR CSR CORRECTLY INITIALIZED VIA START SWITCH - NO SCOPE LOOP
001402  005777  177404                  TST     @BUSCSR         ;TEST CSR FOR ALL ZERO
001406  001401                          BEQ     .+4
001410  104410                          HLT                     ;NOT ALL ZEROES IN CSR

                                ;CHECK TO SEE IF ALL BITS RESPOND CORRECTLY TO DATO OF A ONE TO EACH BIT
                                ;CHECK CSR INITIALIZED CORRECTLY VIA RESET, AND THAT RESET DISCONNECTS THE SWITCH
                                ;IF IT WAS PREVIOUSLY CONNECTED
                                ;SHOW THAT BIT 9 STAYS SET FOR SEVERAL MICROSECONDS, THEN CLEARS
001412  104406          TEST1:  SCOPE
001414  012777  176177  177370          MOV     #176177,@BUSCSR ;DATO ALL ONES EXCEPT IE1, DONE, AND RESET
001422  005767  177456                  TST     DT11AF          ;IS THIS A DT11-A?
001426  001406                          BEQ     CNT1            ;NO- BRANCH
001430  022777  020203  177354          CMP     #20203,@BUSCSR  ;CHECK FOR CORRECT BITS SET IF DT11-A
001436  001401                          BEQ     .+4
001440  104410                          HLT                     ;INCORRECT BITS SET
001442  000405                          BR      CNT1A
001444  022777  026203  177340  CNT1:   CMP     #26203,@BUSCSR  ;CHECK FOR CORRECT BITS SET,DT11-B
001452  001401                          BEQ     .+4
001454  104410                          HLT                     ;BITS SET INCORRECTLY
001456  105777  177344          CNT1A:  TSTB    @TCSR           ;MAKE SURE TTY IS INACTIVE BEFORE ISSUING RESET
001462  100375                          BPL     .-4
001464  000005                          RESET                   ;RESET SHOULD CLEAR ALL BITS IN THE CSR
001466  032777  001000  177316          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO CLEAR IN CASE OF VERY LONG INIT
001474  001374                          BNE     .-6
001476  005777  177310                  TST     @BUSCSR         ;CSR ALL ZERO?
001502  001401                          BEQ     .+4             ;YES - CONTINUE
001504  104410                          HLT                     ;NO - PROCESSOR RESET DIDN'T CLEAR CSR
001506  052777  000600  177276          BIS     #600,@BUSCSR    ;SET INTERRUPT ENABLE AND TRY TO SET BIT 7
001514  022777  000400  177270          CMP     #400,@BUSCSR    ;CHECK FOR ONLY INTERRUPT ENABLE (BIT 8) SET
001522  001401                          BEQ     .+4
001524  104410                          HLT                     ;BITS INCORRECTLY SET IN CSR
001526  105777  177274                  TSTB    @TCSR           ;MAKE SURE TTY IS INACTIVE BEFORE ISSUING RESET
001532  100375                          BPL     .-4
001534  000005                          RESET                   ;RESET SHOULD CLEAR ALL BITS IN THE CSR
001536  005777  177250                  TST     @BUSCSR         ;CSR ALL ZERO?
001542  001401                          BEQ     .+4             ;YES - CONTINUE
001544  104410                          HLT                     ;NO - RESET DIDN'T CLEAR CSR
001546  032777  000020  177260          BIT     #20,@PSR        ;CHECK TRACE BIT
001554  001026                          BNE     CONT1           ;IF SET, SKIP TEST OF BIT 9 (DUE TO TIMING)
001556  016701  177230                  MOV     BUSCSR,R1       ;LOAD R1 WITH ADDRESS OF CSR
001562  012777  000001  177222          MOV     #1,@BUSCSR      ;REQUEST SWITCH
001570  052777  001000  177214          BIS     #1000,@BUSCSR   ;SET BUS SWITCH RESET
001576  031127  001000                  BIT     @R1,#1000       ;BIT 9 SHOULD STAY SET AT LEAST 10 US.
001602  001001                          BNE     .+4
001604  104410                          HLT                     ;BIT 9 DIDN'T STAY SET AT LEAST 10 US.
001606  005027  000000                  CLR     #0              ;STALL
001612  005367  177772                  DEC     .-2
001616  001375                          BNE     .-4
001620  032777  001000  177164          BIT     #1000,@BUSCSR   ;CHECK BIT 9 - SHOULD BE CLEAR BY NOW
001626  001401                          BEQ     .+4
001630  104410                          HLT                     ;BIT 9 DIDN'T CLEAR
```

```
001632  005077  177154          CONT1:  CLR     @BUSCSR         ;REINITIALIZE
001636  032777  001000  177146          BIT     #1000,@BUSCSR   ;WAIT FOR BIT 9 TO CLEAR
001644  001374                          BNE     .-6
001646  012767  000010  020442          MOV     #10,ICOUNT      ;DROP ITERATION COUNT SINCE RESETS TAKE SO LONG

                                ;CLEAR INSTRUCTION SHOULD CLEAR LOW BYTE OF
                                ;CSR (BITS 0 AND 1 DIRECTLY, BIT 7 INDIRECTLY)
001654  104406                  TEST2:  SCOPE
001656  012767  000100  020432          MOV     #100,ICOUNT     ;RESTORE ITERATION COUNT
001664  005077  177122                  CLR     @BUSCSR         ;INITIALIZE CSR
001670  012777  000003  177114          MOV     #3,@BUSCSR      ;SET REQUEST BITS
001676  105777  177110                  TSTB    @BUSCSR         ;WAIT FOR CONNECTED TO SET
001702  100375                          BPL     .-4
001704  005077  177102                  CLR     @BUSCSR         ;CLEAR CSR - CONNECTED SHOULD
001710  105777  177076                  TSTB    @BUSCSR         ;CLEAR SINCE REQUEST BITS WERE CLEARED
001714  001401                          BEQ     .+4
001716  104410                          HLT                     ;LOWER BYTE NOT ALL ZEROES
001720  032777  001000  177064          BIT     #1000,@BUSCSR   ;WAIT FOR BIT 9 TO CLEAR
001726  001374                          BNE     .-6

                                ;SHOW THAT CLEAR INSTRUCTION WILL CLEAR UPPER BYTE (EXCEPT BITS 14 AND 15,
                                ;WHICH CAN'T BE SET WITHOUT OPERATOR INTERVENTION)
001730  104406                  TEST3:  SCOPE
001732  012777  177400  177052          MOV     #177400,@BUSCSR ;DATO ALL ONES TO HIGH BYTE
001740  005077  177046                  CLR     @BUSCSR         ;CLEAR CSR
001744  005777  177042                  TST     @BUSCSR         ;CHECK
001750  001401                          BEQ     .+4
001752  104410                          HLT                     ;UPPER BYTE NOT ALL ZEROES

                                ;CLRB TO LOW BYTE SHOULD CLEAR LOWER BYTE OF CSR, AND NOT HIGH BYTE
001754  104406                  TEST4:  SCOPE
001756  052777  000340  177050          BIS     #340,@PSR       ;PREVENT INTERRUPTS
001764  012777  177403  177020          MOV     #177403,@BUSCSR ;SET BITS
001772  105777  177014                  TSTB    @BUSCSR         ;WAIT FOR CONNECTED TO SET
001776  100375                          BPL     .-4
002000  105077  177006                  CLRB    @BUSCSR         ;CLEAR LOW BYTE
002004  032777  001000  177000          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO COMPLETE
002012  001374                          BNE     .-6
002014  005767  177064                  TST     DT11AF          ;IS THIS A DT11-A?
002020  001006                          BNE     CNT4            ;YES, BRANCH
002022  022777  006400  176762          CMP     #6400,@BUSCSR   ;CHECK CSR, DT11-B
002030  001401                          BEQ     .+4
002032  104410                          HLT                     ;CSR INCORRECT
002034  000405                          BR      CNT4A
002036  022777  000400  176746  CNT4:   CMP     #400,@BUSCSR    ;CHECK CSR, DT11-A
002044  001401                          BEQ     .+4
002046  104410                          HLT                     ;CSR INCORRECT
002050  005077  176736          CNT4A:  CLR     @BUSCSR
002054  032777  001000  176730          BIT     #1000,@BUSCSR
002062  001374                          BNE     .-6

                                ;CLRB TO HIGH BYTE SHOULD CLEAR HIGH BYTE, LEAVE LOW BYTE SET
002064  104406                  TEST5:  SCOPE
002066  052777  000340  176740          BIS     #340,@PSR
002074  012777  177403  176710          MOV     #177403,@BUSCSR ;SET BITS IN CSR
002102  105077  176706                  CLRB    @BUSCSR         ;CLEAR HIGH BYTE
```

DZDTA.B

```
002106  022777  020203  176676          CMP     #20203,@BUSCSR  ;CHECK - SHOULDN'T CLEAR NON-NEUTRAL BIT (13)
002114  001401                          BEQ     .+4
002116  104410                          HLT                     ;CSR INCORRECT
002120  005077  176666                  CLR     @BUSCSR         ;RELEASE BUS SWITCH
002124  032777  001000  176660          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO COMPLETE
002132  001374                          BNE     .-6

                                ;SHOW THAT SETTING REQUEST BITS CAUSES SWITCH CONNECTED
                                ;TO SET IMMEDIATELY IF SB INIT IS NOT PRESENT
                                ;SHOW THAT THE SWITCH IS ACTUALLY CONNECTED BY ADDRESSING
                                ;A LOCATION ON THE SWITCHED BUS
002134  104406                  TEST6:  SCOPE
002136  012777  000003  176646          MOV     #3,@BUSCSR      ;SET REQUEST BITS
002144  105777  176642                  TSTB    @BUSCSR         ;CHECK CSR
002150  100401                          BMI     .+4
002152  104410                          HLT                     ;BIT 7 NOT SET
002154  012737  002212  000004          MOV     #RET6,@#4       ;SETUP TIMEOUT RETURN IN CASE
002162  017737  176646  000006          MOV     @PSR,@#6
002170  016777  176662  176656          MOV     RQBITS,@DVRDRS  ;WRITE IN A LOCATION ON THE SWITCHED BUS
002176  026777  176654  176650          CMP     RQBITS,@DVRDRS  ;CHECK RESULTS
002204  001401                          BEQ     .+4
002206  104410                          HLT
                                                                ;BITS INCORRECT IN LOCATION ON SWITCHED BUS
                                                                ;IS EITHER A SWITCH DATA LINE OR ADDRESS LINE ERROR,
                                                                ;OR INFORMATION SUPPLIED BY USER IS
                                                                ;INCORRECT
002210  000402                          BR      CONT6
002212  022626                  RET6:   CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER AFTER TIMEOUT TRAP
002214  104410                          HLT                     ;SWITCH NOT ACTUALLY CONNECTED
                                                                ;OR ADDRESS OF DEVICE GIVEN BY USER
                                                                ;INCORRECT
002216  012737  000006  000004  CONT6:  MOV     #6,@#4          ;RESTORE TRAP CATCHER
002224  005037  000006                  CLR     @#6
002230  005077  176556                  CLR     @#SCSR          ;RELEASE SWITCH
002234  032777  001000  176550          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO COMPLETE
002242  001374                          BNE     .-6
002244  005767  176626                  TST     INITF           ;IF THIS PASS IS BEING RUN WITH INIT
002250  100424                          BPL     TEST7           ;INHIBITED, SKIP THE NEXT TEST

                                ;SHOW THAT BIT 9 OF THE CSR (RESET) SETS WHEN THE SWITCH IS RELEASED
                                ;SINCE INIT IS ON THE SWITCHED BUS FOR SEVERAL MICROSECONDS.
002252  104406                  TEST6A: SCOPE
002254  032777  000020  176552          BIT     #20,@PSR        ;TRACE BIT SET?
002262  001017                          BNE     TEST7           ;YES-SKIP TEST
002264  012777  000003  176520          MOV     #3,@BUSCSR      ;FAST TEST SWITCH
002272  016701  176514                  MOV     @#SCSR,R1       ;SETUP R1 FOR FAST REFERENCE TO CSR
002276  005077  176510                  CLR     @#SCSR          ;RELEASE SWITCH
002302  031127  001000                  BIT     @R1,#1000       ;FAST CK OF BIT 9 BEING SET
002306  001001                          BNE     .+4
002310  104410                          HLT
                                                                ;BIT 9 (RESET) NOT SET IN CSR
                                                                ;WHEN THE SWITCH WAS RELEASED
002312  032777  001000  176472          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO COMPLETE
002320  001374                          BNE     .-6

                                ;SHOW THAT SETTING BIT 0 CAUSES SWITCH CONNECTED (BIT 7) TO SET IMMEDIATELY
                                ;SHOW THAT THE SWITCH IS CONNECTED (ADDRESS A LOCATION ON THE SWITCHED BUS)
002322  104406                  TEST7:  SCOPE
```

```
002324  105277  176462                  INCB    @BUSCSR         ;SET BIT 0 OF CSR
002330  105777  176456                  TSTB    @BUSCSR         ;CHECK CONNECTED BIT
002334  100401                          BMI     .+4
002336  104410                          HLT                     ;BIT 7 NOT SET
002340  012737  002356  000004          MOV     #RET7,@#4       ;SETUP TIMEOUT RETURN IN CASE
002346  016777  176504  176500          MOV     R%BITS,@DVADRS  ;REFERENCE AN ADDRESS ON THE SWITCHED BUS
002354  000402                          BR      CONT7
002356  022626                  RET7:   CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER AFTER TIMEOUT TRAP
002360  104410                          HLT                     ;SWITCH NOT ACTUALLY CONNECTED
                                                                ;OR ADDRESS OF A SWITCHED BUS LOCATION
                                                                ;GIVEN BY USER INCORRECT
002362  012737  000006  000004  CONT7:  MOV     #6,@#4          ;RESTORE TRAP CATCHER
002370  005037  000006                  CLR     @#6
002374  005077  176412                  CLR     @BUSCSR         ;RELEASE SWITCH
002400  032777  001000  176404          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO COMPLETE
002406  001374                          BNE     .-6

                                ;SHOW THAT SETTING BIT 1 CAUSES SWITCH CONNECTED TO SET IMMEDIATELY
                                ;SHOW THAT THE SWITCHED BUS IS NOT ACTUALLY CONNECTED SINCE IT IS IN POSITION 2(4)
002410  104406                  TEST8:  SCOPE
002412  012777  000002  176372          MOV     #2,@BUSCSR      ;SET BIT 1
002420  105777  176366                  TSTB    @BUSCSR         ;CHECK BIT 7 (CONNNECTED BIT)
002424  100401                          BMI     .+4
002426  104410                          HLT                     ;BIT 7 NOT SET
002430  012737  002450  000004          MOV     #RET8,@#4       ;SETUP TIMEOUT TRAP RETURN
002436  016777  176414  176410          MOV     R%BITS,@DVADRS  ;REFERENCE AN ADDRESS ON THE SWITCHED BUS
                                                                ;SHOULD TRAP SINCE SWITCH IS IN
                                                                ;CONTROLLED BUT NOT CONNECTED POSITION
002444  104410                          HLT                     ;SWITCHED BUS IS CONNECTED TO
                                                                ;THE PROCESSOR BUS AFTER BEING
002446  000401                          BR      CONT8           ;REQUESTED TO GO TO POSITION 2(4)
00    0  0    6                  RET8:   CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER AFTER TIMEOUT TRAP
00    2  012   37  000006  000004  CONT8:  MOV     #6,@#4          ;RESTORE TRAP CATCHER
00  460  00  037  000004                  CLR     @#4
00  464  00  377  176322                  CLR     @BUSCSR         ;RELEASE SWITCH
00  470  00  777  001000  176314          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO COMPLETE
00  476  001374                          BNE     .-6

                                ;SHOW THAT SETTING BIT 7 (CONNECTED) TO ZERO DOESN'T CLEAR IT
002500  104406                  TEST9:  SCOPE
00    2  00  377  176304                  INC     @   SCSR        ;REQUEST SWITCH
00    6  04  777  00    0  176276          BIC     #   0,  USCSR   ;TRY TO CLEAR BIT 7
002514  105777  176272                  TSTB    @BUSCSR
002520  100401                          BMI     .+4
00    2  104410                          HLT                     ;BIT 7 WAS CLEARED VIA BIC - SHOULD BE READ ONLY
00    4  005077  176262                  CLR     @BUSCSR         ;RELEASE SWITCH
002530  032777  001000  176254          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO CLEAR
002536  001374                          BNE     .-6

                                ;CLEARING BIT 1 WITH BIT 0 SET SHOULD LEAVE BIT 7 SET
002540  104406                  TEST10: SCOPE
002542  052777  000003  176242          BIS     #3,@   USCSR    ;REQUEST SWITCH
002550  042777  000002  176234          BIC     #2,@   SCSR     ;CLEAR BIT 1 (SWITCH STILL REQUESTED SINCE BIT 0 IS SET)
00    6  105777  176230                  TSTB    @BUS   SR       ;CHECK CONNECTED BIT
00    2  100401                          BMI     .+4
002564  104410                          HLT                     ;BIT 7 NOT SET
```

```
002566  005077  176220                  CLR     @BUSCSR         ;RELEASE SWITCH
002572  032777  001000  176212          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO CLEAR
002600  001374                          BNE     .-6

                                ;CLEARING BIT 0 WITH BIT 1 SET SHOULD LEAVE BIT 7 SET
002602  104406                  TEST11: SCOPE
002604  052777  000003  176200          BIS     #3,@BUSCSR      ;SET BITS 0 AND 1
002612  042777  000001  176172          BIC     #1,@BUSCSR      ;CLEAR BIT 0 (SWITCH IS STILL REQUESTED
                                                                ;SINCE BIT 1 IS SET)
002620  105777  176166                  TSTB    @BUSCSR         ;CHECK CONNECTED BIT
002624  100401                          BMI     .+4
002626  104410                          HLT                     ;BIT 7 NOT SET
002630  005077  176156                  CLR     @BUSCSR         ;RELEASE SWITCH
002634  032777  001000  176150          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO CLEAR
002642  001374                          BNE     .-6


                                ;BIT 13 SHOULD BE SET IF THE SWITCH IS IN POSITIONS 1(5) OR 2(4), AND CLEARED
                                ;IF IT'S IN POSITION 3
                                ;SHOW THAT THE SWITCHED BUS IS NOT CONNECTED
                                ;WHEN THE SWITCH IS IN POSITION 3
002644  104406                  TEST12: SCOPE
002646  005277  176140                  INC     @BUSCSR         ;REQUEST POSITION 1
002652  032777  020000  176132          BIT     #20000,@BUSCSR  ;CHECK BIT 13
002660  001001                          BNE     .+4
002662  104410                          HLT                     ;POSITION 1, BIT 13 NOT SET
002664  005277  176122                  INC     @BUSCSR         ;REQUEST POSITION 2
002670  032777  020000  176114          BIT     #20000,@BUSCSR  ;CHECK BIT 13
002676  001001                          BNE     .+4
002700  104410                          HLT                     ;POSITION 2, BIT 13 NOT SET
002702  005277  176104                  INC     @BUSCSR         ;REQUEST POSITION 1, BITS 0 AND 1 SET
002706  032777  020000  176076          BIT     #20000,@BUSCSR  ;CHECK BIT 13
002714  001001                          BNE     .+4
002716  104410                          HLT                     ;POSITION 1, BIT 13 NOT SET
002720  005277  176066                  INC     @BUSCSR         ;REQUEST POSITION 3
002724  032777  020000  176060          BIT     #20000,@BUSCSR  ;CHECK BIT 13
002732  001401                          BEQ     .+4
002734  104410                          HLT                     ;POSITION 3, BIT 13 SET
002736  012737  002764  000004          MOV     #RET12,@#4      ;SETUP TIMEOUT TRAP RETURN
002744  017737  176064  000006          MOV     @PSR,@#6
002752  016777  176100  176074          MOV     RWBITS,@DVADRS  ;REFERENCE TO SWITCHED BUS ADDRESS SHOULD TRAP
002760  104410                          HLT                     ;SWITCHED BUS IS CONNECTED WHILE THE SWITCH IS IN
002762  000401                          BR      .+4             ;NEUTRAL, OR THE ADDRESS ON THE SWITCHED BUS GIVEN BY
                                                                ;THE USER IS ACTUALLY ON THE PROCESSOR BUS
002764  022626                  RET12:  CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
002766  012737  000006  000004          MOV     #6,@#4          ;RESTORE TRAP CATCHER
002774  005037  000006                  CLR     @#6
003000  032777  001000  176004          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO COMPLETE
003006  001374                          BNE     .-6

                                ;BIT 13 IS READ ONLY
003010  104406                  TEST13: SCOPE
003012  032777  020000  175772          BIT     #20000,@BUSCSR  ;CHECK BIT 13, SW IN NEUTRAL
003020  001401                          BEQ     .+4             ;BRANCH IF CLEAR
003022  104410                          HLT                     ;SWITCH SHOULD BE IN NEUTRAL, BUT BIT 13 IS SET
003024  052777  020000  175760          BIS     #20000,@BUSCSR  ;TRY TO SET BIT 13
```

```
003032  032777  020000  175752          BIT     #20000,@#BUSCSR ;CHECK BIT 13
003040  001401                          BEQ     .+4
003042  104410                          HLT                     ;BIT 13 SET VIA BIS
003044  005277  175742                  INC     @#BUSCSR        ;REQUEST SWITCH
003050  042777  020000  175734          BIC     #20000,@#BUSCSR ;TRY TO CLEAR BIT 13
003056  032777  020000  175726          BIT     #20000,@#BUSCSR ;CHECK BIT 13
003064  001001                          BNE     .+4
003066  104410                          HLT                     ;BIT 13 CLEARED VIA BIC
003070  005077  175716                  CLR     @#BUSCSR        ;RELEASE SWITCH
003074  032777  001000  175710          BIT     #1000,@#BUSCSR  ;WAIT FOR SB INIT TO CLEAR
003102  001374                          BNE     .-6

                                ;SHOW THAT AN INTERRUPT WILL OCCUR IF THE SWITCH IS REQUESTED BY SETTING BIT 0,
                                ;WITH BIT 8 SET AND THE PROCESSOR STATUS AT LEVEL 0
003104  104406                  TEST14: SCOPE
003106  005077  175700                  CLR     @#BUSCSR        ;INITIALIZE CSR
003112  052777  000340  175714          BIS     #340,@#PSR      ;SET PSR TO LEVEL 7
003120  012777  003174  175670          MOV     #TINT14,@#BSIV1 ;SETUP INTERRUPT RETURN
003126  017777  175702  175664          MOV     @#PSR,@#BSST1
003134  042777  000340  175672          BIC     #340,@#PSR      ;SET PSR TO 0
003142  012777  000401  175642          MOV     #401,@#BUSCSR   ;INTERRUPT ENABLE AND REQUEST
003150  105777  175636                  TSTB    @#BUSCSR        ;WAIT FOR CONNECTED TO SET
003154  100375                          BPL     .-4
003156  017777  175636  175650          MOV     @#BSST1,@#PSR   ;RESTORE PROCESSOR TO LEVEL 7
003164  104410                          HLT                     ;NO INTERRUPT OCCURRED
003166  005077  175620                  CLR     @#BUSCSR        ;RELEASE SWITCH, CLEAR IE1
003172  000407                          BR      CONT14
003174  105777  175612          TINT14: TSTB    @#BUSCSR        ;CHECK CONNECTED BIT
003200  100401                          BMI     .+4
003202  104410                          HLT                     ;CONNECTED BIT NOT SET AFTER CONNECTED INTERRUPT
003204  022626                          CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
003206  005077  175600                  CLR     @#BUSCSR        ;DISABLE INTERRUPT
003212  016777  175602  175576  CONT14: MOV     @#BSST1,@#BSIV1 ;RESTORE TRAP CATCHER
003220  005077  175574                  CLR     @#BSST1
003224  032777  001000  175560          BIT     #1000,@#BUSCSR
003232  001374                          BNE     .-6

                                ;SHOW THAT NO INTERRUPT WILL OCCUR WHEN THE SWITCH IS REQUESTED
                                ;AND INTERRUPT ENABLE 1 IS SET IF THE PROCESSOR IS AT LEVEL 7
003234  104406                  TEST15: SCOPE
003236  052777  000340  175570          BIS     #340,@#PSR      ;SET PROCESSOR TO LEVEL 7
003244  012777  003276  175544          MOV     #TINT15,@#BSIV1 ;SETUP INTERRUPT VECTOR RETURN
003252  017777  175556  175540          MOV     @#PSR,@#BSST1
003260  012777  000401  175524          MOV     #401,@#BUSCSR   ;SET INTERRUPT ENABLE AND REQUEST SWITCH
003266  105777  175520                  TSTB    @#BUSCSR        ;WAIT FOR SWITCH CONNECTED TO SET
003272  100375                          BPL     .-4
003274  000402                          BR      .+6             ;IF OK, SKIP ERROR HALT
003276  104410                  TINT15: HLT                     ;INTERRUPT OCCURRED WITH PROCESSOR AT LEVEL 7
003300  022626                          CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
003302  005077  175504                  CLR     @#BUSCSR        ;CLEAR INTERRUPT ENABLE AND RELEASE SWITCH
003306  016777  175506  175502          MOV     @#BSST1,@#BSIV1 ;CHANGE INTERRUPT RETURN ADDRESS
003314  005077  175500                  CLR     @#BSST1         ;TO CAUSE A HALT ON A FALSE INTERRUPT
003320  032777  001000  175464          BIT     #1000,@#BUSCSR  ;WAIT FOR SB INIT TO CLEAR
003326  001374                          BNE     .-6

                                ;FIND THE LEVEL AT WHICH AN INTERRUPT OCCURS
```

```
                                        ;PRINT OUT A MESSAGE STATING THIS LEVEL IF IT IS OTHER THAN STANDARD
                                        ;(LEVEL 7).  MAKE CERTAIN THAT IT ALWAYS OCCURS AT THIS LEVEL
                                        ;THE MESSAGE STATING THE LEVEL IS PRINTED ONLY ONCE, AND THE PROGRAM
                                        ;MUST BE STARTED OVER FOR IT TO BE PRINTED AGAIN


                                        ;TEST FOR AN INTERRUPT ON LEVEL 7
                                        ;SINCE THIS IS WHERE THE BUS SWITCH NORMALLY IS, DON'T PRINT OUT A
                                        ;MESSAGE IF IT IS FOUND HERE
003330  104406                          TEST16: SCOPE
003332  052777  000340  175474                BIS     #340,@PSR       ;SET PSR TO LEVEL 7
003340  012777  003454  175450                MOV     #TINT16,@BSIVI  ;SETUP RETURN
003346  017777  175462  175444                MOV     @PSR,@#SST1
003354  042777  000040  175452                BIC     #40,@PSR        ;SET PSR TO LEVEL 6
003362  012777  000401  175422                MOV     #401,@BUSCSR    ;INTERRUPT ENABLE AND REQUEST
003370  105777  175416            CONT16:     TSTB    @BUSCSR         ;CHECK CONNECTED
003374  100375                              BPL     CONT16          ;LOOP TILL SET
003376  052777  000040  175430                BIS     #40,@PSR        ;RESTORE PSR TO LEVEL 7
003404  005077  175402                        CLR     @BUSCSR         ;DISABLE INTERRUPTS AND RELEASE SWITCH
003410  032777  001000  175374                BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO CLEAR
003416  001374                              BNE     .-6
003420  016777  175374  175370                MOV     @#SST1,@BSIVI   ;CHANGE INTERRUPT RETURN ADDRESS
003426  005077  175366                        CLR     @#SST1          ;TO CAUSE A HALT IF AN INTERRUPT OCCURS
003432  005767  175404                        TST     INTFLG          ;CHECK FLAG INDICATING LEVEL HAS ALREADY BEEN RECORDED
003436  100042                              BPL     TEST17          ;IF NOT SET, GO TO NEXT TEST
003440  026727  175376  100007                CMP     INTFLG,#100007  ;CHECK FOR RECORDED LEVEL
003446  100401                              BMI     .+4             ;BRANCH IF LESS THAN 7
003450  104410                              HLT                     ;NO INTERRUPT OCCURRED THIS TIME,
                                                                    ;BUT PREVIOUSLY OCCURRED AT THIS LEVEL (7)
003452  000434                              BR      TEST17
003454  105777  175332            TINT16:     TSTB    @BUSCSR         ;CHECK FOR CONNECTED BIT SET
003460  100401                              BMI     .+4
003462  104410                              HLT                     ;BIT 7 NOT SET AFTER CONNECTED INTERRUPT
003464  005077  175322                        CLR     @BUSCSR         ;DISABLE INTERRUPTS AND RELEASE SWITCH
003470  032777  001000  175314                BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO CLEAR
003476  001374                              BNE     .-6
003500  016777  175314  175310                MOV     @#SST1,@BSIVI   ;CHANGE INTERRUPT RETURN ADDRESS
003506  005077  175306                        CLR     @#SST1          ;TO CAUSE A HALT IF AN INTERRUPT OCCURS
003512  022626                              CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
003514  005767  175322                        TST     INTFLG          ;CHECK FOR PREVIOUS INTERRUPT FLAG
003520  100404                              BMI     SET16           ;BRANCH IF FLAG SET
003522  012767  100007  175312                MOV     #100007,INTFLG  ;SET FLAG AND LEVEL
003530  000405                              BR      TEST17          ;GO TO NEXT TEST
003532  026727  175304  100007  SET16:       CMP     INTFLG,#100007  ;CHECK PREVIOUS LEVEL
003540  100001                              BPL     TEST17
003542  104410                              HLT                     ;INTERRUPT PREVIOUSLY OCCURRED ONLY AT
                                                                    ;A LOWER LEVEL


                                        ;TEST FOR AN INTERRUPT ON LEVEL 6
003544  104406                          TEST17:  SCOPE
003546  012777  003676  175242                MOV     #TINT17,@BSIVI  ;SETUP RETURN ADDRESS
003554  052777  000340  175232                BIS     #340,@PSR       ;SET PROCESSOR PRIORITY TO 7
003562  017777  175246  175230                MOV     @PSR,@#SST1     ;SETUP RETURN STATUS
003570  042777  000340  175236                BIC     #340,@PSR       ;SET PSR TO LEVEL 0
003576  052777  000240  175230                BIS     #240,@PSR       ;SET PROCESSOR TO LEVEL 5 PRIORITY
```

```
003604  012777  000401  175200          MOV     #401,@BUSCSR    ;SET INTERRUPT ENABLE AND REQUEST
003612  105777  175174                  TSTB    @BUSCSR         ;CHECK BIT 7 - WAIT FOR CONNECTED TO SET
003616  100375                          BPL     .-4
003620  017777  175174  175206          MOV     @BSST1,@PSR     ;RESTORE PROCESSOR STATUS TO LEVEL 7
003626  005077  175160                  CLR     @BUSCSR         ;DISABLE INTERRUPTS AND RELEASE SWITCH
003632  032777  001000  175152          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO CLEAR
003640  001374                          BNE     .-6
003642  016777  175152  175146          MOV     @SST1,@BSIV1    ;CHANGE INTERRUPT RETURN ADDRESS TO
003650  005077  175144                  CLR     @BSST1          ;CAUSE A HALT IF AN INTERRUPT OCCURS
003654  005767  175162                  TST     INTFLG          ;CHECK FLAG INDICATING THAT AN INTERRUPT LEVEL
                                                                ;HAS ALREADY BEEN RECORDED
003660  100047                          BPL     TEST18          ;IF NOT, GO TO NEXT TEST
003662  026727  175154  100006          CMP     INTFLG,#100006  ;CHECK PREVIOUS LEVEL
003670  100401                          BMI     .+4
003672  104410                          HLT                     ;NO INTERRUPT OCCURRED,
                                                                ;BUT PREVIOUSLY OCCURRED
                                                                ;AT THIS LEVEL OR HIGHER
003674  000441                          BR      TEST18
003676  105777  175110          TINT17: TSTB    @BUSCSR         ;CHECK CONNECTED BIT
003702  100401                          BMI     .+4
003704  104410                          HLT                     ;BIT 7 NOT SET AFTER INTERRUPT
003706  005077  175100                  CLR     @BUSCSR         ;DISABLE FURTHER INTERRUPTS AND RELEASE SWITCH
003712  032777  001000  175072          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO CLEAR
003720  001374                          BNE     .-6
003722  016777  175072  175066          MOV     @SST1,@BSIV1    ;CHANGE INTERRUPT RETURN ADDRESS TO
003730  005077  175064                  CLR     @BSST1          ;CAUSE A HALT IF AN INTERRUPT OCCURS
003734  022626                          CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
003736  005767  175100                  TST     INTFLG          ;CHECK FOR PREVIOUS FLAG
003742  100411                          BMI     SET6            ;BRANCH IF FLAG SET
003744  012767  100006  175070          MOV     #100006,INTFLG  ;SET FLAG AND LEVEL
003752  104002                          PMSG1                   ;PRINT "THE INTERRUPT LEVEL WAS"
003754  012702  000006                  MOV     #6,R2
003760  004767  016000                  JSR     %7,PROCT        ;PRINT LEVEL NUMBER
003764  000405                          BR      TEST18
003766  026727  175050  100006  SET6:   CMP     INTFLG,#100006  ;CHECK PREVIOUS LEVEL
003774  100001                          BPL     TEST18
003776  104410                          HLT                     ;INTERRUPT PREVIOUSLY OCCURRED ONLY AT A
                                                                ;LOWER LEVEL

                                ;TEST FOR AN INTERRUPT ON LEVEL 5
004000  104406                  TEST18: SCOPE
004002  012777  004132  175006          MOV     #TINT18,@BSIV1  ;SETUP RETURN ADDRESS
004010  052777  000340  175016          BIS     #340,@PSR       ;SET PROCESSOR PRIORITY TO 7
004016  017777  175012  174774          MOV     @PSR,@BSST1     ;SETUP RETURN STATUS
004024  042777  000340  175002          BIC     #340,@PSR       ;SET PSR TO LEVEL 0
004032  052777  000200  174774          BIS     #200,@PSR       ;SET PROCESSOR TO LEVEL 4 PRIORITY
004040  012777  000401  174744          MOV     #401,@BUSCSR    ;SET INTERRUPT ENABLE AND REQUEST
004046  105777  174740                  TSTB    @BUSCSR         ;CHECK BIT 7 - WAIT FOR CONNECTED TO SET
004052  100375                          BPL     .-4
004054  017777  174740  174752          MOV     @BSST1,@PSR     ;RESTORE PROCESSOR STATUS TO LEVEL 7
004062  005077  174724                  CLR     @BUSCSR         ;DISABLE INTERRUPTS AND RELEASE SWITCH
004066  032777  001000  174716          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO CLEAR
004074  001374                          BNE     .-6
004076  016777  174716  174712          MOV     @SST1,@BSIV1    ;CHANGE INTERRUPT RETURN ADDRESS TO
004104  005077  174710                  CLR     @BSST1          ;CAUSE A HALT IF AN INTERRUPT OCCURS
004110  005767  174726                  TST     INTFLG          ;CHECK FLAG INDICATING THAT AN INTERRUPT LEVEL
```

```
                                                                ;HAS ALREADY BEEN RECORDED
004114  100047                          BPL     TEST19          ;IF NOT, GO TO NEXT TEST
004116  026727  174720  100005          CMP     INTFLG,#100005  ;CHECK PREVIOUS LEVEL
004124  100401                          BMI     .+4
004126  104410                          HLT                     ;NO INTERRUPT OCCURRED,
                                                                ;BUT PREVIOUSLY OCCURRED
                                                                ;AT THIS LEVEL OR HIGHER
004130  000441                          BR      TEST19
004132  105777  174654          TINT18: TSTB    @#BUSCSR        ;CHECK CONNECTED BIT
004136  100401                          BMI     .+4
004140  104410                          HLT                     ;BIT 7 NOT SET AFTER INTERRUPT
004142  005077  174644                  CLR     @#BUSCSR        ;DISABLE FURTHER INTERRUPTS AND RELEASE SWITCH
004146  032777  001000  174636          BIT     #1000,@#BUSCSR  ;WAIT FOR SB INIT TO CLEAR
004154  001374                          BNE     .-6
004156  016777  174636  174632          MOV     @#SST1,@#SIV1   ;CHANGE INTERRUPT RETURN ADDRESS TO
004164  005077  174630                  CLR     @#SST1          ;CAUSE A HALT IF AN INTERRUPT OCCURS
004170  022626                          CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
004172  005767  174644                  TST     INTFLG          ;CHECK FOR PREVIOUS FLAG
004176  100411                          BMI     SET5            ;BRANCH IF FLAG SET
004200  012767  100005  174634          MOV     #100005,INTFLG  ;SET FLAG AND LEVEL
004206  104002                          PMSG1                   ;PRINT "THE INTERRUPT LEVEL WAS"
004210  012702  000005                  MOV     #5,R2
004214  004767  015544                  JSR     %7,PROCT        ;PRINT LEVEL NUMBER
004220  000405                          BR      TEST19
004222  026727  174614  100005  SET5:  CMP     INTFLG,#100005  ;CHECK PREVIOUS LEVEL
004230  100001                          BPL     TEST19
004232  104410                          HLT                     ;INTERRUPT PREVIOUSLY OCCURRED ONLY AT A
                                                                ;LOWER LEVEL

                                ;TEST FOR AN INTERRUPT ON LEVEL 4
004234  104406                  TEST19: SCOPE
004236  012777  004366  174552          MOV     #TINT19,@#SIV1  ;SETUP RETURN ADDRESS
004244  052777  000340  174562          BIS     #340,@#PSR      ;SET PROCESSOR PRIORITY TO 7
004252  017777  174556  174540          MOV     @#PSR,@#SST1    ;SETUP RETURN STATUS
004260  042777  000340  174546          BIC     #340,@#PSR      ;SET PSR TO LEVEL 0
004266  052777  000140  174540          BIS     #140,@#PSR      ;SET PROCESSOR TO LEVEL 3 PRIORITY
004274  012777  000401  174510          MOV     #401,@#BUSCSR   ;SET INTERRUPT ENABLE AND REQUEST
004302  105777  174504                  TSTB    @#BUSCSR        ;CHECK BIT 7 - WAIT FOR CONNECTED TO SET
004306  100375                          BPL     .-4
004310  017777  174504  174516          MOV     @#SST1,@#PSR    ;RESTORE PROCESSOR STATUS TO LEVEL 7
004316  005077  174470                  CLR     @#BUSCSR        ;DISABLE INTERRUPTS AND RELEASE SWITCH
004322  032777  001000  174462          BIT     #1000,@#BUSCSR  ;WAIT FOR SB INIT TO CLEAR
004330  001374                          BNE     .-6
004332  016777  174462  174456          MOV     @#SST1,@#SIV1   ;CHANGE INTERRUPT RETURN ADDRESS TO
004340  005077  174454                  CLR     @#SST1          ;CAUSE A HALT IF AN INTERRUPT OCCURS
004344  005767  174472                  TST     INTFLG          ;CHECK FLAG INDICATING THAT AN INTERRUPT LEVEL
                                                                ;HAS ALREADY BEEN RECORDED
004350  100047                          BPL     TEST20          ;IF NOT, GO TO NEXT TEST
004352  026727  174464  100004          CMP     INTFLG,#100004  ;CHECK PREVIOUS LEVEL
004360  100401                          BMI     .+4
004362  104410                          HLT                     ;NO INTERRUPT OCCURRED,
                                                                ;BUT PREVIOUSLY OCCURRED
                                                                ;AT THIS LEVEL OR HIGHER
004364  000441                          BR      TEST20
004366  105777  174420          TINT19: TSTB    @#BUSCSR        ;CHECK CONNECTED BIT
004372  100401                          BMI     .+4
```

```
004374  104410                          HLT             ;BIT 7 NOT SET AFTER INTERRUPT
004376  005077  174410                  CLR     @BUSCSR ;DISABLE FURTHER INTERRUPTS AND RELEASE SWITCH
004402  032777  001000  174402          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO CLEAR
004410  001374                          BNE     .-6
004412  016777  174402  174376          MOV     @SST1,@BSIV1    ;CHANGE INTERRUPT RETURN ADDRESS TO
004420  005077  174374                  CLR     @BSST1  ;CAUSE A HALT IF AN INTERRUPT OCCURS
004424  022626                          CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
004426  005767  174410                  TST     INTFLG  ;CHECK FOR PREVIOUS FLAG
004432  100411                          BMI     SET4    ;BRANCH IF FLAG SET
004434  012767  100004  174400          MOV     #100004,INTFLG  ;SET FLAG AND LEVEL
004442  104002                          PMSG1           ;PRINT "THE INTERRUPT LEVEL WAS"
004444  012702  000004                  MOV     #4,R2
004450  004767  015310                  JSR     %7,PROCT        ;PRINT LEVEL NUMBER
004454  000405                          BR      TEST20
004456  026727  174360  100004  SET4:  CMP     INTFLG,#100004  ;CHECK PREVIOUS LEVEL
004464  100001                          BPL     TEST20
004466  104410                          HLT                     ;INTERRUPT PREVIOUSLY OCCURRED ONLY AT A
                                                                ;LOWER LEVEL

                                ;TEST FOR AN INTERRUPT ON LEVEL 3
004470  104406                  TEST20: SCOPE
004472  012777  004622  174316          MOV     #TINT20,@BSIV1  ;SETUP RETURN ADDRESS
004500  052777  000340  174326          BIS     #340,@PSR       ;SET PROCESSOR PRIORITY TO 7
004506  017777  174322  174304          MOV     @PSR,@BSST1     ;SETUP RETURN STATUS
004514  042777  000340  174312          BIC     #340,@PSR       ;SET PSR TO LEVEL 0
004522  052777  000100  174304          BIS     #100,@PSR       ;SET PROCESSOR TO LEVEL 2 PRIORITY
004530  012777  000401  174254          MOV     #401,@BUSCSR    ;SET INTERRUPT ENABLE AND REQUEST
004536  105777  174250                  TSTB    @BUSCSR         ;CHECK BIT 7 - WAIT FOR CONNECTED TO SET
004542  100375                          BPL     .-4
004544  017777  174250  174262          MOV     @BSST1,@PSR     ;RESTORE PROCESSOR STATUS TO LEVEL 7
004552  005077  174234                  CLR     @BUSCSR         ;DISABLE INTERRUPTS AND RELEASE SWITCH
004556  032777  001000  174226          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO CLEAR
004564  001374                          BNE     .-6
004566  016777  174226  174222          MOV     @SST1,@BSIV1    ;CHANGE INTERRUPT RETURN ADDRESS TO
004574  005077  174220                  CLR     @BSST1  ;CAUSE A HALT IF AN INTERRUPT OCCURS
004600  005767  174236                  TST     INTFLG  ;CHECK FLAG INDICATING THAT AN INTERRUPT LEVEL
                                                        ;HAS ALREADY BEEN RECORDED
004604  100047                          BPL     TEST21  ;IF NOT, GO TO NEXT TEST
004606  026727  174230  100003          CMP     INTFLG,#100003  ;CHECK PREVIOUS LEVEL
004614  100401                          BMI     .+4
004616  104410                          HLT             ;NO INTERRUPT OCCURRED,
                                                        ;BUT PREVIOUSLY OCCURRED
                                                        ;AT THIS LEVEL OR HIGHER
004620  000441                          BR      TEST21
004622  105777  174164          TINT20: TSTB    @BUSCSR         ;CHECK CONNECTED BIT
004626  100401                          BMI     .+4
004630  104410                          HLT             ;BIT 7 NOT SET AFTER INTERRUPT
004632  005077  174154                  CLR     @BUSCSR ;DISABLE FURTHER INTERRUPTS AND RELEASE SWITCH
004636  032777  001000  174146          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO CLEAR
004644  001374                          BNE     .-6
004646  016777  174146  174142          MOV     @SST1,@BSIV1    ;CHANGE INTERRUPT RETURN ADDRESS TO
004654  005077  174140                  CLR     @BSST1  ;CAUSE A HALT IF AN INTERRUPT OCCURS
004660  022626                          CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
004662  005767  174154                  TST     INTFLG  ;CHECK FOR PREVIOUS FLAG
004666  100411                          BMI     SET3    ;BRANCH IF FLAG SET
004670  012767  100003  174144          MOV     #100003,INTFLG  ;SET FLAG AND LEVEL
```

```
004676  104002                          PMSG1                   ;PRINT "THE INTERRUPT LEVEL WAS"
004700  012702  000003                   MOV     #3,R2
004704  004767  015054                   JSR     %7,PROCT        ;PRINT LEVEL NUMBER
004710  000405                          BR      TEST21
004712  026727  174124  100003  SET3:   CMP     INTFLG,#100003  ;CHECK PREVIOUS LEVEL
004720  100001                          BPL     TEST21
004722  104410                          HLT                     ;INTERRUPT PREVIOUSLY OCCURRED ONLY AT A
                                                                ;LOWER LEVEL

                                ;TEST FOR AN INTERRUPT ON LEVEL 2
004724  104406                  TEST21: SCOPE
004726  012777  005056  174062          MOV     #TINT21,@#SIV1  ;SETUP RETURN ADDRESS
004734  052777  000340  174072          BIS     #340,@#PSR      ;SET PROCESSOR PRIORITY TO 7
004742  017777  174066  174050          MOV     @#PSR,@#SST1    ;SETUP RETURN STATUS
004750  042777  000340  174056          BIC     #340,@#PSR      ;SET PSR TO LEVEL 0
004756  052777  000040  174050          BIS     #40,@#PSR       ;SET PROCESSOR TO LEVEL 1 PRIORITY
004764  012777  000401  174020          MOV     #401,@#BUSCSR   ;SET INTERRUPT ENABLE AND REQUEST
004772  105777  174014                  TSTB    @#BUSCSR        ;CHECK BIT 7 - WAIT FOR CONNECTED TO SET
004776  100375                          BPL     .-4
005000  017777  174014  174026          MOV     @#SST1,@#PSR    ;RESTORE PROCESSOR STATUS TO LEVEL 7
005006  005077  174000                  CLR     @#BUSCSR        ;DISABLE INTERRUPTS AND RELEASE SWITCH
005012  032777  001000  173772          BIT     #1000,@#BUSCSR  ;WAIT FOR SB INIT TO CLEAR
005020  001374                          BNE     .-6
005022  016777  173772  173766          MOV     @#SST1,@#SIV1   ;CHANGE INTERRUPT RETURN ADDRESS TO
005030  005077  173764                  CLR     @#SST1          ;CAUSE A HALT IF AN INTERRUPT OCCURS
005034  005767  174002                  TST     INTFLG          ;CHECK FLAG INDICATING THAT AN INTERRUPT LEVEL
                                                                ;HAS ALREADY BEEN RECORDED
005040  100047                          BPL     TEST22          ;IF NOT, GO TO NEXT TEST
005042  026727  173774  100002          CMP     INTFLG,#100002  ;CHECK PREVIOUS LEVEL
005050  100401                          BMI     .+4
005052  104410                          HLT                     ;NO INTERRUPT OCCURRED,
                                                                ;BUT PREVIOUSLY OCCURRED
                                                                ;AT THIS LEVEL OR HIGHER
005054  000441                          BR      TEST22
005056  105777  173730          TINT21: TSTB    @#BUSCSR        ;CHECK CONNECTED BIT
005062  100401                          BMI     .+4
005064  104410                          HLT                     ;BIT 7 NOT SET AFTER INTERRUPT
005066  005077  173720                  CLR     @#BUSCSR        ;DISABLE FURTHER INTERRUPTS AND RELEASE SWITCH
005072  032777  001000  173712          BIT     #1000,@#BUSCSR  ;WAIT FOR SB INIT TO CLEAR
005100  001374                          BNE     .-6
005102  016777  173712  173706          MOV     @#SST1,@#SIV1   ;CHANGE INTERRUPT RETURN ADDRESS TO
005110  005077  173704                  CLR     @#SST1          ;CAUSE A HALT IF AN INTERRUPT OCCURS
005114  022626                          CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
005116  005767  173720                  TST     INTFLG          ;CHECK FOR PREVIOUS FLAG
005122  100411                          BMI     SET2            ;BRANCH IF FLAG SET
005124  012767  100002  173710          MOV     #100002,INTFLG  ;SET FLAG AND LEVEL
005132  104002                          PMSG1                   ;PRINT "THE INTERRUPT LEVEL WAS"
005134  012702  000002                   MOV     #2,R2
005140  004767  014620                   JSR     %7,PROCT        ;PRINT LEVEL NUMBER
005144  000405                          BR      TEST22
005146  026727  173670  100002  SET2:   CMP     INTFLG,#100002  ;CHECK PREVIOUS LEVEL
005154  100001                          BPL     TEST22
005156  104410                          HLT                     ;INTERRUPT PREVIOUSLY OCCURRED ONLY AT A
                                                                ;LOWER LEVEL

                                ;TEST FOR AN INTERRUPT ON LEVEL 1
```

```
005160  104406                          TEST22: SCOPE
005162  012777  005312  173626                  MOV     #TINT22,@#BSIV1 ;SETUP RETURN ADDRESS
005170  052777  000340  173636                  BIS     #340,@#PSR      ;SET PROCESSOR PRIORITY TO 7
005176  017777  173632  173614                  MOV     @#PSR,@#BSST1   ;SETUP RETURN STATUS
005204  042777  000340  173622                  BIC     #340,@#PSR      ;SET PSR TO LEVEL 0
005212  052777  000000  173614                  BIS     #00,@#PSR       ;SET PROCESSOR TO LEVEL 0 PRIORITY
005220  012777  000401  173564                  MOV     #401,@#BUSCSR   ;SET INTERRUPT ENABLE AND REQUEST
005226  105777  173560                          TSTB    @#BUSCSR        ;CHECK BIT 7 - WAIT FOR CONNECTED TO SET
005232  100375                                  BPL     .-4
005234  017777  173560  173572                  MOV     @#BSST1,@#PSR   ;RESTORE PROCESSOR STATUS TO LEVEL 7
005242  005077  173544                          CLR     @#BUSCSR        ;DISABLE INTERRUPTS AND RELEASE SWITCH
005246  032777  001000  173536                  BIT     #1000,@#BUSCSR  ;WAIT FOR SB INIT TO CLEAR
005254  001374                                  BNE     .-6
005256  016777  173536  173532                  MOV     BSST1,@#BSIV1   ;CHANGE INTERRUPT RETURN ADDRESS TO
005264  005077  173530                          CLR     @#BSST1         ;CAUSE A HALT IF AN INTERRUPT OCCURS
005270  005767  173546                          TST     INTFLG          ;CHECK FLAG INDICATING THAT AN INTERRUPT LEVEL
                                                                        ;HAS ALREADY BEEN RECORDED
005274  100047                                  BPL     TEST23          ;IF NOT, GO TO NEXT TEST
005276  026727  173540  100001                  CMP     INTFLG,#100001  ;CHECK PREVIOUS LEVEL
005304  100401                                  BMI     .+4
005306  104410                                  HLT                     ;NO INTERRUPT OCCURRED,
                                                                        ;BUT PREVIOUSLY OCCURRED
                                                                        ;AT THIS LEVEL OR HIGHER
005310  000441                                  BR      TEST23
005312  105777  173474          TINT22: TSTB    @#BUSCSR        ;CHECK CONNECTED BIT
005316  100401                                  BMI     .+4
005320  104410                                  HLT                     ;BIT 7 NOT SET AFTER INTERRUPT
005322  005077  173464                          CLR     @#BUSCSR        ;DISABLE FURTHER INTERRUPTS AND RELEASE SWITCH
005326  032777  001000  173456                  BIT     #1000,@#BUSCSR  ;WAIT FOR SB INIT TO CLEAR
005334  001374                                  BNE     .-6
005336  016777  173456  173452                  MOV     BSST1,@#BSIV1   ;CHANGE INTERRUPT RETURN ADDRESS TO
005344  005077  173450                          CLR     @#BSST1         ;CAUSE A HALT IF AN INTERRUPT OCCURS
005350  022626                                  CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
005352  005767  173464                          TST     INTFLG          ;CHECK FOR PREVIOUS FLAG
005356  100411                                  BMI     SET1            ;BRANCH IF FLAG SET
005360  012767  100001  173454                  MOV     #100001,INTFLG  ;SET FLAG AND LEVEL
005366  104002                                  PMSG1                   ;PRINT "THE INTERRUPT LEVEL WAS"
005370  012702  000001                          MOV     #1,R2
005374  004767  014364                          JSR     %7,PROCT        ;PRINT LEVEL NUMBER
005400  000405                                  BR      TEST23
005402  026727  173434  100001  SET1:   CMP     INTFLG,#100001  ;CHECK PREVIOUS LEVEL
005410  100001                                  BPL     TEST23
005412  104410                                  HLT                     ;INTERRUPT PREVIOUSLY OCCURRED ONLY AT A
                                                                        ;LOWER LEVEL

                                        ;SHOW THAT AN INTERRUPT WILL OCCUR IF THE SWITCH IS REQUESTED VIA SETTING
                                        ;BITS 0 AND 1, WITH INTERRUPT ENABLE SET, THE PROCESSOR AT LEVEL 0,
                                        ;AND THE SWITCH PREVIOUSLY IN NEUTRAL
005414  104406                          TEST23: SCOPE
005416  052777  000340  173410                  BIS     #340,@#PSR      ;SET PSR TO LEVEL 7
005424  012777  005474  173364                  MOV     #TINT23,@#BSIV1 ;SETUP INTERRUPT RETURN
005432  017777  173376  173360                  MOV     @#PSR,@#BSST1
005440  042777  000340  173366                  BIC     #340,@#PSR      ;SET PSR TO LEVEL 0
005446  012777  000403  173336                  MOV     #403,@#BUSCSR   ;SET INTERRUPT ENABLE AND REQUEST
005454  105777  173332                          TSTB    @#BUSCSR        ;WAIT FOR SWITCH CONNECTED TO SET
005460  100375                                  BPL     .-4
```

```
005462  017777  173332  173344          MOV     @BSST1,@PSR     ;RESTORE PSR TO LEVEL 7
005470  104410                          HLT                     ;NO INTERRUPT OCCURRED WHEN SWITCH CONNECTED
005472  000405                          BR      CONT23
005474  105777  173312          TINT23: TSTB    @BUSCSR         ;CHECK CONNECTED BIT AFTER CONNECTED INTERRUPT
005500  100401                          BMI     .+4
005502  104410                          HLT                     ;CONNECTED BIT NOT SET AFTER CONNECTED INTERRUPT
005504  022626                          CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
005506  005077  173300          CONT23: CLR     @BUSCSR         ;DISABLE INTERRUPT AND RELEASE SWITCH
005512  016777  173302  173276          MOV     BSST1,@BSIV1    ;CHANGE INTERRUPT RETURN ADDRESS TO
005520  005077  173274                  CLR     @BSST1          ;CAUSE A HALT ON A FALSE INTERRUPT
005524  032777  001000  173260          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO COMPLETE
005532  001374                          BNE     .-6

                                ;SHOW THAT AN INTERRUPT WILL OCCUR IF THE SWITCH IS REQUESTED VIA SETTING
                                ;BIT 1, WITH INTERRUPT ENABLE SET, THE PROCESSOR AT LEVEL 0, AND THE SWITCH
                                ;PREVIOUSLY IN NEUTRAL
005534  104406                  TEST24: SCOPE
005536  052777  000340  173270          BIS     #340,@PSR       ;SET PROCESSOR PRIORITY TO LEVEL 7
005544  012777  005614  173244          MOV     #TINT24,@BSIV1  ;SETUP INTERRUPT RETURN
005552  017777  173256  173240          MOV     @PSR,@BSST1
005560  042777  000340  173246          BIC     #340,@PSR       ;SET PSR TO LEVEL 0
005566  012777  000402  173216          MOV     #402,@BUSCSR    ;SET INTERRUPT ENABLE AND REQUEST
005574  105777  173212                  TSTB    @BUSCSR         ;WAIT FOR SWITCH CONNECTED TO SET
005600  100375                          BPL     .-4
005602  017777  173212  173224          MOV     @BSST1,@PSR     ;RESTORE PROCESSOR PRIORITY TO LEVEL 7
005610  104410                          HLT                     ;NO INTERRUPT OCCURRED WHEN SWITCH CONNECTED
005612  000405                          BR      CONT24
005614  105777  173172          TINT24: TSTB    @BUSCSR         ;CHECK CONNECTED BIT AFTER CONNECTED INTERRUPT
005620  100401                          BMI     .+4
005622  104410                          HLT                     ;CONNECTED BIT NOT SET AFTER INTERRUPT
005624  022626                          CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
005626  005077  173160          CONT24: CLR     @BUSCSR         ;DISABLE INTERRUPT AND RELEASE SWITCH
005632  016777  173162  173156          MOV     BSST1,@BSIV1    ;CHANGE INTERRUPT RETURN ADDRESS TO
005640  005077  173154                  CLR     @BSST1          ;CAUSE A HALT ON A FALSE INTERRUPT
005644  032777  001000  173140          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO COMPLETE
005652  001374                          BNE     .-6

                                ;SHOW THAT AN INTERRUPT WILL NOT OCCUR IF IE1 IS SET AFTER SWITCH IS CONNECTED
                                ;SHOW THAT BIT 7 REMAINS SET ON GOING FROM POSITION 2 TO POSITION 1
                                ;SHOW THAT AN INTERRUPT WILL NOT OCCUR WHEN CHANGING FROM POSITION 2 TO
                                ;POSITION 1 IF INTERRUPT ENABLE 1 IS SET AND THE PROCESSOR IS AT LEVEL 0
005654  104406                  TEST25: SCOPE
005656  042777  000340  173150          BIC     #340,@PSR       ;ALLOW FALSE INTERRUPTS IF THEY OCCUR
005664  012777  000002  173120          MOV     #2,@BUSCSR      ;REQUEST POSITION 2
005672  105777  173114                  TSTB    @BUSCSR         ;CONNECTED BIT SHOULD BE SET
005676  100401                          BMI     .+4
005700  104410                          HLT                     ;CONNECTED BIT NOT SET
005702  052777  000340  173124          BIS     #340,@PSR       ;SET PROCESSOR PRIORITY TO LEVEL 7
005710  012777  005752  173100          MOV     #TIN25,@BSIV1   ;SETUP INTERRUPT RETURN
005716  017777  173112  173074          MOV     @PSR,@BSST1
005724  042777  000340  173102          BIC     #340,@PSR       ;SET PROCESSOR PRIORITY TO LEVEL 0
005732  052777  000400  173052          BIS     #400,@BUSCSR    ;ENABLE INTERRUPT
005740  000240                          NOP
005742  017777  173052  173064          MOV     @BSST1,@PSR     ;RESTORE PROCESSOR PRIORITY TO LEVEL 7
005750  000402                          BR      CN125
005752  104410                  TIN25:  HLT                     ;INTERRUPT OCCURRED WHEN IE1 WAS SET AFTER SWITCH
```

```
                                                                ;WAS CONNECTED
005754  022626                          CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
005756  012777  006022  173032  CNT25:  MOV     #TINT25,@#SIVI  ;CHANGE RETURN POINTER
005764  042777  000340  173042          BIC     #340,@#PSR      ;SET PROCESSOR PRIORITY TO LEVEL 0
005772  005277  173014                  INC     @#BUSCSR        ;REQUEST POSITION 1, IE1 ALREADY SET
005776  000240                          NOP
006000  017777  173014  173026          MOV     @#SST1,@#PSR    ;RESTORE PROCESSOR PRIORITY TO LEVEL 7
006006  022777  020603  172776          CMP     #20603,@#BUSCSR ;CHECK CSR
006014  001401                          BEQ     .+4
006016  104410                          HLT                     ;CSR INCORRECT
006020  000402                          BR      CONT25
006022  104410                  TINT25: HLT                     ;INTERRUPT OCCURRED GOING FROM POSITION 2 TO POSITION 1
006024  022626                          CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
006026  005077  172760          CONT25: CLR     @#BUSCSR        ;DISABLE INTERRUPT, RELEASE SWITCH
006032  016777  172762  172756          MOV     @#SST1,@#SIVI   ;CHANGE INTERRUPT RETURN ADDRESS TO
006040  005077  172754                  CLR     @#SST1          ;CAUSE A HALT ON A FALSE INTERRUPT
006044  032777  001000  172740          BIT     #1000,@#BUSCSR  ;WAIT FOR SB INIT TO COMPLETE
006052  001374                          BNE     .-6

                                ;SHOW THAT THE SWITCH DOES NOT INTERRUPT ON 2 OR MORE LEVELS
                                ;SIMULTANEOUSLY
006054  104406                  TEST26: SCOPE
006056  052777  000340  172750          BIS     #340,@#PSR      ;SET PROCESSOR PRIORITY TO LEVEL 7
006064  012777  006134  172724          MOV     #TINT26,@#SIVI  ;SETUP RETURN
006072  017777  172736  172720          MOV     @#PSR,@#SST1
006100  042777  000340  172726          BIC     #340,@#PSR      ;SET PSR TO 0
006106  012777  000401  172676          MOV     #401,@#BUSCSR   ;SET INTERRUPT ENABLE AND REQUEST
006114  105777  172672                  TSTB    @#BUSCSR        ;WAIT FOR CONNECTED TO SET
006120  100375                          BPL     .-4
006122  017777  172672  172704          MOV     @#SST1,@#PSR    ;RESTORE TO LEVEL 7
006130  104410                          HLT                     ;NO INTERRUPT OCCURRED WHEN SWITCH CONNECTED
006132  000422                          BR      CONT26
006134  105777  172652          TINT26: TSTB    @#BUSCSR        ;CHECK CONNECTED BIT
006140  100401                          BMI     .+4
006142  104410                          HLT                     ;CONNECTED BIT NOT SET AFTER INTERRUPT
006144  022626                          CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
006146  012777  006174  172642          MOV     #TIN26,@#SIVI   ;SETUP FOR DOUBLE INTERRUPT
006154  042777  000340  172652          BIC     #340,@#PSR      ;SET LEVEL TO 0
006162  000240                          NOP
006164  017777  172630  172642          MOV     @#SST1,@#PSR    ;RESTORE STATUS TO LEVEL 7
006172  000402                          BR      CONT26
006174  104410                  TIN26:  HLT                     ;DOUBLE INTERRUPT OCCURRED
006176  022626                          CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
006200  005077  172606          CONT26: CLR     @#BUSCSR        ;CLEAR INTERRUPT ENABLE AND RELEASE SWITCH
006204  005077  172610                  CLR     @#SST1          ;CHANGE INTERRUPT RETURN ADDRESS
006210  016777  172604  172600          MOV     @#SST1,@#SIVI   ;TO CAUSE A HALT ON A FALSE INTERRUPT
006216  032777  001000  172566          BIT     #1000,@#BUSCSR  ;WAIT FOR SB INIT TO CLEAR
006224  001374                          BNE     .-6

                                ;SETTING INTERRUPT ENABLE 1 SHOULD NOT CAUSE AN INTERRUPT IF THE SWITCH IS
                                ;NOT REQUESTED
006226  104406                  TEST27: SCOPE
006230  012767  000010  014060          MOV     #10,ICOUNT      ;DROP ICOUNT DUE TO STALL LOOP
006236  052777  000340  172570          BIS     #340,@#PSR      ;SET PROCESSOR PRIORITY TO LEVEL 7
006244  017777  172564  172546          MOV     @#PSR,@#SST1    ;SETUP INTERRUPT RETURN
006252  012777  006316  172536          MOV     #TINT27,@#SIVI
```

```
006260  042777  000340  172546          BIC     #340,@PSR       ;SET PROCESSOR PRIORITY TO LEVEL 0
006266  052777  000400  172516          BIS     #400,@BUSCSR    ;SET IE1
006274  005027  000000                  CLR     #0              ;WAIT TO SEE IF AN INTERRUPT WILL OCCUR
        006276                          WAIT27=.-2
006300  005367  177772                  DEC     WAIT27
006304  001375                          BNE     .-4
006306  017777  172506  172520          MOV     @BSST1,@PSR     ;RESTORE STATUS
006314  000402                          BR      CONT27
006316  104410                  TINT27: HLT                     ;CONNECTED INTERRUPT OCCURRED WITHOUT SWITCH REQUESTED
006320  022626                          CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
006322  005077  172464          CONT27: CLR     @BUSCSR         ;CLEAR IE1
006326  005077  172456                  CLR     @BSST1          ;CHANGE INTERRUPT RETURN ADDRESS
006332  016777  172462  172456          MOV     BSST1,@BSIV1    ;TO CAUSE A HALT ON A FALSE INTERRUPT

                                        ;SHOW THAT NO INTERRUPT OCCURS ON GOING FROM POSITION 1(5) TO POSITION 3
006340  104406                  TEST28: SCOPE
006342  012767  000100  013746          MOV     #100,ICOUNT     ;RESTORE ICOUNT
006350  005277  172136                  INC     @BUSCSR         ;SET SWITCH TO POSITION 1
006354  052777  000340  172452          BIS     #340,@PSR       ;SET PROCESSOR PRIORITY TO LEVEL 7
006362  017777  172446  172430          MOV     @PSR,@BSST1     ;SETUP RETURN
006370  012777  006430  172420          MOV     #TINT28,@BSIV1
006376  042777  000340  172430          BIC     #340,@PSR       ;SET PROCESSOR PRIORITY TO LEVEL 0
006404  052777  000400  172400          BIS     #400,@BUSCSR    ;SET IE1
006412  105077  172374                  CLRB    @BUSCSR         ;RELEASE SWITCH
006416  000240                          NOP
006420  017777  172374  172406          MOV     @BSST1,@PSR     ;RESTORE STATUS
006426  000402                          BR      CONT28
006430  104410                  TINT28: HLT                     ;INTERRUPT OCCURRED GOING FROM CONNECTED TO NEUTRAL
006432  022626                          CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
006434  005077  172352          CONT28: CLR     @BUSCSR         ;CLEAR IE1
006440  005077  172354                  CLR     @BSST1          ;CHANGE INTERRUPT RETURN ADDRESS TO
006444  016777  172350  172344          MOV     BSST1,@BSIV1    ;CAUSE A HALT ON A FALSE INTERRUPT
006452  032777  001000  172332          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO CLEAR
006460  001374                          BNE     .-6

                                        ;SHOW THAT BIT 7 STAYS SET GOING FROM POSITION 1 TO POSITION 2
                                        ;SHOW THAT NO INTERRUPT OCCURS GOING FROM POSITION 1 TO POSITION 2
006462  104406                  TEST29: SCOPE
006464  005277  172322                  INC     @BUSCSR         ;SET SWITCH TO POSITION 1
006470  052777  000340  172336          BIS     #340,@PSR       ;SET PROCESSOR PRIORITY TO LEVEL 7
006476  017777  172332  172314          MOV     @PSR,@BSST1     ;SETUP RETURN
006504  012777  006554  172304          MOV     #TINT29,@BSIV1
006512  042777  000340  172314          BIC     #340,@PSR       ;SET PROCESSOR PRIORITY TO LEVEL 0
006520  052777  000400  172264          BIS     #400,@BUSCSR    ;SET IE1
006526  005277  172260                  INC     @BUSCSR         ;SET SWITCH TO POSITION 2
006532  000240                          NOP
006534  017777  172260  172272          MOV     @PSST1,@PSR     ;RESTORE STATUS
006542  105777  172244                  TSTB    @BUSCSR         ;CHECK CONNECTED BIT
006546  100401                          BMI     .+4
006550  104410                          HLT                     ;CONNECTED (BIT 7) CLEARED GOING
                                                                ;FROM POSITION 1 TO POSITION 2
006552  000402                          BR      CONT29
006554  104410                  TINT29: HLT                     ;INTERRUPT OCCURRED
006556  022626                          CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
006560  005077  172226          CONT29: CLR     @BUSCSR         ;CLEAR IE1 AND RELEASE SWITCH
006564  005077  172230                  CLR     @BSST1          ;CHANGE INTERRUPT RETURN ADDRESS TO
```

```
006570  016777  172224  172220          MOV     BSST1,@BSIV1    ;CAUSE A HALT ON A FALSE INTERRUPT
006576  032777  001000  172206          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO CLEAR
006604  001374                          BNE     .-6

                                        ;SHOW THAT BIT 7 CLEARS GOING FROM POSITION 2(4) TO POSITION 3
                                        ;SHOW THAT NO INTERRUPT OCCURS GOING FROM POSITION 2(4) TO POSITION 3
006606  104406                  TEST30: SCOPE
006610  012777  000002  172174          MOV     #2,@BUSCSR      ;SET SWITCH TO POSITION 2(4)
006616  052777  000340  172210          BIS     #340,@PSR       ;SET PSR TO LEVEL 7
006624  017777  172204  172166          MOV     @PSR,@BSST1     ;SETUP INTERRUPT RETURN IN CASE
006632  012777  006702  172156          MOV     #TINT30,@BSIV1
006640  042777  000340  172166          BIC     #340,@PSR       ;SET PSR TO LEVEL 0
006646  052777  000400  172136          BIS     #400,@BUSCSR    ;SET IE1
006654  105077  172132                  CLRB    @BUSCSR         ;SET SWITCH TO POSITION 3
006660  000240                          NOP
006662  017777  172132  172144          MOV     @PSST1,@PSR     ;RESTORE STATUS
006670  105777  172116                  TSTB    @BUSCSR         ;CHECK BIT 7
006674  100001                          BPL     .+4
006676  104410                          HLT                     ;CONNECTED (BIT 7) STILL SET AFTER RELEASING SWITCH
006700  000402                          BR      CONT30
006702  104410                  TINT30: HLT                     ;INTERRUPT OCCURRED GOING FROM
                                                                ;POSITION 2(4) TO POSITION 3
006704  022626                          CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
006706  005077  172100          CONT30: CLR     @#SCSR          ;CLEAR IE1
006712  005077  172102                  CLR     @#BST1          ;CHANGE INTERRUPT RETURN ADDRESS TO
006716  016777  172076  172072          MOV     BSST1,@BSIV1    ;CAUSE A HALT ON A FALSE INTERRUPT
006724  032777  001000  172060          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO CLEAR
006732  001374                          BNE     .-6


                                        ;TESTS OF RESET ON THE SWITCHED BUS

                                        ;SETTING BIT 9 OF THE CSR SHOULD GENERATE AN INIT ON THE SWITCHED BUS
                                        ;WHEN THE SWITCH IS IN POSITION 1(5), AND SHOULD NOT CAUSE INIT ON THE PROCESSOR BUS
006734  104406                  TEST31: SCOPE
006736  005277  172050                  INC     @BUSCSR         ;REQUEST SWITCH
006742  016777  172114  172104          MOV     #ALLBTS,@DVRADRS ;SET BITS IN DEVICE REGISTER
006750  017701  172100                  MOV     @DVRADRS,R1     ;READ BACK DEVICE REGISTER TO CHECK
006754  046701  172104                  BIC     #NOCOM,R1       ;MASK OFF OTHER BITS
006760  026701  172076                  CMP     #ALLBTS,R1      ;MAKE SURE THAT THOSE
006764  001402                          BEQ     .+6             ;BITS REALLY DID SET
006766  104410                          HLT                     ;NOT ALL GIVEN BITS SET IN THE
006770  000426                          BR      CNT31A          ;GIVEN ADDRESS (SEE DOCUMENT, SECTION 5.2.9)
006772  052777  000100  172032          BIS     #100,@TKR       ;SET TTY IE
007000  052777  001000  172004          BIS     #1000,@BUSCSR   ;SET SWITCHED BUS RESET (BIT 9)
007006  032777  001000  171776          BIT     #1000,@BUSCSR   ;WAIT FOR COMPLETION OF SB INIT
007014  001374                          BNE     .-6
007016  036777  172040  172030          BIT     #NOBTS,@DVRADRS ;SEE IF THE BITS WERE CLEARED
007024  001401                          BEQ     .+4             ;IN THE DEVICE REGISTER
007026  104410                          HLT                     ;BIT9 DIDN'T CAUSE SWITCHED BUS
                                                                ;RESET IN POSITION 1(5)
007030  032777  000100  171774          BIT     #100,@TKR       ;CHECK IE OF TELETYPE READER
007036  001001                          BNE     .+4             ;BRANCH IF STILL SET
007040  104410                          HLT                     ;SETTING BIT 9 CAUSED INIT ON THE
007042  005077  171764                  CLR     @TKR            ;PROCESSOR BUS IN POSITION 1(5)
007046  005077  171740          CNT31A: CLR     @BUSCSR         ;RELEASE SWITCH
```

F03


```
007052  032777  001000  171732          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO COMPLETE
007060  001374                          BNE     .-6

                                ;SETTING BIT 9 OF THE CSR SHOULD GENERATE AN INIT ON THE SWITCHED BUS
                                ;WHEN THE SWITCH IS IN POSITION 2(4), AND SHOULD NOT CAUSE AN INIT ON THE
                                ;PROCESSOR BUS
007062  104406                  TEST32: SCOPE
007064  012777  000003  171720          MOV     #3,@BUSCSR      ;REQUEST SWITCH
007072  016777  171764  171754          MOV     ANDBTS,@DVADRS  ;SET BITS IN DEVICE REGISTER
007100  017701  171750                  MOV     @DVADRS,R1      ;CHECK BITS SET
007104  046701  171754                  BIC     ANDCOM,R1       ;MASK OFF REST
007110  026701  171746                  CMP     ANDBTS,R1
007114  001402                          BEQ     .+6             ;BRANCH IF OK
007116  104410                          HLT                     ;NOT ALL GIVEN BITS SET (SEE DOCUMENT, SECTION 5.2.9)
007120  000432                          BR      CNT32A
007122  012777  000100  171702          MOV     #100,@TKR       ;SET IE OF TTY READER
007130  005377  171656                  DEC     @BUSCSR         ;PUT SWITCH IN POSITION 2(4)
007134  052777  001000  171650          BIS     #1000,@BUSCSR   ;SET SWITCHED BUS RESET
007142  032777  001000  171642          BIT     #1000,@BUSCSR   ;WAIT FOR COMPLETION OF SB INIT
007150  001374                          BNE     .-6
007152  005277  171634                  INC     @BUSCSR         ;SWITCH TO POSITION 1(5)
007156  036777  171700  171670          BIT     ANDBTS,@DVADRS  ;CHECK THE BITS IN THE DEVICE REGISTER
007164  001401                          BEQ     .+4             ;BRANCH IF CLEARED
007166  104410                          HLT                     ;SETTING BIT 9 DIDN'T CAUSE
                                                                ;SWITCHED BUS RESET IN POSITION 2(4)
007170  032777  000100  171634          BIT     #100,@TKR       ;CHECK IE IN TTY READER CSR
007176  001001                          BNE     .+4             ;BRANCH IF OK
007200  104410                          HLT                     ;SETTING BIT 9 OF THE CSR CAUSED
                                                                ;INIT ON THE PROCESSOR BUS WITH
                                                                ;THE SWITCH IN POSITION 2(4)
007202  005077  171624                  CLR     @TKR            ;REINITIALIZE TTY
007206  005077  171600          CNT32A: CLR     @BUSCSR         ;REINITIALIZE SWITCH
007212  032777  001000  171572          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO COMPLETE
007220  001374                          BNE     .-6
007222  005767  171650                  TST     INITF           ;IF THIS PASS IS BEING RUN WITH THE
007226  100003                          BPL     .+10            ;"INIT-INHIBIT INIT" SWITCH IN "INHIBIT INIT"
007230  104406                          SCOPE                   ;POSITION, SKIP TO THE NEXT APPROPRIATE TEST
007232  000167  000156                  JMP     CNT34

                                ;IF THE BUS SWITCH IS USED WITH THE "INIT" - INHIBIT INIT" SWITCH IN THE "INIT"
                                ;POSITION, AN INIT SHOULD BE GENERATED WHEN THE SWITCH IS SWITCHED
                                ;INTO POSITION 3
007236  104406                  TEST33: SCOPE
007240  005277  171546                  INC     @BUSCSR         ;REQUEST SWITCH - POSITION 1(5)
007244  016777  171612  171602          MOV     ANDBTS,@DVADRS  ;SET BITS IN DEVICE REGISTER
007252  017701  171576                  MOV     @DVADRS,R1      ;CHECK BITS SET
007256  046701  171602                  BIC     ANDCOM,R1       ;MASK OFF REST
007262  026701  171574                  CMP     ANDBTS,R1
007266  001402                          BEQ     .+6             ;BRANCH IF OK
007270  104410                          HLT                     ;NOT ALL GIVEN BITS SET
007272  000427                          BR      CNT33A
007274  012777  000100  171530          MOV     #100,@TKR       ;SET IE OF TTY READER
007302  005077  171504                  CLR     @BUSCSR         ;PUT SWITCH INTO POSITION 3
007306  032777  001000  171476          BIT     #1000,@BUSCSR   ;WAIT FOR COMPLETION OF SB INIT
007314  001374                          BNE     .-6
007316  005277  171470                  INC     @BUSCSR         ;REQUEST SWITCH
```

```
007322  036777  171534  171524          BIT     ANDBTS,@DVADRS  ;CHECK THE BITS SET IN THE DEVICE REGISTER
007330  001401                          BEQ     .+4             ;BRANCH IF CLEARED
007332  104410                          HLT                     ;NO RESET ON GOING INTO POSITION 3 WITH
                                                                ;"INIT - INHIBIT INIT" SET IN THE "INIT" POSITION
007334  032777  000100  171470          BIT     #100,@TKR       ;CHECK TTY IE
007342  001001                          BNE     .+4
007344  104410                          HLT                     ;INIT OCCURRED ON PROCESSOR BUS
007346  005077  171460                  CLR     @TKR
007352  005077  171434          CNT33A: CLR     @BUSCSR         ;RELEASE SWITCH
007356  032777  001000  171426          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO COMPLETE
007364  001374                          BNE     .-6
007366  005767  171502                  TST     SHORTF          ;IF THE ENTIRE TEST HAS ALREADY BEEN RUN,
007372  100002                          BPL     .+6             ;SKIP THE SECTION REQUIRING OPERATOR INTERVENTION
007374  000167  006444                  JMP     END

                                ;WITH THE "INIT - INHIBIT INIT" SWITCH SET TO "INHIBIT INIT," SWITCHING INTO POSITION
                                ;3 SHOULDN'T CAUSE AN INIT TO OCCUR ON THE SWITCHED BUS
007400  104406                  TEST34: SCOPE
007402  012767  007414  012712          MOV     #CNT34,RETURN   ;EXCLUDE MESSAGE PRINTOUT FROM SCOPE LOOP
007410  104030                          PMSG12                  ;PRINT MESSAGE:  "PUT THE 'INIT - INHIBIT INIT' SWITCH
                                                                ;IN THE 'INHIBIT INIT' POSITION.  THEN
007412  000000                          HALT                    ;PRESS 'CONTINUE' ON THIS PROCESSOR,"
007414  005277  171372          CNT34:  INC     @#BUSCSR        ;PUT SWITCH IN POSITION 1 (5)
007420  016777  171436  171426          MOV     #ANDBTS,@DVADRS ;SET BITS IN THE REGISTER ON THE SWITCHED BUS
007426  017701  171422                  MOV     @DVADRS,R1      ;CHECK BITS SET
007432  046701  171426                  BIC     ANDCOM,R1       ;MASK OFF REST
007436  026701  171420                  CMP     ANDBTS,R1
007442  001402                          BEQ     .+6             ;BRANCH IF OK
007444  104410                          HLT                     ;NOT ALL GIVEN BITS SET IN ADDRESS ON SWITCHED BUS
007446  000421                          BR      CNT34A
007450  005077  171336                  CLR     @BUSCSR         ;PUT SWITCH INTO POSITION 3
007454  032777  001000  171330          BIT     #1000,@BUSCSR   ;CHECK SWITCHED BUS RESET - SHOULD NOT OCCUR
007462  001401                          BEQ     .+4
007464  104410                          HLT                     ;SB RESET (BIT 9) WAS SET
007466  005277  171320                  INC     @BUSCSR         ;PUT SWITCH BACK IN 1(5)
007472  017701  171356                  MOV     @DVADRS,R1      ;GET REGISTER CONTENTS
007476  046701  171362                  BIC     ANDCOM,R1       ;MASK OFF BITS NOT USED
007502  026701  171354                  CMP     ANDBTS,R1       ;CHECK BITS IN DEVICE REGISTER
007506  001401                          BEQ     .+4             ;BRANCH IF OK
007510  104410                          HLT                     ;INIT OCCURRED ON THE SWITCHED BUS
007512  005077  171274          CNT34A: CLR     @BUSCSR         ;RELEASE SWITCH
007516  032777  001000  171266          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO COMPLETE
007524  001374                          BNE     .-6

                                ;WITH THE "INIT - INHIBIT INIT" SWITCH SET TO "INHIBIT INIT", SETTING BIT 9 OF THE CSR
                                ;DOESN'T CAUSE A SWITCHED BUS RESET IN POSITION 3, AND DOESN'T CAUSE AN INIT ON
                                ;THE PROCESSOR BUS
007526  104406                  TEST35: SCOPE
007530  012777  000001  171254          MOV     #1,@#BUSCSR     ;PUT SWITCH IN POSITION 1(5)
007536  016777  171320  171310          MOV     #ANDBTS,@DVADRS ;SET BITS IN DEVICE REGISTER
007544  017701  171304                  MOV     @DVADRS,R1      ;CHECK BITS SET
007550  046701  171310                  BIC     ANDCOM,R1       ;MASK OFF REST
007554  026701  171302                  CMP     ANDBTS,R1
007560  001402                          BEQ     .+6             ;BRANCH IF OK
007562  104410                          HLT                     ;NOT ALL GIVEN BITS SET IN ADDRESS ON SWITCHED BUS
007564  000431                          BR      CNT35
```

```
007566  012777  000100  171236          MOV     #100,@TKR       ;SET TTY READER IE
007574  005077  171212                  CLR     @BUSCSR         ;PUT SWITCH IN POSITION 3
007600  052777  001000  171204          BIS     #1000,@BUSCSR   ;SET BIT 9 IN CSR
007606  005277  171200                  INC     @BUSCSR         ;PUT SWITCH IN POSITION 1(5)
007612  017701  171236                  MOV     @OVADRS,R1      ;CHECK BITS IN THE DEVICE REGISTER
007616  046701  171242                  BIC     ANDCOM,R1
007622  026701  171234                  CMP     ANDBTS,R1
007626  001401                          BEQ     .+4             ;BRANCH IF OK
007630  104410                          HLT                     ;AN INIT OCCURRED ON THE SWITCHED BUS
007632  032777  000100  171172          BIT     #100,@TKR       ;CHECK TTY READER IE
007640  001001                          BNE     .+4             ;BRANCH IF OK
007642  104410                          HLT                     ;INIT OCCURRED ON PROCESSOR BUS
007644  005077  171162                  CLR     @TKR            ;CLEAR TTY READER CSR
007650  005077  171136          CNT35:  CLR     @BUSCSR         ;RELEASE SWITCH
007654  005767  171224                  TST     DT11AF          ;IS THIS A DT11-A?
007660  001411                          BEQ     TST35A          ;NO, CONTINUE
007662  005067  012430                  CLR     ICOUNT          ;YES, DROP ITERATION COUNT
007666  005767  171204                  TST     INITF           ;SKIP MESSAGE IF SECOND PASS (RUNNING WITH
007672  100402                          BMI     .+6             ;INIT INHIBITED)
007674  104032                          PMSG13                  ;PRINT MESSAGE: "PUT THE 'INIT-INHIBIT
                                                                ;INIT' SWITCH IN THE 'INIT' POSITION. THEN
007676  000000                          HALT                    ;PRESS 'CONTINUE' ON THIS PROCESSOR."
007700  000167  001262                  JMP     TEST42          ;SKIP TO TEST42

                                ;WITH THE SWITCH CONTROLLED BY BUT NOT CONNECTED TO THE OTHER CPU,
                                ;SETTING BIT 9 IN THIS SIDE'S CSR DOESN'T CAUSE A SWITCHED BUS RESET
007704  104406                  TST35A: SCOPE
007706  005067  012404                  CLR     ICOUNT
007712  005767  171160                  TST     INITF           ;ON SECOND PASS (SWITCH IN "INHIBIT INIT" POSITION)
007716  100402                          BMI     .+6             ;SKIP MESSAGE PRINTOUT
007720  104020                          PMSG8                   ;REQUEST OPERATOR TO START OTHER CPU AT SA 210,
007722  000000                          HALT                    ;AND THEN PRESS "CONTINUE" ON THIS PROCESSOR
007724  005767  171146                  TST     INITF
007730  100402                          BMI     .+6             ;BRANCH IF 2ND PASS
007732  104112                          PMSG37                  ;IF 1ST PASS, REQUEST OPERATOR
007734  000401                          BR      .+4             ;TO SET SR13 ON OTHER CPU
007736  104070                          PMSG28                  ;REQUEST OPERATOR TO SET SWITCH 10 ON OTHER CPU
                                                                ;SWITCH REGISTER, THEN PRESS "CONTINUE"
007740  000000                          HALT
007742  052777  001000  171042          BIS     #1000,@BUSCSR   ;SET BIT 9
007750  032777  001000  171034          BIT     #1000,@BUSCSR   ;CHECK BIT 9 - SHOULDN'T STAY SET
007756  001401                          BEQ     .+4
007760  104410                          HLT                     ;BIT 9 STAYED SET INDICATING SB INIT HAS ISSUED
007762  005077  171024                  CLR     @BUSCSR
007766  104012                          PMSG5                   ;"CLEAR SR OF OTHER CPU, THEN PRESS 'CONT'"
007770  000000                          HALT

                                ;WITH THE SWITCH CONNECTED TO THE OTHER CPU,
                                ;SETTING BIT 9 IN THIS SIDE'S CSR DOESN'T CAUSE A SWITCHED BUS RESET
007772  104406                  TST35B: SCOPE
007774  104072                          PMSG29                  ;REQUEST OPERATOR TO CLEAR SWITCH REGISTER
007776  000000                          HALT                    ;OF OTHER CPU, THEN SET SWITCH 11
010000  052777  001000  171004          BIS     #1000,@BUSCSR   ;SET BIT 9
010006  032777  001000  170776          BIT     #1000,@BUSCSR   ;CHECK BIT 9- SHOULDN'T BE SET
010014  001401                          BEQ     .+4
010016  104410                          HLT                     ;BIT 9 STAYED SET INDICATING SB INIT HAS ISSUED
```

```
010020  104012                          PMSG5                   ;"CLEAR SR OF OTHER CPU, THEN PRESS 'CONT'"
010022  000000                          HALT
010024  005767  171046                  TST     INITF           ;SKIP MESSAGE IF
010030  100402                          BMI     TEST36          ;RUNNING ALL WITH "INHIBIT INIT" SET
010032  104032                          PMSG13                  ;PRINT MESSAGE:  "PUT THE 'INIT - INHIBIT INIT' SWITCH
                                                                ;IN THE 'INIT' POSITION. THEN
010034  000000                          HALT                    ;PRESS 'CONTINUE' ON THIS PROCESSOR."

                                ;CHECK BIT 13
                                ;IT SHOULD BE SET WHENEVER THE SWITCH IS CONTROLLED BY THE OTHER PROCESSOR
010036  104406                  TEST36: SCOPE
010040  104004                          PMSG2                   ;PRINT MESSAGE:  "CHANGE SWITCH REGISTER OF OTHER
                                                                ;PROCESSOR - CLEAR IT AND THEN SET
                                                                ;SWITCH ZERO TO A ONE, THEN PRESS
010042  000000                          HALT                    ;'CONTINUE' ON THIS PROCESSOR."
010044  032777  020000  170740          BIT     #20000,@BUSCSR  ;CHECK BIT 13
010052  001001                          BNE     .+4             ;BRANCH IF SET
010054  104410                          HLT                     ;BIT 13 NOT SET WHEN OTHER PROCESSOR
                                                                ;HAS SWITCH CONNECTED AND CONTROLLED
010056  104006                          PMSG3                   ;PRINT MESSAGE:  "CHANGE SWITCH REGISTER OF OTHER
010060  000000                          HALT                    ;PROCESSOR - CLEAR IT AND THEN SET SWITCH 1 TO A ONE
                                                                ;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."
010062  032777  020000  170722          BIT     #20000,@BUSCSR
010070  001001                          BNE     .+4
010072  104410                          HLT                     ;BIT 13 NOT SET WHEN OTHER PROCESSOR
                                                                ;HAS SWITCH CONTROLLED BUT NOT CONNECTED

                                ;CHECK OPERATION OF BIT 15
                                ;IT SHOULD SET IF EITHER PROCESSOR TIMES OUT
                                ;ANY DATO TO THE CSR SHOULD CLEAR IT
                                ;SHOW THAT THE SWITCHED BUS ACTUALLY IS CONNECTED
                                ;AFTER THE OTHER PROCESSOR TIMES OUT
010074  104406                  TEST37: SCOPE
010076  104004                          PMSG2                   ;PRINT MESSAGE:  "CHANGE SWITCH REGISTER OF OTHER
                                                                ;PROCESSOR-CLEAR IT AND THEN SET SWITCH ZERO
                                                                ;TO A ONE, THEN PRESS 'CONTINUE' ON
010100  000000                          HALT                    ;THIS PROCESSOR."
                                                                ;THIS CAUSES THE OTHER SIDE TO
                                                                ;REQUEST THE SWITCH
010102  005777  170704                  TST     @BUSCSR         ;CHECK BIT IS
010106  100001                          BPL     .+4             ;BRANCH IF NOT SET
010110  104410                          HLT                     ;TIMEOUT WAS SET AFTER CSR WAS CLEARED
010112  012777  000003  170672          MOV     #3,@BUSCSR      ;REQUEST SWITCH-OTHER PROCESSOR
                                                                ;ISN'T REREQUESTING
010120  105777  170666                  TSTB    @BUSCSR         ;WAIT FOR CONNECT TO SET
010124  100375                          BPL     .-4
010126  012737  010152  000004          MOV     #RET37,@#4      ;SETUP RETURN IN CASE
010134  017737  170674  000006          MOV     @PSR,@#6
010142  016777  170710  170704          MOV     R+BITS,@DVADRS  ;MAKE SURE SWITCHED BUS IS ACTUALLY CONNECTED
010150  000402                          BR      .+6             ;BY REFERENCING ADDRESS ON THE SWITCHED BUS
010152  022626                  RET37:  CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
010154  104410                          HLT                     ;SWITCHED BUS NOT ACTUALLY CONNECTED
010156  012737  000006  000004          MOV     #6,@#4          ;RESTORE TRAP CATCHER
010164  005037  000006                  CLR     @#6
010170  005777  170616                  TST     @BUSCSR         ;CHECK TIMEOUT BIT
010174  100401                          BMI     .+4
```

```
010176  104410                          HLT                     ;TIMEOUT NOT SET AFTER OTHER SIDE LOST SWITCH BY TIMEOUT
010200  052777  100000  170604          BIS     #100000,@BUSCSR ;DATO SHOULD CLEAR TIMEOUT BIT
010206  005777  170600                  TST     @BUSCSR
010212  100001                          BPL     .+4
010214  104410                          HLT                     ;DATO DIDN'T CLEAR TIMEOUT BIT
010216  104004                          PMSG2                   ;PRINT MESSAGE:  "CHANGE SWITCH REGISTER OF OTHER
                                                                ;PROCESSOR-CLEAR IT AND THEN SET SWITCH 0
                                                                ;TO A ONE, THEN PRESS 'CONTINUE'
010220  000000                          HALT                    ;ON THIS PROCESSOR."
010222  105777  170564                  TSTB    @BUSCSR         ;WAIT FOR CONNECT TO CLEAR DUE TO
010226  100775                          BMI     .-4             ;REQUEST BY OTHER PROCESSOR
010230  005777  170556                  TST     @BUSCSR         ;CHECK TIMEOUT
010234  100401                          BMI     .+4
010236  104410                          HLT                     ;TIMEOUT DIDN'T SET WHEN THIS SIDE
                                                                ;LOST THE SWITCH BY TIMING OUT
010240  022777  120003  170544          CMP     #120003,@BUSCSR ;TIMEOUT SHOULDN'T CLEAR BITS 0 AND 1
010246  001401                          BEQ     .+4
010250  104410                          HLT                     ;STATUS REGISTER INCORRECT
010252  105077  170534                  CLRB    @BUSCSR         ;DATOB TO LOW BYTE SHOULD CLEAR BIT 15
010256  022777  020000  170526          CMP     #20000,@BUSCSR  ;TIMEOUT SHOULD NOW BE ZERO
010264  001401                          BEQ     .+4
010266  104410                          HLT                     ;BIT 15 STAYED SET OR ANOTHER BIT IS
                                                                ;SET INCORRECTLY
010270  005277  170516                  INC     @BUSCSR         ;REQUEST SWITCH AGAIN
010274  105777  170512                  TSTB    @BUSCSR         ;WAIT FOR CONNECT TO SET
010300  100375                          BPL     .-4
010302  005777  170504                  TST     @BUSCSR         ;TIMEOUT SHOULD BE SET SINCE OTHER SIDE LOST SWITCH
010306  100401                          BMI     .+4
010310  104410                          HLT                     ;TIMEOUT NOT SET
010312  112777  000200  170474          MOVB    #200,@BUSCRH    ;DATOB TO HIGH BYTE SHOULD CLEAR BIT 15
010320  022777  020201  170464          CMP     #20201,@BUSCSR  ;CHECK CSR
010326  001401                          BEQ     .+4
010330  104410                          HLT                     ;SWITCH CSR INCORRECT
010332  005077  170454                  CLR     @BUSCSR         ;RELEASE SWITCH
010336  032777  001000  170446          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO COMPLETE
010344  001374                          BNE     .-6

                                ;CHECK THAT REREQUESTING THE SWITCH WILL PREVENT TIMEOUT
010346  104406                  TST37A: SCOPE
010350  104122                          PMSG41                  ;"WHEN THIS PRINTOUT IS FINISHED, PRESS 'CONTINUE.' THEN
                                                                ;CHANGE SR OF OTHER CPU:
010352  000000                          HALT                    ;TOGGLE SWITCH ZERO AT LEAST TEN TIMES.
                                                                ;THEN SET SWITCH ZERO IN THIS CPU'S SR."
010354  012777  000001  170430          MOV     #1,@BUSCSR      ;REQUEST SWITCH
010362  012777  000001  170422  LOP37A: MOV     #1,@BUSCSR      ;REREQUEST SWITCH
010370  017701  170416                  MOV     @BUSCSR,R1      ;SAVE CONTENTS OF CSR IN R1
010374  020127  020201                  CMP     R1,#20201       ;CHECK SAVED CSR
010400  001401                          BEQ     .+4             ;BRANCH IF CORRECT
010402  104410                          HLT                     ;CSR INCORRECT, SEE CONTENTS SAVED IN R1
010404  032777  000001  170424          BIT     #1,@SR          ;CHECK SWITCH REGISTER SWITCH ONE
010412  001763                          BEQ     LOP37A          ;LOOP IF NOT SET
010414  005077  170372                  CLR     @BUSCSR
010420  032777  001000  170364          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO COMPLETE
010426  001374                          BNE     .-6
010430  104124                          PMSG42                  ;"CLEAR SWITCH REGISTER OF OTHER CPU
                                                                ;THEN CLEAR SWITCH ZERO IN THIS CPU'S SR"
```

```
010432  032777  000001  170376          BIT     #1,@SR          ;WAIT FOR SR TO CLEAR
010440  001374                          BNE     .-6

                                ;CHECK OPERATION OF BITS 11 AND 12
                                ;WHEN OTHER PROCESSOR SETS BIT 11, 12 SHOULD SET HERE
                                ;WHEN OTHER PROCESSOR CLEARS BIT 11, 12 SHOULD CLEAR HERE
                                ;12 SHOULD BE READ ONLY
                                ;NO INTERRUPT SHOULD OCCUR WITH BIT 10 CLEAR
010442  104406                  TEST38: SCOPE
010444  104010                          PMSG4                   ;REQUEST OPERATOR TO CLEAR SWITCH REGISTER OF OTHER CPU,
                                                                ;THEN SET SWITCH TWO
010446  042777  000340  170360          BIC     #340,@PSR       ;ALLOW FALSE INTERRUPTS
010454  000000                          HALT
010456  022777  010000  170326          CMP     #10000,@BUSCSR  ;BIT 12 SET?
010464  001401                          BEQ     .+4             ;YES
010466  104410                          HLT                     ;BIT 12 NOT SET AFTER BIT 11 WAS SET IN THE OTHER
                                                                ;PROCESSOR'S CSR, OR ANOTHER BIT INCORRECT
010470  005077  170316                  CLR     @BUSCSR         ;BIT 12 SHOULD BE READ ONLY
010474  022777  010000  170310          CMP     #10000,@BUSCSR
010502  001401                          BEQ     .+4
010504  104410                          HLT                     ;BIT 12 CLEARED VIA A DATO OR ANOTHER BIT INCORRECT
010506  104012                          PMSG5                   ;REQUEST OPERATOR TO CLEAR SWITCH REGISTER OF OTHER CPU
010510  000000                          HALT                    ;THEN PRESS "CONTINUE" ON THIS PROCESSOR
010512  005777  170274                  TST     @BUSCSR         ;BIT 12 SHOULD BE ZERO SINCE OTHER
010516  001401                          BEQ     .+4             ;PROCESSOR CLEARED BIT 11
010520  104410                          HLT                     ;BIT 12 STILL SET, OR ANOTHER BIT INCORRECT

                                ;IF BIT 10 (IE2) IS SET WHEN 11 ISN'T SET ON OTHER SIDE, NO INTERRUPT SHOULD OCCUR
                                ;IF BIT 10 IS SET WHEN 11 IS ALREADY SET ON OTHER SIDE, AN INTERRUPT SHOULD OCCUR
                                ;IF BIT 10 IS SET AND THEN BIT 11 IS SET ON THE OTHER SIDE, AN INTERRUPT SHOULD OCCUR
010522  104406                  TEST39: SCOPE
010524  104012                          PMSG5                   ;PRINT MESSAGE:  "CHANGE SWITCH REGISTER OF OTHER
                                                                ;PROCESSOR-CLEAR IT. THEN PRESS
                                                                ;'CONTINUE' ON THIS PROCESSOR."
010526  000000                          HALT                    ;CLEARS SWITCH CSR OF OTHER SIDE
010530  042777  000340  170276          BIC     #340,@PSR       ;SET PROCESSOR TO LEVEL 0 TO
010536  012777  010726  170256          MOV     #TINT39,@BSIV2  ;CATCH ANY FALSE INTERRUPT
010544  017777  170264  170252          MOV     @PSR,@BSST2
010552  052777  000340  170244          BIS     #340,@BSST2
010560  012777  002000  170224          MOV     #2000,@BUSCSR   ;SET IE2 ONLY
010566  000240                          NOP                     ;ALLOW WINDOW IN CASE
010570  000240                          NOP
010572  052777  000340  170234          BIS     #340,@PSR       ;SET PROCESSOR BACK TO LEVEL 7
010600  012777  010634  170214          MOV     #TNT39A,@BSIV2  ;CHANGE INTERRUPT RETURN FOR NEXT CHECK
010606  104010                          PMSG4                   ;PRINT MESSAGE:  "CHANGE SWITCH REGISTER OF OTHER
                                                                ;PROCESSOR-CLEAR IT AND THEN SET SWITCH 2 TO A ONE.
010610  000000                          HALT                    ;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."
                                                                ;SETS BIT 11 OF OTHER CSR
010612  042777  000340  170214          BIC     #340,@PSR       ;SET PROCESSOR TO LEVEL 0
010620  000240                          NOP
010622  052777  000340  170204          BIS     #340,@PSR       ;SET PROCESSOR BACK TO LEVEL 7
010630  104410                          HLT                     ;NO INTERRUPT OCCUPRED WHEN BIT
                                                                ;11 WAS SET ON OTHER PROCESSOR AFTER
010632  000401                          BR      .+4             ;BIT 10 WAS SET ON THIS SIDE
010634  022626                  TNT39A: CMP     (SP)+,(SP)+     ;RESTORE STACK
010636  005077  170150                  CLR     @BUSCSR         ;CLEAR INTERRUPT ENABLE
```

```
010642  032777  010000  170142          BIT     #10000,@#BUSCSR ;CHECK BIT 12
010650  001002                          BNE     .+6             ;BRANCH IF STILL SET
010652  104410                          HLT                     ;BIT 12 NO LONGER SET AFTER CLEARING IE2
010654  000426                          BR      CNT39A
010656  012777  010722  170136          MOV     #TNT39B,@#BSIV2 ;SETUP RETURN
010664  017777  170144  170132          MOV     @#PSR,@#BSST2
010672  052777  002000  170112          BIS     #2000,@#BUSCSR  ;SET BIT 10 (IE2)
010700  042777  000340  170126          BIC     #340,@#PSR      ;SET PROCESSOR TO LEVEL 0
010706  000240                          NOP                     ;SWITCH SHOULD INTERRUPT SINCE
                                                                ;BIT 11 ON OTHER SIDE STILL SET
010710  052777  000340  170116          BIS     #340,@#PSR      ;RESTORE PROCESSOR PRIORITY TO LEVEL 7
010716  104410                          HLT                     ;NO INTERRUPT OCCURRED WHEN IE2 WAS SET
                                                                ;WITH BIT 12 ALREADY SET
010720  000404                          BR      CNT39A
010722  022626          TNT39B: CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
010724  000402                          BR      CNT39A
010726  104410          TINT39: HLT                     ;SETTING BIT 10 CAUSED INTERRUPT WITHOUT
                                                        ;BIT 11 SET ON OTHER SIDE
010730  022626                          CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
010732  005077  170066  CNT39A: CLR     @#BSST2         ;CHANGE INTERRUPT RETURN TO CAUSE
010736  016777  170062  170056          MOV     BSST2,@#BSIV2   ;A HALT ON A FALSE INTERRUPT
010744  005077  170042                  CLR     @#BUSCSR        ;REINITIALIZE CSR

                        ;SHOW THAT REREQUESTING THE BUS SWITCH WHEN THE OTHER PROCESSOR HAS NOT
                        ;REQUESTED IT WILL NOT CAUSE THE TIMER TO START
010750  104406          TEST40: SCOPE
010752  104004                  PMSG2                   ;HAVE OPERATOR CAUSE THE OTHER PROCESSOR
                                                        ;TO CLEAR THE BUS SWITCH CSR AND THEN
010754  000000                  HALT                    ;REQUEST THE SWITCH
010756  032777  020000  170026          BIT     #20000,@#BUSCSR ;WAIT FOR NON-NEUTRAL TO SET
010764  001774                          BEQ     .-6
010766  012777  000001  170016          MOV     #1,@#BUSCSR     ;REQUEST SWITCH
010774  005067  170046                  CLR     CNT40           ;INITIALIZE COUNTER
011000  005067  170044                  CLR     CNT40A
011004  062767  000001  170034  LOOP40: ADD     #1,CNT40
011012  005567  170032                  ADC     CNT40A
011016  005777  167770                  TST     @#BUSCSR        ;TIMEOUT SET?
011022  100370                          BPL     LOOP40          ;NO-CONTINUE COUNTING
011024  006367  170016                  ASL     CNT40           ;YES, INCREASE COUNT TO ALLOW MARGIN
011030  006167  170014                  ROL     CNT40A
011034  032777  001000  167750          BIT     #1000,@#BUSCSR  ;WAIT FOR SB INIT TO CLEAR
011042  001374                          BNE     .-6
011044  105777  167742                  TSTB    @#BUSCSR        ;CONNECTED SET?
011050  100401                          BMI     .+4             ;YES-OK
011052  104410                          HLT                     ;NO-TIMEOUT SET BUT CONNECTED DIDN'T
011054  012777  000001  167730          MOV     #1,@#BUSCSR     ;REREQUEST SWITCH, CLEAR TIMEOUT
011062  005777  167724                  TST     @#BUSCSR        ;DID TIMEOUT CLEAR?
011066  100001                          BPL     .+4             ;YES-OK
011070  104410                          HLT                     ;NO-DATO DIDN'T CLEAR TIMEOUT
011072  005467  167750                  NEG     CNT40           ;COUNT DOWN
011076  005267  167746                  INC     CNT40A
011102  062767  000001  167736  LOP40A: ADD     #1,CNT40        ;LOOP SET UP TO TAKE SAME LENGTH
011110  005667  167734                  SBC     CNT40A          ;OF TIME AS PREVIOUS ONE
011114  005737  001050                  TST     @#CNT40A        ;TOTAL TIMING TWICE THAT
011120  001370                          BNE     LOP40A          ;WHICH WAS MEASURED FOR TIMEOUT
011122  022777  020201  167662          CMP     #20201,@#BUSCSR ;CHECK CSR NOW
```

```
011130  001401                          BEQ     .+4
011132  104410                          HLT                     ;TIMEOUT OCCURRED OR ANOTHER BIT IN CSR INCORRECT
011134  005077  167652                  CLR     @BUSCSR         ;INITIALIZE SWITCH
011140  032777  001000  167644          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO COMPLETE
011146  001374                          BNE     .-6
011150  005767  167726                  TST     NOPF            ;IS FLAG SET TO INHIBIT POWER FAIL
011154  100004                          BPL     .+12            ;TESTING?-IF NOT, CONTINUE
011156  104012                          PMSG5                   ;IF SET, REQUEST OPERATOR TO CLEAR SR
011160  000000                          HALT                    ;OF OTHER CPU
011162  000167  004442                  JMP     DONE            ;SKIP POWER FAIL TESTS

                                ;TEST POWER FAIL ON THE PROCESSOR BUS (TEST42 THRU TEST49)
                                ;RUNNING TEST ROUTINES ON BOTH PROCESSORS, POWER DOWN THIS PROCESSOR
                                ;DO THIS TEST ONCE FOR EACH SWITCH POSITION
                                ;NOTE THAT THESE TESTS ALSO SHOW THAT
                                ;THE A AND B PROCESSOR INITS ARE CORRECT

                                ;SHOW THAT THE SWITCH GOES TO NEUTRAL IF IT WAS CONNECTED TO THIS PROCESSOR
                                ;WHEN THE POWER FAIL OCCURRED, AND THAT BIT 14 DOESN'T SET
011166  104406                  TEST42: SCOPE
011170  005767  167706                  TST     NOPF            ;IF DT11-A, THE PREVIOUS CHECK OF POWER
                                                                ;FAIL TESTING BEING INHIBITED WILL BE SKIPPED
                                                                ;SO CHECK IT HERE
011174  100002                          BPL     .+6             ;BRANCH IF NOT INHIBITED
011176  000167  004426                  JMP     DONE            ;SKIP TESTS IF INHIBITED
011202  005767  167676                  TST     DT11AF          ;IF DT11-A, SKIP MESSAGE
011206  001002                          BNE     .+6
011210  104034                          PMSG14                  ;REQUEST OPERATOR TO CLEAR SWITCH REGISTER OF OTHER
                                                                ;PROCESSOR,THEN SET SWITCH 3,
011212  000000                          HALT                    ;AND PRESS CONTINUE ON THIS PROCESSOR
011214  012777  000001  167570          MOV     #1,@BUSCSR      ;REQUEST SWITCH
011222  105777  167564                  TSTB    @BUSCSR         ;WAIT FOR SWITCH TO CONNECT
011226  100375                          BPL     .-4
011230  012737  011250  000024          MOV     #RETA42,@#24    ;SETUP POWER FAIL RETURN
011236  017737  167572  000026          MOV     @PSR,@#26
011244  104052                          PMSG21                  ;PRINT MESSAGE:  "POWER DOWN THIS PROCESSOR AND
                                                                ;THEN POWER THIS PROCESSOR BACK UP"
011246  000777                          BR      .               ;WAIT FOR POWER FAIL TRAP
011250  012737  011300  000024  RETA42: MOV     #RETB42,@#24    ;SETUP POWER UP RETURN
011256  017767  167530  167606          MOV     @BUSCSR,PFSAV   ;SAVE CONTENTS OF CSR FOR CHECKING
011264  010667  167600                  MOV     SP,SPSAV        ;SAVE STACK POINTER
011270  000000                          HALT                    ;HALT ON POWER DOWN
011272  016706  167572                  MOV     SPSAV,SP
011276  104410                          HLT                     ;NO POWER UP RESTART OCCURRED
011300  016706  167564          RETB42: MOV     SPSAV,SP        ;RESTORE STACK POINTER ON POWER UP
011304  022626                          CMP     (SP)+,(SP)+
011306  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER IN POWER
011314  005037  000026                  CLR     @#26            ;FAIL VECTOR ADDRESS
011320  005027  000000                  CLR     #0              ;STALL SO THAT TTY
011324  005367  177772                  DEC     .-2             ;OUTPUT WON'T BE
011330  001375                          BNE     .-4             ;GARBLED
011332  022767  020201  167532          CMP     #20201,PFSAV    ;CHECK SAVED CONTENTS OF CSR AT
011340  001401                          BEQ     .+4             ;TIME OF POWER FAIL-SHOULD NOT HAVE
                                                                ;CHANGED AT THAT POINT
011342  104410                          HLT                     ;CONTENTS OF CSR AT TIME OF
                                                                ;POWER FAIL INCORRECT - SAVED IN
```

```
                                                                ;LOCATION PFSAV
011344  005777  167442                    TST     @BUSCSR       ;CHECK CSR CONTENTS AFTER POWER UP
011350  001401                            BEQ     .+4
011352  104410                            HLT                   ;CSR INCORRECT AFTER POWER DOWN AND UP
                                                                ;SHOULD HAVE BEEN CLEARED BY INIT
011354  012737  011402  000004            MOV     #RET42,@#4    ;SETUP TRAP RETURN
011362  017737  167446  000006            MOV     @PSR,@#6
011370  016777  167462  167456            MOV     RWBITS,@DVADRS ;REFERENCE ADDRESS ON SWITCHED BUS - SHOULD TRAP
011376  104410                            HLT                   ;SWITCHED BUS STILL CONNECTED
011400  000401                            BR      CONT42
011402  022626                  RET42:    CMP     (SP)+,(SP)+   ;RESTORE STACK POINTER
011404  012737  000006  000004  CONT42:   MOV     #6,@#4        ;RESTORE TRAP CATCHER
011412  005037  000006                    CLR     @#6
011416  005077  167370                    CLR     @BUSCSR       ;MAKE SURE SWITCH IS RELEASED
011422  032777  001000  167362            BIT     #1000,@BUSCSR ;WAIT FOR SB INIT TO COMPLETE
011430  001374                            BNE     .-6

                                        ;CHECK PROCESSOR POWER FAIL WITH SWITCH CONTROLLED BY BUT NOT
                                        ;CONNECTED TO THIS PROCESSOR
011432  104406                  TEST43:   SCOPE
011434  005767  167444                    TST     DT11AF        ;IF DT11-A, SKIP MESSAGE
011440  001002                            BNE     .+6
011442  104034                            PMSG14                ;REQUEST OPERATOR TO CLEAR SWITCH REGISTER OF OTHER
                                                                ;PROCESSOR, SET SWITCH 3, AND
011444  000000                            HALT                  ;PRESS CONTINUE ON THIS PROCESSOR
011446  012777  000002  167336            MOV     #2,@BUSCSR    ;REQUEST SWITCH (POSITION 2 OR 4)
011454  105777  167332                    TSTB    @BUSCSR       ;WAIT FOR CONNECTED BIT TO SET
011460  100375                            BPL     .-4
011462  012737  011502  000024            MOV     #RETA43,@#24  ;SETUP POWER FAIL RETURN
011470  017737  167340  000026            MOV     @PSR,@#26
011476  104052                            PMSG21                ;PRINT MESSAGE:  "POWER DOWN THIS PROCESSOR AND
                                                                ;THEN POWER THIS PROCESSOR BACK UP"
011500  000777                            BR      .             ;WAIT FOR POWER FAIL TRAP
011502  012737  011532  000024  RETA43:   MOV     #RETB43,@#24  ;SETUP POWER UP RETURN
011510  017767  167276  167354            MOV     @BUSCSR,PFSAV ;SAVE CONTENTS OF CSR FOR CHECKING
011516  010667  167346                    MOV     SP,SPSAV      ;SAVE STACK POINTER
011522  000000                            HALT                  ;HALT ON POWER DOWN
011524  016706  167340                    MOV     SPSAV,SP
011530  104410                            HLT                   ;NO POWER UP RESTART OCCURRED
011532  016706  167332          RETB43:   MOV     SPSAV,SP      ;RESTORE STACK POINTER ON POWER UP
011536  022626                            CMP     (SP)+,(SP)+
011540  012737  000026  000024            MOV     #26,@#24      ;RESTORE TRAP CATCHER IN POWER
011546  005037  000026                    CLR     @#26          ;FAIL VECTOR ADDRESS
011552  005027  000000                    CLR     #0            ;STALL SO THAT TTY
011556  005367  177772                    DEC     .-2           ;OUTPUT WON'T BE
011562  001375                            BNE     .-4           ;GARBLED
011564  022767  020202  167300            CMP     #20202,PFSAV  ;CHECK SAVED CONTENTS OF CSR AT
011572  001401                            BEQ     .+4           ;TIME OF POWER FAIL - SHOULD NOT HAVE
                                                                ;CHANGED AT THAT POINT
011574  104410                            HLT                   ;CONTENTS OF CSR AT TIME OF POWER
                                                                ;FAIL INCORRECT -( SAVED IN
                                                                ;LOCATION PFSAV)
011576  005777  167210                    TST     @BUSCSR       ;CHECK CSR CONTENTS AFTER POWER UP
011602  001401                            BEQ     .+4
011604  104410                            HLT                   ;CSR INCORRECT AFTER POWER DOWN AND UP
                                                                ;SHOULD HAVE BEEN CLEARED BY INIT
```

```
011606  012737  011634  000004          MOV     #RET43,@#4      ;SETUP TRAP RETURN
011614  017737  167214  000006          MOV     @PSR,@#6
011622  016777  167230  167224          MOV     RWBITS,@OVADRS  ;REFERENCE ADDRESS ON SWITCHED BUS - SHOULD TRAP
011630  104410                          HLT                     ;SWITCHED BUS STILL CONNECTED
011632  000401                          BR      CONT43
011634  022626                  RET43:  CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
011636  012737  000006  000004  CONT43: MOV     #6,@#4          ;RESTORE TRAP CATCHER
011644  005037  000006                  CLR     @#6
011650  005077  167136                  CLR     @BUSCSR         ;MAKE SURE SWITCH IS RELEASED
011654  032777  001000  167130          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO COMPLETE
011662  001374                          BNE     .-6

                                ;CHECK PROCESSOR POWER FAIL WITH SWITCH IN NEUTRAL
011664  104406                  TEST44: SCOPE
011666  005767  167212                  TST     DT11AF          ;IF DT11-A, SKIP MESSAGE
011672  001002                          BNE     .+6
011674  104034                          PMSG14                  ;REQUEST OPERATOR TO CLEAR SWITCH REGISTER OF OTHER
                                                                ;PROCESSOR, SET SWITCH 3, AND
011676  000000                          HALT                    ;PRESS CONTINUE ON THIS PROCESSOR
011700  005077  167106                  CLR     @BUSCSR         ;PUT SWITCH IN NEUTRAL
011704  012737  011724  000024          MOV     #RETA44,@#24    ;SETUP POWER FAIL RETURN
011712  017737  167116  000026          MOV     @PSR,@#26
011720  104052                          PMSG21                  ;PRINT MESSAGE:  "POWER DOWN THIS PROCESSOR AND
                                                                ;THEN POWER THIS PROCESSOR BACK UP"
011722  000777                          BR      .               ;WAIT FOR POWER FAIL TRAP
011724  012737  011754  000024  RETA44: MOV     #RETB44,@#24    ;SETUP POWER UP RETURN
011732  017767  167054  167132          MOV     @BUSCSR,PFSAV   ;SAVE CONTENTS OF CSR FOR CHECKING
011740  010667  167124                  MOV     SP,SPSAV        ;SAVE STACK POINTER
011744  000000                          HALT                    ;HALT ON POWER DOWN
011746  016706  167116                  MOV     SPSAV,SP
011752  104410                          HLT                     ;NO POWER UP RESTART OCCURRED
011754  016706  167110          RETB44: MOV     SPSAV,SP        ;RESTORE STACK POINTER ON POWER UP
011760  022626                          CMP     (SP)+,(SP)+
011762  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER IN POWER
011770  005037  000026                  CLR     @#26            ;FAIL VECTOR ADDRESS
011774  005027  000000                  CLR     #0              ;STALL SO THAT TTY
012000  005367  177772                  DEC     .-2             ;OUTPUT WON'T BE
012004  001375                          BNE     .-4             ;GARBLED
012006  005767  167060                  TST     PFSAV           ;CHECK SAVED CONTENTS OF CSR AT
012012  001401                          BEQ     .+4             ;TIME OF POWER FAIL - SHOULD HAVE BEEN
                                                                ;CLEARED SINCE CSR WAS PREVIOUSLY CLEARED
012014  104410                          HLT                     ;CONTENTS OF CSR AT TIME OF POWER
                                                                ;DOWN INCORRECT (SAVED IN PFSAV)
012016  005777  166770                  TST     @BUSCSR         ;CHECK CSR CONTENTS AFTER POWER UP
012022  001401                          BEQ     .+4
012024  104410                          HLT                     ;CSR INCORRECT AFTER POWER DOWN AND UP
012026  005767  167052                  TST     DT11AF          ;IF DT11-A, SKIP TO TEST50
012032  001402                          BEQ     .+6
012034  000167  001002                  JMP     TEST50

                                ;CHECK PROCESSOR POWER FAIL WITH SWITCH CONTROLLED BY BUT NOT CONNECTED TO
                                ;THE OTHER PROCESSOR
012040  104406                  TEST45: SCOPE
012042  104036                          PMSG15                  ;REQUEST OPERATOR TO CLEAR SWITCH REGISTER OF OTHER
                                                                ;PROCESSOR, SET SWITCH FOUR, AND
012044  000000                          HALT                    ;PRESS CONTINUE ON THIS PROCESSOR
```

```
012046  005077  166740                  CLR     @#BUSCSR        ;INITIALIZE CSR
012052  012737  012072  000024          MOV     #RETA45,@#24    ;SETUP POWER FAIL RETURN
012060  017737  166750  000026          MOV     @#PSR,@#26
012066  104052                          PMSG21                  ;PRINT MESSAGE:  "POWER DOWN THIS PROCESSOR AND
                                                                ;THEN POWER THIS PROCESSOR BACK UP"
012070  000777                          BR      .               ;WAIT FOR POWER FAIL TRAP
012072  012737  012122  000024  RETA45: MOV     #RETB45,@#24    ;SETUP POWER UP RETURN
012100  017767  166706  166764          MOV     @#BUSCSR,PFSAV  ;SAVE CONTENTS OF CSR FOR CHECKING
012106  010667  166756                  MOV     SP,SPSAV        ;SAVE STACK POINTER
012112  000000                          HALT                    ;HALT ON POWER DOWN
012114  016706  166750                  MOV     SPSAV,SP
012120  104410                          HLT                     ;NO POWER UP RESTART OCCURRED
012122  016706  166742          RETB45: MOV     SPSAV,SP        ;RESTORE STACK POINTER ON POWER UP
012126  022626                          CMP     (SP)+,(SP)+
012130  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER IN POWER
012136  005037  000026                  CLR     @#26            ;FAIL VECTOR ADDRESS
012142  005027  000000                  CLR     #0              ;STALL SO THAT TTY
012146  005367  177772                  DEC     .-2             ;OUTPUT WON'T BE
012152  001375                          BNE     .-4             ;GARBLED
012154  022767  020000  166710          CMP     #20000,PFSAV    ;CHECK SAVED CONTENTS OF CSR AT
012162  001401                          BEQ     .+4             ;TIME OF POWER DOWN - ONLY NON-
                                                                ;NEUTRAL SHOULD HAVE BEEN SET
012164  104410                          HLT                     ;CSR AT TIME OF POWER DOWN
                                                                ;INCORRECT (SAVED IN PFSAV)
012166  022777  020000  166616          CMP     #20000,@#BUSCSR ;CHECK CSR CONTENTS AFTER POWER UP
012174  001401                          BEQ     .+4
012176  104410                          HLT                     ;CSR INCORRECT AFTER POWER UP

                                ;CHECK PROCESSOR POWER FAIL WITH SWITCH CONNECTED TO THE OTHER PROCESSOR
012200  104406                  TEST46: SCOPE
012202  104040                          PMSG16                  ;REQUEST OPERATOR TO CLEAR SWITCH
                                                                ;REGISTER OF OTHER PROCESSOR.
                                                                ;SET SWITCH 5, AND PRESS CONTINUE
012204  000000                          HALT                    ;ON THIS PROCESSOR
012206  005077  166600                  CLR     @#BUSCSR        ;INITIALIZE CSR
012212  012737  012232  000024          MOV     #RETA46,@#24    ;SETUP POWER FAIL RETURN
012220  017737  166610  000026          MOV     @#PSR,@#26
012226  104052                          PMSG21                  ;PRINT MESSAGE:  "POWER DOWN THIS PROCESSOR AND
                                                                ;THEN POWER THIS PROCESSOR BACK UP"
012230  000777                          BR      .               ;WAIT FOR POWER FAIL TRAP
012232  012737  012262  000024  RETA46: MOV     #RETB46,@#24    ;SETUP POWER UP RETURN
012240  017767  166546  166624          MOV     @#BUSCSR,PFSAV  ;SAVE CONTENTS OF CSR FOR CHECKING
012246  010667  166616                  MOV     SP,SPSAV        ;SAVE STACK POINTER
012252  000000                          HALT                    ;HALT ON POWER DOWN
012254  016706  166610                  MOV     SPSAV,SP
012260  104410                          HLT                     ;NO POWER UP RESTART OCCURRED
012262  016706  166602          RETB46: MOV     SPSAV,SP        ;RESTORE STACK POINTER ON POWER UP
012266  022626                          CMP     (SP)+,(SP)+
012270  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER IN POWER
012276  005037  000026                  CLR     @#26            ;FAIL VECTOR ADDRESS
012302  005027  000000                  CLR     #0              ;STALL SO THAT TTY
012306  005367  177772                  DEC     .-2             ;OUTPUT WON'T BE
012312  001375                          BNE     .-4             ;GARBLED
012314  022767  020000  166550          CMP     #20000,PFSAV    ;CHECK SAVED CONTENTS OF CSR AT TIME
012322  001401                          BEQ     .+4             ;OF POWER DOWN - ONLY NON-NEUTRAL
                                                                ;SHOULD HAVE BEEN SET
```

```
012324  104410                          HLT                     ;CSR INCORRECT AT TIME OF POWER DOWN
                                                                ;(SAVED IN PFSAV)
012326  022777  020000  166456          CMP     #20000,@BUSCSR  ;CHECK CSR CONTENTS AFTER POWER UP
012334  001401                          BEQ     .+4
012336  104410                          HLT                     ;CSR INCORRECT AFTER POWER UP

                                ;TEST THAT WHEN POWER DOWN OCCURS ON THIS PROCESSOR, THE OTHER PROCESSOR
                                ;CAN GET THE SWITCH

                                ;CHECK WITH SWITCH IN THE CONNECTED AND CONTROLLED POSITION
012340  104406                  TEST47: SCOPE
012342  104042                          PMSG17                  ;REQUEST OPERATOR TO CLEAR SWITCH REGISTER OF OTHER
                                                                ;PROCESSOR, SET SWITCH 6, AND THEN
012344  000000                          HALT                    ;PRESS CONTINUE ON THIS PROCESSOR
012346  012737  012430  000024          MOV     #RETA47,@#24    ;SETUP POWER DOWN RETURN
012354  017737  166454  000026          MOV     @PSR,@#26
012362  104074                          PMSG30                  ;PRINT MESSAGE: "WHEN THIS
012364  104052                          PMSG21                  ;PRINTOUT IS FINISHED, PRESS
012366  000000                          HALT                    ;"CONTINUE", THEN POWER DOWN
                                                                ;THIS PROCESSOR AND THEN POWER
                                                                ;THIS PROCESSOR BACK UP."
012370  012777  000001  166414          MOV     #1,@BUSCSR      ;REQUEST SWITCH
012376  000774                          BR      .-6             ;REREQUEST SWITCH UNTIL POWER DOWN OCCURS
                                                                ;TO AVOID TIMEOUT
012400  012737  012430  000024  RETA47: MOV     #RETB47,@#24    ;SETUP POWER UP RETURN
012406  017767  166430  166456          MOV     @BUSCSR,PFSAV   ;SAVE CONTENTS OF CSR FOR CHECKING
012414  010467  166450                  MOV     SP,SPSAV        ;SAVE STACK POINTER
012420  000000                          HALT                    ;HALT ON POWER DOWN
012422  016706  166442                  MOV     SPSAV,SP
012426  104410                          HLT                     ;NO POWER UP RESTART OCCURRED
012430  016706  166434          RETB47: MOV     SPSAV,SP        ;RESTORE STACK POINTER ON POWER UP
012434  022626                          CMP     (SP)+,(SP)+
012436  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER IN POWER
012444  005037  000026                  CLR     @#26            ;FAIL VECTOR ADDRESS
012450  005007                          CLR     PC              ;STALL SO THAT TTY
012452  005007  177772                  CLR     -2(PC)          ;OUTPUT WON'T BE
012456  001375                          BNE     .-4             ;CLOBBERED
012460  022767  020201  166402          CMP     #20201,PFSAV    ;CHECK SAVED CONTENTS OF CSR
012466  001401                          BEQ     .+4             ;AT TIME OF POWER DOWN
012470  104410                          HLT                     ;CSR INCORRECT AT TIME OF POWER DOWN TRAP
                                                                ;(PFSAV CONTAINS SAVED CONTENTS)
012472  022777  020000  166310          CMP     #20000, @BUSCSR ;CHECK CSR AFTER POWER UP
012500  001401                          BEQ     .+4
012502  104410                          HLT                     ;CSR INCORRECT AFTER POWER UP - SHOULD BE
                                                                ;CONNECTED TO THE OTHER CPU
012504  005077  166300                  CLR     @BUSCSR
012510  032777  001000  166272          BIT     #1000,@BUSCSR
012516  001374                          BNE     .-6

                                ;CHECK WITH SWITCH IN THE CONTROLLED BUT NOT CONNECTED POSITION
012520  104406                  TEST48: SCOPE
012522  005077  166262                  CLR     @BUSCSR         ;INITIALIZE CSR
012526  104042                          PMSG17                  ;REQUEST OPERATOR TO CLEAR SWITCH REGISTER OF OTHER
                                                                ;PROCESSOR, SET SWITCH 6, AND THEN
012530  000000                          HALT                    ;PRESS CONTINUE ON THIS PROCESSOR
012532  012737  012564  000024          MOV     #RETA48,@#24    ;SETUP POWER DOWN RETURN
```

```
012542  017737  166266  000026          MOV     @#PSR,@#26
012550  104074                          PMSG30
012552  104052                          PMSG21
012554  000000                          HALT

012556  012777  000002  166226          MOV     #2,@BUSCSR      ;REQUEST SWITCH
012564  000774                          BR      .-6             ;REREQUEST SWITCH UNTIL POWER DOWN OCCURS
                                                                ;TO AVOID TIMEOUT
012566  012737  012616  000024  RETA48: MOV     #RETB48,@#24    ;SETUP POWER UP RETURN
012574  017767  166212  166270          MOV     @BUSCSR,PFSAV   ;SAVE CONTENTS OF CSR FOR CHECKING
012602  010667  166262                  MOV     SP,SPSAV        ;SAVE STACK POINTER
012606  000000                          HALT                    ;HALT ON POWER DOWN
012610  016706  166254                  MOV     SPSAV,SP
012614  104410                          HLT                     ;NO POWER UP RESTART OCCURRED
012616  016706  166246          RETB48: MOV     SPSAV,SP        ;RESTORE STACK POINTER ON POWER UP
012622  022626                          CMP     (SP)+,(SP)+
012624  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER IN POWER
012632  005037  000026                  CLR     @#26            ;FAIL VECTOR ADDRESS
012636  005027  000000                  CLR     #0              ;STALL SO THAT TTY
012642  005367  177772                  DEC     .-2             ;OUTPUT WON'T BE
012646  001375                          BNE     .-4             ;GARBLED
012650  022767  020202  166214          CMP     #20202,PFSAV    ;CHECK SAVED CONTENTS OF CSR
012656  001401                          BEQ     .+4             ;AT TIME OF POWER DOWN
012660  104410                          HLT                     ;CSR INCORRECT AT TIME OF POWER
                                                                ;DOWN (PFSAV CONTAINS SAVED CONTENTS)
012662  022777  020000  166122          CMP     #20000,@BUSCSR  ;CHECK CSR AFTER POWER UP
012670  001401                          BEQ     .+4
012672  104410                          HLT                     ;CSR INCORRECT AFTER POWER UP
012674  005077  166112                  CLR     @BUSCSR
012700  032777  001000  166104          BIT     #1000,@BUSCSR
012706  001374                          BNE     .-6

                                ;CHECK WITH SWITCH IN NEUTRAL
012710  104406                  TEST49: SCOPE
012712  104012                          PMSG5                   ;REQUEST OPERATOR TO CLEAR
012714  000000                          HALT                    ;SWITCH REGISTER OF OTHER PROCESSOR
                                                                ;AND THEN PRESS "CONTINUE" ON THIS PROCESSOR
012716  012737  012736  000024          MOV     #PFTA49,@#24    ;SETUP POWER DOWN RETURN
012724  017737  166104  000026          MOV     @#PSR,@#26
012732  104054                          PMSG22                  ;PRINT MESSAGE:  "POWER DOWN THIS PROCESSOR,
                                                                ;CHANGE THE SWITCH REGISTER OF THE
                                                                ;OTHER PROCESSOR - SET SWITCH NINE
                                                                ;TO A ONE AND THEN POWER THIS
                                                                ;PROCESSOR BACK UP."
012734  000777                          BR      .               ;WAIT FOR POWER FAIL TRAP TO OCCUR
012736  012737  012766  000024  RETA49: MOV     #RETB49,@#24    ;SETUP POWER UP RETURN
012744  017767  166042  166120          MOV     @BUSCSR,PFSAV   ;SAVE CONTENTS OF CSR FOR CHECKING
012752  010667  166112                  MOV     SP,SPSAV        ;SAVE STACK POINTER
012756  000000                          HALT                    ;POWER DOWN HALT
012760  016706  166104                  MOV     SPSAV,SP
012764  104410                          HLT                     ;POWER UP RESTART NEVER OCCURRED AFTER POWER DOWN
012766  016706  166076          RETB49: MOV     SPSAV,SP        ;RESTORE STACK ON POWER UP
012772  022626                          CMP     (SP)+,(SP)+
012774  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER IN POWER
013002  005037  000026                  CLR     @#26            ;FAIL VECTOR ADDRESS
```

```
013006  005027  000000                  CLR     #0              ;STALL SO THAT TTY
013012  005367  177772                  DEC     .-2             ;OUTPUT WILL BE OK
013016  001375                          BNE     .-4
013020  005767  166046                  TST     PFSAV           ;CHECK SAVED CONTENTS OF CSR
013024  001401                          BEQ     .+4             ;AT TIME OF POWER DOWN
013026  104410                          HLT                     ;CSR INCORRECT AT TIME OF POWER
                                                                ;DOWN (PFSAV CONTAINS SAVED
                                                                ;CONTENTS)-SHOULDN'T HAVE CHANGED FROM NEUTRAL
013030  022777  020000  165754          CMP     #20000,@BUSCSR  ;CHECK CSR AFTER POWER UP
013036  001401                          BEQ     .+4
013040  104410                          HLT                     ;CSR INCORRECT AFTER POWER UP - SHOULD SHOW
                                                                ;SWITCH CONNECTED TO OTHER PROCESSOR

                                ;SHOW THAT IF THE SWITCH IS POWERED DOWN,
                                ;BOTH CPU'S WILL POWER FAIL TRAP
                                ;SHOW THAT BIT 14 WILL BE SET IN THE CSR'S OF BOTH
                                ;SIDES OF THE SWITCH AFTER THE POWER DOWN TRAP.
                                ;WHEN THE SWITCH IS POWERED BACK
                                ;UP, BOTH CSR'S SHOULD BE CLEAR (ZERO)
                                ;TEST THIS WITH THE SWITCH CONNECTED TO THIS PROCESSOR,
                                ;CONTROLLED BUT NOT CONNECTED, AND IN NEUTRAL


                                ;FIRST CHECK IT WITH THE SWITCH CONNECTED
                                ;TO THIS PROCESSOR
013042  104406                  TEST50: SCOPE
013044  005767  166034                  TST     DT11AF          ;IF DT11-A, SKIP MESSAGE
013050  001002                          BNE     .+6
013052  104044                          PMSG18                  ;PRINT MESSAGE: "CHANGE SWITCH REGISTER
                                                                ;OF OTHER PROCESSOR. CLEAR IT AND THEN
                                                                ;SET SWITCH SEVEN TO A ONE. THEN PRESS
                                                                ;'CONTINUE' ON THIS PROCESSOR."
013054  000000                          HALT
013056  012777  000001  165726          MOV     #1,@BUSCSR      ;REQUEST THE SWITCH
013064  105777  165722                  TSTB    @BUSCSR         ;WAIT FOR SWITCH TO
013070  100375                          BPL     .-4             ;CONNECT
013072  012737  013112  000024          MOV     #RET50A,@#24    ;SETUP POWER FAIL RETURN
013100  017737  165730  000026          MOV     @PSR,@#26
013106  104056                          PMSG23                  ;PRINT MESSAGE:  "POWER DOWN THE BUS SWITCH, THEN POWER
                                                                ;THE BUS SWITCH BACK UP."
013110  000777                          BR      .               ;WAIT FOR POWER FAIL TRAP
013112  012737  013142  000024  RET50A: MOV     #RET50B,@#24            ;SETUP POWER UP RETURN
013120  017767  165666  165744          MOV     @BUSCSR,PFSAV   ;SAVE CSR ON POWER DOWN
013126  010667  165736                  MOV     SP,SPSAV        ;SAVE STACK POINTER
013132  000000                          HALT                    ;POWER DOWN HALT
013134  016706  165730                  MOV     SPSAV,SP
013140  104410                          HLT                     ;POWER UP RESTART NEVER OCCURRED AFTER POWER DOWN
013142  016706  165722          RET50B: MOV     SPSAV,SP        ;RESTORE STACK POINTER ON POWER UP
013146  022626                          CMP     (SP)+,(SP)+
013150  005027  000000                  CLR     #0              ;STALL SO THAT TTY OUTPUT
013154  005367  177772                  DEC     .-2             ;WILL BE OK
013160  001375                          BNE     .-4
013162  022767  060201  165702          CMP     #60201,PFSAV    ;CHECK SAVED CONTENTS OF
                                                                ;CSR ON POWER DOWN
013170  001401                          BEQ     .+4
013172  104410                          HLT                     ;CSR INCORRECT ON POWER DOWN
                                                                ;BIT 14 SHOULD HAVE BEEN SET
```

```
                                                        ;AND SWITCH SHOULD STILL HAVE BEEN IN POSITION REQUESTED
013174  005777  165612                TST     @BUSCSR       ;CSR SHOULD BE CLEARED ON POWER UP
013200  001401                        BEQ     .+4
013202  104410                        HLT                   ;CSR NOT CLEAR (ZERO) AFTER
                                                              ;SWITCH POWERED DOWN AND BACK UP
013204  012737  000026  000024        MOV     #26,@#24      ;F. STORE TRAP CATCHER IN
013212  005037  000C36                CLR     @#36          ;POWER FAIL TRAP VECTOR
013216  012737  013244  000004        MOV     #RET5DC,@#4   ;SETUP ADDRESS TIMEOUT RETURN
013224  017737  165604  000006        MOV     @PSR,@#6
013232  016777  165620  165614        MOV     RWBITS,@DVADRS ;CHECK TO SEE IF SWITCHED BUS IS STILL CONNECTED
                                                              ;BY REFERENCING AN ADDRESS ON THE SWITCHED BUS
013240  104410                        HLT                   ;SWITCHED BUS STILL CONNECTED
                                                              ;AFTER SWITCH WAS POWERED DOWN AND BACK UP
013242  000401                        BR      CONT5D
013244  022626              RET5DC:   CMP     (SP)+,(SP)+   ;RESTORE STACK POINTER AFTER TIMEOUT TRAP
013246  012737  000006  000004 CONT5D: MOV     #6,@#4        ;RESTORE TRAP CATCHER
013254  005037  000006                CLR     @#6
013260  005077  165526                CLR     @BUSCSR       ;REINITIALIZE SWITCH
013264  032777  001000  165520        BIT     #1000,@BUSCSR
013272  001374                        BNE     .-6

                                      ;NOW CHECK SWITCH POWER FAIL WITH THE
                                      ;SWITCH INITIALLY CONTROLLED BY BUT NOT
                                      ;CONNECTED TO THIS PROCESSOR
013274  104406              TEST51:   SCOPE
013276  005767  165602                TST     DT11AF        ;IF DT11-A, SKIP MESSAGE
013302  001002                        BNE     .+6
013304  104044                        PMSG1B                ;PRINT MESSAGE: "CHANGE SWITCH REGISTER
                                                              ;OF OTHER PROCESSOR. CLEAR IT AND THEN
                                                              ;SET SWITCH SEVEN TO A ONE. THEN PRESS
                                                              ;'CONTINUE' ON THIS PROCESSOR."
013306  000000                        HALT
013310  012777  000002  165474        MOV     #2,@BUSCSR    ;REQUEST THE SWITCH
013316  105777  165470                TSTB    @BUSCSR       ;WAIT FOR SWITCH TO
013322  100375                        BPL     .-4           ;CONNECT
013324  012737  013344  000024        MOV     #RET51A,@#24  ;SETUP POWER FAIL RETURN
013332  017737  165476  000026        MOV     @PSR,@#26
013340  104056                        PMSG23                ;PRINT MESSAGE:  "POWER DOWN THE BUS SWITCH, THEN POWER
                                                              ;THE BUS SWITCH BACK UP."
013342  000777                        BR      .             ;WAIT FOR POWER FAIL TRAP
013344  012737  013374  000024 RET51A: MOV     #RET51B,@#24
                                                                    ;SETUP POWER UP RETURN
013352  017767  165434  165512        MOV     @BUSCSR,PFSAV ;SAVE CSR ON POWER DOWN
013360  010667  165504                MOV     SP,SPSAV      ;SAVE STACK POINTER
013364  000000                        HALT                  ;POWER DOWN HALT
013366  016706  165476                MOV     SPSAV,SP
013372  104410                        HLT
013374  016706  165470        RET51B: MOV     SPSAV,SP      ;POWER UP RESTART NEVER OCCURRED AFTER POWER DOWN
013400  022626                        CMP     (SP)+,(SP)+   ;RESTORE STACK POINTER ON POWER UP
013402  005227  000000                INC     #0
013406  001367  177772                BNE     .-2           ;STALL SO THAT TTY OUTPUT
013412  001375                        BNE     .-4           ;WILL BE OK
013414  022767  060202  165450        CMP     #60202,PFSAV  ;CHECK SAVED CONTENTS OF
                                                              ;CSR ON POWER DOWN
013422  001401                        BEQ     .+4
013424  104410                        HLT                   ;CSR INCORRECT ON POWER DOWN
                                                              ;BIT 14 SHOULD HAVE BEEN SET
                                                              ;AND SWITCH SHOULD STILL HAVE BEEN IN POSITION REQUESTED
```

```
013426  005777  165360                  TST     @BUSCSR         ;CSR SHOULD BE CLEARED ON POWER UP
013432  001401                          BEQ     .+4
013434  104410                          HLT                     ;CSR NOT CLEAR (ZERO) AFTER
                                                                ;SWITCH POWERED DOWN AND BACK UP
013436  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER IN
013444  005037  000026                  CLR     @#26            ;POWER FAIL TRAP VECTOR
013450  012737  013476  000004          MOV     #RET51C,@#4     ;SETUP ADDRESS TIMEOUT RETURN
013456  017737  165352  000006          MOV     @PSR,@#6
013464  016777  165366  165362          MOV     R4BITS,@DVADRS  ;CHECK TO SEE IF SWITCHED BUS IS STILL CONNECTED
                                                                ;BY REFERENCING AN ADDRESS ON THE SWITCHED BUS
013472  104410                          HLT                     ;SWITCHED BUS STILL CONNECTED
                                                                ;AFTER SWITCH WAS POWERED DOWN AND BACK UP
013474  000401                          BR      CONT51
013476  022626                  RET51C: CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER AFTER TIMEOUT TRAP
013500  012737  000006  000004  CONT51: MOV     #6,@#4          ;RESTORE TRAP CATCHER
013506  005037  000006                  CLR     @#6
013512  005077  165274                  CLR     @BUSCSR         ;REINITIALIZE SWITCH
013516  032777  001000  165266          BIT     #1000,@BUSCSR
013524  001374                          BNE     .-6

                                ;FINALLY, CHECK SWITCH POWER FAIL WITH THE
                                ;SWITCH INITIALLY IN NEUTRAL
013526  104406                  TEST52: SCOPE
013530  005767  165350                  TST     DT11AF          ;IF DT11-A, SKIP MESSAGE
013534  001002                          BNE     .+6
013536  104044                          PMSG18                  ;PRINT MESSAGE: "CHANGE SWITCH REGISTER
                                                                ;OF OTHER PROCESSOR. CLEAR IT AND THEN
                                                                ;SET SWITCH SEVEN TO A ONE. THEN PRESS
013540  000000                          HALT                    ;'CONTINUE' ON THIS PROCESSOR."
013542  012777  000000  165242          MOV     #0,@BUSCSR      ;PUT THE SWITCH IN NEUTRAL
013550  032777  001000  165234          BIT     #1000,@BUSCSR   ;WAIT FOR BIT 9 TO CLEAR
013556  100774                          BMI     .-6
013560  012737  013600  000024          MOV     #RET52A,@#24    ;SETUP POWER FAIL RETURN
013566  017737  165242  000026          MOV     @PSR,@#26
013574  104056                          PMSG23                  ;PRINT MESSAGE:  "POWER DOWN THE BUS SWITCH, THEN POWER
                                                                ;THE BUS SWITCH BACK UP."
013576  000777                          BR      .               ;WAIT FOR POWER FAIL TRAP
013600  012737  013630  000024  RET52A: MOV     #RET52B,@#24            ;SETUP POWER UP RETURN
013606  017767  165200  165256          MOV     @BUSCSR,PFSAV   ;SAVE CSR ON POWER DOWN
013614  010667  165250                  MOV     SP,SPSAV        ;SAVE STACK POINTER
013620  000000                          HALT                    ;POWER DOWN HALT
013622  016706  165242                  MOV     SPSAV,SP
013626  104410                          HLT                     ;POWER UP RESTART NEVER OCCURRED AFTER POWER DOWN
013630  016706  165234          RET52B: MOV     SPSAV,SP        ;RESTORE STACK POINTER ON POWER UP
013634  022626                          CMP     (SP)+,(SP)+
013636  005027  000000                  CLR     #0              ;STALL SO THAT TTY OUTPUT
013642  005367  177772                  DEC     .-2             ;WILL BE OK
013646  001375                          BNE     .-4
013650  022767  040000  165214          CMP     #40000,PFSAV    ;CHECK SAVED CONTENTS OF
                                                                ;CSR ON POWER DOWN
013656  001401                          BEQ     .+4
013660  104410                          HLT                     ;CSR INCORRECT ON POWER DOWN
                                                                ;BIT 14 SHOULD HAVE BEEN SET
                                                                ;AND SWITCH SHOULD STILL HAVE BEEN IN POSITION REQUESTED
013662  005777  165124                  TST     @BUSCSR         ;CSR SHOULD BE CLEARED ON POWER UP
013666  001401                          BEQ     .+4
```

```
013670  104410                          HLT                     ;CSR NOT CLEAR (ZERO) AFTER
                                                                ;SWITCH POWERED DOWN AND BACK UP
013672  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER IN
013700  005037  000026                  CLR     @#26            ;POWER FAIL TRAP VECTOR
013704  005077  165102                  CLR     @#BUSCSR        ;REINITIALIZE SWITCH
013710  032777  001000  165074          BIT     #1000,@#BUSCSR
013716  001374                          BNE     .-6

                                ;SHOW THAT IF A DEVICE ON THE SWITCHED BUS IS POWERED DOWN,
                                ;THE SWITCH WILL GO TO NEUTRAL AND, AFTER DC LO HAS OCCURRED
                                ;ON THE SWITCHED BUS, THE SWITCH CANNOT BE CONNECTED TO
                                ;EITHER PROCESSOR UNTIL THE DEVICE IS POWERED BACK UP.
                                ;BIT 14 SHOULD REMAIN SET UNTIL THE DEVICE IS POWERED UP
                                ;THESE TESTS ARE PARTIALLY INHIBITED IF SW9 IS SET SINCE THAT INDICATES
                                ;THAT THE POWER SUPPLIES ON THE SWITCHED BUS WON'T HOLD DOWN AC AND
                                ;DC LO WHEN POWERED DOWN
013720  105767  165127                  TSTB    SBINH+1         ;IF SW 8 WAS SET, INHIBIT ALL SWITCHED BUS
                                                                ;POWER FAIL TESTING
013724  001407                          BEQ     CNTSB
013726  005767  165152                  TST     DT11AF          ;SKIP MESSAGE IF DT11-A
013732  001002                          BNE     .+6
013734  104012                          PMSG5                   ;REQUEST OPERATOR TO CLEAR SR OF OTHER CPU
013736  000000                          HALT
013740  000167  001664                  JMP     DONE
013744  105767  165102          CNTSB:  TSTB    SBINH           ;SWITCHED BUS POWER DOWN INHIBITED?
013750  001402                          BEQ     TEST53          ;NO-RUN TESTS
013752  000167  001354                  JMP     TEST55          ;YES, SKIP TESTS

                                ;FIRST, CHECK IT WITH THE SWITCH CONNECTED TO THIS PROCESSOR
013756  104406                  TEST53: SCOPE
013760  005767  165120                  TST     DT11AF
013764  001002                          BNE     .+6
013766  104046                          PMSG19                  ;PRINT MESSAGE:"CHANGE SWITCH REGISTER OF THE
                                                                ;OTHER PROCESSOR. CLEAR IT
                                                                ;AND THEN SET SWITCH EIGHT TO A ONE.
013770  000000                          HALT                    ;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."
013772  012777  000001  165012          MOV     #1,@#BUSCSR     ;REQUEST SWITCH
014000  012737  014044  000024          MOV     #RET53A,@#24    ;SETUP POWER FAIL RETURN
014006  017737  165022  000026          MOV     @#PSR,@#26
014014  104014                          PMSG6                   ;PRINT MESSAGE: "POWER DOWN ONE DEVICE ON THE SWITCHED
                                                                ;BUS.  AND THEN SET SWITCH 0 IN THIS
                                                                ;PROCESSOR'S SWITCH REGISTER."
014016  032777  000001  165012          BIT     #1,@SR          ;WAIT FOR SWITCH REGISTER SWITCH 0 TO SET
014024  001774                          BEQ     .-6             ;SHOULD TRAP OUT DUE TO POWER FAIL
014026  104410                          HLT                     ;NO POWER FAIL TRAP ON POWERING DOWN A
                                                                ;SWITCHED BUS DEVICE WHEN THIS PROCESSOR
                                                                ;HAD THE SWITCH
014030  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER
014036  005037  000026                  CLR     @#26
014042  000474                          BR      CONT53
014044  012737  014074  000024  RET53A: MOV     #RET53B,@#24    ;SETUP POWER UP RETURN
014052  010667  165012                  MOV     SP,SPSAV        ;SAVE STACK POINTER
014056  017767  164730  165006          MOV     @#BUSCSR,PFSAV  ;SAVE CSR AT TIME OF POWER DOWN TRAP
014064  000000                          HALT                    ;NO POWER UP OCCURRED AFTER SWITCHED BUS
                                                                ;DEVICE WAS POWERED DOWN.  THE SWITCH SHOULD
                                                                ;HAVE GONE TO NEUTRAL AND ALLOWED THE CPU
```

```
                                                                        ;TO POWER BACK UP
014066  016706  164776                      MOV     SPSAV,SP
014072  104410                              HLT                         ;NO POWER UP RESTART OCCURRED
014074  016706  164770              RET53B: MOV     SPSAV,SP            ;RESTORE STACK POINTER
014100  022626                              CMP     (SP)+,(SP)+
014102  012737  014364  000024              MOV     #RET53D,@#24        ;SETUP NEW POWER FAIL VECTOR IN CASE
                                                                        ;SWITCH CONNECTS WHEN REQUESTED
014110  005027  000000                      CLR     #0                  ;STALL SO THAT TTY
014114  005367  177772                      DEC     .-2                 ;OUTPUT WILL BE OK
014120  001375                              BNE     .-4
014122  032777  000001  164706              BIT     #1,@SR              ;WAIT FOR SWITCH REGISTER SWITCH 0 TO BE SET
014130  001774                              BEQ     .-6
014132  022767  060201  164732              CMP     #60201,PFSAV        ;CHECK SAVED CONTENTS OF CSR AT TIME OF
                                                                        ;POWER DOWN TRAP
014140  001401                              BEQ     .+4
014142  104410                              HLT                         ;CSR INCORRECT WHEN THE POWER FAIL OCCURRED
014144  022777  040000  164640              CMP     #40000,@BUSCSR      ;CHECK CSR NOW - BIT 14 SHOULD BE SET
014152  001401                              BEQ     .+4
014154  104410                              HLT                         ;CSR INCORRECT - ONLY BIT 14 SHOULD BE SET
014156  012777  000001  164626              MOV     #1,@BUSCSR          ;REQUEST SWITCH - SHOULDN'T CONNECT SINCE
                                                                        ;SB DEVICE IS POWERED DOWN
014164  005327  000000                      DEC     #0                  ;S ALL
014170  001375                              BNE     .-4
014172  022777  040001  164612              CMP     #40001,@BUSCSR      ;CK CSR
014200  001401                              BEQ     .+4
014202  104410                              HLT                         ;CSR INCORRECT - ONLY REQUEST AND BIT 14
                                                                        ;SHOULD BE SET
014204  012737  014224  000004              MOV     #RET53C,@#4         ;SETUP ADDRESS TIMEOUT RETURN
014212  016777  164640  164634              MOV     RWBITS,@DVADRS      ;REFERENCE A LOCATION ON THE SWITCHED BUS
                                                                        ;SHOULD TRAP SINCE SWITCH IS NOT CONNECTED
014220  104410                              HLT                         ;SWITCHED BUS ACTUALLY CONNECTED
014222  000401                              BR      CNT53A
014224  022626              RET53C: CMP     (SP)+,(SP)+
014226  012737  000006  000004  CNT53A: MOV     #6,@#4
014234  105077  164552          CONT53: CLRB    @BUSCSR             ;CLEAR REQUEST
014240  032777  001000  164544              BIT     #1000,@BUSCSR
014246  001374                              BNE     .-6
014250  052777  004000  164534              BIS     #4000,@BUSCSR       ;SET COM1- THE OTHER SIDE SHOULD SEE IT
014256  012737  014452  000024              MOV     #RET53F,@#24
014264  104016                              PMSG7                       ;PRINT MESSAGE: "POWER THE DEVICE
                                                                        ;BACK UP, AND THEN CLEAR SWITCH 0 IN THIS
                                                                        ;PROCESSOR'S SWITCH REGISTER."
014266  032777  000001  164542              BIT     #1,@SR              ;WAIT FOR OPERATOR TO CLEAR SWITCH REGISTER SWITCH 0
014274  001374                              BNE     .-6
014276  042777  004000  164506              BIC     #4000,@BUSCSR       ;OTHER SIDE SHOULD HAVE SEEN COM BIT SET BY NOW
014304  005777  164502                      TST     @BUSCSR             ;CHECK CSR AFTER POWER UP OF SWITCHED BUS
014310  001401                              BEQ     .+4                 ;DEVICE
014312  104410                              HLT                         ;CSR INCORRECT AFTER POWER UP OF SWITCHED
                                                                        ;BUS DEVICE - SHOULD HAVE BEEN CLEARED
014314  012777  000001  164470              MOV     #1,@BUSCSR          ;TRY TO CONNECT SWITCH
014322  000240                              NOP
014324  105777  164462                      TSTB    @BUSCSR             ;CHECK SWITCH CONNECTED BIT
014330  100401                              BMI     .+4                 ;BRANCH IF SET
014332  104410                              HLT                         ;SWITCH DIDN'T CONNECT AFTER BIT 0 WAS SET
014334  005077  164452                      CLR     @BUSCSR             ;INITIALIZE CSR
014340  012737  000026  000024              MOV     #26,@#24            ;RESTORE TRAP CATCHER
```

```
014346  005037  000026                  CLR     @#26
014352  032777  001000  164432          BIT     #1000,@BUSCSR
014360  001374                          BNE     .-6
014362  000470                          BR      TEST54
014364  012737  014414  000024  RET53D: MOV     #RET53E,@#24    ;SETUP POWER UP RETURN AFTER ILLEGAL POWER FAIL
014372  010667  164472                  MOV     SP,SPSAV
014376  017767  164410  164466          MOV     @BUSCSR,PFSAV   ;SAVE CSR CONTENTS IN CASE NEEDED
014404  000000                          HALT                    ;POWER DOWN HALT  AFTER SWITCH RECONNECTED WITH A
                                                                ;SWITCHED BUS DEVICE STILL POWERED DOWN

014406  016706  164456                  MOV     SPSAV,SP
014412  104410                          HLT                     ;NO POWER UP RESTART OCCURRED
014414  016706  164450          RET53E: MOV     SPSAV,SP        ;RESTORE STACK POINTER AFTER POWER UP
014420  022626                          CMP     (SP)+,(SP)+
014422  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER TO POWER FAIL VECTOR
014430  005037  000026                  CLR     @#26
014434  005027  000000                  CLR     #0              ;STALL SO THAT TTY OUTPUT WON'T BE GARBLED
014440  005367  177772                  DEC     .-2
014444  001375                          BNE     .-4
014446  104410                          HLT                     ;POWER FAIL TRAP OCCURRED WHEN THE SWITCH
                                                                ;WAS REQUESTED AFTER A SWITCHED BUS DEVICE
                                                                ;HAD BEEN POWERED DOWN

014450  000671                          BR      CONT53
014452  012737  014474  000024  RET53F: MOV     #RET53H,@#24    ;SETUP POWER UP AFTER ILLEGAL POWER DOWN
014460  010667  164404                  MOV     SP,SPSAV
014464  017767  164322  164400          MOV     @BUSCSR,PFSAV   ;SAVE CSR CONTENTS IN CASE NEEDED
014472  000000                          HALT                    ;POWER DOWN HALT- TRAP OCCURRED
                                                                ;WHEN THE SWITCH CONNECTED WHEN
                                                                ;REQUESTED AFTER A SWITCED BUS DEVICE
                                                                ;WAS POWERED DOWN AND BACK UP
014474  016706  164370          RET53H: MOV     SPSAV,SP        ;RESTORE STACK POINTER AFTER POWERUP
014500  022626                          CMP     (SP)+,(SP)+
014502  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER
014510  005037  000026                  CLR     @#26
014514  005027  000000                  CLR     #0              ;STALL SO THAT TTY OUTPUT WON'T BE GARBLED
014520  005367  177772                  DEC     .-2
014524  001375                          BNE     .-4
014526  104410                          HLT                     ;POWER FAIL TRAP OCCURRED WHEN SWITCH WAS
                                                                ;REQUESTED AFTER A SWITCHED BUS DEVICE WAS POWERED
                                                                ;DOWN AND BACK UP
014530  005077  164256                  CLR     @BUSCSR
014534  032777  001000  164250          BIT     #1000,@BUSCSR
014542  001374                          BNE     .-6


                                ;THEN CHECK IT WITH THE SWITCH CONTROLLED BY BUT NOT CONNECTED TO THIS
                                ;PROCESSOR
014544  104406                  TEST54: SCOPE
014546  005767  164332                  TST     DT11AF
014552  001002                          BNE     .+6
014554  104046                          PMSG19                  ;PRINT MESSAGE:"CHANGE SWITCH REGISTER OF THE
                                                                ;OTHER PROCESSOR. CLEAR IT
                                                                ;AND THEN SET SWITCH EIGHT TO A ONE.
014556  000000                          HALT                    ;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."
014560  012777  000002  164224          MOV     #2,@BUSCSR      ;REQUEST SWITCH
014566  012737  014632  000024          MOV     #RET54A,@#24    ;SETUP POWER FAIL RETURN
014574  017737  164234  000026          MOV     @PSR,@#26
```

```
014602  104014                          PMSG6                   ;PRINT MESSAGE: "POWER DOWN ONE DEVICE ON THE SWITCHED
                                                                ;BUS.  AND THEN SET SWITCH 0 IN THIS
                                                                ;PROCESSOR'S SWITCH REGISTER."
014604  032777  000001  164224          BIT     #1,@SR          ;WAIT FOR SWITCH REGISTER SWITCH 0 TO SET
014612  001774                          BEQ     .-6             ;SHOULD TRAP OUT DUE TO POWER FAIL
014614  104410                          HLT                     ;NO POWER FAIL TRAP ON POWERING DOWN A
                                                                ;SWITCHED BUS DEVICE WHEN THIS PROCESSOR
                                                                ;HAD THE SWITCH
014616  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER
014624  005037  000026                  CLR     @#26
014630  000474                          BR      CONT54
014632  012737  014662  000024  RET54A: MOV     #RET54B,@#24    ;SETUP POWER UP RETURN
014640  010667  164224                  MOV     SP,SPSAV        ;SAVE STACK POINTER
014644  017767  164142  164220          MOV     @#BUSCSR,PFSAV  ;SAVE CSR AT TIME OF POWER DOWN TRAP
014652  000000                          HALT                    ;NO POWER UP OCCURRED AFTER SWITCHED BUS
                                                                ;DEVICE WAS POWERED DOWN.  THE SWITCH SHOULD
                                                                ;HAVE GONE TO NEUTRAL AND ALLOWED THE CPU
                                                                ;TO POWER BACK UP.
014654  016706  164210                  MOV     SPSAV,SP
014660  104410                          HLT                     ;NO POWER UP RESTART OCCURRED
014662  016706  164202          RET54B: MOV     SPSAV,SP        ;RESTORE STACK POINTER
014666  022626                          CMP     (SP)+,(SP)+
014670  012737  015152  000024          MOV     #RET54D,@#24    ;SETUP NEW POWER FAIL VECTOR IN CASE
                                                                ;SWITCH CONNECTS WHEN REQUESTED
014676  005027  000000                  CLR     #0              ;STALL SO THAT TTY
014702  005367  177772                  DEC     .-2             ;OUTPUT WILL BE OK
014706  001375                          BNE     .-4
014710  032777  000001  164120          BIT     #1,@SR          ;WAIT FOR SWITCH REGISTER SWITCH 0 TO BE SET
014716  001774                          BEQ     .-6
014720  022767  060202  164144          CMP     #60202,PFSAV    ;CHECK SAVED CONTENTS OF CSR AT TIME OF
                                                                ;POWER DOWN TRAP
014726  001401                          BEQ     .+4
014730  104410                          HLT                     ;CSR INCORRECT WHEN THE POWER FAIL OCCURRED
014732  022777  040000  164052          CMP     #40000,@BUSCSR  ;CHECK CSR NOW - BIT 14 SHOULD BE SET
014740  001401                          BEQ     .+4
014742  104410                          HLT                     ;CSR INCORRECT - ONLY BIT 14 SHOULD BE SET
014744  012777  000001  164040          MOV     #1,@BUSCSR      ;REQUEST SWITCH - SHOULDN'T CONNECT SINCE
                                                                ;SB DEVICE IS POWERED DOWN
014752  005327  000000                  DEC     #0              ;STALL
014756  001375                          BNE     .-4
014760  022777  040001  164024          CMP     #40001,@BUSCSR  ;CK CSR
014766  001401                          BEQ     .+4
014770  104410                          HLT                     ;CSR INCORRECT - ONLY REQUEST AND BIT 14
                                                                ;SHOULD BE SET
014772  012737  015012  000004          MOV     #RET54C,@#4     ;SETUP ADDRESS TIMEOUT RETURN
015000  016777  164052  164046          MOV     RWBITS,@DVADRS  ;REFERENCE A LOCATION ON THE SWITCHED BUS
                                                                ;SHOULD TRAP SINCE SWITCH IS NOT CONNECTED
015006  104410                          HLT                     ;SWITCHED BUS ACTUALLY CONNECTED
015010  000401                          BR      CNT54A
015012  022626          RET54C: CMP     (SP)+,(SP)+
015014  012737  000006  000004  CNT54A: MOV     #6,@#4
015022  105077  163764          CONT54: CLRB    @BUSCSR         ;CLEAR REQUEST
015026  032777  001000  163756          BIT     #1000,@BUSCSR
015034  001374                          BNE     .-6
015036  052777  004000  163746          BIS     #4000,@BUSCSR   ;SET COM1- THE OTHER SIDE SHOULD SEE IT
015044  012737  015240  000024          MOV     #RET54F,@#24
```

```
015052  104016                          PMSG7                   ;PRINT MESSAGE: "POWER THE DEVICE
                                                                ;BACK UP, AND THEN CLEAR SWITCH 0 IN THIS
                                                                ;PROCESSOR'S SWITCH REGISTER."
015054  032777  000001  163754          BIT     #1,@SR          ;WAIT FOR OPERATOR TO CLEAR SWITCH REGISTER SWITCH 0
015062  001374                          BNE     .-6
015064  042777  004000  163720          BIC     #4000,@BUSCSR   ;OTHER SIDE SHOULD HAVE SEEN COM BIT SET BY NOW
015072  005777  163714                  TST     @BUSCSR         ;CHECK CSR AFTER POWER UP OF SWITCHED BUS
015076  001401                          BEQ     .+4             ;DEVICE
015100  104410                          HLT                     ;CSR INCORRECT AFTER POWER UP OF SWITCHED
                                                                ;BUS DEVICE - SHOULD HAVE BEEN CLEARED
015102  012777  000001  163702          MOV     #1,@BUSCSR      ;TRY TO CONNECT SWITCH
015110  000240                          NOP
015112  105777  163674                  TSTB    @BUSCSR         ;CHECK SWITCH CONNECTED BIT
015116  100401                          BMI     .+4             ;BRANCH IF SET
015120  104410                          HLT                     ;SWITCH DIDN'T CONNECT AFTER BIT 0 WAS SET
015122  005077  163664                  CLR     @BUSCSR         ;INITIALIZE CSR
015126  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER
015134  005037  000026                  CLR     @#26
015140  032777  001000  163644          BIT     #1000,@BUSCSR
015146  001374                          BNE     .-6
015150  000470                          BR      TEST55
015152  012737  015202  000024  RET54D: MOV     #RET54E,@#24    ;SETUP POWER UP RETURN AFTER ILLEGAL POWER FAIL
015160  010667  163704                  MOV     SP,SPSAV
015164  017767  163622  163700          MOV     @BUSCSR,PFSAV   ;SAVE CSR CONTENTS IN CASE NEEDED
015172  000000                          HALT                    ;POWER DOWN HALT  AFTER SWITCH RECONNECTED WITH A
                                                                ;SWITCHED BUS DEVICE STILL POWERED DOWN
015174  016706  163670                  MOV     SPSAV,SP
015200  104410                          HLT                     ;NO POWER UP RESTART OCCURRED
015202  016706  163662          RET54E: MOV     SPSAV,SP        ;RESTORE STACK POINTER AFTER POWER UP
015206  022626                          CMP     (SP)+,(SP)+
015210  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER TO POWER FAIL VECTOR
015216  005037  000026                  CLR     @#26
015222  005027  000000                  CLR     #0              ;STALL SO THAT TTY OUTPUT WON'T BE GARBLED
015226  005367  177772                  DEC     .-2
015232  001375                          BNE     .-4
015234  104410                          HLT
                                                                ;POWER FAIL TRAP OCCURRED WHEN THE SWITCH
                                                                ;WAS REQUESTED AFTER A SWITCHED BUS DEVICE
                                                                ;HAD BEEN POWERED DOWN
015236  000671                          BR      CONT54
015240  012737  015262  000024  RET54F: MOV     #RET54H,@#24    ;SETUP POWER UP AFTER ILLEGAL POWER DOWN
015246  010667  163616                  MOV     SP,SPSAV
015252  017767  163534  163612          MOV     @BUSCSR,PFSAV   ;SAVE CSR CONTENTS IN CASE NEEDED
015260  000000                          HALT                    ;POWER DOWN HALT- TRAP OCCURRED
                                                                ;WHEN THE SWITCH CONNECTED WHEN
                                                                ;REQUESTED AFTER A SWITCED BUS DEVICE
                                                                ;WAS POWERED DOWN AND BACK UP
015262  016706  163602          RET54H: MOV     SPSAV,SP        ;RESTORE STACK POINTER AFTER POWERUP
015266  022626                          CMP     (SP)+,(SP)+
015270  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER
015276  005037  000026                  CLR     @#26
015302  005027  000000                  CLR     #0              ;STALL SO THAT TTY OUTPUT WON'T BE GARBLED
015306  005367  177772                  DEC     .-2
015312  001375                          BNE     .-4
015314  104410                          HLT
                                                                ;POWER FAIL TRAP OCCURRED WHEN SWITCH WAS
                                                                ;REQUESTED AFTER A SWITCHED BUS DEVICE WAS POWERED
                                                                ;DOWN AND BACK UP
```

```
015316  005077  163470                  CLR     @BUSCSR
015322  032777  001000  163462          BIT     #1000,@BUSCSR
015330  001374                          BNE     .-6

                                ;FINALLY, CHECK IT WITH THE SWITCH IN NEUTRAL
                                ;SHOW THAT WHEN THE SWITCH IS IN NEUTRAL, BIT 14 GETS SET WHEN A DEVICE
                                ;IS POWERED DOWN ON THE SWITCHED BUS, AND BIT 14 GETS CLEARED WHEN IT IS
                                ;POWERED BACK UP
                                ;SHOW THAT NO POWER FAIL TRAP OCCURS
                                ;ALSO SHOW THAT BIT 14 OF THE CSR IS READ ONLY
015332  104406                  TEST55: SCOPE
015334  005077  163452                  CLR     @BUSCSR         ;PUT SWITCH IN NEUTRAL
015340  012737  015560  000024          MOV     #RET55,@#24     ;SETUP POWER FAIL RETURN IN CASE
015346  017737  163462  000026          MOV     @PSR,@#26
015354  005767  163524                  TST     DT11AF
015360  001007                          BNE     CNT55
015362  105767  163464                  TSTB    SBINH           ;SR 9 SET?
015366  001402                          BEQ     .+6             ;IF NOT SET, ALLOW FULL TESTING
015370  104062                          PMSG25                  ;REQUEST OPERATOR TO CLEAR SWITCH
015372  000402                          BR      .+6             ;REGISTER OF OTHER PROCESSOR
015374  104046                          PMSG19                  ;REQUEST OPERATOR TO CLEAR SWITCH
015376  000000                          HALT                    ;REGISTER OF OTHER PROCESSOR, AND
                                                                ;THEN SET SWITCH 8
015400  104014                  CNT55:  PMSG6                   ;REQUEST OPERATOR TO POWER DOWN ONE DEVICE ON THE
                                                                ;SWITCHED BUS, AND THEN SET SWITCH
                                                                ;ZERO IN THIS PROCESSOR'S SWITCH REGISTER
015402  032777  040000  163402  LOP55A: BIT     #40000,@BUSCSR  ;WAIT FOR BIT 14 TO SET OR FOR
015410  001006                          BNE     LOP55B          ;SWITCH REGISTER SWITCH 0 TO
015412  032777  000001  163416          BIT     #1,@SR          ;BE SET
015420  001770                          BEQ     LOP55A
015422  104410                          HLT

                                ;CSR INCORRECT WHEN SWITCHED BUS
                                ;DEVICE WAS POWERED DOWN - AC LO
                                ;NEVER SET

015424  000404                          BR      CNT55A
015426  032777  000001  163402  LOP55B: BIT     #1,@SR          ;WAIT FOR SWITCH REGISTER SWITCH 0
015434  001774                          BEQ     .-6             ;TO BE SET
015436  032777  040000  163346  CNT55A: BIT     #40000,@BUSCSR  ;IF BIT 14 IS SET, SHOW THAT IT IS RO0
015444  001413                          BEQ     CNT55B
015446  105767  163400                  TSTB    SBINH           ;SKIP IF ONLY CHECKING THAT AC LO CAN BE SET
015452  001010                          BNE     CNT55B          ;SINCE IT MAY GO CLEAR WHEN POWER
                                                                ;SUPPLY LETS IT FLOAT
015454  042777  040000  163330          BIC     #40000,@BUSCSR  ;BIC TO CSR SHOULDN'T AFFECT BIT 14
015462  032777  040000  163322          BIT     #40000,@BUSCSR  ;CHECK BIT 14
015470  001001                          BNE     .+4
015472  104410                          HLT                     ;BIT 14 CLEARED VIA A BIC
015474  052777  004000  163310  CNT55B: BIS     #4000,@BUSCSR   ;SET COMI - SHOULD BE SEEN BY OTHER SIDE
015502  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER
015510  005037  000026                  CLR     @#26
015514  104016                          PMSG7                   ;REQUEST OPERATOR TO POWER THE DEVICE BACK UP AND
                                                                ;THEN CLEAR SWITCH ZERO IN THIS
                                                                ;PROCESSOR'S SWITCH REGISTER
015516  032777  000001  163312          BIT     #1,@SR          ;WAIT FOR SWITCH ZERO TO BE
015524  001374                          BNE     .-6             ;CLEARED
015526  042777  004000  163256          BIC     #4000,@BUSCSR   ;CLEAR COMI- SHOULD HAVE BEEN SEEN BY NOW
015534  005777  163252                  TST     @BUSCSR         ;CK CSR
015540  001401                          BEQ     .+4
```

```
015542  104410                          HLT                     ;CSR INCORRECT AFTER SB DEVICE
                                                                ;POWERED BACK UP
015544  005767  163334                  TST     DT1IAF
015550  001027                          BNE     DONE
015552  104012                          PMSG5                   ;REQUEST OPERATOR TO CLEAR SWITCH REGISTER
015554  000000                          HALT                    ;OF THE OTHER CPU
015556  000424                          BR      DONE            ;SKIP ERROR SECTION
015560  012737  015602  000024  RET55:  MOV     #RET55A,@#24
015566  010667  163276                  MOV     SP,SPSAV
015572  000000                          HALT                    ;POWER FAIL TRAP OCCURRED ON POWERING
                                                                ;DOWN A SWITCHED BUS DEVICE WITH
                                                                ;THE SWITCH IN NEUTRAL TO
                                                                ;RECOVER, PRESS CONTINUE
015574  016706  163270                  MOV     SPSAV,SP
015600  104410                          HLT                     ;NO POWER UP RESTART OCCURRED
015602  016706  163262          RET55A: MOV     SPSAV,SP
015606  022626                          CMP     (SP)+,(SP)+
015610  005027  000000                  CLR     #0              ;STALL SO THAT TTY
015614  005367  177772                  DEC     .-2             ;OUTPUT WON'T BE
015620  001375                          BNE     .-4             ;GARBLED
015622  104410                          HLT                     ;POWER FAIL TRAP OCCURRED
                                                                ;WHEN A DEVICE ON THE
                                                                ;SWITCHED BUS WAS POWERED DOWN
                                                                ;WITH THE SWITCH IN NEUTRAL
015624  000167  177644                  JMP     CNT55B
015630  104406          DONE:   SCOPE
015632  005167  163240                  COM     INITF           ;TOGGLE FLAG THAT INDICATES WHETHER
                                                                ;OR NOT THE TEST IS BEING RUN
                                                                ;IN THE "INHIBIT INIT" STATE
015636  100012                          BPL     INITPS          ;BRANCH IF THIS PASS WAS RUN WITH "INIT-INHIBIT INIT"
                                                                ;IN THE "INHIBIT INIT" POSITION
015640  104030                          PMSG12                  ;REQUEST THAT "INIT-INHIBIT INIT"
                                                                ;SWITCH BE PUT IN THE "INHIBIT
015642  000000                          HALT                    ;INIT" POSITION
015644  005077  163142                  CLR     @BUSCSR
015650  032777  001000  163134          BIT     #1000,@BUSCSR
015656  001374                          BNE     .-6
015660  000167  000164                  JMP     TRCK            ;RUN A PASS WITH THE SWITCH
                                                                ;IN "INHIBIT INIT" STATE AND T-BIT SET
015664  005767  163214          INITPS: TST     DT1IAF
015670  001013                          BNE     INITPB
015672  104110                          PMSG36                  ;REQUEST OPERATOR TO SET SR SWITCH
015674  000000                          HALT                    ;12 OF THE OTHER CPU
015676  032777  010000  163106          BIT     #10000,@BUSCSR  ;CHECK CSR BIT 12- IF SET, ERRORS OCCURRED
                                                                ;ON THE OTHER SIDE
015704  001403                          BEQ     .+10
015706  012767  177777  004016          MOV     #-1,ERR         ;SET FLAG INDICATING ERRORS OCCURRED ON
                                                                ;THE OTHER SIDE
015714  104012                          PMSG5                   ;REQUEST OPERATOR TO CLEAR SR OF
015716  000000                          HALT                    ;THE OTHER CPU
015720  104076          INITPB: PMSG31                          ;PRINT MESSAGE: "END OF PASS"
015722  005767  004004                  TST     ERR             ;DID ANY ERRORS OCCUR?
015726  100402                          BMI     .+6             ;YES - BRANCH
015730  104100                          PMSG32                  ;NO - PRINT MESSAGE "NO ERRORS OCCURRED"
015732  000401                          BR      .+4
015734  104102                          PMSG33                  ;PRINT MESSAGE "ERRORS OCCURRED"
```

```
015736  005767  163140                  TST     NOPF            ;WAS POWER FAIL TESTED?
015742  100402                          BMI     .+6             ;NO - BRANCH
015744  104104                          PMSG34                  ;YES - PRINT MESSAGE "POWER FAIL WAS TESTED"
015746  000406                          BR      INITPA
015750  104106                          PMSG35                  ;PRINT MESSAGE "POWER FAIL WAS NOT TESTED"
015752  004767  004214                  JSR     %7,CRLF
015756  004767  004210                  JSR     %7,CRLF
015762  000413                          BR      INITP1
015764  005767  163062          INITPA: TST     SBINH           ;SWITCHED BUS POWER FAIL FULLY TESTED?
015770  001002                          BNE     .+6             ;NO, BRANCH
015772  104114                          PMSG38                  ;"SWITCHED BUS POWER FAIL WAS FULLY TESTED"
015774  000406                          BR      LOGICAL
015776  105767  163051                  TSTB    SBINH+1         ;SWITCHED BUS POWER FAIL TESTING INHIBITED COMPLETELY?
016002  001402                          BEQ     .+6             ;NO, BRANCH
016004  104116                          PMSG39                  ;"SWITCHED BUS POWER FAIL WAS NOT TESTED"
016006  000401                          BR      LOGICAL
016010  104120                          PMSG40                  ;"SWITCHED BUS POWER FAIL WAS PARTIALLY TESTED"
016012                          LOGICAL:
016012  013701  000042          INITP1: MOV     @#42,R1         ;HOOK TO RETURN TO MONITOR
016016  001405                          BEQ     INITP2
016020  000005                          RESET
016022  004711                          JSR     %7,@R1
016024  000240                          NOP
016026  000240                          NOP
016030  000240                          NOP
016032  104032          INITP2: PMSG13                  ;REQUEST THAT "INIT-INHIBIT INIT" SWITCH  BE PUT BACK
                                                        ;IN THE "INIT" POSITION
016034  000000                          HALT
016036  012767  177777  163030          MOV     #-1,SHORTF      ;SET FLAG TO INDICATE THAT ALL REMAINING PASSES
                                                        ;SHOULD SKIP THE PORTION REQUIRING OPERATOR INTERVENTION

016044  004767  004104          END:    JSR     %7,BELL         ;RING BELL TO SIGNIFY END OF FULL
                                                        ;TEST PASS
016050  005167  163024          TRCK:   COM     TFLAG           ;TOGGLE TRACE TRAP FLAG
016054  100007                          BPL     NOTRC           ;IF NOT SET, RUN PASS WITHOUT TRACE TRAPPING
016056  032777  010000  162752          BIT     #10000,@SR      ;IF SET, CHECK SWITCH REGISTER SWITCH 12
016064  100403                          BMI     NOTRC           ;IF SET, RUN PASS WITHOUT TRACE TRAPPING
016066  012746  000020                  MOV     #20,-(SP)       ;OTHERWISE, SET TRACE BIT
016072  000401                          BR      .+4
016074  005046                  NOTRC:  CLR     -(SP)           ;CLEAR TRACE BIT ON STACK
016076  012746  001366                  MOV     #$$EGIN,-(SP)
016102  105777  162720                  TSTB    @TCSR           ;WAIT FOR TTY TO FINISH SO THAT RESET
016106  100375                          BPL     .-4             ;WON'T CLOBBER THE BELL
016110  000002                          RTI

                                ;ROUTINES TO BE RUN ON OTHER PROCESSOR WHEN OPERATOR INTERVENTION
                                ;SECTION IS RUN
016112  104066                  SAMONX: PMSG27                  ;PRINT MESSAGE: "INPUT THE SAME INFORMATION AS
                                                        ;INITIALLY REQUESTED ON THE OTHER SIDE"
016114  004767  002754                  JSR     %7,INFORM       ;INPUT INFORMATION ABOUT A SWITCHED BUS LOCATION
016120  005067  003606                  CLR     ERR
016124  005327  000000          SAMEX:  DEC     #0              ;ENTER HERE WHEN LEAVING SUBROUTINES
016130  001375                          BNE     .-4             ;STALL TO AVOID SWITCH REGISTER PROBLEMS
016132  005077  162654          SAMON:  CLR     @BUSCSR         ;CLEAR THE CSR OF THE DTII
016136  032777  001000  162646          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO CLEAR
016144  001374                          BNE     .-6
```

```
016146  005067  002720                  CLR     FLAGS
016152  005777  162660                  TST     @SR             ;ANY SR SWITCHES SET?
016156  001775                          BEQ     .-4             ;NO, WAIT

                                ;SET BIT 0 OF THE DT11 CSR IF SWITCH REGISTER SWITCH 0 IS SET
016160  032777  000001  162650  SRM1:   BIT     #1,@SR          ;CHECK SWITCH REGISTER SWITCH ZERO
016166  001414                          BEQ     SRM2            ;GO TO NEXT IF NOT SET
016170  005327  000000                  DEC     #0              ;STALL TO IGNORE SWITCH REGISTER BOUNCE
016174  001375                          BNE     .-4
016176  012777  000001  162606          MOV     #1,@BUSCSR      ;REQUEST BUS SWITCH BY SETTING BIT 0 OF THE CSR
016204  032777  000001  162624          BIT     #1,@SR
016212  001374                          BNE     .-6
016214  000167  177704                  JMP     SRMEX

                                ;SET BIT 1 OF THE DT11 CSR IF SWITCH REGISTER SWITCH 1 IS SET
016220  032777  000002  162610  SRM2:   BIT     #2,@SR          ;EXECUTE THIS SECTION IF SWITCH 1 IS SET
016226  001414                          BEQ     SRM3
016230  005327  000000                  DEC     #0              ;STALL TO AVOID SWITCH REGISTER BOUNCE
016234  001375                          BNE     .-4
016236  012777  000002  162546          MOV     #2,@BUSCSR      ;REQUEST BUS SWITCH BY SETTING BIT 1 OF THE CSR
016244  032777  000002  162564          BIT     #2,@SR
016252  001374                          BNE     .-6
016254  000167  177644                  JMP     SRMEX

                                ;SET COMMUNICATION BIT OF THE CSR IF SWITCH REGISTER SWITCH 2 IS SET
016260  032777  000004  162550  SRM3:   BIT     #4,@SR          ;EXECUTE THIS SECTION IF SWITCH 2 IS SET
016266  001414                          BEQ     SRM4
016270  005327  000000                  DEC     #0              ;STALL TO IGNORE SWITCH REGISTER BOUNCE
016274  001375                          BNE     .-4
016276  052777  004000  162506          BIS     #4000,@BUSCSR   ;SET COMMUNICATION BIT (CSR BIT 11)
016304  032777  000004  162524          BIT     #4,@SR
016312  001374                          BNE     .-6
016314  000167  177604                  JMP     SRMEX

                                ;IF SWITCH REGISTER SWITCH 3 IS SET, EXECUTE THIS ROUTINE
                                ;CK PROCESSOR POWER FAIL IF OTHER SIDE HAS THE SWITCH
                                ;OR IF THE SWITCH IS IN NEUTRAL
016320  032777  000010  162510  SRM4:   BIT     #10,@SR         ;EXECUTE THIS SECTION IF SWITCH 3 IS SET
016326  001502                          BEQ     SRM5
016330  005327  000000                  DEC     #0              ;STALL TO IGNORE SWITCH REGISTER BOUNCE
016334  001375                          BNE     .-4
016336  012777  002400  162446          MOV     #2400,@BUSCSR   ;SET BOTH INTERRUPT ENABLES IN CASE
016344  012737  016344  000024          MOV     #PFIHH,@#24     ;SETUP POWER FAIL RETURN IN CASE
016352  005037  000026                  CLR     @#26
016356  032777  040000  162426  SRM4A:  BIT     #40000,@BUSCSR  ;CHECK BIT 14-SHOULDN'T SET
016364  001401                          BEQ     .+4
016366  104410                          HLT                     ;BIT 14 IN CSR SET DUE TO POWER
                                                                ;FAIL ON OTHER PROCESSOR BUS
016370  032777  000010  162440          BIT     #10,@SR         ;CHECK SWITCH REGISTER
016376  001367                          BNE     SRM4A           ;IF SWITCH IS DOWN, BUS SWITCH
016400  032777  020000  162404          BIT     #20000,@BUSCSR  ;SHOULD HAVE GONE TO NEUTRAL
016406  001401                          BEQ     .+4
016410  104410                          HLT                     ;NON-NEUTRAL BIT STILL SET AFTER
                                                                ;POWER FAIL ON OTHER BUS SHOULD
                                                                ;HAVE DISCONNECTED THE BUS SWITCH
016412  012737  000026  000024          MOV     #26,@#24
```

```
016420  000167  177500                  JMP     SPMEX
016424  012737  016470  000024  RETMM4A: MOV     #RETMM4B,@#24   ;SETUP POWER UP RETURN
016432  010667  162432                  MOV     SP,SPSAV        ;SAVE STACK POINTER
016436  000000                          HALT                    ;POWER DOWN HALT (NO POWER FAIL
016440  016706  162424                  MOV     SPSAV,SP        ;SHOULD HAVE OCCURRED)
016444  104410                          HLT                     ;POWER FAIL TRAP (DOWN ONLY)
                                                                ;OCCURRED
016446  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER
016454  032777  000010  162364          BIT     #10,@SR
016462  001374                          BNE     .-6
016464  000167  177434                  JMP     SRMEX
016470  016706  162274          RETMM4B: MOV     SPSAV,SP        ;RESTORE STACK POINTER
016474  005027  000000                  CLR     #0              ;STALL SO THAT TTY OUTPUT WON'T
016500  005367  177772                  DEC     .-2             ;BE GARBLED
016504  001375                          BNE     .-4
016506  104410                          HLT                     ;POWER FAIL TRAP OCCURRED - CHECK
016510  012737  000026  000024          MOV     #26,@#24        ;STACK TO SEE WHERE IT OCCURRED
016516  032777  000010  162312          BIT     #10,@SR
016524  001374                          BNE     .-6
016526  022626                          CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
016530  000167  177370                  JMP     SRMEX

                                ;IF SWITCH REGISTER SWITCH 4 IS SET
                                ;CHECK PROCESSOR POWER FAIL WHEN THIS SIDE HAS SWITCH CONTROLLED BUT NOT
                                ;CONNECTED, AND OTHER CPU IS POWERED DOWN
016534  032777  000020  162274  SRM5:   BIT     #20,@SR         ;EXECUTE THIS SECTION IF SW 4 IS SET
016542  001512                          BEQ     SRM6
016544  005327  000000                  DEC     #0                      ;STALL TO IGNORE SWITCH REGISTER BOUNCE
016550  001375                          BNE     .-4
016552  012737  016660  000024          MOV     #RETM5A,@#24
016560  005037  000026                  CLR     @#26
016564  012777  000002  162220          MOV     #2,@BUSCSR      ;REQUEST SWITCH TO GO TO CONTROLLED
016572  105777  162214                  TSTB    @BUSCSR         ;BUT NOT CONNECTED POSITION
016576  100375                          BPL     .-4             ;WAIT FOR "CONNECTED" BIT TO SET
016600  052777  002400  162204          BIS     #2400,@BUSCSR   ;ONCE SWITCH IS IN POSITION 2 (4)
                                                                ;SET BOTH INTERRUPT ENABLES
016606  022777  022602  162176  SRM5A:  CMP     #22602,@BUSCSR  ;CHECK CSR-POWER FAIL ON THE
016614  001410                          BEQ     SRM5B           ;OTHER PROCESSOR BUS SHOULDN'T AFFECT IT
016616  032767  000020  002246          BIT     #20,FLAGS       ;PRINT ERROR ONLY ONCE
016624  001004                          BNE     SRM5B
016626  052767  000020  002236          BIS     #20,FLAGS
016634  104410                          HLT                     ;CSR INCORRECT DURING POWER FAIL
                                                                ;TEST
016636  032777  000020  162172  SRM5B:  BIT     #20,@SR         ;CONTINUE CHECKING UNTIL SWITCH
016644  001360                          BNE     SRM5A           ;REGISTER IS CLEARED
016646  012737  000026  000024          MOV     #26,@#24
016654  000167  177244                  JMP     SRMEX
016660  012737  016724  000024  RETM5A: MOV     #RETM5B,@#24    ;SETUP POWER UP RETURN
016666  010667  162176                  MOV     SP,SPSAV        ;SAVE STACK POINTER
016672  000000                          HALT                    ;POWER DOWN HALT (NO POWER FAIL
016674  016706  162170                  MOV     SPSAV,SP        ;SHOULD HAVE OCCURRED)
016700  104410                          HLT                     ;POWER FAIL TRAP (DOWN ONLY)
                                                                ;OCCURRED
016702  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER
016710  032777  000020  162120          BIT     #20,@SR
016716  001374                          BNE     .-6
```

```
016720  000167  177200                  JMP     SRMEX
016724  016706  162140          RETMSB: MOV     SPSAV,SP        ;RESTORE STACK POINTER
016730  005027  000000                  CLR     #0              ;STALL SO THAT TTY OUTPUT WON'T
016734  005367  177772                  DEC     .-2             ;BE GARBLED
016740  001375                          BNE     .-4
016742  104410                          HLT                     ;POWER FAIL TRAP OCCURRED - CHECK
016744  012737  000026  000024          MOV     #26,@#24        ;STACK TO SEE WHERE IT OCCURRED
016752  032777  000020  162056          BIT     #20,@SR
016760  001374                          BNE     .-6
016762  022626                          CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
016764  000167  177134                  JMP     SRMEX

                                ;IF SWITCH REGISTER SWITCH 5 IS SET
                                ;CHECK PROCESSOR POWER FAIL WHEN THIS SIDE HAS THE SWITCH CONNECTED
                                ;AND THE OTHER CPU IS POWERED DOWN
016770  032777  000040  162040  SRM6:   BIT     #40,@SR         ;EXECUTE THIS SECTION IF SW6 IS SET
016776  001512                          BEQ     SRM7
017000  005327  000000                  DEC     #0              ;STALL TO IGNORE SWITCH REGISTER BOUNCE
017004  001375                          BNE     .-4
017006  012737  017114  000024          MOV     #RETM6A,@#24
017014  005037  000026                  CLR     @#26
017020  012777  000001  161764          MOV     #1,@#BUSCSR     ;REQUEST SWITCH
017026  105777  161760                  TSTB    @#BUSCSR        ;WAIT FOR SWITCH TO CONNECT
017032  100375                          BPL     .-4
017034  052777  002400  161750          BIS     #2400,@#BUSCSR  ;SET BOTH INTERRUPT ENABLES
017042  022777  022601  161742  SRM6A:  CMP     #22601,@#BUSCSR ;CHECK CSR-POWER FAIL ON OTHER
017050  001410                          BEQ     SRM6B           ;PROCESSOR BUS SHOULDN'T AFFECT IT
017052  032767  000040  002012          BIT     #40,FLAGS       ;PRINT ERROR ONLY ONCE
017060  001004                          BNE     SRM6B
017062  052767  000040  002002          BIS     #40,FLAGS
017070  104410                          HLT
                                ;CSR INCORRECT DURING TEST OF POWER FAIL
                                ;ON THE OTHER PROCESSOR BUS
017072  032777  000040  161736  SRM6B:  BIT     #40,@SR         ;CONTINUE CHECKING UNTIL SWITCH
017100  001360                          BNE     SRM6A           ;REGISTER IS CLEARED
017102  012737  000026  000024          MOV     #26,@#24
017110  000167  177010                  JMP     SRMEX
017114  012737  017160  000024  RETM6A: MOV     #RETM6B,@#24    ;SETUP POWER UP RETURN
017122  010667  161742                  MOV     SP,SPSAV        ;SAVE STACK POINTER
017126  000000                          HALT                    ;POWER DOWN HALT (NO POWER FAIL
017130  016706  161734                  MOV     SPSAV,SP        ;SHOULD HAVE OCCURRED)
017134  104410                          HLT                     ;POWER FAIL TRAP (DOWN ONLY)
                                                                ;OCCURRED
017136  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER
017144  032777  000040  161664          BIT     #40,@SR
017152  001374                          BNE     .-6
017154  000167  176744                  JMP     SRMEX
017160  016706  161704          RETM6B: MOV     SPSAV,SP        ;RESTORE STACK POINTER
017164  005027  000000                  CLR     #0              ;STALL SO THAT TTY OUTPUT WON'T
017170  005367  177772                  DEC     .-2             ;BE GARBLED
017174  001375                          BNE     .-4
017176  104410                          HLT                     ;POWER FAIL TRAP OCCURRED - CHECK
017200  012737  000026  000024          MOV     #26,@#24        ;STACK TO SEE WHERE IT OCCURRED
017206  032777  000040  161622          BIT     #40,@SR
017214  001374                          BNE     .-6
017216  022626                          CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
017220  000167  176700                  JMP     SRMEX
```

```
                                        ;IF SWITCH REGISTER SWITCH 6 IS SET
                                        ;SHOW THAT WHEN OTHER CPU IS POWERED DOWN AND HAD BUS SWITCH,
                                        ;THIS SIDE CAN GET THE SWITCH
017224  032777  000100  161604  SRM7:   BIT     #100,@SR        ;EXECUTE THIS SECTION IF SW6 IS SET
017232  001516                        BEQ     SRM8
017234  005327  000000                DEC     #0              ;STALL TO IGNORE SWITCH REGISTER BOUNCE
017240  001375                        BNE     .-4
017242  012737  017360  000024        MOV     #RETM7A,@#24
017250  005037  000026                CLR     @#26
017254  032777  020000  161530        BIT     #20000,@BUSCSR  ;WAIT FOR NON NEUTRAL (BIT 13) TO SET
017262  001774                        BEQ     .-6             ;INDICATING OTHER PROCESSOR HAS THE SWITCH
017264  012777  000001  161520        MOV     #1,@BUSCSR      ;REQUEST SWITCH-SHOULD CONNECT
017272  105777  161514        SRM7A:  TSTB    @BUSCSR         ;WHEN OTHER PROCESSOR IS POWERED
                                                              ;DOWN
017276  100412                        BMI     SRM7B           ;BRANCH IF NOW CONNECTED TO THIS SIDE
017300  032777  000100  161530        BIT     #100,@SR        ;CHECK SWITCH REGISTER
017306  001371                        BNE     SRM7A           ;LOOP IF NOT CLEARED
017310  104410                        HLT                     ;CONNECTED BIT NEVER SET, ALTHOUGH
                                                              ;SWITCH WAS REQUESTED AND OTHER
                                                              ;PROCESSOR WAS POWERED DOWN
017312  012737  000026  000024        MOV     #2F,@#24
017320  000167  176600                JMP     SREX
017324  032777  040000  161460  SRM7B:  BIT #40000,@BUSCSR      ;CHECK BIT 14  - SHOULDN'T
017332  001401                        BEQ     .+4             ;BE SET
017334  104410                        HLT                     ;BIT 14 SET IN CSR AFTER
                                                              ;OTHER PROCESSOR WAS POWERED DOWN
017336  032777  000100  161472        BIT     #100,@SR        ;WAIT FOR OPERATOR TO CLEAR SWITCH REGISTER
017344  001374                        BNE     .-6             ;INDICATING END OF TEST
017346  012737  000026  000024        MOV     #26,@#24
017354  000167  176544                JMP     SREX
017360  012737  017424  000024  RETM7A: MOV    #RETM7B,@#24    ;SETUP POWER UP RETURN
017366  010667  161476                MOV     SP,SPSAV        ;SAVE STACK POINTER
017372  000000                        HALT                    ;POWER DOWN HALT (NO POWER FAIL
017374  016706  161470                MOV     SPSAV,SP        ;SHOULD HAVE OCCURRED)
017400  104410                        HLT                     ;POWER FAIL TRAP (DOWN ONLY)
                                                              ;OCCURRED
017402  012737  000026  000024        MOV     #26,@#24        ;RESTORE TRAP CATCHER
017410  032777  000100  161420        BIT     #100,@SR
017416  001374                        BNE     .-6
017420  000167  176500                JMP     SREX
017424  016706  161440  RETM7B:  MOV     SPSAV,SP        ;RESTORE STACK POINTER
017430  005027  000000                CLR     #0              ;STALL SO THAT TTY OUTPUT WON'T
017434  005367  177772                DEC     .-2             ;BE GARBLED
017440  001375                        BNE     .-4
017442  104410                        HLT                     ;POWER FAIL TRAP OCCURRED - CHECK
017444  012737  000026  000024        MOV     #26,@#24        ;STACK TO SEE WHERE IT OCCURRED
017452  032777  000100  161356        BIT     #100,@SR
017460  001374                        BNE     .-6
017462  022626                        CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
017464  000167  176434                JMP     SREX

                                        ;IF SWITCH REGISTER SWITCH 7 IS SET, EXECUTE THIS ROUTINE
                                        ;POWER FAIL TEST RUN WHEN THE SWITCH IS POWERED DOWN
017470  032777  000200  161340  SRM8:   BIT     #200,@SR        ;EXECUTE THIS SECTION IF SW7 IS SET
017476  001477                        BEQ     SRM9
```

```
017500  012737  017544  000024          MOV     #SRET8,@#24     ;SET UP POWER FAIL TRAP RETURN
017506  005037  000026                  CLR     @#26
017512  005327  000000                  DEC     #0              ;STALL TO IGNORE SWITCH REGISTER BOUNCE
017516  001375                          BNE     .-4
017520  032777  000200  161310          BIT     #200,@SR        ;WAIT FOR SWITCH REGISTER TO BE CLEARED
017526  001374                          BNE     .-6             ;POWER FAIL TRAP SHOULD OCCUR FIRST
017530  104410                          HLT                     ;NO POWER FAIL TRAP ON SWITCH POWERING DOWN OR UP
017532  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER IN POWER FAIL TRAP
017540  000167  176360                  JMP     SRMEX           ;LOCATION
017544  012737  017604  000024  SRET8:  MOV     #SRET8A,@#24    ;SET UP POWER UP RETURN
017552  017767  161234  161312          MOV     @BUSCSR,PFSAV   ;STORE CURRENT CSR CONTENTS
017560  010667  161304                  MOV     SP,SPSAV        ;SAVE STACK POINTER
017564  032767  040000  161300          BIT     #40000,PFSAV    ;CHECK FOR AC LO
017572  001767                          BEQ     SRET8+6         ;IF NOT SET, GO BACK TO REREAD CSR
017574  000000                          HALT                    ;POWER DOWN HALT
017576  016706  161266                  MOV     SPSAV,SP
017602  104410                          HLT                     ;NO POWER UP RESTART AFTER POWER DOWN
017604  016706  161260  SRET8A: MOV     SPSAV,SP        ;RESTORE STACK POINTER ON POWER UP
017610  022626                          CMP     (SP)+,(SP)+
017612  005027  000000                  CLR     #0              ;STALL SO THAT TTY OUTPUT WILL BE OK
017616  005367  177772                  DEC     .-2
017622  001375                          BNE     .-4
017624  042767  020000  161240          BIC     #20000,PFSAV    ;CLEAR NOT NEUTRAL BIT IN SAVED CSR CONTENTS
017632  022767  040000  161232          CMP     #40000,PFSAV    ;CHECK CONTENTS OF CSR SAVED WHEN
017640  001401                          BEQ     .+4             ;POWER DOWN OCCURRED (EXCEPT FOR NOT NEUTRAL)
017642  104410                          HLT                     ;CSR INCORRECT AT POWER DOWN - ONLY BIT 14
                                                                ;AND POSSIBLY 13 SHOULD HAVE BEEN SET - SEE
                                                                ;ACTUAL VALUE SAVED IN PFSAV (NOTE THAT
                                                                ;NOT NEUTRAL HAS BEEN CLEARED SINCE IT MAY
                                                                ;HAVE BEEN SET OR CLEAR DEPENDING ON THE
                                                                ;POSITION THE SWITCH WAS IN)
017644  005777  161142                  TST     @BUSCSR         ;CSR SHOULD BE CLEARED ON POWER UP
017650  001401                          BEQ     .+4
017652  104410                          HLT                     ;CSR NOT CLEAR (ZERO) AFTER SWITCH
                                                                ;POWERED DOWN AND BACK UP
017654  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER IN POWER FAIL
                                                                ;TRAP LOCATION
017662  032777  000200  161146          BIT     #200,@SR        ;WAIT FOR SWITCH 7 TO BE CLEARED
017670  001374                          BNE     .-6
017672  000167  176226                  JMP     SRMEX

                                ;IF SWITCH REGISTER SWITCH 8 IS SET, EXECUTE THIS ROUTINE
                                ;POWER FAIL TEST RUN WHEN A SWITCHED BUS DEVICE IS POWERED DOWN
017676  032777  000400  161132  SRM9:   BIT     #400,@SR        ;EXECUTE THIS SECTION IF SW8 IS SET
017704  001562                          BEQ     SRM10
017706  005327  000000                  DEC     #0              ;STALL TO IGNORE SWITCH REGISTER BOUNCE
017712  001375                          BNE     .-4
017714  012737  020142  000024          MOV     #RETM9A,@#24    ;SETUP POWER FAIL RETURN IN CASE
017722  005037  000026                  CLR     @#26
017726  032777  040000  161056          BIT     #40000,@BUSCSR  ;CK BIT 14 - SHOULDN'T BE SET YET
017734  001401                          BEQ     .+4
017736  104410                          HLT                     ;BIT 14 SET BEFORE POWER DOWN OCCURRED
017740  032777  040000  161044  SRM9A:  BIT     #40000,@BUSCSR  ;WAIT FOR 14 TO SET OR SWITCH REGISTER
                                                                ;TO BE CLEARED (NO POWER FAIL TRAP SHOULD OCCUR)
017746  001012                          BNE     SRM9B           ;IF AC LO IS SET, BRANCH OUT
017750  032777  000400  161060          BIT     #400,@SR
```

```
017756  001370                          BNE     SRM9A
017760  104410                          HLT
017762  012737  000026  000024          MOV     #26,@#24        ;BIT 14 NEVER SET DURING POWER
017770  000167  176130                  JMP     SRMEX           ;DOWN AND UP OF A SWITCHED BUS DEVICE
017774  032777  020000  161010  SRM9B:  BIT     #20000,@BUSCSR  ;WAIT FOR SWITCH TO DISCONNECT DUE TO
020002  001374                          BNE     .-6             ;DC LO
020004  005327  000000                  DEC     #0              ;STALL IN CASE DC LO WAS GENERATED BY CPU
020010  001375                          BNE     .-4             ;AND NOT YET ON SB
020012  012777  000001  160772          MOV     #1,@BUSCSR      ;REQUEST SWITCH AFTER SWITCHED BUS DEVICE HAS
                                                                ;BEEN POWERED DOWN-SHOULDN'T CONNECT
020020  005327  000000                  DEC     #0              ;STALL
020024  001375                          BNE     .-4
020026  105777  160760                  TSTB    @BUSCSR         ;CHECK CONNECTED BIT
020032  100001                          BPL     .+4
020034  104410                          HLT                     ;SWITCH CONNECTED TO THIS PROCESSOR
                                                                ;AFTER POWER DOWN OF SB DEVICE
020036  105077  160750                  CLRB    @BUSCSR         ;CLEAR REQUEST
020042  032777  001000  160742          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO COMPLETE
020050  001374                          BNE     .-6
020052  032777  010000  160732  SRM9C1: BIT     #10000,@BUSCSR  ;WAIT FOR THE OTHER SIDE TO SET COM1 BIT
020060  001005                          BNE     SRM9C           ;FALL THRU WHEN SET
020062  032777  000400  160746          BIT     #400,@SR        ;WAIT FOR OPERATOR TO CLEAR SWITCH REGISTER
020070  001370                          BNE     SRM9C1
020072  104410                          HLT                     ;OTHER SIDE SET COM1 BIT AFTER THE SWITCHED BUS
                                                                ;DEVICE WAS POWERED DOWN, BUT COM2 WAS NEVER SET ON
                                                                ;THIS SIDE
020074  032777  040000  160710  SRM9C:  BIT     #40000,@BUSCSR  ;WAIT FOR AC LO TO CLEAR WHEN DEVICE
020102  001406                          BEQ     SRM9D           ;ON SWITCHED BUS IS POWERED BACK UP
020104  032777  000400  160724          BIT     #400,@SR        ;IF NOT CLEAR CHECK SWITCH REGISTER
020112  001370                          BNE     SRM9C           ;LOOP IF OPERATOR HASN'T CLEARED IT YET
020114  104410                          HLT                     ;BIT 14 DIDN'T CLEAR WHEN THE
020116  000404                          BR      .+12            ;SWITCHED BUS DEVICE WAS POWERED
                                                                ;BACK UP
020120  032777  000400  160710  SRM9D:  BIT     #400,@SR
020126  001374                          BNE     .-6
020130  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER
020136  000167  175762                  JMP     SRMEX           ;RETURN TO SWITCH MONITOR
020142  012737  020206  000024  RETM9A: MOV     #RETM9B,@#24    ;SETUP POWER UP RETURN
020150  010667  160714                  MOV     SP,SPSAV        ;SAVE STACK POINTER
020154  000000                          HALT                    ;POWER DOWN HALT (NO POWER FAIL
020156  016706  160706                  MOV     SPSAV,SP        ;SHOULD HAVE OCCURRED)
020162  104410                          HLT                     ;POWER FAIL TRAP (DOWN ONLY)
                                                                ;OCCURRED
020164  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER
020172  032777  000400  160636          BIT     #400,@SR
020200  001374                          BNE     .-6
020202  000167  175716                  JMP     SRMEX
020206  016706  160656  RETM9B: MOV     SPSAV,SP        ;RESTORE STACK POINTER
020212  005027  000000                  CLR     #0              ;STALL SO THAT TTY OUTPUT WON'T
020216  005367  177772                  DEC     .-2             ;BE GARBLED
020222  001375                          BNE     .-4
020224  104410                          HLT                     ;POWER FAIL TRAP OCCURRED - CHECK
020226  012737  000026  000024          MOV     #26,@#24        ;STACK TO SEE WHERE IT OCCURRED
020234  032777  000400  160574          BIT     #400,@SR
020242  001374                          BNE     .-6
020244  022626                          CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
```

```
020246  000167  175652                  JMP     SRMEX

                                ;IF SWITCH REGISTER SWITCH 9 IS SET, EXECUTE THIS ROUTINE
                                ;POWER FAIL TEST RUN WHEN OTHER CPU IS POWERED DOWN
                                ;AND THE SWITCH WAS IN NEUTRAL
020252  032777  001000  160556  SRM10:  BIT     #1000,@SR       ;EXECUTE THIS SECTION IF SW9 IS SET
020260  001512                  BEQ     SRM11
020262  005327  000000                  DEC     #0              ;STALL TO IGNORE SWITCH REGISTER BOUNCE
020266  001375                  BNE     .-4
020270  012737  020376  000024          MOV     #RETM0A,@#24
020276  005037  000026                  CLR     @#26
020302  012777  000001  160502          MOV     #1,@BUSCSR      ;REQUEST SWITCH - SHOULD CONNECT IMMEDIATELY
020310  105777  160476                  TSTB    @BUSCSR         ;SINCE OTHER PROCESSOR HAS ALREADY BEEN
                                                                ;POWERED DOWN
020314  100412                  BMI     SRM10B
020316  104410                  HLT                             ;CONNECTED BIT NOT SET, ALTHOUGH
                                                                ;THE SWITCH WAS REQUESTED AND THE OTHER
                                                                ;PROCESSOR WAS POWERED DOWN
020320  012737  000026  000024          MOV     #26,@#24
020326  032777  001000  160502          BIT     #1000,@SR
020334  001374                  BNE     .-6
020336  000167  175562                  JMP     SRMEX
020342  032777  140000  160442  SRM10B: BIT     #140300,@BUSCSR ;CHECK BITS 14 AND 15 - SHOULDN'T
020350  001401                  BEQ     .+4                     ;BE SET
020352  104410                  HLT                             ;BIT 14 AND/OR 15 SET IN CSR AFTER
                                                                ;OTHER PROCESSOR WAS POWERED DOWN
020354  032777  001000  160454          BIT     #1000,@SR       ;WAIT FOR OPERATOR TO CLEAR SR
020362  001374                  BNE     .-6                     ;INDICATING END OF TEST
020364  012737  000026  000024          MOV     #26,@#24
020372  000167  175526                  JMP     SRMEX
020376  012737  020442  000024  RETM0A: MOV     #RETM0B,@#24    ;SETUP POWER UP RETURN
020404  010667  160460                  MOV     SP,SPSAV        ;SAVE STACK POINTER
020410  000000                  HALT                            ;POWER DOWN HALT (NO POWER FAIL
020412  016706  160452                  MOV     SPSAV,SP        ;SHOULD HAVE OCCURRED)
020416  104410                  HLT                             ;POWER FAIL TRAP (DOWN ONLY)
                                                                ;OCCURRED
020420  012737  000026  000024          MOV     #26,@#24        ;RESTORE TRAP CATCHER
020426  032777  001000  160432          BIT     #1000,@SR
020434  001374                  BNE     .-6
020436  000167  175462                  JMP     SRMEX
020442  016706  160422  RETM0B: MOV     SPSAV,SP        ;RESTORE STACK POINTER
020446  005027  000000                  CLR     #0              ;STALL SO THAT TTY OUTPUT WON'T
020452  005367  177772                  DEC     .-2             ;BE GARBLED
020456  001375                  BNE     .-4
020460  104410                  HLT                             ;POWER FAIL TRAP OCCURRED - CHECK
020462  012737  000026  000024          MOV     #26,@#24        ;STACK TO SEE WHERE IT OCCURRED
020470  032777  001000  160340          BIT     #1000,@SR
020476  001374                  BNE     .-6
020500  022626                  CMP     (SP)+,(SP)+     ;RESTORE STACK POINTER
020502  000167  175416                  JMP     SRMEX

                                ;IF SWITCH REGISTER SWITCH 10 IS SET, EXECUTE THIS ROUTINE
                                ;TEST THAT NO INIT OCCURS ON THE
                                ;SWITCHED BUS IF THIS PROCESSOR HAS THE SWITCH
                                ;IN THE CONTROLLED BUT NOT CONNECTED POSITION (2 OR 4)
                                ;AND BIT 9 IS SET IN THE CSR ON THE OTHER SIDE
```

```
020506  032777  002000  160322  SRM11:  BIT     #2000,@SR       ;EXECUTE THIS SECTION IF SW10 IS SET
020514  001455                          BEQ     SRM12
020516  005327  000000          SRM11A: DEC     #0              ;STALL TO IGNORE SWITCH REGISTER BOUNCE
020522  001375                          BNE     .-4
020524  012777  000001  160260          MOV     #1,@BUSCSR      ;REQUEST SWITCH
020532  105777  160254                  TSTB    @BUSCSR         ;WAIT FOR CONNECTED TO SET
020536  100375                          BPL     .-4
020540  016777  160316  160306          MOV     ANDBTS,@DVADRS  ;SET UP LOCATION ON SWITCHED BUS
020546  017701  160302                  MOV     @DVADRS,R1      ;READ BACK SAME TO VALIDATE
020552  046701  160306                  BIC     ANDCOM,R1       ;BEFORE EXECUTING TEST
020556  026701  160300                  CMP     ANDBTS,R1
020562  001401                          BEQ     .+4
020564  104410                          HLT                     ;LOCATION ON SWITCHED BUS DID NOT LOAD CORRECTLY
020566  012777  000002  160216          MOV     #2,@BUSCSR      ;PUT SWITCH IN CONTROLLED BUT
                                                                ;NOT CONNECTED POSITION
020574  005777  160236                  TST     @SR             ;WAIT FOR SWITCH REGISTER TO CLEAR
020600  001375                          BNE     .-4
020602  012777  000001  160202          MOV     #1,@BUSCSR      ;CONNECT THE SWITCH
020610  017701  160240                  MOV     @DVADRS,R1      ;READ CONTENTS OF LOCATION ON SWITCHED BUS
020614  046701  160244                  BIC     ANDCOM,R1       ;MASK OFF BITS NOT SET
020620  026701  160236                  CMP     ANDBTS,R1       ;CHECK BITS IN THE DEVICE REGISTER
020624  001401                          BEQ     .+4
020626  104410                          HLT                     ;BITS IN LOCATION ON SWITCHED BUS
                                                                ;INCORRECT AFTER BIT 9 WAS SET
020630  005077  160156                  CLR     @BUSCSR
020634  032777  001000  160150          BIT     #1000,@BUSCSR
020642  001374                          BNE     .-6
020644  000167  175254                  JMP     SRMEX           ;IN OTHER PROCESSOR'S CSR

                                ;IF SWITCH REGISTER SWITCH 11 IS SET, EXECUTE THIS ROUTINE
                                ;TEST THAT NO INIT OCCURS ON THE
                                ;SWITCHED BUS IF THIS PROCESSOR HAS THE SWITCH IN
                                ;THE CONNECTED POSITION (1 OR 5) AND BIT 9 IS
                                ;SET IN THE CSR ON THE OTHER SIDE
020650  032777  004000  160160  SRM12:  BIT     #4000,@SR       ;EXECUTE THIS SECTION IF SW11 IS SET
020656  001450                          BEQ     SRM13
020660  005327  000000                  DEC     #0              ;STALL TO IGNORE SWITCH REGISTER BOUNCE
020664  001375                          BNE     .-4
020666  012777  000001  160116          MOV     #1,@BUSCSR      ;REQUEST SWITCH
020674  105777  160112                  TSTB    @BUSCSR         ;WAIT FOR CONNECTED TO SET
020700  100375                          BPL     .-4
020702  016777  160154  160144          MOV     ANDBTS,@DVADRS  ;SET UP LOCATION ON SWITCHED BUS
020710  017701  160140                  MOV     @DVADRS,R1      ;CHECK LOCATION BEFORE TESTING
020714  046701  160144                  BIC     ANDCOM,R1
020720  026701  160136                  CMP     ANDBTS,R1
020724  001401                          BEQ     .+4
020726  104410                          HLT                     ;SWITCHED BUS LOCATION DIDN'T LOAD CORRECTLY
020730  032777  004000  160100          BIT     #4000,@SR       ;WAIT FOR SWITCH REGISTER TO CLEAR
020736  001374                          BNE     .-6
020740  017701  160110                  MOV     @DVADRS,R1      ;CHECK CONTENTS OF THE SWITCHED BUS LOCATION
020744  046701  160114                  BIC     ANDCOM,R1
020750  026701  160106                  CMP     ANDBTS,R1
020754  001401                          BEQ     .+4
020756  104410                          HLT                     ;BITS IN LOCATION ON SWITCHED BUS
                                                                ;INCORRECT AFTER BIT 9 WAS SET
020760  005077  160026                  CLR     @BUSCSR
```

```
020764  032777  001000  160020          BIT     #1000,@BUSCSR   ;WAIT FOR SB INIT TO COMPLETE
020772  001374                          BNE     .-6
020774  000167  175124                  JMP     SRMEX

                                ;IF SWITCH REGISTER SWITCH 12 IS SET, EXECUTE THIS ROUTINE
                                ;SET COMMUNICATION BIT IF ANY ERRORS OCCURRED ON THIS SIDE
021000  032777  010000  160030  SRM13:  BIT     #10000,@SR
021006  001417                          BEQ     SRM14
021010  005767  000716                  TST     ERR
021014  100003                          BPL     .+10                    ;BRANCH IF NO ERRORS OCCURRED
021016  052777  004000  157766          BIS     #4000,@BUSCSR           ;SET COMMUNICATION BIT IF ANY
                                                                        ;ERRORS OCCURRED
021024  005327  000000                  DEC     #0                      ;STALL TO IGNORE SWITCH REGISTER BOUNCE
021030  001375                          BNE     .-4
021032  032777  010000  157776          BIT     #10000,@SR
021040  001374                          BNE     .-6
021042  000167  175056                  JMP     SRMEX

                                ;IF SWITCH REGISTER SWITCH 13 IS SET, EXECUTE THIS ROUTINE
021046  032777  020000  157762  SRM14:  BIT     #20000,@SR
021054  001404                          BEQ     SRM15
021056  005067  000650                  CLR     ERR                     ;INITIALIZE ERROR FLAG
021062  000167  177430                  JMP     SRM11A
021066  000167  175040          SRM15:  JMP     SRMON
021072  000000                  FLAGS:  0

                                ;INPUT OF INFORMATION NECESSARY TO TEST THE SWITCH
                                ;AN ADDRESS OF SOMETHING OUT ON THE SWITCHED BUS MUST BE GIVEN TO RUN
                                ;SOME OF THE TESTS. IF ANY NPR DEVICES ARE ON THE SWITCHED BUS, THE
                                ;ADDRESS OF ONE OF THE WORD COUNT OR BUS ADDRESS REGISTERS SHOULD BE GIVEN.
                                ;SPECIFICALLY, THE PROGRAM NEEDS THE ADDRESS OF A LOCATION WHICH HAS AT LEAST 1
                                ;BIT WHICH IS READ/WRITE AND IS CLEARED BY INIT. IF NO SUCH LOCATION
                                ;EXISTS ON THE SWITCHED BUS, THEN THE BEST YOU CAN DO IS GIVE THE ADDRESS OF
                                ;A LOCATION WHICH IS READ/WRITE ON THE SWITCHED BUS, SUCH AS A MEMORY
                                ;LOCATION.  IN THIS CASE, INIT ON THE SWITCHED BUS WILL NOT BE TESTED.
021074  104022          INFORM: PMSG9                   ;"SET THE ADDRESS OF THE WORD COUNT
021076  000000                  HALT                    ;REGISTER OR BUS ADDRESS REGISTER OF AN
                                                        ;NPR DEVICE WHICH IS ON THE
                                                        ;SWITCHED BUS IN THE SWITCH REGISTER SWITCHES.
                                                        ;SEE SECTION 8 OF THE DOCUMENT
                                                        ;FOR THE CONDITIONS THAT THIS
                                                        ;ADDRESS MUST SATISFY. THEN PRESS
                                                        ;'CONTINUE' ON THIS PROCESSOR."
021100  017767  157732  157746          MOV     @SR,DVADRS      ;SAVE THE DEVICE ADDRESS
021106  104024                          PMSG10                  ;"SET THE SWITCH REGISTER SWITCHES
021110  000000                          HALT                    ;CORRESPONDING TO THE BITS IN THAT
                                                                ;ADDRESS THAT ARE READ/WRITE.
                                                                ;THEN PRESS 'CONTINUE' ON THIS
                                                                ;PROCESSOR."
021112  017767  157720  157736          MOV     @SR,RWBITS      ;SAVE RW LOCATION INFORMATION
021120  104060                          PMSG24                  ;"SET THE SWITCH REGISTER SWITCHES
021122  000000                          HALT                    ;CORRESPONDING TO THE BITS IN THAT
                                                                ;ADDRESS THAT ARE CLEARED BY
                                                                ;INIT. THEN PRESS 'CONTINUE' ON
                                                                ;THIS PROCESSOR."
021124  017767  157706  157726          MOV     @SR,INBITS      ;SAVE INFORMATION
```

```
021132  016767  157720  157722          MOV     RWBITS,ANDBTS   ;SETUP TO FIND WHICH BITS ARE BOTH
021140  005167  157714                  COM     INBITS          ;RW AND CLEARFD BY INIT
021144  046767  157710  157710          BIC     INBITS,ANDBTS   ;ANDBTS IS NOW THE LOGICAL AND
021152  005167  157702                  COM     INBITS          ;OF INBITS AND RWBITS
021156  016767  157   157700            MOV     ANDBTS,ANDCOM
021164  005167  1576.                  COM     ANDCOM          ;SETUP COMPLEMENT TO MASK OFF REST
021170  104026                          PMSG11                  ;"RESTORE THE SWITCH REGISTER TO DYNAMIC SWITCH SETTINGS
021172  000000                          HALT                    ;THEN PRESS CONTINUE ON THIS PROCESSOR"
021174  000207                          RTS     %7

                                ;ROUTINE TO ALLOW SCOPING OF ONE-SHOT DELAYS FOR SETTING
                                ;TIMEOUT TIMER AND SWITCHED BUS INIT TIMER
                                ;BOTH PROCESSORS MUST RUN THE ROUTINE AT THE SAME TIME, AND THE BUS SWITCH
                                ;SHOULD HAVE THE "INIT-INHIBIT INIT" SWITCH SET TO THE "-INIT" POSITION
021176  012777  021224  157612  TIMERS: MOV     #TIMRET,@BSIVI  ;SETUP "SWITCH CONNECTED"
021204  005077  157610                  CLR     @BSSTI          ;INTERRUPT RETURN
021210  005077  157620                  CLR     @PSR            ;SET PROCESSOR STATUS TO 0
021214  012777  000401  157570  TIMREQ: MOV     #401,@BUSCSR    ;REQUEST SWITCH AND SET INTERRUPT
                                                                ;ENABLE 1
021222  000001                          WAIT                    ;UNTIL SWITCH CONNECTS NO
                                                                ;MASTER SYNCS WILL OCCUR
021224  022626                  TIMRET: CMP     (SP)+,(SP)+     ;WHEN SWITCH CONNECTS,RESTORE
                                                                ;STACK POINTER
021226  105777  157560                  TSTB    @BUSCSR         ;CHECK CONNECTED BIT-SWITCH WILL
021232  100775                          BMI     .-4             ;SWITCH DUE TO TIME OUT, AND
                                                                ;SWITCHED BUS INIT WILL OCCUR
                                                                ;WHEN IT SWITCHES
021234  000767                          BR      TIMREQ          ;LOOP TO REQUEST SWITCH AGAIN

                                ;EMT HANDLER
021236  011667  001106          EMTSRV: MOV     @SP,TYTMP       ;GET CALL
021242  162767  000002  001100          SUB     #2,TYTMP
021250  017767  001074  001072          MOV     @TYTMP,TYTMP
021256  105067  001067                  CLRB    TYTMP+1         ;SAVE OFFSET ONLY
021262  062767  021304  001060          ADD     #EMTAB,TYTMP
021270  017767  001054  001052          MOV     @TYTMP,TYTMP    ;SETUP MESSAGE ADDRESS
021276  004767  001022                  JSR     %7,TYPE         ;TYPE MESSAGE
021302  000002                          RTI                     ;RETURN
021304  000000                  EMTAB:  0
021306  025074                          MSG1
021310  025100                          MSG2
021312  025110                          MSG3
021314  025120                          MSG4
021316  025130                          MSG5
021320  025136                          MSG6
021322  025152                          MSG7
021324  025166                          MSG8
021326  025174                          MSG9
021330  025202                          MSG10
021332  025212                          MSG11
021334  025220                          MSG12
021336  025230                          MSG13
021340  025240                          MSG14
021342  025250                          MSG15
021344  025260                          MSG16
021346  025270                          MSG17
```

```
021350  025300                          MSG18
021352  025310                          MSG19
021354  025320                          MSG20
021356  025326                          MSG21
021360  025336                          MSG22
021362  025354                          MSG23
021364  025362                          MSG24
021366  025372                          MSG25
021370  025376                          MSG26
021372  025404                          MSG27
021374  025410                          MSG28
021376  025420                          MSG29
021400  025430                          MSG30
021402  025434                          MSG31
021404  025440                          MSG32
021406  025444                          MSG33
021410  025450                          MSG34
021412  025456                          MSG35
021414  025466                          MSG36
021416  025476                          MSG37
021420  025506                          MSG38
021422  025516                          MSG39
021424  025526                          MSG40
021426  025536                          MSG41
021430  025556                          MSG42

104002                                  PMSG1=EMT+2
104004                                  PMSG2=EMT+4
104006                                  PMSG3=EMT+6
104010                                  PMSG4=EMT+10
104012                                  PMSG5=EMT+12
104014                                  PMSG6=EMT+14
104016                                  PMSG7=EMT+16
104020                                  PMSG8=EMT+20
104022                                  PMSG9=EMT+22
104024                                  PMSG10=EMT+24
104026                                  PMSG11=EMT+26
104030                                  PMSG12=EMT+30
104032                                  PMSG13=EMT+32
104034                                  PMSG14=EMT+34
104036                                  PMSG15=EMT+36
104040                                  PMSG16=EMT+40
104042                                  PMSG17=EMT+42
104044                                  PMSG18=EMT+44
104046                                  PMSG19=EMT+46
104050                                  PMSG20=EMT+50
104052                                  PMSG21=EMT+52
104054                                  PMSG22=EMT+54
104056                                  PMSG23=EMT+56
104060                                  PMSG24=EMT+60
104062                                  PMSG25=EMT+62
104064                                  PMSG26=EMT+64
104066                                  PMSG27=EMT+66
104070                                  PMSG28=EMT+70
104072                                  PMSG29=EMT+72
104074                                  PMSG30=EMT+74
```

```
                104076                          PMSG31=EMT+76
                104100                          PMSG32=EMT+100
                104102                          PMSG33=EMT+102
                104104                          PMSG34=EMT+104
                104106                          PMSG35=EMT+106
                104110                          PMSG36=EMT+110
                104112                          PMSG37=EMT+112
                104114                          PMSG38=EMT+114
                104116                          PMSG39=EMT+116
                104120                          PMSG40=EMT+120
                104122                          PMSG41=EMT+122
                104124                          PMSG42=EMT+124

                                        ;TRAP HANDLER
                                        ;DECODES SCOPE AND HLT CALLS
                                        ;FIRST 3 CALLS LEFT OPEN FOR EASY PATCHES
021432  011667  000032                  TRPSRV: MOV     @SP,TPC         ;GET CALL
021436  162767  000002  000024                  SUB     #2,TPC
021444  017767  000020  000016                  MOV     @TPC,TPC
021452  105067  000013                          CLRB    TPC+1           ;SAVE OFFSET ONLY
021456  062767  021472  000004                  ADD     #TPTAB,TPC
021464  017707  000000                          MOV     @TPC,PC         ;GO TO ROUTINE CALLED
021470  000000                          TPC:    0
                104400                          PATCH1=TRAP
                104402                          PATCH2=TRAP+2
                104404                          PATCH3=TRAP+4
                104406                          SCOPE=TRAP+6
                104410                          HLT=TRAP+10
021472  000000                          TPTAB:  0
021474  000000                                  0
021476  000000                                  0
021500  022224                                  SCOPEC
021502  021570                                  PRINT


                                        ;ROUTINE TO LOOP THRU A SINGLE INSTRUCTION TEST
                                        ;LOAD THE STARTING ADDRESS OF THE TEST
                                        ;YOU WISH TO RUN (THE ADDRESS OF THE TESTXX
                                        ;TAG) AT THE 1ST HALT, SET SWITCH REGISTER
                                        ;OPTIONS AT THE 2ND HALT.
                                        ;NOTE THAT SW11 MUST BE DOWN AFTER THE 2ND HALT
021504  005077  157324                  TESTX:  CLR     @PSR
021510  000000                                  HALT                    ;WAIT FOR STARTING ADDRESS
021512  017767  157320  000602                  MOV     @SR,RETURN      ;LOAD STARTING ADDRESS IN RETURN
021520  062767  000002  000574                  ADD     #2,RETURN       ;ADD 2 TO POINT TO INSTRUCTION AFTER
021526  000000                                  HALT                    ;SET SR OPTIONS
021530  012767  177777  157350                  MOV     #-1,TSTX        ;SET FLAG
021536  032777  010000  157272                  BIT     #10000,@SR      ;CHECK SW12
021544  001404                                  BEQ     .+12            ;BRANCH IF NOT SET
021546  042777  000020  157260                  BIC     #20,@PSR        ;CLEAR TRACE BIT
021554  000403                                  BR      .+10            ;SKIP NEXT INSTRUCTION
021556  052777  000020  157250                  BIS     #20,@PSR        ;SET TRACE BIT
021564  000177  000532                          JMP     @RETURN         ;JUMP TO TEST

                                        ;ENTERED WITH SYSTEM TRAP CALL (HLT)
                                        ;PRINT OUT THE ERROR PC+2 AND STATUS REGISTER
```

```
                                        ;(USES REGISTERS)
021570  012767  177777  000134  PRINT:  MOV     #-1,ERR         ;SET FLAG INDICATING ERROR OCCURRED
021576  037727  157234  020000          BIT     @SR,#20000      ;TEST FOR INHIBIT PRINT OUT
021604  001404                          BEQ     .+12            ;BRANCH TO PRINT
021606  037727  157224  040000          BIT     @SR,#40000      ;ONLY INHIBIT IF SCOPE LOOP WAS REQUESTED
021614  001034                          BNE     CK              ;INHIBIT, CHECK FOR HALT
021616  012667  000104                  MOV     (6)+,SAVPC      ;PC OF FAILING ROUTINE
021622  012667  000102                  MOV     (6)+,SAVPSR     ;PSR OF ERROR CONDITION
021626  024646                          CMP     -(6),-(6)       ;RESTORE STACK
021630  012777  000200  157176          MOV     #200,@PSR
021636  004767  000330                  JSR     X7,CRLF         ;OUTPUT CARRIAGE RETURN AND LINE FEED
021642  010267  000052                  MOV     X2,SAVR2        ;SAVE R2
021646  016702  000054                  MOV     SAVPC,X2        ;LOAD REGISTER WITH FAILING PC+2
021652  004767  000106                  JSR     X7,PROCT        ;PRINT FAILING PC+2
021656  105777  157144                  TSTB    @TCSR           ;WAIT FOR TTY READY
021662  100375                          BPL     .-4
021664  012777  000240  157136          MOV     #240,@TDBR      ;OUTPUT A SPACE
021672  016702  000032                  MOV     SAVPSR,X2       ;LOAD PROCESSOR STATUS
021676  004767  000062                  JSR     X7,PROCT        ;PRINT PROCESSOR STATUS
021702  016702  000012                  MOV     SAVR2,X2        ;RESTORE REGISTER
021706  005777  157124          CK:     TST     @SR             ;CHECK SR FOR HALT SWITCH
021712  100001                          BPL     .+4             ;BRANCH IF NOT SET
021714  000000                          HALT                    ;HALT ON ERROR UP
021716  000002                          RTI                     ;RETURN TO MAIN LINE
021720  000000                  SAVR2:  0
021722  000000                  SAVR3:  0
021724  000000                  SAVR4:  0
021726  000000                  SAVPC:  0
021730  000000                  SAVPSR: 0
021732  000000                  ERR:    0

                                        ;SUBROUTINE TO PRINT OUT OCTAL NUMBER
                                        ;PRSHRT DELETES LEADING ZEROS
                                        ;PROCT PRINTS OUT 6 OCTAL DIGITS
                                        ;BOTH USE REGISTERS
021734  012767  000001  000206  PRSHRT: MOV     #1,PRSFLG       ;SET FLAG TO INDICATE SHORT PRINTOUT
021742  005702                          TST     R2              ;CHECK FOR ZERO
021744  001011                          BNE     PROCT+4         ;BRANCH IF NOT ZERO
021746  105777  157084                  TSTB    @TCSR           ;WAIT FOR TTY READY
021752  100375                          BPL     .-4
021754  012777  000260  157046          MOV     #260,@TDBR      ;OUTPUT A SINGLE ZERO
021762  000207                          RTS     X7              ;RETURN
021764  005067  000160          PROCT:  CLR     PRSFLG          ;CLEAR FLAG TO INDICATE FULL PRINTOUT
021770  010367  177766                  MOV     R3,SAVR3        ;SAVE REGISTERS
021774  010467  177764                  MOV     X4,SAVR4
022000  005004                          CLR     X4              ;CLEAR R4 FOR COUNTING CHARACTERS OUTPUT
022002  005067  000144                  CLR     PRFLG           ;INITIALIZE CARRY FLAG FOR ROTATES
022006  012703  000260                  MOV     #260,X3         ;SETUP R3
022012  005702                          TST     X2              ;CHECK BIT 15 OF NUMBER
022014  100001                          BPL     .+4             ;BRANCH IF ZERO
022016  005203                          INC     X3              ;INCREMENT R3 IF ONE
022020  006102                          ROL     X2              ;ROTATE LEFT MOST OCTAL TO RIGHT END
022022  006102                          ROL     X2
022024  006067  000122                  ROC     PRFLG           ;STORE CARRY
022030  005767  000114          P.CK:   TST     PRSFLG          ;CHECK FOR SHORT PRINTOUT
022034  001403                          BEQ     P.WAIT          ;BRANCH IF NOT SET
```

```
022036  020327  000260                  CMP     X3,#260         ;CHECK FOR ZERO IF SET
022042  001407                          BEQ     P.CONT          ;IF SET, GO TO NEXT CHARACTER

022044  105777  156756          P.WAIT: TSTB    @TCSR           ;WAIT FOR TTY READY
022050  100375                          BPL     P.WAIT
022052  010377  156752                  MOV     X3,@TDBR        ;OUTPUT NEXT CHARACTER
022056  005067  000066                  CLR     PRSFLG          ;PRINT REST OF NUMBER AFTER A NON-ZERO DIGIT
022062  005204                  P.CONT: INC     X4              ;COUNT
022064  020427  000006                  CMP     X4,#6           ;CHECK FOR DONE
022070  001005                          BNE     P.CNT1          ;BRANCH IF NOT DONE
022072  016703  177624                  MOV     SAVR3,R3        ;RESTORE REGISTERS
022076  016704  177622                  MOV     SAVR4,X4
022102  000207                          RTS     X7
022104  000241                  P.CNT1: CLC                     ;CLEAR CARRY
022106  005767  000040                  TST     PRFLG           ;CHECK FOR PREVIOUS CARRY
022112  001403                          BEQ     .+10            ;BRANCH IF PREVIOUSLY ZERO
022114  005067  000032                  CLR     PRFLG           ;INITIALIZE FLAG
022120  000261                          SEC                     ;SET CARRY
022122  006102                          ROL     X2              ;ROTATE NEXT CHARACTER INTO RIGHT END OF REGISTER
022124  006102                          ROL     X2
022126  006102                          ROL     X2
022130  005567  000016                  ADC     PRFLG           ;STORE CARRY
022134  010203                          MOV     X2,X3           ;LOAD DATA INTO R3
022136  042703  177770                  BIC     #177770,X3      ;CLEAR ALL BUT LOWEST OCTAL DIGIT
022142  052703  000260                  BIS     #260,X3         ;SET TO ASCII EQUIVALENT
022146  000730                          BR      P.CK            ;LOOP
022150  000000          PRSFLG: 0
022152  000000          PRFLG:  0

                                        ;BELL ON PASS COMPLETE
022154  105777  156646          BELL:   TSTB    @TCSR
022160  100375                          BPL     .-4
022162  012777  000207  156640          MOV     #207,@TDBR
022170  000207                          RTS     X7

                                        ;SUBROUTINE TO OUTPUT CARRIAGE RETURN AND LINE FEED
022172  105777  156630          CRLF:   TSTB    @TCSR           ;WAIT FOR TTY READY
022176  100375                          BPL     .-4
022200  012777  000215  156622          MOV     #215,@TDBR      ;OUTPUT CARRIAGE RETURN
022206  105777  156614                  TSTB    @TCSR           ;WAIT FOR TTY READY
022212  100375                          BPL     .-4
022214  012777  000212  156606          MOV     #212,@TDBR      ;OUTPUT LINEFEED
022222  000207                          RTS     X7              ;RETURN

                                        ;SCOPE AND/OR ITERATION LOOP FOR EACH TEST 64 TIMES
                                        ;A SETUP ROUTINE SHOULD INITIALIZE RETURN AND ICOUNT
022224  032777  040000  156604  SCOPEC: BIT     #40000,@SR      ;TEST SR FOR SCOPE
022232  001015                          BNE     SCOPEB          ;YES, SCOPE
022234  032777  004000  156574          BIT     #4000,@SR       ;NO-TEST FOR ITERATION
022242  001016                          BNE     SCOPEG          ;INHIBIT ITERATION
022244  005767  156636                  TST     TSTX            ;USING SINGLE SUBTEST STARTUP?
022250  001006                          BNE     SCOPEB          ;YES, LOOP
022252  026767  000042  000036          CMP     SCOPEF,ICOUNT   ;COMPARE CURRENT COUNT TO MAX NUMBER
022260  100007                          BPL     SCOPEG          ;EXIT-DONE
022262  005267  000032                  INC     SCOPEF          ;INCREMENT COUNT
022266  005726          SCOPEB: TST     (6)+                    ;REPOSITION STACK
```

```
022270  012677  156540                  MOV     (6)+,@PSR       ;RESTORE PREVIOUS PROCESSOR STATUS
022274  000177  000022                  JMP     @RETURN         ;REPEAT TEST
022300  005067  156602          SCOPEG: CLR     TSTX            ;IF USING TESTX STARTUP, RETURN TO NORMAL FLOW
022304  005067  000010                  CLR     SCOPEF          ;CLEAR COUNT
022310  011667  000006                  MOV     @6,RETURN       ;SAVE SCOPE RETURN POINTER
022314  000002                          RTI                     ;RETURN INLINE-NEXT TEST
022316  000100          ICOUNT: 100                             ;ITERATION COUNT
022320  000000          SCOPEF: 0                               ;COUNT LOCATION FOR ITERATION LOOP
022322  000000          RETURN: 0                               ;ADDRESS OF LAST TEST

                        ;MESSAGE TABLE HANDLER
022324  017702  000020  TYPE:   MOV     @TYTMP,R2       ;PUT ADDRESS OF ASCII IN R2
022330  001001                  BNE     .+4             ;IF ZERO, EXIT
022332  000207                  RTS     %7
022334  062767  000002  000006          ADD     #2,TYTMP        ;OTHERWISE, MOVE POINTER
022342  004767  000004                  JSR     %7,TOUT         ;TYPE ASCII
022346  000766                          BR      TYPE            ;LOOP TILL ALL SUB-MESSAGES HAVE BEEN PRINTED
022350  000000          TYTMP:  0

                        ;MESSAGE SUBROUTINE
                        ;TO USE, MOVE ADDRESS OF MESSAGE TO REGISTER 2
                        ;THEN JSR %7, TOUT
022352  142777  000177  156446  TOUT:   BICB    #177,@TCSR      ;CLR INT FLAG
022360  105712          A.TOUT: TSTB    @R2             ;COMPARE FOR EOM
022362  001001                  BNE     .+4             ;BRANCH IF NOT END OF MESSAGE
022364  000207                  RTS     %7              ;RETURN IF EOM
022366  121227  000100          CMPB    @R2,#'@         ;CHECK FOR CR,LF REQUEST
022372  001003                  BNE     .+10            ;BRANCH IF NOT
022374  004767  177572          JSR     %7,CRLF         ;OUTPUT CARRIAGE RETURN, LINEFEED
022400  000405                  BR      A.INC           ;NEXT CHARACTER
022402  105777  156420          TSTB    @TCSR           ;WAIT FOR TTY
022406  100375                  BPL     .-4
022410  111277  156414          MOVB    (2),@TDBR       ;OUTPUT NEXT CHARACTER
022414  005202          A.INC:  INC     R2
022416  000760                  BR      A.TOUT          ;CONTINUE

022420  052100  042510  044440  S1:     .ASCIZ  /@THE INTERRUPT LEVEL WAS /
022436  042116  051105  052522
022434  042120  041040  053105
022442  046105  053440  051501
022450  000040

022452  041500  040510  043516  S2:     .ASCIZ  /@CHANGE SR OF OTHER CPU:@/
022460  020105  051123  047440
022466  020106  052117  042510
022474  020122  050103  036125
022502  000100

022504  041500  042514  051101  S3:     .ASCIZ  /@CLEAR SR OF OTHER CPU/
022512  051440  020122  043117
022520  047440  044124  051105
022526  041440  052520      000

022533      123 052105  051440  S4:     .ASCIZ  /SET SWITCH /
022540  044527  041524  020110
022546      000
```

```
022547     040  047524  040440  S5:     .ASCIZ  / TO A ONE/
022554  047440  042516     000

022561     100  046103  040505  S6:     .ASCIZ  /@CLEAR SWITCH /
022566  020122  053523  052111
022574  044103  000040

022600  042532  047522     000  SN0:    .ASCIZ  /ZERO/

022605     117  042516     000  SN1:    .ASCIZ  /ONE/

022611     124  047527     000  SN2:    .ASCIZ  /TWO/

022615     124  051110  042505  SN3:    .ASCIZ  /THREE/
022622     000

022623     106  052517  000122  SN4:    .ASCIZ  /FOUR/

022630  044506  042526     000  SN5:    .ASCIZ  /FIVE/

022635     123  054111     000  SN6:    .ASCIZ  /SIX/

022641     123  053105  047105  SN7:    .ASCIZ  /SEVEN/
022646     000

022647     105  043511  052110  SN8:    .ASCIZ  /EIGHT/
022654     000

022655     116  047111  000105  SN9:    .ASCIZ  /NINE/

022662  040440  042116  052040  S8:     .ASCIZ  / AND THEN /
022670  042510  020116     000

022675     100  044124  047105  S9:     .ASCIZ  /@THEN PRESS "CONT" ON THIS CPU@@@/
022702  050040  042522  051523
022710  021040  047503  052116
022716  020042  047117  052040
022724  044510  020123  050103
022732  040125  040100     000

022737     124  047105     000  SN10:   .ASCIZ  /TEN/

022743     105  042514  042526  SN11:   .ASCIZ  /ELEVEN/
022750  000116

022752  053524  046105  042526  SN12:   .ASCIZ  /TWELVE/
022760     000

022761     124  044510  052122  SN13:   .ASCIZ  /THIRTEEN/
022766  042505  000116

022772  050100  042517  051105  S10:    .ASCIZ  /@POWER DOWN ONE DEVICE ON THE SWITCHED BUS@/
023000  042040  042517  000116
023006  047117  020105  042504
023014  044526  042503  047440
```

```
023022  020116  044124  020105
023030  053523  052111  044103
023036  042105  041040  051525
023044  000100

023046  050100  053517  051105  S11:    .ASCIZ  /@POWER THE DEVICE BACK UP/
023054  052040  042510  042040
023062  053105  041511  020105
023070  040502  045503  052440
023076  000120

023100  051500  040524  052122  S12:    .ASCII  /@START THE OTHER CPU AT SA 210/
023106  052040  042510  047440
023114  044124  051105  041440
023122  052520  040440  020124
023130  040523  031040  030061

023136  040500  042116  044440          .ASCIZ  /@AND INPUT THE INFORMATION REQUESTED/
023144  050116  052125  052040
023152  042510  044440  043116
023160  051117  040515  044524
023166  047117  051040  050505
023174  042525  052123  042105
023202      000

023203      100  042523  020124  S13:    .ASCII  ;@SET THE ADDRESS OF THE WORD COUNT REGISTER OR BUS ;
023210  044124  020105  042101
023216  051104  051505  020123
023224  043117  052040  042510
023232  053440  051117  020104
023240  047503  047125  020124
023246  042522  044507  020123
023254  051105  047440  020122
023262  052502  020123

023266  042101  051104  051505          .ASCII  ;ADDRESS REGISTER @OF AN NPR DEVICE WHICH IS ON ;
023274  020123  042522  044507
023302  052123  051105  040040
023310  043117  040440  020116
023316  047116  020122  020124
023324  040524  042503  020440
023332  044510  044103  044440
023340  020123  047117      040

023345      124  042510  051440          .ASCII  ;THE SWITCHED BUS @IN THE SWITCH REGISTER (SR) SWITCHES.@;
023353  044527  041524  042510
023360  020104  052502  020123
023366  044500  020116  044124
023374  020105  053523  052111
023402  044103  051040  042505
023410  051611  042524  020122
023416  051450  024522  051440
023424  044527  041524  042510
023432  027123      100

023435      123  042505  051440          .ASCII  ;SEE SECTION 5.2.9 OF THE DOCUMENT FOR THE CONDITIONS @;
```

```
023442  041505  044524  047117
023450  032440  031056  034456
023456  047440  020106  044124
023464  020105  047504  052503
023472  042515  052116  043040
023500  051117  052040  042510
023506  041440  047117  044504
023514  044524  047117  020123
023522     100

023523     124  040510  020124          .ASCIZ  ;THAT THIS ADDRESS MUST SATISFY.;
023530  044124  051511  040440
023536  042104  042522  051523
023544  046440  051505  020124
023552  040523  044524  043163
023560  027131     000

023563     100  042523  020124  S14:    .ASCII  /@SET THE SR SWITCHES CORRESPONDING TO@THE /
023570  044124  020105  051123
023576  051440  044527  041524
023604  042510  020123  047503
023612  051122  051505  047520
023620  042116  047111  020107
023626  047524  052100  042510
023634     040

023635     102  052111  020123          .ASCIZ  /BITS IN THAT ADDRESS /
023642  047111  052040  040510
023650  020124  042101  051104
023656  051505  020123     000

023663     124  040510  020124  S14A:   .ASCIZ  #THAT ARE READ/WRITE#
023670  051101  020125  020122
023676  042101  052517  044502
023704  042524     000

023707     100  042522  052123  S15:    .ASCIZ  /@RESTORE SR TO DYNAMIC SWITCH SETTINGS/
023714  051117  020105  051123
023722  020040  020117  054504
023730  040516  044515  020103
023736  053523  052111  044103
023744  051440  020105  044524
023752  043516  000123

023756  050100  052125  052040  S16:    .ASCIZ  /@PUT THE "INIT-INHIBIT INIT" SWITCH IN THE /
023764  042510  021040  047111
023772  052111  044455  044116
024000  041111  052111  044440
024006  044516  021124  051440
024014  044527  041524  020110
024022  047111  052040  042510
024030  000040

024032  044442  044116  041111  S17:    .ASCIZ  /"INHIBIT INIT" POSITION/
024040  052111  044440  044516
024046  021124  050040  051517
```

```
024054  052111  047511  000116

024062  044442  044516  021124  S18:    .ASCIZ  /^INIT^ POSITION/
024070  050040  051517  052111
024076  047511  000116

024102  050100  053517  051105  S19:    .ASCIZ  /@POWER DOWN THIS CPU/
024110  042040  053517  020116
024116  044124  051511  041440
024124  052520     000

024127     100  047520  042527  S20:    .ASCIZ  /@POWER THIS CPU BACK UP@@@/
024134  020122  044124  051511
024142  041440  052520  041040
024150  041501  020113  050125
024156  040100  000100

024162  050100  053517  051105  S21:    .ASCIZ  /@POWER DOWN THE DT11/
024170  042040  053517  020116
024176  044124  020105  052104
024204  030461     000

024207     100  044124  047105  S22:    .ASCIZ  /@THEN POWER THE DT11 BACK UP@@@/
024214  050040  053517  051105
024222  052040  042510  042040
024230  03  24  0  1  0  3
024236  045  03  0  0  040120
024244  040100     000

024247     040  047111  [illegible]  S23:    .ASCIZ  / IN THIS CPU'S SR@@@/
024254  044510  020123  [illegible]
024262  023525  020123  051123
024270  040100  000100

024274  044124  052101  040440  S24:    .ASCIZ  /THAT ARE CLEARED BY INIT./
024302  042522  041440  042514
024310  051101  042105  041040
024316  020131  047111  052111
024324  000056

024327  044500  050116  052125  S25:    .ASCIZ  /@INPUT THE SAME INFORMATION AS INITIALLY REQUESTED ON THE OTHER SIDE/
024335  052040  042510  051440
024343  041501  020105  047111
024351  047506  046522  052101
024357  047511  020116  051501
024365  044440  044516  044524
024373  046101  054514  051040
024401  050505  042525  042123
024407  042105  047440  020116
024415  044124  020105  052117
024423  042510  020122  044523
024431  042504     000

024433     100  046103  040505  S26:    .ASCIZ  /@CLEAR SR OF OTHER CPU, THEN SET SWITCH /
024440  020122  051123  047440
024446  020106  052117  042510
```

```
024454  020122  050103  026125
024462  052040  042510  020116
024470  042523  020124  053523
024476  052111  044103  000040

024504  053500  042510  020116  S27:    .ASCIZ  /@WHEN THIS PRINTOUT IS FINISHED PRESS "CONTINUE." THEN/
024512  044124  051511  050040
024520  044522  052116  052517
024526  020124  051511  043040
024534  047111  051511  042510
024542  020104  051120  051505
024550  020123  041442  047117
024556  044524  052516  027105
024564  020042  044124  047105
024572     000

024573     100  040100  047105  S28:    .ASCIZ  /@@@END OF PASS@/
024600  020104  043117  050040
024606  051501  040123     000

024613     116  020117          S29:    .ASCII  /NO /

024616  051105  047522  051522  S30:    .ASCIZ  /ERRORS OCCURRED/
024624  047440  041503  051125
024632  042522  000104

024636  050100  053517  051105  S31:    .ASCIZ  /@POWER FAIL WAS /
024644  043040  044501  020114
024652  040527  020123     000

024657     116  052117  000040  S32:    .ASCIZ  /NOT /

024664  042524  052123  042105  S33:    .ASCIZ  /TESTED/
024672     000

024673     100  051123  051440  S34:    .ASCIZ  /@SR SWITCH NINE WAS/
024700  044527  041524  020110
024706  044516  042516  053440
024714  051501     000

024717     040  042523  040124  S35:    .ASCIZ  / SET@@@@/
024724  040100  000100

024730  041440  042514  051101  S36:    .ASCIZ  / CLEAR@@@@/
024736  040100  040100     000

024743     100  053523  052111  S37:    .ASCIZ  /@SWITCHED BUS POWER FAIL WAS /
024750  044103  042105  041040
024756  051525  050040  053517
024764  051105  043040  044501
024772  020114  040527  020123
025000     000

025001     106  046125  054514  S38:    .ASCIZ  /FULLY /
025006  000040
```

```
025010  040520  052122  040511  S39:    .ASCIZ  /PARTIALLY /
025016  046114  020131     000

025023     100  047524  043507  S40:    .ASCIZ  /@TOGGLE SWITCH ZERO AT LEAST TEN TIMES@/
025030  042514  051440  044527
025036  041524  020110  042532
025044  047522  040440  020124
025052  042514  051501  020124
025060  042524  020116  044524
025066  042515  040123     000

        025074                          .EVEN
                                ;MSG1:  "THE INTERRUPT LEVEL WAS"

025074  022420  000000          MSG1:   .WORD   S1,0

                                ;MSG2:  "CLEAR SR OF OTHER CPU
                                        ;THEN SET SWITCH 0.
                                        ;THEN PRESS 'CONTINUE' ON THIS
                                        ;PROCESSOR."

025100  024433  022600  022675  MSG2:   .WORD   S26,SN0,S9,0
025106  000000

                                ;MSG3:  "CLEAR SR OF OTHER CPU
                                        ;THEN SET SWITCH ONE. THEN PRESS
                                        ;'CONTINUE' ON THIS PROCESSOR."

025110  024433  022605  022675  MSG3:   .WORD   S26,SN1,S9,0
025116  000000

                                ;MSG4:  "CLEAR SR OF OTHER CPU.
                                        ;THEN SET SWITCH 2. THEN PRESS
                                        ;'CONTINUE' ON THIS PROCESSOR."

025120  024433  022611  022675  MSG4:   .WORD   S26,SN2,S9,0
025126  000000

                                ;MSG5:  "CLEAR SR OF OTHER CPU.
                                        ;THEN PRESS 'CONT' ON THIS CPU."

025130  022504  022675  000000  MSG5:   .WORD   S3,S9,0

                                ;MSG6:  "POWER DOWN ONE DEVICE ON
                                        ;THE SWITCHED BUS, AND THEN SET SWITCH 0
                                        ;IN THIS PROCESSOR'S SWITCH REGISTER."

025136  022772  022662  022533  MSG6:   .WORD   S10,S8,S4,SN0,S23,0
025144  022600  024247  000000

                                ;MSG7:  "POWER THE DEVICE BACK UP, AND THEN CLEAR SWITCH 0 IN
                                        ;THIS PROCESSOR'S SWITCH REGISTER"

025152  023046  022662  022561  MSG7:   .WORD   S11,S8,S6,SN0,S23,0
025160  022600  024247  000000
```

```
                                        ;MSG8:  "START THE OTHER PROCESSOR AT STARTING ADDRESS 210. THEN
                                        ;PRESS 'CONTINUE' ON THIS PROCESSOR."

025166  023100  022675  000000  MSG8:   S12,S9,0

                                        ;MSG9:  "SET THE ADDRESS OF THE WORD COUNT REGISTER OR BUS ADDRESS
                                        ;REGISTER OF AN NPR DEVICE WHICH IS ON THE SWITCHED BUS IN
                                        ;THE SWITCH REGISTER SWITCHES. SEE SECTION 8 OF THE DOCUMENT
                                        ;FOR THE CONDITIONS THAT THIS ADDRESS MUST SATISFY. THEN PRESS
                                        ;'CONTINUE' ON THIS PROCESSOR."

025174  023203  022675  000000  MSG9:   S13,S9,0

                                        ;MSG10: "SET THE SWITCH REGISTER SWITCHES CORRESPONDING TO THE BITS IN
                                        ;THAT ADDRESS THAT ARE READ/WRITE. THEN PRESS 'CONTINUE' ON THIS
                                        ;PROCESSOR."

025202  023563  023663  022675  MSG10:  S14,S14A,S9,0
025210  000000

                                        ;MSG11: "RESTORE SWITCH REGISTER TO DYNAMIC SWITCH SETTINGS.
                                        ;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."

025212  023707  022675  000000  MSG11:  S15,S9,0

                                        ;MSG12: "PUT THE 'INIT-INHIBIT INIT' SWITCH IN THE 'INHIBIT INIT' POSITION.
                                        ;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."

025220  023756  024032  022675  MSG12:  S16,S17,S9,0
025226  000000

                                        ;MSG13: "PUT THE 'INIT-INHIBIT INIT' SWITCH IN THE 'INIT' POSITION.
                                        ;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."

025230  023756  024062  022675  MSG13:  S16,S18,S9,0
025236  000000

                                        ;MSG14: "CLEAR SR OF OTHER CPU,
                                        ;THEN SET SWITCH 3.
                                        ;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."

025240  024433  022615  022675  MSG14:  S26,SN3,S9,0
025246  000000

                                        ;MSG15: "CLEAR SR OF OTHER CPU,
                                        ;THEN SET SWITCH 4.
                                        ;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."

025250  024433  022623  022675  MSG15:  S26,SN4,S9,0
025256  000000

                                        ;MSG16: "CLEAR SR OF OTHER CPU,
                                        ;THEN SET SWITCH 5.
                                        ;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."

025260  024433  022630  022675  MSG16:  S26,SN5,S9,0
```

```
        025266  000000

                                        ;MSG17: "CLEAR SR OF OTHER CPU,
                                        ;THEN SET SWITCH 6.
                                        ;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."

        025270  024433  022635  022675  MSG17:  S26,SN6,S9,0
        025276  000000

                                        ;MSG18: "CLEAR SR OF OTHER CPU,
                                        ;THEN SET SWITCH 7.
                                        ;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."

        025300  024433  022641  022675  MSG18:  S26,SN7,S9,0
        025306  000000

                                        ;MSG19: "CLEAR SR OF OTHER CPU,
                                        ;THEN SET SWITCH 8.
                                        ;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."

        025310  024433  022647  022675  MSG19:  S26,SN8,S9,0
        025316  000000

                                        ;MSG20: "SR SWITCH 9 WAS SET"

        025320  024673  024717  000000  MSG20:  S34,S35,0

                                        ;MSG21: "POWER DOWN THIS PROCESSOR. AND THEN
                                        ;POWER THIS PROCESSOR BACKUP."

        025326  024102  022662  024127  MSG21:  S19,S8,S20,0
        025334  000000

                                        ;MSG22: "POWER DOWN THIS PROCESSOR
                                        ;CHANGE SWITCH REGISTER OF OTHER PROCESSOR:
                                        ;SET SWITCH 9.
                                        ;AND THEN POWER THIS PROCESSOR BACKUP."

        025336  024102  022452  022533  MSG22:  S19,S2,S4,SN9,S8,S20,0
        025344  022655  022662  024127
        025352  000000

                                        ;MSG23: "POWER DOWN THE BUS SWITCH.
                                        ;THEN POWER THE BUS SWITCH BACK UP."

        025354  024162  024207  000000  MSG23:  S21,S22,0

                                        ;MSG24: "SET THE SWITCH REGISTER SWITCHES CORRESPONDING TO THE
                                        ;BITS IN THAT ADDRESS THAT ARE CLEARED BY INIT.
                                        ;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."

        025362  023563  024274  022675  MSG24:  S14,S24,S9,0
        025370  000000

                                        ;MSG25: "CLEAR SR OF OTHER CPU."
```

```
025372  022504  000000          MSG25:  S3,0
                                ;MSG26: "SR SWITCH 9 WAS CLEAR."
025376  024673  024730  000000  MSG26: S34,S36,0

                                ;MSG27: "INPUT THE SAME INFORMATION AS INITIALLY REQUESTED ON
                                ;THE OTHER SIDE."
025404  024326  000000          MSG27:  S25,0
                                ;MSG28: "CLEAR SR OF OTHER CPU,
                                ;THEN SET SWITCH 10.
                                ;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."
025410  024433  022737  022675  MSG28:  S26,SN10,S9,0
025416  000000

                                ;MSG29: "CLEAR SR OF OTHER CPU,
                                ;THEN SET SWITCH 11.
                                ;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."
025420  024433  022743  022675  MSG29:  S26,SN11,S9,0
025426  000000

                                ;MSG30: "WHEN THIS PRINTOUT IS FINISHED, PRESS "CONTINUE". THEN"
025430  024504  000000          MSG3C:  S27,0
                                ;MSG31: "END OF PASS"
025434  024573  000000          MSG31:  S28,0
                                ;MSG32: "NO ERRORS OCCURRED"
025440  024613  000000          MSG32:  S29,0
                                ;MSG33: "ERRORS OCCURRED"
025444  024616  000000          MSG33:  S30,0
                                ;MSG34: "POWER FAIL WAS TESTED"
025450  024636  024664  000000  MSG34:  S31,S33,0
                                ;MSG35: "POWER FAIL WAS NOT TESTED"
025456  024636  024657  024664  MSG35:  S31,S32,S33,0
025464  000000

                                ;MSG36: "CLEAR SR OF OTHER CPU,
                                ;THEN SET SWITCH TWELVE.
                                ;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."
025466  024433  022752  022675  MSG36:  S26,SN12,S9,0
```

```
        025474  000000

                                        ;MSG37: "CLEAR SR OF OTHER CPU,
                                        ;THEN SET SWITCH THIRTEEN.
                                        ;THEN PRESS 'CONT' ON THIS CPU."

        025476  024433  022761  022675  MSG37:  S26,SN13,S9,0
        025504  000000

                                        ;MSG38: "SWITCHED BUS POWER FAIL WAS FULLY TESTED"

        025506  024743  025001  024664  MSG38:  S37,S38,S33,0
        025514  000000

                                        ;MSG39: "SWITCHED BUS POWER FAIL WAS NOT TESTED"

        025516  024743  024657  024664  MSG39:  S37,S32,S33,0
        025524  000000

                                        ;MSG40: "SWITCHED BUS POWER FAIL WAS PARTIALLY TESTED"

        025526  024743  025010  024664  MSG40:  S37,S39,S33,0
        025534  000000

                                        ;MSG41: ;"WHEN THIS PRINTOUT IS FINISHED, PRESS "CONTINUE." THEN
                                        ;CHANGE SR OF OTHER CPU:
                                        ;TOGGLE SWITCH ZERO AT LEAST TEN TIMES
                                        ;THEN SET SWITCH ZERO IN THIS CPU'S SR"

        025536  024504  022452  025023  MSG41:  S27,S2,S40,S8,S4,SN0,S23,0
        025544  022662  022533  022600
        025552  024247  000000

                                        ;MSG42: "CLEAR SR OF OTHER CPU AND THEN
                                        ;CLEAR SWITCH ZERO IN THIS CPU'S SR."

        025556  022504  022662  022561  MSG42:  S3,S8,S6,SN0,S23,0
        025564  022600  024247  000000

                000001                          .END
```

DZDTA.B CROSS REFERENCE TABLE -- USER SYMBOLS

DZDTA.B CROSS REFERENCE TABLE -- USER SYMBOLS

```
CNT1    001444              685     690#
CNT1A   001456              689     693#
CNT2S   005756             1395    1399#
CNT31A  007046             1551    1564#
CNT32A  007206             1579    1596#
CNT33A  007352             1615    1629#
CNT34   007414             1602    1639    1643#
CNT34A  007512             1650    1661#
CNT35   007650             1676    1690#
CNT39A  010732             1904    1914    1916    1920#
CNT4    002036              764     769#
CNT4A   002050              768     772#
CNT40   001046              601#    1933*   1935*   1939*   1950*   1952*
CNT40A  001050              602#    1934*   1936*   1940*   1951*   1953*   1954
CNT53A  014226             2548    2550#
CNT54A  015014             2677    2679#
CNT55   015400             2756    2764#
CNT55A  015436             2774    2777#
CNT55B  015474             2778    2780    2786#   2821
CONT1   001632              712     725#
CONT14  003212              975     981#
CONT16  003370             1020#   1021
CONT23  005506             1343    1348#
CONT24  005626             1367    1372#
CONT25  006026             1407    1410#
CONT26  006200             1428    1437    1440#
CONT27  006322             1460    1463#
CONT28  006434             1479    1482#
CONT29  006560             1504    1507#
CONT30  006706             1528    1532#
CONT42  011404             2022    2024#
CONT43  011636             2073    2075#
CONT50  013246             2362    2364#
CONT51  013500             2417    2419#
CONT53  014234             2510    2551#   2594
CONT54  015022             2639    2680#   2723
CONT6   002216              806     811#
CONT7   002362              843     848#
CONT8   002452              867     872#
COUNT   001066             610#
CRLF    022172             2858    2859    3591    3673#   3721
DONE    015630             1966    1981    2484    2800    2803    2822#
DT11A   001110              581     625#
DT11AF  001104              618#    625*    631*    684     763     1691    1982    2033    2083    2115    2319    2374    2428
                           2480    2491    2620    2755    2799    2836
DVRORS  001054              605#    799*    800     842*    862*    933*    1545*   1546    1556    1573*   1574    1586    1609*
                           1610    1621    1644*   1645    1656    1670*   1671    1681    1781*   2020*   2071*   2358*   2413*
                           2545*   2674*   3308*   3309    3319    3342*   3343    3350    3400*
EMTAB   021304             3447    3451#
EMTSRV  021236              552    3443#
END     016044             1634    2   48
ERR     021732             6444*   2643*   2848    2903*   3365    3378*   3582*   3610#
FLAGS   021072             2909*   3003    3005*   3048    3050*   3381#
HLT   = 104410              676     688     692     700     704     710     718     724     741     752     767     771     783
                            796     802     808     829     840     845     860     865     881     892     904     918     922
                            926     930     934     947     951     956     973     978     996    1032    1037    1050    1075
```

DZDTA.B CROSS REFERENCE TABLE -- USER SYMBOLS

```
                        1081    1097    1121    1127    1143    1167    1173    1189    1213    1219    1235    1259    1265
                        1281    1305    1311    1327    1342    1346    1366    1370    1387    1396    1406    1408    1427
                        1431    1438    1461    1480    1502    1505    1527    1529    1550    1558    1562    1578    1588
                        1592    1614    1623    1627    1649    1654    1660    1675    1685    1688    1719    1732    1750
                        1757    1774    1784    1789    1793    1802    1806    1810    1817    1821    1837    1860    1865
                        1870    1896    1903    1912    1917    1945    1949    1958    2000    2011    2016    2021    2051
                        2062    2067    2072    2099    2110    2114    2136    2147    2151    2170    2181    2185    2210
                        2220    2224    2251    2261    2265    2288    2298    2303    2308    2347    2352    2360    2393
                        2402    2407    2415    2447    2456    2461    2505    2519    2542    2535    2542    2547    2564
                        2570    2583    2591    2609    2634    2648    2661    2664    2671    2676    2693    2699    2712
                        2720    2738    2771    2785    2797    2811    2817    2955    2961    2970    2980    3006    3016
                        3026    3051    3061    3071    3095    3102    3112    3122    3139    3149    3158    3166    3184
                        3190    3203    3212    3219    3230    3240    3260    3269    3279    3289    3313    3323    3347
                        3354    3362#
ICOUNT  022316           670*    728*    733*   1449*   1469*   1693*   1704*   3689    3699#
INBITS  001060           607#   3412*   3414#   3415    3416*
INFORM  021074           628     634    2902    3392#
INITF   001076           614#    640*    816    1599    1694    1705    1709    1735    2823*
INITPA  015764          2856    2861#
INITPB  015720          2837    2842
INITPS  015664          2826    2831#
INITP1  016012          2660    2671#
INITP2  016032          2872    2878#
INTFLG  001042           599#    626*    632*   1028    1030    1044    1046*   1048    1070    1073    1088    1090*   1095
                        1116    1119    1134   1136*   1141    1162    1165    1180    1182*   1187    1208    1211    1226
                        1227    1233    1254   1257    1272    1274*   1279    1300    1303    1318    1320*   1325
LOGICA  016012          2854    2858    2870#
LOOP40  011004          1935#   1938
LOP37A  010362          1833#   1839
LOP40A  011102          1952#   1955
LOP55A  015402          2767#   2770
LOP55B  015426          2768    2775#
MSG1    025074          4052    4043#
MSG10   025202          4061    4102#
MSG11   025212          4062    4108#
MSG12   025220          4063    4113#
MSG13   025230          4064    4119#
MSG14   025240          4065    4124#
MSG15   025250          4066    4133#
MSG16   025260          4067    4140#
MSG17   025270          4070    4147#
MSG18   025300          4071    4154#
MSG19   025310          4072    4161#
MSG2    025160          4053    4050#
MSG20   025320          4073    4166#
MSG21   025330          4074    4171#
MSG22   025340          4075    4179#
MSG23   025350          4076    4186#
MSG24   025360          4077    4192#
MSG25   025370          4078    4197#
MSG26   025400          4079    4201#
MSG27   025410          4080    4207#
MSG28   025420          4081    4213#
MSG29   025430          4082    4220#
MSG3    025110          4054    4057#
MSG30   025440          4083    4225#
```

F07

DZDTA.B CROSS REFERENCE TABLE -- USER SYMBOLS

```
MSG31   025434          3482    4229#
MSG32   025440          3483    4233#
MSG33   025444          3484    4237#
MSG34   025450          3485    4241#
MSG35   025456          3486    4245#
MSG36   025466          3487    4252#
MSG37   025476          3488    4259#
MSG38   025506          3489    4264#
MSG39   025516          3490    4269#
MSG40   025526          3491    4274#
MSG41   025536          3492    4282#
MSG42   025546          3493    4289#
MSG43   025560          3494    4070#
MSG44   025570          3495    4076#
MSG45   025600          3496    4083#
MSG46   025610          3497    4090#
MSG47   025620          3498    4096#
NOP    = 000240          534#
NOPF    001102          617#    647#    649#    1962    1977    2853
NOTRC   016074         2827    2889    2892#
PATCH1= 104400         3548#
PATCH2= 104402         3549#
PATCH3= 104404         3550#
PC     =000007          542#    3546#
PFSAV   001072          612#    1956#   2008    2047#   2059    2095#   2107    2132#   2144    2166#   2178    2206#   2218
                       2247#   2259    2284#   2296    2334#   2344    2389#   2399    2443#   2453    2513#   2529    2579#
                       2597#   2642#   2658    2708#   2726#   3143#   3145    3155#   3156
PIRQ    001040          598#    663
PMSG1 = 104002         1091    1137    1183    1229    1275    1321    3495#
PMSG10= 104024         3401    3504#
PMSG11= 104026         3419    3505#
PMSG12= 104030         1640    2013    3506#
PMSG13= 104032         1696    1737    2078    3507#
PMSG14= 104034         1984    2035    2085    3508#
PMSG15= 104036         2122    3509#
PMSG16= 104040         2155    3510#
PMSG17= 104042         2192    2233    3511#
PMSG18= 104044         2321    2376    2430    3512#
PMSG19= 104046         2493    2622    2761    3513#
PMSG2 = 104004         1744    1766    1794    1927    3496#
PMSG20= 104050         3514#
PMSG21= 104052         1982    2043    2091    2128    2162    2198    2239    3515#
PMSG22= 104054         2277    3516#
PMSG23= 104056         2330    2385    2439    3517#
PMSG24= 104060         3407    3518#
PMSG25= 104062         2759    3519#
PMSG26= 104064         3520#
PMSG27= 104066         2900    3521#
PMSG28= 104070         1713    3522#
PMSG29= 104072         1727    3523#
PMSG3 = 104006         1752    3497#
PMSG30= 104074         2197    2238    3524#
PMSG31= 104076         2847    3525#
PMSG32= 104100         2870    3526#
PMSG33= 104102         2882    3527#
```

DZDTA.B CROSS REFERENCE TABLE -- USER SYMBOLS

DZDTA.B CROSS REFERENCE TABLE -- USER SYMBOLS

```
RETM6A  017114          3040    3057#
RETM6B  017160          3057    3067#
RETM7A  017360          3085    3108#
RETM7B  017424          3108    3118#
RETM8A  020146          3180    3226#
RETM8B  020206          3226    3236#
RETURN  022322           671#   1639#   3568#   3569#   3577    3694    3697#   3701#
RET12   002764           931     937#
RET37   010152          1774    1783#
RET42   011402          2018    2023#
RET43   011634          2069    2074#
RET50A  013112          2328    2333#
RET50B  013146          2333    2339#
RET50C  013244          2343    2353#
RET51A  013324          2363    2368#
RET51B  013374          2388    2394#
RET51C  013476          2411    2418#
RET52A  013600          2437    2445#
RET52B  013630          2443    2448#
RET53A  014044          2498    2511#
RET53B  014074          2511    2520#
RET53C  014524          2544    2549#
RET53D  014364          2562    2577#
RET53K  014414          2577    2584#
RET53M  014452          2585    2595#
RET53N  014474          2595    2602#
RET54B  014632          2627    2640#
RET54B  014662          2640    2648#
RET54C  015012          2673    2678#
RET54D  015152          2651    2706#
RET54E  015202          2706    2713#
RET54F  015240          2694    2724#
RET54H  015262          2724    2731#
RET55   015560          2753    2804#
RET55A  015602          2804    2812#
RET6    00[illegible]212  797     807#
RET7    00[illegible]76   841     844#
RET8    00[illegible]50   861     868#
RSTART  001156          569     637#
R0BITS  001056           606#    799     800     842     862     933     1781    2020    2071    2358    2413    2545    2674
                        3[illegible]#   3413
R0      =%000000         5[illegible]#
R1      =%000001         5[illegible]#   7[illegible]#   716     825#    827     1546#   1547#   1548    1574#   1575#   1576    1610#   1611#
                        1612    1[illegible]   1646#   1647    1656#   1657#   1658    1671#   1672#   1673    1681#   1682#   1683
                        1[illegible]#   1[illegible]   2871#   2874    3309#   3310#   3311    3319#   3320#   3321    3343#   3344#   3345
                        3[illegible]#   3[illegible]#   3352
R2      =%000002         537#    1[illegible]#   1138#   1184#   1230#   1276#   1322#   3617    3704#   3716    3726#
R3      =%0[illegible]3  578#    3624    3647#
R4      =%0[illegible]4  593#
R5      =%0[illegible]5  540#
SAVPC   021726          3[illegible]#   3593    3608#
SAVPSR  021730          3[illegible]#   3598    3609#
SAVR2   021720          3[illegible]#   3600    3605#
SAVR3   021722          3606#   3624#   3647
SAVR4   021724          3607#   3625#   3648
SBINH   001052           603#    650#    653#    656#    2477    2485    2757    2779    2861    2865
```

DZDTA.B CROSS REFERENCE TABLE -- USER SYMBOLS

J07

DZDTA.B CROSS REFERENCE TABLE -- USER SYMBOLS

```
SRET8   017544            3133    3142#   3146
SRET8A  017604            3142    3150#
SRMEX   016124            2904#   2921    2931    2941    2965    2975    2985    3011    3021    3031    3056    3066    3076
                          3099    3107    3117    3127    3141    3172    3192    3225    3235    3245    3266    3274    3284
                          3294    3328    3359    3373
SRMON   016132            2906#   3380
SRMONX  016112             566     572    2900#
SRM1    016160            2914#
SRM10   020252            3177    3250#
SRM10B  020342            3259    3267#
SRM11   020506            3251    3301#
SRM11A  020516            3303#   3379
SRM12   020650            3302    3335#
SRM13   021000            3336    3363#
SRM14   021046            3364    3376#
SRM15   021066            3377    3390#
SRM2    016220            2915    2924#
SRM3    016260            2925    2934#
SRM4    016320            2935    2946#
SRM4A   016356            2953#   2958
SRM5    016534            2947    2950#
SRM5A   016606            3001#   3009
SRM5B   016636            3002    3004    3008#
SRM6    016770            2991    3036#
SRM6A   017042            3046#   3054
SRM6B   017072            3047    3049    3053#
SRM7    017224            3037    3081#
SRM7A   017272            3090#   3094
SRM7B   017324            3092    3100#
SRM8    017470            3082    3131#
SRM9    017676            3132    3176#
SRM9A   017740            3185#   3189
SRM9B   017774            3187    3193#
SRM9C   020074            3209    3215#   3218
SRM9C1  020052            3208#   3211
SRM90   020120            3216    3222#
STACK   001000             562     565     568     571     574     577     580     585#
START   001134             563     631#
S1      022420            3729#   4043
S10     022772            3801#   4076
S11     023046            3810#   4082
S12     023100            3816#   4088
S13     023203            3830#   4096
S14     023563            3878#   4102    4192
S14A    023663            3892#   4102
S15     023707            3897#   4108
S16     023756            3905#   4113    4119
S17     024032            3914#   4113
S18     024062            3919#   4119
S19     024102            3923#   4171    4179
S2      022542            3735#   4179    4282
S20     024127            3928#   4171    4179
S21     024162            3934#   4186
S22     024207            3939#   4186
S23     024247            3946#   4076    4082    4282    4289
S24     024274            3951#   4192
```

DZDTA.B CROSS REFERENCE TABLE -- USER SYMBOLS

```
S25     024326          3957#   4207
S26     024433          3970#   4050    4057    4064    4126    4133    4140    4147    4154    4161    4213    4220    4252
                        4259
S27     024504          3978#   4225    4282
S28     024573          3989#   4229
S29     024613          3993#   4233
S3      023504          3741#   4070    4197    4289
S30     024616          3995#   4237
S31     024636          3999#   4241    4245
S32     024657          4003#   4245    4269
S33     024664          4005#   4241    4245    4264    4269    4274
S34     024673          4008#   4166    4201
S35     024717          4013#   4166
S36     024730          4016#   4201
S37     024743          4019#   4264    4269    4274
S38     025001          4026#   4264
S39     025010          4029#   4274
S4      022533          3746#   4076    4179    4282
S40     025023          4032#   4282
S5      022547          3750#
S6      022561          3753#   4082    4289
S8      022662          3780#   4076    4082    4171    4179    4282    4289
S9      022675          3783#   4050    4057    4064    4070    4088    4096    4102    4108    4113    4119    4126    4133
                        4140    4147    4154    4161    4192    4213    4220    4252    4259
TCSR    001026           593#    693     705    2894    3595    3619    3640    3667    3673    3676    3715*   3723
TDBR    001030           594#   3597*   3621*   3642*   3669*   3675*   3678*   3725*
TESTX   021504           575    3566#
TEST1   001412           671     682#
TEST10  002540           847#
TEST11  002602           858#
TEST12  002644           914#
TEST13  003010           944#
TEST14  003104           963#
TEST15  003234           988#
TEST16  003330          1014#
TEST17  003544          1029    1034    1047    1049    1055#
TEST18  004000          1072    1078    1094    1096    1101#
TEST19  004234          1118    1124    1140    1142    1147#
TEST2   001654           732#
TEST20  004470          1164    1170    1186    1188    1193#
TEST21  004724          1210    1216    1232    1234    1239#
TEST22  005160          1256    1262    1278    1280    1285#
TEST23  005414          1302    1308    1324    1326    1333#
TEST24  005534          1357#
TEST25  005654          1382#
TEST26  006054          1418#
TEST27  006226          1448#
TEST28  006340          1468#
TEST29  006462          1490#
TEST3   001730           747#
TEST30  006606          1515#
TEST31  006734          1543#
TEST32  007062          1571#
TEST33  007236          1607#
TEST34  007400          1638#
TEST35  007526          1668#
```

DZDTA.B CROSS REFERENCE TABLE -- USER SYMBOLS

```
TEST36  010036           1736    1743#
TEST37  010074           1765#
TEST38  010442           1853#
TEST39  010522           1875#
TEST4   001754            755#
TEST40  010750           1926#
TEST42  011166           1699    1976#
TEST43  011432           2032#
TEST44  011664           2082#
TEST45  012040           2121#
TEST46  012200           2154#
TEST47  012340           2191#
TEST48  012522           2231#
TEST49  012710           2271#
TEST5   002064            777#
TEST50  013042           2117    2318#
TEST51  013274           2373#
TEST52  013526           2427#
TEST53  013756           2486    2490#
TEST54  014544           2576    2619#
TEST55  015332           2487    2705    2751#
TEST6   002134            792#
TEST6A  002252            821#
TEST7   002322            817     823     836#
TEST8   002410            856#
TEST9   002500            876#
TFLAG   001100            616#    641*   2886*
TIMERS  021176            578    3427#
TIMREQ  021214           3430#   3440
TIMRET  021224           3427    3434#
TINT14  003174            966     976#
TINT15  003276            990     996#
TINT16  003454           1016    1035#
TINT17  003676           1056    1079#
TINT18  004132           1102    1125#
TINT19  004366           1148    1171#
TINT20  004622           1194    1217#
TINT21  005056           1240    1263#
TINT22  005312           1286    1309#
TINT23  005474           1335    1344#
TINT24  005614           1359    1368#
TINT25  006022           1399    1408#
TINT26  006134           1420    1429#
TINT27  006316           1452    1461#
TINT28  006430           1473    1480#
TINT29  006554           1494    1505#
TINT30  006702           1519    1529#
TINT39  010726           1881    1917#
TIN25   005752           1389    1396#
TIN26   006174           1433    1438#
TKR     001032            595#   1552*  1560   1563*  1580*  1590   1595*  1616*  1625   1628*  1677*  1686   1689*
TNT39A  010634           1868    1899#
TNT39B  010722           1905    1915#
TOUT    022352           3708    3715#
TPC     021470           3541*   3542*  3543*  3544*  3545*  3546   3547#
TPTAB   021472           3545    3553#
```

DZDTA.B CROSS REFERENCE TABLE -- USER SYMBOLS

```
TRCK    016050            2834    2896#
TRET    001346             661     666#
TRPSRV  021432             554    3541#
TSTX    001106             619#    642*  3571#  3687   3695*
TST35A  007704            1692    1703#
TST3_B  007772            1726#
TST37A  010346            1827#
TTRAP   001044             557     600#   664*   666*
TYPE    022324            3449    3704#  3709
TYTMP   022350            3443*   3444*  3445*  3446*  3447*  3448*  3704   3707*  3710#
WAIT27= 006276            1456#   1457#
.       = 025572             549#    551#   556#   561#   564#   567#   570#   573#   576#   579#   584#   586#   646
                             648     652    655    665    675    687    691    694    697    699    703    706    709
                             717     720*   721    723    727    737    740    743    751    759    762    766    770
                             774     782    786    795    801    815    828    832    839    852    859    873    880
                             884     891    895    903    907    917    921    925    929    935    941    946    950
                             955     959    971    977    984    994    995   1002   1025   1031   1036   1040   1063
                            1067    1074   1080   1084   1109   1113   1120   1126   1130   1155   1159   1166   1172
                            1176    1201   1205   1212   1218   1222   1247   1251   1258   1284   1268   1293   1297
                            1304    1310   1314   1340   1345   1352   1364   1369   1376   1386   1405   1414   1425
                            1430    1444   1456   1458   1486   1501   1511   1526   1536   1549   1555   1557   1561
                            1566    1577   1584   1587   1591   1598   1600   1613   1619   1622   1626   1631   1633
                            1648    1653   1659   1663   1674   1684   1687   1695   1706   1710   1712   1718   1731
                            1749    1756   1773   1778   1782   1788   1792   1799   1801   1805   1809   1814   1816
                            1820    1824   1836   1842   1846   1859   1864   1869   1898   1902   1931   1942   1944
                            1948    1957   1961   1963   1980   1983   1989   1994   2006*  2007   2009   2015   2028
                            2034    2040   2045   2057*  2058   2060   2066   2079   2084   2093   2105*  2106   2108
                            2113    2116   2130   2142*  2143   2145   2150   2164   2176*  2177   2179   2184   2203
                            2216*   2217   2219   2223   2228   2244   2257*  2258   2260   2264   2268   2282   2294*
                            2295    2297   2302   2320   2327   2332   2342*  2343   2346   2351   2368   2375   2382
                            2387    2397*  2398   2401   2406   2423   2429   2436   2441   2451*  2452   2455   2460
                            2467    2481   2492   2504   2525*  2526   2538   2531   2534   2539   2541   2553   2560
                            2563    2569   2575   2589*  2590   2607*  2608   2614   2621   2633   2654*  2655   2657
                            2660    2663   2668   2670   2682   2689   2692   2698   2704   2718*  2719   2736*  2737
                            2743    2758   2760   2776   2784   2793   2796   2815*  2816   2833   2842   2849   2851
                            2854    2862   2866   2891   2895   2905   2908   2911   2917   2920   2927   2930   2937
                            2940    2949   2954   2960   2974   2978*  2979   2983   2993   2998   3020   3024*  3025
                            3029    3039   3044   3065   3069*  3070   3074   3084   3088   3101   3105   3116   3120*
                            3121    3125   3136   3138   3153*  3154   3157   3165   3171   3179   3183   3194   3196
                            3200    3202   3207   3220   3223   3234   3238*  3239   3243   3253   3265   3268   3272
                            3283    3287*  3288   3292   3304   3307   3312   3317   3322   3327   3338   3341   3346
                            3349    3353   3358   3366   3370   3372   3437   3573   3575   3584   3596   3602   3620
                            3630    3652   3668   3674   3677   3705   3717   3720   3724   4040#
```

DZDTA.B CROSS REFERENCE TABLE -- MACRO NAMES

```
COMMEN      1#
ENDCOM      1#
ESCAPE      1#
GETPRI      1#
GETSWR      1#
INT      1053#   1054    1100    1146    1192    1238    1284
MULT        1#
NEWTST      1#
PFAIL1    621#   1990    2041    2089    2126    2160
PFAIL2    622#   2195    2236
POP         1#
PUSH        1#
REPORT      1#
SBFAIL   2477#   2490    2619
SETPRI      1#
SETUP       1#
SKIP        1#
SLASH       1#
SRPFCK    624#   2966    3012    3057    3108    3226    3275
STARS       1#
SWFAIL   2315#   2318    2373    2427
SWRSU       1#
TYPBIN      1#
TYPDEC      1#
TYPNAM      1#
TYPNUM      1#
TYPOCS      1#
TYPOCT      1#
TYPTXT      1#
$$ESCA      1#
$$NEWT      1#
$$SKIP      1#
.EQUAT      1#
.HEADE      1#
.KT11       1#
.SETUP      1#
.SWRHI      1#
.$ACTI      1#
.$APTB      1#
.$APTH      1#
.$APTY      1#
.$ASTA      1#
.$CATC      1#
.$CMTA      1#
.$DB2D      1#
.$DB20      1#
.$DIV       1#
.$EOP       1#
.$ERRO      1#
.$ERRT      1#
.$MULT      1#
.$POWE      1#
.$PWRO      1#
.$RDOE      1#
.$RDOC      1#
.$READ      1#
```

DZDTA.B CROSS REFERENCE TABLE -- MACRO NAMES

```
.$R2AZ          1#
.$SAVE          1#
.$SB2D          1#
.$SB2O          1#
.$SCOP          1#
.$SIZE          1#
.$SJPR          1#
.$TRAP          1#
.$TYPB          1#
.$TYPO          1#
.$TYPE          1#
.$TYPO          1#
.$40CA          1#
.1170           1#
```

DZDTA.B CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

ADC	1936	3634	3658												
ADD	1935	1952	3447	3545	3569	3707									
ASL	1939														
BEQ	646	652	655	675	685	687	691	699	703	709	723	740	751	766	770
	782	801	929	946	950	1405	1549	1557	1577	1587	1613	1622	1648	1653	1659
	1674	1684	1692	1718	1731	1805	1809	1820	1836	1839	1859	1864	1869	1931	1957
	2009	2015	2060	2066	2108	2113	2116	2145	2150	2179	2184	2219	2223	2260	2264
	2297	2302	2346	2351	2401	2406	2455	2460	2479	2486	2504	2528	2531	2534	2541
	2563	2633	2657	2660	2663	2670	2692	2758	2770	2776	2778	2796	2842	2866	2872
	2911	2915	2925	2935	2947	2954	2960	2991	3002	3037	3047	3082	3088	3101	3132
	3146	3157	3165	3177	3183	3216	3251	3260	3302	3312	3322	3336	3346	3353	3364
	3377	3573	3584	3636	3638	3652									
BIC	878	889	900	953	968	1018	1059	1105	1151	1197	1243	1289	1337	1361	1383
	1391	1400	1422	1434	1453	1474	1495	1520	1547	1575	1611	1646	1657	1672	1682
	1856	1880	1893	1908	2561	2690	2782	2794	3156	3310	3320	3344	3351	3415	3574
	3660														
BICB	3715														
BIS	701	715	756	778	888	899	948	965	989	1015	1022	1057	1060	1103	1106
	1149	1152	1195	1198	1241	1244	1287	1290	1334	1358	1388	1392	1419	1450	1454
	1471	1475	1492	1496	1517	1521	1552	1553	1582	1679	1716	1729	1790	1883	1887
	1895	1907	1911	2554	2683	2786	2938	2979	3005	3045	3050	3367	3576	3661	
BIT	645	651	654	696	711	716	722	726	742	761	773	785	814	822	827
	831	851	872	883	894	906	916	920	924	928	940	945	949	954	958
	983	1001	1024	1039	1066	1083	1112	1129	1158	1175	1204	1221	1250	1267	1296
	1313	1351	1375	1413	1443	1485	1510	1535	1554	1556	1560	1565	1583	1586	1590
	1597	1618	1621	1625	1630	1652	1662	16[illegible]5	1717	1730	1748	1755	1823	1838	1841
	1[illegible]45	1901	1930	1941	1960	2027	2078	2227	2267	2367	2422	2435	2466	2503	2527
	2[illegible]2	2559	2574	2613	2632	2656	2681	2688	2703	2742	2767	2769	2775	2777	2783
	2792	2832	2840	2888	2907	2914	2919	2924	2929	2934	2939	2946	2953	2957	2959
	2973	2992	2990	3003	3008	3019	3028	3036	3048	3053	3064	3073	3081	3087	3093
	3100	3104	3115	3124	3131	3137	3145	3170	3176	3182	3185	3188	3193	3206	3208
	3210	3215	3217	3222	3233	3242	3250	3264	3267	3271	3282	3291	3301	3326	3335
	3348	3357	3363	3371	3376	3572	3583	3585	3683	3685					
BMI	795	817	839	859	880	891	903	977	1031	1036	1045	1074	1080	1089	1120
	1126	1135	1166	1172	1181	1212	1218	1227	1258	1264	1273	1304	1310	1319	1345
	1369	1386	1430	1501	1695	1706	1710	1736	1788	1799	1801	1816	1944	2436	2569
	2698	2849	2854	2889	3092	3259	3437								
BNE	697	712	717	721	727	743	762	764	774	786	815	823	828	832	852
	873	884	895	907	917	921	[illegible]	941	965	959	984	1002	1025	1040	1067
	1084	1113	1130	1159	1176	1206	[illegible]	[illegible]	[illegible]	[illegible]	1314	1352	1376	1414	1444
	1458	1486	1511	1536	1555	1561	[illegible]	[illegible]	1591	[illegible]	1619	1626	1631	1663	1687
	1749	1756	1824	1842	1846	1902	[illegible]	[illegible]	[illegible]	[illegible]	2007	2020	2034	2058	2079
	2084	2106	2143	2177	2217	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	2343	[illegible]	2375	2398	2423
	2429	2452	2467	2481	2492	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	2590	2608	2614	2621	2655
	2668	2682	2689	2704	2719	2737	[illegible]	[illegible]	[illegible]	2780	2784	2793	2800	2816	2833
	2837	2862	2905	2908	2917	2920	2927	[illegible]	2937	2940	2949	2958	2974	2979	2983
	2993	3004	3009	3020	3025	3029	3039	3049	3054	3065	3070	3074	3084	3094	3105
	3116	3121	3125	3136	3138	3154	3171	3179	3187	3189	3194	3196	3200	3207	3209
	3211	3218	3223	3234	3239	3243	3253	3265	3272	3283	3288	3292	3304	3317	3327
	3338	3349	3358	3370	3372	3586	3610	3646	3684	3686	3688	3705	3717	3720	
BPL	694	706	737	759	971	994	1021	1029	1049	1063	1072	1096	1109	1118	1142
	1155	1164	1188	1201	1210	1234	1247	1256	1280	1293	1302	1326	1340	1364	1425
	1526	1600	1633	1773	1778	1792	1814	1938	1948	1963	1980	1989	2040	2327	2382
	2626	2897	2895	2998	3044	3202	3307	3341	3366	3596	3602	3620	3630	3641	3668
	3674	3677	3690	3724											
BR	629	636	638	648	665	689	768	806	843	867	935	975	995	1034	1047

DZDTA.B CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

```
                1078  1094  1124  1140  1170  1186  1216  1232  1262  1278  1308  1324  1343  1367  1395
                1407  1428  1437  1460  1479  1504  1528  1551  1579  1615  1650  1676  1712  1782  1833
                1924  1914  1916  1994  2022  2045  2073  2093  2130  2164  2203  2244  2282  2332  2382
                2417  2417  2441  2510  2548  2576  2594  2639  2677  2705  2723  2760  2774  2803  2851
                2876  2860  2864  2868  2891  3220  3440  3575  3662  3709  3722  3727
CLC             3410
CLR              625   631   632   639   640   641   642   643   644   649   650   659   660   662   719
                 725   734   743   749   772   784   812   813   826   849   850   870   871   882   893
                 935   939   957   964   974   980   982   998  1000  1023  1027  1038  1042  1045  1069
                1092  1096  1111  1115  1128  1132  1157  1161  1174  1178  1203  1207  1220  1224  1249
                1283  1286  1270  1293  1293  1312  1316  1340  1350  1372  1374  1410  1412  1440  1441
                1455  1463  1484  1503  1483  1507  1508  1532  1533  1563  1564  1595  1596  1617  1628
                1629  1651  1661  1683  1683  1698  1698  1704  1720  1786  1832  1840  1852  1900  1920
                1932  1933  1954  2003  2004  2025  2026  2050  2055  2056  2076  2077  2093  2103  2104
                2125  2140  2141  2173  2174  2215  2216  2230  2232  2235  2256  2276  2286  2322  2333
                2341  2345  2345  2396  2396  2420  2421  2450  2464  2465  2559  2564  2571  2573  2573
                2587  2608  2625  2612  2638  2653  2700  2702  2716  2717  2734  2735  2741  2752  2752
                2788  2824  2831  2903  2906  2909  2952  2977  2995  3023  3041  3068  3086  3119  3119
                3134  3152  3171  3237  3255  3286  3325  3356  3378  3428  3429  3566  3603  3626  3627
                3643  3653  3665  3705
CLRB             760   780  1476  1582  1807  2551  2680  3205  3446  3544
CMP              667   686   690   702   765   769   781   800   807   844   868   937   979   997  1030
                1043  1048  1073  1087  1095  1119  1133  1141  1165  1179  1187  1211  1225  1233  1257
                1271  1279  1303  1317  1325  1347  1371  1398  1404  1409  1432  1439  1452  1491  1506
                1531  1548  1576  1612  1647  1658  1673  1683  1783  1804  1808  1819  1835  1868  1863
                1899  1915  1919  1956  2002  2008  2023  2053  2059  2074  2101  2138  2144  2149  2172
                2178  2183  2212  2218  2222  2253  2259  2263  2280  2301  2340  2344  2363  2395  2399
                2418  2449  2453  2521  2529  2533  2540  2549  2553  2603  2620  2658  2662  2669  2678
                2714  2732  2813  2854  3001  3030  3046  3075  3126  3151  3156  3244  3263  3311  3321
                3345  3352  3434  3589  3637  3645  3689  3692
CMPB            3719
COM             2023  2026  3414  3416  3418
DEC              720  1457  1581  2015  2057  2105  2142  2176  2216  2257  2294  2342  2397  2451  2505
                2538  2589  2607  2614  2667  2718  2736  2815  2904  2916  2926  2936  2948  2978  2992
                3024  3038  3069  3083  3120  3135  3153  3178  3195  3199  3238  3252  3287  3303  3337
                3369
EMT             3485  3496  3497  3498  3499  3500  3501  3502  3503  3504  3505  3506  3507  3508  3509
                3510  3511  3512  3513  3514  3515  3516  3517  3518  3519  3520  3521  3522  3523  3524
                3525  3526  3527  3528  3529  3530  3531  3532  3533  3534  3535  3536
HALT             549  1642  1658  1713  1715  1722  1728  1734  1739  1747  1753  1769  1797  1830  1857
                1867  1879  1901  1913  1915  1936  1945  2037  2049  2087  2097  2124  2134  2158  2168
                2194  2199  2208  2215  2230  2249  2273  2286  2324  2336  2379  2391  2433  2445  2483
                2496  2514  2520  2582  2625  2643  2709  2727  2762  2802  2806  2830  2839  2846  2880
                2928  3014  3059  3110  3147  3176  3277  3393  3402  3408  3420  3567  3570  3603
INC              653   877   915   919   923   967   982  1401  1470  1491  1497  1544  1585  1608  1620
                1643  1655  1680  1812  1951  3631  3644  3691  3726
INCB             656   837
JMP              563   566   569   572   575   578   581  1602  1634  1699  1966  1981  2117  2484  2487
                2621  2634  2641  2931  2941  2965  2975  3003  3011  3021  3031  3056  3066  3076  3099
                3107  3117  3127  3141  3172  3192  3225  3235  3245  3266  3274  3284  3294  3328  3359
                3373  3379  3430  3577  3694
JSR              627   628   633   634   637  1093  1139  1185  1231  1277  1323  2858  2859  2874  2884
                2922  3449  3731  3834  3839  3708  3721
MOV              502   565   568   571   574   577   630   625   647   657   658   661   664   666   668
                 670   671   673   713   714   728   733   735   748   757   779   793   797   798   799
                 811   824   825   841   842   848   857   861   862   869   931   932   933   938   966
```

DZDTA.B CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

```
                967  969  972  981  990  991  992  999 1016 1017 1019 1026 1041 1046 1056
               1058 1061 1064 1068 1085 1090 1092 1102 1104 1107 1110 1114 1131 1136 1138
               1148 1150 1153 1156 1160 1177 1182 1184 1194 1196 1199 1202 1206 1223 1228
               1230 1240 1242 1245 1248 1252 1269 1274 1276 1286 1298 1291 1294 1298 1315
               1330 1322 1335 1336 1338 1341 1346 1359 1360 1362 1365 1373 1384 1389 1390
               1394 1399 1403 1411 1420 1421 1423 1426 1433 1436 1442 1449 1451 1462 1464
               1465 1469 1472 1473 1478 1484 1488 1488 1499 1509 1516 1518 1519 1524 1534
               1545 1546 1572 1573 1574 1580 1609 1610 1616 1639 1644 1645 1656 1669 1670
               1671 1677 1681 1[illegible] 1773 1780 1[illegible] 1[illegible] 1[illegible] 1833 1834 1881 1882 1884 1[illegible]
               1905 1906 1921 1[illegible] 1946 1987 1[illegible] 1[illegible] 1[illegible] 1996 1997 1999 2001 2003 2011
               2019 2020 2024 2[illegible] 2041 2042 2[illegible] 2[illegible] 2[illegible] 2050 2052 2054 2069 2070 2071
               2075 2089 2[illegible] 2[illegible] 2096 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2126 2127 2131 2132 2[illegible] 2[illegible]
               2137 2139 2[illegible] 2[illegible] 2165 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2171 2173 2135 2196 2202 2[illegible] 2[illegible]
               2207 2[illegible] 2[illegible] 2[illegible] 2236 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2230 2252 2254 2[illegible] 2[illegible]
               2283 2[illegible] 2[illegible] 2[illegible] 2289 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2334 2335 2337 2[illegible] 2[illegible]
               2356 2357 2358 2364 2380 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2382 2391 2409 2[illegible] 2[illegible]
               2413 2419 2434 2437 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2497 2498 2[illegible] 2[illegible]
               2511 2512 2513 2518 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2566 2572 2577 2[illegible]
               2579 2582 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2[illegible] 2628 2637 2640 2641
               2642 2647 2649 2651 2665 2673 2674 2679 2684 2695 2701 2706 2707 2708 2711
               2713 2715 2721 2726 2728 2731 2733 2753 2754 2787 2804 2805 2810 2812 2843
               2871 2881 2890 2893 2918 2928 2935 2951 2964 2966 2[illegible] 2969 2972 2976 2981
               2994 2996 3010 3012 3013 3015 3019 3022 3027 3040 3042 3055 3057 3058 3060
               3063 3067 3072 3[illegible] 3[illegible] 3[illegible] 3[illegible] 3108 3109 3111 3114 3118 3123 3133 3140 3[illegible]
               3142 3143 3145 3[illegible] 3[illegible] 3[illegible] 3[illegible] 3[illegible] 3191 3197 3224 3226 3227 3229 3232 3[illegible]
               3241 3254 3[illegible] 3[illegible] 3[illegible] 3[illegible] 3[illegible] 3278 3281 3285 3[illegible] 3[illegible] 3[illegible] 3309 3314
               3318 3319 3[illegible] 3[illegible] 3[illegible] 3[illegible] 3[illegible] 3406 3412 3413 3417 3427 3430 3443 3445
               3448 3541 3[illegible] 3[illegible] 3[illegible] 3[illegible] 3582 3587 3588 3590 3592 3553 3597 3598 3600
               3616 3621 3624 3[illegible] 3[illegible] 3642 3647 3648 3659 3669 3675 3678 3693 3697 3704
MOVB           1818 3725
NEG            1950
NOP            1393 1402 1435 1477 1498 1523 1885 1886 1894 1909 2567 2696 2875 2876 2877
RESET           695  707 2873
ROL            1940 3632 3633 3655 3656 3657
RTI             600  666 2896 3450 3604 3698
RTS             669 3421 3622 3649 3670 3679 3706 3718
RTT             664
SBC            1953
SEC            3[illegible]54
SUB            3[illegible]44 3542
TRAP           3548 3549 3550 3551 3[illegible]52
TST             663  674  684  698  708  750  763  816 1028 1044 1070 1088 1116 1134 1162
               1180 1208 1226 1254 1272 1300 1318 1599 1632 1691 1694 1705 1709 1735 1772
               1787 1791 1800 1815 1868 1937 1947 1954 1962 1977 1982 2014 2033 2065 2083
               2107 2112 2115 2[illegible]6 2319 2350 2374 2405 2428 2459 2490 2491 2562 2620 2691
               2755 2795 2799 2836 2848 2853 2861 2910 3164 3316 3365 3601 3617 3629 3635
               3[illegible]51 3[illegible]7
TSTB            693  705  736  73[illegible] 758  794  838  858  879  890  902  970  976  993 1020
               1035 10[illegible]2 1079 11[illegible] 1125 1154 1171 1200 1217 1246 1263 1292 1309 1339 1344
               1363 1[illegible]8 1[illegible]5 1[illegible]4 1429 1500 1525 1777 1798 1813 1943 1988 2039 2326 2381
               2477 2[illegible]5 2[illegible] 2[illegible]47 2757 2779 2[illegible]5 2894 2997 3043 3090 3201 3257 3306 3340
               3[illegible]36 3[illegible]5 3619 3[illegible]40 3667 3673 3676 3716 3723
WAIT           3432
.ABS              1
.ASCII         3[illegible]16 3830 3840 3849 3[illegible]0 3878 3993
.ASCIZ         3729 3735 3741 3746 3[illegible]0 3753 3757 3759 3761 3763 3766 3768 3770 3772 3775
```

F08

```
DZDTA-B MACY11 27(732)  27-OCT-76  15:57  PAGE 100
DZDTA.B CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

          3778    3780    3783    3790    3792    3795    3798    3801    3810    3822    3871    3887    3892    3897    3905
          3914    3919    3923    3928    3934    3939    3946    3951    3957    3970    3978    3989    3995    3999    4003
          4005    4008    4013    4016    4019    4026    4029    4032
.ENABL       1
.END      4293
.ENOC     2328    2366    2383    2421    2437    2465
.EVEN     4040
.IFF      2328    2383    2434
.IFNZ     2325    2356    2380    2411    2434    2465
.LIST        1     549
.MACR      621     622     624    1053    2315    2477
.MACRO       1
.NLIST       1     549
.REM         1
.REPT      549    2336    2391    2445
.TITLE       1
.WORD     4043    4050    4057    4064    4070    4076    4082


ERRORS DETECTED:  0
DEFAULT GLOBALS GENERATED:  0

*,NOM.SEQ/SOL/CRF/NL:TOC/PAGNUM=SYSMAC.CO,DZDTA.B
RUN-TIME:  33 46 5 SECONDS
RUN-TIME RATIO: 342/87=3.9
CORE USED:  36K  (71 PAGES)
```